Zendex®

ZX-80/05 SINGLE BOARD COMPUTER

HARDWARE REFERENCE MANUAL

SEE CORRECTIONS on SKEMOS

Ordering Information

Part No.	Description
ZX-80/05	Single Board Computer (Comes without EPROM and RS232 Interface Chips) Manual Supplied

Zendex Corporation 6680 SIERRA LANE, DUBLIN, CA 94566, 415/829-1284

Zendex corporation

6680 Sierra Lane • Dublin, California 94566 • 415/829-1284

WARRANTY

All products are warranted against defects in material and workmanship under normal and proper use and in their original unmodified condition. If found defective by Zendex Corp. within the terms of this warranty, Zendex Corp.'s sole obligation shall be to repair or replace at Zendex Corp.'s option the defective product. If Zendex Corp. determines that the product is not defective within the terms of this warranty, customer shall pay all costs of handling and return transportation. All replaced products become the property of Zendex Corp. As a condition of this warranty, customer must obtain a Zendex Corp. Return Material Authorization Number, and must return all products, transportation prepaid and insured, to Zendex Corp.'s Dublin, CA facility or other specified location.

Transportation charges for the return to customer shall be paid by Zendex Corp. within the contiguous United States only. These warranties outside the contiguous United States are limited to repair or replacement only and exclude all costs of shipping, customs clearance, and other related charges. Except for the express warranties stated above, Zendex Corp. disclaims all warranties on products, including all implied warranties of merchantability and fitness; and the stated express warranties are in lieu of all obligations or liabilities on the part of Zendex Corp. for damages, the use or performance with this product.

Warranty period is one (1) year from date of original shipment.

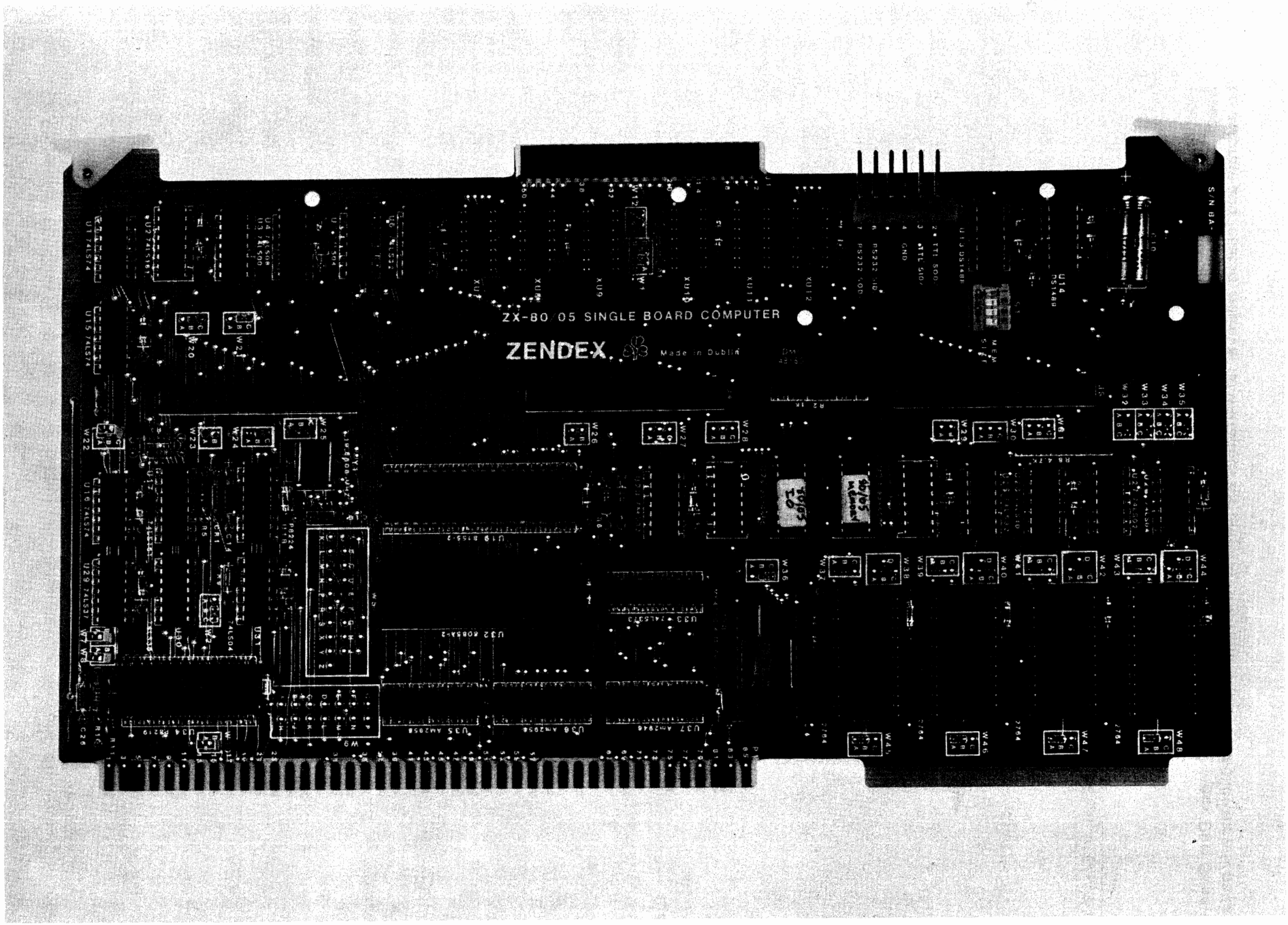
SERVICE POLICY

If a product should fail during the warranty period, it will be repaired for free. There will be a service charge for repair of a product after the warranty period. If a product exhibits misuse, negligence, or user misconnection, the failure will be treated as an out-of-warranty repair. Repair is performed at the factory only, typically with a 72-hour turnaround time.

To return a product for in-warranty repair, first reverify that the unit is indeed at fault. Then, call the factory for Return Material Authorization (RMA) Number. The product should be carefully packaged and shipped prepaid showing the RMA number on the outside of the package. Include a short statement of the malfunction, along with return address information, and the telephone number of a technical contact, in case the need arises.

For out of warranty repairs, a purchase order for repair charges must also be included. These repairs are charged on a time and material basis.

Items should not be returned air freight collect, as they cannot be accepted. It is absolutely necessary to return products in the manner stated here, otherwise considerable delay will result in processing the return.


ZX-80/05 SINGLE BOARD COMPUTER
ZENDEX.
Made in Dublin

C O N T E N T S

CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

The Zendex ZX-80/05 Single Board Computer is a member of the Zendex family of MULTIBUS compatible CPU boards. The ZX-80/05 contains a central processor unit (8085A-2), 1K x 8 of static RAM, sockets for up to 32KB of EPROM, flexible interchangeable parallel I/O capability (22 lines), serial I/O capability (via SID and SOD of the 8085A-2), hardware programmed interrupt (4 levels) and on-board timer capability. Sockets are provided for interchangeable I/O drivers (inverting,noninverting and open collector.) In addition, the ZX-80/05 capabilities can be further expanded using any of a variety of the ZBX multi-modules provided by Zendex and plug-compatible directly with the ZX-80/05 baseboard. These Intel standard SBX™ compatible modules plug directly into the SBC Jacks J3, J4 and J5. MULTIBUS arbitration control logic is also provided on the ZX-80/05 board.

1.2 LOGIC DESCRIPTION

1.2.1 CPU

An on-board 8085A-2 CPU at (U32) controls the operations of the ZX-80/05. The 8085A-2 is an 8 bit n channel CPU which is fully compatible with the popular 8080A, yet runs at a higher basic clock rate. The 8085A-2 contains six 8 bit general purpose registers (B,C,D,E,H,L) and one 8-bit accumulator for data manipulation. A 16-bit program counter provides for direct addressing of up to 64K of memory. Also, a 16-bit stack pointer tracks the current hardware stack address anywhere in the 64K address space.

Several 8085A-2 instructions, as well as the interrupt control logic, manipulate the stack pointer to preserve and restore pertinent state information when interrupts occur or subroutine calls are made. The stack can also be used by the current program when a last in/first out data structure is required.

The 8085A-2 Program Status Word contains flags which reflect the current status of the arithmetic operations performed. Since general purpose registers can also be addressed in pairs (BC, DE, HL), double precision as well as single precision arithmetic is provided.

The 8085A-2 can be run at a basic clock rate of 4.915 MHZ or 1.966 MHZ depending on an on-board jumper which is user selectable. A 19.6608 MHZ crystal (at U18) will be divided by 2 at (U15) and placed on the XI input of the 8085A-2 where an additional divide by 2 provides the 4.915 MHZ CPU rate in the higher speed mode. In the lower speed mode, the crystal frequency is divided by 2.5 at (U17) and divided by 2 at (U15) and placed on the 8085A-2 X1 input where the additional divide by 2 provides the 1.966 MHZ CPU rate.

1.2.2 RAM

1K of Random Access Memory is provided for by an on-board MK4118 static RAM device at (U38). This device operates with an access time of 250 nsec (cycle time = 250 nsec) on a single +5V supply. Since the RAM is socket mounted, an MK4802 can be substituted in order to provide 2K of static RAM. The sockets provided for EPROM can also be used for 4118 or 4802 RAM devices if a total RAM system (up to 10K bytes) is desired. (See Figure 1-1 for details of Memory Map).

1.2.3 EPROM

Four sockets are provided at (U39, U40, U41, and U42) for EPROM devices 2716, 2732 or 2764. These 28-pin sockets allow for the 24 pin 2716/2732 devices as well as the 28 pin 2764. Also, static RAM (above) may be implemented using these sockets. Depending on the EPROM used, cycle

FIGURE 1-1

MEMORY MAP

EPROM (on board)	0000H - 1FFFH*	(2716) Sockets Full
	0000H - 3FFFH	(2732)
	0000H - 7FFFH	(2764)
RAM (on board)	3C00H - 3FFFH	Jumper Selectable Full Mo
(MK 4118)	7C00H - 7FFFH	2732 System
	BC00H - BFFFH	2764 System
	3E00H - 3FFFH	(Intel SBC Equiv)
MEMORY (off board)	0000H - FFFFH	

NOTE: Memory configurations are switch and jumper selectable for various memory device and address combinations.

*For example, could be populated with static RAM in place of 2716 EPROMS.

times vary from 350 ns to 650 ns using a single +5V supply. The EPROMS are ultraviolet erasable and electrically programmable using Zendex MULTIBUS SBC compatible Prom Programmer Module (ZX-908) or development system option ZX-909 thus greatly facilitating low cost program development and installation.

1.2.4 Parallel I/O

The on-board 8155-2 device at (U19) provides 22 programmable parallel I/O lines and a 14-bit counter timer using a single 5V supply. (Note: the on-chip RAM of the 8155-2 is not used for any ZX-80/05 board functions.) The 22 I/O lines can be viewed as two 8-bit I/O ports (A and B) and one 6-bit I/O port (C). A typical application might use one of the ports as status (C), allowing handshake operations utilizing the remaining two ports (A and B). The input/output/status functions of these bits is fully programmable. (Note that the AD Ø-7 lines are tri-state lines that address on-chip RAM, address I/O, or contain memory data depending on the condition of the IO/$\overline{M}$ and $\overline{WR}$ and $\overline{RD}$ lines.) The parallel lines are brought out to a 50-pin edge connector, J1. Optional SBX multi-modules provide for additional parallel I/O utilizing 8255A devices to add three 8-bit ports to the baseboard for each of the three available SBX stations on the ZX-80/05 for a total of three sets of 24 programmable parallel I/O lines. Four 14-pin DIP sockets per module are provided to receive user installed drivers (7438 typ.) or resistor terminators (SBC-901 typ.).

1.2.5 Serial I/O

The SID and SOD lines of the 8085A-2 are used to implement serial I/O (RS232 or TTL). These lines are controlled exclusively by software through the RIM and SIM instructions of the 8085 instruction set. Baud rates are software generated. The ZX-80/05, due to its enhanced clock rate, provides for greater flexibility in baud rate generation than does its SBC equivalent.

The program, by using SIM and RIM and a software delay, does serial bit-by-bit I/O at calculated baud rates on the SID and SOD lines. RS232 and TTL serial I/O are brought out on connector J2. TTL serial R/O is also brought out on edge connector J1. Optional SBX multimodules provide for additional serial I/O utilizing 8251A devices.

1.2.6 Interrupts

By steering various request lines using on-board jumpers, 4 interrupt request levels can be presented to the 8085A-2 TRAP, RST7.5, RST6.5 and RST5.5 inputs, in order of priority, TRAP highest. Among the inputs to the jumper selection stake pins are the eight MULTIBUS interrupt signals (INTØ - INT7), as many as three of the various SBX module interrupt requests, the timer interrupt request, the two parallel I/O interrupt requests, and an external interrupt provided at pin 49 of edge connector J1, a total of 15 sources. Since multiple requests may be tied to a single 8085A-2 level, the interrupt handling routines may require polling to determine the requesting device.

1.2.7 Timer

The 8155-2 at (U19) contains a 14-bit down counter that counts pulses presented at Timer IN (pin 3) of the device. Four different modes of operation are programmable, allowing for the following timer out wave shape:
1) Continuous pulses (i.e. real time clock), 2) Single pulse at terminal count (watchdog timer) 3) Continuous square wave (peripheral control) and 4) Single square wave (process control).

The initial timer value is loaded via the program by accessing a pair of I/O addresses (Base +4 and Base +5). The Mode (01-04) is loaded in the 2 most significant bits of the most significant byte. The remaining 14 bits contain the timer value.

Starting and stopping the timer is performed by using bits 6 and 7 of the 8155-2 command register.

1.2.8 Line Drivers/Terminators

Sockets provided at (XU7, XU8, XU9, XU10, XU11, XU12) are compatible for a variety of line driver/terminator devices. These devices may be inverting, noninverting or open collector (see table 1-1) depending on application characteristics. The inputs to these devices are from the 8155-2 at (U19) while the outputs are presented to edge connector J1. Sockets (U13 and U14) are provided for RS232 drivers and receivers for serial I/O.

1.2.9 SBX Type Expansion

Three Intel standard plug-compatible SBX-type connectors (J3, J4, J5) are provided for system expansion on the ZX-80/05 board. The Zendex product line includes various ZBX type multi-modules which plug into these connectors to provide additional I/O capabilities. (Refer to the Zendex Product catalog for the growing list of these modules).

The SBX bus is in reality an on-board extension of the CPU bus. This low-cost method of expansion precludes the necessity of using the MULTIBUS™ standard to interface to additional I/O logic. The SBX™ (Zendex ZBX) type modules simply plug into J3, J4 and J5 of the baseboard (ZX-80/05 SBC) to provide inexpensive yet versatile I/O configurations - all on a single PC board. The SBX™ bus provides the control lines, data lines, interrupt lines, address and chip select lines, and power lines necessary for operation of the plug-in modules. The reader should refer to Intel iSBX Bus Specs. (Manual 142686-001) for further discussion of the SBX bus. (See table 4-1) Reference section 4-1.

1.2.10 MULTIBUS/Access Arbitration

The ZX-80/05 board contains all the necessary logic to interface to the MULTIBUS™ standard. The MULTIBUS has become an industry standard for microprocessor applications

(see table 1-2 for pin assignments). The ZX-80/05 is fully MULTIBUS compatible. By using Zendex's full line of MULTIBUS compatible boards (SBC, Memory, I/O, Display and other), the user can expand his system to meet current and future needs of his application.

Using the MULTIBUS backplane implemenation for system expansion provides the user with a synchronous data transfer capability between a "Master" and a "Slave" device. The controlling master, in the serial priority scheme provided on the ZX-80/05, resolves bus contention by asserting its bus priority out signal false (high), thereby inhibiting the bus priority in signal to lower priority devices when the master seeks to control the MULTIBUS. The highest priority device in any system should have its bus priority in (BPRN/) tied to ground therefore granting itself the ability to seize MULTIBUS control at any time. A maximum of three bus arbitration devices can be used serially on any system. This type of scheme is required since more than one time critical device (diskette controller, DMA device) asynchronously can request the bus. Bus arbitration, in effect, synchronizes the utilization of system resources.

If more than three masters are required, a parallel bus arbitration scheme must be used. In this case, bus priority in (BPRN/) is determined by an encoder/decoder arrangement utilizing bus request (BREQ/) and disabling the (BPRØ) signal on all master modules. The devices selected for such a scheme are left to the designer's discretion with the obvious restriction that only one bus master be given control at a time.

1.3 Program Development

The user's environment and experience will dictate the manner in which programs which will function on the ZX-80/05 are to be developed. In some cases, the user may already have a microprocessor development system that is quite similar to an Intellec MDS-800 or Series II, such as MDS-220,-221 or -235.

In such cases, programs may be developed under ISIS™ or CP/M™ with the resulting absolute code "down-loaded" to the ZX-80/05 RAM or programmed into EPROM using a Prom Programmer system, possibly the low-cost Zendex ZX-908 Programmer Module, or the ZX-909 option for Zendex Series 800 complete development systems. In the latter case, this procedure is greatly simplified since both the ZX-908 and ZX-909 are MULTIBUS compatible. Zendex provides CP/M V2.2 programs necessary to program various EPROM devices. The final programmed EPROMS are easily then transferred (plugged) into the target system.

It is at the user's discretion to determine his most expeditious method of development and debug of his final system. Evaluation of various software (DDT) and hardware (ICE85) tools aid in that decision-making process.

TABLE 1-1

LINE DRIVERS AND TERMINATORS

IO Drivers - The following line drivers are all compatible with the IO Driver sockets on the ZX-80/05

Driver	Characteristic	Sink (mA)
7438	I OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

I = Inverting
NI = Non-inverting
OC = Open Collector

TABLE 1-2

Connector P1 Pin Assignments

Pin*	Signal	Function
1	GND	Ground
2	GND	
3	+5 VDC	Power Input
4	+5 VDC	
5	+5 VDC	
6	+5 VDC	
7	+12 VDC	Power Input
8	+12 VDC	
9	-5 VDC	Power Input
10	-5 VDC	
11	GND	Ground
12	GND	
13	BCLK/	Bus Clock (9.8304MHz)
14	INIT/	System Initialize
15+	BPRN/	Bus Priority In
16	BPRO	Bus Priority Out
17	BUSY/	Busy
18	BREQ/	Bus Request
19	MRDC/	Memory Read Command
20	MWTC/	Memory Write Command
21	IORC/	I/O Read Command
22	IOWC/	I/O Write Command
23	XACK/	Transfer Acknowledge
24		
25		
26		
27		
28		
29		
30		

TABLE 1-2 (CONTINUED)

Connector P1 Pin Assignments

Pin*	Signal	Function
31	CCLK/	Constant Clock (9.8304 MHz)
32		
33		
34		
35	INT6/	Interrupt request line 6
36	INT7/	Interrupt request line 7
37	INT4/	Interrupt request line 4
38	INT5/	Interrupt request line 5
39	INT2/	Interrupt request line 2
40	UBT3/	Interrupt request line 3
41	INT0	Interrupt request line 0
42	INT1/	Interrupt request line 1
43	ADRF/	
44	ADRF/	
45	ADRC/	
46	ADRD/	
47	ADRA/	
48	ADRB/	
49	ADR8	
50	DR9/	
51	ADR6/	— Address bus
52	ADR7/	
53	ADR4/	
54	ADR5/	
55	ADR2/	
56	ADR3/	
57	ADR0/	
58	ADR1/	
59		
60		

TABLE 1-1 (CONTINUED)

Connector P1 Pin Assignments

Pin*	Signal	Function
61		
62		
63		
64		
65		
66		
67	DA16/	Data bus
68	DA17/	
69	DA14/	
70	DA15/	
71	DA12/	
72	DA13/	
73	DA10/	
74	DA11/	
75	GND	Ground
76	GND	
77		
78		
79	-12 VDC	Power input
80	-12 VDC	
81	+5 VDC	Power input
82	+5 VDC	
83	+5 VDC	
84	+5 VDC	
85	GND	Ground
86	GND	

* All unassigned pins are reserved (do not use).

+ Connect BPRN/ to ground in single master systems.

1.4 Specifications

Table (1-3) contains device and board specifications of the ZX-80/05. Also see component Data Catalogs and Vendor Specification Manuals for more information regarding the ZX-80/05 SBC and its components.

TABLE 1-3

Word Size

Instruction - 8, 16, 24 Bits
Data - 8 Bits
Address - 16-Bits

Cycle

Basic 4 Clock Instruction - 814 nSEC

Memory Addressing

ROM/EPROM - 0-0FFFH 2716 Restricted
0-1FFFH 2716 Full (4 Scokets)
0-3FFFH 2732
0-7FFFH 2764

RAM 3E00-3FFFH Restricted Mode
3C00-3FFFH Full Mode
7C00-7FFFH 2732 System
BC00-BFFFH 2764 System

ROM/EPROM/RAM type selection and addressing selected by dip switch programming and bipolar mapping PROM.

IO Capacity

Parallel - 22 Programmable Lines
Serial - 1 TxD, 1 RxD RS232 for CPU SID/SOD
SBX - 3 Jacks for Multimodules (J3, J4, J5) to Intel standard I/O expansion bus specification

Timer

Input Rate - 122.88 KHZ (8.14 uS Period)
Output Rates - Pulse 8.14 uS/66.67 ms
Sq. Rate Gen.7.50 Hz/61.44 KHz
Strobe 8.14 uS/133.33 mS

TABLE 1-3 (CONTINUED)

System Clock
CPU - 1.966 MHZ or
4.9152 MHZ Internal (Selectable)
Utility - 19.6608 MHZ (BCLK)
1.96608 MHZ (Timer)

Interfaces
Bus - 86 Line Multibus Spec (TTL)
J3, J4, J5 - SBX Spec (TTL)
Serial IO - TTL, Sockets for RS 232C Line Drivers and Receivers
Parallel IO - All Signals TTL

Physical
Width - 12.00" (30.49 cm)
Height - 6.75" (17.15 cm)
Depth - 0.50" (1.27 cm) Max
Weight - 13 Ounces (368.1 gm)

Electrical
DC Power Requirement (Typical)
+5 - 1.0A without EPROMS
+12 - 20mA (RS232 only user)
-12 - 20mA (RS232 only user)

Operating Temperature
$0^{\circ}C$ to $+55^{\circ}C$ to 95% R.H. Given Free Air Flow Across Board Product

Ordering Information

Part No. ZX-80/05

Description Single Board Computer (Comes without EPROM and RS 232 Interface Chips) Manual Supplied.

Various complete development systems and disk subsystems plus additional copies of manuals are available as are current expansion modules:

ZBX-249 Centronics Printer I/F

ZBX-350 Parallel I/O (8255A)

ZBX-351 Serial RS-232 I/F (8251A)

ZBX-218 Floppy Disk Controller (NEC uPD 765)

ZBX-324 Dual Analog ADC and DAC 8-Bit

ZBX-488TI IEEE 488 STD GPIB Interface

and low-cost design aids and baseboards:

ZX-906 MULTIBUS display

ZX-907 MULTIBUS tracer analyzer

ZX-905 Prototyping card

ZX-957 Bus extender when chassis is full

ZX-028B 128KB dynamic RAM card

ZX-85/88 Single board development system, IPB.

CHAPTER 2

PREPARATION FOR USE

2.1 UNPACKING AND INSPECTION

2.1.1 Care In Handling

Mishandling during shipment can damage the ZX 80/05 board. Contact the carrier or his agent if there are any signs of breakage or water damage on the shipping carton. Do this before the carton is opened. In any case, save the packing carton and material. Contact Zendex at 415/829-1284 if there is visible damage, or TWX 910-389-4009.

2.2.2 Warranty.

Fill out and return the enclosed warranty card. This will enable us to provide you with engineering changes and updates should they later develop.

2.1.3 Firmware/Software

Prepare your ZX 80/05 for testing and use by providing your firmware or software and any devices necessary to complete the system. See tables for help in configuring your system.

2.1.4 DC POWER

The ZX-80/05 requires a minimum of 1 amp at +5 volts to run. If RS 232 interfacing is required + 12 volts will be needed (20 ma.). If EPROMS are installed, +5 volts must be able to provide approximately 2 amps.

2.1.5 Cooling

It is recommended that some form of cooling be provided in order to keep the temperature below 50 Centigrade in the immediate vicinity of the ZX-80/05. Air flow at a rate of 20 CFM should be sufficient.

2.1.6 Physical Dimensions

Width	- 12.00 in.	(30.49 cm.)
Height	- 6.75 in.	(17.15 cm.)
Depth	- 0.50 in.	(1.27 cm.)
Weight	- 13 .oz.	(368.1 gm.)

Note: added depth clearance of 0.50 in. is required where Intel SBX or Zendex ZBX expansion modules are mounted on the baseboard, ZX-80/05.

2.1.7 I/O Interfacing

Serial I/O can be either TTL or RS232. Connect serial device to either J2 or J1 depending on the user's requirements. If RS 232 is utilized, install 1488 and 1489 driver/ receivers at (U13 and U14) and use J2. Molex or Amp crimp type connectors are recommended. (See table 2-1)

Parallel I/O should be connected to J1 after appropriate line drivers/terminators are installed at (U7, U8, U9, U10, U11 and U12). A flat cable and connector equivalent to the 3M Part No. 3415-0001 is recommended.

2.1.7.1 Connector Recommendation Details

TABLE 2-1

Function	No. Of Pairs/ Pins	Centers (Inches)	Connector Type	Vendor	Vender Part No.
Parallel I/O Connector (J1)	25/50	0.1	Flat Crimp	3M 3M AMP ANSLEY SAE	3415-0000 WITH EAR 3415-0001 W/O EARS 88083-1 609-5015 SD6750 SERIES
Parallel I/O Connector (J1)	25/50	0.1	Soldered	AMP VIKING T1	2-583485-6 2VH25/1JV5 H312125
Parallel I/O Connector (J1)	25/50	0.1	Wirewrap	T1 VIKING ITT CANNON	H311125 3VH25/1JND5 EC4A050A1A
Serial I/O Connector (J2)			Flat Crimp	3M AMP ANSLEY SAE	3462-0001 88106-1 609-2615 SD6726 SERIES
Serial I/O Connector (J2)			Soldered	T1 AMP	H312113 1-583485-5
Serial I/O Connector (J2)			Wirewrap	T1	H311113

TABLE 2-1 (CONTINUED)

Function	No. Of Pairs/ Pins	Centers (Inches)	Connector Type	Vendor	Vendor Part No.
Multibus Connector (P1)	43/86	0.156	Soldered	EBY VIKING ELFAB EDAC	CD43AE013 2KH43/9AMK12 BS156D43PBA 337086540201
Multibus Connector (P1)	43/86	0.156	Wirewrap	EBY ELFAB EDAC	CD43BA013 BW1562A43PBB 337086540202
Auxiliary Connector (P2)	30/60	0.1	Soldered	ELFAB EDAC	97169001 345060524300
Auxiliary Connector (P2)	30/60	0.1	Wirewrap	ELFAB EDAC	97167901 345060523301

NOTES

1. Connector heights are not guaranteed to conform to OEM packaging equipment.
2. Wirewrap pin lengths are not guaranteed to conform to OEM packing equipment.
3. Connector numbering convention may not agree with board connector numbers.

2.1.8 Jumpers

Install appropriate jumpers on the ZX-80/05 per user's requirements. (See Table 2-2 for details)

2.1.8.1 JUMPER CONFIGURATION

The ZX-80/05 jumper and switch selectable options are listed in table 2-2. The user should use this table to set-up for specific requirements. An asterisk (*) depicts factory setting.

TABLE 2-2

<table>
<tr><th>JUMPER</th><th>DESCRIPTION</th></tr>
<tr><td>W1</td><td>W1 is used to provide for a programmable mode for MULTIBUS override. Depending on the selected mode the ZX-80/05 can gain control of the MULTIBUS as follows:

MODE 1: Requests MULTIBUS as needed.
MODE 2: Programmable over-ride of MULTIBUS with IO output to port on 8155-2
MODE 3: Always over-ride MULTIBUS. ZX-80/05 will keep control once acquired.

<table><tr><th>MODE 1</th><th>MODE 2</th><th>MODE 3</th></tr><tr><td>W1 A-D*
W1 B-D*</td><td>W1 A-B
ONLY</td><td>W1 B-C
ONLY</td></tr></table></td></tr>
<tr><td>W2</td><td>*B-C: PC3 pin of 8155-2 connected to 14-pin socket XU10 for IO on J1.

A-C: Connects INTR Port 2 to interrupt another master on MULTIBUS via W9.</td></tr>
</table>

<table>
<tr><th>JUMPER</th><th>DESCRIPTION</th></tr>
<tr><td>W3
W4</td><td>Not Used on ZX-80/05. Was used on SBC-80/05 to select EPROM type. Refer to
W32, 33, 34, 35
W37, 39, 41, 43
W38, 40, 42, 44
W45, 46, 47, 48
S1
W20, 21</td></tr>
<tr><td>W5</td><td>Jumper pad W5 provides for connection of the many various interrupt sources to one or more of the four available request pins on the 8085A-2 CPU itself. The four request pins have the following characteristics, in order of descending priority.
<table>
<tr><th>W5 Pin</th><th>NAME</th><th>PRIORITY</th><th>TRIGGER SENSITIVITY</th></tr>
<tr><td>A</td><td>TRAP</td><td>Highest</td><td>Edge + Level</td></tr>
<tr><td>E</td><td>RST 7.5</td><td></td><td>Rising Edge</td></tr>
<tr><td>C</td><td>RST 6.5</td><td></td><td>High Level</td></tr>
<tr><td>B</td><td>RST 5.5</td><td>Lowest</td><td>High Level</td></tr>
</table>
W5 E-M* Timer interrupt to RST 7.5
W5 A-F* Trap grounded</td></tr>
<tr><td>W6</td><td>Not Used</td></tr>
<tr><td>W7</td><td>W7* Will connect 9.8 MHz source to MULTIBUS BCLK/ line.</td></tr>
<tr><td>W8</td><td>W8* Will connect 9.8 MHz source to MULTIBUS CCLK/ line.
Disconnect W7 or W8 if another master is to provide Bus Clocks</td></tr>
</table>

JUMPER	DESCRIPTION
W9	W9 will interface the eight Multibus interrupt sources (INTØ-INT7/) to inverters and W5 to eventually connect to interrupt request pins on U32 (8085A-2 CPU)
W10	*A-B Outputs BPRO/ signal to MULTIBUS. Used only in serial priority resolution schemes. Remove for parallel resolution configuration of MULTIBUS masters.
W11	Not Used
W12	*A-B PC4 connects to XU10 for IO through J1 A-C PC4 is used as RS232 reader control signal at J2-5
W13-W19	Not Used
W20, W21	W20 B-C* and W21 B-C* restrict access to the 1Kx8 RAM at U38 to 512 BYTES as in SBC-80/05. Moving W20 to A-B allows 1K access and W21 A-B allows 2K access when U38 is changed to 4802. Refer to table on sheet 2 of schematic.
W22	*A-B Selects the clock input frequency to the CPU to be that of the SBC-80/05 (3.9MHz) Moving W22 to B-C selects near maximum clock rate (9.8 MHz) and fastest possible execution speeds for 8085A-2. Selecting this option requires use of 250 nSec access (or faster) memory devices at U39, U40, U41, and U42.

JUMPER	DESCRIPTION
W23 W26 W29	Posts A and B provide wire-wrap points for optional output lines of SBX-Modules at J3, J4, and J5.
W24 W25 W27 W28 W30 W31	These points allow connection of module interrupts to "or" gates in A-B position or ground inputs of "or" gates in B-C positions. Outputs of gates are at W5 pins X, Y, and Z.
W32 W33 W34 W35	These pads select on-board access of writable locations for addresses covered by memory devices at U39 through U42. The *B-C position causes writes to be steered off-board while reads stay on-board. Position A-B forces all read/writes to on-board. Mapping of memory is in accordance with map found in table on sheet two of the schematic.
W36	*B-C Selects pin 19 of socket U38 to be VCC. This mode is intended for 4118 type RAMS installed at U38. When a 4802 is used at U38 use W36 A-B.
W37 W39 W41 W43	*A-B Selects address line ABA for pin 21 of U39, U40, U41, U42 respectively. Position B-C is used only when a 4118 RAM is used in U39-U42.
W38 W40 W42 W44	*B-C Sends VCC to pin 23 of U39-U42. Depending on device type these jumpers select VCC, ABB, or WR/ for pin 23. See table on sheet 2 of the schematic.

JUMPER	DESCRIPTION
W45 W46 W47 W48	*A-B Position puts the RD/ signal on pin 22 of U39-U42. This signal is used for devices using output enable (OE/). See table on schematic sheet two.

2.1.9 Memory

Install EPROM, RAM according to user's specific requirements. Use sockets at (U38, U39, U40, U41, U42). Note; take care to install 24 pin devices correctly in 28 pin sockets. Refer to Data Book of device manufacturer for correct pin outs. (See Figure 1-1 for memory map detail)

2.1.10 Interrupts

Install interrupt request jumpers according to your requirements. Remember that TRAP (unmasked) is the highest priority interrupt to the 8085A-2. RST 5.5 is the lowest priority interrupt. The TRAP is level and edge sensitive. RST 7.5 is rising edge sensitive. RST 6.5 and RST 5.5 are level sensitive. (See table 2-3)

TABLE 2-3

INTERRUPT LEVELS

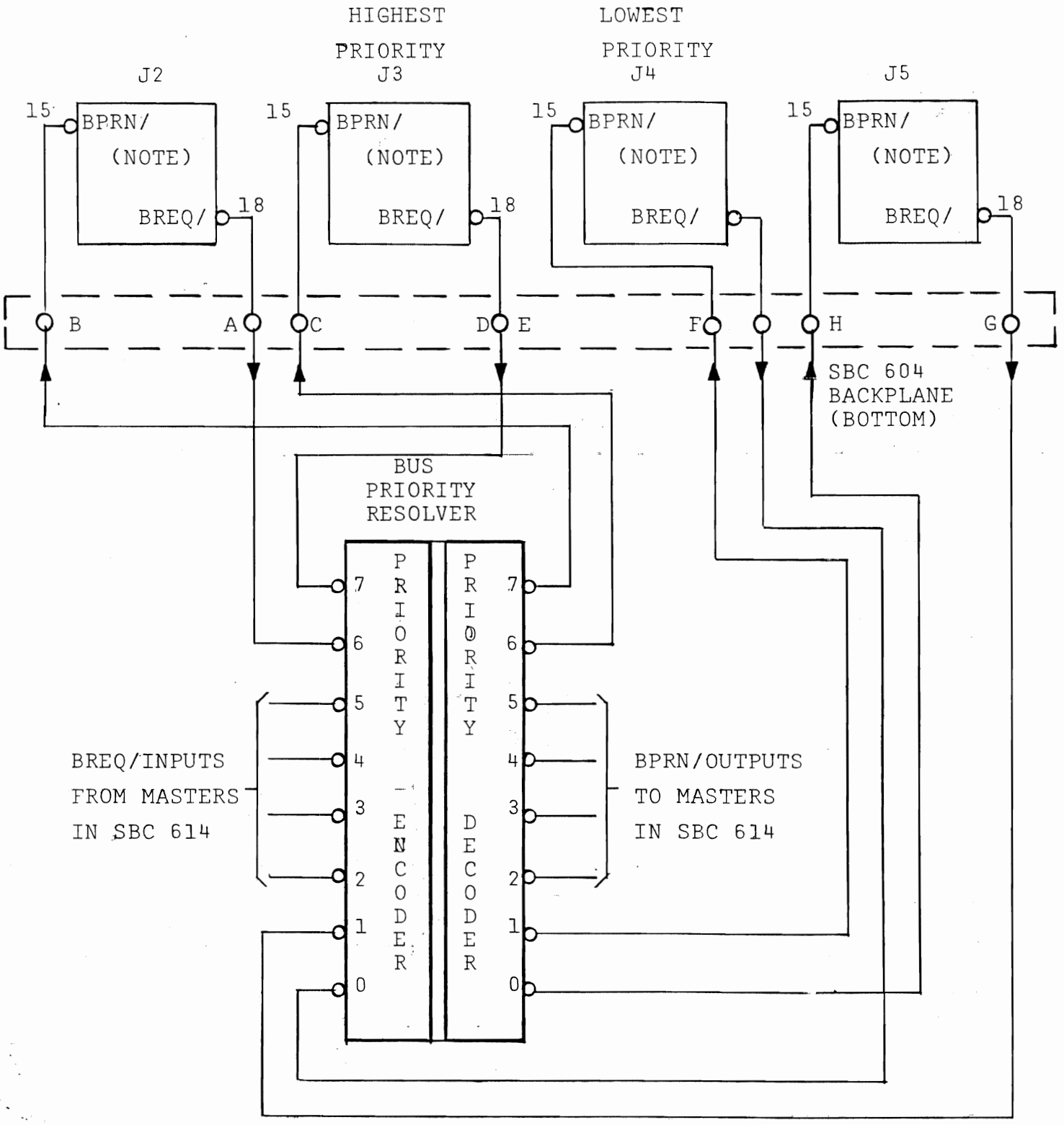
(in ascending order of priority)

Level	Address	Jumpers	Trigger
(lowest)			
RST 5.5	2C H	W5 Pin B	Level (HI)
RST 6.5	34 H	W5 Pin C	Level (HI)
RST 7.5	3C H	W5 Pin E	Rising Edge
TRAP	24 H	W5 Pin A	Edge and Level (HI)
(highest)			

2.1.11 MULTIBUS Considerations

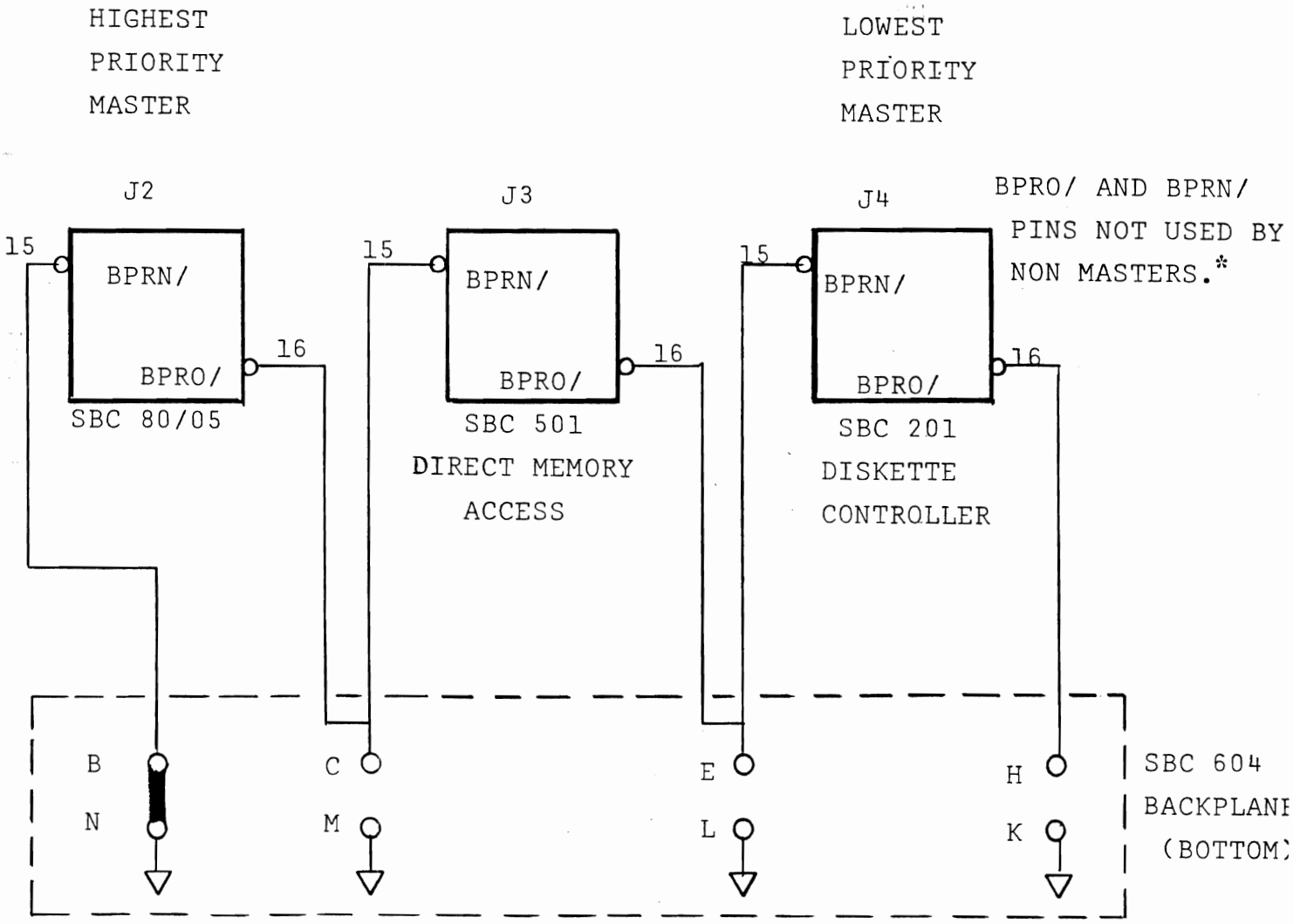
If the ZX-80/05 is used in a MULTIBUS configuration with multiple baseboards, be sure the bus priority jumpering on the MULTIBUS backplane is correct for the user's system master/slave relationships. Refer to the MULTIBUS specifications for more information regarding this requirement. (Also See Figure 2-1 for working examples)

FIGURE 2-1
First Example of
Parallel Priority Resolution Scheme



NOTE: REFER TO IMPORTANT INFORMATION IN MULTIBUS SPECIFICATION.

FIGURE 2-1 (CONTINUED)
Second Example of A
Parallel Priority Resolution Scheme



* Baseboard modules that are not MULTIBUS masters.

TABLE 2-4

DESCRIPTION OF A 4-SLOT MULTIBUS CHASSIS AND BACKPLANE

ITEM	DESCRIPTION
SBC-604	4-Slot Modular Chassis and Backplane for Multibus Boards. Includes Bus termination Expand with SBC-614
J1 Connector	Use Ansley 609-5015 (ribbon) AMP 2-583485-6 (solder) or Viking 3VH25/1JND5 (wire-wrap)
J2 Connector	Use Molex 09-50-7071 W/08-50-0106 or AMP 3-87025-4 W/87023-1
RAM	U38 (MK4118-4) May be replaced by an 4802 to increase RAM to 2Kx8. W36 should be changed to A-B and W21 to A-B.
EPROM	Four sockets are provided at U39, U40, U41, and U42. The sockets are 28 pin and will receive 24 pin types 2716 and 2732. The smaller EPROMS do not use pins 1, 2, 27, and 28 of each socket. Type 2764 EPROMS are 28 pin and use the entire socket.
J1 Line Drivers	14 pin sockets at XU7, XU8, XU11, XU12, XU9, and XU10 may have 74 series logic installed as output drivers for U19 (8155-2) Typical are 7400, 7437, 7438. Consult data sheets for desirable driver characteristics.

NOTE: Zendex unique 9-slot MULTIBUS chassis and backplane ZX-609 is also available for use with the ZX-80/05 SBC CPU. ZX-609 features, optionally both parallel and serial priority resolution schemes with sockets for mounting TTL priority encoder and decoder circuits on the backplane itself. These are simply removed for a serial scheme or when the parallel priority resolution scheme is implemented on one of the MULTIBUS master baseboard cards.

CHAPTER 3

PROGRAMMING INFORMATION

3.1 Introduction

The following paragraphs are intended to aid the user in programming the various I/O and timer devices located on the ZX-80/05 CPU module. Some sections address topics discussed in Chapters I or II and are included to clarify the system by taking an applications point of view. Further some familiarity with the 8085A instruction set listed in the Appendix, is assumed in the ensuing discussion.

3.2 CPU/Memory

Upon reset, the CPU's Program Counter (PC) and Instruction Reg (IR) are set to zero. Then, it is assumed that the user's program either starts here or that a jump to the start is contained at locations 0000 thru 0002. The address and data fetching are then, of course, under program control. Since the ZX-80/05 memory can be configured in a variety of ways the user must be careful not to address non-existent memory or try to write into PROM/EPROM locations. A write to PROM will cause a loss of data while a reference to non-existent memory will cause the CPU to remain in the wait state since memory acknowledge is not received. On-board memory requests allow the CPU to operate at full speed. Off-board references, however, must make use of the bus arbitration logic with an inherent reduction in CPU operating speed. See Section 2.1.9 and Figure 1-1 for a list of memory location options.

3.3 Serial I/O with simplified examples

Serial I/O is performed utilizing the SIM and RIM instructions of the 8085A-2 instruction set. The following are simplified examples of how output to the SOD line and input to the SID line of the 8085A can be accomplished.

```
;
;  Routine Name:          Output
;  Input arguments:       Output Byte in Reg C.
;  Return arguments:      None
;  Function:              Use SOD line to output character in
                          Reg C to serial device.


OUTPUT:
        MVI     E,7             ; Bit count for Character
        MOV     A,C             ; Data in AC
        CMA                     ; Data will be inverted
        MOV     C,A             ; At the SOD line
        MVI     A,1100 0000B    ; Bit 7 = start bit
        SIM                     ; Bit 6 = command
MORE:
        Wait Time               ; MACRO to Delay
                                ; For Proper Baud Rate
                                ; Based on Selected Clock
                                ; Rate of ZX-80/05
        MOV     A,C             ; Get Data
        RRC                     ; Put LSB in Bit 7
        MOV     C,A             ; Save data again
        ORI     0100 0000B      ; Force command (Bit 6 = 1)
        ANI     1100 0000B      ; get shed of superfluous bits
        SIM                     ; output bit 7
        DCR     E               ; count - 1
        JNZ     MORE            : JMP if more to output
        MVI     0100 0000B      ; Stop bit and command
        SIM                     ; Output stop bit (1)
        Wait Time               ; Wait for Baud Rate
        RET                     ; Bye!

;
;  Routine Name:          Input
;  Input Arguments:       None
;  Return Arguments:      Return with input Byte in Reg C
;  Function:              Use SID line to input a
                          character from the serial device into
                          Reg C.  Wait at SID for start bit.
```

```
INPUT:

        MVI     E,7                     ; Bit count
        MVI     C,0                     ; Clear return character

WAIT:

        RIM                             ; Read a bit?
        ANI     10000 0000B             ; Is it start Bit
        JZ      Wait                    ; No. JMP
        Wait    Time                    ; Delay for Baud rate
        RIM                             ; Again
        ANI     1000 0000B              ; debounce input
        JZ      Wait                    ; false alarm, JMP

READIT:

        DCR     E                       ; count - 1
        RZ                              ; Bye
        Wait    Time                    ; Delay for baud rate
        RIM                             ; Get a bit
        ANI     1000 0000B              ; see if 1 or 0
        ORA     C                       ; or in the preceding bits
        RRC                             ; Shift to position
        MOV     C,A                     ; save the result
        JMP     READIT                  ; next bit
```

The user may wish to implement buffer or string, output and input, and therefore would want to enhance the above fundamental approaches. Also optional SBX-type Zendex serial I/O module ZBX-351 may be installed. It utilizes a USART 8251A for serial I/O.

3.4 I/O Register Addresses

The 8085A-2 addresses I/O via the IN and OUT instructions of the 8085A instruction set. Byte 2 of these instructions contains an 8-bit address used during decode. Jumpers, dip switches or mapping PROMS on various boards determine exactly which devices will respond to the given address. The following sections on parallel and timer programming illustrate I/O programming of the ZX-80/05.

3.5 Parallel I/O

The I/O mapping PROMSat (U22) in conjunction with the decoder at (U21) specifies that the I/O address (00 - 07) select the 8155-2 at (U19.)

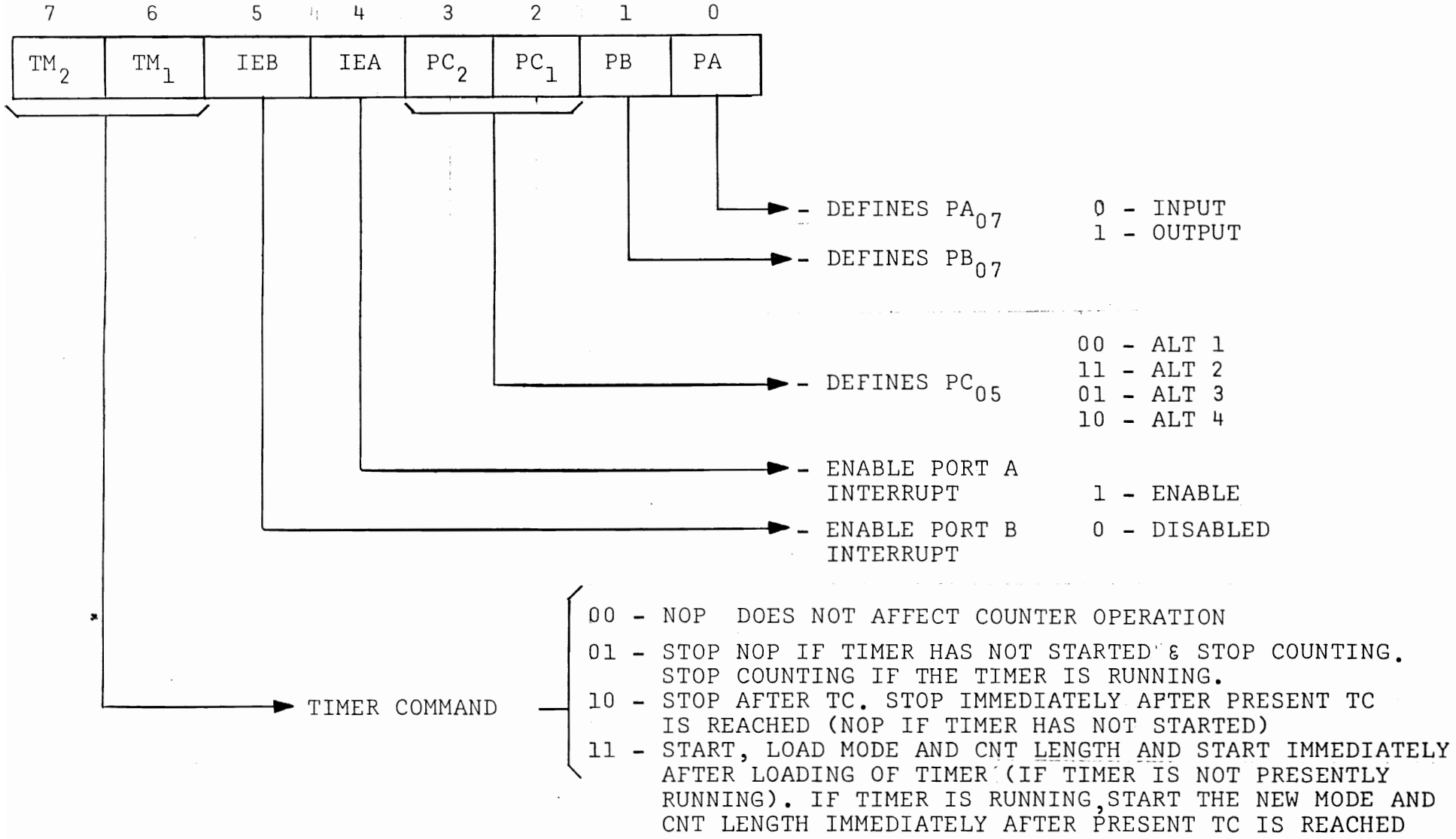
Register	Length In Bits	I/O ADDR
Command/STATUS	8	00
Port 01	8	01
Port 02	8	02
Port 03	6	03

The commands to the 8155 are sent to the command register by an OUT instruction specifying address 00. Four bits control port configurations (0 - 3), two bits control interrupts (4 - 5) and two bits specify timer commands. (See Figure 3 - 1).

The status register can be read by executing an IN instruction specifying address 00. Three status bits report port 01 status, three bits report port 02 status, and one bit is a timer interrupt status bit. Bit 7 of the status word is unused. (See Figure 3 - 2).

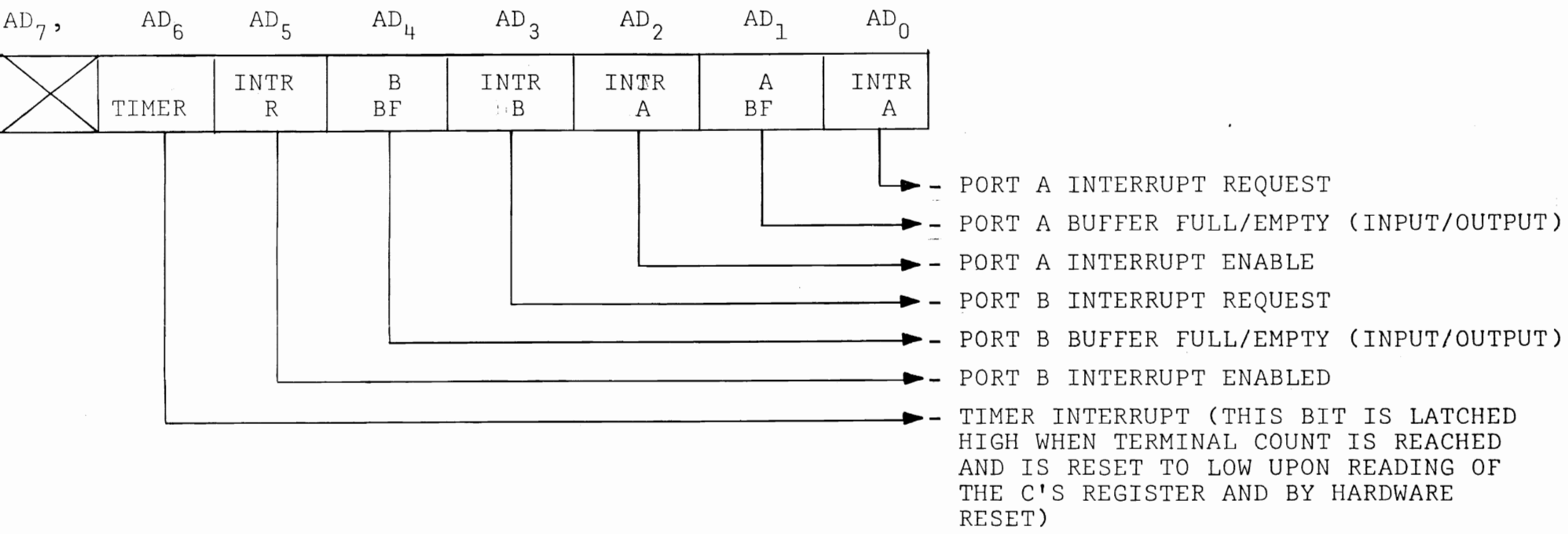
Command Register I Assignment

FIGURE 3 - 1



STATUS REGISTER BIT ASSIGNMENT

FIGURE 3 - 2



Depending on the command issued to the command register, Port 01 can be either input or output. The same is true for Port 02. Also, the mode of operation of both these ports may be strobed or direct I/O depending on command output to Port 03. For example, if Alt mode 4 is selected (See Figure 3-3, Timer Format) Ports 01 and 02 may be strobed by bit 2 and bit 5 respectively of Port 03. A typical application might use a keyboard strobe on port 03 bit 2 to strobe data into Port 01. Likewise, in Alt mode 4, an interrupt request from Port 01 can utilize Port 03 bit 0 tied to an RST input on the 8085A. This, in fact, is the case with respect to the Zendex ZX-80/05 board.

In summary, the three I/O ports can be configured in several different ways with Port 03 serving a valuable function as control lines for Port 01 and Port 02, if the user so desires. See Table 3-1, Port 03 Programmable Modes.

3.6 Timer Operation

An integral part of the 8155-2 is a timer (down counter) section useful in a variety of time-critical applications. This 14 bit counter uses I/O address 04 and 05 of the 8155-2. Pulses at (pin 3) of the 8155-2 are counted and pulse or square wave outputs are generated depending on the particular mode specified. The output at (pin 6) is low when 1/2 the terminal count is reached in modes 0 and 1. The output is active low when terminal count is reached in modes 2 and 3. See Figure 3-3 Timer Format.

The following four modes are supported.

Mode 0 - A single square wave is output at Pin 6 which is high during the first half of the count and low during the second half. If the count is odd, the wave is high for the extra "tick".

Mode 1 - A continuous square wave is output at Pin 6 which is high during the first half of the count and low during the second half. At terminal count, the counter is automatically relocated.

Mode 2 - A single low true pulse is output at terminal count.

Mode 3 - A continuous low true pulse is output at terminal count. At TC, the counter is automatically reloaded.

Two bits (6-7) of the 8155-2 command register are used for starting and stopping the timer as follows:

CMD 00 - No operation

CMD 01 - STOP timer. No operation if already stopped.

CMD 10 - STOP timer after terminal count is reached. No operation if already stopped.

CMD 11 - START timer. Load mode and counter length and start immediately if stopped. Load mode and counter length and start when terminal count is reached if started.

Note: The clock input to the timer is 133.88 KHz generated at (U2) of the ZX-80/05 board.

The user should be aware that the count in the counter can be read by an IN instruction to addresses 04 and 05. However, the value returned does not directly correspond to the number of pulses detected since a decrement by 2 is performed by the device. The user must compute the actual counts remaining. Also, a new start command must be issued in order to change either the count or the mode or both.

3.7 Interrupt Processing

The on-board 8085A-2 CPU device includes four vectored interrupt inputs. These are TRAP, RST 7.5, RST 6.5 and RST 5.5. Jumper posts are provided on the ZX-80/05 which enable the user to steer various signals from the multibus interrupt lines, timer, parallel ports and external interrupt to these 4 interrups on the 8085A-2. The RST 5.5 RST 6.5 and RST 7.5 are maskable with the 8085A-2 SIM instruction. The TRAP is not maskable. The user

TABLE 3 - 1

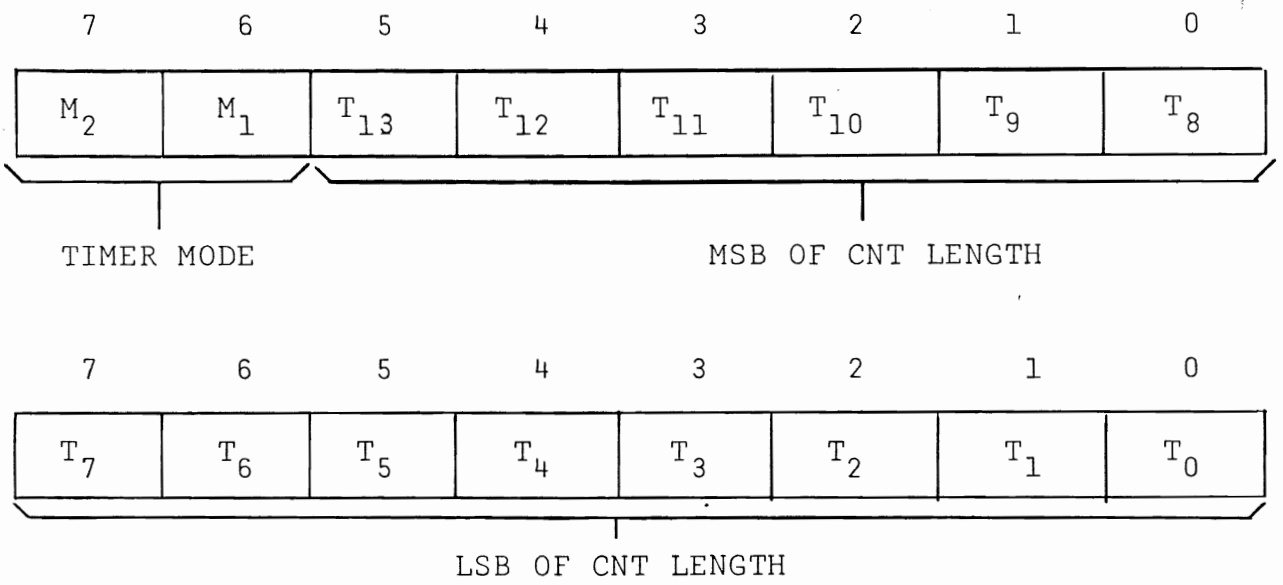
Port 03 Programmable Modes

PORT 03 BIT	A1 1 1	A1 1 2	A1 1 3	A1 1 4
0	Input Port	Output Port	Port 01 Interrupt	Port 01 Interrupt
1	Input Port	Output Port	Port 01 Buffer Full	Port 01 Buffer Full
2	Input Port	Output Port	Port 01 Strobe	Port 01 Strobe
3	Input Port	Output Port	Note 1	Port 02 Interrupt
4	Input Port	Output Port	Note 2	Port 02 Buffer Full
5	Input Port	Output Port	Note 3	Port 02 Strobe

Notes:

1. If W2 is in position B-C, bit 3 is output bit.
2. If W12 is in position A-B, bit 4 is output bit; if W12 is in position A-C bit 4 is RS232C Reader Control (RDR C 11) signal.
3. If W1 is in position A-B (only) and W6 is in position A-B, bit 5 is used to provide the programmable bus override mode; i.e., the SBC 80/05 will not relinquish the Multibus until Port 03 bit 5 is cleared. If the override function is not jumpered, bit 5 is not functional.

FIGURE 3 - 3



Timer Format

There are four modes to choose from M2 and M1 define the timer mode as shown in Figure 9.

FIGURE 3 - 3 (CONTINUED)

TIMER OUT WAVEFORMS

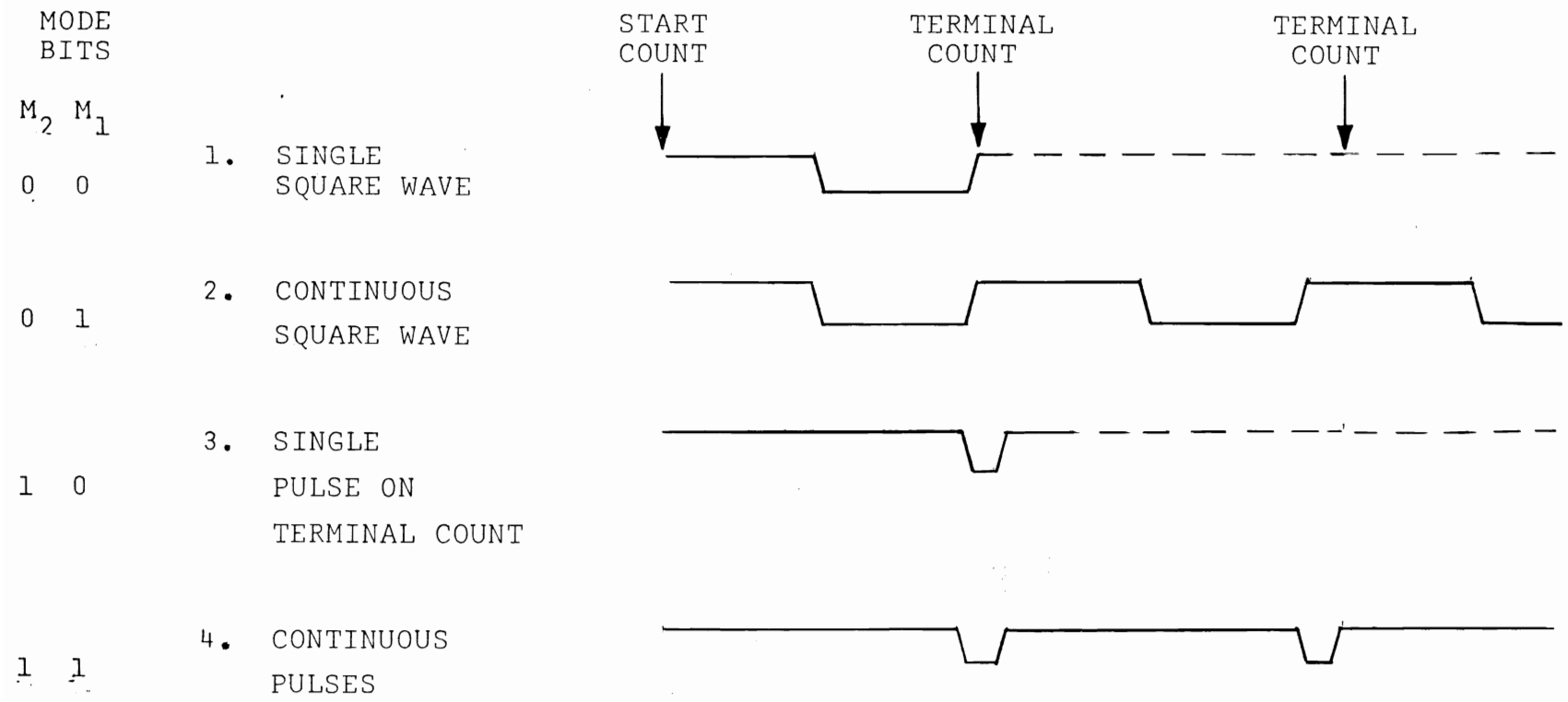


FIGURE 3 - 3 (CONTINUED)

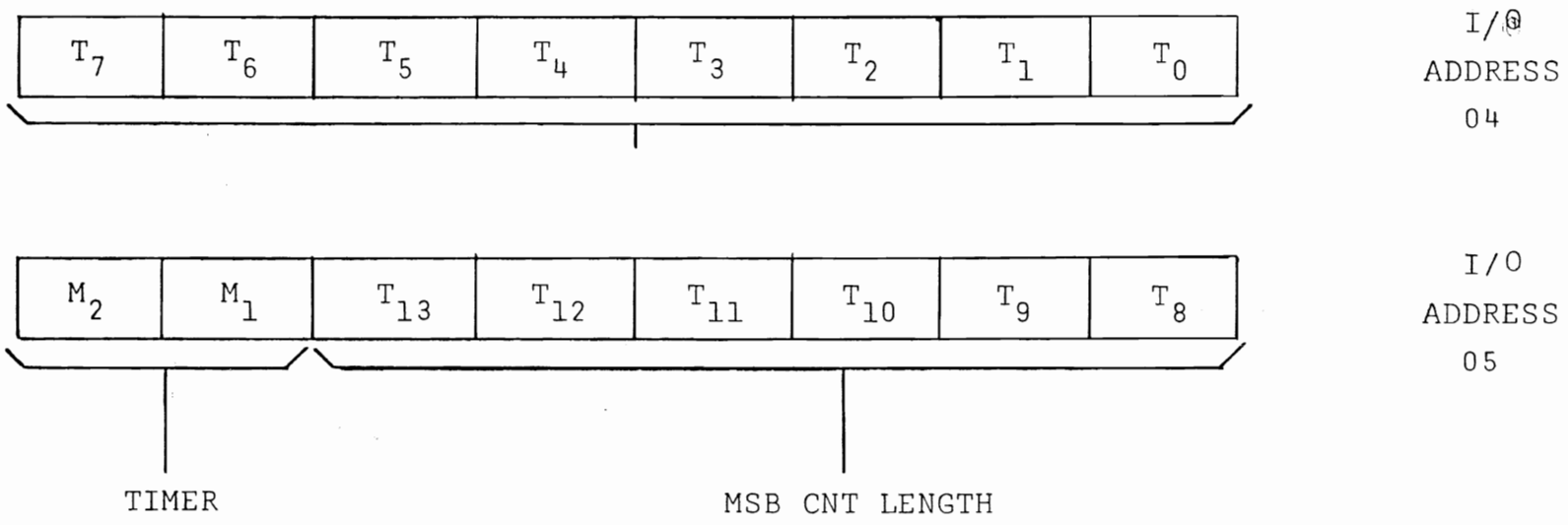
TIMER MODES

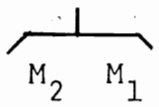
Bits 6-7 (TM_2 and TM_1) of command register contents are used to start and stop the counter. There are four commands to choose from.

TM_2	TM_1	
0	0	NOP - Do not affect counter operation
0	1	STOP - NOP if timer has not started, stop counting if the timer is running..
1	0	STOP AFTER TC - Stop immediately after present TC is reached (NOP if timer has not started).
1	1	START - Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

FIGURE 3 - 4

Timer Format





0	0	OUTPUT LOW DURING SECOND HALF OF COUNT. (SEE NOTE).
0	1	SQUARE WAVE OUTPUT; i.e., THE PERIOD OF THE SQUARE WAVE EQUALS THE COUNT LENGTH PROGRAMMED WITH AUTOMATIC RELOAD AT TERMINAL COUNT.
1	0	SINGLE PULSE OUTPUT UPON TC BEING REACHED.
1	1	AUTOMATIC RELOAD; i.e., SINGLE PULSE OUTPUT EVERY TIME TC IS REACHED.

NOTE: In case of an asymmetric count (e.g., 15), output will be high during larger half of count.

Must provide an interrupt processing routine at the target interrupt address where machine state information is saved and the interrupt handled. The return to mainline program processing can then be implemented by a simple RET instruction since the PC has been saved.

The RST type interrupts function in the following manner: The RST 7.5 line is asserted on the 8085A-2. The 8085A-2 then executes a forced RST 7.5 instruction, which causes a vector to location 60 (3C H). A valid instruction at 3C H (typically a JMP or CALL)will then be executed as part of the interrupt handling routine. Registers should be saved prior to any processing. The last instruction executed by the handler routine would be a RET instruction whereby the normal program would be resumed. Prior to returning, the user should restore registers and enable interrupts (EI). The system would then be ready to process subsequent interrupts. The following addresses apply to the RST group of interrupts.

RST 7.5 vectors thru 3C H
RST 6.5 vectors thru 34 H
RST 5.5 vectors thru 2C H

The user is directed to the discussion of RST instructions in the 8085A instruction manual. (See Table 2-3 Interrupt Levels)

3.8 Traps

The Trap is a special case of the RST type interrupt. It can be viewed as functioning as if it were a pseudo RST 4.5 line in that it vectors thru location 24 H. However, it is the highest priority interrupt and it is not maskable. Because it is not maskable, it should not be used in any application where a specific segment of code must "lockout" interrupts from occuring and possibly altering critical machine state information. The trap functions well as a power-fail mechanism or catastrophic error processor.

CHAPTER 4

CIRCUIT ANALYSIS - HARDWARE ORGANIZATION

4.1 General

The following discussion references Figures 4-1 and 4-2 schematic diagrams. Grid coordinates A-D (Y) and 1-8 (X) are used to locate items under discussion. Low true signals are indicated with a trailing (/) in the signal name. High true signals contain no (/) in the mnemonic name. High levels are $\geq$ 2.0 volts. Low levels are $\leq$ 0.5 volts. If the sheet number is not stated, assume sheet 1 of the schematics.

4.2 Power Up Initialization

Since various bi-stable devices are unpredictable at initial power application, a reset signal must be generated and used to "clear" the CPU at (C5) sheet 1, the Bus controller at (C2) sheet 1 and the I/O Ports at (C3) sheet 2. The integrated signal at capacitor C14 at (C7) is applied to pin 2 of the 8224 at (C7) where the reset signal output at pin 1 is applied thru inverters at (C6) to the 8085A, pin 36 as RST IN. This signal is also presented at pin 1 of the 8219 at (B2) sheet 1. The RESET signal at (D6) sheet 1 is also placed on pin 4 of the 8155 at (B4) of sheet 2. These signals, in conjunction, clear the PC, IR and INT EN flip-flops,as well as,preset the bus controller and initialize the 8155 to input mode.

4.3 Clocks

A 19.6608 MHz crystal at (D7) sheet 1 provides the time base for the ZX-80/05 board. The crystal output at pin 12 of the 8224 is divided by 2 by the 74LS74 at (B4) sheet 1. The outputs are inverted by the 7437 at (B4) and presented to the MULTIBUS as BCLK/ and CCLK/. BCLK/ and CCLK/ lines are jumperable.

Also, the crystal oscillator output at pin 12 of the 8224 is jumper selectable for placement directly on pin 11 of the 74LS74 at (C6) sheet 1 or placed thru a divide by 2.5 using the 74161 at (A4) then to pin 11 of the 74LS74 at (C6). By placing jumper W22, the user may select a CPU speed at 4.9 MH_Z or 1.96 MHZ since the 8085A-2 again divides by 2 at its X1 input.

The divide by 5 at the 74161 at (A4) sheet 1 is applied as 3.93 MZ to pin 3 of the 74LS74 at (B6) sheet 1 where it is divided by 2 and then further divided by 16 by the 74161 at (B5) sheet 1. The 122.88 KHZ output is then used as the timer in signal for the 8155-2 at (C3) sheet 2.

4.4 CPU

Communications between CPU and Memory or I/O are conducted as a sequence of read or write operations. The program executes instructions as sequences of machine cycles. A machine cycle is a simple read or write between CPU and an external device. An instruction on the 8085-A can consist of up to 5 machine cycles and as few a 1 machine cycle. All instructions must cycle thru a fetch operation where the target instruction is read from memory. A given instruction may contain up to 3 fetch operations. Within a machine cycle there will be between 3 and 6 "states." A state is defined as the time interval of 1 CPU clock cycle. Depending on the jumper configuration of the ZX-80/05 board, this time frame is either 508 nanoseconds or 203 nanoseconds. The total number of time states per instruction is variable since the different instructions require different numbers of time states and machine cycles to perform their operation. (See Figure 4-3 Timing)

Wait states may be imposed on the CPU (READY/) when off-board memory or I/O access is required.

The READY/ signal effectively idles (freezes) the CPU. The following narrative describes the operation of a memory read request by the CPU during a fetch cycle.

1. CPU generates IO/$\overline{M}$ low signalling a memory reference.
2. PC address placed on A8-A15 and AD0 - AD7. AD0 - AD7 are also data lines, so these bits remain true for only one time state. Later, they will hold the contents of memory accessed during the cycle.
3. Assert ALE for I/O device enable if applicable.
4. RD/, presented at start of T2, enables memory device.
5. Contents of memory placed on AD0 - AD7.

   (If this is an off board reference, the CPU may be placed in a wait state before data is presented to AD0 - AD7.)
6. Opcode (if applicable) is decoded during T4 and additional time states (T5, T6) are entered if required to carry on the instruction. If T5 and T6 are not required, the next machine cycle is started at T1.

4.5 Memory

Memory Read and Memory Write cycle timing is similar to the CPU fetch cycle above except that T4, T5, T6 are not required for Mem Read and Write. Also, the address lines for memory references are not always derived from the PC, and Data is not returned to the IR as in the fetch cycle but to the various CPU registers. (AC, B, C, D, E, H, L, SP, PSW) The T4, T5, T6 cycles are not required since no opcode decode is required.

However, wait states may be initiated as in opcode fetch

AD0 - AD7 are dual functioning lines. The distinction between Mem Read and Mem Write is that data is placed on AD0 - AD7 at T2 and WR/ is asserted for write operations to memory.

4.6 I/O (INPUT/OUTPUT)

I/O read and write operations are similiar to Mem. Read and Write operations with the exception of the condition of the IO/$\overline{M}$ line. Obviously, this line must be asserted high if the I/O devices are being accessed. Also, data is returned to the accumulator or loaded from the accumulator in the case of I/O. Note too, that the I/O address is loaded from the second byte of the fetched instruction.

4.7 Bus Interface

The MULTIBUS interface section of the ZX-80/05 board consists of the 8219 Bus Controller at (C2) sheet 1, two AM 2958 unidirectional bus drivers at (D2) sheet 1, and one AM 2946 bi-directional bus driver/receiver at (A2) sheet 1. A tri-state 74LS373 latch is also utilized at (D4) to latch address bits 0 - 7 onto the MULTIBUS (used on board also) since the data bus shares the same lines.

The 8219 arbitrates control of the MULTIBUS system. The BPRN/ signal enables the 8219 to contend for bus control. The actual process of bus control begins when BCR2 is asserted and RSTB/ (BCLK) time occurs. Two VCLK pulses later, BREQ is asserted and BPRO7 removed. BUSY/ signals other devices that the MULTIBUS has been seized and is currently busy.

The 8219 timing function starts with ADEN/ which enables the AM 2958 s at (C2) and (D2) for placement of I/O memory address on the MULTIBUS depending on the presence of IORC, IOWC or MRDC, MWTC. These latter signals (only one per MULTIBUS cycle) are asserted after a time delay defined by the RC network at (C1) sheet 1. When the slave device generates XACK/ on pin 23 of the MULTIBUS (C8) sheet 1, it signals the master that data has been accepted (IOWC or MWTC) or data is available on the MULTIBUS data lines (IORC or MRDC) and the basic MULTIBUS cycle is complete. XACK/ is inverted by the 74LS32 at (B6) and the 74LS00 at (C3) before being placed on pin 9 of the 8219 signalling completion of the bus cycle.

The various Read and Write control signal outputs of the 8219 are derived from the RD, WR and IO/$\overline{M}$ lines of the 8085A-2. The RDD signal output directs the 2946 Data driver/receiver at (A2) sheet 1, while ANYR of the 8219 is derived internally by the above I/O and memory read and write signals and can be used to initiate a bus transfer. Furthermore, the OVRD signal at pin 27 is used to inhibit deselect due to higher priority bus requests. This line allows consecutive bus cycles without external interference once the bus is seized.

4.8 Memory and I/O Addressing

Two 93446 mapping PROMS at (A7) and (B7) sheet 2 provide the inputs to a 74LS138 at (A6) sheet 2 and 74LS139 at (B6) sheet 2 which further decode memory and I/O addressing. Only one of these two pairs of devices is selected at a time based on the condition of the IO/$\overline{M}$ line at the 74LS04 at (A7) sheet 2. Switch S1 and jumpers W20 and W21 allow for different addressing of the on board RAM. See Table at (A4) sheet 2.

Jumper pads at (B5), (D5) and (C5) of sheet 2 provide for different addressing and EPROM types. Since 29 pin sockets are provided, the user should note that pin numbers are offset by 2 when using 24 pin devices such as 2716 and 2732 EPROMS. They are, however, accurate for 2764s. The jumpers cited above provide for these variations. See the device data book for further clarifications. See Table at (B4) sheet 2 for jumper configurations.

4.9 Parallel Port and Timer I/O

The 8155-2 at (C3) sheet 2 (see Chap. 3) is a 22 line parallel device with an on chip timer useful for various timing applications. Also on the 8155-2 is a 256 byte RAM segment which is not used, however, by the ZX-80/05 board. The WR/ and RD/ signals determine data direction of the current operation while the IO/$\overline{M}$ and $\overline{CE}$ lines signal a duty cycle for the 8155-2. The $\overline{CE}$ signal is a function of the previously mentioned I/O mapping PROMS and decoders at (A6) and (A7) sheet 2. The dual purpose address/data lines (DB0 - DB7) will contain address or data depending on the current state of the I/O operation. The ports of the 8155-2 are programmable for Input or Output depending on the user's application. (see Chap. 3)

Sockets are provided for use of various types of driver/receivers depending on the user's application. If Port 03 is programmed in Alt 3 or Alt 4 mode, PC2 can be used as a strobe for Port 1, also, PCL will be asserted by Port 1 to indicate that the Port 1 buffer is full and thereby provide a handshaking mechanism required by many application. PC0 can be used as an interrupt to the 8085-A to indicate a service request by the I/O device. The timer is addressed using the same elements as the parallel ports (See Chap. 3). The timer out line is programmable for any of 4 different signal types.

FIGURE 4 - 3
Timing

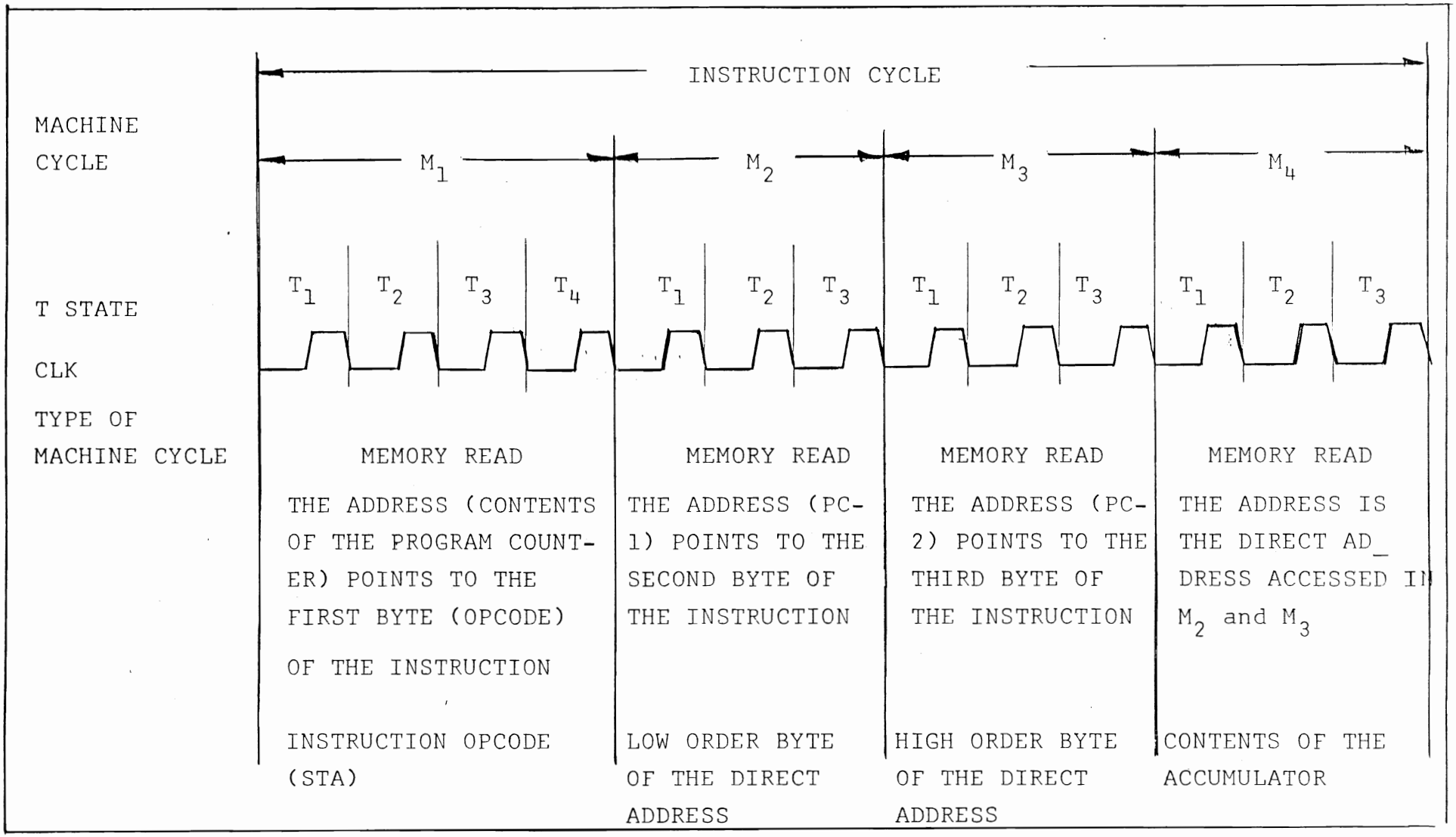


FIGURE 4 - 3 (CONTINUED)

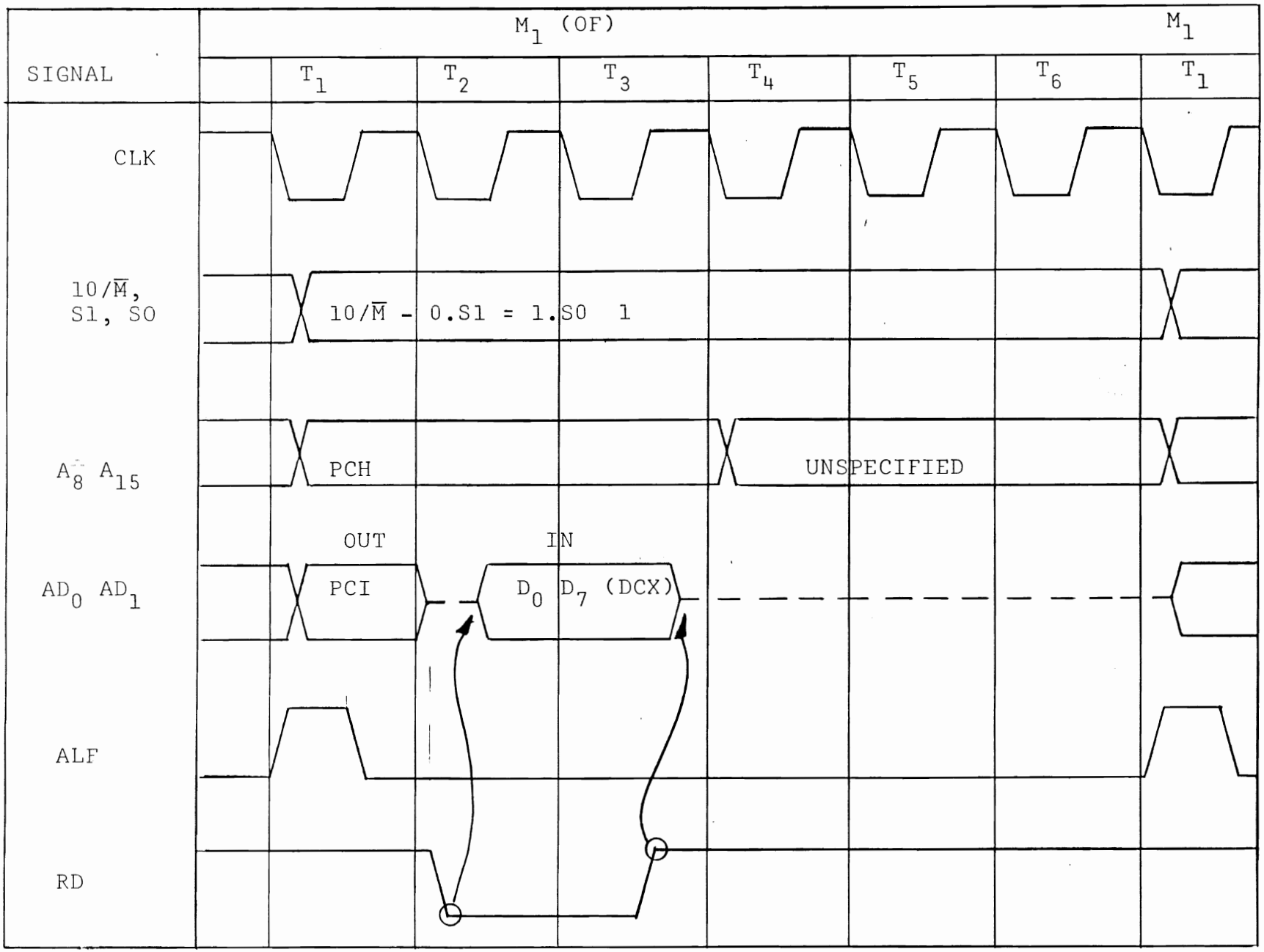
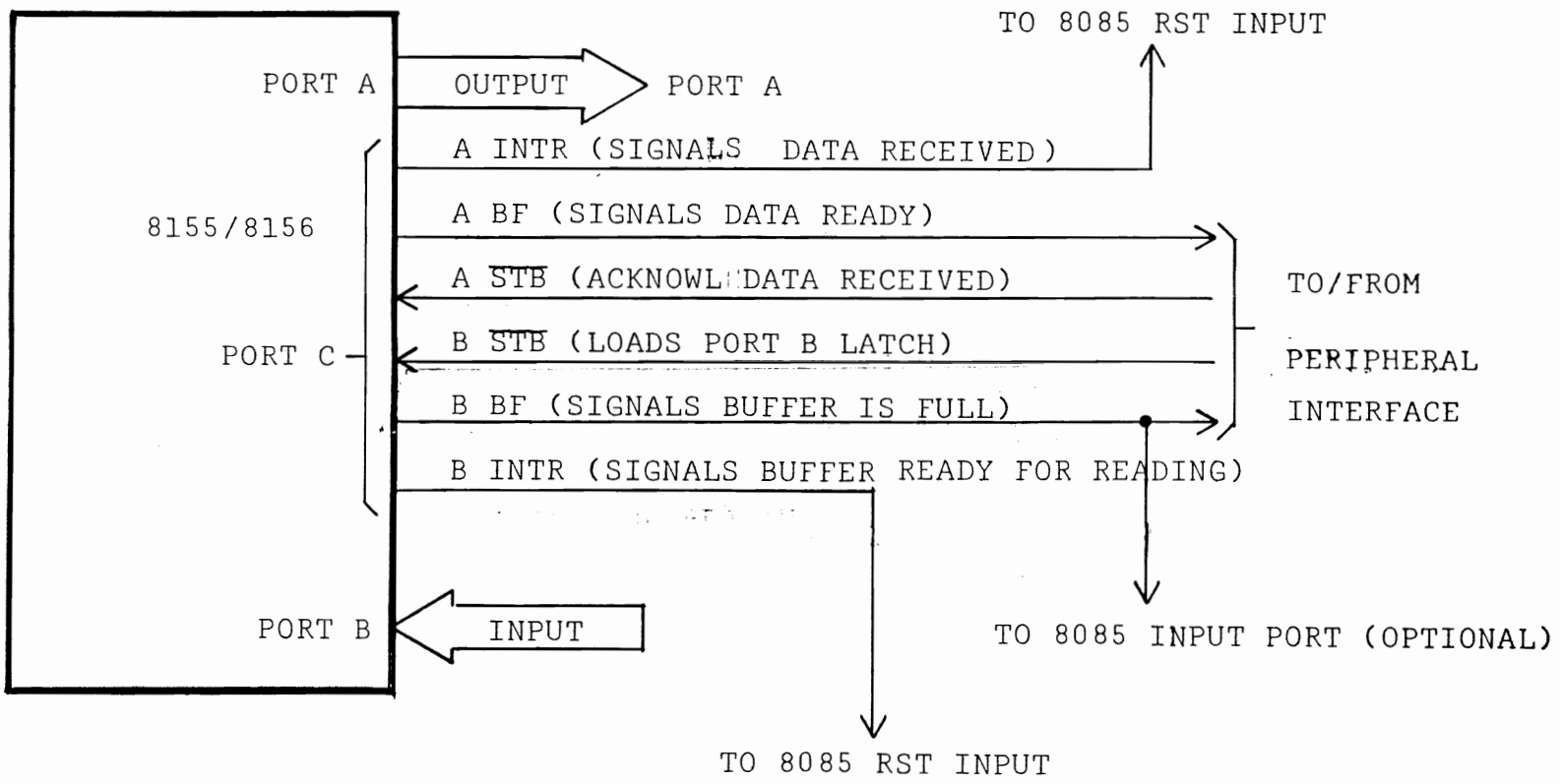


FIGURE 4 - 4

Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{\text{STB}}$ (Port A Strobe)	A $\overline{\text{STB}}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{\text{STB}}$ (Port B Strobe)

FIGURE 4 - 4 (CONTINUED)



4.10 Advanced Acknowledge

Two signals, MEMAACK/ and IO AACK/ are provided by the on-board logic of the ZX-80/05 in order to prevent a CPU wait cycle when on-board access is being made. These signals output at the decoder logics on sheet 2 and are gated at (B7) sheet 1 to the 8085A-2 ready line.

4.11 SBX Modules

Sockets J3, J4, J5 are provided for SBX type modules used for on board system expansion. These connectors bus command, control, clock, address and data to and from SBX type modules. On the ZX-80/05 board, the following signals are utilized.

1. MCLK at (A1) sheet 1 provides SBX TM basic timing (pin 6)
2. RESET at (B4) initializes SBX modules to a predetermined state (pin 5)
3. IORD/ at (B8) indicates to the SBX module that address is valid and a read operation is to be performed. (pin 15)
4. IOWRT/ at (B8) indicates to the SBX module that address is valid and a write operation is to be performed (pin 13)
5. MSCØ/, MCS1/ at (A5) sheet 2 are chip-select lines which are steered to the different SBX modules on-board and enable subsequent communications. (pins 20, 22)
6. MINTRO, MINTRI at (A8) sheet 1 are interrupt requests from the three SBX modules. (pins 12, 14)
7. OPTO, OPT1 at (A8) sheet 1 are optional signal lines provided for unique user requirements. (pins 28,30)

8. MA0, MA1, MA2 at (D8) sheet 2 are typically the three least significant I/O addresses to the SBX module. They are used in conjunction with chip select lines (above) to complete the I/O address of the SBX module. (pins 7, 9, 11)

9. MD0 thru MD7 at (D8) sheet 2 are the eight bi-directional data lines to the SBX modules. (pins 19-33 odd)

10. MPST at (A8) sheet 2 is the indication to the base board that an SBX module is installed in a particular jack. (pin 8)

11. MWAIT/ at (B8) sheet 1 will put the CPU in a wait state by removing READY when the SBX module needs additional time for I/O.

12. +5V (pins 4, 18, 36)

13. +12V (pin 1)

14. -12V (pin 2)

15. GND (pins 3, 17, 35)

16. Reserved (pins 10, 24)

TABLE 4 - 1

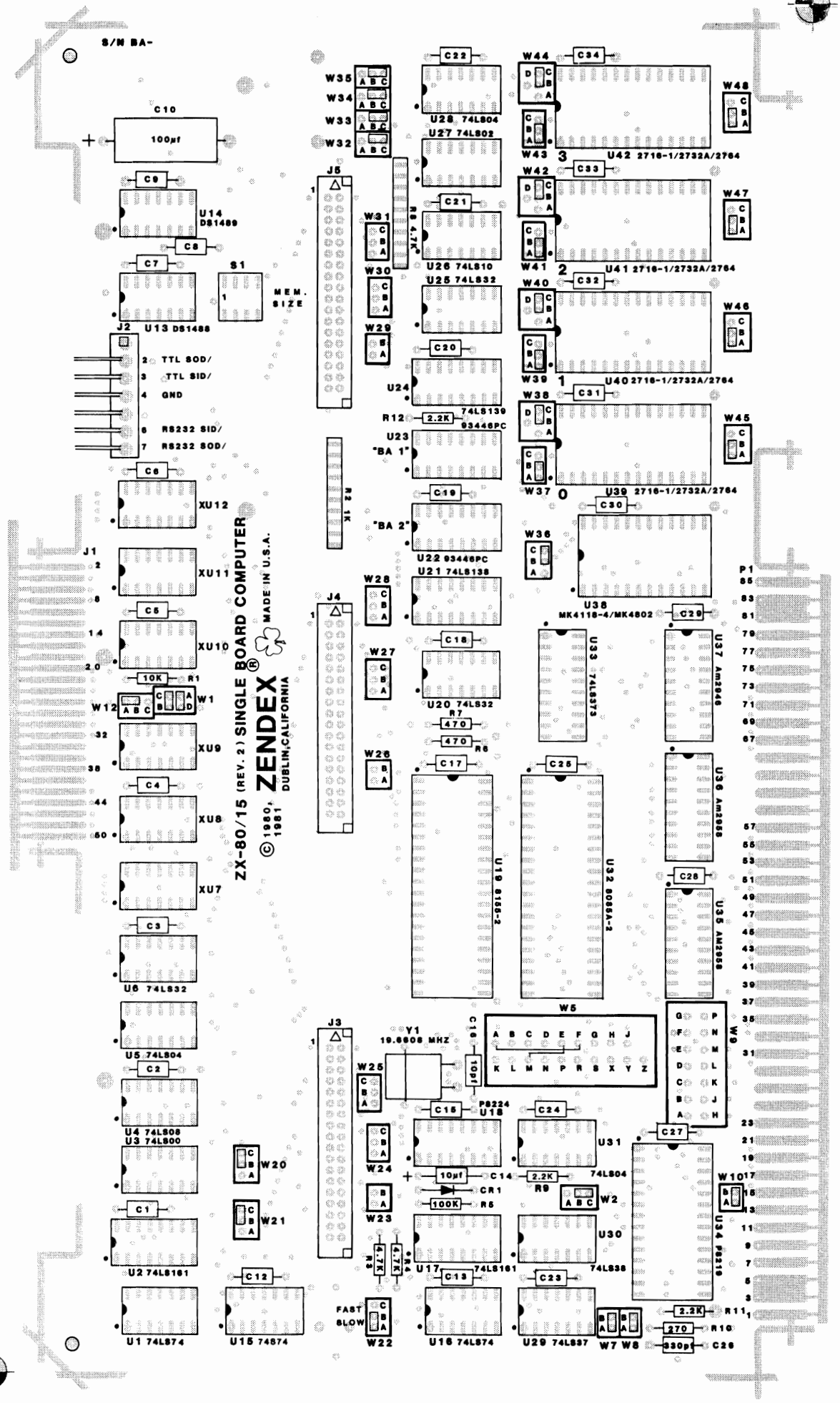
iSBX Signal Pin Assignments

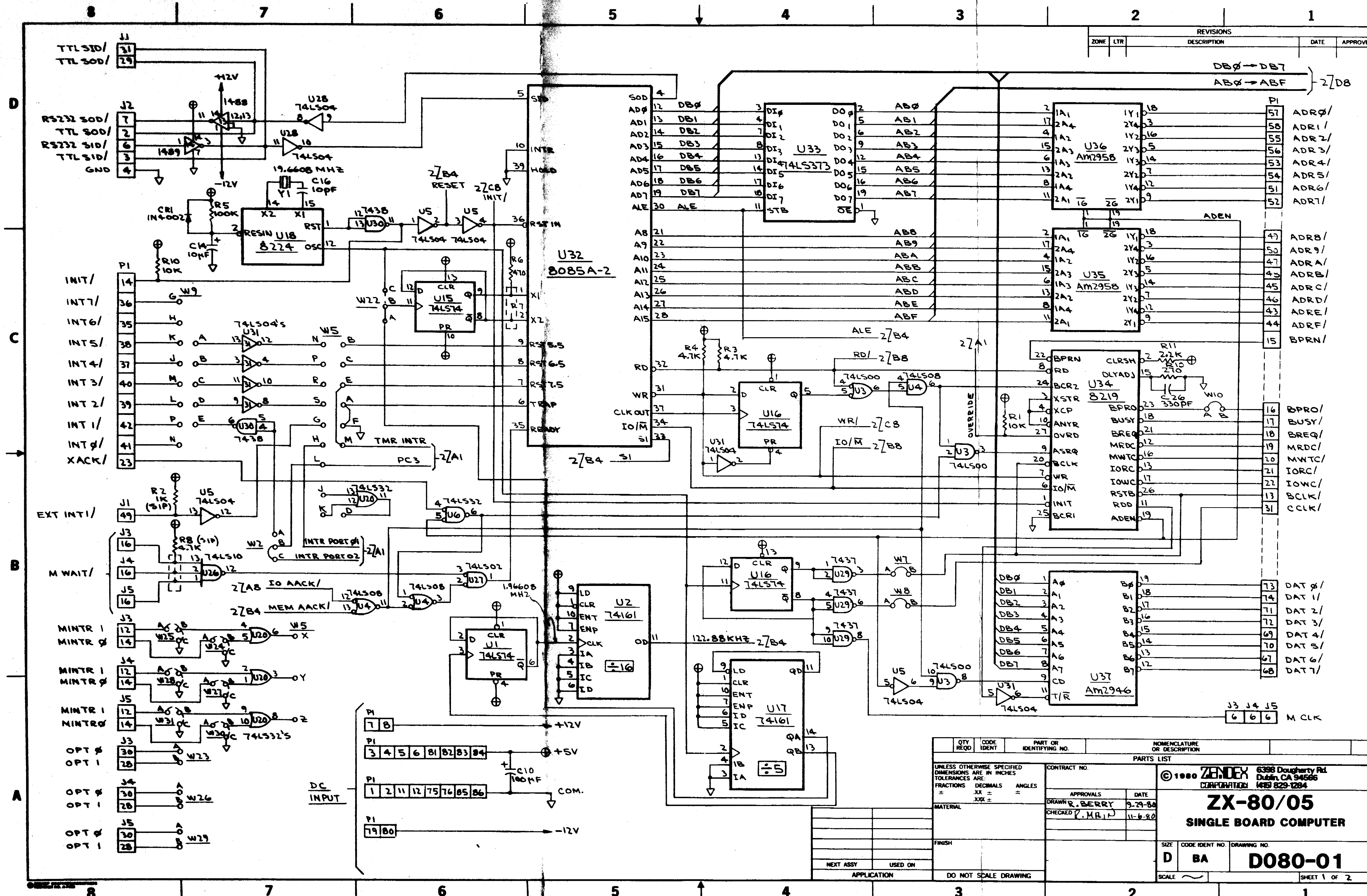
Pin	Mnemonic	Description
35	GND	Signal Ground
33	MD0	MDATA Bit 0
31	MD1	MDATA Bit 1
29	MD2	MDATA Bit 2
27	MD3	MDATA Bit 3
25	MD4	MDATA Bit 4
23	MD5	MDATA Bit 5
21	MD6	MDATA Bit 6
19	MD7	MDATA Bit 7
17	GND	Signal GND
15	IORD/	I/O Read Cmd
13	IOWRT/	I/O Write CMD
11	MA0	M Address 0
9	MA1	M Address 1
7	MA2	M Address 2
5	RESET	Reset
3	GND	Signal Gnd
1	+12V	+12 Volts

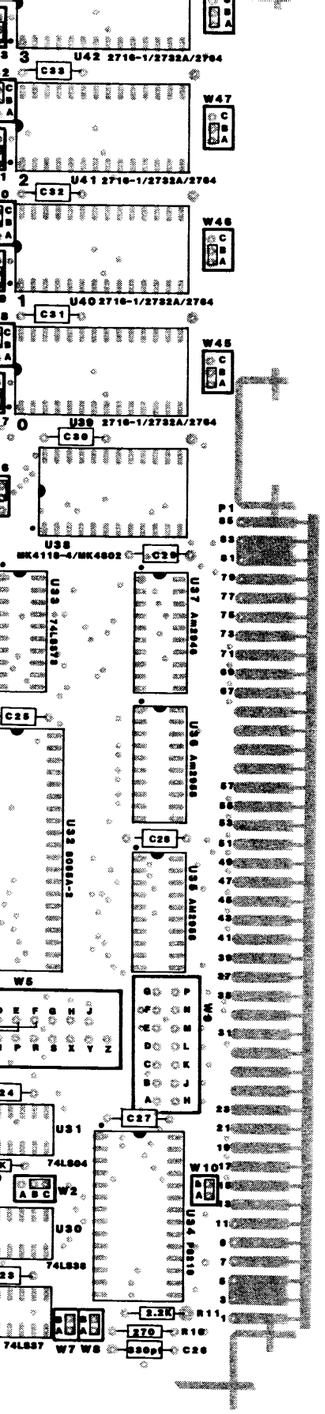
Pin	Mnemonic	Description
36	15V	15 Volts
34	MDRQT	M DMA Request
32	MDACK/	M DMA Acknowledgw
30	OPT0	Option 0
28	OPT1	Option 1
26	TDMA	Terminate DMA
24		Reserved
22	MCS0/	M Chip Select 0
20	MCS1/	M Chip Select 1
18	15V	15 Volts
16	MWAIT/	M Wait
14	MINTR0	M Interrupt 0
12	MINTR1	M interrupt 1
10		Reserved
8	MPST/	iSBX Multimodule * Board Present
6	MCLK	M Clock
4	+5V	+5 Volts
2	12V	12 Volts

All undefined pins are reserved for future use.

* and ZBX plug-in module made by Zendex


S/N BA-
C10
100µf
C9
U14 DS1489
C8
C7
S1
MEM. SIZE
J2
U13 DS1488
2 TTL SOD/
3 TTL SID/
4 GND
6 RS232 SID/
7 RS232 SOD/
C6
XU12
J1
XU11
C5
XU10
10K R1
W12
W1
XU9
C4
XU8
XU7
C3
U6 74LS32
U5 74LS04
C2
U4 74LS08
U3 74LS00
C1
U2 74LS161
U1 74LS74
W20
W21
C12
U15 74S74
ZX-80/15 (REV.2) SINGLE BOARD COMPUTER
© 1980, 1981
ZENDEX
MADE IN U.S.A.
DUBLIN,CALIFORNIA
W35
W34
W33
W32
J5
R8 4.7K
W31
W30
W29
C22
U28 74LS04
U27 74LS02
C21
U26 74LS10
U25 74LS32
C20
U24
R12 2.2K
74LS139
93446PC
U23 "BA 1"
R2 1K
C19
"BA 2"
U22 93446PC
U21 74LS138
W28
W27
W26
J4
C18
U20 74LS32
R7 470
R6 470
C17
U19 8155-2
C16
W44
C34
W48
U42 2716-1/2732A/2764
W43
W42
C33
W47
U41 2716-1/2732A/2764
W41
W40
C32
W46
U40 2716-1/2732A/2764
W39
W38
C31
W45
U39 2716-1/2732A/2764
W37
C30
W36
U38 MK4118-4/MK4802
C29
U33 74LS373
U37 Am2946
C25
U32 8085A-2
U36 Am2965
C28
U35 AM2965
W5
W9
P1
J3
Y1 19.6608 MHZ
C15 10pf
W25
C18
P8224 U18
C24
U31
W24
C14 10µf
2.2K R9
74LS04
W2
CR1
100K R5
W23
R3 4.7K
R4 4.7K
U17 74LS161
C13
U16 74LS74
U30
74LS38
C23
U29 74LS37
W7 W8
U34 P8216
W10
W22
FAST SLOW
C12
2.2K R11
270 R10
330pf C26


REVISIONS
DB∅ → DB7
AB∅ → ABF
U32 8085A-2
U33 74LS373
U36 AM2958
U35 AM2958
U34 8219
U37 AM2946
U18 8224
U2 74161
U17 74161
U15 74LS74
U16 74LS74
U1 74LS74
19.6608 MHZ
1.96608 MHZ
122.88KHZ
DC INPUT
+12V
+5V
COM.
-12V
M CLK
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DRAWN R. BERRY 9-29-80
CHECKED 11-6-80
NEXT ASSY
USED ON
APPLICATION
DO NOT SCALE DRAWING
© 1980 ZENDEX CORPORATION 6398 Dougherty Rd. Dublin, CA 94566 (415) 829-1284
ZX-80/05
SINGLE BOARD COMPUTER
SIZE D
CODE IDENT NO. BA
DRAWING NO. D080-01
SHEET 1 OF 2



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
C6	B	U15 WAS 74LS74	6-8-81	RBM

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS ± ANGLES ±
XX ±
XXX ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN R. BERRY	3-29-80
CHECKED R. MAIN	11-6-80
R. MAIN	6-13-81

ZX-80/15 (REV. 2)

SINGLE BOARD COMPUTER

SIZE	CODE IDENT NO.	DRAWING NO.
D	BA	D080-01C

SCALE ~ SHEET 1 OF 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
ALL	C	CHANGED FROM 80/05[2] 14 PIN DIP SOCKETS	12-10-81	

DB0→DB7
AB0→ABF
1ZD1

J3 J4 J5
MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7 → DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
ABB ABA ABB ABA
+5V +12V -12V GND → +12V -12V

U38 MK4118-4 "AUX RAM"
U39 MEM 0 (28 PIN SOCKET)
U40 MEM 1 (28 PIN SOCKET)
U41 MEM 2 (28 PIN SOCKET)
U42 MEM 3 (28 PIN SOCKET)
W36 A-B=4802 B-C=4118
W37 W38 W39 W40 W41 W42 W43 W44 W45 W46 W47 W48

U19 8155-2 "IO&TIMER"
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 WR/ RD/ IO/M
TIMER IN 122.88KHZ 1ZA4
RESET 1ZD6
ALE 1ZC4
CE
TIMER OUT

XU8 7438
XU7 7438
XU12 220/330
XU11 220/330
XU10 220/330
XU9 220/330
J1 BIT 0 PORT 01 BIT 7 BIT 0 BIT 7 PORT 02 BIT 0 BIT 7 PORT 03 BIT 5 * ALL EVEN PINS

U1 74LS74 PR CLR
U6 74LS32
U27 74LS03
U28 74LS04
U26 74LS10
U25 74LS32's
U3 74LS00
U24 74LS139 MEM DECODER
U23 93446PC "MEM" MAP7 "BA1"
U22 93446PC "I/O" MAP8 "BA2"
U21 74LS138 I/O DECODER
R12 2.2K
R2 1K (SIP)
R8 4.7K (SIP)
S1 MEM. SIZE (SEE TABLE 2)
W1 W12 W35 W34 W33 W32
W20 W21 W20&W21 DETERMINE SIZE OF ON-BOARD U38 RESPONSE

NOTE:
W32-W35 = A-B FOR WRITEABLE MEMORY INSTALLED IN U39-U42

1488 J2 5 RS232 RDR CTL/
PC3 INTR PORT 01 INTR PORT 02 OVERRIDE TMR INTR → 1ZB6 1ZC3 1ZC6
MEM AACK/ 1ZB7
S1 1ZB5
INT/ 1ZD6
IO AACK/ 1ZB7
IOWRT/ IORD/

MEMORY TYPE – TABLE 1

MEM. TYPE	U39-U42 PART	SIZE	PINS	W32,33 34,35	W37,39 41,43	W38,40, 42,44	W45,46 47,48
EPROM	2716-1	2K x 8	24	B-C	A-B	B-C	A-B
EPROM	2732A	4K x 8	24	B-C	A-B	B-D	A-B
EPROM	2764	8K x 8	28	B-C	A-B	B-D	A-B
RAM	MK4118-4	1K x 8	24	A-B	B-C	A-B	A-B
RAM	MK4802	2K x 8	24	A-B	A-B	A-B	A-B

ON BOARD MEMORY SIZE – TABLE 2

	SI-1	SI-2	SI-3	TYPE	PART	ROM ADDRESS	AUX RAM(U38)	W20	W21
'0'	ON	ON	ON	EPROM	2716-1	0—0FFFH	3E00-3FFFH	C-B	C-B
'1'	OFF	ON	ON	EPROM	2716-1	0—1FFFH	3C00-3FFFH	A-B	C-B
'2'	ON	OFF	ON	EPROM	2732A	0-3FFFH	7C00-7FFFH	A-B	C-B
'3'	OFF	OFF	ON	EPROM	2764	0-7FFFH	8C00-8FFFH	A-B	C-B
'4'	ON	ON	OFF	EPROM	2732A	0-1FFFH	3C00-3FFFH	A-B	C-B
5-7	~	~	OFF	NONE	~	~	~	~	~

NOMENCLATURE OR DESCRIPTION
PARTS LIST

CONTRACT NO.

APPROVALS	DATE
DRAWN R.BERRY	9-30-80
CHECKED R. MAIN	11-6-80

ZX-80/15 (REV. 2)
SINGLE BOARD COMPUTER

SIZE	CODE IDENT NO.	DRAWING NO.
D	BA	D080-01C

SCALE ~ SHEET 2 OF 2