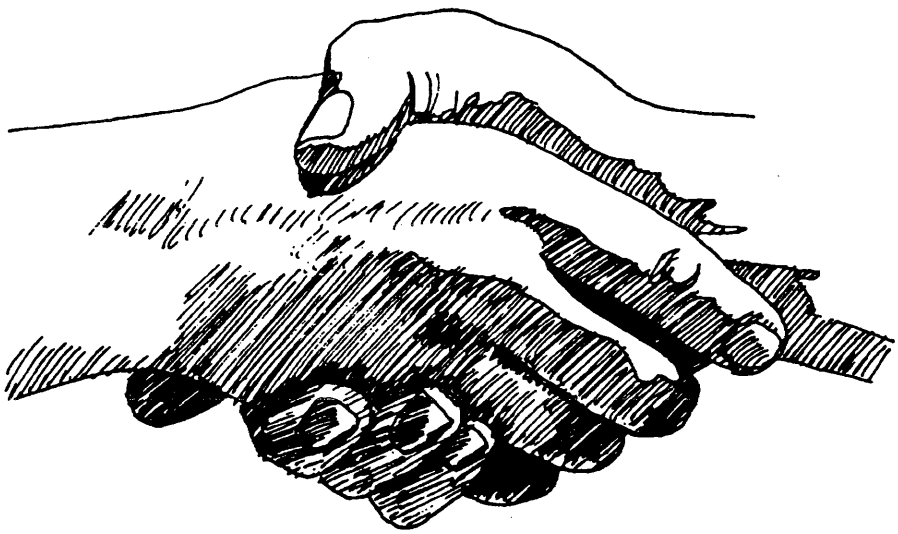
Xylogics

Model 43x
User's Manual



Your Partner For Performance

166-430-001
Revision D
July 24, 1988

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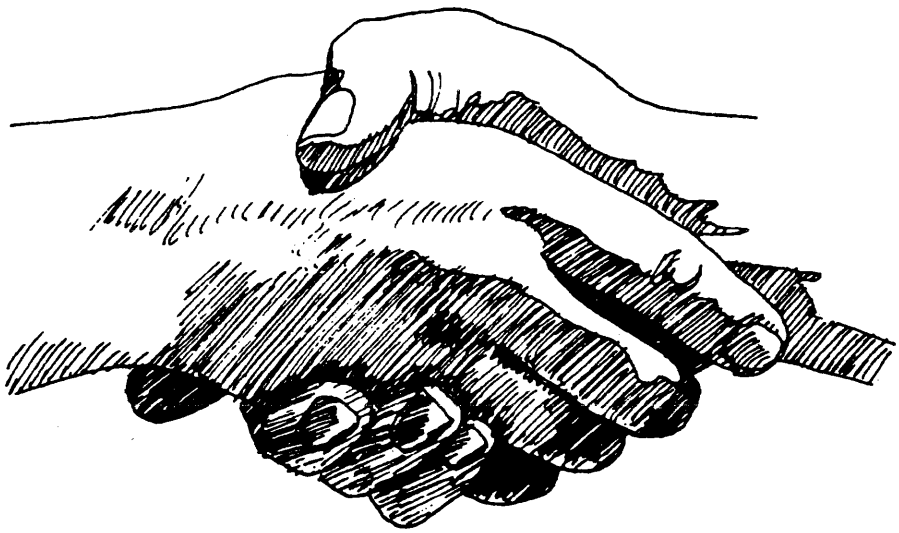

Your Partner For Performance

166-430-001
Revision D
July 24, 1988

43x Revision Level History

Revision	Description
Rev. A (9/2/85)	Initial release.
Rev. A1 (12/5/85)	Technical change. Clarified Sections 5.6.1 and 5.6.2. **Note** *Only pages 105, 106, and the Table of Contents are marked Rev. A1.*
Rev. B (1/9/86)	Technical clarifications throughout the manual. Section 7 now reflects the 431S and the 432. Section 8 reflects the 431T. All subsequent sections increment by one.
Rev. B1 (12/5/86)	Technical corrections/additions. Revised subsection numbers in Sections 3 and 4. Added Sections 3.8.6 (Spiral Format), 3.13 (Winchester Disk Send Serial command), and 3.14 (Winchester Disk Read Defect Map command). Section 7.2.3: jumper J-P corrected to read J-D; jumper J-I on Figure 7-1 corrected to read J-D. Sections 7.2.8 and 8.2.8 removed: the 43x does not support CBRQ/. Added Sections 7.2.9 and 8.2.9 (Light Emitting Diodes). Added information to Section 7.2.12 regarding 5.25-inch high performance quad density floppy disk drives. Added Figure 9-1 (431 Block Diagram).
Rev. C (4/1/87)	Technical corrections/additions. Removed all references to head offset. Added Sections 7.2.6 (Bus Busy) and an addendum explaining the basic differences between the 431S and the 431T.
Rev. D (7/24/88)	Section 2.4 renamed Section 3. All subsequent sections increment by one, i.e., 3=4, 4=5, etc. Added information regarding the 15-MHz 432 to Sections 1, 4, and 8. Added the *High Performance* bit (bit 5, byte 8) to the Floppy Read Drive Status and Set Drive Parameters IOPBs. Added error 56 (header error) to Table 6-1.

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Section 1: Specifications

Section 1: Specifications

1.0 Introduction

The Xylogics Model 43x peripheral controller is a triple function controller for Multibus™ systems. The 43x can run both Winchester and tape or floppy drives simultaneously, alternating DMA bursts between the peripherals as needed. The 43x implements data and command transfers via DMA, allowing maximum throughput; it implements system control via Input/Output Parameter Blocks (IOPBs) and byte I/O Registers. The 43x circuitry includes a DMA sequencer, disk sequencer, tape sequencer, floppy disk controller chip, and a microprocessor for control.

The Xylogics Model 431 controller connects up to two ST506/412 5.25-inch Winchester disk drives to the IEEE 796 Multibus system; the 432 connects up to two ESDI Winchester disk drives. The 431 and 432 also connect up to two SA400 5.25-inch floppy disk drives and one QIC-02 1/4-inch streaming tape drive to the Multibus system.

1.1 Using this Manual

This manual provides two system software reference cards that illustrate the IOPB structure and codes (see inserts). The following sections detail the operation of the 43x family of Multibus disk and tape controllers. Each controller supports a different array of options; some of these options may not be applicable to the particular controller you are using.

> *Unless otherwise noted, the word* **disk** *refers to both Winchester and floppy disks.*

1.1.1 Abbreviations

This manual uses the following mnemonics:

BPI	Bits per Inch
BOT	Beginning of Tape
BOM	Beginning of Media (BOT, Track 0)
CCR	Controller Command Register
CPU	Central Processing Unit

Multibus is a trademark of Intel Corporation.

1.1.1 Abbreviations (continued)

CRC	Cyclical Redundancy Check
CSR	Control and Status Register
DMA	Direct Memory Access
ECC	Error Correction Code
EOD	End of Data
EOM	End of Media (EOT, Last Track)
EOT	End of Tape
ESDI	Enhanced Small Device Interface
FD	Floppy Disk
FDC	Floppy Disk Controller Chip
FIFO	First In/First Out Buffer
GCR	Group Coded Recording
H	Notation for Hexadecimal Values
I/O	Input/Output
IOPB	Input/Output Parameter Block
IPS	Inches Per Second
KB	Kilobytes
KBS	Kilobytes Per Second
LED	Light Emitting Diode
MB	Megabytes
MBS	Megabytes Per Second
NRZI	Non-return to Zero, Change on One
PE	Phase Encoded
PLL	Phase Lock Loop
RAM	Random Access Memory
ROM	Read Only Memory
RTZ	Return to Zero

1.2 Design Reliability

The following Xylogics features minimize the likelihood of product failure:

- Low-stress design on all components.
- All components burned-in.
- One card; resides in backplane or expansion chassis.
- Controller is power-cycled under thermal stress during test.
- Custom gate arrays.

1.3 Physical

Packaging: The 43x completely resides on one printed circuit board. It plugs into any 16-, 20-, or 24-bit Intel Multibus or IEEE P796 card cage.

Dimensions: The 43x is 12-inches long by 6.75-inches high (30.48 cm by 17.15 cm); it is identical in form-factor to the standard Intel Multibus, and IEEE P796 printed circuit board.

Shipping Weight: 3 pounds (1.4 kg).

1.4 Environmental

The 43x environmental requirements are similar to the Intel 86/12 SBC or equivalent Multibus processors (typically 0–55°C; up to 90% relative humidity without condensation). The 43x requires sufficient air circulation for cooling.

1.5 Electrical

Power: The 43x requires 6 amperes at +5 VDC nominal; 6.4 amperes maximum, with peripherals connected.

Tolerance: Voltages must be within plus or minus 5% (4.75 to 5.25).

1.6 System-related Specifications

Transfer Control: Direct Memory Access (DMA).

DMA Throttle Control: Programmable throttle value supports any Multibus throughput speed.

Interrupt Priority: Multibus INT5/, standard; others jumper selectable.

Interrupts: Non-bus vectored.

Control Technique: Channel driven control; programmable microprocessor.

1.6 System-related Specifications (continued)

Addressing Capability: 16-, 20-, and 24-bit.

IOPB Length: 24 bytes.

Controller Registers: Five 8-bit I/O Registers; byte addressable only.

I/O Addressing Capability: The 43x decodes byte addresses for its on-board registers; it responds to 8- or 16-bit I/O addresses.

DMA Data Transfer Modes: The 43x transfers data in bytes or words.

IOPB Transfer Modes: The 43x transfers IOPBs in bytes or words.

Winchester Disk Data Buffering: On-board FIFO memory holds 4K-bytes.

Floppy Disk Data Buffering: On-board 128-byte FIFO buffer connects between the floppy interface and a 128-byte DMA buffer.

Tape Data Buffering: On-board 512-byte buffer.

Disk Data Transfer Limit: Data transfer length from 1 to 65,535 sectors.

Tape Data Transfer Limit: Data transfer length from 1 to 65,535 blocks.

Software Support: Sample software drivers supplied for use in UNIX™ or RMX-86™ systems (source included).

Status LEDs: The 43x implements two status LEDs. L1 is the Active LED; it indicates when the 43x is ready for commands. L2 is the Busy LED; it indicates the successful completion of on-board diagnostics.

DMA Data Transfer Rate: The system memory XACK response time determines the rate at which the 43x transfers data to memory. With a XACK of 300 ns, the 43x achieves a data rate of up to 2.5 MBS. The maximum data rate for an ST506 disk drive is 625 KBS. The maximum data rate is 1.8 MBS for an ESDI disk drive and 200 KBS for a tape drive.

1.7 Disk Drive-related Specifications

1.7.1 Winchester Disk Drives

Disk Interface : 431 - ST506/412-type drives (Industry standard).
432 - ESDI (Enhanced Small Device Interface).

Maximum Disk Capacity: Limited by the capacity of currently available disk drives.

Number of Disk Drives: The 43x supports up to two Winchester disk drives, including any mix of capacities.

Header Format: Contains sector, head, cylinder address, drive type and header ECC.

Disk Data Verification: Built-in 32-bit ECC word on both the header and data portions of the sector. The ECC word detects and corrects error bursts up to 11-bits long, assuring data integrity. On-board, automatic data error correction is software programmable.

Implied Seek Capability: Data transfer commands contain an inherent implied seek.

Overlap Seek Capability: When an IOPB chain requests more than one drive, the controller may initiate implicit overlap seeking, if the drive interface supports the feature (software programmable).

Bit Cell Time: 431 - 200 ns.
432 - 100 ns.
432-103 (and above) - 66 ns.

Disk Data Transfer Rate: ESDI - 10-MHz peak;
432-103 (and above) - 15-MHz peak.
ST506/412 - 5-MHz peak.

Cabling: Standard flat cable for appropriate interface.

Defective Sectors: The 43x skips a defective sector and reads the next sector on each track.

1.7.2 Floppy Disk Drives

Disk Interface: Industry standard floppy disk interface; compatible with SA400 series.

Maximum Disk Capacity: Single density; 250 KB per surface.
Double density; 500 KB per surface.
Quad density available on models 432–103 and above.

Number of Disk Drives: The 43x supports up to two floppy disk drives, including any mix of capacities.

Header Format: Header contains sector, head, cylinder address, and header CRC. The 43x only writes headers when it formats the media.

Disk Data Verification: Built-in 16-bit CRC on both the header and data portions of the sector. The CRC detects errors, assuring data integrity.

Implied Seek Capability: Data transfer commands contain an inherent implied seek.

Overlap Seek Capability: The 43x does not support overlap seeking on floppy disks.

Disk Data Transfer Rate: 250 KBS with double density (DD), using MFM recording; 125 KBS with single density (SD), using FM recording.

Cabling: Standard 34-pin flat ribbon cable and connectors.

1.7.3 Tape Drives

Tape Interface: Industry standard; QIC-02.

Maximum Tape Capacity: Limited by the capacity of currently available tape drives.

Number of Tape Drives: The 43x supports one tape drive.

Tape Speed: 45 or 90 IPS.

Tape Density: 8,000 BPI.

1.7.3 Tape Drives (continued)

Number of Tracks: Drive-dependent.

Tape Position and Data Verification: Inherent in the QIC-02/24 tape drive and recording format using NRZI (Non-return to Zero, Change on One) with GCR (Group Coded Recording) and CRC (Cyclical Redundancy Check).

Tape Data Transfer Rate: 88 KBS average; drive-dependent. The data rate burst between the tape drive and the controller can be greater than 200 KBS.

Cabling: Standard QIC-02 compatible, 50-pin flat ribbon cable and connectors.

1.8 Programmable Features

- Software controlled 16- or 20/24-bit DMA data address bus support.
- Software controlled 8- or 16-bit DMA transfers.
- Software controlled interrupt or software polled operation.
- Software programmable DMA throttle.
- Sector interleaving software programmable during format (standard 1:1).

1.9 Command Technique

The 43x command technique allows command-chaining and concurrent host and disk controller operations. Channel control allows a software driver to establish disk or tape drive commands in an IOPB in system memory. Section 3 describes the use of specific bits within the IOPBs; Table 3-2 lists IOPB formats.

The 43x reads the command IOPB from system memory by Direct Memory Access (DMA) and performs the required function. After completing an IOPB, the 43x writes a completion code into Bytes 4 and 5 (also 6 and 7 for tape) of the IOPB related to the completed operation. The following procedures clear hard errors:

- Set CLRE in the Controller Command Register (CCR); or
- Execute a *Controller Reset* (set CRST in the CCR); or
- Set *Go* in the Controller Command Register; or
- Execute a Multibus *INIT/*.

1.9.1 Command-chaining

The 43x has an inherent command-chaining capability for multiple operations. The software driver sets up a string of commands that execute a series of operations without operating system intervention. At any time, system software can add new IOPBs and/or remove completed IOPBs from the chain using the attention protocol. Command-chaining may provide overlap seeking on Winchester disks in multidrive systems (see Section 5.2).

Section 2:
Programming Reference

Section 2: Programming Reference

2.0 Introduction

This section describes how to program the Xylogics Model 43x peripheral controller. The 43x easily interfaces many different processors with a wide variety of disk and tape drives.

2.1 Programming Techniques

The IOPB resides in system memory and contains the 43x command parameters. The CPU writes and reads the IOPB with byte or word instructions. The 43x reads and writes the IOPB with byte or word mode DMA.

Set up the 43x commands by preparing an IOPB in system memory. System software loads the IOPB address into the I/O Registers and sets the *Go* bit in the Controller Command Register (CCR). The 43x clears the *Controller Ready* (CRDY) bit in the Control and Status Register (CSR), and transfers the IOPB from memory at the start of a command; it processes the command, stores status information in the associated IOPB, and sets CRDY in the CSR on completion. While processing the command, the 43x can access the IOPB again and can also DMA data to or from system memory. The 43x may chain IOPBs together. When the *Chain Enable* (CHEN) and *Overlap Seek* (OVS) bits are set, the 43x can initiate overlap seeking on multiple drives and execute data transfers without operating system intervention.

Each byte in the IOPB has an address relative to the first byte in the IOPB. Reserving all 24 bytes of allowable space maintains IOPB integrity.

2.2 Multibus Address Relocation

The 43x addresses Multibus memory using a technique called address relocation. Address relocation is the addition of two addresses to form a larger physical address.

2.2 Multibus Address Relocation (continued)

This manual refers to both IOPB relocation and data relocation. Do not confuse them. IOPB relocation refers to the method of computing the address at which the IOPB resides in memory. Data relocation refers to the method of computing the data buffer address. The jumper for 24-bit address selection affects address relocation for both data and IOPBs.

2.2.1 20-Bit Address Relocation

The 43x forms a 20-bit physical address by adding a 16-bit address word to a shifted 16-bit relocation word. The 43x shifts the relocation word by four bits. This combined address is the 20-bit Multibus address.

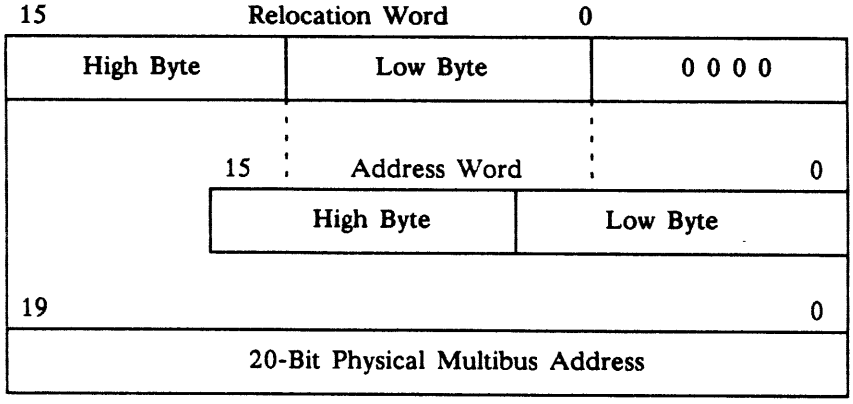


Figure 2-1. 20-Bit Multibus Address Relocation

2.2.2 24-Bit Address Relocation

The 43x calculates a 32-bit physical address for 24-bit address relocation. The address word comprises the least significant 16 bits. The relocation word comprises the most significant 16 bits. When addressing memory, the 43x only uses the lower 24 bits of the physical address.

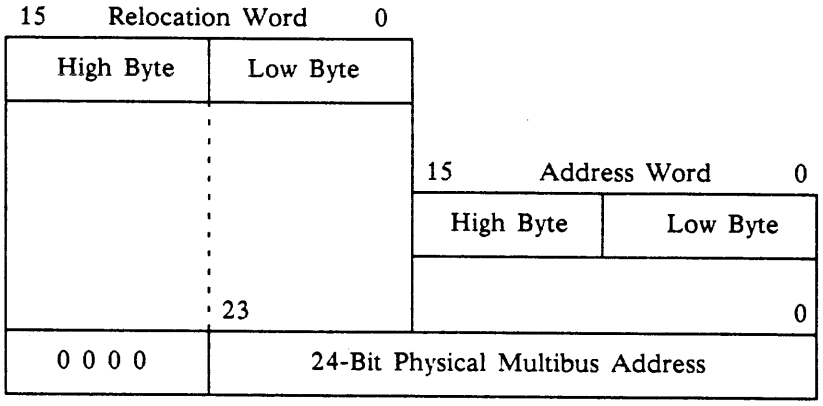


Figure 2–2. 24-Bit Multibus Address Relocation

2.2.3 IOPB Address Relocation

IOPB relocation occurs whenever a value is loaded into the IOPB Relocation Registers. The 43x combines the IOPB Address Registers and IOPB Relocation Registers and forms either a 20- or 24-bit physical memory address (see Figure 2–1 and Figure 2–2).

When chaining IOPBs, the 43x adds the Relocation Registers to the Next IOPB Address bytes and forms a new 20- or 24-bit physical Multibus address. This address points to the next IOPB in the chain. All IOPBs in a chain must reside in the same 64K-byte segment whose base address is in the Relocation Registers. The 43x computes the base address by shifting the Relocation Registers 4 or 16 bits to the left, depending on the relocation mode.

2.2.4 Data Transfer Address Relocation

IOPB Bytes C, D, E, and F specify the starting memory address for a data transfer operation. If RELO is clear, the Data Address bytes (IOPB Bytes C and D) specify the transfer's physical Multibus address. If RELO is set, the 43x uses Bytes E And F as the Data Relocation bytes, and Bytes C and D as the Data Address bytes. Data relocation occurs in the same manner as IOPB relocation (see Figure 2-1 and Figure 2-2).

2.3 Register Addressing

The 43x Input/Output Registers are addressed as input/output byte ports on the Multibus. The I/O Registers use a standard base address of 80H for 8-bit addressing or EE80H for 16-bit addressing. Table 2-1 summarizes the 43x I/O Registers (see Section 8.2.3 for alternate base addresses).

Table 2-1. Input/Output Register Addresses (Hex)

Use	8-Bit	16-Bit
IOPB Relocation Register Low Byte	80	EE80
IOPB Relocation Register High Byte	81	EE81
IOPB Address Register Low Byte	82	EE82
IOPB Address Register High Byte	83	EE83
Control and Status Register (Read)	84	EE84
Controller Command Register (Write)	84	EE84

2.3.1 Relocation Registers (Low Byte Address 80 or EE80) (High Byte Address 81 or EE81)

The Relocation Register comprises two bytes. These bytes may be read at any time, but may only be written when CRDY is set. The Relocation Register is the most significant portion of the IOPB memory address. The 43x clears this register on power-up, Multibus *INIT/*, and a *Controller Reset*. Clear this register to zero when running in 16-bit addressing mode. Writing anything but zero to this register causes IOPB relocation. When the controller is set for 20- or 24-bit addressing, it relocates the IOPB using the value in this register.

2.3.1 Relocation Registers (continued)

A jumper option enables 24-bit memory addressing. Bit 3 (ADRM) in the CSR indicates the jumper's status; if set, the 43x is jumpered for 24-bit addressing. In extended addressing mode, the Relocation Register comprises the most significant 16 bits of a 32-bit physical memory address. The Address Register comprises the least significant 16 bits. The 43x ignores the high byte of the Relocation Register in this mode, and generates 24-bit addresses.

2.3.2 Address Registers

(Low Byte Address 82 or EE82)
(High Byte Address 83 or EE83)

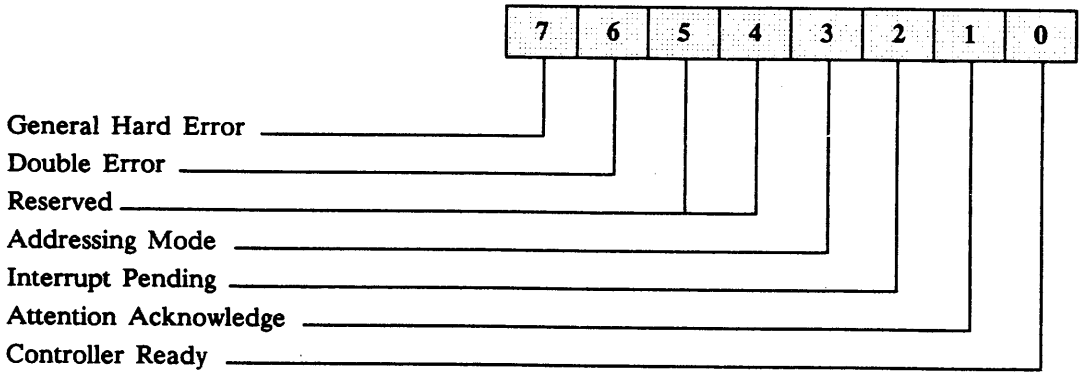
There are two Address Registers: one contains the low byte of the IOPB address, the other contains the high byte. These registers are the least significant portion of the IOPB memory address. The 43x clears these registers during a power-up, Multibus *INIT/*, or a *Controller Reset*. While executing an IOPB chain, the Address Register points to the address that was loaded when *Go* was set, unless the 43x encounters a hard error.

> *All IOPB registers may be read at any time, but may only be written when CRDY is set. A register write at any other time flags a busy conflict or general error.*

2.3.3 Control and Status Register

(Low Byte Address 84 or EE84)

This register has two functions. When read, it is defined as the Control and Status Register (CSR); when written, it is defined as the Controller Command Register (CCR).

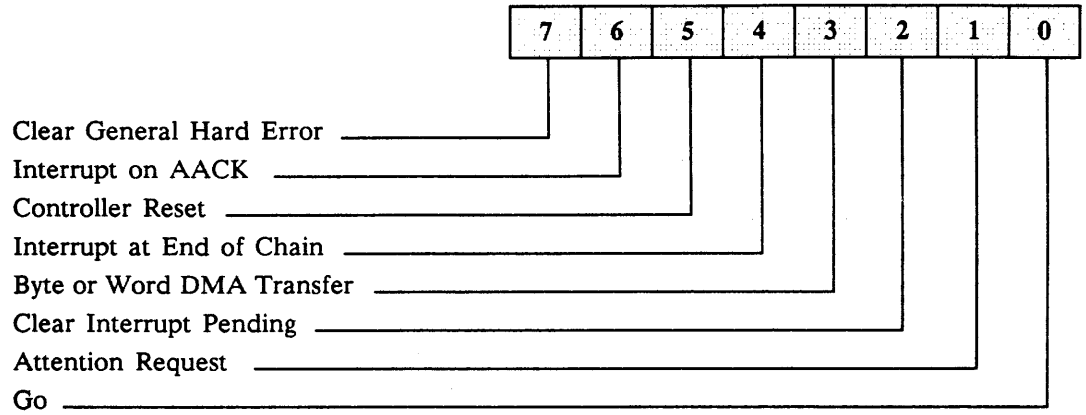


2.3.3 Control and Status Register (continued)

Bit	Mnemonic	Description
7	ERR	**General Hard Error:** The 43x sets ERR when it encounters a hard error, and writes the error status into the IOPB Status bytes. Hard errors stop IOPB processing. Setting CLRE or CRST before issuing another *Go* clears a hard error. If the error is not cleared, setting *Go* clears ERR, EFF, IPND, and AACK.
6	DERR	**Double Error:** The 43x sets DERR when it encounters more than one error; it returns a completion code for the most severe error in the IOPB. DERR can also indicate the 43x did not properly DMA the IOPB error to system memory. Clear DERR by setting CLRE or CRST.
		It is more efficient to clear an error by setting CLRE than by setting CRST. A Controller Reset terminates all IOPB processing and takes up to 100 microseconds to execute.
5-4		**Reserved.**
3	ADRM	**Addressing Mode:** When set, the 43x supports 16- or 24-bit addressing, subject to relocation. When clear, the 43x supports 16- or 20-bit addressing. Jumper JA, pins 21–22, selects the addressing mode. The 43x reads ADRM on power-up. The addressing mode is not software programmable (see Sections 8.2.3 through 8.2.5).
2	IPND	**Interrupt Pending:** Sets when an interrupt is pending. Three procedures clear the *Interrupt Pending* bit: setting CLRI, setting CRST, and setting *Go* for the next command.
1	AACK	**Attention Acknowledge:** The 43x sets AACK to acknowledge an AREQ by system software. Software may now add new and/or remove completed IOPBs. The 43x clears AACK after software clears the *Attention Request. Do not issue another request until the 43x clears AACK.* When set, the 43x generates an interrupt if IAA is set. Software may only add new IOPBs to the end of the chain (see Section 6.2).
0	CRDY	**Controller Ready:** Sets when the 43x is ready to accept new command information. When clear, only AREQ, CLRI, and CRST have write access. The 43x sets CRDY after completing the last IOPB in a chain, or encountering a hard error that halts IOPB processing.

2.3.4 Controller Command Register (Low Byte Address 84 or EE84)

The Command Register is a write only register that gives system software control of the 43x.



Bit	Mnemonic	Description
7	CLRE	**Clear General Hard Error:** When set, the 43x clears ERR and DERR in the CSR. Set CLRE only when CRDY is set.
6	IAA	**Interrupt on AACK:** When set, the 43x issues an interrupt whenever it sets AACK in the CSR. Setting IAA is only valid when simultaneously setting *Go*. When clear, system software polls the CSR and determines AACK's status.
5	CRST	**Controller Reset:** Setting CRST initializes the 43x without initializing all the devices on the bus: the 43x registers clear to zero. You may write CRST at any time; however, a *Controller Reset* terminates any IOPB processing. A *Controller Reset* does not clear the maximum parameters on a Set Drive Parameters command.
4	IEC	**Interrupt at End of Chain:** When set, the 43x issues an interrupt at the end of an IOPB chain. If a hard error occurs, the 43x defines it as the end of the chain. Setting IEC is only valid when simultaneously setting *Go*. When clear, and ITI in the IOPB and IAA in the CCR are clear, the 43x does not interrupt.

2.3.4 Controller Command Register (continued)

Bit	Mnemonic	Description
3	BWM	**Byte or Word Mode DMA Data Transfer:** Selects either word or byte mode data transfers between the 43x and system memory, allowing the 43x to operate with word- and byte-oriented memory mixtures. When clear, the 43x reads or writes 16-bit words in memory. When set, the 43x reads or writes bytes in memory. Setting BWM is valid only when simultaneously setting *Go*. If CRDY is clear, and you are clearing IPND and/or AREQ, BWM must be clear, regardless of the controller mode. The 43x decodes BWM only when system software sets *Go*. If software specifies word mode, but the starting address is odd, the 43x reverts to byte mode for the first byte, then switches to word mode, and then switches back to byte mode for the last byte.
2	CLRI	**Clear Interrupt Pending:** You may set CLRI at any time. Setting CLRI clears an interrupt and IPND in the CSR.
1	AREQ	**Attention Request:** System software sets AREQ when it wishes to service the IOPB chain. The 43x responds by setting AACK in the CSR. System software may now add new IOPBs to the end of the chain or remove completed IOPBs. After software manipulates the chain, it clears AREQ, completing the attention protocol, and releases the chain to the 43x. The 43x clears AACK after software clears AREQ. When AACK is set, the 43x continues processing any IOPBs stored in its internal buffers.
0	GO	**Go:** When set, the 43x processes the IOPB (chain) pointed to by the Address Registers. Set *Go* only when CRDY is set in the CSR. When set, *Go* clears all errors, IPND, and AACK.

While the 43x is busy (CRDY clear), only CRST, CLRI, and AREQ have register write access. Writing any other bit causes a busy conflict error.

The 43x only accepts IAA, IEC, and BWM when simultaneously writing Go. Changing these bits at any other time does not affect the 43x.

Section 3: IOPB Description

Section 3: IOPB Description

3.0 Introduction

An IOPB comprises 24 bytes, all of which have standard definitions. Some bytes have optional definitions, depending on the command. The tables in Section 3.1 list the standard and optional byte definitions for disk and tape. *Unless otherwise noted, the word* **disk** *refers to both Winchester and floppy disks.* If IOPB relocation is enabled, all IOPBs in a chain must exist in the same 64K-byte segment whose base address is specified by the 43x IOPB Relocation Registers. This section describes the byte definitions for all devices. Section 4 describes disk commands and Section 5 describes tape commands.

3.1 IOPB Byte Definitions

Table 3-1. IOPB Byte Definitions for Floppy Disks

Standard Byte	Optional Byte
00 Device Type/Unit Select	00 ---
01 Command Byte	01 ---
02 Next IOPB Address Low	02 ---
03 Next IOPB Address High	03 ---
04 Controller Status Byte 0	04 ---
05 Controller Status Byte 1	05 ---
06 Head Address	06 Drive Option
07 Sector Address	07 Max Sector
08 Cylinder Address	08 Max Cylinder
09 Reserved	09 ---
0A Sector/Track Count Low	0A Read Drive Status
0B Sector/Track Count High	0B Firmware Revision Code
0C Memory Data Address Low	0C ---
0D Memory Data Address High	0D Bytes Per Sector
0E Memory Data Relocation Low	0E Length of Gap 3
0F Memory Data Relocation High	0F Recording Format
10 Throttle	10 ---
11 Mode	11 ---
12 Subfunction Code	12 ---
13-17 Reserved	13-17 ---

3.1 IOPB Byte Definitions (continued)

Table 3-2. IOPB Byte Definitions for Winchester Disks

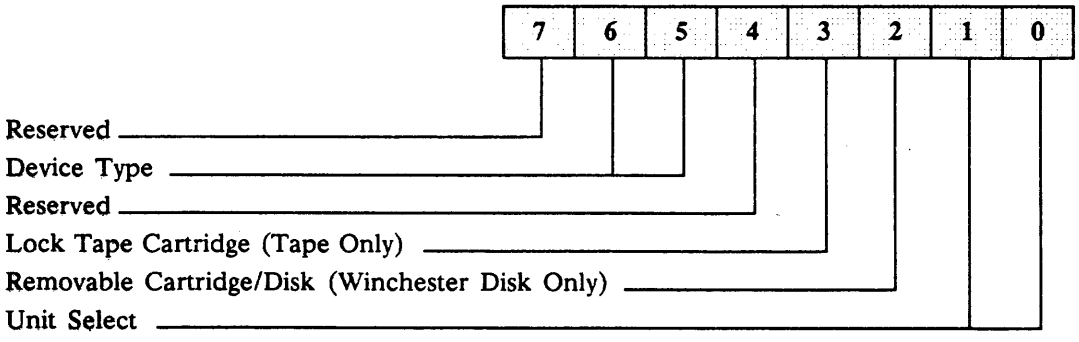
Standard Byte		Optional Byte	
00	Device Type/Unit Select	00	---
01	Command Byte	01	---
02	Next IOPB Address Low	02	---
03	Next IOPB Address High	03	---
04	Controller Status Byte 0	04	---
05	Controller Status Byte 1	05	---
06	Head Address	06	Drive Option
07	Sector Address	07	Max Sector
08	Cylinder Address Low	08	Max Cylinder Low
09	Cylinder Address High	09	Max Cylinder High
0A	Sector/Track Count Low	0A	Read Drive Status
0B	Sector/Track Count High	0B	Firmware Revision Code
0C	Memory Data Relocation Low	0C	Bytes Per Sector
OD	Memory Data Address High	0D	Bytes Per Sector
0E	Memory Data Relocation Low	0E	Reduced Write Current/ Precompensation Starting Cylinder Low
0F	Memory Data Relocation High	0F	Reduced Write Current/ Precompensation Starting Cylinder High
10	Throttle	10	---
11	Mode	11	---
12	Subfunction Code	12	---
13	Reserved	13	---
14	ECC Mask Pattern Low	14	---
15	ECC Mask Pattern High	15	---
16	ECC Bit Address Low	16	---
17	ECC Bit Address High	17	---

3.1 IOPB Byte Definitions (continued)

Table 3-3. IOPB Byte Definitions for Tape Drives

Standard Byte		Optional Byte	
00	Device Type/Unit Select	00	---
01	Command Byte	01	---
02	Next IOPB Address Low	02	---
03	Next IOPB Address High	03	---
04	Controller Status Byte 0	04	---
05	Controller Status Byte 1	05	---
06	Reserved	06	Tape Status Byte 0
07	Reserved	07	Tape Status Byte 1
08	Reserved	08	Tape Status Byte 2
09	Reserved	09	Tape Status Byte 3
0A	Block Count Low	0A	Tape Status Byte 4
0B	Block Count High	0B	Tape Status Byte 5
0C	Memory Data Address Low	0C	---
0D	Memory Data Address High	0D	---
0E	Memory Data Relocation Low	0E	---
0F	Memory Data Relocation High	0F	---
10	Throttle	10	---
11	Mode	11	---
12	Subfunction Code	12	---
13-17	Reserved	13-17	---

3.1.1 Device Type/Unit Select (IOPB Byte 0)



3.1.1 Device Type/Unit Select (IOPB Byte 0) (continued)

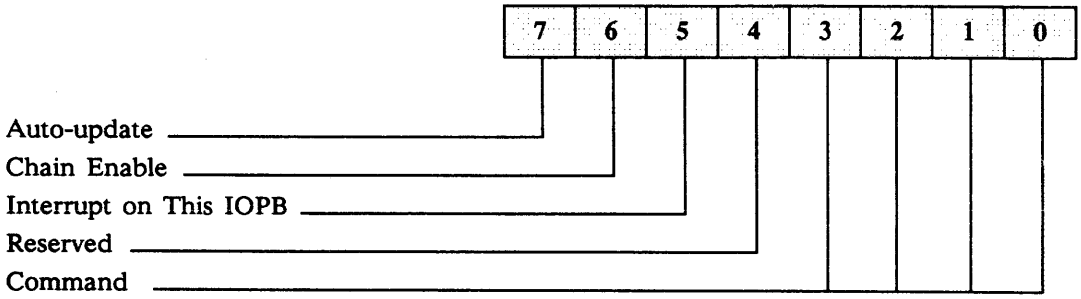
Bit	Mnemonic	Description
7		**Reserved.**
6-5	DT	**Device Type:** Selects the disk or tape drive(s) that connect to the 43x.

Bits 6-5	Drive
00 (0)	Reserved
01 (1)	Winchester
10 (2)	Tape
11 (3)	Floppy

4		**Reserved.**
3	LTC	**Lock Tape Cartridge (Tape Only):** When set, the tape cartridge locks after the 43x selects the drive. When clear, the cartridge does not lock. Only certain drives support the locked cartridge feature. System software must clear LTC for drives that do not support this feature (see your drive manual).
2	RCD	**Removable Cartridge/Disk (Winchester Disks Only):** When set, the 43x selects the removable media of a dual disk drive. When clear, the 43x selects the fixed media of a dual disk drive (see Section 4.16.9). System software must clear RCD for drives that do not support this feature.
1-0	UNIT	**Unit Select:** Selects either one of two Winchester disk drives, one of two floppy disk drives, or the tape drive that connects to the 43x. Winchester and tape drives are commonly numbered from 1 to 4; unit select values are numbered from 0 to 3. Setting the 43x to Unit Select 0 selects Drive 1. Floppy drives are commonly numbered 0 and 1; setting Unit Select 0 selects Drive 0 for a floppy.

Bits 1-0	Tape Unit No.	Winchester Unit No.	Floppy Unit No.
00 (0)	1	1	0
01 (1	2	2	1
10 (2)	3	-	-
11 (3)	4	-	-

3.1.2 Command Byte (IOPB Byte 1)



Bit	Mnemonic	Description
7	AUD	**Auto-update (For Disk):** When set, the 43x updates the current IOPB upon its completion. The Controller Status, Sector, Head, Cylinder, Sector Count, Data Address and Data Relocation bytes reflect the IOPB processing. When clear and no error occurs, the 43x only updates the Status bytes. If an error occurs, the 43x defaults to AUD and performs a full update unless *No Update on Error* (NUE) in the Function Modification byte is set. **Auto-update (For Tape):** When set, the 43x updates the current IOPB upon its completion. The Controller Status, Tape Status 1, Tape Status 2, Block Count, Data Address, and Data Relocation bytes reflect the IOPB processing. When clear and no error occurs, the 43x updates the Controller Status, Tape Status 1, and Tape Status 2 bytes. If an error occurs, the 43x defaults to AUD and performs a full update, unless NUE is set.
6	CHEN	**Chain Enable:** Setting CHEN enables IOPB chain processing. The Next IOPB Address bytes and the Relocation Registers specify the next IOPB address. The 43x starts processing the next chained IOPB if the channel is free; if the 43x encounters a hard error during IOPB processing, it completes the current IOPB, but stops executing the chain. The 43x sets CRDY after executing the last IOPB in the chain (see Section 6.2). When clear, the 43x executes the current IOPB and then sets CRDY.

3.1.2 Command Byte (IOPB Byte 1) (continued)

Bit	Mnemonic	Description
5	ITI	**Interrupt on this IOPB:** the 43x generates an interrupt if ITI is set in the completed IOPB.
4		**Reserved.**
3–0	COM	**Command:** Table 3–4 lists the 43x command codes (see Sections 4 [disk] and 5 [tape] for a detailed explanation of each command). Certain tape commands require a valid subfunction code (see Section 3.1.17.3).

> *Some commands have associated subfunction codes for additional flexibility (see Section 3.1.17.1 for Winchester, 3.1.17.2 for floppy, and 3.1.17.3 for tape).*

Table 3–4. Command Codes

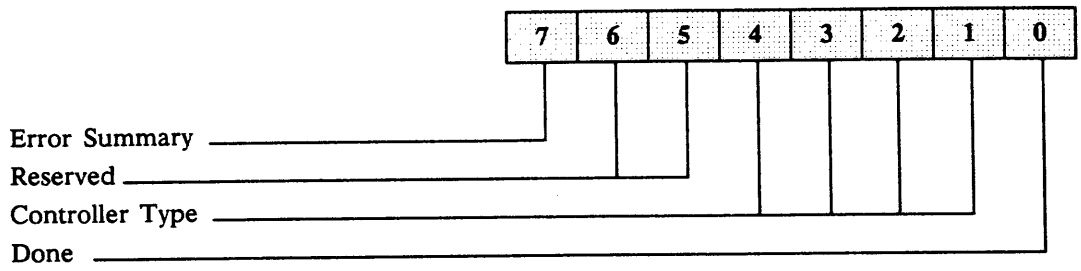
Code(H)	Command	Disk	Tape	Floppy
00	No Operation (NOP)	Yes	Yes	Yes
01	Write Data	Yes	Yes	Yes
02	Read Data	Yes	Yes	Yes
03	Write Track Header	Yes	No	No
04	Read Track Header	Yes	No	No
05	See/Position	Yes	Yes	Yes
06	Drive Reset	Yes	Yes	Yes
07	Write Format/File Mark	Yes	Yes	Yes
08	Read Drive Status	Yes	Yes	Yes
09	Set Drive Parameters	Yes	No	Yes
0A	Self Test	Yes	Yes	Yes
0B	Maintenance	Yes	No	Yes
0C	Send Serial (432 Only)	Yes	No	No
0D	Read Defect Map (432 Only)	Yes	No	No
0E–0F	Reserved			

3.1.3 Next IOPB Address (IOPB Bytes 2 and 3)

IOPB Byte 2 is Next IOPB Low (NIOPBL); Byte 3 is Next IOPB High (NIOPBH). These two bytes comprise the 16-bit Next IOPB Address, similar to the IOPB Address Register.

To implement command-chaining, system software must set CHEN in IOPB Byte 1, and specify the starting address of the next IOPB in Bytes 2 and 3. The 43x combines the Next IOPB bytes with the IOPB Relocation Registers to determine the next IOPB address (see Sections 2.2.1 and 2.2.2). They are the links in the IOPB chain. The 43x ignores NIOPBL and NIOPBH if CHEN is clear.

3.1.4 Controller Status Byte 0 (IOPB Byte 4)



Bit	Mnemonic	Description
7	ERSM	**Error Summary:** When set and the IOPB is complete, a hard error occurred in the CSTAT1, TSTAT0, or TSTAT1 bytes (see Section 6.3). The 43x sets ERSM for any tape error.
6–5		**Reserved.**
4–1	CTYP	**Controller Type:** Xylogics assigns each controller a unique controller type code as follows: Code 5 = 431 and Code 6 = 432.
0	DONE	**Done:** The 43x sets *Done* after completing and releasing the IOPB. More status is available in CSTAT1 and/or TSTAT0 and TSTAT1 for tape drives. System software must clear *Done* before passing an IOPB to the controller. The 43x will not execute the IOPB if *Done* is set.

3.1.5 Controller Status Byte 1

Controller Status Byte 1 (CSTAT1) contains the completion code for each IOPB. CSTAT1 is not valid until the 43x sets *Done*. CSTAT1 contains the previous memory contents for an incomplete IOPB. System software should clear CSTAT1. A code of 0x indicates a successful completion; any other value indicates an error occurred (see Section 6.3).

3.1.6 IOPB Byte 6 (Multifunction)

This byte has three definitions, based on the device type and the selected command.

For disk, IOPB Byte 6 is:

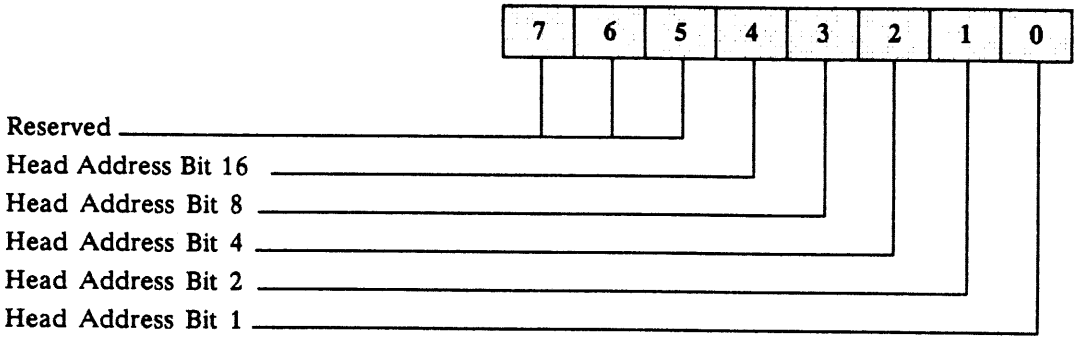
- Head Address (HEAD) for Read and Write operations.
- Drive Option for Read Drive Status and Set Drive Parameters commands (see Section 4.16.2).

For tape, IOPB Byte 6 is:

- QIC-02 Tape Status Byte 0 (TSTAT0) for all tape commands.

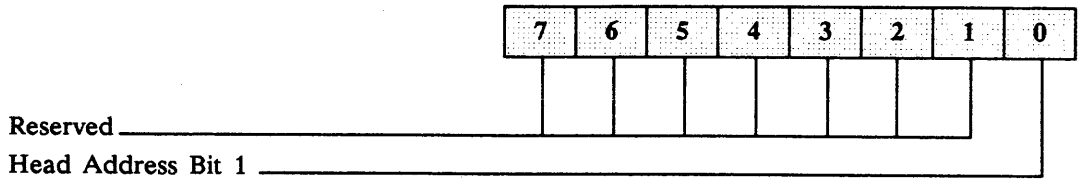
3.1.6.1 Winchester Disk Head Address (IOPB Byte 6)

The Head Address byte specifies the starting head number for a disk transfer. Head numbers start with Head 0. Attempting to access a head number larger than max head causes an *illegal head* error. The 43x handles up to 32 heads, numbered 0 through 31.



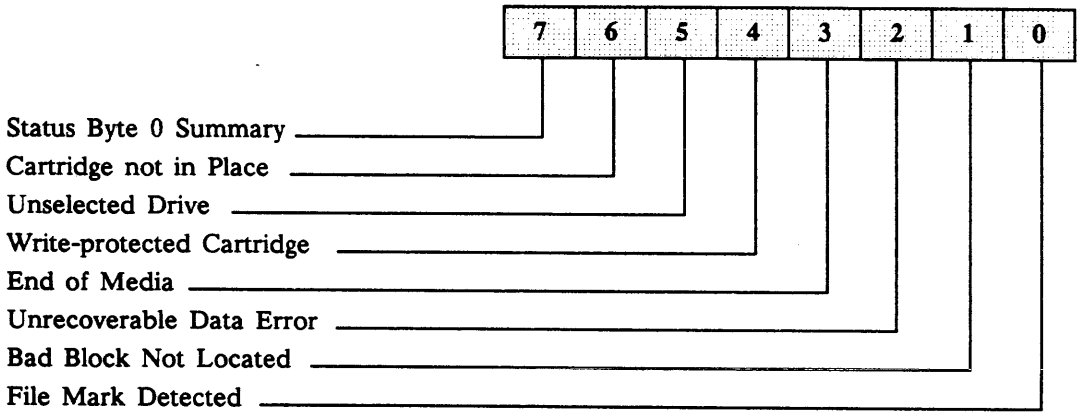
3.1.6.2 Floppy Disk Head Address (IOPB Byte 6)

The Head Address byte specifies the starting head number for a disk transfer. A floppy disk has a maximum of two heads, numbered 0 and 1.



3.1.6.3 Tape Status Byte 0 (IOPB Byte 6)

This byte displays QIC-02 Status Summary Byte 0. The 43x returns Tape Status Byte 0 for all tape commands.



Bit	Mnemonic	Description
7	ST0	**Status Byte 0 Summary:** ST0 sets when any other bit in this byte sets.
6	CNI	**Cartridge not in Place:** The drive sets CNI when the cartridge is not fully inserted into the selected tape drive and a BOT, Initialize, Erase, Write, Write File Mark, Read or Read File Mark command is issued. CNI also sets when the cartridge is removed while the drive is selected. Correcting this condition clears CNI.

3.1.6.3 Tape Status Byte 0 (IOPB Byte 6) (continued)

Bit	Mnemonic	Description
5	USL	**Unselected Drive:** The QIC-02 formatter sets USL if the selected drive is not connected to the interface or is not receiving power when a BOT, Initialize, Erase, Write, Write File Mark, Read or Read File Mark command is issued. Software must correct the condition to clear USL.
4	WRP	**Write-protected Cartridge:** The drive sets WRP when the cartridge in the selected drive has the write-protect in the *safe* position and an Erase, Write, or Write File Mark command is issued. Clear WRP by turning off the write-protect.
3	EOM	**End of Media:** The drive sets EOM when it detects the logical early warning hole of the last track during a Read or Write operation. EOM remains set as long as the drive is past the logical end of media. Some tape drives permit reading and writing beyond EOM.
2	UDA	**Unrecoverable Data Error:** The drive sets UDA if a hard error occurs during a Read or Write operation. Due to limitations in the QIC-02 interface, the 43x cannot determine the location of the error. System software should retry the operation.
1	BNL	**Bad Block Not Located:** The drive sets BNL if a hard error occurs during a Read or Write operation. The 43x can detect this error but cannot confirm that the error is in the last block transferred from the drive. Due to limitations in the QIC-02 interface, the 43x cannot determine the location of the error. Software should retry the operation.
0	FIL	**File Mark Detected:** The drive sets FIL when it detects a file mark during a Read or Read File Mark command. FIL clears without intervention.

3.1.7 IOPB Byte 7 (Multifunction)

This byte has four definitions, based on the device type and the selected command.

For disk, IOPB Byte 7 is:

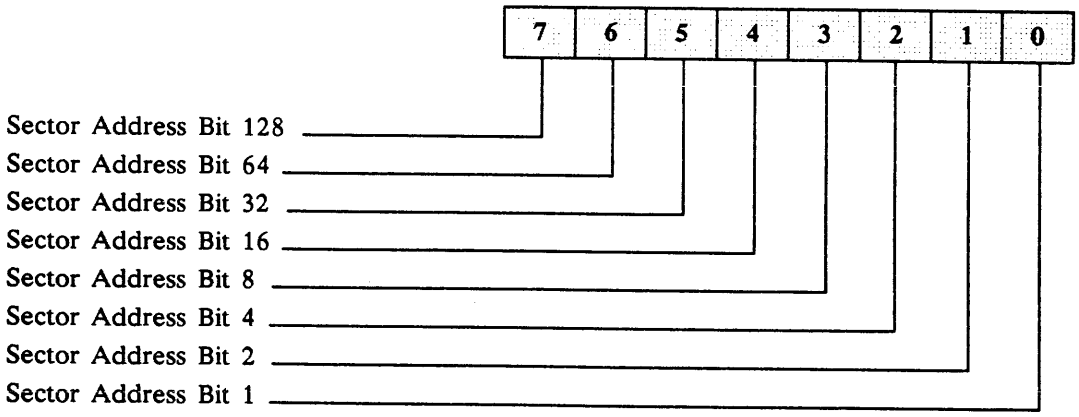
- Sector Address (SECT) for Read and Write operations.
- Max Sectors for Set Drive Parameters and Read Drive Status commands (see Sections 4.15.2 and 4.16.3).
- Count Sectors for a Maintenance command (Winchester only; see Section 4.18.2.1, Code 3).

For tape, IOPB Byte 7 is:

- QIC-02 Tape Status Byte 1 (TSTAT1) for all tape commands.

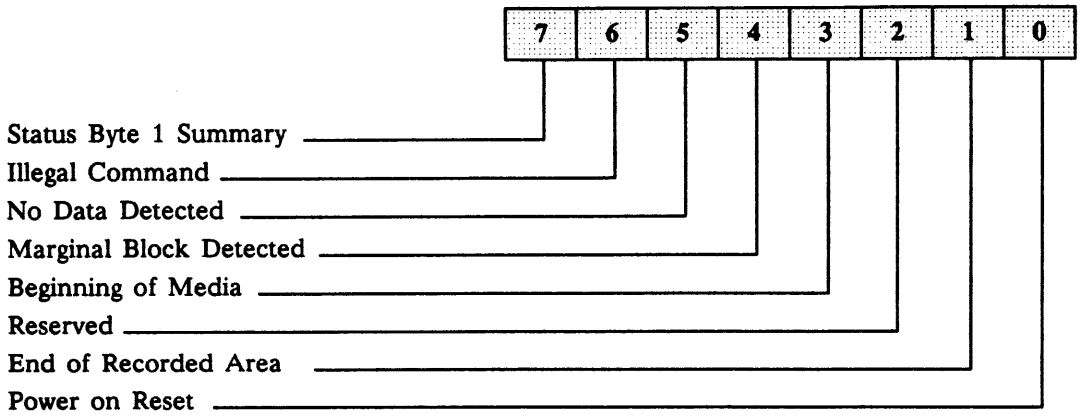
3.1.7.1 Disk Sector Address (IOPB Byte 7)

The Sector Address byte specifies the starting sector number for a disk transfer. All commands that read or write the disk use the sector number, except Format and Read/Write Track Headers. Winchester disk sectors are numbered from 0 to *n*-1, where *n* is the number of sectors per track. Floppy disk sectors are numbered from 1 to *n*, where *n* is the number of sectors per track (see Section 4.15.2).



3.1.7.2 Tape Status Byte 1 (IOPB Byte 7)

This byte displays QIC-02 Status Byte 1. The 43x returns Tape Status Byte 1 for all tape commands.



Bit	Mnemonic	Description
7	ST1	**Status Byte 1 Summary:** ST1 sets when any other bit in this byte sets.
6	ILL	**Illegal Command:** The drive sets ILL if system software issues an illegal subfunction code. The command may be illegal due to a *sequence/ protocol* error, or may not be supported by the drive. The drive manual lists the commands that your drive supports.
5	NDT	**No Data Detected:** The drive sets NDT when a hard data error occurs due to a lack of recorded data.
4	MBD	**Marginal Block Detected:** The drive sets MBD if it detects a marginal data block.
3	BOM	**Beginning of Media:** The drive sets BOM when the tape is at the logical beginning of the tape; Track 0. The drive clears BOM when the tape moves away from the beginning of the tape. A Drive Reset clears BOM, regardless of its location (see Section 5.5).
2		**Reserved.**
1	EOR	**End of Recorded Area:** The 43x sets EOR during a Read Data, Read File Mark, or Seek End of Data command if 45 inches of erased tape follows a valid file mark.
0	POR	**Power on Reset:** Sets on power-up or after a tape Drive Reset.

3.1.8 IOPB Byte 8 (Multifunction)

This byte has three definitions, based on the device type and the selected command.

For disk, IOPB Byte 8 is:

- Cylinder Address (floppy) and Cylinder Address Low (Winchester) for any type of Read, Write, Format, and Seek operations.
- Max Cylinder (floppy) and Max Cylinder Low (Winchester) for Set Drive Parameters and Read Drive Status commands (see Sections 4.15.3 and 4.16.4).

For tape, IOPB Byte 8 is:

- QIC-02 Tape Status Byte 2 (TSTAT2) for a Read Drive Status command (see Section 5.7.2).

3.1.8.1 Disk Cylinder Address Low (IOPB Byte 8)

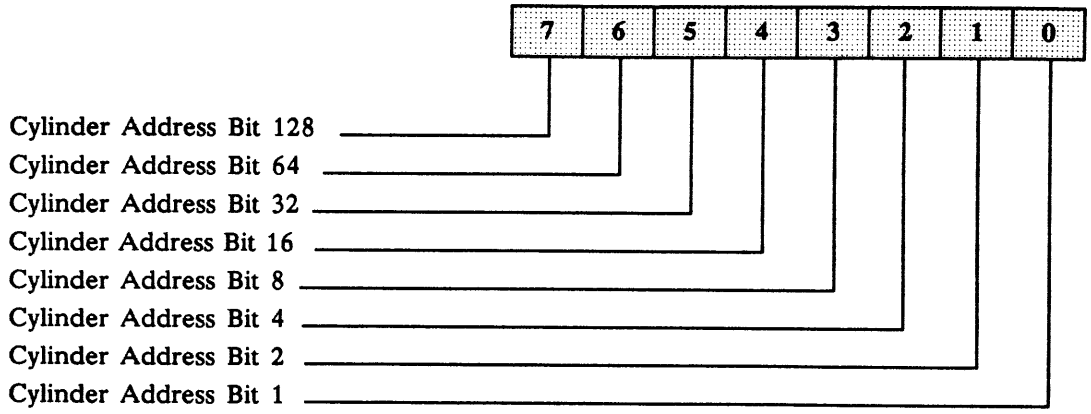
IOPB Byte 8 specifies the Cylinder Address Low (CYLL); it is the least significant portion of the cylinder address for Winchester disks. IOPB Byte 9 (CYLH) is the most significant portion. Byte 8 contains the full cylinder address for floppy disks (80 tracks).

System software must specify the cylinder address for all operations that move data on or off the disk. The cylinder address for Winchester disks is a 12-bit binary number; for floppy disks it is a 7-bit number. The lowest cylinder address is zero; the largest cylinder address is the number of cylinders on the drive, minus 1. The maximum cylinder number that the 43x supports for Winchester disks is 4095; the max cylinder for floppy disks is 127.

During format, the 43x writes the cylinder address into each sector header on the disk. During Read Data and Write Data operations, the 43x reads the cylinder address and compares it to the IOPB cylinder address. A *cylinder head/header* error occurs if the cylinder and/or head address in the sector header does not match the cylinder and/or head address in the IOPB.

A *cylinder address* error occurs if the cylinder address in the IOPB is larger than the max cylinder number specified in the last Set Drive Parameters command.

3.1.8.1 Disk Cylinder Address Low (IOPB Byte 8) (continued)



3.1.9 IOPB Byte 9 (Multifunction)

This byte has three definitions, based on the device type and the selected command. *Floppy disks do not use IOPB Byte 9.*

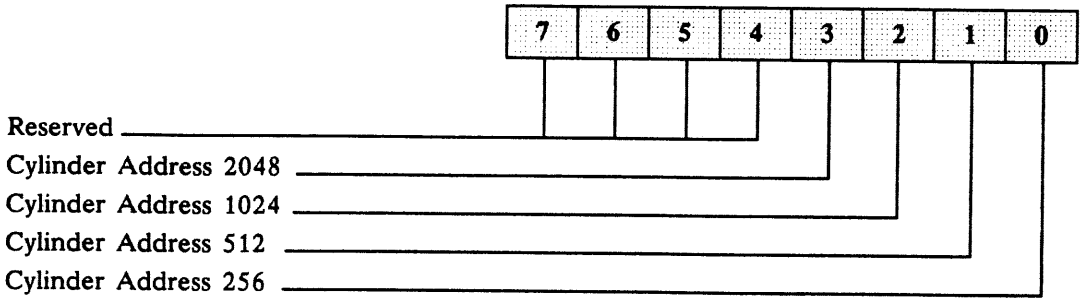
For Winchester disks, IOPB Byte 9 is:

- Cylinder Address (CYLH) for any Read, Write, Format, and Seek operations.
- Max Cylinder High for Set Drive Parameters and Read Drive Status commands (see Sections 4.15.2 and 4.16.3).

For tape, IOPB Byte 9 is:

- QIC-02 Tape Status Byte 3 (TSTAT3) for a Read Drive Status command (see Section 5.7.2).

3.1.9.1 Winchester Disk Cylinder Address High (IOPB Byte 9)



3.1.10 IOPB Byte A (Multifunction)

This byte has five definitions, based on the device type and the selected command.

For disk, IOPB Byte A is:

- Sector Count Low (CNTL) for Read and Write operations.
- Track Count Low for a Format command (see Section 4.14.4).
- Drive Status for a Read Drive Status command (see Section 4.15.4).

For tape, IOPB Byte A is:

- Block Count Low (CNTL) for Read and Write operations.
- QIC-02 Tape Status Byte 4 (TSTAT4) for a Read Drive Status command (see Section 5.7.3).

3.1.10.1 Disk Sector Count Low (IOPB Byte A)

The 43x transfers information in whole sectors. The sector count, a 16-bit number stored as two bytes in the IOPB, is the number of sectors to be transferred. IOPB Byte A (CNTL) is the least significant half of the sector count; Byte B (CNTH) is the most significant half. A 16-bit sector count allows a continuous transfer of 65,535 sectors with one command.

3.1.10.2 Tape Block Count Low (IOPB Byte A)

The block count, a 16-bit number stored as two bytes in the IOPB, is the number of blocks to be transferred or spaced. IOPB Byte A (CNTL) is the least significant half of the block count; Byte B (CNTH) is the most significant half. For Read and Write commands, the desired record length is specified in blocks; the range is from 1 to 65,535. Each block is 512-bytes long.

The 43x aborts Read and Position commands if it detects a file mark before reading all of the requested data blocks; it posts the number of blocks it did not read in the Block Count bytes.

During spacing commands, if supported by the drive, the 43x posts the number of blocks it did not space over in the Block Count bytes.

3.1.11 IOPB Byte B (Multifunction)

This byte has five definitions, based on the device type and the selected command.

For disk, IOPB Byte B is:

- Sector Count High (CNTH) for Read and Write operations.
- Track Count High for a Format command (see Section 4.14.4).
- Firmware Revision Code for a Read Drive Status command (see Section 4.15.5).

For tape, IOPB Byte B is:

- Block Count High (CNTH) for Data Transfer commands.
- QIC-02 Tape Status Byte 5 (TSTAT5) for a Read Drive Status command (see Section 5.7.3).

3.1.11.1 Disk Sector Count High (IOPB Byte B)

The 43x transfers information in whole sectors. The sector count, a 16-bit number stored as two bytes in the IOPB, is the number of sectors to be transferred. IOPB Byte A (CNTL) is the number of sectors to be transferred; Byte B (CNTH) is the most significant half. Error 50H occurs if the sector count causes a transfer of 8 MB or more to the floppy disk.

3.1.11.2 Tape Block Count High (IOPB Byte B)

The block count, a 16-bit number stored as two bytes in the IOPB, is the number of blocks to be transferred. IOPB Byte A (CNTL) is the least significant half of the block count; Byte B (CNTH) is the most significant half.

3.1.12 Data Address Low (IOPB Byte C) (Multifunction)

For Winchester and floppy disks, IOPB Byte C (DATAL) is:

- Data Address Low, subject to relocation, for Read and Write operations.

3.1.12 Data Address Low (IOPB Byte C) (Multifunction) (continued)

For Winchester disks, IOPB Byte C is:

- Sector Size Low for a Read Drive Status command; firmware determines the sector size (see Sections 4.15.6 and 8.2.1).

For floppy disks, IOPB Byte C is:

- The data field fill character for a Format (00-F4) command (see Section 4.14.2).

For tape, IOPB Byte C is:

- Data Address low, subject to relocation, for all tape commands.

3.1.13 Data Address High (IOPB Byte D) (Multifunction)

For Winchester and floppy disks, IOPB Byte D (DATAH) is:

- Data Address High, subject to relocation, for Read and Write operations.

For Winchester disks, IOPB Byte D is:

- Sector Size High for a Read Drive Status command (see Sections 4.15.6 and 8.2.1).

For floppy disks, IOPB Byte D is:

- Decoded Bytes Per Sector for Set Drive Parameters and Read Drive Status commands (sector size for a floppy is software programmable; see Sections 4.15.6 and 4.16.5).

For tape, IOPB Byte D is:

- Data Address High, subject to relocation, for all commands.

3.1.14 Data Relocation (IOPB Bytes E and F) (DATAL, DATAH)

The 43x, when configured for 20-bit addressing, forms the DMA starting address by shifting DATAL and DATAH to the left four places and adding the data address.

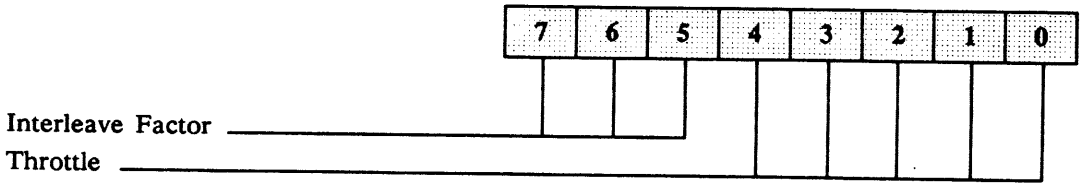
3.1.14 Data Relocation (IOPB Bytes E and F) (continued)

The 43x, when configured for extended addressing, forms the DMA starting address by appending the Data Relocation bytes to the left of the data address. The 43x uses only the lower 24 bits of the physical address (see Section 2.2.2).

Sections 4.15.7 through 4.15.9, and 4.16.6 through 4.16.8 define Bytes E and F for the Read Drive Status and Set Drive Parameters commands.

3.1.15 Throttle (IOPB Byte 10)

The Throttle byte selects the maximum number of DMA cycles in a DMA burst, and the interleave factor for disks.



Bit Mnemonic Description

7-5 INTF **Interleave Factor (Disk Only):** The 43x uses INTF during formatting. In normal 1:1 interleaving, the interleave factor is zero. For other factors, the interleave ratio is $(n+1):1$, where n is the interleave factor.

Table 3-5. Interleave Ratios

Interleave Factor	Interleave Ratio
0	1:1
1	2:1
2	3:1
3	4:1
4	5:1
5	6:1
6	7:1
7	8:1

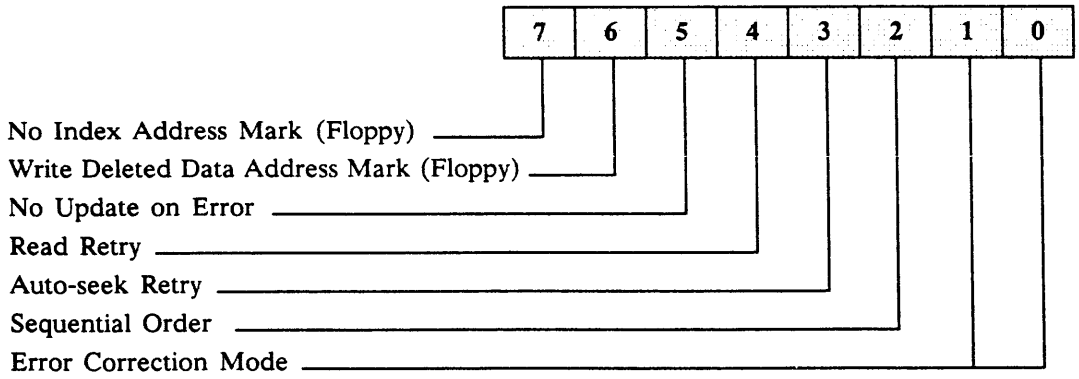
3.1.15 Throttle (IOPB Byte 10) (continued)

4-0 THRO **Throttle:** Selects the maximum number of words/bytes the 43x transfers each time it executes a data transfer. The relationship between the throttle number and the actual throttle (or DMA cycles) is $2n + 2$, where n is the throttle number (see Section 4.3). In byte mode, each DMA cycle transfers one byte; word mode transfers two bytes per DMA cycle.

Table 3-6. Maximum Number of Bytes Transferred per Throttle Burst

Throttle	No. DMA Cycles	Number of Bytes Transferred Word Mode	Byte Mode
0	2	4	2
1	4	8	4
2	6	12	6
3	8	16	8
:	:	:	:
1F	64	128	64

3.1.16 Function Modification (IOPB Byte 11)



Bit Mnemonic Description

7 NIXM **No Index Address Mark (Floppy Disk Only):** When set during a Format command on a floppy disk, the 43x omits the index address field, including the gap, sync, and address mark (see Section 4.14.3).

3.1.16 Function Modification (IOPB Byte 11) (continued)

Bit	Mnemonic	Description
6	WDDM	**Write Deleted Data Address Mark (Floppy Disk Only):** When set during a Write or Write Format command on a floppy disk, the 43x precedes the data field with a deleted data address mark, F8. When clear, the 43x precedes the data field with a data address mark, FB (see Section 4.14.3).
5	NUE	**No Update on Error:** For diagnostic purposes only. If an error occurs while NUE is set, the 43x returns: • For disk, CSTAT0 and CSTAT1. • For tape, CSTAT0, CSTAT1, TSTAT0, and TSTAT1. When clear, the 43x performs a full update on error. Normal operation leaves NUE clear.
4	RTRY	**Read Retry:** When set, the 43x attempts an automatic retry. For Winchester disks, if an ECC error occurs and RTRY and the error correction mode are set, the 43x reads the sector in error one more time to obtain a correct read. If the read fails, the 43x reports an ECC soft error or a hard error. For floppy disks, if the 43x detects a CRC error on a read, it retries the Read operation once. If the error persists, the 43x reports a hard error; if the retry succeeds, the 43x posts completion code 42 (*read retry recovered*) and continues IOPB processing.
3	ASR	**Auto-seek Retry:** If a *cylinder/head* error occurs and ASR is set, the 43x recalibrates the disk drive and retries the seek once before reporting an error.
2	SO	**Sequential Order:** When set, the 43x executes chained IOPBs in sequential order. SO disables implied overlap seeking on Winchester and floppy disks and may affect tape streaming. When clear, the 43x executes mixed tape and disk IOPBs in chained order, regardless of drive type or IOPB order.

3.1.16 Function Modification (IOPB Byte 11) (continued)

Bit	Mnemonic	Description
1-0	ECM	**Error Correction Mode (Winchester Disks Only):**

ECM	Mode	Action
00	0	The 43x provides an ECC pattern and offset, stops a chained transfer, and reports an ECC error. Software must perform the ECC correction.
01	1	The 43x does not correct or flag an error; it continues the IOPB chain.
10	2	The 43x corrects an ECC error, updates the IOPB with the soft error status, and continues the IOPB chain.
11	3	The 43x does not correct an ECC error, but flags it (*ECC ignored* error) and continues the IOPB chain.

3.1.17 Subfunction Code (IOPB Byte 12) (Multifunction)

The subfunction codes (SUBF) further define the manner of command execution (see Section 3.1.2). Each 43x command may have one or more associated subfunctions. Subfunction codes feature:

- Disk diagnostic reads and writes.
- Count sectors per track.
- All standard Rev. D, QIC-02 commands.
- All optional Rev. D, QIC-02 commands.

3.1.17.1 Winchester Disk Subfunction Codes (IOPB Byte 12)

The Maintenance command (Command Code B) enables the following Winchester disk subfunction codes.

Code	Command
0	NOP
1	Write Data and ECC
2	Read Data and ECC
3	Count Sectors per Track
4–255	Reserved

3.1.17.2 Floppy Disk Subfunction Codes (IOPB Byte 12)

The Maintenance command enables the following floppy disk subfunction codes.

Code	Command
0	NOP
1–3	Reserved
4	Read Next Header
5	Read Full Track
6–255	Reserved

3.1.17.3 Tape Subfunction Codes (IOPB Byte 12)

These codes are taken directly from the QIC-02 interface specification. The 43x supports the standard, and certain optional, QIC-02 commands. The 43x uses the subfunction code to pass an optional command to the tape drive; an *illegal command* error occurs if the drive does not support the command.

> *Do not enter the subfunction codes for tape drive selects in the Subfunction byte (SUBF). COM specifies all the necessary controller selects and deselects.*

3.1.17.3 Tape Subfunction Codes (IOPB Byte 12) (continued)

Table 3–7 lists the subfunction codes. System software must set up the IOPB with the appropriate command code in COM for the associated subfunction code in SUBF; it must load a subfunction code into the IOPB for every tape related operation, except Select Drive.

Table 3–7. Tape Command and Subfunction Codes

Command CodeH	Description	Subfunction CodeH	S,O	Description
1	Write Data	40	S	Write
		41	O	Write Without Underruns
2	Read Data	80	S	Read
		84	O	Read, Reduced Track Density (RTD)
		88	O	Read Reverse
		8C	O	Read Reverse, RTD
5	Position	A0	S	Read File Mark
		A8	O	Read File Mark Reverse
		A4	O	Read File Mark, RTD
		AC	O	Read File Mark Reverse, RTD
		B*n*	O	Read *n* File Marks
		21	S	Position to BOT
		22	S	Erase Entire Tape
		24	S	Initialize Cartridge
		25	O	Select Auto-cartridge Initialization
		81	O	Space Forward
		85	O	Space Forward, RTD
		89	O	Space Reverse
		8D	O	Space Reverse, RTD
		A3	O	Seek End of Data (EOD)
		A7	O	Seek EOD, RTD
6	Drive Reset	00	-	Null
7	Write File Mark	60	S	Write File Mark
		7*n*	O	Write *n* file Marks
8	Rd. Drv. Status	C0	S	Read Status
9	Set Drive Status	48	O	Enter 6-byte Parameter Block

S = Standard; O = Optional QIC-02, Rev. D, Command

3.1.17.4 Hardware Self Test Subfunction Codes (IOPB Byte 12)

The Self Test command (Command Code A) enables the following subfunction codes.

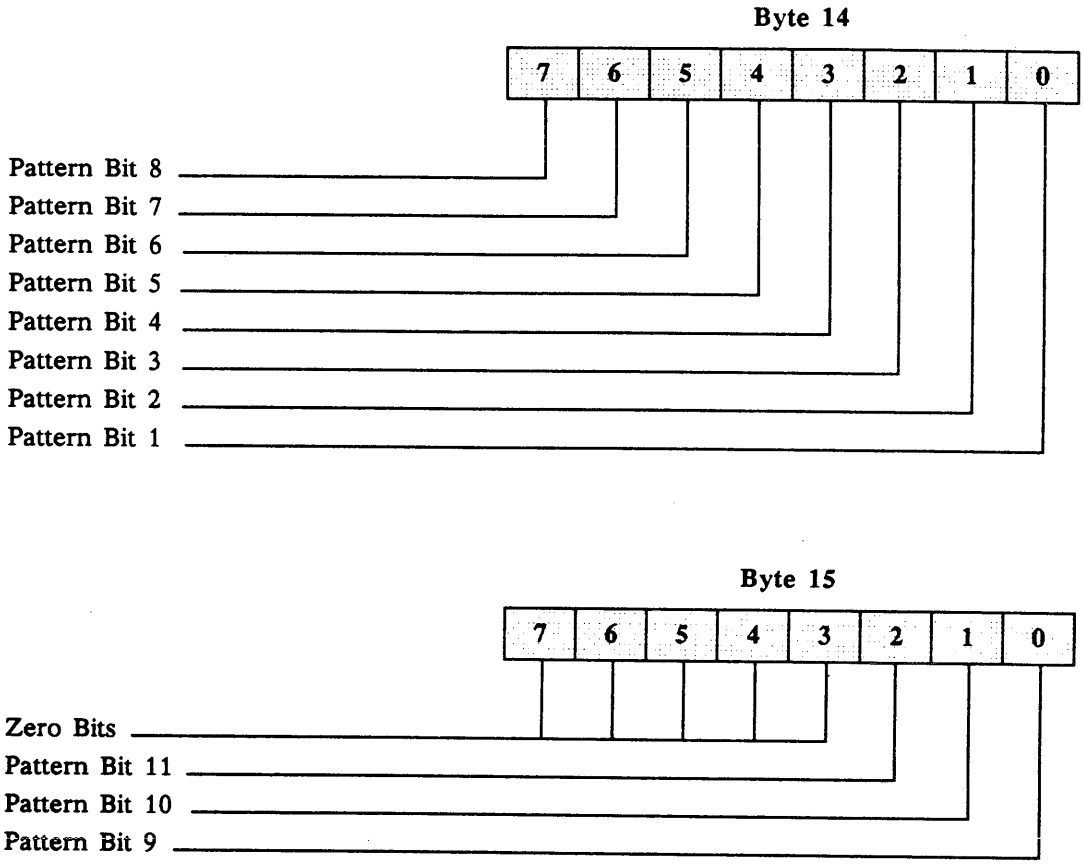
Code	Description
0	Executes the self test (Tests 1 through 5).
1	Executes the self test plus round robin DMA (Tests 1 through 6).
2	Writes the on-board RAM in the DFE.
3	Reads the on-board RAM in the DRE.
4	Loads the DFE with a Read-Data-ECC command; DMA to system memory.
5	Loads the DFE with a Write-Data-ECC command; DEM to system memory.
6	Loads the DFE with a Format command; DMA to system memory.
7	Loads the DFE with a Read Track Headers command; DMA to system memory.
8	Loads the DFE with a Write Track Headers command; DMA to system memory.

Subfunction Codes 1 through 8 are for Xylogics' test purposes only. Using these codes may corrupt parameters that are stored in the Disk Front End (DFE) chip's internal RAM.

3.1.18 Winchester Disk ECC Pattern Word (IOPB Bytes 14 and 15)

The 43x calculates the 16-bit ECC pattern word when a soft ECC error occurs. Eleven of the bits are active; the top five bits are always zero. The 43x stores this word in the ECC Pattern Word Low (least significant) and High (most significant) bytes. The 43x corrects a soft ECC error by exclusive-ORing the ECC pattern word with the bytes pointed to by the ECC Address word. These bytes are only valid in ECC Mode 0; they are indeterminate in other ECC modes.

3.1.18 Winchester Disk ECC Pattern Word (IOPB Bytes 14 and 15) (continued)



3.1.19 Winchester Disk ECC Address Word (IOPB Bytes 16 and 17)

The 43x calculates an ECC address word when a soft ECC error occurs. Two bytes comprise the ECC address word. The ECC Address Word Low byte (ECCAL) is the least significant half of the address word; the ECC Address Word High byte (ECCAH) is the most significant half. The ECC address word points to the bit, within a sector, where the data in error starts. The 43x corrects the error by exclusive-ORing the ECC mask with this bit string. These bytes are only valid in ECC mode 0. They are indeterminate in any other mode.

Section 4: Disk Commands

Section 4: Disk Commands

4.0 Introduction

An IOPB diagram follows each command description. The diagrams indicate which bytes the 43x requires for command execution, and which bytes it returns after execution. *Unless otherwise stated, the word* **disk** *refers to both Winchester and floppy drives.*

The four least significant bits of the Command byte are the *Command Code* bits. These four bits allow up to sixteen possible commands, four of which are reserved. The 43x commands comprise a 24-byte long IOPB.

4.1 Implied Seeks

The 43x issues an implied seek with every data transfer command. The implied seek feature eliminates issuing a separate seek before issuing a command, thus saving program overhead. The 43x issues the implied seek as the first operation after reading the IOPB.

4.1.1 Winchester Disk Drives

If CHEN is set, the drive supports buffered seeks (ST506/412) or serial addressing (ESDI), and overlap seeking is enabled (see Section 4.16.2). The 43x scans the remaining IOPBs and issues seeks to drives that are not busy.

> *The 431's support for overlap seeking is drive-dependent. To support this feature, the drive must allow deasserting the Direction line after the controller generates the last step pulse. Setting the Sequential Order (SO) bit disables overlap seeking; however, the 431 still issues implied seeks.*

4.1.2 Floppy Disk Drives

Floppy disks do not support overlap seeking due to their use of the slower stepper motors for the head access mechanism.

4.2 Seek Completion

4.2.1 Winchester Disk Drives

Write, Write Track Headers, Write Data and ECC commands: after a drive completes its implied seek, the 43x starts the data transfer part of the command, and starts filling the FIFO buffer. After the buffer receives at least one sector of data, the 43x looks for sector coincidence. This process ensures that enough data is available in the buffer when the Write operation begins.

Read, Read Track Headers, Read Data and ECC commands: after a drive completes its implied seek, the 43x accesses the proper head and sector and looks for sector coincidence. When the 43x finds the desired sector, it transfers the data from the Winchester disk to the FIFO buffer; as it transfers data from the Winchester disk to the FIFO, the 43x DMAs data from the FIFO to system memory.

If overlap seeking is enabled, the 43x polls the drives and determines if any seeks are complete. The 43x services the drive that completes its seek first. The 43x may not complete the IOPBs in sequential order.

4.2.2 Floppy Disk Drives

Write and Write Format commands: when a drive completes its implied seek, the 43x determines the proper head and sector, and starts filling the fixed buffer (128 bytes). After the 43x fills the fixed buffer, it looks for sector coincidence and fills the 128-byte floppy disk (FD) FIFO buffer. This process ensures enough that data is available in the FD FIFO and fixed buffers when a Write operation begins.

Read and Read Full Track commands: when a drive completes its seek, the 43x accesses the IOPB, determines the head and sector, and looks for sector coincidence. When the 43x finds the desired sector, it transfers data to the FD FIFO buffer, preparing for transfer to the fixed buffer, and then transfers it to memory. When the 43x fills the fixed buffer, or completes the transfer, it DMAs data from the fixed buffer to system memory.

4.3 Sector Coincidence

The 43x selects the proper drive head, reads each sector header, and compares it to the requested disk address. The 43x begins the data transfer when it finds a match. If the cylinder and head are correct, but the 43x cannot find a sector match, it reports a *header* error. For Winchester disks, the 43x searches for one revolution plus five sectors; for floppy disks, it searches for five revolutions.

4.4 Throttle

The throttle is the maximum number of transfers allowed each time the 43x becomes bus master. All DMA bursts are at the programmed throttle value. During a Write transfer the buffer must be full before the 43x transfers data to the drive. During a Read transfer the 43x transfers the next sector/block into its on-board buffer and then DMAs that data to system memory. The 43x transfers data until the sector/block count goes to zero. If system software specifies a large throttle value, the 43x may not release the bus in 12 microseconds (μs). If you require the 43x to release the bus within 12 μs, software must keep the throttle value within that window (system-dependent).

4.5 Incrementing the Disk Address

4.5.1 Winchester Disk Drives

The 43x increments the sector address by one after writing or reading each sector. If the sector address is greater than max sector, the 43x clears it to zero and increments the head address. If the resulting head address is greater than max head, the 43x clears it to zero and increments the cylinder address. The 43x reports an error if the cylinder address is greater than max cylinder.

4.5.2 Floppy Disk Drives

The 43x increments the sector address by one after writing or reading each sector. If the sector address is greater than max sector, the value of the multitrack (MT) option flag (bit 4 in IOPB Byte 6), set in the last Set Drive Parameters command, determines the next step (see Section 4.16.2). If MT=0, the 43x sets the sector address to one and increments the cylinder address. If MT=1, the 43x sets the sector address to one and increments the head address. If the head address is greater than max head, the 43x clears it to zero and increments the cylinder address. The 43x reports an error if the cylinder address is greater than max cylinder.

4.6 Completing a Disk Transfer

The 43x decrements the sector count by one as it transfers each sector. At the end of the sector, the 43x tests this count and determines if the transfer is complete. If the count is not zero, the 43x transfers the next sector. The 43x issues a seek each time it increments the cylinder address.

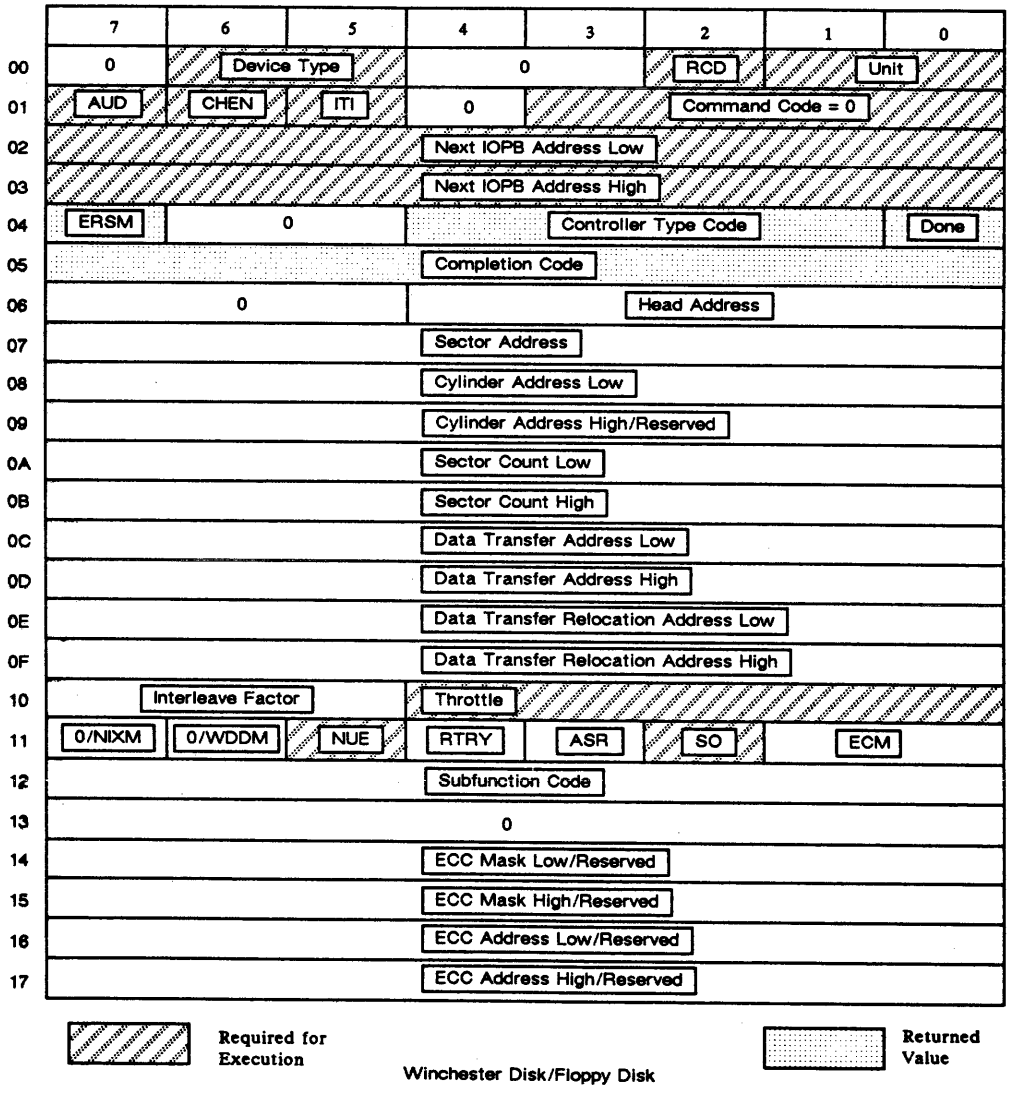
The 43x updates the two IOPB Controller Status bytes after completing the transfer, and generates an interrupt, if enabled. The 43x also updates the Sector, Head, Cylinder, Sector Count, Data Address and Data Relocation bytes if AUD is set in COM.

If a hard error occurs, the 43x stops the transfer. It updates the entire IOPB, regardless of AUD's setting, and generates an interrupt, if enabled. If NUE is set, it overrides *Update On Error*. The 43x halts any chained operations, sets ERR and ERSM, and posts a completion code.

If the 43x completes the transfer with a soft error, it updates the two IOPB Status bytes, and generates an interrupt, if enabled. Any chained operations continue. The 43x updates the faulty IOPB if AUD is set, and sets ERSM; it does not set ERR.

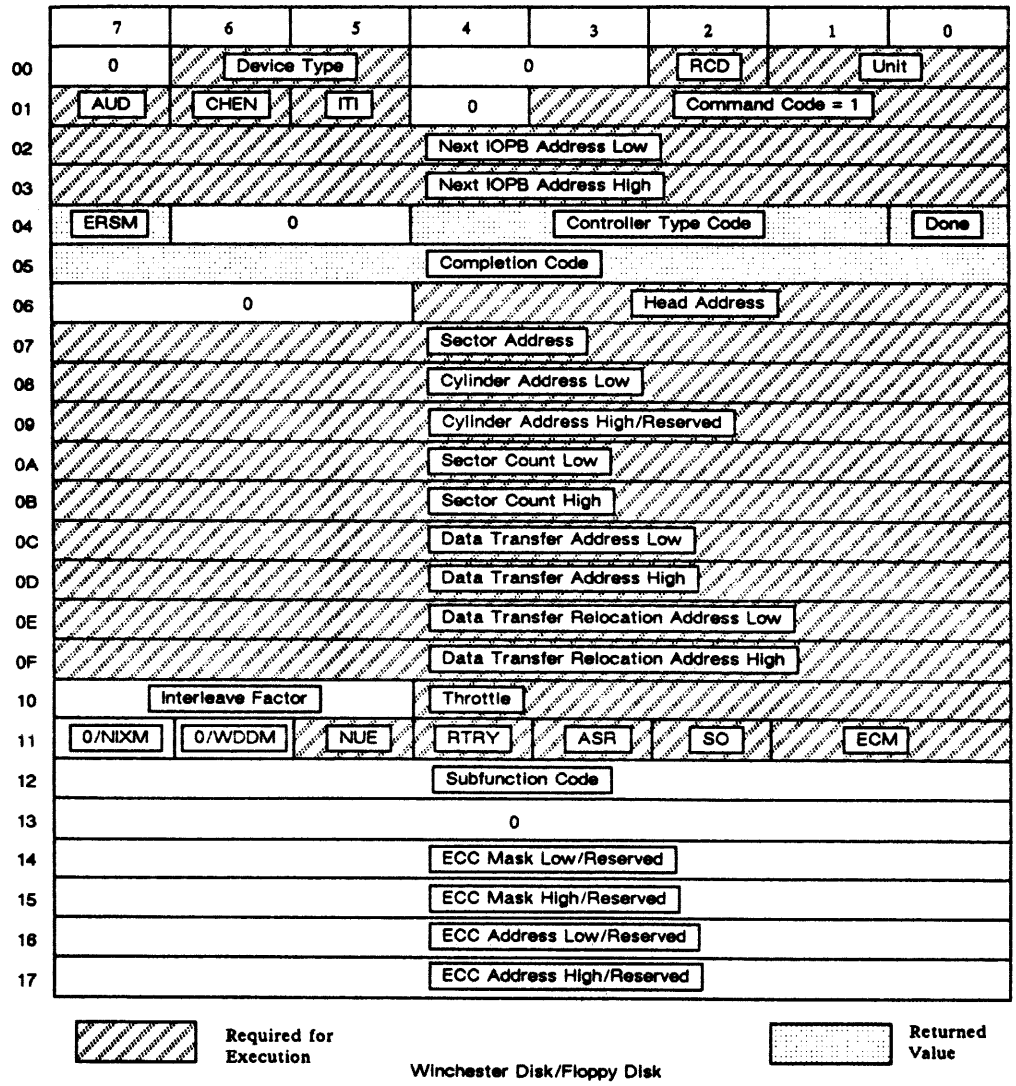
4.7 No Operation (NOP; Command Code 0)

The NOP command verifies that the 43x is operational. The 43x reads the IOPB from system memory, sets *Done*, and posts a completion code in Controller Status Bytes 0 and 1.



4.8 Write Data (Command Code 1)

The Write command transfers data to the disk. This command begins at the disk and memory addresses specified in the IOPB, and transfers the requested sectors. The 43x crosses cylinder, head, and sector boundaries as required.



4.8.1 Writing Data

After the 43x finds a valid header, it skips over the splice area and writes the data preamble and Data Sync byte. It then takes words out of the FIFO buffer, serializes them, and writes them to the disk. The 43x DMAs additional data from host memory as it removes data from the FIFO.

As the 43x transfers data to the Winchester disk, it computes a 32-bit ECC value and appends it, as four bytes, to the data field of each sector.

As the 43x transfers data to the floppy disk, it computes a 16-bit CRC value and appends it, as two bytes, to the data field of each sector.

4.8.2 Write-protect

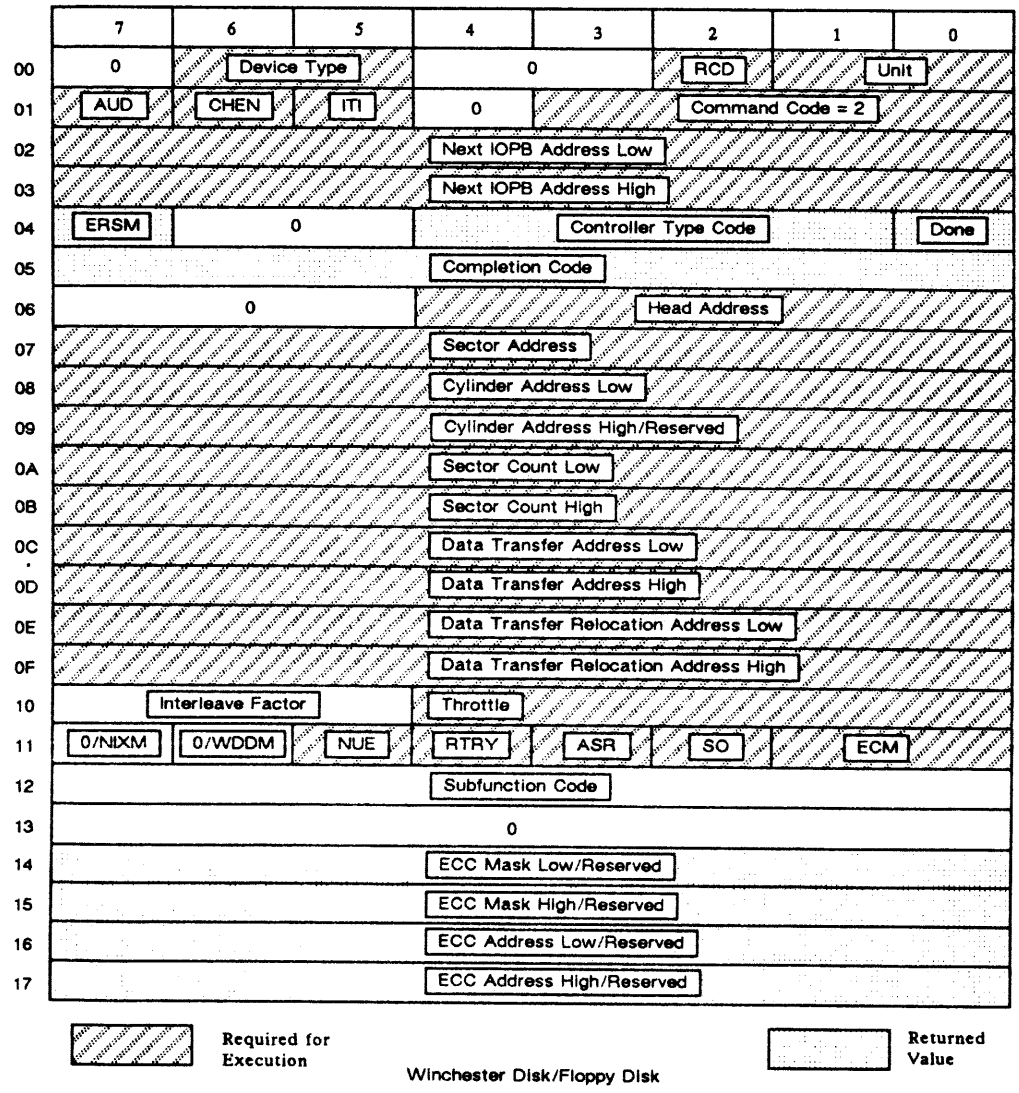
ST506/412 drives have no write-protect signal. On non-ST506/412 drives, the 43x checks the drive's *write-protect* status before attempting a Write operation. If the drive is write-protected, the 43x aborts the command, sets ERR, ERSM, and WPRT.

4.8.3 Deleted Data Address Mark (Floppy Disk Only)

The 43x writes a deleted data address mark at the front of each data field in a sector if WDDM is set. If WDDM is clear, the 43x writes a normal data address mark.

4.9 Read Data (Command Code 2)

The Read command transfers data from the disk to system memory, starting at the disk and memory addresses specified in the IOPB. The transfer crosses sector, head, and cylinder boundaries as required.



4.9.1 Reading Data

4.9.1.1 Winchester Disk Drives

After finding a valid header, the 43x waits for the Data Sync bits. The 43x deserializes the data as it reads it from the Winchester disk, and places it into the FIFO buffer. When data becomes available at the other end of the FIFO, the 43x requests the bus and DMAs the data to memory.

4.9.1.2 Floppy Disk Drives

After the 43x finds a valid header, it waits for the data field address mark. The 43x reads data from the floppy disk, deserializes it, and places it into the FD FIFO buffer. When data becomes available at the other end of the FIFO, the 43x pulls it into the fixed 512-byte buffer. After the 43x fills the fixed buffer, it requests the bus and empties the buffer in a series of DMA transfers to memory.

4.9.2 Winchester Disk ECC During a Transfer

After the 43x reads the data field of a sector, it compares the newly calculated ECC value to the ECC value written on the Winchester disk during the original Write operation.

4.9.3 Floppy Disk Cyclical Redundancy Check (CRC) During a Transfer

After the 43x reads the data field of a sector, it compares the newly calculated CRC value to the CRC written on the floppy disk during the original Write operation. The data is valid if the CRC values match. The 43x reports an error if the CRCs do not match. After the 43x updates the IOPB the floppy disk address points to the sector plus one containing the error. The data and relocation addresses point to the first byte following the sector in error, and the sector count equals the number of remaining sectors.

The 43x returns this information in the IOPB as long as NUE is clear. The 43x identifies the bad sector and its related address in memory. Restarting the IOPB continues the transfer after a soft error.

4.9.4 Winchester Disk Drives and ECC Errors

4.9.4.1 Read Command Encounters an ECC Error in ECC Mode 0

The 43x stops reading when the ECC value calculated from a Read operation does not match the ECC value written on the Winchester disk. The 43x writes all the data for that sector to memory. Through a shifting and counting process, the 43x determines the location and pattern of the error. The 43x considers an error burst hard if it is larger than 11 bits and posts the completion code 14 in CSTAT1.

The 43x considers any error burst of 11 bits or less as soft; it writes the ECC pattern and address words to the IOPB, and posts the completion code 1A. System software must correct the error.

When the 43x encounters an ECC error, its internal registers reflect the following state: the Winchester disk address points to the sector, plus one, containing the error, the data and relocation addresses point to the first byte following the sector in error, and the sector count equals the number of remaining sectors in the transfer.

The 43x returns this information in the IOPB as long as NUE is clear. The controller identifies the bad sector and its related address in memory. Restarting the IOPB continues the transfer after an error.

4.9.4.2 Read Command Encounters an ECC Error in Mode 1

The 43x ignores ECC errors in Mode 1 and continues a data transfer as if no error occurred. It does not set any error bits, and does not post a completion code.

4.9.4.3 Read Command Encounters an ECC Error in Mode 2

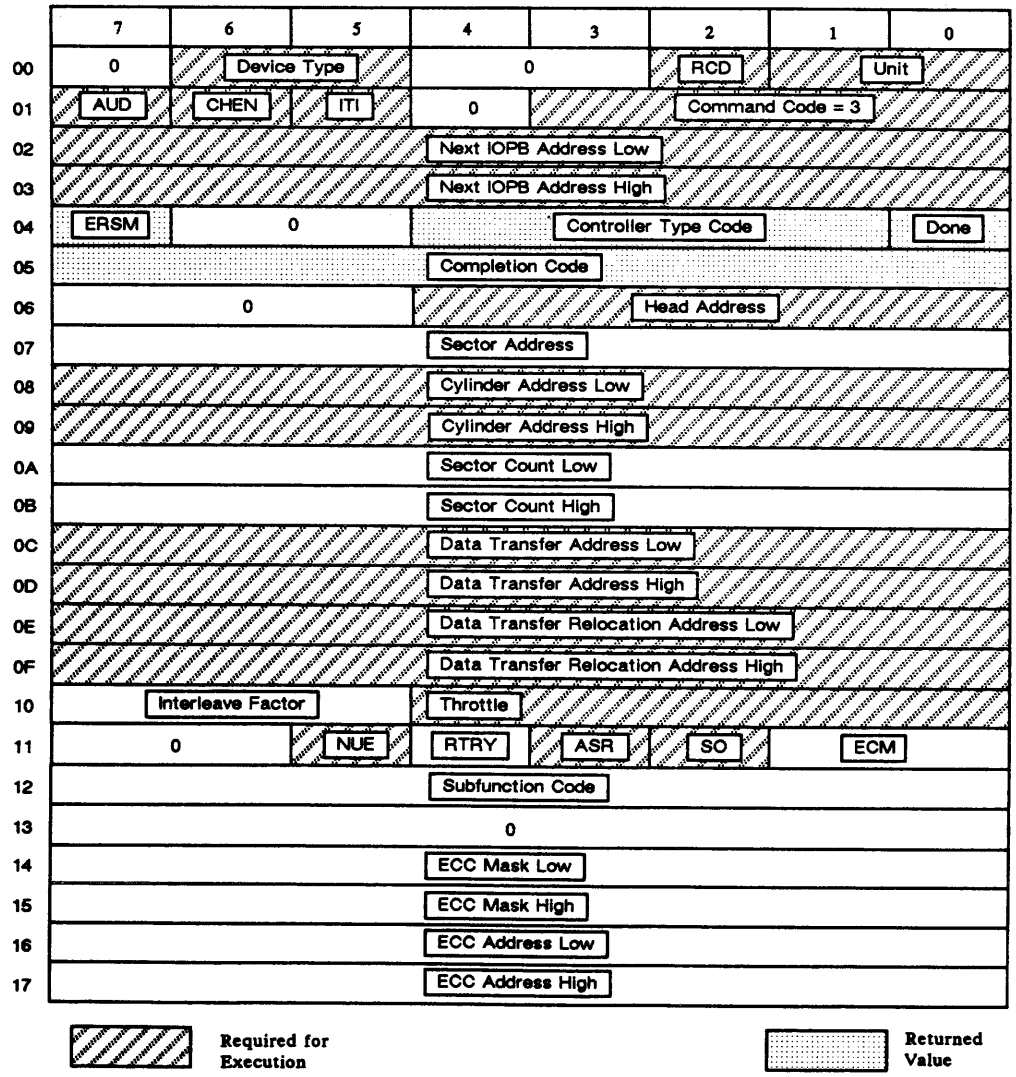
If the 43x encounters a correctable ECC error in Mode 2, it stops the transfer, corrects the data in system memory, and resumes the data transfer on the next revolution of the Winchester disk. The 43x posts the completion code 12 (soft ECC recovered) in CSTAT1, and sets ERSM. IOPB processing continues if CHEN is set.

4.9.4.4 Read Command Encounters an ECC Error in Mode 3

The 43x ignores an ECC error in Mode 3, and continues a data transfer as if no error occurred. When the 43x completes the transfer, it posts the completion code 12 in CSTAT1, indicating it encountered one or more uncorrected soft ECC errors. The 43x does not set ERR on this error, but it does set ERSM.

4.10 Winchester Disk Write Track Headers

The Write Track Headers and Read Track Headers commands enable system software to map out media defects and create any kind of logical sector organization. These commands enable sector slipping so data sectors bypass media defects. Write Track Headers formats a single track with header data from system memory; it also suspends overlap operations. Read Track Headers transfers the header data to system memory. This data is the actual header for each sector on the track starting at index, including bad and spare sectors. Write Track Headers is a form of the Format command and overwrites all data on a track; use it to mark sectors spare or bad (see Section 6.7).



4.10.1 Write Track Headers and Media Defects

During a Read Track Headers command, the 43x will not transfer the header to system memory accurately if the defect area involves the address mark. Do not rely on a Read Track Headers command to set up system memory. Always verify the headers manually. Issue a Write Track Headers command after the headers in the buffer are verified and rearranged for sector slip.

> *Xylogics does not recommend using Read Track Headers for slipping sectors; you may lose a sector if there is a media defect in the address mark area. We recommend building the header table in system memory, modifying the table for the slipped sectors, and using Write Track Headers to write headers back to the disk.*

4.10.2 Data Buffer

Software must construct a data buffer in system memory before issuing a Write Track Headers command. The first four bytes are the header data for physical Sector 0, which is the first sector after index. The next four bytes are for physical Sector 1, etc. The data in the buffer is organized in physical sector order. The data in the sector header indicates the logical sector order. Section 6.5 describes the header format. Table 4–1 shows the buffer format.

Writing four bytes of DDH in the header marks a sector spare; writing four bytes of EEH in the header marks a sector bad (see Sections 6.5.2 and 6.7.2).

4.10.3 Formatting the Track

When index arrives under the head, the 43x formats the sector with the first four bytes of data. The 43x automatically calculates and appends the ECC to the header, writes zeros into the data field, calculates a data ECC, and appends it to the sector. As each successive sector arrives under the head, the 43x takes four bytes from the buffer and uses them as the header for that sector. The 43x repeats this operation for each sector on the requested track.

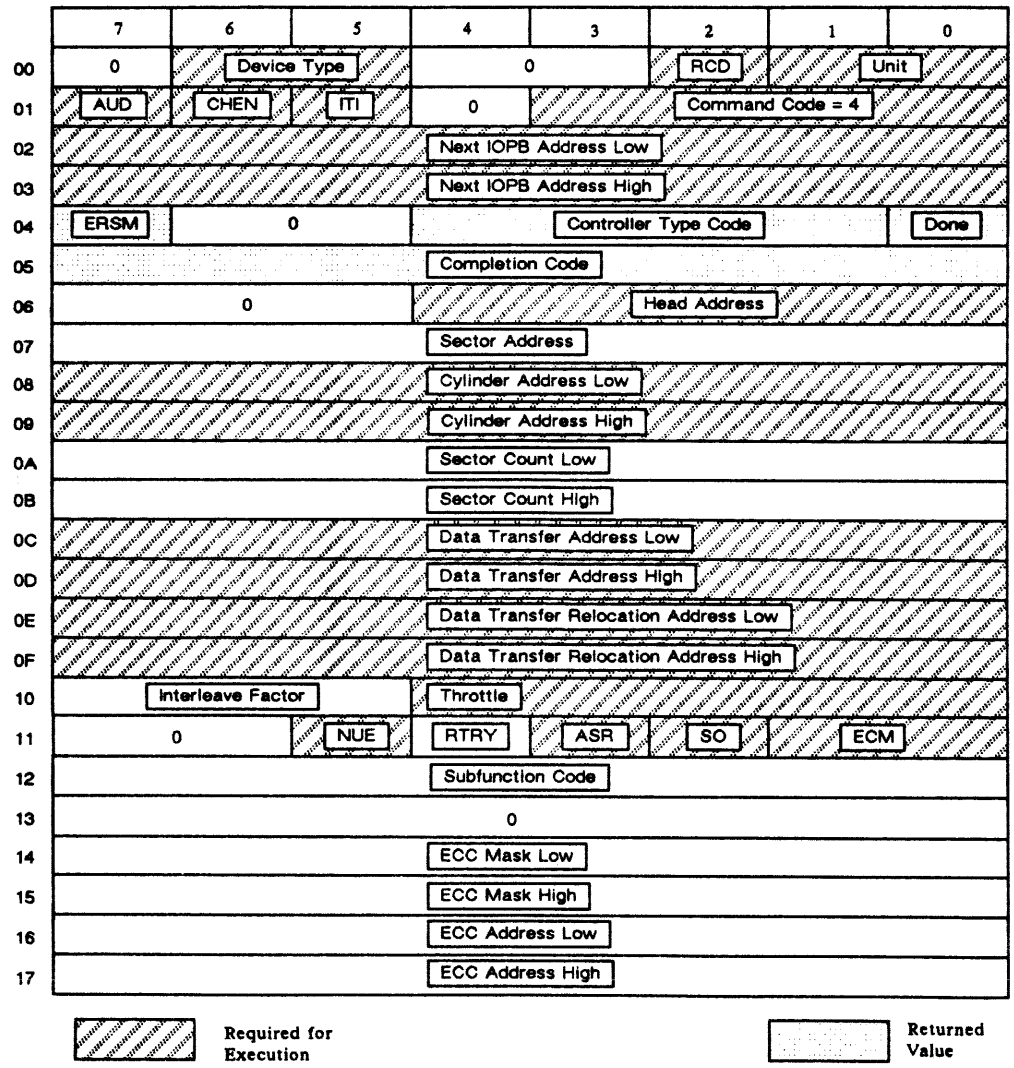
4.10.4 Completing a Disk Transfer

The 43x formats an entire track if no errors occur; it then updates CSTAT0 and CSTAT1, and generates an interrupt, if enabled.

The 43x stops a transfer, along with any chained operations, if a hard error occurs. The only fields it updates are CSTAT0 and CSTAT1, regardless of AUD's value. No soft errors are associated with the Write Track Headers command.

4.11 Winchester Disk Read Track Headers (Command Code 4)

The Read Track Headers and Write Track Headers commands enable system software to map out media defects and create any kind of logical sector organization. They enable sector slipping so data sectors bypass media defects. The Read Track Headers command reads the header from each physical sector, starting at index, and transfers the data to system memory. The headers arrive in physical order and are not necessarily in logical sector order, due to interleaving and sector slip. The Write Track Headers command writes the headers back to the track. The buffer contains the actual header data from each sector on the track, starting at index. Read Track Headers transfers the sector headers for a single track, including sectors marked spare and bad, and suspends overlap operations.



4.11.1 Read Track Headers and Media Defects

The 43x will not transfer the header to system memory if the defect area involves the address mark. Do not rely on this command to set up system memory. Always verify the headers manually before writing them to the disk.

4.11.2 Data Buffer

Software must allocate a data buffer in system memory before issuing a Read Track Headers command. The total buffer length must be four bytes times the total number of physical sectors on the track. The 43x counts the actual number of sectors on the drive and uses this value as the sector count for the Read Track Headers command (see Table 4–1).

Table 4–1. Sample Buffer from a Read Track Headers Command

Buffer Address	Physical Sector	Contents
0	0	Cylinder High
1	0	Cylinder Low
2	0	Head
3	0	Logical Sector Number
4	1	Cylinder High
5	1	Cylinder Low
6	1	Head
7	1	Logical Sector Number
8	2	Cylinder High
:	:	:
4(*n*)H	*n*	Cylinder High
4(*n*)+2	*n*	Cylinder Low
4(*n*)+3	*n*	Head
4(*n*)+4	*n*	Logical Sector Number

4.11.3 Index

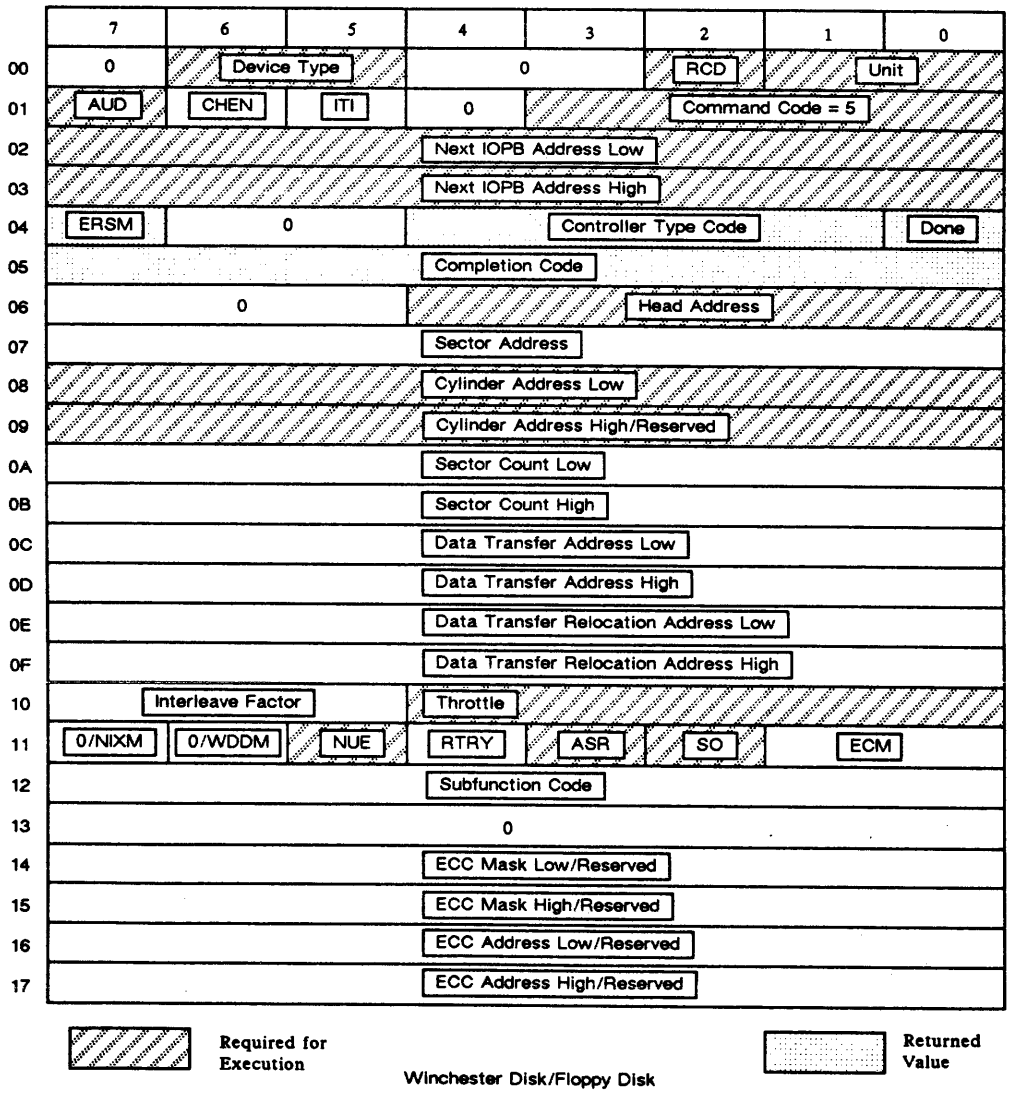
When index arrives under the selected head, the 43x reads the header from the first sector and transfers the track header data to the FIFO buffer.

4.11.4 Read the Track

As each subsequent sector arrives under the head, the 43x reads four bytes from the header and transfers them to the FIFO buffer. The controller repeats this operation for each sector on the requested track. After the 43x reads a complete track, it DMAs all the header data to system memory.

4.12 Seek (Command Code 5)

The Seek command moves the selected disk drive's heads to the cylinder address specified in the IOPB. The 43x scans the drives, determines when each completes its seek, and marks the associated IOPB *Done*. The Seek command is generally used for diagnostic purposes only, since an implied seek is inherent in all data transfer commands.



4.12.1 Winchester Disk Drives

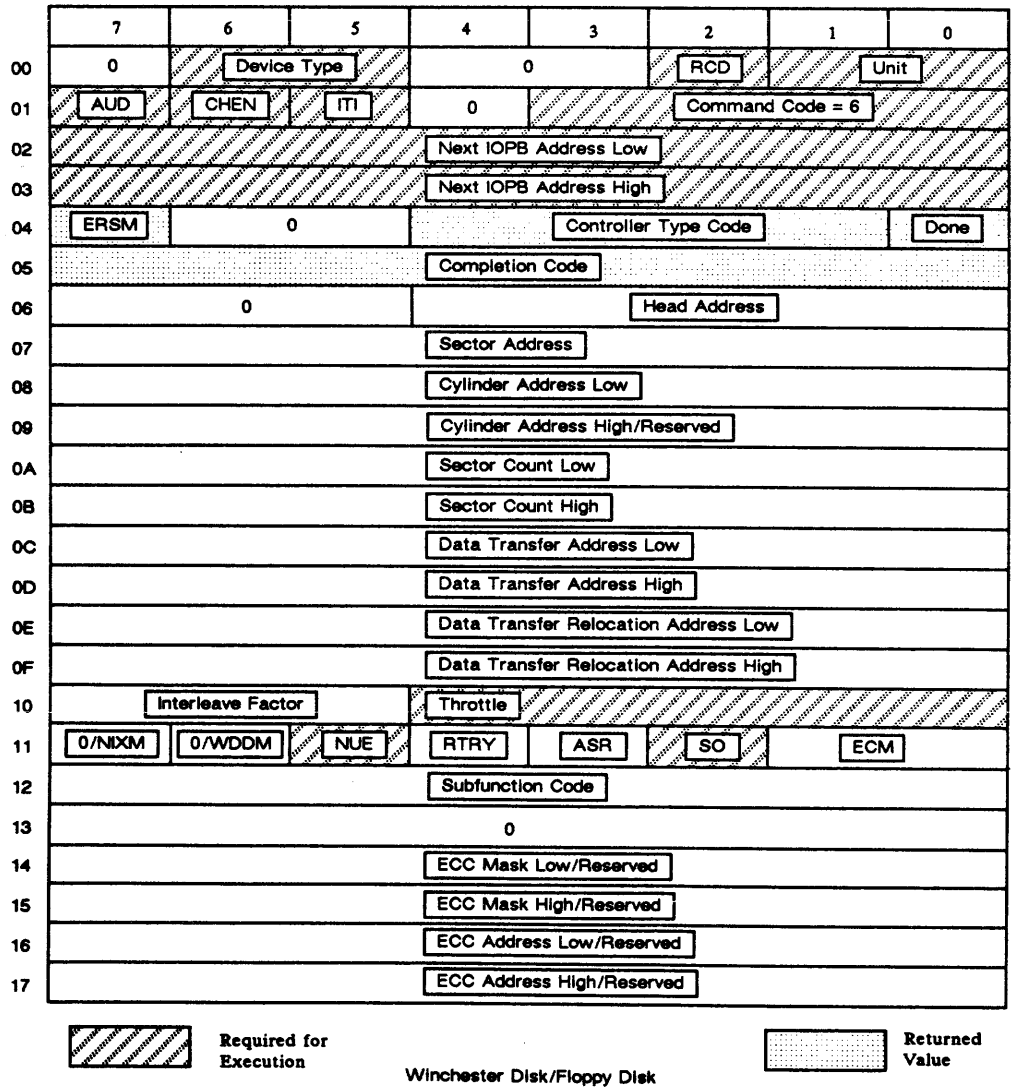
The 43x initiates overlap seeking if IOPBs for different drives are chained together, sequential order is not enabled, and the drives support buffered seeks or serial addressing. If the *Overlap Seek* bit is set, Explicit Seek commands overlap like implicit seeks unless the *Sequential Order* bit is set in each IOPB.

4.12.2 Floppy Disk Drives

Because the on-board microprocessor issues step pulses and monitors the floppy disk, overlap seeking is not possible with floppy disk drives.

4.13 Drive Reset (Command Code 6)

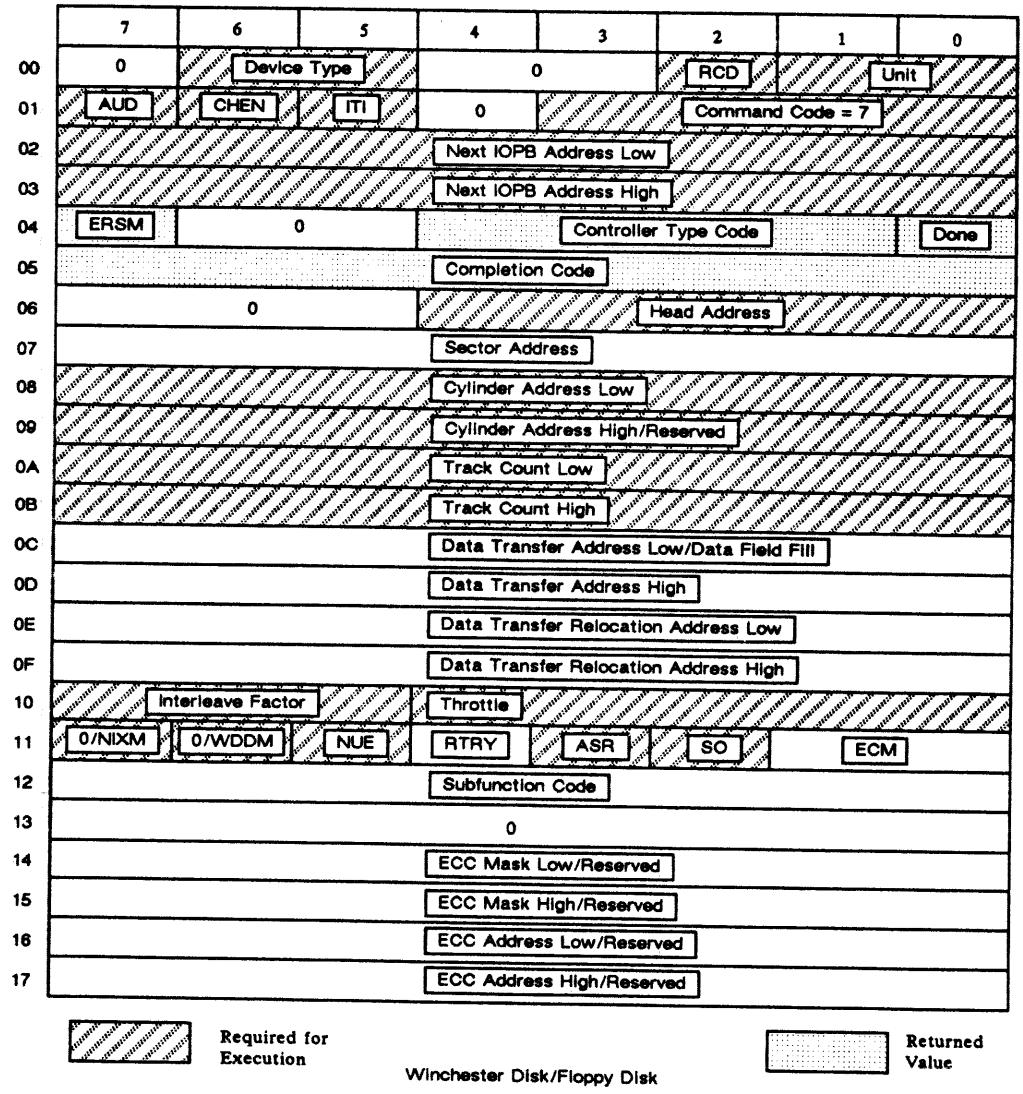
The Drive Reset command deselects and then reselects the drive. The 43x moves the heads back to Cylinder 0 (recalibrate). This command clears drive faults and other drive related problems. Do not use a Drive Reset in the normal course of events as recalibrating is very time consuming.



4.14 Write Format (Command Code 7)

The Write Format command formats a disk with header information, specified by the interleave factor, crossing head and cylinder boundaries as required. For floppy disks, the MT flag specifies these values. The 43x reports IOPB *Done* when the track count reaches zero; it ignores the sector address in the IOPB.

When formatting floppy disk drives that do not use motor-up-to-speed for *drive ready*, execute a seek. Wait the specified *drive ready* time before starting (see your drive manual).



4.14.1 Set Sectors Per Track

4.14.1.1 Winchester Disk Drives

Before issuing a Format command, set the number of physical sectors per track with the Set Drive Parameters command. The number of physical sectors must equal the number of logical data sectors plus the number of allocated spares, minus one.

4.14.1.2 Floppy Disk Drives

Before issuing a Format command, set the following, using the Set Drive Parameters command: the number of physical sectors per track, the recording density, the MT flag, and BPS. Set the interleave factor and NIXM.

The physical format of the media is IBM-compatible: the first sector is numbered 1, and max sector is the total number of sectors. Through the 431 software interface the first sector on a track is addressed as 0, and max sector is the total number of sectors minus one. The 431 automatically converts the logical-to-physical sector numbers. For example, on a 17-sector configuration: the 431 software interface addresses sectors from 0 to 16 (max-1); the actual header format is written from 1 to 17.

4.14.2 Filling the Buffer

4.14.2.1 Winchester Disk Drives

When a drive completes its seek, the 43x accesses the IOPB and determines the command parameters. The 43x fills its own internal buffer for use by the Format command. The only DMA activity during format is the reading and updating of IOPBs.

4.14.2.2 Floppy Disk Drives

Set IOPB Byte C to the fill pattern for use when writing the data field. This Pattern byte fills the data block of each sector. The only DMA activity during format is reading and updating IOPBs (Fill Bytes 00 - F4 only).

4.14.3 Writing the Format

4.14.3.1 Winchester Disk Drives

The 43x waits for the index pulse, then counts the appropriate number of bytes and writes the Sync bits. It then takes the header words out of the FIFO, serializes them, generates an ECC value, and writes the header to the disk. The 43x appends the ECC value generated for the header to the disk header. It then writes the data field portion of the sector, filling it with zeros. The 43x appends the ECC value generated for the data to the data field; it writes all the sectors on a track.

4.14.3.2 Floppy Disk Drives

The 43x waits for the index pulse and then counts the appropriate number of bytes and writes an index address mark if NIXM is clear. It then writes a preamble and the Sync bits, takes the header words out of the FD FIFO, serializes them, generates a CRC value, and writes the header to the floppy disk. The 43x appends the CRC value generated for the header to the header, and the CRC generated for the data to the data field. The 43x writes all the sectors on the track.

4.14.4 Track Count

4.14.4.1 Winchester Disk Drives (IOPB Bytes A and B)

On a Format command, CNTL is the least significant half of the track count; CNTH is the most significant half. The 43x can format 65,535 tracks with one command.

4.14.4.2 Floppy Disk Drives (IOPB Byte A - CNTL)

On a Format command, CNTL is the track count. The 43x is capable of formatting 255 tracks with one command.

4.14.5 Completing a Disk Transfer

The 43x decrements the track count by one each time the disk passes over a track boundary during formatting; for floppy disks, the 43x increments the track or cylinder number, depending on the value of MT. At the end of the track, the 43x tests the track count and determines if the transfer is complete. If the transfer is not complete, it formats the next track. The 43x issues an implied seek each time it increments the cylinder address.

4.14.5 Completing a Disk Transfer (continued)

After the 43x completes the transfer it updates CSTAT0 and CSTAT1, and generates an interrupt, if enabled. The 43x updates the head, cylinder, and track count if AUD is set.

If a hard error occurs, the 43x stops the transfer and marks the IOPB *complete with error*. It updates the head, cylinder, and track count in the IOPB and halts any chained operations.

4.14.6 Spiral Format (432 Only)

The 432 uses a spiral format, accommodating drives that require more time for head switching without losing a revolution. Microcode Revisions 2.1.2 and greater support this format. To specify the spiral factor: load bits 0 through 4 in IOPB Byte 7 with the desired factor (see Table 4–2). The spiral format supports interleaving.

The spiral factor is a slip of physical sectors between logical Sector 0 on the previous and current heads within a cylinder. Head 0 always starts at index. The formula for finding logical Sector 0 on a track is: [(Spiral Factor + 1) x Head] mod-PS, where PS represents the number of physical sectors per track.

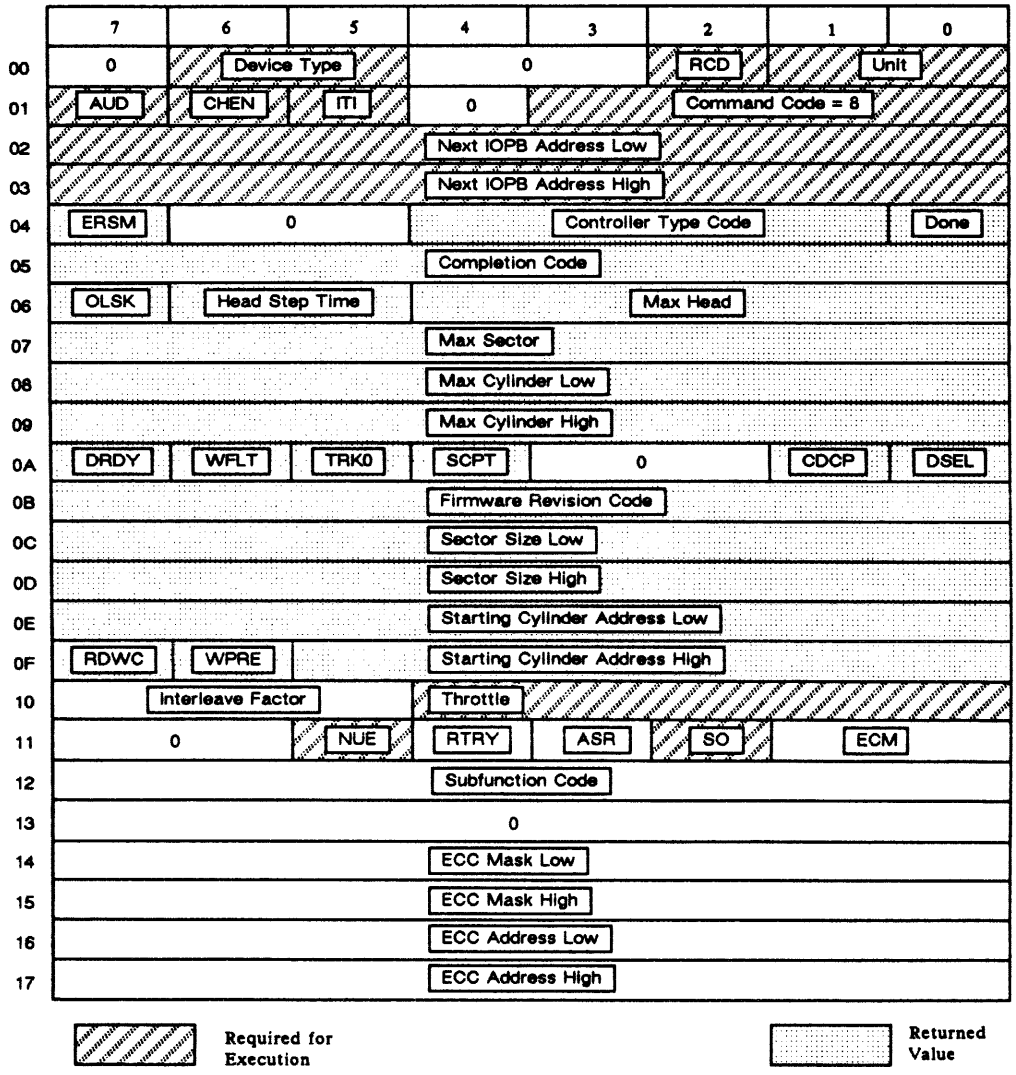
Table 4–2. Spiral Write Values

Spiral Factor Value (Hex)	Offset from Previous Logical Sector 0 (Decimal)
00	1
01	2
02	3
04	5
05	6
06	7
07	8
08	9
09	10
0A	11
0B	12
0C	13
0D	14
0E	15
0F	16
10–1E	Reserved
1F	0 or Spiral Off

4.15 Read Drive Status (Command Code 8)

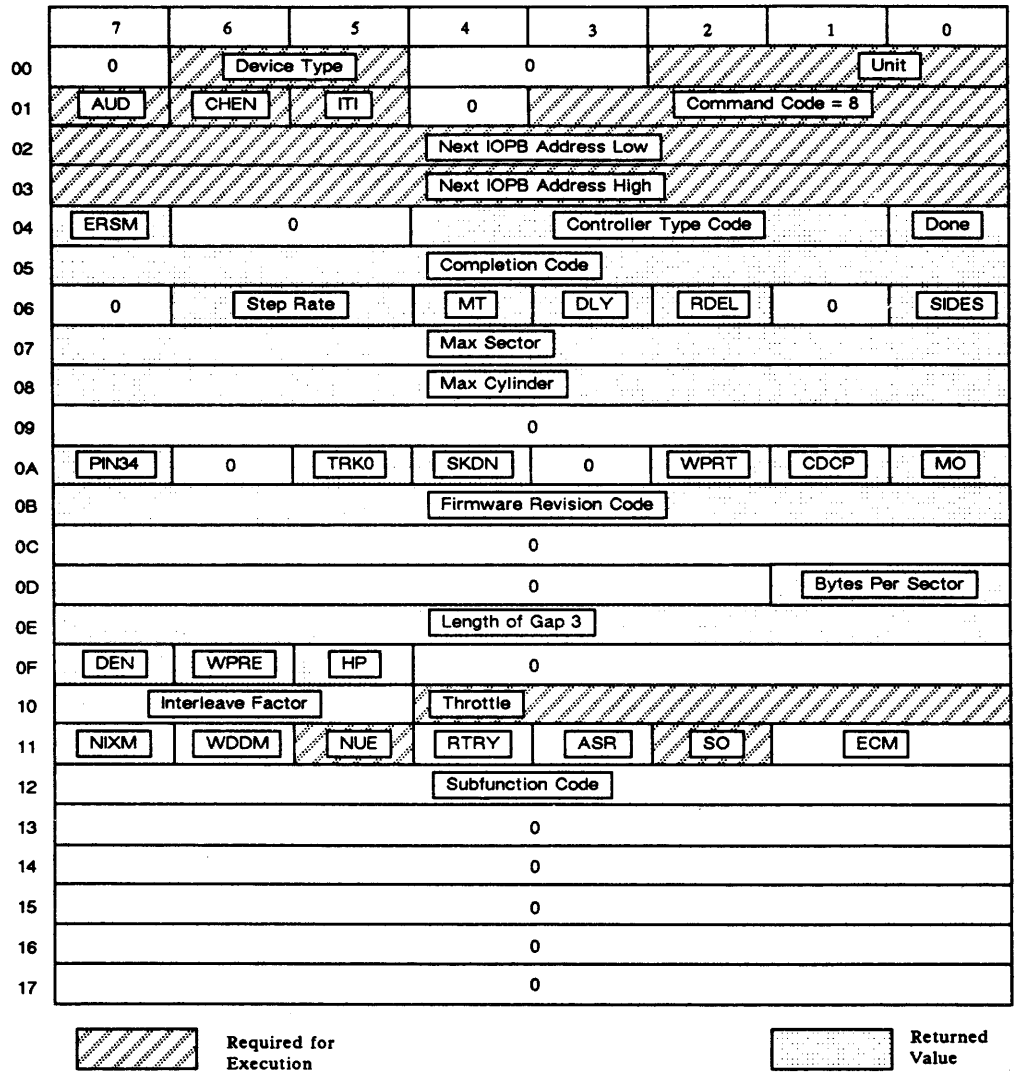
The Read Drive Status command returns the selected drive's parameters and status. The IOPB must include the device type and unit number. The 43x returns the values in Bytes 4 through 13 of the resulting IOPB.

Winchester



4.15 Read Drive Status (Command Code 8) (continued)

Floppy



4.15.1 Maximum Head Number (IOPB Byte 6)

4.15.1.1 Winchester Disk Drives

The 43x returns the maximum head number, step rate, and *Overlap Seek* bit currently set for the drive. A previous Set Drive Parameters command sets these values.

4.15.1.2 Floppy Disk Drives

The 43x returns the current setting for the maximum head number, step rate, and MT. A previous Set Drive Parameters command sets these values.

4.15.2 Maximum Sector Number (IOPB Byte 7)

4.15.2.1 Winchester Disk Drives

The 43x returns the maximum sector number set for the drive. A previous Set Drive Parameters command sets this value.

4.15.2.2 Floppy Disk Drives

The 43x returns the current setting for the maximum sector number. A previous Set Drive Parameters command sets this value.

4.15.3 Maximum Cylinder Number

4.15.3.1 Winchester Disk Drives (IOPB Bytes 8 and 9)

The 43x returns the maximum cylinder number set for this drive. Byte 8 comprises the Max Cylinder Low byte; Byte 9 comprises the Max Cylinder High byte. A previous Set Drive Parameters command sets this value.

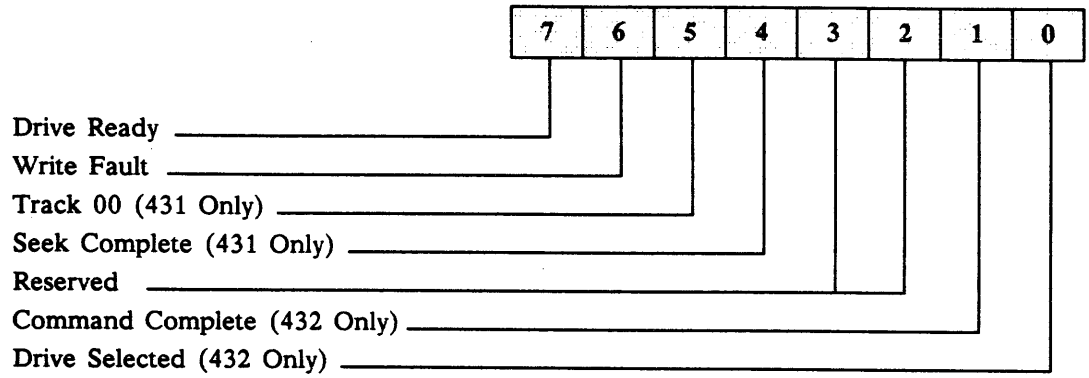
4.15.3.2 Floppy Disk Drives (IOPB Byte 8)

The 43x returns the current setting for the maximum cylinder number. A previous Set Drive Parameters command sets this value.

4.15.4 Drive Status Byte (IOPB Byte A)

4.15.4.1 Winchester Disk Drives

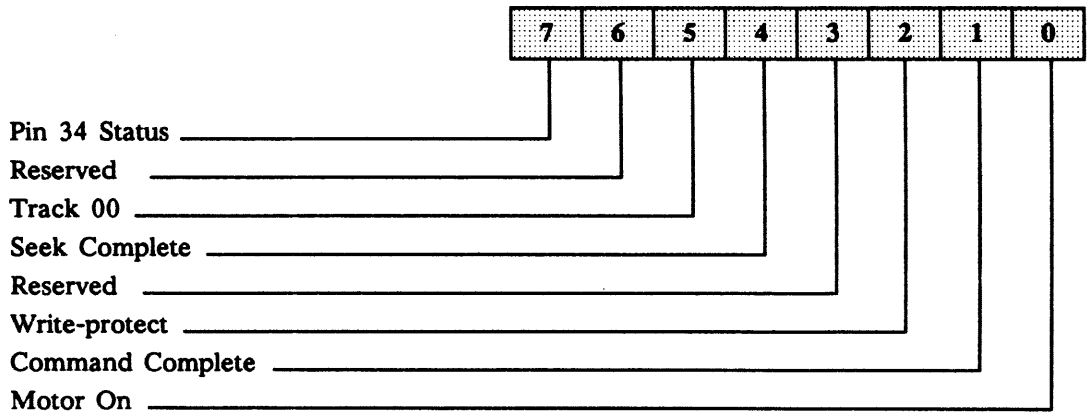
On a Read Drive Status command, the 43x selects the drive and latches the status information. Byte A contains the latched drive status information. The 431 uses only bits 7 through 4; bits 3 through 0 are reserved. The 432 uses all eight bits.



Bit	Mnemonic	Description
7	DRDY	**Drive Ready:** Sets when the drive is ready to read, write, or seek. Clearing DRDY inhibits all reads, writes, and seeks.
6	WFLT	**Write Fault:** The selected drive sets WFLT if there is a drive fault; normally clear.
5	TRK0	**Track 00 (431 Only):** Sets when the drive's read/write heads are positioned at Cylinder 0.
4	SKCT	**Seek Complete (431 Only):** Sets when the 431 completes an implied or explicit seek.
3-2		**Reserved.**
1	CDCP	**Command Complete (432 Only):** The drive sets CDCP to signal command completion. CDCP allows the host to monitor the drive's *command complete* status during explicit overlap operations. CDCP is clear: when the drive initiates a recalibration sequence on power-up, and the read/write heads are not over Track 0, and during the entire command sequence, after receipt of the first *Command Data* bit.
0	DSEL	**Drive Selected (432 Only):** Sets when the controller selects the drive.

4.15.4.2 Floppy Disk Drives

On a Read Drive Status command, the 43x selects the drive and latches the status information. Byte A contains the latched drive status information. The 43x only uses bits 7 through 4 for floppy disks; bits 3 through 0 are reserved.



Bit	Mnemonic	Meaning
7	PIN34	**Pin 34 Status:** Shows the status of the signal on interface pin 34. The signal's exact meaning is drive-dependent.
6		**Reserved.**
5	TRK0	**Track 00:** Sets when the drive's read/write heads are positioned at Cylinder 0.
4	SKDN	**Seek Done:** Sets when a drive completes its seek (normally set).
3		**Reserved.**
2	WPRT	**Write-protect:** The selected drive sets WPRT when the write-protect notch on the floppy disk in the drive is covered.
1	CDCP	**Command Complete:** The FDC is not busy.
0	MO	**Motor On:** Requested by the FDC in response to a previous IOPB.

4.15.5 Disk Firmware Revision Codes (IOPB Byte B)

This byte contains the 43x firmware revision code for the EPROM currently plugged into the board. The 43x returns the following in IOPB Byte B:

Controller Type	IOPB Byte B H	Revision
300-154-9x (431T)	03	A
	04	B
	:	:
300-164-9xx (43S)	80	Prerelease
	81	2.1.x
	82	2.2.x
	:	:
300-168-9xx (432)	00	Prerelease
	01	2.1.x
	02	2.2.x
	:	:

A one in the most significant bit (MSB) of IOPB Byte B denotes the 431S; a zero in the MSB denotes the 431T.

The 431S and the 432 do not report their interim revisions in IOPB Byte B (i.e., they only report two levels deep: 2.1, 2.2, etc.)

4.15.6 Bytes Per Sector

4.15.6.1 Winchester Disk Drives (IOPB Bytes C and D)

IOPB Bytes C and D contain the 43x configuration in bytes per sector. Byte C is the least significant half of the count; Byte D is the most significant half. The bytes per sector parameter is not software programmable.

4.15.6.2 Floppy Disk Drives (IOPB Byte D)

IOPB Byte D contains the encoded number of bytes per sector (BPS) set by a previous Set Drive Parameters command (0 = 128 BPS, 1 = 256 BPS, and 3 = 1 to 24 BPS).

4.15.7 Winchester Disk Reduced Write Current/Write Precompensation (IOPB Bytes E and F) (431 only)

The 43x returns the 16-bit starting cylinder address for Reduced Write Current and/or Write Precompensation in Bytes E and F. Byte E comprises the low bits; Byte F comprises the high bits. Byte F also contains the status of the *Enable* bits for Reduced Write Current and Write Precompensation (see Section 4.16.6).

4.15.8 Floppy Disk Length of Gap 3 (IOPB Byte E)

The 43x returns the length of Gap 3 in IOPB Byte E. Gap 3 follows the data field. A previous Set Drive Parameters command sets this value.

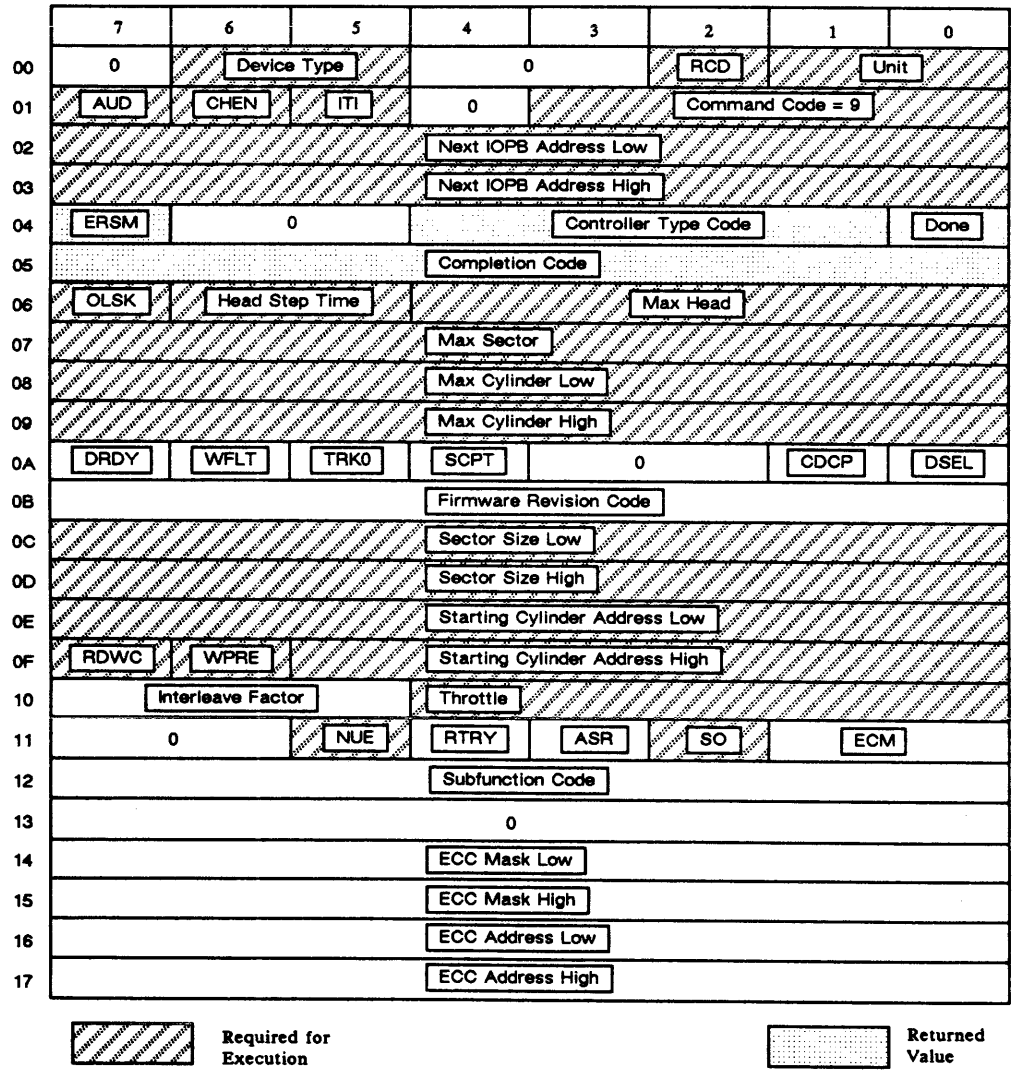
4.15.9 Floppy Disk Recording Format (IOPB Byte F)

The 43x indicates the recording density (single or double), and whether Write Precompensation is enabled, in IOPB Byte F. A previous Set Drive Parameters command sets both options. When set, the *High Performance* (HP) bit enables high performance mode in models 432-103 and above.

4.16 Set Drive Parameters (Command Code 9)

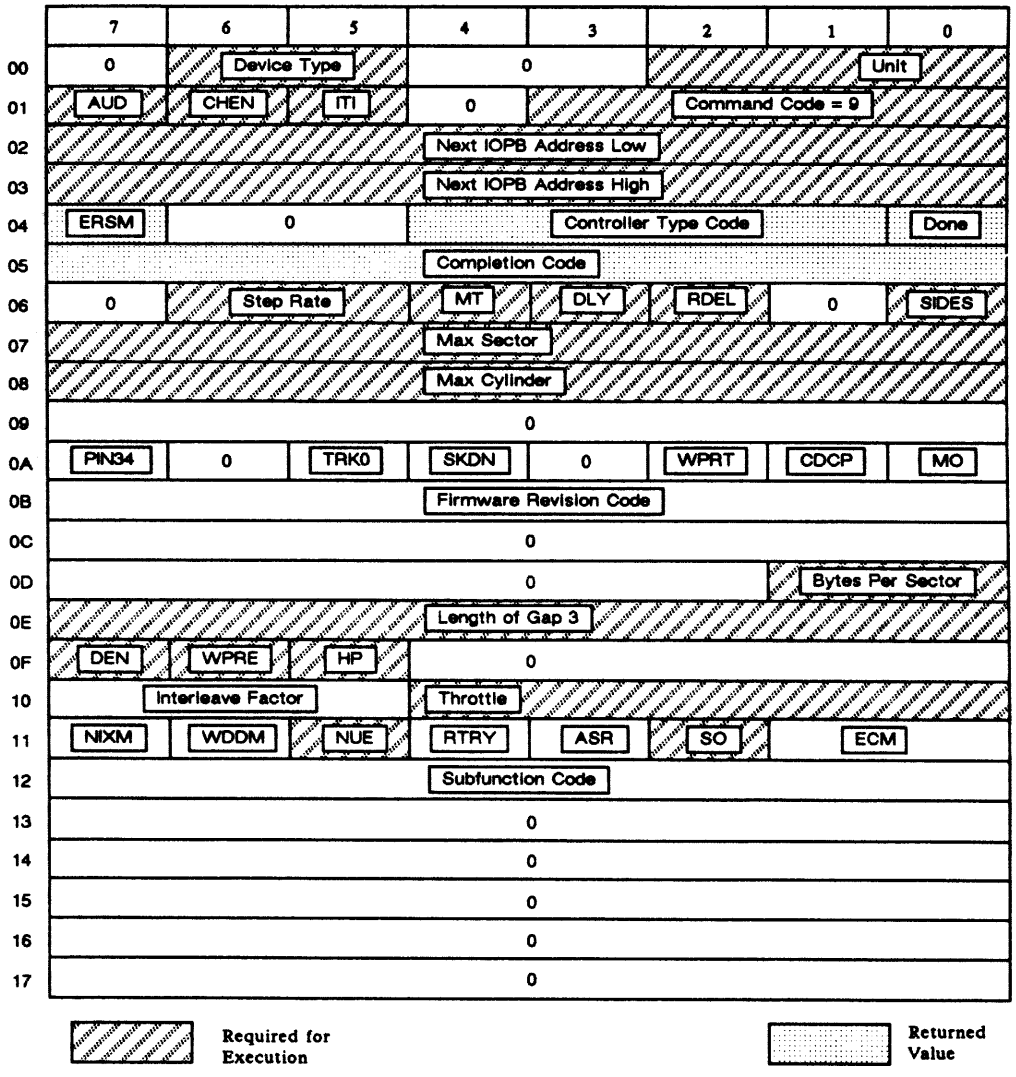
This command customizes the 43x for drives with different numbers of sectors, heads, cylinders, step rates, and densities. Software must specify the device type and unit number.

Winchester



4.16 Set Drive Parameters (Command Code 9) (continued)

Floppy



4.16.1 Winchester Disk Drives

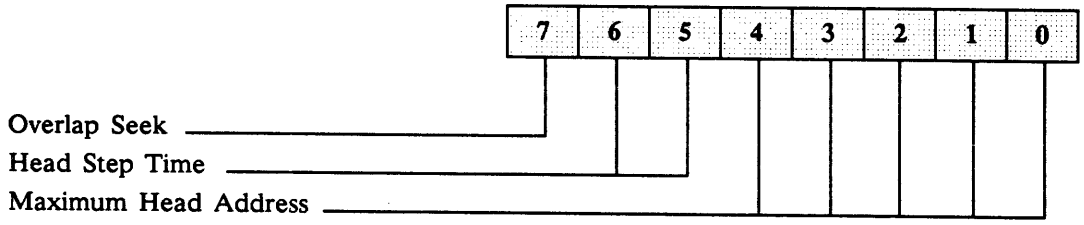
Fill the max head value in Byte 7, the max sector value in Byte 6, and the max cylinder value in Bytes 8 and 9 (9 is the most significant half). For 300-964-9xx series 431 controllers, fill Bytes C and D with the number of bytes per sector (see Section 4.16.9).

On a Set Drive Parameters command, the Data Relocation bytes hold the starting cylinder address for Reduced Write Current and Write Precompensation for the 431. Setting RDWC enables Reduced Write Current; setting WPRE enables Write Precompensation.

This command allows the 43x to control drives that support overlap seeking and various step rates. A *Controller Reset* does not clear the parameters that Set Drive Parameters sets.

4.16.2 Drive Option Byte (IOPB Byte 6)

4.16.2.1 Winchester Disk Drives



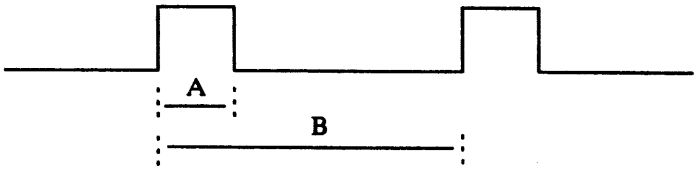
Bit	Mnemonic	Description
7	OLSK	**Overlap Seek:** When set, the 43x enables overlap seeking, when possible. See the drive manufacturer's manual and determine if your drive supports overlap seeking in a multiple drive configuration. Only buffered seeks and serial mode addressing allow overlap seeking. Buffered seek drives must allow the 43x to deassert the *Direction* line when overlap seeking.
6-5	HST	**Head Step Time (431 Only):** Selects the head step time. Short head steps imply buffered seeks. For maximum performance, select the fastest head step time your drive supports (see your drive manual), then select a slower 431 head step time. For example, if your drive has a step time of 8 µs, use the 15 µs controller step time.

4.16.2.1 Winchester Disk Drives (continued)

Bit	Mnemonic	Description

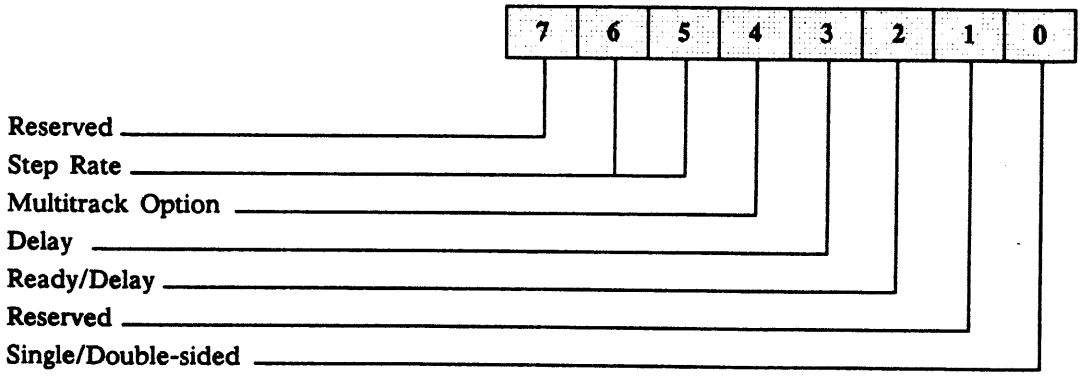
6-5 HST **Head Step Time (431 Only) (continued):** Using a 7 µs head step time may affect tape streaming since the 431's microprocessor is not internally interrupt-driven after issuing step pulses. If this is a problem in your application, use a head step time of 15 µs. HST options include:

Bits 6-5	Step Times: A	B
0	3.2 µs	3.05 ms
1	2.6 µs	15 µs
2	2.2 µs	7 µs
3	Reserved	



4-0 MAXH **Maximum Head Address:** Selects the maximum head address. The 432 uses all five bits; only bits 3 through 0 are valid for the 431.

4.16.2.2 Floppy Disk Drives



4.16.2.2 Floppy Disk Drives (continued)

Bit	Mnemonic	Description
7		**Reserved.**
6-5	STEP	**Step Rate:** Step defines the rate at which the controller issues step pulses to the drive, causing it to seek to another cylinder (drive-dependent). The four possible rates are:

Bits 6-5	Rate
00	6 ms
01	12 ms
10	20 ms
11	30 ms

4	MT	**Multitrack Option:** MT defines the controller's action after reaching the last sector on a track. When set, the 43x sets the sector address to one and increments the head address. If the head address is greater than one, the 43x clears it to zero and increments the cylinder address. A transfer operates on one full cylinder (two surfaces) before going to the next cylinder. When clear, the 43x sets the sector address to one and increments the cylinder address. A transfer operates on one full surface before going to the next surface.
3	DLY	**Delay:** When DLY and RDEL are set, the 43x has a short delay between asserting the *Head-load* signal and initiating a read or write operation to the floppy drive. When DLY is clear and RDEL is set, the 43x has a longer delay before initiating a read or write operation.
2	RDEL	**Ready/Delay:** When set, the 43x delays for a set amount of time, as per DLY, before initiating a read or write to the floppy drive. When clear, the *Ready-L* signal from the drive indicates when the drive is up to speed or the heads are loaded. DLY and RDEL depend on the type of floppy drive you are using. The distinguishing characteristics are: 1) the drive sends an active *Ready-L* signal (on pin 34 of the floppy interface) to the 43x indicating it is ready for a read or write, or 2) the drive either continually sends an active *Ready-L* signal or sends no active *Ready-L* signal.

4.16.2.2 Floppy Disk Drives (continued)

Bit	Mnemonic	Description
2	RDEL	**Ready/Delay (continued):** If the drive sends an active *Ready-L*, the 43x asserts the *Head-load* signal and waits for *Ready-L* from the drive before initiating a read or write. If there is a continuous active *Ready-L* signal or no active *Ready-L* signal from the drive, the 43x asserts *Head-load* and waits a predetermined period of time, assumes the drive is up to speed, and then initiates the read or write. The following chart shows how the 43x reacts to DLY and RDEL.

DLY	RDEL	Jumper JL	43x Action
N/A	0	1,2	Waits for *Ready-L* from drive
1	1	2,3	Short delay before Init. R/W
0	1	2,3	Long delay before init. R/W

1		**Reserved.**
0	SIDES	**Single/Double-sided:** Specifies whether the drive supports single- or double-sided floppy disks. A zero indicates single-sided disks; a one indicates double-sided disks.

4.16.3 Sectors per Track (IOPB Byte 7)

4.16.3.1 Winchester Disk Drives

The IOPB must contain the maximum number of sectors per track minus one. If the Winchester disk you are using is set for 32-sectors per track, the maximum sector is 31, and the physical sectors are numbered from 0 through 31.

4.16.3.2 Floppy Disk Drives

The IOPB must contain the number of sectors per track. If the floppy disk is set for 17-sectors per track, the maximum sector is 16, and the sectors are numbered 0 through 16. This byte indicates the value that software set for the drive parameters; i.e., max sector minus one.

4.16.4 Maximum Cylinder

4.16.4.1 Winchester Disk Drives

The IOPB must contain the maximum number of cylinders minus one. If the Winchester disk you are using has 823 cylinders, the maximum cylinder number is 822; the 43x refers to them as Cylinders 0 through 822. Enter the value 36H in Byte 8, and 03H in Byte 9 (336H is the hexadecimal equivalent of 822).

4.16.4.2 Floppy Disk Drives

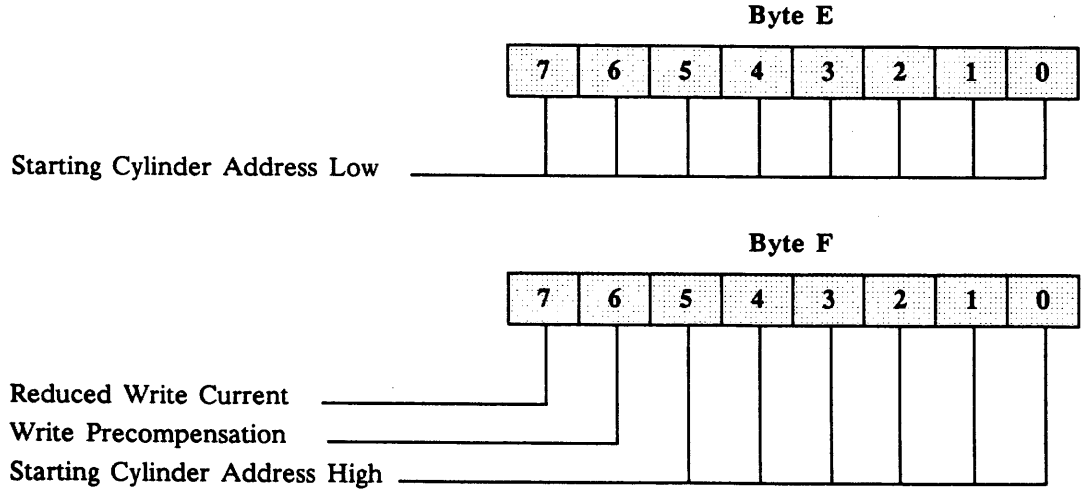
The IOPB must contain the maximum cylinder value minus one. If the floppy disk has 77 cylinders, the maximum cylinder number is 76; the 43x refers to them as Cylinders 0 through 76. The actual format written on the disk is 1 through 77.

4.16.5 Floppy Disk Bytes per Sector (IOPB Byte D)

The IOPB must contain the encoded bytes per sector for all Read, Write, and Format commands. The 43x writes the encoded value in the header during format. Zero = 128 bytes per sector (BPS), 1 = 256 BPS, 2 = 512 BPS, and 3 = 1024 BPS. A value of zero is valid only with single density operations.

4.16.6 Winchester Disk Reduced Write Current/Write Precompensation (IOPB Bytes E and F) (431 Only)

IOPB Byte E contains the least significant half of the starting cylinder address; Byte F contains the most significant half. During Set Drive Parameters, use these bytes to set the starting cylinder address for Reduced Write Current and Write Precompensation for ST506/ST412-type drives (431).



4.16.6 Winchester Disk Reduced Write Current/Write Precompensation (IOPB Bytes E and F) (431 Only) (continued)

Bit	Mnemonic	Description
7	RDWC	**Reduced Write Current:** Setting RDWC enables Reduced Write Current starting at the cylinder specified in Bytes E and F. The 431 supports drives requiring Reduced Write Current with up to eight heads. When clear, the 431 changes the definition of the Reduced Write Current line to Head 23 in the ST506/412 interface, and supports drives with up to 16 heads.
6	WPRE	**Write Precompensation:** Setting WPRE enables Write Precompensation starting at the cylinder specified in Bytes E and F.
5-0	SCYL	**Starting Cylinder Address:** SCYL is the most significant half of the starting cylinder address for Reduced Write Current and Write Precompensation. IOPB Byte E is the least significant half of this address.

4.16.7 Floppy Disk Length of Gap 3 (IOPB Byte E)

This byte sets the length of Gap 3 in each sector. The maximum value for Gap 3 is 141 (8DH) in double density or 134 (86H) in single density (see Table 4-3). Gap 3 follows the data field; use it to format floppy disks with non-standard Gap 3 lengths. The following formula calculates the recommended values for this field:

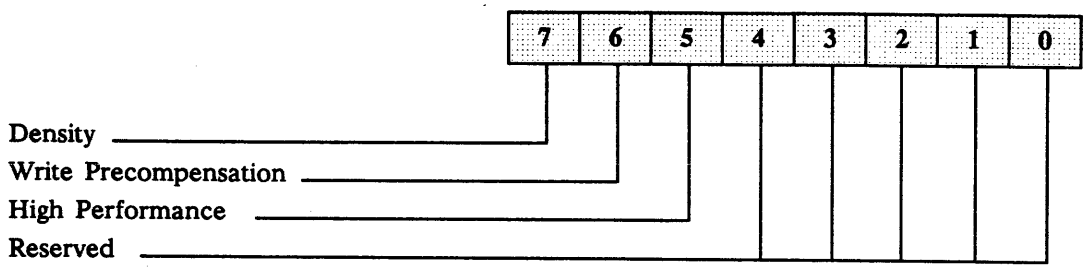
[2 x (maximum rotational speed variation) x BPS] + [Read After Write Recovery Time ÷ (32 μs MFM or 64 μs FM)]; with 1.5% long term and 1.5% instantaneous variation, and 1 ms Read After Write recovery; this is 6% of BPS plus 36 or 17.

Table 4-3. Typical Length of Gap 3 in Bytes

Sector Size	Single Density (Dec)	Single Density (Hex)	Double Density (Dec)	Double Density (Hex)
128	25	17	-	-
256	32	20	49	31
512	47	2F	64	40
1024	78	4E	95	5F

4.16.8 Floppy Disk Recording Format (IOPB Byte F)

Byte F specifies the recording density and whether or not Write Precompensation is enabled.



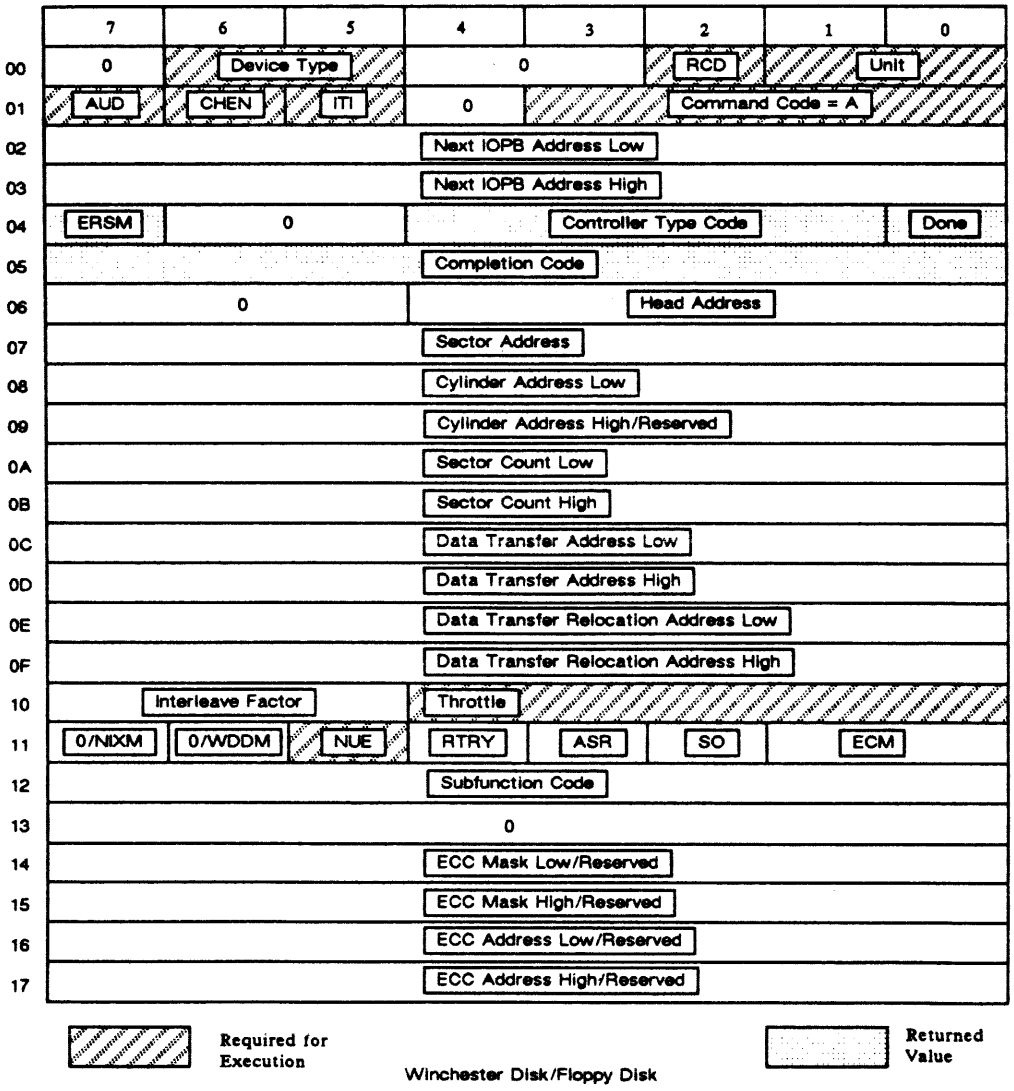
Bit	Mnemonic	Meaning
7	DEN	**Density:** Setting DEN selects double density recording. Clearing DEN selects single density recording.
6	WPRE	**Write Precompensation:** Setting WPRE enables Write Precompensation. Clearing WPRE disables Write Precompensation.
5	HP	**High Performance:** Setting HP enables high performance mode for drives that support quad-density formats.
4-0		**Reserved.**

4.16.9 Winchester Disk Bytes per Sector (IOPB Bytes C and D)

Fill Bytes C (Sector Size Low) and D (Sector Size High) with the number of bytes per sector. The three sector sizes Xylogics supports, and their hexadecimal equivalents, are: 100H = 256 bytes per sector, 200H = 512 bytes per sector, and 400H = 1024 bytes per sector.

4.17 Self Test (Command Code A)

The Self Test command starts the internal controller test, which is similar to the test that runs automatically on power-up and Multibus *INIT*. This test checks the 43x I/O, RAM, and ROM. The 43x completes the diagnostic in approximately one second. While the diagnostic is running, CRDY is clear, and the diagnostic LED (L1) is on. All registers can be read during the process. The 43x reports a *success* status if it completes the self test. If the 43x fails, and it is still capable of DMAing status, it reports the appropriate error code and L1 remains on (see Section 6.3.1, Codes 18, 28, 38, 48, 58). The 43x only runs the self test if CHEN is clear.



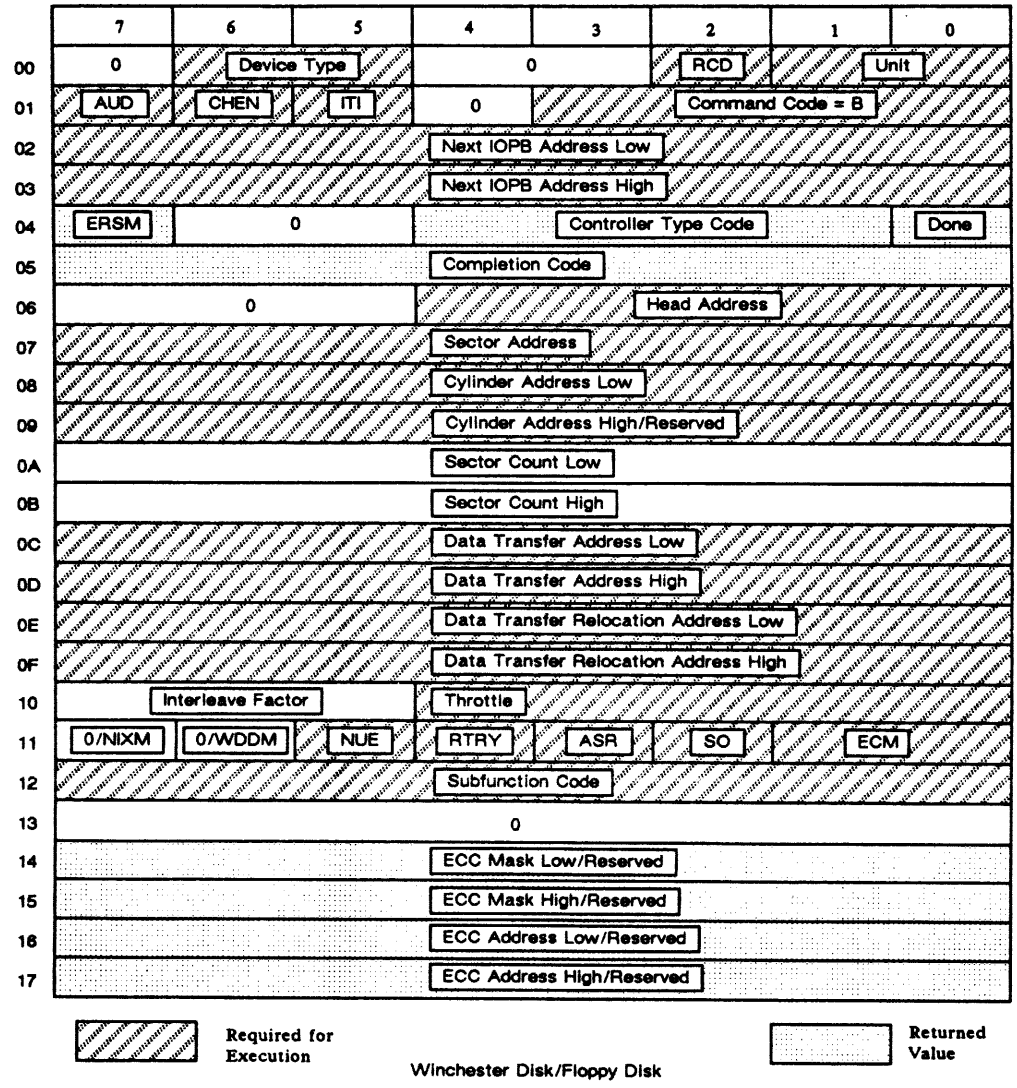
4.17 Self Test (Command Code A) (continued)

There are five self tests: Self Test 1 tests the tape RAM address, Self Test 2 tests the tape RAM data, Self Test 3 tests the Header Shift Register, Self Test 4 tests the DMA controller chip (DMAC), and Self Test 5 tests the DMA circuitry. If the 43x fails one of these tests, it posts the test number in Register XX82 and the completion code in IOPB Byte 5.

The 43x aborts the Self Test command with an *illegal device type* error and does not execute the test if system software specifies an invalid drive type.

4.18 Maintenance (Command Code B)

Specify Maintenance commands via the subfunction codes.



4.18.1 Executing the Maintenance Command

4.18.1.1 Winchester Disk Drives

The Winchester Disk Maintenance command works on physical sectors, including all sectors on the disk (spare, good, and bad). The Read Data and ECC subfunction can recover data, if necessary, by reading sectors with errors in the header or data field. Count Sectors counts all the sectors on a Winchester disk, including spares, good, bad, and runts.

4.18.1.2 Floppy Disk Drives

The Floppy Disk Maintenance command reads all the bytes on a track including address marks, sector headers, Sync bytes, CRC fields, data fields and gaps. It can also be used for rotational position sensing.

4.18.2 Maintenance Command Subfunction Codes

4.18.2.1 Winchester Disk Drives

Code	Description
0	**NOP:** This subfunction is identical to the NOP command.
1	**Write Data and ECC:** The 43x gets the data and ECC, specified by the data address, from system memory, and writes the Data and ECC words onto the Winchester disk (see Table 4–4). System software must specify the physical sector number for the 43x to write the sector in the correct position on the Winchester disk.
2	**Read Data and ECC:** The 43x reads the Data and ECC words from specified sectors on the Winchester disk into the system memory locations specified by the data address. The 43x reads an additional four bytes for each sector and may read multiple sectors. The 43x can read the sectors in the correct order from the drive only if system software specifies the physical sector number. The 43x omits the header verification before reading or writing the data. The Read Data and ECC command is a useful diagnostic aid; it may also be used to recover data from sectors with possible hard ECC errors.

4.18.2.1 Winchester Disk Drives (continued)

Code — Description

2 — Read Data and ECC (continued):

Table 4–4. Byte Number/Definition

Byte Number	Byte Definition
1 to *n*	*n* Bytes of Data Field
(*n*+1) to (*n*+4)	4 Bytes of ECC on Data Field

3 — Sectors Per Track Count: The 43x counts the actual number of sectors on a specific track and displays the count in IOPB Byte 7. This command requires that software load a cylinder and head number into the IOPB.

4-255 — Reserved Subfunctions: An *unimplemented command* error occurs if software specifies these codes.

4.18.2.2 Floppy Disk Drives

Code — Description

0 — NOP: This subfunction is identical to the NOP command.

1-3 — Reserved.

4 — Read Next Header: The 43x uses Read Next Header for rotational position sensing. It transfers six bytes of information from the header of the next sector and passes them under the disk heads to the buffer pointed to by the IOPB's data address and relocation fields. The 43x ignores the IOPB's count field (Bytes A and B) and does not issue a seek (see Table 4–5).

Table 4–5. Read Next Header Format

Byte	Description
0	Cylinder Number (0-76)
1	Side Number (0 or 1)
2	Sector Number
3	Sector Length (0=128, 1=256, 2=512, 3=1024)
4	CRC
5	CRC

4.18.2.2 Floppy Disk Drives (continued)

Code	Description
5	**Read Full Track:** The 43x reads the entire track from index pulse to index pulse. It transfers all bytes in the track, including gaps, address marks, headers, CRC fields, and data fields, to the buffer pointed to by the IOPB's Data Address and Relocation Address bytes. Use this when reading foreign disks, recovering data with CRC errors, and for diagnostic purposes. A 5.25-inch MFM floppy disk (DD) has a nominal capacity of 6250-bytes per track. Allowing 2% speed variation, the buffer should have 6375 bytes. For FM recording (SD), allocate a 3200-byte buffer. The 43x performs no CRC checks, the data stream includes gap information, there is no internal side comparison, and the address mark (AM) detector remains on until command completion. The 43x may look for an AM if there are write splices or noise; it sets the *lost data* status flag if it doesn't find one. The ID AM, ID field, ID CRC bytes, DAM, Data, and Data CRC bytes for each sector will be correct. The 43x may read the Gap bytes incorrectly during write splice time because of synchronization.
6-255	**Reserved Subfunctions:** An *unimplemented command* error occurs if software issues these commands.

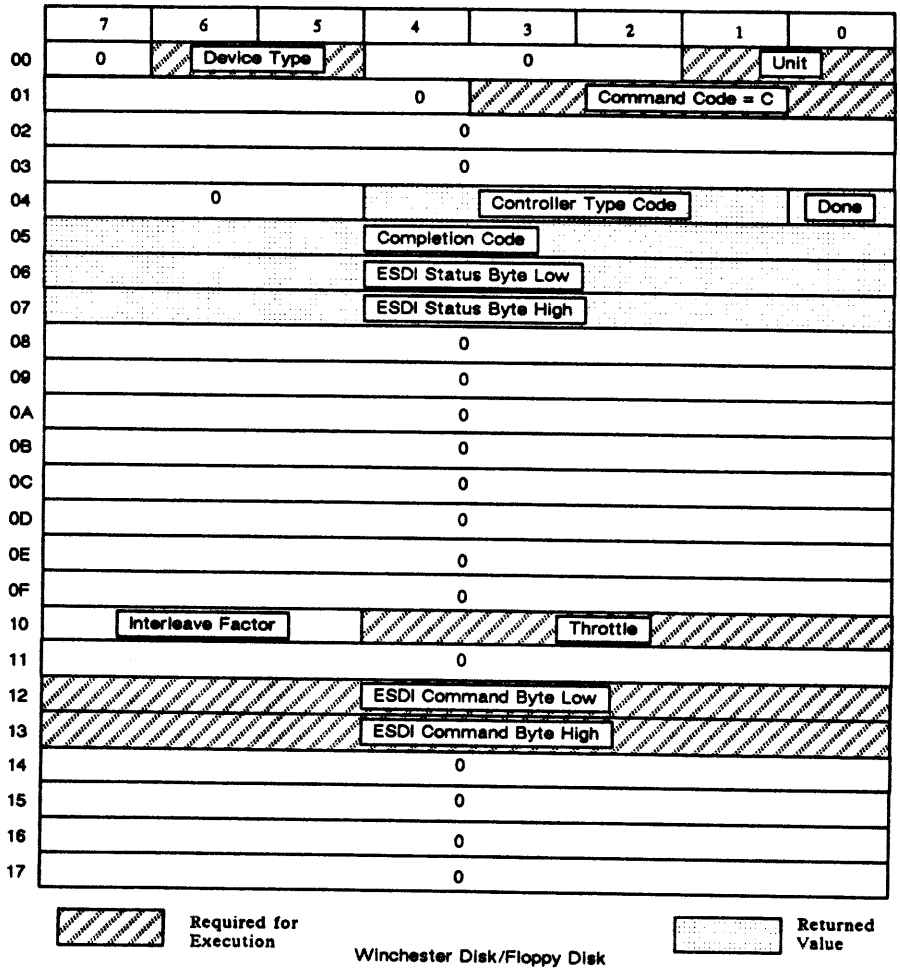
4.18.3 Winchester Disk Direct Memory Access

The Read/Write Data and ECC commands DMA data identically to other commands; the 43x increments the sector, head, and cylinder numbers.

4.19 Winchester Disk Send Serial (Command Code C) (432 Only)

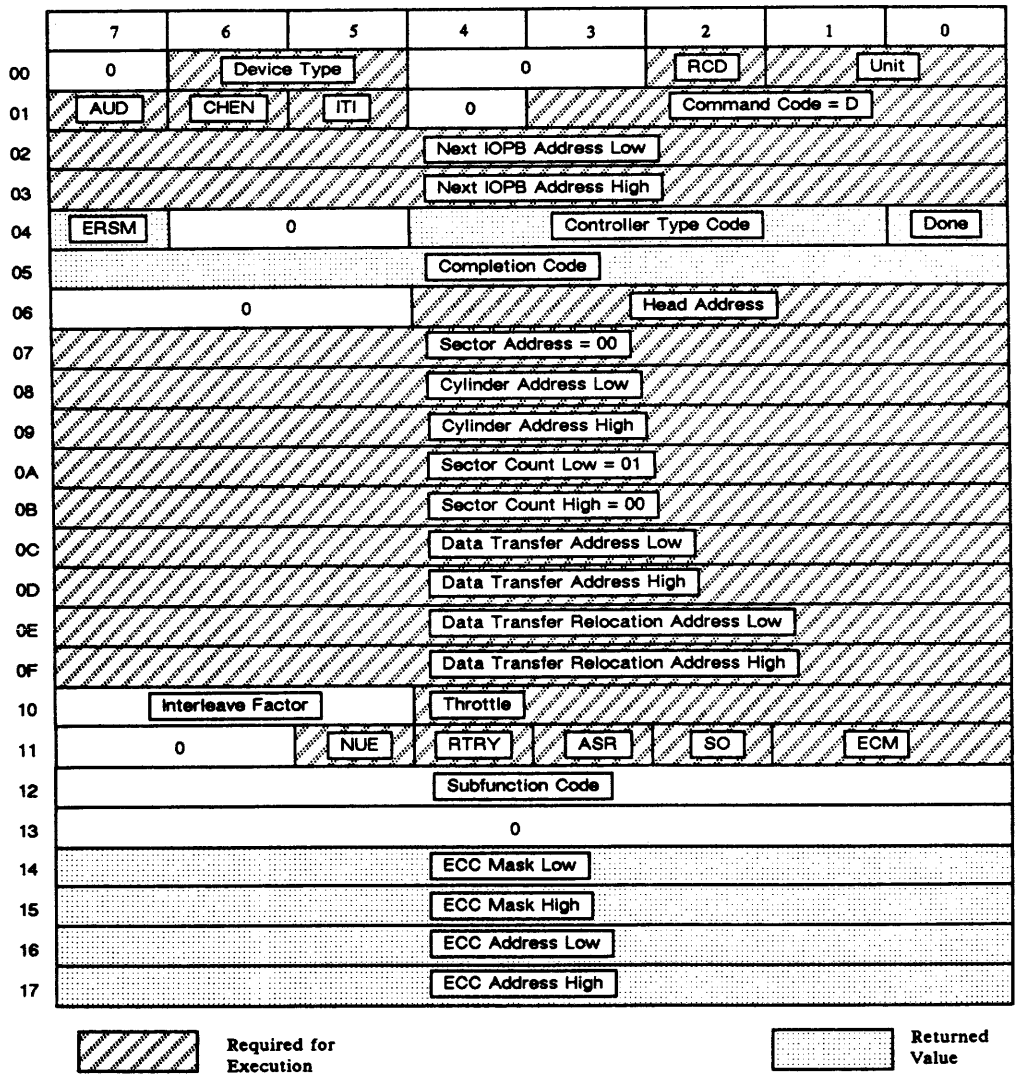
The Send Serial command transfers a Serial command directly to an ESDI drive. Specify this command by entering the appropriate code into IOPB Bytes 12 and 13. For commands that return information, the microcode displays the information in IOPB Bytes 6 and 7. These bytes are valid only for commands returning status or configuration information.

The Send Serial command is two bytes wide plus a parity bit. The 432 automatically calculates and appends parity to the command. If the drive is faulted, the 432 allows only a Reset Attention or Request Status command. If any command causes a drive fault, or if a command times out, the 432 reports an *ESDI drive fault* or *disk sequencer* error. The ESDI Specification, Revision F (January 31, 1986) or later, details the commands. The drive manual lists the commands that your drive supports.



4.20 Winchester Disk Read Defect Map (Command Code D) (432 Only)

The 432 transfers the defect map data (including the header, header CRC, data field, and data CRC) on the track specified by the disk address bytes to system memory, starting at the DMA address. The *Flag* bits in the sector's header field determine the transfer length. Xylogics recommends allocating a buffer large enough to handle the worst case transfer size (see Figure 4-1 and Table 4-6).



4.20 Winchester Disk Read Defect Map (continued)

CYL	
CYL	Header
HD	
SEC	
Flag	
CRC	
CRC	
Month	
Day	
Year	
Head	Date
Pad	
Pad	
CYL MSB	
CYL LSB	First Defect
Byte Count MSB	
Byte Count LSB	
Error Length (Bits)	
"	
"	Second Defect
"	
"	
End of Sector	
CRC	
CRC	

Figure 4–1. Defect Map Data Transferred to Memory

Table 4–6. Defect Map Data Transferred to Memory

Flag	Sector Size	Total Bytes Transferred
00	256	265
01	512	521
10	1024	1033
11	2048	2057

4.20.1 Position and Data Verification

The 432 verifies its position by detecting index and the Header Sync byte, and comparing (bit-by-bit) the Cylinder, Head, Sector, and Flag bytes. The 432 does not check the CRC bytes on the header.

The 432 verifies the data using the CRC bytes appended to the data field. The 432 implements this check as per the ESDI Specification (Revision F).

4.20.2 Error Reporting

A *header not found* error (Code 24) occurs if the 432 does not detect the proper header. The 432 does not differentiate between *cylinder/head header* and *header not found* errors. When the 432 reports the error, it does not transfer the defect map data to system memory.

A CRC error on the data results in a *CRC* error (Code 14). The 432 transfers the defect map data to system memory, but the data is unreliable. Use it with caution, or not at all.

4.20.3 Using the Defect Map

Before using the defect map, determine the location and length of the factory-detected defect. The position of the defect is provided in bytes from the index mark. To translate the byte from index count into a physical sector location, you must know the drive's format. For soft-sectored drives, the 432 always determines the unformatted sector size. For hard-sectored drives, the 432 makes the calculation. You can override the 432 by setting the drive, if possible, or by executing a Send Serial command (set unformatted bytes per sector).

4.20.3 Using the Defect Map (continued)

Soft sector format involves:

Index gap = 100 bits;
Physical sector size = 23 + 2 (PLO Sync) + SSZ + ISG + SPD TOL;
where 1) PLO Sync and ISG are as reported from drive;
2) SSZ = formatted bytes per sector, i.e., 256, 512, 1024; and
3) SPD TOL, if required, is as follows:

Logical Sector Size	SPD (1%)	TOL (2%)
256	4	7
512	7	13
1024	12	23

Hard sector format, if determined by the 432, involves:

Index gap as reported by the drive via ISG bytes after the index/sector pulse.
Physical sector size = 19 + 2 (PLO Sync) + SSZ + ISG.

Section 5: Tape Commands

Section 5: Tape Commands

5.0 Introduction

An IOPB diagram follows each command description. The diagrams indicate which bytes the 43x requires for command execution, and which bytes it returns after execution. System software must post the appropriate tape subfunction code into each IOPB.

The four least significant bits of the Command byte are the *Command Code* bits. These four bits allow up to sixteen possible commands, four of which are reserved. The 43x commands comprise a 24-byte long IOPB.

Due to the nature of tape, there are a number of conditions that are not errors, but which affect software. The 43x reports these conditions via the status bits in TSTAT0 and TSTAT1. Typically, if the 43x sets these bits, it also sets ERSM in CSTAT0, and reports a successful completion in CSTAT1. Always check ERSM after a successful command completion for any special conditions. Check TSTAT0 and TSTAT1, whether ERSM is set or not, for BOT or a detected a file mark.

If no errors occur, the 43x sets *Done* in CSTAT0, and generates an interrupt, if ITI is set. It continues processing an IOPB chain if CHEN is set. If a hard error occurs, the 43x terminates the command, stops the IOPB chain, and, if ITI is set, generates an interrupt. The 43x sets ERR , ERSM and *Done*, and posts a completion code in CSTAT1. The 43x fully updates TSTAT0 through TSTAT4, regardless of AUD's setting, except when NUE is set. The 43x does not update Tape Status Bytes 3, 4, and 5 on hard errors. You may examine these bytes by issuing a Read Drive Status command.

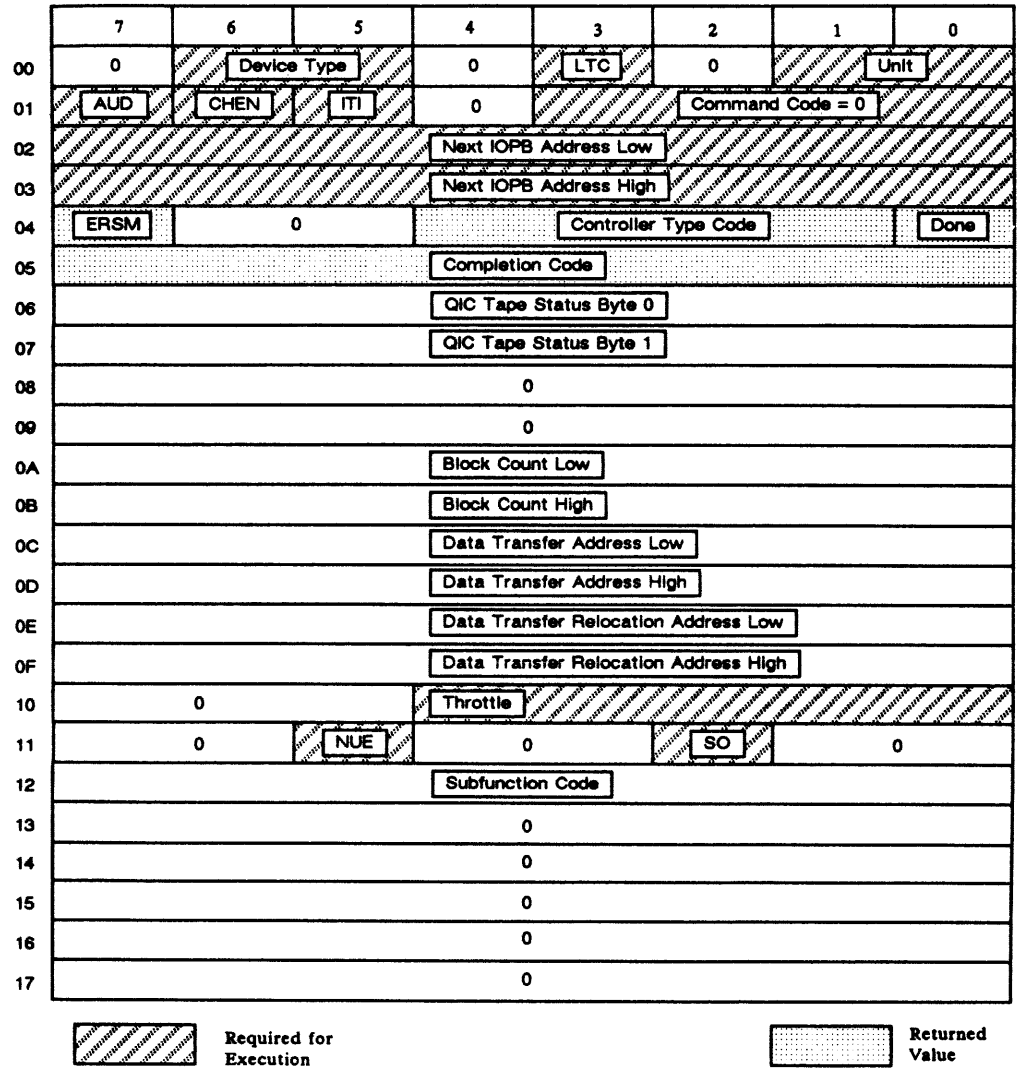
If the 43x encounters a soft error, it continues processing an IOPB chain, and sets ERSM and *Done*. If ITI is set, the 43x interrupts after completing the IOPB.

If a gross tape drive error occurs, such as removing a cartridge while the drive is running or powering off the drive while it is running, the 43x hangs on the next IOPB. If this occurs, execute a *Controller Reset* before issuing another command. Depending on the error, a Tape Drive Reset may also be necessary.

Throttle considerations are the same as for the Winchester disk (see Section 4.3).

5.1 No Operation (NOP) (Command Code 0)

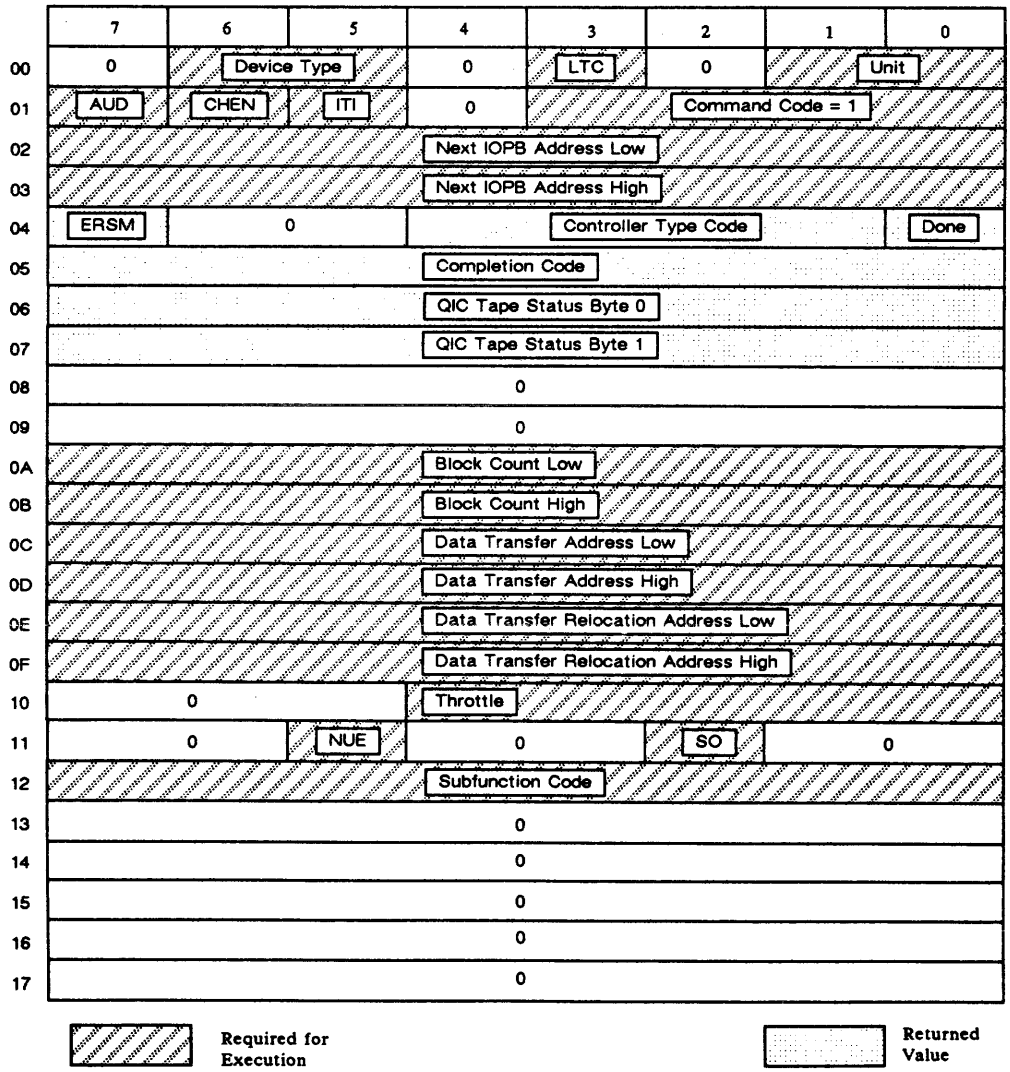
The NOP command verifies that the 43x is operational. The 43x reads the IOPB from system memory, sets *Done*, and posts a completion code in Controller Status Bytes 0 and 1.



5.2 Write Data (Command Code 1)

The Write command transfers blocks of data from the memory buffer, pointed to by the IOPB data address and relocation words, to the tape.

The 43x aborts the Write command if the tape is write-protected, the drive is off-line, or software specifies an illegal subfunction. The 43x DMAs a maximum of one block (512 bytes) to its on-board buffer before starting the drive. Then it transfers the entire buffer to the tape drive and decrements the block count to zero.



5.2.1 Completing a Transfer

When the block count reaches zero, the 43x waits for a *drive not busy* status, and checks the EOM (early warning hole detected) and error status. The 43x updates Tape Status Bytes 1 and 2 after transferring all the data, and generates an interrupt, if enabled. The 43x sets CRDY after completing the chain.

When the 43x detects EOM, system software should write an end of volume record and rewind the tape. The 43x does not prevent writing past EOM, which remains set as long as the tape is positioned beyond that mark. A Read Drive Status command does not clear EOM. The amount of data allowed after EOM sets is drive-dependent; see your drive manufacturer's manual for additional information.

If AUD is set, the 43x updates the block count, Controller Status bytes, Tape Status Bytes 1 and 2, Data Address, and Data Relocation bytes.

5.2.2 Write Command Error Handling

The 43x, by nature of the QIC-02 interface, automatically retries a write until it clears an error or exhausts the retry count (drive-dependent). Exhausting the retry count is a fatal error and halts IOPB processing.

5.2.3 Write Data Command Subfunction Codes

All 43x tape subfunction codes are either standard or optional QIC-02 commands. These command descriptions are taken from the QIC-02, Revision D, standard. In certain cases, tape drive manufacturers may further define commands and still comply with the standard. Consult the tape drive manufacturer's manual for your specific drive.

5.2.3 Write Data Command Subfunction Codes (continued)

Code	Description
40	**Write:** A Write command following cartridge insertion, reset, or a Position to BOT command, begins recording at BOT; otherwise, recording begins at the current tape position.
41	**Write Without Underruns:** This Write command has the drive continue tape movement when a buffer underrun (no data available from the 43x) occurs. This feature keeps the tape streaming. The drive proceeds by writing an elongated preamble and/or redundant blocks until it reaches the end of track or data becomes available.

5.2.4 Write Command Followed By A Position To BOT

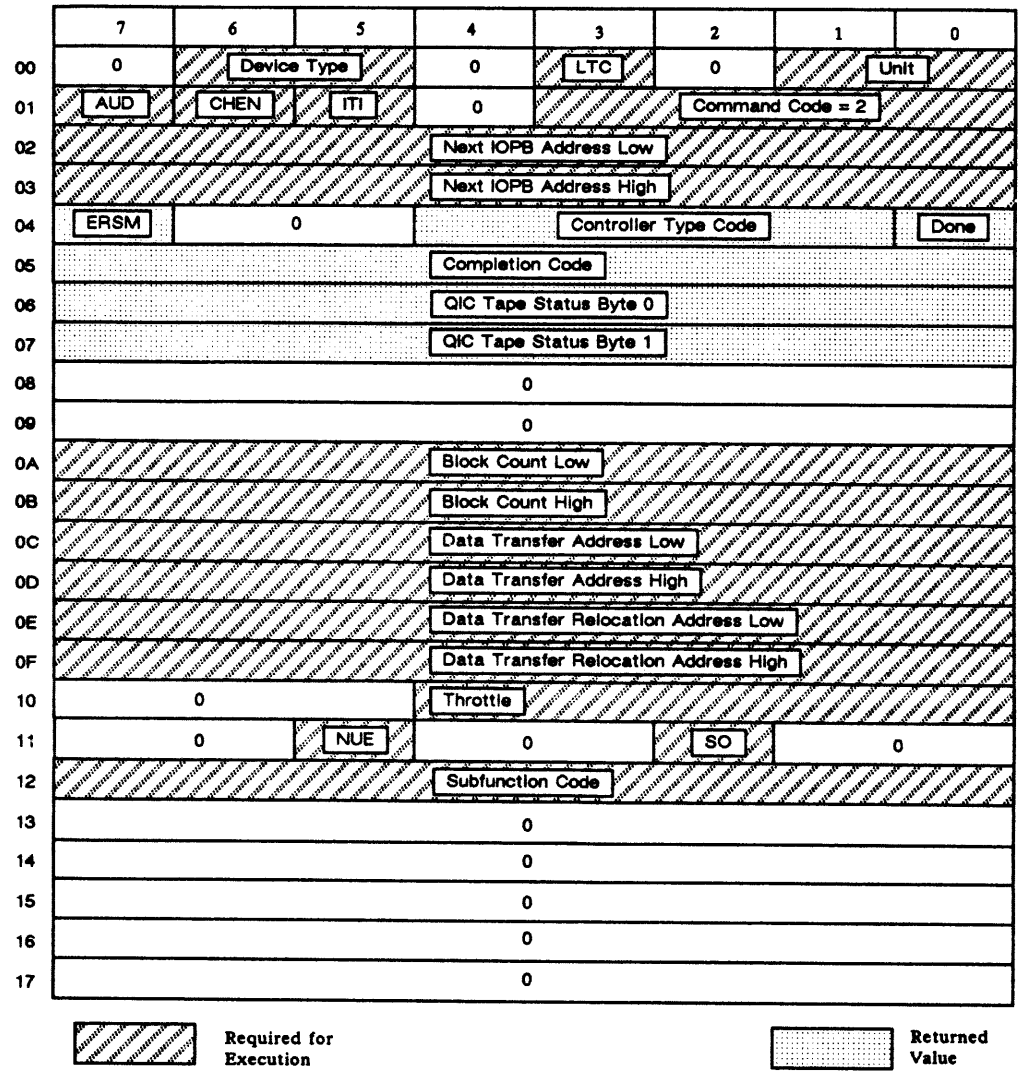
If any command other than another Write or Write File Mark follows a Write command, the QIC-02 formatter automatically writes a file mark on the tape. This ensures that recorded data always ends with a file mark. Never rewind the tape without marking the end with at least one file mark, preferably two. By convention, two consecutive file marks indicate the end of data on tape.

5.2.5 Ensuring That Data Gets to Tape

Since the QIC-02 interface has a buffer, the 43x transfers data to the tape drive and signals system software when it finishes. Some time later, the tape drive actually empties its buffer to tape. Read Drive Status and Write File Mark commands verify that your data reached the tape. The 43x waits for the drive to empty its buffer before returning *Done*.

5.3 Read Data (Command Code 2)

The Read command transfers data from the tape to system memory. The 43x reads from BOT following a cartridge insertion or reset; otherwise, it reads from the current tape position. The 43x reads the first block of data before initiating a DMA to memory.



5.3 Read Data (Command Code 2) (continued)

The 43x aborts the Read command if the drive is off-line or software specifies an illegal subfunction. Most tape formatters organize the data into 512-byte blocks on the tape using the QIC-24 format. If the 43x detects EOM, limiting further reads avoids reaching the physical end of tape.

The 43x does not read past data if it detects a file mark; it treats a file mark as a separate record, but does not transfer data when it detects one. On a subsequent read, the 43x passes the file mark and starts reading a data block, if it exists.

5.3.1 Read Command Error Handling

The tape drive automatically retries a read until it clears the error or exhausts the retry count (drive-dependent). Exhausting the retry count is a fatal error that halts IOPB processing.

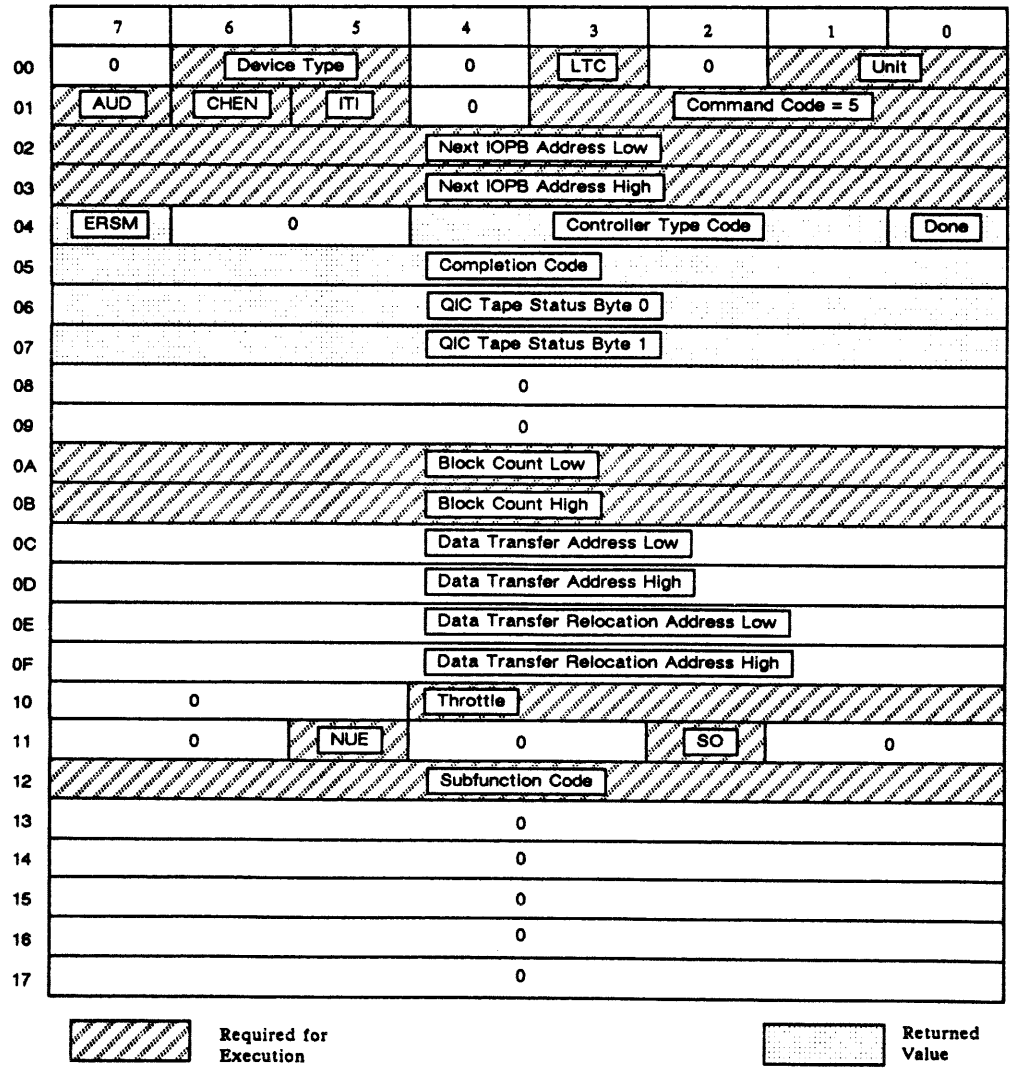
5.3.2 Read Data Command Subfunction Code

Code	Description
80	**Read:** The drive continues reading if a Read command is issued and accepted. A Read command following cartridge insertion, Position to BOT, or Reset, begins at BOT; otherwise, the read begins at the current tape position.

5.4 Position (Command Code 5)

The Position command moves the tape to the requested position, in the requested direction, without transferring data. The 43x may set status bits in TSTAT0 and TSTAT1 as a result of this motion; always check TSTAT0 and TSTAT1 after a Position command. The 43x takes relatively long periods of time to complete many of these commands due to the amount of tape motion required. A 450-foot long tape moving at 90 IPS takes 60 seconds to position from BOM to EOT on one track. A 9-track tape drive takes 540 seconds to position from BOM on Track 1 to EOM on Track 9. The 43x aborts the Position command if the drive is off-line or software specifies an illegal subfunction code.

Some of the QIC-02 Position subfunctions are optional and may vary with each drive manufacturer. The 43x aborts an optional command with an *illegal command sequence* error if the drive does not support it.

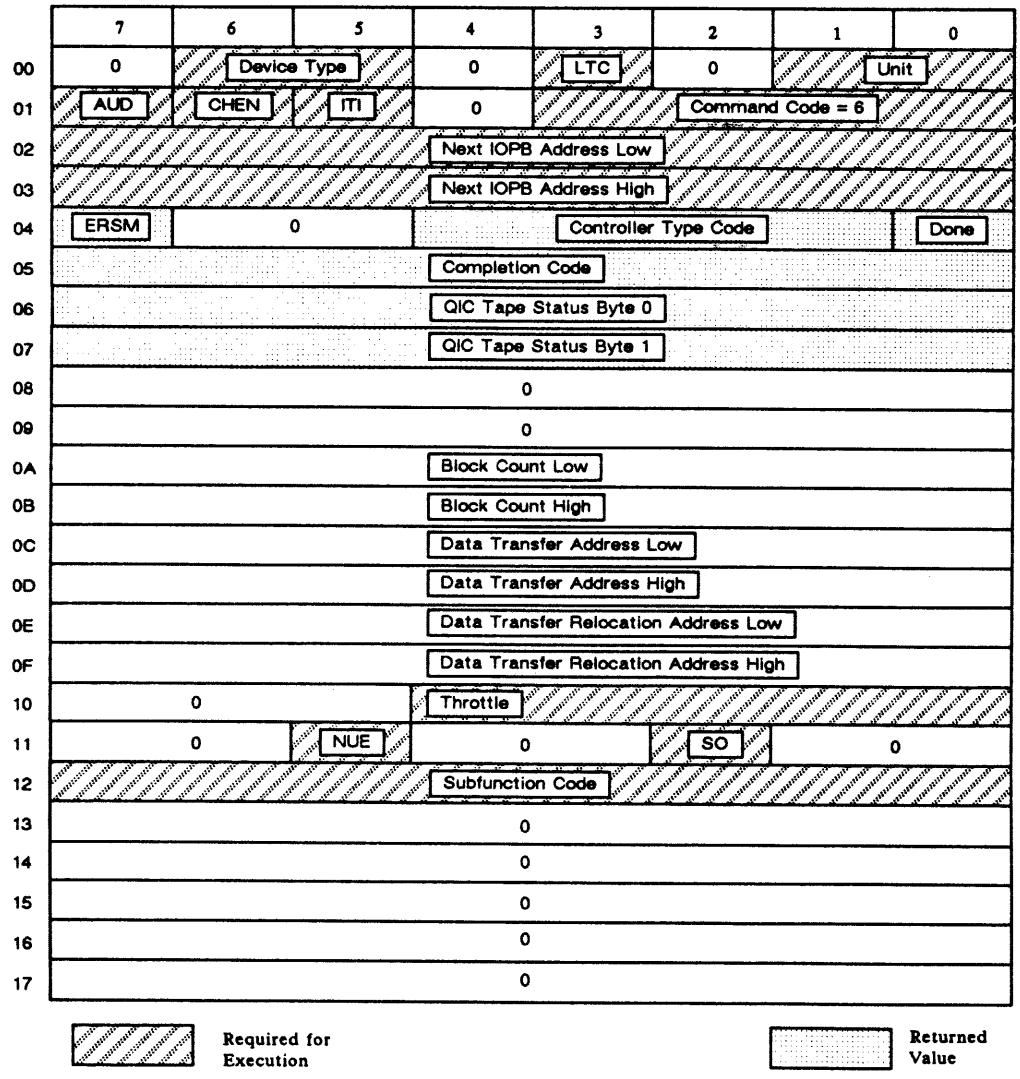


5.4.1 Position Command Subfunction Codes

Code	Description
21	**BOT:** The 43x initiates BOT as soon as the drive is ready and immediately posts *Done* in the IOPB. The drive rewinds the tape, selects Track 1, and sets *drive ready*. Due to the time involved in a rewind, system software should issue a Read Drive Status and determine if the tape is at BOT (BOM in TSTAT1 is set). The 43x completes a Read Drive Status when the drive reaches BOM. If the BOT was preceded by a write, the QIC-02 formatter automatically writes a file mark before rewinding the tape, ensuring that all tapes have a file mark at the end of their recorded data.
22	**Erase:** Completely erases the tape in the selected drive; it also fulfills the requirements of initialization. The Erase command: • Rewinds the tape to BOT. • Activates the erase head and moves to EOT. • Deactivates the erase head and rewinds the tape to BOT.
24	**Initialization:** Rewinds the tape to BOT, then to EOT, and back to BOT. This sequence tensions the tape in the cartridge for improved data reliability and recovery. The 43x does not complete the IOPB until the tape is retensioned; it takes the drive more than 80 seconds to complete initialization.
25	**Select Auto-cartridge Initialization:** The drive executes a cartridge initialization with each new cartridge insertion (taking more than 80 seconds to complete) until the resetting the drive or truning off the power. The 43x completes this command as soon as it sends it to drive.
80	**Space Forward:** Moves the tape forward by the number of blocks specified in the IOPB block count. No data transfers to the 43x. If the 43x detects a file mark, it returns the count of the blocks not spaced in the IOPB and tape movement ceases. If the tape reaches EOM, the 43x sets EOM in TSTAT0; if it reaches a file mark, the 43x sets FIL. Checking for both of these conditions avoids running off the end of tape.
A0	**Read File Mark:** Moves the tape to the next file mark; the 43x sets FIL. A Read File Mark following cartridge insertion, Position to BOT, or Reset, begins reading at BOT; otherwise, reading begins at the current tape position. If the tape reaches EOM, the 43x sets EOM in TSTAT0. Checking for this condition avoids running off the end of tape.

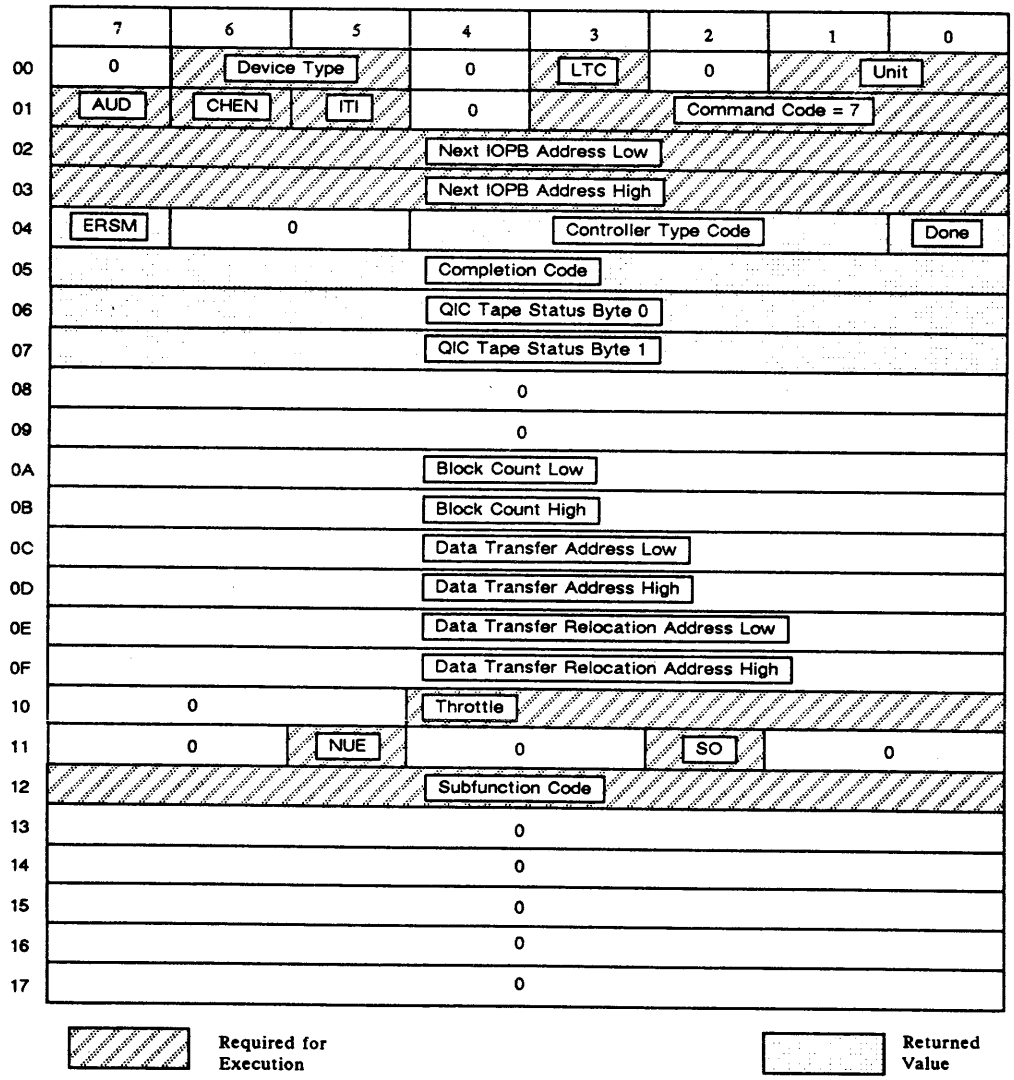
5.5 Drive Reset (Command Code 6)

The Drive Reset command clears the drive's internal registers and sets them to a known electronic state. Issue a Drive Reset only if you suspect a runaway tape condition or to initiate the tape. Tape position after the reset is unknown: the next command requiring tape motion positions the drive to BOM. The BOM status is invalid until the drive reaches BOM. Executing a Position to BOT after a Drive Reset repositions the tape to BOM; system software must specify a subfunction code of zero for this command.



5.6 Write File Mark (Command Code 7)

The Write File Mark command writes a file mark on the tape at the current position, flagging the beginning or end of a set of logical data. Two consecutive file marks usually indicate the logical end of data on the tape. The QIC-02 file mark has the same format as a data block, except a unique code is written into the 512-byte data area.



5.6 Write File Mark (Command Code 7) (continued)

File marks allow software to record many files and headers on one tape cartridge. After writing the tape, software can locate a particular file with a Read File Mark command, which skips to the next file on the tape. Each Write File Mark command writes a single file mark.

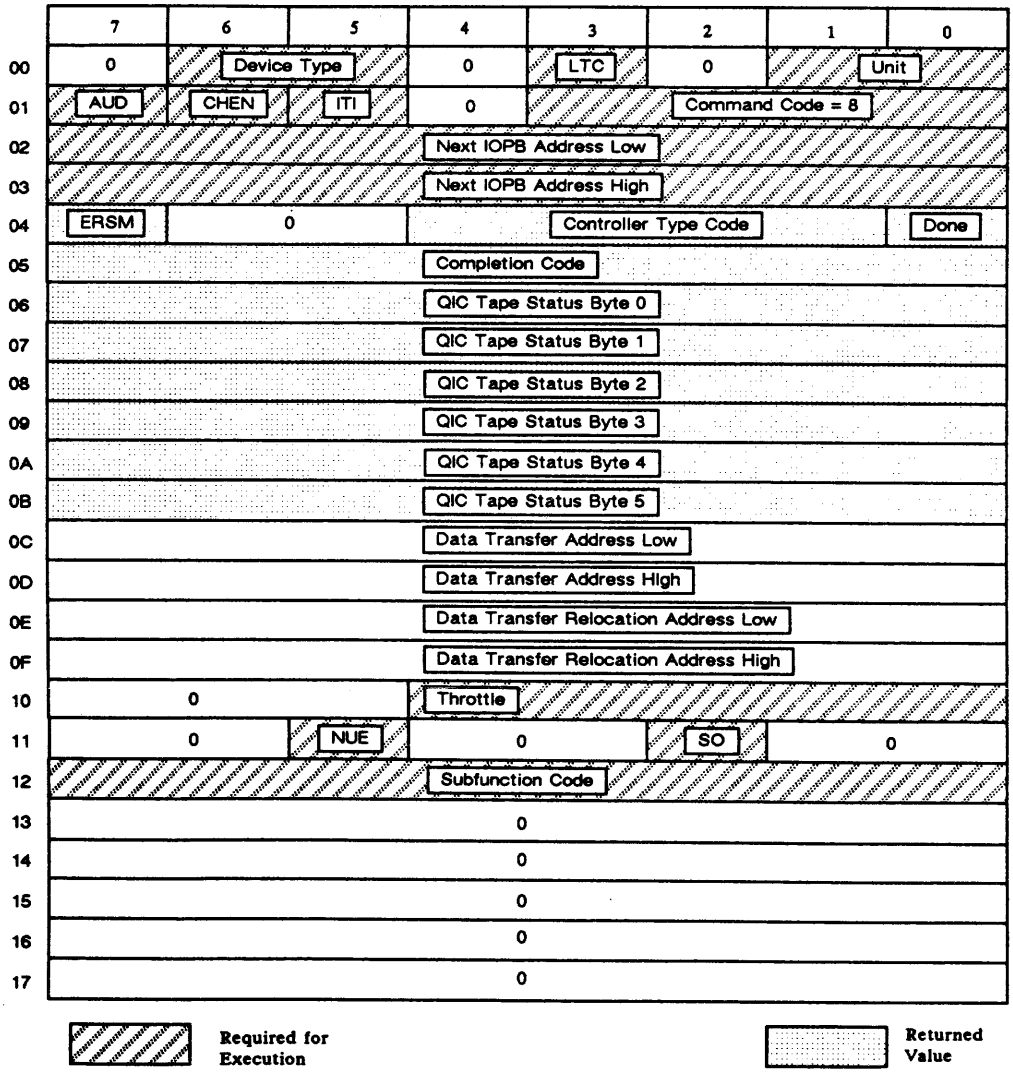
The 43x treats a file mark like a separate record on tape; when it detects a file mark, it sets FIL and does not transfer data. The 43x detects file marks during Read Data, Read File Mark, and Space commands.

5.6.1 Write File Mark Command Subfunction Code

Code	Description
60	**Write File Mark:** Writes a file mark on the tape in the selected drive. A Write File Mark following cartridge insertion, Position to BOT, or Reset, begins recording at BOT. Otherwise, recording begins at the current tape position.

5.7 Read Drive Status (Command Code 8)

Read Drive Status selects the drive and returns its status in TSTAT0 through TSTAT5. The 43x updates CSTAT0 and CSTAT1. System software can use this command to determine if a drive is ready for a particular command. Read Drive Status does not induce any tape motion or transfer data, but can monitor a tape already in motion from a BOT command. *The Maintenance command provides additional status information (see Section 5.8).*



5.7.1 Tape Status Bytes 0 and 1 (TSTAT0 and TSTAT1)

The 43x sets TSTAT0 and TSTAT1 to their appropriate values, depending on the selected drive's status.

5.7.2 Tape Status Bytes 2 and 3 (TSTAT2 and TSTAT3)

During a Read Drive Status command, Status Bytes 2 and 3 display QIC-02 status information reflecting the data error count. TSTAT2 is the most significant half of the data error counter; TSTAT3 is the least significant half. These bytes compile the number of blocks rewritten during a write or the number of soft read errors during a read.

5.7.3 Tape Status Bytes 4 and 5 (TSTAT4 and TSTAT5)

During a Read Drive Status command, Status Bytes 4 and 5 display QIC-02 status information reflecting the underrun count. TSTAT4 is the most significant half of the underrun counter; TSTAT5 is the least significant half. These bytes compile how many times the 43x interrupts streaming because of failure to maintain the minimum throughput rate.

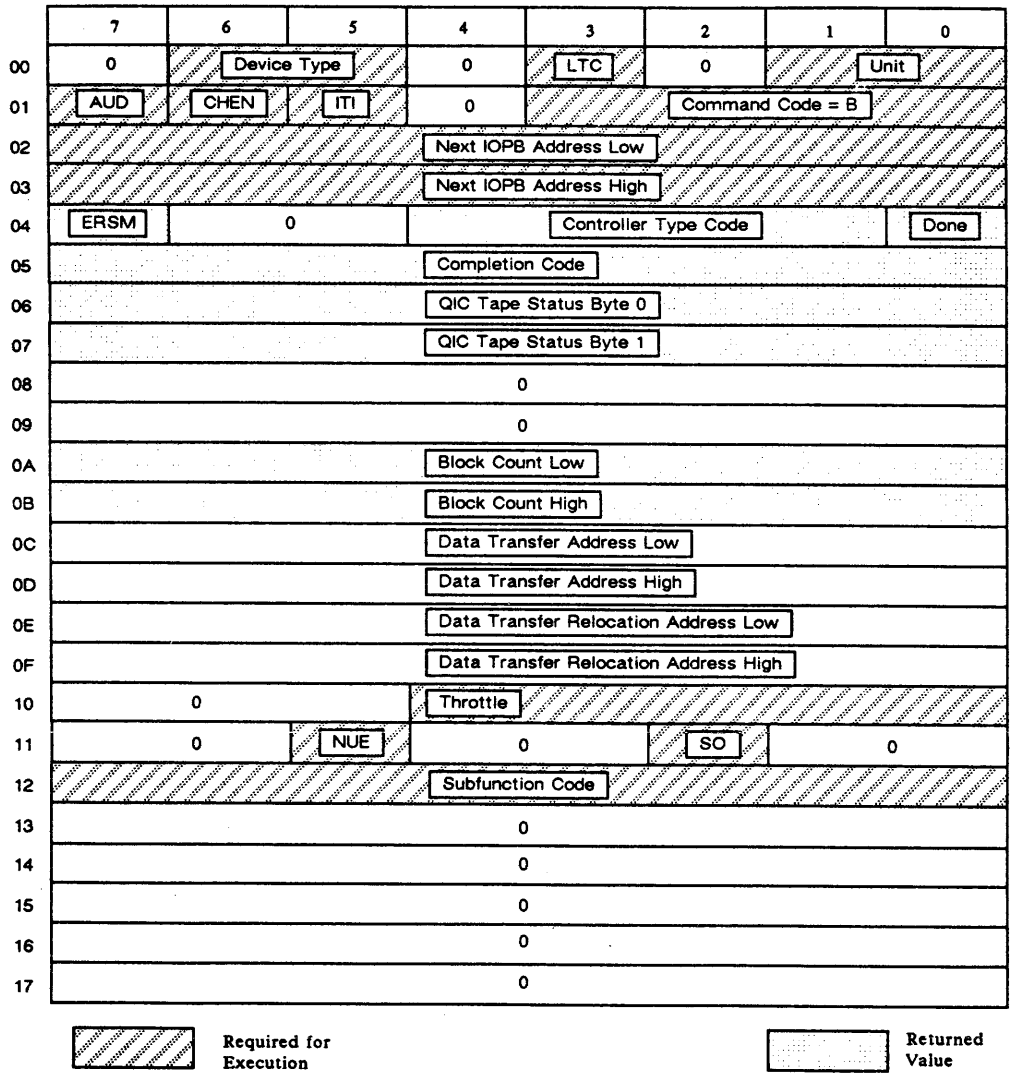
> *The 43x clears the data error counter (TSTAT2 and TSTAT3) and the underrun counter (TSTAT4 and TSTAT5) after a Drive Reset or Read Drive Status command.*

5.7.4 Read Drive Status Command Subfunction Code

Code	Description
C0	**Read Status:** The drive transfers the six standard status bytes (TSTAT0 through TSTAT5) to the 43x; the 43x then transfers these bytes to the appropriate bytes in the IOPB.

5.8 Maintenance (Command Code B)

The Maintenance command executes special IOPBs that cause information transfers between the system and the drive, but which cannot be handled like Read/Write commands. It also initiates self test operations in the drive. *This optional command is drive-dependent.*



5.8.1 Maintenance Command Subfunction Code

Code	Description
C4	**Read Extended Status 2:** The drive transfers the following status bytes to TSTAT0 through TSTAT5.

Table 5-1. Read Extended Status 2

Byte	Description	
TSTAT0	Current Read File	MSB
TSTAT1	Current Read File	LSB
TSTAT2	Current Write File	MSB
TSTAT3	Current Write File	LSB
TSTAT4	Diagnostic Error Code	
TSTAT5	Track Number	

Section 6:
Programming Procedures

Section 6: Programming Procedures

6.0 Introduction

This section describes programming procedures for the 43x.

6.1 Individual IOPB Processing

The 43x starts processing an IOPB when the *Go* bit is set. First, the 43x uses the Address and Relocation Registers to address Multibus memory and read the IOPB. Next, it examines the command, and takes the appropriate action.

For disk drive commands requiring an implied seek, the 43x checks the disk cylinder, head, and sector address, and confirms that they are less than the maximums set by a previous Set Drive Parameters command. The 43x transfers data when the drive completes its seek. For Winchester disks, the 43x transfers data, crossing sector and head boundaries, and executes implied seeks to cross cylinder boundaries. For floppy disks, the 43x transfers data, crossing sector boundaries and, depending on the value of the multitrack option (MT), executes implied seeks to cross cylinder boundaries, and selects the second head. The 43x completes the command when it transfers the required number of sectors.

The 43x considers a tape drive Position to BOT (rewind) command complete when the drive starts moving the tape. The 43x can process additional disk commands while the tape rewinds. The 43x does not complete any other tape commands in the chain until the tape reaches BOT and is ready.

After the 43x completes the command, it updates the IOPB, sets *Done*, and generates an interrupt, if enabled. The 43x is ready for another operation after the operating system processes the interrupt, or, if interrupts are disabled, when it sets CRDY in the CSR. If an error occurs, the 43x updates the necessary bytes.

6.1 Individual IOPB Processing (continued)

The programming sequence is:

- **Set up the IOPB**

System software should allocate a 24-byte segment of memory for the IOPB; the IOPB must not straddle a 64K-byte memory boundary. Set the various IOPB parameters, as required, to perform a function (see Section 3).

- **Point the 43x to the IOPB**

Write the IOPB address into the 43x IOPB Address and Relocation Registers.

- **Set GO**

Set the *Go* bit in the CCR. The 43x clears CRDY in the CSR. CRDY remains clear until the 43x completes the command or detects a hard error.

- **Command Processing**

The 43x starts processing the IOPB after *Go* is set in the CSR. The 43x uses the Address and Relocation Registers to address Multibus memory and read the IOPB. Then it executes the function, updates the IOPB status bytes, interrupts, and sets CRDY.

The 43x posts a completion code in CSTAT1. A code of 00 indicates successful completion; any other code indicates that an error occurred (see Section 6.3).

- **Check for Errors**

If an error occurs, the 43x posts a completion code, and sets ERSM in the errored IOPB. The CSR and CSTAT0 reflect the *completion* status.

For disk and tape drives, determine if DERR is set: possibly, the 43x did not update CSTAT0. If DERR is clear, determine if ERR is set. If ERR is clear, the 43x successfully completed the disk command. For tape commands, also check ERSM.

6.2 Command-chaining

Command-chaining enables rapid queueing and processing of multiple IOPBs. The IOPB Address and Relocation Registers point to the first IOPB in the chain. The Next IOPB address pointers in each IOPB are the links in the IOPB chain. The 43x stops processing a chain after either completing all the IOPBs or detecting a hard error.

Each IOPB has a field pointing to its successor. CHEN must be set in the Command byte so the 43x can follow the link to the next IOPB. The 43x is considered busy when it is processing an IOPB chain. System software must not add or remove IOPBs from the chain without executing the attention protocol; this ensures that all IOPBs are in good order. When AUD is set, the 43x updates the IOPB in memory, whether or not an error occurs. By default, the 43x always updates the IOPB on an error, regardless of AUD's setting. For diagnostic purposes, setting NUE disables this default.

The 43x can execute overlap operations during chained sequences. The 43x scans the IOPB chain for requests for non-busy disk and tape drives each time it starts, or after each *Attention Request*. Since tape and floppy drives share the same buffer and data path, only one tape drive, or one floppy drive, can be busy at a time. The 43x analyzes the first unprocessed request for a non-busy device and executes the command.

If the device is a disk, and the request is a seek, read, or write, the 43x initiates a seek, sending the access mechanism to the correct cylinder. If overlap seeking is enabled, the 43x services the disk drive that reaches the desired cylinder first. The 43x repeats this procedure until it completes the chain. The 43x may not complete the IOPBs in their chained order. Setting SO in the Function Modification byte forces the 43x to complete an IOPB chain in sequential order.

> *Floppy drives, and some Winchester ST506/412 drives, do not support overlap seeking.*

The 43x may execute data transfers simultaneously between a Winchester disk and system memory, and a tape or floppy disk and system memory. This feature allows system software to stream the tape to or from the disk. Interspersing tape and floppy disk commands causes streaming to fail.

6.2 Command-chaining (continued)

Setting ITI in an IOPB directs the 43x to interrupt after completing the IOPB. Setting CLRI in the CCR acknowledges an interrupt. While executing a chain, do not clear IPND, AACK, ERR, or DERR with a *Controller Reset;* drive faults, misposition errors, or runaway tape conditions can occur.

6.2.1 The Chain

Each IOPB has a field (NIOPBL and NIOPBH) pointing to the next IOPB in the chain. The 43x does not look at this chain pointer unless CHEN is set; it uses the IOPB Relocation Registers to relocate the Next IOPB Address bytes. All IOPBs in a chain must be located within the same 64K-byte memory block starting at the base address in the IOPB Relocation Register. CHEN must be set in all but the last IOPB in the chain.

6.2.2 Executing the Chain

The 43x is considered busy when it starts processing an IOPB chain. System software must not add or remove IOPBs from the chain without executing the attention protocol. This protocol ensures that all IOPBs are in good order. System software can take advantage of the overlap command feature by chaining multiple IOPBs. Set IAA, IEC, and BWM at the same time as *Go*.

The 43x remains busy until it completes the chain, or a hard error occurs. Clearing AREQ causes the 43x to rescan the IOPB chain after it completes the current IOPB.

6.2.3 Completing IOPBs

After the 43x completes each IOPB, it updates the status bytes, sets *Done*, and returns a completion code. If AUD is set, the 43x updates all meaningful IOPB fields after completing a command. If IEC is set, the 43x interrupts after completing the last IOPB in the chain. If ITI is set, the 43x interrupts after completing each IOPB. If IAA is set, the 43x generates an interrupt when it sets AACK. Setting CLRI in the CCR clears an interrupt. While chaining, do not clear IPND, ERR, or DERR with a *Controller Reset*, as chaining stops.

6.2.4 Chain Interrupts

The 43x stacks up to 16 interrupts. It generates interrupts if ITI is set in the completed IOPB, at the end of an IOPB chain if IEC is set in the CCR, and after setting AACK if IAA is set in the CCR.

6.2.5 The Attention Protocol

The 43x uses two bits for the attention protocol: *Attention Request* (AREQ) in the CCR, and *Attention Acknowledge* (AACK) in the CSR. System software sets AREQ when it wishes to add and/or remove IOPBs from the chain. The 43x sets AACK and allows software to manipulate the chain. The 43x interrupts if IAA is set. Setting CLRI clears this interrupt.

After the 43x sets AACK, system software can remove completed IOPBs and/or add new IOPBs to the chain. To add IOPBs to the chain, system software must set CHEN and write the new IOPB address (NIOPBL and NIOPBH) into the *last* IOPB in the current chain; it must set the Next Address field to zero, and clear CHEN in the last IOPB in the chain. When system software removes a completed IOPB from a chain, it must clear the preceding IOPBs NIOPB to point to the IOPB following the removed IOPB. Do not touch IOPBs that are queued but not complete, except to modify CHEN and the Next IOPB Address bytes.

System software must clear AREQ after adding and/or removing IOPBs. The 43x then clears AACK, restarts the IOPB chain (if CRDY is clear), and continues processing IOPBs. System software must check for a valid status when reading the Control and Status Register.

The 43x has on-board buffer storage for 15 IOPBs. Software may not add or remove IOPBs from this buffer during the attention protocol, but the 43x continues IOPB processing. The buffer holds completed IOPBs until AREQ and AACK are clear. The 43x then updates all the completed IOPBs in system memory, generates appropriate interrupts, and rescans the chain (see Figure 6–1).

6.2.5 The Attention Protocol (continued)

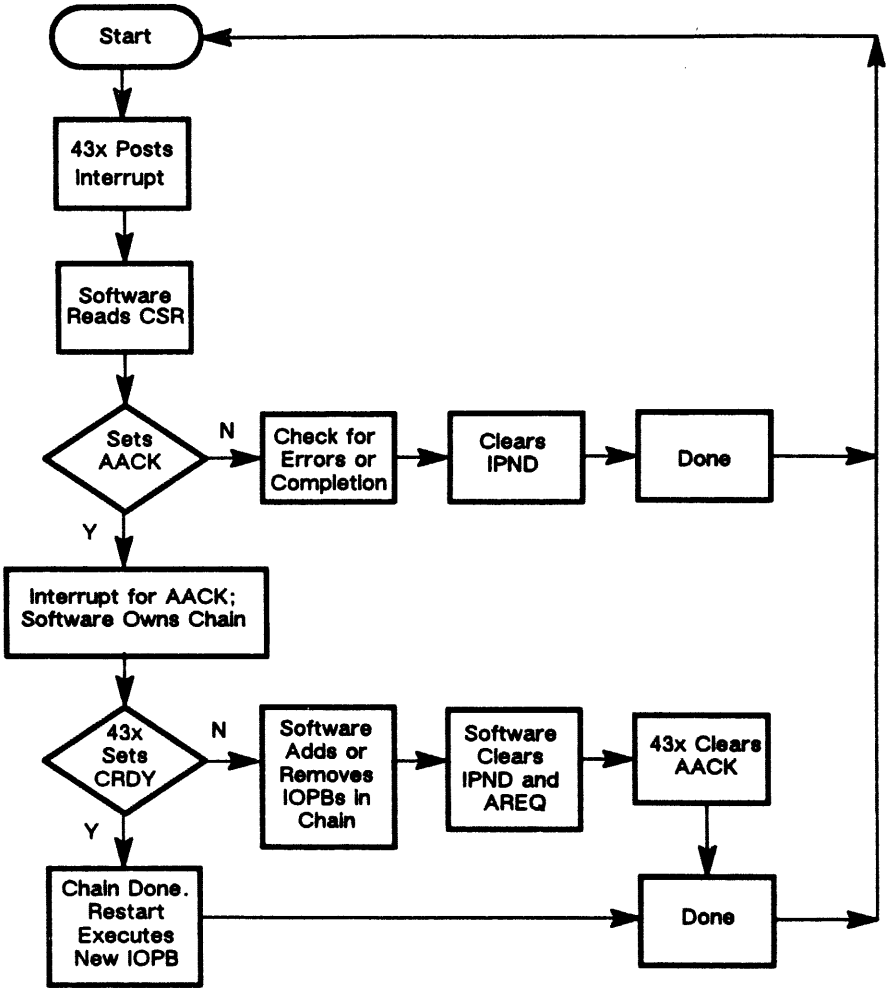


Figure 6-1. Attention Protocol

6.2.6 Using the Attention Protocol

1. (a) Interrupt on Each IOPB causes one interrupt for each completed IOPB.

   (b) Interrupt on the Last IOPB causes one interrupt for each completed IOPB chain.

   > *Since fatal errors stop chain execution, the 43x considers the chain complete even if some IOPBs are not done.*

   (c) Interrupt on AACK causes one interrupt for each AACK.

2. Add all new IOPBs to the last logical IOPB (the one with CHEN clear) of the existing chain. A chain of IOPBs can be built outside of the attention protocol and added to the existing chain; one attention protocol links the two chains together.

3. CRDY does not change state when both AREQ and AACK are set.

4. When adding to the chain, check CRDY after the 43x sets AACK. The 43x executes the additional IOPBs if CRDY is clear. If CRDY is set, it is too late to add IOPBs to the chain. You must restart the 43x by loading the IOPB Address Registers and setting *Go*.

5. Interrupts on AACK: If AACK is set when an interrupt occurs, the interrupt is set for AACK. If AACK is clear, the interrupt is set for IOPB, or end of chain, completion. The next interrupt is for AACK.

6. The 43x will not set AACK if a previous interrupt is pending. You must clear this interrupt before the 43x will set AACK.

7. When clearing an IOPB completion interrupt, and AREQ is set, *do not* clear AREQ.

6.2.7 Completing a Chain

The chain is complete when all of the IOPBs are processed. The 43x completes the chain with an error if any one IOPB has a hard error. In this case, the 43x may not process previous and subsequent IOPBs. The 43x completes all IOPBs in process before posting the error and stopping the chain. Status Bytes 1 and 2 (CSTAT0 and CSTAT1) indicate this condition. The 43x generates an interrupt if IEC is set in the CSR. *The 43x interrupts and sets CRDY at the same time.*

6.3 Completion Codes

The 43x posts a completion code in IOPB Byte 5. A completion code is valid only if *Done* is set. Table 6-1 lists the completion codes. All codes not listed in the table are reserved. The codes are grouped according to their recovery procedure (see Section 6.4).

Table 6-1. Summary of Completion Codes

Code H	Device	Category	Description
00	W,T,F	None	Successful Completion
Non-retryable			
10	W,F	Programming	Illegal Cylinder Address
20	W,F	Programming	Illegal Head Address
30	W,F	Programming	Illegal Sector Address
40	W,T,F	Programming	Busy Conflict
50	W,T,F	Programming	Block/Sector Count Zero (or too large; > 8 MB on FD)
60	W,T,F	Programming	Unimplemented Command
70	T	Programming	Illegal Command Sequence
80	W,T,F	Programming	Illegal Drive Type
90	W,T,F	Programming	Illegal Unit Number
A0	F	Programming	Illegal Bytes/Sector
Soft Errors			
12	W	Media	Soft ECC Corrected
22	W	Media	ECC Error Ignored
32	W	Drive	Auto Seek Retry Recovered
42	W	Media	Read Retry Recovered
52	F	Media	Deleted Data Address Mark
62	F	Bus	Data Late Recovered
72	F	Media	Missing Sync Byte

W = Winchester Disk Drive; T = Tape Drive; F = Floppy Disk Drive

6.3 Completion Codes (continued)

Table 6-1. Summary of Completion Codes (continued)

Code H	Device	Category	Description
Hard Errors/Retry			
14	W,F	Media	Hard Data ECC or CRC Error
24	W,F	Multiple	Header Not Found
34	W,T,F	Drive	Drive Not Ready
44	W,F	Multiple	Operation Timeout
54	W,F	Programming	Slave ACK (Non-existent Memory)
64	W	Drive	Disk Sequencer Error
74	T	Drive	Unexpected File Mark Detected
84	W,F	Drive	PLL Lock Failure
94	W,F	Drive	Write-protect Error
A4	F	Bus	Data Late Detected
Hard Errors: Reset/Retry			
16	W,T,F	Drive	Drive Faulted
26	W,F	Drive	Header Error/Cylinder/Head
56	W	Drive	Header Error
Fatal Errors			
18	W,T,F	Hardware	Self Test 1
28	W,T,F	Hardware	Self Test 2
38	W,T,F	Hardware	Self Test 3
48	W,T,F	Hardware	Self Test 4
58	W,T,F	Hardware	Self Test 5
Miscellaneous Errors			
1A	W	Media	Soft ECC
2A	W	Tape Excp.	Tape Drive Error

W = Winchester Disk Drive; T = Tape Drive; F = Floppy Disk Drive

6.3.1 Completion Code Descriptions

CodeH	Description
00	*Successful Completion:* Not an error; the command is complete. Software may remove the IOPB from the queue.
10	*Illegal Cylinder Address:* System software specified a cylinder address greater than the maximum cylinder number specified in the last Set Drive Parameters command for this drive. Correct the cylinder address and retry the operation.
12	*Soft ECC Corrected:* During a Winchester disk read transfer in ECC Mode 2, the 43x detected and corrected one or more ECC errors.
14	*Hard Data ECC or CRC Error:* During a Read operation, the 43x detected a hard data ECC error (longer than 11 bits) in the data field of a Winchester disk, or a CRC error (of any length) on a floppy disk. Retry the previous read.
16	*Drive Faulted:* The selected drive is faulted. Issue a Drive Reset; if the fault persists, you must intervene.
18	*Self Test 1 Failure:* See Section 4.17.
1A	*Soft ECC Error:* During a Read operation in ECC Mode 0, the 43x detected a soft error, having 11 bits or less, in the data field of the current sector. Software must perform the final correction (see Section 3.1.16, ECM).
20	*Illegal Head Address:* System software specified a head address greater than the maximum head address specified in the last Set Drive Parameters command for this drive. Correct the head address and retry the operation.
22	*ECC Error Ignored:* During a Read operation in ECC Mode 3, the 43x detected an ECC error.

6.3.1 Completion Code Descriptions (continued)

CodeH	Description

24 *Header Not Found:* The 43x cannot find the requested sector; it searches for a match for four disk revolutions to locate the header. The floppy 43x searches for five revolutions before reporting this error if RTRY is set. The 43x verifies the header field of the sector before reading or writing the sector.

26 *Header Error/Head and or Cylinder:* The head or cylinder address did not match while searching for a sector. Check the cylinder or head address and retry the operation.

28 *Self Test 2 Failure:* See Section 4.17.

2A *Tape Exception:* One of the following tape exceptions occurred:

- NDT No Data Detected.
- ILL Illegal Command.
- BNL Bad Block Not Located.
- UDA Recoverable Data Error.
- EOM End of Media.
- USL Unselected Drive.
- CNI Cartridge not in Place.

30 *Illegal Sector Address:* System software specified a sector address greater than the maximum sector number specified in the last Set Drive Parameters command for this drive. Correct the sector address and retry the operation.

32 *Auto Seek Retry Recovered:* The 43x recovers from a *seek* error by retrying the operation. The 43x executes a seek retry by recalibrating and reseeking to the selected cylinder (see Section 3.1.16, RTRY).

34 *Drive Not Ready/Drive Off-line:* The selected drive is not ready, but not faulted. Issue a Drive Reset (Command Code 06H). If the drive does not become ready, check these possible causes:

- Drive not up-to-speed.
- Drive hardware error.
- Bad or improperly connected cable(s).
- No drive with the specified unit number is connected to the 43x.

6.3.1 Completion Code Descriptions (continued)

CodeH	Description
38	*Self Test 3 Failure:* See Section 4.17.
40	*Busy Conflict:* A register write is attempted while the 43x is busy. Only CRST, CLRI, and AREQ have write access while the 43x is busy.
42	*Read Retry Recovered:* The 43x recovers from a *read* error by retrying the operation once.
44	*Operation Timeout:* The 43x did not complete the IOPB within the appropriate timeout period for this command and device. *IOPBs may be queued indefinitely without timing out.*
48	*Self Test 4 Failure:* See Section 4.17.
50	*Sector/Track/Block Count Zero:* System software issued the 43x an IOPB that required a count, but the count was zero, or greater than 8 MB for floppy disk drives. Normal Read, Write, and Format commands require a valid count. Correct the IOPB in error and start the transfer again.
52	*Deleted Data Address Mark Detected:* The 43x detected a deleted data address mark (F8) during a read when WDDM was clear (see Section 3.1.16).
54	*Slave ACK Error (Non-existent Memory):* The memory addressed by the 43x failed to respond within one millisecond. Validate the memory address, or memory itself, and retry the command.
58	*Self Test 5 Failure:* See Section 4.17.
60	*Unimplemented Command:* This error occurs on all reserved commands.
62	*Data Late Recovered:* The 43x recovers from a *data late* error by retrying the operation once.

6.3.1 Completion Code Descriptions (continued)

CodeH	Description
64	*Disk Sequencer Error:* The disk sequencer did not complete its task within the allotted time limit. The 43x cannot send or receive the appropriate signals from the selected drive. Possible causes include: • Drive is not connected. • Improper cabling. • Unformatted drive.
70	*Illegal Command Sequence:* System software issued an illegal command to the 43x. See your drive manufacturer's manual for more information.
72	*Missing Sync Byte:* The 43x detected a missing Sync byte during a Read Full Track command. The 43x does not retry the operation; this error does not stop IOPB chain processing.
74	*Unexpected File Mark Detected:* The 43x detected a file mark before it was expected.
80	*Illegal Drive Type:* Drive Type 00 is reserved.
84	*PLL Lock Failure:* The phase lock loop failed to lock up on the data field preamble within the prescribed time window.
90	*Illegal Unit Number:* Unit Numbers 2 and 3 are illegal for Winchester drives.
94	*Write-protect:* A command that writes the disk (e.g., Write, Format, Write Track Headers) was issued, but the drive is write-protected.
A0	*Illegal Bytes per Sector:* A value other than one 0, 1, 2, or 3 is entered in IOPB Byte D for a floppy disk drive (see Section 4.15.6).
A4	*Data Late Detected:* The floppy disk controller chip (FDC) detects a *data late* condition (i.e., the buffer is full or empty).

6.4 Error Recovery

Certain procedures may recover errors. These procedures vary, depending on the type of error the 43x encounters. The errors in the following subsections are grouped according to the recommended recovery procedure.

6.4.1 Programming Errors 10, 20, 30, 40, 50, 60, 70, 80, 90, A0

These are either programming errors or hard failures. Do not retry the operation (see Section 6.3).

10	Illegal Cylinder Address
20	Illegal Head Address
30	Illegal Sector Address
40	Busy Conflict
50	Sector/Block Count Zero
60	Unimplemented Command
70	Illegal Command Sequence
80	Illegal Drive Type
90	Illegal unit Number
A0	Illegal Bytes Per Sector

6.4.2 Hard Errors 14, 24, 34, 44, 54, 64, 74, 84, 94, A4

Retrying the operation may recover these errors. Execute two retries; if the error persists, it either cannot be recovered or requires manual intervention.

14	Hard Data ECC/CRC
24	Header Not Found
34	Drive Not Ready/Off-line
44	Operation Timeout
54	Slave AACK (Non-existent Memory)
64	Disk Sequencer Error
74	Read File Mark Failure
84	PLL Lock Failure
94	Drive Write-protected
A4	Data Late

6.4.3 Hard Errors 16, 26, 2A

These errors indicate that the drive may be off-cylinder. Issue a Drive Reset, and retry the transfer. Setting ASR in the Mode byte has the 43x automatically retry faulty transfers.

16	Drive Faulted
26	Header Error/Head and/or Cylinder
2A	Tape Exception

6.4.4 Soft Errors 12, 22, 32, 42, 52, 62, 72

These errors indicate that the 43x corrected one or more errors during a transfer, or it detected a deleted data address mark in the data field of a floppy sector. Error Code 52 is more a flag than an error.

12	Soft ECC Corrected/CRC Recovered
22	ECC Error Ignored
32	Auto Seek Retry Recovered
42	Read Retry Recovered
52	Deleted Data Address Mark Detected
62	Data Late Recovered
72	Missed Sync Byte

6.4.5 Miscellaneous Errors

This error indicates that an ECC recoverable error occurred, and Auto-ECC Recovery was not selected on a Winchester disk.

1A	Soft ECC Error

Software may correct this condition as follows:

For a byte-oriented system (e.g., 8080, 8085, 8088, 6800, Z80):

1. Reserve 16-bits of storage for the ECC mask word (two bytes). Initialize them to zero.

6.4.5 Miscellaneous Errors (continued)

2. Get the bit address word from the IOPB and subtract one. Since the bit address always starts at one, this starts the bit count at zero.

3. Shift the stored mask word left using the three least significant bits of the adjusted bit address from Step 2 as a count. These three bits represent the starting bit number within the byte.

4. Divide the bit address by eight by performing three logical shifts to the right. The result is the byte offset into the data where the stored mask word is exclusive-ORed (XOR) with the data. Adding this offset to the start of the bad sector creates a pointer to the first data byte for correction.

5. XOR the data bytes in ascending order with the two mask bytes, using the least significant mask byte first.

For 16-bit word-oriented systems:

1. Reserve 32-bits of storage for ECC mask (two words). Initialize them to zero.

2. Get the ECC bit address from the IOPB and subtract one; this starts the bit count at zero rather than one.

3. Shift the stored address mask bits left using the four low order bits of the adjusted ECC address from Step 2 as a count.

4. Divide the bit address by sixteen by performing four logical shifts to the right. The result is the word offset into the bad sector. Adding this offset to the start of the sector memory address creates a pointer to the first word for correction.

5. XOR two consecutive words in the data with the mask.

6.5 Disk Sector Format

A sector consists of many fields, each with a specific size and purpose. The 43x supports two types of Winchester disks: hard- and soft-sectored. Hard-sectored disks provide an electrical pulse at the beginning of each sector on the disk. Soft-sectored disks record a special bit pattern, called an address mark (AM), that indicates the start of a sector. All floppy disks are soft-sectored.

6.5 Disk Sector Format (continued)

There are gaps between sectors and within sectors that allow for electronic switching times and rotational speed variations in the disks. These gaps are sometimes called preambles, postambles, and splices. Each has a specific purpose. In addition to these gaps, each sector contains a header identifying the sector, the header ECC field, the actual sector data, and the data ECC field. The header records the address of the sector by cylinder, head, and sector number. The header verifies that the 43x finds the requested sector.

The 43x supports logical sectoring. This means the sector number recorded in the header is not necessarily the same as the physical sector position. This feature allows logical sector interleaving, spare sectoring, and skewed index, all of which improve the disk/43x subsystem's throughput.

6.5.1 431 Soft-sectored Winchester Disk Format

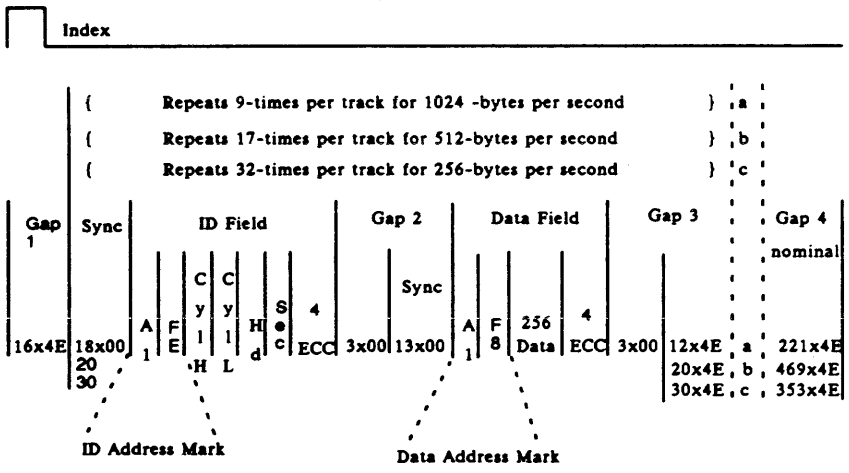


Figure 6–2. 431 Soft-sectored Winchester Disk Format

6.5.2 Winchester Disk Sector Header Format

The sector header is a four-byte field containing a two-byte cylinder number, a one-byte head number, and a one-byte sector number (see Table 6-2).

EEH in all four bytes indicates a bad sector. DDH in all four bytes indicates a spare sector. A four-byte header ECC follows the header field. The 43x detects header errors with the ECC, but never corrects them with it.

Table 6-2. Winchester Disk Header (ID Field) Format

Byte	Description
Byte 0	Cylinder High
Byte 1	Cylinder Low
Byte 2	Head
Byte 3	Sector
Bytes 4-7	ECC

6.5.3 Single Density Floppy Disk Sector Format

The 43x supports four sector lengths in single density mode: 128-, 256-, 512- and 1024-bytes. Gap 3 is different for each sector length. The sector size is encoded in the sector ID field. The address mark for the data field is BF for data and F8 for deleted data (see Figure 6-3). The 43x omits the index field if NIXM is set (see Section 3.1.16).

6.5.3 Single Density Floppy Disk Sector Format (continued)

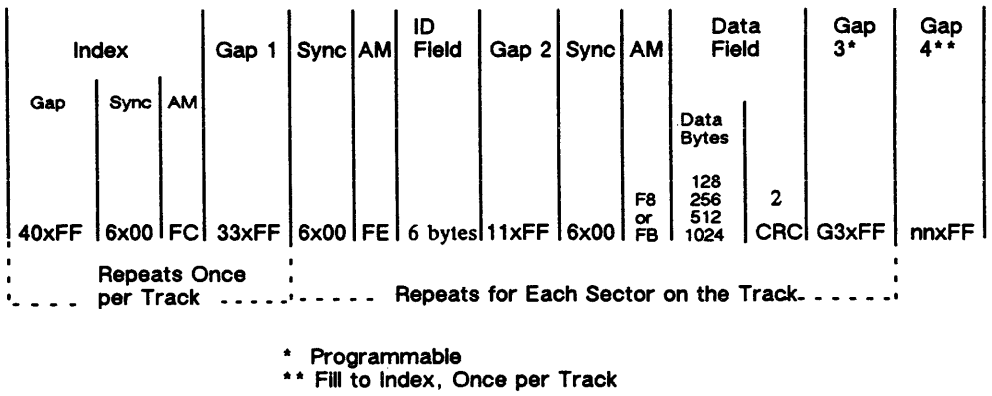


Figure 6–3. Single Density Floppy Disk Sector Format

6.5.4 Double Density Floppy Disk Sector Format

The 43x supports three sector lengths in double density mode: 256-, 512-, and 1024-bytes. Gap 3 is different for each sector length. The sector size is encoded in the sector ID field. The double density format differs from single density format in the bytes written in the gaps and the ID address mark field. The data field address mark is FB for data and F8 for deleted data. The 43x omits the index field if NIXM is set (see Section 3.1.16, Figure 6–4, and Table 6–3).

6.5.4 Double Density Floppy Disk Sector Format (continued)

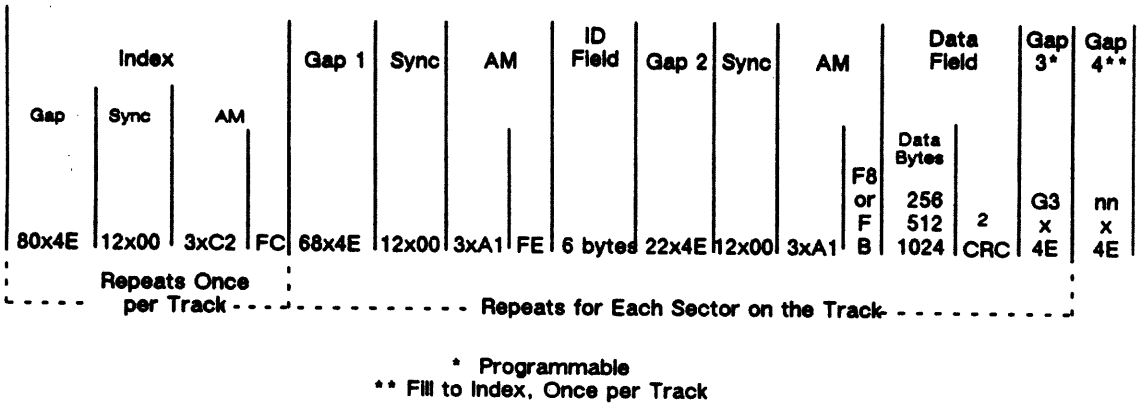


Figure 6–4. Double Density Floppy Disk Sector Format

Table 6–3. Floppy Disk Header (ID Field) Format

Byte	Description
Byte 0	Cylinder Number 90–Max Cylinder)
Byte 1	Head Number (0,1)
Byte 2	Sector Number (1–Max Sector)
Byte 3	Encoded Sector Length (0=128, 1=256, 2=512, and 3=1024)
Byte 4	CRC
Byte 5	CRC

6.6 Formatting

This section describes how to format a disk. The 43x sequencer PROMs define the number of bytes per sector.

6.6.1 Winchester Disk Set Drive Parameters

Set the number of sectors in the drive size parameters equal to the number of physical sectors in an entire track minus one. Do not subtract the number of spare sectors software uses for sector slipping.

6.6.2 Winchester Disk Format

Format the disk one cylinder at a time. Write a data pattern, read it, and verify the data. Use several different patterns when checking for media defects. Build a table in memory of all the media defects as software verifies the disk.

> *Most Winchester disks come with a hard copy list of media defects. Your format routine should make use of this information.*

6.6.3 Winchester Disk Media Defects

Winchester disk drives produce a soft error in about one out of every 10^{10} transfers. A sector is not bad if it fails with a soft error once. Rewrite the pattern and read the sector up to ten times, or until a second error occurs. Sector slipping is not necessary if only one error occurs in every ten transfers. If a second error occurs, add the sector to the bad sector table. Record whether the error is a bad header, hard or soft ECC.

6.6.4 Winchester Disk Reset Drive Size Parameters

Set the drive size parameters equal to the number of desired data sectors. This number should equal the number of physical sectors the drive supports, minus the desired number of spare (slip) sectors, and the runt sector, if it exists.

6.6.5 Winchester Disk Slip Defective Sectors

Using the procedure in Section 6.7, slip the defective sectors and mark them bad. Make sure that no two sectors on a track have the same sector number.

6.6.6 Floppy Disk Format

Set the number of sectors in the drive size parameters equal to the number of sectors desired. Format the disk, specifying the fill characters, and the size of Gap 3 in the IOPB.

6.7 Sector Slipping on Winchester Disks

Sector slipping involves system software marking sectors with media defects as defective using the Write Track Headers command; the 43x uses the next good sector in its place. System software slips all succeeding logical sectors to succeeding physical sectors. The last logical sector uses the spare physical sector. The spare sectors are usually the last sectors on the track. The 43x automatically skips over a sector marked bad. You may keep spare sectors on a separate track or cylinder, but system software must keep them in a table and initiate the seeks to and from the spare cylinder.

6.7.1 Read Track Headers

Software must allocate a buffer in system memory for storing the sector header information during this procedure. The buffer length, in bytes, must be four times the total number of physical sectors on a track; each header is four-bytes long. Issue a Read Track Headers command for the track containing the sector(s) for slipping. The 43x reads all headers on the track; it ignores the max sector value. Manually check the buffer in system memory and verify that the 43x transferred the headers correctly (see Sections 4.10 and 4.11).

6.7.1 Read Track Headers (continued)

> *Xylogics does not recommend using the Read Track Headers command for slipping sectors. You may lose a sector if there is a media defect in the address mark area. We recommend building the header table in system memory, modifying the table for the slipped sectors, and using the Write Track Headers command to write headers back to the disk.*

6.7.2 Recording Bad and Spare Sectors

Determine which sectors are spares, and which are bad. Build a table in memory with two variables: the physical sector number from index and the status of that sector (good, bad, or spare).

Table 6-4 reflects disk Cylinder 142H, Head 5. Physical sectors 0-4 and 6-14 are good, physical sector 5 is bad, and physical sector 15 is a spare. This results in 15 good logical sectors, numbered 0 through 14.

Table 6-4. Logical to Physical Mapping

Table In Memory H				Physical Sector Number	Status	Logical Sector Number After Slipping
CYLH	CYLL	HEAD	SECT			
01	42	05	00	0	Good	0
01	42	05	01	1	Good	1
01	42	05	02	2	Good	2
01	42	05	03	3	Good	3
01	42	05	04	4	Good	4
EE	EE	EE	EE	5	Bad	-
01	42	05	05	6	Good	5
:	:	:	:	:	:	:
01	42	05	0E	14	Good	13
DD	DD	DD	DD	15	Spare/Good	14

6.7.3 Spare Sector Available

Determine if enough spare sectors are available. There must be a spare available for every sector you are slipping.

6.7.4 Determining the Physical Sector Number

To determine the physical sector number: calculate the physical sector number in relation to index; then add it to the number of bad sectors between index and the sector you are slipping.

The physical sector number equals the logical sector number if the interleave factor is 1:1, and there are no defective sectors. Adjust the physical sector number by the interleave factor if the sectors are not contiguous.

For example, upon reading a track interleaved 2:1, the logical sectors are arranged as follows:

0, 8, 1, 9, 2, 10, 3, 11, 4, 12, 5, 13, 6, 14, 7.

Table 6–4 shows physical sectors 0 through 4 good, 5 bad, and 6 through 15 good. The sixth sector after index is bad. There are no defective sectors between index and the sector you are slipping. The physical sector for slipping is the sixth physical sector from index, or logical sector 10. The new sector organization is:

0, 8, 1, 9, 2, EE, 10, 3, 11, 4, 12, 5, 13, 6, 14, 7, 15.

6.7.5 Slipping Sectors

Using Table 6–4, and the vector generated in Section 6.6.4, modify the buffer for the Write Track Headers command. Set up the header for the first sector at the beginning of the buffer. The following procedure modifies the buffer:

6.7.5 Slipping Sectors (continued)

1. Get the physical sector number you are modifying.

2. Multiply this number by four, and add it to the starting buffer address to determine where that sector's header begins.

3. Determine if this sector is good or bad. If the sector is bad, the four Header bytes are EEH, EEH, EEH, EEH. If the sector is good:

   - The first byte is the most significant byte (MSB) of the cylinder number.
   - The second byte is the least significant byte (LSB) of the cylinder number.
   - The third byte is the head number.
   - The fourth byte is the new sector number (see Table 6–4).

4. Determine the new logical sector number using:

   - The interleave algorithm.
   - The physical sector number.
   - The number of bad sectors encountered so far.

   Take the physical sector number and subtract the number of bad sectors found between it and index. Use this value to calculate the new logical sector number. Place this number into the buffer sector number field.

5. Continue setting up the buffer for each physical sector on the track. Use the procedure outlined above to determine how to set up each sector.

> *The physical locations of bad sectors must not move in relation to index. Media defects do not move when slipping sectors. Any physical sector marked bad must remain bad.*

6.7.6 Write Track Headers

You can now write the modified headers to the disk, thus reformatting the track with slipped sectors. Once reformatted, the defective sectors are invisible to the operating system through normal Read and Write commands. The 43x accesses defective sectors, as well as good sectors, with Read/Write Data and ECC commands.

6.7.7 Sector Slip With Live Data

The following procedure allows sector slipping without losing live data on the disk. This procedure requires a full track buffer; implement it with a stand-alone program.

1. Allocate a full track buffer in memory, and read a track into memory. Use ECC Mode 2, which corrects the bad data, if possible. If a full track buffer is not available in memory, allocate disk space, and store the data in that space.

2. Using the sector slip procedure, slip the sector with the media defect.

3. Write the data from the buffer back onto the disk. The 43x compensates for slipped sectors.

6.8 Floppy Disk Initialization

Set the sector size in the 43x before reading or writing a floppy disk. A Read Next Header command helps determine the sector size. The fourth byte in the data transferred from the header gives the value of n(BPS). The 43x uses n in Byte D of the Set Drive Size IOPB.

Section 7:
Performance Considerations

Section 7: Performance Considerations

7.0 Introduction

This section suggests how to get the best possible performance from the 43x for your particular application. It considers the various tradeoffs, their advantages and disadvantages.

7.1 Streaming

The key to an efficient system is matching the dissimilar disk and tape transfer rates. One solution to this problem includes using appropriate multiple buffer schemes. The maximum disk latency a streaming mode operation must support determines the buffer size. This buffering scheme arranges several buffers as a circular queue. Memory buffers and the controller's on-board buffer provide a steady data flow to the streaming tape. This technique avoids stopping for new data. Do not use the floppy disk drive in streaming mode.

The 43x is capable of running disk and tape at the same time. Due to the start/stop time of streaming drives, it is very important to keep the tape drive streaming. The following guidelines ensure successful tape drive streaming.

1. Efficient streaming necessitates multiple IOPB processing. Software must set up an IOPB chain in system memory.

2. Allocate a large buffer in system memory during back-up operations so the disk can be well ahead of the tape, absorbing seek times. Large buffers also allow the 43x to start the DMA for the next tape operation before completing the current tape IOPB.

3. For file structured back-up, rewriting the data so it is contiguous avoids tape drive repositioning due to excessive seek times or gather reads. You may do this on spare cylinders if they are not allocated or in system memory.

4. Instructing each disk and tape IOPB to transfer a large number of sectors or blocks cuts down excessive IOPB processing time for both system software and the 43x.

7.1 Streaming (continued)

Even when you follow these guidelines, there may be times when streaming is interrupted. General causes include:

1. CRC or ECC errors causing the tape to reposition. If software allocates large system memory buffers it should set one of the Auto-correct ECC modes, ensuring a soft error does not stop IOPB execution.

2. Operation of slow DMA devices on the bus may make streaming impossible. Excessive file processing may also abort streaming.

7.2 Throttle

From the controller's viewpoint, the throttle value should be as high as possible so it never misses a disk revolution or has to reposition tape due to a full or empty buffer. You may have some other real-time application that needs to access the bus periodically. The bus use formula is:

[XACK Response Time + XXX ns (43x overhead)] x Number of DMA Cycles (words) + XXX ns (busack/req) = Bus Use (microseconds).

In these applications:

- Determine the maximum time the 43x can be bus master.

- Determine your memory response time, add XXX ns, and divide this value into the allowable 43x bus master time. This number is the maximum throttle value. For smaller throttles, reduce this number to allow for accessing and releasing the bus.

- Pick the number closest to the 43x throttle value without going over the actual amount.

7.2.1 High Throttle Advantage

- Maximum bus throughput with minimum bus overhead.

7.2.2 High Throttle Disadvantages

- Tendency to *hog* the bus; time critical devices fail.
- Other DMA units may not get enough bus time.

7.3 Word or Byte Mode

Word mode is more efficient than byte mode on the bus. Using word mode effectively doubles the 43x throughput.

7.3.1 Word Mode Advantages

- Increased throughput with less bus use.
- Helps DMA keep up with the disk and tape.

7.3.2 Word Mode Disadvantage

- Works only on word-oriented memory.

7.3.3 Word Mode on Odd Boundary

When a word mode transfer begins on an odd address, the 43x defaults to byte mode. The disadvantage is that the overall DMA throughput is one-half that of word mode. This slower DMA requires more time during a transfer and reduces the margin for keeping up with the disk and tape.

7.4 Interleaving

Interleaving Winchester or floppy disks may increase throughput on either a fully loaded system or one with a slow operating system response time. It effectively cuts the disk speed in half for 2:1, or a third for 3:1 interleaving, etc., removing the chance of lost revolutions. Lost revolutions drastically reduce overall system throughput.

7.4.1 Advantages of Interleaving

- Maximum throughput on fully loaded systems.

  Fully loaded systems usually have many DMA devices contending for bus time. In this environment, the 43x may be forced to fall behind the disk. If the 43x does fall behind, it stops the transfer and waits one revolution until the next sector arrives under the head. This slows the aggregate data rate of the disk subsystem. Interleaving slows the aggregate data rate, lowering the 43x bus requirements, but not as much as losing a revolution.

- Maximum throughput on slow software systems.

  Slow software systems cannot turn interrupts around in the required time and usually transfer one sector at a time. In this environment, interleaving allows the system to catch many sectors per revolution instead of just one as on a non-interleaved disk.

7.4.2 Disadvantages of Interleaving

- Slows aggregate data throughput from the disk by the interleave factor.

7.5 Command-chaining

Command-chaining results in several performance advantages:

- The 43x may automatically perform overlap operations, allowing it to execute several functions simultaneously to several devices. This greatly improves system throughput.

- The operating system does not have to respond as rapidly after each command. The 43x executes the next command without operating system intervention. The 43x allows interrupts at the end of each IOPB and notifies the system after completing the IOPB.

Section 8: Installing and Testing the 431S and the 432

Section 8: Installing and Testing the 431S and the 432

8.0 Introduction

The following section describes how to unpack, configure, install, and test your 43x peripheral controller.

8.1 Unpacking and Inspection

8.1.1 Inspecting the Shipping Carton and the Controller

Inspect the carton for possible shipping damage. If there is damage, do not unpack the unit. Notify Xylogics and the freight carrier immediately. If no damage is visible, carefully unpack the 43x. Save the carton and other shipping material for possible later use.

Inspect the 43x for any loose parts; make sure they are all firmly seated in their sockets. If any parts need reinsertion, observe proper orientation.

8.1.2 Contents

The 43x is a single printed circuit board. Optional items include a manual and/or software on a magtape or floppy disk.

If any items are missing, please contact Xylogics at one of the following telephone numbers:

United States (Burlington, MA):	617-272-8140;
United Kingdom (Milton Keynes):	44-908-569444.

8.2 Configuring the 43x

You can configure the 43x with several jumper options. The following paragraphs describe these options (see Figure 8-1 [431S] and Figure 8-2 [432]).

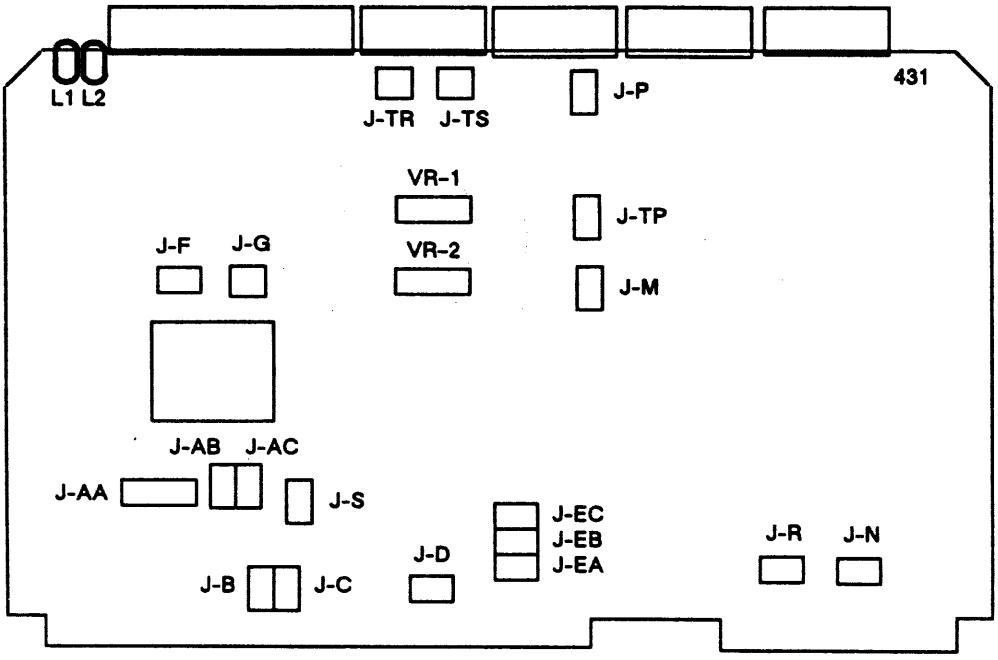


Figure 8-1. 431S Jumper Locations

8.2 Configuring the 43x (continued)

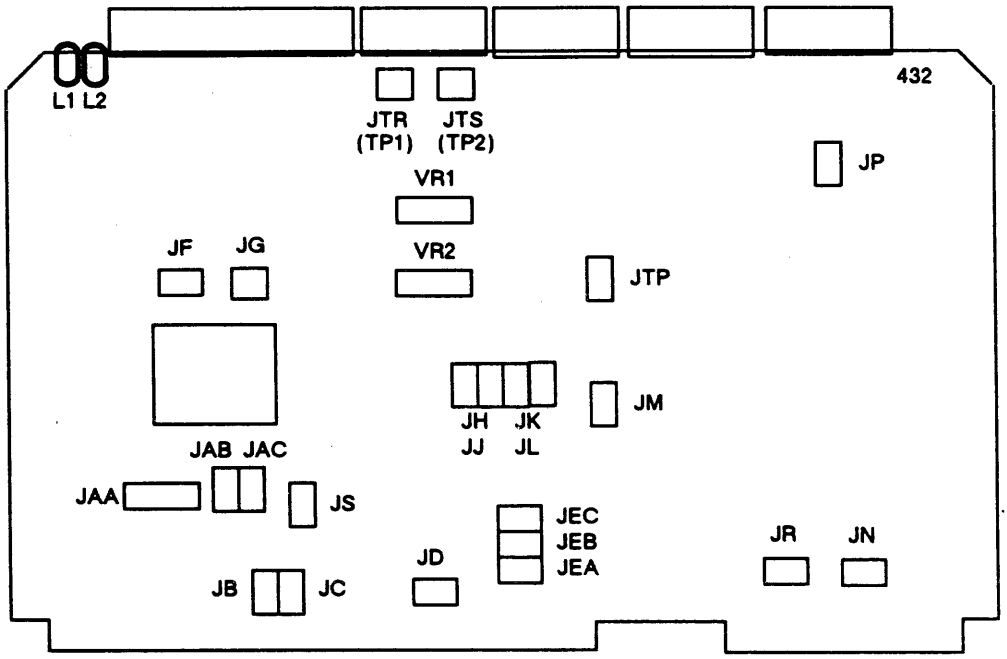


Figure 8–2. 432 Jumper Locations

8.2.1 Bytes Per Sector

Xylogics currently supports three sector sizes: 256-, 512-, and 1024-bytes per sector. Section 4.16 describes downloading these parameters.

8.2.2 Firmware

431S Firmware	Rev.	Type	Location
180-002-136	x	EPROM	M8
180-001-025	x	PAL	M2
181-001-026	x	PAL	N2
181-001-027	x	PAL	D4
181-001-028	x	PAL	G4
181-001-029	x	PAL	T8
181-001-030	x	PAL	F10

432 Firmware	Rev.	Type	Location
180-002-158	x	EPROM	L8
180-001-031	x	PAL	M2
180-001-032	x	PAL	N2
180-001-033	x	PAL	D4
180-001-034	x	PAL	G4
180-001-035	x	PAL	T8

8.2.3 Base Address Selection

There are two steps to selecting the base address. First, jumper the 43x for 8- or 16-bit register addresses. Jumpering pins 2–3 on jumper block J-S selects 8-bit addressing. Eight-bit addressing disables address bits 8 through F (see Table 8–1 and Figure 8–3). Factory configuration: J-S 1–2 *in*.

Table 8–1. 8/16-bit Addressing

J-S	1–2	2–3
8-bit:	Out	In
16 bit:	In	Out

8.2.3 Base Address Selection (continued)

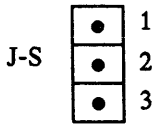


Figure 8–3. Jumper Block J-S

Second, jumper blocks J-AA and J-D control the actual base address selection. When selecting 8-bit addressing, only the jumpers for address bits 0 through 7 are valid. Ignore the jumpers for bits 8 through F (see Table 8–2). Factory configuration: EE80 (16-bit).

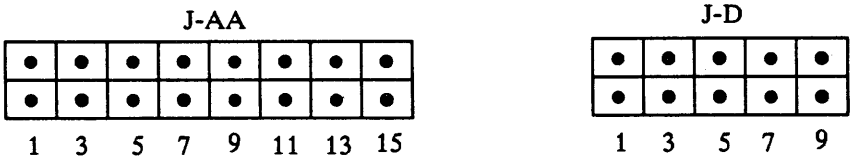


Figure 8–4. Jumper Blocks J-AA and J-D

Table 8–2. Base Address Selection

Address Bits:	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Jumper Block:	<--------- J-AA ---------->						<---------- J-D ---------->									
Pin Numbers:	2	4	6	8	10	12	14	16	2	4	6	8	10	N	N	N
	|	|	|	|	|	|	|	|	|	|	|	|	|			
	1	3	5	7	9	11	13	15	1	3	5	7	9			
Address:																
XX80-8-bit	X	X	X	X	X	X	X	X	I	O	O	O	O			
EE80-16-bit *	I	I	I	O	I	I	I	O	I	O	O	O	O			
XX70-8-bit	X	X	X	X	X	X	X	X	O	I	I	I	O			
EE70-16-bitX	I	I	I	O	I	I	I	O	O	I	I	I	O			

* Standard Factory Configuration

O = Out; I = In; X = Don't Care; N = Cannot Select (Always Zero)

8.2.4 20/24-Bit Address Relocation

The 43x functions in backplanes of 16-, 20-, and 24-bit addresses. Jumper block J-AB, pins 1-2, select the 20- and 24-bit addressing modes (see Figure 8–5). The 16-bit addressing mode is software programmable. System software determines jumper J-AB's status by reading ADRM; if set, the board is jumpered for 24-bit addressing. Both 20- and 24-bit addressing modes support 16-bit addressing. Factory configuration: pins 1–2 *in*.

Table 8–3. 20/24-Bit Addressing

Jumper J-AB Pins 1–2	Mode	ADRM Value
Installed	16/20	0
Removed	16/24	1

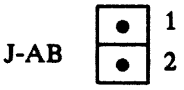


Figure 8–5. Jumper Block J-AB

8.2.5 24-Bit Extended Addressing

Xylogics provides jumpers for disconnecting the 24-bit addressing signals from the 43x's P2 connector. Factory configuration: all jumpers *in*.

Table 8–4. 24-Bit Extended Addressing

Address Bit	Jumper J-N
ADR17/	Pins 1-2
ADR16/	Pins 3-4
ADR15/	Pins 5-6
ADR14/	Pins 7-8

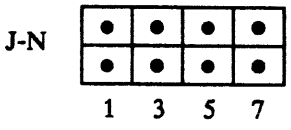


Figure 8–6. Jumper Block J-AB

8.2.6 Bus Busy

The IEEE 796 Specification requires fully deasserting the *Bus Busy* (*BUSY*) signal within 70 nanoseconds (ns) after the *Bus Clock* (*BCLK*) signal falls. The 43x releases *BUSY* from 15 to 32 ns after *BCLK* falls, after which *BUSY*'s behavior is a function of bus conditions (total bus capacitance and passive and active loads).

Jumper block J-B controls the *BUSY* signal timing for DMA bus arbitration. When pins 1–2 are jumpered, the 43x DMAC bus arbiter interprets *BUSY* as received from the bus. Jumpering pins 2–3 delays *BUSY* to the DMAC bus arbiter by resynchronizing it to *BCLK*, avoiding potential metastable problems caused by poor system bus rise time. Factory configuration: pins 1-2 *in*.

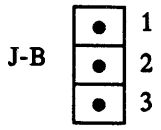


Figure 8–7. Jumper Block J-B

8.2.7 Interrupt Request Levels

The 43x supports eight interrupt request levels (IRLs). Table 8–5 lists the jumper positions for the various interrupt request levels (see Figure 8–8). Factory configuration: INT5/.

Table 8–5. Interrupt Request Levels

Interrupt Level	Jumper Position
INT0/	J-EC 1 to J-EB 1
INT1/	J-EC 2 to J-EB 2
INT2/	J-EC 3 to J-EB 3
INT3/	J-EC 4 to J-EB 4
INT4/	J-EA 1 to J-EB 1
INT5/	J-EA 2 to J-EB 2
INT6/	J-EA 3 to J-EB 3
INT7/	J-EA 4 to J-EB 4

8.2.7 Interrupt Request Levels (continued)

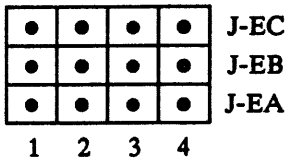


Figure 8–8. Jumper Blocks J-EA, J-EB, and J-EC

8.2.8 Winchester Disk Drive Unit Select Numbers

Jumper block J-P configures the 431S for addressing any one of the four drive select lines available on most disk drives. Remember, two disk drives may interface the 431S at any given time. The factory connects Unit 0 to Drive Select 1, and Unit 1 to Drive Select 2.

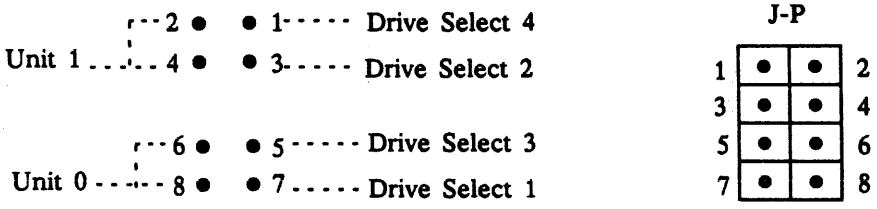


Figure 8–9. Jumper Block J-B

On the 432, JP comprises DFE test points. Do not jumper these pins.

8.2.9 Disable Bus Priority Out

Jumper block J-AC controls the *Disable Bus Priority Out* (*BPRO/*) signal for DMA bus arbitration. Jumpering pins 1–2 enables serial DMA priority; removing the jumper from pins 1–2 isolates the *BPRO/* signal from the Multibus, enabling parallel DMA priority. Factory setting: pins 1–2 *in*.

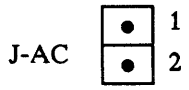


Figure 8–10. Jumper Block J-AC

> *The Multibus Specification does not clearly define the timing between BPRO/ and BUSY; therefore, it is open to interpretation. In the 43x, BPRO/ goes inactive before the BUSY line is deasserted. In the Xylogics 450 and 472 controllers, both signals go inactive at approximately the same time. Most customers use BUSY, rather than BPRO/, to determine when the device releases the bus. Xylogics improved the 43x's bus throughput by changing the timing.*

8.2.10 Light Emitting Diodes

The 43x has two light emitting diodes (LEDs). L1 is the Active LED; when on, the 43x is ready to accept commands. L2 is the Busy LED; it lights for a moment, and then goes off, indicating that the 43x successfully completed the on-board diagnostics. If L2 remains on, the 43x is not functioning properly. Contact Xylogics for further assistance.

8.2.11 Remote Activity Indicator

You can connect a remote activity indicator signal to the backplane. Jumper block J-R controls this option. Jumper pins 1–2, and wire the remote LED between +5 volts and pin 42 of the P2 connector. Factory configuration: pins 1-2 *out*.

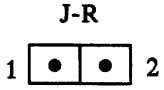


Figure 8–11. Jumper Block J-R

8.2.12 Software Programmable Drive Characteristics

Different Winchester disk drives require that you configure the 43x with regard to:

- Write Precompensation (see Section 4.16.6).
- Reduced Write Current (see Section 4.16.6).
- Buffered Seeks (see Section 4.16.2).
- Head Step Times (see Section 4.16.2).

8.2.13 Floppy Disk Jumpers

The jumper settings for floppy disk drives are:

Factory	Jumper
Out	**J-F:** 1–2 – *in* for 8-inch and 5.25-inch high performance quad density (HPQD) floppy drives. FDC operates at 2-MHz.
In	**J-F:** 2–3 – *in* for 5.25-inch drives. FDC operates at 1-MHz.
Out	**J-F (Models 432–103 and above):** 1–2 – *in* for software programmable standard of HPQD mode.
In	**J-F (Models 432–103 and above):** 2–3 – *in* for 5.25-inch drives. FDC operates at 1-MHz.

> *For models 432–103 and above, removing the jumpers from J–F forces the hardware into high performance quad density (HPQD) mode.*

Out	**J-G:** 1–2 – *in* to set VR1 and VR2; normally *out*.
In	**J-G:** 3–4 – *in* sets internal VC0 frequency of FDC for 5.25-inch floppy drives; *out* sets internal VCO frequency of FDC for 8- and 5.25-inch HPQD floppy drives.
Out	**J-H:** All – Reserved; normally *out*.

8.2.13 Floppy Disk Jumpers (continued)

Factory Jumper

In **J-J:** 1–2 – *in* for drives requiring Write Precompensation on tracks greater than 43.

Out **J-J:** 2–3 – *in* for drives requiring Write Precompensation on all tracks.

> *Jumper J-J is only effective if Write Precompensation is enabled when the drive parameters are set.*

In **J-K:** 1–2 – *in* for systems that turn the motor on and off depending on activity. Connects the line from the FDC to the floppy drive.

Out **J-K:** 2–3 – *in* for systems that permanently engage the drive motor. Pulls up the *Motor On* signal to the drive.

Out **J-L:** 1–2 – *in* for drives that give *Ready-L* or *Door Closed-L* on pin 34 (e.g., Teac, Shugart 410/460, DCD 9409). Connects the line from the floppy drive to the floppy disk controller chip (FDC).

In **J-L:** 2–3 – *in* for all other drives. Pulls up the *Ready* line to the FDC.

In **J-M:** 1–2 – *in* enables the *In Use* line (pin 4) to the drive (grounds J2 P4); *out* disables the *In Use* line.

8.3 Floppy Disk Analog Components

8.3.1 Setting Up Floppy Disk Analog Components for the 43x

The following steps describe how to set up the floppy disk analog components.

1. Power-up the 43x and allow it to complete the normal power sequence initialization.
2. Insert jumper J-G pins 1–2; this sets TEST, pin 22, low.

> *Do not initialize the 43x while jumper J-G pins 1–2 are installed.*

8.3.1 Setting Up Floppy Disk Analog Components for the 43x (continued)

3. For 5.25-inch HPQD floppy drives, jumper J-TR to J-G pin 3.

4. For informational purposes only: Xylogics changes the value of C4 for each drive type (5.25-inch floppy drives use 0.22μF; 8- and 5.25-inch HPQD drives use 0.1μF ± 10%).

5. Adjust VR1 (10K-ohm) while monitoring J-TP1 with an oscilloscope. Set the pulse width observed on J-TP1 (± 2%) to:

   a) the precompensation time the floppy drive requires;
   b) one-third of the desired write data pulse width; or
   c) 160 ns, which gives 200 ns Write Precompensation, if enabled, and a write data pulse width of 480 ns.

   The factory setting is 200 ns.

6. Verify the density; setting J-TP4 low selects double density.

7. Adjust VR2 (50K-ohm) while monitoring J-TP2 with an oscilloscope. Set the pulse width observed on J-TP2 (± 2%) to:

Density	Drive	Pulse (ns)	Data Rate (KHz)
Double	8- and 5.25-inch HPQD	250	500
Single	8- and 5.25-inch HPQD	500	250
Double	5.25-inch	500	250
Single	5.25-inch	1000	125

   The factory setting is single density.

8. Adjust VC1 while monitoring J-TP3 with a counter. The frequency observed on J-TP3 should equal the data rate listed above (± 1%). The factory setting is 250-KHz.

Density	Drive	Wavelength
Single	5.25-inch	8 microseconds (μs)
Double	5.25-inch	4 μs
Single	8- and 5.25-inch HPQD	4 μs
Double	8- and 5.25-inch HPQD	2 μs

   The factory setting is single density.

8.3.2 Setting Up Floppy Disk Analog Components for the 432-103

The following steps describe how to set up the floppy disk analog components for the 432-103 (and above).

1. Power-up the 432 and allow it to complete the normal power sequence initialization.

2. Insert jumper J-G pins 1-2; this sets the FDC to TEST mode.

> *Do not initialize the 432 while jumper J-G pins 1-2 are installed.*

3. For 5.25-inch drives, install jumper J-G pins 3-4. Remove for 8-inch drives.

4. Remove jumper, if any, from jumper J-F. This defaults the 432 to high performance mode.

5. Adjust VR1 (10K-ohm) while monitoring J-TP1 with an oscilloscope. Set the pulse width observed on J-TP1 (± 2%) to:

   a) the precompensation time the floppy drive requires;
   b) one-third of the desired write data pulse width; or
   c) 160 ns, which gives 200 ns Write Precompensation, if enabled, and a write data pulse width of 480 ns.

   The factory setting is 200 ns.

6. Verify the density on J-TP4; setting it low selects double density. The firmware default is single density.

7. Adjust VR2 (50K-ohm) while monitoring J-TP2 with an oscilloscope. Set the pulse width observed on J-TP2 (± 2%) to:

Density	Drive	Pulse (ns)	Data Rate (KHz)
Single	8-, 5.25-, and 3.5-inch HP	500	250
Double	8-, 5.25-, and 3.5-inch HP	250	500

8.3.2 Setting Up Floppy Disk Analog Components for the 432-103 (continued)

8. Adjust VC1 while monitoring J-TP3 with an oscilloscope. Set the frequency (± 1%) to:

Density	Drive	Wavelength
Single	8-, 5.25-, and 3.5-inch HP	4 µs
Double	8-, 5.25-, and 3.5-inch HP	2 µs

9. Install jumper J-F pins 2-3. This sets the hardware to the standard mode.

10. Adjust VR3 (50K-ohm) while monitoring J-TP2 with an oscilloscope. Set the pulse width (± 2%) to:

Density	Drive	Pulse (ns)	Data Rate (KHz)
Single	5.25-inch	1000	125
Double	5.25-inch	500	250

11. Verify the setting of VC1 by observing J-TP3 with an oscilloscope. The frequency should equal:

Density	Drive	Wavelength
Single	8-, 5.25-, and 3.5-inch HP	8 µs
Double	8-, 5.25-, and 3.5-inch HP	4 µs

12. Remove the jumper from J-F pins 2-3 and jumper pins 1-2.

13. Remove the jumper from J-G pins 1-2.

8.4 Preparing the Computer System

The backplane of your system must provide a Multibus slot for the 43x. The slot must be capable of handling a bus master, and the power source must handle the power consumption of the entire system, including the 43x.

8.4.1 Card Cage Slot

The card cage must have a slot available for the 43x. Placement of the 43x in the DMA priority chain can be critical; consider this when choosing a slot.

8.4.2 DMA Bus Arbitration

The 43x uses either serial or parallel DMA arbitration. Serial arbitration is much easier to implement, but has restrictions on the number of bus masters it can arbitrate. Parallel bus arbitration is harder to implement, but is more versatile and can handle more bus masters.

8.4.2.1 Serial DMA Priority

To implement serial priority, connect the *Bus Priority Out (BPRO/)* and *Bus Priority In (BPRN/)* lines in a serial fashion (see Figure 8-12). The first slot has the highest priority, and must have its *BPRN/* line grounded. The next slot has the next highest priority. A unit must assert its *BPRN/* line to become bus master. If a unit is not currently a bus master, it deasserts its *BPRO/* line so the following units cannot assert their *BPRN/* lines and become bus master.

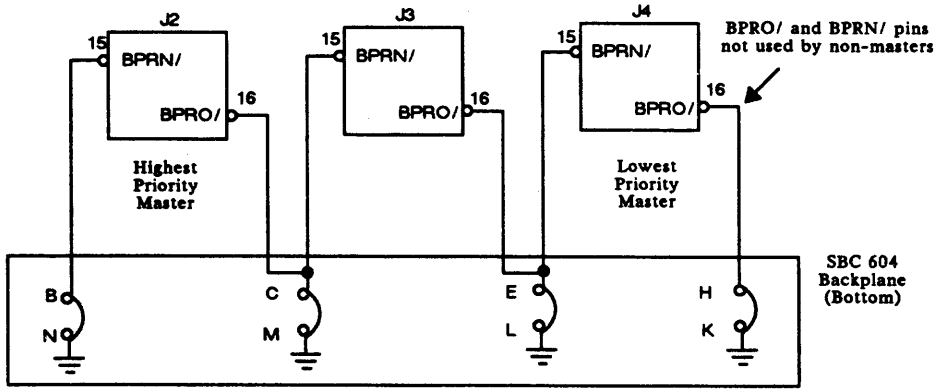


Figure 8-12. Serial DMA Priority

8.4.2.2 Parallel DMA Priority

Parallel and serial priority use the same connections to each board. To implement parallel priority, connect these signals to an external circuit similar to Figure 8–13. The *Bus Request (BREQ/)* line requests the bus. The external circuit performs bus arbitration. Since the *BPRN/* line of one board usually connects to the *BPRN/* line of the next board, the circuit in Figure 8–13 has two outputs tied together. You can correct this by disabling the *BPRO/* lines from each board.

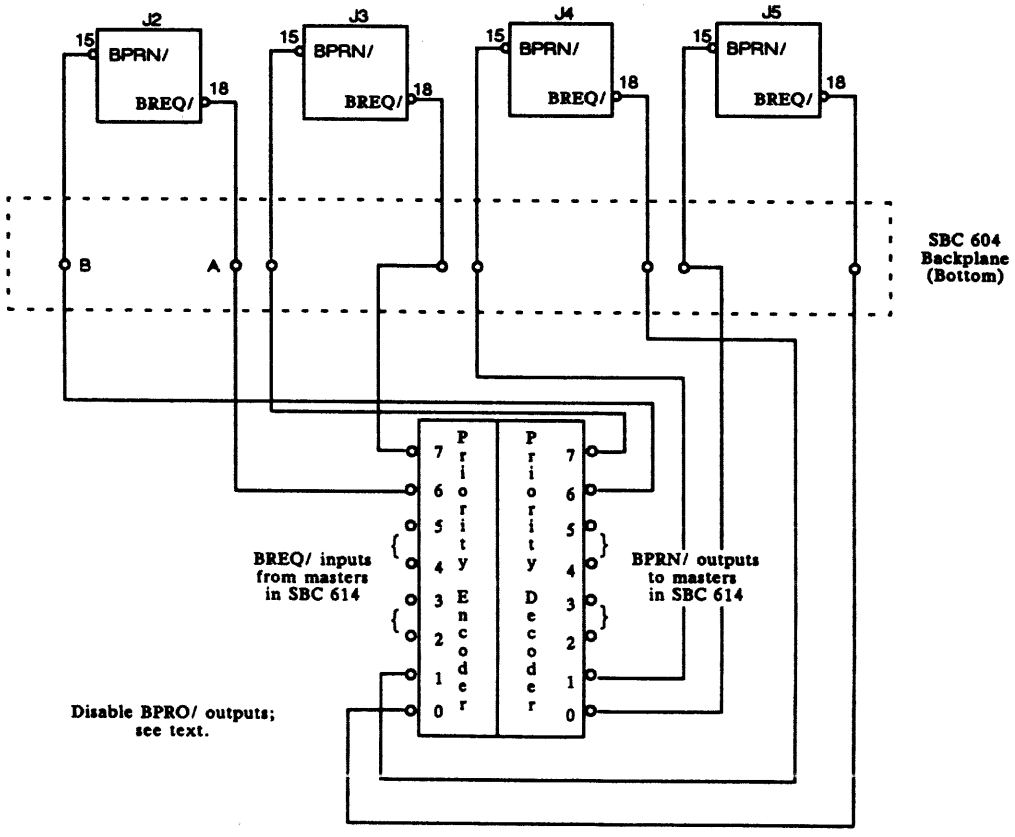


Figure 8–13. Parallel DMA Priority

8.4.3 Power Considerations

The 43x affects the power consumption of the entire computer system. Make sure the power supplies can handle the entire power load. Readjust the voltages *after* plugging in the controller. A power supply that is just adequate may cause intermittent and unusual problems from noise generated by occasional overcurrent protection.

8.5 Preparing the Disk Drive

Carefully unpack the disk drive and configure it according to the drive manual.

8.5.1 Drive Unit Select

Switches or jumpers on one of the drive's internal circuit cards usually select the drive unit number. The 43x can access drives addressed as 1, 2, 3, or 4 (see Section 8.2.8).

8.5.2 Number of Sectors Per Track

If you are using the sector slip feature, the number of sectors available to system software is the number of allocated sectors less the spares (see Section 6.7). Some hard-sectored disk drives have a runt sector (a very small sector at the end of the disk). The 43x requires that all sectors on a track are formatted. Sometimes the runt sector is too small to format.

8.5.3 Bytes Per Sector

The 43x sequencer PROMs define the sector size for Winchester disk drives (see Section 8.2.1). The sector size for floppy disk drives is software programmable (see Sections 4.15 and 4.16).

8.6 Preparing the Tape Drive

Carefully unpack the tape drive and configure it according to the drive manual. The 43x supports up to four QIC-02 formatted tape drives. Number these drives 1, 2, 3, and 4.

8.7 Install and Cable the 43x

8.7.1 Install the 43x

Place the 43x into the computer card cage; make sure it is firmly seated. Do not dislodge any socketed ICs. Situate the disk drive and connect it to the appropriate power source.

8.7.2 Install the Cables

Connect the cables to only one drive at a time. Using *pull tabs* on the cables greatly reduces connector damage. Observe *pin 1* markings on both the 43x and the cables. Mechanically restraining the cables at both ends prevents them from accidentally disconnecting. Install a ground braid wire between the ground terminal on the drive(s) and the computer ground.

8.8 Initial Tests

This section relies upon your familiarity with the computer system's monitor.

8.8.1 Power-up and Self Test

On power-up, the 43x initiates a self test. L1 lights for a moment, and then goes off. If it remains on, the controller is not functioning properly; contact Xylogics for assistance. *Make sure the power supply voltage is within limits (4.75 to 5.25 volts).*

8.8.2 Register Verification

Check the 43x registers. On power-up, the IOPB Address and Relocation Registers clear to all zeros; verify this by reading them. The CSR contains an 01 or 09 if ADRM is set for 24-bit addressing. If you are unable to access the registers, check the 43x base address jumpers and/or your particular system I/O register requirements. Try writing some value to the Address Registers and read it back to verify the data.

8.8.3 Drive On-line

This procedure requires a Read Drive Status command. If bit 5 in Tape Status Byte 3 (TSTAT3) is set, the selected tape drive is off-line; check the drive cable connections and try again. If you still cannot get the proper status, check the tape drive with the off-line diagnostics or tester.

8.8.4 Tape Drive Diagnostics

Many tape drive manufacturers offer power-on and off-line diagnostic capabilities. See your tape drive manual for more information.

8.8.5 Cabling Multiple Drives

When daisy-chaining tape drives, connect the first drive in the chain to the 43x (50-pin connector); connect additional drives together, starting with the initial drive. For example, the 43x connects to Drive 1; Drive 1 connects to Drive 2; Drive 2 connects to Drive 3, etc. Be careful; do not reverse the cables. Terminate the cabling at the last drive in the chain.

When daisy-chaining Winchester disk drives, connect the *A* cable directly from the first drive in the chain to the 43x (34-pin connector); connect the second drive to the first drive, observing the *pin 1* cable markings. Terminate the *A* cable at the second drive. The *B* cables connect directly from each drive to a *B* cable port on the 43x (20-pin connector).

8.8.5 Cabling Multiple Drives (continued)

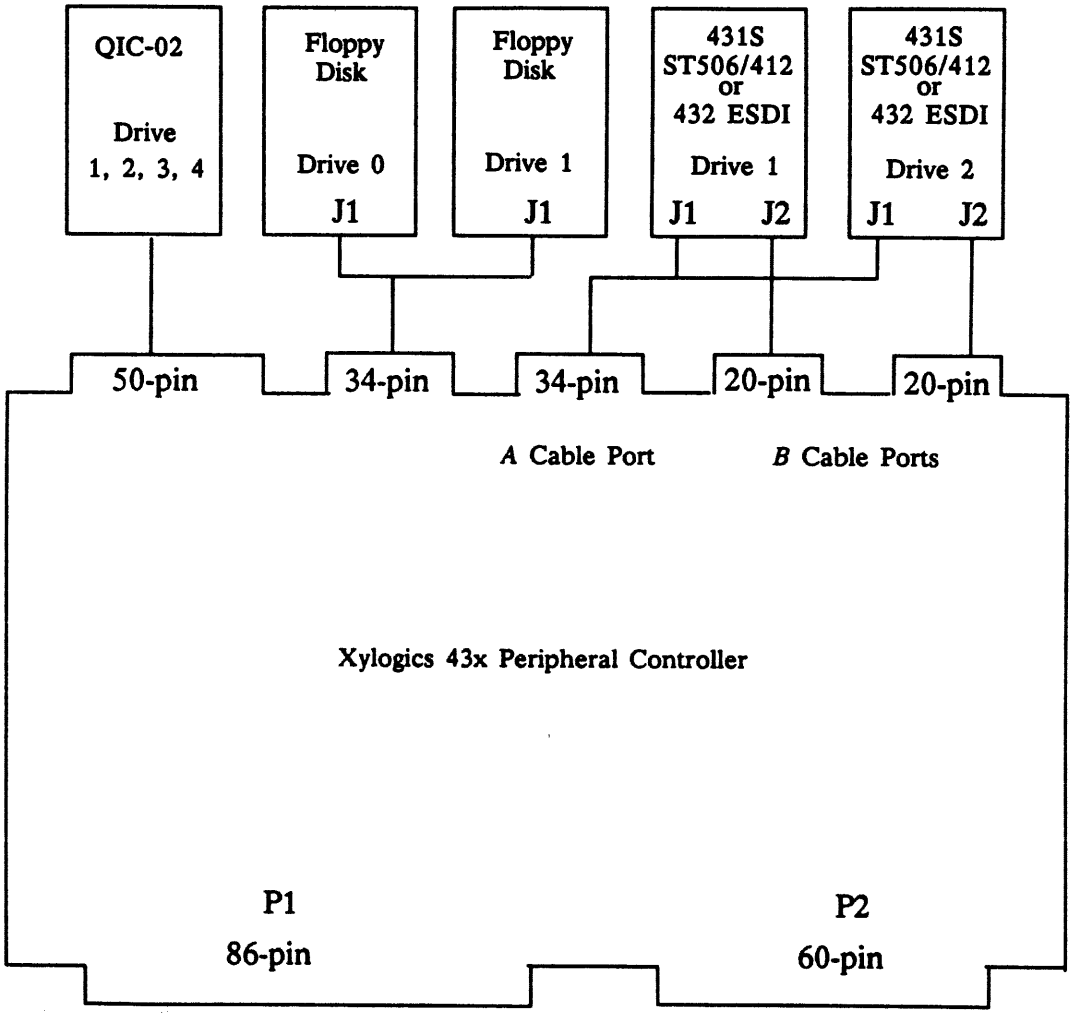


Figure 8-14. Multiple Drive Connection Diagram

Section 9: Installing and Testing the 431T

Section 9: Installing and Testing the 431T

9.0 Introduction

The following section describes how to unpack, configure, install, and test your 431T.

9.1 Unpacking and Inspection

9.1.1 Inspect the Shipping Carton and the Controller

Inspect the carton for possible shipping damage. If there is damage, do not unpack the unit. Notify Xylogics and the freight carrier immediately. If no damage is visible, carefully unpack the 431T. Save the carton and other shipping material for possible later use.

Inspect the 431T for loose parts; all parts should be firmly seated in their sockets. If any parts need reinsertion, observe proper orientation.

9.1.2 Contents

The 431T is a single printed circuit board. Optional items include a manual and/or software on a magtape or floppy disk.

If any items are missing, please contact Xylogics at one of the following telephone numbers:

United States (Burlington, MA):	617-272-8140;
United Kingdom (Milton Keynes):	44-908-569444.

9.2 Configuring the 431T

You can configure the 431T with several jumper options. The following subsections describe these options.

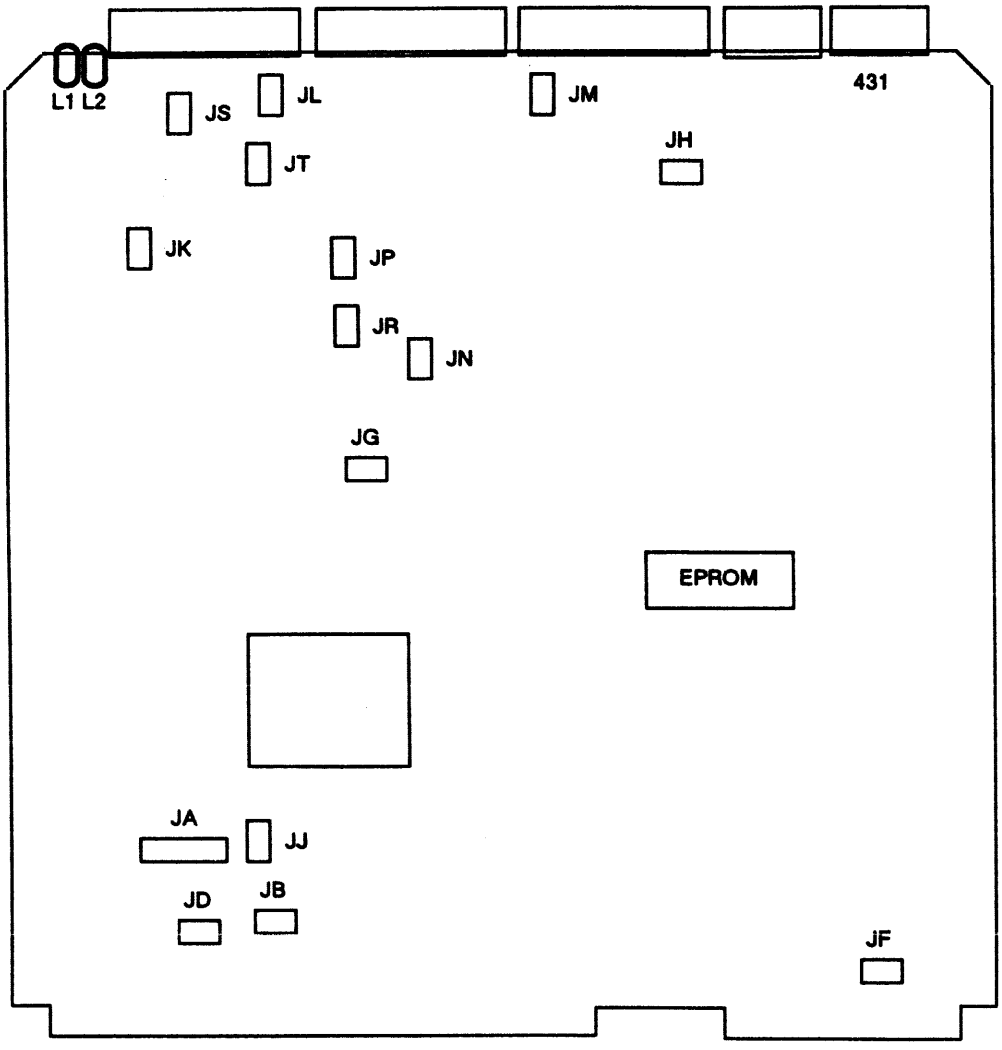


Figure 9-1. 431T Jumper Locations

9.2.1 Bytes Per Sector

The 431T sequencer PROMs K9 and L11 determine the number of bytes in a sector.

Part Number	Bytes Per Sector	PROM Part Number	
		K9	L11
900-431-000	256	180-002-008	180-002-008
900-431-001	512	180-001-013	180-002-014
900-431-002	1024	180-002-015	180-002-016

9.2.2 Firmware

Firmware	Rev.	PROM	Location
180-001-097	x	EPROM	F8
180-002-005	x	Disk Sequencer	J9
180-002-007	x	Disk Sequencer	L9
181-001-014	x	PAL	F1
181-001-006	x	PAL	H5
181-001-007	x	PAL	C3
181-001-008	x	PAL	V13
181-001-010	x	PAL	H2
181-001-011	x	PAL	Y4

9.2.3 Base Address Selection

There are two steps to selecting the base address. First, jumper the 431T for 8- or 16-bit register addresses. Jumpering pins 2-3 on jumper block JJ selects 8-bit addressing (see Table 9-1 and Figure 9-2); 8-bit addressing disables address bits 8 through F. Factory configuration: JJ 1-2 *in*.

9.2.3 Base Address Selection (continued)

Second, jumper blocks JA and JD control the actual base address. When selecting 8-bit addressing, only the jumpers for address bits 0 through 7 are valid. Ignore the jumpers for bits 8 through F (see Table 9-2). Factory configuration: EE80.

> *Pins 1-2 on jumper block JA are not used.*

Table 9-1. 8/16-Bit Addressing

Jumper Block:	JJ 1-2	JJ 2-3
8-bit:	Out	In
16-bit:	In	Out

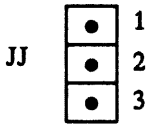


Figure 9-2. Jumper Block JJ

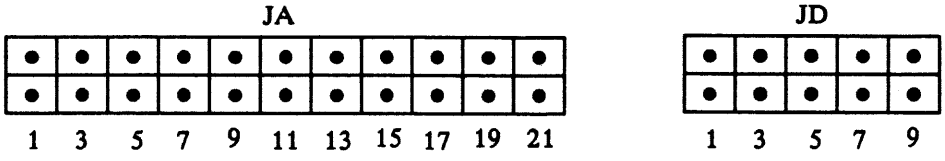


Figure 9-3. Jumper Blocks JA and JD

9.2.3 Base Address Selection (continued

Table 9–2. Base Address Selection

Address Bits:	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Jumper Block:	|<---------- J A----------\>|<------ JD --------\>|										N	N	N			
Pin Numbers:																
	4	8	12	16	6	10	14	18	10	8	6	2	4	N	N	N
	|	|	|	|	|	|	|	|	|	|	|	|	|			
	3	7	11	15	5	9	13	17	9	7	5	1	3			
Address:																
XX80–8-bit	X	X	X	X	X	X	X	X	I	O	O	O	O			
EE80–16-bit *	I	I	I	O	I	I	I	O	I	O	O	O	O			
XX70–8-bit	X	X	X	X	X	X	X	X	O	I	I	I	O			
EE70–16-bitX	I	I	I	O	I	I	I	O	O	I	I	I	O			

* Standard Factory Configuration

O = Out; I = In; X = Don't Care; N = Cannot Select (Always Zero)

9.2.4 20/24-Bit Address Relocation

The 431T functions in backplanes of 16-, 20-, and 24-bit addresses. Jumper block JA, pins 21–22, selects the 20- and 24-bit addressing modes (see Figure 9–3). The 16-bit addressing mode is software programmable. Software reads ADRM in the CSR and determines the status of this jumper; when set, the board is jumpered for 24-bit addressing. Both 20- and 24-bit addressing modes support 16-bit addressing. Factory configuration: pins 21–22 *in*.

Table 9–3. 20/24-Bit Addressing

Jumper Block JA Pins 21–22	Mode	ADRM
In	16/20	0
Out	16/24	1

9.2.5 24-Bit Extended Addressing

Xylogics provides jumpers for disconnecting the 24-bit addressing signals from the 431T's P2 connector for systems not utilizing this option. Factory configuration: all jumpers *in*.

Table 9–4. 24-Bit Extended Addressing

Address Bit	Jumper Block JF
ADR17/	Pins 3–4
ADR16/	Pins 7–8
ADR15/	Pins 5–6
ADR14/	Pins 9–10

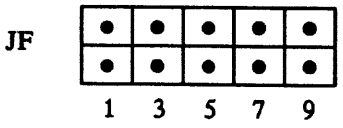


Figure 9–4. Jumper Block JF

9.2.6 Interrupt Request Levels

The 431T supports eight interrupt request levels. Table 9–5 lists the jumper positions for the various interrupt request levels; Figure 9–5 illustrates the jumper block JB. Factory configuration: INT5/.

Table 9–5. Interrupt Request Levels

Int. Req. Level	Jumper Position
INT0/	E1 to JB pin 8
INT1/	E1 to JB pin 7
INT2/	E1 to JB pin 6
INT3/	E1 to JB pin 5
INT4/	E1 to JB pin 4
INT5/	E1 to JB pin 3
INT6/	E1 to JB pin 2
INT7/	E1 to JB pin 1

9.2.6 Interrupt Request Levels (continued)

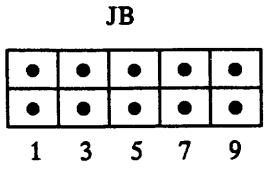


Figure 9–5. Jumper Block JB

9.2.7 Winchester Disk Drive Unit Select Numbers

Jumper block JH configures the 431T to address any one of the four drive select lines available on most disk drives. Remember, two disk drives may interface the 431T at any given time. The factory connects Unit 0 to Drive Select 1, and Unit 1 to Drive Select 2.

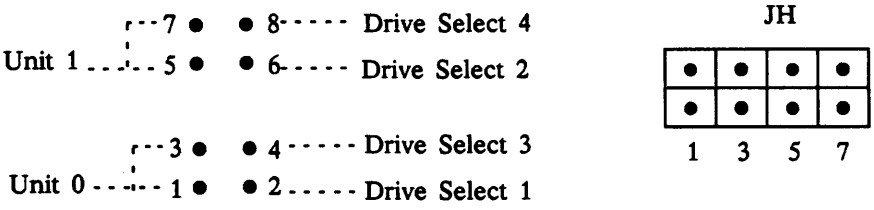


Figure 9–6. Jumper Block JH

9.2.8 Disable Bus Priority Out

Jumper block JA controls the *Disable Bus Priority Out* (*BPRO/*) signal for DMA bus arbitration (see Figure 9–3). Jumpering pins 19–20 enables serial DMA priority; removing the jumper from pins 19–20 isolates the *BPRO/* signal from the Multibus, enabling parallel DMA priority. Factory setting: pins 19–20 *in*.

9.2.8 Disable Bus Priority Out (continued)

> *The Multibus Specification does not clearly define the timing between BPRO/ and BUSY; therefore, it is open to interpretation. In the 431T, BPRO/ goes inactive before the BUSY line is deasserted. In the Xylogics 450 and 472 controllers, both signals go inactive at approximately the same time. Most customers use BUSY, rather than BPRO/, to determine when the device releases the bus. Xylogics improved the 431T's bus throughput by changing the timing.*

9.2.9 Light Emitting Diodes

The 431T has two light emitting diodes (LEDs). L1 is the Self Test LED; it lights during self testing and goes off when the controller successfully completes the tests. L2 is the Idle LED; when lit, the controller is ready to accept commands.

9.2.10 Remote Activity Indicator

You can connect a remote activity indicator signal to the backplane. Jumper block JF controls this option (see Figure 9-4). Jumper pins 1-2, and wire the remote LED between +5 volts and pin 42 of the P2 connector. Factory configuration: pins 1-2 *out*.

9.2.11 Software Programmable Drive Characteristics

Different Winchester disk drives require configuring the 431T with regard to the following:

- Write Precompensation (see Section 4.16.6).
- Reduced Write Current (see Section 4.16.6).
- Buffered Seeks (see Section 4.16.2).
- Head Step Times (see Section 4.16.2).

9.2.12 Floppy Disk Jumpers

The jumper settings for floppy disk drives are:

Factory	Jumper
Out	**JP:** 1-2 – *in* for drives that give *Ready-L* or *Door Closed-L* on pin 34 (e.g., Teac, Shugart 410/460, CDC 9409). Connects the line from the floppy drive to the floppy disk controller chip (FDC).
In	**JP:** 2–3 – *in* for all other drives. Pulls up the *Ready* line to the FDC.
Out	**JN:** 1–2 – *in* for systems that turn the motor on and off dependng on the activity. Connects the line from the FDC to the floppy drive.
In	**JN:** 2–3 – *in* for systems that permanently engage the drive motor. Pulls up the *Motor On* signal to the drive.
Out	**JR:** 1–2 – *in* for drives requiring Write Precompensation on tracks greater than 43.
In	**JR:** 2–3 – *in* for drives requiring Write Precompensation on all tracks.

> *Jumper block JR is only effective if Write Precompensation is enabled when the drive parameters are set.*

In	**JK:** 1–2 – *in* for all 8-inch drives. FDC operates at 2-MHz.
Out	**JK:** 2–3 – *in* for 5.25-inch drives. FDC operates at 1-MHz.
Out	**JM:** All – Reserved; normally *out*.
Out	**JL:** 1–2 – *in* enables the *In Use* line (pin 4) to the drive (grounds J2 P4); *out* disables the *In Use* line.
Out	**JT:** 1–2 – *in* to set VR1 and VR2; normally *out*.
In	**JS:** 1–2 – *in* sets internal VCO frequency of FDC for 5.25-inch floppy drives; *out* sets internal VCO frequency of FDC for 8-inch floppy drives.

9.3 Setting Up Floppy Disk Analog Components

1. Power-up the 431T and allow it to complete the normal power sequence initialization.

2. Insert jumper JT; this sets TEST, pin 22, low.

> *Do not initialize the 431T while jumper JT is installed.*

3. Adjust VR1 (10K-ohm) while monitoring TP1 with an oscilloscope. The pulse width observed on TP1 should be set (± 2%) to:

   a) the precompensation time the floppy drive requires;
   b) one-third of the desired write data pulse width; or
   c) 160 ns, which gives 200 ns Write Precompensation, if enabled, and a write data pulse width of 480 ns.

   The factory setting is 200 ns.

4. Verify the density; if pin 37 of the 2797 is low, double density is selected.

5. Adjust VR2 (50K-ohm) while monitoring TP2 with an oscilloscope. The pulse width observed on TP2 should be set (± 2%) to:

Density	Drive	Pulse (ns)	Data Rate (KHz)
Double	8-inch	250	500
Single	8-inch	500	250
Double	5.25-inch	500	250
Sinble	5.25-inch	1000	125

6. Adjust VC1 while monitoring TP3 with a counter. The frequency observed on TP3 should be set to the data rate listed above ± 1%. Factory setting is 250-KHz.

Density	Drive	Wavelength
Single	5.25-inch	8 microseconds (µs)
Double	5.25-inch	4 µs
Single	8-inch	2 µs
Double	8-inch	2 µs

7. Remove jumper JT.

Section 10:
Interface Signals

Section 10: Interface Signals

10.0 Introduction

This section provides useful interface information for installing and maintaining your 43x peripheral controller.

10.1 Multibus Interface Signals

Mnemonic	Conn.	Pin	Used By 43x	Description
ADR0/	P1	57	Y	
ADR1/	P1	58	Y	
ADR2/	P1	55	Y	
ADR3/	P1	56	Y	
ADR4/	P1	53	Y	
ADR5/	P1	54	Y	
ADR6/	P1	51	Y	
ADR7/	P1	52	Y	
ADR8/	P1	49	Y	
ADR9/	P1	50	Y	
ADRA/	P1	47	Y	
ADRB/	P1	48	Y	
ADRC/	P1	45	Y	
ADRD/	P1	46	Y	Address Bus
ADRE/	P1	43	Y	
ADRF/	P1	44	Y	
ADR10/	P1	28	Y	
ADR11/	P1	30	Y	
ADR12/	P1	32	Y	
ADR13/	P1	34	Y	
ADR14/	P2	57	P	
ADR15/	P2	58	P	
ADR16/	P2	55	P	
ADR17/	P2	56	P	
DAT0/	P1	73	Y	Data Bus
DAT1/	P1	74	Y	
DAT2/	P1	71	Y	
DAT3/	P1	72	Y	

Y = Yes; N = No; P = Possibly (Jumper or Optionally Available)

10.1 Multibus Interface Signals (continued)

Mnemonic	Conn.	Pin	Used By 43x	Description
DAT4/	P1	69	Y	
DAT5/	P1	70	Y	
DAT6/	P1	67	Y	
DAT7/	P1	68	Y	
DAT8/	P1	65	Y	Data Bus
DAT9/	P1	66	Y	
DATA/	P1	63	Y	
DATB/	P1	64	Y	
DATC/	P1	61	Y	
DATD/	P1	62	Y	
DATE/	P1	59	Y	
DATF/	P1	60	Y	
Strobes				
IORC/	P1	21	Y	I/O Read Command
IOWC/	P1	22	Y	I/O Write Command
MRDC/	P1	19	Y	Memory Read Command
MWTC/	P1	20	Y	Memory Write Command
XACK/	P1	23	Y	Transfer Acknowledge
DMA				
BPRN/	P1	15	Y	Bus Priority In
BPRO/	P1	16	Y	Bus Priority Out
BREQ/	P1	18	P	Bus Request
BUSY/	P1	17	Y	Bus Busy
CBRQ/	P1	29	N	Common Bus Request
Clocks				
BCLK/	P1	13	P	Bus Clock
CCLK/	P1	31	N	Constant Clock
PLC/	P2	31	N	Power Line Clock

Y = Yes; N = No; P = Possibly (Jumper or Optionally Available)

10.1 Multibus Interface Signals (continued)

Mnemonic	Conn.	Pin	Used By 43x	Description
Interrupts				
INT0/	P1	41	P	
INT1/	P1	42	P	
INT2/	P1	39	P	
INT3/	P1	40	P	
INT4/	P1	37	P	Interrupt Request Levels
INT5/	P1	38	P	
INT6/	P1	35	P	
INT7	P1	36	P	
INTA/	P1	33	N	Interrupt Acknowledge
Miscellaneous Control				
BHEN/	P1	27	Y	Byte High Enable
BD RESET/	P2	36	N	Board Reset
HALT/	P2	28	N	Bus Master Wait State
INH1/	P1	24	N	Inhibit 1; Disable RAM
INHT/	P1	14	Y	Initialize
Power				
12VB	P2	11,12	N	+12VDC Battery
5VB	P2	3	N	+5 VDC Battery
GVB	P2	4	N	Return
-5VB	P2	7,8	N	-5 VDC Battery
-12VB	P2	15,16	N	-12VDC Battery
+5V	P1	3,4,5,6,81,82,82,84	Y	+5VDC
+12V	P1	7,8	N	+12 VDC
+15	P2	23,24	N	+15 VDC
-5V	P1	9,10	P	-5 VDC Supply
-12V	P1	79,80	P	-12 VDC
-15V	P2	25,26	N	-15 VDC
EEVPP	P2	6	N	E2 PROM Power
GND	P1	1,2,11,12,75,76,85,86	N	Signal GND
GND	P2	1,2,21,22	N	Signal GND

Y = Yes; N = No; P = Possibly (Jumper or Optionally Available)

10.1 Multibus Interface Signals (continued)

Mnemonic	Conn.	Pin	Used By 43x	Description
Miscellaneous				
ACLO/	P2	18	P	AC Low
ALE/	P2	32	N	Bus Master ALE
AUX RESET/	P2	38	N	Reset Switch Reserved
MPRO/	P2	20	N	Memory-protect
PAR1/	P2	27	N	Parity 1
PAR2/	P2	29	N	Parity 2
WAIT/	P2	30	N	Bus Master Wait State
LOCK/	P1	25	N	Inhibit 2; Disable PROM or ROM

Y = Yes; N = No; P = Possibly (Jumper or Optionally Available)

10.2 ST506/412 Drive Interface

J1/P1 Connector Pin Assignment

Ground Return Pin	Signal Pin	Signal Name
1	2	Reduced Write Current (-)
3	4	Reserved (Head 2^2)
5	6	Write Gate (-)
7	8	Seek Complete (-)
9	10	Track 0 (-)
11	12	Write Fault (-)
13	14	Head Select 2^0 (-)
15	16	Reserved (To J2 Pin 7)
17	18	Head Select 2^1 (-)
19	20	Index (-)
21	22	Ready (-)
23	24	Step (-)
25	26	Drive Select 1 (-)
27	28	Drive Select 2 (-)
29	30	Drive Select 3 (-)
31	32	Drive Select 4 (-)
33	34	Direction In (-)

10.2 ST506/412 Drive Interface (continued)

J2/P2 Connector Pin Assignment

Ground Return Pin	Signal Pin	Signal Name
2	1	Drive Selected (-)
4	3	Reserved
6	5	Reserved
8	7	Reserved
	9,10	Reserved
12	11	GND
	13	MFM Write Data (+)
	14	MFM Write Data (-)
16	15	GND
	17	MFM Read Data (+)
	18	MFM Read Data (-)
20	19	GND

J3/P3 DC-Connector Pin Assignments

Voltage	Ground
Pin 4 +5 VDC	Pin 3 +5 VDC Return

10.3 ESDI Interface

10.3.1 ESDI Stepper Drive Interface

J1/P1 Connector Pin Assignment

Ground Return Pin	Signal Pin	Signal Name
1	2	Head Select 2^3 Change Cartridge
3	4	Head Select 2^2
5	6	Write Gate
7	8	Seek Complete
9	10	Track 00
11	12	Write Fault
13	14	Head Select 2^0
15	16	Sector/Byte Clock/Address Mark Find
17	18	Head Select 2^1
19	20	Index
21	22	Ready
23	24	Step
25	26	Drive Select 1
27	28	Drive Select 2
29	30	Drive Select 3
31	32	Read Gate
33	34	Direction In

J2/P2 Connector Pin Assignment

Ground Return Pin	Signal Pin	Signal Name
	1	Drive Selected
	2	Sector/Byte Clock/Address Mark Find
	3	Seek Complete
	4	Address Mark Enable
6	5	Write-protected
	7,8	Write Clock (±)
	9	Cartridge Changed
12	10,11	Read Reference Clock (±)
15,16	13,14	Write Data (±)
19	17,18	NRZ Read Data (±)
	20	Index

10.3.1 ESDI Stepper Drive Interface (continued)

J3/P3 Connector Pin Assignment

J3 Connector Pin	Voltage
1	+12 VDC (± 5%)
2	+12 Return
3	+5 Return
4	+5 VDC (± 5%)

10.3.2 ESDI Serial Drive Interface

J1/P1 Connector Pin Assignment

Ground Return Pin	Signal Pin	Signal Name
1	2	Head Select 2^3
3	4	Head Select 2^2
5	6	Write Gate
7	8	Configuration/Status Data (-)
9	10	Transfer ACK
11	12	Attention
13	14	Head Select 2^0
15	16	Sector/Byte Clock/Address Mark Find
17	18	Head Select 2^1
19	20	Index
21	22	Ready
23	24	Transfer Request
25	26	Drive Select 1
27	28	Drive Select 2
29	30	Drive Select 3
31	32	Read Gate
33	34	Command Data

10.3.2 ESDI Serial Drive Interface (continued)

J2/P2 Connector Pin Assignment

Ground Return Pin	Signal Pin	Signal Name
	1	Drive Selected
	2	Sector/Byte Clock/Address Mark Find
	3	Command Complete
	4	Address Mark Enable
6	5	Reserved for Step Mode
	7,8	Write Clock (±)
	9	Reserved for Step Mode
12	10,11	Read Reference Clock (±)
15,16	13,14	Write Data (±)
19	17,18	NRZ Read Data (±)
	20	Index

J3/P3 Connector Pin Assignment

J3 Connector Pin	Voltage
1	+12 VDC (± 5%)
2	+12 Return
3	+5 Return
4	+5 VDC (± 5%)

10.4 Floppy Disk Interface

J1/P1 Connector Pin Assignment

Ground Return Pin	Signal Pin	Signal Name
1	2	Option
3	4	In Use
5	6	Drive Select 4
7	8	Index Sector
9	10	Drive Select 1
11	12	Drive Select 2
13	14	Drive Select 3
15	16	Motor On
17	18	Direction Select
19	20	Step
21	22	Write Data
23	24	Write Gate
25	26	Track 00
27	28	Write-protect
29	30	Read Data
31	32	Side Select (SA460 only)
33	34	Drive Status

10.5 QIC-02 Drive Interface

This section describes the QIC-02, 1/4-inch cartridge tape drive interface. The 43x transfers data and commands to and from the device on an 8-bit bidirectional data bus, using asynchronous handshaking techniques to eliminate rigorous timing constraints. This interface supports up to four tape drives.

10.5.1 QIC-02 Interface Signal Connectors

The signal connector on each drive is a 50-pin edge connector. The mating connector is a 3M-type 3415-0001, or equivalent. The signal cable is a 50-pin flat ribbon cable. Use a 3M-type 3365/50 fiat cable, or equivalent.

10.5.2 QIC-02 Interface Signal Levels

All signals to the 43x are the following standard TTL levels:

False: Logic 0 (High) = 2.4 to 5.25 VDC.
True: Logic 1 (Low) = 0.0 to 0.55 VDC.

All signals to each tape drive are the following standard standard TTL levels:

False: Logic 0 (High) = 2.0 to 5.25 VDC.
True: Logic 1 (Low) = 0.0 to 0.80 VDC.

Voltages are measured at each drive connector. The QIC-02 interface supports a maximum cable length of 3 meters.

10.5.3 QIC-02 Signal Terminators

The standard termination is 220 ohms to +5 VDC and 330 ohms to GND or Thevenin equivalent. Resistance tolerance is ± 5%, maximum. The bidirectional data bus and the four control signals from the 43x to the drive terminate at the drive. If you are daisy-chaining multiple drives, terminate the cabling at the last drive in the chain. The bidirectional data bus and the four control signals from the drives to the 43x terminate at the 43x.

10.5.4 QIC-02 Signal Loading

The 43x does not load the interface signal by more than 2.0 mA plus required terminations. No drive loads the interface signal by more than 2.0 mA plus required terminations.

10.5.5 QIC-02 Input/Output Signal Pin Assignments

All odd pins connect to signal ground at the controller. The *To* nomenclature indicates the receiver of the particular signal and is defined as follows:

X = Undefined; B = Bidirectional; D = Drive; and C = Controller (43x)

Pin	Name	To	Description
02	NUS-	X	Not Used – Unconnected Signal Lines.
04	NUS-	X	
06	NUS-	X	
08	NUS-	X	
10	HBP-	B	Host Bus Odd Parity – reserved for optional odd bus parity.
12	HB7-	B	Host Bus Bit 7 – (MSB)
14	HB6-	B	Host Bus Bit 6 –
16	HB5-	B	Host Bus Bit 5 –
18	HB4-	B	Host Bus Bit 4 – Data Bus
20	HB3-	B	Host Bus Bit 3 –
22	HB2-	B	Host Bus Bit 2 –
24	HB1-	B	Host Bus Bit 1 –
26	HB0-	B	Host Bus Bit 0 – (LSB)
28	ONL-	D	*On-line* – 43x-generated control signal. Activated before transferring a Read or Write command and deactivated to terminate the Read or Write command.
30	REQ-	D	*Request* – 43x-generated control signal. Command data was placed on the data bus in Command mode or status was taken from the data bus in status imput mode. The 43x asserts *Request* only if the drive asserts *Ready* or *Exception* (EXC-).
32	REQ-	D	*Reset* – 43x-generated signal. Initiates drive initialization, defaults selection to Device 0, and asserts *Exception*.

10.5.5 QIC-02 Input/Output Signal Pin Assignments (continued)

Pin	Name	To	Description
34	XFR-	D	*Transfer* – 43x-generated control signal. Data was placed on the data bus in write mode or taken from the data bus in read mode.
36	ACK-	C	*Acknowledge* – Drive-generated signal. Data was taken from the data bus in write mode or placed on the data bus in read mode.
38	RDY-	C	*Ready* – Drive-generated signal; indicates one of the following conditions: 1. The drive transferred data from the data bus in command transfer mode. 2. The drive placed data on the data bus in status input mode. 3. The drive completed a BOT, Cartridge Initialization, or Erase command. 4. The drive is ready to receive the next block or a Write or Write File Mark command from the 43x in write mode. 5. The drive completed a Write File Mark command in write file mark mode. 6. The drive is ready to transfer the next block to the 43x or ready to receive a Read or REM from the 43x in read mode. 7. The drive is ready to receive a new command.

10.5.5 QIC-02 Input/Output Signal Pin Assignments (continued)

Pin	Name	To	Description
40	EXC-	C	*Exception* – Drive-generated signal. An exception condition exists in the drive. The 43x *must* issue a Status command and perform a status input.
42	DIR-	C	*Direction* – Drive generated signal. When *false*, the 43x data bus drivers assert their data bus levels and the drive data bus drivers assume high impedance status. When *true*, the 43x data bus drivers assume high impedance states and the drive data bus drivers assert their data bus levels.
44	NUS-	X	Not Used – Unconnected signal line.
46	NUS-	X	Not Used – Unconnected signal line.
48	NUS-	X	Not Used – Unconnected signal line.
50	NUS-	X	Not Used – Unconnected signal line.

10.6 431 Block Diagram

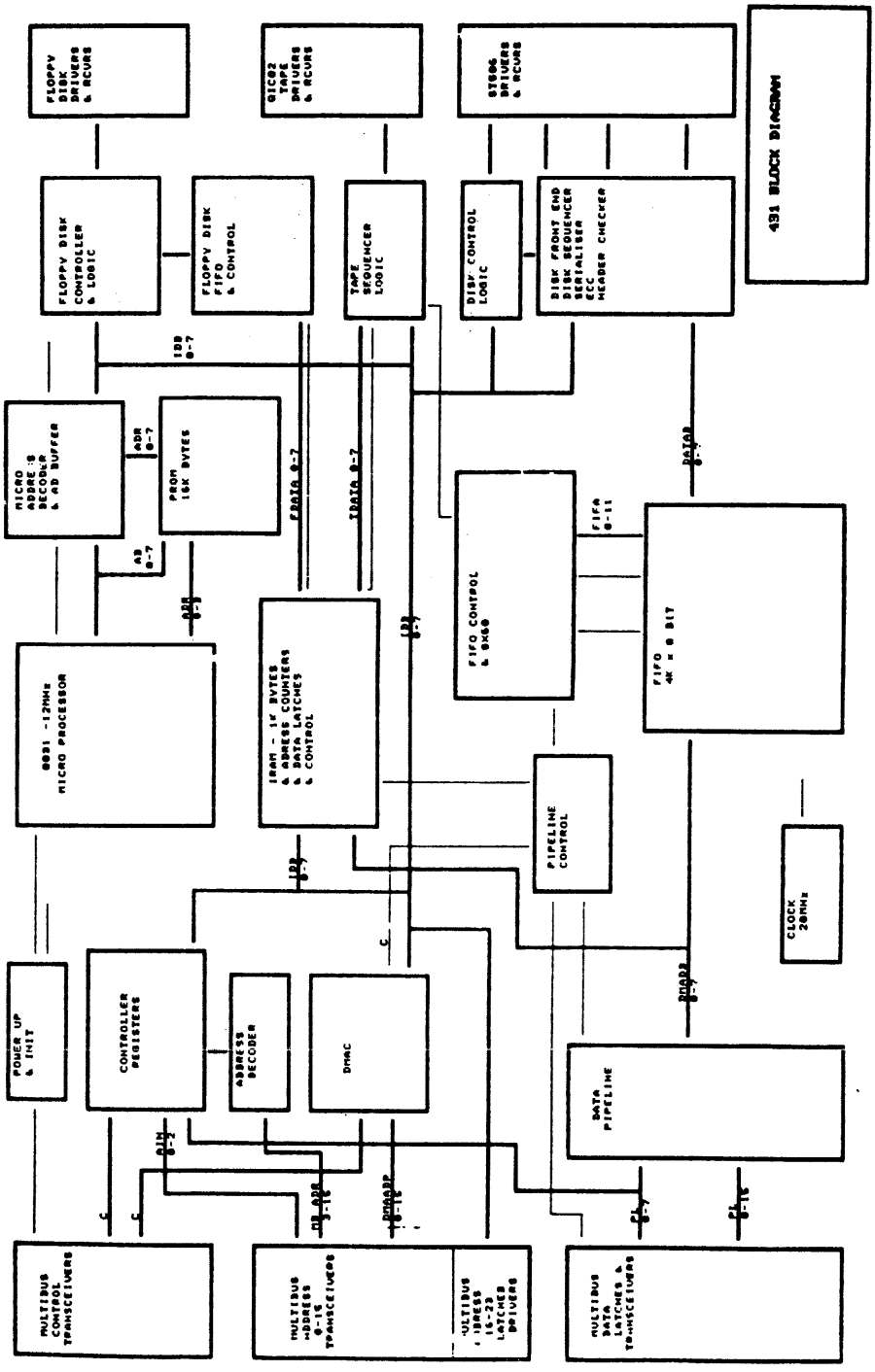


Figure 10–1. 431 Block Diagram

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