XVME-653/658

Single-Slot VMEbus
Intel Pentium®/AMD-K6®-2
Processor Module

P/N 74653-001B

Printed in the United States of America

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A	Manual Released	2/98
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WARNING

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may be required to take adequate measures.

European Union Directive 89/336/EEC requires that this apparatus comply with relevant ITE EMC standards. EMC compliance demands that this apparatus is installed within a VME enclosure designed to contain electromagnetic radiation and which will provide protection for the apparatus with regard to electromagnetic immunity. This enclosure must be fully shielded. An example of such an enclosure is a Schroff 7U EMC-RFI VME System chassis, which includes a front cover to complete the enclosure.

The connection of non-shielded equipment interface cables to this equipment will invalidate European Economic Area (EEA) EMC compliance and may result in electromagnetic interference and/or susceptibility levels that are in violation of regulations which apply to the legal operation of this device. It is the responsibility of the system integrator and/or user to apply the following directions, as well as those in the user manual, which relate to installation and configuration:

> All interface cables should be shielded, both inside and outside of the VME enclosure. Braid/foil type shields are recommended for serial, parallel, and SCSI interface cables. Whereas external mouse cables are not generally shielded, an internal mouse interface cable must either be shielded or looped (1 turn) through a ferrite bead at the enclosure point of exit (bulkhead connector). External cable connectors must be metal with metal backshells and provide 360-degree protection about the interface wires. The cable shield must be terminated directly to the metal connector shell; shield ground drain wires alone are not adequate. VME panel mount connectors that provide interface to external cables (e.g., RS-232, SCSI, keyboard, mouse, etc.) must have metal housings and provide direct connection to the metal VME chassis. Connector ground drain wires are not adequate.

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Chapter 1 – Introduction

The XVME-653 VMEbus Pentium® MMX™ PC-compatible VMEbus processor module and the XVME-658 VMEbus AMD-K6®-2 PC-compatible VMEbus processor module are designed to combine the high performance and ruggedized packaging of the VMEbus with the broad application software base of the IBM PC standard. These modules integrate the latest processor and chipset technology.

At the core of the XVME-653 is an Intel® 233 MHz Pentium CPU with MMX technology. This generation of Pentium processors features enhanced multimedia instructions, larger level 1 caches, and a 10 to 20 percent performance increase over standard Pentium processors.

At the core of the XVME-658 is an AMD 333 MHz K6-2 CPU with 3DNOW!™ Technology. 3DNOW!™ Technology is the first innovation to the x86 processor architecture that significantly enhances floating-point-intensive three-dimensional (3D) graphics performance. The AMD-K6-2 system can provide performance comparable to the many of the Pentium II systems on the market today.

Module Features

The XVME-653 and the XVME-658 offer the following features:

- 233 MHz Intel Pentium MMX CPU (XVME-653)
- 333 MHz AMD-K6-2 CPU with 3DNOW! Technology (XVME-658)
- Up to 256 MB fast-page or EDO DRAM in 72-pin SIMM sites, with ECC or parity
- 512 KB of synchronous level 2 pipeline cache
- High-performance PCI local bus SVGA controller with 2 MB of VRAM
- PCI Enhanced IDE controller with DMA
- 10/100 Mbit PCI Ethernet controller with front RJ-45 connector
- 32-pin site for *DiskOnChip* or battery-backed SRAM
- PCI-to-VMEbus interface with DMA
- Two high-speed 16550-compatible serial ports
- One Universal Serial Bus (USB) port
- EPP or ECP configurable parallel port
- PS/2-style keyboard and mouse ports
- Configurable hardware byte-swapping logic (XVME-658 and XVME-653/31x)
- Expansion options for PC/104, PMC, ISA, and PCI cards

Architecture

This section describes the XVME-653/658 processor modules' architecture.

CPU Chip

The XVME-653 supports the Intel 233 MHz Pentium MMX processor. The MMX processor features new instructions to improve multimedia performance. A dynamic branch prediction unit, improved internal pipelines, and separate 16 KB data and instruction caches further enhance performance.

The XVME-658 supports the AMD 333 MHz K6-2 processor with 3DNOW! Technology. The AMD 333 MHz K6-2 processor incorporates the MMX instruction set as well as the new 3DNOW! Technology instruction set which can increase the speed of floating-point-intensive operations and 3D graphics. In addition, a 64 KB L1 cache, four x86 instructions decoders, a large branch prediction table, and six integer-execution units further enhance performance.

Ethernet Controller

The XVME-653/658 contains a state-of-the-art Intel 82558 10/100 BaseTX Ethernet controller with a 32-bit PCI bus mastering interface to support 100 Mbits per second bus transfers. The RJ-45 connector on the module's front panel provides autosensing for 10BaseT and 100BaseTX connections.

PCI Local Bus Interface

The PCI-to-ISA bridge device provides an accelerated PCI-to-ISA interface that includes a high-performance enhanced IDE controller, PCI and ISA master/slave interfaces, enhanced DMA functions, and a plug-and-play port for onboard devices. The bridge device also provides many common I/O functions found in ISA-based PC systems, including a seven channel DMA controller, two 82C59 interrupt controllers, an 8254 timer/counter, and control logic for NMI generation.

Video Controller

The PCI bus video controller features a 64-bit graphics engine, with 24-bit RAMDAC for true color support. It has 2 MB of VRAM and supports resolutions up to 1280 x 1024 with 256K colors.

Fast IDE controller and Floppy Drive Controller

The enhanced IDE controller supports programmed I/O (PIO) and bus mastering DMA with transfer rates to 22 MB/second. The controller contains an 8 x 32 bit buffer for bus master IDE PCI burst transfers, and will support up to two IDE devices. This controller can also handle a single optional floppy drive device. If present, this floppy drive will be designated Drive A.

Caution

The IDE controller supports enhanced PIO modes, which reduce the cycle times for 16-bit data transfers to the hard drive. Check with your drive manual to see if the drive you are using supports these modes. The higher the PIO mode, the shorter the cycle time. As the IDE cable length increases, this reduced cycle time can lead to erratic operation. As a result, it is in your best interest to keep the IDE cable as short as possible.

The PIO modes are selected in the BIOS setup (see p. 3-4). The Autoconfig will attempt to classify the connected drive if the drive supports the auto ID command. If you experience problems, change the **Transfer Mode:** to *Standard*.

Caution

The total cable length must not exceed 18 inches. Also, if two drives are connected, they must be no more than six inches apart.

VMEbus Interface

The XVME-653/658 uses the PCI local bus to interface to the VMEbus. The VMEbus interface supports full DMA to and from the VMEbus, integral FIFOs for posted writes, block mode transfers, and read-modify-write operations. The interface contains one master and four slave images that can be programmed in a variety of modes to allow the VMEbus to be mapped into the XVME-653/658 local memory. This makes it easy to configure VMEbus resources in protected and real mode programs. The XVME-658 and the XVME-653/31x modules also incorporate onboard hardware byte-swapping (see Table 1-1).

Card Expansion Options

The XVME-653/658 supports optional PMC (PCI Mezzanine Card), PC/104, short ISA, or PCI expansion using XVME-976 expansion modules. The XVME-976/201 provides one PCI Mezzanine Card (PMC) site and one 16-bit PC/104 site. The XVME-976/202 provides one 16-bit short ISA expansion site. The XVME-976/203 provides two PMC sites. The XVME-976/204 provides two 16-bit PC/104 sites. The XVME-976/205 provides one PCI card expansion site. All XVME-976 modules are designed to plug directly into the XVME-653/658 using the 80-pin interboard connectors.

Onboard Memory

DRAM Memory

The XVME-653/658 has two 72-pin SIMM memory sites, providing up to 256 MB of DRAM. The memory sites can be populated with standard fast page mode memory or enhanced data out memory (EDO). EDO memory is designed to improve DRAM read performance. Using EDO memory improves the back-to-back burst timing to 5-2-2-2 from the 5-3-3-3 of standard memory. The XVME-653/658 also supports error checking

and correction (ECC) or parity checking DRAM memory. Approved DRAM suppliers are listed in Appendix A.

Secondary Cache

The XVME-653/658 comes equipped with 512 KB synchronous level 2 pipeline burst cache.

Flash BIOS

The XVME-653/658 system BIOS is contained in a 512 KB flash device to facilitate system BIOS updates. You can program and enable additional areas of the flash device to provide optional ROM support. You should contact Xycom Automation for more information on flashing option ROMs and video ROMs into the BIOS image.

ROM Site

This 32-pin onboard site supports nonvolatile SRAM and *DiskOnChip*.

Nonvolatile SRAM

The board supports 32K x 8 and 128K x 8 nonvolatile SRAM memory sizes. Packaged in a standard 32-pin DIP format, the SRAM contains a built-in battery and battery backup. Battery life is seven years minimum in absence of V_{CC}.

DiskOnChip

The *DiskOnChip* is a single-chip flash disk in a standard 32-pin DIP format. It requires an 8 KB window to view as an extension BIOS. During boot up, the *DiskOnChip* loads its software in the PC memory and installs itself as an additional drive. See Table 1-2 for *DiskOnChip* size options.

Universal Serial Bus Port

The XVME-653/658 incorporates a Universal Serial Bus (USB) port that is compatible with USB devices. The port terminates in a standard two-pin connector.

Serial and Parallel Ports

PC peripherals include two high-speed 16550-compatible serial ports and an ECP or EPP configurable parallel port.

Mouse Port

The XVME-653/658 includes a PS/2-compatible mouse port.

Keyboard Interface

The keyboard interface uses a PS/2-style connector on the front panel. The +5 V is protected with a polyswitch. This device will open up if the +5 V is shorted to GND. Once the shorting condition is removed, the polyswitch will allow current flow to resume.

Hard and Floppy Drives

The XVME-653/658 IDE hard drive and floppy drive signals are routed through the P2 connector, providing a simplified method of connecting external floppy and hard drives. The XVME-653/658 will support only one floppy drive.

When used with the XVME-977 mass storage module, the hard and floppy drives do not need to be located next to the processor. Using the supplied six-inch ribbon cable (which connects the XVME boards' J2 VME backplane connectors), the XVME-977 can be installed up to six slots away from the XVME-653/658 on the VME backplane. This allows greater flexibility in configuring the VMEbus card cage.

For applications that require mass storage outside the VMEbus chassis, the XVME-973/1 drive adapter module plugs onto the VMEbus J2 connector. This module provides industry standard connections for IDE and floppy signals. One floppy drive can be connected to the XVME-973/1. This drive may be 2.88 MB, 1.44 MB, 1.2 MB, or 360 KB in size. For more information on the XVME-973/1, refer to Chapter 5.

Caution

The total cable length must not exceed 18 inches. If two drives are connected, they must be no more than six inches apart.

Watchdog Timer

The XVME-653/658 incorporates a watchdog timer. When enabled, the timer can either generate an interrupt or a master reset, depending on how you configure the watchdog timer port. The timer input needs to be toggled within 1.6 seconds to prevent timeout.

Operational Description

Figure 1-1 is the block diagram for the XVME-653/658.

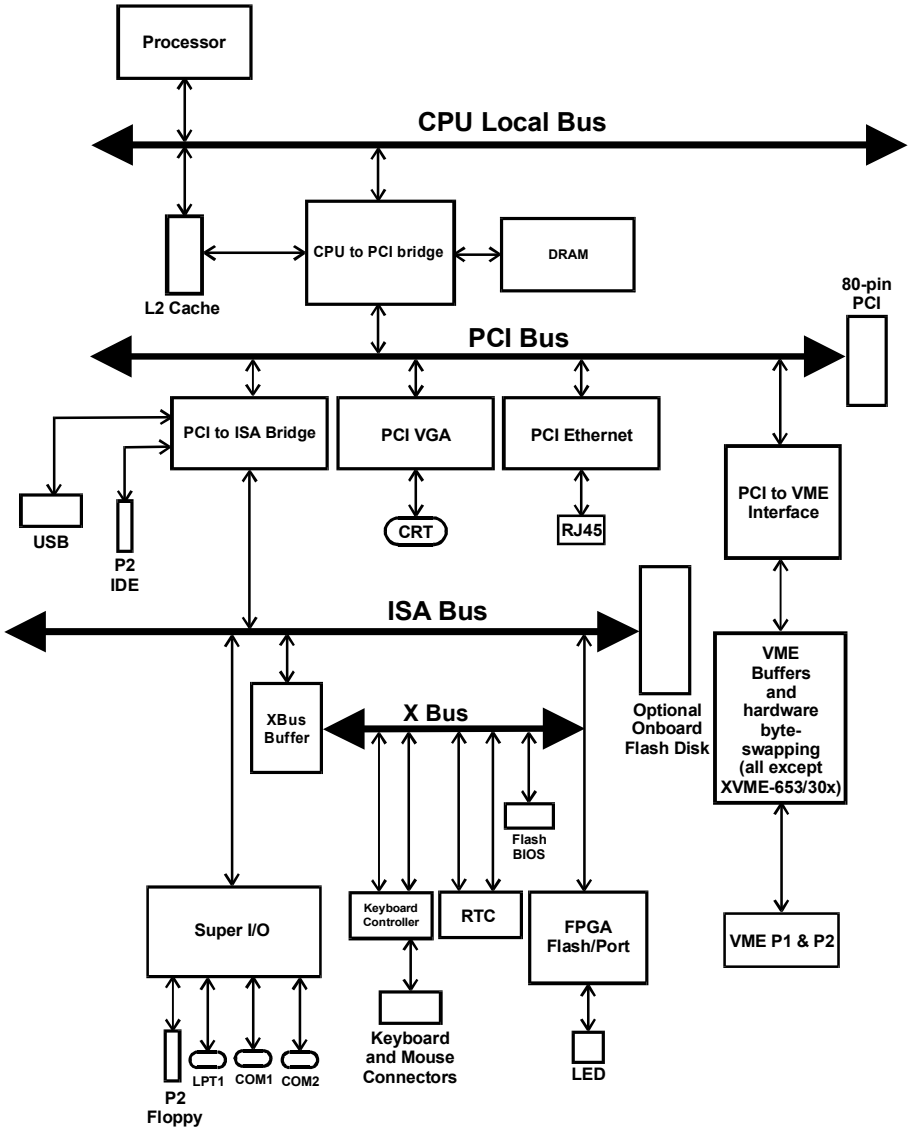


Figure 1-1 XVME-653/658 Block Diagram

Environmental Specifications

Characteristic	Specification
Temperature: Operating (100 cfm airflow) XVME-653 (Intel 233 MHz Pentium) XVME-658 (AMD 333 MHz K6-2) Nonoperating	 0 to 50°C (32 to 122°F) 0 to 45°C (32 to 113°F) -45 to 85°C (-49 to 185°F)
Vibration: Frequency Operating Nonoperating	 5 to 2000 Hz 0.015” (0.38 mm) peak-to-peak displacement 2.5 G (maximum) acceleration 0.030” (0.76 mm) peak-to-peak displacement 5.0 G (maximum) acceleration
Shock: Operating Nonoperating	30 G peak acceleration, 11 msec duration 50 G peak acceleration, 11 msec duration
Humidity	20% to 80% RH, noncondensing

Hardware Specifications

Characteristic	Specification
Power Specifications: +12V -12V +5V: XVME-653 (Intel 233 MHz Pentium) XVME-658 (AMD 333 MHz K6-2)	 75 mA maximum 24 mA maximum 10.59 A (maximum); 5.87 A (typical) 10.59 A (maximum); 6.5 A (typical)
CPU speed: XVME-653 XVME-658	233 MHz 333 MHz
Cache	512 KB pipeline burst cache
Ethernet controller	Intel 82558 10/100 BaseTX Fast Ethernet; RJ-45
PCI Super VGA Graphics Controller	1280 x 1024 maximum resolution, 256 colors; 2 MB VRAM
Serial Ports	RS-232C, 16550 compatible (2) USB (1)
Parallel Interface	EPP/ECP compatible (1)
Onboard memory	Fast-page or EDO DRAM, ECC or parity, up to 256 MB
Regulatory Compliance	European Union Electromagnetic Compatibility - 89/336/EEC

VMEbus Compliance

Complies with VMEbus Specification ANSI/VITA 1–1994
A32/A24/A16:D64/D32/D16/D08(EO) DTB Master
A32/A24/A16:D64/D32/D16/D08(EO) DTB Slave
R(0-3) Bus Requester
Interrupter I(1)-I(7) DYN
IH(1)-IH(7) Interrupt Handler
SYSCLK and SYSRESET Driver
PRI, SGL, RRS Arbiter
RWD, ROR bus release
Form Factor: Double-height, single-width 233 mm x 160 mm (9.2” x 6.3”)

System Configuration and Expansion Options Tables

Your XVME-653/658 can be ordered in a variety of configurations and expanded as well. The following tables show these options.

Table 1-1 XVME-653/658 CPU and DRAM Configurations and Byte-Swapping Hardware

XVME-653 Intel 233 MHz Pentium CPU			XVME-658 AMD 333 MHz K6-2 CPU		
Ordering Number	**Byte-Swapping Hardware?**	**DRAM**		**Byte-Swapping Hardware?**	**DRAM**
XVME-653/310	Yes	None	**XVME-658/310**	Yes	None
XVME-653/313	Yes	32 MB	**XVME-658/313**	Yes	32 MB
XVME-653/314	Yes	64 MB	**XVME-658/314**	Yes	64 MB
XVME-653/315	Yes	128 MB	**XVME-658/315**	Yes	128 MB
XVME-653/316	Yes	256 MB	**XVME-658/316**	Yes	256 MB
XVME-653/300	No	None			
XVME-653/303	No	32 MB			
XVME-653/304	No	64 MB			
XVME-653/305	No	128 MB			
XVME-653/306	No	256 MB			

The ordering number is broken into two parts. The model number is the 653 or 658. The tab number is the three digits after the slash. For the XVME-653/658, the tab number indicates the presence of byte-swapping hardware (the second digit is a one if the unit has byte-swapping hardware, otherwise it is a zero) and the amount of DRAM memory (the third digit). DRAM options are explained more fully in Appendix A.

There are also several expansion options for the XVME-653/658.

Table 1-2 XVME-653/658 Expansion Options

Ordering Number	Description
XVME-973/1	Drive Adapter Module for external drives
XVME-976/201	PMC and PC/104 Expansion Module
XVME-976/202	16-bit short ISA Expansion Module
XVME-976/203	Dual PMC Expansion Module
XVME-976/204	Dual PC/104 Expansion Module
XVME-976/205	PCI Carrier Module
XVME-977	Single-slot Mass Storage Module
XVME-992/8	8 MB *DiskOnChip*
XVME-992/24	24 MB *DiskOnChip*
XVME-992/40	40 MB *DiskOnChip*
XVME-992/72	72 MB *DiskOnChip*
XVME-992/144	144 MB *DiskOnChip*

The XVME-976 expansion modules and the XVME-977 module are described in their own manuals. The XVME-973/1 is described in Chapter 5.

Chapter 2 – Installation

This chapter provides information on configuring the XVME-653/658 modules. It also provides information on installing the XVME-653/658 into a backplane and enabling the Ethernet controller. Figure 2-1 and Figure 2-2 illustrate the jumper, switch, and connector locations on the XVME-653/658. Note that the version of the XVME-653 module without the byte-swapping hardware has three jumpers in slightly different positions.

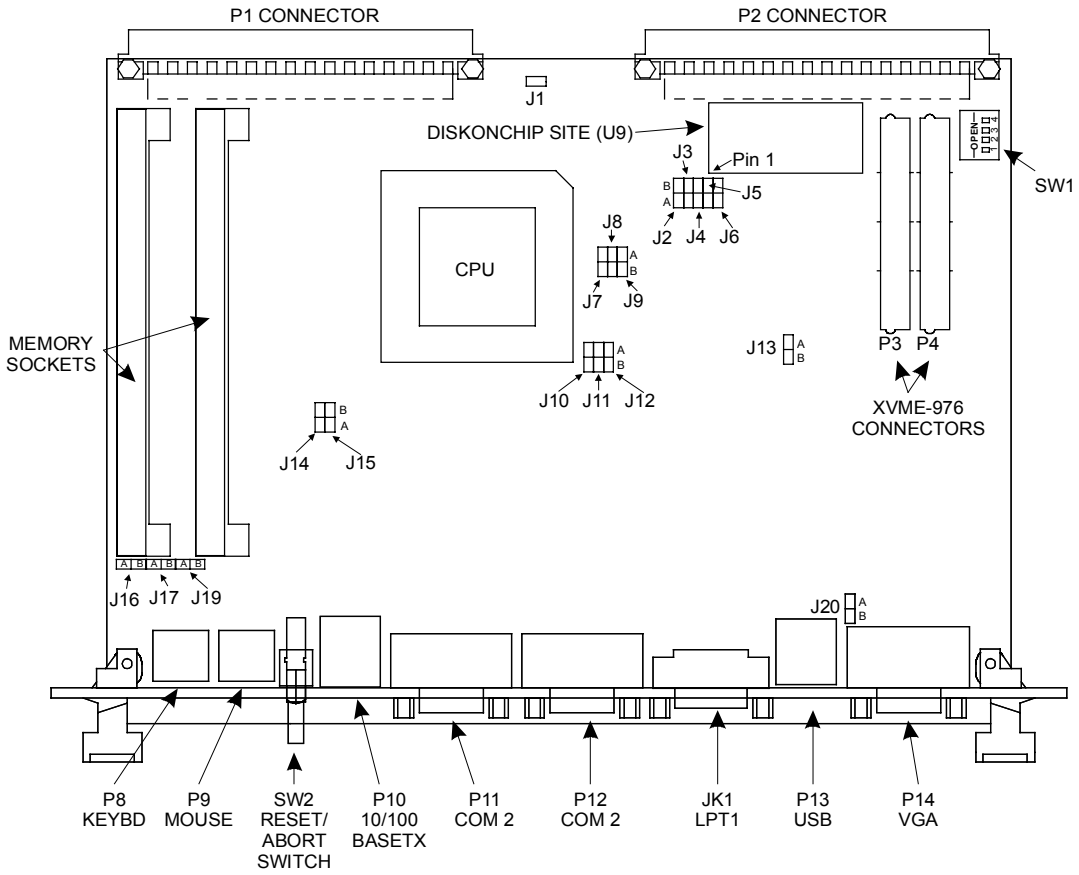


Figure 2-1 XVME-653/658 Jumper, Switch, and Connector Locations

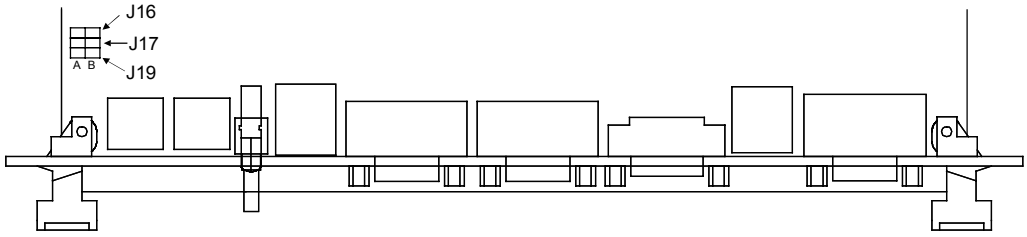


Figure 2-2 J16, J17, and J19 Jumper Locations for XVME-653/30x (no byte-swapping hardware)

Jumper Settings

The following tables list the XVME-653/658 jumpers, their default positions (either checked or labeled by module number), and their functions. Jumper locations are shown in Figure 2-1 and Figure 2-2.

Table 2-1 General Jumper Settings

Jumper	Position	Function
J1	In Out √	Disables system resource function Enables system resource function
J13	A √ B	Reserve 1
J16	A √ B	Boot from Flash Boot from ROM
J17	A B √	Clear CMOS memory Normal CMOS memory
J19	A √ B	Reserve 2
J20	A B √	Reserve 3

CPU Configuration

Table 2-2 CPU Configuration Jumper Settings

Module/Speed	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12
XVME-653/233 MHz	B	A	A	A	A	B	B	B	A	A	A
XVME-658/333 MHz	A	A	B	A	A	B	B	B	B	A	B

CPU Core Voltage

Table 2-3 CPU Core Voltage Jumper Settings

CPU Core Voltage	J2	J3	J4	J5	J6
2.2 V (XVME-658/333 MHz)	A	A	B	A	A
2.8 V (XVME-653/233 MHz)	B	A	A	A	A

CPU Voltage Plane Configuration

Table 2-4 CPU Voltage Plane Configuration Jumper Settings

CPU Configuration	J7	J8	J9
Single Voltage Plane	A	A	A
Split Voltage Planes (XVME-653/658) √	B	B	B

Processor Speed

Table 2-5 Processor Speed Jumper Settings

Processor Speed	J10	J11	J12
3/2x (XVME-653/233 MHz)	A	A	A
5x (XVME-658/333 MHz)	B	A	B

Memory

Table 2-6 Memory Voltage Jumper Settings

Memory	J14	J15
5.0 V √	A	A
3.3 V	B	B

Switch Settings

The XVME-653/658 has one four-pole switch (SW1). This switch controls the system response to the front panel **Reset** switch (SW2). Table 2-7 shows the switch settings required to reset on the XVME-653/658 CPU, to reset only the VME backplane, or to reset both. The switch 3 is reserved and should always be closed. The XVME-653/658 is shipped with all four switches in the closed position (which causes SW2 to reset both the XVME-653/658 and the VME backplane). Both switches are shown on Figure 2-1.

Table 2-7 Four-Pole Switch (SW1) Settings

For the front panel reset switch (SW2) is to do this:	The four-pole switch (SW1) settings must be:		
	1	2	4
No Resets	Closed	Open	Open
Reset the VME backplane only*	Open	Closed	Open
Reset the XVME-653/658 CPU only**	Closed	Open	Closed
Reset both the VME backplane and the XVME-653/658 CPU (default setting)	Closed √	Closed √	Closed √

*Caution

Resetting only the VME backplane will reset the Universe chip.

**Caution

If you have an older XVME-653 which has a Tundra Universe chip instead of a Tundra Universe II chip (U19), you do not have the ability to reset the CPU only. The option to reset both the CPU and the VME backplane still works normally.

You can tell a Universe from a Universe II by looking at the model number on the top of the chip. The Universe has CA91C042-33CE and the Universe II has CA91C142-33CE.

Registers

The XVME-653/658 contains four I/O port registers: 218h, 219h, 233h, and 234h.

Register 218h – Abort/Clear CMOS Port

This register controls the abort toggle switch and allows you to read the CMOS clear jumper (J17).

Table 2-8 Abort/Clear CMOS Port Register Settings

Bit	Signal	Result	R/W
0	RESERVED	Reserved	
1	RESERVED	Reserved	
2	RESERVED	Reserved	
3	RESERVED	Reserved	
4	ABORT_STS	1 = Abort toggle switch caused interrupt	R
5	ABORT_CLR	0 = Clear and disable abort 1 = Enable abort	R/W
6	RESERVED	Reads jumper J13	R
7	CLRCMOS	0 = Clear CMOS 1 = CMOS okay	R

Register 219h – LED/BIOS Port

This register controls the following LEDs and signals.

Table 2-9 LED/BIOS Port Register Settings

Bit	LED/Signal	Result	R/W
0	FAULT	0 = Fault LED on 1 = Fault LED off	R/W
1	PASS	0 = PASS LED off 1 = PASS LED on	R/W
2	FLB_A18_EN	1 = Flash write enabled and A18 is controllable	R/W
3*	FLB_A18/reserve2	Reads jumper J19 when FLB_A18_EN = 0 Flash BIOS address A18 when FLB_A18_EN = 1	R/W
4	RESERVED	Reserved	
5	BIOS_D0	1 = Enable UPPER on board BIOS area @D0000	R/W
6	RESERVED	Reserved	
7	RESERVED	Reserved	

***Note**

A18, along with control ROM/RAM 15-17 are to be used to page the Flash when FLB_A18_EN is asserted.

Register 233h – Watchdog Timer Port

This register controls watchdog timer operation.

Table 2-10 Watchdog Timer Port Register Settings

Bit	Signal	Result
0	RESERVED	Reserved
1	RESERVED	Reserved
2	RESERVED	Reserved
3	RESERVED	Reserved
4	WDOG_EN	Enables the watchdog timer
5	MRESET_EN	Timeout generates reset when asserted
6	WDOG_STS	Watchdog timer status bit
7	WDOG_CLR	Clears the watchdog timer

Register 234h – NVRAM and DiskOnChip Port

This register controls access to either the NVRAM or the *DiskOnChip* (DOC) component. Bits 7 and 8 also control the byte swapping on XVME-653/658 modules that are equipped with byte-swapping hardware. In XVME-653/30x modules without byte-swapping hardware, bits 7 and 8 are RESERVED.

Table 2-11 NVRAM and DiskOnChip Port Register Settings

Bit	Signal	Result
0	Control ROM/RAM15	ROM address 15 - page control bit
1	Control ROM/RAM16	ROM address 16 - page control bit
2	Control ROM/RAM17	ROM address 17 - page control bit
3	DOC enable	Enables DOC mode
4	Range select 0	
5	Range select 1	
6	SWAPS	1 = No swapping (data invariant) occurs during Slave cycles (This byte can only be set for byte-swapping modules.)
7	SWAPM	1 = No swapping (data invariant) occurs during Master cycles (This byte can only be set for byte-swapping modules.)

The following ranges are defined by bits 4 and 5 in register 234h.

Table 2-12 Register 234h Defined Ranges

Range Select Bits	Range
00	No range
01	CC000-CFFFF
10	D0000-D7FFF
11	D8000-DFFFF

Connectors

This section provides the pinouts for the XVME-653/658 connectors. Refer to the EMC warning at the beginning of this manual before attaching cables.

Serial Port Connectors

Table 2-13 Serial Port Connector Pinout

COM1		COM2	
Pin	**Signal**	**Pin**	**Signal**
1	DCD1	1	DCD2
2	RXD1	2	RXD2
3	TXD1	3	TXD2
4	DTR1	4	DTR2
5	GND	5	GND
6	DSR1	6	DSR2
7	RTS1	7	RTS2
8	CTS1	8	CTS2
9	RI1	9	RI2

Parallel Port Connector

Table 2-14 Parallel Port Connector Pinout

Pin	Signal	Pin	Signal
1	STROBE	14	AUTOFEED
2	PDOUT0	15	PERROR
3	PDOUT1	16	INIT
4	PDOUT2	17	SELIN
5	PDOUT3	18	GND
6	PDOUT4	19	GND
7	PDOUT5	20	GND
8	PDOUT6	21	GND
9	PDOUT7	22	GND
10	PACK	23	GND
11	PBUSY	24	GND
12	PE	25	GND
13	SELECT		

USB Port Connector

Table 2-15 USB Port Connector Pinout

Pin	Signal
1A	+5V
2A	USBP0-
3A	USBP0+
4A	GND
1B	+5V
2B	USBP1-
3B	USBP1+
4B	GND

VGA Connector

Table 2-16 VGA Connector Pinout

Pin	Signal
1	RED
2	GREEN
3	BLUE
4	NC
5	GND
6	GND
7	GND
8	GND
9	25MIL_VIDA
10	GND
11	NC
12	LDDCDAT
13	HYSNC
14	VSYNC
15	LDDCCLK

Keyboard Port Connector

Table 2-17 Keyboard Port Connector Pinout

Pin	Signal
1	DATA
2	NC
3	GND
4	+5V
5	CLK
6	NC

Auxiliary Connector

The auxiliary port accepts a PS/2-compatible mouse, track ball, etc.

Table 2-18 Auxiliary Port Connector Pinout

Pin	Signal
1	DATA
2	NC
3	GND
4	VCC
5	CLK
6	NC

VMEbus Connectors

P1 and P2 are the VMEbus connectors.

P1 Connector

Table 2-19 P1 Connector Pinout

Pin	A	B	C
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	NC	A17
22	IACKOUT*	NC	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	NC	+12V
32	+5V	+5V	+5V

P2 Connector

Table 2-20 P2 Connector Pinout

Pin	A	B	C
1	+5V	+5V	HDBRSTDRV*
2	+5V	GND	HDD0
3	+5V	RES	HDD1
4	RES	VA24	HDD2
5	RES	VA25	HDD3
6	RES	VA26	HDD4
7	RES	VA27	HDD5
8	RES	VA28	HDD6
9	RES	VA29	HDD7
10	RES	VA30	HDD8
11	RES	VA31	HDD9
12	RES	GND	HDD10
13	RES	+5V	HDD11
14	RES	VD16	HDD12
15	RES	VD17	HDD13
16	RES	VD18	HDD14
17	RES	VD19	HDD15
18	RES	VD20	GND
19	GND	VD21	HDIOW*
20	FRWC*	VD22	HDIOR*
21	IDX*	VD23	HDIORDY
22	MO0*	GND	+5V (10K pullup)
23	HDRQ0	VD24	IRQ14
24	FDS0*	VD25	RES
25	HDACK0*	VD26	DA0
26	FDIRC*	VD27	DA1
27	FSTEP*	VD28	DA2
28	FWD*	VD29	CS1P*
29	FWE*	VD30	CS3P*
30	FTK0*	VD31	RES
31	FWP*	GND	FHS*
32	FRDD*	+5V	DCHG*

Interboard Connector 1 (P4)

Table 2-21 Interboard Connector 1 Pinout

Pin	Signal	Pin	Signal
1	SYSCLK	41	SA10
2	OSC	42	SA11
3	SD(15)	43	SA12
4	SD(14)	44	SA13
5	SD(13)	45	SA14
6	SD(12)	46	SA15
7	SD(11)	47	SA16
8	SD(10)	48	SA17
9	SD(9)	49	SA18
10	SD(8)	50	SA19
11	MEMW*	51	BALE
12	MEMR*	52	TC
13	DRQ5	53	DACK2*
14	DACK5*	54	IRQ3
15	DRQ6	55	IRQ4
16	DACK6*	56	SBHE*
17	LA17	57	IRQ5
18	LA18	58	IRQ6
19	LA19	59	IRQ7
20	LA20	60	REF*
21	LA21	61	DRQ1
22	LA22	62	DACK1*
23	LA23	63	RESETDRV
24	IRQ14	64	IOW*
25	IRQ15	65	IOR*
26	IRQ12	66	SMEMW*
27	IRQ11	67	AEN
28	IRQ10	68	SMEMR*
29	IOCS16*	69	IOCHRDY
30	MEMCS16*	70	SD0
31	SA0	71	SD1
32	SA1	72	SD2
33	SA2	73	SD3
34	SA3	74	SD4
35	SA4	75	SD5
36	SA5	76	SD6
37	SA6	77	SD7
38	SA7	78	DRQ2
39	SA8	79	IRQ9
40	SA9	80	IOCHCK*

Interboard Connector 2 (P3)

This connector provides power through the center pins.

Table 2-22 Interboard Connector 2 Pinout

Pin	Signal	Pin	Signal
1	TCLK	41	AD23
2	TRST*	42	AD22
3	TMS	43	AD21
4	TDO	44	AD20
5	TDI	45	AD19
6	PCI-RSVD9A (Pn2-8)	46	AD18
7	PCI-RSVD10B (Pn2-9)	47	AD17
8	PCI-RSVD11A (Pn2-10)	48	AD16
9	PCI-RSVD14A (Pn1-12)	49	BE2*
10	PCI-RSVD14B (Pn1-10)	50	FRAME*
11	PCI-RSVD19A (Pn2-17)	51	IRDY*
12	PMC-RSVD_Pn2-34	52	TRDY*
13	PMC-RSVD_Pn2-52	53	DEVSEL*
14	PMC-RSVD_Pn2-54	54	STOP*
15	PCICLK3	55	PLOCK*
16	PIRQA*	56	PERR*
17	PIRQB*	57	SDONE
18	PIRQC*	58	SBO*
19	PIRQD*	59	SERR*
20	REQ3*	60	PAR
21	PCICLK2	61	BE1*
22	REQ1*	62	AD15
23	GNT3*	63	AD14
24	PCICLK1	64	AD13
25	GNT1*	65	AD12
26	PCIRST*	66	AD11
27	PCICLK0	67	AD10
28	GNT0*	68	AD9
29	REQ0*	69	AD8
30	REQ2*	70	BE0*
31	AD31	71	AD7
32	AD30	72	AD6
33	AD29	73	AD5
34	AD28	74	AD4
35	AD27	75	AD3
36	AD26	76	AD2
37	AD25	77	AD1
38	AD24	78	AD0
39	BE3*	79	ACK64*
40	GNT2*	80	REQ64*

Installing the XVME-653/658 into a Backplane

This section provides the information necessary to install the XVME-653/658 into the VMEbus backplane. The XVME-653/658 is a double-high, single board VMEbus module that occupies one VMEbus slot.

Note

Xycom Automation XVME modules are designed to comply with all physical and electrical VMEbus backplane specifications.

Caution

Do not install the XVME-653/658 on a VMEbus system without a P2 backplane.

Warning

Never install or remove any boards before turning off the power to the bus and all related external power supplies.

1. Disconnect all power supplies to the backplane and the card cage. Disconnect the power cable.
2. Make sure backplane connectors P1 and P2 are available.
3. Verify that all jumper settings are correct.
4. Verify that the card cage slot is clear and accessible.
5. Install the XVME-653/658 in the card cage by centering the unit on the plastic guides in the slots (P1 connector facing up). Push the board slowly toward the rear of the chassis until the P1 and P2 connectors engage. The board should slide freely in the plastic guides.

Caution

Do not use excessive force or pressure to engage the connectors. If the boards do not properly connect with the backplane, remove the module and inspect all connectors and guide slots for damage or obstructions.

6. Secure the module to the chassis by tightening the machine screws at the top and bottom of the board.
7. Connect all remaining peripherals by attaching each interface cable into the appropriate connector on the front of the XVME-653/658 board as shown in Table 2-23.
8. Turn on power to the VMEbus card cage.

Table 2-23 Front Panel Connector Labels

Connector	Label
Keyboard	KEYBD
Mouse	MOUSE
Ethernet cable	100BT
Serial devices	COM 1, COM 2
Parallel device	LPT1
USB cable	USB
Display cable	VGA

Note

The floppy drive and hard drive are either cabled across P2 to the XVME-977 disk unit, or they are connected to the XVME-973/1 board. Refer to Chapter 5 for more information on the XVME-973/1.

Figure 2-3 illustrates the XVME-653/658 front panel, to help you locate connectors.

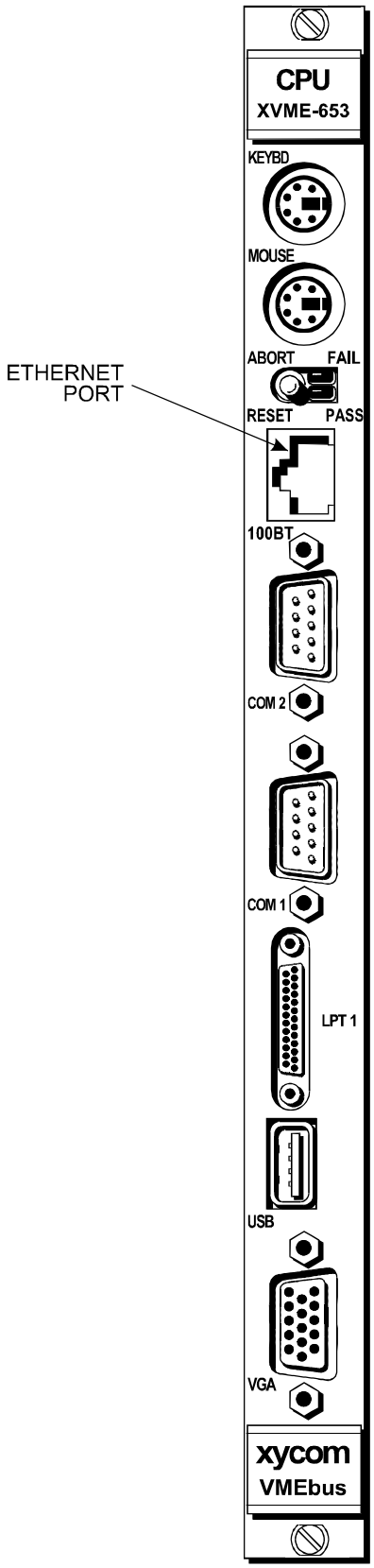


Figure 2-3 XVME-653/658 Front Panel

Enabling the PCI Ethernet Controller

The XVME-653/658 incorporates a high-performance 32-bit PCI bus mastering Ethernet controller.

Loading the Ethernet Driver

To enable the Ethernet controller, you must load the applicable Ethernet driver for your operating system. Refer to the READMEFIRST.TXT file on the Intel 558 Ethernet Drivers disk for installation instructions. For best results, always use the supplied drivers.

Pinouts for the RJ-45 10/100 BaseT Connector

Table 2-24 RJ-45 10/100 BaseT Connector Pinout

Pin	Signal
1	TX+
2	TX-
3	RX+
4	GND
5	GND
6	RX-
7	GND
8	GND

Using a *DiskOnChip*

The *DiskOnChip* device is a self-contained solid-state disk drive that is packaged in a 32-pin device. It can be plugged into the onboard SRAM/Flash socket.

Perform the following steps to configure the XVME-653/658 to use a *DiskOnChip*:

1. Plug the *DiskOnChip* into socket U9 on the CPU module. Be sure the direction is correct (pin 1 of the *DiskOnChip* is aligned with pin 1 of the socket).
2. Turn on the system and enter the BIOS setup menus. (See Chapter 3 for information on accessing the BIOS setup menus.)
3. Select the Advanced menu option from the BIOS Setup main screen.
4. Select the Integrated peripherals option.
5. Select the 32-pin ROM site option.
6. Set the 32-pin ROM site type to DiskOnChip.
7. Set the 32-pin ROM site address to the desired value.
8. Exit the BIOS setup menus and reboot the system.

If the *DiskOnChip* is the only drive in the system, it will appear as the first disk (drive C: in DOS). If there are other drives in the system, the *DiskOnChip* will appear by default as the last drive, unless it is programmed as the first drive.

If you want the *DiskOnChip* to be bootable, copy the operating system files into it using the standard DOS command (for example *sys d*).

The *DiskOnChip* works with MS-DOS, Windows 3.11, and Windows NT. To fit a version of Windows NT onto the *DiskOnChip* (72 MB minimum), reduce the size of the Windows NT space requirement with a utility such as VenturCom *Component Integrator*™. If you use another operating system, please visit the M-Systems web site at *www.m-sys.com* or contact Xycom Automation Application Engineering at 734-429-4971.

Chapter 3 – BIOS Setup Menus

The XVME-653/658 customized BIOS is designed to surpass the functionality provided for normal PCs. This custom BIOS allows you to access the value-added features on the XVME-653/658 module without interfacing to the hardware directly.

Getting to the BIOS Setup Menus

If the setup prompt is disabled on your system (the default setting) press F2 repeatedly after the memory tests and before your system loads the operating system in order to access the main menu.

If the setup prompt is enabled on your system, the BIOS displays the following message: *Press F2 to enter Setup*. Once this message appears, press F2 to access the main menu.

The BIOS Main Setup Menu is shown on the next page.

Moving through the Menus

General instructions for navigating through the screens are described below:

Key	Result
F1 or ALT-H	Accesses the general Help window
ESC	Exits the menu
← or → arrow keys	Selects a different menu
↑ or ↓ arrow keys	Moves the cursor up or down
TAB or SHIFT-TAB	Cycles the cursor up or down
HOME or END	Moves the cursor to the top or bottom of the window
PGUP or PGDN	Moves the cursor to the next or previous page
F5 or -	Selects the previous value for the field
F6 or + or SPACE	Selects the next value for the field
F9	Loads the default configuration values for the menu
F10	Loads the previous configuration values for the menu
ENTER	Executes the Command or Selects a ▸ Submenu

To select an item, use the arrow keys to move the cursor to the field you want. Then use the TAB, SHIFT-TAB, or ENTER keys to select a subfield, if any. Then use the + and – keys or the F5 and F6 keys to select a value for that field. The **Save Changes** commands in the **Exit Menu** save the values currently displayed in all the menus.

To display a submenu, use the arrow keys to move the cursor to the submenu you want. Then press ENTER. A triangle bullet (▸) indicates a submenu.

BIOS Main Setup Menu

PhoenixBIOS Setup–Copyright 1985-95 Phoenix Technologies Ltd.

Main Advanced Security VMEbus Exit

		Item Specific Help
System Time:	[16:19:20]	
System Date:	[03/02/95]	
Diskette A:	[1.44 MB, 3½"]	*If the line item you are viewing*
▸ IDE Adapter 0 Master	(C: 260 Mb)	*has specific help, it will be listed*
▸ IDE Adapter 0 Slave	(D:105 Mb)	*here.*
▸ IDE Adapter 1 Master	(None)	
▸ IDE Adapter 1 Slave	(None)	
Video System:	[EGA/VGA]	
▸ Memory Cache		
▸ Memory Shadow		
▸ Boot sequence:	[A: then C:]	
▸ Numlock:	[Auto]	
System Memory:	640 KB	
Extended Memory:	63 MB	

F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults

ESC Exit ←→ Select Menu Enter Select ▸ Submenu F10 Previous Values

Figure 3-1 Main Setup Menu

Note

IDE Adapter 1 (the secondary IDE controller) is not available to the XVME-653/658.

Table 3-1 Main Setup Menu Options

Option	Description
System Time (HH/MM/SS)	Sets the real-time clock for hour, minute, and seconds. The hour is calculated according to the 24 hour military clock (i.e., 00:00:00 through 23:59:59). Use TAB to move right and SHIFT-TAB to move left. The ENTER key may be used to move from one field to the next. The numeric keys, 0-9, are used to change the field values. The F6 and the + keys may also be used to increment the values, while the F5 and the – keys may be used to decrement them. It is not necessary to enter the seconds or type zeros in front of numbers.
System Date (MM:DD:YYYY)	Sets the real-time clock for the month, day, and year. Use TAB to move right and SHIFT-TAB to move left. The ENTER key may be used to move from one field to the next. The numeric keys, 0-9, are used to change the field values. The F6 and the + keys may also be used to increment the values, while the F5 and the – keys may be used to decrement them. It is not necessary to type zeros in front of numbers.
Diskette A or B	Selects the floppy disk drive installed in your system. The XVME-653/658 can only support one floppy drive (Drive A).
Video System	Selects the default video device.
System Memory	Displays the amount of conventional memory detected during bootup. This field is not user configurable.
Extended Memory	Displays the amount of extended memory detected during bootup. This field is not user configurable.

IDE Adapter 0 Master and Slave Submenus

The IDE Adapter 0 Master and Slave submenus are used to configure IDE hard drive information. If only one drive is attached to the IDE adapter, then only the parameters in the Master Submenu need to be entered. If two drives are connected, both Master and Slave Submenu parameters will need to be entered. The Master and Slave Submenus contain the same information.

PhoenixBIOS Setup–Copyright 1985-95 Phoenix Technologies Ltd.

Main

IDE Adapter 0 Master (C: 850 Mb)		Item Specific Help
Autotype Fixed Disk:	[Press Enter]	
Type:	[User] 850 Mb	
Cylinders:	[1647]	*If the line item you are viewing*
Heads:	[16]	*has specific help, it will be listed*
Sectors/Track:	[63]	*here.*
Write Precomp:	[None]	
Multi-Sector Transfers:	[8 Sectors]	
LBA Mode Control:	[Enabled]	
32 Bit I/O:	[Disabled]	
Transfer Mode:	[Standard]	

F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults

ESC Exit ←→ Select Menu Enter Select ▸ Submenu F10 Previous Values

Figure 3-2 IDE Adapter Submenu

Table 3-2 IDE Adapter Submenu Options

Option	Description
Autotype Fixed Disk	Reads the hard disk parameters from the drive if you press ENTER. It then sets the Type field to User and lets you edit the other fields. Do not attempt to manually set the disk drive parameters unless instructed to do so by Xycom Application Engineering.
Type	Options include *1 to 39*, *User*, or *Auto*. The *1 to 39* option fills in all remaining fields with values for predefined disk type. *User* prompts you to fill in remaining fields. *Auto* autotypes at each boot, displays settings in setup menus, and does not allow you to edit the remaining fields.
Cylinders	Indicates the number of cylinders on the hard drive. This information is automatically entered if the Autotype Fixed Disk option is set.
Heads	Indicates the number of read/write heads on the hard drive. This information is automatically entered if the Autotype Fixed Disk option is set.
Sectors/Track	Indicates the number of sectors per track on the hard drive. This information is automatically entered if the Autotype Fixed Disk option is set.
Write Precomp	This value is not used or required by IDE hard drives.
Multi-Sector Transfers	Sets the number of sectors per block. Options are *Auto*, *2*, *4*, *8*, or *16* sectors. *Auto* sets the number of sectors per block to the highest number supported by the drive.
LBA Mode Control	Enables Logical Block Access. The default (*Disabled*) should work with most hard drives.
32 Bit I/O	Enables 32-bit communication between CPU and IDE interface.
Transfer Mode	Selects the method for transferring the data between the hard disk and system memory. Available options are determined by the drive type and cable length.

Memory Cache Submenu

Enabling cache increases CPU performance by holding data most recently accessed in a special high-speed static RAM area called cache. The XVME-653/658 provides two levels of cache memory; level one is internal to the CPU (see **CPU Chip** on p. 1-2), and level two (external cache) is 512 KB of high-speed cache memory.

```
        PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.

     Main

                    Memory Cache                        Item Specific Help

External Cache:              [Enabled]

Cache System BIOS area:      [Enabled]
Cache Video BIOS area:       [Enabled]                  If the line item you are viewing
                                                        has specific help, it will be listed
Cache Memory Region                                     here.
  CC00-CFFF:                 [Disabled]
  D000-D3FF:                 [Disabled]
  D400-D7FF:                 [Disabled]
  D800-DBFF                  [Disabled]
  DC00-DFFF:                 [Disabled]

F1   Help      ↑↓  Select Item    -/+   Change Values        F9   Setup Defaults
ESC  Exit      ←→  Select Menu    Enter Select ▸ Submenu     F10  Previous Values
```

Figure 3-3 Memory Cache Submenu

Table 3-3 Memory Cache Submenu Options

Option	Description
External Cache	Controls the state of external cache memory. The system BIOS automatically disables external cache if it is not installed. The default is *Enabled*.
Cache System BIOS Area	Allows the system BIOS memory area to be cached if *Enabled*. Enabling also increases system performance. The default is *Enabled*.
Cache Video BIOS Area	Allows the video BIOS memory area to be cached if *Enabled*. Enabling also increases system performance. The default is *Enabled*.
Cache Memory Region	Caches the corresponding memory when *Enabled*. Memory in this area is usually extended BIOS or AT-bus memory. Enabling cache may increase system performance, depending on how the extended BIOS is accessed. The default is *Disabled*.

Memory Shadow Submenu

The summary screen displays the amount of shadow memory in use. Shadow memory is used to copy system and/or video BIOS into RAM to improve performance. The XVME-653/658 displays the number of KB allocated to Shadow RAM on the summary screen. The System Shadow field, which is not editable, is for reference only.

The XVME-653/658 is shipped with both the system BIOS and video BIOS shadowed.

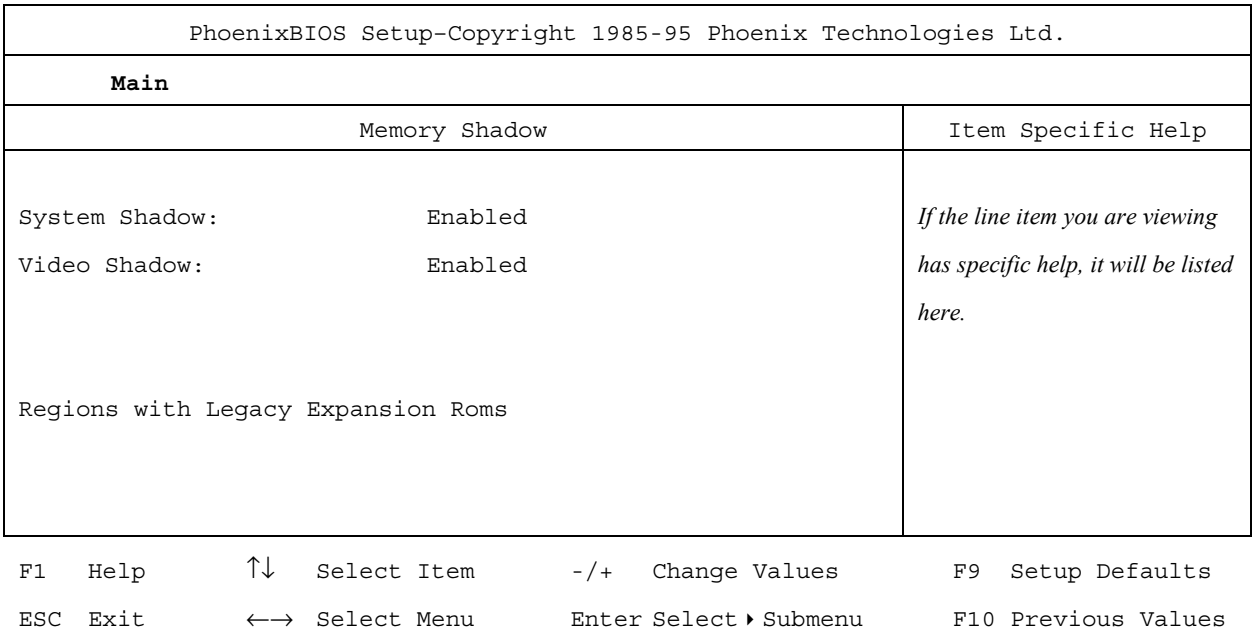


Figure 3-4 Memory Shadow Submenu

Table 3-4 Memory Shadow Submenu Options

Option	Description
System Shadow	Permanently *Enabled*.
Video Shadow	Permanently *Enabled*.
Regions with Legacy Expansion ROMs	Regions are listed below the header if detected by the BIOS

Boot Sequence Submenu

This menu allows the boot sequence to be configured.

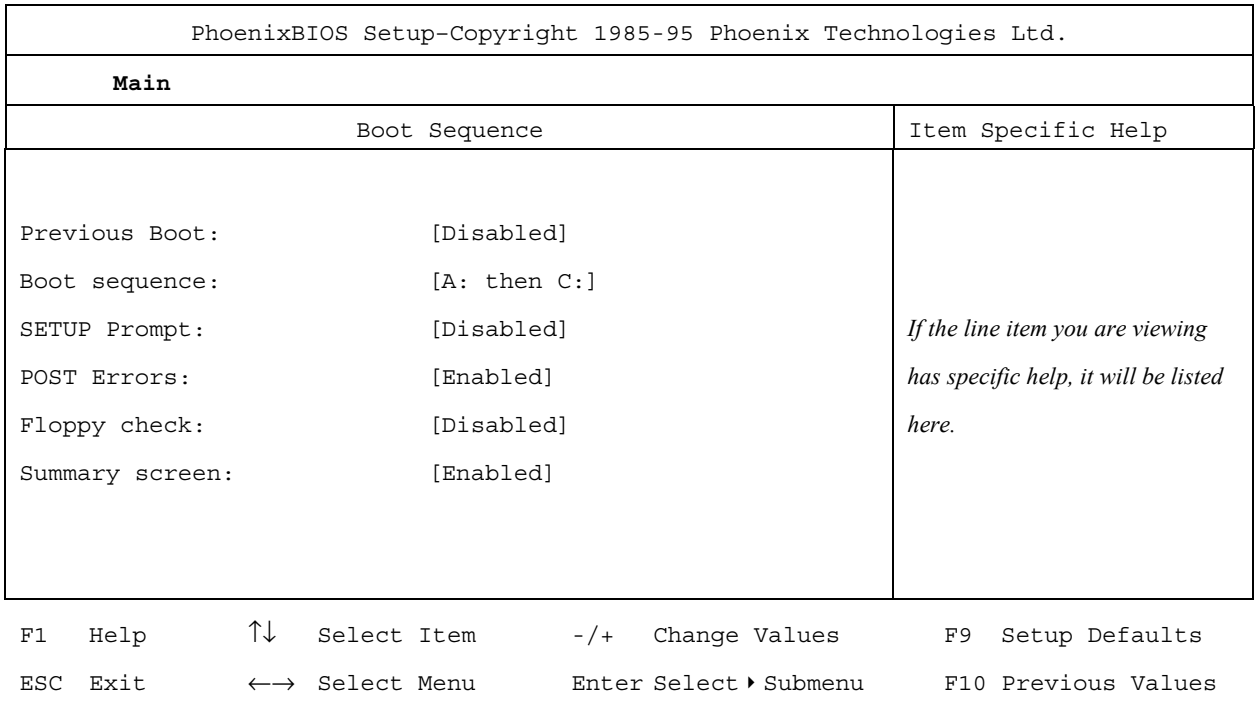


Figure 3-5 Boot Sequence Submenu

Table 3-5 Boot Sequence Submenu Options

Option	Description
Previous Boot	Detects if a boot sequence was not completed properly, if *Enabled*. An incomplete boot may be caused by a power failure, a reset during bootup, or an invalid CMOS configuration. If the BIOS detects this condition, it will display the following message: *Previous boot incomplete – Default configuration used.* The system will be rebooted using the default configuration. If this option is *Disabled*, the system BIOS will not detect an incomplete boot. As a result, the system may not boot if the CMOS settings are wrong. The default is *Disabled*.
Boot Sequence	Attempts to load the operating system from the disk drives in the sequence selected here. The default is *A: then C:*.
Setup Prompt	Displays the message *Press <F2> for Setup* during boot up. The default is *Disabled*.
POST Errors	Halts the system if it encounters a boot error when *Enabled*, and will display *Press <F1> to resume, <F2> for Setup*. The default is *Enabled*.
Floppy Check	Seeks diskette drives on the system during boot up if *Enabled*. Disabling speeds boot time. The default is *Disabled*.
Summary Screen	Displays system summary screen during boot up, when *Enabled*. The default is *Enabled*. This screen is a standard Phoenix BIOS screen and provides information on the following items: Processor Type Coprocessor Type BIOS Date System ROM Address System RAM Extended RAM Shadow RAM Cache RAM COM Ports LPT Ports Display Type Hard Disk 0 Hard Disk 1 Diskette A Diskette B

Numlock Submenu

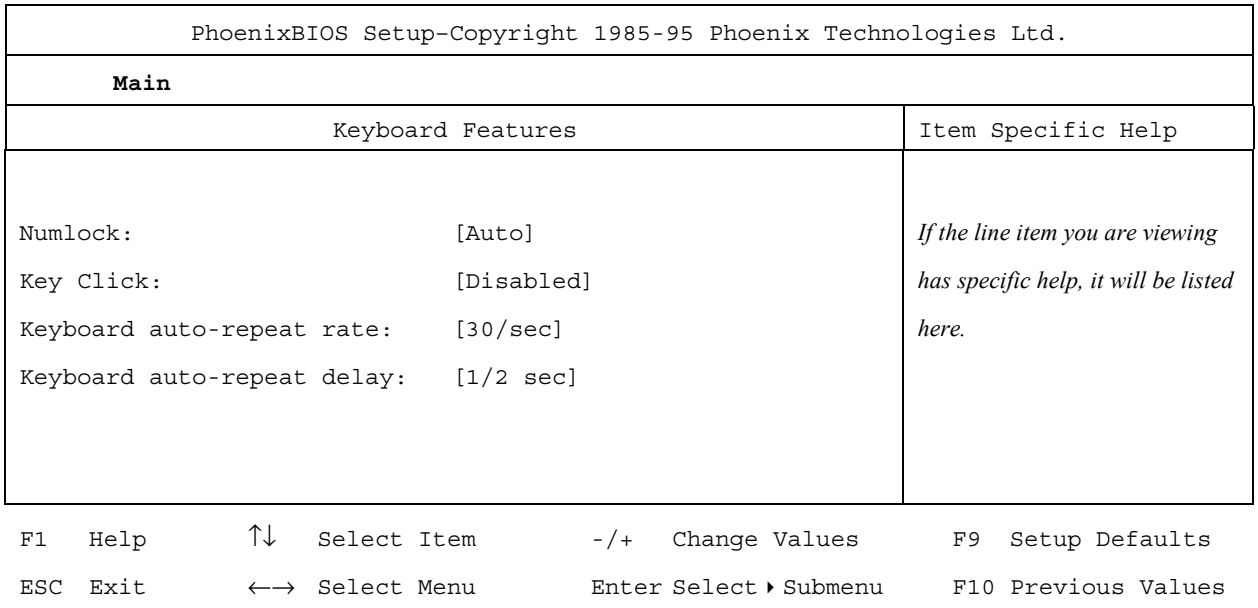


Figure 3-6 Numlock Submenu

Table 3-6 Numlock Submenu Options

Option	Description
Numlock	Determines how the BIOS defines the numlock key at power up or soft reset. Normally, the BIOS sets the numlock on (numeric keys selected) if it detects a 101- or 102-key keyboard at power up. If it detects an 84-key keyboard, it turns numlock off (cursor keys selected). Select *Auto* to keep this state, *On* to select the numeric keys regardless of keyboard, or *Off* to select cursor keys regardless of keyboard. The default is *Auto*.
Keyboard click	Provides audible keypress feedback by having the BIOS click through the system speaker every time a key is pressed, if *Enabled*. This option is only valid for systems with a speaker connected to the speaker jack. The default is *Disabled*.
Keyboard auto-repeat rate	Defines the rate at which the keyboard repeats while a key is pressed. The higher the number, the faster the key repeats. The default is *30/sec*, or 30 times per second.
Keyboard auto-repeat delay	Sets the delay time after a key is held down, before it begins to repeat the keystroke. The default is a *1/2 sec*.

Advanced Menu

This menu allows you to change the peripheral control, advanced chipset control, and disk access mode.

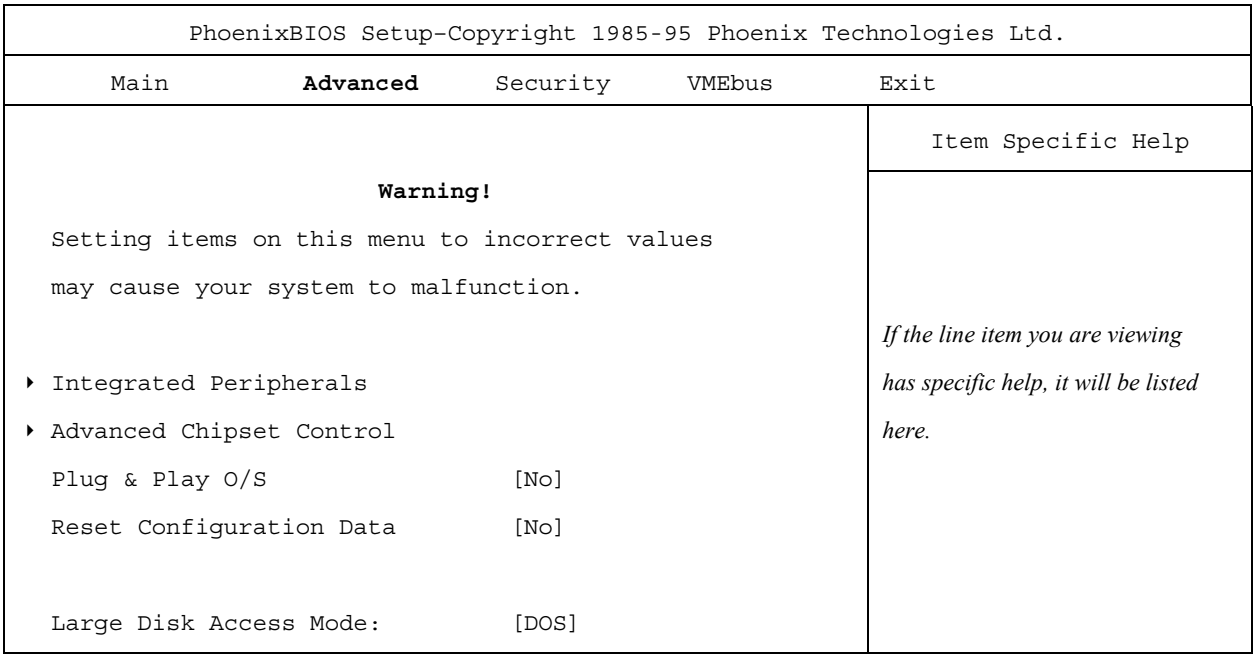


Figure 3-7 Advanced Setup Menu

Table 3-7 Advanced Menu Options

Feature	Description
Plug & Play O/S	Select *Yes* if you are using an operating system with Plug & Play capabilities (such as Windows 95).
Reset Configuration Data	Used to reset the Plug & Play configuration data table when new devices are added or removed, or whenever the BIOS is upgraded.
Large Disk Access Mode	Select *DOS* if your system has DOS. Select *Other* if you have another operating system, such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads, or more than 63 tracks per sector.

Integrated Peripherals Submenu

The Integrated Peripherals Submenu is used to configure the COM ports and the parallel ports, and enable/disable the diskette, enhanced IDE controllers, and onboard BIOS.

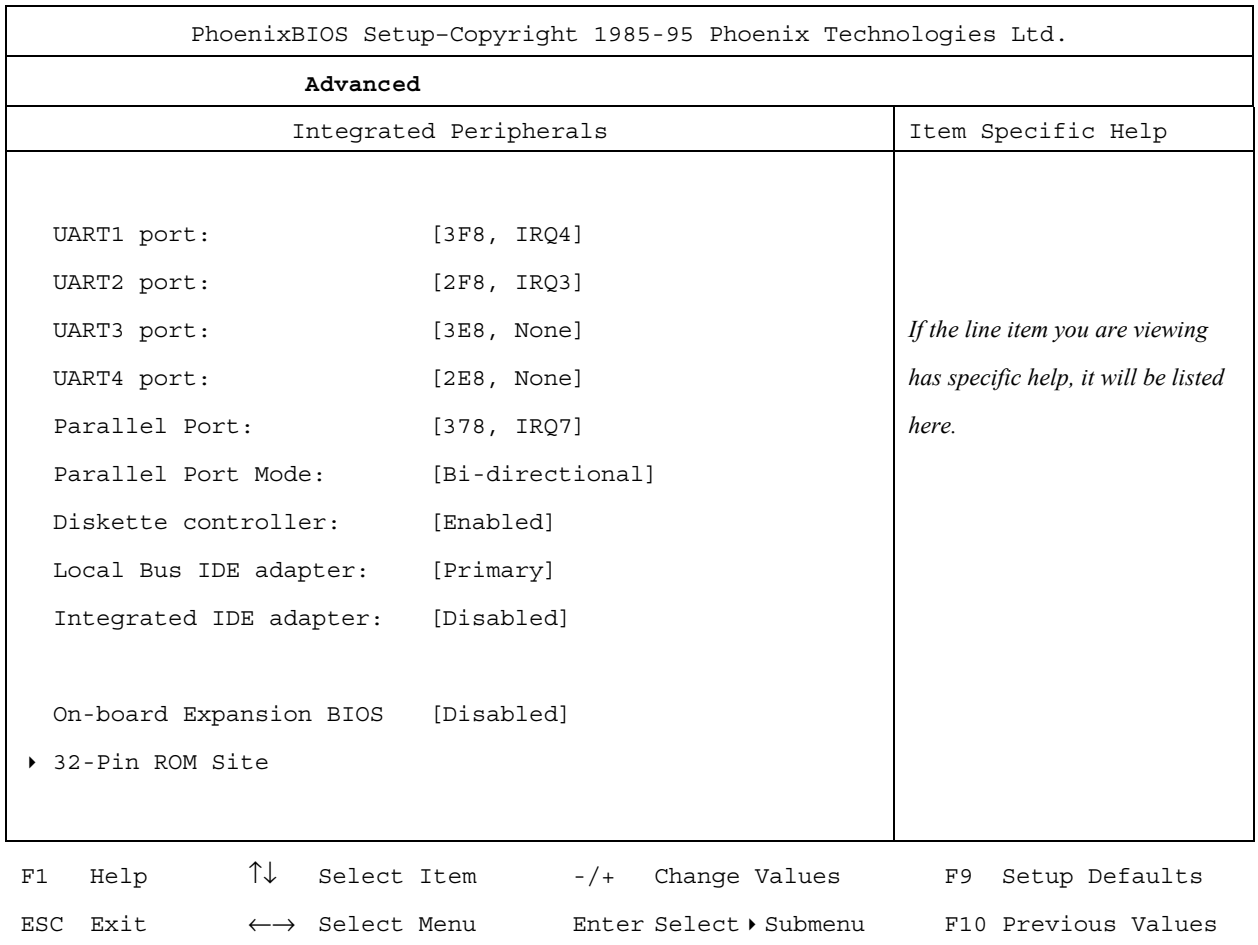


Figure 3-8 Integrated Peripherals Submenu

Table 3-8 Integrated Peripherals Submenu Options

Option	Description
UART1-4 Port	Allows the COM port address and IRQ levels to be modified or disabled.
Parallel Port	Select a unique address and interrupt request for the LPT port, or disable it. *Auto* selects the next available combination.
Parallel Mode	LPT port can be configured for *Bi-directional* or output only (*Standard*).
Diskette Controller	Enables or disables the onboard floppy disk controller.
Local Bus IDE Adapter	Enables or disables the onboard IDE controller.
Integrated IDE Adapter	Enables or disables the secondary IDE controller.
Onboard Expansion BIOS	Enables or disables the onboard expansion BIOS. The default is *Disabled*.

32-Pin ROM Site Submenu

The 32-Pin ROM Site Submenu lets you enable or disable this site, as well as specify the type of device that will occupy it if it is enabled.

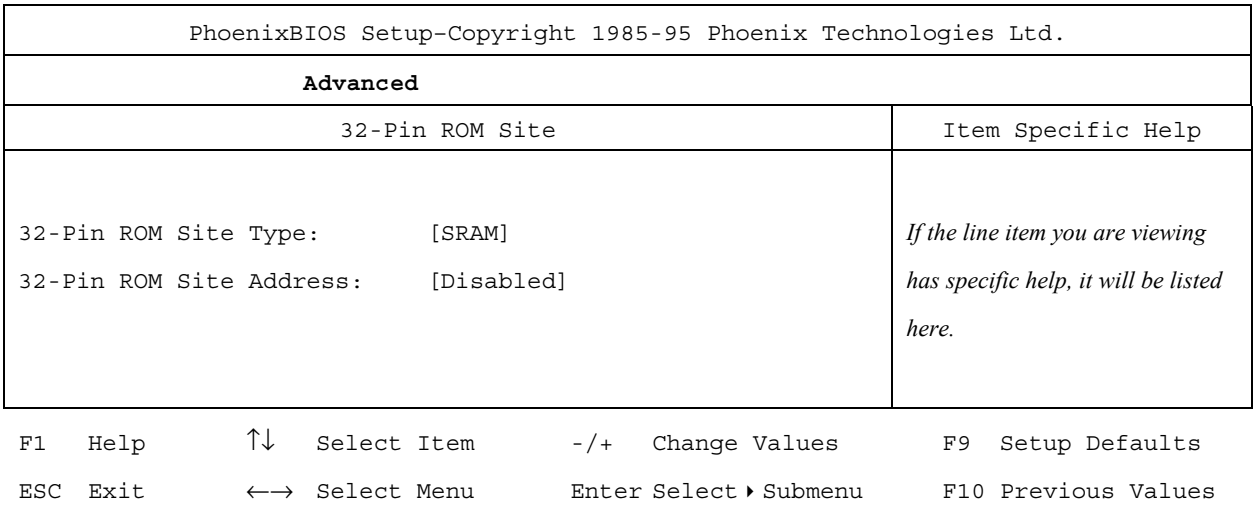


Figure 3-9 32 Pin ROM Site Submenu

Table 3-9 32 Pin ROM Site Submenu Options

Option	Description
32-Pin ROM Site Type	Selects the type of device installed in the 32-Pin ROM site. The choices are *SRAM* or *Disk-On-Chip*. *SRAM* is the default. You can disable this feature by selecting *Disabled* in the 32-Pin ROM Site Address field.
32-Pin ROM Site Address	Disables or selects the address for the device installed in the 32-Pin ROM site. You can disable the SRAM or DiskOnChip by selecting *Disabled*. Other choices are *CC000h-CFFFFh (16 KB)*, *D0000h-D7FFFh (32KB)*, or *D8000h-DFFFFh (32KB)*. *Disabled* is the default.

Advanced Chipset Control Submenu

Use this menu to change the values in the chipset registers and optimize your system's performance.

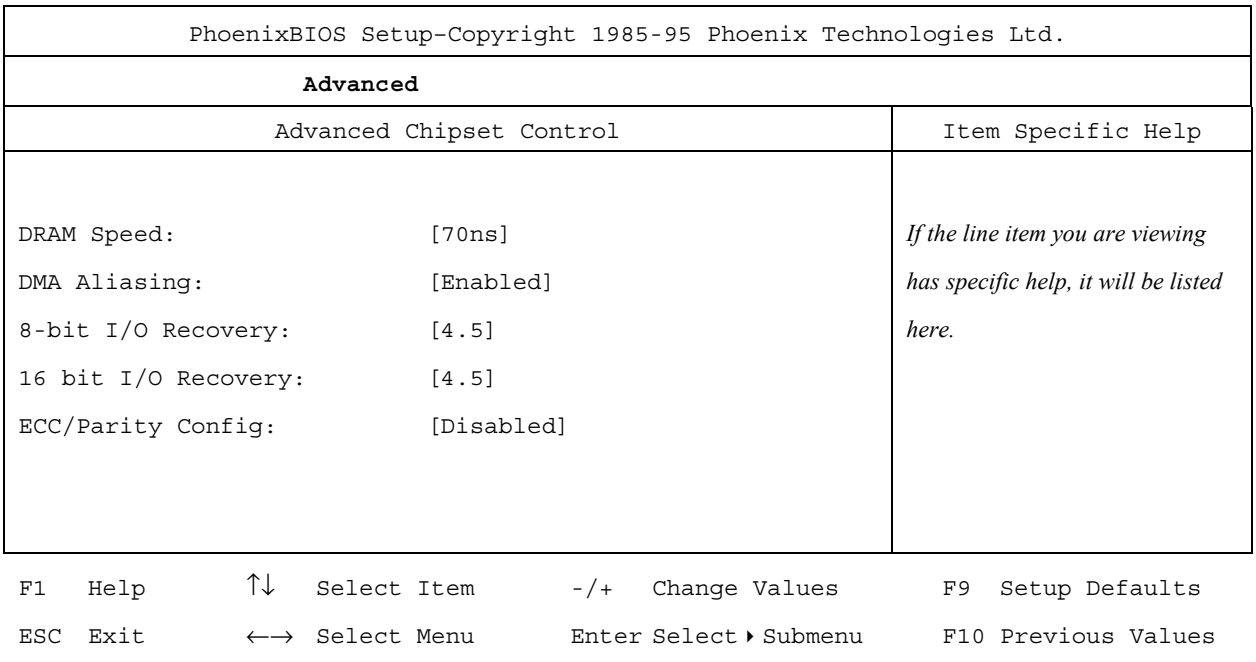


Figure 3-10 Advanced Chipset Control Submenu

Table 3-10 Advanced Chipset Control Submenu Options

Option	Description
DRAM Speed	Speed of the SIMMs installed. This configures the system for maximum performance.
DMA Aliasing	Disable DMA Aliasing if a device exists on the ISA bus that uses I/O ports 90-9Fh.
8-bit I/O Recovery	Number of ISA clock cycles inserted between back-to-back I/O operations
16 bit I/O Recovery	Number of ISA clock cycles inserted between back-to-back I/O operations
ECC/Parity Config	If all memory in the system supports parity (x36), this selection enables simple parity checking or ECC mode.

Note

Leave the options in this menu in their default configurations.

Security Menu

This menu prompts you for the new system password and requires you to verify the password by entering it again. The password can be used to stop access to the setup menus or prevent unauthorized booting of the unit. The supervisor password can also be used to change the user password.

```
        PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.
      Main        Advanced      Security      VMEbus       Exit

                                                          Item Specific Help

Supervisor Password is      Disabled
User Password is            Disabled
Set Supervisor Password     [Press Enter]                 If the line item you are viewing
Set User Password           Press Enter                   has specific help, it will be listed
                                                          here.
Password on boot:           [Disabled]


Diskette access:            [Supervisor]
Fixed disk boot sector:     [Normal]
System backup reminder:     [Disabled]
Virus check reminder:       [Disabled]


F1   Help      ↑↓   Select Item      -/+   Change Values      F9  Setup Defaults
ESC  Exit      ←→   Select Menu      Enter Select ▸ Submenu   F10 Previous Values
```

Figure 3-11 Security Menu

Table 3-11 Security Menu Options

Option	Description
Supervisor Password	Provides full access to Setup menus. You may use up to seven alphanumeric characters. This option is disabled by setting it to *[CR]* or *Nothing*.
Set User Password	Provides restricted access to Setup menus. It requires the prior setting of Supervisor password. You may use up to seven alphanumeric characters.
Password on Boot	If the supervisor password is set and this option is *Disabled*, BIOS assumes the user is booting.
Diskette Access	Restricts access to floppy drives to the supervisor when set to *Supervisor*. Requires setting the Supervisor password.
Fixed Disk Boot Sector	Write protects the disk boot sector to help prevent viruses.
System Backup Reminder/Virus Check Reminder	Displays a message during boot up asking if you have backed up the system or scanned it for viruses (Y/N). The message returns on each boot until you respond *Y*. It displays the message *Daily* (on the first boot of the day), *Weekly* (on the first boot after Sunday), or *Monthly* (on the first boot of the month). The default is *Disabled*.

VMEbus Setup Menu

Using the VMEbus Setup menus, you are able to configure the XVME-653/658 VMEbus master and slave interfaces.

This setup provides the following configurable items:

- System Controller
- Master Interface
- Slave Interface

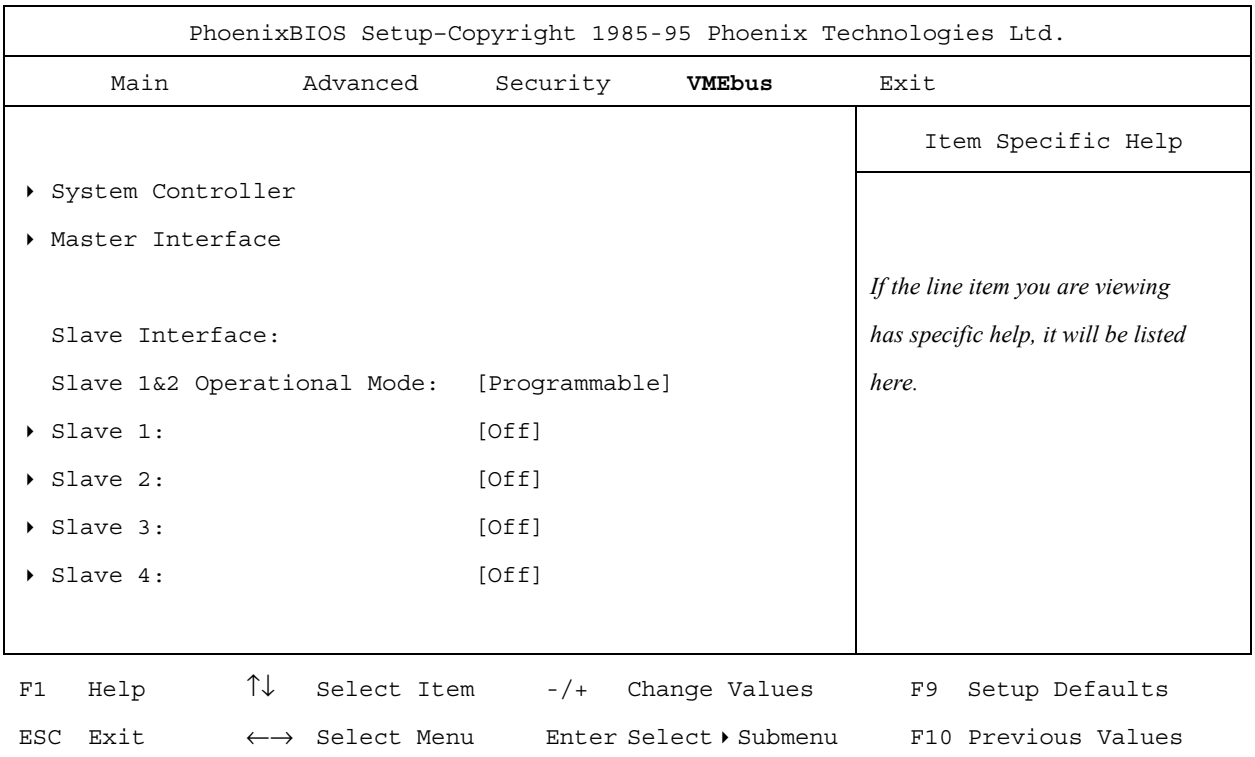


Figure 3-12 VMEbus Setup Menu

Table 3-12 VMEbus Setup Menu Options

Option	Description
Slave 1 & 2 Operational Mode	Selecting *Programmable* allows you to configure and enable VMEbus slaves 1, 2, 3, and 4. When *Compatible* is selected, the BIOS automatically configures and enables VMEbus slaves 1 and 2. *Compatible* sets up the XVME-653/658 slave interface so that it is compatible with older Xycom Automation VME PC processor boards which did not use the Universe chip.

System Controller Submenu

The XVME-653/658 automatically provides slot 1 system resource functions. The system resource functions are explained in the Universe manual. (Contact Tundra at *www.tundra.com* for a .pdf version of the Universe II manual.) This function can be disabled using jumper J1. Refer to **Jumper Settings** in Chapter 2 (p. 2-2) for more information. System resources are VMEbus Arbiter, BERR timeout, SYSCLK, and IACK daisy chain driver. These resources must be provided by the module installed in the system controller slot. The status of the XVME-653/658 system resources is reported in an uneditable field.

Note

The BERR timeout is the VMEbus error timeout value.

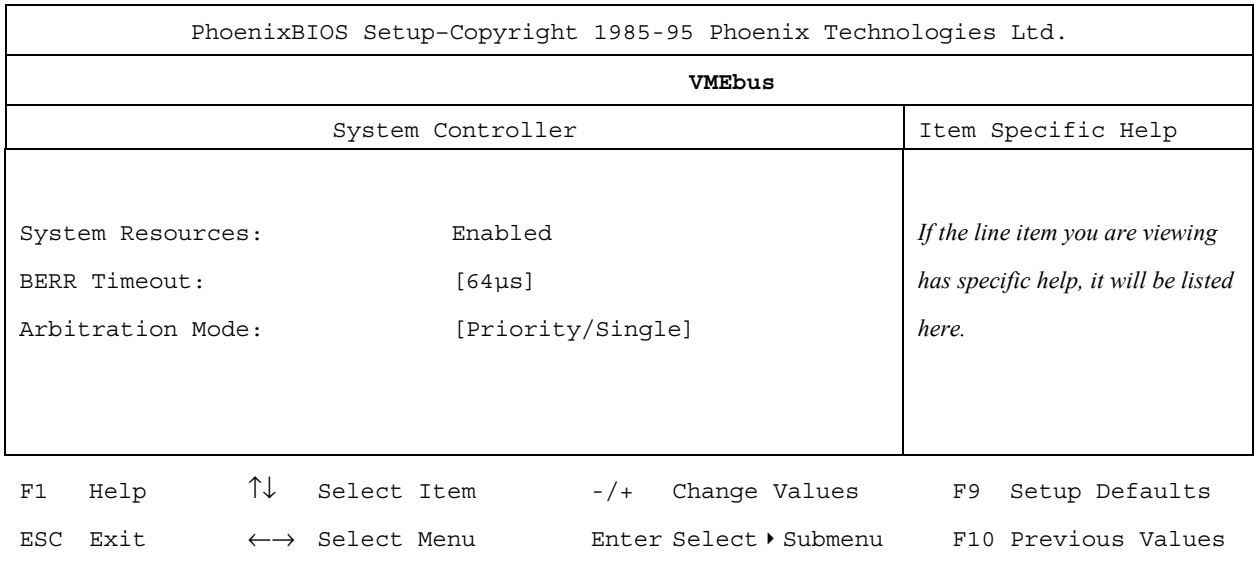


Figure 3-13 System Controller Submenu

Table 3-13 System Controller Submenu Options

Option	Description
System Resources	Enables or disables system resources. You cannot edit this field. It is automatically detected by the board.
BERR Timeout*	Sets the VMEbus error timeout. Choices *are 16µs*, *32µs*, *64µs*, *128µs*, *256µs*, *512µs*, *1024µs*, and *Disabled*. The default is *64µs*.
Arbitration Mode*	Sets the VMEbus arbitration mode. Choices are *Priority/Single* or *Round Robin*. *Priority/Single* is the default.

***Note**

These fields are only referenced if the board is the system controller. If it is not the system controller, the setup field values are ignored, BERR Timeout is set to 0 = *Disabled*, and Arbitration Mode is set to *Round Robin*, with an Arbitration timeout value of 0 (*Disabled*).

Master Interface Submenu

The VMEbus master setup lets you configure the XVME processor board's VMEbus master interface.

> **Note**
>
> When the master interface setting is turned on, master image 0 is reserved for BIOS use. To avoid conflict, master images 1, 2, and 3 are available for use.

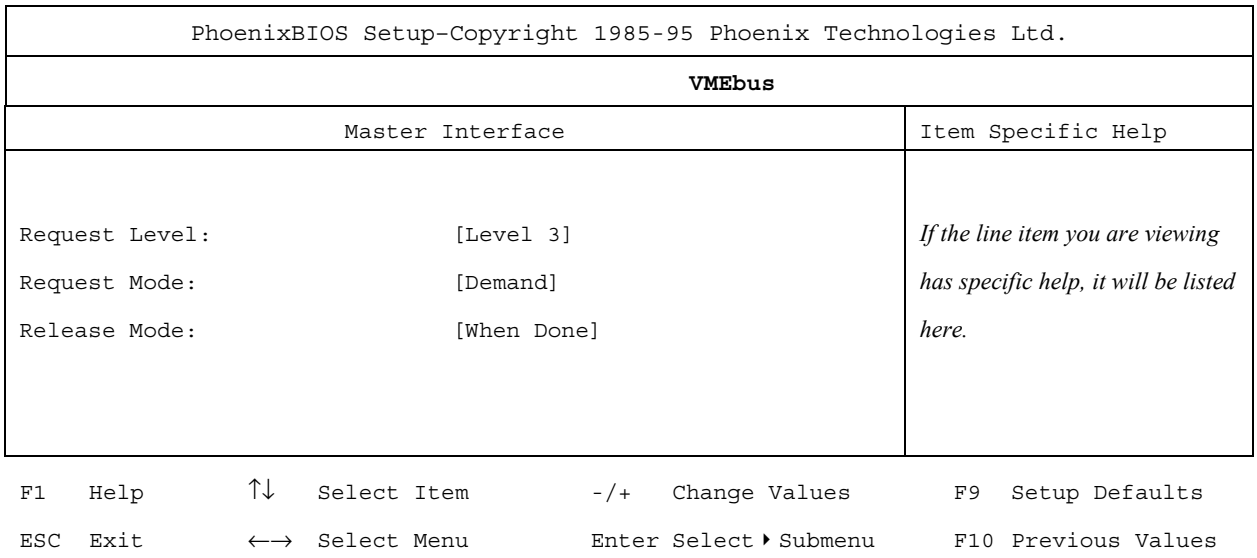


Figure 3-14 Master Interface Submenu

Table 3-14 Master Interface Submenu Options

Option	Description
Request Level	Sets the bus request level when requesting use of the VMEbus to *Level 0*, *Level 1*, *Level 2*, or *Level 3*. The default is *Level 3*.
Request Mode	Sets the bus request mode. Choices are *Demand* or *Fair*. The default is *Demand*.
Release Mode	Sets the bus release mode to use when controlling the VMEbus. The default is *When Done*.

Slave Interface Submenus

The VMEbus slave setup allows configuration of the XVME processor board's VMEbus slave interfaces.

> **Note**
>
> When the Slave 1 & 2 Operational Mode setting is *Compatible*, slave images 0 and 1 are reserved for BIOS use. See p. 3-15 for more details.

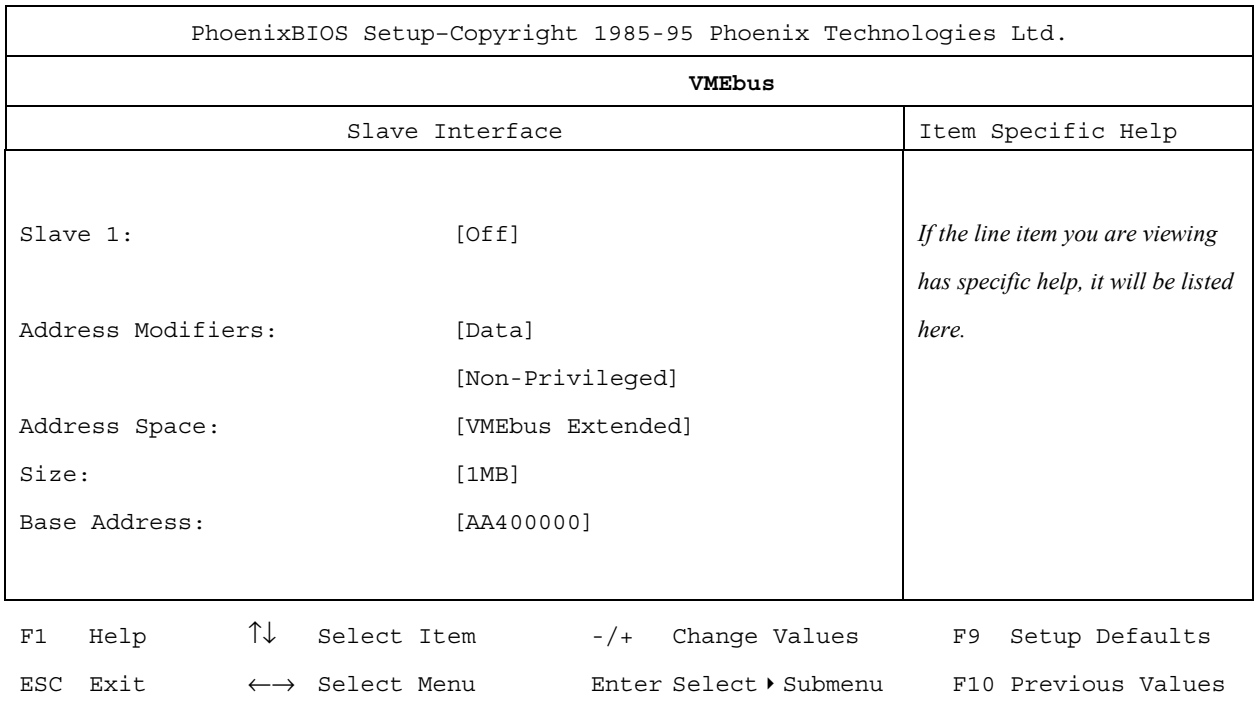


Figure 3-15 Slave Interface Submenu

Table 3-15 Slave Interface Submenu

Option	Description
Slave 1 (or 2, 3, or 4)	Turns the slave interface *On* or *Off*. The default is *Off*. When turned off, other VME masters cannot access memory on the XVME-653/658.
Address Modifiers	Determines which type of VMEbus slave access is permitted to read or write to the XVME-653/658 dual-access DRAM. The first field determines whether the slave interface responds to *Data a*ccess only, *Program* access only, or to *Both* program and data access. The default is *Data*. The second field determines whether the slave interface responds to *Supervisory* access only, *Non-Privileged* access only, or to *Both* supervisory and non-privileged access. The default is *Non-Privileged*.
Address Space	Determines if VME masters access the slave's dual-access memory in the VMEbus *Standard* (A24) or VMEbus *Extended* (A32) address space. The default is VMEbus *Extended*.
Slave Memory Size	Determines the amount of dual-access memory that is available to external VMEbus masters when the Slave Address Space option is set to *Extended*. The slave memory size cannot be more than the total memory size or greater than *16 MB* in *Standard* mode. The default is *1 MB*.
Slave Base Address	Sets the VMEbus address of the XVME-653/658 dual-access RAM. When the Slave Address Space option is set to VMEbus *Standard* (A24), the dual-access memory must be located on a 1 MB boundary and the upper two hex digits of the slave address are ignored. When the Slave Address Space option is set to VMEbus *Extended* (A32), the slave address must be a multiple of the slave memory size. The default is *AA400000*.

Exit Menu

This menu prompts you to exit setup.

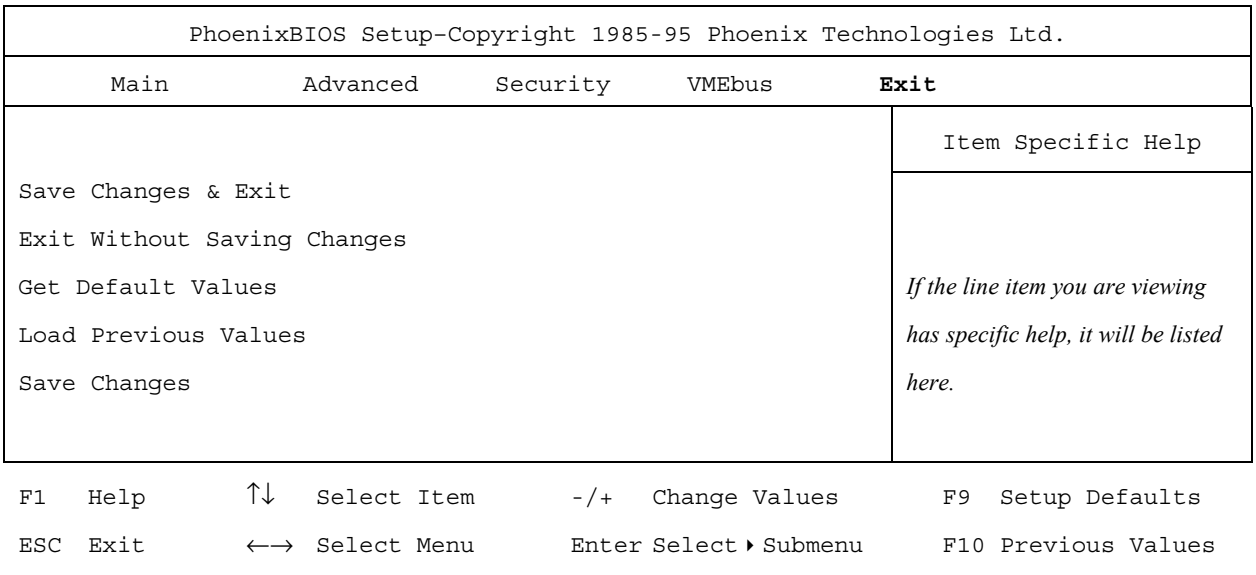


Figure 3-16 Exit Menu

Table 3-16 Exit Menu Options

Option	Description
Save Changes & Exit	After making your selections on the Setup menus, always select either *Save Changes & Exit* or *Save Changes*. Both procedures store the selections displayed in the menus in battery-backed CMOS RAM. After you save your selections, the program displays this message: Notice Changes have been saved. [Continue] If you try to exit without saving, the program asks if you want to save before exiting. The next time you boot your computer, the BIOS configures your system according to the setup selections stored in CMOS. If those values cause the system boot to fail, reboot and press F2 to enter Setup. In Setup, you can get the default values (as described below) or try to change the selections that caused the boot to fail.
Exit Without Saving Changes	This option exits Setup without storing any new selections you have made in CMOS. The previous settings remain in effect.
Get Default Values	To display the default values for all the Setup menus, select this option. The program displays this message: Notice Default values have been loaded. [Continue] If during boot up, the BIOS program detects a problem in the integrity of values stored in CMOS, it displays these messages: System CMOS checksum bad - run SETUP Press <F1> to resume, <F2> to Setup This means the CMOS values have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS. Press F1 to resume the boot (this causes the system to be configured using the default values) or F2 to run Setup with the ROM default values already loaded into the menus. You can make other changes before saving the values to CMOS.
Load Previous Values	If, during a Setup session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you previously saved to CMOS. Selecting *Load Previous Values* updates all the selections and displays this message: Notice Previous values have been loaded. [Continue]
Save Changes	This option saves your selections without exiting Setup. You can return to the other menus if you want to review and change your selections.

BIOS Compatibility

This BIOS is IBM PC compatible with additional CMOS RAM and BIOS data areas used.

Chapter 4 – Programming

Memory Map

Table 4-1 XVME-653/658 Memory Map

Address Range	Size	Usage
FFFC0000-FFFFFFFF	256 KB	System BIOS
Top of DRAM-FFFBFFFF		Allocated to PCI bus by BIOS or operating system*
00100000-0FFFFFFF 00100000-07FFFFFF 00100000-03FFFFFF 00100000-01FFFFFF 00100000-00FFFFFF 00100000-007FFFFF	256 MB 128 MB 64 MB 32 MB 16 MB 8 MB	System DRAM
000F0000-000FFFFF	64 KB	System BIOS
000E0000-000EFFFF	64 KB	System BIOS, Universe chip, or I/O channel memory
00D0000-00DFFFF	64 KB	Universe chip, I/O channel memory, SRAM, or *DiskOnChip*
000CC000-000CFFFF	16 KB	I/O channel memory, SRAM, or *DiskOnChip*
000C0000-000CBFFF	48 KB	VGA BIOS
000A0000-000BFFFF	128 KB	VGA DRAM memory
00000000-0009FFFF	640 KB	System DRAM

***Note**

The PCI devices are located at the very top of memory, just below the system BIOS.

I/O Map

Table 4-2 XVME-653/658 I/O Map

Address Range	Device
000-01F	DMA controller 1, 8237A-5 equivalent
020-021	Interrupt controller 1, 8259 equivalent
022-023	Available
025-02F	Interrupt controller 1, 8259 equivalent*
040-05F	Timer, 8254-2 equivalent
060-06F	Keyboard, 8742 equivalent
070-07F	Real-time clock, bit 7 NMI mask*
080-091	DMA page register*
93-9F	DMA page register*
0A0-0BF	Interrupt controller 2, 8259 equivalent*
0C0-0DF	DMA controller 2, 8237A-5 equivalent*
0F0-0FF	Numeric Data Processor
100	Available
101-1EF	Available
1F0-1F7	IDE controller (AT drive)
1F8-217	Available
218	XA TEMP/ABORT port
219	XA LED/BIOS port
220-232	Available
233	XA Watchdog timer port
234	XA NVRAM and *DiskOnChip* port
280-2F7	Available
2F8-2FF	Serial port 2**
378-37F	Parallel port 1**
3E0-3EF	Available
3F0-3F7	Primary floppy disk controller
3F8-3FF	Serial port 1**

***Note**

Reference the Intel HX PCI chip set data book for detailed information.

****Note**

Serial and parallel port addresses are controlled in the BIOS Setup Menu and they may be changed or disabled. Changing the setting will change the I/O location. Therefore, these addresses may be used for some applications and not for others.

IRQ Map

Table 4-3 AT-bus IRQ Map

Interrupt	Description
IRQ 0	System Timer Tick
IRQ 1	Keyboard
IRQ 2	Reserved (Programmable Interrupt Controller)
IRQ 3	COM 2
IRQ 4	COM 1
IRQ 5	Ethernet LAN Controller
IRQ 6	Floppy Disk Controller
IRQ 7	Parallel Port (LPT1)
IRQ 8	Real-Time Clock
IRQ 9	Pin 4 - PIIX3 USB Interface
IRQ 10	Onboard Reset switch
IRQ 11	Pin 1 - Universe Chip (PCI Bridge)
IRQ 12	PS/2 Mouse
IRQ 13	Reserved (Numeric Data Processor)
IRQ 14	IDE Hard Disk Controller
IRQ 15	Reserved (Secondary IDE Controller)

Note

Serial and parallel port IRQs are available if software does not use the ports or does not use the interrupt.

VME Interface

The VME interface is the Tundra Universe chip, which is a PCI bus-to-VMEbus bridge device. The XVME-653/658 implements a 32-bit PCI bus and a 32/64-bit VMEbus interface. The Universe chip configuration registers are located in a 64 KB block of PCI *memory* space. This memory location is programmable and defined by PCI configuration cycles. The Universe configuration registers should be set up using PCI interrupt calls provided by the BIOS.

For information on accessing the PCI bus, refer to the PCI BIOS Functions section later in this chapter.

Caution

The Universe II manual states that the Universe Control and Status Registers (UCSR) occupy 4 KB of internal memory. While this is true, the Universe controller decodes the entire 64 KB region and shadows the 4 KB 16 times. Contact Tundra at *www.tundra.com* for a .pdf version of the Universe II manual.

Note

PCI memory slave access = VMEbus master access

PCI memory master access = VMEbus slave access

System Resources

The XVME-653/658 automatically provides slot 1 system resource functions. The system resource functions are explained in the Universe manual. (Contact Tundra at www.tundra.com for a .pdf version of the Universe II manual.) This function can be disabled using jumper J1. Refer to **Jumper Settings** in Chapter 2 (p. 2-2) for more information.

VMEbus Master Interface

The XVME-653/658 can act as a VMEbus master by accessing a PCI slave channel or by the DMA channel initiating a transaction. The Universe chip contains eight PCI slave images. Slave images 0 and 4 have a 4 KB resolution; the others (1-3, 5-7) have a 64 KB resolution. Slave images 0 through 3 have been implemented on the XVME-653/658. Slave images 4-7, if required, need to be implemented by the user. The VMEbus master can generate A16, A24, or A32 VMEbus cycles for each PCI slave image.

The address mode and type are programmed on a PCI slave image basis. The PCI memory address location for the VMEbus master cycle is specified by the Base and Bound address. The VME address is calculated by adding the Base address to the Translation Offset address. All PCI slave images are located in the PCI bus memory space.

All VMEbus master cycles are byte-swapped by the Universe chip to maintain address coherency. For more information on the Xycom Automation software selectable byte-swapping hardware on the XVME-658 and the XVME-653/31x modules, refer to p. 4-12.

Caution

PCI slave images mapped to a system DRAM area will access the system DRAM, not the PCI slave image. Also, the Universe configuration register has a higher priority than the PCI slave images. As a result, if the PCI slave image and the Universe configuration registers are mapped into the same memory area, the configuration registers will take precedence.

VMEbus Slave Interface

The XVME-653/658 can act as a VMEbus slave by configuring the VMEbus slave images. There are eight PCI slave images Slave images 0 and 4 have a 4 KB resolution; the others (1-3, 5-7) have a 64 KB resolution. Slave images 0 through 3 have been implemented on the XVME-653/658. Slave images 4-7, if required, need to be implemented by the user. The slave can respond to A16, A24, or A32 VMEbus cycles for each VMEbus slave image.

The address mode and type are programmed on a VMEbus slave image basis. The VMEbus memory address location for the VMEbus slave cycle is specified by the Base and Bound address. The PCI address is calculated by adding the Base address to the Translation offset address.

The XVME-653/658 DRAM memory is based on the PC architecture and is not contiguous. The VMEbus slave images may be set up to allow this DRAM to appear as one contiguous block.

In Compatible Mode, the first VMEbus slave image will have the Base and Bound register set to 640 KB by the BIOS. For example:

VMEbus Slave Image 0 BS= 0000000h BD= A0000h TO = 0000000h

The second VMEbus slave image will have the Base register set to be contiguous with the Bound register from the first VMEbus Slave image by the BIOS. The Bound register is limited by the total XVME-653/658 DRAM. The Translation Offset register is offset by 384 KB, which is equivalent to the A0000h-FFFFFh range on the XVME-653/658 board. For example:

VMEbus Slave Image 1 BS=A0000h BD= 400000h TO = 060000h

Mapping defined by the PC architecture can be overcome if the VMEbus Slave image window is always configured with a 1 MB Translation Offset. From a user and software standpoint, this is desirable because the interrupt vector table, system parameters, and communication buffers (keyboard) are placed in low DRAM. This provides more system protection.

Caution

When setting up slave images, the address and other parameters should be set first. Only after the VMEbus slave image is set up correctly should the VMEbus slave image be enabled. If a slave image is going to be remapped, disable the slave image first, and then reset the address. After the image is configured correctly, re-enable the image.

The VMEbus slave cycle becomes a master cycle on the PCI bus. The PCI bus arbiter is the TSC chip. It arbitrates between the various PCI masters, the Pentium CPU, and the Local bus IDE bus mastering controller. Because the VMEbus cannot be retried, all VMEbus slave cycles must be allowed to be processed. This becomes a problem when a PCI cycle to a PCI slave image is in progress while a VMEbus slave cycle to the onboard DRAM is in progress. The PCI cycle will not give up the PCI bus and the VMEbus slave cycle will not give up the VMEbus, causing the XVME-653/658 to become deadlocked. If the XVME-653/658 is to be used as a master and a slave at the same time, the VMEbus master cycles must obtain the VMEbus prior to initiating VMEbus cycles.

All VMEbus slave interface cycles are byte-swapped to maintain address coherency. For more information on the Xycom Automation software selectable byte-swapping hardware on the XVME-658 and the XVME-653/31x modules, refer to p. 4-12.

VMEbus Interrupt Handling

The XVME-653/658 can service VME IRQ[7:1]. A register in the Universe chip enables the interrupt levels that will be serviced by the XVME-653/658. When a VMEbus IRQ is asserted, the Universe requests the VMEbus and generates an IACK cycle. Once the IACK cycle is complete, a PCI bus interrupt is generated to allow the proper Interrupt

Service Routine (ISR) to be executed. The Universe connects to all four PCI bus interrupts. These interrupts may be shared by other PCI bus devices. The BIOS maps the PCI bus interrupts to the AT-bus interrupt controllers on IRQ11.

Because the PCI devices share interrupt lines, all ISR routines must be prepared to chain the interrupt vector to allow the other devices to be serviced.

Note

All PCI devices on the XVME-653/658 are routed through IRQ11.

Caution

IRQ10 is defined for the Abort toggle switch.

VMEbus Interrupt Generation

The XVME-653/658 can generate VMEbus interrupts on all seven levels. There is a unique STATUS/ID associated with each level. Upper bits are programmed in the STATUS/ID register. The lowest bit is cleared if the source of the interrupt is a software interrupt, and set for all other interrupt sources. Consult the Universe User's Manual for a more in-depth explanation.

VMEbus Reset Options

When the front panel **Reset** switch is toggled, the XVME-653/658 can perform the following reset options:

1. Reset the VME backplane only.
2. Reset the XVME-653/658 CPU only.
3. Reset both.
4. Reset neither.

See **Switch Settings** on p. 2-4 for information on how to configure the **Reset** options.

PCI BIOS Functions

Special PCI BIOS functions provide a software interface to the Universe chip, providing the PCI-to-VMEbus interface. These PCI BIOS functions are invoked using function and subfunction codes. A user sets up the host processor registers for the function and subfunction desired and calls the PCI BIOS software. The PCI BIOS function code is B1h. Status is returned using the Carry flag ([CF]) and registers specific to the subfunction invoked.

Access to the PCI BIOS special functions for 16-bit callers is provided through interrupt 1Ah. Thirty-two bit (i.e., protect mode) access is provided by calling through a 32-bit protect mode entry point.

Calling Conventions

The PCI BIOS functions preserve all registers and flags except those used for return parameters. The Carry Flag [CF] will be altered as shown to indicate completion status. The calling routine will be returned to with the interrupt flag unmodified and interrupts will not be enabled during function execution. These routines, which are re-entrant, require 1024 bytes of stack space and the stack segment must be the same size (i.e., 16- or 32-bit) as the code segment. The PCI BIOS provides a 16-bit real and protect mode interface and a 32-bit protect mode interface.

16-Bit Interface

The 16-bit interface is provided through the Int 1Ah software interrupt. The PCI BIOS Int 1Ah interface operates in either real mode, virtual-86 mode, or 16:16 protect mode. The Int 1Ah entry point supports 16-bit code only.

32-Bit Interface

The protected mode interface supports 32-bit protect mode callers. The protected mode PCI BIOS interface is accessed by calling through a protected mode entry point in the PCI BIOS. The entry point and information needed for building the segment descriptors are provided by the BIOS32 Service Directory. Thirty-two bit callers invoke the PCI BIOS routines using CALL FAR.

The BIOS32 Service Directory is implemented in the BIOS in a contiguous 16-byte data structure, beginning on a 16-byte boundary somewhere in the physical address range 0E0000h-0FFFFFh. The address range should be scanned for the following valid, checksummed data structure containing the following fields:

Table 4-4 BIOS32 Service Table

Offset	Size	Description
0	4 bytes	Signature string in ASCII. The string is *_32_*. This puts an underscore at offset 0, a *3* at offset 1, a *2* at offset 2, and another underscore at offset 3.
4	4 bytes	Entry point for the BIOS32 Service Directory. This is a 32-bit physical address.
8	1 byte	Revision level.
9	1 byte	Length of the data structure in 16-byte increments. (This data structure is 16 bytes long, so this field contains 01h.)
0Ah	1 byte	Checksum. This field is the checksum of the complete data structure. The sum of all bytes must add up to 0.
0Bh	5 bytes	Reserved. Must be zero.

The BIOS32 Service Directory is accessed by doing a FAR CALL to the entry point obtained from the Service data structure. There are several requirements about the calling environment that must be met. The CS code segment selector and the DS data segment selector must be set up to encompass the physical page holding the entry point as well as the immediately following physical page. They must also have the same base. The SS stack segment selector must be 32-bit and provide at least 1 KB of stack space. The calling environment must also allow access to I/O space.

The BIOS32 Service Directory provides a single function call to locate the PCI BIOS service. All parameters to the function are passed in registers. Parameter descriptions are provided below. Three values are returned by the call. The first is the base physical address of the PCI BIOS service, the second is the length of the service, and the third is the entry point to the service encoded as an offset from the base. The first and second values can be used to build the code segment selector and data segment selector for accessing the service.

ENTRY:

[EAX] Service Identifier = “$PCI” (049435024h)

[EBX] Set to Zero

EXIT:

[AL] Return Code:

00h = SUCCESSFUL

80h = SERVICE_IDENTIFIER_NOT_FOUND

81h = INVALID VALUE IN [BL]

[EBX] Physical address of the base of the PCI BIOS service

[ECX] Length of the PCI BIOS service

[EDX] Entry point into the PCI BIOS Service. This is an offset from the base provided in [EBX].

PCI BIOS Function Calls

The available function calls are used to identify the location of resources and to access configuration space of the VMEbus interface. Special functions allow the reading and writing of individual bytes, words, and dwords in the configuration space.

PCI BIOS routines (for both 16- and 32-bit callers) must be invoked with appropriate privilege so that interrupts can be enabled/disabled and the routines can access I/O space.

Locating the Universe Chip

This function returns the location (bus number) of the Universe chip providing the PCI interface to the VMEbus.

ENTRY:

[AH] BIOS_FUNCTION_ID = B1h

[AL] BIOS_SUBFUNCTION_ID = 02h

[CX] Device ID = 0

[DX] Vendor ID = 10E3h

[SI] Index = 0

EXIT:

[BH] Bus Number (0-255)

[BL] Device Number in upper 5 bits

Function Number is bottom 3 bits

[AH] Return Code:

00h = SUCCESSFUL

86h = DEVICE_NOT_FOUND

83h = BAD_VENDOR_ID

[CF] Completion Status, set = error, reset = success

Read Configuration Byte

This function reads individual bytes from the configuration space of the VMEbus interface.

ENTRY:

[AH] BIOS_FUNCTION_ID = B1h

[AL] BIOS_SUBFUNCTION_ID = 08h

[BH] Bus Number (0-255)

[BL] Device Number in upper 5 bits
Function Number is bottom 3 bits

[DI] Register Number (0...255)

EXIT:

[CL] Byte Read

[AH] Return Code:
00h = SUCCESSFUL
87h = BAD_REGISTER_NUMBER

[CF] Completion Status, set = error, reset = success

Read Configuration Word

This function reads individual words from the configuration space of the VMEbus interface. The Register Number parameter must be a multiple of two (i.e., bit 0 must be set to 0).

ENTRY:

[AH] BIOS_FUNCTION_ID = B1h

[AL] BIOS_SUBFUNCTION_ID = 09h

[BH] Bus Number (0-255)

[BL] Device Number in upper 5 bits
Function Number is bottom 3 bits

[DI] Register Number (0, 2, 4, ...254)

EXIT:

[CL] Word Read

[AH] Return Code:
00h = SUCCESSFUL
87h = BAD_REGISTER_NUMBER

[CF] Completion Status, set = error, reset = success

Read Configuration Dword

This function reads individual dwords from the configuration space of the VMEbus interface. The Register Number parameter must be a multiple of four (i.e., bits 0 and 1 must be set to 0).

ENTRY:

[AH] BIOS_FUNCTION_ID = B1h

[AL] BIOS_SUBFUNCTION_ID = 0Ah

[BH] Bus Number (0-255)

[BL] Device Number in upper 5 bits
Function Number is bottom 3 bits

[DI] Register Number (0, 4, 8, ...252)

EXIT:

[ECX] Dword Read

[AH] Return Code:
00h = SUCCESSFUL
87h = BAD_REGISTER_NUMBER

[CF] Completion Status, set = error, reset = success

Write Configuration Byte

This function writes individual bytes from the configuration space of the VMEbus interface.

ENTRY:

[AH] BIOS_FUNCTION_ID = B1h

[AL] BIOS_SUBFUNCTION_ID = 0Bh

[BH] Bus Number (0-255)

[BL] Device Number in upper 5 bits
Function Number is bottom 3 bits

[DI] Register Number (0...255)

[CL] Byte Value to Write

EXIT:

[AH] Return Code:
00h = SUCCESSFUL
87h = BAD_REGISTER_NUMBER

[CF] Completion Status, set = error, reset = success

Write Configuration Word

This function writes individual words from the configuration space of the VMEbus interface. The Register Number parameter must be a multiple of two (i.e., bit 0 must be set to 0).

ENTRY:

[AH] BIOS_FUNCTION_ID = B1h

[AL] BIOS_SUBFUNCTION_ID = 0Ch

[BH] Bus Number (0-255)

[BL] Device Number in upper 5 bits
Function Number is bottom 3 bits

[DI] Register Number (0, 2, 4, ...254)

[CX] Word Value to Write

EXIT:

[AH] Return Code:
00h = SUCCESSFUL
87h = BAD_REGISTER_NUMBER

[CF] Completion Status, set = error, reset = success

Write Configuration Dword

This function writes individual dwords from the configuration space of the VMEbus interface. The Register Number parameter must be a multiple of four (i.e., bits 0 and 1 must be set to 0).

ENTRY:

[AH] BIOS_FUNCTION_ID = B1h

[AL] BIOS_SUBFUNCTION_ID = 0Dh

[BH] Bus Number (0-255)

[BL] Device Number in upper 5 bits
Function Number is bottom 3 bits

[DI] Register Number (0, 4, 8, ...252)

[ECX] Dword Value to Write

EXIT:

[AH] Return Code:
00h = SUCCESSFUL
87h = BAD_REGISTER_NUMBER

[CF] Completion Status, set = error, reset = success

Software-Selectable Byte-Swapping Hardware

Software-selectable byte-swapping hardware is integrated into all XVME-658 and XVME-653/31x boards (see Table 1-1) to allow for the difference between the Intel and Motorola byte-ordering schemes, allowing easy communication over the VMEbus. The byte-swapping package incorporates several buffers either to pass data straight through or to swap the data bytes as they are passed through.

Byte-Ordering Schemes

The Motorola family of processors stores data with the least significant byte located at the highest address and the most significant byte at the lowest address. This is referred to as a big-endian bus and is the VMEbus standard. The Intel family of processors—which includes the AMD-K6 processors as well as the Intel Pentium processors—stores data in the opposite way, with the least significant byte located at the lowest address and the most significant byte located at the highest address. This is referred to as a little-endian (PCI) bus. This fundamental difference is illustrated in Figure 4-1, which shows a 32-bit quantity stored by both architectures, starting at address *M*.

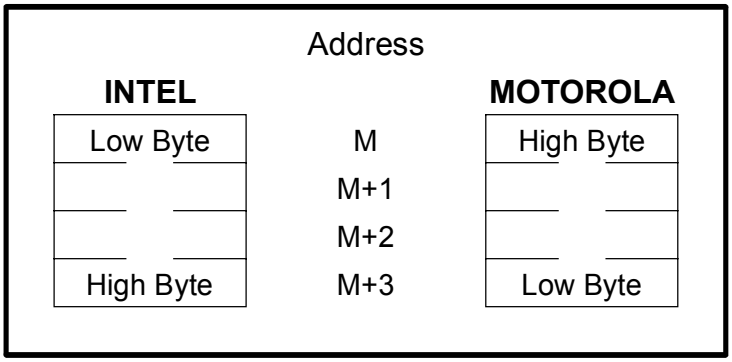


Figure 4-1 Byte Ordering Schemes

Note

The two architectures differ only in the way in which they store data into memory, not in the way in which they place data on the shared data bus.

The XVME-653/658 contains a Universe chip that performs address-invariant translation between the PCI bus (Intel architecture) and the VMEbus (Motorola architecture), and byte-swapping hardware to reverse the Universe chip byte-lane swapping. (Contact Tundra at *www.tundra.com* for a .pdf version of the Universe II manual.) Figure 4-2 shows address-invariant translation between a PCI bus and a VMEbus.

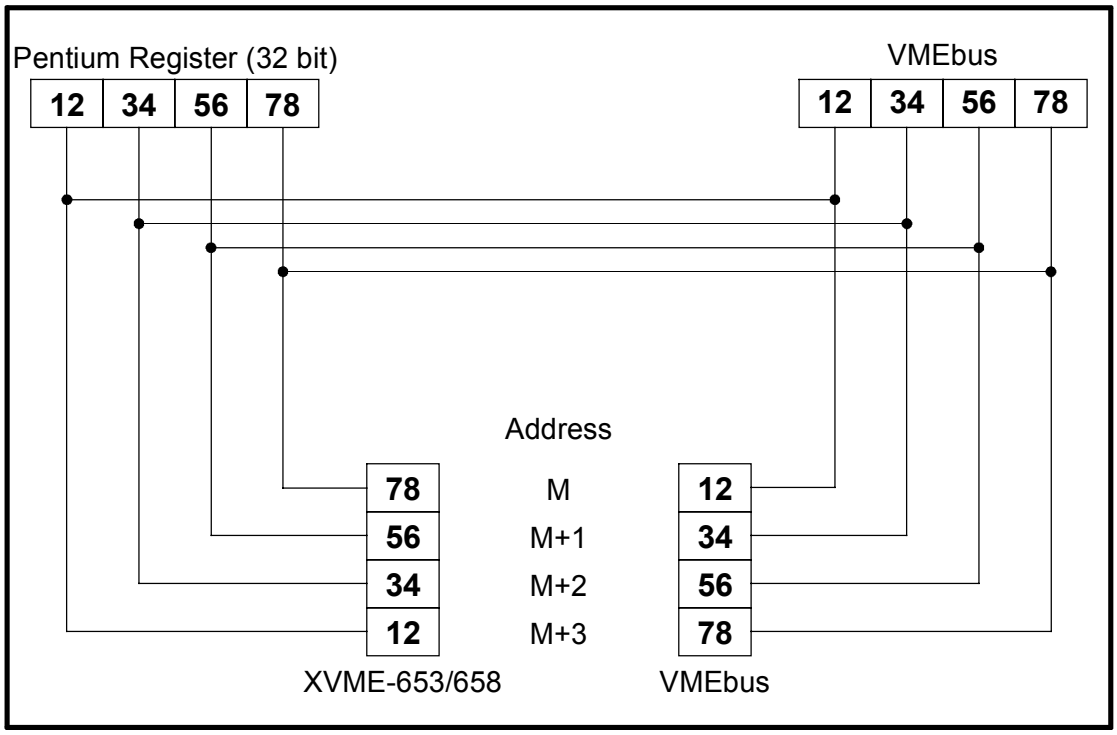


Figure 4-2 Address-Invariant Translation

Notice that the internal data storage scheme for the PCI (Intel) bus is different from that of the VME (Motorola) bus. For example, the byte *78* (the least significant byte) is stored at location *M* on the PCI machine while the byte *78* is stored at the location *M+3* on the VMEbus machine. Therefore, the data bus connections between the architectures must be mapped correctly.

Numeric Consistency

Numeric consistency, or data consistency, refers to communications between the XVME-653/658 and the VMEbus in which the byte-ordering scheme described above is maintained during the transfer of a 16-bit or 32-bit quantity. Numeric consistency is achieved by setting the XVME-653/658 buffers to pass data straight through, which allows the Universe chip to perform address-invariant byte-lane swapping. Numeric consistency is desirable for transferring integer data, floating-point data, pointers, etc. Consider the long word value 12345678h stored at address *M* by both the XVME-653/658 and the VMEbus, as shown in Figure 4-3.

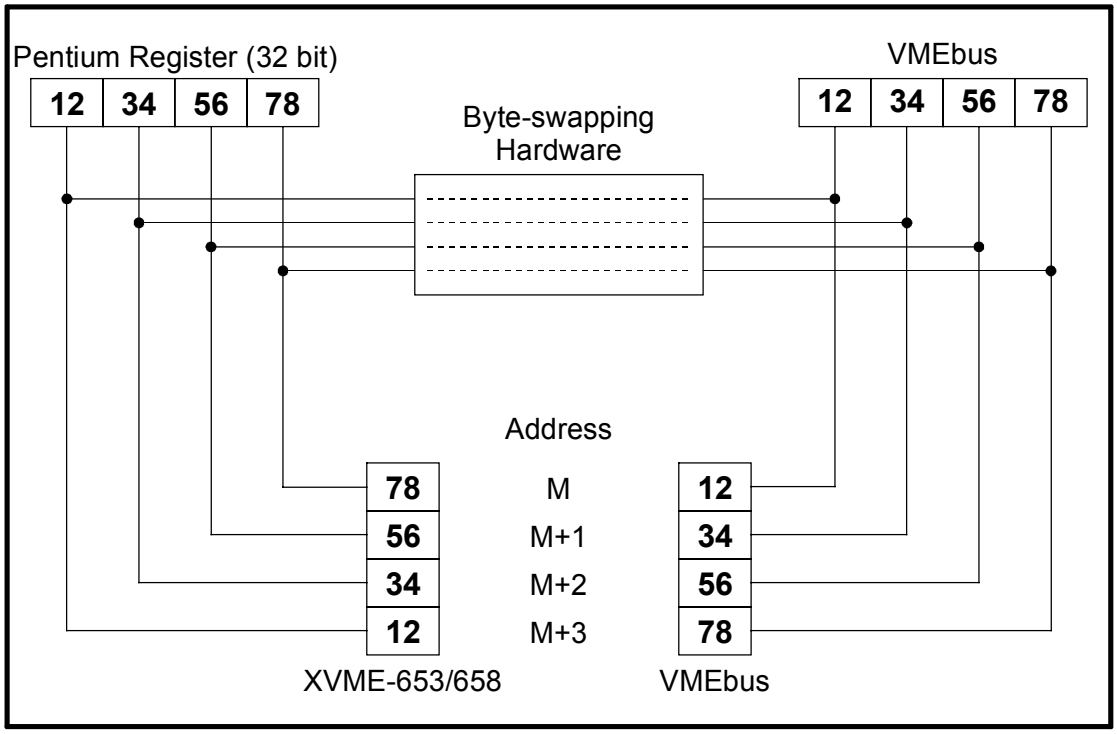


Figure 4-3 Maintaining Numeric Consistency

Due to the Universe chip, the data must be passed straight through the byte-swapping hardware. To do this, maintaining numeric consistency, enable the straight-through buffers by setting bits 6 and 7 of the NVRAM and DiskOnChip Port (Register 234h) to 1 (see p. 2-6).

Note

With the straight-through buffers enabled, the XVME-653/658 does not support unaligned transfers. Sixteen-bit or 32-bit transfers must have an even address.

Address Consistency

Address consistency, or address coherency, refers to communications between the XVME-653/658 and the VMEbus in which both architectures' addresses are the same for each byte. In other words, the XVME-653/658 and the VMEbus memory images appear the same. Address consistency is desirable for byte-oriented data such as strings or video image data. Consider the example of transferring the string *Text* to the VMEbus memory using a 32-bit transfer in Figure 4-4.

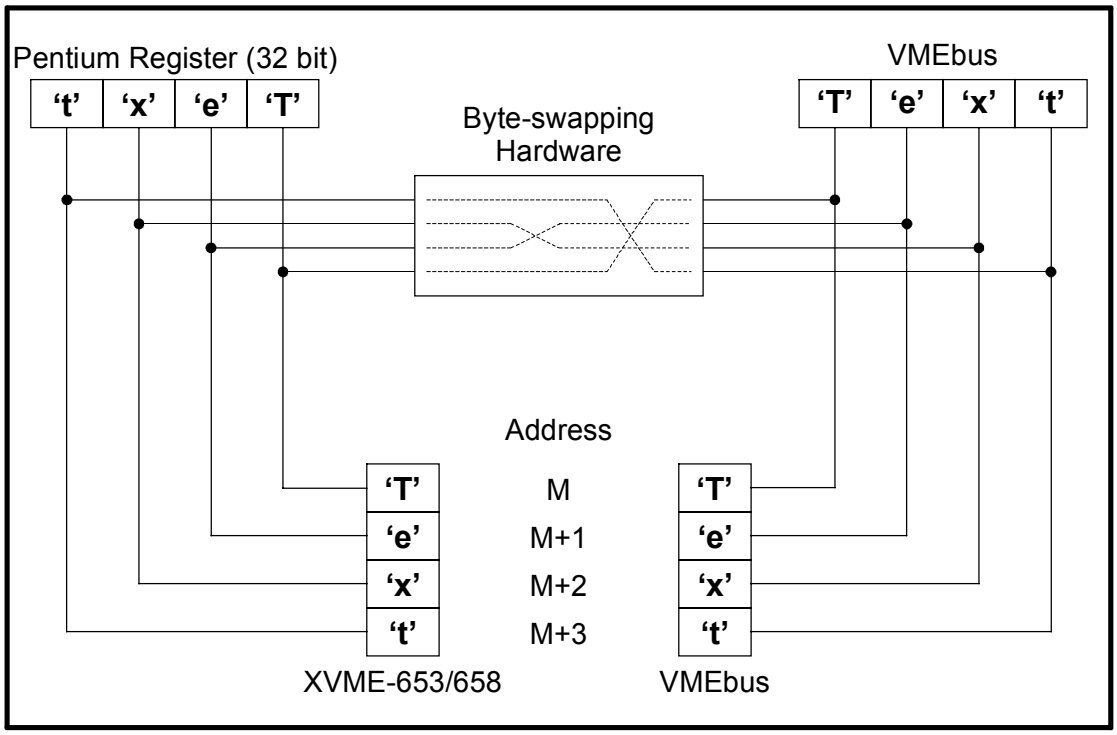


Figure 4-4 Maintaining Address Consistency

Notice that the data byte at each address is identical. To achieve this, the data bytes need to be swapped as they are passed from the PCI bus to the VMEbus. To maintain address consistency, enable the byte-swapping buffers by setting setting bits 6 and 7 of the NVRAM and DiskOnChip Port (Register 234h) to 0 (see p. 2-6).

Chapter 5 – XVME-973/1 Drive Adapter Module

The XVME-973/1 Drive Adapter Module is used to connect an external hard and floppy drive to your XVME-653/658 module. It has a single edge connector, labeled P2, that connects to the P2 backplane connector on the rear of the VME chassis. Figure 5-1 illustrates how to connect the XVME-973/1 P2 connector to the VME chassis backplane P2 connector.

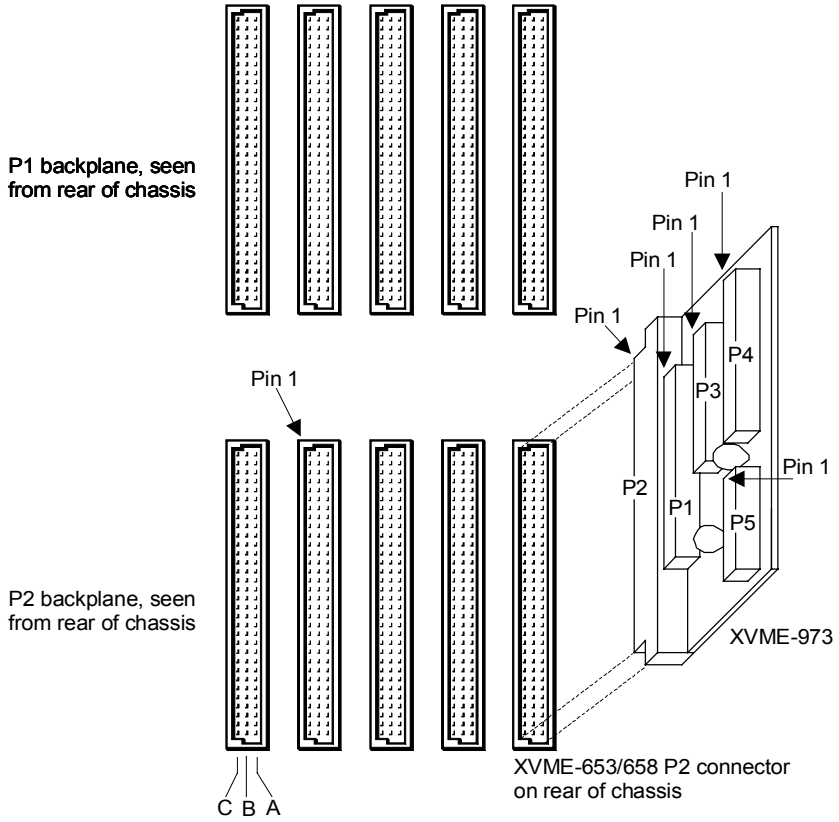


Figure 5-1 XVME-973/1 Installation

The XVME-973/1 module has four connectors on it for the connection of up to two IDE hard drives and one 3.5" floppy drive. Pinouts for all of the connectors are given in this chapter.

The P3 connector connects a single 3.5" floppy drive and the P5 connector connects a single of 3.5" floppy drive of the type found in many laptop computers. Since both of these connectors are routed to the same signal lines on the P2 connector, only one may be used at a time.

Similarly, the P1 connector connects up to two standard 3.5" hard drives and the P4 connector connects up to two 2.5" hard drives. Both of these connectors also use the same P2 connector signal lines, so only one may be used at a time.

The XVME-973/1 is shipped with cables for the P1 and the P3 connectors. The pinouts in this chapter may be used as references to make cables for the P2 and P4 connectors.

Connectors

This section describes the pinouts for each of the five connectors on the XVME-973/1.

P1 Connector

The P1 connector connects up to two 3.5" hard drives. Power for the drives is *not* supplied by the XVME-973/1.

Table 5-1 XVME-973/1 P1 Connector Pinout

Pin	Signal	Pin	Signal
1	HDRESET*	21	HDRQ
2	GND	22	GND
3	HD7	23	DIOW*
4	HD8	24	GND
5	HD6	25	DIOR*
6	HD9	26	GND
7	HD5	27	IORDY
8	HD10	28	ALE
9	HD4	29	HDACK*
10	HD11	30	GND
11	HD3	31	IRQ14
12	HD12	32	IOCS16*
13	HD2	33	DA1
14	HD13	34	NC
15	HD1	35	DA0
16	HD14	36	DA2
17	HD0	37	CS1P*
18	HD15	38	CS3P*
19	GND	39	IDEATP*
20	KEY (NC)	40	GND

Caution

The IDE controller supports enhanced PIO modes, which reduce the cycle times for 16-bit data transfers to the hard drive. Check with your drive manual to see if the drive you are using supports these modes. The higher the PIO mode, the shorter the cycle time. As the IDE cable length increases, this reduced cycle time can lead to erratic operation. As a result, it is in your best interest to keep the IDE cable as short as possible.

The PIO modes are selected in the BIOS setup (see p. 3-4). The Autoconfig will attempt to classify the connected drive if the drive supports the auto ID command. If you experience problems, change the **Transfer Mode:** to *Standard*.

Caution

The total cable length must not exceed 18 inches. Also, if two drives are connected, they must be no more than six inches apart.

P2 Connector

The XVME-973/1 P2 connector connects directly to the XVME-653/658 P2 connector through the VME chassis backplane.

Table 5-2 XVME-973/1 P2 Connector Pinout

Pin	A	B	C
1	RES	+5V	HDRSTDRV*
2	RES	GND	HD0
3	RES	RES	HD1
4	RES	RES	HD2
5	RES	RES	HD3
6	RES	RES	HD4
7	RES	RES	HD5
8	RES	RES	HD6
9	RES	RES	HD7
10	RES	RES	HD8
11	RES	RES	HD9
12	RES	GND	HD10
13	RES	+5V	HD11
14	RES	RES	HD12
15	RES	RES	HD13
16	RES	RES	HD14
17	RES	RES	HD15
18	RES	RES	GND
19	GND	RES	DIOW*
20	FRWC*	RES	DIOR*
21	IDX*	RES	IORDY
22	MO1*	GND	ALE
23	HDRQ	RES	IRQ14
24	FDS1*	RES	IOCS16*
25	HDACK*	RES	DA0
26	FDIRC*	RES	DA1
27	FSTEP*	RES	DA2
28	FWD*	RES	CS1P*
29	FWE*	RES	CS3P*
30	FTK0*	RES	IDEATP*
31	FWP*	GND	FHS*
32	FRDD*	+5V	DCHG*

P3 Connector

P3 connects a single 3.5" floppy drive. Only one drive is supported. Power for this drive is *not* supplied by the XVME-973/1.

Table 5-3 XVME-973/1 P3 Connector Pinout

Pin	Signal	Pin	Signal
1	GND	18	FDIRC*
2	FRWC*	19	GND
3	GND	20	FSTEP*
4	NC	21	GND
5	KEY (NC)	22	FWD*
6	NC	23	GND
7	GND	24	FWE*
8	IDX*	25	GND
9	GND	26	FTK0*
10	MO1*	27	GND
11	GND	28	FWP*
12	NC	29	GND
13	GND	30	FRDD*
14	FDS1*	31	GND
15	GND	32	FHS*
16	NC	33	GND
17	GND	34	DCHG*

P4 Connector

P4 connects up to two 2.5" hard drives. Power for the drives is supplied by the connector.

Table 5-4 XVME-973/1 P4 Connector Pinout

Pin	Signal	Pin	Signal
1	HDRSTDRV*	23	DIOW*
2	GND	24	GND
3	HD7	25	DIOR*
4	HD8	26	GND
5	HD6	27	IORDY
6	HD9	28	ALE
7	HD5	29	HDACK*
8	HD10	30	GND
9	HD4	31	IRQ14
10	HD11	32	IOCS16*
11	HD3	33	DA1
12	HD12	34	NC
13	HD2	35	DA0
14	HD13	36	DA2
15	HD1	37	CS1P*
16	HD14	38	CS3P*
17	HD0	39	IDEATP*
18	HD15	40	GND
19	GND	41	+5V
20	NC	42	+5V
21	HDRQ	43	GND
22	GND	44	NC

Caution

The IDE controller supports enhanced PIO modes, which reduce the cycle times for 16-bit data transfers to the hard drive. Check with your drive manual to see if the drive you are using supports these modes. The higher the PIO mode, the shorter the cycle time. As the IDE cable length increases, this reduced cycle time can lead to erratic operation. As a result, it is in your best interest to keep the IDE cable as short as possible.

The PIO modes are selected in the BIOS setup (see p. 3-4). The Autoconfig will attempt to classify the connected drive if the drive supports the auto ID command. If you experience problems, change the **Transfer Mode:** to *Standard*.

Caution

The total cable length must not exceed 18 inches. If two drives are connected, they must be no more than six inches apart.

P5 Connector

P5 connects a single 3.5" floppy drive. Power for this drive is supplied by the connector.

Table 5-5 XVME-973/1 P5 Connector Pinout

Pin	Signal	Pin	Signal
1	+5V	14	FSTEP*
2	IDX*	15	GND
3	+5V	16	FWD*
4	FDS1*	17	GND
5	+5V	18	FWE*
6	DCHG*	19	GND
7	NC	20	FTKO*
8	NC	21	GND
9	NC	22	FWP*
10	MO1*	23	GND
11	NC	24	FRDD*
12	FDIRC*	25	GND
13	NC	26	FHS*

Appendix A – DRAM Installation

The XVME-653/658 has two 72-pin single inline memory module (SIMM) sites in which memory is inserted. Due to the CPU speed, DRAM access time should be 70 ns or less, and must be 60 ns to run with the zero wait states.

The XVME-653/658 supports 32, 64, 128, and 256 MB of DRAM. You can use 4Mx32, 8Mx32, 16Mx32 DRAM SIMM, and 32Mx32 DRAM SIMM sizes. Table A-1 lists the combinations needed for the memory configurations. (The *U* number is silkscreened on the front of the board.)

Table A-1 DRAM SIMM Combinations

Memory	SIMM Site U34	SIMM Site U35
32 MB	4M x 32	4M x 32
64 MB	8M x 32	8M x 32
128 MB	16M x 32	16M x 32
256 MB	32M x 32	32M x 32

Figure A-1 illustrates DRAM installation.

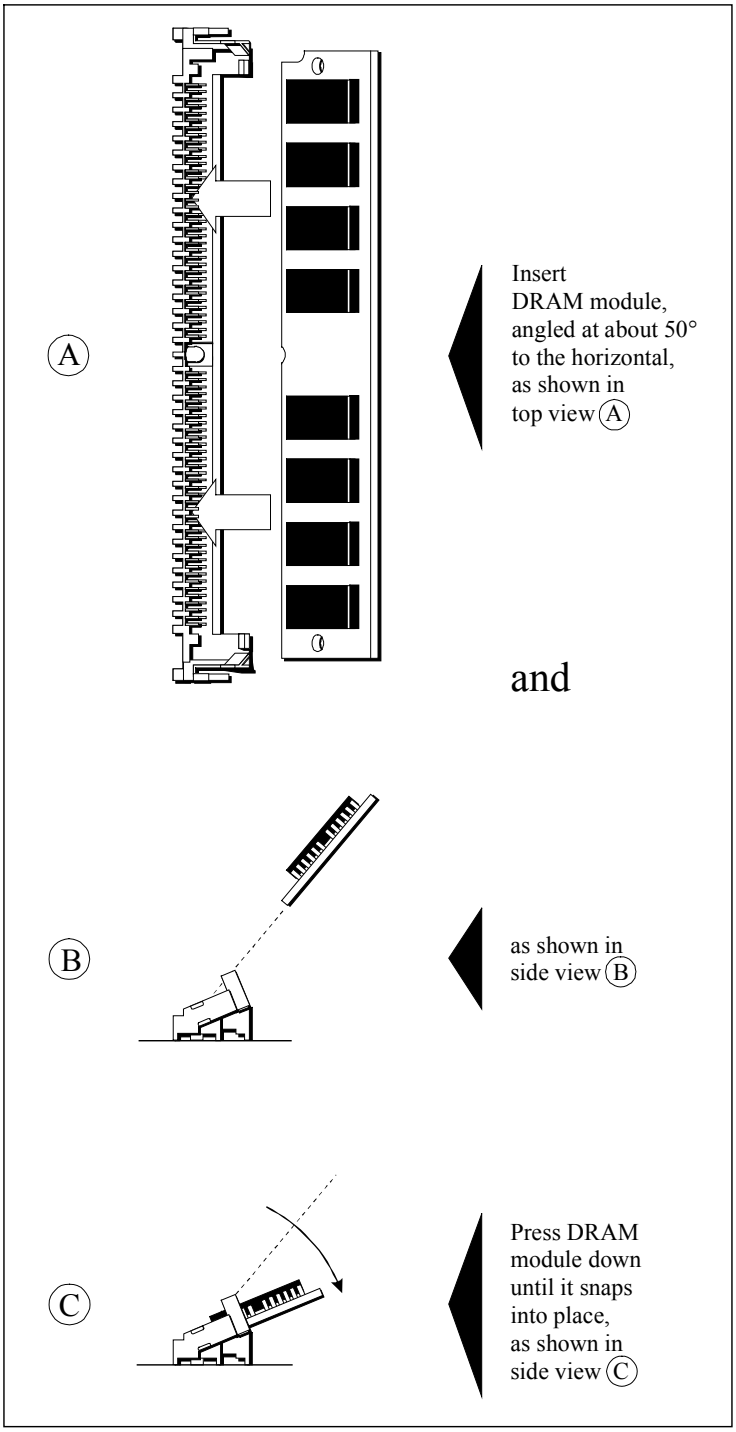


Figure A-1 DRAM Installation

To remove a strip, pull outward on the plastic tab while lifting the end. Loosen one side, then the other.

Tables A-2 through A-5 list recommended DRAM manufacturers along with part numbers. All recommended DRAM is EDO mode DRAM. Fast page mode DRAM is indicated in the tables.

Table A-2 4M x 32 Part Numbers

Manufacturer	Part Number
Samsung	KMM5324004BSW-6
Viking Components	VE432-416-60TS (fast page mode)
Xycom Automation	104302

Table A-3 8M x 32 Part Numbers

Manufacturer	Part Number
Samsung	KMM5328004BSW-6
Viking Components	VE832-416-60TS (fast page mode)
Xycom Automation	106054

Table A-4 16M x 32 Part Numbers

Manufacturer	Part Number
Advantage Memory Corp.	E1632-16X4-66T (fast page mode)
Xycom Automation	123514

Table A-5 32M x 32 Part Numbers

Manufacturer	Part Number
Advantage Memory Corp.	E3232-16X4-66TA (fast page mode)
Xycom Automation	138802

Appendix B – Drawings

This appendix contains the board assembly drawings (top view) for the XVME-653/658. Figure B-1 is the assembly drawing for the XVME-658 and the XVME-653/31x modules, both of which have the byte-swapping hardware. Figure B-2 is the assembly drawing for the XVME-653/30x module, which doesn't have the byte-swapping hardware.

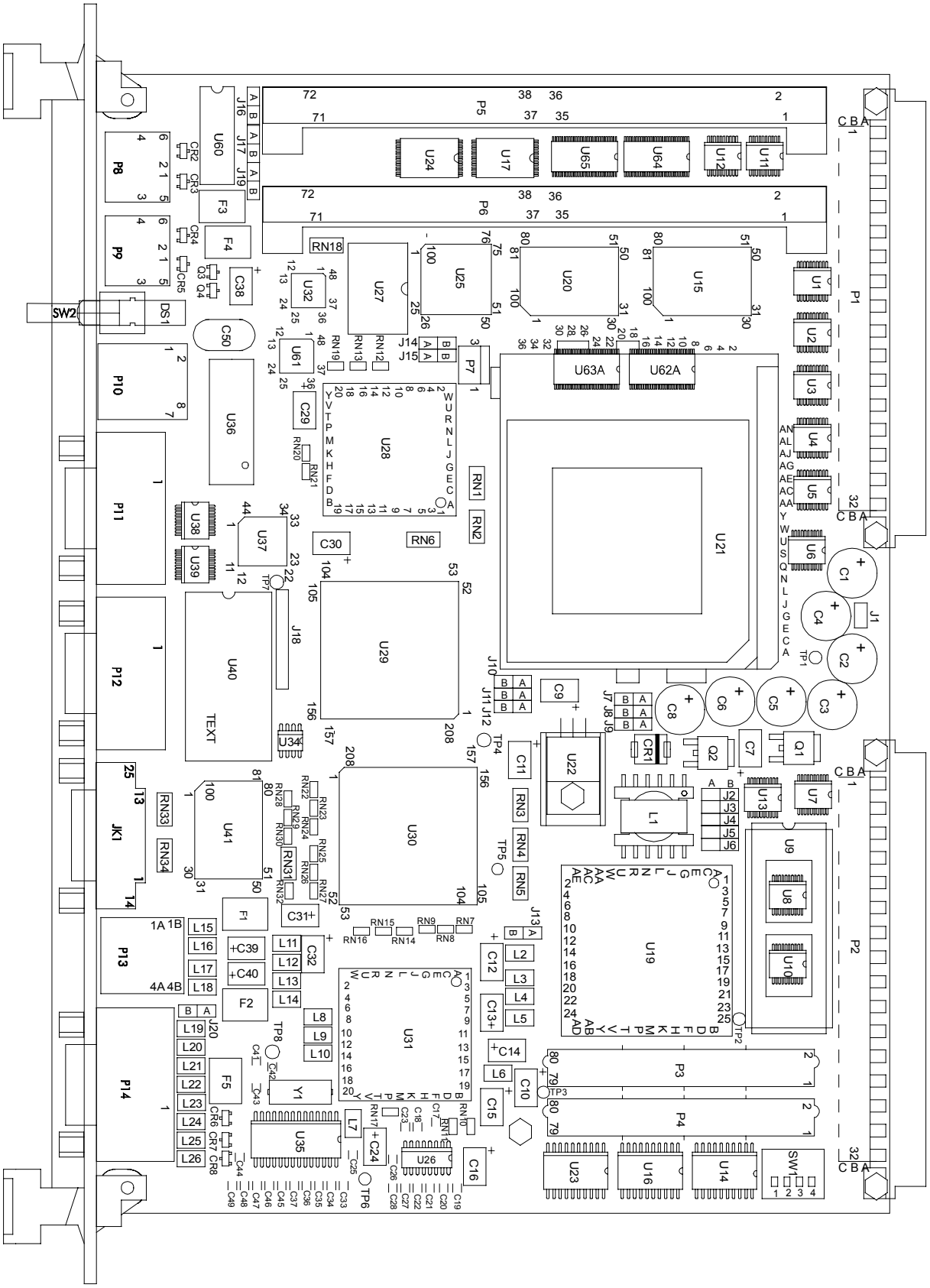


Figure B-1 Assembly Drawing for XVME-658 and XVME-653/31x

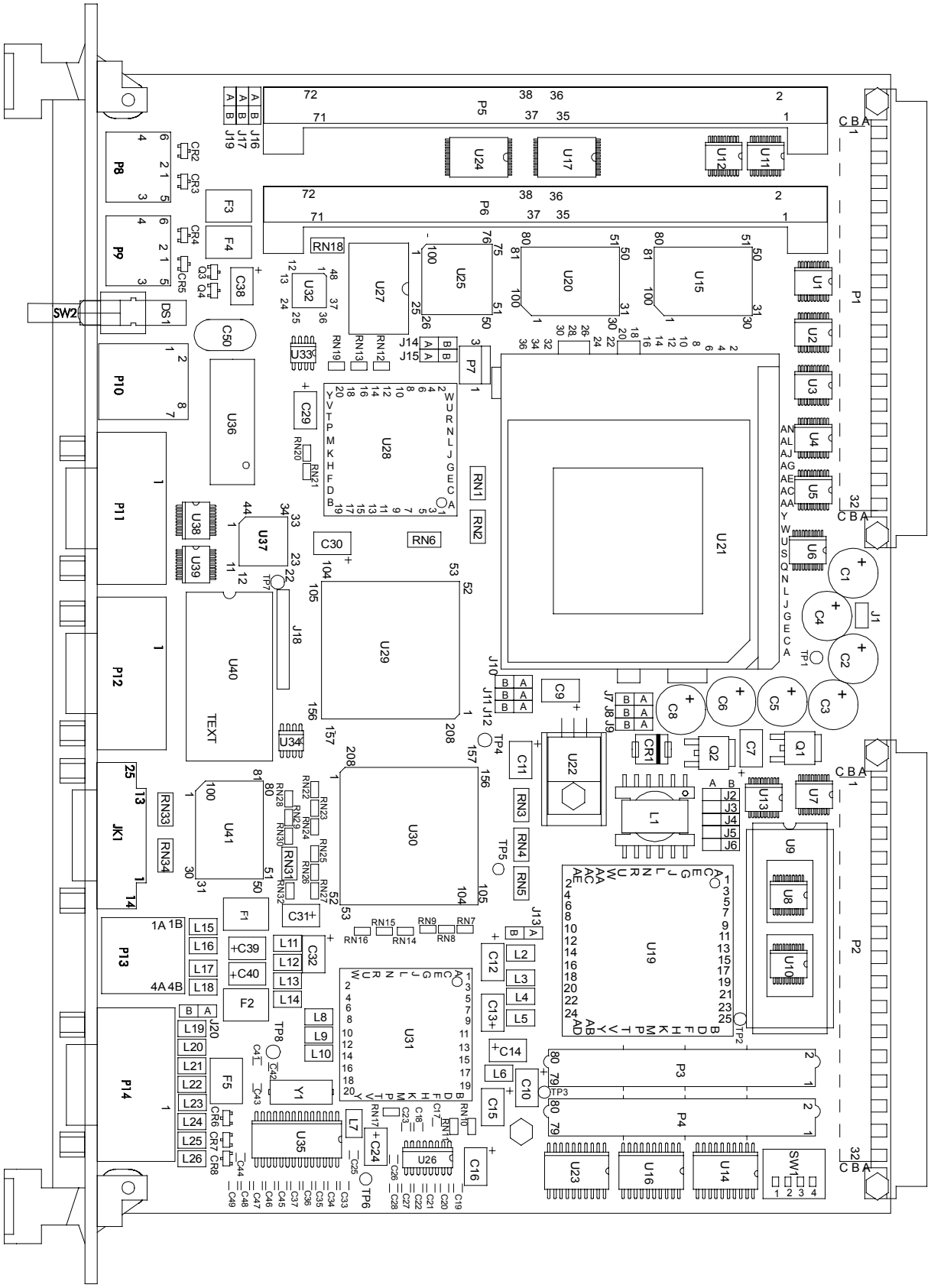
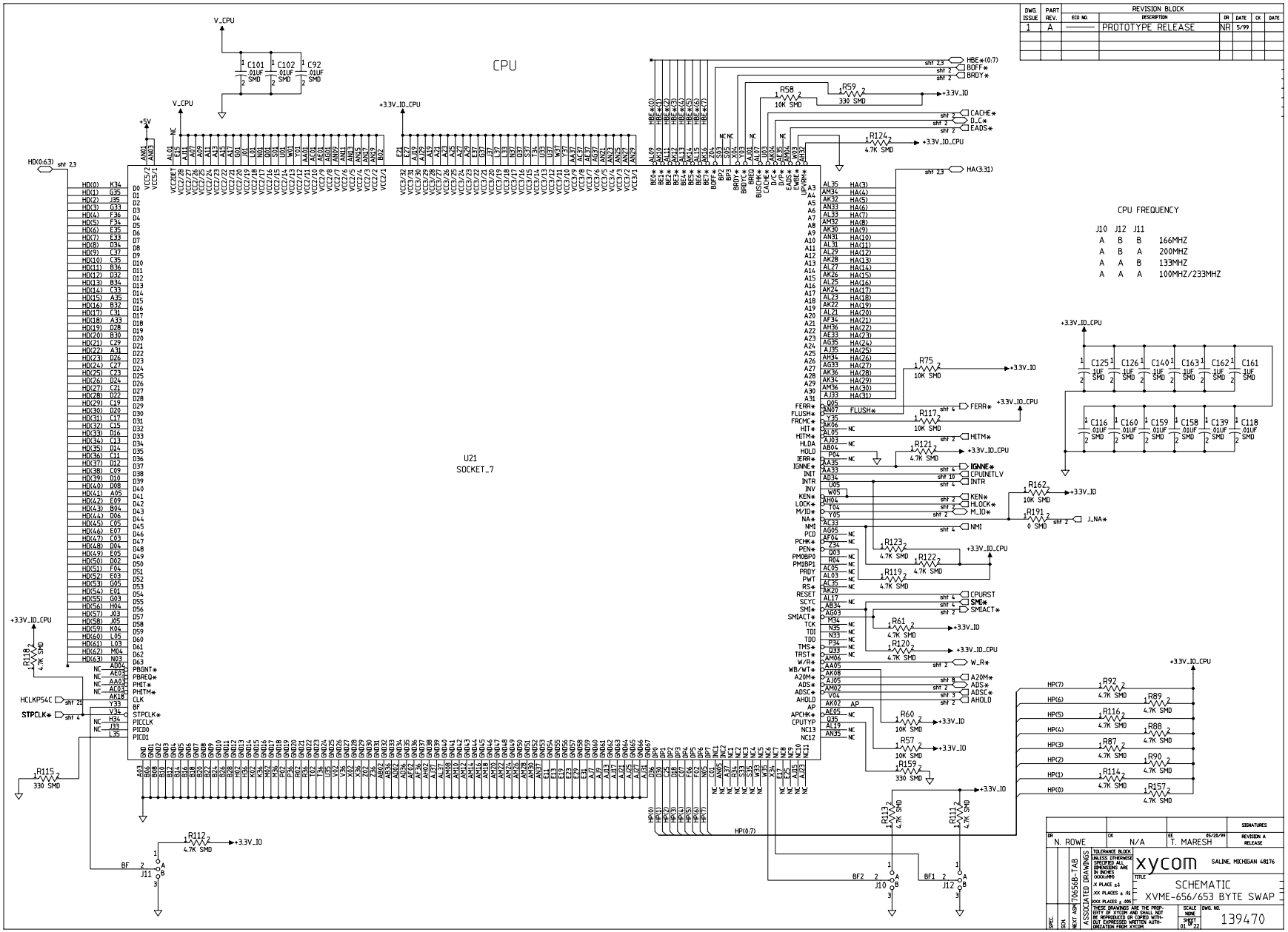
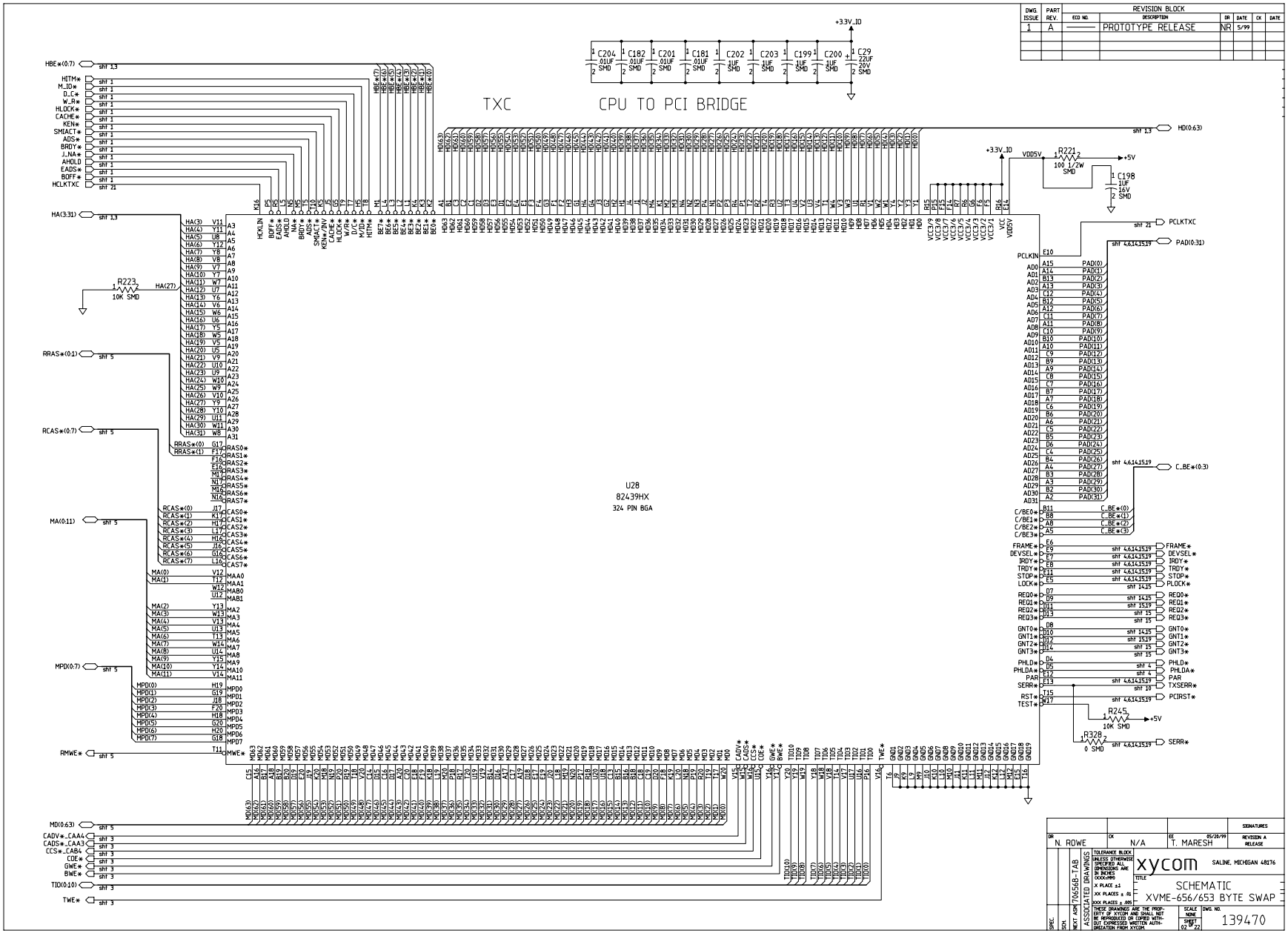


Figure B-2 Assembly Drawing for XVME-653/30x

Appendix C – Schematic

This appendix contains the schematic for the XVME-653/658. It consists of 22 pages and is for the XVME-658 and the XVME-653/31x, both of which have the byte-swapping hardware. To use the schematic with an XVME-653/30x module (which has no byte-swapping hardware), ignore the last page of the schematic (schematic page 22). Schematic page 22 and the signal lines to and from schematic page 22 (connecting to schematic pages 8, 10, 14, 16, 17, and 21) are used only with modules that include the byte-swapping hardware.


CPU
U21
SOCKET_7
V_CPU
+3.3V_IO_CPU
+3.3V_IO
+5V
HD(0:63)
HA(3:31)
HBE#(0:7)
HP(0:7)
HCLKPS4C
STPCLK#
BF
BF2
BF1
J11
J10
J12
CPU FREQUENCY
J10 J12 J11
A B B 166MHZ
A B A 200MHZ
A A B 133MHZ
A A A 100MHZ/233MHZ
REVISION BLOCK
PROTOTYPE RELEASE
xycom
SALINE, MICHIGAN 48176
SCHEMATIC
XVME-656/653 BYTE SWAP
139470


TXC
CPU TO PCI BRIDGE
U28
82439HX
324 PIN BGA
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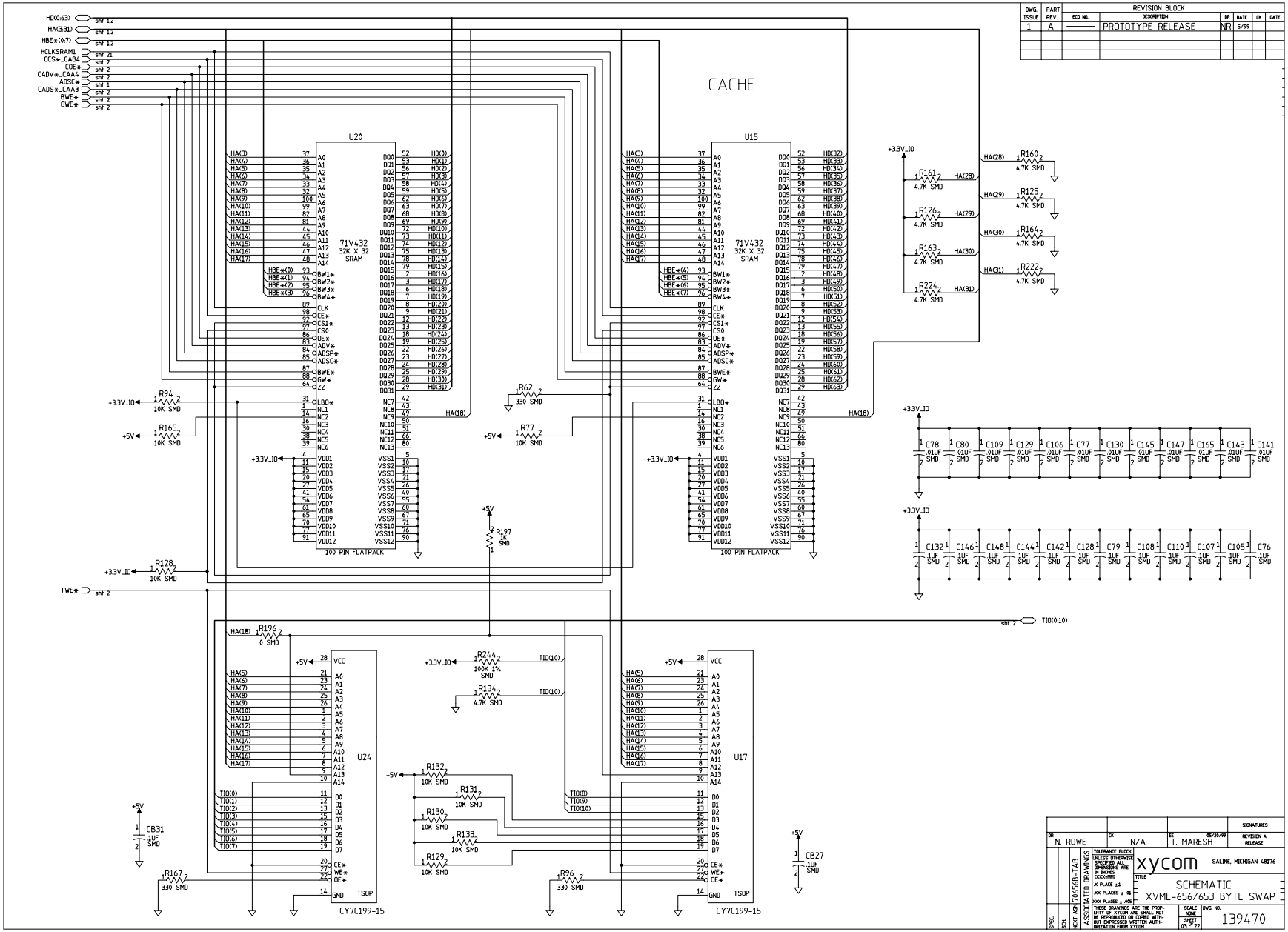
PROTOTYPE RELEASE
xycom
SALINE, MICHIGAN 48176
SCHEMATIC
XVME-656/653 BYTE SWAP
139470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U20
U15
71V432
32K X 32
SRAM
100 PIN FLATPACK
U24
U17
CY7C199-15
TSOP
REVISION BLOCK
DWG. ISSUE
PART REV.
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
1
A
PROTOTYPE RELEASE
NR
5/99
N. ROWE
N/A
T. MARESH
05/26/99
SALINE, MICHIGAN 48176
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SCHEMATIC
XVME-656/653 BYTE SWAP
139470
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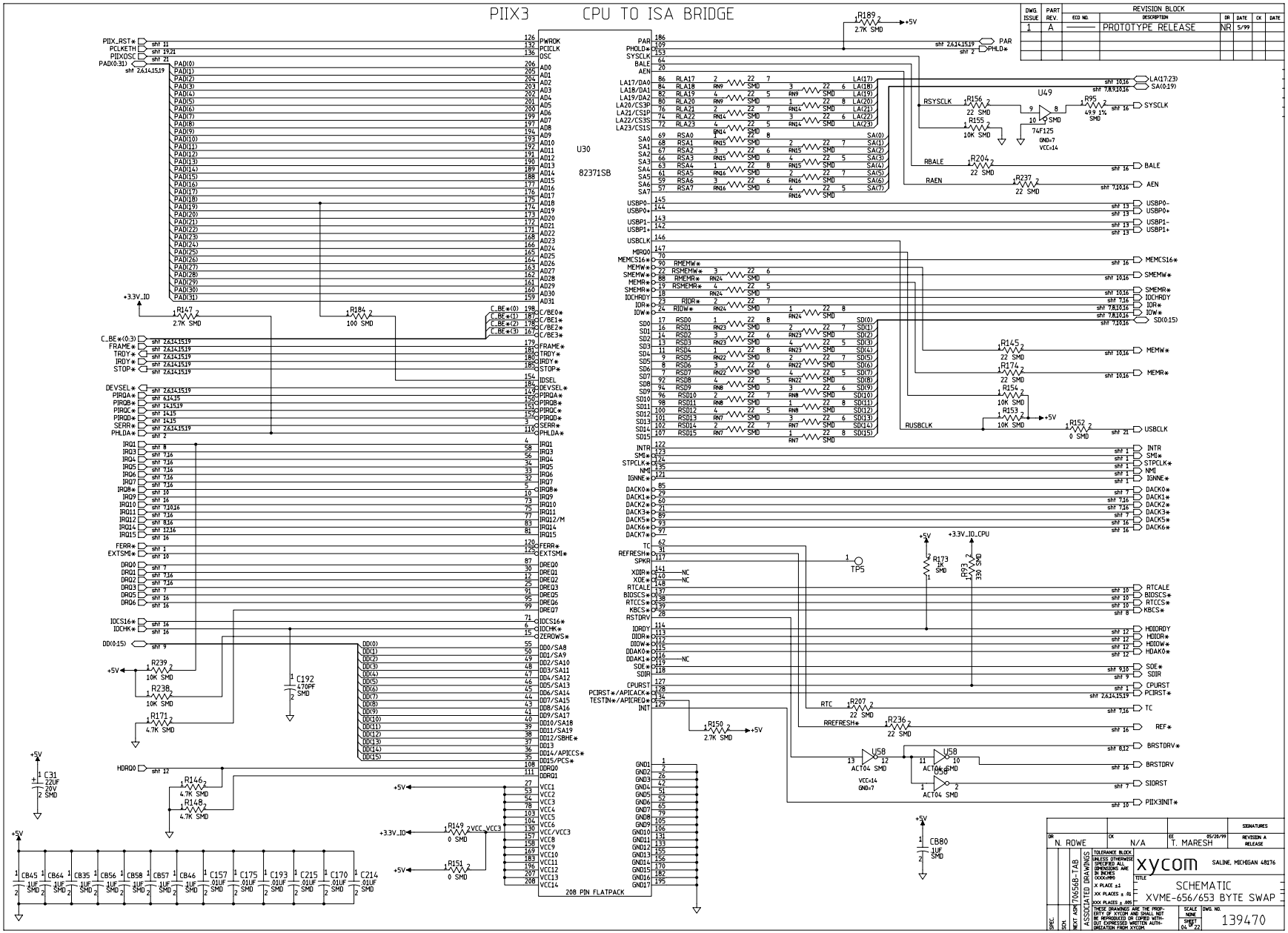
PIIX3 CPU TO ISA BRIDGE
U30
82371SB
208 PIN FLATPACK
U49
74F125
U58
ACT04
R189 2.7K SMD
R147 2.7K SMD
R184 100 SMD
R239 10K SMD
R238 10K SMD
R171 4.7K SMD
R146 4.7K SMD
R148 4.7K SMD
R149 0 SMD
R151 0 SMD
R150 2.7K SMD
R156 22 SMD
R155 10K SMD
R99 499 1% SMD
R204 22 SMD
R237 22 SMD
R145 22 SMD
R174 22 SMD
R154 10K SMD
R153 10K SMD
R152 0 SMD
R173 1K SMD
R207 22 SMD
R236 22 SMD
C192 470PF SMD
C31 22UF 20V SMD
CB45 CB64 CB35 CB56 CB58 CB57 CB46 C157 C175 C193 C215 C170 C214 .01UF SMD
CB80 1UF SMD
TP5
+5V
+3.3V_IO
+3.3V_IO_CPU
VCC_VCC3
PIIX_RST*
PCIKETH
PIIXOSC
PAD(0:31)
PAR
PHOLD*
SYSCLK
BALE
AEN
LA17/DA0
LA18/DA1
LA19/DA2
LA20/CS3P
LA21/CS1P
LA22/CS3S
LA23/CS1S
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
USBP0-
USBP0+
USBP1-
USBP1+
USBCLK
MIRQ0
MEMCS16*
MEMW*
SMEMW*
MEMR*
SMEMR*
IOCHRDY
IOR*
IOW*
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
RSYSCLK
RBALE
RAEN
RUSBCLK
C_BE*(0:3)
FRAME*
TRDY*
IRDY*
STOP*
DEVSEL*
PIRQA*
PIRQB*
PIRQC*
PIRQD*
SERR*
PHLDA*
IDSEL
IRQ1
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ8*
IRQ9
IRQ10
IRQ11
IRQ12
IRQ14
IRQ15
FERR*
EXTSMI*
DRQ0
DRQ1
DRQ2
DRQ3
DRQ5
DRQ6
IOCS16*
IOCHK*
DD(0:15)
HDRQ0
INTR
SMI*
STPCLK*
NMI
IGNNE*
DACK0*
DACK1*
DACK2*
DACK3*
DACK5*
DACK6*
DACK7*
TC
REFRESH*
SPKR
XDIR*
XOE*
RTCALE
BIOSCS*
RTCCS*
KBCS*
RSTDRV
IORDY
DIOR*
DIOW*
DDAK0*
DDAK1*
SOE*
SDIR
CPURST
PCIRST*/APICACK*
TESTIN*/APICREQ*
INIT
RTC
RREFRESH*
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
GND16
GND17
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
VCC/VCC3
VCC8
VCC9
VCC10
VCC11
VCC12
VCC13
VCC14
DD0/SA8
DD1/SA9
DD2/SA10
DD3/SA11
DD4/SA12
DD5/SA13
DD6/SA14
DD7/SA15
DD8/SA16
DD9/SA17
DD10/SA18
DD11/SA19
DD12/SBHE*
DD13
DD14/APICCS*
DD15/PCS*
DDRQ0
DDRQ1
LA(17:23)
SA(0:19)
SD(0:15)
MEMCS16*
SMEMW*
SMEMR*
IOCHRDY
IOR*
IOW*
MEMW*
MEMR*
USBCLK
INTR
SMI*
STPCLK*
NMI
IGNNE*
DACK0*
DACK1*
DACK2*
DACK3*
DACK5*
DACK6*
RTCALE
BIOSCS*
RTCCS*
KBCS*
MDIORDY
MDIOR*
MDIOW*
MDAK0*
SOE*
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CPURST
PCIRST*
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REF*
BRSTDRV*
BRSTDRV
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PIIX3INIT*
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NR
5/99
SIGNATURES
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N/A
T. MARESH
05/28/99
REVISION A RELEASE
TOLERANCE BLOCK
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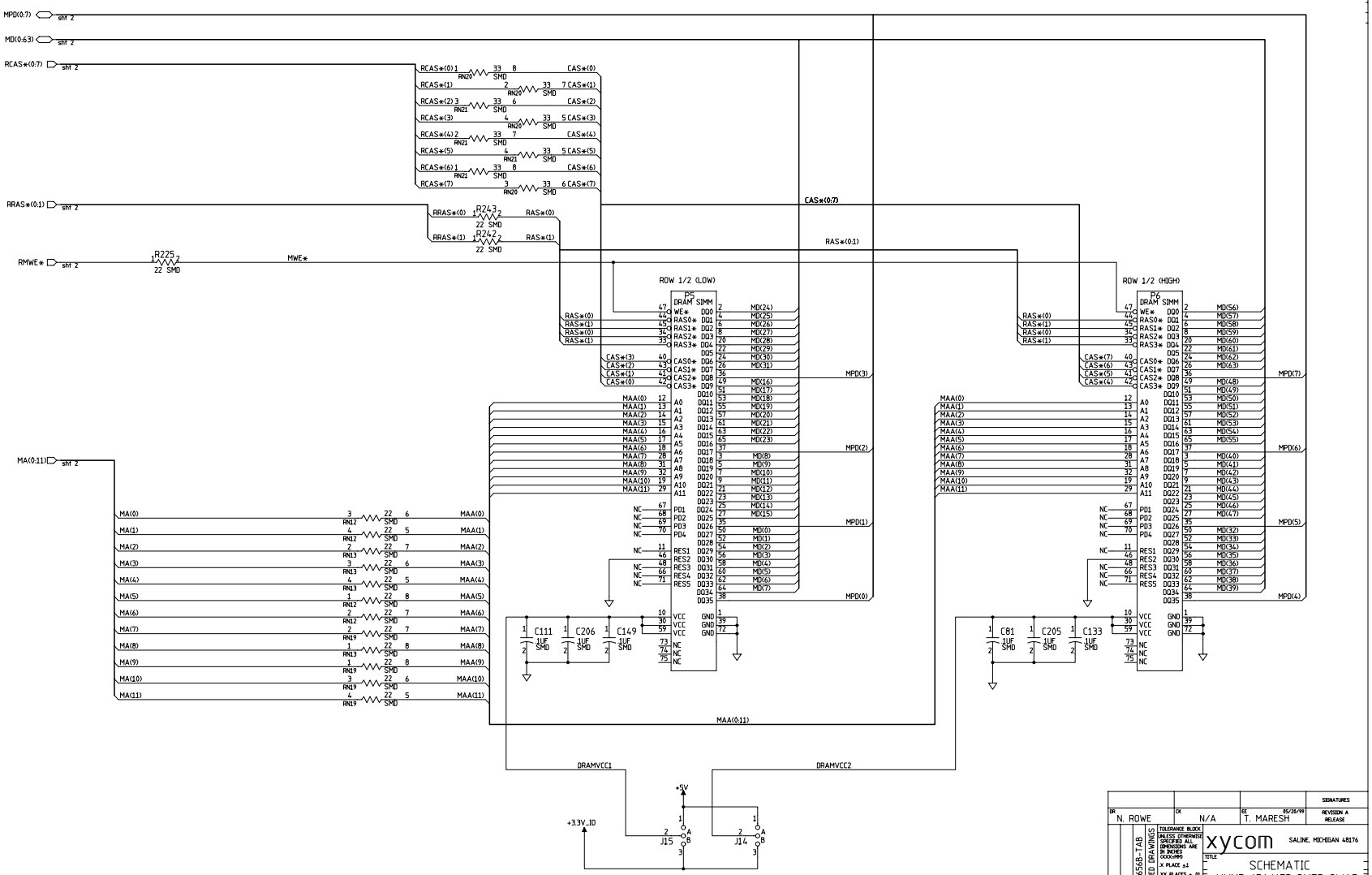
XVME-656/653 BYTE SWAP
SCALE NONE
DWG NO.
139470
SHEET 04 OF 22
DRFC
DSN
MKT
ASSOCIATED DRAWINGS
706568-TAB

DWG ISSUE	PART REV.	ECO NO.	DESCRIPTION	DR	DATE	CK	DATE
1	A	———	PROTOTYPE RELEASE	NR	5/99		

DRAM CONNECTORS



				SIGNATURES
DR N. ROWE	CK N/A	EE 05/28/99 T. MARESH		REVISION A RELEASE

TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
DECIMALS
X PLACE ±.1
XX PLACES ± .01
XXX PLACES ± .005
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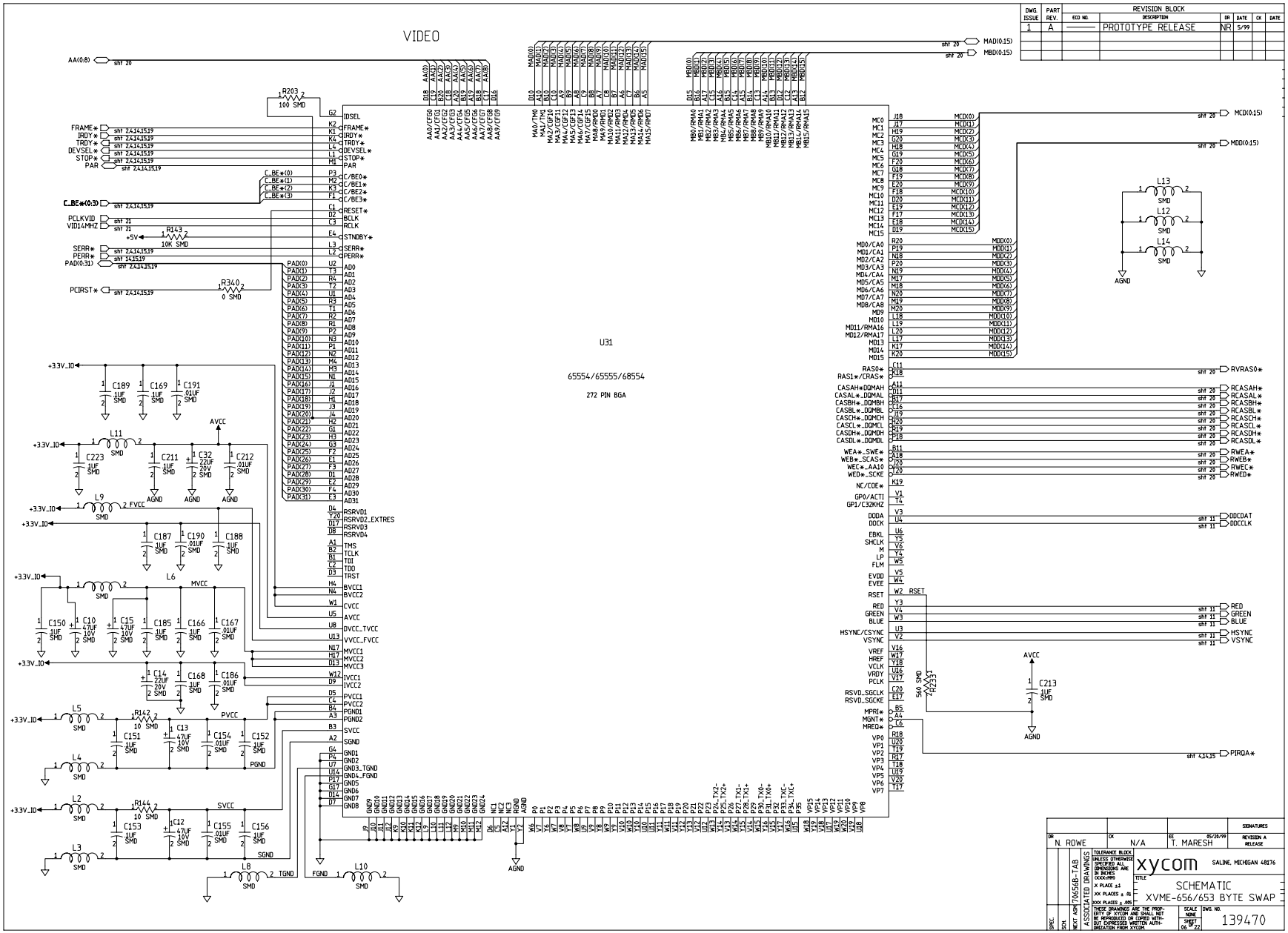
SALINE, MICHIGAN 48176

TITLE
SCHEMATIC
XVME-656/653 BYTE SWAP

SCALE NONE
DWG. NO. 139470
SHEET 05 OF 22

NEXT ASSY 706568-TAB
ASSOCIATED DRAWINGS
DES.
DRFC.


VIDEO
U31
65554/65555/68554
272 PIN BGA
REVISION BLOCK
PROTOTYPE RELEASE
SCHEMATIC
XVME-656/653 BYTE SWAP
SALINE, MICHIGAN 48176
N. ROWE
T. MARESH
139470

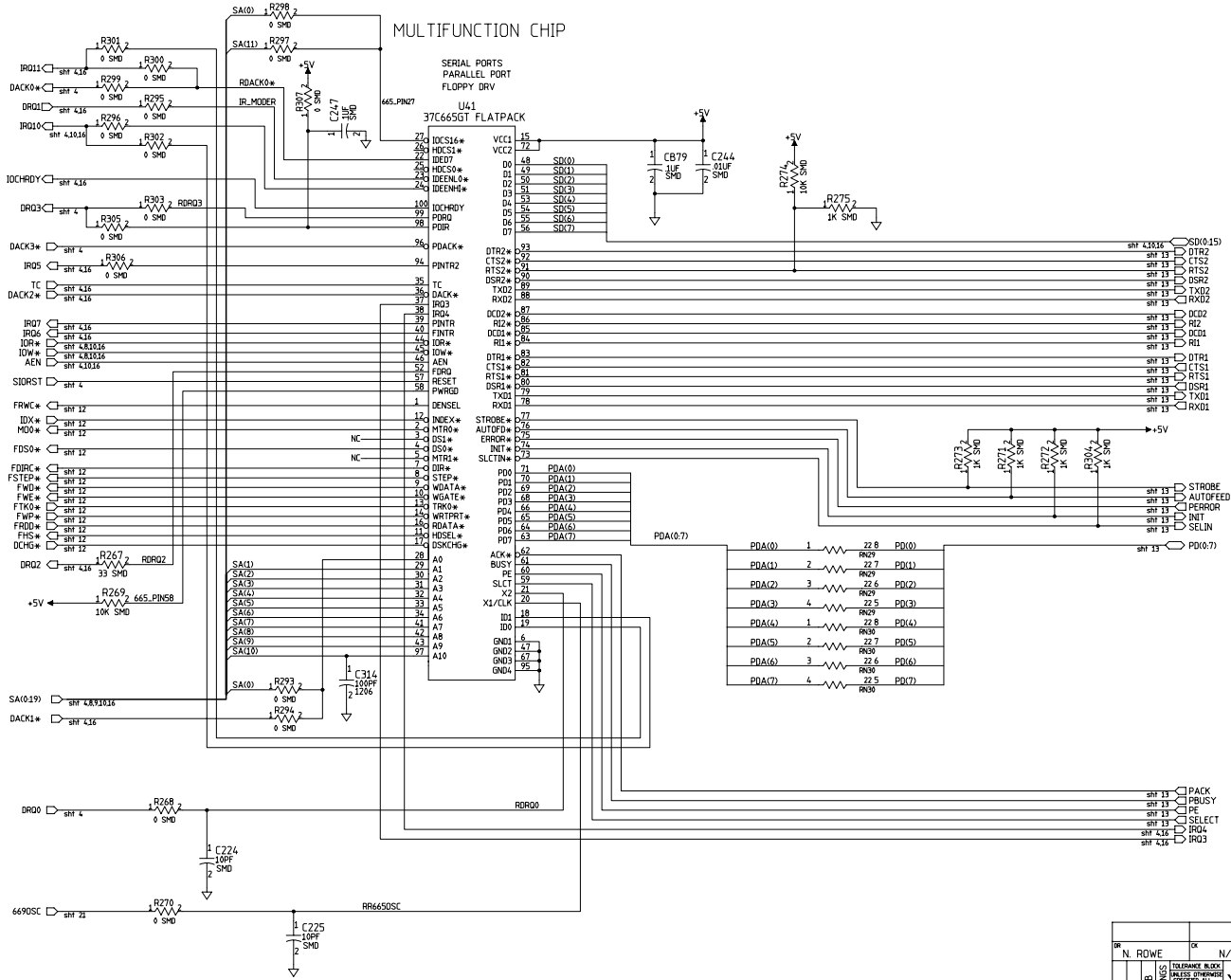
DWG. ISSUE	PART REV.	ECO NO.	DESCRIPTION	DR	DATE	CK	DATE
1	A	———	PROTOTYPE RELEASE	NR	5/99		

SUPPORTS: SMC669 ALI M5113

MULTIFUNCTION CHIP

SERIAL PORTS
PARALLEL PORT
FLOPPY DRV

U41
37C665GT FLATPACK



				SIGNATURES
DR N. ROWE	CK N/A	EE 05/28/99 T. MARESH		REVISION A RELEASE

TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
DECIMALS
X PLACE ±.1
XX PLACE ± .01
XXX PLACE ± .005

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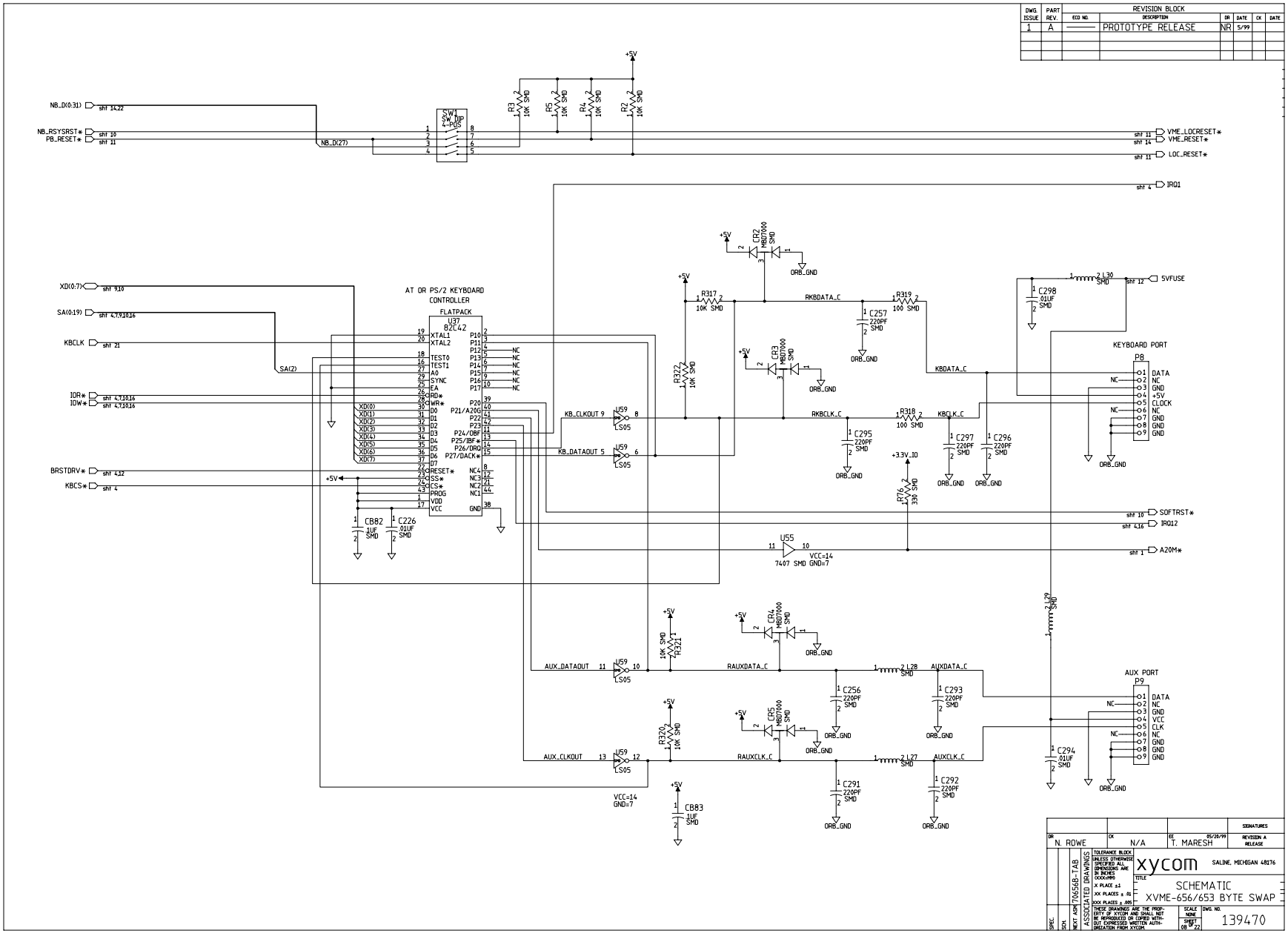
TITLE
SCHEMATIC
XVME-656/653 BYTE SWAP

SCALE NONE
SHEET 07 OF 22
DWG. NO. 139470

NEXT ASSY 706568-TAB
ASSOCIATED DRAWINGS
DES.
DRFT.


REVISION BLOCK
DWG ISSUE
PART REV.
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
1
A
PROTOTYPE RELEASE
NR
5/99
NB_D(0:31)
NB_RSYSRST*
PB_RESET*
NB_D(27)
SW1
SW DIP 4-POS
R3 10K SMD
R5 10K SMD
R4 10K SMD
R2 10K SMD
+5V
VME_LOCRESET*
VME_RESET*
LOC_RESET*
IRQ1
XD(0:7)
SA(0:19)
KBCLK
SA(2)
IOR*
IOW*
BRSTDRV*
KBCS*
AT OR PS/2 KEYBOARD CONTROLLER
FLATPACK
U37
82C42
XTAL1
XTAL2
TEST0
TEST1
A0
SYNC
EA
RD*
WR*
RESET*
SS*
CS*
PROG
VDD
VCC
P10
P11
P12
P13
P14
P15
P16
P17
P20
P21/A20G
P22
P23
P24/OBF
P25/IBF*
P26/DRQ
P27/DACK*
NC4
NC3
NC2
NC1
GND
CB82 1UF SMD
C226 .01UF SMD
CR2 MBD7000 SMD
CR3 MBD7000 SMD
CR4 MBD7000 SMD
CR5 MBD7000 SMD
ORB_GND
R317 10K SMD
R322 10K SMD
R319 100 SMD
R318 100 SMD
R320 10K SMD
R321 10K SMD
RKBDATA_C
KBDATA_C
RKBCLK_C
KBCLK_C
KB_CLKOUT 9
KB_DATAOUT 5
AUX_DATAOUT 11
AUX_CLKOUT 13
U59 LS05
C257 220PF SMD
C295 220PF SMD
C297 220PF SMD
C296 220PF SMD
C256 220PF SMD
C293 220PF SMD
C291 220PF SMD
C292 220PF SMD
C294 .01UF SMD
CB83 1UF SMD
+3.3V_IO
R76 330 SMD
L30 SMD
L29 SMD
L28 SMD
L27 SMD
C298 .01UF SMD
5VFUSE
KEYBOARD PORT
P8
DATA
NC
GND
+5V
CLOCK
AUX PORT
P9
VCC
CLK
SOFTRST*
IRQ12
A20M*
U55
7407 SMD GND=7
VCC=14
RAUXDATA_C
AUXDATA_C
RAUXCLK_C
AUXCLK_C
VCC=14 GND=7
DR N. ROWE
CK N/A
EE T. MARESH 05/28/99
SIGNATURES
REVISION A RELEASE
TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
DECIMALS
X PLACE ±1
XX PLACES ± .01
XXX PLACES ± .005
ANGLES ± 1°
NEXT ASSY 706568-TAB
ASSOCIATED DRAWINGS
SPEC
DES
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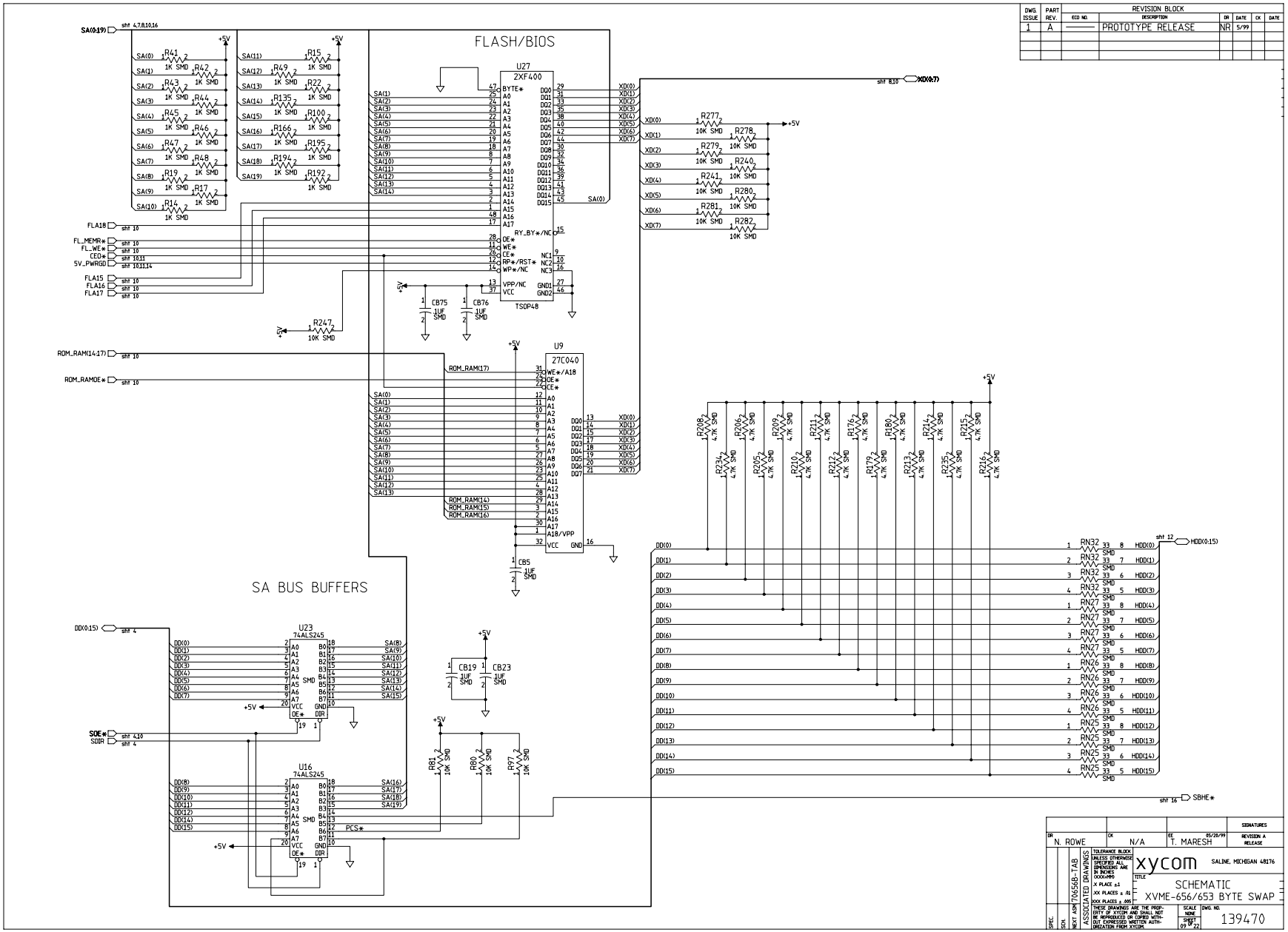
SALINE, MICHIGAN 48176
TITLE
SCHEMATIC
XVME-656/653 BYTE SWAP
SCALE NONE
SHEET 08 OF 22
DWG NO.
139470


FLASH/BIOS
SA BUS BUFFERS
U27
2XF400
TSOP48
U9
27C040
U23
74ALS245
U16
74ALS245
REVISION BLOCK
DWG. ISSUE
PART REV.
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
1
A
PROTOTYPE RELEASE
NR
5/99
SIGNATURES
N. ROWE
N/A
T. MARESH
05/26/99
REVISION A RELEASE
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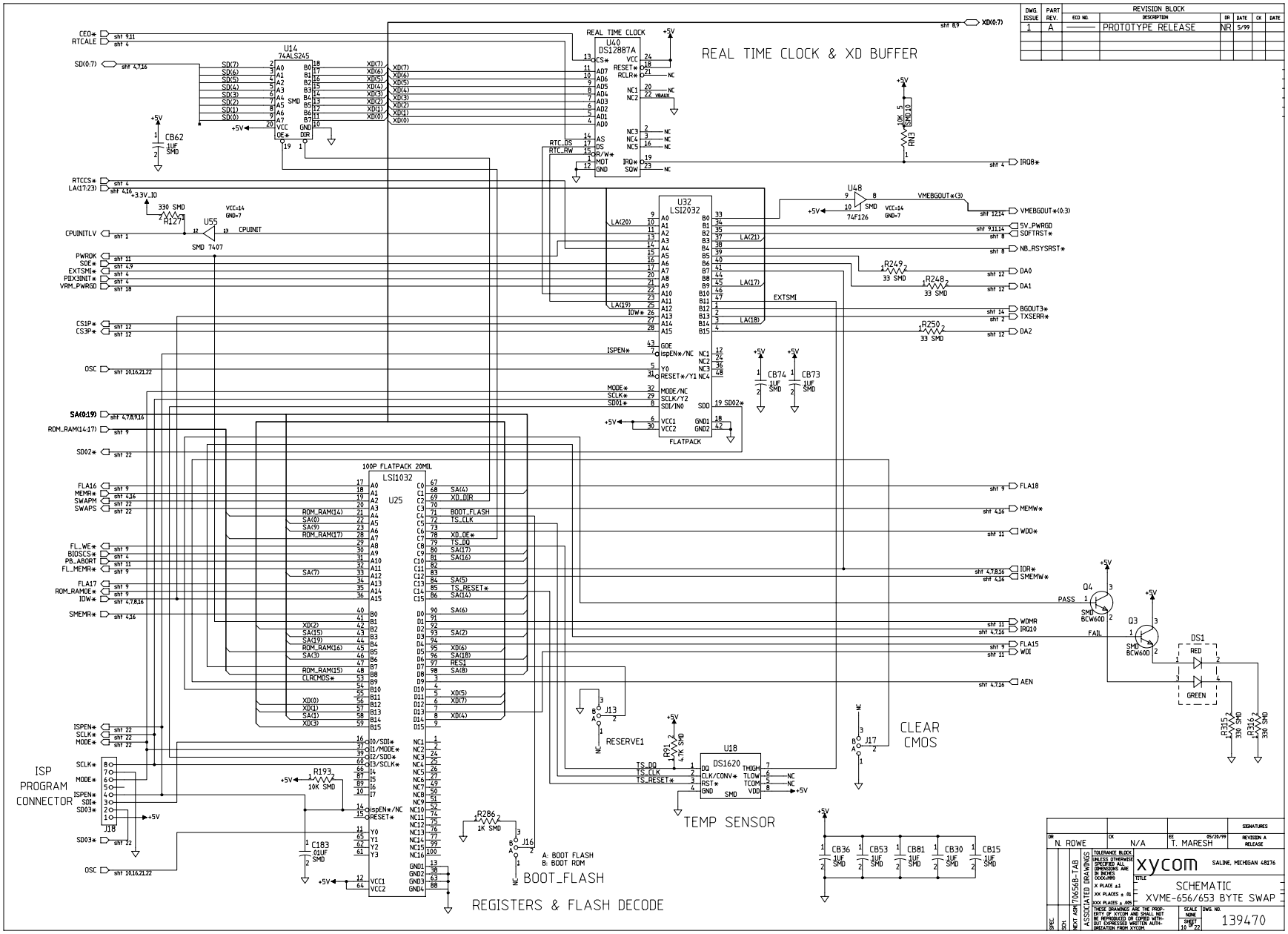
SALINE, MICHIGAN 48176
SCHEMATIC
XVME-656/653 BYTE SWAP
SCALE NONE
DWG. NO.
139470
SHEET 09 22


REAL TIME CLOCK & XD BUFFER
U14 74ALS245
U40 DS12887A
REAL TIME CLOCK
U32 LSI2032
U48 74F126
U55 SMD 7407
U25 LSI1032
100P FLATPACK 20MIL
FLATPACK
U18 DS1620
TEMP SENSOR
REGISTERS & FLASH DECODE
BOOT_FLASH
A: BOOT FLASH
B: BOOT ROM
RESERVE1
CLEAR CMOS
ISP PROGRAM CONNECTOR
J18
J13
J16
J17
R193 10K SMD
R286 1K SMD
R91 4.7K SMD
RN3 10K SMD
R249 33 SMD
R248 33 SMD
R250 33 SMD
R315 330 SMD
R316 330 SMD
CB62 1UF SMD
CB74 1UF SMD
CB73 1UF SMD
CB36 1UF SMD
CB53 1UF SMD
CB81 1UF SMD
CB30 1UF SMD
CB15 1UF SMD
C183 .01UF SMD
R127 330 SMD
Q4 SMD BCW60D
Q3 SMD BCW60D
DS1 RED GREEN
PASS
FAIL
EXTSMI
SA(0:19)
XD(0:7)
IRQ8*
VMEBGOUT*(0:3)
5V_PWRGD
SOFTRST*
NB_RSYSRST*
DA0
DA1
DA2
BGOUT3*
TXSERR*
FLA18
MEMW*
WDO*
IOR*
SMEMW*
WDMR
IRQ10
FLA15
WDI
AEN
REVISION BLOCK
PROTOTYPE RELEASE
SIGNATURES
N. ROWE
T. MARESH
05/28/99
REVISION A RELEASE
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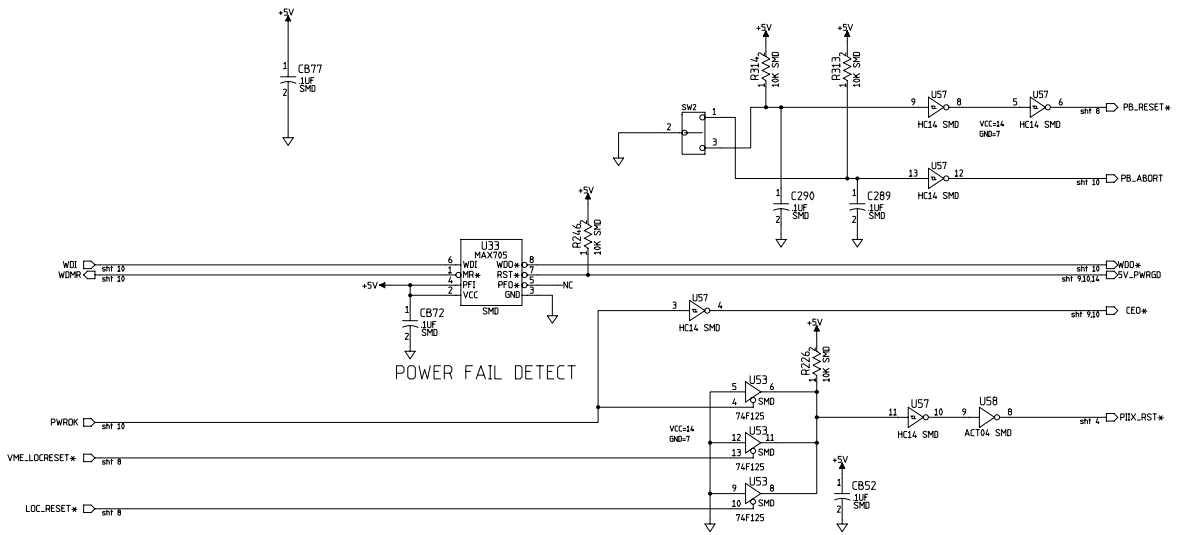
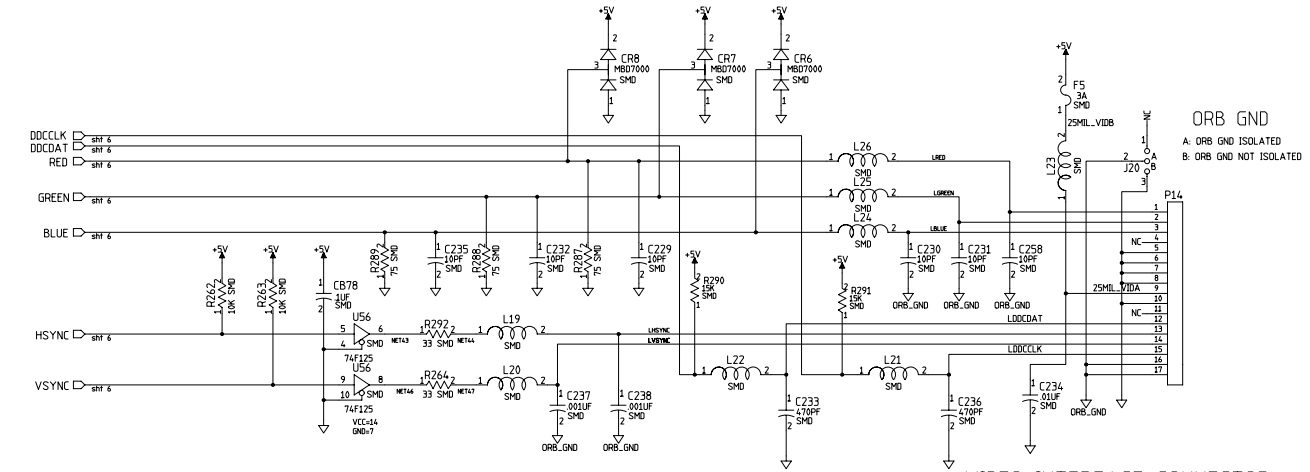
SCHEMATIC
XVME-656/653 BYTE SWAP
139470

DWG ISSUE	PART REV.	REVISION BLOCK ECO NO.	DESCRIPTION	DR	DATE	CK	DATE
1	A	———	PROTOTYPE RELEASE	NR	5/99		





VIDEO INTERFACE CONNECTOR

			SIGNATURES
DR N. ROWE	CK N/A	EE 05/28/99 T. MARESH	REVISION A RELEASE

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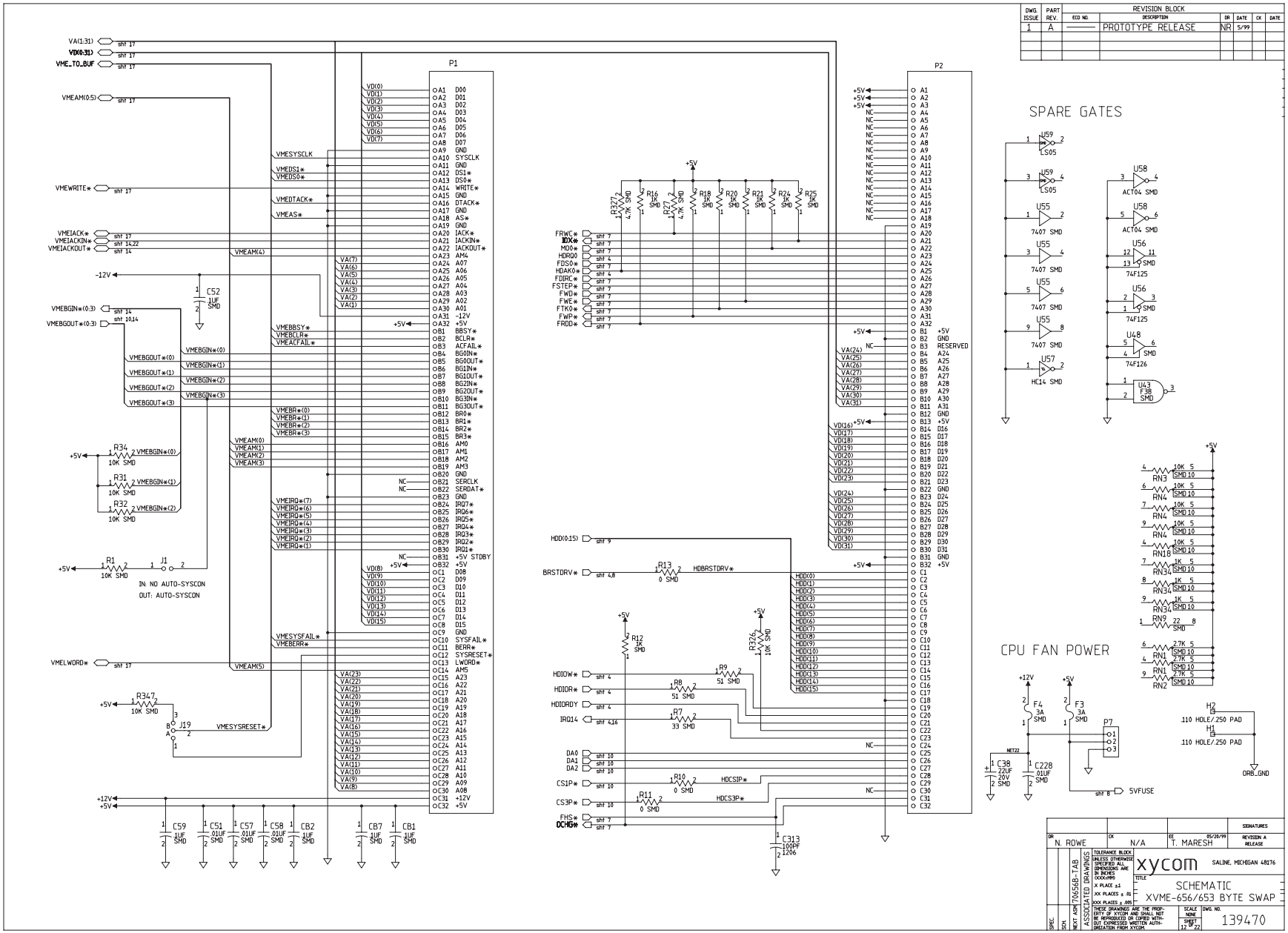
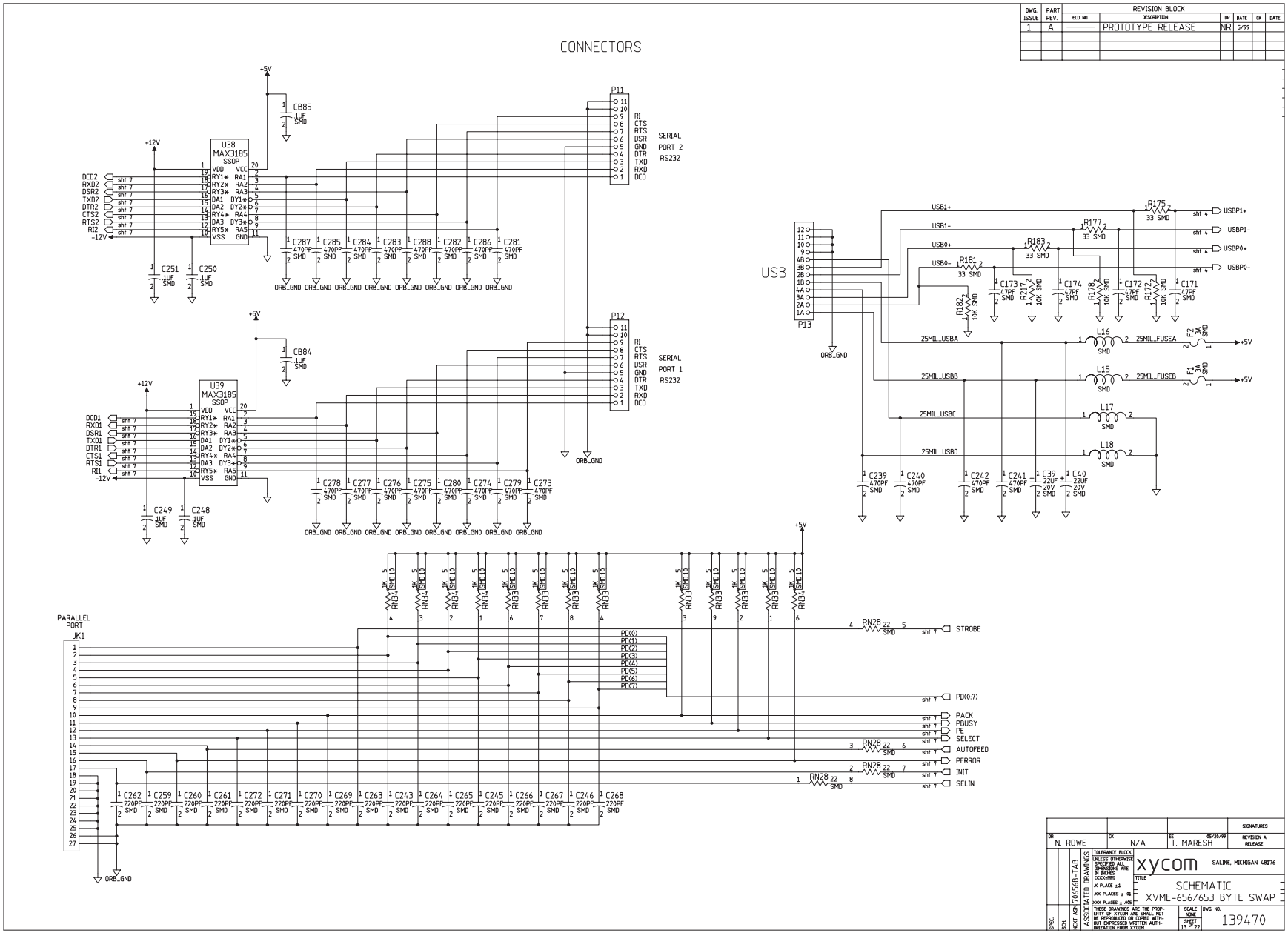
TITLE: SCHEMATIC XVME-656/653 BYTE SWAP

SCALE NONE | DWG. NO. 139470 | SHEET 11 OF 22

NEXT ASSY 706568-TAB ASSOCIATED DRAWINGS

TOLERANCE BLOCK UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES XXX=±.005


REVISION BLOCK
DWG ISSUE
PART REV.
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
1
A
PROTOTYPE RELEASE
NR
5/99
P1
P2
SPARE GATES
CPU FAN POWER
IN: NO AUTO-SYSCON
OUT: AUTO-SYSCON
SCHEMATIC
XVME-656/653 BYTE SWAP
xycom
SALINE, MICHIGAN 48176
139470


CONNECTORS
REVISION BLOCK
DWG. ISSUE
PART REV.
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
1
A
PROTOTYPE RELEASE
NR
5/99
U38
MAX3185
SSOP
U39
MAX3185
SSOP
P11
P12
P13
SERIAL PORT 2 RS232
SERIAL PORT 1 RS232
USB
PARALLEL PORT
JK1
STROBE
PD(0:7)
PACK
PBUSY
PE
SELECT
AUTOFEED
PERROR
INIT
SELIN
ORB_GND
+5V
+12V
-12V
SIGNATURES
N. ROWE
N/A
T. MARESH
05/28/99
REVISION A RELEASE
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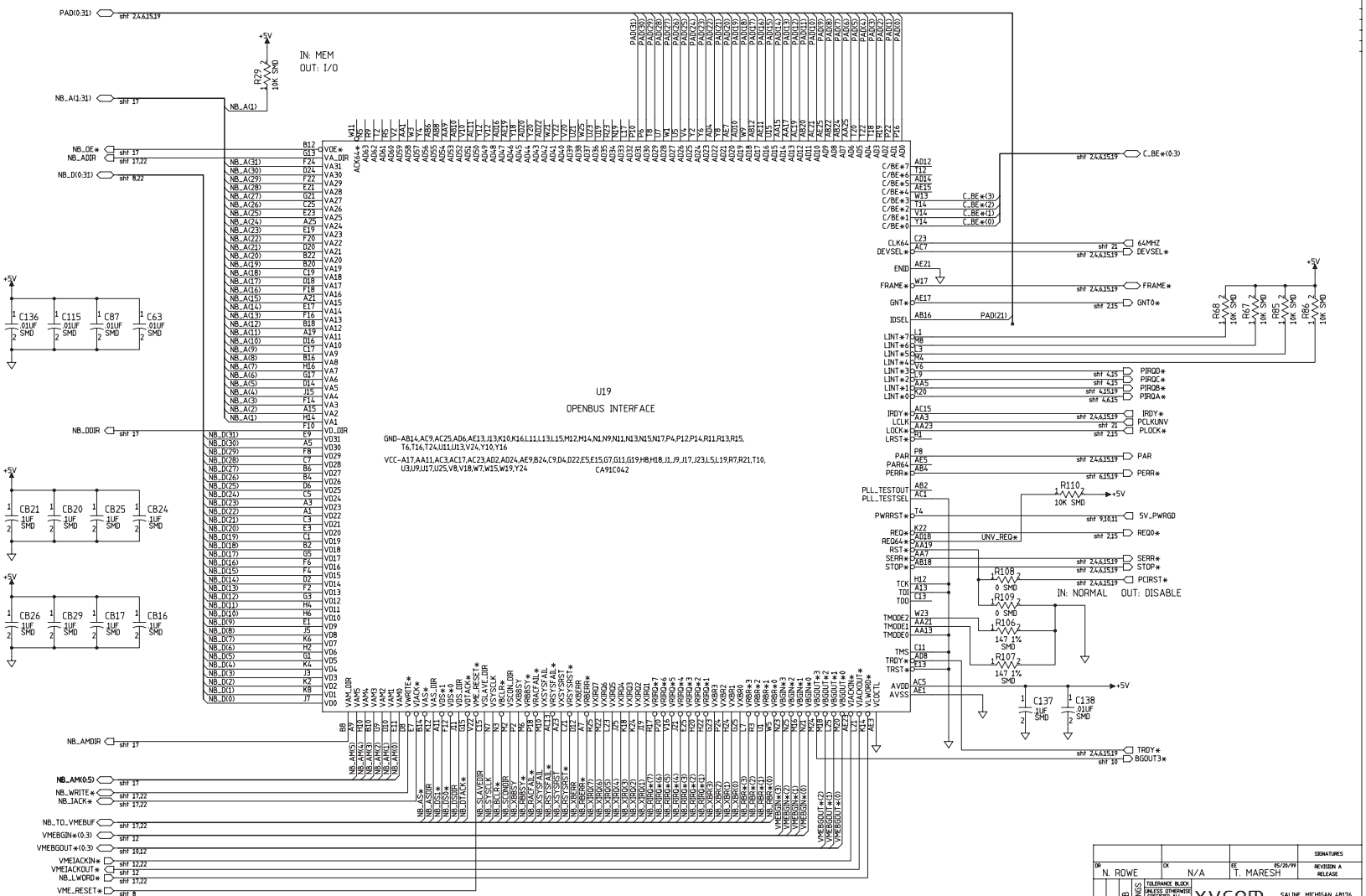
SCHEMATIC
XVME-656/653 BYTE SWAP
139470

PCI TO VME INTERFACE

DWG. ISSUE	PART REV.	REVISION BLOCK ECO NO.	DESCRIPTION	DR	DATE	CK	DATE
1	A	———	PROTOTYPE RELEASE	NR	5/99		



DR	CK	EE	SIGNATURES
N. ROWE	N/A	05/28/99 T. MARESH	REVISION A RELEASE

ASSOCIATED DRAWINGS: SPEC. 706568-TAB; SCH. ABM

TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
DECIMALS
X PLACE ±.1
XX PLACES ± .01
XXX PLACES ± .005

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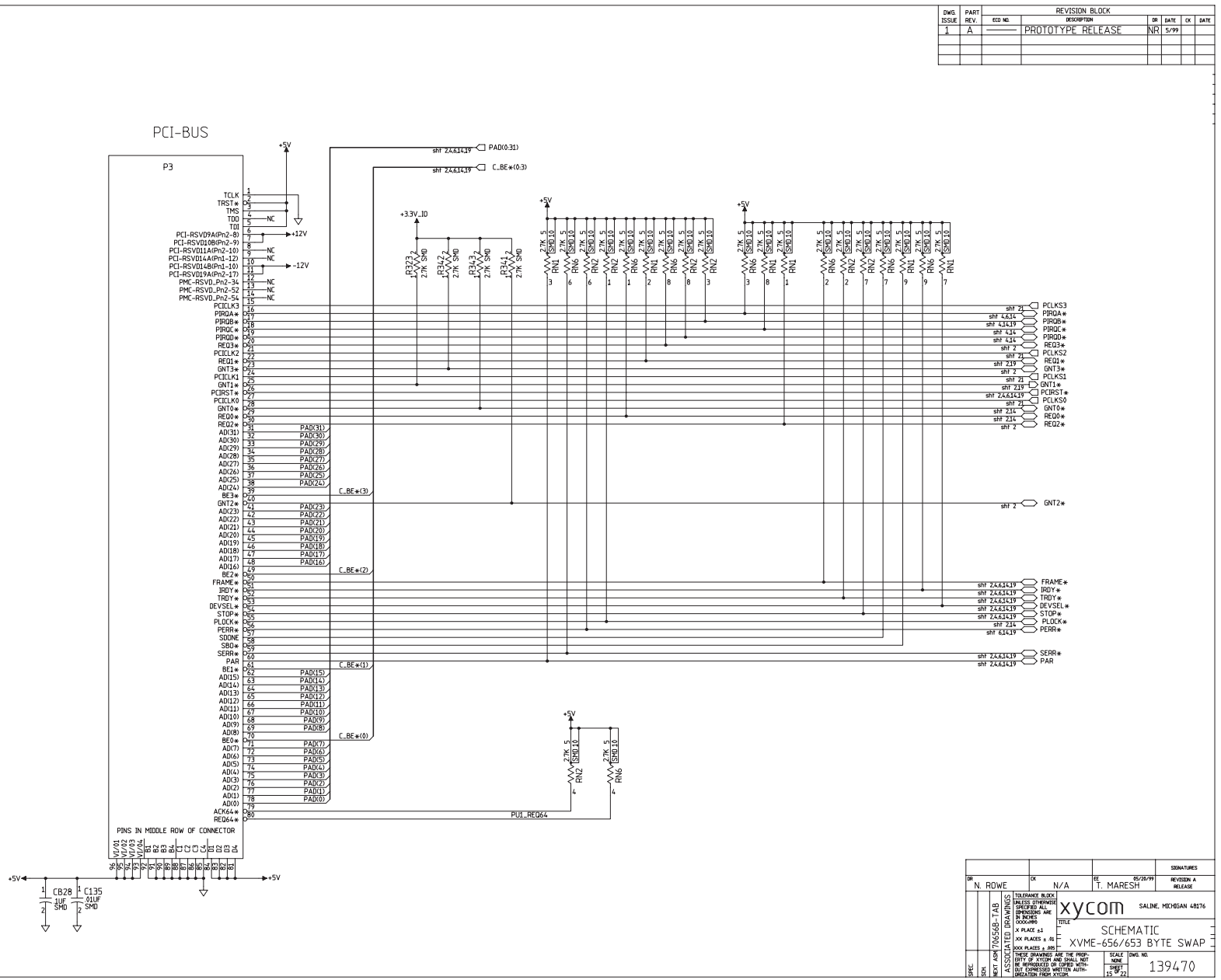
SALINE, MICHIGAN 48176

TITLE
SCHEMATIC
XVME-656/653 BYTE SWAP

SCALE NONE
SHEET 14 OF 22
DWG. NO. 139470



DWG. ISSUE	PART REV.	ECO NO.	DESCRIPTION	DR	DATE	CK	DATE
1	A	———	PROTOTYPE RELEASE	NR	5/99		

			SIGNATURES
DR N. ROWE	CK N/A	EE 05/28/99 T. MARESH	REVISION A RELEASE

TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
DECIMALS
X PLACE ±1
XX PLACES ± .01
XXX PLACES ± .005
ANGLES ± 1°

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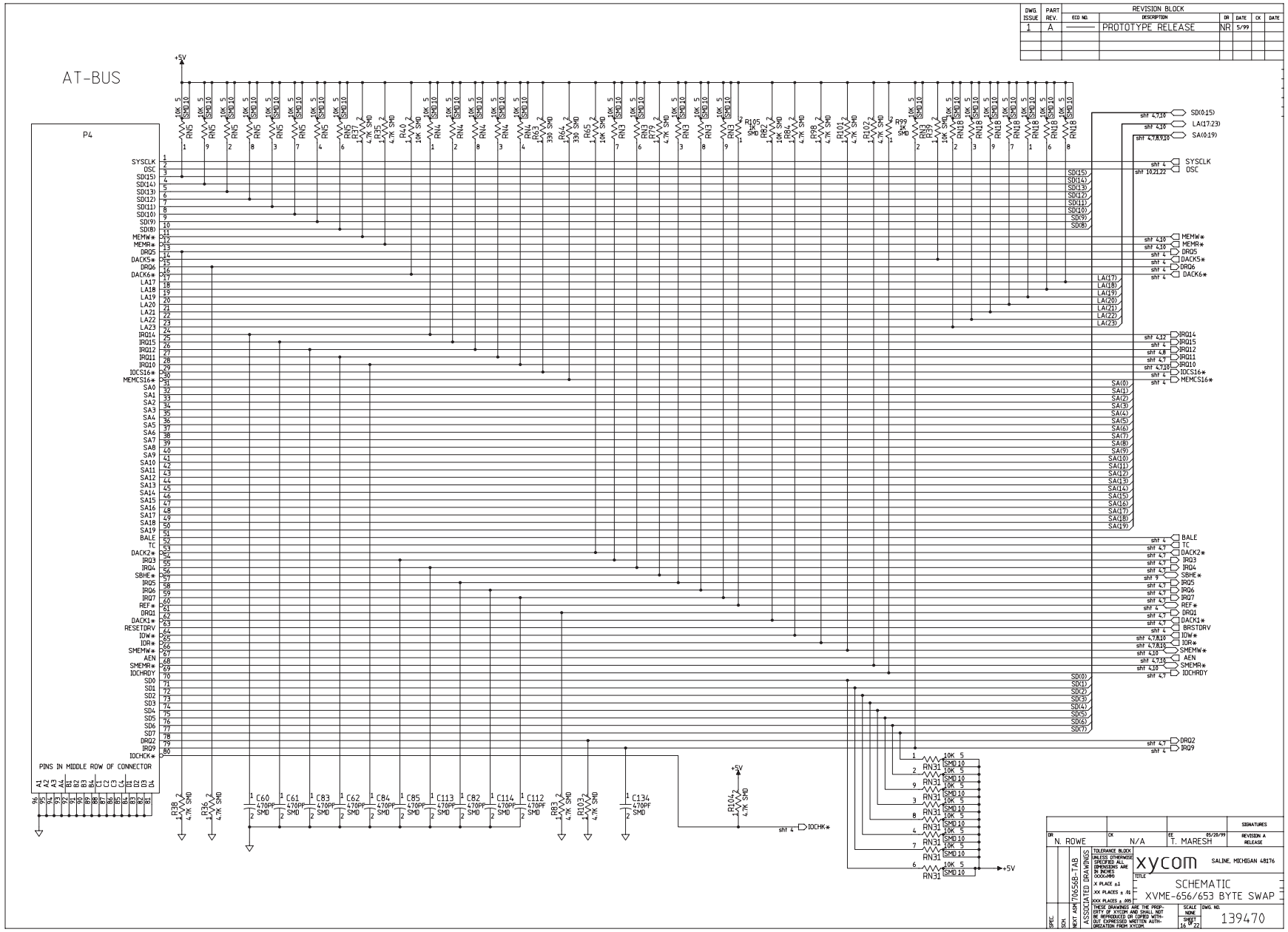
SALINE, MICHIGAN 48176

TITLE
SCHEMATIC
XVME-656/653 BYTE SWAP

SCALE NONE
SHEET 15 OF 22
DWG. NO. 139470

NEXT ASSY 706568-TAB
ASSOCIATED DRAWINGS
SPEC.
DESN.


AT-BUS
P4
PINS IN MIDDLE ROW OF CONNECTOR
REVISION BLOCK
DWG ISSUE
PART REV.
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
1
A
PROTOTYPE RELEASE
NR
5/99
N. ROWE
N/A
T. MARESH
05/28/99
SIGNATURES
REVISION A RELEASE
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SALINE, MICHIGAN 48176
SCHEMATIC
XVME-656/653 BYTE SWAP
139470
SCALE NONE
SHEET 16 OF 22
TOLERANCE BLOCK
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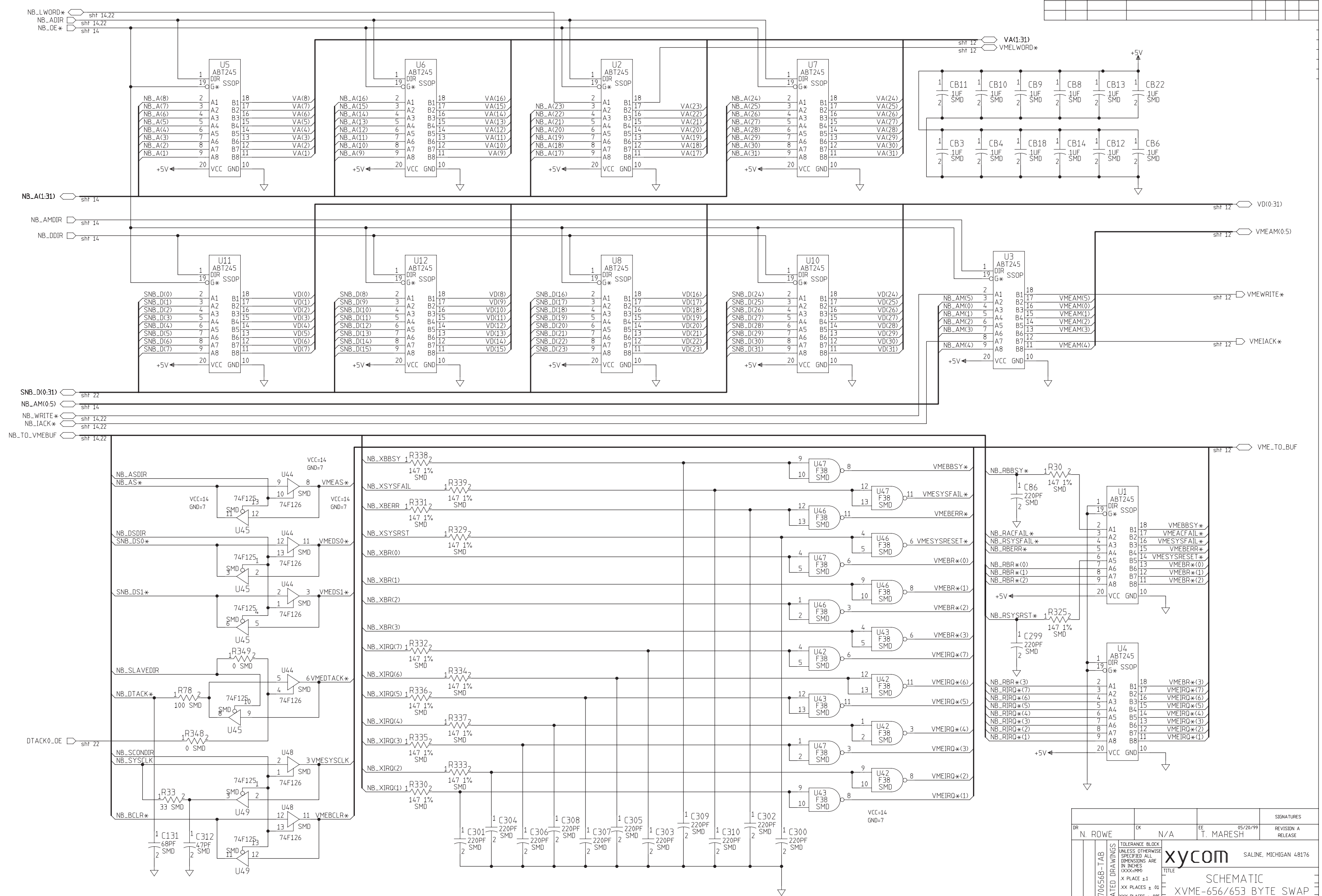
NEXT ASSY 706568-TAB
ASSOCIATED DRAWINGS

VME BUFFERS



DWG ISSUE	PART REV.	ECO NO.	DESCRIPTION	DR	DATE	CK	DATE
1	A	——	PROTOTYPE RELEASE	NR	5/99		

DR N. ROWE | CK N/A | EE T. MARESH 05/20/99 | SIGNATURES: REVISION A RELEASE

NEXT ASM 70656B-TAB

ASSOCIATED DRAWINGS

TOLERANCE BLOCK: UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (XXX=MM); X PLACE ±1; XX PLACES ± .01; XXX PLACES ± .005

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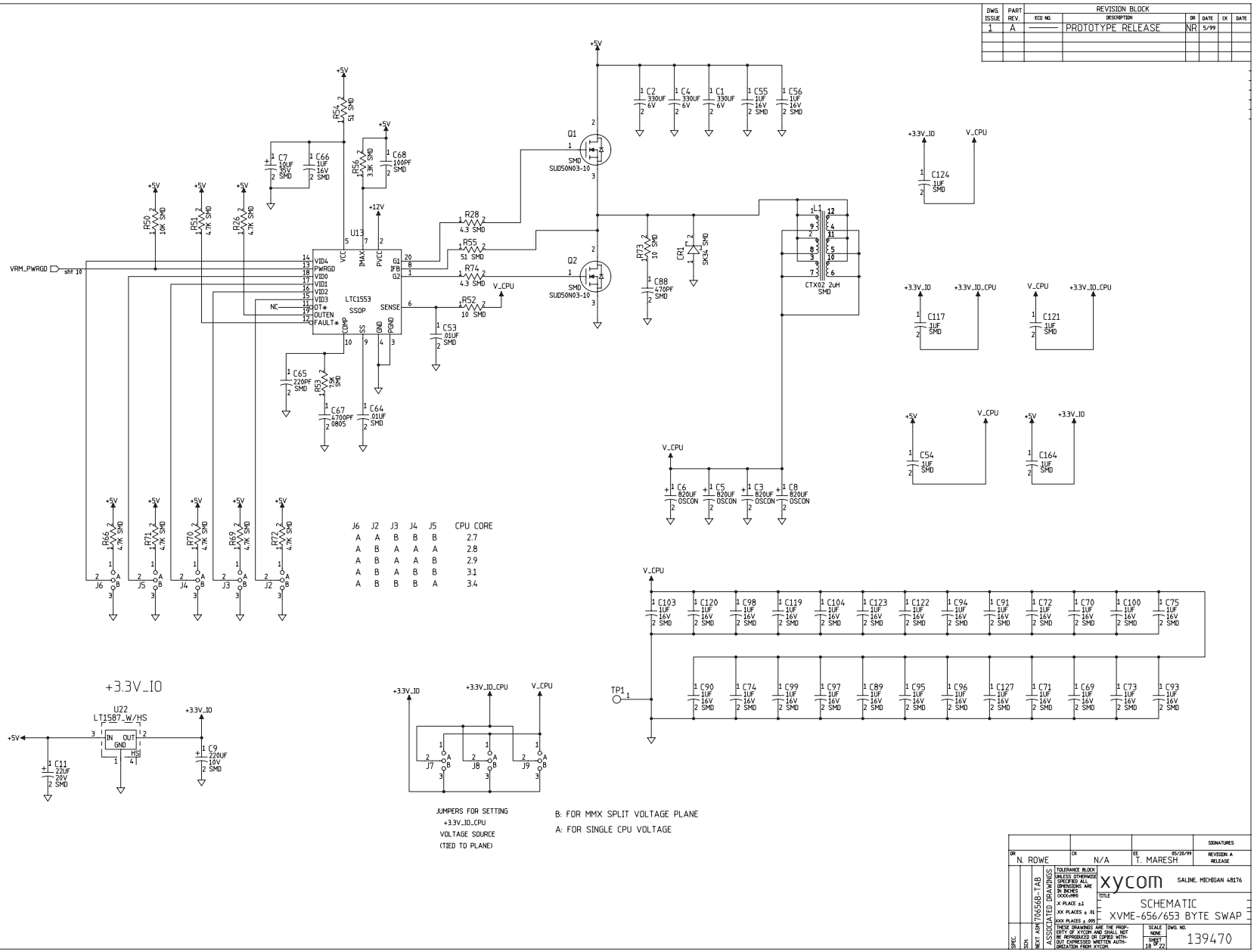
TITLE: SCHEMATIC XVME-656/653 BYTE SWAP

SCALE NONE | SHEET 17 OF 22 | DWG. NO. 139470


REVISION BLOCK
DWG. ISSUE
PART REV.
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
1
A
PROTOTYPE RELEASE
NR
5/99
U13
LTC1553
SSOP
VID4
PWRGD
VID0
VID1
VID2
VID3
OUT*
OUTEN
FAULT*
COMP
SS
GND
PGND
VCC
IMAX
PVCC
G1
G2
IFB
SENSE
VRM_PWRGD
sht 10
NC
Q1
Q2
SMD
SUD50N03-10
CTX02 2uH
SMD
SK34
U22
LT1587_W/HS
IN
OUT
GND
HSK
+3.3V_IO
V_CPU
+3.3V_IO_CPU
+5V
+12V
J6 J2 J3 J4 J5 CPU CORE
A A B B B 2.7
A B A A A 2.8
A B A A B 2.9
A B A B B 3.1
A B B B A 3.4
JUMPERS FOR SETTING
+3.3V_IO_CPU
VOLTAGE SOURCE
(TIED TO PLANE)
B: FOR MMX SPLIT VOLTAGE PLANE
A: FOR SINGLE CPU VOLTAGE
TP1
SIGNATURES
N. ROWE
N/A
05/28/99
T. MARESH
REVISION A RELEASE
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SALINE, MICHIGAN 48176
SCHEMATIC
XVME-656/653 BYTE SWAP
139470
SCALE NONE
SHEET 18 OF 22
TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
XXX PLACES ± .005
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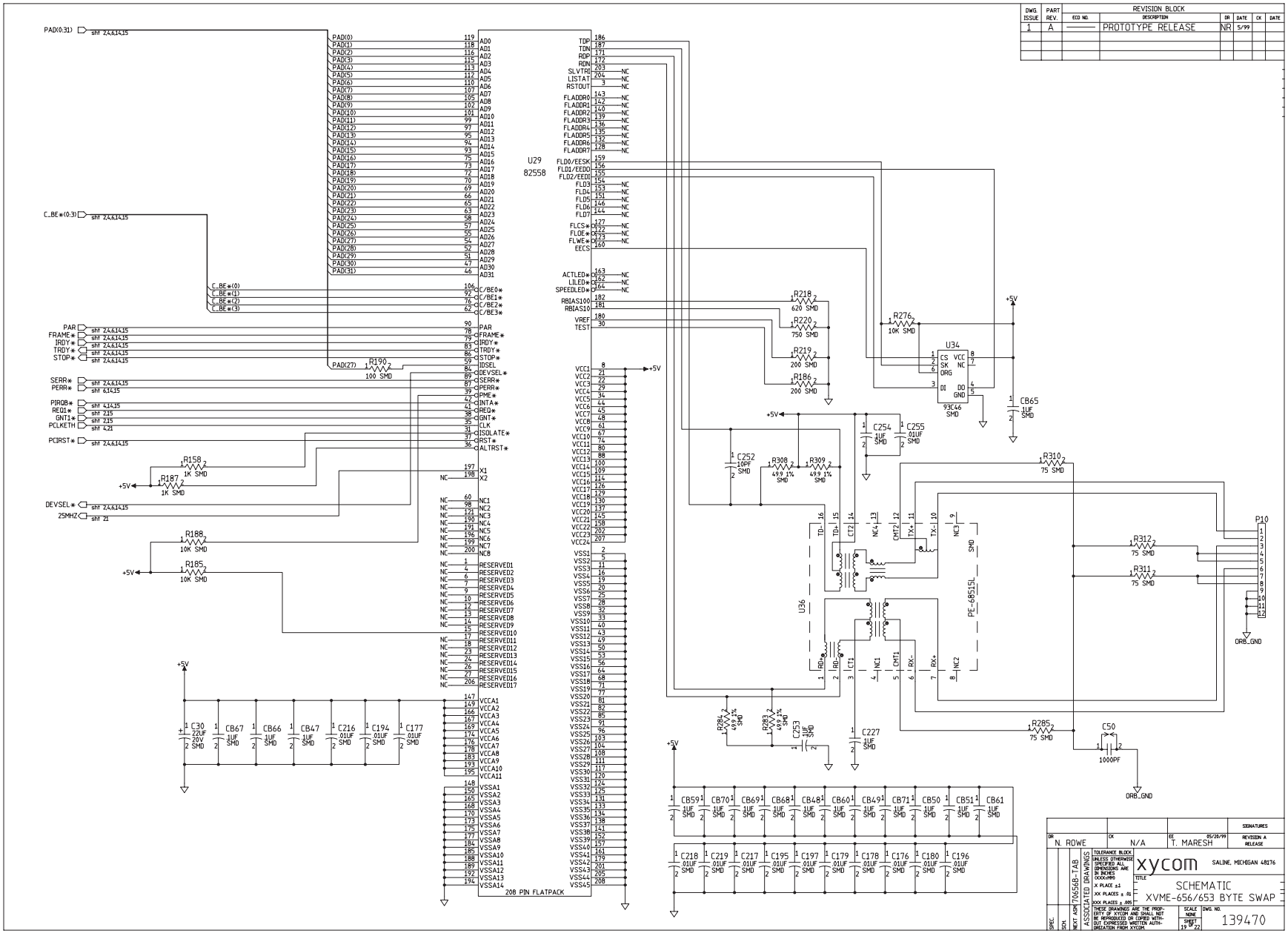
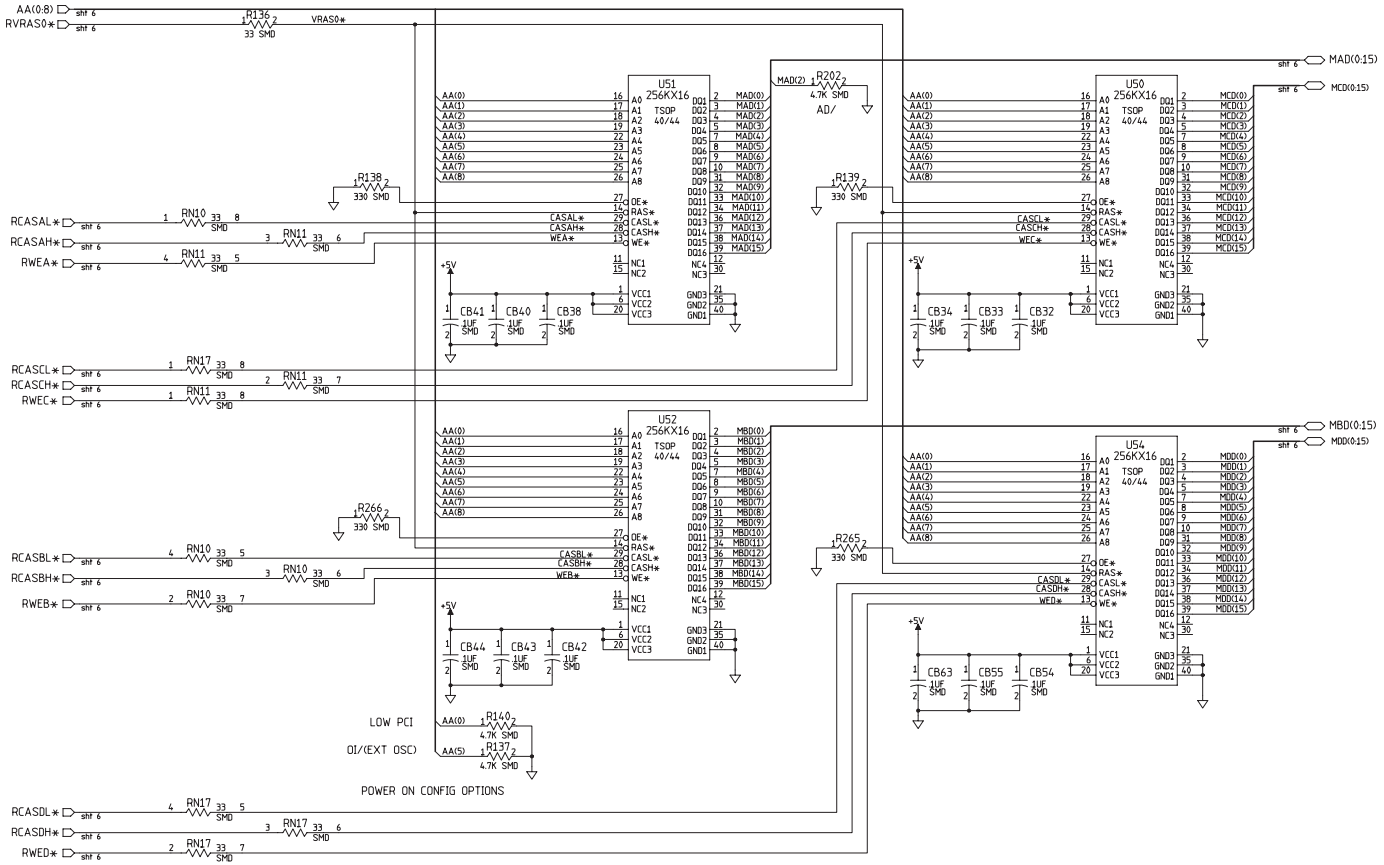

REVISION BLOCK
DWG. ISSUE
PART REV.
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
1
A
PROTOTYPE RELEASE
NR
5/99
U29
82558
208 PIN FLATPACK
U34
93C46 SMD
U36
PE-68515L SMD
P10
ORB_GND
R218 620 SMD
R220 750 SMD
R219 200 SMD
R186 200 SMD
R276 10K SMD
R158 1K SMD
R187 1K SMD
R188 10K SMD
R185 10K SMD
R190 100 SMD
R308 499 1% SMD
R309 499 1% SMD
R310 75 SMD
R312 75 SMD
R311 75 SMD
R285 75 SMD
R284 499 1% SMD
R283 499 1% SMD
C30 22UF 20V SMD
C50 1000PF
C252 100PF SMD
C253 1UF SMD
C254 1UF SMD
C255 .01UF SMD
C227 1UF SMD
C65 1UF SMD
CB59 CB70 CB69 CB68 CB48 CB60 CB49 CB71 CB50 CB51 CB61
C218 C219 C217 C195 C197 C179 C178 C176 C180 C196
SCHEMATIC
XVME-656/653 BYTE SWAP
SALINE, MICHIGAN 48176
xycom
N. ROWE
N/A
T. MARESH
05/28/99
SIGNATURES
REVISION A RELEASE
SCALE NONE
DWG. NO. 139470
SHEET 19 OF 22

DWG. ISSUE	PART REV.	REVISION BLOCK ECO NO.	DESCRIPTION	DR	DATE	CK	DATE
1	A	———	PROTOTYPE RELEASE	NR	5/99		

MEMORY INTERFACE



			SIGNATURES
DR N. ROWE	CK N/A	EE 05/28/99 T. MARESH	REVISION A RELEASE

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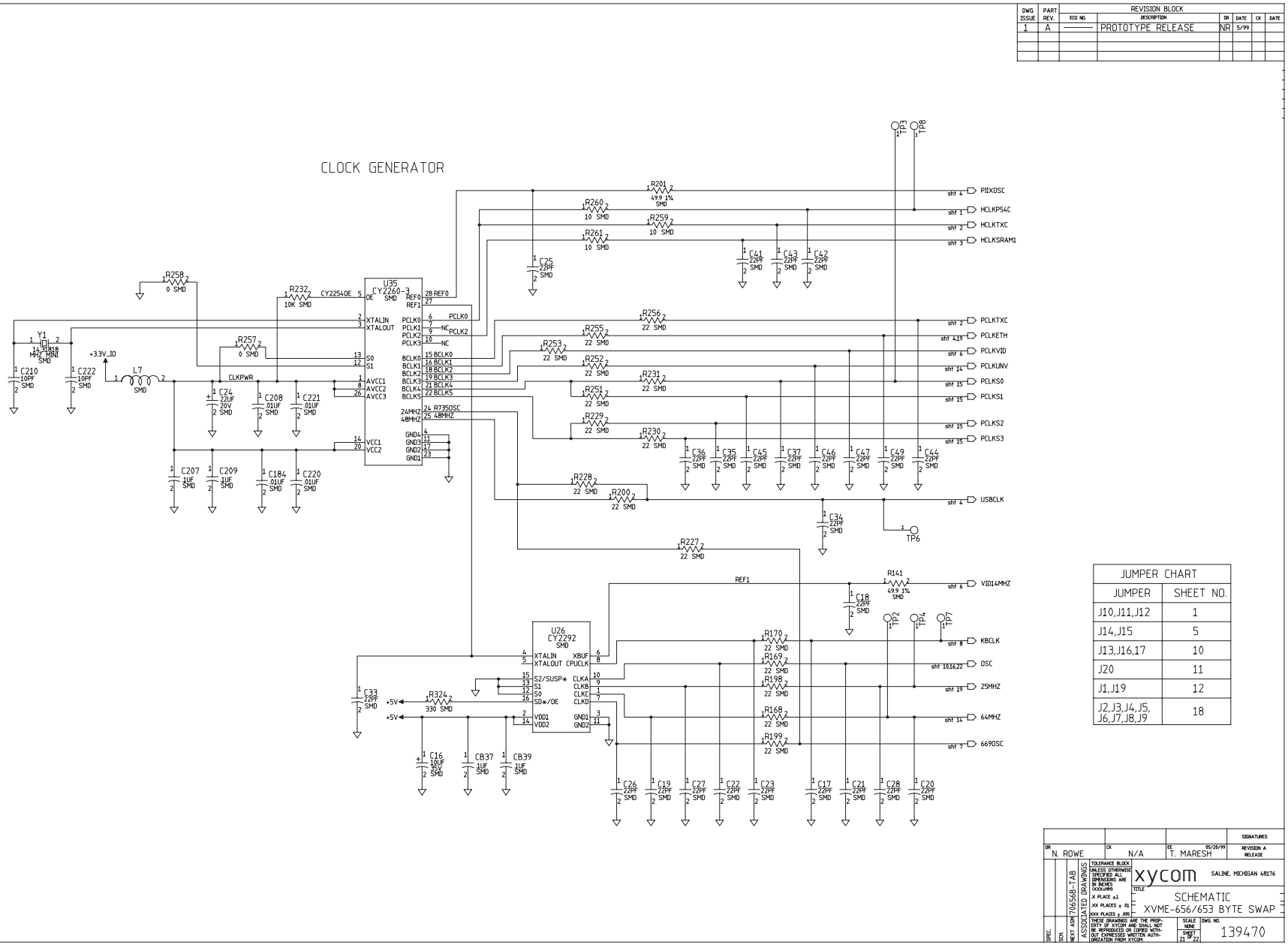
TITLE: SCHEMATIC XVME-656/653 BYTE SWAP

SCALE NONE | DWG. NO. 139470 | SHEET 20 OF 22

TOLERANCE BLOCK UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
DECIMALS
X PLACE ±1
XX PLACES ± .01
XXX PLACES ± .005

NEXT ASSY 706588-TAB ASSOCIATED DRAWINGS

DES. DEC.



DWG. ISSUE	PART REV.	ECO NO.	DESCRIPTION	DR	DATE	CK	DATE
1	A	———	PROTOTYPE RELEASE	NR	5/99		

REVISION BLOCK

JUMPER CHART	
JUMPER	SHEET NO.
J10,J11,J12	1
J14,J15	5
J13,J16,17	10
J20	11
J1,J19	12
J2,J3,J4,J5, J6,J7,J8,J9	18

			SIGNATURES
DR N. ROWE	CK N/A	EE 05/28/99 T. MARESH	REVISION A RELEASE

NEXT ASSY 706568-TAB
ASSOCIATED DRAWINGS
CHK
DES
SPEC

TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
DECIMALS
X PLACE ±.1
XX PLACES ± .01
XXX PLACES ± .005

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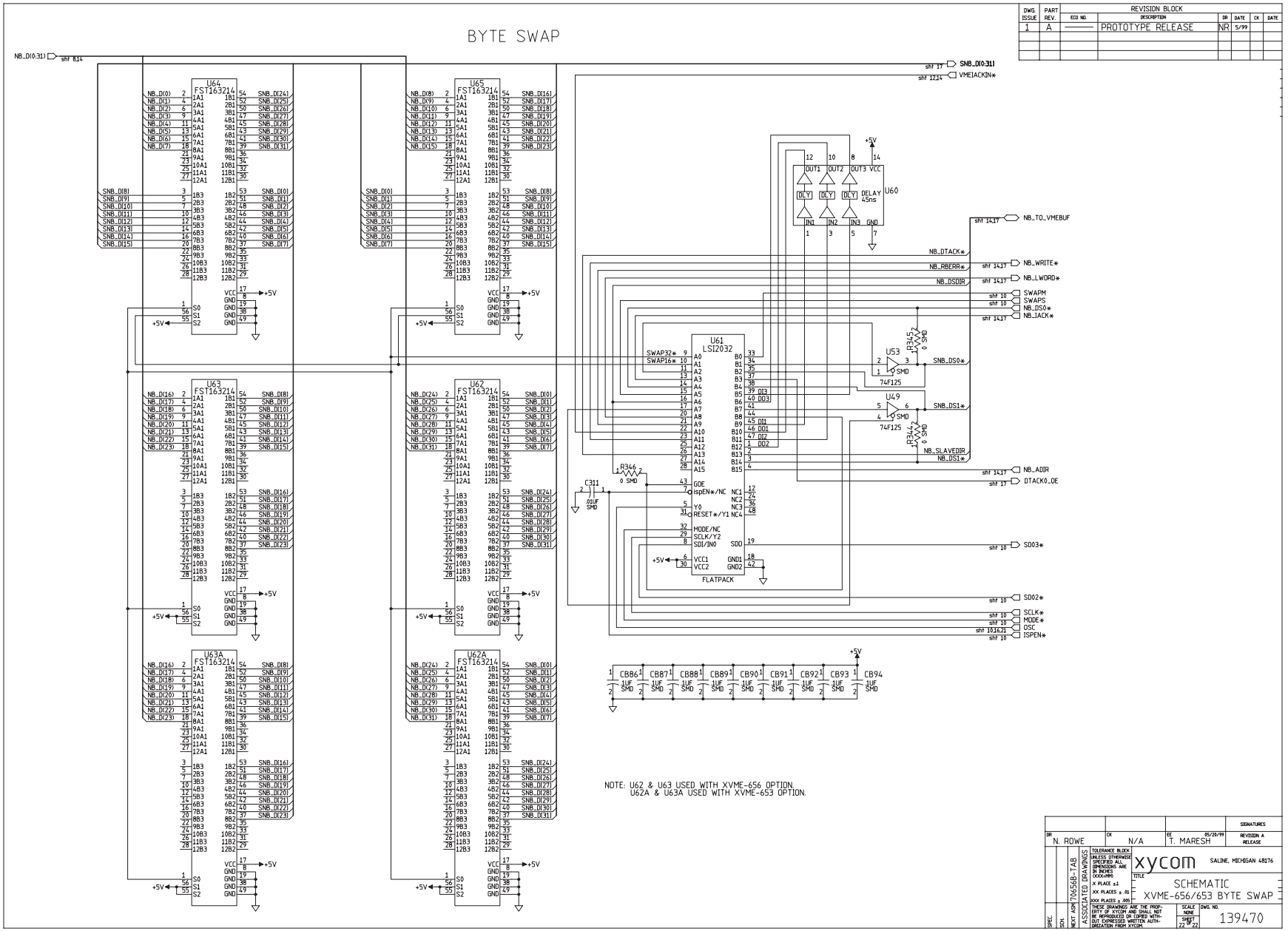
TITLE
SCHEMATIC
XVME-656/653 BYTE SWAP

SCALE NONE
SHEET 21 22
DWG. NO. 139470

BYTE SWAP



DWG. ISSUE	PART REV.	ECO NO.	DESCRIPTION	DR	DATE	CK	DATE
1	A	———	PROTOTYPE RELEASE	NR	5/99		

DR	CK	ENG	SIGNATURES
N. ROWE	N/A	T. MARESH 05/28/99	REVISION A RELEASE

TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
DECIMALS
X PLACE ±.1
XX PLACES ± .01
XXX PLACES ± .005

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