

Daylily Design Review

February 28, 1986

|                     |                           |                       |                                 |                           |                 |                        |                    |
|---------------------|---------------------------|-----------------------|---------------------------------|---------------------------|-----------------|------------------------|--------------------|
| <b>XEROX</b><br>SDD | <i>Project</i><br>DayLily | Daylily Design Review | <i>File</i><br>DaylilyDR01.silx | <i>Designer</i><br>Colvin | <i>Rev</i><br>A | <i>Date</i><br>2/28/86 | <i>Page</i><br>01x |
|---------------------|---------------------------|-----------------------|---------------------------------|---------------------------|-----------------|------------------------|--------------------|

**Functional Overview**

**Enhanced Graphics Adaptor Emulation**

**Block Diagram**

**System Timing**

**Memory & IO Maps**

**Logic**

## Functional Overview

Daylily provides two major functions

- Runs Mesa software
- Emulates an IBM Enhanced Graphics Adaptor

Uses existing AT peripherals  
excluding keyboard and display

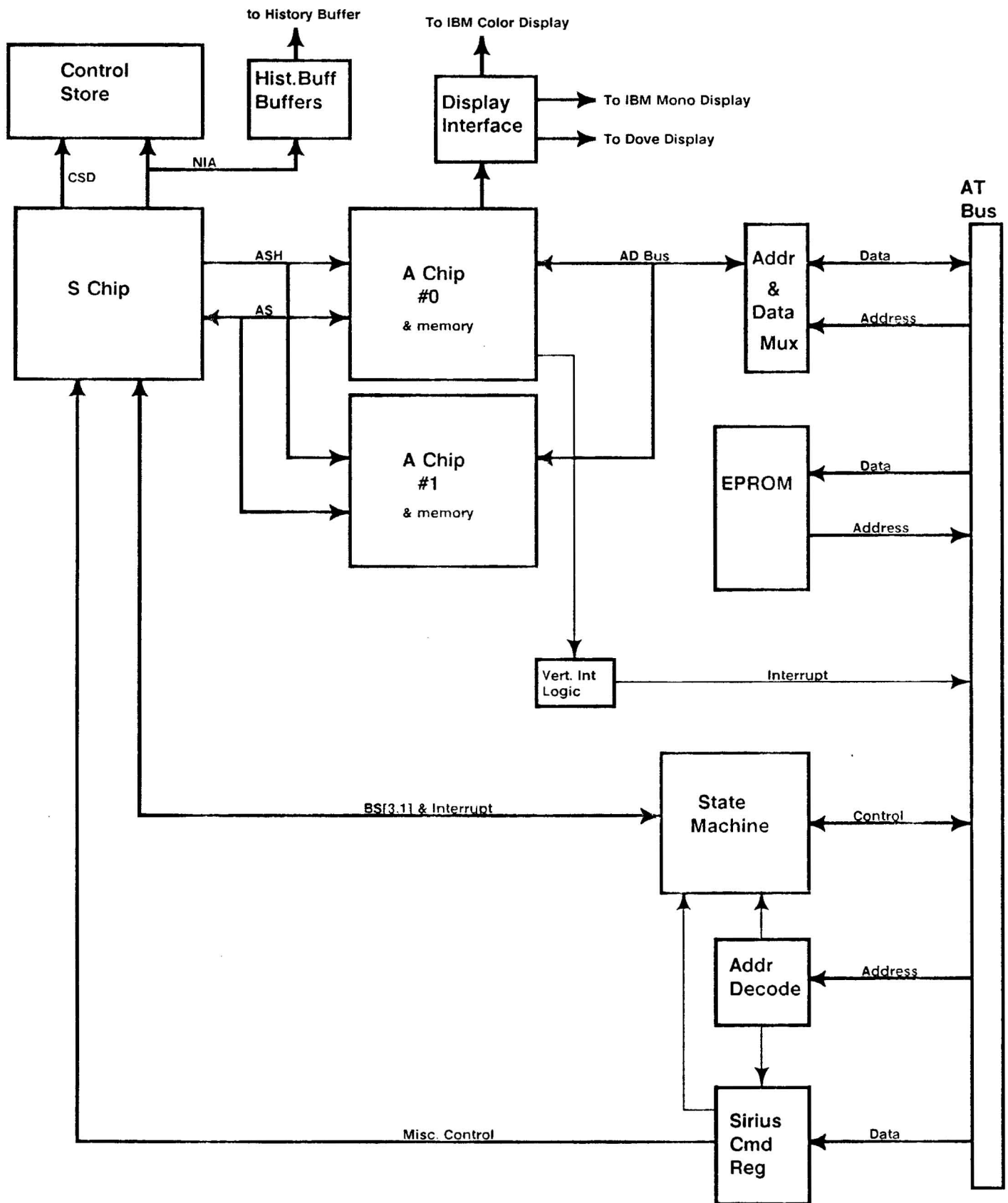
## Enhanced Graphics Adaptor Emulation

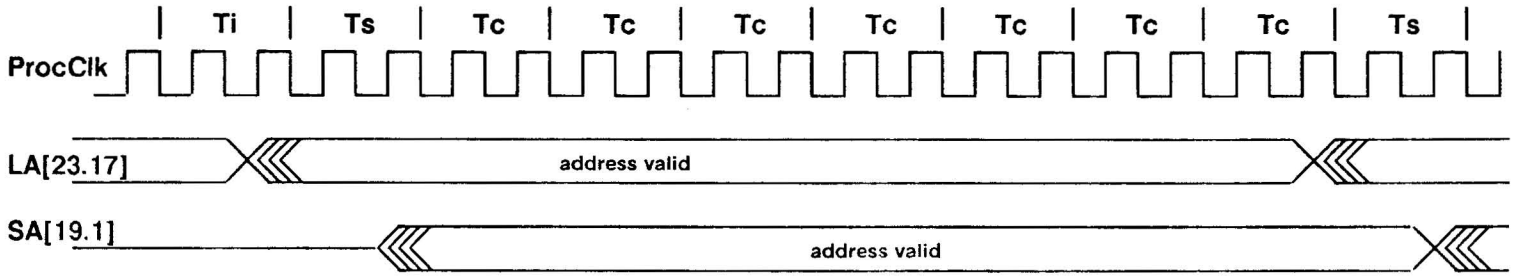
Daylily is hardware compatible with EGA

- Will respond to all EGA IO and memory addresses
  - Color Graphics Adaptor addresses
  - Monochrome Adaptor addresses
- Generates Vertical Interrupt

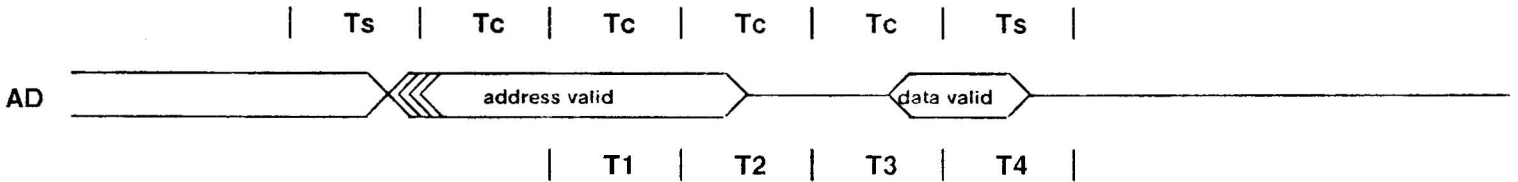
Daylily will support all EGA modes of operation

- 40 x 25 Text
- 80 x 25 Text
- 320 x 200 Graphics
- 640 x 200 Graphics
- 640 x 350 Graphics

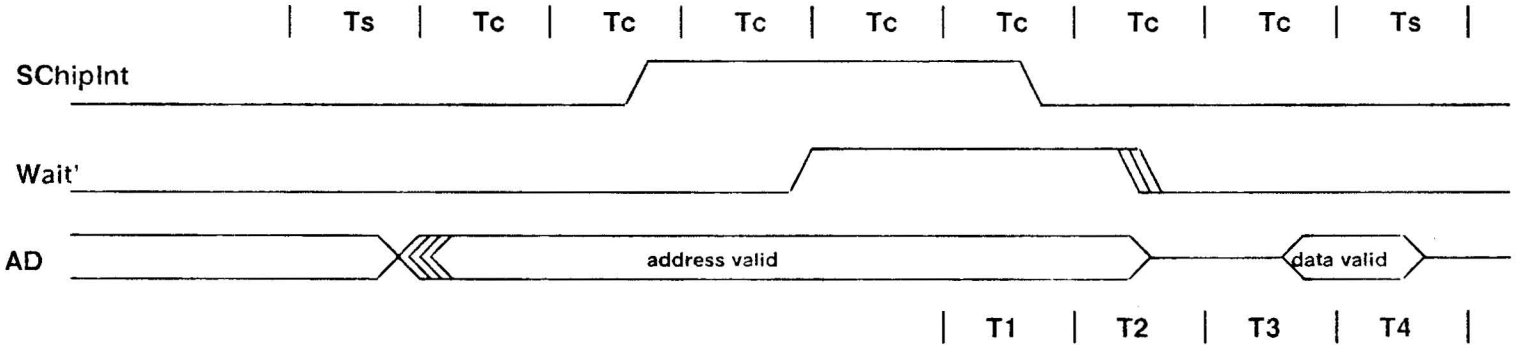




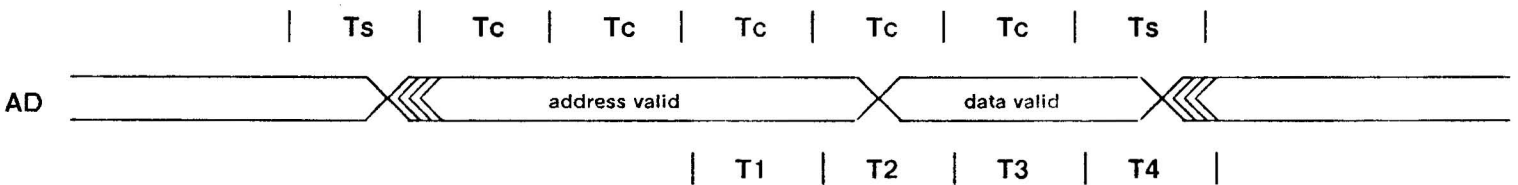
### Reads from AChip Addresses



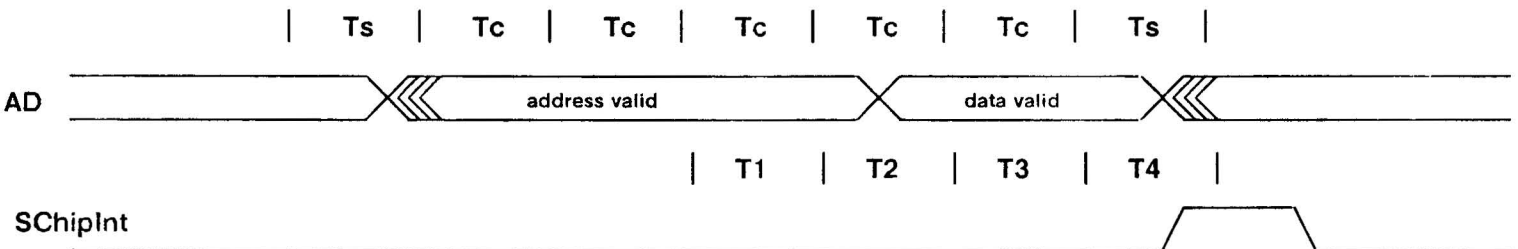
### Reads from EGA Addresses

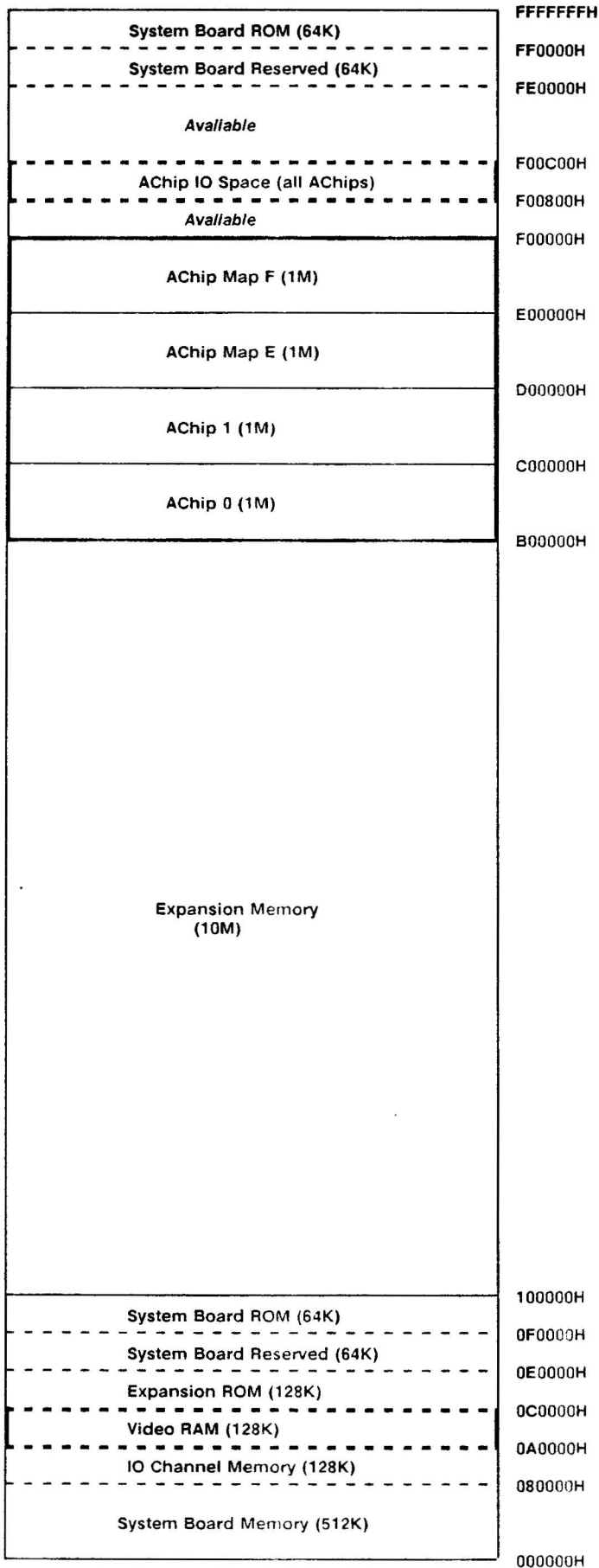


### Writes to AChip Addresses



### Writes to EGA Addresses





This is the memory map for an IBM AT with the Daylily board installed. The two AChip in italics(2 &3) are mapped but not necessarily installed. The AChip IO registers are memory mapped in the area above F00000H as shown. Below are the address range for each AChip IO space.

|               |                   |
|---------------|-------------------|
| <i>AChip0</i> | F00800H - F008FFH |
| <i>AChip1</i> | F00900H - F009FFH |
| <i>AChip2</i> | F00A00H - F00AFFH |
| <i>AChip3</i> | F00B00H - F00BFFH |

The Map E for the AChip is also mapped into the video RAM area at 0A0000H - 0C0000H, to allow emulation of the IBM graphics adaptor cards.

Bold lines represent Daylily memory addresses

## I/O Address Map for IBM AT

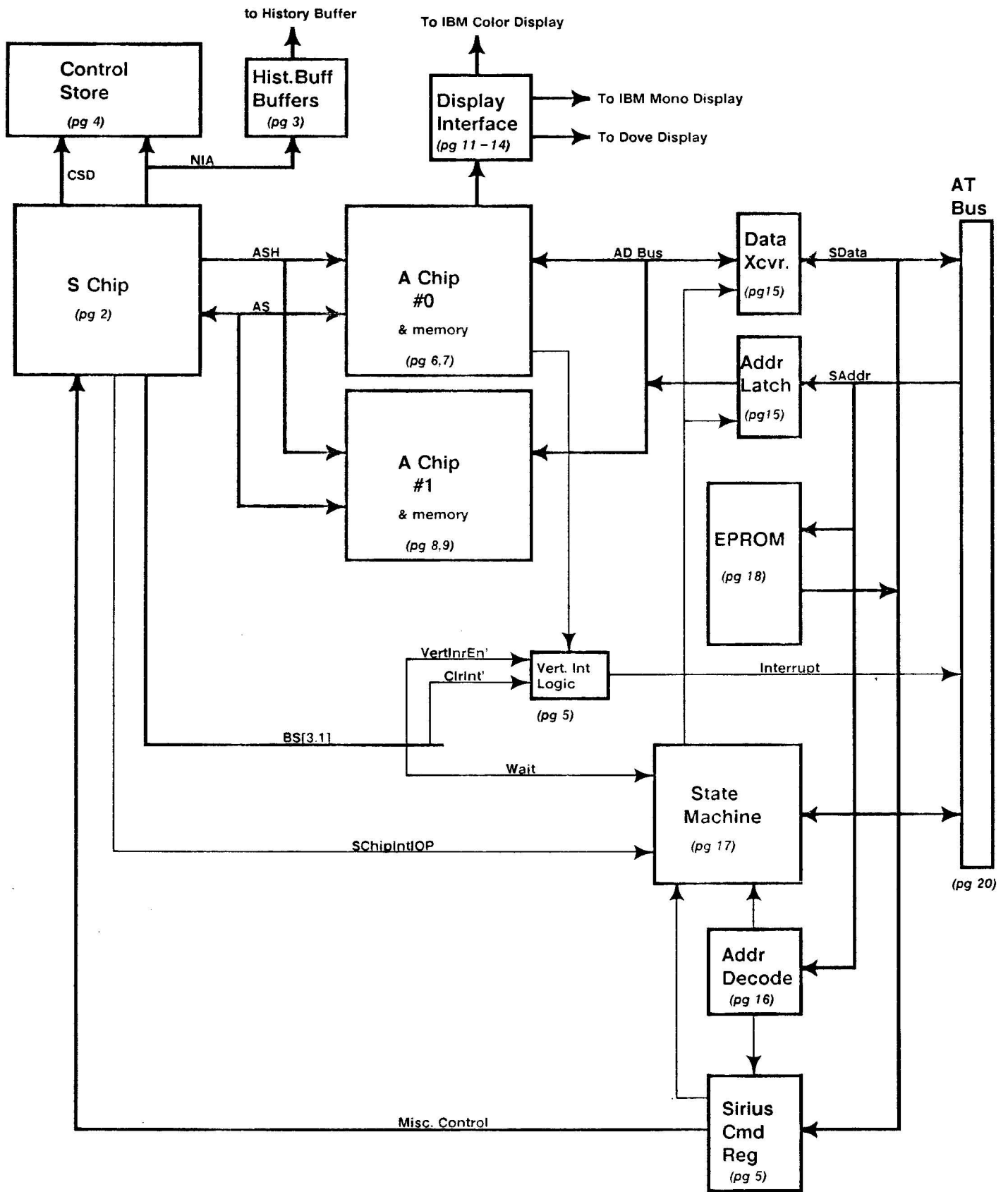
| <u>Hex Addr</u> |            | <u>Hex Addr</u> |                         | <u>Hex Addr</u> |   |
|-----------------|------------|-----------------|-------------------------|-----------------|---|
| 100 - 107       |            | 200 - 207       | Game IO                 | 300 - 307       | Prototype Card                          |
| 108 - 10F       |            | 208 - 20F       |                         | 308 - 30F       | Prototype Card                          |
| 110 - 117       |            | 210 - 217       | <u>SChipReq?</u>        | 310 - 317       | Prototype Card                          |
| 118 - 11F       |            | 218 - 21F       |                         | 318 - 31F       | Prototype Card                          |
| 120 - 127       |            | 220 - 227       | <u>SChipReq?</u>        | 320 - 327       |   |
| 128 - 12F       |            | 228 - 22F       |                         | 328 - 32F       |   |
| 130 - 137       |            | 230 - 237       | <u>SChipReq?</u>        | 330 - 337       | <u>SChipReq?</u>                        |
| 138 - 13F       |            | 238 - 23F       |                         | 338 - 33F       |   |
| 140 - 147       |            | 240 - 247       |                         | 340 - 347       |   |
| 148 - 14F       |            | 248 - 24F       |                         | 348 - 34F       |   |
| 150 - 157       |            | 250 - 257       |                         | 350 - 357       |   |
| 158 - 15F       |            | 258 - 25F       |                         | 358 - 35F       |   |
| 160 - 167       |            | 260 - 267       |                         | 360 - 367       | Network Adaptr                          |
| 168 - 16F       |            | 268 - 26F       |                         | 368 - 36F       | Network Adaptr                          |
| 170 - 177       |            | 270 - 277       |                         | 370 - 377       |   |
| 178 - 17F       |            | 278 - 27F       | Parallel Printer Port 2 | 378 - 37F       | Parallel Printer Port 1                 |
| 180 - 187       |            | 280 - 287       |                         | 380 - 387       | SDLC, bisynchronous 2                   |
| 188 - 18F       |            | 288 - 28F       |                         | 388 - 38F       | SDLC, bisynchronous 2                   |
| 190 - 197       |            | 290 - 297       |                         | 390 - 397       |   |
| 198 - 19F       |            | 298 - 29F       |                         | 398 - 39F       |   |
| 1A0 - 1A7       |            | 2A0 - 2A7       |                         | 3A0 - 3A7       | Bisynchronous 1                         |
| 1A8 - 1AF       |            | 2A8 - 2AF       |                         | 3A8 - 3AF       | Bisynchronous 1                         |
| 1B0 - 1B7       |            | 2B0 - 2B7       |                         | 3B0 - 3B7       | <u>Mono Display &amp; Printer Adptr</u> |
| 1B8 - 1BF       |            | 2B8 - 2BF       |                         | 3B8 - 3BF       | <u>Mono Display &amp; Printer Adptr</u> |
| 1C0 - 1C7       |            | 2C0 - 2C7       |                         | 3C0 - 3C7       | <u>Extended Graphics Adptr</u>          |
| 1C8 - 1CF       |            | 2C8 - 2CF       |                         | 3C8 - 3CF       | <u>Extended Graphics Adptr</u>          |
| 1D0 - 1D7       |            | 2D0 - 2D7       |                         | 3D0 - 3D7       | <u>Color/Graphics Monitor Adptr</u>     |
| 1D8 - 1DF       |            | 2D8 - 2DF       |                         | 3D8 - 3DF       | <u>Color/Graphics Monitor Adptr</u>     |
| 1E0 - 1E7       |            | 2E0 - 2E7       | GPIB & Data Acquisition | 3E0 - 3E7       |   |
| 1E8 - 1EF       |            | 2E8 - 2EF       |                         | 3E8 - 3EF       |   |
| 1F0 - 1F7       | Fixed Disk | 2F0 - 2F7       |                         | 3F0 - 3F7       | Diskette Controller                     |
| 1F8 - 1FF       | Fixed Disk | 2F8 - 2FF       | Serial Port 2           | 3F8 - 3FF       | Serial Port 1                           |

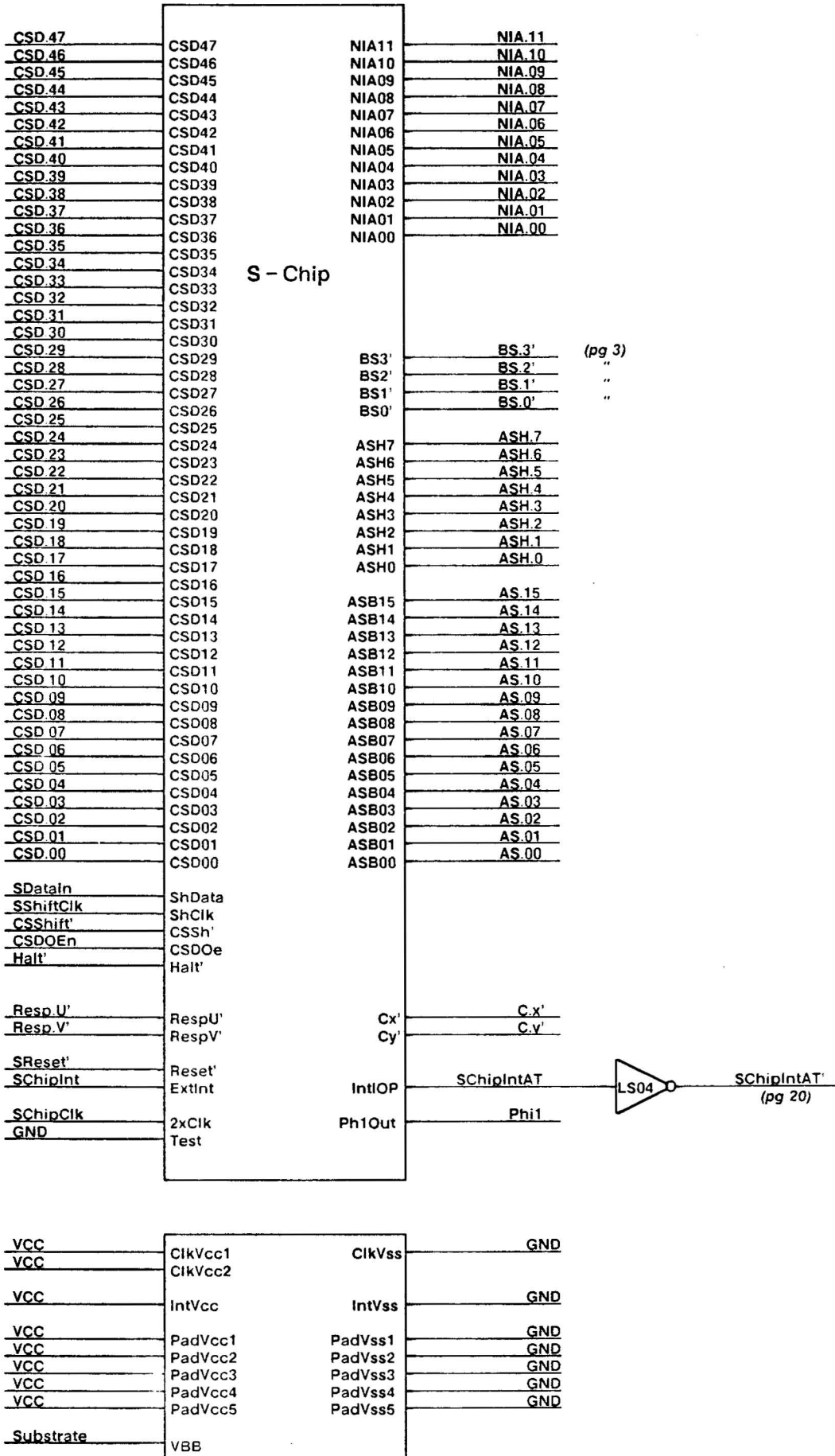
Daylily board responds to all underlined entries



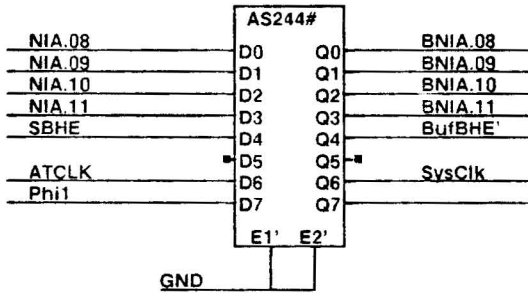
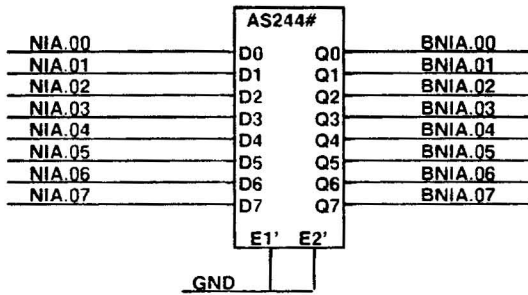
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| 03              | Control Store Address Bus,<br>History Buffer Connector     |
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| 05              | Sirius Output Register,<br>Vertical Interrupt, SChip Clock |
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| 07              | A - Chip.0 RAM   |
| 08              | A - Chip.1   |
| 09              | A - Chip.1 RAM   |
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| 11              | Monochrome Video Interface                                 |
| 12              | Dove Display Drivers                                       |
| 13              | IBM Display Drivers &<br>Connectors                        |
| 14              | Dove Display Connector,<br>AChip Substrate Bias            |
| 15              | AT Address and Data Bus<br>Interface                       |
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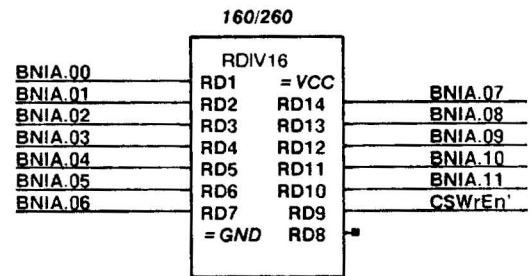




## Control Store Address Buffers

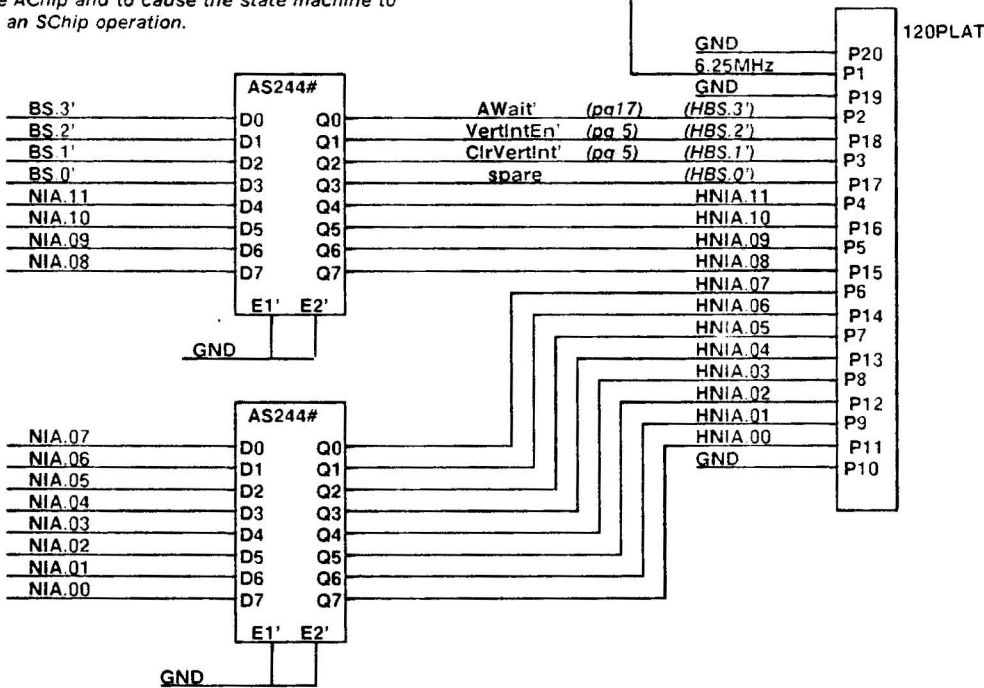


## Bus Terminator



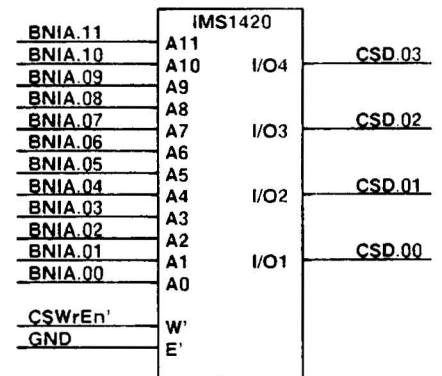
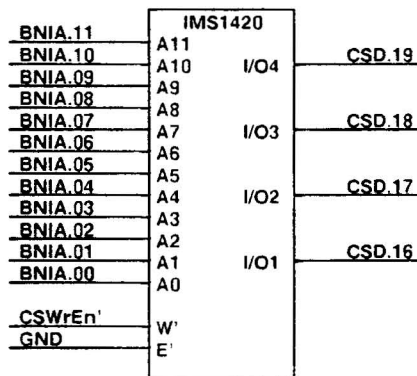
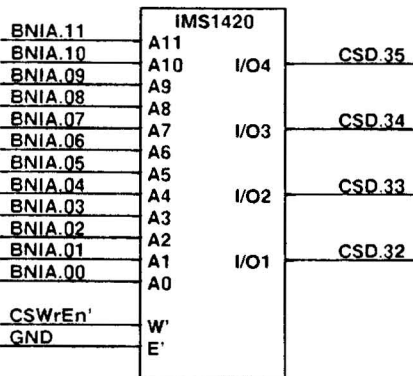
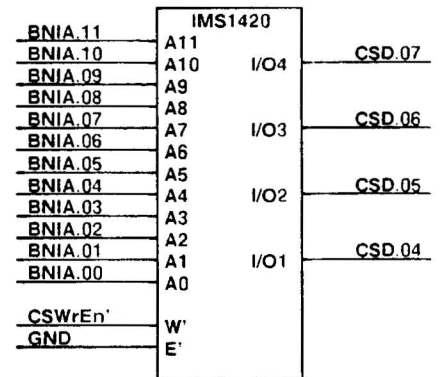
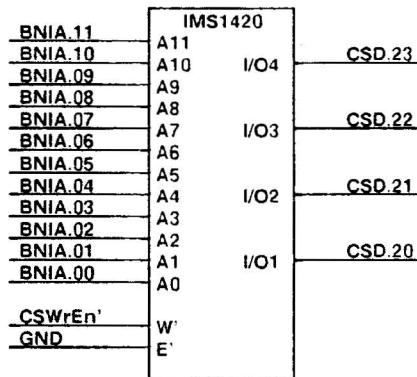
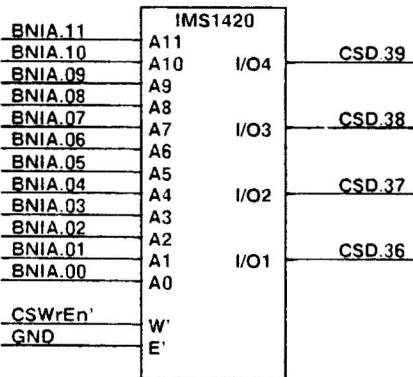
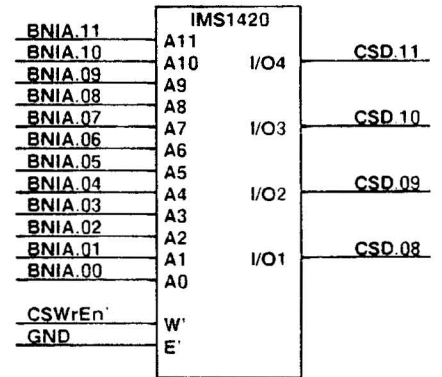
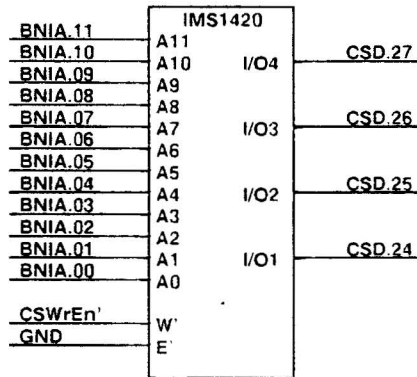
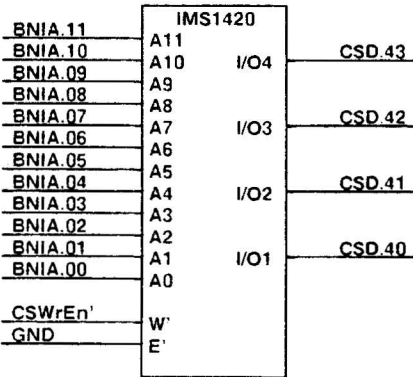
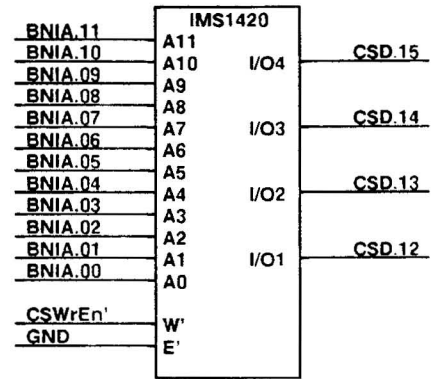
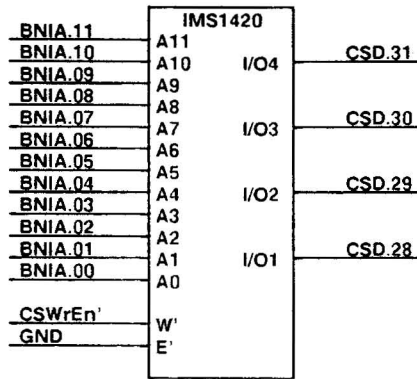
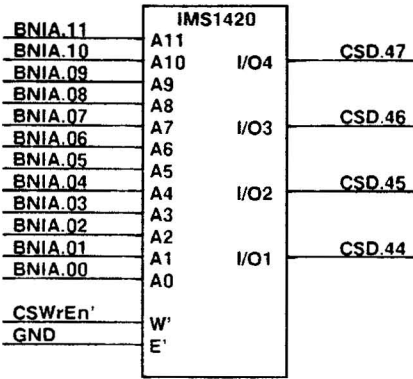
The upper three bank select lines on the SChip are buffered and used to control the vertical interrupt from the AChip and to cause the state machine to wait for an SChip operation.

## History Buffer Connector

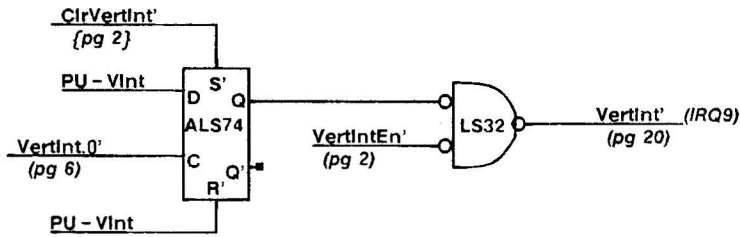


Font 4 macros:

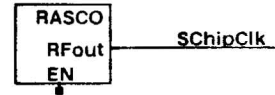
- 1 = AS244#
- 2 = I20PLAT
- 3 = RASCO



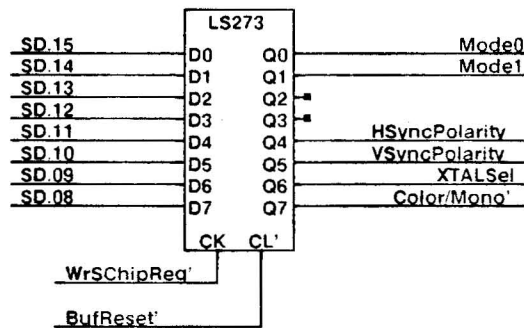
## Vertical Interrupt Logic



## Sirius Clock

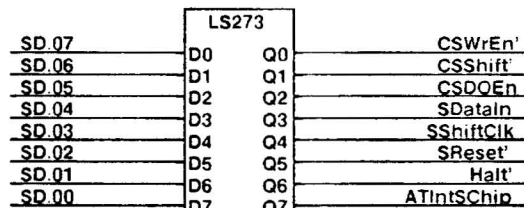


## Sirius Command Register

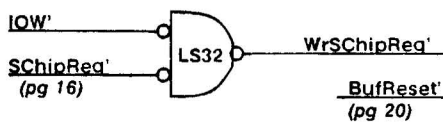


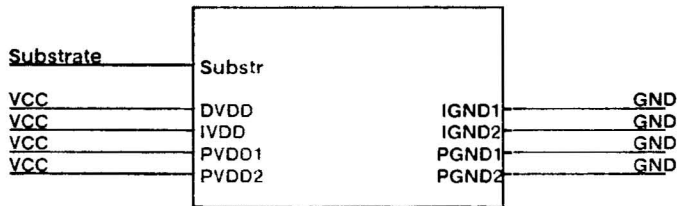
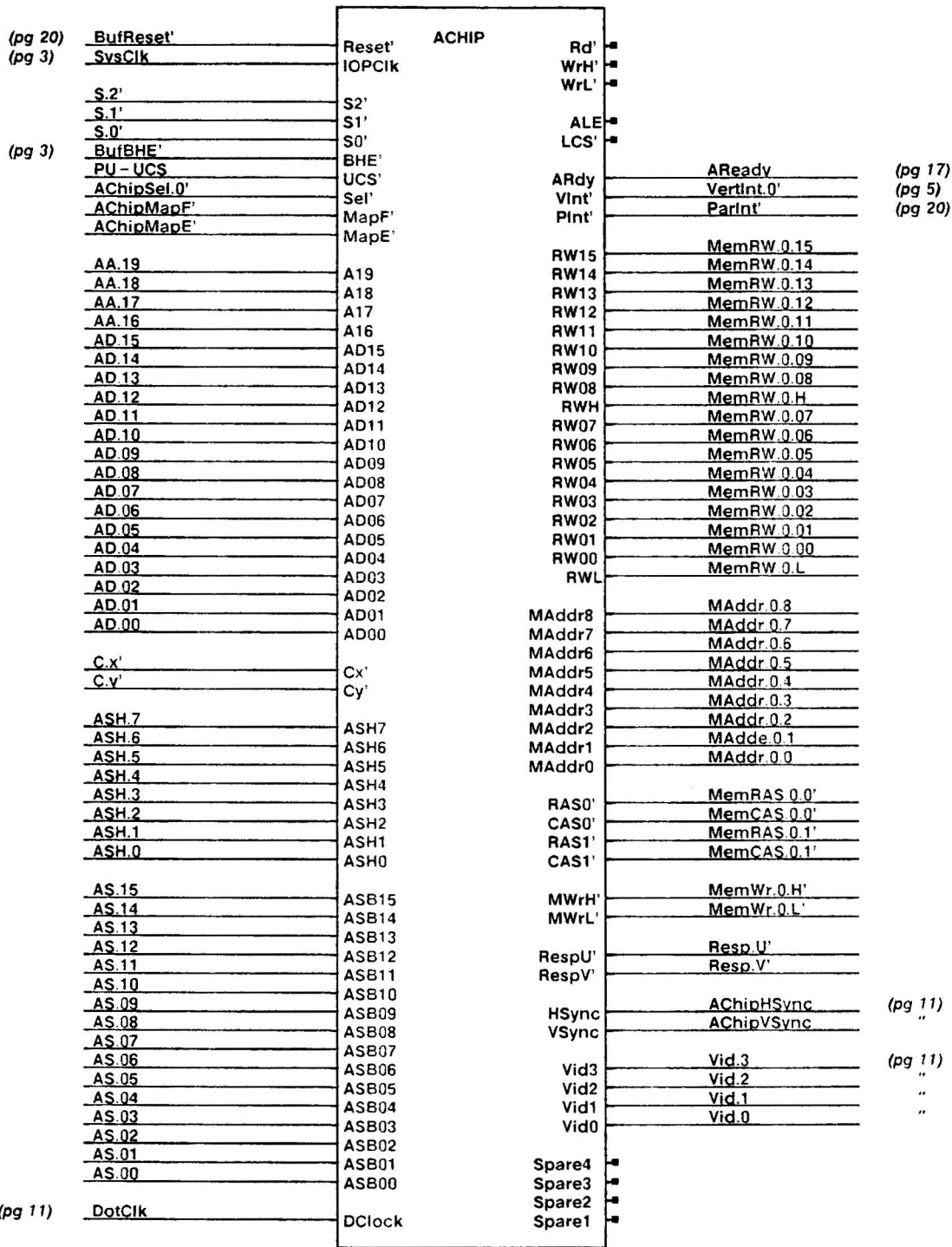
The two mode lines are used to select the desired display mode, when emulating an IBM Enhanced Graphics Adaptor. (pg 16)

(pg 11)  
"  
"  
"



(pg 2)  
"  
"  
"  
"  
"  
"  
"  
(pg 17)





Add 0.1uF CAPs between corresponding Vcc and GND.

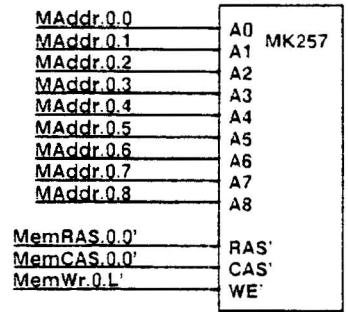
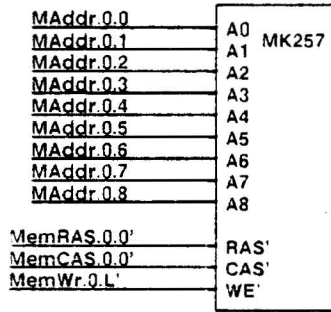
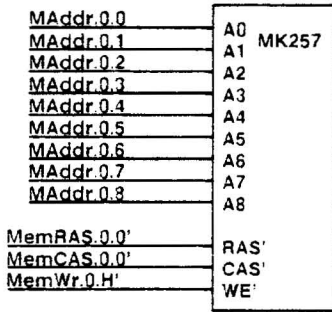
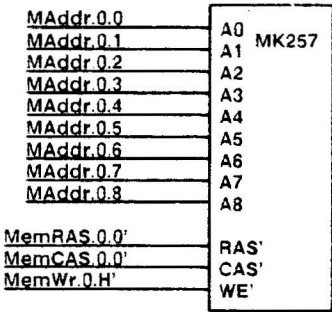
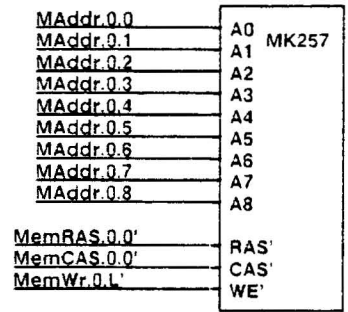
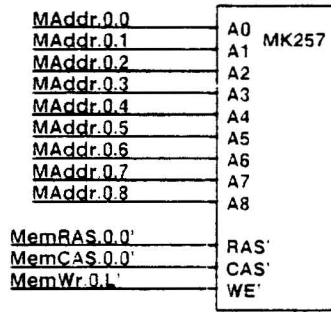
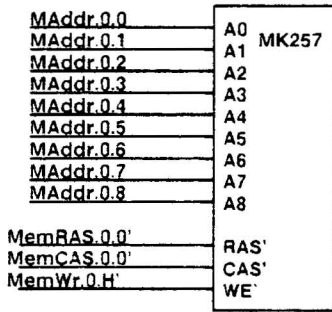
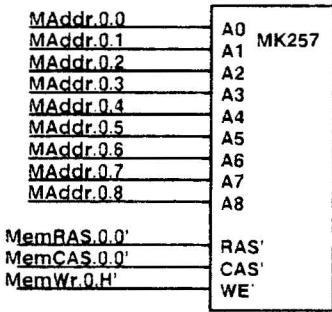
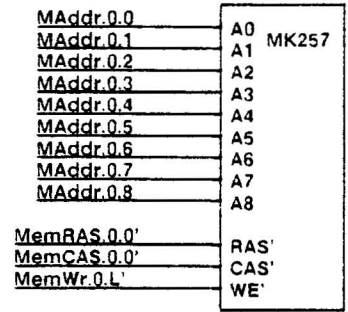
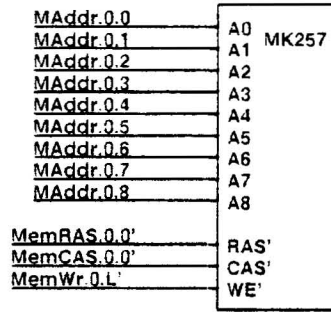
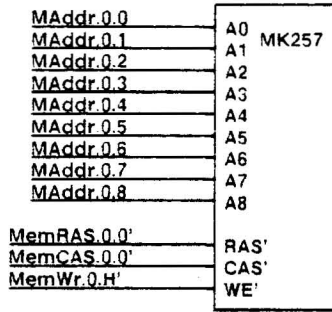
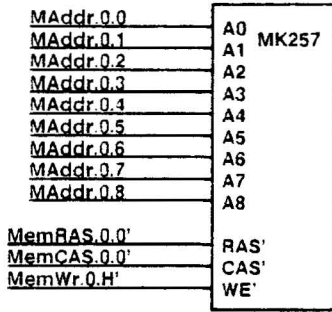
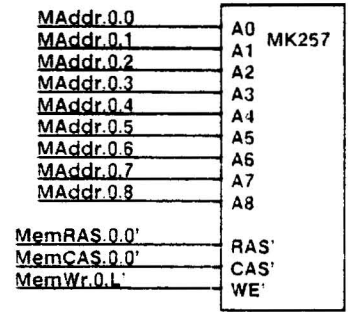
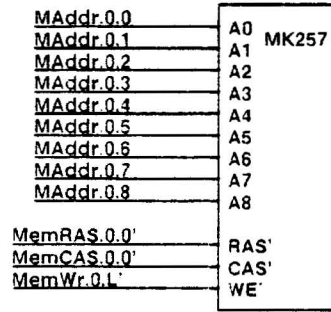
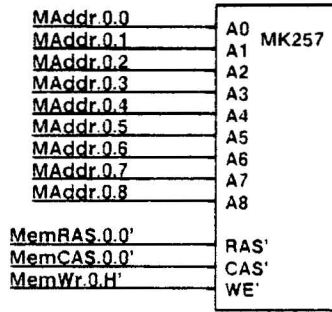
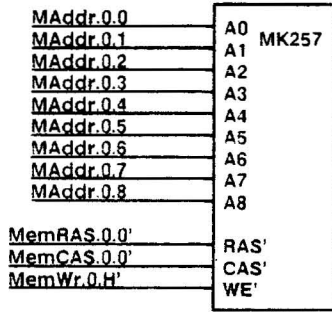
Font 4 macros:

1 = AChip  
2 = Power

|              |                    |         |                       |                    |          |                 |            |
|--------------|--------------------|---------|-----------------------|--------------------|----------|-----------------|------------|
| XEROX<br>SDD | Project<br>DayLily | AChip.0 | File<br>Daylily06.sil | Designer<br>Colvin | Rev<br>A | Date<br>2/26/86 | Page<br>06 |
|--------------|--------------------|---------|-----------------------|--------------------|----------|-----------------|------------|

### High Byte

### Low Byte



Memory addresses:

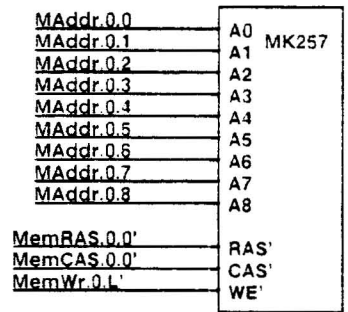
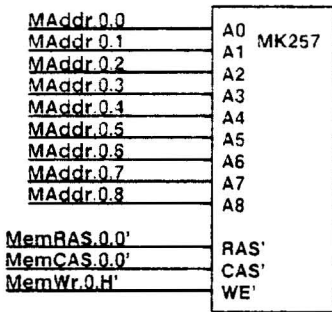
AddrL.0.0  
AddrL.0.1  
AddrL.0.2  
AddrL.0.4  
AddrL.0.5  
AddrL.0.7

may be arbitrarily assigned to aid in PWBA layout.

Memory addresses:

AddrL.0.3  
AddrL.0.6  
AddrL.0.8

**MUST NOT BE REASSIGNED!!**

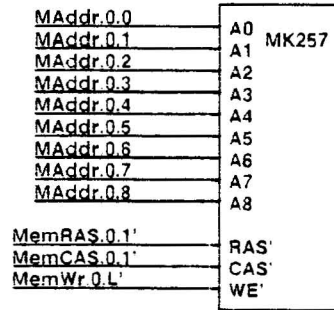
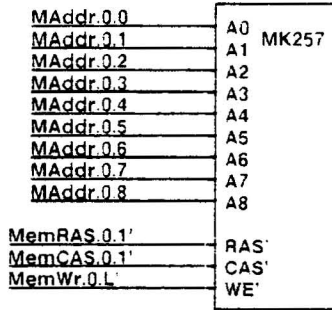
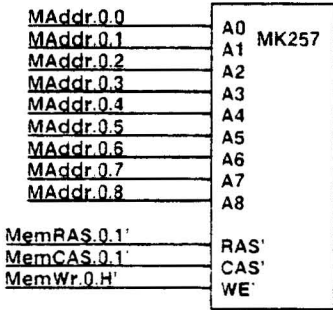
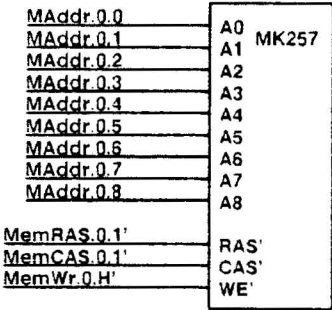
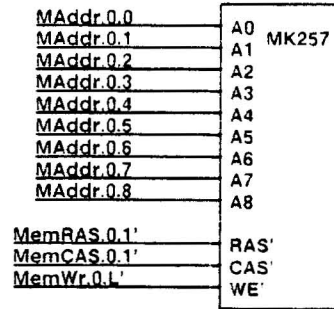
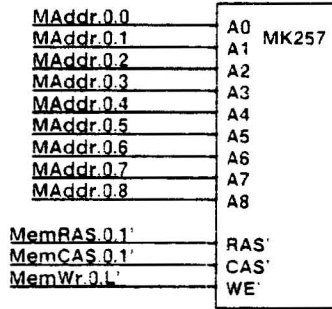
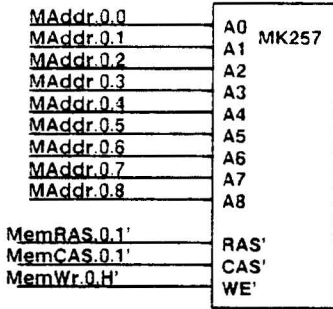
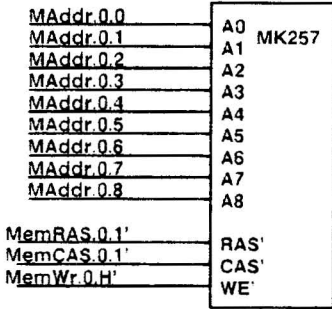
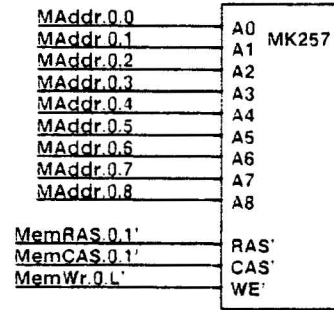
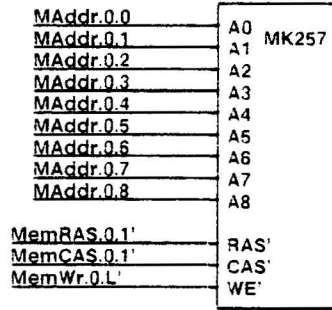
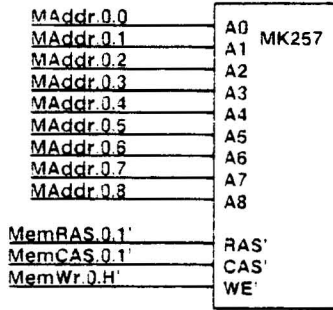
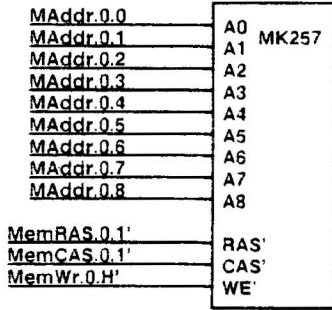
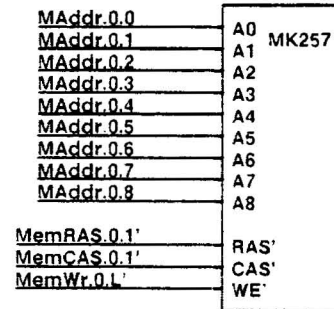
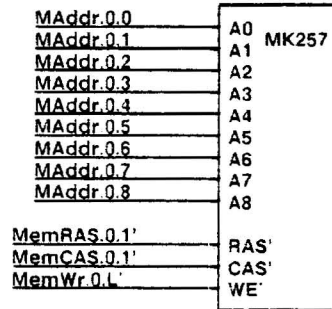
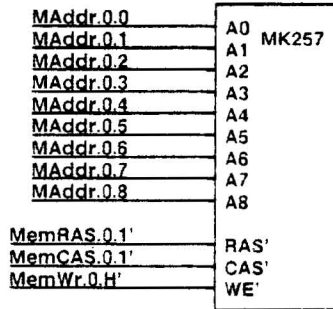
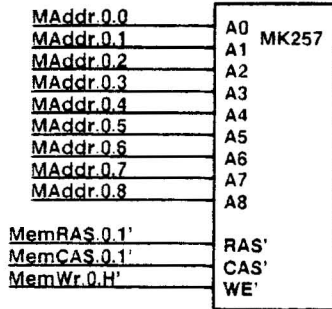


Font 4 macros:  
1 = MK257



## High Byte

## Low Byte



Memory addresses:

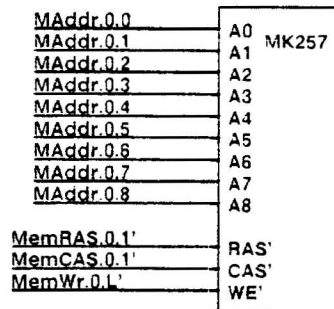
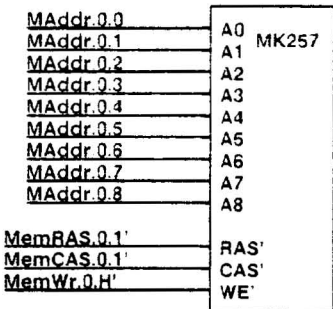
AddrL.0.0  
AddrL.0.1  
AddrL.0.2  
AddrL.0.4  
AddrL.0.5  
AddrL.0.7

may be arbitrarily assigned to aid in PWBA layout.

Memory addresses:

AddrL.0.3  
AddrL.0.6  
AddrL.0.8

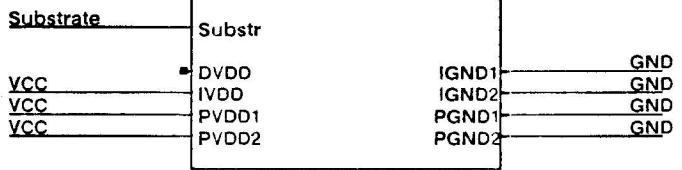
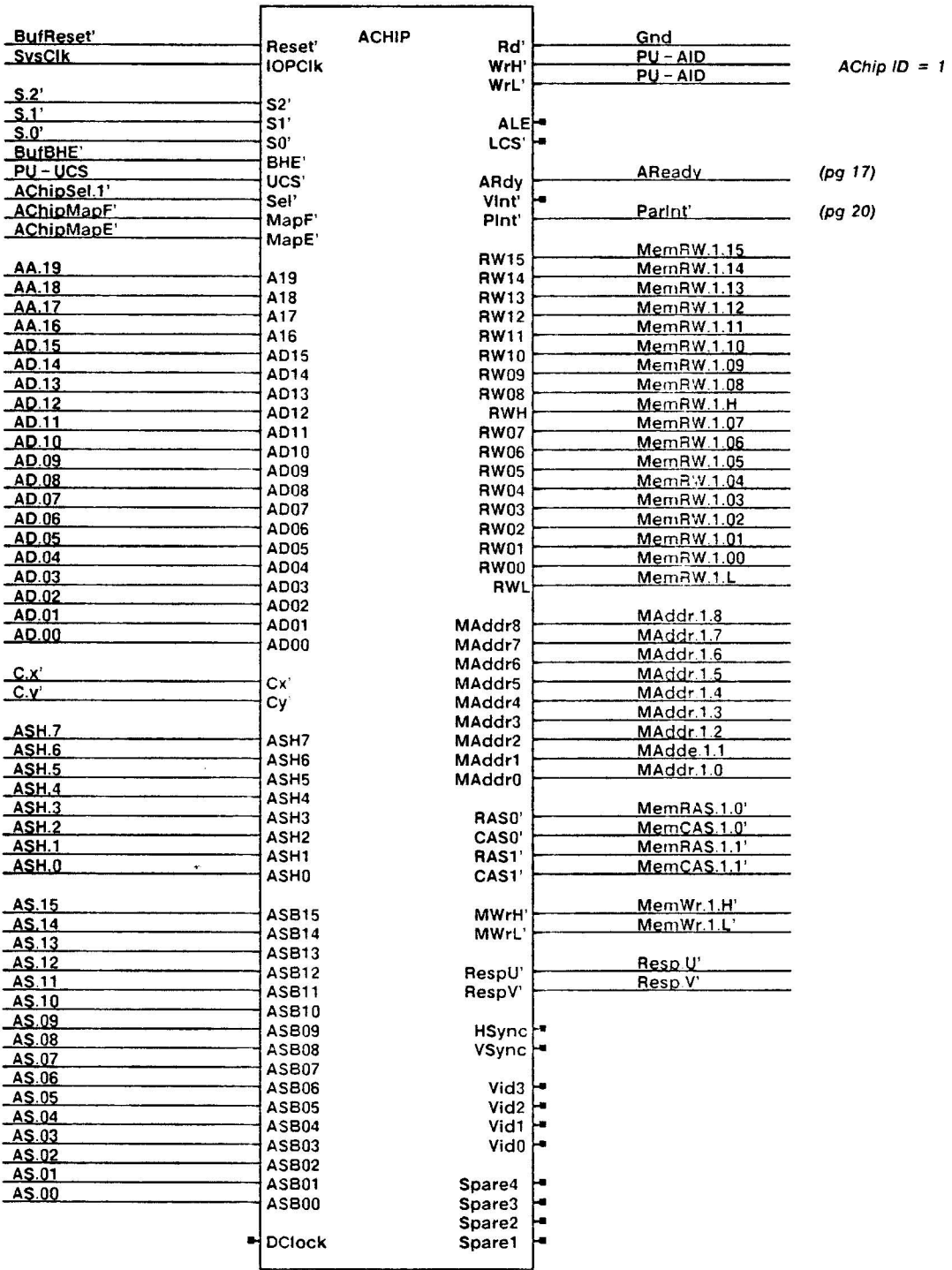
**MUST NOT BE REASSIGNED!!**



Font 4 macros:  
1 = MK257



(pg 20)  
(pg 3)



Do not want to power the display controller section of this AChip

Add 0.1uF CAPs between corresponding Vcc and GND.

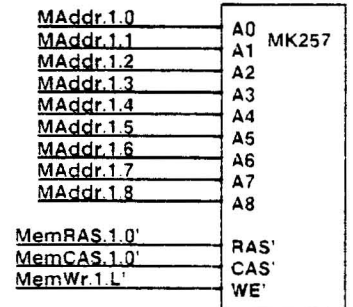
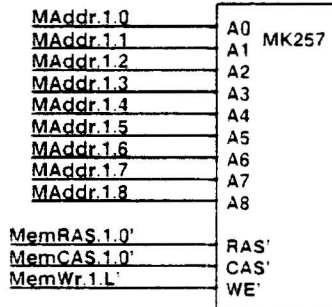
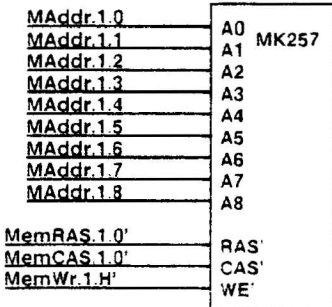
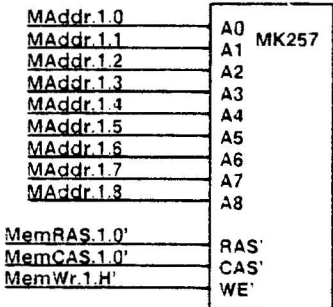
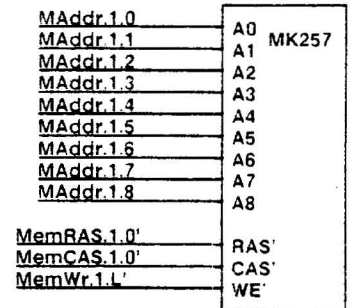
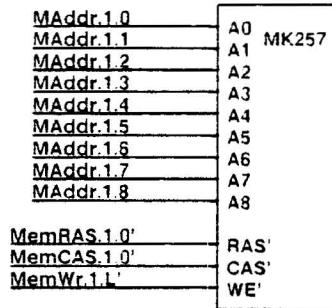
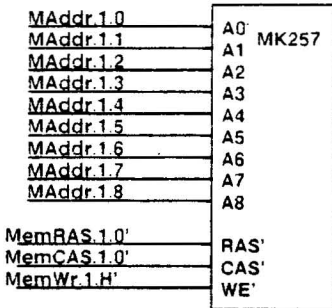
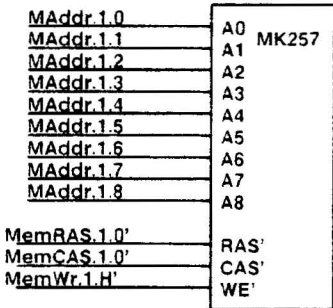
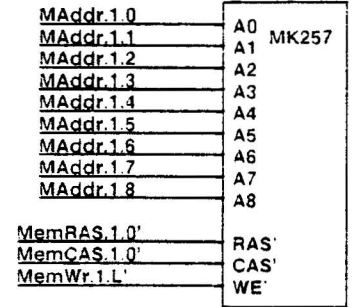
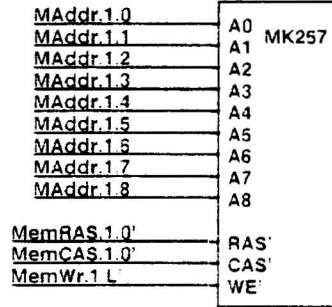
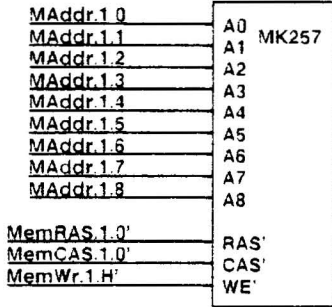
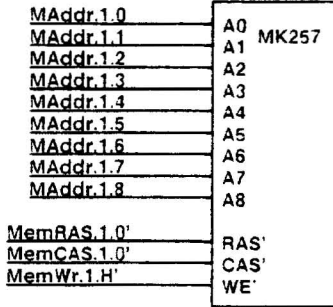
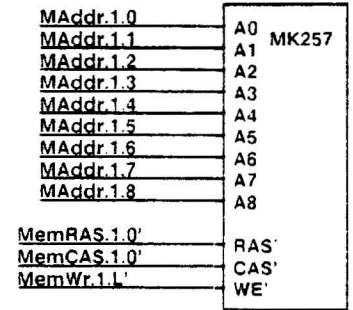
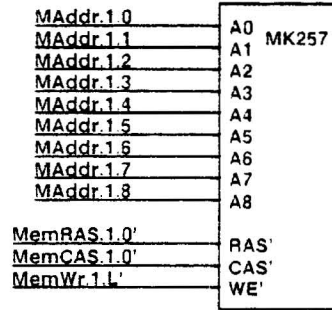
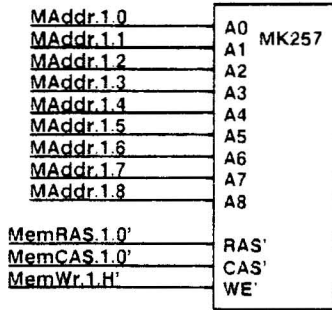
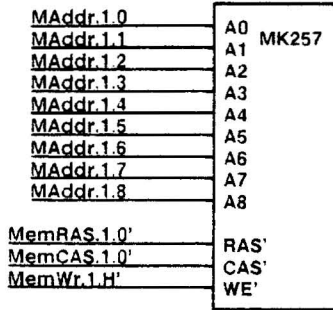
Font 4 macros.

1 = AChip  
2 = Power

|              |                    |         |                       |                    |          |                 |            |
|--------------|--------------------|---------|-----------------------|--------------------|----------|-----------------|------------|
| XEROX<br>SDD | Project<br>DayLily | AChip.1 | File<br>Daylily08.sil | Designer<br>Colvin | Rev<br>A | Date<br>2/26/86 | Page<br>08 |
|--------------|--------------------|---------|-----------------------|--------------------|----------|-----------------|------------|

## High Byte

## Low Byte



Memory addresses:

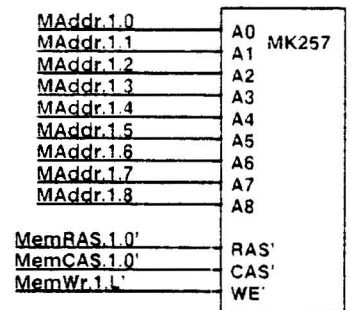
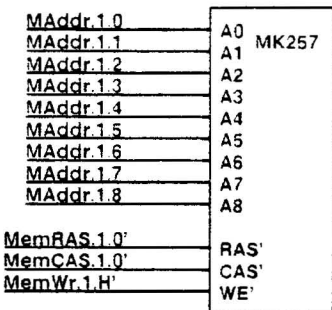
AddrL.0.0  
 AddrL.0.1  
 AddrL.0.2  
 AddrL.0.4  
 AddrL.0.5  
 AddrL.0.7

may be arbitrarily assigned to aid in PWBA layout.

Memory addresses:

AddrL.0.3  
 AddrL.0.6  
 AddrL.0.8

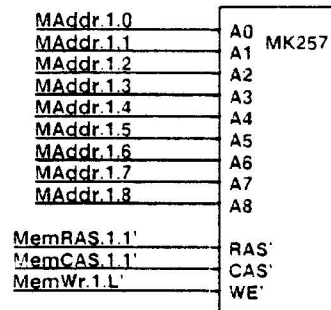
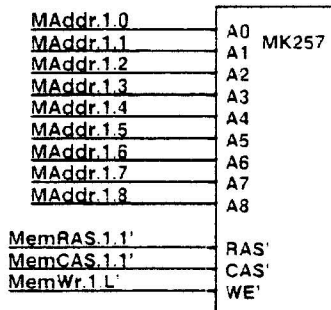
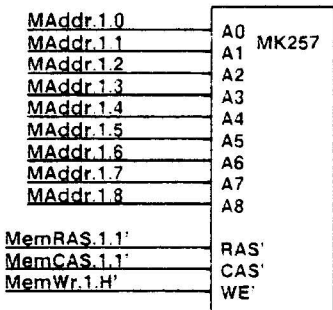
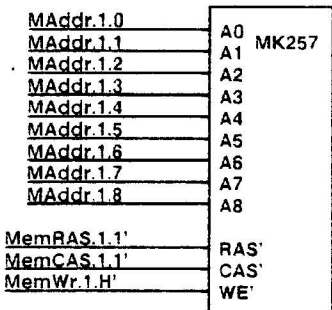
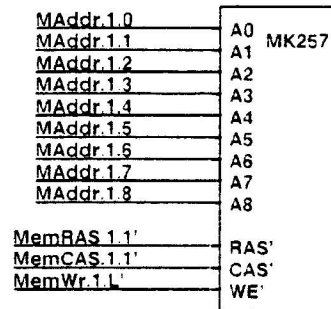
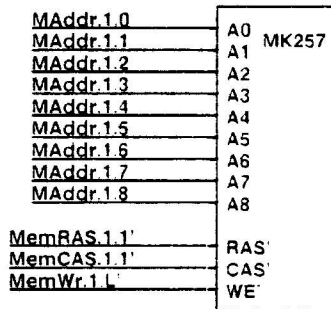
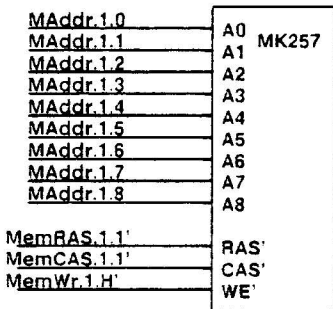
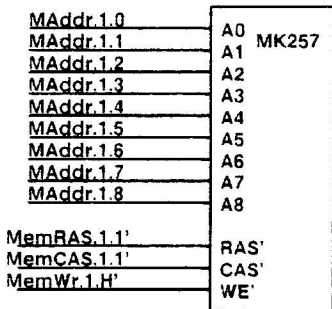
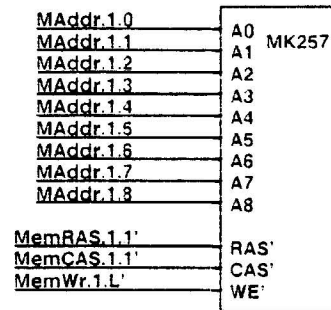
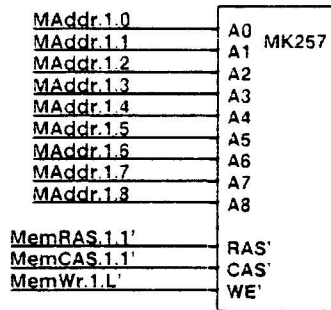
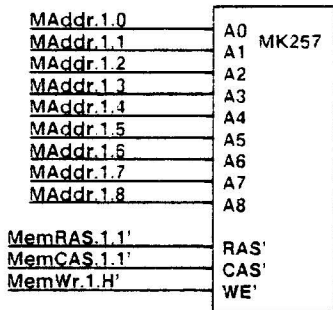
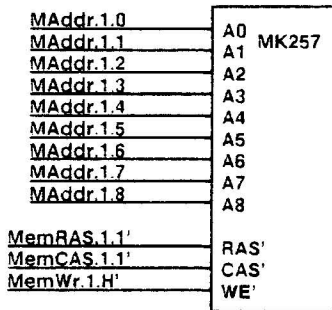
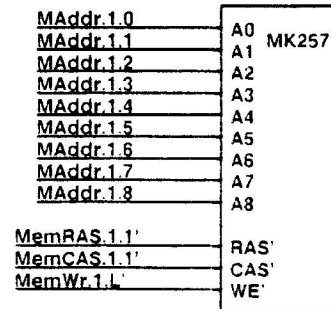
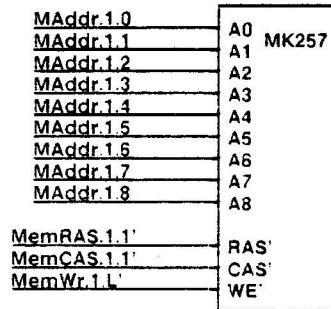
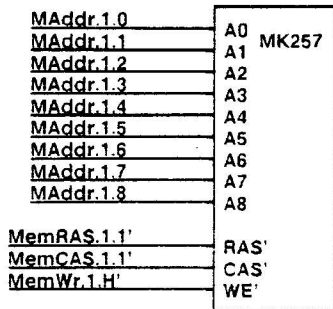
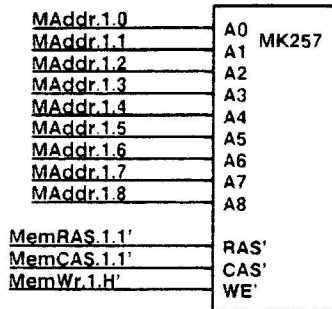
**MUST NOT BE REASSIGNED!!**



Font 4 macros:  
 1 = MK257

## High Byte

## Low Byte



Memory addresses:

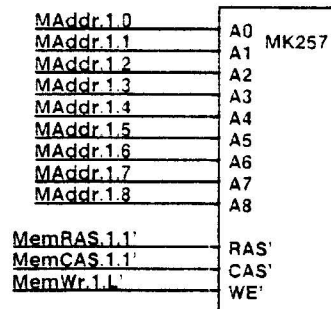
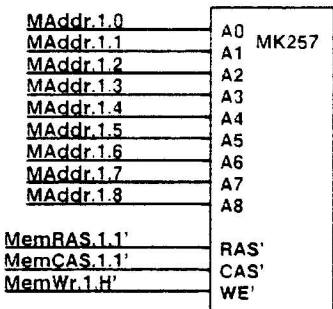
AddrL.0.0  
AddrL.0.1  
AddrL.0.2  
AddrL.0.4  
AddrL.0.5  
AddrL.0.7

may be arbitrarily assigned to aid in PWBA layout.

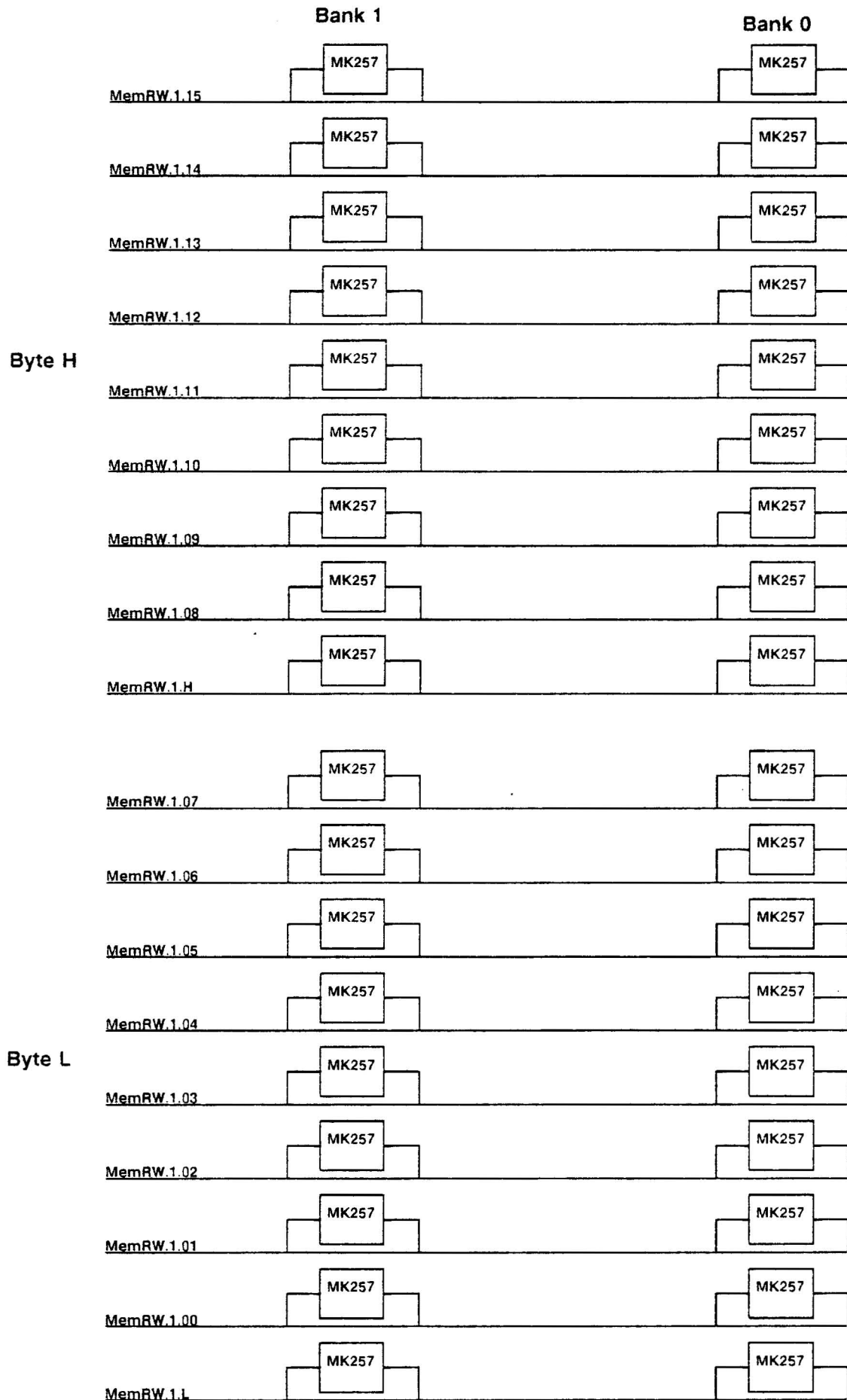
Memory addresses:

AddrL.0.3  
AddrL.0.6  
AddrL.0.8

**MUST NOT BE REASSIGNED!!**



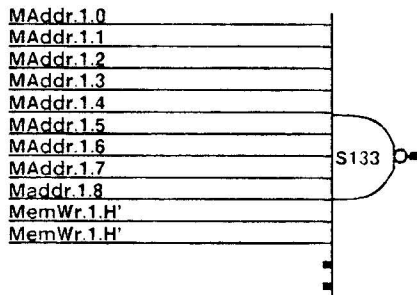
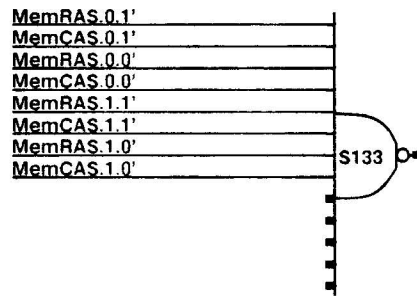
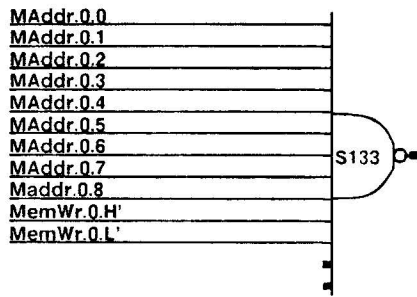
Font 4 macros:  
1 = MK257



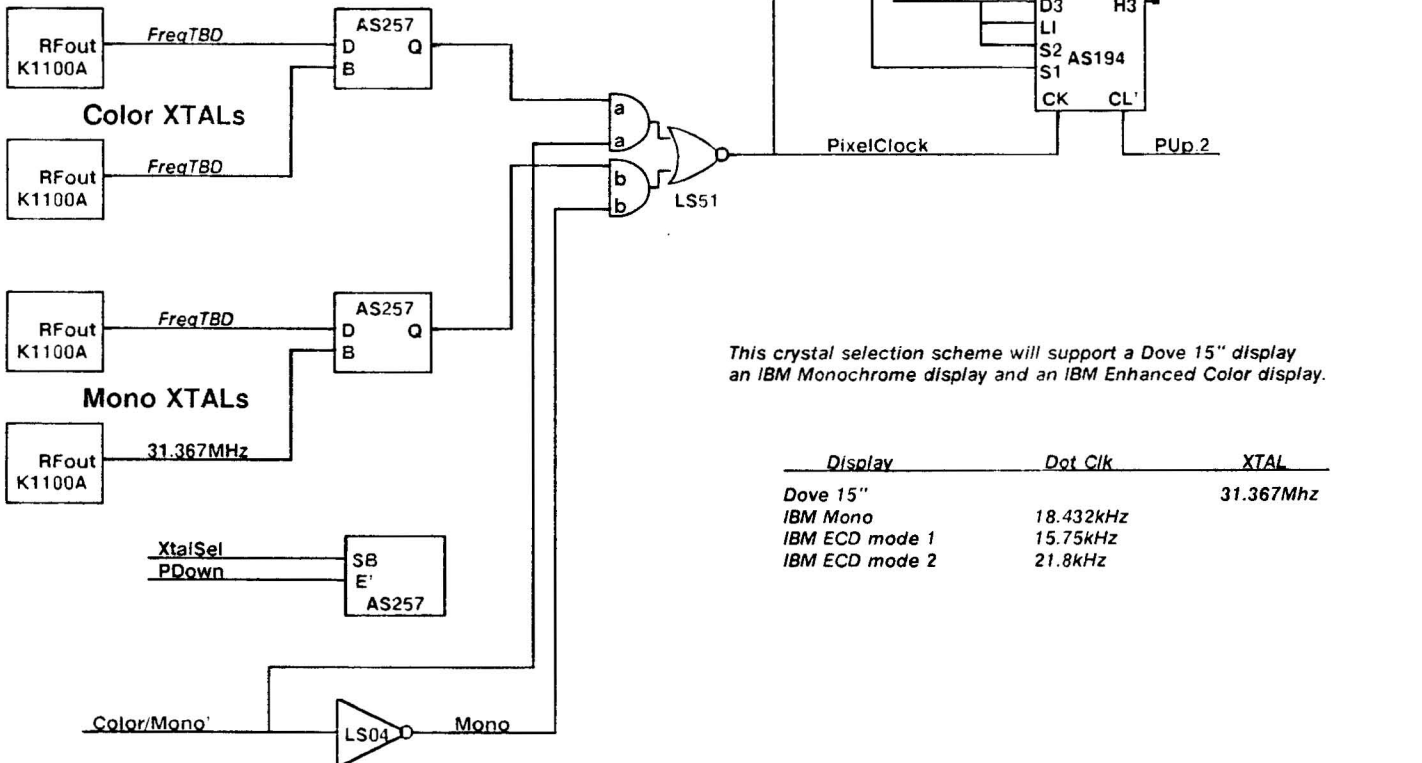
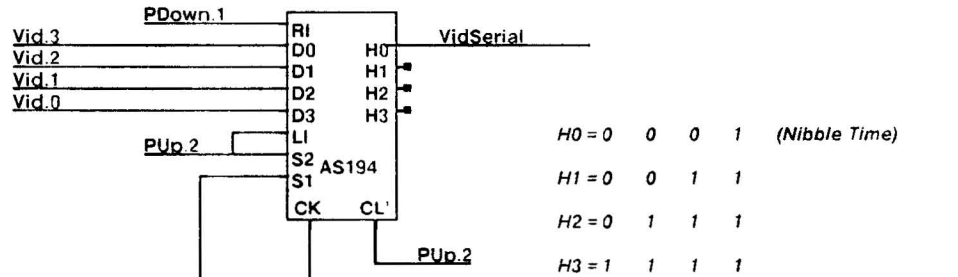
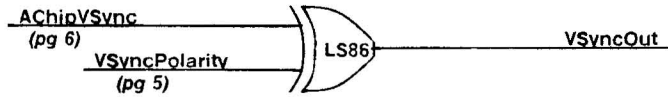
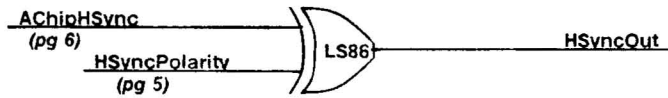
Font 4 macr

1 = MK257

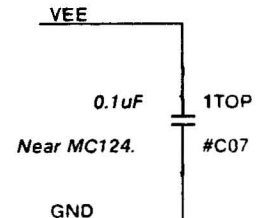
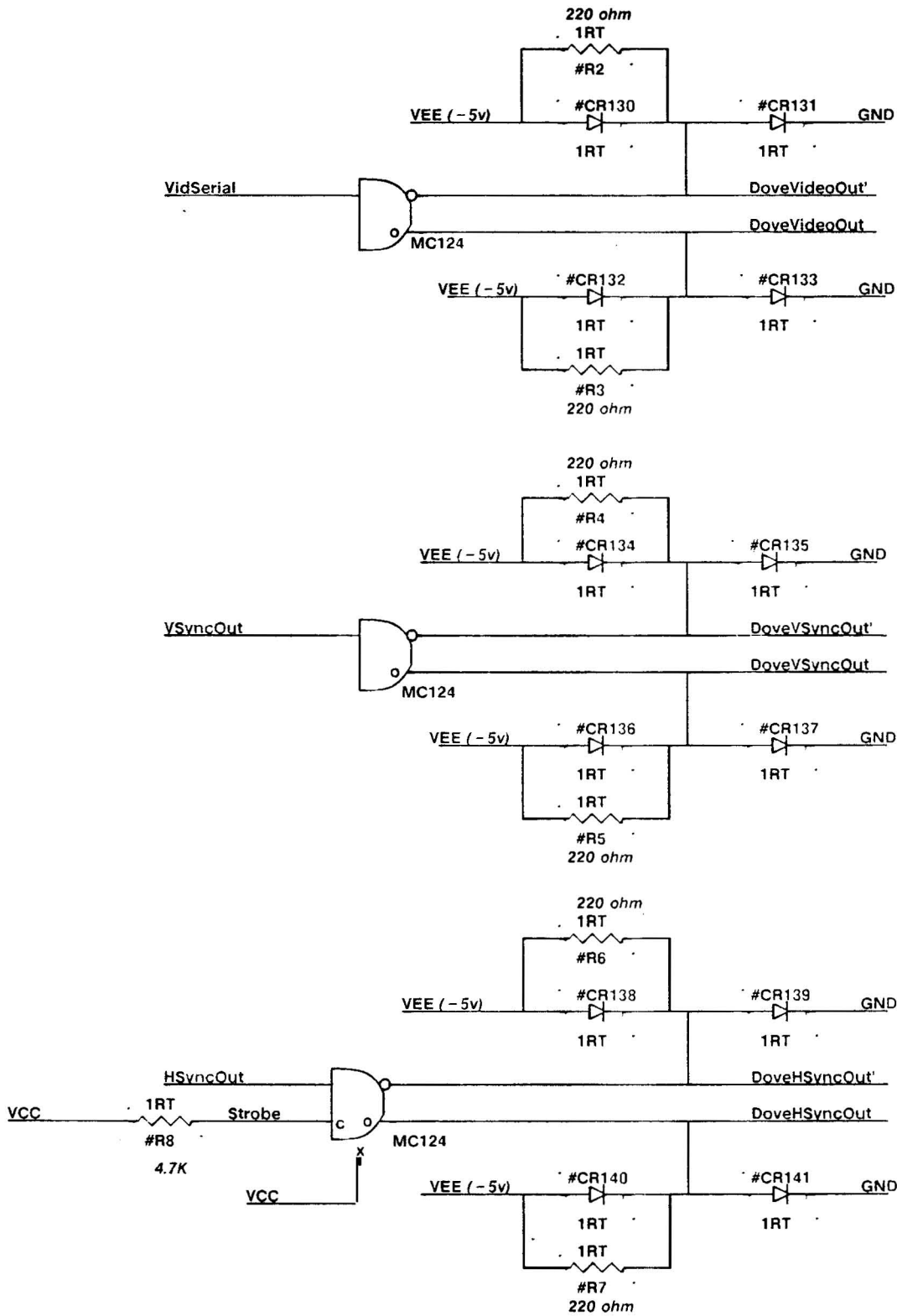
|                     |                    |                        |                        |                                |          |                 |             |
|---------------------|--------------------|------------------------|------------------------|--------------------------------|----------|-----------------|-------------|
| <b>XEROX</b><br>SDD | Project<br>DayLily | A - Chip.1 Memory Data | File<br>Daylily09c.sil | Designer<br>Camacho,<br>Colvin | Rev<br>A | Date<br>2/27/86 | Page<br>09c |
|---------------------|--------------------|------------------------|------------------------|--------------------------------|----------|-----------------|-------------|



*If this scheme does not work, HP1001 diodes will be tried as terminators. This will be done via platforms.*





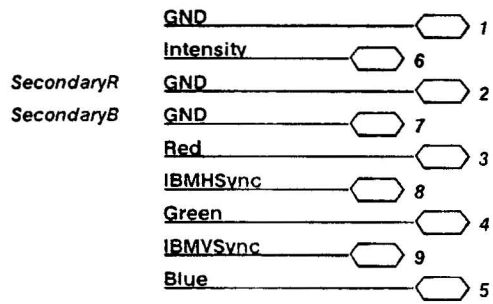


To prevent time varying return currents, the syncs are differential.  
Termination of ECL is also provided by the display monitor.

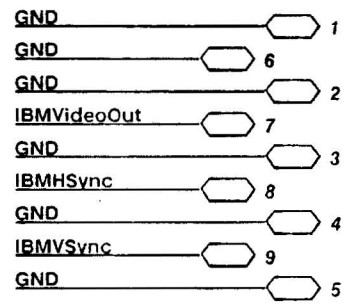
Diodes = SD103A

|                     |                    |                      |                       |  |          |                 |            |
|---------------------|--------------------|----------------------|-----------------------|--|----------|-----------------|------------|
| <b>XEROX</b><br>SDD | Project<br>Daylily | Dove Display Drivers | File<br>Daylily12.sil | Designer<br>Dillon, Colvin,<br>Camacho | Rev<br>A | Date<br>2/26/86 | Page<br>12 |
|---------------------|--------------------|----------------------|-----------------------|--|----------|-----------------|------------|

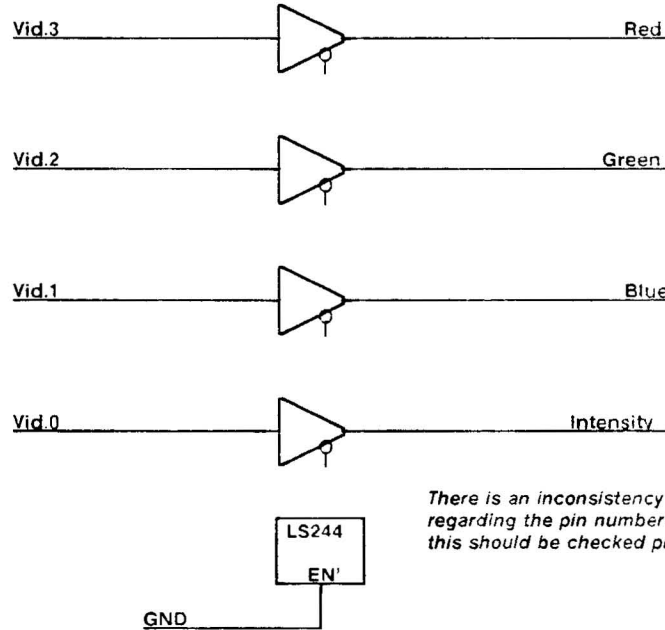
## IBM Color Connector



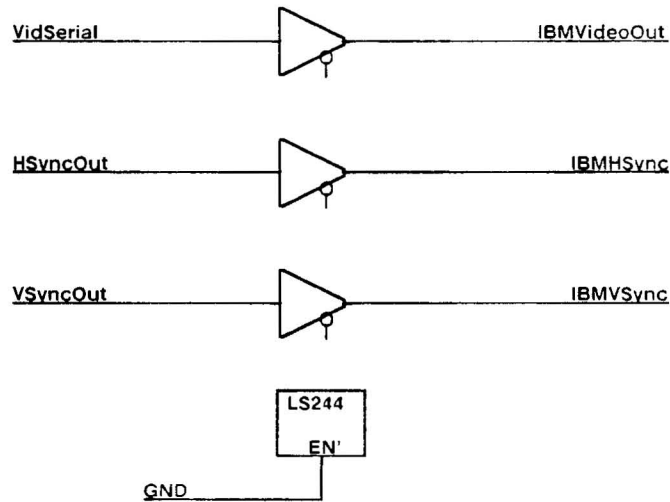
## IBM Monochrome Connector



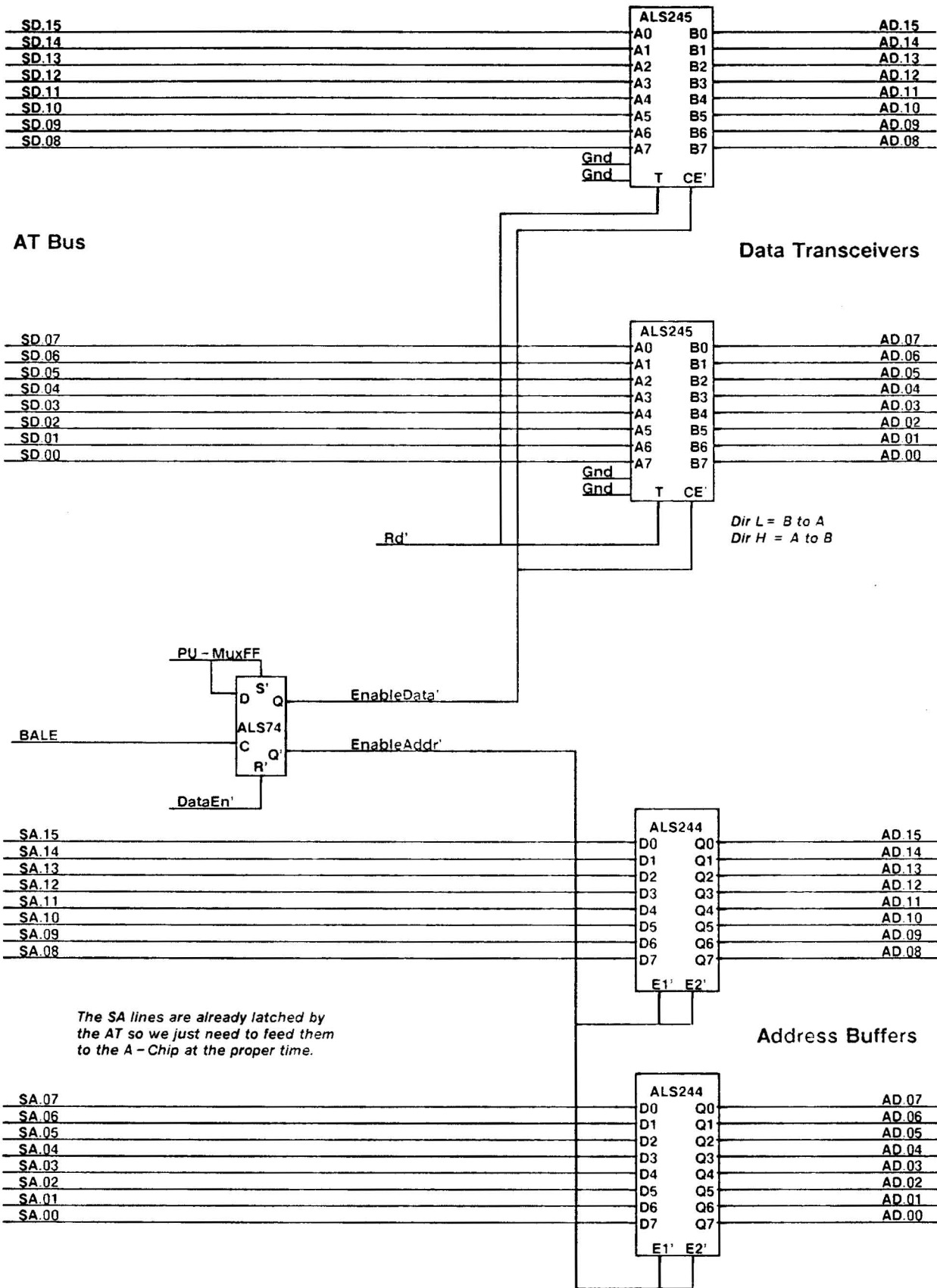
*The numbers in italics are the DB-9 pin numbers*



*There is an inconsistency in the AChip spec regarding the pin numbers for R,G & B. So this should be checked prior to fabrication.*



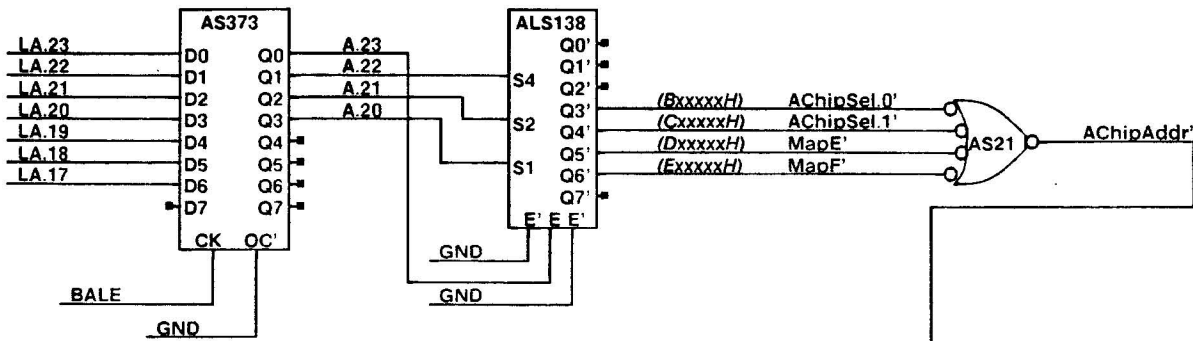




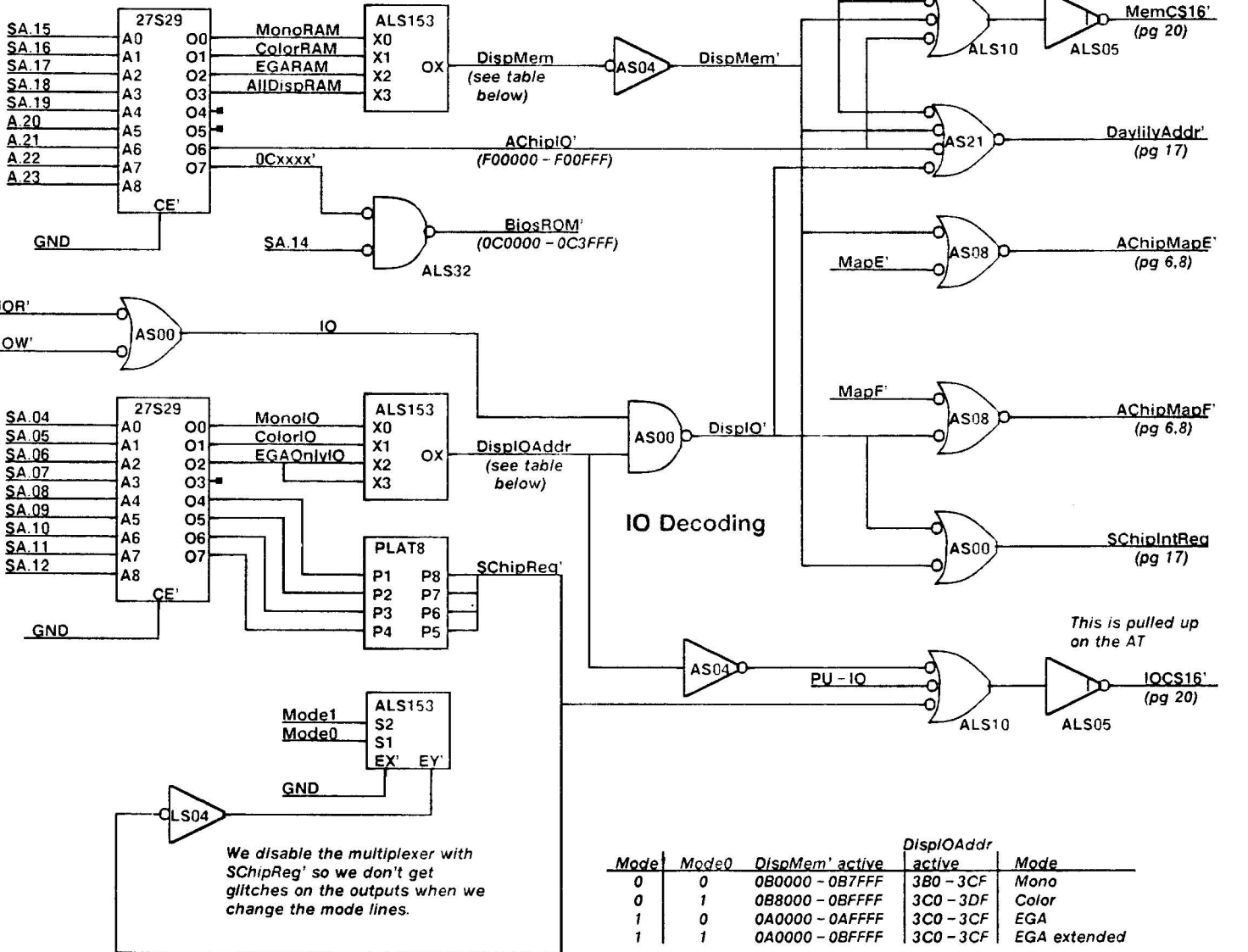
How this Works:

The address from the 80286 is available when BALE goes high and is latched on the falling edge of BALE, which also clocks the flip-flop above enabling the address to pass thru the ALS244's to the A - Chip. This will continue until DataEn' goes low which resets the flip-flop enables the data transceivers. The direction of the transfer is controlled by Rd'

|              |                    |                                  |                       |                    |          |                 |            |
|--------------|--------------------|----------------------------------|-----------------------|--------------------|----------|-----------------|------------|
| XEROX<br>SDD | Project<br>DayLily | AT to AChip Address and Data Mux | File<br>Daylily15 sil | Designer<br>Colvin | Rev<br>A | Date<br>2/26/86 | Page<br>15 |
|--------------|--------------------|----------------------------------|-----------------------|--------------------|----------|-----------------|------------|



### Memory Decoding



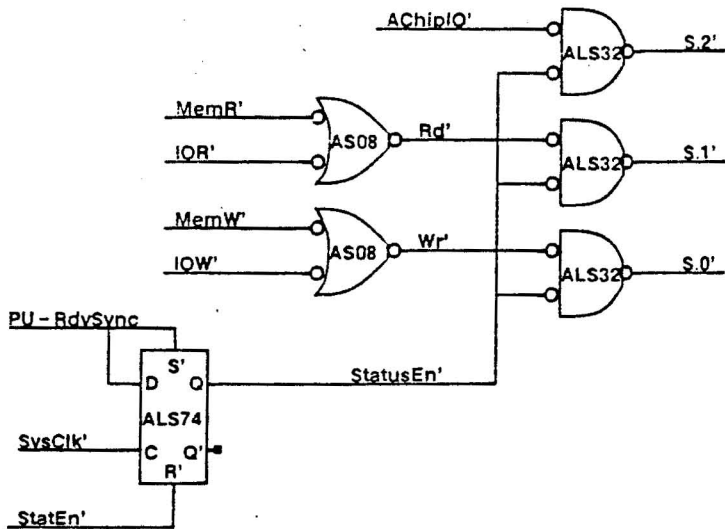
We disable the multiplexer with SChipReg' so we don't get glitches on the outputs when we change the mode lines.

This circuitry is the result of many iterations and many days of effort. I am not really happy with the way it turned out but it seems to work. This circuitry performs several major functions. The LS138 decodes the AChip memory address space. The top 27S29 PROM decodes the addresses for EGA display memory, the EGA BIOS EPROM, and maps memory to AChip IO addresses. This will decode both IO and memory addresses, but the AT spec says that there are no valid IO addresses in range that we are decoding (I am not sure that I believe that). The lower 27S29 PROM decodes IO to IBM EGA addresses and for the SChip register. The EGA addresses are qualified with IOR' and IOW' to verify that they are IO and not memory addresses. The PROM decodes four addresses for the SChip register, only one of these is used and is selected by a jumper on the platform shown. This allows the board address to be changed if it's address conflicts with another board in the system.

All references to EGA addresses are mapped into the AChip using the map E & F registers, they also interrupt the SChip, so the SChip can update the appropriate memory values.

Any addresses for the EGA or AChip lowers DaylilyAddr' which starts the state machine.

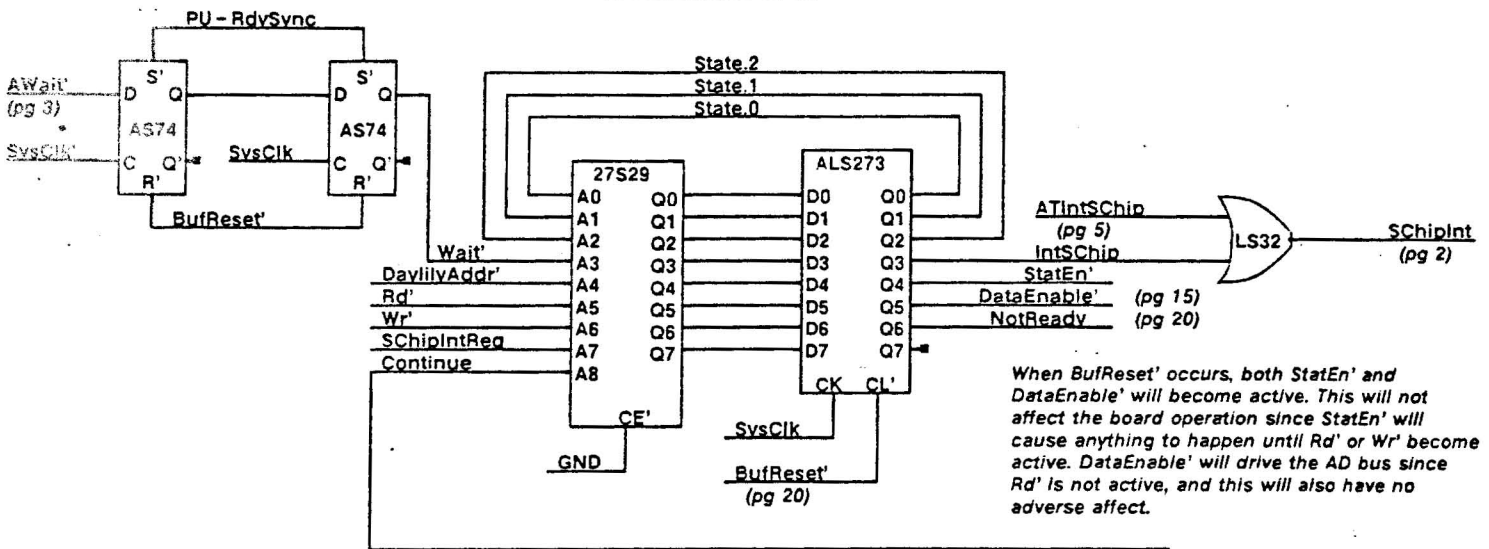
## Status Generation



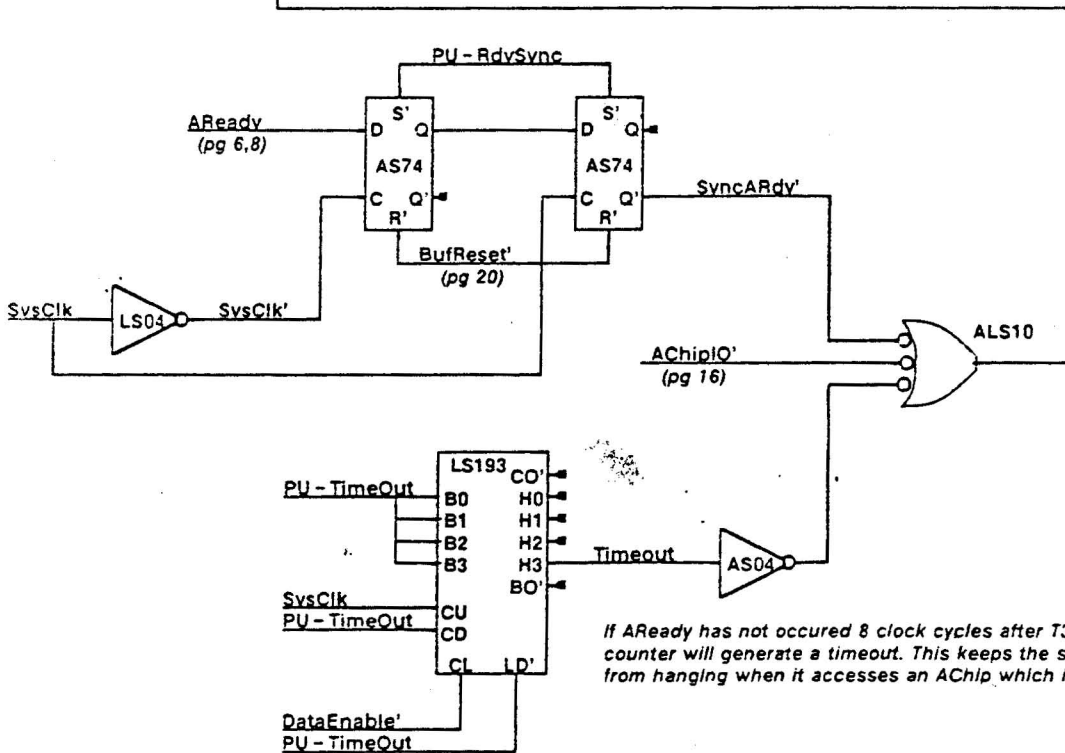
| S2 | S1 | S0 | ACHip operation    |
|----|----|----|--------------------|
| 0  | 0  | 0  | idle               |
| 0  | 0  | 1  | IO Read            |
| 0  | 1  | 0  | IO Write           |
| 0  | 1  | 1  | idle               |
| 1  | 0  | 0  | Memory Read (idle) |
| 1  | 0  | 1  | Memory Read        |
| 1  | 1  | 0  | Memory Write       |
| 1  | 1  | 1  | idle               |

StatEn' is controlled by the state machine. It is asserted whenever an AChip is addressed or whenever an AT Graphics Adaptor IO port is addressed. Enabling the status lines starts all AChip operations.

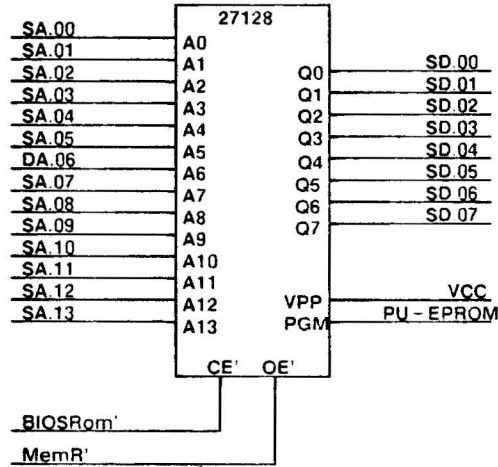
## State Machine



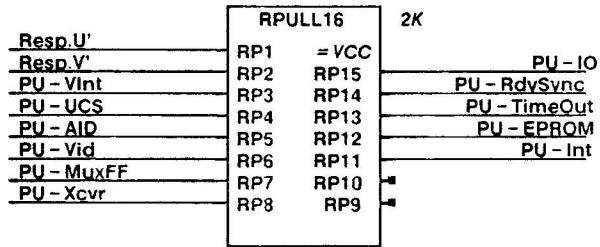
When BufReset' occurs, both StatEn' and DataEnable' will become active. This will not affect the board operation since StatEn' will cause anything to happen until Rd' or Wr' become active. DataEnable' will drive the AD bus since Rd' is not active, and this will also have no adverse affect.



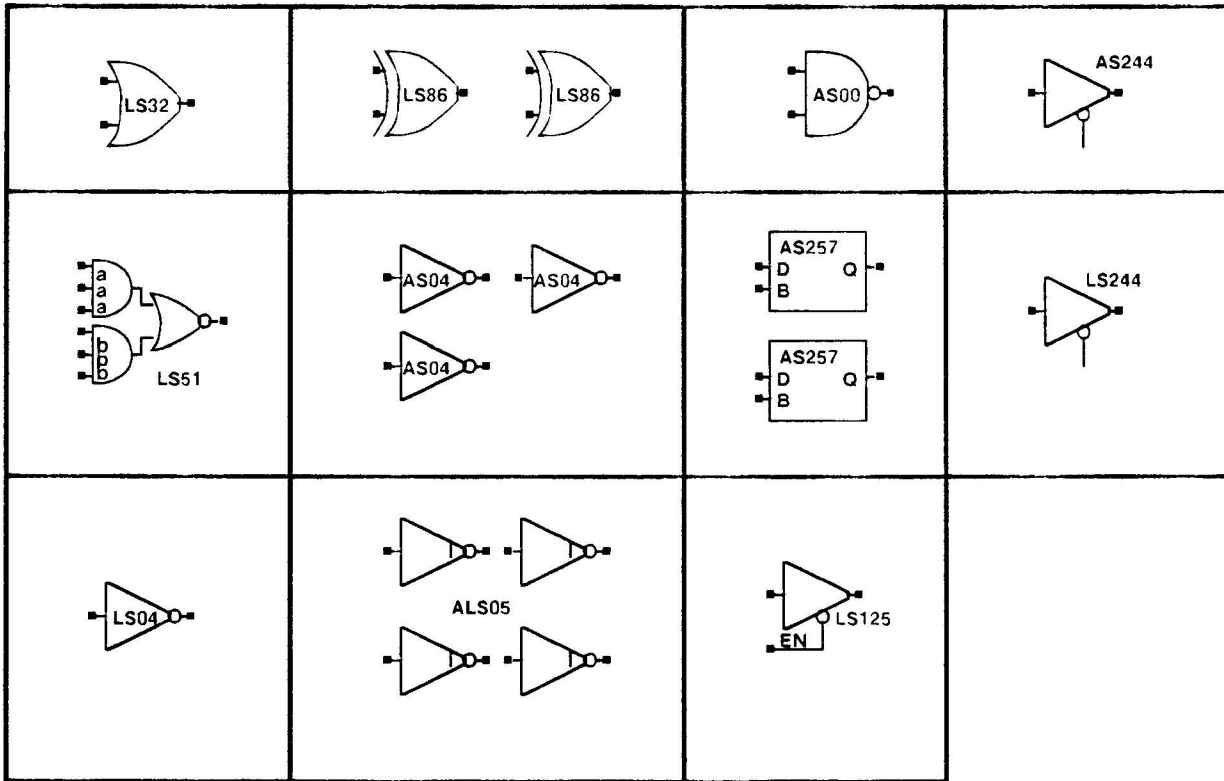
If AReady has not occurred 8 clock cycles after T3 then this counter will generate a timeout. This keeps the state machine from hanging when it accesses an AChip, which is not present.



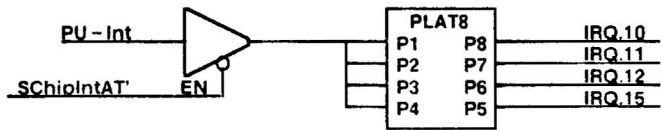
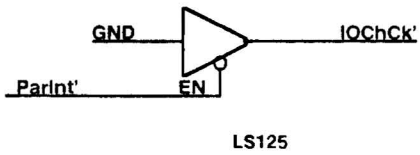
*This is currently implemented as a single EPROM due to board space requirements. It would be a performance win to replace this with two 2764's if they can fit on the board.*



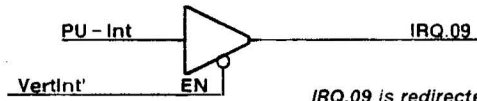
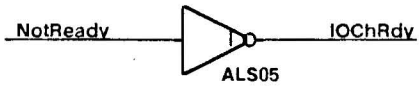
Spares



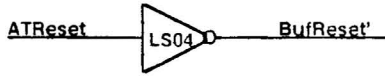




This platform is included so that the interrupt can be easily changed.



IRQ.09 is redirected in software to IRQ.02 so it will agree with use of IRQ.02 on PC's

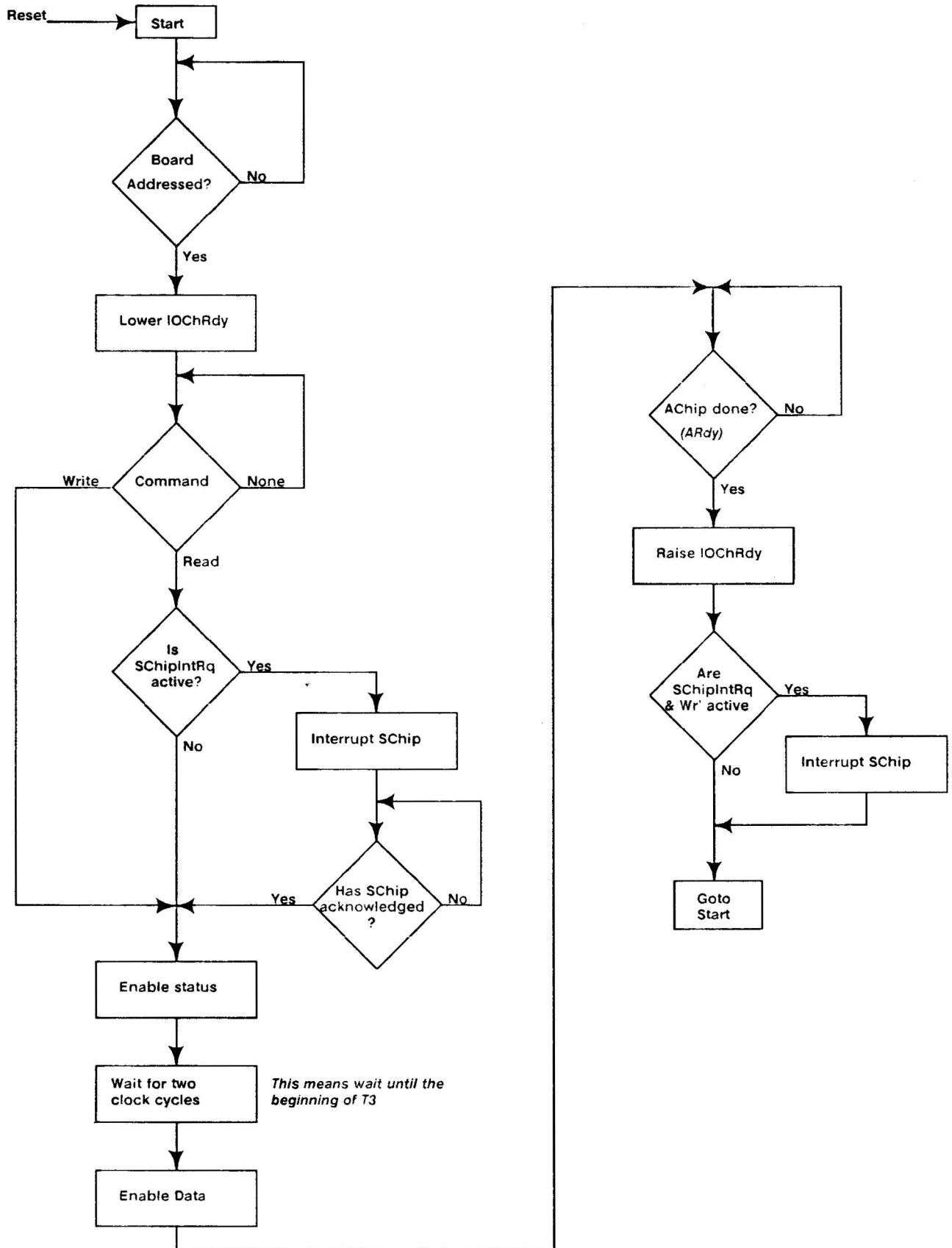


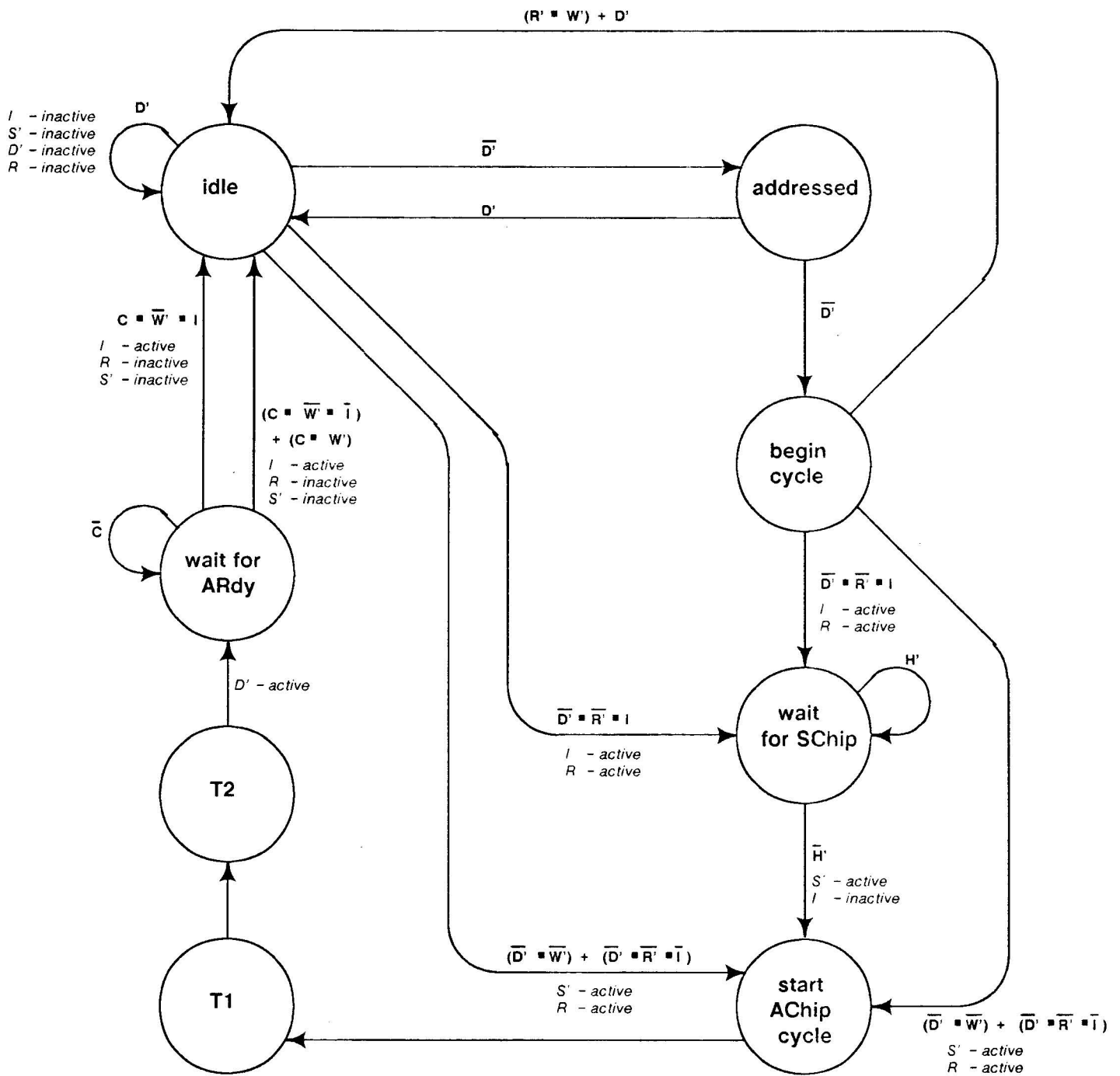
|        |  |     |
|--------|--|-----|
| SA.00  |  | A31 |
| SA.01  |  | A30 |
| SA.02  |  | A29 |
| SA.03  |  | A28 |
| SA.04  |  | A27 |
| SA.05  |  | A26 |
| SA.06  |  | A25 |
| SA.07  |  | A24 |
| SA.08  |  | A23 |
| SA.09  |  | A22 |
| SA.10  |  | A21 |
| SA.11  |  | A20 |
| SA.12  |  | A19 |
| SA.13  |  | A18 |
| SA.14  |  | A17 |
| SA.15  |  | A16 |
| SA.16  |  | A15 |
| SA.17  |  | A14 |
| SA.18  |  | A13 |
| SA.19  |  | A12 |
| LA.17  |  | C8  |
| LA.18  |  | C7  |
| LA.19  |  | C6  |
| LA.20  |  | C5  |
| LA.21  |  | C4  |
| LA.22  |  | C3  |
| LA.23  |  | C2  |
| IRQ.03 |  | B25 |
| IRQ.04 |  | B24 |
| IRQ.05 |  | B23 |
| IRQ.06 |  | B22 |
| IRQ.07 |  | B21 |
| IRQ.09 |  | B4  |
| IRQ.10 |  | D3  |
| IRQ.11 |  | D4  |
| IRQ.12 |  | D5  |
| IRQ.14 |  | D7  |
| IRQ.15 |  | D6  |

|          |  |     |
|----------|--|-----|
| SD.00    |  | A9  |
| SD.01    |  | A8  |
| SD.02    |  | A7  |
| SD.03    |  | A6  |
| SD.04    |  | A5  |
| SD.05    |  | A4  |
| SD.06    |  | A3  |
| SD.07    |  | A2  |
| SD.08    |  | C11 |
| SD.09    |  | C12 |
| SD.10    |  | C13 |
| SD.11    |  | C14 |
| SD.12    |  | C15 |
| SD.13    |  | C16 |
| SD.14    |  | C17 |
| SD.15    |  | C18 |
| ATCLK    |  | B20 |
| ATRreset |  | B2  |
| BALE     |  | B28 |
| IOChck'  |  | A1  |
| IOChRdy  |  | A10 |
| TermCnt  |  | B27 |
| SBHE     |  | C1  |
| Master'  |  | D17 |
| DRQ.0    |  | D9  |
| DRQ.1    |  | B18 |
| DRQ.2    |  | B6  |
| DRQ.3    |  | B16 |
| DRQ.5    |  | D11 |
| DRQ.6    |  | D13 |
| DRQ.7    |  | D15 |
| DACK.0   |  | D8  |
| DACK.1   |  | B17 |
| DACK.2   |  | B26 |
| DACK.3   |  | B15 |
| DACK.5   |  | D10 |
| DACK.6   |  | D12 |
| DACK.7   |  | D14 |

|          |  |     |
|----------|--|-----|
| IOR'     |  | B14 |
| IOW'     |  | B13 |
| SMemR'   |  | B12 |
| SMemW'   |  | B11 |
| MemR'    |  | C9  |
| MemW'    |  | C10 |
| AEN      |  | A11 |
| Refresh' |  | B19 |
| MemCS16' |  | D1  |
| IOCS16'  |  | D2  |
| QWS      |  | B8  |
| Qsc      |  | B30 |
| GND      |  | B1  |
| GND      |  | B10 |
| GND      |  | B31 |
| GND      |  | D18 |
| +5v      |  | B29 |
| +5v      |  | D16 |
| +5v      |  | B3  |
| -5v      |  | B5  |
| +12v     |  | B9  |
| -12v     |  | B7  |

The softcard remains inactive until a valid address for either main memory or a memory/I/O request for the Enhanced Display adaptor occurs. At that time state machine lowers the IOChRdy signal on the bus which will cause the 80286 processor to wait until the softcard is done. The state machine then enables the status lines to the A-Chip and starts cycling thru the T-states of an 80186. At T3 it will pause until it receives the ARdy signal from the AChip.





**INPUTS**

$D'$  = DaylilyAddr'  
 $R'$  = Rd'  
 $W'$  = Wr'  
 $I$  = SChipIntRq  
 $C$  = Continue  
 $H'$  = Wait'

**Outputs**

$I$  =  $\bar{S}$ Chip  
 $S'$  =  $\bar{S}$ atEn'  
 $D'$  = DataEnable'  
 $R$  = NotReady