3. Display Control

3. Display Control

3.1 General Information

The display controller, display memory, memory controller, and part of system memory are contained on the Display Control and Memory (DCM) board. This section describes display control. Refer to Section 4 for discussion of memory.

The display controller uses a partitioned, three-port memory to reduce the loss of processor bandwidth while the display is running. The display controller has highest priority access to the low 256K memory bank only when it is acquiring data bits during an active horizontal line. The IOP or Mesa processor has complete access to the low bank at all other times.

Figure 3.1 illustrates the ports for data transfer between the DCM and other system components.

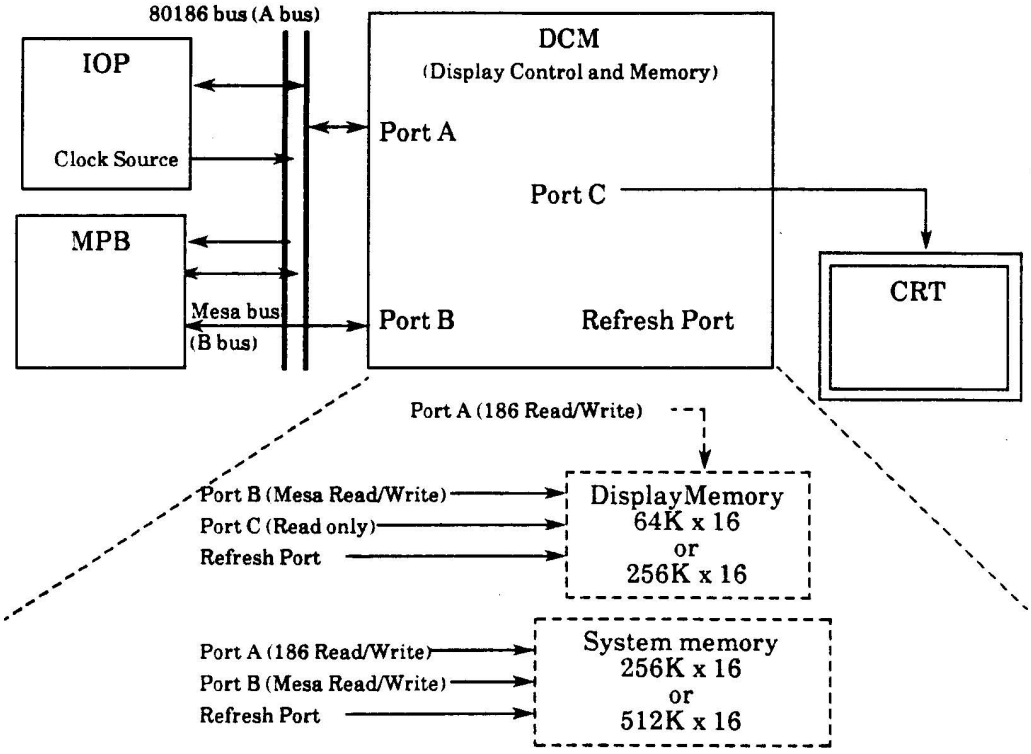


Figure 3.1. DCM data paths

Port A is the 80186 bus port to memory. For display memory, this port is used for diagnostics. Port B is the Mesa bus read/write port to memory. Port C is a read-only port in display memory, accessed by the display controller; Port C is passive in system memory. The refresh port refreshes memory on command from the MCC gate array.

3.1.1 Display Parameters

DCM control parameters, control registers, and cursor RAM are written and read by the Input/Output Processsor (IOP).

Dove display parameters include:

- 10.4 in. high by 7.9 in. wide bit map display. Active bitmap for 15-inch monitor is 13 quadwords x 633 lines; for 19-inch monitor, 17 quadwords x 861 lines.
- Separate video, horizontal, and vertical sync signals.
- Software-controlled horizontal and vertical scrolling.
- Hardware-supported cursor.
- Visible area: Total = 896 x 697 pixels of bitmap and border, of which 832 x 633 pixels are bitmap for 15-inch monitor.
- Total frame (visible + non-visible) = 737 lines x 1120 bits for 15-inch monitor; for 19-inch monitor = 981 lines x 1520 bits.
- Border area = 32 lines at top, 32 lines at bottom, 32 bits at each side. Contents of programmable register are repeated to form the border pattern. The size of top and bottom borders is set by microcode.
- Refresh rate = 38 frames/second, or one frame every 26.3 ms.
- Memory used - optional. Baseline is 64 KWord (64 x 16), expandable to 256 KWord (256 x 16).

The display memory is implemented in 64K or 256K DRAMs and is the first 64 KW of the 256 KW memory space. Up to 1.0 Mbytes of system memory, in 512 Kbyte blocks, is placed on the DCM card. System memory size is independent of the optional display memory size.

3.1.2 Hardware

The DCM board contains:

- three bipolar gate arrays that constitute the display controller, as described in section 3.2.1
- other display subsystem hardware, also described in section 3.2.1
- memory controller gate array chips, described in Section 4, for display memory and system memory
- buses, as follows: A-Bus (IOP) and B-Bus (Mesa) for system memory; A-Bus, B-Bus, and C-Bus (display) for bitmap memory.

This section describes the DCM board layout, interfaces, and power.

3.1.2.1. Display Control and Memory Board

The DCM board is a full size (10.9" x 16"), four signal layer PWBAthat connects to the backplane connector J2.

Figure 3.2 illustrates the board layout. Appendix C contains the parts list for the board.

Figure 3.2. DCM board layout

3.1.2.2 Interfaces

Table 3.1 lists the backplane interfaces of the board. On the backplane, pins are grouped in six rows of three columns each. The table reflects the grouping.

Table 3.1. DCM Backplane Pin Assignment (Front View).

Outmost — Inmost

1) 80186 Bus

Spare-1 J2.001	GND J2.002	Spare-2 J2.003
A/AD.07 (bi) J2.004	A/DT/R' (i) J2.005	A/AD.15 (bi) J2.006
A/AD.06 (bi) J2.007	A/DEN' (i) J2.008	A/AD.14 (bi) J2.009
A/AD.05 (bi) J2.010	GND J2.011	A/AD.13 (bi) J2.012
A/AD.04 (bi) J2.013	A/MemRdy (o) J2.014	A/AD.12 (bi) J2.015
A/AD.03 (bi) J2.016	A/ALE' J2.017	A/AD.11 (bi) J2.018
A/AD.02 (bi) J2.019	A/IOPMemWr' (i) J2.020	A/AD.10 (bi) J2.021
A/AD.01 (bi) J2.022	Spare-3 J2.023	A/AD.09 (bi) J2.024
A/AD.00 (bi) J2.025	GND J2.026	A/AD.08 (bi) J2.027
GND J2.028	A/CLK (i) J2.029	VCC J2.030

J2.031 GND	J2.032 GND	J2.033 GND
J2.034 A/AA.19*	J2.035 (i) A/S.2'	J2.036 A/AA.23*
J2.037 A/AA.18*	J2.038 (i) A/S.1'	J2.039 A/AA.22*
J2.040 A/AA.17*	J2.031 (i) A.S.0'	J2.042 A/AA.21*
J2.043 A/AA.16*	J2.044 (i) A/BHE'	J2.045 A/AA.20*
J2.046 A/EPROMCs'	J2.047 GND	J2.048 (i) A/IOR'
J2.049 Reserved-0	J2.050 A/LocRamCS'*	J2.051 Spare-4
J2.052 (i) A/IOPLock'	J2.053 GND	J2.054 (i) A/IOW'
J2.055 A/PCHldToArb	J2.056 (i) A/IOPMemRd'	J2.057 (i) Spare-5
J2.058 -5V	J2.059 -5V	J2.060 -5V

2) MPB-DCM

GND J2.061	GND J2.062	GND J2.063
A/IORdy* J2.064	A/MA.23 (i) J2.065	A/MA.22 (i) J2.066
Spare-7 J2.067	A/MA.21 (i) J2.068	A/MA.20 (i) J2.069
SpareID'* J2.070	A/MA.19 (i) J2.071	A/MA.18 (i) J2.072
DBRK/DAISY'* J2.073	A/MA.17 (i) J2.074	A/AA.16B (i) J2.075
A/PEINT' (o) J2.076	GND J2.077	MPB-DCM-spare1 J2.078
A/MEBIntr'* J2.079	MPB-DCM-spare2 J2.080	
A/VRETINT (o) J2.082		
GND J2.085	GND J2.083	
A/RawCLK (i) J2.088	MPB-DCM-spare3 J2.086	
	GND J2.089	

3) Mesa Bus

B/MWT' (i)	J2.081
Dawn-Mp-spare1	J2.084
B/MRD' (i)	J2.087
VCC	J2.090

* Not used

- more -

Table 3.1. DCM Backplane Pin Assignment (continued)

Outmost

4) IOP-Mesa

J2.091	GND	J2.092	GND	J2.093	GND
J2.094	A/IOPIntMP*	J2.095	CSWREN*	J2.096 (o)	A/MEMS'
J2.097	A/MPIntIOP*	J2.098	CSLOAD/SHIFT*	J2.099 (i)	B/Lock'
J2.100	A/IOPRdNIA	J2.101	CSBUFFEREN*	J2.102	B/IOR*
J2.103	A/Halt'	J2.104	CSDATAIN*	J2.105 (i)	B/MemRef
J2.106	IOP-S-spare1	J2.107	CSSHIFTCLK*	J2.108	B/IOW*
J2.109	A/ResetMPB'	J2.110	CSDATOUT*	J2.111 (o)	B/Rdy
J2.112	VCC	J2.113	VCC	J2.114	VCC
J2.115	VCC	J2.116	VCC	J2.117 (i)	VCC
J2.118	VCC	J2.119	VCC	J2.120	VCC

Inmost

3) MesaBus (continued)

GND	J2.121	GND	J2.122	GND	J2.123
GND	J2.124	GND	J2.125	GND	J2.126
GND	J2.127	GND	J2.128	GND	J2.129
INTDIS'	J2.130	B/A.18 (i)	J2.131	B/ALE' (o)	J2.132
B/A.23 (i)	J2.133	B/A.17 (i)	J2.134	Dawn-Mp-spare3	J2.135
B/A.22 (i)	J2.136	GND	J2.137	B/D.11 (bi)	J2.138
B/A.21 (i)	J2.139	B/D.15 (bi)	J2.140	B/D.10 (bi)	J2.141
B/A.20 (i)	J2.142	B/D.14 (bi)	J2.143	B/D.09 (bi)	J2.144
B/A.19 (i)	J2.145	B/D.13 (bi)	J2.146	B/D.08 (bi)	J2.147
-12V	J2.148	-12V	J2.149	-12V	J2.150

J2.151	GND	J2.152	GND	J2.153	GND
J2.154 (bi)	B/D.07	J2.155 (bi)	B/D.12	J2.156 (bi)	B/D.06
J2.157 (bi)	B/D.05	J2.158	GND	J2.159 (bi)	B/D.04
J2.160 (bi)	B/D.03	J2.161 (i)	A/Reset'	J2.162 (bi)	B/D.02
J2.163 (bi)	B/D.01	J2.164	GND	J2.165 (bi)	B/D.00

The DCM interfaces with the 80186 bus (A bus) at Port A and with the Mesa bus at Port B. Table 3.2 lists the pins and signals for the interfaces.

Table 3.2. Bus Interface Signals

80186 BUS (A bus)

Signal	Pin	Signal Description
A/MA.23	J1.065	
A/MA.22	J1.066	
A/MA.21	J1.068	Mapped
A/MA.20	J1.069	
A/MA.19	J1.071	Address
A/MA.18	J1.072	
A/MA.17	J1.074	
A/A.16B	J1.075	Address 16
A/AD.15	J1.006	
A/AD.14	J1.009	
A/AD.13	J1.012	
A/AD.12	J1.015	
A/AD.11	J1.018	
A/AD.10	J1.021	
A/AD.09	J1.024	Address/Data
A/AD.08	J1.027	
A/AD.07	J1.004	
A/AD.06	J1.007	Bus
A/AD.05	J1.010	
A/AD.04	J1.013	
A/AD.03	J1.016	
A/AD.02	J1.019	
A/AD.01	J1.022	
A/AD.00	J1.025	
A/BHE'	J1.044	Bus High Enable
A/S2'	J1.035	
A/S1'	J1.038	Bus cycle
A/S0'	J1.041	status
A/PEINT"	J1.076	Parity error interrupt
A/MRD'	J1.086	Memory read operation
A/MWT"	J1.080	Memory write operation
A/IOR'	J1.048	IOP read operation
A/IOW'	J1.054	IOP write operation
A/RAWCLK	J1.088	80186 system clock
A/RESET"	J1.161	Reset
A/VRETINT"	J1.014	Vertical retrace interrupt
A/IOWL'	J1.082	Not used
A/ALE	J1.057	Address latch enable
A/DEN'	J1.008	Data enable
A/DT/R'	J1.005	Data transmit/receive
A/MEMS'	J1.096	Memory status select
IOPLOCK'	J1.052	Lockout other bus masters
8MHzCLK	J1.029	System Clock
A/PCEHLDA'	J1.055	PCE Hold acknowledge

MESA BUS (B bus)

Signal	Pin	Signal Description
B/A.23	J1.133	
B/A.22	J1.136	
B/A.21	J1.139	Mesa
B/A.20	J1.142	Address
B/A.19	J1.145	Bus
B/A.18	J1.131	
B/A.17	J1.134	
B/D.15	J1.140	
B/D.14	J1.143	
B/D.13	J1.146	
B/D.12	J1.155	
B/D.11	J1.138	
B/D.10	J1.141	
B/D.09	J1.144	
B/D.08	J1.147	Mesa
B/D.07	J1.154	Data
B/D.06	J1.156	Bus
B/D.05	J1.157	
B/D.04	J1.159	
B/D.03	J1.160	
B/D.02	J1.162	
B/D.01	J1.163	
B/D.00	J1.165	
B/MRD'	J1.087	Memory read operation
B/MWT"	J1.081	Memory write operation
B/MEMREF"	J1.105	Memory reference request
B/LOCK'	J1.099	Lock out other bus masters
B/RDY	J1.111	Mesa bus ready
B/ALE	J1.132	Address latch enable

3.1.2.3 Power

Table 3.3 lists the power consumption by the display controller. Table 3.4 lists the power interface for the DCM board. Power interface to the backplane is given in Table 1.1.

Table 3.3. Display Controller Power Consumption

	Typical	Maximum
+5V	2721 mA 13.61 W	3888 mA 19.44 W
-5.2V	70 mA 0.36 W	100 mA 0.52 W

Table 3.4. Power Interface

Vee	J1.058	RawVCC	J1.030	GND	J1.085	GND	J1.002
	J1.059		J1.190		J1.089		J1.011
	J1.060		J1.112		J1.091		J1.026
			J1.113		J1.092		J1.032
			J1.114		J1.093		J1.047
GND	J1.061		J1.115		J1.121		J1.053
	J1.062		J1.116		J1.122		J1.151
	J1.063		J1.117		J1.123		J1.152
			J1.118		J1.124		J1.153
			J1.119		J1.125		J1.158
			J1.120		J1.126		J1.164
					J1.127		
					J1.128		
					J1.129		

3.2 Display Control

Figure 3.3 illustrates the major components that control display, as described in this section:

- display controller – retrieves data from display memory, mixes the cursor pattern with display data at the cursor position, and sends the data to the display monitor. The controller consists of three gate array chips: an 84-pin display data chip (DDC); an 84-pin display cursor chip (DCC); and a 68-pin display memory chip (DMC). See also Appendix A for a description of a CMOS display controller chip.
- horizontal and vertical control store – 256 x 4 (horizontal) and 2K x 4 (vertical) PROMs that control vertical and horizontal events. Each PROM holds parameters for two display sizes.
- display data FIFO – a 64 x 16 RAM buffer between memory and the display data chip. Data is input from memory in Intel bit format and is output in Mesa bit format.
- cursor buffer – holds the cursor pattern. Data is input in Intel byte format (32 x 8 byte) and is output in Mesa word format (16 x 16).
- Video shift register – shifts the data out to the display in a serial format.

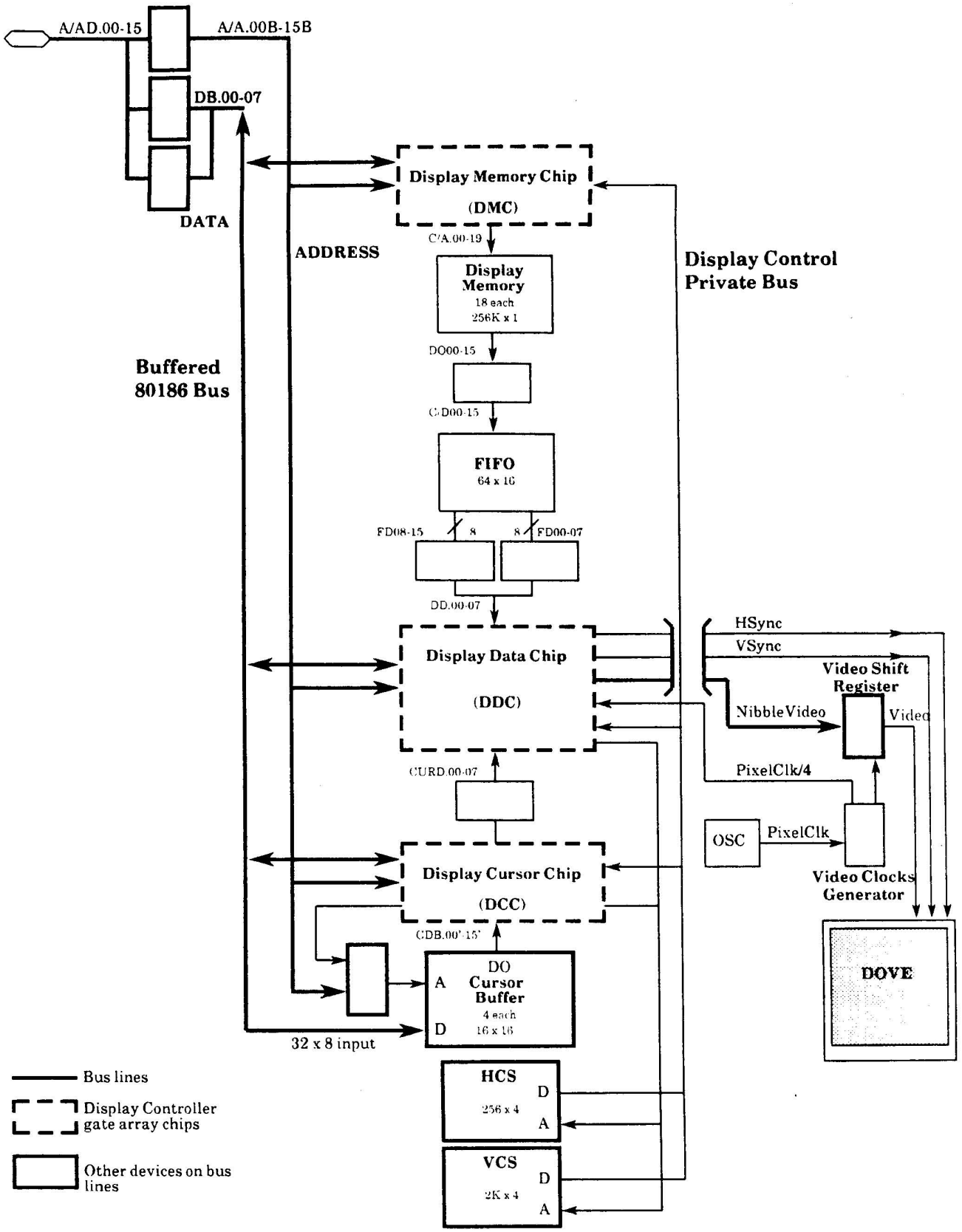


Figure 3.3. Display controller block diagram

3.2.1 Hardware

The following figures illustrate pins and signals for the display subsystem components.

- Figure 3.4 Display Data Chip
- Figure 3.5 Display Cursor Chip
- Figure 3.6 Display Memory Chip
- Figure 3.7 Vertical and Horizontal Control Store
- Figure 3.8 FIFO
- Figure 3.9 Cursor Buffer

Table 3.5 describes the signals shown in the figures.

Table 3.6 describes internal signals. Data paths for these signals are illustrated in the subsection 3.2.2, titled " Theory of Operations."

HCSA.00	(Output)		1	P1	P84	84	(Output)		HCSA.01
		(Input)	2	P2	P83	83	(Output)		HCSA.02
		(Input)	3	P3	P82	82	(Output)		HCSA.03
		(Input)	4	P4	P81	81	(Output)		HCSA.04
	CURD.00	(Input)	5	P5	P80	80	(Output)		HCSA.05
	CURD.01	(Input)	6	P6	P79	79	(Output)		HCSA.06
	CURD.02	(Input)	7	P7	P78	78	(Output)		HCSA.07
	CURD.03	(Input)	8	P8	P77	77			
	CURD.04	(Input)	9	P9	P76	76	(Output)		CURWORDB'
		VCC	10	P10	P75	75			
		GND	11	P11	P74	74	VCC		
	CURD.05	(Input)	12	P12	P73	73	GND		
	CURD.06	(Input)	13	P13	P72	72			
	CURD.07	(Input)	14	P14	P71	71			
	PXLCLK/4	(Input)	15	P15	P70	70	(I/O)		DB.07
	CENB'	(Input)	16	P16	P69	69	(I/O)		DB.06
	CSD.00	(Input)	17	P17	P68	68	(I/O)		DB.05
	CSD.01	(Input)	18	P18	P67	67	(I/O)		DB.04
	CSD.02	(Input)	19	P19	P66	66	(I/O)		DB.03
	CSD.03	(Input)	20	P20	P65	65	(I/O)		DB.02
BHSYNC	(Output)		21	P21	P64	64	(I/O)		DB.01
HA'/VAB	(Output)		22	P22	P63	63	(Output)		DB.00
BYTECLKB	(Output)		23	P23	P62	62	(Input)		A/A.01B
HA/VA'B	(Output)		24	P24	P61	61	(Input)		A/A.00B
PCLK/16B	(Output)		25	P25	P60	60	(Input)		DDCS'
BVSYNC'	(Output)		26	P26	P59	59	(Input)		A/IORB'
PCLK/16B	(Output)		27	P27	P58	58			
			28	P28	P57	57	(Input)		SHCLKB
PCLK/16B	(Output)	29		P29	P56	56	(Input)		A/IOWB'
		VCC	30	P30	P55	55			
			31	P31	P54	54	(Input)		DDCRST'
		GND	32	P32	P53	53	VCC		
			33	P33	P52	52	(Input)		DD.07
			34	P34	P51	51	(Input)		DD.06
CBKGNDB	(Output)		35	P35	P50	50	(Input)		DD.05
VRESTNB	(Output)		36	P36	P49	49	(Input)		DD.04
INTLACEB	(Output)		37	P37	P48	48			
	(Output)		38	P38	P47	47	(Input)		DD.03
VID.0	(Output)		39	P39	P46	46	(Input)		DD.02
VID.1	(Output)		40	P49	P45	45	(Input)		DD.01
VID.2	(Output)		41	P41	P44	44			
VID.3	(Output)		42	P42	P43	43	(Input)		DD.00

Figure 3.4. Display Data Chip (DDC) pin-out

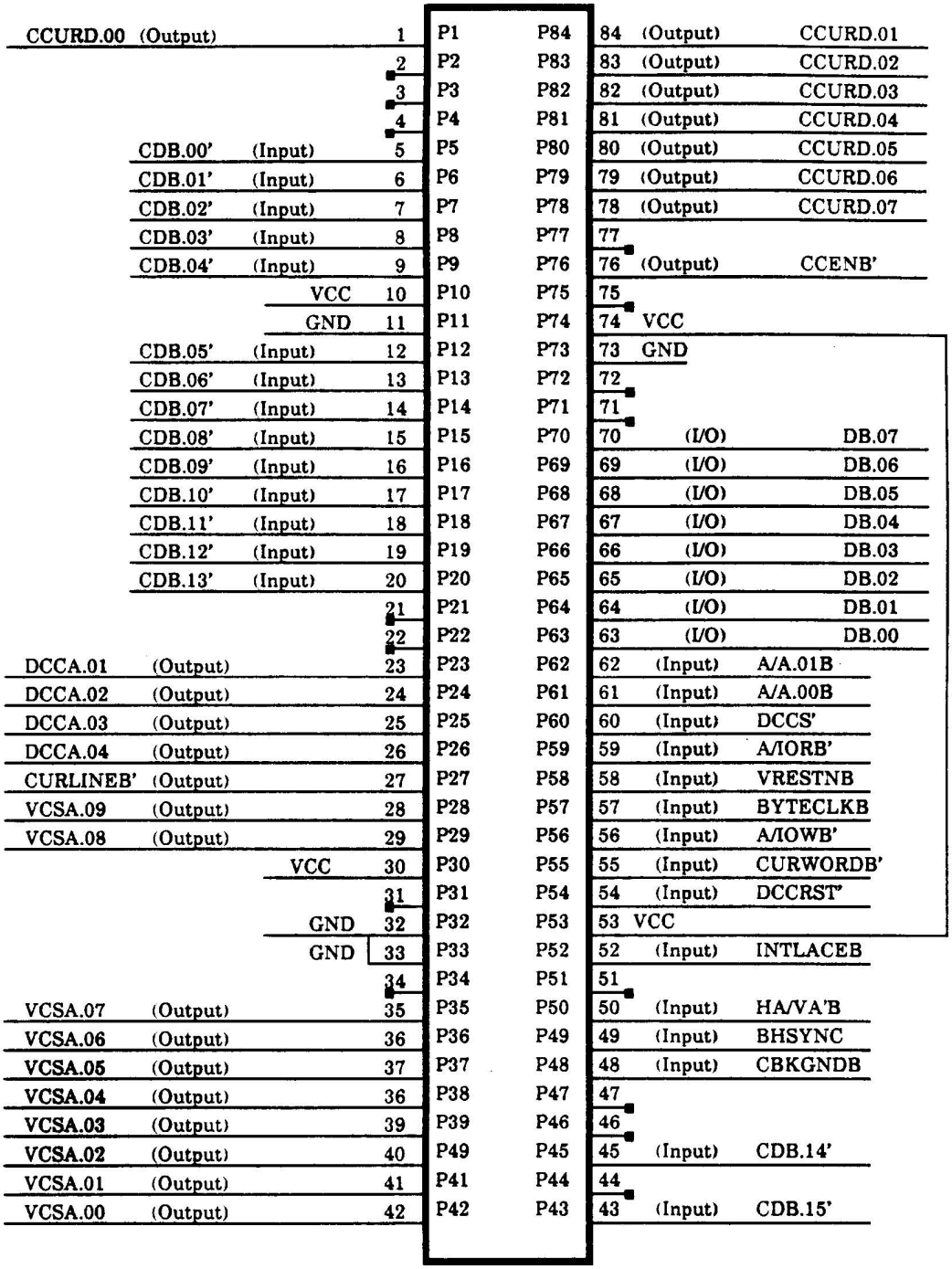


Figure 3.5. Display Cursor Chip (DCC) pin-out

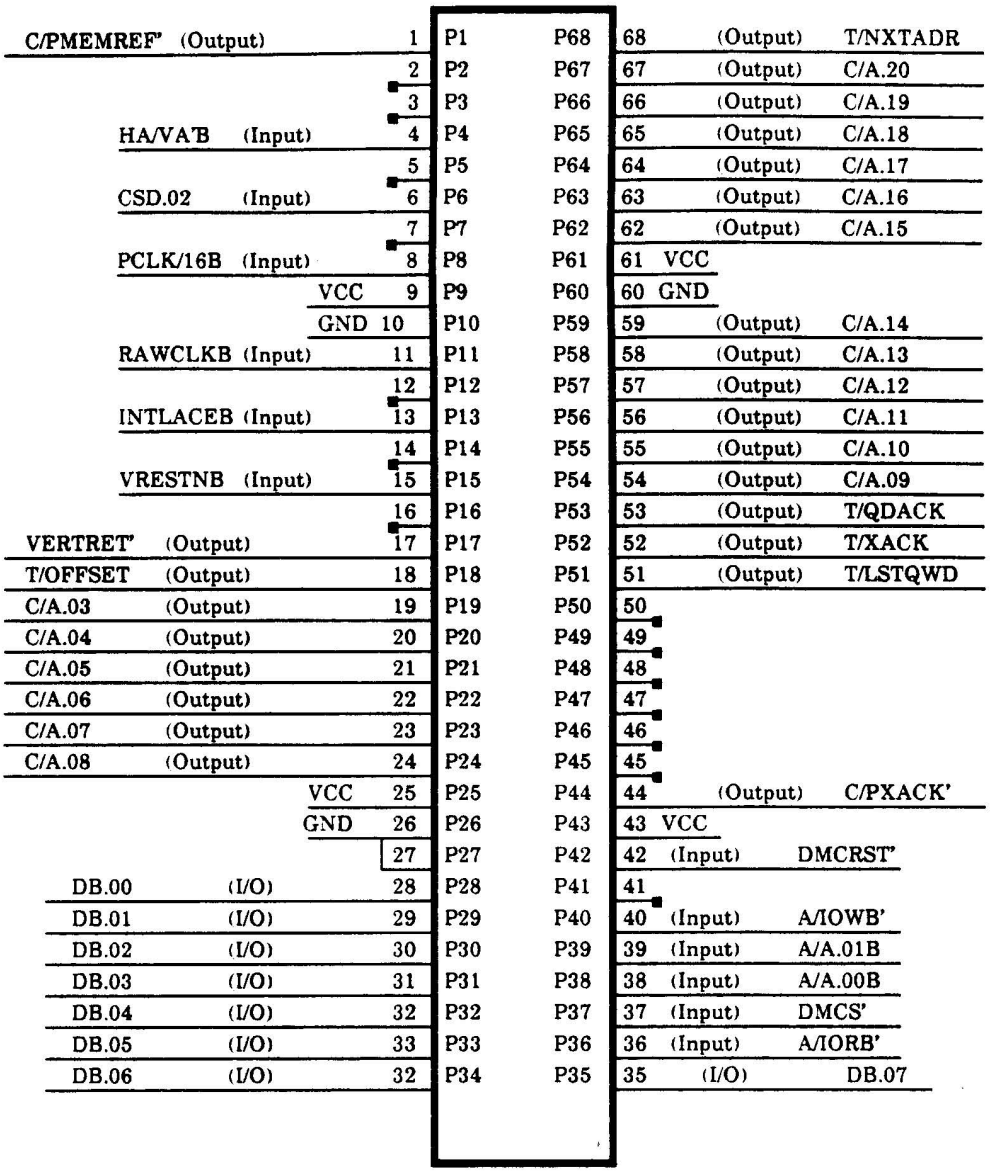


Figure 3.6. Display Memory Chip (DMC) pin-out

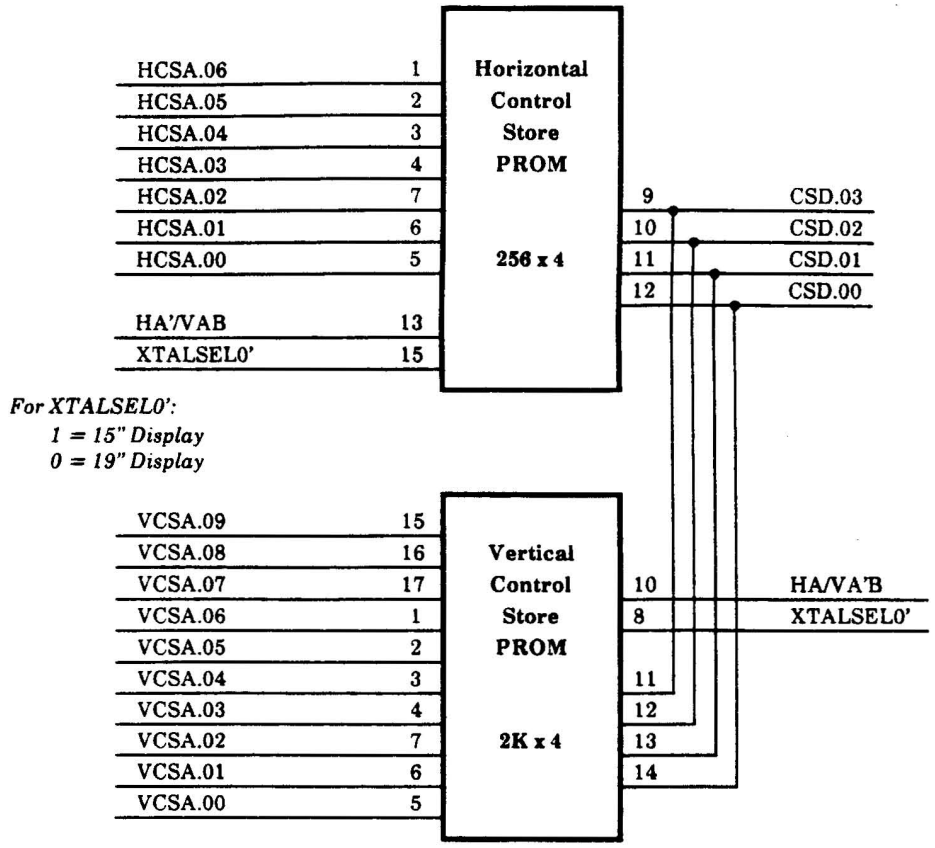


Figure 3.7. Horizontal and Vertical CS pins and signals

Intel Bit Format CHIP 1	2	3	4		← Display FIFO (4) →			Mesa Bit Format CHIP 1	2	3	4
GND	→	→	→	8	D4	04	11				
C/D07	C/D03	C/D15*	C/D11	7	D3	03	12	FD.00*	FD.04	FD.08	FD.12
C/D06	C/D02	C/D14	C/D10	6	D2	02	13	FD.01	FD.05	FD.09	FD.13
C/D05	C/D01	C/D13	C/D09	5	D1	01	14	FD.02	FD.06	FD.10	FD.14
C/D04	C.D00**	C/D12	C/D08	4	D0	00	15	FD.03	FD.07	FD.11	FD.15**
				2	IR	OR	16				
TXACK	→	→	→	3	SI	SO	17	PCLK/16G	→	→	→
BVSYNC'	→	→	→	10	MR'						

Note: These signals are sent to the display data latches, which output DD.00-07. DD.00 is MSB; DD.07 is LSB.

* *MSB*
** *LSB*

Figure 3.8. Display FIFO pins and signals

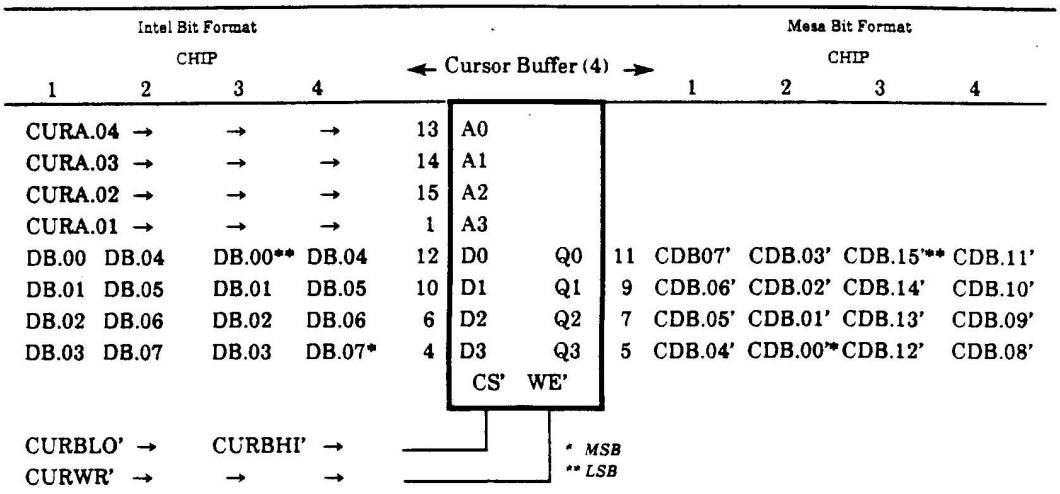


Figure 3.9. Cursor buffer pins and signals

Table 3.5. Display Control External Signal Description

Signal	From (see key at end of table)	To	Function
A/A.00B-01B	IOP	DC, CS, CB	Address lines to select internal registers within devices.
A/IORB', A/IOWB'	IOP	DC, CS	Read/Write controls. Active low strobe...
BHSync	DDC	DCC, CRT	Horizontal synchronizer to the CRT. Increments line counter in DCC.
BVSync	DDC	CRT, DF	Synchronizes vertical events for CRT, and clears display FIFO.
ByteClkB	DDC	DCC	Pixel clock divided by 8 and inverted. Informs DCC when to switch a byte and which byte to switch.
C/A.00-20	DMC	Memory	Address to port C in display memory; addresses bitmap.
C/D.00-15	Memory	DF	Data from bitmap to FIFO.
C/PMEMREF'	DMC	Memory	Memory request to bitmap memory; that is, to the MCC for display memory.
C/XACK'	MCC	DMC	DMC counts CXACK' strobes to determine how many more words must be requested. Also a control signal to FIFO.
CBKGNDB	DDC	DCC	Cursor Background. Determines value of background data to DDC when a cursor is not being mixed with display data.
CDB.00'-15'	CB	DCC	Cursor data.
VCSA.00-09 HCSA.00-07	DCC DDC	CS	Address to control store. DDC generates the signal during horizontal events, DCC generates it during vertical events.
CSD.00-03	CS	DC	Data bits that inform the display controller what to do for every line (vertical events controlled by the DCC) and every word (horizontal events controlled by the DDC). During line events, the DMC monitors the bits to determine if data must be fetched.
CENB'	DDC	DDC	Cursor enable. Active low signal that informs DDC to mixcursor data with display data.

- more -

Table 3.5. Display Control External Signal Description (continued)

Signal	From	To	Function
CURA.00-04	IOP	CB	Addresses to load cursor buffer. DCC uses the addresses to read the buffer.
CURBLO'/HI'	(IOP)	CB	Enables high and low bytes for cursor RAMs. Sent by the IOP unless the cursor is being displayed. If the cursor is displayed, then the signals are sent by the DCC, and both bytes are enabled.
CURD.00-07	DCC	DDC	Shifted data (full shift) from RAM. This data is the actual, bit-aligned cursor information.
CURLINEB'	DCC	DDC	Active low signal that notifies DDC to display the cursor for this line.
CURWORDB'	DDC	DCC	Qualifier for cursor word. Enables DCC cursor-enable logic.
CURWR'	(IOP)	CB	A/IOWB' buffered and enabled for H/V control store.
DB.00-07	IOP	DC, CB	IOP data bus.
DCCA.01-04	DCC	CB	Cursor buffer address.
DD.00-07	DF	Memory	Bitmap display data from latches at the end of the FIFO.
DD(/C/M)CRST'		DC	Reset from hardware or software to a display controller gate array chip.
DD(/C/M)CS'		DC	Chip select for a display controller gate array chip.
FD.00-15	DF	Latches	Intermediate data from display FIFO to display data latches.
HA/VA'B	DCC	CS, DMC	Active low signal requesting data for a vertical event.
HA'/VAB	DDC	CS	Active low signal requesting data for a horizontal event.
INTLACEB	DDC	DCC	Control signal indicating whether display is programmed for interlaced mode, as follows: 1 = interlace; 0 = non-interlace.
PCLK/16B	DDC	DMC	Pixel clock divided by 16. DMC uses this clock to synchronize internal functions and to clock data from the display FIFO into the display data latches. Also selects which output goes to the DDC at a given time; multiplexes data from 16 to 8 bits.
PCLK/16G'	DDC	DF	Pixel clock divided by 16. Internally gated in DDC; indicates when to pull words from the display FIFO.
PCSA.08-09	DCC	CS	Precursor or intermediate CSA addresses.
PXLCLK/4	DCM Board	DDC	Pixel clock divided by 4. Generates other clocks for the display subsystem.
RAWCLKB	IOP	DMC	80186 system clock that synchronizes memory requests.
SHCLKB	DCM Board	DDC	Select Horizontal Clock selects whether to delay HSYNC by nibble clock or byte clock.
T/LSTQWD	DMC	MCC	Indicates that last quadword has been received; stops memory requests.
T/NXTADR T/OFFSET T/QDACK	DMC		Test points
T/XACK	DMC	DF	Clocks data into FIFO
VID0:3	DDC	vid shift reg	4-bit nibble of video data.
VERTRET'	DC	IOP	Vertical retrace interrupt sent once per field.
VRESTNB	DDC	DCC, DMC	Notification to start a new field.

Abbreviation Key:

DC Display Controller (all three display gate arrays)
DCC Display Cursor Chip
CB Cursor Buffer
CRT Display Monitor
MCC Memory Controller Chip
DDC Display Data Chip
DMC Display Memory Chip
CS Horizontal and Vertical Control Store
DF Display FIFO

The letter B appended to a signal name indicates a buffered signal.

Table 3.6. Display Subsystem Internal Signals

Signal	Interface		Function
	From	To	
DDC			
Blank	Event machine	flip-flop	Output is ANDed with video data and blanks the screen: Video forced to 0.
BorderSelect	Event machine	mux	Determines high or low border byte to be displayed
HAddr.0-7	Horizontal address counter	horizontal control store	Horizontal control store address
(Mix Function)	IOP	Data/Cursor Mixer	Part of control byte sent from IOP that informs DDC how to mix the data and cursor; that is, by logic functions 1 of 16 mix.
Pic/Bdr'	Event machine	mux	Determines whether picture or border is shown.
(VertClks) 3	Event machine	DDC logic	Three pulses generated in time across a line, as specified by H/V control store. Identifies three points at which specific actions should occur, as follows: Vertclk1 - Zero horizontal counter, load vertical parameters. Vertclk2 - If VSync is true and line is odd, enable VSync. Vertclk3 - If VSync is true and line is even, enable VSync.
DCC			
1. BOS.0-1 2. BOS.2 3. BOS.3	IOP	1 bit shifter 2 nibble shifter 3 byte shifter	Bit Offset that determines how many bits to shift the cursor within a word, as follows: 1. Bits 0-1 determine how many bits are to be shifted within locations 0-3 (of a nibble). 2. Bit 2 determines whether to shift an entire nibble; that is, a 0-7 bit shift. 3. Bit 3 determines whether to shift the entire byte.
CByte0'-2'	Cursor byte select	Nibble shifter	Byte enable; determines which of three bytes to send to the DDC.
(Cursor line)	Cursor Line	logic	Counts H-syncs to determine if this is a cursor line.
DMC			
(Bitmap starting addr)	Preset latches (IOP)	Quadword adder addresser	Informs addresser where in the bitmap to begin display.
EOFBBB'	V/H control store		End of Frame - with HA/VA informs DMC that an end of line or end of field (EOF) has occurred. If EOF, then a reset occurs, setting the starting address at the next field.
EOField	V/H control store	Interrupt generator	CSD3, qualified by HA/VA. EOFBBB and vertical retrace are derived from the signals.
Evenfield	Interrupt	Memory address generator	Notifies the address generator where to start the address or whether to add a number of words and show that line.
Lastquad-wordactive0-3	Last quadword detector	Mem reference circuitry	Turns off memory request.
LatchSel0-3	decoder	Preset latches	Selects latches
MemAddr0:17	Quadword adder	drivers	Memory address that was generated in the adder.
MemRefBef'	Mem reference circuitry		Controls quadword counts per line.

- more -

Table 3.6. Display Subsystem Internal Signals (continued)

Signal	Interface		Function
	From	To	
DMC			
Next Address Sel	Next memory address selection	Quadword adder	Selects either the bitmap starting address (beginning of field) or the current memory address + 1.
QuadWord	IOP writes to Preset latches	Last quadword detector	Indicates how many quadwords to include in one line, depending on the size of the display monitor; for example, 13 quadwords for a 15" display.
QuadWord Count	Quadword counter	Last quadword detector	Actual count, which is compared to QuadWord. If the two are not equal, then 1 is added. If the two are equal, then the integer equal to the number of quadwords per line is added.
QuadWord Offset 0:7	Mem Addr quadword offset	Quadword adder	Causes a line jump. Memory addresses jump a number of addresses in a line in the bitmap. Informs DMC whether to add 1 or an integer number (4 x number of quadwords).
QuadXAck	XACK counter	a) Quadword counter b) latch	Divide-by-four counter of XACK syncs to generate the number of quadword acknowledges; clocks the counts.
VerretInt'	Interrupt generator	drivers	Vertical Retrace Interrupt; sent to IOP once per field.
Vert.PPic/Bdr'	Control store	Next memory address selection	CSD02 gated with HA/VA. Determines whether next line will show bitmap data. Stops DMC from retrieving bitmap data during borders and blanking.
XAckSync	Sync	a) XACK counter b) Next memory address selection	C/XACK synchronized with raw clock.

3.2.2 Theory of Operations

The display controller on the DCM board provides a high resolution bitmap display. The controller autonomously fetches display data from memory, buffers it in a FIFO, and sends it synchronously to the display. Vertical and horizontal syncs are generated. A 16 bit by 16 bit, bit-aligned cursor is stored internally and mixed into the display stream. Video data and syncs are supplied directly to a simple display interface. The pixel clock rate is independent of other clocks, and can be as high as 56.66 MHz.

The parameters of the display controller are set from the 80186 bus; in other respects the display controller is transparent to the programmer.

The display controller competes with the Mesa processor and IOP for access to display memory. Because the display memory accesses are normally performed at a lower priority than the refresh and higher priority than the 80186 and Mesa memory accesses, the display controller must contain a pixel buffer to absorb fluctuations in the available bandwidth. The pixel buffer, a FIFO on the DCM board, is filled whenever a memory cycle is available at the beginning of each active display (bitmap only) line, and is emptied to the display at a constant rate.

3.2.2.1 Display Controller

This subsection illustrates the functional blocks of the gate array chips that constitute the display controller. First the chip I/O is illustrated, then internal data paths are shown. Refer to the preceding tables for signal descriptions.

Note: Appendix A describes the Daybreak Display Controller (DDC) chips, which is a CMOS LSI chip replacing the gate array chips in later Daybreak machines.

Display Data Chip (DDC)

The display data chip retrieves data from the display FIFO and sends it to the display monitor. It mixes display data with cursor pattern data, provides addressing for the horizontal control store, and generates the sync signals to the CRT.

Figure 3.10 illustrates the I/O for the functional blocks of the DDC; Figure 3.11 illustrates the internal data paths.

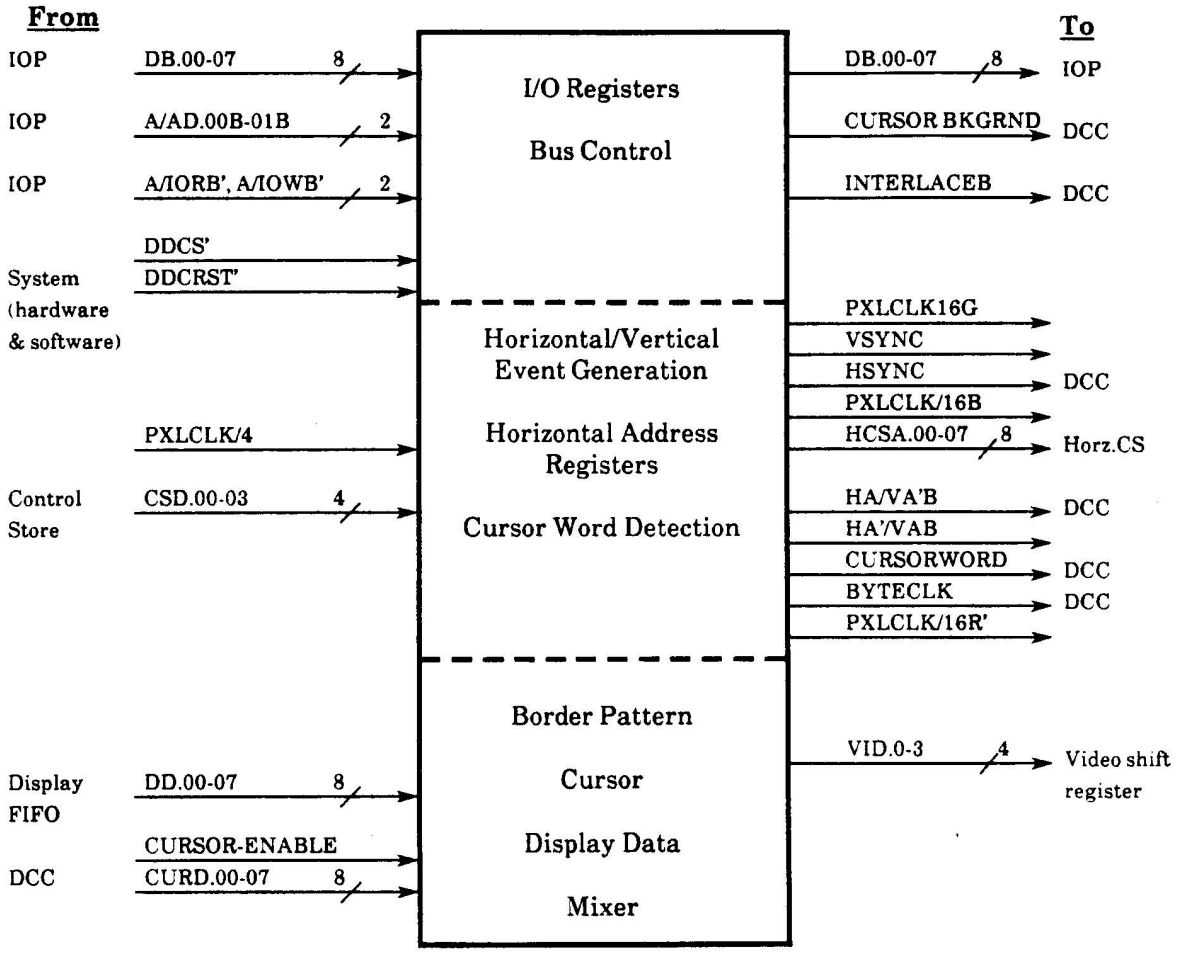


Figure 3.10. Display Data Chip I/O

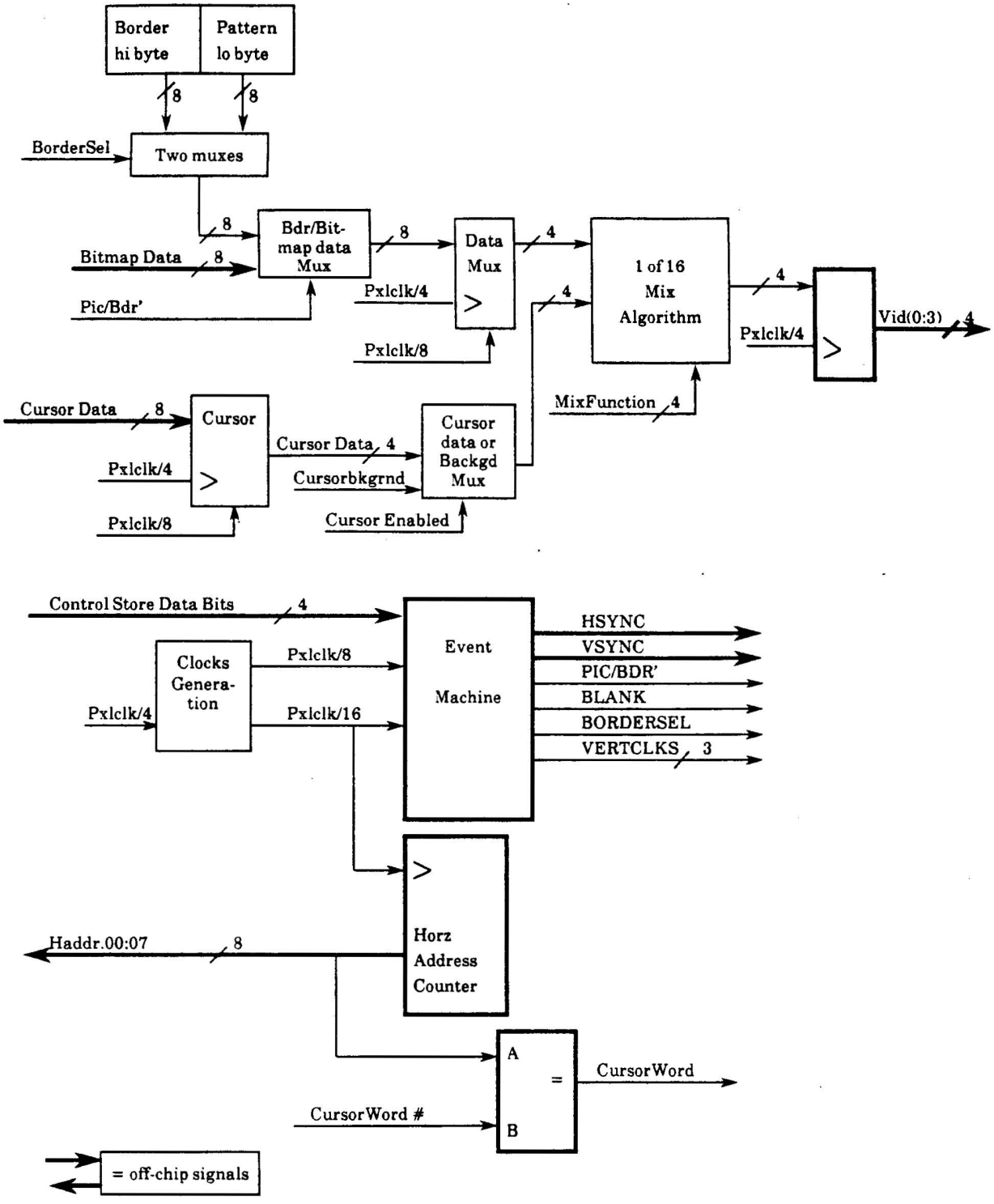


Figure 3.11. DDC internal data paths

Display Cursor Chip (DCC)

The display cursor chip fetches data from the 16 x 16 cursor buffer. It aligns cursor data to a bit boundary. It also provides cursor control, based on data from the IOP which specifies the scan line and word at which to locate the cursor, and generates the vertical control store addresses.

Figure 3.12 illustrates the I/O for the functional blocks of the DCC; Figure 3.13 illustrates the internal data paths.

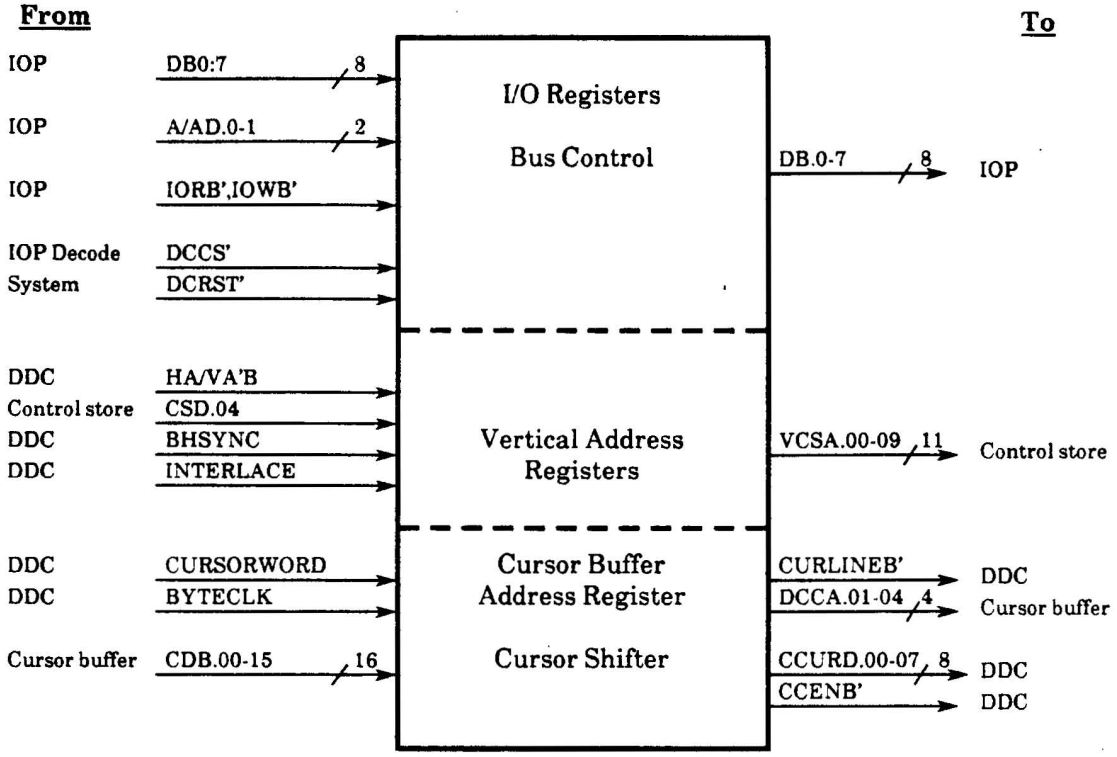


Figure 3.12. Display Cursor Chip I/O

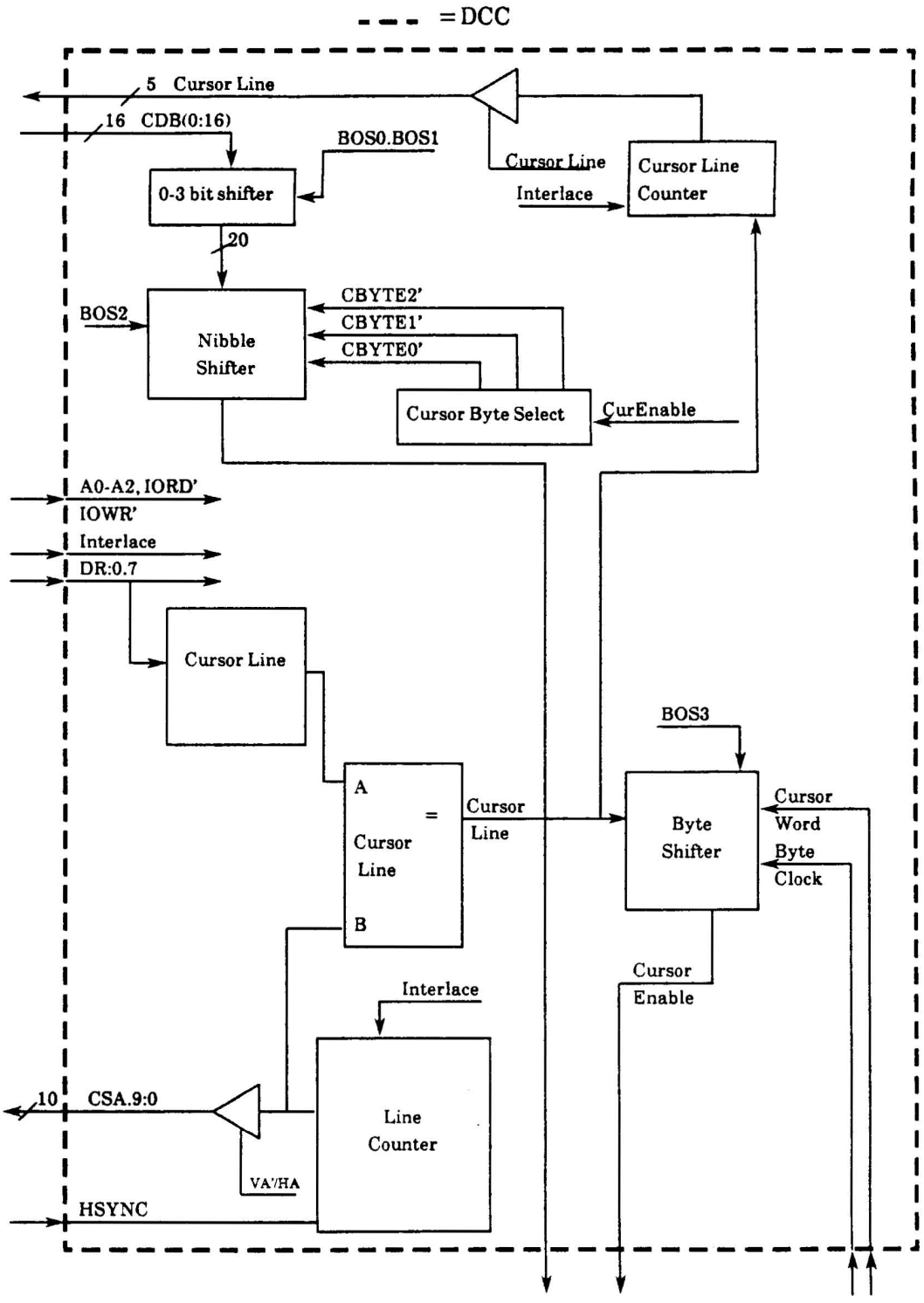


Figure 3.13. DCC internal data paths

Display Memory Chip (DMC)

The display memory chip retrieves bitmap data from memory and stores it into a FIFO. Data is fetched in quadwords, using the nibble mode feature of the DRAM. Every reference, therefore, is 4 bits.

Figure 3.14 illustrates the I/O of the functional blocks of the display memory chip; Figure 3.15 illustrates internal DMC data paths.

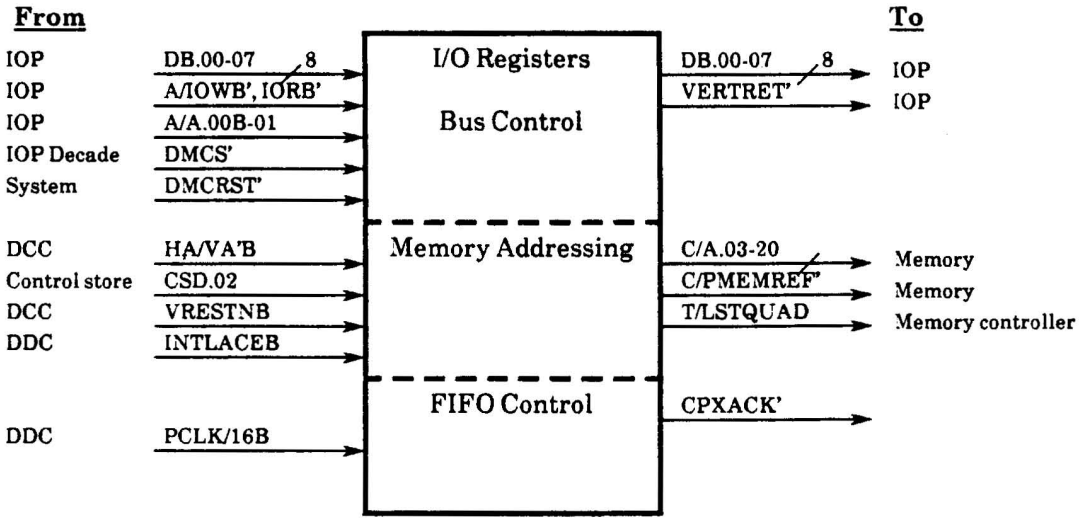


Figure 3.14. Display Memory Chip I/O

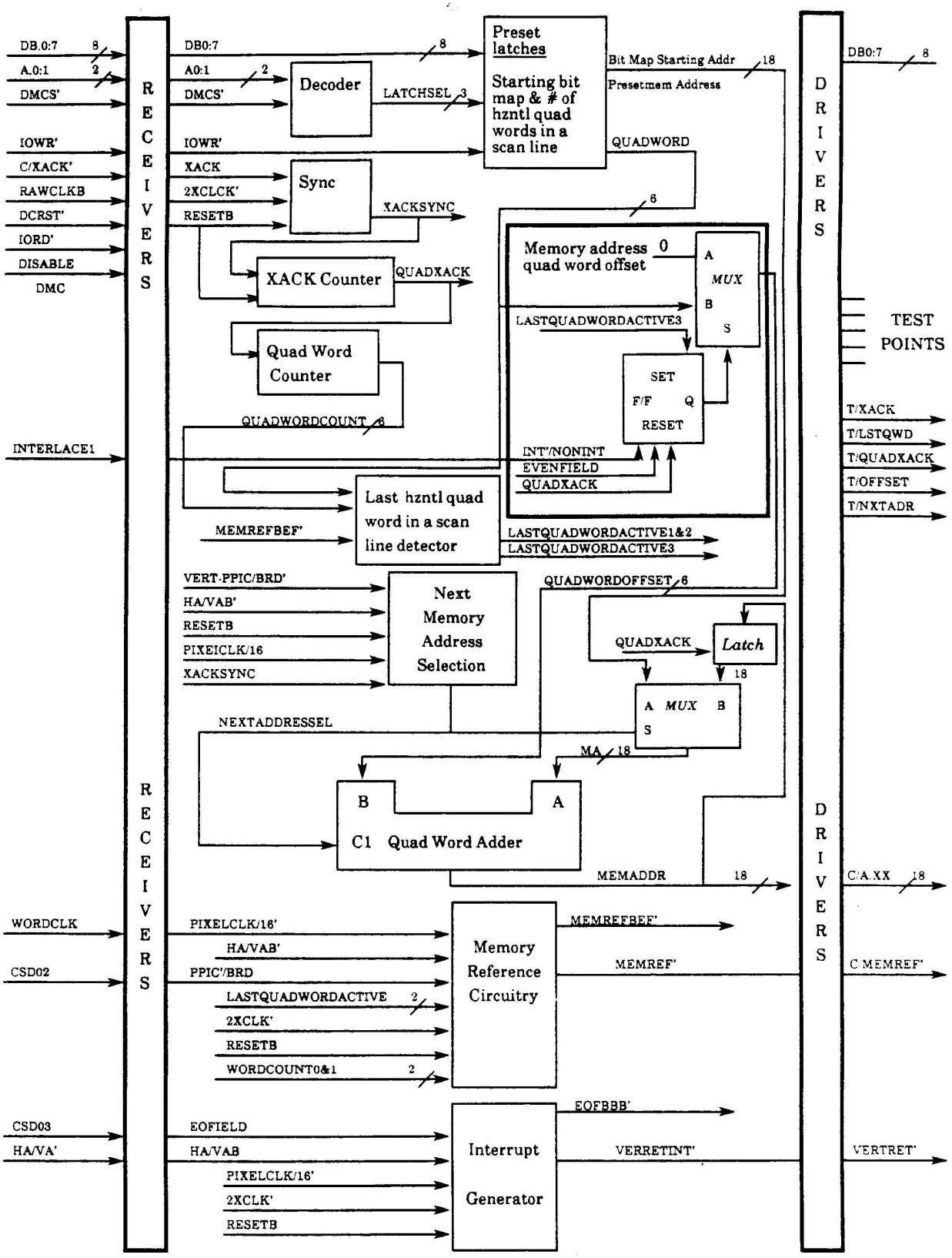


Figure 3.15. DMC internal data paths

3.2.2.2. Display Initialization

Display is initialized as follows:

1. The display size port is read to determine the CRT size.
2. The cursor may be initialized (depending on the operating system). The cursor pattern is loaded into the cursor buffer. The cursor address is loaded: the line number and bit offset into the DCC, and the word number into the DDC.
3. The Display Memory Chip is initialized, the bitmap starting location is loaded, and the number of quadwords per line is loaded.

   Note: Steps 2 – 3 can be done in any sequence.
4. The Display Data Chip is initialized. The border pattern and control register are loaded. When the control register is loaded, the display is enabled, and the display is started at the first word, first line (top left corner of the display).

3.2.2.3. Display Line Control

The following sequence describes the control of the display line. Figure 3.16 summarizes the sequence; Figure 3.17 illustrates the timing.

1. Hblank is started. This step occurs after step 4 of display initialization, after a reset or power-on, or after completion of the line control sequence.
2. At the signal Vertclk1, the vertical parameters for the next line are loaded. The vertical parameters include Vblank', Vpic/bdr', Vsync', and EOF (end of field).

   If the next line is an active bitmap display line, then a memory read sequence is started.
3. Hsync is started and clocks the DCC. The line number is incremented.
4. For non-interlace mode, all vertical signals are enabled at Vertclk2.

   For interlaced mode, at Vertclk2, if Vblank' and Vpic/brd' were set in step 2, then they are now enabled. When Vblank' goes low, a vertical retrace interrupt is sent to the IOP.

   If the line is an odd number, and if Vsync' was set true at step 2, then Vsync' is now enabled. If the line is an even number, then Vsync is not yet enabled.
5. The DDC clears Hsync and Hblank; the border is enabled for two more words.
6. The border is cleared and bitmap data is displayed.

7. Halfway through the scan line, Vertclk3 occurs. If Vsync' was true and if the line number is an even number, then (in interlace mode) Vsync' is enabled now. Otherwise, no action occurs at Vertclk3.
8. When the data ends, the display switches from bitmap to display border, and displays the border for two more words.
9. Loop to step 1.

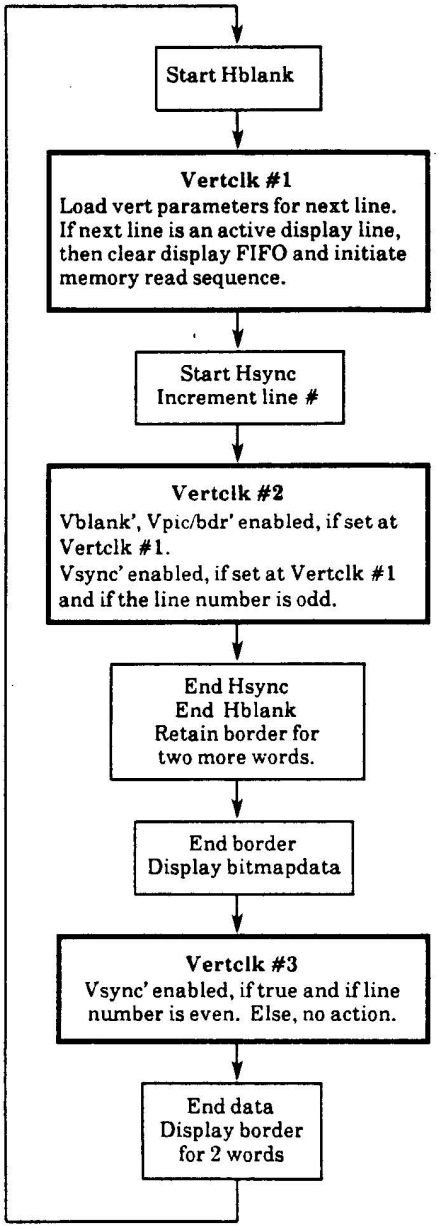


Figure 3.16. Display line control flow

Timing

Horizontal control address counters are clocked by PxlClk/16; vertical control address counters are clocked by Hsync.

Figure 3.17 illustrates control timing. In the figure, the numbers in the first line indicate a sequence in time; that is, the numbers do not correspond to a control store address. The number 0 is the first border word on the left side of the screen. The circled numbers refer to the vertical clock pulse.

Part A of the figure illustrates the case for an active display line. At clock 57, with vertical control store selected, the vertical control parameters for the line are latched. Note that Pblnk', Psync, and Ppic/bdr' are 'false' at clock 57, indicating no vertical action.

Part B illustrates the case for vertical sync and blank line. Note that at clock 57, Pblnk', Psync, and Ppic/bdr' are 'true,' indicating vertical events for the next line.

Figure 3.18 illustrates sync timing. Vertical events across the line are controlled by VertClk'. The circled number refers to the vertical clock pulse.

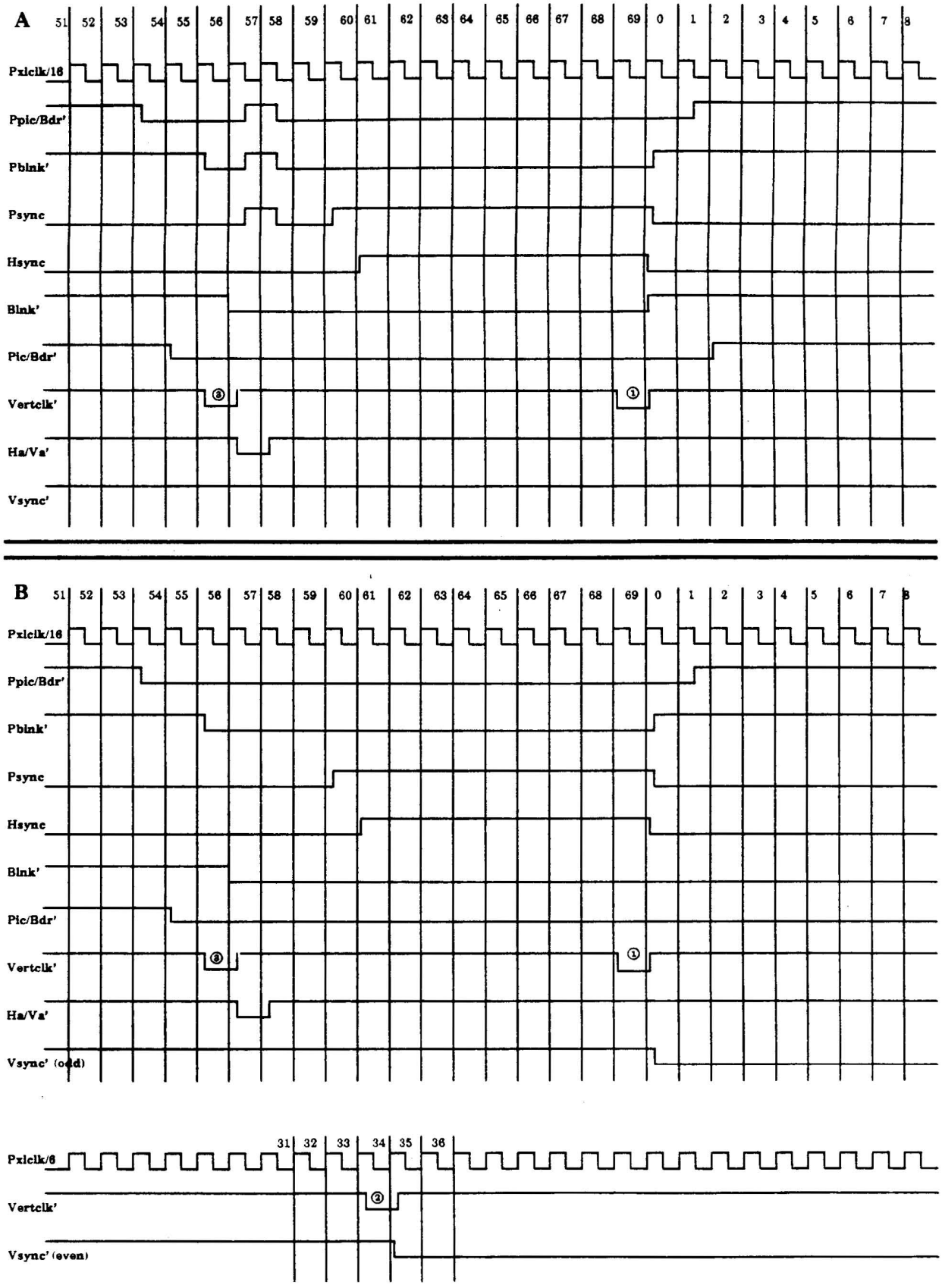


Figure 3.17. Control timing

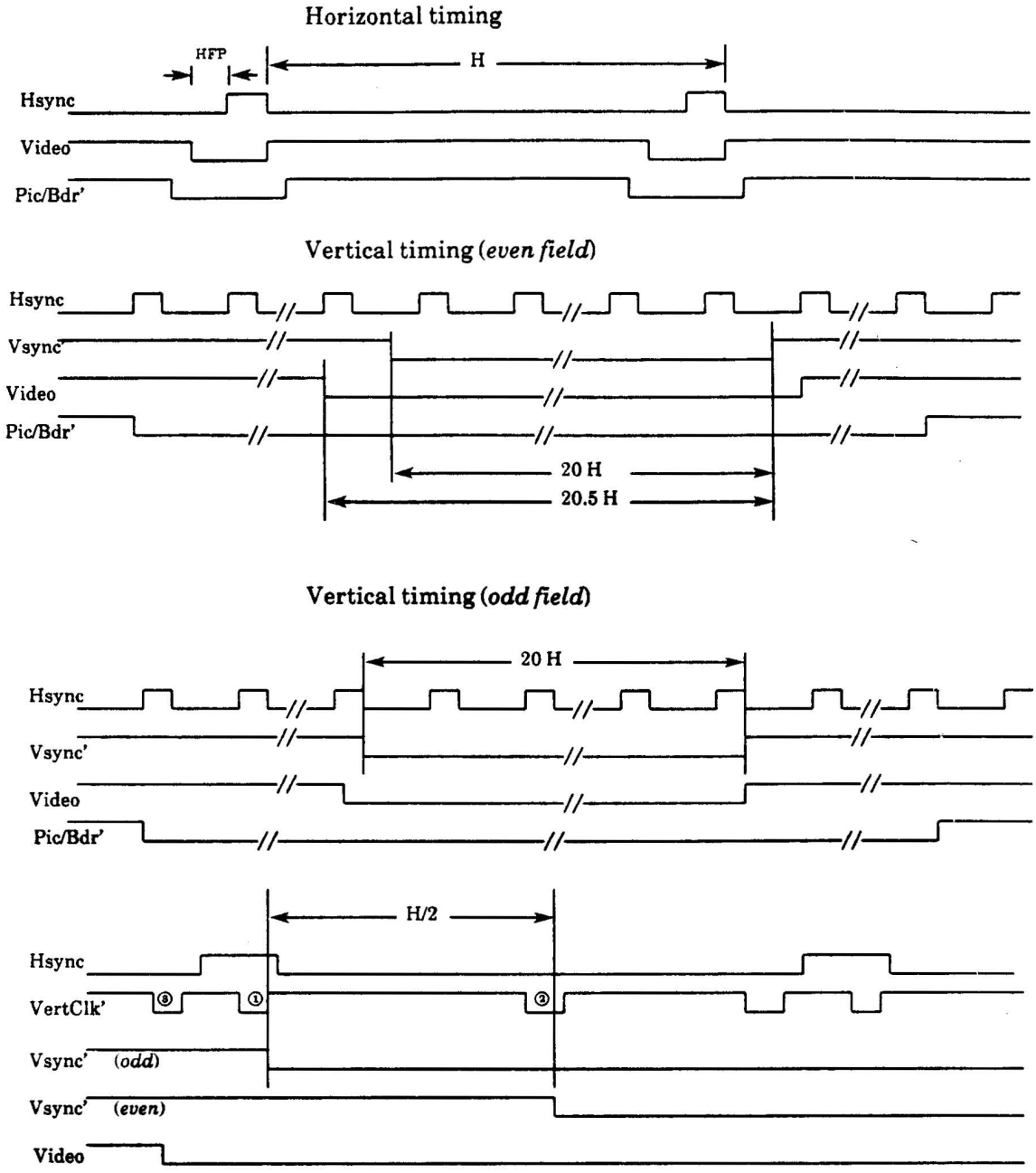


Figure 3.18. Sync timing

3.2.2.4 Display FIFO

A 64 x 16-word data FIFO buffers data between memory and the display data chip (DDC) and translates data from Intel format (LSB = bit 0 and MSB = bit 15) to Mesa format (LSB = bit 15, MSB = bit 0). The display FIFO performs bit swapping within a byte. The swap is completed at the display latches, which latch the FIFO output sent to the DDC.

3.2.3 Programmer Interface

This section describes the registers and timing for components of the display subsystem.

3.2.3.1. Vertical/Horizontal Control Store

The vertical and horizontal control store are stored in PROM. Two sets of parameters are store in each PROM; the 15-inch display and the 19-inch display parameters.

The status of XTALSEL0' determines which set of parameters is addressed by the display controller (DDC and DCC). If XTALSEL0' is a logic 1, then the 15-inch parameters are selected. If XTALSEL0' is logic 0, then the 19-inch parameters are chosen.

Figures 3.19 and 3.20 illustrate the format of the vertical and horizontal control store data.

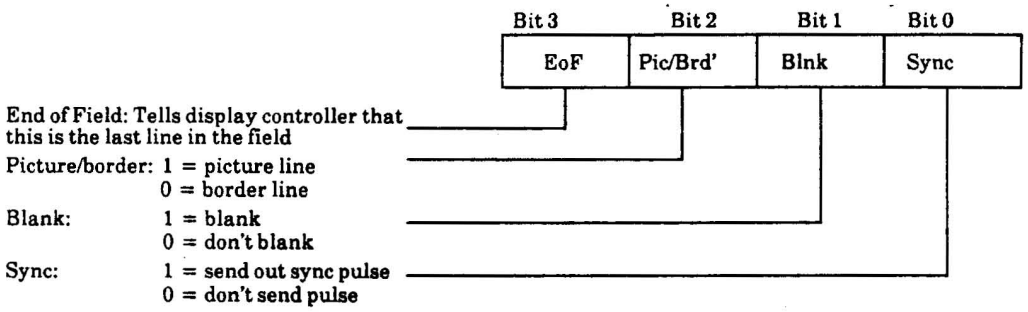


Figure 3.19. Vertical control store registers

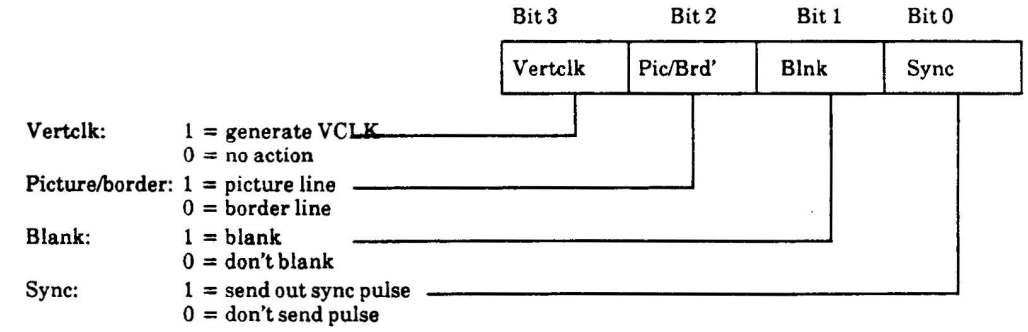


Figure 3.20. Horizontal control store registers

3.2.3.2. Display Data Chip: Registers and Timing

The display data chip contains four command registers and one status register.

The Display Control register is an 8-bit write-only register. Bits 7-4 of the register specify how the cursor and data are to be merged. Bits 3-0 enable display, and specify interlace/non-interlace, and border/bitmap. Two 8-bit, write-only border registers specify the border pattern. An 8-bit, write-only cursor word number register specifies the word number in the display line.

Figure 3.21 illustrates the write operations of the DDC control registers.

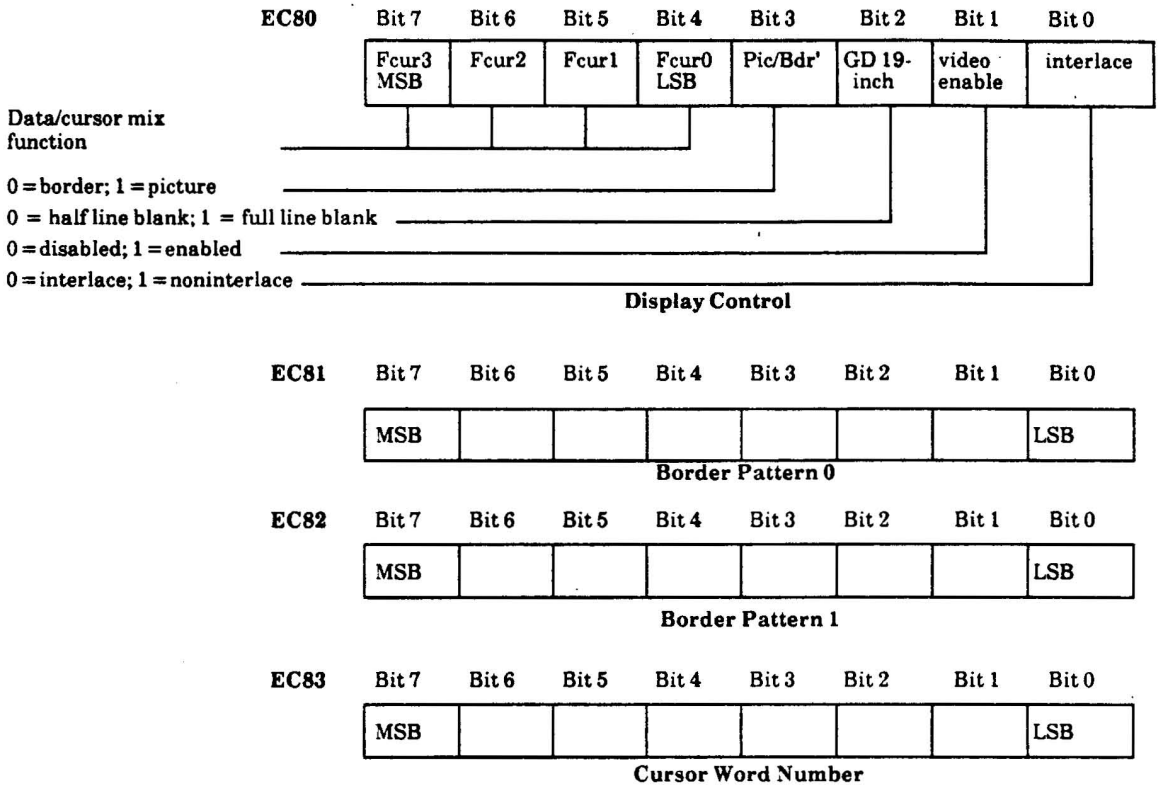


Figure 3.21. Display control registers: Write operations

The DDC status register is an 8-bit, read-only register that holds the current status of the DDC. Figure 3.22 illustrates the register; Figure 3.23 illustrates DDC timing.

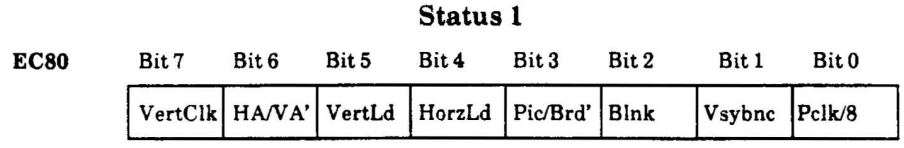
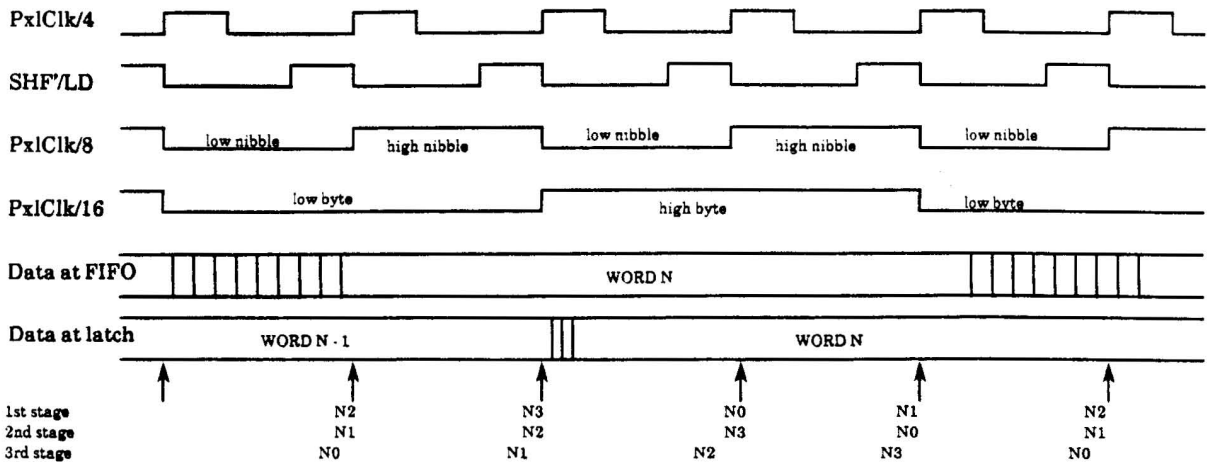


Figure 3.22. DDC status register: Read operation



1st stage is latched at mixer input; 2nd stage is latched at video register within the DDC gate array; 3rd stage is loaded into video shift register. N0, N1, N2, and N3 denote the nibbles that make up any one word.

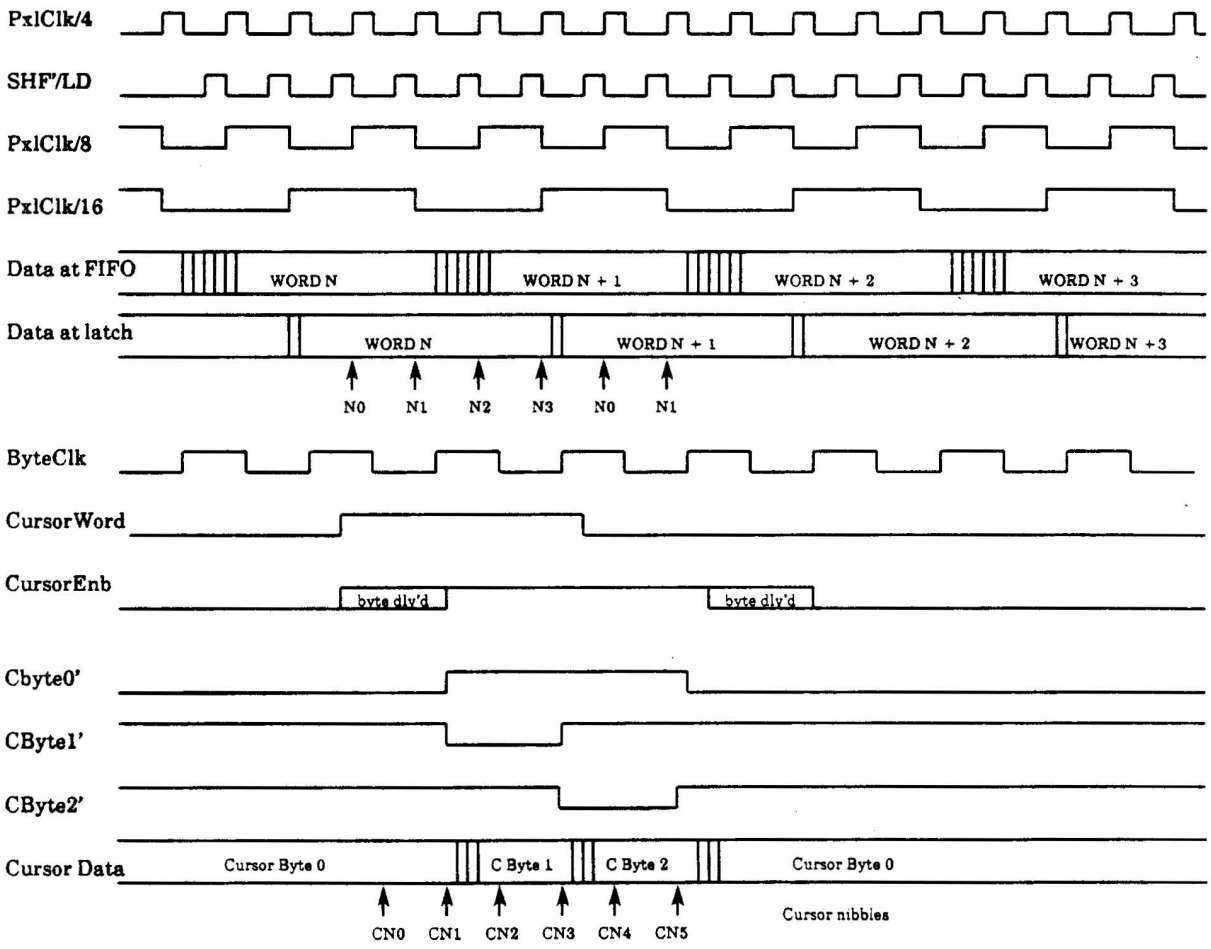


Figure 3.23. DDC timing

3.2.3.3. Display Cursor Chip: Registers

The display cursor chip contains three control registers for cursor bit offset and cursor line number and also contains a status register.

The cursor bit offset register is an 8-bit, write-only register that provides a 4-bit offset for the cursor (0-15 bit shifter). Two 8-bit, write-only registers represent the line number in the frame where the cursor is displayed. Figure 3.24 illustrates the registers.

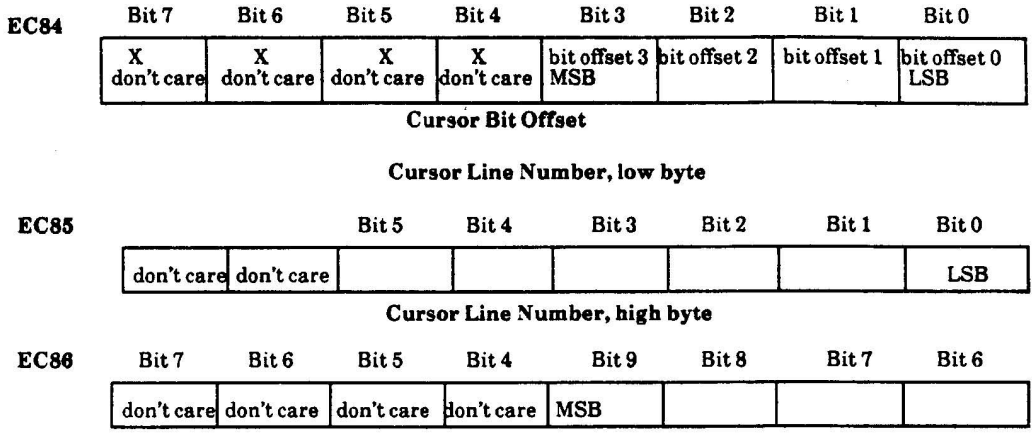


Figure 3.24. DCC control registers: Write Operations

The DCC status register is an 8-bit, read-only register that describes the current status of the DCC. Figure 3.25 illustrates the register.

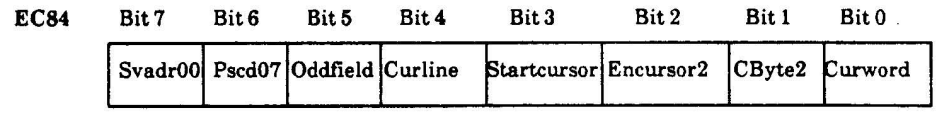


Figure 3.25. DCC status register: Read Operations

3.2.3.4. Display Memory Chip: Registers & Timing

The display memory chip contains three control registers and one status register.

The horizontal active quad word register is an 8-bit, write-only, control register that specifies the number of words to be displayed and retrieved from memory during an active display line. Memory bitmap starting address registers are 8-bit, write-only, control registers. Figure 3.26 illustrates the registers.

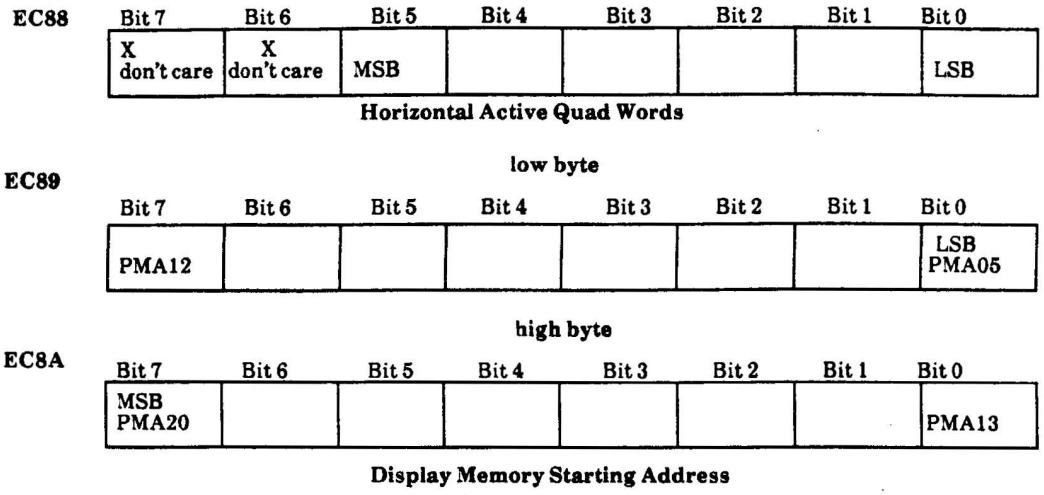


Figure 3.26. DMC control registers: Write operations

Figure 3.27 illustrates the DMC status register, which indicates the current status of the display memory chip.

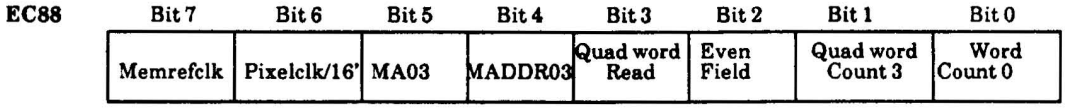


Figure 3.27. DMC status register: Read operation

Timing

Figure 3.28 illustrates DMC timing; Figure 3.29 illustrates memory access timing.

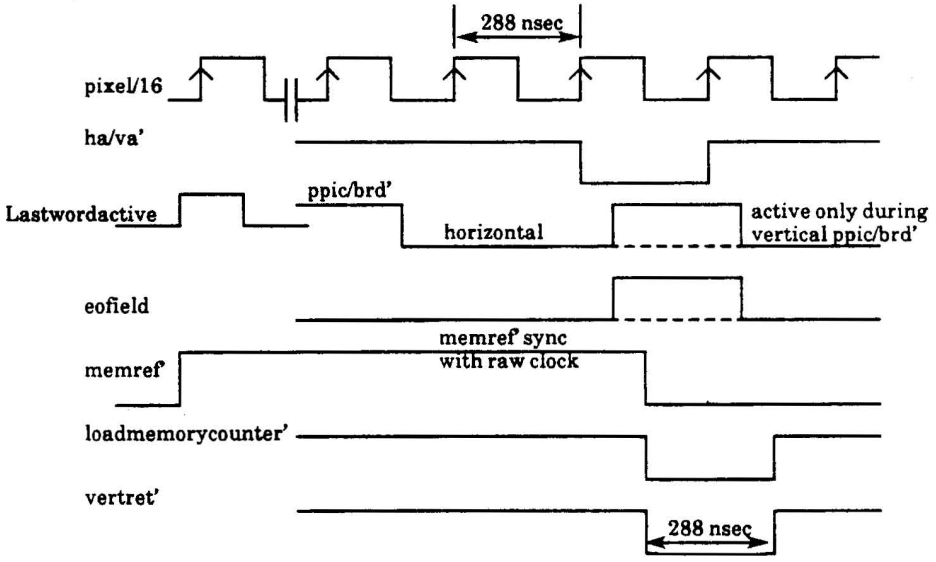


Figure 3.28. DMC timing

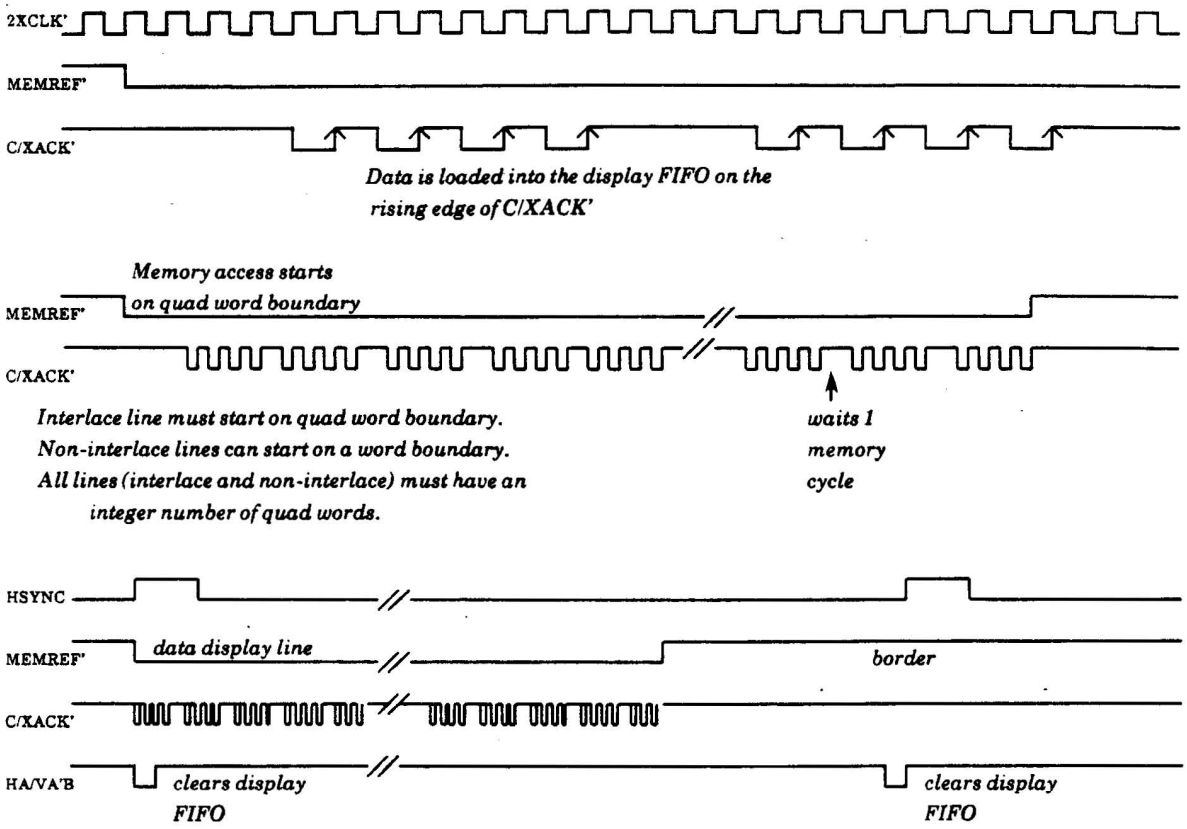


Figure 3.29. Memory access - nibble mode

3.2.3.5 Cursor

The cursor is 16 x 16 bit aligned. The positioning and bit alignment of the cursor is done entirely in hardware.

The cursor pattern is written into the cursor buffer by the IOP in intel byte format, and read from the cursor buffer by the display controller in Mesa word format. Figure 3.30 illustrates the display word format.

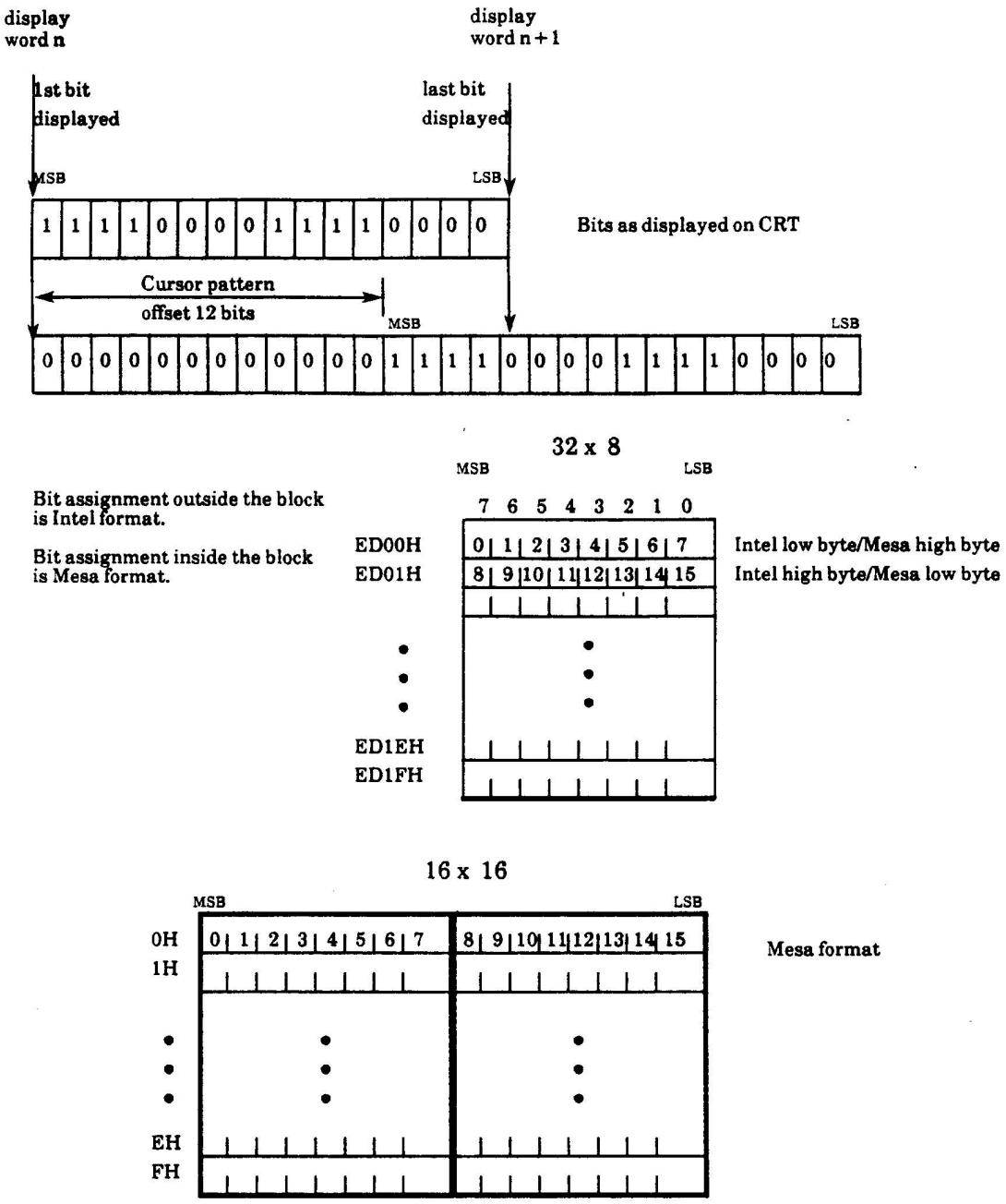


Figure 3.30. Cursor pattern

Cursor Buffer

The cursor buffer consists of four 16 x 4 RAMs that store the cursor data. These buffers are byte-written by the IOP and word-read by the DCC.

Figure 3.31 illustrates the cursor buffer registers.

ED00 - ED1F

Intel even byte

ED00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CURD.00 Mesa MSB	CURD.01	CURD.02	CURD.03	CURD.04	CURD.05	CURD.06	CURD.07

Intel odd byte

ED01

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CURD.08	CURD.09	CURD.10	CURD.11	CURD.12	CURD.13	CURD.14	CURD.15 MesaLSB

CURD.00-CURD.15 represent Mesa bits

Figure 3.31. Cursor buffer (32 x 8) registers