

DX-500

OPERATION AND MAINTENANCE MANUAL

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PROPRIETARY INFORMATION

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1.00 SCOPE OF MANUAL

This manual provides the information required to operate and maintain the DX-500 Disk Exerciser.

2.00 CAPABILITY

The DX-500 Disk Exerciser will test Wangco Series F and Series T drives, Pertec D3000 Series, Diablo Models 30 and 40, and similar drives by other manufacturers. PC adapters are required for each drive type.

2.01 DRIVE SPECIFICATIONS

Drive options accomodated by the DX-500 include:

- 1. Number of cylinders 203/406/609
- 2. Number of heads 8
- 3. Spindle speeds 1500/2400
- 4. Data densities 2000/2200/4400
- 5. Data coding NRZI/DF

3.00 FEATURES

3.01 CYLINDER ADDRESS

Eight different servo exercising modes:

- 1. Restore
- 2. Seek fixed cylinder
- 3. Seek increment
- 4. Seek random cylinder
- 5. Alternate seeks to a fixed cylinder combined with any of the above produces four additional modes.
- 6. An OFF position is provided for writing and reading without servo action.

A seek delay of 0.5 seconds may optionally be imposed between seeks. Choice of repeated seeks or a single seek with each RUN start. Nine LEDs show cylinder address. A seek error LED locks on if a seek error is detected.

3.02 DRIVE, DISK AND HEAD ADDRESS

The drive number is selected by a 4-position slide switch. The

disk and head address are manually selected or automatically sequenced.

LEDs show disk and head address.

3.03 WRITE/READ CONTROLS

The write/read control, in combination with the seek control, permits seven modes of action.

- 1. Seek only
- 2. Seek and write
- 3. Seek and read
- 4. Seek and write and read
- 5. Write without seek
- 6. Read without seek
- 7. Write and read without seek

3.04 DATA FORMATTING

Two modes of data formatting: Either each sector pulse starts a new record, or the entire track is written and read as a single record. In the sector mode, the sector interface lines are continuously monitored and compared each sector time against a sector pulse counter. A

sector error LED locks on if an error is detected.

3.05 DATA PATTERN

Four data patterns:

- 1. All ones
- 2. All zeros
- 3. Alternate ones and zeros
- 4. Scrambled data varying continuously throughout the sector and modified to provide different data for each track.

Each sector begins with a single word of track address. All read data is checked against a generated pattern.

3.06 DATA ERROR

A switch selects STOP ON ERROR or OVERRIDE. One data error LED flashes on each error, a second LED locks on with the first error. Action is stopped if an error occurs in the STOP ON ERROR position.

3.07 STATUS LEDS AND TEST POINTS

Six LEDs continuously display interface status. Ten test points provide scoping convenience.

4.00 PHYSICAL CHARACTERISTICS

Portable carrying case with cover. Operated on +5 volt power from drive, or optional +5 volt internal power. Compartment in case for I/0 cable and manual.

4.01 OUTLINE DIMENSIONS

Length 17 inches, height 10 inches, depth 5 inches, weight 6 lbs.

5.00 CONTROLS, INDICATORS, AND TEST POINTS

1. DRIVE TYPE

Selects Diablo, Pertec, Wangco type, and special.

2. DRIVE SELECT 1/2/3/4

Applies select signal to one of four I/O lines.

3. 4400/2200/2000 BPI

Selects density to match drive specification.

4. 2400 RPM/1500 RPM

Select speed to match drive.

5. 200 TPI/100 TPI

Select cylinder address capacity.

6. SECTOR/TRACK

Select data formatting.

7. WRITE DF/NRZI

Select write data coding.

8. READ DF/NRZI

Select read data coding.

9. OFFSET 0/-/+/BOTH

For margin testing drives that have margin option.

10. DATA 0/1/10/SCRAMBLE

Select data pattern for writing and for read checking.

11. STOP ON ERROR/OVERRIDE

Provides for optional stop on error.

12. OFF/REST/MAN/INC/RANDOM

Selects seek mode.

13. SEEK DELAY

Enforces delay interval between seeks.

14. CONT/SINGLE

Selects continuous or single cycle action.

15. ALT/OFF/ALTSET

ALT selects alternate mode of seek action. ALTSET loads alternate cylinder address used in MAN + ALT mode.

16. RUN/STOP

Push button START/STOP for exercising. Also clears error LEDs.

17. CLEAR

Resets cylinder address count to starting point for INC seek mode.

18. OFF/W/R/WR

Select data handling mode.

19. CYLINDER ADDRESS 511-1

Selects cylinder address for MAN and ALT modes.

20. DISK

Select disk to be exercised.

21. HEAD

Select head to be exercised.

22. SEQ/FIXED

FIXED enables HEAD and DISK select switches.

SEQ enables automatic sequencing through the two heads on each disk. SEQ also enables automatic disk sequencing in the INC and RANDOM seek mode.

23. ADDRESS LEDS

Cylinder address, head and disk LEDs show current track selected.

24. WG

LED shows when exerciser is writing.

25. RG

LED shows when exerciser is reading.

26. RUN

LED shows when exerciser is operation.

27. SEEK ERROR

LED locks on if an error is detected.

28. DATA ERROR

Two LEDs, one locks on with first data error. The second flashes on each error.

29. TEST POINTS

INDEX ---- Index pulse signal from drive.

SEC ---- Sector pulse signal from drive.

SCOM ---- High during seek time.

ADACK ---- Drive response to cylinder address strobe.

WDN ----- Data generated by exerciser (NRZI).

RDN ----- Read data compared to write data.

SYNC ---- Marks beginning of data in each sector.

RD ----- Read data as received from drive.

ERROR ---- Signals data error.

DC ----- Data clock.

30. STATUS

READY = Drive is ready for operation.

SCOM = SEEK operation completed.

INCOMPL = SEEK operation incomplete.

ILLAD = Illegal address.

WRITE

CHECK = Write check function in some drives represents malfunction

READ

ONLY = Selected platter is write protected.

6.00 OPERATING PROCEDURES

6.01 ON LINE PREPARATION

Connect the I/O cable to the disk drive using the specified adapter. Verify that pin 1 orientation at cable end and drive is correct (red line on cable is pin 1). Set the DIABLO/PERTEC/WANGCO/SPL switch to match the drive type. Turn on and load the drive. Set the DRIVE SELECT switch to match the drive number. The READY and SCOM LEDs should come on to indicate that the drive is on line.

NOTE: All drives being tested <u>must use</u> drive's terminator. If drive

terminator is not present tester will not function properly.

6.02 CONFIGURATION

Set the 2400 RPM/1500 RPM switch to match the drive speed. Set the 4400 BPI/2200 BPI/2000 BPI switch to the specified density. Set 200 TPI/100 TPI to match the cylinder address range, 200 TPI equals 406 cylinders and 100 TPI equals 203 cylinders. Set the WRITE DF/NRZI and READ DF/NRZI switch to match the data coding specified for the drive.

6.03 CYCLING OPERATION

Set SEEK ON/OFF to ON. Set the SEEK control to RANDOM. Set CONT/SINGLE on CONT. Set WRITE/READ to W/R and set ALT/OFF/ALTSET to OFF. Set STOP ON ERROR/OVERRIDE to OVERRIDE. Set the SEQ/FIXED switch to FIXED. Press the RUN/STOP button. Observe the RUN LED light to indicate that the exerciser is in operation. There will be seeks to random cylinder addresses followed by writing then reading of each address. Select the SEEK DELAY switch to slow the action. Observe the SCOM LED blink off at each seek. Observe the WG and RG LEDs flash on after each seek. Observe the CYLINDER ADDRESS LEDs display the address of each seek.

6.04 DATA VERIFY

The DATA ERROR LED should not flash during 6.03 operation, indicating that correct data is read from the track. If an error does occur, set the SEEK mode switch to MAN. There will be repeated seeks to the same cylinder address followed by writing and reading, the error flashing will stop because the data will be rewritten to the new pattern selected, however if the media is bad the error lite will continue to flash.

If the READ DF/NRZI coding selection of the exerciser is mismatched to the drive configuration, the mismatch may show as data error. However some mismatch combinations will not show data error but will instead be indicated by the failure of the RG or WG LED to light.

6.05 TRACK SELECT

With RUN continuing, the SEEK switch at MAN and the WRITE/READ switch at W/R, put each CYLINDER ADDRESS switch up one at a time and observe that the LED above it light to show that the drive has moved to the address selected.

Also, set up the DISK and HEAD switches and observe their LEDs light according to the switch position. See Table 1 for DISK and HEAD selection. Now put the SEQ/FIXED switch up and note that the HEAD LED flickers showing that both tracks are sequentially written and read after each seek.

TABLE #1

20 MEG 10 MEG DISK 1 DISK 2 DISK 1 DISK 2 UP UP DWN DWN Removable DWN DWN DWN DWN UP DWN UP UP HEAD SELECT UP FOR UPPER HEAD / DOWN FOR LOWER HEAD

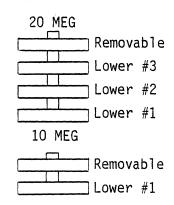


Table #1 is for PERTEC and WANGCO drives. Other drives check specific drive manual.

6.06 INC MODE

Lower #1

Lower #2

Lower #3

Press RUN/STOP to stop run. Set the SEEK switch to INC, press CLEAR, then RUN/STOP to start run. Observe that the CYLINDER ADDRESS LEDs show increment counting. When the count reaches the maximum value (202 or 405), it will automatically return to zero. If the SEQ/FIXED switch is still on SEQ, the disk LED will alternate for each pass and

the entire recording media will be tested. All tracks will be written and read.

After a complete write pass the WRITE/READ switch may be changed to READ so that read-only passes can be continued. Once the complete media is written with the same data selection, then it may be read in any seek mode and should not show data error.

6.07 ALT SEEK MODE

Set the CYLINDER ADDRESS switches to a first address and move the ALT/OFF switch down and back up to ALT. Then change the CYLINDER ADDRESS switches to a second address. Put SEEK CONTROL at MANUAL, and start run. Observe that there are alternate seeks to the first and second addresses.

Change the SEEK control to INC. Now there will be alternate seeks between the CYLINDER ADDRESS switch address and the incrementing address. The ALT variation may be used with all the seek modes.

7.00 CIRCUIT MNEMONICS

- A8:0 \pm Outputs of cylinder address register. Source of cylinder address in the INC and RANDOM seek modes.
- ADACK Acknowledge pulse emitted by drive in response to CAS pulse from exerciser.

AC+ Outputs of a FF toggled in the ALT seek mode. Selects the ALT address on alternate seeks.

ALT Low when ALT/OFF/ALTSET switch is up.

 $\overline{\text{AU3:0}}$ Used only on Pertec drives. Busy seeking signals are matched with unit select signals to develop replacements for $\overline{\text{ADACK}}$ and $\overline{\text{SCOM}}$.

4400 BPI Low when density switch is at 4400.

2000 BPI Low when density switch is at 2000.

CA8:0 Cylinder address signals sent by exerciser to drive.

CAS Cylinder address strobe sent to drive.

CAS \pm Clocked on for each seek to generate $\overline{\text{CAS}}$ strobe. Reset by $\overline{\text{ADACK}}$.

CI8:0 Cylinder address of last seek.

CLEAR Low when CLEAR button is pressed. Resets cylinder address register.

Data clock received from drive.

DS Disk select signal sent to drive.

DS \pm Internal signals corresponding to $\overline{\rm DS}$. DS- drives DISK LED. DS+ and DS- are combined to develop disk change detect pulse used to block sector error compare during change.

DRDY+ A combined ready signal, necessary to allow seek and write/read action.

DT+ True with the beginning of data in each sector.

DIAB Low when Diablo drive is selected.

ED+ Erase delay. A 30 microsecond wide pulse which follows each sector pulse in SECTOR format and follows the index pulse only in TRACK format.

 $\overline{\text{END}}$ True at the end of each seek pass in the INC seek mode. Resets the address register in both the INC and RANDOM seek modes.

Erase gate signal sent to drive.

ERR+ Data error signal.

ERASE+ Lags WRITE+ signal by ED time.

HS Head select signal sent to drive.

INDEX Index pulse from drive.

IND<u>+</u>
Begins at INDEX pulse and ends at first sector pulse in SECTOR format. Begins and ends with INDEX pulse in TRACK format.

IND1 \pm A 10 microsecond wide pulse which follows IND \pm .

IND2- Occurs with alternate IND1- pulses when reading or writing in the head SEQ mode. Otherwise occurs with every IND1- pulse.

INC Low when INC seek mode is selected.

ILLAD Illegal address signal from drive. Results when a seek is attempted to an address greater than the maximum.

2.88 MHZ Three basic crystal oscillator generated clocks which are 6.25 MHZ 10.0 MHZ the sources of five different data writing clocks.

MAL Malfunction status signal from the drive.

MAN Low when manual seek mode is selected.

PT+ Preamble timing pulse 100 microseconds duration follows each sector pulse in the SECTOR mode and follows index pulse in the TRACK mode.

PERT Low when Pertec drive is selected.

RAND Low when RANDOM seek mode is selected.

REST Low when RESTORE seek mode is selected.

READ+ True when the drive is reading.

RG Read gate signal sent to drive.

RD Read data received from drive.

RD+ True high NRZI read data.

RESET Low when RUN/STOP switch is depressed.

RWC+ A combined read and write clock.

RO Read only status signal from drive.

RDY Low when drive is ready for action.

RDY+ True high follower of $\overline{\text{RDY}}$.

RUN+ True when exerciser is operating.

R Low when read mode is selected.

SEC Sector pulses sent by the drive.

SCOM High when drive is seeking.

SINC Seek incomplete signal from drive.

STOP+ Terminates run.

ST256:1 Outputs of cylinder address switches.

SD+ Outputs of seek delay one shot.

SOFF Low when non-seek mode is selected.

SECTOR+ True when sector format mode is selected.

SEQ+ High when head sequence mode is selected.

SA6:0 Sector address signals sent by drive.

200 TPI+ True when 200 tracks per inch configuration is selected.

US3:0 Unit select signals sent to drive by select switch.

WC Write clock.

WD Write data signal sent to drive.

WD+ NRZI write data.

WRITE+ True when drive in writing.

W Low when write mode is selected.

W/R Low when write/read mode is selected.

WRF+ Write read finished. Cleared on a seek command if a write or a read operation is needed. True again when operation is complete.

WG Write gate signal sent to drive.

XC+ Crystal frequency scaled to write clock rate.

2XC Double XC frequency.

8.00 CIRCUIT DESCRIPTION

8.01 SEEK OPERATION

Cylinder address signals $\overline{\text{CA8:0}}$ are sent to the drive at all times. Tristate drivers multiplex these signals from three sources:

The cylinder address switches ST256:1

The SETALT register

The address counter A8:0+

The CA8:0 signals need not be held steady while the drive is performing read, write or seek operations. The drive samples the $\overline{\text{CA8:0}}$ lines only when the $\overline{\text{CAS}}$ strobe is sent. The $\overline{\text{CAS}}$ strobe also initiates seek action.

The condition for generating \overline{CAS} to start the seek action are:

- 1. The drive must be selected and ready.
- 2. SCOM must be low so that no seek is in process.
- 3. RUN+ must be true.
- 4. The seek mode switch must be ON.
- 5. WRF+ must be true so that reading or writing is not in process.
- 6. $SD\underline{+}$ seek delay must have timed out since the previous seek.

When all of these conditions are met the first rising edge of 0.4 MHZ continuous clock on CAS+.

CAS+ rise will trigger a new SD+ delay. CAS- becomes $\overline{\text{CAS}}$ sent to the drive. The drive starts seek action, sends an $\overline{\text{ADACK}}$ pulse and allows $\overline{\text{SCOM}}$ to rise if the seek is to a new cylinder.

CAS- also resets WRF+ if the WRITE/READ select is not set to OFF.

As long as RUN+ is true the exerciser sends a stream of $\overline{\text{CAS}}$ pulses to the drive. If the SEEK select is set to REST the $\overline{\text{CAS}}$ pulses also become $\overline{\text{REST}}$ pulses which cause repeated restore action in the drive.

In the MAN position the $\overline{\text{CAS}}$ pulse strobes $\overline{\text{CA8:0}}$ address signals taken from the cylinder address switches. These switches may be moved while in RUN and the LED indicators above each switch will show that the drive has followed the switch address.

Set the SEEK selector to INC. Now the $\overline{\text{CA8:0}}$ signals come from the A8:0+ address counter outputs. In the INC mode the counter is incremented by the trailing edge of CAS- after the seek is initialed. Press the CLEAR button and the counter is reset to zero. When the count reaches one beyond the maximum, END+ becomes true. END- resets the counter so the next $\overline{\text{CAS}}$ after the maximum is to address zero. The CAS- starting this seek also resets END+.

When the RAND seek mode is selected the cylinder address counter is high speed counted by a 0.4 MHZ clock between seeks to generate a random address.

8.02 HEAD AND DISK ADDRESSING

The head and disk selection within a drive is controlled through the $\overline{\rm HS}$ and $\overline{\rm DS}$ lines. Low $\overline{\rm HS}$ and $\overline{\rm DS}$ signals select upper head and upper disk and correspond to lighted HEAD and DISK LEDs. The head and disk selection responds instantaneously to the signal level, not waiting for the $\overline{\rm CAS}$ strobe.

In the FIXED position of the SEQ/FIXED switch the $\overline{\rm HS}$ and $\overline{\rm DS}$ signals are directly controlled by the HEAD and DISK switch positions.

In the SEQ position each read and write is for two revolutions. $\overline{\rm HS}$ is toggled so that each head is read or written for one of the two revolutions.

In the INC seek mode $\overline{\text{DS}}$ is also toggled at the end of each cylinder address pass.

8.03 SECTOR FORMATTING

In the SECTOR mode the $\overline{\text{INDEX}}$ pulse sets IND+, then the trailing edge of the next $\overline{\text{SEC}}$ pulse clocks IND+ off. Sector zero follows IND+. IND1+ is a 10 MS wide pulse which follows the trailing edge of IND+. IND1-becomes IND2- whose trailing edge clocks WRITE+ and READ+ on and off.

The $\overline{\text{WG}}$ write gate signal to the drive is WRITE- redriven and is continuous for a complete revolution. The $\overline{\text{RG}}$ read gate signal to the drive is READ- redriven but is inhibited during ED+ time. Erase delay ED+ is a 50 MS wide pulse which follows each sector pulse, thus $\overline{\text{RG}}$ appears for a full revolution but is interrupted at the beginning of each sector.

PT+ preamble time is 100 MS wide when writing and 80 MS wide when reading. PT+ begins at each sector pulse. All-zero preambles are written during PT+ time. When reading, PT is used as an inhibit to block premature recognition of the data beginning.

DT+ data time on a write revolution begins with the first data clock edge after PT+ and continues to the beginning of the next PT+ pulse. After the preamble zeros, data begins at DT+ rise with two ones, followed by eleven bits of track address and then by three zeros. Then follows the data pattern selected by the four-position DATA switch which is continued to the end of the sector.

Erase+ and \overline{EG} appear with \overline{WG} but lag \overline{WG} by ED time.

DT+ on a read revolution begins when the first RD+ one is detected after PT+ time and continues to the next PT+ beginning. Write-to-read lag built into the drive avoids receiving read data beyond valid write data at the end of the sector.

8.04 TRACK FORMAT

In the TRACK format mode the $\overline{\text{SEC}}$ line is held low. ED+, PT+ and IND1+ all occur at the $\overline{\text{INDEX}}$ pulse time only. IND+ appears for the duration of $\overline{\text{INDEX}}$. A single address word is composed after PT time, then the remainder of the track is filled with the selected data pattern.

8.05 DATA PATTERNS

All zeros, all ones, one/zeros or a scrambled data pattern may be selected. The pattern selected appears at WD+ after the 16 bit address word and when writing is sent to the drive as $\overline{\text{WD}}$. When reading, the same pattern is generated for comparison with the $\overline{\text{RD}}$ read data received from the drive.

8.06 DATA ERRORS

When reading, the generated data pattern is compared bit by bit with data read from the track and any mismatch is signaled as on error by the rise of ERR+. If ERR+ rises it will remain high until the end of the sector where it is reset by the rise of $\overline{\text{RG}}$. ERR- drives a flashing error LED.

DATA ERROR and SEEK ERROR are two latching LEDs. SEEK ERROR will light if ERR+ rises during the 16 bit address word time. DATA ERROR will light if ERR+ rises after the address word. Both LEDs remain latched until cleared by depressing RUN/STOP.

The rise of ERR+ will force a stop if the STOP ON ERROR switch is up.

8.07 CLOCKS

Three crystal oscillators run continuously. Scalers and a multiplexer provide at 2XC one of five frequencies; 10MHZ, 5 MHZ, 6.25 MHZ, 3.125 MHZ and 2.88 MHZ. The multiplexer selection is determined by the positions of the RPM and BPI switches. 2XC is a double bit rate clock necessary for writing DF coded data.

The writing of NRZI coded data uses the \overline{DC} clock supplied by the drive. When reading, either NRZI or DF, the \overline{DC} clock from the drive is also the only data clock required.

One of the crystal oscillators is further scaled to produce a 0.8 MHZ clock that is used to clock the seek strobe and also to generate random cylinder addresses.

8.08 SECTOR ERROR

The drive supplies seven lines $\overline{SA6:0}$ of sector count information. The exerciser compares these seven lines with the outputs of a seven - stage counter counting sector pulses. Mismatch is indicated by latching the SECTOR ERROR LED.

On a disk select change the error sensing is disabled until the first index pulse after the change.

For TRACK formatting the sector error circuit is continuously disabled.

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SIGNAL GOES THRU 2 DIODES .001 CAP FILTER.

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P/N 100201 : 50 PIN D-SHELL,AMP P/N 205740-1 P/N 100202 : 50 PIN D-SHELL, AMP P/N 205740-1

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6. P/N 100133 : 50 PIN CARD EDGE,3M P/N 3415-0001 7. P/N 100220 : 50 PIN SOCKET,3M P/N 3425-3000

4. P/N 100134 : 50 PIN SOCKET, WINCHESTER P/N MRAC 50S 5. P/N 100192: 50 PIN SOCKET, WINCHESTER MRAC 50S

100134 : 42 PIN SOCKET, WINCHESTER P/N MRAC 428

ತಿ. P/N P/N 100083 : 50 PIN CARD EDGE,3M P/N 3415-0001 100214 : PCB

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(SELF POWER OPTION)

