WANG

6102

VS-100 COMPUTER SYSTEM

Customer Engineering
Product Maintenance Manual

741-0871

PREFACE

Fourth Edition (August 1984)

This edition of the VS-100 Computer System manual obsoletes document(s) no. 729-0871, 729-0871-A, and 729-0871-A1. The material in this document may only be used for the purpose stated in the Preface. Updates and/or changes to this document will be published as Publications Update Bulletins (PUB's) or subsequent editions.

CUSTOMER ENGINEERING

PUBLICATION UPDATE BULLETIN

DATE: 10/01/84

This PUB: 741-0871-1

Class Code: 6102

Base Document: 741-0871

Previous Notice(s):

REASON FOR CHANGE:

To correct errors in the VS-100 Product Maintenance Manual, 741-0871, for the 22V88/22V88 Very Large Disk Adapter switch settings, and in the procedure for determining the PDA of the IPL device.

INSTRUCTIONS:

Remove pages and insert attached pages as follows:

	REMOVE	INSERT
1.	5-1/2	5-1/2
2.	7-25/26	7-25/26
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To add 22V36 Async Device Controller description to manual.

INSTRUCTIONS:

Remove pages and insert attached pages as follows:

	REMOVE	INSERT
1.	v	v
2.		K-1 thru K-19
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This PUB provides information for the installation of the new VS-100 I/O panel connector plates.

INSTRUCTIONS:

Remove pages and insert attached pages as follows:

	REMOVE	INSERT
1.	v/vi	v/vi
2.	3-27/3-28	3-27/3-28
3.	3-29/3-30	3-29/3-30
4.	3-31/3-32	3-31/3-32
5.		3-32A
6.	B-11/B-12	B-11/B-12
7.	B-13	B-13
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This PUB adds Appendix L, a description of the CDC Virtual Machine Operating System, to the VS-100 Product Maintenance Manual.

INSTRUCTIONS:

Remove pages and insert attached pages as follows:

	REMOVE	INSERT
1.	v/vi Nothing	v/vi Appendix L
2.		
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REASON FOR CHANGE:

This PUB adds Appendix M (a description of the 4 Meg Main Memory Board), and Appendix N (a description of the 32 Port Serial Controller Board), to the VS-100 Product Maintenance Manual.

INSTRUCTIONS:

Remove and insert attached pages and/or microfiche as follows:

	REMOVE PAGES	INSERT PAGES
1.	v/vi	v/vi
2.	Nothing	Appendix M
3.	Nothing	Appendix N
4.		
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1.	1	1
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REASON FOR CHANGE:

This PUB provides references to the appropriate product maintenance manuals for installation and interconnection of the FiberWay Active Port Assembly.

INSTRUCTIONS:

Remove and insert attached pages and/or microfiche as follows:

	REMOVE PAGES	INSERT PAGES
1.	iii/iv	iii/iv
2.	3-27/28	3-27/28/28a
3.		
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1.	1	1
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VS-100 MAINTENANCE MANUAL
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INTRO-DUCTION

CHAPTER 1
INTRODUCTION

1.1 PURPOSE

This manual contains information necessary to install and maintain the VS-100 CPU (WLI #191-0010-16). Additional information will be provided as it becomes available, either as update/revisions of this manual or as PSN (Product Service Notice) documents.

1.2 SCOPE

This manual contains introductory information pertaining to the VS-100 system, and its installation and maintenance. This information is divided into eight chapters, as follows:

Chapter 1: "Introduction," provides a general outline of the manual and gives a brief description of the VS-100 and associated peripherals.

Chapter 2: "Theory of Operation," provides block-diagram level theory discussion for the VS-100 CPU and Mainframe components.

Chapter 3: "Unpacking, Inspection, and Installation," gives guidelines necessary to ensure that the installation site conforms to specific requirements of the VS-100 system; provides procedures for unpacking and inspecting the VS-100 Mainframe; and provides instructions for initial set-up and operation of the VS-100, together with associated program-loading and operation-confirmation procedures.

Chapter 4: "Switches, Controls, and Indicators," identifies all VS-100 Mainframe controls and indicators, including a functional description of each, together with standby settings and operating procedures.

Chapter 5: "Initial Program Loading And SYSGEN," has been deleted and replaced with a list of reference materials to be used when SYSGENing the VS-100.

Chapter 6: "Preventive Maintenance and Adjustments," gives guidelines and schedules for necessary preventive maintenance routines. Also contains reference data and procedures for required adjustments and a description of the 'System Log Book', required at every VS-100 installation site. Included in this chapter is a list of tools required for proper repair and maintenance of the VS-100 System.

Chapter 7: "Removal/Replacement," contains procedures pertaining to disassembly, repair, and replacement of system components that are field-replaceable.

Chapter 8: "Diagnostics," identifies the available offline and online diagnostic test programs and gives guidelines for their use. Also provides guidelines for isolating fault locations to field-replaceable or repairable components.

In addition, appendices at the rear of the manual provide the CE with a ready reference for necessary information. These appendices include a detailed BOM, a mnemonics dictionary, a listing of assorted reference material, and a part number cross-reference list of all available VS-100 devices.

1.3 RELATED PUBLICATIONS

For a list of all categories that contain information pertaining to the VS-100 System and related equipment, refer to the front of the manual. Refer to Appendix G for a list of related software documents pulished by Corporate Publications.

1.4 SYSTEM DESCRIPTION

The Wang VS-100 computer system is a high-performance data processor combining the programming flexibility of Virtual Storage with the speed of a 'Cache' memory. The VS-100 supports interactive, multiuser operations in a general-purpose computer environment and offers programming capability in BASIC, COBOL, FORTRAN, PL/1, and RPG II languages. The VS-100 also supports Assembler and Procedure languages, allowing operational sequences to be performed without user interaction.

Designed to serve as a complete commercial data processing system, the standard VS-100 system consists of a CP4 processor with from 512 kilobytes to 2 megabytes of main memory, 30 megabytes to 4.6 gigabytes of on-line storage, two to 128 (projected) workstations (including the Archiver Workstation), from one to 32 printers, and telecommunications interface capabilities ranging from a single "remote" terminal to full-protocol compatibility with a larger host computer. The VS-100 supports all SERIAL VS peripheral devices; parallel printers and workstations are NOT supported on the VS-100.

The VS-100 provides an expanded and improved computer architecture in comparison with the VS 60/80 system. Based on a new and faster CP4 processor, this architecture incorporates three new major components: a separate cache memory, a 64-bit data bus between main memory and other major processor components, and a 32-bit CP data bus. Together these new features provide a major improvement in total System performance.

The following paragraphs provide general descriptions of the major components that make up the VS-100 Mainframe. For a more detailed explanation of the VS-100 CPU, refer to Chapter 2, "Theory of Operation." Refer to the appendices for a list of related VS documents.

1.4.1 CENTRAL PROCESSOR

Housed in a compact cabinet with the main memory and optional IOPs, the CP4 central processor (CP) is the heart of the VS-100. It consists of a 210-7600 A-Bus card and a 210-7601 B-Bus card. The CP4 processor is a faster, more sophisticated version of the 8300 CP used in the VS 60/80. It supports

the same instruction set as the 8300, with the exception of certain privileged instructions related to address translation.

The VS-100 CP supports binary, packed-decimal, and floating-point arithmetic. Included in the CP are sixteen 32-bit general-purpose registers and four 64-bit floating-point registers. As in the VS 60/80, the machine instruction set is compatible with the IBM 370 instruction set.

The following features of the CP4 are not found in the 8300 They provide the CP4 processor with much of its expanded processing power.

1. 32-Bit CPU Architecture--ALU operations in the CPU use 32-bit register operands. The CP also has a 32-bit data path to main memory.
2. Fast Cycle Time--Processing time in the CP4 is approximately 160 nanoseconds/micro-instruction.
3. Overlapped Macro-Instruction Decoding--The use of a dedicated, buffered Memory Address Register (MAR0) allows the simultaneous processing of several different macro-instructions.
4. Buffered Operand Access--Allows the 32-bit ALU path to be used in important storage-to-storage macro-instructions (for example, MOVE, COMPARE).
5. Hardware Multiplication and Division Support--Hardware within the CPU supports the multiplication of two 16-bit operands to form a 32-bit result within two instruction cycles (320 nsecs). This feature allows floating-point fractional and fixed-point multiplication, and the processing of array-oriented macro-instructions. An efficient non-restoring binary division operation is provided by two micro-instructions, ASH and ASL.

1.4.2 CONTROL MEMORY

Control Memory (CM) in the VS-100 is based on 4Kx1-bit loadable RAM chips located on a 210-7602 Control Memory card. To load operational or diagnostic microcode into CM, a minidiskette drive is provided on the front of the VS-100 chassis. A loadable CM allows for functional CP expansion, CP microcode updates using a floppy diskette instead of replacing expensive PROMs, and the use of loadable CPU micro-diagnostics.

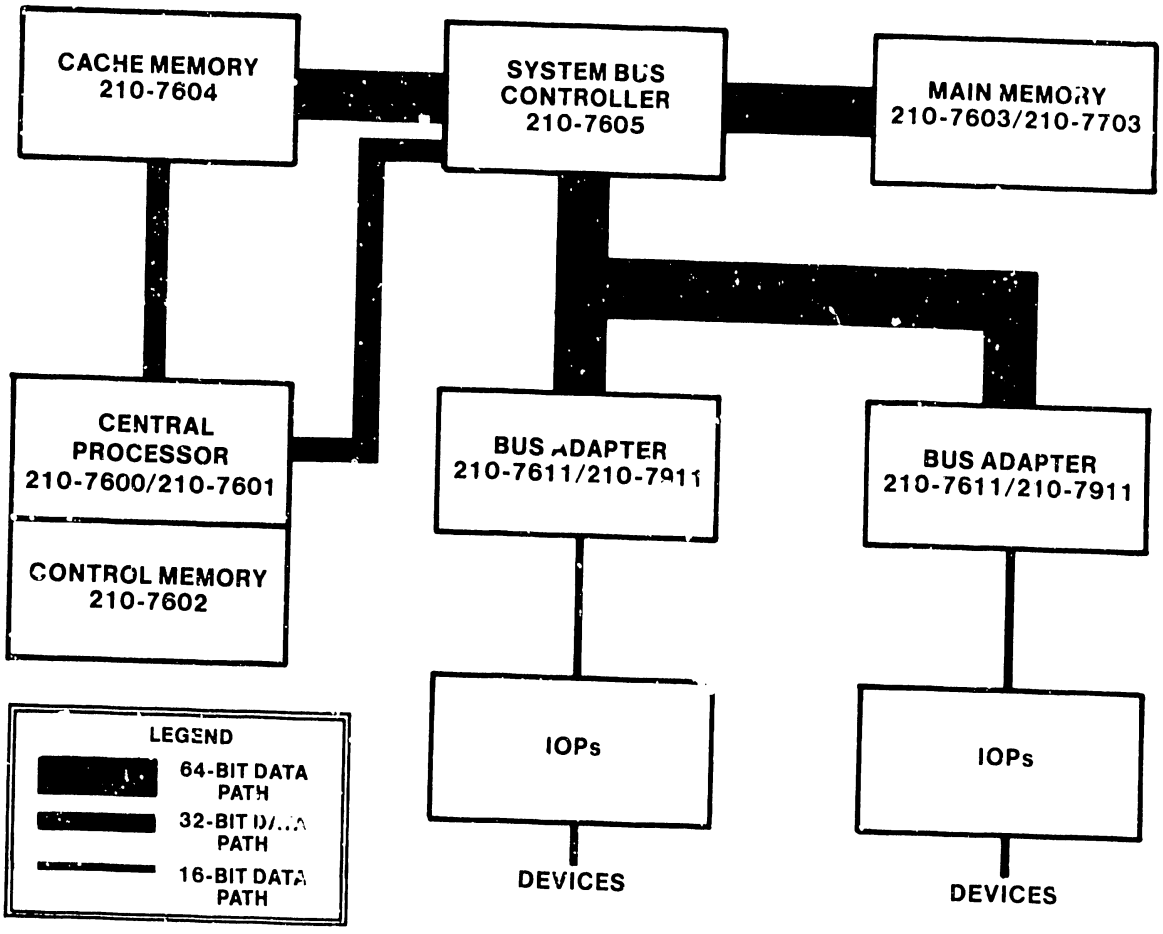


FIGURE 1-1 VS-100 CENTRAL PROCESSING UNIT ARCHITECTURE

Control Memory in the VS-100 is 8-Kbytes in size. A 1K PROM located on the minidiskette controller board contains the bootstrap program necessary to load the operational or diagnostic microcode into Control Memory.

1.4.3 CACHE MEMORY

A new feature added to the VS-100 is a 32-Kbyte block of high-speed (80 nsec) local memory called the 'Cache.' The cache function is transparent to the user, 'cached' or concealed within the depths of the CPU. Only the apparent increase in main memory access speed is visible to the user. With this feature, the CP is able to access needed data without initiating a full Main Memory read cycle. If the necessary information is found in Cache, a considerable savings in processing time is achieved (on the order of 480 nsecs). In the VS-100, cache memory is located on a 210-7604 Cache Memory card.

Cache memory is a buffer between the CP and main memory. Its main function is to improve memory transfer rate by providing high speed access to needed data. It accomplishes this by storing a copy of the most recently used subset of main memory. When the CP does a memory read, it first references the cache. If the needed data is found here, a cache 'hit' occurs and no main memory cycle is initiated. If the required data is not found in cache, a cache 'miss' occurs and a main memory cycle is initiated. The data read from memory is then gated to both the CP and the cache, keeping the cache contents current with Main Memory.

Cache memory operates on the 'locality of reference' concept, which is based on two assumptions: once a location in memory is referenced, it is often referenced again within a short period of time; and once a location is referenced, a nearby location will also be referenced. These assumptions hold true for the most part because, in programming, commonly used variables are usually located near each other and much use is made of program loops and common subroutines. The use of sequential instruction indexing and linear data arrays also play a part in the successful incoporation of a cache memory. For a detailed look at the cache and its operation, refer to Chapter 2, Theory of Operation.

1.4.4 MAIN MEMORY

The VS-100 can contain from two to eight 210-7603 (7703 in later models) Main Memory cards. Memory can range in size from 512 Kbytes (two cards) to a maximum of 2 Mbytes (eight cards) with memory size increasing in 256-Kbyte increments through the use of half-loaded boards. Each MM card can contain a maximum of 256 Kbytes of data. Memory cards are loaded into the VS-100 in pairs to accomodate the 64-bit data path employed in memory operations.

1.4.5 SYSTEM BUS CONTROLLER

Acting as the 'traffic cop' of the VS-100 CPU, the System Bus Controller (SBC) controls the routing of data between the CP, the Bus Adapters (BA), and Main Memory. The SBC (210-7605) is also responsible for generating parity on MM writes and correcting single bit errors on MM reads. Other features of the SBC include Error Logging, Read Modify Writes and single byte CP reads, and the use of an External Condition Register to select and record events occurring outside the CP.

1.4.6 BUS ADAPTER

The Bus Adapter (BA) is the interface between the VS-100 CPU and up to eight IOPs and attached peripheral devices. The BA (210-7611/7911) also provides data buffering and routing between the 16-bit IOP data path and the 64-bit Main Memory (MM) data path. Because the IOPs use a 16-bit path and MM uses a 64-bit path, the BA must put data going from the IOP to MM into 64-bit blocks for transfer to MM. It must also perform the reverse function on data going from MM to an IOP. A maximum of two BAs can be installed on the VS-100, allowing the CPU to interface with a maximum of 16 IOPs. With the 210-7611 BA, however, only one disk IOP can be installed on the associated I/O motherboard. With the introduction of the 210-7911 BA, two disk IOPs can be installed in each I/O motherboard.

1.5 CPU MOTHERBOARD

The Central Processor Motherboard (210-7608) contains all CPU logic circuit cards, the main memory cards, and associated bus control logic cards.

All applicable IOP's (Input/Output Processors) are mounted on associated I/O Motherboards (210-7609). All circuit cards installed on the VS-100 CP Motherboard, along with a brief description of each card, follows:

1. 210-7600 "A"-Bus (CP #1)--Contains all A-bus registers, status registers, branch decision logic, multiplier, and the real time clock.
2. 210-7601 "B"-Bus (CP #2)--Contains all B-bus registers, Translation RAM, binary ALU, and the decimal ALU.
3. 210-7602 Control Memory--Contains micro-instruction storage, insruction counter, trap handling logic, and System clock.
4. 210-7603 256K Main Memory Board (early version)/210-7703 256K Main Memory Board (later version)--Used for storage of software instructions and data.
5. 210-7604 Cache Memory--Contains memory sequencing controls, cache memory and control logic, and buffers for all read data.
6. 210-7605 System Bus Control--Controls all Read/Write data to/from Main Memory, 'ECC' generation, correction logic, and error checking. The SBC also contains the Bus Transaction Log (BTL) and the External Condition Register (ECR).
7. 210-7611 Bus Adapter (early version)/210-7911 Bus Adapter (later version)--Contains the logic necessary to interface up to eight IOPs with the SBC.

1.5.1 I/O MOTHERBOARD

Located next to the CP motherboard, two I/O motherboards (210-7609) contain all required IOPs for a particular system. Each motherboard can accomodate a maximum of eight IOPs providing a total of 16 IOP locations. The IOPs supported by the VS-100 are modified versions of the 60/80 IOPs. The major difference is the addition of new firmware to interface the IOPs (except the TC IOP) with the VS-100 CPU.

1.6 INPUT/OUTPUT PROCESSORS

In the VS-100 as in the 60/80, the IOPs relieve the CPU of the time consuming task of communicating directly with attached peripherals. With this feature, I/O processing and data processing can run concurrently on the VS-100

with the resultant increase in processor job-handling speed. Following is a list of the available IOPs with a description of the individual peripherals each IOP can support.

1. 22V25-2 Dual-Density Tape Drive IOP (WLI #212-3010)--Supports up to four 2209V-1/2209V-2 Nine-Track Magnetic Tape Transports and 2209V-3 Seven-Track Magnetic Tape Transports in any desired combination.
2. 22V26 Telecommunications IOP (WLI #212-3020)--Supports up to three separate synchronous communications lines (including Automatic Calling Units). Currently-available line speeds include 1200, 2400, 4800, and 9600 baud. Since each line is independently programmed, the system can run different protocols on separate lines concurrently from the same IOP. Currently-supported industry-standard protocols for bisynchronous transmission include 2780/3780 emulation, 3270 emulation, and HASP. Model 2246R Remote Standalone Workstations also can be attached to the system via 22V26 IOPs, either locally through a "dummy" modem or remotely through a standard modem.
3. 22V27 Serial IOP (WLI #212-3021)--Supports the 2246S Serial Workstation, the 2246C (2-Board only) Combined Workstation, the AWS-1 Archiving Workstation, the 2221V-S/2231V-2S/- 2231V-6S Serial Matrix Character Printers, the 2263V-1S/2263V-2S/- 2263V-3S Serial Chain Printer, 2273V-1S/2273V-2S Serial Band Printer, and the 2281V-S Serial Daisy Wheel Printer in any desired combination. This IOP is available in two models: the 22V27-1, which supports up to eight serial devices, and the 22V27-2, which supports up to sixteen serial devices.
4. 22V28 Large Disk Drive IOP (WLI #212-3023)--Supports up to four 2265V-1/2265V-2 Storage-Module Disk Drives or 2280V-1/2280V-2/-2280V-3 Cartridge Module Disk Drives in any desired combination.

1.7 FRONT AND MAINTENANCE PANELS

Located behind a smoked-glass window on the front cover, the Front Panel provides the user or CE with a quick check of system status. A series of LEDs on the panel indicate to the user the status of certain critical CPU and IOP functions. Refef to Chapter 4, Switches and Indicators, for further details.

Also new to the VS-100 is a maintenance panel located behind the front

cover. Because it is strictly a tool used by the CE, this panel is not accessible to the user . The maintenance panel provides the CE with a powerful troubleshooting aid. It allows the CE to check and monitor most major CPU functions. The maintenance panel when used in conjunction with newly released microcode diagnostics allows the CE to exercise all critical areas of the CPU.

1.8 POWER SUPPLIES

Power for the VS-100 Mainframe is supplied from two sources: a Wang Linear Power Supply providing the +12VDC and -5VDC voltages, and two OEM switching supplies providing the +5VDC voltages. These units are located behind the front cover, directly below the CPU motherboard. Neither of these two units are accessible by the customer. Any work involving these units should be done by a Wang CE. (Refer to Chapter 6, Preventive Maintenance and Adjustments.)

1.9 SOFTWARE DESCRIPTION

The VS-100 supports Release 5.01 of the VS Operating System (OS). This software release contains several new features and functional improvements over previous releases (Release 4). Major areas of change are in the Command Processor, the Operator's Console Menu, and the SYSGEN procedure. Most other features of Release 5.01 are similar to previous releases and are discussed in Paragraphs 1.9.1 through 1.9.4.

Changes in the Command Processor include a slightly changed Main Menu to reflect the combination of two commands, SHOW DEVICE STATUS and MOUNT/DISMOUNT VOLUMES, into one called COMMAND DEVICES. This new command also includes several new options that allow the user to perform such functions as changing mount restrictions and modifying work and spool file eligibility more easily.

Changes in the Operator's Console menu include the displaying and controlling of all devices through separate PF keys (PF9 through PF13), the setting of up to eight workstations as dual operator/user mode terminals with PF14, and the activating of the PRINT I/O ERROR LOG command also with PF14.

1.9.1 USER CONVENIENCE FEATURES

A system must be designed so that its users can make the most effective use of its facilities, without being forced to undergo a long and arduous learning process. The VS-100 System is such a user-oriented system. The VS-100 offers a multitude of convenience features that make it easy to use by programmers and non-programmers alike. These features include a versatile data entry, file maintenance, and report generation facility; an interactive text editor for entering and editing source programs; an easy-to-use symbolic debug facility for program debugging; and an assortment of system utility programs, including SORT, COPY and LINK routines.

1.9.2 ADDITIONAL SYSTEM UTILITIES

The VS-100 system provides a variety of additional system utility programs to support the general programming task. These include, among others, COPY, SORT, and LINK utilities. The versatile COPY utility permits the user to copy a single program or data file, an entire library of such files, or a complete disk volume. For data files, the COPY utility provides an option to change the file organization from sequential to indexed or vice-versa. The SORT utility provides high-speed sorting and merging capabilities for both indexed and sequential files, with either fixed- or variable-length records. The LINK program is used to link together two or more program modules into a single large program, and also offers the option to remove the symbolic debug information previously inserted for debugging purposes. Other utilities include a translation utility which translates from EBCDIC to ASCII and vice-versa; a special copy utility which copies and automatically translates Wang 2200 program and data files to VS format (and vice-versa); and a display utility, which can be used to display and/or print printer files. Table 1A lists all major VS-100 utilitiy programs with a brief description of the function of each utility.

TABLE 1A VS-100 SYSTEM UTILITY PROGRAMS

PROGRAM NAME	DESCRIPTION
ASSEMBLE	-- Assembles a source program written in VS assembler language.
BASIC	-- Compiles a program written in VS BASIC.
COBOL	-- Compiles a program written in VS COBOL.
CONTROL	-- Defines attributes and validation criteria for a data file.
COPY	-- Copies files, libraries, or volumes from one location to another.
COPY 2200	-- Copies and automatically converts files from 2200 standard format to VS format, and vice versa.
DATENTRY	-- Creates and updates data files.
DISKINIT	-- Initializes a new disk volume in VS format, with a volume label and Volume Table of Contents.
DISPLAY	-- Displays file contents on the workstation screen.
DUMP	-- Produces a printed copy of a task dump previously written to diskette with the DUMP AND CANCEL function of the Debug Processor.
EDITOR	-- Enters and edits source program text.
EZFORMAT	-- Creates display files for formatting the work station screen.
LINKER	-- Combines two or more program modules into a single executable program.
LISTVTOC	-- Produces complete or selective listings of a specified volume's Table of Contents, and examines the VTOC for errors.
PL/1	-- Compiles source programs written in VS PL/1.
PRINT	-- Prints the contents of a print file.
REPORT	-- Produces customized reports from a data file.
RPG II	-- Compiles source programs written in VS RPG II.
SORT	-- Sorts a data file, with an optional capability to merge two or more sorted files.
TRANSL	-- Automatically translates the contents of a specified file from EBCDIC to ASCII (the code used internally by the VS-100 system), or vice versa.

1.9.3 FILE PROTECTION AND SECURITY

All VS-100 system disk and tape files are classified according to a flexible file protection and security system, tailored at installation to the specific needs of the user. This system is under the direct control of the Security System Administrators at each installation. These Security System Administrators are specially-recognized users who determine the meaning and use of the file protection classes. They are able to access all files on the system, including the System User List and the Special Privilege Program List.

Every program, procedure, and data file on the system can be placed in one of twenty-eight file protection classes. Protection class codes are designated by a capital letter, 'A' through 'Z', which represent protection classes whose meanings are assigned by the Security System Administrators. Such assignments normally are given mnemonic relationships--as indicated in the following list of "typical" examples:

Class W = The Workorder File
Class P = The Product File
Class C = The Customer File
Class Q = The Sales Quota File

The system also recognizes two special classes, "#" and " " (blank), which are reserved for specific uses:

Class ' ' -- Desginates unprotected files, which are open to all users.

Class '#' -- Designates private and/or Security System Administration files that are not available to any of the normal class codes.

The class of unprotected files is specified by setting the file protection class to blank. An unprotected file can be accessed by any user of the system. The '#' class, unlike the other file protection classes, is used to define one protection class for each user. When specified, the '#' class code identifies those files which can be accessed only by the user who created them (and by the Security System Administrators).

Before users of the system can access a protected file, they must identify themselves using the LOG-ON command. At log-on time, the user's LOG-ON ID and password are validated by lookup in the System User List, and the user's "access rights" are determined relative to the defined file protection classes. Access rights are listed in the System User List for each file protection class to specify three different levels of privilege in order of increasing responsibility, as follows:

1) Execute Only Access (EXEC)
2) Execute and Input Access (READ)
3) Execute, Input, Update, Rename, Scratch and Debug Access (WRITE)

These access rights are checked whenever users attempt to execute a program or procedure, open an existing file, or rename or scratch a file.

1.9.4 RELIABILITY

To ensure the integrity of information stored in memory and on external storage devices (disk or tape), the system provides automatic error detection and correction facilities. In physical memory, all single-bit errors are corrected automatically, while multi-bit errors cause an error indication. Similar checks also are performed on information stored on disk or tape.

1.10 EXPANDABILITY

The modular design of the VS-100 system permits it to be readily expanded with additional physical memory (a maximum of 2Mbytes), more on-line storage devices (a PROJECTED maximum of 16 devices), and additional workstations and printers (a PROJECTED maximum of 128 SERIAL peripherals). Expansion can be carried out with no impact on existing software, except for the need to "regenerate" the system to update the Operating System software to reflect the newly-added devices. Consequently, the user with distributed data processing requirements can purchase several assorted system configurations of differing size and complexity, and can use a common set of application software on all systems. "Typical" VS-100 system-option configurations are as follows:

1. MINIMUM VS-100 SYSTEM CONFIGURATION:

512-KB Main Memory	Two 210-7603 MM Cards
Two Workstations*, One Printer	One 22V27-2 IOP
One Disk Drive	One 22V28 IOP
One Magnetic Tape Drive	One 22V25-2 IOP

2. TYPICAL VS-100 SYSTEM CONFIGURATION:

768-KB to 1.5-MB Main Memory	Four to Six 210-7603 MM Cards
28 Workstations*, 4 Printers	Two 22V27-2 IOP's
Two 288-MB Disk Drives	One 22V28 IOP
One Magnetic Tape Drive	One 22V25-2 IOP
One Telecommunications Channel	One 22V26-1 IOP

3. MAXIMUM (PROJECTED) VS-100 SYSTEM CONFIGURATION:

2-MB Main Memory	Eight 210-7603 MM Cards
96 Workstations*, 32 Printers	Eight 22V27-2 IOP's
Sixteen 288-MB Disk Drives	Four 22V28 IOP's
Eight Magnetic Tape Drives	Two 22V25-2 IOP's
Six Telecommunications Channels	Two 22V26-3 IOP's

* One of these workstations will be an AWS-1 Archiving Workstation. One AWS-1 is shipped as standard equipment with every VS-100.

1.11 ASSOCIATED PERIPHERALS

The VS-100 System supports all currently offered VS peripheral devices, with the exception of all parallel workstations and printers. The following paragraphs list and describe those peripherals available to the VS-100.

1.11.1 WORKSTATIONS

CRT/Workstations are the primary means of communicating with the VS-100 system. Four models are available for use on the VS-100. These can be divided into two types, the 2246 series and the 2266 series, as follows:

1. 2246-SERIES WORKSTATIONS

The 2246S Serial Workstations connect to the VS-100 using coaxial cables and a 22V27 Serial IOP. The system also interfaces with 2246C Combined Data-Processing/Word-Processing Workstations, which are particularly useful for those applications requiring word-processing functions. A VS-100 system can support up to 128 such workstations, in any combination (requiring a separate 22V27-2 IOP for each group of 16 workstations), but the normal system configuration uses some portion of this 128-port capacity for serial printers.

The workstations consist of a keyboard and a display screen combined in a single case. The keyboard contains the familiar typewriter-like arrangement of alpha-numeric, and special character keys, together with two extra banks of keys to the right of the standard group. The first of these two banks consists of cursor-control and special-function keys; the second bank contains numeric keys in a calculator arrangement. In addition, a strip of 16 PF (Program Function) keys runs along the top of the keyboard. On the 2246S model, these sixteen dual-function keys are marked PF01/PF17 through PF16/PF32; on the 2246C model, these same designations are provided on a plastic strip located just below the keys, while the keys themselves are enscribed with the associated WP functions initiated by each key. The 12-inch diagonal CRT has a total display capacity of 1920 characters (24 rows, with 80 characters per row) which can be displayed in either "normal" or "highlighted" (bright) intensity.

Locally-attached workstations can be located anywhere up to a maximum distance of 2,000 feet from the CPU Mainframe unit. Remotely located TC workstations can be installed wherever a telephone line can be accessed. Such workstations communicate with the CPU Mainframe via a 22V26 TC IOP.

2 ARCHIVER WORKSTATION

All VS-100 Systems will be shipped with one 2266-series Archiving Workstation as standard equipment. The Model 2266-series VS-AWS system consists of a 2266 Archiver Terminal connected to a 2266-series Archiver Master Unit by a 25-ft (7.6m) data cable. Contained in the Master Unit is

a Model 2270V Double-Sided Double-Density (DSDD) Diskette Drive and all associated logic cards. The VS-AWS system is available in five models, covering different capabilities in either combined word and data processing or strictly data processing. Model numbers for the combined systems are 2266C-1 and 2266C-3. Model numbers for the data processing systems are 2266S-1, 2266S-2, and 2266S-3.

The VS-AWS system is designed to handle either or both of two different diskette media formatting techniques: conventional hard-sector formatting or a new soft-sector formatting technique. The Model 2266S data processing Archiver is available in three different versions: the -1, which includes a hard-sector controller providing 315Kbytes of storage; the -2, which includes a soft-sector controller providing a maximum of 1.2Mbytes of storage; or the -3, which includes both controllers. The Model 2266C combined system is available as a -1, outfitted with the hard-sector controller, or a -3, which contains both kinds of controllers.

The Archiver Terminal has its own power supply and plugs into any convenient 115V (60 Hz)/230V (50 Hz) outlet through a built-in 7-ft (2.1m) power cord. Except for intensity, focusing, and key-response electronics, all workstation logic cards are located in the Archiver Master Unit. The Master Unit has an independent power supply for the contained diskette drive electronics and logic boards and plugs into any convenient 115V (60 Hz)/230V (50 Hz) outlet through a built-in 6-ft (1.8m) power cord.

The Archiver Master Unit connects to a VS host computer through a standard coax cable, available in multiples of 50 ft (15.2m) up to a maximum length of 2,000 ft (609.6m). Connection to the VS-100 system is made through a 22V27-1 (8-port) or 22V27-2 (16-port) Extended Serial IOP (Input/Output Processor) assembly located in the host Mainframe.

1.11.2 SERIAL PRINTERS

The primary output devices of the VS-100 system are serial printers. These devices are available in a variety of types and models, offering different speeds and print styles. Each printer attaches to the Mainframe through a coaxial cable that connects independently to any desired I/O port of

any one of up to eight 22V27 Serial Workstation/Printer IOPs. Although the VS-100 system is designed for operation only with serial printers, the associated 2246R Standalone TC Workstation can itself operate with a satellite parallel printer, which connects to the rear of the 2246R workstation via a standard RS-132C coupling. Following are descriptions of the printers supported by the VS-100.

1. 5521 Matrix Character Printer

The 5521 Matrix Character Printer forms most characters with a 9x7 dot matrix; a larger 9x9 matrix is used for special characters for greater detail. The 5521 provides a 96 character set, including uppercase, lowercase, and special characters. It can handle multipart forms of up to four carbons plus an original. The printer accepts paper in widths from 3 1/2 inches (8.9 cm) to 14.9 inches (37.2 cm). The printer provides automatic vertical formatting, programmable audio alarm, and an expanded-print capability. The 5521 prints at an average speed of 200 characters per second (cps). The number of lines printed per minute (lpm) varies, according to the line length, from 65 to about 300 lpm.

2. 5531-2 Matrix Printers

The 5531-2 is an economical matrix printer offering many of the same features of the 5521V matrix printer, but at a slower print speed. The 5531-2 provides a full 96-character set, including uppercase, lowercase, and special characters, using a 7-by-9 dot matrix to form each character. The 5531-2 prints a 132-character line at an average speed of 120 cps (actual speed varies, according to line length, from 45 to about 250 lpm) The 5531-2 can handle multipart forms and variable paper widths, and is equipped with an audio alarm.

3. 5570/5571 Chain Printers

The 5570 and 5571 are solid-character line printers which produce quality printed output at high speed. The 5570 has a printing speed of 400 lpm; and the 5571 has a printing speed of 600 lpm.

The 5570 and 5571 print one entire line (up to 132 characters) at a time. They can print one original and up to five carbon copies, and handle paper widths from 3.5 inches (8.9 cm) to 19.5 inches (48.8 cm). These printers provide a number of useful features, including an automatic paper puller, static eliminator, and programmable audio alarm. Different typefaces and special character sets (including foreign language character sets) are optionally available.

4. 5573/5574 Band Printers

The 5573 and 5574 are solid-character line printers producing quality printed output at high speed. The 5573 has a printing speed of 300 lines per minute (lpm); and the 5574 has a printing speed of 600 lpm. The 5573 and 5574 print one entire line (up to 136 characters) at a time. They can print one original and up to five carbon copies, and handle paper widths from 3 inches (7.6 cm) to 16 inches (40.6 cm). These printers provide a number of useful features, including an automatic paper feed, static eliminator, and programmable audio alarm. Different typefaces and special character sets (including foreign language character sets) are optionally available.

5. 6581W Serial Daisy Wheel Printer

The 6581W Serial Daisy Wheel Printer is a bidirectional output writer that uses a "daisy" character wheel with an 86-character set (uppercase/lowercase alphamerics and special characters). This printer produces typewriter-quality output at a rate of 30 cps. The removable character wheels can be replaced to change character sets as desired.

1.11.3 DISK DRIVES

The VS-100 system is designed to operate with either or both of two different models of large-capcity disk drives, each of which is available in different capacities. One of these is the 2265V-Series SMD (Storage Module Disk) Drive. The other is the 2280V-Series CMD (Cartridge Module Disk) Drive.

1. 2265V SMD Drive

The Model 2265V-Series SMD Drive is a high-performance, high-capacity disk unit which provides fast access to large volumes of data. The SMD drive contains a multiplatter storage module that can be removed easily for off-line storage or replacement by another module containing different applications tasks. The top and bottom platter surfaces in the storage module are not used for data storage; they serve as physical protection for all inner platters. In addition, one side of an internal platter is used solely for servo-head track selection, with the remaining platter surfaces being configured to store 16 megabytes each of data. Besides high speed and large data storage, each SMD provides extensive error checking and correcting facilities.

The 2265V-Series SMD Drive is available in two models:

a. The Model 2265V-1 SMD Drive provides a maximum of 75 Mbytes of storage using a 5-platter module, providing six storage surfaces.
b. The Model 2265V-2 SMD Drive provides a maximum of 288 Mbytes of storage using uses an 12-platter module, providing 19 storage surfaces.

Up to four SMDs of either capacity in any desired combination (including combinations mixing either or both with one or more different configurations of the 2280V Phoenix CMDs) can be connected to the VS-100 Mainframe Unit via a single 22V28 Large Disk Drive IOP. Connecting four 2265V-2 288-MB SMDs thus provides a maximum on-line storage capability of 1.15 gigabytes for each such 22V28 IOP-controlled group. The VS-100 addressing structure allows up to four such groupings to be installed, thereby producing a maximum VS-100 on-line storage capacity of 4.6 gigabytes if the system contains 16 Model 2265V-2 SMDs.

2. 2280V Phoenix CMD DRIVE

The Model 2280V-Series Phoenix Cartridge Module (CMD) Drives are high-performance units which combine the high-density track-selection features and the security-supporting module removability of the 2265V-Series SMD with the convenience of a fixed-platter package. The

Phoenix drives contain a multi-platter "fixed" disk pack and a easily removable single-platter cartridge for off-line data storage. One surface of the removable cartridge is available for 16-Mbyte storage of data, and the other surface is used for track selection. In addition, one of the surfaces in the multiplatter fixed disk pack also is used for track selection in order to integrate the removable platter with the fixed pack. All remaining surfaces of the fixed pack are available for use, providing 16-megabytes of storage on each surface, with the number of available surfaces depending on which of three CMD models is used:

a. The Model 2280V-1 (30-MB) CMD Drive uses one "fixed" platter, providing a total of two useful 16-megabyte storage surfaces.
b. The Model 2280V-2 (60-MB) CMD Drive uses two "fixed" platters, providing a total of four useful 16-megabyte storage surfaces.
c. The Model 2280V-3 (90-MB) CMD Drive uses three "fixed" platters, providing a total of six useful 16-megabyte storage surfaces.

Up to four Phoenix CMDs in any desired combination (including mixes of one or more CMDs with one or more 2265V-series SMDs in any combination) can be connected to the VS-100 Mainframe Unit via a single 22V28 Large Disk Drive IOP. The VS-100 addressing structure allows up to four such groupings to be installed.

1.11.4 TAPE DRIVES

The 2209V-Series Magnetic Tape drives are particularly useful for transferring bulk-stored data between the VS-100 and other computer systems. These drives support both ASCII and EBCDIC character codes, handle PE (Phase Encoded) or NRZI (Non-Return to Zero, Indiscrete) recording formats, and provide read-after-write verification and automatic correction for single-track errors and those multiple-track errors that can be reduced to a single track. Up to four tape drives can be connected to the VS-100 system in any desired combination through a single 22V25-2 Magnetic Tape Drive IOP; one of the tape drives must contain a Formatter subassembly (WLI #725-0064), making it the "Master Tape Unit"; the other tape drives are "slave" units, connected to and governed by that same Formatter subassembly.

1. 2209V-1 Nine-Track Tape Drive

The 2209V-1 Tape Drive reads from or writes to tape at a 1600 bits-per-inch (bpi) rate, using Phase Encoding. The unit contains a dual-gap read/write head, full-width erase head, tape cleaner, and photo electric sensors to detect reflective tape markers and tape breakage. The drive transports tape at a velocity of 75 ips during read and write operations, and up to 200 ips during rewind.

2. 2209V-2 Nine-Track Dual-Density Tape Drive

The 2209V-2 Dual-Density Tape Drive is program-selectable for operation at either 1600 or 800 bpi. Specifications for the 2209V-2 are the same as the 2209V-1 described above with the exception that the 2209V-2 uses Phase Encoding for data transfers at 1600 bpi, and NRZI coding for 800 bpi data transfers.

3. 2209V-3 Seven-Track Tape Drive

The 2209V-3 Tape Drive operates with 7-track tape, handling NRZI coding at a maximum speed of 800 bpi. Specifications for this unit are the same as the above two units. The drive transports tape at a speed of 75 ips during read/write operations, and up to 200 ips during rewind.

1.12 TELECOMMUNICATIONS

The ability to transfer data between remotely located terminals and the VS-100, or between the VS-100 and other mainframes at distant sites is becoming more and more important in the business world. To accomodate this need, the VS-100 uses the 22V26 TC IOP. Depending on the model selected, the 22V26 can support one (22V26-1), two (22V26-2), or three (22V26-3) separate bisynchronous communications lines, allowing concurrent handling of up to three different protocols.

The 22V26 IOP in conjunction with the 2246R Remote Workstation allows a remote user full access to the VS-100. The 22V26 IOP in conjunction with the available 2780/3780 or 3270 emulations allows the VS-100 to communicate

directly with remotely located host systems, compatible terminals, or other Wang systems.

Data transmissions speeds of 1200, 2400, 4800, and 9600 baud are accomodated by the 22V26 IOP. All lines on a 22V26 can support an Automatic Calling Unit (ACU).

1.12 SYSTEM SPECIFICATIONS

Following are the physical, electrical, environmental, and operational specifications for the VS-100.

1. Physical Specifications

Width	48.0 Inches	121.9 cm
Height	41.0 Inches	104.1 cm
Depth	31.5 Inches	80.0 cm
Weight	750 lbs.	340.2 Kgs

2. Electrical Specifications

Input Circuit	Dedicated w/30A circuit breaker in computer room
Voltage	220VAC +10%, -15%
Frequency	50/60Hz Split Phase
Amps	17.0 (maximum; 14.2 plus 2.8 for fans)
Power	2027 Watts (calculated max.)
Heat Output	8000 BTU/Hr (max.); 1750 KCAL/Hr (max.)
Power Cable	9 Feet 2.9 Meters

3. Environmental Specifications

Temperature	+60°F (+15.5°C) to +80°F (+26.7°C)
Humidity	40% to 60% non-condensing

4. Operational Specifications

Control Memory Size	8 Kbyte
Cache Memory Size	32 Kbyte (8K 32-Bit Words)
Main Memory Size	512 Kbyte (minimum) 2 Megabyte (maximum)
Main Memory Word Size	32-Bit Data Word, 7-Bit Parity Field
Main Memory Cycle	640 nanoseconds (480 nsec memory cycle plus a 160 nsec SBC arbitration cycle.)
Main Memory REFRESH Cycle	Every 15 microseconds
CP Cycle	160 nsec (synchronized with SBC cycle)
SBC Cycle	160 nsec
CP4 Data Path	32 Bits Wide
Main Memory Data Path	64 Bits Wide
BA-IOP Data P th	16 Bits Wide
CP4 Address Path	24 Bits Wide
Main Memory Address Path	20 Bits Wide
BA-IOP Control Path	8 Bits Wide
Inter-Processor Communication (IPC) Word	32 Bits
System Clock	25 MHz, 40 nsec (derived from a 50 MHz oscillator on the 210-7602 card)
CP Micro-Instruction	48 Bits Long (22-Bit Process Field, 8-Bit Memory Field, 18-Bit Branch Field)
CP Registers	Sixteen 32-bit General Purpose Registers Four 64-bit Floating Point Registers

CHAPTER 2

THEORY OF OPERATION

CHAPTER 2
BLOCK DIAGRAM LEVEL THEORY OF OPERATION

2.1 OVERVIEW

The VS-100 consists of eight major card assemblies, as shown in Figure 2-1, the System Block diagram. The System Block should be used to observe the multitude of inter-board signal lines and busses and the direction of data flow while reading the block theory of operation. Because the I/O Processor (IOP) is common to other VS systems, it will only be referred to when necessary in relation to the remaining seven cards. A block diagram of the major logic elements on the other cards accompanies the theory of the card. The theory explains the major logic element functions of each card, but these explanations do not trace specific signals, busses, or micro-instructions through the entire system.

2.2 VS-100 CONTROL MEMORY

The VS-100 Control Memory, (Figure 2-2) a loadable Random Access Memory, stores all Central Processor micro-instructions. The loadable Control Memory permits CP microcode updates, microcode expansion, and use of micro-level diagnostics. The Control Memory card, containing 8K of RAM, is separate from the CP to allow flexible Control Memory size. The CP branch field allows 14-bits (16K possible locations) for Control Memory addressing. CP micro-instructions are 6 bytes (48 bits) long with a seventh byte containing two parity bits.

All system microcode is recorded on a mini-floppy diskette. A simple, low cost, mini-floppy diskette drive is used to load the microcode into the Control Memory RAM. A 1K PROM, located on the diskette drive controller, contains micro-routines to support the mini-floppy Z80 microprocessor during the microcode loading.

Fetching a micro-instruction from Control Memory requires a full 48-bit path to the CP. Two micro-instructions, Write Control Memory and Read Control

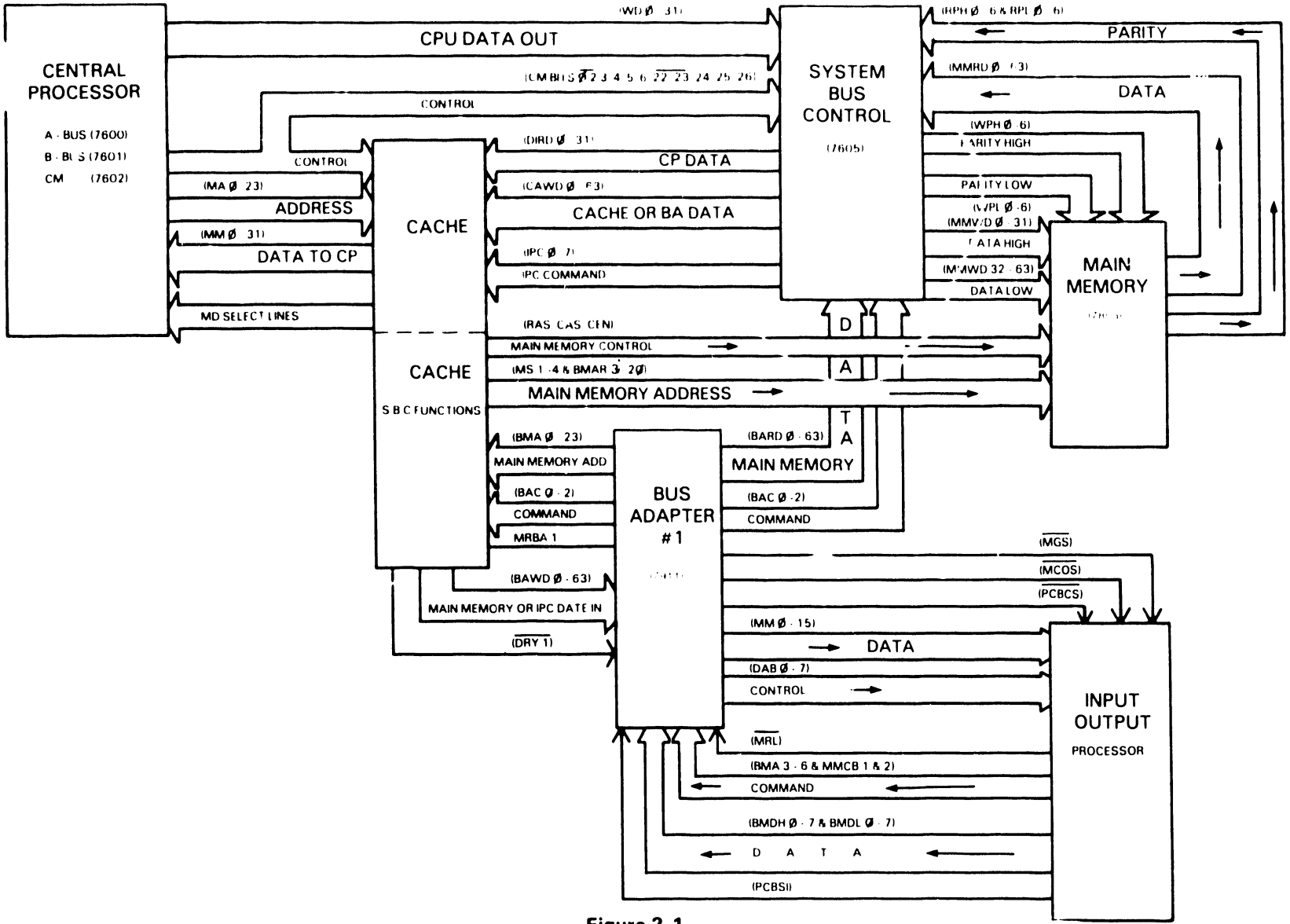


Figure 2-1
VS-100 SYSTEM BLOCK

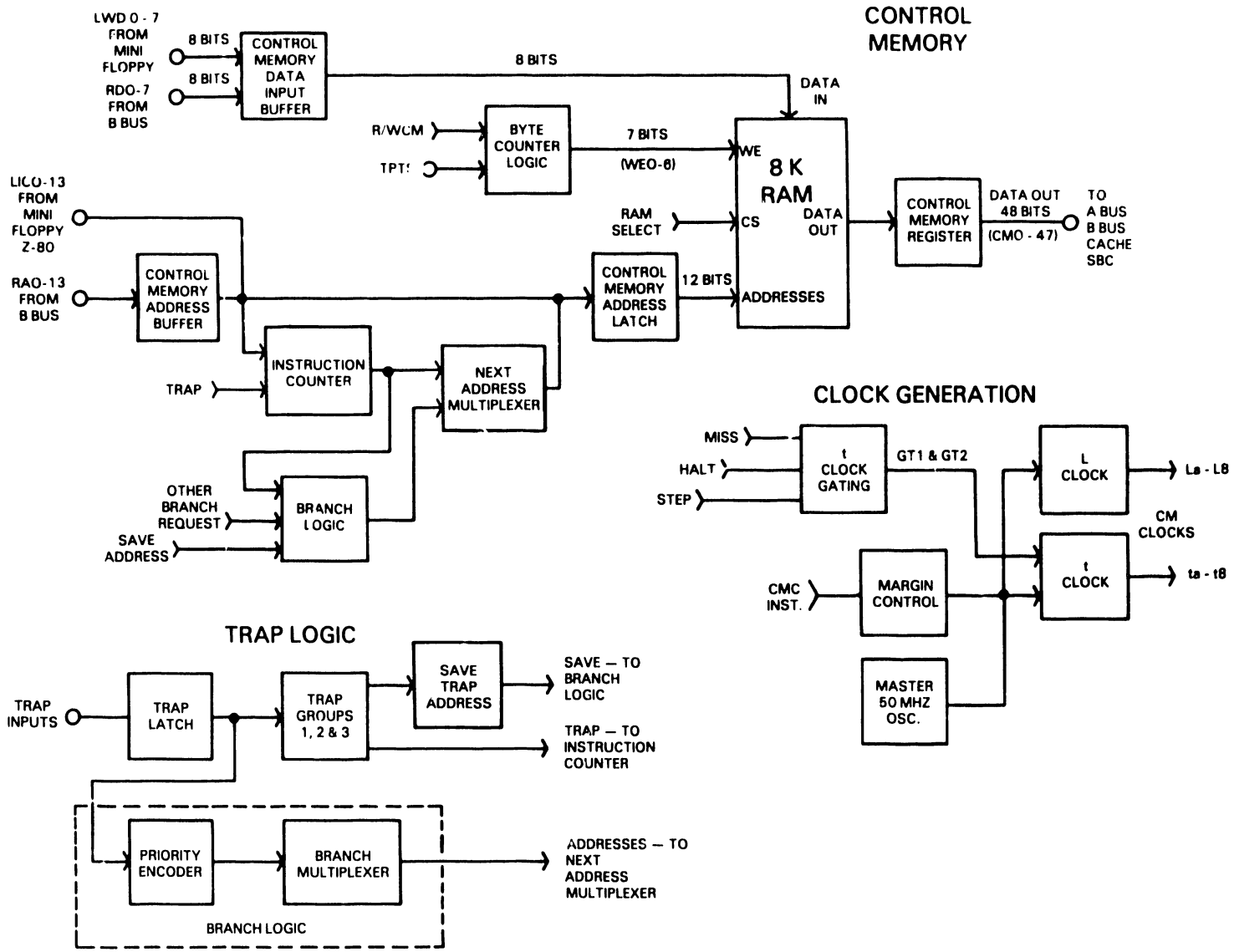


Figure 2-2
VS-100 CONTROL MEMORY

Memory, are provided for reading or writing one Control Memory byte at a time. Traps, branching, and master timing are all functions of the Control Memory card, even though not directly related to Control Memory functions.

2.2.1 Writing Control Memory

There are two methods for writing to Control Memory RAM. The first method allows the system microcode to be loaded from the mini-floppy diskette using the CPU 'BT' (BOOT) button on the front panel. One byte of data read from the mini-floppy, as LWD0-7, is written through the Control Memory Data Input Buffer to a RAM location. Addresses (LIC0-13) are supplied to the CM Address Latch from the Z80 microprocessor chip on the mini-floppy controller as the data is read from the diskette. A Byte Counter tallys the number of bytes loaded for each CM word. The Byte Counter increments the RAM write enable inputs (WE0-6) each time a byte is written. As each CM word is 50 bits long (48 data and 2 parity), the Byte Counter cycles 7 bytes per word. When the last byte of a word has been written, the counter is reset.

The second method, using an outer level Patch CP Micro-code instruction, can be used for testing microcode updates. Control Memory is modified one byte at a time using RD0-7 (6 data bits and 2 parity bits) from the Program Mask Register on the B Bus through the CM Data Input Buffer. The byte will be written to the RAM using addresses (RA0-13) from the B Bus Virtual Memory Address Register to the Control Memory Address Buffer and through the Control Memory Address Latch. The Byte Counter tallys the number of bytes loaded for each CM word.

2.2.2 Reading Control Memory

After the system microcode has been loaded, pressing the System Load button on the front panel causes a trap (see paragraph 2.2.3) and branch to Control Memory location zero to begin system IPL execution. The trap address will be forced into the Branch Multiplexer and sent to the Next Address Multiplexer for loading into the Control Memory Address Latch. The Instruction Counter is also loaded with this current address and incremented

by one to prepare the next address. The RAM write enable inputs are inactive, allowing the RAM to be read. The Control Memory Register is always output enabled and the data, as CM bits 0-47, is available to the A Bus, B Bus, Cache Memory, and System Bus Controller. The sequential incrementing of the Instruction Counter and the fetching of micro-instructions continues unless interrupted by branch, trap, or write Control Memory operations.

TABLE 2A VS-100 TRAP ADDRESSES

TRAP	CONDITION		TRAP ADDRESS
POWERON	CP Power-on		0000
LOAD	CP Initialize		0001
INVA	Invalid (physical) Memory Address		0002
TT0	MAR0 Translation		0003
TT1	MAR1/MAR2 Translation		0004
TT2	Protection (any MAR)		0005
ATR1	Word Alignmant (CM27-29 = 001)		0006
ATR2	Word Alignment (CM27-29 = 010)		0007
ATW	Word Alignment (write)		0008
ATM0	Alignment MAR0 (halfword)		0009
OVFT	Overflow (ACT or SCT instructions)		000A
MMPT	Main Memory Parity		000B
BEX	Execute Target	(EXEC = 1)	000C
PAR	CP Control Memory Parity		000D
BX	External Event	(EXT = 1)	0011
BDEBUG	Software	(DEBUG = 1)	0012
BCLKM	Clock Maintenance	(CS1 = 1)	0013
BCLKI	Clock Interrupt	(CS3 = 1; CS4 = 1)	0014
BIO	IO Interrupt	(IO3 = 1; IOMASK = 1)	0015
BPAGE	Pagebreak	(PAGEOV = 0)	0016
BENTRY	Entry Pagebreak	(New PAGEOV = 0) and not rr case)	0017

Note: - Trap BEX and traps 0011-0017 are Branch to Next Macro-related traps.

2.2.3 Traps

Traps, interrupts to the CP micro-program, are caused by conditions not initiated within the CP. (Refer to TABLE 2A.) CP micro-trap conditions can occur due to process, memory, branch field operations, or external conditions. When a trap condition is detected, the hardware forces a branch

to a specific Control Memory address, determined by the type of trap, for execution of a routine intended to take action in response to the condition causing the trap. All micro-traps branch to locations in the Control Memory RAM. Return addresses can be saved, when necessary, with a micro-routine that follows the trap handling routine, so that execution of a program in progress prior to the trap can resume. Traps are first loaded into the Trap Latch for servicing. The trap will be prioritized to produce a specific Control Memory address of the trap handling routine for the Branch Multiplexer. The address from the Branch Multiplexer will be sent to the Next Address Multiplexer for loading into the Control Memory Address Latch and the trap routine will begin execution. The Instruction Address Counter is also loaded with this current address and incremented by one.

2.2.4 Branching

Three formats of branching are available to the VS-100: full address, conditional, and status setting. All are dependent on the state of the current micro-instruction branch field. The branch field logic decodes the current micro-instruction branch field, CM bits 30-33. The Branch Multiplexer (using CM bits 34-47 and other inputs to determine a branch address) loads the address into the Next Address Multiplexer. The NAMX might also contain the contents of the Instruction Counter (used for status setting and certain types of branching).

The address is loaded from NAMX into the Control Memory Address Latch for instruction execution. The Instruction Counter is also loaded with the address from NAMX and incremented by one. This logic operates much the same as trap logic as far as sequencing is concerned. The branch logic also allows nesting of branch routines to a depth of 16 when certain branch conditions require current or next micro-instruction addresses to be saved.

2.2.5 Clock Generation And Control

The VS-100 Master Clock is generated by a 50 Mhz oscillator and is then

divided by two. The clock produces two strings of 40 nanosecond master timing pulses, L times (La-L8) and t times (ta-t8). The t times are activated by the free running L times and are delayed 20 nanoseconds from the L times. A different number of L and t time clocks occur for each micro-instruction execution. The instruction length time period is synchronously controlled by a binary counter. This counter is counted up from 0 to 2 and then loaded with the results of the decoding of CM bits 0-6. CM0-6 determines the type of instruction to be executed. The counter then resumes count from this new value. When the counter reaches a count of 15 (F) this signals the end of the instruction length. The counter is reset and the L sequence begins again.

The master clock is distributed to the A and B Bus for generation of their own L and t times in synchronization with the CM card. Gating signals GT1 and GT2 will reset the t time clocks on the CM, A Bus, and B Bus, to halt program execution upon occurrence of certain conditions such as Cache miss, halt, and the run/step maintenance switch.

The clock margin control logic varies the L time and t time clock frequencies within 10% of the standard frequency. Micro-instructions are available to increase or decrease the clock speed, or to reset the clock speed to normal. The use of these micro-instructions is for detecting marginal hardware problems and not for system performance acceleration.

2.3 VS-100 CENTRAL PROCESSOR

The Central Processor (also known as CP4) is the heart of the VS-100 system. The primary task of the Central Processor is to execute the machine instruction set and monitor the results of execution. The CP contains facilities for addressing physical Main Memory, fetching and storing information, arithmetic and logical processing of data, sequencing instructions in the desired order, and initiating communication between Main Memory and external devices. The Central Processor is composed of two cards, the A Bus and the B Bus, with each card containing many standard and unique logical elements.

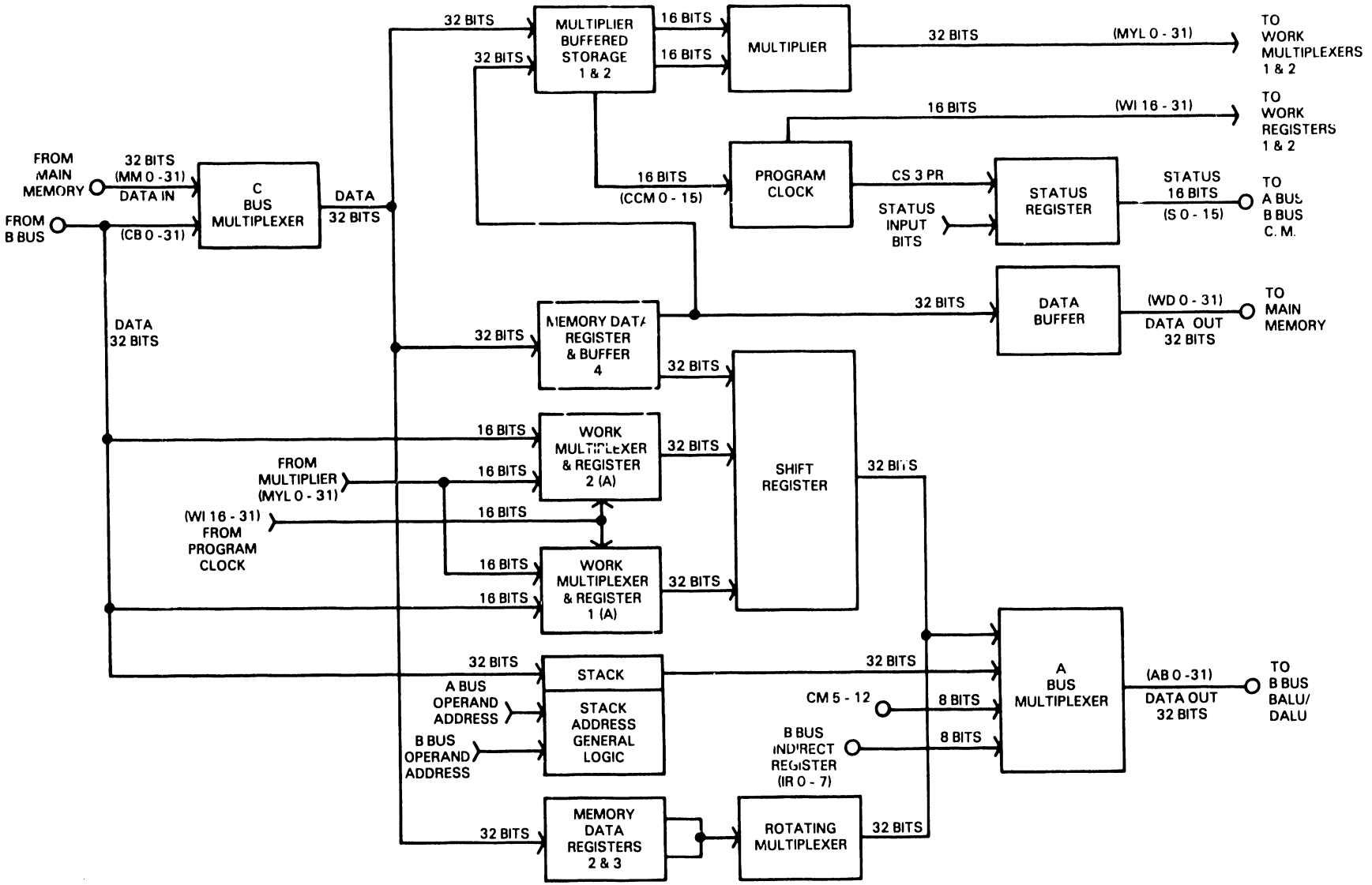


Figure 2-3
VS-100 A BUS

2.4 VS-100 A BUS

The VS-100 A Bus (Figure 2-3) contains all A Bus registers and multiplexers, the status register, multiplier, stack, and program clock.

2.4.1 C Bus Main Memory Multiplexer (CBMMX)

The CBMMX, 32 bits wide, receives C Bus data (CB0-31) from the B Bus card, or Main Memory data (MM0-31). The C Bus inputs are selected by default (no Main Memory read) while the Main Memory data inputs are selected when Main Memory is being read. The data can be transfered to four possible receiving elements: Memory Data Registers 2, 3 or, 4, or Multiplier Buffer Storage 1.

2.4.2 Memory Data Registers 2 And 3, And Rotating Multiplexer

The three memory data registers (MDR 2, 3, And 4) are also 32 bits wide. MDR 2 and 3, in conjunction with Memory Address Register 1, provide buffered read access of four non-aligned bytes for storage to storage operations. MDR2 is also used for general memory operations. Output data (from MDR2 or MDR3) is sent to the Rotating Multiplexer. Two Control Memory bits and three MAR1 address bits determine which data bytes (a maximum of 4) from the available four data bytes will be sent to the Rotating Multiplexer. Whether MDR2 or MDR3 is selected depends upon gating developed on the Cache card from decoded memory commands.

The Rotating Multiplexer (RMUX) is 32 bits wide and has the ability to shift the four bytes of a word to suit the requirements of the particular instruction being executed. For example, the Switch 16 instruction requires that the high and low halfwords be reversed. The RMUX input data can come from either MDR2 or MDR3. The 32 bits of output data are Or'd with the Shift Register output data and forwarded to the A Multiplexer. The RMUX function select process is used in conjunction with MDR2/MDR3 Byte Selection. Byte selection determines whether one byte or all bytes of MDR2 or MDR3 are sent to the RMUX. The RMUX function select logic determines in what order the bytes are to be transmitted on the RMUX output lines.

2.4.3 Memory Data Register 4, Data Buffer, Work Multiplexers/ Registers, And Shift Register

Memory Data Register 4 (MDR4), a 32-bit register, along with Memory Address Register 2 is available as a general purpose register for memory data, and Interprocessor Communications data. It is the data output path to Main Memory. Input data comes from the CBMMX and is transfered out by gating developed on the Cache card from decoded memory commands. The output is forwarded to the Data Buffer (DTBF), Memory Register 4 Buffer (M4BF), and Multiplier Buffer Storage 2 (MBS2).

The 64-bit Data Buffer (DTBF) receives 32 input bits from MDR4 and transfers 32 bits, as WD0-31, to Main Memory via the System Bus Controller. The remaining 32 bits (identical to WD0-31) are used for the CP Tester Interface.

Memory Register 4 Buffer (M4BF) is a buffer between MDR4 and the Shift Register. The buffer is controlled by several process field A Bus operations.

The Work 1 and Work 2 Multiplexers (WMX1 and WMX2) are each 16 bits wide. WMX1 selects bits 16-31 from either the C Bus or the Multiplier for delivery to Work 1 or Work 2 Registers. The C Bus input is selected by a multiply operation decoded from an instruction memory operation field. The outputs are enabled by not performing a Store Counter or Store Comparator operation. WMX2 multiplexer selects bits 0-15 from either the C Bus or the Multiplier for delivery to Work 1 or Work 2 Registers. WMX2 is identical in operation and controls to WMX1.

The Work 1 and Work 2 Registers (WK1-A and WK2-A) are both 32-bit registers. They are used for gating data from WMX1 and WMX2 to the Shift Register. Both can also transfer the Program Clock outputs to the Shift Register as data bits 0-15 or 16-31. The outputs are controlled by Work 1 and Work 2 A Bus operands.

The 32-bit Shift Register operates in three shift modes; shift 1 bit right, shift 4 bits right, or shift 4 bits left. For all other functions, the input data (from MDR4, WK1, or WK2) is gated directly through. The 32-bit output is forwarded to the A Multiplexer. Channel selection for the shift register is accomplished using the Shift instruction group.

2.4.4 Multiplier

Multiplier Buffered Storage 1 (MBS1) and Multiplier Buffered Storage 2 (MBS2) are 32 and 16-bit storage buffers for the Multiplier. MBS1 input data comes from the CBMMX. MBS2 input data comes from MDR4, and MBS2 forwards 16 of the 32 input bits to the Multiplier. Output of both MBS1 and MBS2 are controlled by the memory field translation and ripple operations.

The Multiplier consists of 4 high-speed 8 X 8 multiplier chips which multiply two 16-bit operands to form a 32-bit output result. The Multiplier inputs are from MBS1 and MBS2. The outputs, after passing thru a 4-bit binary full-adder, are forwarded to WMX1.

2.4.5 A Bus Multiplexer

The 32-bit A Bus Multiplexer (AMX) collects data from several sources. It receives its high order 24 input bits from the Stack, or from an Or'd combination of RMUX and the Shift Register. The low order 8 input bits are from five possible sources: Stack bits 24-31, RMUX bits 24-31, Shift Register bits 24-31, B Bus Indirect Register bits 0-7, or Control Memory bits 5-12. Output data, AB0-31, is used at the Binary Arithmetic Logic Unit (BALU) and the Decimal Arithmetic Logic Unit (DALU).

2.4.6 CP Stack

The CP Stack, a local RAM storage area, is configured as 256 32-bit registers logically divided into two halves of 128 32-bit registers. The first half of the Stack is again divided into two banks of 64 32 bit

registers, containing general registers used for address calculation and accumulation of fixed point arithmetic or logical operations, and floating point registers used for floating point arithmetic operations. Other registers in the Stack include file and auxiliary registers used as temporary storage areas for micro-program functions, and control registers used to store Program Control Word (PCW) trap addresses and the time of day. The second half of the Stack is used for Translation RAM (T-RAM) monitoring. (Refer to paragraph 2.5.10, the T-RAM.)

The unit of access from the Stack is always 32 bits (one word). Since the Stack access time is significant compared to the total micro-instruction cycle time, only one Stack access is performed within a micro-instruction. The Stack can be addressed using A Bus operands (read only access) or C Bus operands (read and write access). The Stack is addressed using 8 bits made up of some of the following: Bank Select Status bit, Control Memory bits 8-12 (for A Bus selection), Control Memory bits 17-21 (for C Bus selection), Indirect Register bits 0-7, and Current Halfword bits 0-3.

The A Bus Operand Multiplexer, in the Stack Address General Logic block, selects and delivers the appropriate A Bus operand Stack address value to the Stack via the A/B operand Stack Address Multiplexer. The multiplexer has 8 inputs, one of which can be selected according to the value of Control Memory bits 7,10, and 11. Control Memory bit 7 specifies direct Stack access. Stack write operations are not allowed with A Bus operands (read operations only). Channel 4 of the multiplexer is selected for access to the Operating System File Registers.

The C Bus Operand Multiplier, in the Stack Address General Logic block, selects and delivers the appropriate C BUS operand Stack address value to the Stack via the A/B operand Stack Address Multiplexer. The multiplexer has 4 inputs, any one of which can be selected according to the value of Control Memory bits 16, 19, and 20. Control Memory bit 16 allows direct Stack access and also write enables the Stack. Channel 3 of the multiplexer is selected for access to the Operating System File Registers.

The Stack Address Multiplexer (STKMX) is also part of the Stack Address General Logic. It is used to gate either the A Bus operand or C Bus operand address to the Stack address lines. The multiplexer is always output enabled and A or B half selection depends on the value of Stack Load, decoded from Control Memory bits 16-18.

2.4.7 CP Status Register

The CP maintains a 32-bit status register whose contents are designated S0 through S31. The status bits are described in four 4-bit and two 8-bit groups as follows: Loop Control, MAR0 Status, Decode, Indirect Register, Bank Select/MAR2 Translation, and Process Field/ Miscellaneous. (Refer to TABLE 2B.) The Loop Control status bit group contains the most frequently used status bits. Only status bits S0-S15 can be directly accessed for conditional branch operations. For Status Setting operations, the A and B status bit select fields of the Status Setting portion of the branch field format can indicate any one of the 32 status bits. Control Memory bit 39 indicates A bit usage or A bit inverse usage. (The CP Assembler supports A bit inverse usage through the SSI mnemonic.) The bit operations are indicated by Status Operation Control Memory bits 40-41. The B bit is updated with the resultant bit value. The Control Memory bit 40-41 assignments are Move, And, Or, and Xor. (Refer to Appendix E for a complete list of the CP status bits).

TABLE 2B VS-100 STATUS BIT GROUPS

GROUP NAME	STATUS BITS
Loop Control	S0-S3
MAR0 Status	S4, S21-23
Decode	S24-31
Indirect Register	S13-15, S19
Bank Select/MAR2 Translation	S6-7, S16, S20
Process Field/Miscellaneous	S5, S8-12, S17-18

2.4.8 Program Clock

The CP supports a 64-bit program clock and comparator at the macro-level.

The hardware provides a 16-bit counter and a 16-bit comparator. These 16 bits correspond to the low order 16 bits of the macro-level registers. There are four CP status bits (CS1-4) associated with clock operations. A Continous Counter (CCNT) increments once every 500 nanoseconds and when a carry out at the high order bit of the counter occurs, the hardware will set a Counter Overflow status bit. The Continous Comparator (CCMP) is enabled by a Compare Enable status bit. The counter is compared against the comparator for every counter increment. If the counter value is greater than or equal to the comparator, the Clock Interrupt Request status bit is set.

Clock related micro-instructions are available to set the counter to zero, store the counter (in WK1-A and WK2-A registers), load the comparator, and store the comparator. The CP can move the counter contents (process field) and counter overflow bit (branch field) within one micro-instruction.

There are 2 clock micro-traps related to the clock status bits. These traps can occur only within the Branch to Next micro-instruction. The Clock Maintenance micro-trap (BCKLM) is taken when the Continous Counter overflows. This micro-trap is used to propagate the carry-out from the hardware counter into the high order 48 bits of the macro-level clock. The Clock Interrupt micro-trap (BCKLI) is taken when both the Clock Interrupt Request and the Clock Interrupt Enable status bits are set. This micro-trap is used to determine Clock Interrupts at the macro-level.

2.5 VS-100 B BUS

The VS-100 B Bus (Figure 2-4) contains all B Bus registers, buffers and multiplexers and the translation RAM, binary ALU, and decimal ALU.

2.5.1 C Bus Main Memory Multiplexer (CBMMX)

The CBMMX, 32 bits wide, receives either Main Memory data (MM0-31), or C Bus data (CB0-31) for the B Bus. The Main Memory data inputs are selected when Main Memory is being read and the C Bus inputs are selected by default

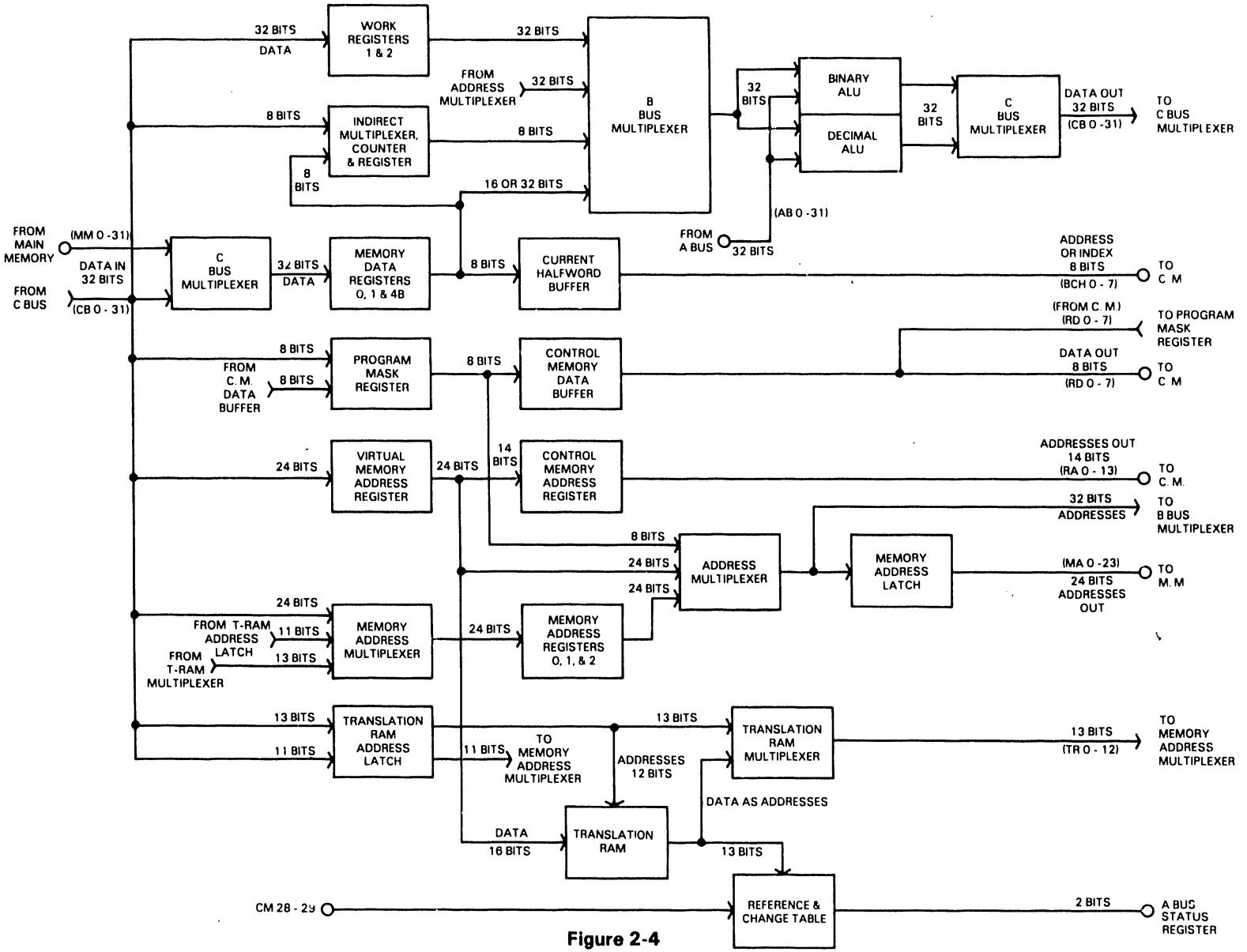


Figure 2-4
VS-100 B BUS

(no Main Memory read). The data can be transfered to three possible receiving elements, Memory Data Register 0, 1, or 4B.

2.5.2 Memory Data Registers 0, 1, And 4B, And Current Halfword Buffer

Memory Data Register 0 and 1 (MDR0 and MDR1), both 32-bit registers, are dedicated to accessing halfwords from the macro-instruction stream to provide overlapped macro-instruction fetching. Input is Main Memory data from the C Bus Main Memory Multiplexer. Whether MDR0 or MDR1 is selected depends upon the decoding of process field C Bus destination operands and gating developed on the Cache card from memory commands.

Multiplexed access of the 16-bit Current Halfword from MDR0 or MDR1 is controlled by Virtual Memory Address Register bits 21-22 passed through the Control Memory Address Buffer (RABF) to the Current Halfword selector. The Current Halfword (CH0-15) is then forwarded to the B Bus Multiplexer. Also, the high order byte of the Current Halfword will be sent to the Current Halfword Buffer.

The 32-bit Memory Data Register 4B (MDR4B buffered) is a buffer between input data from the CBMMX and the output data to the B Bus Multiplexer. The register is selected by decoding of process field C Bus destination operands and by gating developed on the Cache card from memory commands. The register output is always enabled.

The 8-bit Current Halfword Buffer (CHBF) accepts the high order byte from MDR0 or MDR1 as the CH (Current Halfword). The buffer is always enabled and outputs the data (an address or index for a Branch to Next macro-instruction) as BCH0-7 to the Branch Multiplexer and Same Address Multiplexer on Control Memory.

2.5.3 Work Registers, Indirect Counter, And Indirect Register

The input data to the 32-bit general Work Registers 1 And 2 (WK1 And WK2)

is from the C Bus Multiplexer (CB0-31). Whether WK1 or WK2 is selected depends upon the decoding of process field C Bus destination operands. Access to the 32-bit word from WK1 or WK2 is controlled by process field B Bus operand selection and the output data is sent the B Bus Multiplexer.

The 8-bit Indirect Register Multiplexer (IREG MUX) input comes from MDR0 or MDR1 via the Current Halfword Buffer as CH8-15, or from the C Bus as CB24-31. A Branch to Next or Branch to Next (Execute) macro-instruction selects the CH8-15 inputs for the Current Halfword. All other instructions select the CB24-31 inputs. The outputs go to the Indirect Register Counter.

The 8-bit binary Indirect Register Counter (IREG Counter) input data comes from the IREG Multiplexer. The counter is disabled during a Branch to Next or Branch to Next (Execute) instruction, or Indirect Register Load instruction, and will cause the outputs to equal the inputs. During a Move And Increment IREG instruction (move A bus operands or B Bus operands to C Bus) the counter is up-counted. A Move And Decrement IREG instruction will cause the counter to be down-counted. Outputs go to the Indirect Register and the A Bus Stack Addressing logic as IR0-7, and to the B Bus Multiplexer as IR4-7.

The 8-bit Indirect Register (IREG) is a work register used for indirect Stack addressing. Input data comes from the IREG counter and output data goes to the B Bus Multiplexer. The only control for the IREG is the process field B Bus IREG operand.

2.5.4 B Bus Multiplexer

The 32-bit B Bus Multiplexer (BMX) collects data from several sources, including WK1, WK2, IREG and IREG Counter, Address Multiplexer (MG0-31), MDR0-1, or MDR4-B. Output data, BB0-31, is used at the Binary Arithmetic Logic Unit (BALU) and the Decimal Arithmetic Logic Unit (DALU).

2.5.5 Binary Arithmetic Logic Unit, Decimal Arithmetic Logic Unit, And C Bus Multiplexer

The Binary ALU (BALU) consists of eight 4-bit high speed parallel arithmetic logic units. Each ALU has a complexity of 75 equivalent gates per chip. The eight chips are cascaded to allow 32 bits (one word) of data to be acted upon as a whole. Controlled by four function select inputs and a Mode control input, it can perform 16 possible logic operations or 16 different arithmetic operations. The Mode control input will determine whether all internal carries are inhibited and the device performs logic operations (Or, Nor, Exclusive Or, And, Nand, or Compare) on the individual bits, or whether the carries are enabled and the device performs arithmetic operations (Add, Subtract, Compare, or Double) on the two 4-bit words. BALU operations, whether logical or arithmetic, are completed within one system clock period.

The Decimal ALU (DALU) consists of eight 4-bit high speed binary coded decimal (BCD) arithmetic units. The eight chips are cascaded to allow 32 bits (one word) to be acted upon as a whole. Depending on the state of the Add/ Subtract control, the unit produces the BCD sum or difference of two decimal numbers. A decimal addition is performed by adding the A Bus to the B Bus and placing the results on the C Bus. A decimal subtract operation (B minus A) is performed by internally adding the 9's complement of the A Bus to the B Bus and placing the result on the C Bus. ALU operations are completed within one system clock period.

The 32-bit C Bus Multiplexer (CMX) receives data from either the Decimal Arithmetic Logic Unit or the Binary Arithmetic Logic Unit for transmission on the C Bus as CB0-31. The DALU is selected for output during any of the four decimal instructions. Otherwise, the output will be from the BALU. C Bus data is used at the C Bus Main Memory Multiplexer, Program Mask Register, Work 1 And 2 Registers, Stack, Indirect Register Multiplexer, Virtual Memory Address Register, T-RAM Address Latch, and Memory Address Multiplexer.

2.5.6 Program Mask Register And Virtual Memory Address Register

The 8-bit Program Mask Register (PMR) is dedicated to part of the Linkword macro and is used with Linkword as a B Bus operand for Arithmetic Logic Unit input. The C Bus (CB0-7) is used as input to the PMR when the PMR is accessed, along with the Virtual Memory Address Register, during Move operations. Together PMR and VMAR compose the Linkword. CB0-7 is also used as data input to the PMR during a Write Control Memory operation. The CM RAM address (CB18-31) is set into the Virtual Memory Address Register and then forwarded to the Control Memory Address Buffer to become RA0-13. CB0-7 is moved from the PMR as data to be written and is sent on to Control Memory as RD0-7. Program Mask Register bits 0 And 1 are used with Condition Code instructions.

The 24-bit Virtual Memory Address Register (VMAR) is dedicated to Virtual Addresses of current halfwords in the macro-instruction stream. Input to the VMAR comes from the C Bus as CB8-31. Used as a B Bus operand source for Arithmetic Logic Unit input, VMAR outputs go to the Address Multiplexer for transfer to the B Bus and ALUs.

As a C Bus operand destination register, VMAR outputs are sent to the T-RAM as a Page Frame number entry or to the Control Memory Address Buffer as addresses. These addresses, in conjunction with data from the Program Mask Register, will be used when writing Control Memory.

VMAR can be incremented by two to allow the next halfword to become current. There are several micro-instructions which use the current halfword as an Arithmetic Logic Unit input or as the input for a multiway branch. VMAR incremented by two occurs during a Branch to Next or Branch to Next (Execute) micro-instruction.

2.5.7 Control Memory Address Buffer And Control Memory Data Buffer

The 14-bit Control Memory Address Buffer (RABF) will gate 14 bits of

address (VMAR10-19 and CB28-31) from the Virtual Memory Address Register to the Control Memory as RA0-13 for a Write Control Memory instruction.

The one-byte Control Memory Data Buffer (RDBF) transfers data as RD0-7 between the Program Mask Register and the Control Memory. The buffer is enabled during a Write Control Memory instruction.

2.5.8 Memory Operation Overviews, Memory Address Multiplexer, And Memory Address Registers 0, 1, And 2

General Memory Operations Overview

The CP can initiate only one memory read or write operation for each micro-instruction. CP memory read or write requests rely on a physical address contained in a Memory Address Register (MAR) and data contained in a Memory Data Register (MDR). There are three MARs (MAR1, MAR2, and MAR3) and five MDRs (MDR0, MDR1, MDR2, MDR3, and MDR4). The memory operation field (MOP) of the micro-instruction will select a Memory Address Register and indicate the type of read/write operation, address translation operation, or address ripple operation. Translation, changing virtual memory addresses into physical memory addresses, and Ripple, incrementing or decrementing a MAR value, are mutually exclusive.

A Word Alignment feature is used with MAR2 doubleword writes and translation operations if the virtual addresses are not word aligned. There are three micro-trap locations for address translation and three micro-trap locations for word alignment. An address translation trap has priority over a word alignment trap. (Refer to TABLE 2A, VS-100 TRAP ADDRESSES.)

Read and Write Overview

The read operation uses the selected Memory Address Register contents at the start of the micro-instruction. The CP must wait for the data to be returned before resuming micro-instruction execution. Error returns for read

operations are handled by micro-traps during the micro-instruction. Buffered read memory support is provided for MAR0 and for MAR1 by having 2 MDRs associated with one MAR. The MDRs receive either the even or odd addressed word when a buffered read operation is performed. The write operation uses MAR2 and MDR4 contents at the start of the micro-instruction. The CP can continue program execution without waiting for memory operation completion. Asynchronous error returns for write operations are handled through the External Condition Register on the System Bus Controller.

Translation Overview

When a translation operation changing virtual memory addresses into physical memory addresses is performed, no memory read or write operations are allowed. The translation is coded by specifying a No Op in the memory operation portion of the memory operation field and a translation operation in the translation/ripple field of the MOP. The Translation RAM, after translating the virtual address, supplies the physical addresses for the three Memory Address Registers. The Memory Address Register select field indicates the destination MAR of the physical address. MAR0, MAR1, and MAR2 support read translations while MAR2 supports read and write translations.

Ripple Overview

The Memory Address Register ripple operation involves a small increment or decrement of the MAR value. All three Memory Address Registers support ripple operations. The ripple operation is specified by the Translation/Ripple portion (CM27-29) of the memory operation field format. The ripple operation for the MARs only affects the low order 12 bits of the MAR value and any carry or borrow beyond 12 bits is lost. If a memory read or write operation is also requested, then the ripple occurs after the memory operation has been initiated. A ripple operation always involves a corresponding Page bit to indicate that the MAR address has or has not crossed a 2K memory page boundry. If the 2K boundry has been crossed, a new address must be supplied.

The 32-bit Memory Address Multiplexer (MAMX) supplies data to the Memory Address Registers from either the Translation RAM and the Translation Address Latch (as a Page Frame number and a location within the page) for Translation operations, or from the C Bus (CB0-31) for read or write operations.

Memory Address Registers 0, 1, And 2

The CP uses the three Memory Address Registers (MARs) with the five Memory Data Registers (MDRs), grouped as follows:

The 24-bit Memory Address Register 0 (MAR0), with MDR0 and MDR1, is dedicated to accessing halfwords from the macro-instruction stream. The buffered MDRs provide overlapped macro-instruction fetching. Only three memory operations affect MAR0. A Read Translation operation with halfword alignment check is used when a new physical address is required for current halfword access because a Branch micro causes a new virtual address to be used. The address is a Page Frame number and location within the page. A Buffered Read operation follows a Read Translation and uses that physical address now in MAR0 to point to the data in memory to be read into MDR0 or MDR1. After the operation has been initiated, a count of four will be added to the contents of MAR0. (MAR0 will be rippled plus four.)

A Word Conditional Read operation allows prefetching of the next word in the macro-instruction stream. The condition is that neither MDR0 or MDR1 is full. The word addressed by MAR0 will again be read into MDR0 or MDR1 and MAR0 will be rippled plus four.

The 32-bit Memory Address Register 1 (MAR1), with MDR2 and MDR3, provides read only access for Main Memory operands. Several memory read operations, including byte, word, word conditional, and multi-conditional reads, are supported by MAR1. A byte read will cause data to be placed in the low order byte position of MDR2 with the three high order byte positions of MDR2 set to zero. Data from a word read will also be placed in MDR2. A word conditional read places the word into MDR2 or MDR3 with the condition that the new MAR

address be within the same 2K memory area (Page 1) as the initial MAR address. If the MAR address is not within the same 2K memory area, a Page boundary has been crossed and a new virtual address must be supplied. No read or ripple will be performed. A multi-conditional read also places the word into MDR2 or MDR3, again depending on the 2K memory area plus the state of the two low order bits of MAR1. MAR1 supports plus one or four ripples, or minus one or four ripples, as indicated by the memory operation field, for conditional and multi-conditional reads.

The 32-bit Memory Address Register 2 (MAR2), with MDR4, is available for general, non-buffered read and write access of Main Memory. MAR2 supports byte, word, byte conditional, and word conditional reads as well as byte and word writes. All data is read into and written from MDR4. A byte read will cause the data to be placed in the low order byte position of MDR4 with the three high order byte positions of MDR4 set to zero. The byte and word conditional reads are the same as MAR1 except that the 2K memory area is Page 2. If the MAR address is not within the same 2K memory area, a Page boundry has been crossed and a new virtual address must be supplied. No read or ripple will be performed. MAR2 supports plus one or four ripples, or minus one or four ripples, as indicated by the memory operation field for conditional reads. A byte write (Read Modified Write) uses the data in low order byte position of MDR4. For a word write operation, the internal counters of MAR2 are disabled. MAR2 then operates as a straight forward gate by allowing its outputs to follow its inputs when the register receives a clock pulse.

2.5.9 Address Multiplexer and Memory Address Latch

The 32-bit Address Multiplexer (ADMX) receives input from the Program Mask Register and Virtual Memory Address Multiplexer, or from one of the three Memory Address Registers. ADMX input selection is based on the micro-instruction process field B-Bus operand for input from PRM and VMAR, and the MAR-select portion of the memory operation field for inputs from the Memory Address Registers. The Address Multiplexer output is sent to the B Bus

Multiplexer for input to the Arithmetic Logic Units, or to the Memory Address Latch as Main Memory addresses.

The 24-bit Memory Address Latch (MAL) consists of three eight bit latches with the outputs always enabled. Input is from the Address Multiplexer and output is transfered to the Cache as Main Memory addresses, MA0-23.

2.5.10 Translation RAM Address Latch, Translation RAM, Reference/ Change Table, And Translation RAM Multiplexer

The input to the 24-bit Translation RAM Address Latch (TAL) is 13 bits (CB8-20) of the virtual address from the C Bus (C Bus micro-code operation output), of which 12 bits are used to address a Page Frame in the Translation RAM. The TAL also forwards the 11 low order bits (CB21-31) of the virtual address to the Memory Address Multiplexer as the location within the page. The TAL outputs will be available for the Translation instruction group and two micro-instructions (MVN and MVX) from the Move instruction group.

Translation RAM

The physical Main Memory storage capacity of the VS-100 is currently limited to 2 Megabytes. Because the VS-100 uses Virtual Memory techniques, Main Memory can be made to appear much larger. The translation of virtual (disk) addresses to physical (Main Memory) addresses is performed by the CP. Three elements recognized by the Operating System during translations are segments, pages, and page frames.

A segment is a block of contiguous disk storage. There are three types of segments. The first type (Segment 0) is 512K bytes containing supervisory routines and data for the Operation System. The second type (Segment 1) is 512K bytes for each user program. The third type (Segment 2) is 4K to 512K bytes (in 4K increments) for each users data. A page is 2K of contiguous bytes of disk storage space within the user program or data segments, and a page frame is a Main Memory area exactly large enough to contain a disk page.

Since the system is intended to operate in a multi-task, multi-user environment, it is necessary to have a mapping mechanism to direct the CP to the pages of the tasks being executed. The CP uses a 4K x 16-bit local Translation RAM (T-RAM) to perform the mapping (translation) of a 24-bit virtual memory address into its current corresponding 24-bit physical Main Memory address. Each T-RAM entry (a C Bus operand destination from the Virtual Memory Address Register) contains a 13-bit page frame number, a fault bit, and read and write protect bits. These correspond to a particular page within the total virtual address space. The Translation operation addresses the T-RAM entry using the 12 bits (TRA0-11), or 4K, of the virtual address (C Bus micro-code operation output) from the Translation RAM Address Latch.

Reading and writing the RAM is controlled by the Load T-RAM instruction. The 13-bit page frame number read from the T-RAM is concatenated with the low order 11 bits of the virtual address (location within the page) from the Translation Address Latch at the Memory Address multiplexer to create the 24-bit physical Main Memory address. If the operation traps on an invalid virtual address (fault), the micro-instruction can be restarted if the T-RAM entry can be updated; otherwise, a page fault interrupt is generated. A trap will also be taken if the page is protected against being read or over-written.

The T-RAM can be monitored to provide rapid clearing of T-RAM entries for a user whose time slice has expired, while allowing entries for other users to remain. Monitoring occurs by segment and is based on a flag bit associated with the segment. The current users entries in the T-RAM are faulted when a different virtual address space is to be accessed. The CP will store these virtual addresses in the second half of the CP Stack when servicing a T-RAM fault. The CP micro-program maintains a counter of the monitored entries. The Stack is read one word at a time to get the virtual address for clearing each T-RAM entry when that users time slice has expired.

The CP maintains a table for each page frame entry in the T-RAM to record a reference bit, indicating a page was recently used, and a change bit indicating the contents of page were modified. An 8K by 2-bit Reference And

Change Table (RCT) RAM is responsible for maintaining the table. The reference bits tell the operating system what pages have not been used recently and could be written over with new pages. The change bit allows the operating system to determine what pages have been modified and should be written back onto disk to make room in memory for new pages. These two R and C bits (M2BI and M2HI) are updated to reflect the page frame status during each MOP translation process. Addressing the RCT is done by using the Page Frame Number from the T-RAM entry. An entry can be cleared or inspected by micro-instructions.

The 13-bit Translation RAM Multiplexer (TRMUX) normally passes the selected T-RAM entry to the Memory Address Multiplexer. However, if the selected entry should be faulted indicating that it is invalid, then the virtual address from the T-RAM Address Latch used for addressing the T-RAM is routed directly to the Memory Address Multiplexer by the TRMUX.

2.6 VS-100 MAIN MEMORY

The VS-100 Main Memory (Figure 2-5) consists of up to eight memory cards (modules) with each card containing 64K words or 256K bytes. A minimum of two cards are required. Each memory card is logically divided into four groups of 16k words. The memory uses the Mostek 16K (16,384) x 1 bit Dynamic RAM chip. Total maximum memory capacity is 2 Megabytes at present although, when 64K RAM chips become more readily available, total capacity will increase to 8 Megabytes. Addressing is already available for accessing this potential 8 Megabytes.

2.6.1 Control Signals

Main memory control signals are generated on the SBC (System Bus Controller) portion of the Cache card due to the physical limitations of the SBC card. (Refer to paragraph 2.8.8, Main Memory Control.) They are RAS (Row Address Strobe), CAS (Column Address Strobe), CEN (Column Enable), R/W (Read/Write), two WPs (Write Pulses), MS1-4 (Module Select #), and REF (Refresh). The Main Memory cycle runs synchronously with the SBC cycle.

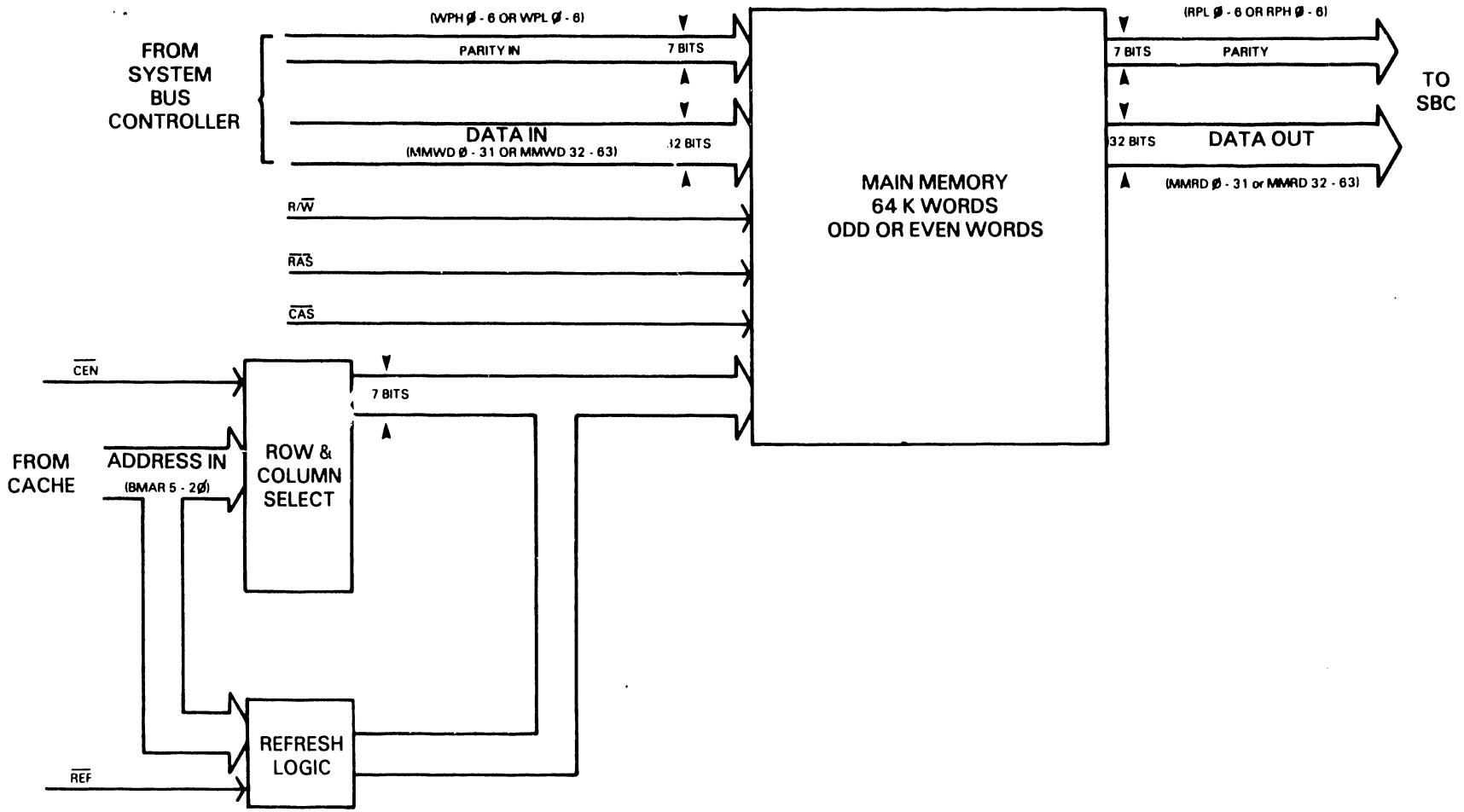


Figure 2-5
VS-100 MAIN MEMORY

2.6.2 Memory Write And Read

CP or Bus Adapter data transfer to and from the memory is controlled by the SBC. The basic memory data word is 32 bits with a 7 bit ECC (Error Correction Code) field. Write operations allow any card to be accessed seperately for word writes, or in pairs for doubleword writes. The SBC can align units of 1, 2, 4, or 8 bytes, but only words or doublewords can be written. All read operations cause a doubleword (8 bytes or 64 bits) to be accessed with the first card (0) containing the even addressed word, and the second card (1) containing the odd addressed word. Hence, the necessity of a minimum configuration two cards.

For a memory write operation, the even word of data (MMWD0-31) and parity (WPH0-6), and/or the odd word of data (MMWD32-63) and parity (WPL0-6) from the SBC will be written into the RAM by the WP (Write Pulse) as long as R/W (Read/Write), CAS (Column Address Strobe), and RAS (Row Address Strobe) are active. Row and column addresses are available coincident with RAS and CAS. WP is generated on the Cache for the odd and/or even word cards. This allows a single word write without having to encode an address to distinguish between cards in a pair. When the Check ECC (Error Correction Code) diagnostic feature is active, all data RAMs will be disabled and writing will only be allowed into the parity RAMs.

For a memory read operation, the even word of data (MMRD0-31) and parity (RPH0-6), and the odd word of data (MMRD32-63) and parity (RPL0-6) will be read from the RAM and transfered to the SBC, when the Column Address Strobe is active, as long as Read/Write remains inactive. Again, row and column addresses are available coincident with RAS and CAS.

2.6.3 Addressing

Memory addresses are supplied by the CP or the BA. Of the 24 address bits available (BMAR0-23), (Refer to TABLE 2C) only sixteen (BMAR5-20) are used at the memory card. BMAR0-2, the high order bits, will not be used until 64K RAM

chips are installed. BMAR3-4 are decoded on the Cache into card pair selection (Module Select #). BMAR5 and BMAR6 directs the Row Address Strobe to each group of 16K words as long as the Module Select (MS#) for that pair of cards is active.

Fourteen address bits (BMAR7-20) are required to decode one of the 16k memory locations. The seven row addresses (BMAR7-13) are latched into the RAM's internal row address decoder by the Row Address Strobe. The seven column addresses (BMAR14-20) are selected by CEN (Column Enable). These addresses are then latched into the RAM's internal column address decoder by the Column Address Strobe. The RAM does not use the low order column address bit (BMAR20) for column decoding. It is used for internal data bus selection. BMAR21-23 are not used because the lowest accessable addressed unit is eight bytes (two words).

TABLE 2C VS-100 MAIN MEMORY ADDRESSES

BMAR BIT	HEX	COMMENT	MEMORY CAPACITY
BMAR 0		NOT USED	
BMAR 1		NOT USED	
BMAR 2		NOT USED	
BMAR 3	3	MODULE SELECT	1MEG BYTES
BMAR 4		MODULE SELECT	512K BYTES
BMAR 5	F	16K WORD GROUP	128K BYTES
BMAR 6		16K WORD GROUP	64K BYTES
BMAR 7		ROW ADDRESS	32K BYTES
BMAR 8		ROW ADDRESS	16K BYTES
BMAR 9	F	ROW ADDRESS	8K BYTES
BMAR 10		ROW ADDRESS	4K BYTES
BMAR 11		ROW ADDRESS	2K BYTES
BMAR 12		ROW ADDRESS	1K BYTES
BMAR 13	F	ROW ADDRESS	512 BYTES
BMAR 14		COLUMN ADDRESS	256 BYTES
BMAR 15		COLUMN ADDRESS	128 BYTES
BMAR 16		COLUMN ADDRESS	64 BYTES
BMAR 17	F	COLUMN ADDRESS	32 BYTES
BMAR 18		COLUMN ADDRESS	16 BYTES
BMAR 19		COLUMN ADDRESS	8 BYTES
BMAR 20		COLUMN ADDRESS	RAM BUS SELECT
BMAR 21		NOT USED	
BMAR 22		NOT USED	
BMAR 23		NOT USED	

2.6.4 Refresh

Because a dynamic RAM will not store data indefinitely, the data must be written back at least once every two milliseconds. Rewriting the RAM is done internally and is called "refresh". The VS-100 will refresh every 15 microseconds. This operation has priority over all other memory operations.

When a refresh cycle (REF) is initiated, RAS (Row Address Strobe) will be enabled for all RAMs, as they require refresh with only RAS cycles. Row refresh addresses (BMA6-13) are supplied by the SBC portion of the Cache. All CAS inputs will be disabled by the refresh. Normal memory operations also accomplish refresh.

2.7 VS-100 SYSTEM BUS CONTROLLER

The System Bus Controller (SBC) (Figure 2-6) provides a 64-bit data path between the Cache Memory, Main Memory, and the Bus Adapter(s), and acts as a data "traffic cop". It directs a doubleword of data read from Main Memory to the Cache Memory, or to the Bus Adapter with alignment of any one of four single bytes of one word for the CP; directs and aligns units of 1, 2, 4, or 8 bytes of data to be written to memory from the CP or BA; and directs IPC (Interprocessor Communications) data between the CP and BA.

The SBC is responsible for correcting a single bit memory error for each 32-bit word of the doubleword that is read, notifying the Control Memory or BA if multi-bit read errors occur, and generating parity for a Main Memory write. It logs parity errors in the BTL (Bus Transaction Log), and controls and records "external" events using the ECR (External Condition Register).

2.7.1 Data Error Correction

Both the CP and the BA are responsible for generating their own individual memory requests. When a memory read operation is initiated, a doubleword will be transfered to the S.B.C from memory and the SBC will attempt to correct a

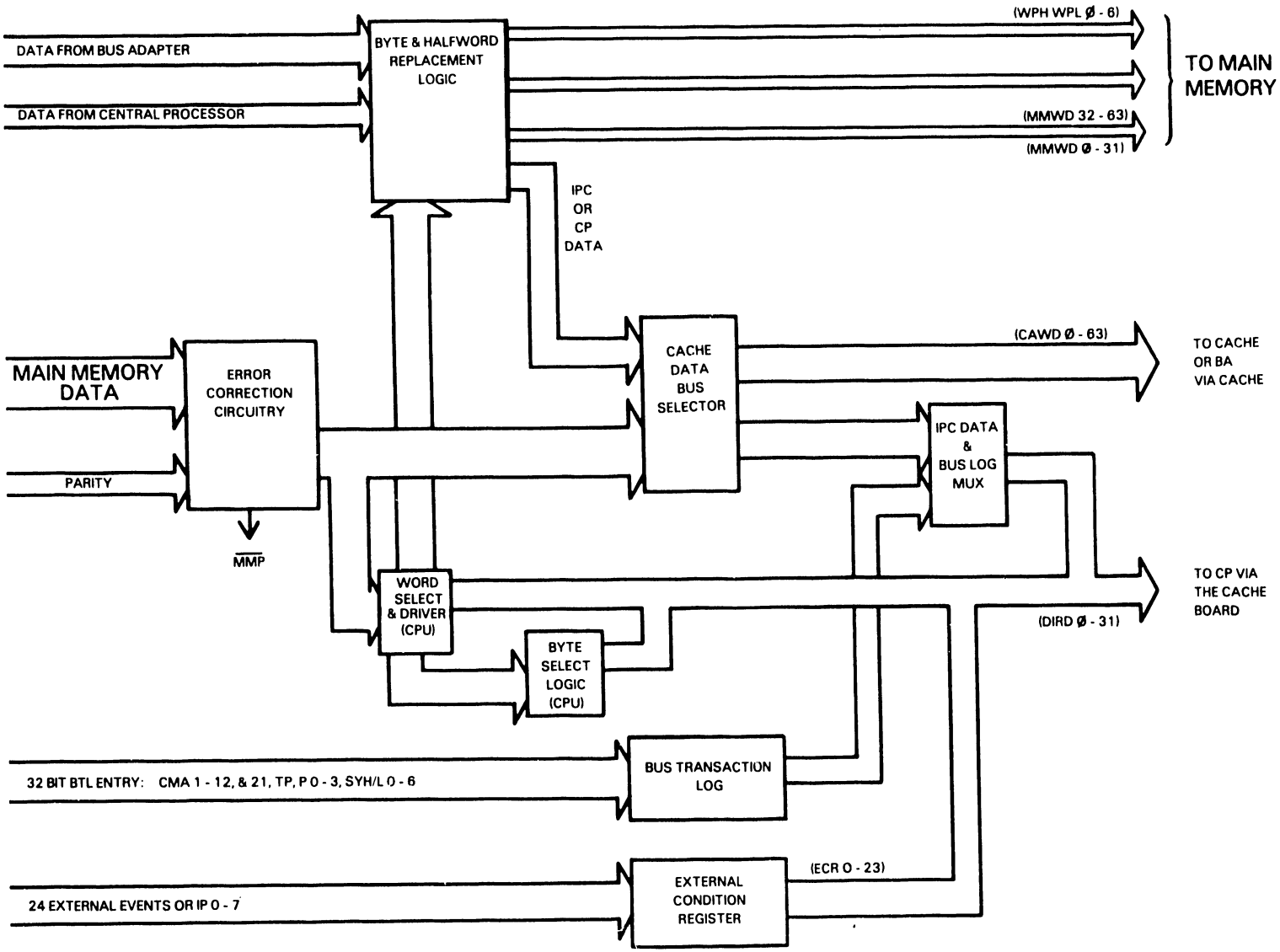


Figure 2-6
VS-100 SYSTEM BUS CONTROLLER

single bit error for each 32-bit word of the doubleword. This is done by circulating the doubleword (MMRD0-63) and parity bits (RPH/LO-6) through ECC (Error Correction Code) circuitry. If a bad bit is detected by data and parity bit comparison, it will be corrected by an inversion process.

If an uncorrectable multiple bit error is detected, a Main Memory Parity Error condition will notify the Bus Adapter of the error during a BA operation, or set a trap (MMPT) in Control Memory for a CP read operation. If a CP Read Modify Write (1-byte) is in progress, the error indication will set a bit in the ECR to notify the CP and prevent the memory control portion of the SBC (located on the Cache) from generating Write Pulse.

As a diagnostic feature, the ECC can be disabled by setting a bit (ECR5) in the External Condition Register. If the bit is reset, the SBC reports an error to the CP only if a multiple bit error is detected. Single bit errors are corrected with no indication given to the CP. If the bit is set, then the SBC reports both single and multiple bit errors to the CP as they occur.

2.7.2 Read Data Path

Data that has been processed by the ECC must be directed to the CP and the Cache, or to the BA. The CP requested a doubleword read because the Cache did not contain the current data. The C.P requires one word of the doubleword, but the entire doubleword will be used to update the Cache. A Bus Adapter request for a doubleword read will deliver the full doubleword of data to the BA.

As the C.P needs only one word of the doubleword of corrected data, a decision must be made as to which word the CP will receive. This decision is made at the Word Selector and is software controlled by Memory Address bit 21 (MA21) which was available during the read instruction. If MA21 is reset, the even word of the doubleword will be selected and if MA21 is set, the odd word will be chosen. The selected word can also be used during certain read modify memory write operations.

Following the word selection, an opportunity exists to rotate, or "swap" any one byte of the selected word into the low order byte position. The Byte Selector conveniently manipulates the byte here, otherwise the destination register of the data word (CP Memory Data Register #2) would have to be searched for the selected byte. This feature is software controlled by Memory Address bits 22 and 23 (MA22-23), which are used for selecting bytes and halfwords. Following the word select (and byte "swap", if requested), the word is sent through the IPC Data and Bus Log Multiplexer to the Cache card, as DIRD0-31, for transfer to the CP.

At the same time the CP word is being selected, the doubleword is being transfered to update the Cache. The doubleword will pass through the Cache Data Bus Selector, which can only distinguish between the doubleword or IPC data (or CP data that will update the Cache on a CP write). The SBC does not know the destination of the doubleword, CAWD0-63. It can be for either the Cache or the BA. This decision is controlled by logic on the Cache card.

A BA read request will send the corrected doubleword directly to the Cache Data Bus Selector. Again, the SBC does not know or decide the destination of the doubleword.

2.7.3 Data To Main Memory

Data to be written to Main Memory is from either the CP or the Bus Adapter, or it is corrected data, via the Word Selector, to be written back to memory as a replacement byte or halfword. The S.B.C will align the data in 1, 2, 4, or 8-byte increments, and write a word or doubleword to memory with correct parity. The word of data from the CP will also be made available to the Cache because the Cache must be updated when Main Memory is written. Because of timing constraints, the BA does not write to Cache Memory. Interprocessor Communications (IPC) data between the CP and BA will also be present, but will not be written to memory.

A CP write memory request allows one word of CP data to be admitted to the

Byte and Halfword Replacement logic. It is up to the Byte and Halfword logic to decide on a 1-byte replacement, using read data from the CP Word Select logic, for a Read Modified Write operation, or allow an unmodified CP word write. This is also software controlled by Memory Address bits 22 and 23 (MA22-23).

Another decision here is to permit a CP word or doubleword write. If a single word is to be written, the data will be available to memory as an even word (MMWD0-31) and an odd word (MMWD31-63). The memory control, by decoding the write instruction, will generate the appropriate even or odd word Write Pulse. For a doubleword write, the first word will be latched in the SBC's Main Memory output drivers while the CP transfers a second word. The memory control will produce both an even and odd word Write Pulse.

As the word(s) are prepaired for memory, they will also be made available to the Cache Data Bus Selector to allow updating of the Cache Memory.

A Bus Adapter write memory operation is similiar to the CP write operation. The BA is allowed the normal byte replacement, and also a halfword replacement. The halfword is necessary because the IOP is a halfword device. The halfword or byte will be corrected memory data from the Word Selector and will be aligned by MA22-23.

The BA is also permitted a word or doubleword write. The complete BA doubleword is available to memory as MMWD0-63 and no second data transfer is needed. The memory control will again generate even and/or odd word Write Pulse(s). The word(s) will NOT be made available to the Cache Memory.

2.7.4 Interprocessor Communications

Interprocessor Communications are used for generalized message passing and interrupt service between all processors (CP, BA, and SBC). Thirty two bit messages are transferred directly between processors without using Main Memory facilities. IPC transmission control is generated on the SBC portion of the Cache card.

If no write operations are in progress, the data word appearing at the Byte and Halfword Replacement logic will be Interprocessor Communications data, transmitted on the normal data paths, from the CP or the BA. IPC data is left untouched and is sent to the Cache Data Bus Selector. The Cache Data Bus Selector will select the IPC data word originating at the BA and transfer it through the IPC Data and Bus Log Multiplexer, as DIRD0-31, to the CP via the Cache card.

An IPC data word from the CP for the BA will also pass through the Cache Data Bus Selector, but will be directed to the Cache card as CAWD31-63. Logic on the Cache card will determine that this IPC word will be sent to the BA.

2.7.5 External Condition Register

The External Condition Register is a twenty four bit register (ECR0-23) maintained by the SBC to record or control "external" events. (Refer to Appendix E.) The register is divided into 5 groups. Events recorded include write parity errors, invalid memory addresses for write operations, Cache hits and misses, rejection of IPC data words, and Bus Adapter "Attention Needed" requests. The full ECR can be read by the Read ECR micro-instruction. The 24-bit output of the ECR passes through the IPC Data and Bus Log Multiplexer and on to the low order 24-bit positions of CP Memory Data Register #4, as DIRD0-31, via the Cache card.

To control events, 4 of the groups can be written by a Write ECR micro-instruction. These include initializing the BA, and enabling and disabling Cache or ECC.

2.7.6 Bus Transaction Log

The Bus Transaction Log (BTL) is a local RAM storage area, configured as 256 32-bit words. It is used to record all hard and soft ECC errors with the associated upper twelve Main Memory address bits (CMA1-12) generated by the CP or the BA. Main Memory Address bits 3-4 will point to the Main Memory card

while bits 5-6 will indicate the row select. Also recorded will be Cache data and tag parity errors, with addresses, and whether the odd or even Cache word is in error. The BTL can be read with the Read BTL diagnostic micro-instruction.

2.8 VS-100 CACHE MEMORY

The Cache Random Access Memory (Figure 2-7) provides high speed data read access for the CP by acting as a buffer between the CP and Main Memory. A complete Cache cycle is 160 nanoseconds while a Cache read only cycle is 80 nanoseconds, compared with the 480 nanosecond cycle time for a Main Memory doubleword read. The Cache is in synchronization with the memory control.

The Cache contains a subset of the same data found in Main Memory and allows the CP to read this subset data, making it unnecessary for the CP to wait for data read from Main Memory. To accomplish this, the Cache has a write tnrough strategy so when the CP writes to Main Memory, via the System Bus Controller, the Cache entry is fully updated.

The effectivness of the Cache is measured by the "hit" raito, or how often the requested data is found in Cache. The hit ratio will increase as job execution proceeds because the job tends to reuse data it has already referenced. A "miss" indicates the requested data was not found in Cache. The CP then requests a doubleword read directly from Main Memory and that doubleword will be written to Cache to keep the Cache updated.

Because of timing constraints, the Bus Adapter does not write to Cache Memory. When the BA modifies a data word which is also buffered in Cache, the Cache entry is invalidated because it is no longer current.

The Cache can be disabled and enabled by setting a bit (ECR8) in the External Condition Register on the SBC. When the Cache is disabled, all CP read accesses are satisfied directly with a Main Memory doubleword read. When the Cache is enabled, it contains stale data and must be cleared, as it is upon system initialization.

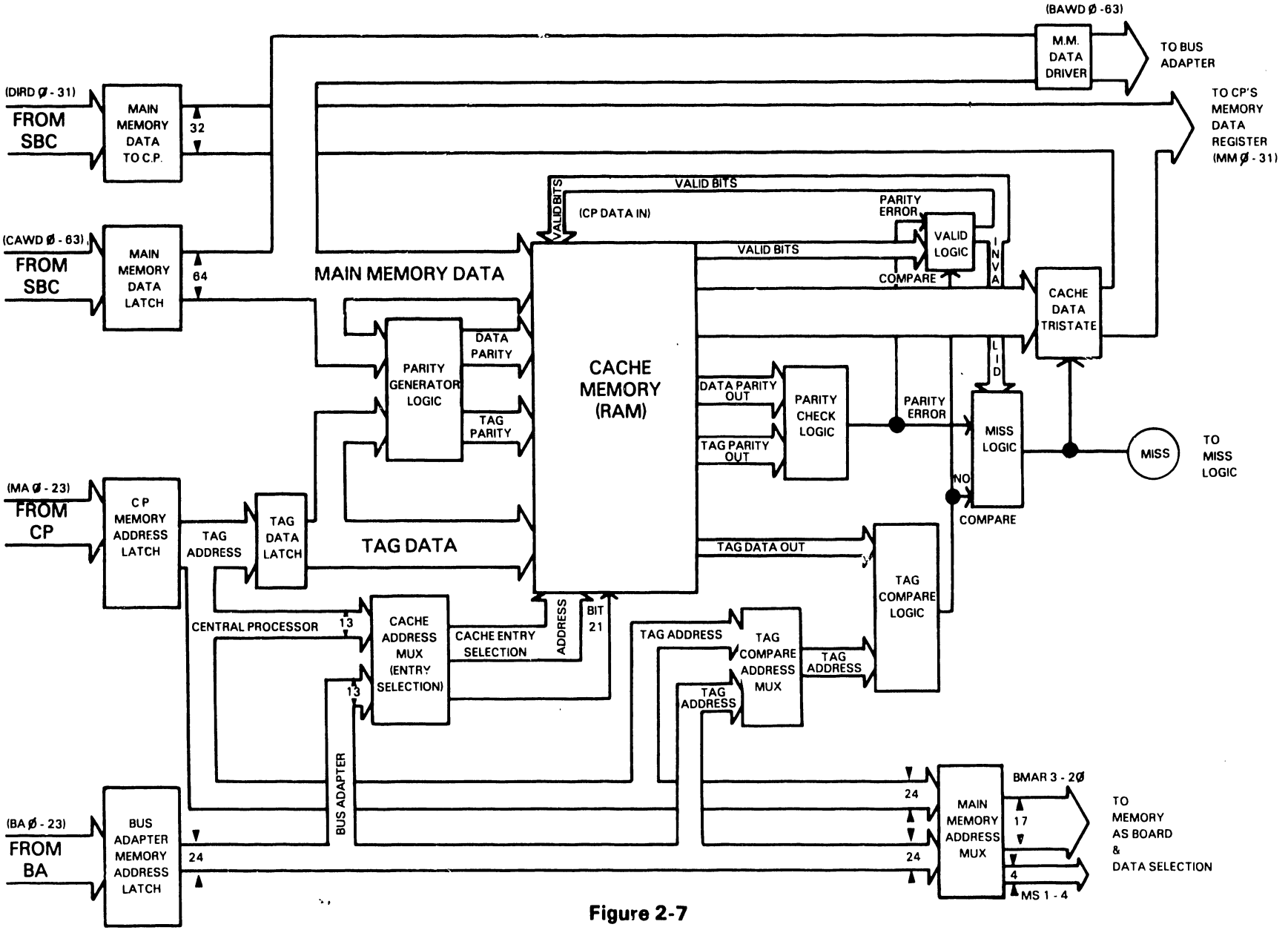


Figure 2-7
VS-100 CACHE MEMORY

Cache parity errors, which also cause a doubleword read, are recorded in the Bus Transaction Log on the SBC, but are otherwise invisible to the CP microprogram. The only indication of Cache parity errors is system access degradation.

Two other sections of the Cache card, although not part of the Cache Memory, are the Main Memory control and the IPC (Interprocessor Communications) control logic. This logic is actually SBC logic, but is placed on the Cache card due to the physical limitations of the SBC card.

2.8.1 Configuration

There are four thousand Cache Memory entry pairs (32K bytes), and each pair contains an even word entry and an odd word entry. Each entry contains a 32-bit data word and a 9-bit "tag" field. The tag, which is used for address comparison, identifies the actual physical address of an entry. As each location in Cache can contain the corresponding Main Memory location and every 32K increment of the location to the end of memory, the tag indicates which 32K increment is resident in Cache.

Of the 24 bits of physical address available, MA0-23 from the CP or BA0-23 from the BA, the 12 "middle" bits (MA9-20 or BA9-20) are used to select a Cache entry pair. One of the remaining 12 bits (MA21 or BA21) is used to select the even or odd Cache entry from the pair, and nine bits, (MA0-8) from the CP address, are used to compare tag fields of the selected entry. The low order 2 bits are ignored because the unit of access is one word.

2.8.2 Data Written To Cache

Data to the Cache can be written in 1, 4, or 8-byte increments. There are two types of 8-byte writes. This data, appearing at the Main Memory Data Latch as CAWD0-63, is either one or two words of CP data, or is a doubleword of memory read data, corrected by the SBC. The CP data appears here to update the Cache, and at the SBC for a normal one or two word CP memory write.

If the data is a doubleword of read data, then a Cache "miss" occured and the CP was forced to do a memory read access.

The doubleword of read data can also be for the Bus Adapter and it will not be written to Cache, but will be sent directly to the BA as CAWD0-63. This route of data to the BA is because of the convenience of locating hardware at this point.

The Cache will generate its own write pulses for 1, 4, or 8-byte writes, decoded from CP memory operation commands. When the Cache writes one byte it overwrites (replaces) one byte of a word already stored in Cache. The location of the byte to be written is software controlled by the tag identification and memory address bits MA21-23. MA21 controls the odd or even word selection while MA22-23 decide on the most or least significiant halfword and byte of the word. A 4-byte (word) write is also controlled by the tag and MA21. The 8-byte (doubleword) CP write is accomplished by tag comparison only when the CP transfers two words.

The second type of 8-byte write happens when the tags did not compare, the Cache missed, and the CP was forced to read a doubleword from Main Memory. This operation is done by default, when no CP write operation is decoded and Control Memory bit 24 (MCM24) is on indicating that the CP requested a Cache read. The tag indicates the correct location to be written and MCM24 produces two write pulses to write the entire doubleword. Four bits of parity are generated and written to Cache for every word.

If the BA writes a doubleword to Main Memory, the memory address of the write is compared to the corresponding address and tag in Cache, and, if there is a match, the data in the Cache location is invalidated.

2.8.3 Data Read From Cache

The read instruction for the Cache is a normal memory read operation determined by the decoding of a Control Memory word. The word of data

addressed in Cache for transfer to the CP is made available, through the Cache Tri State Drivers, to the CP's Memory Data Register on the MM0-31 lines. Nothing prevents Main Memory from being read, but the data word returned (DIRD0-31) is effectively blocked from the CP at the Tri State Drivers.

2.8.4 Main Memory Addresses From BA And CP

Both the CP and the BA produce a 24-bit Main Memory address for their respective Main Memory operations. The CP addresses (MA0-23) pass through the CP Memory Address Latch while the BA addresses (BA0-23) pass through the BA Address latch. The addresses are sent to the Main Memory Address Multiplexer and the memory operation in progress (CP or BA) will gate the correct set of addresses through to Main Memory as BMAR3-20. Missing bits BMAR0-2 and BMAR21-23 have been explained under Main Memory Addressing, paragraph 2.6.3.

These addresses are also made available to the Cache Address Multiplexer for Cache entry pair selection in an attempt to locate the subset of data in Cache. Twelve of the "middle" address bits (MA9-20 or BA9-20) pass through the multiplexer for Cache entry selection. The BA addresses are only used to invalidate the cache entry, not to write a new entry.

2.8.5 Tag Compare (MISS) And Parity

The nine tag bits (TWD0-8) from the CP memory address are written into the Cache RAM, through the Tag Data Latch, at the same time that the Cache word is written. One bit of parity is also written for each tag entry. When the CP requests a Cache read of a selected entry, the tag bits of the current CP memory address are compared, through the Tag Compare Address Multiplexer and Compare Logic, to the tag bits of the selected Cache entry. If the tag comparison is not correct, the MISS signal is generated and sent to the Control Memory to stop the CP t and L clocks, if no BA is requesting a Main Memory cycle, as a Main Memory doubleword read must be initiated. The MISS is also recorded in the External Condition Register of the System Bus Controller only for diagnostic purposes as the miss will be invisible to the micro program.

As the tag was being compared, both the tag and data parity bits are being checked in the Parity Check logic. If a parity error occurs, MISS is generated regardless of the tag comparison results as bad parity indicates an unusable word. A Main Memory doubleword read will be initiated.

2.8.6 Valid And Invalid Cache Locations

Because of timing constraints, the BA will not access any data in Cache. But, if the BA writes to Main Memory and that particular Main Memory location's data was in Cache, then the data in Cache will no longer be current or "valid". When the BA does a Main Memory write, the Cache checks to see if that Main Memory location also resides in Cache. If it does, a Cache location "valid" bit is written into the Cache RAM to indicate that the Cache entry is no longer valid. There is an even and odd valid bit for the even and odd cache word. If the CP requests a read of that cache location, the valid bit will cause a Cache MISS and a Main Memory doubleword read will be initiated. The Cache word will be updated and will again become valid.

2.8.7 Main Memory Data Direct To CP

Data from Main Memory to the CP, caused by a Cache miss and a doubleword read, passes through the Cache card on the way to the CP. The data word, DIRD0-31, is directed from the SBC at the same time that the doubleword from the SBC for the Cache update arrives at the Cache card. The word can also be IPC data from the BA to the CP. In that case, the word will not be used to update Cache. Any data from the Cache will not be permitted through the Cache Tri State Drivers.

2.8.8 Main Memory Control

The Main Memory Control logic on the Cache card (Figure 2-8) is actually an System Bus Controller function, but is located on the Cache card due to the physical limitations of the SBC card. Both the CP and the Bus Adapter can request a variety of memory read and write operations, and both encode their

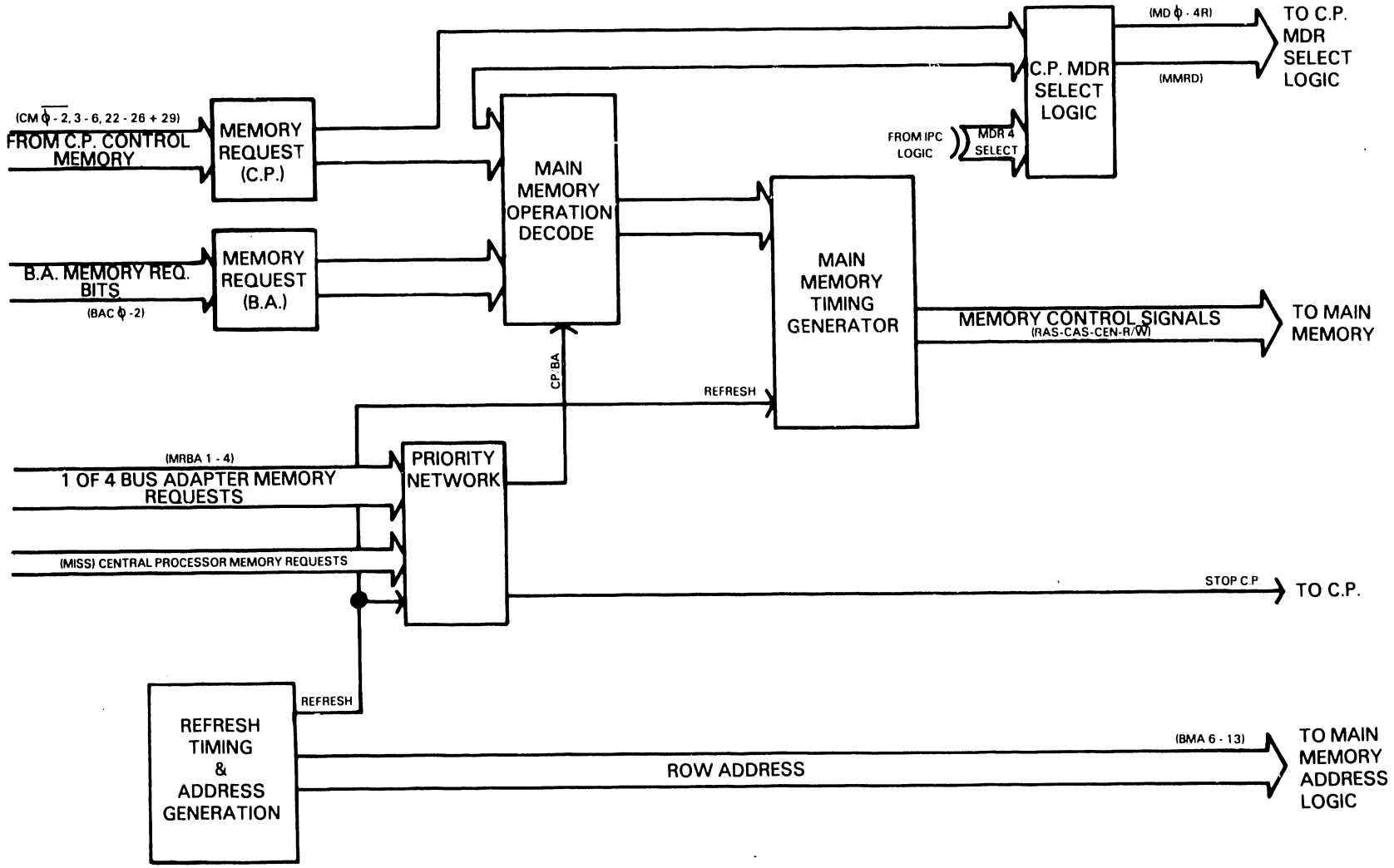


Figure 2-8
VS-100 MEMORY TIMING

own memory operations and requests. The BA, because it must support the I.O. Processor, is permitted a 16-bit (halfword) memory write that the CP is not allowed. The CP has the lowest memory priority and does not require a request line because the memory control defaults all unused memory requests to the CP. Each B.A has a request line.

The Main Memory Operation Decoder decodes the CP memory operation from a Control Memory word when no BA memory requests are present. The BA Priority Network chooses the BA with the highest priority (MRBA1-4) and allows the Main Memory Operation Decoder to decode the BA operation from bits BAC0-2.

The Main Memory Timing Generator produces all the memory control signals discussed under Main Memory Control Signals, paragraph 2.6.1. The CP MDR Select Logic allows the selection of the appropriate CP Memory data Register for memory read commands. The STOP CP signal, halting the 't' time clocks of the CP, will be present if there was a Cache MISS because the data in the Cache was invalid and must be updated; if control was busy or doing a refresh and a CP write command was issued; or, if a BA memory request was in progress and a CP write command was issued.

Main Memory refresh logic is also part of the memory control. It provides refresh control and row addresses (BMAR6-13) to the Main Memory at 15 micro second intervals. Refresh has priority over all other requesting processors.

2.8.9 Interprocessor Communications Control

IPC (Interprocessor Communications) control logic (Figure 2-9) is also a System Bus Controller function but is located on the Cache card due to the physical limitations on the SBC. The logic is responsible for IPC message send and receipt control. The IPC feature has two basic functions. The first function allows two processors to communicate with each other without using Main Memory facilities, and the second function allows the I.O. Processor to interrupt the CP because the CP will not accept asynchronous messages from the IOP. The CP, Bus Adapter, and SBC are all considered processors.

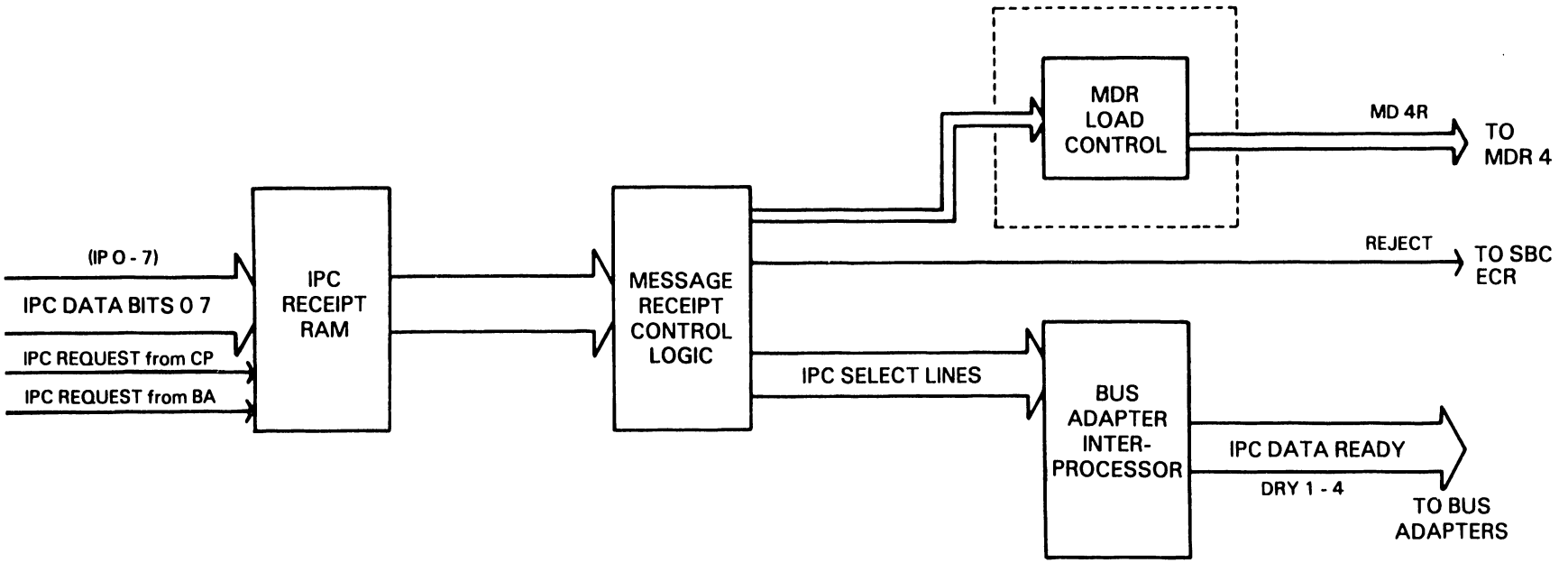


Figure 2-9
VS-100 INTERPROCESSOR COMMUNICATION

The IPC data words are 32-bit messages created by a processor. There are two types of messages (dialogs); CP initialization of the BA, and I/O initialization and interrupts. The BA is used for buffering and routing the message.

The IPC receipt RAM stores IPC data bits 0-7 in the form of a message receipt control, a sending processor number, and a destination processor number. The RAM does not store the actual message. The Message Receipt Control Logic allows acceptance or rejection of any IPC message from any processor. The MDR Load Control alerts MDR#4, the IPC memory data register for the CP, of a pending message. The Bus Adapter IPC Ready Control produces the proper Data Ready (DRY1-4) signal to a particular Bus Adapter. DRY1-4 corresponds to Bus Adapter 1-4. DRY will be used at the BA to gate the IPC data into the B. A. IPC Data Latch.

2.9 VS-100 BUS ADAPTER

The Bus Adapter (Figure 2-10) is an intermediate processor serving as an interface between the 16-bit Input/Output Processor and the 64-bit VS-100 system bus. The VS-100 can support one or two Bus Adapters, although provisions have been made for four BAs. Each BA supports up to eight IOPs. The BA has access to basic VS-100 memory and Interprocessor Communications (IPC) services, and is synchronized with the SBC. The main service the BA provides is data buffering. The IOPs use 16-bit write and read operations, while data is transmitted to and from memory 64 bits at a time. The BA blocks data going from the IOP to memory and unblocks data from memory for the IOP, effectively using the 64-bit high speed data bus during I/O operations.

The BA supports six words per IOP in a local RAM buffer/ register. The words are used to buffer memory or IPC data, and for holding physical addresses through which the IOP will access Main Memory. The BA generates a 24-bit physical Main Memory address from the 16-bit word supplied by the IOP, allowing access to the possible future 8 megabytes of memory.

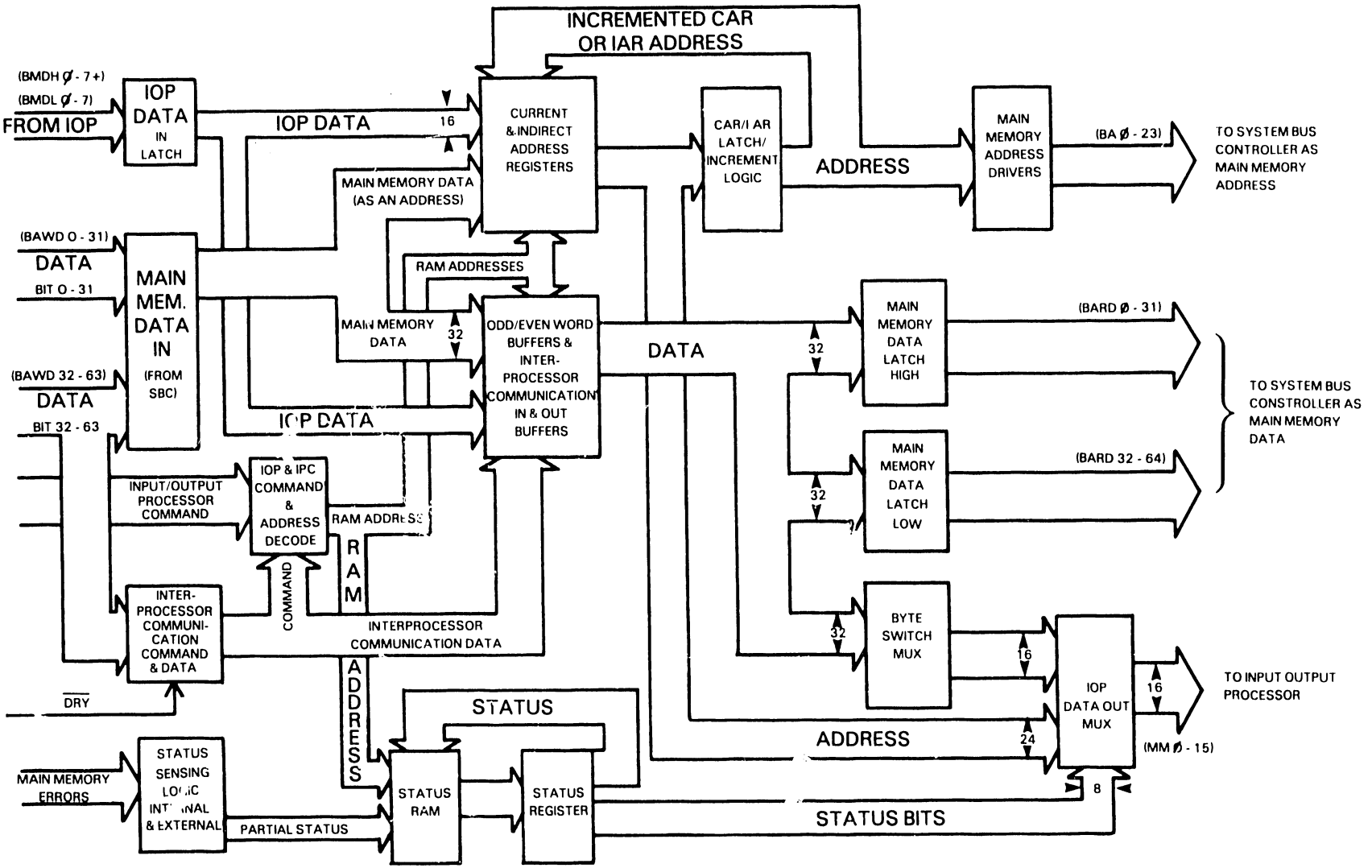


Figure 2-10
VS-100 BUS ADAPTER

Four groups of commands are developed by the IOP to control internal BA events and Interprocessor Communications, and to direct Main Memory operations. Four types of errors, plus other IOP status information, are logged in a one byte Status Register maintained on the BA. The IOP cannot directly set the full Status Register, but it can inspect the status byte. Under direction of the CP, IOP interrupts can be allowed or rejected by the BA. The BA also controls the priority of devices attached to the IOPs.

2.9.1 IOP Priority

The first two IOP positions on BA #1 are always reserved for disk devices. (Note that the present 210-7611 BA card will not support two disk IOPs, however, the future 7911 BA card will support two disk IOPs.) The disk devices, because of their high speed data transfer rates, must have memory access priority over all other I.O. devices. The BA must assign priority to the first disk IOP, but still allow the second disk IOP to share every other available memory access. This is accomplished by "conflict resolution" logic. The other IOP priorities are assigned on a decending IOP position basis. The priority assignment process is initiated when an IOP raises its memory request line.

2.9.2 IOP Instructions

After an IOP has requested a memory cycle and has received a memory grant from the BA in return, it can send a command, in the form of a CMBI (Control Memory Bus Interface) instruction, to the BA. The BA will decode the CMBI into one of four instruction groups; Read/Write group, Address Control group, State Control group, or Interprocessor Communications group.

Each group is sub-divided into several instructions. The instructions will be used to control data and address transfers between the IOP and Main Memory, or in the case of IPC instructions, between the IOP and the CP. Each command contains a number of "type codes" and "qualifier bits" to further define the instruction execution.

2.9.3 Encoding of BA Memory Commands

The BA must have read and write access to Main Memory to support the IOPs. The BA memory commands are encoded on the BA from the IOP instructions and are decoded on the Main Memory control portion of the SBC, located on the Cache card. The BA memory operations include Write 1, 2, 4, or 8 bytes, and Read 8 bytes.

2.9.4 Write IOP Data To Main Memory

To accomplish 1,2, 4, or 8-byte writes, the IOP will use 1, 2, or 4 halfword data transfers to the BA. The BA will either send a byte directly to the S.B.C for writing to Main Memory, or store the halfwords of data in the odd or even word buffers until all transfers are complete.

After the BA has granted the IOP memory request and decoded the IOP instruction, data is received from the IOP as two bytes, BMDL0-7 and BMDH0-7, at the IOP Data In Latch. A 1-byte Read Modified Write will cause the high order byte (BMDH0-7) to be transfered directly to the SBC with a memory address. The byte will be sent (as the low order byte BARD56-63) through the Main Memory Data Latch Low. The other 24 bits (BARD32-55) will all be zeros. The Main Memory Data Latch Low will be enabled when the BA requests a memory cycle and the data will be transfered to the SBC when the memory control is ready. This byte replaces a byte in a full word read from memory by the SBC and the SBC is responsible for positioning the byte within the word before the word is rewritten to memory.

Because the IOP is a 16-bit device, a halfword (2-byte Read Modified) write is permitted. Only a halfword will be loaded into an odd or even word buffer.

For a 4-byte (word) write, two data transfers from the IOP are required. The first transfer will load the least significiant halfword of the odd or even word buffer. The second transfer will load the most significiant halfword of the odd or even word buffer.

The loading of odd and or even buffers, for both halfword and word writes, is controlled by Current Address Register bits 21 (buffer select) and 22 (half word select within the buffer). Address bit 20 causes a write request to be issued to the SBC using the current address. Half words and word write data passes through Main Memory Data Latch Low.

For a 8-byte (doubleword) write, four transfers from the IOP are needed and four odd and even word buffers are loaded. Memory Data Latch High (BARD0-31) is used for the even word of an 8-byte write.

2.9.5 Addresses To Main Memory

Two types of addressing schemes, direct or indirect, are used by the BA to access Main Memory. Set Address, issued by the IOP, provides the mechanism where the IOP loads a 24-bit direct physical address into the Current Address Register before accessing a Main Memory area for reading or writing. Loading the physical address requires that the IOP load the least significiant byte of an IOP halfword, followed by a complete halfword, into the CAR as BMDL0-7 and BMDH0-7 via the IOP Data In Latch.

Set Address Indirect causes a packaged operation, including reading Main Memory, to be performed. When a Set Address Indirect is issued, the BA will use the 24-bit Indirect Address Register as a Main Memory address as long as no other memory operations are in progress. A Main Memory doubleword, consisting of addresses, is read by the BA as BAWD0-63 through the Main Memory Data In Latch. One word is selected by Current Address Register bit 22 while the other is discarded. Twenty four bits of the word are then placed in the CAR and the IAR is rippled plus 4. Set Address Indirect can be used by the IOP for effective access of an Indirect Address List.

The IOP (via the MM0-15 lines) can also fetch a 16-bit address (one of four halfwords) from the IAR/CAR before processing an IOP level interrupt operation. The CAR/IAR Latch/Incrementer can ripple the CAR plus 1 or plus 2 for sucessive memory operations, and ripple the IAR plus 4 for the next doubleword.

2.9.6 Main Memory Data To IOP With Byte Switching

The IOP read request causes the deblocking of the 64-bit data in the BA Odd/Even Word Buffer into 16-bit half words. When the Main Memory read is serviced, using a memory address from the Current Address Register, a doubleword of data is read from Main Memory and returned as BAWD0-63 to the Main Memory Data In Latch from the SBC. One odd or even buffer word is selected as determined by the state of Current Address Register address bit 21 (buffer select), while CAR bit 22 selects the half word from within the buffer. CAR bit 23 determines if the bytes within the halfword will be switched in the Byte Switch Multiplexer. This conforms to the firmware convention in the IOP.

The halfword output of the Byte Switch Multiplexer is sent to the IOP via the IOP Data Out Multiplexer as MM0-15. The CAR address is incremented 1 or 2, and if CAR bit 20 changes, then the next doubleword read is performed. Bit 20 changing indicates that the buffer has been emptied.

2.9.7 Interprocesser Communications

Interprocessor Communications (IPC) is used for generalized message passing and interrupt service between all processors (CP and BAs). Thirty two bit messages are transferred directly between processors without using Main Memory facilities. Each message must contain its own routing information. These messages are controlled by "dialogs", which are defined as a CP initiated SEND followed by a BA response. There are two classes and five types of IPC dialogs for loading and unloading registers, reading and disabling IOP interrupts, and performing diagnostic functions. The IOP is not directly involved with the dialogs. The BA maintains an IPC In register and an IPC Out register for buffering the IPC messages. The registers can be written and read on command from the IOP.

The IPC message, controlled by an IPC dialog and by the Send and Receipt logic on the Cache card, (paragraph 2.8.9, Interprocessor Communications

Control) enters the BA in the form of a seperate word of data (BAWD32-63) and transfers to the IPC Command And Data Latch. The message is entered into the correct IPC In register, selected by an IOP number. The register is read and the data is sent to the IOP, via the Byte Swap Multiplexer and the IOP Data Out Multiplexer, as MM0-15. An acknowledgement message is returned by the BA to the CP indicating that either the IPC In Register was loaded and no other message be sent, or that the IPC In Register was busy and the CP should repeat the message.

When the IOP has completed the task, (start I/O, halt I/O, or control I/O, etc.) it returns the IPC message through the IOP Data In Latch to the correct IPC Out register. An IOP interrupt request is activated by the BA and the CP will read the interrupt. The CP responds with a Give IPC Out register dialog and the data word will be sent from the register through the Main Memory Data Latch Low to the CP.

2.9.8 Status Register

The BA supports a status byte for each attached IOP. The status byte is held seperately from the other IOP register areas. These status bytes are maintained by the BA during the servicing of IOP commands. The IOP cannot set the full status byte directly, but it can inspect the value of the status byte. Main Memory command errors, IOP command rejection errors, and status bits ACT, MODE, PB, DWD, TOR, and IPCA are detected by the Status Sensing logic. (Refer to Appendix D, VS-100 Hardware Mnemonics.) The byte is stored in the Status RAM using an address developed from an IOP number. The RAM is updated by the Status Register and the status byte is sent to the IOP, through the IOP Data Output Multiplexer, as MM0-7.

CHAPTER 3

UNPACKING & INSTALLATION

CHAPTER 3
UNPACKING AND INSTALLATION

3.1 GENERAL

This chapter describes the procedures for unpacking, inspecting, and installing the VS-100 Mainframe. Included in this chapter are instructions for system interconnection and initial power-up. Refer to Chapter 4, Switches and Indicators; Chapter 5, Sysgen; Chapter 6, Maintenance and Adjustments; and Chapter 7, Removal/Replacement of this manual for further information needed to complete installation. Actual installation should not begin until the site requirements detailed in the following publications have been met:

1. VS Presale Guidelines & Use of the Physical Planning Guide. (A Customer Engineering publication)
2. VS Configuration Guide (WLI P/N 800-2100).
3. 2200VS Physical Planning Guide (WLI P/N 800-1106PG; Class. I.A.7)
4. Customer Site Planning Guide (WLI P/N 700-5978; Class. I.A.7).
5. Other pertinent documents in Category I.A.7.

3.2 SITE PREPARATION

Prior to installation, the following conditions must have been met:

1. All site plans must have been approved by both the customer and a Wang Service Representative.
2. All building alterations must have been completed and inspected.
3. All wiring, air conditioning, and TC modifications must have been completed and tested.
4. If the installation is an upgrade only (CPU replacement), the SALESMAN will ensure that serial devices replace all parallel peripherals
5. The salesman will also make arrangements to replace all 2260V 10-Mbyte Drives. These drives are NOT supported on the VS-100 System.

NOTE

It is the responsibility of the salesman to ensure that an upgrade site meets all necessary VS-100 specifications.

6. The CE will perform a pre-installation inspection two weeks prior to delivery. At this time, the CE will check the site for compliance with VS site specifications. The CE will bring any unsatisfactory conditions noted to the attention of the customer for correction.

NOTE

Before installation of a VS-100 can take place, the minimum specifications as described in the previously-listed publications should be met. Failure to meet these requirements can be cause for the installing CE to deem a site as unsuitable for the proper functioning of a VS-100 System.

3.3 INITIAL INSPECTION

Before unpacking the VS-100, check all packing slips to ensure that the proper equipment has been delivered (refer to the serial tag information below). After checking packing slips, inspect all shipping containers for damage (crushed corners, punctures, etc.). If damage is discovered during this or subsequent inspections, file an appropriate claim promptly with the carrier involved, and notify the WLI Distribution Center (Dept. #90), Quality Assurance Dept. Inform them of the damage, and arrange for equipment replacement, if necessary.

SERIAL TAG #	MEMORY SIZE (Bytes)
177-VS16F	512K
177-VS24F	768K
177-VS32F	1.0M
177-VS40F	1.2M
177-VS48F	1.5M
177-VS56F	1.7M
177-VS64F	2.0M

3.4 UNPACKING THE MAINFRAME

The Mainframe is shipped pre-assembled, covered by a corrugated cap and sleeve, and bolted to a shipping pallet. A new feature has been incorporated into this pallet making it easier for CE's to unload the Mainframe from it. With the use of a few simple tools shipped with the pallet, one end can be lowered to the floor forming a ramp, enabling the CE to roll the unit off the pallet to its permanent location. This and all other unpacking proced res are performed as follows: (See Figures 3-1 through 3-4.)

NOTE

Because of the size and weight of the Mainframe, it is recommended that the following procedure be performed by two persons.

1. Using snips, cut the bands encircling the shipping container.
2. Lift the corrugated cap from the top of the container.
3. Lift the corrugated sleeve from around the Mainframe.
4. Locate and set aside the package containing the jack-screws, plates, and T-nuts. (See Figure 3-1.)
5. Inspect the Mainframe for any obvious external damage. If damage is discovered, refer to Paragraph 3.3 for appropriate action.
6. Position the pallet so that the end with the removable cushion affixed to it faces in the direction the Mainframe will be moved. In the following text this will be referred to as the FRONT END of the pallet.
7. Using an adjustable wrench, remove the four bolts located under the pallet that secure the Mainframe to the pallet. (See Figure 3-2.)
8. Lower the chassis levelers located at the BACK end of the pallet until they are in firm contact with the surface of the pallet. This MUST be done to prevent the Mainframe from rolling off the pallet when the front end is lowered.
9. Lower the front end of the pallet as follows: (See Figure 3-3.)
   a. Insert a jack-screw into each of the pre-drilled holes on the pallet sides, and screw a t-nut onto the end of each jack-screw.
   b. Under each jack-screw, center a plate so that the nub at the end of the screw sits in the small hole in the center of the plate.

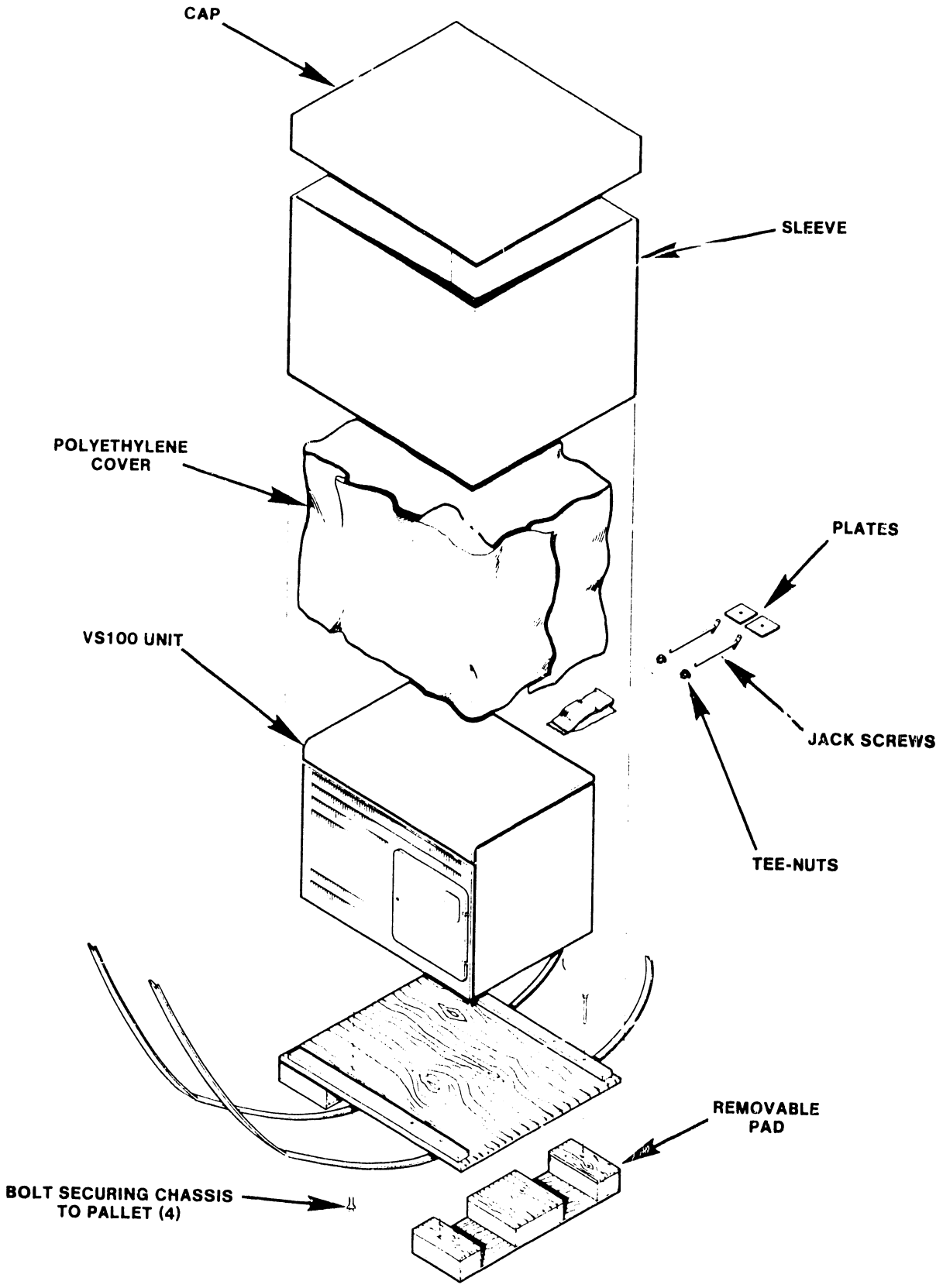


FIGURE 3-1 EXPLODED VIEW OF PACKAGED VS-100 MAINFRAME

c. Turn the T-nut counter-clockwise until it penetrates the bottom of the pallet. Once this is done, turn the jack-screw handle clockwise until the pallet front is raised ¼-inch off the floor.

d. Remove the two bolts securing the cushion to the pallet and remove the cushion. At this point, the front end of the pallet is supported entirely by the jack-screws.

e. Turn the jack-screws counter-clockwise to lower the pallet.

f. With the pallet front resting on the floor, raise the levelers on the Mainframe and carefully ease the Mainframe off the pallet.

10. Move the Mainframe to its permanent location and remove the protective polyethylene film. (See Figure 3-4.)

11. With the Mainframe in its permanent location, the unit must be raised off the casters and leveled. This is accomplished by adjusting the leveling-pad screw bolts located next to each caster until the Mainframe is lifted off its casters and is level with adjacent peripherals. Level the Mainframe as follows:

    a. Turn the leveling pads clockwise (down) until they support the full weight of the Mainframe.

    b. Adjust the leveling pads to align the unit with adjacent equipment. Ensure that the unit is not supported by the casters.

    c. If a bubble level is available, place it on top of the cabinet assembly and level the unit front-to-back and side-to-side. If a level is unavailable, align the unit by sight. Ensure that the Mainframe is level with no detectable rocking motion.

12. Once the Mainframe is in place and leveled, check that the service clearances are as follows:

a)	Front	36"	91.44cm
b)	Rear	30"	76.20cm
c)	Left	00"	00.00cm
d)	Right	00"	00.00cm

3.4.1 UNPACKING THE PERIPHERALS

Before proceeding, carefully unpack all peripherals according to procedures outlined in applicable maintenance manuals in Classification III. As each unit is unpacked, check it for any obvious shipping damage.

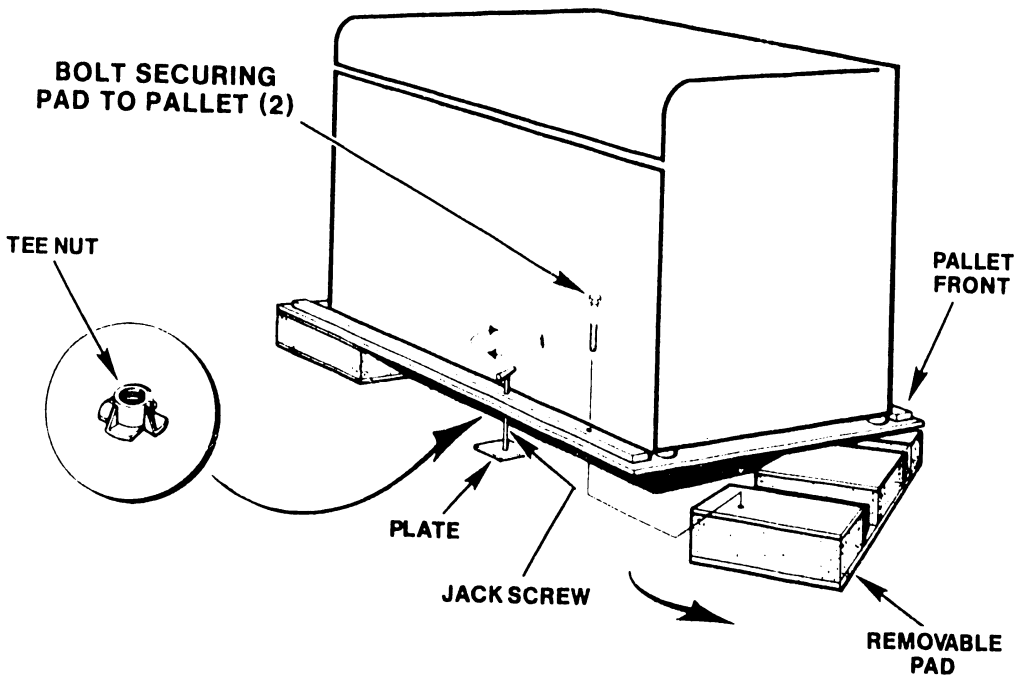


FIGURE 3-2 NEW SHIPPING PALLET WITH JACK-SCREWS IN PLACE

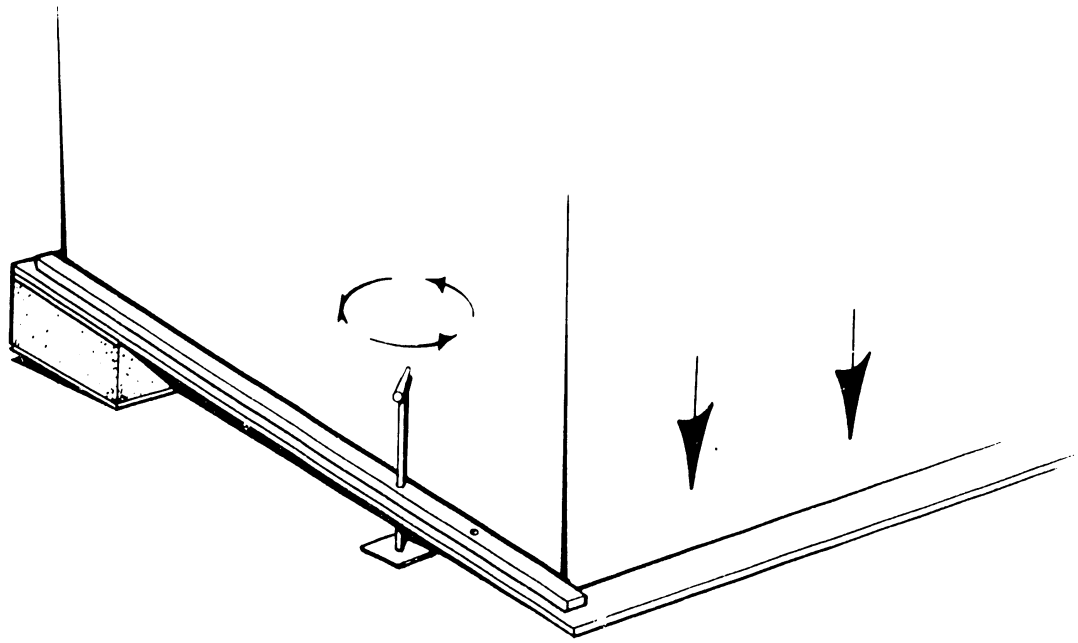


FIGURE 3-3 LOWERING THE PALLET FRONT END

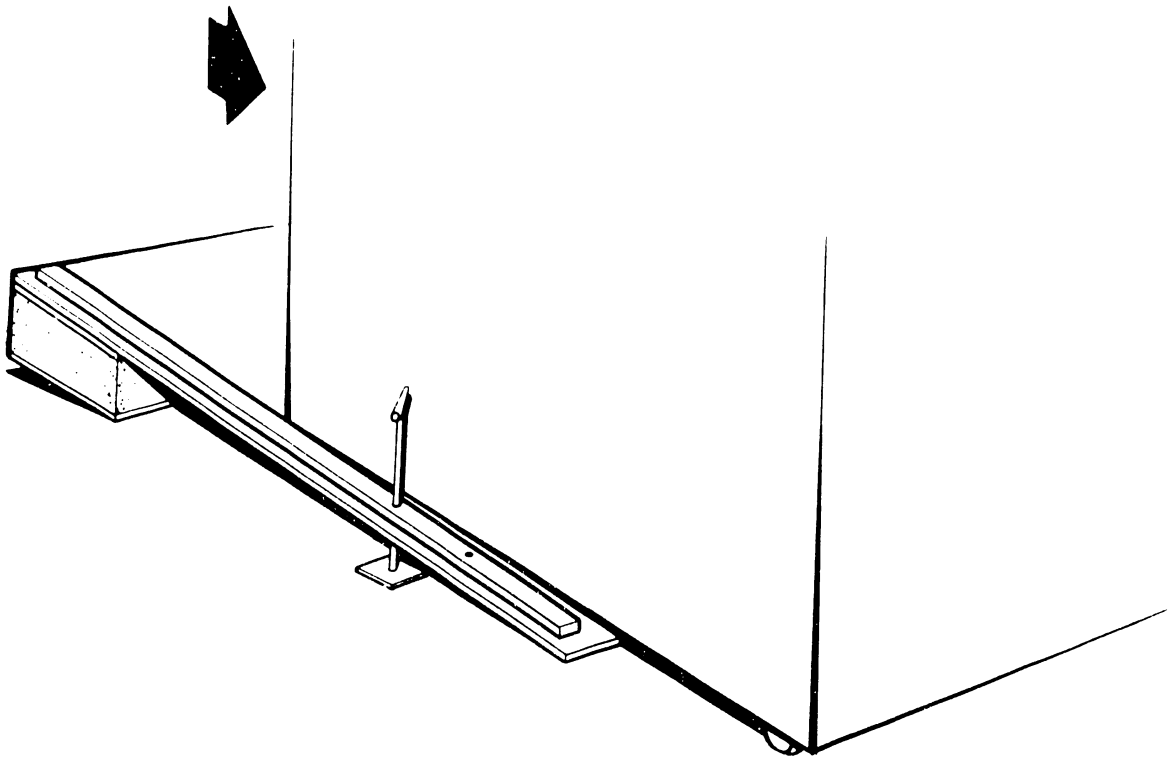


FIGURE 3-4 REMOVING THE MAINFRAME

3.5 INITIAL MAINFRAME INSPECTION

To ensure the integrity of the equipment, a detailed internal inspection must be performed before final installation of the System. Perform an internal inspection of the Mainframe, as follows: (See Figures 3-5 and 3-6.)

1. Remove the top and front covers, and lower the fan panel. (Refer to Chapter 7 for disassembly procedures.)
2. Inspect the interior of the Mainframe for packing material or such shipping damage as broken connectors and loose fastening hardware.
3. After confirming that the appropriate circuit cards have been shipped (refer to shipping list), remove all cards. (Refer to Chapter 7.)
4. Carefully inspect the motherboards and fans for obvious damage or loose connections.
5. Slide the power supply tray out from the Mainframe, and inspect the power supply assemblies for damage and loose connections. At this time, ensure that all power supply connections are tight.

6. If necessary, vacuum clean the unit.
7. After inspecting the power supplies, slide the tray back in place.
8. Do not re-assemble the Mainframe at this time.
9. If damage is discovered at any time during the inspection, follow the reporting procedure in Paragraph 3.3.

3.5.1 INITIAL PERIPHERAL INSPECTION

After inspecting the Mainframe, carefully inspect each peripheral according to procedures outlined in the applicable maintenance manuals in Classification III. If damage is discovered at any time during the peripheral inspection, follow the reporting procedure in Paragraph 3.3.

3.6 MAINFRAME INSTALLATION

The following paragraphs describe the procedures for checking and installing all VS-100 Mainframe circuit cards in the CP and I/O Motherboards. Perform this procedure before INITIAL system power-up or before any subsequent power-up where system status is either unknown or suspect.

3.6.1 CP MOTHERBOARD CIRCUIT CARD INSTALLATION

Refer to Chapter 4 for information pertaining to switch-settings on the different circuit cards used in the CP Motherboard. Install all cards in the Mainframe with their component sides facing left when viewed from the chassis front. Refer to Figures 3-7 through 3-14 when installing the following cards.

CAUTION

Exercise care when installing the large, flexible VS-100 cards. Ensure that all cards are seated properly in the appropriate CP Motherboard sockets. Do not damage the sockets when inserting cards.

---

1. Install the 210-7602 Control Memory card (see Figure 3-8) in Motherboard slot #1.
2. Install the 210-7600 CP1 (A-Bus) card (see Figure 3-9) in Motherboard slot #2.

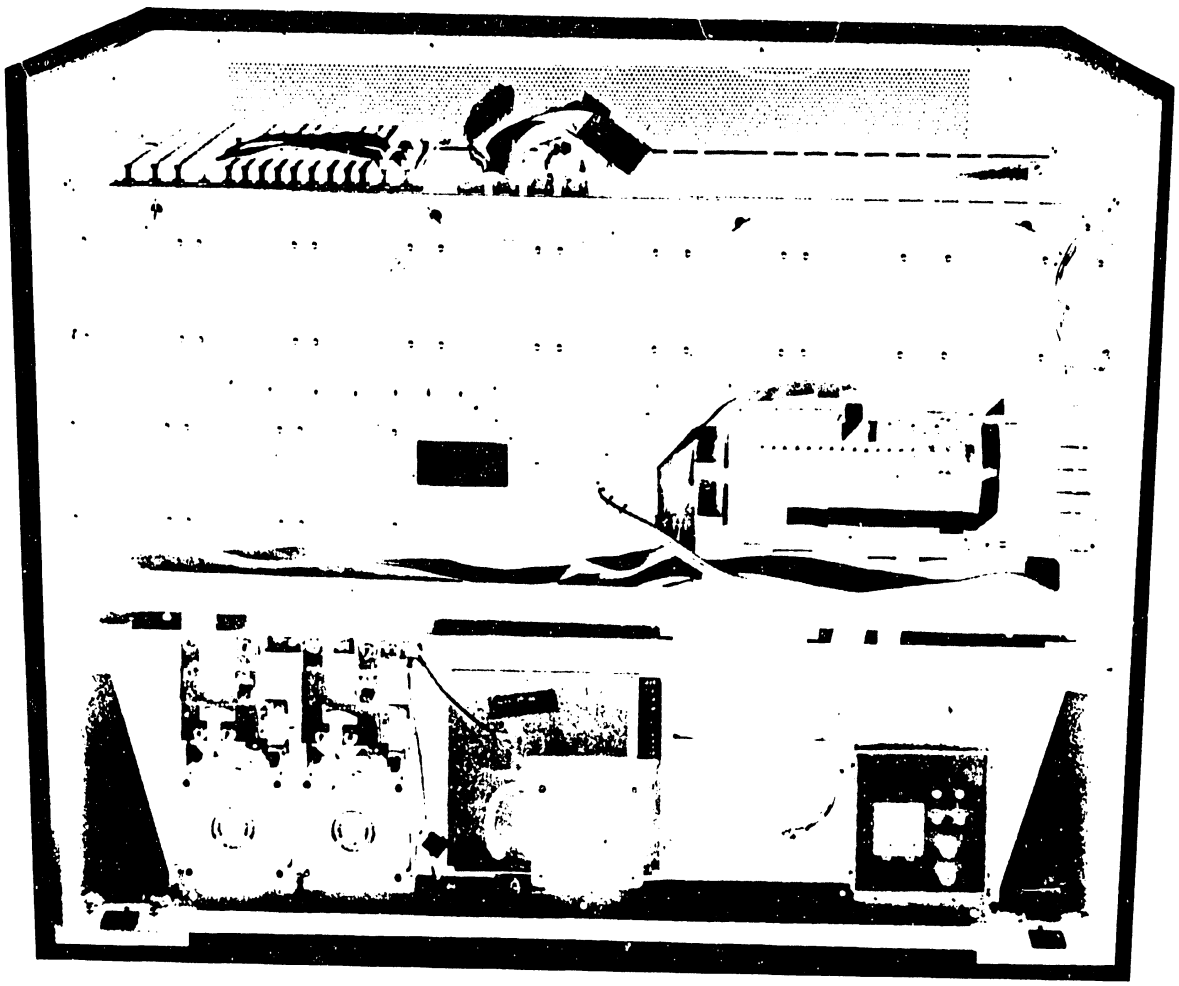


FIGURE 3-5 VS-100 WITH TOP AND FRONT COVERS REMOVED

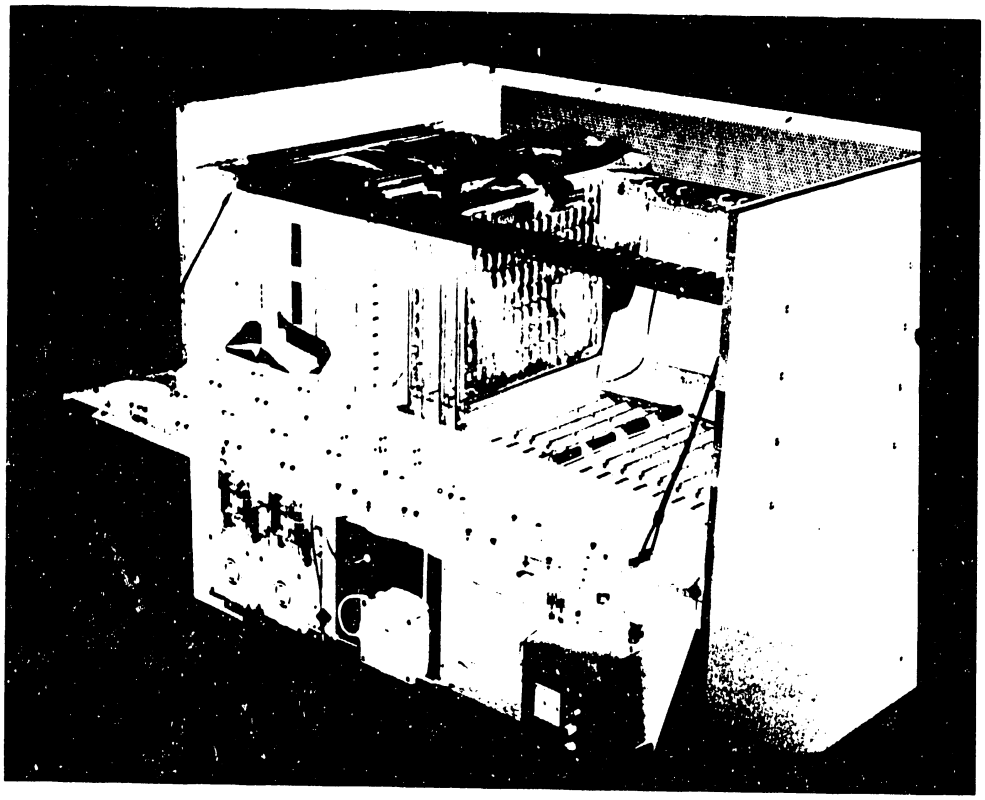


FIGURE 3-6 VS-100 CPU WITH FAN ASSEMBLY LOWERED

3. Install the 210-7601 CP2 (B-Bus) card (see Figure 3-10) in Motherboard slot #3.
4. After checking memory-size switch settings on the Cache Memory card per Chapter 4, connect the 16-pin ribbon cable from L46 of the 210-7604 Cache Memory card to L83 of the 210-7605 System Bus Controller card
5. Install the 210-7604 Cache Memory card (see Figure 3-11) and the 210-7605 System Bus Controller card (see Figure 3-12) as one unit in Motherboard slots #4 and #5, respectively.
6. Install the 210-7603 Main Memory cards (see Figure 3-13) in pairs starting at Motherboard slot numbers 6 and 7. Cards in even-numbered slots (6, 8, 10, 12) contain even data words; cards in odd-numbered slots (7, 9, 11, 13) contain odd data words. The total number of PAIRED memory cards determines Main Memory size (refer to Table 3A). Ensure that the number of memory cards equals desired memory size (refer to work request). Do NOT leave open slots between memory cards.

7. Install a 210-7611 Bus Adapter (BA) card (see Figure 3-14) in Motherboard slot #15: the card in this slot becomes Bus Adapter #1. If the system is to contain a second BA card, install it in Motherboard slot #14: the card in this slot becomes BA #2. Refer to Paragraph 3.6.3 for internal cable connections.

TABLE 3A MAIN MEMORY SIZE

SLOT #'s	PAIR #	MEMORY SIZE*	COMMENTS
6 and 7	0	512 Kbyte	Slot 6 is memory board 0 (even words). Slot 7 is memory board 1 (odd words).
8 and 9	1	1 Mbyte (Maximum)	Slot 8 is memory board 2 (even words). Slot 9 is memory board 3 (odd words).
10 and 11	2	1.5 Mbyte (Maximum)	Slot 10 is memory board 4 (even words). Slot 11 is memory board 5 (odd words).
12 and 13	3	2 Mbyte (Maximum)	Slot 12 is memory board 6 (even words). Slot 13 is memory board 7 (odd words).

* Except for pair 0 which must always be 512 Kbyte, this is maximum memory size with the specified number of memory cards. Using half-loaded cards results in smaller memory sizes than indicated by this table; that is, with half-loaded memory cards, pair 0 fully loaded and pair 1 half-loaded will equal 750 Kbyte, and so forth.

3.6.2 I/O MOTHERBOARD CIRCUIT CARD INSTALLATION

Refer to Chapter 4 of this document and the appropriate documents in Category VI.B for information pertaining to IOP switch-settings. Ensure that the device address for each IOP is unique to that assembly. Install all assemblies in the Mainframe with component sides facing left when viewed from the chassis front. Refer to Figure 3-7 when installing assemblies.

IOP assemblies are assigned to I/O Motherboard slots on a priority basis. Each assembly is weighted according to IOP type, as follows:

NOTE

In the VS-100, the OS requires that I/O slot #0 on BA1 be reserved for a high-speed disk drive IOP (22V28). BA1 tekes priority over BA2 when devices on both boards try to access the CPU simultaneously.

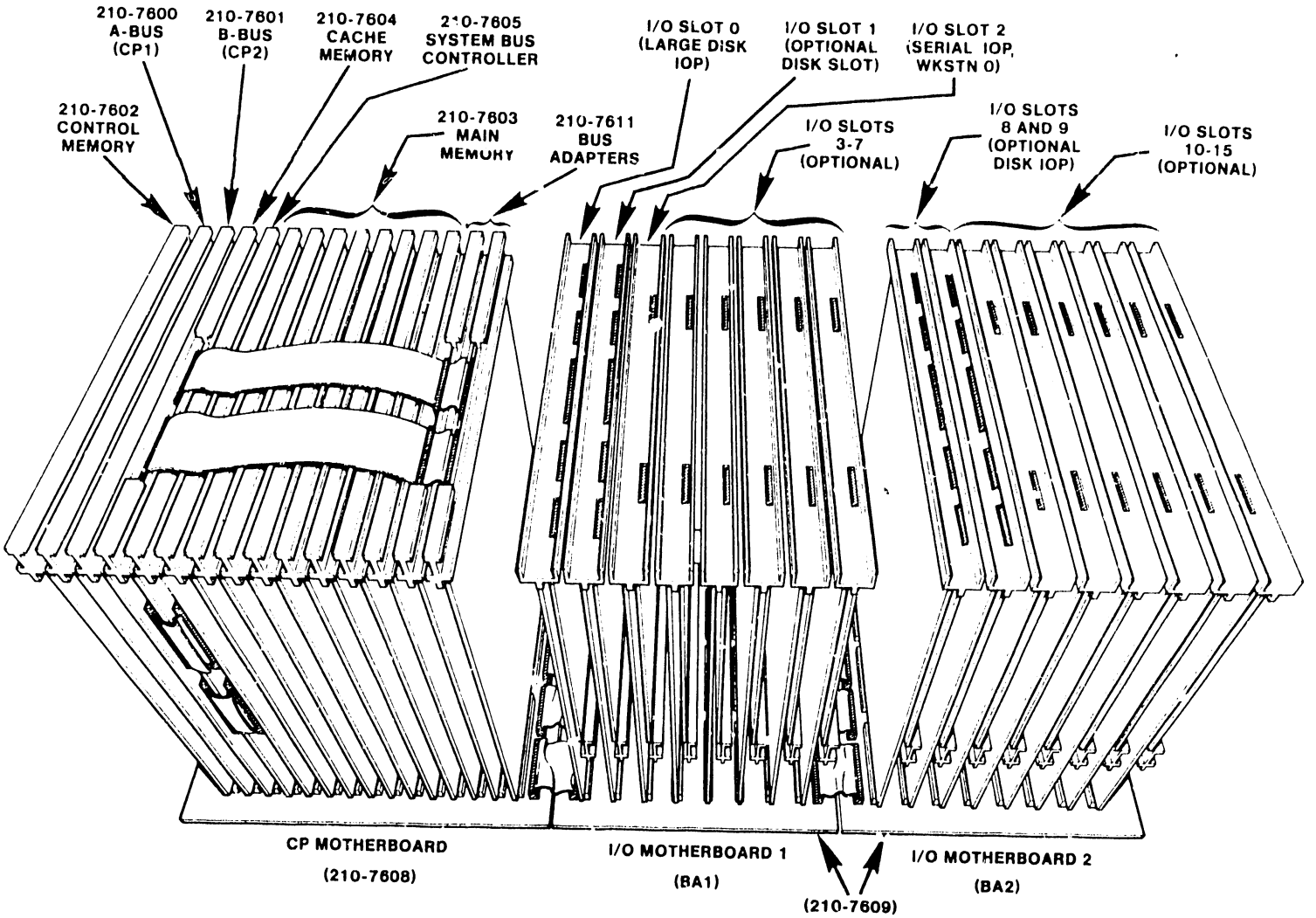


FIGURE 3-7 CPU AND I/O MOTHERBOARDS WITH FULL COMPLEMENTS OF CIRCUIT CARDS

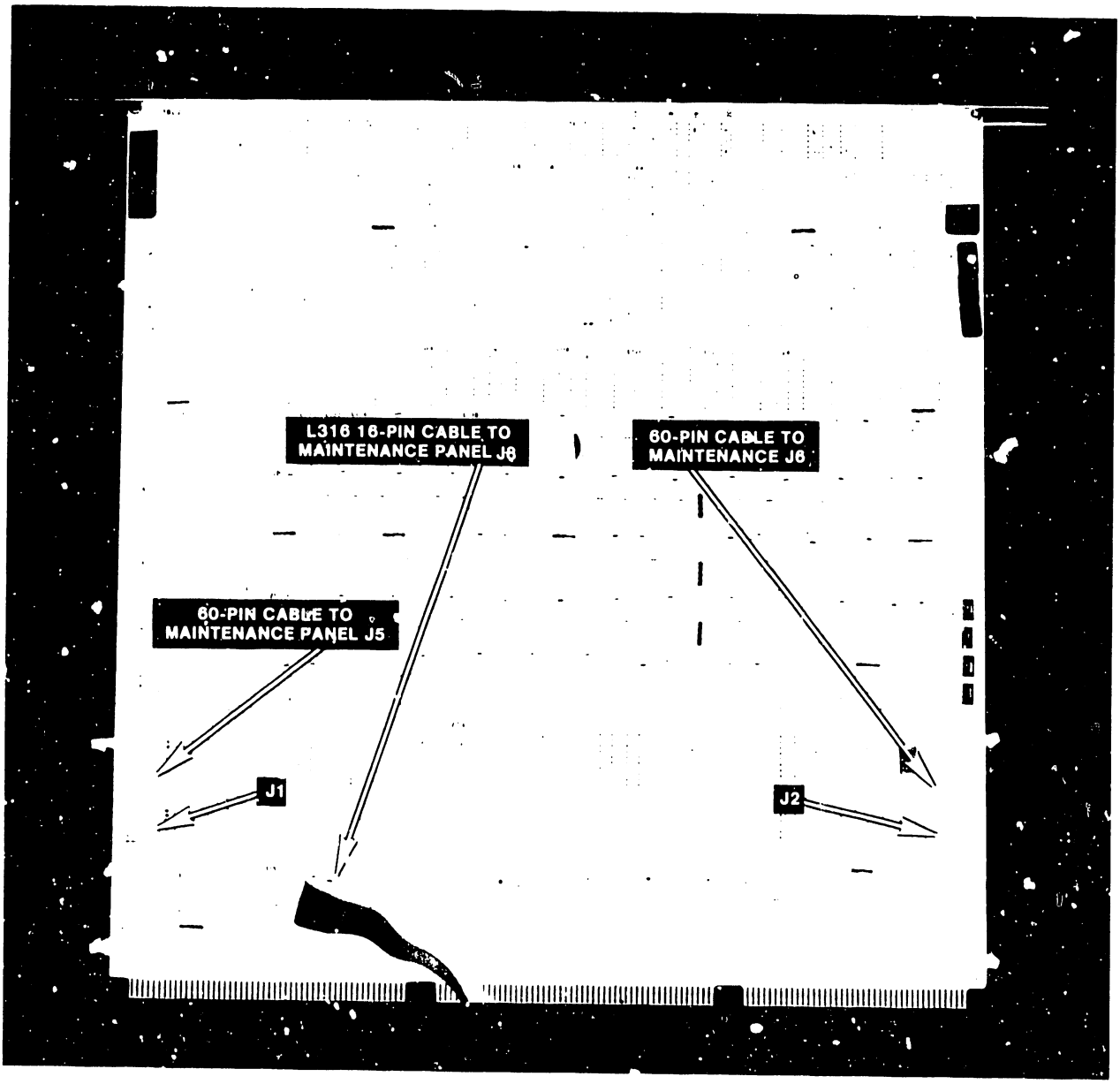


FIGURE 3-8 210-7602 CONTROL MEMORY CARD WITH CONNECTOR LOCATIONS

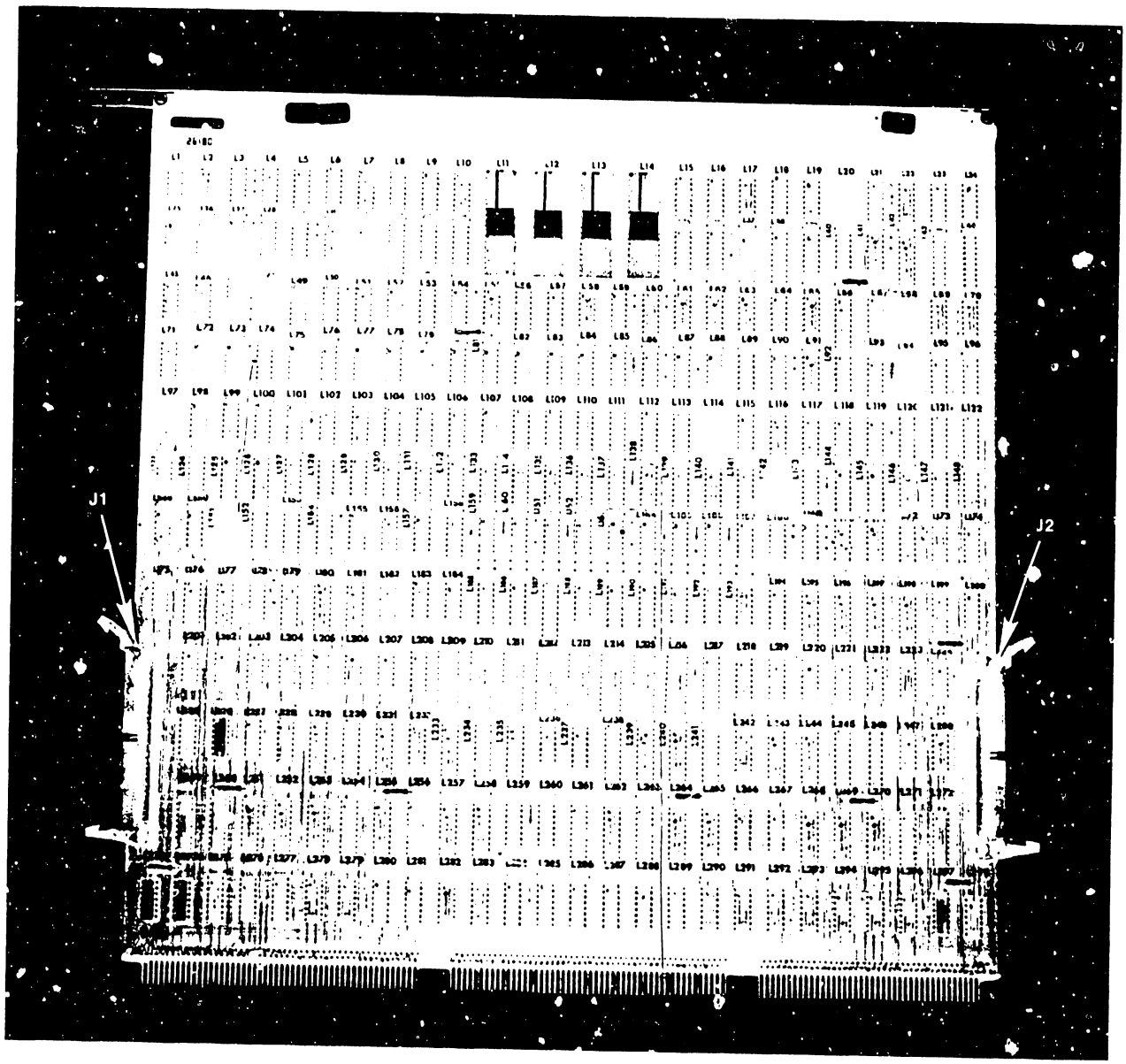


FIGURE 3-9 210-7600 A - BUS CARD WITH CONNECTOR LOCATIONS

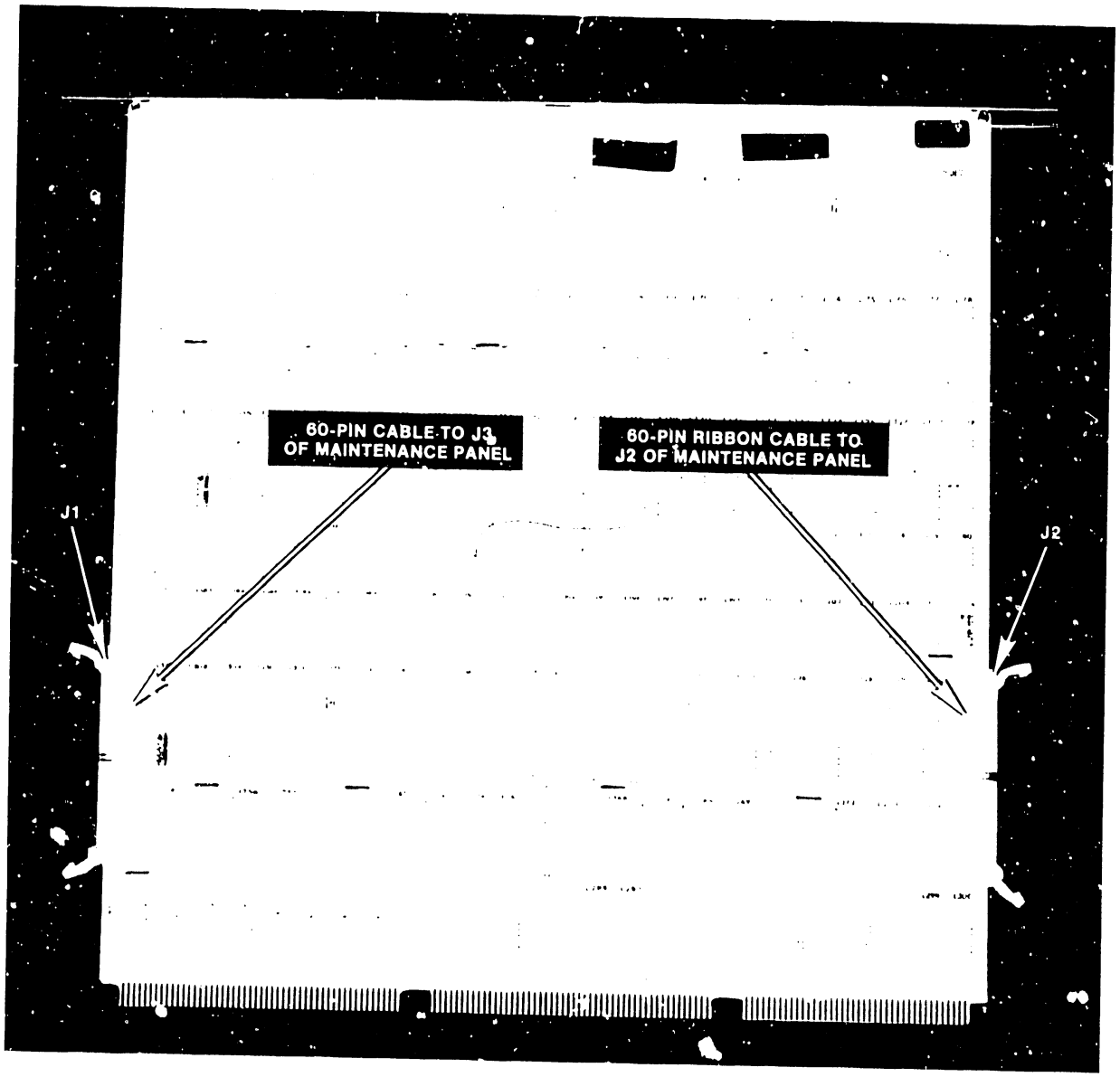


FIGURE 3-10 210-7601 B - BUS CARD WITH CONNECTOR LOCATIONS

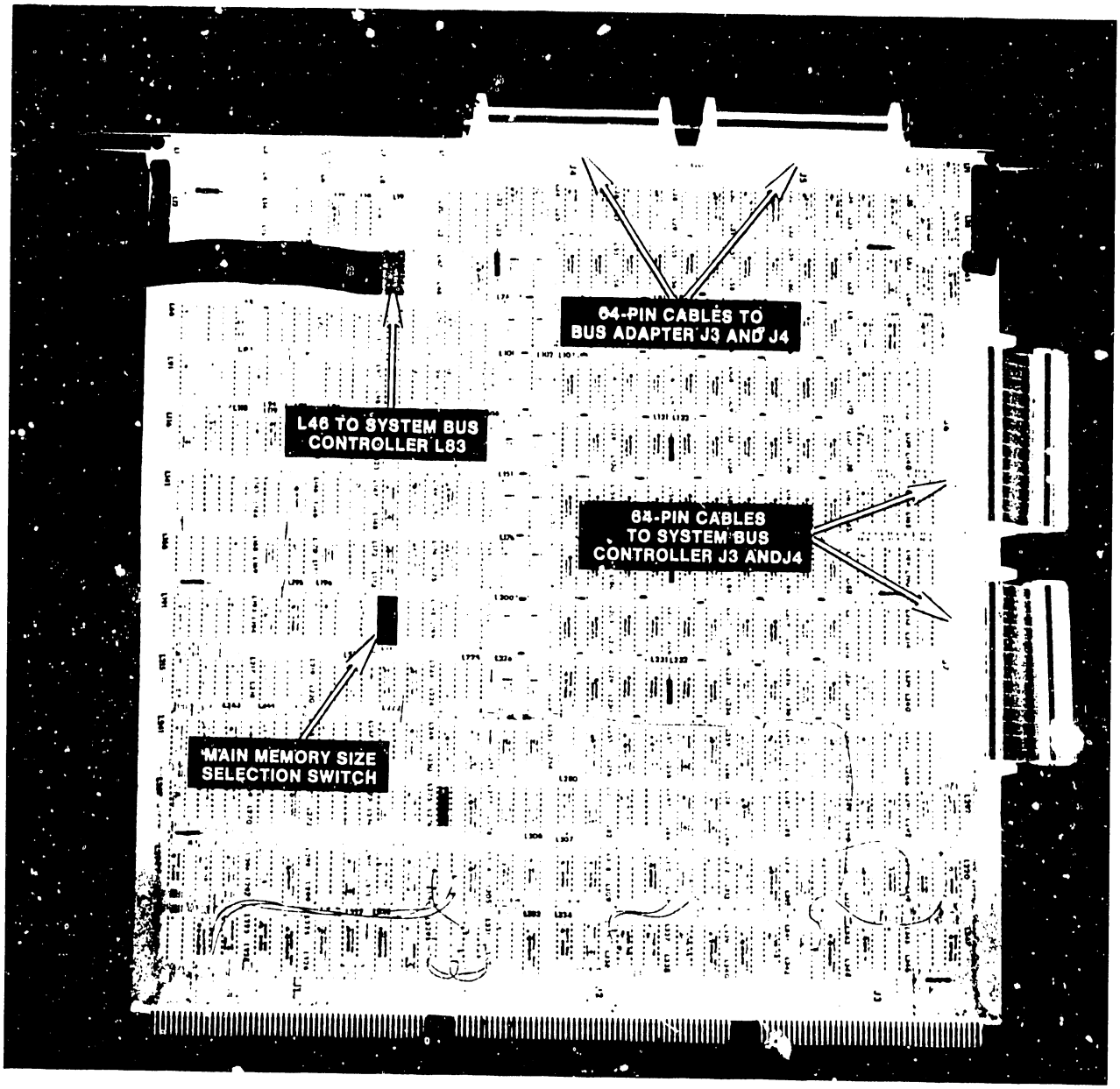


FIGURE 3-11 210-7604 CACHE MEMORY CARD WITH CONNECTOR LOCATIONS

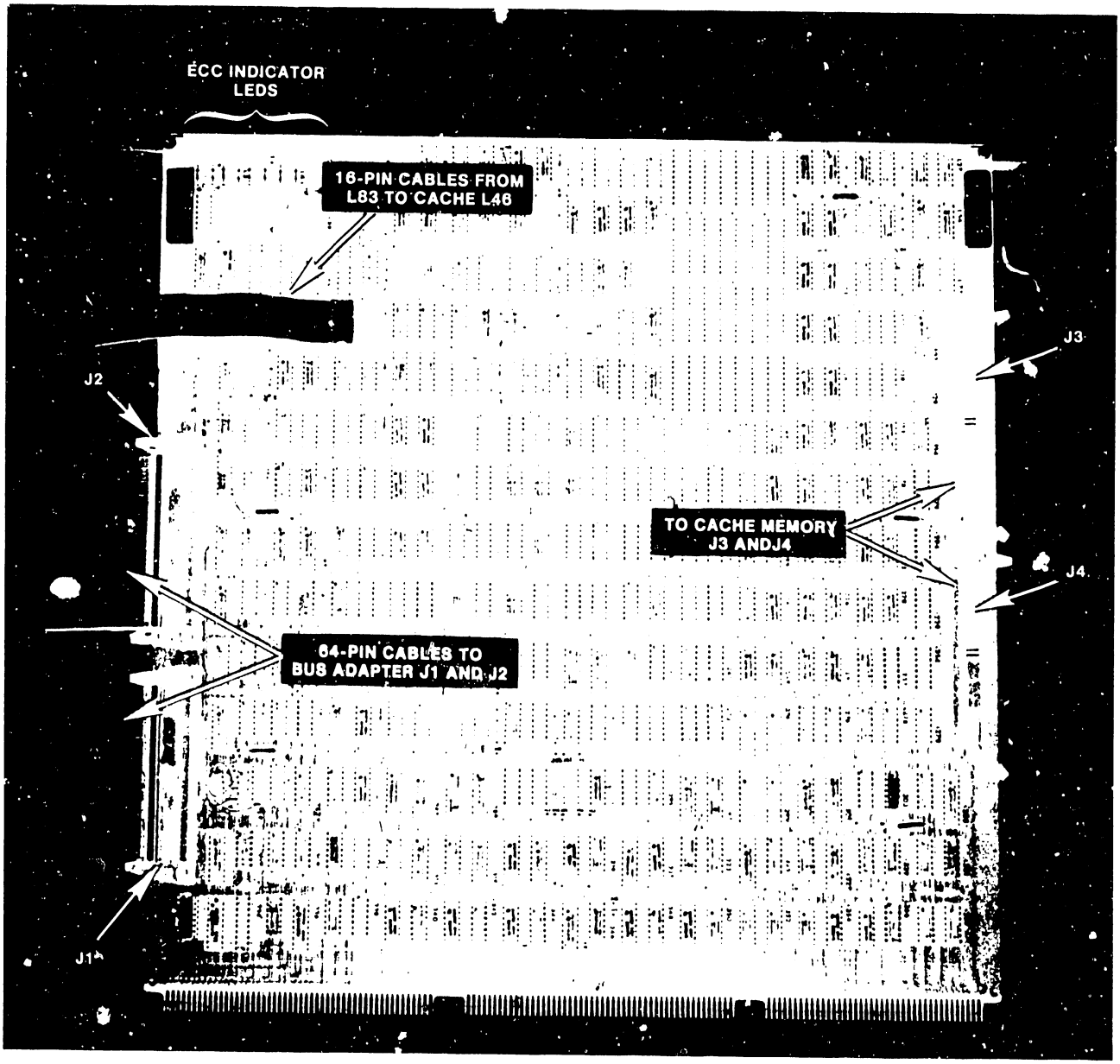


FIGURE 3-12 210-7605 SYSTEM BUS CONTROLLER CARD WITH CONNECTOR LOCATIONS

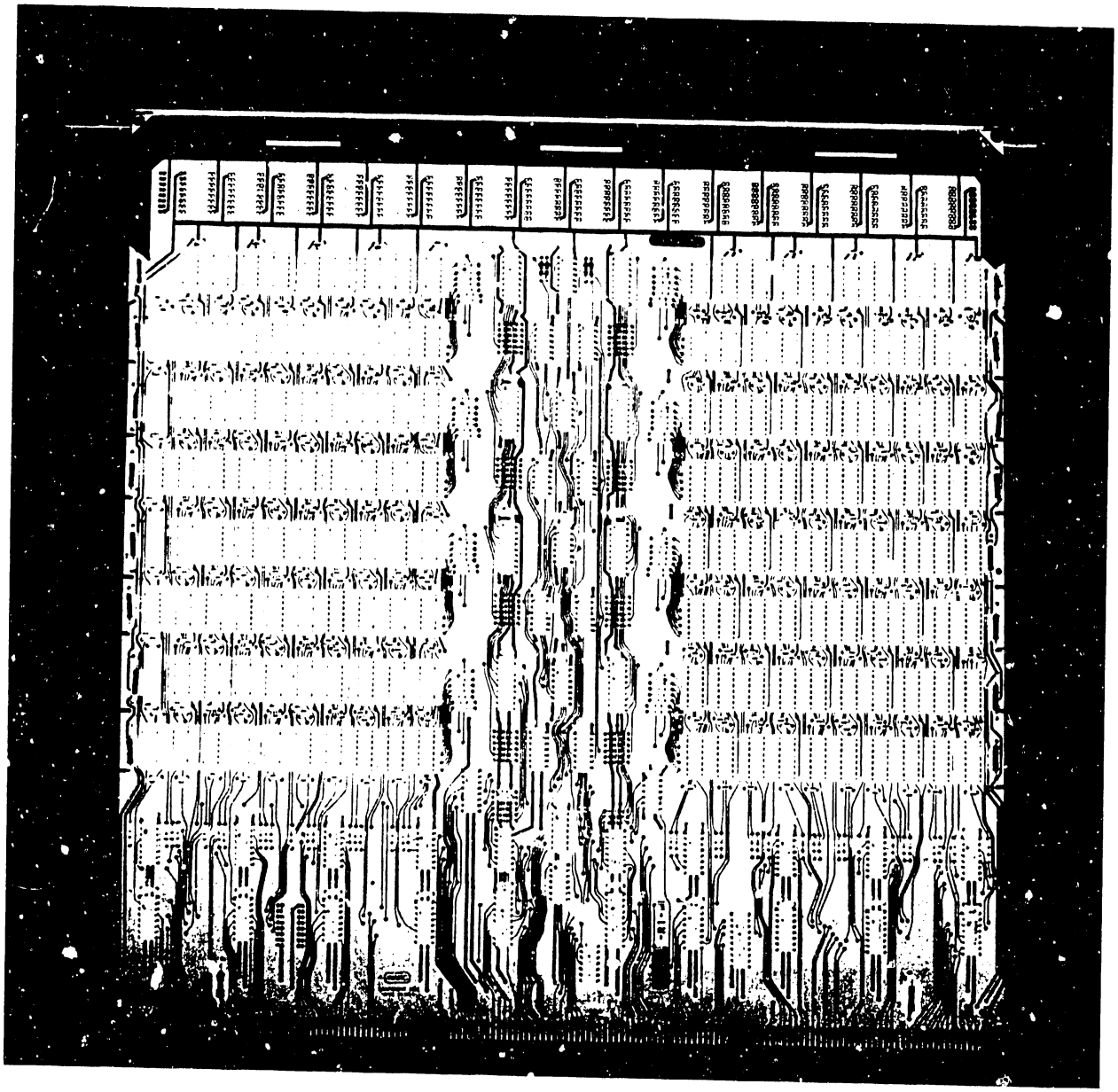


FIGURE 3-13 210-7603 MAIN MEMORY CARD

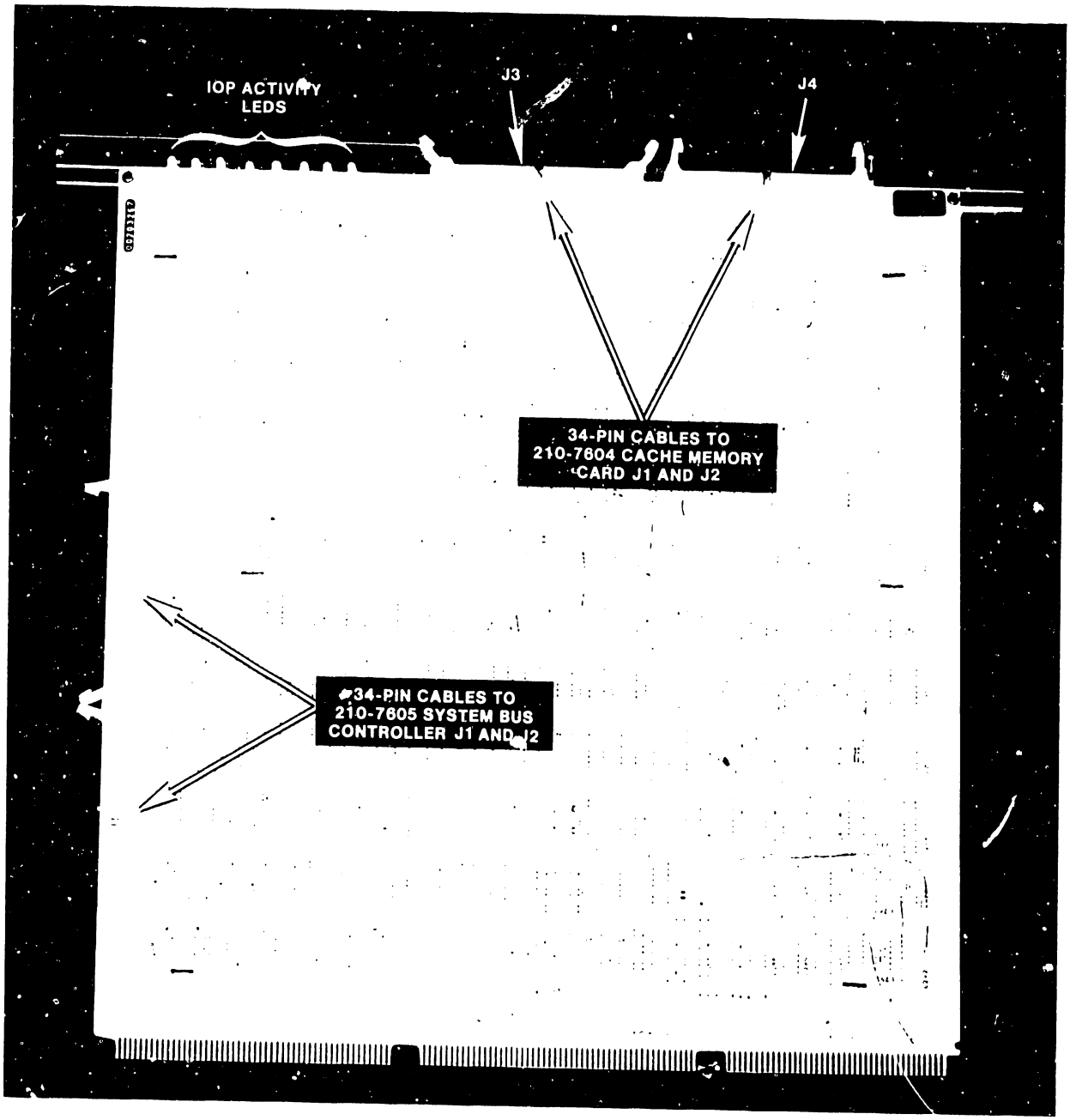


FIGURE 3-14 210-7611 BUS ADAPTER CARD WITH CONNECTOR LOCATIONS

TABLE 3B VS-100 IOP PRIORITY LIST

IOP TYPE	WLI #	PLACEMENT PRIORITY ON MOTHERBOARD
22V28 Large Disk Drive assembly	212-3023	#1
22V25-2 Tape Drive assembly	212-3011	#2
22V27-2 16-Port Serial Workstation/Printer assembly	212-3022	#3
22V26-3 TC IOP assembly	212-3020	#4

1. Install the 22V28 Large Disk IOPs in slot 0 of the I/O motherboards. At present, the VS-100 cannot handle more than one disk IOP per Bus Adapter. See following note.
2. Install a 22V27-1 16-Port Serial IOP in slot #2 of I/O motherboard 1; Workstation 0 must be connected to port #0 of this IOP. This is a microcode convention and MUST be adhered to.
3. After performing steps 1 and 2, install all remaining IOPs according to the priority table listed above. Install all IOP's of one type before installing other IOPs.
4. Because TC has the lowest priority of all IOP's, install any 22V26 IOP's immediately following all other IOP assemblies.

NOTE

Because of timing considerations, the Bus Adapter (210-7611) presently in use cannot handle more than one Large Disk IOP. For this reason, only two 22V28 IOPs can be installed on the VS-100; one disk IOP in slot 0 of I/O motherboard 1, one disk IOP in slot 0 of I/O motherboard 2. If more than one disk IOP is needed, two BA's are required on the VS-100.

3.6.3 INTERNAL CABLE CONNECTIONS

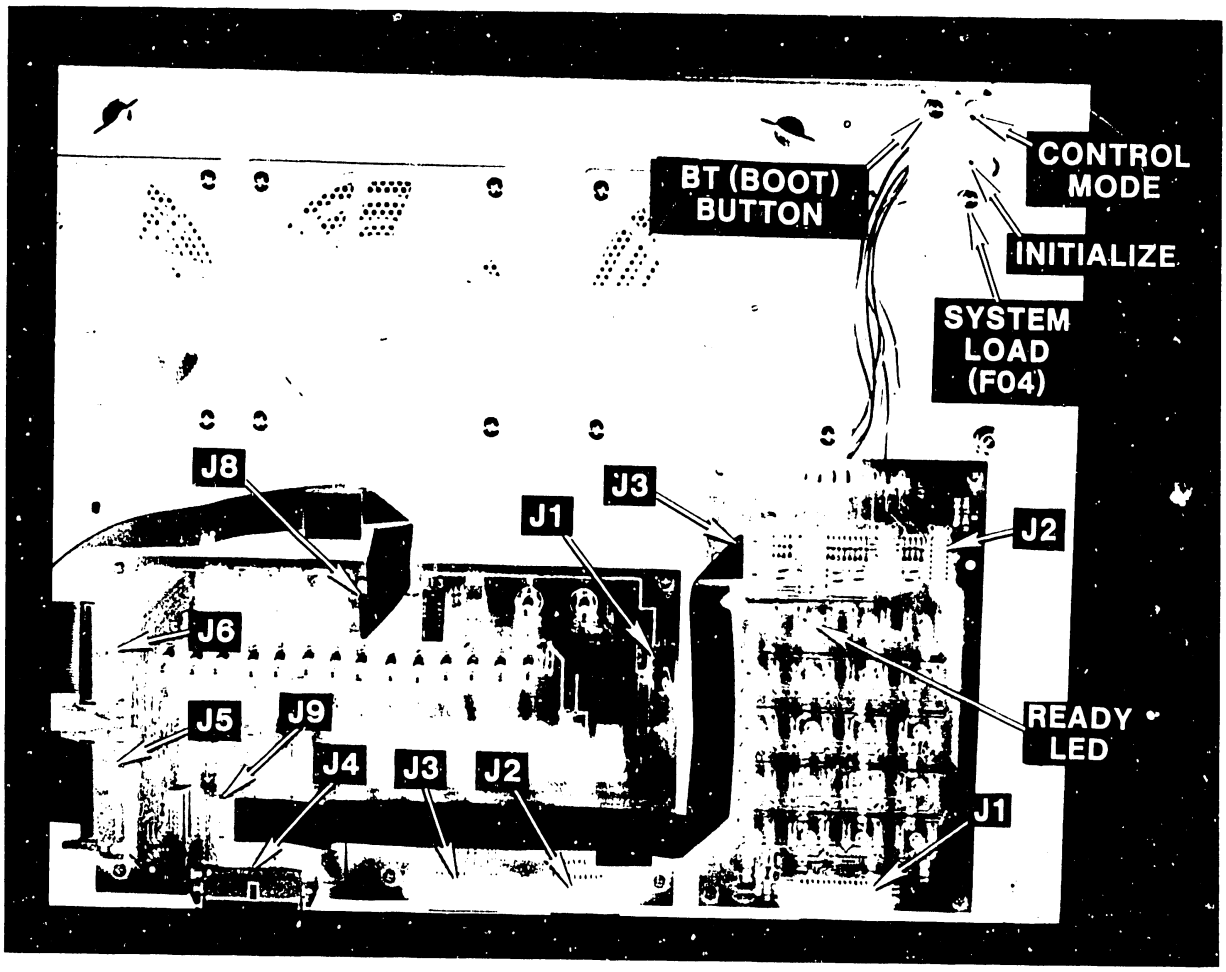
Once all Mainframe circuit cards and IOP assemblies have been installed, ensure that all internal interconnection cables are installed according to Figures 3-7 through 3-14 and Table 3C. Do not attach peripheral cables to the IOP assemblies at this time. Ensure that all card cables are secured in place, and re-install the fan panel. Refer to Figure 3-15 for proper cable configurations for the 210-7613 Front Panel and the 210-7614 Maintanance Panel.

TABLE 3C VS-100 INTERNAL CABLE CONNECTIONS

PC BOARD	CONNECTOR	TO	CONNECTOR	PC BOARD
210-7601	J1	26-pin connector	J3	210-7614 Maint-
"	J2	26-pin connector	J2	enance Panel
210-7602	L316	16-pin ribbon cable	J8	210-7614
"	J1		J5	Maintenance
"	J2		J6	Panel
210-7604	J1		J3	210-7611
"	J2		J4	"
"	J3		J3	210-7605
"	J4		J4	"
"	L46	16-pin ribbon cable	L83	"
210-7605	J1		J1	210-7611
"	J2		J2	"
210-7608	J47		J37	210-7609
"	J48		J38	(Multipled if
"	J49		J39	two I/O Mother-
"	J50		J40	boards are used.)
"	J1	16-pin ribbon cable	J1	210-7613 Front
				Panel Display
210-7609	J4		J2	210-7613 Front
				Panel Display
210-7613	J3	16-pin ribbon cable	J9	210-7614 Mainten-
				ance Panel
210-7614	J1		J2	210-7610 Mini-
	J4		J3	Disk Controller

3.7 PRELIMINARY POWER-UP ROUTINES

Before completing Mainframe re-assembly and peripheral equipment installation, perform the following physical and electrical checks.

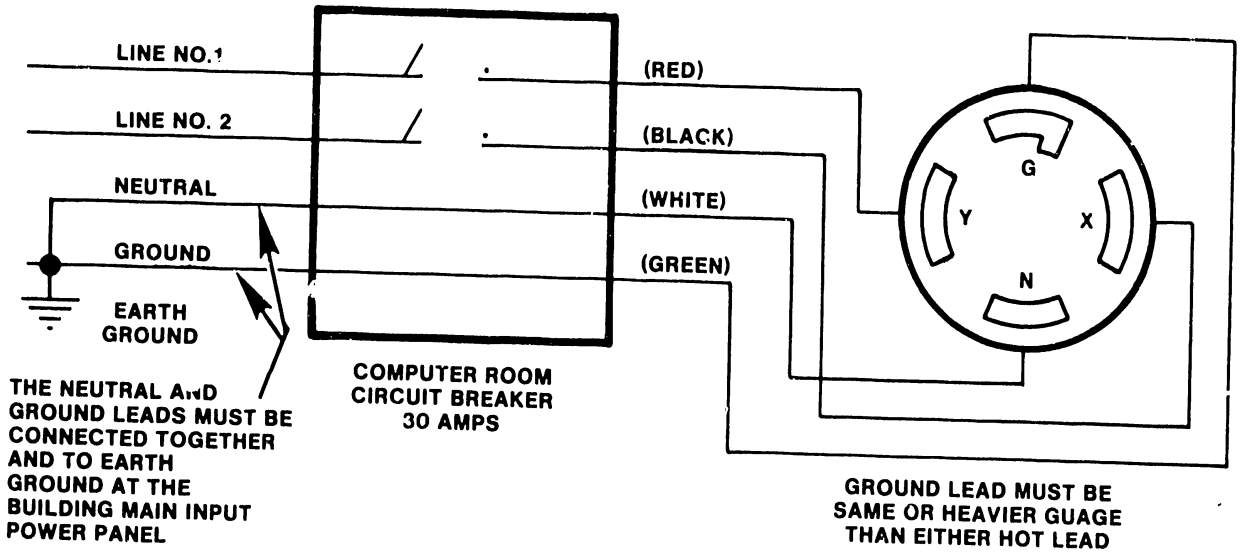


BOARD #	FROM	TO	BOARD#
210-7613	J2	J4	210-7609
210-7613	J1	J1	210-7608
210-7613	J3	J9	210-7614
210-7614	J2	J2	210-7601
210-7614	J3	J1	210-7601
210-7614	J4	J3	210-7610
210-7614	J5	J1	210-7602
210-7614	J6	J2	210-7602
210-7614	J8	L316	210-7602
210-7614	J9	J3	210-7613

FIGURE 3-15 FRONT AND MAINTENCE PANEL CABLE LOCATIONS

CAUTION

Failure to perform the following check properly can result in serious damage to Mainframe circuits and to connected peripherals.



	RECEPTACLE BODY	MATCHING CONNECTOR
NEMA Configuration:	L14-30	L14-30
Hubble Part Numbers:	2710	2711

TEST POINT LOCATIONS	DVM READINGS
X TO N	115V AC (+10%, -15%)
Y TO N	115V AC (+10%, -15%)
X TO Y	230V AC (+10%, -15%)
G TO N	+0V AC*

DVM CHART FOR VOLTAGE MEASUREMENTS AT THE SOCKET

* If a difference in potential of more than .2V exists between Neutral and Ground, notify building electrician that power supply is UNACCEPTABLE.

FIGURE 3-16 POWER SERVICE REQUIREMENTS FOR MAINFRAME/DISK DRIVES

3.7.1 MAINFRAME SOURCE-POWER CHECK

Check the Mainframe power-supply receptacle for proper wiring and service, as defined in Figure 3-16. Ensure that the outlet meets all specified requirements before proceeding with the installation.

3.7.2 INITIAL MAINFRAME POWER-UP

1. After ensuring that the Mainframe circuit breaker is OFF, plug the Mainframe power connector into the wall outlet and twist the connector to lock it in place.
2. Perform the following in the sequence given: (See Figures 3-17, -18.)
   a) Set the Mainframe circuit breaker ON.
   b) Depress the Power-On pushbutton located on the power panel.
3. Ensure that the Power-On indicator on the power panel is lit and that the Mainframe cooling fans activate.
4. Check the Voltage-Sensing LEDs on the linear power supply chassis. If LEDs are lit, voltages are present on the System but not necessarily within limits.
5. Perform the voltage adjustment procedures in Chapter 6 of this manual.

3.7.3 INITIAL MICROCODE LOADING

With the completion of the voltage adjustment procedures, the initial Mainframe power-up routines are done. As part of the installation and PM procedures, and at any time CPU integrity becomes suspect, the microcode diagnostics will be loaded and run. Refer to Chapter 8, Daignostics, for this procedure.

Once the diagnostics have run successfully, load the System Microcode into Control Memory as follows:

1. Insert the microcode diskette (WLI #705-0154) into the mini-floppy drive and press the silver 'BT' (BOOT) button on the Control Panel (See Figure 3-18) to load the microcode into Control Memory.
2. Wait for the 'READY' LED on the Front Panel to light.

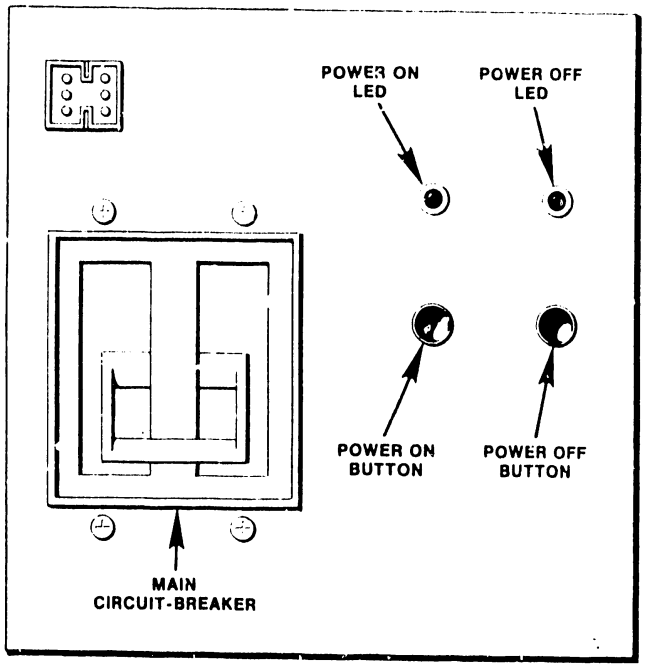


FIGURE 3-17 VS-100 POWER PANEL

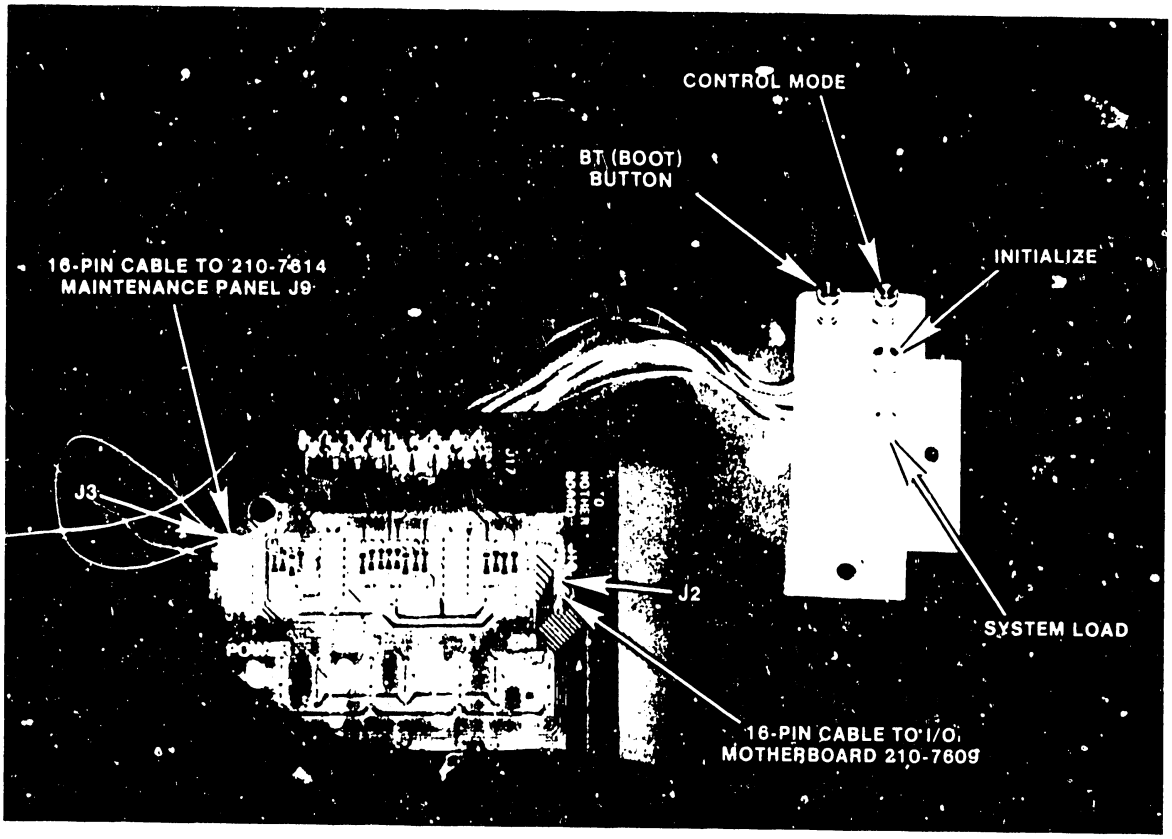


FIGURE 3-18 VS-100 FRONT PANEL CONTROLS AND INDICATORS

NOTE

If LED flashes instead of remaining in the steady ON state, system has failed to load the microcode. Reseat diskette and repeat the loading procedures.

3. If microcode cannot be loaded, insert and run the back-up diskette if available. If this fails, the drive or drive controller (210-7610) are suspect. Refer to drive maintenance procedures in Chapter 6.
4. Power-down the Mainframe and create a minimum system as follows:
   a) Attach a serial workstation to IOP 2, Port 0 on BA1. This device will be Workstation 0.
   b) Connect a disk drive to IOP 0, Port 0 on BA1. This drive is the System Disk, storing the Operating System created during SYSGEN.
5. IPL the System and perform the SYSGEN procedure described in VS Releases 5.01 SYSGEN Procedures (WLI #800-8201SP-05) and VS SOFTWARE BULLETIN--RELEASE 5.01 (WLI #800-3105-01).
6. After completing SYSGEN, connect all peripherals according to the following paragraph.

3.8 SYSTEM INTERCONNECTION

After microcode is loaded and SYSGEN has been performed, power-down the Mainframe and connect all peripheral devices according to the configuration created during SYSGEN. Refer to Figures 3-19, 3-20A, 3-20B, 3-21, the following paragraphs, and the appropriate documents in Classification III for cabling procedures.

3.8.1 CONNECTOR PLATE-TO-I/O MOTHERBOARD CABLING

Before installing cables in the connector plates at the rear of the Mainframe, all cables between the plates and associated IOPs must be installed. Ensure that the cable from the connector plate containing workstation 0 connects to J1 of the Serial IOP assembly in I/O slot 2 of BA1. Ensure that the 'B' cable of the System disk is attached to the top connector of the disk connector plate in rear panel location #0. The 'B' cable from this connector plate must be connected to J2 of the Disk IOP assembly in I/O slot 0 of BA1. (See Figure 3-19 for rear-panel connector plate layout.)

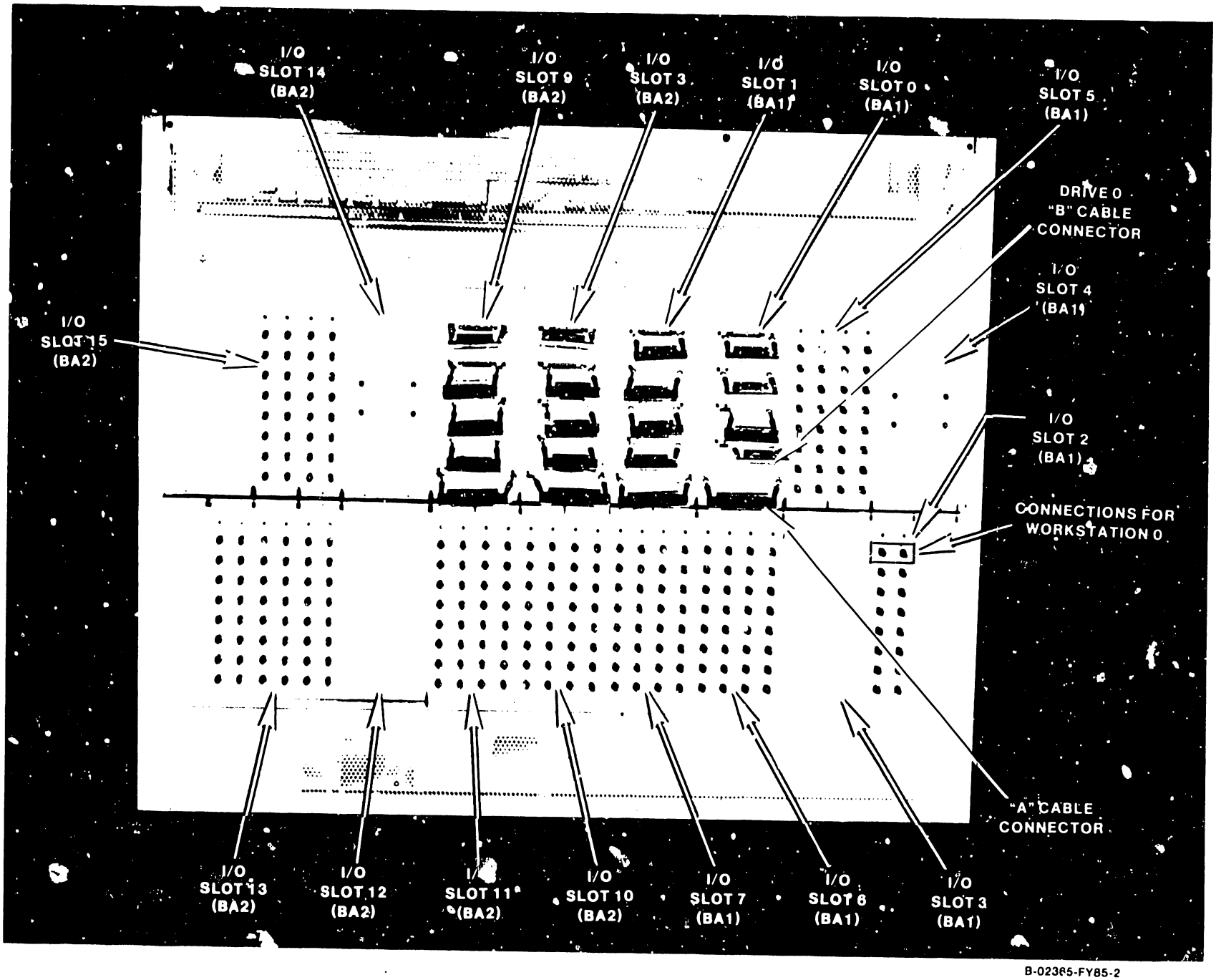


FIGURE 3-19 VS 100 REAR PANEL CONNECTOR PLATE LOCATIONS

3.8.2 BNC/TNC CONNECTORS

Serial I/O devices (workstations, printers, etc.) connect to the Mainframe by means of standard BNC/TNC connectors mounted on a 16-connector plate (WLI #270-0704). Maximum cable length for these devices is 2000 feet. Workstation 0 MUST be attached to Port 0 on IOP 2, BA1. The connectors for Workstation 0 are located in the upper position of the connector plate in the lower right-hand corner of the rear panel of the Mainframe. Refer to Figure 3-19 for details on connector plate and BNC/TNC count for peripherals.

NOTE

The VS-100 supports the FiberWay Active Port Assembly (FWAPA). The FWAPA is a multiplexed fiber optic link that supports up to 32 peripheral connections over two optical ports, using the 32-port 22V47 Serial IOP. FWAPAs for the VS-100 are installed only in the Wang VS Large Cable Concentrator. For installation and interconnection interformation for the FWAPA, refer to the Wang VS Large Cable Concentrator product maintenance manual and the Remote Cluster Switch product maintenance manual.

3.8.3 DISK CABLE CONNECTORS

Two sizes of disk cable connectors and clamps are located on the disk connector plates (WLI #270-0910). The top four (narrow) connectors contain 26-pin sockets for the 'B' cable connections; the bottom (wide) connector contains a 60-pin socket for the 'A' cable connection. Both types connect the disk cable to the Mainframe in the same manner. Connector plate locations 1 and 2 (I/O slots 0 and 1) are usually reserved for Disk IOP connectors.

Before connecting a disk cable, prepare it as follows, if necessary:

1. Remove 6 inches of plastic sheathing from one end of the cable.
2. Fold the copper shield back exposing the disk cable.

To connect a disk cable to the Mainframe proceed as follows: (See Figure 3-20A.)

1. Disassemble the cable clamp by removing the Phillips screws on either side of the clamp.
2. Lay the disk cable in the portion of the clamp still attached to the Mainframe. Slide the plastic sheathing under the ground clip, with the copper shielding against the clamp. The exposed disk cable should extend to the connector on the disk connector plate.
3. Reassemble the cable clamp by installing the two Phillips screws removed in step 1. Ensure that pin 1 is oriented properly and tighten the clamp screws until solid contact with the copper shield is made. Do NOT overtighten, as this could damage the disk cable.

4. Plug the cable into the cable connector on the disk connector plate. The top four connectors of each disk connector plate attach the "B" cable of each drive; the bottom connector on the plate attaches the "A" cable daisy-chained through each drive to the VS-100 Mainframe. The "B" cable connector directly above the "A" cable connector attaches to Port 0 of the associated disk IOP.

NOTE

Sector-switch settings for the VS-100 on the 2265V-1/V-2 disk drives are the same as the VS 60/80. Refer to the v3 Reference Summary for switch settings.

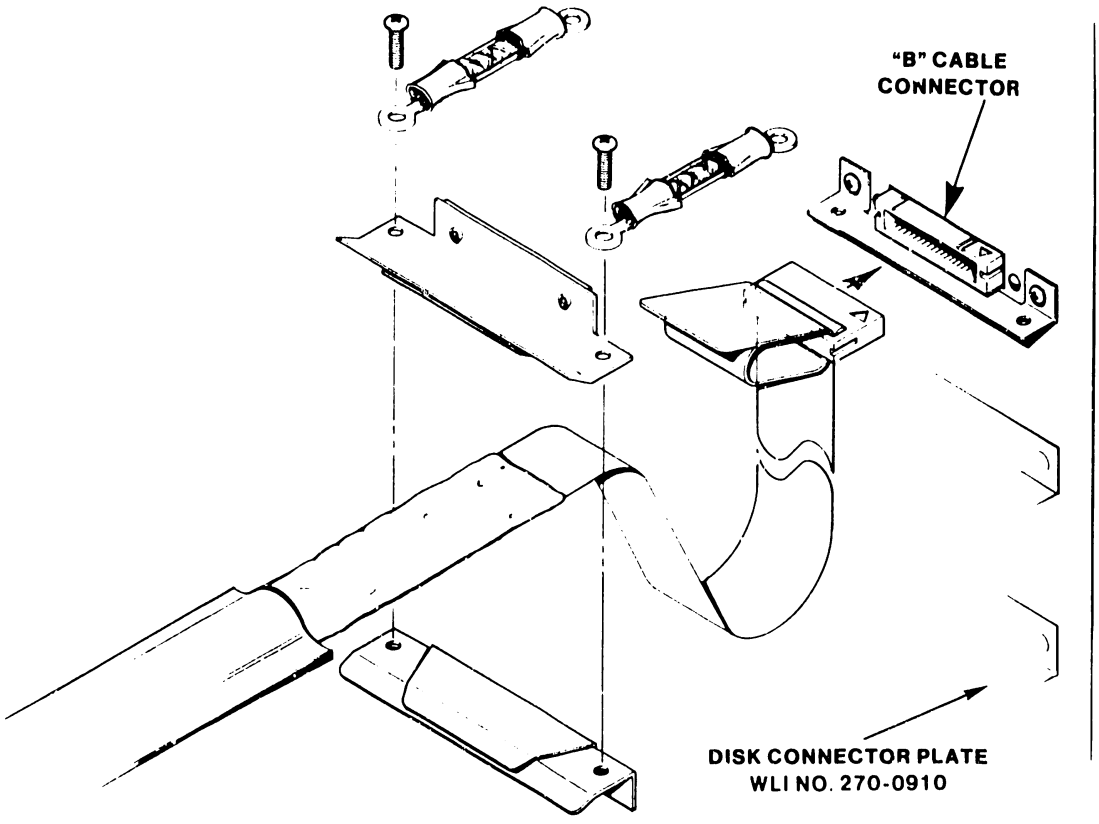


FIGURE 3-20A "B" CABLE CONNECTION

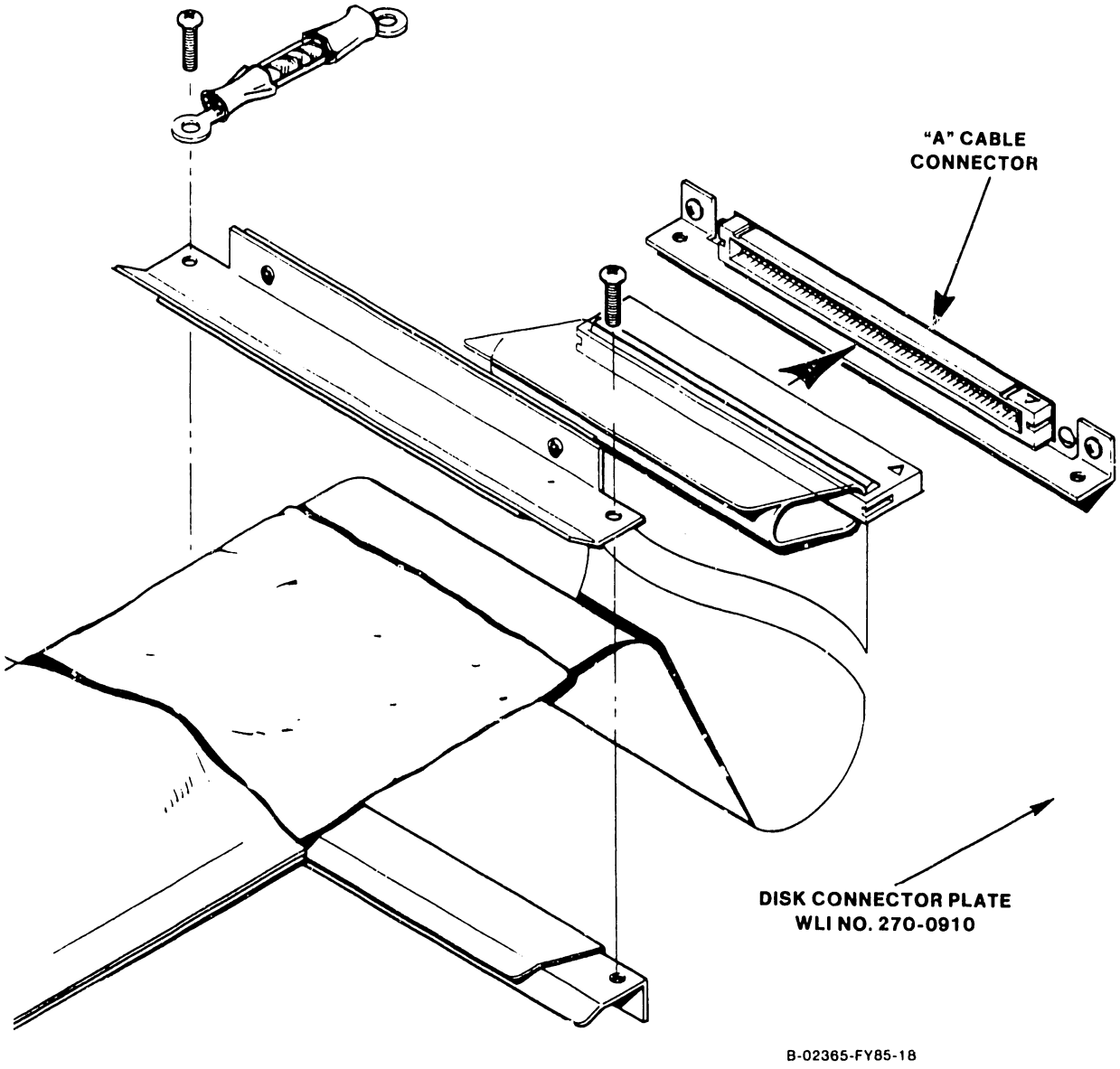


FIGURE 3-20B 'A' CABLE CONNECTION

3.8.4 TELECOMMUNICATION CONNECTORS

If the TC option is to be installed, the TC cables must be attached to a an RS-232 connector plate (WLI P/N 270-0705 for 1-port, 270-0705-2 for 2-port, 270-0705-3 for 3-port) at the rear of the Mainframe. This plate supports as many as three TC connections, providing plugs for both the modem and Automatic Calling Unit (ACU) cables for each installation. This connector plate then attaches to a 22V26-series TC IOP. The top connectors (modem and ACU cables) on this plate attach to Port 1, the middle connectors attach to Port 2, and the bottom connectors attach to Port 3. (See Figure 3-20C.)

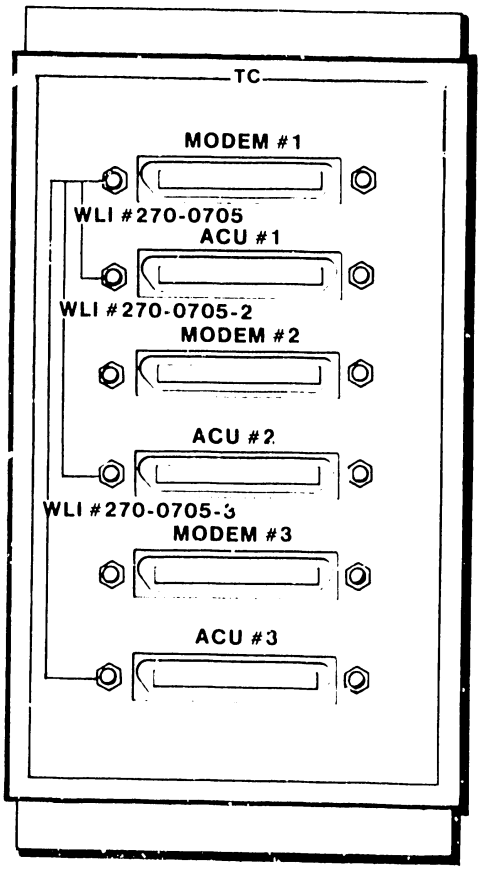


FIGURE 3-20C TELECOMMUNICATIONS CONNECTOR PLATE

3.8.5 TAPE CABLE CONNECTORS

Two types of tape connector plates are available to attach tape drives to the mainframe. The two types of tape connector plates are: Kennedy tape drive plate (WLI P/N 270-0911) and Telex tape drive plate (WLI P/N 270-0741).

For the Kennedy tape dive, two sockets are located on the plate for attachment to the drives. The top socket receives the data cable and the bottom socket receives the control cable. Note the orientation of the cable plug when inserting it into the socket.

For the Telex tape drive, three sockets are located on the plate for attachment to the drives. The top socket receives the control cable, the middle socket receives the data cable, and the bottom socket receives the status cable. Note the orientation of the cable plug when inserting it into the socket. See figure 30-20D.

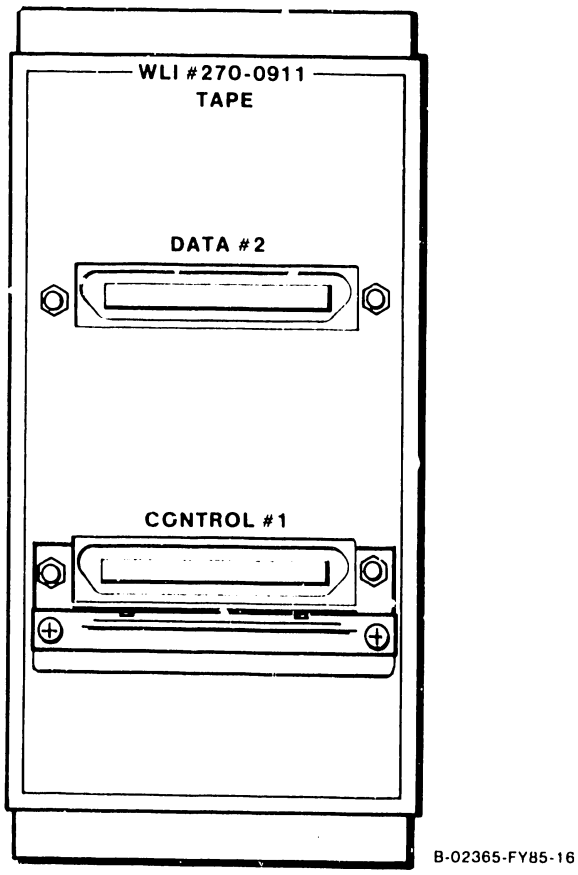


FIGURE 3-20D KENNEDY TAPE CABLE CONNECTIONS

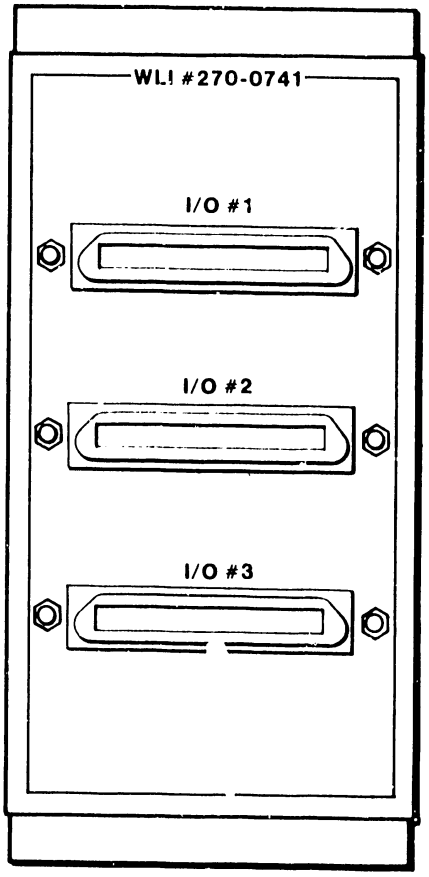


FIGURE 3-20E TELEX TAPE CABLE CONNECTIONS

3.8.6 INSTALLING THE ARCHIVING WORKSTATION

All VS-100 Systems are equipped with an Archiving Workstation (VS-AWS) as standard equipment. The VS-AWS, which consists of an Archiver Terminal and an Archiver Master Unit, provides the user with remote batch storage facilities that allow the archiving of WP documents (when used with suitable software and a 'C'-type keyboard), the storing and processing of VS/DP files, and the using of IBM compatible diskettes.

The VS-AWS connects to the VS-100 through a WLI #120-2300 paired-coax signal cable assembly of up to 2000 feet in length, connecting to one port of a 22V27 Serial IOP assembly (see Figure 3-21). The only restriction when connecting a VS-AWS is that the two devices making up the Archiver must be assigned to consecutive device numbers on a common port with the Archiver Terminal ("S" or "C" workstation) assigned to the EVEN numbered port and the Disk Unit assigned to the ODD numbered port. Refer to Chapter 4 for IOP switch settings on the VS-100. Refer to Category III.D.4 for more detailed information concerning the AWS-1.

NOTE

If the AWS-1 is used as W/S 0, the WP function cannot be used.

3.9 PRELIMINARY SYSTEM CHECKOUT

At this point, all peripherals should be installed, powered off, and attached to their respective IOPs. Before proceeding, perform the following checkout procedure:

1. Visually inspect all Mainframe circuit cards for correct switch settings and proper cabling configuration.
2. Visually inspect all peripheral devices to ensure that I/O cabling is correctly installed, all switch settings are correct, and all covers and panels are in place.
3. Ensure that all devices are powered off.

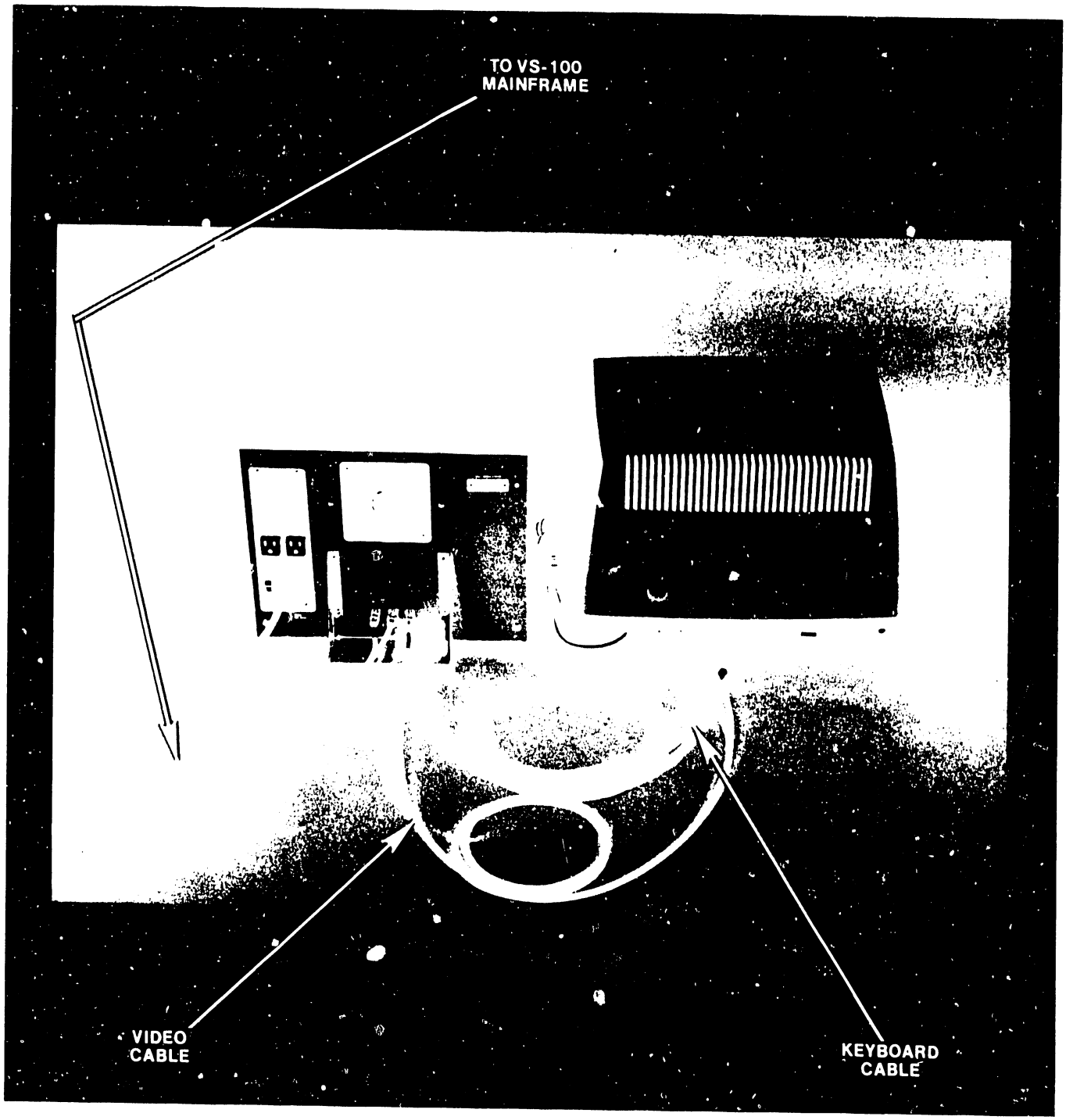


FIGURE 3-21 CONNECTING THE ARCHIVING WORKSTATION

3.9.1 SYSTEM POWER-UP/POWER-DOWN PROCEDURES

After all peripherals are connected to the Mainframe, the power-up from a cold start and power-down procedures for the VS-100 System are as follows:

1. POWER-UP
   a. Ensure that the Mainframe power connector is plugged into the wall receptacle.
   b. Power-Up Workstation #0 and the PRIMARY disk drive.
   c. Switch the Mainframe circuit-breaker to the ON position.
   d. Press the Power-On button located on the Power Panel.
   e. Ensure that the system microcode diskette is in the mini-floppy drive, and press the BT button.
   f. After successfully loading microcode, depress the Initialize button to begin loading the Operating System.
   g. Workstation 0 will display CM F04. Hit the 'BACKSPACE' key and type in F/R and the Physical Device Address of the disk the system will be IPL'ing from. (Refer to Chapter 8 for details.)
   h. After successfully loading the OS, mount the disks and power-up all peripherals.
   i. If this is a new installation, perform all applicable peripheral diagnostics. Refer to Chapter 8 of this document, the VS Service Program Guide, the VS Central Processor Micro-diagnostic Test mannual, and appropriate documents in Class. III for the necessary instructions. Ensure that all peripherals function correctly.

2. POWER-DOWN
   a. Power-Down all peripheral devices according to procedures in the applicable documents in Classification III.
   b. Press the Power-Off button located on the Mainframe Power Panel.
   c. Switch the circuit breaker to the OFF position.

3.10 SYSTEM TURNOVER

1. Remove any scratch or Customer Engineering OS disk packs from the system disk drives.
2. Mount the customer's OS pack and perform an IPL from this pack.

3. Log on to a Workstation and use the Command Processor display functions to display the files in the @SYSTEM@ library on the customer's Operating System pack. Check through the listed files to ensure the presence of all customer-purchased options. If the BASIC compiler was purchased by the customer, for example, the following files should be present in the @SYSTEM@ library:
   a. BASIC
   b. WB1PASS1
   c. WB2PASS2

   If the COBOL compiler was purchased, conversely, the following files should be present:
   a. COBOL
   b. WC1PASS1
   c. WC1PASS2

   If the RPG compiler was purchased, only the following file should be present:
   a. "RPGII"
4. Delete any of the above compilers not purchased by the customer from the related files using the Command Processor SCRATCH function.
5. Mount customer scratch packs on all additional disk drives. (The customer determines which packs will be scratch packs.) Perform a disk initialization procedure on each of the customer's scratch packs.

CAUTION

Ensure that the customer's scratch packs have no files on them before performing the initialize procedure. Also, demonstrate to the customer or to the responsible computer operator how the disk initialization procedure is performed. Include in the demonstration a description of disk drive operations--including loading and unloading of disk packs, emergency power-down of the disk drive, and disk drive fault recovery.

---

6. Perform the following "Evening Shut-down Procedure" and explain each step to applicable customer personnel:
   a. Ensure all workstations have been 'logged-off'.
   b. Press the 'CONTROL MODE' button on the VS-100 front panel. This prevents a disk I/O command from being halted prior to completion.

c. Place all drives in the "LOAD MODE" condition (heads unloaded).

d. Power down all workstations.

e. Power down all printers.

f. Unload and power down all tape drives.

7. Perform the following "Daily Start-up Procedure" and explain each step to applicable customer personnel:

   a. Bring all disk drives up to the ready condition.

   b. On Workstation #0, press the 'X" key and then the ENTER key.

   c. Power on all other workstations and press the HELP key at each workstation (a LOG-ON screen should be displayed on each CRT).

   d. Power on all printers.

   e. Power on all tape drives.

8. Allow the customer to test the system using his programs. If the customer is satisfied with the operation of the system, officially turn the system over to the customer. (As of this printing, there is no official form to sign which effects turnover, nor has one been proposed. This should be merely a verbal notification given by the CE performing installation.)

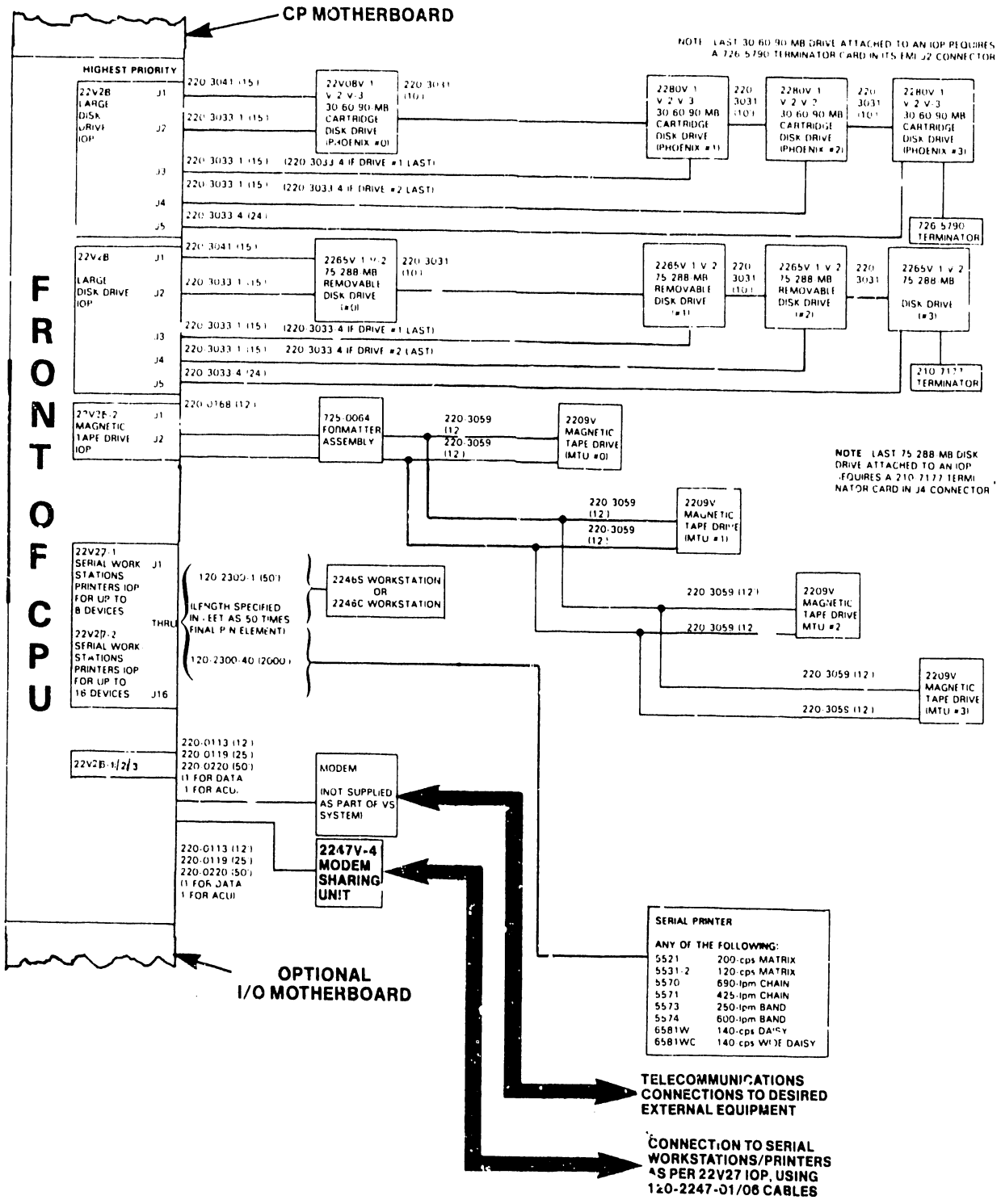


FIGURE 3-22 SYSTEM INTERCONNECTION DIAGRAM

CHAPTER 4

SWITCHES AND INDICA-TORS

CHAPTER 4
SWITCHES AND INDICATORS

4.1 GENERAL

This chapter provides the CE with tables listing all switches and indicators found on and in the VS-100 Mainframe. Included in this chapter are the procedures for using these devices and a brief statement on the purpose of each switch and indicator.

Tables 4A and 4B list the switches and indicators found on the VS-100 along with a brief description of their purpose. Actual locations of the switches and indicators are shown in Figures 4-1 and 4-2.

Because of its function as a diagnostic tool, a detailed description of the Maintenance Panel is included in Chapter 8 of this document.

TABLE 4A VS-100 SWITCHES

SWITCH NAME/TYPE	LOCATION	PURPOSE
Circuit Breaker	Power Panel	Applies input power to the Mainframe when in the ON position.
Power-On Pushbutton	Power Panel	Applies power to the CP and I/O Motherboards when activated.
Power-Off Pushbutton	Power Panel	Removes power from the CP and I/O Motherboards when activated.
BOOT (BT) Silver Pushbutton	Control Panel	Causes System microcode or diagnostic microcode to be loaded into Control Memory from the mini-floppy drive.
CONTROL MODE Red Pushbutton	Control Panel	Forces System into Control Mode.
INITIALIZE Green Pushbutton	Control Panel	Causes System to IPL from primary disk drive and System clock will be reset.
SYSTEM LOAD Black Pushbutton	Control Panel	Causes System to IPL from primary disk drive, System clock will not be reset.

TABLE 4A VS-100 SWITCHES (cont'd)

SWITCH NAME/TYPE	LOCATION	PURPOSE
Maintenance Panel Switches	Maintenance Panel	Refer to Chapter 8.
-5VA, -5VB, +12VA, +12VB Adjustment POTs	Linear Power Supply Front Cover	Adjusts the indicated voltage up or down, as needed. Refer to Chapter 6 For details.
+5VA, +5VB Adjustment POTs	Switching Power Supply Front Cover	Adjusts the indicated voltage up or down, as needed. Refer to Chapter 6 for details.
Memory Size DIP-Switches	7604 Cache	Used to determine Main Memory Size. Refer to Paragraph 4.6 for details.
IOP Address	IOP Circuit Cards	Used to set Device Address for each IOP on the I/O Motherboard. Refer to Para-4.7 for details.

TABLE 4B VS-100 INDICATORS

INDICATOR NAME/TYPE	LOCATION	PURPOSE
Power-On LED	Power Panel	Indicates Power-On Switch activated. Power applied to Motherboard when lit.
Power-Off LED	Power Panel	Indicates Power-Off Switch activated. All Power except -15VDC to TC IOP removed from Motherboard when lit.
±5VA, ±5VB, +12VA, Voltage Sensing LEDs	Linear Power Supply	Six LEDs indicate designated voltages are within limits when lit.
±5VA, ±5VB, +12VA, Voltage Test Points	Linear Power Supply	Operating voltages for the Mainframe measured at these points.
Power-On Indicator LED	Front Panel, Top Row, Left-most LED	Indicates power is applied to the CPU when lit.

TABLE 4B VS-100 INDICATORS (cont'd)

INDICATOR NAME/TYPE	LOCATION	PURPOSE
READY LED	Front Panel, Top Row, Second LED From Left	Indicates successful microcode load when in steady-on state; unsuccessful load when flashing.
CP HALT LED*	Front Panel, Top Row, Third LED From Left	Indicates CPU is in the HALT state when lit.
CM PARITY ERROR LED*	Front Panel, Top Row, Rightmost LED	Indicates an error in Control Memory when lit.
IOP Parity Error LEDs	Front Panel, Bottom Four Rows	Sixteen LEDs, one for each IOP slot on the I/O Motherboards. Indicate occurrance of parity error on a specific IOP when lit.
Maintenance Panel Indicators	Maintenance Panel	Refer to Chapter 8 for details.
ECC Indicator LEDs	Top Edge, 7605 System Bus Controller	Eight LEDs that keep count of all single-bit parity errors detected and corrected by the system. LEDs keep a continuous count of errors that occur.
IOP Activity LEDs	Top Edge, 7611 Bus Adapter Card	Eight LEDs indicating which IOP is active at any given time.
Diskette Activity LEDs	Front of mini-floppy drive	When lit, indicates that drive is in use. (Drive head is loaded.)

* CM Parity Error and CP HALT LEDs both light during a microcode load operation. Ignore these displays, neither indicator reflects a valid trouble condition until after the VS-100 is initialized.

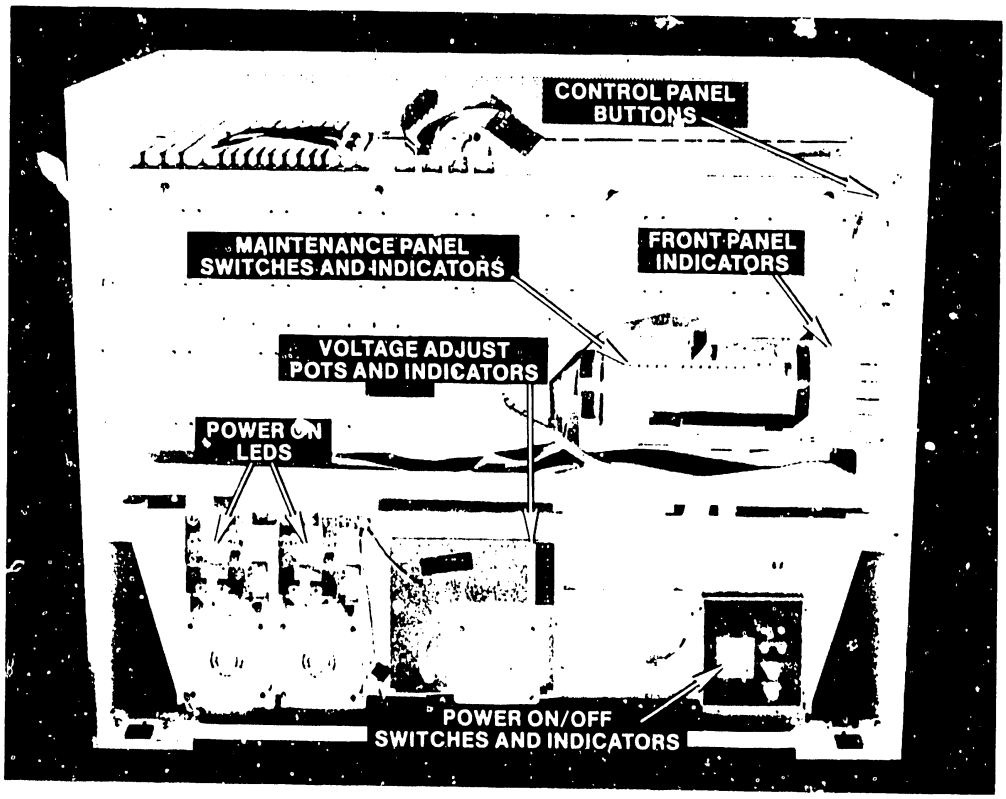


FIGURE 4-1 SWITCH AND INDICATOR LOCATIONS ON THE VS-100 MAINFRAME

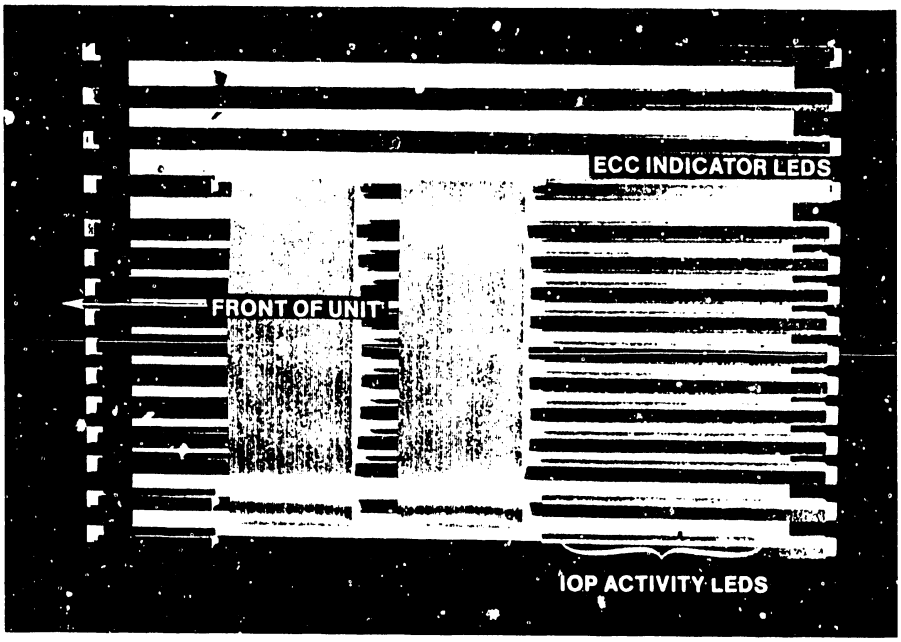


FIGURE 4-2 INTERNAL SWITCH AND INDICATOR LOCATIONS

4.2 POWER PANEL

Source-power is applied to the VS-100 Mainframe through the Power Box. Located on the front of the box are the Mainframe circuit-breaker, the Power-On Pushbutton, the Power-On LED, the Power-Off Pushbutton, and the Power-Off LED. (See Figure 4-3.)

To apply power to the Mainframe, switch the Mainframe circuit-breaker ON and press the Power-On Pushbutton. When the Power-On button is engaged, the Power-On LED is lit, indicating that power is being supplied to the Switching and Linear Power Supplies. If this LED does not light or goes on then extinguishes, a power supply problem exists on the System.

Removing power from the Mainframe consists of depressing the Power-Off Pushbutton and switching the circuit-breaker OFF. If the circuit-breaker is left ON, the Power-Off LED remains lit and the System fans remain on.

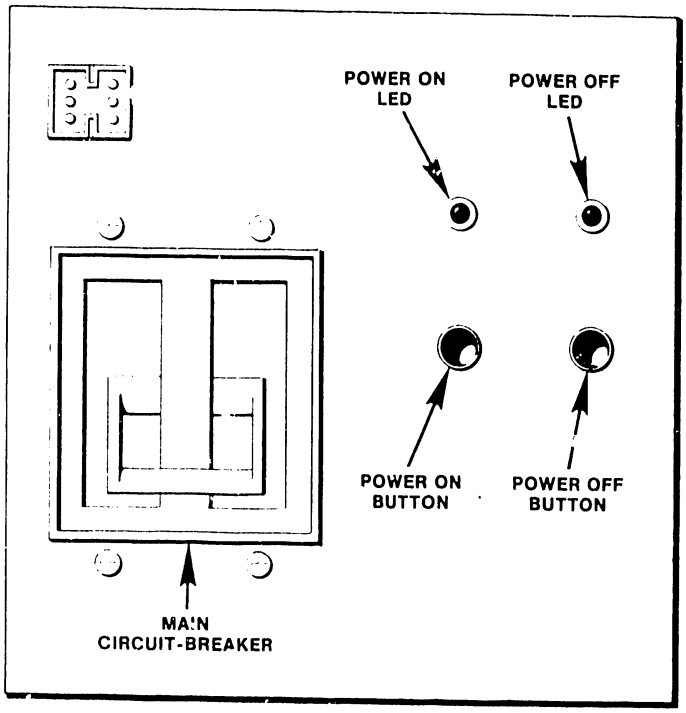


FIGURE 4-3 POWER PANEL SWITCHES AND INDICATORS

4.3 FRONT PANEL CONTROL BUTTONS

Located in the top right-front corner of the Mainframe, the Control Buttons allow the user to load System or diagnostic microcode, initialize the System, or force it into the Control Mode. These pushbuttons are part of the Front Panel board (210-7613) and are hardwired direclty to it. The four buttons are as follows silver BOOT (BT) pushbutton; black (or silver, depending on model) CONTROL MODE pushbutton; green LOAD pushbutton; and red INITIALIZE pushbutton. (See Figure 4-4.)

4.3.1 BOOT PUSHBUTTON

The silver BOOT button is used whenever operational or diagnostic microcode is loaded into the System. When pressed, this button causes the CPU to halt and load microcode from a diskette inserted in the mini-floppy drive. Successful loading is indicated by the READY LED on the Front Panel being lit--a flashing READY LED indicates the microcode failed to load properly.

4.3.2 CONTROL MODE PUSHBUTTON

Pressing the CONTROL MODE button sets the CM bit to one, forcing the CPU into the Control Mode. The CPU then issues an 'ALERT' command to BA 1 IOP 2 Port 0 where Workstation 0 must be connect d. The VS-100 Control Mode is similar in operation to the VS 60/80 Control Mode. Most CPU and System diagnostics are performed in the Control Mode. Refer to Chapter 8 for details.

4.3.3 INITIALIZE PUSHBUTTON

The green INITIALIZE pushbutton, when activated, forces the System into the 'Initialized' state. In this state, the System is as follows:

1. Main and Cache Memories, the Segment Control Registers (SCR's), and the CPU Reference and Change Table are all set to zero.
2. The Page Table for Segment Zero (Operating System) is loaded into the T-Ram for access by the CPU--remaining T-Ram entries are faulted.
3. The External Condition Register (ECR) is set to zero by the hardware as soon as the CPU begins executing microcode instructions. Because

zero equals Enable in the ECR, all System features under ECR control become enabled at Initialization.

4. The BA-Inhibit bits IN1 and IN2 are set to zero. In this case, zero equals inhibit preventing any IOP commands from accessing the BA until the CPU acknowledges the BA. IN2 remains at zero if BA2 is not installed.

5. The System Clock is zeroed and the Comparator bits are set to one. Because of this, the user must enter the Date and Time into the System whenever the System is Initialized using the INITIALIZE pushbutton.

4.3.4 SYSTEM LOAD PUSHBUTTON

The black SYSTEM LOAD pushbutton, when activated, causes the System to perform all functions as stated in Paragraph 4.3.3, steps 1 through 4. Because the System Clock is not zeroed and the Comparator bits are not set to one, however, use of the LOAD button eliminates the necessity of entering the date and time at the completion of initialization.

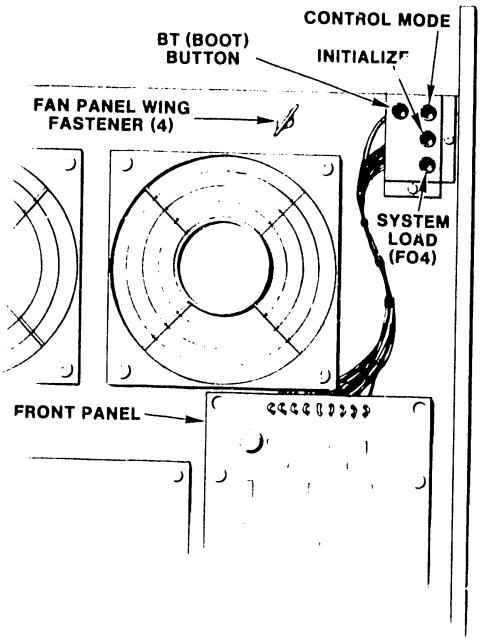


FIGURE 4-4 CONTROL PANEL SWITCHES AND INDICATORS

4.4 THE FRONT PANEL

Acting as a monitor of System status, the Front Panel provides the user with pertinent information concerning the operating condition of all I/O devices connected to the Mainframe as well as data concerning the CP status. The Front Panel consists of 20 LEDs arranged in five rows of four LEDs each. The top row of LEDs provides general CP information. The remaining 16 LEDs provide status checks on data transfers between the individual peripherals attached to the VS-100 and the Central Processor. (See Figure 4-4.)

4.4.1 CENTRAL PROCESSOR INDICATORS

The four indicators that make up the top row of LEDs on the Front Panel provide a quick check of CP status. The leftmost (Power-On) LED, when lit, indicates power has been successfully applied to the CP. The second (Ready) LED, when lit, indicates that microcode has been successfully loaded. When this LED is flashing, loading was unsuccessful. The third (Halt) LED ,when lit, indicates that the CPU is in the HALT state. The fourth (CM Parity Error) LED lights whenever the CPU detects any uncorrectable parity error in Control Memory.

4.4.2 PERIPHERAL STATUS INDICATORS

When lit, each of the remaining 16 Front Panel LEDs indicate the occurrence of a parity error in the control memory of the IOP associated with that particular LED. The first two rows of LEDs are associated with Bus Adapter 1, IOP numbers zero through seven. The second two rows of LEDs are associated with Bus Adapter 2, IOP numbers zero through seven. See Figure 4-5 for LED assignments.

4.5 INTERNAL INDICATORS

Located within the CP chassis are several indicators that provide the CE with important system status indications. These indicators are the ECC LEDs and the IOP Activity LEDs. A brief description of these LEDs follows. (See Figure 4-2 for location.)

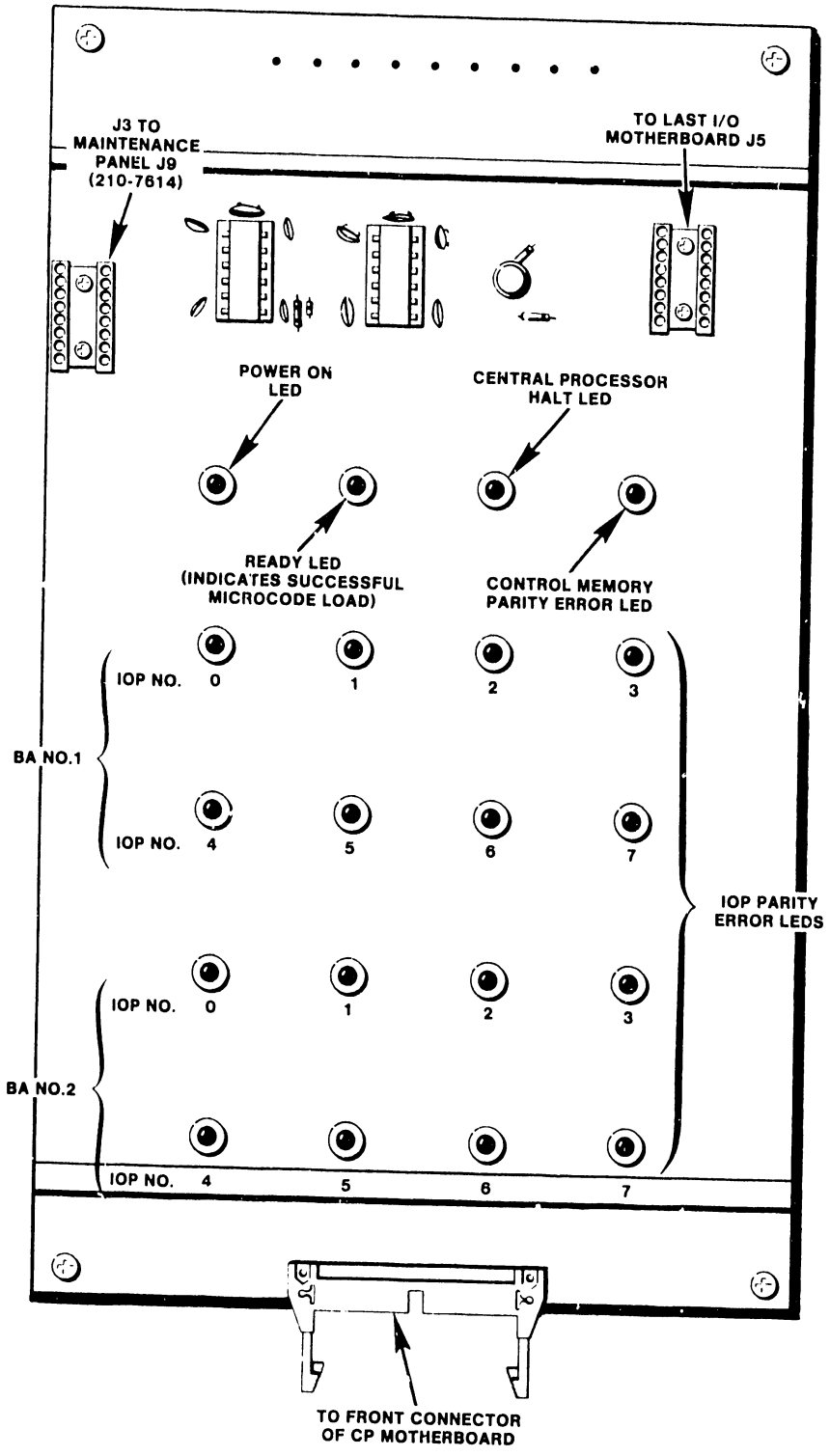


FIGURE 4-5 FRONT PANEL CONTROL BUTTONS AND INDICATORS

4.5.1 ECC INDICATOR LEDS

Located on the 7605 System Bus Controller card, these eight LEDs are used by the System to keep a running count of all single-bit parity errors detected and corrected. When maximum count has been reached (all LEDs lit), the counter is zeroed and counting begins again.

4.5.2 IOP ACTIVITY LEDS

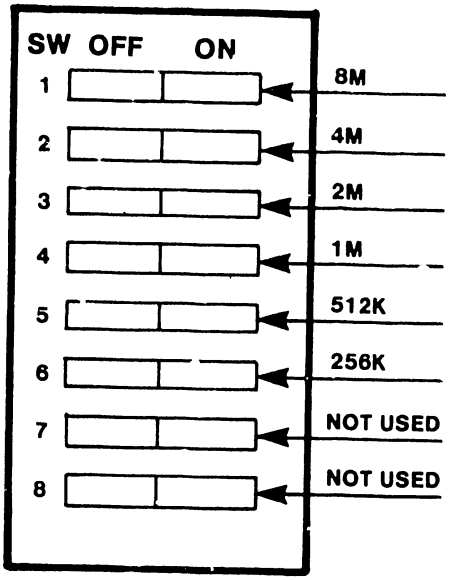
Located on the top edge of the 7611 Bus Adapter Card, these eight LEDs indicate which IOP is active at any given time. Whenever an IOP request for access to the CP is granted, the LED associated with that particular IOP lights and remains lit until the transaction is completed.

4.6 MEMORY SIZE SELECTION

An 8-position DIP switch located on the 7604 Cache Card and the number of 7603 Main Memory card pairs on the CP motherboard determine the size of Main Memory. Incorrect altering of switch settings, or altering of switch settings without adding the correct number of memory cards, can result in CP hangups and loss of data. Adding cards without altering switch settings results in no change in apparent memory size to the CP.

Switch settings on the Cache card are compared with the high-order memory adress bits (0-5) in L120 and L145 (7485 Comparator). If the switch setting is greater than or equal to the address bits, the System considers the address to be legitimate and *IMA goes High. If the switch setting is less than the address bits, *IMA goes Low (active) and the address is not processed. If the switches are set higher than the actual physical memory, however, the memory address will be accepted as legitimate and the CP will attempt to process the address. This can result in system hang-ups and possible data loss.

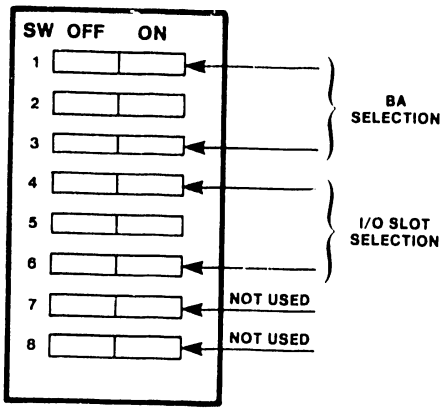
As of this writing, maximum Main Memory size is 2-Mbytes--four memory board pairs with 512-Kbytes of storage per pair. Minimum memory size is 512 Kbytes with memory increasing in 256-Kbyte increments, using half-loaded and fully loaded memory cards, until maximum size is reached. Figure 4-6 provides a set of tables for determining switch settings for different memory sizes.



SW NO. 8 7	6	5	4	3	2	1	MEMORY SIZE IN BYTES
NOT USED	1	0	0	0	0	0	256K
	0	1	0	0	0	0	512K
	1	1	0	0	0	0	768K
	0	0	1	0	0	0	1M
	1	0	1	0	0	0	1.2M
	0	1	1	0	0	0	1.5M
	1	1	1	0	0	0	1.7M
	0	0	0	1	0	0	2M

OFF = 1
ON = 0

FIGURE 4-6 MAIN MEMORY SIZE SELECTION



SW NO. 4	5	6	IOP NO.
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

SW NO. 1	2	3	BA NO
1	0	0	1
0	1	0	2
1	1	0	3*
0	0	1	4*

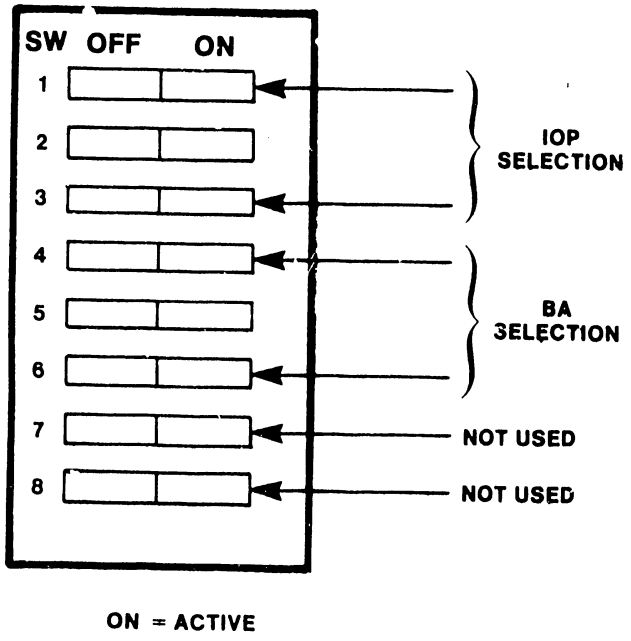
OFF = 1
ON = 0

* FOR FUTURE EXPANSION

FIGURE 4-7 IOP BOARD SWITCH SETTING (EXCEPT TC)

4.7 IOP SWITCH SETTINGS

An eight-position DIP switch on each IOP motherboard determines the location of the IOP on the I/O Motherboard. On all boards except the TC IOP, switches 1, 2, and 3 determine the Bus Adapter selected; switches 4, 5, and 6 determine the I/O slot on the motherboard; switches 7 and 8 are not used at this time. Refer to Figure 4-7 for an explanation of the switch settings for all IOPs except the TC IOP, which is shown in Figure 4-8.



SW NO.	1	2	3	IOP NO.
	0	0	0	0
	0	0	1	1
	0	1	0	2
	0	1	1	3
	1	0	0	4
	1	0	1	5
	1	1	0	6
	1	1	1	7

SW NO.	4	5	6	BA NO.
	0	0	1	1
	0	1	0	2
	0	1	1	3*
	1	0	0	4*

ON = 1
OFF = 0

* FOR FUTURE EXPANSION

FIGURE 4-8 TC IOP BOARD SWITCH SETTING

CHAPTER 5

INITIAL PROGRAM LOADING AND SYSGEN

CHAPTER 5
INITIAL PROGRAM LOADING AND SYSGEN

5.1 GENERAL SYSGEN INFORMATION AND REFERENCES

The VS-100 uses a dynamic SYSGEN procedure that simplifies the creation of a unique Operating System. With the dynamic SYSGEN, the user can create a configuration almost at will. Configurations can be created and stored on the System disk or the user can create a one-time configuration for a particular need at IPL.

B cause of the on-going changes to the VS SYSGEN Procedures, the SYSGEN Procedure instructions are being deleted from the VS-100 Product Maintenance Manual. The following are reference materials to be used when SYSGENing the VS-100:

For the complete SYSGEN procedures refer to VS System Management Guide, WLI P/N 800-1104SM-03.

For further information concerning changes and additions to the VS Operating System for Release 6.0, refer to VS Software Bulletin, Release 6.0, WLI P/N 800-3111-01.

5.2 DETERMINING PHYSICAL DEVICE ADDRESS (PDA)

Before IPLing, it may be necessary to change the Physical Device Address (PDA) of the IPL device. The following shows how to determine the PDA.

1. After pressing the Initialize pushbutton, Workstation #0 will display the following:

CONTROL MODE R00

2. a. If R00 (the default address) is the Physical Device Address (PDA) of the system disk (or the IPL disk), press ENTER to IPL.

b. If R00 is not the desired PDA, press the bACKSPACE key and enter F (for a fixed disk) or R (for a removable disk).

Calculate the PDA as follows:

(1) Determine the BA, IOP, and Port numbers of the system disk.

(2) Construct an 8-bit word as follows:

BIII PPPP

Where: B = 0 for BA1
= 1 for BA2

III = 000 for IOP0
= 001 for IOP1
= 010 for IOP2
= 011 for IOP3
= 100 for IOP4
= 101 for IOP5
= 110 for IOP6
= 111 for IOP7

PPPP = 0000 - 1111 for device 0 through 15

(3) In the example below, if the disk is located on BA1, IOP1, Port 4, the 8-bit word is 0001 0100. Converting the 8-bit word to HEX format gives a PDA of 14.

	BA	ICP#	PORT
BIT POSITION	0	123	4567
8-BIT WORD	0	001	0100
HEX RESULT		1	4

The LOAD command would then read: CONTROL MODE R14.

c. Enter the PDA into the LOAD command and press ENTER.

CHAPTER 6

MAINTENANCE AND ADJUSTMENT

CHAPTER 6
MAINTENANCE AND ADJUSTMENTS

6.1 GENERAL

This chapter consists of preventive maintenance requirements and necessary adjustments for the VS-100 Mainframe. Also included in this chapter is a discussion of the 'System Log Book'.

6.2 PREVENTIVE MAINTENANCE

Periodic maintenance is essential to the proper operation of the VS-100 Mainframe and associated peripherals. Because of its design, the Mainframe requires a minimum amount of maintenance to ensure continued efficient operation. Scheduled maintenance for the Mainframe will be performed quarterly, and is as follows:

1. Inspect and clean, if necessary, the filters attached to the front cover of the Mainframe.
2. Inspect the interior of the Mainframe for any noticeable accumulation of dust or debris, or any loose hardware connections. Refer to Chapter 7 for disassembly procedures.
3. Check and adjust, if necessary, the Power Supply voltages. Refer to Paragraph 6.4 for adjustments.
4. Perform all applicable Mainframe and peripheral diagnostics. Refer to Chapter 8 of this document for Mainframe diagnostics and Category III for periheral diagnostics.
5. Inspect all muffin fans for proper operation. Ensure that all fans spin freely and are not obstructed in any way. Replace damaged fans. Refer to Chapter 7 for replacement procedures.
6. Inspect the mini-diskette drive read/write heads for any noticeable oxide build-up; clean if necessary. (Refer to Paragraph 6.5.4.)

6.2.1 PERIPHERAL PREVENTIVE MAINTENANCE

Refer to the appropriate documents in Classification III Categories A

through H for PM procedures for all VS-100 associated peripherals.

6.2.2 TEST EQUIPMENT AND TOOLS

The majority of all VS-100 Mainframe maintenance and repair procedures can be performed using the following tools and test equipment:

1. Customer Engineering Standard Tock Kit (WLI P/N 726-9401) containing the following :
   a. Allen Wrench (Hex Key) Set.
   b. Small Slotted Screwdriver (insulated shaft) (WL #726-9406) - for voltage adjustments.
   c. Medium Phillips Screwdriver (WL #726-9407).
   d. Medium Slotted Screwdriver (WL #726-9408).
   e. Handle and Assorted Nutdrivers (WL #726-9478, 726-9469 through 9477).
2. Digital Voltmeter - accuracy of at least $\pm$.1% of full scale and 1 mv. resolution factor. (Acceptable Type/Equivalent: FLUKE #8000A.)
3. Oscilloscope with two X1 probes and/or two X10 probes. (Acceptable Type/Equivalent: TEKTRONIX #465.)
4. Alcohol Pads - for R/W head cleaning (WL #660-0130).

6.3 THE SYSTEM LOG BOOK

Because of the size of the VS-100 CPU and the number of peripherals it is capable of handling, it is difficult for a CE to keep track of problems, P.M. schedules, and correct equipment revision levels. Add to these problems the fact that several different CE's may cover an account or different on-site shifts can be faced with different troubles, and it is readily apparent that repair and maintenance becomes more confusing as system size increases. For these reasons, a properly maintained system log book can be an important tool in cutting down duplication of effort when following ongoing or intermittent problems. It also allows for smoother and more co-ordinated shift turn-overs.

Although Call Reporting Booklets serve an important function, they were not designed for use with a large-scale computer system. To fill this need, the System Log Book has been created. The Log is designed as a means of

documenting and aiding in future troubleshooting of system faults; it should be updated only by the engineer who handles the trouble call. The System Log Book is divided into the following sections:

1. Section One contains customer statistics that may be needed on a trouble call. Included in this section are emergency phone numbers (police, fire, etc.) and an Equipment Statistics sheet that will list all equipment attached to the system, along with the serial numbers and other vital statistics.
2. Section Two is the software/hardware update section. Each update/ECN will be logged in this section for quick reference. Each update/ECN will also appear in the quick log and device log for a particular piece of equipment.
3. The Quick (or 'Running Fault') Log composes Section Three. All service calls will be logged here. The date and time will be logged, as well as the type (software or hardware) of fault. The device number, a brief description of the fault, and the signature of the CE answering the call will also be included here.
4. Section Four consists of a series of device categories (Disk, Tape, Etc.) where problems associated with individual pieces of equipment will be logged. These categories will serve as the Device (or 'Equipment History') Logs. Entries should include all symptoms and information gathered by the CE(s) involved and a step by step description of the solution. Everything done to the system should be included whether or not it solved the problem. This expedites follow-up repairs in areas where a new problem may have been inadvertently injected during a long troubleshooting procedure. This section is designed to help the C.E. taking a call at an unfamiliar site. It also aids the site C.E. in troubleshooting a long-term or intermittent problem.
5. The last section of the system log is the Preventive Maintenance Schedule. Each piece of equipment for the system will be listed by model and serial number on a chart containing maintenance date headings. Next to each device a letter (Weekly, Monthly, Quarterly, Semi-Annually, or Annually) specifying required maintenance intervals will be placed in the column that corresponds to the maintenance date written in at the chart top.

A properly maintained System Log Book can be a valuable troubleshooting aid to the CE. It provides the CE with complete maintenance and problem histories for each device on a customer's System.

6.4 MAINFRAME VOLTAGE ADJUSTMENTS

Voltage adjustments are performed at initial installation and every three months thereafter. All adjustment pots except the +5VA and +5VB pots, all test-points, and all voltage-sensing LED's are located on the Wang linear power supply chassis. The +5VA and +5VB voltage adjustment pots are located on the front of the individual switching supplies. (See Figure 6-1 for test point locations.)

The following voltages and their limits, listed in the sequence they appear on the power supply unit, are checked and adjusted on the VS-100.

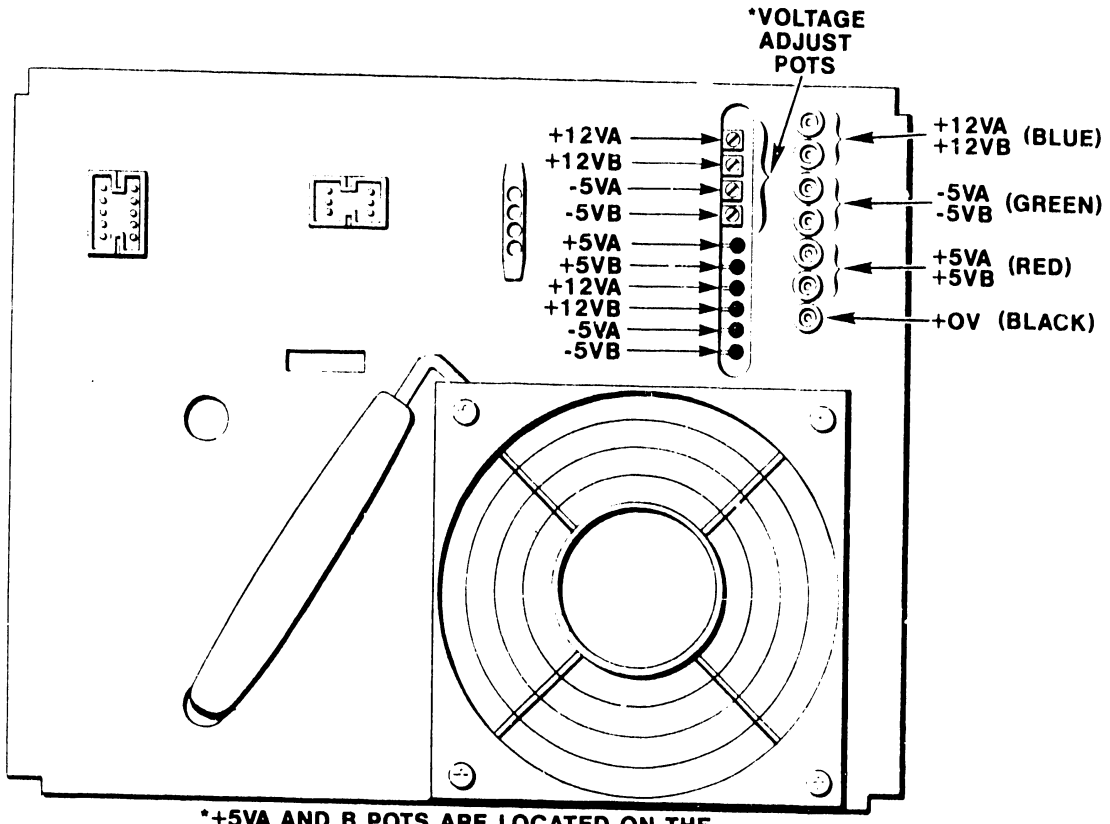
VOLTAGES	VOLTAGE AT TEST POINT	OPERATING LIMITS
+12VA	+12.1	±0.1V
+12VB	+12.1	±0.1V
+5VA	+5.1	±0.1V
+5VB	+5.1	±0.1V
-5VA	-5.1	±0.1V
-5VB	-5.1	±0.1V

6.4.1 VOLTAGE SENSING LEDS

The Voltage Sensing LEDs are located on the Wang Linear Power Supply chassis to the left of the voltage test points. These LEDs indicate whether or not the correct voltages are being applied to the Mainframe. At initial power-up these LEDs light in sequence as the different voltages are applied to the Mainframe.

NOTE

The voltage-sensing LEDs indicate a trouble condition when they are NOT lit; normal status is ON. These LEDs merely indicate that the voltage is present at the power supplies, they do not indicate that actual voltage on the motherboards is correct.



*+5VA AND B POTS ARE LOCATED ON THE INDIVIDUAL SWITCHING SUPPLIES.

VOLTAGE ADJUST TABLE

OUTPUT VOLTAGE	OPERATING VOLTAGE*	OPERATING LIMITS	MARGINAL ERROR-TESTING LIMITS
+12VA	+12.1	±0.1 (±9%)	±0.25 (±2%)
+12VB	+12.1	±0.1 (±9%)	±0.25 (±2%)
-5VA	-5.1	±0.1 (±2%)	±0.25 (±5%)
-5VB	-5.1	±0.1 (±2%)	±0.25 (±5%)
+5VA	+5.1	±0.1 (±2%)	±0.25 (±5%)
+5VB	+5.1	±0.1 (±2%)	±0.25 (±5%)

* ALL MEASUREMENTS MADE AT TEST POINTS ON LINEAR POWER SUPPLY

FIGURE 6-1 VOLTAGE TEST-POINT AND ADJUSTMENT POT LOCATIONS

6.5 THE MINI-DISKETTE DRIVE

The VS-100 uses a Shugart SA-400 minifloppy drive for loading operational and diagnostic microcode into Control Memory. The SA-400 is used as a READ-ONLY device; the VS-100 cannot write onto a diskette in the drive.

The mini-diskette used in the SA-400 contains 35 tracks divided into 10 sectors per track. Each sector contains 256 bytes of data, providing a total of 90-Kbytes of storage. On the VS-100, the CP micro-program resides on the first 15 tracks of the diskette.

When the silver 'BT' button is depressed, data is transferred directly from the diskette to Control Memory, bypassing the data path used in communicating with other peripherals attached to the Mainframe. Data is transmitted from the diskette starting at Sector 0 and gated into Control Memory starting at micro-location 0; data transfer continues until all microcode instructions are transmitted.

6.5.1 THE MINI-DISKETTE DRIVE CONTROLLER

Because the SA-400 is employed as a read-only device, the drive controller board governs data transfers FROM the mini-diskette drive TO the VS-100 Control Memory (CM). Data is transferred in 256-byte blocks to the CM one byte at a time from the drive. A Z80 CPU on the mini-disk controller board monitors the searching of tracks and sectors on the diskette.

The Z80 CPU uses three main commands when communicating with the minifloppy drive:

1) IN00 - Used to enable a byte of data on the data bus.

2) IN01 - Used to read track, sector and error status conditions.
   ZD7 - ON (One) - CRC ERROR
   ZD6 - ON (One) - SECTOR MARK
   ZD5 - ON (One) - INDEX MARK
   ZD4 - ON (One) - TRACK ZERO

3) OUT00 - Used to control the minidiskette drive.

ZD5 - ON (One) - Sync Pulse present

ZD4 - ON (One) - TURN ON the Re dy Light

OFF (Zero) - TURN OFF the Ready Light

ZD3 - ON (One) - Supply the initialize pulse to the VS-100 CPU

ZD2 - ON (One) - MOTOR ON

ZD1 - ON (One) - DIRECTION pulse ON

ZD0 - ON (One) - STEP pulse ON

6.5.2 DATA SEPARATOR THEORY

READ DATA*, a combination of clock and data pulses coming from the diskette, enters the controller at L13 pin 1, where the signal is amplified and inverted. From the inverter, READ DATA* appears at pins 13 and 10 of L7. Also present, at L7 pins 9 and 12, are the clock and data separator signals from pin 7 and pin 10, respectively, of L6.

The output signal at L7 pin 11 is the data separated from READ DATA*. The output signal at L7 pin 8 is the clock pulse. The data signal appears at L14 pin 4 and is gated out of L14 at pin 5 by the occurance of the clock signal at L14 pin 3. From here the data signal appears at pins 1 and 2 of L3, a serial-to-parallel 8-bit shift register. At this time, the data is converted from serial to parallel: most significant bit at pin 13, least significant at pin 3.

The decode of the three sync bits (011, a combination of SYNC*, and L3 pins 4 and 5) by L8 produces a LOW, which is applied to L22, forcing the output of pin 8 ($*Q_2$) low. This low is applied to L23 pin 1, clearing it. L23 is an asynchronous clear counter, preloaded to one, used to count the 8 bits of each data byte. At the count of 8, the output at L23 pin 11 goes HIGH clocking L4 pin 11 and holding the byte of data until L4 receives IN00 (out enable signal) at pin 1. When a byte of data is ready for transfer to control memory, A15* is applied to L5 pins 1 and 19.

As soon as IN00 is applied to L4 pin 1, data is transferred over the data bus lines via L5 to control memory along with the address, which is transferred via L1 and L2. The Z80 CPU on the disk controller supplies and keeps track of this address.

After every 256 bytes of data, two CRC bytes are read into L34 and checked by the Z80 CPU. If the CRC check produces a zero output at L34 pin 13, no error has occurred during the data transfer to Control Memory. If an error is detected, the Front Panel READY LED on the VS-100 chassis flashes.

After successfully reading all sectors, the Z80 causes the READY LED on the front panel to go to the steady-on state.

6.5.3 MINI-DISKETTE DRIVE DATA SEPARATOR ADJUSTMENTS

Because data and clock signals enter the minifloppy drive controller board combined in one signal called READ DATA*, the clock pulses must be separated from the data. This is done in the Data Separator circuit. The two separator pulses are outputs of a VCO, and must be in sync with READ DATA* for the Data Separator to function correctly. This procedure details the steps required to align the separator pulses with READ DATA*.

6.5.3.1 REQUIRED EQUIPMENT

1. Tektronix 465 Oscilloscope (or equivalent)
2. 8-inch clip lead
3. Phillips screwdriver
4. Mini-Diskette (any known good diskette available)
5. Narrow-blade screwdriver for pot adjustments

6.5.3.2 PRELIMINARY PROCEDURES

Before adjusting the separator pulses, perform the following:

1. Power OFF the Mainframe and place the circuit breaker in the OFF position.
2. If necessary, remove the top and front covers from the Mainframe.
3. Remove the mini-drive from the Mainframe (see Figure 6-2) and set it UPSIDE down on an INSULATED work surface sufficiently low enough to re-attach the minifloppy connector plugs.
4. Re-attach the power and Maintenance Panel connectors and apply power to the Mainframe.

5. Insert the known good mini-floppy diskette.
6. If a dual-trace oscilloscope is being used, set it up as follows:
   a) Power-up the oscilloscope.
   b) Set Volts/Div to 2 Volts.
   c) Set Time/Div to 1 microsecond.
   d) Set Slope negative.
   e) Set Source to Channel one.
   f) Set Coupling to DC.
   g) Set AC-GND-DC to DC.
   h) Set Vert Mode to CHOP.
   i) Ensure that probes are grounded.
   j) Connect the clip lead from TP_3 (L19-6) to ground.
   k) Connect probe 1 to TP_1 (L6-7). (See Figure 6-3.)
   l) Connect probe 2 to TP_2 (L6-9). (See Figure 6-3.)

6.5.3.3 PERFORMING THE ADJUSTMENT

Adjust the Clock Separator pulse as follows:

1. The display obtained from TP_1 is the Clock Separator signal. The total waveform period must be 8 microseconds from the trailing edge of the first pulse to the trailing edge of the second pulse.
2. Adjust R2 on the mini-disk controller board until the negative portion of the waveform is exactly six microseconds long. The positive-going portion of the waveform must be two microseconds long.
3. If an 8-microsecond pulse cannot be obtained, either the diskette is defective or the drive itself is bad. Attempt the adjustment procedure using a new mini-diskette. If no change in waveform occurs, replace the drive.

Adjust the Data Separator pulse as follows:

1. The display obtained from TP_2 is the inverse of the actual Data Separator pulse. The total waveform period of this pulse must be 8 microseconds from trailing edge to trailing edge.
2. Adjust R1 on the mini-disk controller board until the negative portion of the waveform is exactly five microseconds long. This portion is

the window that allows the data bits to be gated through the NAND gate. The positive-going waveform must be three microseconds long. It prevents Clock signals from passing through the NAND gate.

3. If an 8-microsecond pulse cannot be obtained, either the diskette is defective or the drive itself is bad. Attempt the adjustment procedure using a new mini-diskette. If no change in waveform occurs, replace the drive.

If a single trace oscilloscope is used, the procedures remain essentially the same. The oscillscope settings must be changed, however, when going from TP_1 to TP_2. Refer to the settings given in Paragraph 6.5.3.2.

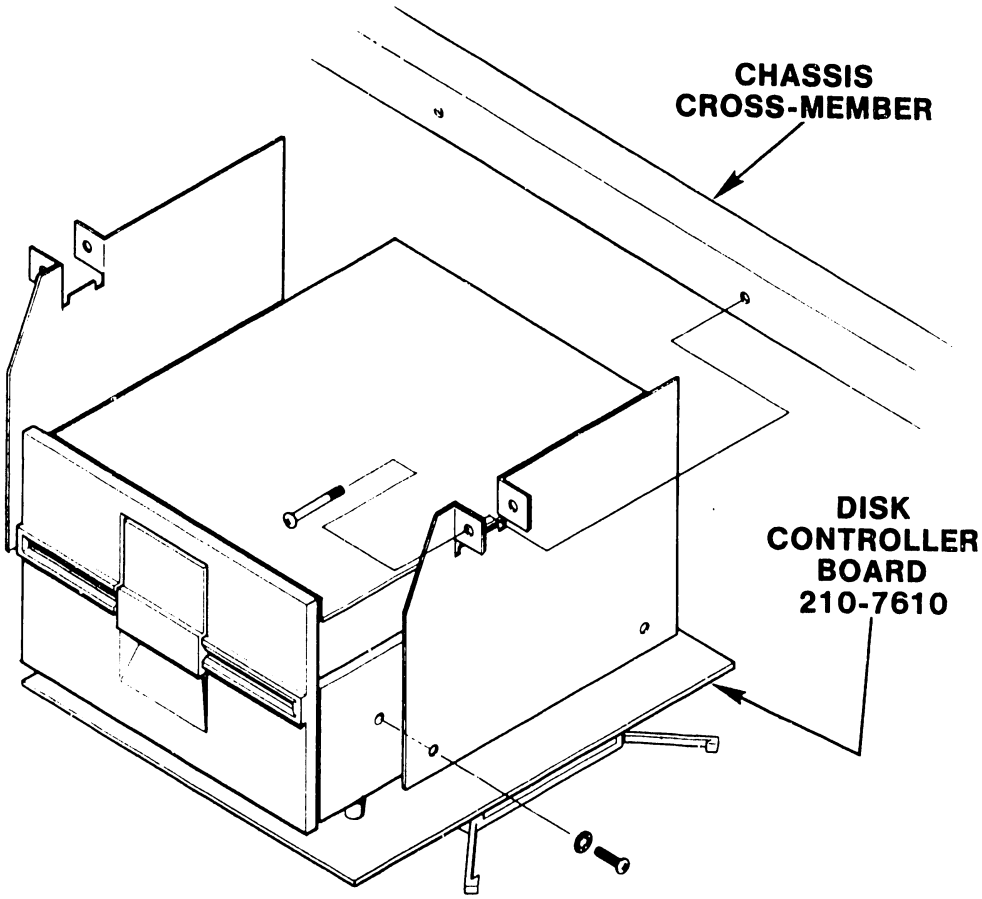


FIGURE 6-2 REMOVING THE SA-400 MINIDISKETTE DRIVE

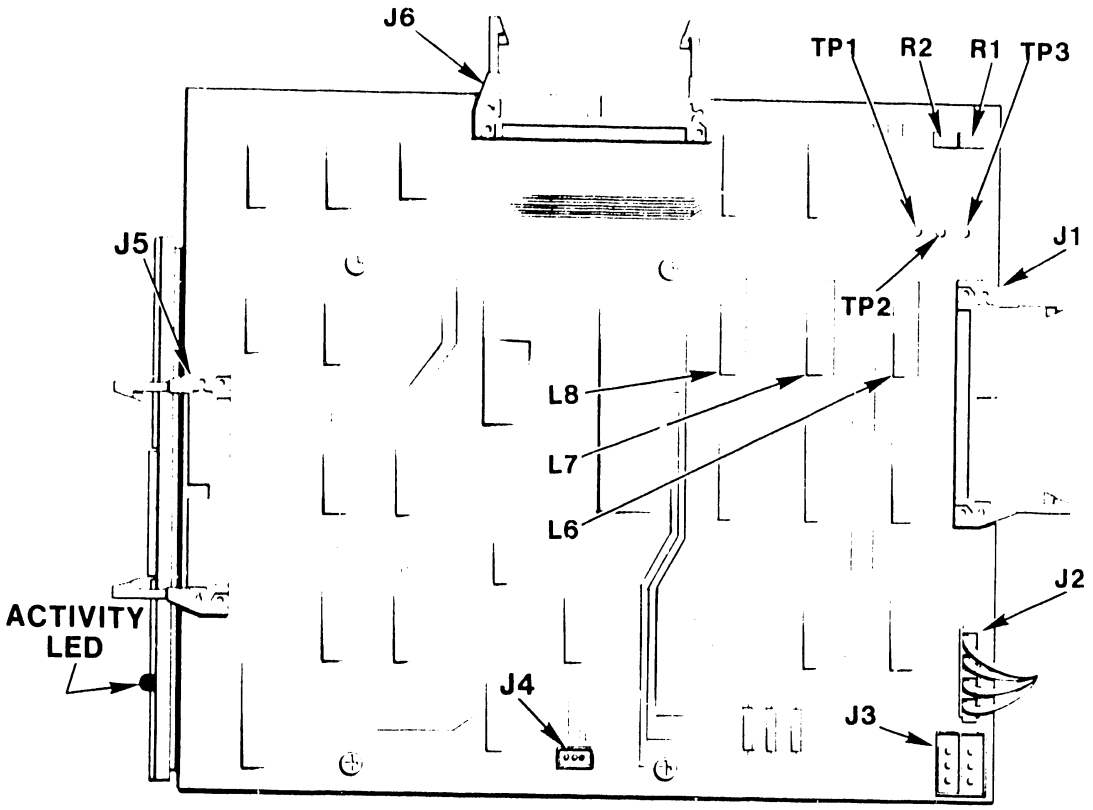


FIGURE 6-3 CONTROLLER BOARD CONNECTOR AND TESTPOINT LOCATIONS

6.5.4. CLEANING THE DRIVE HEADS

As part of the normal maintenance routine, the minidiskette drive heads will be inspected for dirt or damage. If an oxide build-up is detected during this inspection, the heads must be cleaned to ensure continued proper operation of the drive. Clean the heads as follows:

CAUTION

Cleaning methods and materials other than those specified below can permanently damage the head and should be avoided.

---

1. Remove the mini-drive as described in Paragraph 7.9.
2. Lift the load arm off the head, being careful not to touch the load button.

3. With an alcohol pad (WL #660-0130), lightly wipe the head.
4. After the alcohol has evaporated, lightly polish the head with a clean, lint free tissue.
5. Gently lower the load arm back onto the head. Do NOT let the load arm snap back into place as this could permanently damage the drive head.

CHAPTER 7

REMOVAL AND REPLACE-MENT

CHAPTER 7
REMOVAL/REPLACEMENT PROCEDURES

7.1 REMOVAL/REPLACEMENT OF MAJOR MAINFRAME COMPONENTS

This chapter describes the steps involved in removing and replacing or re-installing all major field-replaceable components in the VS-100 Mainframe.

7.2 TOP COVER REMOVAL

At the rear of the Mainframe, two slot-head fasteners secure the top cover to the back panel. (See Figures 7-1 and 7-1A.) Using a wide-blade screwdriver, disengage the fasteners by turning them ½-revolution counter-clockwise. With the fasteners free, slide the top cover 2-3 inches to the front to disengage the top cover from the front cover catch. This frees the top cover from the main chassis. At the front of the Mainframe, firmly grasp the top cover on each side and lift it up and away from the chassis. Re-install the top cover by reversing this procedure.

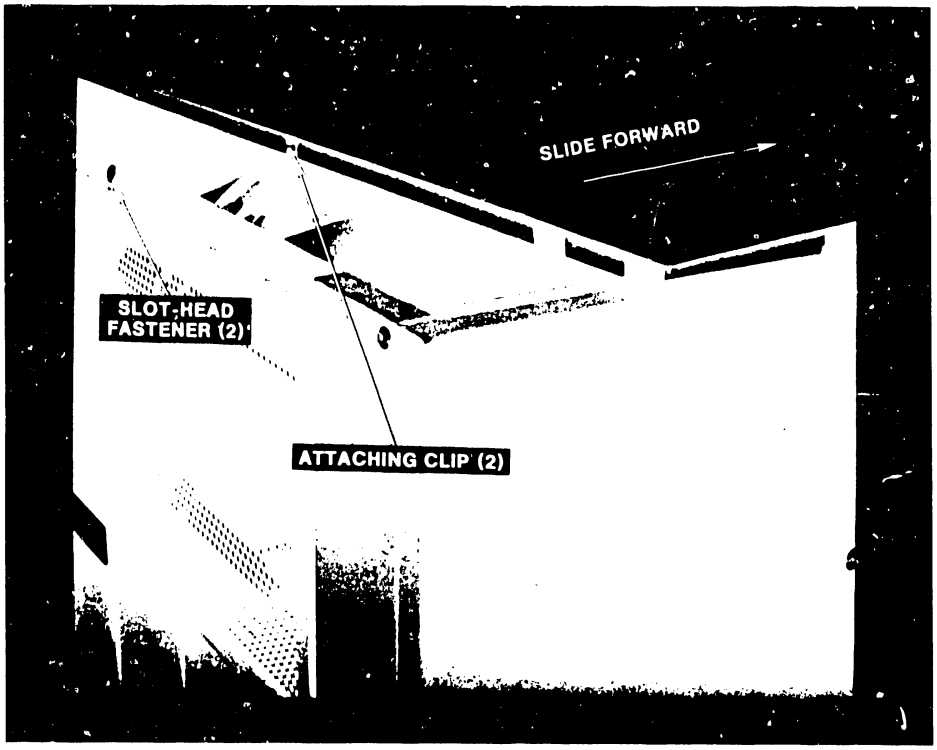


FIGURE 7-1 TOP COVER REMOVAL

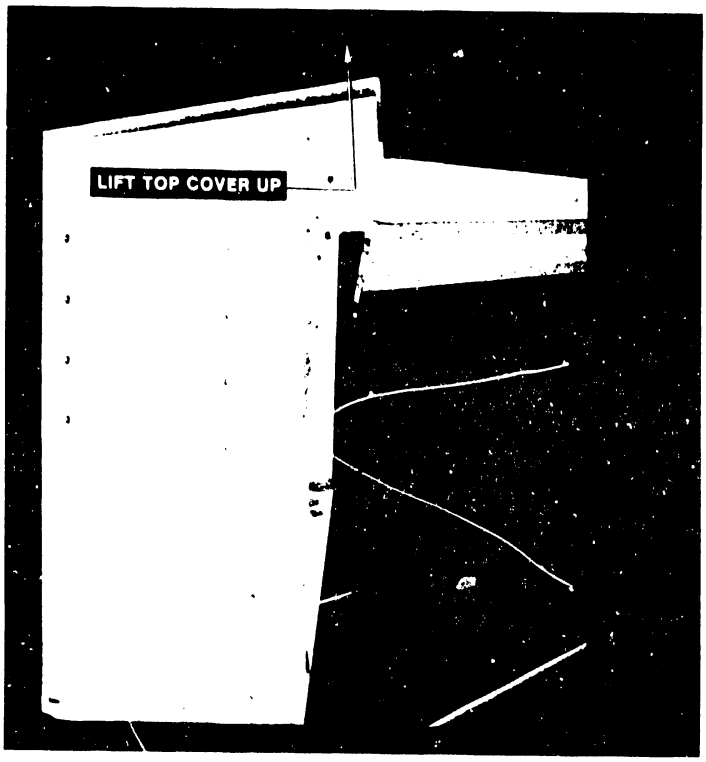


FIGURE 7-1A TOP COVER REMOVAL

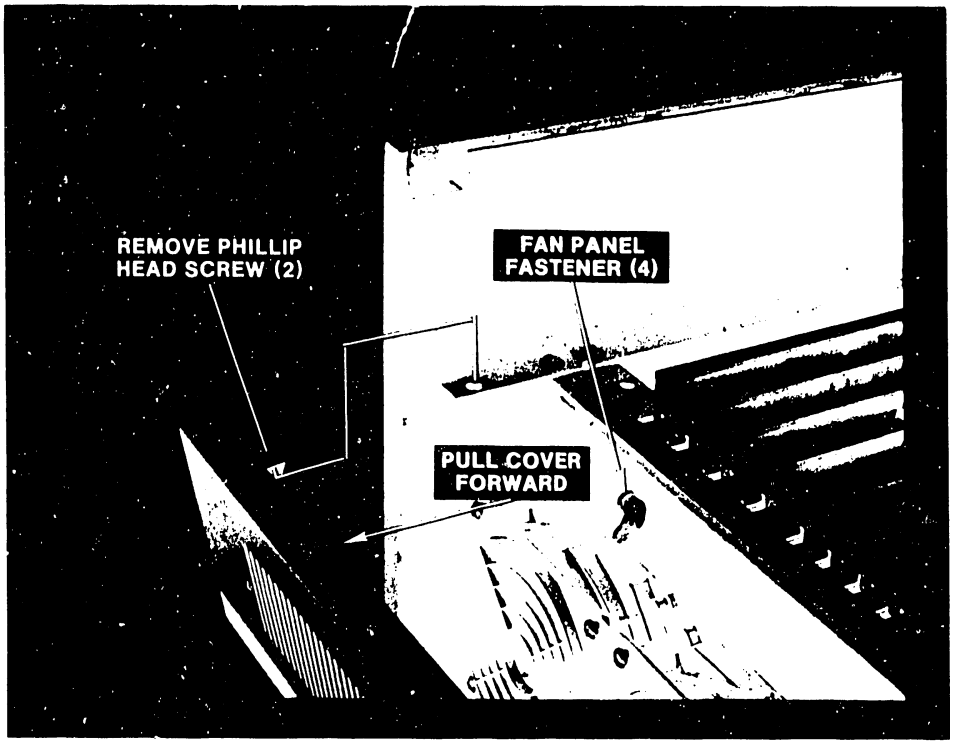


FIGURE 7-2 FRONT COVER REMOVAL

7.3 FRONT COVER REMOVAL

Remove the front cover as follows: (See Figures 7-2 and 7-2A.)

1. Open the hinged panel on the right side of the frontcover and remove the Front Panel board from it. Hang the Front Panel board on the hook provided for it on the main chassis. (See Figure 7-9.)
2. Remove the top cover as described above.
3. With the top cover removed, use a flat-blade screwdriver to remove the screws located on the top left and right corners of the front cover.
4. After removing the two screws, tilt the cover away from the chassis and remove the two ground straps located in the lower left and right corners of the cover.
5. The front cover attaches to the lower part of the chassis by means of two metal tabs inserted into plastic slots on the chassis. Grasp the front cover firmly and lift it up and out of the chassis.

Re-install the front cover by reversing this procedure.

FIGURE 7-2A FRONT COVER REMOVAL

7.4 FAN REMOVAL

CAUTION

Because of the high current passing through the connector block at the front of the chassis, power-down the Mainframe and place the circuit breaker in the OFF position before performing the following procedures.

The eleven cooling fans used in the VS-100 are mounted on a hinged fan assembly. Before an individual fan can be removed, the fan assembly must be lowered. Lowering the assembly also allows easy access to all circuit cards and motherboards. The following paragraphs describe the procedures involved in lowering the panel and removing a fan.

7.4.1 LOWERING THE FAN ASSEMBLY

Lowering the fan assembly requires the loosening of four wing-head stud fasteners, which secure the top of the fan assembly to the main chassis. (See Figure 7-3.) Loosen the fasteners by turning them ½-revolution counter-clockwise. Once all fasteners are loose, grasp the top of the panel and pull it away from the chassis. Lower the panel to the down position.

7.4.2 REMOVING A FAN

Remove a damaged or defective muffin fan as follows: (See Figure 7-4.)

1. Power-down the Mainframe and place the circuit breaker in the OFF position.
2. Disconnect the plug on the lower left corner of the fan to be removed.
3. Lower the fan assembly as described in paragraph 7.4.1.
4. Remove the four screws securing the fan to the fan assembly.
5. Remove the fan from the panel.

To install a fan, reverse the above procedure.

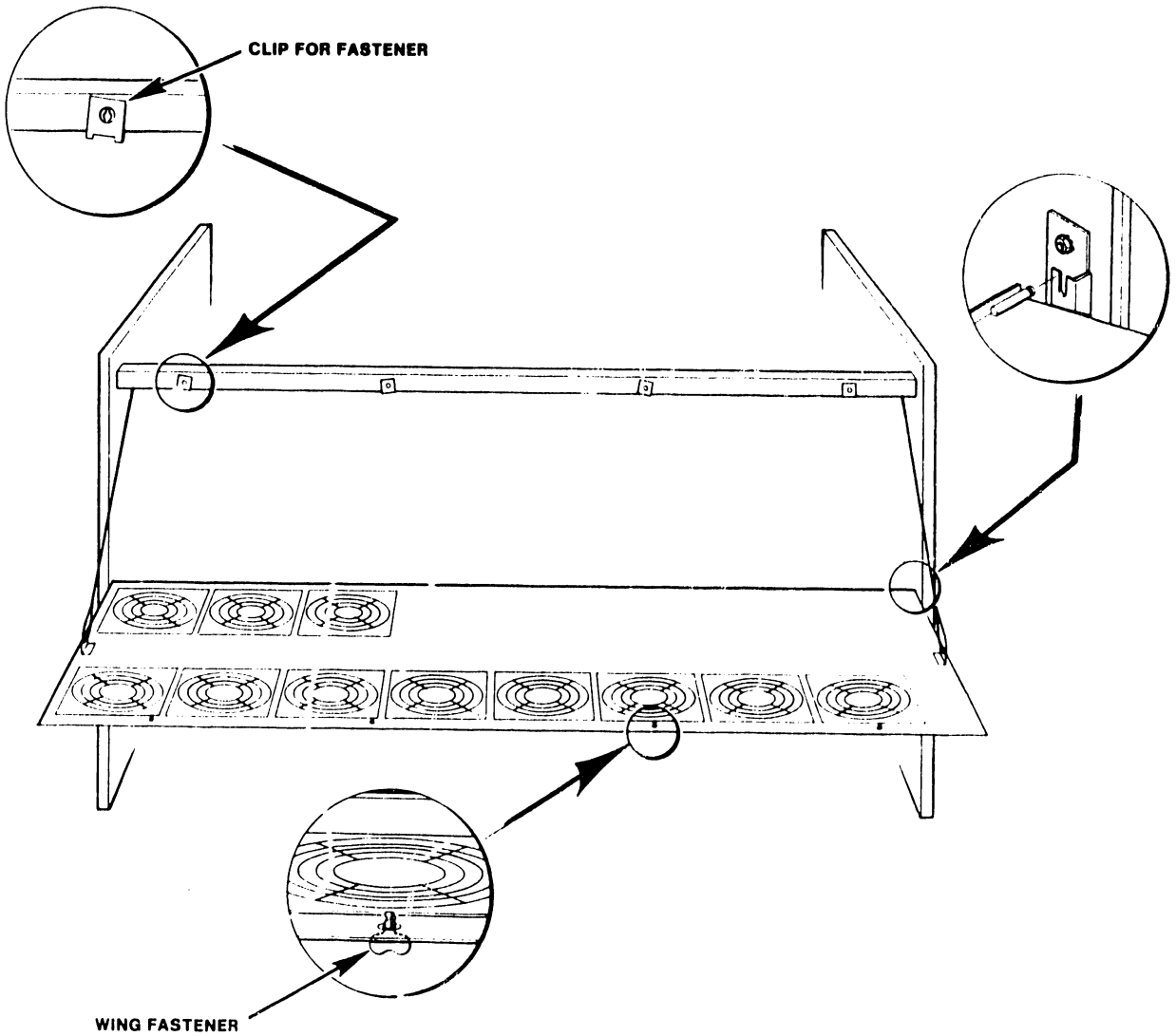


FIGURE 7-3 LOWERING THE FAN ASSEMBLY

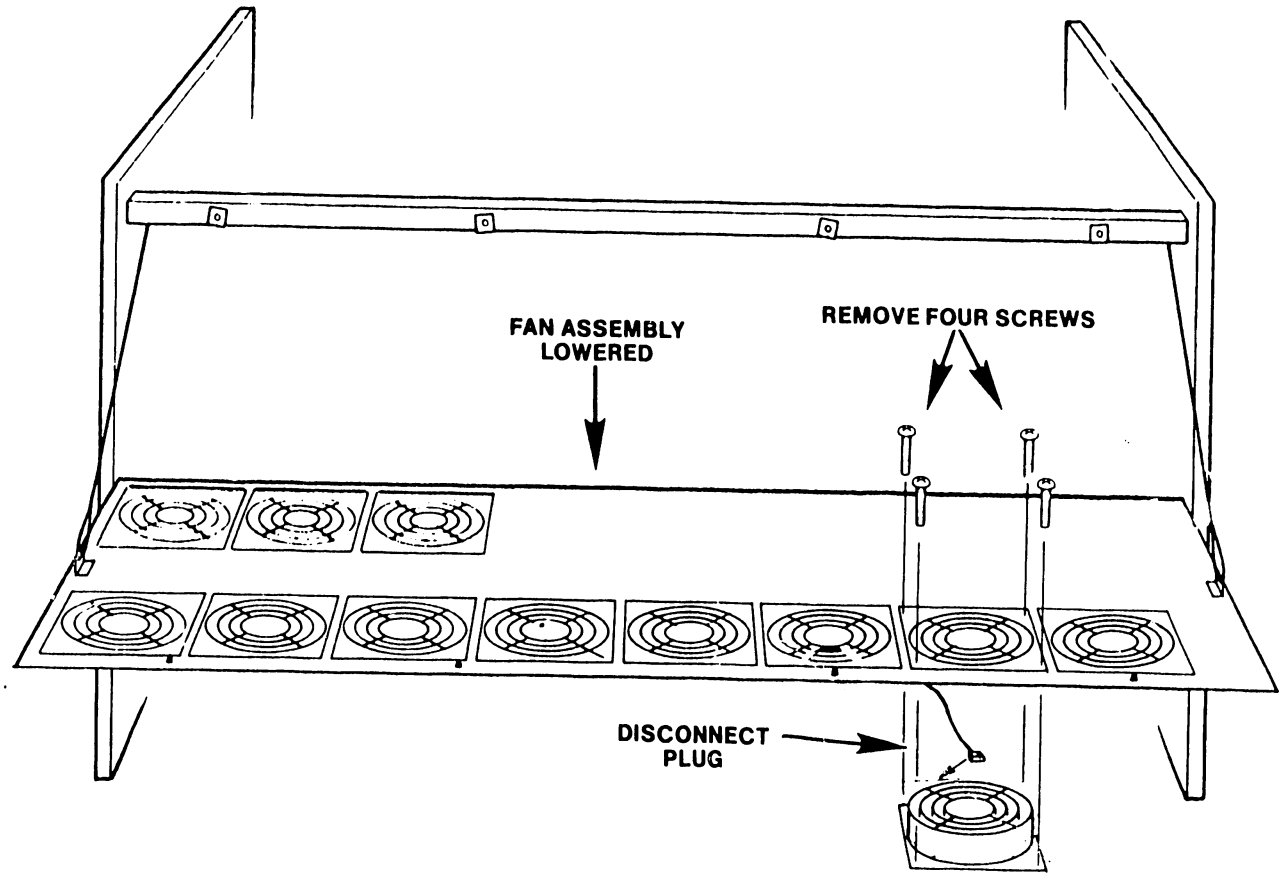


FIGURE 7-4 REMOVING A FAN

7.5 CIRCUIT CARD REMOVAL

Two types of circuit cards are found in the VS-100: CP cards and I/O cards. Following are the procedures to remove both types.

7.5.1 REMOVING A CENTRAL PROCESSOR CIRCUIT CARD

There are seven different CP cards found in the VS-100. The removal procedures for the different boards are given in the order in which they are found on the CP Motherboard. The cards are removed as follows:

1. Power down the Mainframe and place the circuit breaker in the OFF position.
2. Before removing the 7602 Control Memory card, disconnect the 16-pin ribbon cable from the component side of the card and the two cables attached to the left edge (as seen from the non-component side) of the card. Once the cables are disconnected, remove the card by grasping the top corners and gently rocking it from side-to-side while exerting a steady upward pressure. Once the card is free of the slot, ease it up and out of the Mainframe.
3. Remove both the 7600 A-Bus and 7601 B-Bus cards in the manner as described in step 2.
4. Remove the two 60-pin connectors from the top edge of the 7604 Cache Memory card that attach to the 7611 Bus Adapter card(s). Remove the two 64-pin connectors that attach to the 7605 System Bus Controller from the right edge of the 7604 Cache Memory card. Remove the Cache card in the same manner as previous cards.
5. Remove the two 60-pin connectors from the left edge of the 7605 System Bus Controller (SBC) card that attach to the 7604 Cache card. Remove the two 60-pin connectors from the right edge of the SBC that attach to the 7611 BA card. Remove the SBC in the same manner as other cards.
6. Remove the 7603 Main Memory cards in the same manner as previous cards.
7. Remove the two 60-pin connectors from the top edge of the 7611 Bus Adapter (BA) card that attach to the 7604 Cache card. Remove the two 60-pin connectors that attach to the BA from the right edge of the 7605 SBC. Remove the BA in the same manner as previous cards. (There may be two BAs, depending on the number of IOP devices installed.)

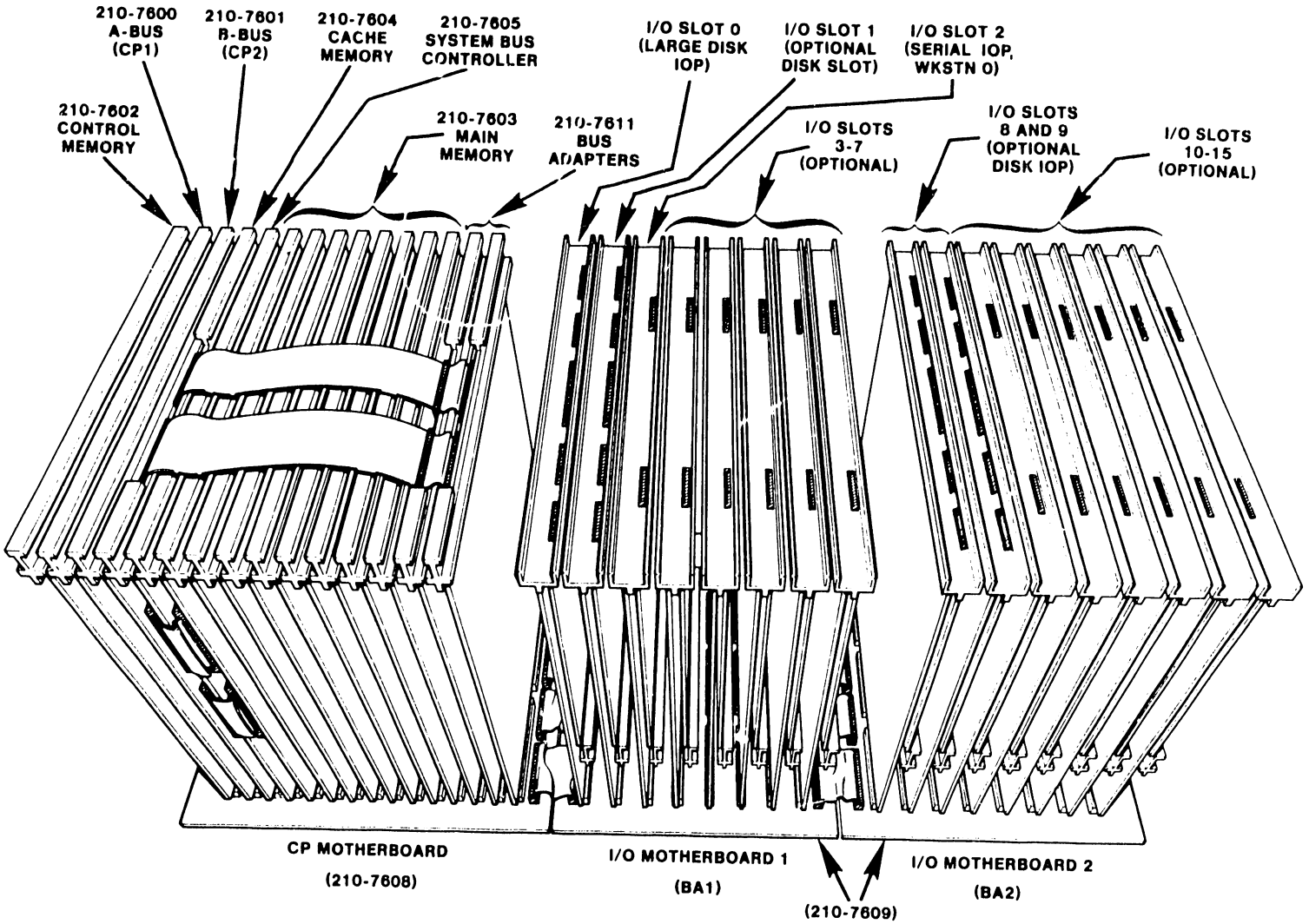


FIGURE 7-5 CPU AND I/O MOTHERBOARD LAYOUT

Re-install the circuit cards by reversing the above procedures. Ensure that all cables running to the various cards are re-installed in the correct locations and all cards are seated firmly in place. (See Figure 7-5.)

7.5.2 REMOVING AN I/O ASSEMBLY

As of this writing, there are four different types of I/O assemblies. All four types are removed in a similar manner, as follows: (See Figure 7-5.)

1. Power down the Mainframe and place the circuit breaker in the OFF position.
2. Remove all connectors from the top of the I/O assembly. Note the position of all connectors for later re-assembly.
3. Grasp the I/O assembly at the top corners and loosen it from its motherboard slot by gently rocking it from side-to-side while exerting a steady upward pressure.
4. Once the I/O assembly is free, ease it up and out of the Mainframe.

Re-install the I/O assemblies by reversing the above procedures. Ensure that all cables connected to the assemblies are re-installed in their appropriate locations and that all assemblies are seated firmly in place.

7.6 MOTHERBOARD REMOVAL

Because of the complexity of the task, removal of the CPU or I/O motherboard should be undertaken only if it has been determined conclusively that the fault is in the motherboard. The following paragraphs describe the procedures involved in removing the VS-100 motherboards.

CAUTION

When re-installing the CPU or I/O motherboards, ensure that no conductive (metal) parts of the motherboard come in contact with the Mainframe chassis. This could cause a short to ground on the motherboard resulting in serious damage to CPU or I/O cards and assemblies.

7.6.1 CPU MOTHERBOARD REMOVAL

Remove the 210-7608 CPU Motherboard as follows: (See Figure 7-6.)

1. Power-down the Mainframe and unplug the power cord from the wall.
2. Remove the top and front covers.
3. Lower the fan assembly.
4. Remove all CPU circuit cards. Because of inter-board cabling, remove the Cache and SBC cards together.
5. Once all cards are removed, remove the cables attached to motherboard connectors J1 and J47 through J50. (Callouts 1 and 2 on Figure 7-6.)
6. Using a ¼-inch nut-driver, remove the two nuts securing the four wires to the back of the motherboard (callout 3).
7. Using a ½-inch nut-driver, remove the nut securing the +5V supply cable to the motherboard. (At rear of Motherboard.)
8. Remove all (8) Phillips-head srews located on the outer edges of the motherboard and the Phillips-head screws located between the card slots on the motherboard (Callout 4)
9. With all screws and nuts removed, grasp the motherboard and lift it up and out of the Mainframe.

To re-install the motherboard, reverse the above procedure. Ensure that all screws and nuts are re-installed in their proper locations, and that all wires and cables are installed correctly. Ensure that no metal part of the motherboard makes contact with the Mainframe chassis (see CAUTION in paragraph 7.6). Carefully re-install all circuit cards according to the layout in Chapter 3 and ensure that all card cabling is installed correctly.

7.6.2 I/O MOTHERBOARD REMOVAL

Before removing either I/O motherboard, perform steps 1, 2, and 3 of the previous motherboard removal procedure. Remove the 210-7609 I/O Motherboards as follows: (See Figure 7-7.)

1. Remove the I/O motherboard closest to the CPU by disconnecting all cables from the IOP assemblies and removing the assemblies.
2. Once all cards are removed, disconnect the cables attached to

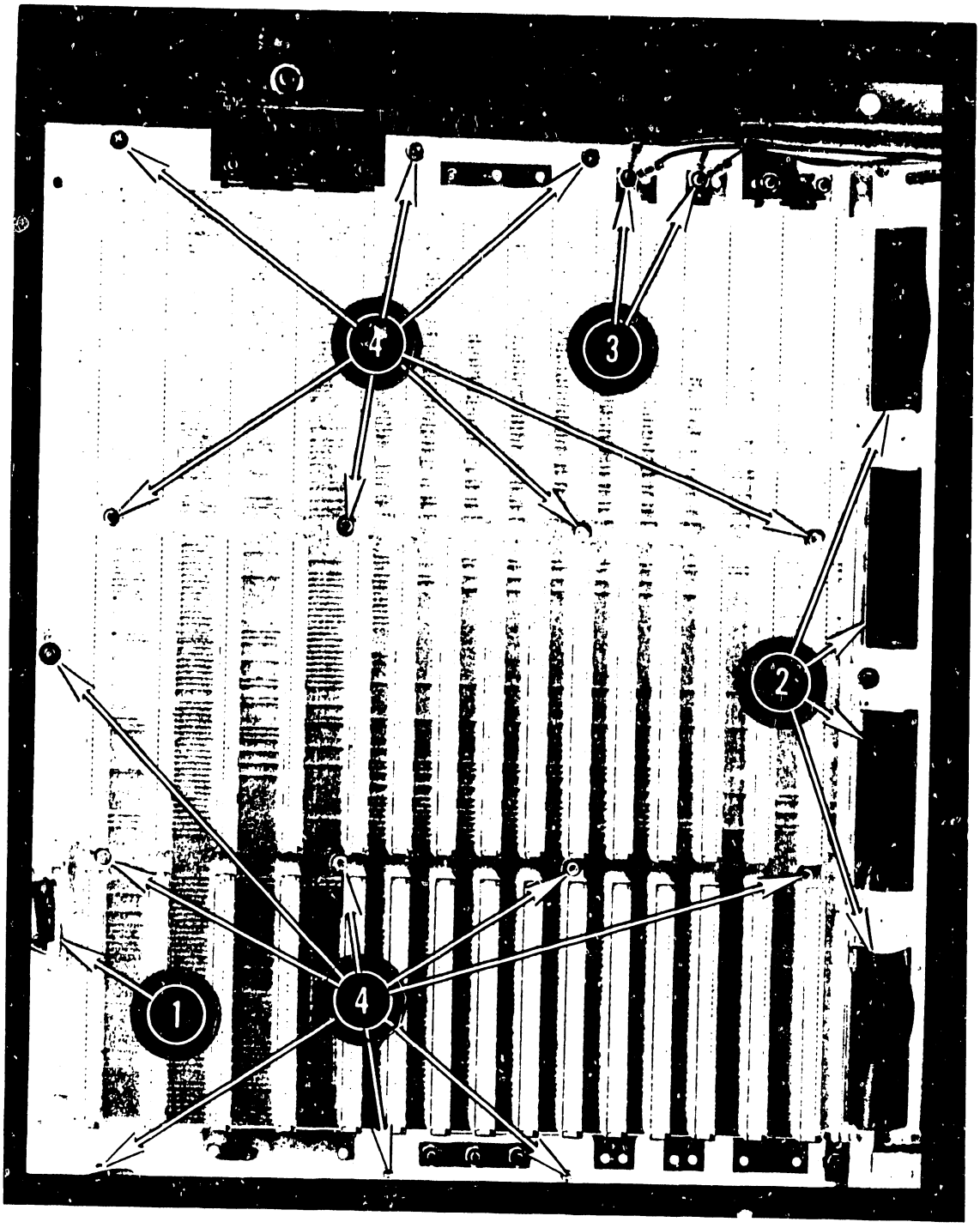


FIGURE 7-6 CP MOTHERBOARD REMOVAL

motherboard connectors J1 through J4, and J37 through J40. (Callout 1 on Figure 7-7.)

3. Using a ¼-inch nut-driver, remove the four nuts securing the seven wires to the back of the motherboard (callout 2).
4. Remove the Phillips-head srews located on the outer edges and between the card slots on the motherboard (callout 3).
5. With all screws and nuts removed, grasp the motherboard and lift it up and out of the Mainframe.
6. Remove the I/O motherboard farthest from the CPU motherboard by disconnecting all cables from and removing the IOP assemblies.
7. Once all cards are removed, remove the cables attached motherboard connectors J37 through J40 and the cable from the front panel (210-7613) attached to J5 (callouts 1 and 4).
8. Using a ¼-inch nut-driver, remove the four nuts securing wires to the back and front of the motherboard. (Callouts 5 on Figure 7-7.)
9. Remove all (8) Phillips-head srews located on the outer edges of the motherboard and the four Phillips-head screws located between card slots on the motherboard (callout 6).
10. With all screws and nuts removed, grasp the motherboard and lift it up and out of the Mainframe.

To re-install the motherboards, reverse the above procedures. Ensure that all screws and nuts are re-installed in their proper locations, and that all wires and cables are installed correctly. Ensure that no metal part of the motherboard makes contact with the Mainframe chassis (see CAUTION in paragraph 7.6). Carefully re-install all circuit cards according to the layout in Chapter 3 and ensure that all assembly cabling is installed correctly.

7.7 FRONT PANEL REMOVAL

The 210-7613 Front Panel board in the VS-100 is attached to the hinged panel of the front cover by four clips. Remove the Front Panel as follows: (See Figures 7-8, 7-9, and 7-10.)

1. Power-down the Mainframe.
2. Open the hinged panel on the front cover and remove the board from it by gently spreading the clips that secure the board to the panel.

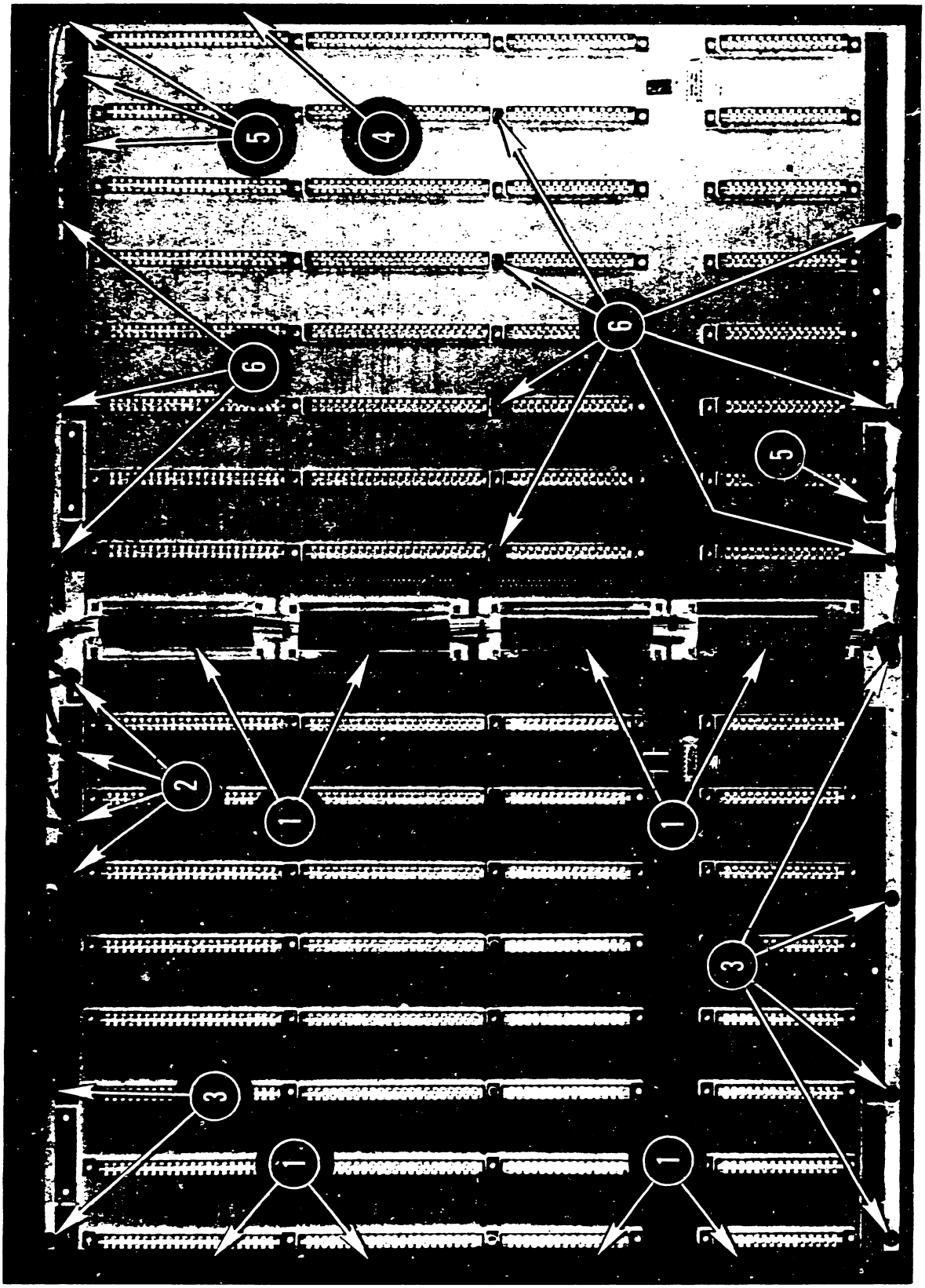


FIGURE 7-7 I/O MOTHERBOARD REMOVAL

3. Remove the cables from connectors J1, J2, and J3 on the Front Panel.
4. Unplug the Molex connector from J4.
5. Hang the Front Panel on the hooks attached to the fan located just above the Front Panel. (See Figure 7-9.)
6. Remove the top and front covers from the Mainframe. (Refer to Paragraphs 7.2 and 7.3.)
7. Remove the two Phillips-head screws securing the control buttons to the top right corner of the chassis.
8. Remove the Front Panel and attached control buttons from the chassis.

Re-install the Front Panel by reversing the above procedures.

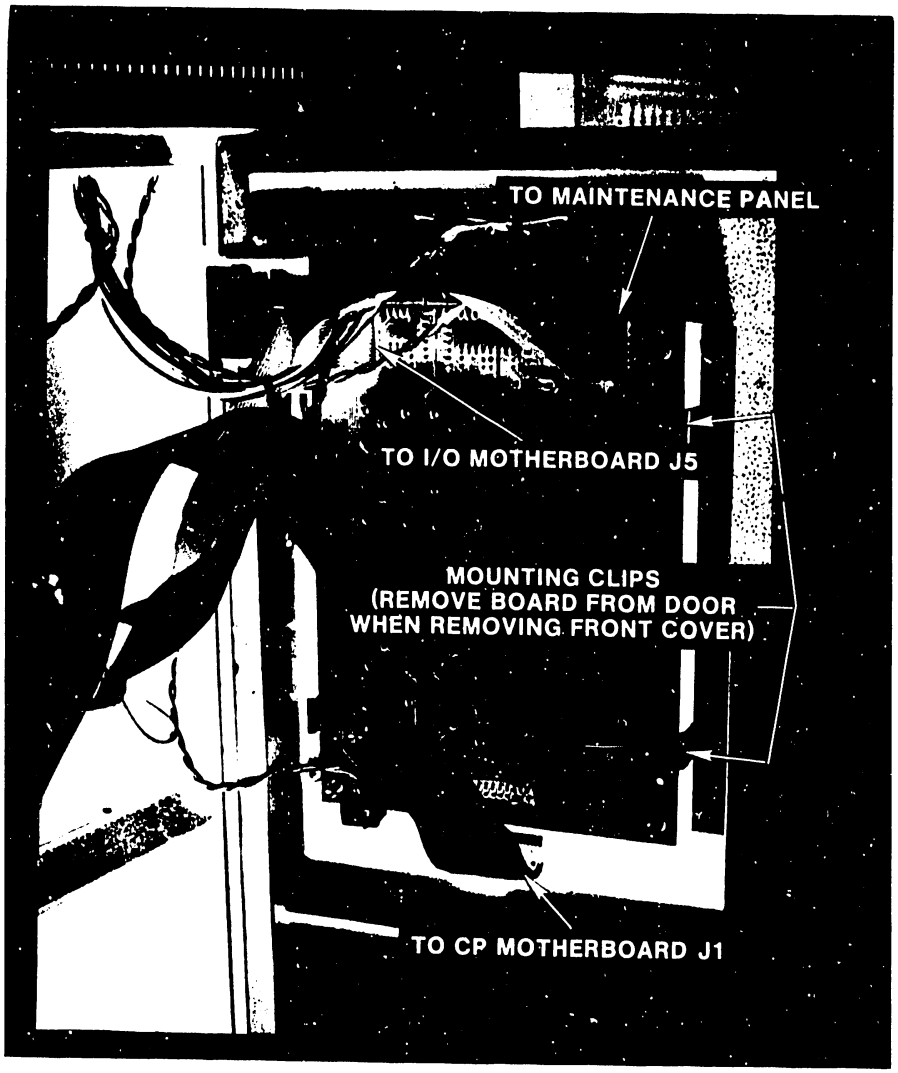


FIGURE 7-8 FRONT PANEL REMOVAL

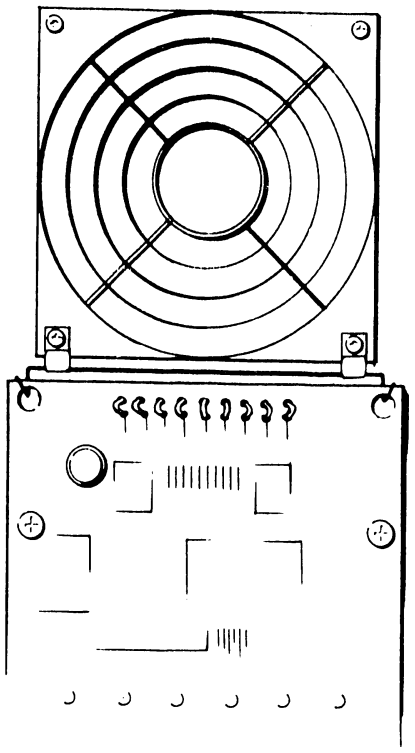


FIGURE 7-9 FRONT PANEL MOUNTED ON CHASSIS

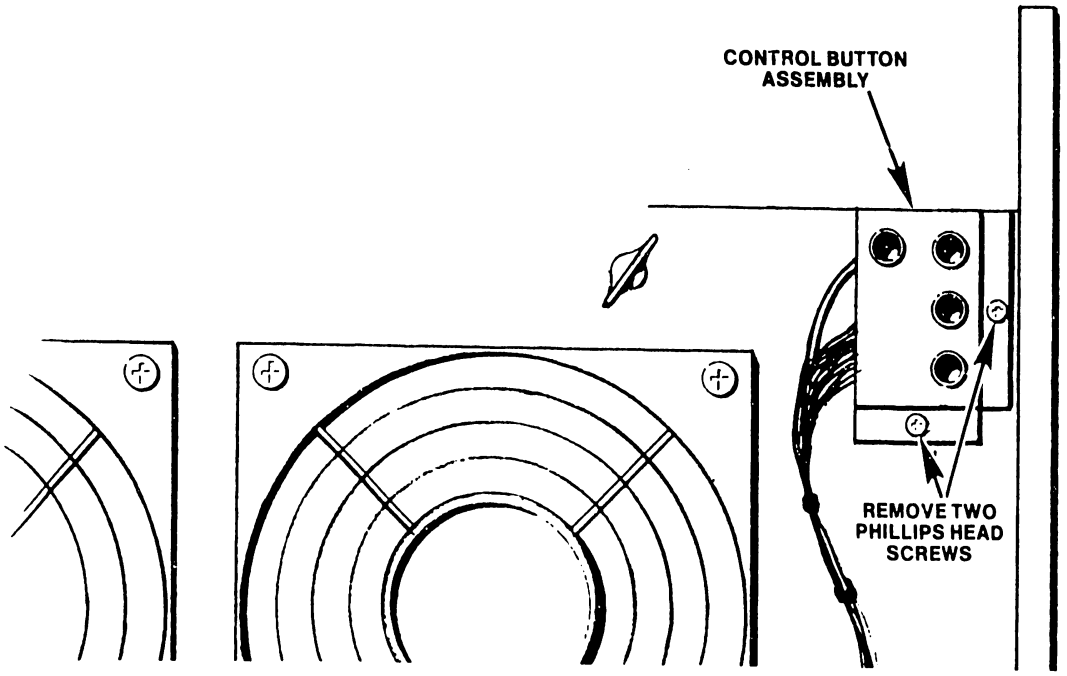


FIGURE 7-10 CONTROL BUTTON ASSEMBLY REMOVAL

7.8 MAINTENANCE PANEL REMOVAL

Remove the 210-7614 Maintenance Panel as follows: (See Figure 7-11.)

1. Power-down the Mainframe.
2. Disconnect the cables from J2 through J6, and J8 and J9.
3. Unplug the Molex connector from J1.
4. Remove the Phillips-head screws from each corner of the Maintenance Panel and lift the board away from the chassis.

Re-install the Maintenance Panel by reversing the above procedures.

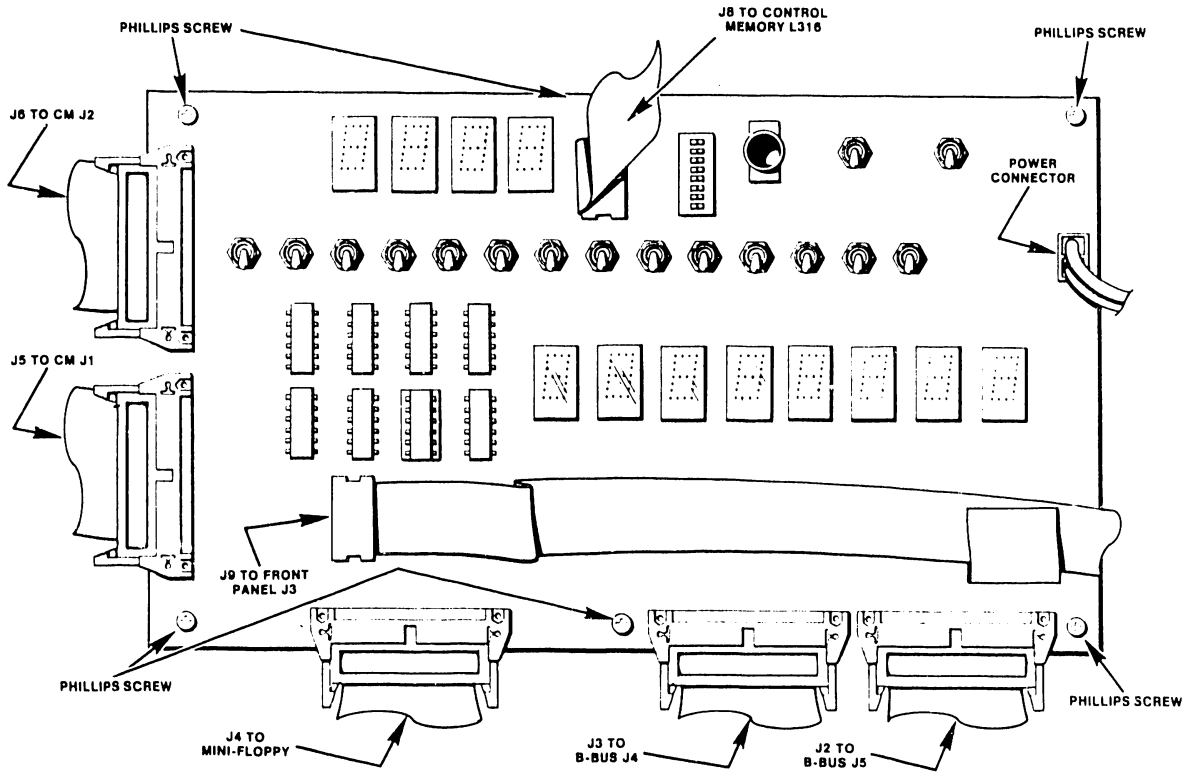


FIGURE 7-11 MAINTENANCE PANEL REMOVAL

7.9 MINI-FLOPPY DRIVE REMOVAL

The minifloppy drive attaches to the Mainframe chassis by means of two 3-inch bolts that pass through the horizontal cross-brace extending across the front of the Mainframe. Remove the drive as follows: (See Figure 7-12.)

1. Power-down the Mainframe and remove the top and front covers if necessary. (Refer to Paragraphs 7.2 and 7.3.)
2. Disconnect the power and maintenance panel plugs from the mini-floppy controller board, located under the drive unit.
3. Disconnect the ribbon cable from the right side of the controller board.
4. Carefully remove the two screws that secure the drive to the Mainframe. Ensure that the drive does not drop out of position damaging either itself or a nearby power supply.
5. Carefully remove the drive from the Mainframe, avoiding contact between the drive and adjacent equipment.

Replace or re-install the drive by reversing the above procedure.

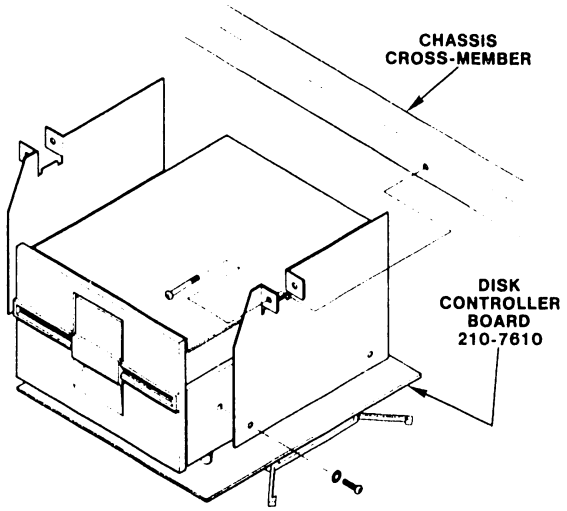


FIGURE 7-12 MINI-FLOPPY DRIVE REMOVAL

7.10 POWER SUPPLY REMOVAL

Before the power supplies can be removed, the top and front covers of the VS-100 Mainframe must be removed (refer to Paragraphs 7.2 and 7.3). On EARLY versions of the VS-100, the power supply tray on which the power supplies are mounted must be pulled from beneath the Motherboards. Remove the tray as follows: (See Figure 7-13, callouts 1, 2, and 3.)

CAUTION

Because of the high operating voltages used in the Power Supplies, POWER-DOWN the Mainframe and REMOVE the plug from the wall receptacle before performing the following removal/replacement procedures.

---

1. Using a 7/16-inch nut-driver, disconnect the ground bar on the switching power supplies from the Mainframe chassis (callout 1).
2. Disconnect the motherboard +5V supply cables from the switching supplies (callouts 2 and 3).
3. Firmly grasp the power supply tray under the front lip with both hands.
4. Pull the tray as far forward as possible, using a firm steady pressure.

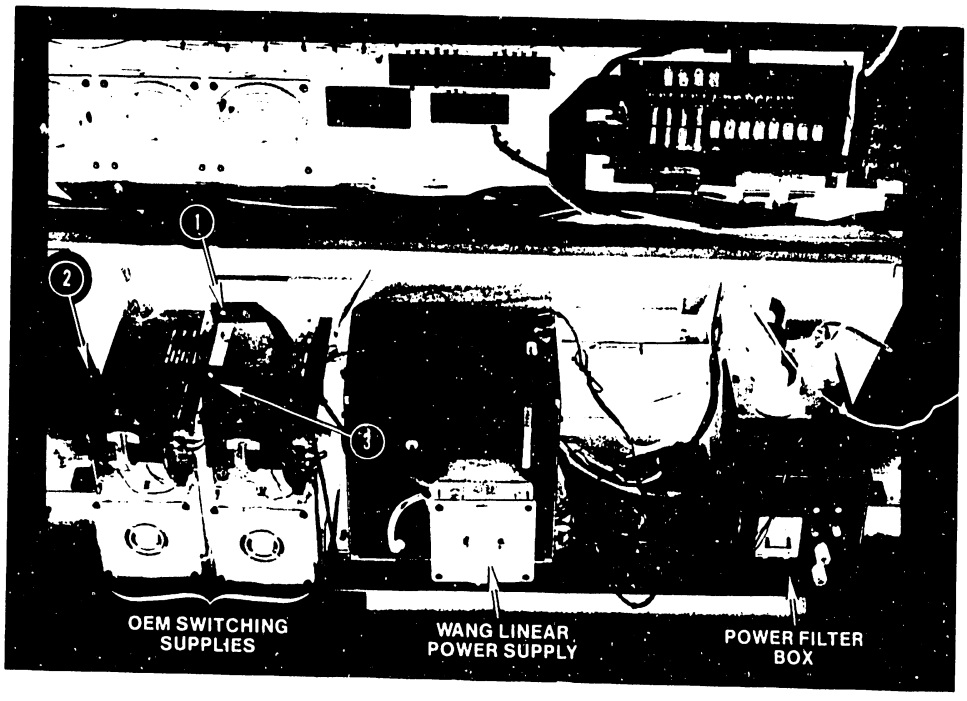


FIGURE 7-13 WITHDRAWING THE POWER SUPPLY TRAY

7.10.1 REMOVING THE WANG LINEAR POWER SUPPLY

The Wang Linear Supply is located to the immediate left of the mini-floppy drive. The voltage test points, indicator LEDs, and adjustment pots are located on the front of this unit. Remove the linear supply as follows: (See Figure 7-14.)

1. Remove the Phillips-head screw securing the linear-supply ground strap to the switching-supply ground bar. (See Figure 7-13.)
2. Remove the two Phillips-head screws securing the bottom of the power supply to the tray.
3. Two tabs on the rear of the power supply fit into two slots located on the tray. Carefully pull the supply forward out of the slots.
4. Disconnect the Molex connectors attaching the linear supply to the power box and the switching supplies.
5. Lift the supply up and away from the Mainframe.

To install the linear supply, reverse the above procedure. Ensure that the tabs at the rear of the supply engage the slots on the tray when installing the supply, and that all Molex connectors are re-attached.

7.10.2 REMOVING THE OEM POWER SUPPLIES

The vendor-supplied (OEM) +5VDC Switching supplies are located to the immediate left of the linear supply. Remove as follows: (See Figure 7-15.)

1. Determine which supply is to be removed and disconnect that supply from the ground bar.
2. If both supplies are to be removed together, disconnect the chassis ground strap from the ground bar.
3. Remove the Phillips-head screws securing the bottom of the power supply to the tray.
4. Two tabs on the rear of each power supplies fit into slots located on the tray. Carefully pull the supply out of these slots.
5. Disconnect the Molex connector attaching the switching supply to the linear supply.

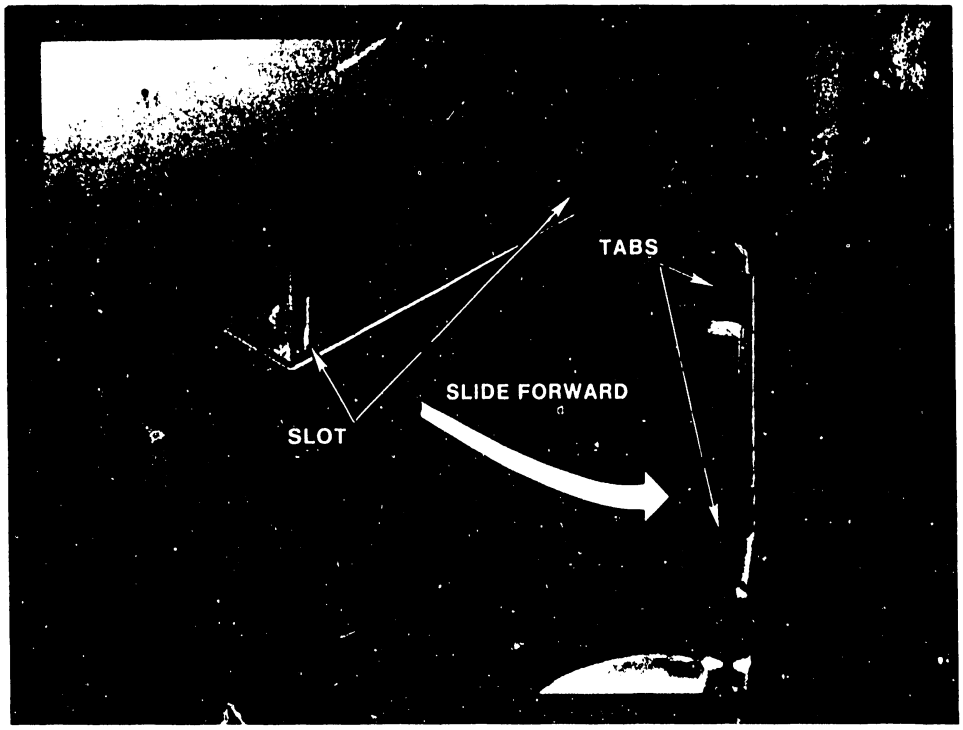


FIGURE 7-14 REMOVING THE WANG LINEAR POWER SUPPLY

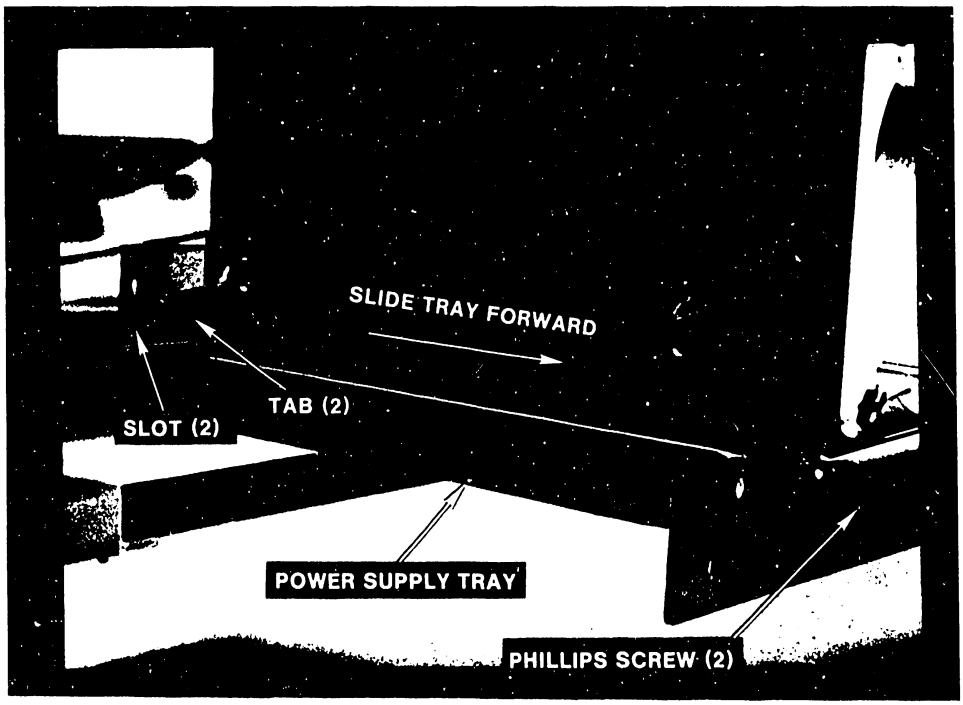


FIGURE 7-15 REMOVING THE OEM POWER SUPPLIES

6. Lift the supply up and away from the Mainframe.
7. If both supplies were removed as a single unit, remove an individual supply by detaching it from the ground bar. This bar has been designed for use with power supplies of various dimensions. The arms securing the supply to the bar are adjustable allowing the use of power supplies from several different vendors. (See Figure 7-16.)

To install the switching supplies, reverse the above procedure. Ensure that the tabs at the rear of the supplies engage the slots on the tray when installing the supply and that the Molex connectors are re-attached. Also check that the chassis ground-strap is re-attached to the switching-supply ground bar, if it has been previously removed.

NOTE

Each +5V power supply has its own fuse, located behind the muffin fan at the front of each supply (see Figure 7-16). If a +5V supply is not functioning, inspect this fuse first before removing the supply.

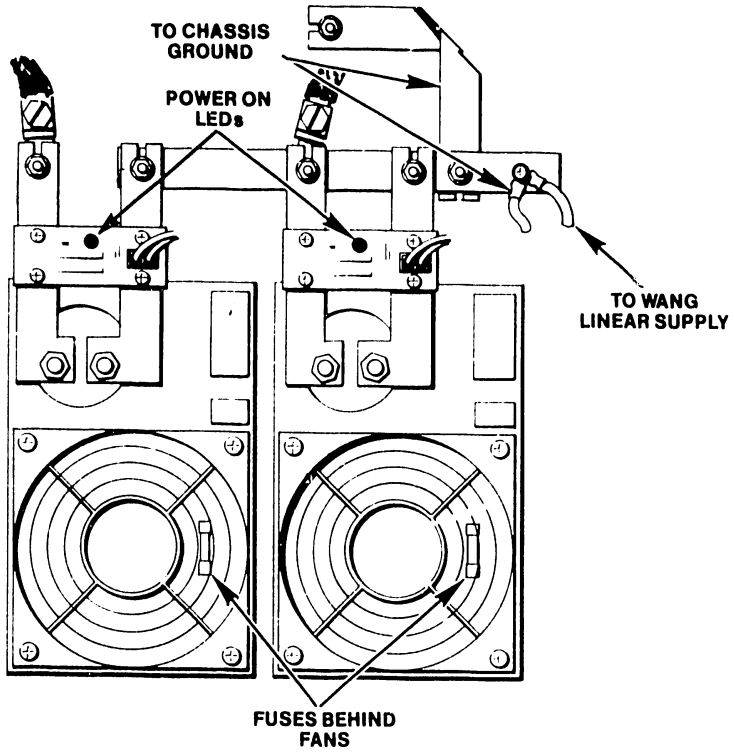


FIGURE 7-16 LINEAR SUPPLY GROUND BAR

7.11 REMOVING THE POWER BOX

The power box is located to the right of the mini-diskette drive. It connects the outside line voltage to the VS-100 Mainframe. Internal to the power box are filters used to smooth out transient voltage spikes and line current sureges. Remove the power box as follows: (See Figure 7-17.)

CAUTION

Because of the high operating voltages passing through the power box, power-down the Mainframe and remove the plug from the wall receptacle before performing the following removal/replacement procedures.

---

1. Remove the top and f ont covers.
2. Slide the power supply tray out from under the motherboards.
3. Unplug the Molex connector attaching the power box to the linear supply.
4. Disconnect the two fan plugs, the two switching-supply plugs, and the linear supply plug from the top of the power box.
5. Remove the two Phillips-head screws securing the box to the power supply tray.
6. Two tabs on the rear of the power box fit into two slots located on the tray. Carefully pull the supply forward out of the slots.
7. Disconnect the three wires attached to the line cord at the rear of the Mainframe chassis. Note the color code for these wires.
8. Lift the power box up and away from the Mainframe.

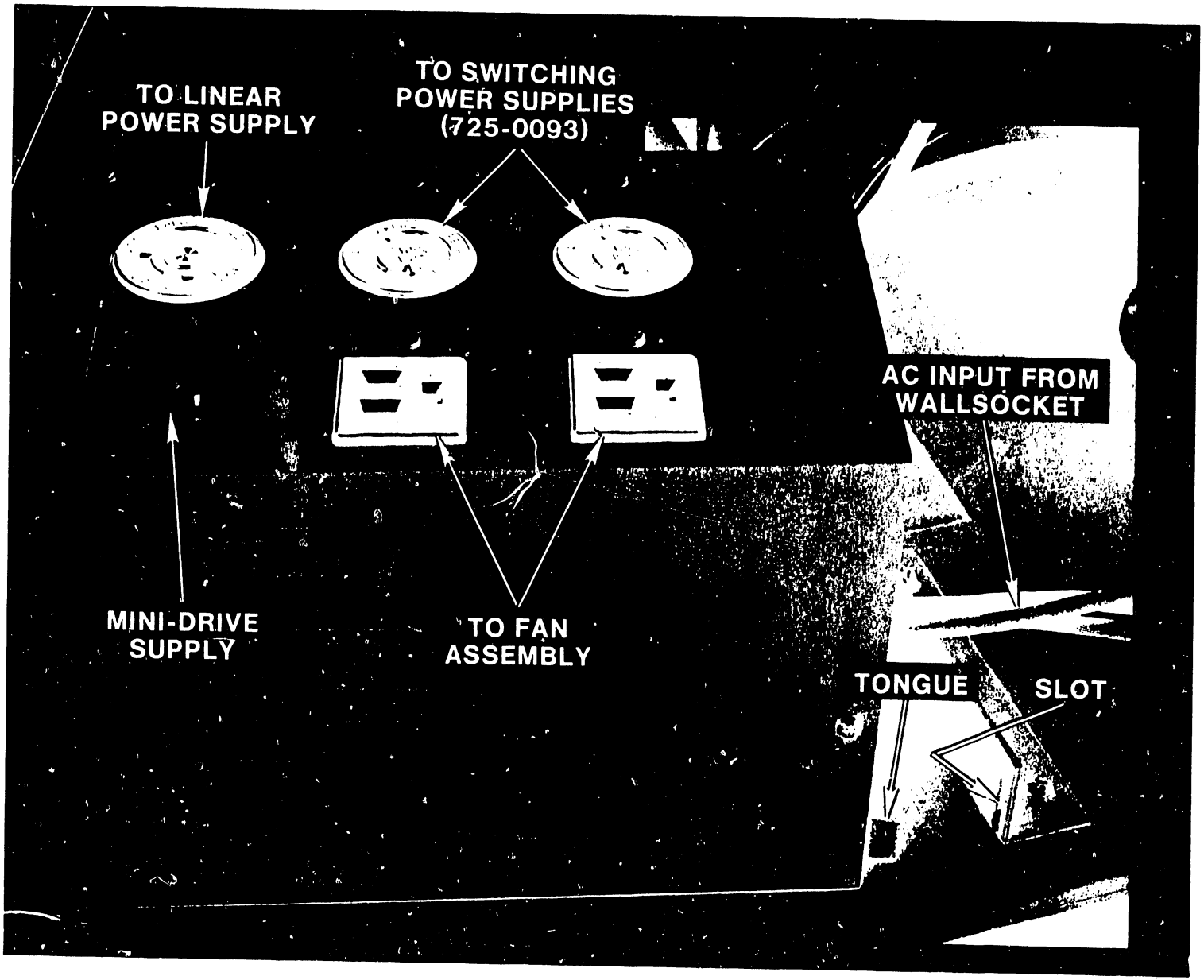


FIGURE 7-17 POWER BOX REMOVAL

7.12 VERY LARGE DISK ADAPTER BOARD

7.12.1 INTRODUCTION

This section describes the device switch settings for the 22V78/22V88 Very Large Disk Adapter Board. The 22V78/22V88 Very Large Disk Device Adapter Board is an addition to the existing 7114 SMD Device Adapter and the 8214 Dual Port SMD Device Adapter. It will control the single and dual port SMD type drives including 675 Meg drives. Four versions of the Device Adapter will be offered as listed below:

a.) A 1 Port Disk Controller
b.) A 2 Port Disk Controller
c.) A 3 Port Disk Controller
d.) A 4 Port Disk Controller

A hardwired 2 bit code to define the version will be readable by the IOP. Each version will not be upgradable to support more drives.

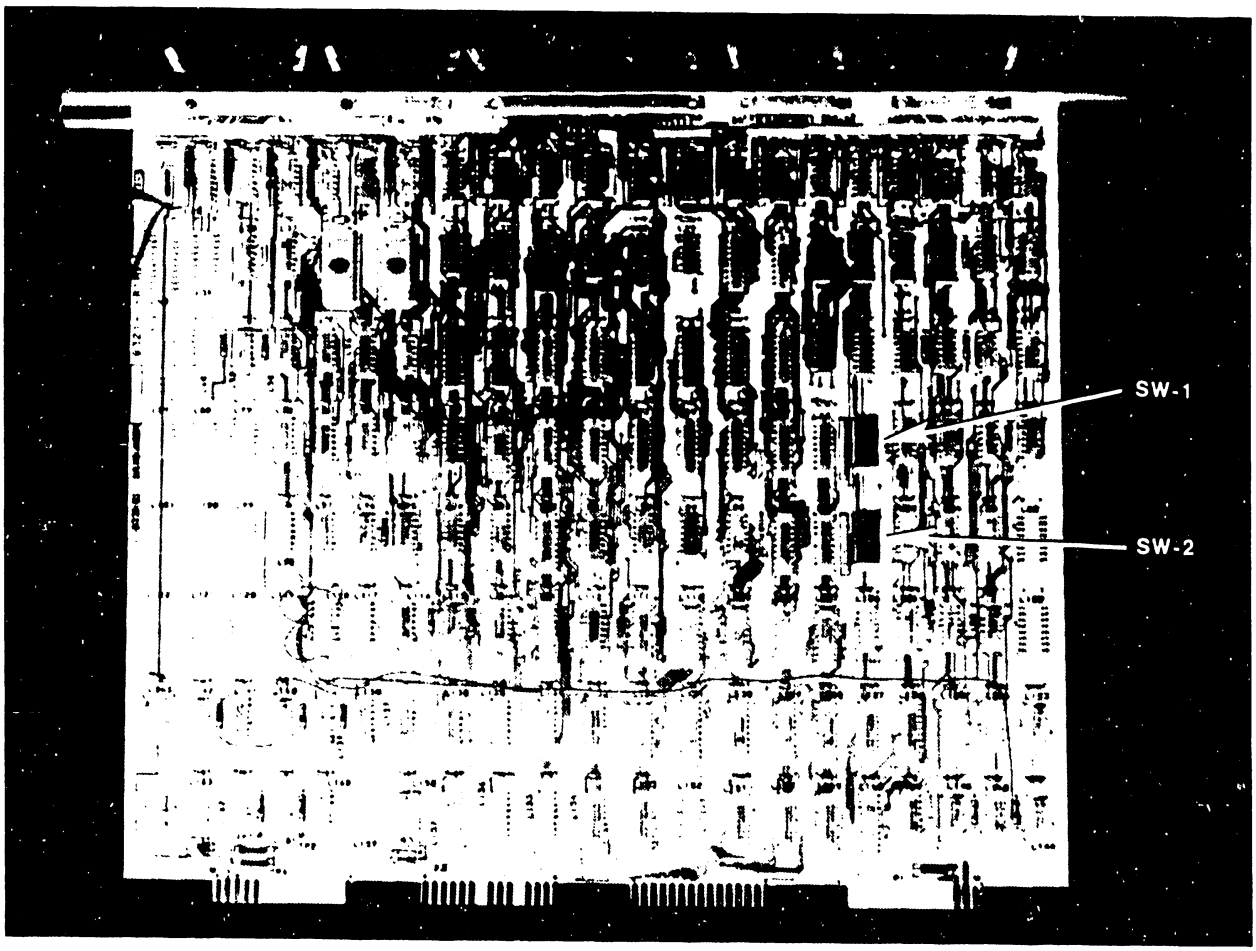


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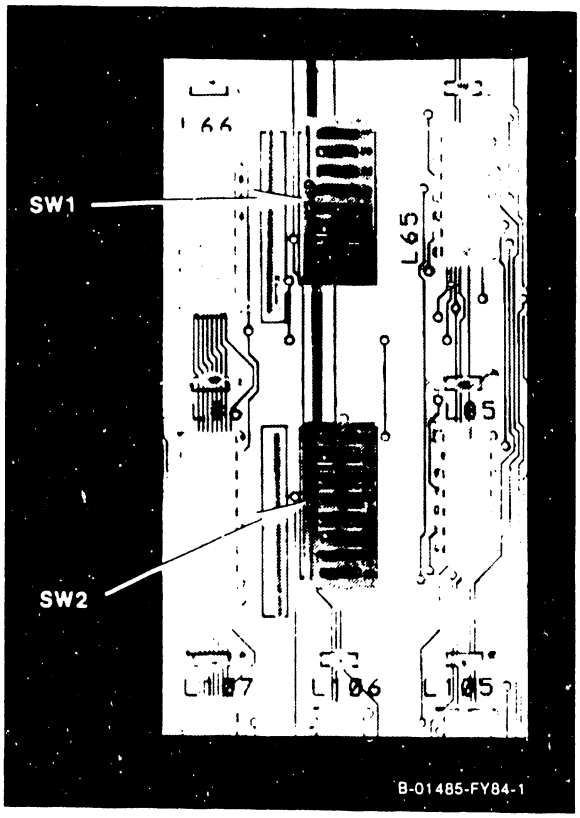
FIGURE 7-18 210-8321 SMD/CMD DISK DEVICE ADAPTER

7.12.2 22V78/22V88 SMD/CMD DA SWITCH SETTINGS

The two 8-position disk device type switches, SW1 and SW2, define the type of drive connected to the SMD/CMD Device Adapter ports 0-3. Set the switches for the type of drive(s) to be connected to the system, referring to Figures 7-18 and 7-19, and Table 7A. On the #210-8318 (1-port) and #210-8319 (2-port) adapters, SW1 may not be installed. The switch location may be hard-wired to indicate that ports number 2 and 3 cannot be used.



	SW1	OPEN / CLOSED
DRIVE 3	1	BIT 3
	2	BIT 2
	3	BIT 1
	4	BIT 0
DRIVE 2	5	BIT 3
	6	BIT 2
	7	BIT 1
	8	BIT 0

	SW2	OPEN / CLOSED
DRIVE 1	1	BIT 3
	2	BIT 2
	3	BIT 1
	4	BIT 0
DRIVE 0	5	BIT 3
	6	BIT 2
	7	BIT 1
	8	BIT 0

FIGURE 7-19 210-8321 SMD/CMD DISK DEVICE ADAPTER.
DISK DEVICE TYPE SWITCH SETTINGS.

DRIVE TYPE	BIT 3	BIT 2	BIT 1	BIT 0
75 MEG SMD	OPEN	OPEN	OPEN	OPEN
288 MEG SMD	OPEN	OPEN	OPEN	CLOSED
30 MEG CMD	OPEN	CLOSED	OPEN	OPEN
60 MEG CMD	OPEN	CLOSED	OPEN	CLOSED
90 MEG CMD	OPEN	CLOSED	CLOSED	OPEN
620 MEG SMD	CLOSED	OPEN	CLOSED	CLOSED
NO DRIVE	CLOSED	CLOSED	CLOSED	CLOSED

TABLE 7A SMD/CMD DISK DRIVE TYPES.

7.12.3 PART NUMBERS

This section contains a breakdown of the various part numbers used in ordering a Very Large Disk IOP for either a VS80 or VS100.

Part Number	Description
212 - 3042	1 Port 22V78 Very Large Disk IOP for VS80
212 - 3043	2 Port 22V78 Very Large Disk IOP for VS80
212 - 3044	3 Port 22V78 Very Large Disk IOP for VS80
212 - 3045	4 Port 22V78 Very Large Disk IOP for VS80
212 - 3050	1 Port 22V88 Very Large Disk IOP for VS100
212 - 3049	2 Port 22V88 Very Large Disk IOP for VS100
212 - 3048	3 Port 22V88 Very Large Disk IOP for VS100
212 - 3047	4 Port 22V88 Very Large Disk IOP for VS100

CHAPTER 8 DIAG-NOSTICS

CHAPTER 8
DIAGNOSTICS

8.1 GENERAL

Two types of diagnostics are available to the VS-100: inner-level CP microcode diagnostics, and outer-level memory and peripheral diagnostics. With these diagnostics, the field-level CE is able to locate and repair most problems that occur in the System. All available diagnostics will be run prior to customer turnover as a check for System integrity. All currently available VS 60/80 on-line diagnostics will be available on the VS-100.

Corporate Publications is in the process of documenting all available diagnostic and service programs relating to the VS family of data processors. This documentation will contain procedures for running and interpreting all available diagnostics. The documents are tentatively titled "VS SERVICE PROGRAM GUIDE" and "VS CENTRAL PROCESSOR MICRO-DIAGNOSTIC TESTS".

8.2 VS-100 MICROCODE DIAGNOSTICS

An important diagnostic tool for testing the VS-100 CPU is a series of microcode diagnostics available on mini-diskettes. Used in conjunction with the Maintenance Panel, these diagnostics enable the CE to routine all major CPU functions. Loaded by means of the mini-floppy drive built into the Mainframe, the microcode diagnostics consist of five different testing levels. The five levels and the CPU functions tested by each are as follows:

1. LEVEL 1--Tests op-codes needed for higher test levels.

Operation/Component Tested	Test #
Branch Unconditional	0010
Instruction Counter	1010
Branch True/False Status Opcodes	2010
Subroutine Stack Data Integrity	3010

1. LEVEL 1 (cont'd)

Addressability	4010
A/B Bus - Register	
Data Integrity	4110
Register Select	4120

2. LEVEL 2--Tests additional op-code levels.

Operation/Component Tested	Test #
Visual Verification	
Move, Shift Add/Sub	5000

3. LEVEL 3--Tests process and Control Memory (CM) op-codes. From this point on all diagnostics are supported by the MONITOR program.

Operation/Component Tested	Test #
R/W CM (Upper)	6010
CM Parity Trap	
R/W CM (Lower)	7010
A/B Bus - Register	
Data Integrity	8010
Register Select	8110
Data Stack Data/Address	9010
Translation-RAM	9110

4. LEVEL 4--Completes process and op-code tests.

Operation/Component Tested	Test #
Addition	A010
Overflow	
Subtraction	A110
Logicals	
AND, OR, XOR	B010
Move (MV, MC, MINC	
MDEC, MNUM)	B110
Shift (SHL/SHR/Zero/One/4)	C010

4. LEVEL 4 (cont'd)

Decimal Add/Subtract	C110
CCSET, STAT	D010
Compare	
Arithmetic/Logical	D030
Add High/Low	D110
Current Halfword	
Counter/Comparator	
ECC/ECR, BTL, INIT, CLOCK	

5. LEVEL 5--Tests outer level of CPU and Control Mode.

Operation/Component Tested	Test #
Memory Opcodes	
Ripple Opcodes	AA10
MAR0/MAR1/MAR2	AA20
Read/Write Opcodes	AA30
Doubleword Write	AA50
BNM (Macro-Stream)	AA70
Main Memory	
Invalid Address Trap	DD10
ECC Bank/Chip Addressing	DD20
ECC Moving Inversions	DD30
ECC Refresh	DD40
Data Memory (DM) Data Bus/	
Main Memory Parity Trap	DD50
DM Bank/Chip Addressing	DD60
DM Moving Inversions	DD70
DM Refresh	DD80
Cache Memory	
Data/Tag Field Integrity	
Hit/Miss Logic	
CP Write Cache Update	
BA Write Cache Invalidate	
Parity Error Detection	CC10

5. LEVEL 5--(cont'd)

System Bus Controller	
Extent Bit	BB10
Main Memory (MM) Bus	BB20
External Condition Register (ECR) Read/Write (RECR/WECR)	BB30
ECC (MM Parity)	BB40
Bus Transaction Log	BB50
Error Correction Code Data Register	
INIT - SWE Instruction	BB60
Bus Adapter	
Status	TEST 1
IAR/CAR Data Integrity	TEST 2
Write 8 Memory Operations	TEST 3
Write 16 Memory Operations	TEST 4
Write 32 Memory Operations	TEST 5
Write 64 Memory Operations	TEST 6
Read Deblocking	TEST 7
CAR Address Integrity	TEST 8
IAR Address Integrity	TEST 9
Control Mode (Alert)	N/A

8.3 THE MAINTENANCE PANEL

The Maintenance Panel is used by the CE in conjunction with the microcode diagnostics for troubleshooting the VS-100 Mainframe. The Maintenance Panel consists of a 16-bit (4 HEX LEDs) IC register display, 14 address selection switches, an 8-position DIP switch, three control switches, and a 32-bit (8 HEX LEDs) B-Bus display.

When a fault (or successful completion) is detected by the microcode diagnostics, the results are displayed as a HEX 'code' on the 16-bit IC Register display. This code is listed in the "VS CENTRAL PROCESSOR MICRO-DIAGNOSTIC TESTS" manual, which describes the test that failed, the function it was performing, and the most likely reason for failure.

Once the CE has identified the failing card and recorded the error code, the card is sent to a Repair Depot. At the depot, repair personnel will run the same diagnostics the CE ran to verify the observations of the CE. This duplicating of trouble conditions results in fast turn-around time in the ultimate repair of the board.

8.3.1 PERFORMING MICROCODE DIAGNOSTICS

Load the microcode diagnostics into Control Memory as follows:

1. Insert the first microcode diagnostic diskette (WLI # not available) into the mini-floppy drive and press the silver BT (BOOT) button on the Control Panel (See Figure 3-18). This causes the CP to load the microcode into Control Memory.
2. Wait for the READY LED on the Front Panel to light.

NOTE

If LED flashes instead of remaining in the steady ON state, reseat diskette. If LED again begins to flash, insert another diagnostic diskette. If this does not correct the problem, Control Memory or the drive itself may be defective.

3. After loading the microcode, set all switches on the maintenance panel 8-position DIP switch to the ON position and depress the INITIALIZE button. (Refer to the Switch Configuration Table.) The program will now halt at Location 0000. There are some exceptions to this rule, such as TEST5000 (Visual Verification test) which stops at Location 0020.
4. Place the RUN/STEP switch to RUN mode and press the STEP button. This causes the diagnostic program to begin executing.
5. Refer to the next sub-paragraph for an explanation of the 8-position maintenance panel DIP switch. This switch is used in conjunction with the micro-diagnostics which support the MONITOR program. At this time, these diagnostics reside in Test Level 3 and above. Also refer to the VS CENTRAL PROCESSOR MICRO-DIAGNOSTIC TESTS manual for interpretations of any trouble numbers that occur.

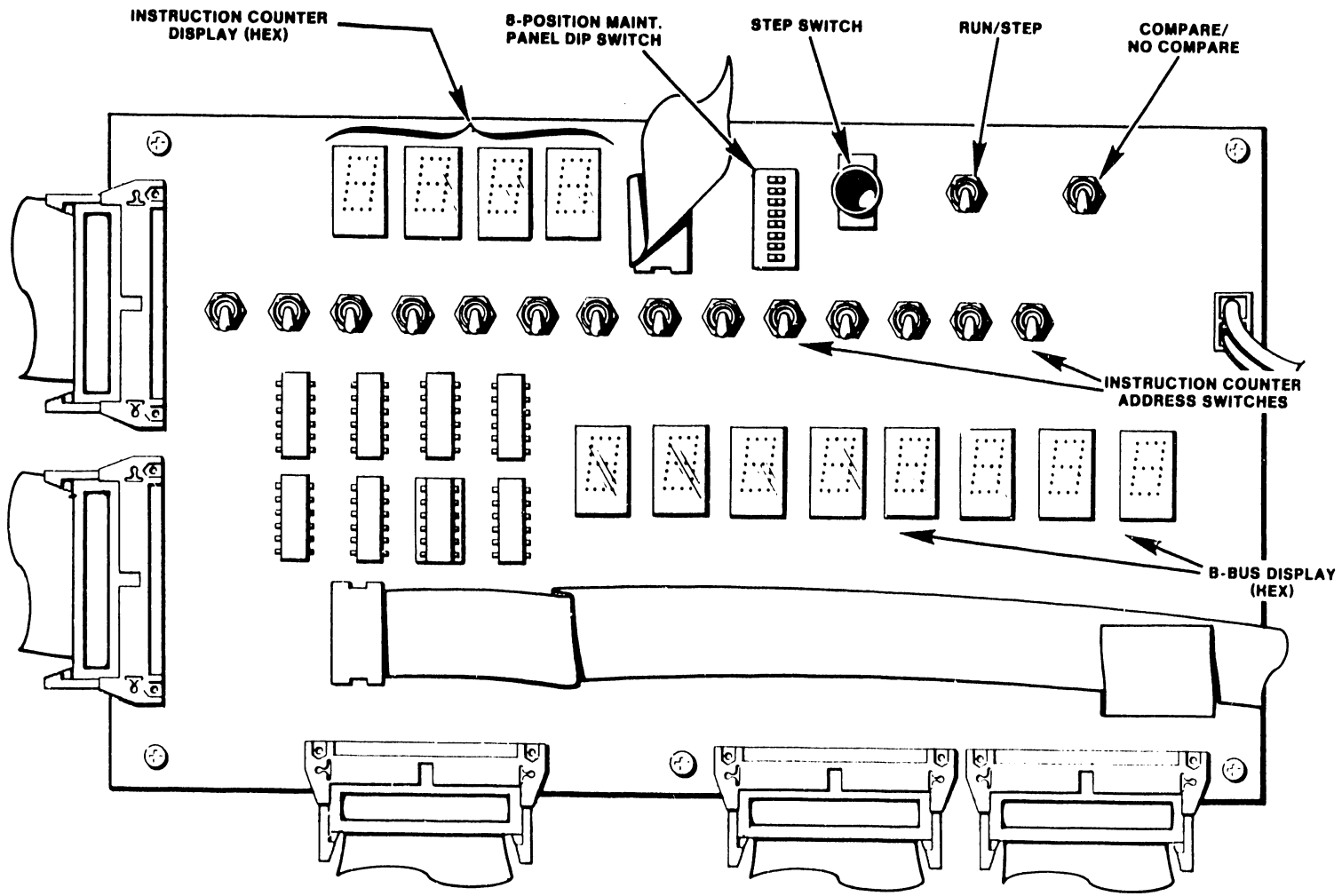


FIGURE 8-1 THE MAINTENANCE PANEL (210-7614)

8.3.2 MONITOR DIAGNOSTIC SWITCH

The following is a brief description of the switch settings for the MONITOR Diagnostic Switch located on the Maintenance Panel. (OFF is ACTIVE.)

NOTE

This switch is used with Level 3 and above micro-diagnostics only.

1. Switch 1 OFF--HALT ON ERROR--test halts and ERROR CODE appears on B-Bus display if an error occurs. Consult the micro-diagnostic test manual and the program listings for error-code definitions.
2. Switch 2 OFF--DATA DISPLAY--displays 'expected' and 'received' results of operations whenever an error has been detected. Used with HALT ON ERROR function to display contents of the File Register specified by switches 5 through 8.
3. Switch 3 OFF--LOOP ON ERROR--prevents test from halting when an error occurs. The LOOP ON ERROR function puts the system in a very tight loop utilizing only those instructions necessary to generate the fault condition. Switch 1 must be ON. Because LOOP ON ERROR can be used with an oscilloscope, this function is useful when troubleshooting to chip level on a particular circuit card.
4. Switch 4 OFF--LOOP ON TEST--Used to troubleshoot an intermittent error. Causes the specified subtest to cycle repeatedly from beginning to end until the error re-occurs. Setting switch 4 ON causes the routine to proceed to next subtest. LOOP ON TEST can be used in conjunction with HALT ON ERROR (SW1) or LOOP ON ERROR (SW3).
5. Switch 5 OFF--SLOW CLOCK--For diagnostic purposes only, provides a means of proving marginal System errors. To use this function, CPU must be halted at CM location 0000.
6. Switch 6 OFF--FAST CLOCK--For diagnostic purposes only, provides a means of proving marginal System errors. To use this function, CPU must be halted at CM location 0000.
7. Switches 5 and 6 ON--NORMAL CLOCK--Returns clock to normal operating cycle. To use this function, CPU must be halted at CM location 0000.
8. Switch 7 OFF--EXECUTE SINGLE TEST--Run test once and then halt. After halt, B-bus will display number of test that was run. Monitor Program will ignore other switches when this switch is OFF.

9. SWITCH 8 OFF--LOOP ON DISKETTE--Run diagnostic routines stored on diskette repeatedly. To stop looping, set Switch 8 ON. Monitor Program will ignore other switches when this switch is OFF.
10. Switches 5, 6, 7, 8--FILE REGISTER SELECTION--To display the contents of a particular File Register, switches 5 through 8 must be set to the number of the specific register. The contents of the register are then diplayed on the B-Bus LEDs. The display represents the 'expected' data from the execution of a specific opcode. To use this function, switches 1 and 2 must be OFF. Refer to Table 8A for File Register contents.

    EXAMPLES: Switches 1, 2, 7, 8 OFF (C3) displays contents of File Reg 3.
    Switches 1, 2, 6 OFF (C4) displays contents of File Reg 4.

The KNOWN GOOD HALT for all tests is location 1FFF. Other halt locations not documented as valid halts indicate a documented error condition. Note that the MONITOR Program resides in all LEVEL 3 and higher tests.

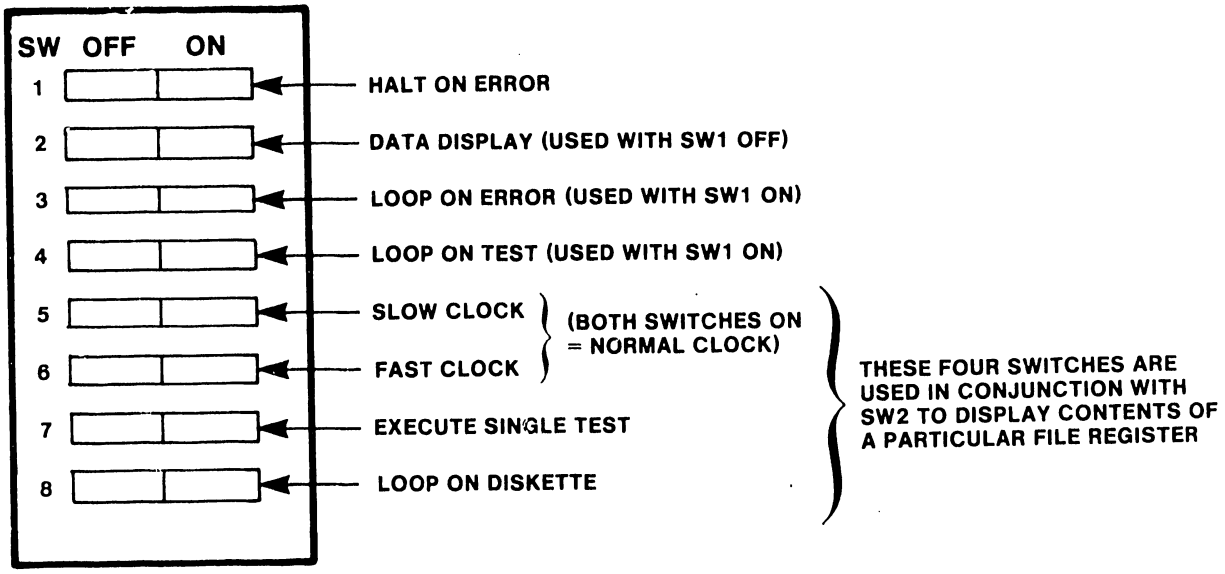


FIGURE 8-2 8-POSITION MONITOR DIAGNOSTIC SWITCH

Even though Levels 1 and 2 of the microcode diagnostics are not supported by the MONITOR Program, all error halts are documented in the listings and manuals. Levels 3 and 4 are supported by the MONITOR Program. All error codes are fully documented in the listings and manuals, providing the expected data for the detected error condition. Level 5 is also supported by the MONITOR Program, except in situations where the system is unable to recover from an error condition caused by the hardware failing to respond to the CPU.

TABLE 8A FILE REGISTER CONTENTS

FILE REGISTER	CONTENTS
FR00	TEST NUMBER
FR01	ERROR CODE
FR02	EXPECTED DATA
FR03	RECEIVED DATA
FR04 through FR11	ERROR DATA
FR12 FR13 FR14	SAVE AREA FOR WK1, WK2, AND MDR4
FR15 through FR31	UNUSED

8.3.3 USING THE MONITOR DIAGNOSTIC SWITCH

The following paragraphs provide a brief discussion of how the Monitor Diagnostic Switch is used in actual practice. These paragraphs outline basic procedures. As the CE becomes more proficient in its use, the diagnostic switch can be an invaluable troubleshooting aid.

While a Level 3 or higher diagnostic test is halted at Location 0000, set switches 5 and 6 to regulate the System Clock for either SLOW, NORMAL, or FAST cycle time. (See Figure 8-2.) Depress the STEP button on the maintenance panel and the test will halt at Location 001F. Reset all switches to the ON position and place those switches that pertain to the desired Monitor function

to OFF. For example, placing switch 1 in the OFF position causes the test being run to halt if an error occurs (HALT ON ERROR) during test execution.

Should an error occur while using the HALT ON ERROR function, the test will halt and an ERROR CODE will appear on the B-Bus display. Consult the program listings for an explanation of the cause of the fault and what area of the CPU the trouble occurred in.

The DATA DISPLAY routine is used to display 'expected' and 'received' results of operations whenever an error has been detected. It is run in combination with the HALT ON ERROR function. Once a test has halted with an ERROR CODE present on the B-Bus LEDs, set switch 2 to the OFF position to display data. The configuration of switches 5 through 8 determine which File Register contents will be displayed on the B-Bus LEDs.

For example, switches 1, 2, 7 and 8 in the OFF position (C3) displays the contents of File Register 3 (FR3), which is the 'expected' data from the execution of a certain opcode. By leaving switches 1 and 2 OFF, resetting switches 7 and 8 ON, and setting switch 6 OFF (representing a C4 configuration) the contents of File Register 4 will be displayed. This is the 'received' data from the execution of a certain opcode.

Once an error has been detected and the test has halted, the LOOP ON ERROR function can be run. To use LOOP ON ERROR, place switch 3 in the OFF position and switch 1 to the ON position. This prevents the test from halting when an error occurs and puts the system in a very tight loop using only those instructions necessary to generate the fault condition. With this function an oscilloscope can be used to locate the problem. The LOOP ON ERROR function is useful when troubleshooting defective boards down to chip level.

If an intermittent error occurs, the LOOP ON TEST function is used. To exercise this function, place switch 4 in the OFF position. This causes the specified subtest to cycle repeatedly from beginning to end until the error re-occurs. Resetting switch 4 to the ON position causes the routine to proceed to the next subtest. The LOOP ON TEST function can be used in conjunction with the LOOP ON ERROR function or the HALT ON ERROR function for fault isolation routines.

8.4 VS-100 MEMORY AND PERIPHERAL DIAGNOSTICS

Memory and peripheral diagnostics available to the VS-100 are divided into three categories: ON-LINE, STAND-ALONE, and CONTROL MODE. The following paragraphs provide a brief description of these diagnostics. For a detailed description of the actual test procedures, refer to the "VS SERVICE PROGRAM GUIDE" manual.

8.4.1 ON-LINE DIAGNOSTICS

With ON-LINE diagnostics (located in library @DIAGS@), The CE logs-on to the System through a workstation and executes a specific test routine, which runs under control of the Operating System (while customer is running). All currently available VS 60/80 on-line test routines will be available on the VS-100. Diagnostic programs currently available for individual peripherals are as follows:

1. Tape Diagnostics:
   TPTEST42--Permits exercising of tape unit.
2. Disk Diagnostics:
   FTU--Allows CE to do most disk read, write and control functions. The CE can do most of the disk alignment procedures without removing the disk drive from the system.
3. Printer Diagnostics:
   PRTEST--Provides full character-set ripples on all 132 print positions, character broadsides, printing specific characters in specific columns, and test of spacing and format functions. Will attempt things unique to printer under test (i.e., variable pitch, loadable forms control, etc.).
4. Telecommunications Diagnostics:
   TCTEST--Tests IOP memory, TC clock generation, DMA transfers, and IOP Loop Back.
5. Workstation Diagnostics:
   WSTEST--Checks screen and I/O capabilities.
   AWSTEST--Archiving Workstation test.

6. Memory diagnostics:

   SYSMEM--On-line version of FASTMEM, tests only those areas that the OS allows it to write to. Usually failures are reported as Machine Checks (system dies). Causes significant throughput degradation. If possible, use standalone FASTMEM diagnostic for routine trouble-shooting, and SYSMEM for intermittent problems.

8.4.2 STAND-ALONE

Using the stand-alone diagnostic routines (located in library @DIAGSA@), the CE creates a 'mini-operating system' with a menu display of all currently available stand-alone test routines. The CE then selects and executes the desired test. The customer cannot access the System while these tests are being performed. Currently available diagnostics are as follows:

1. Stand-Alone Boot Loader--Displays diagnostic menu on Workstation 0. @SYS000@ first loads the microcode file @MC2246S into the WS, then displays the diagnostic menu.
2. Memory Diagnostics:

   FASTMEM--Checks Main Memory data cells, ECC cells, address errors, pattern sensitivity, and address-to-data conflicts. Displays failing chip locations.
3. Disk Diagnostics:

   INITDISK--Provides same functions as DISKINIT (Initialize, Verify, Relabel, Reformat) but in off-line mode.

   FTU--Allows the exercising of disk units still connected to the system. Permits verifying, reading and writing, initializing, positioning heads, and alternate seeks.

   VERIFY--Will be replaced by INITDISK. Verifies that a disk can be read. Lists errors by address.
4. System Diagnostics:

   SYSTEST--Identifies and tests all devices, and logs error counts. Use at installation or when exercising multiple I/O operations.
5. Other Diagnostics:

   COPY--Performs the same functions as the On-line version of the COPY program.

GENLIST--Will identify units to build a sample CONFIG file relating to actual system configuration, which should require little modification to permit a SYSGEN.

8.4.3 CONTROL MODE

Control Mode is a CPU state where normal programming activities are suspended and certain other facilities (mainly diagnostic and initialization) are made available to the user. These facilities are divided into two groups of commands as follows:

1. LOAD Group -- contains commands for initializing the OS, loading a stand-alone program, loading a diagnostic program, or restarting a program from an initialized state.
2. DEBUG Group -- contains commands for displaying or modifying Main Memory, general registers, control registers, or the PCW. Also included in this group are commands for single step program execution, hard copy dump of memory and registers, and virtual address translation.

Control Mode uses Workstation 0 for communications between the operator and the System. To enter Control Mode, Workstation 0 must be powered-on. Control Mode uses only the top line of the CRT display (line 1); the contents of the line are saved on entry and restored at exit. This makes Control Mode transparent to any program that may be using Workstation 0. For a detailed discussion of Control Mode commands, refer to Chapter 8 of the VS Principles of Operation manual (800-1100P0). All standard VS 60/80 control mode functions are available on the VS-100.

8.5 CONTROL MODE DUMP

This procedure allows the user to dump the contents of certain areas of Main Memory to a specified disk drive or tape for later analysis.

CAUTION

Control mode dump will destroy the VTOC on the pack being dumped to, it will NOT destroy the label.

To begin a Control Mode dump, proceed as follows:

1. Place System in Control Mode.
2. Record the displayed current Program Control Word (PCW).
3. Key in: P 000070 (ENTER) -- Where 'P' is the Physical Memory Address. This displays the Master Control Block (MCB) pointer, as follows:

   AAAAXXXX XXXXXXXX

   Where AAAA is the address of the MCB and X = "don't care".
4. Key in: P 00AAAA (ENTER) -- Where AAAA is address of MCB from Step 3. This displays the first 8 bytes of the MCB, as follows:

   XXXXXXXX XXXXDDDD

   Where DDDD is the address of the dump program in main memory and X = "don't care".
5. Key in: W (ENTER).

   This will display the present PCW.
6. Key in: M 0000DDDD 00000000 (ENTER) -- Where DDDD is the address of the dump program from step #4. All other places must be zero-filled.
7. Key in: P 00DDD(D-2) (ENTER) -- Where DDD(D-2) is the dump program address from step #4 minus two. This will display a portion of memory as follows:

   QQQQXXXX XXXXXXXX

   Where QQQQ is the Physical Device Address (PDA) of the device receiving the memory dump. Construct QQQQ as follows:

   BBBI IIPP PPPP PPPP

   Where: BBB = BA #; III = IOP #; PP PPPP PPPP = Port #

   Example: 2401 = BA #1, IOP #1, Port #1.
8. Ensure that the device being dumped to is <u>not</u> ready.
9. Key in: W (ENTER).
10. Key in: X (ENTER). At this point the DUMP program assumes control and forces the CPU back into Control Mode.
11. Remove the Control Mode bit from the PCW as follows:

    XXXXXXXX ZXXXXXXX is the PCW where Z is the digit containing the Control Mode bit -- bit 3 of the digit. Remove the bit by typing M, spacing to the Control Mode digit, and modifying it to turn off (setting to zero) the Control Mode bit. Ensure that only the Control Mode bit is changed -- i.e., If digit = 4 change it to 0; if digit = C change it to 8.

12. Key in: X (ENTER). This will start the dump waiting for pack or tape mount on drive. The dump will go to that drive upon unsolicited interrupt, and the System will fall into the Control Mode with:

    PCW = XXXXXXXX C000C000

This completes a memory dump.

8.6 FILING A MEMORY DUMP

In order to obtain a hard copy of a memory dump, or to allow the dump to be backed up onto tape, diskette, or another disk, the data obtained from a dump must be filed from the disk receiving the original dump to another disk. Doing this converts the dump data into a form usable by the System. To create a disk file from a memory dump, proceed as follows:

1. Mount the dump disk pack on a previously IPL'd System as an SL (Standard Label) pack.
2. Execute the FLOPYDUP program.
3. Using option "C" of FLOPYDUP program, copy the dump onto the previously mounted pack (ensure pack has a VTOC on it).
4. When output file is requested, change number of records to 1026.
5. The FLOPYDUP program will reply with a re-verify query to ensure that change is wanted. Affirm this.
6. This file can now be backed up on an individual basis (or as part of regular backups) to tape or other disk packs.

APPENDIX A

RECOM-MENDED SPARES LIST

APPENDIX A
RECOMMENDED SPARES LISTS (RSLs)

"A"-LEVEL* RSL

WLI PART #	NAME/DESCRIPTION	QTY
270-0458	Motherboard Ass'y	1
220-3001	16-pin 13" Flat Cable	1
220-3115	Cache-to-SBC Cable	2
220-3117	Cache-to-BA Cable	2
220-3116	SBC-to-BA Cable	2
220-3148	Control Memory-to-Maintenance Panel Cable	1
220-3149	Control Memory-to-Maintenance Panel Cable	1
220-3151	B Bus-to-Maintenance Panel Cable	1
220-3152	B Bus-to-Maintenance Panel Cable	1
220-3145	Minifloppy Data Cable	1
220-3110	Motherboard-to-Motherboard Cables	4
220-3146	Front Panel-to-Motherboard Cable	1

* "A" (AREA) LEVEL RSL lists those parts which, because of cost or low failures, are not economical to replace at the Branch level.

"B"-LEVEL* RSL

WLI PART #	MODEL #	CEI PART #	NAME/DESCRIPTION	QTY
210-7600-A			CP1 (A-BUS)	1
210-7601-A			CP2 (B-BUS)	1
210-7602-A			Control Memory (CM)	1
210-7603-A/				
7703-A			Main Memory (MM)	2
210-7604-A			Cache Memory	1
210-7605-A			SBC	1
210-7611	CO-1001	177-7101	BUS Adapter (BA)	1
270-0459			Mini Disk Controller	1
278-4004			5" Mini-Floppy Drive (SA400)	1
270-0706			Switching Power Supply	1
270-0460	Domestic		Linear Power Supply (60 Hz)	1
270-0460-1	Intrntn'l		Linear Power Supply (50 Hz)	1
210-7613			Front Panel Board	1
210-7614			Maintenance Panel	1
360-0000			Fuse Holder	1
279-0300			On/Off Switch	1
370-0026			LED (Power Box)	1
400-1003			Muffin Fan	1
377-0345			Chips, Main Memory (16K)	20
377-0360			Chips, Control Memory	20
377-0413			Chips, Cache Memory	20
360-1020			Fuse 2A	24
212-3022	(22V27-2)	177-7107	Serial IOP (16 Port)	1
212-3020	(22V26-3)	177-7105	TC IOP (3 Port)	1
212-3017	(22V25-2)	177-7102	Dual Density Tape IOP	1
212-3023	(22V28)	177-7108	Large Disk IOP	1

* "B" (BRANCH) LEVEL RSL lists those parts needed to perform corrective maintenance successfully 80% of the time. Also lists those parts needed to perform preventive maintenance successfully 100% of the time.

APPENDIX
B
VS-100
ILLUSTRATED
PARTS
BREAKDOWN

APPENDIX B

ILLUSTRATED PARTS BREAKDOWN

B.1 SCOPE

This appendix contains the illustrated parts breakdown for the VS-100 Computer System. Use this breakdown for part number identification when ordering field-replaceable components.

VS 100 CABINET ASSEMBLY (ASSEMBLY PART NO. 279-4125)

ITEM NO.	PART NO.	DESCRIPTION
1	458-0971	PANEL SIDE L.H. WELDMENT
2	654-1286	FLAT CABLE CLAMP
3	451-5026	STIFFNER BRACKET L.H.
4	660-0791	FILTER FOAM VENT PANEL
5	660-0792	FILTER FOAM FRONT PANEL TOP
6	451-3126	PANEL VENT DRESS SILK SCREEN
7	650-9013	1/4-20x1/2 FLANGE WHIZ LOCK
8	458-0973	PANEL, FRONT WELDMENT
9	660-0789	FILTER FOAM ACCESS DOOR TOP
10	220-1701	WIRE & LUG ASSEMBLY
11	652-0032	6-32 LOCKNUT KEPS
12	451-3123	PANEL LED SUPPORT
13	452-2227	DEAD FRONT PANEL
14	650-6122	10-32x3/8 FLANGE WHIZ LOCK
15	458-0961	HINGE, DOOR
16	458-0958	DOOR ACCESS FRONT PANEL
17	660-0788	FILTER FOAM ACCESS DOOR BOTTOM
18	651-0233	CATCH PUSH BUTTON (4 PCS)
19	653-6001	#10 WASHER INT. TH.
20	652-6002	10-32 KEPS NUT
21	451-7111	BRACKET BOTTOM LATCH
22	279-4126	VS 100 FRONT PANEL ASSEMBLY
23	650-6201	10-32x5/8 FLANGE WHIZ LOCK
24	458-0709	STOP LATCH 2263
25	650-4133	8-32x3/8 FLANGE WHIZ LOCK
26	654-0125	TERMINAL LUG
27	660-0790	FILTER FOAM FRONT PANEL BOTTOM LEFT
28	650-3121	6-32x3/8 FLAT HEAD PHL SCREW
29	660-0793	FILTER FOAM FRONT PANEL FRONT LEFT
30	458-0956	PAN, BOTTOM
31	451-5025	STIFFNER BRACKET R.H.
32	650-9013	1/4-20 FLANGE WHIZ LOCK
33	650-9024	5/16-18x3/4 HEX HEAD SCREW
34	653-6008	5/16 SPLIT WASHER
35	458-0950	FRAME UPPER
36	653-6006	1/4 FLAT WASHER
37	458-0972	PANEL SIDE R.H. WELDMENT
38	650-6201	10-32x5/8 FLANGE WHIZ LOCK
39	449-0229	PAD LATCH MOULDING 220 VS
40	655-0032	GLIDES LEVELING

VS 100 CABINET ASSEMBLY (ASSEMBLY PART NO. 279-4125)

ITEM NO.	PART NO.	DESCRIPTION
41	655-0020	CASTER 2" DIA DUAL WHEEL
42	652-0020	1/4-20 WHIZ LOCK NUT
43	650-9013	1/4-20 FLANGE WHIZ LOCK NUT
44	451-7107	STIFFNER REAR, VS 100
45	451-1991	RAIL, FRONT FACE PLATE
46	652-0021	5/16-18 HEX NUT
47	653-6008	5/16 SPLIT WASHER
48	653-6025	WASHER FLAT .328x.562 .063 T SS
49	451-1990	RAIL, REAR FACE PLATE
50	650-6122	10-32x3/8 FLANGE WHIZ LOCK
51	478-1070	CABLE SUPPORT
52	650-3280	6-32x7/8 LG. PAN HD PIL
53	652-0032	6-32 LOCKNUT KEPS
54	279-4066	TOP COVER ASSEMBLY
55	651-0226	RECEPTICLE "D-ZUS" #SL4X-280
56	651-0225	STUD OVAL HEAD "D-ZUS" AJ4-60
57	655-0254	BUMPER, .640OD x .340
58	458-0499	STOP, TOP COVER (2200VS)
59	650-6122	10-32x3/8 FLANGE WHIZ LOCK
60	462-0519	STANDOFF
61	650-9013	1/4-20x1/2 FLANGE WHIZ LOCK
62	653-6006	1/4 F' AT WASHER
63	270-0696	VS-100 FILTER BOX ASSEMBLY
64	650-6122	10-32x3/8 FLANGE WHIZ LOCK

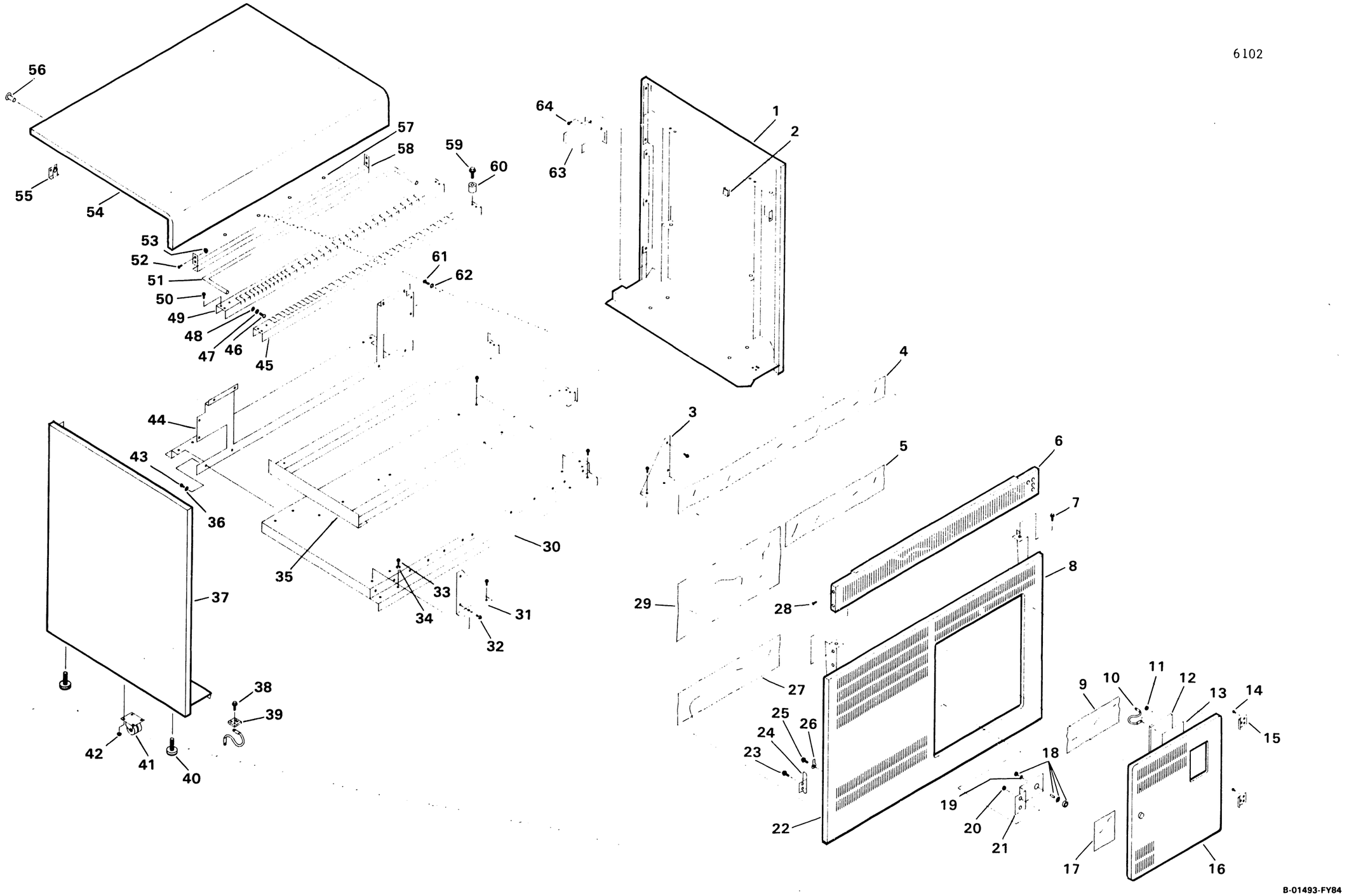


FIGURE 1 CABINET ASSEMBLY (ASSEMBLY PART NO. 279-4125)

VS-100 FAN ASSEMBLY (ASSEMBLY PART NO. 270-0697)

ITEM NO.	PART NO.	DESCRIPTION
1	652-0029	#8 KEPS NUT
2	272-0012	SWITCH BRACKET ASSEMBLY
3	458-1030	HANGER LED BOARD
4	210-7613	FRONT PANEL BOARD ASSEMBLY
5	220-1552	MAINTENANCE PANEL CABLE
6	462-0064	SPACER 8-32 .25OD .375L HEX
7	210-7614	VS-100 MAINTENANCE PANEL
8	220-3154	16 PIN FLAT CABLE ASSEMBLY
9	220-3152	VS-100 FNT. "B" BUS MAINTENANCE PNL
10	653-3002	#6 FLAT NYLON
11	650-3120	6-32x3/8 PAN HD SEMS
12	220-3151	"B" BUS MAINTENANCE PNL BACK
13	220-3153	16 PIN FLAT CABLE ASSEMBLY
14	451-2357	COVER, MAINTENANCE PANEL
15	650-3320	6-32x1 PAN HD SCREW
16	653-3000	#6 FLAT WASHER
17	653-3002	#6 NYLON WASHER
18	462-0017	SPACER .171ID .250OD
19	220-3146	FLOPPY CONT. SIG. CABLE
20	220-3149	CONT. MEM. ERT. MAINTENANCE PANEL
21	220-3148	BK. CONT. MEM. BOM. MAINTENANCE PANEL
22	478-1029	COVER, TERMINAL BLOCK
23	462-0204	SPACER .140ID .250OD .437L ROUND
24	310-1206	TERMINAL BLOCK
25	400-1003	FAN MUFFIN
26	220-1550	FAN ASSEMBLY CENTER
27	270-0697	VS-100 FAN ASSEMBLY
28	651-0071	WING HEAD 1/4 TURN FASTENER
29	449-0101	FAN GUARD 4" BLACK

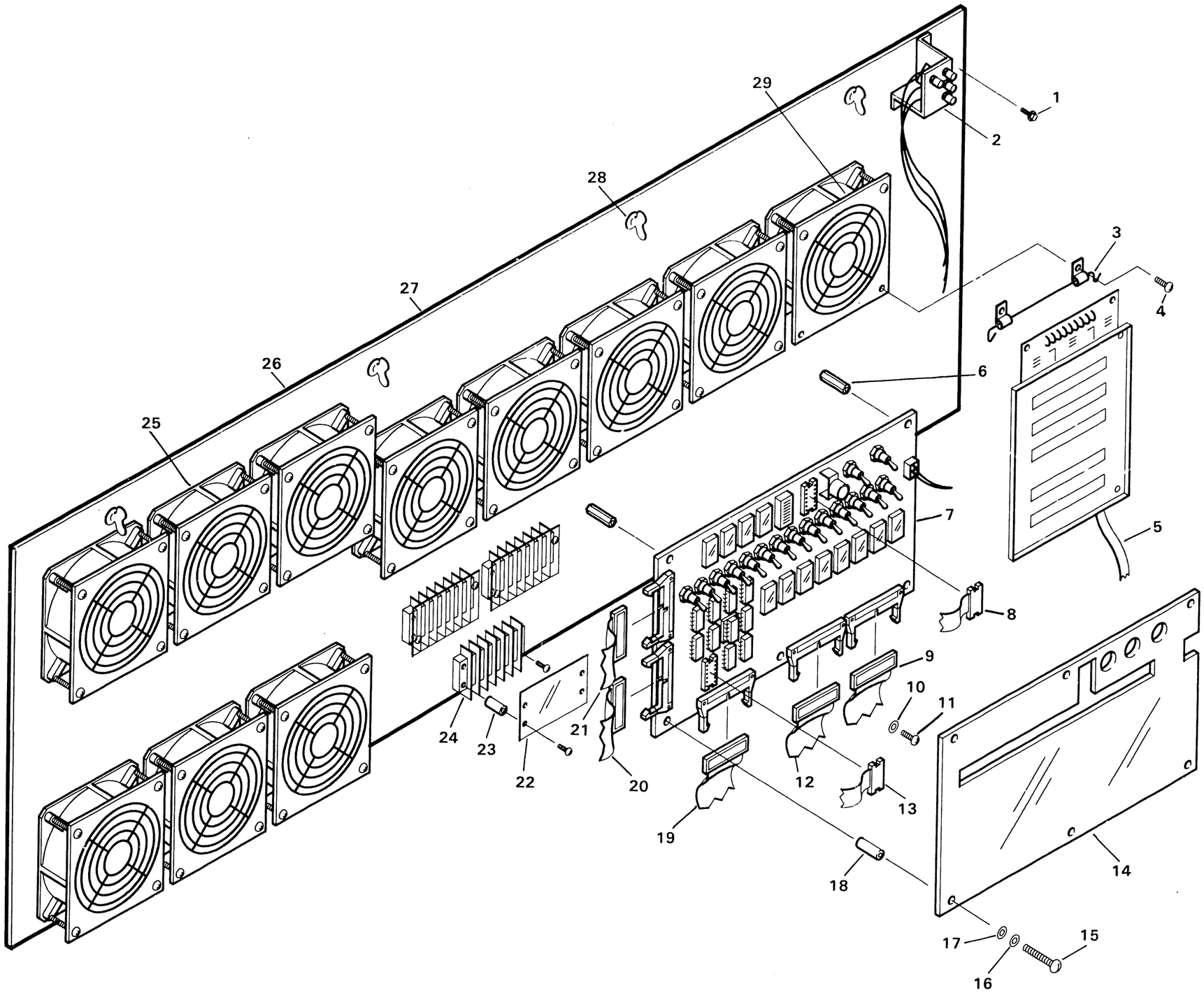


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FIGURE 2 VS-100 FAN ASSEMBLY (ASSEMBLY PART NO. 270-0697)

UNIT, FRONT ASSEMBLY (NO ASSEMBLY PART NO.)

ITEM NO.	PART NO.	DESCRIPTION
1	451-5034	BRACKET, CATCH POWER BOX
2	350-2124	CONNECTOR 4 POS FEMALE 1200V
3	650-3132	6-32x3/8TRUSS HD PARKERIZE
4	652-0032	6-32 LOCKNUT KEPS
5	350-2121	CONNECTOR 4 POS FEMALE 73V
6	451-5030	BRACKET POWER BOX CONN.
7	279-0456	POWER BOX ASSEMBLY VS-100
8	650-3120	6-32x3/8 PAN HD PHIL
9	653-3000	6-32 FLAT WASHER
10	325-2524	CIRCUIT BREAKER 20AMP 200V
11	220-1191	CABLE GROUND
12	650-6122	10-32x3/8 FLANGE WHIZ LOCK
13	458-0960	CHASSIS POWER BOX SILKSCREEN
14	650-4120	8-32x3/8 PAN HD PHIL SEMS
15	653-4000	WASHER #8 FLAT
16	325-9034	PUSH BUTTON RED
16	325-9035	PUSH BUTTON BLACK
17	220-1539	POWER BOX LED SWITCH CBL
18	220-1538	POWER BOX CABLE
19	451-5024	BRACKET MINI FLOPPY L.H.
20	210-7610-A	VS-100 MINI DISK CONTROLLER
21	270-0459	MINI FLOPPY ASSEMBLY
22	462-0204	SPACER, .140ID .250OD
23	653-3002	#6 FLAT NYLON WASHER
24	650-3207	6-32x5/8 PAN HD PHIL
25	650-6560	10-32x1 3/4 PHIL SCREW
26	653-6003	#10 SPLIT WASHER
27	451-5023	BRACKET MINI FLOPPY R.H.
28	653-3000	#6 FLAT WASHER
29	650-3120	6-32x3/8 PAN HD PHIL SEMS
30	654-2105	JACK TIP BLUE
31	654-2104	JACK TIP GREEN
32	654-2103	JACK TIP RED
33	654-2102	JACK TIP BLACK
34	400-1003	FAN MUFFIN
35	652-0032	6-32 LOCKNUT KEPS
36	653-3000	WASHER, #6 FLAT
37	650-3207	6-32x5/8 SCREW
38	220-1553	CABLE, POWER BOX TO POWER SUPPLY
39	654-1289	SNAP BUSHING
40	220-1535	FAN CORD

UNIT, FRONT ASSEMBLY (NO ASSEMBLY PART NO.)

ITEM NO.	PART NO.	DESCRIPTION
41	654-1303	HEYCO STRAIN RELIEF SR-4N-4
42	650-6122	10-32x3/8 FLANGE WHIZ LOCK
43	220-1581	CABLE, GROUND
44	220-1528	POWER SUPPLY CABLE
45	220-1529	POWER SUPPLY CABLE
46	220-1530	POWER SUPPLY CABLE
47	653-4000	WASHER, #8 FLAT
48	650-4133	8-32x3/8 FLANGE WHIZ LOCK
49	220-1191	CABLE, GROUND
50	451-2110	BRACKET CATCH POWER SUPPLY
51	650-6122	10-32x3/8 FLANGE WHIZ LOCK
52	220-1557	CABLE, 5V POWER LONG
53	220-1556	CABLE, 5V POWER SHORT
54	PART OF 57	
55	650-9012	1/4-20x3/8 FLANGE WHIZ LOCK
56	270-0706	SWITCHING POWER
57	654-0194	LUG CABLE CONNECTOR
58	458-1007	BRACKET SWITCHING BRIDGE
59	458-1008	BRACKET SWITCHING BRIDGE
60	652-0020	1/4-20 NUT WHIZ LOCK
61	653-6006	WASHER 1/4 FLAT
62	650-9012	1/4-20x3/4 FLANGE WHIZ LOCK
63	220-1527	POWER SUPPLY POWER CORD
64	270-0460(TW)	WANG POWER SUPPLY (VS-100)
65	220-1540	MINI FLOPPY POWER
66	220-3145	MINI FLOPPY DATA CABLE

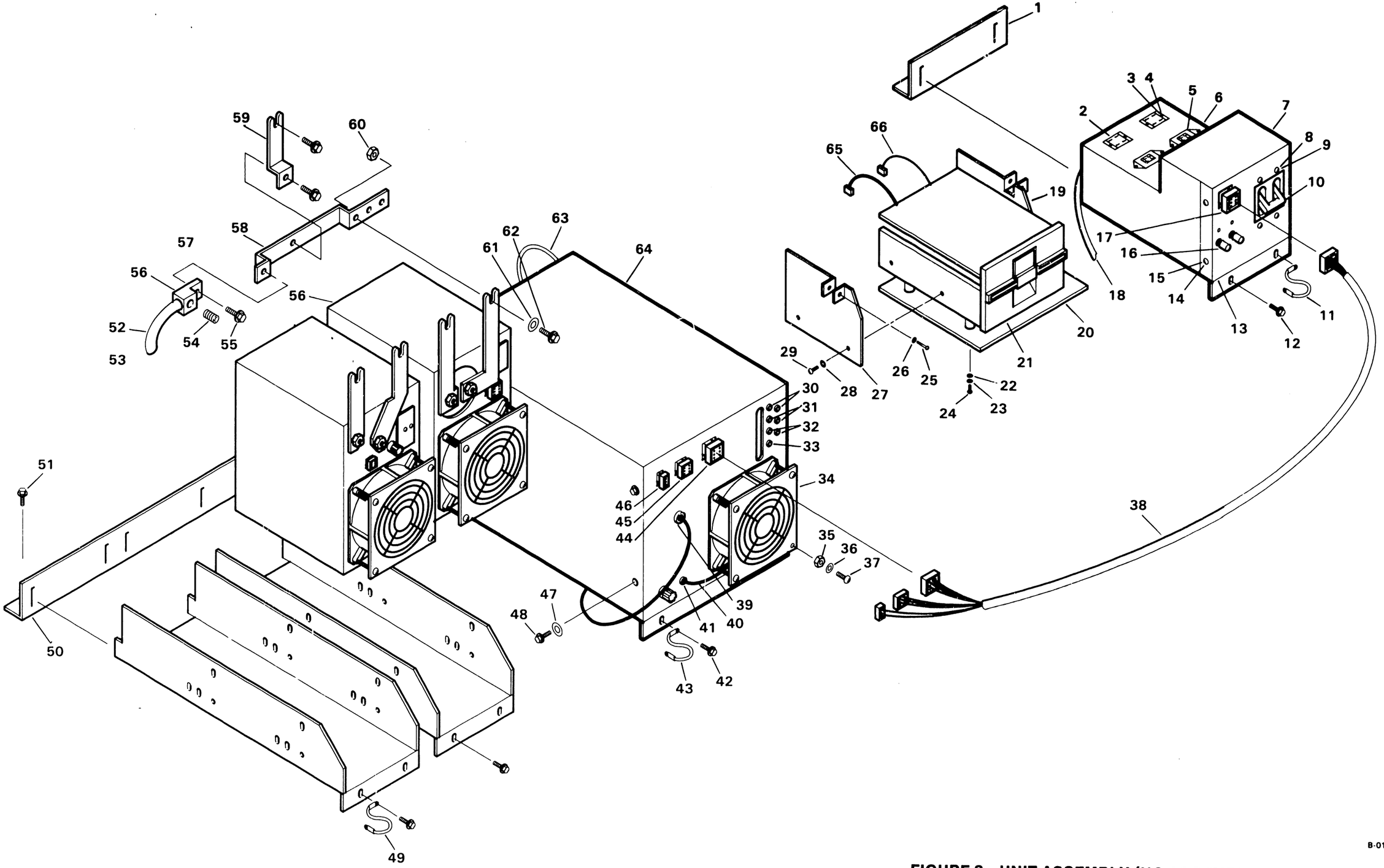

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FIGURE 3 UNIT ASSEMBLY (NO ASSEMBLY PART NO.)

UNIT, REAR ASSEMBLY (NO ASSEMBLY PART NO.)

ITEM NO.	PART NO.	DESCRIPTION
1	650-4127	8-32x3/8 PAN HD PHIL SCREW
2	270-0741	TELEX TAPE CONNECTOR PLATE
3	652-0032	6-32 LOCKNUT
4	654-1011	3/8 GROUND LUG
5	350-1036	BNC CONNECTOR
6	350-2078	TNC BULKHEAD CONNECTOR
7	270-0704	PANEL, REAR, BNC-TNC
8	452-2394	PLATE BLANK
9	270-0705	TC CONNECTOR PLATE
10	270-0911	KENNEDY TAPE CONNECTOR PLATE
11	270-0910	DISK CONNECTOR PLATE

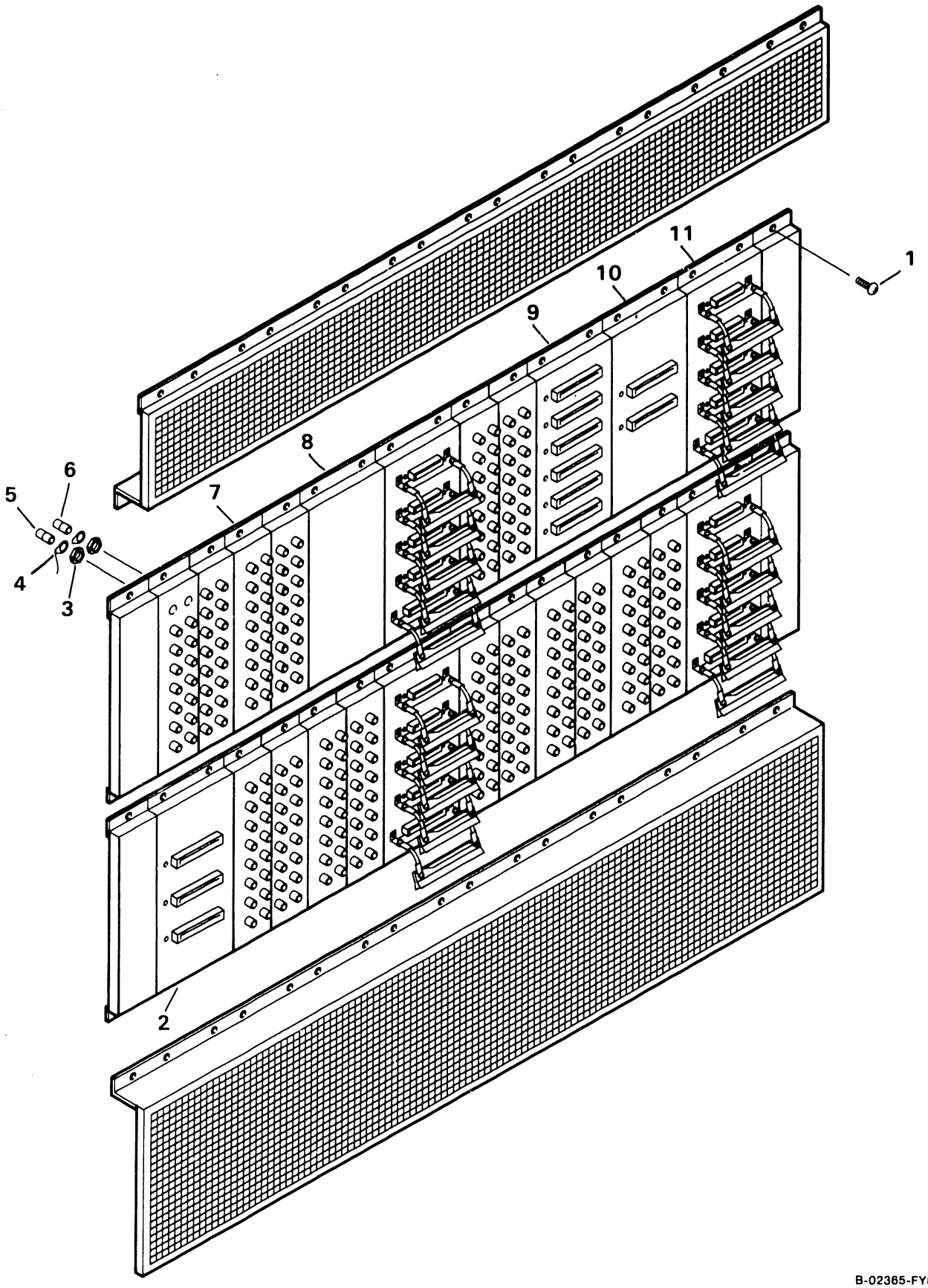


FIGURE 4 UNIT REAR ASSEMBLY (NO ASSEMBLY PART NO.)

MOTHERBOARD ASSEMBLY (ASSEMBLY PART NO. 270-0458)

ITEM NO.	PART NO.	DESCRIPTION
1	210-7602-A	CONTROL MEMORY BOARD
2	210-7600-A	A-BUS (CP1) BOARD
3	210-7601-A	B-BUS (CP2) BOARD
4	210-7604-1A	CACHE MEMORY BOARD
5	210-7605-A	SYSTEM BUS CONTROLLER BOARD
6	210-7803-2A	MAIN MEMORY BOARD
7	210-7911	BUS ADAPTERS
8	(SEE PG. 19)	I/O SLOT 0 (LARGE DISK IOP)
9	(SEE PG. 19)	I/O SLOT 1 (OPTIONAL DISK SLOT)
10	(SEE PG. 19)	I/O SLOT 2 (SERIAL IOP,WKSTN 0)
11	(SEE PG. 19)	I/O SLOTS 3-7 (OPTIONAL)
12	(SEE PG. 19)	I/O SLOTS 8 AND 9 (OPTIONAL DISK IOP)
13	(SEE PG. 19)	I/O SLOTS 10-15 (OPTIONAL)
14	650-2120	4-40x3/8 PAN HD PHIL
15	653-3000	#6 FLAT WASHER
16	653-3002	#6 NYLON WASHER
17	462-0512	SHIM FOR MOTHERBOARD .09
18	462-0511	SHIM FOR MOTHERBOARD .06
19	462-0510	SHIM FOR MOTHERBOARD .03
20	220-3110	MOTHERBOARD CONNECTOR CABLE
21	654-1289	SNAP BUSHING
22	654-1286	FLAT CABLE CLAMP
23	650-9013	1/4-20x1/2 FLANGE WHIZ LOCK
24	653-6006	1/4 FLAT WASHER
25	210-7608	CP MOTHERBOARD
26	210-7509	I/O MOTHERBOARD 1 (BA1)
27	210-7609	I/O MOTHERBOARD 2 (BA2)

MOTHERBOARD ASSEMBLY (ASSEMBLY PART NO. 270-0458)

IOP TYPE	PART NO.	DESCRIPTION
DISK	177-7108	EACH DISK IOP SUPPORTS A MAXIMUM OF FOUR 30/60/90M CMDs, AND/OR 75/288M CMDs.
SERIAL IOP 8-PORT	177-7106	SUPPORTS SERIAL PERIPHERAL DEVICES (W/S, PRINTER, AND ARCHIVING W/S).
SERIAL IOP 16-PORT	177-7107	SUPPORTS SERIAL PERIPHERAL DEVICES (W/S, PRINTER, AND ARCHIVING W/S).
TAPE	177-7102	SUPPORTS 7/9 TRACK, 800/1600 BPI TAPE DRIVES.
TC IOP	177-7103	SUPPORTS ONE TC PORT, BOTH MODEM AND ACU.
TC IOP	177-7104	SUPPORTS TWO TC PORTS; BOTH MODEMs AND ACUs.
TC IOP	177-7105	SUPPORTS THREE TC PORTS; BOTH MODEMs AND ACUs.

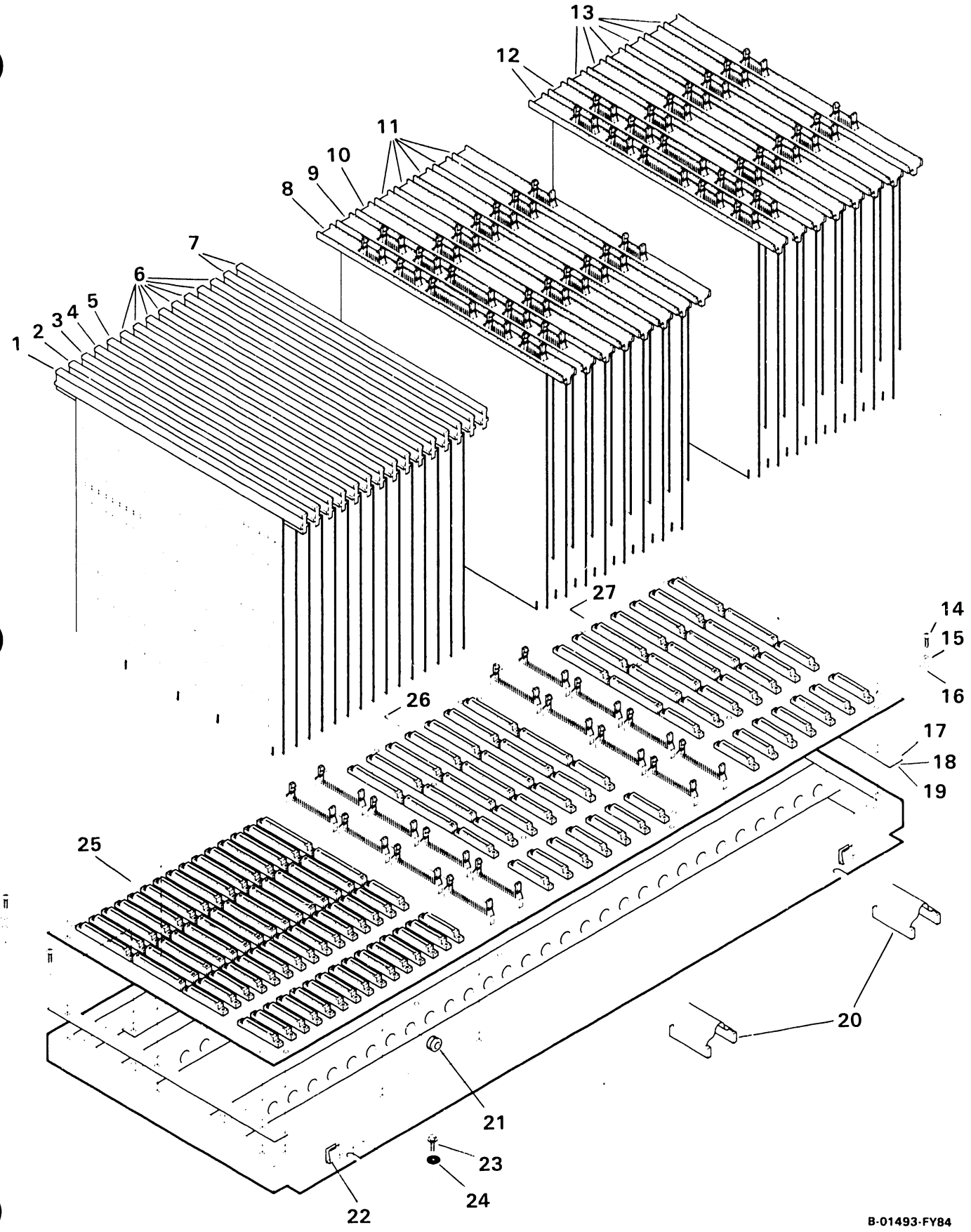


FIGURE 5 MOTHERBOARD ASSEMBLY (ASSEMBLY PART NO. 270-0458)

CABLING ASSEMBLY (NO ASSEMBLY PART NO.)

ITEM NO.	PART NO.
1	279-0358 (14)
2	220-3150
3	220-3147
4	220-3110 (8)
5	220-3153
6	220-1553
7	220-1552
8	220-3152
9	220-3146
10	220-1540
11	220-1581
12	220-1581
13	220-3151
14	220-3148
15	220-3149
16	220-3154
17	220-3116
18	220-3115
19	220-3001
20	220-3116
21	220-3116

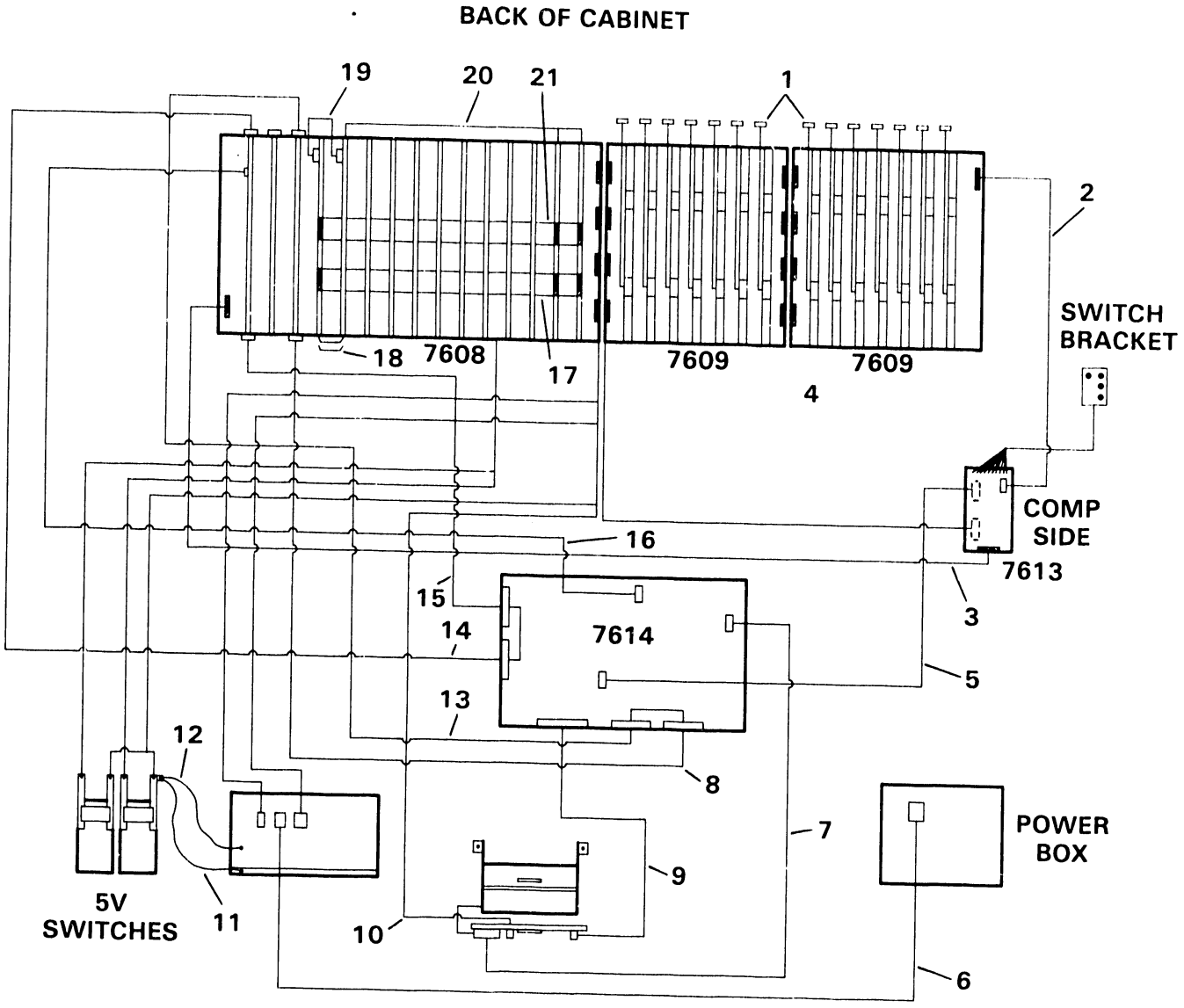


FIGURE 6 CABLING ASSEMBLY (NO ASSEMBLY PART NO.)

APPENDIX
C
VS-100
EQUIPMENT PART NUMBER LISTS

VS-100 SYSTEMS

PART #	SYSTEM SIZE (memory)
177-VS16F	512K
177-VS24F	768K
177-VS32F	1.0M
177-VS40F	1.2M
177-VS48F	1.5M
177-VS56F	1.7M
177-VS64F	2.0M

SYSTEM CONFIGURATIONS

Minimum VS-100 Configuration:

- 512-Kbyte Main Memory
- 2 W/S
- 1 Printer
- 1 Tape Drive and 1 Disk (30-300MB)
  - or,
- 2 Disk Drives (30-300 MB)
- 1 VS Archiver (VS-AWS)

Typical VS-100 Configuration:

- 768K to 1-Mbyte Main Memory
- Two 300 Meg Disk Drives
- 25 to 30 Workstations
- 3-4 Printers
- 2 TC Lines
- 1 VS Archiver (VS-AWS)

Maximum VS-100 Configuration:

- 2-Mbyte Main Memory
- 95 Workstations
- Sixteen 300 Mbyte Disk Drives
- 32 Printers
- 8 Tape Drives
- 6 TC Lines
- 1 VS Archiver (VS-AWS)

AVAILABLE SOFTWARE

NAME	PART #
COBOL	195-5100-3
RPGII	195-5200-3
BASIC	195-5300-3
FORTRAN-77	195-2087-3
PL/1	195-2086-3
TC REMOTE	195-2091-3
3270 EMULATION	195-2089-3
2780/3780 EMULATION	195-2090-3
DBMS	195-2088-3
WORD PROCESSING	195-2078-3
MAILWAY	N/A
HRMS	N/A

VS-100 PERIPHERAL DEVICES

DISK DRIVES

MODEL #	PART #	NAME/DESCRIPTION
2280V1,2,3	187-2280	Phoenix Disk 30, 60, 90
	167-2280	
2265V-1	187-2265V-1	80 Meg Disk
	167-2265V-1	
2265V-2	187-2265V-2	300 Meg Disk
	167-2265V-2	
2260V	187-9210	10 Meg Disk
	167-9210	

TAPES

MODEL #	PART #	NAME/DESCRIPTION
2209V	187-2209AV	9-Track 1600 bpi tape
	167-2209AV	
2209V-2	187-2209V-2	9-Track, 800/1600 bpi tape
	167-2209V-2	
2209V-3	187-2209V-3	7-Track, 800 bpi
	167-2209V-3	

WORKSTATIONS AND RELATED ACCESSORIES

MODEL #	PART #	NAME/DESCRIPTION
2246S	187-7022	Serial Workstation
	167-7022	
2246C	187-7020	Combined Workstation
	167-7020	
2246R	187-2246R	Remote Workstation
	167-2246R	
2247V-4	177-22VS-77	MODEM SHARING UNIT
2246S	187-7005	ERGO (279-2017 Keyboard)
	167-7005	
2246C	187-7004	ERGO (279-2018 Keyboard)
	167-7004	

PRINTERS

2263V-2S	187-2263S	600LPM Printer (Prt)
2263V-3S	187-9242	430LPM Prt
5531/2231V-2S	187-2231-P2	Matrix (Mat.) Prt
5521/2221V-S	187-2272-P1	2200CPS Mat Prt
6581W	187-9211/167-9211	40CPS Daisy Prt
6581WC	187-9219/187-9219	40CPS Wide Daisy Ptr
5574/2273V-2S	187-9284-1/167-9284-1	600LPM Band Prt
5573/2273V-1S	187-9285-1/167-9285-1	250LPM Band Prt
5521K		200CPS Katakana Mat Prt
55312K		120CPS Katakana Mat Prt
5548Z		Typesetter
IP41F		Intelligent Image Prt
5521I		200CPS Ideographic Mat. Prt
5581WD		Dual-Head Daisy Prt
CP210		Okidata Matrix Prt

AVAILABLE VS-100 IOPs

IOP TYPE	MODEL #	CEI #	WLI #	BOARD #	COMMENTS
Disk	22V28	177-7108	212-3023	210-7110T 210-7114	Each disk IOP supports a maximum of four 30/60/90M CMDs, and/or 75/288M SMDs.
Serial IOP 8-Port	22V27-1	177-7106	212-3021	210-7110W 210-7216A	Supports serial peripheral devices (W/S, Printer, and Archiving W/S).
Serial IOP 16-Port	22V27-2	177-7107	212-3022	210-7110W 210-7216A	Supports Serial peripheral devices (W/S, Printer, and Archiving W/S).
Tape	22V25-2	177-7102	212-3017	210-7110S 210-7217	Supports 7/9 Track, 800/ 1600 BPI Tape Drives.
TC IOP	22V26-1	177-7103	212-3018	210-7426C	Supports one TC port, both modem and ACU.
TC IOP	22V26-2	177-7104	212-3019	210-7426C 210-7427A	Supports two TC ports; both modems and ACUs.
TC IOP	22V26-3	177-7105	212-3020	210-7426C 210-74271A	Supports three TC ports; both modems and ACUs.

MISCELLANEOUS EQUIPMENT

MODEL #	PART #	DESCRIPTION
TSF-31	187-9220W	Twin Sheet Feeder for 6581W (Domestic)
TSF-33	187-9260	Twin Sheet Feeder for 6581W (Intern't'l)
TSF-41	187-9735	Twin Sheet Feeder for 6581WC (Domestic)
TSF-43	187-9260	Twin Sheet Feeder for 6581WC (Intern't'l)
N/A	725-0162	Ribbon for 2263V-2S and 3S printers
N/A	279-0181	Ribbon for 2231V-2S
N/A	279-0159	Ribbon for 2221V-S
N/A	279-5204	Ribbon (film) for 6581W/WC printers
N/A	279-5234	Ribbon (fabric) for 6581W/WC printers
N/A	720-6124	Print Wheel for 6581W and 6581WC printers
N/A	279-5161	Shield for 6581W printer
N/A	279-5162	Shield for 6581WC printer
N/A	279-5159	Tractor for 6581W printer
N/A	279-5148	Tractor for 6581WC printer
N/A	705-0154	System Microcode Diskette

AVAILABLE CABLES

SERIAL PERIPHERAL LOCAL CABLES

PART #	DESCRIPTION
220-0148	25' 2246S/C Workstation Cable (standard w/device).
220-0148	25' 2246S/C ERGO Workstation Cable (standard w/device).
120-2300-1 to 120-2300-40	Optional-length peripheral device cable. As final digit of part number is incremented, length of cable increases by fifty feet--WLI #120-2300-1 is a 50' cable; WLI #120-2300-40 is a 2000' cable.

REMOTE WORKSTATION CABLES

PART #	DESCRIPTION
220-0219	25' 2247V-4 MSU-to-modem Cable (standard w/device).
220-0247	25' 2246R Workstation-to-MSU Cable (standard w/device).
120-2247-01	50' 2246R-to-MSU Cable (optional).
120-2247-02	100' 2246R-to-MSU Cable (optional).
120-2247-03	200' 2246R-to-MSU Cable (optional).
120-2247-04	300' 2246R-to-MSU Cable (optional).
120-2247-05	400' 2246R-to-MSU Cable (optional).
120-2247-06	500' 2246R-to-MSU Cable (optional).

DISK DRIVE CABLES

PART #	DESCRIPTION
220-3031	10' "A" cable for all VS-100 disk drives
220-3041	15' "A" cable for all VS-100 disk drives
220-3033-1	15' "B" cable for all VS-100 disk drives
220-3033-4	24' "B" cable for all VS-100 disk drives

TAPE CABLES

PART #	DESCRIPTION
220-0168	12' IOP-to-Formatter cable
220-3059	12' Formatter-to-Tape Drive cable

APPENDIX D

MNE-MONIC LIST

APPENDIX D

MNEMONICS LISTS

VS-100 HARDWARE MNEMONICS

MNEMONIC	MEANING
ACT	B.A. "Active" status bit. Accept/reject IOP memory commands
ADMX	Memory Address Multiplexer
ALU	Arithmetic Logic Unit
AMX	A-Bus Multiplexer
BA	Bus Adapter
BAAR	Bus Adapter Address Register
BADRLH	Bus Adapter Read Data Latch High
BADRLL	Bus Adapter Read Data Latch Low
BALU	Binary Arithmetic Logic Unit
BAM	Bus Adapter Multiplexer
BAMAL	Bus Adapter Memory Address Latch
BARDLA	Bus Adapter Read Data Latch "A"
BARDM	Bus Adapter Read Data Multiplexer
BAWDL	Bus Adapter Write Data Latch
BMDL	Bus Adapter Memory Data Latch
BMX	B-Bus Multiplexer
BRMX	Branch Multiplexer
BS	Buffer Word Select
BSM	Byte Swap Multiplexer
BTL	Bus Transaction Log
CABF	Control Memory Address Buffer
CAM	Cache Address Multiplexer
CAR	Current Address Register
CAR/IAR	Current/Indirect Address Register
CAR/IAR L/I	Current/Indirect Address Register Latch/Incrementer
CAS	Column Address Strobe
CBL	C-bus Latch
CBMMX	C-bus/Main-Memory Data Multiplexer
CCPMAL	Current CP Memory Address Latch
CDIBF	Control Memory Data Input Buffer
CDOBF	Control Memory Data Output Buffer
CDOMX	Control Memory Data Output Multiplexer
CE/D	Cache Enable/Disable
CEN	Column Enable
CH	Current Halfword
CHBF	Current Half-word Buffer
CM	Control Memory
CMAL	Control Memory Address Latch
CMBF	Control Memory Buffer
CMBI	Control Memory Bus Interface. IOP memory control micro inst.
CMR	Control Memory Register
CMX	C-Bus Multiplexer
CMnn	Control Memory bits: CM0 through CM47
CP/BADM	CP/Bus Adapter Data Multiplexer
CPDL	CP Data Latch
CPMAL	CP Memory Address Latch

MNEMONIC	MEANING
CPWDR	CP Write Data Latch
CPWSM	CP Word Swap Multiplexer
CRDY	Cache Data Ready
DALU	Decimal Arithmetic Logic Unit
DCA	CP "Decimal Carry" status bit
DEC	CP "Invalid decimal digit" status bit
DRY	Data Ready
DTBF	Data Buffer to Main Memory
DWD	Doubleword
ECC	Error Correction Circuitry
ECR	External Condition Register
ECR/IPC/BTLDM	ECR/IPC or BTL Data Multiplexer
EN	Enable IPC
F	Fault
FA/BSM	FA (Signal FAnn)/Byte Swap Multiplexer
FAM	FA (Signal FAnn) Multiplexer
HS	Halfword Select
IAR	Indirect Address Register
IC	Instruction Counter
ICLD	Instruction Counter Load
INIT	Initialize
INVE	Invalid Even
INVO	Invalid Odd
IP/BAM	IPC/Bus Adapter Multiplexer
IPC	InterProcessor Communications
IPC/BTLDM	IPC/BTL Data Multiplexer
IPCA	IPC Active
IPCDL	IPC Data Latch
IREG	Indirect Register
IREG COUNTER	Eight bit binary counter
IREG MUX	Indirect Register Multiplexer
IRM	Interrupt Request Mask
LDRY	Load Data Ready
M	Monitor (status flag bit)
MAL	Memory Address Latch
MAMX	Memory Address Mux
MAR0	Memory Address Register #0
MAR1	Memory Address Register #1
MAR2	Memory Address Register #2
MBS1	Multiplier Buffer Storage 1
MBS2	Multiplier Buffer Storage 2
MCOS	Memory Complete Out Strobe
MDR0	Memory Data Register #0
MDR1	Memory Data Register #1
MDR2	Memory Data Register #2
MDR3	Memory Data Register #3
MDR4	Memory Data Register #4
MDR4B	MDR4, Buffered
MLPY	Multiplier Unit
MMAM	Main Memory Address Multiplexer
MMDL	Main Memory Data Latch
MMOSD	Main Memory Output Selector/Driver

MNEMONIC	MEANING
MMP	Main Memory Parity
MMPT	Main Memory Parity Trap
MODE	B.A. "Mode" status bit. Allow IOP Write/Read to main memory
MRC	Message Receipt Control
MRI	Memory Request In
NAMX	Next Address Multiplexer
O/EWDM	Odd/Even Word Data Multiplexer
OE/BSM	Odd/Even Byte Swap Multiplexer
OVF	CP "Overflow" status bit
PB	B.A. "PageBreak" status bit. Terminate/continue thru PB
PCB	Processor Communications Bus
PCBCS	PCB Control Out Strobe
PCBGS	PCB Grant Strobe
PCBRI	PCB Request In
PCBSI	PCB Strobe In
PDA	Physical Device Address
PMR	Program Mask Register
PMX	PMR Multiplexer
PR	Purge Buffer
Q	Qualifier
R	Ripple
R/B	Ready/Busy
R/RMW	Read/Read Modify Write
R/W	Read/Write
RABF	Control Memory Address Buffer
RAS	Row Address Strobe
RBS	Ready/Busy Status IOP bit
RCM	Read Control Memory (Deliver byte to PMR)
RDBF	Control Memory Data Buffer
RDSTR	Read Strobe
REF	Refresh
RMUX	Rotating Multiplexer
SAMX	Subroutine Address Multiplexer
SBC	System Bus Controller
SCR	Segment Control Register
SN	Send IPC
SR	Shift Register
SSTK	Subroutine Address Stack
STKMX	Stack Address Multiplexer
SW	Byte Switch
Snn(0-31)	CP Status bits
T	Termination
T-RAM	Translation Random Access Memory
TAL	T-RAM Address Latch
TC	Type Code
TCAM	Tag Compare Address Multiplexer
TDL	Tag Data Latch
TINT	Tester Interface
TOR	B.A. "To Be Written Out" status bit. Allow a write to be completed.
TRMUX	T-RAM Multiplexer
TT	Translation Trap

MNEMONIC	MEANING
VMAR	Virtual Memory Address Register
WA	Write Address Error
WCM	Write Control Memory (Set CM byte from PMR)
WK1	Work Register #1
WK1-A	Work Register 1--A-Bus
WK2	Work Register #2
WK2-A	Work Register 2--A-Bus
WMX1	WK1 Multiplexer
WMX2	WK2 Multiplexer
WP	Write Pulse

VS-100 SOFTWARE MNEMONICS

MNEMONIC	DEFINITION
ARS	Activate Read State
ATR	Word Alignment, Read
ATW	Word Alignment, Write
AWS	Activate Write State
BOP	Branch field of CP micro instruction
CC	Condition Code
CMD	Command
DCT	Device Configuration table
DTYPE	Dialog Type
FA	Fetch Address
FLUB	File Length and User Block
IEM	Interrupt Enable Mask
INVA	Invalid Address
IO	Input/Output
IOCA	I/O Command Address
IOCW	I/O Control Word
IOSW	I/O Status Word
IPC	Inter-Processor Communication
LRA	Load Real Address
LRU	Least Recently Used
M	Monitor bit
MMPFT	Main Memory Page Frame Table
MOP	Memory Operation field of CP micro instruction
NOP	No Operation
OS	Operating System
OVF	Overflow
PA	Physical Address
PCW	Program Control Word
PF	Page Frame
PFN	Page Frame Number
POP	Process field of CP micro instruction
PT	Page Table
PTA	Page Table Address
PTE	Page Table Entry
R/C	Reference and Change status bits
RCT	Reference/Change Table
RP	Read Protect
RS	Reset State
SA	Set Address
SAI	Set Address Indirect

MNEMONIC	DEFINITION
SIO	Start I/O
SQB	Status Qualifier Byte
VA	Virtual Address
WP	Write Protect

MICRO-INSTRUCTION MNEMONICS

MNEMONIC	DEFINITION
A	Add
AC	Add with Carry
ACO	Add with Carry (CA in = 1)
ACP	Add for Pagespan Check
ACT	Add with Carry (Overflow Trap option)
ACV	Add with Carry (Overflow bit set)
ACZ	Add with Carry (CA in = 0)
AND	Logical AND
ANDI	Logical AND Immediate
ANDS	Logical AND (with SGN bit set)
ASH	Add/Subtract High
ASL	Add/Subtract Low
AZH	Add High with Zeros
AZL	Add Low with Zeros
BD	Generate Base-Displacement Address
CAR	Compare Arithmetic and set CC
CCK	Clear Counter (Program Clock support)
CCS0	Set Logical CC (1-2 on SPX)
CCS1	Set Arithemtic CC (0-2 on ALU + SGN)
CCS2	Set Full Logical CC (0-3 on CA / ALU)
CCSET	Set Explicit CC Value (0-3)
CKECC	Check ECC (Read or Write control)
CL	Compare Logical and set CC
CMC	Clock Margin Control (Reset)
CMCF	Clock Margin Control Fast
CMCS	Clock Margin Control Slow
COMP	Compare Arithmetic
DAC	Decimal Add with Carry
DACZ	Decimal Add with Carry (DCA in = 0)
DSC	Decimal Subtract with Carry
DSCO	Decimal Subtract with Carry (DCA in = 1)
HALT	Halt Micro-program Execution
INIT	Initialize an IOP
LCOMP	Load Comparator (Program Clock support)
LTRAM	Load a T-RAM entry
MCA	Move and set Arithemtic CC
MCH	Move Current Halfword
MCHX	Move Current Halfword and Extend
MCL	Move and set Logical CC
MDEC	Move and Decrement IREG
MINC	Move and Increment IREG
MNUM	Move Numeric
MV	Move
MVA	Move Address (high byte = 0)
MVH	Move Halfword
MVN	Move (without setting ALU or C-Bus Latch)

MNEMONIC	DEFINITION	
MVS	Move	(with sgn bit set)
MVX	Move	(with non-standard B-Bus)
OR	Logical OR	
ORI	Logical OR Immediate	
RBCL	Read a BCL entry (hi-part)	(also RBCLL - low part)
RBTL	Read a BTL entry (hi-part)	(also RBTLL - low part)
RCM	Read Control Memory	
RECR	Read ECR	
RIPC	Read IPC Data	
RRCT	Reset an RCT entry	
RSW	Read Switches	
S	Subtract	
SC	Subtract with Carry	
SCO	Subtract with Carry	(CA in = 1)
SCOMP	Store Comparator	(Program Clock support)
SCT	Subtract with Carry	(Overflow Trap option)
SCV	Subtract with Carry	(Overflow bit set)
SCZ	Subtract with Carry	(CA in = 0)
SEND	Send IPC data to another Processor	
SHL4	Shift Left 4 bits	
SHLO4	Shift Left 4 bits	(4 bits in = 1111)
SHLZ4	Shift Left 4 bits	(4 bits in = 0000)
SHR	Shift Right 1 bit	
SHR4	Shift Right 4 bits	
SHRO	Shift Right 1 bit	(SCA in = 1)
SHRO4	Shift Right 4 bits	(4 bits in = 1111)
SHRZ	Shift Right 1 bit	(SCA in = 0)
SHRZ4	Shift Right 4 bits	(4 bits in = 0000)
STAT	Move IREG to Status bits	(IREG 4-7 to S12-S15)
STCK	Store Counter	(Program Clock support)
SW16	Move and Switch	
TRCT	Test an RCT entry	(set M2H, M2B)
WCM	Write Control Memory	
WECR	Write ECR	(5-bit unit)
WIPC	Write IPC Data	
XOR	Logical Exclusive OR	
XORI	Logical Exclusive OR Immediate	

VS-100 SIGNAL MNEMONICS DEFINITIONS

MNEMONIC	DEFINITION	SOURCE	DESTINITION	DESCRIPTION
AB0-AB31	A Bus	A-Bus	B-Bus	Data for Binary and Decimal ALUs
BAC0-2	Bus Adapter Command	BA	Cache	Bus Adapter command bits
BAWD0-63	BA Write Data	Cache	BA	Two words of data from main memory to BA or one word of IPC data from CP to BA
BMA0-23	Bus Adapter Memory Address	BA	Cache	Bus Adapter main memory addresses via Cache
BMA3-6	Bus-Main Memory Address	IOP	BA	IOP command bits for the BA
BMAR5-20	Buffered Memory Address	Cache	Main Memory	Main Memory addresses from either CP or BA
BMDH0-7	Bus-Memory Data High	IOP	BA	One byte of IOP data for BA
BMDL0-7	Bus-Memory Data Low	IOP	BA	One byte of IOP data for BA
CAWD0-63	Cache Write Data	SBC	Cache BA	Two words of data from main memory for either the BA or the Cache
CB0-CB31	C Bus	B-Bus	A-Bus	C-Bus output data
DAB0-7	Device Address Bits	BA	IOP	Device Address for IOP
DIRD0-31	Not defined	SBC	Cache	One word of main memory data for CP
IPC0-7	Interprocessor Communications	SBC	Cache	IPC Command
MA0-23	Memory Address	B-Bus	Cache	CP memory addresses for either main memory (MA0-23) or Cache tag compare (MA0-8)
MM0-15	Main Memory	BA	IOP	Data or status returned to IOP along with IAR/CAR addresses

MNEMONIC	DEFINITION	SOURCE	DESTINITION	DESCRIPTION
MM0-31	Main Memory	Cache	B-Bus	Word of data from either main memory or Cache for CP
MMCB1-2	Main Memory Bits Control	IOP	BA	IOP command bits for the BA
MMRD0-63	Main Memory Read Data	Main Memory	SBC	Two words of memory read data
MMWD0-63	Main Memory Write Data	SBC	Main Memory	Two words of data to be written to main memory
MS1-4	Module Select	Cache	Main Memory	Main memory board select from either CP or the BA
RA0-13	Not defined	B Bus	CM	Addresses for a Control Memory write
RD0-7	Not defined	B Bus	CM	Data for a Control Memory write
RPH0-6	Read Parity High	Main Memory	SBC	Parity bits for even word of read data
RPL0-6	Read Parity Low	Main Memory	SBC	Parity bits for odd word of read data
WD0-31	Write Data	A-Bus	SBC	CP write data to main memory
WPH0-6	Write Parity High	SBC	Main Memory	Parity bits for even word of write data
WPL0-6	Write Parity Low	SBC	Main Memory	Parity bits for odd word of write data

APPENDIX E

CPU/ECR STATUS BIT DEFINITIONS

APPENDIX E
CPU/ECR STATUS BIT DEFINITIONS

CPU STATUS BITS

Status Bits	Label	Definition
S0	ALU	Result Bit for last ALU C-bus value (=0 or non-zero)
S1	CA	Carry Bit (Carry Out from arithmetic operations)
S2	PAGE1	MAR1 page bit (set on ripple)
S3	PAGE2	MAR2 page bit (set on ripple)
S4	PAGE0V	VMAR0 page bit (set on ripple)
S5	EXEC	Execute Flag; Stop after Target if EXEC = 1 (in BNM)
S6	M2H	Bit is set = to MAR2 bit 30 when MAR2 is destination MAR for translation operation
S7	M2B	Bit is set = to MAR2 bit 31 when MAR2 is destination MAR for translation operation
S8	SGN	Set from high order bit of 32-bit C-bus, etc. Value = 0/1 indicates two's complement sign bit
S9	DEC	Invalid decimal digit bit. (Set = 1 by hardware if invalid decimal digit found)
	OVF	Overflow bit (2's complement arithmetic). OVF = (CA-out) XOR (CA-out at bit position 1)
S10	DCA	Carry bit for Decimal process operations
S11	PCA	Carry out bit set by micro-opcode = ACP only
	SPX	Result bit (inverse) set only on micro-opcode = CL. Also set as comparison bit for micro-opcode = COMP.
S12	ALUS	Zero/non Zero status bit for 4-bit Shift-hold register. Set only on 4-bit shift instructions.
S13	X2	This bit = 0 if IREG 4-7 = 0; else = 1
S14	R10DD	This bit is set = IREG bit 3
S15	FLT	This bit is set based on IREG and ILC (CH0-CH1). (ILC = instruction length code in Current Halfword).
	RR Case	ILC = 00; set FLT = IRG0 or IRG3 or IRG4 or IRG
	RX Case	ILC not = 00; set FLT = IRG0 or IRG3
S16	CS2	Comparator enable bit (Set by CP4; inspected by hardware)
S17	STATE	Software bit for priviledged status (on translation)
S18	MS1	MAR select bit for translation fault involving MAR1 or MAR2 (MS1=0 for VA in MAR1; MS1=1 for VA in MAR2). Note - MS1 is always set = 0/1 for translation operations involving MAR1 or MAR2
S19	STK	This bit = 0 if IREG 0-3 = 0; else = 1
S20	BNK	Used as CP4 stack address bit. (Set by BNM)
S21	PAGE0	MAR0 page bit (set on ripple)
S22	M0F	MDR0 full bit (empty = 0, full = 1)
S23	M1F	MDR1 full bit (empty = 0, full = 1)
S24	DEBUG	One or more Software Traps enabled if set = 1
S25	IOMASK	IO Interrupts enabled if set = 1
S26	CS4	Clock Interrupt enabled if set = 1
S27	ISET	Bit 1 of the multi-way BNM micro-address
S28	CS1	Hardware Counter Overflow bit
S29	CS3	Clock Interrupt Request Pending if set = 1
S30	EXT	External Event bit (see ECR for setting)
S31	IO3	BA Interrupt-Request Pending if bit = 1

EXTERNAL CONDITION REGISTER (ECR) STATUS BITS

Status Bits	Label	Definition
ECR0	IN1	Initialize/enable B.A. #1.
ECR1	IN2	Initialize/enable B.A. #2.
ECR2	IN3	Initialize/enable B.A. #3.
ECR3	IN4	Intiialize/enable B.A. #4.
ECR4	MON	Monitor System Code.
ECR5	ECC	Enable/disable ECC.
ECR6	BTL	Enable/disable BTL.
ECR7	BCL	Enable/disable BCL.
ECR8	Cache	Enable/disable Cache ($\overline{CE}$/D).
ECR9	Reserved.	
ECR10	WP	C.P. write parity error (preset by MMP and $\overline{CP8W}$).
ECR11	WA	Incorrect C.P. write address (preset by UNVA and CPW).
ECR12	RJ	Reject IPC data from C.P. (preset by RJ and CP).
ECR13	Reserved.	
ECR14	HM	Cache hit (preset by $\overline{MISS}$ high).
ECR15	CAM	Cache miss (preset by $\overline{MISS}$ low).
ECR16	RJO	Reject IPC data sent from any processor (preset by RJ and CP).
ECR17	BTLA	BTL active, stored error entry.
ECR18	BTLO	BTL overflowed.
ECR19	CM	Control mode button (preset by CM).
ECR20	BA1	B.A #1 requested attention ($\overline{REQ1}$).
ECR21	BA2	B.A #2 requested attention ($\overline{REQ2}$).
ECR22	BA3	B.A #3 requested attention ($\overline{REQ3}$).
ECR23	BA4	B.A #4 requested attention ($\overline{REQ4}$).

APPENDIX F

DEFINI-TIONS OF TERMS

APPENDIX F
DEFINITIONS OF TERMS

TERM	DEFINITION
Background Processing	The automatic execution of batched lower-priority programs by the Operating System whenever no higher-priority programs are being handled.
Base Address	Starting address of a page frame.
Byte Index	A value, when added to a base address, that results in the true physical address of a byte in main memory.
Cache Hit	Successful Cache Memory Read; no Main Memory cycle is required.
Cache Miss	Unsuccessful Cache Memory Read; a Main Memory cycle is initiated.
Command Processor	A special program used to call up all system functions.
Concatenated	Linked together in series.
Current PCW	The "active" or "controlling" Program Control Word--the one that pertains to the instruction that is currently being executed.
Data Base Management System	Process (program) that allows multiple users to access common data files.
Demand Paging	A memory management feature where portions of a program are called into memory as needed.
Displacement	See Byte Index.
Distributed Processing	a. The sharing of a Central Processor among more than one user. b. A network of computer systems that support the data processing needs of an organization, interacting with each other and a large data base through a larger computer that oversees the entire system.
Dynamic Access Mode	A technique which lets a program switch back and forth between sequential access and random access in the same data file.
Field	A single item of information one or more characters in length.
File	A collection of Logical Records having a common characteristic.

WORD/PHRASE	DEFINITION
Indexed Filing	A technique which stores data records in the order of specified key values.
Interactive System	System in which the user and computer engage in two-way communications; the user keys in data in response to prompts or inquiries from the computer until the desired task is completed.
Linking	Connecting or tying together.
Locality Of Reference	A concept in programming where once a location in memory is referenced, it will probably be referenced again in a short period of time; and once a location is referenced, a nearby location will also be referenced.
Logical Record	A group of related fields that are treated as a single unit.
Macro	A named routine that is called up for processing whenever the corresponding name is specified as part of a high-level instruction.
Macro ('Inner-layer' type)	A series of micro-instructions which, when executed, accomplish the purpose of the Macro ... equivalent to a machine instruction, IBM instruction, or Assembler instruction).
Macro ('outer-layer' type)	An instruction which, when executed, calls up a sequence of instructions (a subroutine) for execution, and then branches back to the original program.
Macroassembler	A computer having the capability to process defined macro's.
Macroinstruction	The name of a routine, prepared in Assembler language, that gets called up for execution whenever the name is used as part of a high-level instruction.
Menu	Generally, a list of available options displayed on the CRT when the system is turned on or after an operation has been completed.
Multiprogramming	The ability to process more than one program simultaneously.
Outboard Side	External to (away from) the CP.
Page	A 2K block of contiguous one-byte virtual-memory locations that begin at an address of zero, 2048, or multiple of 2048.

WORD/PHRASE	DEFINITION
Page Fault	An indication that a particular page is not in main memory.
Page Fault Exception	An error condition indicating that a page is invalid.
Page Frame	2K blocks of contiguous one-byte physical memory locations that begin at a physical (main) memory address of zero, 2048, or some multiple of 2048.
Page In	Read from disk into main memory.
Page Out	Write to the disk from main memory.
Page Table	An entry into Translation RAM containing the starting address of a physical page boundry.
Paging Task	That portion of the operating system that controls paging.
Print File	A disk file that is to be printed by a specific printer at the convenience of the Operating System and/or the System Console operator.
Print Queue	A collection of print file records pertaining to one or more printers (also, the sequence list identifying those records and the order in which they are to be printed).
Print Spooling	Temporarily storing print jobs on disk until a printer is available.
Procedure (Language)	A language used to create special text functions to perform operations normally executed interactively at a workstation.
Program Interrupt	A break in the normal sequence of instruction execution because of an error or request for assistance. The supervisory system seizes control to take action.
Prompt	The name of a message (usually one-line) directing the operator to perform some action.
Relocatability	Capability of a program to be initiated at any page frame and to randomly occupy any number of additional page frames as a consequence of a linkage of its subsequent parts by an address pointer.

WORD/PHRASE	DEFINITION
Segment	A block of contiguous one-byte virtual-memory locations, with the block beginning on a decimal-value virtual address of zero, 1,048,576, or some multiple of that value.
Segment Control Register	A CP register containing the page table virtual address and the page table length.
Sequential Filing	A technique which stores data records in the order in which they are written or entered.
Stack	Local RAM area used for temporary storage by the CP.
Swapped In	When an entire program is brought into main memory and allowed to run for a certain amount of time.
Swapped Out	When an entire program is replaced in main memory by another program which is allowed to run for a certain amount of time.
System Console	That workstation with access to special control or supervisor functions not available to other, "regular," workstations of the system.
Thrashing	The phenomenon of excessively moving pages back and forth between memory and secondary storage" (particularly because of "removing a page from memory and then immediately needing it again due to a page fault re-referencing that page").
Type 1 Dialog	Interprocessor Communications dialog used by the VS100 to support I/O initiation and interupts.
Type 0 Dialog	Interprocessor Communications dialog used by the VS100 to support Bus Adapter initialization and diagnostics.
Virtual Address	An address of a location in virtual memory. This address contains a page location in memory and a location within that page.
Write-through Strategy	For Cache memory, when the CP writes to main memory the same word is also written to Cache to ensure that the Cache has been updated.

APPENDIX G

VS-RELATED CORPORATE PUBLICATIONS

APPENDIX G

VS-RELATED CORPORATE PUBLICATIONS

Refer to the following publications for more information concerning system programming and operation.

1. VS Release 5.00 SYSGEN Procedure (WLI # not available)-- VI.C.1
2. VS Executive Introduction, WLI #800-1105EI-01 -- VI.A.1
   Designed as a relatively non-technical introduction to VS system features. This manual includes an overview of the major software and hardware features of the VS system, including a discussion of the system approach to problem solving.
3. VS Processors Data Sheet, WLI #800-2105-02 -- VI.A.1
4. VS Peripherals Data Sheet, WLI #800-2102-05
5. VS System Software Data Sheet, WLI #800-2101-04
6. VS Principles of Operation, WLI #800-1100PO-03 -- VI.C.1
   Describes the VS machine architecture and data organization, with special attention given to instruction execution, interrupts, and I/O operation. This manual documents the general machine instruction set and special operating system assist instructions. It also discusses Control mode and describes the characteristics of all I/O device types, including workstations, printers, disk drives, and tape drives.
7. VS Programmer's Introduction, WLI #800-1101PI-04 -- VI.C.2
   Introduces and discusses basic concepts of the VS and interactive processing. Major topics discussed are the workstation and Command Processor, system access and LOGON procedures, file management hierarchy, and the system program library. This manual is intended as an introduction for VS programmers.
8. VS Operating System Services, WLI #800-1107OS-02 -- VI.C.1
   Designed for the programmer/analyst. This manual explains the VS operating system software and the system components, such as virtual memory, control blocks, and paging. System macroinstructions, supervisor calls, and the VS Data Management System are also discussed.
9. VS Operating System Services Pocket Guide, WLI #800-62040P-01 -- VI.C.1
   Designed as a reference for system macroinstructions, Control Mode commands, and Program Control, I/O, and Status Words. Intended for use by those familiar with VS Operating System Services manual.

10. VS Language Data Sheet, WLI #800-2201-05 -- VI.C.2
11. VS Assembler Language Reference Manual, WLI #800-1200AS-02 -- VI.C.2
    Discusses the instructions and functions of VS Assembler language. Contained in this manual is information about assembler, machine, macro, and conditional assembly instructions. Also included are discussions of the usage of the instructions for such purposes as addressing, program sectioning, and linking. Background information is supplied on such topics as coding conventions, language elements and structure, and the assembler/operating system relationship.
12. VS Assembler Language Pocket Guide, WLI #800-6203AP-01 -- VI.C.2
    Designed as a reference for machine instructions, VS assembler macro-language, and pseudo-instructions. This guide is for use by those familiar with the VS Assembler Language Reference Manual.
13. VS BASIC Language Reference Manual, WLI #800-1202BA-01 -- VI.C.2
    Designed as a reference guide for programmers experienced in Wang VS BASIC. This manual describes the structure and format of VS BASIC source files, data types and operations, program control, and input/output operations. The manual also contains a detailed summary of syntax for VS BASIC statements, with examples of usage.
14. 2200 to VS BASIC Conversion Guide, WLI #800-1207BC-01 -- VI.C.2
15. VS COBOL Language Reference Manual, WLI #800-1201CB-03 -- VI.C.2
    Designed as a reference guide for the VS COBOL programmer. This manual describes VS COBOL syntax rules; VS COBOL supports standard 1974 ANSI Level 1 nucleus features, with many Level 2 features and VS extensions for interactive processing.
16. VS COBOL Conversion Guide, WLI #800-1204CC-01 -- VI.C.2
    Intended as an aid for the programmer converting from IBM and other versions of ANSI-standard COBOL to Wang VS COBOL. The conversion process is discussed in terms of device compatibility, syntax requirements, data file considerations, control language, and possible logic changes. Syntactical differences between IBM COBOL and VS COBOL are also discussed.
17. VS COBOL Pocket Guide, WLI #800-6200CP-02 -- VI.C.2
    Designed as a reference for VS COBOL syntax, reserved words, and workstation FAC values. Hexadecimal to decimal and EBCDIC to ASCII conversion charts are included. This guide is intended for use by those familiar with VS COBOL Language Reference Manual.

18. VS RPG II Language Reference Manual, WLI #800-1203RP-02 -- VI.C.2
    Designed as a reference for programmers preparing RPG II specifications for the VS system. This manual provides an introduction to RPG II implementation on the VS, with a discussion of workstation characteristics and RPG II program logic. The specifications for header, file description, extension, line counter, input, calculations, output, workstation, and alternate key coding sheets are included.
19. VS System 3/System 32 RPG II Conversion Guide, WLI #800-1206RC-02 -- VI.C.2
    This manual provides information concerning the conversion of source program and data files from IBM System 3 or System 32 installations to a Wang VS. It is intended for use in conjunction with the RPG II Conversion Aid Package. Topics include media conversions, equipment, system differences, and control languages.
20. VS Procedure Language Reference Manual, WLI #800-1205PL-01 -- VI.C.2
    Describes the syntax rules of the VS Procedure language, which is the executing command language of the VS system. This manual is intended as a reference guide for the user already familiar with the VS Programmer's Introduction.
21. VS Procedure Language Pocket Guide, WLI #800-6201PP-02 -- VI.C.2
    Designed as a reference for the user already familiar with the VS Procedure language. This guide includes the syntax for all Procedure language verbs, with a definition of syntax terminology and notation.
22. VS/WP Integrated Information System Data Sheet, WLI #800-2104-02
23. VS/WP Integrated Information System, WLI #800-2103-04
24. VS/WP Integrated Information System Addendum, WLI #800-2103.01
25. VS/IIS Operators Guide, WLI #800-1109WO-01
    Provides instructions for the Word Processing software available on the Wang VS. Included in this manual is introductory information, a description of the keys and functions needed to create and edit most Word Processing documents, the various print functions, and how to file and retrieve documents. Also included are error messages, sample exercises, and helpful hints.
26. VS/IIS Supervisor Procedures Guide, WLI #800-1110
27. VS/WP Introducing Word Processing on the VS, WLI #800-1407IW-02
    This manual introduces Word Processing operators and supervisors to WP on the VS, describes the basic VS hardware, and explains how to access

Word Processing from a VS workstation. A brief introduction to Data Processing on the VS is also included.

28. VS Programmers Guide to VS/WP, WLI #800-1304PW-02
    Details the current Data Processing interfaces to the VS Word Processing System. This guide discusses Word Processing document structure on the VS, documents the COPYWP conversion and archiving utility, and describes the use of the document handling subroutines for VS Word Processing document manipulation by Assembler, BASIC, or COBOL programs. A familiarity with the VS system is assumed.
29. VS Word Processing Operator's Guide, WLI #800-1109WO-01
    This manual provides Word Processing instructions for both new and accomplished users of the Word Processing software available on the VS systems. It is designed for operator/system interaction in a step-by-step format. The reader will learn how to perform Word Processing on the VS by actually utilizing the WP capabilities.
30. VS Data Base Management System Data Sheet, WLI #800-2106-01
31. VS KEYENTRY Data Sheet, WLI #800-2300-01
32. VS File Management Utilities, WLI #800-1300FM-02 -- VI.C.4
    Describes the three File Management Utilities (Control, DATENTRY, and Report) used to create and maintain data files, and generate customized reports from the file.
33. VS Utilities Reference Manual, WLI #800-1303UT-02 -- VI.C.4
    Designed as a guide for both programmers and non-programmers to the interactive use of the system utilities. This manual includes the File Management utilities (used for creating, maintaining, and supporting data files) and the general System utilities (used by programmers to perform support and maintenance program development, maintenance and testing, and other functions).
34. VS User Aids Reference Manual, WLI #800-1301UA-01 -- VI.C.4
    Describes the VS User Aids distributed by the International Society of Wang Users. These programs are not provided with the operating system, and are not supported in the same manner as utilities. The subroutines and aids described in this manual are designed to enhance the versatility of the BASIC and COBOL languages on the VS.
35. VS Data Communications Data Sheet, WLI #800-2107-02 -- VI.C.4
36. VS Data Communications User's Guide, WLI #800-1302DC-02 -- VI.C.4
    Provides operating instructions and procedure writing information for

2780/3780 batch communications using the TCCOPY program. Also describes VS-to-VS communications using the VSCOPY program.

37. VS Mailway Data Sheet, WLI #800-2108-01 -- VI.C.4
38. VS System Operation Guide, WLI #800-1102SO-05 -- VI.C.1
    Designed for use by operations personnel. This guide explains the system functions accessible from the Operator's Console, including printer allocation and control of the print queue, control of the job queue, and the role of the Operator's Console in Control mode. Also covered in this manual are operational characteristics of peripherals (printers, disk drives, and tape drives), and device specifications.
39. VS System Management Guide, WLI #800-1104SM-03 -- VI.C.1
    Designed for use by system security administrators. This guide discusses the VS file protection and security system, along with the BACKUP utility and SYSGEN operations. File protection classes, a system user list, special privilege program files, LOGON procedure, and BACKUP execution are also among the topics discussed.

APPENDIX H

BASIC SOFTWARE CONCEPTS AND TERMINOLOGY

APPENDIX H
BASIC SOFTWARE CONCEPTS AND TERMINOLOGY

Any machine using high-level programming languages (BASIC, COBOL, RPGII, FORTRAN, etc.) cannot directly execute any statement written in that language. Each such statement must first be transformed, by some means, into a series of executable machine language instructions. High-level programming languages in the VS-100 are compiled rather than interpreted.

1. COMPILERS

In a compiler system, a program is first entered in one of the available high-level languages (COBOL, BASIC, RGPII, PL/1, or FORTRAN in the VS-100) by interacting with a 'Text Editor' program. Entering text via the 'Text Editor' program is very similar to typing text into a word processing machine. The programmer may enter anything he wants, making modifications as desired during or after that entry process. The Text Editor program causes the machine to blindly accept this program text, letting the user edit his text on entry and giving no indication of programming errors. This initial-entry data of high-level user program text, which cannot be executed by the computer in this initial form, is called the source program (or, alternatively, source code, or source text or source module).

After text has been entered and edited as desired, another function of the Text Editor program stores this source program on disk. Once on disk, the source program becomes known as a source file (still not machine executable).

Once the source file has been created, the programmer loads a compiler program, which is written in machine language. The compiler program uses the source file as input to produce a compiled version of the user's program in machine language, called the object program or object code. The compiler program then creates an object file or program file on disk, and then generates a printout of source code, object code, syntax errors, and other relevant information for the programmer's use. Bear in mind that the computer can execute only this object or program file--and that the computer cannot execute the operator-input source code.

In a compiler system such as the VS-100 system, therefore, two versions of each program are produced: the source program, written in a high-level language; and the object program, consisting of machine language statements and produced by a compiler.

To execute the object program, the object file must be loaded and run. Execution errors will show up at this time. The VS-100 system produces its error messages in plain English, rather than in number codes. When an error is encountered, the user program goes into a debug mode. Machine code, memory, and registers may be examined and changed. The program can be stepped, rerun, or cancelled.

Since all programming languages ultimately compile to the same machine code, a VS-100 program may have different portions written in different languages. It is not unusual, for example, to write a machine-code routine for something that is not convenient in a high-level language. The various pieces then are put together by a system program called the "Linkage Editor" program, which works with the object files.

In a compiler system, a programmer will be more efficient if he makes flow charts and 'desk checks' his code in advance. This approach slows down the coding process but significantly speeds up the overall run-time period, because the prechecked program will work successfully that much sonner.

2 INTERPRETERS

An interpretive system, in contrast to a compiler system, uses an interpreter program, which translates high-level source-code program statements as they are encountered during execution, converting them directly into individual sets of executable machine instructions. An interpreter program thus does not have to generate the object code for each source statement and then save that object code for later execution. The major disadvantage of an interpretive system is speed: an interpreter program may generate results 10 to 20 times slower than the equivalent compiled code. In an interpretive system, for example, a statement describing a 1,000-pass loop must be retranslated and executed for each of the 1,000 passes in that loop.

In a compiler system, conversely, the loop would be translated to the equivalent machine code just once, rather than 1,000 separate times; its stored machine code (the object program) would produce the same end result, but the system can execute the previously-complied code much faster. (The interpretive system does have its own advantages, of course, in that the executing program being interpreted can be interrupted, changed, and/or resumed much more easily.)

3 ASSEMBLERS

An assembler program, also known as an assembly routine or an assembly program, or even simply as the assembler, is a program designed to convert a set of non-executable symbolic (mnemonic) instructions directly into executable machine language instructions. Assembler language therefore permits a programmer to write machine-level instructions. Each assembler symbolic instruction has a one-to-one correspondence to a machine language instruction. Figures A and B for example, show a typical assembly language source program for a Wang Model 700 calculator. Notice in these figures the one-to-one relationship between the assembly language steps and the resulting machine code. This relationship is a distinctive hallmark of an assembler as opposed to a compiler function, which may produce several machine code instructions from a single high-level instruction.

STEP NUMBER	MNEMONIC INSTRUCTION
1	1
2	UP
3	WR AL
4	CR/LF
5	END AL

A. "Representative" Source Code for a Specific Operation

STEP NUMBER	MNEMONIC INSTRUCTION
1	0701
2	0604
3	0412
4	0108
5	0413

B. "Representative" Object Code for the Same Operation

Since the instruction set of a machine defines the complete set of elementary capabilities provided by the machine, Assembler language provides the programmer with access to the machine's total repertoire of functions.

The VS-100 Assembler also allows a programmer to define a routine consisting of a series of instructions, and to assign a name to that routine. The name can then be specified (instead of the entire routine) as a single instruction in a program. Such named routines are called macros, and the names assigned to them are called macro-instructions. Because the VS-100 Assembler permits the definition of macros, it is also referred to as a macroassembler.

Programmer-created macroinstructions are used to simplify the writing of a program and to ensure that a standard sequence of instructions is used to accomplish a desired function. For instance, the logic of a program may require the same instruction sequence to be executed again and again. Rather than code this entire sequence each time it is needed, the programmer creates a macroinstruction to represent the sequence and then, each time the sequence is needed, the programmer simply codes the macroinstruction statement. During assembly, the sequence of instructions represented by the macroinstruction is inserted in the object program.

The Assembler program language also contains mnemonic operation codes to specify auxiliary functions performed by the assembler. These are instructions to the assembler program, and in most cases do not themselves result in the generation of machine-language object code by the assembler program. Again, it is important to note that the VS-100 machine instruction set contains all instructions available on the IBM 360, as well as most available on the IBM 370.

Macro-instructions used in preparing an assembler language source program fall into two categories. The first consists of system macro-instructions, provided by Wang, which relate the object program to components of the OS. All Wang system macros belong to the library '@MACLIB@'; Table 1 lists the currently available system macros. The second category consists of programmer-created macros, developed by a user specifically for use in an application program at hand, or for incorporation in a library for future use.

Table 1 VS-100 System Macros Stored in the @MACLIB@ Library

AIR	FREEMEM	REWRITE
ALEX	GETBUF	RMSG
AXD1	GETMEM	SCRATCH
AXDGEN	GETPARM	SEND
BCE	IORE	SETIME
BCTBL	KEYLIST	START
BCTGEN	LINK	STMB
CALL	LNKB	SVCE
CANCEL	LOW	SVCT
CHECK	MCB	SYSCODE
CLOSE	MSGLIST	TCB
CMSG	OFB	TIME
CREATE	OPEN	TPLAB
DBTB	PATCH	TPLB2
DELETE	PCEXIT	TQEL
DESTROY	PFB	TS
DPT	PFSA	UCB
ETCB	PFT	UFB
EXTRACT	PFTX	UFB2
FDAV	PT	UFBGEN
FDR1	PUTPARM	VCB
FDR2	PXE	VOL1
FDX1	READ	WAIT
FDX2	REGS	WRITE
FLUB	RENAME	XIO
FMSG	RESETIME	XMBUF
FMILIST	RETURN	XMIT
FREEBUF		

OPERATING SYSTEM CAPABILITIES

The Operating System (OS) is an integrated group of service routines that collectively supervise the sequencing and processing of all programs, including the user-application software. The OS performs input/output operations, machine accounting tasks, compilation and storage assignment, program debugging, etc. This collection of routines receives and responds appropriately to all inputs, including operator/peripheral inputs and status conditon signals both from peripheral devices and from the mainframe circuits themselves. The OS then effectively makes decisions for each such input based on a retained record of assigned tasks and concurrent hardware conditions. The OS thus is the the entity that runs the machine and gives it its functional capabilities and "personality."

1. INTERACTIVE OPERATION

Like all previous 2200 and VS systems, the VS-100 is interactive, allowing users to communicate directly with the system from respective workstations. The system requests user-specified data and provides useful information in a series of clear, nontechnical prompts displayed on the workstation screen. Such prompts may ask the user to "fill in the blanks" with requested data, or to select a desired item from a number of displayed options, or simply to press a certain key to confirm a specific intention.

Most computer systems require the use of a complex special language for issuing instructions to the system and for controlling system functions. The VS-100 system, however, requires no special language inputs. Instead, all system functions are invoked through selections/confirmations entered under the control of a special program called the Command Processor. The user simply chooses the desired function from a displayed menu, and then responds to any subsequent prompt messages asking for information pertaining to that function. If the user response is erroneous or insufficient, the system generally returns an error message which identifies the problem--and, in many cases, suggests a possible solution.

To run a program on the VS-100, the user simply loads the program, chooses the RUN PROGRAM function from the Command Processor menu, and then types in

the program name, disk library, and volume in which it is located. When this information is entered, the user keys ENTER to begin program execution.

At any point during the execution of a program, a user can interrupt the program by pressing the HELP key, which temporarily halts program execution without destroying any critical information or closing any files. The program can be resumed from the point of interruption simply by pressing the PF key associated with the CONTINUE command. While a program is interrupted, however, the user has access to all system functions. He can, for example, examine the status of open files or I/O devices, scratch or rename files, or begin debug processing. Once these functions are completed, normal execution of the interrupted program can be continued.

2. MULTIPLE-USER OPERATION

The VS-100 is projected to support up to 128 individual workstations simultaneously. Each such workstation can be running its own job, independent of the others. Since each "job" is actually a separate program, such a system is often referred to as a multiprogramming system. Since there is only one cen- tral processor and one memory, of course, two or more programs actually cannot be executing at exactly the same instant, but each user generally is undis- turbed by other users, and no-one has to wait for access time. All programs on the VS-100 system share a common set of resources. Each program (or some portion of it) is kept in its own location(s) in memory. The central process- or permits each program to run for a short period of time, and then interrupts that program, permitting another program to run for a similar brief period. This process continues indefinitely, or until all programs terminate. Because the central processor is fast and is managed efficiently, each user's program appears to run without interruption, simultaneously with all other programs.

The key to the success of such a scheme is the OS software, which must manage the use of common resources--including the central processor, memory, and I/O devices--with maximum efficiency. The VS-100 OS is designed for such efficiency; it is designed to guarantee that each user will have reasonable response time for his program, while ensuring that each program runs without interference from others. Each user can proceed exactly as if he had access

to his own private system. This process of sharing a single computer among many users is called distributed processing.

The VS-100 OS imposes no special restrictions on the types of jobs which can be run concurrently from each workstation. It is not un- likely, for example, that an installation might have two or more workstations running a large data entry application, while other workstations are simul- taneously running an order-entry program, and still other workstations are being used by programmers for program development. Such a system obviously provides great flexibility for the user, who is not forced to purchase several different systems to perform different jobs.

One workstation is designated as the System Console. In addition to running normal programs, the System Console provides a second mode of operation in which it can control a number of special system features not accessible from regular workstations. Such special features include print spooling and background processing (both of which are explained in detail further on in this discussion).

3. MULTILINGUAL SYSTEM

As in the VS-60 and VS-80 systems, the VS-100 supports (with respective compilers) multiple high-level languages, including ANSI COBOL, BASIC, FORTRAN, PL/1, and RPG II, as well as Assembler language and an English-like command language called PROCEDURE.

COBOL, (Common Business Oriented Language), is one of the most popular programming languages in use today for commercial data processing (DP) applications. COBOL programs are based on and read much like ordinary business English, but the language provides an array of powerful record formatting, data manipulation, and file handling capabilities particularly important for DP applications. In part, COBOL's popularity also derives from the fact that it is the only major language subject to an industry-wide standard, administered by the American National Standards Institute (ANSI).

For the programmer who wishes to obtain a greater degree of control over the system and to write more efficient programs, the VS-100 system also

provides an Assembler language. Since the instruction set of a machine defines the complete set of elementary capabilities provided by the machine, Assembler language provides the programmer with access to the machine's total repertoire of functions.

The VS-100 Assembler language also allows a programmer to define a routine consisting of a series of instructions and to assign a name to that routine. That name (rather than the entire routine) can then be specified as a single instruction in a program. Such named routines are called macros, and the names assigned to them are called macro-instructions. Because the VS-100 Assembler permits the definition of macros, it is also referred to as a macroassembler.

The VS-100 machine instruction set contains all instructions available on the IBM 360, along with most of the instructions that are available on the 370. Programmers familiar with IBM 360/370 Assember Language consequently find VS-100 Assembler either familiar or easy to learn.

The VS-100 Procedure language allows users to create special text files which perform many of the operations normally executed interactively by the user at a workstation. Some typical procedures of this nature include running two or more programs sequentially, supplying run-time parameters to a program, and scratching or renaming programs. The use of such procedures can reduce the number of keystrokes and interactions required of a user who is running a program.

4. FILE MANAGEMENT UTILITIES

To support applications with large on-line data base requirements, the VS-100 system supports extensive on-line data storage capacity. This support covers 30-MB/60-MB/90-MB 2280V-Series Disk Drive units and 75-MB/288-MB 2265V-Series Disk Drive units, handling up to 4608 megabytes of on-line storage.

The VS-100 Data Management System provides a comprehensive disk file access and maintenance capability. Two types of files are supported on the system: sequential files, in which records are stored in the order in which

they are written, and indexed files, in which records are stored in the order of their key values. In both types of files, records may be accessed either sequentially or randomly. A third technique, called dynamic access mode, permits a program to switch back and forth between sequential and random access on the same data file.

The indexed file system permits multiple indexes for a single file. This feature enables a record to be accessed on different keys for different purposes. An employee record, for example, may be accessed by employee name for personnel purposes and by employee number for payroll purposes.

A single file can be shared among several different users. Consequently, several users may perform updates and/or inquiry operations on a common file concurrently. In data entry applications, for example, all operators can directly update a single master file. The additional steps of creating temporary files for all operators, and then merging them together are therefore eliminated. The Data Management System is discussed in detail in the VS Operating System Services Manual (WL# 800-11070S-02 -- VI.C.1).

5. DATA ENTRY/FILE MAINTENANCE

The VS-100 system software includes a package of three programs designed to facilitate the creation and maintenance of data files, as well as the creation of reports based on such files. A Setup Utility program permits the user to define a data file by specifying the types of data in each record of the file, and to design the screen display used to prompt an operator for information to be entered for each record. A Data Entry program can then be used to solicit operator input by displaying the defined prompt messages and accepting and/or validating entered data. Finally, a Report Utility program, intended for use by management as well as programmers, provides great flexibility in the design of custom reports which present information from a data file in a useful and coherent format.

6. INTERACTIVE TEXT EDITING

An interactive Text Editor program greatly facilitates software development on the VS-100 system. The Text Editor program lets a programmer

create and modify program files interactively, using any one of the supported languages. Entering program text is as easy as typing it into the display, and editing an existing program is equally simple because of a large number of provided editing functions. Interactive program development permits programmers to work with maximum productivity in the development and maintenance of programs.

7. INTERACTIVE DEBUG FACILITY

In many cases, the process of identifying and correcting bugs in a program is more time-consuming than the writing process itself. To assist the programmer in this task, the VS-100 system supports an easy-to-use, interactive debugging facility.

The VS Debug Processor program not only permits inspection of program code but also permits inspection and modification of data by memory address. In addition, the program provides an easy-to-use "symbolic" debugging feature that displays sections of source code in a "program window" on the workstation screen, and permits data values to be examined and modified by symbolic data name rather than by address. The VS Debug Processor also includes facilities for examining and modifying internal registers and the Program Control Word. Breakpoints can be set in a program, and another feature allows the user to manually step through program execution.

8. MAJOR PERFORMANCE FEATURES

The VS-100 system provides a diversity of features designed to increase total throughput and to improve system performance, in addition to those features that have already been mentioned. These additional features include automatic program sharing, independent I/O processors, automatic data compaction, automatic print spooling, and background processing.

A. AUTOMATIC PROGRAM SHARING

When two or more users are running the same program at the same time, it would be wasteful to keep a separate copy of the program in memory for each user. To avoid such duplication, the VS-100 system automatically

causes several users to share the same copy of a program in memory whenever possible. The amount of memory saved by this feature can be substantial when, for example, a number of users are running a large data entry program, or several programmers are compiling COBOL programs. Program sharing also improves performance for all users by reducing the total number of pages which must be transferred in and out of memory.

B. INDEPENDENT I/O PROCESSORS (IOP'S)

Most commercial-application programs spend a good deal of time performing input/output (I/O) operations, such as reading and writing disk files, or sending output to a printer. The VS-100 System handles such I/O operations by independent I/O processors (IOP's), which control the transfer of data between Mainframe memory and the various I/O devices associated with respective IOP's. When any program requests an I/O operation, the central processor notifies the appropriate IOP, supplies it with any necessary information, and then turns its attention to other processing tasks while the I/O operation is carried out. Because the disk and tape IOPs can transfer information directly to or from memory via Direct Memory Access (DMA) techniques without central processor involvement, the central processor is able to perform internal processing concurrently with certain I/O operations. This overlap of I/O processing and internal processing guarantees that maximum use is made of the central processor, and increases overall system throughput.

C. AUTOMATIC DATA COMPACTION

To conserve disk storage and hasten data transfer, the system provides an option to compress data records automatically before storing them on disk. In the compaction process, characters which are repeated three or more times in sequence are stored as a single character and a repetition count. Data compaction is performed automatically on all print files, and is performed on a data file if the "compressed records" option is specified when the file is created. Compressed records are automatically expanded to their original format by the system when they are read back into memory, making the entire compaction process completely transparent to the user. Data compaction can reduce the disk storage requirements of

many files up to 50% and contributes to improved performance by reducing the total number of characters which must be transferred between disk and memory for each record access.

D. AUTOMATIC PRINT SPOOLING

Print spooling, a function of the Data Management System, is a technique by which a job scheduled for printing is temporarily stored in a disk file rather than being sent directly to the printer. The Print Files thus created on disk are placed in a print queue under the control of the System Console. When a printer becomes available, each job is then printed in the order determined by the print queue. Print spooling offers two significant benefits: it frees individual workstations from dependence upon printer availability, and it enables the printers to be scheduled efficiently.

E. BACKGROUND PROCESSING

Background processing is the automatic execution of batched lower-priority programs whenever there are no higher-priority programs being handled by the OS. Although the VS-100 system is designed primarily for interactive operation, it also supports the running of jobs which require large amounts of processor or I/O time, with a minimum amount of operator interaction, on a "background" basis. Background jobs can be run in a batch from any workstation. While a background job is running at a workstations, all other workstations remain available for interactive use.

APPENDIX I

VS-100 UPDATES

APPENDIX I

This appendix contains updated information concerning the new 210-7803 Main Memory and 210-7911 Bus Adapter cards.

As the old 210-7603 Main Memory and 210-7611 Bus Adapter cards are still supported, the sections of the VS-100 manual referencing these cards are still valid.

1. GENERAL

This appendix will describe the upgrades in the VS-100 to increase Main Memory size and allow more disk drive I/O Processors (IOPs) to be installed in the system. Also included is card installation information, diagnostic information, updated theory of operation, and updated "A" and B" level RSLs.

The upgrades are directed at three cards (Figure I-1), as follows:

a. 210-7603 Main Memory card -- Now designated as 210-7803 using 64K RAM chips instead of 16K RAM chips.
b. 210-7604 Cache card -- Now designated as 210-7604-1A with changes to the Main Memory refresh timing to accomodate the 64K RAM chips on the Main Memory card.
c. 210-7611 Bus Adapter Card -- Now designated as 210-7911 with timing changes to allow an increase from one 212-3023 disk IOP per Bus Adapter (BA) to two 212-3023 disk IOPs per BA.

There are two Engineering Change Orders (ECOs) already being implemented in the field to support the 210-7911 BA upgrade, as follows:

a. ECO #20204 -- This ECO decreases the clock pulse width on the 210-7905 System Bus Controller (SBC) card from 80 nanoseconds to 40 nanoseconds. The BA is synchronized with the SBC clock and this decreased clock pulse width will allow the 210-7911 BA to handle the two disk IOPs.
b. ECO #20205 -- This ECO allows the 210-7611 BA to accept the decreased clock pulse width, received from the 210-7905 SBC, that is required by the 210-7911 BA.

2. MAIN MEMORY DESCRIPTION

The VS-100 can contain from two to eight 210-7803 Main Memory cards. Memory can range in size from 1 Mbytes (two cards) to a maximum of 8 Mbytes (eight cards) with memory size increasing in 512-Kbyte increments through the use of half-loaded cards. Each Main Memory card can contain a maximum of 1

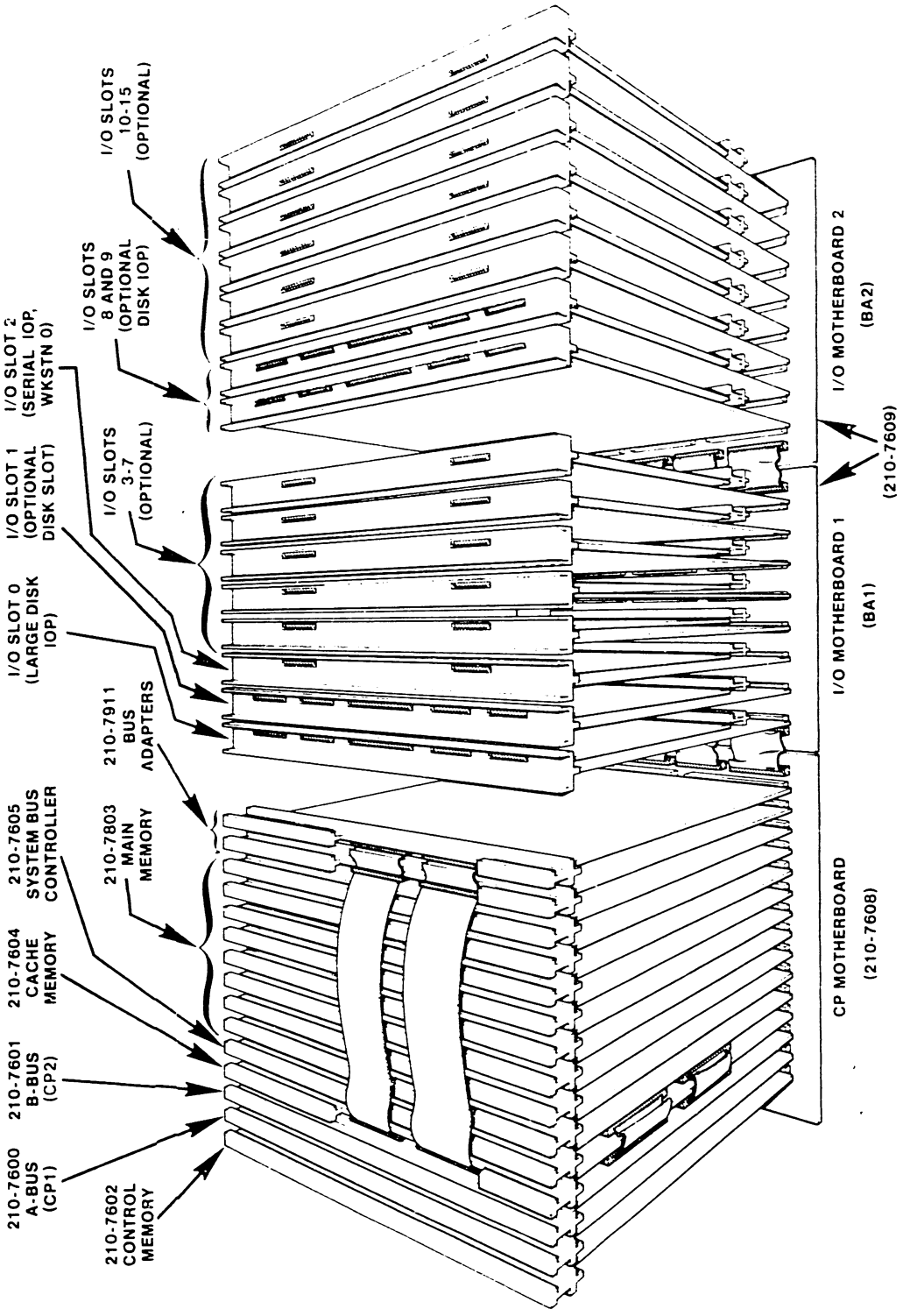


FIGURE I-1. CPU AND I/O MOTHERBOARDS WITH FULL COMPLEMENTS OF CIRCUIT CARDS

megabytes of data. Memory cards are loaded into the VS-100 in pairs to accomodate the 64-bit data path employed in memory operations.

The three most common versions of the 210-7803 Main Memory card are as follows:

PART NUMBER	MEMORY SIZE
210-7803-1A	256 Kbytes
210-7803-2A	512 Kbytes
210-7803-4A	1024 Kbytes

3. CACHE DESCRIPTION

The 210-7604-1A Cache Random Access Memory provides high speed data read access for the CP by acting as a buffer between the CP and Main Memory. Its main function is to improve memory transfer rate by providing high speed access to needed data. Two other sections of the Cache card, although not part of the Cache Memory, are the Main Memory control and the IPC (Interprocessor Communications) control logic. Main Memory refresh logic is also part of the memory control to provide refresh control and refresh row addresses to the Main Memory.

4. BUS ADAPTER DESCRIPTION

The 210-7911 BA is the interface between the VS-100 CPU and up to eight IOPs and attached peripheral devices. The BA also provides data buffering and routing between the 16-bit IOP data path and the 64-bit Main Memory (MM) data path. Because the IOPs use a 16-bit path and MM uses a 64-bit path, the BA must put data going from the IOP to MM into 64-bit blocks for transfer to MM. It must also perform the reverse function on data going from MM to an IOP. With the 210-7911 BA, two disk IOPs can now be installed on the associated I/O motherboard. A maximum of two BAs can be installed on the VS-100, allowing the CPU to interface with a maximum of 16 IOPs.

5. REMOVAL OF MAIN MEMORY, CACHE, AND BUS ADAPTER CARDS

Refer to Chapter 7, Removal/Replacement Procedures, of the VS-100 manual for removal information for other Mainframe circuit cards.

A. Power down the Mainframe and place the circuit breaker in the OFF position.

B. Remove the two 60-pin connectors from the top edge of the 7604 Cache Memory card (Figure I-2) that attach to the 7611 BA card(s) (Figure I-3). Remove the two 64-pin connectors that attach to the 7605 SBC card (Figure I-4) from the right edge of the 7604 Cache Memory card. Remove the 16-pin ribbon cable from L46 of the 210-7604 Cache Memory card to L83 of the 210-7605 SBC card. Remove the Cache card by grasping the top corners and gently rocking it from side-to-side while exerting a steady upward pressure. Once the card is free of the slot, ease it up and out of the Mainframe.

C. Remove the 7603 Main Memory card (Figure I-5) in the same manner as the previous card.

D. Remove the two 60-pin connectors from the top edge of the 7611 BA card that attach to the 7604 Cache Card. Remove the two 60-pin connectors that attach to the BA from the right edge of the 7605 SBC card. Remove the BA in the same manner as the previous cards. (There may be two BAs, depending on the number of IOP cards installed.)

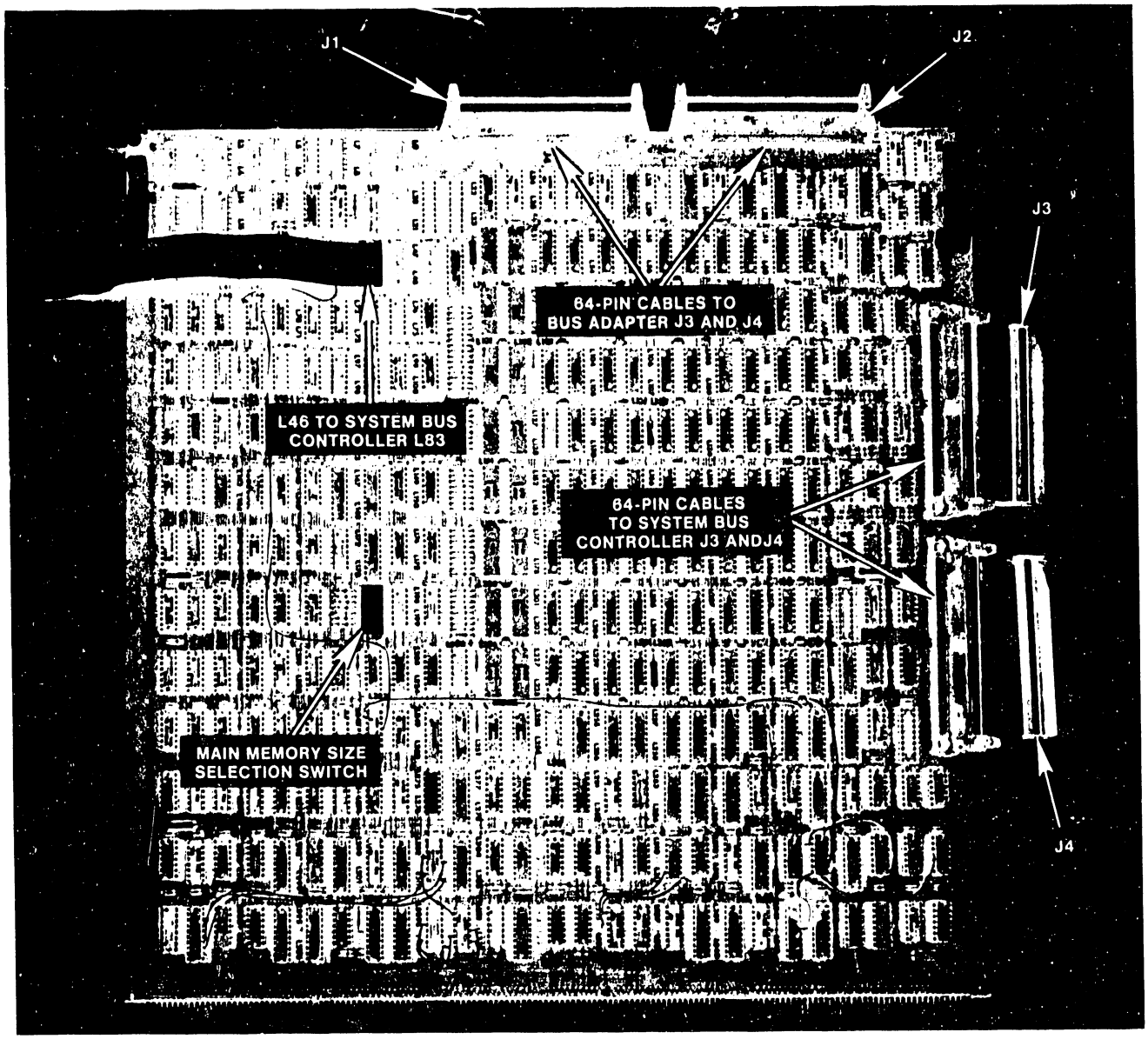


FIGURE I-2. 210-7604 CACHE MEMORY CARD
WITH CONNECTOR LOCATIONS

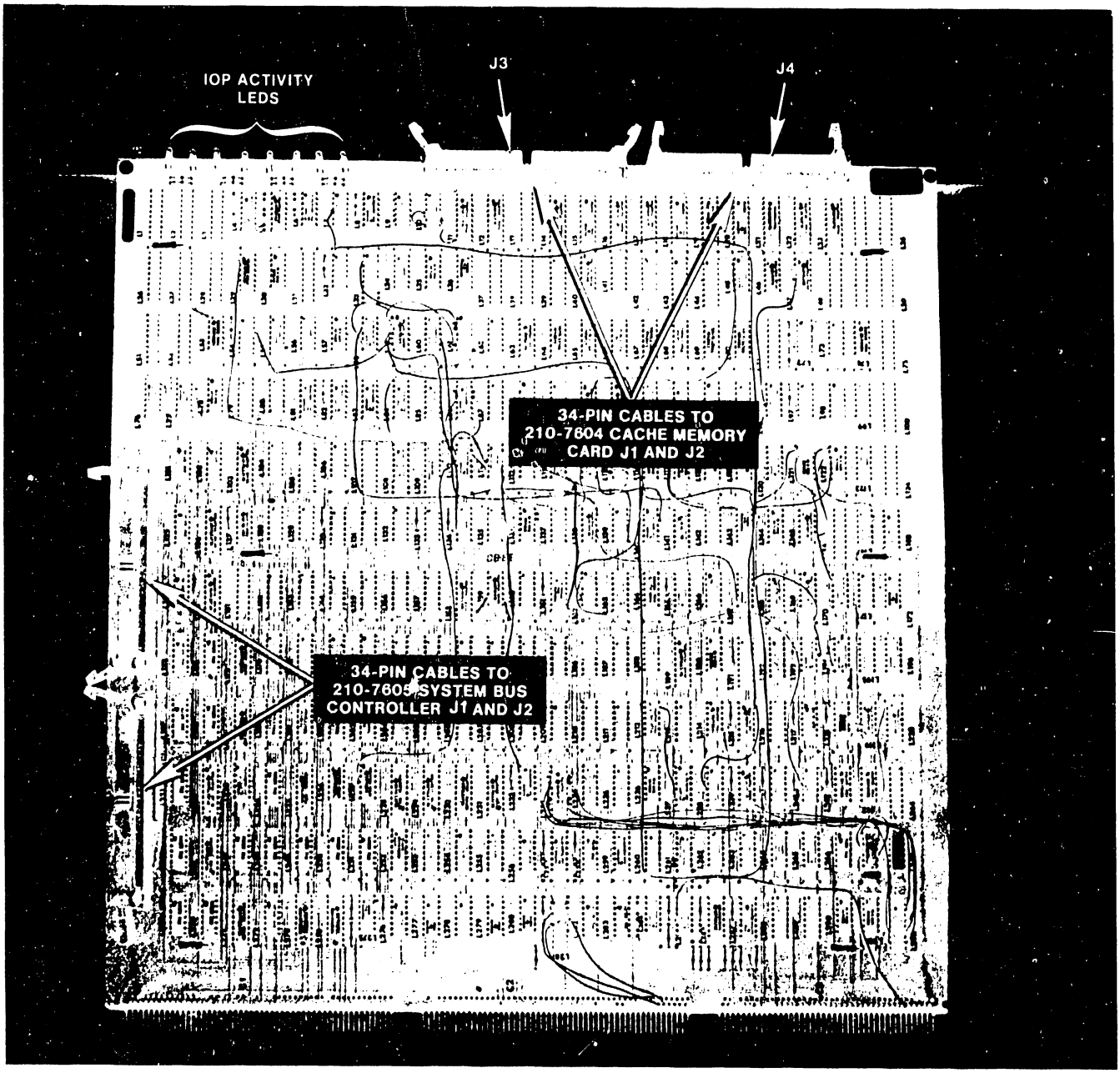


FIGURE I-3. 210-7911 BUS ADAPTER CARD
WITH CONNECTOR LOCATIONS

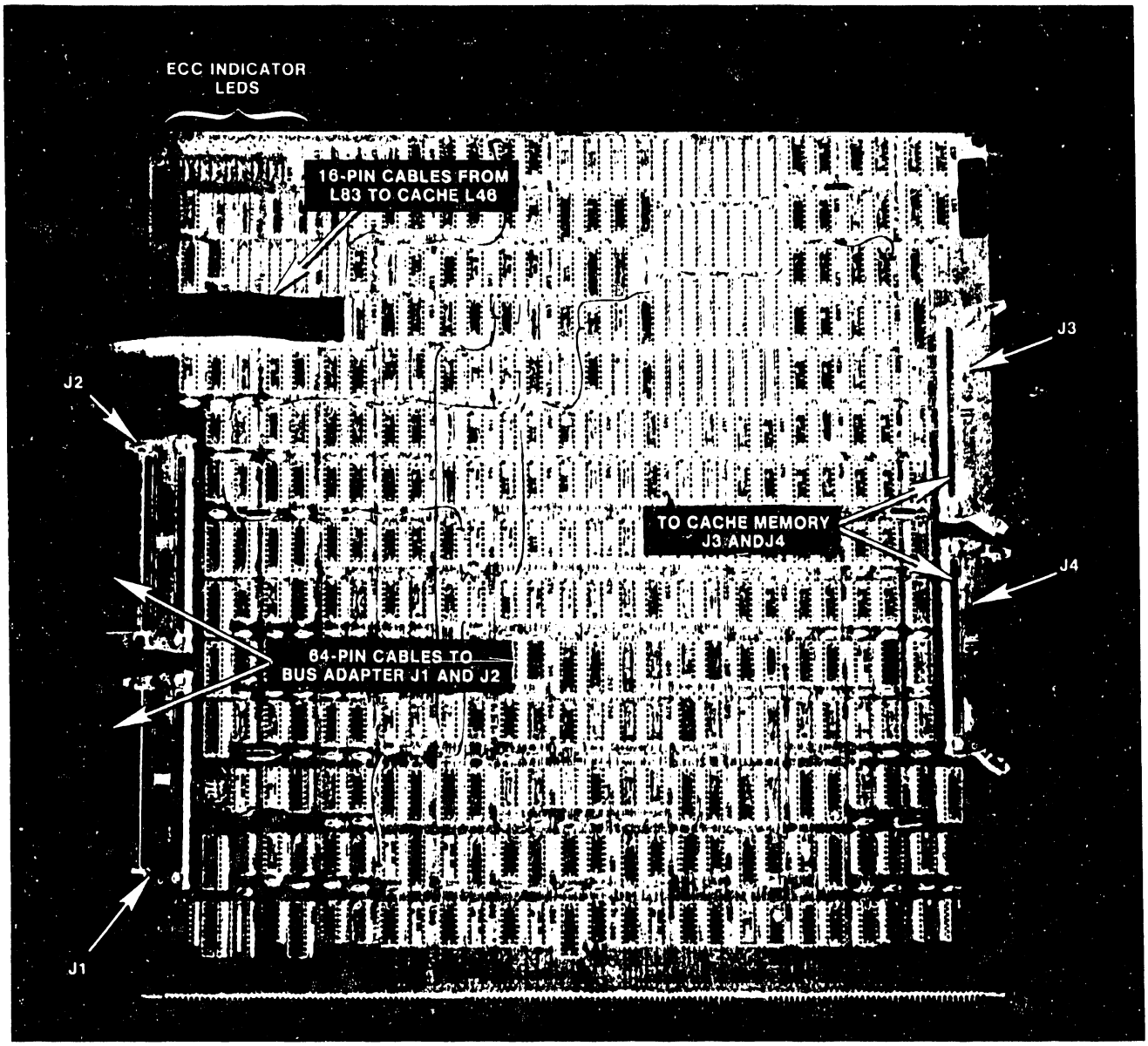


FIGURE 1-4. 210-7605 SYSTEM BUS CONTROLLER CARD WITH CONNECTOR LOCATIONS

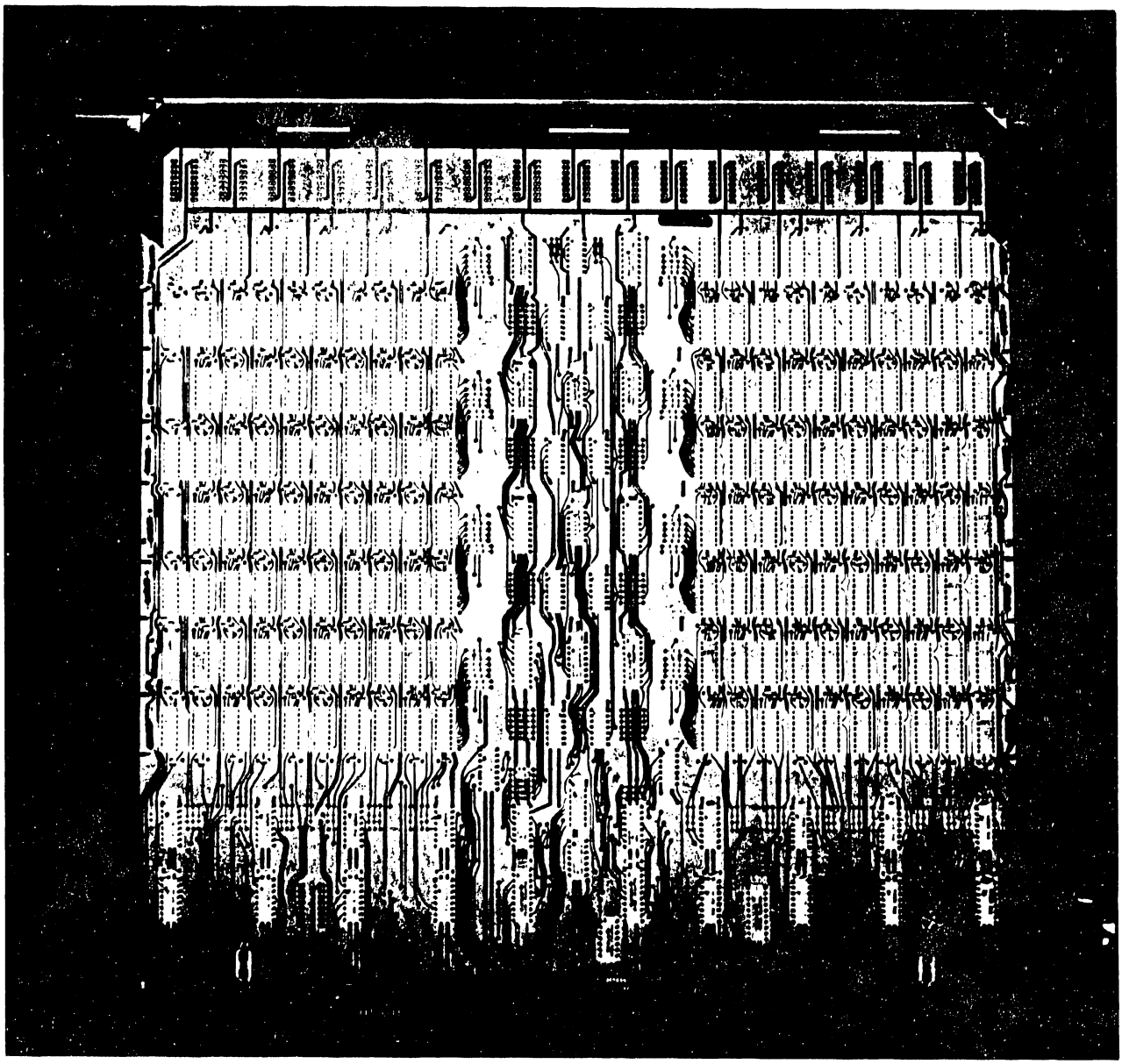


FIGURE I-5. 210-7803 MAIN MEMORY CARD

6. INSTALLATION OF MAIN MEMORY, CACHE, AND BUS ADAPTER CARDS

Refer to Chapter 3, Unpacking and Installation, of the VS-100 manual for installation information for other Mainframe circuit cards.

Listed below is the new serial tag information for 60 cps ac line frequency machines. The serial tag number prefix for 50 cps ac line frequency machines is 157.

MODEL NUMBER	SERIAL TAG #	MEMORY SIZE (Bytes)
VS-16F	177-7111	0.512 Meg
VS-32F	177-7113	1.024 Meg
VS-64F	177-7117	2.048 Meg
VS-96F	177-7142	3.072 Meg
VS-128F	177-7143	4.096 Meg
VS-160F	177-7144	5.120 Meg
VS-192F	177-7145	6.144 Meg
VS-224F	177-7146	7.168 Meg
VS-256F	177-7147	8.192 Meg

*****NOTE*****

NEW 210-7803 MAIN MEMORY CARDS CANNOT BE INTERMIXED WITH OLD 210-7603 MAIN MEMORY CARDS. ALSO, NEW 210-7604-1A CACHE CARDS CANNOT BE USED WITH OLD 210-7603 MAIN MEMORY CARDS AND OLD 210-7604 CACHE CARDS CANNOT BE USED WITH NEW 210-7803 MAIN MEMORY CARDS.

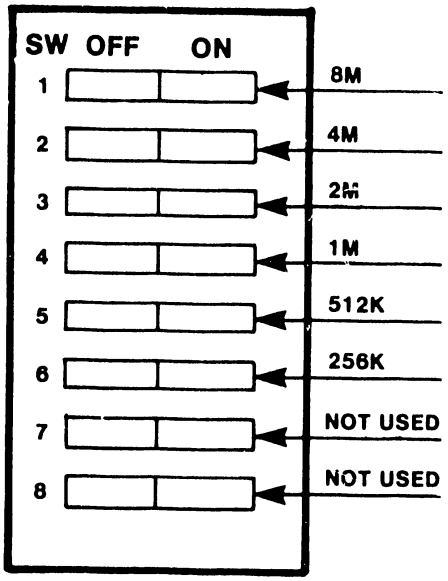
A. After checking memory-size switch settings on the Cache Memory card (Figure I-6), connect the 16-pin ribbon cable from L46 of the 210-7604-1A Cache Memory card to L83 of the 210-7605 SBC card.

B. Install the 210-7604-1A Cache Memory card in Motherboard slot #4.

C. Install the 210-7803 Main Memory cards in <u>pairs</u> starting at Motherboard slot numbers 6 and 7. Cards in even-numbered slots (6, 8, 10, 12) contain even data words; cards in odd-numbered slots (7, 9, 11, 13) contain odd data words. The total number of PAIRED memory

SW. NO	8	7	6	5	4	3	2	1	MEMORY SIZE IN BYTES
NOT USED			1	0	0	0	0	0	256K
			0	1	0	0	0	0	512K
			1	1	0	0	0	0	768K
			0	0	1	0	0	0	1M
			1	0	1	0	0	0	1.2M
			0	1	1	0	0	0	1.5M
			1	1	1	0	0	0	1.7M
			0	0	0	1	0	0	2M
			1	0	0	1	0	0	2.2M
			0	1	0	1	0	0	2.5M
			1	1	0	1	0	0	2.7M
			0	0	1	1	0	0	3M
			1	0	1	1	0	0	3.2M
			0	1	1	1	0	0	3.5M
			1	1	1	1	0	0	3.7M
			0	0	0	0	1	0	4M
			1	0	0	0	1	0	4.2M
			0	1	0	0	1	0	4.5M
			1	1	0	0	1	0	4.7M
			0	0	1	0	1	0	5M
			1	0	1	0	1	0	5.2M
			0	1	1	0	1	0	5.5M
			1	1	1	0	1	0	5.7M
			0	0	0	1	1	0	6M
			1	0	0	1	1	0	6.2M
			0	1	0	1	1	0	6.5M
			1	1	0	1	1	0	6.7M
			0	0	1	1	1	0	7M
			1	0	1	1	1	0	7.2M
			0	1	1	1	1	0	7.5M
			1	1	1	1	1	0	7.7M
			0	0	0	0	0	1	8M

OFF = 1
ON = 0



OFF = ACTIVE

FIGURE I-6. VS-100 MAIN MEMORY SWITCH SETTINGS
LOCATED ON THE 210-7604 CACHE CARD

cards determines Main Memory size (refer to Table I-1). Ensure that the number of memory cards equals desired memory size (refer to work request). Do NOT leave open slots between memory cards.

D. Install a 210-7911 BA card in Motherboard slot #15: the card in this slot becomes BA #1. If the system contains a second BA card, install it in Motherboard slot #14: the card in this slot becomes BA #2.

E. Make sure that all cables running to the cards are reinstalled in the correct locations (refer to Table I-2) and all cards are firmly seated in place.

TABLE I-1. MAIN MEMORY SIZE

SLOT #'s	PAIR #	MEMORY SIZE*	COMMENTS
6 and 7	0	2 Mbyte (Maximum)	Slot 6 is memory card 0 (even words). Slot 7 is memory card 1 (odd words).
8 and 9	1	4 Mbyte (Maximum)	Slot 8 is memory card 2 (even words). Slot 9 is memory card 3 (odd words).
10 and 11	2	6 Mbyte (Maximum)	Slot 10 is memory card 4 (even words). Slot 11 is memory card 5 (odd words).
12 and 13	3	8 Mbyte (Maximum)	Slot 12 is memory card 6 (even words). Slot 13 is memory card 7 (odd words).

* Except for pair 0 which must always be 1 Mbytes, this is maximum memory size with the specified number of memory cards. Using half-loaded cards results in smaller memory sizes than indicated by this table; that is, with half-loaded memory cards, pair 0 fully loaded and pair 1 half-loaded will equal 3 Mbytes, and so forth.

TABLE I-2. INTERNAL CABLE CONNECTIONS

PC CARD	CONNECTOR	TO	CONNECTOR	PC CARD
210-7604	J1		J3	210- 11
"	J2		J3	
"	J3		J3	210-7605
"	J4		J4	"
"	L46	16-pin ribbon ca	L83	"
210-7605	J1		J1	210-7911
"	J2		J2	"

7. DIAGNOSTICS

There are changes in the VS-100 diagnostics to support the 210-7803 Main Memory card, as follows:

A. DE10 (WLI #702-8026) -- VS-100 Microdiagnostic Main Memory (64K RAM) stand-alone memory diagnostic that isolates failures to the RAM chip. Currently, it will not work on memory configurations of less than 2 magabytes and is now being rewritten.

B. FASTMEM (WLI #702-0108A) -- This stand-alone memory diagnostic also isolates failures to the RAM chip. Currently, it is not compatable with the 64K RAM chips and is now being rewritten. However, it can function as a Go/No Go Main Memory test. It can be run on the 210-7803 card and if there are no failures it will indicate that there are no failures. If there is a memory failure, the test will indicate only that there is a failure but will not indicate the correct location of the failing RAM chip.

There are no changes to the current diagnostics to support the 210-7604-1A Cache Memory or the 210-7911 BA.

8. VS-100 MAIN MEMORY THEORY

The VS-100 Main Memory (Figure I-7) consists of up to eight memory cards (modules) with each card containing 256K 32-bit half words or 1 Megabytes and is logically divided into four groups of 64k 32-bit half words.. A minimum of two cards are required. The memory uses the Hitachi 4864, 64K-word x 1-bit Dynamic RAM chip. Total maximum memory capacity is 8 Megabytes.

A. Control Signals

Main memory control signals are generated on the SBC portion of the Cache card due to the physical limitations of the SBC card. (Refer to paragraph 2.8.8, Main Memory Control.) They are RAS (Row Address Strobe), CAS (Column Address Strobe), CEN (Column Enable), R/W (Read/Write), two Write Pulses (WP0-31 and WP32-63), MS1-4 (Module Select #), and REF (Refresh). The Main Memory cycle runs synchronously with the SBC cycle.

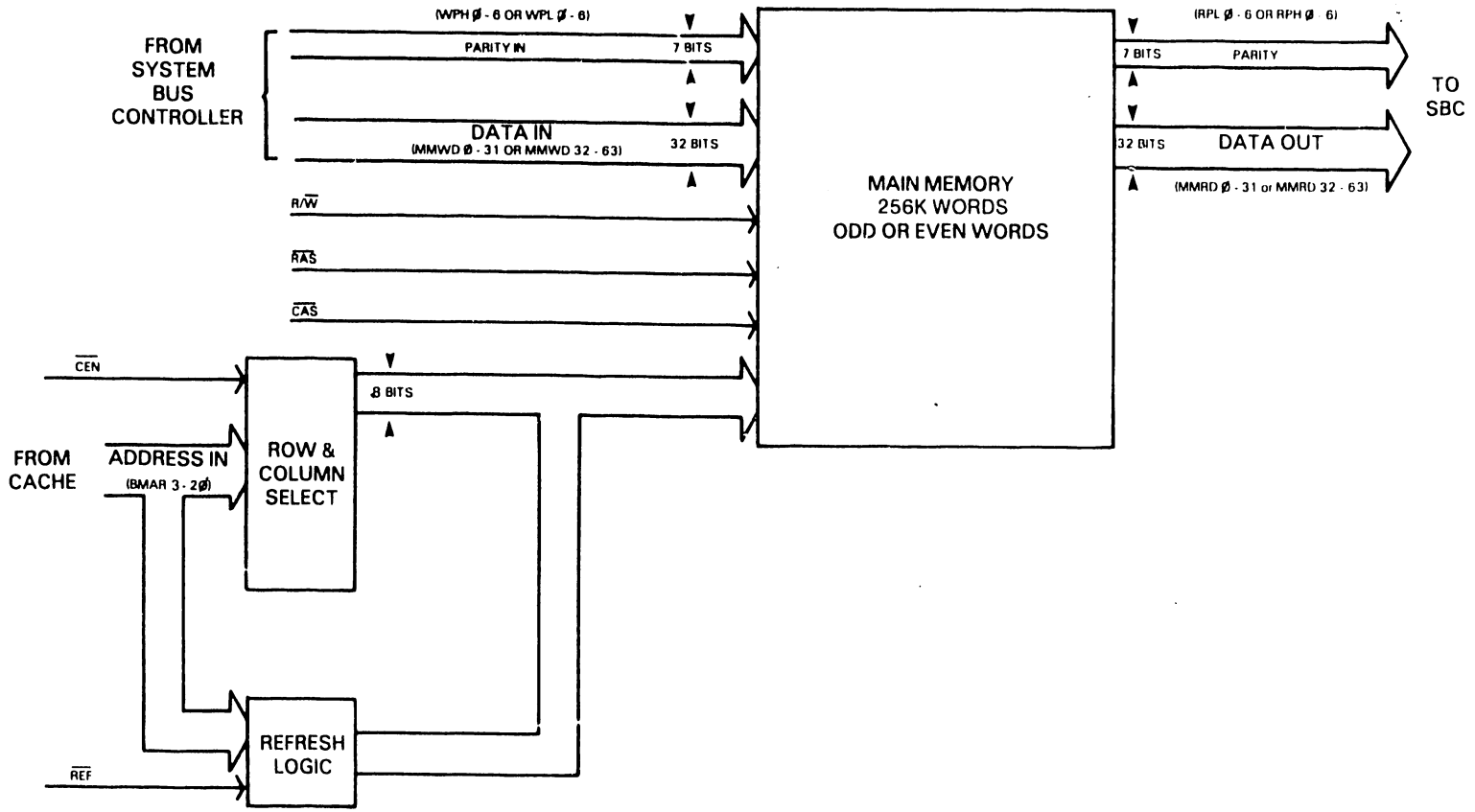


FIGURE I-7. VS-100 MAIN MEMORY

B. Memory Write And Read

CP or BA data transfer to and from the memory is controlled by the SBC. The basic memory data word is 32 bits with a 7 bit ECC (Error Correction Code) field. Write operations allow any card to be accessed seperately for word writes, or in pairs for doubleword writes. The SBC can align units of 1, 2, 4, or 8 bytes, but only words or doublewords can be written. All read operations cause a doubleword (8 bytes or 64 bits) to be accessed with the first card (0) containing the even addressed word, and the second card (1) containing the odd addressed word. Hence, the necessity of a minimum configuration two cards.

For a memory write operation, the even word of data (MMWD0-31) and parity (WPH0-6), and/or the odd word of data (MMWD32-63) and parity (WPL0-6) from the SBC will be written into the RAM by the Write Pulse (WP0-31 or WP32-63) as long as R/W (Read/Write), CAS (Column Address Strobe), and RAS (Row Address Strobe) are active. Row and column addresses are available coincident with RAS and CAS. Write pulses are generated on the Cache for the odd and/or even word cards. This allows a single word write without having to encode an address to distinguish between cards in a pair. When the Check ECC (Error Correction Code) diagnostic feature is active, all data RAMs will be disabled and writing will only be allowed into the parity RAMs.

For a memory read operation, the even word of data (MMRD0-31) and parity (RPH0-6), and the odd word of data (MMRD32-63) and parity (RPL0-6) will be read from the RAM and transfered to the SBC, when the Column Address Strobe is active, as long as Read/Write remains inactive. Again, row and column addresses are available coincident with RAS and CAS.

C. Addressing

Memory addresses are supplied by the CP or the BA. Of the 24 address bits available (BMAR0-23), (Refer to TABLE I-3) only eighteen (BMAR3-20) are used at the memory card. BMAR0 is not used. BMAR1-2 are decoded on the Cache into card pair selection (Module Select #).

Sixteen address bits (BMAR5-20) are required to decode one of the 64k memory locations. The eight row addresses (BMAR6-13) are latched into the RAM's internal row address decoder by the Row Address Strobe. The eight column addresses (BMAR5 and BMAR14-20) are selected by CEN (Column Enable). These addresses are then latched into the RAM's internal column address decoder by the Column Address Strobe. BMAR21-23 are not used because the lowest accessable addressed unit is eight bytes (two words).

D. Refresh

Because a dynamic RAM will not store data indefinitely, the data must be written back at least once every two milliseconds. Rewriting the RAM is done internally and is called "refresh". With the new 64K RAM chips, the VS-100 will still refresh every 15 microseconds. This operation has priority over all other memory operations.

When a refresh cycle (REF) is initiated, RAS (Row Address Strobe) will be enabled for all RAMs, as they require refresh with only RAS cycles. Row refresh addresses are supplied by the SBC portion of the Cache. All CAS inputs will be disabled by the refresh. Normal memory operations also accomplish refresh.

TABLE I-3. VS-100 MAIN MEMORY ADDRESSES

BMAR BIT	HEX	COMMENT
BMAR 0		NOT USED
BMAR 1	F	MODULE SELECT
BMAR 2		MODULE SELECT
BMAR 3		64K WORD GROUP
BMAR 4		64K WORD GROUP
BMAR 5	F	COLUMN ADDRESS
BMAR 6		ROW ADDRESS
BMAR 7		ROW ADDRESS
BMAR 8		ROW ADDRESS
BMAR 9	F	ROW ADDRESS
BMAR 10		ROW ADDRESS
BMAR 11		ROW ADDRESS
BMAR 12		ROW ADDRESS
BMAR 13	F	ROW ADDRESS
BMAR 14		COLUMN ADDRESS
BMAR 15		COLUMN ADDRESS
BMAR 16		COLUMN ADDRESS
BMAR 17	F	COLUMN ADDRESS
BMAR 18		COLUMN ADDRESS
BMAR 19		COLUMN ADDRESS
BMAR 20		COLUMN ADDRESS
BMAR 21		NOT USED
BMAR 22		NOT USED
BMAR 23		NOT USED

9. VS-100 CACHE MEMORY THEORY

The Cache Theory of Operation section has not changed from the original VS-100 Product Maintenance Manual.

10. VS-100 BUS ADAPTER THEORY

The Bus Adapter Theory of Operation section has not changed from the original VS-100 Product Maintenance Manual.

"A"-LEVEL* RECOMMENDED SPARES LIST

WLI PART #	NAME/DESCRIPTION	QTY
220-3001	16-pin flat cable, 13 inch	1
220-3033-21	26-pin shielded flat cable, 15 feet	1
220-3033-22	26-pin shielded cable W/JKT 24 feet	1
220-3033-23	26-pin flat cable W/JKT 15 feet	1
220-3033-24	26-pin shielded flat cable W/JKT 24 feet	1
220-3033-25	26-pin shielded flat cable W/JKT 15 feet	1
220-3033-26	26-pin shielded flat cable W/JKT 24 feet	1
220-3033-33	26-pin shielded flat cable W/JKT 50 feet	1
220-3033-34	26-pin shielded flat cable W/JKT 50 feet	1
220-3115	Cache-to-SBC cable, Assy B06482-0592	2
220-3116	SBC-to BA cable, Assy B06482-0594	2
220-3145	Minifloppy data cable	1
220-3146	Minifloppy control signal cable	1
220-3148	CM-to-Maintenance Panel Cable	1
220-3149	CM-to-Maintenance Panel Cable	1
220-3151	B Bus-to-Maintenance Panel cable	1
220-3152	B Bus-to-Maintenance Panel cable	1

* "A" (AREA) LEVEL RSL lists those parts which, because of cost or low failures, are not economical to replace at the Branch level.

"B"-LEVEL* RECOMMENDED SPARES LIST

WLI PART #	MODEL #	CEI PART #	NAME/DESCRIPTION	QTY
210-7600-A			CP1 (A-BUS)	1
210-7601-A			CP2 (B-BUS)	1
210-7602-A			Control Memory (CM)	1
210-7604-1A			Cache Memory	1
210-7605-A			System Bus Controller (SBC)	1
210-7608			CPU Motherboard	1
210-7609			I/O Motherboard	1
210-7614			Maintenance Panel	1
210-7803-1A			256K Main Memory (MM)	1
210-7803-2A			512K Main Memory (MM)	2
210-7803-4A			1024K Main Memory (MM)	2
210-7812			Power Supply	1
210-7911			Bus Adapter (BA)	1
212-3017	(22V25-2)	177-7102	Dual Density Tape IOP	1
212-3018	(22V26-1)	177-7103	TC IOP (1 Port)	1
212-3019	(22V26-2)	177-7104	TC IOP (2 Port)	1
212-3020	(22V26-3)	177-7105	TC IOP (3 Port)	1
212-3022	(22V27-2)	177-7107	Serial IOP (16 Port)	1
212-3023	(22V28)	177-7108	Large Disk IOP	1
270-0459			Mini Disk Controller	1
270-0460	Domestic		Linear Power Supply (60Hz)	1
270-0460-1	Interntn'l		Linear Power Supply (50Hz)	1
270-0706			Switching Power Supply	1
272-0012			Front Panel board	1
377-0415HT			Chip, Main Memory (64K)	20
400-1003			Muffin Fan	1

* "B" (BRANCH) LEVEL RSL lists those parts needed to perform corrective maintenance successfully 80% of the time. Also lists those parts needed to perform preventive maintenance successfully 100% of the time.

M500R0-A MULTI-LEVEL BILL OF MATERIAL AS OF MON DA

ASSEMBLY PART NUMBER 219-7911- - -
ASSEMBLY DESCRIPTION PCA VS-100 BUS ADAPTER MD

LEGEND
1: PERMANENT; 2: ITEM MASTER ONLY CODE; 3

POSITION IN STRUCTURE	LEGEND 1 2 3	COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY	U/M
1	FS	300-1966- - -	CAP .047 UF [illegible]V+80-20% CERAMIC MLE	200180	159.0000	EACH
1	FS	300-4022- - -	CAP 15.0 UF 20 V 10% TANT AXIAL	19278D	6.0000	EACH
2	FS	300-4022-R - -	CAP 15.0 UF [illegible]0V 10% TANT AXIAL T&R		1.0000	EACH
1	FS	330-2016- - -	RES 150 OHM 1/4W 5% FIXED COMP	21586L	2.0000	EACH
1	FS	330-2019- - -	RES 180 OHM 1/4W 5% FIXED COMP	21587P	1.0000	EACH
1	FS	330-2043- - -	RES 330 OHM 1/4W 10% FIXED COMP	20018E	15.0000	EACH
1	FS	330-2043- - -	RES 820 OHM 1/4W 5% FIXED COMP	216220	9.0000	EACH
1	IN	330-3011- - -	RES 1K OHM 1/4W 5% FIXED COMP	216220	58.0000	EACH
1	IN	350-0440- - -	64 PIN HDR 90 DEG PC+ LOK/EJT .125	200180	4.0000	EACH
1	IN	370-0026- - -	LAMP,RED (LED) MV5024	200180	9.0000	EACH
1	IN	376-0069- - -	IC 74145 BCD TO DEC DECODER DRIVER	200180	1.0000	EACH
1	IN	376-6002- - -	TAPPED DELAY LINE 100NS/100 OHM IMP		2.0000	EACH
1	IN	380-4019- - -	DIODE SCHOTTKY BARRIER RECT 1N5819	200180	8.0000	EACH
1	IN	396-0352- - -	BI/TSTD IC 7400N	19278D	12.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0730	EACH
2	IN	376-0002- - -	IC 7400N 4 2 IN POS NAND GATE		1.0000	EACH
1	IN	396-0003- - -	BI/TSTD IC 7410N	19278D	5.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0730	EACH
2	IN	376-0003- - -	IC 7410N 3 3 IN POS NAND GATE		1.0000	EACH
1	IN	396-0004- - -	BI/TSTD IC 7420N		1.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0680	EACH
2	IN	376-0004- - -	IC 7420N 2 4 IN POS NAND GATE		1.0000	EACH
1	IN	396-0006- - -	BI/TSTD IC 7474N	200180	7.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0800	EACH
2	IN	376-0006- - -	IC 7474N 2 D EDGE TRIG FLIP-FLOP		1.0000	EACH
1	IN	396-0007- - -	BI/TSTD IC 7476N		1.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0007- - -	IC 7476N 2 JK MA-SLV F/F PRST CLEAR		1.0000	EACH
1	IN	396-0008- - -	BI/TSTD IC 7442N	200180	2.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0880	EACH
2	IN	376-0008- - -	IC 7442N 4 LINE-10 LINE DECODER		1.0000	EACH
1	IN	396-0010- - -	BI/TSTD IC 7404N	19278D	2.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0010- - -	IC 7404N HEX INVERTER		1.0000	EACH
1	IN	396-0016- - -	BI/TSTD IC 7402N		2.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0016- - -	IC 7402N 4 2 IN POS NOR GATE		1.0000	EACH
1	IN	396-0031- - -	BI/TSTD IC 7430		1.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.4450	EACH
2	IN	376-0031- - -	IC 7430 8 I POS NAND GATE		1.0000	EACH
1	IN	396-0049- - -	BI/TSTD IC 74145	200470	1.0000	EACH
2	IN	376-0049- - -	IC 74145 BCD TO DEC DECODER DRIVER		1.0000	EACH

POSITION IN STRUCTURE	LEGEND 1 2 3	COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY	U/M
1	IN	396-0081- - -	BI/TSTD IC 7408	20018D	5.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0081- - -	IC 7408 4 2 IN POS AND GATE		1.0000	EACH
1	IN	396-0093- - -	BI/TSTD IC 7432	19278D	2.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.2250	EACH
2	IN	376-0093- - -	IC 7432 4 2 IN OR GATE		1.0000	EACH
1	IN	396-0098- - -	BI/TSTD IC 74174		1.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0650	EACH
2	IN	376-0098- - -	IC 74174 HEX D TYPE FLIP FLOP		1.0000	EACH
1	IN	396-0138- - -	BI/TSTD IC 74298	19278D	4.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0138- - -	IC 74298 4 2 IN MX W/STORAGE		1.0000	EACH
1	IN	396-0139- - -	BI/TSTD IC 7414	19278D	1.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0650	EACH
2	IN	376-0139- - -	IC 7414 HEX SCHMITT TRIGGER		1.0000	EACH
1	IN	396-0171- - -	BI/TSTD IC 74148		1.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0171- - -	IC 74148 8-3 LINE PRIORITY ENCODER		1.0000	EACH
1	IN	396-0184- - -	BI/TSTD IC 74S51	19278L	7.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0184- - -	IC 74S51 2 2 & 2 IN AND OR INV GT		1.0000	EACH
1	IN	396-0189- - -	BI/TSTD IC 8T97	19278D	22.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0189- - -	IC 8T97 H SPEED HEX 3 STATE BUFFER		1.0000	EACH
1	IN	396-0197- - -	BI/TSTD IC 74S04	19278D	7.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0197- - -	IC 74S04 HEX INVERTER		1.0000	EACH
1	IN	396-0199- - -	BI/TSTD IC 74S02		2.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0199- - -	IC 74S02 4 2 IN POS NOR GATE		1.0000	EACH
1	IN	396-0200- - -	BI/TSTD IC 74S08	19278D	14.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0200- - -	IC 74S08 4 2 IN POS AND GATE		1.0000	EACH
1	IN	396-0201- - -	BI/TSTD IC 74S64	19278D	7.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0201- - -	IC 74S64 4 2 3 2 IN AND OR INV GT		1.0000	EACH
1	IN	396-0202- - -	BI/TSTD IC 74S74	20018D	13.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0202- - -	IC 74S74 2 D TYPE F F & PRESET CLER		1.0000	EACH

POSITION IN STRUCTURE	LEGEND 1 2 3	COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY	U/M
1	IN	396-0204- - -	BI/TSTD IC 74LS257		2.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0204- - -	IC 74LS257 4 2-1 LINE DATA SELC MX		1.0000	EACH
1	IN	396-0205- - -	BI/TSTD IC 74S32	19278D	7.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0205- - -	IC 74S32 4 2 IN POS OR GATE		1.0000	EACH
1	IN	396-0206- - -	BI/TSTD IC 74S260		3.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0206- - -	IC 74S260 2 5 IN POS NOR GATE		1.0000	EACH
1	IN	396-0217- - -	BI/TSTD IC 74S157	20407D	18.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0217- - -	IC 74S157 4 2-1 LINE DATA SELC MX		1.0000	EACH
1	IN	396-0221- - -	BI/TSTD IC 74S194	19278D	3.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0770	EACH
2	IN	376-0221- - -	IC 74S194 4 BIT BI DIR UNIV SHIFT		1.0000	EACH
1	IN	396-0228- - -	BI/TSTD IC 74S00	19278D	9.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0590	EACH
2	IN	376-0228- - -	IC 74S00 4 2 IN POS NAND GATE		1.0000	EACH
1	IN	396-0230- - -	BI/TSTD IC 74S20	19278D	2.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0580	EACH
2	IN	376-0230- - -	IC 74S20 2 4 IN POS NAND GATE		1.0000	EACH
1	IN	396-0235- - -	BI/TSTD IC 74S163		7.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0235- - -	IC 74S163 SYN 4 BIT COUNTER		1.0000	EACH
1	IN	396-0237- - -	BI/TSTD IC 74S11		3.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0580	EACH
2	IN	376-0237- - -	IC 74S11 3 3 IN POS AND GATE		1.0000	EACH
1	IN	396-0238- - -	BI/TSTD IC 74S10	19278D	1.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0580	EACH
2	IN	376-0238- - -	IC 74S10 3 3 IN POS NAND GATE		1.0000	EACH
1	IN	396-0246- - -	BI/TSTD IC 74S280	19278D	18.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0580	EACH
2	IN	376-0246- - -	IC 74S280 9 BIT ODD EVEN PARITY GEN		1.0000	EACH
1	IN	396-0247- - -	BI/TSTD IC 74S174		8.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0580	EACH
2	IN	376-0247- - -	IC 74S174 HEX D TYPE FLIP FLOP		1.0000	EACH
1	IN	396-0270- - -	BI/TSTD IC 74S175	19278D	6.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0580	EACH
2	IN	376-0270- - -	IC 74S175 4 D-TYPE F/F		1.0000	EACH

POSITION IN STRUCTURE	LEGEND 1 2 3	COMPONENT PART NUMBER	DESCRIPTION	F C N	QUANTITY PER ASSY	U/M
1	IN	396-0271- - -	BI/TSTD IC 74S86		1.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.4110	EACH
2	IN	376-0271- - -	IC 74S86 4 2 INPUT EXCLUSIVE OR		1.0000	EACH
1	IN	396-0286- - -	BI/TSTD IC 74LS374	19278D	1.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.1360	EACH
2	IN	376-0286- - -	IC 74LS374 8 LATCHES W/TR ST OUTP		1.0000	EACH
1	IN	396-0288- - -	BI/TSTD IC 74LS244		4.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0288- - -	IC 74LS244 OCTUAL BUF/LINE DR 3 OUT		1.0000	EACH
1	IN	396-0296- - -	BI/TSTD IC 74S37	20018D	4.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.1750	EACH
2	IN	376-0296- - -	IC 74S37 4 2 IMPUT POS NAND BUFFER		1.0000	EACH
1	IN	396-0298- - -	BI/TSTD IC 74S138		3.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0580	EACH
2	IN	376-0298- - -	IC 74S138 3 TO 8 LINE DECODER/MPX		1.0000	EACH
1	IN	396-0301- - -	BI/TSTD IC 74S158	19278D	13.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
2	IN	376-0301- - -	IC 74S158 QUAD 2/1 DATA SELECT/MVX		1.0000	EACH
1	IN	396-0305- - -	BI/TSTD IC 74S374	19278D	18.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.1750	EACH
2	IN	376-0305- - -	IC 74S374 OCTAL D TYP E-F SCHOTTKY		1.0000	EACH
1	IN	396-0306- - -	BI/TSTD IC 74S373		15.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0580	EACH
2	IN	376-0306- - -	IC 74S373 OCTAL D-TYP LATCHES SCHTT		1.0000	EACH
1	IN	396-0310- - -	BI/TSTD IC 74LS373		3.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0580	EACH
2	IN	376-0310- - -	IC 74LS373 OCTL D-TYP LATCHES SCHTT		1.0000	EACH
1	IN	396-0333- - -	BI/TSTD IC 74S139		2.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0580	EACH
2	IN	376-0333- - -	IC 74S139 2 TO 4 LINE DECODE DEMUX		1.0000	EACH
1	IN	396-0334- - -	BI/TSTD IC 74S241	19278D	3.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.0580	EACH
2	IN	376-0334- - -	IC 74S241 OCTAL BUF/LINE DR/LN REC		1.0000	EACH
1	IN	396-0349- - -	BI/TSTD IC 74S189		32.0000	EACH
2	IN	000-9999- - -	OTHER DIRECT COST		.1580	EACH
2	IN	376-0349- - -	IC 74S189 16 4-BIT WORDS TRI-ST O/P		1.0000	EACH
1	IN	452-2095-55- -	FACEPLATE, P.C. BD C604 D10010-5106	17706D	1.0000	EACH
1	IN	510-7511- - -	PCB VS-100 BUS ADAPTER BD		1.0000	EACH
1	FS	650-2087- - -	4-40X1/4 PAN HD PHL MS SS MAG. SEMS	17706D	6.0000	EACH

MH0080-A M U L T I - L E V E L B I L L O F M A T E R I A L AS OF RUN DA

ASSEMBLY PART NUMBER 210-7803-4A- -
ASSEMBLY DESCRIPTION PCA VS130 256X39 BIT MAIN MEM 1024K

LEGEND
1: PHANTOM; 2: ITEM MASTER DELY CODE: *

POSITION IN STRUCTURE	LEGEND 1 2 *	COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY	U/M
1	IN	00 -0033- - -	LABOR CALCULATING SYSTEMS	21167	4.25[illegible]	
1	IN	000-0011- - -	LABOR QUALITY CONTROL	21167	.85[illegible]	
1	P IN	210-7803-4 - -	PCA VS130 256X39 BIT MAIN MEM 1024K	21167	1.0000	EACH
2	IN	390-1930- - -	.1 UF 50V +80-20% CERAMIC CAP(HIFRQ	21167	156.0000	EACH
2	FS	300-1966- - -	CAP .047 UF 50V+80-20% CERAMIC MLD	21167	45.0000	EACH
2	FS	300-4018- - -	CAP 18.0 UF 15 V 10% TANT AXIAL	21167	8.0000	EACH
3	FS	30[illegible]-4018-R - -	CAP 18.0 UF 15V 10% TANT AXIAL T&R		1.0000	EACH
2	FS	30[illegible]-4022- - -	CAP 15.0 UF 20 V 10% TANT AXIAL	21167	3.0000	EACH
3	FS	3[illegible]-4022-R - -	CAP 15.0 UF 20V 10% TANT AXIAL T&R		1.0000	EACH
2	FS	330-1022- - -	RES 22 OHM 1/4W 10% FIXED COMP	21167	8.0000	EACH
2	FS	330-1047- - -	RES 47 OHM 1/4W 10% FIXED COMP	21167	52.0000	EACH
2	FS	330-1056- - -	RES 56 OHM 1/4W 10% FIXED COMP	21167	104.0000	EACH
2	FS	330-3010- - -	RES 1K OHM 1/4W 10% FIXED COMP	21167	8.0000	EACH
2	IN	376-0139- - -	IC 74S14 HEX SCHMITT TRIGGER	21167	2.0000	EACH
2	IN	376-0333- - -	IC 74S139 2 TO 4 LINE DECODE DEMUX	21167	1.0000	EACH
2	IN	376-0334- - -	IC 74S240 OCTAL BUF/LINE DR/LN REC	21167	8.0000	EACH
2	IN	376-9002- - -	IC 16 PIN SOCKET BURNDY	21167	156.0000	EACH
2	IN	396-0184- - -	BI/TSTD IC 74S51	21167	2.0000	EACH
3	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
3	IN	376-0184- - -	IC 74S51 2 2 W 2 IN AND OR INV GT		1.0000	EACH
2	IN	396-0189- - -	BI/TSTD IC 8T97	21167	16.0000	EACH
3	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
3	IN	376-0189- - -	IC 8T97 H SPEED HEX 3 STATE BUFFER		1.0000	EACH
2	IN	396-0197- - -	BI/TSTD IC 74S04	21167	1.0000	EACH
3	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
3	IN	376-0197- - -	IC 74S04 HEX INVERTER		1.0000	EACH
2	IN	396-0200- - -	BI/TSTD IC 74S08	21167	1.0000	EACH
3	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
3	IN	376-0200- - -	IC 74S08 4 2 IN POS AND GATE		1.0000	EACH
2	IN	396-0205- - -	BI/TSTD IC 74S32	21167	1.0000	EACH
3	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
3	IN	376-0205- - -	IC 74S32 4 2 IN POS OR GATE		1.0000	EACH
2	IN	396-0228- - -	BI/TSTD IC 74S00	21167	8.0000	EACH
3	IN	000-9999- - -	OTHER DIRECT COST		.3750	EACH
3	IN	376-0228- - -	IC 74S00 4 2 IN POS NAND GATE		1.0000	EACH
2	IN	396-0301- - -	BI/TSTD IC 74S158	21167	2.0000	EACH
3	IN	000-9999- - -	OTHER DIRECT COST		.0750	EACH
3	IN	376-0301- - -	IC 74S158 QUAD 2/1 DATA SELECT/MVX		1.0000	EACH
2	IN	396-0306- - -	BI/TSTD IC 74S374	21167	3.0000	EACH
3	IN	000-9999- - -	OTHER DIRECT COST		.3750	EACH
3	IN	376-0306- - -	IC 74S374 OCTAL D-TYP LATCHES SCHTT		1.0000	EACH
2	IN	450-2095-01- -	HANDLE, P.C. BOARD C10016-5018	21167	1.0000	EACH

POSITION IN STRUCTURE	LEGEND 1 2 3	COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY	U/M
2	IN	51[illegible]-7623- - -	ICP VS-1[illegible] 256X36 BIT MAIN MEMORY	21167	1.0000	EACH
2	FS	6[illegible]-2120- - -	4-40 X 3/4 PAN HD PHL MS SS SEMS	21167	3.0000	EACH
1	IN	377-0415- - -	IC HM4864-3 64KX1 DYM RAM-200 NS	22289	156.0000	EACH

END OF REPORT MB[illegible]-A

APPENDIX

J

VS-90

APPENDIX J

This section contains information concerning the new VS-90, including description, specifications, installation, diagnostics, theory of operation, and an updated "A" and "B" level Recommended Spares List (RSL).

1. GENERAL

This appendix will describe the VS-90 and includes system installation information, Cache and Main Memory card installation and removal information, diagnostic information, updated theory of operation, and "A" and B" level RSLs.

2. DESCRIPTION

The VS-90, a modified version of the VS-100, is a packaged system, consisting of the CPU and:

A. One 22V27-2 serial IOP to control up to sixteen workstations/printers.

B. One 22V28 or 22V28A disk IOP to control up to four disk drives.

C. One 22V25-2 or 22V15-2 tape IOP to control up to four tape drives.

D. One 22V26-3 TC IOP to control three telecommunications lines.

E. One 2266S-1 Archiving Workstation to serve as the operator console.

The standard VS Operating System and one compiler (customer's choice) are part of the package. The VS-90 CPU will run on the standard VS Operating System Revision 5.0 or above, but Revision 5.2 is required for systems containing more than 2 megabytes of Main Memory.

Listed below is the new serial tag information for 60 cps ac line frequency Mainframes. The serial tag number prefix for 50 cps ac line frequency Mainframes is 157.

MODEL NUMBER	SERIAL TAG #	MEMORY SIZE (Bytes)
VS-90-1	177-7155	1.024 Meg
VS-90-2	177-7157	2.048 Meg
VS-90-3	177-7158	3.072 Meg
VS-90-4	177-7159	4.096 Meg

From an architectural point of view, the VS-90 is identical to the VS-100 except:

A. The Cache Memory card, now designated as 210-7604-1B, has modified refresh timing to support the new 210-7803 64K RAM Main Memory card.

(Refer to Appendix I of the VS-100 Product Maintenance Manual for information concerning the 210-7803 Main Memory card.) The old 16K RAM Main Memory card, 210-7603, is NOT supported.

B. All RAM (Random Access Memory) chips, WLI #377-0413, have been removed from the Cache card.

Cache Memory Description

With all RAM (Random Access Memory) chips removed from the 210-7604-1B Cache card, it can no longer provide high speed data read access for the CP by acting as a buffer between the CP and Main Memory. Its three remaining important logical functions are:

A. Main Memory control.

B. Main Memory refresh.

C. IPC (Interprocessor Communications) control.

All other VS-100 hardware features are found on the new VS-90 (e.g., 64-bit data busses, System Bus Controller, loadable Control Memory, etc.).

The VS-90 has the following configuration restrictions:

A. Main Memory can be increased from a minimum of 1 megabytes of Main Memory to a maximum of 4 megabytes in one megabyte increments. Only the first four memory slots of the motherboard are used.

B. Only one Bus Adapter with a maximum of eight IOPs is supported.

C. A maximum of 48 serial devices (workstations/printers) are supported.

D. A maximum of two disk IOPs are supported. This means that 2.3 gigabytes of on-line disk storage are available when the VS-90 is fully configured with 8-288 megabyte disk drives.

Any hardware additions that exceed these restrictions will require a field upgrade. This field upgrade will change the VS-90 to a VS-100.

Additional tape and telecommunication IOP's (a maximum of 8) can be added to the system. (Total: a maximum of eight (8) IOP's.)

3. SPECIFICATIONS

Following are the physical, electrical, and enviromental specifications of the VS-90.

A. Physical Specifications

Net Weight	Pounds	Kilograms
	353	158.3

All other physical specifications are identical to the VS-100 specifications. (Refer to paragraph 1.12, System Specifications).

B. Electrical Specifications: All electrical specifications are identical to the VS-100.

C. Enviromental Specifications: All enviromental specifications are identical to the VS-100.

D. Architectural

Minimum Main Memory	-- 1MB	Maximum # IOPs	-- 8
Maximum Main Memory	-- 4MB	Maximum # of Disk @1.2MB	-- 8
Incremental Memory	-- 1MB	Maximum # of Tape Drives	-- 4/IOP
Cache Memory	-- None	Maximum # of TC Lines	-- 3/IOP
Maximum Disk Storage	-- 2GB		
Memory Cycle Time	-- 480ns	Microinstruction Time	-- 160ns
CPU Data Path	-- 32-bit	Main Memory Data Path	-- 64-bit
IO Data Path	-- 16-bit	Word Length	-- 32-bit
Virtual Address Space Per User	-- 1MB	Virtual Address Space Per Process	-- 1MB
Concurrent User Tasks	-- 72	Background Tasks	-- 24
Concurrent Ser. WS	-- 48	Concurrent WS & Printer	-- 48
Concurrent Peripheral	-- 128		

4. SYSTEM INSTALLATION

Installation of the VS-90 is the same as the installation of the VS-100 except for Main Memory card locations and Main Memory size switch settings. Refer to Chapter 3, Unpacking and Installation, for complete installation instructions. Refer to paragraph Figure J-2 and Table J-1 of this Appendix for new Main Memory size switch settings and Main Memory card locations.

5. INSTALLATION OF CACHE AND MAIN MEMORY CARDS

Refer to Chapter 3, Unpacking and Installation, for installation information on other Mainframe circuit cards.

A. After checking memory-size switch settings (Figure J-2) on the Cache Memory card, connect the 16-pin ribbon cable from L46 of the 210-7604-1B Cache Memory card (Appendix I, Figure I-2) to L83 of the 210-7605 SBC card (Appendix I, Figure I-4).

B. Install the 210-7604-1B Cache Memory card in Motherboard slot #4. (Refer to Figure 3-7 for card locations.)

C. Refering to Table J-1, install the 210-7803 Main Memory cards in pairs starting at Motherboard slot numbers 6 and 7. Cards in even-numbered slots (6, 8,) contain even data words; cards in odd-numbered slots (7, 9,) contain odd data words. The total number of PAIRED memory cards determines Main Memory size. Make sure that the number of memory cards equals desired memory size (refer to work request). Do NOT leave open slots between memory cards.

D. Make sure that all cables running to the cards are reinstalled in the correct locations (refer to Table J-2) and all cards are firmly seated in place.

FIGURE J-2. VS-100 MAIN MEMORY SWITCH SETTINGS
LOCATED ON THE 210-7604-1B CACHE CARD

SW. NO	8	7	6	5	4	3	2	1	MEMORY SIZE IN BYTES
	NOT USED		0	1	0	0	0	0	512 K N/S
			1	1	0	0	0	0	768 K N/S
			0	0	1	0	0	0	1.0 M
			1	0	1	0	0	0	1.2 M N/S
			0	1	1	0	0	0	1.5 M N/S
			1	1	1	0	0	0	1.7 M N/S
			0	0	0	1	0	0	2.0 M
			0	0	1	1	0	0	3.0 M
			0	0	0	0	1	0	4.0 M
			0	0	1	0	1	0	5.0 M N/S
			0	0	0	1	1	0	6.0 M N/S
			0	0	1	1	1	0	7.0 M N/S
			0	0	0	0	0	1	8.0 M N/S

NOTE: N/S in the Memory Size column indicates the memory sizes that are NOT supported on the VS-90.

TABLE J-1. MAIN MEMORY SIZE

SLOT #'s	PAIR #	MEMORY SIZE*	COMMENTS
6 and 7	0	2 Mbyte (Maximum)	Slot 6 is memory card 0 (even words). Slot 7 is memory card 1 (odd words).
8 and 9	1	4 Mbyte (Maximum)	Slot 8 is memory card 2 (even words). Slot 9 is memory card 3 (odd words).

* Except for pair 0 which must always be 1 Mbytes, this is maximum memory size with the specified number of memory cards. Using half-loaded cards results in smaller memory sizes than indicated by this table; that is, with half-loaded memory cards, pair 0 fully loaded and pair 1 half-loaded will equal 3 Mbytes, and so forth.

TABLE . INTERNAL CABLE CONNECTIONS

PC CARD	CONNECTOR	TO	CONNECTOR	PC CARD
210-7604-1B	J1		J3	210-7911
"	J2		J4	"
"	J3		J3	210-7605
"	J4		J4	"
"	L46	16-pin ribbon cable	L83	"

6. REMOVAL OF CACHE AND MAIN MEMORY CARDS

Refer to Chapter 7, Removal/Replacement Procedures, for removal information on other Mainframe circuit cards.

A. Power down the Mainframe and place the circuit breaker in the OFF position.

B. 1. Remove the two 60-pin connectors from the top edge of the 7604-1B Cache Memory card that attach to the 7911 BA card.

2. Remove the two 64-pin connectors that attach to the 7605 SBC card from the right edge of the 7604-1B Cache Memory card.

3. Remove the 16-pin ribbon cable from L46 of the 210-7604-1B Cache Memory card to L83 of the 210-7605 SBC card.

4. Remove the Cache card by grasping the top corners and gently rocking it from side-to-side while exerting a steady upward pressure. Once the card is free of the slot, ease it up and out of the Mainframe.

C. Remove the 7803 Main Memory card from the Motherboard in the same manner as the previous card.

7. DIAGNOSTICS

The VS-90 has two forms of diagnostics available; On-line diagnostics and Off-line diagnostics.

All currently available VS 100 On-line diagnostics will be available on the VS-90. On-line diagnostics are stored on the system disk in library @SYSTST@. They will be executed under the control of the operator in the standard VS Operating System environment (i.e. while the system is in operation).

Standard Off-line diagnostics are stored on standard disk volumes in library @DIAGSA@. They are selected using the Stand-Alone Boot Loader.

In addition the VS90, like the VS100, will have a set of microdiagnostics available for off-line testing of the CP, Control Memory, SBC, and Main Memory. With the exception of three tests that have been modified to run on the VS90 and one test that will no longer pertain (Cache Memory test), the remainder of these microdiagnostics will be the same as those used on the VS100. Note that even the three microdiagnostics that have been modified will reference the VS100 version of the applicable diagnontics documentation.

The following microdiagnostics that referenced Cache Memory have been rewritten by Diagnostic Engineering so that they can be used on the VS-90.

Part Number	Test	Description
702-8027	VS90AA10	Memory Opcodes and Multiply Group Diagnostic
702-8028	VS90AF10	Branch Next Macro-Instruction Group Diagnostic
702-8029	VS90DE10	Main Memory Board Diagnostic (64K Chips)

A. ON-LINE DIAGNOSTICS

The following is a list and description of the "System Level" Diagnostics that will be available for the VS90.

1. FTU Program (WLI #702-0099A)

   The FTU program is a software simulation of the functions

available on the hardware Field Test Unit (FTU) that is used for testing and adjusting disk drives. It lets the operator execute the Control functions and Read/Write operations necessary to test and perform field level maintainence adjustments on the disk drives.

2. TPTEST (WLI #702-0187)

   This program is a software exerciser that lets the operator test and troubleshoot the tape drives currently used on existing VS systems. It tests the control functions, tape movement, BOT/EOT sensing, Write Protect, and other tape unit functions.

3. TCIOPTST (WLI #702-0132)

   This is a test program for the existing VS telecommunications IOP. It lets the operator test the basic functions of the telecommunications controller.

4. SERIAL DIAGNOSTIC MONITOR PACKAGES

   The Serial Diagnostic Monitor Packages are OIS Diagnostic packages converted to run under the control of the VS Operating System. They are used to down-load diagnostic microcode to the serial peripheral device to be tested. These packages include coverage for all serial workstations, matrix printers, chain printers, band printers, daisy printers, archiving workstations, twin sheet feeders, envelope feeders, typesetters, the TCB1, and Image printers. They also include the ability to test the Z80 microprocessor and it's RAM memory.

B. OFF-LINE DIAGNOSTICS

The following is a list and description of the "Stand-alone" Diagnostics that will be available for the VS90.

1. STAND-ALONE BOOT LOADER

   This program is not a diagnostic but enables the loading of Stand-alone diagnostics without a resident Operating System.

It allows multiple Stand-alone diagnostics to reside on self-booting, standard label disk volumes.

2. VS100MEM

VS100MEM will be altered to execute in the VS90 environment (64K memory chips) for repair of Main Memory to the chip level.

3. FTUA

FTUA is a "Stand-alone" version of the On-line FTU program described earlier in this document. It is designed for use when the Operating System cannot be run.

C. OFF-LINE MICRODIAGNOSTICS

Part Number	Test	Description
702-8001A	T0010	CP4 Microsequencer
702-8002A	T1010	CP4 Instr. Cntr.
702-8003A	T2010	CP4 Branch Cond.
702-8004A	T3010	CP4 Stack
702-8005A	T4010	CP4 Stack Address
702-8006A	T4110	CP4 Registers
702-8007A	T5000	CP4 Maint. Panel
702-8008A	T6010	CP4 Control Mem.
702-8009A	T7010	CP4 Control Mem.
702-8010A	T8010	CP4 Registers
702-8011A	T9010	CP4 Stack & TRAM
702-8012A	TA010	CP4 Add & Subtract
702-8013A	TB010	CP4 Logical Instr's
702-8014A	TB110	CP4 Move Instr's
702-8015A	TC010	CP4 Shift & Decimal
702-8016A	TD010	CP4 CC & Arith.
702-8019A	TBB10	CP4 SBC & ECR
702-8020A	TBB40	CP4 SBC & ECC
702-8027	VS90AA10	CP4 Mem Opcodes
702-8028	VS90AF10	CP4 BNM Instr.
702-8029	VS90DE10	Main Mem (64K Chip)

8. VS-90 CACHE THEORY

A. Cache Revisions

With all of the RAM chips removed, the Cache Random Access Memory (figure 2-7) can no longer provide high speed data read access for the CP by acting as a buffer between the CP and Main Memory.

The cache principle is based on a "HIT" (data was found in cache) or a "MISS" (data was not found in cache). Because all of the RAM chips have been removed, data that the CP requested from cache will never be found and every request will result in a "MISS".

The MISS signal is sent to the Control Memory to stop the CP 't' and 'L' clocks, if no BA is requesting a Main Memory cycle. The CP is forced to request a doubleword read directly from Main Memory. It will now take a full 480 nanosecond cycle for a Main Memory doubleword read compared to a Cache read only cycle of 80 nanoseconds when the RAM chips are installed. The MISS is also recorded in the External Condition Register of the System Bus Controller but will be invisible to the micro program.

Cache parity errors, which would normally cause a doubleword read, are no longer recorded in the Bus Transaction Log on the SBC. They have been eliminated to prevent false error indications when diagnostics are being run.

B. Main Memory Addresses From BA and CP

Both the CP and the BA produce a 24-bit Main Memory address for their respective Main Memory operations. The CP addresses (MA0-23) pass through the CP Memory Address Latch on the Cache card while the BA addresses (BA0-23) pass through the BA Address latch. The addresses are sent to the Main Memory Address Multiplexer and the memory operation in progress (CP or BA) will gate the correct set of addresses through to Main Memory as BMAR3-20.

C. Main Memory Data Direct To CP

Data from Main Memory to the CP, caused by a Cache MISS and a doubleword read, passes through the Cache card on the way to the CP. The data word, DIRD0-31, can also be IPC data from the BA to the CP.

Two other sections of the Cache card, although not part of the Cache Memory, are the Main Memory control and the IPC (Interprocessor Communications) control logic.

D. Main Memory Control

The Main Memory Control logic on the Cache card (Figure 2-8) is actually a System Bus Controller function, but is located on the Cache card due to the physical limitations of the SBC card. Both the CP and the Bus Adapter can request a variety of memory read and write operations, and both encode their own memory operations and requests. The BA, because it must support the I/O Processor, is permitted a 16-bit (halfword) memory write that the CP is not allowed. The CP has the lowest memory priority and does not require a request line because the memory control defaults all unused memory requests to the CP. Each BA has a request line.

The Main Memory Operation Decoder decodes the CP memory operation from a Control Memory word when no BA memory requests are present. The BA Priority Network chooses the BA with the highest priority (MRBA1-4) and allows the Main Memory Operation Decoder to decode the BA operation from bits BAC0-2.

The Main Memory Timing Generator produces all the memory control signals discussed under Main Memory Control Signals, paragraph 2.6.1. The CP MDR Select Logic allows the selection of the appropriate CP Memory data Register for memory read commands. The STOP CP signal, halting the 't' time clocks of the CP, will be present because there was a Cache MISS; if control was busy or doing a refresh and a CP write command was issued; or, if a BA memory request was in progress and a CP write command was issued.

Main Memory refresh logic is also part of the memory control. It provides refresh control and row addresses (BMAR6-13) to the Main Memory at 15 microsecond intervals. Refresh has priority over all other requesting processors.

E. Interprocessor Communications Control

IPC (Interprocessor Communications) control logic (Figure 2-9) is also a System Bus Controller function but is located on the Cache card due to the physical limitations on the SBC. The logic is responsible for IPC message send and receipt control.

The IPC feature has two basic functions. The first function allows two processors to communicate with each other without using Main Memory facilities, and the second function allows the I/O Processor to interrupt the CP because the CP will not accept asynchronous messages from the IOP. The CP, Bus Adapter, and SBC are all considered processors.

The IPC data words are 32-bit messages created by a processor. There are two types of messages (dialogs); CP initialization of the BA, and I/O initialization and interrupts. The BA is used for buffering and routing the message.

The IPC receipt RAM stores IPC data bits 0-7 in the form of a message receipt control, a sending processor number, and a destination processor number. The RAM does not store the actual message. The Message Receipt Control Logic allows acceptance or rejection of any IPC message from any processor. The MDR Load Control alerts MDR#4, the IPC memory data register for the CP, of a pending message. The Bus Adapter IPC Ready Control produces the proper Data Ready (DRY1-4) signal to a particular Bus Adapter. DRY1-4 corresponds to Bus Adapter 1-4. DRY will be used at the BA to gate the IPC data into the B. A. IPC Data Latch.

"A"-LEVEL* RECOMMENDED SPARES LIST

WLI PART #	NAME/DESCRIPTION	QTY
210-7604-1B	Cache Memory	1
210-7608	CPU Motherboard	1
210-7609	I/O Motherboard	1
210-7614	Maintenance Panel	1
210-7812	Power Supply	1
270-0460	Linear Power Supply	1
272-0012	Front Panel Board	1

* "A" (AREA) LEVEL RSL lists those parts which, because of cost or low failures, are not economical to replace at the Branch level.

"B"-LEVEL* RECOMMENDED SPARES LIST

WLI PART #	NAME/DESCRIPTION	QTY
210-7600-A	CP1 (A-Bus)	1
210-7601-A	CP2 (B-Bus)	1
210-7602-A	Control Memory (CM)	1
210-7605-A	System Bus Controller (SBC)	1
210-7803-2A	512K Main Memory (MM)	1
210-7611	Bus Adapter (BA)	1
212-3017	Dual Density Tape IOP	1
212-3018	TC IOP (1 Port)	1
212-3019	TC IOP (2 Port)	1
212-3020	TC IOP (3 Port)	1
212-3022	Serial IOP (16-port)	1
212-3023	Large Disk IOP	1
270-0459	Mini Disk Controller	1
270-0706	Switching Power Supply	1

* "B" (BRANCH) LEVEL RSL lists those parts needed to perform corrective maintenance successfully 80% of the time.

APPENDIX
K
VS-100 ASYNC DEVICE CONTROLLER

APPENDIX K

VS-100 ASYNC DEVICE CONTROLLER

K.1 GENERAL

This appendix describes the VS-100 22V36 Async Device Controller (ADC). Included in this appendix is information on theory of operation, installation, maintenance, troubleshooting, and field replaceable units (FRUs).

K.2 HARDWARE DESCRIPTION

The heart of the ADC is an Intel 8086 Microprocessor, which supervises eight RS-232-C I/O channels with programmable baud rate (1200-19.2 KB) and protocol for each channel, and one Wang PC-compatible parallel printer port. The ADC can support eight Wang 2110 workstations or eight async devices with RS-232-C interface. The eight serial devices are driven through an async serial link via a full duplex RS-232-C connector. The ADC communicates with the host VS through a 2K-word direct memory access (DMA).

The ADC consists of the following four pc boards:

- TCP/IOP Motherboard (WLI P/N 210-7826) -- This previously existing 16 x 16.5 inch board plugs directly into the VS-100 motherboard and contains the IOP hardware. The 7826 is used as the motherboard for the 210-8168 device adapter (see below) in order to maintain compatibility with the existing IOP software.

- Controller Board (WLI P/N 210-8168) -- This 16 x 14 inch 8086-based device adapter board plugs directly into the TCP/IOP Motherboard and contains the electronics and logic (except for transceivers and IOP). The controller board also has four 40-pin cable connectors and one 26-pin cable connector to carry the signals for the eight RS-232-C ports via ribbon cables to the back panel assembly.

- Line Driver/Receiver Daughterboard (WLI P/N 210-8324) -- Discrete drivers and receivers, which support the eight RS-232-C ports and the printer port and provide communications up to 2000 feet, are located on this 5 x 9 inch board. It plugs into the 210-8323 connector board and is located just inside the back panel of the system. The transceiver board interfaces the connector board to the controller board via ribbon cables.

- Line Driver/Receiver Motherboard (WLI P/N 210-8323) -- This 5 x 9 inch board fastens directly to the back panel of the system and provides the eight RS-232-C connectors to the user. It is the motherboard into which the 8324 board plugs. The 8323 and the 8324 boards fasten together to form the Async Rear Panel Assembly.

K.3 SOFTWARE DESCRIPTION

The ADC requires Operating System (OS) Release 6.4X.XX to provide the support to load a microcode file to the ADC and to support the eight async workstations.

K.4 FUNCTIONAL DESCRIPTION

The following paragraphs give a brief overview of the operation of the VS-100 ADC. An upper level block diagram (figure K-2) is provided to aid the reader in understanding the workings of and the relationship between the different functional areas.

K.4.1 MEMORY

ADC memory is organized in three parts (see figure K-1):

- Code RAM
- DMA Memory
- PROM Memory

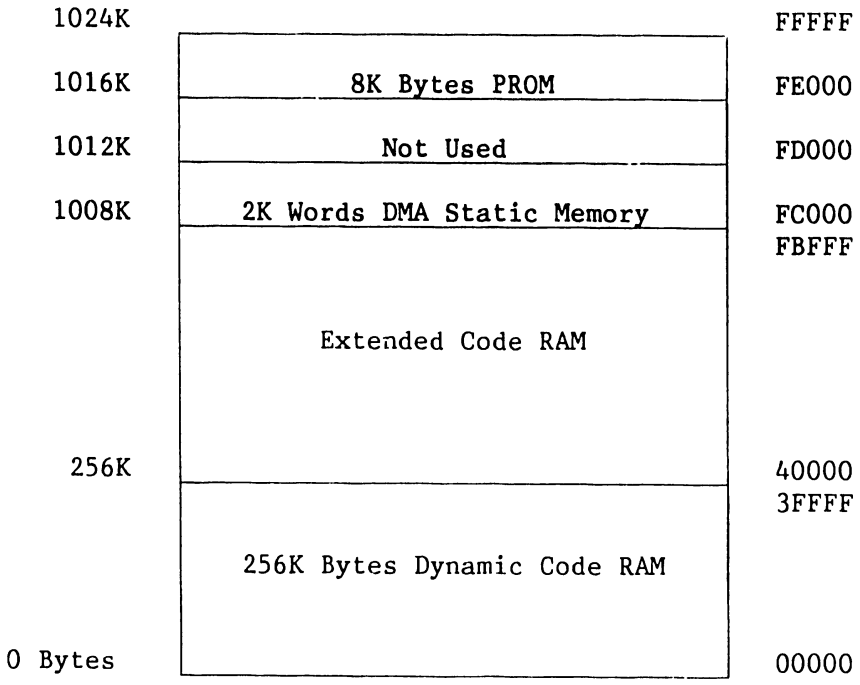


Figure K-1. ADC Memory Organization

K.4.1.1 Code RAM

Code RAM is a 256K, 640K, or 1 Meg (depending on whether and to what extent 256K chips are used) dynamic random access memory, accessible to both the 8086 microprocessor and the direct memory access (DMA) controller. The 8086 uses code RAM to buffer data to and from the I/O ports. The DMA controller

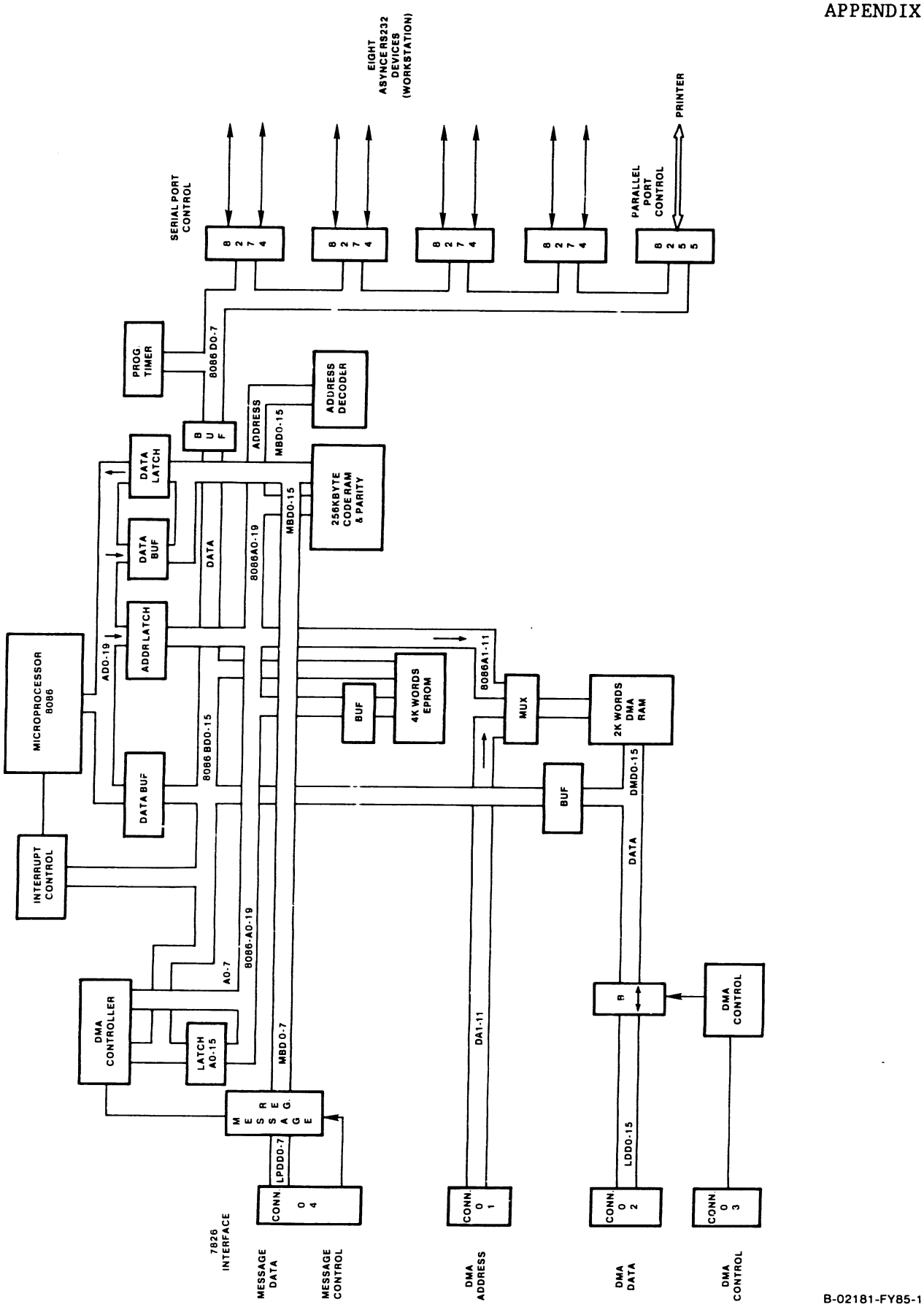


Figure K-2. ADC Functional Block Diagram

passes messages to and from the IOP via this RAM under the control of the 8086. Arbitration between the 8086 and the DMA and refresh are hardware controlled and all non-contended accesses occur without wait states.

K.4.1.2 DMA Memory

DMA memory can be accessed directly by the 8086 or the host VS via the IOP's DMA circuitry. This memory allows the 8086 to initiate the transfer of data to or from the host VS while simultaneously handling the incoming data from terminals. Hardware arbitration allows the 8086 to access the DMA memory while a DMA is in progress. The DMA itself, even when initiated by the ADC, is controlled by the IOP motherboard. All accesses to this RAM are word (16-bit) oriented.

K.4.1.3 PROM Memory

Two 2732A PROMs reside at addresses FE000 to FFFFF Hex. These PROMs are accessible only to the 8086 and are used for diagnostics and IPL.

K.4.2 ADC/IOP COMMUNICATION

There are two communication paths between the ADC and the IOP -- one for messages and one for data.

K.4.2.1 Message Transfer

IOP to ADC Messages:

- START I/O
- HALT I/O
- CONTROL I/O
- RESET
- GRANTED (TASK COMPLETED)
- INIT

ADC to IOP Messages:

- READ DATA
- WRITE DATA
- WRITE I/O STATUS
- QUIT

Message transfer is accomplished over an eight-bit bus between the ADC code RAM and the IOP. When the ADC wishes to send a message to the IOP, the 8086 sets up the message in code RAM and programs the DMA controller. The DMA controller will interrupt the 8086 only at the completion of a message transfer to the IOP. Because the DMA controller has only 16 address bits and paging is not supported, message transfer must use the lower 128K words of code RAM. Also, the RAM address will be twice the value in the address register of the DMA controller.

K.4.2.2 Data Transfer

Data transfers between the IOP and the ADC include microcode loads to the ADC as well as communication to and from the ADC I/O ports. The IOP initiates the microcode load, but thereafter all transfers are initiated by the ADC, using the Read Data and Write Data messages to pass the parameters of the trans

fer to the DMA hardware on the IOP. The IOP DMA hardware then takes control of the transfer of data between the ADC's DMA RAM and the system I/O bus. The 8086 may access the DMA RAM during such a transfer.

K.4.3 SERIAL I/O CHANNELS

Four 8274 multi-protocol communication chips support eight full duplex serial I/O channels which are routed to the RS-232-C interface for both short (up to 2000 feet) distance direct communication and longer distance connection via modems. The basic function of the 8274 is serial-to-parallel and parallel-to-serial conversion. The 8086 accomplishes single byte data transfers between the 8274s and memory via I/O. Each 8274 has an interrupt request line to a slave 8259 interrupt controller.

Power on or software reset enables the baud rate generators (BRG) to the transmit and receive clocks. An I/O command may be issued to switch the clock selection to external. In this mode, the transmit and receive clocks are enabled to the RS-232-C connectors.

K.4.4 BAUD RATE GENERATOR

There are four Motorola K1135C Dual Baud Rate Generators (BRGs) on the 8168 Board. Each BRG simultaneously generates two output frequencies for the 8274s. Each frequency is selectable in baud rates from 50 to 19200.

K.4.5 PROGRAMMABLE TIMER

An Intel 8253 Programmable Timer has three independent 16-bit counters. The 8086 sends out control words to initialize the counters with the desired mode. A 1.228 MHz signal is applied to the clock input of counter 0 and the output of this counter is tied to the master 8259 interrupt controller. Counter 0 is used for software timer applications. Counters 1 and 2 are not used.

K.4.6 INTERRUPTS

The 8168 board contains two 8259A Programmable Interrupt Controllers. The slave interrupt controller has as inputs the four interrupts from the 8274 communication chips. These interrupts are given highest priority by directing the slave output into the master request level 1 and not using request level 0. The interrupts to the 8086 are listed below in order of decreasing priority.

Table K-1. ADC Interrupts

INTERRUPT NAME	DESCRIPTION
Master IR0	Not used
Master IR1	Slave interrupts (8274s)
Master IR2	Parallel I/O port interrupt for printer
Master IR3	Interrupt from the 8253 timer
Master IR4	Message In interrupt
Master IR5	Message Out interrupt
Master IR6	Code RAM parity error
Master IR7	Not used
Slave IR0	8274-1
Slave IR1	8274-2
Slave IR2	8274-3
Slave IR3	8274-4

K.4.7 DIAGNOSTIC STATUS LAMP

The 8168 Controller board contains a LED (located at the top edge of the board between connectors J2 and J3) that is used to indicate the status of the power-up built-in test (BIT). A flip-flop (diagnostic status register) turns the LED on at power up. When the BIT is successfully completed, the flip-flop is reset and the LED is turned off.

K.4.8 WAIT STATE GENERATORS

There are two wait state generators associated with 8086 accesses. One generates two wait states for the EPROMS and all I/O devices, and the other provides six wait states for the parallel port data.

K.5 INSTALLATION

The following paragraphs describe the unpacking, inspection, and installation instructions for the VS-100 Async Device Controller. Refer to Chapter 4 of the VS-100 Computer System Product Maintenance Manual for more details.

K.5.1 UNPACKING

Before unpacking the VS-100 Async Device Controller, check all packing slips to ensure that the proper equipment has been delivered. Inspect all shipping containers for damage (crushed corners, punctures, etc.). Open the boxes and remove the Async Controller boards.

K.5.2 INSPECTION

Inspect the boards for packing material and such shipping damage as broken connectors. If damage is discovered, follow the reporting procedure in paragraph 4.4 of the VS-100 Product Maintenance Manual.

K.5.3 MINIMUM REQUIREMENTS

K.5.3.1 Hardware

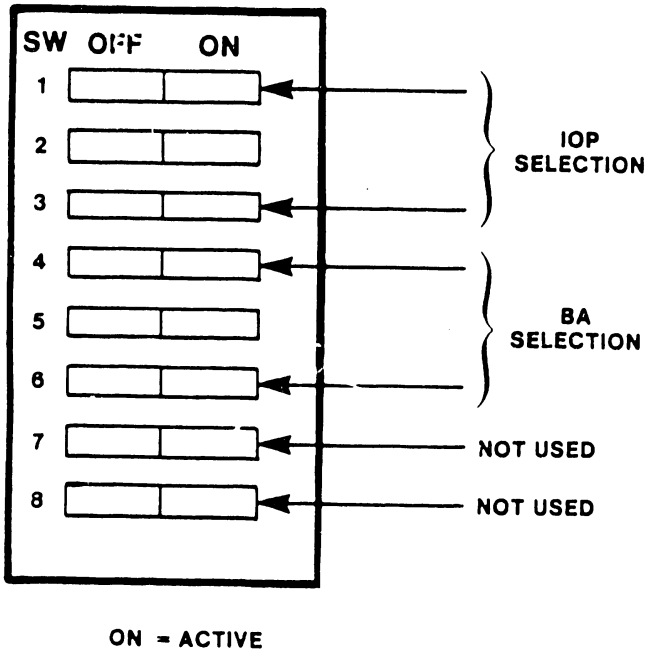
Hardware minimum requirements are listed in paragraph 4.6 of the Product Maintenence Manual.

K.5.3.2 Software

The VS-100 Async Device Controller requires a minimum OS Release 6.4X.XX.

K.5.4 ASYNC CONTROLLER INSTALLATION

1. Power down the system.
2. Remove the top cover.
3. Ensure that the switch settings, on the 210-7826 TCP/IOP motherboard to be inserted, are correct (see figures K-3 and K-4).



SW NO.	1	2	3	IOP NO.
	0	0	0	0
	0	0	1	1
	0	1	0	2
	0	1	1	3
	1	0	0	4
	1	0	1	5
	1	1	0	6
	1	1	1	7

SW NO.	4	5	6	BA NO.
	0	0	1	1
	0	1	0	2
	0	1	1	3*
	1	0	0	4*

ON = 1
OFF = 0

*FOR FUTURE EXPANSION

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Figure K-3. TCP/IOP Board Switch Settings

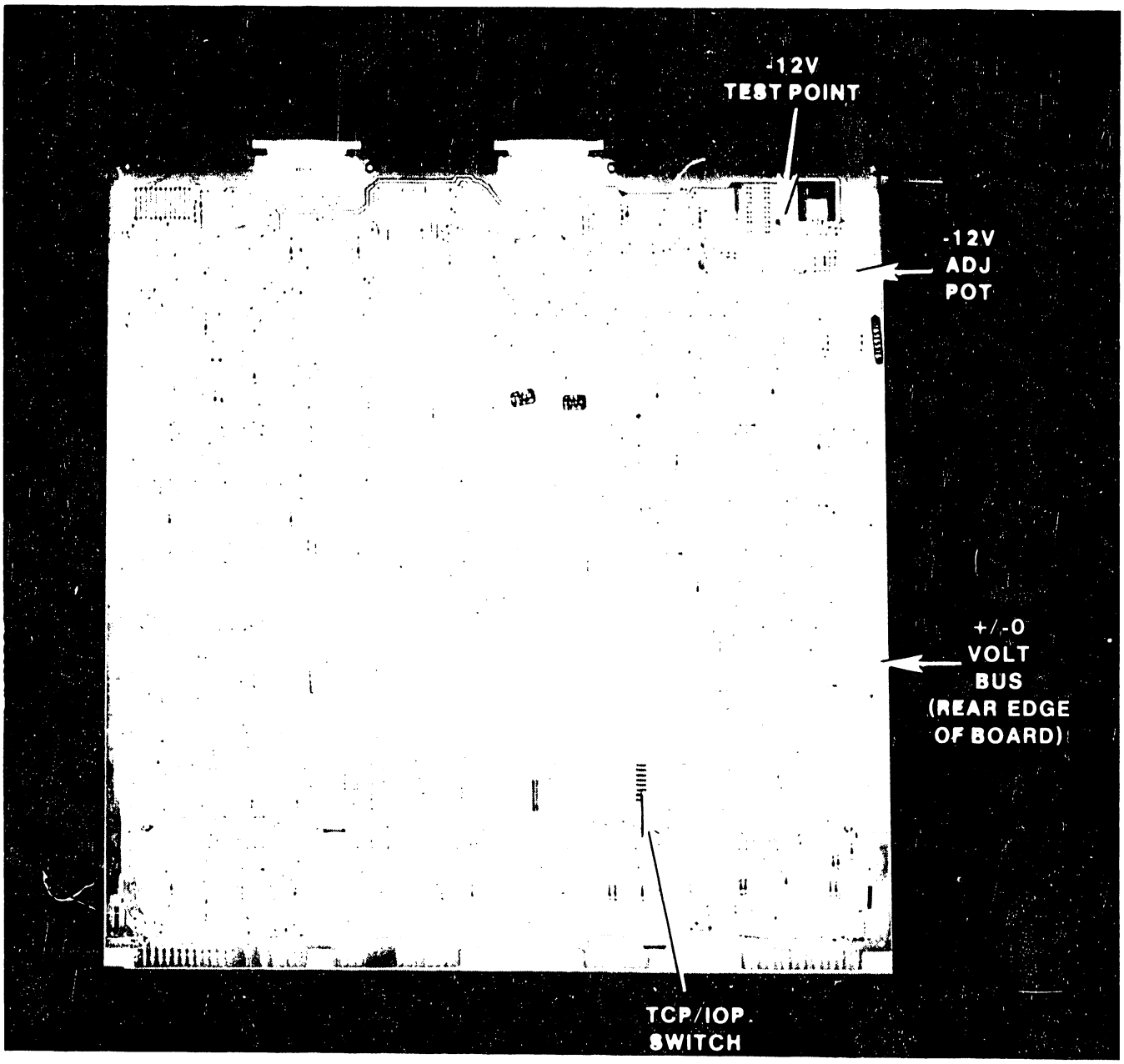


Figure K-4. 210-7826 TCP/IOP Motherboard

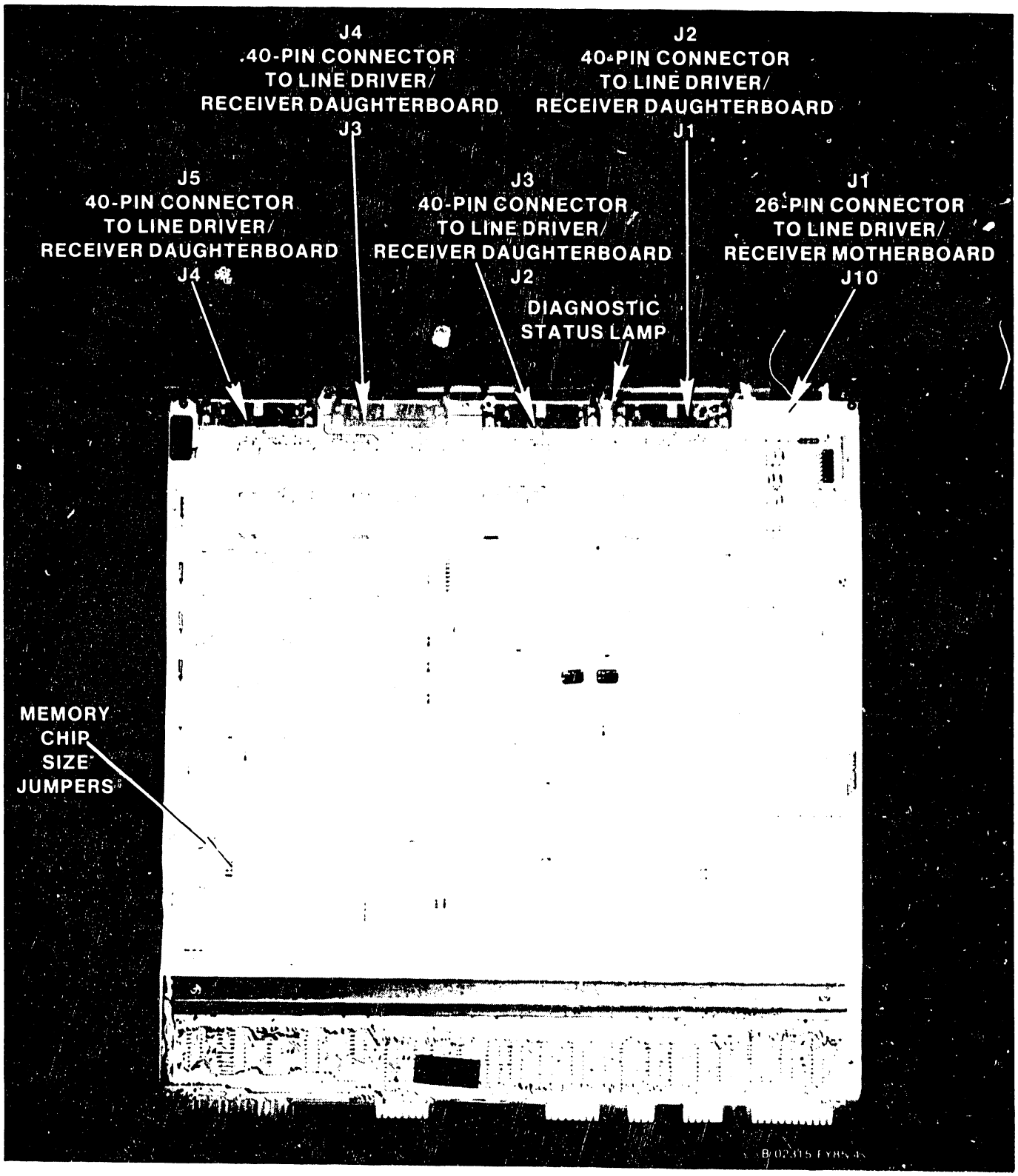


Figure K-5. 210-8168 Controller Board

4. Ensure that the memory chip size jumpers on the controller board (figure K-5 above) are in the position shown below in figure K-6. These jumpers determine the type of memory chip used. Presently only 64K RAM chips are supported.

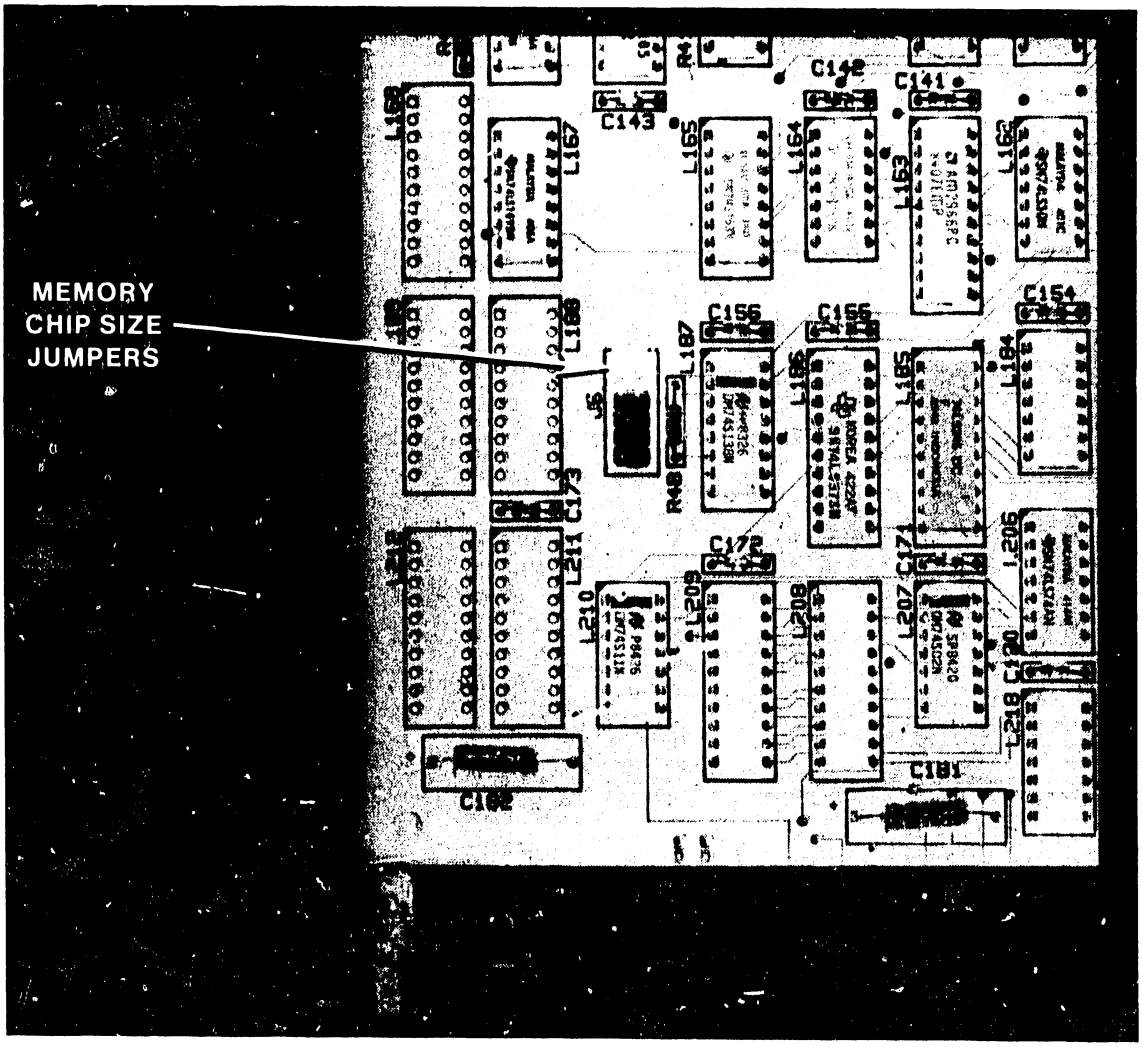


Figure K-6. 210-8168 Memory Chip Size Jumpers

5. Insert the TCP/IOP Motherboard/Controller Board assembly into an available TCP/IOP slot in the motherboard. Ensure that the connectors are mated before pushing down on board.
6. Install the Rear Panel Assembly, consisting of the 8324 Line Driver/Receiver Daughterboard (figure K-7) and the 8323 Line Driver/Receiver Motherboard (figure K-8), in the blank connector plate location (shown in figure K-9) in the rear of the mainframe using the hardware provided.

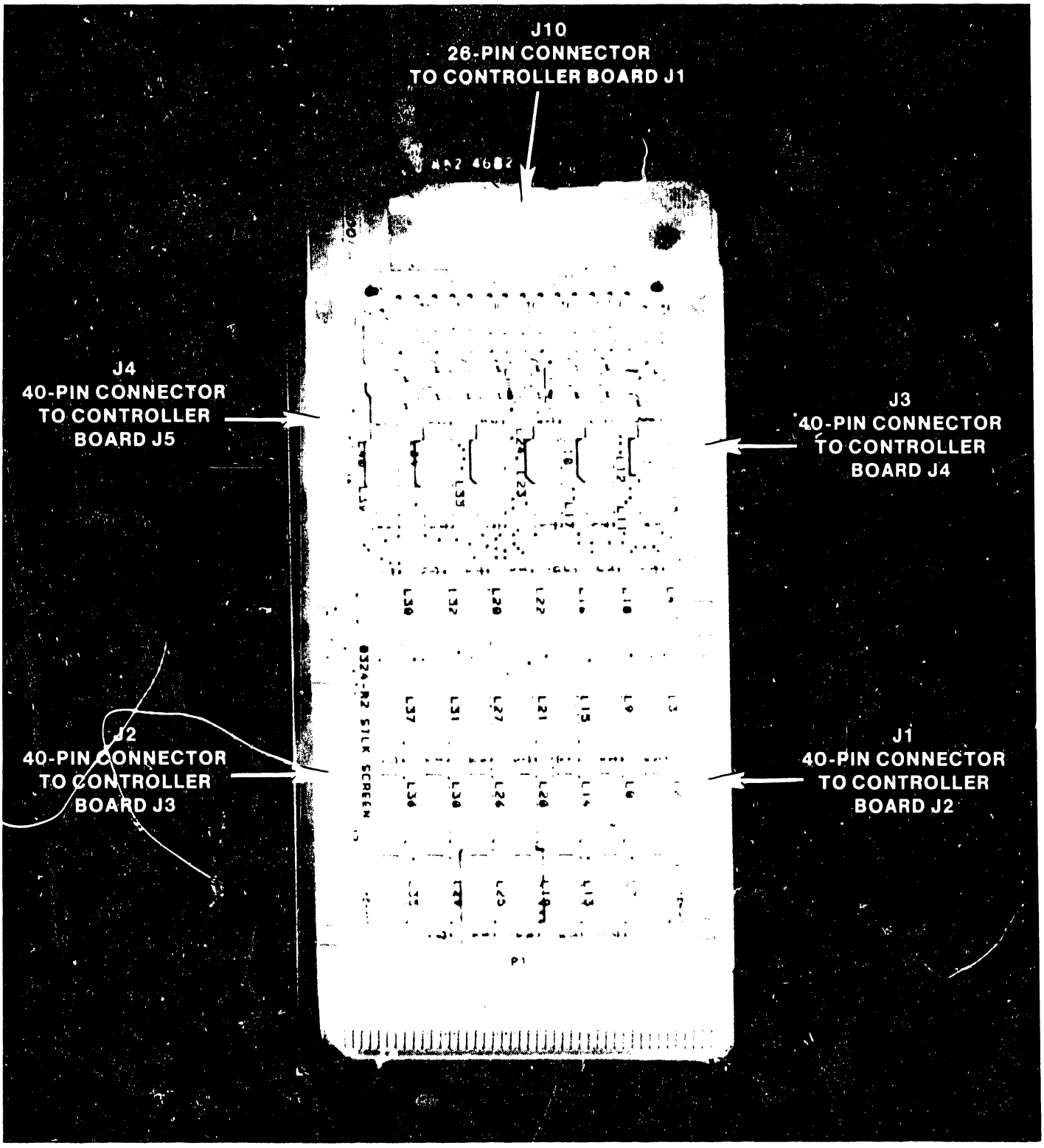


Figure K-7. Async Rear Panel Assembly (210-8324 Daughterboard Side)

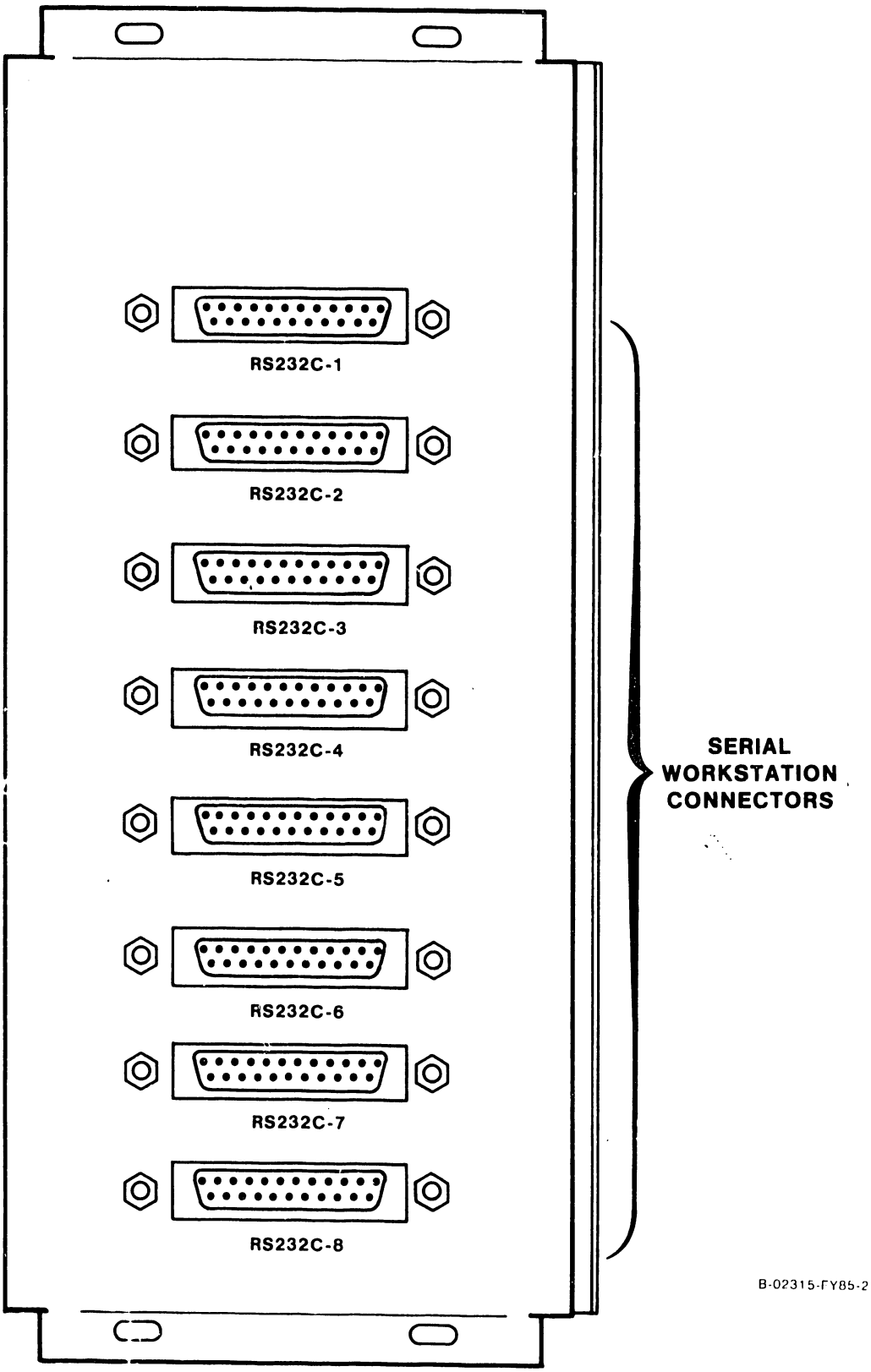


Figure K-8. Async Rear Panel Assembly (Connector Side)

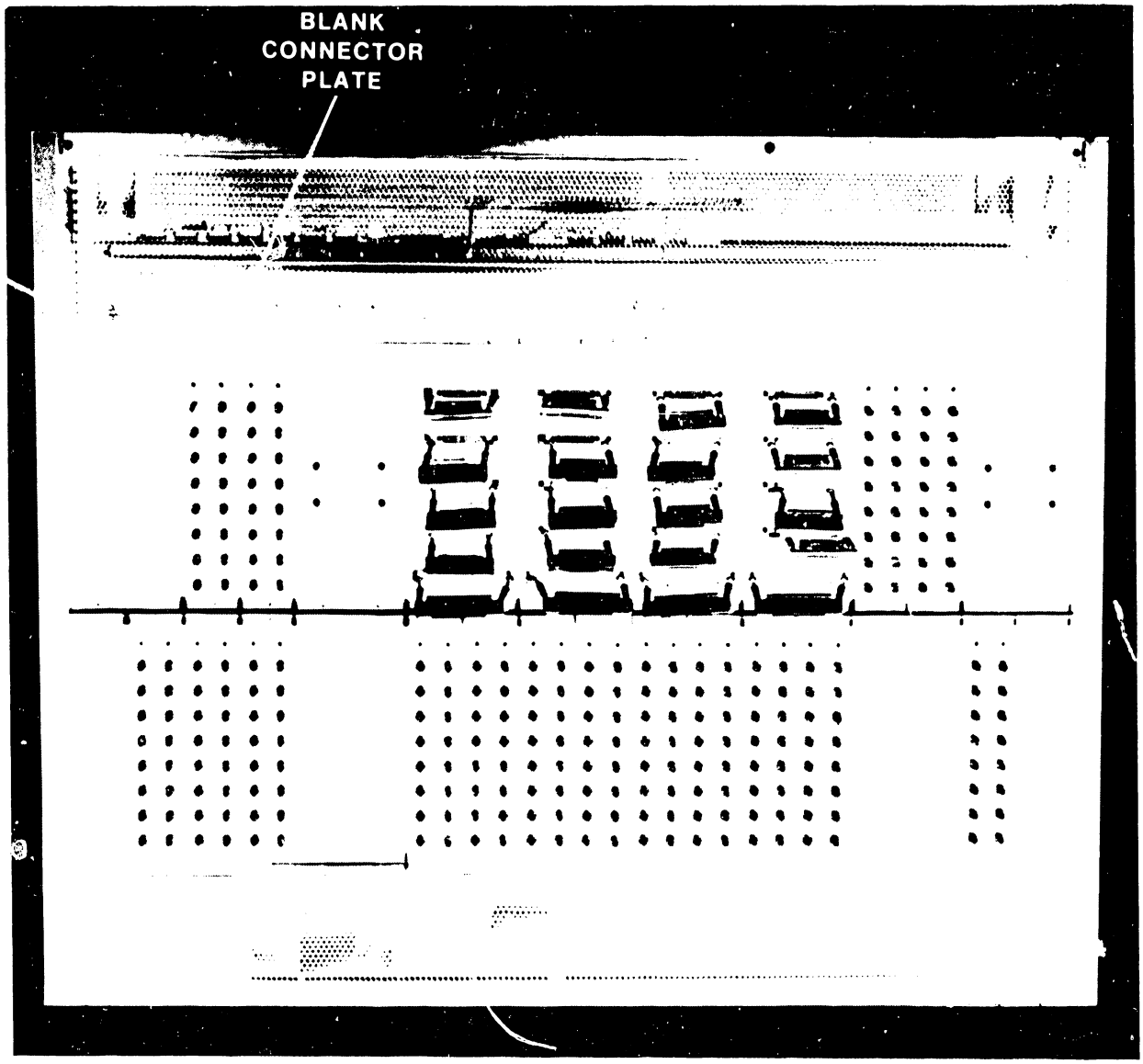
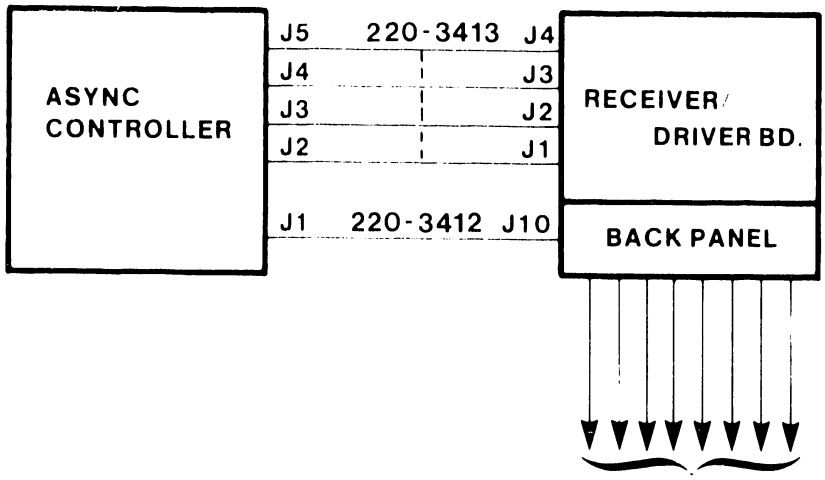


Figure K-9. Blank Connector Plate for Rear Panel Installation

7. Connect the cables as shown in figure K-10.



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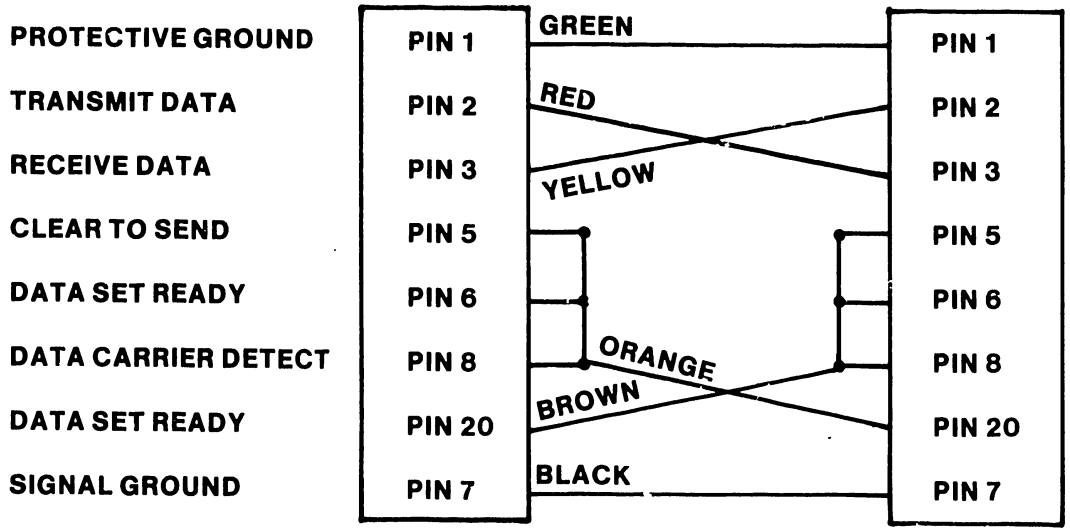

RS232 INTERFACE TO 2110 WORKSTATION

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Figure K-10. Cable Connections

8. Connect all workstations.
9. Power on the mainframe and check the -12 Volt supply on the 7826 TC Motherboard as follows:
   a. Connect the negative lead of a digital voltmeter to the -12 Volt test point and the positive to the ±0 Volt bus. (See figure K-4.)
   b. Adjust trimpot (figure K-4) until the meter reads -12 V ±0.5 V.

K.5.5 SYSTEM CHECKOUT

1. Power up the system.
2. Load microcode and IPL the system.
3. Power on all peripherals.
4. Ensure that all workstations configured through the Async Controller display the logon screen.
5. Ensure that logon is possible from each workstation.
6. Turn the system over to the customer.

K.6 PREVENTIVE MAINTENANCE

There is no preventive maintenance for the VS-100 Async Device Controller.

K.7 CORRECTIVE MAINTENANCE

Corrective maintenance for the VS-100 ADC consists of removal and replacement of defective parts.

K.7.1 ASYNC CONTROLLER BOARD ASSEMBLY REMOVAL AND REPLACEMENT

1. Power down the mainframe.
2. Remove the top cover.
3. Remove the cables from the top of the controller board.
4. Lift the TCP/IOP/Controller Board assembly straight up and out of the card cage.
5. To replace the Controller Board, reverse the removal procedure.
6. Power on the mainframe and check the -12 Volt supply on the 7826 TC Motherboard as follows:
   a. Connect the negative lead of a digital voltmeter to the -12 Volt test point and the positive to the ±0 Volt bus. (See figure K-4.)
   b. Adjust the trimpot (figure K-4) until the meter reads -12 V ±0.5 V.

NOTE

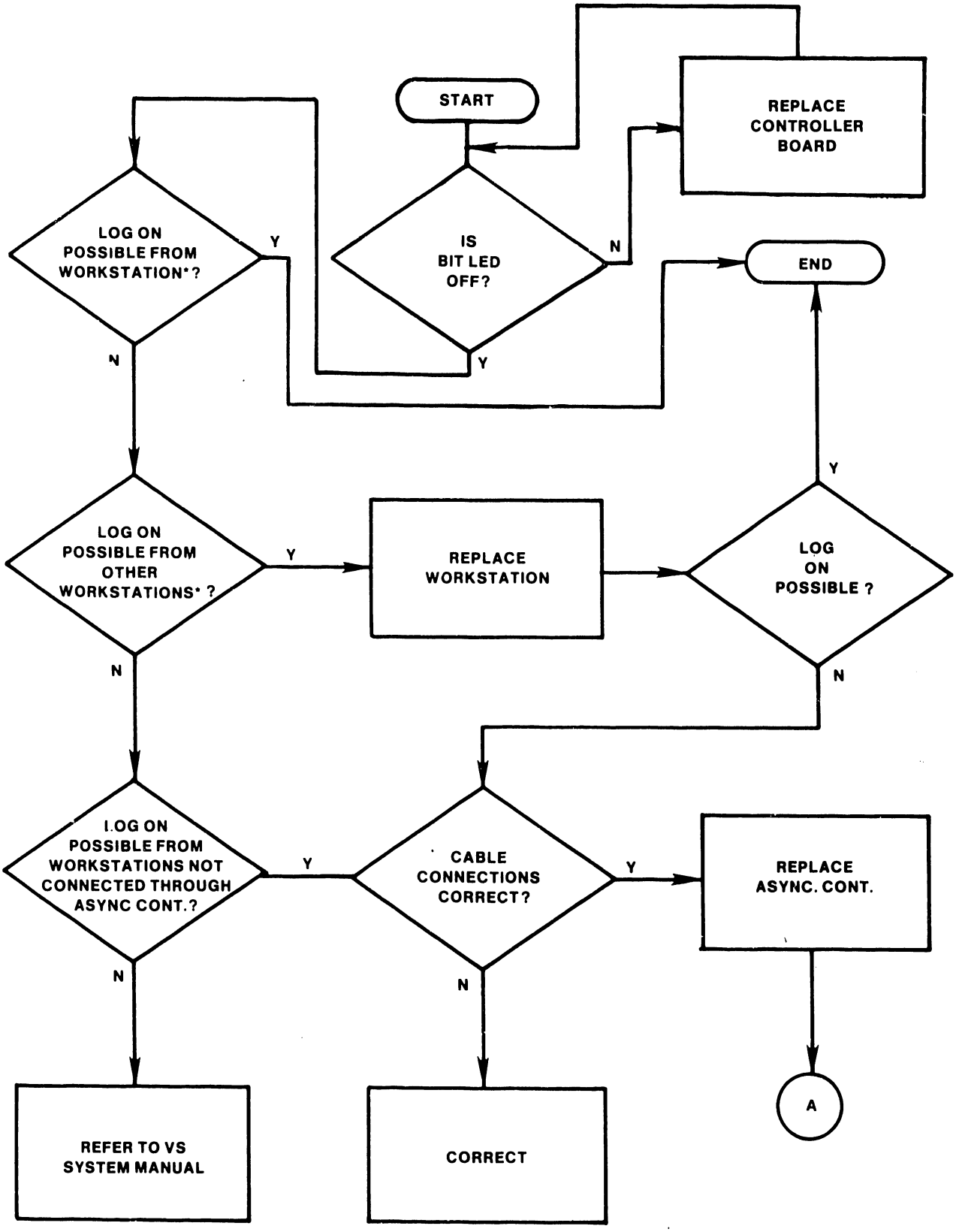
The system power supply must be adjusted to -13.6 V to obtain the necessary -12 V on the TC board.

K.7.2 REAR PANEL ASSEMBLY REMOVAL AND REPLACEMENT

1. Power down the mainframe.
2. Remove the top cover.
3. Remove the cables from the Line Driver/Receiver Daughterboard and Motherboard of the rear panel.
4. Remove and save the hardware securing the Rear Panel to the mainframe.
5. To replace the Async Rear Panel Assembly, reverse the removal procedure.

K.8 TROUBLESHOOTING THE ADC

This paragraph describes, in flow chart form, procedures for fault isolation in the VS-100 Async Device Controller. Refer to the flow chart in figure K-11.



* DENOTES DEVICE CONFIGURED THROUGH THE ASYNC CONTROLLER

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Figure K-11. ADC Troubleshooting Flow Chart (Sheet 1 of 2)

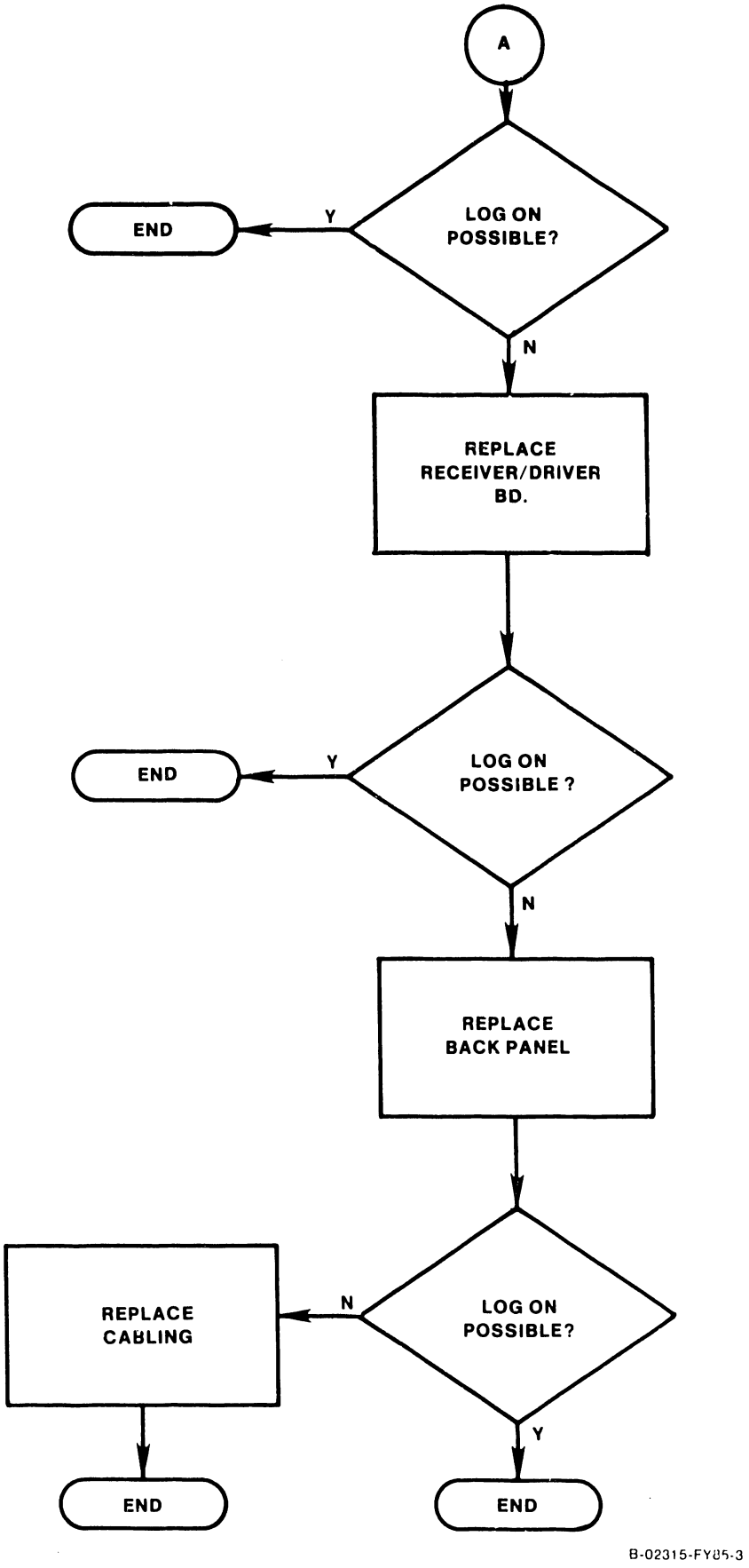


Figure K-11. ADC Troubleshooting Flow Chart (Sheet 2 of 2)

K.9 FIELD REPLACEABLE UNITS

The following table lists the field replaceable units (FRUs) for the VS-100 Async Device Controller.

Table K-2. VS-100 ADC Field Replaceable Units

WLI P/N	DESCRIPTION	FRU
220-0521	25-ft 2110 Workstation Cable	CBL
120-2381-01	50-ft 2110 Workstation Cable	CBL
120-2381-02	100-ft 2110 Workstation Cable	CBL
120-2381-03	500-ft 2110 Workstation Cable	CBL
120-2381-04	1000-ft 2110 Workstation Cable	CBL
120-2381-05	2000-ft 2110 Workstation Cable	CBL
210-8324	Driver/Receiver Daughterboard	PCB
212-3104	Async Controller	ASSY
220-0113	12-ft RS-232-C TC Cable	CBL
220-0219	25-ft RS-232-C TC Cable	CBL
220-0220	50-ft RS-232-C TC Cable	CBL
220-3412	26-pin Ribbon Cable	CBL
220-3413	40-pin Ribbon Cable	CBL
272-0043	Async Rear Panel Assembly	ASSY

APPENDIX
L
VS-100 CDC
VIRTUAL MACHINE OPERATING SYSTEM

APPENDIX L

CDC VIRTUAL MACHINE

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

CHAPTER L1

INTRODUCTION

L1.1 SCOPE AND PURPOSE

This Addendum provides installation and maintenance information for the CDC Virtual Machine Operating System. This material is designed to supplement the standard Product Maintenance Manual for the VS-90/100 Computer Systems.

> NOTE
> Throughout the remainder of this document, the CDC Virtual Machine Operating System will be refered to as CDC/VM. Also, although the CDC/VM Operating System is supported on several members of the VS family (VS-85, VS-90 and VS-100), this document will only make reference to VS-90 and VS-100 systems.

L1.2 RELATED DOCUMENTATION

A complete listing of Wang technical documentation is presented in the Technical Documentation Catalog/Index (742-0000). Other product documentation is identified in the Corporate Resource Catalog (700-7647).

L1.3 SYSTEM DESCRIPTION

The CDC Virtual Machine Operating System, developed for WANG VS systems by Control Data Corporation, allows a physical VS computer to be divided into a number of subsystems. It does this by allowing multiple operating systems to run concurrently from the same physical VS system, making this single system appear to be two or more machines.

With each user choosing a different operating system, an installation running CDC/VM on one VS system appears to be running many separate computer systems, each with different capabilities.

New or existing VS-90/100 systems can be upgraded to run CDC/VM, with only a few minor changes to the standard VS. A new B-Bus board, new Control Memory board, and a Floppy Disk Controller Prom, along with appropriate system microcode is required in this upgrade.

CDC/VM will be marketed exclusively by Control Data Corporation, with service to be performed by Wang Customer Engineers.

CHAPTER L2

INSTALLATION

L2.1 SCOPE

This chapter describes the procedures for unpacking, inspecting, and installing the various components required for operation of CDC/VM. Included in this chapter are instructions for initial power-up and checkout.

Actual installation should not begin until the site requirements detailed in the appropriate VS Product Maintenance Manual.

L2.2 SPECIAL TOOLS AND TEST EQUIPMENT

All tools and test equipment required for maintaining the VS systems are listed in the VS-100 Product Maintenance Manual. No special tools or test equipment are needed to maintain a VS system with CDC/VM installed.

L2.3 UNPACKING

1. Before unpacking any PC boards when field installing this option, check all packing slips to make sure that the proper equipment has been delivered.

2. After checking packing slips, inspect all shipping containers for damage (crushed corners, punctures, etc.).

3. If damage is discovered during inspection, file an appropriate claim promptly with the carrier involved, and notify your supervisor.

NOTE

For VS system unpacking instructions please refer to Chapter 3 of the VS-100 Product Maintenance Manual.

L2.4 INSPECTION

1. Inspect all PC boards for packing material or such shipping damage as broken connectors.

2. If damage is discovered during the inspection, follow the aforementioned reporting procedure.

L2.5 INSTALLATION

NOTE

The following procedure applies only to the field installation of the CDC/VM option. For VS System Installation Instructions please refer to Chapter 3 of the VS-100 Product Maintenance Manual.

L2.5.1 Field Installation of the CDC/VM option

1. Insure all users have logged off and remove power from the system.
2. Remove the covers from the system as shown in Chapter 7 of the VS-100 Product Maintenance Manual.
3. Following the removal procedure in Chapter 7 of the VS-100 maintenance manual, remove the "B" Bus Board from slot 3 of the Motherboard.
4. Insert the new "B" Bus Board (Ref. Fig. L2-1) into slot 3.
5. Following the removal procedure in Chapter 7 of the VS-100 maintenance manual, remove the Control Memory Board from slot 1 of the Motherboard.
6. Insert the new Control Memory Board (Ref. Fig. L2-2) into slot 1 of the Motherboard.
7. Following the removal procedure in Chapter 7 of the VS-100 maintenance manual, remove the Minifloppy Drive from the system.
8. Remove the Microcode Prom from location L10 of the Minifloppy Drive Controller Board and replace it with the new Microcode Prom P/N 378-3219. (Ref. Fig. L2-3.) Installation of this Prom changes the Minifloppy Drive Controller Board part number to 210-7610-1A.
9. Reinstall the Minifloppy Drive into the system following the procedure outlined in Chapter 7 of the maintenance manual.
10. Install the covers on the system (Ref. Chapter 7 of the VS-100 Product Maintenance Manual.)
11. Apply Power to the Machine and follow the system checkout procedures found in Chapter 3 of the VS-100 Product Maintenance Manual.
12. The following Microcode Diagnostics must be run to verify the B Bus board and the Control Memory Board. (Ref. Chapter 8 of the Product Maintenance Manual.)

T9110	Data Stack and T-RAM
T6110	CM Moving Inversions (upper 8K)
T7110	CM Moving Inversions (lower 4K)

13. After successful completion of these procedures, the system may be turned over to the customer in accordance with Chapter 3 of the Product Maintenance Manual.

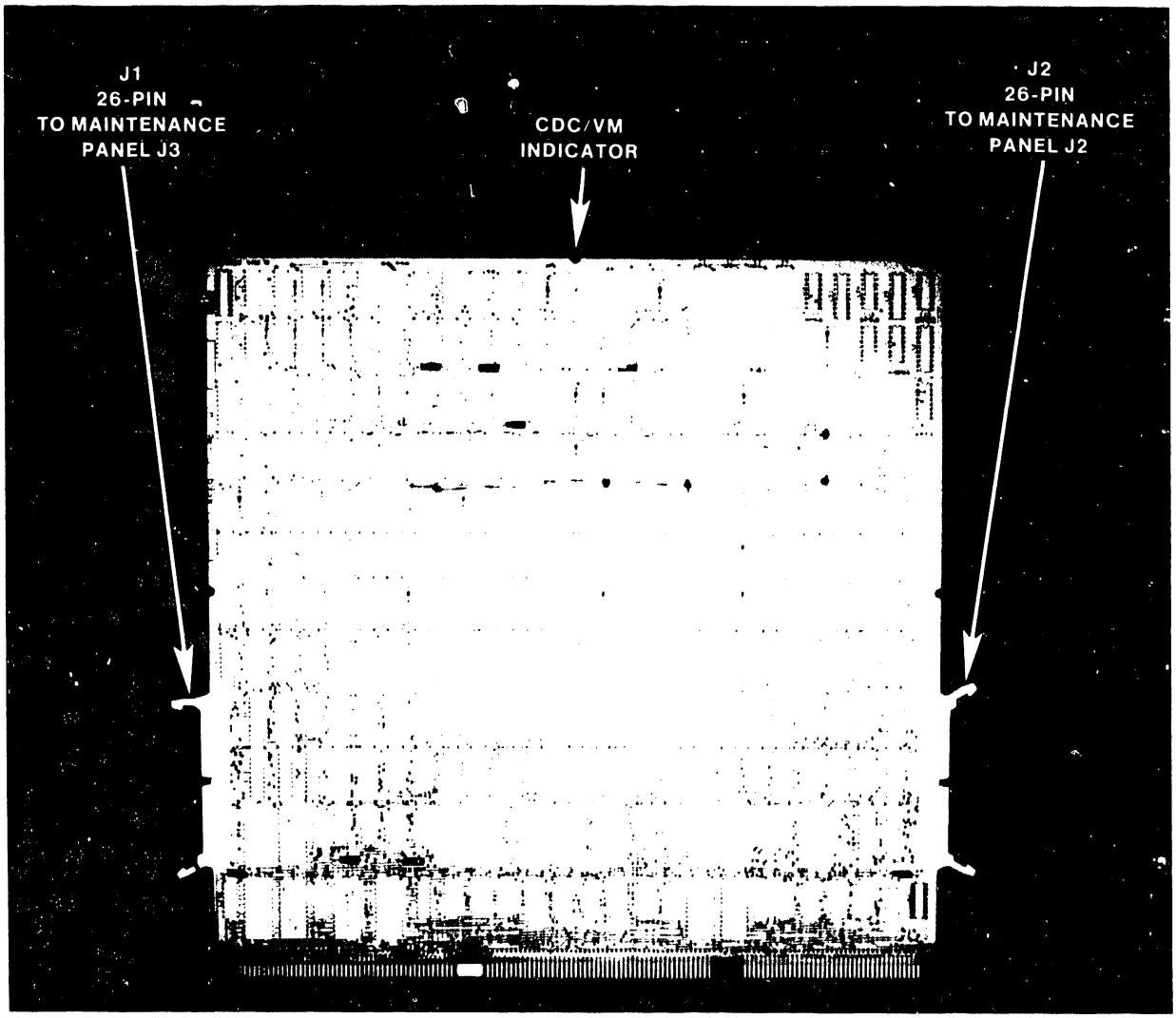


Figure L2-1 "B" Bus Board
210-8569

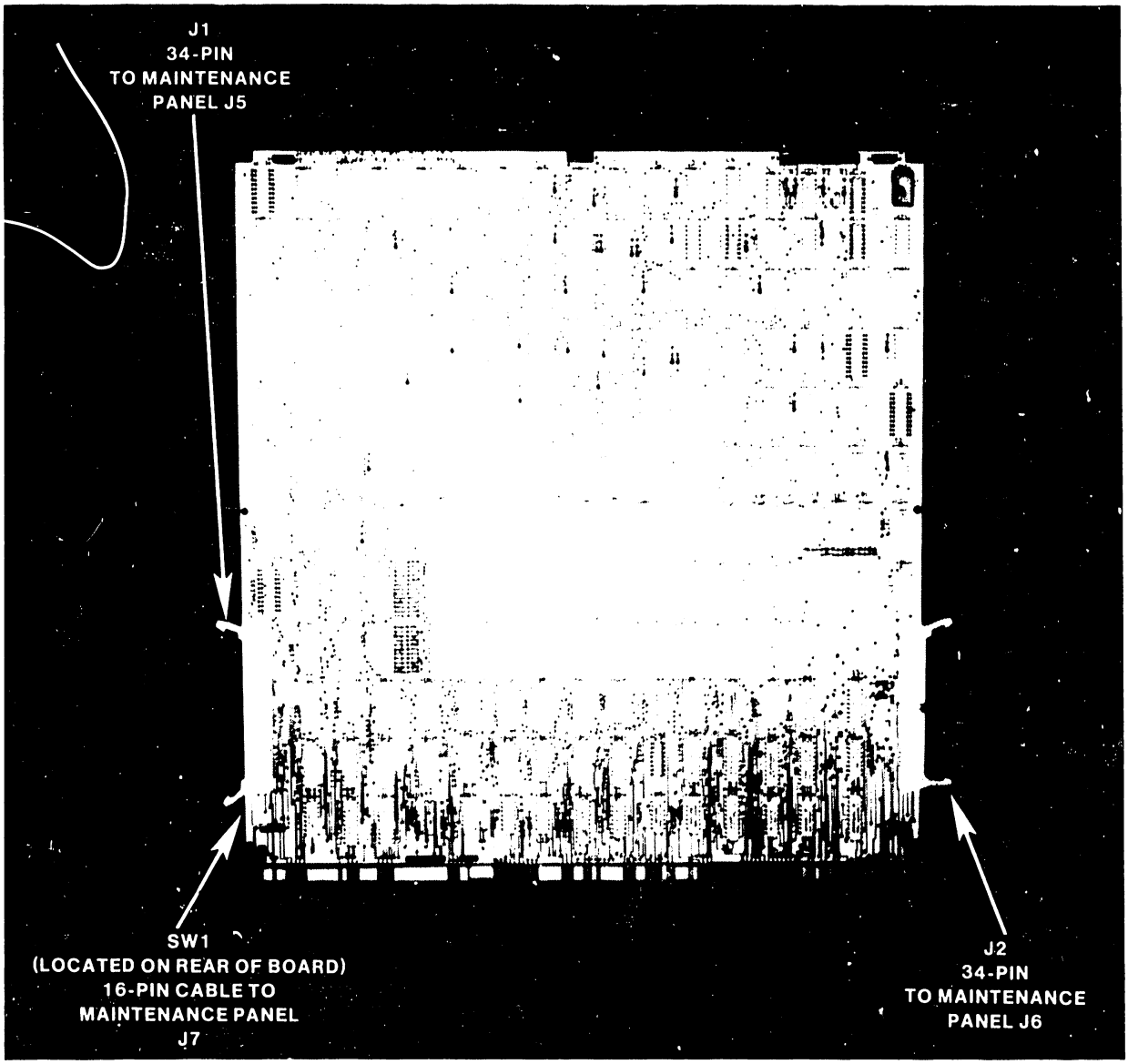


Figure L2-2 Control Memory Board
210-8204-1A

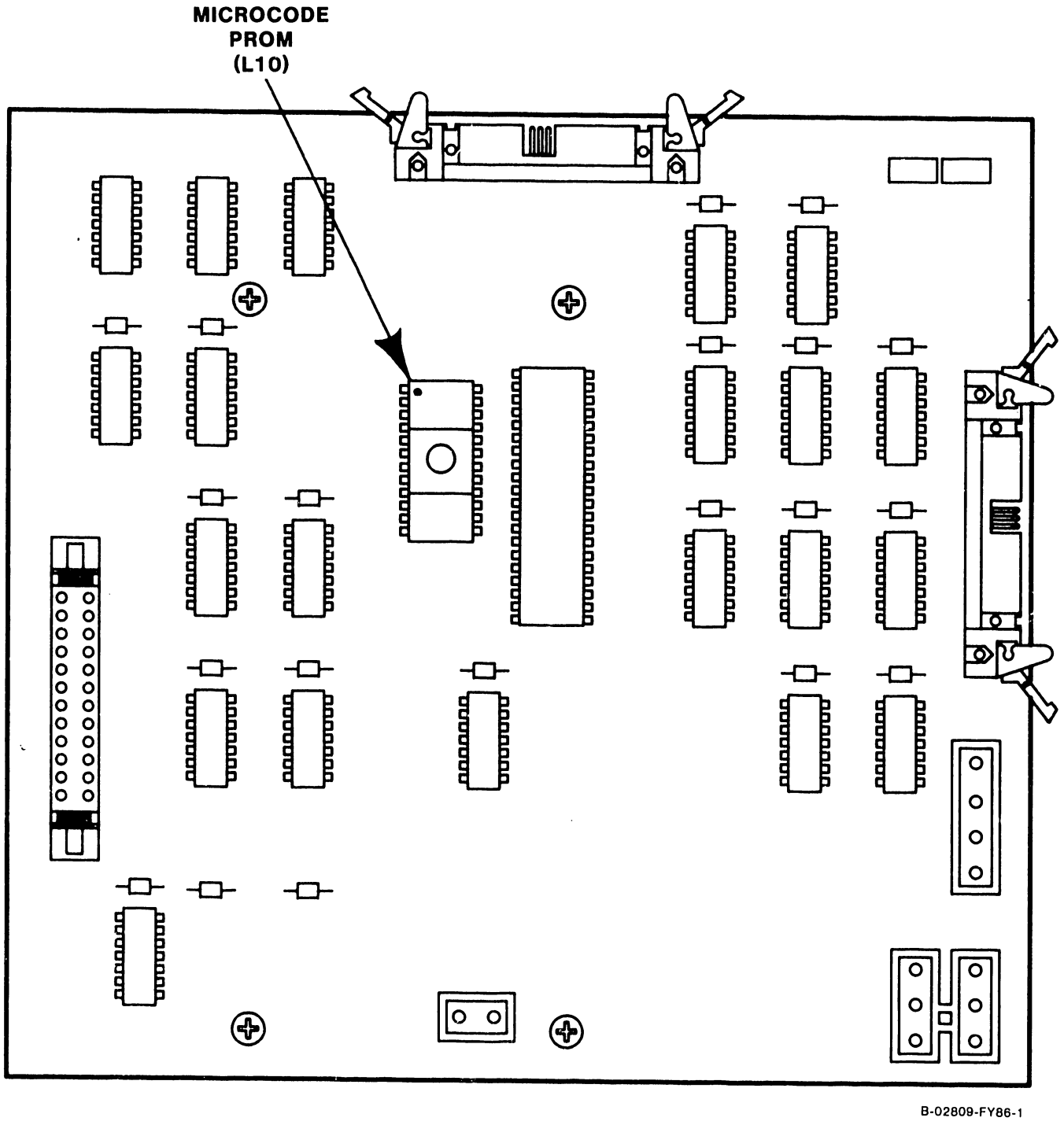


Figure L2-3 Minifloppy Drive Controller Board
210-7610-1A

CHAPTER L3

ILLUSTRATED PARTS BREAKDOWN

L3.1 SCOPE

This chapter contains the illustrated parts breakdown for the hardware components used with the CDC/VM. Use this breakdown for part number identification when ordering field replaceable items.

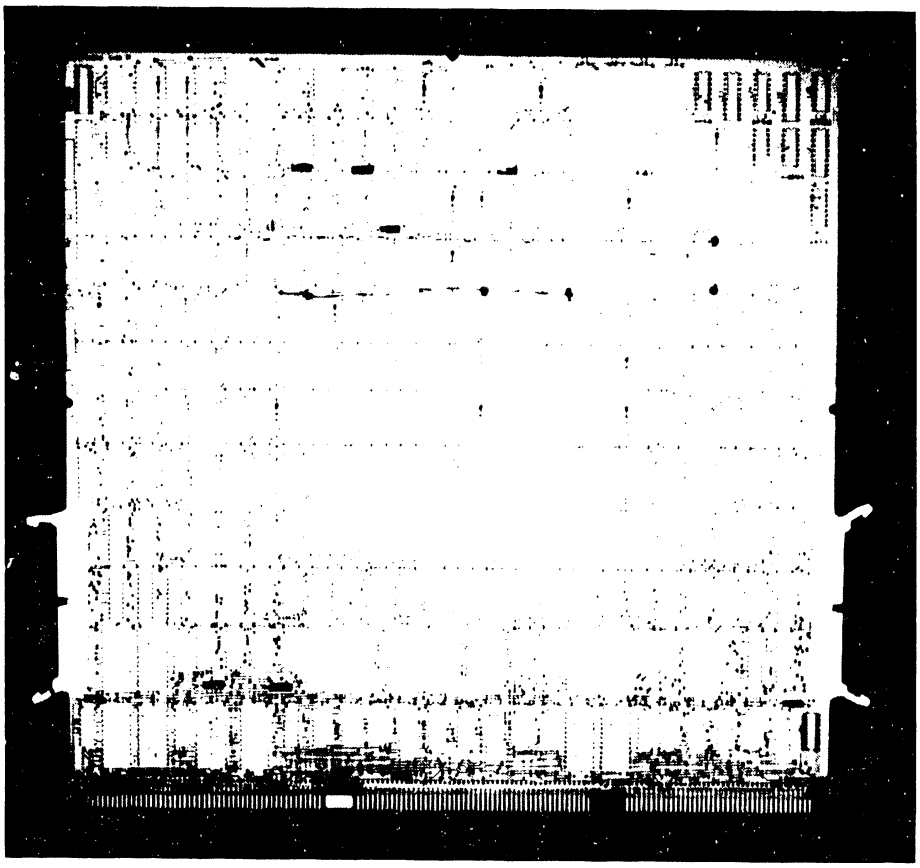


Figure L3-1 "B" Bus Board
210-8569

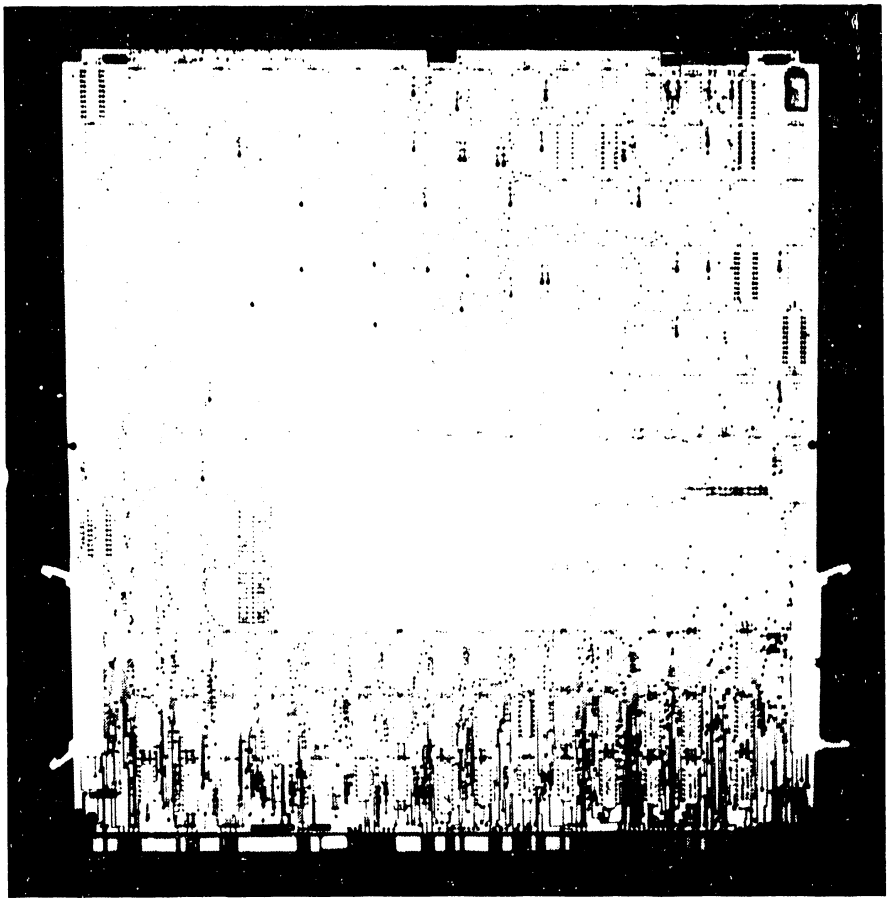


Figure L3-2 Control Memory Board
210-8204-1A

CHAPTER L4

TROUBLESHOOTING

To troubleshoot VS systems equipped with the CDC Virtual Machine Operating System, follow the procedures outlined in Chapter 8 of the VS-100 Product Maintenance Manual. The Microcode Diagnostics listed below specifically test the components required by CDC/VM.

T9110	Data Stack and T-RAM
T6110	CM Moving Inversions (upper 8K)
T7110	CM Moving Inversions (lower 4K)

Verify also that when running CDC/VM, the CDC/VM indicator on the "B" Bus board (see Fig. L2-1) is pulsating off and on. This light indicates memory address translation activity. The light is on when address translation is not in use. Thus, under normal virtual machine operating conditions, the light will never remain continuously on or off.

APPENDIX
M
4 MEGABYTE
MAIN MEMORY
BOARD

APPENDIX M

4 MEGABYTE MAIN MEMORY BOARD

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER M1

INTRODUCTION

M1.1 SCOPE AND PURPOSE

This Addendum to the VS-100 Computer System Product Maintenance Manual provides instructions to increase the main memory capacity of the present VS-100 from either 8MB to 12MB or 12MB to 16MB by installing new 210-8603 Main Memory Boards, replacing the original system motherboard with a modified motherboard, and installing/replacing 210-8570-A cache memory. By using this upgrade in conjunction with the present memory boards available, the VS-100 will now support memory configurations of 2, 4, 8, 12, or 16MB of main memory.

NOTE

VS-90 systems may be upgraded with this memory, but must first be upgraded to a VS-100.

M1.2 RELATED DOCUMENTATION

A complete listing of Wang technical documentation is presented in the Technical Documentation Catalog/Index (742-0000). Other product documentation is identified in the Corporate Resource Catalog (700-7647).

M1.3 MODEL DESCRIPTION

The 210-8603 Main Memory Board is equipped with 256K RAM chips. The population of these chips on the board account for the three possible memory configurations available.

The model structure for the main memory option is as follows:

P/N	MEMORY CAPACITY
210-8603-1	1MEG
210-8603-2	2MEG
210-8603-3	4MEG

M1.4 SOFTWARE REQUIREMENTS

Software Operating System release 6.40.xx or above, and CP microcode 4.59.01 are required to support operation of the 12 and 16 Meg system configurations. Previous operating systems will support the memory boards in configurations of 8 Meg or less.

M1.5 VS-100 MEMORY UPGRADE KITS

Table M1-1 below, shows the various memory configurations now in the field, and lists the appropriate Wang update kits which must be installed to bring the total system memory to a supported memory configuration (2, 4, 8, 12, or 16 Meg).

NOTE

Configurations which currently contain less than 2MB must first upgrade to 2MB, and then order the appropriate upgrade from that point

Current Total System Memory	Wang UJ Kit Required for Memory Upgrade				
	2 Meg	4 Meg	8 Meg	12 Meg	16 Meg
512 K	UJ-3401				
768 K	UJ-3402				
1 Meg	UJ-3403				
1.25 Meg	UJ-3404				
1.5 Meg	UJ-3405				
1.75 Meg	UJ-3406				
2 Meg		UJ-3407	UJ-3409	UJ-3415*	UJ-3422*
3 Meg		UJ-3408	UJ-3410	UJ-3416*	UJ-3423*
4 Meg			UJ-3411	UJ-3417*	UJ-3424*
5 Meg			UJ-3412	UJ-3418*	UJ-3425*
6 Meg			UJ-3413	UJ-3419*	UJ-3426*
7 Meg			UJ-3414	UJ-3420*	UJ-3427*
8 Meg				UJ-3421*	UJ-3428*
12 Meg					UJ-3429*

* Requires the above UJ kit, as well as UJ-3380 which contains a R3 motherboard, 210-8570-A cache memory, and extra hardware.

Table M1-1 VS-100 Memory Upgrade Kits

CHAPTER M2

INSTALLATION

M2.1 GENERAL

This chapter presents information for unpacking, inspecting and installing the 4 megabyte main memory board and the modified system motherboard into the VS-100 Computer System. This section also contains a listing of the jumper differences between the existing system motherboard and the modified motherboard, as well as instructions for memory configuration switch and jumper settings required to support the 4 meg memory board. General information concerning VS-100 installation can be found in Chapter 3 of this Product Maintenance Manual.

M2.2 UNPACKING AND INSPECTION

The 4 megabyte main memory board and system motherboard are packed in shipping cartons as shown in figure M2-1. Refer to figure M2-1 while performing the procedure given below.

1. Before unpacking the PC boards, inspect the shipping cartons for damage. If any damage is noticed, notify the carrier and your supervisor immediately.

2. Using a sharp knife, carefully cut the shipping tape used to secure the cartons. Carefully open the cartons and save all packaging material for reshipment, if necessary.

3. Check the contents against the shipping bill to ensure that nothing is missing or damaged.

4. Inspect the boards for shipping damage (broken connectors, etc.).

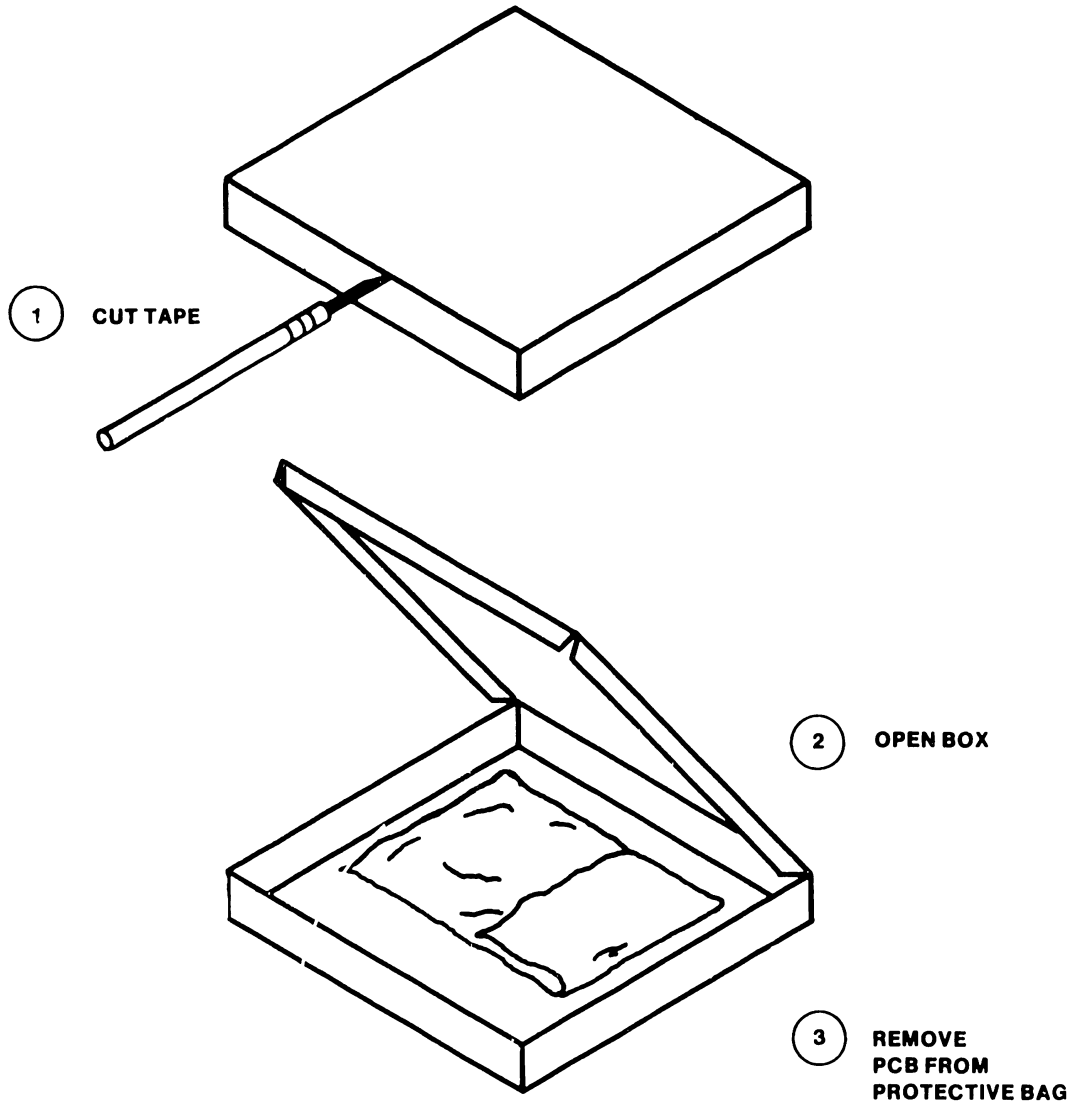


Figure M2-1 Unpacking the PC Boards

M2.3 MEMORY CONFIGURATIONS

The 4 megabyte main memory board is available in 3 memory configurations (1, 2, or 4 Meg). The memory configuration is determined by the population of 256K memory chips (377-0589) present on the board. Figure M2-2 depicts the memory chip loading configurations and associated chip part numbers.

M2.4 JUMPER SETTINGS

M2.4.1 Cache Memory Board Switch and Jumper Settings

The 210-8570-A cache memory board used on VS-100 systems is equipped with memory configuration jumpers and switches which must be set for proper system operation. Figures M2-3 and M2-4 show the location and proper settings for the jumpers and memory switches on the 210-8570-A board. Refer to these figures while performing the procedure given below.

1. Power down the VS-100 by pressing the ac power on/off rocker switch to the 0 position.

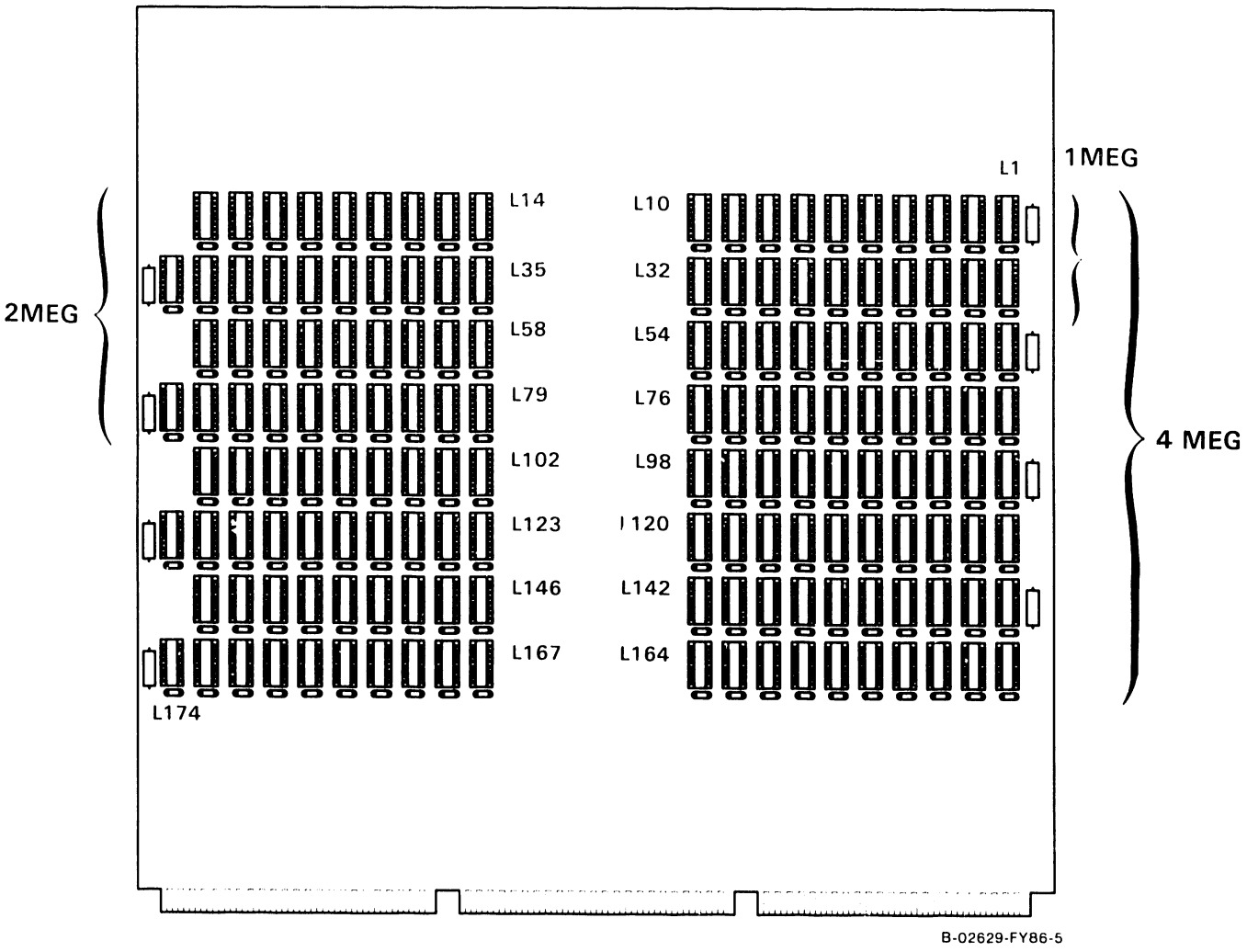
2. Following the procedure given in Chapter 7 of the VS-100 maintenance manual, remove the cache memory board from the system.

3. Refering to the figures listed above, set the memory configuration jumpers to reflect the largest memory board to be installed into the system, and set the memory configuration switches, in combination if necessary, to reflect the total amount of system memory to be installed.

4. Following the procedure given in Chapter 7 of the VS-100 maintenance manual, reinstall the cache memory board into the system.

M2.4.2 Main Memory Board Jumper JP1 Settings

JP1 on the main memory board contains three pins . With the board held connector edge down, Pin 1 is located on the top, pin 2 in the center, and pin 3 on the bottom. Manufacturing will install a shunt connecting pins 1 and 2. In no case should this shunt be moved in the field.



4 Megabyte Main Memory Chip Loading

210-8603-1 (1M)	377-0589 Chips in locations	L1-L10, L14-L32, L35-L44
210-8603-2 (2M)	377-0589 Chips in locations	L1-L10, L14-L32, L35-L54, L58-L76, L79-L88
210-8603-3 (4M)	377-0589 Chips in locations	L1-L10, L14-L32, L35-L54, L58-L76, L79-L98, L102-L120, L123-L142, L146-L164, L167-L174

Figure M2-2 4 Meg Memory Board Chip Loading

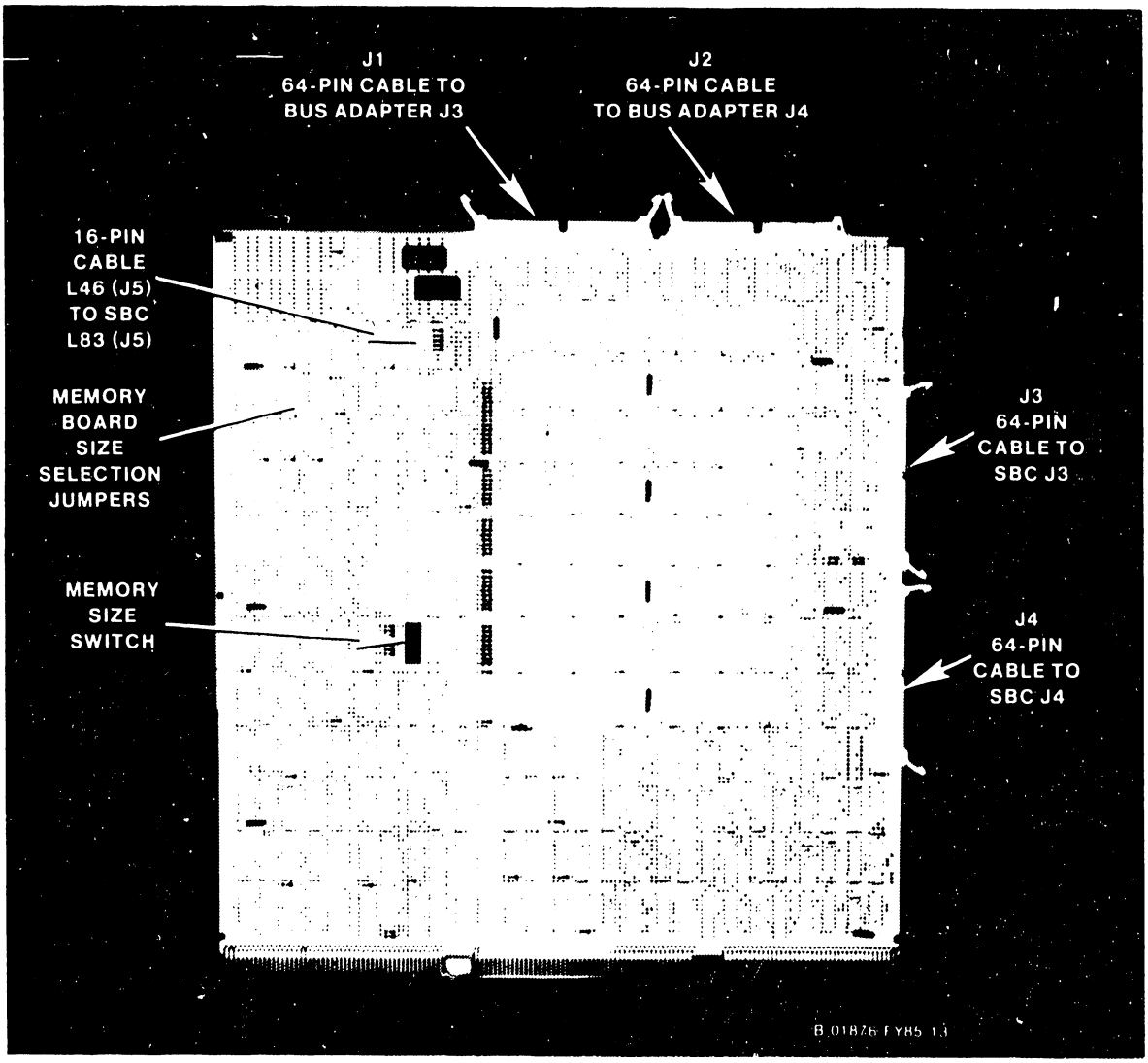
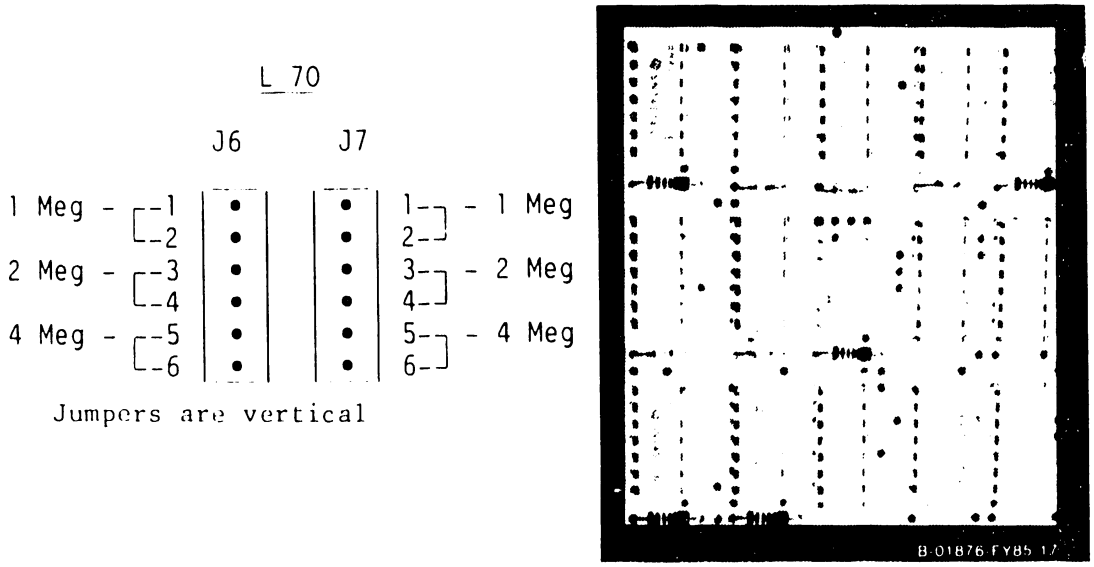
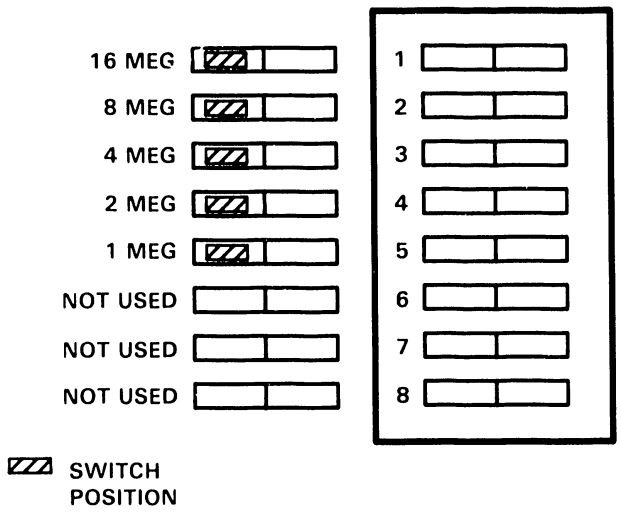


Figure M2-3 VS-100 Cache Memory Board
210-8570-A



JUMPER SETTINGS
(REFLECTS THE LARGEST CAPACITY MEMORY BOARD TO BE INSTALLED IN THE SYSTEM)



SW1 SWITCH SETTING
(REFLECTS THE TOTAL SYSTEM MEMORY CAPACITY)

Figure M2-4 VS-100 Cache Memory Board Jumper and Switch Settings

M2.5 MODIFIED SYSTEM MOTHERBOARD AND 4 MEG MAIN MEMORY BOARD INSTALLATION

1. Power down the VS-100 by pressing the ac power on/off rocker switch to the 0 position. Remove the ac power cable from its outlet, and remove the top cover.

2. Check revision level of existing motherboard. If board is marked R3 on the component side of the board, left of the control memory, proceed to step 7.

3. Carefully remove all boards from the system's CPU section (ref. Chapter 7 of the VS-100 Product Maintenance Manual).

4. Remove the system motherboard from the unit (see Chapter 7 of the VS-100 Product Maintenance Manual).

5. Carefully install the modified system motherboard from UJ-3380, into the unit.

6. Install PC boards removed in step 3 into the system.

7. Verify cache memory jumper and switch configurations, and memory size.

8. Install new memory boards as required for system configuration, reinstall the top cover, plug the AC power cable into its outlet, and power up the CPU.

NOTE

Memory boards must be installed in pairs, with the largest pair installed in the first two slots. For example, a memory upgrade to 12MB would require installation of two 4MB and two 2MB memory boards. The two 4MB boards would be installed in the first two slots, followed by the two 2MB boards.

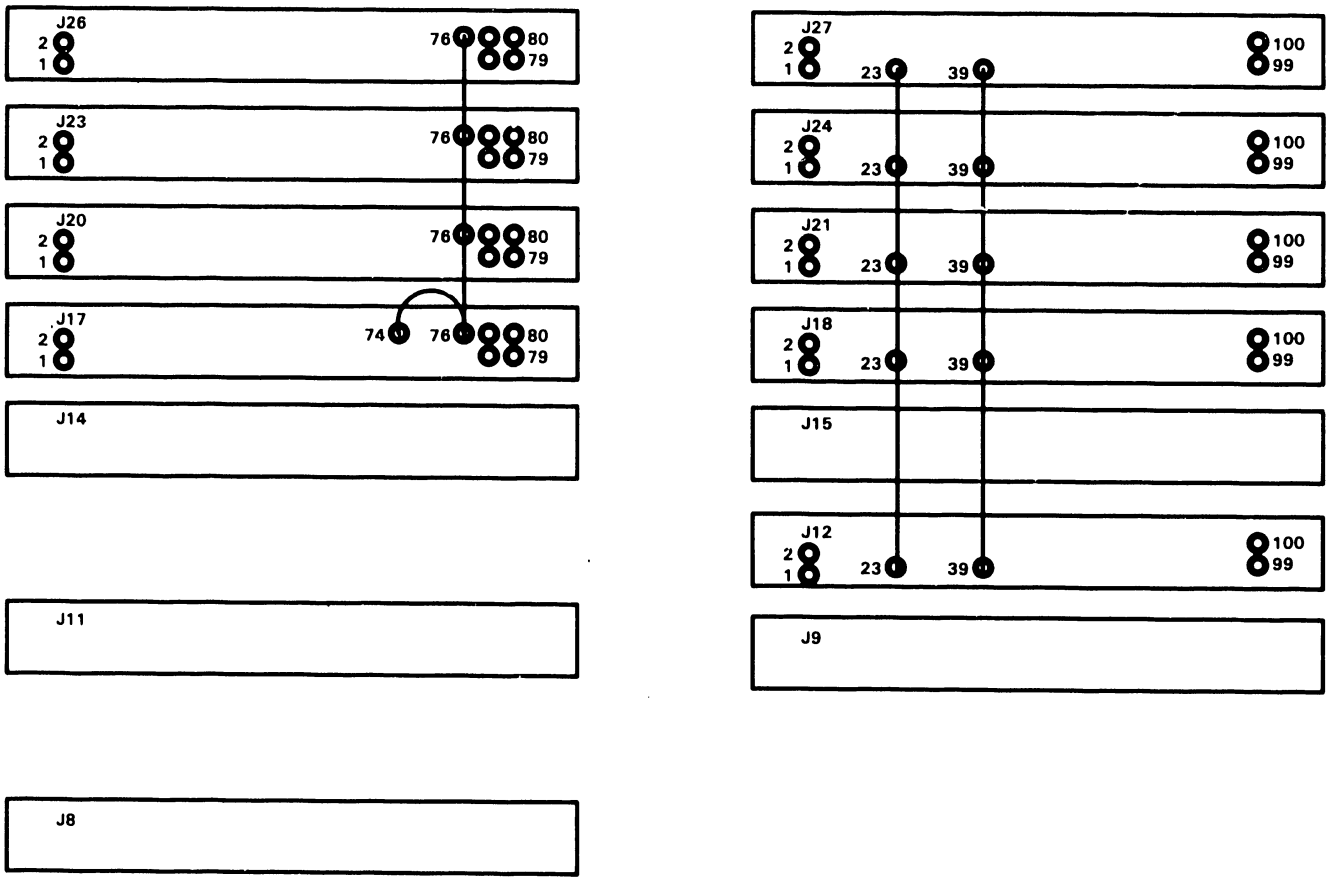
9. Run Diagnostics (see Chapter 8 of the VS-100 Product Maintenance Manual) to verify correct system operation.

M2.6 MODIFIED SYSTEM MOTHERBOARD DESCRIPTION

The modified VS-100 motherboard (210-7608, R3) contains jumpers to accommodate the new memory configurations. These modifications must be incorporated into the motherboard for proper operation of the 2 megabyte and 4 megabyte memory boards. The jumpers for this modification are outlined in fig. M2-5.

M2.7 VS-90 MEMORY UPGRADES

As previously stated, VS-90 systems may be upgraded with this memory, but must first be updated to a VS-100.



a. Jumper J12 pin 23 to J18 pin 23, J21 pin 23, J24 pin 23, J27 pin 23.
b. Jumper J12 pin 39 to J18 pin 39, J21 pin 39, J24 pin 39, J27 pin 39.
c. Jumper J17 pin 74 to J17 pin 76, J20 pin 76, J23 pin 76, J26 pin 76.

The assembly will be marked Revision R3 on the component side of the board, left of the control memory.

Figure M2-5 Modified VS-100 Motherboard Wiring

CHAPTER M3

TROUBLESHOOTING

M3.1 GENERAL

Micro-diagnostic tests DA10 and DE10 are used to troubleshoot the 4 meg main memory board. The exact test which should be run is determined by the amount of main memory installed in the system. Use the table below to determine the test to be run with each configuration.

MAIN MEMORY INSTALLED IN SYSTEM	TEST TO BE RUN
2 Meg (Two 1 MB boards)	DE10
4 Meg (Four 1 MB boards)	DE10
8 Meg (Eight 1 MB boards)	DE10
8 Meg (Two 4 MB boards)	DA10
16 Meg (Four 4 MB boards)	DA10
12 Meg (Two 4 MB boards and two 2 MB boards)	Run DA10 on 8 Meg (Two 4 MB boards) then run DE10 on the remaining 4 Meg (Two 2 MB boards)

CHAPTER M4

ILLUSTRATED PARTS BREAKDOWN

M4.1 GENERAL

If defective, the entire 4 megabyte main memory board should be swapped out and replaced as a complete unit. The individual memory chips are not field replaceable units. The exact model number of the board to be replaced can be determined by the population of memory chips resident on the memory board as specified in figure M2-2. Model numbers of the memory board are as follows:

MODEL	SIZE
210-8603-1	1M
210-8603-2	2M
210-8603-3	4M

APPENDIX N

32 PORT SERIAL CONTROLLER BOARD

Appendix N

32 Port Serial Controller
22V47

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

CHAPTER N1

INTRODUCTION

N1.1 SCOPE AND PURPOSE

This Addendum provides installation and maintenance information for the Wang 32 Port Serial Controller IOP (212-3109). This material is designed to supplement the standard Product Maintenance Manual for the VS-100 Computer System.

N1.2 RELATED DOCUMENTATION

A complete listing of Wang technical documentation is presented in the Technical Documentation Catalog/Index (742-0000). Other product documentation is identified in the Corporate Resource Catalog (700-7647).

N1.3 FUNCTIONAL DESCRIPTION

The 32 Port Serial Controller is a modularized, Z-80 based, 32 port, 928 daughter board controller which mates with the 7826 TC IOP. It has a MUXBUS connection which will support connection of elements of the Modular 928 Serial I/O Subsystem, such as Electrical APAs. Resident on the board are 64Kx9 of DRAM, a Z-80 microprocessor, two Z-80 CTCs, two 9517 DMA Controllers, a discrete DMA controller, two 2Kx8 Static RAMs, and a diagnostic LED for BIT testing. (Ref. Fig. N1-1.)

N1.4 SOFTWARE REQUIRED

The 32 Port Serial Controller requires an Operating System of 6.40.xx or above to support the loading of microcode file @MC22V47, revision 7.05.02.

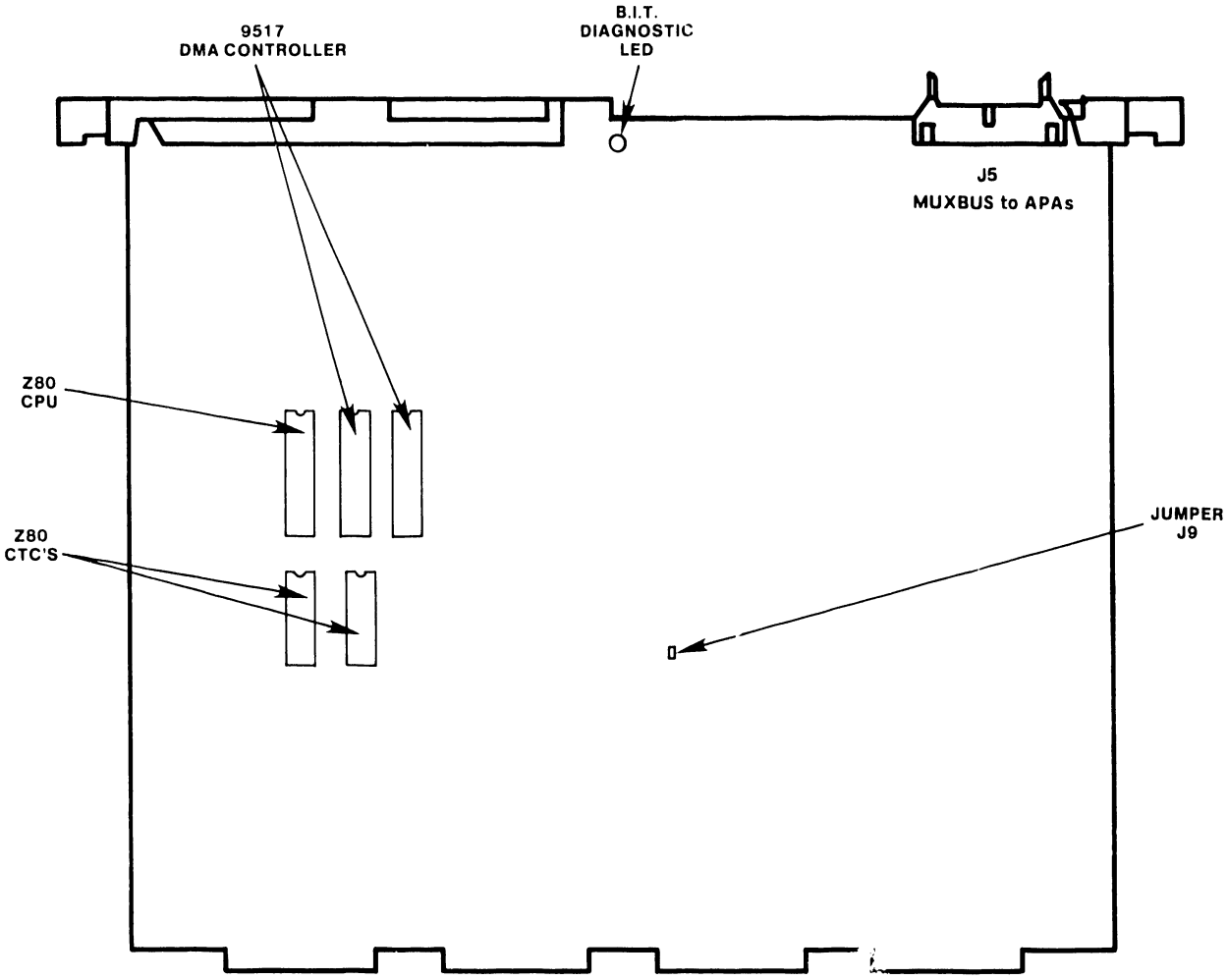


Figure N1-1 32 PORT SERIAL CONTROLLER BD.
212-3109

CHAPTER N2

INSTALLATION

N2.1 SCOPE

This chapter describes the procedures for unpacking, inspecting, and installing the 32 Port Serial Controller. Included in this chapter are instructions for interconnection and initial power-up. Actual installation should not begin until the site requirements detailed in the VS-100 Maintenance Manual have been met. If further information is required, refer to the VS-100 Computer System Product Maintenance Manual.

N2.2 SPECIAL TOOLS AND TEST EQUIPMENT

No special tools or test equipment are required for the installation and maintenance of the 32 Port Serial Controller.

N2.3 UNPACKING

1. Before unpacking the Controller Board check all packing slips to make sure that the proper equipment has been delivered.
2. After checking packing slips, inspect all shipping containers for damage (crushed corners, punctures, etc.).
3. Open the box and remove the PC Board as shown in Fig. N2-1.

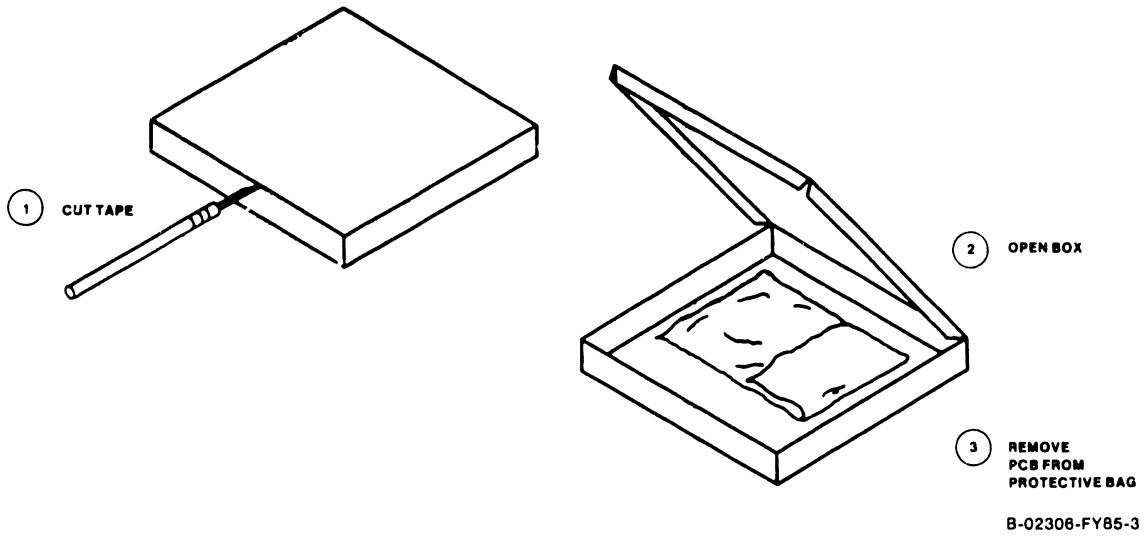


Figure N2-1 Unpacking the 32 Port Serial Controller Board

N2.4 INSPECTION

1. Inspect the Controller and associated cabling for packing material or such shipping damage as broken connectors.
2. If damage is discovered during the inspection, follow the reporting procedure in chapter 3 of the VS-100 Maintenance Manual.

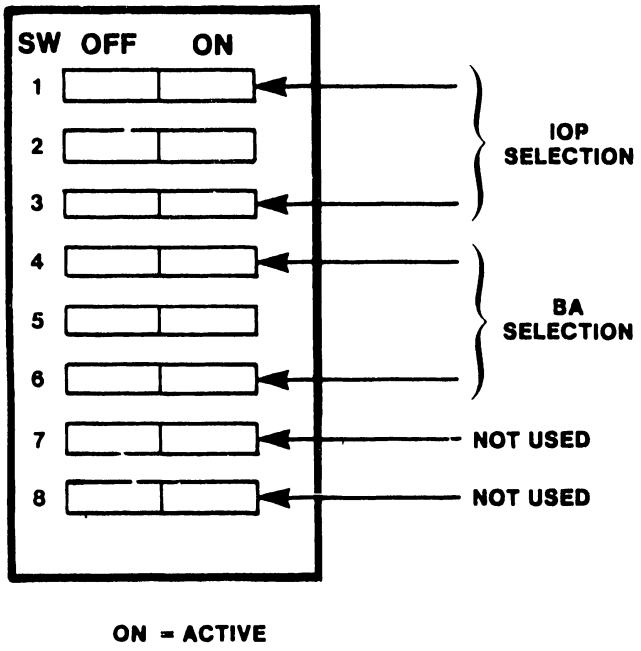
N2.5 INSTALLATION

1. Prior to installation, ensure that J9 pins 1 and 2 are jumpered together (ref. fig. N1-1). This jumper is not intended for field use and must be in at all times for proper operation of the controller.
2. Set the IOP motherboard switches as shown in figure N2-2.
3. With the system power off, insert the Controller Board into an available I/O Device Adapter slot by placing it in the board guides and lowering it to the Motherboard connector.
4. Make sure the board edge connectors are lined up with the motherboard connector, and insert the IOP.
5. Attach the CPU Interface Panel to the rear of the VS-100, in an available I/O panel.
6. Connect J5 of the controller to the CPU Interface Panel via a 34 pin ribbon cable.
7. Attach cable between the VS-100 and the VS Cable Concentrator.
8. Attach the VS Cable Concentrator to J1 of the 8 port active port assembly (APA). Reference figure N2-3.

NOTE

Up to 4 APA's may be daisy chained together to achieve a 32 port configuration. Refer to figure N2-3 for daisy chain configuration examples.

8. Connect serial peripherals to the APA(s) as required for proper system configuration.



SW NO.	1	2	3	IOP NO.
	0	0	0	0
	0	0	1	1
	0	1	0	2
	0	1	1	3
	1	0	0	4
	1	0	1	5
	1	1	0	6
	1	1	1	7

SW NO.	4	5	6	BA NO.
	0	0	1	1
	0	1	0	2

B-02729-FY86-2

Figure N2-2 Serial Controller IOP Motherboard Switch Settings

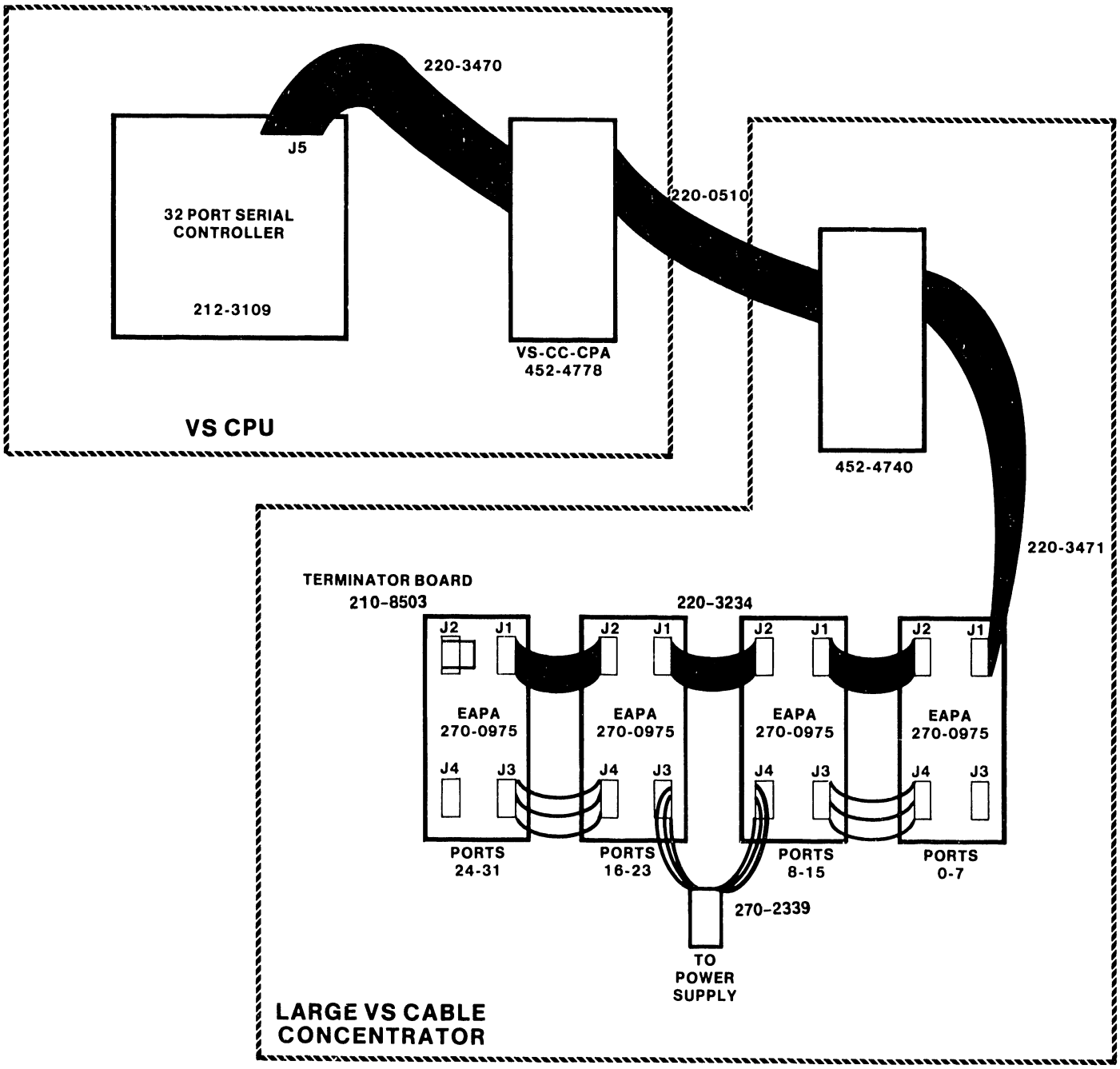


Figure N2-3 VS-100 32 Port Serial Controller/Electrical APA Cabling

CHAPTER N3

TROUBLESHOOTING

N3.1 GENERAL

Troubleshooting the 32 Port Serial Controller Board is accomplished with BIT (Built In Test) capablities. On power up, the diagnostic LED located on the Controller (ref. fig. N1-1) will light. After approximately 10 seconds the LED will extinguish indicating the board has passed all built in diagnostic tests. If the LED remains lit, a fault is indicated.

CHAPTER N4

ILLUSTRATED PARTS BREAKDOWN

N4.1 GENERAL

If defective, the entire 32 Port Serial Controller (212-3109) should be swapped out and replaced as a complete unit. Below is a listing of the Field Replaceable Units associated with the 32 Port Serial Controller.

COMPONENT	PART NUMBER
32 Port Serial Controller Bd.	212-3109
Electrical APA	270-0975
Terminator Board	210-8503
VS Backpanel (VS-CC-CPA)	452-4778
External Cable (from VS to Cable Concentrator)	220-0510
Electrical APA Cable (Ribbon Cable connecting APAs)	220-3234
DC Power Cable (Connects APA DC power)	220-2345
Cable (from Serial Cont. to rear of VS)	220-3470
Cable (from rear of Cable Concentrator to first APA)	220-3471
DC Power Cable (Connects APA DC power to power supply)	220-3470

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