WANG

7301

TELECOMMUNICATION CONTROLLERS

LVP/MVP Models:

2228D-4E,	2228D-4A,	2228D-4X
2228D-8E,	2228D-8A,	2228D-8X

SVP Models:

OP28D-4E,	OP28D-4A,	OP28D-4X
OP28D-8E,	OP28D-8A,	OP28D-8X

Customer Engineering
Product Maintenance Manual

729-1305-A

PREFACE

This document is the Standard Maintenance (STD) Manual for the models of the Wang 2228D Telecommunictions Controller listed in Chapter 1. It is organized in accordance with the approved STD outline established at the Field/Home Office Publications meetings conducted on September 14th and 15th, 1982. The scope of this manual reflects the type of maintenance philosophy selected for this product (swap unit, printed circuit assembly, chip level or any combination thereof).

The purpose of this manual is to provide the Wang-trained Customer Engineer (CE) with instructions to operate, troubleshoot and repair the above mentioned models of the 2228D. It will be updated on a regular schedule.

Second Edition (January, 1984)

This edition of the Telecommunications Controller STD manual obsoletes document no. 729-1305. The material in this document may only be used for the purpose stated in the Preface. Updates and/or changes to this document will be published as Product Service Notices (PSN's) or subsequent editions.

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CHAPTER 1

INTRODUCTION

1.1 SCOPE & PURPOSE

This manual contains information necessary to install and maintain the models of the Wang 2228D Telecommunications Controller listed below. Included are installation and operation instructions, a functional block level theory of operation, maintenance information, schematic diagrams, troubleshooting information and appropriate appendices. With the aid of this manual the Wang Customer Engineer will be able to make all necessary cable connections, perform initial turn-on and system checkout, analyze failures and troubleshoot faults down to the major component and board level and remove and replace major components.

The models covered in this manual are:

2228D-4E	OP28D-4E
2228D-8E	OP28D-8E
2228D-4A	OP28D-4A
2228D-8A	OP28D-8A
2228D-4X	OP28D-4X
2228D-8X	OP28D-8X

When reference is made in this manual to all of the above models as a group, the designation 2228D (ALL) will be used.

NOTE

Previousely released engineering hardware and software documents may refer to the 2228E and the 2228F controllers. The 2228E refers to the 2228D-4E/4A/4X while the 2228F refers to the 2228D-8E/8A/X.

This document does not cover the older 2228D-4 RS-232/RS-449 model (210-7658/210-7659).

1.2 GENERAL DESCRIPTION

The 2228D-(All) Telecommunications Controllers are microprocessor based and capable of supporting a variety of protocols over an asynchronous/ synchronous data link. The controllers are a motherboard/daughterboard combination. The 64K version consists of the 210-7857-A, 210-7858-A or 210-7859-A motherboard and 210-7659-C daughterboard. The 128K version includes the same motherboards but with 210-7855-A daughterboard. These controllers will support X.21 connections in addition to all RS232 and RS449 connections currently supported by the older 2228D-4 controllers.

The 2228D-(128K) TC Controller daughterboard (210-7855-A) is an expanded memory option of the previous 2228D-(64K) daughterboard (210-7659). The 2228D-(64K) daughterboard has a 64K x 9 memory structure and the 2228D-(128K) daughterboard has a 128K x 9 memory structure. Refer to paragraph 1.3 for complete part number matrix for the motherboard and daughterboard combinations.

Transmission speed at the modem side will support rates up to and including 9600 BAUD. In addition, full duplex capability and support of HDLC/SDLC protocols is possible.

The previous 2228D-4 and OP28D-4 controllers are combined RS-232/RS-449 (210-7658) switch selection connection controllers and were designed to support the IBM 3271 BSC Emulation (195-2159). All orders for the IBM 3271 BSC Emulation still require this version of the controller. Therefore, the 2228D-4 and OP28D-4 controllers have been put back into the pricing manual. It should be noted that this controller does not support auto-dial and that only the RS-232 interface is implemented with the IBM 3271 BSC Emulation.

1.3 CONTROLLER OPTIONS

A summary of the 2228D and OP28D controller revisions follows:

- All 32K TC Controllers (2228D-2 and OP28D-2) are being discontinued. All software products that were announced to operate on a 32K controller now require a minnimum of a 64K controller.

- The two RS-449/RS-336 connection controllers (2228D-4A and OP28D-4A) will only be available on special request.

The actions taken in replacing the various controller versions is shown below:

Old Controllers				Current Controllers		
LVP/MVP	SVP	Description	Action	LVP/MVP	SVP	Description
2228D-2	OP28D-2	32K,RS-232/449	Replaced by	2228D-4E	OP28D-4E	64K,RS-232/366
2228D-2A	OP28D-2A	32K,RS-449/366	Replaced by	2228D-4A	OP28D-4A	64K,RS-449/366
2228D-2X	OP28D-2X	32K,X.21	Replaced by	2228D-4X	OP28D-4X	64K,X.21
2228D-4	OP28S-4	64K,RS-232/449		Same (see NOTE)		
None	None		New	2228D-4E	OP28D-4E	64K,RS-232/366
2228D-4X	OP28D-4X	64K,X.21		Same		
None	None		New	2228D-8E	OP28D-8E	128K,RS-232/366
None	None		New	2228D-8X	OP28D-8X	128K,X.21

Table 1-1 (next page) lists the latest product structure for all models of the 2228D. The LVP/MVP boards are electrically identical to the SVP boards but there are mechanical differences. Reference to 2228D models also implies reference to OP28D models.

NOTE

The existing 2228D-4 64K TC Controller will remain in the price book to support IBM 3271 protocol.

An extension cable assembly is required with controllers used on the SVP system. Cable requirements are listed below:

Controller Model	Cable/Plate part no.
OP28D-4E/8E	270-0881 (Plate) 220-3109 (Cable)
OP28D-4X/8X	Not available
OP28D-4A/8A	Not available

Table 1-1 Latest 2228D Products

LVP/MVP Systems

Model #	Features	CEI #	Contr. #s	M.B. #	D.B. #	Cable #
2228D-4E	232,ACU&64K	177-2228-DE	212-2228-DE	210-7858-A	210-7659-3C	220-0332
2228D-4A	449,ACU&64K	177-2228-DF	212-2228-DF	210-7857-A	210-7659-3C	220-0248
2228D-4X	X.21 & 64K	177-2228-DG	212-2228-DG	210-7859-A	210-7659-3C	220-0274
2228D-8E	232,ACU&128K	117-2228-DH	212-2228-DH	210-7858-A	210-7855-A	220-0332
2228D-8A	449,ACU&128K	177-2228-DJ	212-2228-DJ	210-7857-A	210-7855-A	220-0248
2228D-8X	X.21 & 128K	177-2228-DK	212-2228-DK	210-7859-A	210-7855-A	220-0274

SVP Systems

OP28D-4E	232,ACU, 64K&SVP	177-2228-SE	212-2228-DE	210-7858-A =232/ACU SVP Ext.	210-7659-3C	220-0332 220-3109
OP28D-4A	449,ACU, 64K&SVP	177-2228-SF	212-2228-DF	210-7857-A =449/ACU SVP Ext.	210-7659-3C	220-0248
OP28D-4X	X.21,64K&SVP	177-2228-SG	212-2228-DG	210-7859-A =X.21 SVP Ext.	210-7659-3C	220-0274
OP28D-8E	232,ACU, 128K&SVP	177-2228-SH	212-2228-DH	210-7858-A =232/ACU SVP Ext.	210-7855-A	220-0332 220-3109
OP28D-8A	449,ACU, 128K&SVP	177-2228-SJ	212-2228-DJ	210-7857-A =449/ACU SVP Ext.	210-7855-A	220-0248
OP28D-8X	X.21, 128K&SVP	177-2228-SK	212-2228-DK	210-7859-A =X.21 SVP Ext.	210-7855-A	220-0274

NOTE

Models 2228D-4A, 2228D-8A, OP28D-4A and OP28D-8A are available on special order only.

Models 2228D-4X, 2228D-8X, OP28D-4X and OP28D-8X are not released at this time.

CEI = Customer End Item
Contr. = Control Number
M. B. = Motherboard
D. B. = Daughterboard

CHAPTER 2 THEORY OF OPERATION

CHAPTER 2

THEORY OF OPERATION

2.1 INTRODUCTION

This chapter describes the new 2228D TC Controllers on a functional block level (see Figure 2-1). The information included will provide the CE with an overall understanding of circuit functions and how they interrelate.

There are three new motherboard hardware configurations (see Table 1-1). The 210-7857-A supports the RS-449 interface which includes the RS-422 differential or balanced line driver and receiver interface from the Z80A-SIO chip to a 37-pin male connector. It also supports the RS-366 ACU which is connected to a female 25-pin connector. The 210-7858-A supports the ACU and the RS-232 interfaces. The 210-7859-A will interface only with a 15-pin male connector for networks using X.21 communication protocol.

The 2228D contains four LSI chips - the Z80A CPU, the SIO/2-A, the 9517-1 Multi-Mode DMA Controller and the PIO-A. These chips, along with memory, input/output architecture, 2200 interface, and the RS-232C, X.21 and RS449 option interfaces form the basic hardware configuration.

2.2 Z80A CPU

The Z80A CPU chip governs all controller functions. The chip uses a 16-bit address bus and an 8-bit data bus for bi-directional data flow. A reset line initializes the chip and six major status output lines. These lines are M1, MREQ, IORQ, RD, WR, and RFSH, which collectively inform the associated circuitry what function the CPU is to perform. The M1 signal is active during the first cycle (the fetch cycle) of each instruction and also during a special interrupt-acknowledge cycle. The MREQ (Memory REQuest) signal is active when memory is being accessed to fetch either an instruction or data. The IORQ (Input/Output ReQuest) signal goes active to indicate an input or output to a peripheral device or during the same previously mentioned interrupt acknowledge cycle. The RD (Read) signal indicates that the CPU will input data while performing a memory access or I/O instruction, while the WR (WRite) signal indicates the CPU will output data. During an M1 (Memory period #1) fetch cycle, the CPU will output an address for memory refresh. The RFSH (ReFreSH) signal confirms the active presence of that address.

In addition, the Z80A CPU receives a BUSRQ (BUS-ReQuest) input, which requests the CPU to switch its address, data, and status bus lines to the high impedance state so that an outside device may use these buses. An associated BUSAK (BUS-AKnowledge) output goes active when the CPU has complied with this request. Another WAIT input requests the CPU to extend the current memory access or I/O cycle as long as it is active. Finally, the Z80A CPU uses two interrupt inputs, INT (INTerrupt) and NMI (Non-Maskable Interrupt). The non-maskable NMI input signals the DLP when a parity error occurs. The maskable INT signal serves as the interrupt input for all other interrupt-causing devices in the system and is under software control.

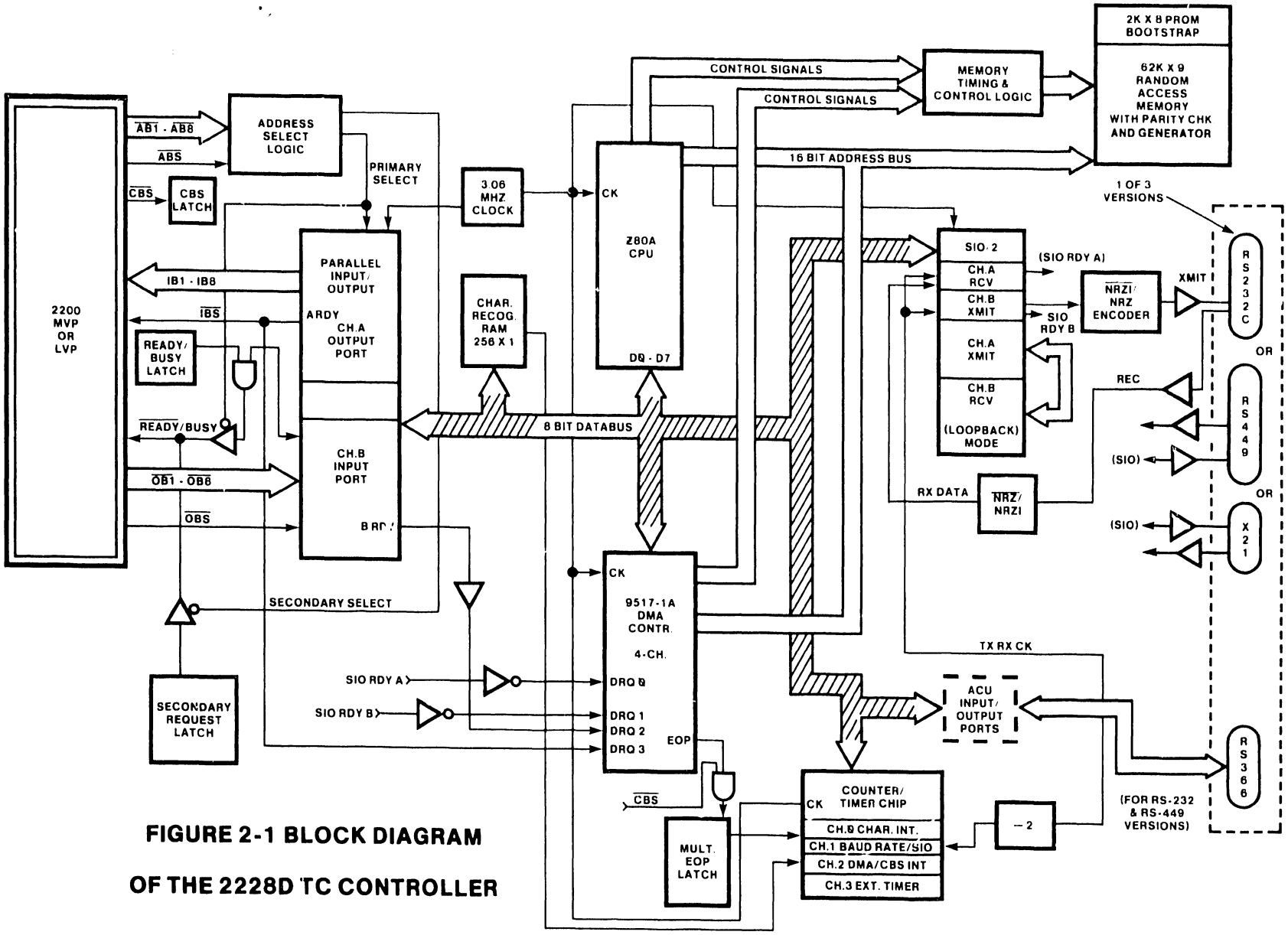


FIGURE 2-1 BLOCK DIAGRAM

OF THE 2228D TC CONTROLLER

The Z-80A non-maskable interrupt is used for parity error reporting. Z-80A vectored interrupts, in order of decreasing priority, are generated by:

1) SIO Channel A receiver

2) SIO Channel A transmitter (used only by loopback diagnostic)

3) SIO Channel A status (not used by bisync support)

4) SIO channel B receiver (used only by loopback diagnostic)

5) SIO channel B transmitter

6) SIO channel B status (not used by bisync support)

7) CTC channel 0 software timer

8) CTC channel 1 used for internal clocking to the SIO for asynchronous mode and clocking for secondary request to send during synchronous mode.

9) CTC channel 2 (interrupt vector source for all DMA channels)

10) CTC channel 3 (interrupt vector source for Ring Indicator/Incoming Call Signal).

11) PIO channel A

12) PIO channel B

2.3 THE 2200 INTERFACE

The major features of the 2228D interface to the 2200 are:

1) The 2200 can do a software reset to the 2228D.

2) The 2228D can interrupt the 2200 under microcode control.

3) Data transfers between the 2228D and 2200 can use hardware DMA to the 2228D memory, providing speed, and efficiency for both processors.

4) Data transfers are buffered by Zilog PIO chip which provides most of the signal synchronization. All handshaking signals between the 2228D and the 2200 operate in the active low condition.

5) CBS strobe along with OB8 not on will force a BUSY on the Read/Busy line to the 2200.

6) EOP from the DMA will force a Busy on the Read/Busy line to the 2200 for both DMA to PIO Read/Write channels.

7) Upon power-on reset, the Read/Busy latch is in the Ready condition. This output is combined with the ready signal from the B Input channel of the PIO to produce a Ready condition on the Ready/Busy line to the 2200.

8) An OUT '48' with D2 set to a logic 1 will set Ready Condition on the Ready/Busy latch.

2.3.1 2200 I/O BUS SIGNALS

The 2200 I/O bus signals are described in this section to make the following sections describing 2228D specifics more understandable.

Address Lines and ABS Strobe

The 2200 selects a controller with which it wishes to communicate by setting the 8-bit address on the address lines and pulsing the ABS-Strobe signal line. A controller may respond to one or more addresses.

Reset-Strobe

The 2200 pulses the Reset-Strobe signal line whenever the reset key on the keyboard is depressed. The 2228D ignores this signal.

Data Input Lines, ENDI-Signal, CPB-Signal, and IBS-Strobe

The 2200 sets CPB-signal off (CPB = logic 1) whenever it will accept data from the controller, and sets CPB-signal on whenever it will not accept data from the controller. With CPB signal off (CPB = logic 1) and ARDY from channel A (output channel) from the PIO is active high, the controller is ready to transfer data to the 2200. The data input lines are set to the value of the data byte along with the ENDI-signal. The IBS strobe is immediately generated by the ARDY signal becoming active from the PIO along with the CPB signal in the inactive state. An OUT '54' instruction by the Z80A CPU will set the ENDI-signal (IB9) to the active state. This bit remains latched in its last state until it is cleared at the end of IBS strobe.

Data Output Lines, (READY)/(BUSY) Signal, OBS-Strobe, and CBS-Strobe

The controller sets Ready signal (READY/BUSY) active low ON whenever it will accept data from the 2200, and off BUSY whenever it will not accept data from the 2200. When READY is on and the 2200 wishes to send a byte of data to the controller, it sets the data-output lines to the value of the data byte and pulses either CBS-strobe or OBS-strobe. The 2228D uses only OBS-strobe as a data strobe. A few enhancements have been designed into the 2228D for the CBS strobe signal. With OB8 not on, the CBS strobe will force a BUSY condition on the READY/BUSY Latch to the 2200. At the same time, CBS strobe is latched by the CBS Latch circuit.

To detect whether a CBS strobe has been sent by the 2200 computer, an IN '44' instruction will read the status of the CBS Latch on data bit D1. To clear the CBS latch, an OUT '44' must be executed. Otherwise, the last state of CBS latch will be read by the Z80A CPU when executing an IN '44'. After the occurrence of a CBS strobe and completion of the IN '44' instruction, an interrupt vector will be generated by CTC channel 2. The CBS strobe, along with OB8 on, will generate a hardware reset to the 2228D from the 2200.

The option to abort a data byte transfer is possible since a CBS strobe can generate a BUSY condition, thus forcing the 2228D not to accept data from the 2200. Also, the 2228D can go into an interrupt handling routine upon receiving a CBS strobe via the GIO commands. DMA single-byte transfer can also be halted in mid-stream by receiving a CBS strobe which may signal a special character byte that has been previously transfered from the 2200.

2.3.2 ADDRESSING THE 2228D CONTROLLER

Like other 2200 system telecommunications controllers, the 2228D contains a set of 8 device address switches. The value set into these switches defines the primary device address used by all 2200 I/O statements which interchange data with the controller. A secondary device address, equal to the primary device address with the high order bit (AB8) inverted, is used by the 2200 to test a request status bit set by the 2228D microcode.

When the 2200 I/O bus issues an ABS strobe, the contents of the address bus are compared with the primary device address. If they are equal, the controller is selected as the currently active device and dialog may proceed between the 2200 and the controller.

When the 2200 I/O bus issues an ABS strobe, the contents of the address bus are also compared with the secondary device address. If they are equal, the 2200 I/O bus "ready" signal is set equal to the request status bit.

2.3.3 RESETTING THE 2228D BY THE 2200

The 2228D is not reset by the 2200 reset-strobe signal. It is reset under program control by the 2200 when a byte having the high-order bit (OB8) set to 1 is outputed with a CBS strobe. This reset operation causes the Z-80A and all resettable hardware to be reset. The Z-80A starts executing at address 0, causing it to initialize all programmable parts of the controller hardware.

2.3.4 2200 REQUEST STATUS REGISTER

The Request Status Register contains one bit, D7, which determines the value of the 2200 (READY/BUSY) signal when the secondary address is selected via an OUT "60" command. The request status bit (RQB) may be tested by an $IF ON statement or used as an interrupt request condition. The interrupt request is set when the request status register is a logic 0. Conversely, the interrupt request bit is not set when the request status register is a logic 1.

2.3.5 PARALLEL INPUT/OUTPUT (PIO) CHIP

Data transfer between the 2228D and the 2200 is through the two channel PIO chip. Channel A is configured in the output mode to transfer data (IB1-IB9) from the 2228D to the input bus of the 2200. Channel B is configured in the input mode to transfer data (OB1-OB8) from the 2200 output bus to the 2228D. Signals are routed among the PIO channels and the 2200 input/output bus as shown below:

2228D Source Signal	Ready/	Busy
PIO CH.B READY Active High, and Primary Address Select is on.	Active Low	-
Secondary Address Select Is ON and OUT '60' Status Request Latch Is Set.	Active Low	-
Secondary Address Is On and OUT '60' Status Request Latch is Not Set	-	Act. High

Source Signal	Resultant Signals
2200 OBS Strobe and Primary Address Select Is On.	PIO CH.B STROBE
2200 CPB Signal is Off (Logic 1) and Primary Address Select Is On and PIO CH.A Is Ready Active High.	PIO CH.A STROBE Also, 2200 IBS Strobe
PIO CH.B READY	2200 READY/BUSY

2.4 SERIAL INPUT/OUTPUT (SIO/2) CHIP AND MODEM INTERFACE

The SIO/2 chip is the focal point where all serial data communication protocols originate from. Its basic function is a serial-to-parallel and parallel-to-serial converter/controller. Within that role, it can be configured by software to satisfy asynchronous and synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC along with CRC check codes.

The SIO/2 contains 2 independent, full-duplex channels. The T.C. controller configures one set of channels for loopback to provide diagnostic software testability. Channel A is set up as the transmit channel. It is then connected back to Channel B which is configured as the receive channel. A Ring indicator signal is routed to the Clear to Send input of channel A for external status interrupt for the RS-232C version.

The other Channel A is used as the receive channel and is routed to either the RS-232C and RS-449, or the X.21 interfaces. Similarly, channel B is set up as the transmit side and is routed to the other interface configurations.

High speed single byte data transfers between the SIO/2 and memory are accomplished through the 9517-1 DMA controller. The SIO receive Channel A is routed through DMA channel 0 during a DMA write cycle. The SIO transmit channel B is connected to DMA channel 1 during DMA read cycle. Full duplex operation can be supported through the modem.

2.4.1 CLOCK MODE REGISTER AND INTERNAL/EXTERNAL TIMING

After power-on reset has been initiated, the clock mode register is preset to a logic 1, thus enabling synchronous clock transmission to the SIO's transmitter and receiver clocks via the modem's synchronous clocks.

When an OUT 40 instruction from the Z80A CPU has been executed along with the value of D0, the clock mode register is then selected for a specific data transmission operation. When D0 is a logic 1, the internal clock from the CTC channel 1 is routed to the SIO transmitter and receiver clocks. Also, at this time the modem control signal secondary Request to Send is set to a MARK condition when D4 is equal to a logic 0. Conversely, a logic 1 on D4 will set the signal to a SPACE condition. This allows for secondary channel break transmission using half duplex 1200 bps modem. Asynchronous transmission can be programmed at this time via the SIO/2 when interfacing with asynchronous modems.

Conversely, with the data bit D0 set to a logic 0, the SIO transmit and receive channels will derive their clock sources from the external synchronous modems. At this time, the CTC channel 1 clock source will provide timing to the dedicated loopback channels of the SIO/2.

If external modems are used, which requires an active Secondary Request to Send signal other than a secondary channel break transmission, a two position header shunting cap can be removed on the 2228D board. This allows pin 19 to be disconnected from the board and thus be used exclusively for normal Secondary Request to Send.

Note that the above discussion of using an OUT 40 with data bit D0 set to a logic (0/1) condition pertains only to situations where a RS-232C or RS-449 modem or null modems are connected.

When an external loopback connector for both RS-232C or RS-449 is plugged into the 2228D board, asynchronous or synchronous data transmission can be implemented without the necessity of an OUT 40 command. This is useful for diagnostic checkout for the various protocols provided by the SIO/2.

2.4.2 SYNCHRONOUS INPUT/OUTPUT (SIO) CHIP AND MODEM RS-449 INTERFACE

Beside interfacing to a RS-232C connector, the 2228D will also provide a RS-449 interface via a 37-pin male connector. The RS-449 interface provides a functional interface between the data terminal equipment and the data communication equipment for use with the electrical characteristics specified in the EIA standards RS-422 and RS-423. The 2228D will support directly the RS-422 specification which provides a differential or balanced voltage digital line driver and line receiver interface. The RS-442 interface provides for longer cable lengths and faster baud rates than the RS-232C connection. Depending upon the data modulation rate, a maximum of 4,000 feet of cable length between the data terminal equipment and the data communication equipment can be used.

2.4.3 NRZ/NRZI MODE

Upon power-up, the NRZ/NRZI mode register will select the NRZ mode. The SIO will then transmit the data in the non-return-to-zero (NRZ) format.

When D1 is executed with an OUT 40 instruction, the NRZ/NRZI mode register will be enabled. A logic 0 on D1 will select a NRZ code while a logic 1 on D1 will enable the NRZI code format. Unlike the NRZ format, the NRZI code is an invert-on-zero transmission coding. To send a binary 1, the controller will hold the signal condition in the same state, whereas to send a binary 0, the controller will change the signal condition to the opposite state. The 2228D is provided with the option of transmitting and receiving digital data in the NRZI code when D1 is set to a logic 1 in the NRZ/NRZI mode register.

2.4.4 CHARACTER RECOGNITION

By using a 1K x 1 static RAM (2102A-2) and control logic for the DMA controller, up to 256 character patterns can be used for recognition to signal a character interrupt during synchronous operation of the SIO/2-A on the receiver channel. The databus will provide the RAM chip address. Address bit A0 from the Z80A is wired to the data input of the static RAM. This bit will distinguish the two OUT commands from the Z80A.

An OUT "31" instruction will execute incremental data from the Z80A accumulator of HEX "00" through HEX "FF" during a write cycle to the static RAM. This procedure initializes the RAM chip so that no interrupt will take place during SIO RCV DMA mode. The value of A0 will be a logic 1 at that time.

An OUT "30" instruction with the value of A0 equal to a logic 0 and the correct interrupt character code from the databus will be loaded into the static RAM. Therafter, a read cycle into the static RAM and the correct interrupt code will cause the RAM to output an active low signal. This signal is then clocked by the DMA output signals to trigger channel 0 of the CTC. The CTC, in turn, will generate an 8 bit interrupt vector on the databus during maskable interrupt mode 2. This character recognition is useful during Bi-sync operation via the DMA chip.

2.5 9517 - 1 DMA CHIP

To relieve the CPU's overhead during high speed data transfers between peripheral devices and system's memory, the AMD 9517 - 1 DMA controller will solely provide high-speed single byte transfer modes:

1) From the controller's memory through the Z80A - SIO/2 chip to the RS-232 connector's Transmit Data signal or the RS-449 connector's Send Data or the X.21's transmit signal;

2) From the RS-232, the RS-449 or the X.21 connector Receive Data signal through the Z80A - SIO/2 chip to the controller's memory;

3) From the controller's memory through the Z80A - PIO chip to the controllers memory; and

4) From the 2200 I/O bus through the Z80A - PIO chip to the controller's memory.

The DMA request input lines are programmed for active high. The DMA acknowledge outputs are programmed for the active low state. The Z80A-CTC channel 2 will provide a DMA completion interrupt to the Z80A CPU for all four DMA channels. The connections of the DMA chip are outlined as follows:

DMA REQUEST	DMA CHANNEL	DATA SOURCE	DATA DESTINATION	DMA CYCLE
$\overline{\text{SIO}}$ CH.A $\overline{\text{READY}}$	0	SIO RCV. CH.A	MEMORY	WRITE
$\overline{\text{SIO}}$ CH.B $\overline{\text{READY}}$	1	MEMORY	SIO XMIT CH.B	READ
$\overline{\text{PIO}}$ CH.A $\overline{\text{READY}}$	2	PIO CH.B INPUT	MEMORY	WRITE
$\overline{\text{PIO}}$ CH.B $\overline{\text{READY}}$	3	MEMORY	PIO. CH.A OUTPUT	READ

By executing an IN "18" instruction, the DMA status register output can be read by the Z80A. The status register contains information on which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set everytime terminal count is reached by that channel. Hence, an IN "18" instruction will distinguish which channels have triggered an interrupt vector via the CTC. By examining the status register contents, the programmer will know when the first interrupt service routine has been completed prior to receiving another interrupt request during any successive terminal counts or pending DMA requests.

2.5.1 DMA MULTIPLE EOP/CBS LATCH CIRCUIT

Since the Z80A-CTC does not have internal latch circuitry to handle successive EOP signals from the DMA chip during its interrupt handling routine, an EOP/CBS latch was designed into the board. This circuit eliminate the problem of missing a second EOP or CBS pulse when the Z80A CTC is processing the initial interrupt routine during interrupt mode 2 upon reception of the first EOP or CBS pulse. The circuit will also allow for DMA to SIO interleaving processing when the SIO is used for full duplex capability such as Bisync protocol operation. The time constant data word must be programmed to a single one count for the CTC Counter Mode in order to permit the CTC to handle one interrupt routine at a time. To accomplish this, the programmer must execute an IN "18" instruction to the DMA chip. The Z80A CPU will then be able to read the DMA status register output. The status register contains information on which channels have reached a terminal count and which channels having pending DMA requests. In addition, the IN"18" instruction will be decoded by the hardware circuitry to strobe a previous latched EOP signal over to the CTC channel. The CTC in turn will trigger a DMA completion interrupt to the Z80A CPU for any of the four DMA channels. The additional hardware will save the programmer from latching and masking off the EOP signals via a register.

The CBS strobe will also cause an interrupt on CTC channel 2 since it is hardwired to the same DMA Multiple Latch Circuit which triggers the CTC. By executing an IN'44', the programmer can read whether the CBS strobe has occurred on D1. Concurrently, an IN'44' instruction is decoded to determine the presence of a CBS strobe (logic 1) and, if present, triggers channel 2 of the CTC. The electronic mechanism is similar to detecting the EOP signals whereby successive CBS strobes can be handled in a similar fashion.

2.5.2 DMA CHANNEL 0 AND 1 REQUESTS LATCH

By latching the SIO WAIT/READY signals to the DMA, the DMA request signals will be guaranteed to be a logic 1 for at least four T-states or more. This will eliminate any truncated pulses that may arise due to the SIO's WAIT open drain outputs which can become active for either SIO Receive or Transmit channels when the opposite channel is addressed during full duplex operation.

2.6 COUNTER TIMER CHIP (CTC)

The Z80A - CTC will provide the following features:

1) A source of interrupts for the DMA to SIO interface on both the SIO Received Channel A and the SIO Transmit Channel B;

2) A source of interrupts for the DMA to PIO interface on both the PIO Output Channel A and PIO Input Channel B;

3) A counter for character interrupts on SIO Receive Channel A;

4) A dedicated software timer on channel 3 and an extended software timer feature that starts on channel 2 connected in series with channel 3;

5) An internal clock for diagnostic loopback test on the SIO, CRC check on the SIO Receive Channel A, and null modem application;

6) A programmable baud rate clock generator; and

7) A source of interrupts upon the detection of CBS strobe without OB8 on.

All input channels of the CTC should be programmed to receive active low trigger inputs in the counter mode.

The overall operation of the CTC is diagrammed as shown below:

CTC Channel	Operating Mode	Signal Input	Clock Output
0	Counter	Character Interrupt Signal (Bisync operation of SIO)	None
	Timer	None	
1	Timer	None	SIO CH.A. RCV CLK & SIO CH.B XMIT CLK
			Internal Clock* for SIO Loopback Test on SIO XMIT CH.A & SIO RCV. CH.B to RS232 Pins 19 & 11; Internal Clock* for CRC characters & null modem application.
Counter		Transmit Clock From Either RS-232 or RS-449.	SIO SMIT CH.B Clock for Checking SDLC/HDLC Flag Characters.
2	Counter must be Set To a 1	EOP or CBS strobe from the DMA Multiple Latch Circuit	None
3	Timer	None	None

* Enabled by clock mode register with value of D0 = logic 1.

2.7 AUTOMATIC CALLING UNIT (ACU)

The purpose of the ACU is to automatically establish a call for the purpose of information exchange over the communication channel under control of the 2200 CPU. Automation of the data transmission in a telephone network will be conducted by the 2200 via the 2228D-449 and the 2228D-366 interface standards (i.e. RS-232C type line drivers/receivers) which are connected to a 25-pin female connector.

Signals to the RS-366 interface are defined below. Output port (OUT '4C') from Z80A databus to the ACU interface:

			Pin #
D0	Digit Bit 0	NB1	14
D1	Digit Bit 1	NB2	15
D2	Digit Bit 2	NB4	16
D3	Digit Bit 3	NB8	17
D4	Digit Present	DPR	2
D5	Digit Request	CRQ	4

Input port (IN '4C') from the ACU interface to the Z80A databus:

			Pin #
D0	Abandon Call and Retry	ACR	3
D1	Present Next Digit	PND	5
D2	Power Indication	PWI	6
D3	Call Origination Status	COS*	13
D4	Data Line Occupied	DLO	22

* Formerly DSS from earlier RS-366 document. Signals on this circuit indicates whether a connection has been established to a remote workstation or to indicate the status of the automatic call origination procedures. However, this signal should not be interpreted to convey information regarding the operational status or preparedness of the associated data set.

EON (End Of Number) will be sent by the 2200 computer after the last digit of the number to be called has been transmitted. In response to EON, and ACU transfers the communication channel to the data set immediately without waiting for an answer signal from the called data set. The SEP signal or the separation control character is used to indicate a pause between successive digits. For example, in response to SEP, the ACU may again wait for a dial tone before turning ON circuit PND.

2.7.1 FUNCTIONAL DESCRIPTION OF ACU SIGNALS

Digital Signal Circuits (to ACU)

These signals defined as NB1, NB2, NB4, and NB8 are transmitted as digits of the called number. Its other function is to indicate a pause between successive digits by sending a SEP pattern.

Digit Present (to ACU)

This signal indicates that the ACU may read the 4 bit code combination presented on the Digit Signal Circuits - NB1, NB2, NB4, and NB8. The states of the Digit Signal Circuits must not change when the Digit Present signal is in the ON condition.

Call Request (to ACU)

When this signal is ON, the 2200 is requesting the ACU to originate a call. This signal must be ON in order to hold the communication channel (remain "OFF HOOK"). The call is aborted if CRQ is turned off prior to turning ON Call Origination Status (COS) or Distant Station Connected (DSC).

Abandon Call and Retry (From ACU)

When this signal is ON, it will indicate whether a preset time has elapsed between successive events in the calling procedure. It also points out that the call should be abandoned. Action is required by the 2200 to abandon the call.

Present Next Digit (From ACU)

when this signal is ON, the ACU is ready to accept the next digit indicated by the 4-bit word from the 2200. The OFF conditin indicates that the 2200 should also turn OFF the Digit Present (DPR) signal and set the states of the Digit Signal Circuits for the next digit.

Power Indication (From ACU)

This signal monitors the power available within the ACU. The ON condition indicates that the ACU is powered-ON.

Distant Station Connected (From ACU)

This signal monitors whether a connection has been established to a remote data station. The ON condition indicates the reception of the signal from the 2200 confirming that a connection to that equipment has been established and the control of the communication channel has been transferred to the 2200 interface via the ACI Interface Board.

Data Line Occupied (From ACU)

This signal is used to indicate whether the communication channel or a group of communication channels are in use when they are controlled by any equipment other than the ACU originating the call. The ON to OFF transition of signal DLO shall not occur until all of the other interchange circuits from the ACU are returned to their proper idle condition.

2.8 SYNCHRONOUS INPUT/OUTPUT (SIO) CHIP AND X.21 INTERFACE

In the X.21 interface, the DTE and DCE control signals are sent by a combination of steady state binary signals and coded character strings on the receive and transmit circuits. Before they are connected to the SIO, these signals are level converted by the RS-422 balanced differential line drivers and receivers. The X.21 is another communication protocol that is used between terminals and the new, synchronous public data networks that provide circuit switched and leased-circuit services for data communication. In the circuit switched network environment, the user interacts with four interface phases. They are the quiescent, call establishment, data transfer, and clearing phases. User interaction with leased-circuit networks consists of two phases - the quiescent phase and the data transfer phase. These interface phases are analagous to a conventional switched telephone network operation. The SIO chip will again provide the X.21 protocol setup. The interface signals are routed through a 15-pin male connector. They are summarized below.

Destination Signal	Source Signal
SIO Channel A Receive Clock SIO Channel B Transmit Clock	Signal Element Timing Pins 6 and 13
SIO Channel A Receive Data	Receive on pins 4 and 11
SIO Channel B Carrier Detect	Indication on pins 5 and 12
SIO Channel B Clear To Send	Byte Timing on Pins 7 and 14 ANDed with SIO Ch.B Request to Send
Transmit on pins 2 and 9	SIO Channel B Transmit Data
Control on pins 3 and 10	SIO Channel B Data Terminal Ready
SIO Channel A Clear to Send (CTSA)	OUT '4C' with D7 = 1 allows Receive Data to CTSA

The CTSA input of the SIO is used primarily as a monitor line during the call establishment phase of the X.21 protocol. The DCE will issue a string of zeroes during the Clear Indication procedure which will asK for 16 contiguous bit times along with the Indicator circuit in the OFF state. The software engineer can read into Read Register "0" (RRO) to check whether it has received a clear signal in the active low state. After detecting a clearing signal, the 2228D should send the DTE CLEAR CONFIRMATION.

2.9 MEMORY ORGANIZATION

Memory consists of a 2K PROM, for bootstrap loading and power-up diagnostics, along with 62K of available RAM. The RAMs are MOS 16Kx1-bit, dynamic memory circuits, having a chip access time of 150 nanoseconds and a read/modify-write cycle time of 320 nanoseconds. The PROM occupies address space 0 through 2K, while the RAM occupies address space 2K + 1 through 64K. Parity checking of RAM is supported. A parity error should trigger the Z80A non-maskable interrupt, and initiate an interrupt to the 2200.

2.9.1 MULTIPLEXED MEMORY ADDRESSING

Each MOS memory chip is physically arranged as a two-dimensional array of cells. Certain address inputs are used for row selection and the remaining address inputs are used for column selection. Row selection is required before the sense amplifiers can begin their slow detection process. However, column selection is not required until the outputs of the sense amplifiers become valid because its function is to gate data from the selected sense amplifier to the data output circuitry. Since the column selection information is not used internally until well after the row selection information is required, only the row addresses need to be available to the chip at the start of a cyle. Thus, the column address can be determined later with no penalty of access time. The multiplexed memory address technique takes advantage of this delayed need for a column address. Rather than using 13 address lines to select one of 16,384 memory cells, the memory first uses seven address lines to select one of 128 rows and then subsequently uses those same sever lines to select one of 128 columns in that selected row.

2.9.2 MULTIPLEX TIMING CONSIDERATIONS

Although address multiplexing provides some very substantial system benefits, it complicates system timing. The multiplexing technique requires that both row and column addresses get into the chip within a short time, using the same address pins. The requirement establishes a rather tight timing window during which the individual events must occur. The sequence of events required to address any given memory chip location is as follow:

1) Establish a 7-bit row address to specify one of 128 rows of storage cells in the chip.

2) Bring the RAS (Row Address Strobe) signal low to start the row selection process by the chip's sense amplifiers.

3) Maintain that same row address valid for some minimum hold time to allows the chip's sense amplifiers to complete the detection process.

4) Establish a 7-bit column address (on the same address lines) to specify one of 128 columns in the selected row of memory storage cells.

5) Bring the CAS (Column Address Strobe) signal low to confirm the stabilized column address.

6) Hold that same column address valid for some minimum hold time to allow the chip's sense amplifiers to complete the column-address detection process (and to allow the associated read/write operation for the resultant location).

To achieve the specified access time from RAS, CAS must be brought low within some specified maximum delay after RAS goes low.

To summarize; the functions of RAS are to initiate a cycle, to strobe or latch the row address, to enable the selected row of memory cells, to sense and restore the data in that row of memory cells, and to maintain the sensed data from the entire row of addressed memory cells in their respective sense amplifiers. The sense amplifiers maintain this data as long as RAS remains active. At the end of a cycle, when RAS is taken high, the selected row is immediately turned off, isolating the correct data in the cells. After the row is off, the half-digit lines are prepared for a new cycle.

CAS, on the other hand, controls column selection circuitry and the transfer of data from the selected sense amplifier to the output circuitry. After RAS strobes the row address information from the multiplexed address input pins, CAS strobes the column address from the same pins. When CAS goes active (low), the column address is strobed or latched into the circuit. This address is then decoded to select the proper column. Data from the selected sense amplifier is then transfered to the output buffer, completing the read-access operation.

2.10 WRITE BAD PARITY (OUT'71')

Additional circuitry has been added to allow writing bad parity to the data bus. An OUT '71' instruction executed by the Z80A will force a one on the 9th bit of an even number of ones pattern, thus causing a parity error for even parity. The parity error will then trigger the Z80A non-maskable interrupt to location 0066. This feature will verify the performance of the parity check circuit.

2.11 LED STATUS DISPLAY (IN '70')

To make room for the OUT '71' instruction for writing bad parity, an IN '70' instruction will be used by the Z80A to extinguish the LED, thus indicating that the system diagnostic software is running. The LED will still be initially illuminated upon power-up, indicating that the system is ON.

CHAPTER 3 OPERATION

CHAPTER 3

OPERATION

3.1 CONTROLS AND INDICATORS

The controls and indicators of the 2228D-4E/8E (64K/128K) Controller boards are shown in Figures 3-1, 3-2, 3-3 and 3-4, including the locations of the External/Internal Test Option Switch (SW1), the Device Address Switch (SW2), the power-up diagnostic PROM (L37 on 210-7855-A or L44 on 210-7659-3C) and the diagnostic LED. (The 2228D-4X/8X and the 2228D/4A/8A units were not available at the time of this document release.)

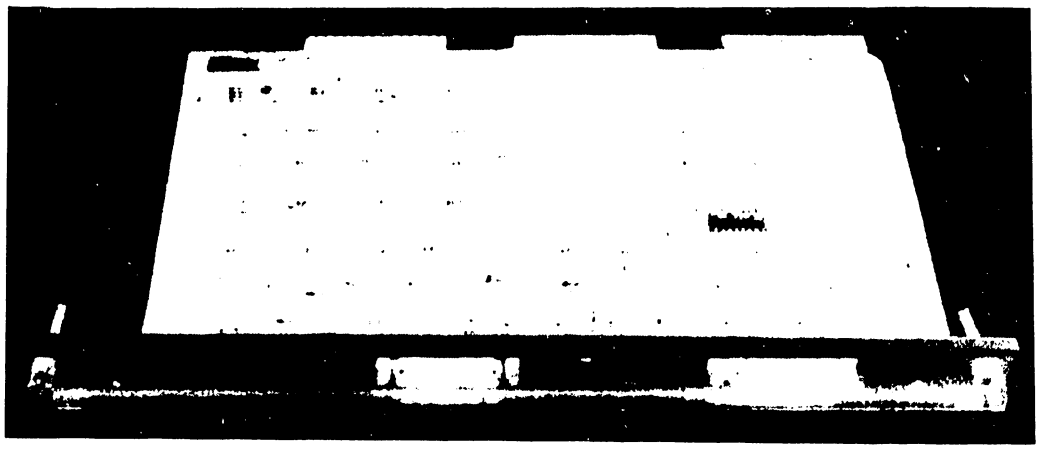


Figure 3-1 2228D-4E/8E Controller Assembly

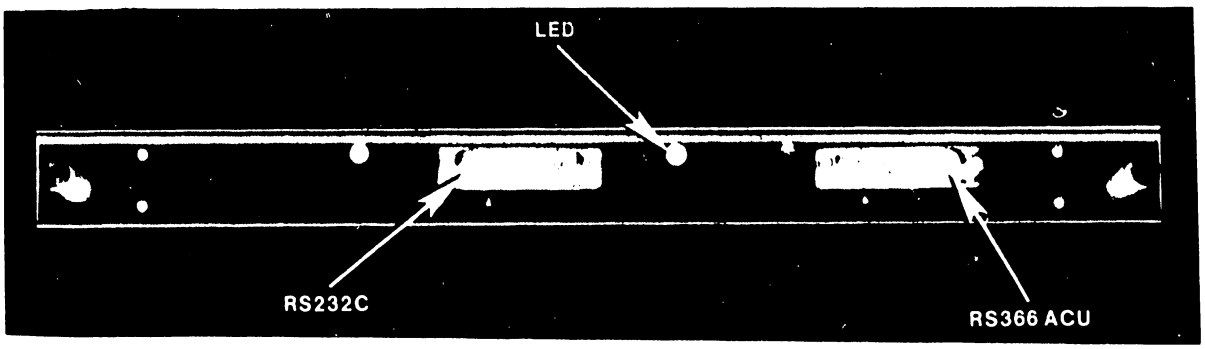


Figure 3-2 2228D-4E/8E Mounting Panel

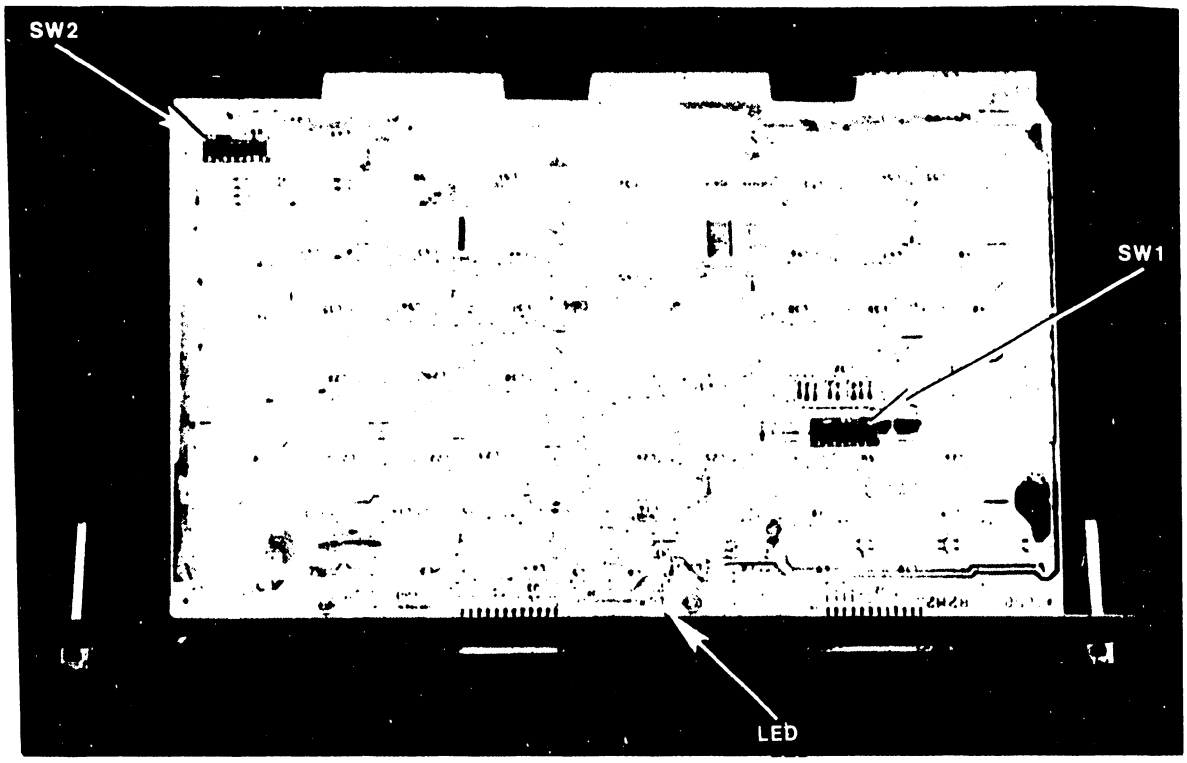


Figure 3-3 210-7858-A Motherboard

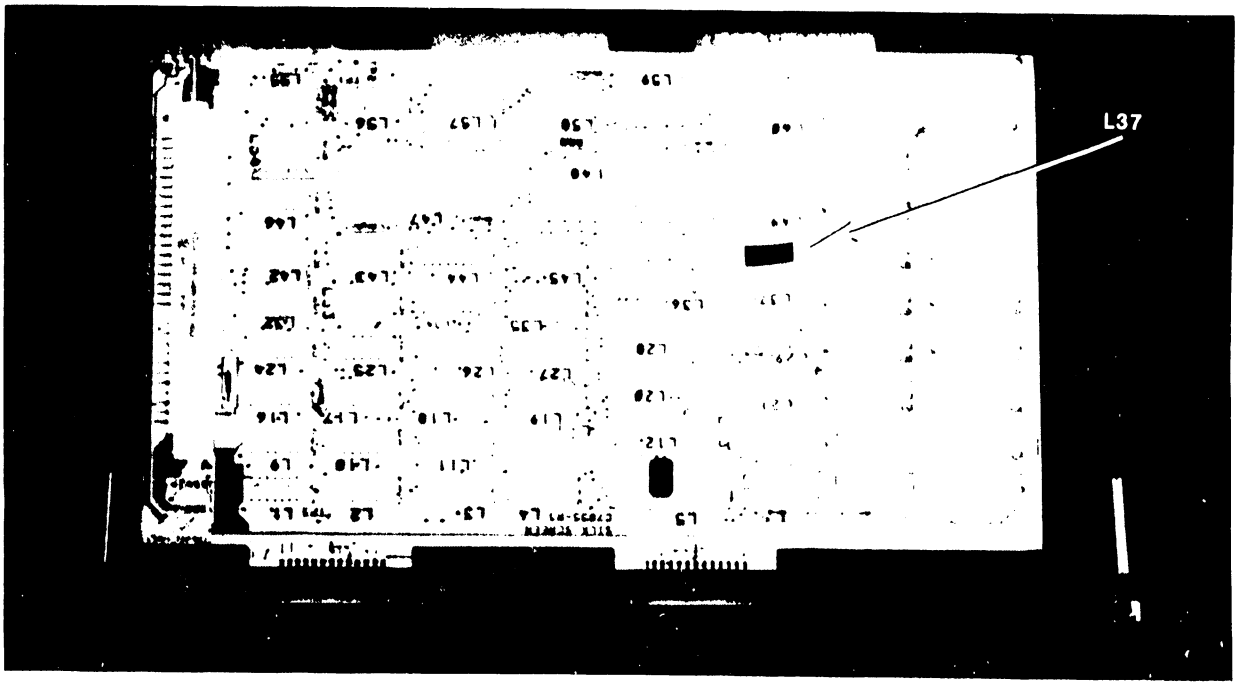


Figure 3-4 210-7855-A Daughterboard

3.1.1 LED INDICATIONS

Follow the procedures outlined in Chapter 4 to set switches, install the mother/daughterboard assembly in the 2200 mainframe and power-up the system.

Within 10 to 15 seconds after power-up, the LED (see Figure 3-2) will give one of the following three indications.

a. LED goes off

This indicates that all TC controller power-up tests have passed and the program enters the 2228D-4E/8E bootstrap firmware.

b. LED remains on

The LED remaining on indicates a catastrophic failure. The controller board should be replaced.

c. LED flashes

A flashing LED indicates a reportable failure. Go to section 4.5.2. (Use Power-up Error Code Interpreter software).

CHAPTER 4

INSTAL-LATION

CHAPTER 4

INSTALLATION

4.1 PARTS REQUIRED

The only parts required for installation are the 2228D-(A11) TC Controller Assembly and the appropriate modem interface cable (see paragraph 4.6). Controllers used on the SVP system will also require an extension cable (see paragraph 1.3).

4.2 PROM AND RAM CHECK

The controller power-up diagnostic is factory loaded into a 2K power-up PROM. The PROM locations (L44 on 210-7659-3C or L37 on 210-7855-A) are shown in Figure 4-1. The correct PROM and RAM numbers are as follows:

Model	Motherboard	Memory	Daughterboard	PROM	PROM WLI#	RAM WLI#
2228D-4E	210-7858-A	64K	210-7659-3C	L44	378-4390	377-0345-M
2228D-4A	210-7857-A			Same		
2228D-4X	210-7859-A			Same		
2228D-8E	210-7858-A	128K	210-7855-A	L37	378-5145-R1	377-0645
2228D-8A	210-7857-A			Same		
2228D-8X	210-7859-A			Same		

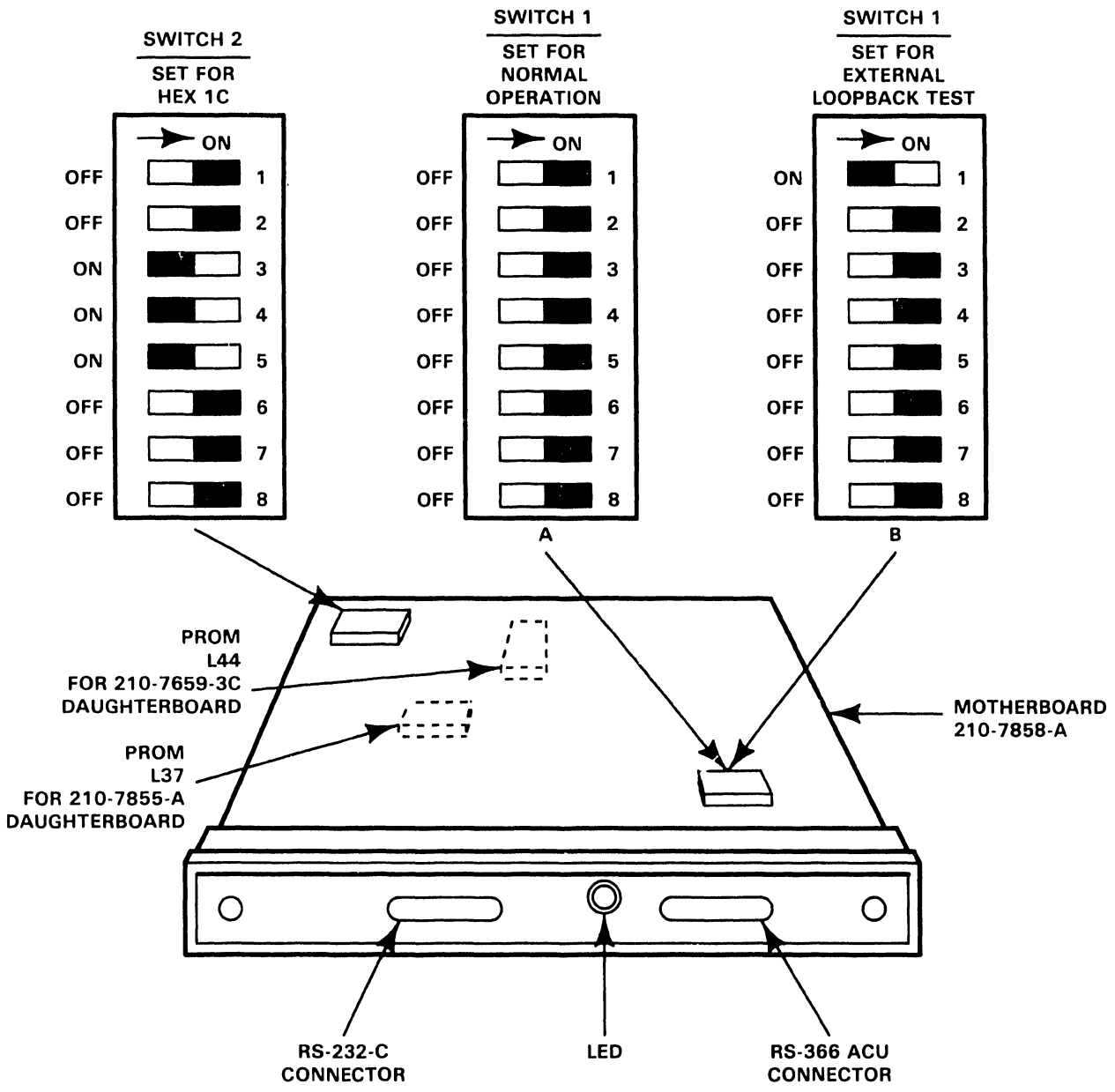
4.3 SWITCH SETTINGS

The option switches are used to set the site address of a multipoint secondary station and to set any other user options. Figure 4-1 shows the settings for the switch banks that are located on the motherboard. Switch SW2 is the device address switch. It must be set for HEX 1C (switches 3,4 and 5 ON and all others OFF).

NOTE

If a 2228B or 2228D TC Controller board is presently installed and will remain installed in the 2200 CPU, ensure that its device address switch is set for HEX 1C. The 2228D-(A11) device address should then be set to 1F (slide switches 1, 2, 3, 4 and 5 ON and 6, 7 and 8 OFF).

Switch SW1 is the test option switch. It has two settings, one for normal operation and the other for diagnostic external loopback test. The loopback test must be made during initial installation. Therefore, SW1 must be set for this test before installing the mother/daughterboard assembly. The setting for the loopback test is HEX 01 (slide switch 1 ON and all others OFF). When the switch is in this position, the power-up diagnostic will run a self test routine called "S10 Bisync External Test" in addition to the Internal Loopback Test.



NOTE: Model 2228D-4E/8E is illustrated above. Models 2228D-4A/8A and 2228D-4X/8X are not yet available.

Figure 4-1 Controller Switch Settings

4.4 EXTERNAL LOOPBACK TEST (POWER-UP)

In order to run the external loopback test, the test option switch must be set to HEX 01 as stated on the previous page and the appropriate loopback connector must be installed on the interface connector. Refer to Appendix F for the proper loopback connector part numbers. Note that the 366 connector is not required during power-up tests. The wiring diagrams for the loopback connectors are also shown in Appendix F. After installing the loopback connector, the controller assembly may be installed in the 2200 master. Board placement references are given below.

Document No.	Manual/Category	Figure No.	Page No.
729-0602	LVP/4103	8-2	8-4
729-0583	VP/4103	3-1	3-4
729-0584	MVP/4103	1-8	1-9
729-0935	SVP/4103	8-7	8-9

CAUTION

The 2228D-(A11) controller is slightly larger than other 2200 system controllers and may contact the fan if mounted next to it. Therefore, it should be mounted in a slot away from the fan.

The power to the 2200 CPU may be turned on after installing the controller. The supply voltages for the controller boards should then be checked at the 2200 power supply. Power supply reference material is listed in below.

Document No.	Manual/Category	Section No.	Page No.
729-0602	LVP/4103	11.2	11-2
729-0583	VP/4103	3.3.2	3-12
729-0584	MVP/4103	7.3.2	7-5
729-0935	SVP/4103	11.2	11-1

The loopback tests will start to run automatically when ac power to the 2200 CPU is turned on. The tests take 10 to 15 seconds. The diagnostic LED on the panel of the controller assembly will come on during the tests and will go off at the conclusion of the tests if all tests pass. Test failure is indicated by the LED either remaining on or flashing. If the LED remains on steady, a catastrophic failure is indicated and the controller assembly should be replaced. A blinking LED indicates a reportable failure. If this condition is observed, go to section 4.5.2 for a description of the power-up error code interpreter program.

After the external loopback tests are complete, turn off the power to the 2200 CPU and remove the controller assembly. Next, set the test option switch (SW1) to HEX 00 (all switches off) and remove the loopback connector. Now reinstall the controller in the 2200 CPU and turn on the ac power. The power-up diagnostic will then run the internal loopback test only.

Upon successful completion of the Power-Up Diagnostic the Field Level diagnostics should be executed (see paragraph 4.5.3).

4.5 2228D-(A11) DIAGNOSTICS/TESTS

4.5.1 POWER-UP DIAGNOSTICS (Description)

Upon powering-up, the 2228D-(A11) microprocessor will run the 2228D-(A11) TC Controller Power-Up Diagnostics resident in the 2228D-(A11) PROM. This takes 10 to 15 seconds. After this time the LED located on the mounting bracket will give an ON, OFF or FLASHING indication (refer to section 3.1.1 for an explanation of these indications).

The following is a list of the tests that are performed by the Controller during the Power-Up Diagnostics.

POWER-UP TESTS

1. Z80 Power Up
2. Prom Checksum Test
3. PIO Power UP
4. Write Bad Parity/Parity Generator Test
5. Bank Decoder Test
6. 62K Ram Marching AA and 55 Test
7. DMA 9517 Power Up
8. DMA 9517 Current and Word Count
9. CTC Power Up
10. CTC Channel Interrupt Test
11. SIO Bisync Internal Test

4.5.2 POWER-UP ERROR CODE INTERPRETER

4.5.2.1 Introduction

The 2228D-(A11) Power-Up Error Code Interpreter (software) will interpret the error codes supplied by the 2228D-(A11) TC Controller Power-Up Diagnostic Program (firmware). The Power-Up Diagnostic program is resident in the 378-4390 PROM, located in position L44, on 64K daughterboard (210-7659) or in the 378-5145 PROM, located in position L37 on the 128K daughter board (210-7855).

NOTE

The Power-Up Error Code Interpreter program is used only if the LED is FLASHING (reportable failure)

4.5.2.2 Program Description

The Power-Up Error Code Interpreter program is designed to test the LSI circuitry needed for overall TC board operation. It will also aid in troubleshooting hardware faults. The following routines are performed by this program:

1. Request device address for 2228D-(A11) TC Controller.
2. Request error code from 2228D-(A11) TC Controller.
3. Interpret error code and display appropriate information.

Refer to paragraph A.2 for software part numbers pertaining to the Power-up Error Code Interpreter.

4.5.2.3 Operation

To run the 2228D-(A11) Power-Up Error Code Interpreter Program, perform the following Program Loading Procedure in sequential order.

a. Load diskette (#702-0182).
b. Select that disk drive with SELECT DISK statement.
c. Press 'LOAD'.
d. Press 'RUN'.
e. Press 'T' and enter the name "28DEIRO".
f. Follow screen instructions.

4.5.3 FIELD LEVEL DIAGNOSTICS

4.5.3.1 Configuration Requirements

4.5.3.1.1 Hardware

2200 MVP/LVP/SVP/VP
2228D-(A11) TC Controller
Appropriate loopback connector for RS-232, X.21 or RS449 Controller
RS 366 ACU loopback connector
Requires 56K Bytes of memory

4.5.3.1.2 Software

Software Part No.	Comments
702-0183 Rev 11C0 (2228D-4E only)	Used only with 2228D-4E (64K) presently in the field. Loopback connectors are 420-1040 or the RS-232 portion of the 420-1041 only (do not use the 366/ACU portion. Use the 420-1104 connector for the 366/ACU.
702-0240 Rev 1340	
2228D-4E or 2228D-8E	Use the RS-232 (420-1041) and 366(420-1104) loopback connectors.
2228D-4X or 2228D-8X	Use the 421-0010 loopback connector for X.21.
2228D-4A or 2228D-8A	Use the 270-3193 loopback connector for 449 and use the 420-1104 for the ACU connector.

Refer to Appendix F for loopback connector wiring diagrams.
Refer to Appendix A for a complete list of diagnostic part numbers.

Diskette containing MVP BASIC 2 Rev. 2.1 or VP Basic 2 Rev.2.3 and up. MVP Basic is used to configure the 2200 CPU for the Field Level Diagnostic.

When using the MVP software, the Device Table must have the Secondary Address of the TC Controller defined as follows:

Primary Address	Secondary Address
019	099
01A	09A
01B	09B
01C	09C
01D	09D
01E	09E
01F	09F

4.5.3.1.3 Program Description

The 2228D-(All) Field Level Diagnostic is controlled by a Monitor program in the 2200 CPU. The Monitor downline loads a microcode file to the 2228D-(All) RAM. The Monitor program is menu driven. A test is selected from the menu by keying the appropriate S.F. key. The test is run and any error is reported to the 2200, where it is interpreted by the Monitor program. Upon successful completion of a test, the Monitor program again displays the menu.

4.5.3.1.4 Load Procedures

a. Load MVP Basic

b. Respond to the querries displayed on the Monitor, such as selecting the correct 2200 Peripheral Device Address, partition size, etc.

c. Software #702-0183 - The operator must key LOAD RUN "file name" RETURN.

Software #702-0240 - Insert the program disk into the selected disk drive. Press the LOAD, RUN, "28EFSR1", and RETURN Keys.

NOTE

If your floppy had the START File, and it is set up to load "28EFSR1", you need only press the LOAD, RUN, and RETURN Keys. The "28EFSR1" Program will be loaded and executed.

d. Install the appropriate loopback connector on the motherboard. See paragraph 4.5.3.1.6 below for correct part numbers. Appendix F contains wiring diagrams of the loopback connectors.

e. When a menu of the available tests is displayed, select the test that you wish to run by pressing the appropriate S.F. Key.

Refer to Appendix C for a complete list of error codes and descriptions. Appendix D contains RAM chip locations and bit assignments.

4.5.3.1.5 Revision History

Software part no. 702-0240 Rev. 1340 -- First Release

4.5.3.1.6 Loopback Connector Part Numbers

Software part no.	Loopback connector part no.
702-0183	420-1040 for RS-232 or 420-1041 for RS-232 and 420-1104 for 366/ACU
702-0240	420-1040 for RS-232 or 420-1041 for RS-232 and 420-1104 for 366/ACU 270-3193 for 449 421-0010 for X.21

4.6 INTERCONNECTION WITH MODEMS

Standard modem interface cables are provided to connect the controller assembly to the modem. The part numbers and lengths of these cables are as follows:

Modem Cable	Part Number	Length
RS-232-C	220-0332	12 feet
RS-449	220-0248	20 feet
X.21	220-0274	12 feet

Connect the cable from the appropriate connector on the controller panel to the connector on the modem (on most Bell modems this connector will be labeled "CUST EQUIP"). If required, refer to Appendix B for interface pin assignments and descriptions.

4.6.1 OPTIONAL CABLES

For modem cable lengths longer than those specified in paragraph 4.6, the following optional cables are available.

Length	Wang Part Number		
	RS-449-C	RS-232-C	X.21
25 ft	120-2325-01	220-0333	120-2326-01
50 ft	120-2325-02	220-0334	120-2326-02
100 ft	120-2325-03	N/A	120-2326-03
350 ft	120-2325-04	N/A	120-2326-04
500 ft	120-2325-05	N/A	120-2326-05
750 ft	120-2325-06	N/A	120-2326-06
1000 ft	120-2325-07	N/A	120-2326-07

CHAPTER 5 MAINT-ENANCE

CHAPTER 5

MAINTENANCE

The 2228D-(A11) Controller boards are not to be repaired in the field and there are no parts requiring preventative or corrective maintenance. The only replaceable parts are the RAMS (WLI #377-0345-M or #377-0645) located on the daughterboard (210-7659-3C or 210-7855-A). Appendix D contains RAM chip locations and bit assignments. Refer to paragraph 4.4 for board placement reference manuals.

CHAPTER 6 SCHE-MATICS

THE SCHEMATICS, WHEN AVAILABLE, ARE ON THE LAST FICHE IN THIS SET.

CHAPTER 7

ILLUSTRATED PARTS BREAKDOWN

CHAPTER 7

ILLUSTRATED PARTS BREAKDOWN

The 2228D-(All) Controller assembly is not to be repaired in the field except for RAM failures. When a controller develops trouble in a user's system it will be replaced as a unit (see Chapter 1 for part numbers). Therefore, no internal parts breakdown is required.

CHAPTER 8

TROUBLE-SHOOTING

CHAPTER 8

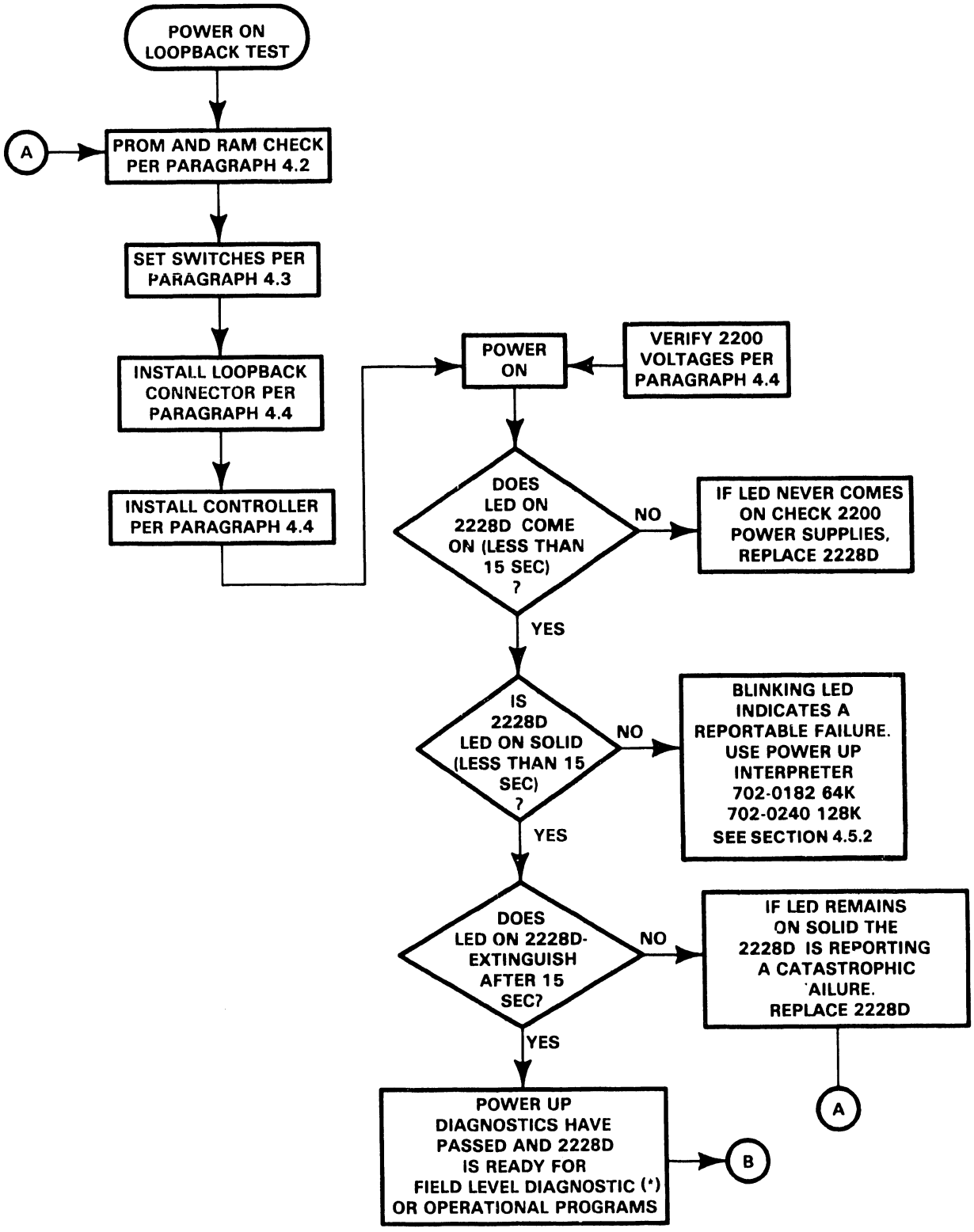
TROUBLESHOOTING FLOW CHARTS

8.1 INTRODUCTION

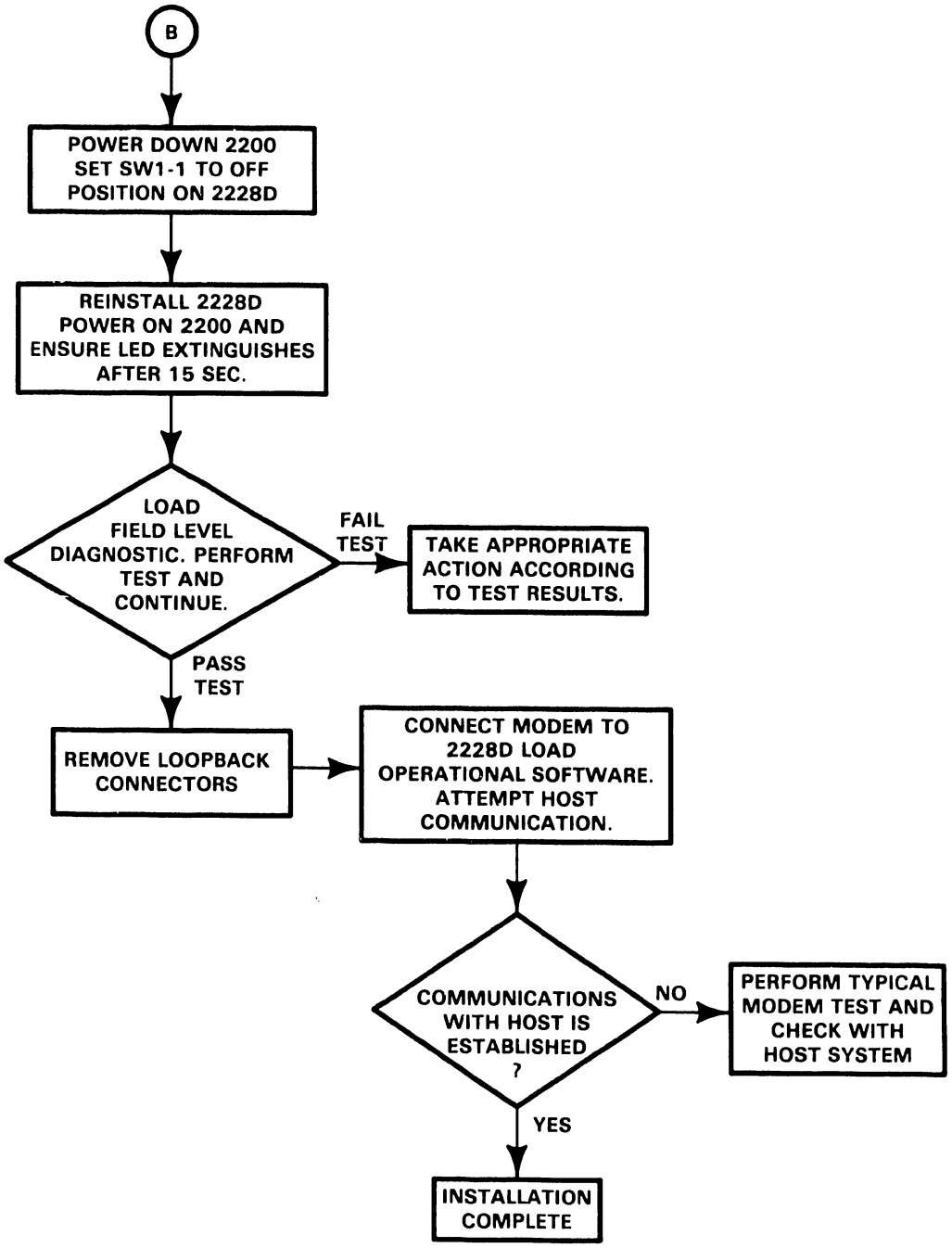
Troubleshooting any telecommunications system can be a complex task. There may be many components involved, such as telephone lines, modems and host computers, and any one of these can cause a problem. When a problem is encountered in the telecommunications, system refer to the troubleshooting flow charts which follow. These flow charts are designed to assist the Customer Engineer in locating and repairing faults.

8.2 TROUBLESHOOTING FLOW CHARTS

8.2.1 EXTERNAL/INTERNAL LOOP TEST



8.2.2 FIELD LEVEL TESTS



APPENDIX A

DIAG-NOSTIC PART NUM-BERS

APPENDIX A

DIAGNOSTIC PART NUMBERS

A.1 POWER-UP SELF TEST

Description	For 2228D-4E	For 2228D-8E/8A/8X
Package part no.		195-2609-3
Documentation part no.		760-1123
PROM File Diskette SSSD part no.	702-0186	702-0242
PROM part no.	378-4390	378-5145

A.2 POWER-UP ERROR INTERPRETER

Description	For 2228D-4E	For 2228D-(All)
Package part no.		195-2607-3
Documentation part no.		760-1121
Program Diskette SSSD part no.	702-0182	702-0240

A.3 FIELD SERVICE DIAGNOSTIC

Description	For 2228D-4E	For 2228D-(All)
Package part no.		195-2607-3
Documentation part no.		760-1122
Program Diskette SSSD part no.	702-0183	702-0240

NOTE

Documentation and Program Diskette are included under the Package part number.

APPENDIX B MODEM INTER-FACE SIGNALS

APPENDIX B

MODEM INTERFACE SIGNALS

EIA RS 232-C

RS 232-C provides an interface between the data terminal equipment (DTE) - and the data communications equipment (DCE)- typically a modem, employing serial binary data interchange. The following paragraphs describe the RS 232-C modem interface signals. The modem must be in the data mode when checking the control signals.

Table B-1
Summary of RS 232-C Interface Signals

Pin	Circuit	Circuit Name	Function	Source
1	---		Protective Ground	
2	BA	TXD	Transmitted Data	DTE
3	BB	RXD	Received Data	DCE
4	CA	RTS	Request To Send	DTE
5	CB	CTS	Clear To-Send	DCE
6	CC	DSR	Data Set Ready	DCE
8	CF	RLSD	Received Line Signal Detector	DCE
15	DB	TC	Transmitter Signal Element Timing	DCE
17	DD	RC	Receiver Signal Element Timing	DCE
20	CD	DTR	Data Terminal Ready	DTE

NOTE: The ON condition=(+3 to +25V), the OFF condition=(-3 to -25V).

Pins 1 and 7 are electrically bonded to the chassis and reference ground.

Transmitted Data - Signals on this circuit are generated by data terminal equipment and are transferred to the local transmitting signal converter for transmission of data to remote data terminal equipment. The data terminal equipment will not transmit unless an On condition is present on all of the following circuits:

Circuit CA (Request to Send)
Circuit CC (Data Set Ready)
Circuit CB (Clear-To-Send)
Circuit CD (Data Terminal Ready)
Circuit CF (Received Line Signal Detector) Note: May be required by some modems before transmitting data.

Received Data - Signals on this circuit are generated by the receiving signal converter in response to data signals received from remote data terminal equipment via the remote transmitting signal converter.

Request to send - Data terminal presents ON signal on this circuit when terminal intends to transmit data. Once this signal is present, data terminal must wait for clear-to-send signal before starting data transmission.

Clear To-Send - Signal on this circuit are generated by the data set to indicate whether or not the data set is ready to transmit data. The ON condition together with the ON condition on Circuits CA and CC (Request to Send and Data Set Ready) and if implemented Circuit CD (Carrier Detect), indicates that signals present on circuit Transmitted Data will be transmitted to the communication channel. The off condition is an indication to the DTE that it should not transfer data across the interface to Circuit BA (Transmitted Data).

Data Set Ready - Signals on this circuit are used to indicate the status of the local data set. The on condition on this circuit indicates that the local data communication equipment is connected to a communication channel ("OFF hook" in switched service) and the local data communication equipment is not in test (local or remote), or dial mode. The On condition also indicates that any timing functions required by the switching system to complete a call has completed.

Received Line Signal Detector (carrier) - The ON condition on this circuit indicates the data communications equipment is receiving a signal which meets the criteria established by the DCE manufacturer. The off condition indicates that no signal is being received or that the recieved signal is unsuitable for demodulation.

Transmitter Signal Elemnet Timing - Signals on this circuit are used to provide the DTE with signal element timing information. The DTE will provide a data signal on Circuit BA (Transmitted Data) in which the transitions between signal element timing nominally occurs at the time of the transitions from off to on of this circuit.

Receiver Signal Element Timing -Signals on this circuit are used to provide the DTE with received signal element timing information. The transition from ON to OFF will nominally indicate the center of each signal element on Circuit BB (Received Data). Timing information on this circuit will be provided at all times when Circuit CF (Received Line Signal Detector) is in the On condition.

Data Terminal Ready - Signals on this circuit are used to control switching of the DCE to the communications channel. The ON condition prepares the DCE to be connected to the communications channel amd maintains the connnection established (e.g. manual call origination, manual answering or automatic call origination.

RS 366 Interface

RS 366 provides an interface between data terminal equipment (DTE) and Automatic Calling Equipment (ACE) for data communication. The following paragraphs define the signal characteristics of RS 366. RS 366 is enabled through 25 position connector.

Table B-2 RS 366 Interface Summary

Pin	Circuit Mnemonic	Circuit Function	Source
7	SG	Signal Ground	
18	RC	Receive Common	
19	SC	Send Common	
4	CRQ	Call Request	DTE
6	PWI	Power Indication	ACE
22	DLO	Data Line Occupied	ACE
13	DSC	Distant Station Connected	ACE
3	ACR	Abandon Call & Retry	ACE
5	PND	Present Next Digit	ACE
2	DPR	Digit Present	DTE
14	NB1	Digital Signal Circuit 1	DTE
15	NB2	Digital Signal Circuit 1	DTE
16	NB4	Digital Signal Circuit 1	DTE
17	NB8	Digital Signal Circuit 1	DTE

Signal Ground - This conductor directly connects the DTE circuit ground to the ACE circuit ground to provide a conductive path between the DTE and ACE signal commons.

Send Common - This conductor is connected to the DTE circuit ground and is used at the ACE as a reference potential for the interchange circuit receivers.

Call Request - Signals on this circuit are generated by the DTE to request the ACE to originate a call. The OFF condition indicates that the DTE is not using or has completed use of the ACE.

Power Indication - Signals on this circuit indicate whether power is available within the ACE.

Data Line Occupied - Signals on this circuit are used to indicate when the associated modem is Off Hook or the associated telephone is in use. The OFF condition indicates that the DTE may originate a call provided that Circuit PWI is ON.

Distant Station Connected - Signals on this circuit indicate whether a connection has been established to a remote data station.

Abandon Call and Retry - Signals on this circuit are used to indicate whether a preset time has elapsed between successive events in the calling procedure. The ON condition indicates that the call should be abandoned.

Present Next Digit - Signals on this circuit are generated by the ACE to control the presentation of digits on Circuits NBV1, NB2, NB4, and NB8 (digits of a called number) (digits used for control purposes).

Digit Present - Signals on this circuit are generated by the DTE to indicate that the ACE may read the code combination presented on Circuits NB1, NB2, NB4, and NB8.

Digit Signals Circuits (NB1-NB8) - Parallel binary signals generated by the DTE that represents the digits of a dialed number or parallel binary signals that are used locally for control purposes.

X.21 Interface

X.21 is a general purpose interface between the data terminal equipment (DTE) and data communication equipment (DCE) for synchronous operation on public data networks. Signals that specify the DTE/DCE interface that are supported by X.21 are enabled through a 15 pin connector of which eight pins are used as specified below.

Table B-3
Summary of X.21 Interface Signals

Pin	Circuit Name	Circuit	Source
1	Protective Gnd	G	
8	DTE ground rtn	Ga	DTE
2,9	Transmit	T	DTE
4,11	Receive	R	DCE
3,10	Control	C	DTE
5,12	Indication	I	DCE
6,13	Signal Element Timing	S	DCE
7,14	Byte Timing	B	DCE

Transmit - Signals on this circuit are generated by the DTE. As well as being used for the transmission of data or selection sequences to the DCE, this circuit may be held in a steady logic state of 0 or 1 together with on or off conditions of the control circuit (C) to signal DTE conditions or states.

Receive - Signals on this circuit are generated by the DCE. The signals may be generated in response to signals received from a remote data set, generated locally by the DCE as response or control information to the DTE or held in a steady logic state of 0 or 1 together with on or off condition of the indication circuit (I) to signal DCE conditions or states.

Control - Signals on this circuit are generated by the DTE. The on or off conditions of this circuit are used together with steady logic states (0 or 1) on the Transmit circuit to signal DTE conditions.

Indication -	Signals on this circuit are generated by the DCE. The on or off conditions of this circuit are used together with steady logic states (0 or 1) on the Receive circuit to signal DCE conditions.
Signal Element Timing	Signals on this Circuit are generated by the DCE. The signals are used for bit rate timing for the DTE.
Byte Timing -	Signals on this circuit are generated by the DCE and are optional. The signal provides byte boundaries for call control character alignment.
Signal Ground	
DTE Common GD.	

Unlike RS232 or RS449, where a DTE's or DCE's condition or state is signaled via a unique control line (ie Request To Send), X.21; uses the T, R, C and I lines to signal encoded state conditions. This is accomplished by the DTE or DCE sending steady logic conditions 0 or 1 on circuits T or R, together with associated conditions (ON or OFF) on circuits C or I, for a period of at least 24 bit intervals. Table B-4 lists X.21 signaling conditions and associated states:

Table B-4
X.21 Signaling Conditions and States

State	Circuit				Description
	T	R	C	I	
	1		Off		DTE Ready
	0		Off		DTE Uncontrolled Not Ready
	0		Off		DTE Controlled Not Ready (a 0/1 pattern is transmitted on T circuit)
		1		Off	DCE Ready
		0		Off	DCE Not Ready
1	1	1	Off	Off	Ready (DTE and DCE are Ready)
2	0		On		Call Request
3		X		Off	Proceed to Select (X = DCE transmits contiguous "+" characters preceded by 2 or more SYN characters)
4	X		On		Selection Signal Sequence (X = DTE transmits selection sequence preceded by 2 or more SYN characters)
5	1		On		DTE Waiting
6		X		Off	DCE Waiting (X = DCE transmits 2 or more SYN characters)
7		X		Off	Call progress signal sequence (x = DCE transmits 1 or more call progress blocks
8		X		Off	Incoming Call (X = DCE transmits continuous BEL character preceded by 2 or more SYN characters
9	1		On		Call accepted (DTE accepts incoming call)
10		X		Off	DCE provided information sequence (X = DCE transmits 1 or more DCE provided information blocks)
11		1		Off	Connector in progress (DCE Ready - entered when connection is in progress)

Table B-4 (cont'd)
X.21 Signaling Conditions and States

State	Circuit				Description
	T	R	C	I	
12		1		On	Ready for Data (DCE signals that connection is available for data transfer.
13	X	X	On	On	Data Transfer (X = data transfer on circuits T and R.)
14	0	1	Off	Off	Quiescent State - DTE signals controlled not ready and DCE signals ready, simultaneously
15	0	X	On	Off	Call collision - DTE detects incoming call in response to call request
16	0		Off		DTE Clear Request to DCE
17		0		Off	DCE clear confirmation (DCE response to state 16)
18	1	0	Off	Off	Quiescent State - DTE signals ready and DCE signals not ready, simultaneously
19		0		Off	Clear Indication - DCE indicates clearing to the DTE
20	0		Off		DTE clear confirmation - response to state 19
21		1		Off	DCE ready - response to state 17 or 20.

RS-449-C Interface

RS-449 is a general purpose 37-position and 9 position interface for data terminal equiment (DTE), circuit equipment and data communications equipment (DCE), employing serial binary data interchange. The following paragraphs define the electrical signal characteristics of RS 449.

Table B-5 RS 449 Interface Summary

Pin	Circuit Mnemonic	Circuit Name	Source
19,37	Sg	Signal Ground	---
37	SC	Send Common	DTE
20	RC	Receive Common	DCE
28	IS	Terminal In Service	DTE
15	IC	Incoming Call	DCE
12,30	TR	Terminal Ready	DCE
11,29	DM	Data Mode	DCE
4,22	SD	Send Data	DCE
6,24	RD	Receive Data	DCE
17,35	TT	Terminal Timing	DCE
5,23	ST	Send Timing	DCE
8,26	RT	Receive Timing	DCE
7,25	RS	Request To Send	DCE
9,27	CS	Clear To Send	DCE
13,31	RR	Receiver Ready	DCE
33	SQ	Signal Quality	DCE
34	NS	New Signal	DCE
16	SF	Select Frequency	DCE
16	SR	Signaling Rate Selector	DCE
2	SI	Signaling Rate Indicator	DCE
10	LL	Local Loopback	DCE
14	RL	Remote Loopback	DCE
18	TM	Test Mode	DCE
32	SS	Select Standby	DCE
36	SB	Standby Indicator	DCE

Send Common - This conductor is connected to the DTE circuit ground.

Receive Common -This conductor is connected to the DCE circuit ground.

Terminal In Service - The ON condition indicates that the DTE is in service and, in switched network applications that employ line polling, allows incoming calls to be connected to the DCE. The OFF condition signals that the DCE is not availalbe for service. This may be caused by a DTE test condition.

Incoming Call - The ON condition indicates that an incoming call is being received by the DCE. The OFF condition is maintained during the OFF segment of the ringing cycle.

Terminal Ready - Signals on this circuit are used to control switching of the DCE to and from the communications channel.

Data Mode - The ON condition of this circuit indicates that the DCE is transmitting. The OFF condition is an indication that the DTE is to disregard signals appearing on all other interchange circuits with the exception of Circuit IC (Incoming Call), Circuit TM (Test Mode) and Circuit SB (Standby Indicator).

Send Data - The data signal originated by the DTE to be transmitted via the data channel to one or more remote data stations are transferred on this circuit to the DCE.

Receive Data - The data signals generated by the DCE in response to data channel line signals received from a remote data station are transferred on this circuit to the DTE.

Terminal Timing - Signals on this circuit provide the DCE with transmit signal element timing information.

Send Timing - Signals on this circuit provide the DTE with transmit signal element information.

Receive Timing - Signals on this circuit provide the DTE with receive element timing information.

Request to Send - Signals on this circuit control the data channel transmit function of the local DCE and, on a half duplex channel, control the direction of data transmission of the local DCE.

Clear To Send - Signals on this circuit indicate the transmit enable state on the data channel.

Receiver Ready - Signals on this circuit indicate that the DCE receiver may or may not be conditioned to receive data signals from the communication channel.

Signal Quality - Not supported

New Signal - Not supported

Select Frequency - Signals on this circuit are used to select the transmit and receive frequency bands of a DCE.

Signaling Rate Detector - Signals on this circuit are used to select one of the two data signaling rates of a dual rate synchronous DCE or to select one of the two ranges of data signaling rates of a dual range non-synchronous DCE.

Signaling Rate Indicator - Not supported.

Secondary Send Data (To DCE) - Not supported.

Secondary Receive Data (From DCE) - Not supported.

Secondary Request To Send (To DCE) - Not supported.

Secondary Clear To Send (From DCE) - Not supported.

Secondary Receiver Ready (From DCE) - Not supported.

Local Loopback (To DCE) - Not Supported.

Remote Loopback - Not supported.

Test Mode - Not supported.

Select Standby - Not supported.

APPENDIX
C
FIELD LEVEL DIAGNOSTIC ERROR CODES

APPENDIX C

FIELD LEVEL DIAGNOSTIC ERROR CODES

(702-0183) or (702-0240)

TEST NO.	TEST NAME	ERROR CODE	FAILING MODULE or DESCRIPTION
1	DMA/PIO	NONE	Screen display of the expected data and actual data.
2	DMA	NONE MULTIPLEXER TEST	Screen display of the failing address, expected data and actual data.
3	MOVING INVERSIONS	NONE	Screen display of the failing address, expected data and actual data.
4	SIO EXTERNAL LOOP	F0	Receiver failed to enter hunt mode in either Bisync or SDLC mode of testing. Display will give mode of testing.
		F1	Transmitter failing to send sync or flag characters during Bisync or SDLC mode of testing. Display will give mode of testing.
		F2	Receiver failed to receive sync or flag character and exit hunt mode. Display will give mode of testing.
		F3	Transmitter failing to transmit data characters. Display will give mode of testing.
		F4	Receiver failed to receive transmitted character. Display will give mode of testing.
		F5	Data error between transmitted and received character. Display will give mode of testing, expected and actual character.
		F6	Transmit interrupt failed to occur during Bisync mode of testing.

TEST NO.	TEST NAME	ERROR CODE	FAILING MODULE or DESCRIPTION
		F7	Receive interrupt failed to occur during Bisync mode of testing.
		F8	Overrun interrupt failed to occur during Bisync mode of testing.
		F9	CTS interrupt failed to occur during Bisync mode of testing.
		FA	DCD interrupt failed to occur during Bisync mode of testing.
		FB	DCD interrupt occurred when DCD was supposed to be turned off during Bisync mode of testing.
5	SIO/DMA	F0	SIO failed to enter hunt mode after initialization.
		F1	SIO failed to transmit sync characters after transmitter initialization.
		F2	SIO failed to receive sync characters and exit hunt mode.
		F3	Timed out waiting for transfer complete on channels 0 and 1 of the DMA chip.
		F4	CTC channel 2 downcounter failed to decrement as a result of EOP from the DMA.
		F5	Data error between transmitted and received data. Expected and actual data are displayed.
		F6	Parity error occurred during DMA transfer.
6	CC RAM	F0	Character was recognized during non-recognition test. The character that caused the failure which equivocates to the RAM address is displayed.

TEST NO.	TEST NAME	ERROR CODE	FAILING MODULE or DESCRIPTION
		F1	Character failed to be recognized during recognition test. The character that caused the failure which equivocates to the RAM address is displayed.
7	PRIORITY	F0	CTC interrupt failed to occur in allotted time.
		F1	SIO interrupt failed to occur after CTC interrupt had occurred and before a return from interrupt was executed.
		F2	PIO interrupt occurred before completion of service to the CTC interrupt (i.e., a return from interrupt has not been executed).
		F3	PIO interrupt failed to occur within the allotted time.
8	ACU LOOP BACK TEST	F0	The all 00's test failed.
		F1	The sliding bit test failed.

APPENDIX D

RAM CHIP LAY-OUTS

APPENDIX D

RAM CHIP LAYOUTS

RAM chip layout for the 210-7659-3C (64K) daughterboard is shown below. The RAM (WLI #377-0345-M) is 16K x 1 bit format.

Bank #	Bit Weight								
	80	40	20	10	8	4	2	1	P
1 (0000 to 3FFF)	L13	L12	L11	L10	L9	L8	L7	L6	L5
3 (8000 to BFFF)	L26	L25	L24	L23	L22	L21	L20	L19	L18
2 (4000 to 7FFF)	L39	L38	L37	L36	L35	L34	L33	L32	L31
4 (C000 to FFFF)	L53	L52	L51	L50	L49	L48	L47	L46	L45

RAM chip layout for the 210-7855-A (128K) daughterboard is shown below. The RAM (WLI #377-0645) is 64K x 1 bit format.

Bank #	Bit Weight								
	80	40	20	10	8	4	2	1	P
1 (0000 to FFFF)	L7	L14	L22	L30	L38	L40	L50	L52	L61
2 (10000 to 1FFFF)	L8	L15	L23	L31	L39	L41	L51	L53	L62

APPENDIX
E
EIA INTERFACE TEST SET AND BREAKOUT BOXES

APPENDIX E

EIA INTERFACE TEST SET AND BRE/KOUT BOXES

An EIA Interface Test Set or "Breakout Box" is a self-contained pocket size test set that can be inserted between the Data Communication Equipment (DCE) or modem and Data Terminal Equipment (DTE). Breakout Boxes allow the user to monitor the interface signals and to isolate and identify sources of trouble.

A Breakout Box contains indicators which continuously monitor the level of the EIA sensing circuits which drive LEDs to indicate the ON or OFF levels of the following EIA signals - transmitted data, received data, request to send, clear to send, data set ready, received carrier detect, data terminal ready, signal quality detect and ring indicator.

Two indicators also monitor the transmit and receive clock signals. Two additional uncommitted indicators are available for monitoring either positive or negative levels on any of the interface lines.

Breakout Boxes also contain 24 switches which allow any of the interface signals except line one (Frame Ground) to be interrupted. These switches are physically located in the center of the front panel and functionally divide the test set into two halves. One half contains a cable and connector for connecting the test set to the DCE (data communications equipment) or modem. The other half of the Test Set contains a connector to which the DTE (Terminal or CPU) can be connected .

Twenty five pins are located on both sides of the switches. These pins permit monitoring of any of the interface lines with either or both of the positive and negative test indicators with jumpers supplied or by probing with an external meter or oscilloscope.

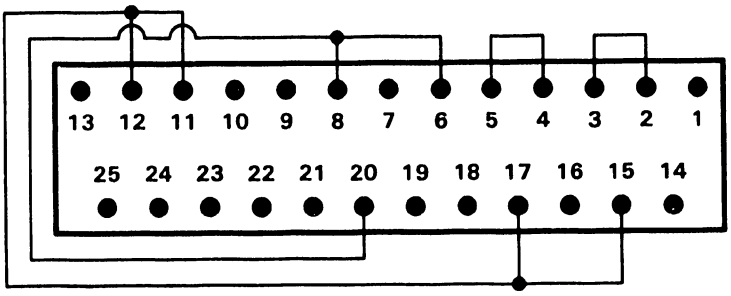
To operate a test set, the EIA RS-232 interface cable from the modem is unplugged and plugged into the Test Set 25-pin female connector labeled "To DCE" (data communications equipment). The Test Set male connector, labeled "To DCE" is then connected directly to the modem.

APPENDIX F

LOOP-BACK CONNEC-TOR DIAGRAMS

APPENDIX F

LOOPBACK CONNECTOR DIAGRAMS

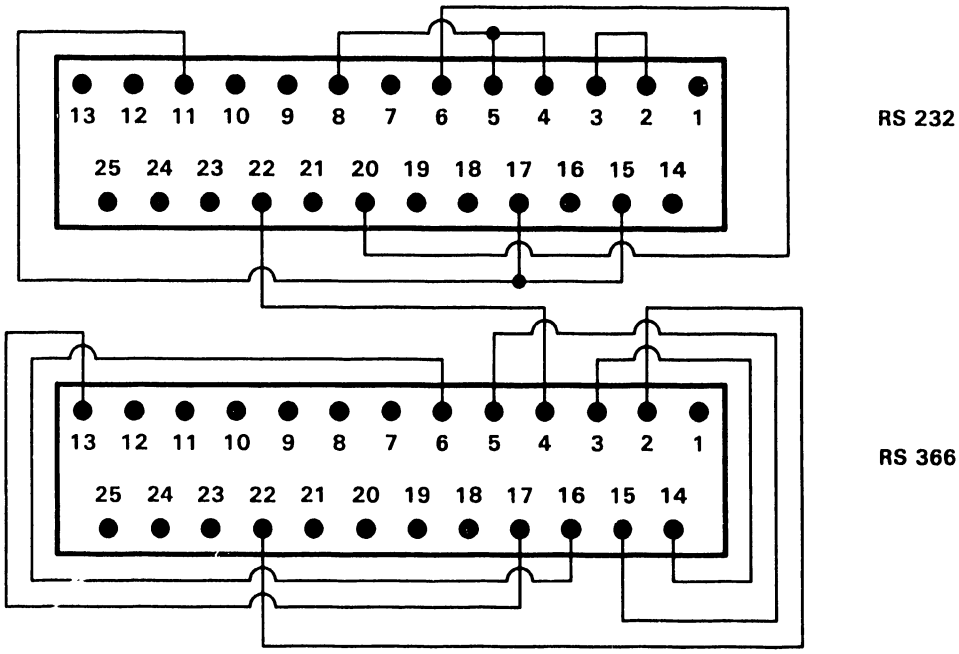


350-1030 DB-25P CH Connector 6000 Series

Pins	Description
2	Transmit Data
3	Receive Data
4	Request to Send
5	Clear to Send
6	Data Set Ready
8	Receive Line Sig Detector
11	Secondary Req to Send
12	Secondary Rec'd Line Sig Det
15	Receiver Sig Element Tim
17	Receiver Sig Element Tim
20	Data Terminal Ready

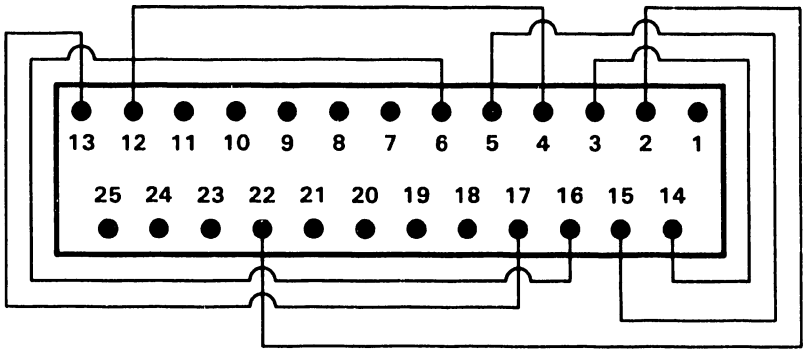
Jumper Pin Location	
From	To
2	3
4	5
6	8
8	20
11	12
12	15
15	17

Figure F-1 RS-232 Loopback Connector (WLI #420-1040)



	Pins	Description	Jumper Pin Location	
RS-232			RS-232	
	2	Transmit Data	From	To
	3	Receive Data	2	3
	4	Request to Send	4	5
	5	Clear to Send	5	8
	6	Data Set Ready	6	20
	8	Receive Line Sig Detector	11	15
	11	Secondary Req to Send	15	17
	12	Secondary Rec'd Line Sig Det		22--|
	15	Receiver Sig Element Tim		|
	17	Receiver Sig Element Tim	RS-366	|
	20	Data Terminal Ready		|
	22	Ring Indicator		4--|
RS-366			2	22
	2	Digit Present	3	14
	3	Abandon Call and Retry	5	15
	4	Call Request	6	16
	5	Present Next Digit	13	17
	6	Power Indication		
	13	Data Set Status		
	14	Digit Bit 0 (LSB)		
	15	Digit Bit 1		
	16	Digit Bit 2		
	17	Digit Bit 3		
	22	Data Line Occupied		

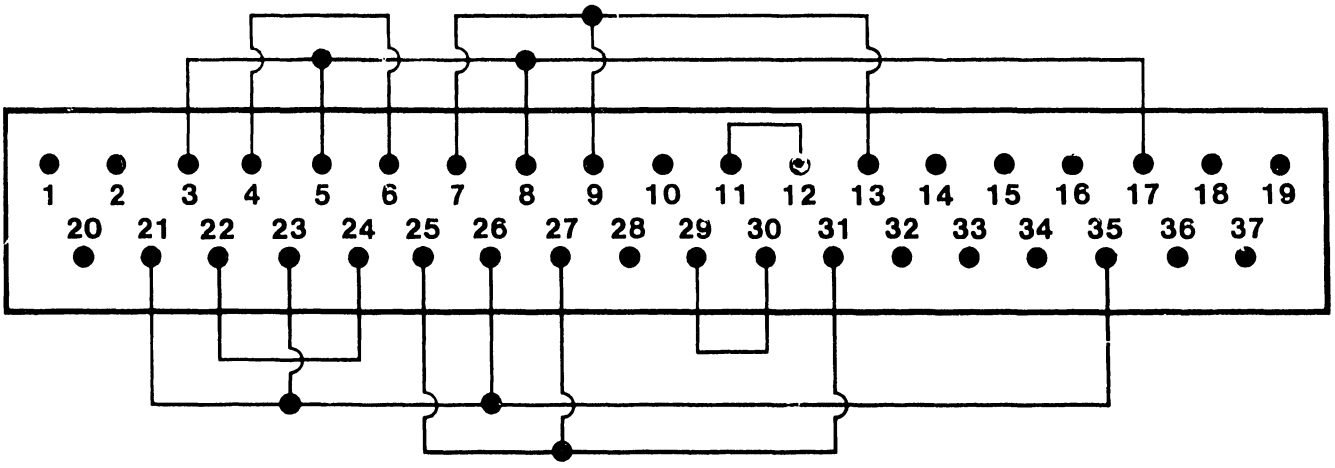
Figure F-2 RS-232-366 Loopback Connector (WLI #420-1041)



RS 366

Pins	Description	Jumper Pin Location	
		From	To
2	Digit Present	2	22
3	Abandon Call and Retry	3	14
4	Call Request	4	12
5	Present Next Digit	5	15
6	Power Indication	6	16
12	Secondary Carrier Detect	13	17
13	Data Set Status		
14	Digit Bit 0 (LSB)		
15	Digit Bit 1		
16	Digit Bit 2		
17	Digit Bit 3		
22	Data Line Occupied		

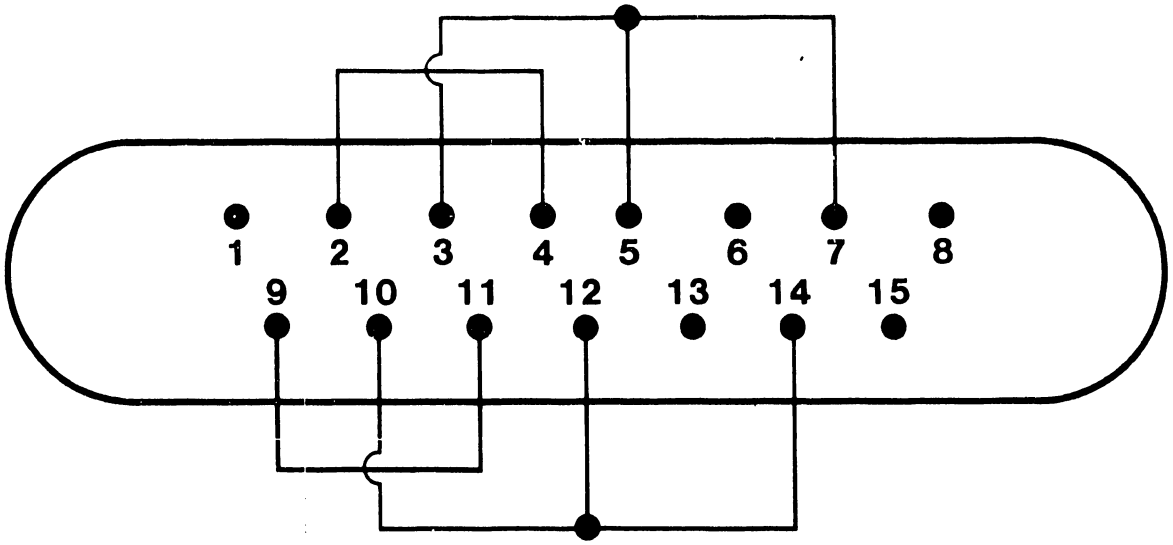
Figure F-3 RS-366/ACU Loopback Connector (WLI #420-1104)



DC-37S Connector 6000 Series WLI #350-1033

Pins	Description		Jumper Pin Location	
			From	To
3	Spare		3	5
21	Spare		4	6
4	Send Data	(+)	5	8
22	Send Data	(-)	7	9
5	Send Timing	(+)	8	17
23	Send Timing	(-)	9	13
6	Receive Data	(+)	11	12
24	Receive Data	(-)	21	23
7	Request to send	(+)	22	24
25	Request to send	(-)	23	26
8	Receive Timing	(+)	25	27
26	Receive Timing	(-)	26	35
9	Clear to Send	(+)	27	31
27	Clear to Send	(-)	29	30
11	Data Mode	(+)		
29	Data Mode	(-)		
12	Terminal Ready	(+)		
30	Terminal Ready	(-)		
13	Receive Ready	(+)		
31	Receive Ready	(-)		
17	Terminal Timing	(+)		
35	Terminal Timing	(-)		

Figure F-4 RS-449 Loopback Connector (WLI #270-3193)



Female Connector 15 Pos. D Series WLI #350-1068

Pins	Description		Jumper Pin Location	
			From	To
2	Transmit	(+)	2	4
9	Transmit	(-)	3	5
4	Receive	(+)	5	7
11	Receive	(-)	9	11
5	Indication	(+)	10	12
12	Indication	(-)	12	14
3	Control	(+)		
10	Control	(-)		
7	Byte Timing	(+)		
14	Byte Timing	(-)		

Figure F-5 X.21 Loopback Connector (WLI # 421-0010)

CHAPTER 6 SCHE-MATICS

CHAPTER 6

SCHEMATICS

This chapter contains the following schematic drawings:

Part No.	Sheets	Title
210-7659	4	TC Controller, Daughterboard (64K)
210-7855	5	TC Controller, Daughterboard (128K)
210-7857	5	TC Controller, Motherboard (RS-449)
210-7858	6	TC Controller, Motherboard (RS-232)
210-7859	5	TC Controller, Motherboard (X.21)

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DO NOT SCALE

TCWRE (53) · ERFSH (59) · MCK (52) · DMREQ (60) · OUT0 (11) · OUT1 (21)

L43 Z80A CPU

L44 2716

L16 LS373

L42 AM9517A-1

L17 LS241 TL

L20 LS241

L29 LS75 · L28 LS139 · L14 S194 · L15 LS75 · L26 LS139

L61 LS74 · L54 LS280 · L58 2102A-2

L40 LS04 · LS125 · L3 LS32 · L4 LS08 · L2 04 · L95 LS32 · L57 LS08 · L56 LS74

R21 4.7K +5VR · R44 10K · R43 10K · R35 10K · R34 10K · R36 10K · R33 10K · R23 4.7K · R24 4.7K · R22 4.7K · R37 10K · R41 10K · R42 10K · R32 4.7K · R38 10K · R11 AOVA7 33Ω · R12 AOVA7' 33Ω · R19 AIVA8 33Ω · R20 AIVA8' 33Ω · R15 A2VA9 33Ω · R16 A2VA9' 33Ω · R9 A3VA10 33Ω · R10 A3VA10' 33Ω · R13 33Ω AGVAI1 · R19 AGVAI1' 33Ω · R17 A5VA12 33Ω · R18 A5VA12' 33Ω · R7 AGVAI3 33Ω · R8 ALVAI3' 33Ω · R30 10K · R40 2.2K · R39 4.7K · R31 2.2K · R29 33Ω · R1 33Ω · R4 33Ω · R5 33Ω · R2 33Ω · R3 33Ω · R6 2.2K

AOVA7 - AGVAI3 (2F10) · AOVA7' - AGVAI3' (2F10) · D8-D7 (2G9) · AEN (1A10) · DACK0 (1A11) · DACK1 (1A10) · TCBUSAK (1B3) · TCWRE (2E9) · RESET (1E11) · TCBUSAK (1C11) · TCNMI (1F10) · RAS0 (2G9) · RAS1 (2E9) · RAS2 (2D9) · RAS3 (2C9)

RESET (4T) · RESET (1B4) (1E2) · TCBUSAK (43) · IOTIX (14) · SIORDY (56) · SIOWR (57) · MI (46) · BRDY (55) · DRQ (54) · I/OW (54) · AEN (3) · REQ (2) · ZOP (18) · WR (12) · MEN (41) · DACK3 (49) · DACK2 (51) · DACK1 (48) · DACK0 (50) · ERFSH (58) · DMREQ (32) · IORQ (17) · MI (20) · RD' (29)

JMPR1 · JMPR2 · JMPR3 · JMPR4

BY	DATE	APPROVED BY	DATE
DWNR ROLL-BLAKE IV	2-15-82	E ENGR	
CHK		M ENGR	
		MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL · FINISH

MODEL NO. 2228D

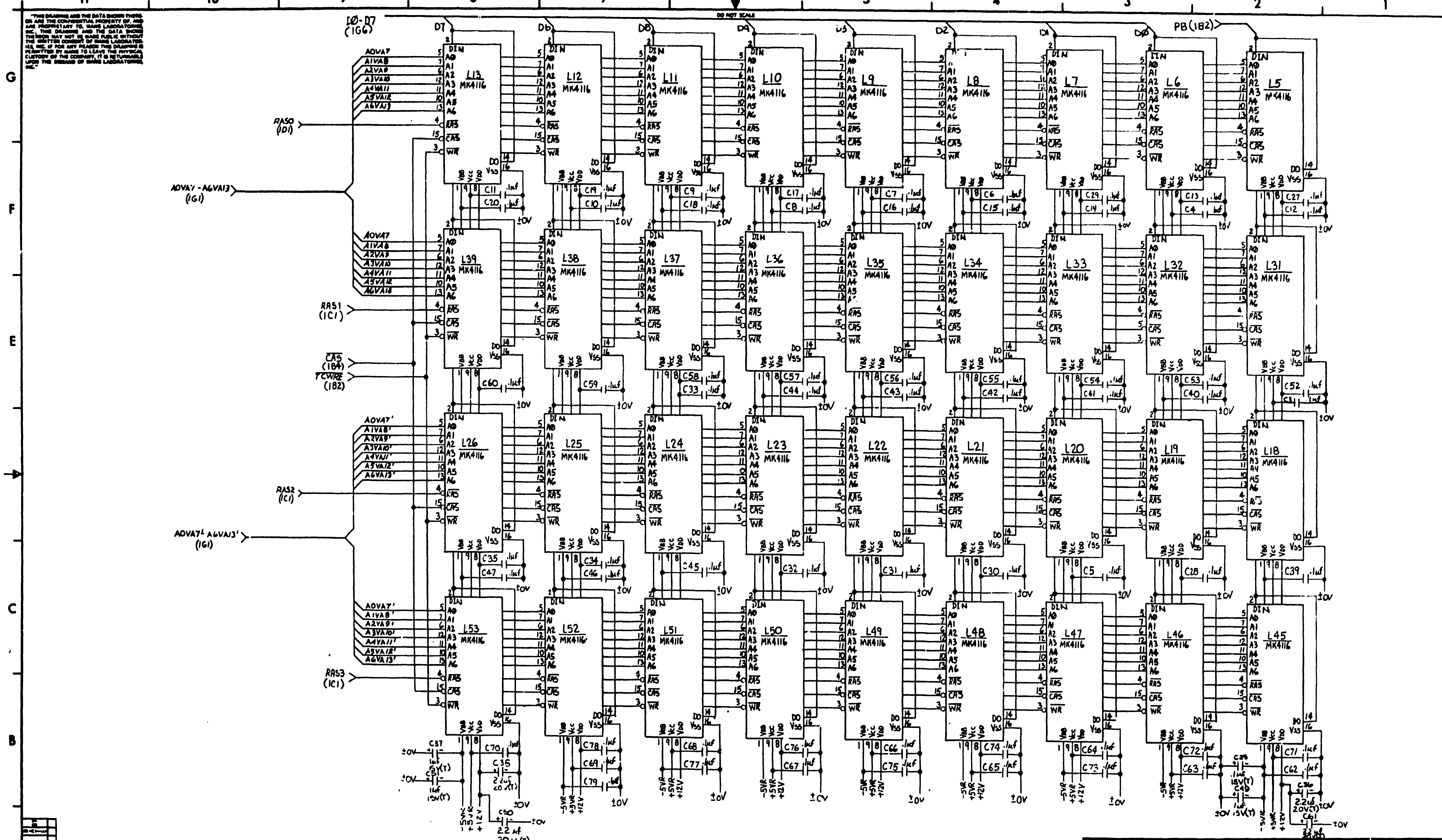
SEE BOARD SPECIFICATIONS

TOL. EX. AS NOTED FRAC. ± DEC. ± ANG. ± FINISH √

TITLE: TELECOMMUNICATION CONTROLLER DAUGHTER BOARD

SEE CHART · D · 7659 · 12

SCALE · SHT · OF 4 · WANG PART NUMBER · SIZE · DRAWING NUMBER · REV.



WANG LABORATORIES, INC.	BY	DATE	APPROVED BY	DATE
	DWN	2/14	E ENGR	
	CHK		M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO. 2228 D

SEE ENGRG. SPECIFICATIONS

No.

FINISH

TOL. EX. AS NOTED
.XX ± FRAC. ±
.XXX ± ANG. ± FINISH

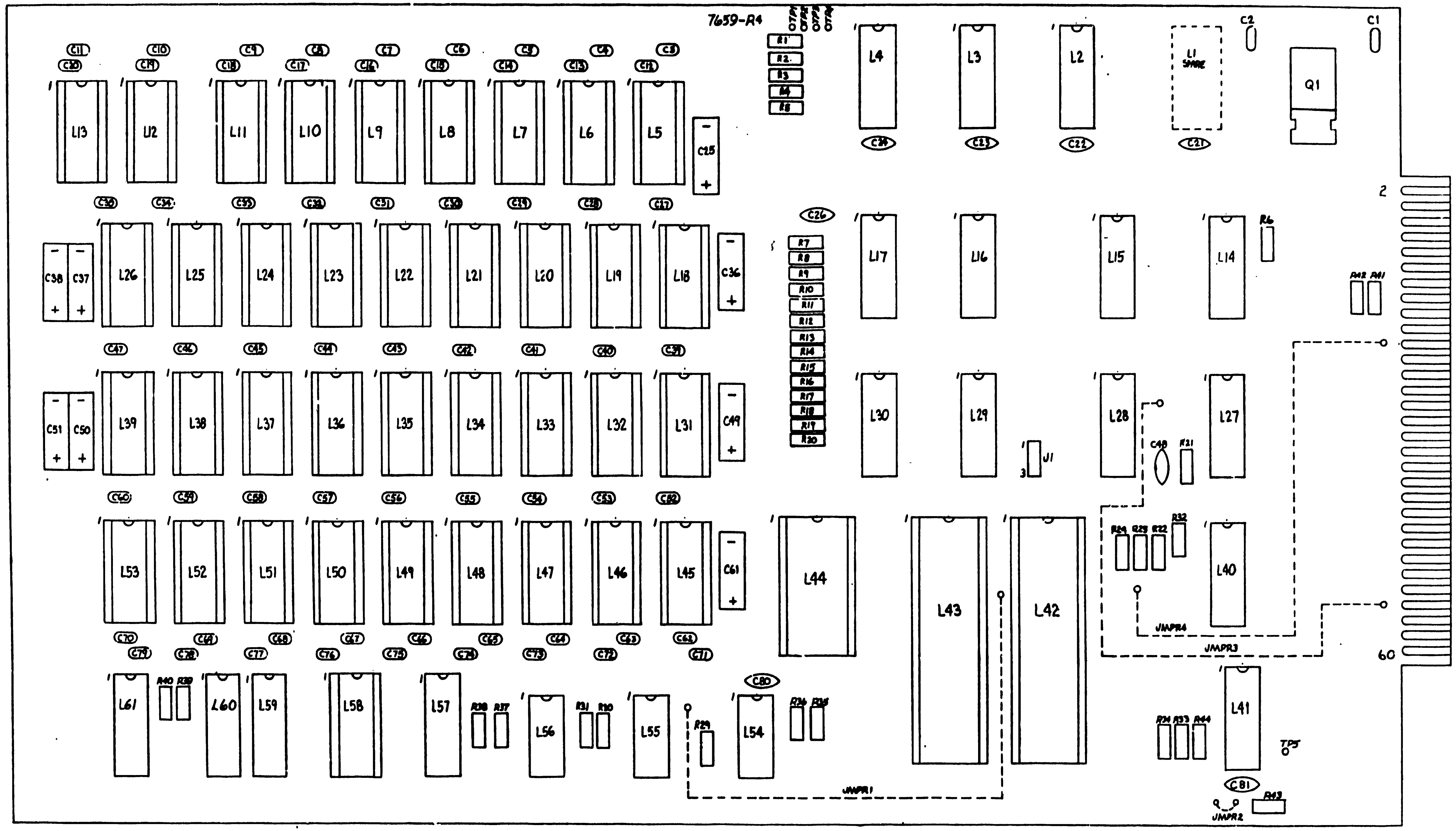
SCALE SHT 2 OF 4

TITLE TELECOMMUNICATION CONTROLLER DAUGHTER BOARD

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
SEE CHART	D	7659	12

D 7659

REVISION



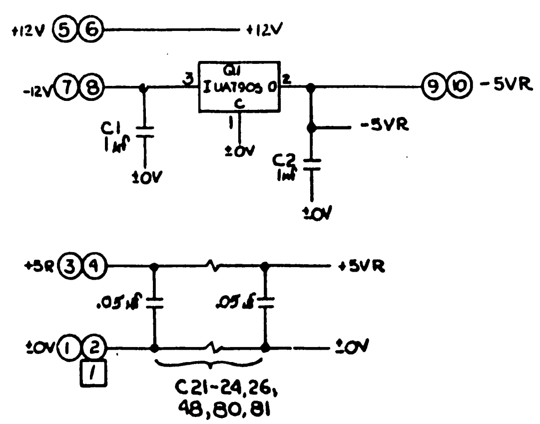
SEE SHT FOR REV.

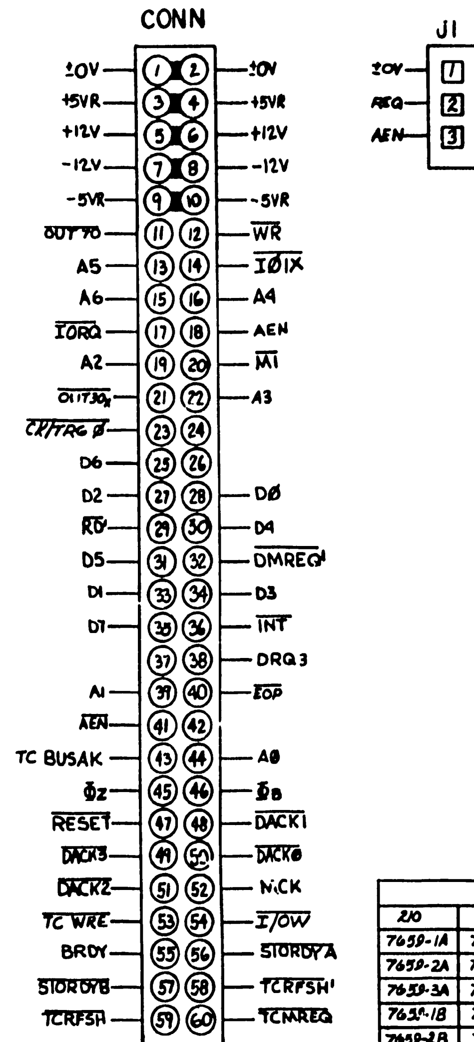
WANG LABORATORIES, INC.	BY	DATE	APPROVED BY
	POLUBINSKY	2-8-80	
MODEL NO. 2228D	TITLE TELECOMMUNICATION CONTROLLER DAUGHTER BOARD		
SEE CHART	D	7659	12

COMPONENT	TYPE	W.L. PART NO.
Q1	UA7905	374-0002
R1-5,7-20,29	33Ω, ¼W, 10%	330-1033
R6,31,40	2.2K, ¼W, 10%	330-3022
R21-24,32,39	4.7K, ¼W, 10%	330-3047
R30,33-38,41-44	10K, ¼W, 10%	330-4010
C1,2	1 µf, 50V	300-1931
C3-20,27-35,39-47,52-60,62-79	.1 µf, 50V	300-1930
C21-24,26,48,80,81	.05 µf, 12V	300-1900
C25,31,49,51	1 µf, 15V(T)	300-4056
C36,38,50,61	2.2 µf 20V(T)	300-9019
J1	3 POS. HEADER	654-0104

IC LOCATION	W.L. PART NO.	TYPE
L1		SPARE
L2	376-0010	7404
L3,55,59	376-0211	74LS32
L4,57	376-0153	74LS08
L5-13,18-26,31-39,45-53	SEE CHART	MK4116
L14	376-0221	74S194
L15,29	376-0312	74LS75
L16	376-0310	74LS373
L17,30	376-0284	74LS241
L28	376-0226	74LS139
L41,60	376-0486	74LS125
L42	SEE CHART	AM9517A-1
L43	SEE CHART	Z80ACPU
L44	SEE CHART	TMS 2716
L54	376-0242	74LS280
L56,27,61	376-0155	74LS74
L40	376-0180	74LS04
L58	SEE CHART	2102A-2
L5-13,18-26,31-39,45-53	SKT, 16 PIN	376-9002
L42,43	SKT, 40 PIN	376-9011
L44	SKT, 24	376-9003

IC TYPE	LOCATION	SPARES
7404	L2	2
74LS32	L3	1
	L59	3
74LS74	L61	1
74LS125	L60	1





MNEMONIC	COORD.
AØ-A6	1G1
AEN	1A7
AEN	1A9
BRDY	1B11
DØ-D7	1G11
CK/TRG Ø	1F1
DACKØ-DACK3	1A7
DMREQ'	1A6
DRQ3	1B11
IØIX	1D11
ΦB	1B11
Φz	1F11
INT	1F11
IORQ	1A6
MCR	1G6
MI	1A6
RD'	1A5
RESET	1E11
SIORDYA	1B11
SIORDYB	1B11
TC	1A9
TCBUSAK	1C11
TCMREQ	1G5
TCRFSH	1G6
TCRFSH'	1A6
TCWRE	1G7
WR	1A7
OUT 30	1G2
OUT 70	1G2
I/OW	1A10
EOP	1A9
REQ	1A8

210 = 209 + 377 OR 378								
210	209	L5-13,31-39	L18-26	L42	L43	L44	L45-53	L58
7659-1A	7659-1	377-0345		377-0388	377-0368	378-4379-R1		377-0363
7659-2A	7659-2	377-0345	377-0345	377-0388	377-0368	378-4380-R1		377-0363
7659-3A	7659-3	377-0345	377-0345	377-0388	377-0368	378-4381-R1	377-0345	377-0363
7659-1B	7659-1	377-0345		377-0388	377-0368	378-4235-R2		377-0363
7659-2B	7659-2	377-0345	377-0345	377-0388	377-0368	378-4235-R2		377-0363
7659-3B	7659-3	377-0345	377-0345	377-0388	377-0368	378-4235-R2	377-0345	377-0368
7659-1C	7659-1	377-0345		377-0388	377-0368	378-4388		377-0363
7659-2C	7659-2	377-0345	377-0345	377-0388	377-0368	378-4389		377-0363
7659-3C	7659-3	377-0345	377-0345	377-0388	377-0368	378-4390	377-0345	377-0363
7659-1D	7659-1	377-0345		377-0388	377-0368	378-4391		377-0363
7659-2D	7659-2	377-0345	377-0345	377-0388	377-0368	378-4391		377-0363
7659-3D	7659-3	377-0345	377-0345	377-0388	377-0368	378-4391	377-0345	377-0363

E-REV

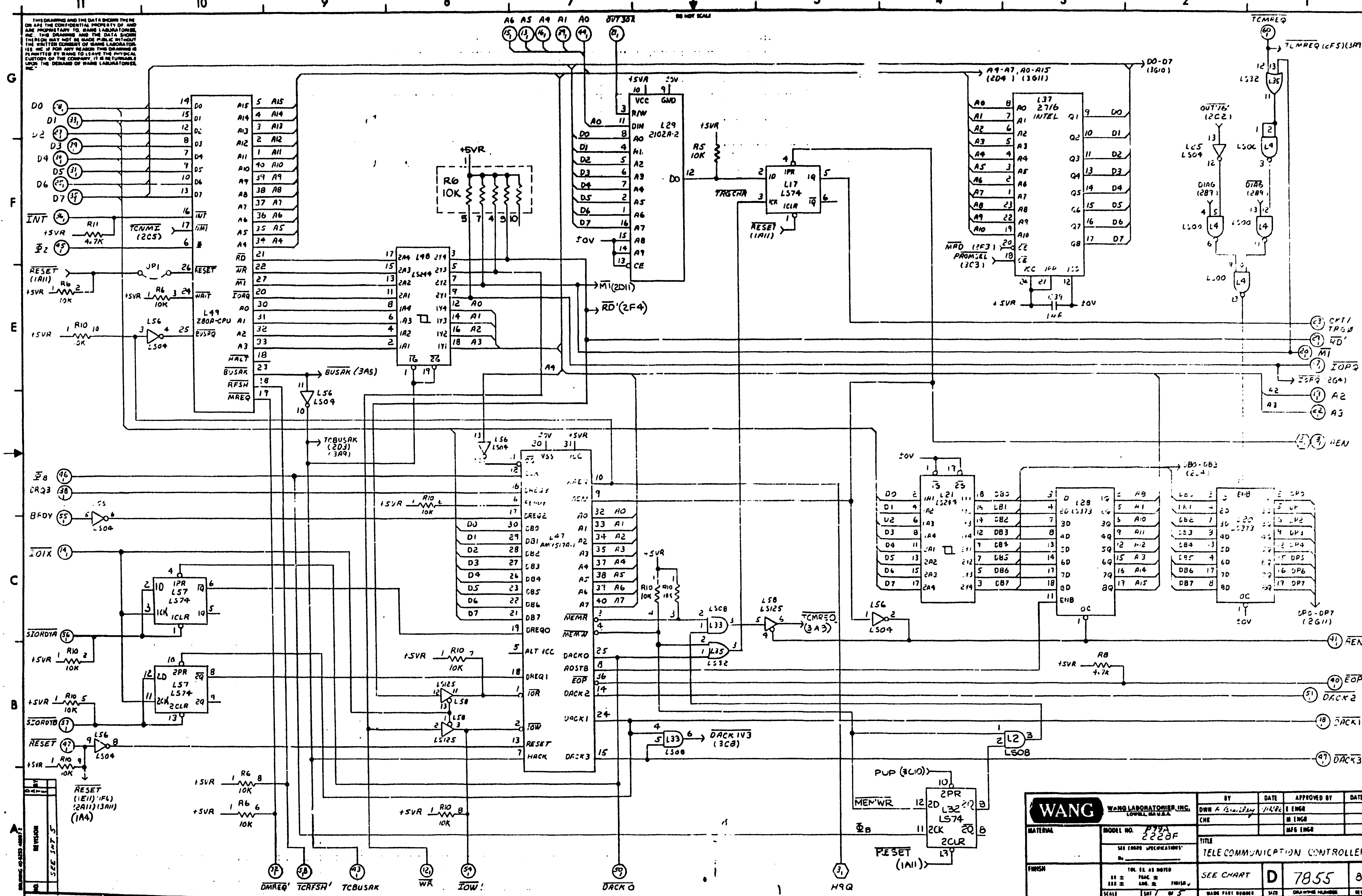
2	0	0	0
7659	7659-1	7659-2	7659-3

WANG LABORATORIES, INC.

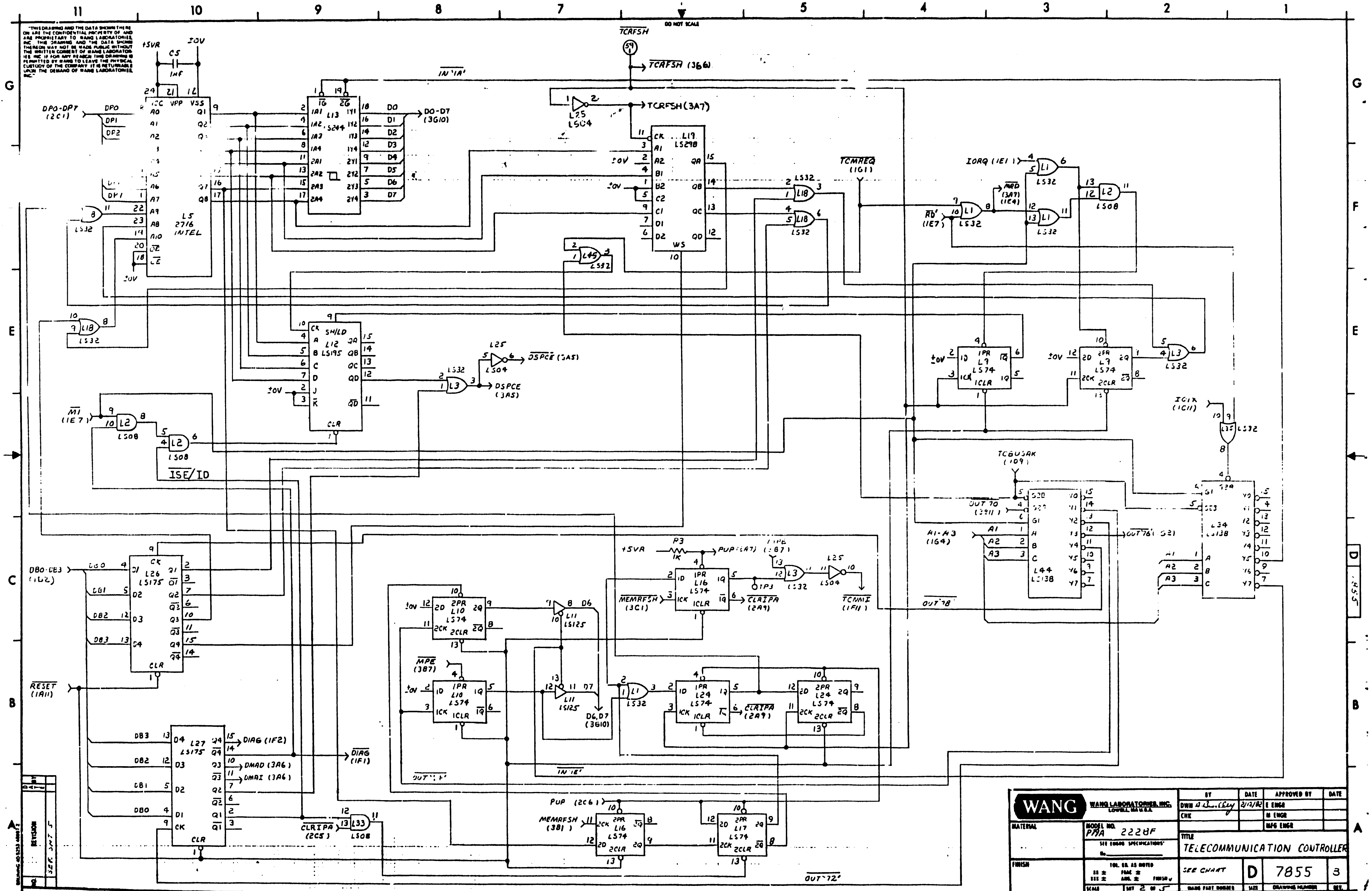
MODEL NO. 2228D

TITLE: TELECOMMUNICATION CONTROLLER DAUGHTER BOARD

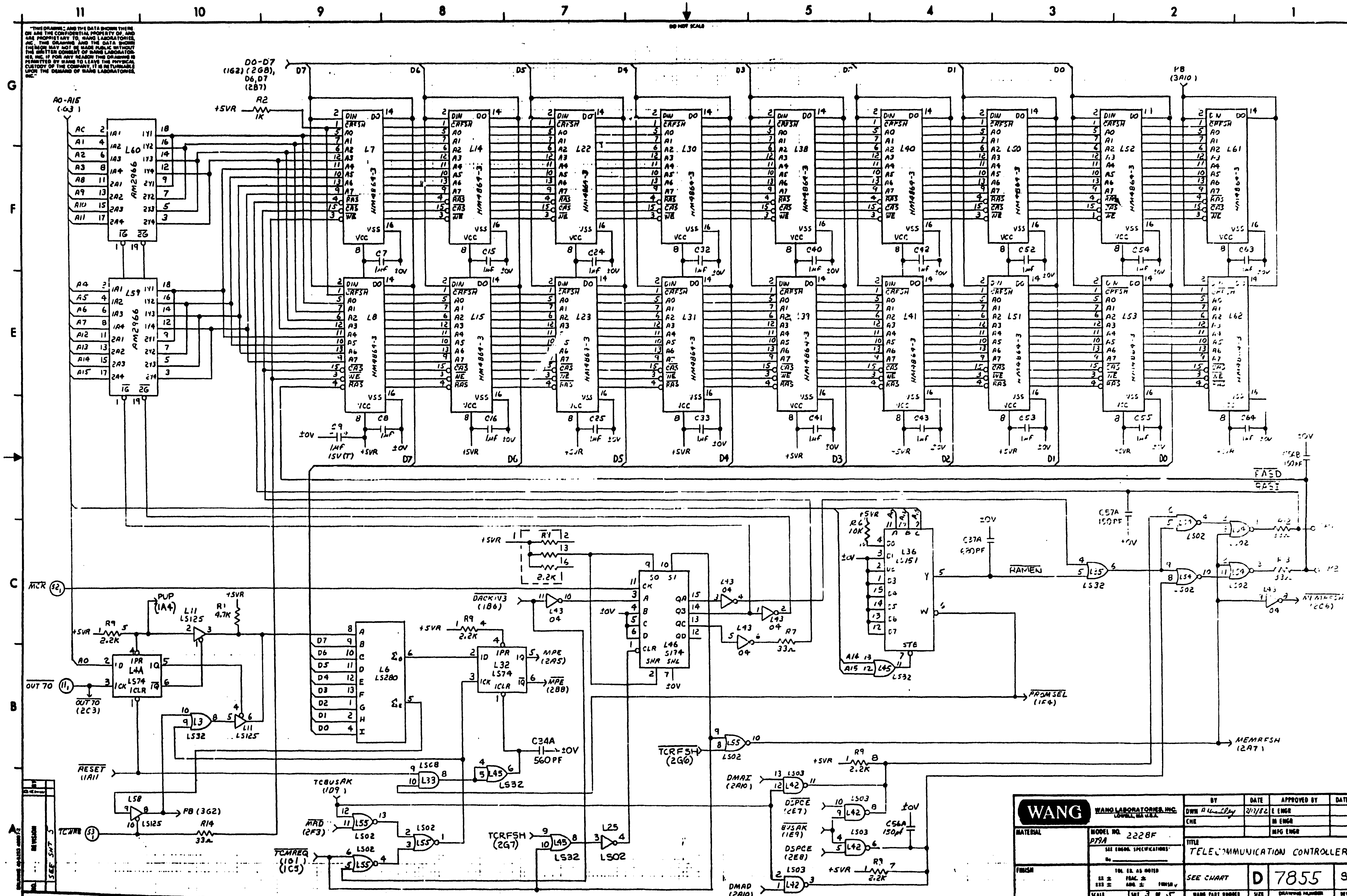
SEE CHART | D | 7659



WANG
WANG LABORATORIES, INC.
LOWELL, MA U.S.A.
TELE COMMUNICATION CONTROLLER
SEE CHART
D
7855
8
MODEL NO. P79A
2228F
L49
Z80A-CPU
L47
AM9517A-1
L29
2102A-2
L37
2716
INTEL
L48
LS244
L17
LS74
L57
LS74
L32
LS74
L21
LS244
L28
LS373
R6
10K



WANG
WANG LABORATORIES, INC.
LOWELL, MA U.S.A.
MODEL NO. PMA 2228F
TELECOMMUNICATION CONTROLLER
SEE CHART
D
7855
3
DO NOT SCALE
TCRFSH
TCRFSH (3G6)
TCRFSH (3A7)
L5
2716
INTEL
L13
LS244
L19
LS298
L12
LS195
L26
LS175
L27
LS175
L44
LS138
L34
LS138
L10
LS74
L16
LS74
L17
LS74
L24
LS74
L9
LS74
L11
LS125
DO-D7 (3G10)
DPO-DP7 (2C1)
IN 'IA'
TCMREQ (1G1)
IORQ (1E1)
DSPCE (3A5)
DSPCE (3A5)
ISE/ID
DBO-DB3 (1D2)
RESET (1A11)
DIAG (1F2)
DIAG (1F1)
DMAD (3A6)
DMAI (3A6)
CLRIPA (2C5)
CLRIPA (2A9)
MEMRFSH (3C1)
MEMRFSH (3B1)
PUP (2C6)
MPE (3B7)
TCNMI (1F11)
TCBUSAK (1G9)
A1-A3 (1G4)
D6,D7 (3G10)
IN 'IE'
OUT '78'
OUT '72'
+5VR
0V



WANG

WANG LABORATORIES, INC.
LOWELL, MA U.S.A.

BY	DATE	APPROVED BY	DATE
DWN	2/17/82	E ENGR	
CHK		M ENGR	
		MFG ENGR	

MATERIAL

MODEL NO. 2228F
PT9A

SEE ENGRG. SPECIFICATIONS

TITLE: TELECOMMUNICATION CONTROLLER

FINISH

TOL. EX. AS NOTED

SEE CHART

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
SEE CHART	D	7855	8

SCALE | SHT 3 OF 5

DO NOT SCALE

7855- -R3

REVISION	DATE	APPROVED

	BY	DATE	APPROVED BY	DATE
DWN	A Cawley	1/11/82	E ENGR	
CHK			M ENGR	
			MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL

MODEL NO. P79A 2228F

SEE ENGRG. SPECIFICATIONS

No.

FINISH

TOL. EX. AS NOTED

.XX ±. .XXX ±. FRAC. ± ANG. ± FINISH √

TITLE: TELECOMMUNICATION CONTROLLER

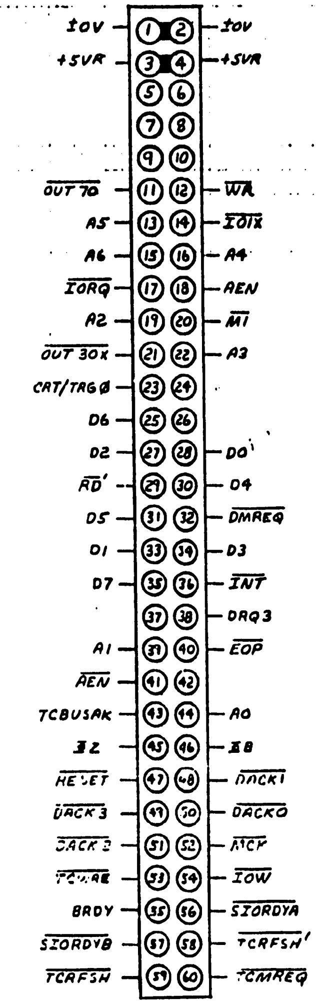
SCALE	SHT 1 OF 5	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
SEE CHART			D	7855	8

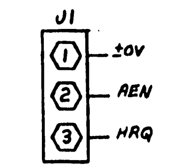
D 7355

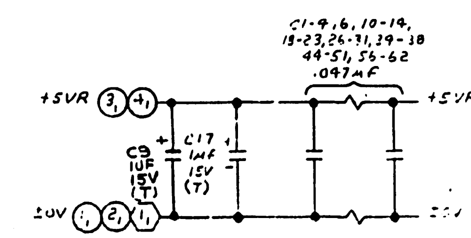
I.C. LOCATION	TYPE	W.L. PART NO.
L1,3,18,35,45	74LS32	376-0211
L2,33	74LS08	376-0153
L4	74LS00	376-0297
L5,37	2716	SEE CHART
L6	74LS280	376-0242
L7,8,14,15,22,23, 30,31,38-41, 50-53,61,62	HM4864-3	SEE CHART
L9,10,16,17,24, 32,57,4A	74LS74	376-0155
L11,58	74LS125	376-0486
L12	74LS195	376-0248
L13,21,48	74LS244	376-0288
L19	74LS298	376-0232
L20,28	74LS373	376-0310
L25,56	74LS04	376-0180
L26,27	74LS175	376-0160
L29	2102A-2	SEE CHART
L34,44	74LS138	376-0294
L36	74LS151	376-0214
L4?	74LS03	376-0224
L43	7407	376-0310
L46	74S174	376-0221
L47	AM9517A-1	SEE CHART
L49	Z80A-CPU	SEE CHART
L54,55	74LS02	376-0208
L59,60	AM2966	SEE CHART
L5,37	24 PIN SKT	376-7003
L7,8,14,15,22,23, 29-31,38-41, 50-53,61,62	16 PIN SKT	376-7002
L47,49	40 PIN SKT	376-7011

COMPONENT	TYPE	W.L. PART NO.
R1,8,11	4.7K 1/4W 5%	330-3048
R2,3,	1K 1/4W 5%	330-3011
R5	10K 1/4W 5%	330-4011
R6,10	10K SIP	333-0809
R7,12,13,14	33Ω 1/4W 5%	330-1034
R9	2.2K SIP	333-0906
C34A	560PF 50V.	3?0-1562
C1-4,6,10-14, 18-23,26-31,34-38, 44-51,56-62	.047μF 50V	300-1966
C5,7,8,15,16,24, 25,32,33,39-43, 52-55,63,64	1μF 50V	300-1931
C9,17	1μF 15V (T)	300-4056
C56A,56B,57A	150pf 50V	300-1150
C37A	680 PF 50V	300-1682
J1	3 POS PIN HDR	654-0104

MNEMONICS	COORD
A0,A1	1G7
A2,A3	1D1
A4-A6	1G7
AEN	1D1
$\overline{AEN}$	1C1
BRDY	1C11
CRT/TRGØ	1E1
$\overline{DACK0}$	1A7
$\overline{DACK1}$ - $\overline{DACK3}$	1B1
D0-D7	1G11
$\overline{DMREQ}$	1A7
DRQ3	1D11
$\overline{EOP}$	1B1
HRQ	1A5
Φ8	1D11
Φ2	1F11
$\overline{INT}$	1F11
$\overline{IO1X}$	1C11
$\overline{IOW}$	1A8
$\overline{IORQ}$	1E1
$\overline{M1}$	1E1
$\overline{MCK}$	3C11
$\overline{OUT 30X}$	1G7
$\overline{OUT 70}$	3B?1
$\overline{RESET}$	1B11
$\overline{RD'}$	1E1
$\overline{SIORDYA}$	1C11
$\overline{SIORDYB}$	1B11
TCBUSAK	1A9
$\overline{TCMREQ}$	1G1
$\overline{TCRFSH'}$	1A9
$\overline{TCRFSH}$	2G6
$\overline{TCWRE}$	3A11
$\overline{WR}$	1A8







I.C TYPE	LOCATION	SPARES
7404	L43	1
74LS74	L4A	1

210 = 209 + 377 OR 378							
210	209	L37	L7,8,14,15,22, 23,30,31,38-41, 50-53,61,62	L29	L47	L49	L5
7855A	7855	378-5145	377-0465	377-0363	377-0388	377-0368	378-5137

E-REV 1

NOTE:
1. ALL RES. ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

REVISION: ORIGINATED PER DWG# L1508 — A.B. 2.12.82; REVISED PER ECO — JEP; REVISED PER ECO#23003P — A.B. 6.8.82; REVISED PER ECO#24113, 24181 — PED 8.25.82; REVISED PER ECO — KM(?) 12.17.82; REVISED PER ECO#26328 — D.S.S. 2.28.83; REVISED PER ECO#26749 — 1.8.83; REVISED PER ECO#28007D — GHW 6.2.83; REVISED PER ECO#28050 — KTH 6.16.83

WANG LABORATORIES, INC. LOWELL, MA U.S.A.

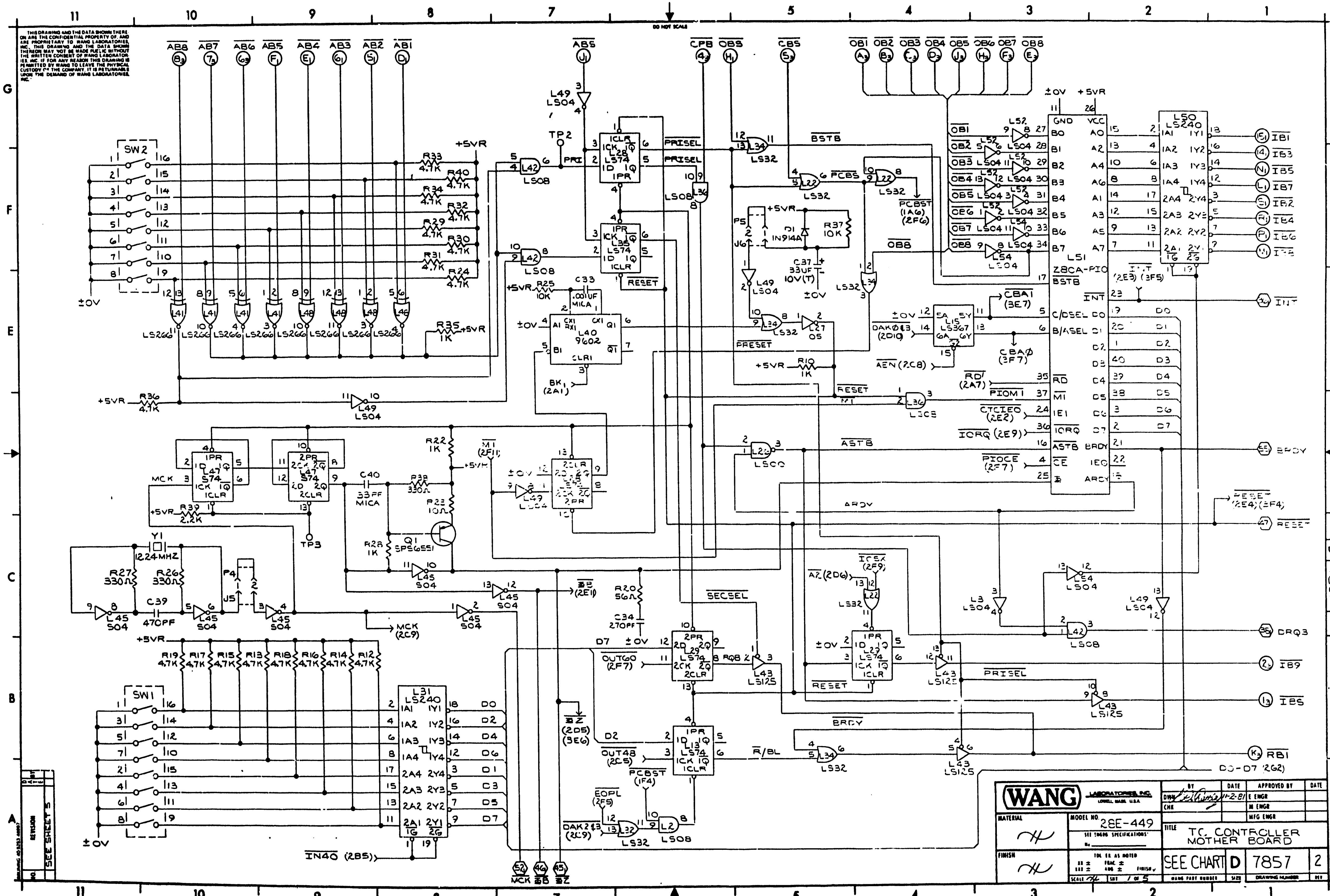
BY	DATE	APPROVED BY	DATE
DWN A. Bradley	2.12.82	E ENGR	2.25.82
CHK D. T. CORBIN	2.25.82	M ENGR	
		MFG ENGR	

MODEL NO. 2??A 2228F

TITLE: TELECOMMUNICATION CONTROLLER

SEE CHART | D | 7855 | 8

SHT 5 OF 5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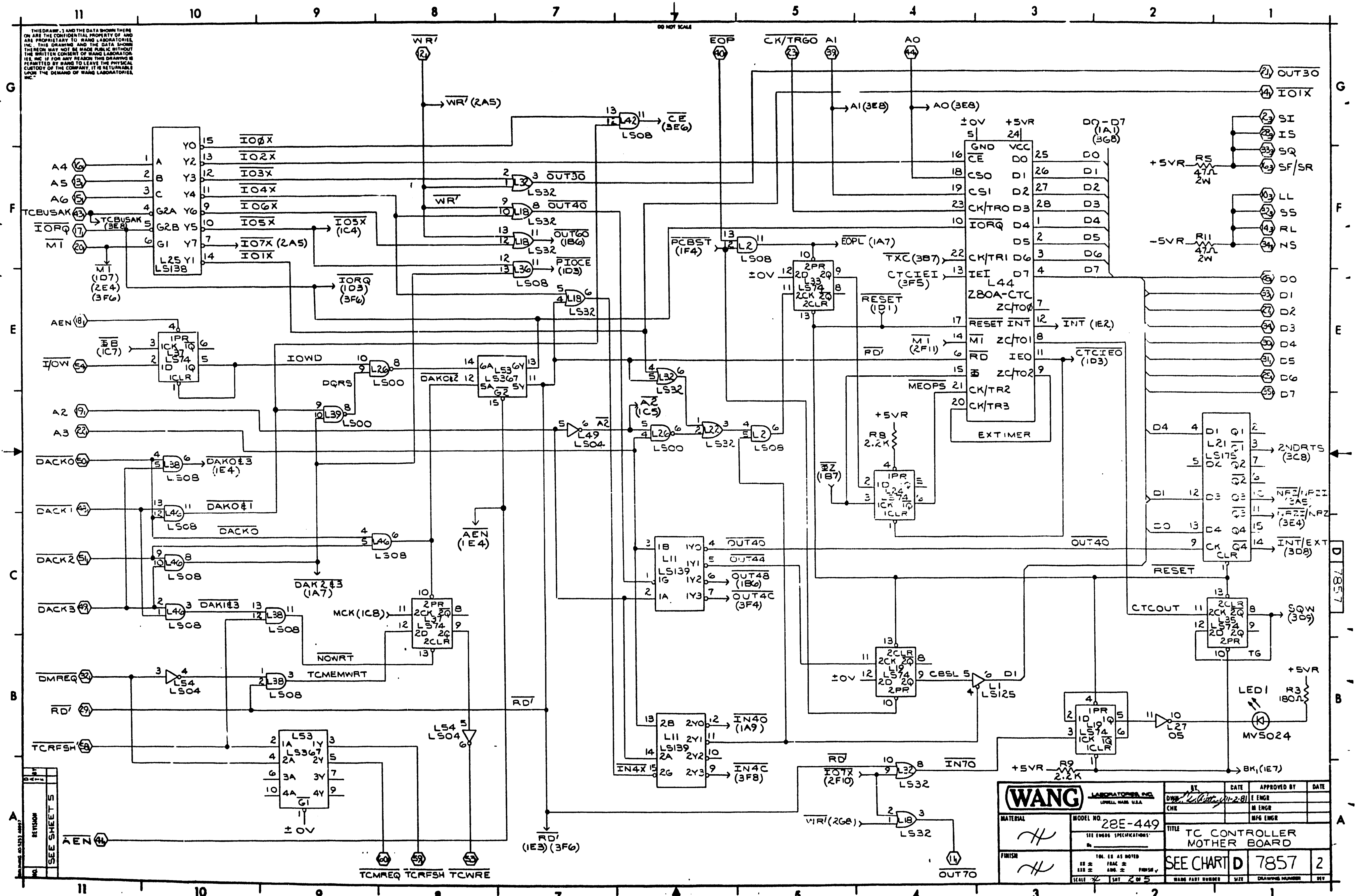
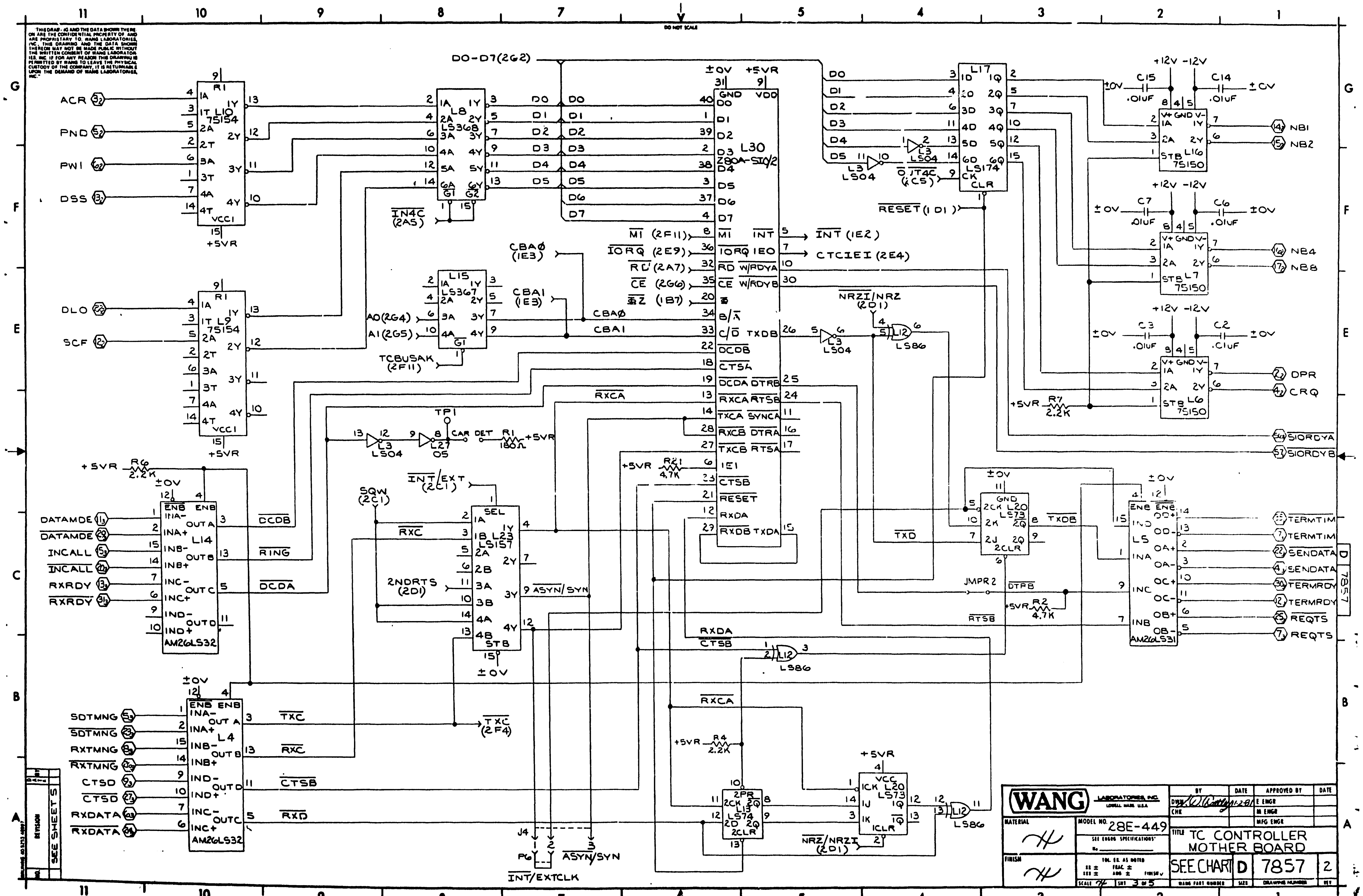
DO NOT SCALE
AB8 AB7 AB6 AB5 AB4 AB3 AB2 AB1
ABS CPB OBS CBS
OB1 OB2 OB3 OB4 OB5 OB6 OB7 OB8
SW2
SW1
L51 Z8CA-PIO
L50 LS240
L31 LS240
L40 9602
Y1 12.24MHZ
Q1 SPS6551
PRISEL
BSTB
PCBS
PCBST
ASTB
ARDY
BRDY
SECSEL
RESET
PRESET
IB1 IB3 IB5 IB7 IB2 IB4 IB6 IB8
INT
DRQ3
IB9
IBS
RB1
D0-D7 (2G2)
MCK
BB
BZ
IN40 (2B5)
OUT60 (2F7)
OUT48 (2C5)
DAK2 $3 (2C9)
DAK0 $3 (2D10)
EOPL (2F5)
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
MATERIAL
FINISH
MODEL NO. 28E-449
DWN 11-2-81
E ENGR
M ENGR
MFG ENGR
TITLE T.C. CONTROLLER MOTHER BOARD
SEE CHART D 7857 2
SHT 1 OF 5
REVISION
SEE SHEET 5


WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
TITLE TC CONTROLLER MOTHER BOARD
MODEL NO. 28E-449
SEE CHART D 7857 2
SHT 2 OF 5
SEE SHEET 5
D 7857
DO NOT SCALE
L44 Z80A-CTC
EXTIMER
L25 LS138
L21 LS175
LED1 MV5024
WR'
EOP
CK/TRGO
A1
A0
OUT30
IO1X
SI
IS
SQ
SF/SR
LL
SS
RL
NS
AEN
I/OW
A2
A3
A4
A5
A6
TCBUSAK
IORQ
M1
DACK0
DACK1
DACK2
DACK3
DMREQ
RD'
TCRFSH
TCMREQ
TCWRE
OUT70
IN70
IN40
IN4C
OUT40
OUT44
OUT48
OUT4C
SQW (3D9)
2NDRTS (3C8)
INT/EXT (3D8)
RESET
CTCOUT
MEOPS
PCBST
EOPL (1A7)
TXC (3B7)
INT (1E2)
CTCIEO (1D3)
BK1 (1E7)
+5VR
-5VR



WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
TITLE TC CONTROLLER MOTHER BOARD
MODEL NO. 28E-449
SEE CHART D 7857 2
SHT 3 OF 5
REVISION SEE SHEET 5
DO NOT SCALE
11 10 9 8 7 6 5 4 3 2 1
G F E C B A
D0-D7(2G2)
ACR
PND
PW1
DSS
R1 L10 75154
+5VR
L8 LS368
IN4C (2A5)
DLO
SCF
R1 L9 75154
L15 LS367
A0(2G4)
A1(2G5)
TCBUSAK (2F11)
CBAØ (1E3)
CBA1 (1E3)
L30 Z80A-SIO/2
M1 (2F11)
IORQ (2E9)
RD (2A7)
CE (2G6)
Φ Z (1B7)
INT (1E2)
CTCIEI (2E4)
NRZI/NRZ (2D1)
L12 LS86
L3 LS04
L17 LS174
RESET (1D1)
OJT4C (1C5)
+12V -12V
C15 .01UF
C14 .01UF
L16 75150
NB1
NB2
C7 .01UF
C6 .01UF
L7 75150
NB4
NB8
C3 .01UF
C2 .01UF
L6 75150
DPR
CRQ
R7 2.2K
SIORDYA
SIORDYB
TP1
L27 OS
CAR DET
R1 180Ω
R6 2.2K
L14 AM26LS32
DATAMDE
INCALL
RXRDY
DCDB
RING
DCDA
RXCA
R21 4.7K
SQW (2C1)
INT/EXT (2C1)
L23 LS157
RXC
2NDRTS (2D1)
ASYN/SYN
L20 LS73
TXDB
TXD
JMPR 2
DTRB
R2 4.7K
RTSB
AM26LS31
TERMTIM
SENDATA
TERMRDY
REQTS
RXDA
CTSB
L4 AM26LS32
SDTMNG
RXTMNG
CTSD
RXDATA
TXC
TXC (2F4)
RXD
R4 2.2K
L13 LS74
L20 LS73
NRZ/NRZI (2D1)
J4
P6
INT/EXTCLK

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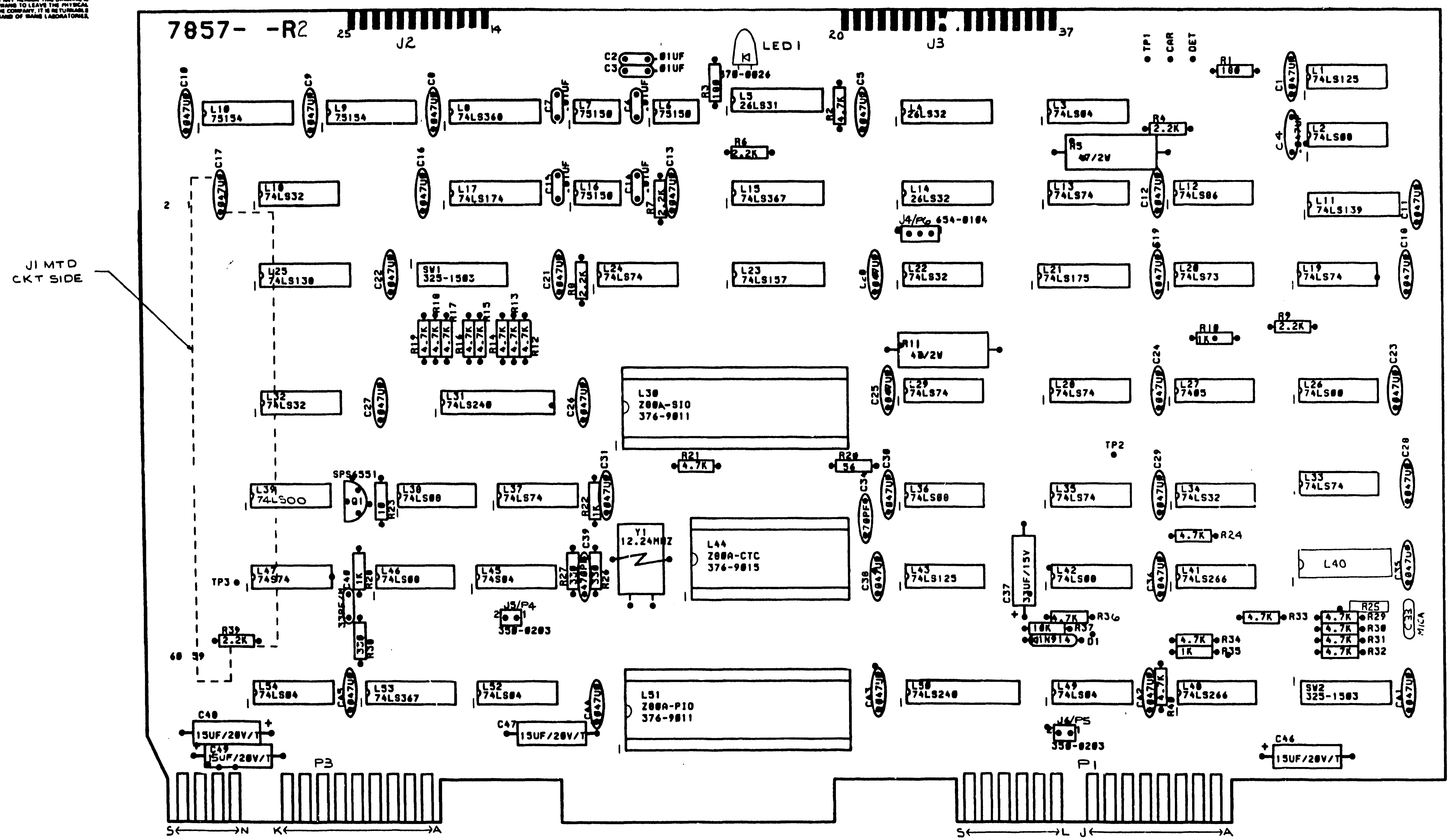
DO NOT SCALE



7857- -R2
J2
J3
LED1
TP1
CAR
DET
J1 MTD CKT SIDE
L1 74LS125
L2 74LS00
L3 74LS04
L4 26LS32
L5 26LS31
L6 75150
L7 75150
L8 74LS360
L9 75154
L10 75154
L11 74LS139
L12 74LS86
L13 74LS74
L14 26LS32
L15 74LS367
L16 75150
L17 74LS174
L18 74LS32
L19 74LS74
L20 74LS73
L21 74LS175
L22 74LS32
L23 74LS157
L24 74LS74
L25 74LS138
SW1 325-1503
L26 74LS00
L27 7405
L28 74LS74
L29 74LS74
L30 Z80A-SIO 376-9011
L31 74LS240
L32 74LS32
L33 74LS74
L34 74LS32
L35 74LS74
L36 74LS00
L37 74LS74
L38 74LS00
L39 74LS00
L40
L41 74LS266
L42 74LS00
L43 74LS125
L44 Z80A-CTC 376-9015
L45 74S04
L46 74LS00
L47 74S74
L48 74LS266
L49 74LS04
L50 74LS240
L51 Z80A-PIO 376-9011
L52 74LS04
L53 74LS367
L54 74LS04
SW2 325-1503
Y1 12.24MHZ
SPS6551 Q1
J4/P6 654-0104
J5/P4 350-0203
J6/P5 350-0203
C40 15UF/20V/T
C49 15UF/20V/T
C47 15UF/20V/T
C46 15UF/20V/T
C37 33UF/15V
C33 MICA
D1 1N914
TP2
TP3
P3
P1
S N K A
S L J A

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	DWN	11-2-81	E ENGR	
	CHK		M ENGR	
MATERIAL	MODEL NO. 28E-449		MFG ENGR	
	SEE ENGRG SPECIFICATIONS	TITLE TC CONTROLLER MOTHER BOARD		
FINISH	TOL EX AS NOTED	SEE CHART	D	7857 2
	SCALE	SHT 4 OF 5	WANG PART NUMBER / SIZE / DRAWING NUMBER / REV	

REVISION: SEE SHEET 5

D 7857

DO NOT SCALE

COMPONENT	TYPE	W.L. PART NO.
R1,3	180Ω 1/4W 10%	330-2018
R2,12-19,21,24, 29-34,36,40	4.7K 1/4W 10%	330-3047
R4,6-9,39	2.2K 1/4W 10%	330-3022
R5,11	47Ω 2W 10%	337-1047
R10,22,28,35	1K 1/4W 10%	330-3010
R20	56Ω 1/4W 10%	330-1056
R23	10Ω 1/4W 10%	330-1010
R25,37	10K 1/4W 10%	330-4010
R26,27,38	330Ω 1/4W 10%	330-2033
C1,4,5,8-13, 16-31,35,36,38, 41-45	.047UF 50V	3[illegible]-1966
C2,3,6,7,14,15	.01UF 25V	300-1903
C33	.001UF 100V(MICA)	300-5006
C39	470PF 500V	300-1470
C37	33UF 10V (T)	300-4024
C40	33PF 500V (MICA)	300-5016
C46-49	15 UF 20V(T)	300-4022
C34	270PF 500V	300-1270
LED1	MV5024	370-0026
D1	IN914A	380-1012
Y1	12.24 MHZ	321-0019
Q1	SPS-6551	375-1050
J1	60 PIN CONN	350-0051
J2	25 PIN CONN	350-1051
J3	37 PIN CONN	350-1066
J4	3 POS HEADER	654-0104
J5,6	2 POS HEADER	350-0203
P4,5,6	2 POS SHUNT	350-4506
SW1,2	SPST 8 POS	325-1503

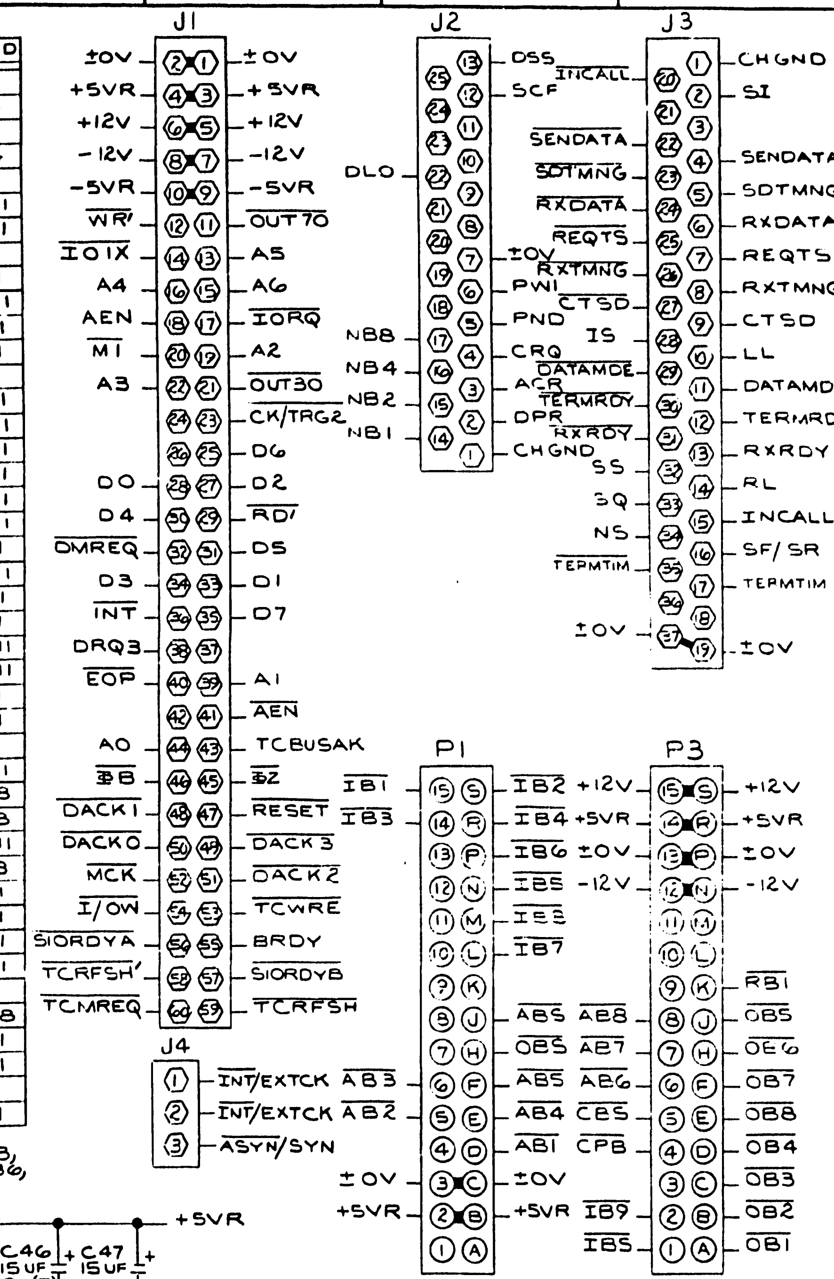
I.C. LOCATION	TYPE	W.L. PART NO.
L1,43	74LS125	376-0486
L2,36,38,42,46	74LS08	376-0153
L3,49,52,54	74LS04	376-0180
L4,14	AM26LS32	376-0471
L5	AM26LS31	376-0470
L6,7,16	75150	376-0076
L8	74LS368	376-0193
L9,10	75154	376-0077
L11	74LS139	376-0226
L12	74LS86	376-0231
L13,19,24,28, 29,33,35,37	74LS74	376-0155
L15,53	74LS367	376-0192
L17	74LS174	376-0159
L18,22,32,34	74LS32	376-0211
L20	74LS73	376-0304
L21	74LS175	376-0160
L23	74LS157	376-0216
L25	74LS138	376-0294
L26,39	74LS00	376-0207
L27	7405	376-0029
L30	Z80A-SIO/2	SEE CHART
L31,50	74LS240	376-0297
L40	9602	376-0104
L41,48	74LS266	376-0148
L44	Z80A-CTC	SEE CHART
L47	74S74	376-0202
L51	Z80A-PIO	SEE CHART
L45	74S04	376-0197
L30,51	40 PIN SOCKET	376-9011
L44	28 PIN SOCKET	376-9015

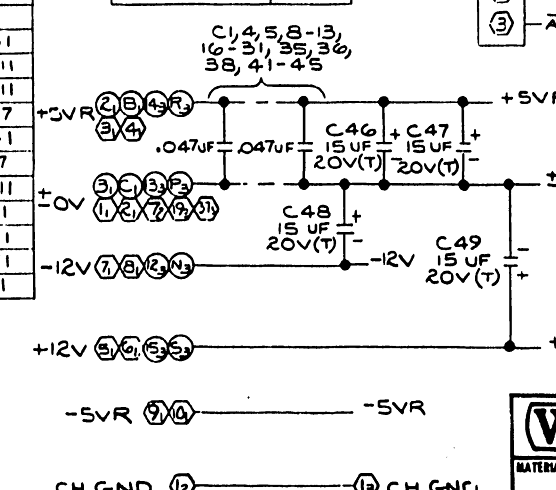
TYPE	I.C. LOCATION	SPARE
74LS00	L26	1
74LS04	L3	1
	L54	1
7405	L27	3
74LS08	L2	1
	L36	1
	L38	1
74LS74	L24	1
	L33	1
74LS00	L39	3
74LS86	L12	1
74LS125	L1	3
9602	L40	1

210 = 209 + 377 OR 378				
210	209	L30	L44	L51
7857-A	7857	377-0393	377-0371	377-0373

MNEMONICS	COOR'D
AB1-AB8	1G9
ABS	1G7
ACR	3G11
AEN	2E11
AEN	2A11
ASYN/SYN	3A7
A0	2G4
A1	2G5
A2,A3	2D11
A4-A6	2F11
BRDY	1D1
CBS	1G5
CK/TRG0	2G5
CPB	1G6
CRQ	3E1
CTSD	3A11
CTSD	3A11
DACK0	2D11
DACK1	2D11
DACK2	2C11
DACK3	2C11
DATAMDE	3C11
DATAMDE	3C11
DLO	3E11
DMREQ	2B11
DPR	3E1
DRQ3	1C1
DSS	3F11
D0-D7	2E1
EOP	2G6
EB	1A7
IB1-IB8	1F1
IB9	1B1
IBS	1B1
INCALL	3C11
INCALL	3C11
INT	1E1
INT/EXTCK	3A7
IOIX	2G1
I/OW	2E11
IORQ	2F11
EZ	1A7
IS	2G1
MCK	1A7
M1	2F11
LL	2F1
NB1,NB2	3G1
NB4,NB8	3F1
NS	2F1

MNEMONICS	COOR'D
OBS	1G5
OB1-O8	1G4
OUT 30	2G1
OUT 70	2A4
PND	2G11
PW1	3F11
RB1	1B1
RD	2B11
REQTS	3C1
REQTS	3C1
RESET	1C1
RX DATA	3A11
RX DATA	3A11
RXRDY	3C11
RXRDY	3C11
RXTMNG	3B11
RXTMNG	3A11
RL	2F1
SCF	3E11
SENDATA	3C1
SENDATA	3C1
SDTMNG	3B11
SDTMNG	3B11
SIORDYA	3D1
SIORDYB	3D1
TCBUSAK	2F11
TCMREQ	2A8
TCRFSH	2A8
TCRFSH'	2B11
TCWRE	2A8
TERMRDY	3C1
TERMRDY	3C1
TERMTIM	3C1
TERMTIM	3C1
WR	2G8
SF/SR	2F1
SI	2G1
SQ	2F1
SS	2F1





E-REV
0

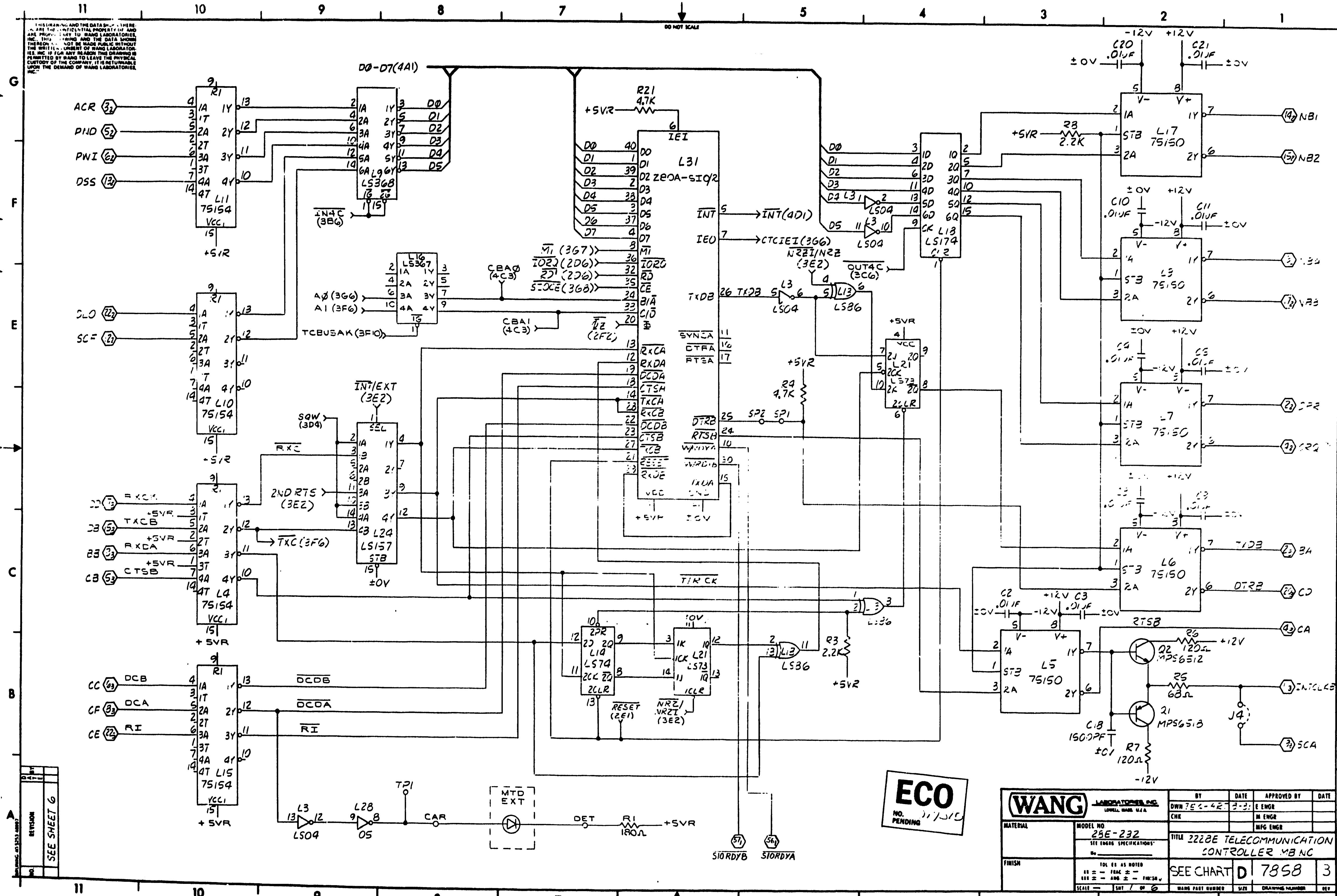
WANG LABORATORIES INC. LOWELL, MASS. U.S.A.

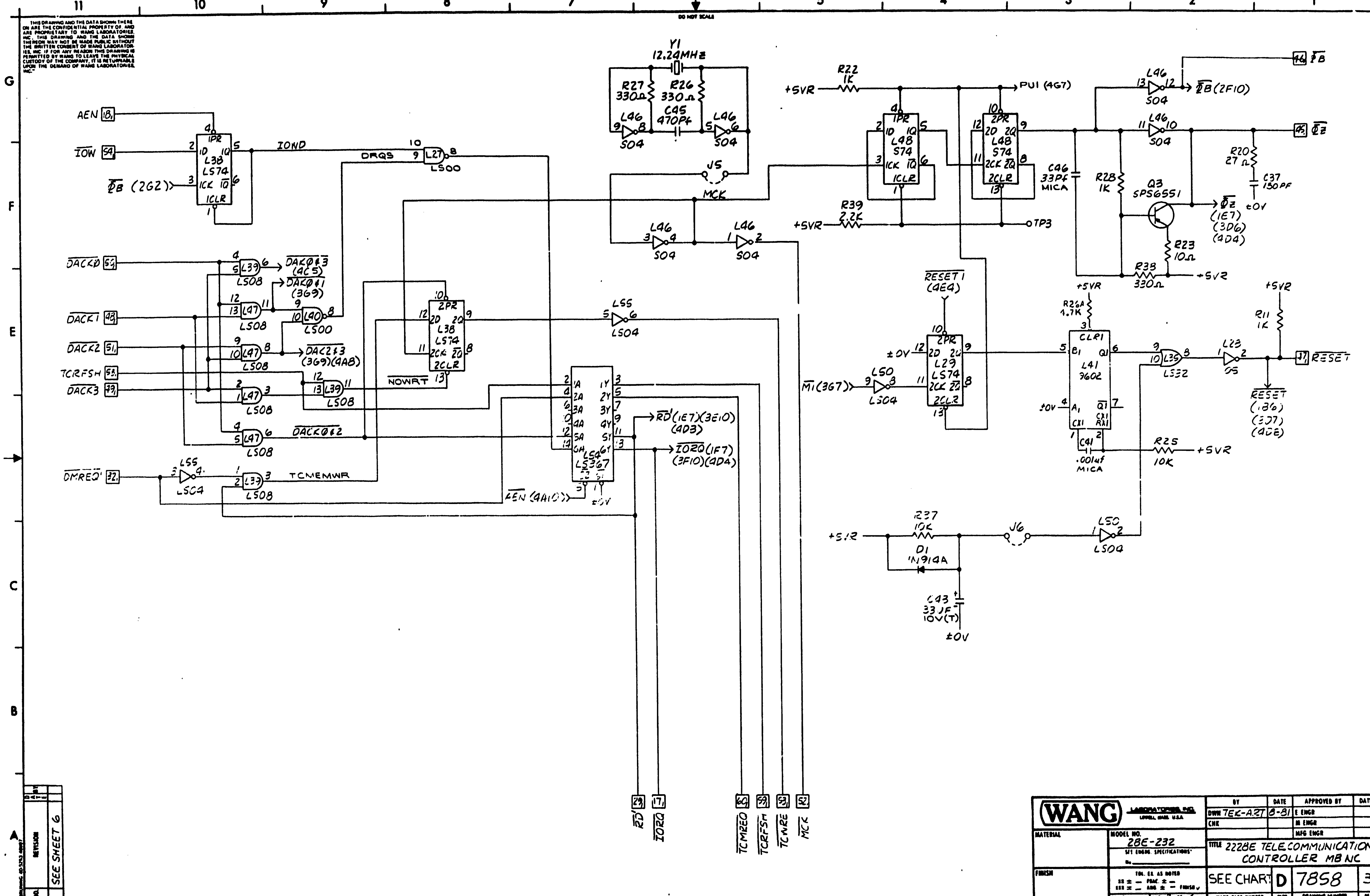
MODEL NO. 28E-449

TITLE TC CONTROLLER MOTHER BOARD

SEE CHART | D | 7857 | 2

SHT 5 OF 5


DO NOT SCALE
D0-D7(4A1)
ACR
PND
PWI
DSS
L11
75154
L9
LS368
L31
Z80A-SIO/2
INT
IEO
TXDB
INT(4D1)
CTCIEI(3G6)
L13
LS174
L17
75150
L5
75150
L6
75150
L7
75150
L8
75150
L16
LS367
L10
75154
L24
LS157
L4
75154
L15
75154
L14
LS74
L21
LS73
L3
LS04
L12
LS86
L28
05
SEL
TP1
CAR
MTD EXT
DET
R1
180Ω
+5VR
R21
4.7K
R8
2.2K
R4
4.7K
R3
2.2K
R5
68Ω
R6
120Ω
R7
120Ω
Q1
MPS6513
Q2
MPS6512
C18
1500PF
TXC(3F6)
2ND RTS (3E2)
RESET (2E1)
NRZI/NRZ (3E2)
OUT4C (3C6)
SIORDYB
SIORDYA
DCDB
DCDA
RI
T/R CK
J4
+12V
-12V
±0V
ECO
NO. PENDING
SEE SHEET 6
REVISION
WANG LABORATORIES, INC.
MODEL NO 25E-232
TITLE 2228E TELECOMMUNICATION CONTROLLER MB NC
SEE CHART
D
7858
3
SHT 1 OF 6



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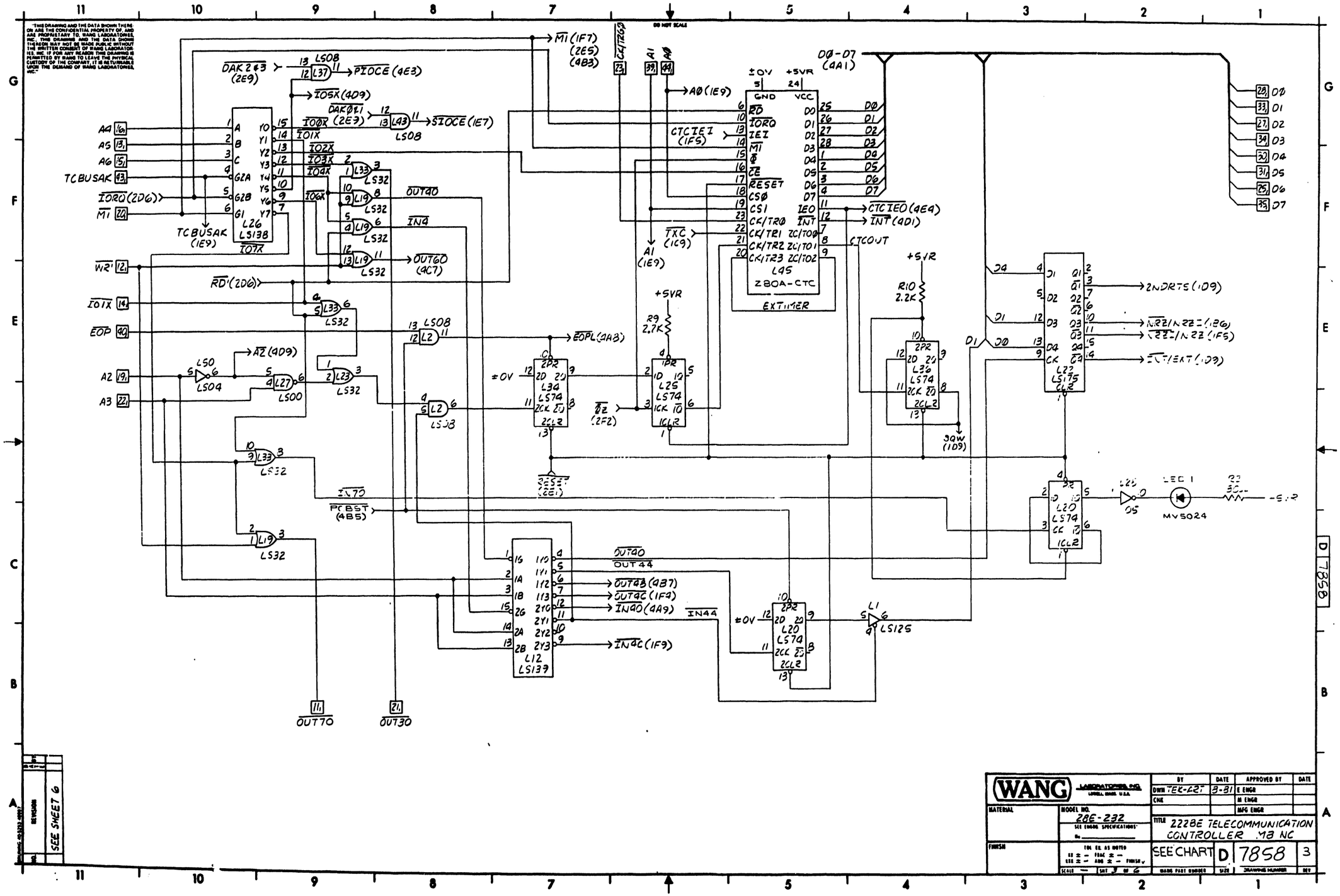
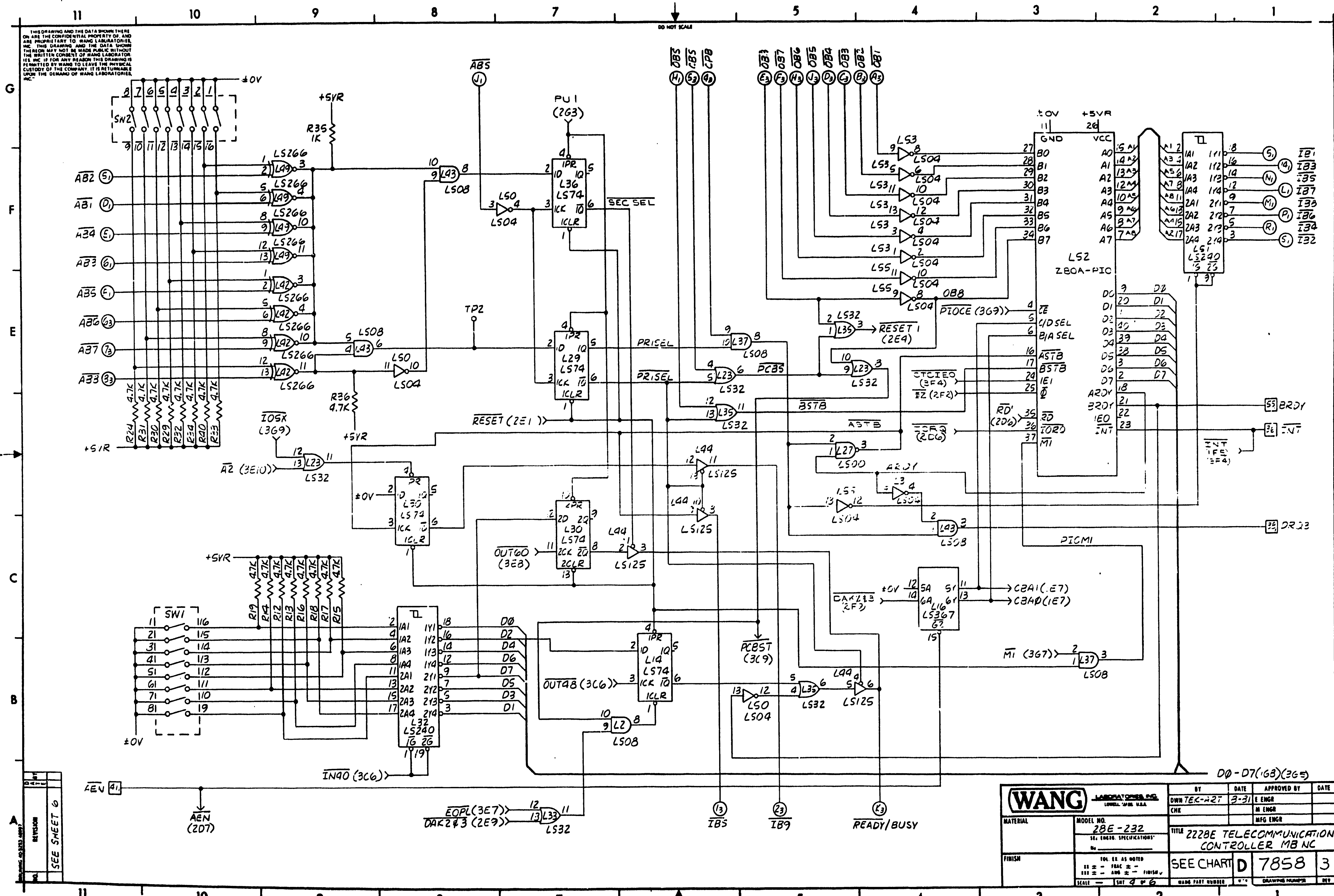
Y1 12.24MHz
R27 330Ω
R26 330Ω
C45 470PF
L46 S04
J5
MCK
AEN
IOW
ΦB (2G2)
L38 LS74
IOND
DRQS
L27 LS00
DACK0
DACK1
DACK2
DACK3
TCRFSH
DACK0#3 (4C5)
DACK0#1 (3G9)
DACK2#3 (3G9)(4A8)
DACK0#2
L39 LS08
L47 LS08
L40 LS00
NOWRT
L55 LS04
DMREQ'
TCMEMWR
AEN (4A10)
LS367
RD' (1E7)(3E10) (4D3)
IORQ (1F7) (3F10)(4D4)
RD'
IORQ
TCMREQ
TCRFSH
TCWRE
MCK
+5VR
R22 1K
PUI (4G7)
L48 S74
R39 2.2K
TP3
C46 33PF MICA
R28 1K
Q3 SPS6551
R20 27Ω
C37 150PF
R23 10Ω
R33 330Ω
ΦB (2F10)
Φ2
Φ2 (1E7) (3D6) (4D4)
RESET1 (4E4)
M1 (3G7)
L50 LS04
L29 LS74
R26A 1.7K
L41 9602
C41 .001uf MICA
R25 10K
L35 LS32
L23 05
R11 1K
RESET
RESET (1B6) (3D7) (4DE)
R37 10K
D1 1N914A
J6
C43 33UF 10V(T)
±0V
REVISION
SEE SHEET 6
WANG LABORATORIES INC. LOWELL MASS. U.S.A.
DWN TEK-ART 8-81
MODEL NO. 28E-232
TITLE 2228E TELECOMMUNICATION CONTROLLER MB NC
SEE CHART D 7858 3
SHT 2 OF 6
D 7858



WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN TEK-LZT	3-81	E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. 2BE-232 SEE ENGRG SPECIFICATIONS No.			MFG ENGR	
		TITLE 2228E TELECOMMUNICATION CONTROLLER .MB NC			
FINISH	TOL EX AS NOTED XX ± — FRAC ± — XXX ± — ANG ± — FINISH √	SEE CHART	D	7858	3
	SCALE — SHT 3 OF 6	USED ON NEXT ASSY	SIZE	DRAWING NUMBER	REV



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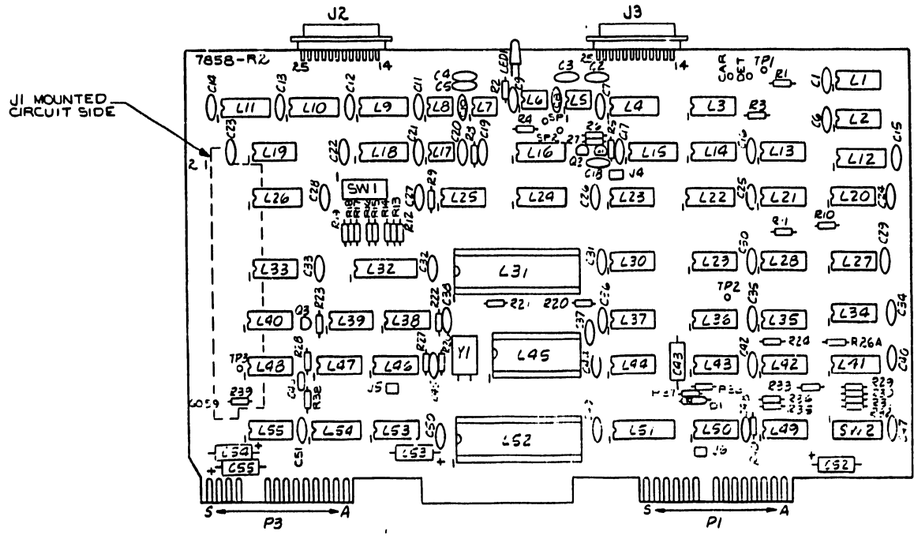
DO NOT SCALE
SW2
SW1
+5VR
±0V
R35 1K
R36 4.7K
PU1 (2G3)
TP2
SEC SEL
PRISEL
RESET (2E1)
IOSX (3G9)
A2 (3E10)
OUTGO (3E8)
OUT48 (3C6)
IN40 (3C6)
AEN (2D7)
EOPL (3E7)
DAK2Ø3 (2E9)
PIOCE (3G9)
RESET1 (2E4)
PCBS
BSTB
ASTB
PCBST (3C9)
PICMI
CBA1(1E7)
CBAD(1E7)
M1 (3G7)
BRDY
INT
DRQ3
L52 Z80A-PIO
L51 LS240
L32 LS240
L16 LS367
L36 LS74
L29 LS74
L30 LS74
L14 LS74
D0-D7(1G8)(3G5)
IB5
IB9
READY/BUSY
SEE SHEET 6
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
DWN TEC-ART 3-31
MODEL NO. 28E-232
TITLE 2228E TELECOMMUNICATION CONTROLLER MB NC
SEE CHART D 7858 3
SHT 4 OF 6

DO NOT SCALE



WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN TEK-ART	8-81	E ENGR	
		CHK		M ENGR	
				MFG ENGR	
MATERIAL	MODEL NO. 228E-232 SEE ENGR'G SPECIFICATIONS No.	TITLE 2228E TELECOMMUNICATION CONTROLLER M3 NC			
FINISH	TOL. EX. AS NOTED .XX ± — FRAC. ± — .XXX ± — ANG. ± — FINISH √ SCALE — SHT 3 OF 6	SEE CHART	D	7858	3
		WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

NO.	REVISION	BY	DATE
	SEE SHEET 6		

D 7858

DO NOT SCALE

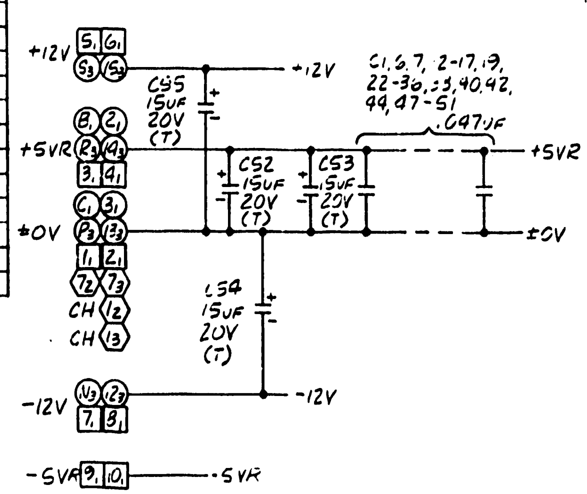
I.C. LOCATION	TYPE	W.L. PART NO.
L1,44	74LS125	376-0486
L2,37,39,43,47	74LS08	376-0153
L3,50,53,55	74LS04	376-0180
L4,10,11,15	75154	376-0077
L5-8,17	75150	376-0076
L9	74LS368	376-0193
L12	74LS139	376-0226
L13	74LS86	376-0231
L14,20,25,29,30, 34,36,38	74LS74	376-0155
L16,54	74LS367	376-0192
L18	74LS174	376-0159
L19,23,33,35	74LS32	376-0211
L21	74LS73	376-0304
L22	74LS175	376-0160
L24	74LS157	376-0216
L26	74LS138	376-0294
L27,40	74LS00	376-0207
L23	7405	376-0029
L31	Z80A-SIO	SEE CHART
L32,51	74LS240	376-0297
L41	9602	376-0104
L42,49	74LS266	376-0198
L45	Z80A-CTC	SEE CHART
L46	74S04	376-0197
L48	74S74	376-0202
L52	Z8OA-PIO	SEE CHART
L31,52	SOCKET, 40 PIN	376-9011
L45	SOCKET, 28 PIN	376-9015

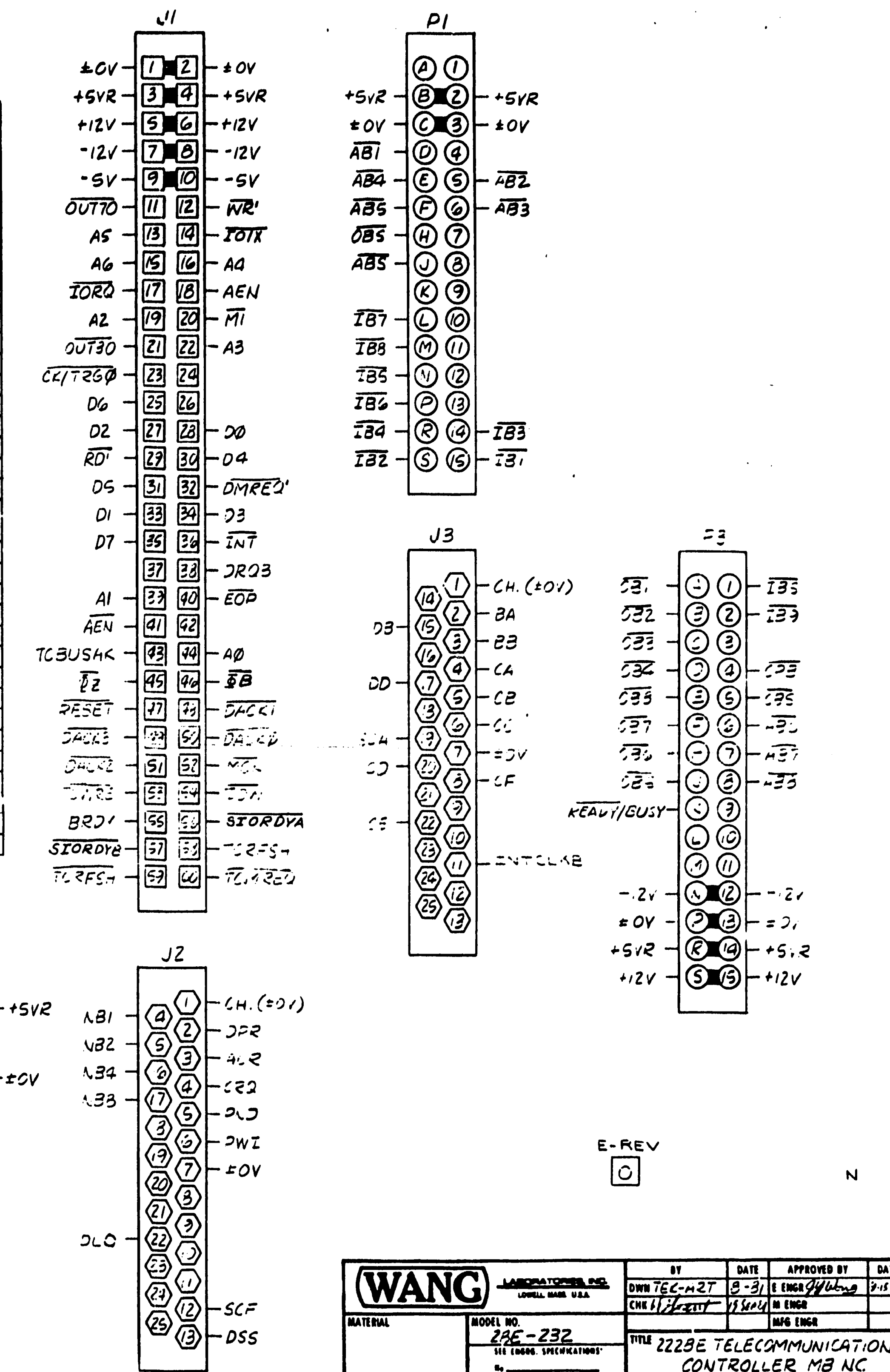
TYPE	I.C. LOCATION	SPARES
74LS00	L27 L40	1 3
74LS04	L3 L55	1 1
7405	L28	3
74LS08	L2 L37 L39	1 1 1
74LS74	L25 L34	1 1
74LS86	L13	1
74LS125	L1	3
9602	L41	1

210 = 209 + 377 OR 378				
210	209	L31	L45	L52
7858-A	7858	377-0393	377-0371	377-0373

COMPONENT	TYPE	W.L. PART NO.
C1,6,7,12-17,19, 22-36,38,40,42, 44,47-51	.047UF 50V	300-1966
C2-5,8-11,20,21,	.01UF 25V	300-1903
C18	1500PF 200V	300-1964
C37	150PF 100V	300-1150
C41	.001UF 5% MICA	300-5006
C43	33UF 10V (T)	300-4024
C45	470PF 500V	300-1470
C46	33PF 500V MICA	300-5016
C52-55	15UF 20V (T)	300-4022
R1,2	180Ω 1/4W 10%	330-2018
R3,8,9,10,39	2.2K 1/4W 10%	330-3022
R4,12-19,21,24, 29-34,36,40,26A	4.7K 1/4W 10%	330-3047
R5	68Ω 1/4W 10%	330-1068
R6,7	120Ω 1/4W 10%	330-2012
R11 22,28,35	1K 1/4W 10%	330-3010
R20	27Ω 1/4W 10%	330-1027
R23	10Ω 1/4W 10%	330-1010
R26,27 38	330Ω 1/4W 10%	330-2033
R37,25	10K 1/4W 10%	330-4010
Q1	MPS6518	375-1014
Q2	MPS6512	375-1012
Q3	MPS6551	375-1050
Y1	12.24 MHZ	321-0019
SW1,2	SPST, 8 PCS	325-1503
D1	IN914A	380-1012
LED 1	MV5024, RED	370-0026
J1	CONN., 90° 60 PIN	350-0051
J2,3	CONN., 25 PIN	350-1051
J4,5,6	SHUNT	350-4506
J4,5,6	CONN 2 PIN	350-0203

MNEMONIC	COORD	MNEMONIC	COORD
A0	3G6	DSS	1F11
A1	3G6	EOP	3E11
A2	3E11	IB1 - IB8	4F1
A3	3D11	IB9	4A5
A4	3G11	IBS	4A4
A5	3F11	INT	4D1
A6	3F11	INTCLKB	1B1
AB1 - AB8	4F11	IORQ	2A6
ABS	4G9	IOW	2F11
ACR	1G11	MCK	2A5
AEN	2G11	M1	3F11
AEN	4A11	NB1	1G1
BA	1C1	NB2	1F1
BB	1C11	NB4	1F1
BRDY	4D1	NB8	1E1
CA	1C1	OB1 - OB8	4C5
CB	1C11	OBS	4G6
CBS	4G6	OUT30	3B8
CC	1B11	OUT70	3B9
CD	1C1	ΦZ	2G1
CE	1B11	PND	1G11
CF	1B11	PWI	1F11
		READY/BUSY	4A4
CK/TRGΦ	3G6	RD'	2A6
CPB	4G6	RESET	2E1
CRQ	1D1	SCA	1B1
D0-D7	3G1	SCF	1E11
DACK0-DACK3	2E11	TCBUSAK	3F11
DB	1C11	TCRFSH	2E11
DD	1D11	TCRFSH	2A5
DLO	1E11	TCMREQ	2A6
DMREQ	2D11	TCNRE	2A5
DPR	1D1	WR	3E11
DRQ3	4C1	SIORDYA	1A5
ΦB	2G1	SIORDYB	1A5
IOIX	3E11		





E-REV
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REV	REVISION	BY	DATE
0	ORIGINATED PER DWR E1254 APP'D	TEC-H2T	8-31
1	REVISED PER ECO #29837 APP'D	PGD	10-30-81
2	REVISED PER ECO#21574 APP'D: DJC	SSB	1-4-82
3	REVISED PER ECO#21748 APP'D: DJC	SSB	1-4-82

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

BY		DATE	APPROVED BY	DATE
DWN	TEC-H2T	8-31	E ENGR	9-15-81
CHK		15 Sep 81	M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO. 2BE-232

SEE ENGRG. SPECIFICATIONS

FINISH

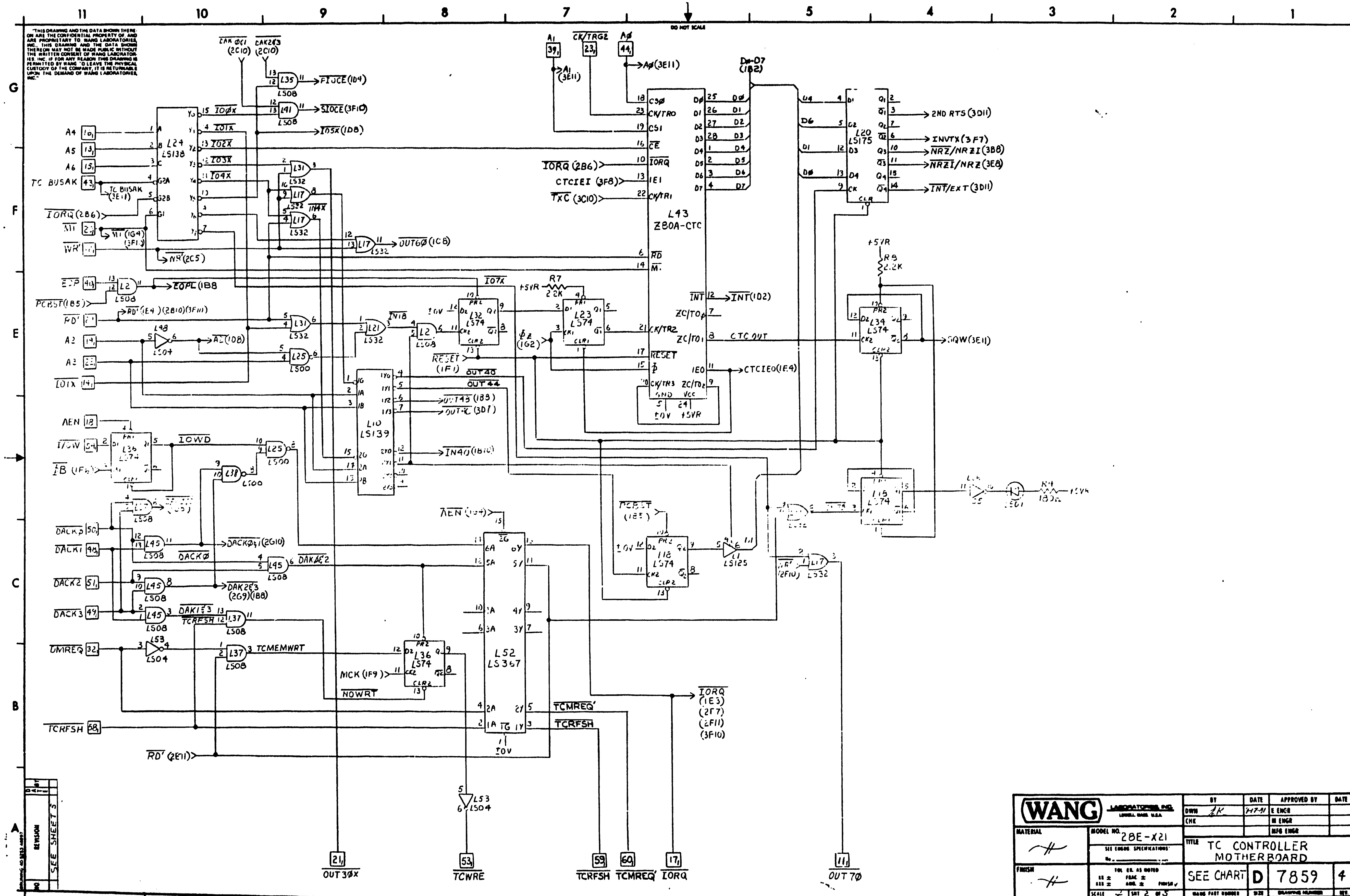
TOL. EX. AS NOTED

SCALE — SHT 6 of 6

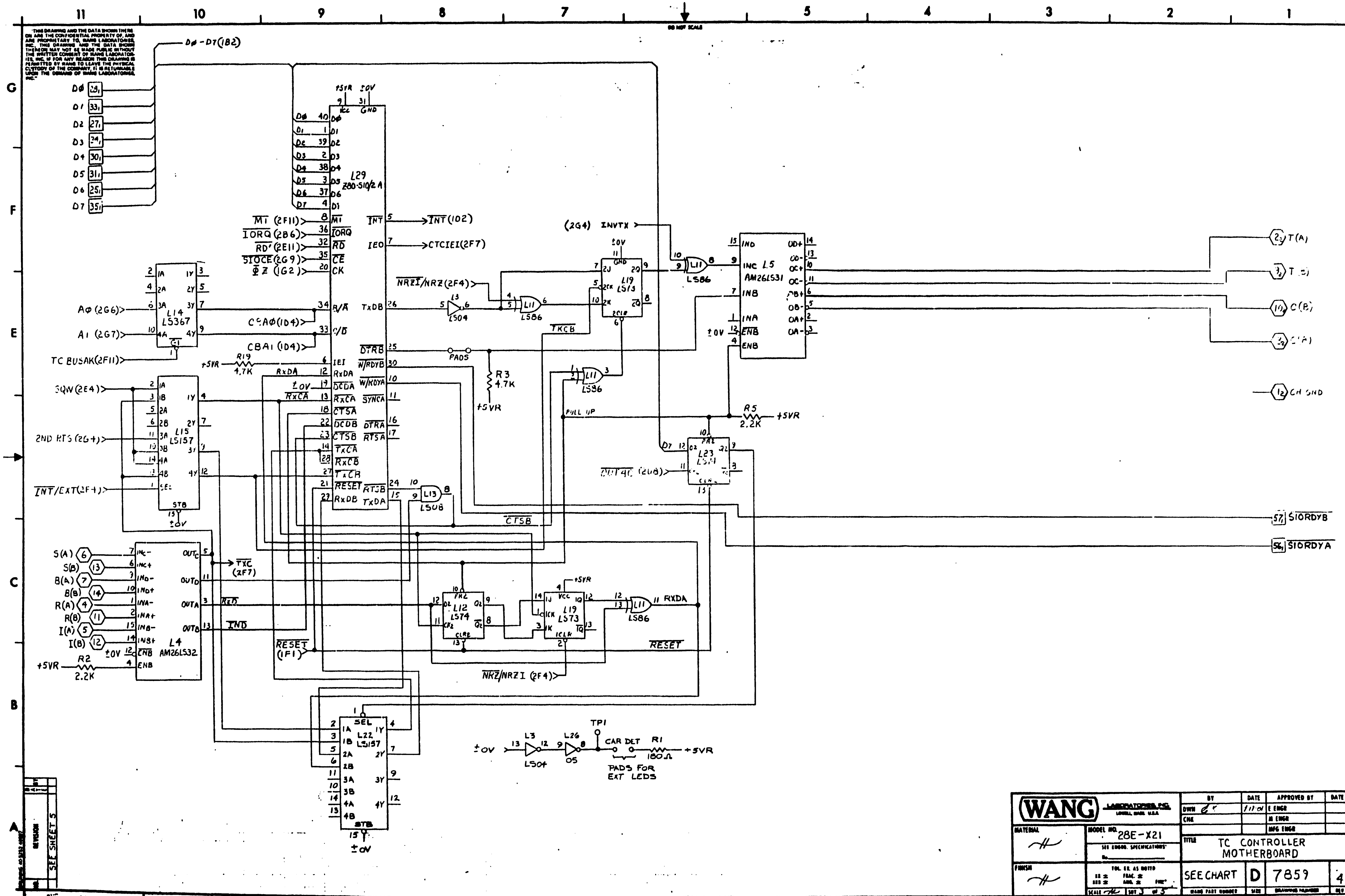
TITLE 2228E TELECOMMUNICATION CONTROLLER MB NC

WANG PART NUMBER		DRAWING NUMBER	REV
SEE CHART	D	7858	3

D 7858

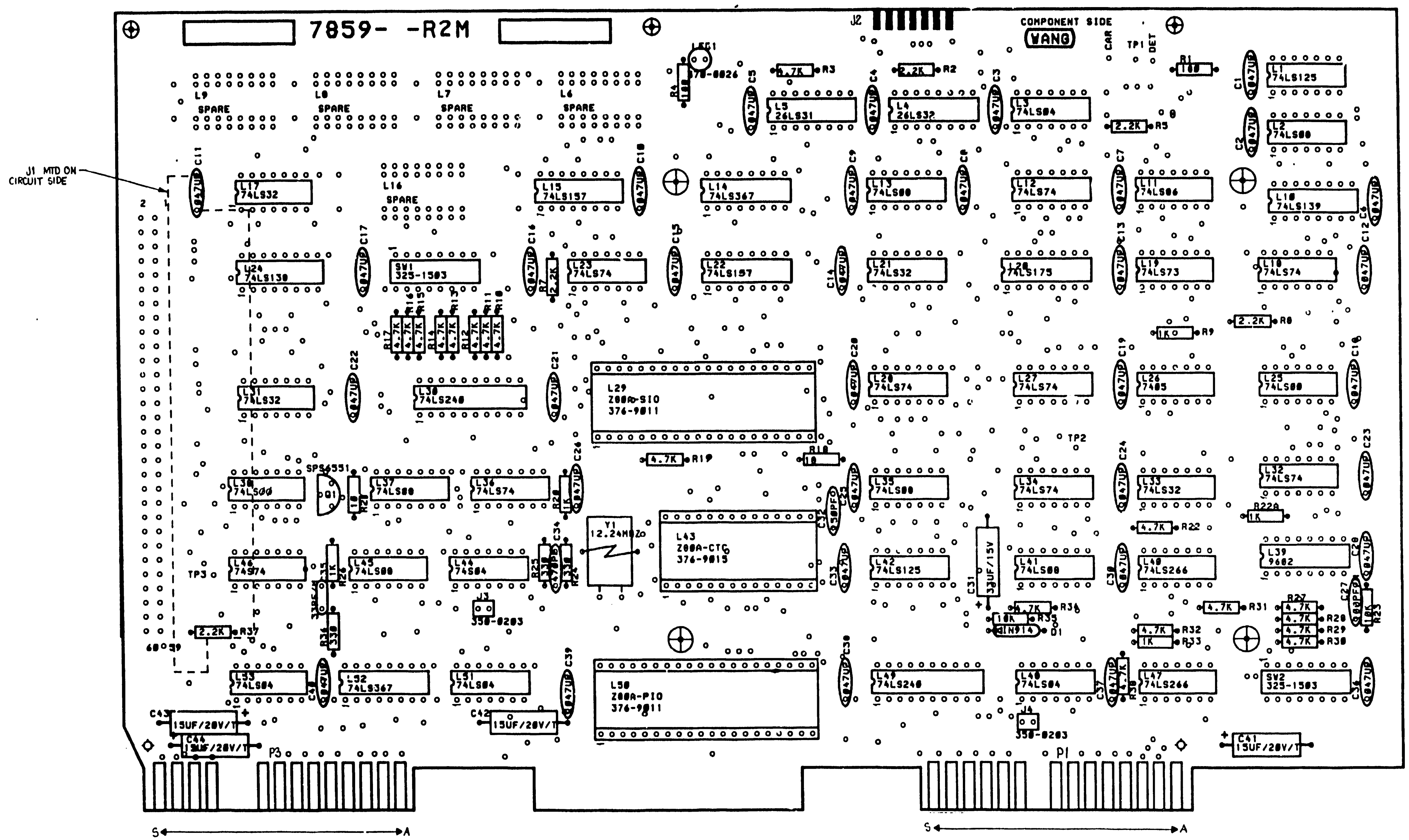


L24 LS138
L43 Z80A-CTC
L20 LS175
L10 LS139
L52 LS367
L32 LS74
L23 LS74
L34 LS74
L36 LS74
L18 LS74
L15 LS74
2ND RTS (3D11)
INVTX (3F7)
NRZ/NRZI (3B8)
NRZI/NRZ (3E8)
INT/EXT (3D11)
SQW (3E11)
CTC OUT
CTCIEO (1E4)
TCMEMWRT
NOWRT
TCMREQ'
TCRFSH
OUT 30X
TCWRE
OUT 70
WANG LABORATORIES INC.
MODEL NO. 28E-X21
TC CONTROLLER MOTHERBOARD
SEE CHART
D 7859
4
SEE SHEET 5



Dφ-D7(1B2)
L29 Z80-SIO/2 A
L14 LS367
L15 LS157
L4 AM26LS32
L5 AM26LS31
L19 LS73
L23 LS74
L12 LS74
L22 LS157
L11 LS86
L13 LS08
TC BUSAK(2F11)
INT(1D2)
CTCIEI(2F7)
NRZI/NRZ(2F4)
(2G4) INVTX
R3 4.7K
R5 2.2K
R19 4.7K
R2 2.2K
+5VR
PADS
PULL UP
SIORDYB
SIORDYA
CH GND
RESET (1F1)
TXC (2F7)
RxDA
TP1
CAR DET
R1 180Ω
PADS FOR EXT LEDS
DO NOT SCALE
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
MODEL NO. 28E-X21
TC CONTROLLER MOTHERBOARD
SEE CHART
D 7859
4
SEE SHEET 5

DO NOT SCALE


7859- -R2M
COMPONENT SIDE
WANG
J2
J1 MTD ON CIRCUIT SIDE
L9 SPARE
L8 SPARE
L7 SPARE
L6 SPARE
L16 SPARE
L1 74LS125
L2 74LS00
L3 74LS04
L4 26LS32
L5 26LS31
L10 74LS139
L11 74LS86
L12 74LS74
L13 74LS00
L14 74LS367
L15 74LS157
L17 74LS32
L18 74LS74
L19 74LS73
L20 74LS175
L21 74LS32
L22 74LS157
L23 74LS74
L24 74LS138
SW1 325-1503
L25 74LS00
L26 7485
L27 74LS74
L28 74LS74
L29 Z80A-SIO 376-9011
L30 74LS240
L31 74LS32
L32 74LS74
L33 74LS32
L34 74LS74
L35 74LS00
L36 74LS74
L37 74LS00
L38 74LS00
SPS4551
Y1 12.24MHZ
L39 9602
L40 74LS266
L41 74LS00
L42 74LS125
L43 Z80A-CTC 376-9015
L44 74S04
L45 74LS00
L46 74S74
TP1
TP2
TP3
L47 74LS266
L48 74LS04
L49 74LS240
L50 Z80A-PIO 376-9011
L51 74LS04
L52 74LS367
L53 74LS04
SW2 325-1503
J3 350-0203
J4 350-0203
1N914 D1
C41 15UF/20V/T
C42 15UF/20V/T
C43 15UF/20V/T
C44 15UF/20V/T
33UF/15V
P1
P3
S A
S A

WANG LABORATORIES, INC. LOWELL MASS. U.S.A.	BY	DATE	APPROVED BY / DATE
	DWN E.B. Blubinski	11/4/81	E ENGR
	CHK		M ENGR
			MFG ENGR
MATERIAL	MODEL NO 28E-X21		
	SEE ENGRG SPECIFICATIONS No	TITLE TC CONTROLLER MOTHER BOARD	
FINISH	TOL EX AS NOTED XX ± FRAC ± XXX ± ANG ± FINISH ✓	SEE CHART (WANG PART NUMBER)	D (SIZE) · 7859 (DRAWING NUMBER) · 4 (REV)
	SCALE · SHT 4 OF 5		

REVISION: SEE SHEET 5

N

D 7859

THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF AND ARE PROPRIETARY TO WANG LABORATORIES, INC. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC.

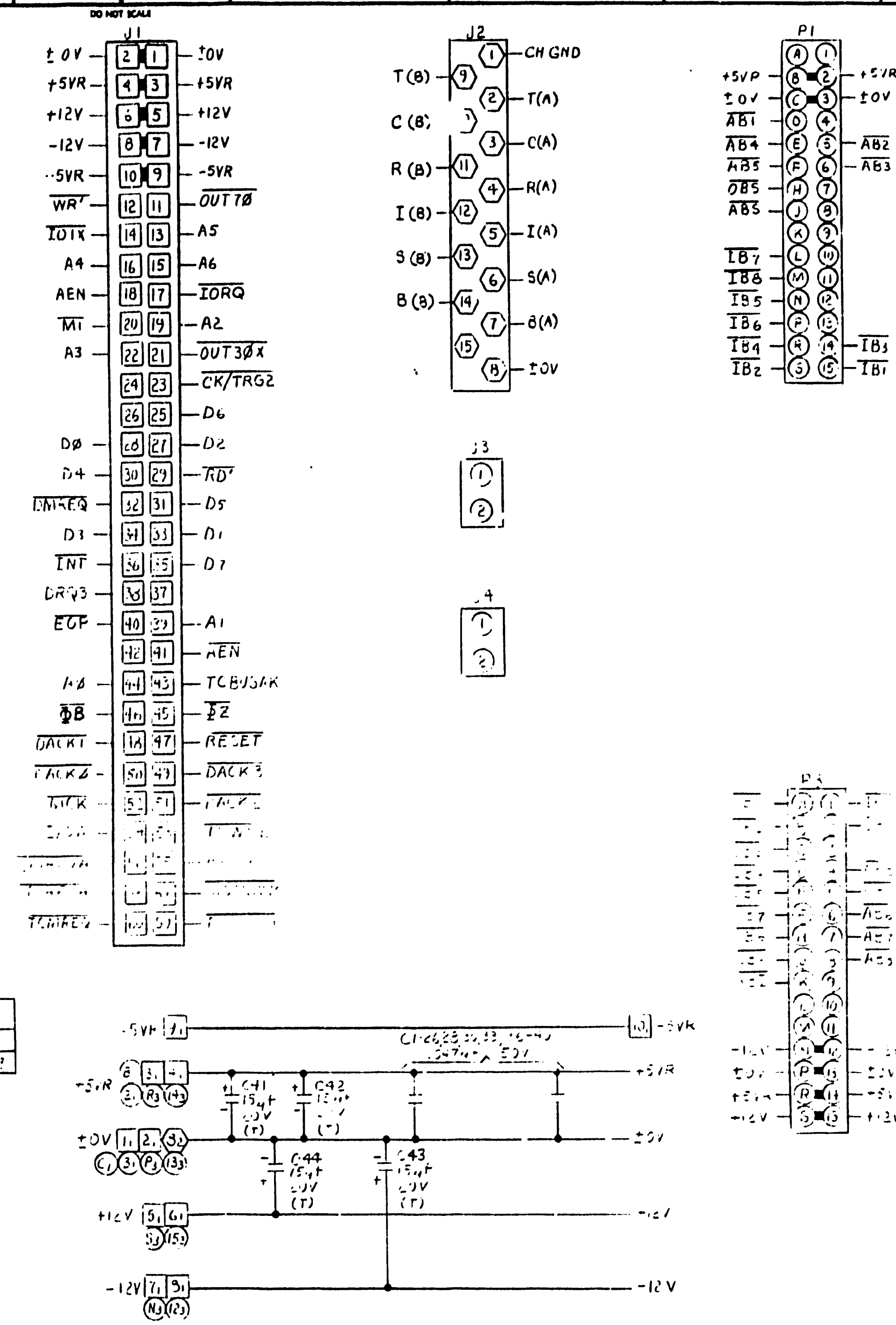
DO NOT SCALE

LOCATION	TYPE	WL PART NO.
L1,42	74LS125	376-0486
L25, 38	74LS00	376-0207
L3,48,51,53	74LS04	376-0180
L4	26LS32	376-0471
L5	26LS31	376-0470
L6,7,8,9,16	SPARE	
L10	74LS139	376-0226
L11	74LS86	376-0231
L12,18,23,27,28,32, 34,36	74LS74	376-0155
L2,13,35,37,41,45	74LS08	376-0153
L14,52	74LS367	376-0192
L15,22	74LS157	376-0216
L17,21,31,33	74LS32	376-0211
L19	74LS73	376-0304
L20	74LS175	376-0160
L24	74LS138	376-0294
L26	7405	376-0029
L29	Z80A-SIO/2	SEE CHART
L30,49	74LS240	376-0297
L39	9602	376-0104
L40,47	74LS266	376-0148
L43	Z80A-CTC	SEE CHART
L44	74S04	376-0197
L46	74S74	376-0202
L50	Z80A-PIO	SEE CHART
L29,50	40 PIN SKT	376-9011
L43	28 PIN SKT	376-9013

TYPE	LOCATION	SPARES
74LS00	L25	1
	L38	3
74LS08	L2	1
	L13	3
	L35	1
	L37	1
74LS04	L3	3
	L53	1
7405	L26	3
74LS74	L32	1
74LS125	L1	3
9602	L39	1

COMPONENT	TYPE	WL PART
R1,4	180Ω 1/4W 5%	330-2019
R2,5,7,8,37	2.2K 1/4W 5%	330-3023
R3, 10-17,19, 22,27-32,34,38	4.7K 1/4W 5%	330-3048
R9,20,26,33,22A	1K 1/4W 5%	330-3011
R18	18Ω 1/4W 5%	330-1019
R21	10Ω 1/4W 5%	330-1011
R23,35	10K 1/4W 5%	330-4011
R24,25,36	330Ω 1/4W 5%	330-2034
C1-26,28,30,33,36-40	.047µf 50V	300-1966
C27	100Cpf 100V MICA	300-5CC6
C29	100pf 500V MICA	300-5028
C31	33µf 10V TANT	300-4024
C32	150pf 500V 10%	300-1150
C34	470pf 500V	300-1470
C35	33pf 500V MICA	300-[illegible]
C41-44	15µf 20V TANT	300-4022
Y1	12.[illegible]MHZ XTAL	321-0019
SW1, SW2	8 POS DIL	325-1503
LED 1	LED RED	370-0075
Q1	SPS6551	375-1050
J1	[illegible] PIN CONN	350-0051
J2	16 PIN CONN	350-1081
[illegible]	2 PIN HEADER	350-[illegible]
P3, P4	[illegible]	350-[illegible]
D1	[illegible] DIODE	3[illegible]-[illegible]

210 = 209 + [illegible]				
210	209	L29	L43	L50
7859-A	7859	[illegible]	[illegible]	[illegible]



MNEMONIC	COORD
A0, A1	2G7
A2, A3	2E11
A4	2G11
A5, A6	2F11
AB1-AB8	1F11
$\overline{AES}$	1G3
AEN	2G11
$\overline{AEN}$	1G5
B(A), B(B)	3C11
BRDY	1C1
C(A) C(B)	3F1
[illegible]	1G6
$\overline{CK/TRG2}$	2G7
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
DRQ3	[illegible]
$\overline{EOP}$	[illegible]
I(A) I(B)	[illegible]
$\overline{IB1}$-$\overline{IB8}$	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
S(A), S(B)	3C
T(A), T(B)	3F1
TC BUSAK	2F11
TC[illegible]	2A7
[illegible]	2A7, 3B
[illegible]	2A6
$\overline{WR}$	2F11
$\overline{IZ}$	1G1

REVISION

[illegible]	REVISED PER ECO# 20880 APP'D: [illegible]	FEB [illegible]	
[illegible]	REVISED PER ECO# 27151, 27856, 27936 APP'D: [illegible]	7/21/[illegible]	KTH
[illegible]	REVISED PER ECO# 26812 APP'D: [illegible]	[illegible]	
[illegible]	REVISED PER ECO# 29321 APP'D: [illegible]	4-24-[illegible]	[illegible]

WANG LABORATORIES, INC. LOWELL MASS. U.S.A.

MATERIAL	MODEL NO 23E-X21	DWN	CHK	E ENGR R.G.
FINISH	TOL EX AS NOTED	TITLE TC CONTROLLER MOTHERBOARD		
		SEE CHART	D	7859	4

WANG LABORATORIES, INC.

ONE INDUSTRIAL AVENUE, LOWELL, MASSACHUSETTS 01851, TEL. (617) 459-5000, TWX 710 343-6769, TELEX 94-7421

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