WANG

CUSTOMER ENGINEERING

IV.B.2-M

PRODUCT MAINTENANCE MANUAL FOR 2228D TELECOMMUNICATIONS CONTROLLER

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SECTION 1
INTRODUCTION

1.1 SCOPE

This document provides field personnel with the necessary information for installing, operating and troubleshooting the WANG 2228D Synchronous Telecommunication (TC) Controller (referred to as the 2228D TC Contoller in the remaining text).

1.2 ORGANIZATION

The documentation for the 2228D TC Controller is organized in the following manner.

Section 1	INTRODUCTION: This section provides the reader with the scope and organization of the 2228D TC Controller manual.
Section 2	DESCRIPTION: Contained in this section is a general description of the 2228D TC Controller and its related hardware, firmware software, and modems.
Section 3	THEORY OF OPERATION: In this section explanations of the electronic assemblies are provided in sufficient detail to aid the Service Representative in understanding the structure of the 2228D TC Controller.

Section 4	OPERATION: This section deals with toggle switch settings and LED indications.
Section 5	INSTALLATION: The necessary information for installing the 2228D TC Controller is supplied in this section. This includes initial set-ups, switch settings, installation and interconnection with modems.
Section 6	TROUBLESHOOTING: By performing the diagnostics and tests provided in this section the Service Representative can locate system faults to the board level.

SECTION 2 DESCRIP-TION

SECTION 2
DESCRIPTION

2.1 GENERAL DESCRIPTION

The 2228D is a combination motherboard (WLI #210-7658-A) and daughterboard (WLI #210-7659-A) Z80 microprocessor-based telecommunications controller, capable of supporting a variety of protocols over a single synchronous data link. The 2228D will be used only on the 2200 MVP, LVP, SVP and VP systems. Initially the 2228D will be released to the field supporting only 3271 emulation. Other synchronous and asynchronous protocols currently available on the 2228B will be available at some later date.

Besides having a RS-232-C interface, the 2228D will also provide a RS-449-C interface via a 37 pin male connector. Either the RS-232-C or RS-449-C interface is selected by the user via a toggle switch. The modem interface toggle switch, LED, RS-232-C connector, and RS-449-C connector are located on the mounting bracket (refer to Figure 1) and are visible with the controller mounted into the CPU.

With the RS-449-C interface, cable lengths and baud rates are significantly increased over RS-232-C connections. Depending upon the baud rate, a maximum of 4000 feet (1219 meters) of cable length between the data terminal equipment (DTE) and the data communications equipment (DCE) can be achieved.

The memory organization consists of 2K PROM (for bootstrap loading and power-up diagnostics) and 62K of RAM (for memory).

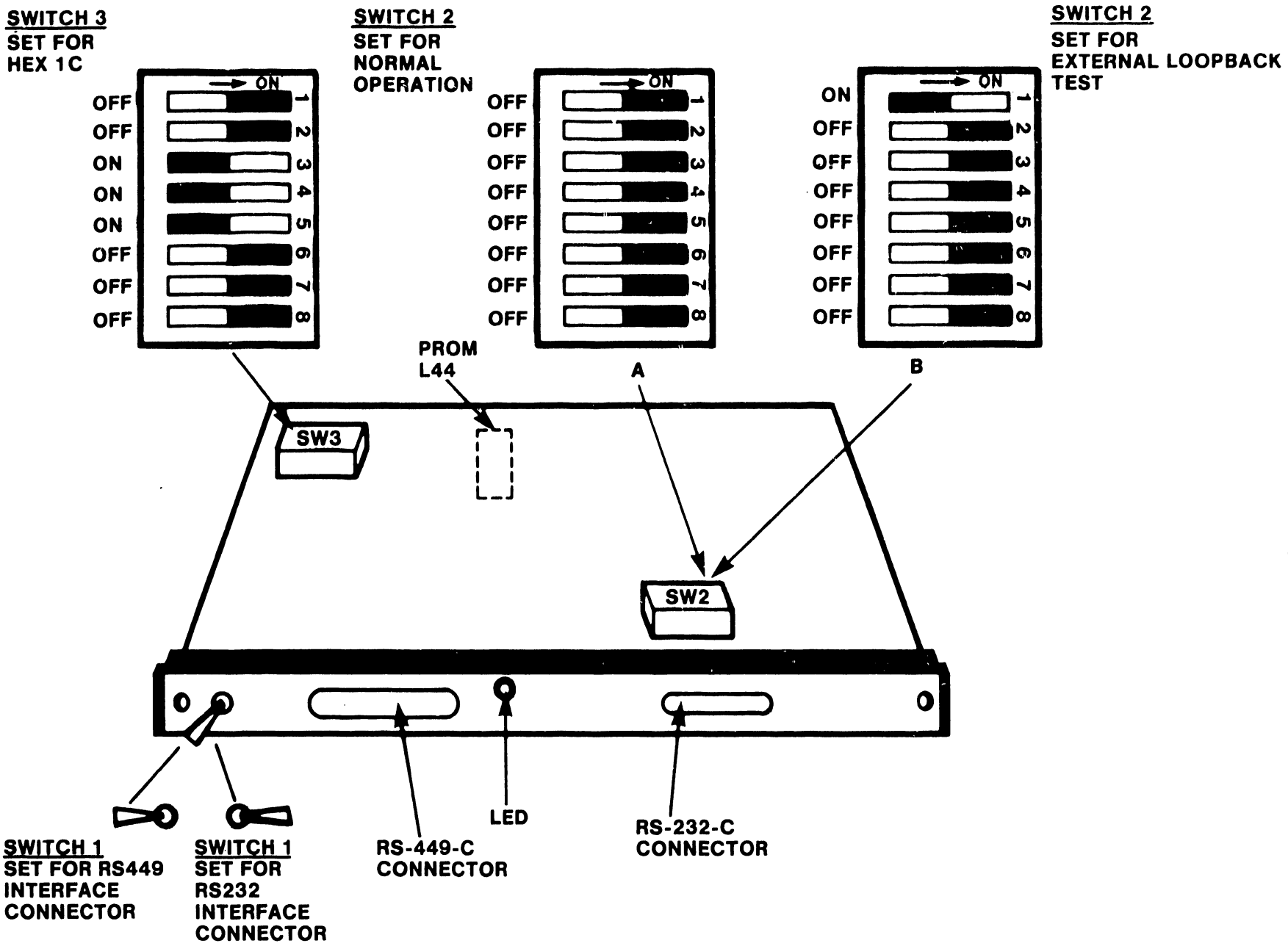

SWITCH 3
SET FOR
HEX 1C
ON
OFF
OFF
ON
ON
ON
OFF
OFF
OFF
1
2
3
4
5
6
7
8
SWITCH 2
SET FOR
NORMAL
OPERATION
SWITCH 2
SET FOR
EXTERNAL LOOPBACK
TEST
PROM
L44
A
B
SW3
SW2
SWITCH 1
SET FOR RS449
INTERFACE
CONNECTOR
SWITCH 1
SET FOR
RS232
INTERFACE
CONNECTOR
RS-449-C
CONNECTOR
LED
RS-232-C
CONNECTOR

FIGURE 1

2.2 PRODUCT HARDWARE DESCRIPTION

The purpose of the 2228D TC Controller is to:

1) Support new protocols including 3271 emulation, HDLC, X.25 and SNA.
2) Support synchronous protocols currently supported by the 2228B.
3) Support asynchronous protocols currently supported by the 2228B.

The 2228D contains a significantly higher degree of testability than previous controllers by having an internal serial loopback channel. The Theory of Operation (Section 3) defines in greater detail the existing hardware for the 2228D TC Controller.

2.3 PRODUCT SOFTWARE DESCRIPTION

Refer to the 3271 SOFTWARE EMULATION INSTALLATION MANUAL for information concerning 2228D software.

2.4 PRODUCT FIRMWARE DESCRIPTION

The 2228D TC Controller power-up diagnostic is factory loaded into a 2K power-up PROM (WLI #378-4219). This PROM is in location L44 of the Daughterboard (WLI #210-7659, refer to Figure 1). It has 1K for bootstrap loading and a second 1K for the power-up diagnostic.

2.5 MODEMS

The modem, or dataset, used with the system may be rented from the telephone company or purchased from any one of several modem vendors. In either case, the telephone company must connect the modem to the telephone network via telephone company installed data access arrangement (DAA). The DAA consists of a telephone handset and a modem

interface rented from the telephone company. Usually a modem or DAA is permanently wired to a wall; therefore, it should be installed as close as possible to the Wang word processing system.

NOTE

Ordering of a modem for a Wang Customer is not the responsibility of a Wang Salesman nor is the installation of a modem the responsibility of a Wang Serviceman.

The modems used at both ends of a communications line must be compatible. For example, if a BELL 201C type modem is used at one end, another BELL 201C or equivalent must be used at the other end (not a 201A, 208B, 202C, or 202S). The modems listed in Appendix J or their equivalents may be used.

2.5.1 MODEM INTERFACE RS-232-C

The controller conforms to the nationally recognized EIA RS-232-C and the internationally recognized CCITT V.24 standards for voltage levels and pin connections (refer to PRODUCT SERVICE TELEPROCESSING GUIDE, page 76). The signal polarity and the voltage of driven and detected signals are as follows:

Logic Level	Applied Voltage	Detected Voltage
0 or ON (Spacing)	+8 vdc	+5 to +15 vdc
1 or OFF (Marking)	-8 vdc	-5 to -15 vdc

The pin assignments are listed in Appendix H with both the EIA and the CCITT designations given for the circuit associated with each pin. Also, the signal descriptions and sources are included in Appendix H.

2.5.2 MODEM INTERFACE RS-449-C

The familiar RS-232-C interface standard has been used on almost all data communication terminals and modems manufactured since its adoption by the Electronic Industries Association (EIA). However, RS-232-C has serious shortcomings for use in modern data communications systems--the most critical being speed and distance limitations.

To overcome these shortcomings, the EIA has developed a successor to RS-232-C, called RS-449-C, which has improved performance specifications. For example, data rates have been increased from 20K bps in RS-232-C to 2M bps in RS-449-C. Also, maximum-transmission distances have been extended from 50 ft. to 200 ft (6.09 meters to 15.24 meters). In addition, RS-449-C supports remote loopback testing, and other control functions missing in RS-232-C.

The federal government has resently adopted RS-449-C as a federal standard. Therefore, RS-449-C is expected to come into widespread use during the 1980's and eventually replace RS-232-C altogether.

Differences between RS-232-C and RS-449-C

RS-449-C incorporates substantial changes from RS-232-C, for example:

NEW ELECTRICAL INTERFACE: The electrical characteristics of the RS-232-C interface are redefined in RS-449-C to allow greater transmission rates and distances.

NEW CONNECTOR: A 37-pin connector replaces the 25-pin connector used in the RS-232-C. This enables the use of the extra lines required by the expanded RS-449-C interface.

The RS-449-C interface differs mostly from RS-232-C in the electrical characteristics of the signals passing across the communications interface. For one thing, RS-449-C uses both balanced and unbalanced circuits to carry

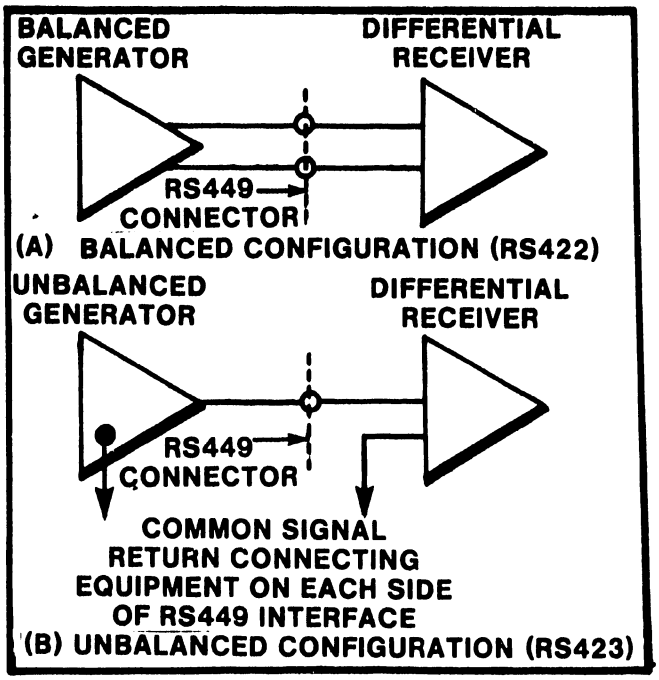


FIG. 2 RS449 INTERFACE CIRCUIT CONFIGURATIONS

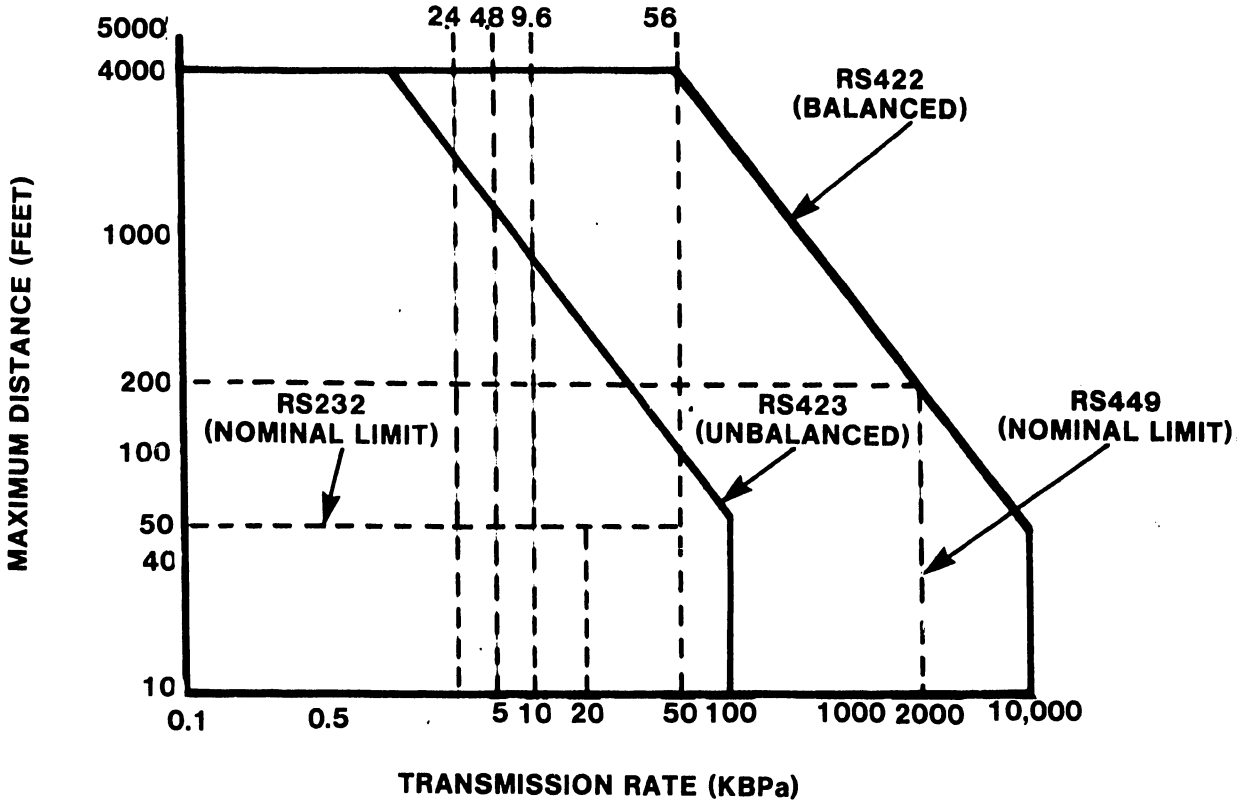


FIG. 3 PERFORMANCE PARAMETERS OF RS449 AND RS232 CIRCUITS

interface signals, with the balanced circuits carrying the most critical signals. The RS-232-C uses only unbalanced circuits. A balanced RS-449-Circuit, as defined in the RS-422-C standard, consists of a pair of wires connecting a balanced generator with a differential receiver (see Figure 2A). An unbalanced circuit, as defined in the RS-423-C standard, comprises a single wire connecting an unbalanced generator with a differential receiver (see Figure 2B), with electrical ground serving as a common return path for interface signals. The unbalanced circuit configuration is less expensive to implement, because it requires only one wire and connector pin for each interface function. The balanced configuration, however, offers better circuit performance in terms of distance and data rates transmitted.

The maximum transmission rates supported by RS-422-C and RS-423-C circuits differ with circuit length as shown in Fig. 3. RS-449-C sets nominal speed limits of 20K bps unbalanced circuits and 2M bps for balanced circuits. The distance limitation is 200 ft., but this limit can be exceeded in special applications by trading off speed for distance, or vice-versa.

2.5.3 COMPATIBLE BELL MODEMS

Initially the 2228D TC Controller will be released to the field supporting only 3271 emulation which is used in a leased line enviroment. Therefore, the 201C and 208A are two of the compatible Bell Modems. At a later date other asynchronous/synchronous protocols currently used on the 2228B will be available. The 201C and 208A modems are located in Appendix J along with the modems which will be used when additional protocols become availible.

SECTION 3

HARDWARE THEORY OF OPERATION

SECTION 3
HARDWARE THEORY OF OPERATION

3.1 INTRODUCTION

This section consist of three basic parts: an electrical section which gives a detailed description of the controller's major electrical components; a 2200 interface section which describes input/output lines; and a section on addressing the 2228D TC Controller.

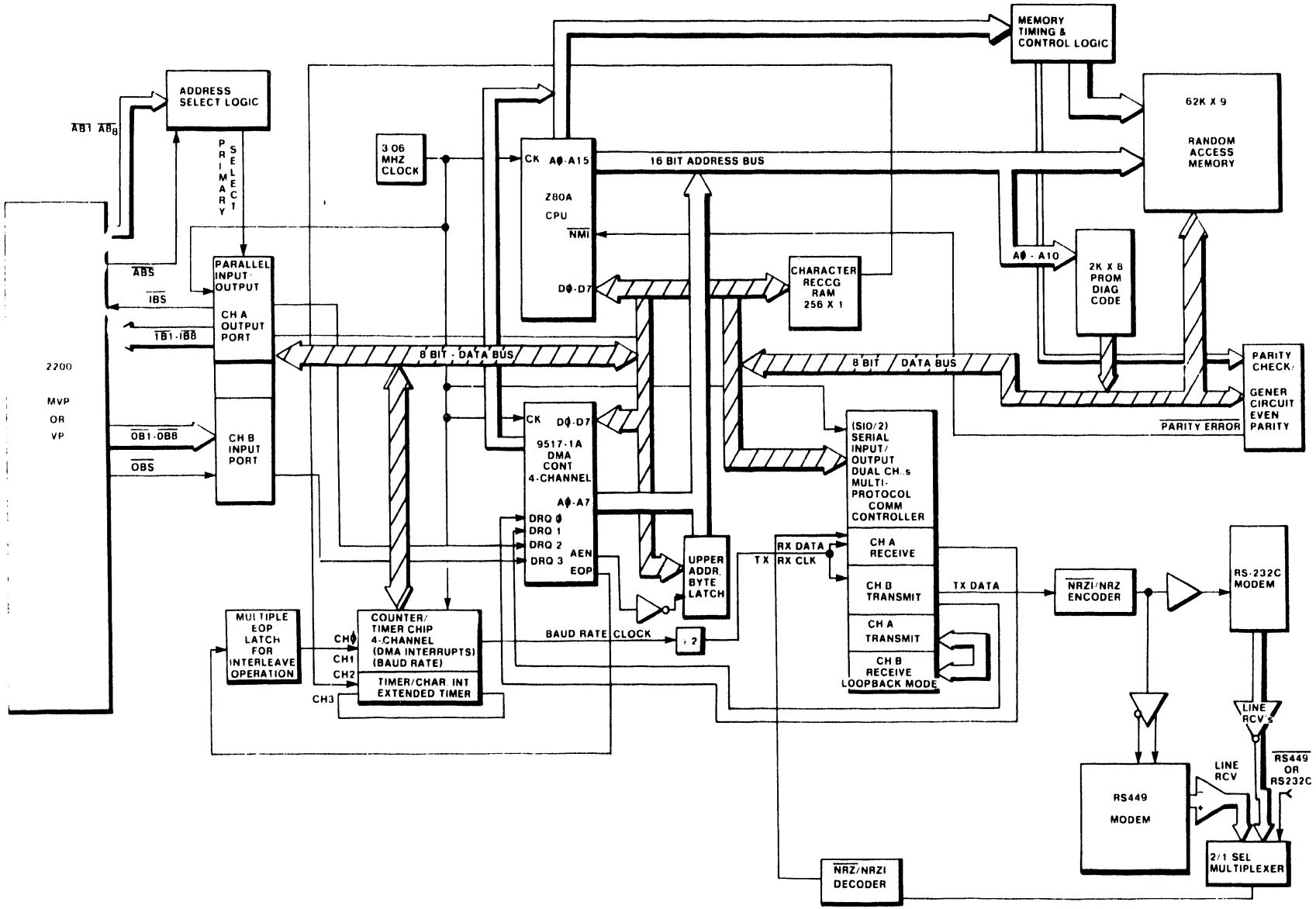
3.1.1 2228D TELECOMMUNICATIONS CONTROLLER

The 2228D is a microprocessor based telecommunications controller capable of supporting a variety of protocols over an asynchronous/synchronous data link. It is capable of supporting transmission speeds up to 9600 bits/sec. The operating frequency of system clock is at 3.06 Mhz. In addition, full duplex capability is possible with SDLC or HDLC protocols.

3.1.2 Z80 CPU

The Z80 CPU chip is the hub around which the DLP is built. It requires a single +5V power source and a single clock frequency, which in this case is 12.24 MHz. The chip uses a 16-bit address bus and an 8-bit data bus for bi-directional data flow. A reset line initializes the chip and six major status output lines. These lines are M1, MREQ, IORQ, RD, WR, and RFSH, which collectively inform the associated circuitry what function the CPU is about to perform. The M1 signal is active during the first cycle (the fetch cycle) of each instruction cycle and also during a special interrupt-acknowledge cycle that is discussed in further detail later in this discussion. The MREQ (Memory REQuest) signal is active when memory is being accessed to fetch either an instruction or data. The IORQ (Input/Output ReQuest) signal goes active to indicate an input or output to a peripheral device or during the same previously mentioned interrupt acknowledge cycle. The RD (Read) signal indicates that the CPU will input data while performing a memory access or I/O

BLOCK DIAGRAM OF 2228D TELECOMMUNICATION CONTROLLER



instruction, while the WR (WRite) signal indicates the CPU will output data. During an M1 (Memory period #1) fetch cycle, the CPU will output an address for memory refresh; the RFSH (ReFreSH) signal confirms the active presence of that address.

In addition, the Z80 CPU receives a BUSRQ (BUS-ReQuest) input, which requests the CPU to switch its address, data, and status bus lines into the high impedance state so that an outside device may use three buses. An associated BUSAK (BUS-AKnowledge) output goes active when the CPU has complied with this request. Another WAIT input requests the CPU to extend the current memory access or I/O cycle as long as it is active. Finally, the Z80 CPU uses two interrupt inputs, INT (INTerrupt) and NMI (Non-Maskable Interrupt). The non-maskable NMI input signal the DLP when a parity error occurs. The maskable INT signal serves as the interrupt input for all other interrupt-causing devices in the system and is under software control.

The Z-80 non-maskable interrupt is used for parity error reporting. Z-80 vectored interrupts, in order of decreasing priority, are generated by:

1) SIO channel A receiver
2) SIO channel A transmitter (used only by loopback diagnostic)
3) SIO channel A status (not used by bisync support)
4) SIO channel B receiver (used only by loopback diagnostic)
5) SIO channel B transmitter
6) SIO channel B status (not used by bisync support)
7) CTC channel 0 software timer
8) CTC channel 1 used for internal clocking to the SIO for asynchronous mode and clocking for secondary request to send during synchronous mode.
9) CTC channel 2 (interrupt vector source for all DMA channels)
10) CTC channel 3 (interrupt vector source for Ring Indicator/Incoming Call Signal).
11) PIO channel A
12) PIO channel B

3.1.3 INPUT/OUTPUT ARCHITECTURE

All I/O hardware is addressed as input-output ports by the DLP. Memory mapped I/O is not used. The I/O port addresses are summarized in the following table:

PORT	OUTPUT PORT DESTINATION	INPUT PORT SOURCE
X'00'	SIO Channel A Data Register	SIO Channel A Data Register
X'01'	SIO Channel B Data Register	SIO Channel B Data Register
X'02'	SIO Channel A Command Reg.	SIO Channel A Status Reg.
X'03'	SIO Channel B Command Reg.	SIO Channel B Status Reg.
X'10'	DMA Channel 0 Address Reg.	DMA Channel 0 Address Reg.
X'11'	DMA Channel 0 Word Count Reg.	DMA Channel 0 Word Count Reg.
X'12'	DMA Channel 1 Address Reg.	DMA Channel 1 Address Reg.
X'13'	DMA Channel 1 Word Count Reg.	DMA Channel 1 Word Count Reg.
X'14'	DMA Channel 2 Address Reg.	DMA Channel 2 Address Reg.
X'15'	DMA Channel 2 Word Count Reg.	DMA Channel 2 Word Count Reg.
X'16'	DMA Channel 3 Address Register	DMA Channel 3 Address Reg.
X'17'	DMA Channel 3 Word Count Reg.	DMA Channel 3 Word Count Reg.
X'18'	DMA Command Register	DMA Status Register
X'20'	CTC Channel 0 Control Reg.	CTC Channel Status Reg.
X'21'	CTC Channel 1 Control Reg.	DMA Channel 1 Status Reg.
X'22'	CTC Channel 2 Control Reg.	CTC Channel 2 Status Reg.
X'23'	CTC Channel 3 Control Reg.	CTC Channel 3 Control Reg.
X'40'	Int. Clock Enable Reg. D0	User Option Switches
X'40'	Syn./Asyn Tran., D4	
X'40'	NRZ/NRZI Mode Register, D1	
X'50'	PIO Ch-A Data ENDI=0	PIO Ch-A Data In Register
X'51'	PIO Ch-B Data Out; ENDI=0	PIO Ch-B Data In Register
X'52'	PIO Ch-A Control Register	
X'53'	PIO Ch-B Control Register	
X'54'	PIO Ch-A Data Out; ENDI=1	
X'60'	2200 Reguest Status Reg.	
X'70'	LED Status	

3.1.4 COUNTER TIMER CIRCUIT (CTC)

The Z80A - CTC will provide the updated features as follows:

1. A source of interrupts for the DMA to SIO interface on both the SIO Received Channel A and the SIO Transmit Channel B;

2. A source of interrupts for the DMA to PIO interface on PIO both the Output Channel A and PIO Input Channel B;

3. A counter for character interrupts SIO Receiver Channel A;

4. A dedicated software timer on channel 3 and an extended software timer feature that starts on channel 2 connected in series with channel 3;

5. An internal clock for diagnostic loopback test on the SIO, CRC check on the SIO Receive Channel A, and null modem application; and

6. A programmable baud rate clock generator.

The overall operation of the CTC is diagrammed on the next page.

CTC Channel	Operating Mode	Signal Input	Clock Output
0	Counter must be Set to 1.	End of Process (EOP From DMA Multiple EOP Latch Circuit	None
1	Timer	None	SIO CH.A RCV CLK & SIO CH.B XMIT CLK Internal Clock For SIO Loopback Test on SIO XMIT CH.A & SIO RCV. CH. B To RS232 Pins 19 & 11; Internal Clock For CRC Characters & Null Modem Application.
	Counter	Transmit Clock From Either RS-232 or RS-449.	SIO XMIT CH.B Clock for Checking SDLC/ HDLC Flag Characters
2	Counter	Character Interrupt Signal (Bisync Operation of SIO)	None
	Timer	None	None
3	Timer	None	None

3.1.5 SYNCHROUNOUS INPUT/OUTPUT (SIO) CHIP AND MODEM RS-232-C INTERFACE

The RS-232 modem connector is interfaced through a SIO chip, which also supports an internal loopback diagnostic capability. The SIO chip contains two transmit channels and two receive channels. Transmit channel A output is connected to receive channel B for internal loopback diagnostic use. Transmit channel B and receive channel A are connected to the RS-232 connector via a multiplexer. SIO receive channel A is connected to DMA channel 0, and SIO transmit channel B is connected to DMA channel 1.

CTC channel 1 provides the synchronous clocking for the diagnostic loopback channels and may be switched into receive channel A under program

control in order to guartantee clock pulses for the cyclic redundancy check (CRC) in the HDLC and SDLC mode. It is also outputted to RS-232 connector pin 11, which is the otherwise unused Secondary Request to Send signal, for null modem use.

Signals are routed among the SIO channels and RS-232 connector as shown:

DESTINATION SIGNAL	SOURCE SIGNAL
SIO channel A Carrier Detect	Modem pin 8 Carrier Detect
SIO channel A Receive Clock	Determined by Clock Mode Reg.
SIO channel A Receive Data	RS-232 pin 3 Receive Data
RS-232 pin 20 Data Terminal Ready	SIO channel B Data Terminal Ready
RS-232 pin 4 Request to Send	SIO channel B Request to Send
SIO channel B Clear to Send	RS-232 pin 5 Clear to Send
SIO channel B Transmit Clock	RS-232 pin 15 Transmit Clock
RS-232 pin 2 Transmit Data	SIO channel B Transmit Data
SIO channel A Clear to Send	SIO channel A Request to Send
SIO channel A Transmit Clock	CTC channel 1 Clock Output
SIO channel B Carrier Detect	RS-232 pin 6 Data Set Ready
SIO channel B Receive Data	SIO channel A Transmit Data
SIO channel B Receive Clock	CTC channel 1 Clock Output
RS-232 pin 11 Sec. Req. to Send	CTC channel 1 Clock Output

3.1.6 SYNCHRONOUS INPUT/OUTPUT (SIO) CHIP AND MODEM RS-449-C INTERFACE

Besides having an RS-232C interface, the 2228D will also provide a RS-449 interface via a 37 pin male connector. This interface will be multiplexed along with the RS-232C interface. The RS449 interface will be selected by the 2228D when the toggle switch is switched to RS449 position. The RS449 interface provides a functional interface between the data terminal equipment and the data communication equipment for use with the electrical characteristics specified in the EIA standards RS-422 and RS-423. The 2228D will support directly the RS-422 specification which provides differential or balanced - voltage digital line driver and line receiver interface. With RS-422 interface, longer cable lengths and faster baud rates are significantly

increased over RS-232C connections. Depending upon the data modulation rate, a maximum of 4,000 feet of cable length between the data terminal equipment and the data communication equipment can be achieved.

The RS-423 specification will not be supported by the 2228D. The RS423 specification covers the single-ended or unbalanced digital interface portion of the overall RS-449 specification.

When the RS-422 circuit is selected, the signals are multiplexed through the SIO chip. Below is a routing of the RS-449 signal to the SIO.

DESTINATION SIGNAL	SOURCE SIGNAL
SIO channel A Carrier Detect	RS-449 pins 31 & 13 Receive Ready
SIO channel A Receive Clock	RS-449 pins 8 & 26 Receive Timing to be determined by Clock Mode Reg.
SIO channel A Receive Data	RS-449 pins 6 & 24 Receive Data
RS-449 pins 12 & 30 Terminal Ready	SIO channel B Data Terminal Ready
RS-449 pins 7 & 25 Request to Send	SIO channel B Request to Send
SIO channel B Clear to Send	RS-449 pins 9 & 27 Clear To Send
SIO channel B Transmit Clock	RS-449 pins 5 & 23 Send Timing
RS-449 pins 4 & 22 Send Data	SIO channel B Transmit Data
SIO channel B Carrier Detect	RS-449 pins 11 & 29 Data Mode

Hence the SIO chip has the option to connect its transmit B and receive channel A to the RS-449 connector when such a connection is needed.

3.1.7 SET SECONDARY REQUEST TO SEND AND CLOCK MODE

After power on reset has been initiated, the clock mode register is presetted to a logic 1, thus enabling synchronous clock transmission to the SIO's transmitter and receiver clocks. The SIO receiver clock comes from either the Modem RS-232 pin 17 receive clock signal or the RS-449 pins 8 & 26 receive timing while the SIO transmitter clock comes from the modem RS-232 pin 15 transmitter clock signal or the RS-449 pins 5 & 23 send timing. The modem

control signal, Secondary Request to Send is driven by an internal clock signal during synchronous transmission via CTC channel 1 clock output after power on reset, thus enabling usage for null modem application.

When an OUT 40 instruction has been executed, the clock mode register selects either asychronous or synchronous transmission mode depending upon the value of D0. If D0 is a logic 1, then asynchronous transmission is selected. The SIO transmitter and receiver clock is derived from their clock sources from the CTC channel 1 clock output during asychronous mode. Also, at this time, the modem control signal, Secondary Request to Send, is set ON or OFF depending upon the value of D4. This allows for secondary channel break transmission using half duplex 1200 bps modems.

3.1.8 CHARACTER RECOGNITION

With an addition of a 1Kx1 static RAM (2102A-2) and some additional control logic, up to 256 character patterns can be used for recognition to signal a character interrupt during synchronous operation of the SIO/2 - A on the receiver channel. The databus will provide the RAM chip address. Address bit A0 from the Z80A is wired to the data input of the static RAM. This bit will distinguish the two OUT commands from the Z80A.

An OUT "31" instruction will execute incremental data from the Z80A accumulator of HEX "00" through HEX "FF" during a write cycle to the static RAM. This procedure initializes the RAM chip so that no interrupt will take place during SIO RCV DMA mode. The value of A0 will be a logic 1 at that time.

An OUT "31" instruction with the value of A0 equal to a logic 0 and the correct interrupt character code from the databus will be loaded into the static RAM. Thereafter, a read cycle into the static RAM and the correct interrupt code will then cause the RAM to output an active low signal. This signal is then clocked by the DMA output signals to trigger channel 0 of the CTC. The CTC, inturn, will generate and 8 bit interrupt vector on the databus during maskable interrupt mode 2. This character recognition is useful during Bi-Sync operation via the DMA chip.

3.1.9 9517 - 1 DMA CHIP

To relieve CPU's overhead during high speed data transfers between peripheral devices and system's memory, and 9517-1 DMA controller will provide high-speed single, byte transfer modes:

1. From the controller's memory through the Z80 - A SIO/2 chip to the RS-232 connector Transmit Data signal or the RS - 449 connector Send Data;

2. From the RS - 232 or the RS - 449 connector Receiver Data signal through the Z80A - SIO/2 chip to the controller's memory;

3. From the controller's memory through the Z80A - PIO chip to the controllers memory; and

4. From the 2200 I/O bus through the Z80A - PIO chip to the controller's memory.

The DMA request input lines are to be programmed for active high. The DMA acknowledge outputs are to be programmed for the active low state. Z80A-CTC channel 2 will provide a DMA completion interrupt to the Z80A for all four DMA channels. The Z80 CTC Channel 3 will provide an interrupt routine for the ring indication.

The CK/TRG0 thru CK/TRG3 of the Z80A - CTC should be programmed to receive active low trigger inputs. The connection of the DMA chip are as shown:

DMA CHANNEL	DATA SOURCE	DATA DESTINATION	DMA CYCLE
0	SIO Rcv. CH. A	Memory	Write
1	Memory	SIO XMIT CH. B	Read
2	PIO CH.A. INPUT	Memory	Write
3	Memory	PIO CH.B OUTPUT	Read

By executing an IN"18" instruction, the DMA status register output can be read by the Z80A. The status register contains information on which channels have reached a terminal count and which channels have pending DMA requests. Bit 0-3 are set everytime the terminal count is reached by that channel. Hence, an IN "18" instruction will distinguish which channels have triggered an interrupt vector via the CTC. By examining the status register contents, the programmer will know when the first interrupt service routine has been completed prior to receiving another interrupt request during any successive terminal counts or pending DMA requests. The complete I/O port address assignments to the AMD's 9517 DMA chip is shown as follows:

PORT	OUTPUT PORT DESTINATION	INPUT PORT SOURCE
X'10'	DMA ch 0 address register	DMA ch 0 address register
X'11'	DMA ch 0 word count reg.	DMA ch 0 word count reg.
X'12'	DMA ch 1 address reg.	DMA ch 1 address reg.
X'13'	DMA ch 1 word cou t reg.	DMA ch 1 word count reg.
X'14'	DMA ch 2 address reg.	DMA ch 2 address reg.
X'15'	DMA ch 2 word count reg.	DMA ch 2 word count reg.
X'16'	DMA ch 3 address reg.	DMA ch 3 address reg.
X'17'	DMA ch 3 word count reg.	DMA ch 3 word count reg.
X'18'	DMA command register	DMA status register
'19'	DMA request register	Illegal
X'1A'	DMA single mask reg. bit	Illegal
X'1B'	DMA mode register	Illegal
X'1C'	DMA clear byte pointer flip flop	Illegal
X'1D'	DMA master clear	DMA temporary reg.
X'1E'	Illegal	Illegal
X'1F'	DMA all mask reg bits	Illegal

3.1.10 MEMORY ORGANIZATION

Memory consists of 2K PROM, for bootstrap loading and power-up diagnostics, along with 62K of available RAM. The RAMs are MOS 16Kx1-bit, dynamic memory circuits, having a chip access time of 150 nanoseconds and a read/modify-write cycle time of 320 nanoseconds. The PROM occupies address space 0 through 2K, while the RAM occupies address space 2K + 1 through 64K. Parity checking of RAM is supported. A parity error should trigger the Z80 non-maskable interrupt, and initiate an interrupt to the 2200.

3.1.10.1 MULTIPLEXED MEMORY ADDRESSING

Each MOS memory chip is physically arranged as a two-dimensional array of cells. Certain address inputs are used for row selection and the remaining address inputs are used for column selection. Row selection is required before the sense amplifiers can begin their slow detection process. Column selection is not required until the outputs of the sense amplifiers become valid, however, because its function is to gate data from the selected sense amplifier to the data output circuitry. Since the column selection information is not used internally until well after the row selection information is required, only the row addresses need to be available to the chip at the start of a cycle. The column address thus can be determined later with no penalty of access time. The multiplexed memory address technique takes advantage of this delayed need for a column address; rather than using 13 address lines to select one of 16,384 memory cells, the memory first uses seven address lines to select one of 128 rows and then subsequently uses those same seven lines to select one of 128 columns in that selected row.

3.1.10.2 MULTIPLEX TIMING CONSIDERATIONS

Although address multiplexing provides some very substantial system benefits, it complicates system timing. The multiplexing technique requires that both row and column addresses get into the chip within a short time, using the same address pins. The requirement establishes a rather tight timing window during which the individual events must occur. The sequence of

events required to address any given memory-chip location is as follows:

1) Establish a 7-bit row address to specify one of 128 rows of storage cells in the chip.

2) Bring the RAS (Row Addrss Strobe) signal low to start the row selection process by the chip's sense amplifiers.

3) Maintain that same row address valid for some minimum hold time to allows the chip's sense amplifiers to complete the detection process.

4) Establish a 7-bit column address (on the same address lines) to specify one of 128 columns in the selected row of memory storage cells.

5) Bring the CAS (Column Address Strobe) signal low to confirm the stabilized column address.

6) Hold that same column address valid for some minimum hold time to allow the chip's sense amplifiers to complete the column-address detection process (and to allow the associated read/write operation for the resultant location).

To achieve the specified access time from RAS, CAS must be brought low within some specified maximum delay after RAS goes low.

To summarize, the functions of RAS are to initiate a cycle, to strobe or latch the row address, to enable the selected row of memory cells, to sense and restore the data in that row of memory cells, and to maintain the sensed data from the entire row of addressed memory cells in their respective sense amplifiers. The sense amplifiers maintain this data as long as RAS remains active. At the end of a cycle, when RAS is taken high, the selected row is immediately turned off, isolating the correct data in the cells. After the row is off, the half-digit lines are prepared for a new cycle.

CAS, on the other hand, controls column selection circuitry and the transfer of data from the selected sense amplifier to the output circuitry. After RAS strobes the row address information from the multiplexed address input pins, CAS strobes the column address from the same pins. When CAS goes active (low), the column address is strobed or latched into the circuit. This address is then decoded to select the proper column. Data from the selected sense amplifier is then transfered to the output buffer, completing the read-access operation.

The 2716 PROM is fully-static 16,348-bit (2048 X 8), erasable programmable read-only memory.

3.2 WRITE BAD PARITY (OUT'71')

Additional circuitry has been added on to allow writing bad parity to the databus. An OUT '71' instruction executed by the Z80A will force a one on the 9th bit of a even number of ones pattern, thus causing a parity error for even parity. The parity error will then trigger the Z80 non-maskable interrupt to location 0066. This feature will verify the performance of the parity check circuit.

3.3 LED STATUS DISPLAY (IN '70')

To make room for the OUT '71' instruction for writing bad parity, an IN '70' instruction will be used by the Z80A to extinguish the LED, thus indicating that the system diagnostic software is running. The LED will still be initially illuminated upon power-up, indicating that the system is ON.

3.4 NRZ/NRZI MODE

Upon power up, the NRZ/NRZI mode register will select the NRZ mode. The SIO will then transmit the data in the non-return to zero (NRZ) format. The NRZ code is a conventional digital code that has a TTL level in which a bit interval is one full clock period long.

When D1 is executed with an OUT 40 instruction, the NRZ/NRZI mode register will be enabled. A logic 0 on D1 will select a NRZ code while a logic 1 on D1 will enable the NRZI code format. Unlike the NRZ format, the NRZI code is an invert-on-zero transmission coding. To send a binary 1, the controller will hold the signal condition in the same state whereas to send a binary 0, the controller will change the signal condition to the opposite state. The 2228D is provided with the option of transmitting and receiving digital data in the NRZI code when D1 is a logic 1 in the NRZ/NRZI mode register.

3.5 2200 INTERFACE

The major features of the 2228D interface to the 2200 are:

1) The 2200 may hard reset the 2228D under program control, as can the 2228B. (see 3.7.1)

2) The 2228D can interrupt the 2200 under microcode control, as can the 2228B. (see 3.7.1)

3) Data transfer between the 2228D and 2200 can use hardware DMA to the 2228D memory, providing speed and effeciency for both processors.

4) Data transfer are buffered by Zilog PIO chip which provides most of the signal synchronization.

3.6 2200 I/O Bus Signals

The 2200 I/O bus signals are described in this section will make the following sections describing 2228D specifics more understandable.

3.6.1 ADDRESS LINES AND ABS STROBE

The 2200 selects a controller with which it wishes to communicate by setting the 8-bit address on the address lines and pulsing the ABS-Strobe

signal line. A controller may respond to one or more addresses. The 2228D responds to two, as described in section 3.7.1.

3.6.2 RESET STROBE

The 2200 pulses the Reset-Strobe signal line whenever the reset key on the keyboard is depressed. The 2228D ignores this signal.

3.6.3 DATA INPUT LINES, ENDI-SIGNAL, CPB-SIGNAL, AND IBS-STROBE

The 2200 sets CPB-signal off (CPB=logic 1) whenever it will accept data from the controller, and sets CPB-signal on whenever it will not accept data from the controller. When CPB signal is off and the controller wishes to send a byte of data to the 2200, it sets the data-input lines to the value of the data byte, sets the ENDI-signal to the desired value, and pulses IBS-strobe. The ENDI-signal, whose value is determined by the output port, is latched by the 2228D when a data byte is outputted to the PIO. As used by the 2228D, it signals end-of-block when set.

3.6.4 DATA OUTPUT LINES, RDY-SIGNAL, OBS-STROBE, AND CBS - STROBE

The controller sets RDY-signal on (active low for RBI) whenever it will accept data from the 2200, and off whenever it will not accept data from the 2200. When RDY is on and the 2200 wishes to send a byte of data to the controller, it sets the data-output lines to the value of the data byte and pulses either CBS-strobe or OBS-strobe. The 2228D uses only OBS-strobe as a data strobe. CBS-strobe is used to generate a hardware reset of the controller (see section 3.7).

3.7 ADDRESSING THE 2228D CONTROLLER

Like other 2200 system telecommunications controllers, the 2228D contains a set of 8 device address switches. The value set into these switches defines

the primary device address used by all 2200 I/O statements which interchange data with the controller. A secondary device address, equal to the primary device address with the high order bit inverted, is used by the 2200 to test a request status bit set by the 2228D microcode.

When the 2200 I/O bus issues an ABS strobe, the contents of the address bus are compared with the primary device address. If they are equal, the controller is selected as the currently active device and dialog may proceed between the 2200 and the controller.

When the 2200 I/O bus issues an ABS strobe, the contents of the address bus are also compared with the secondary device address. If they are equal, the 2200 I/O bus "ready" signal is set equal to the request status bit.

3.7.1 RESETTING THE 2228D BY THE 2200

Like the 2228B, the 2228D is not reset by the 2200 reset-strobe signal. It is reset under program control by the 2200 when a byte having the high-order bit set 1 is output with a CBS strobe. This reset operation causes the Z80 and all resettable hardware to be reset. The Z80 starts executing at address 0, causing it to initialize all programmable parts of the controller hardware.

3.7.2 2200 REQUEST STATUS REGISTER

The Request Status Register contains one bit, bit-0, which determines the value of the 2200 RDY-signal when the secondary address is selected. The request status bit (RBI) may be tested by an $IF ON statement or used as an interrupt request condition. The interrupt request is set when the request status register is a logic 0 conversely, the interrupt request bit is not set when the request status register is a logic 1.

3.7.3 PARALLEL INPUT/OUTPUT (PIO) CHIP

Data transfer between the DLP (data link processor) and the 2200 is through a two-channel PIO chip. Channel A is used in "output mode" to transfer data from the DLP to the 2200 input bus. Channel B is used in "input mode" to transfer data from the 2200 output bus to the DLP. Signals are routed among the PIO channels and 2200 input/output bus as shown:

DESTINATION SIGNAL	SOURCE SIGNAL
PIO channel A strobe	2200 CPB-Signal is off, Primary select is on, PIO channel A ready is on.
2200 IBS - Strobe	
PIO channel B strobe	2200 OBS-Strobe and Primary Select is active low
2200 BDY - Signal	PIO channel B Ready

Logic must pulse:

1) 2200 IBS - Strobe at the first occasion when 2200 CPB - signal is off and PIO channel A ready is ON.

2) PIO channel A strobe at the first occasion <u>following pulsing 2200 IBS - strobe</u> when 2200 CPB - signal is ON and PIO channel A ready is OFF.

SECTION 4 INSTAL-LATION

SECTION 4
INSTALLATION

4.0 INITIAL SET-UPS

The initial set-ups prepare the 2228D TC Controller for installation into the 2200 mainframe.

4.1 INTRODUCTION

Before installing the 2228D TC Controller for customer use, perform in sequential order, sections 4.1.1 thru 4.1.3.

4.1.1 PARTS CHECKLIST

The only parts required for this installation procedure are the 2228D TC Controller Board (WLI #177-2228D) and a 12ft TC Cable (WLI #220-0113), which is needed for modem connection.

4.1.2 PROM REVISION-LEVEL CHECK

Check the PROM for a recent updating of revision-level. Up to the date of this writing, PROM chip L44 (WLI #378-4219) should be Revision 1.0 or higher.

4.1.3 SWITCH SETTINGS

The software defined User Option Switches are used to set the site address of a multipoint secondary station and to set any other user options. The switch settings are read into the Z80 accumulator. Prior to installing the 2228D into the 2200 CPU, set switches SW 1, 2, and 3 (located on the Motherboard, WLI #210-7658-A) as follows below. Refer to Figure 1 for switch

locations.

A. Modem Interface Toggle Switch (SW 1)

The Modem Interface Toggle Switch (SW 1) can be used to select either the RS-232-C or RS-449-C interface connector. This switch has two positions; one is labeled "RS232"; the other, "RS449". Select the desired interface connector by positioning the switch as follows: set switch toward the RS-interface connectors for RS-232-C, set switch away from RS-interface connectors for RS-449-C (refer to Figure 1).

NOTE

During initial set-up of the 2228D TC Controller, set the modem-interface toggle switch for selection of the RS-232-C interface.

B. SIO Bisync External/Internal Test Option Switch (SW 2)

The Test Option Switch (SW 2), is not utilized during normal operation (all slide switches OFF; refer to Figure 1A)). It is used for the diagnostic External Loopback Test. This test is performed during initial installation or during unit troubleshooting; therefore, select a HEX 01 (slide switch 1 of SW2 ON; the others of SW2 OFF; refer to Figure 1B). This enables the Power-Up Diagnostics to run the SIO Bisync External and Internal Loopback tests (only the Internal test runs when SW2 is in the OFF position).

NOTE

When the External Loopback Test is completed, set the Test Option Switch to HEX 00 (all slide switches of SW2 OFF; refer to Figure 1A).

C. Device Address Switch SW 3:

Before installing the 2228D Telecommunications Controller into the local 2200 CPU, set the Device Address Switch (SW 3), located on the 2228D Motherboard (WLI #210-7658-A), to HEX 1C (set slide switches 3, 4, and 5 of SW3 to ON and the others to OFF; refer to Figure 1).

NOTE

If a 2228B TC Controller board is presently installed in the 2200 CPU, ensure its device address is set to HEX 1C. The 2228D device address should then be set to 1F. (Set slide switches 1, 2, 3, 4, and 5 to ON set 6, 7, and 8 to OFF.)

4.1.4 2228D INITIAL INSTALLATION

Turn the CPU ac power switch OFF and install the 2228D TC Controller into any available 2200 MAINFRAME I/O slot away from the fan.

CAUTION

THE 2228D TC CONTROLLER IS SLIGHTLY LARGER THAN OTHER SYSTEM 2200 CONTROLLERS. THEREFORE TO PREVENT IT FROM CONTACTING THE FAN, INSTALL IT INTO ANY AVAILABLE 2200 MAINFRAME I/O SLOT AWAY FROM THE FAN.

Refer to the following manuals for figures showing PCB layout.

MANUAL/CATEGORY	FIGURE NO.	PAGE NO.
MVP/IV.A.3	1-8	1-9
VP/IV.A.3	3-1	3-4
LVP/IV.A.3	8-2	8-4

NOTE:

Upon initial installation of the 2228D TC Controller the RS-232-C Loopback Test must be performed. Therefore, install the RS-232-C loopback plug (WLI #350-1030; for wiring diagram refer to Appendix D) into the RS-232-C connector (see Figure 1), then, go to section 6.6.2 and perform the RS-232-C Loopback Test.

4.2 2228D INSTALLATION

The installation of the 2228D TC Controller into a 2200 VP, SVP, MVP or LVP mainframe is accomplished by the following steps:

a. Turn the CPU ac power switch OFF.
b. Remove the loopback plug (if inserted) from the RS-232-C connector.
c. Remove the 2228D TC Controller board from the 2200 CPU chassis.
d. Set the Test Option Switch (SW 2) to OFF (all slide switch OFF).
e. Re-install the 2228D TC Controller board into any available 2200 mainframe I/O slot away the from fan.
f. Power-Up CPU (refer to 2228D Power-Up Diagnostics in section 6.6.1).

4.3 INTERCONNECTION WITH MODEMS

A standard 12ft RS-232-C TC cable (WLI #220-0113) is provided to connect the 2228D TC controller to the modem. Connect the cable from the RS-232-C female connector located on the controller mounting bracket to the RS-232-C female connector on the modem (for most Bell modems, this connector will be labeled "CUST. EQUIP.").

4.3.1 Optional cables

For distances longer than 12ft the following optional cables are available.

	Wang Part Number	
Length	RS-449-C	RS-232-C
25ft	120-2325-01	220-0219
50ft	120-2325-02	220-0220
100ft	120-2325-03	N/A
250ft	120-2325-04	N/A
500ft	120-2325-05	N/A
750ft	120-2325-06	N/A
1000ft	120-2325-07	N/A

SECTION 5 OPERATION

SECTION 5
OPERATION

5.0 INTRODUCTON

This section provides information on modem interface toggle switch settings and LED indications. This information is needed to operate the 2228D TC Controller.

5.1 MODEM INTERFACE TOGGLE SWITCH SETTING

Set the Modem Interface Toggle Switch as indicated in step A of section 4.1.3.

5.2 LED INDICATIONS

Within 10 to 15 seconds of powering-up the LED located on the mounting bracket (see Figure 1), will give one of the following three indications.

A. LED EXTINGUISHES (BOARD PASSED)

The LED extinguishes within 10 to 15 seconds after powering up. This indicates that all TC Controller Power-Up Tests have passed, and the program enters the 2228D bootstrap firmware.

B. LED REMAINS ON (CATASTROPHIC FAILURE)

If the LED remains ON after approximately 15 seconds (catastrophic failure), replace the 2228D TC Controller board.

C. LED FLASHING (REPORTABLE FAILURE)

If the LED is FLASHING (reportable failure) go to section 6.6.3 (2228D TC Controller Power Up Error Code Interpreter).

SECTION 6

TROUBLESHOOTING DIAGNOSTICS

SECTION 6
TROUBLESHOOTING/DIAGNOSTICS

6.1 INTRODUCTION

Troubleshooting the telecommunications system can be a complex task. There are many components involved, such as telephone lines, modems, and host computers, any one of these can cause a problem. This section provides tests and diagnostics for troubleshooting these components. When a problem is encountered in the telecommunications system at installation time refer to the Troubleshooting Checklist (section 6.2). This checklist is designed to assist the Customer Engineer in locating and repairing faults in the telecommunications system.

6.2 TROUBLESHOOTING CHECKLIST

The first thing any service representative should do is to check the installation items as follows.

a) Check the entire 2200 system by running the SYSTEM LEVEL DIAGNOSTICS available in section 6.6.4 and checking all voltages. To check voltages refer to the following product maintenance manuals for the CPU VOLTAGE CHECK/ADJUSTMENT PROCEDURES.

MANUAL/CATEGORY	SECTION NO.	PAGE NO.
LVP/IV.A.3	11.2	11-2
VP/IV.A.3	3.3.2	3-12
MVP/IV.A.3	7.3.2	7-5

b) Check the PROM level. Up to the date of this writing, PROM chip L44 (WLI #378-4219) should be revision 1.0 or higher.

c) Check the 2228D TC Controller for correct device address, assuring switches SW 1, 2, and 3 (located on the 2228D motherboard, WLI # 210-7658-A) are set as indicated in section 4.1.3. Visually inspect

the board for any broken components, short etches, etc. Make sure the board is seated properly into its connectors.

d) Run the Power-Up Error Code Interpreter (refer to section 6.6.3). This diagnostics will test 2228D TC Controller and will aid in troubleshooting hardware faults..

e) Check the T.C. cable for any bad contacts. Do a continuity check on the cable from one end to another end and make sure all the required signal wires are connected on both ends of the cable.

f) Call the Telephone Data Service Center and have the modem checked. If possible be present when the modem service representative arrives and show him the problem.

g) Make sure the host computer can, in fact, support the Wang system. For example, the host computer can support only single record blocks, in that case a change in the Wang Software is required to accomodate host computer compatibility.

h) Get in touch with data processing personnel at the host computer and discuss the sign-on procedure and explain the problem. Almost all of the sign-on type problems can be resolved this way. If you know anyone else using the same host computer or similar system, find out how he is using it.

i) Most important of all, try to get help from your area office, program analyst, home office, or anyone you know who has a telecommunications background.

6.3 ITS-1 EIA INTERFACE TEST SET

The model ITS-1 EIA Interface Test Set is a self-contained pocket size test set that can be inserted between the Data Communication Equipment (DCE) or modem and Data Terminal Equipment (DTE). It permits the user to monitor the EIA RS-232 signals and isolate and identify sources of trouble.

The EIA Interface Test Set contains nine indicators which continuously monitor the level of the following interface signals: transmitted data, received data, request to send, clear to send, data set ready, received carrier detect, data terminal ready, signal quality detect and ring indicator. Two indicators monitor the transmit and receive clock signals. Unlike the nine levels indicators, these two indicators will not respond when only a DC level is present. The clock interface signal indicators will only turn on when there is an active clock signal present. Two additional uncommitted indicators are available for monitoring either positive or negative levels on any of the interface lines.

The Interface Test Set contains 24 switches which allow any of the interface signals except line one, (Frame Ground) to be interrupted. These switches are physically located in the center of the front panel and functionally divide the Test Set into two halves. The upper half contains a cable and connector for connecting the Test set to the DCE (data communications equipment) or modem. The indicators which monitor signals originating from the modem are also located on the upper half of the front panel. Likewise, the lower half of the Test Set contains a connector to which the DTE (Terminal or CPU) can be connected and the indicators which monitor signals originating from the DTE. The positive and negative test indicators are also located on the lower half of the Test Set. All indicators are labeled with both the standard EIA designation and the commonly used abbreviations.

Twenty five pins are located both above and below the switches. These pins permit monitoring of any of the interface lines with either or both the positive and negative test indicators with jumpers supplied or probing with an external meter or oscilloscope. Both sets of pins are arranged in the same configuration and order as the pins in a standard EIA RS-232 female connector.

The Interface Test Set is housed in a sturdy plastic case with aluminum extrusions and hinge. A positive latch is provided on the cover to keep the Test Set closed securely when not in use. The front panel is photographically etched and overcoated to prevent the lettering from being scratched or marred during use. The Test Set is self-contained and is powered by two penlite batteries which will provide over 100 hours of continuous operation. No power

is consumed by the Test Set when not in use.

EIA INTERFACE TEST SET SPECIFICATIONS

LEVEL INDICATORS	ACTIVITY INDICATORS .....Transmit Clock
Transmitted Data	Receive Clock
Received Data	INDICATOR THRESHOLD .....± 3 volts
Request to Send	
Clear to Send	INDICATOR INPUT IMPENDANCE.....30,000 ohms
Data Set Ready	
Received Carrier	POWER .....Two 1.5 volts
Detect	AA Batteries
Data Terminal Ready	
Signal Quality Detect	DIMENSIONS .....5.5"L x 3.6"W
	1.6"H
Ring Indicator	
Positive Test	
Negative Test	WEIGHT .....12 oz.

6.4 MODEM CONTROL SIGNALS CHECKOUT

If the modem is suspected of causing trouble, the following control signals can be checked using an oscilloscope or an EIA Interface Test Set which provides test points and LED's that indicate signal activity. The modem must be in the data mode when checking the control signals.

1) Position the 2228D TC Controller so that you have access to the signals used by the EIA Interface Test Set connector (25 pin Cannon connector) or use an EIA Interface Test Set. Signal pin numbers given below are in reference to 25 pin Cannon connector (refer to Appendix H).

2) Pins 1 and 7 are chassis and reference ground. Check for any noise on ground circuit.

3) Pin 2 TRANSMITTED DATA (TO data set).

Signals on this circuit are generated by data terminal equipment. Check to see if terminal is transmitting data when in transmit mode. The data terminal will not transmit data unless Clear-To-Send

signal is ON (+3V to +25v) on pin 5, Data Terminal Ready signal is ON (+3v to +25v) on pin 20 and Data Set Ready signal is ON (+3V to +25v) on pin 6.

4) Pin 3 RECEIVED DATA (FROM data set).

Signals on this circuit are generated by receiving data set in response to data signals received from a remote data set. This circuit is always held in the MARK state (-3v to -25v) when the Received Line Signal Detector (pin 8) is OFF (-3v to -25v).

5) Pin 4 REQUEST-TO-SEND (TO data set).

Data terminal presents ON signal (+3v to +25v) on this circuit when terminal intends to transmit data. After turning this signal ON, data terminal must wait for ON condition to Clear-To-Send (pin 5) circuit before starting data transmission.

6) Pin 5 CLEAR-TO-SEND (FROM data set).

Signal on this circuit is generated by data set to indicate whether or not data set is ready to transmit data. This circuit is turned ON (+3v to +25v) in response to ON signal on pin 4 (Clear-To-Send) delayed approximately 50 to 200 ms depending on type of modem and customer options selected.

7) Pin 6 DATA SET READY (FROM data set).

The ON condition (+3v to +25v) on this circuit indicates that data set is in DATA mode and is capable of receiving and transmitting data. The Data Terminal Ready signal on pin 20 must be ON (+3v to +25v) during DATA mode. The OFF condition (-3v to -25v) indicates that data set is Talk, Test, or On-Hook mode.

8) Pin 8 RECEIVED LINE SIGNAL DETECTOR (carrier) (FROM data set).

The ON condition (+3v to +25v) on this circuit indicates the presence of the data carrier signal above the receiver threshold for

at least 47 ±3 milliseconds. This circuit is ON during the receive mode and will turn OFF (-3v to -25v) and disable the receiver when data terminal is in the transmit mode or when Request-To-Send signal is turned ON.

9) Pin 15 TRANSMITTER SIGNAL ELEMENT TIMING (FROM data set).

The square wave signals on this circuit at 2000 HZ (for 2000 baud modem) or 2400 HZ (for 2400 baud modem) or 4800 HZ (for 4800 baud modem) are used to provide the data terminal equipment with signal element timing information for the transmitted data circuit. A timing signal will be present on this circuit in most cases when power is on in the data set.

10) Pin 17 RECEIVER SIGNAL ELEMENT TIMING (FROM data set).

The square wave signal on this circuit at 2000 HZ (2000 baud modem) or 2400 HZ (2400 baud modem) or 4800 HZ (4800 baud modem) rate is used to provide the data terminal equipment with receiver signal element timing information. The transition from ON to OFF normally indicates the center of each signal element on the received data circuit. A timing signal will be present on this circuit when CARRIER (pin 8) is ON for data sets 201A and 201C.

11) Pin 20 DATA TERMINAL READY (TO data set).

The data terminal must apply an ON condition (+3v to +25v) on this circuit at all times to go into the DATA mode. An OFF signal on this line will not allow data set to go in the data mode. An OFF signal on this line during data transmission/reception will make data set drop the communication line.

6.5 MODEM SELF TESTS

Several manufacturers including Bell Telephone have the self loopback test along with other tests built into their modem. Before calling the

Telephone company or manufacturer, please use these self tests. Test procedures are always given in the modem operating manual. The Bell 201C and 208B data sets which have self tests and instructions to run them are given below.

6.5.1 DATA SET 201C SELF TESTS

6.5.1.1 BUTTONS ON THE DATA SET

Five buttons are located on the front panel of the data set. The functions of the buttons are as follows:

RO (Receive Only) - Used when testing the data set to condition it locally as a receiver.

AL (Analog Loopback) - Connects the output of the local transmitter to the input of the local receiver.

ST (Self Test) - When depressed this button causes the data set transmitter to turn on and transmit fixed pattern.

RT (Remote Test) - When depressed, this button conditions the data set to be tested remotely from a Telephone Company Data Test Center.

DL (Digital Loopback) - This button allows for digital loopback test on a 4 wire data set.

6.5.1.2 STATUS LAMPS ON THE DATA SET

The data set is provided with eight status lamps. Each lamp lights a portion of the front panel which shows the name of the control lead being monitored. The lamps and their functions are as follows:

ON Lamp - This lights when the power cord is plugged into a 105- to 130-volt ac source.

TR (Terminal Ready) - This lamp monitors the status of the data terminal ready signal on the customer interface. When the lamp is lighted, the signal is in the on condition and tells the data set that the terminal is ready for data communication.

MR (Modem Ready) - This lamp monitors the status of the data set ready signal on the customer interface. When the lamp is lighted, the signal is in the on condition and the data set is ready for data communication.

RS (Request-to-Send) - This lamp indicates the status of the request-to-send signal on the customer interface or from the internal circuts which check the data set. When the lamp is lighted, the request-to-send signal is in the on condition and tells the data set to be conditioned to transmit data. In normal operation, when the CO lamp is on, the RS lamp will be off regardless of the status of the RS signal at the customer interface.

CS (Clear-to-Send) - This lamp monitors the status of the carrier on signal on the customer interface during both normal and test modes of operation. The lamp comes on when a signal is being received by the data set.

CO (Carrier On) - This lamp monitors the status of the carrier on signal on the customer interface during both normal and test modes of operation. The lamp comes on when a signal is being recieved by the data set.

MC (Modem Check) - The MC lamp indicates the absence of the receiver signal timing (pin 17) signal at the customer interface. In normal operation, the lamp will be ON when the CO lamp is OFF. It will be OFF when the CO lamp and interface signal CF (pin 8) are ON. When using the self-test feature, the MC lamp is ON whenever CO is OFF. However, when CO is ON during self-test, the MC flashes ON whenever an error occurs on the received data lead.

TM (Test Mode) - This lamp will light when the data set is placed in the test mode by use of the AL, ST, RT or DL test switches.

6.5.1.3 DATA SET TESTING

Perform an analog loop-back self-test with a data set at each end. If either set fails, replace it with one known to be operating properly.

If both data sets pass the analog loop-back self-test, perform the end-to-end self-test (2-wire sets).

6.5.1.4 ANALOG LOOP-BACK SELF TEST (2-WIRE OR 4-WIRE DATA SETS)

1. Depress the AL and ST switches.

   Requirement: All lamps except MC are lighted during a 30-second testing interval. If the MC lamp blinks or remains steadily ON, or if any of the other lamps are extinguished, the data set is defective and should be replaced.

2. Depress the RO switch.

   Requirement: RS and CS lamps extinguish. MC lamp lights. CO lamp extinguishes if data set optioned for switched carrier operation (option XA, XD, or XE).

3. Return the data set to normal operation by depressing the RO, ST and AL switches.
   Requirement: Switches return to the out position and TM lamp extinguishes.

6.5.1.5 END-TO-END SELF TEST (2-WIRE DATA SET)

1. Depress ST switch at both ends.

   Requirement: TM lamp lights.

2. Depress RO switch at receive ends.

3. Establish line connection.

   Requirement: At transmit end, all lamps are lighted except CO lamp. At receive end, all lamps are light except RS, CS, and MC lamps. If MC lamp blinks an average or more than twice per minute or remains steadily ON, the data set or telephone facility is the source of trouble.

4. Repeat the test in the opposite direction by releasing the RO switch at one end and depressing the RO switch at the other end.

5. Return to pretest mode by releasing the ST switches at both ends and releasing the RO switch at the receive end.

   Requirement: TM lamp extinguishes.

6.5.2 DATA SET 208B SELF TESTS

6.5.2.1 BUTTONS ON THE DATA SET

Six buttons are located on the front panel of the data set. All of these except the LP button are push-to-operate, push-to-release type. The functions of the buttons are as follows:

LP (Lamp Test) - When depressed, this button causes all lamps to light except the ON lamp.* This button is used to determine if all the status lamps are functional. Its use does not affect other data set operations.

* The ON lamp is normally lighted when power is applied.

AL (Analog Loopback) - Connects the output of the local transmitter to the input of the local receiver. Depressing the AL button prevents the data set from entering the data mode from the talk mode or upon automatic answer. While the talk mode is not inhibited and

calls can be made with the telephone set, any attempt to transfer to the data mode will result in the line being disconnected if the AL button is depressed.

ST (Self Test) - When depressed, this button causes the data set transmitter to turn on and transmit a fixed pattern. The receiver is conditioned to look for this pattern and generate a signal whichcauses the ER lamp to flash if an error is detected.

RO (Receive Only) - Used when testing the data set to condition it locally as a receiver. When depressed, the switch internally conditions the request-to-send signal to off regardless of the state of the request-to-send signal from the terminal equipment or from other test buttons.

RT (Remote Test) - When depressed, this button conditions the data set to be tested remotely from a Telephone Company Data Test Center (DTC).

50 Button - When depressed, this button provides a request-to-send/-clear-to-send interval of 50 millisecond (ms). When the button is released, the request-to-send/clear-to-send interval is 150-ms. In almost all cases, the 50-ms request-to-send/clear-to-send interval can be used (button depressed). The 150-ms request-to-send/clear-to-send interval (button released) is provided to assure terminal compatibility and for applications where the channel delay exceeds the length of the transmitted signal. If the terminal equipment experiences frequence time-outs, the 150-ms request-to send/clear-to send interval might correct the condition.

6.5.2.2 STATUS LAMPS ON THE DATA SET

The data set is provided with seven status lamps. Each lamp lights a portion of the front panel which shows the name of the control lead being monitored. The lamps and their functions are as follows:

ON Lamp - This lights when the power cord is plugged into a 105- to 130-volt ac source.

TR (Terminal Ready) - This lamp monitors the status of the data terminal ready signal on the customer interface. When the lamp is lighted, the signal is in the ON condition and tells the data set that the terminal is ready for data communication.

MR (Modem Ready) - This lamp monitors the status of the data set ready signal on the customer interface. When the lamp is lighted, the signal is in the ON condition and the data setis ready for data communication.

RS (Request-to-Send) - This lamp indicates the status of the request-to-send on the customer interface or from the internal circuits which check the data set. When the lamp is lighted, the request-to-send signal is in the on condition and tells the data set to be conditioned to transmit data. In normal operation, when the CO lamp is on, the RS lamp will be off regardless of the status of the RS signal at the customer interface.

CS (Clear-to-Send) - This lamp monitors the status of the clear-to-send signal on the customer interface during both the normal and test modes of operation. When the lamp is lighted, the signal is in the on condition and the data set is ready to transmit data.

CO (Carrier ON) - This lamp monitors the status of the carrier on signal on the customer interface during both normal and test modes of operation. The lamp comes on when a signal is being received by the data set.

ER (Equalizer Retrain) - This lamp monitors the status of the automatic retrain mode. If the CO lamp is lighted and the ER indicator is blinking, it indicates that invalid data has been received and that the automatic equalizer is now retraining. Continuous blinking, while the CO lamp is on, is an indication of marginal performance. When the data set is in the ST mode, the ER lamp blinks when an error is detected in received data. For normal operation, when the CO lamp is off, the ER lamp should be lighted

and, when the CO lamp is lighted, the ER lamp should be off. Thus, CO and ER lamps light alternately in normal operation. A lighted ER lamp indicates an abnormal condition only when the CO lamp is also lighted.

6.5.2.3 DATAPHONE TESTING

In cases of suspected trouble, the attendant should perform the Lamp Check, the Analog Loopback Test, test the data terminal equipment, and perform and End-to-End Self Test before calling the Telephone Company to report trouble. Only if these checks indicate trouble in Telephone Company provided equipment should the problem be reported to the Telephone Company.

In addition to the following tests, the Telephone Company Test Center personnel may request further assistance in trouble isolation by use of built-in features.

6.5.2.4 LAMP TEST

Depress the LP nonlocking button. All the lamps on the data set should be lighted. The LP can be depressed at any time since it does not affect normal data set operation.

6.5.2.5 ANALOG LOOPBACK SELF TEST

The Analog Loopback Self Test is performed to analyze the data set without using external equipment. The test is performed as follows:

Check that the data set is idle and that power is applied.

1. Depress AL button.

2. Depress ST button.

Check that the ON, RS, CS and CO lamps are on and that ER and MR lamps are off. Disregard the status of the TR lamp. If the lamps are not as indicated, the data set has failed the Analog Loopback Self Test.

3. Observe the ER lamp for 30 seconds.

If the ER lamp is on or blinks, this indicates that the data set has failed the Analog Loopback Self Test.

At the end of the test:

4. Depress the AL and ST buttons.

The data set is returned to the normal operating condition.

NOTE:

The data set power supply is equipped with an over-voltage protection circuit which limits the output voltage as it rises excessively. If this occurs, the data set will fail the Analog Loopback Self Test. To reset the power supply, the power cord must be unplugged and replugged into the ac outlet. If the data set still fails the Analog Loopback Self Test, notify the Telephone Company Repair Service for correction of the problem.

6.5.2.6 END-TO-END SELF TEST

The End-to-End Self Test is performed to test both far-end and near-end data sets and the telphone channel between the two sets. The test is performed as follows:

1. Place a call to the far end and arrange to perform the End-to-End Self Test. Discuss the duration of the test (at least 5 minutes) and when to return to the talk mode.

Request the far end to check the following lamps after the far-end data set has been transferred to the data mode. (ON, RS, CS, and ER lamps are on;

MR and CO lamps are off; disregard status of TR lamp.) If the lamps are not as indicated, the system has failed the End-to-End Self Test.

2. Request the far end to depress the ST buttom on the data set and the DATA button on the telephone set.

The far-end data set is now transferred to the data mode.

3. Depress the ST and RO buttons on your data set and then depress the DATA button on the telephone set.

Your data is now transfered to the data mode and it is possible to recieve data.

Check that the ON and CO lamps are on at your data set and that the RS, CS, MR, and ER lamps are off. Disregard status of the TR lamp. If the lamps are not as indicated after transferring to the data mode, the system has failed the End-to-End Self Test.

Observe the ER lamp for a 5-minute period. The ER lamp should be off and should not blink more than an average of three times in any 1-minute period.

4. After the prearrange time, return to the talk mode and discuss the results of the test.

5. Repeat the test in the opposite direction by releasing the RO button on your data set. Request the far end to depress the RO button on that set.

Request the far end to check the following lamps after both data sets have been transferred to the data mode. (ON and CO lamps are on; RS, CS, MR, and ER lamps are off; disregard status on TR lamp.) If the lamps are not as indicated, the system has failed the End-to-End Self Test.

6. Return both data sets to data mode by depressing DATA buttons on the telephone sets at both locations.

Check that the ON, RS, CS, and ER lamps are on at your data set and that the MR and CO lamps are off. Disregard status of TR lamp. After transferring to the data mode, if the lamps are not as indicated, the system has failed the End-to-End Self Test.

7. Repeat the 5-minute check for this direction of transmission; then return to talk mode.

After the 5-minute check has been performed and the results have been discussed, return the data sets to normal operation as follows:

8. Release the ST button at your data set.

Data set is returned to normal operation.

9. Request the far end to release the ST and RO buttons.

Far-end data set is returned to normal operation.

NOTE:
If tests fail, make another attempt before reporting trouble by establish;ng a new connection.

6.6 2228D DIAGNOSTICS/TESTS

6.6.1 2228D Power-Up Diagnostics

Upon Powering-Up, the 2228D Microprocessor will run the 2228D TC Controller Power-Up Diagnostics (resident in the 2228D PROM). This takes 10 to 15 seconds, after this time the LED located on the mounting bracket, will give an ON, OFF or FLASHING indication (refer to section 5.2 for an explanation of these indications).

The following is a list of the tests that are performed by the 2228D TC Controller during the Power-Up Diagnostics. For an explanation of each test refer to Appendix F.

POWER-UP TESTS

1. Z80 Power Up
2. Prom Checksum Test
3. PIO Power UP
4. Write Bad Parity/Parity Generator Test
5. Bank Decoder Test
6. 62K Ram Marching AA and 55 Test
7. DMA 9517 Power Up
8. DMA 9517 Current and Word Count Registers Tests
9. CTC Power Up
10. CTC Channel Interrupt Test
11. SIO Bisync Internal Test*

*NOTE

When performing the RS-232-C Loopback Test (refer to section 6.6.2) the SIO Bisync External Test will run in addition to the SIO Bisync Internal Test

6.6.2 RS-232-C Loopback Test

Once the RS-232-C Loopback plug is installed into the RS-232-C connector the RS-232-C Loopback Test can be performed. This test is only performed during initial installation. It includes all the tests performed during the 2228D Power-Up Diagnostics with the addition of the SIO Bisync External Test (refer to section 6.6.1 for a listing of these tests).

To perform the Loopback Test simply turn the CPU ac power switch ON, the test will run automatically, taking 10 to 15 seconds. Once the test is completed the LED (see Figure 1) will indicate the condition of the board. Failures results in either the LED remaining ON solid or FLASHING, if the LED is FLASHING this indicates a reportable failure. If the LED is ON solid this indicates a catastrophic failure has been detected with no reporting

capabilities. Once the board has passed perform the installation procedure located in section 4.2.

6.6.3 POWER-UP ERROR CODE INTERPRETER

6.6.3.1 INTRODUCTION

The 2228D Power Up Error Code Interpreter, will interpret the error codes supplied by the 2228D TC Controller Power-Up Diagnostic Program. The Diagnostic program is resident in the 2716 prom, located in position L44, on the 2228D TC Daughter Board.

NOTE

The Power-Up Error Code Interpreter program is used only if the LED is FLASHING (reportable failure)

6.6.3.2 PROGRAM DESCRIPTION

The Power-Up Error Code Interpreter program is designed to test the LSI circuitry needed for overall TC board operation. It will also aid in troubleshooting hardware faults. The following routines are performed by this program:

1. Request device address for 2228D TC Controller.
2. Request error code from 2228D TC Controller.
3. Interpret error code and display appropriate information.

6.6.3.3 OPERATION

To run the 2228D Power-up Error Code Interpretor Program perform the following Program Loading Procedure in sequential order.

6.6.3.4 PROGRAM LOADING PROCEDURE

NOTE

Use the Single Density Disk WLI #702-0068, Rev 1.0 for VP and MVP Mainframes or Double Density Disk WLI #732-0002, Rev 1.0 for SVP and LVP Mainframes

A. Load diskette into Floppy Disk
B. Select that Disk drive containing the diagnostic diskette using the SELECTS DISK statement.
C. Depress 'RETURN'
D. Depress 'LOAD'
F. Depress 'RUN'
G. Depress 'T' and enter in "28DEIRO"
H. Depress 'RETURN'
G. The CRT will display the screens needed to run the error code interpreter. All operations are screen prompted and require no detailed explanation.

6.6.3.5 SCREEN DISPLAYS AND DESCRIPTIONS

A. ADDRESS ENTRY ROUTINE AND SCREEN DISPLAY

This routine requests the user to enter one of two hex addresses for the TC board--01C or 01F. No other addresses will be accepted.

Screen display:

```
PLEASE ENTER THE CORRECT ADDRESS (01C OR 01F) FOR THIS CONTROLLER
WHAT IS THE ADDRESS OF THIS CONTROLLER? ___

KEY RETURN TO CONTINUE

ADDRESS IS NOT WITHIN SPECIFIED RANGE
LINE 3: Will be visible upon entry of incorrect address.
```

B. PROGRAM IDENIFICATION

This routine is entered after the correct address has been entered and the operator has keyed RETURN to continue. This routine identifies the program that is about to be used by the operator and requests a RETURN entry to continue.

Screen Display:

```
ERROR CODE INTERPRETER FOR THE 2228D POWER UP DIAGNOSTIC

KEY RETURN TO CONTINUE
```

C. SELECTING DEVICE ADDRESS

This routine selects the device address entered during the first screen display. It reports to the user whether the device is ready or busy. Key RETURN to continue.

Screen Display:

```
SELECTING DEVICE ADDRESS 01C

DEVICE IS ! READY !

KEY RETURN TO CONTINUE
```

D. ERROR STATUS REQUEST

This routine is entered from the Key RETURN of the previous screen. During this routine, an interim screen is displayed while the 2200 requests the error code from the 2228D; the error code is then used to find the appropriate screen display for the operator.

Screen Display:

```
REQUESTING STATUS WORD FROM 2228D CONTROLLER
```

The Remaining Routines Are Screen Displays Of The Error Code Interpreter

ERROR CODE 01: REPLACE PCB WLI #210-7659

Screen display:

```
WRITE BAD PARITY/PARITY GENERATOR TEST ERROR
ERROR CODE RECEIVED = 01

KEY RETURN TO TEST PIO & 2200 OB'S AND IB'S
```

NOTE

Refer to section C (Page 6-27) for PIO & 2200 OB'S and IB'S screen display

ERROR CODE 02: REPLACE PCB WLI #210-7659

```
BANK DECODER TEST ERROR
ERROR CODE RECEIVED = 02

KEY RETURN TO TEST PIO & 2200 OB'S AND IB'S
```

ERROR CODE 03: REPLACE BAD 4116 RAM CHIPS (16K X 1) WLI #377-0345, LOCATED ON TC CONTROLLER DAUGHTERBOARD (WLI #210-7659).

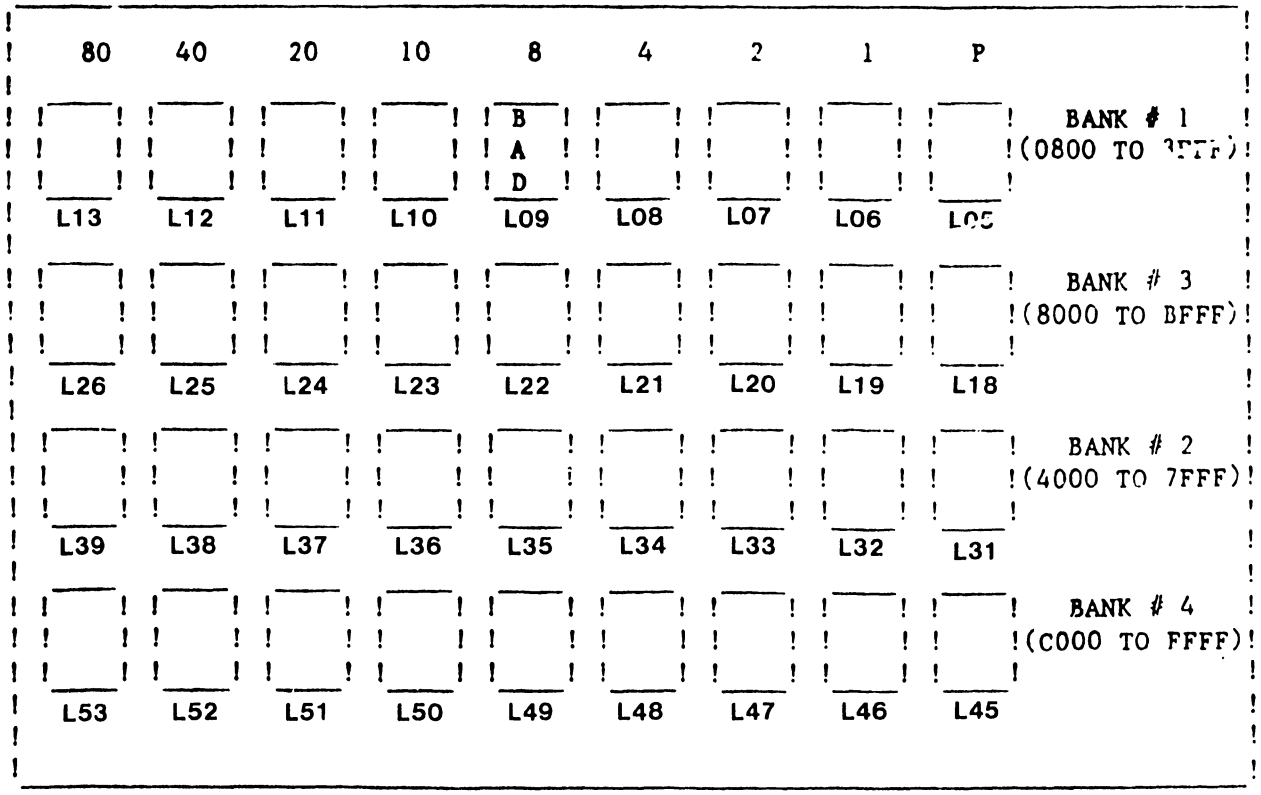
This is the Ram Data Error, and the controller can supply additional information for screening. Upon detection of this error code, the program enters an additional request routine to get more pertinent information from the controller.

Screen display:

```
                    ! MEMORY ERROR !

          FAILING MEMORY ADDRESS = !            !

          EXPECTED DATA = !      !        ACTUAL DATA = !      !

LINES 2 AND 3 MAY BE REPEATED TWO ADDITIONAL TIMES IF THE CONTROLLER
GIVES ERROR INFORMATION FOR THESE POSITIONS.

          KEY RETURN FOR BOARD DISPLAY OF ERROR
```

SCREEN DISPLAY OF BOARD IS A GRAPHIC RAM CHIP LAY OUT WITH THE BAD RAM OR RAMS POSITIONS IDENTIFIED.

Screen display:



ERROR CODE 04: REPLACE PCB WLI #210-7659

Screen display:

```
CONTROLLER FAILED DMA POWER UP TEST
ERROR CODE RECEIVED = 04

KEY RETURN TO TEST PIO & 2200 OB'S AND IB'S
```

ERROR CODE 05: REPLACE PCB WLI #210-7659

Screen display:

```
CONTROLLER FAILED DMA CURRENT AND WORD COUNT REGISTER TEST
ERROR CODE RECEIVE = 05

KEY RETURN TO TEST PIO & 2200 OB'S AND IB'S
```

ERROR CODE 06: REPLACE PCB WLI #210-7658

Screen display:

```
CONTROLLER FAILED CTC GO/NO GO POWER UP TEST
ERROR CODE RECEIVE = 06

KEY RETURN TO TEST PIO & 2200 OB'S AND IB'S
```

ERROR CODE 07: REPLACE PCB WLI #210-7658

Screen display:

```
CONTROLLER FAILED CTC CHANNEL INTERRUPT TEST
ERROR CODE RECEIVED = 07

KEY RETURN TO TEST PIO & 2200 OB'S AND IB'S
```

ERROR CODE 10: REPLACE PCB WLI #210-7658

Screen display:

```
CONTROLLER FAILED SIO BISYNC EXTERNAL LOOP BACK TRANSMIT/RECEIVE TEST
ERROR CODE RECEIVE = 10

KEY RETURN TO TEST PIO & 2200 OB'S AND IB'S
```

ERROR CODE 11: REPLACE PCB WLI #210-7658

Screen display:

```
CONTROLLER FAILED SIO BISYNC LOOP BACK TRANSMIT/RECEIVE TEST
ERROR CODE RECEIVE = 11

KEY RETURN TO TEST PIO & 2200 OB'S AND IB'S
```

ERROR CODE 08: REPLACE PCB WLI #210-7659

Screen display:

```
NMI OCCURRED DURING POWER UP DIAGNOSTIC
ON A TEST OTHER THAN PARITY, BANK DECODER, OR MARCHING RAM TEST
ERROR CODE RECEIVED = 08

KEY RETURN TO TEST PIO & 2200 OB'S AND IB'S
```

ERROR CODE 09: REPLACE PCB WLI #210-7659

Screen display:

```
NMI OCCURRED DURING NORMAL OPERATION FROM BOOTSTRAP
ALL POWER UP DIAGNOSTICS PASSED UPON RETRY
ERROR CODE RECEIVE = 09

KEY RETURN TO TEST PIO & 2200 OB'S AND IB'S
```

ADDITIONAL SCREENS

A. Invalid Status Screen

NOTE

When the following is displayed replace the 2228D Controller.

Screen display:

```
INVALID STATUS ERROR CODE RECEIVED FROM CONTROLLER
ERROR CODE RECEIVE = XX

KEY RETURN TO TEST PIO & 2200 OB'S AND IB'S
```

B. Screen display

```
UNABLE TO COMMUNICATE WITH CONTROLLER
```

NOTE

If the above screen appears,
take the following actions:

1. Re-load program (section 6.6.3.3 of the power-up diagnostics).
2. If screen re-appears, replace 2228D controller.

C. PIO & 2200 OB'S / IB'S ROUTINE

Screen display:

```
INPUT THE HEX CHARACTER TO BE TRANSMITTED XX

RECEIVED BYTE XX

KEY RETURN TO CONTINUE
```

NOTE:

When using the OB's/IB's test above, do not use a HEX 'FF'. This code will be used for further testing of the controller using another diagnostic package. At present, the results will be one of two possibilities. If error codes 01, 02, or 03 exist, then the previous pattern entered will be returned and the controller will remain in the error-reporting routine. This board is considered untestable until the present memory problem is corrected. If any error code other than the ones mentioned above exists, the result will be a return of the previous pattern entered. The controller will go to the Bootstrap Firmware Program to enable additional microcode diagnostic to be entered via another diagnostic package.

6.6.4 SYSTEM LEVEL DIAGNOSTICS

6.6.4.1 INTRODUCTION

The 2228D System Level Diagnostic is designed so that the controller can be continuously tested automatically. This will aid the Service Representative in troubleshooting intermittant faults. There are nine other tests that will test the LSI circuitry needed for overall TC board operation

6.6.4.2 PROGRAM DESCRIPTION

The System Level Diagnostic Program handles all screening, test control, and error reporting.

Upon entering the System Level Diagnostics Program the operator will be instructed to indicate the condition of the controller. If the LED is ON or Flashing the operator will answer "N". The next question will appear which asks the operator if the LED is Flashing. If the operator answers "N", indicating the LED is ON solid an error screen will be displayed and no further testing will take place.

If the answer is "Y", indicating the LED is Flashing the monitor will check the controller's power-up diagnostic error reporting routine for the error that was detected. If a RAM failure or some type exists an error screen will be displayed and no further testing will take place.

If any other type of error exists, the controller will be forced into the operating system firmware portion of the PROM and the communications test will be invoked.

Below is a procedure (section 6.6.4.3) for loading the System Level Diagnostic Program, followed by display screens that are encountered when using this diagnostic. Each display screen is preceded by a description of

that particular screen.

NOTE:

If the communications test is invoked after determining no RAM error exist, the LED may remain ON or OFF, ignore this condition.

6.6.4.3 OPERATION

To run the System Level Diagnostics perform the following program loading procedure in sequential order.

NOTE

The System Level Diagnostic Program is stored on the 702-0097 Floppy Diskette under file names 28DFSR1 and FSDIAGS respectively

6.6.4.4 PROGRAM LOADING PROCEDURE

A. Load the diskette into the floppy drive
B. Select that disk drive containing the diagnostic diskette using the SELECT DISK statement
C. depress 'RETURN'
D. depress 'LOAD'
E. depress 'RUN'
F. depress "28DFSR1"
G. depress 'RETURN'
H. The CRT will display the appropriate routines for system level diagnostics. All operating instructions are screen prompted and require no detailed explanation.

6.6.4.5 SCREEN DISPLAYS AND DESCRIPTIONS

A. WARNING SCREEN

This is a warning screen identifying the intended use of this diagnostic.

Screen display:

```
WARNING FIELD SERVICE DIAGNOSTIC FOR 2228 REV 1 ONLY

KEY 'RETURN' TO CONTINUE
```

B. DEVICE ADDRESS SELECTION

This screen requests the operator to input the correct device hex address for the controller, 01C or 01F (located on the motherboard WLI #210-7658-A) . After the operator keys RETURN the Monitor program checks the device for a Ready/Busy condition. The result is displayed to the operator.

Screen display:

```
                2228D TC FIELD SERVICE DIAGNOSTICS REV 1.0

    Available device addresses are:          Requires MVP BASIC Revision 1.9

                                  01C     01F

What is the device address ? 01C

(depress RETURN for Ready condition)

                                DEVICE IS READY

                              KEY 'RETURN' TO CONTINUE
```

NOTE:

A busy response indicates either the device address is wrong or the controller will be unable to respond to any future requests from the Monitor program.

C. CONTROLLER CONDITION REQUEST

This screen requests the operator to input the condition of the controller. The LED which is located on the mounting bracket (see Figure 1), will indicate what condition the controller is in by remaining ON, OFF or by FLASHING. These indications are explained in section 5.2. If the LED is OFF the operator answers "Y". The monitor will immediately enter a communications test between the controller and the 2200.

Screen display:

```
Device address '01C' will be used for all tests

Is the LED OFF ? 'Y' or 'N'*Y
```

depress RETURN to continue

NOTE:

The communications test is only run upon initial entry of this diagnostic or upon a re-start request by the operator from the menu. If the LED is ON or FLASHING the operator will answer "N", the monitor will immediatly ask if the LED is flashing? An "N" response is used if the LED remains ON and a "Y" if the LED is flashing. The following screen displays will appear with the following responses.

The diagnostics will enter the AUTOMATIC TESTS (refer to the AUTOMATIC TESTS on page 6-35) by answering "Y" to the question "Is the LED OFF ?" and depressing RETURN.

D. LED ON INDICATION (error screen)

Screen display:

```
Device address'01C' will be used for all test

Is the LED OFF? 'Y' or 'N'   N

Is the LED FLASHING? 'Y' or 'N'   N

The controller has a non reportable failure you cannot use
this diagnostic or the Error Interpreter
```

NOTE:
If the LED remains ON (catastrophic failure), replace the 2228D TC Controller board.

E. LED FLASHING INDICATION (error screen)

Screen display:

```
Device address '01C' will be used for all test

Is the LED OFF? 'Y' or 'N'   N

Is the LED FLASHING? 'Y' or 'N'   Y

The power up diagnostic has detected a failure in one of the following tests
write bad parity/parity generator test/bank decoder test/marching AA/55 test.
This failure must be corrected before this diagnostic can be used.
```

NOTE:
If the LED is FLASHING (reportable failure) perform the Power-Up Error Code Interpreter in section 6.6.3.

AUTOMATIC TESTS

These two tests check the communications capability of the controller utilizing the firmware microcode portion of the PROM. These tests check the ability of the controller and 2200 to communicate utilizing the PIO and DMA chips.

The first communications test transfers a 256 byte incremental data pattern to the controller memory starting at address 0900. It then reads back and compares the data sent with the expected data. Successful functioning of this test will result in advancement to the next communications tests.

The second communications test is designed to check the high order address bit multiplexer for the DMA chip. A unique byte is placed in each of the memory locations shown below. Then each unique byte is read at the specific address and checked with the expected byte. Successful completion of this test will result in advancement to the parameter inputs by the operator and eventual loading of the microcode diagnostic program.

ADDRESS AND BYTE = 8000 (00), 8100 (01), 8200 (02), 8400 (04), 8800 (08)
9000 (10), A000 (20), C000 (40)

F. FIRST COMMUNICATIONS TEST

This screen displays the condition of the first communications test. Any errors will be reported on this screen and no error looping will be used. If a CPU Time Out error occurs, no further testing will take place. If a failure to get an IBS from the controller occurs, no further testing can take place. Both failures indicate a fault in either the DMA or PIO.

Screen display:

```
                    CHECKING DMA/PIO

SEND 256 BYTES OF DATA TO CONTROLLER MEMORY

READING & COMPARING 256 BYTES OF DATA FROM CONTROLLER MEMORY

DMA/PIO TEST PASSED
```

G. SECOND COMMUNICATIONS TEST

This screen displays the conditions of the second communications test. Any errors will be reported on this screen and error looping will be automatically invoked.

Screen display:

```
                    DMA MULTIPLEXER TEST

SENDING UNIQUE ADDRESS PATTERNS

READING AND COMPARING UNIQUE ADDRESS PATTERNS

DMA ADDRESS MULTIPLEXER TEST PASSED
```

H. INPUT PARAMETERS REQUEST

This screen requests testing parameter inputs from the operator. The parameters are Loop or Halt On Error, Display or no Display of instruction/information screens, and the number of passes each test is to make.

Screen display:

```
Device address '01C' will be used for all tests

Do you want to loop on error 'Y' or 'N' Y
(depress RETURN)
* The program will LOOP on error
Do you want to display instructions 'Y' or 'N' Y
(depress RETURN)
* Instructions will be displayed
How many passes do you wish to make (less than 10000)? 4
(depress RETURN)
* All tests will make 4 pass(es)

                        KEY 'RETURN' TO CONTINUE
```

I. MICROCODE TEST PROGRAM TRANSFER

This screen displays the conditions encountered by the controller after successful completion of the communications tests. It is at this time the microcode diagnostic program file is downline loaded from the disk to the controller memory, starting at location 0900.

NOTE:
This test is performed automatically upon entering the number of pass(es) and keying 'RETURN'

Screen display:

```
        SENDING MICROCODE TEST PROGRAMS TO CONTROLLER MEMORY

        TRANSFER OF MICROCODE SUCCESSFUL

        FORCING CONTROLLER INTO MICROCODE TEST PROGRAM
```

J. CONTROLLER TEST REQUEST

This is the menu screen which indicates that the microcode was successfully loaded into the controllers memory and that the controller has been sent to this program and is awaiting test requests from the monitor.

Screen display:

```
                        TEST SELECTION MENU

SF 0 - RE-KEY INPUT PARAMETERS
SF 1 - MOVING INVERSIONS MEMORY TEST
SF 2 - SIO EXTERNAL LOOP
SF 3 - SIO/DMA TEST
SF 4 - CONTROL CHARACTER RAM TEST
SF 5 - PRIORITY INTERRUPT TEST
SF 6 - RS449 LOOP BACK TEST
SF 7 - OPTION SWITCH TEST
SF 8 - CHAIN MODE
SF 9 - RESTART

STRIKE THE SPECIAL FUNCTION KEY ASSOCIATED WITH THE DESIRED TEST
WHICH TEST DO YOU DESIRE?
```

The remaining screens are test screens and are self-explanitory. Each test will provide the operator with error information indicating the cause of failure.

Each screen display is preceded by a brief description of each test that will or can be performed using this diagnostic. These tests are more exhaustive checks of the various capabilities of the controller not performed in the power-up diagnostic.

The remaining tests are invoked by the operator from the Test Selection Menu by depressing the appropriate SPECIAL FUNCTION (SF) KEY..
depress SF0

RE-KEY INPUT PARAMETERS

The Input Parameters Request screen is displayed as seen on page 6-37. This routine allows the operator to re-input the Loop On Error or Halt On Error, Instruction/Information Display, and Number of Passes parameters. After re-entry the microcode program is again downline loaded into controller memory.

depress SF1

MOVING INVERSIONS MEMORY TEST

This test program performs a more exhaustive RAM memory check using the moving inversions test procedure with a AA/55 test pattern.

NOTE:

If all banks are to be tested, the number of passes must be set to 4 and CHAIN MODE (SF8) requested. Otherwise, the test requests the bank in which you desire to test and will test only that bank for the number of passes requested during the input parameters screen.

NOTE:

If an error is detected which will display the address of failure and the expected and actual data patterns, and the data patterns are equal this indicates a Parity RAM failure has occurred.

First screen display:

```
                    MOVING INVERSIONS TEST


This test will run a more complete RAM check and is bank selective.  In the
Chain Mode bank selection will be an automatic function.


                    KEY 'RETURN' TO CONTINUE
```

Second screen display:

```
                    MOVING INVERSIONS TEST


          RAM MEMORY WILL ONLY BE TEST ON 1 BANK AT A TIME

               ENTER 1 FOR BANK 1 ADDRESS 2000 TO 3FFF
               ENTER 2 FOR BANK 2 ADDRESS 4000 TO 7FFF
               ENTER 3 FOR BANK 3 ADDRESS 8000 TO BFFF
               ENTER 4 FOR BANK 4 ADDRESS C000 TO FFFF

          ENTER THE NUMBER OF THE BANK YOU WISH TO TEST ? 4
```

depress RETURN

Third screen display:

PASS #1

MOVING INVERSIONS TEST

WAITING FOR CONTROLLER TO COMPLETE TESTS

CURRENTLY TESTING BANK #3

Fourth screen display:

PASS #1

MOVING INVERSIONS TEST

MOVING INVERSIONS TEST PASSED

CONTROLLER IS BACK IN HOST

depress SF2

SIO EXTERNAL LOOP

This test requires the RS-232-C Loopback plug be installed into the RS-232-C connector. The test runs a more extensive test of the SIO and associated circuitry utilizing Async, Bisync, and SDLC modes of operation. Error messages are more detailed than the one for the power-up diagnostic. No option switch setting is required.

First screen display:

```
                    SIO EXTERNAL LOOP

This program tests the controller's SIO external loop back circuitry.  The
tests are conducted in all 3 modes ie Async, Bisync and SDLC.  In addition 3
vectored interrupt tests are performed, Transmit, Receive, Overrun, CTS, & DCD.


                    KEY 'RETURN' TO CONTINUE
```

Second screen display:

```
PASS #1
                    SIO EXTERNAL LOOP


                    WAITING FOR CONTROLLER TO COMPLETE TESTS
```

Third screen display:

```
PASS #1
                    SIO EXTERNAL LOOP


                    SIO EXTERNAL LOOP PASSED

                    CONTROLLER IS BACK IN HOST
```

depress SF3

SIO/DMA TEST

Install the RS-232-C loopback plug into the RS-232-C connector to perform this test. The test performs an interaction check between the SIO, DMA, and CTC utilizing the Async mode of operation. Transfers of 256 bytes, 512 bytes 1K, 2K, 4K, 8K and 16K are performed with error checking after each transfer completion. A time out feature is also incorporated in case no transfer operation takes place as expected, indicating an SIO DMA problem exists.

First screen display:

```
                    SIO/DMA TEST

This test requires the RS232 LOOP BACK Plug. The test checks the ability to
transfer data from one section of memory to another. The test is run in the
Async mode.

This test checks transfers of 256 bytes, 512 bytes, 1k, 2k, 4k, 8k, and 16k.

                KEY 'RETURN' TO CONTINUE
```

Second screen display:

```
PASS #1
                    SIO/DMA TEST


            WAITING FOR CONTROLLER TO COMPLETE TESTS
```

Third screen display:

PASS #1

SIO/DMA TEST

SIO/DMA TEST PASSED

CONTROLLER IS BACK IN HOST

depress SF4

CONTROL CHARACTER RAM TEST

Install the RS-232-C Loopback plug into the RS-232-C connector to perform this test. The test operates in two modes. First the Control Character RAM is flooded not to recognize any characters. With the SIO and DMA (Receive channel only) activated 256 characters 00 to FF are transmitted and received. The CTC is monitored, as well as the DMA, checking each character that did not cause a downcount of CTC channel 0 after completion of each transfer. The Control Character RAM is then flooded to recognize all characters as control characters. The CTC channel 0 is monitored after each transfer to insure a downcount occurred indicating a control character was recognized.

First screen display:

```
                CONTROL CHARACTER RECOGNITION RAM TEST

This program checks the static ram using the SIO in Async mode.  The failing
character is interpreted as the RAM address.  INSTALL RS232 LOOP BACK.

                        KEY 'RETURN' TO CONTINUE
```

Second screen display:

```
PASS #1
                CONTROL CHARACTER RECOGNITION RAM TEST

                WAITING FOR CONTROLLER TO COMPLETE TESTS
```

Third screen display:

```
PASS #1
                CONTROL CHARACTER RECOGNITION RAM TEST

                        CHARACTER RAM TEST PASSED

                        CONTROLLER IS BACK IN HOST
```

depress SF5

PRIORITY INTERRUPT TEST

Connect the RS-232-C plug into the RS-232-C connector to perform this test. The test will check the IEI/IEO line connected between the SIO, CTC and PIO is functioning properly. It also insures the priority scheme with the SIO having the highest and the PIO the lowest is maintained.

First screen display:

```
                    PRIORITY INTERRUPT TEST

This test checks the IEI and IEO line between the SIO, CTC, and PIO
chips. The test insures that higher priority is observed. INSTALL
RS232 LOOP BACK.

                    KEY 'RETURN' TO CONTINUE
```

Second screen display:

```
PASS #1
                    PRIORITY INTERRUPT TEST

                    WAITING FOR CONTROLLER TO COMPLETE TESTS
```

Third screen display:

```
PASS #1

                    PRIORITY INTERRUPT TEST



                PRIORITY INTERRUPT TEST PASSED

                CONTROLLER IS BACK IN HOST
```

depress SF6

RS449 LOOP BACK TEST

The RS-449-C Loopback plug (wiring diagram is located in Appendix E) must be connected into the RS-449-C connector for this test, also the Modem Interface Toggle Switch on the rail must be in the RS449 position. The tests performed are the same as those performed by the SIO EXTERNAL LOOP Test.

First screen display:

```
                    RS449 LOOP BACK

This program tests the controller's SIO external loop back circuitry for
the RS449 plug.  The RS449 LOOP BACK must be INSTALL and the Toggle
switch switched.  Testing is the same as for the SIO External Loop Test.

                KEY 'RETURN' TO CONTINUE
```

Second screen display:

```
PASS #1

                    RS449 LOOP BACK


              WAITING FOR CONTROLLER TO COMPLETE TESTS
```

Third screen display:

```
PASS #1

                    RS449 LOOP BACK


                  RS449 LOOP BACK PASSED


                CONTROLLER IS BACK IN HOST
```

depress SF7

OPTION SWITCH TEST

This test allows the operator to test SW2 on the controller motherboard (WLI #210-7658). After test entry the screen will display the current switch setting. The operator need only change the setting of the switch at will and the screen display will automatically reflect the new setting. To exit the test the operator must key RETURN.

First screen display:

```
                    OPTION SWITCH TEST

This program tests the user option switch on the mother board.  The user
sets the switch to the desired switch setting which will automatically
be updated on the screen.  To exit the routine the user must key RETURN.


                    KEY 'RETURN' TO CONTINUE
```

Second screen display:

```
                    OPTION SWITCH TEST

                    1  2  3  4  5  6  7  8
               0    0 ! 0 ! 0 ! 0 ! 0 ! 0 ! 0 ! 0
               N    F ! F ! F ! F ! F ! F ! F ! F
                    F ! F ! F ! F ! F ! F ! F ! F

                USER OPTION SWITCH (SW2)


                KEY RETURN TO EXIT TEST
```

Third screen display:

```
CONTROLLER RETURN TO HOST
```

CHAIN MODE

This test invokes the tests associated with Special Function Keys SF1, SF2, SF3, SF4 and SF5. This program will invoke each test one at a time for the number of passes entered during parameter entry. The bank number for the Moving Inversions Test will automatically be incremented. If a minimum of 4 passes is selected by the operator, each bank of memory will be tested once by Moving Inversions.

NOTE:

The asterisk designates those tests which are performed by the Chain Mode Test.

depress SF8

Screen display:

```
                    TEST SELECTION MENU

SF 0 - RE-KEY INPUT PARAMETERS
SF 1 - MOVING INVERSIONS MEMORY TEST *
SF 2 - SIO EXTERNAL LOOP *
SF 3 - SIO/DMA TEST *
SF 4 - CONTROL CHARACTER RAM TEST *
SF 5 - PRIORITY INTERRUPT TEST *
SF 6 - RS449 LOOP BACK TEST
SF 7 - OPTION SWITCH TEST
SF 8 - CHAIN MODE
SF 9 - RESTART

STRIKE THE SPECIAL FUNCTION KEY ASSOCIATED WITH THE DESIRED TEST
WHICH TEST DO YOU DESIRE?
```

NOTE:

The Test Selection Menu is automatically followed by the Chain Mode Test Routine

Screen display:

CHAIN MODE TEST ROUTINE

THIS TEST WILL CALL AND EXECUTE ALL MARKED (*) TEST
THE ENTIRE TEST WILL BE EXECUTED 4 TIME(S)

KEY 'RETURN' TO CONTINUE

NOTE:

Upon depressing 'RETURN' the Chain Mode Test will automatically perform the tests designated be the asterisk on the Test Selection Menu.

depress SF9

RESTART

This entry forces a software reset of the controller to location 0000 of the PROM. The Monitor program is also reset to the first screen of the System Level Diagnostics. Thus, returning the operator to the Warning Screen on page 6-31 of this document.

APPENDIX
A
REFERENCE
DOCUMENTATION

APPENDIX A

REFERENCE DOCUMENTATION

LVP Product Maintenance Manual	729-0602
VP Product Maintenance Manual	729-0583
MVP Product Maintenance Manual	729-0584
3271 Software Emulation Installation Manual	
Product Service Teleprocessing Guide	

For additional information refer to the the following Bell System technical reference publications.

Bell Pub. #40000	Technical Reference Catalog
Bell Pub. #40001	Technical Reference Ring Binder
Bell Pub. #41001	Complete Set Of Data Communication Technical References
Bell Pub. #41004	Data Communications Using Voiceband Private Line Channels
Bell Pub. #41005	Switched Telecommunications Network
Bell Pub. #41008	Affecting Voiceband Data Transmission--Description of Parameters
Bell Pub. #41009	Transmission Parameters Affecting Voiceband Data Transmission--Measuring Techniques
Bell Pub. #41021	Interface Specification
Bell Pub. #41101	Data Set 103A Interface Specification
Bell Pub. #41102	Data Set 103A3 Data Set 103E Data Set 103G Data Set 103H Interface Specification
Bell Pub. #41103	Data Set 103F Interface Specification
Bell Pub. #41105	113 Type Data Station Interface Specification
Bell Pub. #41201	Data Sets 201A and 201B
Bell Pub. #41202	Data Sets 202C and 202D Interface

	Specification
Bell Pub. #41209	Data Set 208A Interface Specification
Bell Pub. #41210	Data Set 201C Interface Specification
Bell Pub. #41211	Data Set 208B Interface Specification
Bell Pub. #41212	Data Sets 202S and 202T Interface Specification
Bell Pub. #41213	Data Set 209A Interface Specification
Bell Pub. #41214	Data Set 212A Interface Specification
Bell Pub. #41450	Data Service Unit Interface Specification
Bell Pub #41601	Data Auxiliary Set 801A (Automatic Calling Unit)
Bell Pub. #41602	Data Auxiliary Set 801C (Automatic Calling Unit)
Bell Pub. #41603	801C-L 1/2 Data Auxiliary Set Interface Specification
Bell Pub. #41802	Data Couplers CBS And CBT For Automatic Terminals

NOTE:

INQUIRIES RELATED TO THESE TECHNICAL REFERENCES SHOULD BE REFERRED IN WRITING TO:

AMERICAN TELEPHONE AND TELEGRAPH COMPANY
INFORMATION DISTRIBUTION CENTER, ROOM C190
ATTN: TECHNICAL REFERENCES
P.O. BOX 3513
NEW BRUNSWICK NEW JERSEY 08903

APPENDIX B

SCHEMATIC DRAWINGS

THE SCHEMATICS, WHEN AVAILABLE, ARE ON THE LAST FICHE IN THIS SET.

APPENDIX C

BILL OF MATER-IALS

ASSEMBLY PART NUMBER 177-2228-D - -
ASSEMBLY DESCRIPTION 2228D TC 27 & 3780/3270&75/X25/SDLC

LEGEND
1: P=PHANTOM; 2: ITEM MASTER DELY CODE; 3: *=TAGGED OUT OF KIT(PROD STR)

POSITION IN STRUCTURE	LEGEND 1 2 3	COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY	U/M	L/T
1	IN	210-7658-A - -	PCA 2228D TC CNTLR MB		1.0000	EACH	00010
2	IN	209-7658- - -	PCA 2228D TC CNTLR MB NC		1.0000	EACH	00010
3	IN	000-0001- - -	LABOR CIRCUIT SYSTEMS		1.5000		00000
3	IN	000-0011- - -	LABOR QUALITY CONTROL		.3000		00000
3	IN	300-1560- - -	CAP 560 PF 10% 500 V CERAMIC DISC		1.0000	EACH	
3	IN	300-1900- - -	CAP .05 UF +80-20% 12 V CERAMIC D	X13726	19.0000	EACH	00000
3	IN	300-1906- - -	CAP .001 UF 10% 500 V CERAMIC DISC		3.0000	EACH	
3	IN	300-1930- - -	.1 UF 50V +80-20% CERAMIC CAP(HIFRQ		4.0000	EACH	
3	IN	300-1931- - -	1 UF CERAMIC CAPACITOR(HIGH FREQ)		2.0000	EACH	
3	IN *	300-1966- - -	CAP .047 UF 50V+80-20% CERAMIC MLD	X13726	19.0000	EACH	
3	IN	300-4022- - -	CAP 15.0 UF 20 V 10% TANT AXIAL		1.0000	EACH	00001
4	FS	300-4022-R - -	CAP 15.0 UF 20V 10% TANT AXIAL T&R		1.0000	EACH	
3	IN	300-5005- - -	CAP 470 PF 5% 500 V MICA DIPPED		1.0000	EACH	
3	IN	321-0019- - -	CRYSTAL 12.24 5 % QUARTZ HC-18/U	E15282	1.0000	EACH	
3	IN	325-1503- - -	SWITCH SLIDE SPST 8 POS DIL		2.0000	EACH	
3	FS	330-2012-4B- -	RES 120 OHM 1/4W 10% FIXED COMP		2.0000	EACH	00001
4	FS *	330-2012- - -	RES 120 OHM 1/4W 10% FIXED COMP		1.0000	EACH	
3	FS	330-3010-4B- -	RES 1K OHM 1/4W 10% FIXED COMP		2.0000	EACH	00001
4	FS *	330-3010- - -	RES 1K OHM 1/4W 10% FIXED COMP		1.0000	EACH	
3	FS	330-3022-4B- -	RES 2.2K OHM 1/4W 10% FIXED COMP	E15643	4.0000	EACH	00001
4	FS *	330-3022- - -	RES 2.2K OHM 1/4W 10% FIXED COMP		1.0000	EACH	
3	FS	330-3047-4B- -	RES 4.7K OHM 1/4W 10% FIXED COMP		17.0000	EACH	00001
4	FS *	330-3047- - -	RES 4.7K OHM 1/4W 10% FIXED COMP		1.0000	EACH	
3	FS	330-4010-4B- -	RES 10K OHM 1/4W 10% FIXED COMP	E15643	7.0000	EACH	00001
4	FS *	330-4010- - -	RES 10K OHM 1/4W 10% FIXED COMP		1.0000	EACH	
3	FS	330-4033- - -	RES 33K OHM 1/4W 10% FIXED COMP		1.0000	EACH	
3	FS	330-6027-4B- -	RES 2.7M OHM 1/4W 10% FIXED COMP		2.0000	EACH	00001
4	FS *	330-6027- - -	RES 2.7M OHM 1/4W 10% FIXED COMP		1.0000	EACH	
3	IN	375-1012- - -	MPS 6512 SILICON TRANSISTOR		1.0000	EACH	
3	IN	375-1014- - -	MPS 5518 SILICON TRANSISTOR		1.0000	EACH	
3	IN	376-0068- - -	IC 7437N 4 2 IN POS NAND BUFFER		1.0000	EACH	
3	IN	376-0076- - -	IC 75150 2 LINE DRIVER		5.0000	EACH	
3	IN	376-0077- - -	IC 75154 4 LINE REC		4.0000	EACH	
3	IN	376-0104- - -	IC 9602 2 RETRIG RESET MONOSTBL MVB		1.0000	EACH	
3	IN	376-0148- - -	IC 74LS266 4 2 IN EXCL NOR GATE		2.0000	EACH	
3	IN	376-0153- - -	IC 74LS08 4 2 IN POS AND GATE		2.0000	EACH	
3	IN	376-0155- - -	IC 74LS74 2 D TYPE EDGE TRIG FF		4.0000	EACH	
3	IN	376-0159- - -	IC 74LS174 HEX D TYPE FLIP FLOP		1.0000	EACH	
3	IN	376-0180- - -	IC 74LS04 HEX INVERTER		3.0000	EACH	
3	IN	376-0193- - -	IC 74LS368 HEX BUS DRIVER 3 STATE		1.0000	EACH	
3	IN	376-0207- - -	IC 74LS00 4 2 IN POS NAND GATE		1.0000	EACH	
3	IN	376-0211- - -	IC 74LS32 4 2 IN POS OR GATE		3.0000	EACH	
3	IN	376-0216- - -	IC 74LS157 4 2-1 LINE DATA SELC MX		1.0000	EACH	
3	IN	376-0284- - -	IC 74LS241 OCT BUF&LINE DR W/TRI ST		1.0000	EACH	
3	IN	376-0294- - -	IC 74LS138 3-8 LINE DECODER/MPX		1.0000	EACH	

ASSEMBLY PART NUMBER 177-2228-D - -
ASSEMBLY DESCRIPTION 2228D TC 27 & 3780/3270&75/X25/SDLC

LEGEND
1: P=PHANTOM; 2: ITEM MASTER DELY CODE; 3: *=TAGGED OUT OF KIT(PROD STR)

POSITION IN STRUCTURE	LEGEND 1 2 3	COMPONENT PART NUMBER	DESCRIPTION	F C N	QUANTITY PER ASSY	U/M	L/T
3	IN	376-0297- - -	IC 74LS240 OCTAL BUF/LINE DR/LN REC		1.0000	EACH	
3	IN	376-0322- - -	IC 74LS14 LOW POWER SCHOTTKY		1.0000	EACH	
3	IN	376-0341- - -	IC NE556 DUAL TIMER		2.0000	EACH	
3	IN	376-0486- - -	IC 74LS125 QUAD BUS BUFF TRI-ST L P	E15643	2.0000	EACH	
3	IN	376-9011- - -	IC 40 PIN SOCKET BURNDY # DILBZ40P1		2.0000	EACH	
3	IN	376-9015- - -	IC 28 PIN SOCKET BURNDY		1.0000	EACH	
3	IN	380-1014- - -	DIODE 1N4148		1.0000	EACH	
3	IN	452-2095-05- -	FACE PLATE 2228D-TC (M) C06422-0375	E14956	1.0000	EACH	
3	IN	510-7558- - -	PCB 2228D TC CNTLR MB		1.0000	EACH	
3	FS	650-2102- - -	SCR 4-40 5/16 PAN SLOT MS NYL	E14956	2.0000	EACH	
3	FS	650-3080- - -	6-32 X 1/4 PAN HD PHL MS SS SEMS	E14956	2.0000	EACH	
2	IN	377-0371- - -	IC Z80 CTCA 28 PIN	E15282	1.0000	EACH	
2	IN	377-0373- - -	IC Z80 PIOA 140	E15282	1.0000	EACH	
2	IN	377-0393- - -	Z80A-SIO/2 SERIAL I/O 40 PIN 4MHZ	E15282	1.0000	EACH	
1	IN	210-7559-A - -	PCA 2228D TC CNTLR DB		1.0000	EACH	00010
2	IN	209-7659- - -	PCA 2228D TC CNTLR DB NC		1.0000	EACH	00010
3	IN	000-0001- - -	LABOR CIRCUIT SYSTEMS		2.0000		00000
3	IN	000-0011- - -	LABOR QUALITY CONTROL		.4000		00000
3	IN	300-1930- - -	.1 UF 50V +80-20% CERAMIC CAP(HIFRQ	PATREL	64.0000	EACH	
3	IN	300-1931- - -	1 UF CERAMIC CAPACITOR(HIGH FREQ)	PATREL	2.0000	EACH	
3	IN *	300-1966- - -	CAP .047 UF 50V+80-20% CERAMIC MLD	PATREL	8.0000	EACH	
3	IN	300-4014- - -	CAP 2.2 UF 20 V 10% TANT AXIAL	PATREL	4.0000	EACH	00001
4	FS	300-4014-R - -	CAP 2.2 UF 20V 10% TANT AXIAL T&R		1.0000	EACH	
3	IN	300-4056- - -	CAP 1.0 UF 10% 15V TANT	PATREL	4.0000	EACH	
3	FS	330-1033-4B- -	RES 33 OHM 1/4W 10% FIXED COMP		20.0000	EACH	00001
4	FS *	330-1033- - -	RES 33 OHM 1/4W 10% FIXED COMP		1.0000	EACH	
3	FS	330-3022-4B- -	RES 2.2K OHM 1/4W 10% FIXED COMP	E15733	3.0000	EACH	00001
4	FS *	330-3022- - -	RES 2.2K OHM 1/4W 10% FIXED COMP		1.0000	EACH	
3	FS	330-3047-4B- -	RES 4.7K OHM 1/4W 10% FIXED COMP	E15733	6.0000	EACH	00001
4	FS *	330-3047- - -	RES 4.7K OHM 1/4W 10% FIXED COMP		1.0000	EACH	
3	FS	330-4010-4B- -	RES 10K OHM 1/4W 10% FIXED COMP	E15283	11.0000	EACH	00001
4	FS *	330-4010- - -	RES 10K OHM 1/4W 10% FIXED COMP		1.0000	EACH	
3	IN	374-0002- - -	IC REG UA 7905 -5V TO-220		1.0000	EACH	
3	IN	376-0010- - -	IC 7404N HEX INVERTER		1.0000	EACH	
3	IN	376-0153- - -	IC 74LS08 4 2 IN POS AND GATE	E15283	2.0000	EACH	
3	IN	376-0155- - -	IC 74LS74 2 D TYPE EDGE TRIG FF	E15733	2.0000	EACH	
3	IN	376-0180- - -	IC 74LS04 HEX INVERTER		2.0000	EACH	
3	IN	376-0211- - -	IC 74LS32 4 2 IN POS OR GATE	E15733	3.0000	EACH	
3	IN	376-0221- - -	IC 74S194 4 BIT BI DIR UNIV SHIFT	PATREL	1.0000	EACH	
3	IN	376-0226- - -	IC 74LS139 2 2-4 LINE DECODE	PATREL	1.0000	EACH	
3	IN	376-0242- - -	IC 74LS280 9 BIT ODD EVEN PARITY GN		1.0000	EACH	
3	IN	376-0284- - -	IC 74LS241 OCT BUF&LINE DR W/TRI ST		2.0000	EACH	
3	IN	376-0310- - -	IC 74LS373 OCTL D-TYP LATCHES SCHTT		1.0000	EACH	
3	IN	376-0312- - -	IC 74LS75 4-BIT BISTABLE LATCH	PATREL	2.0000	EACH	
3	IN	376-0486- - -	IC 74LS125 QUAD BUS BUFF TRI-ST L P	E15733	1.0000	EACH	

ASSEMBLY PART NUMBER 177-2228-D - -
ASSEMBLY DESCRIPTION 2228D TC 27 & 3780/3270&75/X25/SDLC

LEGEND
1: P=PHANTOM; 2: ITEM MASTER DELY CODE; 3: *=TAGGED OUT OF KIT(PROD STR)

POSITION IN STRUCTURE	LEGEND 1	2	3	COMPONENT PART NUMBER	DESCRIPTION	F C N	QUANTITY PER ASSY	U/M	L/T
3		IN		376-9002- - -	IC 16 PIN SOCKET BURNDY		36.0000	EACH	
3		IN		376-9003- - -	IC 24 PIN SOCKET BURNDY		1.0000	EACH	
3		IN		376-9011- - -	IC 40 PIN SOCKET BURNDY # DILBZ40P1		2.0000	EACH	
3		IN		510-7659- - -	PCB 2228D TC CNTLR DB		1.0000	EACH	
2		IN		377-0344- - -	Z80 CPU 40 PIN I.C.		1.0000	EACH	
2		IN		377-0345- - -	16K BY 1 BIT DYNAMIC RAM		36.0000	EACH	
2		FS		377-0348- - -	TMS 2716 2K BY 8 BIT E PROM		1.0000	EACH	
2		IN		377-0363- - -	2102-A2 1K BY 1 BIT STATIC RAM 250N	E15283	1.0000	EACH	
2		IN		377-0388- - -	IC A99517A1PC DIRECT MEMORY ACCESS	E15283	1.0000	EACH	
1		IN		220-0113- - -	2200 TC CABLE C6482-5		1.0000	EACH	
2		IN		000-9999- - -	OTHER DIRECT COST		18.8980	EACH	00000
2		IN		350-1030- - -	DB-25P CH CONN 6000 SERIES		2.0000	EACH	
2		IN		350-4215- - -	DB51226-1 CONN HOOD FAST		2.0000	EACH	
2		FS		420-0053- - -	24 COND 26 GA SHIELDED CABLE	EC8399	12.2500	FEET	
2		IN		458-0361- - -	GROUND STRAP C5815-28	EC6407	2.0000	EACH	
2		FS		605-0002- - -	TUBING #15 CLEAR	EC8399	1.0000	FEET	
2		FS		605-0123- - -	SHRINK TUBING TYPE RNF 3/16 ID BLK	E8583A	.0800	FEET	
2		FS		605-0143- - -	TUBING 1/2" HEATSHRINK PVC BLACK	E10230	.4200	FEET	
2		FS		606-0113- - -	CBL MARKER WH/BK 2200TC 220-0113	EC9129	1.0000	EACH	00001
3		FS		605-0138- - -	TUBING 3/8 WH SHRINK POLYOLEFIN		.1140	FEET	
2		IN		685-0099- - -	BUBBLE BAG (AIRCAP) 4X5 1/2	EC9254	2.0000	EACH	

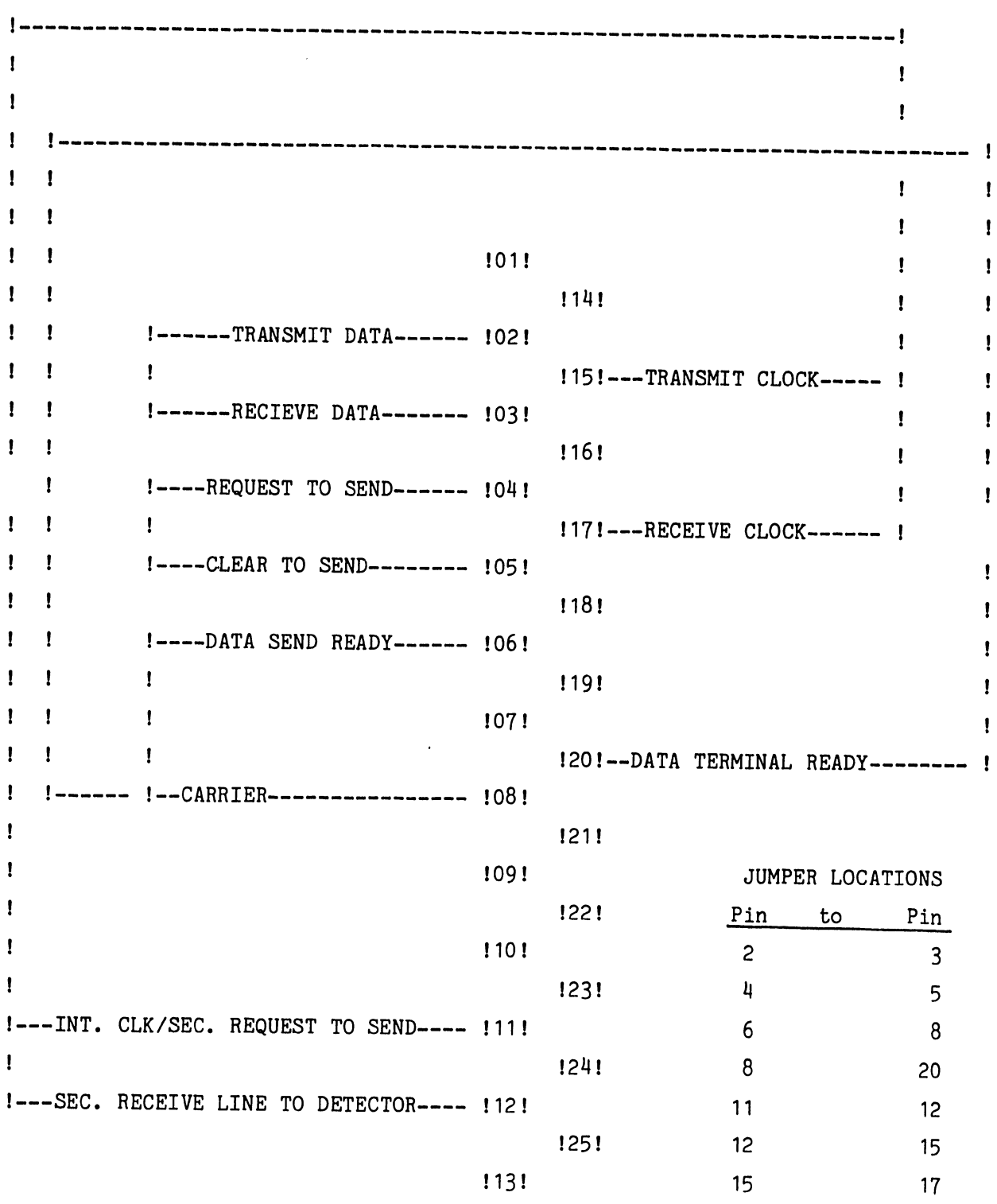
END OF REPORT MB0080-A

APPENDIX D

APPENDIX D

RS232 LOOP BACK CONNECTOR

WIRING DIAGRAM



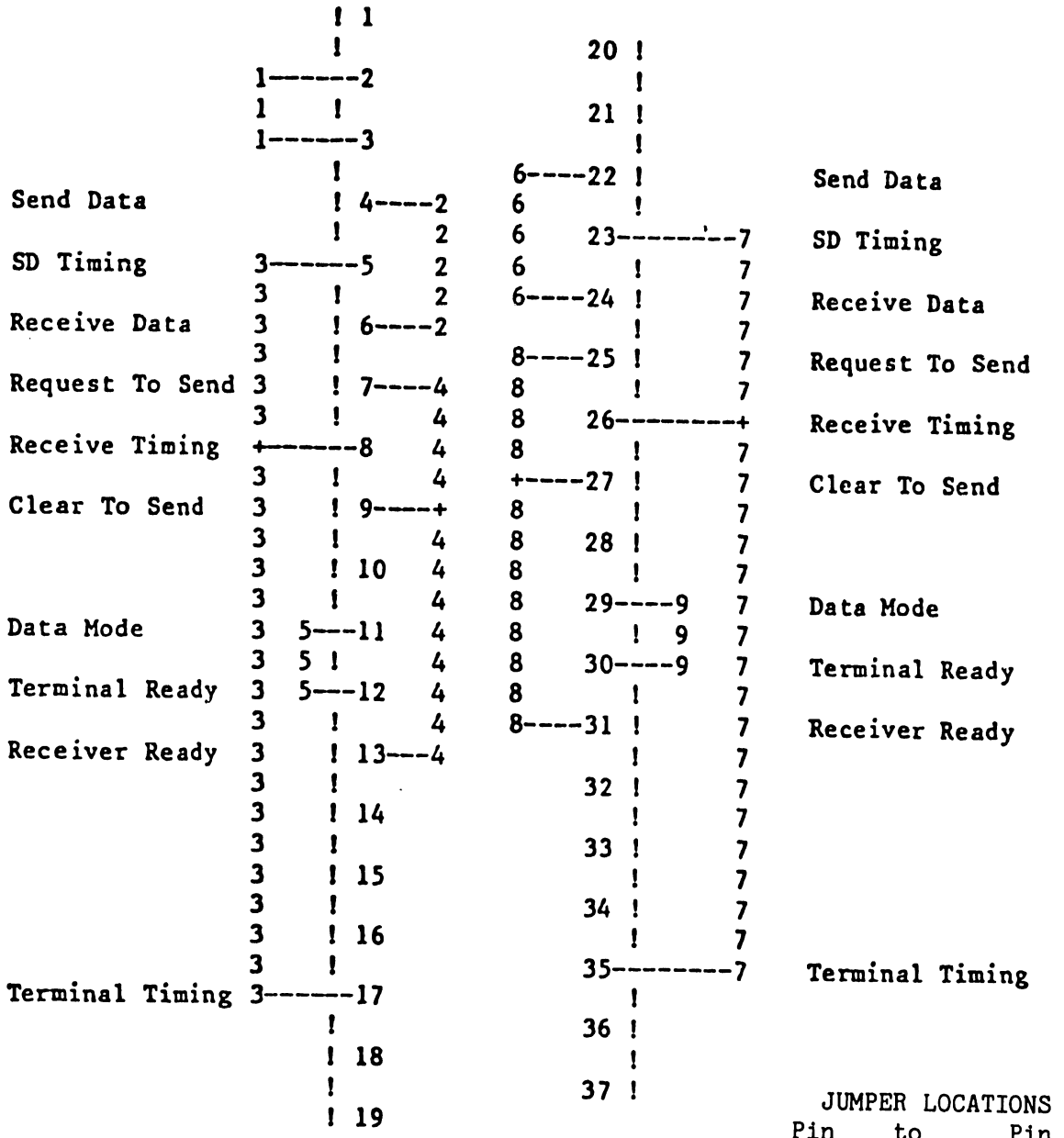
JUMPER LOCATIONS

Pin	to	Pin
2		3
4		5
6		8
8		20
11		12
12		15
15		17

APPENDIX E

APPENDIX E

RS449 LOOP BACK CONNECTOR WIRING DIAGRAM



JUMPER LOCATIONS

Pin	to	Pin
2		3
4		6
5		8
7		9
8		17
9		13
11		12
22		24
23		26
25		27
26		35
27		31
29		30

APPENDIX F

APPENDIX F

2228D TELECOMMUNICATIONS CONTROLLER POWER UP TESTS

The following tests are designed to briefly and efficiently test most of the LSI circuitry needed for overall board operation. The testing sequence is carried out as follows:

1. The Z80 Power-Up Test checks the known power-up conditions of the Z80 CPU. A failure here will result in a loop-on error within the test module. This is considered a catastrophic failure and no further testing will take place.

2. The PROM Checksum Test runs a checksum of the PROM to determine if any errors exist in PROM. If errors exist, the test will loop, keeping the LED on. This is considered a catastrophic failure and no further testing will take place.

3. The PIO Power-Up Test checks the known power-up conditions of the PIO chip. It also exchanges data patterns with both port output registers to insure they will hold data. Testing is limited to this since all pins of the PIO chip cannot be controlled directly by the Z80 CPU. If the basic register test is successfull data transfers between the 2200 and the 2228D TC Controller can be achieved . A failure here is considered catastrophic and no further testing will take place.

4. The Write Bad Parity/Parity Generator Test runs a two-pattern, write-bad-parity test using the write-bad-parity circuitry. Error information will be reported to the 2200 upon request.

5. The Bank Decoder Test stores a unique pattern in the first location of each bank. A read-after-write is performed to insure data errors do not exist. Then each unique pattern is read back and checked for errors. If a data error or pattern error is found, the bank test error will be reported to the 2200 upon request.

NOTE:

Data errors make the banks untestable, and therefore the memory is considered unreliable.

6. The 62K Ram Marching AA and 55 Test checks the 62K of RAM using a modified Marching Test. It is imperative that RAM is functioning properly since system operation depends on good memory for the purpose of either holding operating system micro-code or test Micro-code. A failure will result in either looping in the test (all 4 banks are bad), or the saving of error information for reporting to the 2200 at test end. Error information supplied is shown in the RAM test header.

NOTE:

This test uses an AA and 55 data pattern instead of the normal 00 and FF patterns due to the Data line etch layouts closeness in proximity.

7. The DMA (9517) chip is checked if RAM passes, to determine whether power-on conditions were met. It is also tested to see if the current address registers and word-count registers of all channels are capable of holding incremental data patterns. Error information will be reported to the 2200 at the end of the test.

8. The CTC chip is tested for functioning of the software timer channel (channel 0). It is also tested in the timer mode for each channel, for the purpose of detecting interrupts and checking down-counting. A failure will be reported to the 2200 upon request.

9. The SIO chip is tested in the Bisync, internal loop back-mode. Internal clocks at 9600 baud are provided by the CTC chip. A failure will be reported to the 2200 upon request.*

*See notes on next page

NOTE:

External loop back testing may be selected by installing a loop back plug and placing a HEX 01 in the option switches of the motherboard.

Failures result in either the LED remaining ON SOLID or FLASHING, if the LED is FLASHING this indicates a reportable failure. If the LED is ON SOLID this indicates a catastrophic failure has been detected with no reporting capabilities.

APPENDIX G

APPENDIX G

EBCDIC CODE CHART

IBM EBCDIC CODE SET

LOW ORDER HEX DIGIT \ HIGH ORDER HEX DIGIT	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NUL	DLE			SP	&	-						{	}	\	0
1	SOH	DC1			RSP		/		a	j	~		A	J		1
2	STX	DC2		SYN					b	k	s		B	K	S	2
3	ETX	DC3							c	l	t		C	L	T	3
4									d	m	u		D	M	U	4
5	HT	NL	LF						e	n	v		E	N	V	5
6			ETB						f	o	w		F	O	W	6
7			ESC	EOT					g	p	x		G	P	X	7
8									h	q	y		H	Q	Y	8
9		EM							i	r	z		I	R	Z	9
A					¢	!		:								
B	VT				.	$	,	#								
C	FF				<	*	%	@								
D	CR	IGS	ENQ	NAK	(	)	-	'								
E		IRS			+	;	>	=								
F		ITB	BEL		|	¬	?	"							PAD

BSC DATA LINK CHARACTERS

BEL	Bell
CR	Carriage Return
DLE	Data Link Escape
ENQ	Enquiry
EOT	End of Transmission
ESC	Escape
ETB	End of Text Block
ETX	End of Text
HT	Horizontal Tab
ITB	Intermediate Text Block
NAK	Negative Acknowledgement
NUL	Null
PAD	Trailing Pad Character
SOH	Start of Header
STX	Start of Text
SYN	Synchronous Idle

3270 Control Characters

DUP	Duplicate
EM	End of Medium
EUA	Erase Unprotected to Address
FF	Form Feed
FM	Field Mark
IC	Insert Cursor
NL	New Line
NUL	Null
PT	Program Tab
RA	Repeat to Address
SBA	Set Buffer Address
SF	Start Field
SUB	Substitute

IBM 2780 CONTROL CHARACTERS

EM	End of Media
SP	Space

IBM 3780 CONTROL CHARACTERS

DC1	Device Select Printer
DC2	Device Select Punch
DC3	Device Select Punch
FF	Form Feed
IGS	Interchange Group Separator
IRS	Interchange Record Separator
LF	Line Feed
NL	New Line
SP	Space
VT	Vertical Tab

BSC DATA LINK CONTROL SEQUENCES

ACK 0	Positive Acknowledgement 0 (DLE X '70)
ACK 1	Positive Acknowledgement 1 (DLE /)
DLE EOT	Disconnect Sequence for a Switched Line
RVI	Reverse Interrupt (DLE @)
TTD	Temporary Text Delay (STX ENQ)
WACK	Wait-Before-Transmit Positive Acknowledgement (DLE ,)

APPENDIX H

APPENDIX H

RS-232C CONNECTOR PIN ASSIGNMENT

PIN	EIA	CCITT	SIGNAL DESCRIPTION	SOURCE
1	AA	101	Protective Ground	
2	BA	103	Transmitted Data	2228D
3	BB	104	Received Data	Modem
4	CA	105	Request to Send	2228D
5	CB	106	Clear to Send	Modem
6	CC	107	Data Set Ready	Modem
7	AB	102	Signal Ground	
8	CF	109	Received Line Signal Detector	Modem
9				
10				
11	SCA	120	Secondary Request to SEnd	2228D
12	SCF	122	Secondary Rec'd Line Sig. Det.	Modem
13	SCB	121	Secondary Clear to Send	Modem
14	SBA	118	Secondary Transmitted Data	2228D
15	DB	115	Receiver Signal Element Timing	Modem
16	SBB	119	Secondary Received Data	Modem
17	DD	115	Receiver Signal Element Timing	Modem
18		124	Select Frequency Groups	2228D
19	SCA	120	Secondary Request to SEnd	2228D
20	CD	108.2	Data Terminal Ready	2228D
21	CG	110	Signal Quality Detector	Modem
22	CE	125	Ring Indicator	Modem
23	CH/CI	111/112	Data Signalling Rate Selector	2228D/Modem
24	DA	113	Trans. Signal Element Timing	2228D
25			Unassigned	

APPENDIX

I

APPENDIX I
RS-449-C CONNECTOR PIN ASSIGNMENT

PIN	SIGNAL DESCRIPTION	MNEM.	SOURCE
1		Shield	
2	Signal Rate Indicator	SI	Modem
3	Terminal Timing	TT	2228D
4	Send Data	SD	2228D
5	Send Timing	ST	Modem
6	Receive Data	RD	Modem
7	Request to Sent	RS	2228D
8	Receive Timing	RT	Modem
9	Clear to Send	LS	Modem
10	Local Loopback	LL	
11	Data Mode	DM	Modem
12	Terminal Ready	TR	2228D
13	Receive Ready	RR	Modem
14	Remote Loopback	RL	
15	Incoming Call	IC	Modem
16	Select Freq./Signal Rate Select.	SF/SR	
17	Spare	TT	
18	Test Mode		
19	Signal Ground	SG	
20	Incoming Call	IC	Modem
21	Terminal Timing	TT	2228D
22	Send Data	SD	2228D
23	Send Timing	ST	Modem
24	Receive Data	RD	Modem
25	Request to Send	RS	2228D
26	Receive Timing	RT	Modem
27	Clear to Send	CS	Modem
28	Terminal in Service	IS	
29	Data Mode	DM	Modem
30	Terminal Ready	TR	2228D
31	Receive Ready	RR	Modem
32	Select Standby	SS	
33	Signal Quality	SQ	
34	New Signal	NS	
35	Spare	TT	
36	Standby Indicator		
37	Signal Ground	SG	

APPENDIX J

APPENDIX J
BELL MODEMS

TELECOMMUNICATIONS SUPPORT

BELL MODEM 201C

TYPE Synchronous, half-duplex

SPEED 2400 BPS PRIVATE LINE

NETWORK For medium speed point-to-point PRIVATE LINE

WANG SYSTEMS For Wang VS 22V06 IOP.
For Wang VS Remote Workstations 2246R
For Wang Computers using the 2228B/OP62B, and 2228C/D
For Wang Word Processors using TC-3, TC-WS, TC-B2, TC-8, TC-B1

STANDARD MODEM DECISIONS FOR COMPATIBILITY WITH

DECISION		WANG SYSTEMS	COMMENTS
A	1. EIA Interface 2. Contace Interface	A1	(Note 1)
B	3. Alternate Voice	B3	Customers Choice
	4. W/O Alternate Voice		
C	5. With New Sync 6. W/O New Sync	C5	
D	7. 2-Wire 8. 4-Wire	D7	(Note 2)
E	9. 4-Wire Private Line (Continuous Carrier) 10. 4-Wire Private Line (Carrier controlled by Request-to-Send or multiparty)	E9	

Note 1 EIA is always used on Private Line with the 201C data set.
Note 2 If Decision D7 Decision E is not required

BELL MODEM 208A

TYPE Synchronous, half-duplex
SPEED 2400 BPS
NETWORK For high speed PRIVATE line point-to-point or multi-point networks
WANG SYSTEMS For Wang VS 22V06 IOP.
For Wang VS Remote Workstations 2246R
For Wang Computers using the 2228B/OP62B, and 2228C/D (multipoint operation with Burroughs emulation)
For Wang Word Processors using TC-3, TC-WS, TC-B2, TC-B, TC-B1 (point-to-point operation only)

DECISION			STANDARD MODEM DECISIONS FOR COMPATIBILITY WITH WANG SYSTEMS	COMMENTS
A	1.	transmitter internally timed	A1	
	2.	transmitter externally timed		
B	3.	continuous carrier	B3	Normal option for point to point connection. Use B4 if multipoint.
	4.	switched carrier		
C	5.	switched request to send		
	6.	continuous request to send	C5	If B4 was selected, C5 must be ***NOTE 1*** selected for proper operation
D	7.	one second holdover used	D7	
	8.	one second holdover not used		
E	9.	new sync used		
	10.	new sync not used	E10	
F	11.	data set ready lead on in analog loopback test	F11	
	12.	data set ready lead off in analog loopback test		

NOTE 1 For 2246R the modem on the remote side must have option C5. The modem on the CPU side must have option C6.

BELL MODEM 103J

TYPE Asynchronous, full-duplex
SPEED Up to 300 BPS
NETWORK For low speed, point-to-point SWITCHED networks
WANG SYSTEMS For Wang Computers using 2227B/OP62, 2228B/OP62B, or 2228C
For Wang Word Processors using TC-3, TC-WS.

DECISION			STANDARD MODEM DECISIONS FOR COMPATIBILITY WITH WANG SYSTEMS	COMMENTS
A	1.	Send space disconnect	A1	
	2.	No Send space disconnect		
B	3.	Receive Space Disconnect	B3	
	4.	No Receive Space Disconnect		
C	5.	Loss of Carrier Disconnect	C5	
	6.	No Loss of Carrier Disconnect		
D	7.	Fail Safe State of ON Circuit OFF	D7	
	8.	Fail Safe State of ON Circuit ON		
E	9.	Automatic Answer IN	E9	
	10.	Automatic Answer OUT		
F	11.	Factory Supplied EIA Interface	F11	
	12.	Customer Selected EIA Interface		

BELL MODEM 202S

TYPE Asynchronous, half-duplex
SPEED Up to 1200 BPS
NETWORK For medium speed, point-to-point SWITCHED networks
WANG SYSTEMS For Wang Computers using 2227B/OP62, 2228B/OP62B, or 2228C
For Wang Word Processors using TC-3, TC-WS.

DECISION		STANDARD MODEM DECISIONS FOR COMPATIBILITY WITH WANG SYSTEMS	COMMENTS
A	1.	Local copy on primary channel	
	2.	no Local copy on primary channel	A2
B	3.	local copy on reverse channel	
	4.	No local copy on reverse channel	B4
C	5.	Telco engineered timing options	C5
	6.	customer engineered timing options	
D	7.	DSR lead on in analog loopback test	D7
	8.	SDR lead off in analog loopback test	
E	9.	automatic answer in	E9
	10.	automatic answer out	
F	11.	signal and frame ground connected	F11
	12.	signal and frame ground not connected	

BELL MODEM 202T

TYPE Asynchronous, half-duplex or full-duplex
SPEED Up to 1800 BPS
NETWORK For medium speed PRIVATE line, point-to-point or multi-point networks
WANG SYSTEMS For 2236 Remote Terminal connection to 2200MVP with 2236MXD (for point-to-point connections only)
For Wang Computers using 2227B/OP62, 2228B/OP62B, or 2228C (multi-point operation only with BURROUGHS emulator)
For Wang Word Processors using TC-3, TC-WS.

DECISION		STANDARD MODEM DECISIONS FOR COMPATIBILITY WITH WANG SYSTEMS	COMMENTS
A	1. local copy on primary channel	A1	See NOTE 1
	2. no Local copy on primary channel		
B	3. local copy on reverse channel		
	4. No local copy on reverse channel	B4	
C	5. Telco engineered timing options	C5	
	6. customer engineered timing options		
D	7. Telco engineered timing options	D7	See NOTE 2
	8. customer engineered timing options		
E	9. Reverse Channel installed		
	10. Reverse Channel not installed	E10	See NOTE 3
F	11. signal and frame ground connected	F11	
	12. signal and frame ground not connected		

NOTE 1 Option A1 & A2 does not apply when 4-wire required.

NOTE 2 The following control options are provided by decision D7, and are recommended.

Option		Designation
Carrier Detector Reset	OUT	ZM
Continuous Carrier	IN	ZN
State of DSR in Analog Loopback	OFF	YA
Receive Data Clamp	IN	F

NOTE 3 Specify 4-wire for 2236 terminal. (This is a standard option)

BELL MODEM 212A

TYPE Asynchronous, full-duplex
Synchronous, full-duplex
SPEED 300/1200 BPS dual mode - Asynchronous operation
1200 BPS - Synchronous/300 BPS Asynchronous operation
NETWORK For low or medium speed, point-to-point SWITCHED networks
WANG SYSTEMS For Wang VS 22V06 IOP.
For Wang VS Remote Workstation 2246R
For Wang Computers using 2227B/OP62, 2228B/OP62B, or 2228C
For Wang Word Processors using TC-3, TC-WS, TC-B2, TC-B, TC-B1

DECISION			STANDARD MODEM DECISIONS FOR COMPATIBILITY WITH WANG SYSTEMS	COMMENTS
A	1.	factory supplied disconnect options	A1	See NOTE 1
	2.	customer selected disconnect options		
B	3.	automatic answer - yes		
	4.	automatic answer - no	B3	
C	5.	factory supplied EIA interface	C5	
	6.	customer selected EIA interface		
D	7.	factory supplied dual	D7	This option will mode enable Dual 300/1200ASYNC Mode
	8.	for 1200 BPS synchronous	Select D8 and the mode below listed sub-options for dual mode 1200 synchronous and 300 asynchronous operation. D8a2 D8c1 D8d2 D8e1	
E	9.	interface controlled make busy/analog loop-in		
	10.	interface controlled make busy/analog loop-out	E10	

NOTE At 1200 BPS, the 212A is not compatible with Bell 202 type modems.

BELL MODEM 201C

TYPE Synchronous, half-duplex
SPEED 2400 BPS
NETWORK For medium speed, point-to-point SWITCHED networks
WANG SYSTEMS For Wang VS 22V06 IOP.
For Wang VS Remote Workstation 2246R
For Wang Computers using 2227B/OP62, 2228B/OP62B, or 2228C
For Wang Word Processors using TC-3, TC-WS, TC-B2, TC-B, TC-B1

DECISION			STANDARD MODEM DECISIONS FOR COMPATIBILITY WITH WANG SYSTEMS	COMMENTS
A	1.	Transmitter Timing Internal	A1	
	2.	Transmitter Timing External		
B	3.	Automatic Answer not provided		
	4.	Automatic Answer controlled by DTR only	B4	
C	5.	Ring indicator on EIA interface pin 22	C5	
	6.	Ring indicator contact closure on pins 22 and 23		
D	7.	Continuous receiver bit clock-in		
	8.	Continuous receiver bit	D8	Select D7 if direct distance-dialing oversatellite link, otherwise D8
E	9.	EIA interface pin 18 includes local analog loopback		
	10.	EIA interface pin 18 provides receive symbol clock	E10	
F	11.	signal and frame ground connected	F11	
	12.	signal and frame ground not connected		

BELL MODEM 208B

TYPE Synchronous, half-duplex
SPEED 4800 BPS
NETWORK For high speed, point-to-point SWITCHED networks
WANG SYSTEMS For Wang VS 22V06 IOP.
For Wang VS Remote Workstation 2246R
For Wang Computers using 2227B/OP62, 2228B/OP62B, or 2228C
For Wang Word Processors using TC-3, TC-WS, TC-B2, TC-B, TC-B1

DECISION			STANDARD MODEM DECISIONS FOR COMPATIBILITY WITH WANG SYSTEMS	COMMENTS
A	1.	Transmitter Internally Timed	A1	
	2.	Transmitter Externally Timed		
B	3.	Without R01 Auto calling unit	B3	Select B4 if auto-calling is reqiured.
	4.	With R01 Auto calling unit		
C	5.	CC off when AL pressed		
	6.	CC on when AL pressed	C6	
D	7.	Without Automatic Answer		
	8.	With Automatic Answer	D8	
E	9.	desk mounting	E9	
	10.	rack or cabinet mounting		

BELL MODEM 209A

TYPE Synchronous, Binary Serial

SPEED(S)

9600bps	___	
7200 - 2400bps	!	
4R00 - 4800bps	!	Mutliplex
4800 - 2400 - 2400bps	!	Combinations
2400 - 2400 - 2400 - 2400bps	!	

NETWORK Point-to-Point 9600 Service
Point-to-Point 9600 Multiplex Service
Many Point Multiplexing Service
One - to - Many Mutiplexing Service
DDD Backup at a selectable speed of 9600 bps or 4800 bps

WANG SYSTEMS For Wang VS 22V06 IOP.
For Wang VS Remote Workstation 2246R
For Wang Computers using 2227B/OP62, 2228B/OP62B, or 2228C
For Wang Word Processors using TC-3, TC-WS, TC-B2, TC-B, TC-B1

DECISION		STANDARD MODEM DECISIONS FOR COMPATIBILITY WITH WANG SYSTEMS	COMMENTS
A	1. Transmitter Timing by Data Set	A1	
	2. Transmitter Timing by Data Terminal		
B	3. Data Set Read interface Load On in Analog Loopback Mode	B3	
	4. Data Set Ready interface Lead OFF in Analog Loopback Mode		
C	5. Transmit Timing Slaved to Receive Timing	C5	
	6. Transmit Timing Not Slaved to Receive Timing		
D	7. Elastic Stores IN		
	8. Elastic Stores OUT	D8	NOTE 1
E	9. Continuous Carrier	E9	(Decision F required)
	10. Switched Carrier		(Decision F not required)
F	11. Switched Request to Send	F11	
	12. Continuous Request to Send		

NOTE 1 Elastic Stores should be IN for 209A (multiplexer) to Modem operation and OUT for 209A to Terminal operation.

BELL MODEL 801A

AUTOMATIC CALLING UNIT

DATA SET - PRIVATE LINE - SERIES 800

DECISON	OPTION	SELECT DECISION
A	1. EIA Voltage Interface	A1
	2. Contact Interface	
B	3. Call terminated through ACU after DSS on	
	4. Call terminated through data set after DSS on	B4
C	5. ACR timer stopped after DSS on	C5
	6. ACR timer not stopped after DSS on	
D	7. End-of-number signal from Customer terminal	D7
	8. No end-of-number signal from customer terminal(**See Note**)	
E	9. ACR answer-tone detection (801A6 only)	
	10. Data set answer-tone detection without EON signal (R01A5 only)	

NOTE: If D7 decision, no E decision is required. If D8 decision E decision is made.

BELL MODEL 801C

AUTOMATIC CALLING UNIT

DATA SET - PRIVATE LINE - SERIES 800

DECISON	OPTION	SELECT DECISION
A	1. 2-Wire	A1
	2. 4-Wire	
B	3. Call terminated ACU	
	4. Call terminated through data set after DSS on	B4
C	5. ACR timer stopped after DSS on	C5
	6. ACR timer not stopped after DSS on	
D	7. Line transfer controlled by end-of-number signal from customer terminal (see Note 2)	D7
	8. No end-of-number signal from customer terminal(see Note 2)	
E	9. Line transfer after ACU answer-tone detection (R01C4 only)	
	10. Data set answer-tone detection without EON	E10
F	11. Loop start (R01C4 only)	
	12. Ground Start	

NOTE 1: If Decision D7, ACU option B must be installed in R01C3 or 801C4 and Decision E is limited to 9.

NOTE 2: If Decision is D8, then the choice must be made in Decision E between an 801C4 with option B or option E in 801C3 or 801C4

BELL MODEL 801C L1/2

AUTOMATIC CALLING UNIT

DATA SET - PRIVATE LINE - SERIES 800

DECISON	OPTION	SELECT DECISION
A (See Note 1)	1. Signal ground connected to frame ground	A1
	2. Signal ground NOT connected to frame ground	
B	3. Call terminated through ACU	
	4. Call terminated through data set after DSS ON	B4
C	5. ACR timer stopped after DSS on	C5
	6. ACR timer NOT stopped after DSS ON	
D (see Note 2)	7. Longest ACR timing interval	
	8. ACR timing interval specified by customer	

Note 1: If second dial tone detection is required option A2 must be selected and TELCO option 12 (Loop start) must be selected. Grounding option of the data set and ACU must be the same.

Note 2: The longest ACR time available is 40 seconds or greater

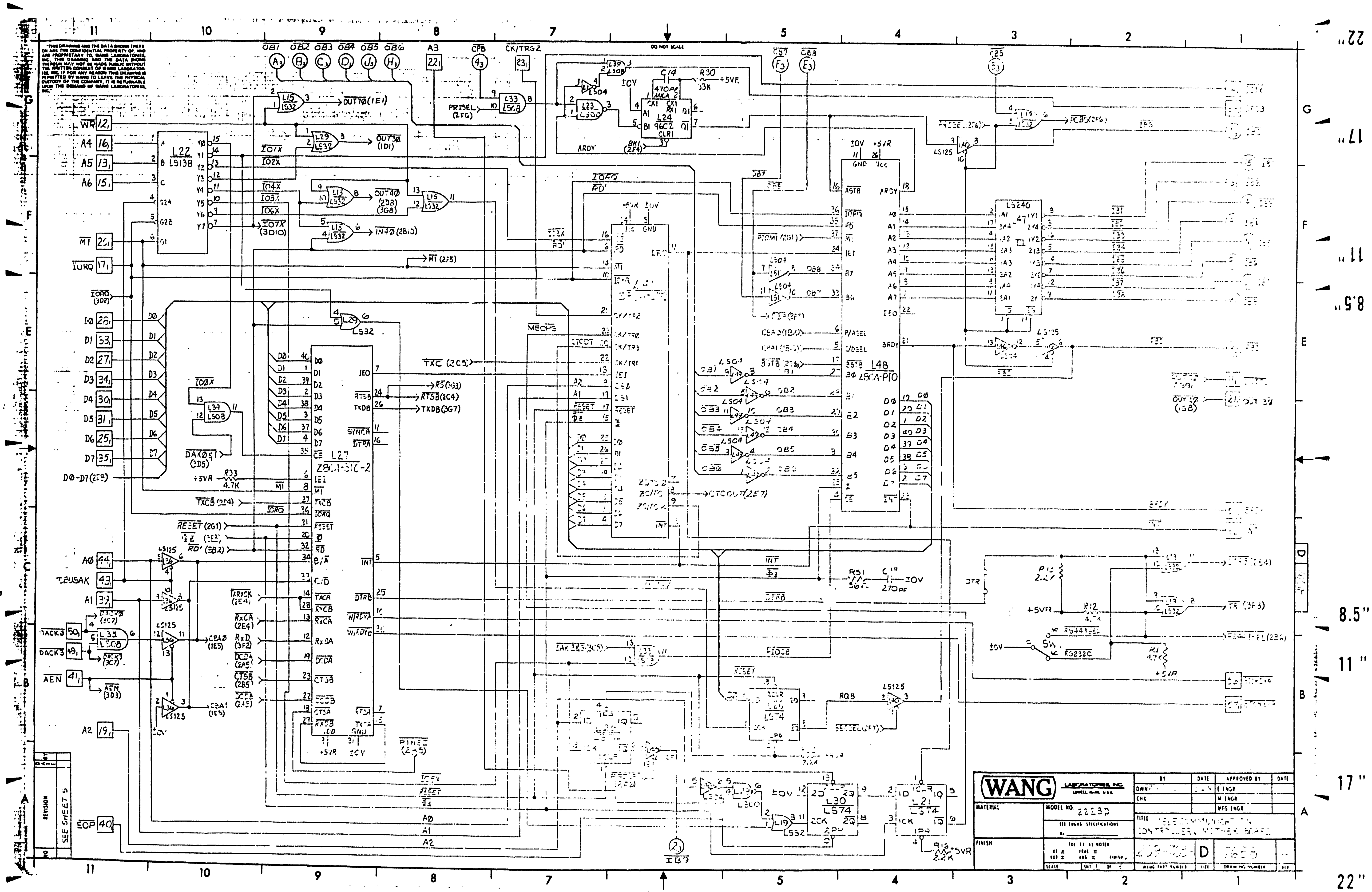
The customer specified ACR times are:

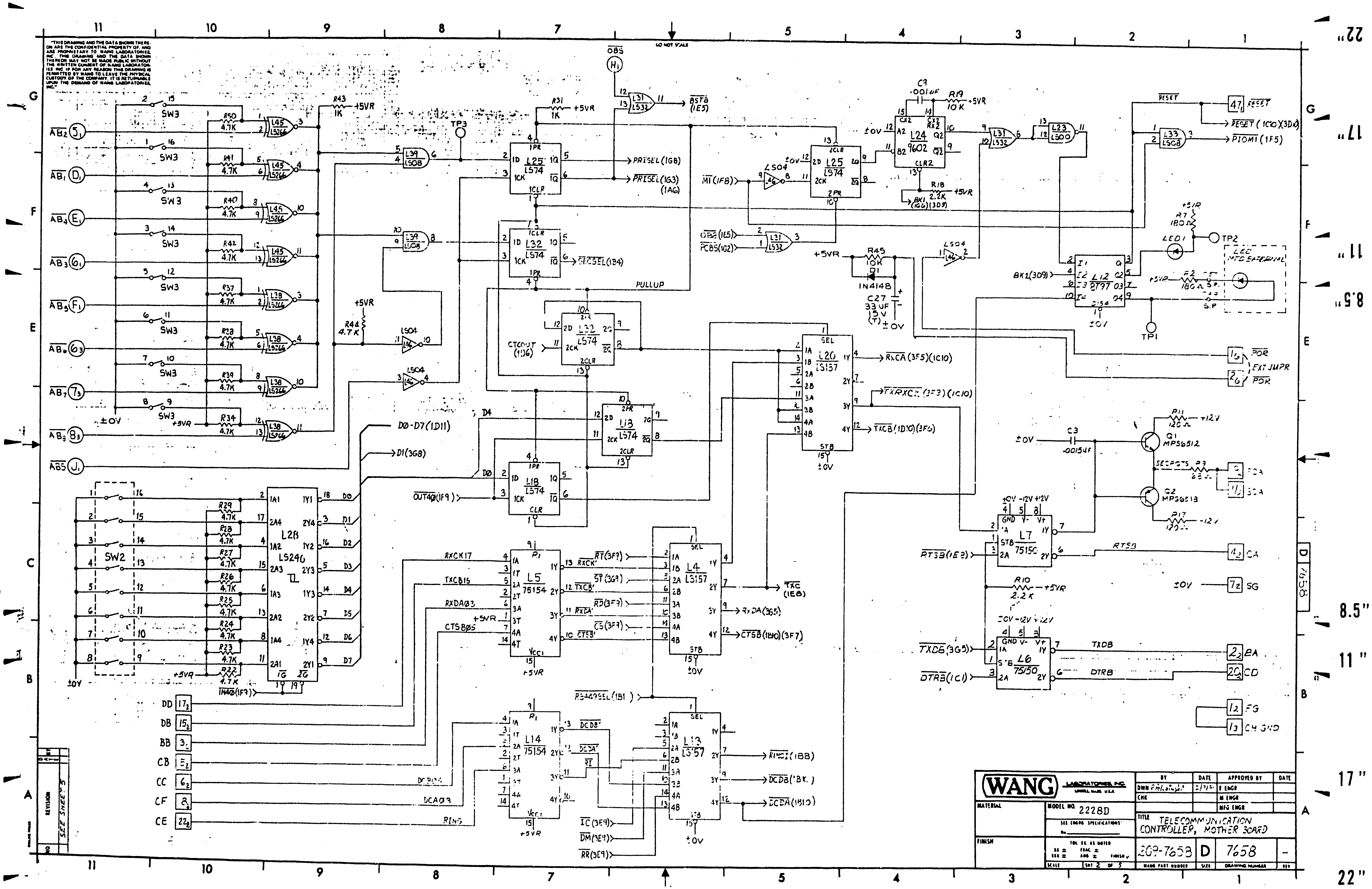
1. 7 seconds
2. 14 to 15 seconds
3. 25 to 28 seconds

APPENDIX
B
SCHEMATIC
DRAWINGS

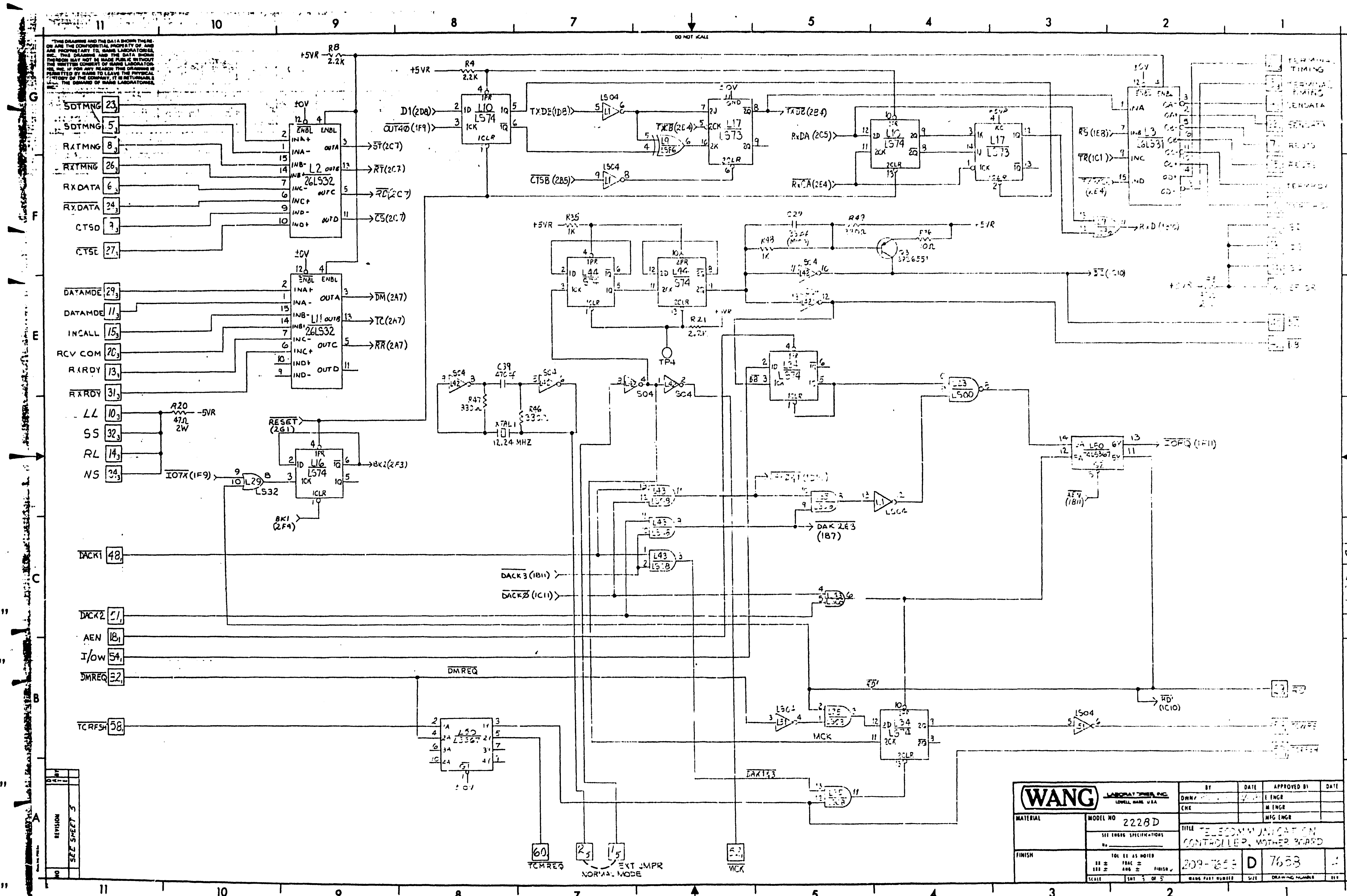
APPENDIX B
SCHEMATIC DRAWINGS

Schematic No.	Title	No. of Sheets
210-7658	motherboard	5
210-7659	daughter	4

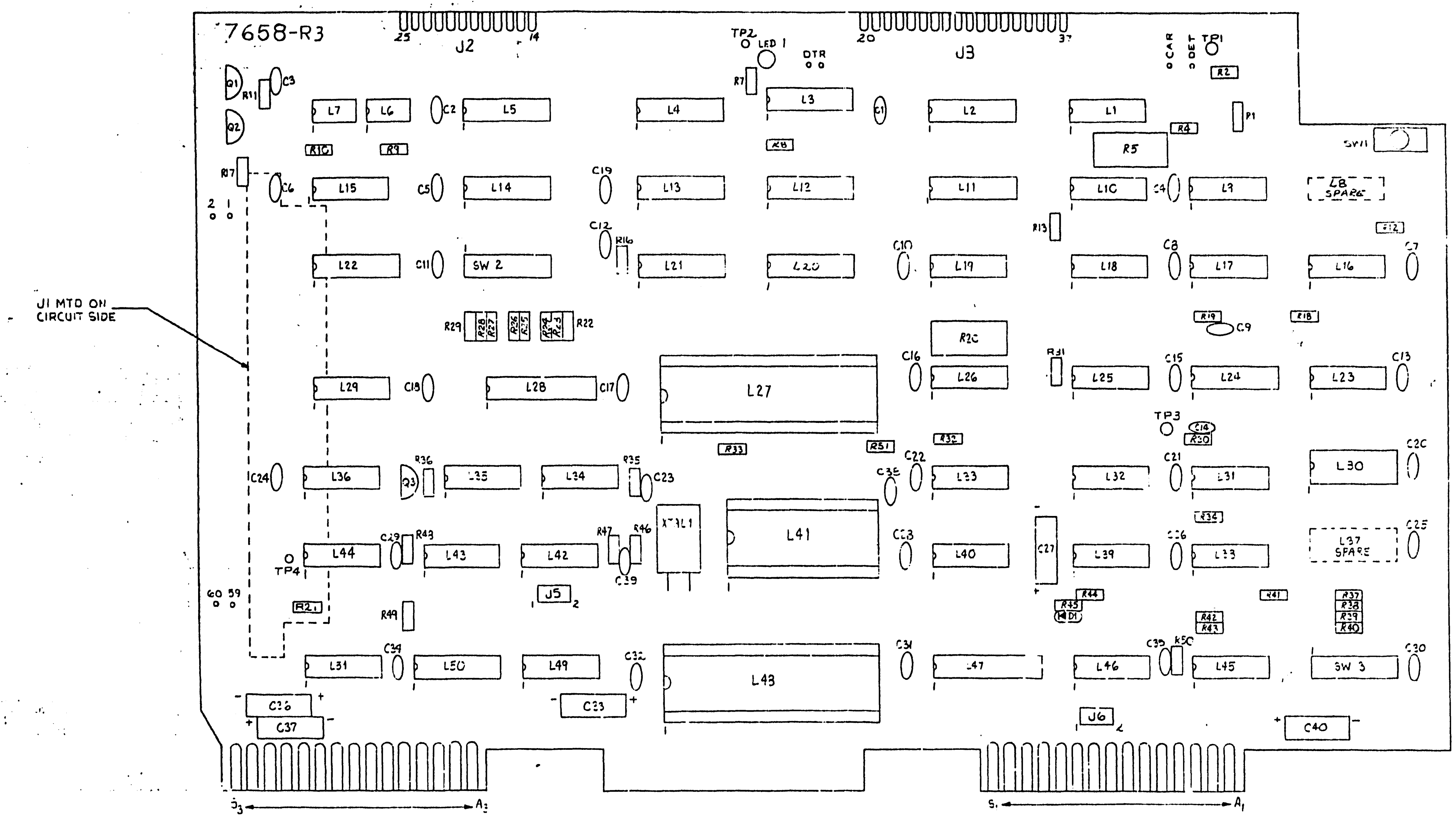

L22 LS138
L27 Z80A-SIO-2
L48 Z80A-PIO
L24 96C2
L30 LS74
L21 LS74
LS240
DO NOT SCALE
WANG LABORATORIES, INC.
MODEL NO. 2223D
SEE SHEET 5



WANG LABORATORIES INC.
MODEL NO. 2228D
TITLE TELECOMMUNICATION CONTROLLER, MOTHER BOARD
209-7658 D 7658
SHT 2 OF 5
L28 LS240
L5 75154
L4 LS157
L14 75154
L13 LS157
L20 LS157
L25 LS74
L24 9602
L12 2797
L7 75150
L6 75150
Q1 MPS6512
Q2 MPS6513
SW2
SW3
D0-D7 (1D11)
PRTSEL (1G8)
RESET (1C0)(3D4)
PIOMI (1F5)


DO NOT SCALE
SDTMNG 23
SDTMNG 5
RXTMNG 8
RXTMNG 26
RXDATA 6
RXDATA 24
CTSD 3
CTSC 27
DATAMDE 29
DATAMDE 11
INCALL 15
RCV COM 20
RXRDY 13
RXRDY 31
LL 10
SS 32
RL 14
NS 34
DACK1 48
DACK2 51
AEN 18
I/OW 54
DMREQ 32
TCRFSH 58
L2 26LS32
L11 26LS32
L10 LS74
L16 LS74
L29 LS32
L17 LS73
L44 S74
L34 LS74
L3 26LS31
L60 LS367
L43 LS08
L23 LS00
R8 2.2K
R4 2.2K
R20 47Ω 2W
R35 1K
R21 2.2K
C39 470pf
XTAL1 12.24 MHZ
TP4
+5VR
-5VR
D1(2D8)
OUT40(1F9)
TXDE(1D8)
TXDE(2E4)
RxDA (2C5)
RxCA(2E4)
CTSB (2B5)
RESET (2G1)
IOTX(1F9)
BK1 (2F4)
BK2(2F3)
ST(2C7)
RT(2C7)
RD(2C7)
CS(2C7)
DM(2A7)
TC(2A7)
RR(2A7)
DACK3 (1B11)
DACK0 (1C11)
DAK 2E3 (1B7)
DMREQ
MCK
DAK1,3
TCMREQ 60
EXT JMPR
NORMAL MODE
MCK 52
IOFIQ (1F11)
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
MODEL NO 2228D
TITLE TELECOMMUNICATION CONTROLLER, MOTHER BOARD
SIZE D
DRAWING NUMBER 7653
SHT 5 OF 5
REVISION SEE SHEET 3
MATERIAL
FINISH

DO NOT SCALE



REVISION: SEE SHEET 5

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN		E ENGR	
		CHK		M ENGR	
				MFG ENGR	
MATERIAL	MODEL NO 2228D	TITLE TELECOMMUNICATION CONTROLLER, MOTHER BOARD			
	SEE ENGRG SPECIFICATIONS No.				
FINISH	TOL EX AS NOTED .XX ± FRAC ± .XXX ± ANG ± FINISH	WANG PART NUMBER 209-7658	SIZE D	DRAWING NUMBER 7658	REV
	SCALE / SHT 1 OF 5				

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DO NOT SCALE

COMPONENT	TYPE	W.L. PART NO.
SW1	SPDT	325-0033
SW2,3	8 POS SPST	325-1503
R1,12, 22-29,33,34, 37-42,44,50	4.7K 1/4W 10%	330-3047
R4,8,10,13,16,18, 21,32	2.2K 1/4W 10%	330-3022
R5,20	47Ω 2W 10%	337-1047
R2,7	180Ω 1/4W 10%	330-2018
R9	68Ω 1/4W 10%	330-1068
R11,17	120Ω 1/4W 10%	330-2012
R19,45	10K 1/4W 10%	330-4010
R30	33K 1/4W 10%	330-4033
R31,35,43,48	1K 1/4W 10%	330-3010
R36	10Ω 1/4W 10%	330-1010
R46,47,49	330Ω 1/4W 10%	330-2033
R51	56Ω 1/4W 10%	330-1056
C1,2,4-8,10-13, 15-26,28,30-32, 34,35	.05uF, 12 V	300-1900
C3	.0015uF 500V	300-1907
C9	.001uF 500V	300-1906
C14	470pF 500V MICA	300-5005
C27	33uF 15V(T)	300-4019
C29	33pF 500V(MICA)	300-5016
C33,36,37,40	15uF 20V (T)	300-4022
C38	270PF 500V	300-1270
D1	IN4148	380-1014
LED1	MV5024	370-0026
XTAL1	12.24 MHZ	321-0019
Q1	MPS6512	375-1012
Q2	MPS6518	375-1014
Q3	SPS6551	375-1050
J1	60 PIN 90°	350-0051
J2	CONN. 25 PIN	350-1031
J3	CONN. 37 PIN	350-1066
J5,6	HEADER 2 POS	350-0203
C39	470PF 500V	300-1470

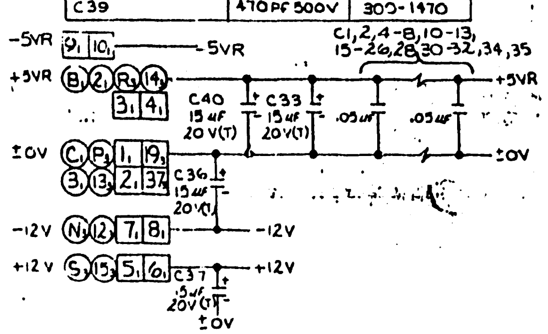
I.C. LOCATION	TYPE	W.L. PART NO.
L1,46,49,51	74LS04	376-0180
L2,11	26LS32	376-0471
L3	26LS31	376-0470
L4,13,20	74LS157	376-0216
L5,14	75154	376-0077
L6,7	75150	376-0076
L8,37	SPARE	
L9	74LS86	376-0231
L10,16,18,21,25,26,30,32,34	74LS74	376-0155
L12	8T97	376-0189
L15,19,29,31	74LS32	376-0211
L17	74LS73	376-0304
L22	74LS138	376-0294
L23	74LS00	376-0207
L24	9602	376-0104
L27	Z80A-SIO-2	SEE CHART
L28,47	74LS240	376-0297
L36,40	74LS125	376-0486
L33,35,39,43	74LS08	376-0153
L44	74S74	376-0202
L38,45	74LS266	376-0148
L41	Z80A-CTC	SEE CHART
L42	74S04	376-0197
L48	Z80A-PIO	SEE CHART
L50	74LS367	376-0192
L27,48	SKT, 40 PIN	376-9011
L41	SKT, 28 PIN	376-9015

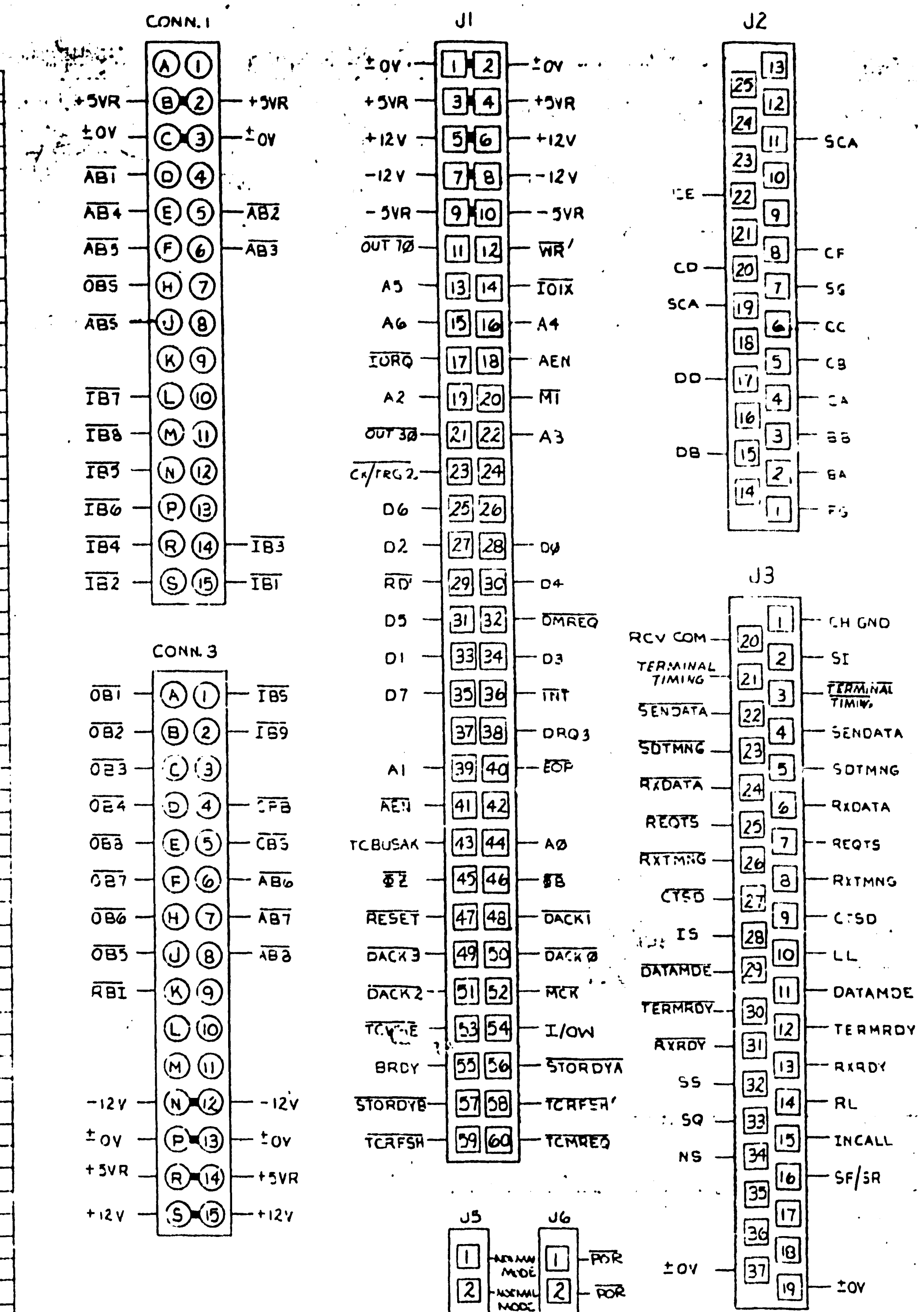
TYPE	I.C. LOCATION	SPARES
74LS04	L1	2
	L51	2
74LS08	L33	1
74LS32	L29	1
	L31	1
74LS74	L16	1
	L21	1
	L30	1
74LS86	L3	2
8T97	L12	1

210 = 209 + 377 OR 378				
210	209	L27	L41	L48
7658-A	7658	377-0353	377-0371	377-0373

MNEMONICS	COORD
A0	1C11
A1	1C11
A2	1B11
A3	1G8
A4	1G11
A5	1F11
A6	1F11
AB1-AB8	2F11
ABS	2D11
AEN	3C11
AEN	1B11
BA	2B1
BB	2A10
BRDY	1D1
CA	2C1
CB	2A10
CBS	1G3
CC	2A10
CD	2B1
CE	2A10
CF	2A10
CH GND	2B1
CPB	1G8
CTSD	3F11
CTSD	3F11
CK/TRG 2	1G7
D0-D7	1E11
DACK0, DACK3	1B11
DATAMDE	3E11
DATAMDE	3E11
DB	2B10
DD	2E10
DMREQ	3B11
DRQ3	1G1
EOP	1A11
FG	2B1
IB1-IB8	1F1
IB9	1A6
IBS	1G1
INCALL	3E11
RCV COM	3E11
INT	1C1
IOIX	1G1
IORQ	[illegible]
I/OW	3B11
IS	3F1
DACK1	3C11
DACK2	3C11

MNEMONICS	COORD
BB	3E1
BZ	3E1
LL	3D11
MT	1F11
MCK	3A6
OUT30	1E1
NS	3D11
OUT70	1E1
OB1-OB6	1G9
OB7	1G5
OB8	1G5
OBS	2G6
RBI	1E1
RCV COM	3E11
RD'	3B1
RESET	2G1
REQTS	3G1
REQTS	3F1
RL	3D11
RXDATA	3F11
RXDATA	3F11
RXRDY	3E11
RXRDY	3C11
RXTMNG	3G11
RXTMNG	3F11
SCA	2D1
SDTMNG	3G1
SDTMNG	3G1
SENDATA	3G1
SENDATA	3G1
SF/SR	3E1
SG	2C1
SI	3F1
SQ	3F1
SS	3D11
STORDYA	1B1
STORDYB	1B1
TCBUSAK	1C11
TCMREQ	3A7
TCRFSH	3B1
TCRFSH'	3B11
TCWRE	3B1
TERMINAL TIMING	3G1
TERMINAL TIMING	3G1
TERMRDY	3F1
TERMRDY	3F1
WR'	1G11
NORMAL MODE	3A7
SSQ	2E1





NO	REVISION	DATE	BY
0	ORIGINATED PER DWR # E783 APPD.		
1	REVISED PER ECN # 15643 APPD.		
2	REVISED PER ECO # 16396 APPD.	11-17-80	L.B.C.
3	REVISED PER ECO # 16541 APPD.	11-17-80	L.B.C.
4	REVISED PER ECO # 17320 APPD.	1-6-81	T.K.

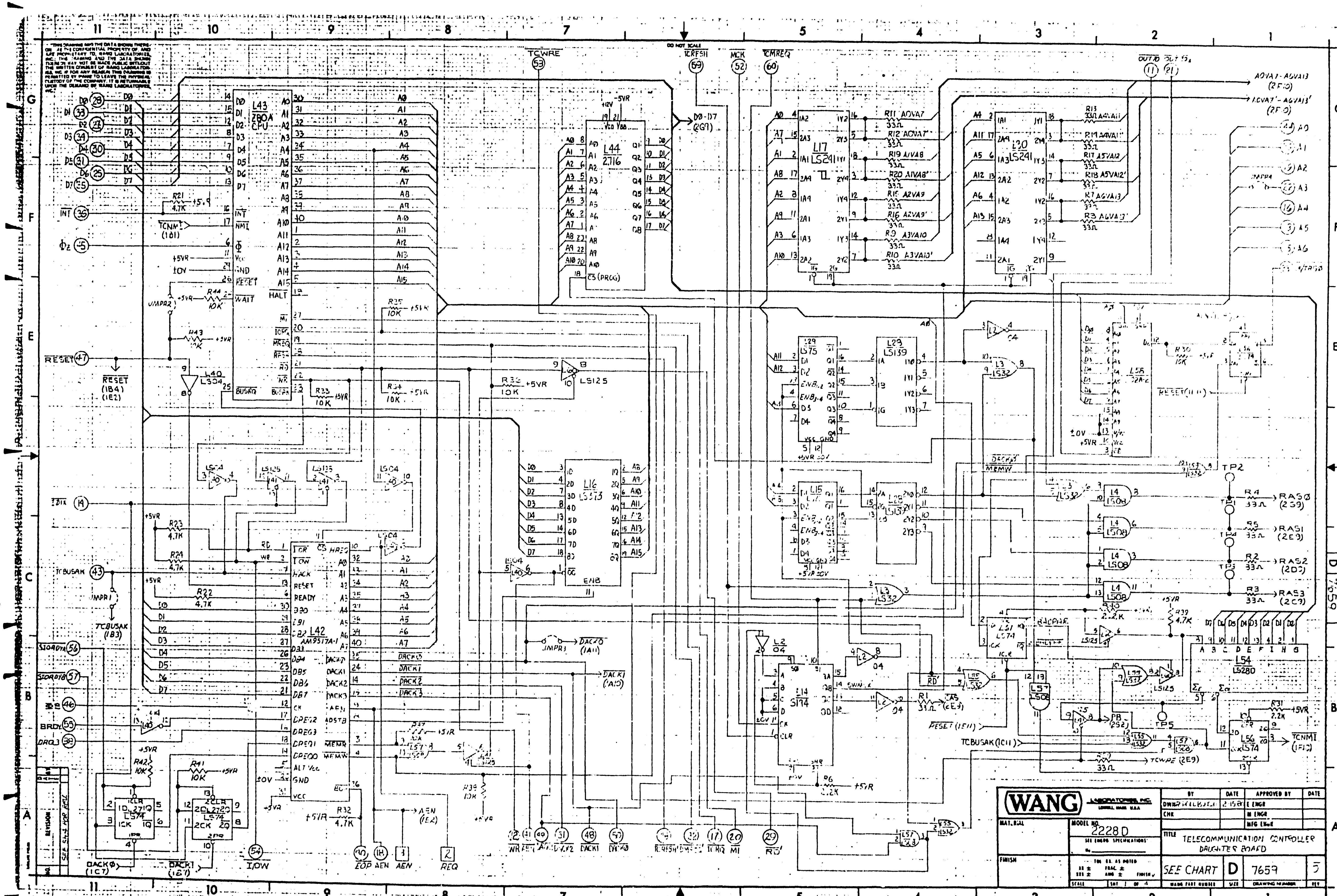
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MODEL NO. 2228D

TITLE TELECOMMUNICATION CONTROLLER, MOTHER BOARD

WANG PART NUMBER 209-7658 | SIZE D | DRAWING NUMBER 7658

SHT 5 OF 5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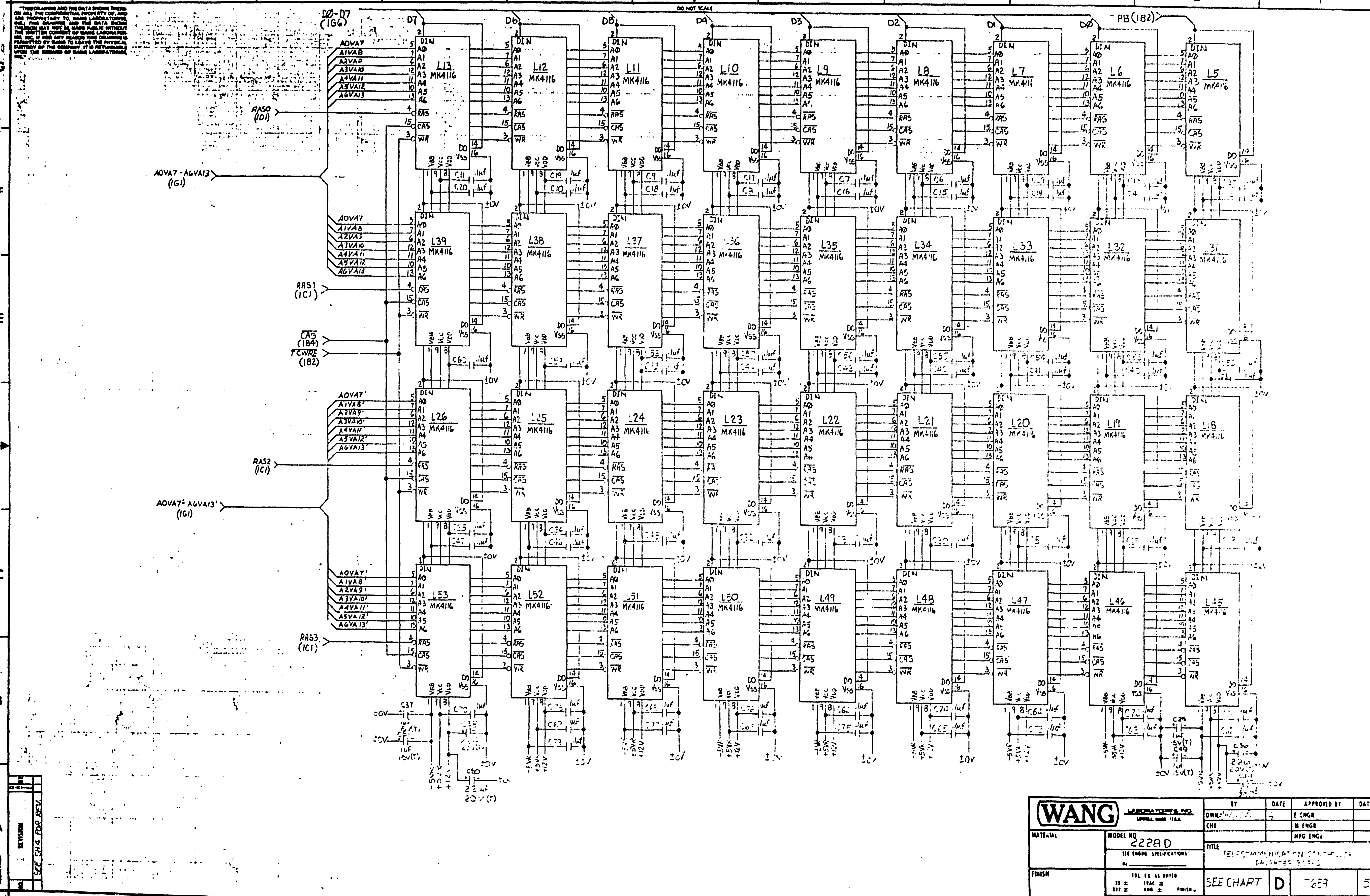
DO NOT SCALE
L43 Z80A CPU
L44 2716
L17 LS241
L30 LS241
L29 LS75
L23 LS139
L16 LS373
L15 LS75
L28 LS139
L42 AM9517A-1
L14 S174
L54 LS280
L56 LS74
TCWRE
TCRFSH
MCK
TCMREQ
D0-D7 (2G9)
A0VA7 - A6VA13 (2F10)
A0VA7' - A6VA13' (2F10)
RESET (1B4) (1E2)
TCBUSAK (1B3)
DACK0 (1A11)
DACK1 (1A10)
RAS0 (2G9)
RAS1 (2E9)
RAS2 (2D9)
RAS3 (2C9)
TCNMI (1F10)
TCWPE (2E9)
CAS (2E9)
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
MODEL NO. 2228D
TITLE TELECOMMUNICATION CONTROLLER DAUGHTER BOARD
SEE CHART
D
7659
5
SHT 1 OF 4



WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

BY	DATE	APPROVED BY	DATE
DWN		E ENGR	
CHK		M ENGR	
		MFG ENG.	

MATERIAL

MODEL NO 2228D

SEE ENGRG SPECIFICATIONS No.

TITLE TELECOMMUNICATION CONTROLLER DAUGHTER BOARD

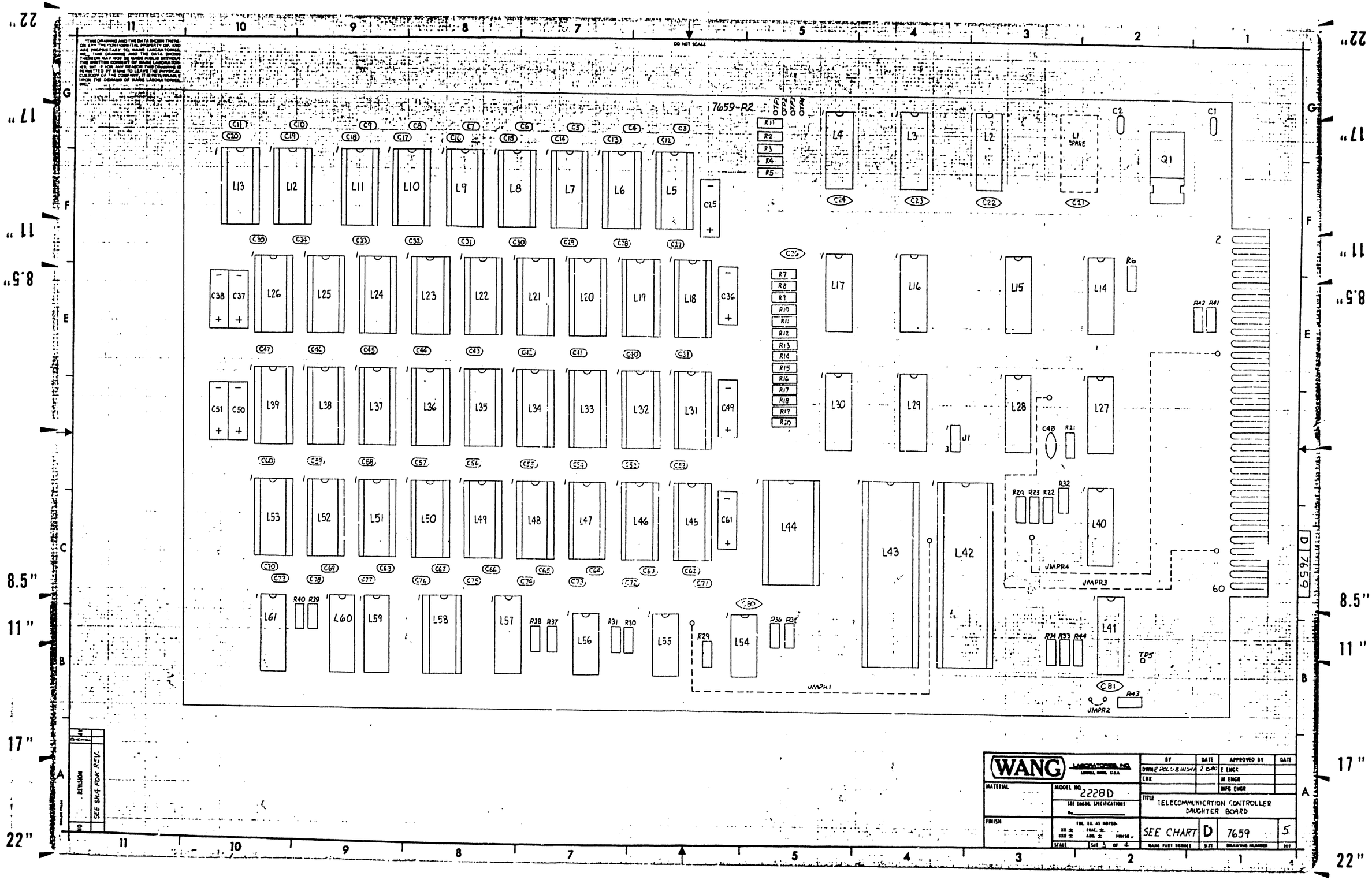
FINISH

TOL. EX. AS NOTED XX ± XXX ± FRAC ± ANG ± FINISH

SCALE SHT 2 OF 3

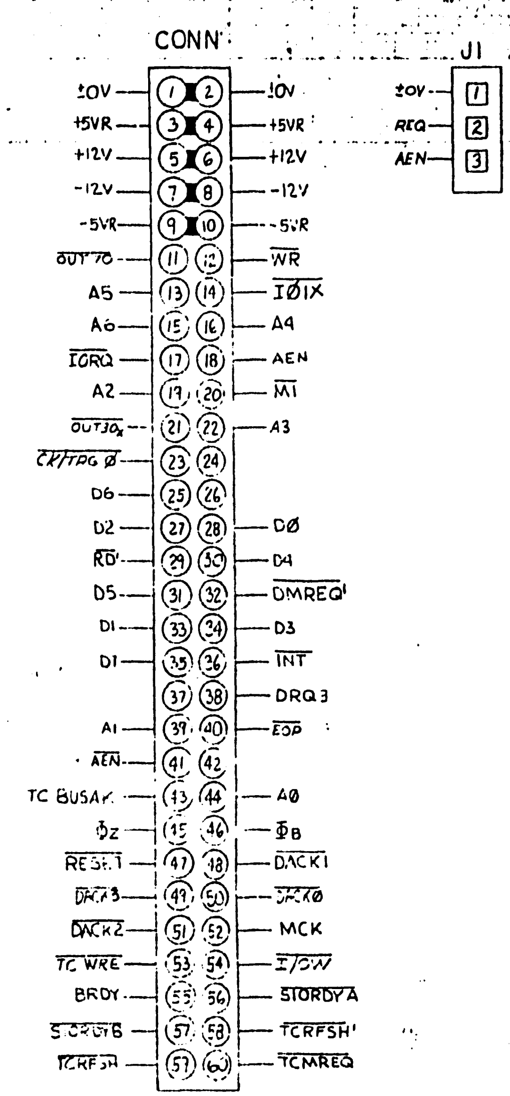
SEE CHART | D | 7659 | 5

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV


7659-R2
L1 SPARE
JMPR1
JMPR2
JMPR3
JMPR4
TP5
DO NOT SCALE
SEE SHT FOR REV.
REVISION
WANG LABORATORIES, INC.
MODEL NO. 2228D
SEE ENGRG SPECIFICATIONS
TITLE TELECOMMUNICATION CONTROLLER DAUGHTER BOARD
SEE CHART
D
7659
5

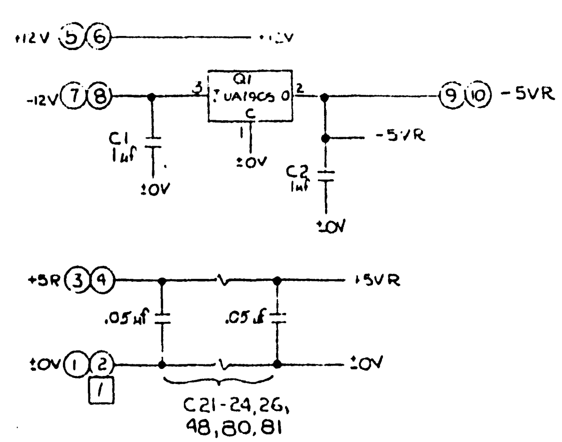
COMPONENT	TYPE	W.L. PART NO.
Q1	UA7905	374-0002
R1-5, 7-20, 29	33Ω, ¼W, 10%	330-1033.
R6, 31, 40	2.2K, ¼W, 10%	330-3022
R21-24, 32, 39	4.7K, ¼W, 10%	330-3047
R30, 33-38, 41, 44	10K, ¼W, 10%	330-4010
C1, 2	1uf, 50V	300-1931
C3-20, 27-35, 39-47, 52-60, 62-79	.1uf, 50V	300-1930
C21-24, 26, 48, 80, 81	.05 uf, 12V	300-1900
C25, 37, 49, 51	1uf, 15V(T)	300-4056
C36, 38, 50, 61	2.2 uf 20V(T)	300-9019

IC LOCATION	W.I. PART NO.	TYPE
L1		SPARE
L2	376-0010	7404
L3, 55, 59	376-0211	74LS32
L4, 57	376-0153	74LS08
L5-13, 18-26, 31-39, 45-53	SEE CHART	MK4116
L14	376-0221	74S194
L15, 29	376-0312	74LS75
L16	376-0310	74LS373
L17, 30	376-0289	74LS241
L28	376-0226	74LS139
L41, 60	376-0486	74LS125
L42	SEE CHART	AM95172-1
L43	SEE CHART	Z80A CPU
L44	SEE CHART	TMS 2716
L54	376-0242	74LS280
L56, 27, 61	376-0155	74LS74
L40	376-0180	74LS04
L58	SEE CHART	2102A-2
L5-13, 18-26, 31-39, 45-53	SKT, 16 PIN	376-9002
L42, 43	SKT, 40PIN	376-9011
L44	SKT, 24	376-9003



MNEMONIC	COORD
AØ-A6	1G1
AEN	1A7
AEN	1A9
BRDY	1B11
DØ-D7	1G11
CK/TRG Ø	1F1
DACKØ-DACK3	1A7
DMREQ'	1A6
DRQ 3	1B11
IØIX	1D11
ΦB	1B11
ΦZ	1F11
INT	1F11
IORQ	1A6
MCK	1G6
MI	1A6
RD'	1A5
RESET	1E11
SIORDYA	1B11
SIORDYB	1B11
TC	1A9
TCBUSAK	1C11
TCMREQ	1G5
TCRFSH	1G6
TCRFSH'	1A6
TCWRE	1G7
WR	1A7
OUT 30	1G2
OUT 70	1G2
I/OW	1A10
EOP	1A9
REQ	1A8

IC TYPE	LOCATION	SPARES
7404	L2	2
74LS32	L3	1
	L59	3
74LS74	L61	1
74LS125	L60	1



210 = 209 + 377 OR 378						
210	209	L5-13,18-26, 31-39,45-53	L42	L43	L44	L58
7659-A	7659	377-0345	377-0333	377-0362	377-0348	377-0363
7659-B	7659	377-0345	377-0333	377-0368	378-4235	377-0363
7659-C	7659	377-0345	377-0333	377-0368	378-4219	377-0363

E-REV
2

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL	MODEL NO. 2228D	TITLE	TELECOMMUNICATION CONTROLLER DAUGHTER BOARD
	SEE ENGRG SPECIFICATIONS No.		
FINISH	TOL. AS NOTED	WANG PART NUMBER: SEE CHART	SIZE: D
SCALE	SHT 3 OF 3	DRAWING NUMBER: 7659	REV: 5

END