SPERRY UNIVAC

Buffer Interlace Controller

Model 7X-3102 (F3024-02)

Operation and Service

Mini-Computer Operations

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UP-8626 Rev. 1

SPERRY UNIVAC

PUBLICATIONS REVISION

V70 and V77 Computers

Buffer Interlace Controller Model 7X-3102 (F3024-02) Operation and Service

UP-8626 Rev. 1
(98A 9902 118)

This Library Memo announces the release and availability of Revision 1 of the SPERRY UNIVAC Buffer Interlace Controller Model 7X-3102 (F3024-02) Operation and Service manual, UP-8626 (98A 9902 118). This is a Standard Library Item (SLI).

Revision 1 includes additional information on Direct Memory Access (DMA).

Destruction Notice: This revision supersedes and replaces the original issue of UP-8626 (98A 9902 117), released April 1978, and its Library Memo. Users may destroy all copies of UP-8626 (98A 9902 117) and its library memo.

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		RELEASE DATE April 1981

SPERRY UNIVAC®

BUFFER INTERLACE CONTROLLER
MODEL 7X-3102 (F3024-02)
OPERATION AND SERVICE MANUAL

UP-8628 Rev. 1
98A 9902 118

APRIL 1981

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Printed in U.S.A.

PAGE STATUS SUMMARY

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(98A 9902 118)

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CHANGE RECORD

Change Designation	Issue Date	Change Description
	4-78	Original issue.
Revision 1	4-81	Added Direct Memory Access (DMA) information.

Change Procedure:

When changes are made to this manual, updated pages are issued. These updated pages are either added to this manual or used to replace obsolete pages. The specific pages affected by each change are identified on the PAGE STATUS SUMMARY page.

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SECTION 1
GENERAL DESCRIPTION

The Buffer Interface Controller (BIC) is a special-purpose hardware option for use with SPERRY UNIVAC V70 series and 77 series computers. This manual is divided into six sections:

- Features and specifications
- Installation and interconnection
- Operation
- Theory of operation
- Maintenance
- Mnemonics list

Documents such as logic diagrams, schematics and parts lists are supplied in a system documentation package. This documentation is assembled when the equipment is shipped, and reflects the configuration of a specific system.

There are two versions of the BIC available. One version (without key bits) is for systems that do not have the memory map option and the other version (with key bits) is for systems that do have the memory map option. The BIC with key bits may be used on non-key bit computers such as the V77-200. When used on non-mapped computers, the key bit section of the BIC is inactive.

The BIC enables an I/O device to transfer data in a direct memory access (DMA) mode. DMA operation allows the system to do central processing and I/O operations concurrently. DMA operation frees the processor from performing its programmed I/O functions on a character-by-character basis, so that a block of data may be transferred between memory and an I/O device. The transfer of data on the DMA bus does not alter the processor's operational registers, allowing the processor to continue its operation between DMA bus activity. The impact of BIC DMA activity on overall system performance depends primarily on the type of processor in use. The system reference (or processor) manual for each computer contains information on DMA bus performance, processor latency, and I/O transfer rates.

The BIC can be used on a variety of V70 and V77 processors. Typically, the maximum DMA rate of the processors in these systems exceeds 300,000 words per second. For more detailed information on the DMA rate that a specific processor can attain, refer to the appropriate systems reference (or processor) manual.

The BIC works in conjunction with an I/O controller to initiate and control trap (DMA) requests. Trap requests are used to initiate transfers of data between the computer's main memory and an I/O device. Up to ten peripheral controllers can be connected to one BIC. Using standard I/O device addressing, a computer system can include up to four BICs.

The BIC is considered to be an I/O controller. Priorities for I/O controllers having trap or interrupt capabilities are established by the order of their placement in the priority chain. The BIC is a system priority device. Peripheral controllers connected to a BIC have no system priority of their own, but, while a controller is doing a BIC-controlled DMA transfer, it has the same system priority as the BIC to which it is connected.

Table 1-1 lists the BIC specifications.

Table 1-1. BIC Specifications

Parameter	Description
Organization	Contains input receivers and output drivers, two 16-bit address registers, a 4-bit key register, and a sequence control circuit
Control capability	Up to ten peripheral controllers
I/O transfer rate	Synchronized to peripheral device rate and dependent upon the transfer rates of the processor and the peripheral device. See the systems reference (or processor) manual for the particular V7X processor for details.
I/O signal limits (rise-fall)	Minimum 10 nanoseconds; maximum 100 nanoseconds
Logic levels (internal)	High = +2.4 to +5.0V dc Low = 0 to +0.4V dc
Logic levels (I/O bus)	High = +2.8 to +3.6V dc Low = 0 to +0.5V dc
Size	Contained on one 7-3/4-by 12-inch (19.7 x 30.3 cm) printed-circuit board

(continued)

Table 1-1. BIC Specifications *(continued)*

Parameter	Description
Interconnection	Interfaces with I/O cable through backplane connector; connects to peripheral controllers through the backplane connector or through a cable
Connectors	One 122-terminal card-edge connector (mates with female connector at backplane) and two 44-terminal card-edge connectors (each mates with a 44-terminal connector on B cable for special configurations)
Power	+5V dc at 0.6A
Operating environment	0 to 50 degrees C, 10 to 90 percent relative humidity without condensation

SECTION 2
INSTALLATION

The BIC has been packed and inspected to ensure its arrival in good working order. To prevent damage, take care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. If damage exists:

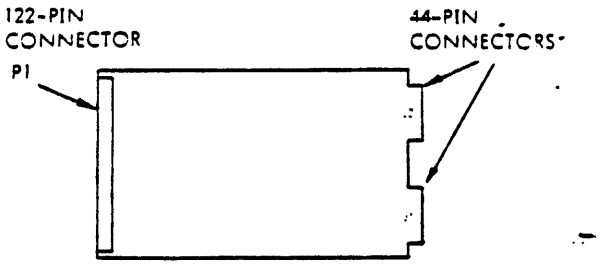
- Notify the transportation company
- Notify Sperry Univac
- Save all packing material

2.1 PHYSICAL DESCRIPTION

The BIC circuits are contained on a single printed-circuit (PC) board (p n 44P0689). As illustrated in figure 2-1, the board contains three connectors P1, J1, and J2. Connectors J1 and J2 are wired in parallel and contain the peripheral control lines. Connector P1 also contains the same peripheral control lines as well as all I/O bus control signals for the BIC. Connectors J1 and J2 are used for special configurations.

2.2 INTERCONNECTION

When two or more BIC controllers are installed in the same chassis, the B cable signals are connected only to the controller or controllers with which each BIC communicates. There are no B cable signals between BICs. If the BIC and the peripheral controllers are installed in different chassis, the interconnection is made through the J1 and J2 connectors. Figure 2-2 illustrates BIC/peripheral interconnections. B cables are required for those signals required to implement the DMA function.



* CONNECTORS J1 AND J2 ARE PARALLEL WIRED

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Figure 2-1. BIC Board (Component Side)

2.3 INTERFACE DATA

All BIC input/output signals utilize receiver/driver stages to buffer internal circuits and external lines. The BIC interfaces with the computer via the "—I" signal lines and with peripheral controllers via the "—B" signal lines listed in table 2-1. The corresponding pin number of circuit card edge connector P1 follows each signal mnemonic (see logic diagram 91C0459). Refer to section 6 for definitions of the mnemonics.

Table 2-1. BIC Inputs and Outputs

INPUTS				OUTPUTS			
BCDX-B	52	EB10-I	16	DCEX-B	56	EB12-I	18
BIMES-I	93	EB11-I	17	DESX-B	60	EB13-I	19
CDCX-B	54	EB12-I	18	EB00-I	2	EB14-I	20
DRYX-I	29	EB13-I	19	EB01-I	4,68,69*	EB15-I	21
EB00-I	2	EB14-I	20	EB02-I	6,71,72	INTX-	75
EB01-I	4,65	EB15-I	21	EB03-I	8	IOK1-I	109
EB02-I	6,70	FRYX-I	27	EB04-I	10	IOK2-I	110
EB03-I	8	IUAX-I	44	EB05-I	11	IOK3-I	112
EB04-I	10	IUCX-I	45	EB06-I	12	IOK4-I	113
EB05-I	11	PRMX-I	37	EB07-I	13	PRNX-I	42
EB06-I	12	SYRT-I	43	EB08-I	14	SERX-I	31
EB07-I	13	TROX-B	50	EB09-I	15	TAKX-B	58
EB08-I	14	TRQX-B	49	EB10-I	16	TPIX-I	33
EB09-I	15			EB11-I	17	TPOX-I	35

NOTE: On systems with memory map, the BIMES-I and BTMES-I signals are floating and must be pulled up to +5 volts by adding the following jumpers:

a. On each backplane slot, pin 93 (BIMES-I) is connected to pin 73 (PRMY-I).

b. On each PMA/BTC backplane slot, pin 96 (BTMES-I) is connected to pin 73 (EXPU+).

Many peripheral controllers, under software control, can transfer data either by programmed I/O or via BIC control. Controllers for peripherals such as discs and drums usually are not able to transfer data via programmed I/O due to their high transfer rates. Figure 2-3 shows a computer system with peripheral controllers that operate with and without BIC. Figure 2-4 is typical interface logic.

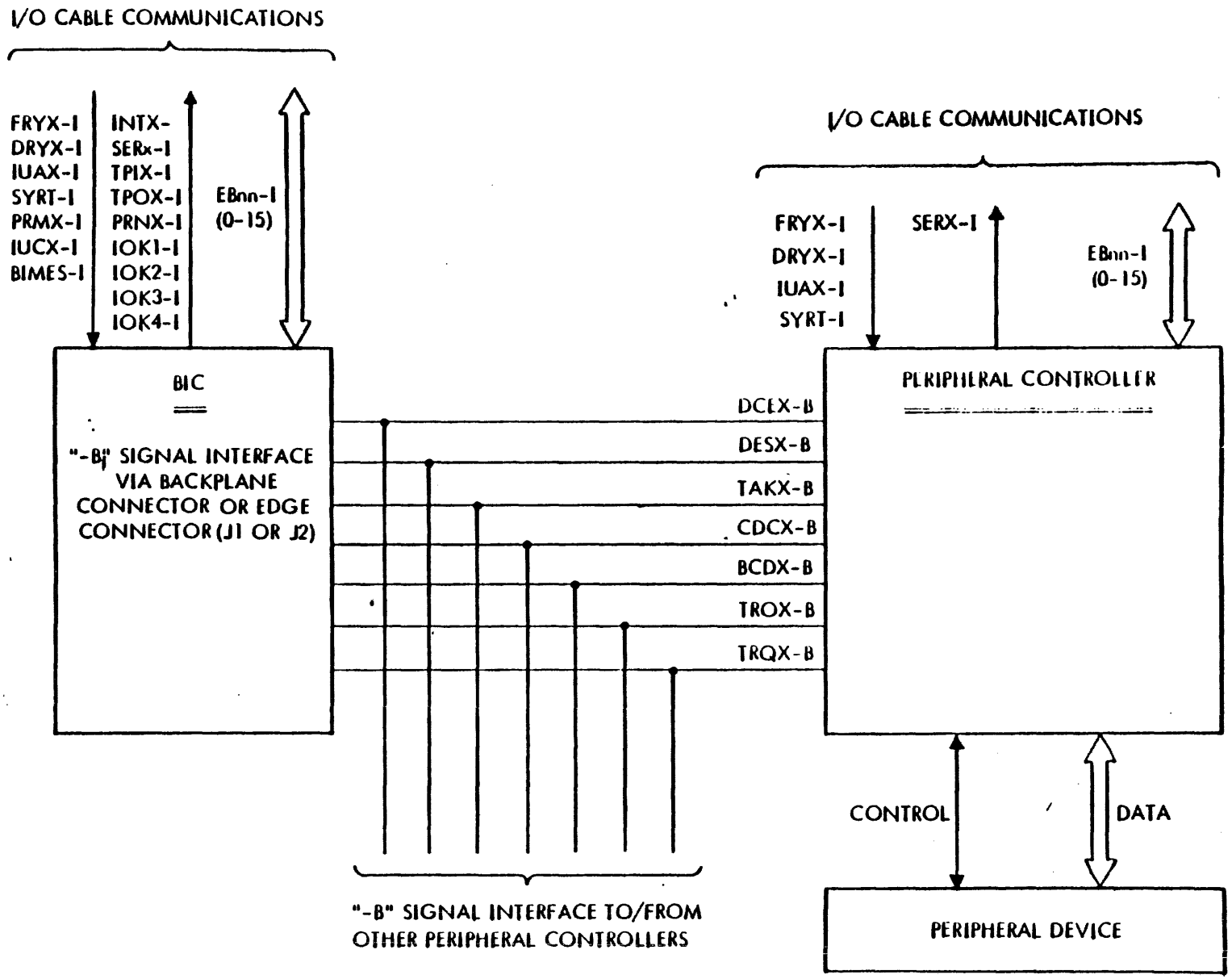

Figure 2-2. BIC Peripheral Controller Interface

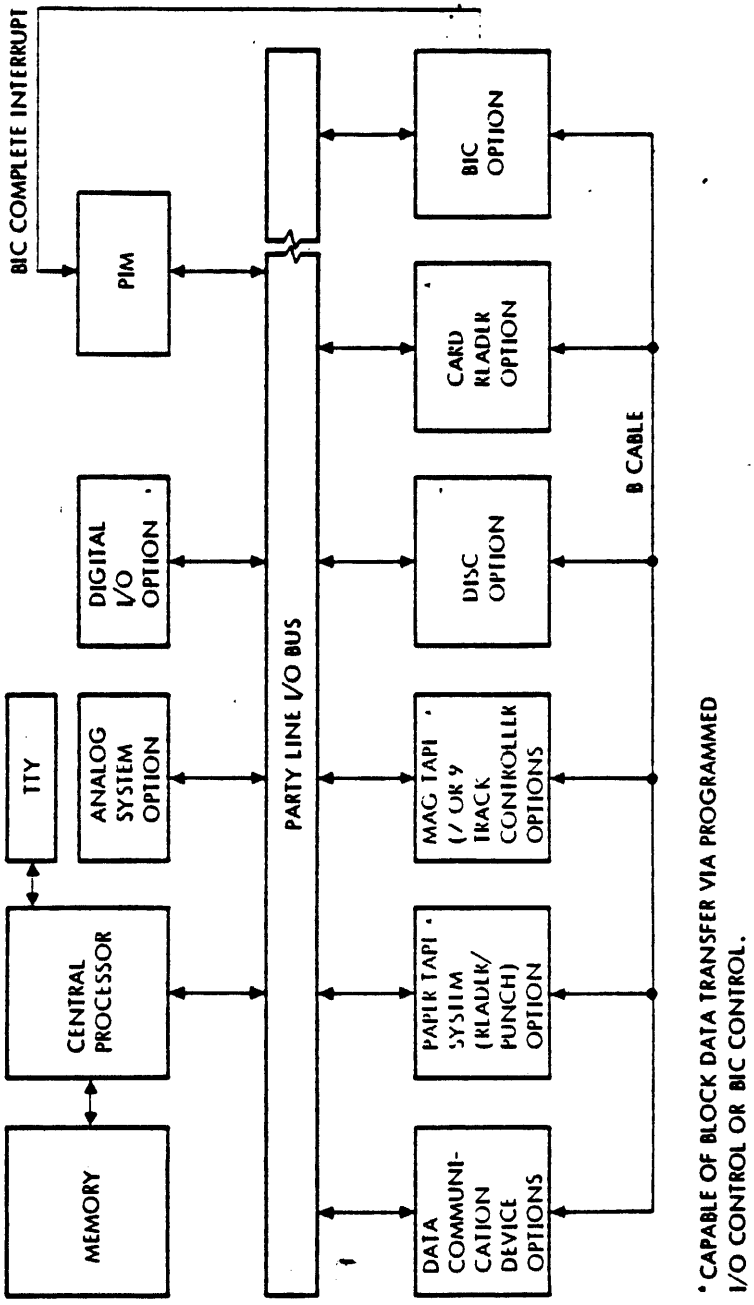

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Figure 2-3. Interface for Peripheral Devices with and

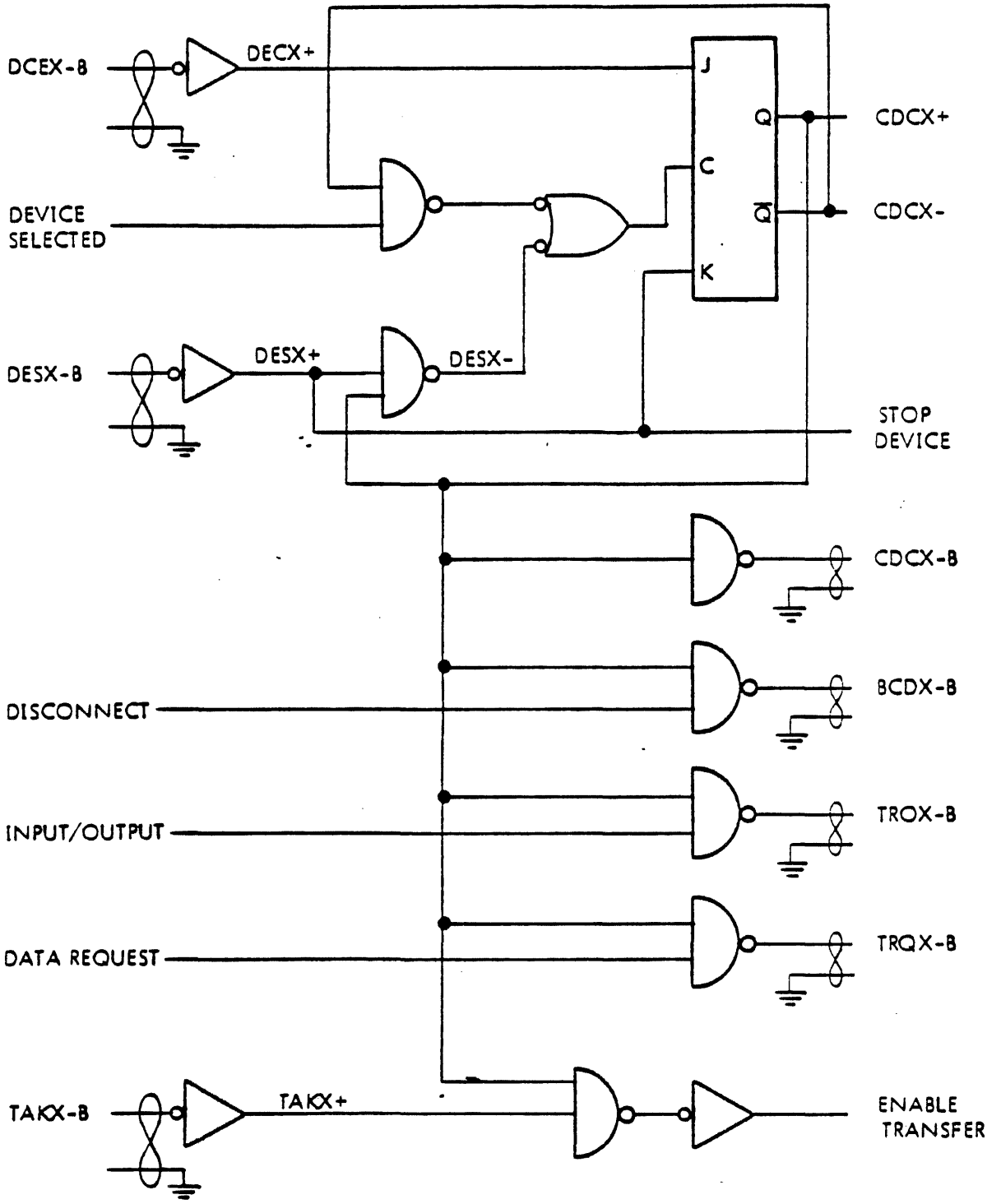

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Figure 2-4. Typical B Cable Interface Logic

SECTION 3
OPERATION

The BIC has no operating controls or indicators. It operates under program control.

3.1 I/O INSTRUCTIONS

The BIC responds to the instructions listed in table 3-1. Two device addresses are assigned to each BIC to differentiate functions directed by the I/O instruction. Addresses 020 through 027 are reserved for BICs. Address/instruction codes in table 3-1 are for the first BIC in a system. If additional BICs are installed, the addresses shown should be incremented by two for each additional BIC (i.e., second BIC addresses should be 022 and 023).

Table 3-1. I/O Instructions

Mnemonics	Octal Code	Description
		External Control
EXC 020	100020	Activate BIC
EXC 021	100021	Initialize
EXC 0321	100321	Enable loading of key bits
		Transfer
OAR 020	103120	Load initial register from A
OBR 020	103220	Load initial register from B
OME 020	103020	Load initial register from memory
OAR 021	103121	Load final register from A
OBR 021	103221	Load final register from B
OME 021	103021	Load final register from memory
INA 020	102120	Read initial register into A
INB 020	102220	Read initial register into B
IME 020	102020	Read initial register into memory
CIA 020	102520	Read initial register into cleared A
CIB 020	102620	Read initial register into cleared B
		Sense
SEN 020	101020	Sense BIC not busy
SEN 021	101021	Sense abnormal device stop
SEN 0121	101121	Senses if BIC has been stopped due to a memory-map error

3.2 PROGRAMMING CONSIDERATIONS

The user writes the programs that use the BIC. When preparing a program for use with the BIC, the programmer first initializes then senses the status of the BIC and the selected peripheral controller. After a not-busy response is received from both the BIC and the peripheral controller, the BIC address registers are loaded with the initial and final memory addresses of the block of data to be transferred, a BIC activate enable instruction is placed on the I/O cable, and the transfer is started. Although the program requires loops for use with sense instructions and to handle abnormal conditions, transfer of the data block is accomplished by the BIC without further program instructions.

The key bit register (for memory map option) is loaded by first issuing the "Enable (loadingof) Key Bit Register" instruction (0100321) followed by one of the "Load Final Register" instructions (0103021, 0103121, 0103221).

3.3 SAMPLE PROGRAM

Table 3-2 shows a typical service routine for the BIC, a Teletype paper tape punch operation under BIC control. Using DAS symbols with corresponding machine language

Table 3-2. Typical Service Routine

Memory Location	Octal Code	Label	Operation	Variable Field	Comments
001000			,ORG	,01000	
001000	101020	BIC0	,SEN	,020,BIC1	CK BIC NOT BUSY
001001	001007 R				
001002	100401		,EXC	,0401	INIT TTY
001003	100021		,EXC	,021	INIT BIC
001004	005000		,NOP	,	
001005	001000		,JMP	,*-3	

(continued)

Table 3-2. Typical Service Routine *(continued)*

Memory Location	Octal Code	Label	Operation	Variable Field	Comments
001006	001002 R				
001007	101101	BIC1	,SEN	,0101,BIC2	CK TTY WRITE READY
001010	001014 R				
001011	005000		,NOP	,	
001012	001000		,JMP	,*-3	
001013	001007 R				
001014	103120	BIC2	,OAR	,020	SET BIC I REG
001015	103221		,OBR	,021	SET BIC F REG
001016	100020		,EXC	,020	ACTIVATE BIC
001017	100101		,EXC	,0101	CONNECT WRITE REG
001020	101020		,SEN	,020,BIC3	CK BIC NOT BUSY
001021	001025 R				
001022	005000		,NOP	,	
001023	001000		,JMP	,*-3	
001024	001020 R				
001025	101021	BIC3	,SEN	,021,BIC5	CK ABN STOP
001026	001032 R				
001027	007400		,ROF	,	
001030	102520	BIC4	,CIA	,020	INPUT BIC I REG
001031	000000		,HLT	;	
001032	007401	BIC5	,SOF	,	SET ABN FLAG
001033	001000		,JMP	,BIC4	
001034	001030 R				
	000000		,END	,	

octal codes. the program covers memory locations 01000 through 01034.

Once the program is loaded. the operator must insert the initial punch buffer address into the A register and the final address into the B register for each run. When started. the program will:

a. initialize the BIC and Teletype punch

b. initiate the data transfer.

c. read the contents of the BIC initial register into the A register at the completion of the transfer

d. set the overflow indicator if the termination was abnormal

e. halt

The punch buffer must contain only ASCII characters. The first character is 0222 (punch on) and the last is 0224 (punch off).

SECTION 4
THEORY OF OPERATION

The BIC is functionally divided into address registers and a sequence control circuit (figure 4-1). A functional description of these circuits is provided in the following paragraphs.

4.1 ADDRESS REGISTERS

The two address registers contain the memory locations of output or input data, depending on the I/O instruction. The initial register stores the address of the first input or output word, and is incremented during each data-word transfer. When the block transfer is complete, the initial register contains the address + 1 of the last data word to be transferred.

The final register stores the address of the last word to be transferred. Unless the peripheral device is abnormally stopped, the address in the final register will be one less than the address in the initial register when the block transfer is complete. When the initial and final registers reach comparison, the block word transfer is complete.

The key-bit register stores the four key bits that are used with the memory map. The key-bit register is not used on systems without the memory map. The enable instruction sets a flip-flop which directs the data being transferred by a load (of final register) instruction, into the key-bit register. The flip-flop is reset when the transfer is complete.

4.2 SEQUENCE CONTROL

The sequence control circuit generates the control signals which coordinate address and data transfer between the processor, BIC, and the peripheral controllers. The data are not routed through the BIC but are directly transferred between the peripheral controller and memory.

Under program control, the processor senses that the BIC is not busy and prepares the BIC to receive the initial and final data addresses. The processor then senses that the selected peripheral controller is not busy and loads the initial and final registers and the key register. The BIC is then activated and the peripheral controller is started. The BIC then assumes control of the data transmission, allowing the processor operational registers to be used by the program for other functions.

Data transfer is accomplished between memory and the peripheral controller via the I/O bus. The BIC counts the words transferred and when the data block transfer is complete, disconnects the peripheral controller and assumes a not-busy state. Data transfer may also be terminated upon request from the peripheral controller.

4.3 OPERATING SEQUENCE

The following paragraphs describe the sequence of operations of the BIC. Refer to the block diagram (figure 4-1), the timing diagram (figure 4-2), and the logic diagram 91C0459.

4.3.1 Initial Conditions

The processor senses the BIC for a not-busy condition. The sense instruction places the BIC device address and a function code on the I/O bus. The BIC responds with a low SERX-I if it is not busy (CDCX-B low). The processor then executes the initialize instruction which generates a low INIT- which prepares BIC for receiving the initial and final addresses of the block data to be transferred.

The initial register is loaded from the I/O bus when the processor issues the "load initial register" command. (See Table 3-1.)

The final register is loaded from the I/O bus when the processor issues the "load final register" command (see Table 3-1).

4.3.2 Device Selection

The processor executes the activate BIC instruction which causes DCEX-B to go low. This signal is sent to all peripheral controllers connected to the BIC. The processor then executes an instruction to select a peripheral device. This instruction with DCEX-B low, connects the selected device to the BIC and starts the device.

The connected peripheral controller sends a low CDCX-B to the BIC causing DCEX-B to go high, thus disabling the selection of any other peripheral controllers. When CDCX-B goes low, the connected peripheral controller also selects the state of TROX-B. When data is to be transferred to memory, a high TROX-B is sent. If data is to be transferred from memory, a low TROX-B is sent.

4.3.3 Data Address

When the connected peripheral controller is ready for the data transfer, it sends a low TROX-B to the BIC. The BIC then sends a TPIX-I or low TPOX-I to the processor, depending on the state of TROX-B.

When the processor is ready for the data transfer, it sends a low IUAX—I to the BIC. IUAX—I going low generates a low TAKX—B which is sent to the peripheral controller to initiate the transfer. The BIC then causes OIRX + to go high which gates the memory address, that is in the initial register plus the key bits onto the I/O bus. The connected peripheral controller is thus enabled. FRYX—I, from the processor, going high terminates the address phase of the BIC. FRYX—I going high causes CLEX— to go high, which

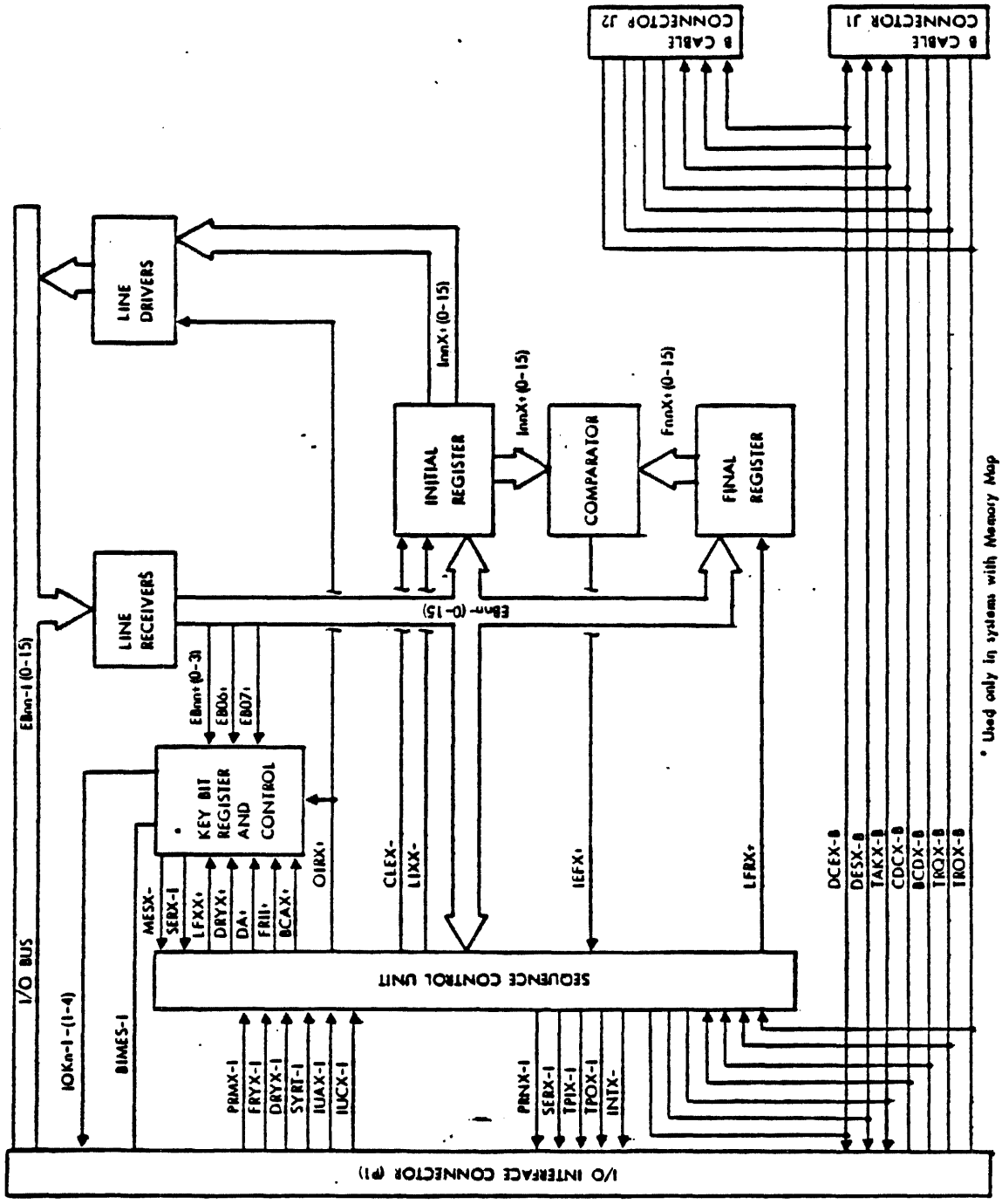

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Figure 4-1. BIC Block Diagram

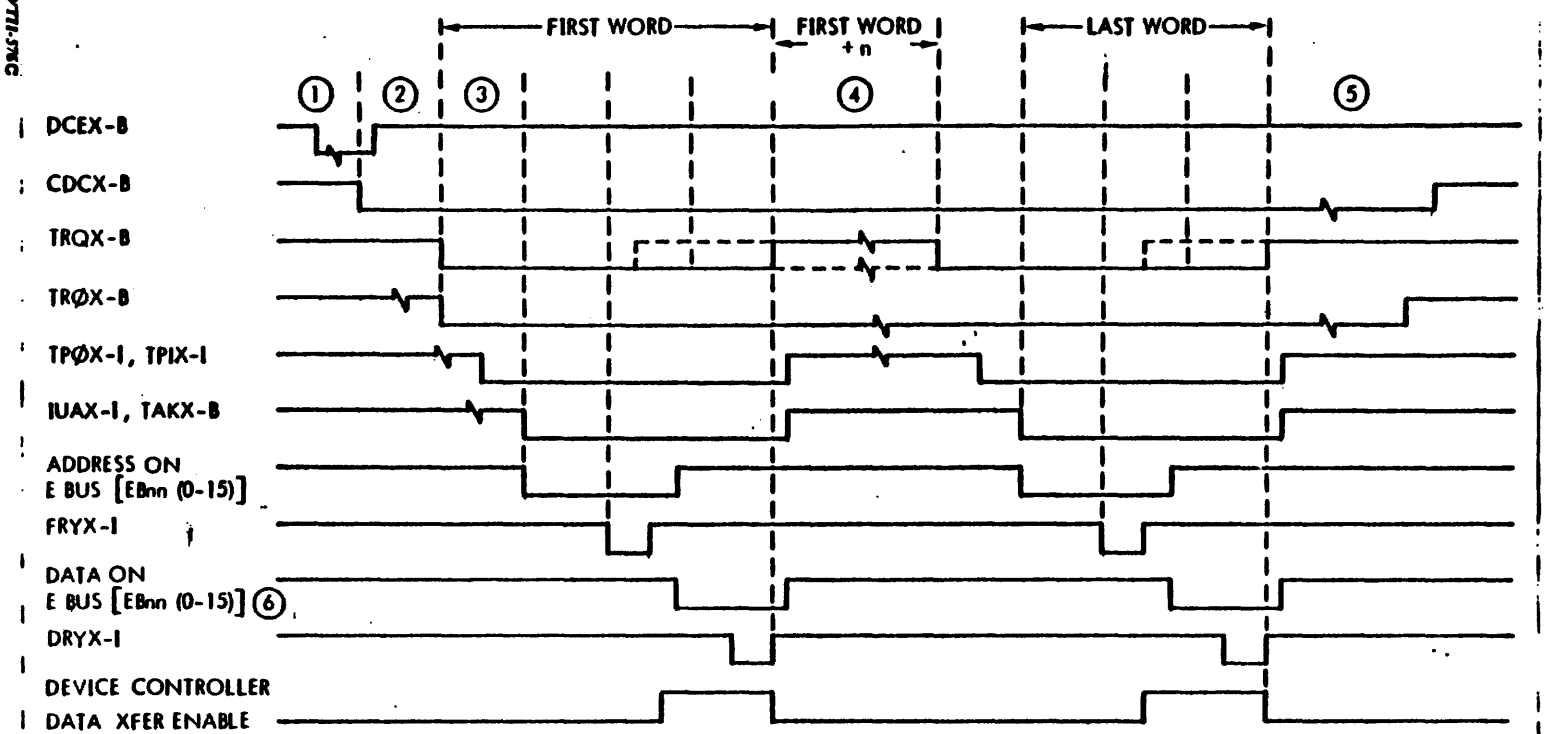


Figure 4-2. BIC Trap Sequence Timing

NOTES:

1. TIMING REQUIRED TO ISSUE THE COMMAND TO CONNECT THE DEVICE.
2. TIME REQUIRED FOR DEVICE TO REQUEST FIRST DATA TRANSFER AFTER STARTING.
3. TIME REQUIRED TO SERVICE CURRENT AND/OR HIGHER PRIORITY REQUESTS FOR I/O ACCESSES.
4. SIGNAL TRQX-B MAY BE BROUGHT LOW (TRUE) AGAIN, AS EARLY AS THE TRAILING EDGE OF DRYX-I. HOWEVER, SIGNAL TRQX-B MUST HAVE BEEN HIGH FOR AT LEAST 50 NANOSECONDS BEFORE GOING LOW.
5. END OF DATA BLOCK. SIGNAL CDCX MAY REMAIN HIGH BETWEEN BLOCKS.
6. INCLUDES KEY BITS IF PRESENT [IOKn-I (0-3)].
7. FOR DMA TIMING REFER TO THE APPLICABLE SYSTEM HANDBOOK.

causes the initial register to be incremented to the next memory address.

4.3.4 Data Transfer

The data transfer may be an output from or an input to the processor. For output, the processor places the data on the I/O bus, and the data is strobed into the peripheral controller by DRYX-I going high. For input, the peripheral controller places the data on the I/O bus when FRYX-I goes high and removes the data when DRYX-I goes high. BIC keeps TAKX-B low until the end of the transfer when IUAX-I goes high.

4.3.5 Transfer Termination and Interrupt

When the contents of the initial and final registers become equal, the comparator circuit generates a high IEFX—. This creates a low DESX—B which is sent to the peripheral controller. The peripheral controller then causes CDCX—B to go high. This causes the BIC to assume a not busy state. The transfer of data is thus terminated.

When an abnormal device stop occurs, the peripheral controller terminates the transfer without regard to the contents of the initial and final registers. The peripheral controller generates a low BCDX—B. This causes a low DESX—B to be sent to the peripheral controller. The peripheral controller responds with a high CDCX—B. This causes the BIC to assume a not busy state. The transfer of data is thus terminated. After an abnormal device stop, the processor can read the contents of the initial register to determine the number of words that were transferred. The number in the initial register will be the address of the last word transferred plus one.

An abnormal device stop can occur as a result of any of the following situations: the length of the data block is unknown, and the device has detected the end of the data; the peripheral controller has detected an invalid operation of the device; the processor has issued an instruction to stop the operation of the peripheral device.

Another abnormal stop is created when an error is detected by the memory map during a BIC operation. The error causes BIMES—I to go low. This causes a low DESX—B to be sent to the peripheral controller. The peripheral controller responds with a high CDCX—B. This causes the BIC to assume a not busy state. The transfer of data is then terminated.

When the BIC goes to a not busy state, either from a normal termination or from an abnormal device stop, an interrupt signal (INTX) is generated. When signal INTX goes low, the signal at Pin 75 on P1 connector also goes low. This signal is normally wired to an interrupt port of a Priority Interrupt Module (PIM). This interrupt is normally referred to as "BIC Complete". "BIC Complete" signifies to the processor program that the DMA transfer has been completed. The processor program then verifies that the transfer completion was either normal or abnormal. If the "BIC Complete" was caused by an abnormal condition, the processor program takes the steps that are necessary to recover from the abnormal situation. If the "BIC Complete" was normal, the processor could then set up the next DMA transfer and continue operation.

SECTION 5
MAINTENANCE

Maintenance personnel should be familiar with the contents of this manual before attempting to troubleshoot the BIC. The MAINTAIN II test program system (Test Programs Manual, 98 A 9952 06x)* contains a BIC test program used to test various phases of the BIC operation. Further diagnosis can then be made by referring to this manual.

5.1 TEST EQUIPMENT

The following test equipment and tools are recommended for maintenance:

a. Oscilloscope, Tektronix type 547 with dual-trace plug-in unit, or equivalent.

b. Multimeter, Triplett type 630 or equivalent.

c. Soldering iron, 39-watt pencil type.

d. Card extender VDM p/n 44P0540.

*The x at the end of the document number is the revision number and can be any digit 0 through 9.

5.2 CIRCUIT-COMPONENT IDENTIFICATION

All reference designations used in the logic diagram appear on the BIC board adjacent to each component. Component part numbers can be found in the parts list in volume 2.

5.3 CIRCUIT-BOARD REPAIR

If it has been determined that circuit-board repair is required, it is recommended that the Sperry Univac customer service department be contacted so that a new circuit board can be installed in the user's system and the faulty one returned to the factory for repairs. However, if the user decides to perform his own repairs, caution should be used so that the circuit board is not permanently damaged. Approved repair procedures should be followed such as the ones described in document IPC-R-700A prepared by the Institute of Printed Circuits.

SECTION 6
MNEMONICS

Table 6-1 provides an alphabetized list of the signal mnemonics used in the BIC.

Table 6-1. Mnemonics

Mnemonic	Description
ACEX	Activate enable. Stores activation of BIC.
ADSX	Abnormal device stop. Stores end of data from peripheral controller
BCAX	Buffer controller activate. Stores the activation of the BIC and the peripheral controller.
BCDX	Buffer controller deactivate. Initiates termination of data transfer by the peripheral controller.
BIMES	BIC map error stop. Stores the map error indication during a BIC operation.
CARx	Carry out. Increments the next higher position of the initial register on overflow.
CDCX	Controller device connected. Indicates that the peripheral controller to be connected is connected.
CLEX	Clock enabled. Enables the initial register to be incremented.
DA	Device address decode. Gates the device address from the I O bus.
DCEX	Device connect enable. Enables the selection of a peripheral device.
DESX	Device stop. Stores the requirement to stop the peripheral device.
DRYX	Data ready. Indicates the I O bus contains a word of data.
DSTX	Device stop enable. Stores the end of the data transfer.
EBii	E-bus bit. Address or function code bits from the I O bus.
EKBR	Enable loading of key bit register. Gates the key bits into the key-bit register.
FRYX	Function ready. Indicates the I/O bus contains an address.
FiiX	Final register bit. Stores bit ii of the final address.
IEFX	Initial equals final. Indicates that the contents of the initial register is equal to the contents of the final register.
IFMX	Initial equals final memory. Clears the BIC active flip-flop when the contents of the initial register is equal to the contents of the final register.
INIT	Initialize. Resets BIC flip-flops to their initial condition.
INTX	Interrupt request. Used to generate an interrupt signal to a Priority Interrupt Module (PIM) when a block transfer is complete. INTX occurs for either normal or abnormal transfer completions.
IOKi	Key-bit register output i to I/O bus.
IUAX	Interrupt acknowledge. Indicates that the processor is ready to send or receive data.
IUCX	Interrupt clock. Provides timing for servicing BIC.
IiiX	Initial register data bit. Stores bit ii of the initial address.
LFRX	Load final register. Loads data on I/O bus into final register.
LFXX	Load final. Gates the I/O bus contents into the key-bit register when EKBR is set.
LIXX	Load initial register. Loads data on I/O bus into initial register.
MESX	Map error stop. Indicates that there was a memory map error during a BIC operation.

(continued)

Table 6-1. Mnemonics *(continued)*

Mnemonic	Description
OIRX	Output initial register. Gates contents of initial register and key-bit register onto the I O bus.
PLUP	Pullup voltage.
PRMX	Priority in. Gives priority to BIC.
PRNX	Priority out. Passes priority to next in line after BIC is serviced.
RIXX	Read initial register. Stores requirement of processor to read contents of initial register.
RTPD	Reset trap detect. Resets the trap request detection flip-flop.
SERX	Sense response. Indicates whether the BIC is busy.
SYRT	System reset. Generates initialize signal when SYSTEM RESET is pressed.
TAKX	Trap acknowledge. Indicates that the requirements for data transfer have been met.
TCOX	Trap command. Synchronizes trap request with interrupt clock.
TPDX	Trap request detect. Detects the peripheral controller request for a trap.
TPIX	Trap in. Indicates that the BIC is ready to transfer data to the processor.
TPOX	Trap out. Indicates that the BIC is ready to transfer data from the processor.
TROX	Trap out (from peripheral). Indicates the direction (in or out) of the data transfer.
TRQX	Trap request. Indicates that the peripheral controller is ready for a data transfer.

S.O.454618 Rev.00
Maintenance Documentation Set
F-3024-02

Buffer Interlace Controller

F3024-02

0101563-001	Buffer Interlace Controller
66P0191	Buffer Interlace Cont. Assy.
66D0191	Buffer Interlace Cont. Assy.
6600187	Logic Diagram
9809902-118	Buffer Interlace Manual

SPERRY UNIVAC PARTS LIST

SPERRY UNIVAC IS A DIVISION OF SPERRY CORPORATION

MFG CODE	ISSUE DATE	CONTROL		DOC NO.	AC	SHEET
J ,W	81/03/03	W 777	PL	W0101563	8	1

TITLE	PCC	ADC	PCD	COMM CODE	CA	U/M	ST	TYPE	SIZE	CLASS
BIC OPTION ASSEMBLY						EA	A	M	A	A

FIND NO.	QUANTITY REQUIRED		U/M	PCC	PART OR IDENT NO. DOCUMENT NO.	PART OR IDENT NO. DASH	EIR AND PART DESCRIPTION INFORMATION	ECC	ST	CHG
Z006					W 94616	-02	PL REV F, PIC REV E, RANGE 00 - 01 EIR RELEASED 81/03/03			*
Z005					W 94295	-01	PL REV E, PIC REV E, RANGE 00 - 01 EIR RELEASED 80/06/18			
*****	*******	***	**	*	**********	****	********** COMMON DATA **********			
8001			X		8W01163	-00	MARKING,MECHANICAL SPECS DSGN=F/GENERAL IDENTIFICATION		A	
8002			X		8W00115	-00	CMPTR COMPS W/FEATURE NUM SPEC TEST=F3024=02 BUFFER CONT		A	
8003			X		8W00190	-00	CMPTR COMPS W/FEATURE NUM SPEC DSGN=F3024=02 BUFFER CONT		A	
*****	*******	***		*	**********	****	WITHOUT KEY BITS VAR DATA PART = 00 *********		A	
1	1		EA		W4400689	-00	PC ASSEMBLY - BIC DM402 BASIC (PLASTIC IC'S)		A	
*****	*******	***		*	**********	****	WITH KEY BITS VAR DATA PART = 01 *********		A	
2	1		EA		6600191	-01	PC ASSEMBLY-BIC REWORK 6600191-00/ W 94616-02		A	*

DWG NO. W010 3

REVISIONS

REV	EIR	CHG CODE	DESCRIPTIONS	DR	APPD
C	W87436 -02		SHT. 3 NOTES 9 & 10 ADDED BIC P/N 6600191 RELEASED PER EIR W87436-02	PB	
D	W94124-01		SEE EIR	CN	
E	W94295-01		CHANGED PER EIR.	DL	

TABULATION BLOCK

PART NO.	FEATURE NO.	DESCRIPTION	USED ON
W0101563- 00	-	BIC (W/O Key Bits) (DM402)	620/i, 620/L, 620/L-100, 620/f, 620/f-100, V7X (W/O Memory Map)
W0101563- 01	F3024-02	BIC Wtih Key Bits (DM402	V7X W/O Memory Map (See Note 12)

PART NO. SEE TABULATION BLOCK
IDENT NO. -

FOR MATL REQUIREMENTS SEE PL
PL REV LETTER CONTROLS DOCUMENT.

NEXT ASSEMBLY

MODEL NO.

SPERRY UNIVAC

DR		
CHK	R. JORDAN	6/20/73
ENGR	T.E. HANSON	6/21/73
APPD	A. WHITCOMB	6/21/73
APPD		

CODE IDENT NO. 21101

TITLE OPTION ASSY, BUFFER INTERLACE CONTROLLER (BIC)

SIZE	DWG NO.	REV
A	W010 1563	E

SHEET 1 OF 9

NOTES: (SEE NOTE 14 FOR INTEGRATION INTO V77 'S' SLOT CONNECTOR PLANE)

1. This drawing provides the BIC (w/o Key Bits) and the BIC with Key Bits for controlling DMA block transfers to/from peripheral controllers. (Reference tabulation block, page 1.)

2. The standard configuration is with the BIC and the associated controller located in the same expansion chassis. Reference Figure 1 for installation and interconnection information.

3. The non-standard configuration is shown in Figure 2 for reference. The edge connector, B-Cable, and termination resistors are not supplied with the BIC.

4. Connect BIC in priority chain per Systems Memo:
   Priority In (PRMX-1) - Pin 37
   Priority Out(PRNX-1) - Pin 42

~~5. Add jumpers to groundplane on BIC slot to select the desired standard device address as shown in Table 1.~~

~~For non-standard device address, add wires to groundplane per Table 1 and perform etch cuts and add jumpers to BIC assy per Table 2.~~

5.0 Use tables 1 through 5 for standard and non-standard device address selection.

5.1 For BIC P/N W4400026 use table 1. Install jumpers on I/O backplane.

5.2 For BIC P/N W4400689 use tables 2 and 3. Install jumpers on I/O backplane for standard address. Cut etch and add jumpers on BIC assy. For non-standard.

5.3 For BIC P/N 6600191 use tables 4 and 5. This BIC does not require I/O backplane jumpers. Address selection is accomplished by on-board switches.

TABLE 1

DEVICE ADDRESS	ADD JUMPER FROM		
	PIN 65 TO	PIN 70 TO	GROUND TO
020,021	69	72	
022,023	68	72	69
024,025	69	71	72
026,027	68	71	69,72

TABLE 2 (WAS 1)

DEVICE ADDRESS (OCTAL)		ADD JUMPER FROM	
STANDARD	NON-STANDARD	PIN 65 TO	PIN 70 TO
020,021	0X0, 0X1	Pin 69	Pin 72
022,023	0X2, 0X3	Pin 68	Pin 72
024,025	0X4, 0X5	Pin 69	Pin 71
026,027	0X6, 0X7	Pin 68	Pin 71

X= 0, 1, 3, 4, 5, 6, 7

TABLE 3 (WAS 2)

NON-STANDARD DEVICE ADDRESS (OCTAL)	CUT ETCH ON BIC ASSY BETWEEN POINTS			ADD JUMPER ON BIC ASSY BETWEEN POINTS		
00 Z	-	E4 & E5	-	-	E5 & E6	-
01 Z	E7 & E8	E4 & E5	-	E8 & E9	E5 & E6	-
03 Z	E7 & E8	-	-	E8 & E9	-	-
04 Z	-	E4 & E5	E2 & E3	-	E5 & E6	E1 & E2
05 Z	E7 & E8	E4 & E5	E2 & E3	E8 & E9	E5 & E6	E1 & E2
06 Z	-	-	E2 & E3	-	-	E1 & E2
07 Z	E7 & E8	-	E2 & E3	E8 & E9	-	E1 & E2

Z = 0 or 1, 2 or 3, 4 or 5, 6 or 7

(ADD) TABLE 4

LOCATION	E7	B4	DEVICE
SWITCH	S1	S1	ADD
POSITION	A	A	X0, X1
	A	B	X2, X3
	B	A	X4, X5
	B	B	X6, X7

(ADD) TABLE 5

LOCATION	E7			DEVICE
SWITCH	S4	S3	S2	ADD12
	A	B	A	2X
	A	B	B	3X
	B	A	A	4X
	B	A	B	5X
	B	B	A	6X
	B	B	B	7X

6. If option is to be shipped for customer installation, package in suitable container and mark container with the following information:

BIC (w/o Key Bits) (or "BIC with Key Bits" when applicable)

W0101563-(Applicable Dash Number and Revision Letter)

7. Test Specification W00115

Design Specification SW00190

8. ~~Add no jumpers to Pin 69 and/or Pin 72 for device address wiring on BIC Slot(s) of I/O Groundplane.~~

9. ~~To replace an old BIC W4400026 with a new BIC, P/N 6600191 or W4400689, remove any connection on I/O groundplane, PIN 69 and/or 72(Only).~~

10. ~~To replace a new BIC P/N 6600191 or W4400689 with an old BIC P/N W4400026.~~

a. ~~Whenever Pin 65 is connected to Pin 68, then at Pin 69 add ground.~~

b. ~~Whenever Pin 70 is connected to Pin 71, then at Pin 72 add ground.~~

11. In systems without memory map add the following jumper to each slot in which a W0101563- 01 BIC is to be installed:

Pin P1-93 (BIMES-I) to Pin P1-73 (PRMY-I)

In systems with memory map the BIMES-I signal string must be terminated on the associated I/O System Term Shoe. ALTERNATIVELY SEE NOTE 14.6.

12. The W0101563- 01 version may be used on all 620 and V73 Systems, with and without memory map, by terminating Pin 93 BIMES-I per Note 11, above.

13. Jumper +5V from connector plane pin 118 to pin 115 to provide pull up bias for BIC control bus signals.

14.0 Connector plane W/W for V77 'S' slot

14.1 The standard configuration is for the BIC and the associated controllers to be located in the same connector plane. When this is unsatisfactory, the 'B' bus (BIC control bus) will have to be wire wrapped between two connector planes or other special cabling may be required such as in Figure 2.

14.2 Connect BIC in priority chain per systems memo. In V77-400/200 systems use data transfer chain labeled PXFR- at pin 59 of J1, J2 on the backplane.

14.3 Perform address wiring per Note 5.

14.4 Perform Note 13 for bias.

14.5 Perform Note 11 for systems without map.

14.6 Systems with map

The V70 mega map modified to drive BIMES on 10K4-1 and receive 10K4-1 on the same line. In standard universal plane nomenclature this signal is EB19-1 at pin 22 of the J1-2 connectors of the backplane. The 'S' plane wiring old and new nomenclature are given in table 8.

14.7 Use twisted pair wire wrap for notes 14.2 and 14.6.

15.0

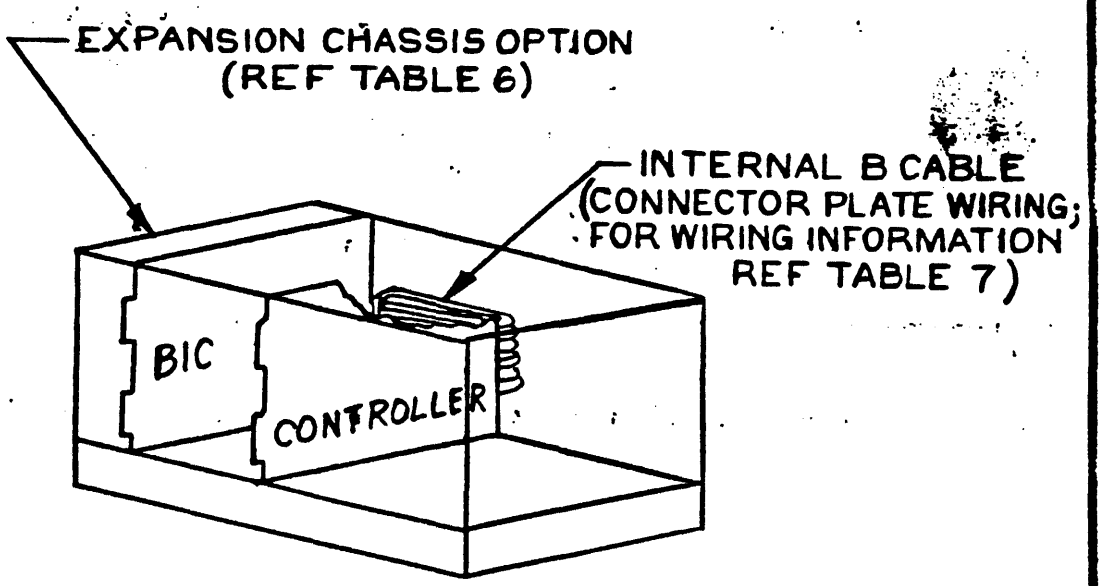
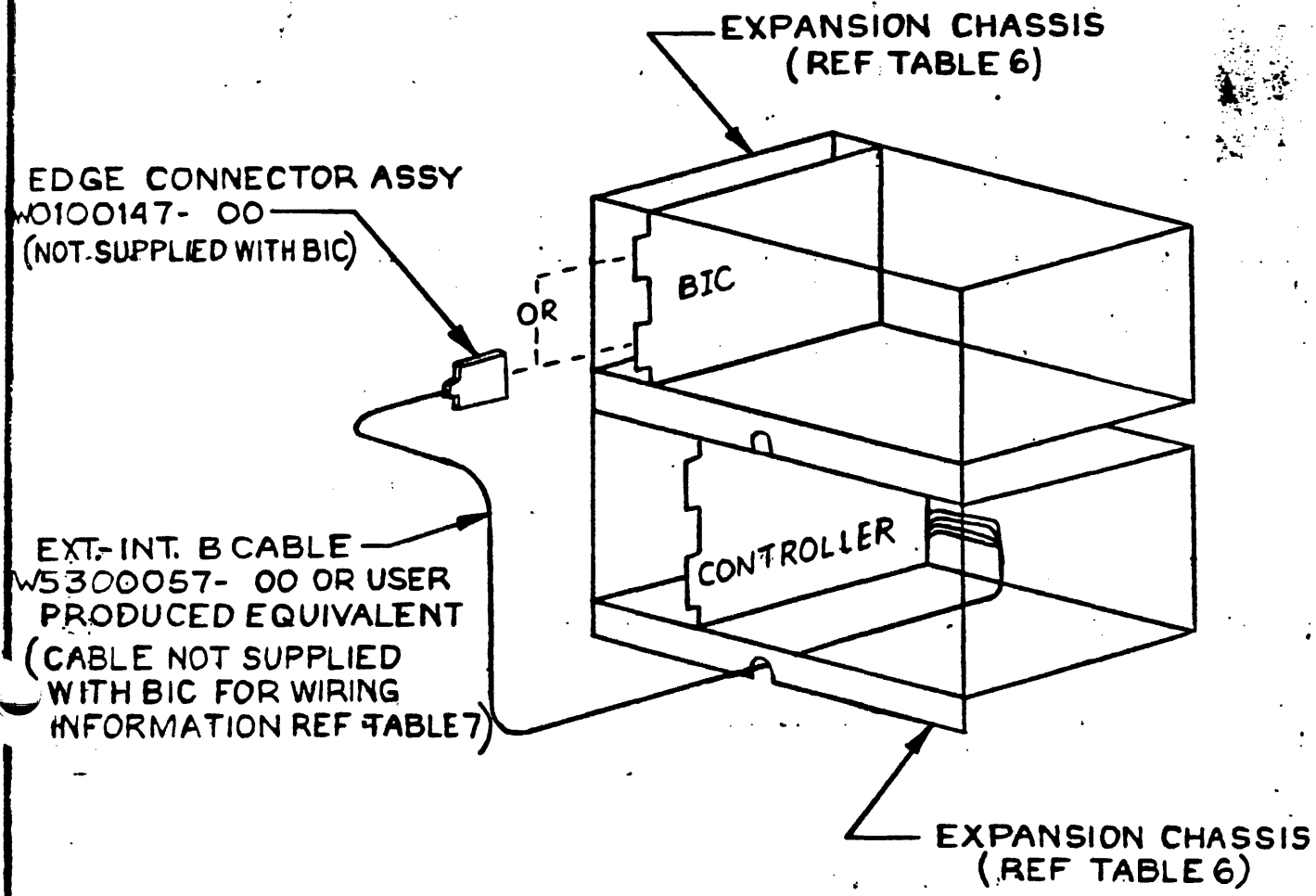


FIGURE 1

Table 6

COMPUTER	EXP. CHASSIS OPTION
620/i	W0100074- 00
620/L (S/N 1 thru 600)	W0101424- 04, 05, 06, 09
620/L (S/N 601 & On)	W0101424- 03, 04, 05, 06
620/L-100	W0101424- 03, 04, 05, 06
620/f	W0100927- 00, W0100929- 00
620/f-100	W0101265- 00, 01, 02
V73	W0101365- 01, 02, 03, 04, 05, 06, 07



NOTE: When controller is located external to either expansion chassis or the B-Cable length is greater than 6 feet, provide a 150 ohm, 1/2 W, 5% termination to +5 VDC on each line at the controller. Maximum cable length is 20 feet.

Figure 2

(This figure is shown for reference only to document non-standard interconnection).

The following functions are assigned to the connector pins as shown below:

FUNCTION	CARD-EDGE CONNECTORS	CONNECTOR PLATE PINS
DESX-B	39	60
R	40	59
TAKX-B	13	58
R	14	59
DCEX-B	27	56
R	28	57
TROX-B	17	50
R	18	53
TRQX-B	23	49
R	24	55
CDCX-B	35	54
R	36	57
BCDX-B	31	52
R	32	55
+5V	43	-
GND	42	-
SPARE	5	-
SPARE	6	-
SPARE	9	-
SPARE	10	-

Table 7

TABLE 8 'S' Plane Wiring for Key Bits and Mapping Error

Nomenclature		S Plane 60 Pin Connector Pins	BIC P1 Connector Pins	V7X I/O Cable * P1 Connector Pins
Old V70	New S Plane			
10K1-1	EB16-1,w/w	J1, 2 pin 19	109	109
10K2-1	EB17-1, w/w	J1, 2 pin 20	110	110
10K3-1	EB18-1, w/w	J1, 2 pin 21	112	112
BIMES-1 10K4-1	EB19-1, w/w	J1, 2 pin 22	113, 93	113
BTMES-1 for BTC	Uncommitted 2/2	Not used	Not used	94

*Cable from V7X mainframe chassis (P slots) I/O port to first I/O expansion chassis.

SPERRY UNIVAC PARTS LIST
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MFG CODE	ISSUE DATE	CONTROL		DOC NO.	AC	SHEET	
J ,W	81/03/03	W 781	PL	6600191	1	1	*

TITLE	PCC	ADC	PCD	COMM CODE	CA	U/M	ST	TYPE	SIZE	CLASS	
PC ASSEMBLY-BIC						EA	M	AP	D	A	*

FIND NO.	QUANTITY REQUIRED	U/M	PCC	PART OR IDENT NO. DOCUMENT NO.	DASH	EIR AND PART DESCRIPTION INFORMATION	ECC	ST	CHG
Z001				W 94616	-02	PL REV A, PIC REV A, RANGE 00 - 01 EIR RELEASED 81/03/03			*
Z000				W 87436	-02	PL REV -, PIC REV -, RANGE 00 - 00 EIR RELEASED 79/12/21			
*****	*******	***	*	**********	****	WITH KEY BITS (4400689-003) VAR DATA PART - 00 *********		B	*
				W 94616	-02	ABOVE PART SUPERSEDED UNILATERALLY BY 6600191- 01 81/03/03			
*****	*******	***	*	**********	****	REWORK 6600191-00/ W 94616-02 VAR DATA PART - 01 *********		A	
1	1	EA		6600186	-01	PC BOARD-BIC		A	*
2	4	EA	I	3008195	-00	INTEGRATED CIRCUIT TTL 7475 * REG LATCH 4BT		I	*
3	2	EA		W7800114	-00	SWITCH, TOGGLE, ROCKER DPDT ON NONE OFF,05A 30VDC		A	*
4	3	EA	I	5036520	-00	INTEGRATED CIRCUIT DIGITAL TTL 7473 * FF J-K DUAL		I	*
6	3	EA	I	3008194	-00	INTEGRATED CIRCUIT TTL 7474 * FF D DUAL		I	*
8	2	EA	I	2899573	-00	INTEGRATED CIRCUIT DIGITAL TTLH 74H11 * GT AND 3IN		I	*
10	5	EA	I	3007755	-00	INTEGRATED CIRCUIT TTLH 74H04 * GT HEX INVERT		I	*
12	1	EA	I	5036515	-00	INTEGRATED CIRCUIT TTLH 74H00 * GT NAND 2IN		I	*
14	4	EA	I	3008183	-00	INTEGRATED CIRCUIT TTL 7404 * GT HEX INVERT		I	*
16	4	EA	I	3013354	-00	INTEGRATED CIRCUIT TTLH 74H01 * GT NAND 2IN		I	*
18	1	EA	I	5036157	-00	INTEGRATED CIRCUIT DIGITAL DUAL D TYPE EDGE TRIG, F-F		A	*
20	3	EA		W4900093	-01	INTEGRATED CIRCUIT, DIGITAL TTLH 74H50		A	*
22	1	EA	I	3013355	-00	INTEGRATED CIRCUIT-IC192 TTLH 74H21 * GT AND 4IN		I	*
24	4	EA	I	5036505	-00	INTEGRATED CIRCUIT TTLH 74H08 * GT AND 2IN		I	*
26	4	EA		W4900127	-00	INTEGRATED CIRCUIT, DIGITAL TTL 74161 CNTR 4BT BIN		A	*
28	8	EA		W4900128	-01	INTEGRATED CIRCUIT, DIGITAL TTL 7438 QUAD 2IN NAND		I	*
30	1	EA	I	2899587	-00	INTEGRATED CIRCUIT DIGITAL TTL 74175 * FF D QUAD		A	*
31	1	EA		W4900554	-01	INTEGRATED CIRCUIT, DIGITAL TTLH 74H10 GT NAND 3IN		A	*
33	6	EA		W6502500	102	RES,FXD,COMPOSITION,1/4W,5% 1000 OHMS		A	*
				REF DES	(1)	R1 R2 (2) R11 R13 R14			

SPERRY UNIVAC PARTS LIST

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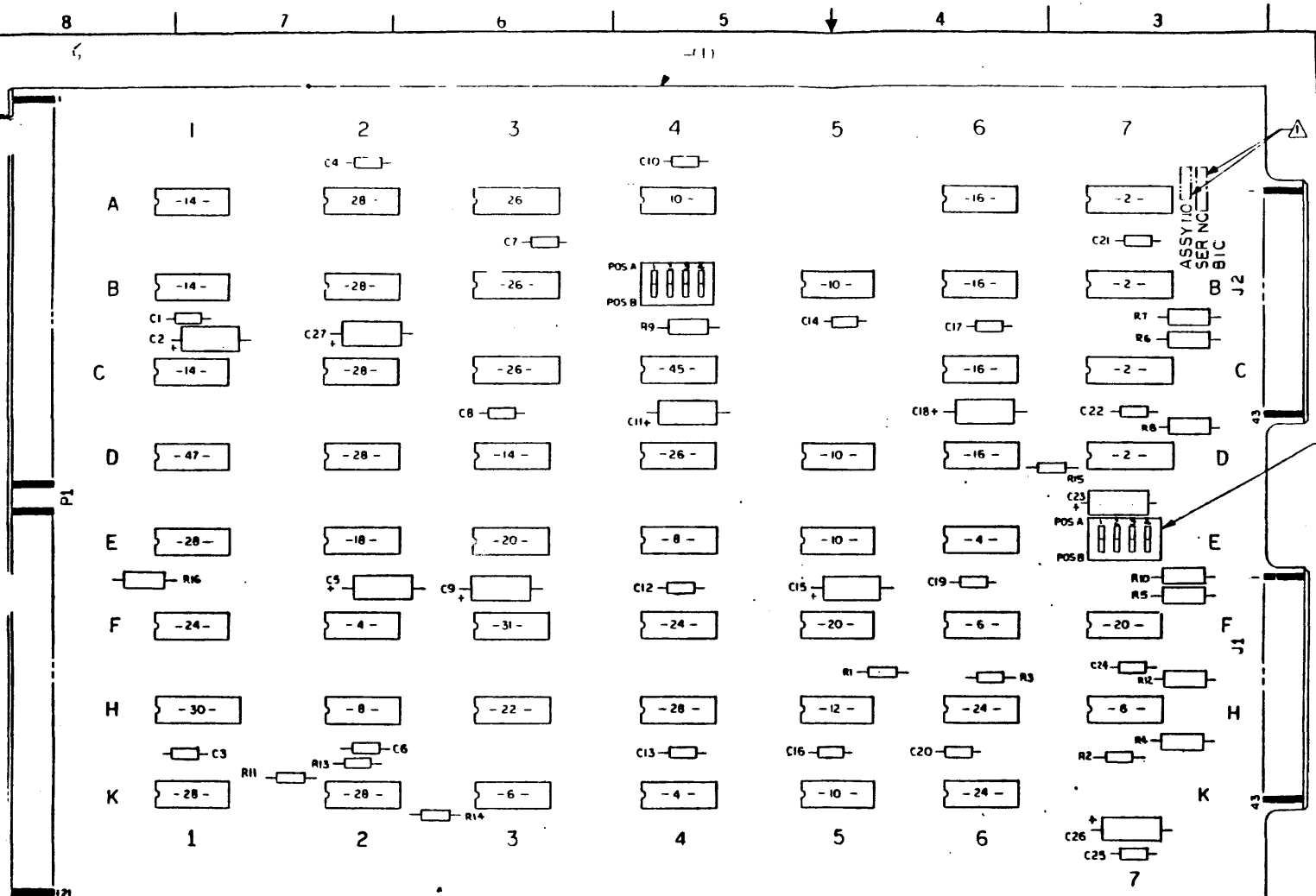
MFG CODE	ISSUE DATE	CONTROL		DOC NO.	AC	SHEET	
J ,W	81/03/03	W 781	PL	6600191	1	2	*

TITLE	PCC	ADC	PCD	COMM CODE	CA	U/M	ST	TYPE	SIZE	CLASS	
PC ASSEMBLY-BIC						EA	M	AP	D	A	*

FIND NO.	QUANTITY REQUIRED	U/M	PCC	PART OR IDENT NO. DOCUMENT NO.	DASH	EIR AND PART DESCRIPTION INFORMATION	ECC	ST	CHG
34	8	EA		W6505000	151	RES,FXD,COMPOSITION .5W 5% 150 OHMS		A	*
				REF DES	(1)	R4 THRU R10 (2) R12			
35	18	EA	C	4916657	-06	CAP FXD CER DIEL 50V +80 - 20% 100K PF		A	*
				REF DES	(1)	C1 C3 C4 (2) C6 C7 C8			
				REF DES	(3)	C10 C12 C13 (4) C14 C16 C17			
				REF DES	(5)	C19 C20 C21 (6) C22 C24 C25			
36	9	EA		W7100200	475	CAPACITOR, FXD, TANTALUM DIEL 4.7 UF 10% 20V		A	*
				REF DES	(1)	C2 C5 C9 (2) C11 C15 C18			
				REF DES	(3)	C23 C26 C27			
39	1	EA		W6502500	511	RES,FXD,COMPOSITION,1/4W,5% 510 OHMS		A	*
				REF DES	(1)	R15			
42	1	EA		W6505000	821	RES,FXD,COMPOSITION .5W 5% 820 OHMS		A	*
				REF DES	(1)	R16			
45	1	EA	I	5036504	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74804 * GT HEX INVERT		A	*
47	1	EA	I	3013703	-00	INTEGRATED CIRCUIT TTLS 74838 * GT NAND BFR		A	*
F001		X		6600187	-01	LOGIC DIAGRAM BIC		A	*
8001		X		8W01163	-00	MARKING,MECHANICAL SPECS DSGN-F/GENERAL IDENTIFICATION		A	*



REVISIONS						
ZONE	LTR	F1R	DESCRIPTION — FOR DETAILS SEE F1R	CHK	DATE	APPROVED
			RELEASE PART (X)	GA		
	A		SUPERSEDED PT -00 BY -01			

NOTES:
1. IDENTIFY PER (SOI)
2. NUMBERS BETWEEN DASHES ARE FIND NUMBERS IN PARTS LIST
3. "FIND" NUMBERS FOR PARTS, IDENTIFIED BY REFERENCE DESIGNATORS, APPEAR IN PARTS LIST.

MULTISTATUS DWG

SEE PL FOR PART NUMBER STATUS

PART NO. 6600191-01
IDENT NO.

FOR MAIL REQUIREMENTS SEE PL
PL REV LETTER CONTROLS DOCUMENT.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES TOL ON
2 PLACE DECIMALS ± .03 | 3 PLACE DECIMALS ± .010 | ANGLES ± 0.5°
HOLE DIA TOL
6 THRU .250 ± .005 — .002
.251 THRU .500 ± .005 — .010
.501 AND LARGER ± .010 — .010
THREADS EXT CL 2A, INT CL 2B
COMMODITY CODE

		DATE
LAYOUT		
DRAFTSMAN	E. OMERGAATEN	7/14/71
CHECKER		7/16
ENGINEER		
APPROVAL		

CLASS A

SPERRY UNIVAC

TITLE
PC ASSEMBLY-BIC
(WITH KEY BITS)

SIZE	CODE IDENT NO.	DWG NO.
D	21101	6600191

SCALE 2/1 | WEIGHT | SHEET 1 OF 1

DO NOT SCALE THIS PRINT

DWG NO 6600191 B

REVISIONS						
ZONE	LTR	E I R	DESCRIPTION — FOR DETAILS SEE E I R	CHK	DATE	APPROVED
	—	W94634-02	RELEASE -00			JVL
	A	W94616-02	INACTIVATED -00, RELEASED -01 REVISED SH. 13.0		1-23-81	MTM

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS VALUES ARE IN OHMS, 1/4W. ±5%.
2. CAPACITORS VALUES ARE IN MICROFARADS, 50V, ±$^{80}_{20}$%.
3. POWER AND GROUND DISTRIBUTION FOR IC'S:
   VOLTAGE - PIN 16 FOR 16 PIN IC'S
   PIN 14 FOR 14 PIN IC'S
   GROUND - PIN 8 FOR 16 PIN IC'S
   PIN 7 FOR 14 PIN IC'S

   EXCEPTIONS:
   IC'S AT F2, K4 & E6
   VOLTAGE - PIN 4
   GROUND - PIN 11
   IC'S AT A7, B7, C7 & D7
   VOLTAGE - PIN 5
   GROUND - PIN 12

TABLE OF CONTENTS

MULTISTATUS DWG

SEE PL FOR PART NUMBER STATUS

REFERENCE DESIGNATIONS	
E 13	
C 27	
R 16	
HIGHEST	NOT USED

ASSEMBLY NO. 6600191 IDENT NO. 6600 87-01

SHEET INDEX																							
SHEET	1.0		2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0	11.0	12.0	13.0									
REV	A	–	A	–	–	–	–	–	–	–	–	–	–	A									

LAYOUT	DATE	CLASS A
DRAFTSMAN E. DYNEBRATEN	7/20/-3	SPERRY UNIVAC
CHECKER	9/1/3	TITLE: LOGIC DIAGRAM - BIC
ENGINEER		
APPROVAL	9/10/81	SIZE C · CODE IDENT NO. 21101 · DWG NO. 6600187 · REV A

SHEET 1.0 OF 13.0

4 3 2 1

LOC	CHIP TYPE	WHERE USED					
A1	7404	7.0	8.0	9.0	9.0	9.0	9.0
A2	7438 SEL	9.0	9.0	9.0	9.0		
	74161	9.0					
	74H04	9.0	9.0	9.0	9.0	9.0	7.0
A6	74H01	9.0	9.0	9.0	9.0		
A7	7475	9.0	9.0	9.0	9.0		
B1	7404	10.0	10.0	10.0	10.0	12.0	12.0
B2	7438 SEL	10.0	10.0	10.0	10.0		
B3	74161	10.0					
B4							
B5	74H04	10.0	10.0	10.0	10.0	11.0	11.0
B6	74H01	10.0	10.0	10.0	10.0		
B7	7475	10.0	10.0	10.0	10.0		
C1	7404	11.0	11.0	11.0	11.0	12.0	12.0
C2	7438 SEL	11.0	11.0	11.0	11.0		
C3	74161	11.0					
C4	74S04	5.0	8.0	9.0	9.0	10.0	3.0
C5							
C6	74H01	11.0	11.0	11.0	11.0		
C7	7475	11.0	11.0	11.0	11.0		
D1	74S38	8.0	8.0	8.0	8.0		
D2	7438 SEL	12.0	12.0	12.0	13.0		
D3	7404	5.0	5.0	5.0	7.0	7.0	8.0
D4	74161	12.0					
D5	74H04	11.0	11.0	12.0	12.0	12.0	12.0
D6	74H01	12.0	12.0	12.0	12.0		
	7475	12.0	12.0	12.0	12.0		
E1	7438 SEL	7.0	8.0	8.0	8.0		
E2	74H74	8.0	8.0				
E3	74H50	8.0	13.0				
E4	74H11	5.0	5.0	5.0			
E5	74H04	5.0	5.0	5.0	6.0	8.0	8.0
E6	7473	6.0	7.0				
E7							
F1	3001	6.0	8.0	8.0	8.0		
F2	7473	8.0	8.0				
F3	74H10	5.0	8.0	8.0			
F4	3001	5.0	5.0	5.0	5.0		
F5	74H50	5.0	5.0				
F6	7474	5.0	5.0				
F7	74H50	6.0	7.0				
H1	74175	13.0					
H2	74H11	13.0	13.0	13.0			
H3	74H21	7.0	8.0				
H4	7438 SEL	5.0	6.0	6.0	6.0		
H5	74H00	6.0	6.0	6.0	7.0		
H6	3001	6.0	6.0	6.0	6.0		
H7	7474	6.0	7.0				

LOC	CHIP TYPE	WHERE USED					
K1	7438 SEL	13.0	13.0	13.0	13.0		
K2	7438 SEL	13.0	13.0	13.0			
K3	7474	13.0	13.0				
K4	7473	7.0	8.0				
K5	74H04	6.0					
K6	3001	7.0	7.0	7.0	7.0		
K7							

LOC	CHIP TYPE	WHERE USED					

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	6600187	-
SCALE		SHEET 1.1 OF 13.0	

POWER GROUND & DECOUPLING CAPACITORS

CODE IDENT NO.	SIZE	DWG NO	REV
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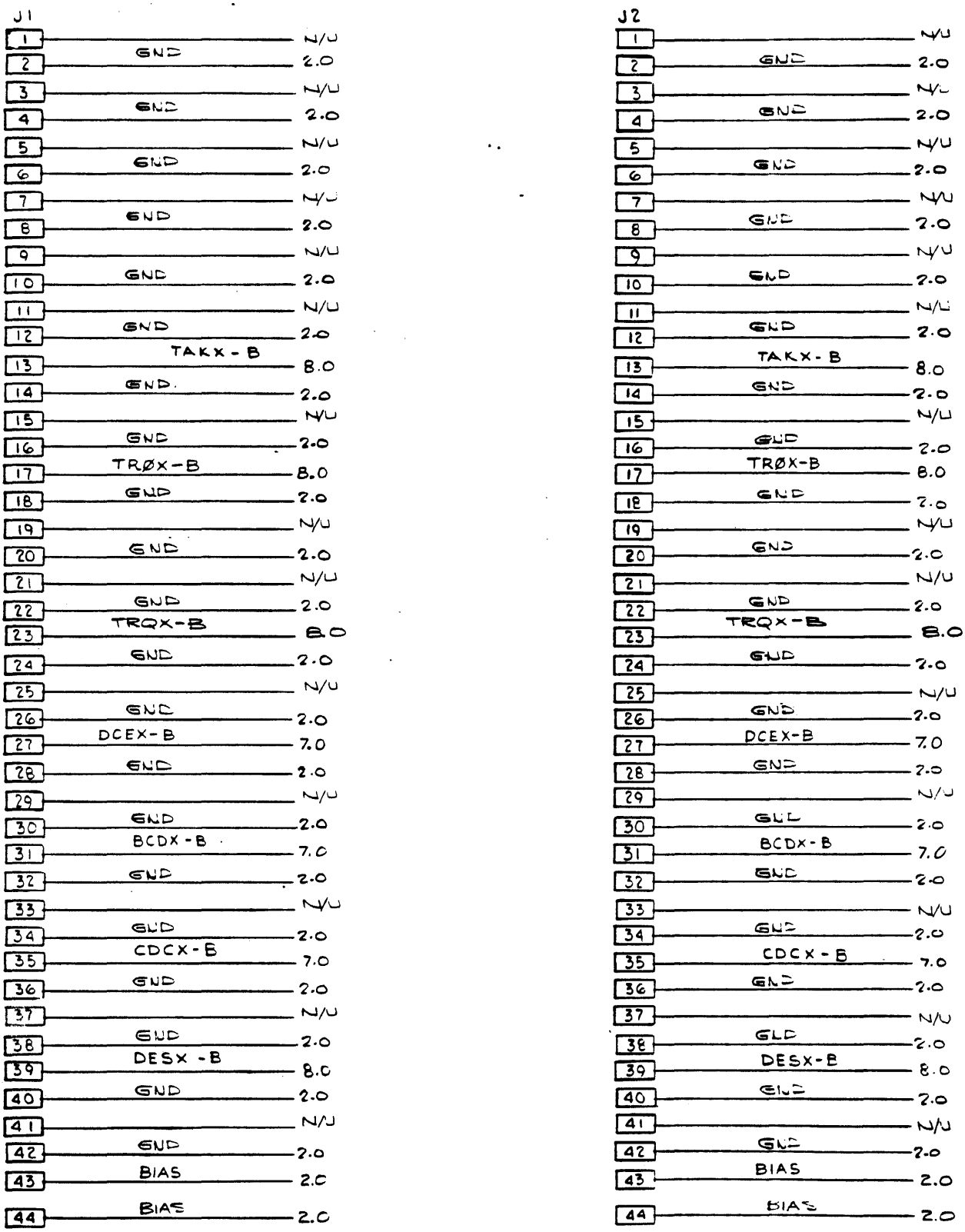
SCALE			SHEET 2.0 OF



CONNECTOR FUNCTION PG 3.0 & 4.0

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	6600187	1
SCALE		SHEET 3.0 OF	

4	3	2	1

P1							
1	GND	2.0	42	PRNX-I	8.0	84	N/U
2	EB00-I	9.0	43	SYRT-I	6.0	85	N/U
3	GND	2.0	44	IUAX-I	5.0	86	N/U
4	EB01-I	9.0	45	IUCX-I	7.0	87	N/U
5	GND	2.0	46		N/U	88	N/U
6	EB02-I	9.0	47		N/U	89	N/U
7	GND	2.0	48	GND	2.0	90	N/U
8	EB03-I	9.0	49	TRQX-B	8.0	91	N/U
9	GND	2.0	50	TRØX-B	8.0	92	N/U
10	EB04-I	10.0	51	GND	2.0	93	BIMEG-I 13.0
11	EB05-I	10.0	52	BCDX-B	7.0	94	N/U
12	EB06-I	10.0	53	G D	2.0	95	GND 2.0
13	EB07-I	10.0	54	CDCX-B	7.0	96	N/U
14	EB08-I	11.0	55	G D	2.0	97	N/U
15	EB09-I	11.0	56	DCEX-B	7.0	98	N/U
16	EB10-I	11.0	57	G D	2.0	99	N/U
17	EB11-I	11.0	58	TAKX-B	8.0	100	GND 2.0
18	EB12-I	12.0	59	G D	2.0	101	N/U
19	EB13-I	12.0	60	DESX-B	8.0	102	N/U
20	EB14-I	12.0				103	N/U
21	EB15-I	12.0				104	N/U
22	GND	2.0	63		N/U	105	N/U
23		N/U	64		N/U	106	N/U
24	GND	2.0	65		N/U	107	N/U
25		N/U	66		N/U	108	N/U
26	GND	2.0	67		N/U	109	IØK1-I 13.0
27	FRYX-I	5.0	68		N/U	110	IØK2-I 13.0
28	GND	2.0	69		N/U	161	GND 2.0
29	DRYX-I	5.0	70		N/U	112	IØK3-I 13.0
30	GND	2.0	71		N/U	113	IØK4-I 13.0
31	SERX-I	6.0	72		N/U	114	GND 2.0
32	GND	2.0	73	PRMY-I	8.0	115	BIAS 2.0
33	TPIX-I	8.0	74		N/U	116	N/U
34	GND	2.0	75	INTX-	8.0	117	N/U
35	TPOX-I	8.0	76		N/U	118	+5V 2.0
36	GND	2.0	77		N/U	119	N/U
37	PRMX-I	8.0	78		N/U	120	N/U
38	GND	2.0	79		N/U	121	+5V 2.0
39		N/U	80		N/U	122	GND 2.0
40	GND	2.0	81		N/U		
41		N/U	82		N/U		
			83		N/U		

CODE IDENT NO.	SIZE	DWG NO	REV
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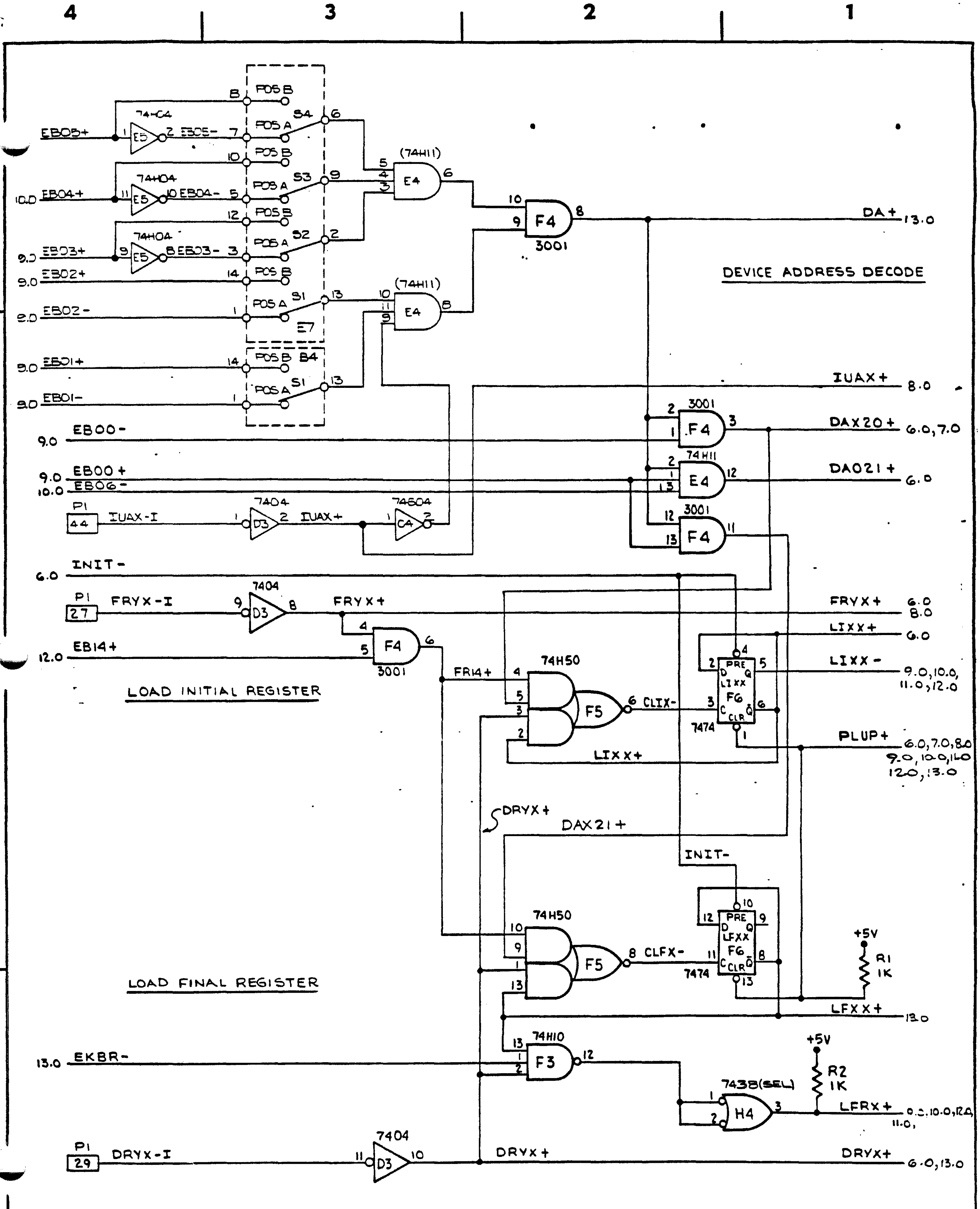
SCALE		SHEET 4 OF	



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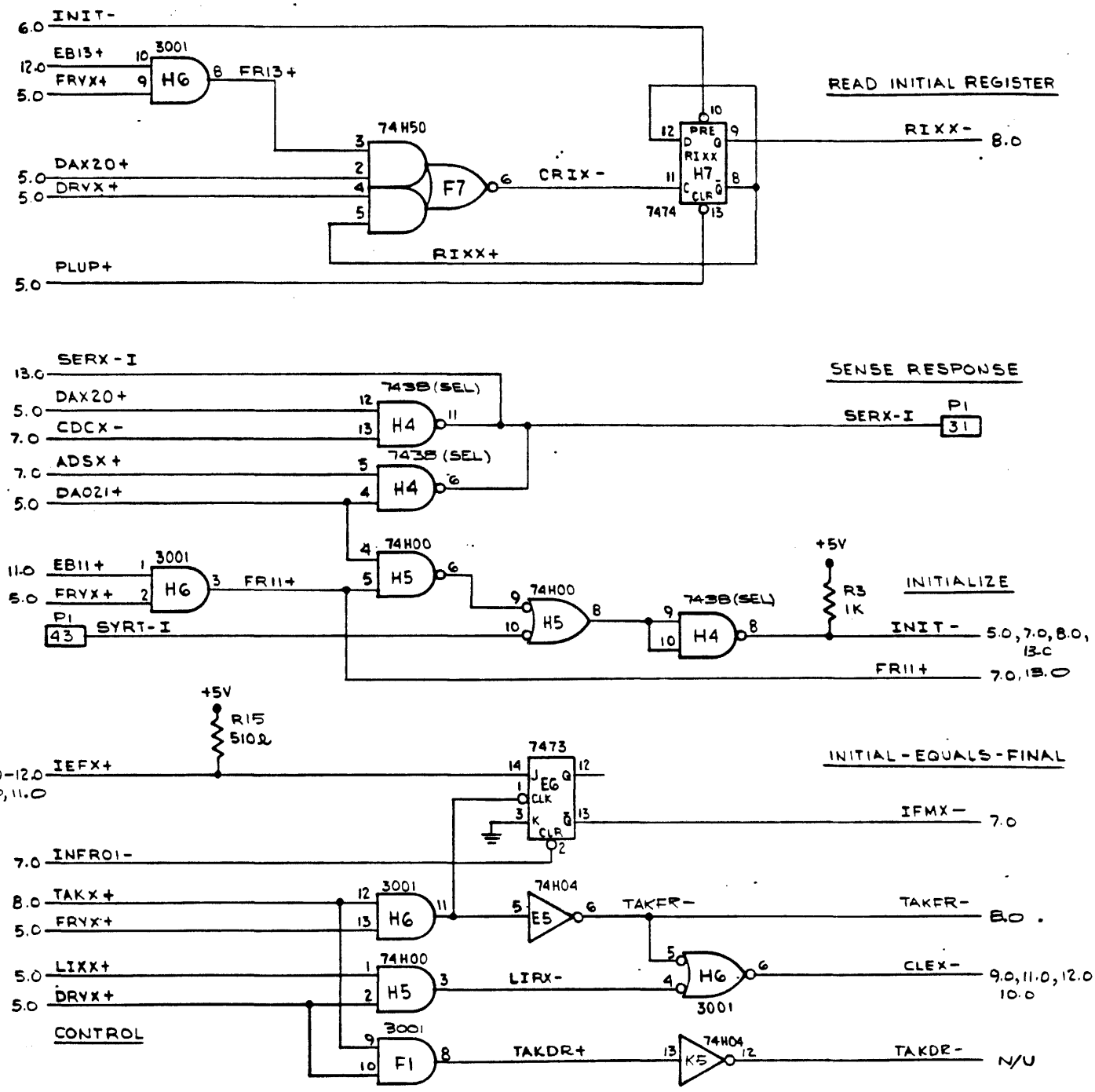
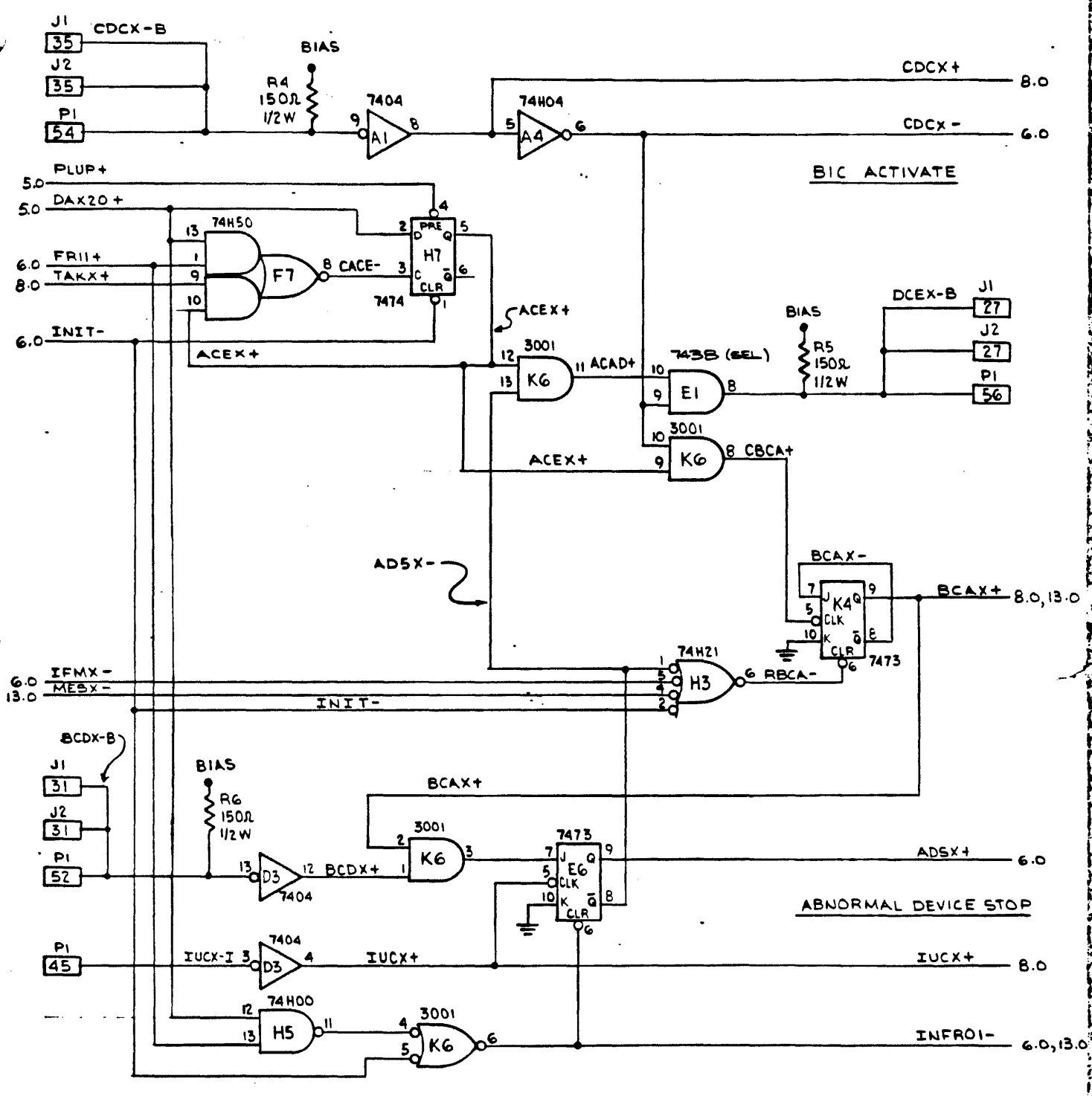
21101	C	6600187	–
SCALE		SHEET 5.0 OF	

DIETZGEN-POST CLEARPRINT



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	6600187	
SCALE		SHEET 6.0 OF	



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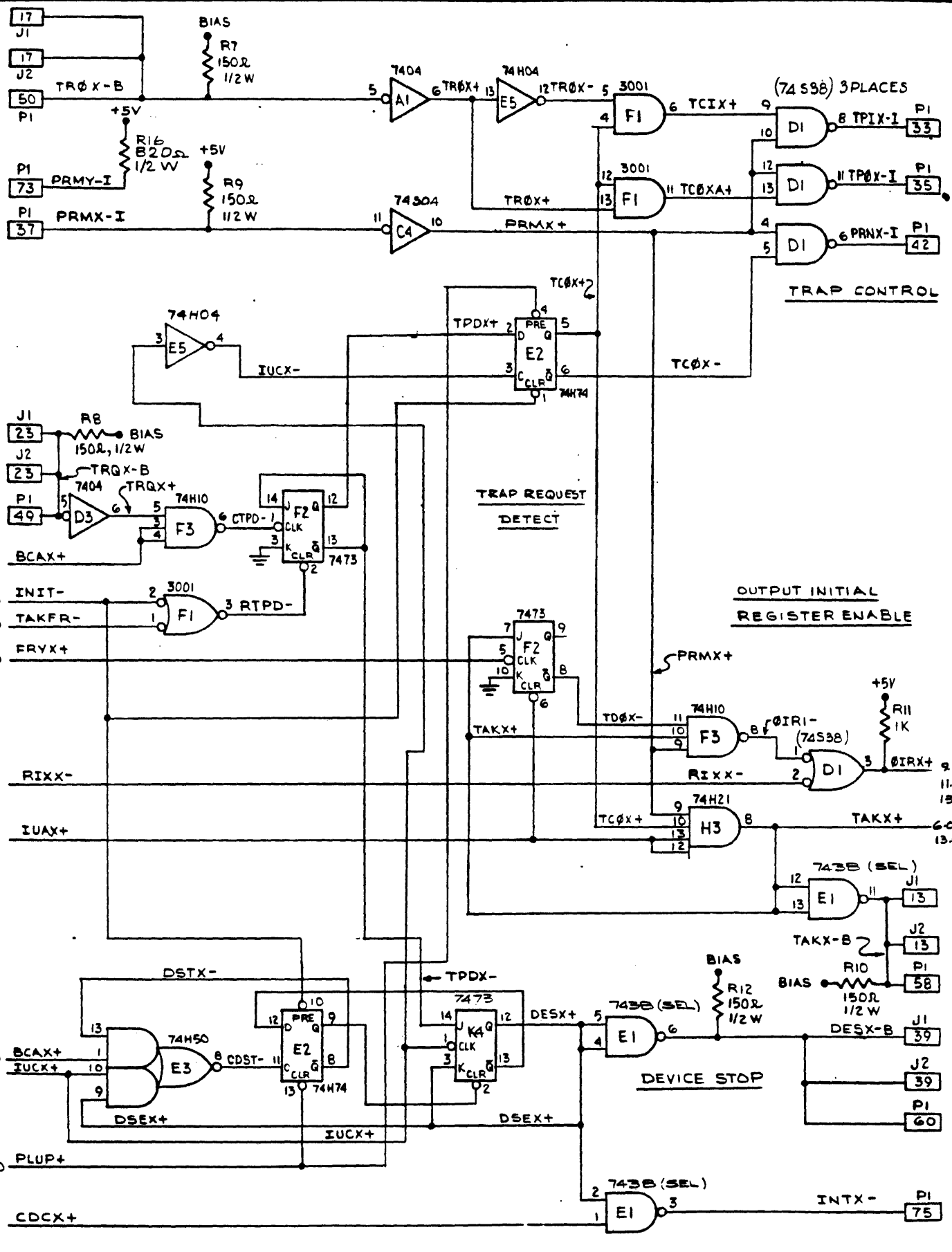
21101	C	6600187	
SCALE			SHEET 7.0 OF



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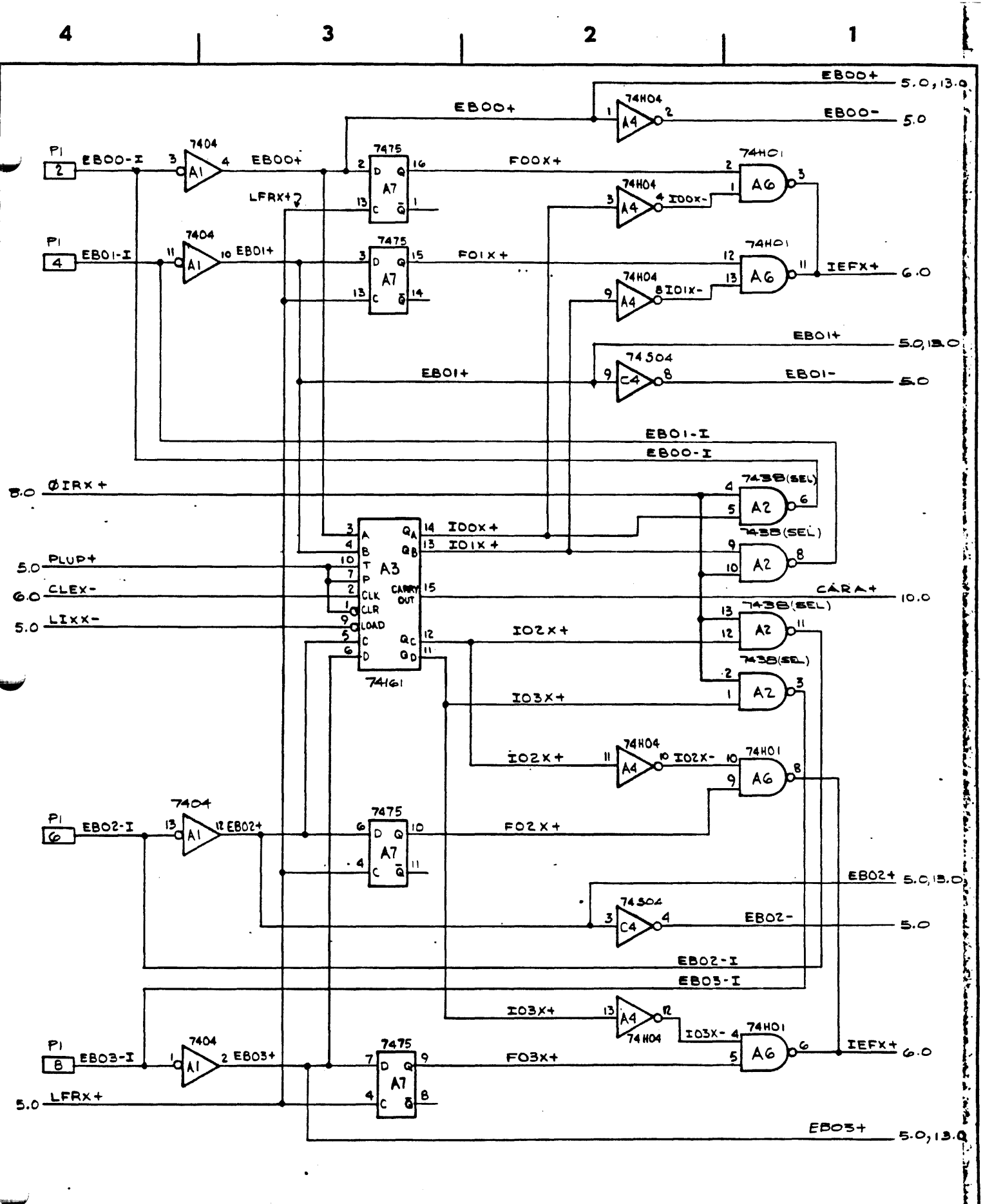
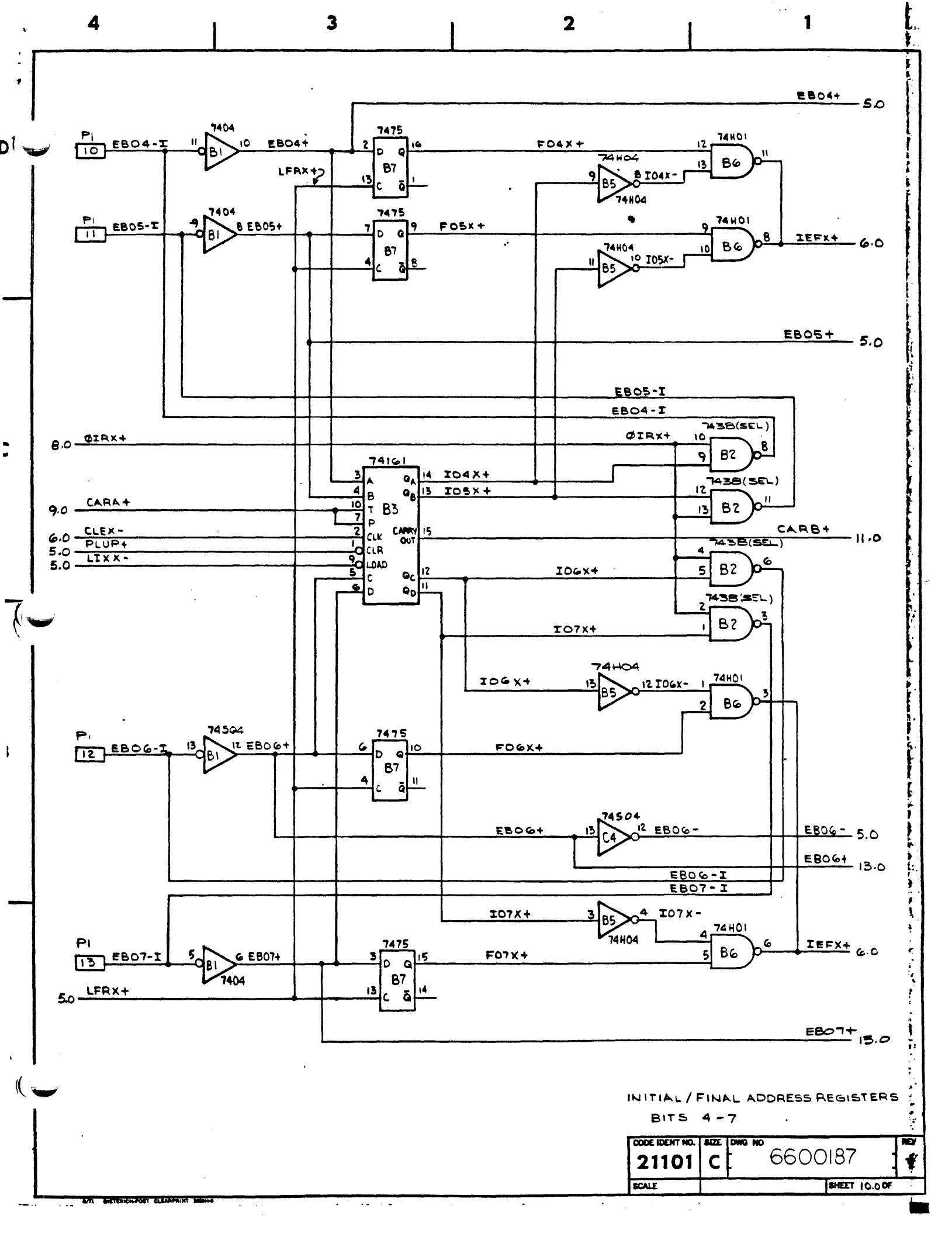
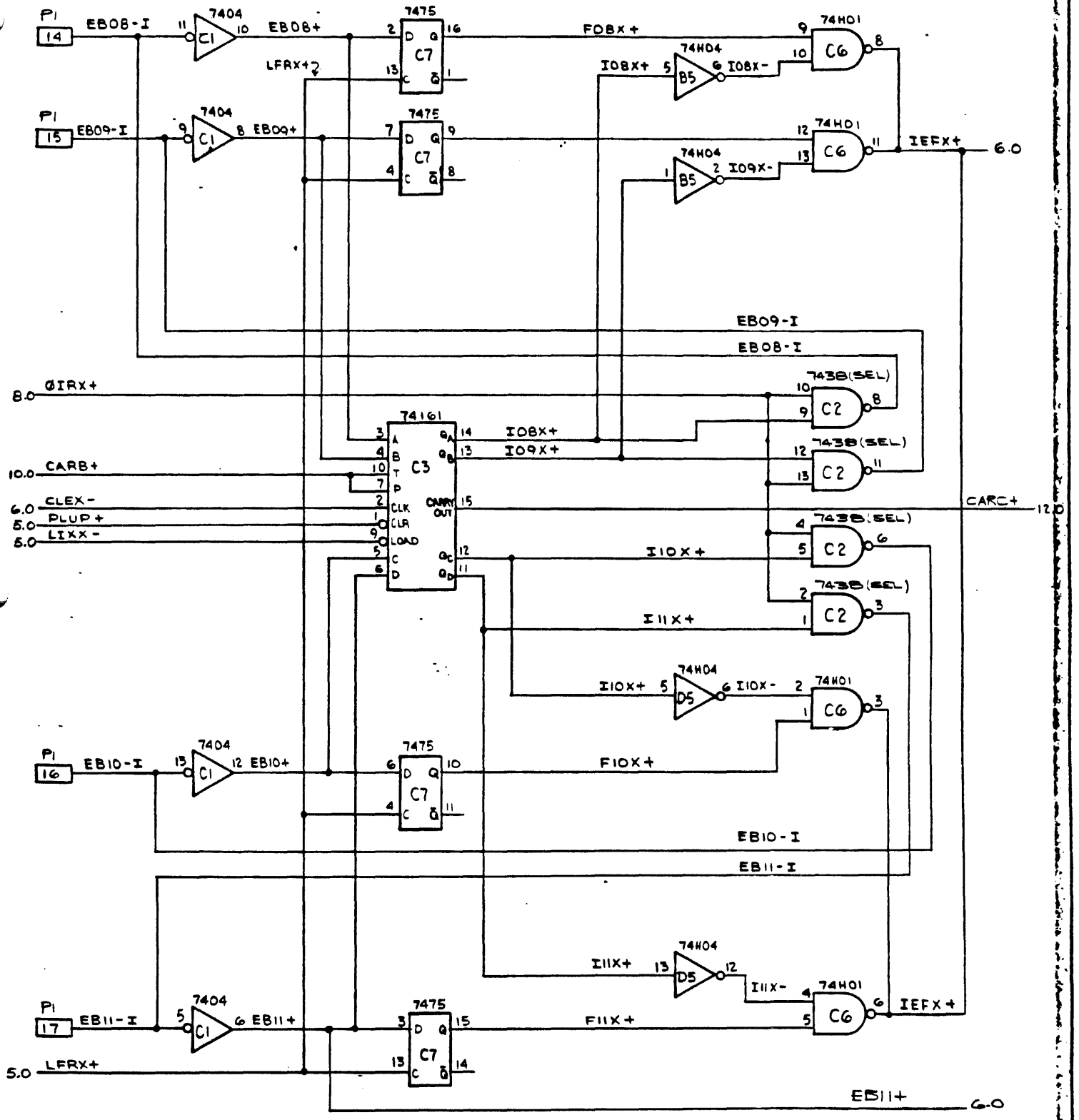
21101	C	6600187	
SCALE		SHEET 8.0 OF	

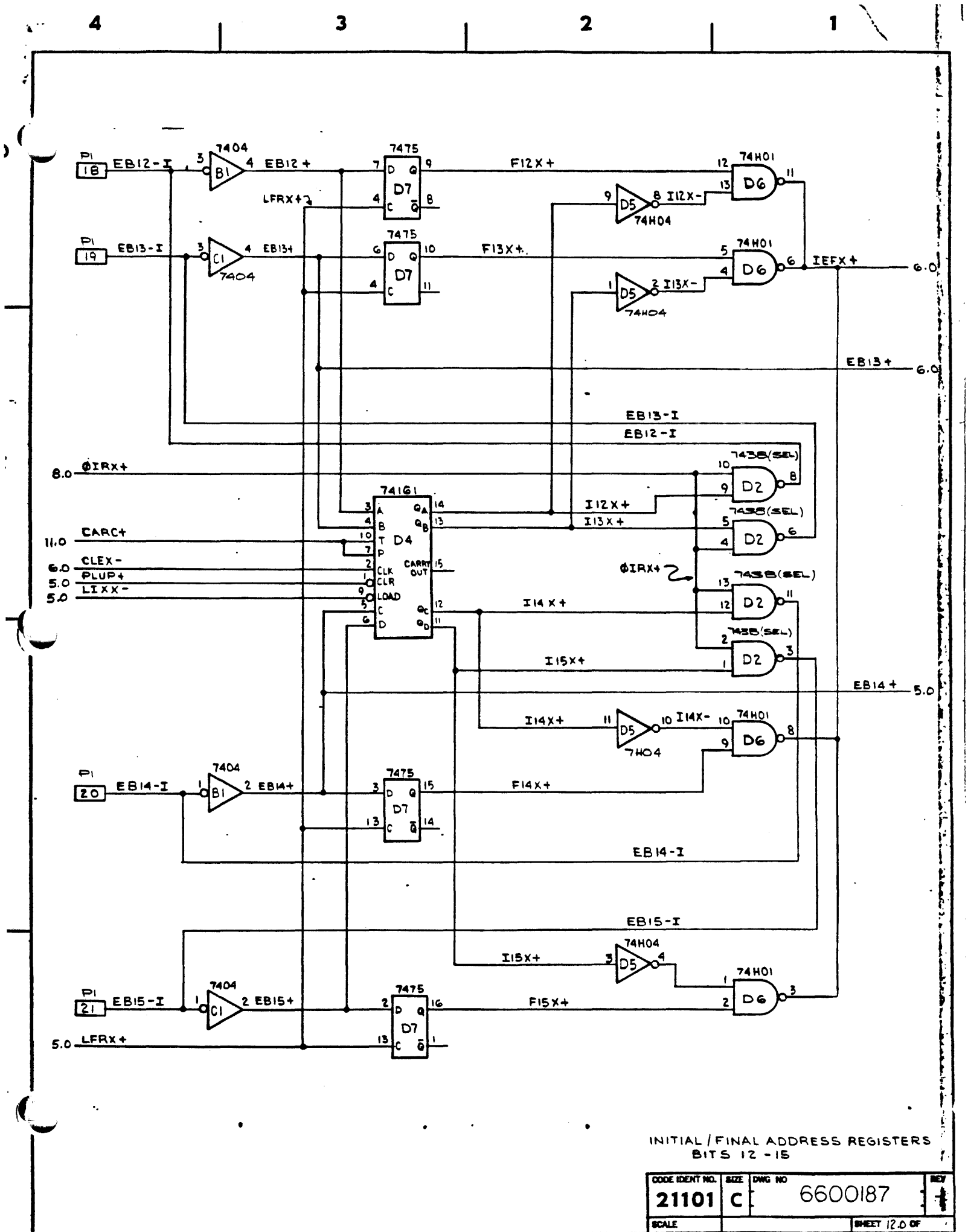

4
3
2
1
EB00+
5.0,13.0
74H04
A4
EB00-
5.0
P1
2
EB00-I
7404
A1
7475
A7
F00X+
74H01
A6
LFRX+?
74H04
I00X-
P1
4
EB01-I
F01X+
IEFX+
6.0
I01X-
EB01+
5.0,13.0
74S04
C4
EB01-
5.0
EB01-I
EB00-I
5.0
ØIRX+
7438(SEL)
A2
I00X+
I01X+
5.0
PLUP+
6.0
CLEX-
5.0
LIXX-
A3
CARRY OUT
CARA+
10.0
74161
I02X+
I03X+
I02X-
P1
6
EB02-I
EB02+
F02X+
EB02+
5.0,13.0
EB02-
5.0
EB02-I
EB03-I
I03X+
I03X-
P1
8
EB03-I
EB03+
F03X+
5.0
LFRX+
EB03+
5.0,13.0
INITIAL/FINAL ADDRESS REGISTERS
BITS 0-3
CODE IDENT NO.
21101
SIZE
C
DWG NO
6600187
REV
SCALE
SHEET 9.0 OF

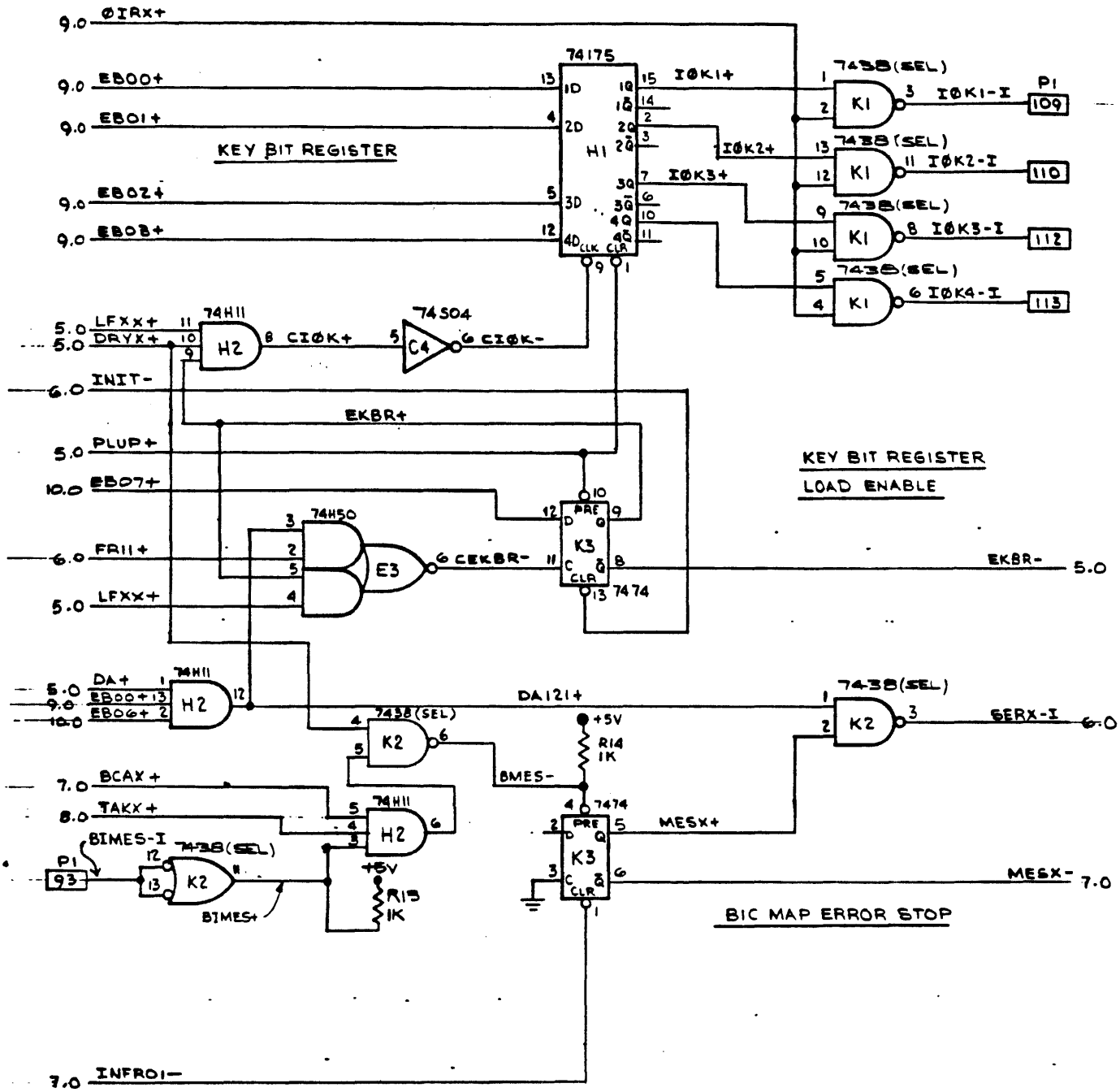

4
3
2
1
EB04+ 5.0
P1 10 EB04-I
7404 B1
EB04+
LFRX+
7475 B7
F04X+
74H01 B6
74H04 B5
IO4X-
IEFX+ 6.0
P1 11 EB05-I
EB05+
F05X+
IO5X-
EB05+ 5.0
EB05-I
EB04-I
8.0 ØIRX+
ØIRX+
74S38(SEL) B2
74161 B3
IO4X+
IO5X+
9.0 CARA+
6.0 CLEX-
5.0 PLUP+
5.0 LIXX-
CARRY OUT
CARB+ 11.0
IO6X+
IO7X+
IO6X-
P1 12 EB06-I
74S04 B1
EB06+
F06X+
EB06- 5.0
EB06+ 13.0
EB06-I
EB07-I
IO7X-
P1 13 EB07-I
EB07+
F07X+
5.0 LFRX+
EB07+ 13.0
INITIAL / FINAL ADDRESS REGISTERS
BITS 4-7
CODE IDENT NO. 21101
SIZE C
DWG NO 6600187
REV
SCALE
SHEET 10.0 OF



INITIAL / FINAL ADDRESS REGISTERS
BITS 8-11

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	6600187	
SCALE		SHEET 11.0 OF	


4
3
2
1
P1
18
EB12-I
7404
B1
EB12+
7475
D7
F12X+
74H01
D6
LFRX+
74H04
D5
I12X-
P1
19
EB13-I
C1
7404
EB13+
F13X+
I13X-
IEFX+
6.0
EB13+
6.0
EB13-I
EB12-I
8.0
ΦIRX+
7438(SEL)
D2
74161
D4
I12X+
I13X+
11.0
CARC+
6.0
CLEX-
5.0
PLUP+
5.0
LIXX-
CLK
CLR
LOAD
CARRY OUT
ΦIRX+
I14X+
I15X+
EB14+
5.0
I14X+
I14X-
P1
20
EB14-I
EB14+
F14X+
EB14-I
EB15-I
I15X+
P1
21
EB15-I
EB15+
F15X+
5.0
LFRX+
INITIAL / FINAL ADDRESS REGISTERS
BITS 12 - 15
CODE IDENT NO.
21101
SIZE
C
DWG NO
6600187
REV
SCALE
SHEET 12.0 OF



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	6600187	A
SCALE		SHEET 13 OF	

SPERRY UNIVAC®

BUFFER INTERLACE CONTROLLER
MODEL 7X-3102; P/N 0101563-001
OPERATION AND SERVICE MANUAL

98A 9902 117

APRIL 1978

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Printed in U.S.A.

SECTION 1
GENERAL DESCRIPTION

The Buffer Interlace Controller (BIC) is a special-purpose hardware option for use with SPERRY UNIVAC V70 series and 77 series computers. This manual is divided into six sections:

- Features and specifications
- Installation and interconnection
- Operation
- Theory of operation
- Maintenance
- Mnemonics list

Documents such as logic diagrams, schematics and parts lists are supplied in a system documentation package. This documentation is assembled when the equipment is shipped, and reflects the configuration of a specific system.

There are two versions of the BIC available. One version (without key bits) is for systems that do not have the memory map option and the other version (with key bits) is for systems that do have the memory map option.

The function of the BIC is to free the processor to perform other program functions during block word transfers between memory and peripheral controllers. Cycle-stealing trap requests inhibit the processing of a stored program for only the memory cycle required to transfer one word of data between memory and a peripheral controller. Operation register contents are not changed by the transfer, thus freeing the processor to execute an instruction from the stored program between successive data word transfers.

The BIC will perform DMA transfers at the peripheral device rate up to a maximum rate defined as follows:

$$R_{max} = \frac{1}{\frac{1}{R_{CPU\ max}} + T_{IUCX}}$$

where: R_{max} is the maximum rate through a BIC (words/second)
R_{CPU} is the maximum DMA rate for the processor (words/second)
T_{IUCX} is the period of interrupt clock (seconds)

As an example, the maximum DMA rate for any V70 series computer with core memory and a 990 nanosecond interrupt clock period is 361,800 words/second. The maximum rate through the BIC is then:

$$R_{max} = \frac{1}{\frac{1}{361{,}800} + (990 \times 10^{-9})} = 266{,}383 \text{ words/second}$$

The BIC monitors trap requests initiated by the peripheral controllers.

Up to ten peripheral controllers can be connected to one BIC. Using standard I/O device addressing, a computer system can include up to four BICs.

The BIC is considered to be an I/O controller. Priorities for optional controllers having trap or interrupt capabilities are established by the order of their placement in the priority chain. The BIC is a system priority device; however the peripheral devices connected to it have no priority of their own.

Table 1-1 lists the BIC specifications.

Table 1-1. BIC Specifications

Parameter	Description
Organization	Contains input receivers and output drivers, two 16-bit address registers, a 4-bit key register, and a sequence control circuit
Control capability	Up to ten peripheral controllers
I/O transfer rate	Synchronized to peripheral device rate
I/O signal limits (rise/fall)	Minimum 10 nanoseconds; maximum 100 nanoseconds
Logic levels (internal)	High = +2.4 to +5.0V dc Low = 0 to +0.4V dc
Logic levels (I/O bus)	High = +2.8 to +3.6V dc Low = 0 to +0.5V dc
Size	Contained on one 7-3/4-by 12-inch (19.7 x 30.3 cm) printed-circuit board

(continued)

Table 1-1. BIC Specifications *(continued)*

Parameter	Description
Interconnection	Interfaces with I/O cable through backplane connector; connects to peripheral controllers through the backplane connector or through a cable
Connectors	One 122-terminal card-edge connector (mates with female connector at backplane) and two 44-terminal card-edge connectors (each mates with a 44-terminal connector on B cable for special configurations)
Power	+5V dc at 0.6A
Operating environment	0 to 50 degrees C; 10 to 90 percent relative humidity without condensation

SECTION 2
INSTALLATION

The BIC has been packed and inspected to ensure its arrival in good working order. To prevent damage, take care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. If damage exists:

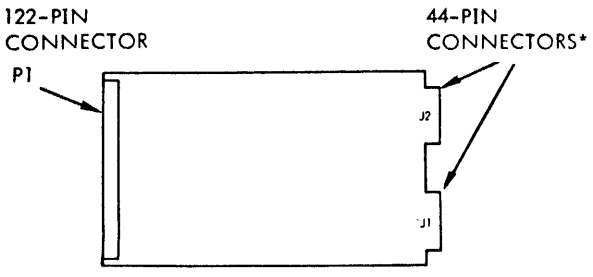
- Notify the transportation company
- Notify Sperry Univac
- Save all packing material

2.1 PHYSICAL DESCRIPTION

The BIC circuits are contained on a single printed-circuit (PC) board (p/n 44P0689). As illustrated in figure 2-1, the board contains three connectors P1, J1, and J2. Connectors J1 and J2 are wired in parallel and contain the peripheral control lines. Connector P1 also contains the same peripheral control lines as well as all I/O bus control signals for the BIC. Connectors J1 and J2 are used for special configurations.

2.2 INTERCONNECTION

When two or more BIC controllers are installed in the same chassis, the B cable signals are connected only to the controller or controllers with which each BIC communicates. There are no B cable signals between BICs. If the BIC and the peripheral controllers are installed in different chassis, the interconnection is made through the J1 and J2 connectors. Figure 2-2 illustrates BIC/peripheral interconnections.



* CONNECTORS J1 AND J2 ARE PARALLEL WIRED

VTII-1792

Figure 2-1. BIC Board (Component Side)

2.3 INTERFACE DATA

All BIC input/output signals utilize receiver/driver stages to buffer internal circuits and external lines. The BIC interfaces with the computer via the "—I" signal lines and with peripheral controllers via the "—B" signal lines listed in table 2-1. The corresponding pin number of circuit card edge connector P1 follows each signal mnemonic (see logic diagram 91C0459). Refer to section 6 for definitions of the mnemonics.

Table 2-1. BIC Inputs and Outputs

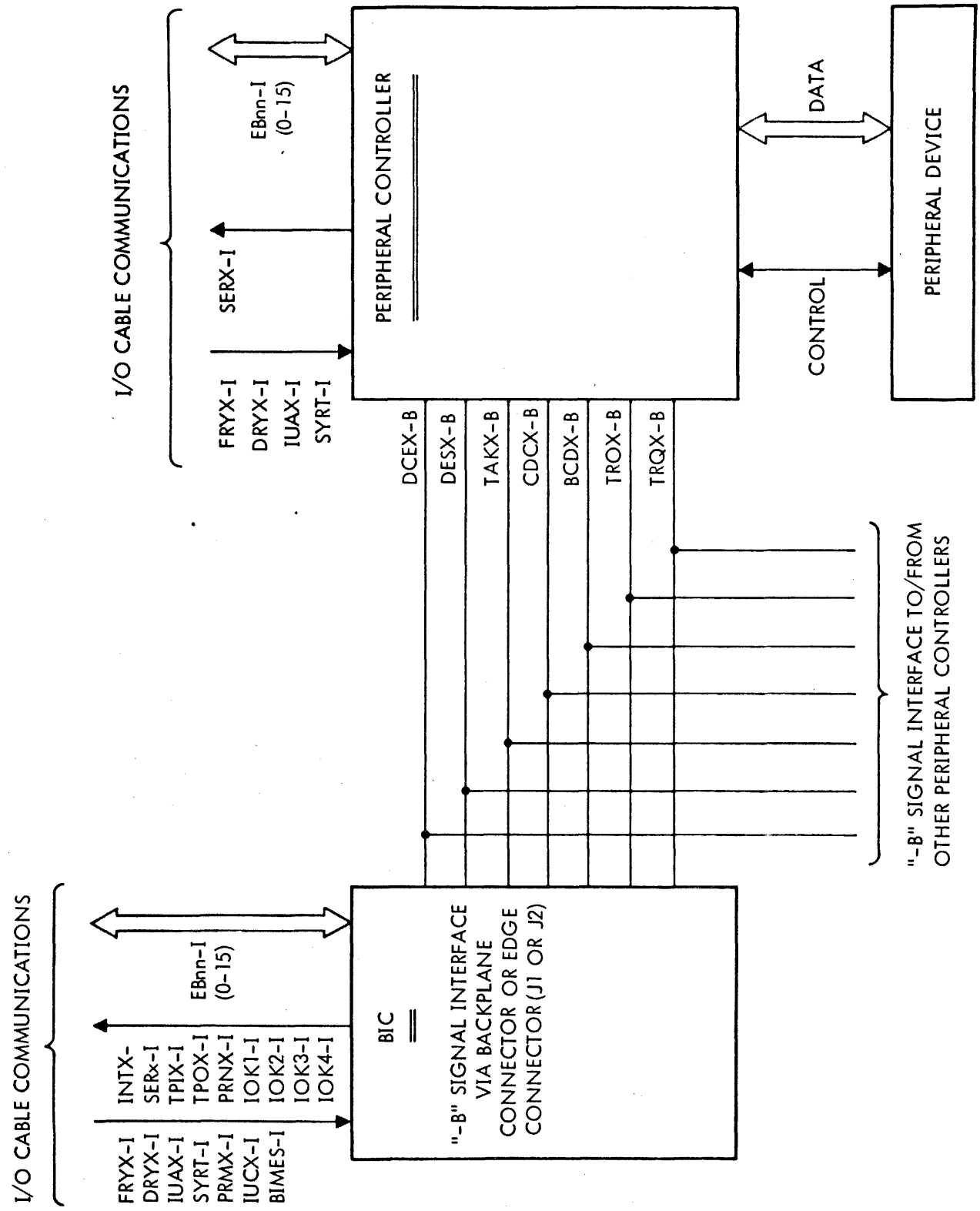
INPUTS				OUTPUTS			
BCDX-B	52	EB10-I	16	DCEX-B	56	EB12-I	18
BIMES-I	93	EB11-I	17	DESX-B	60	EB13-I	19
CDCX-B	54	EB12-I	18	EB00-I	2	EB14-I	20
DRYX-I	29	EB13-I	19	EB01-I	4,68,69*	EB15-I	21
EB00-I	2	EB14-I	20	EB02-I	6,71,72	INTX-	75
EB01-I	4,65	EB15-I	21	EB03-I	8	IOK1-I	109
EB02-I	6,70	FRYX-I	27	EB04-I	10	IOK2-I	110
EB03-I	8	IUAX-I	44	EB05-I	11	IOK3-I	112
EB04-I	10	IUCX-I	45	EB06-I	12	IOK4-I	113
EB05-I	11	PRMX-I	37	EB07-I	13	PRNX-I	42
EB06-I	12	SYRT-I	43	EB08-I	14	SERX-I	31
EB07-I	13	TROX-B	50	EB09-I	15	TAKX-B	58
EB08-I	14	TRQX-B	49	EB10-I	16	TPIX-I	33
EB09-I	15			EB11-I	17	TPOX-I	35

NOTE: On systems with memory map, the BIMES-I and BTMES-I signals are floating and must be pulled up to +5 volts by adding the following jumpers:

a. On each backplane slot, pin 93 (BIMES-I) is connected to pin 73 (PRMY-I).

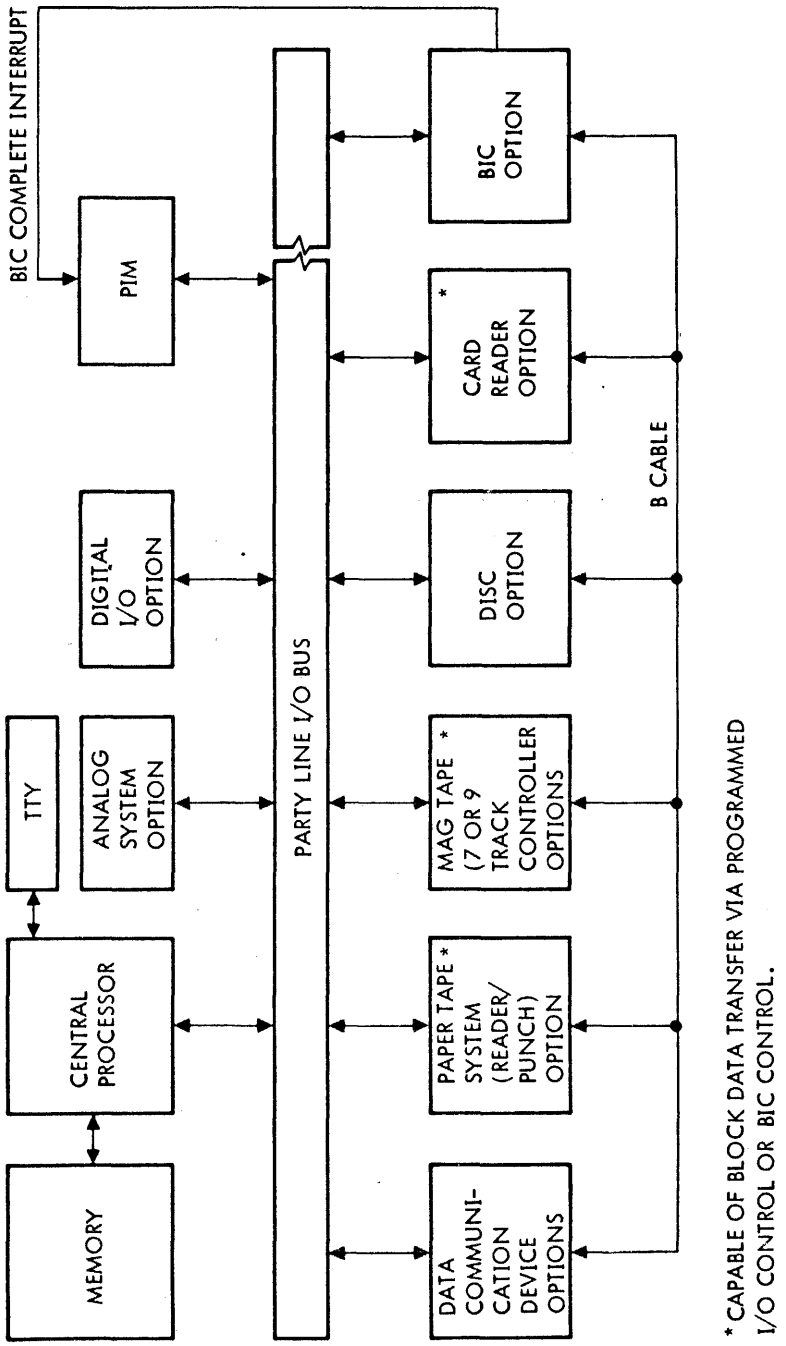
b. On each PMA/BTC backplane slot, pin 96 (BTMES-I) is connected to pin 73 (EXPU+).

Many peripheral controllers, under software control, can transfer data either by programmed I/O or via BIC control. Controllers for peripherals such as discs and drums usually are not able to transfer data via programmed I/O due to their high transfer rates. Figure 2-3 shows a computer system with peripheral controllers that operate with and without BIC. Figure 2-4 is typical interface logic.



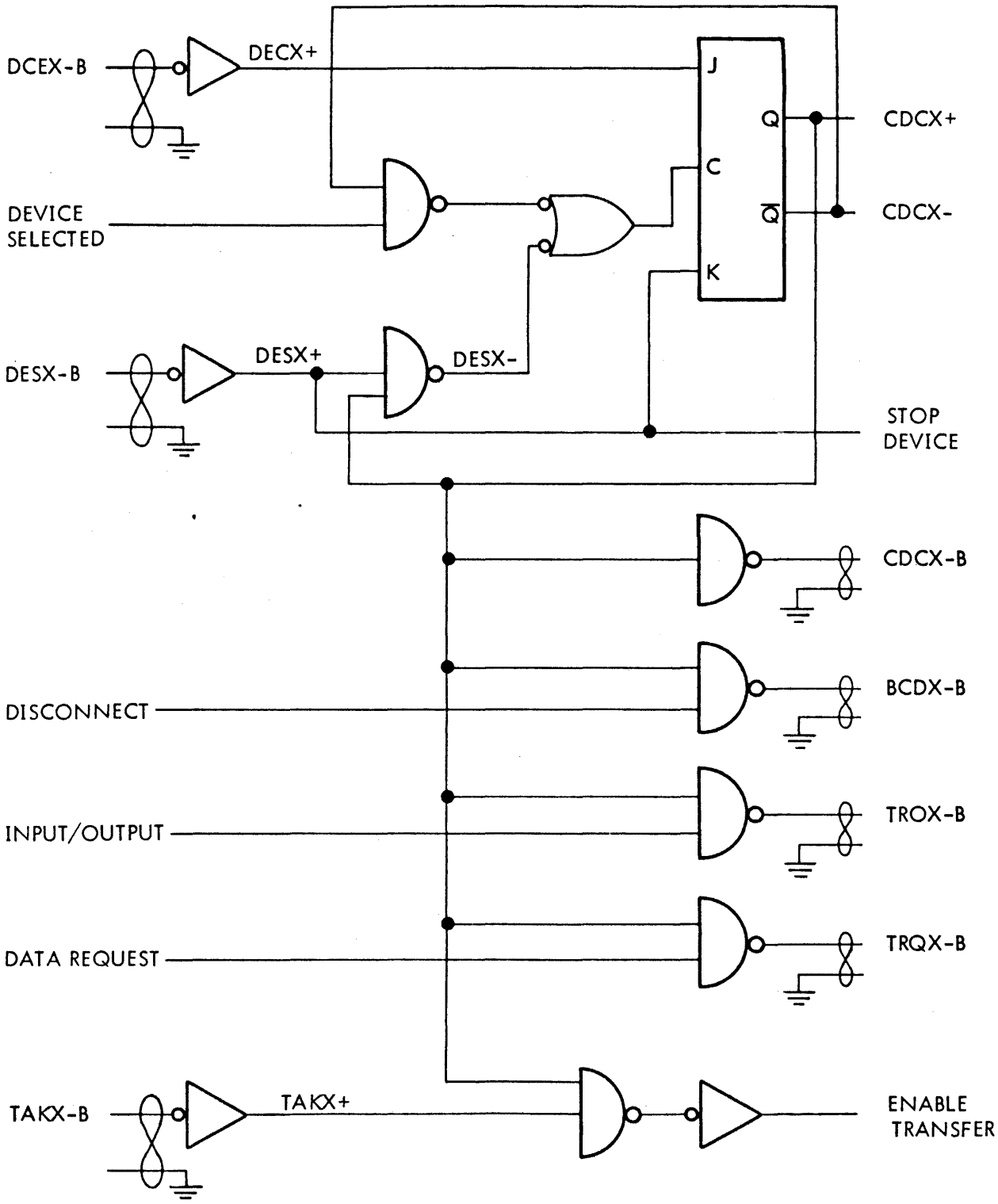
VTII-233A

Figure 2-2. BIC/Peripheral Controller Interface



VTII-340B

Figure 2-3. Interface for Peripheral Devices with and



VTII-232A

Figure 2-4. Typical B Cable Interface Logic

SECTION 3
OPERATION

The BIC has no operating controls or indicators. It operates under program control.

3.1 I/O INSTRUCTIONS

The BIC responds to the instructions listed in table 3-1. Two device addresses are assigned to each BIC to differentiate functions directed by the I/O instruction. Addresses 020 through 027 are reserved for BICs. Address/instruction codes in table 3-1 are for the first BIC in a system. If additional BICs are installed, the addresses shown should be incremented by two for each additional BIC (i.e., second BIC addresses should be 022 and 023).

Table 3-1. I/O Instructions

Mnemonics	Octal Code	Description
		External Control
EXC 020	100020	Activate BIC
EXC 021	100021	Initialize
EXC 0321	100321	Enable loading of key bits
		Transfer
OAR 020	103120	Load initial register from A
OBR 020	103220	Load initial register from B
OME 020	103020	Load initial register from memory
OAR 021	103121	Load final register from A
OBR 021	103221	Load final register from B
OME 021	103021	Load final register from memory
INA 020	102120	Read initial register into A
INB 020	102220	Read initial register into B
IME 020	102020	Read initial register into memory
CIA 020	102520	Read initial register into cleared A
CIB 020	102620	Read initial register into cleared B
		Sense
SEN 020	101020	Sense BIC not busy
SEN 021	101021	Sense abnormal device stop
SEN 0121	101121	Senses if BIC has been stopped due to a memory-map error

3.2 PROGRAMMING CONSIDERATIONS

The user writes the programs that use the BIC. When preparing a program for use with the BIC, the programmer first initializes then senses the status of the BIC and the selected peripheral controller. After a not-busy response is received from both the BIC and the peripheral controller, the BIC address registers are loaded with the initial and final memory addresses of the block of data to be transferred, a BIC activate enable instruction is placed on the I/O cable, and the transfer is started. Although the program requires loops for use with sense instructions and to handle abnormal conditions, transfer of the data block is accomplished by the BIC without further program instructions.

The key bit register (for memory map option) is loaded by first issuing the "Enable (loadingof) Key Bit Register" instruction (0100321) followed by one of the "Load Final Register" instructions (0103021, 0103121, 0103221).

3.3 SAMPLE PROGRAM

Table 3-2 shows a typical service routine for the BIC, a Teletype paper tape punch operation under BIC control. Using DAS symbols with corresponding machine language

Table 3-2. Typical Service Routine

Memory Location	Octal Code	Label	Operation	Variable Field	Comments
001000			,ORG	,01000	
001000	101020	BIC0	,SEN	,020,BIC1	CK BIC NOT BUSY
001001	001007 R				
001002	100401		,EXC	,0401	INIT TTY
001003	100021		,EXC	,021	INIT BIC
001004	005000		,NOP	,	
001005	001000		,JMP	,*-3	

(continued)

Table 3-2. Typical Service Routine *(continued)*

Memory Location	Octal Code	Label	Operation	Variable Field	Comments
001006	001002 R				
001007	101101	BIC1	,SEN	,0101,BIC2	CK TTY WRITE READY
001010	001014 R				
001011	005000		,NOP	,	
001012	001000		,JMP	,*-3	
001013	001007 R				
001014	103120	BIC2	,OAR	,020	SET BIC I REG
001015	103221		,OBR	,021	SET BIC F REG
001016	100020		,EXC	,020	ACTIVATE BIC
001017	100101		,EXC	,0101	CONNECT WRITE REG
001020	101020		,SEN	,020,BIC3	CK BIC NOT BUSY
001021	001025 R				
001022	005000		,NOP	,	
001023	001000		,JMP	,*-3	
001024	001020 R				
001025	101021	BIC3	,SEN	,021,BIC5	CK ABN STOP
001026	001032 R				
001027	007400		,ROF	,	
001030	102520	BIC4	,CIA	,020	INPUT BIC I REG
001031	000000		,HLT	,	
001032	007401	BIC5	,SOF	,	SET ABN FLAG
001033	001000		,JMP	,BIC4	
001034	001030 R				
	000000		,END	,	

octal codes, the program covers memory locations 01000 through 01034.

Once the program is loaded, the operator must insert the initial punch buffer address into the A register and the final address into the B register for each run. When started, the program will:

a. initialize the BIC and Teletype punch

b. initiate the data transfer

c. read the contents of the BIC initial register into the A register at the completion of the transfer

d. set the overflow indicator if the termination was abnormal

e. halt

The punch buffer must contain only ASCII characters. The first character is 0222 (punch on) and the last is 0224 (punch off).

SECTION 4
THEORY OF OPERATION

The BIC is functionally divided into address registers and a sequence control circuit (figure 4-1). A functional description of these circuits is provided in the following paragraphs.

4.1 ADDRESS REGISTERS

The two address registers contain the memory locations of output or input data, depending on the I/O instruction. The initial register stores the address of the first input or output word, and is incremented during each data-word transfer. When the block transfer is complete, the initial register contains the address + 1 of the last data word to be transferred.

The final register stores the address of the last word to be transferred. Unless the peripheral device is abnormally stopped, the address in the final register will be one less than the address in the initial register when the block transfer is complete. When the initial and final registers reach comparison, the block word transfer is complete.

The key-bit register stores the four key bits that are used with the memory map. The key-bit register is not used on systems without the memory map. The enable instruction sets a flip-flop which directs the data being transferred by a load (of final register) instruction, into the key-bit register. The flip-flop is reset when the transfer is complete.

4.2 SEQUENCE CONTROL

The sequence control circuit generates the control signals which coordinate address and data transfer between the processor, BIC, and the peripheral controllers. The data are not routed through the BIC but are directly transferred between the peripheral controller and memory.

Under program control, the processor senses that the BIC is not busy and prepares the BIC to receive the initial and final data addresses. The processor then senses that the selected peripheral controller is not busy and loads the initial and final registers and the key register. The BIC is then activated and the peripheral controller is started. The BIC then assumes control of the data transmission, allowing the processor operational registers to be used by the program for other functions.

Data transfer is accomplished between memory and the peripheral controller via the I/O bus. The BIC counts the words transferred and when the data block transfer is complete, disconnects the peripheral controller and assumes a not-busy state. Data transfer may also be terminated upon request from the peripheral controller.

4.3 OPERATING SEQUENCE

The following paragraphs describe the sequence of operations of the BIC. Refer to the block diagram (figure 4-1), the timing diagram (figure 4-2), and the logic diagram 91C0459 in volume 2.

4.3.1 Initial Conditions

The processor senses the BIC for a not-busy condition. The sense instruction places the BIC device address and a function code on the I/O bus. The BIC responds with a low SERX-I if it is not busy (CDCX-B low). The processor then executes the initialize instruction which generates a low INIT- which prepares BIC for receiving the initial and final addresses of the block data to be transferred.

The initial register is loaded from the I/O bus when data ready DRYX—I returns high and LIxx— is low.

The final register is loaded from the I/O bus when DRYX—I returns high, and LFRX + is high.

4.3.2 Device Selection

The processor executes the activate BIC instruction which causes DCEX-B to go low. This signal is sent to all peripheral controllers connected to the BIC. The processor then executes an instruction to select a peripheral device. This instruction with DCEX-B low, connects the selected device to the BIC and starts the device.

The connected peripheral controller sends a low CDCX-B to the BIC causing DCEX-B to go high, thus disabling the selection of any other peripheral controllers. When CDCX-B goes low, the connected peripheral controller also selects the state of TROX-B. When data is to be transferred to memory, a high TROX-B is sent. If data is to be transferred to memory, a low TROX-B is sent.

4.3.3 Data Address

When the connected peripheral controller is ready for the data transfer, it sends a low TRQX-B to the BIC. The BIC then sends a TPIX-I or low TPOX-I to the processor, depending on the state of TROX-B.

When the processor is ready for the data transfer, it sends a low IUAX—I to the BIC. IUAX—I going low generates a low TAKX—B which is sent to the peripheral controller to initiate the transfer. The BIC then causes OIRX + to go high which gates the memory address, that is in the initial register plus the key bits onto the I/O bus. The connected peripheral controller is thus enabled. FRYX—I, from the processor, going high terminates the address phase of the BIC. FRYX—I going high causes CLEX— to go high, which

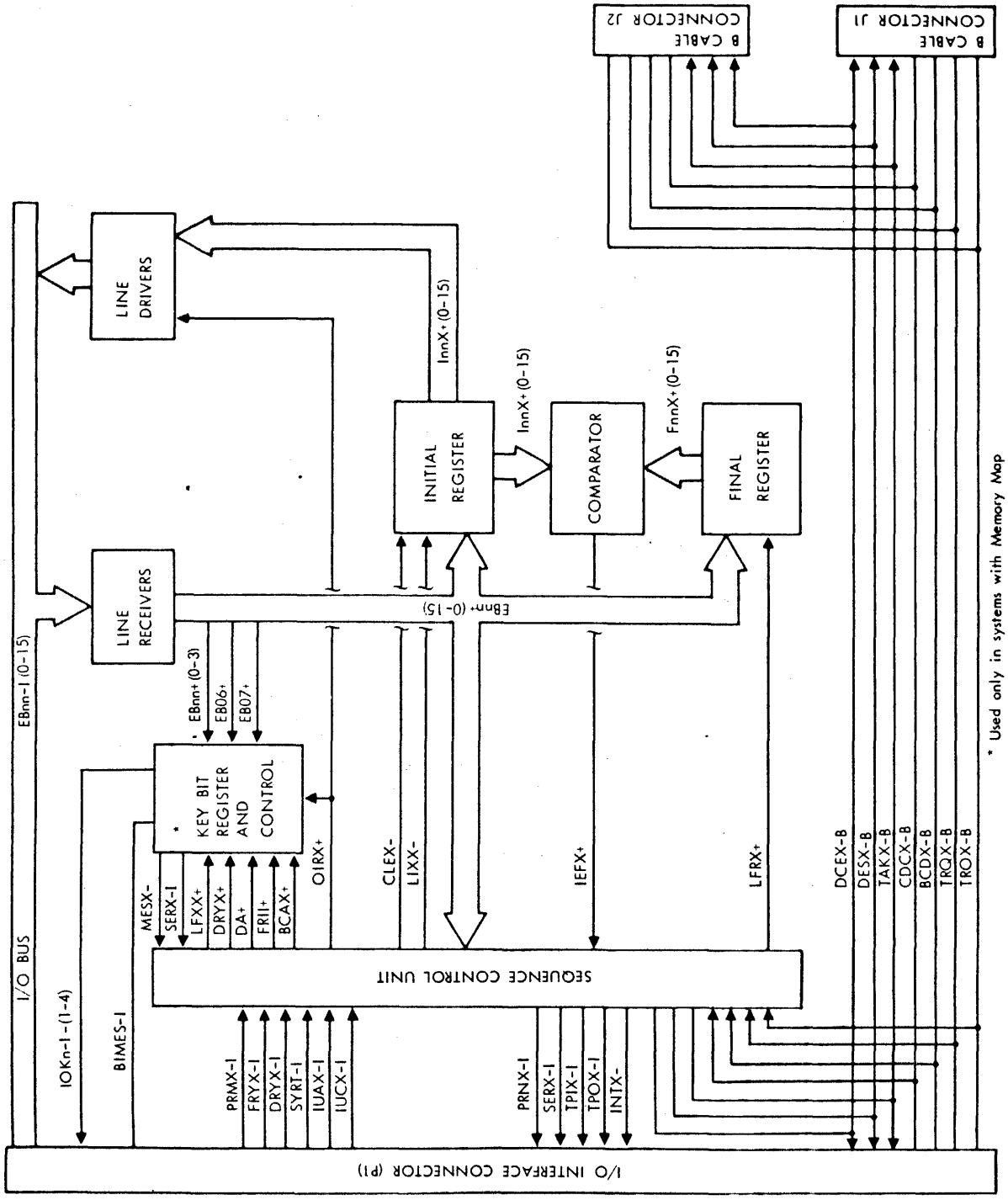


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Figure 4-1. BIC Block Diagram

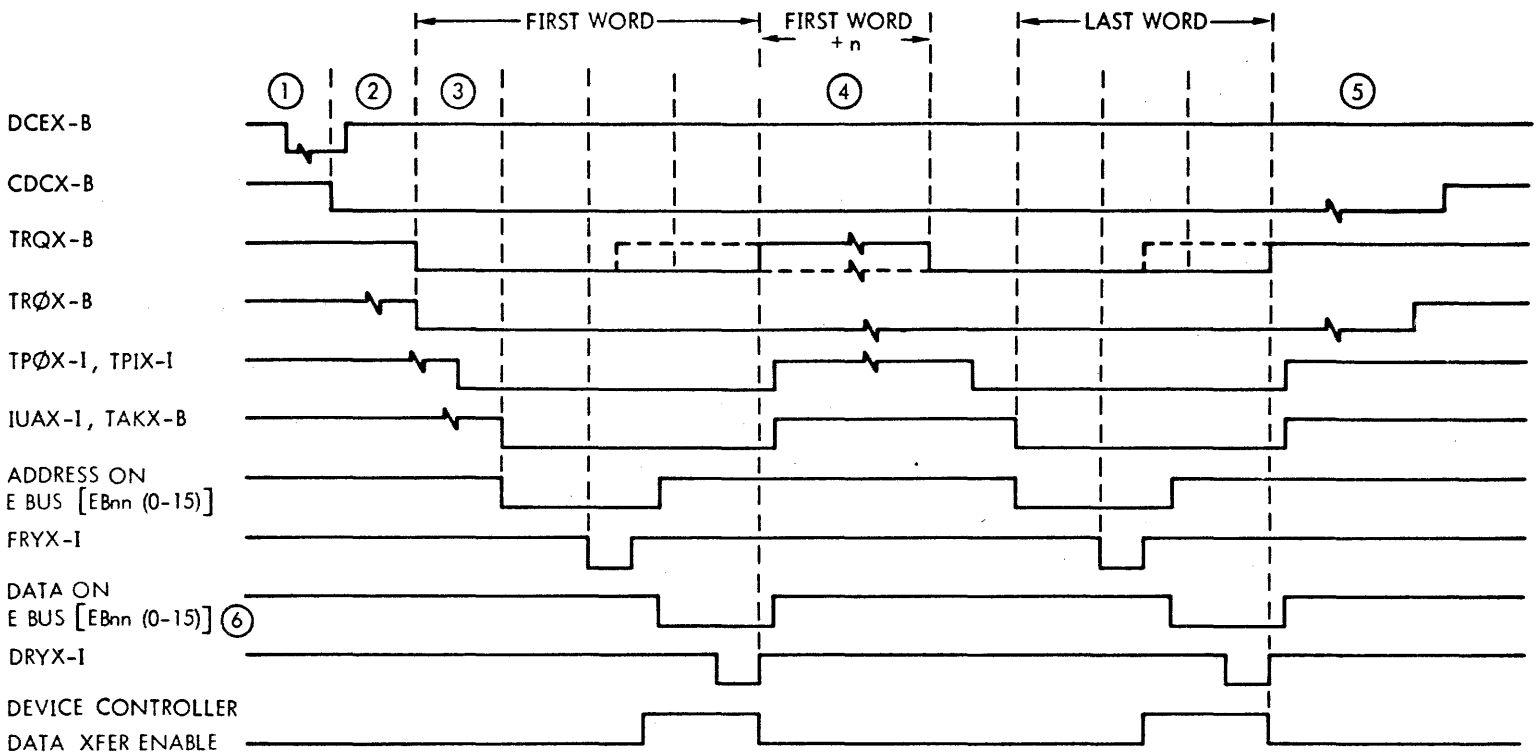

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Figure 4-2. BIC Trap Sequence Timing

NOTES:

1. TIMING REQUIRED TO ISSUE THE COMMAND TO CONNECT THE DEVICE.
2. TIME REQUIRED FOR DEVICE TO REQUEST FIRST DATA TRANSFER AFTER STARTING.
3. TIME REQUIRED TO SERVICE CURRENT AND/OR HIGHER PRIORITY REQUESTS FOR I/O ACCESSES.
4. SIGNAL TRQX-B MAY BE BROUGHT LOW (TRUE) AGAIN, AS EARLY AS THE TRAILING EDGE OF DRYX-I. HOWEVER, SIGNAL TRQX-B MUST HAVE BEEN HIGH FOR AT LEAST 50 NANOSECONDS BEFORE GOING LOW.
5. END OF DATA BLOCK. SIGNAL CDCX MAY REMAIN HIGH BETWEEN BLOCKS.
6. INCLUDES KEY BITS IF PRESENT [IOKn-I (0-3)].
7. FOR DMA TIMING REFER TO THE APPLICABLE SYSTEM HANDBOOK.

causes the initial register to be incremented to the next memory address.

4.3.4 Data Transfer

The data transfer may be an output from or an input to the processor. For output, the processor places the data on the I/O bus, and the data is strobed into the peripheral controller by DRYX-I going high. For input, the peripheral controller places the data on the I/O bus when FRYX-I goes high and removes the data when DRYX-I goes high. BIC keeps TAKX-B low until the end of the transfer when IUAX-I goes high.

4.3.5 Transfer Termination

When the contents of the initial and final registers become equal, the comparator circuit generates a high IEFX—. This creates a low DESX—B which is sent to the peripheral controller. The peripheral controller then causes CDCX—B to go high. This causes the BIC to assume a not busy state. The transfer of data is thus terminated.

When an abnormal device stop occurs, the peripheral controller terminates the transfer without regard to the contents of the initial and final registers. The peripheral controller generates a low BCDX—B. This causes a low DESX—B to be sent to the peripheral controller. The peripheral controller responds with a high CDCX—B. This causes the BIC to assume a not busy state. The transfer of data is thus terminated. After an abnormal device stop, the processor can read the contents of the initial register to determine the number of words that were transferred. The number in the initial register will be the address of the last word transferred plus one.

An abnormal device stop can occur as a result of any of the following situations: the length of the data block is unknown, and the device has detected the end of the data; the peripheral controller has detected an invalid operation of the device; the processor has issued an instruction to stop the operation of the peripheral device.

Another abnormal stop is created when an error is detected by the memory map during a BIC operation. The error causes BIMES—I to go low. This causes a low DESX—B to be sent to the peripheral controller. The peripheral controller responds with a high CDCX—B. This causes the BIC to assume a not busy state. The transfer of data is then terminated.