SPERRY UNIVAC

V77-600 and V76 Megamap

Operation and Service

Mini-Computer Operations

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UNIVAC®

V77-600 and V76 MEGAMAP

Model 77-3301; P/N 01P1938-001

Model 76-3301; P/N 01P1938-000

Operation and Service Manual

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CHANGE RECORD

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LIST OF EFFECTIVE PAGES

Page Number	Change in Effect
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SECTION 1
GENERAL DESCRIPTION

The SPERRY UNIVAC 77-600 and V76 Megamap Manual describes the memory and its interface with SPERRY UNIVAC 77-600 and V76 computers.

The manual is divided into six sections:

- Introduction to the megamap, related publications, specifications, and glossary
- Installation and interconnection data
- Operation
- Maintenance
- Mnemonics List

Documents such as logic diagrams, schematics, and parts lists are supplied in a system documentation package. This manual is assembled when the equipment is shipped, and reflects the configuration of the specific system.

The following list contains the part numbers of other manuals pertinent to the 77-600 and V76 computers (the x at the end of each document number is the revision number and can be any digit 0 through 9):

V70 Series Architecture Reference Manual	98A 9906 00x
Processor Manual	98A 9906 02x
Option Board Manual	98A 9906 05x
V76 System Reference Manual	98A 9906 23x
64K Semiconductor Memory (660 ns)	98A 9906 26x
Cache Manual	98A 9906 28x
77-600 System Reference Manual	98A 9906 40x
MAINTAIN III Manual	98A 9952 07x

The megamap performs address relocation and memory protection for up to 1024K words (K = 1,024) of physical memory by translating the 16-bit memory address and a 4-bit key into a 20-bit physical address. Mapping operations can be performed independently in up to sixteen 32K logical (virtual) memory areas. A 64K-mode of operation is available to provide eight 64K logical-memory areas. Map numbers 0 through 15 are used to identify the logical memory area, with map 0 being reserved for the VORTEX II operating system. The logical memory addresses are mapped into physical memory pages consisting of 512 words each. Page assignments for each logical memory are under control of the VORTEX II page-allocation routine.

NOTE

Although the VORTEX II operating system is referred to in this manual, the megamap consists of general-purpose hardware that allows operation in other software environments.

Figure 1-1 is a block diagram showing the address translation that is performed by the megamap. Either the processor or priority memory access (PMA) option generates a 16-bit logical address plus a 4-bit key. The most-significant seven bits of the address are combined with the key bits to address a location in the megamap's random-access-memory (RAM) array. The RAM array produces a 13-bit output consisting of two fields:

a. An 11-bit field that is concatenated with the least-significant 9-bit field of the logical address to form the 20-bit physical address.

b. A 2-bit field used for access control.

The most-significant four bits of the physical address are decoded to select one of the sixteen 64K memory banks. The other 16 bits of the physical address are used to address a location in the selected memory bank. The 2-bit access control field is used to provide full access, read only access, read operand only access, or no access to the memory page.

Specifications for the megamap are listed in table 1-1. A glossary of terms used in this manual is provided in table 1-2.

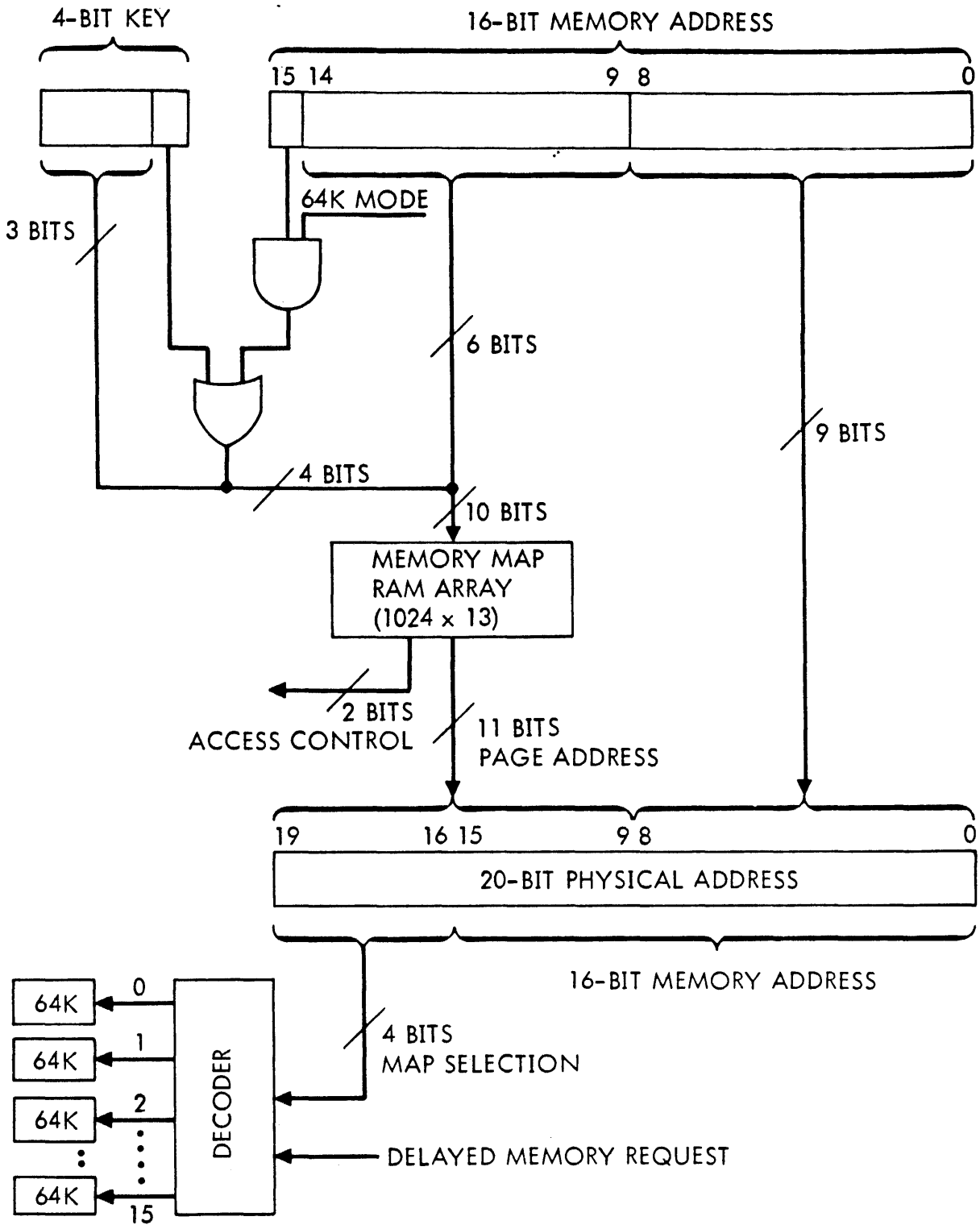

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Figure 1-1. Megamap Address Formation

Table 1-1. Megamap Specifications

Parameter	Specification
Physical memory size	Up to 1024K words.
Logical memory size	Two modes are available: a. up to 32K words b. up to 64K words
Page size	512 words.
Number of logical memory areas	Up to 16 with 32K or 8 with 64K words. A combination of 32K and 64K words sizes is possible.
Memory access times	With the megamap active, memory access is delayed 120 nanoseconds. With the megamap inactive, memory access is delayed by 73 nanoseconds. These are worst-case delays for standard operating modes.
System configuration	Provides mapping of addresses for processor, DMA, and PMA on memory port B. Supports cache configurations.
Loading	The megamap RAM array is loaded and read via DMA operations. The loading word rate is 715 kHz; the reading word rate is 358 kHz.
Operating modes	User mode, executive mode, and inactive mode.
Priority assignments	The megamap's memory-protection feature is assigned the highest system priority. Priority assignment for DMA operation is made independently.
I/O Bus loading	0.36 milliamperes or 1/6 standard dc load.
Logic levels (internal)	High = +2.4 to +5.0V dc Low = 0 to +0.4V dc

Table 1-1. Megamap Specifications (Continued)

Parameter	Specification
Logic levels (I/O bus)	High = +2.8 to +3.6V dc Low = 0 to +0.5V dc
Dimensions	Contained on a 15.6 by 19 inch printed-circuit board.
Installation	Plugs into a V70 series mainframe chassis using one module slot.
Input power	+5V dc at 9 amperes.
Operational environment	0 to 50 degrees C, 0 to 90 percent relative humidity without condensation.

Table 1-2. Glossary

Term	Definition
Logical address	An address in a logical memory area.
Logical memory	A set of memory locations used by the programmer. Logical memory may or may not have contiguous physical memory locations.
Map numbers	Numbers 0 through 15 assigned to the maps used by the operating system and the various users. The numbers are determined by four key bits originating from either the BIC, PMA, or map key register.
Mapping	The process of translating a logical memory address to a physical memory address.

Table 1-2. Glossary (continued)

Term	Definition
Page	A 512-word block of physical memory.
Physical address	An address in physical memory.
Physical memory	Random-access memory defined by hardware.
Privileged instruction	Any instruction that causes a memory protection violation when used in the user mode (i.e., halt and I/O instructions). The halt instruction is permitted only in the inactive mode.

SECTION 2
INSTALLATION

2.1 INSPECTION

The megamap has been packed and inspected to ensure its arrival in good working order. To prevent damage, take care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. Ascertain that wires and cables are neither loose nor broken, and that hardware is secure. If damage exists:

a. Notify the transportation company.

b. Notify Sperry Univac.

c. Save all packing material.

2.2 PHYSICAL DESCRIPTION

The megamap circuits are on a 15.6 by 19 inch printed-circuit (PC) board (p/n 44P0785). Figure 2-1 shows dimensions and connectors of the megamap board.

2.3 DISCRETIONARY WIRING

Connections of the various jumper terminals on the megamap PC board are listed in the megamap option drawing (01A1938). These connections are normally installed at the factory, but are referenced here in case the user wishes to have his megamap system expanded or changed in the field. The jumper-terminal designations referred to in the option drawing appear on the megamap board adjacent to the particular terminal and in the logic diagram.

2.4 INTERCONNECTION

The megamap board plugs into a single module slot of the V70 series mainframe chassis. Functions of the memory map board connectors are listed as follows:

P1, mainframe memory

J2, cache connection

J3, option-board auxiliary I/O bus

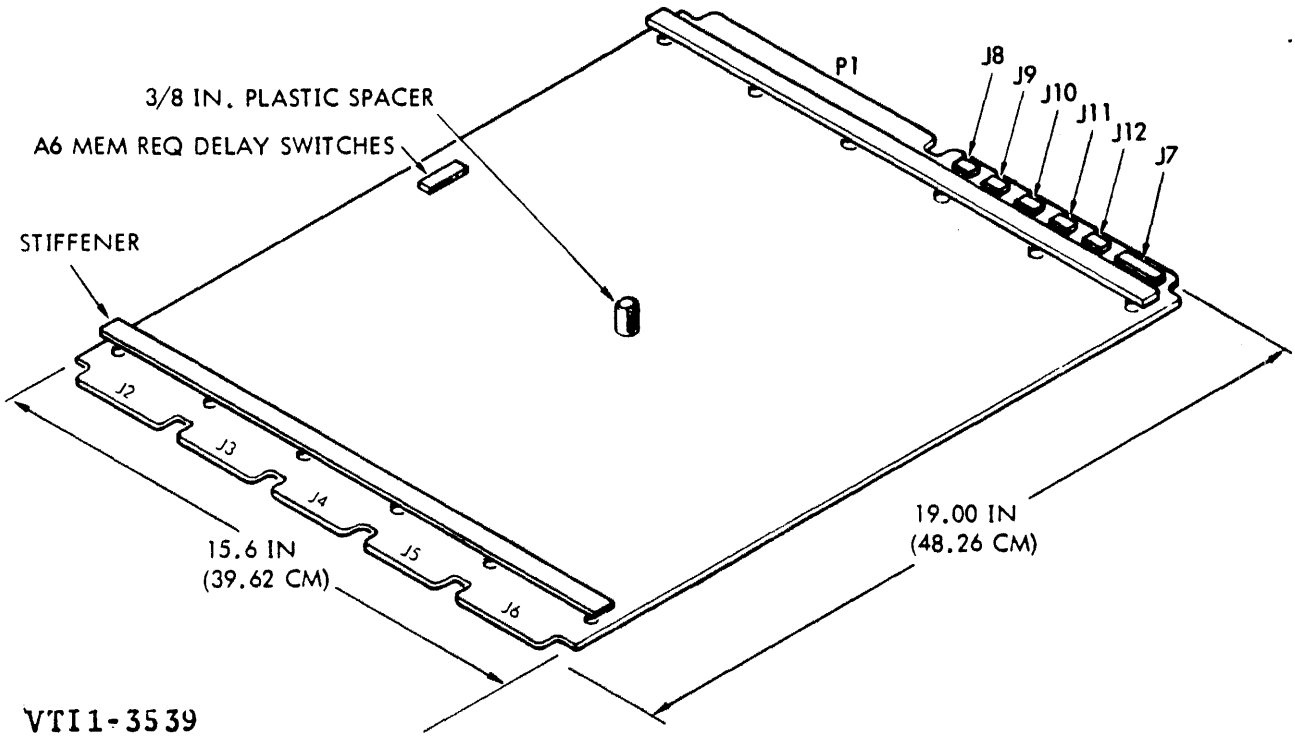

Figure 2-1. Megamap Board

J4, processor

J5, I/O bus

J6, option board and processor

J7, power

J8 through J12, 64K bank selections

Power supplied to the megamap board via connector J7 is normally provided by a +5-volt power supply (p/n 01P1280). It may also be supplied by excess +5-volt power from a memory expansion supply.

Figure 2-2 shows the megamap board interconnection in a V70 series mainframe. Pin assignments for the connectors on the megamap board are provided in the logic diagram (p/n 91C0569) in the system documentation package.

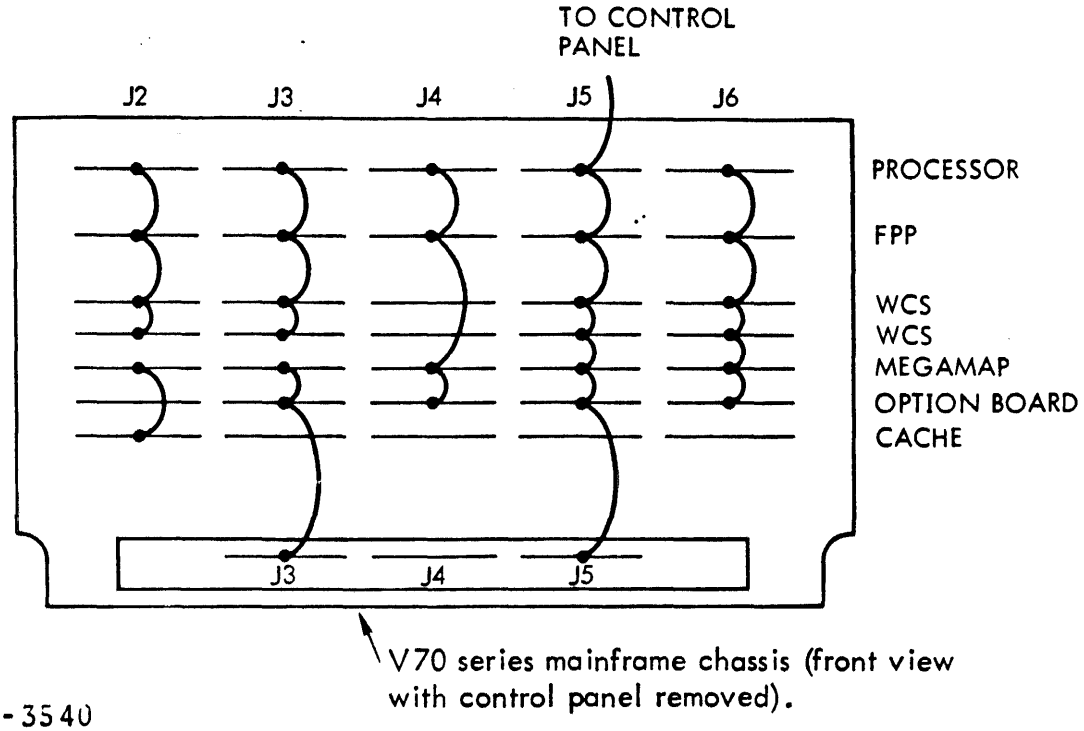

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Figure 2-2. Megamap Interconnection

2.5 CONFIGURATION

The normal megamap configuration is supported by VORTEX II and has the following characteristics:

a. The processor key bits are provided by the key register (section 4.3) on the megamap board.

b. The active megamap is placed in the executive mode (section 3.2) on any interrupt.

c. The megamap enters the user mode (section 3.2) by the EXC2 0246 instruction followed by a jump instruction (section 3.1).

d. Privileged instructions are assigned to map 0.

SECTION 3
OPERATION

The megamap contains no operating controls or indicators. Operation of the megamap is normally controlled by the VORTEX II operating system. However, by writing his own control program, the user can operate the megamap without using VORTEX II. For maintaining and testing the megamap, a MAINTAIN III memory map test program is available in the MAINTAIN III Reference Manual.

3.1 I/O INSTRUCTIONS

Megamap I/O instructions can only be executed from map 0 (operating system) or an inactive memory map. Table 3-1 lists the I/O instructions with the mnemonics and octal codes for device address 46. An alternate device address is 56.

Table 3-1. I/O Instructions

Mnemonic	Octal Code	Function
External Control		
EXC2 046	104046	Executive Mode to Inactive Mode. Places the megamap in the inactive mode upon fetching the contents at the effective address of the jump instruction that follows.
EXC2 0146	104146	Inactive Mode to Executive Mode. Places the megamap in the executive mode upon fetching the contents at the effective address of the jump instruction that follows.
EXC2 0246	104246	Executive Mode to User Mode. Places the megamap in the user mode upon fetching the contents at the effective address of the jump instruction that follows.
EXC2 0346	104346	Start DMA Transfer. Starts a megamap DMA transfer.
EXC2 0446	104446	Reset DMA Transfer. Resets the megamap's DMA-transfer logic.

Table 3-1. I/O Instructions (continued)

Mnemonic	Octal Code	Function
EXC2 0546	104546	Clear Executive-Mode Mask. Removes the executive-mode mask.
EXC2 0646	104646	Enable Memory Protection. Enables the memory protection function of the megamap.
EXC2 0746	104746	Disable Memory Protection. Disables the memory protection function of the megamap.
Sense		
SEN 046	101046	Sense DMA Activity. Senses if the megamap is performing a DMA operation.
SEN 0146	101146	Sense Abnormal DMA Termination. Senses for the error termination of a DMA loading or read-back operation.
Transfer*		
IME 046	102046	Transfers data from megamap to main memory.
INA 046	102146	Transfers data from the megamap to the A register.
INB 046	102246	Transfers data from the megamap to the B register.
CIA 046	102546	Transfers data from the megamap to the cleared A register.
CIB 046	102646	Transfers data from the megamap to the cleared B register.
OME 046	103046	Transfers data from main memory to the megamap.
OAR 046	103146	Transfers data from the A register to the megamap.
OBR 046	103246	Transfers data from the B register to the megamap.

*These transfer instructions are for control registers in the megamap. High-speed DMA operations are used for loading and reading the megamap RAM array.

3.2 OPERATING MODES

The megamap has three modes of operation: inactive, executive, and user.

3.2.1 Inactive Mode

When the megamap is in the inactive mode, the first 32K of physical memory is available unmapped and all instructions are permitted. This mode is entered by either a system reset condition or a branch sequence from the executive mode consisting of the EXC2 046 instruction followed by a jump instruction.

3.2.2 Executive Mode

This mode is entered from the user mode by an interrupt or from the inactive mode by a branch to an active-map condition. The branch sequence is an EXC instruction followed by any jump instruction. In this mode, all instructions except HLT are permitted. From the executive mode, the megamap can be switched to the inactive mode by using a branch sequence.

The executive mode has four states that define operations occurring between map 0 and the user maps. Setting up of the executive mode states is accomplished with I/O instructions under control of the VORTEX II operating system. As shown in table 3-2, instruction-fetch operations are always from map 0, while operand-fetch and operand-store operations can be from any map depending on the executive-mode state. The following are exceptions:

a. To ensure that all instruction fetches are from map 0, indirect addressing must not exceed the first level in states 2 or 3 of the executive mode. This is because after the first level of indirect addressing, instruction fetches in some cases (i.e., SRE and IJMP instructions) are treated as operand fetches by the memory map.

b. In all executive-mode states, the execution of a jump-and-mark instruction causes the program-counter contents to be stored in map 0.

c. In all executive-mode states, the execution of a LDAI, LDBI, or LDXI instruction causes the effective register to be loaded with the operand fetched from map 0.

d. Any interrupt causes the megamap to enter the masked executive mode. This masked condition causes the executive mode to operate as if it were in state 0 even though the executive-state register may contain another value. In this condition, megamap status is read into map 0 during the interrupt service routine. By executing the EXC2 0546 instruction, the mask is removed and the executive mode returns to the state determined by the value in the executive-state register.

Table 3-2. Executive-Mode States

State	Instruction Fetch	Operand Fetch	Operand Store
0	Map 0	Map 0	Map 0
1	Map 0	Map 0	Map n
2	Map 0	Map n	Map 0
3	Map 0	Map n	Map n

Note:

1. Map 0 refers to the operating system.
2. Map n refers to the user map specified by the map key bits.
3. States 1 through 3 cause an additional 246 nanoseconds delay in memory accessing.

3.2.3 User Mode

In this mode, all operands and instructions are mapped according to the map key bits and the contents of the RAM array. If an interrupt occurs, the memory map is switched to the executive mode. Entry to the user mode is by a jump following an EXC2 instruction.

3.3 MAPPING

The mapping function is performed for either a DMA, PMA, or processor operation. In DMA operations, the mapped address utilizes the 4-bit key from the BIC plus the 16-bit logical address from the processor DMA memory control. In PMA operations,

the mapped address utilizes the 4-bit key from the block-transfer controller (BTC) plus the 16-bit logical address from the PMA option. In processor operations, the mapped address is normally derived from the megamap's key register and the 16-bit logical address from the processor.

3.4 OPERATING SEQUENCES

This section describes the sequences of the various megamap operations. Figures 3-1 and 3-2 show the data-word formats used with output- and input-data transfers, respectively. The cache control functions (figure 3-1a) are described in detail in the V70 Cache Manual (98A9906-28x). Figure 3-3 shows the data-word format for the megamap loading and read-back operations.

3.4.1 Megamap Loading and Read-Back

The following sequences occur in megamap loading and read-back operations via DMA (using map 0):

a. The processor issues the EXC2 0446 instruction to reset the DMA-control logic in the megamap.

b. Using output-data transfer instructions, (OME, OAR, or OBR), the processor transfers three data words to the megamap. The first word contains the direction of DMA transfer and the initial 10-bit map address (figure 3-1b). The second word contains the initial 16-bit memory address of the DMA transfer (figure 3-1c). The third word contains the number of words in the DMA transfer (figure 3-1d).

c. The processor issues the EXC2 0346 instruction to start DMA transfer operation. Data is transferred using the data word format of figure 3-3.

d. The standard method for verifying the completion of DMA transfers consists of using the two SEN instructions. The processor issues SEN 046 to sense if the megamap is still performing the DMA transfer. If it is not performing the DMA transfer, SEN 0146 is issued to sense if the DMA-transfer termination is due to an error.

e. An optional method for verifying the completion of DMA transfers consists of using the DMA-completion interrupt. A counter in the megamap counts the number of DMA transfers and indicates when all transfers are complete. An interrupt is sent to the processor when either all transfers are completed or an error occurs

during one of the transfers. When the interrupt is acknowledged, the processor is directed to memory address 016. This option is configured by jumpers.

NOTE: If the DMA-completion interrupt is not used, the EXC2 446 instruction should be executed following the sensing of the DMA-transfer completion.

3.4.2 Programmed I/O Read-Back

This operation provides a read-back function of the megamap's internal-status signals (figure 3-2a), instruction address register (figure 3-2b), and the unassigned address register (figure 3-2c). The sequences of operations are listed below:

a. Using an output-data transfer instruction, the processor transfers a control word (figure 3-1c) to the memory map. The type of data to be read back is specified by bits 10 and 11 of this control word.

b. Using an input-data transfer instruction (IME, INA, INB, CIA, or CIB), the processor reads back the data specified by the control word.

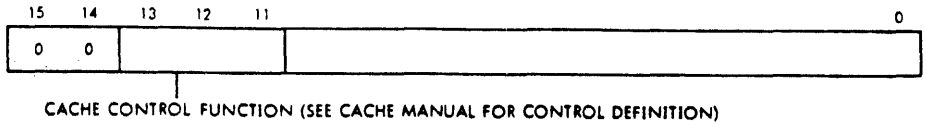
3.4.3 Executive Mode to Inactive Mode

The following sequences occur when the megamap is switched from the executive mode to the inactive mode:

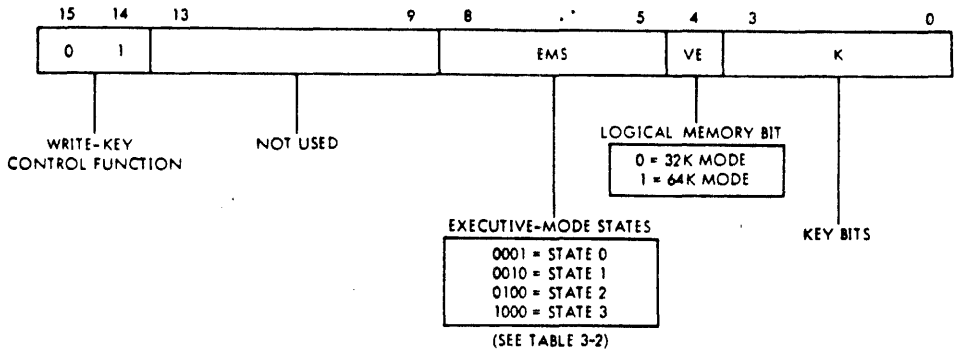
a. The processor issues the EXC2 046 instruction to enable switching to the inactive mode.

b. The processor executes a jump instruction. If the jump condition is not met, the megamap remains in the executive mode and enabled for mode switching.

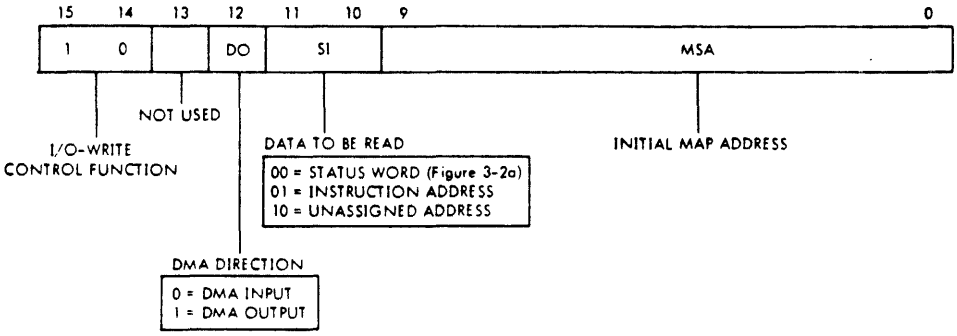
c. If the jump condition is met, the megamap switches to the inactive mode when the contents of the effective jump address are fetched. The effective jump address is not mapped.



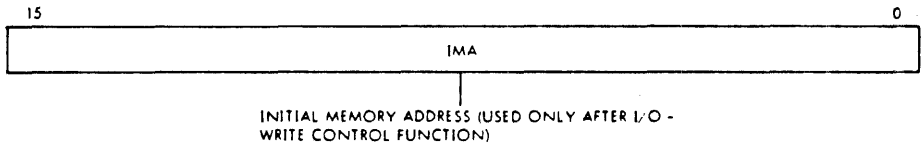
a. Cache Control Function



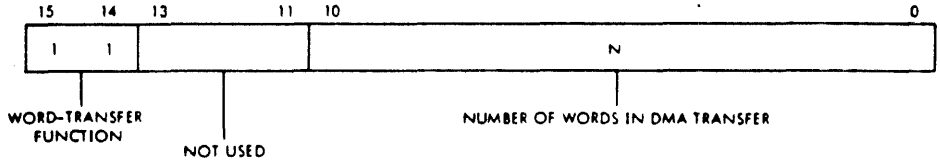
b. Write-Key Control Function



c. I/O-Write Control Function



d. Initial Memory Address of a DMA Transfer



e. Word-Transfer Function

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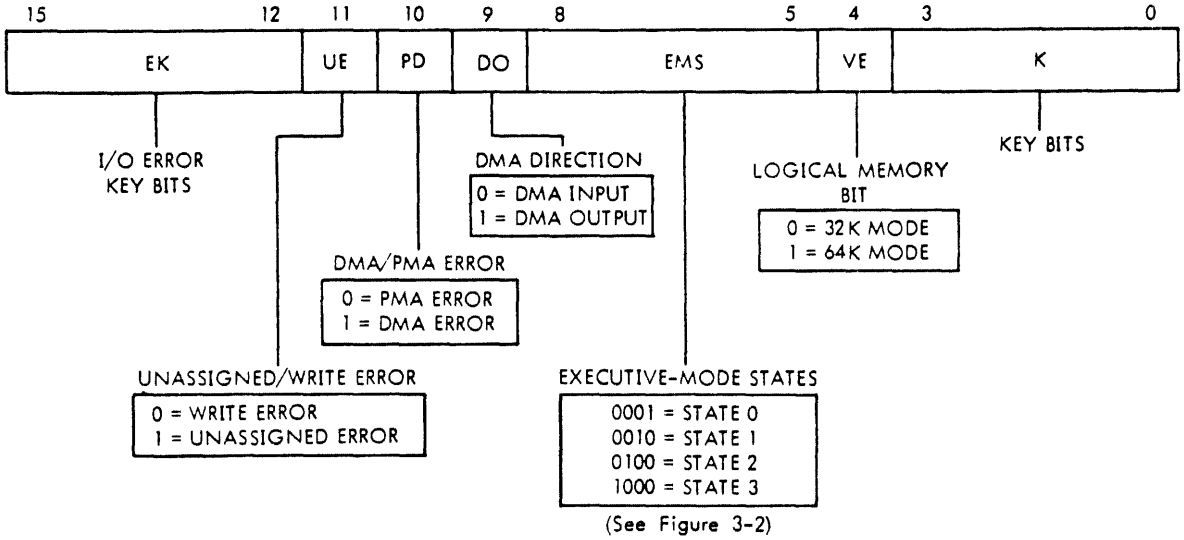
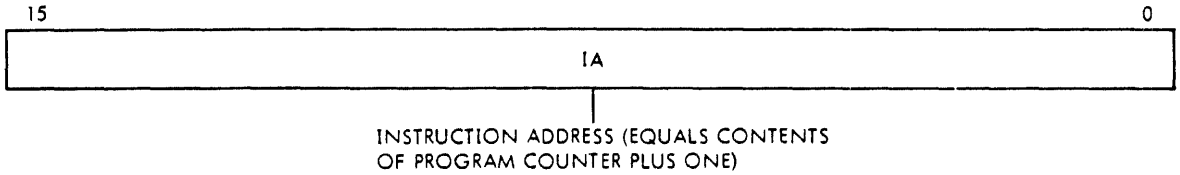
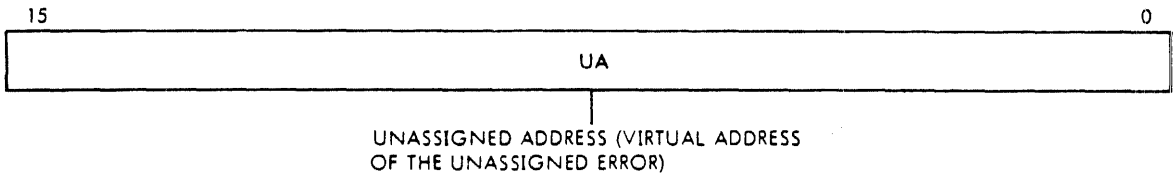
Figure 3-1. Data Word Formats for Output-Data Transfers (For Map Setup and Control)



a. Status Word



b. Instruction Address



c. Unassigned Address

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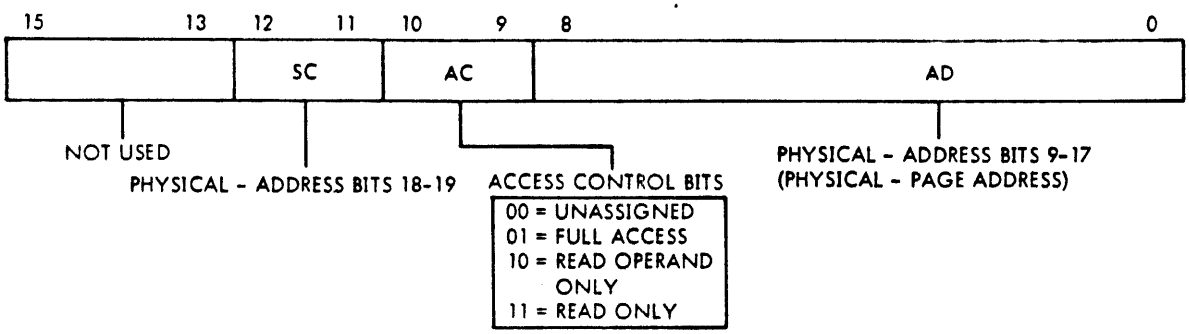
Figure 3-2. Data-Word Formats for Input-Data Transfers



VTI1-3499A

Figure 3-3. Data-Word Format For Megamap Loading and Read-Back Operations

3.4.4 Inactive Mode to Executive Mode

The following sequences occur when the megamap is switched from the inactive mode to the executive mode:

a. The processor issues the EXC2 0146 instruction to enable switching to the executive mode.

b. The processor executes a jump instruction. If the jump condition is not met, the megamap remains in the inactive mode and armed for mode switching.

c. If the jump condition is met, the megamap switches to the executive mode when the contents of the effective jump address are fetched. The effective address is mapped using map 0.

3.4.5 Executive Mode to User Mode

The following sequences occur when the megamap is switched from the executive mode to the user mode.

a. The processor issues the EXC2 0246 instruction to enable switching to the user mode.

b. The processor executes a jump instruction. If the jump condition is not met, the megamap remains in the executive mode and armed for mode switching.

c. If the jump condition is met, the megamap switches to the user mode when the contents of the effective jump address are fetched. The effective address is mapped using the user map.

3.4.6 User Mode to Executive Mode

Switching the megamap from the user mode to the executive mode, can be initiated by interrupts resulting from the following:

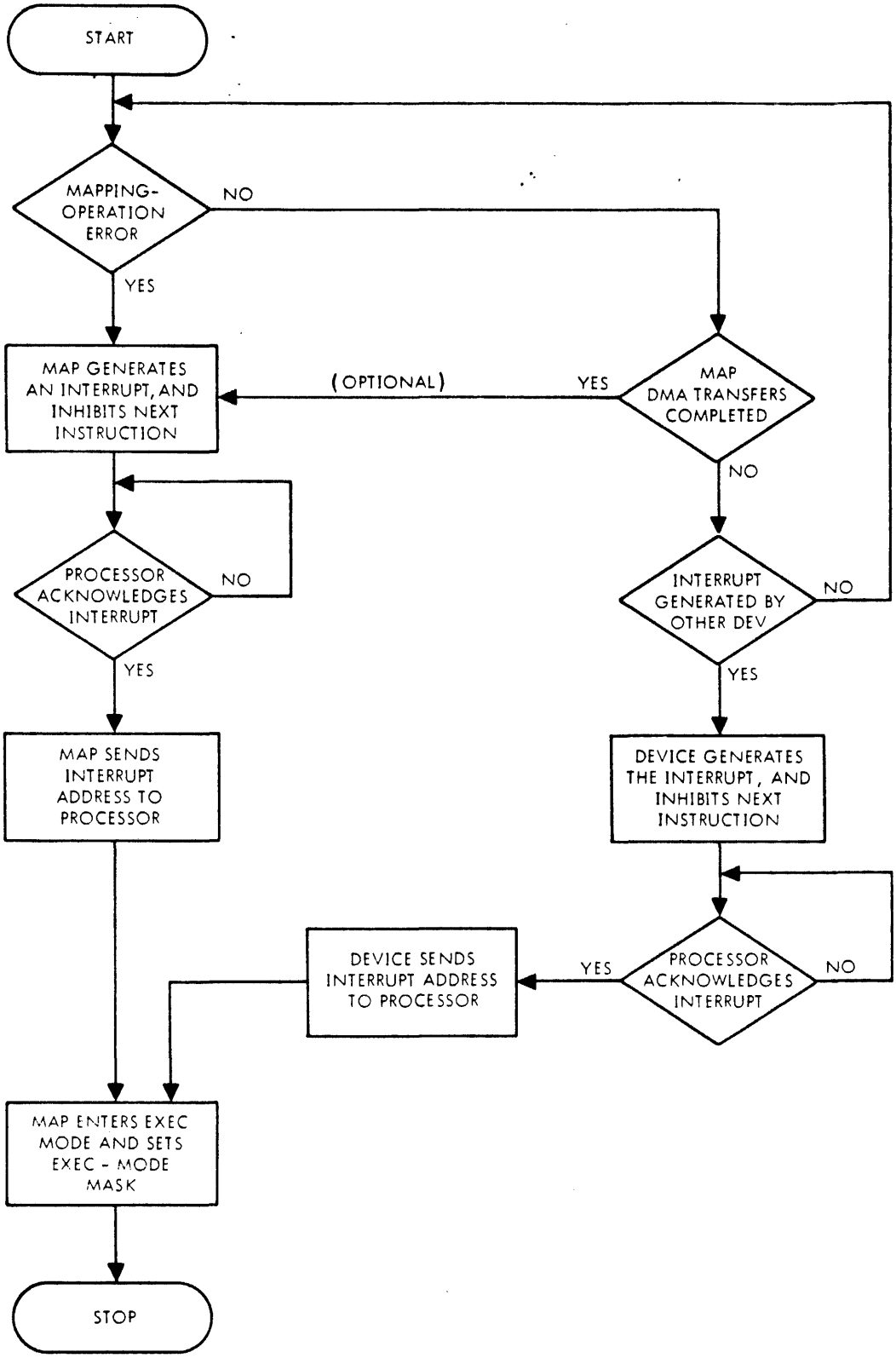
a. an error during a mapping operation

b. an I/O system interrupt

The sequences of this operation are shown in the flow chart of figure 3-4.

3.5 ACCESS-CONTROL MODES

Four access-control modes for mapping operations are provided by access-control bits 9 and 10 of the RAM-array data word (figure 3-3). The four modes with corresponding binary values of bits 9 and 10 are listed in table 3-3.



VTI1-2048

Figure 3-4. User Mode to Execute Mode Flow Chart

Table 3-3. Access-Control Modes

Bits 10	Bits 9	Mode	Function
0	0	Unassigned	The logical address is unassigned (non-resident address)
0	1	Full access	All types of access are permitted in this page.
1	0	Read operand only	Only operand fetches are permitted. Instruction fetches from this page will not be executed. This restriction includes execution instructions (XEC, XOF, etc.).
1	1	Read only	Only instruction or operand fetches are permitted in this page (no operand-stored operations permitted). The instruction fetches include single- and double-word instructions.

3.6 MEMORY PROTECTION

The memory protection function monitors the address of the instruction being processed on the basis of the access-control mode. When the megamap is active and its memory protection function is enabled, the instruction address register (in the megamap) is updated with each decoded instruction. When an error condition is detected, the memory protection function is disabled, and updating of the instruction-address register is inhibited until the EXC2 0646 instruction (enable memory protection) is executed. The detection of an error interrupts the program in process and directs it to one of seven preassigned memory addresses. These interrupt addresses are listed in table 3-4. Halt, I/O, and jump errors are detected earlier in the mapping operation to prevent them from being detected at the same time as the other errors.

Table 3-4. Interrupt Addresses

Octal Address	Error
20	Halt. The execution of a halt instruction is attempted.
22	I/O. The execution of an I/O instruction is attempted from a map number other than 0.
24	Write. An attempt is made to write into read-only or read-operand-only locations.
26	Jump. An attempt is made to jump into a read-operand-only location.
30	Unassigned. A read, write, or jump operation is attempted using an unassigned logical address.
32	Instruction fetch. An attempt is made to fetch an instruction from a read-operand-only location.
34	Data transfer. A write or unassigned error is detected during a DMA or PMA data transfer.

3.6.1 Halt Errors

When a halt error is detected, the execution of the halt instruction is allowed to be completed. However, due to the detection of the halt error, the megamap holds the memory-protection interrupt flag true (OINT-) so that the processor re-enters the run mode immediately after halting. The processor then goes to an interrupt-wait state until the program being processed is directed to the interrupt address 20. Upon completion of the hardware interrupt service, the interrupt signal OINT- is reset. A halt error is not detected when the halt is initiated manually using the STEP/RUN switch on the computer control panel.

3.6.2 I/O Errors

When an I/O instruction error is detected, the execution of the I/O instruction is allowed to be completed. However, all I/O control functions and data transfers between the processor and peripheral controllers are inhibited. By holding the I/O instruction error flag true, the contents of memory and the

A, B, and X registers cannot be modified by the I/O instruction. When the execution of the I/O instruction is completed, the program being processed is directed to the interrupt address 022.

3.6.3 Writing Errors

When a writing error is detected, the execution of the instruction is allowed to be completed. To prevent memory modification, the writing cycle for memory is changed to a reading cycle. When the execution of the instruction is completed, the program being processed is directed to the interrupt address 024.

Even though the writing error is not detected because the memory protection function is disabled, the active megamap always changes the writing sequence to a reading sequence if an attempt is made to write into a non full-access location. This protection applies to all DMA, PMA (if connected to megamap), and processor memory cycles.

3.6.4 Jump Errors

A jump error can occur during the following types of instructions:

a. All jump instructions including IJMP, JSR, and BT

b. All jump-and-mark instructions including SRE

A jump error occurs when an attempt is made to jump or skip to a read-operand-only location and if this location is the effective address of the jump or skip instruction.

When a jump error is detected, the execution of the instruction is allowed to be completed. For jump-and-mark instructions, the memory writing cycle is changed to a reading cycle to prevent memory modification. When the execution of the instruction is completed, the program being processed is directed to the interrupt address 026.

3.6.5 Unassigned Errors

When an unassigned error is detected, the execution of the instruction is allowed to be completed. If a memory writing cycle contains the unassigned error, it is changed to a reading cycle. When the execution of the instruction is completed, the program being processed is directed to the interrupt address 030. The unassigned logical address is contained in the megamap's unassigned address register, which can be read by the processor using an input-data transfer I/O instruction (figure 3-2c).

3.6.6 Instruction-Fetch Errors

When an instruction-fetch error is detected, the execution of the current instruction is allowed to be completed but the next erroneous instruction is not executed. The program being processed is directed to the interrupt address 032.

3.6.7 I/O Data-Transfer Errors

The detection of an I/O data-transfer error during a DMA or PMA operation causes the megamap to generate an interrupt that directs the processor to the interrupt address 034.

When an I/O data-transfer error occurs during a DMA operation, the megamap holds the DMA termination signal (BIMES-I) true. This causes the selected BIC (or a user-designed controller) to terminate the data transfer on the trailing edge of the data-ready signal (DRYX-I or DRYF-I).

When a data-transfer error occurs during a PMA operation, the megamap holds the PMA termination signal (BTMES-I) true. This causes the block-transfer controller (or a user-designed controller) to terminate the data transfer immediately after receiving the termination signal.

When an I/O data-transfer error occurs, the megamap stores error-status data that include error-key number, writing or unassigned error, and DMA or PMA error. This error-status data (figure 3-2a) can be read by the processor by using an input-data transfer instruction.

When an I/O data-transfer error is detected during a megamap DMA loading or read-back operation, the memory map generates a DMA error flag (PDMTRM+). In response to the SEN 046 instruction, the memory map provides a DMA not-busy status.

An optional mode of operation, for the detection of an I/O data-transfer error in a DMA loading or read-back operation, consists of using the DMA completion interrupt. When the error is detected, the megamap generates the interrupt directing the processor to the interrupt address 016. The same interrupt is also generated to signal the processor when the loading or read-back operation is successfully completed. Upon receipt of this interrupt, the processor can issue the SEN 0146 instruction to sense if the DMA transfer termination is due to an error.

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

This section contains system and functional descriptions followed by timing waveforms for the various megamap operations. For ease of reading, some mnemonics are written with the variable n in place of the actual numbers. For example, memory data mnemonics MYDA00- through MYDA17- are written MYDAn-(0-17). Mnemonic descriptions are provided in section 6.

4.2 SYSTEM DESCRIPTION

The system block diagram of figure 4-1 shows the map configuration without cache. Figure 4-2 shows the map/cache system configuration. The processor/map memory connection is always made on the B port. When a cache is in the system, both A and B ports are utilized, with data transferred between the memory and cache on the A port, and between the cache and processor-PMA on the B port. In the cache system, the map supplies physical addresses to the A port during memory service to the cache.

The map provides decoded requests for sixteen 64K memory banks. The request for the first 64K is sent to the main memory bus, while the other selections are supplied over individual memory request cables. This fact, along with drive limitations on the memory bus and data lines, restricts the types of memory modules which can be used to expand the system above 64K.

4.3 FUNCTIONAL CIRCUITS

The functional circuits of the megamap are shown in figure 4-3. Page numbers of the megamap logic diagram (p/n 91C0569 in System Maintenance Manual) are provided in parentheses for each circuit block.

4.3.1 RAM Array Address Circuits

A 10-bit RAM address, PRAMAn-(0-9), is provided by the RAM address multiplexor to address one of 1024 13-bit locations in the array. The control signal PIIMRQ selects the required address source: the map address register PMARn+(0-9) or megamap input bits MYMBn+(9-15) and key multiplexor bits PRKMMXn+(0-3).

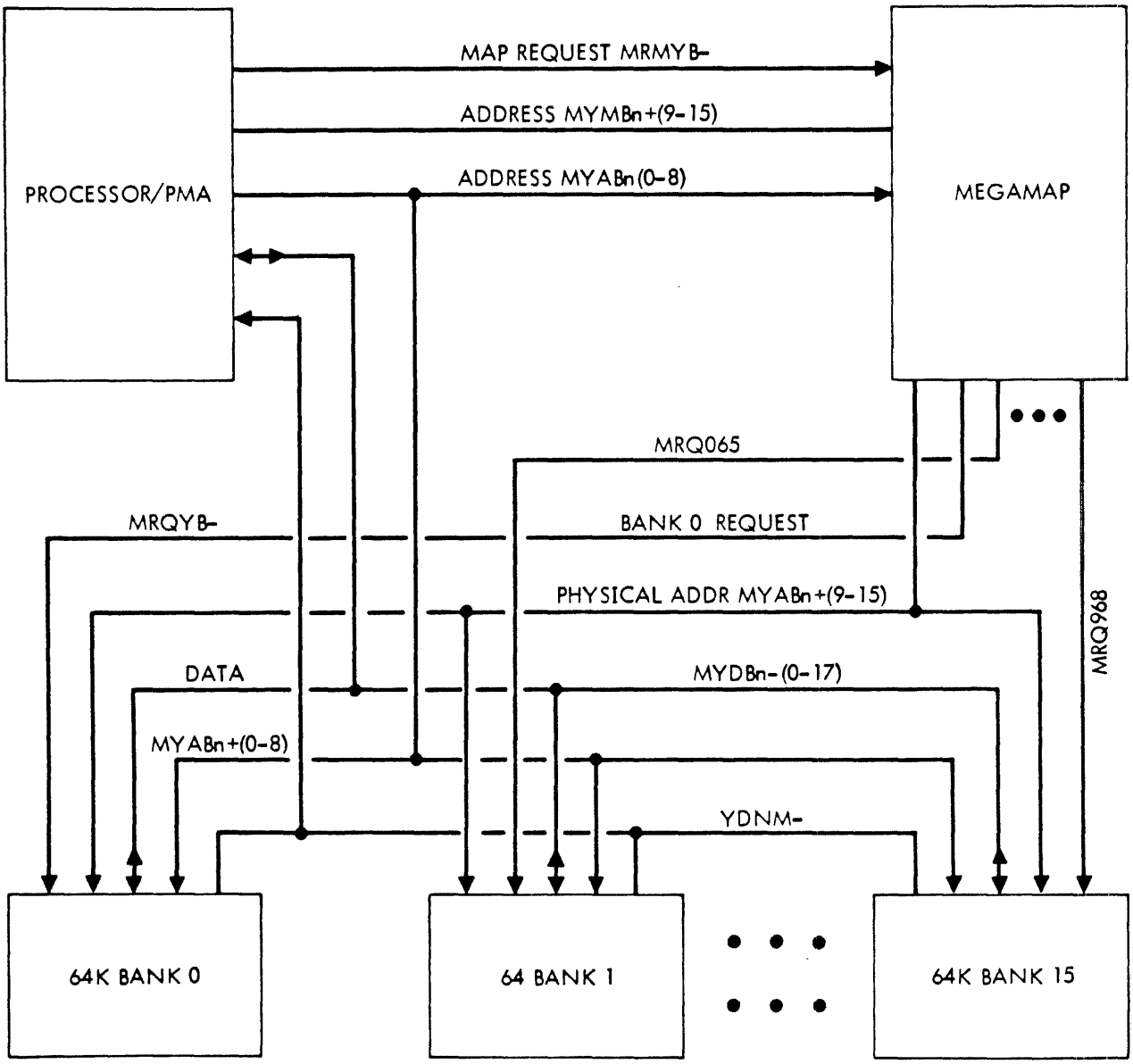


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Figure 4-1. Megamap System Without Cache

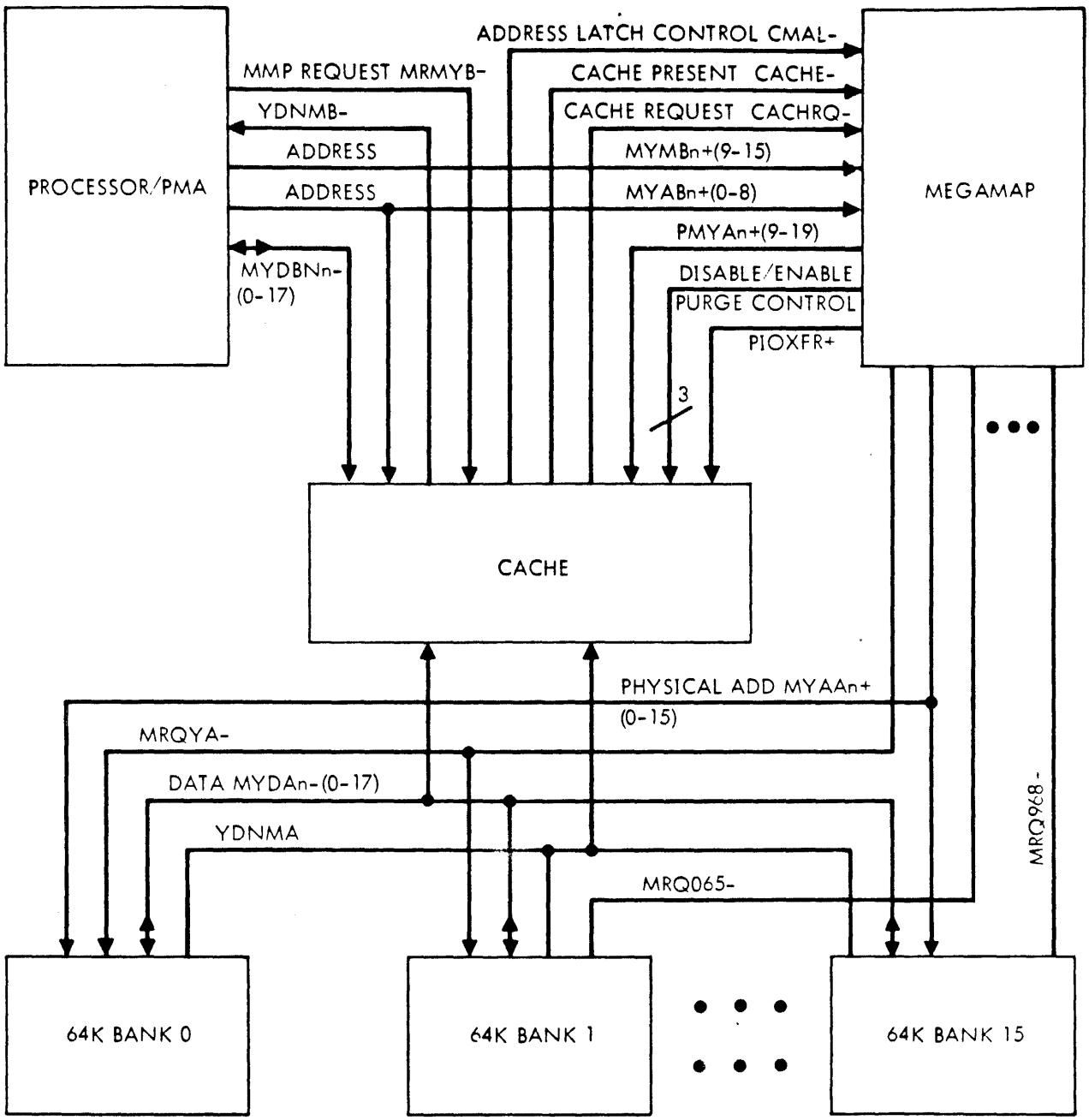

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Figure 4-2. Megamap System With Cache

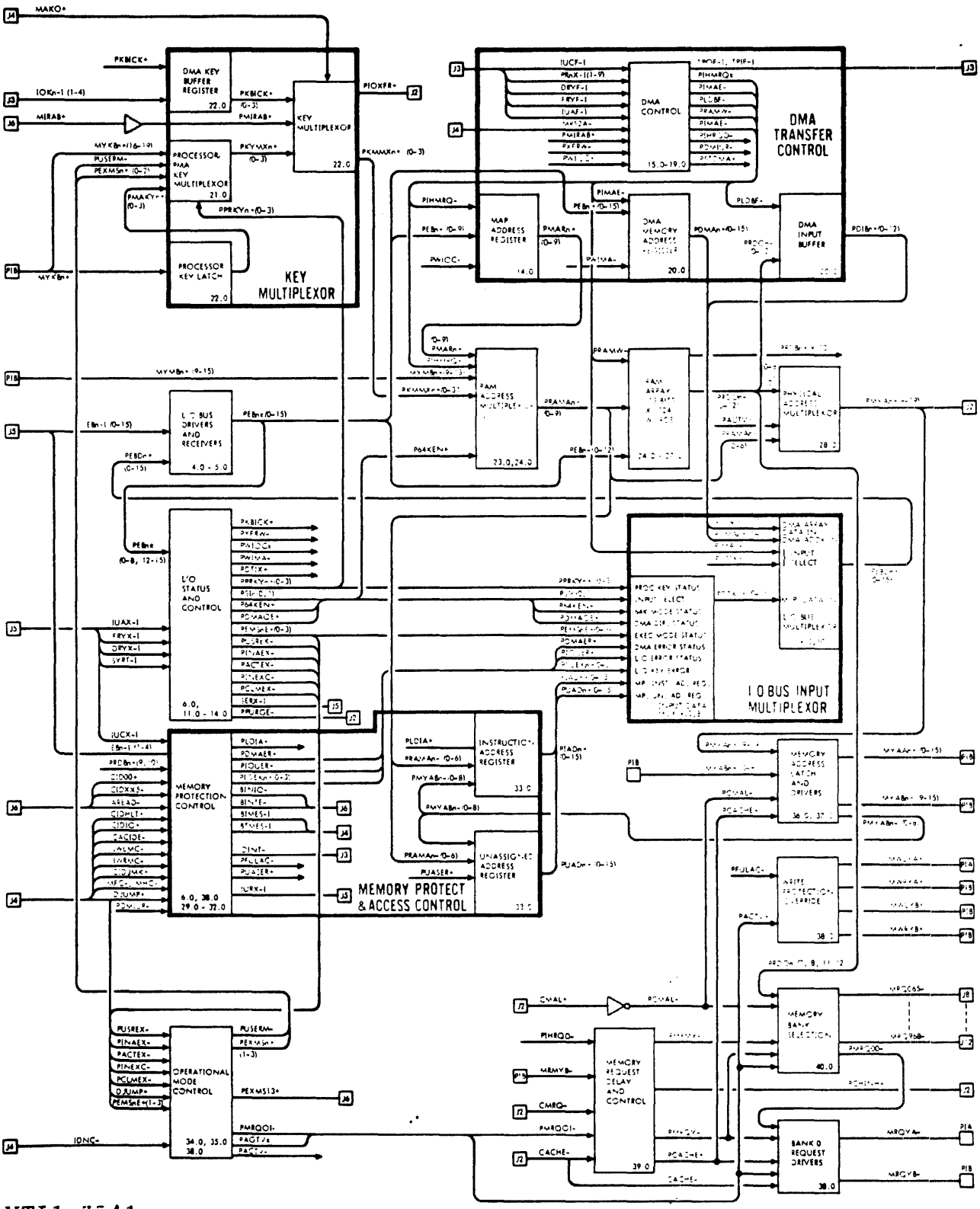

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Figure 4-3. Megamap Functional Block Diagram

4.3.1.1 Key Multiplexor

The key information is selected from the BIC key buffer register (loaded on every FRYX, FRYF) or from the processor/PMA key multiplexor. The control signal PMIRAB+ defines when the current memory transfer is a DMA transfer and selects the BIC key register.

4.3.1.2 Processor/PMA Key Multiplexor

This multiplexor selects key information from the memory bus key bits (for PMA) or the MAP II processor key register. If MAKO is active, the PMA key is selected.

4.3.2 Physical Address Multiplexor, PMYAn+(9-19)

This circuit selects the mapped physical address, PRDOn(0-8,11,12) if the map is in any active state. If map is inactive, the virtual or logical page, PRAMAn-(0-5), is the same as the physical. This physical address is sent to the cache via connector J2 for hit/miss comparison.

4.3.3 Memory Address Latch and Drivers

The low-order bits of the physical page address, bits PMYAn+(9-15), are passed through a latch. These bits drive MYABn+(9-15) when the cache is not present. The lower bits MYABn+(0-8) do not pass through the megamap for memory port B use.

When cache is present, the output of the latch drives MYAAn+(9-15). Also the lower bits MYABn+(0-8) are passed through a latch and driven to MYAAn+(0-8). If the cache requires service from main memory, it activates CMAL+ to hold the latched physical address during its main memory service.

4.3.4 Bank Selection Latch and Decoding Logic

The four bits of the physical address from the RAM, PRDOn-(7,8,11,12), are passed through a latch and are decoded by a one-of-16 decoder. The latch is under control of CMAL from the cache and functions to hold request stable during cache service to main memory. The decoded results are gated by active memory request (PMRQY-) and provide a decoded request signal to one 64K memory bank.

4.3.5 Bank 0 Request Drivers

Bank 0 is the only bank that can be accessed when the map is inactive. It will drive port B if cache is not present, and port A if cache is present.

4.3.6 Memory Request Delay and Control

The input memory request is inhibited by PIHRQD- if the array is being accessed for DMA transfer of its content. It is also inhibited during mode selection by PMRQOI- to ensure adequate mapping time for key changes (inactive to active, executive to user, etc.).

A delay is selected for the request depending on a map inactive or active state. If the cache is present, the request for memory transfer comes from the cache.

4.3.7 Memory Protection and Access Control

The two access control bits, PRDOn-(9,10), of the RAM are latched under control of the cache memory address latch control signal CMAL-. The buffered bits, PRDBn+(9,10), are then used by the memory protection logic to define any access control errors.

The memory protection enable signal PMPEN+ is enabled by EXC2 0646. It is disabled whenever an error is detected, by EXC2 0746, or by the map inactive state.

4.3.7.1 Instruction Error Detection, Primary Errors

Execution of any HALT instruction, or an I/O instruction from selected key not 0 (user key) is detected at full clock of the primary decoding microinstruction when CICIDE+ is true. A principle of the pipeline structure of the machine is that the next instruction fetch is also started at the beginning of the decoding microinstruction; so generally this error is strobed at the end of the first 165 to 180 nanoseconds of a memory request.

Whenever the memory fetch for the effective jump address occurs, the micro signal DJUMP+ is true. At the end of this micro-instruction the access control is tested for read-operand only status and, if true, a jump error is strobed.

The instruction error address register, PIADn+(0-15), is updated every primary decoding time with the current logical address. Because of the pipeline structured microcoding, this is P+1 of the logical address for the instruction causing the error.

If any of the above three errors occurs, they inhibit detection of a secondary set of errors.

4.3.7.2 Secondary Error Detection

The following access control errors are strobed on the trailing edge of the processor request.

Unassigned error. The unassigned address error register has the logical address causing the error, and the instruction address register has logical P+1 of the instruction causing the error.

Write protection error. The write operation is changed to a read, and the instruction address register, PIADn+(0-15), has the logical address of the instruction which caused a write at a read only/read operand only address.

Instruction fetch error. The instruction address register has the logical address of the first instruction fetch in a read operand only area. This error occurs when program execution overflows into a read operand only space, as contrasted to a jump error which does the same thing by way of a jump.

I/O transfer errors. If an I/O transfer attempts to write in a read only location, or if it attempts to access an unassigned area, the error is detected. The active buffer interlace controller or PMA is signaled to terminate by a pulse on BIMES-I or BTMES-I, respectively. Since I/O transfers are controlled by the operating system, these errors should never occur, and are mainly an aid to operating system debugging.

4.3.7.3 Special Control for Register-to-Register Function

When a register-to-register operation with multiple destination occurs, a dummy read memory cycle to an address related to register data will occur. This cycle is given full access status by signal PRGXFD+, so that an access mode protection error cannot occur.

4.3.7.4 Memory Protection Interrupt Control

When an error is detected the protection error interrupt request, BINTE+, is set. This activates OINT-, which causes the processor to wait for interrupt service at its next primary decoding time. This ensures that the processor will not execute past the point of the memory protection.

4.3.7.5 Memory Protection Priority

The memory protection priority is the highest in the system. The signal BINTE- provides priority into the power fail interrupt, which is second in priority. After power fail, priority is configured using PRnX-I lines.

4.3.7.6 Memory Protection Interrupt Address

The memory protection interrupt address circuits are on page 6 of the logic diagram. The different types of interrupts are encoded to different interrupts according to the description in section 3.6.

4.3.8 Operational Mode Control

Various EXC commands arm the map logic to change modes on the effective address of the next jump instruction. The mode changes implemented in this manner are:

a. Inactive to active executive

b. Active executive to inactive

c. Active executive to user mode

When one of these transitions is armed, signal PMODSW+ is true, which causes PMSWIP+ to go true on the trailing edge of the instruction fetch request following the EXC. This event causes PMRQOI+ to be set which inhibits the map request input to cache and the map delay line. As soon as the next request occurs the inhibit starts to count down for the next two half clock times. If DJUMP is true during the first full clock period of the request, the mode transition will occur at the full clock, causing a key change to the mapping input. On the following half clock PMRQOI is clocked out, and a mapping access begins.

Additional mode switching occurs under the following conditions:

a. Executive mode state not 0. In this condition, the inhibit is active on each processor memory cycle. Since a key change could occur at full clock time following the start of a memory cycle (read overrides write during indirection) the delay of inhibit to the second half clock of the cycle is required.

b. User to executive mode on interrupt. In this condition, the logic must ensure that the interrupt vector is mapped in key 0. The executive mode mask PEMSMK+ is activated on FRYX of the interrupt sequence to assure executive mode state 0 operation at the interrupt service. The same logic sets a flip-flop, PUSERB, which clears user mode and sets executive mode at the end of the current memory cycle. This flip-flop is cleared on the leading edge of the next processor memory request. In this situation the key change is well ahead of the request, and the inhibit delay PMRQOI+ is not used.

4.3.9 DMA Transfer Control

Transfer of array data over high speed DMA is set up and initialized using programmed I/O functions as explained in section 3.4. DMA transfers are mapped in key 0 when the map is active.

4.3.9.1 DMA Priority Control

Since the map is a fully buffered device, it should have the lowest priority required to not interfere with synchronous device transfers. The map is designed to be the lowest priority on the high-speed DMA priority chain, and does not provide for a high-speed priority chain output.

In order to subordinate the map DMA transfer to a low-speed DMA transfer, the line PPRMX- can be jumpered to a system priority level PRnX-I. No system priority out is required for this function, since high-speed versus low-speed DMA service is determined on the option board.

4.3.9.2 DMA Tranfer Out to the Map Array

DMA output is active if the EXC function to start DMA (PSTDMA+) is set. The request PDMARQ+ is set on IUCF-I, causing a synchronized activation of TPOF-I. Upon receiving FRYF trailing edge, the data phase flip-flop, PDTPF+, is set. When this function is set, the DMA address register is incremented for the next transfer by signal PIMAE-. This signal also enables the address selection for the I/O bus.

At the end of the memory fetch, when MRS2A- returns high, the inhibit request function PIHMRQ is set. This ensures that the next request will be inhibited at the map and cache until the data just accessed and placed on the E-bus is written into the map array.

As soon as PIHMRQ is set true it forces its clock low again, until the data phase flip-flop PDTPF is cleared on the trailing edge of DRYF. At that time, PIHMRQ is cleared and map key selection begins for the next cycle. One full clock later PIHRQD- goes true and the next mapping cycle begins.

On the full clock following setting of PIHMRQ+ the write strobe PRMWEN+ is set. It is cleared when PIHMRQ+ returns false. The strobe PRAMW- is gated by the DRYF for proper width.

4.3.9.3 DMA Transfer In to Memory from the Array

This operation is different from the output transfer in that data from the array is buffered in the DMA transfer control so that the array can be used to map the actual transfer.

When start DMA is set PDMAIN+ and PBUFF- are true. As soon as as memory cycle is completed, PIHMRQ+ is set. The next full clock causes PBUFF+ to set, which enables transfer request PDMARQ+ to set on the next IUCF-I clock.

As soon as PIHMRQ+ is set, the array address multiplexor selects the array address counter as the address source. One full clock later this data is loaded into the input buffer. On the following half clock PIHMRQ+ is cleared, and the array is released for mapping purposes and cache/map request are re-enabled.

When a data transfer service occurs the data phase function PDTPF+ sets on the trailing edge of FRYF-I. When PDTPF+ is cleared on the trailing edge of DRYF-I, PBUFF+ is clocked off, and the sequence is ready to repeat for the next cycle.

4.3.9.4 Termination of DMA Transfer

Each time PIHMRQ- is cleared, the array address pointer, PMARn+0-9, is incremented for the next transfer. The logical memory address register, PDMAn+(0-15), is incremented on the trailing edge of FRYF (via PIMAE-) for the next transfer.

The length counter is decremented on the trailing edge of DRYF which is gated by PDTPF+. When a zero count is achieved, PWCZ- activates the DMA interrupt request PIURF- on the next IUCX clock. The interrupt signal clears MDA start and terminates DMA transfer.

When the sense DMA completion is used rather than the DMA completion interrupt, it is necessary to use the reset DMA command to complete the DMA transfer operation. The decoded function PRDMEX- clears both PIURF- and PSTDMA+.

4.3.10 I/O Status and Control Section

4.3.10.1 I/O-Bus Drivers and Receivers

The I/O-bus drivers transfer either a 16-bit address/data word EBnn-I(0-15) or a 4-bit interrupt address EBnn-I(1-4) onto the bidirectional I/O bus.

During an input-data transfer, a high PEBEN+ transfers a 16-bit data word through the drivers onto the I/O bus. When an interrupt address is being generated, a low PEBEN+ disables the sixteen drivers causing all of their outputs to go high (all zeros). This allows the four interrupt I/O-bus drivers to transfer the interrupt address onto the I/O bus.

The I/O-bus receivers convert I/O-bus data into PEBn(0-15) for use in various circuits of the memory map.

4.3.10.2 Address Detection and Function Control

Address signal PADR46+ goes high when address 046 (or alternate address 056) is decoded from bits PEBn(0-5) and there are no DMA or interrupt requests (IUAX-I high). An external control (EXC2) instruction is decoded when PEB15+ is high and PADR46+ is gated with the function ready control FRYX-I (PFRY46+ is high). As illustrated in table 4-1, specific EXC2 instructions are executed by decoding the function code bits PEBn+(6,7,8). The decoded outputs correspond to the various EXC2 instructions and are described as follows:

a. PINAEX- arms mode switching from the executive mode to the inactive mode (EXC2 046).

b. PACTEX- arms mode switching from inactive mode to executive mode (EXC2 0146).

c. PUSREX- arms mode switching from executive mode to user mode (EXC2 0246).

d. PSDMEX- starts a memory-map DMA transfer (EXC2 0346).

e. PRDMEX- resets the memory map's DMA-transfer logic (EXC2 0446).

f. PCLMEX- removes the executive-mode mask (EXC2 0546).

g. PEMPEX- enables the memory protection function and instruction address updating (EXC2 0646).

h. PDMPEX- disables the memory protection function and instruction address updating (EXC2 0746).

Function code bits PEBn+(6,7,8) are also decoded for sense (SEN) instructions (PEB12+ high). Table 4-2 lists the function codes for the SEN instructions. If the condition sensed by the instruction is true, a sense response (SERX-I low) is sent to the processor.

4.3.10.3 Programmed I/O Transfer

Execution of input- and output-data transfer instructions consists of a device-address phase and a data phase. A high PEB13+ indicates an input-data transfer and high PEB14+ indicates an output-data transfer. When gated with a high PERY46+, these signals start the device-address phase by setting the input- or output-transfer flip-flop (PDTIX+ or PDTOX+ high). The data phase is initiated when a low data-ready signal DRYX- resets the input- or output-transfer flip-flop. Control signals for the four formats of output-data transfers are decoded from PEB14+ and PEB15+ (table 4-3). The control signals are:

a. PCSTB-, encoded command strobe to cache

b. PWRKC-, write key control

c. PWIOC-, write I/O control

d. PXFRW-, write number of words to be transferred via DMA

Table 4-1. EXC2 Decoder Truth Table

INPUTS			OUTPUTS							
PEB08+	PEB07+	PEB06+	PINAEX-	PACTEX-	PUSREX-	PSDMEX-	PRDMEX-	PCLMEX-	PEMPEX-	PDMPEX-
L	L	L	L							
L	L	H		L						
L	H	L			L					
L	H	H				L				
H	L	L					L			
H	L	H						L		
H	H	L							L	
H	H	H								L

Notes:

1. L = low, H = high
2. For clarity, only the low (or active) states of the outputs are included in the table.

Table 4-2. Function Codes for SEN Instructions

PEB08+	PEB07+	PEB06+	Instruction
L	L	L	SEN 046 (SEN0+ high)
L	L	H	SEN 0147 (SEN1+ high)

Table 4-3. Output-Transfer Format Truth Table

Inputs		Outputs			
PEB15+	PEB14+	PCSTB-	PWRKC-	PWIOC-	PXFRW-
L	L	L	H	H	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	L

Note: L = low, H = high

4.3.10.4 Key and 64K-Mode Registers

On the positive-going transition of the write-key control PWRKC+, PEBn+(0-3) and PEB04+ are clocked into the key (internal status) and 64K-mode registers, respectively. The 4-bit output of the key register PPRKYn+(0-3) is sent to the key multiplexor and to the I/O-bus data multiplexor as part of the status-signal input. The output bit of the 64K-mode register P64KEN+ is also sent to the I/O-bus data multiplexor as part of the status-signal input. A high P64KEN+ enables the 64K mode of operation. When P64KEN+ is low, the 32K mode is used.

4.3.10.5 Executive-State Register

This register, PEMSnE+(0-3), stores one of the four states of the executive mode. On positive-going transitions of the write-key control PWRKC+, PEBn+(5-8) are clocked into the executive-state buffer. This buffer is cleared with a low system reset PSYRTA-. Buffer-output bits PEMSnE+(1-3) are applied to the I/O-bus data multiplexor as well as the executive-state output gates in the operational mode control. When the executive-state masking flip-flop is reset, a high PEMSMK- transfers the buffer-output bits through the output gates to the key multiplexor. Resetting of the flip-flop occurs during either the inactive mode of operation (PACTV+ low) or the decoding of an external control (EXC2 0546) I/O instruction.

When an interrupt occurs, the executive-state masking flip-flop is set (PEMSMK- low) causing all bits of PEXMSn+(1-3) to go low. This results in executive-mode state 0 operation (executive map).

4.3.10.6 Input-Data Selection Register

On the positive-going transition of the I/O-write control PWIOC+, I/O data bits PEBn+(10,11) are clocked into the input-data selection register. The register contents PSIn+(0,1) are used to select one of three data inputs for the I/O-bus data multiplexor. Bit configurations for data-input selection are listed in the following table (L is low, H is high):

PSI1+	PSI0+	Selected Input Data
L	L	Status signals
L	H	Instruction address
H	L	Unassigned address

4.3.10.7 I/O Bus Data Multiplexor

This multiplexor selects I/O-bus data from one of the following sources:

a. RAM array input register: PDIBn+(0-12)

b. Instruction address register: PIADn+(0-15)

c. Unassigned address register: PUADn+(0-15)

d. Status signals: PPRKYn+(0-3), P64KEN+, PEMSnE+(0-3), PDMAOE+, PDMAER+, PIOUER+, PIOEKn+(0-3)

e. DMA memory address register: PDMAn+(0-15)

The I/O-bus data multiplexor consists of two multiplexors. Under control of selector signals PSIn+(0,1), the first multiplexor selects data from either the instruction-address register, unassigned address register, or internal-status register. Under control of selector signals PIMAE- and PDTIX+, the second multiplexor selects data from either the DMA data input buffer, first multiplexor, or DMA memory-address register. Output data PEBDn+(0-15) is applied to the I/O bus drivers.

4.4 MEGAMAP TIMING

This section provides timing waveforms for the various memory-map operations. The operations with their figure numbers are listed below:

Figure 4-4, Programmed I/O Data Transfer

Figure 4-5, Megamap Loading via High-Speed DMA

Figure 4-6, Megamap Read-Back via High-Speed DMA

Figure 4-7, Megamap Loading/Read-Back Termination

Figure 4-8, Memory Mapping

Figure 4-9, I/O and Halt Error Detection

Figure 4-10, Jump-Error Detection

Figure 4-11, Unassigned and Writing Error Detection

Figure 4-12, Instruction-Fetch Error Detection

Figure 4-13, I/O Data-Transfer Error Detection

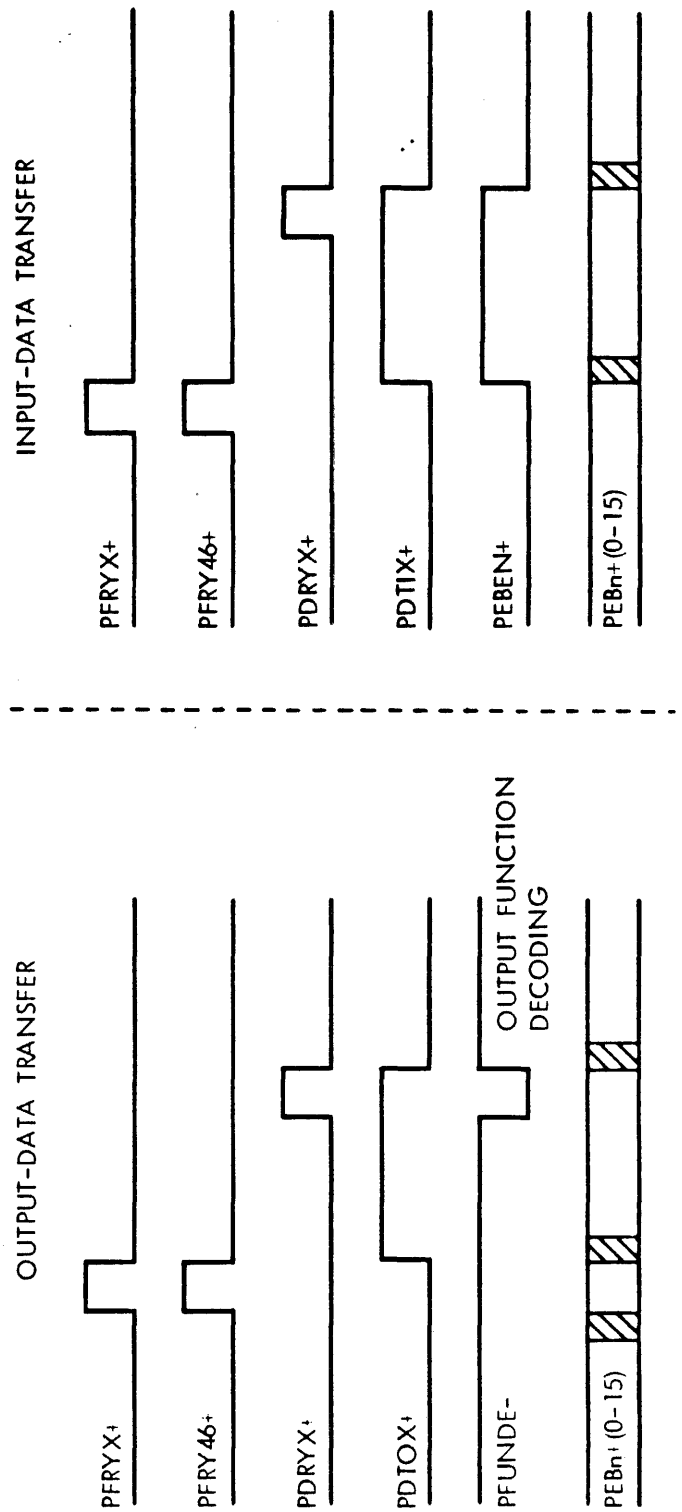
Figure 4-14, Memory Protection Interrupt

Figure 4-15, Executive-Mode to Inactive-Mode Switching

Figure 4-16, Inactive-Mode to Executive-Mode Switching

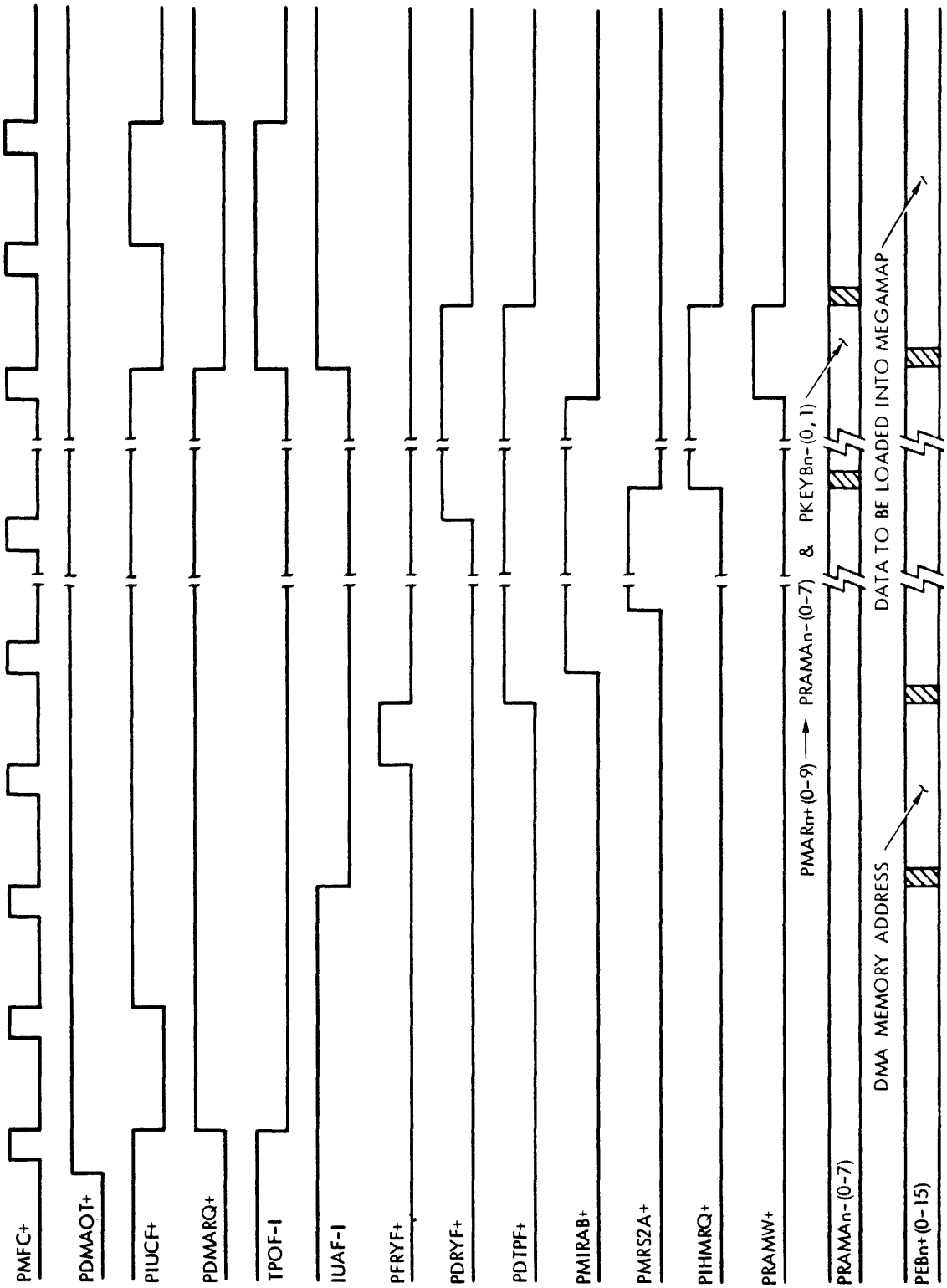
Figure 4-17, Executive-Mode to User-Mode Switching

Figure 4-18, User-Mode to Executive-Mode Switching



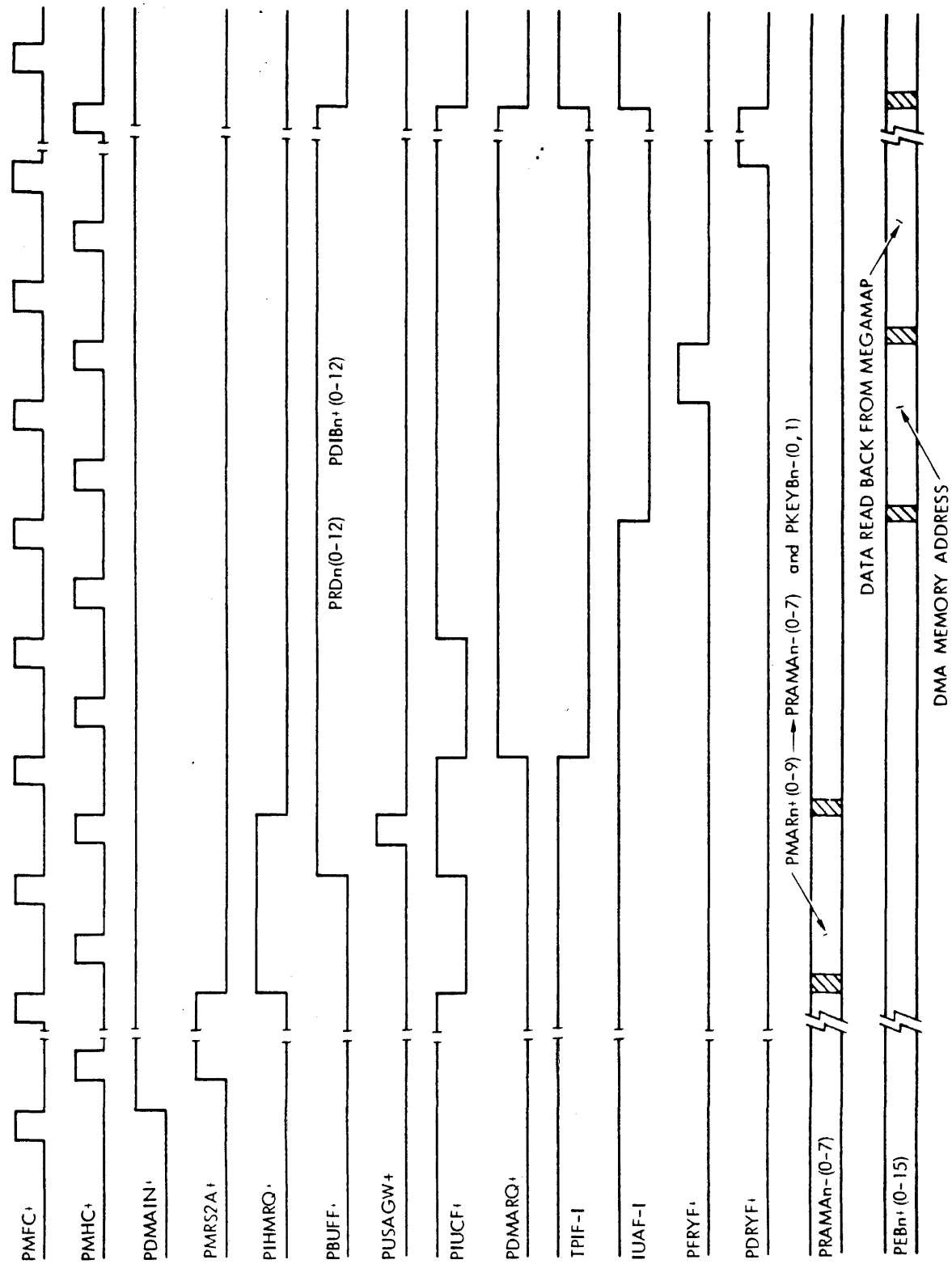
VTI1-2061

Figure 4-4. Programmed I/O Data Transfer



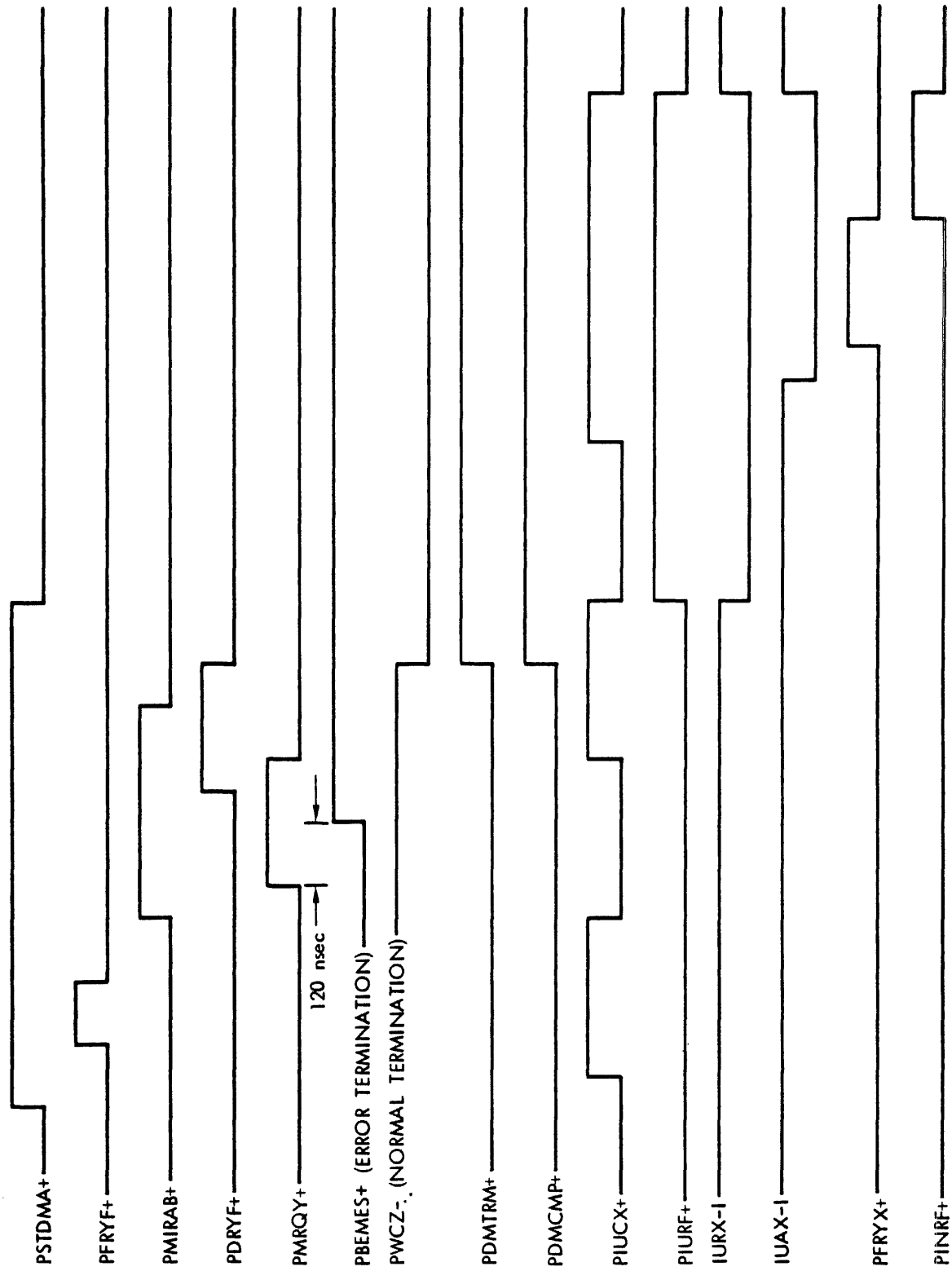
VTI1-2062

Figure 4-5. Megamap Loading via High-Speed DMA



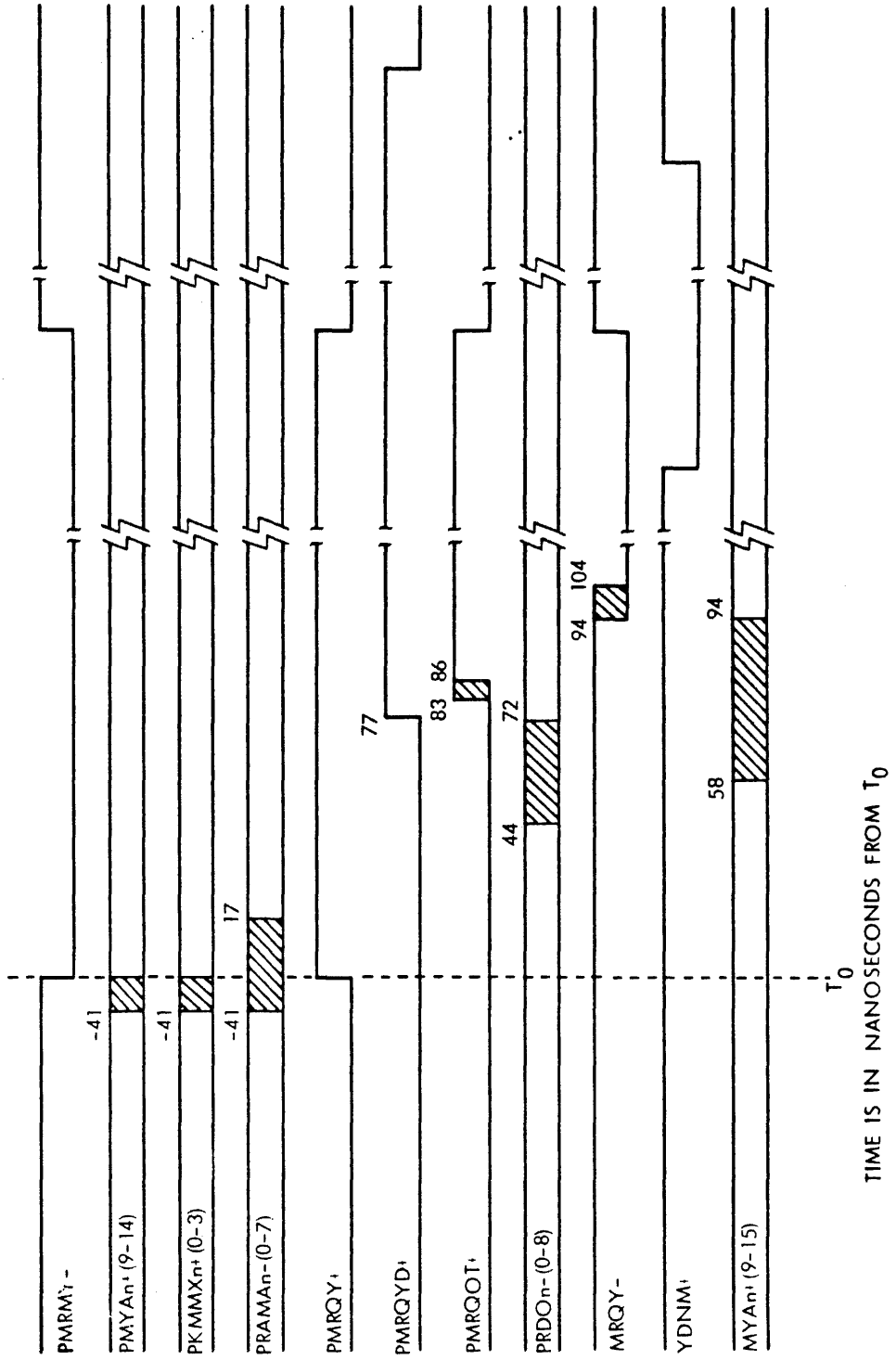
VTI1-3498

Figure 4-6. Megamap Read-Back via High-Speed DMA



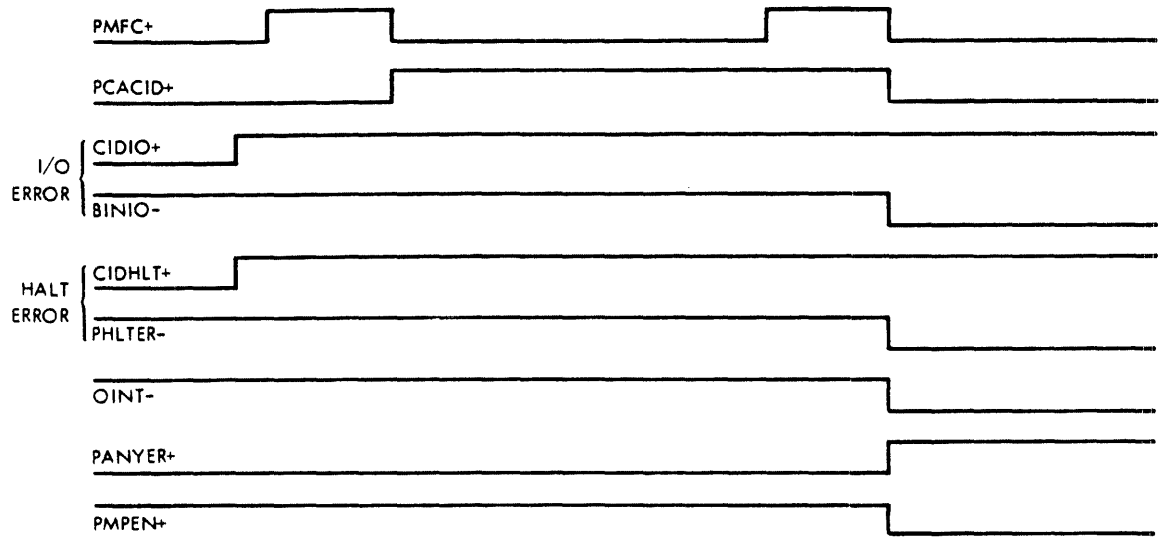
VTI1-2064

Figure 4-7. Megamap Loading/Read-Back Termination



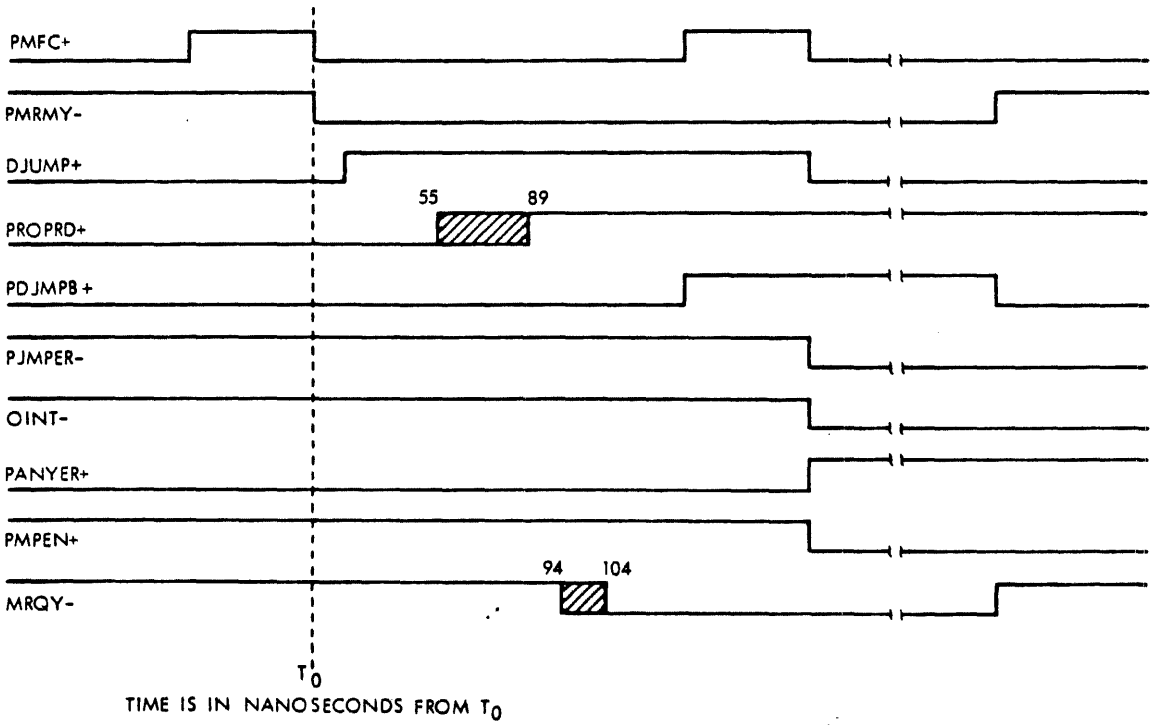
VTI1-2065

Figure 4-8. Memory Mapping



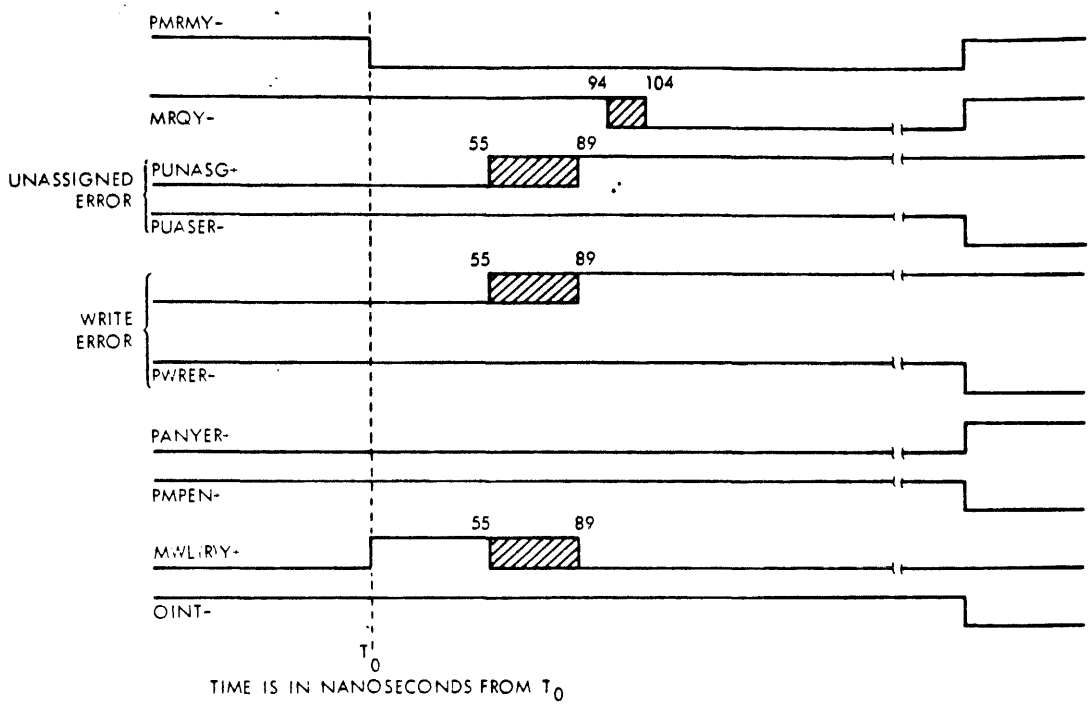
VTI1-2066

Figure 4-9. I/O and Halt Error Detection



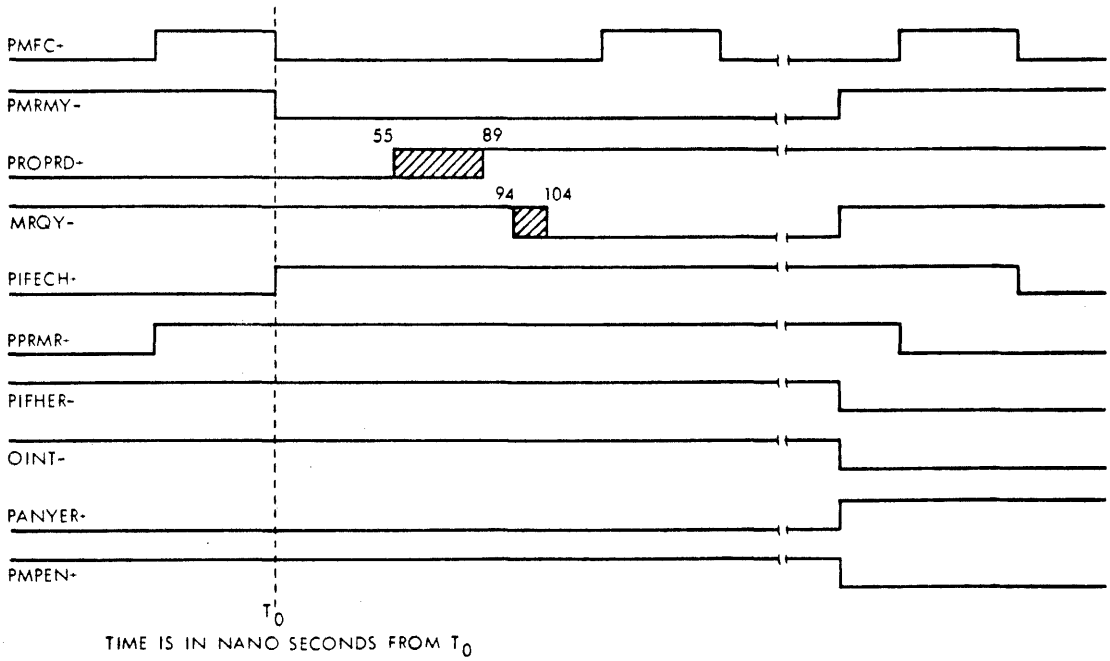
VTI1-2067

Figure 4-10. Jump-Error Detection



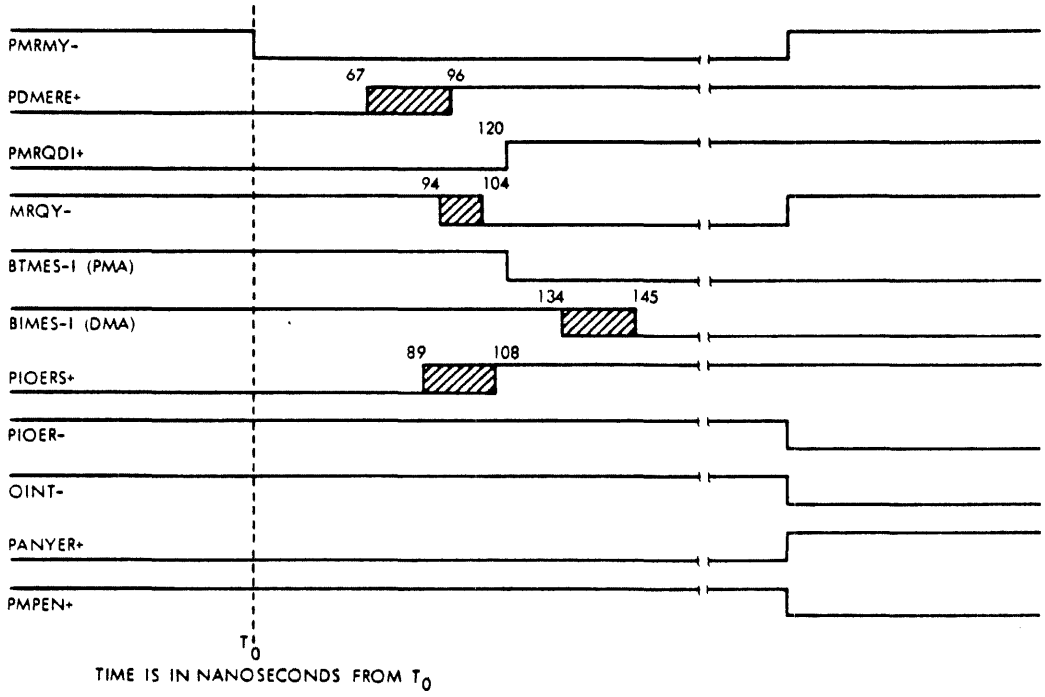
VTI1-2068

Figure 4-11. Unassigned and Writing Error Detection



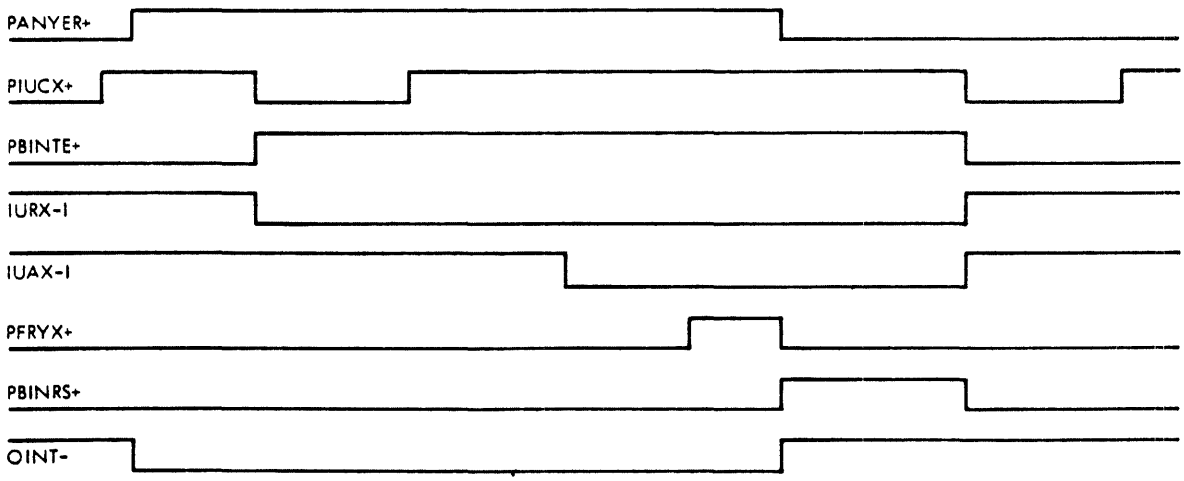
VTI1-2069

Figure 4-12. Instruction-Fetch Error Detection



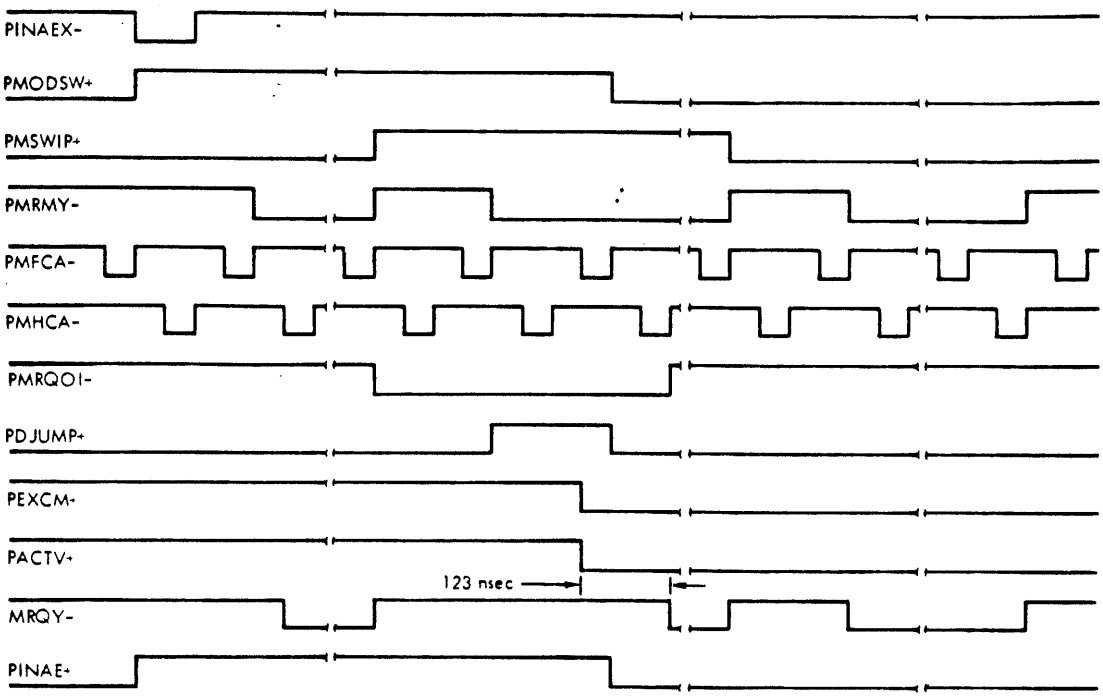
VTI1-2070

Figure 4-13. I/O Data-Transfer Error Detection



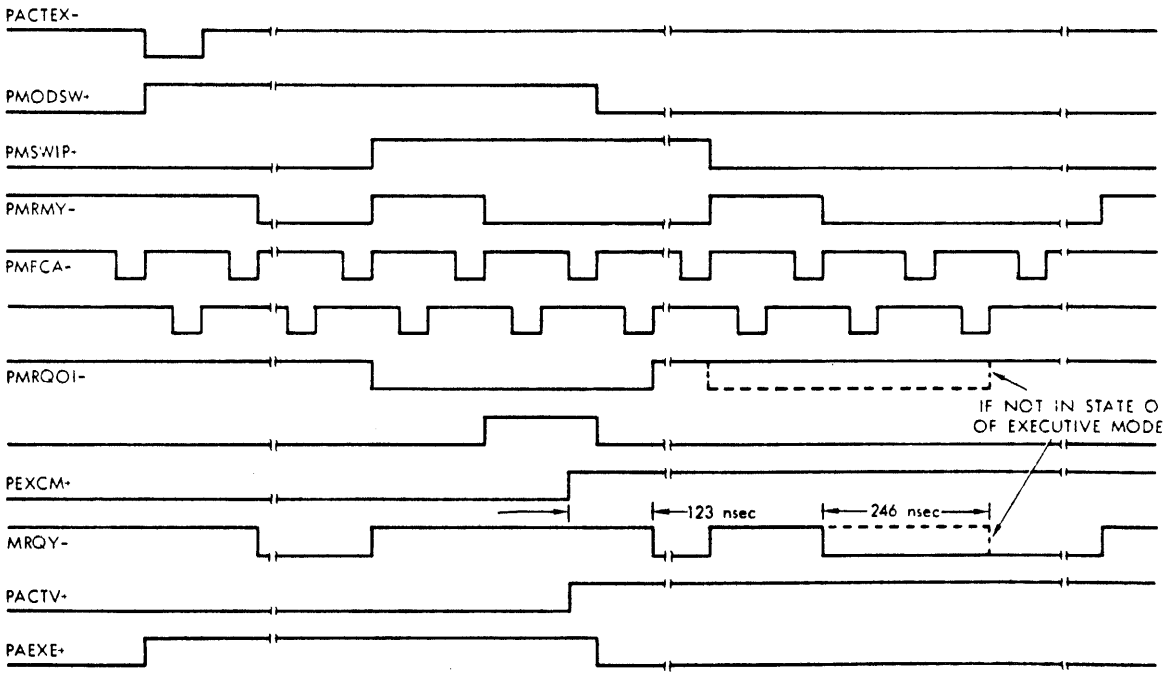
VTI1-2071

Figure 4-14. Memory Protection Interrupt



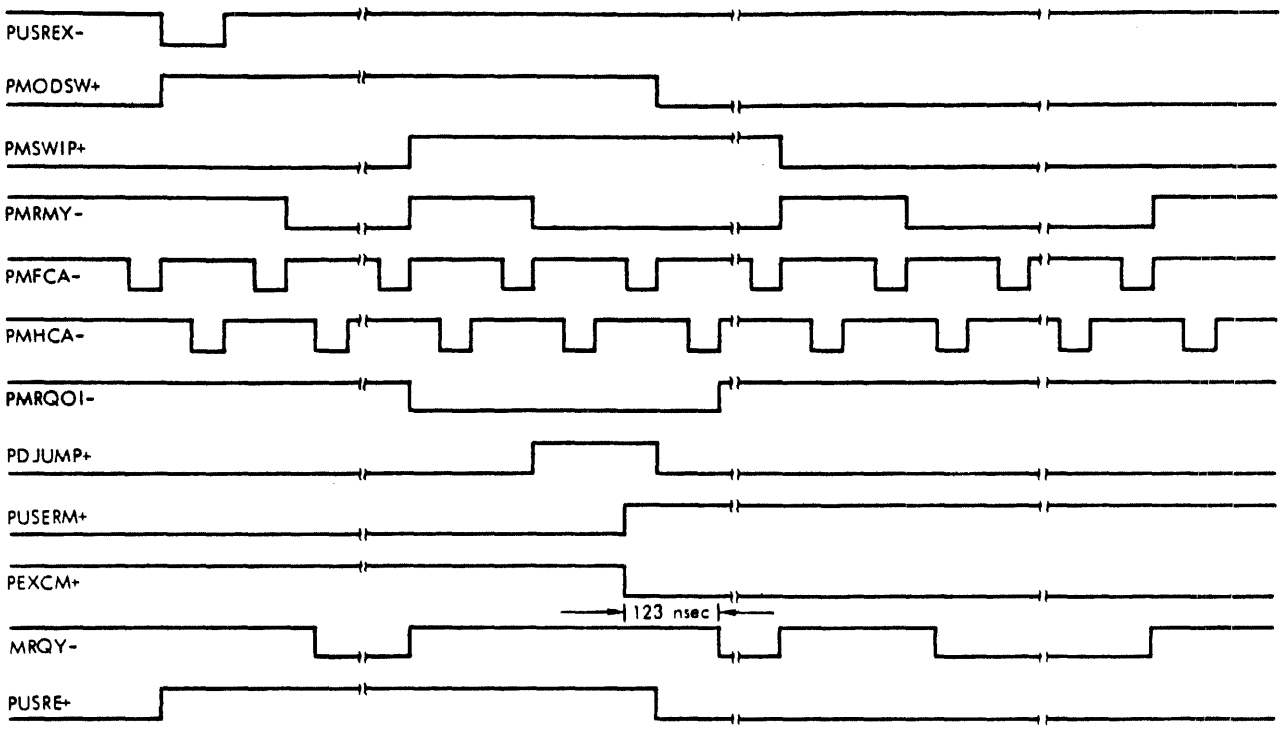
VTI1-2072

Figure 4-15. Executive-Mode to Inactive-Mode Switching



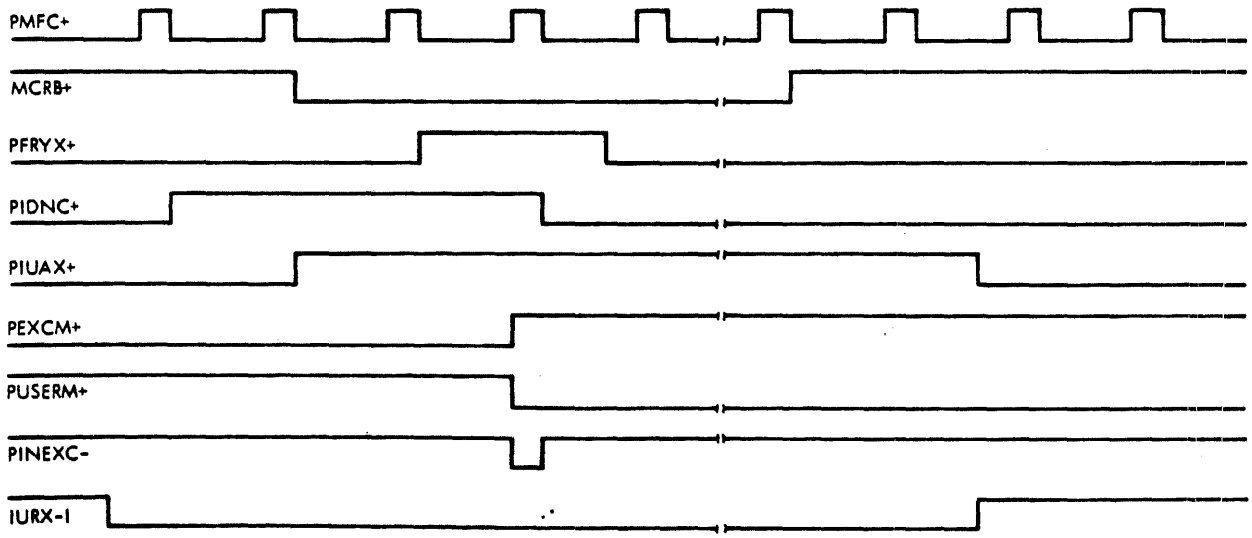
VTI1-2073

Figure 4-16. Inactive-Mode to Executive-Mode Switching



VTI1-2074

Figure 4-17. Executive-Mode to User-Mode Switching



VTI1-2075

Figure 4-18. User-Mode to Executive-Mode Switching

SECTION 5
MAINTENANCE

Maintenance personnel should be familiar with the contents of this manual before attempting megamap troubleshooting. A test program is available to verify correct operation and to isolate malfunctions to a particular section of the megamap. Further diagnosis can then be made by referring to this manual.

5.1 TEST EQUIPMENT

The following test equipment and tools are recommended for megamap maintenance:

a. Oscilloscope, Tektronix type 547 with dual-trace plug-in unit or equivalent.

b. Multimeter, Triplett type 630 or equivalent.

c. Soldering iron, 15-watt pencil type.

5.2 CIRCUIT BOARD REPAIR

The megamap board is a two-layer PC board. The ICs contained on the board consist of LSI memories; MSI multiplexors, decoders, and registers; and SSI gates and flip-flops.

If it has been determined that circuit board repair is required, it is recommended that the Sperry Univac customer service department be contacted so that a new circuit board can be installed in the user's system and the faulty one returned to the factory for repairs. However, if the user decides to perform his own repairs, extreme caution should be used so that the circuit board is not permanently damaged. Approved repair procedures should be followed such as the ones described in document IPC-R-700A prepared by the Institute of Printed Circuits.

5.3 CIRCUIT-COMPONENT IDENTIFICATION

For IC components, the megamap board has location coordinates that are used in the logic diagrams as reference designations. For example, a flip-flop designated C8 in the megamap logic diagram is in the IC packaged at location row C column 8 on the megamap board. For discrete components, the reference designations used in the logic diagrams appear on the circuit board adjacent to each component.

Parts lists in the system documentation package provide a cross reference between Sperry Univac and the manufacturers part numbers.

SECTION 6
MNEMONICS

This section presents an alphabetized list of megamap signal mnemonics with definitions.

Plus or minus signs are included at the end of each mnemonic. The plus sign indicates the signal is at a high logical level when its function is being performed. The minus sign indicates the signal is at a low logical level when its function is being performed. A signal that is the logical inversion of another uses the same mnemonic with an opposite sign; these signals are complements of each other.

I/O bus signal mnemonics end with-I.

Mnemonic	Description
AREAD-	Read/write signal from the PMA option. A low level indicates a PMA reading operation.
BIMES-I	Stops a DMA transfer due to an error during a memory-mapping operation.
BINIO-	Indicates an I/O instruction error has occurred.
BINTE-	Memory-protection interrupt priority.
BTMES-I	Stops a PMA transfer due to an error during a memory-mapping operation.
CACHE-	Configuration signal from the cache board to define the presence of cache.
CACIDE+	Used by the processor to transfer instruction-decoder contents onto the control-store address bus.
CIDHLT+	Indicates that the processor has decoded a halt instruction.
CIDIO+	Indicates that the processor has decoded an I/O instruction.
CIDJMK+	Indicates that the processor has decoded a jump-and-mark instruction.

Mnemonic	Description
CMAL+	Cache memory-address latch control.
CMRQ-	Cache memory request
DJUMP+	Indicates that the program has been directed to the effective jump address of a jump instruction.
DRYF-I	Data ready for high-speed DMA operation.
DRYX-I	Data ready for normal DMA operation.
EBnn-I(0-15)	I/O-bus data.
FRYF-I	Function ready for high-speed DMA operation.
FRYX-I	Function ready for normal DMA operation.
IDNC-	I/O done signal from option board.
IOKn-I(1-4)	I/O key bits from BIC.
IUAF-I	Interrupt acknowledgment for high-speed DMA operation.
IUAX-I	Interrupt acknowledgment for normal DMA operation.
IUCF-I	Interrupt clock for high-speed DMA operations.
IUCX-I	Interrupt clock for normal DMA operation.
IURX-I	I/O-bus interrupt request.
IWLMC-	I/O-write left byte.
IWRMC-	I/O-write right byte.
MAKO+	From processor, indicating the PMA memory request has been acknowledged.
MFC-	Processor full clock.
MHC-	Processor half clock.
MIMCn+(0,1)	Contains bits 0 and 1 of the IM field to specify a reading or writing operation.
MIRAB+	I/O memory request.

Mnemonic	Description
MRMYB-	Megamap memory request of port B.
MRQYx-(A,B)	Mainframe memory request, port A,B.
MRQYnnn-	Fifteen 64K-bank selection requests where nnn is 065, 128, 193, 256, 321, 386, 446, 512, 577, 642, 708, 773, 838, 904, or 968.
MRS2A-	Memory sequencing flip-flop in processor.
MWLYx+(A,B)	Mainframe-memory write, left byte, ports A and B.
MWRYx+(A,B)	Mainframe-memory write, right byte, ports A and B.
MYAAn+(0-15)	Mainframe memory address bits, port A
MYABn+(0-15)	Mainframe memory address bits, port B.
MYKBn+(16-19)	PMA key bits, port B.
MYMBn+(9-15)	Megamap memory address bits, port B.
OINT-	Memory protection internal interrupt.
P64KEN+	Enables the 64K mode of operation.
PACTEX-	Results from the decoding of instruction EXC2 0146.
PACTV+	Indicates that the megamap is active.
PADR46+	Indicates that device address 46 is decoded.
PADSEL+	Device address selector.
PANYER+	Indicates that the megamap has detected an error.
PBINTE+	Interrupt priority output.
PBEMES+	Enabling signal to stop a DMA transfer due to an error.
PBICKn+(0-3)	BIC key bits.
PBINIO+	Megamap I/O-instruction error flag.

Mnemonic	Description
PBINRS+	Megamap interrupt response flag.
PBINTA+	Enables the interrupt address.
PBUFE-	Enables buffer data PDIBN+(0-12) to be transferred onto the I/O bus.
PBUFF+	Buffer-full flag.
PCACID+	Primary instruction decode signal.
PCLMEX-	Removes the executive-mode mask.
PCSTB-	Encoded command strobe to cache.
PCCOMn+(0,1)	Encoded cache command.
PCHINH+	Inhibits the start of cache service on memory request.
PDIBn+(0-12)	Output of DMA array buffer.
PDJMPB+	Buffered effective jump address signal.
PDMAn+(0-15)	Outputs of DMA memory-address counter.
PDMAER+	DMA error flag.
PDMAIN+	Indicates that a read-back operation is in progress.
PDMAOE+	Enabling signal for megamap loading operation.
PDMAOT+	Indicates that a megamap loading operation is in progress.
PDMARQ+	Megamap loading or read-back DMA request.
PDMCMP+	Indicates that a megamap loading or read-back operation has been completed.
PDMERE+	Enabling signal for an error stop.
PDMIAE+	Enables an interrupt address at the completion of a megamap loading or read-back operation.

Mnemonic	Description
PDMIEN+	Enables an interrupt at the completion of a megamap loading or read-back operation.
PDMIUR-	Interrupt request at the completion of a megamap loading or read-back operation.
PDMODP+	Indicates the data-phase of a megamap loading operation.
PDMPEX-	Disables the memory protection function of the megamap.
PDMRCn-(1-3)	Internal (ripple) clock for the DMA memory address counter.
PDMRQP+	Indicates that a request for a megamap loading or read-back operation has received I/O priority.
PDMTRM+	Terminates a megamap loading or read-back operation due to an error.
PDTIX+	Indicates the data phase of an input data transfer.
PDTOX+	Indicates the data phase of an output data transfer.
PDTPF+	Indicates the data phase of a megamap loading or read-back operation.
PDTPFE+	Enabling signal for the data phase of the megamap loading or read-back operation.
PDTXn+(0-15)	Output of the first multiplexor of the I/O-bus data multiplexor.
PDWIOC+	Delayed write I/O control.
PEBn+(0-15)	Received I/O bus data.
PEBDn+(0-15)	Output of the I/O bus data multiplexor.
PEBEN+	Enabling signal for I/O bus drivers.
PEMPEX-	Results from the decoding of instruction EXC2 0646.

Mnemonic	Description
PEMSnE+(1-3)	Enabling signals for the executive-mode states.
PEMSMK-	Executive-mode mask.
PERRR-	Reset for an error condition.
PEXCM+	Executive mode.
PEXDEN-	Enables the decoding of an EXC2 instruction.
PEXMPB+	Buffered signal resulting from the decoding of the EXC2 0646 instruction.
PEXMSn+(1-3)	Executive-mode state bits.
PEXMS13+	Indicates that the executive-mode states 1 through 3 are active.
PFRY46+	Decoded address 46 for function ready.
PFRYAR+	Indicates that a function ready condition has occurred when IUAX-I is true.
PFULAC+	Full-access mode.
PFUNDE-	Enabling signal for output function decoding.
PHLTER-	Halt-instruction error flag.
PIADn+(0-15)	Output of instruction address register.
PIFECH+	Instruction fetch.
PIFERE+	Instruction-fetch error enabler.
PIFHER+	Instruction fetch error.
PIFJMK-	Jump-and-mark instruction fetch.
PIHMQD+	Delays the release of PIHMRQ+.
PIHMRQ+	Inhibits memory requests.
PIMAE-	Memory address enabler for loading and read-back operation.
PINAn+(1-3)	Interrupt-address data.

Mnemonic	Description
PINADM+	Interrupt address strobe.
PINAE+	Inactive-mode enabler.
PINAEX-	Results from the decoding of instruction EXC2 046.
PINEXC-	Indicates the megamap has entered the executive mode by an interrupt.
PINRF+	Interrupt response flag indicating the loading/ read-back operation is complete.
PINRXE+	Interrupt enabler.
PIOEKn+(0-3)	I/O-error key bits.
PIOER+	I/O data-transfer error.
PIOERE+	I/O-instruction error set enabler.
PIOUER+	I/O unassigned error.
PIOWR-	I/O memory write request.
PIURF+	Interrupt request for the completion of loading/read-back operation.
PIWLRM+	I/O writing operation.
PJMPER-	Jump error.
PKB1EN-	Enabling signal for key bit 1.
PKBEME+	Clock for PBEMES+.
PKBICK+	Clock for BIC key bits.
PKBUFF-	Clock for PBUFF.
PKDTIX-	Clock for PDTIX+.
PKDTOX-	Clock for PDTOX+.
PKDTPF-	Clock for PDTPF+.
PKEYBn-(0,1)	Key bits.
PKIHMR-	Clock for PIHMRQ+.

Mnemonic	Description
PKLPMA+	Clock for PLPMAK+.
PKMMXn+(0-3)	Output of key multiplexor.
PKWC-	Clock for word-transfer counter.
PKWIOC-	Clock for PDIOC+.
PKYMXE-	Enabling signal in key multiplexor.
PKYMXn+(0-3)	Processor or PMA key bits.
PKYNZ+	Key is not equal to zero.
PLDBF-	Loading signal for the buffer in I/O-bus data multiplexor.
PLDIA+	Loading signal for the instruction address register.
PLPMAK+	Loads PMA key bits.
PMAKIR+	PMA or I/O memory cycle.
PMAKYn-(0-3)	PMA key bits.
PMARn+(0-9)	Output of map-address counter.
PMARCn-(1,2)	Internal clock for map-address register.
PMFC	Buffered full clock
PMFCMP+	Clock for error testing of halt, jump, and I/O instructions.
PMHC	Buffered half clock
PMIRAB+	Current memory cycle is DMA.
PMIRBF+	Buffered MIRAB+.
PMODSW+	Megamap mode switching.
PMPEN+	Enabling signal for the memory protection function.
PMRMY-	Buffered memory request for port B.

Mnemonic	Description
PMRQOI-	Memory request inhibit for mode switch.
PMRQPA+	Clock for testing unassigned address, instruction fetch, and writing and I/O data-transfer errors.
PMRQY-	Megamap delayed request (internal signal).
PMRS2A+	Processor memory control store MRS2A.
PMSWIP+	Indicates the megamap is in the process of switching from one operating mode to another.
PMYAn+(0-8)	Physical-address latch output for port A.
PMYAn+(9-19)	Physical page address to cache for hit/miss comparison.
POINTE+	Enabling signal for memory-protection internal interrupt.
PPMAWR-	PMA writing request.
PPRnF+(1-4)	High-speed DMA priority lines.
PPRKYn+(0-3)	Output bits from the megamap's key register.
PPRMF+	Priority input signal for high-speed DMA.
PPRMR+	Indicates processor is requesting memory.
PPRMX+	System interrupt priority input.
PPRMXB+	Buffered PPRMX+.
PPRNX-	System interrupt priority output.
PPROWR-	Processor writing request.
PRnX-I(1-9)	I/O-bus priority lines. PR1X-I is the highest priority and PR9X-I is the lowest.
PRAMAn-(0-9)	Output bits from the RAM address multiplexor.

Mnemonic	Description
PRAMW-	When low, loads data into the RAM array.
PRDMEX-	Resets the megamap's DMA-transfer logic.
PRDOn-(0-12)	Output data from RAM array.
PRIVLG+	Enabling signal for privileged instructions.
PRMAKn+(0-3)	Input for key multiplexor from either the PMA option or the megamap's key register.
PRMWEN+	Enabling signal for PRAMW-.
PROBn+(9,10)	Buffer register output from RAM array.
PROPRD+	Indicates that only operand fetches are permitted.
PRWRn-(11,12)	Read/write control signals for bits 11 and 12 of the RAM array.
PSDMEX-	Starts a megamap DMA transfer.
PSEDMA+	Senses if the megamap is performing a DMA operation.
PSENn+(0,1)	Decoding bits for a SEN instruction.
PSENEN+	Enabling signal for SEN instruction.
PSIn+(0,1)	Selector signals for the I/O-bus data multiplexor.
PUADn+(0-15)	Output bits from unassigned address register.
PUASER+	Indicates an unassigned address error.
PUNASG+	Indicates an unassigned page.
PUSAGW+	Write strobe for usage bit.
PUSERM+	User mode.
PUSRE+	Enabling signal for user mode.
PUSREX-	Switches megamap from executive mode to user mode.

Mnemonic	Description
PWCRCn-(1,2)	Internal (ripple) clock for word-transfer counter.
PWCZ-	Output of word-transfer counter. Count equals zero.
PWIMA-	Loads the initial memory address into the DMA memory-address counter.
PWIOC-	Loads the initial map address into the map-address counter.
PWRER-	Indicates a writing error.
PWRFUA-	Writing into a full-access page.
PWRKC-	Write-key control signal. Loads data into key register, 64K-memory register, and executive-state register.
PWRT-	Writing request.
PXFRW-	Loads data into the word-transfer counter.
SERX-I	I/O-bus sense response.
SYRT-I	I/O bus system reset.
TPIF-I	High-speed trap-in request of I/O bus.
TPOF-I	High-speed trap-out request of I/O bus.
YDNMA+	Memory acknowledgment from port A of main-frame memory.
YDNMB+	Memory acknowlegment from port B of main-frame memory.

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PARTS LIST

MFG CODE	ISSUE DATE	CONTROL	CA	TYPE	COMM. CODE	ST	DOC NO	SHEET	PL REV
J W	02/05/80	W777		M		A	PL W 0101938	1	H

TITLE: MEGA MEMORY MAP OPTION

CL	U/M		AC	DOC SIZE	RANGE	THRU	ISSUE	PIC REV
A	EA		11	A				H

FIND NO	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT NO. DOCUMENT NO.	DASH	NOMENCLATURE OR DESCRIPTION	SP	CHG
Z08				W-940728	-01	PL REV H, PIC REV H, RANGE 00 - 01 EIR RELEASED 02/04/80		
Z07				NONE		PL REV G, PIC REV G, RANGE 00 - 01		
**********				**********		********** COMMON DATA **********		
1	1	EA		6600260	-00	PC ASSEMBLY-MEGA MAP (44P0785-000)	A	
2	AR	IN	W	5300333	-90	WIRE, WIRE-WRAP, SOLID WHITE 30AWG	A	
4	AR	EA	W	5300996	-18	CABLE ASSEMBLY,MAP REQUEST 18 INCHES LONG	A	
S01		X		SW01163	-00	PART IDENTIFICATION MARKING SPEC	A	
S02		X	W	9801194	-00	TEST SPEC - MEGA MAP	A	
**********			*	F2960-08	****	MEGA MEMORY MAP * VARIABLE DATA - 00 **********	**	
3	1	EA	W	5300808	-60	CABLE ASSY-DC POWER (WCS)	A	
**********			*	F3026-00	****	MEGA MEMORY MAP/DC CABLE * VARIABLE DATA - 01 **********	**	
5	1	EA	W	5300954	-48	CABLE ASSEMBLY 48 INCHES LONG	A	

DWG NO. W0101938

REVISIONS					
REV	EIR	CHG CODE	DESCRIPTIONS	DR	APPD
H	W7572-01		REVISED NOTE 6.6 ON SHEET 4, RELEASED TO API, UPDATED FORMAT, DOC. NO. WAS CIP1938.	TN	

TABULATION BLOCK		
PART NUMBER	MODEL NO.	DESCRIPTION
W0101938-00	F2960-08	MEGA-MEM MAP
W0101938-01	F3026-00	MEGA-MEM MAP/DC CABLE

NEXT ASSEMBLY		
END ITEM		
DR	S.J.	3/12/6
CHK	SALINUS	3/13/6
DSGN	T.E.H.	3/14/6
ENGR		
APPD	W.J. ZIM	3/14/6
APPD	K.D. LAMB	3/15/6

MODEL NO.
SEE TAB BLOCK

CODE IDENT NO. **21101**

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TITLE
MEGA - MEMORY MAP OPTION

SIZE	DWG NO.	REV
A	W0101938	H

printed in USA

NOTES: UNLESS OTHERWISE SPECIFIED

1.0 This drawing provides for a Mega-Memory Map Board (DM467) to be used in the S.U. . V70 series computers.

2.0 Identify per specification (SOI) .

3.0 Table 1 lists all of the discretionary wiring features of the Memory Map Board along with the standard configuration as manufactured and tested by S.U. In the Table, the column headings are defined as follows:

3.1 CONFIGURATION:

FUNCTION - The name of the feature under consideration.

LOGIC PAGE - The page of the logic(W9100569) on which the feature is located.

STANDARD CONFIG. - The standard test configuration as assembled prior to discretionary system wiring.

ALTN. CONFIG'S. - The way the feature may be wired on completion of system test. This wiring is specified by the S.U systems engineer.

4.0 Power for the map (- 00) may be provided in one of three ways as follows:

a. USE W0101280-004 (115 VAC) or
W0101280-005 (230 VAC)
power supply and cable W5300872.

b. USE W5300808 cable as second cable from a V76 main power supply (W0101896) if sufficient excess +5V logic power is available.

c. Use specially designed power supply arrangement.

4.1 Power for the map (- 01) is provided with a DC Power Cable (F/N 5) for use with the System Power Supply. (See Figure 3)

5.0 Mapping is restricted to B Port only.

6.0 Memory Expansion

6.1 The map can address up to 1024K (K = 1024) words of memory.

6.2 The first 64K of memory map be made up of any V70 series compatible memory modules. Modules above the first 64K must be designed to use the bank select lines provided by the map (e.g., the 660 ns Semiconductor Memory). However, the combined loading of all the memories in the system must not exceed 19.0 ma total. When 19.0 ma is reached, no more memory modules can be added. The calculations should be made based on the values in the following table:

Memory Type	Part Number	Loading
660ns 8K Core	W4400613	2ma
330ns 8K Semi	W4400618	4ma
990ns 16K Core	W4400767	2ma
660ns 16K, 32K, or 64K Semi	W4400769	.36ma

6.3 The map provides 15 memory bank select lines for selecting memory banks above 64K in 64K increments (only) up to 1024K total. Note that, unless 64K memory modules are utilized, the memory space will not be continuous.

6.4 The connector/pin assignments for the memory bank select lines are given in the following table:

Bank Select Line for Memory Bank	Mega-Memory Map Bank Select Connector/Pin
0	No Cable Required
1	J8-2 (65)
2	J8-6 (128)
3	J8-10 (193)
4	J9-2 (256)
5	J9-6 (321)
6	J9-10 (386)
7	J10-2 (446)
8	J10-6 (512)
9	J10-10 (577)
10	J11-2 (642)
11	J11-6 (708)
12	J11,10 (773)
13	J12-2 (838)
14	J12-6 (904)
15	J12-10 (968)

6.5 Connect one memory bank select cable from the appropriate map bank select connector/pins to each memory module assigned to memory space above 64K (per the table in paragraph 6.4). Reference 660ns Semiconductor Memory option drawing for proper connection at memory end of each cable.

6.6 The bank select cables must be provided by systems memo (one for each 64K increment utilized) use cable W5300996-XX.

7.0 Processor Board Requirements

7.1 BINS - (Memory Protect Present) must be wired to ground (Jumper Clip or Wire Wrap F-F).

7.2 Configure jumpers at locations 23, 24, 25 and 26 per Note 5 and the Chart on Sheet 6 of W0101331.

7.3 Remove jumper clip L1-L2 and add jumper clip L2-L3.

8.0 BTC Requirements

8.1 If a BTC, W4400629-01 or W4400874-00 is used for a system with PMA and Memory Map, the following wires should be added to the I/O expansion chassis to accommodate the map error stop signal (BTMES-I):

a. JX-94 to JY-96 and JZ-94

b. JX-95 to JY-98 and JZ-95

where JX is the I/O cable slot,
JY is the BTC slot and
JZ is the terminator slot.

9.0 BIC Requirements

9.1 If a BIC, W4400689-03, is used for a system with map, the following wires should be added to the I/O expansion chassis to accommodate the map error stop signal (BIMES-I) and I/O key bits (IOK1-4-I):

			V77-600	
a.	JX-109 to JU-109	and	JZ-109	IOK1-I
b.	JX-110 to JU-110	and	JZ-110	IOK2-I
c.	JX-111 to JU-111	and	JZ-111	GND
d.	JX-112 to JU-112	and	JZ-112	IOK3-I
e.	JX-113 to JU-113	and	JZ-113	IOK4-I (BIMES-I)
f.	JX-114 to JU-114	and	JZ-114	GND
g.	JU-93 to JU-113	(all BIC slots)		

a.	JX-93	to	JU-93	and	JZ-93	BIMES-I
b.	JX-95	to	JU-95	and	JZ-95	GND
c.	JX-109	to	JU-109	and	JZ-109	IOK1-I
d.	JX-110	to	JU-110	and	JZ-110	IOK2-I
e.	JX-111	to	JU-111	and	JZ-111	GND
f.	JX-112	to	JU-112	and	JZ-112	IOK3-I
g.	JX-113	to	JU-113	and	JZ-113	IOK4-I
h.	JX-114	to	JU-114	and	JZ-114	GND

where JX is the I/O cable slot,
JU is the BIC slot and
JZ is the terminator slot.

10.0 I/O Terminator Requirement

10.1 Terminator shoe, W4400664- 00 or W4400718- 00 or W4400718- 03, should be replaced by W4400664- 02 or W4400718- 02 or W4400718- 05 respectively on the I/O expansion chassis in a system with map installed.

11.0 For additional information, refer to the following documents:

a. V73 Process Board
Option Drawing W0101331

b. V73 Option Board
Option Drawing W0101332

c. V73 WCS Board
Option Drawing W0101444

d. V73 WCS Board
Option Drawing W0101884

12.0 For cable connections on the front edge of boards, see sheets 9 and 10 of this drawing.

13.0 When connectors are added to accommodate this option, remark the cables with the appropriate dash number, as determined by reference to the basic cable assembly drawing, W5300674, W5300709 or W5300807.

14.0 I/O Port Requirements

14.1 Add the following wires to the I/O port.

a. J03-29 to J02-109 (IOK-1)
J03-30 to J02-110 (IOK-2)
J03-31 to J02-112 (IOK-3)
J03-32 to J02-113 (IOK-4)
J03-27 to J02-94 (BTMES-1)
J03-34 to J02-93 (BIMES-1)

15.0 Option Board Requirements

15.1 "B Port" memory time out is accomplished by a wire wrap jumper on the option board.

Add Jumper

A25 (MRMYB-) to B25 (MRQY-)

B25 (MRQY-) to B49 (MRQPTB-)

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REV E

SPECIFICATION FOR MEMORY MAP MODULE

FUNCTION	LOGIC PAGE	STANDARD CONFIGURATION *Indicates Locations Where Wire Wrap is Required	ALTERNATE CONFIGURATIONS
I/O Device Address	11.0	V7E1-V7E2 Etched I/O Device Address = 46	Cut etch and jumper V7E2-V7E3 I/O Device Address = 56
Map Loading/Reading High Speed DMA Priority	16.0	*FIE10, FIE11, FIE12, FIE13 should be wired to the High Speed DMA Chain such that the Map Loading/Reading has the Lowest Priority of all high speed DMA users.	
Normal DMA Priority to enable Map Loading/Reading	16.0	FIE3 TO FIE14	*FIE14 and FIE15 can be wired to any normal DMA Priority Chain. FIE14 is the Priority in and FIE15 is the Priority out.
Map Loading/Reading Complete Interrupt Enable	19.0	F2E1-2 Etched Interrupt Disabled (Vortex II Compatible)	Cut etch and jumper F2E2-3 Interrupt Enabled
Key Select From Processor Key Bus or Map Key Register	21.0	K11E2-9 Etched Select Map K11E4-10 Etched Key Register K11E6-11 Etched (Standard) K11E8-12 Etched	Cut etch and jumper K11E1-9 Select K11E3-10 Processor K11E5-11 Key Bus K11E7-12
Privileged Instruction Enable	21.0	K2E1-2 Etched Privileged Instruction Enabled (Standard)	Cut etch and jumper K2E2-3 Privileged Instructions Disabled

96A0039-000B

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SH 8 OF 11

REV H

SPECIFICATION FOR MEMORY MAP MODULE

FUNCTION	LOGIC PAGE	STANDARD CONFIGURATION *Indicates Locations Where Wire Wrap is Required	ALTERNATE CONFIGURATIONS
Executive Mode Enable	35.0	D6E1-2 Etched — Executive Mode Enabled (Standard)	Cut etch and jumper D6E1-3 Executive Mode Disabled
E-Bus Enable	6.0	V1E2-V1E3 Etched — E-Bus Enabled	Cut etch and jumper V1E1-V1E2 Disable of Map E-Bus Drive
Select PMA Key (Special Mode)	21.0	L2E1-2 Etched — Dynamic PMA Key Select	Cut etch and jumper L2E1-3 Static PMA Key Select
Memory Request Delay #1	39.0	Set A-B Delay per timing diagram on page 39 of logics (W9100569).	
Memory Request Delay #2	39.0	Set A-C Delay per timing diagram on page 39 of logics (W9100569).	
Memory Protect	30.0	N5E1-2 Etched — Memory Protect Enabled	Cut etch and jumper N5E2-3 Memory Protect Disabled
Enable DMA Key	22.0	D2E2-3 Etched — DMA Key 'Enabled	Cut etch and jumper D2E1-2 DMA Key Disabled
V76 I/O	31.0	V72-76 (switch at board location X7)	
V77 I/O	31.0	V77 (switch at board location X7) logic shows switch in V77 configuration	

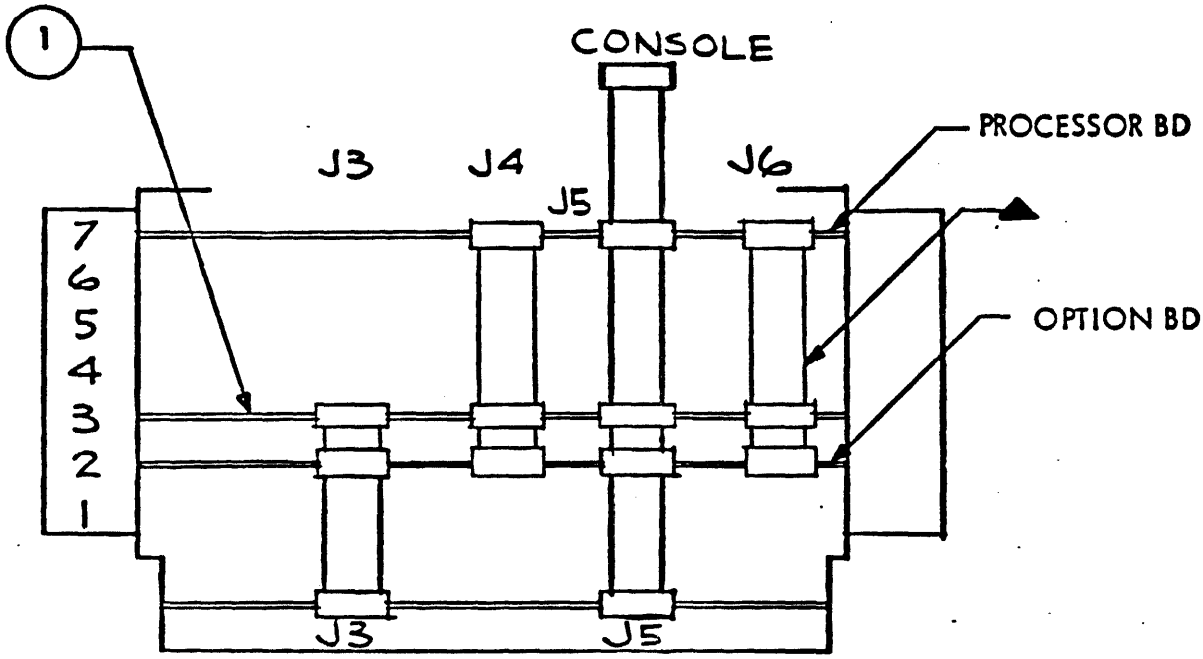

FIGURE 1
FOR -00 & -01 IN A 7" CHASSIS

▲ Required Cable J6 and the addition of Connectors to J3, J4 and J5 must be specified by systems memo.

	CODE IDENT NO. 21101		W010 1938	H
			SH 9 OF 11	REV

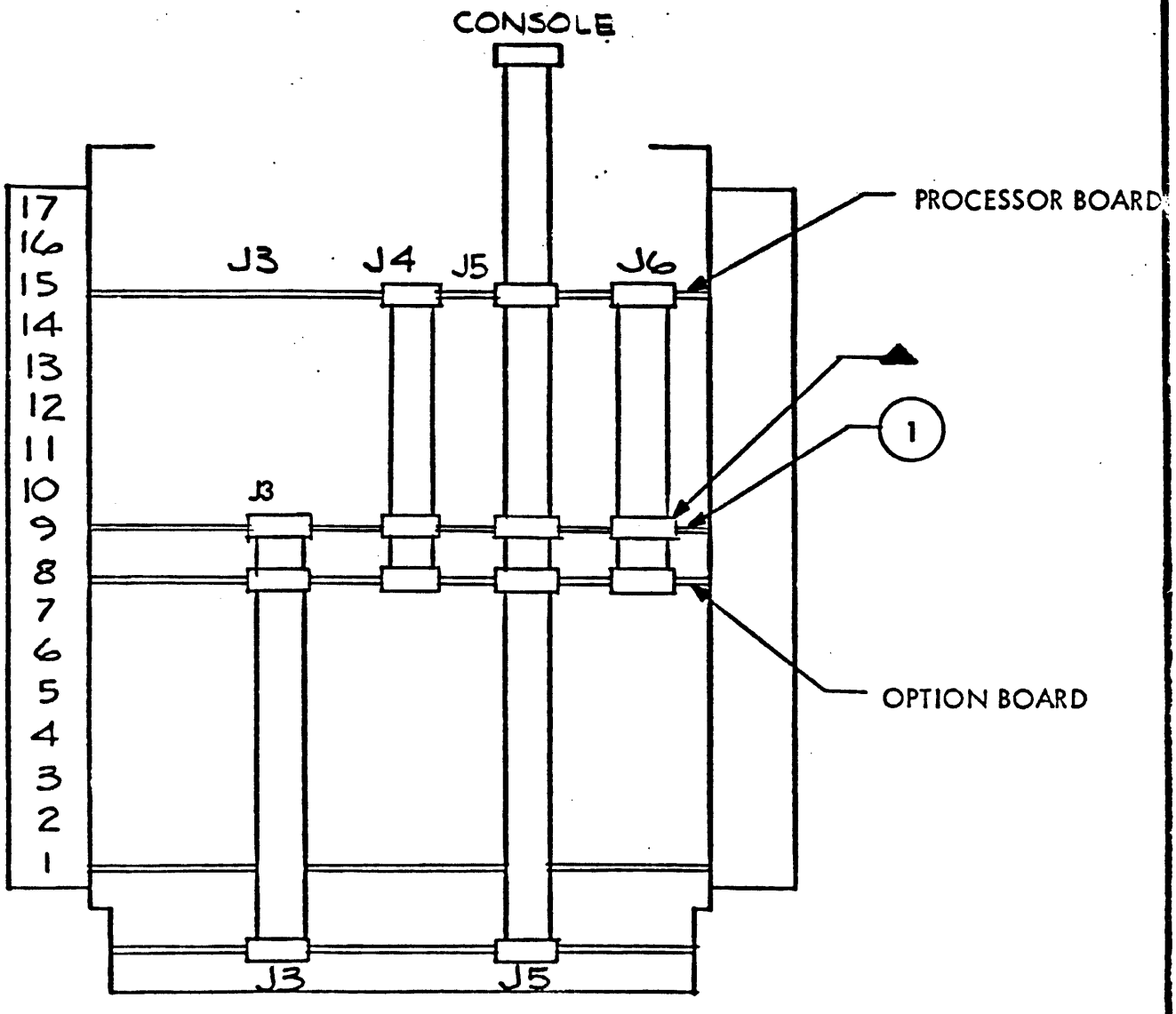

FIGURE 2

FOR -00 & -01 IN A 14" CHASSIS

▲ Required Cable J6 and the addition of Connectors to J3, J4 and J5 must be specified by systems memo.

	CODE IDENT NO. 21101		W 0101938	H
			SH 10 OF 11	REV

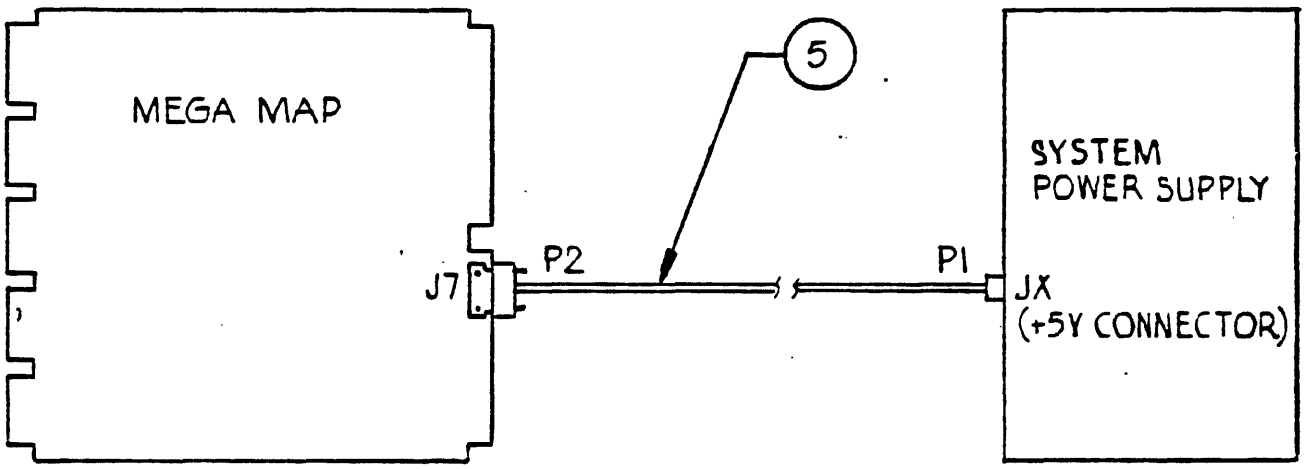

FIGURE 3

(-01) WITH DC POWER CABLE

	CODE IDENT NO. 21101		W0101935	H
			SH 11 OF 11	REV

UNIVAC PARTS LIST

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MFG CODE	ISSUE DATE	CONTROL		DOC NO.		SHEET
J ,W	81/02/23	W 777	PL	W4400785	2	1

TITLE	PCC	ADC	PCD	COMM CODE	CA	U/M	ST	TYPE	SIZE	CLASS
PC ASSY-MEGA MAP						EA	A	M	C	A

FIND NO.	QUANTITY REQUIRED	U/M	PCC	PART OR IDENT NO DOCUMENT NO.	PART OR IDENT NO DASH	EIR AND PART DESCRIPTION INFORMATION	ECC	ST	CHG
Z026				W 94519	-01	PL REV AD, PIC REV AD, RANGE 00 - 00 EIR RELEASED 81/02/23			*
Z025				W 94490	-01	PL REV AC, PIC REV AA, RANGE 00 - 00 EIR RELEASED 80/10/08			
*****	*******	***	**	*	*****	********** COMMON DATA **********			
1	1	EA		W4000651	-00	PC BOARD MEGA MAP (DM467)		A	*
2	3	EA	I	3007755	-00	INTEGRATED CIRCUIT TTLH 74H04 * GT HEX INVERT		I	*
3	4	EA	I	5036515	-00	INTEGRATED CIRCUIT TTLH 74H00 * GT NAND 2IN		I	*
4	2	EA	I	5036519	-00	INTEGRATED CIRCUIT DIGITAL 2, 2WIDE 2INPUT AND/OR INVERT		I	*
5	1	EA	I	3008190	-00	INTEGRATED CIRCUIT TTL 7442 * DCDR 4-10LN		I	*
6	2	EA	I	5036149	-00	INTEGRATED CIRCUIT DIGITAL DUAL 4-INPUT NAND GATE		I	*
7	2	EA		3013468	-00	INTEGRATED CIRCUIT - IC204 TTLH 74H30 * GT NAND 8IN		I	*
8	5	EA	I	5036157	-00	INTEGRATED CIRCUIT DIGITAL DUAL D TYPE EDGE TRIG, F-F		A	*
9	2	EA	I	3013355	-00	INTEGRATED CIRCUIT-IC192 TTLH 74H21 * GT AND 4IN		I	*
10	2	EA	I	9004321	-01	INTEGRATED CIRCUIT DIGITAL TTL FF 2 JK ET BT	0	I	*
11	7	EA	I	5036505	-00	INTEGRATED CIRCUIT TTLH 74H08 * GT AND 2IN		I	*
12	1	EA	I	5036521	-00	INTEGRATED CIRCUIT DIGITAL TTL 3002 * GT NOR 2IN		I	*
13	5	EA	I	2899571	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S00 * GT NAND 2IN		A	*
14	1	EA	I	5036522	-00	INTEGRATED CIRCUIT DIGITAL TTL 3003 * GT OR 2IN		I	*
15	4	EA	I	4915711	-01	INTEGRATED CIRCUIT TTL 7438 * GT NAND 2IN		I	*
16	18	EA		W4900128	-01	INTEGRATED CIRCUIT, DIGITAL TTL 7438 QUAD 2IN NAND		I	*
17	5	EA		5036524	-00	INTEGRATED CIRCUIT DIGITAL TTL 3404 * FF LATCH 6BT		I	*
18	4	EA	I	2892081	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S64 * GT AOI		A	*
19	1	EA		2899712	-00	INTEGRATED CIRCUIT DIGITAL TTL 9321 * DECODE 1-4		A	*
20	16	EA	I	3012655	-00	INTEGRATED CIRCUIT - IC 167 TTL 74153 * MUX 4-1LN		I	*
21	14	EA	I	5036504	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S04 * GT HEX INVERT		A	*
22	4	EA	I	5036516	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S10 * GT NAND 3IN		A	*

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MFG CODE	ISSUE DATE	CONTROL		DOC NO.		SHEET	
J ,W	81/02/23	W 777	PL	W4400785	2	2	*

TITLE	PCC	ADC	PCD	COMM CODE	CA	U/M	ST	TYPE	SIZE	CLASS	
PC ASSY-MEGA MAP						EA	A	M	C	A	*

FIND NO	QUANTITY REQUIRED	U/M	PCC	PART OR IDENT NO DOCUMENT NO.	DASH	EIR AND PART DESCRIPTION INFORMATION	ECC	ST	CHG
23	2	EA	I	5036506	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S11 * GT AND 3IN		A	*
24	8	EA	I	5036146	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S74 * FF DUAL D		A	*
25	7	EA	I	9004633	-01	INTEGRATED CIRCUIT DIGITAL TTLS 74S112 * FF DUAL JK		A	*
26	2	EA		3013359	-00	INTEGRATED CIRCUIT TTLS 74S157 * MUX 2 INPUT		A	*
27	17	EA	I	2899587	-00	INTEGRATED CIRCUIT DIGITAL TTL 74175 * FF D QUAD		A	*
28	6	EA		3013489	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S158 * MPX 2-1LN		I	*
29	1	EA	I	2892053	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S175 * FF QUAD D		A	*
30	1	EA		3013471	-00	INTEGRATED CIRCUIT - IC207 TTLS 74S139 * DCDR 2-4 LINE		A	*
31	2	EA	I	2892085	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S138 * DCDR 3-8 LINE		A	*
32	1	EA	I	2892084	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S02 * GT NOR 2IN		A	*
33	10	EA		6558762	-00	INTEGRATED CIRCUIT TTL 74191 * CNTR 4BT UP/D		I	*
34	6	EA	I	3013587	-00	INTEGRATED CIRCUIT DIGITAL TTLS 74S08 * GT AND 2IN		A	*
35	1	EA	I	3013503	-00	INTEGRATED CIRCUIT TTLLS 74LS04 * GT HEX INVERT		A	*
36	13	EA	B	W4900314	-02	INTEGRATED CIRCUIT, MEMORY TTL 93425A RAM TS 1KX1		I	*
37	5	EA	I	3013504	-00	INTEGRATED CIRCUIT TTLLS 74LS08 * GT AND 2IN		A	*
39	84	EA	C	4916657	-06	CAP FXD CER DIEL 50V +80 - 20% 100K PF		A	*
				REF DES	(1)	C1-C4,C6-C50,C52 C53			
40	1	EA		W6901500	101	CAPACITOR, FIXED, MICA DIEL 500V 5% 100 PF		A	*
				REF DES	(1)	C54			
41	5	EA		W7100200	225	CAPACITOR, FXD, TANTALUM DIEL 2.2 UF 10% 20V		A	*
				REF DES	(1)	C5 C51 C88 C89 C90			
42	1	EA		W8000046	-00	DELAY LINE 168.00NSEC TD26TERM 900HM		A	*
				REF DES	(1)	DL1			
43	1	EA		W6502500	910	RES,FXD,COMPOSITION,1/4W,5% 91 OHMS		A	*
				REF DES	(1)	R21			

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MFG CODE	ISSUE DATE	CONTROL		DOC NO.		SHEET	
J ,W	81/02/23	W 777	PL	W4400785	2	3	*

TITLE	PCC	ADC	PCD	COMM CODE	CA	U/M	ST	TYPE	SIZE	CLASS	
PC ASSY-MEGA MAP						EA	A	M	C	A	*

FIND NO.	QUANTITY REQUIRED	U/M	PCC	PART OR IDENT NO. DOCUMENT NO.	DASH	EIR AND PART DESCRIPTION INFORMATION		ECC	ST	CHG
44	5	EA		W6502500	151	RES,FXD,COMPOSITION,1/4W,5%	150 OHMS		A	*
				REF DES	(1)	R1-R7				
45	6	EA		W6502500	201	RES,FXD,COMPOSITION,1/4W,5%	200 OHMS		A	*
				REF DES	(1)	R10-R13 R13 R16 R17				
46	6	EA		W6502500	471	RES,FXD,COMPOSITION,1/4W,5%	470 OHMS		A	*
				REF DES	(1)	R1 R2 R8 R9 R14 R19				
47	2	EA		W6502500	331	RES,FXD,COMPOSITION,1/4W,5%	330 OHMS		A	*
				REF DES	(1)	R15 R18				
49	1	EA	I	2899573	-00	INTEGRATED CIRCUIT DIGITAL	TTLH 74H11 * GT AND 3IN		I	*
50	1	EA		W5700311	-01	CONN, PRINTED CIRCUIT, ELEC	8CR MTD 26 FIXED PINS		A	*
				REF DES	(1)	J7				
51	5	EA		W5700353	-08	CONN, PRINTED CIRCUIT, ELEC	9 PINS		A	*
				REF DES	(1)	J8-J12				
52	1	EA		W7800104	-03	SWITCH, TOGGLE, ROCKER	SPST ON NONE OFF 1A 40VDC		A	*
53	1	EA		W2200105	-03	SPACER	.25/.38 DIA X .406 4-40 THD		A	*
54	1	EA		W2200105	-00	SPACER	.38 DIA X .120		A	*
55	2	EA		W0400709	-00	BOARD STIFFENER,FRONT			A	*
56	1	EA		2899827	-00	DIODE LIGHT EMITTING	7MA CONT FWD CUR		A	*
57	4	EA		W5800066	-02	TERMINAL, STUD	PRESS IN,.084MTG LG TURRET		A	*
				REF DES	(1)	E1-E4				
58	15	EA		W5800062	-09	CONTACT ELECTRICAL WIRE WRAP	1 POST .385 F/.076		A	*
59	1	EA		W5800195	-10	SOCKET INTEGRATED CIRCUIT	16TERM 2 INLINE PC BOARD TIN		A	*
				REF DES	(1)	J13				
60	4	EA		W6502500	301	RES,FXD,COMPOSITION,1/4W,5%	300 OHMS		A	*
				REF DES	(1)	R23-R26				

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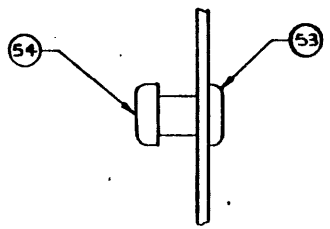
MFG CODE	ISSUE DATE	CONTROL		DOC NO.		SHEET	
J ,W	81/02/23	W 777	PL	W4400785	2	4	*

TITLE	PCC	ADC	PCD	COMM CODE	CA	U/M	ST	TYPE	SIZE	CLASS	
PC ASSY-MEGA MAP						EA	A	M	C	A	*

FIND NO.	QUANTITY REQUIRED		U/M	PCC	PART OR IDENT NO. DOCUMENT NO.	DASH	EIR AND PART DESCRIPTION INFORMATION		ECC	ST	CHG
61	1		EA		W7800114	-00	SWITCH, TOGGLE, ROCKER	DPDT ON NONE OFF.05A 30VDC		A	*
62	2		EA		2892034	-00	INTEGRATED CIRCUIT DIGITAL	TTL 7414 * TRIG HEX 8CHM		A	*
63	AR		IN		W5300333	-90	WIRE, ELEC	30SLD 300V PVD WHT		A	*
F001			X		W9100569	-00	LOGIC DIAGRAM	MEMORY MAP		A	
S001			X		SW01163	-00	MARKING,MECHANICAL SPECS	D8GN-F/GENERAL IDENTIFICATION		A	
S002			X		SW00536	-00	THREADED FASTENERS SPECS	D8GN-SELECTION-INSTALLATION		A	
*****	*******	***		*	**********	****	**********	VAR DATA PART - 00 *********		A	

WIRE LIST								
IDENTIFICATION		TERMINATION		TERMINATION		WIRE		
NO.	SIGNAL	FROM	F/N	TO	F/N	COLOR	AWG	F/N
1	JUMPER	FIE 5	W/W	FIE 14	W/W	WHT	30	63

REVISIONS					
REV	EN	CHG CODE	DESCRIPTION	DR	APPD
A	[illegible]	—	PRODUCTION RELEASE	[illegible]	[illegible]
B	[illegible]	3	REVISED SECTION A-A	[illegible]	[illegible]
C	84422	3	LCT F10, SH 2, C62 WAS C55. DELETE R19 LCT EF9. LCT D10, SH 2, C61 WAS C52. REVISED STIFFENER. ADDED MAX COMPONENT HEIGHT. TITLE WAS MEMORY MAP. ADDED '+' AT DS1.	[illegible]	[illegible]
—	84719	—	ADDED NOTE 4 TO SH.1 & NOTE FLAG 4 TO PIN 3 ON SH 2 ZONE B1	[illegible]	[illegible]
D	85093	5	DELETED NOTE 4, REVISED CONN PIN CALLOUT	[illegible]	[illegible]
E	85065	1	REVISED IC LOCATIONS X6, W8 & M10, ADDED F/N 57	[illegible]	[illegible]
F	85064	1	ADDED R23, 24, 25, 26	[illegible]	[illegible]
G	85196	1	REVISED IC LOCATIONS B2 & S5	[illegible]	[illegible]
H	85448	1	ADDED F/N 61	[illegible]	[illegible]
J	85602	1	LOCATIONS A10 & C10 WERE -35- (SH.2)	T.N	[illegible]
K	85624	2	ADDED WIRE LIST	T.N	[illegible]
L	EIR W87474-02		RELEASE INTO API	R.B.	
AA	W96232 01		UPDATED FORMAT. DOCUMENT NO. WAS 4400785	R.B.	[illegible]
AD	W98519-01		SEE EIR		[illegible]



SECTION A-A

SCALE 2/1

W4400785

AD

REFERENCE DRAWINGS	
W4000651	PW BOARD
W9701028	ARTWORK
W9701029	SOLDERMASK
W9701030	SILKSCREEN
W9100569	LOGIC DIAGRAM

6. "FIND" NUMBERS FOR PARTS, IDENTIFIED BY REFERENCE DESIGNATIONS, APPEAR IN PARTS LIST

5. NUMBER BETWEEN DASHES ARE PARTS LIST FIND NUMBERS

4. ~~REMOVE P/N 3 AT ASSY — TYP J8 THRU J12~~

3. INSTALL F/N 32 & 61 AFTER CLEANING PROCESS.

2. USE HARDWARE IN ACCORDANCE WITH (S02)

1. IDENTIFY PER (S01)

NOTE: UNLESS OTHERWISE SPECIFIED

PART NO. W4400785-00

~~IDENT NO.~~

FOR MATL REQUIREMENTS SEE PL

PL REV LETTER CONTROLS DOCUMENT.

MODEL NO.

NEXT ASSY

MATERIAL

FINISH

DIMENSIONS ARE IN INCHES AND AFTER FINISHING

TOLERANCES (UNLESS OTHERWISE SPECIFIED)

.X ± .1

.XX ± .03

.XXX ± .010

ANGLES ± 0.5°

BREAK ALL SHARP EDGES .010 R APPROX

DO NOT SCALE DRAWING

DR	[illegible]	2/4/75
CHK	[illegible]	2/10/75
DSGN	[illegible]	2/4/75
ENGR	[illegible]	2/10/75
APPD	[illegible]	2/10/75
APPD		

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SPERRY UNIVAC

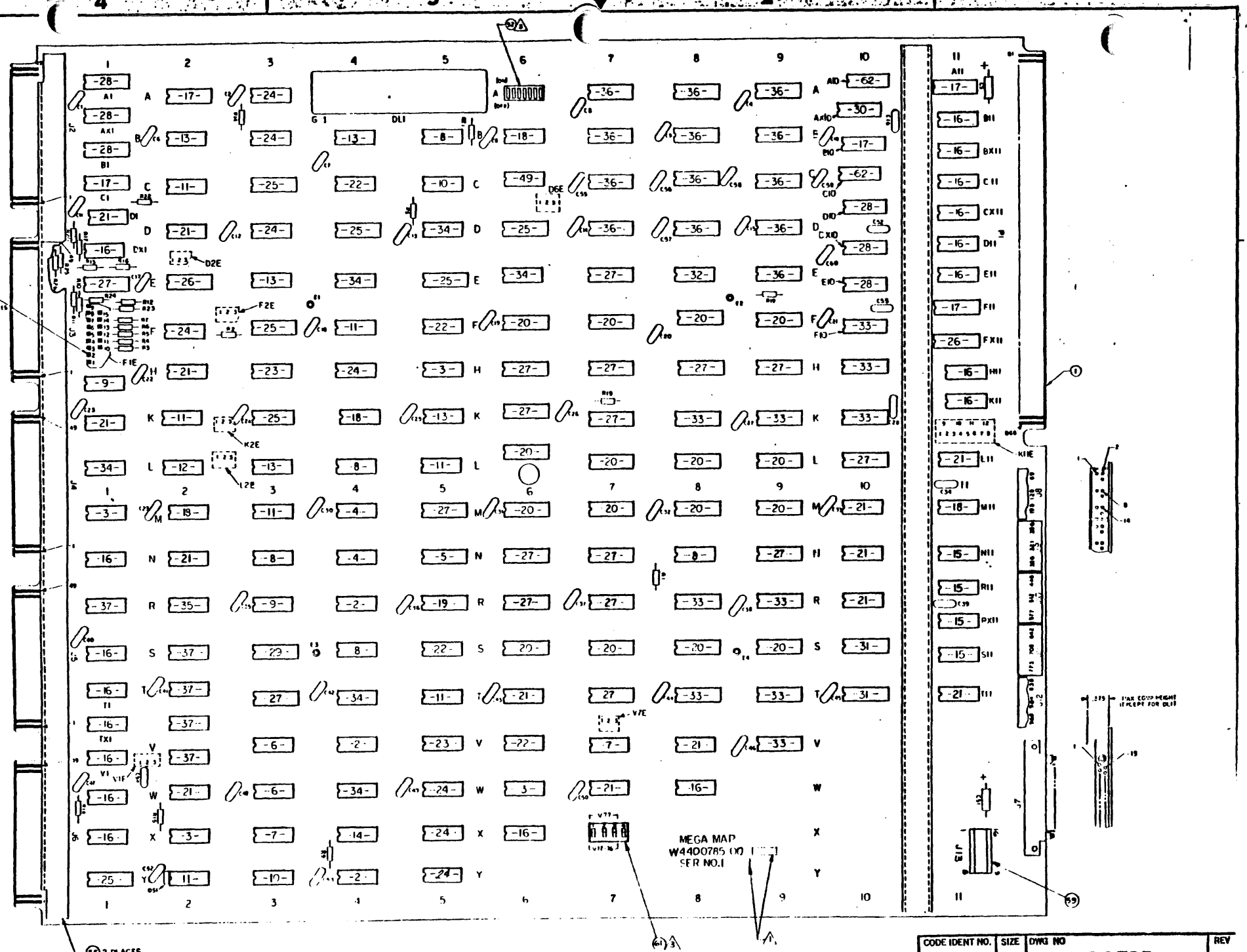
TITLE

PC ASSEMBLY MEGA MAP

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	W4400785	AD

SCALE 1/1

SHEET 1 OF 2



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	W4400785	AD
SCALE —		SHEET 2 OF 2	

4 | 3 | 2 | 1

REVISIONS						
ZONE	LTR	E N	DESCRIPTION — FOR DETAILS SEE	DR	DATE	APPROVED
	K	85624	REVISED SHEET 16	T.N	11-26-79	W.C.
	L	87965	REVISED SH'S 1, 3 & 41	T N	5/30/79	

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE 0.1 μf
2. POWER AND GND DISTRIBUTION FOR IC'S:
   VOLTAGES - PIN 14 FOR 14 PIN IC'S
   PIN 16 FOR 16 PIN IC'S
   GND - PIN 7 FOR 14 PIN IC'S
   PIN 8 FOR 16 PIN IC'S
3. ALL RESISTORS ARE 1/4 W, ± 5%.

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REFERENCE DRAWINGS	
44P0785	PARTS LIST
44C0785	ASSEMBLY
40C0651	P.W. BOARD
97E1028	ARTWORK
97E1029	SOLDER MASK
97E1030	SILKSCREEN

E4	
J13	J1
P1	
DS1	
C90	
R26	
HIGHEST	NOT USED

REFERENCE DESIGNATIONS

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| SHEET | | | | | |

LOC	CHIP TYPE	WHERE USED
A1	745158	2A0
A2	3404	3A0 4A0 5A0 6A0 7A0
A3	74S74	3B0 3C0
A4		
A5		
A6		
A7	93425A	2B0
A8	93425A	2C0
A9	93425A	2D0
A10	7414	3A0 4A0 5A0 6A0 7A0 8A0 9A0
A11	3404	3B0 4B0 5B0 6B0 7B0 8B0 9B0
AX1	745158	2B0
AX10	745139	2C0
B1	745158	2C0
B2	74S00	2D0 3D0 4D0 5D0
B3	74S74	3B0 3C0
B4	74S00	3B0 3C0 4C0 5C0
B5	74H74	3A0 3D0
B6	74S64	3D0
B7	93425A	2A0
B8	93425A	2C0
B9	93425A	2D0
B10	3404	2D0 3D0 4D0 5D0 6D0
B11	7438SEL	3A0 4A0 5A0 6A0
BX11	7438SEL	3A0 4A0 5A0 6A0
C1	3404	2D0 3B0 3C0 3D0 4D0 5D0 6D0
C2	5001	3B0 4B0 4C0 5B0 5C0
C3	745112	4B0 5B0
C4	74S10	3B0 3C0 5A0
C5	74H108	3A0 3A0
C6	74H11	3D0 5D0
C7	93425A	2B0
C8	93425A	2C0
C9	93425A	2D0
C10	7414	3A0 4A0 5A0 6A0
C11	7438SEL	3D0 3D0 3A0
CX11	7438SEL	3D0 3D0 4D0 5D0 6D0
D1	74S04	3B0 4B0 4D0 5B0 5D0 6B0
D2	74S04	4A0 4C0 5D0 6A0 6C0 6D0
D3	74S74	4A0 4D0
D4	745112	4D0 5D0
D5	74S08	3A0 3B0 3A0 3B0
D6	745112	3B0 3C0
D7	93425A	2A0
D8	93425A	2B0
D9	93425A	2C0

LOC	CHIP TYPE	WHERE USED
D10	745158	2D0
D11	7438SEL	2B0 2D0 3A0 3D0
DX1	7438SEL	3A0 3C0 4D0 5D0
DX10	745158	2A0
E1	74175	2B0
E2	745157	2D0
E3	74S00	4A0 4B0 4D0 5D0
E4	74S08	4D0 5B0 5A0 5C0
E5	745112	2B0 3A0
E6	74S08	3A0 3B0 3A0 3B0
E7	74175	6A0
E8	74S02	3B0 3A0 3B0 3D0
E9	93425A	2D0
E10	745158	2A0
E11	7438SEL	3D0 3D0 4D0 5D0
F1		
F2	74S74	3D0 3B0
F3	745112	4B0 4D0
F4	5001	2A0 2B0 2A0 2B0
F5	74S10	4B0 4B0
F6	74LS32	7A0 7D0
F7	74LS32	7A0 7D0
F8	74LS32	8A0 8D0
F9	74LS32	8A0 8D0
F10	74191	4A0
F11	3404	2B0
FX11	745157	2A0
H1	74H21	4A0 4D0
H2	74S04	4A0 3A0 3B0 5A0 5D0 6D0
H3	74S11	4B0 4C0 5B0
H4	74S74	4B0 4D0
H5	74H00	4A0 4D0 5B0 5D0
H6	74175	3B0
H7	74175	3B0
H8	74175	3B0
H9	74175	3C0
H10	74191	4A0
H11	7438SEL	3B0 3B0 3A0 3B0
K1	74S04	4B0 4B0 5A0 5A0 5B0 5B0
K2	5001	4B0 4D0 5D0 5A0
K3	745112	2B0 3A0
K4	74S64	4B0
K5	74S00	4A0 4D0 5B0 5D0
K6	74175	3A0
K7	74175	3B0

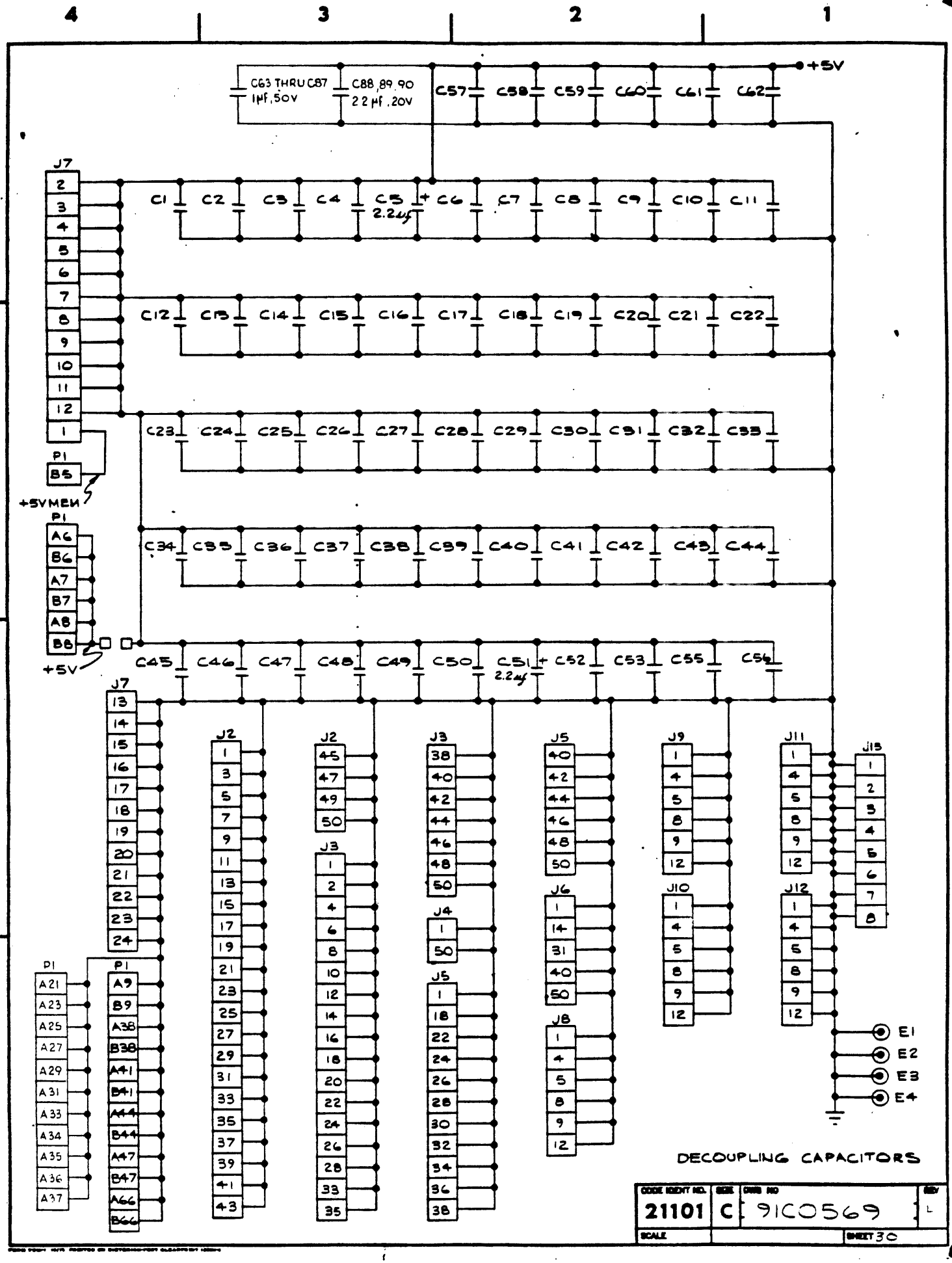
LOC	CHIP TYPE	WHERE USED
K8	74191	3A0
K9	74191	3A0
K10	74191	4A0
K11	7438SEL	3B0 3A0 3B0
L1	74S08	3B0 3D0 4A0 5B0 5A0
L2	3002	2B0 2A0 2D0 2B0
L3	74S00	2D0 2A0 3A0
L4	74H74	3A0 4A0
L5	3001	4A0 4D0 4B0 5A0
L6	74153	7A0 7D0
L7	74153	7A0 7D0
L8	74153	8A0 8D0
L9	74153	8A0 8D0
L10	74175	4A0
L11	74S04	2B0 2D0 3D0 3A0 4A0 4B0
M1	74H00	3A0 3B0 3A0 3B0
M2	74S64	2A0
M3	3001	4A0 3A0 3A0 3B0
M4	74H51	4A0 4D0
M5	74175	4A0
M6	74153	8A0 8D0
M7	74153	8A0 8D0
M8	74153	10A0 10D0
M9	74153	10A0 10D0
M10	74S04	2A0 2D0 3D0 3A0
M11	74S64	3A0
N1	7438SEL	4A0 4D0 5A0 5B0 5D0
N2	74S04	5A0 5D0 6A0 6D0 11A0 11D0
N3	74H74	8A0 12A0
N4	74H51	12A0 13A0
N5	7442	4A0
N6	74175	3B0
N7	74175	3B0
N8	74H74	12A0 13A0
N9	74175	3A0
N10	74S04	4A0 4B0 4D0 4A0 4B0 4D0
N11	7438	4B0 4D0 5B0 5D0
R1	74LS08	4A0 11A0 12A0 13A0
R2	74LS04	6A0 4A0 5B0 5A0 5D0
R3	74H21	6A0
R4	74H04	4A0 11A0 11B0 12A0 12D0 13A0
R5	9321	4A0 5B0
R6	74175	3B0
R7	74175	3B0
R8	74191	2A0
R9	74191	2A0

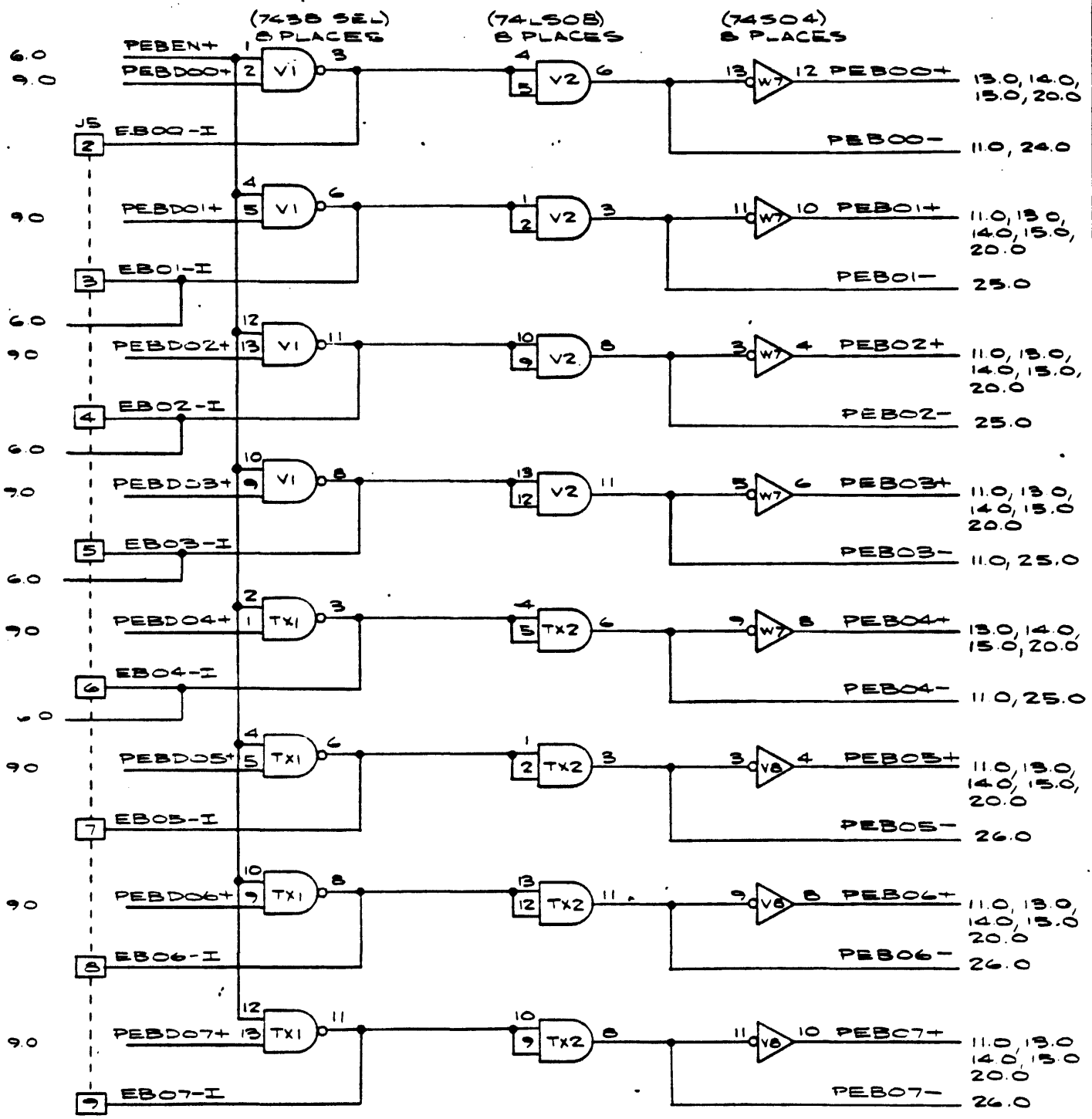
IC LOCATION CHART

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0569	L
SCALE			SHEET 2.0

LOC	CHIP TYPE	WHERE USED
R10	74S04	4.0 4.0 4.0 4.0 4.0 4.0
R11	7438	4.0 4.0 4.0 4.0
RX11	7438	4.0 4.0 4.0 4.0
S1	7438SEL	5.0 5.0 5.0 5.0
S2	74LS08	5.0 5.0 5.0 5.0
S5	74S175	2.0
S4	74H74	2.0 2.0
S5	74S10	5.0 5.0 5.0
S6	74153	3.0 3.0
S7	74153	3.0 3.0
S8	74138	4.0 4.0
S9	74155	4.0 4.0
S10	74S188	4.0
S11	7438	4.0 4.0 4.0
T1	7438SEL	6.0 6.0 6.0 6.0
T2	74LS08	5.0 5.0 5.0 5.0
T3	74175	11.0
T4	74S08	3.0 3.0 3.0 3.0
T5	3001	11.0 2.0 3.1.0 11.0
T6	74S04	3.0 3.0 3.0 3.0 3.0 3.0
T7	74175	11.0
T8	74191	15.0
T9	74191	15.0
T10	74S138	4.0
T11	74S04	4.0 4.0 4.0 4.0 4.0 4.0
TX1	7438SEL	4.0 4.0 4.0 4.0
TX2	74LS08	4.0 4.0 4.0 4.0
V1	7438SEL	4.0 4.0 4.0 4.0
V2	74LS08	4.0 4.0 4.0 4.0
V3	74H20	3.0 3.0
V4	74H04	6.0 6.0 6.0 6.0 11.0
V5	74S11	12.0 2.0 2.9.0
V6	74S10	6.0 6.0 6.0
V7	74H30	11.0
V8	74S04	4.0 4.0 4.0 2.8.0 2.9.0
V9	74191	15.0
W1	7438SEL	6.0 6.0 6.0 6.0
W2	74S04	2.0 2.0 2.9.0 3.0.0 3.2.0 11.0
W3	74H20	6.0 6.0
W4	74S08	3.1.0 2.8.0 3.5.0 11.0
W5	74S74	3.0 2.8.0
W6	74H00	2.0 2.0 3.0.0 3.1.0
W7	74S04	4.0 4.0 4.0 4.0 4.0 3.1.0

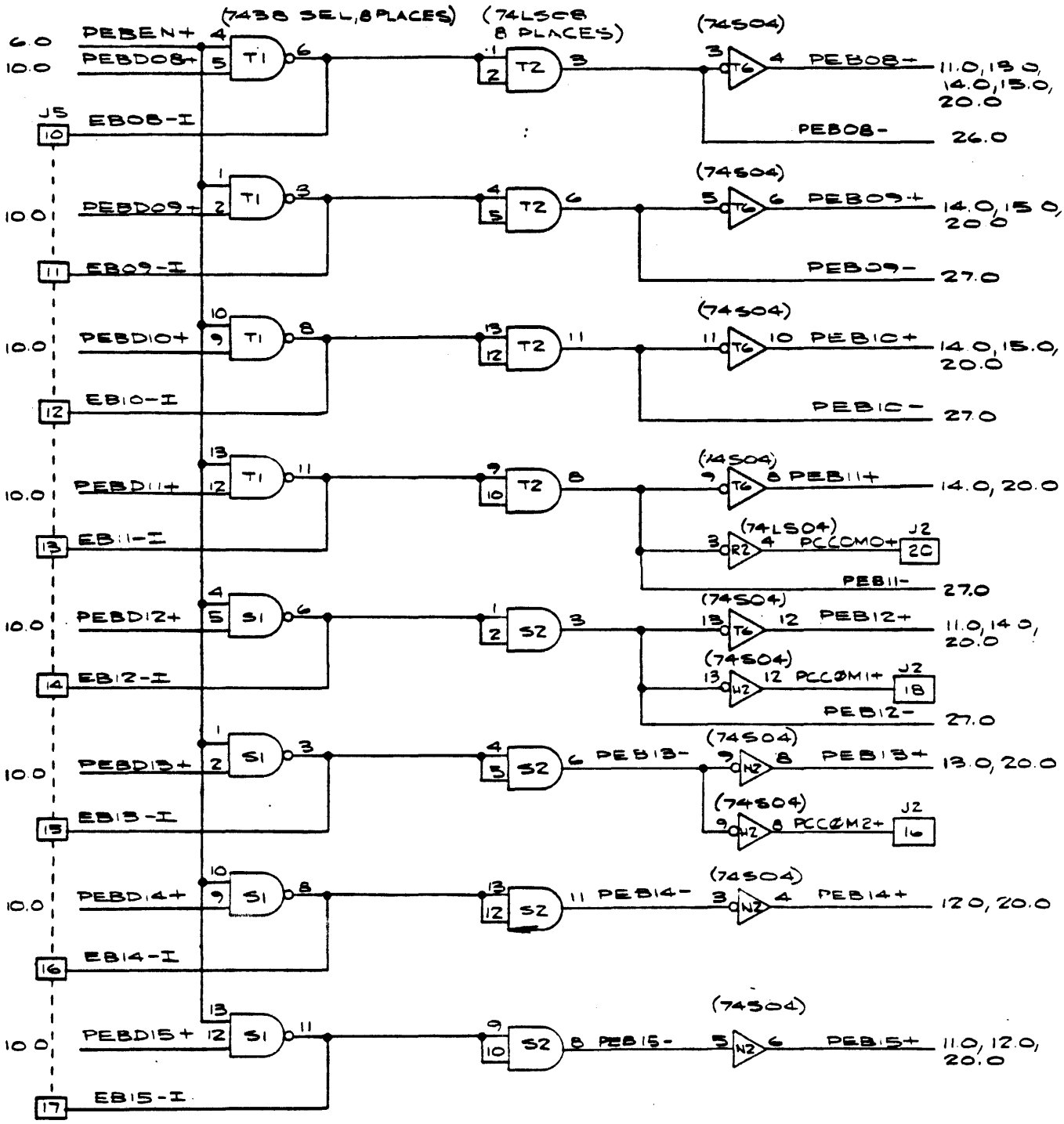
LOC	CHIP TYPE	WHERE USED
W8	7438 SEL	2.8.0 2.8.0 2.8.0 2.8.0
X1	7438 SEL	2.8.0 3.2.0 3.4.0
X2	74H00	6.0 3.0.0 3.4.0 3.1.0
X3	74H30	3.2.0
X4	3003	2.2.0 3.0.0 3.4.0
X5	74S74	2.9.0 3.1.0
X6	7438SEL	2.2.0 2.7.1.0 2.7.1.0 2.7.2.0
X7	78A0114-000	3.1.0 3.1.0 3.1.0
Y1	74S112	3.2.0 3.2.0
Y2	3001	2.8.0 3.4.0 3.1.0 3.8.0
Y3	74H108	3.0.0 3.0
Y4	74H04	6.0 3.0.0 3.0.0 3.4.0 3.7.0
Y5	74S74	3.1.0


4
3
2
1
D
C
B
A
C63 THRU C87
1MF, 50V
C88, 89, 90
22 MF, 20V
C57 C58 C59 C60 C61 C62
+5V
J7
2 3 4 5 6 7 8 9 10 11 12 1
C1 C2 C3 C4 C5 2.2uf + C6 C7 C8 C9 C10 C11
C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22
C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33
P1
B5
+5VMEM
P1
A6 B6 A7 B7 A8 B8
+5V
C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44
C45 C46 C47 C48 C49 C50 C51 2.2uf + C52 C53 C55 C56
J7
13 14 15 16 17 18 19 20 21 22 23 24
P1
A21 A23 A25 A27 A29 A31 A33 A34 A35 A36 A37
P1
A9 B9 A38 B38 A41 B41 A44 B44 A47 B47 A66 B66
J2
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43
J2
45 47 49 50
J3
1 2 4 6 8 10 12 14 16 18 20 22 24 26 28 33 35
J3
38 40 42 44 46 48 50
J4
1 50
J5
1 18 22 24 26 28 30 32 34 36 38
J5
40 42 44 46 48 50
J6
1 14 31 40 50
J8
1 4 5 8 9 12
J9
1 4 5 8 9 12
J10
1 4 5 8 9 12
J11
1 4 5 8 9 12
J12
1 4 5 8 9 12
J15
1 2 3 4 5 6 7 8
E1
E2
E3
E4
DECOUPLING CAPACITORS
CODE IDENT NO. 21101
SIZE C
DWG NO 9100569
REV L
SCALE
SHEET 30



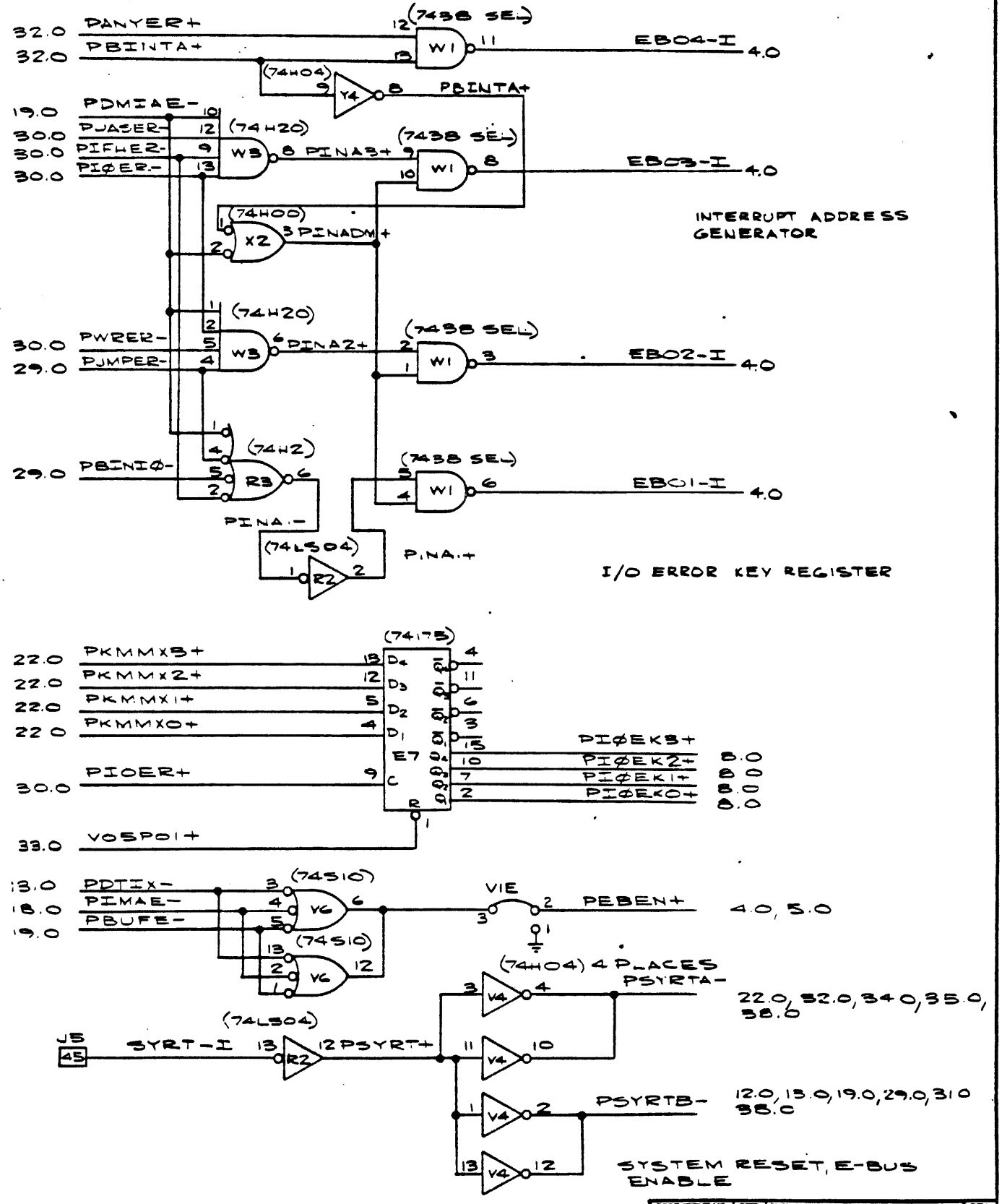
E-BUS DRIVERS/RECEIVERS
BITS 0-7

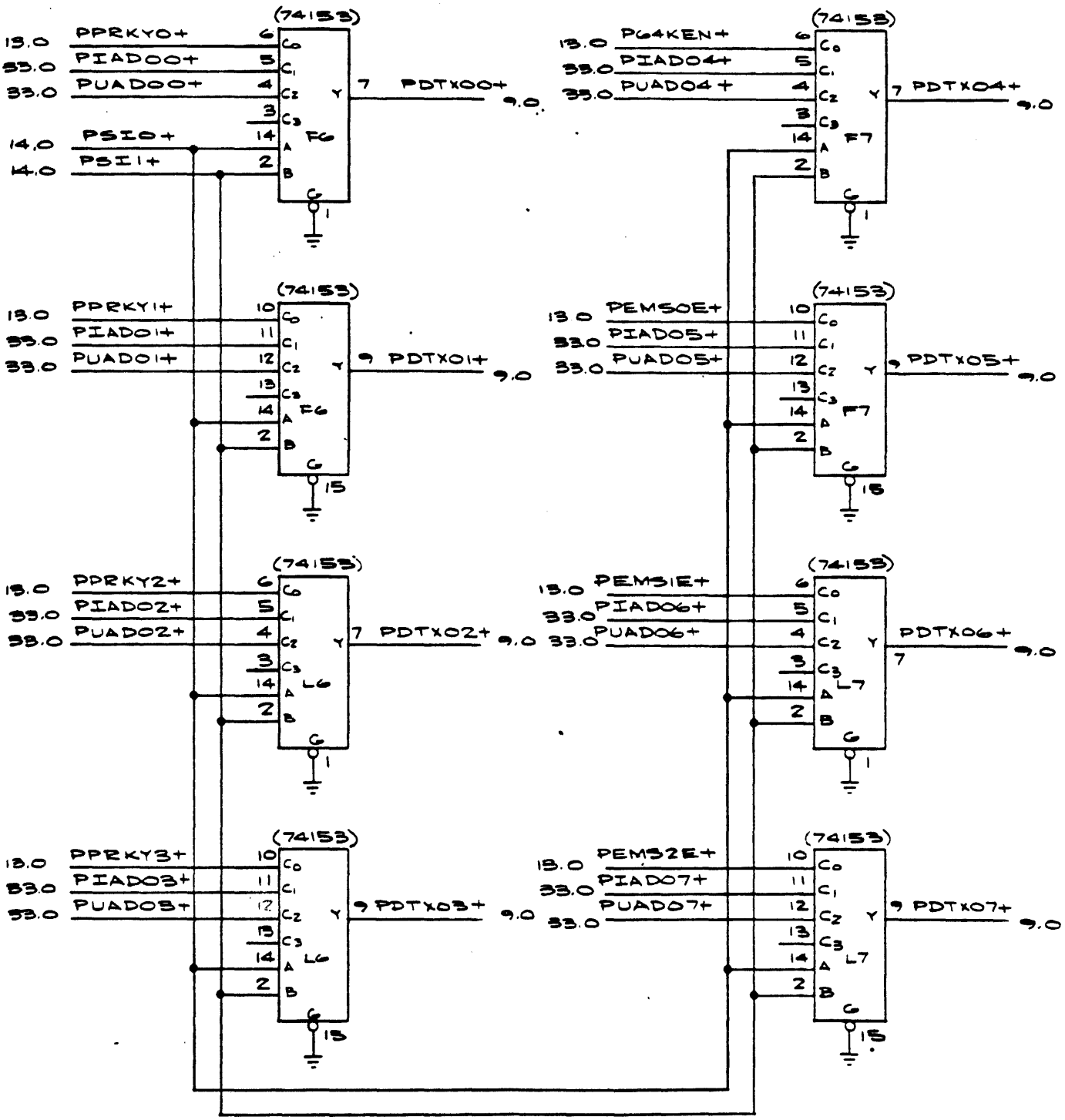
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100569	L
SCALE		SHEET 40	



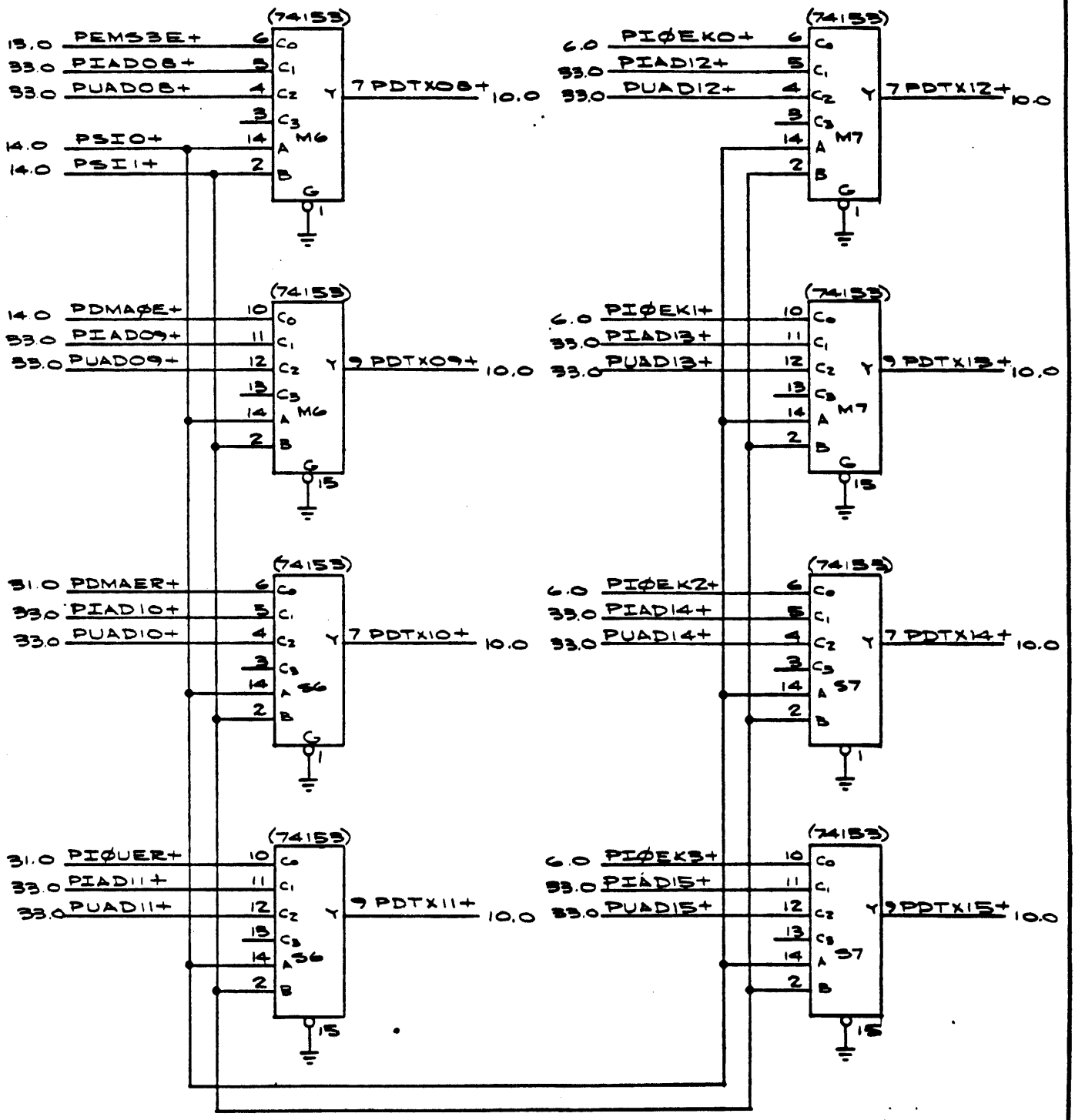
E-BUS DRIVERS/RECEIVERS
BITS 8-15

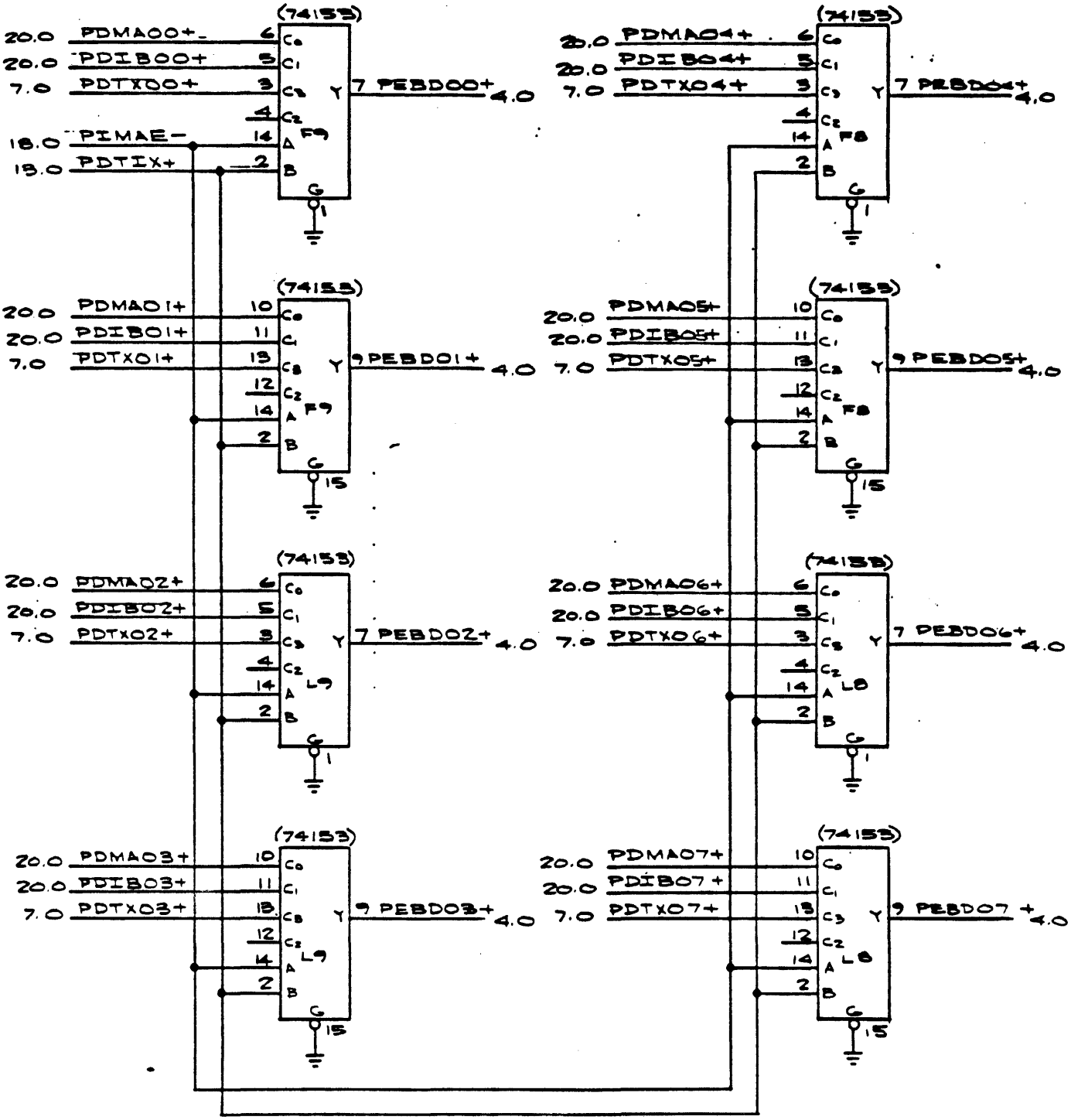
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100569	L
SCALE		SHEET 5.0	


4
3
2
1
D
C
B
A
32.0 PANYER+
32.0 PBINTA+
(74S38 SEL)
W1
EB04-I 4.0
(74H04)
Y4
PBINTA+
19.0 PDMIAE-
30.0 PJASER-
30.0 PIFHER-
30.0 PIØER-
(74H20)
W3
8 PINA3+
(74S38 SEL)
W1
EB03-I 4.0
INTERRUPT ADDRESS GENERATOR
(74H00)
X2
3 PINADM+
30.0 PWRER-
29.0 PJMPER-
(74H20)
W3
6 PINA2+
(74S38 SEL)
W1
EB02-I 4.0
29.0 PBINIØ-
(74H2)
R3
(74S38 SEL)
W1
EB01-I 4.0
PINA.-
(74LS04)
R2
PINA.+
I/O ERROR KEY REGISTER
(74175)
22.0 PKMMX3+
22.0 PKMMX2+
22.0 PKMMX1+
22 0 PKMMX0+
30.0 PIOER+
E7
PIØEK3+
PIØEK2+
PIØEK1+
PIØEK0+
8.0
8.0
8.0
8.0
33.0 VOSP01+
13.0 PDTIX-
18.0 PIMAE-
19.0 PBUFE-
(74S10)
V6
(74S10)
V6
VIE
PEBEN+
4.0, 5.0
(74H04) 4 PLACES
V4
PSYRTA-
22.0, 32.0, 34.0, 35.0, 38.6
(74LS04)
J5
45
SYRT-I
R2
PSYRT+
V4
V4
PSYRTB-
12.0, 15.0, 19.0, 29.0, 31.0 38.0
V4
SYSTEM RESET, E-BUS ENABLE
CODE IDENT NO. 21101
SIZE C
DWG NO 9IC0569
REV L
SCALE
SHEET 6.0

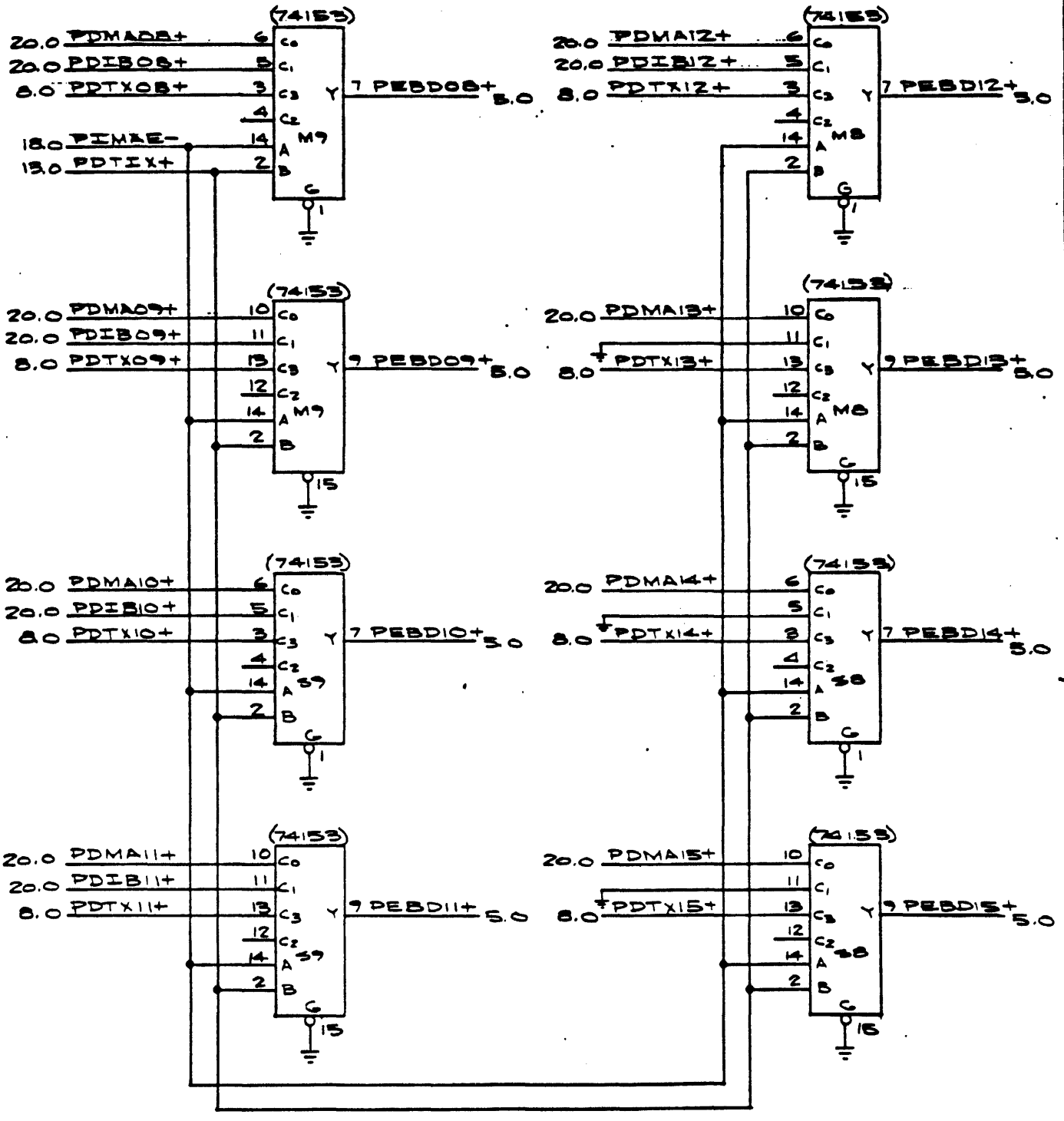


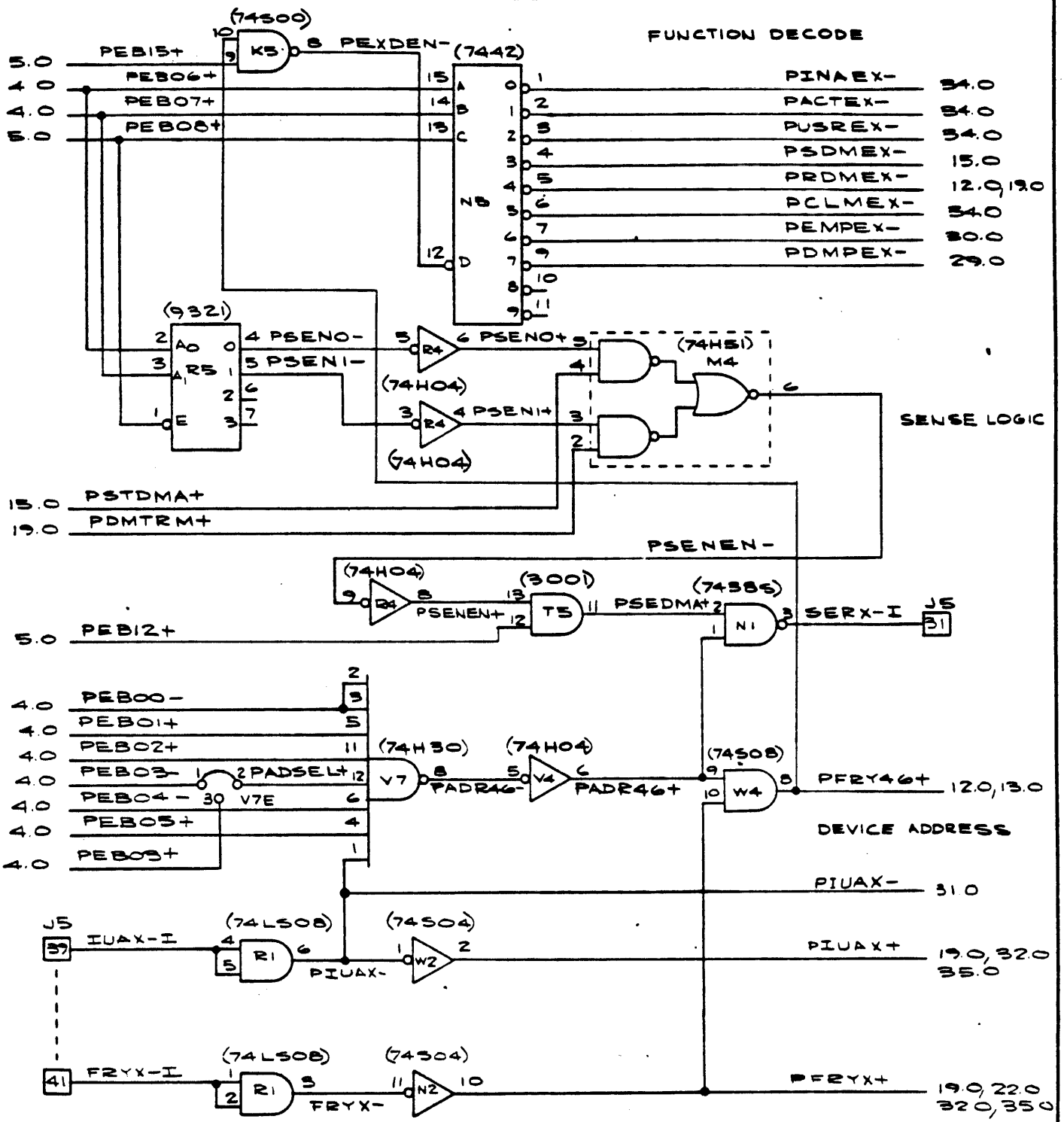
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100569	L
SCALE		SHEET 70	


4
3
2
1
D
C
B
A
(74153)
15.0 PEM53E+
33.0 PIADO8+
33.0 PUADO8+
14.0 PSIO+
14.0 PSI1+
7 PDTXO8+ 10.0
M6
14.0 PDMAØE+
33.0 PIADO9+
33.0 PUADO9+
9 PDTXO9+ 10.0
31.0 PDMAER+
33.0 PIAD10+
33.0 PUAD10+
7 PDTX10+ 10.0
31.0 PIØUER+
33.0 PIAD11+
33.0 PUAD11+
9 PDTX11+ 10.0
6.0 PIØEKO+
33.0 PIAD12+
33.0 PUAD12+
7 PDTX12+ 10.0
M7
6.0 PIØEK1+
33.0 PIAD13+
33.0 PUAD13+
9 PDTX13+ 10.0
6.0 PIØEK2+
33.0 PIAD14+
33.0 PUAD14+
7 PDTX14+ 10.0
S7
6.0 PIØEK3+
33.0 PIAD15+
33.0 PUAD15+
9 PDTX15+ 10.0
- INPUT DATA MUX BITS 8-11
INPUT DATA MUX BITS 12-15
21101
C
9100569

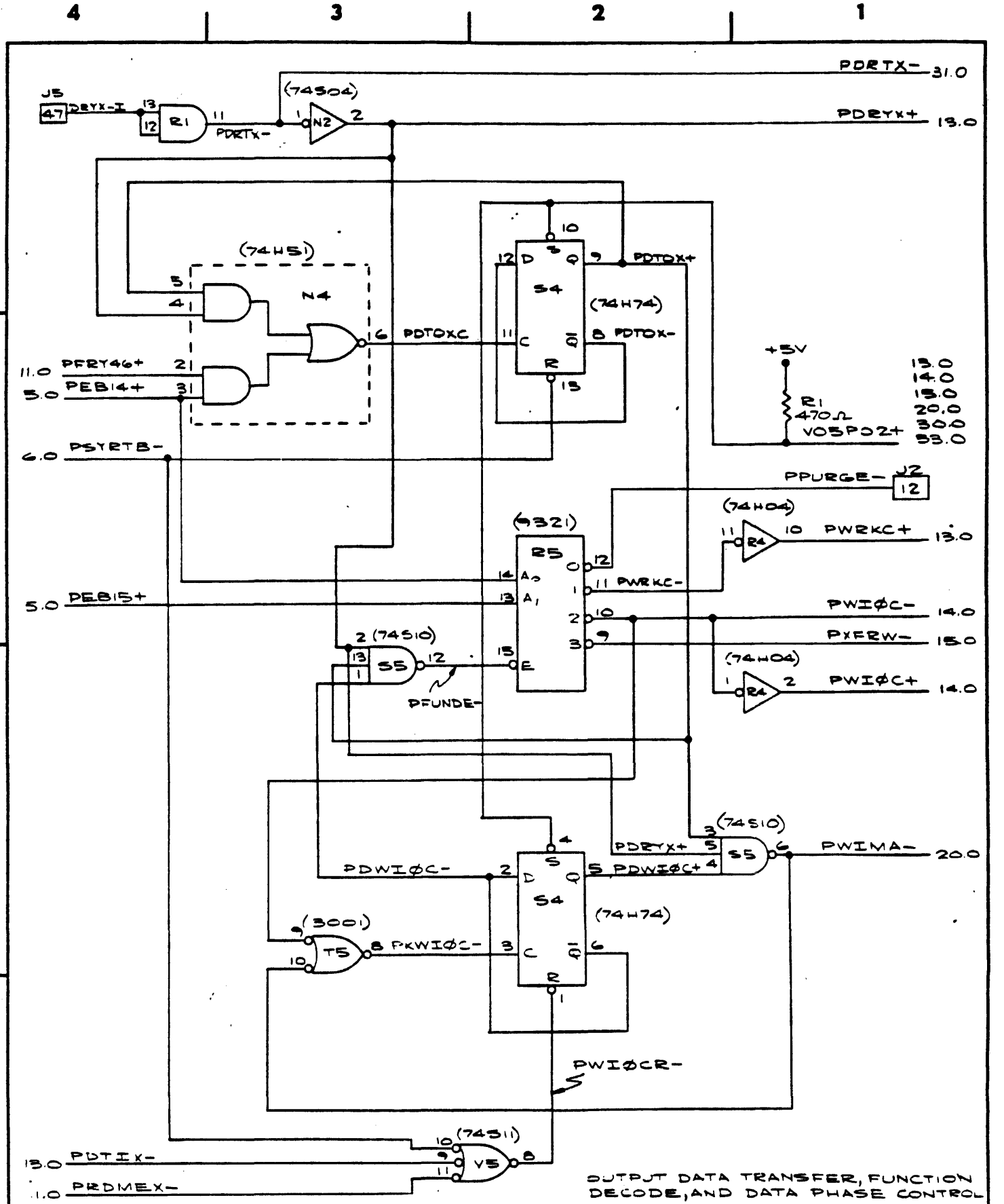


CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100569	L
SCALE		SHEET 90	


4
3
2
1
D
C
B
A
(74153)
M9
M8
20.0 PDMA08+
20.0 PDIB08+
8.0 PDTX08+
18.0 PIMAE-
15.0 PDTIX+
7 PEBD08+ 5.0
20.0 PDMA12+
20.0 PDIB12+
8.0 PDTX12+
7 PEBD12+ 5.0
20.0 PDMA09+
20.0 PDIB09+
8.0 PDTX09+
9 PEBD09+ 5.0
20.0 PDMA13+
8.0 PDTX13+
9 PEBD13+ 5.0
20.0 PDMA10+
20.0 PDIB10+
8.0 PDTX10+
7 PEBD10+ 5.0
20.0 PDMA14+
8.0 PDTX14+
7 PEBD14+ 5.0
20.0 PDMA11+
20.0 PDIB11+
8.0 PDTX11+
9 PEBD11+ 5.0
20.0 PDMA15+
8.0 PDTX15+
9 PEBD15+ 5.0
E-BUS MUX
BITS 8-11
E-BUS MUX
BITS 12-15
CODE IDENT NO. 21101
SIZE C
DWG NO 9100569
REV L
SCALE
SHEET 10.0

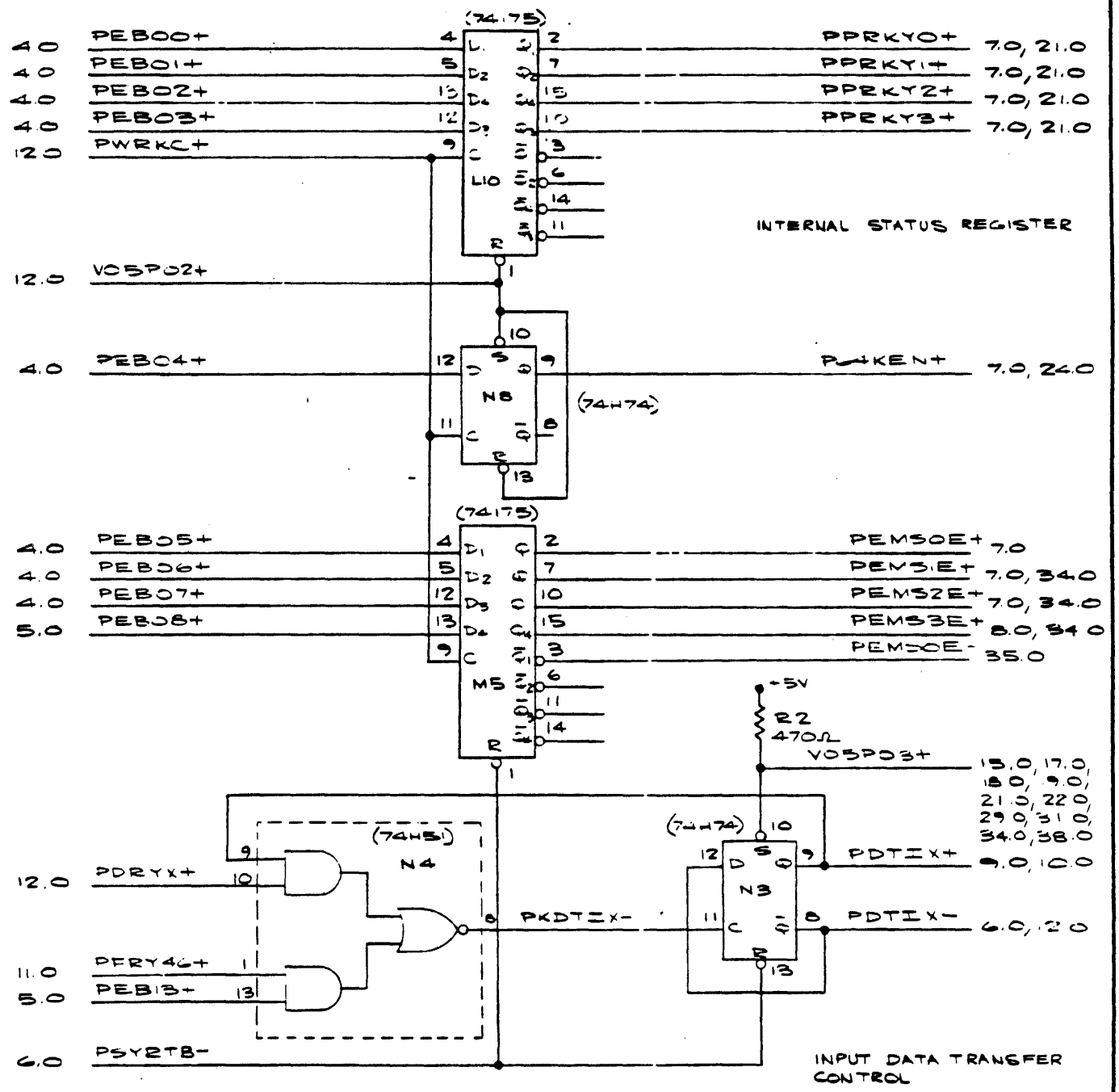


CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100569	L
SCALE			SHEET 11.0

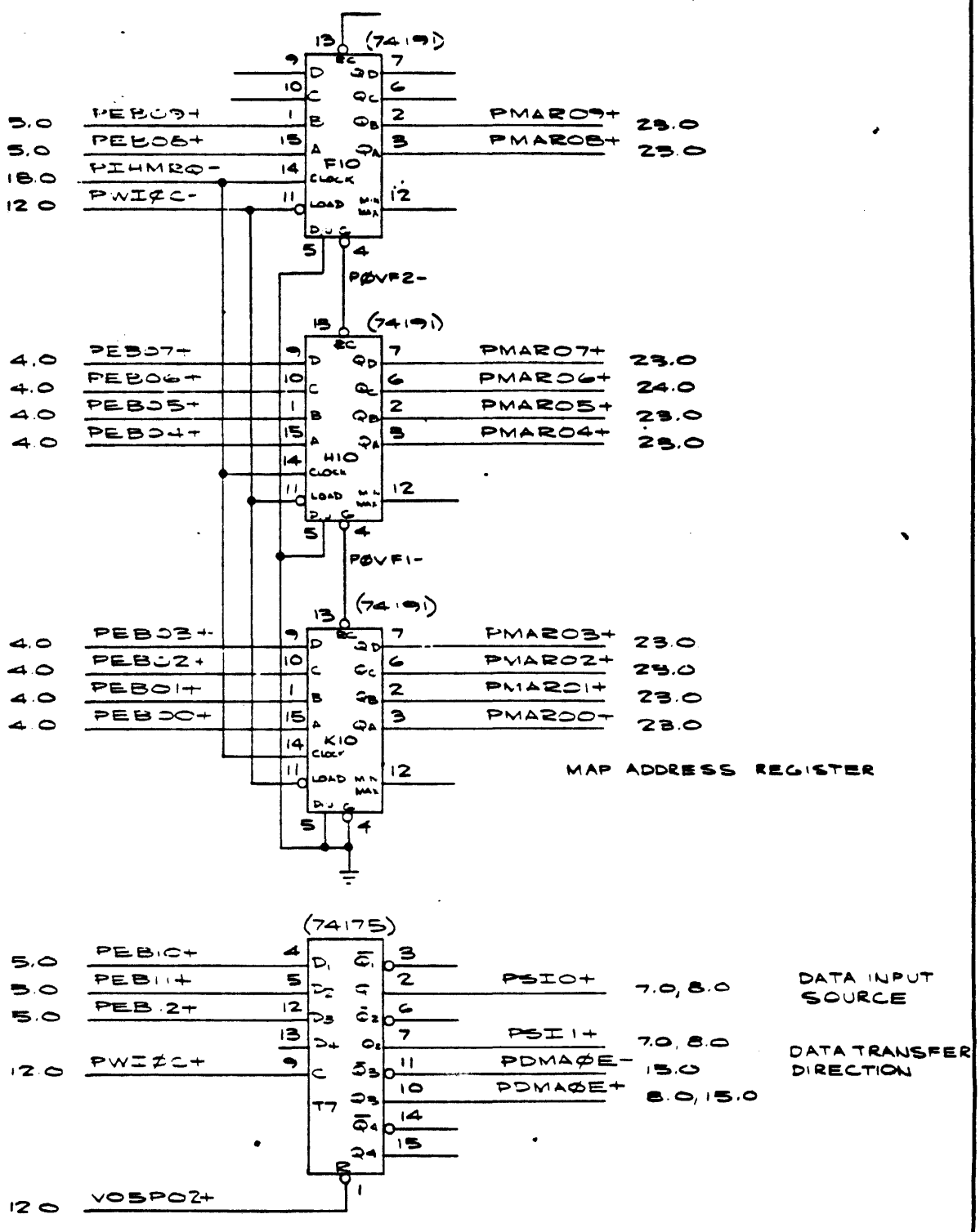


OUTPUT DATA TRANSFER, FUNCTION DECODE, AND DATA PHASE CONTROL

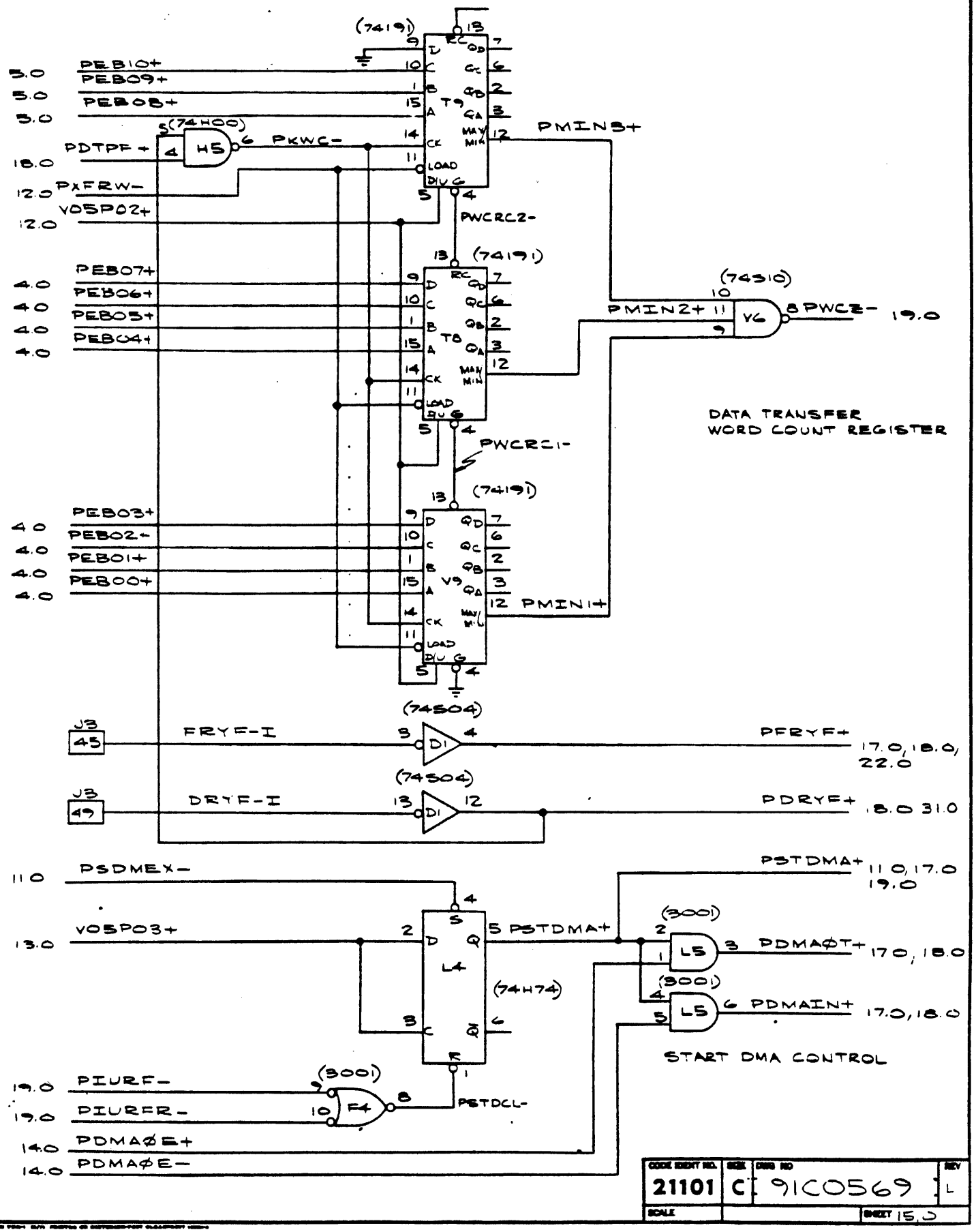
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0569	L
SCALE		SHEET 12.0	

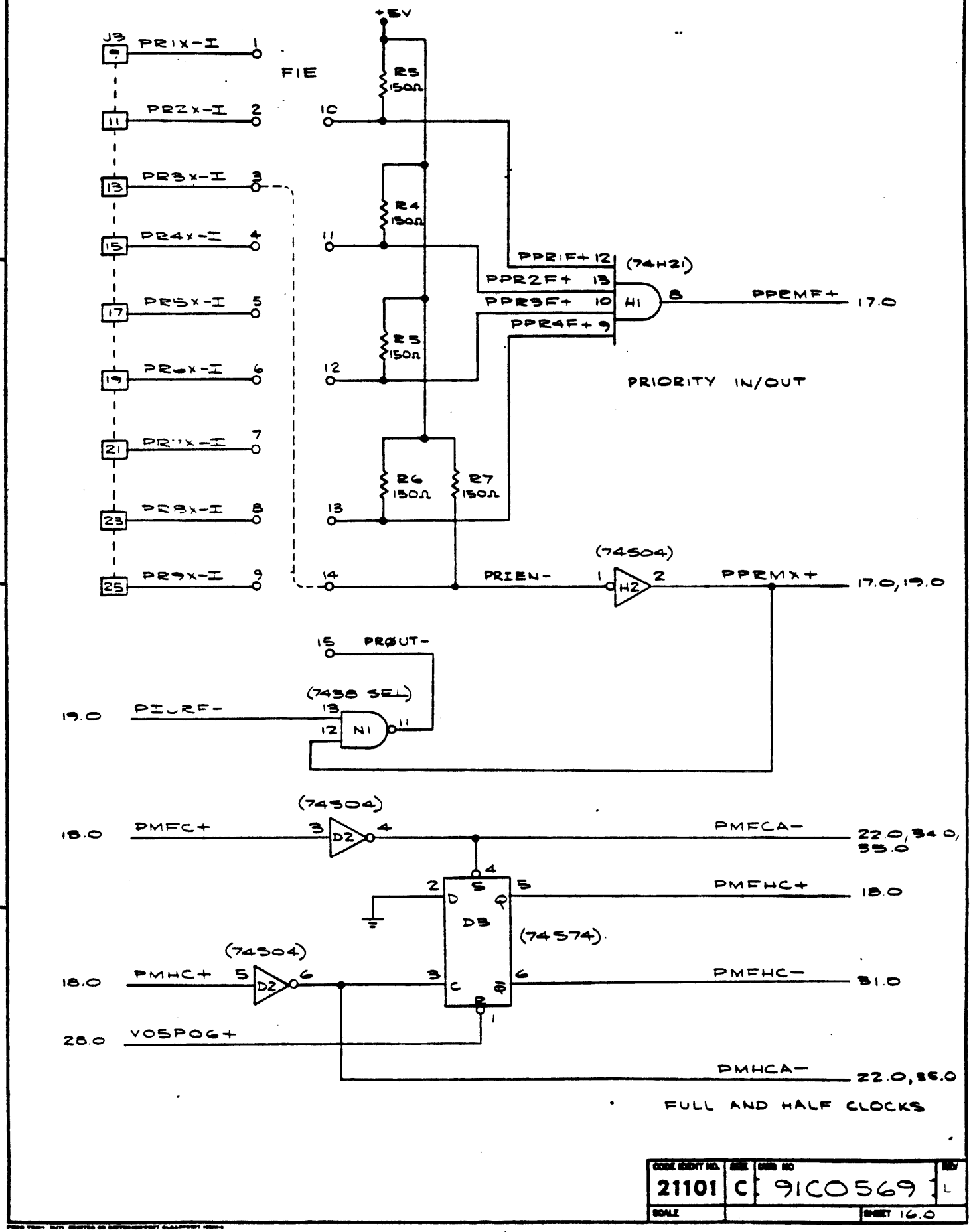


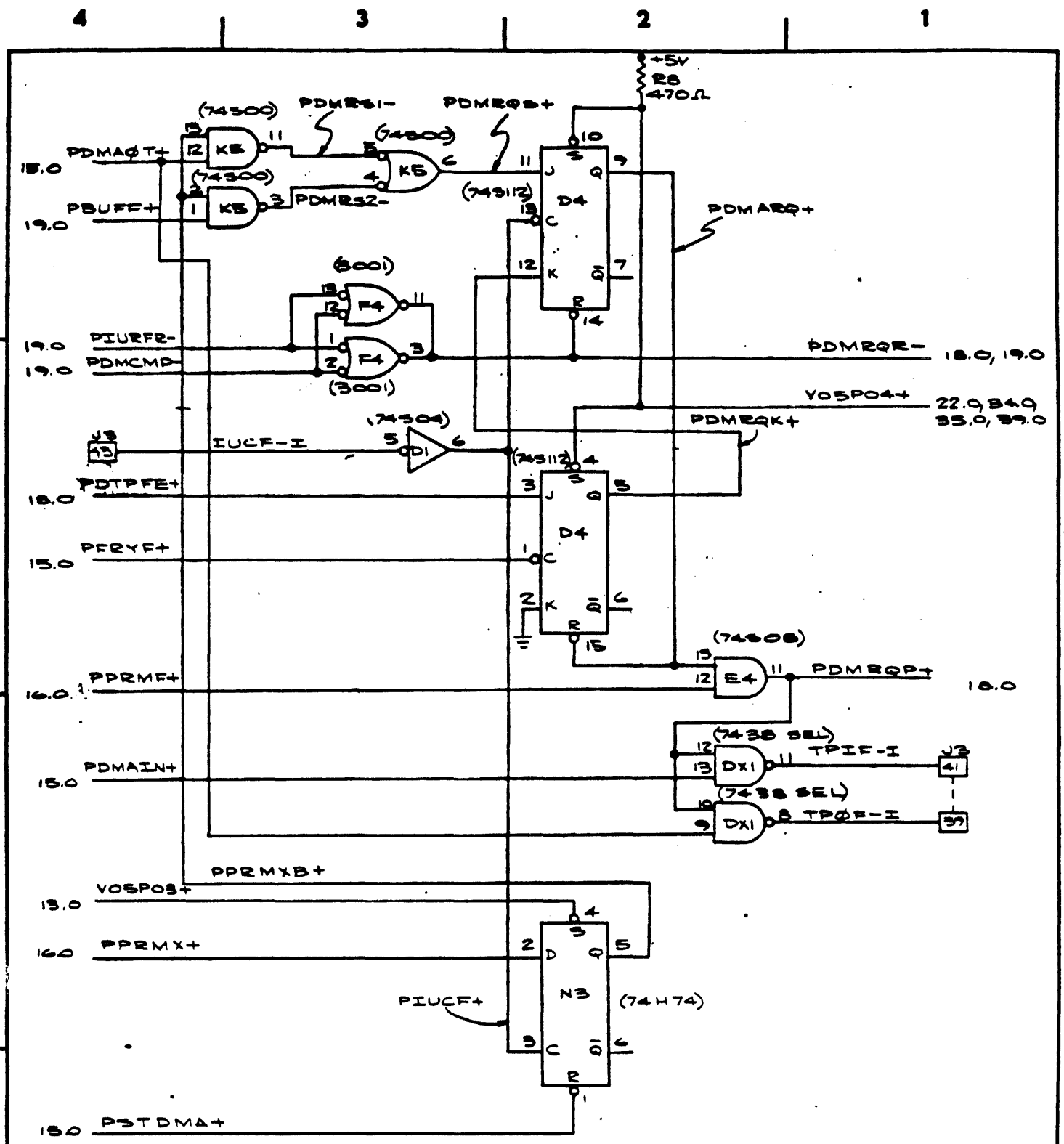
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100569	L
SCALE		SHEET 130	



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100569	L
SCALE		SHEET 14.0	

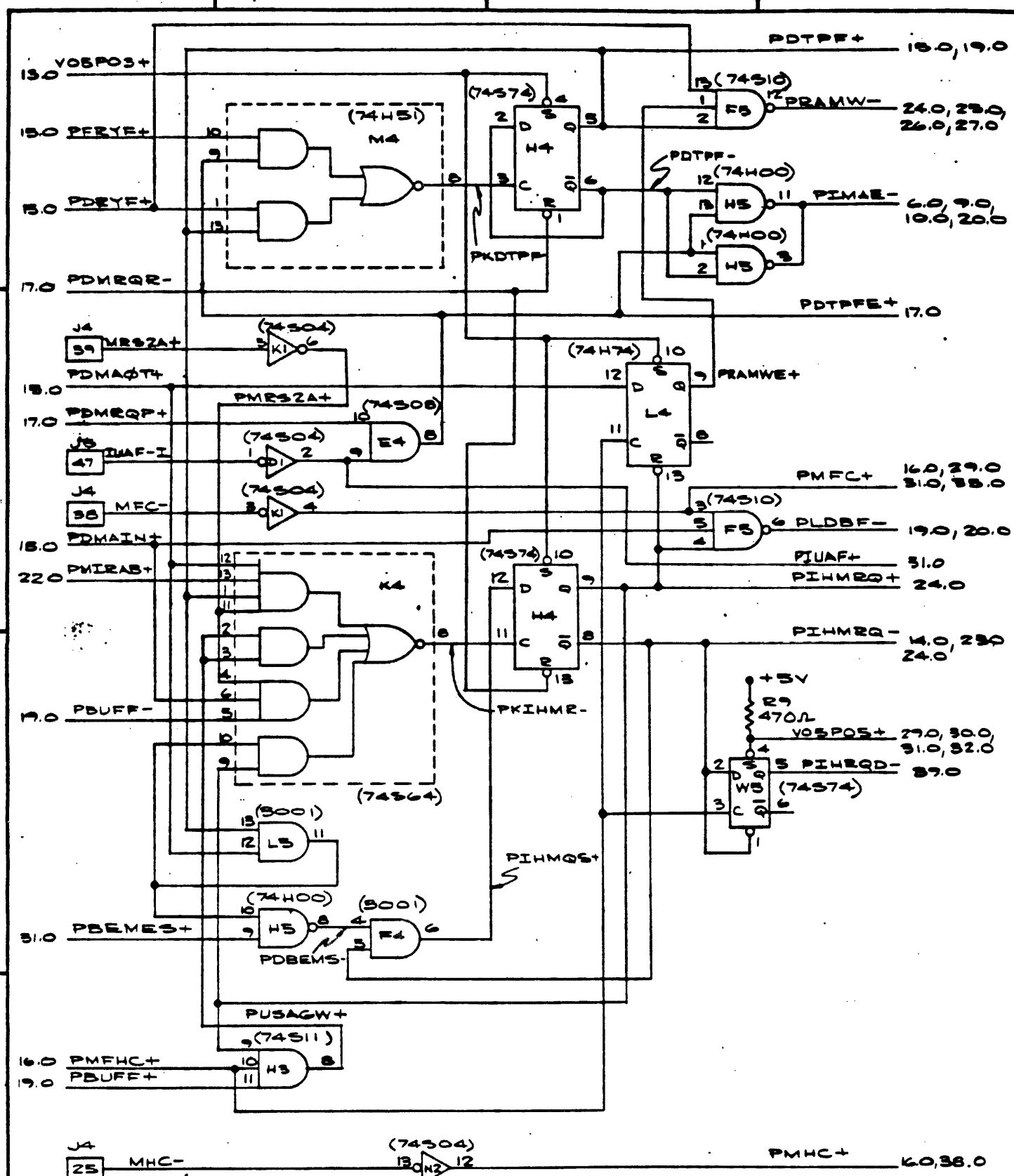

4
3
2
1
D
C
B
A
(7419)
T9
PEB10+
PEB09+
PEB08+
5.0
5.0
5.0
(74H00)
H5
PDTPF+
18.0
PKWC-
12.0 PXFRW-
12.0 VO5PO2+
PMIN3+
PWCRC2-
(74191)
T8
PEB07+
PEB06+
PEB05+
PEB04+
4.0
4.0
4.0
4.0
(74S10)
Y6
PMIN2+
PWCE-
19.0
DATA TRANSFER
WORD COUNT REGISTER
PWCRC1-
(74191)
V9
PEB03+
PEB02+
PEB01+
PEB00+
4.0
4.0
4.0
4.0
PMIN1+
(74S04)
J3
45
FRYF-I
D1
PFRYF+
17.0, 18.0, 22.0
(74S04)
J3
49
DRYF-I
D1
PDRYF+
18.0 31.0
11.0 PSDMEX-
PSTDMA+
11.0, 17.0 19.0
13.0 VO5PO3+
L4
(74H74)
PSTDMA+
(3001)
L5
PDMAØT+
17.0, 18.0
(3001)
L5
PDMAIN+
17.0, 18.0
START DMA CONTROL
19.0 PIURF-
19.0 PIURFR-
(3001)
F4
PSTDCL-
14.0 PDMAØE+
14.0 PDMAØE-
CODE IDENT NO. 21101
SIZE C
DWG NO 9100569
REV L
SCALE
SHEET 15.5


4
3
2
1
D
C
B
A
+5V
J3
PR1X-I
PR2X-I
PR3X-I
PR4X-I
PR5X-I
PR6X-I
PR7X-I
PR8X-I
PR9X-I
FIE
R3 150Ω
R4 150Ω
R5 150Ω
R6 150Ω
R7 150Ω
PPR1F+
PPR2F+
PPR3F+
PPR4F+
(74H21)
H1
PPEMF+
17.0
PRIORITY IN/OUT
(74504)
H2
PRIEN-
PPRMX+
17.0,19.0
PROUT-
(7438 SEL)
N1
PIURF-
19.0
PMFC+
18.0
D2
PMFCA-
22.0,34.0,55.0
D3
(74574)
PMFHC+
18.0
PMHC+
PMFHC-
31.0
VOSPOG+
28.0
PMHCA-
22.0,86.0
FULL AND HALF CLOCKS
21101
C
9100569
L
SCALE
SHEET 16.0



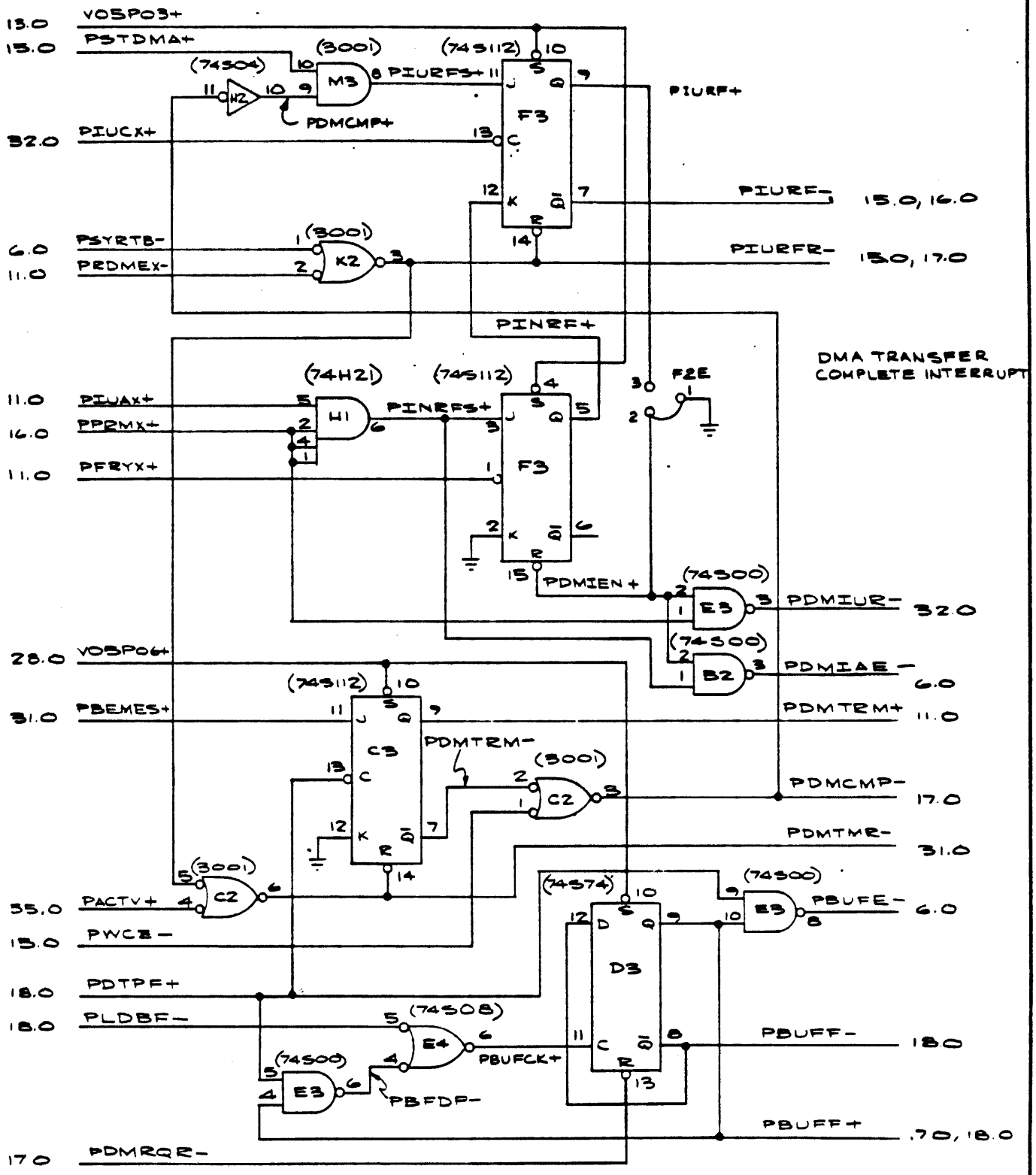
HIGH SPEED DMA REQUEST

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9C0569	L
SCALE			SHEET 17.0

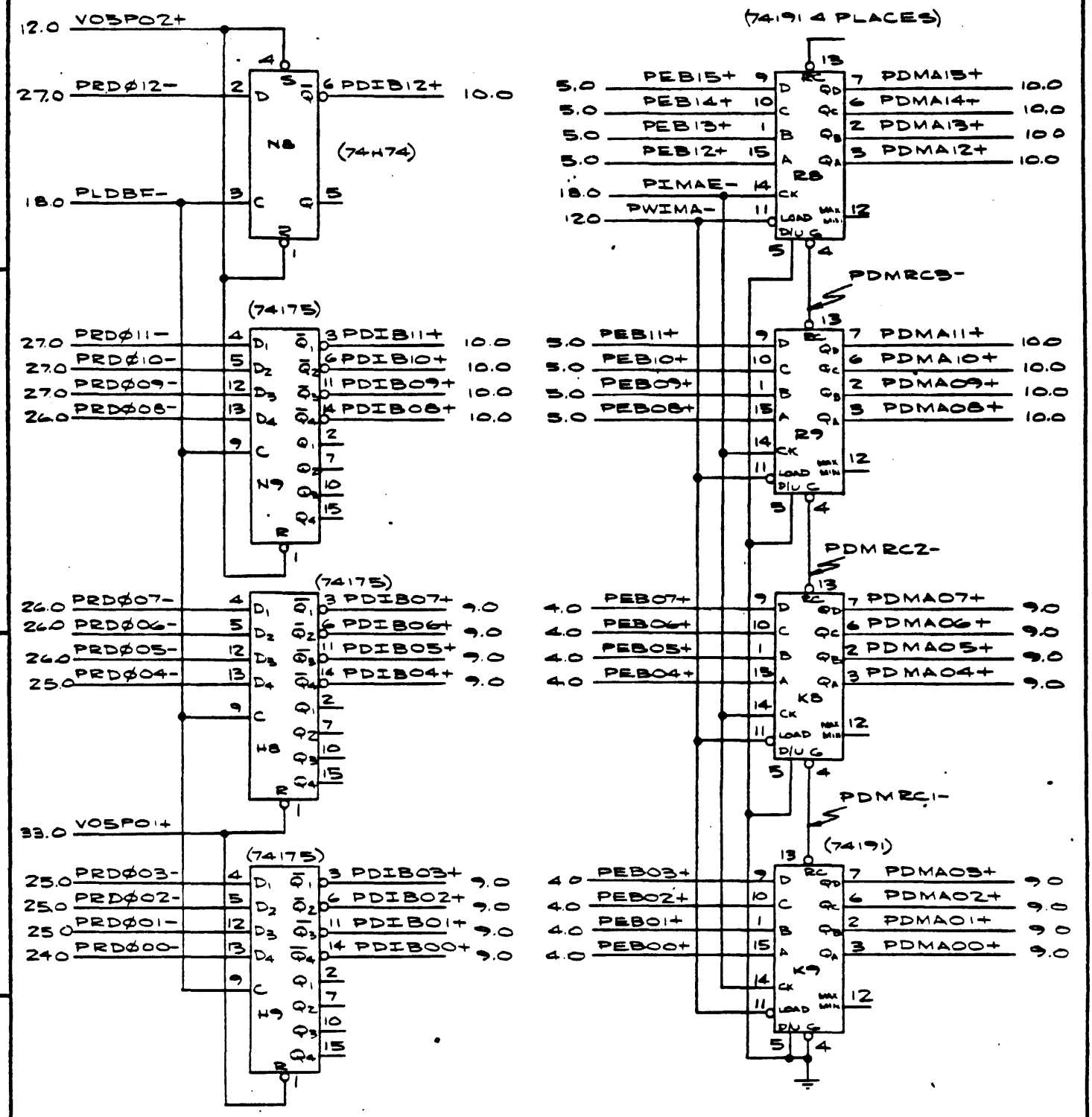


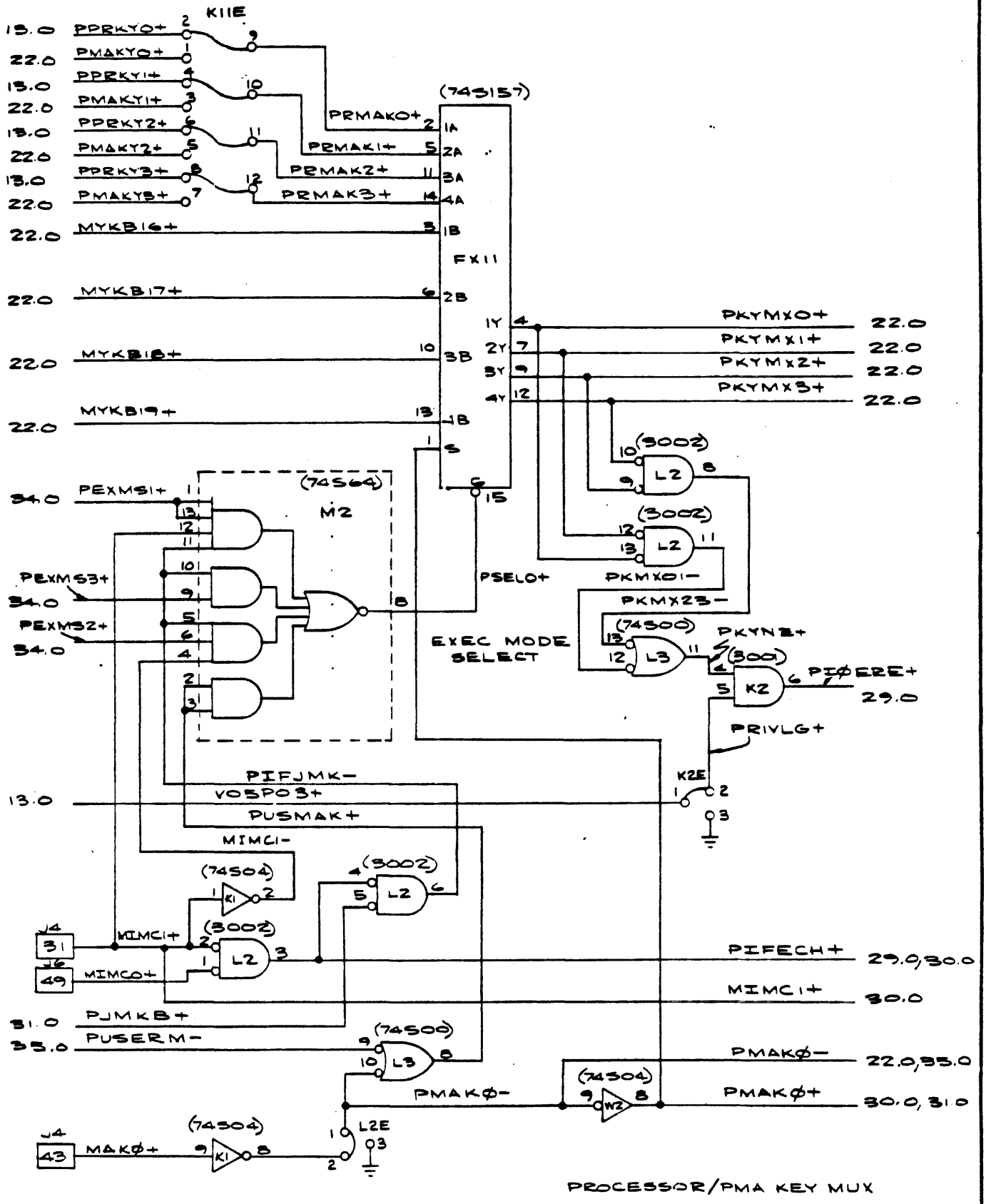
DMA DATA PHASE CONTROL
MEMORY REQUEST INPUT INHIBIT
RAM WRITE ENABLE

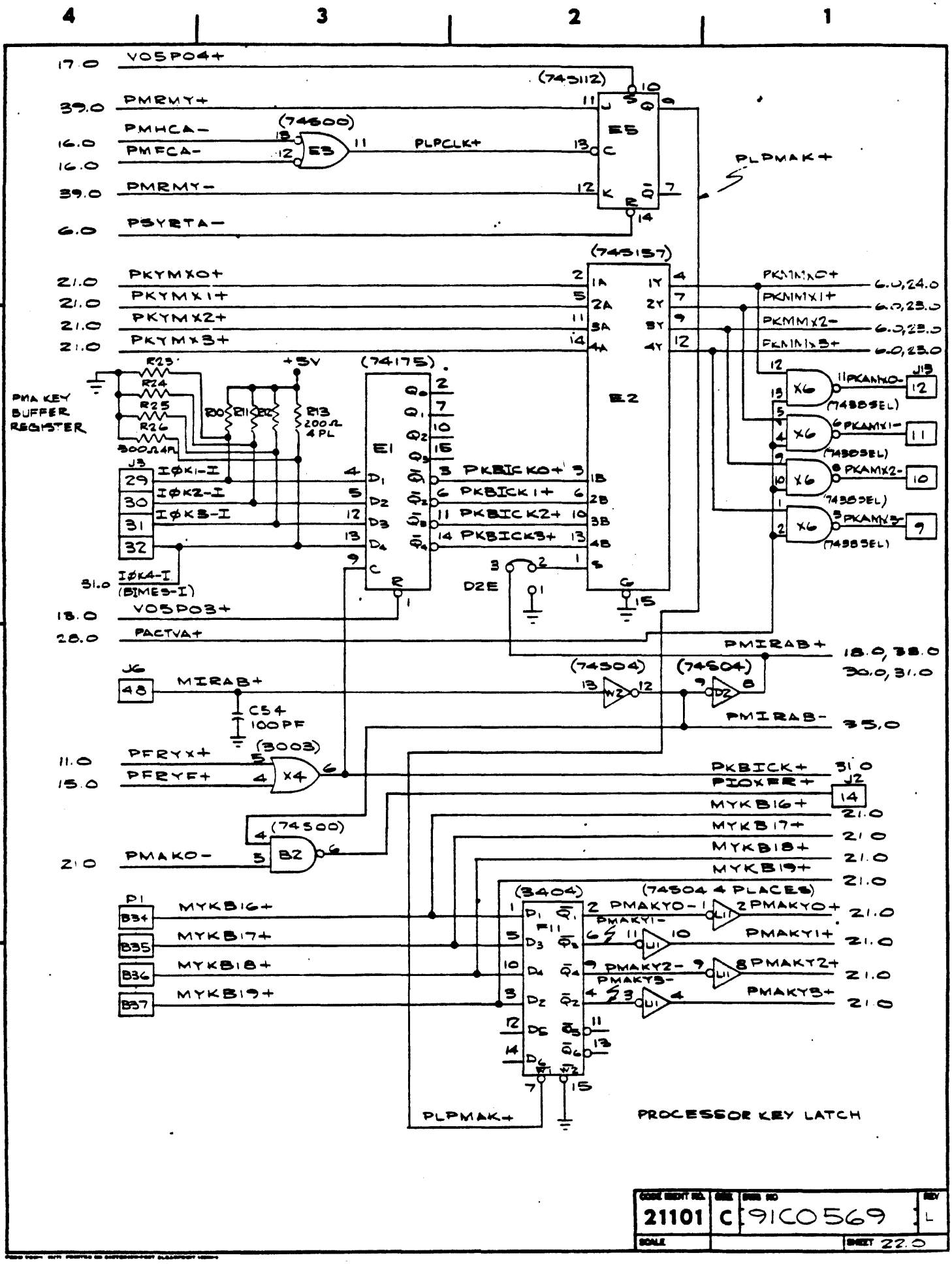
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0569	L
SCALE		SHEET 18.0	

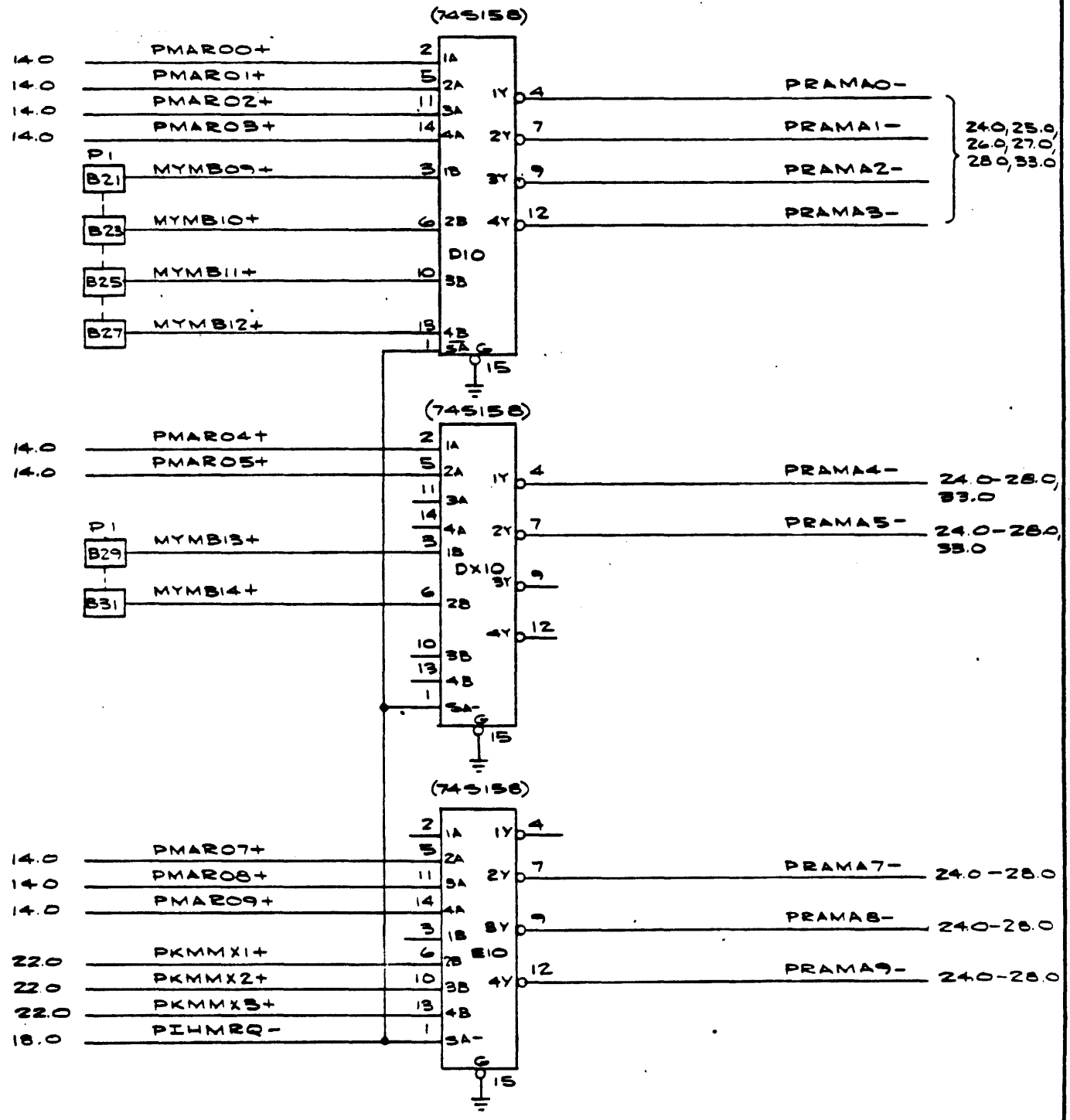


CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100569	L
SCALE			SHEET 19 C


4
3
2
1
D
C
B
A
12.0 VO5PO2+
27.0 PRDØ12-
18.0 PLDBF-
N8
(74H74)
6 PDIB12+ 10.0
(74175)
27.0 PRDØ11-
27.0 PRDØ10-
27.0 PRDØ09-
26.0 PRDØ08-
3 PDIB11+ 10.0
6 PDIB10+ 10.0
11 PDIB09+ 10.0
14 PDIB08+ 10.0
N9
26.0 PRDØ07-
26.0 PRDØ06-
26.0 PRDØ05-
25.0 PRDØ04-
3 PDIB07+ 9.0
6 PDIB06+ 9.0
11 PDIB05+ 9.0
14 PDIB04+ 9.0
H8
33.0 VO5PO1+
25.0 PRDØ03-
25.0 PRDØ02-
25 PRDØ01-
24.0 PRDØ00-
3 PDIB03+ 9.0
6 PDIB02+ 9.0
11 PDIB01+ 9.0
14 PDIB00+ 9.0
H9
DMA INPUT BUFFER
(74191 4 PLACES)
5.0 PEB15+
5.0 PEB14+
5.0 PEB13+
5.0 PEB12+
18.0 PIMAE-
12.0 PWIMA-
7 PDMA15+ 10.0
6 PDMA14+ 10.0
2 PDMA13+ 10.0
3 PDMA12+ 10.0
R8
PDMRC3-
5.0 PEB11+
5.0 PEB10+
5.0 PEB09+
5.0 PEB08+
7 PDMA11+ 10.0
6 PDMA10+ 10.0
2 PDMA09+ 10.0
3 PDMA08+ 10.0
R9
PDMRC2-
4.0 PEB07+
4.0 PEB06+
4.0 PEB05+
4.0 PEB04+
7 PDMA07+ 9.0
6 PDMA06+ 9.0
2 PDMA05+ 9.0
3 PDMA04+ 9.0
K8
PDMRC1-
(74191)
4.0 PEB03+
4.0 PEB02+
4.0 PEB01+
4.0 PEB00+
7 PDMA03+ 9.0
6 PDMA02+ 9.0
2 PDMA01+ 9.0
3 PDMA00+ 9.0
K9
DMA MEMORY ADDRESS REGISTER
CODE IDENT NO. 21101
SIZE C
DWG NO 9100569
REV L
SCALE
SHEET 20.0

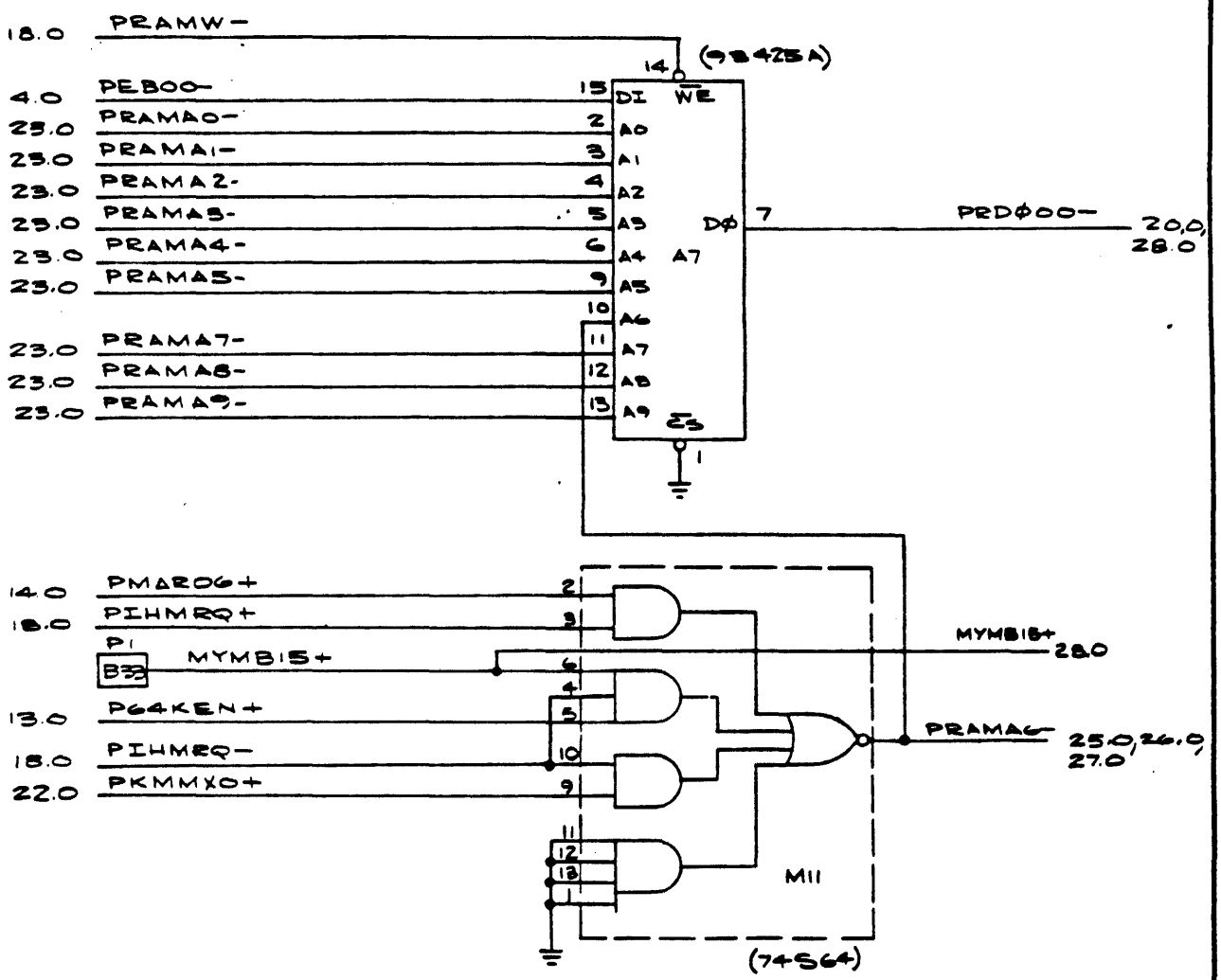

4
3
2
1
D
C
B
A
K11E
(74S157)
15.0 PPRKY0+
22.0 PMAKY0+
15.0 PPRKY1+
22.0 PMAKY1+
15.0 PPRKY2+
22.0 PMAKY2+
15.0 PPRKY3+
22.0 PMAKY3+
PRMAK0+
PRMAK1+
PRMAK2+
PRMAK3+
1A
2A
3A
4A
22.0 MYKB16+
22.0 MYKB17+
22.0 MYKB18+
22.0 MYKB19+
1B
2B
3B
4B
FX11
1Y PKYMX0+ 22.0
2Y PKYMX1+ 22.0
3Y PKYMX2+ 22.0
4Y PKYMX3+ 22.0
(74S64)
M2
34.0 PEXMS1+
PEXMS3+ 34.0
PEXMS2+ 34.0
PSELO+
EXEC MODE SELECT
(3002)
L2
PKMX01−
PKMX23−
(74S00)
L3
PKYN3+
(300)
K2
PIΦERE+ 29.0
PRIVLG+
K2E
13.0 PIFJMK−
VOSPO3+
PUSMAK+
MIMCI−
(74S04)
K1
MIMCI+
MIMCO+
J4 31
J6 49
PIFECH+ 29.0,30.0
MIMCI+ 30.0
31.0 PJMKB+
35.0 PUSERM−
PMAKΦ− 22.0,35.0
PMAKΦ+ 30.0,31.0
W2
J4 43 MAKΦ+
L2E
PROCESSOR/PMA KEY MUX
CODE IDENT NO. 21101
SIZE C
DWG NO 9100569
REV
SCALE
SHEET 21.0


4
3
2
1
D
C
B
A
17.0 VO5PO4+
39.0 PMRMY+
PMHCA-
16.0 PMFCA-
16.0
39.0 PMRMY-
6.0 PSYRTA-
(74500)
E3
PLPCLK+
(74S112)
E5
PLPMAK+
(74S157)
E2
21.0 PKYMX0+
21.0 PKYMX1+
21.0 PKYMX2+
21.0 PKYMX3+
PKMMX0+ 6.0,24.0
PKMMX1+ 6.0,23.0
PKMMX2- 6.0,23.0
PKMMX3+ 6.0,23.0
(74175)
E1
PMA KEY BUFFER REGISTER
R23
R24
R25
R26
300Ω 4PL
R10 R11 R12
R13 200Ω 4 PL
+5V
J3
29 IØK1-I
30 IØK2-I
31 IØK3-I
32
31.0 IØK4-I (BIMES-I)
PKBICK0+
PKBICK1+
PKBICK2+
PKBICK3+
D2E
X6 (74S85EL)
11 PKAMX0- J13 12
6 PKAMX1- 11
8 PKAMX2- 10
3 PKAMX3- 9
18.0 VO5PO3+
28.0 PACTVA+
PMIRAB+ 18.0, 38.0 30.0, 31.0
PMIRAB- 35.0
(74504)
(74S04)
J6
48 MIRAB+
C54 100PF
11.0 PFRYX+
15.0 PFRYF+
(3003)
X4
PKBICK+ 31.0
PIOKER+ J2 14
MYKB16+ 21.0
MYKB17+ 21.0
MYKB18+ 21.0
MYKB19+ 21.0
(74500)
B2
2.0 PMAKO-
(3404)
(74504 4 PLACES)
F11
P1
B34 MYKB16+
B35 MYKB17+
B36 MYKB18+
B37 MYKB19+
PMAKY0- 1
PMAKY0+ 2 21.0
PMAKY1- 6
PMAKY1+ 10 21.0
PMAKY2- 9
PMAKY2+ 8 21.0
PMAKY3- 4
PMAKY3+ 4 21.0
PLPMAK+
PROCESSOR KEY LATCH
21101
C
9100569
L
SCALE
SHEET 22.0



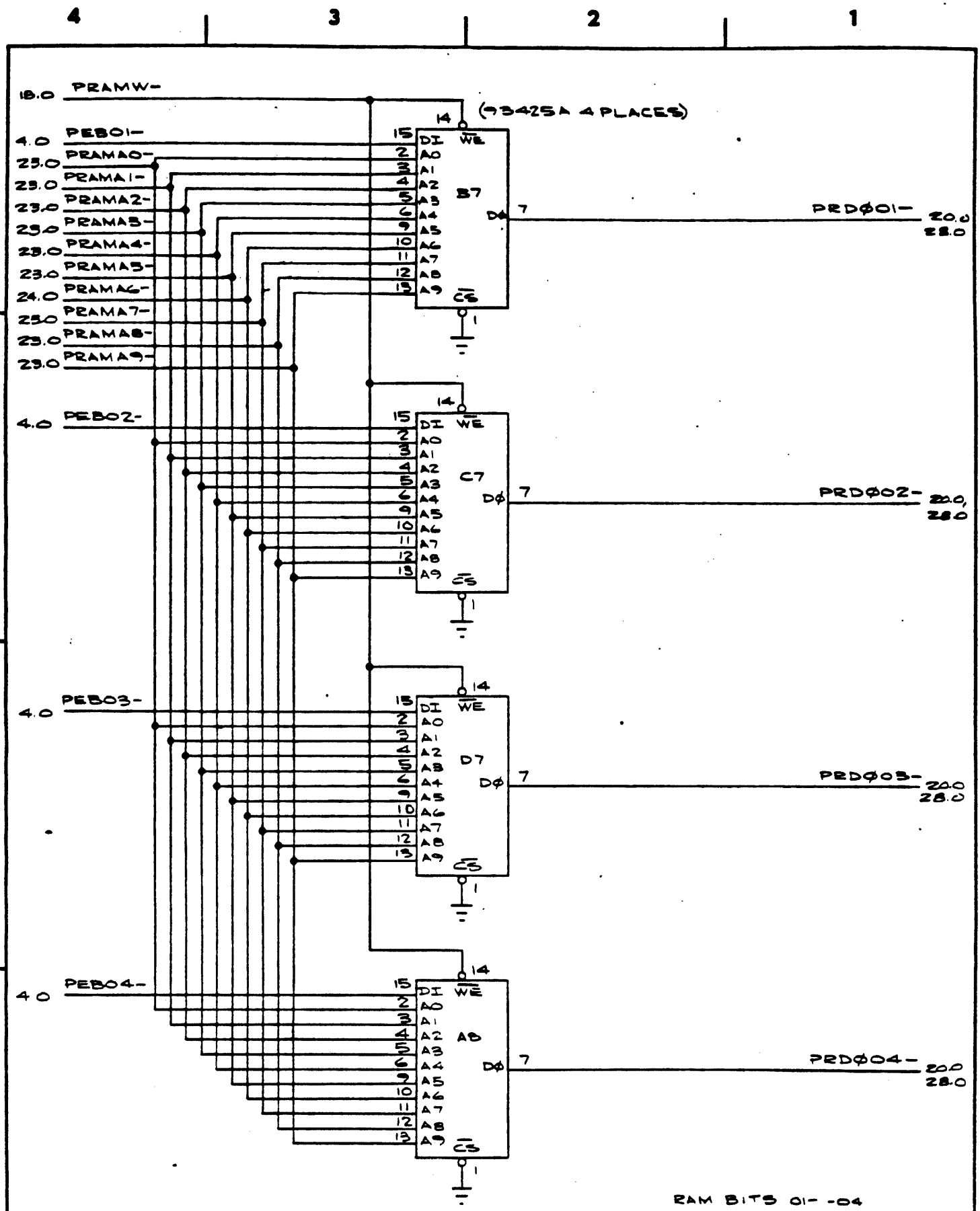
RAM ADDRESS MUX
BITS 0-5, 7-9

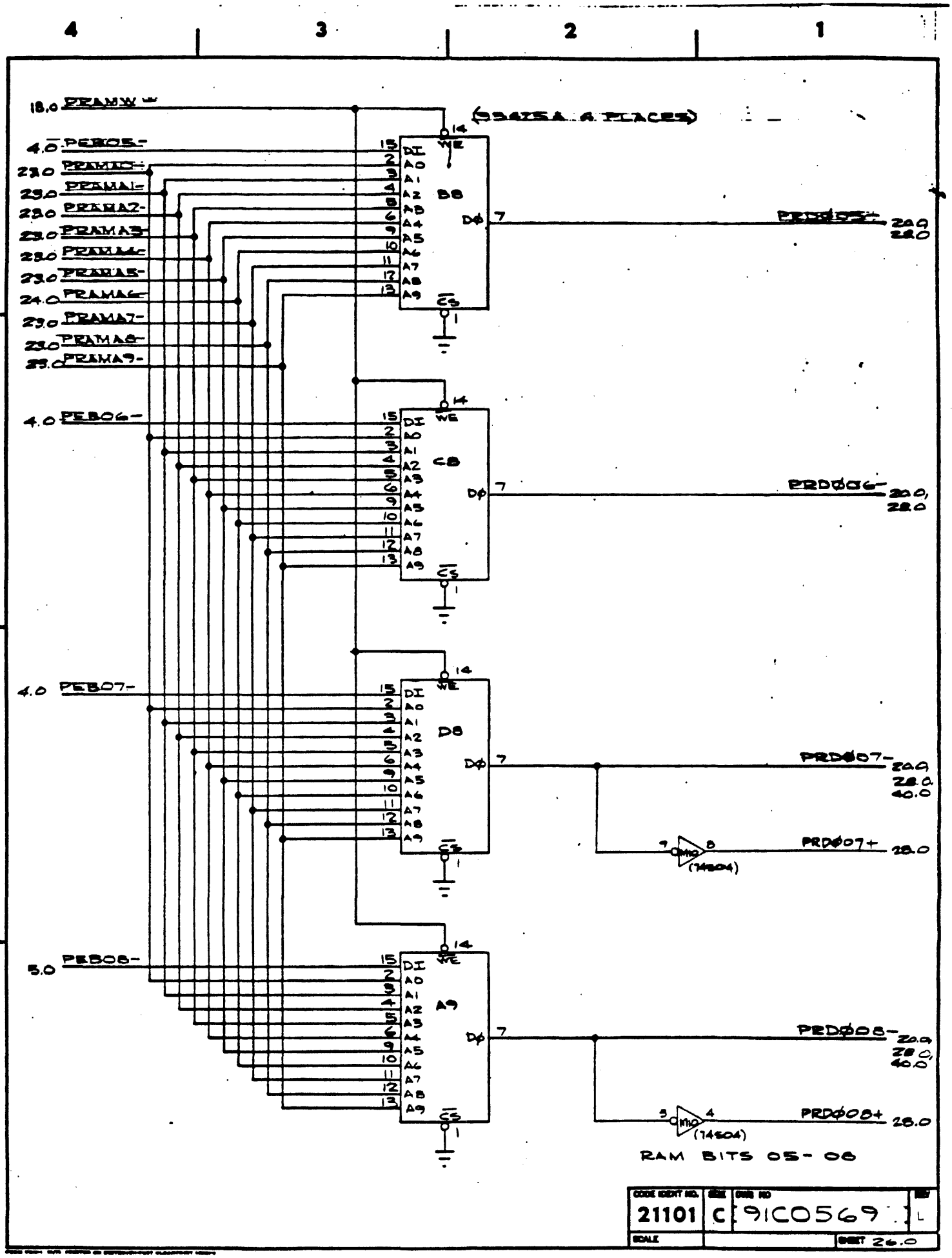
21101	C	9100569	L
SCALE		SHEET 23.0	



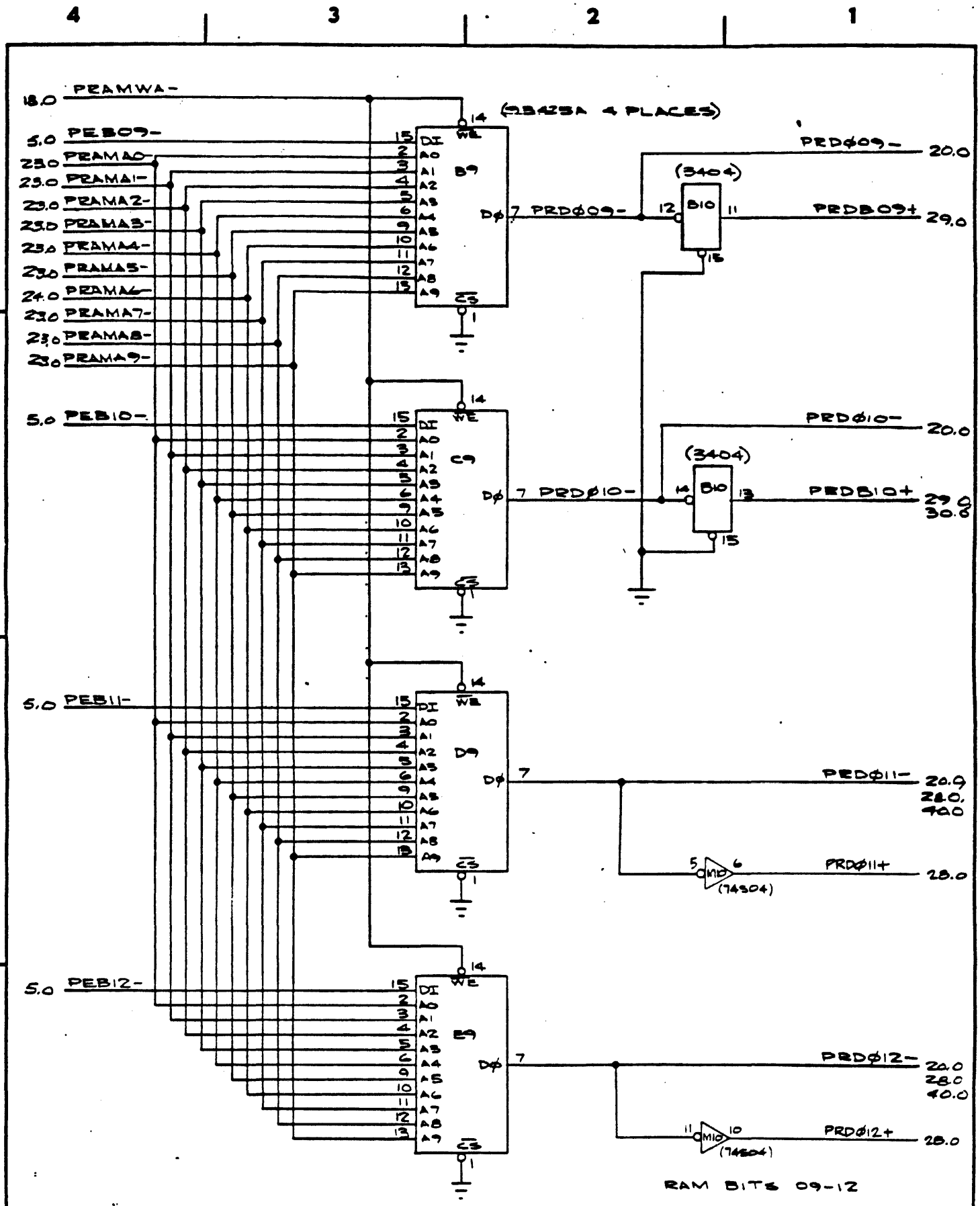
BIT 0 RAM
RAM ADDRESS MUX
BIT 6

21101	C	9105691	L
SCALE			SHEET 24.0

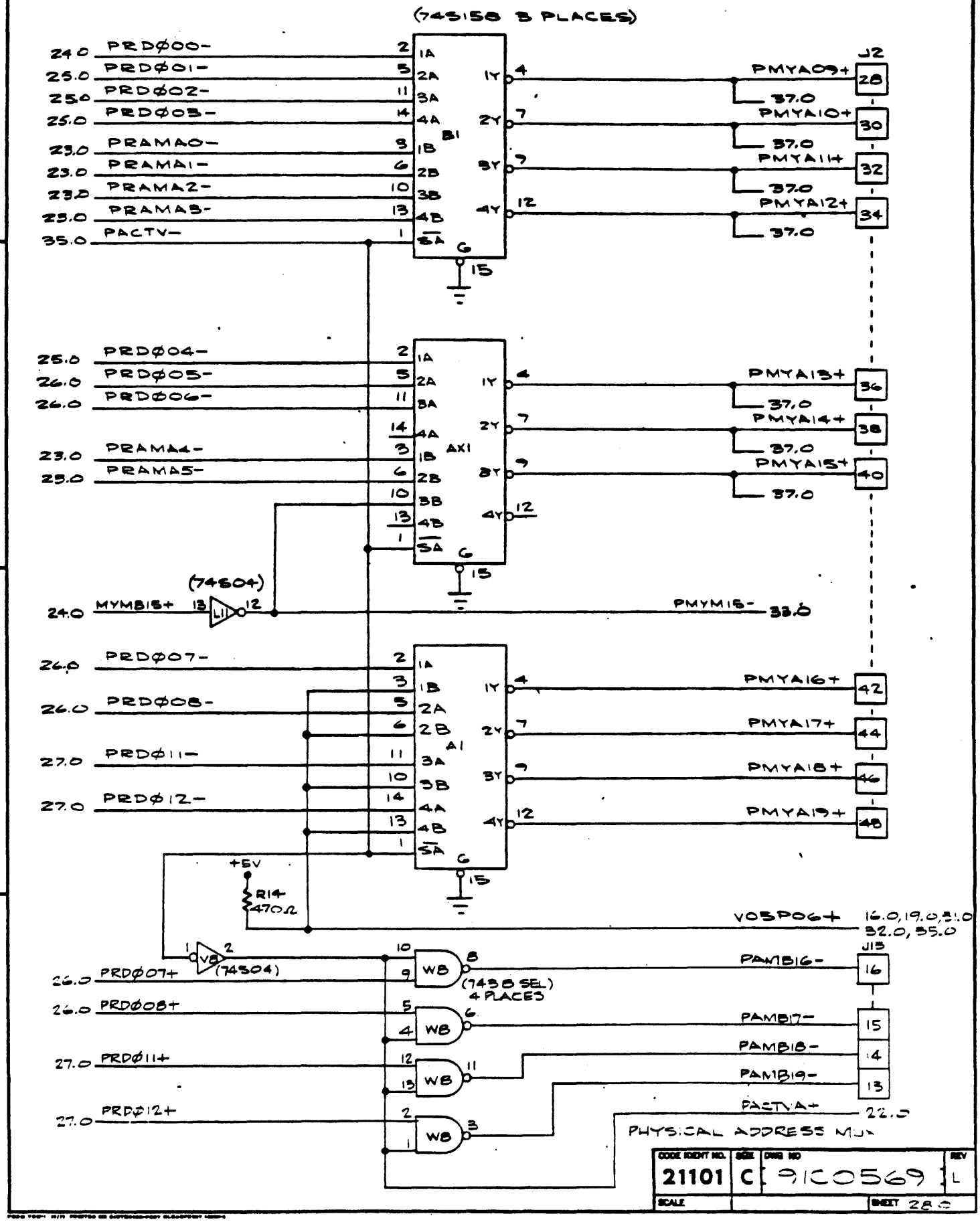

4
3
2
1
D
C
B
A
18.0 PRAMW-
(93425A 4 PLACES)
4.0 PEB01-
PRAMA0-
25.0
PRAMA1-
25.0
PRAMA2-
25.0
PRAMA3-
25.0
PRAMA4-
29.0
PRAMA5-
23.0
PRAMA6-
24.0
PRAMA7-
25.0
PRAMA8-
23.0
PRAMA9-
29.0
B7
PRDØ01-
20.0
28.0
4.0 PEB02-
C7
PRDØ02-
20.0,
28.0
4.0 PEB03-
D7
PRDØ03-
20.0
28.0
4.0 PEB04-
A8
PRDØ04-
20.0
28.0
DI
WE
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
CS
DØ
14
15
7
1
RAM BITS 01- -04
CODE IDENT NO. 21101
SIZE C
DWG NO 9100569
REV L
SCALE
SHEET 250



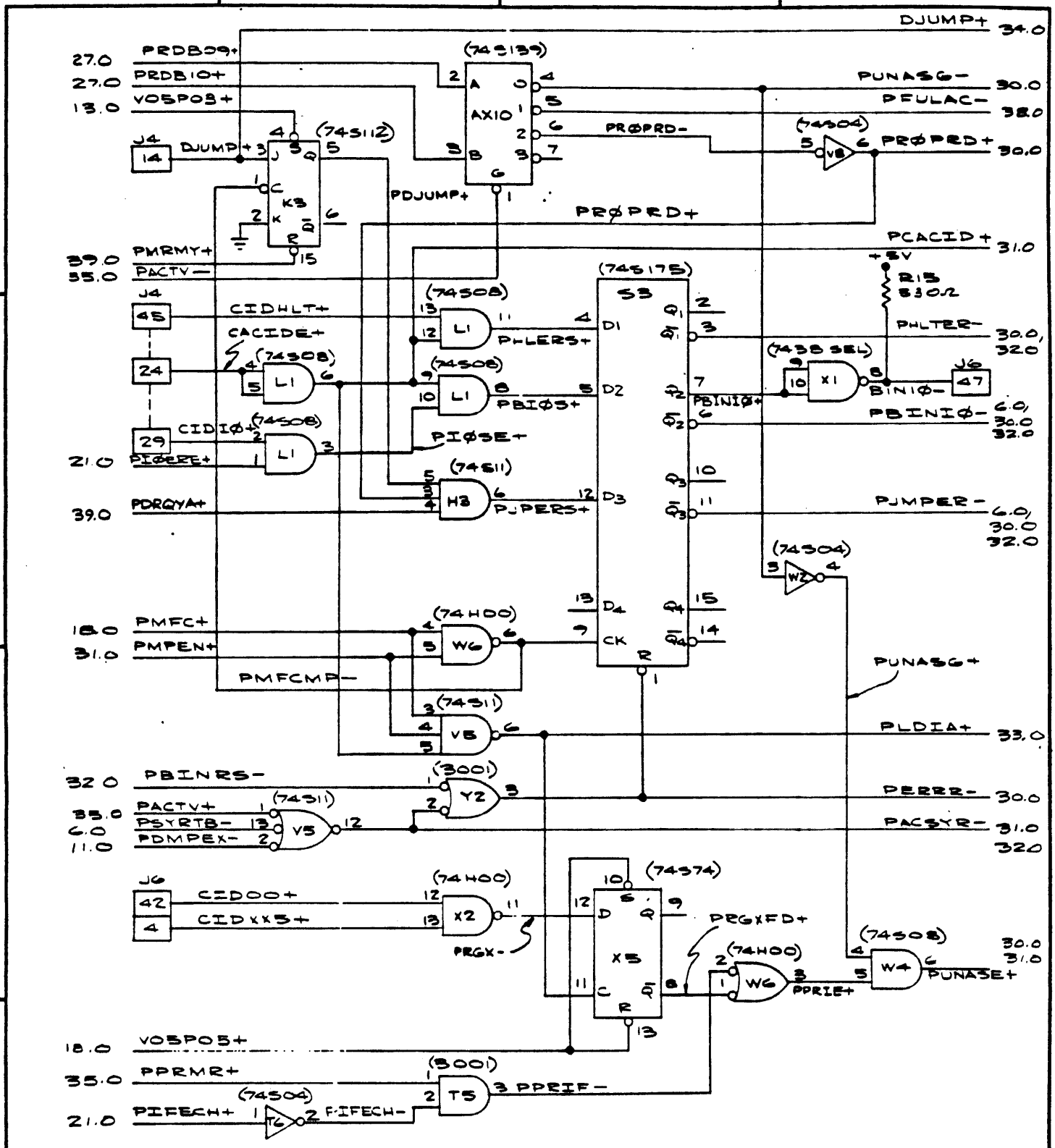
4
3
2
1
D
C
B
A
18.0 PRAMW
4.0 PEB05-
23.0 PRAMA0-
23.0 PRAMA1-
23.0 PRAMA2-
23.0 PRAMA3-
23.0 PRAMA4-
23.0 PRAMA5-
24.0 PRAMA6-
23.0 PRAMA7-
23.0 PRAMA8-
23.0 PRAMA9-
4.0 PEB06-
4.0 PEB07-
5.0 PEB08-
B8
C8
D8
A9
DI
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
WE
CS
DØ
PRDØ05-
PRDØ06-
PRDØ07-
PRDØ07+
PRDØ08-
PRDØ08+
20.0
28.0
40.0
M10
(74S04)
RAM BITS 05-08
CODE IDENT NO.
21101
SIZE
C
DWG NO
91C0569
REV
L
SCALE
SHEET 26.0



4
3
2
1
D
C
B
A
18.0 PRAMWA-
5.0 PEB09-
23.0 PRAMA0-
23.0 PRAMA1-
23.0 PRAMA2-
23.0 PRAMA3-
23.0 PRAMA4-
23.0 PRAMA5-
24.0 PRAMA6-
23.0 PRAMA7-
23.0 PRAMA8-
23.0 PRAMA9-
5.0 PEB10-
5.0 PEB11-
5.0 PEB12-
(93425A 4 PLACES)
B9
C9
D9
E9
DI
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
WE
CS
DØ
PRDØ09-
PRDØ10-
PRDØ11-
PRDØ12-
(3404)
B10
M10
(74S04)
PRDØ09- 20.0
PRDB09+ 29.0
PRDØ10- 20.0
PRDB10+ 29.0 30.0
PRDØ11- 20.0 28.0 40.0
PRDØ11+ 28.0
PRDØ12- 20.0 28.0 40.0
PRDØ12+ 28.0
RAM BITS 09-12
CODE IDENT NO. 21101
SIZE C
DWG NO 91C0569
REV L
SCALE
SHEET 27.0

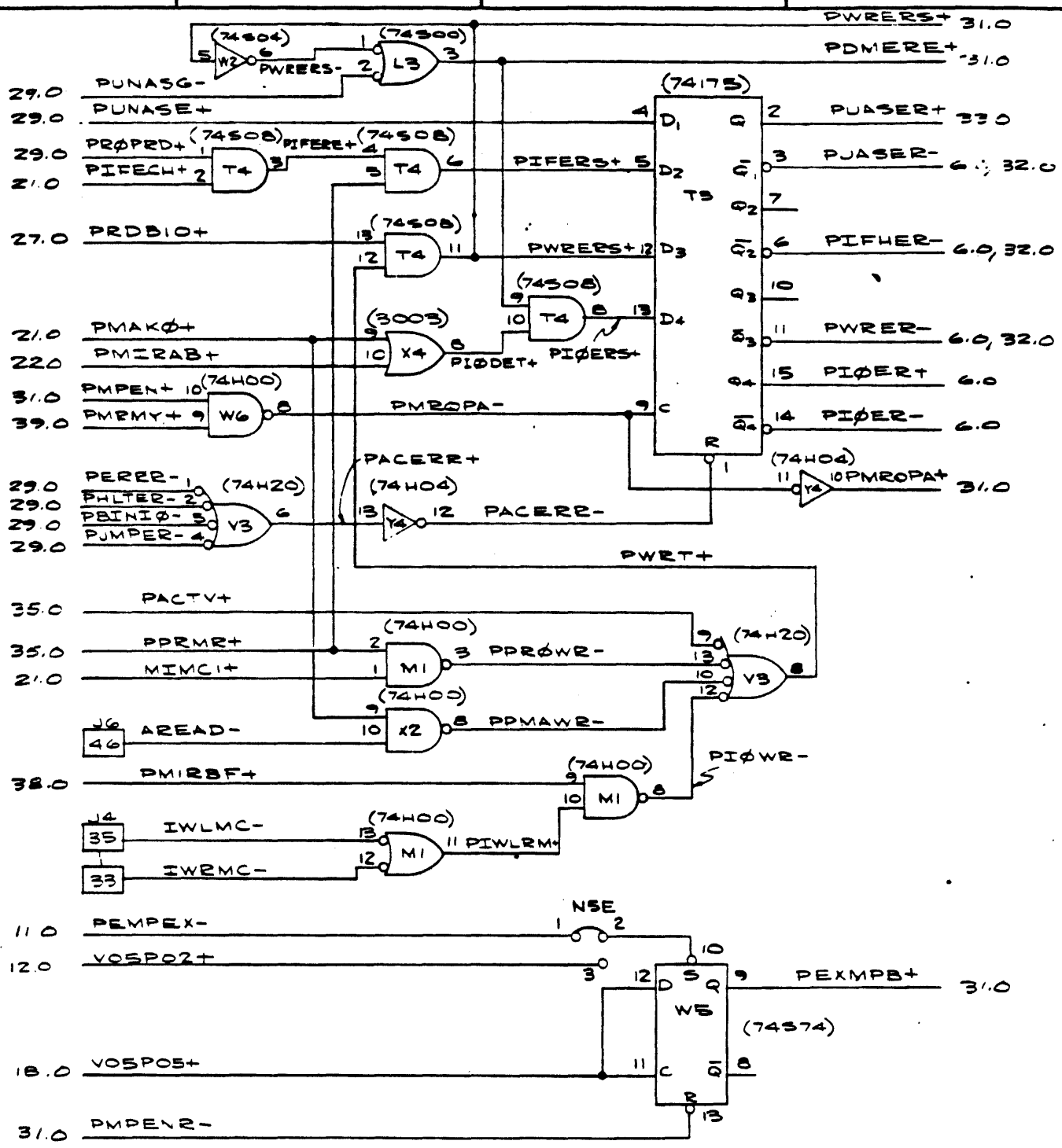


(74S158 3 PLACES)
B1
AX1
A1
J2
J13
(74S04)
L11
V8
(74S04)
W8
(74S8 SEL) 4 PLACES
PRDØ00-
PRDØ01-
PRDØ02-
PRDØ03-
PRAMA0-
PRAMA1-
PRAMA2-
PRAMA3-
PACTV-
PRDØ04-
PRDØ05-
PRDØ06-
PRAMA4-
PRAMA5-
MYMB15+
PRDØ07-
PRDØ08-
PRDØ11-
PRDØ12-
PRDØ07+
PRDØ08+
PRDØ11+
PRDØ12+
PMYA09+
PMYA10+
PMYA11+
PMYA12+
PMYA13+
PMYA14+
PMYA15+
PMYM15-
PMYA16+
PMYA17+
PMYA18+
PMYA19+
PAMB16-
PAMB17-
PAMB18-
PAMB19-
PACTVA+
+5V
R14 470Ω
V05P06+
16.0, 19.0, 31.0, 32.0, 35.0
PHYSICAL ADDRESS MUX
CODE IDENT NO. 21101
SIZE C
DWG NO 91C0569
REV L
SCALE
SHEET 28.0



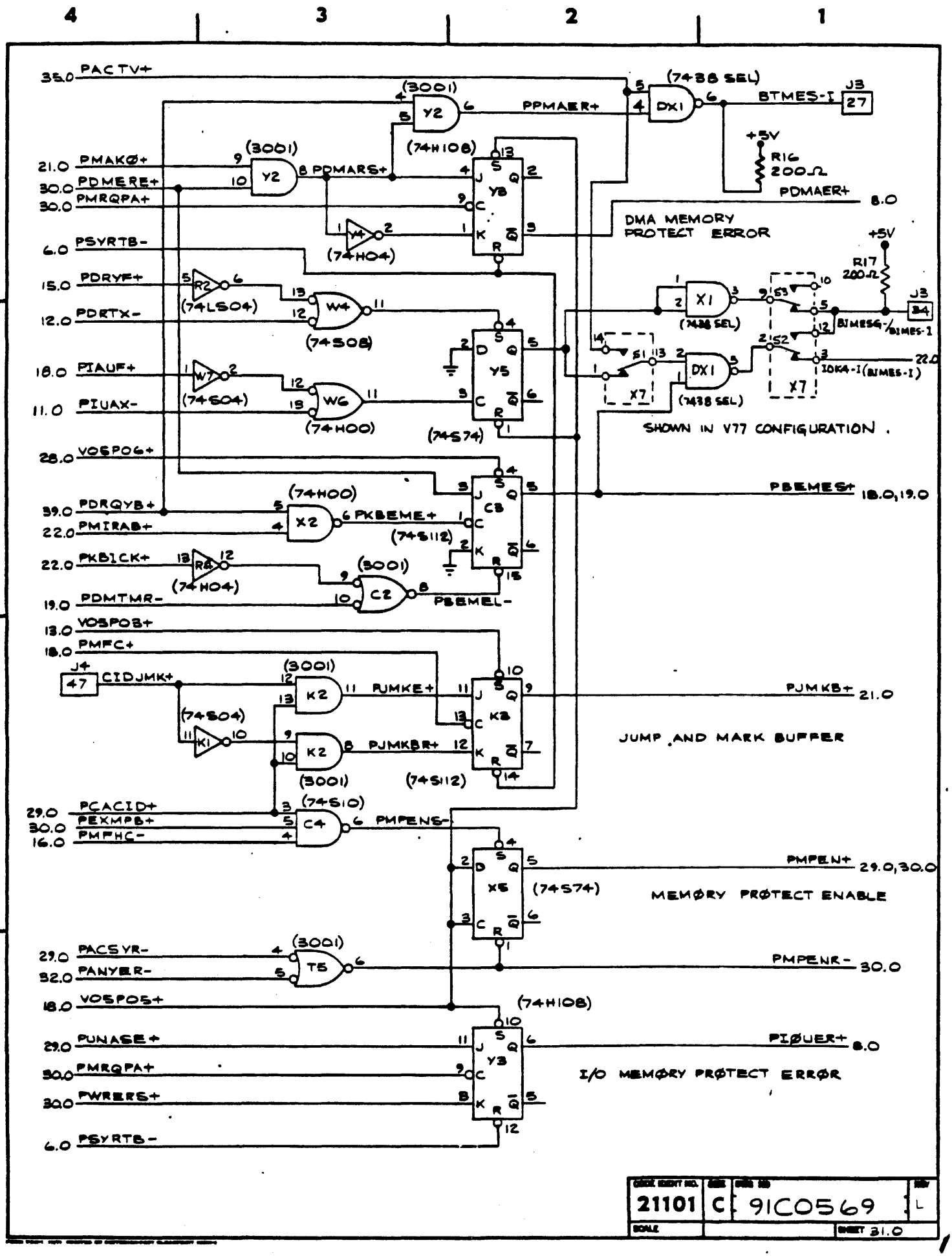
MEMORY PROTECT PRIMARY ERRORS

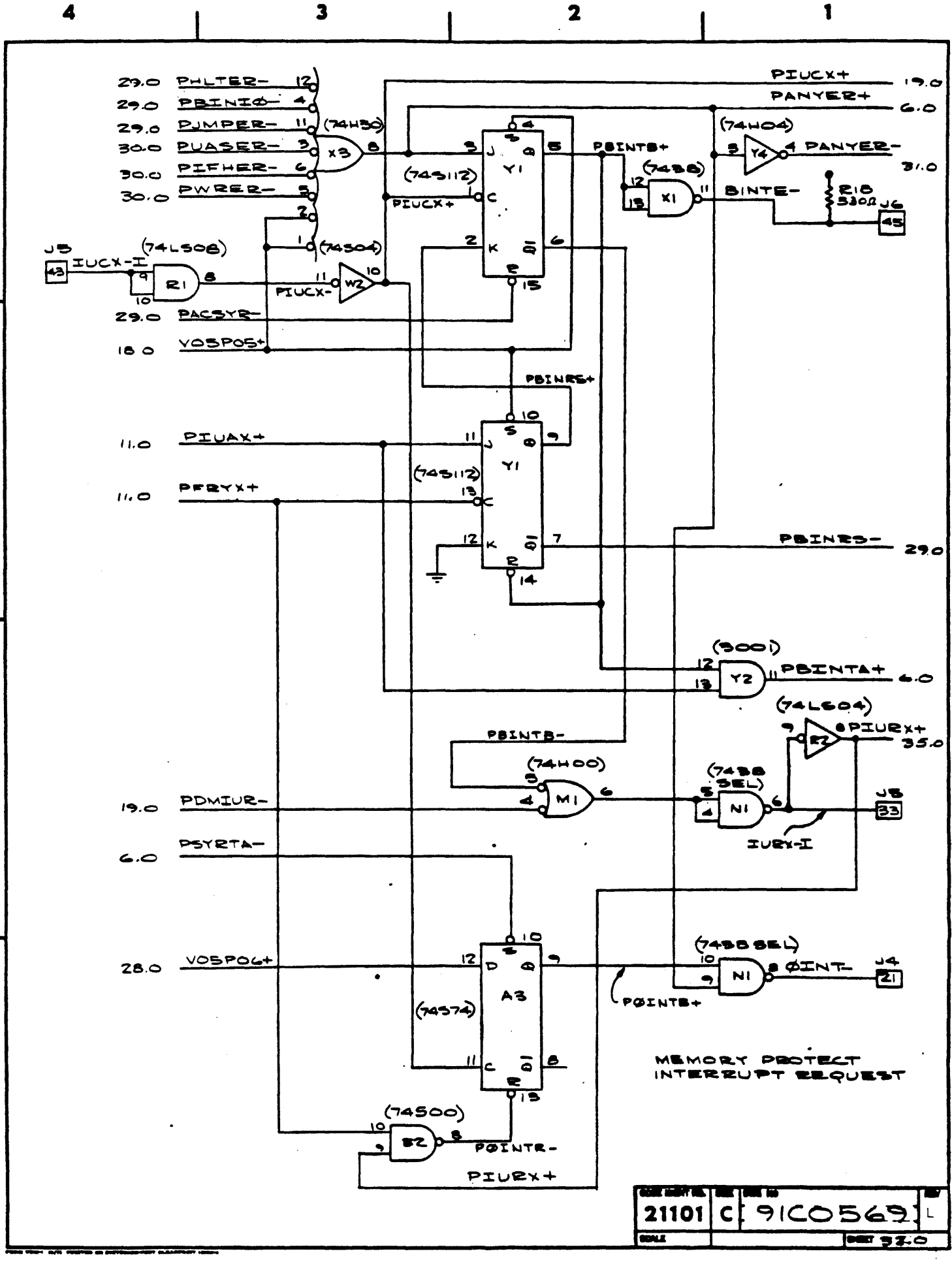
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100569	L
SCALE		SHEET 29 0	

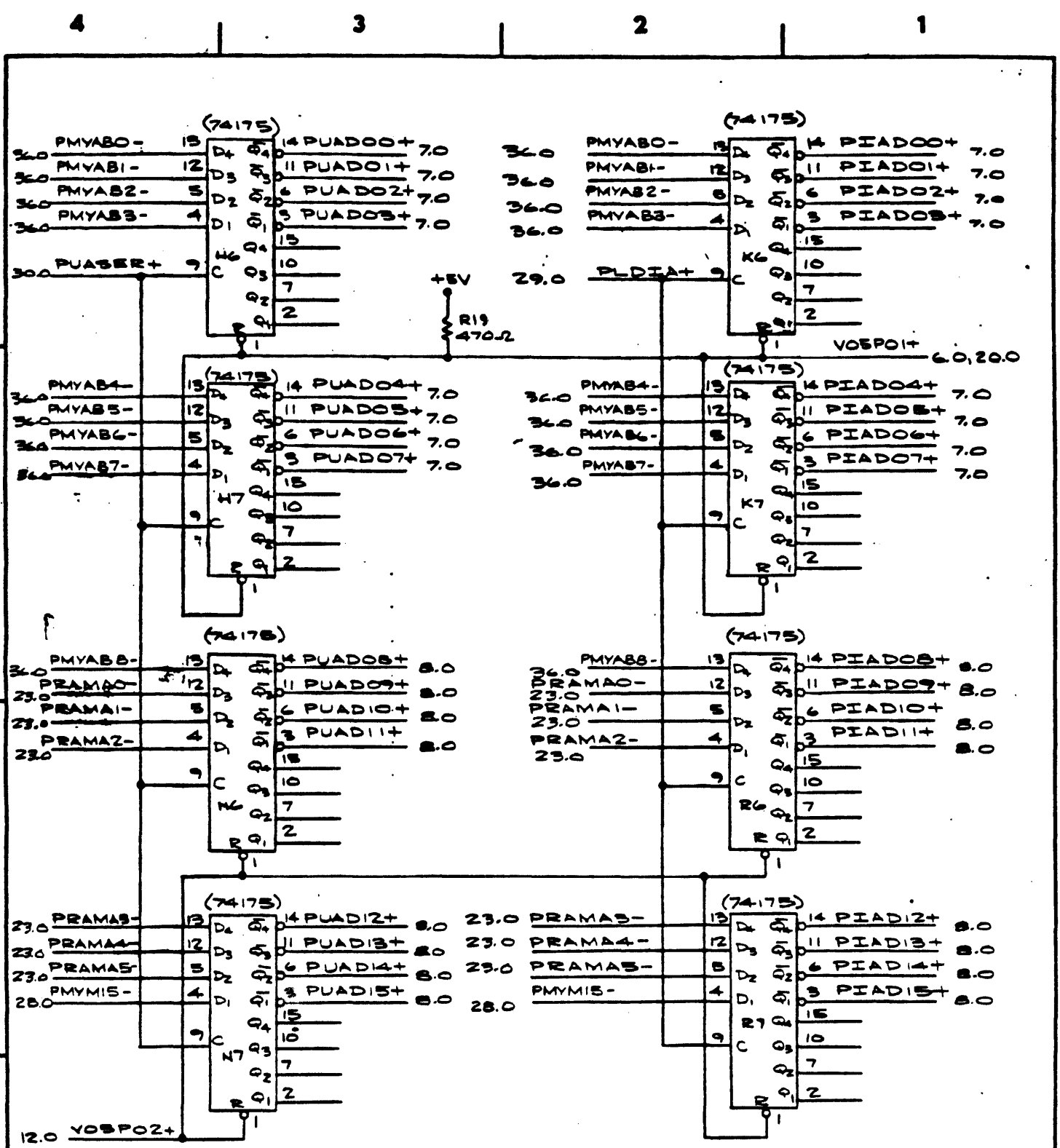


MEMORY PROTECT
SECONDARY ERRORS

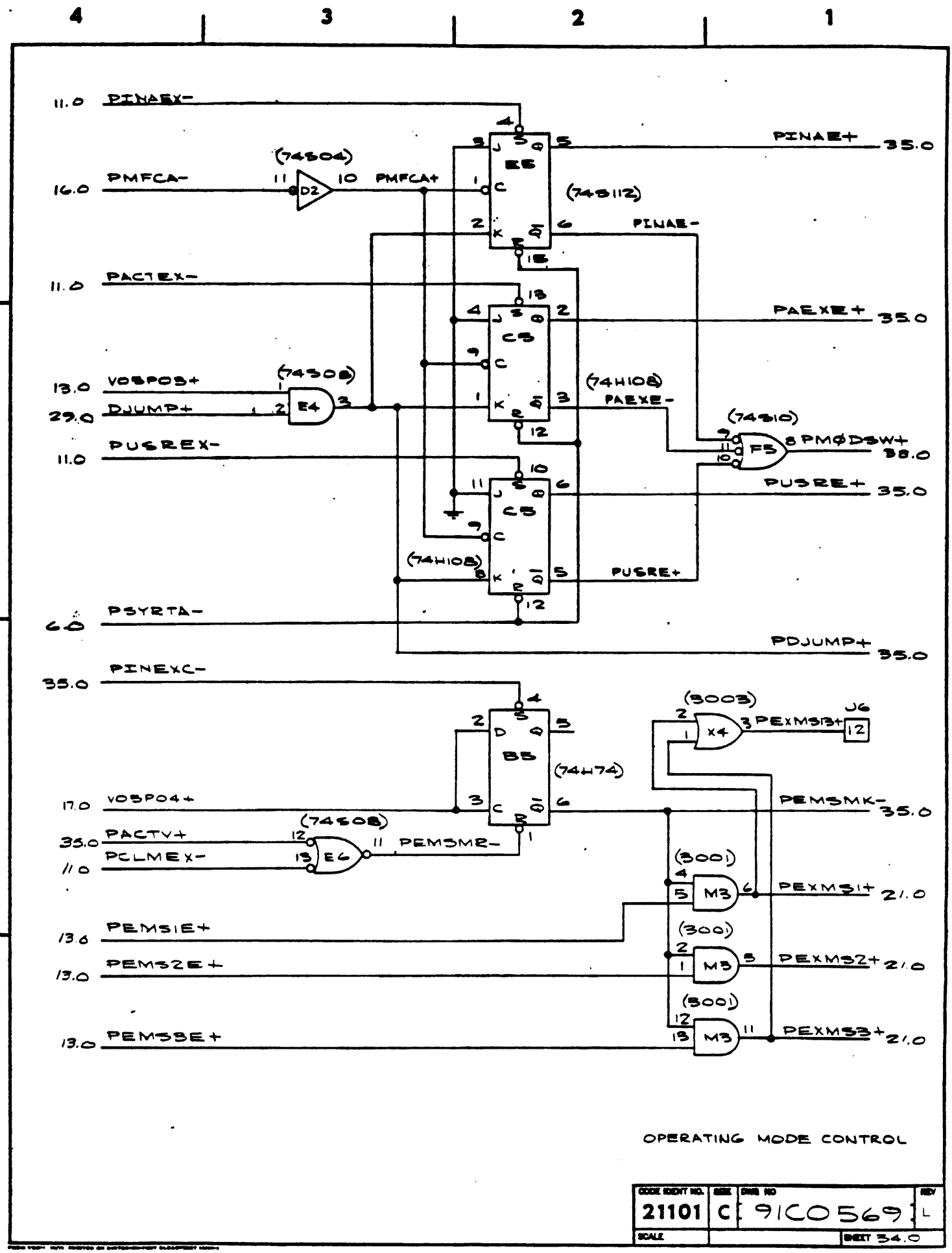
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100569	L
SCALE		SHEET 30.0	

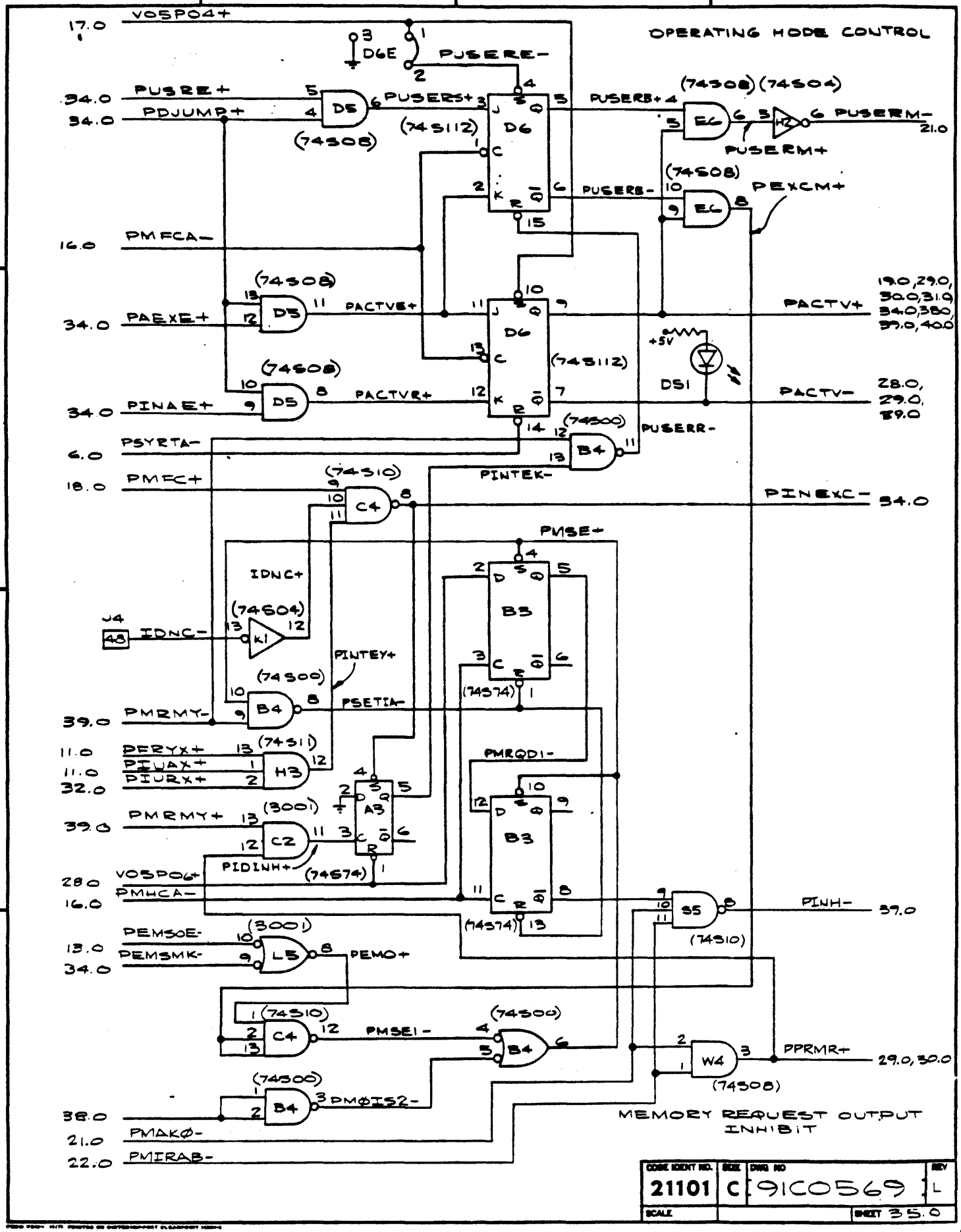

4
3
2
1
D
C
B
A
35.0 PACTV+
(3001)
Y2
PPMAER+
(7438 SEL)
DX1
BTMES-I
J3
27
+5V
R16
200Ω
PDMAER+ 8.0
21.0 PMAKØ+
30.0 PDMERE+
30.0 PMRQPA+
PDMARS+
(74H108)
Y8
DMA MEMORY
PROTECT ERROR
(74H04)
6.0 PSYRTB-
15.0 PDRYF+
12.0 PDRTX-
R2
(74LS04)
W4
(7408)
+5V
R17
200Ω
X1
(7438 SEL)
J3
34
BIMES4-/BIMES-1
18.0 PIAUF+
11.0 PIUAX-
W7
(74S04)
W6
(74H00)
Y5
(74S74)
DX1
(7438 SEL)
10K4-I(BIMES-I)
22.0
X7
X7
SHOWN IN V77 CONFIGURATION.
28.0 VOSPO6+
(74H00)
39.0 PDRQYB+
22.0 PMIRAB+
X2
PKBEME+
C8
(74S112)
PBEMES+ 18.0,19.0
22.0 PKBICK+
R4
(74H04)
(3001)
C2
19.0 PDMTMR-
PBEMEL-
13.0 VOSPO8+
18.0 PMFC+
J4
47
CIDJMK+
(3001)
K2
PJMKE+
K8
PJMKB+ 21.0
(74S04)
K1
K2
PJMKBR+
(3001)
(74S112)
JUMP AND MARK BUFFER
29.0 PCACID+
30.0 PEXMPB+
16.0 PMPHC-
(74S10)
C4
PMPENS-
PMPEN+ 29.0,30.0
X5
(74S74)
MEMØRY PRØTECT ENABLE
29.0 PACSYR-
32.0 PANYER-
(3001)
T5
PMPENR- 30.0
18.0 VOSPO5+
(74H108)
29.0 PUNASE+
30.0 PMRQPA+
30.0 PWRERS+
Y3
PIØUER+ 8.0
I/O MEMØRY PRØTECT ERRØR
6.0 PSYRTB-
21101
C
91C0569
L
SHEET 31.0


4
3
2
1
D
C
B
A
29.0 PHLTER- 12
29.0 PBINIØ- 4
29.0 PJMPER- 11
30.0 PUASER- 3
30.0 PIFHER- 6
30.0 PWRER- 5
(74H30)
X3
PIUCX+ 19.0
PANYER+ 6.0
(74H04)
Y4
4 PANYER- 31.0
PBINTB+
(7438)
X1
BINTE-
R10 330Ω
J6 45
(74S112)
Y1
PIUCX+
J5 43
IUCX-I
(74LS08)
R1
(74S04)
W2
PIUCX-
29.0 PACSYR-
18.0 VOSPOS+
PBINRS+
11.0 PIUAX+
11.0 PFRYX+
(74S112)
Y1
PBINRS- 29.0
(9001)
Y2
PBINTA+ 6.0
(74LS04)
R2
PIURX+ 35.0
PBINTB-
(74H00)
M1
(7438 SEL)
N1
J8 33
IURX-I
19.0 PDMIUR-
6.0 PSYRTA-
28.0 VOSPOG+
(74S74)
A3
(74S00 SEL)
N1
ØINT-
J4 21
PØINTB+
MEMORY PROTECT
INTERRUPT REQUEST
(74S00)
B2
PØINTR-
PIURX+
21101
C
91C0569
L
SHEET 33.0

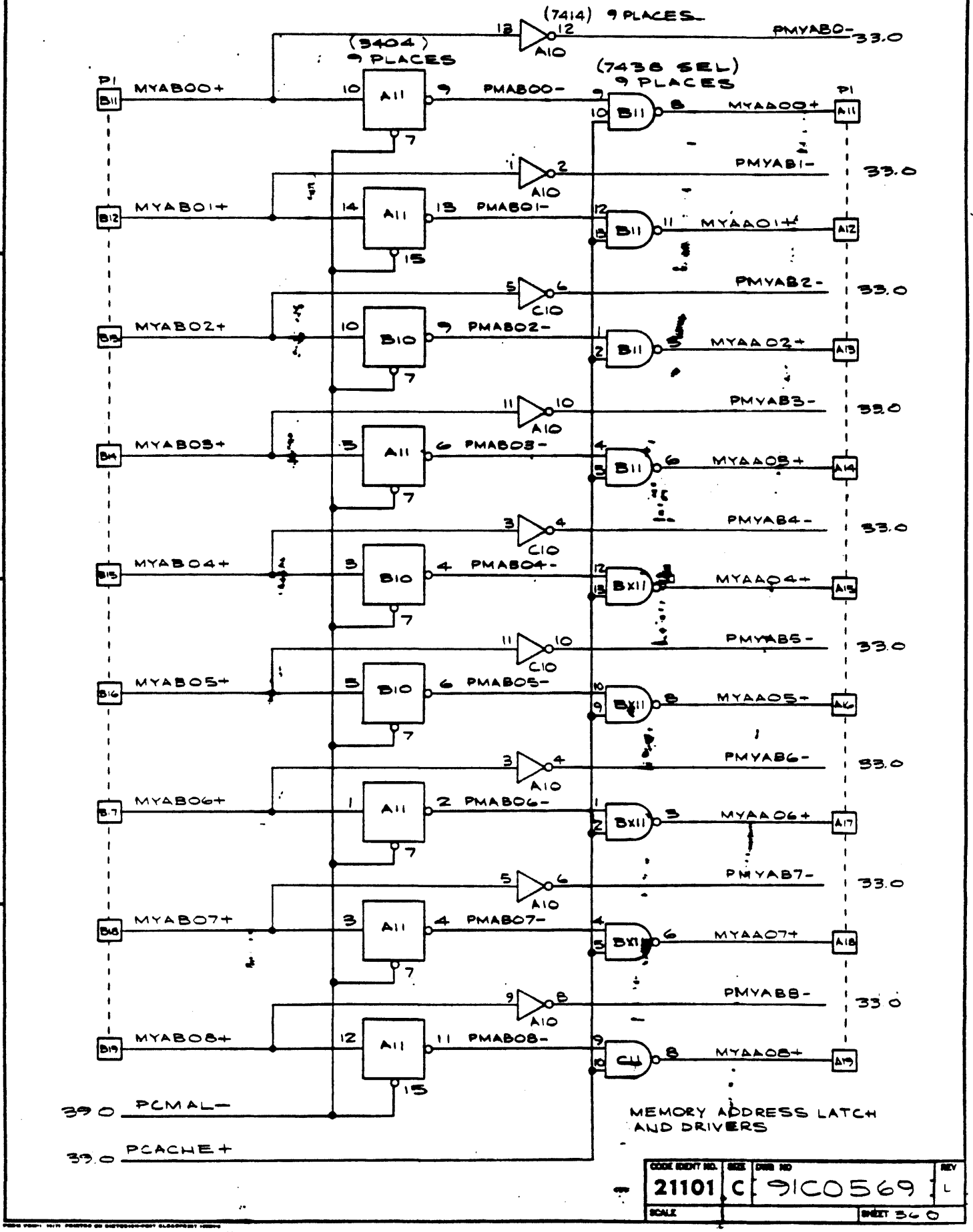


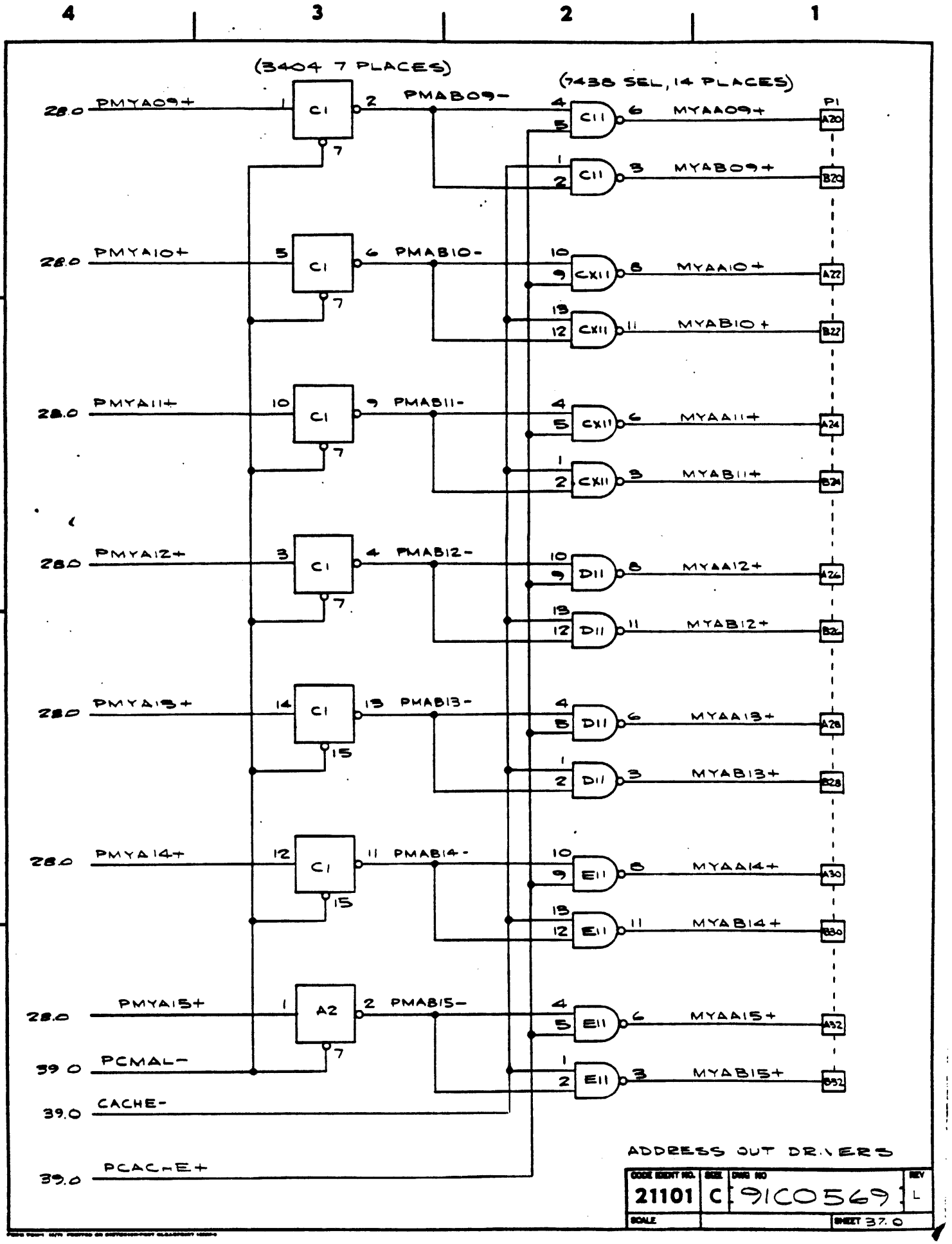
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100569	L
SCALE		SHEET 33.0	


4
3
2
1
D
C
B
A
11.0 PINAEX-
PINAE+ 35.0
(74S04)
16.0 PMFCA-
D2
PMFCA+
E5
(74S112)
PINAE-
11.0 PACTEX-
PAEXE+ 35.0
C5
13.0 VOSPO3+
29.0 DJUMP+
(74S08)
E4
(74H108)
PAEXE-
(74S10)
F5
PMΦDSW+ 38.0
11.0 PUSREX-
PUSRE+ 35.0
C5
(74H108)
PUSRE+
60 PSYRTA-
PDJUMP+ 35.0
35.0 PINEXC-
B5
(74H74)
(3003)
X4
PEXMS3+
J6
12
17.0 VOSPO4+
PEMSMK- 35.0
35.0 PACTV+
11.0 PCLMEX-
(74S08)
E6
PEMSMR-
(3001)
M3
PEXMS1+ 21.0
13.6 PEMS1E+
(3001)
M3
PEXMS2+ 21.0
13.0 PEMS2E+
(3001)
M3
PEXMS3+ 21.0
13.0 PEMS3E+
OPERATING MODE CONTROL
CODE IDENT NO. 21101
SIZE C
DWG NO 9100569
REV L
SCALE
SHEET 34.0



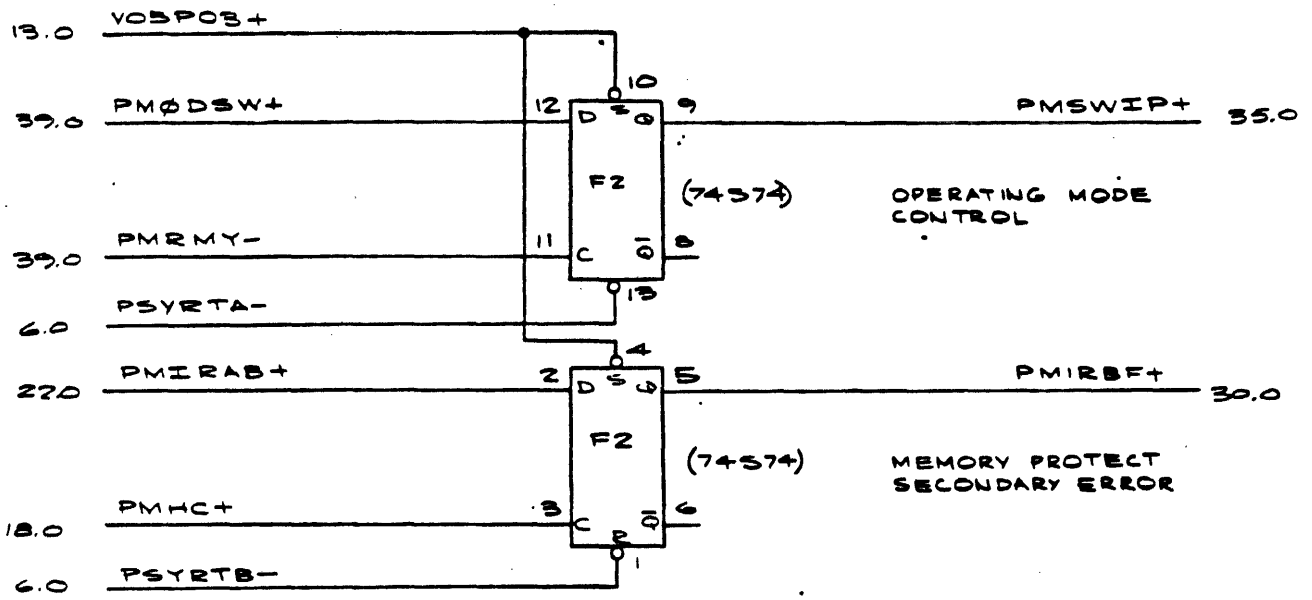
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9IC0569	L
SCALE		SHEET 35.0	

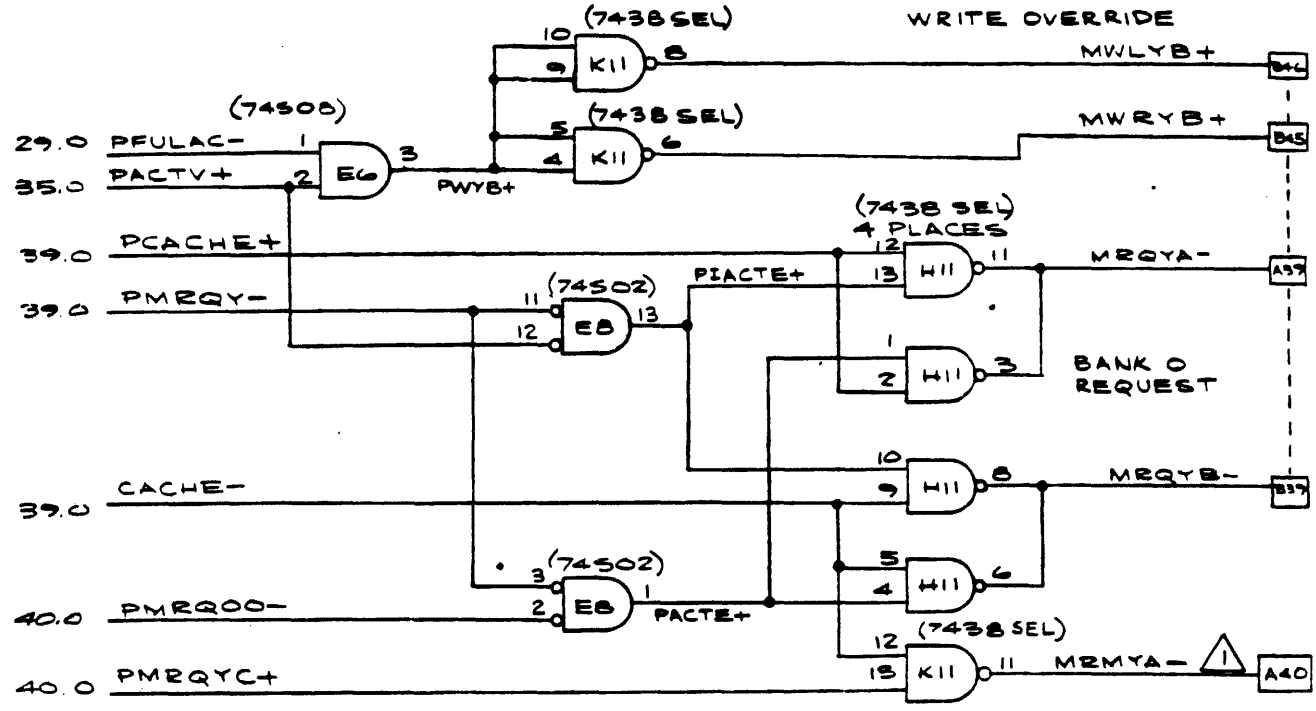

(7414) 9 PLACES
(3404) 9 PLACES
(7438 SEL) 9 PLACES
MYABO0+
MYABO1+
MYABO2+
MYABO3+
MYABO4+
MYABO5+
MYABO6+
MYABO7+
MYABO8+
PMABO0-
PMABO1-
PMABO2-
PMABO3-
PMABO4-
PMABO5-
PMABO6-
PMABO7-
PMABO8-
PMYABO-
PMYAB1-
PMYAB2-
PMYAB3-
PMYAB4-
PMYAB5-
PMYAB6-
PMYAB7-
PMYAB8-
MYAAO0+
MYAAO1+
MYAAO2+
MYAAO3+
MYAAO4+
MYAAO5+
MYAAO6+
MYAAO7+
MYAAO8+
PCMAL-
PCACHE+
MEMORY ADDRESS LATCH AND DRIVERS
CODE IDENT NO. 21101
SIZE C
DWG NO 9IC0569
REV L
SCALE
SHEET 36 0



ADDRESS OUT DRIVERS

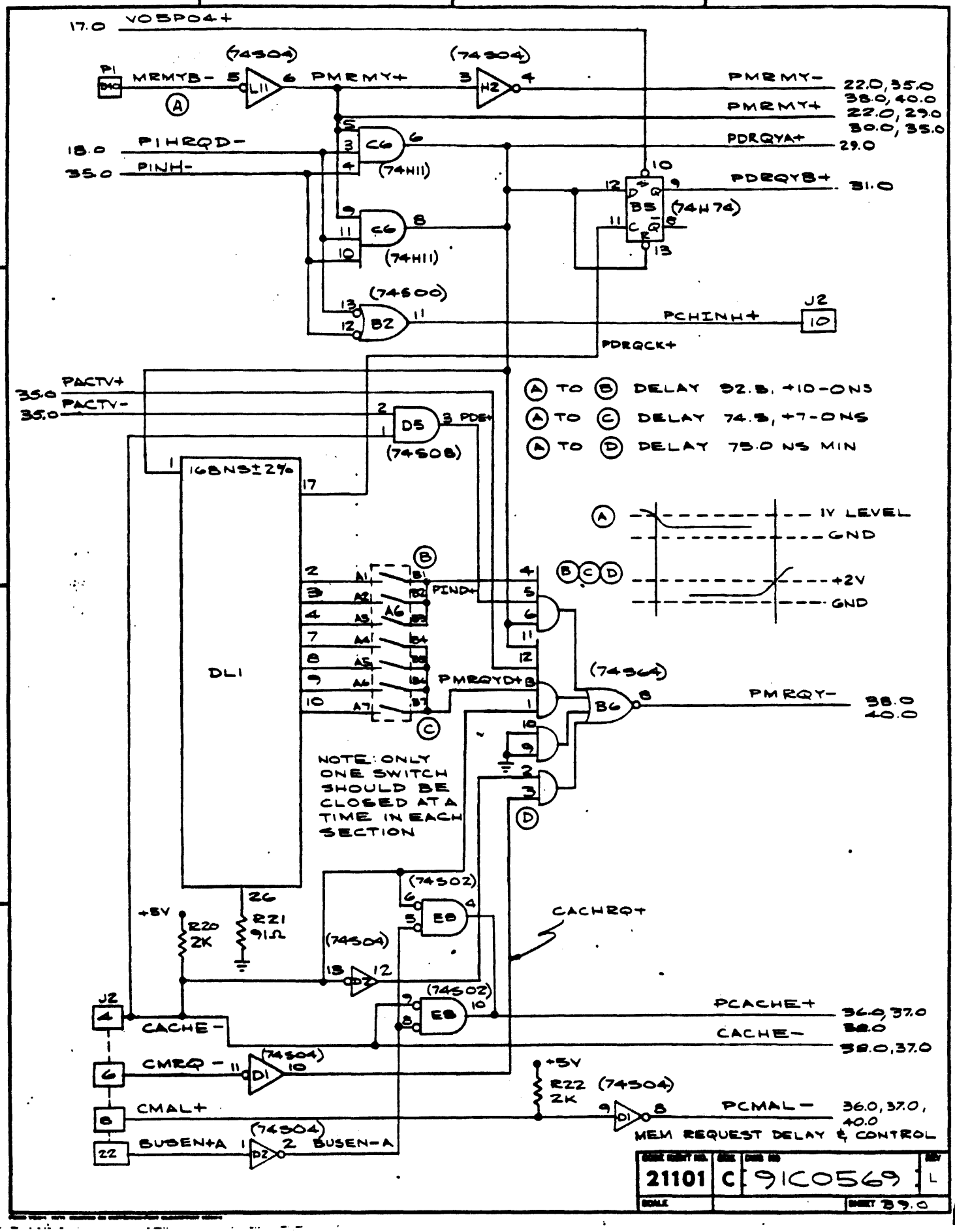
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100569	L
SCALE		SHEET 37.0	



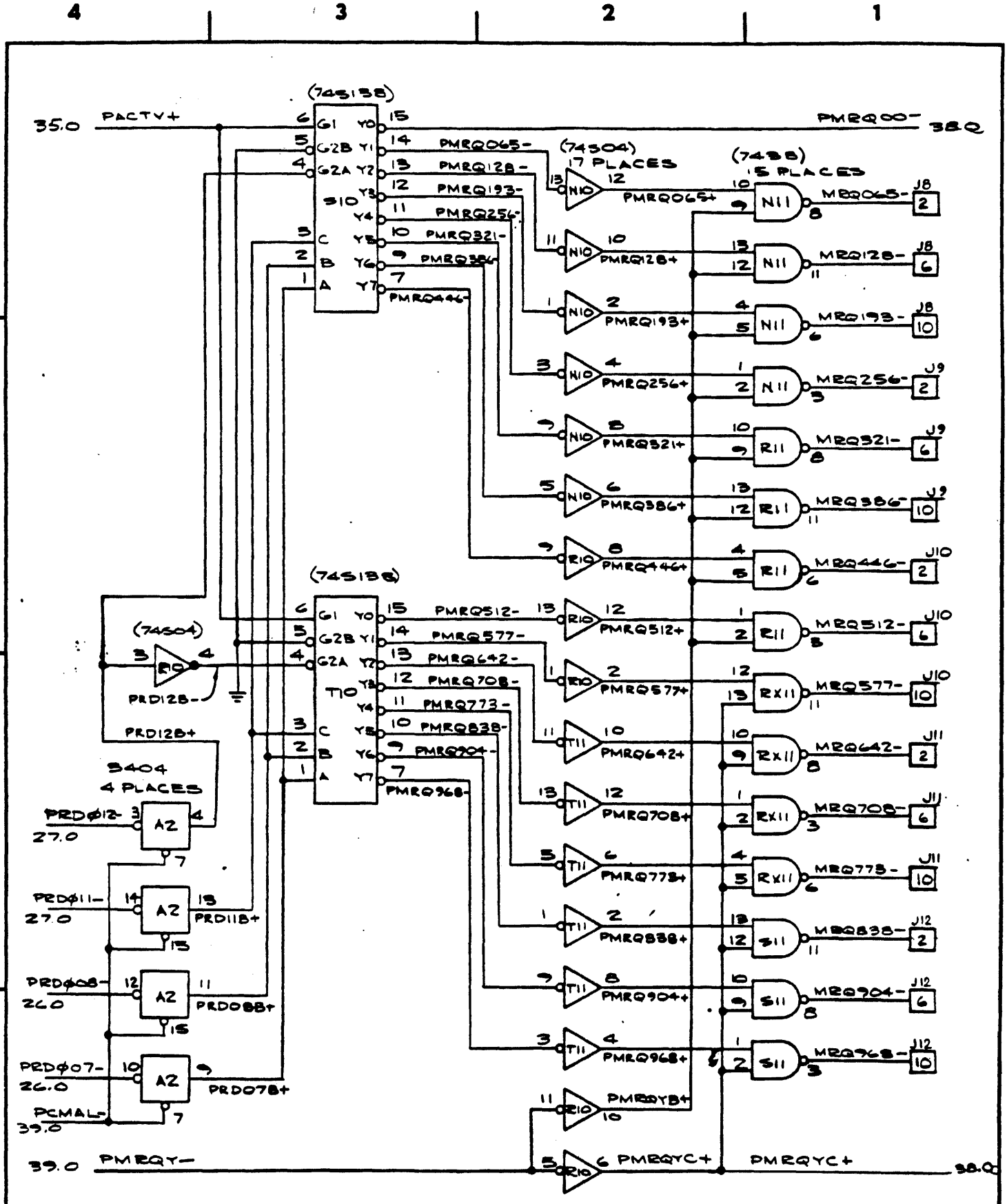


⚠1 PI-A40 IS FOR TIME OUT WHEN CACHE IS NOT IN SYSTEM. PROCESSOR MAP REQUEST (MRMYA-) IS ALWAYS CONFIGURED TO B PORT FOR THIS MAP.

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9C0569	L
SCALE			SHEET 38.0



17.0 V05P04+
(74S04)
P1
MRMYB-
L11
PMRMY+
H2
PMRMY- 22.0, 35.0 38.0, 40.0
PMRMY+ 22.0, 29.0 30.0, 35.0
18.0 PIHRQD-
35.0 PINH-
C6
(74H11)
PDRQYA+ 29.0
PDRQYB+ 31.0
B5
(74H74)
(74S00)
B2
PCHINH+
J2
PDRQCK+
PACTV+
35.0 PACTV-
D5
PDE+
(74S08)
A TO B DELAY 92.5, +10-0NS
A TO C DELAY 74.5, +7-0NS
A TO D DELAY 75.0 NS MIN
168NS±2%
DL1
1V LEVEL
GND
+2V
GND
PIND+
A6
PMRQYD+
(74S64)
B6
PMRQY- 38.0 40.0
NOTE: ONLY ONE SWITCH SHOULD BE CLOSED AT A TIME IN EACH SECTION
(74S02)
E8
CACHRQ+
+5V
R20 2K
R21 91Ω
(74S04)
D2
J2
CACHE-
PCACHE+ 36.0, 37.0 38.0
CACHE- 38.0, 37.0
CMRQ-
D1
R22 2K
CMAL+
PCMAL- 36.0, 37.0, 40.0
BUSEN+A
BUSEN-A
MEM REQUEST DELAY & CONTROL
21101
C
91C0569
L
SHEET 39.0


4
3
2
1
D
C
B
A
35.0 PACTV+
(74S138)
PMRQ00- 38.0
PMRQ065-
PMRQ128-
PMRQ193-
PMRQ256-
PMRQ321-
PMRQ386-
PMRQ446-
(74S04)
17 PLACES
(74S38)
15 PLACES
PMRQ065+
PMRQ128+
PMRQ193+
PMRQ256+
PMRQ321+
PMRQ386+
PMRQ446+
MRQ065- J8 2
MRQ128- J8 6
MRQ193- J8 10
MRQ256- J9 2
MRQ321- J9 6
MRQ386- J9 10
MRQ446- J10 2
(74S138)
PMRQ512-
PMRQ577-
PMRQ642-
PMRQ708-
PMRQ773-
PMRQ838-
PMRQ904-
PMRQ968-
PMRQ512+
PMRQ577+
PMRQ642+
PMRQ708+
PMRQ773+
PMRQ838+
PMRQ904+
PMRQ968+
MRQ512- J10 6
MRQ577- J10 10
MRQ642- J11 2
MRQ708- J11 6
MRQ773- J11 10
MRQ838- J12 2
MRQ904- J12 6
MRQ968- J12 10
(74S04)
PRD12B-
PRD12B+
5404
4 PLACES
PRDφ12- 27.0
PRDφ11- 27.0
PRDφ08- 26.0
PRDφ07- 26.0
PCMAL- 39.0
PRD11B+
PRD08B+
PRD07B+
PMRQYB+
39.0 PMRQY-
PMRQYC+
PMRQYC+ 38.0
MEMORY BANK SELECTION
21101
C
9100569
L
SCALE
SHEET 40.0

4 3 2 1

D C B A

CONNECTOR J8

PIN	FUNCTION	SHEET	PIN	FUNCTION	SHEET
1	GND	3.0	26	GND	3.0
2	GND	3.0	27	BTMES-I	31.0
3			28	GND	3.0
4	GND	3.0	29	IØK1-I	22.0
5			30	IØK2-I	22.0
6	GND	3.0	31	IØK3-I	22.0
7			32	IØK4-I(BIMES-I)	22.0
8	GND	3.0	33	GND	3.0
9	FI1X-I	16.0	34	BIMES6-/BIMES-I	31.0
10	GND	3.0	35	GND	3.0
11	FI2X-I	16.0	36		
12	GND	3.0	37		
13	FI3X-I	16.0	38	GND	3.0
14	GND	3.0	39	TPOF-I	17.0
15	FI4X-I	16.0	40	GND	3.0
16	GND	3.0	41	TPIF-I	17.0
17	FI5X-I	16.0	42	GND	3.0
18	GND	3.0	43	IUCF-I	17.0
19	FI6X-I	16.0	44	GND	3.0
20	GND	3.0	45	FIYF-I	15.0
21	FI7X-I	16.0	46	GND	3.0
22	GND	3.0	47	IUAF-I	18.0
23	FI8X-I	16.0	48	GND	3.0
24	GND	3.0	49	DIYF-I	15.0
25	FIYX-I	16.0	50	GND	3.0

CONNECTOR J4

PIN	FUNCTION	SHEET	PIN	FUNCTION	SHEET
1	GND	3.0	26	IIA5+	N/U
2	CBTS0+	N/U	27	CBMF+	N/U
3	ICD3+	N/U	28	IIA2+	N/U
4	CBTS1+	N/U	29	CIDIO+	29.0
5	ICD2+	N/U	30	IIA1+	N/U
6	CBTS2+	N/U	31	MIMC1+	21.0
7	ICD1+	N/U	32	MOCLK+	N/U
8	CBTS3+	N/U	33	IWIMC-	30.0
9	ICD4A+	N/U	34	MIMI1+	N/U
10	INTF+	N/U	35	IWLMC-	30.0
11	IIRQM-	N/U	36	CBMB+	36.0
12	FIIX-I	N/U	37	MAKIO+	37.0
13	ICD0+	N/U	38	MPC-	18.0
14	DJUMP+	29.0	39	MRS2A+	18.0
15	MIL14A+	N/U	40	CPMAST+	N/U
16	CBAB0+	N/U	41	OBQM-	N/U
17	IIS0+	N/U	42	CCS3D+	N/U
18	CBAB1+	N/U	43	MAKO+	21.0
19	CINMPC-	N/U	44	IAKC1-	N/U
20	IIA0+	N/U	45	CIDHLT+	29.0
21	OINT-	32.0	46	CBQIO+	N/U
22	MTRC-	N/U	47	CIDJMK+	31.0
23	IIQC-	N/U	48	IDNC-	35.0
24	CACIDE+	29.0	49	MCR0+	N/U
25	MWC-	18.0	50	GND	3.0

CONNECTOR J5

PIN	FUNCTION	SHEET	PIN	FUNCTION	SHEET
1	GND	3.0	26	GND	3.0
2	EB00-I	4.0	27	OPSTRT-	N/U
3	EB01-I	4.0	28	GND	3.0
4	EB02-I	4.0	29	FI10X-I	N/U
5	EB03-I	4.0	30	GND	3.0
6	EB04-I	4.0	31	SERX-I	11.0
7	EB05-I	4.0	32	GND	3.0
8	EB06-I	4.0	33	IURX-I	32.0
9	EB07-I	4.0	34	GND	3.0
10	EB08-I	5.0	35	TPOX-I	N/U
11	EB09-I	5.0	36	GND	3.0
12	EB10-I	5.0	37	TPIX-I	N/U
13	EB11-I	5.0	38	GND	3.0
14	EB12-I	5.0	39	IUAX-I	11.0
15	EB13-I	5.0	40	GND	3.0
16	EB14-I	5.0	41	FIYX-I	11.0
17	EB15-I	5.0	42	GND	3.0
18	GND	3.0	43	IUCX-I	32.0
19	NSS2-	N/U	44	GND	3.0
20	NSS1-	N/U	45	SYRT-I	6.0
21	NSS3-	N/U	46	GND	3.0
22	GND	3.0	47	DIYX-I	12.0
23	IEIDLA+	N/U	48	GND	3.0
24	GND	3.0	49	IUJX-I	N/U
25	NSTP-	N/U	50	GND	3.0

CONNECTOR J6

PIN	FUNCTION	SHEET	PIN	FUNCTION	SHEET
1	GND	3.0	26	IIO04+	N/U
2	CESK+	N/U	27	IIO03+	N/U
3	CPMAST+	N/U	28	IIO02+	N/U
4	CIDXX5+	29.0	29	IIO01+	N/U
5	NSTP-	N/U	30	FIO00+	N/U
6	OINT-	N/U	31	GND	3.0
7	NSS3-	N/U	32	IIA07+	N/U
8	NSS1-	N/U	33	IIA06+	N/U
9	NSS2-	N/U	34	IIA01+	N/U
10	CIDXX3+	N/U	35	IIA04+	N/U
11	FIUX-I	N/U	36	IIA03+	N/U
12	FEXMS13+	34.0	37	IIA05+	N/U
13	MPC-	N/U	38	IIA02+	N/U
14	GND	3.0	39	IIA00+	N/U
15	IIO15+	N/U	40	GND	3.0
16	IIO14+	N/U	41	XIOCE-	N/U
17	IIO13+	N/U	42	CID00+	29.0
18	IIO12+	N/U	43	CIDIO+	N/U
19	IIO11+	N/U	44	HNMC-	N/U
20	IIO10+	N/U	45	INTE-	32.0
21	IIO09+	N/U	46	AREAD-	30.0
22	IIO08+	N/U	47	MNO-	29.0
23	IIO07+	N/U	48	MIRA8+	22.0
24	IIO06+	N/U	49	MIMC0+	21.0
25	IIO05+	N/U	50	GND	3.0

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0569	L
SCALE			SHEET 41.1

CONNECTOR J8

PIN	FUNCTION	SHEET
1	GND	3.0
2	MRQ065-	40.0
3	N/U (KEY)	
4	GND	3.0
5	GND	3.0
6	MRQ128-	40.0
7	N/U (KEY)	
8	GND	3.0
9	GND	3.0
10	MRQ193-	40.0
11	N/U (KEY)	
12	GND	3.0

CONNECTOR J9

PIN	FUNCTION	SHEET
1	GND	3.0
2	MRQ256-	40.0
3	MRQ256-	40.0
4	GND	3.0
5	GND	3.0
6	MRQ321-	40.0
7	MRQ321-	40.0
8	GND	3.0
9	GND	3.0
10	MRQ386-	40.0
11	MRQ386-	40.0
12	GND	3.0

CONNECTOR J12

PIN	FUNCTION	SHEET
1	GND	3.0
2	MRQ836-	40.0
3	N/U (KEY)	
4	GND	3.0
5	GND	3.0
6	MRQ904-	40.0
7	N/U (KEY)	
8	GND	3.0
9	GND	3.0
10	MRQ968-	40.0
11	N/U (KEY)	
12	GND	3.0

CONNECTOR J10

PIN	FUNCTION	SHEET
1	GND	3.0
2	MRQ446-	40.0
3	MRQ446-	40.0
4	GND	3.0
5	GND	3.0
6	MRQ512-	40.0
7	MRQ512-	40.0
8	GND	3.0
9	GND	3.0
10	MRQ577-	40.0
11	MRQ577-	40.0
12	GND	3.0

CONNECTOR J11

PIN	FUNCTION	SHEET
1	GND	3.0
2	MRQ642-	40.0
3	MRQ642-	40.0
4	GND	3.0
5	GND	3.0
6	MRQ708-	40.0
7	MRQ708-	40.0
8	GND	3.0
9	GND	3.0
10	MRQ773-	40.0
11	MRQ773-	40.0
12	GND	3.0

CONNECTOR J13

PIN	FUNCTION	SHEET
1	GND	3.0
2		
3		
4		
5		
6		
7		
8	GND	3.0
9	PKAMX3-	22.0
10	PKAMX2-	
11	PKAMX1-	
12	PKAMX0-	22.0
13	PAMB19-	28.0
14	PAMB18-	
15	PAMB17-	
16	PAMB16-	28.0

CODE IDENT NO.	SIZE	DRG NO	REV
21101	C	91C0569	L
SCALE			SHEET 41.2