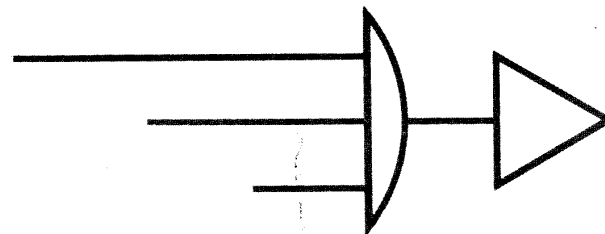


UNIVAC[®] Solid-State Computer

— Manual 2 —



LOGIC DRAWINGS

Volume IB

**BASIC SYSTEM
ALL
PROCESSOR MODELS**

Remington Rand Univac[®]
DIVISION OF SPERRY RAND CORPORATION

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INTRODUCTION

Manual 2, volume IB, contains the logic drawings for the UNIVAC Solid-State Computer system with magnetic tape, RANDEX® drum files, the card-punching printer (CPP), core storage, dual tape synchronizers*, and paper tape. The drawings in this volume are numbered 1-1B, 1-2B, and so forth. The designation 1- indicates that drawing is in volume 1; the letter B distinguishes these drawings from others published at an earlier or later date.

This volume presently contains the logic drawings for the following USSC systems:

Models 130A and 154 — including the 90-column tower read-punch unit;

Models 131A and 159 — including the 80/90-column Bull read-punch unit;

Model 139 — including the CPP;

Models 176 and 184 — including core storage, dual tape synchronizers, and paper tape.

The same manual drawing numbers have been assigned to drawings which represent different models. The model number(s) for each drawing is included in the manual title. Models 130A, 131A, 154, 159, 176, and 184 use the I/O Synchronizer Tape/RANDEX (models 146 and 153), the logic drawings of which are contained in manual 2, volume III.

Sections of the volume-IB drawings not common to all models of the USSC system are enclosed in labeled boxes which are identified as follows:

Identification	System	Identification	System
C80	80-column card only	TR	System with magnetic-tape and RANDEX only
C90	90-column card only	CPP	System with card-punching printer only
T80	80-column magnetic-tape only	R	RANDEX system only
T90	90-column magnetic-tape only	2HSP	System with two high-speed printers only
80	80-column only	C	System with core storage
90	90-column only	DS	System with dual tape synchronizer
T	Magnetic-tape only	PT	System with paper tape
IR	System with index-registers only		

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*The system with dual tape synchronizers may consist of two model 153 synchronizers (tape only) or one model 153 and one model 146 (tape/RANDEX) synchronizer.

The following information concerns all drawings: Signal names in boxes with a dagger (†) are only input or output signals for the model number referenced by the dagger.

The NM and SM signals are interchangeable. Signals that appear on the drawings with a prime (such as TB'2), will be typed out in a signal glossary printout with the letter V substituted for the prime (TBV2).

Tables 1-1 through 1-4 supply a cross-reference from the manual drawings to the engineering logic diagrams. Although the same basic processor is used in all USSC systems, each processor model is represented by a sepa-

rate engineering-drawing series. Thus tables 1-1 through 1-4 are oriented by processor model numbers; each manual drawing number is keyed to a processor model number which is, in turn, keyed to a specific engineering-drawing series. For complete reference accuracy, the processor model number must be taken into account when the engineering sources are consulted. The revision column indicates the revision level at which the 1B drawings were prepared.

Table 1-1. Engineering-Drawing Sources for Models 130A and 131A

Volume 1B Drawing Numbers	Processor Model Numbers		Engineering-Drawing Source		Volume 1B Drawing Numbers	Processor Model Numbers		Engineering-Drawing Source	
	130A	131A	Number	Revision		130A	131A	Number	Revision
1-1B	✓	✓	D 809 432	G	1-26B	✓	—	D 810 073	B
1-2B	✓	✓	D3 821 162	None	1-27B	✓	—	D 810 072	G
1-3B	✓	✓	D 809 442	T	1-27B	✓	—	D 810 076	C
1-3B	✓	✓	D 809 443	H	1-27B	✓	—	D 810 074	E
1-4B	✓	✓	D3 821 163	None	1-28B	—	✓	D 810 811	J
1-5B	✓	✓	D 809 446	L	1-29B	—	✓	D 810 812	F
1-6B	✓	✓	D 809 437	J	1-30B	—	✓	D 810 813	K
1-7B	✓	✓	J 809 438	F	1-31B	✓	—	D 810 070	G
1-8B	✓	✓	D 809 434	R	1-31B	—	✓	D 810 807	G
1-8B	✓	✓	D3 813 413	C	1-32B	✓	—	D 810 071	H
1-9B	✓	✓	D3 820 626	C	1-32B	—	✓	D 810 808	H
1-10B	✓	✓	D 809 435	R	1-33B	—	✓	D 811 043	D
1-11B	✓	✓	D3 820 626	E	1-33B	—	✓	D 810 809	F
1-12B	✓	✓	D3 821 160	None	1-34B	—	✓	D 810 800	A
1-13B	✓	✓	D 809 439	A	1-34B	✓	—	D 810 063	B
1-14B	✓	✓	D3 821 161	None	1-35B	✓	—	D 810 064	B
1-15B	✓	✓	D 809 431	E	1-35B	—	✓	D 810 801	B
1-16B, 1-17B	✓	✓	D 809 436	M	1-36B	✓	—	D 810 065	C
1-18B	✓	✓	D 809 452	L	1-36B	—	✓	D 810 802	B
1-19B	✓	✓	D 809 451	G	1-37B	✓	—	D 810 069	E
1-20B	✓	✓	D 809 450	C	1-37B	—	✓	D 810 806	F
1-21B	✓	✓	D3 821 164	None	1-38B	✓	—	D 810 068	B
1-22B	✓	✓	D 809 448	C	1-38B	—	✓	D 810 805	A
1-23B	✓	✓	D 809 449	A	1-39B	✓	—	D 810 067	D
1-24B	✓	✓	D 809 472	G	1-39B	—	✓	D 810 804	C
1-25B	✓	✓	D 809 473	D	1-40B	✓	—	D 810 066	B
1-26B	—	✓	D 810 810	D	1-40B	—	✓	D 810 803	B

Table 1-2. Engineering-Drawing Sources for Models 154 and 159

Volume 1B Drawing Numbers	Processor Model Numbers		Engineering-Drawing Source		Volume 1B Drawing Numbers	Processor Model Numbers		Engineering-Drawing Source	
	154	159	Number	Revision		154	159	Number	Revision
1-1B	✓	✓	D3 814 723	C	1-21B	✓	✓	D3 814 716	F
1-2B	✓	✓	D3 814 710	E	1-21B	✓	✓	D3 814 717	B
1-3B	✓	✓	D3 814 711	C	1-22B	✓	✓	D3 814 718	B
1-3B	✓	✓	D3 814 712	D	1-23B	✓	✓	D3 814 720	C
1-4B	✓	✓	D3 814 713	E	1-24B	✓	✓	D3 814 729	C
1-5B	✓	✓	D3 814 734	F	1-25B	✓	✓	D3 814 730	A
1-6B	✓	✓	D3 814 721	B	1-26B	—	✓	D3 814 362	None
1-7B	✓	✓	D3 814 722	B	1-26B	—	✓	D3 814 361	None
1-8B	✓	✓	D3 814 724	B	1-27B	—	✓	D3 814 363	None
1-8B	✓	✓	D3 814 725	A	1-28B	—	✓	D3 815 366	None
1-9B	✓	✓	D3 820 626	E	1-29B	—	✓	D3 815 367	None
1-10B	✓	✓	D3 814 726	B	1-30B	—	✓	D3 815 368	A
1-11B	✓	✓	D3 820 626	E	1-31B	—	✓	D3 815 364	None
1-12B	✓	✓	D3 814 727	B	1-32B	—	✓	D3 815 365	None
1-13B	✓	✓	D3 814 732	A	1-34B	—	✓	D3 815 370	A
1-14B	✓	✓	D3 814 733	E	1-35B	—	✓	D3 815 371	None
1-15B	✓	✓	D3 814 731	C	1-36B	—	✓	D3 815 372	None
1-16B, 1-17B	✓	✓	D3 814 715	D	1-37B	—	✓	D3 815 369	None
1-18B	✓	✓	D3 814 737	B	1-38B	—	✓	D3 815 374	A
1-19B	✓	✓	D3 814 735	C	1-39B	—	✓	D3 815 373	None
1-20B	✓	✓	D3 814 719	D	1-40B	—	✓	D3 815 375	None

Table 1-3. Engineering-Drawing Sources for Model 139 (cont)

Volume 1B Drawing Numbers	Engineering-Drawing Source		Volume 1B Drawing Numbers	Engineering-Drawing Source	
	Number	Revision		Number	Revision
1-25B	D3 815 099	None	1-34B	D3 814 764	A
1-26B	D3 814 755	E	1-35B	D3 814 765	C
1-27B	D3 814 754	F	1-36B	D3 814 766	C
1-28B	D3 814 759	L	1-37B	D3 814 762	L
1-29B	D3 814 764	E	1-37B	D3 814 763	J
1-30B	D3 814 761	R	1-38B	D3 814 768	E
1-31B	D3 814 757	B	1-39B	D3 814 767	F
1-32B	D3 814 758	B	1-40B	D3 814 769	D
1-33B	D3 814 756	B			

Table 1-4. Engineering-Drawing Sources for Models 176 and 184

Volume 1B Drawing Numbers	Processor Model Numbers		Engineering-Drawing Source		Volume 1B Drawing Numbers	Processor Model Numbers		Engineering-Drawing Source	
	176	184	Number	Revision		176	184	Number	Revision
1-1B	✓	✓	D3 817 030	None	1-24B	✓	✓	D3 817 035	B
1-2B	✓	✓	D3 817 018	F	1-25B	✓	✓	D3 817 036	A
1-3B	✓	✓	D3 817 019	C	1-26B	✓	—	D3 817 002	None
1-3B	✓	✓	D3 817 020	E	1-26B	—	✓	D3 817 045	B
1-4B	✓	✓	D3 817 021	F	1-27B	✓	—	D3 817 001	A
1-5B	✓	✓	D3 817 040	D	1-27B	—	✓	D3 817 044	B
1-6B	✓	✓	D3 817 028	C	1-28B	✓	—	D3 817 006	A
1-7B	✓	✓	D3 817 029	None	1-29B	✓	—	D3 817 007	B
1-8B	✓	✓	D3 817 031	E	1-30B	✓	—	D3 817 008	None
1-8B, 1-9B	✓	✓	D3 817 032	A	1-31B	✓	—	D3 817 004	None
1-10B	✓	✓	D3 817 033	E	1-31B	✓	—	D3 817 005	None
1-11B	✓	✓	D3 817 032	A	1-32B	—	✓	D3 817 046	None
1-12B	✓	✓	D3 817 034	E	1-32B	—	✓	D3 817 047	None
1-13B	✓	✓	D3 817 038	None	1-33B	✓	—	D3 817 003	None
1-14B	✓	✓	D3 817 039	C	1-34B	✓	—	D3 817 010	None
1-15B	✓	✓	D3 817 037	B	1-35B	✓	—	D3 817 011	None
1-16B	✓	✓	D3 817 022	A	1-36B	✓	—	D3 817 012	A
1-17B	✓	✓	D3 817 022	A	1-37B	✓	—	D3 817 009	None
1-18B	✓	✓	D3 817 042	E	1-37B	—	✓	D3 817 051	None
1-19B	✓	✓	D3 817 041	B	1-38B	✓	—	D3 817 014	None
1-20B	✓	✓	D3 817 026	A	1-39B	✓	—	D3 817 013	None
1-21B	✓	✓	D3 817 023	D	1-40B	—	✓	D3 817 057	None
1-21B	✓	✓	D3 817 024	None	1-40B	—	✓	D3 817 053	None
1-22B	✓	✓	D3 817 025	None	1-41B	✓	✓	D3 816 799	None
1-23B	✓	✓	D3 817 027	None					

Table 1-3. Engineering-Drawing Sources for Model 139

Volume 1B Drawing Numbers	Engineering-Drawing Source		Volume 1B Drawing Numbers	Engineering-Drawing Source	
	Number	Revision		Number	Revision
1-1B	D3 815 093	None	1-12B	D3 815 097	None
1-2B	D3 815 080	K	1-13B	D3 815 101	None
1-3B	D3 815 081	None	1-14B	D3 815 102	D
1-3B	D3 815 082	None	1-15B	D3 815 100	None
1-4B	D3 815 083	F	1-16B, 1-17B	D3 815 085	None
1-5B	D3 815 103	J	1-18B	D3 815 105	G
1-6B	D3 815 091	None	1-19B	D3 815 104	None
1-7B	D3 815 092	None	1-20B	D3 815 089	F
1-8B	D3 815 094	None	1-21B	D3 815 086	E
1-8B	D3 815 095	None	1-21B	D3 815 087	A
1-9B	D3 820 626	E	1-22B	D3 815 088	D
1-10B	D3 815 096	None	1-23B	D3 815 090	C
1-11B	D3 820 626	E	1-24B	D3 815 098	None

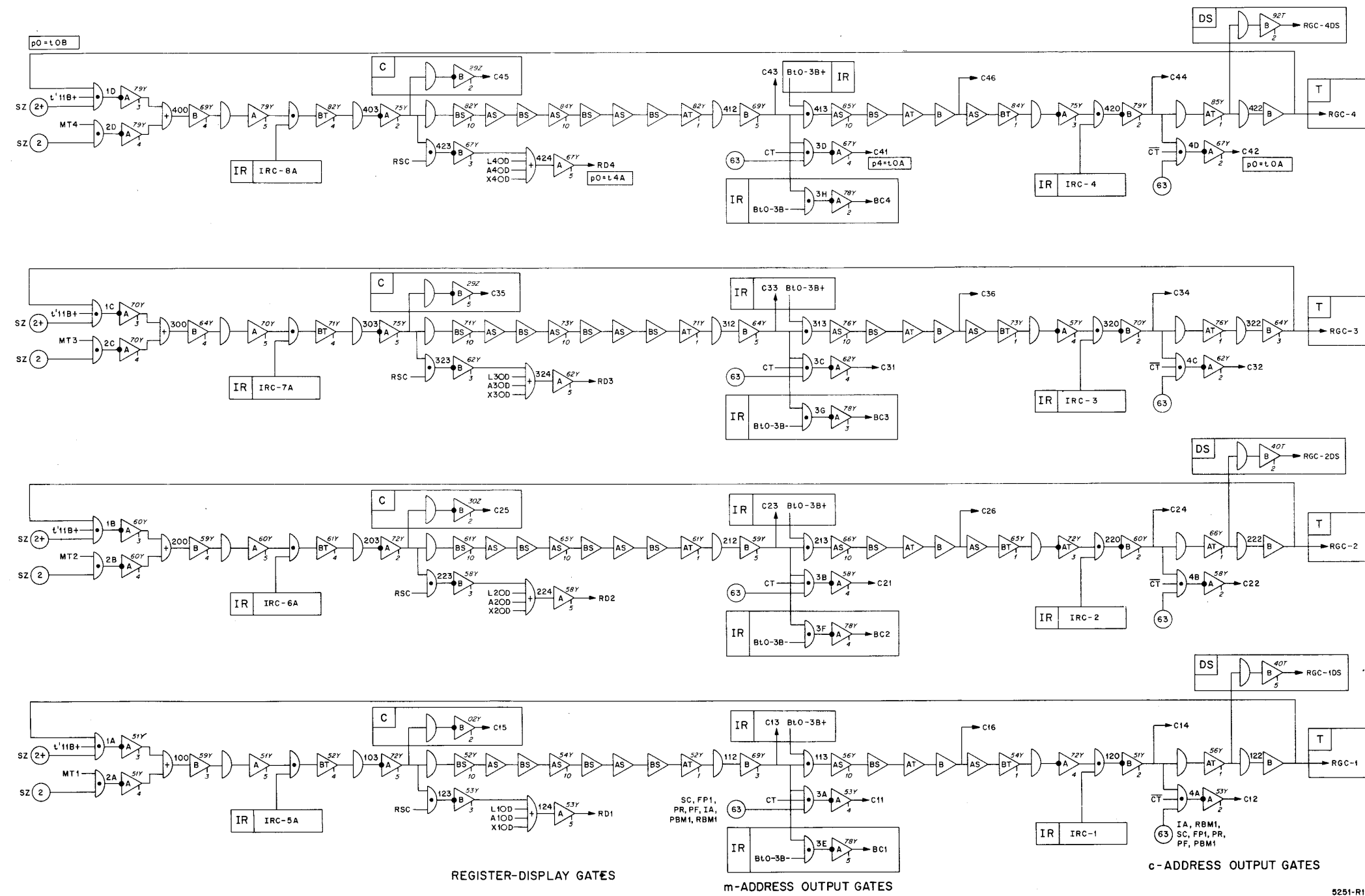
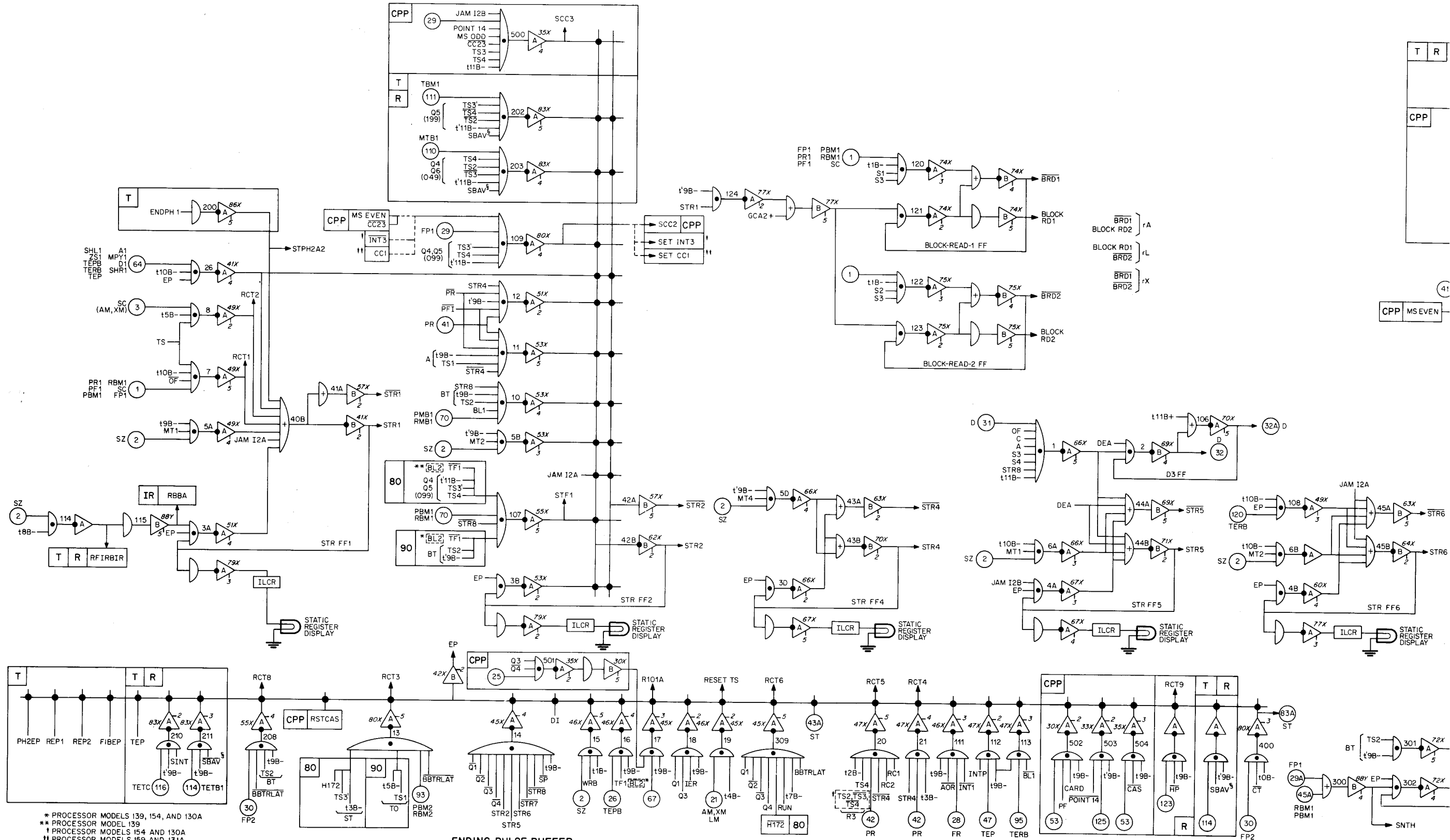


Figure 1-1B. Register C



* PROCESSOR MODELS 139, 154, AND 130A
 ** PROCESSOR MODEL 139
 † PROCESSOR MODELS 154 AND 130A
 †† PROCESSOR MODELS 159 AND 131A
 § TBLU/TBLU FOR PROCESSOR MODELS 130A AND 131A.

ENDING-PULSE BUFFER

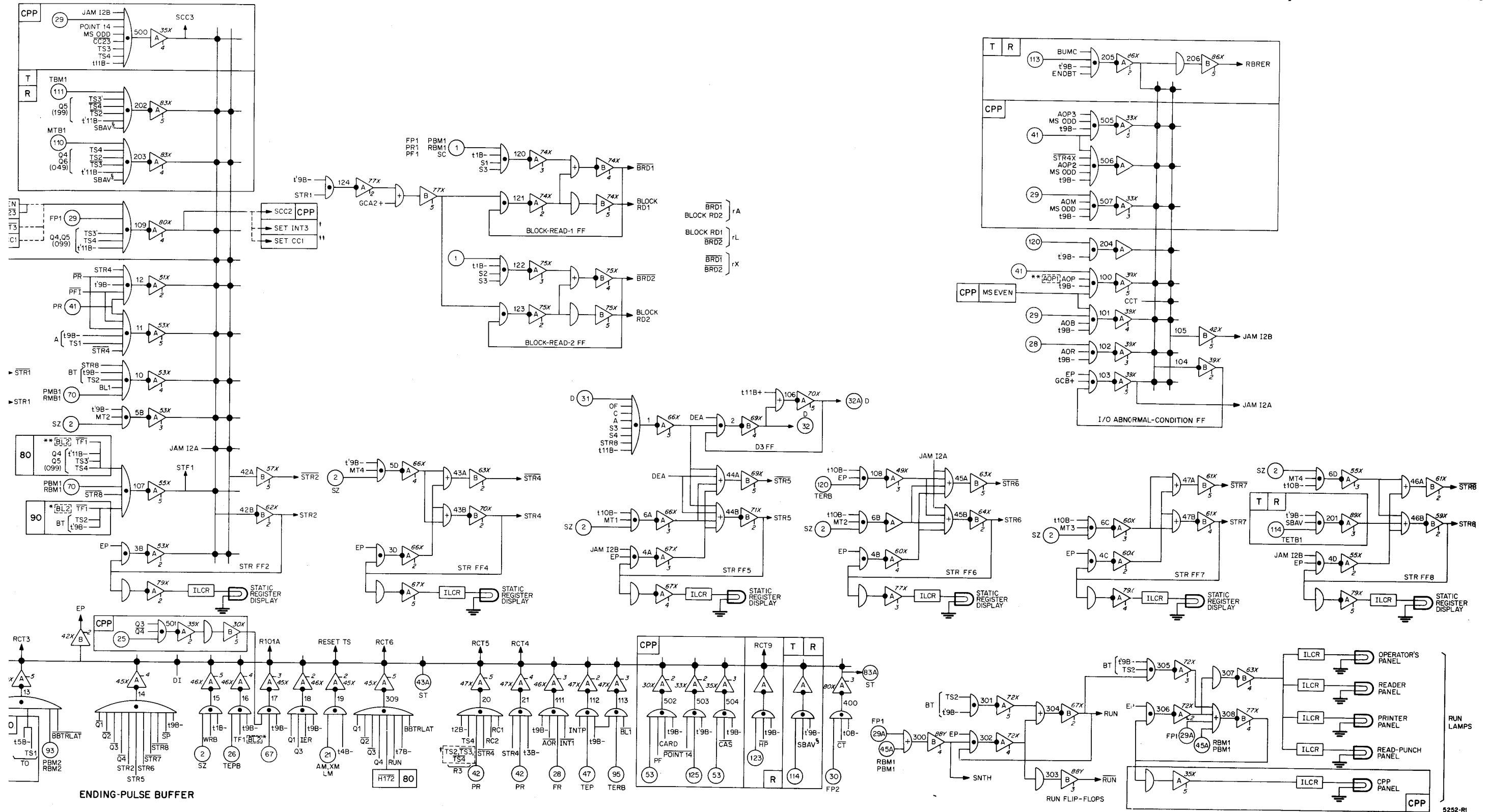
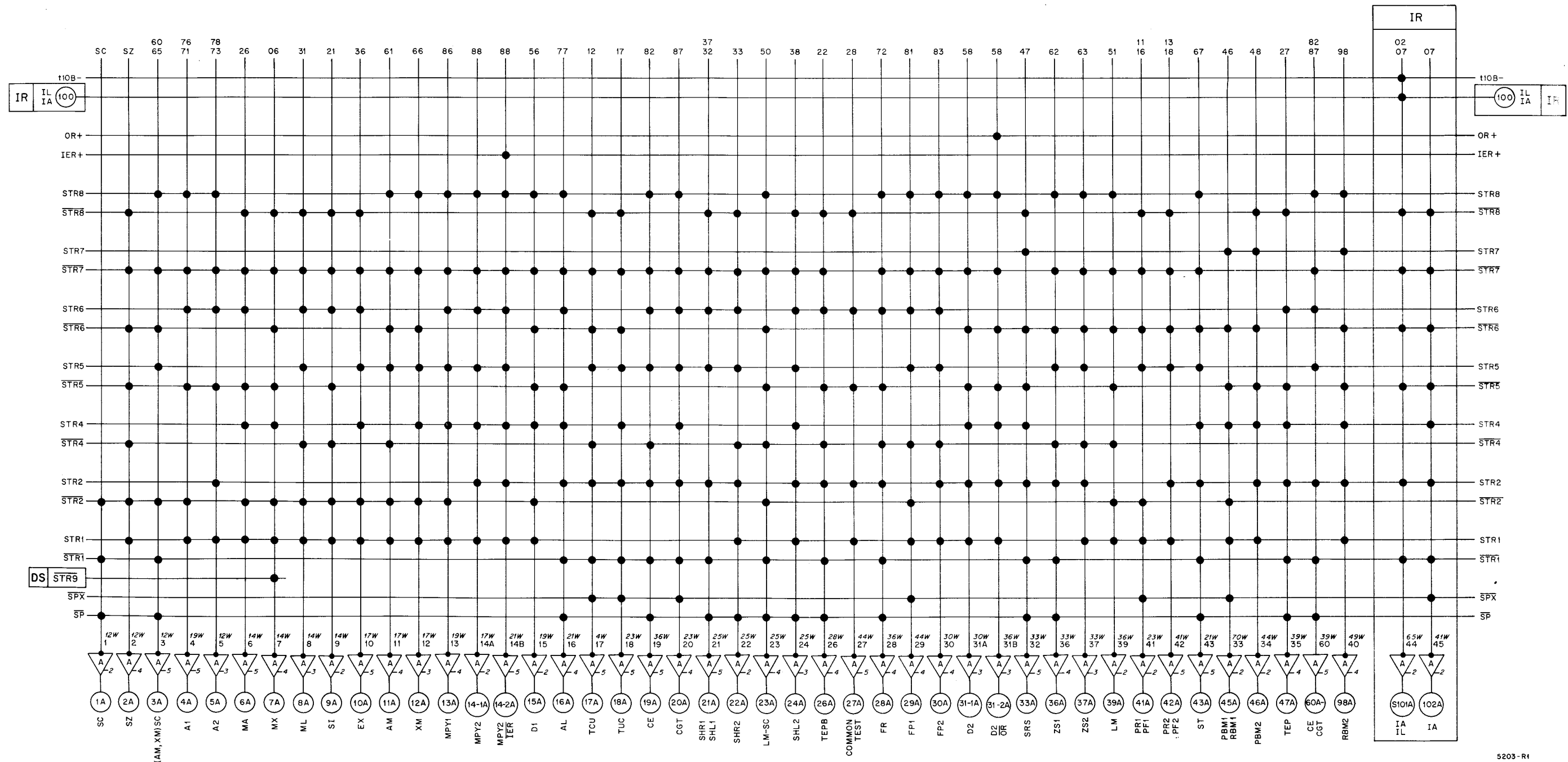
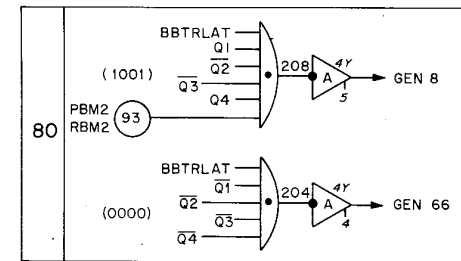
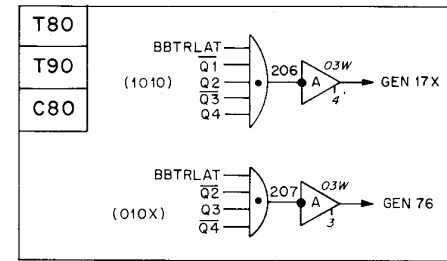
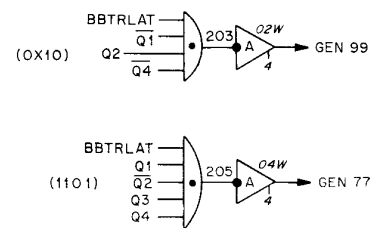
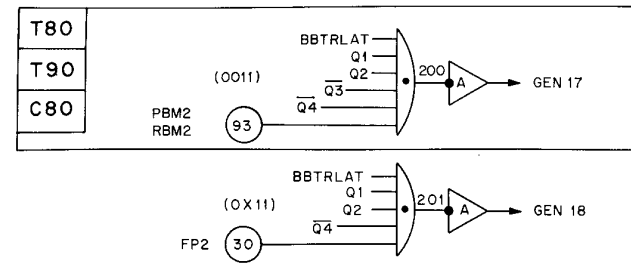


Figure 1-2B. Static Register, Models 130A, 131A, 139, 154, and 159



5203-R1

Figure 1-3B. Instruction Decoder (2 sheets)

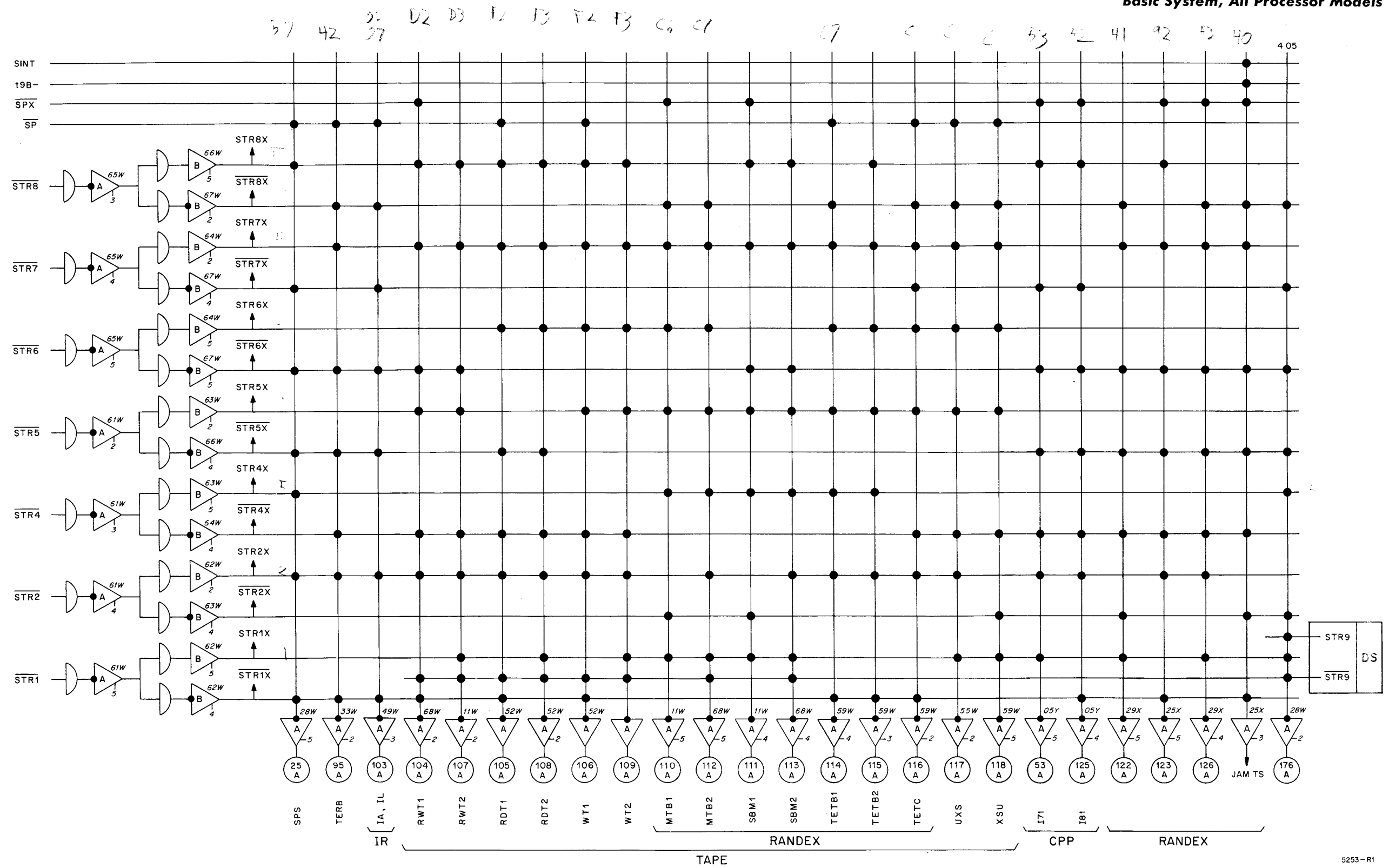
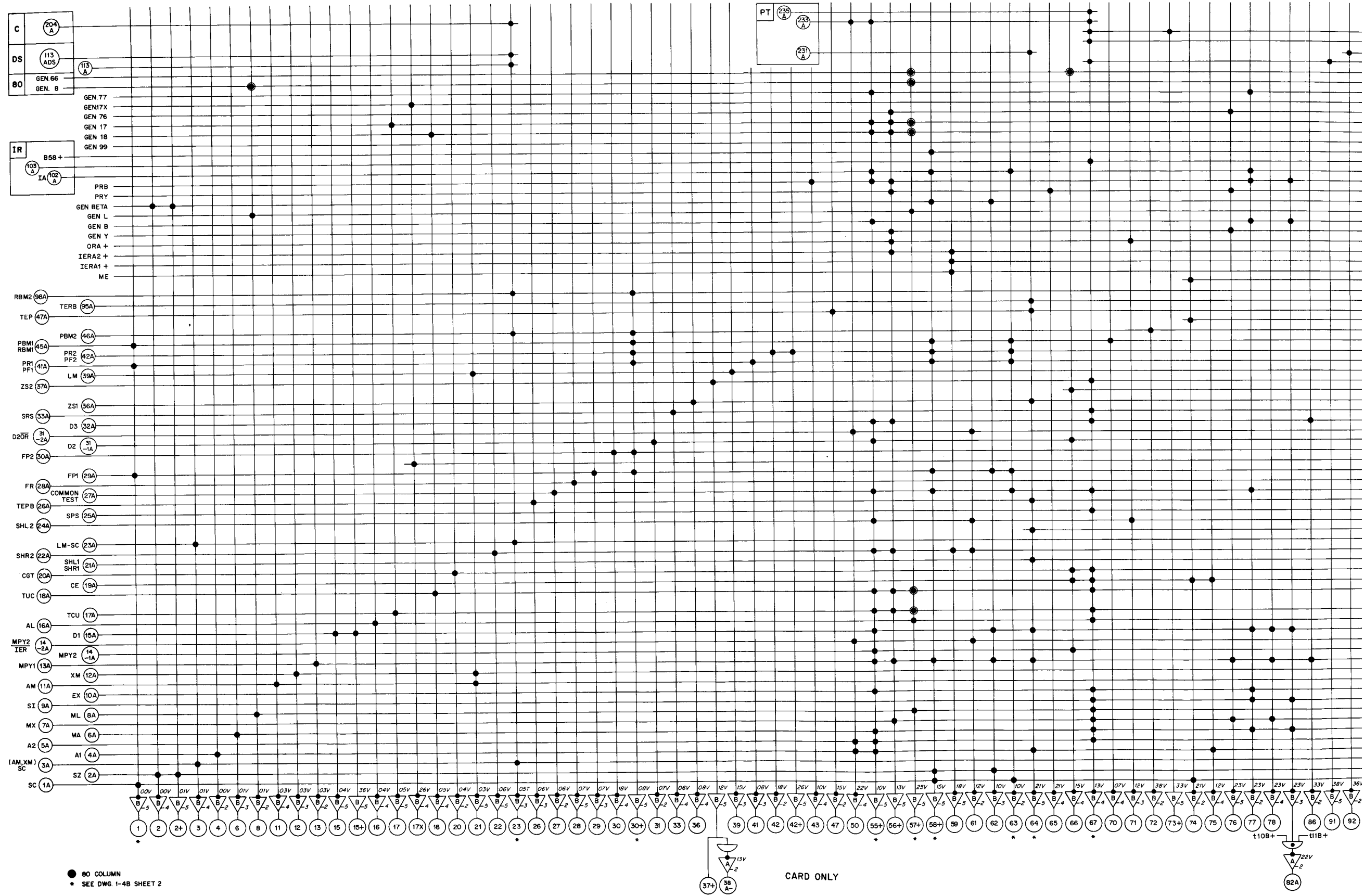


Figure 1-3B. Instruction Decoder (2 sheets)

5253-R1



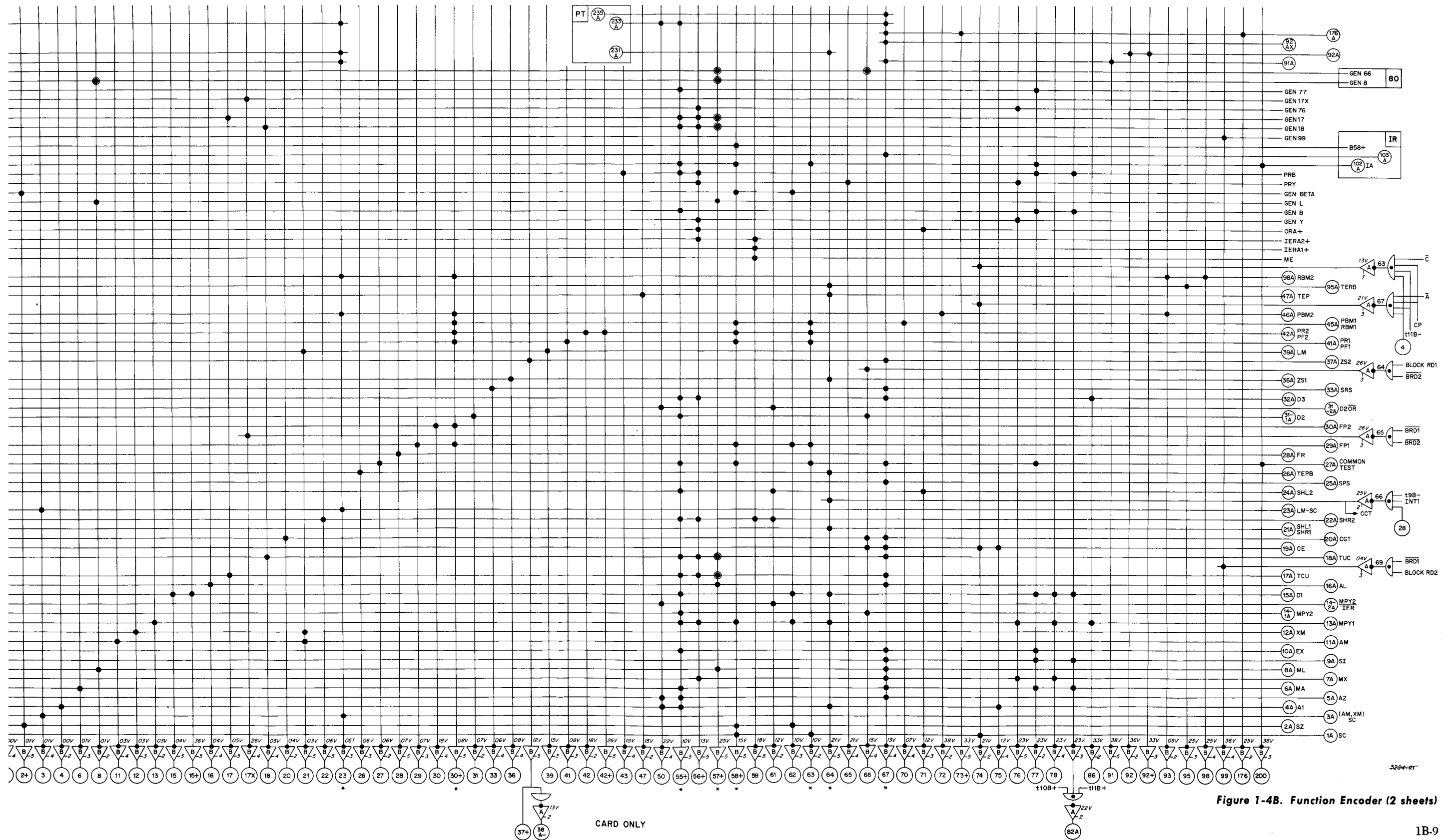
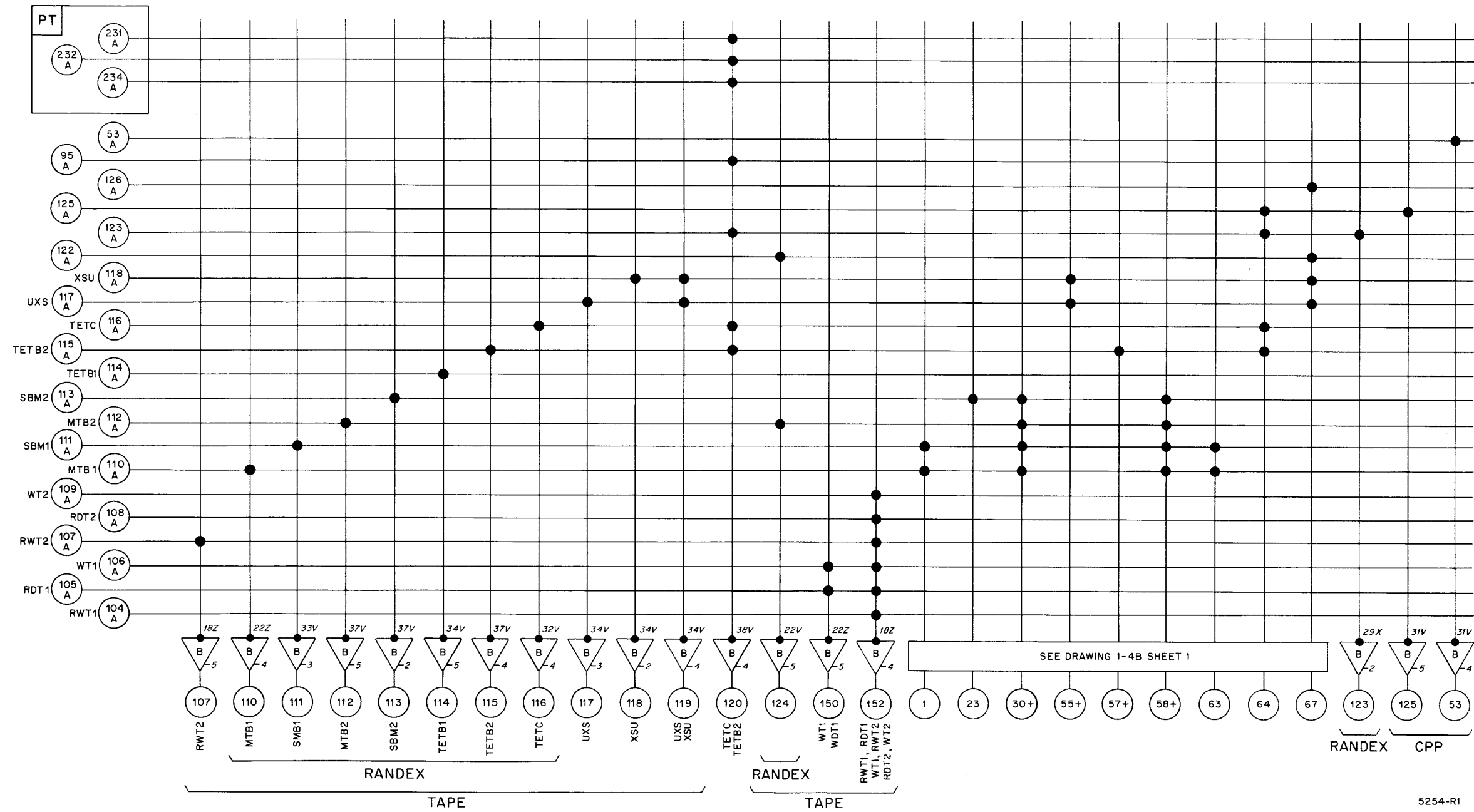
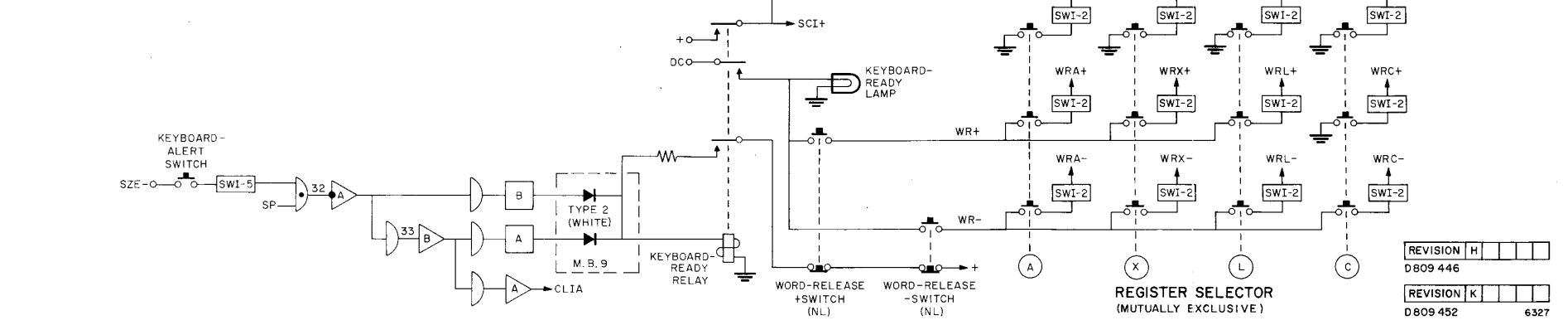
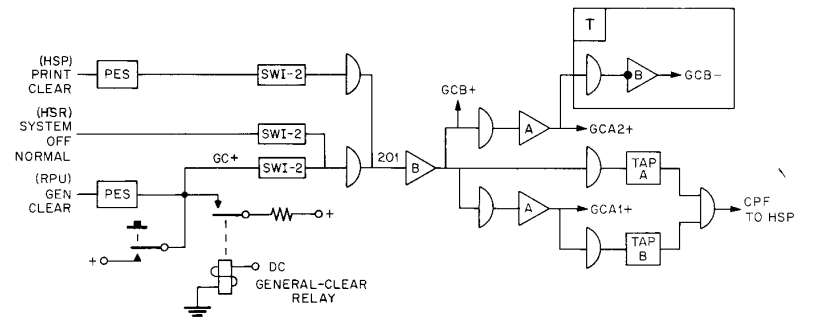
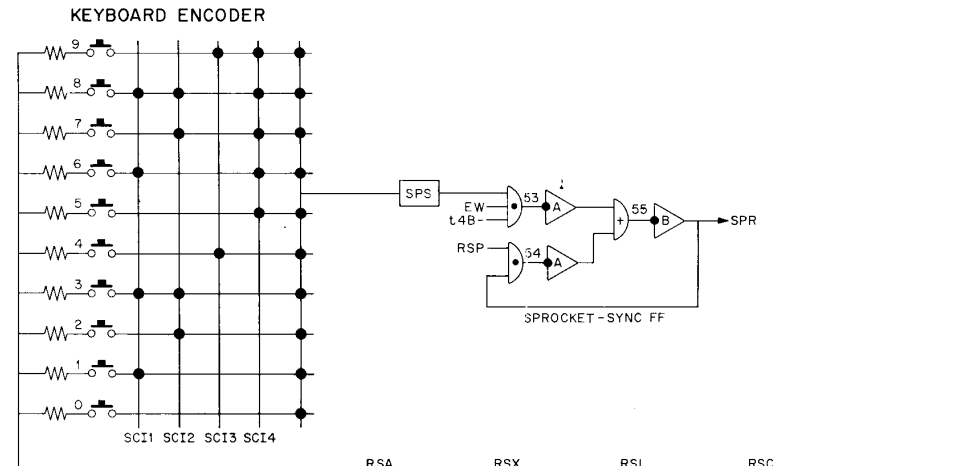
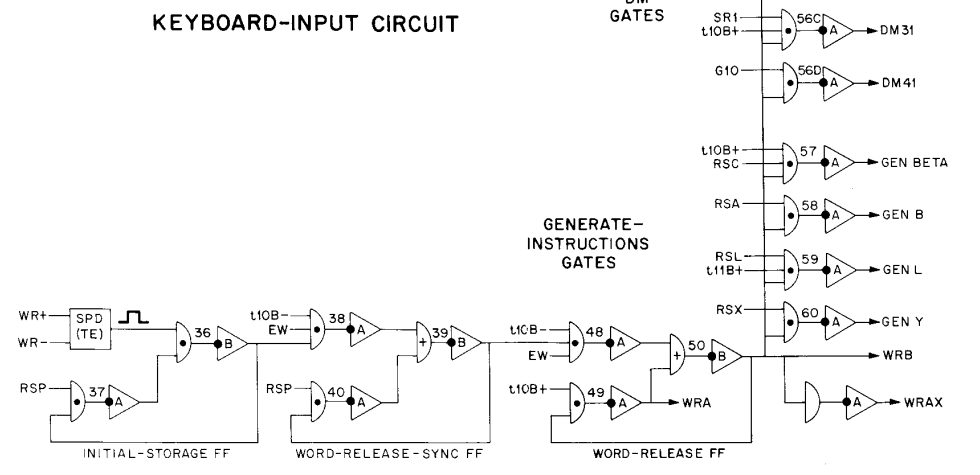
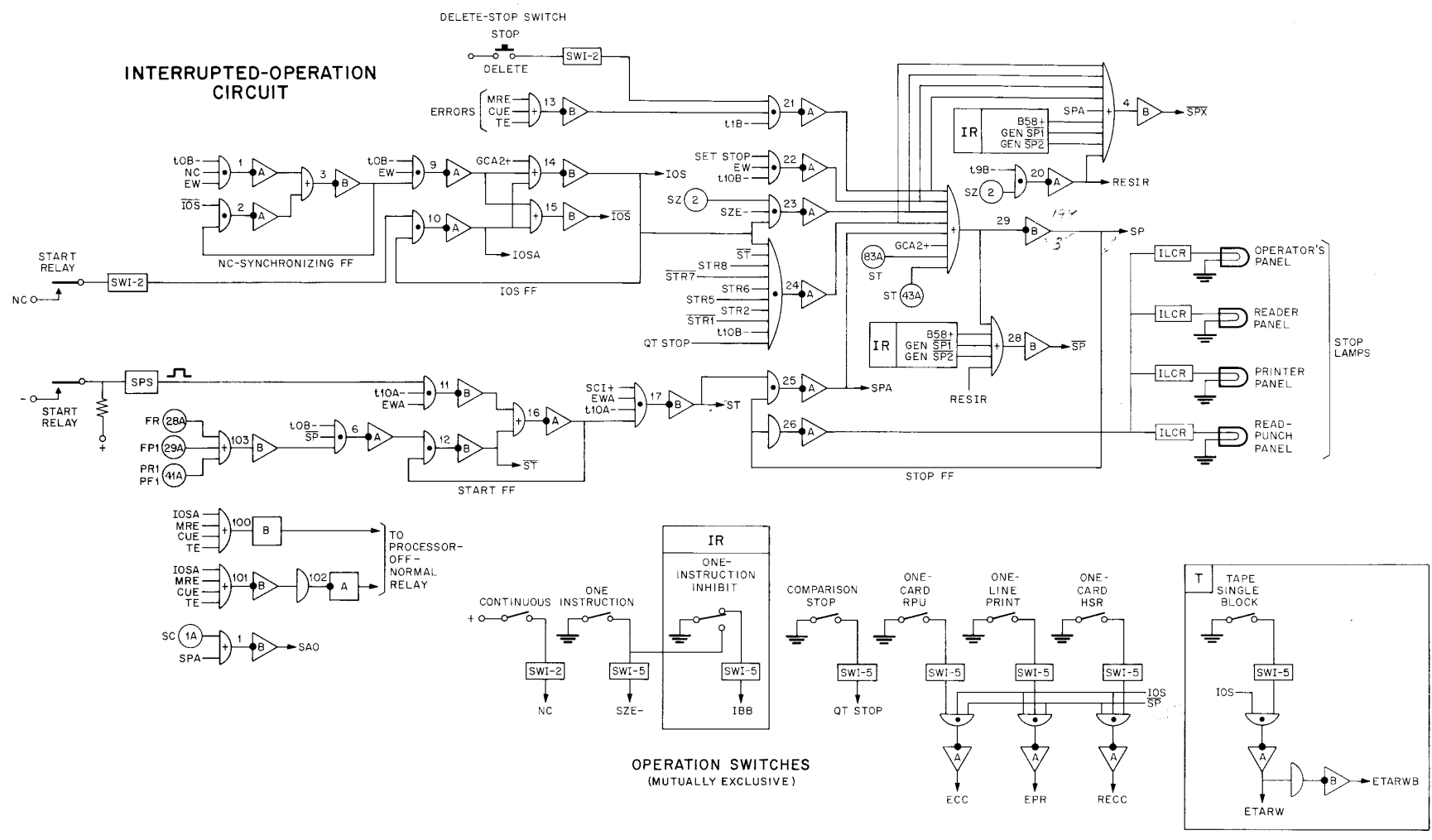


Figure 1-4B. Function Encoder (2 sheets)



5254-R1

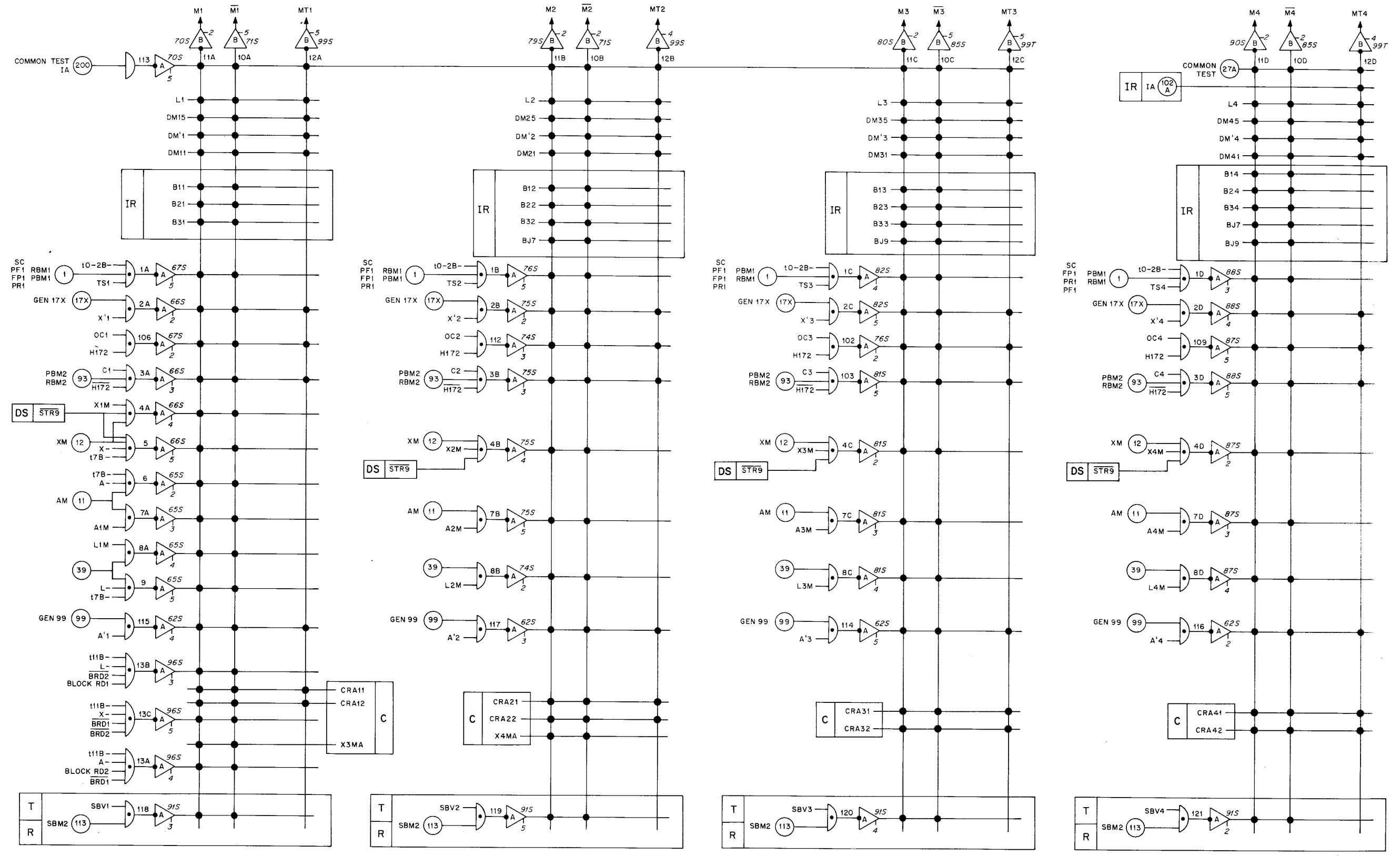
Figure 1-4B. Function Encoder (2 sheets)



Interrupted Operation (Model 130)
1-5B

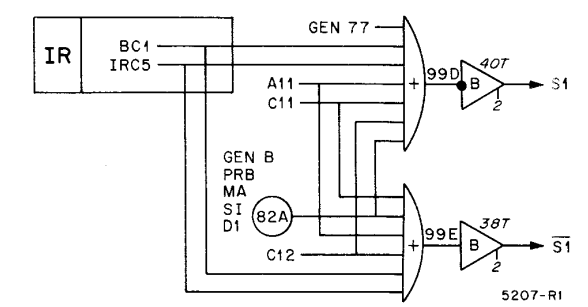
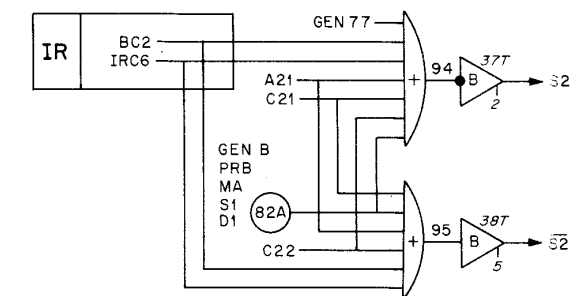
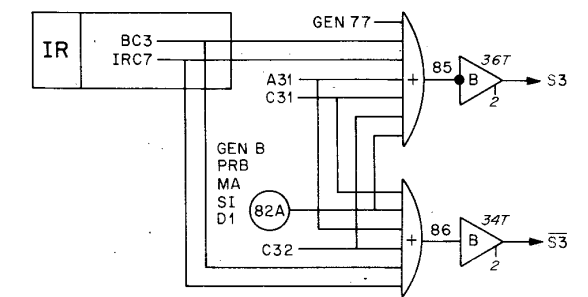
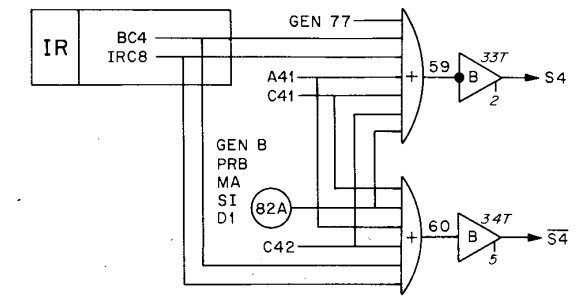
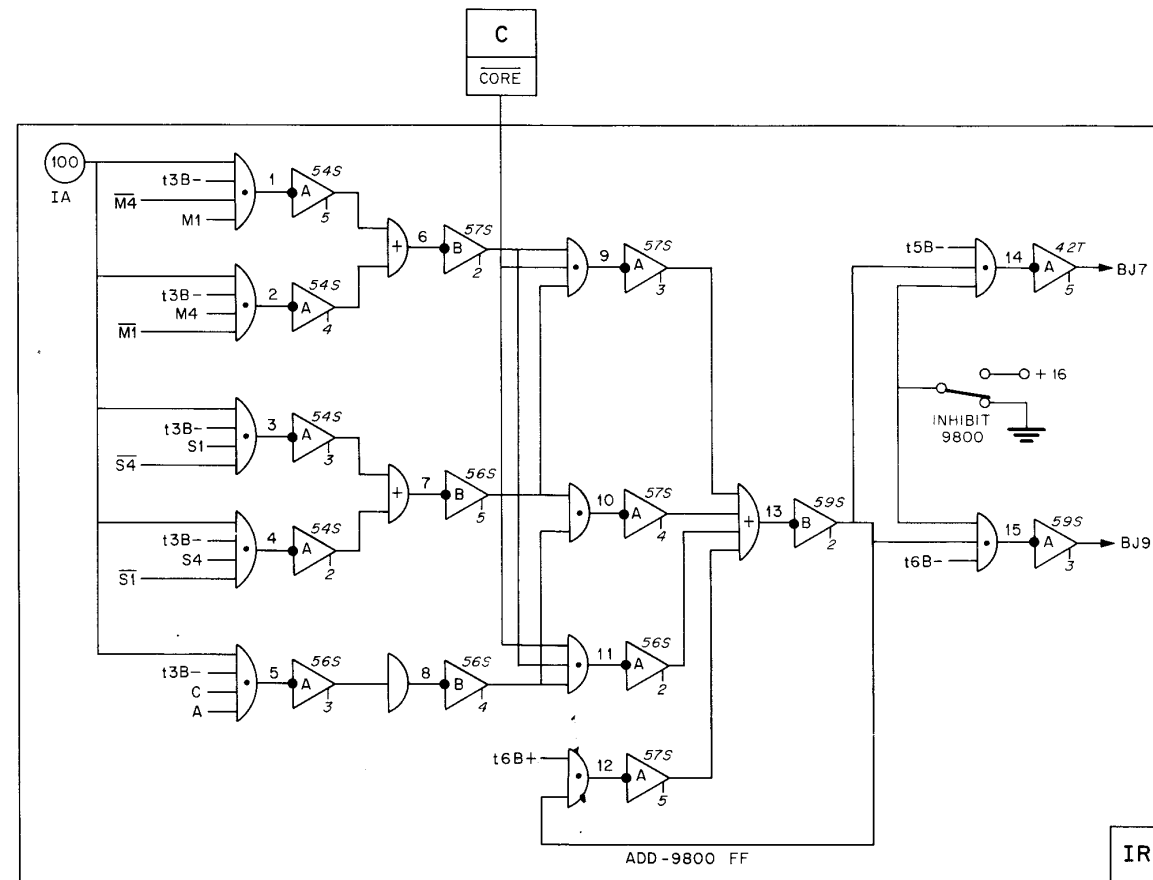
REVISION	H				
	0809	446			
REVISION	K				
	0809	452			6327

Basic System, All Processor Models



5256-R1

Figure 1-6B. M Buffer



5207-R1

Figure 1-7B. S Buffer

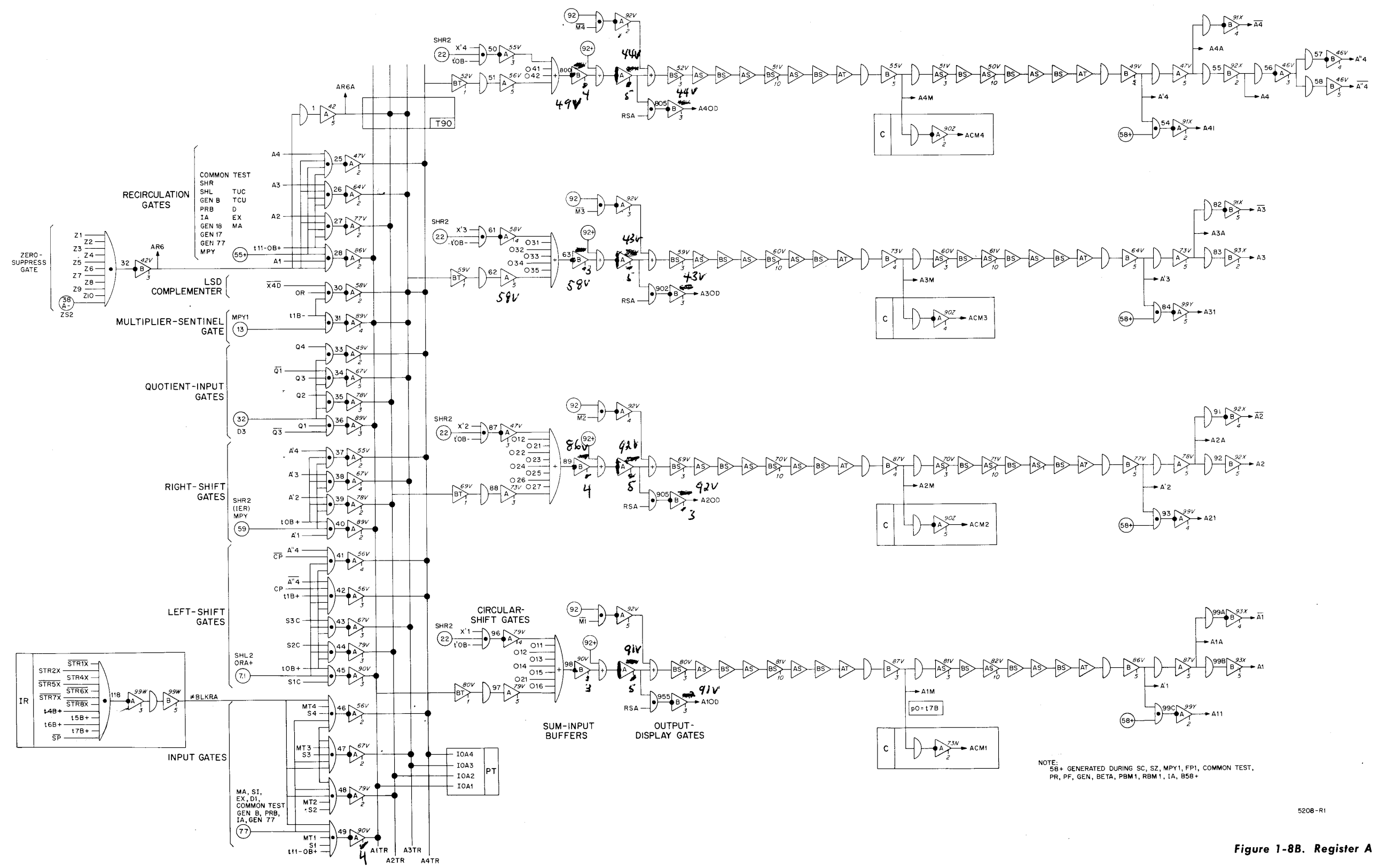


Figure 1-8B. Register A

5208-R1

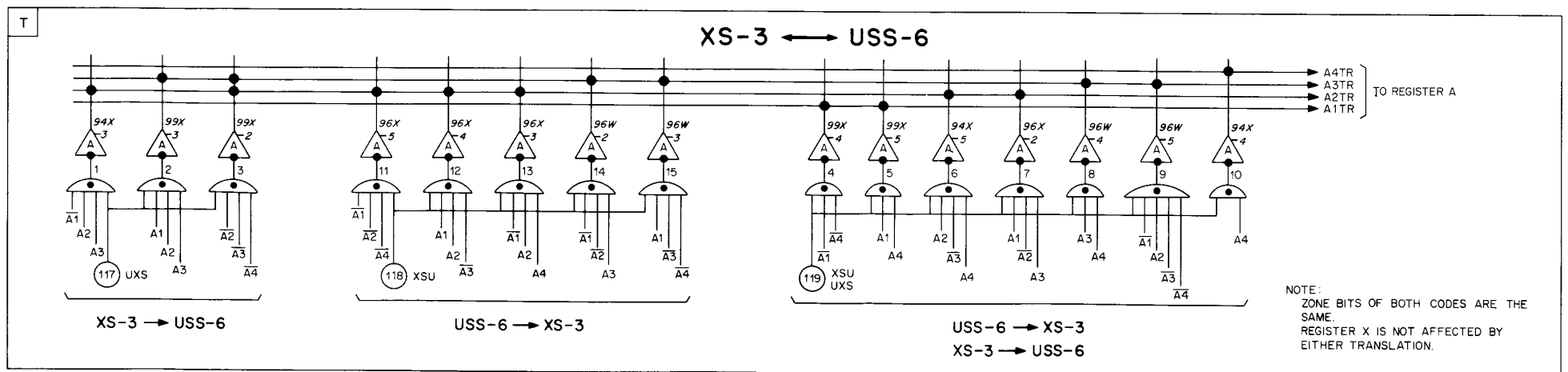
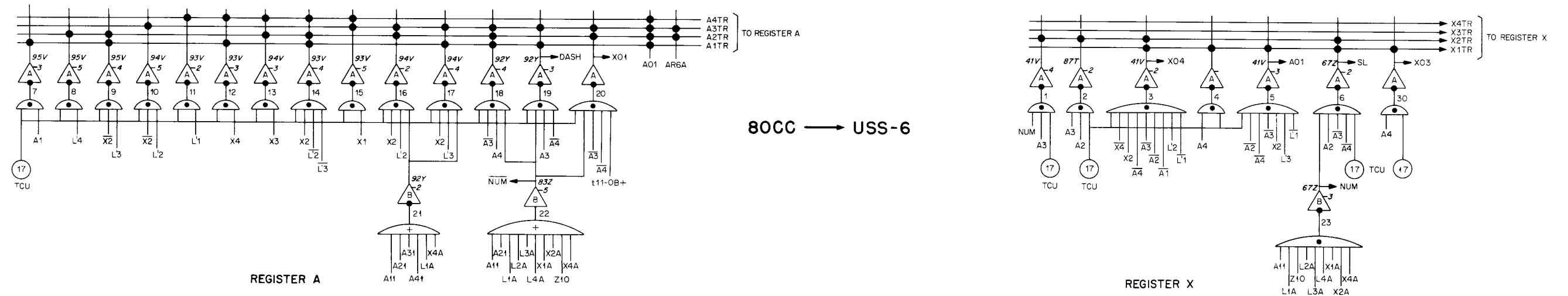
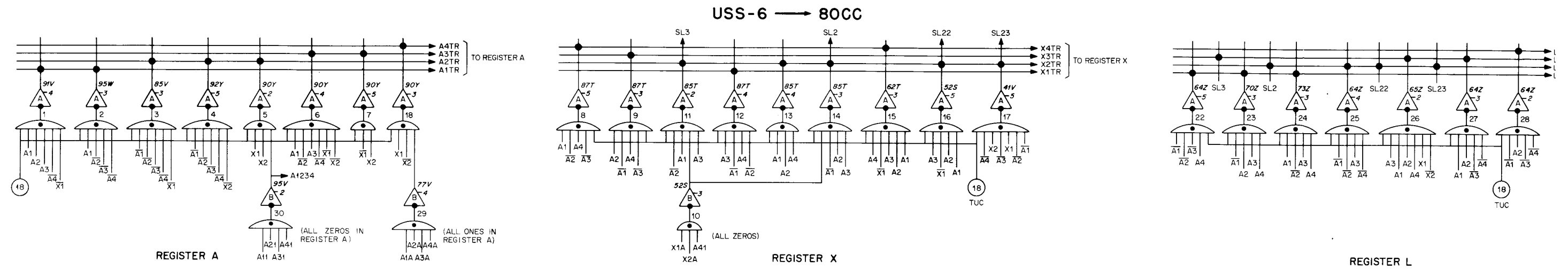


Figure 1-9B. Tr

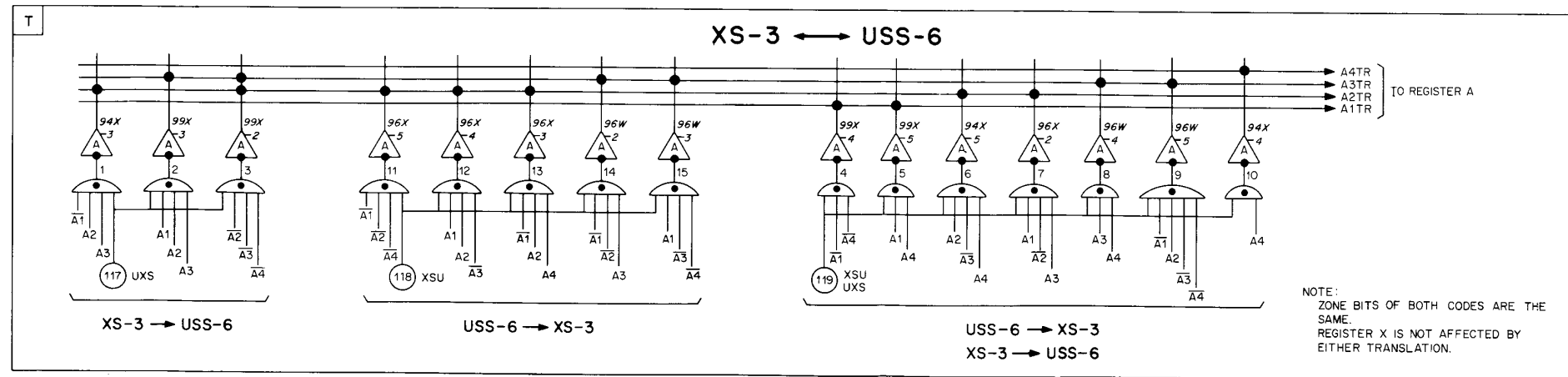
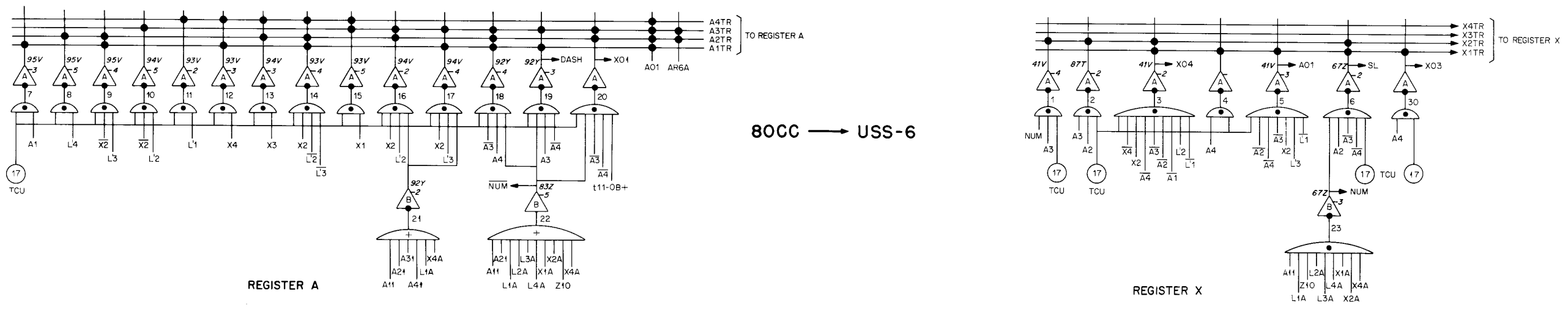
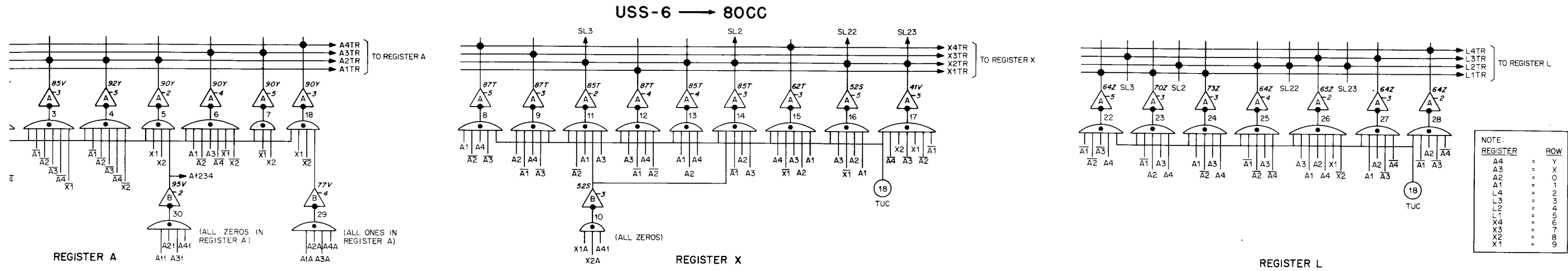
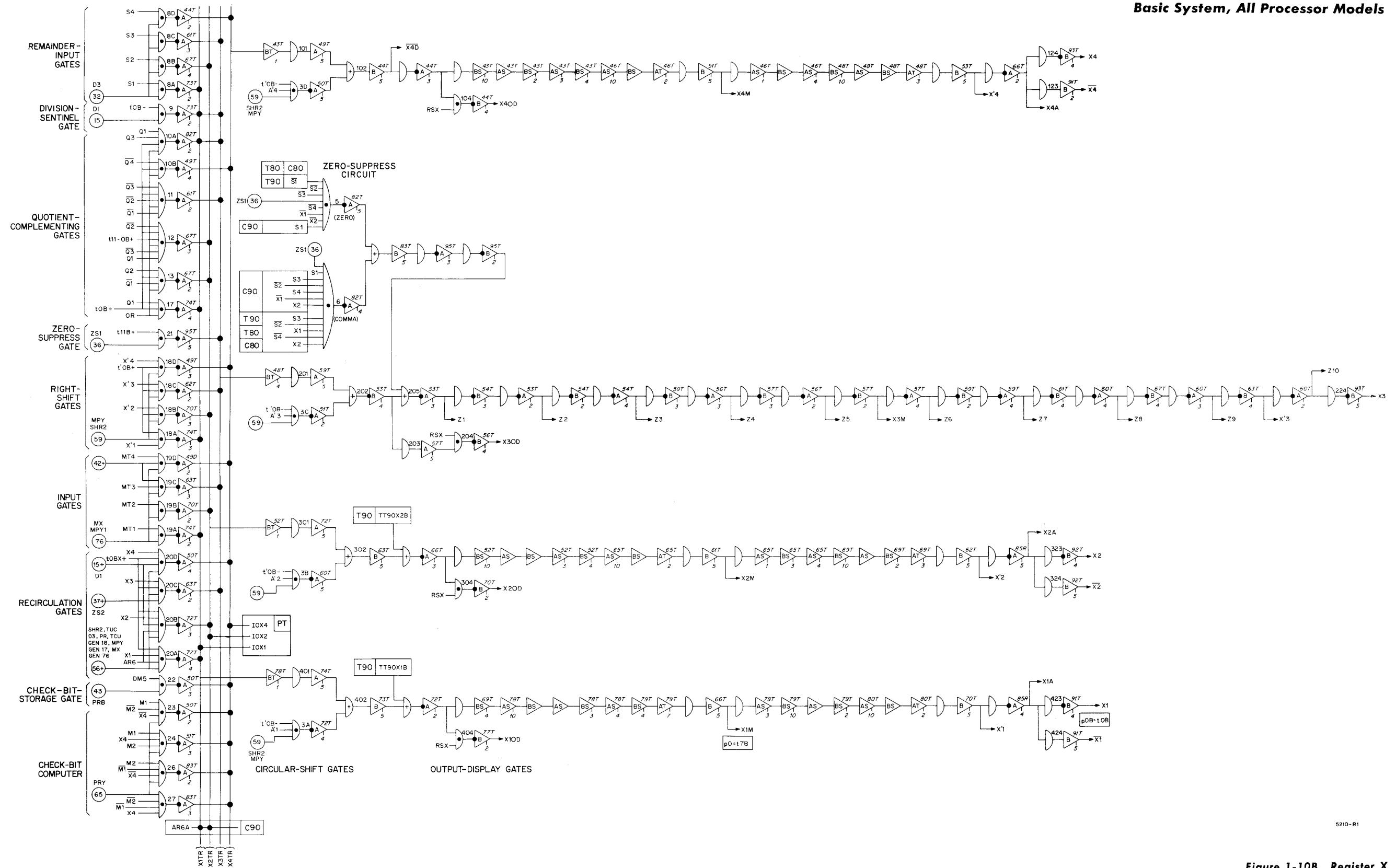


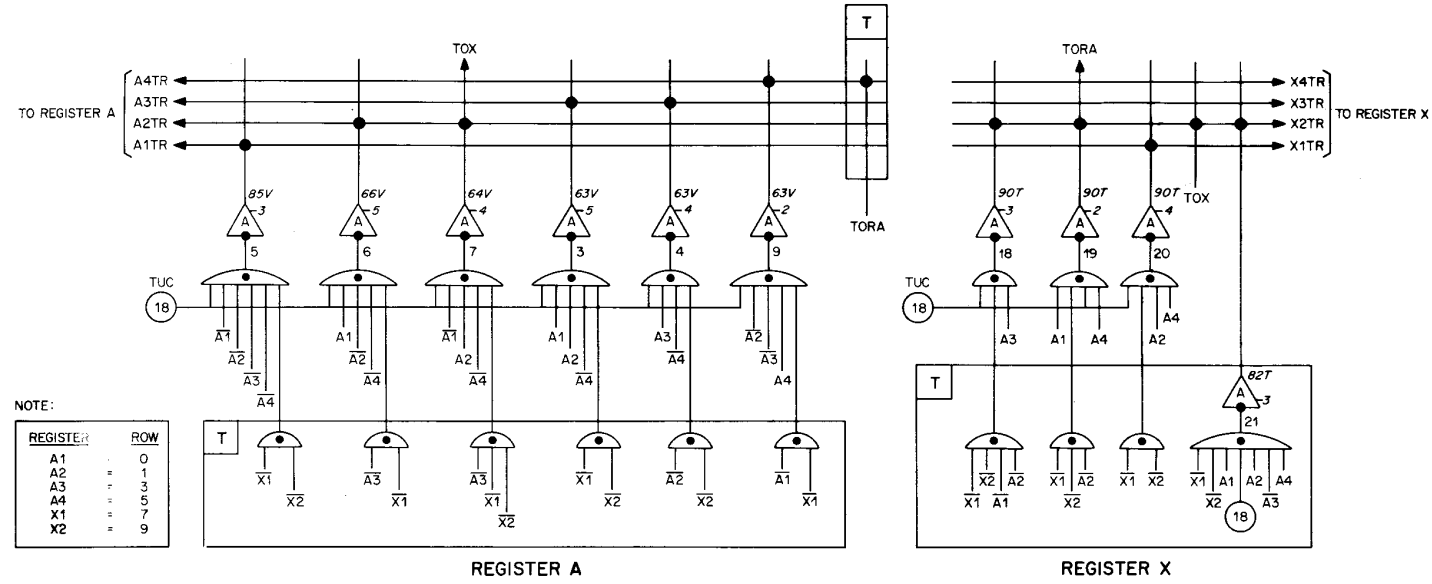
Figure 1-9B. Translate Gates, Part 1



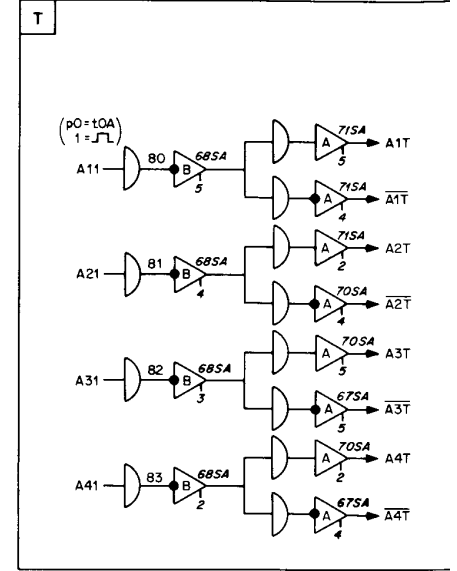
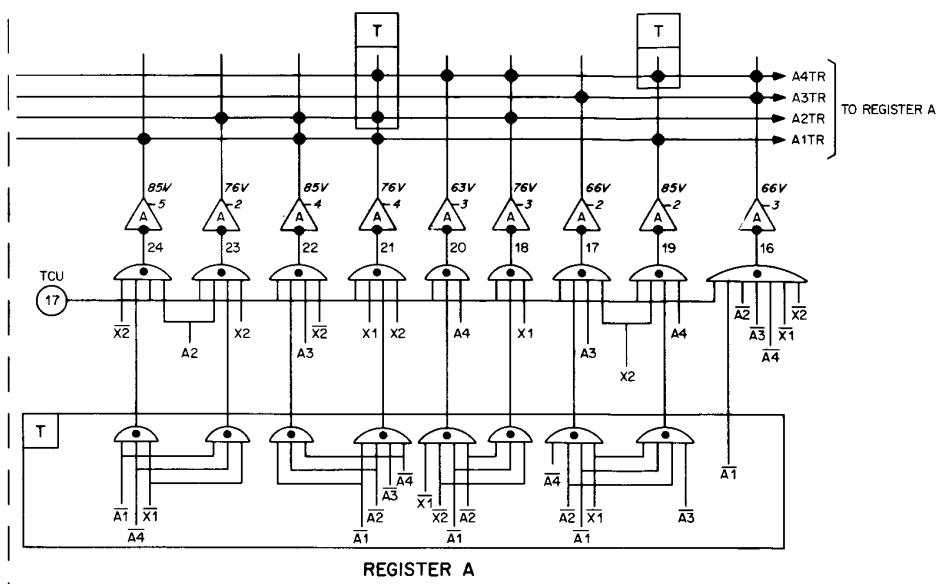
5210-R1

Figure 1-10B. Register X

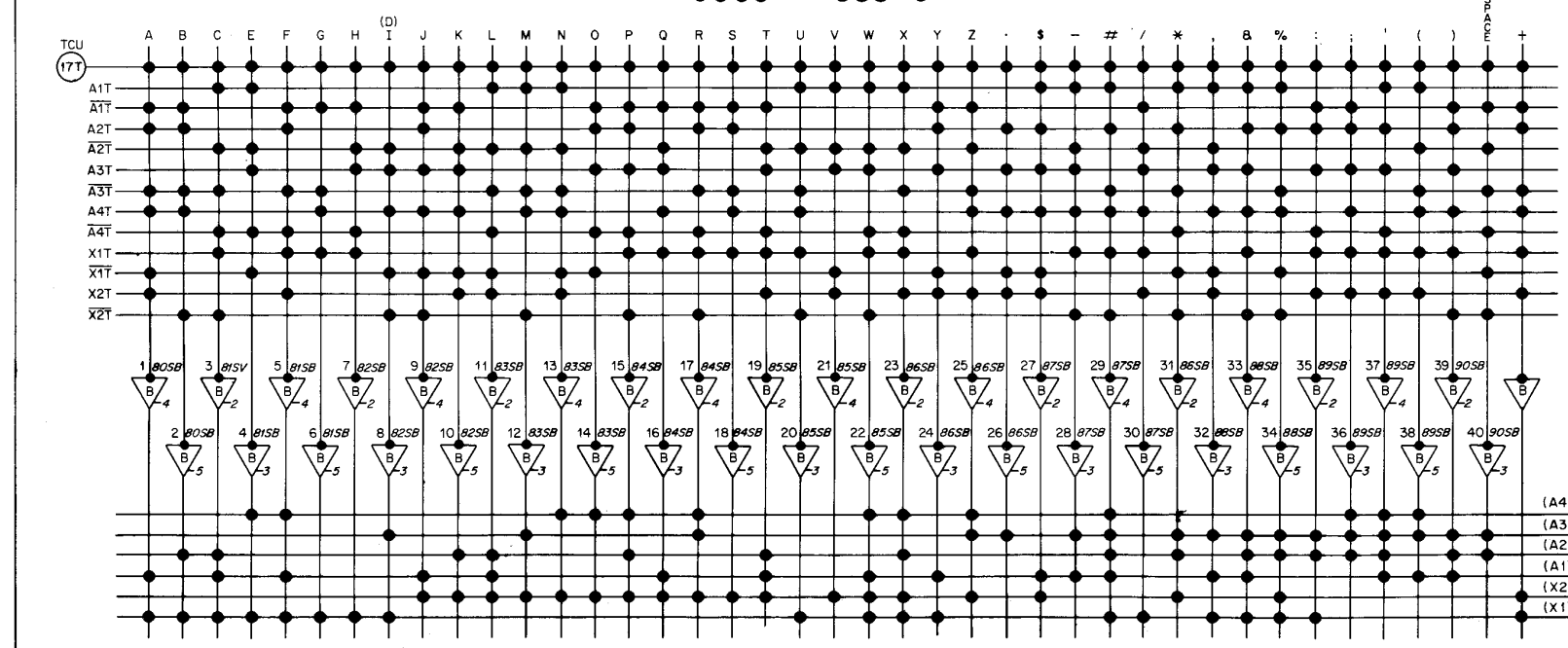
USS-6 → 90CC



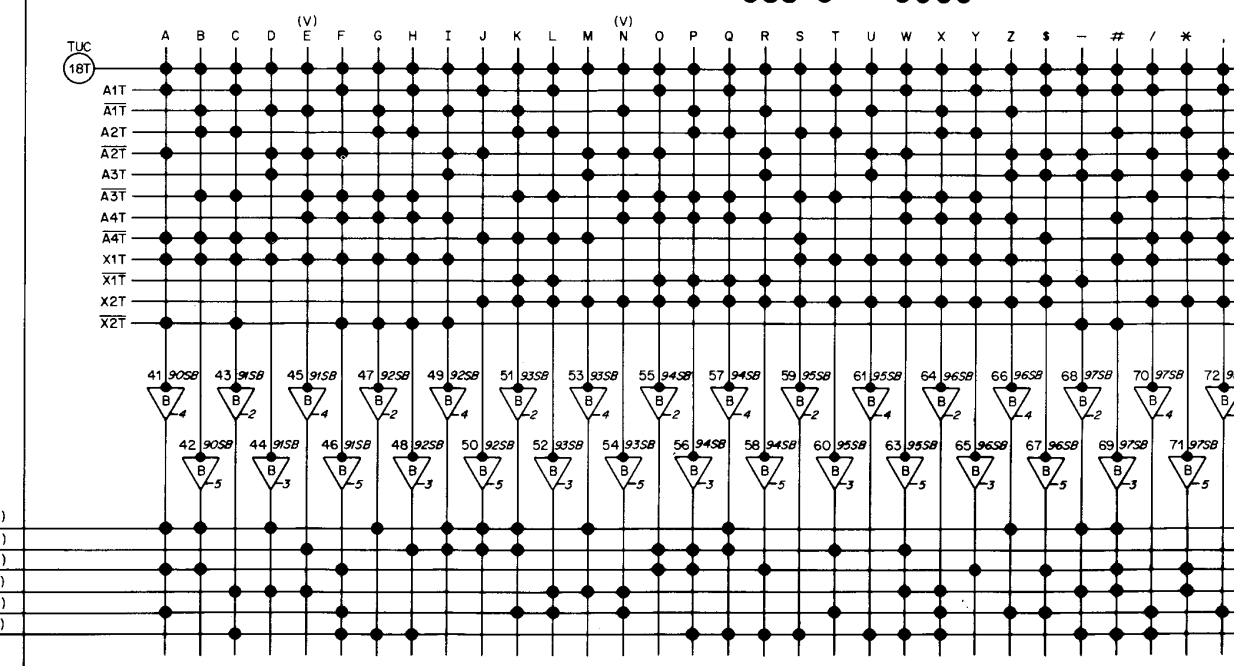
90CC → USS-6



90CC → USS-6



USS-6 → 90CC



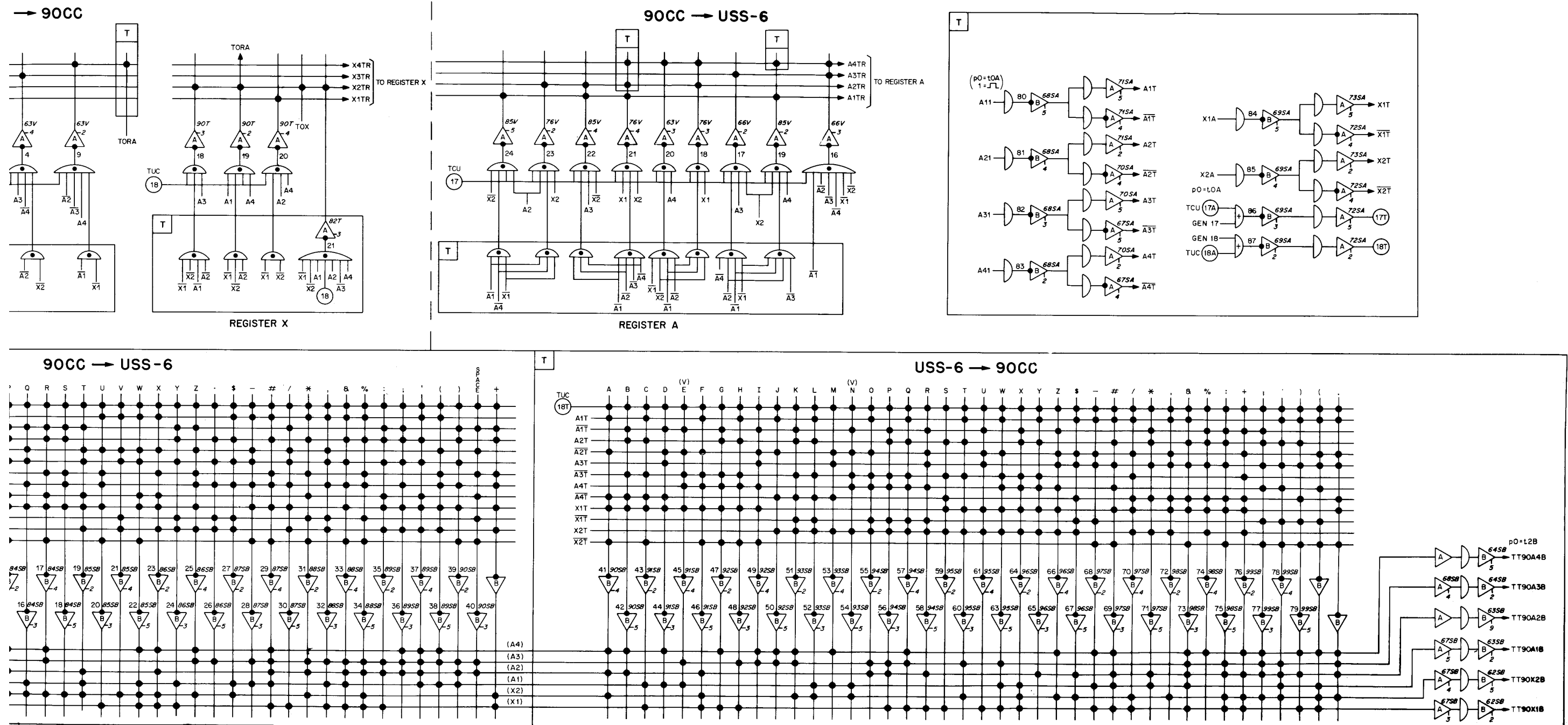


Figure 1-11B. Translate Gates, Part 2

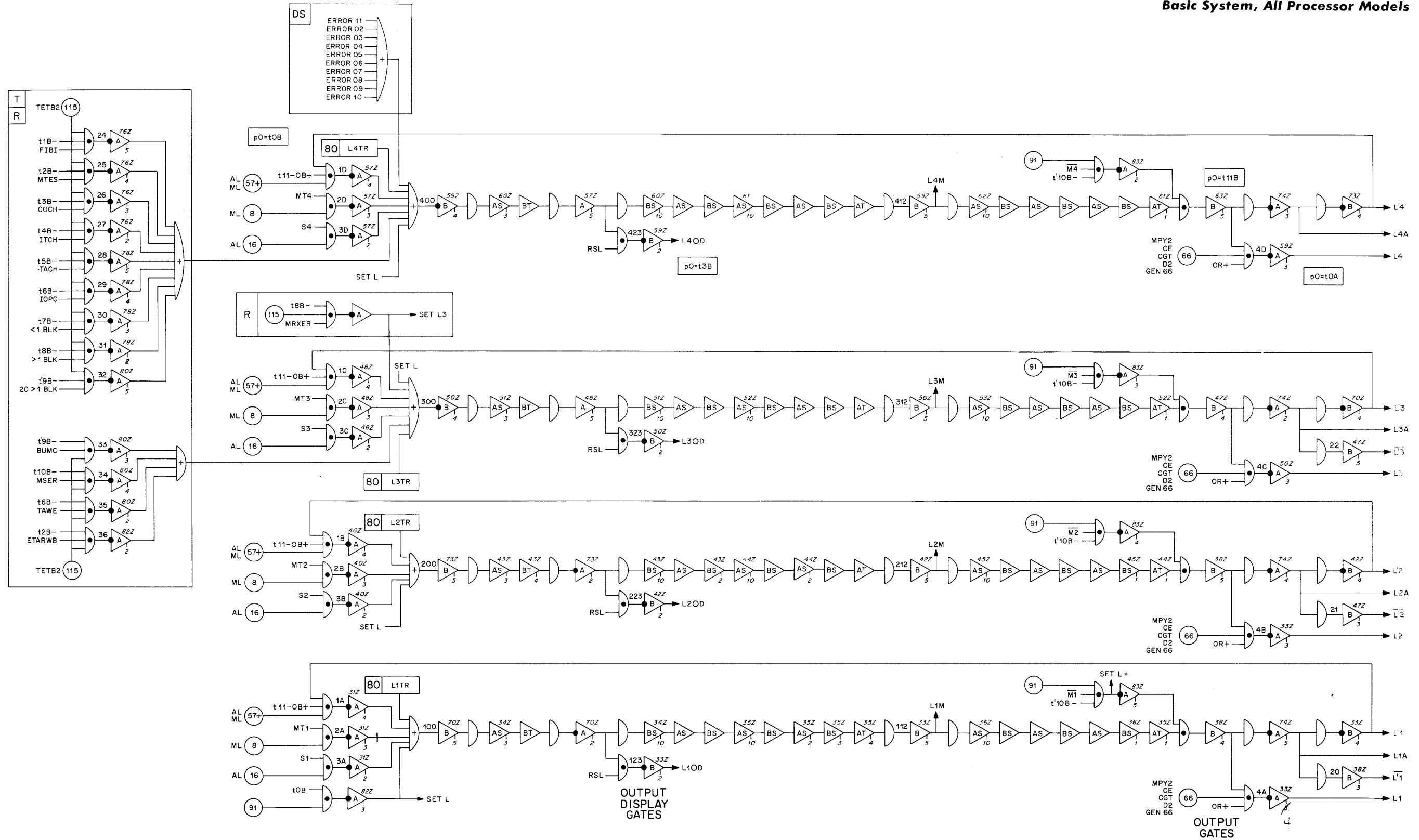
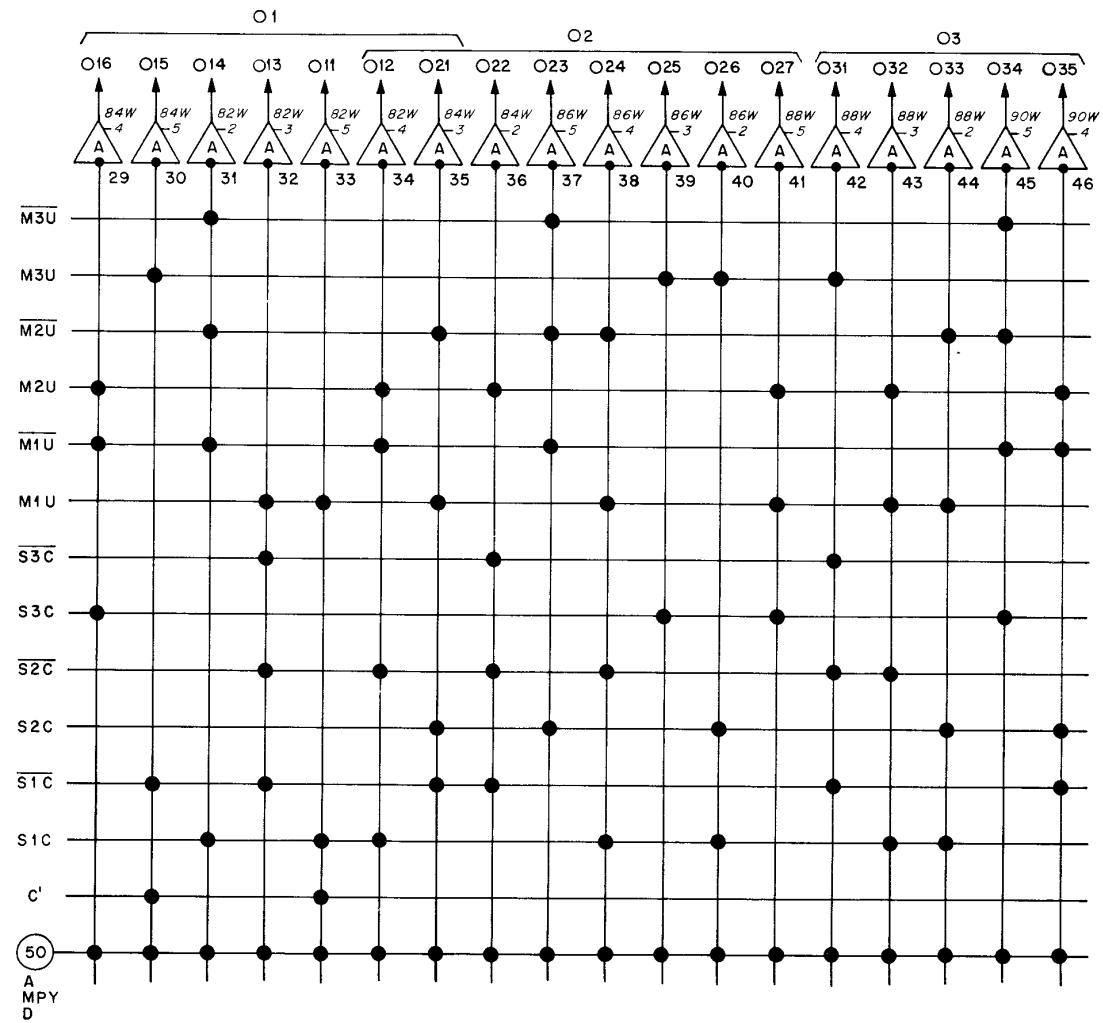
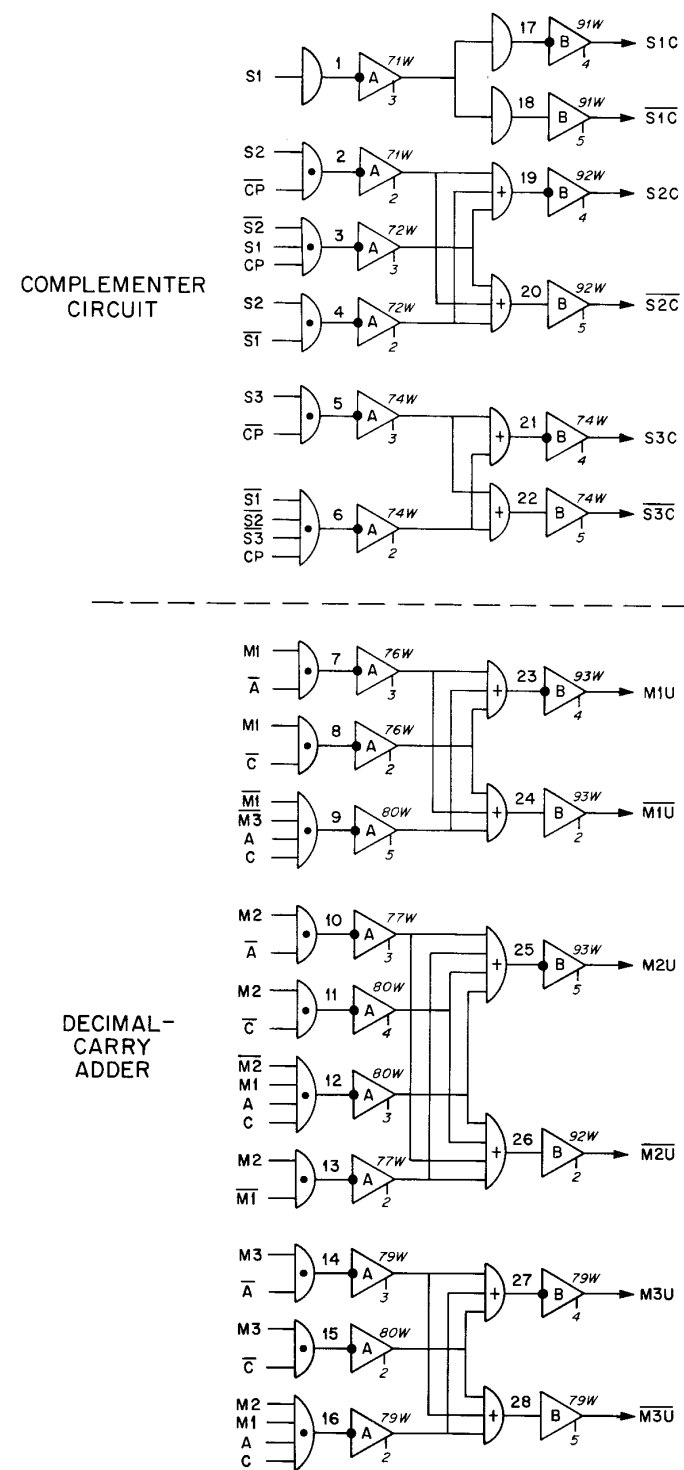


Figure 1-12B. Register L



5213

Figure 1-13B. Quinary Adder

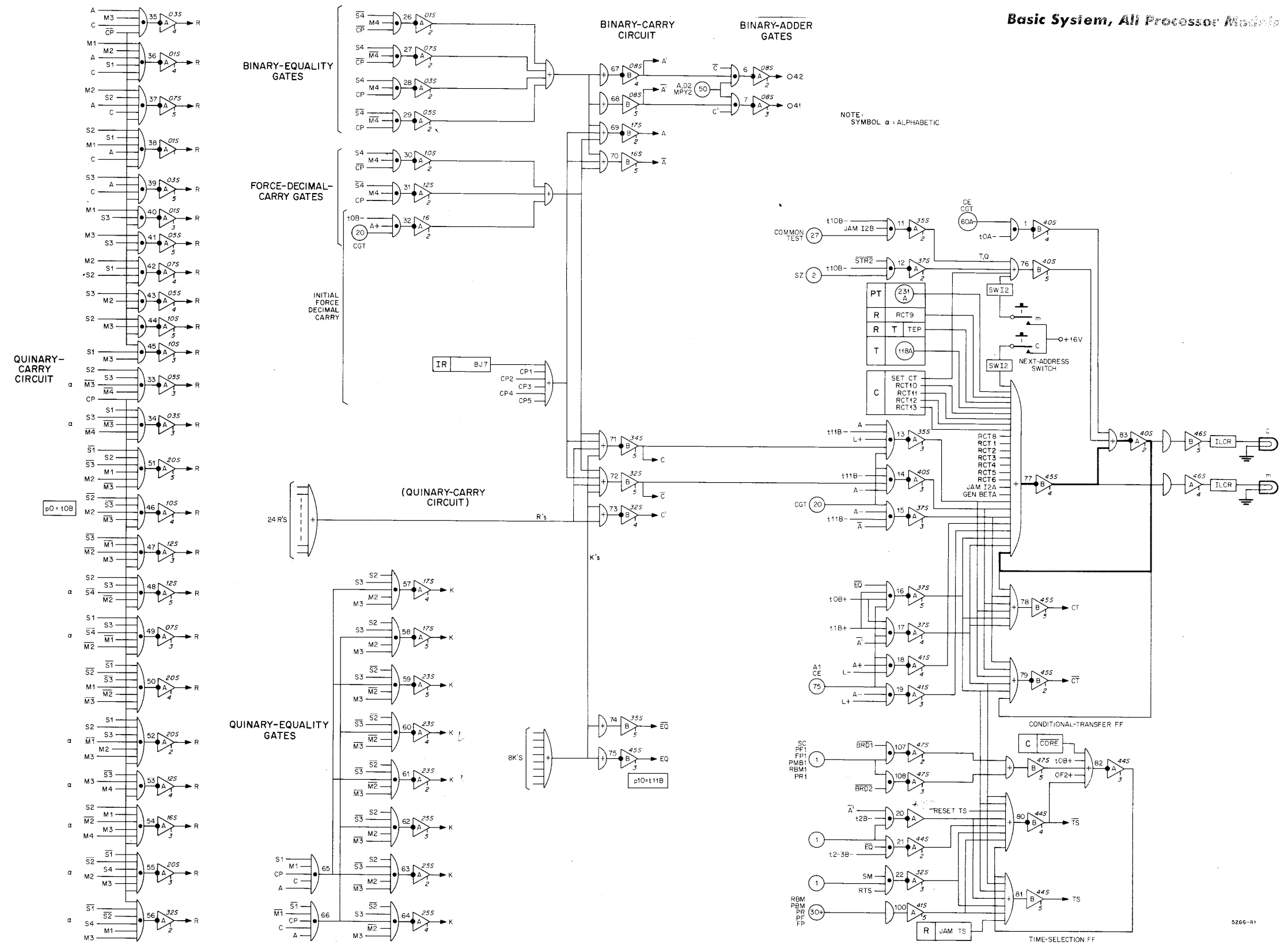
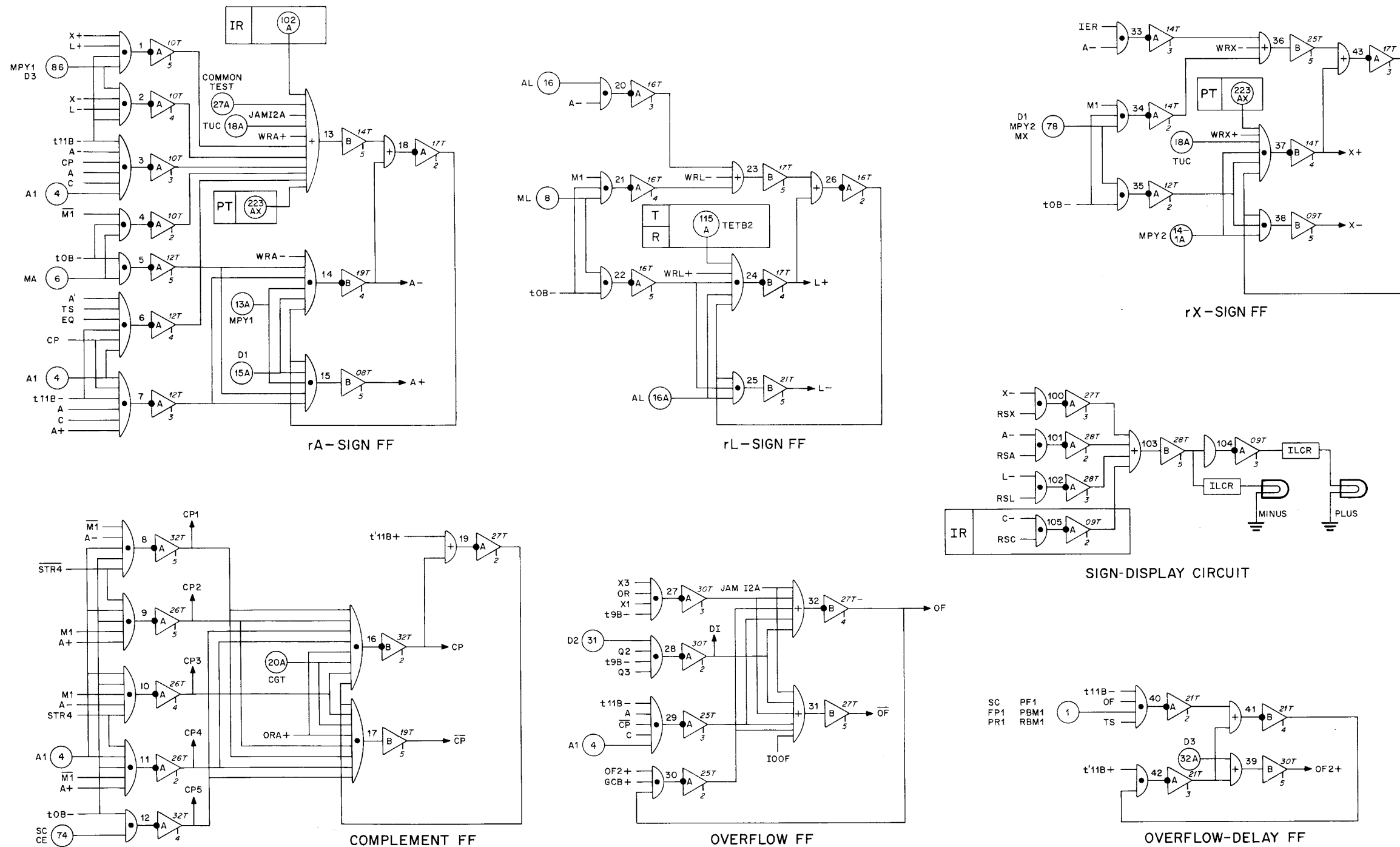


Figure 1-14B. Comparator



5260-R1

Figure 1-15B. Sign and Control Flip-Flops

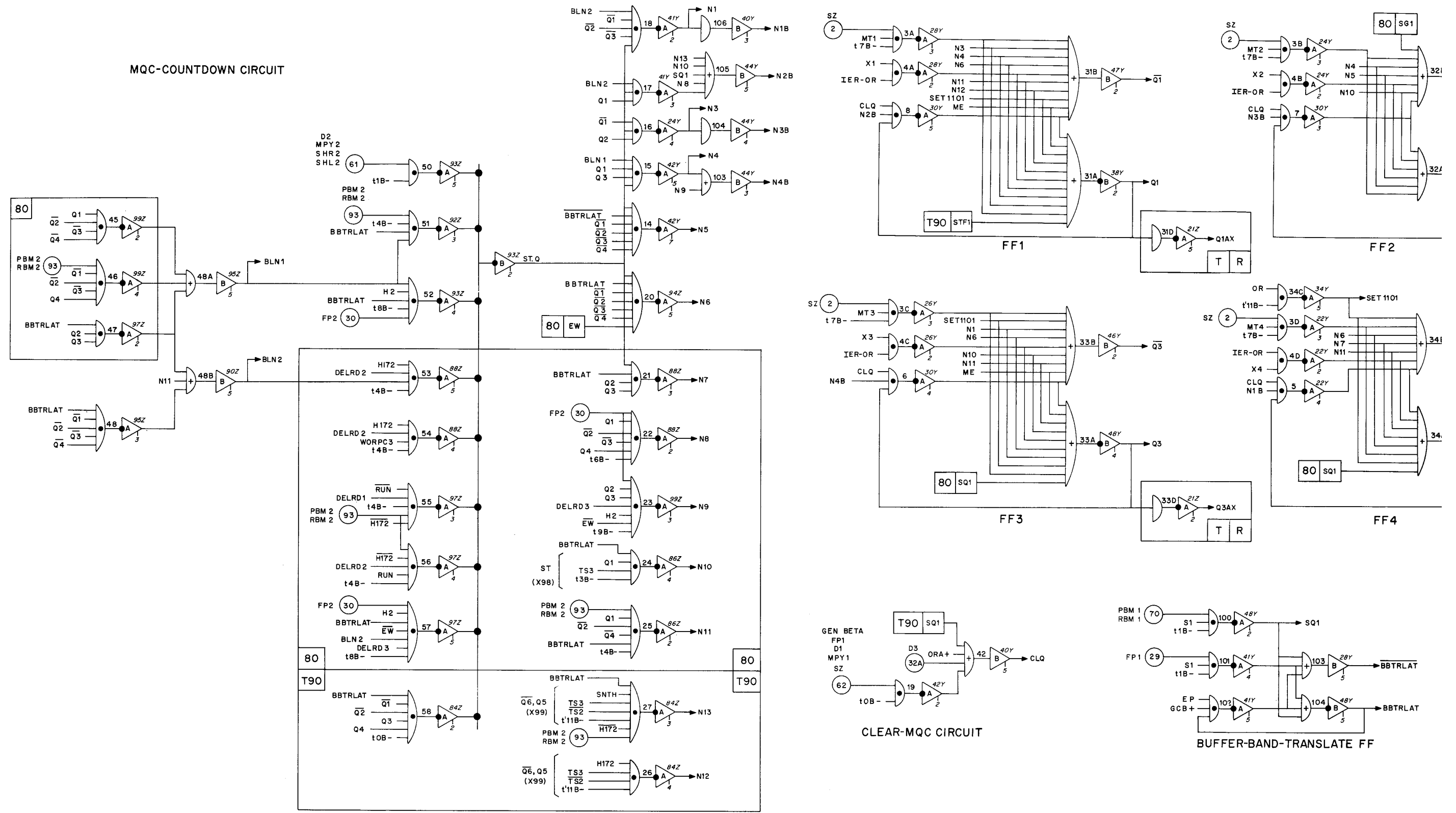
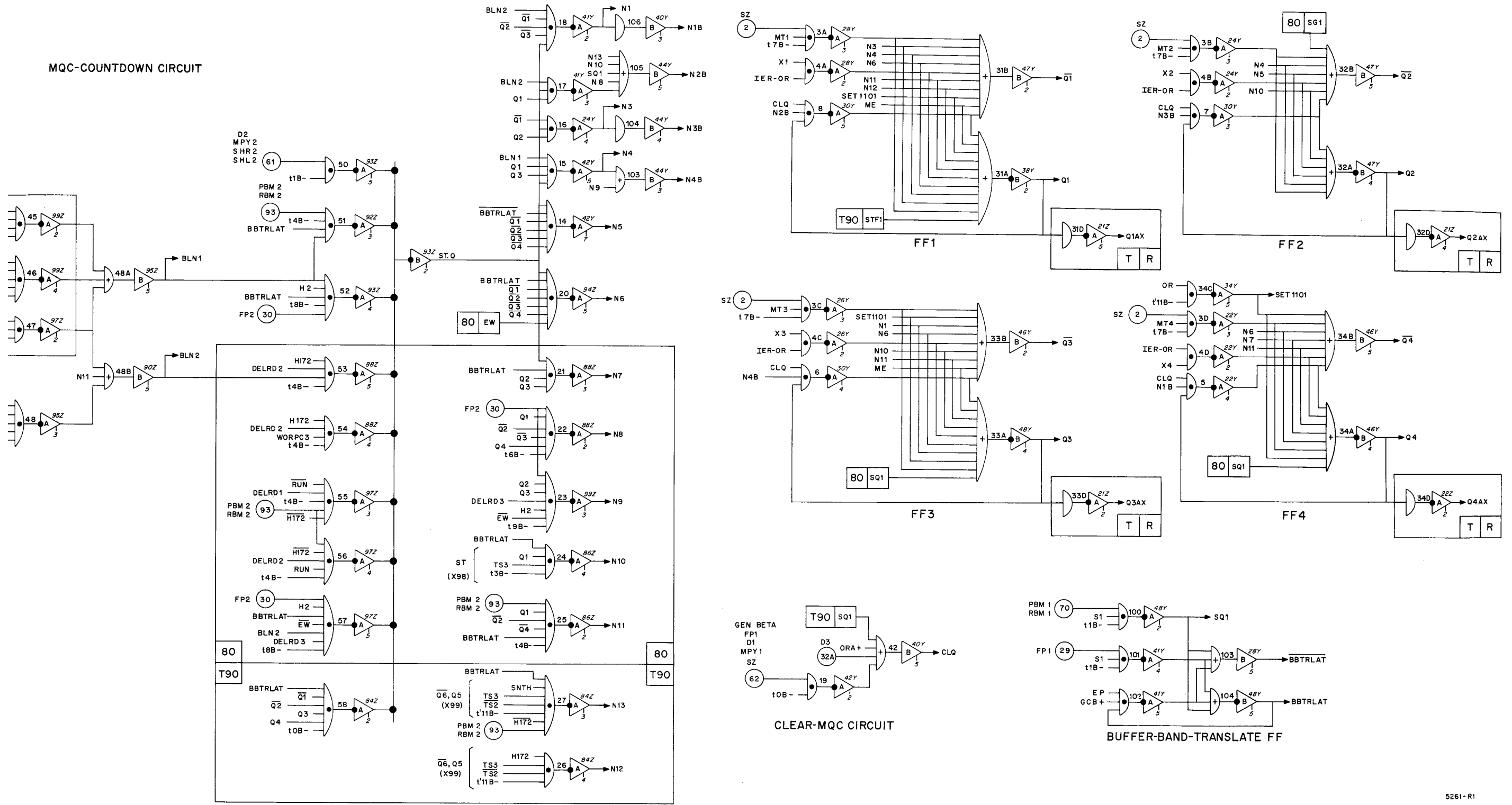
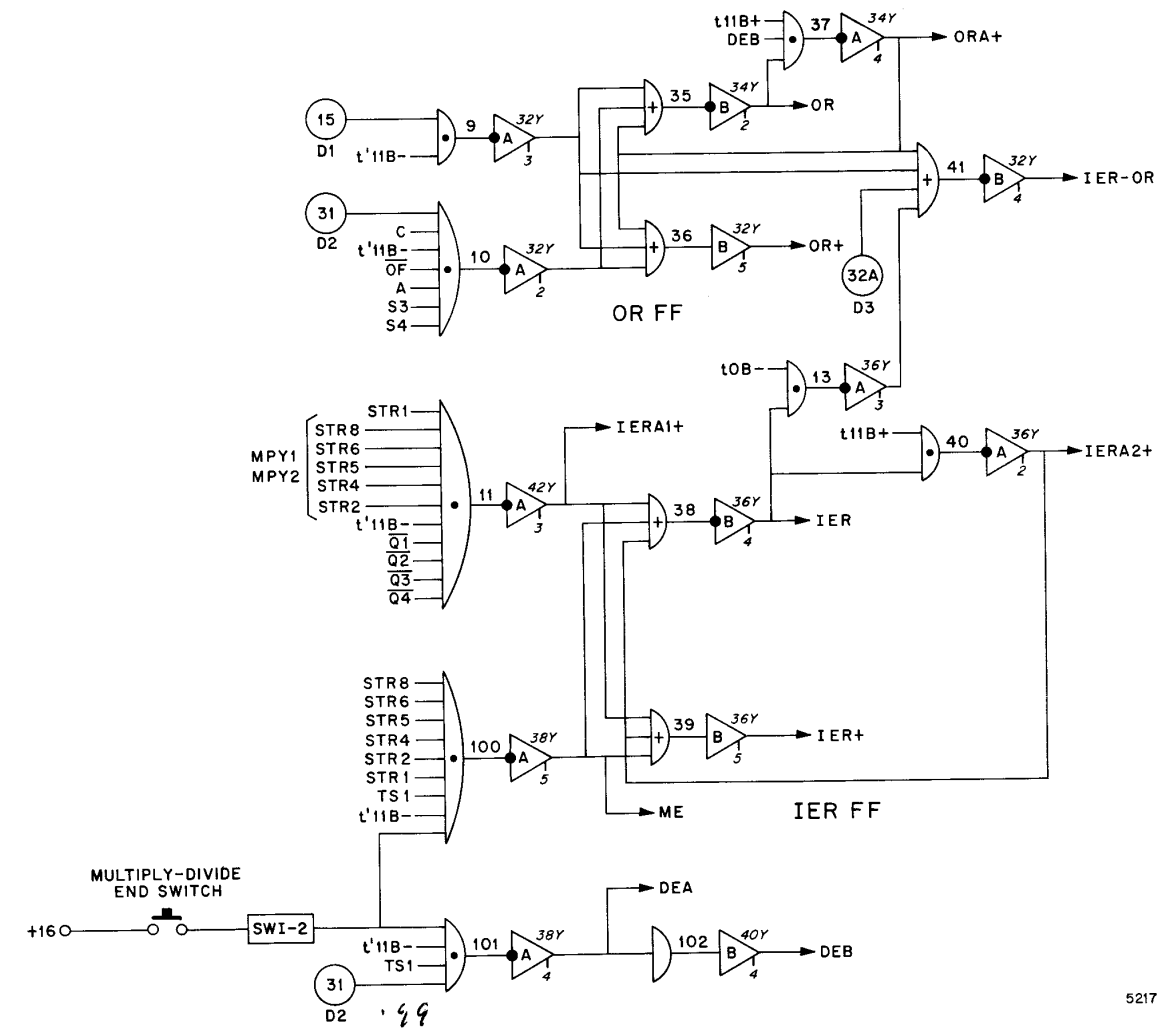


Figure 1-16B.



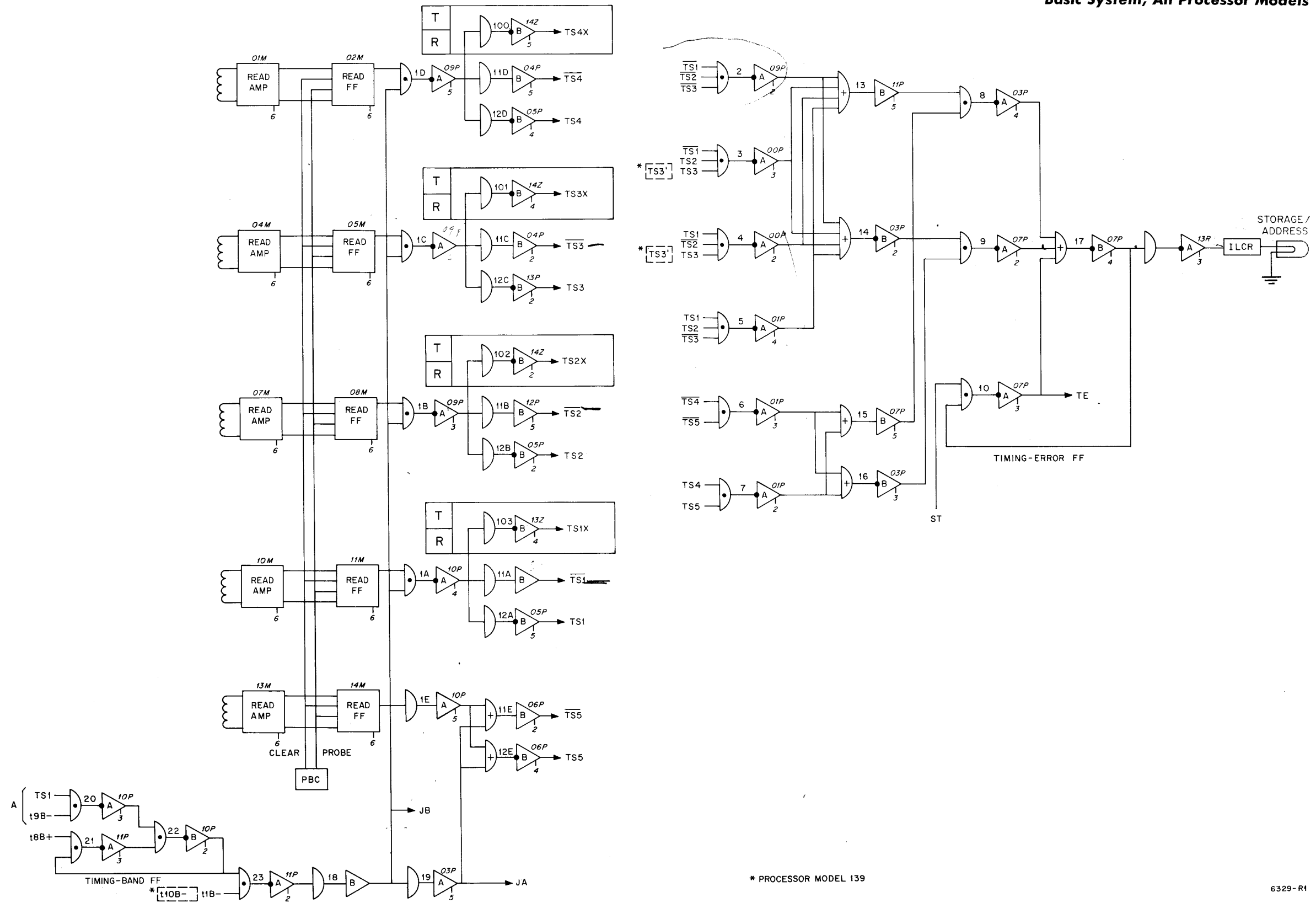
5261-R1

Figure 1-16B. Multiplier-Quotient Counter



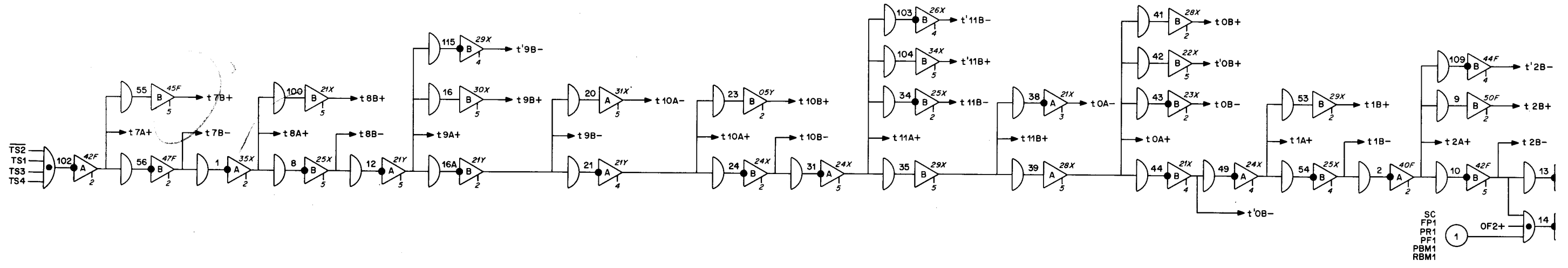
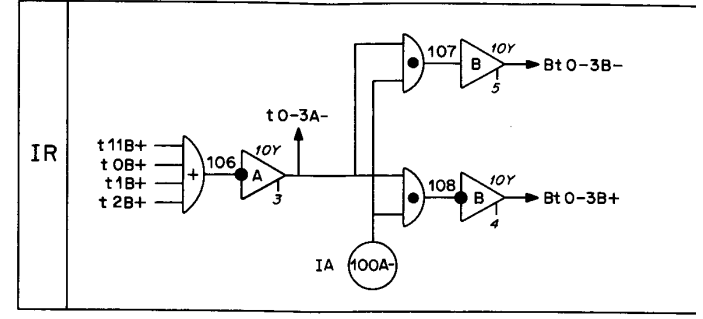
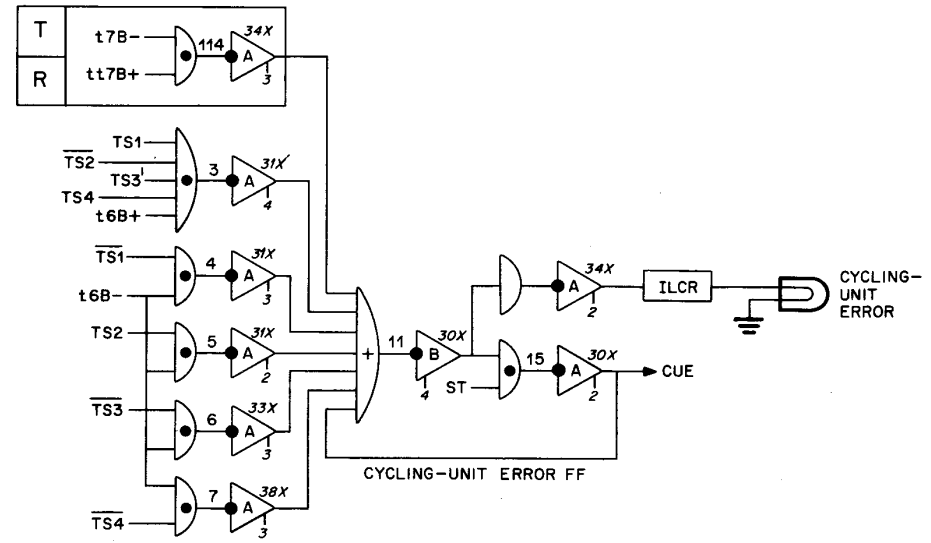
5217

Figure 1-17B. IER-OR Flip-Flops

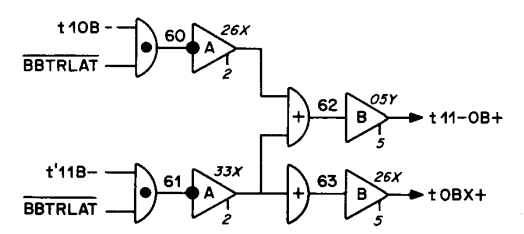
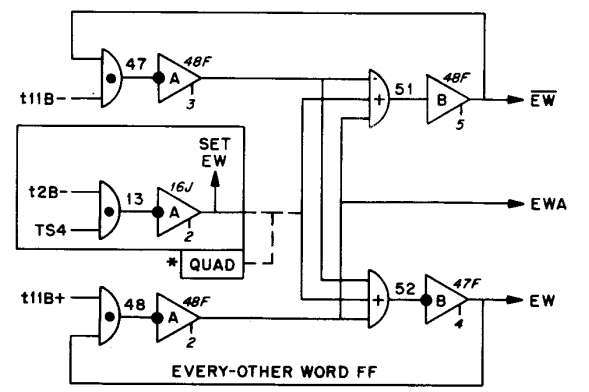
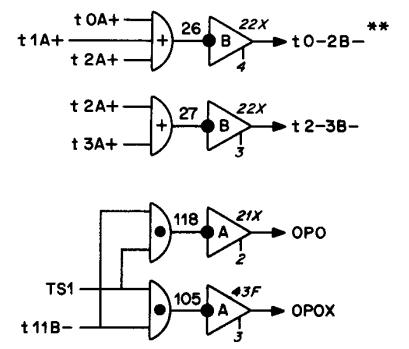


6329-R1

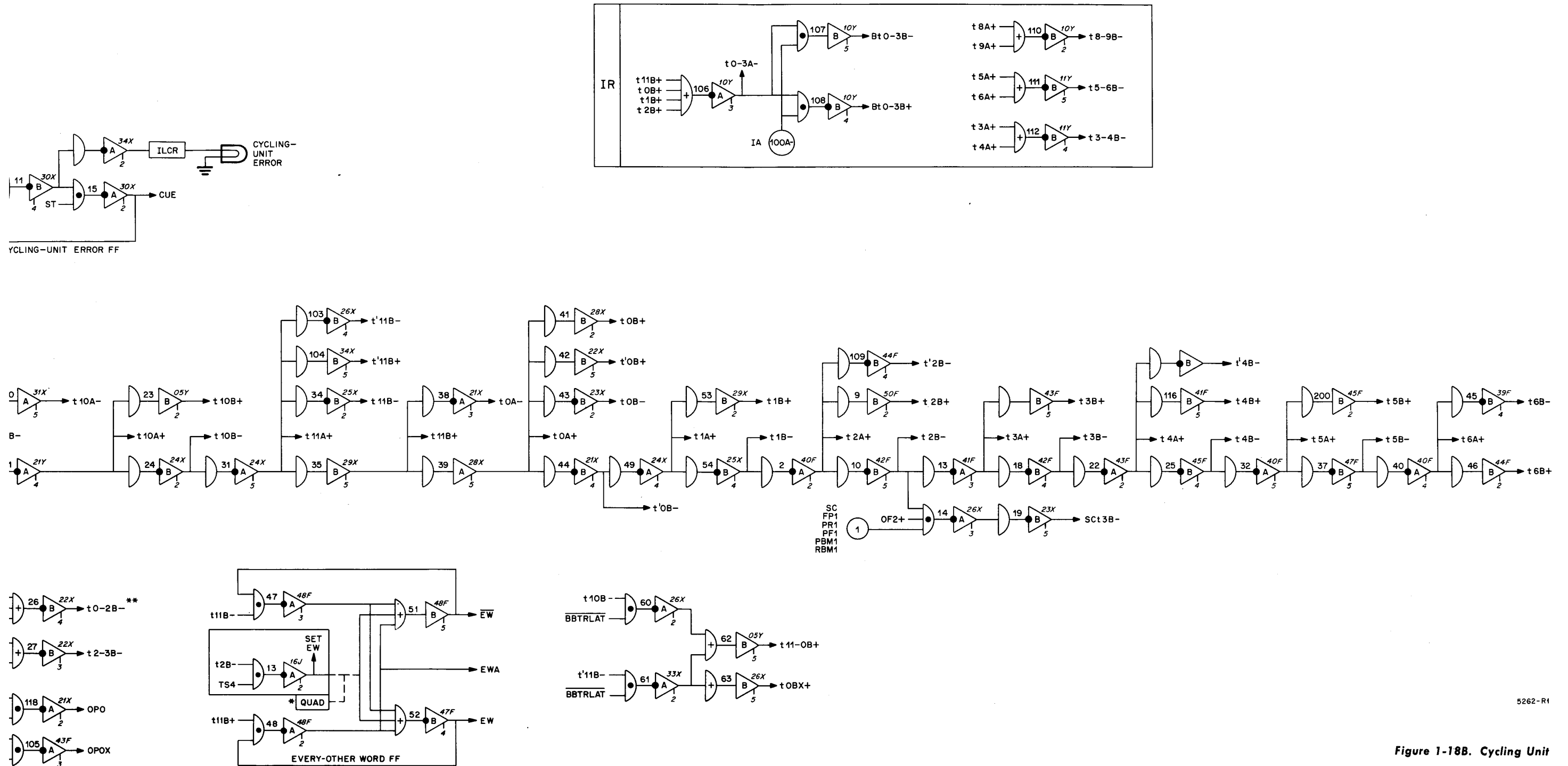
Figure 1-19B. Timing-Band Read Circuits



* PROCESSOR MODELS 130A AND 154
 ** MULTIPLE TIMING SIGNALS ARE PRESENT FOR THE LENGTH OF TIME DESIGNATED; e.g. t0-2B- IS PRESENT FOR t0B-, t1B-, AND t2B-.



SC
 FP1
 PR1
 PF1
 PBM1
 RBM1



5262-R1

Figure 1-18B. Cycling Unit

Basic System, All Processor Models

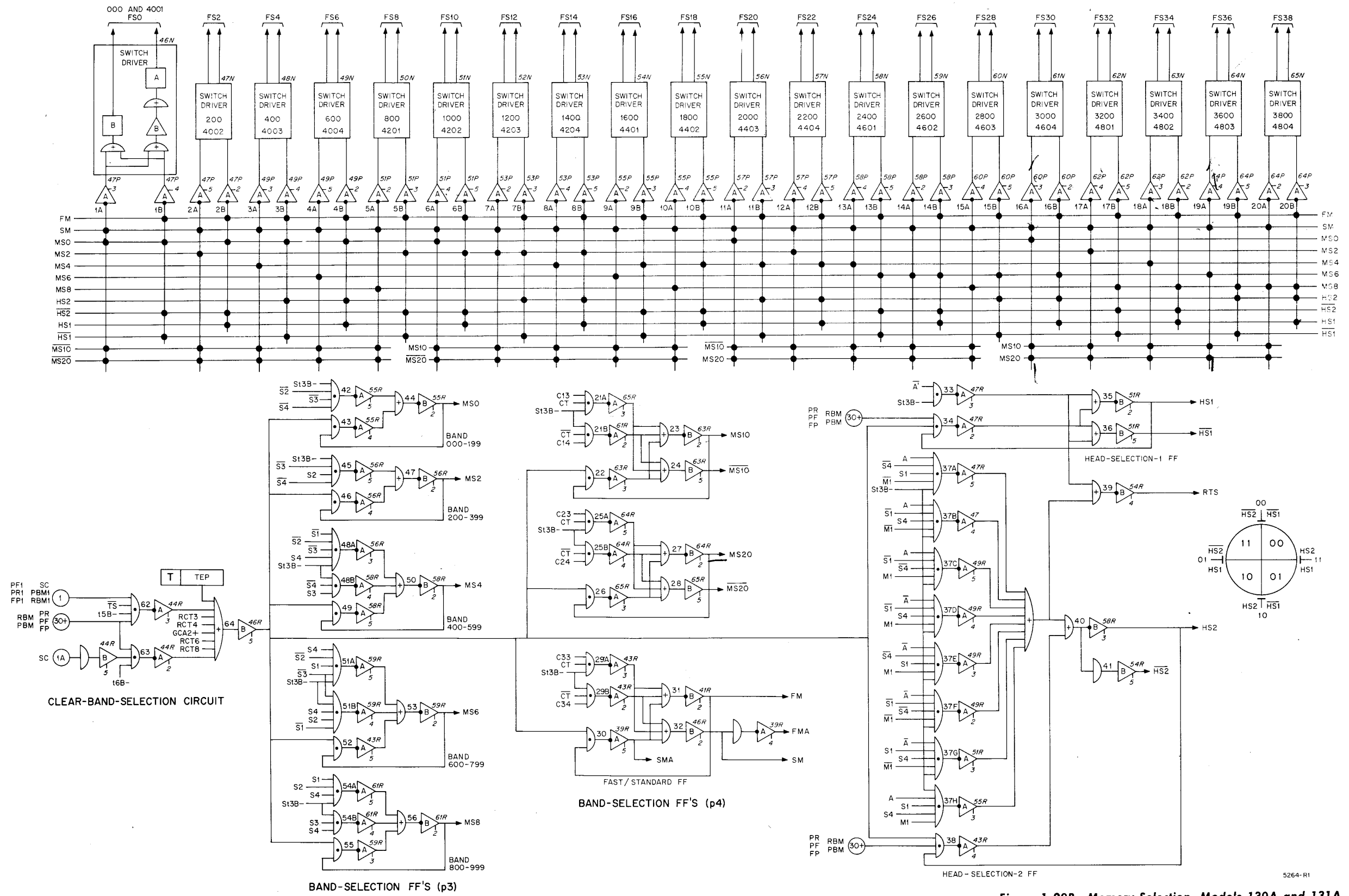


Figure 1-20B. Memory Selection, Models 130A and 131A

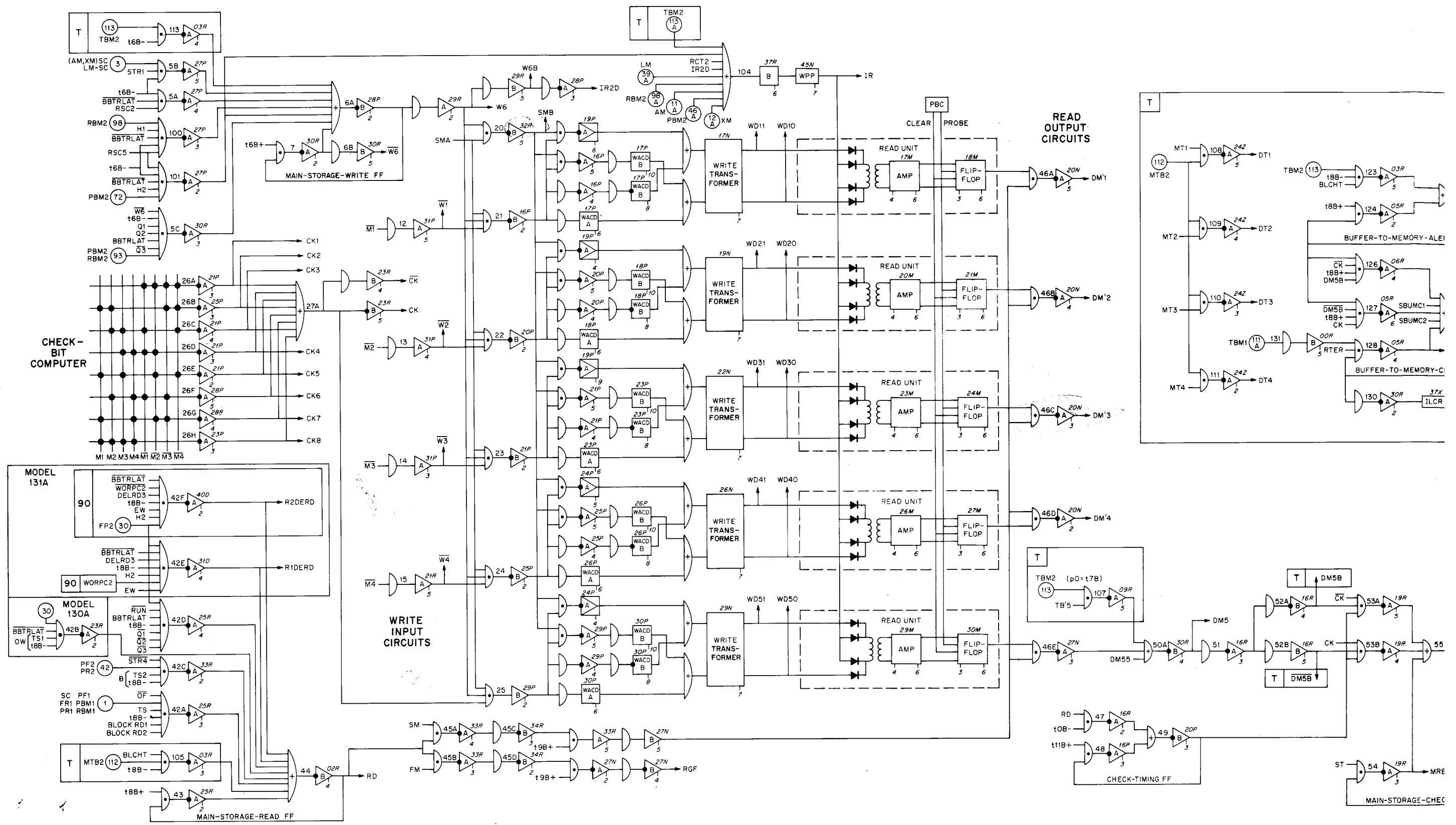


Figure 1-21B. N

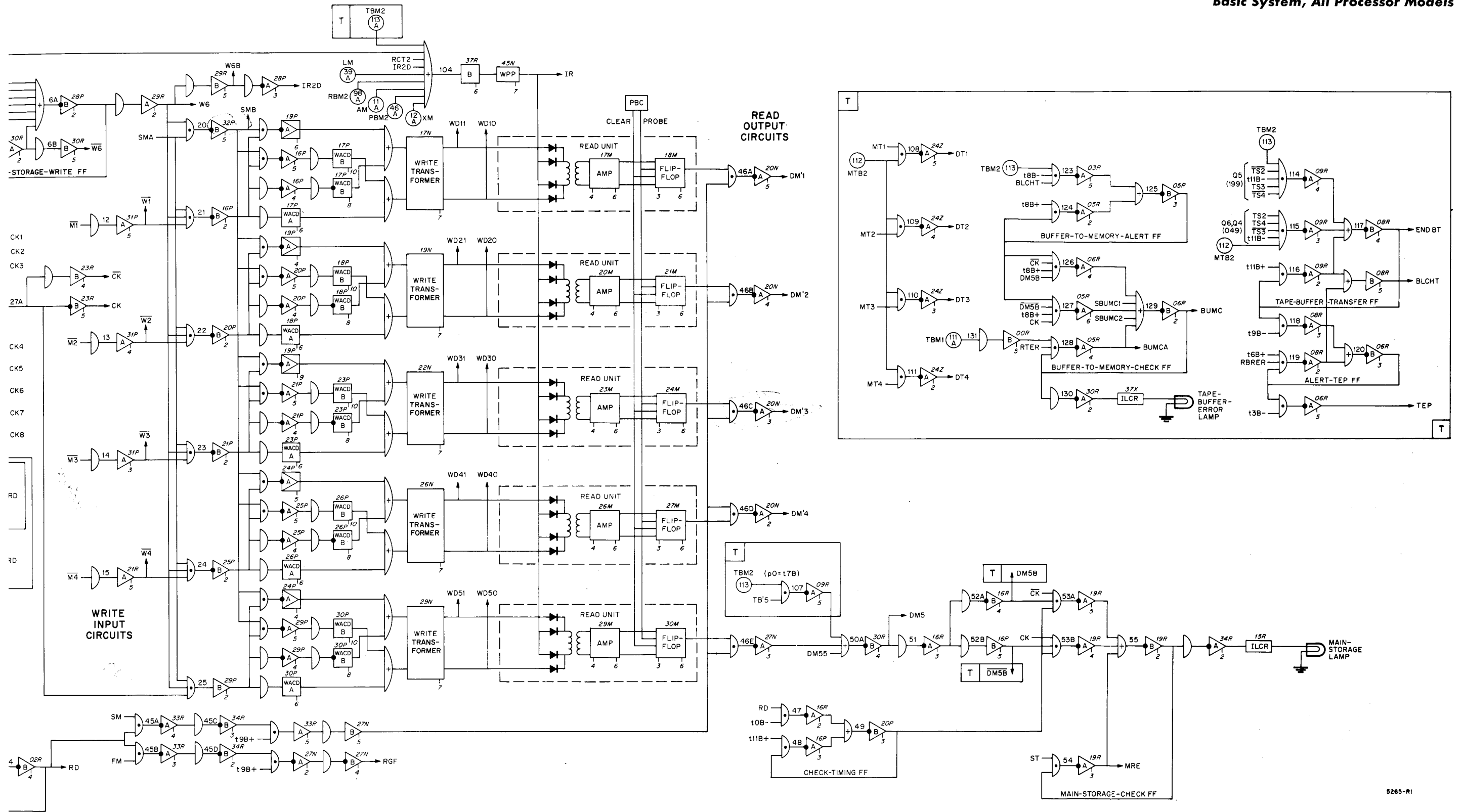


Figure 1-21B. Normal-Access Read/Write Circuits, Models 130A and 131A

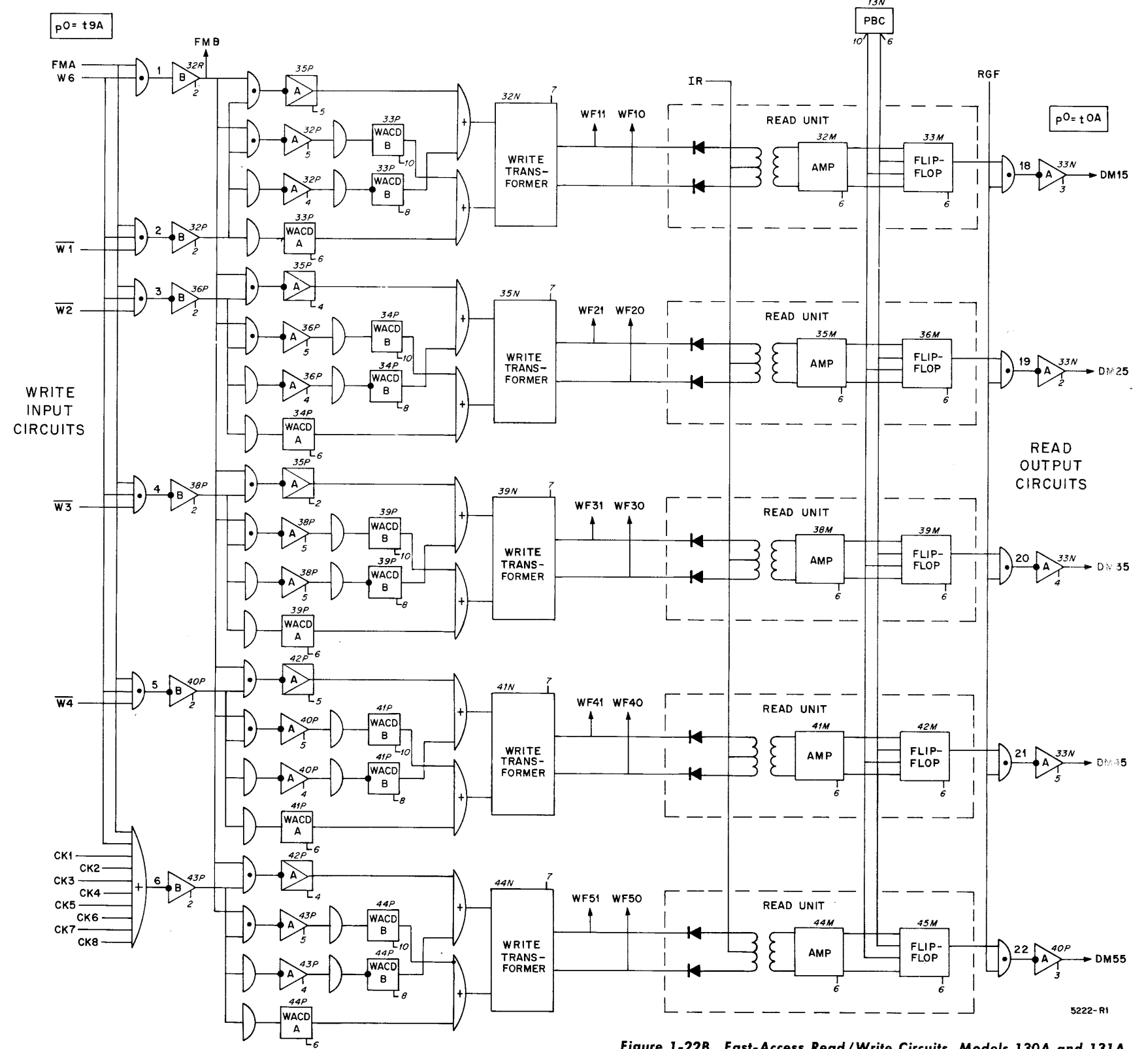


Figure 1-22B. Fast-Access Read/Write Circuits, Models 130A and 131A

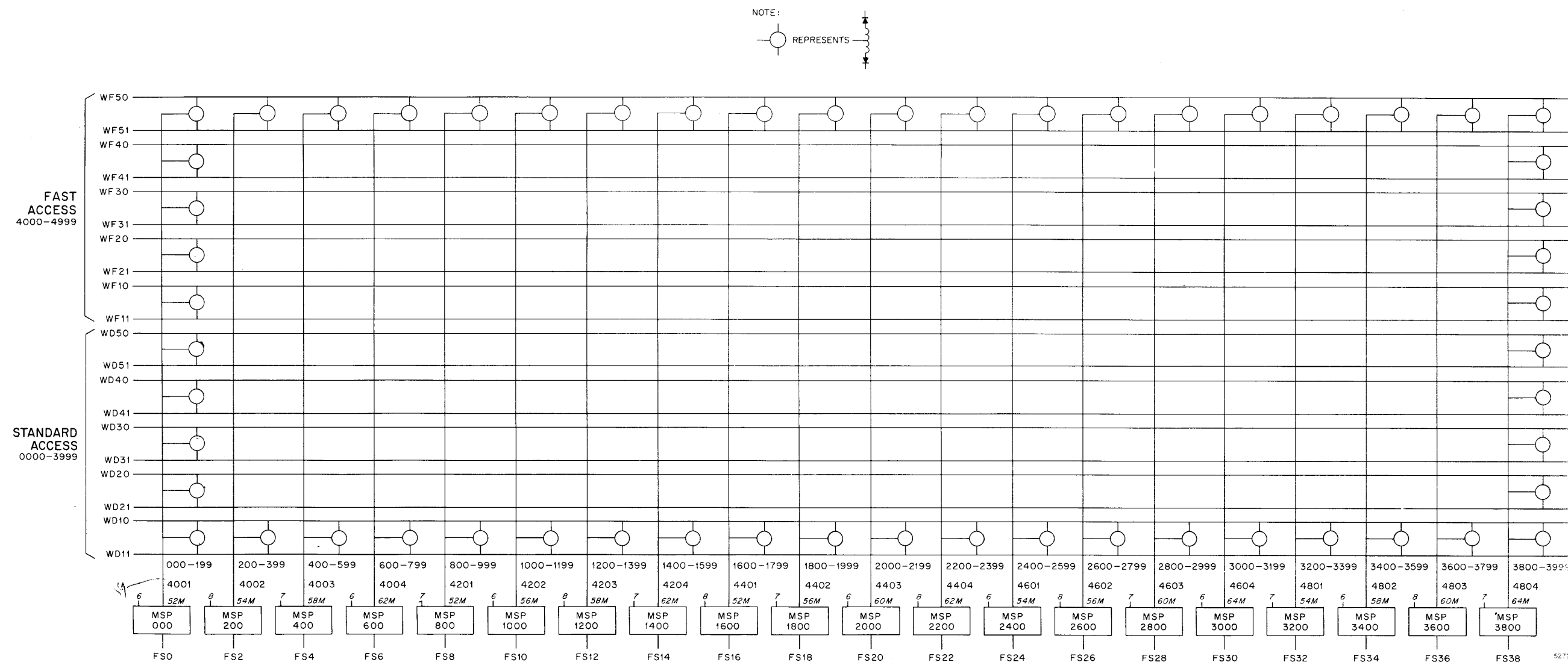


Figure 1-23B. Memory Switch

Basic System, All Processor Models

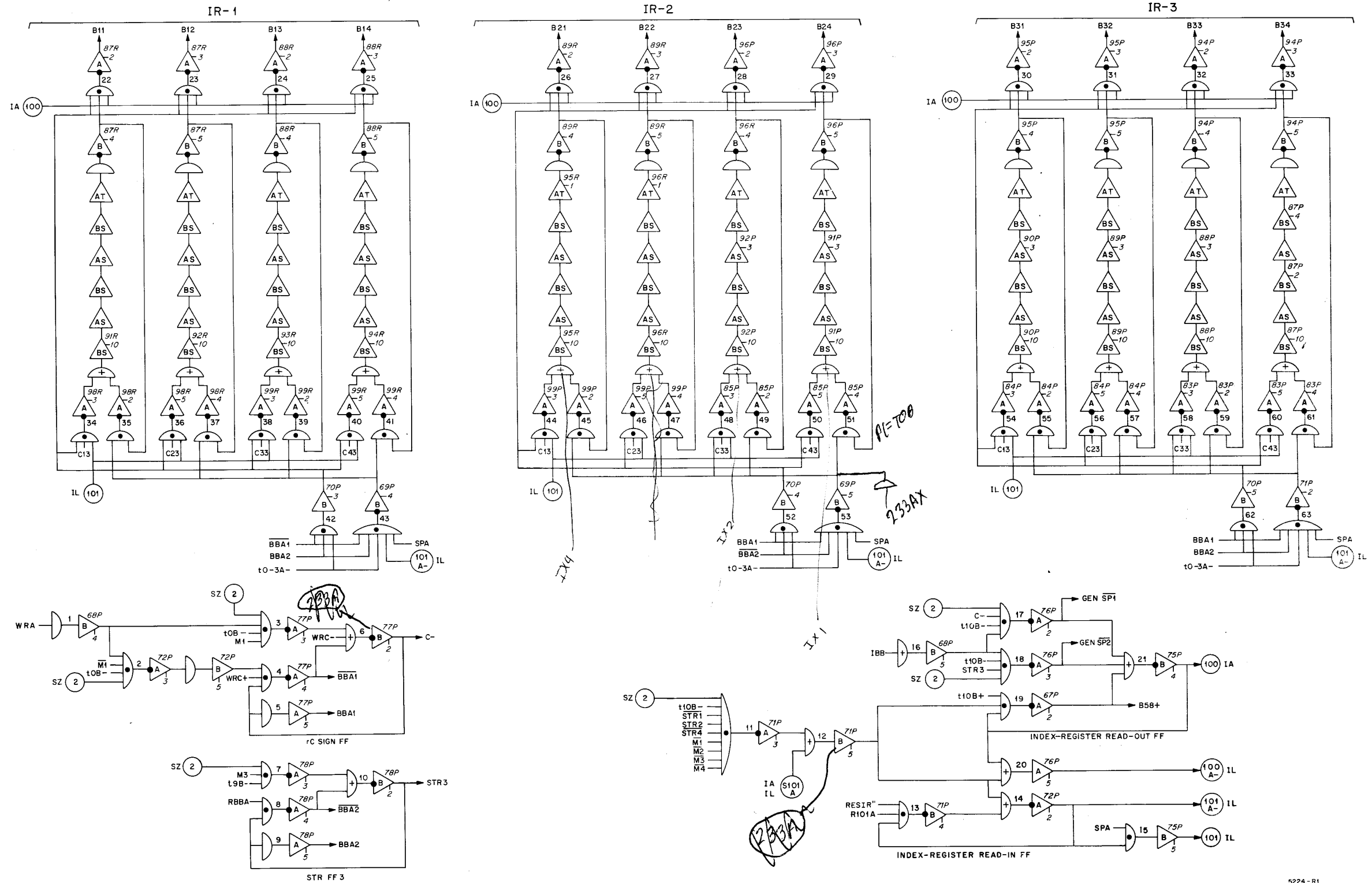


Figure 1-24B. Index Registers

Basic System, All Processor Models

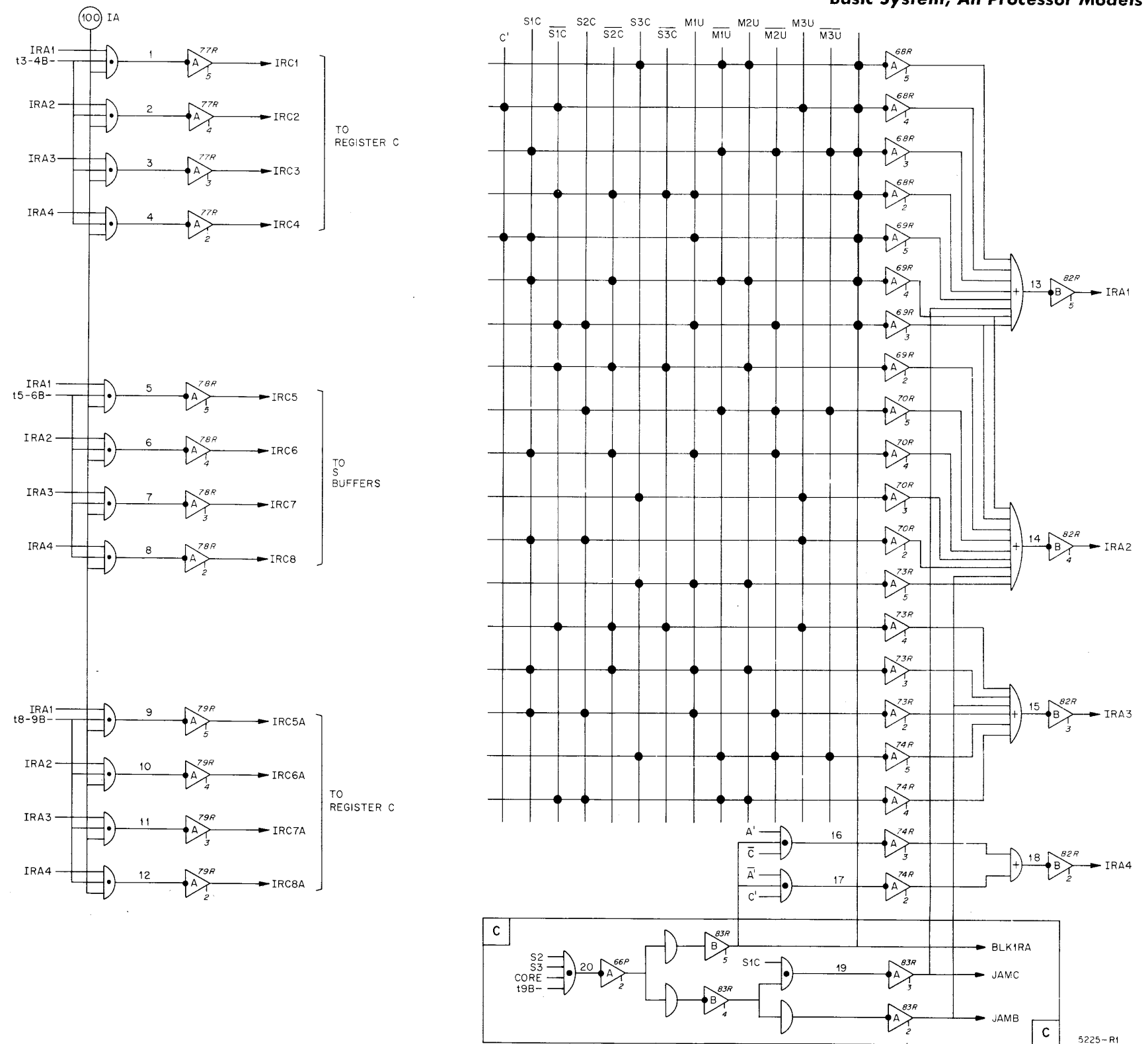


Figure 1-25B. Index-Register Adder

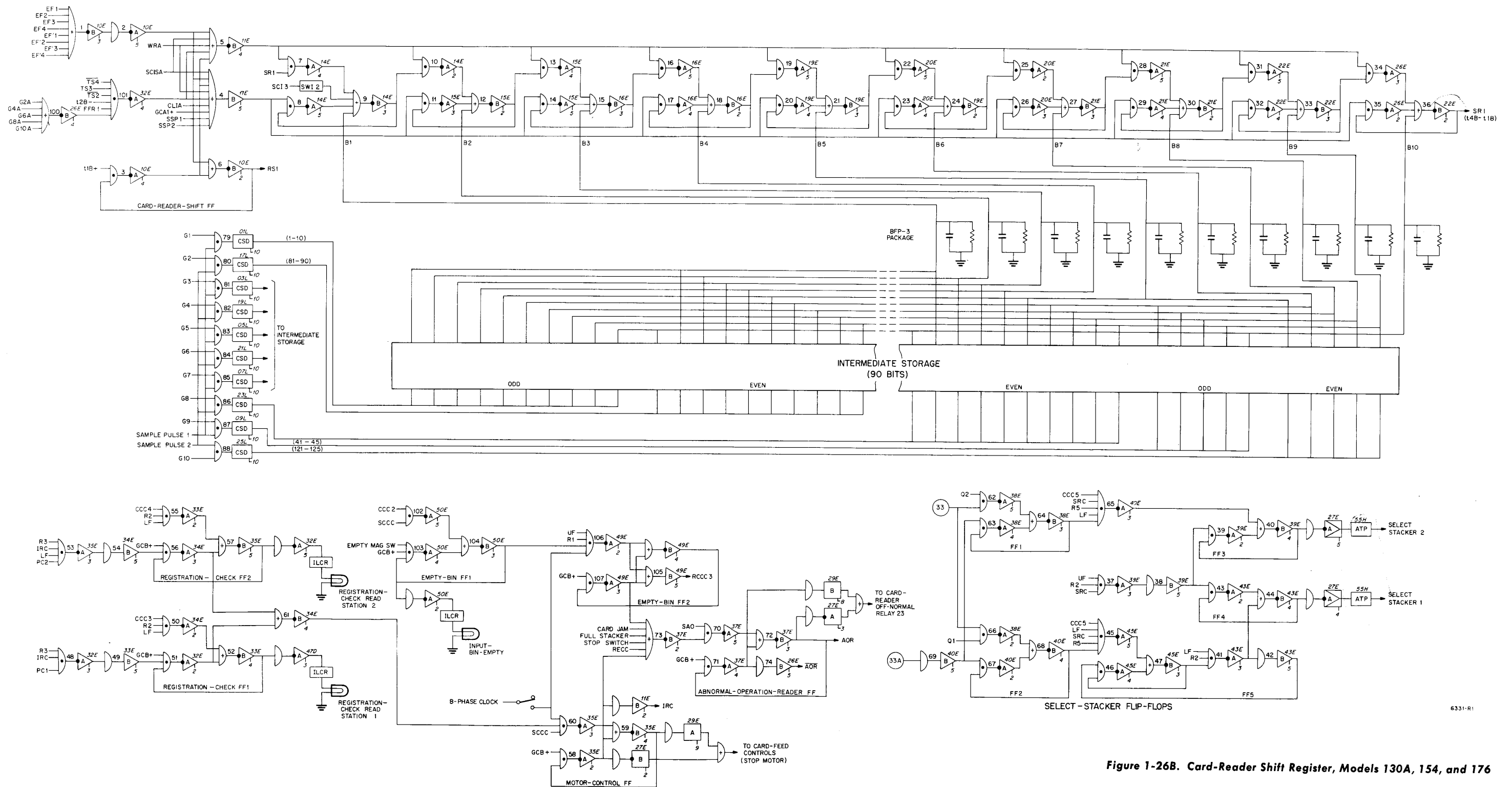


Figure 1-26B. Card-Reader Shift Register, Models 130A, 154, and 176

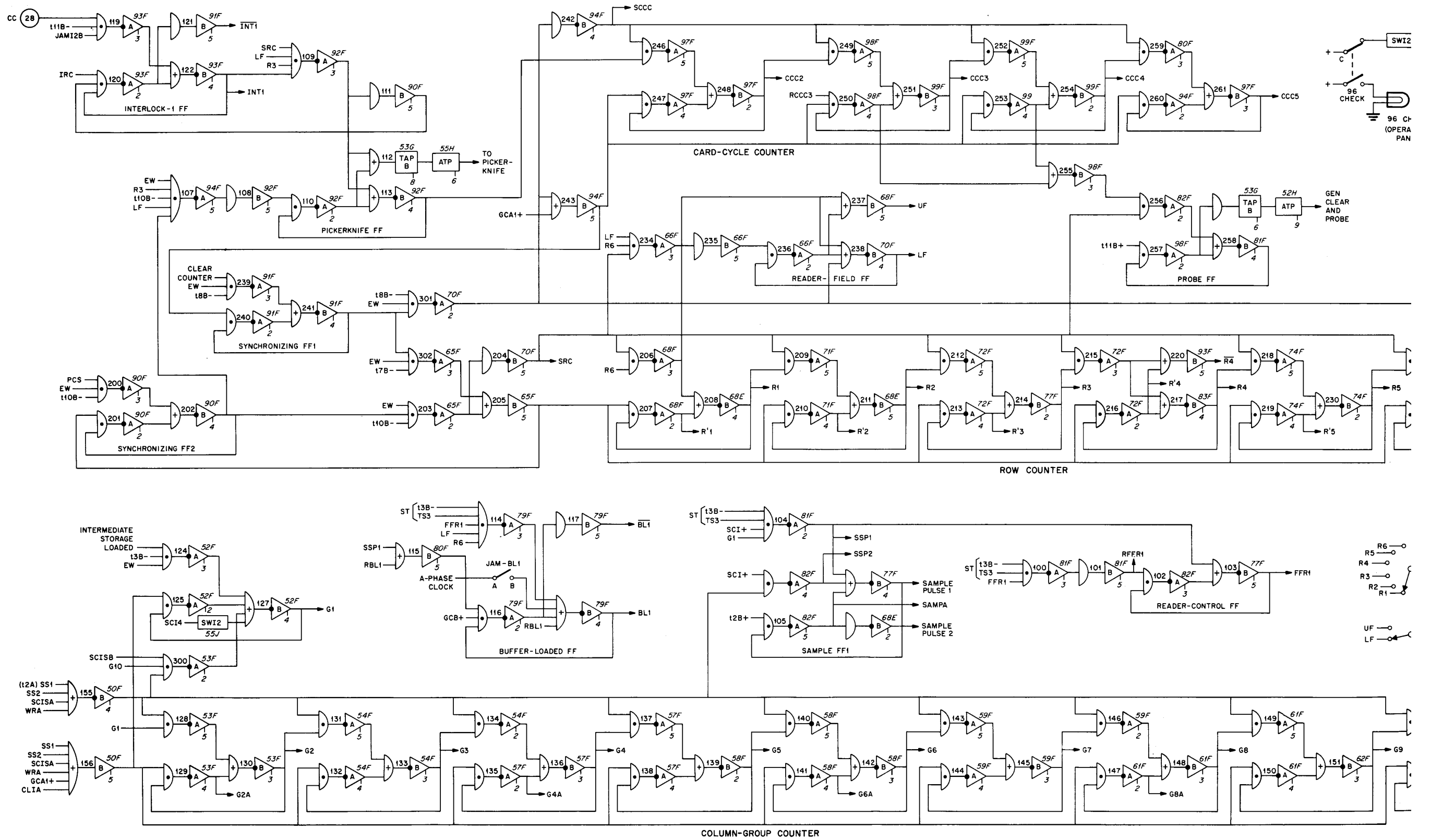


Figure 1-27B. Card-Reader Control, I

Basic System, All Processor Models

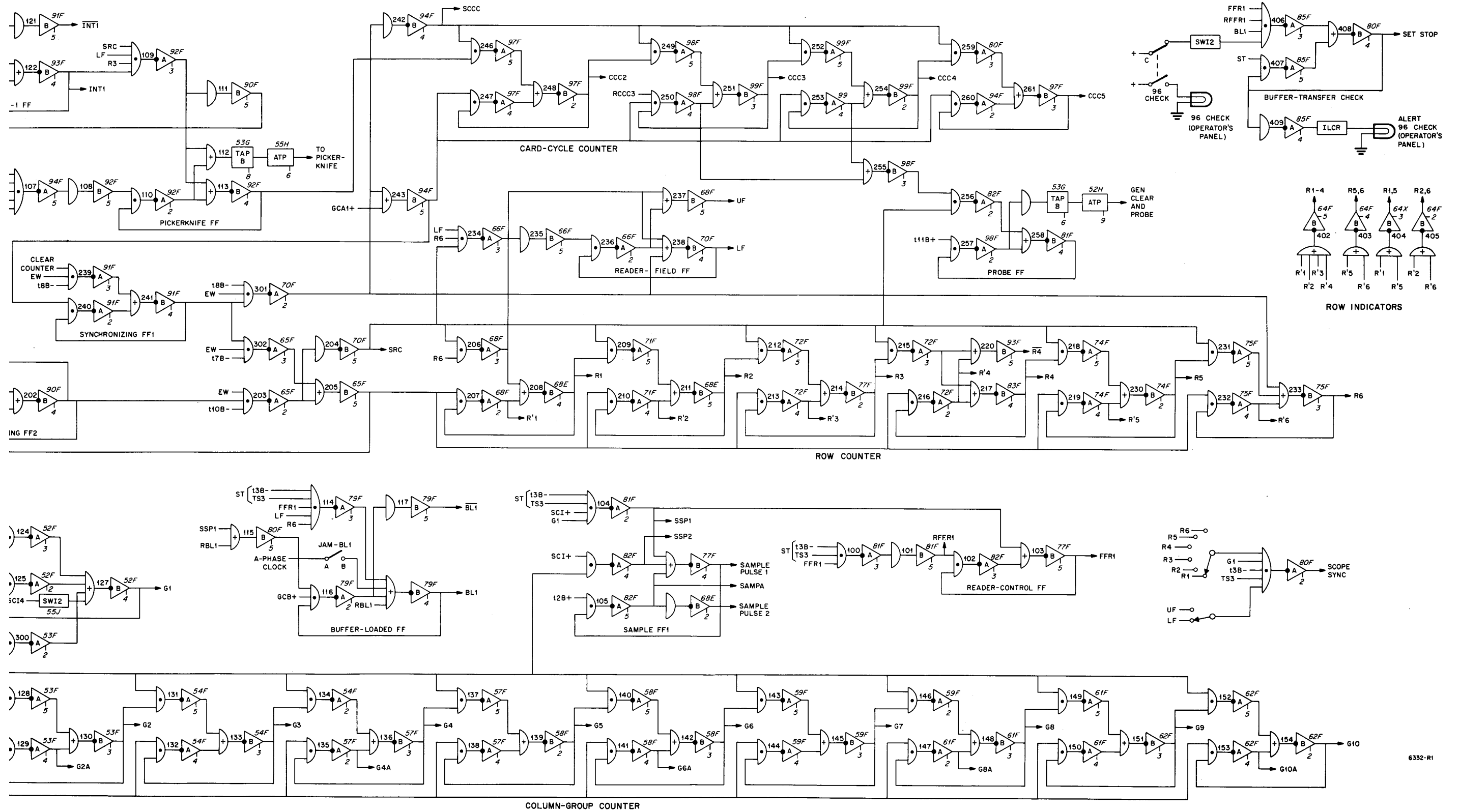
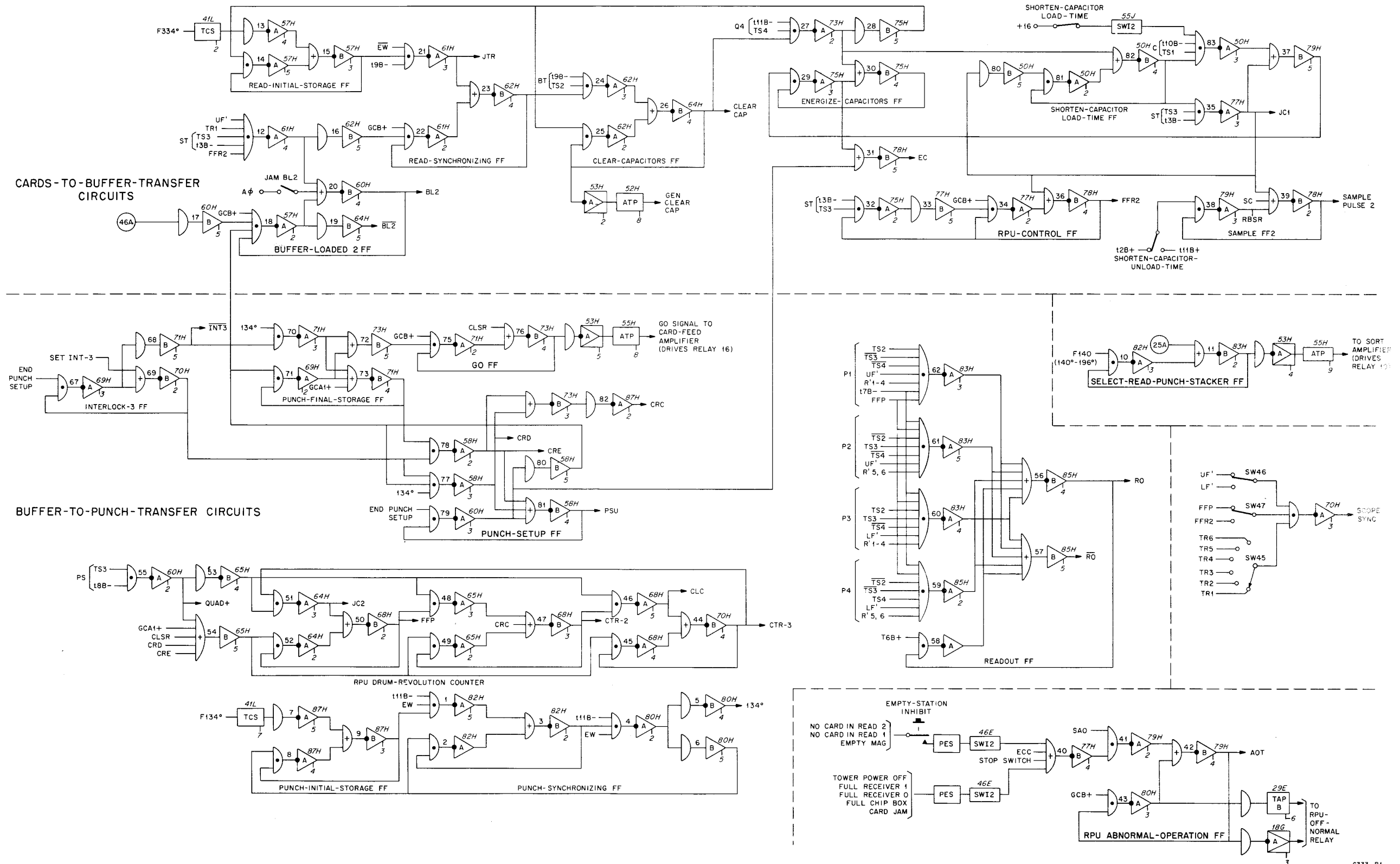


Figure 1-27B. Card-Reader Control, Models 130A, 144, and 176



6333-R1

Figure 1-28B. Sense and Punch Logic, Part 1, Models 130A, 154, and 176

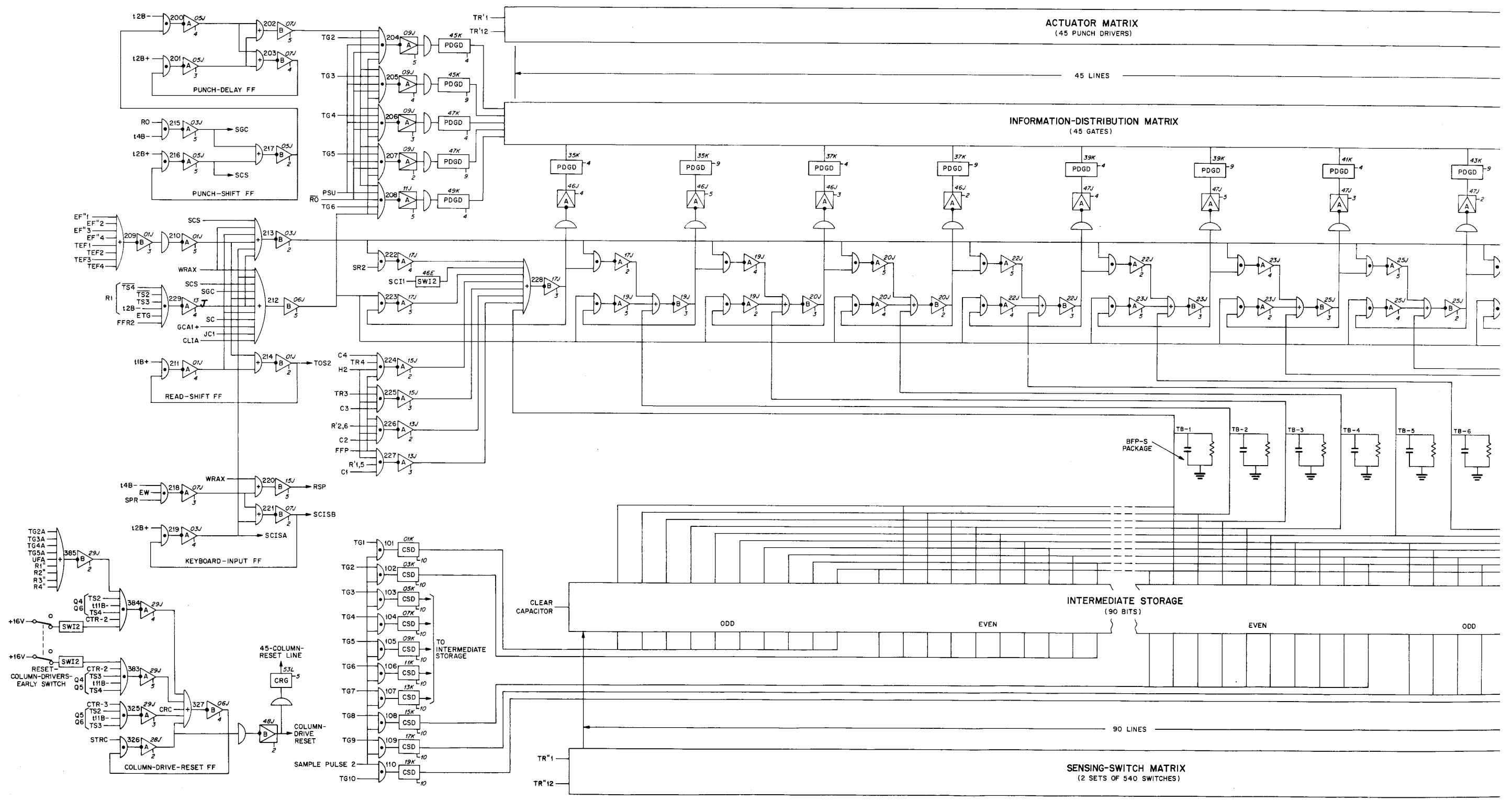


Figure 1-29B. Sense and Pun

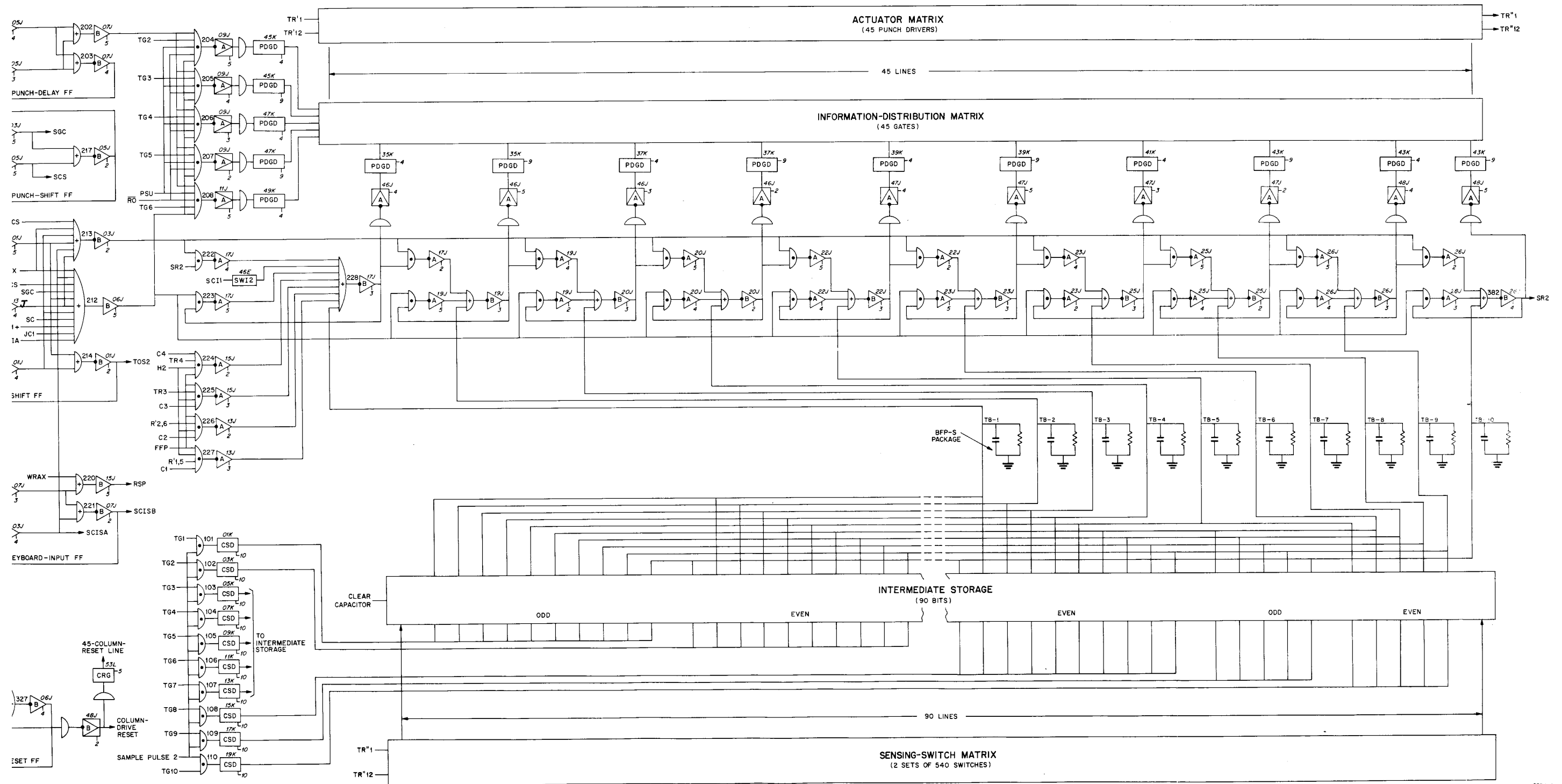
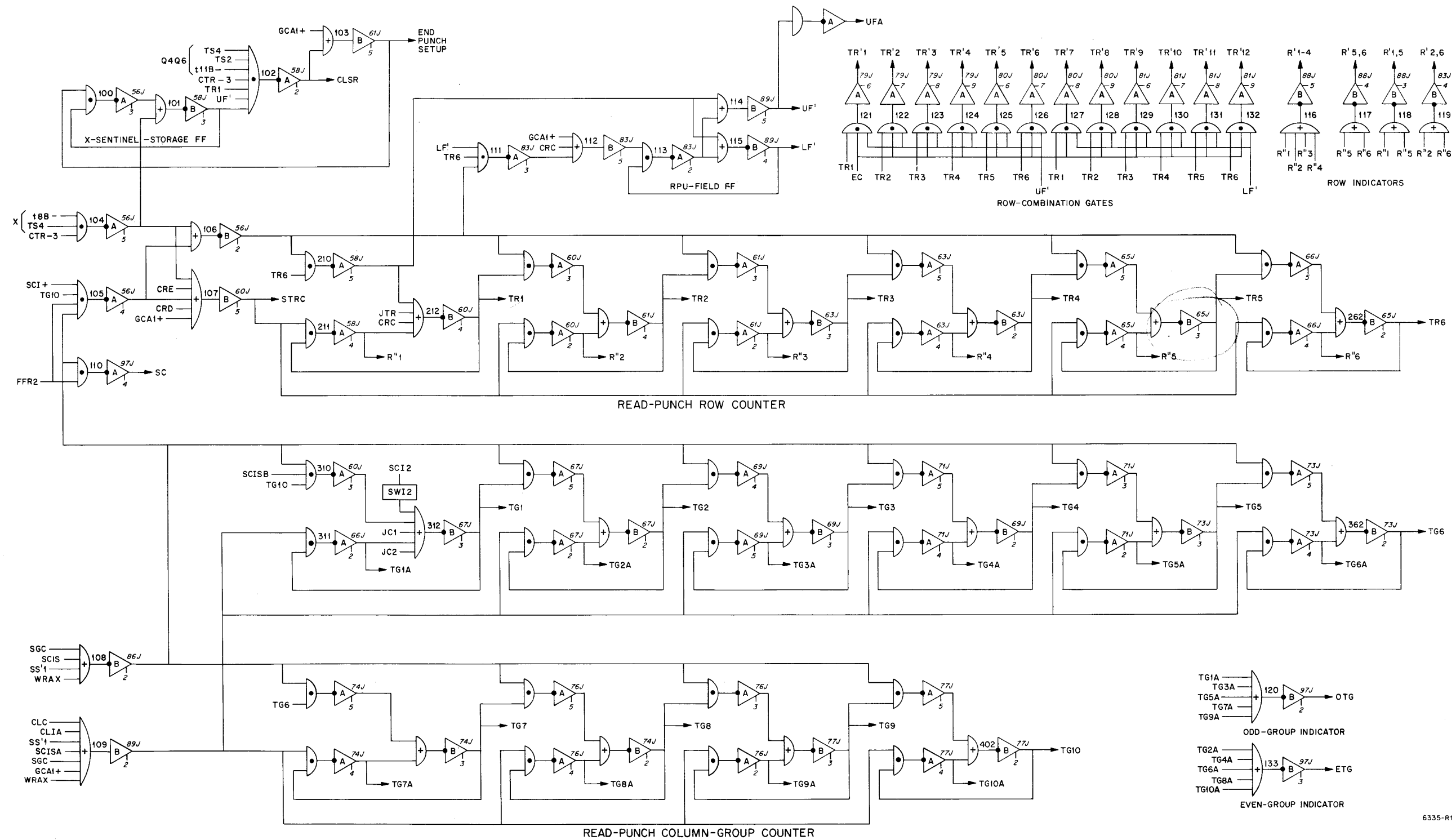


Figure 1-29B. Sense and Punch Logic, Part 2, Models 130A, 154, and 176



6335-R1

Figure 1-30B. Sense and Punch Logic, Part 3, Models 130A, 154, and 176

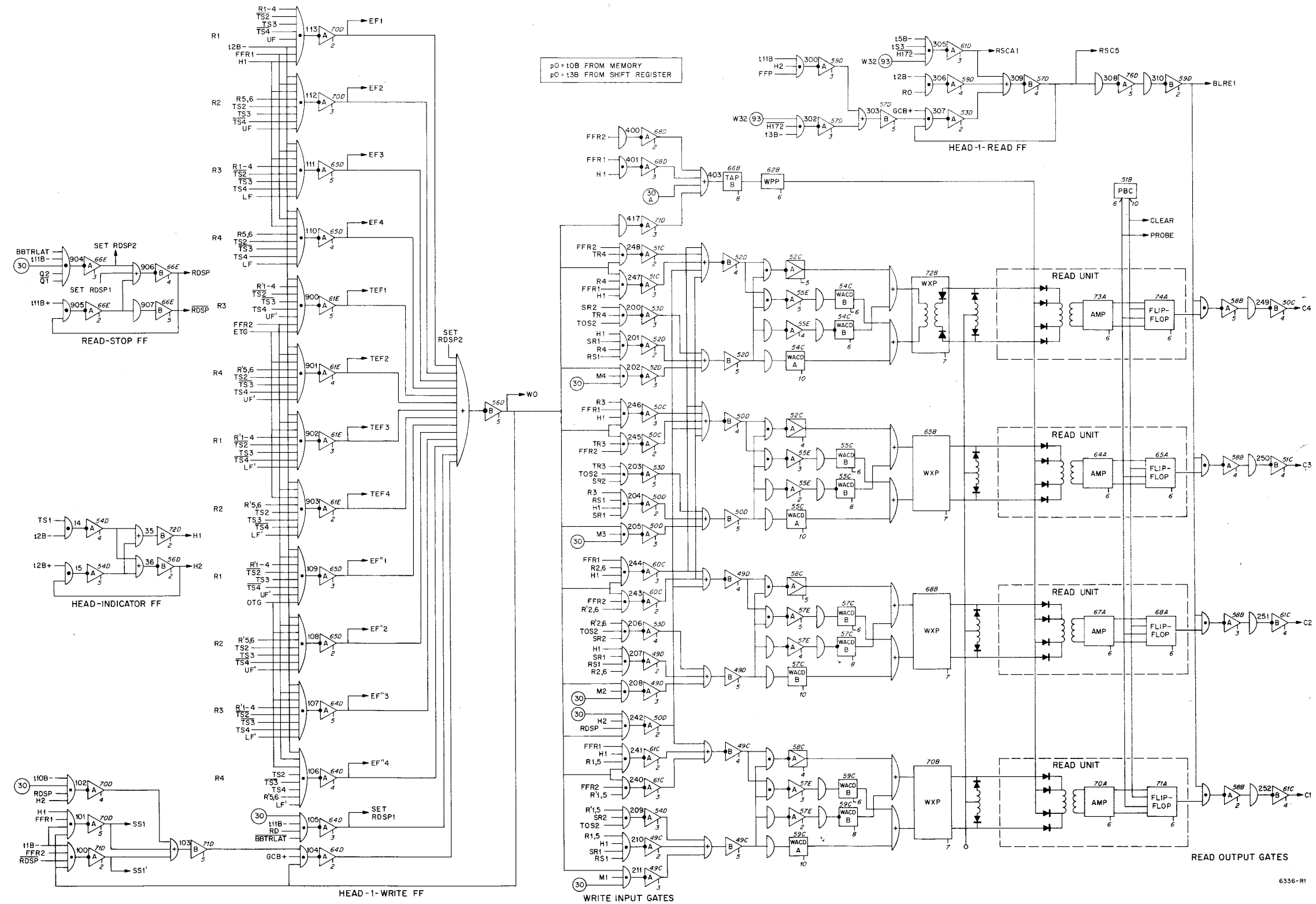


Figure 1-31B. Card-Buffer Head 1, Models 130A, 154, and 176

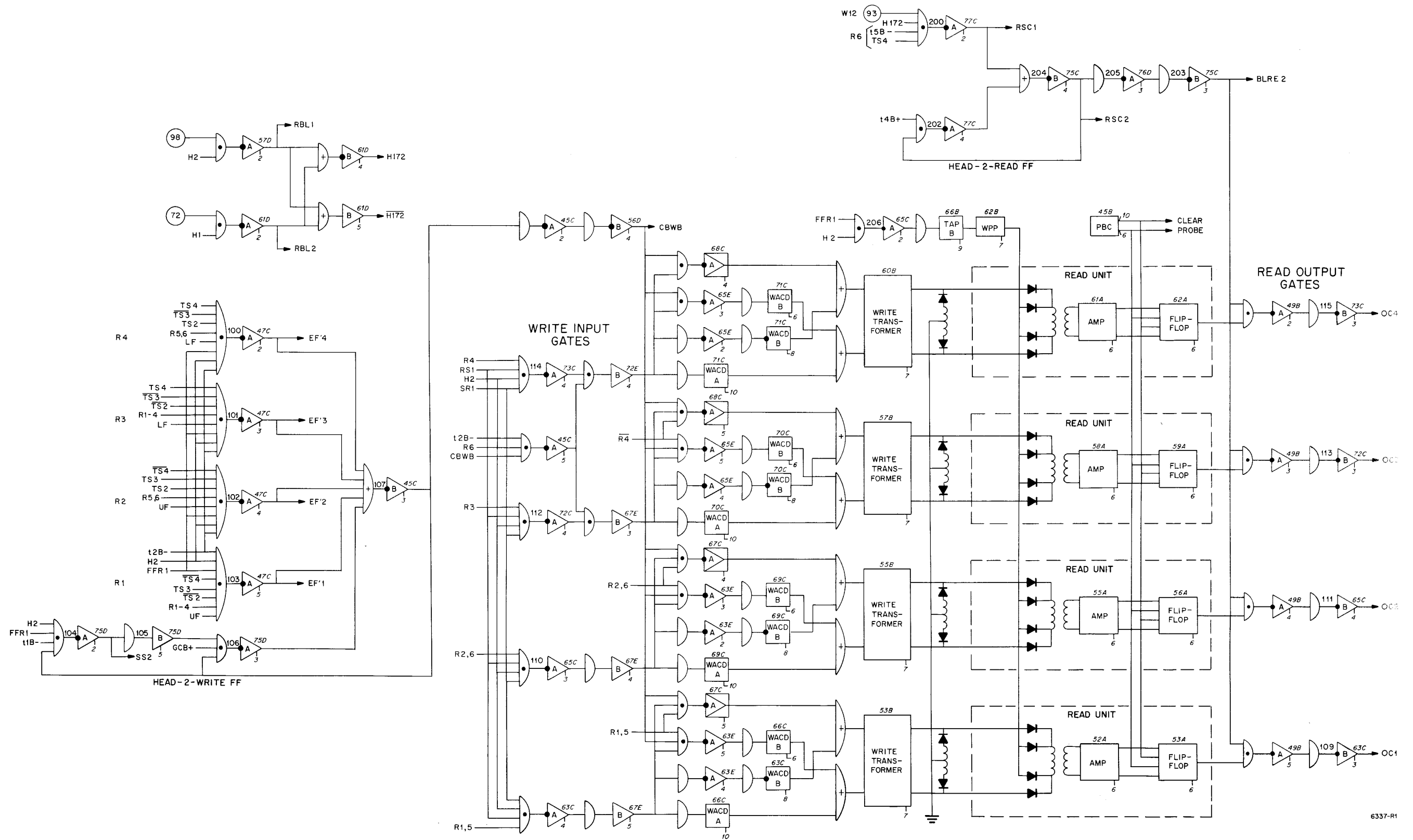


Figure 1-32B. Card-Buffer Head 2, Models 130A, 154, and 176

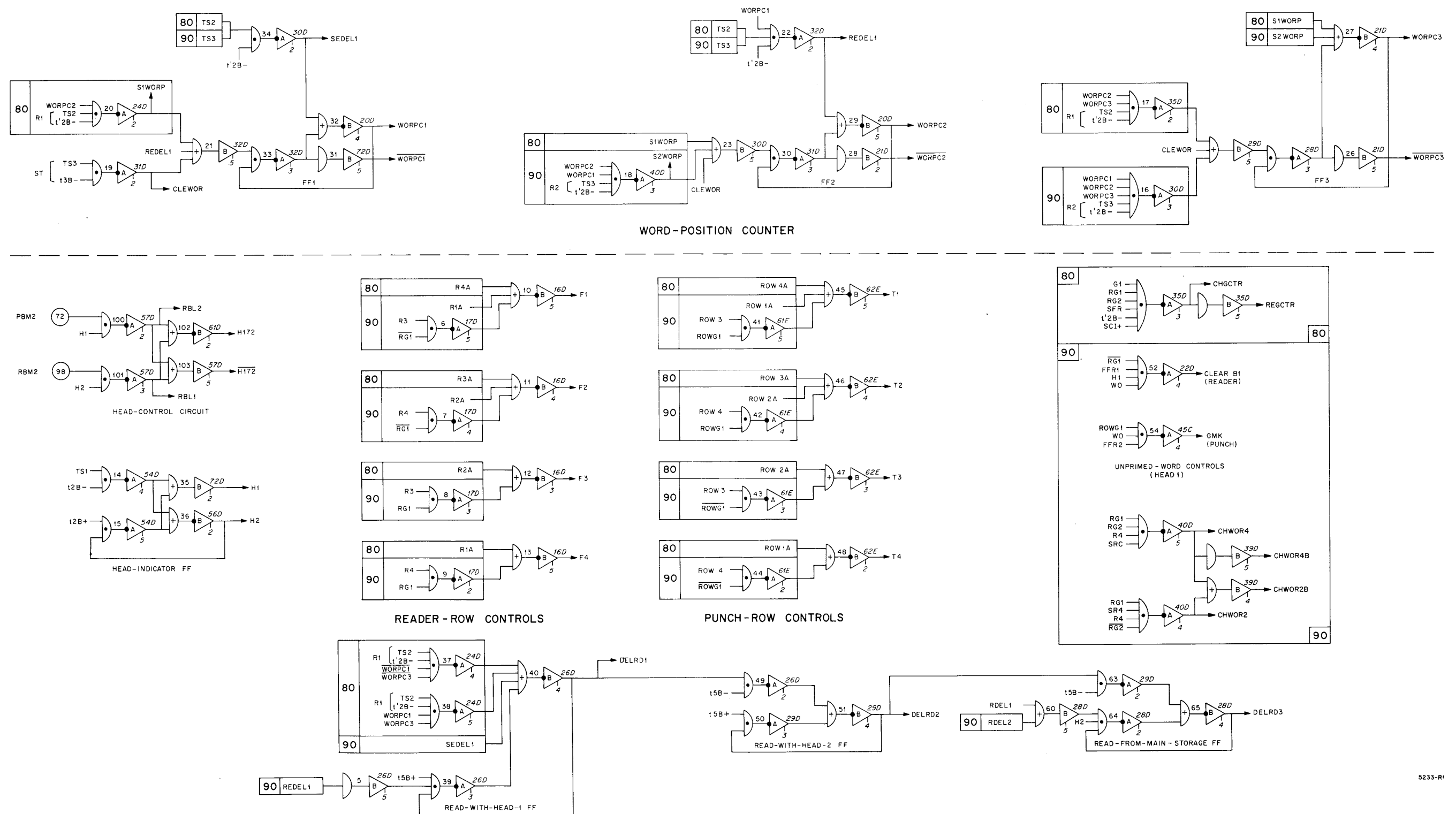


Figure 1-33B. Card-Buffer-Band Control, Models 131A, 139, 154, and 184

5233-R1

Basic System, All Processor Models

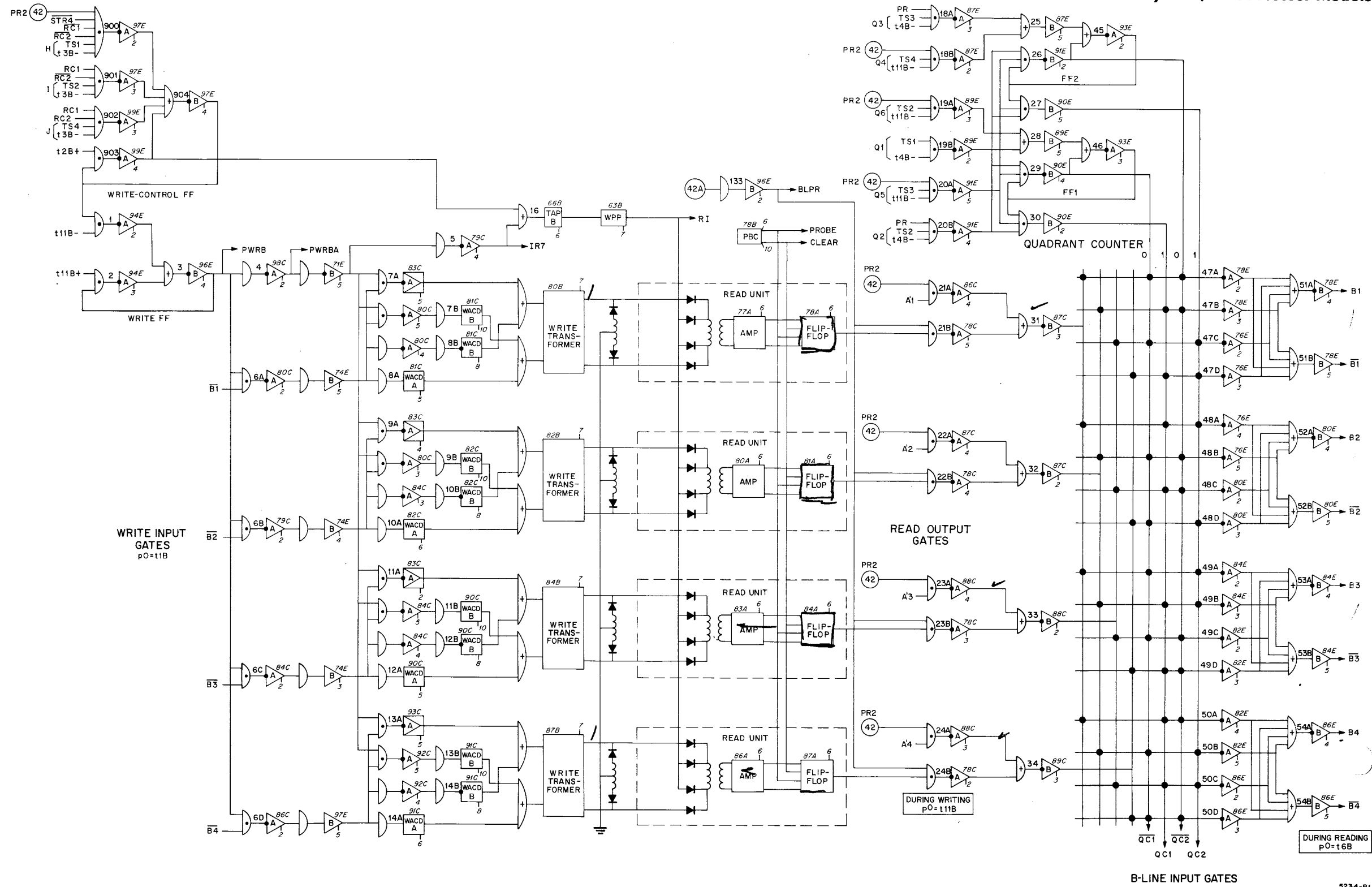
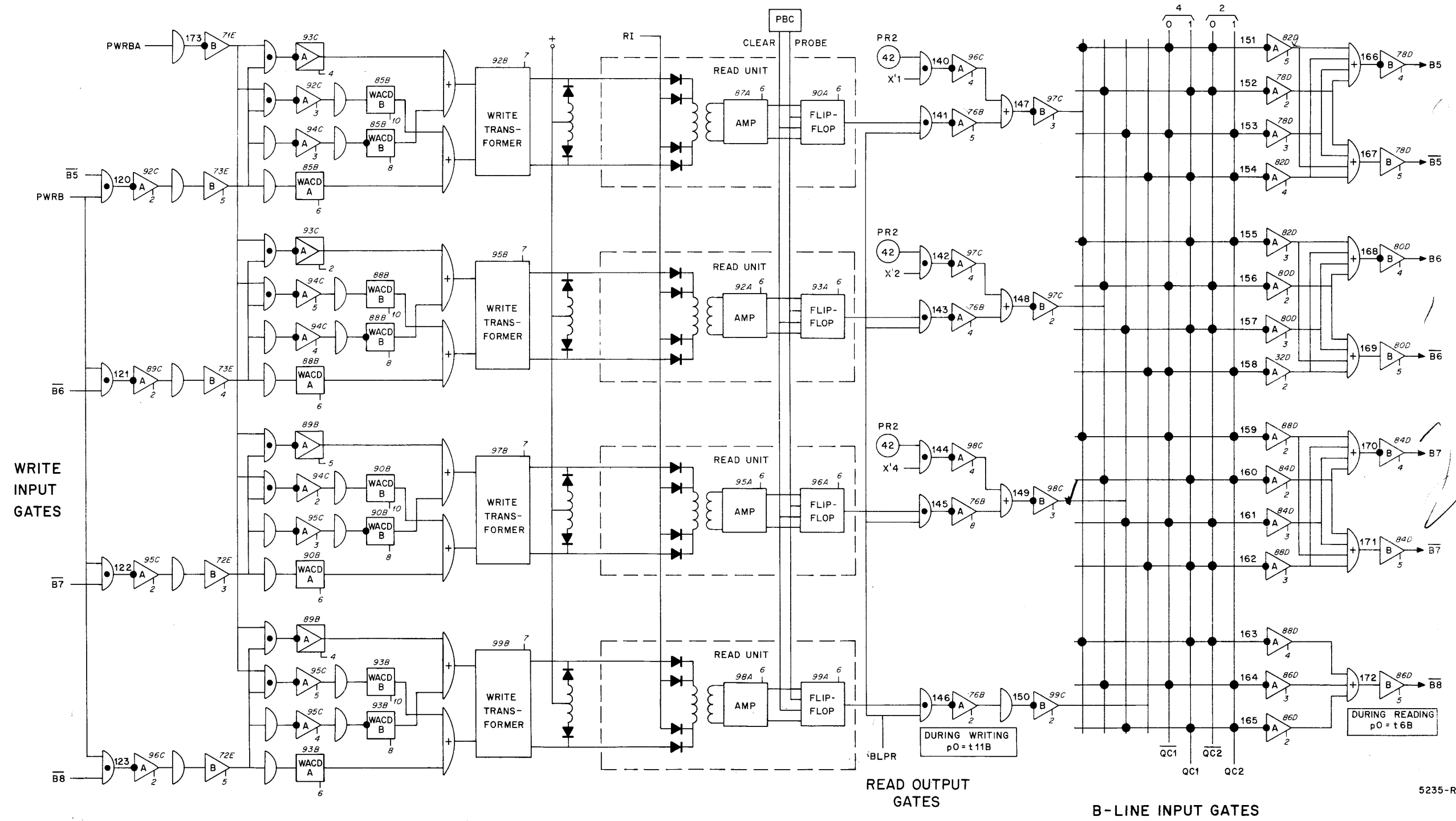
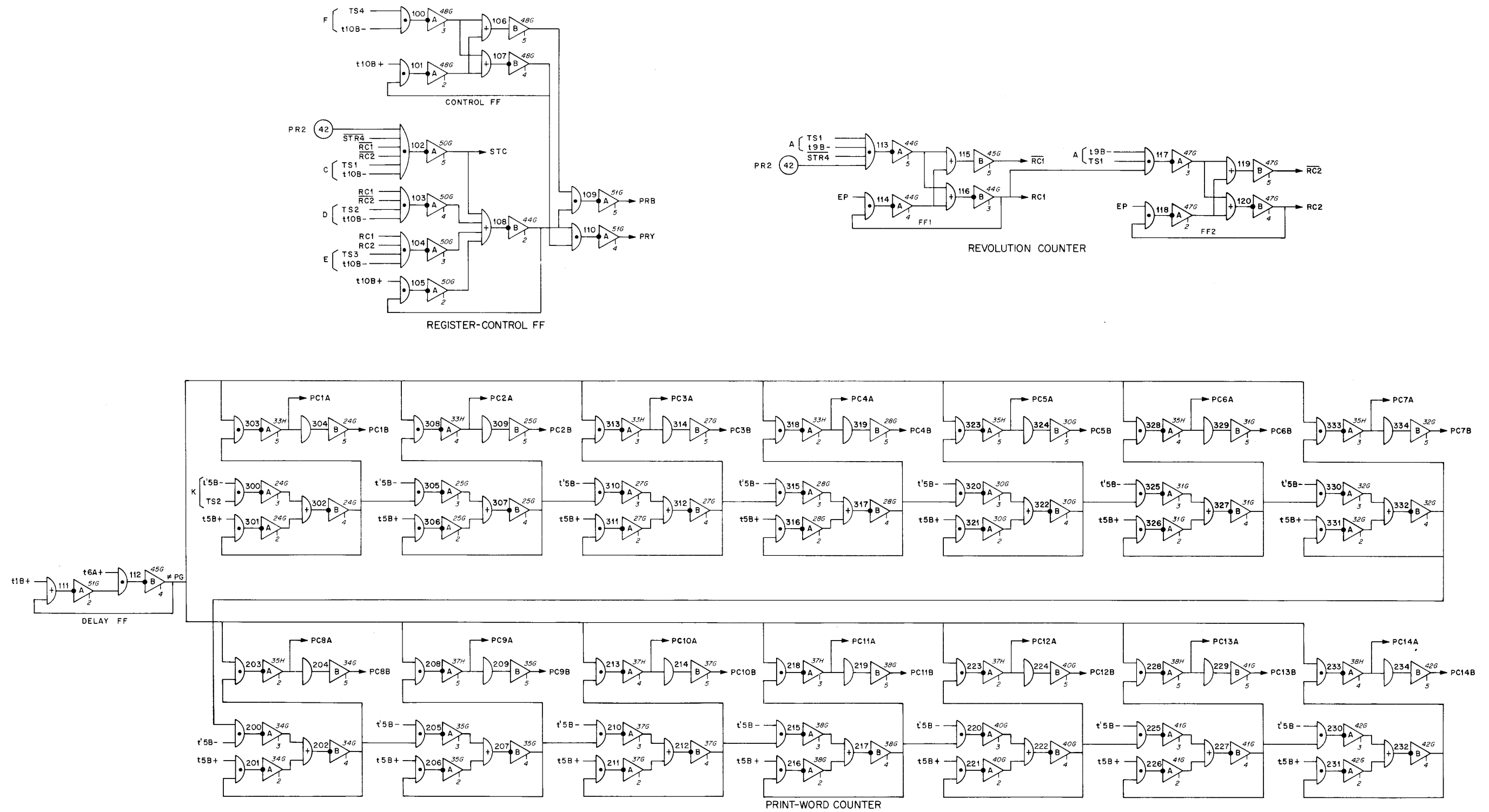


Figure 1-34B. Print-Buffer Track 1



5235-R1

Figure 1-35B. Print-Buffer Track 2



5236-R1

Figure 1-36B. Memory-To-Print-Buffer Control, Models 130A, 131A, 154, 159, 176, and 184

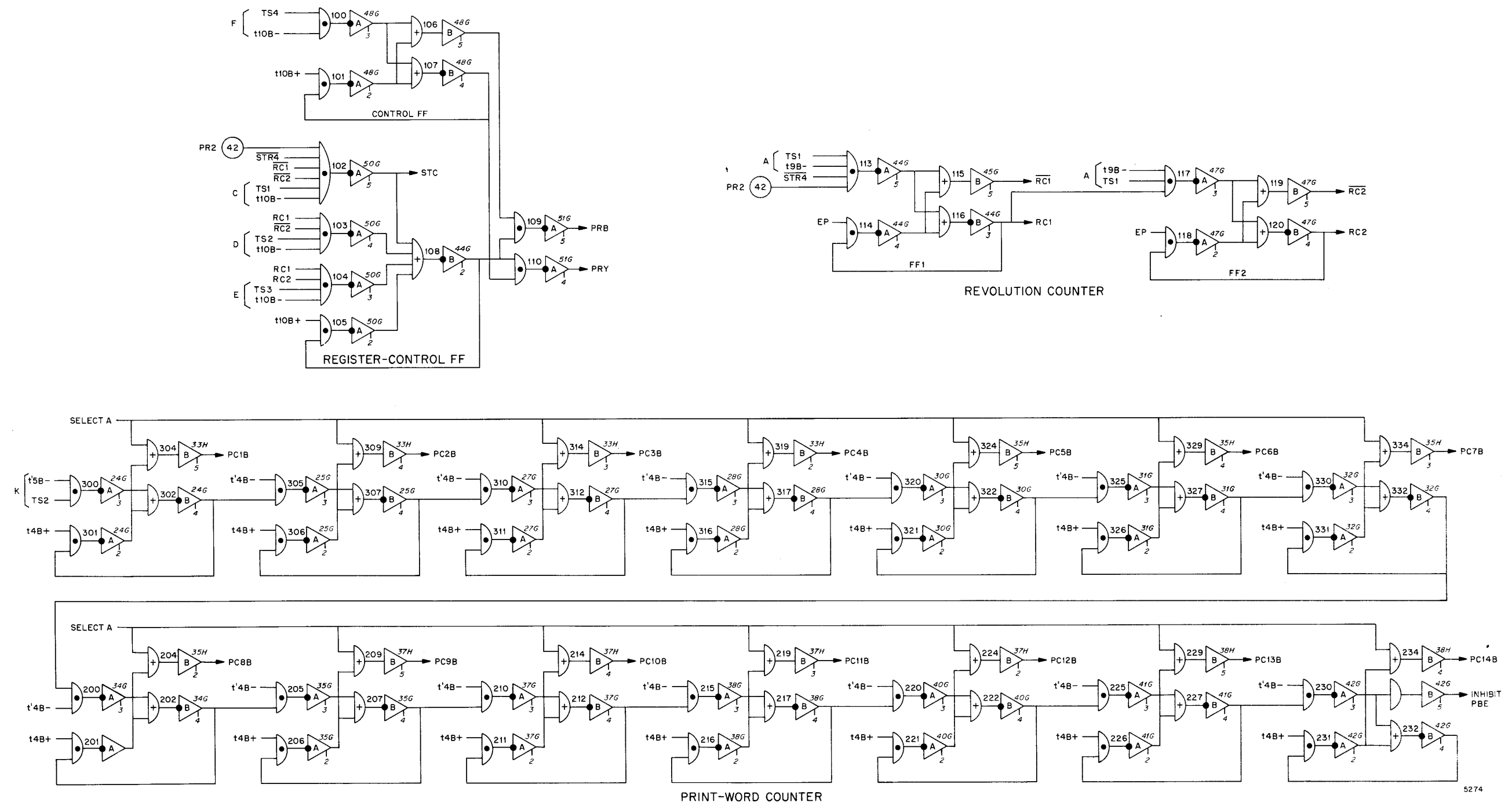


Figure 1-36B. Memory-To-Print-Buffer Control, Model 139

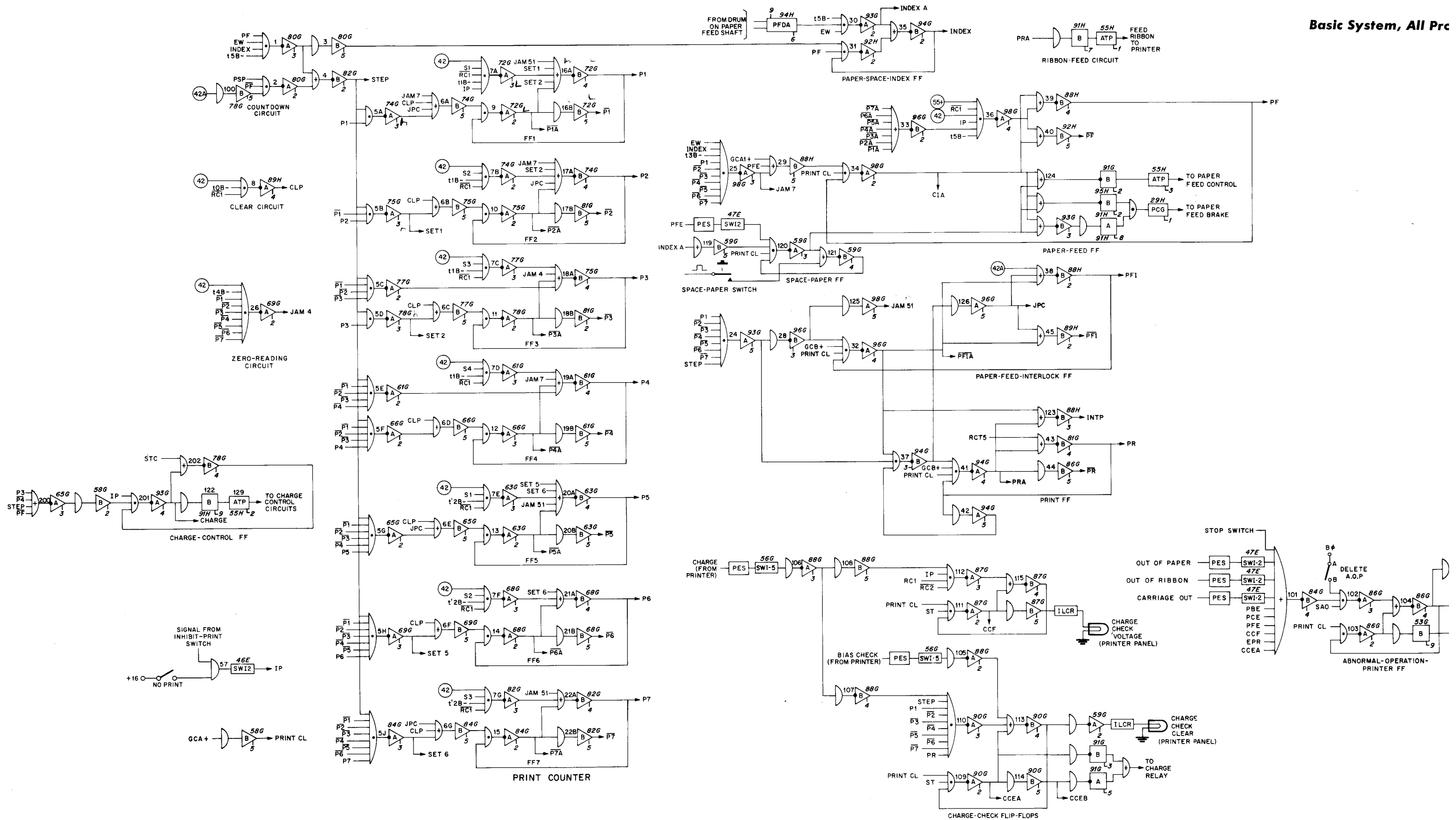


Figure 1-37B. Print Control, Models 130A, 131A, 154,

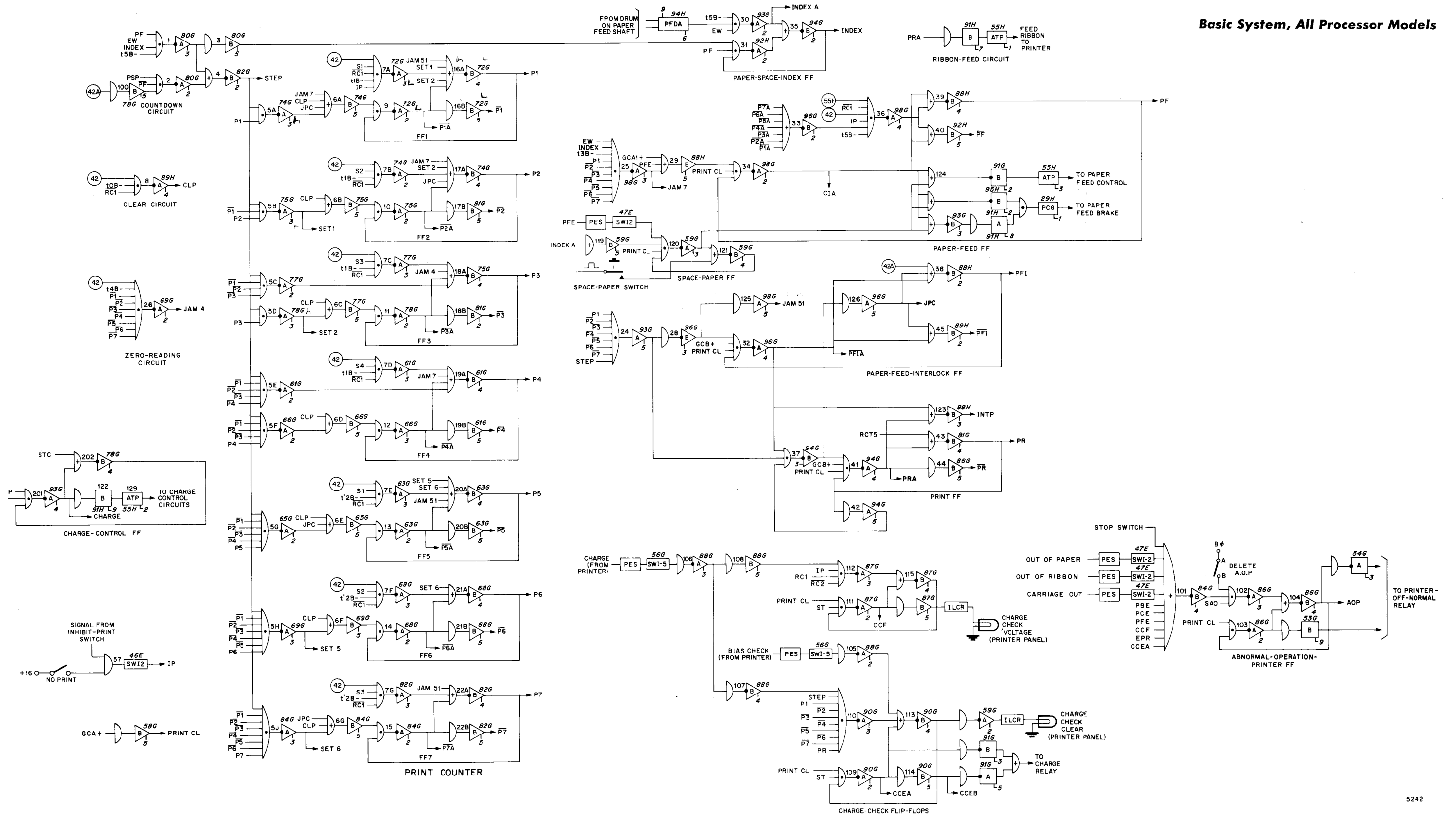
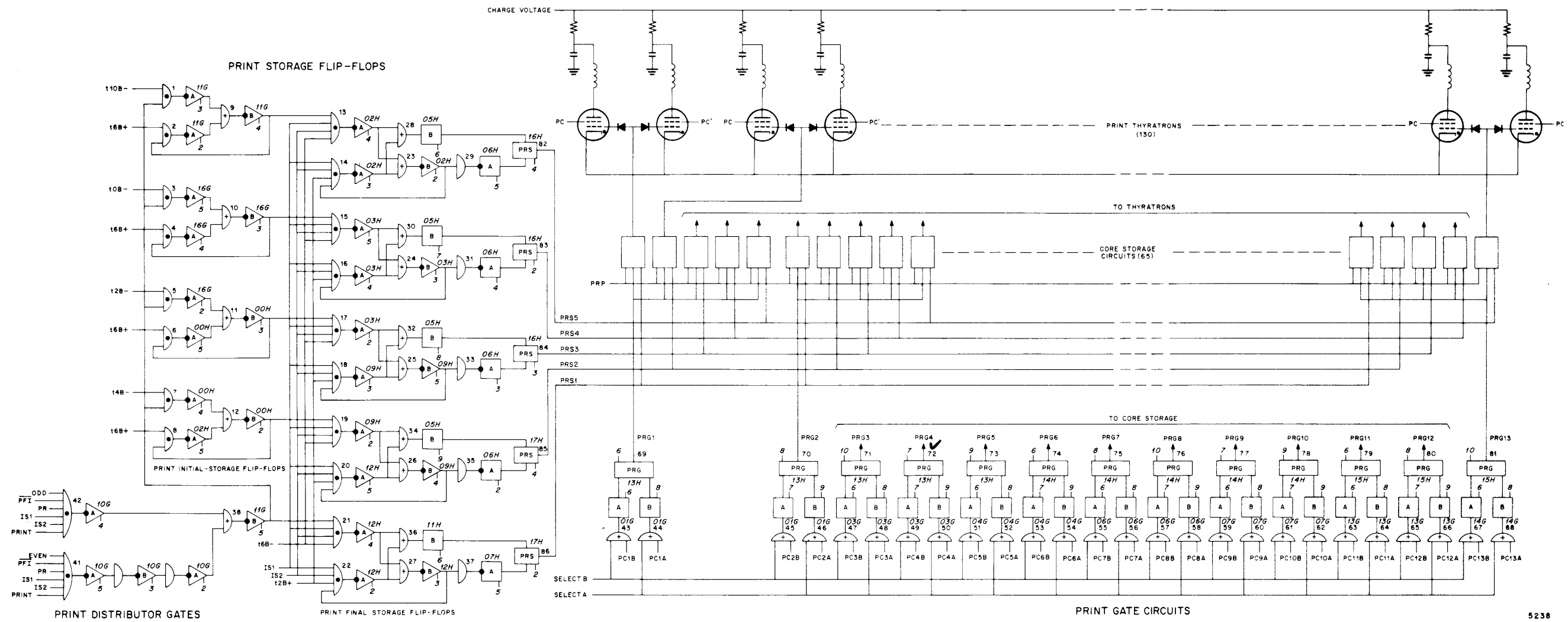


Figure 1-37B. Print Control, Models 130A, 131A, 154, 159, 176, and 184



5238

Figure 1-38B. Print Distributor, Models 130A, 131A, 154, 159, 176, and 184

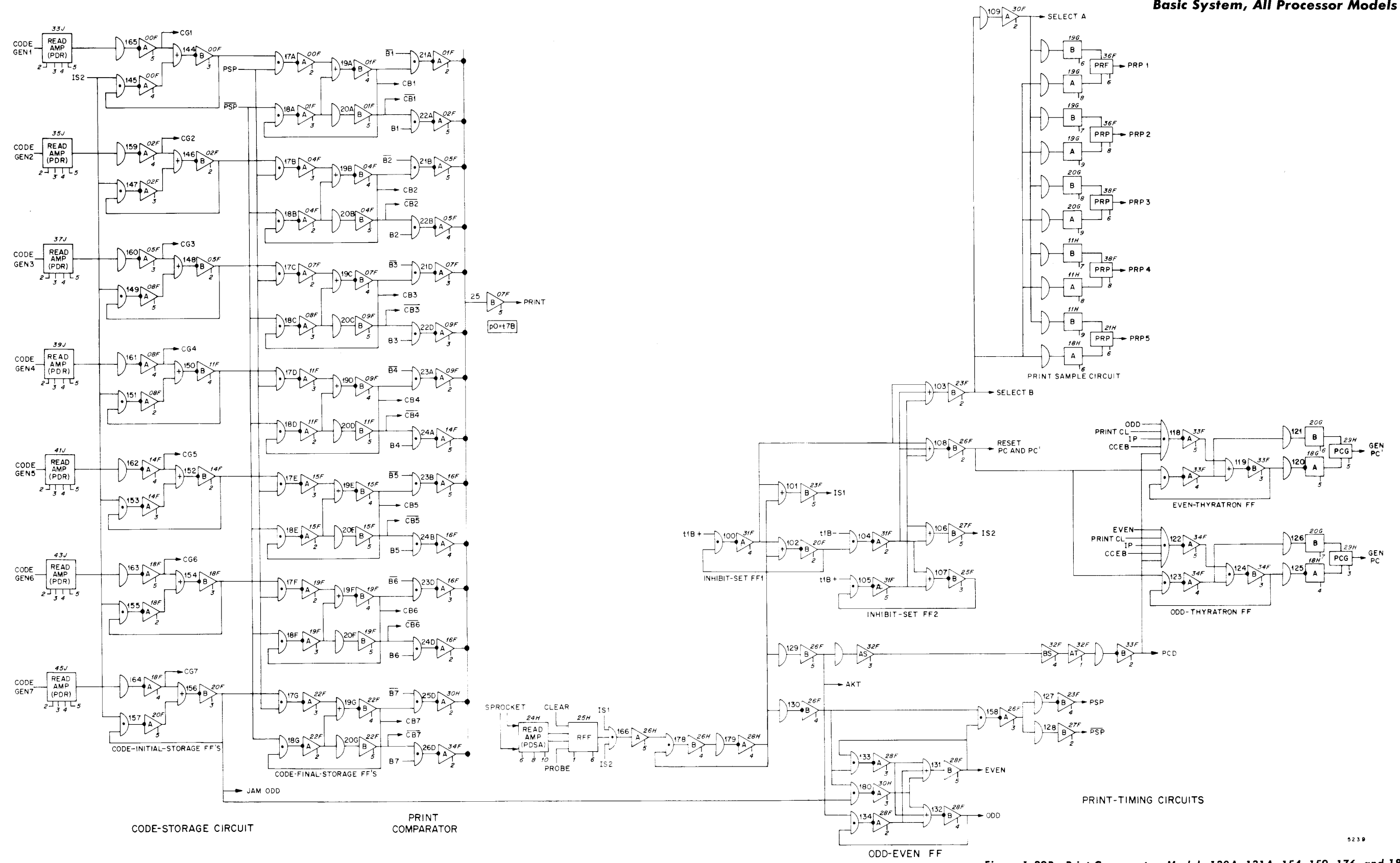


Figure 1-39B. Print Comparator, Models 130A, 131A, 154, 159, 176, and 184

Basic System, All Processor Models

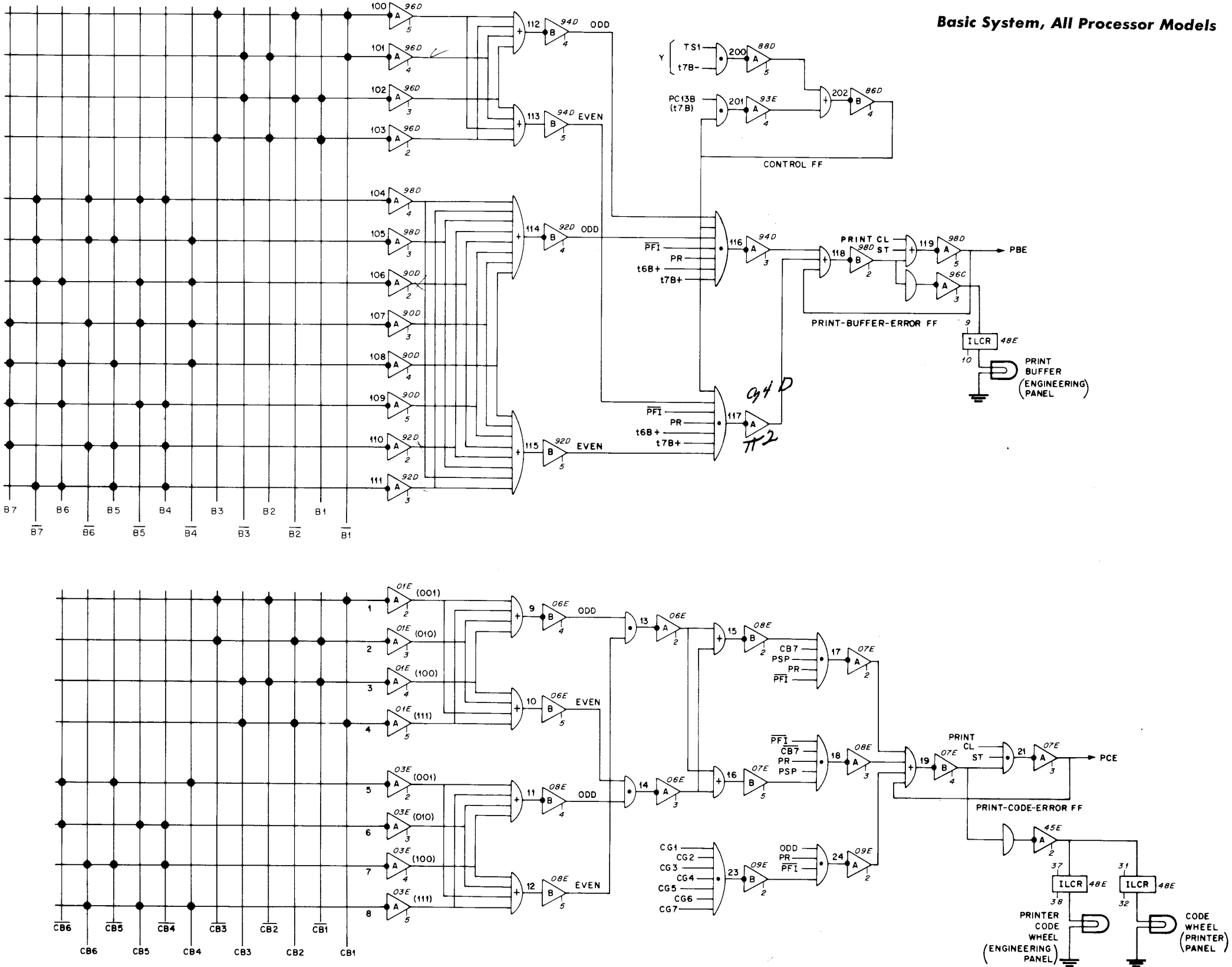
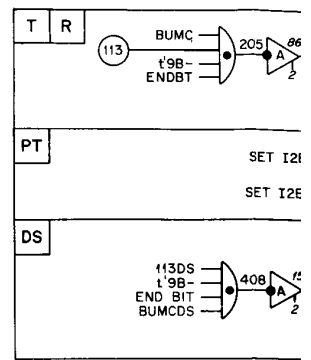
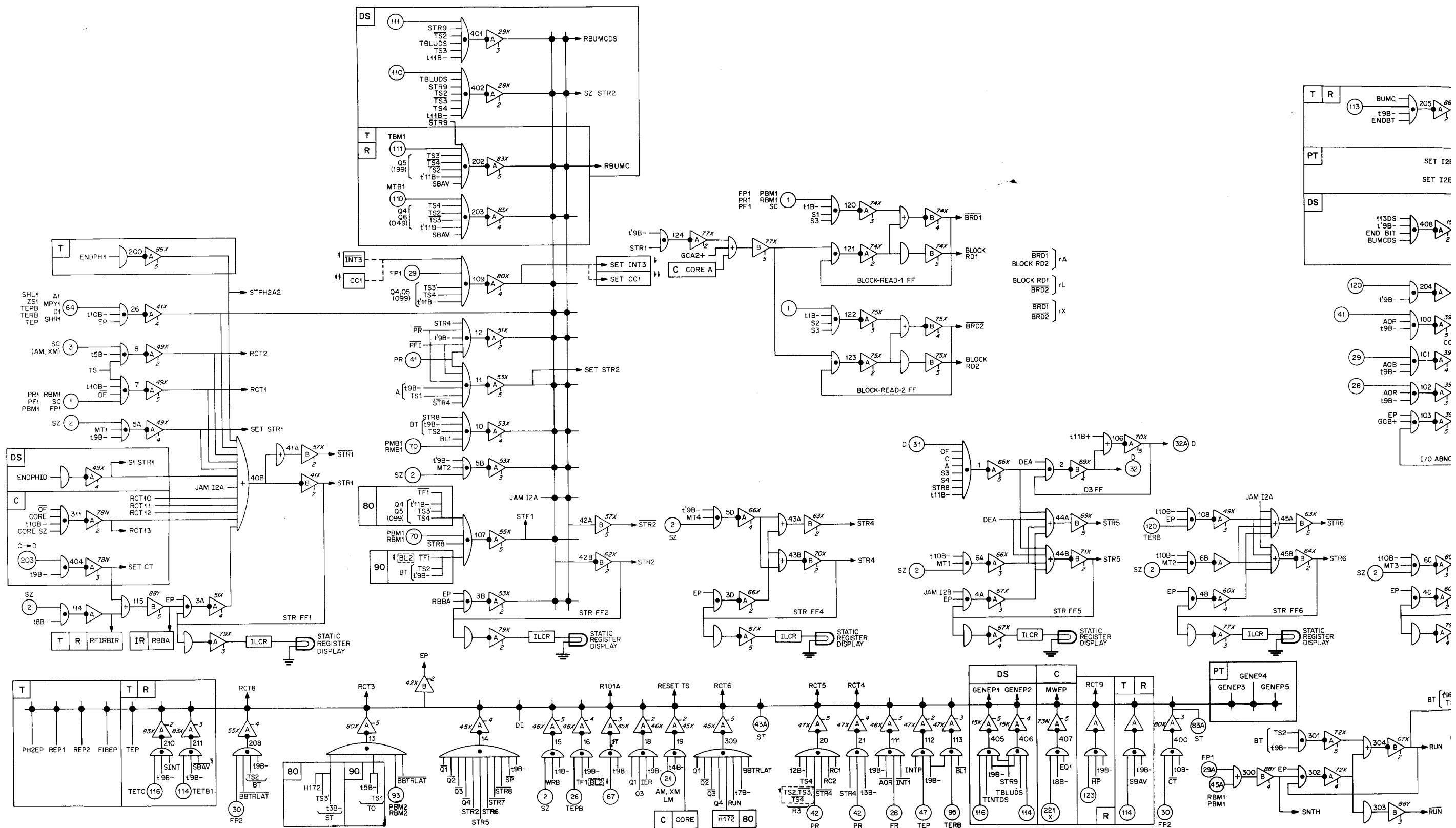


Figure 1-40B. Print-Code and Print-Buffer Error Flip-Flops, Models 130A, 131A, 154, 159, 176, and 184



† PROCESSOR MODELS 154 AND 130A
 †† PROCESSOR MODELS 159 AND 131A

ENDING-PULSE BUFFER

RUN FLIP-FLOPS

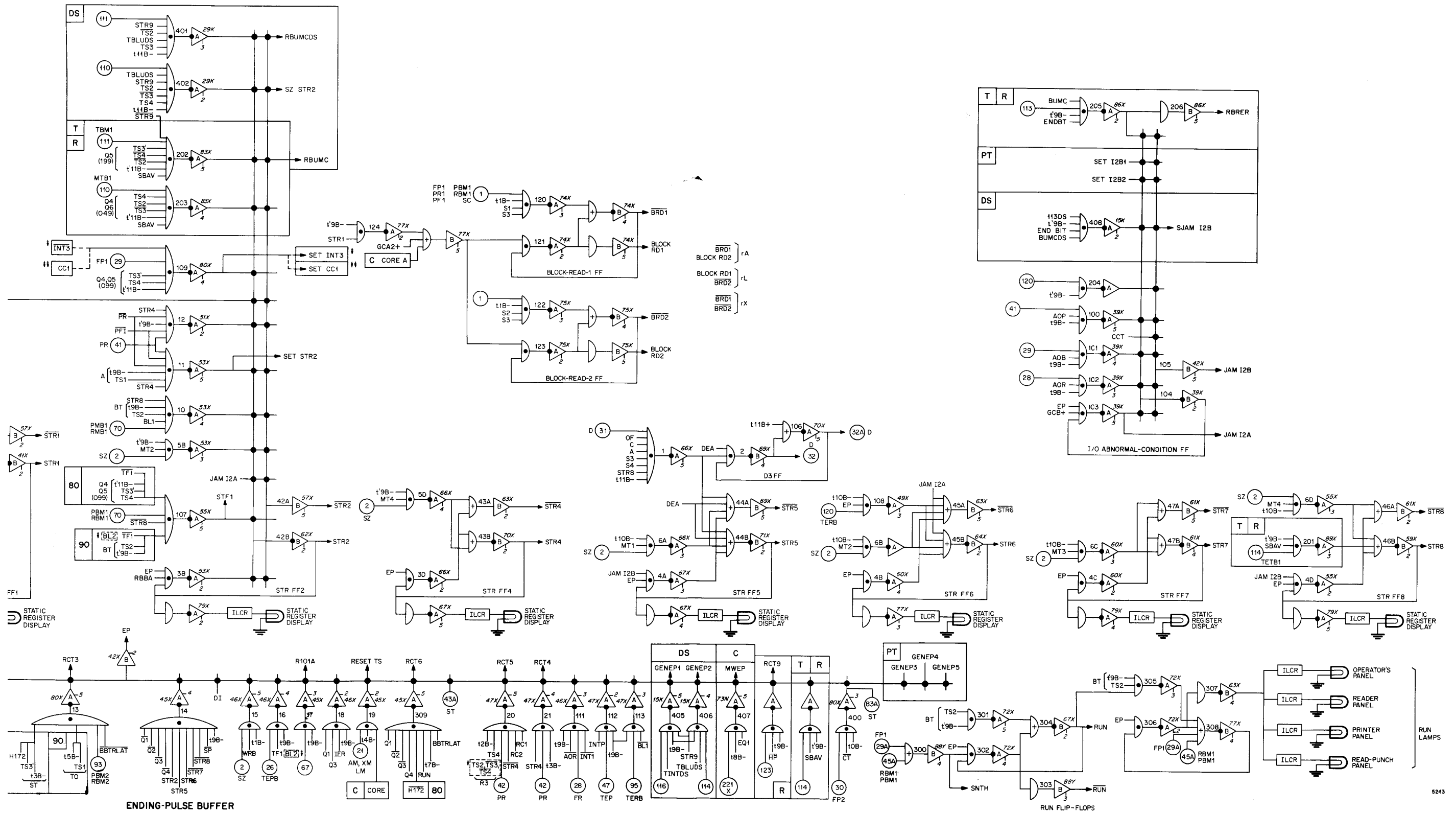
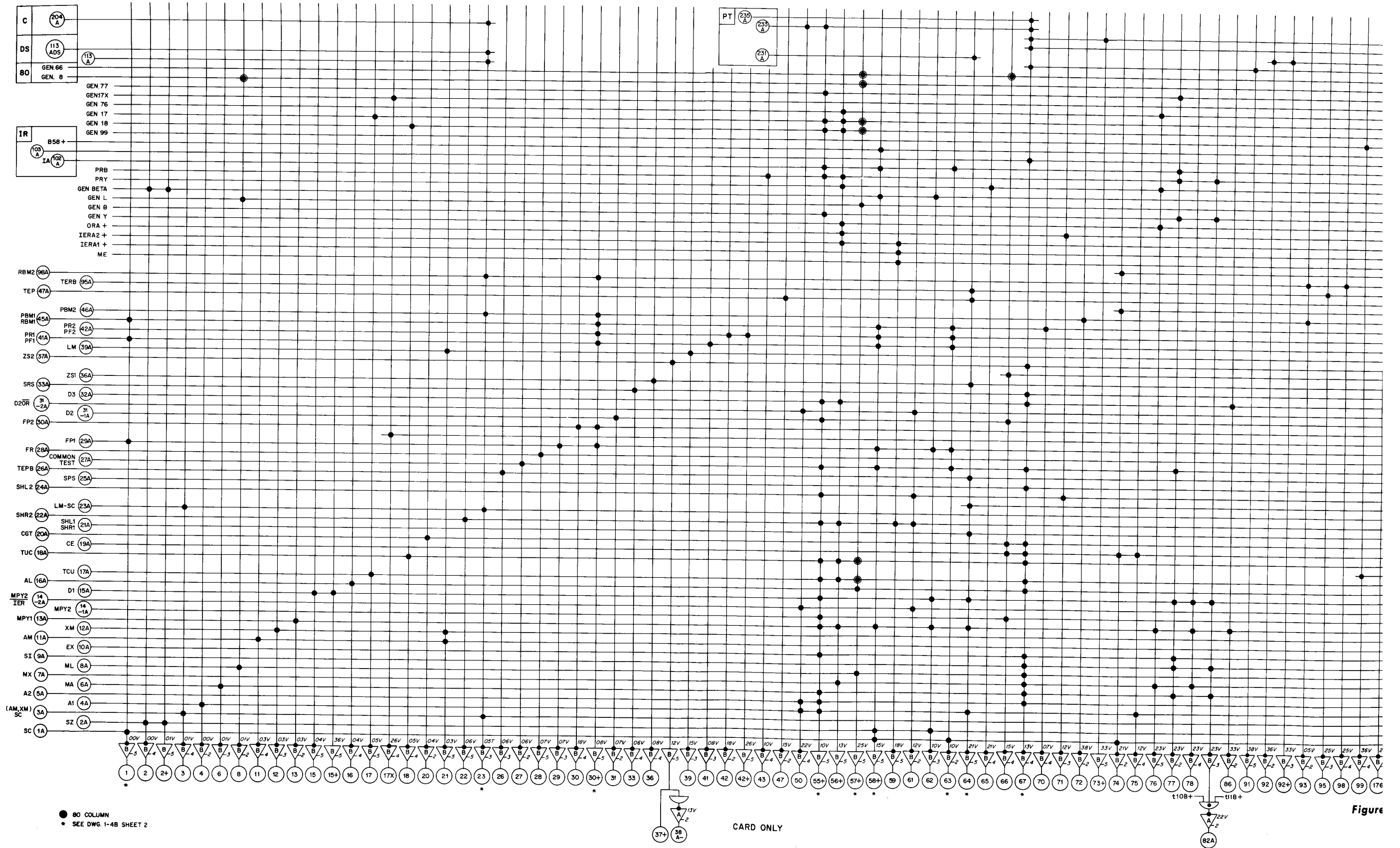


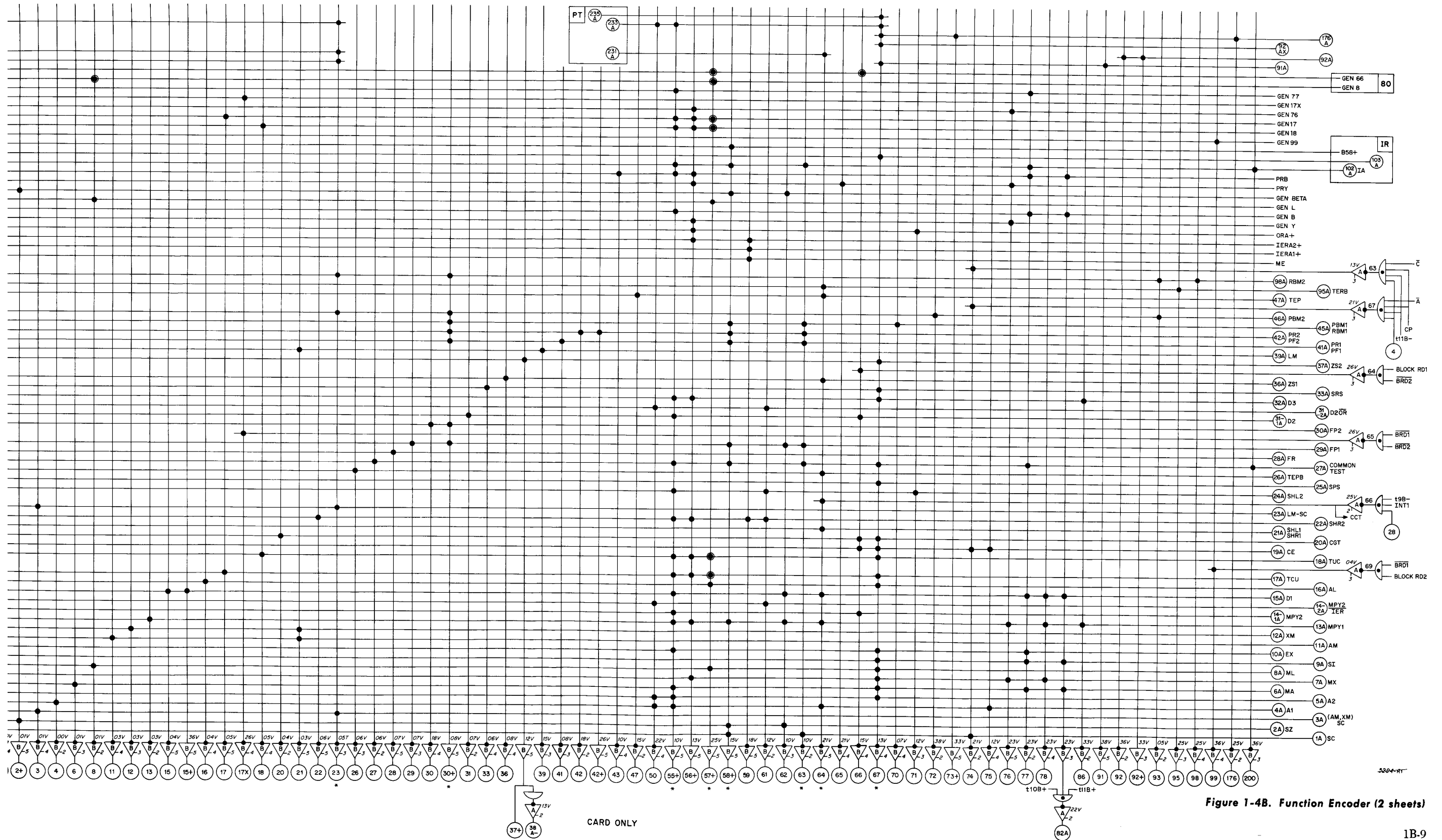
Figure 1-2B. Static Register, Models 176 and 184

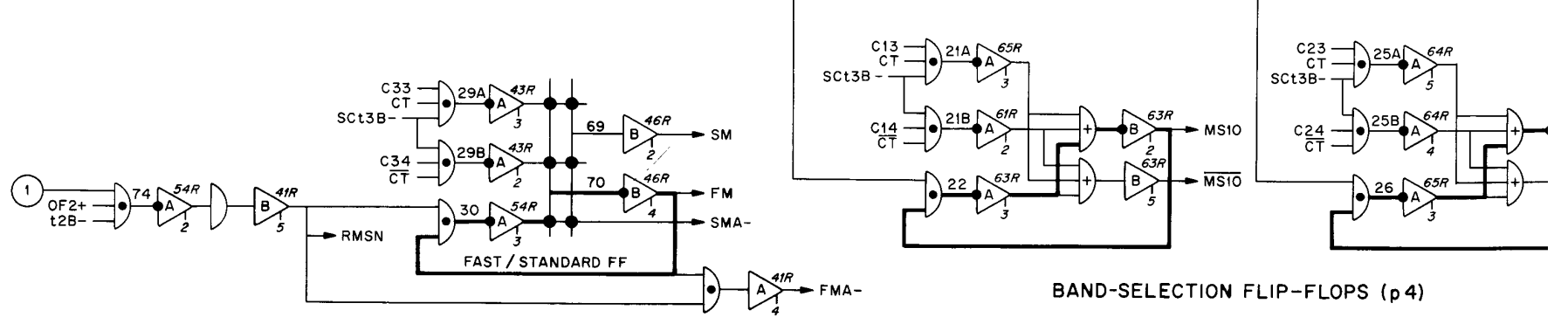
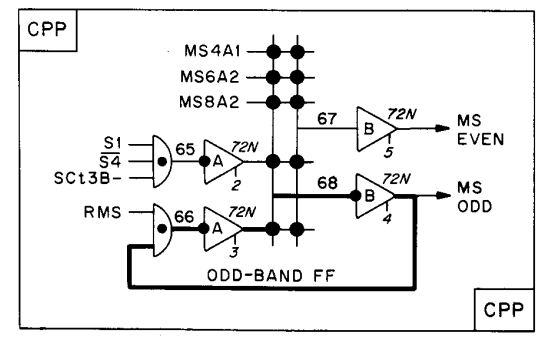
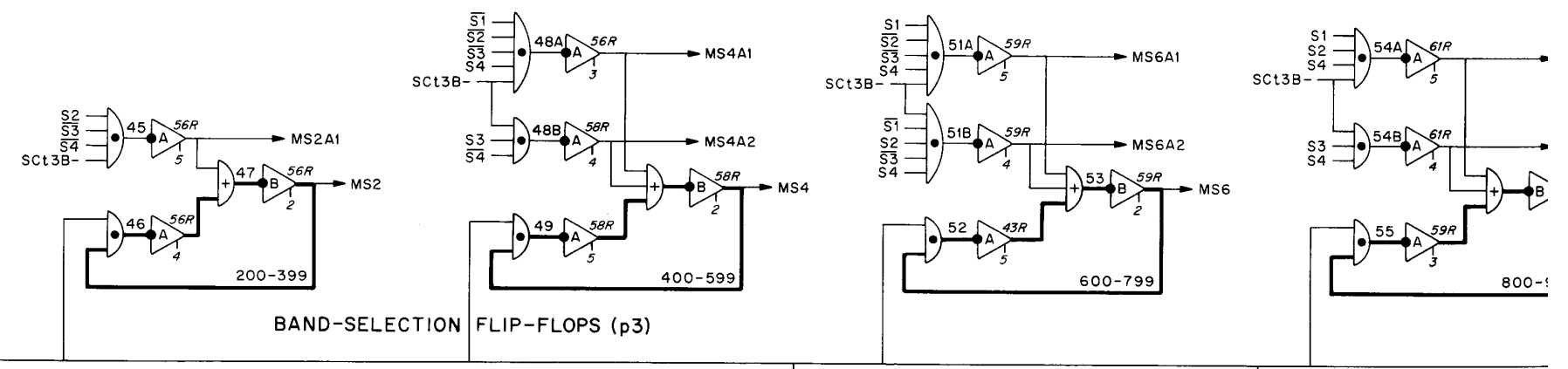
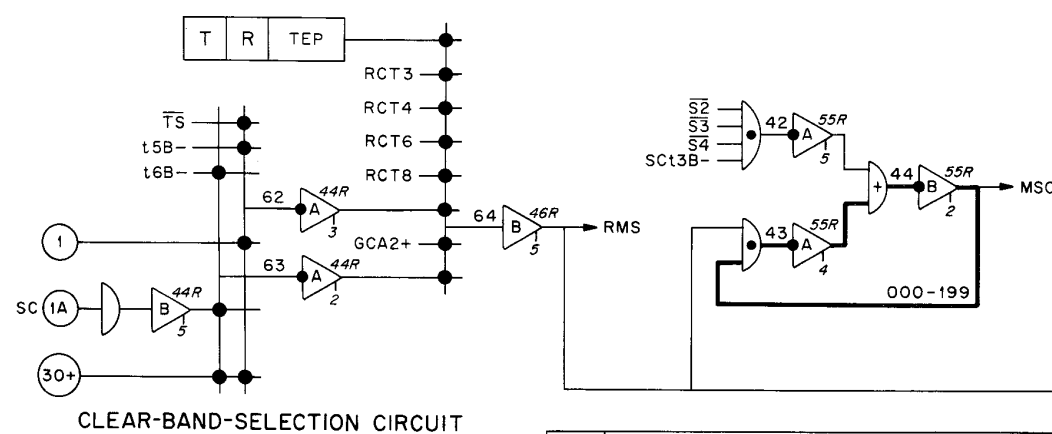
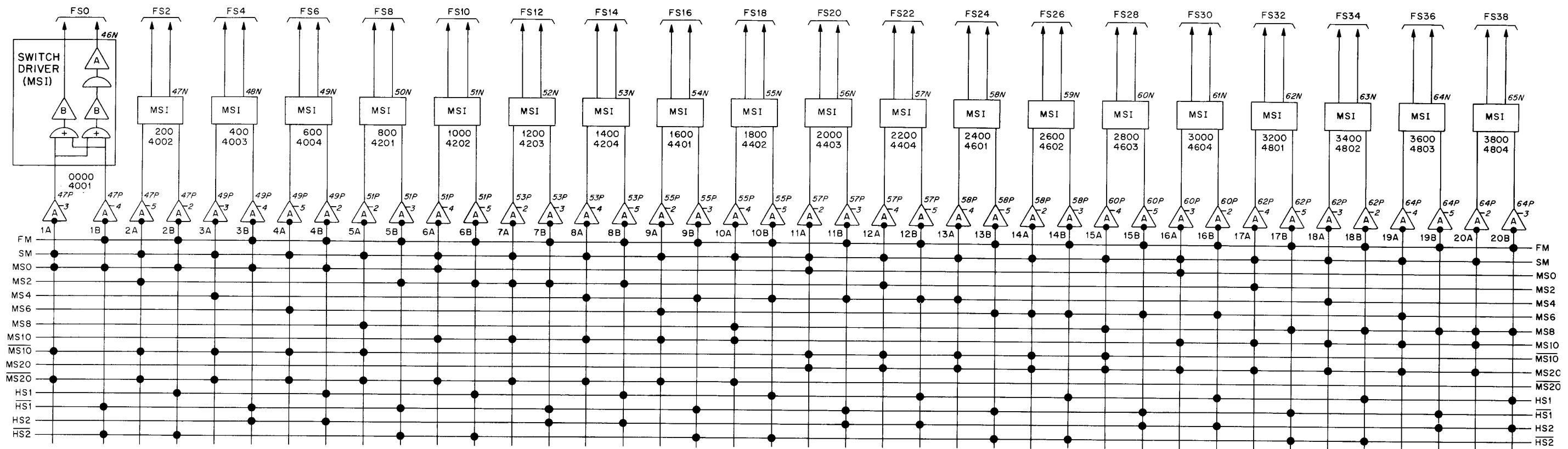


● 80 COLUMN
● SEE DWG. 1-4B SHEET 2

CARD ONLY

Figure





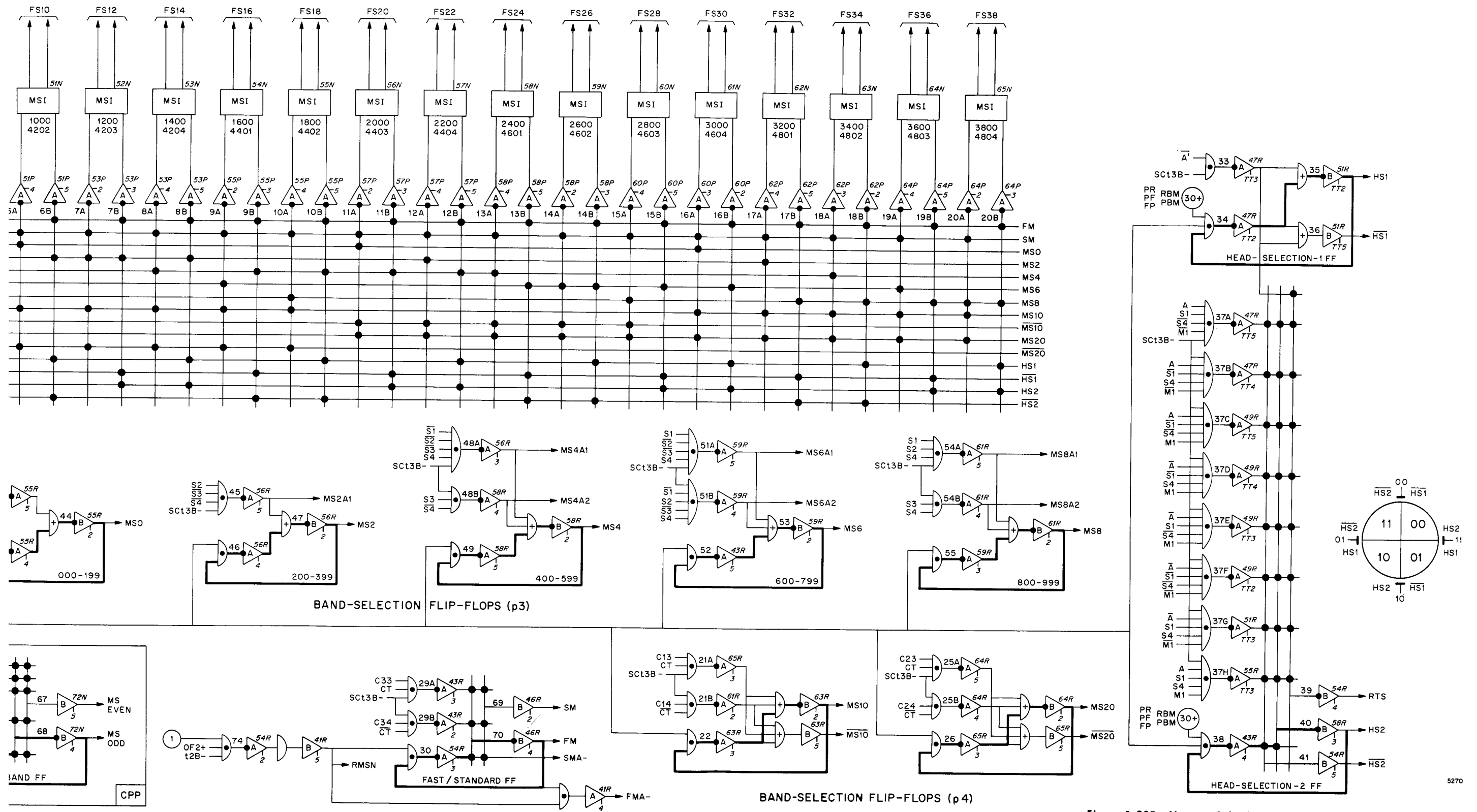
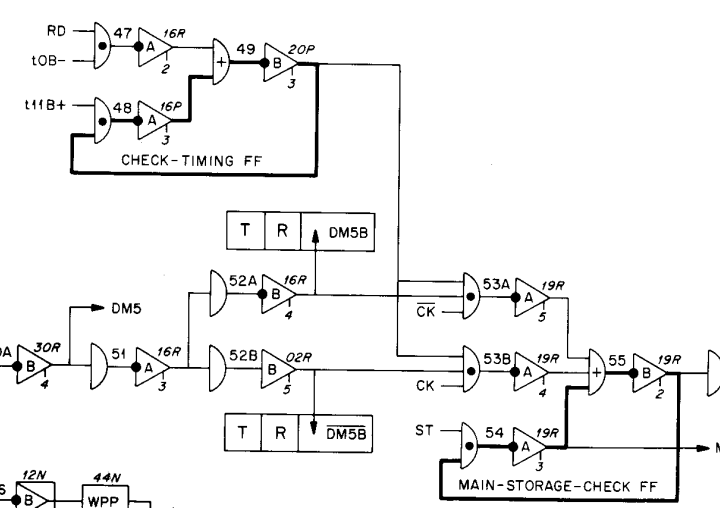
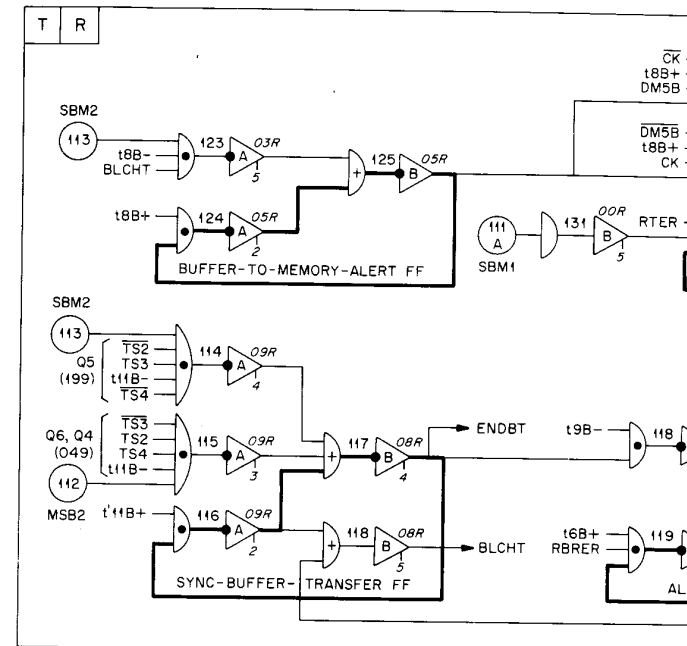
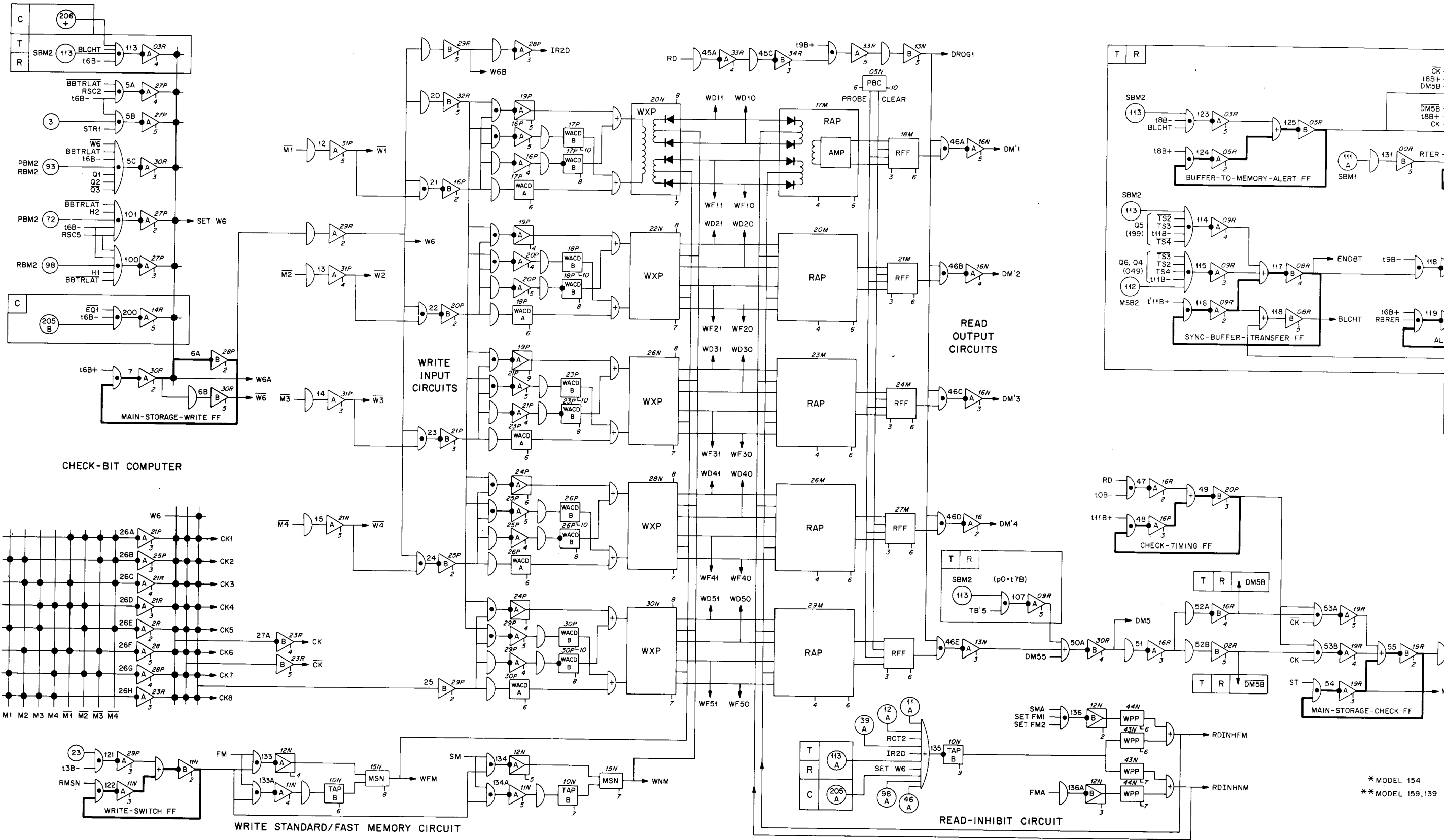


Figure 1-20B. Memory Selection, Models 139, 154, 159, 176, and 184



* MODEL 154
 ** MODEL 159, 139

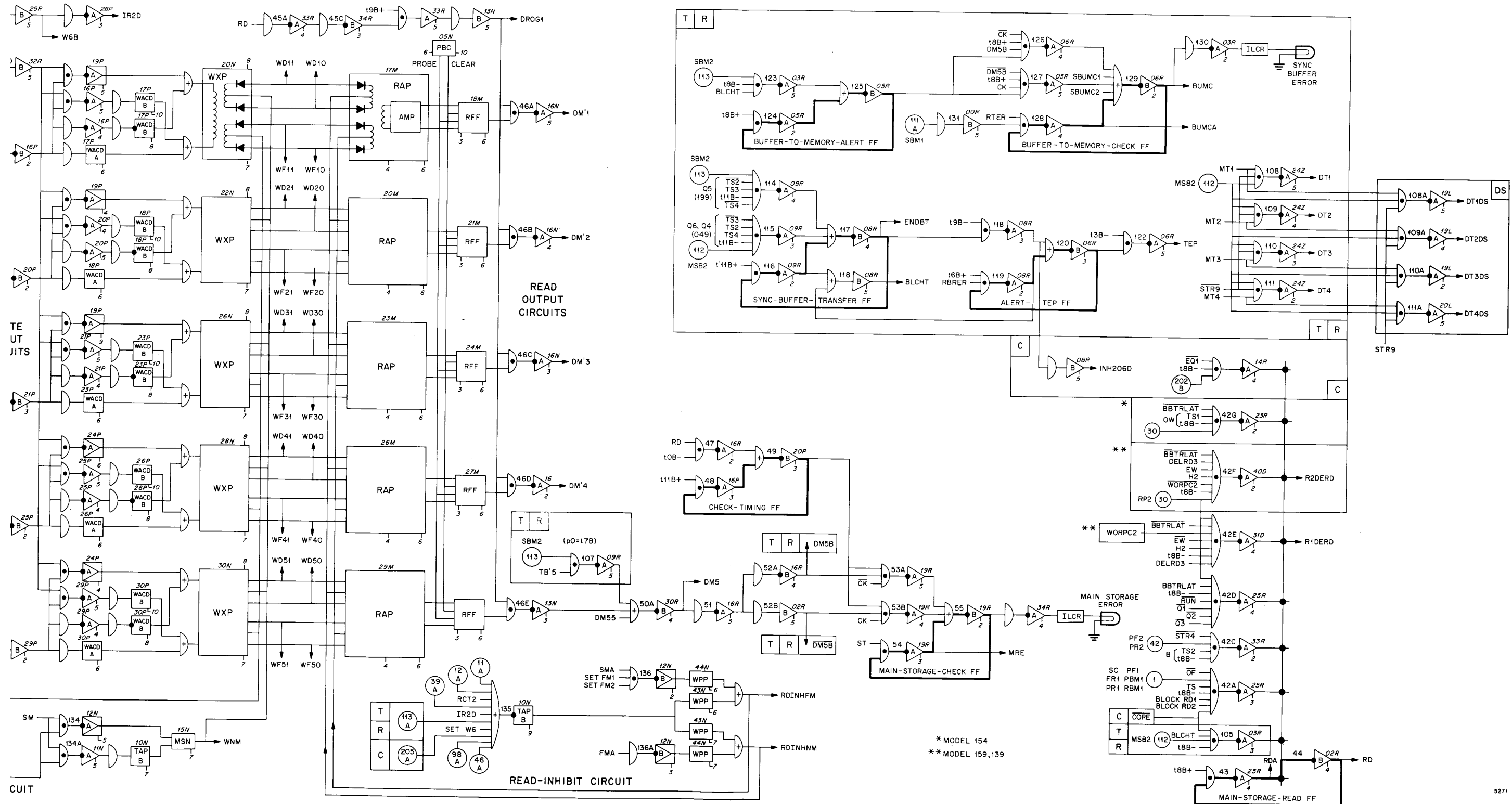


Figure 1-21B. Section-A-Access Read/Write Circuits, Models, 139, 154, 159, 176, and 184

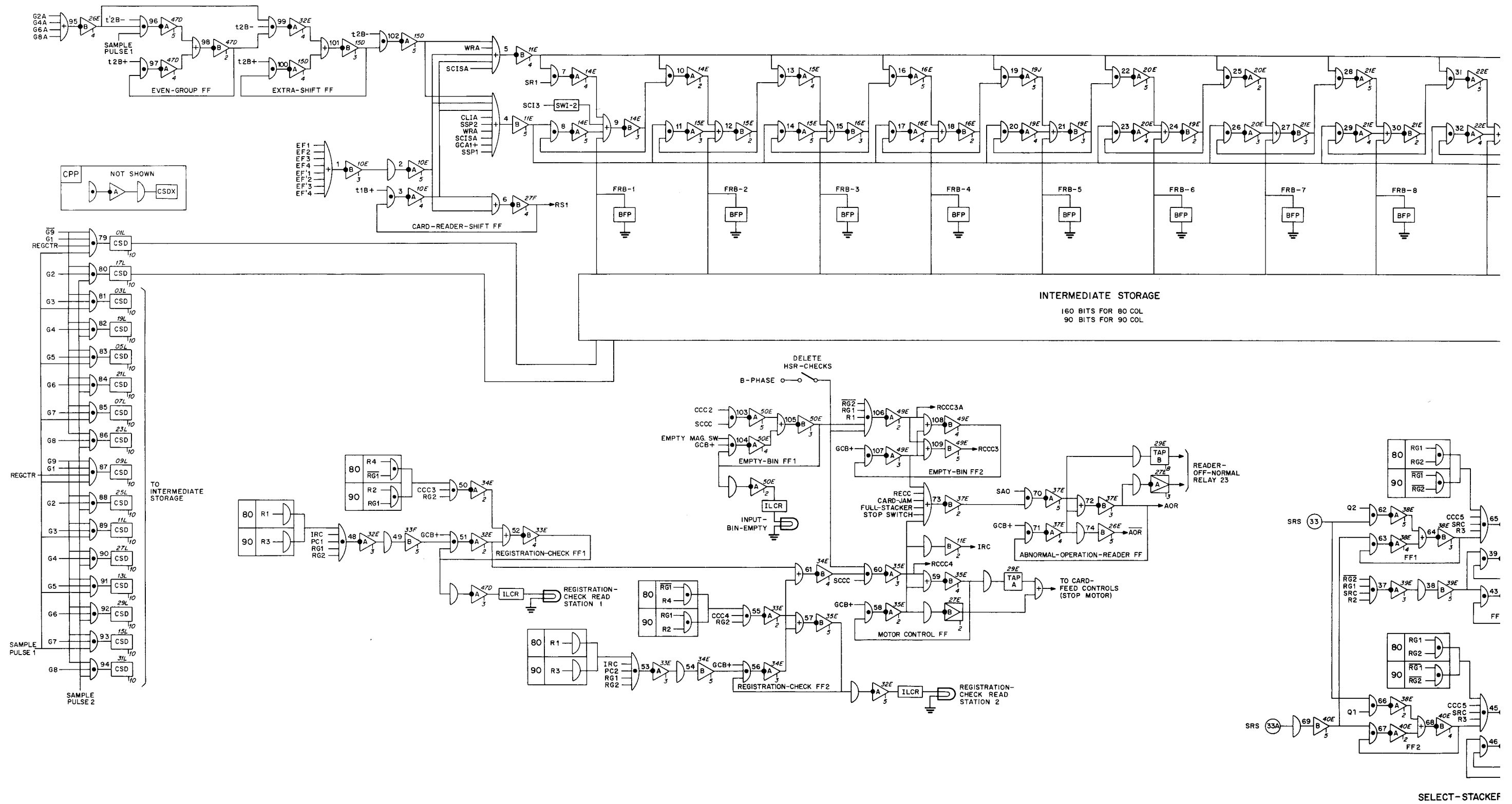


Figure 1-26B. Card-Reader Shift Register

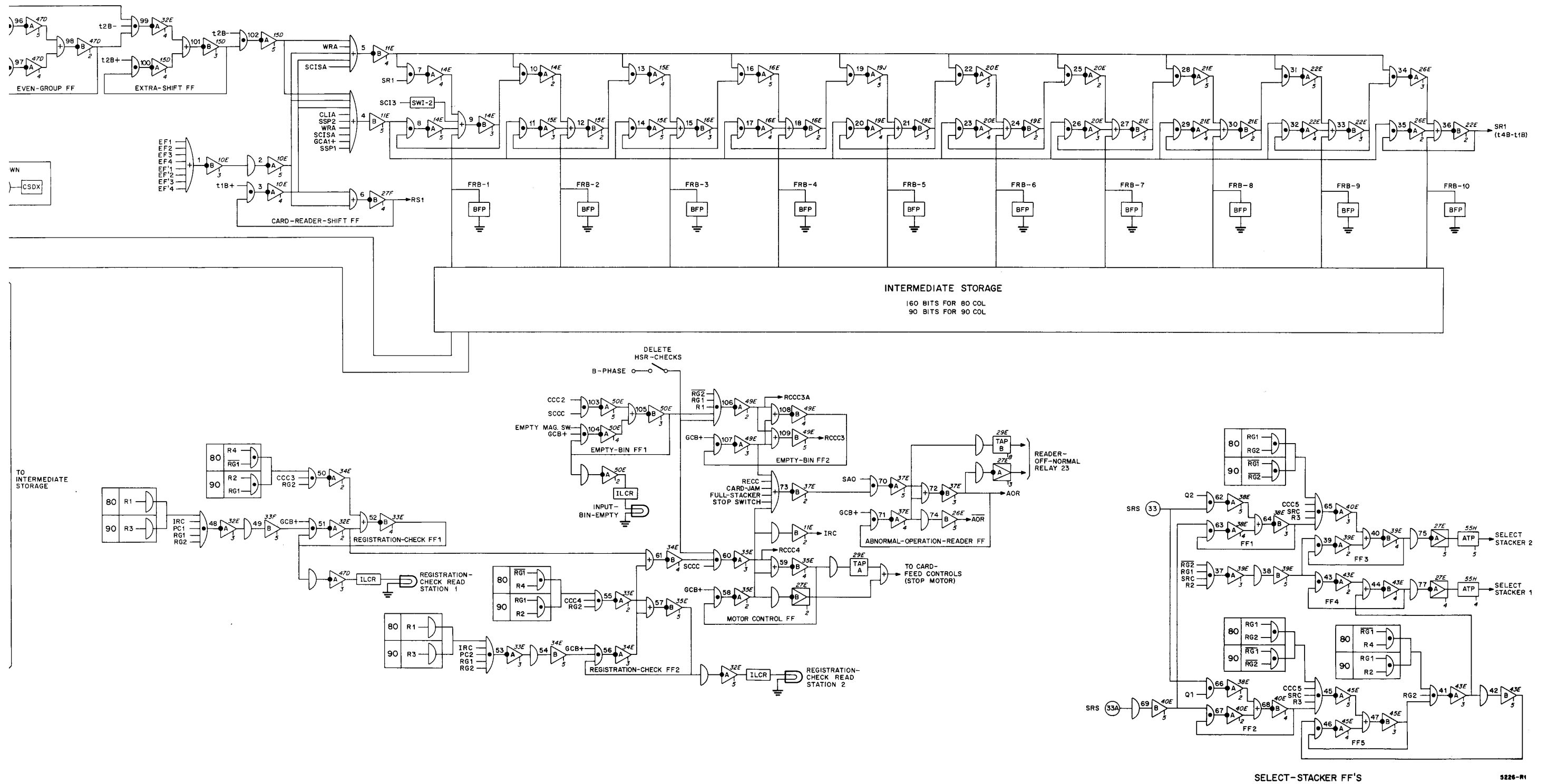


Figure 1-26B. Card-Reader Shift Register, Models 131A, T39, 159, and 184

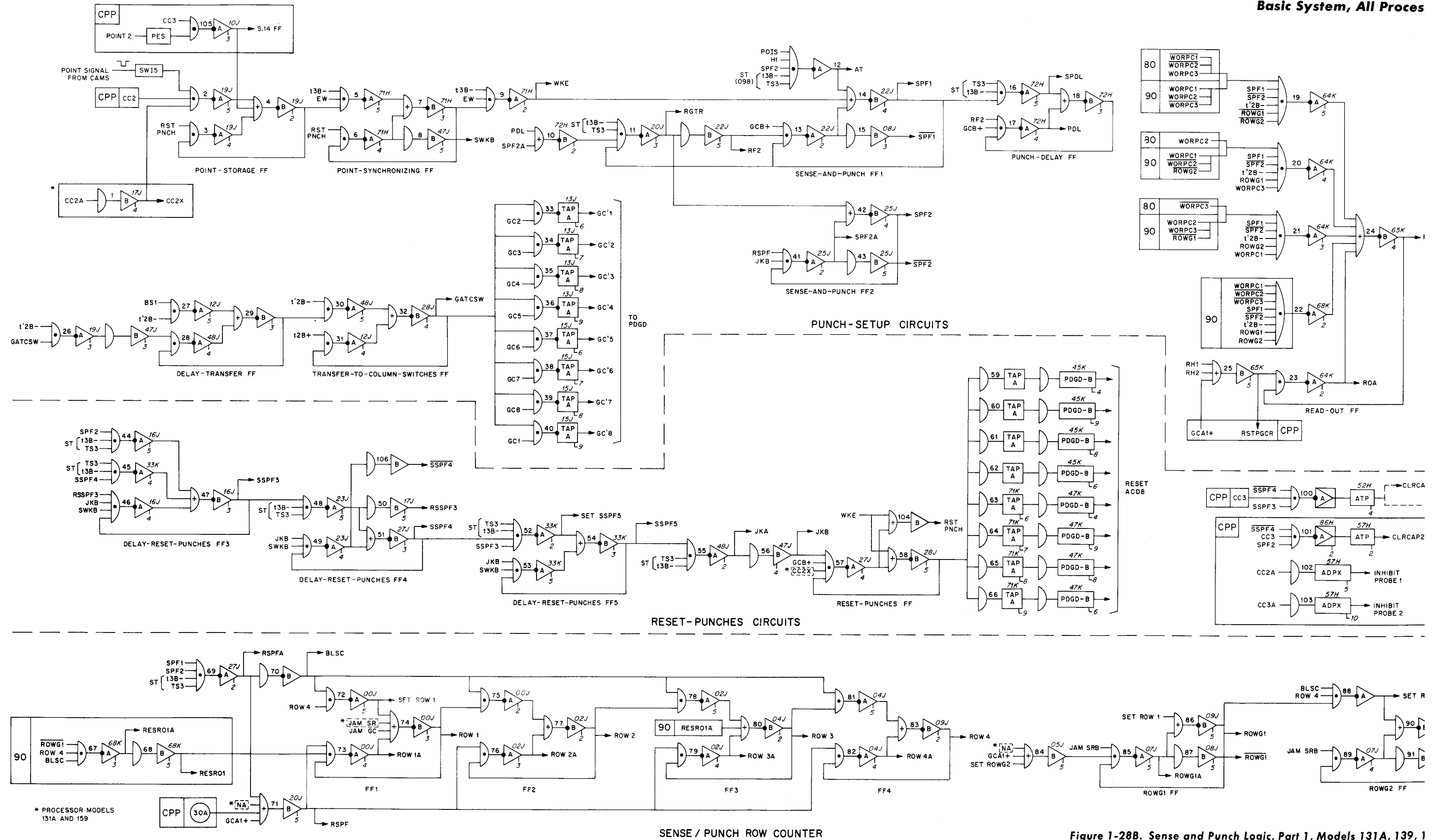


Figure 1-28B. Sense and Punch Logic, Part 1, Models 131A, 139, 1

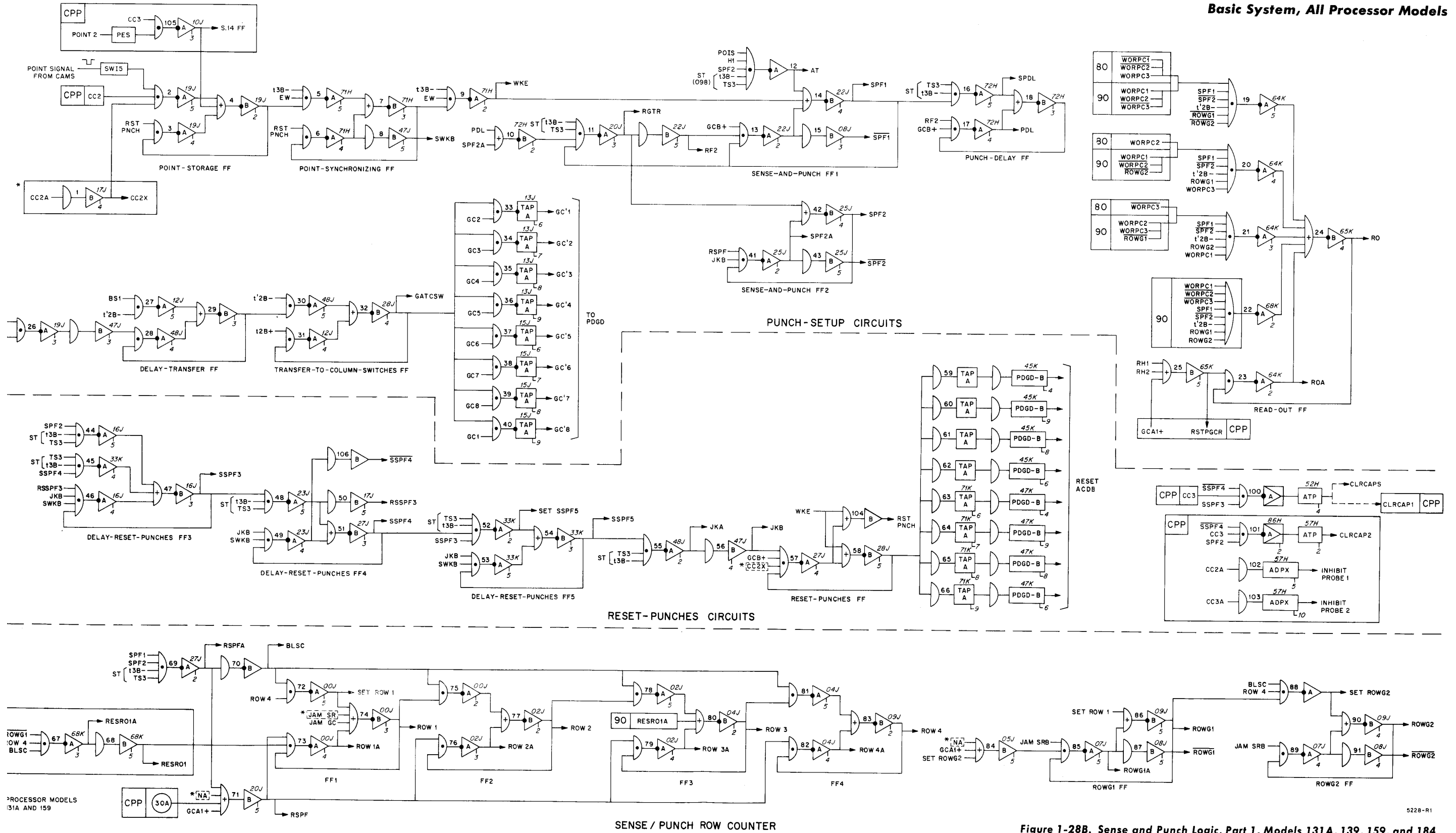
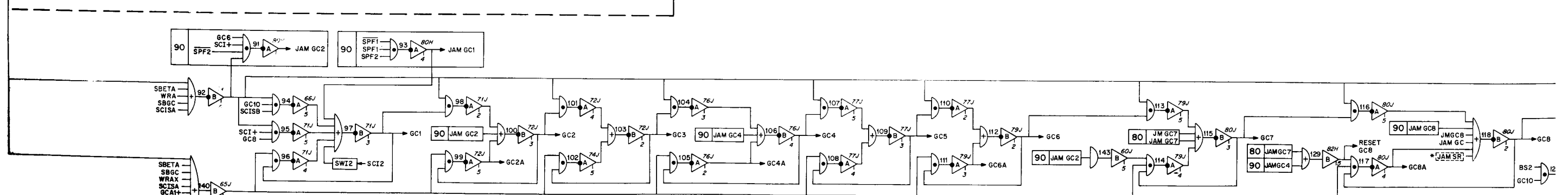
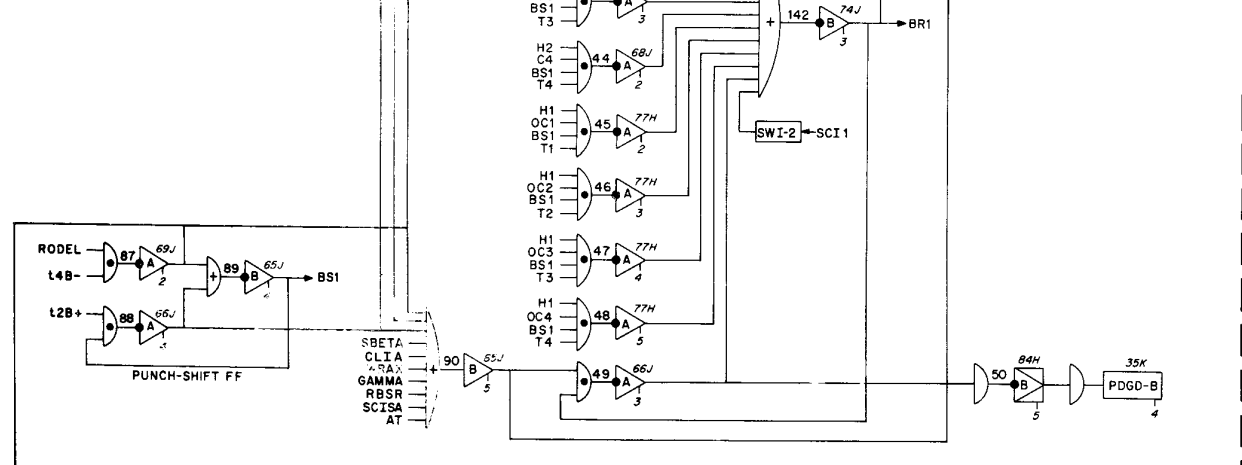
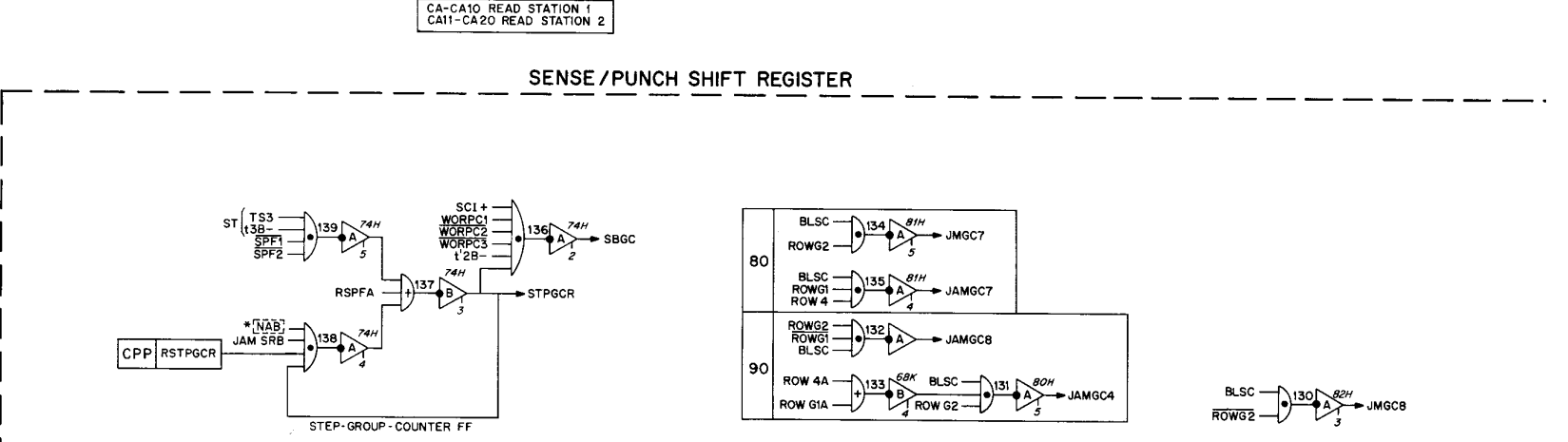
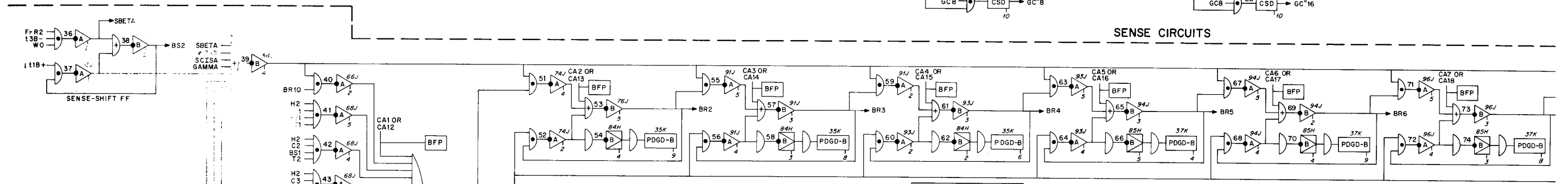
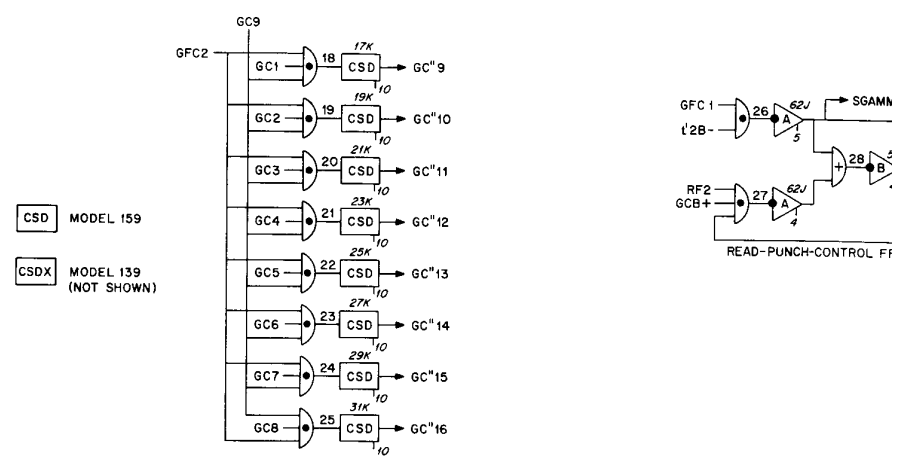
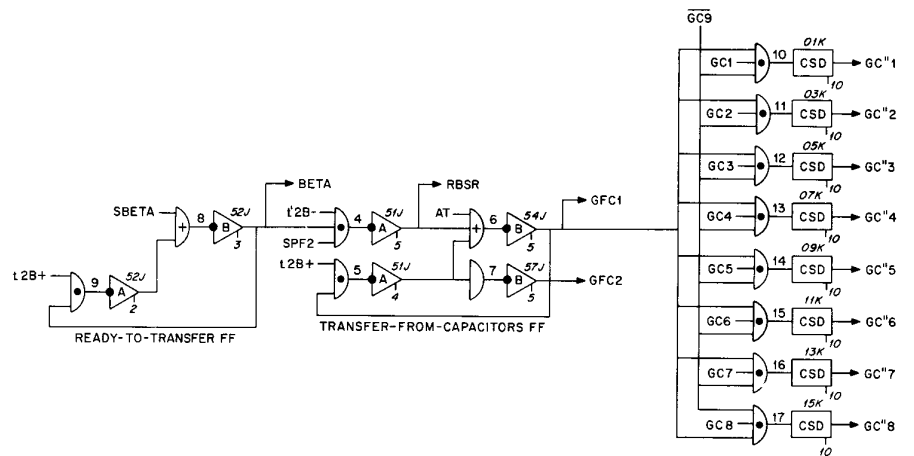
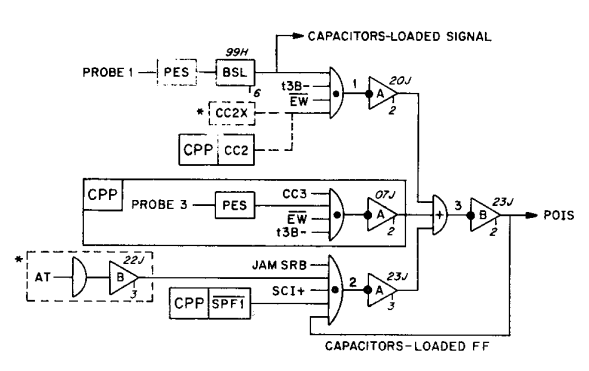


Figure 1-288. Sense and Punch Logic, Part 1, Models 131A, 139, 159, and 184

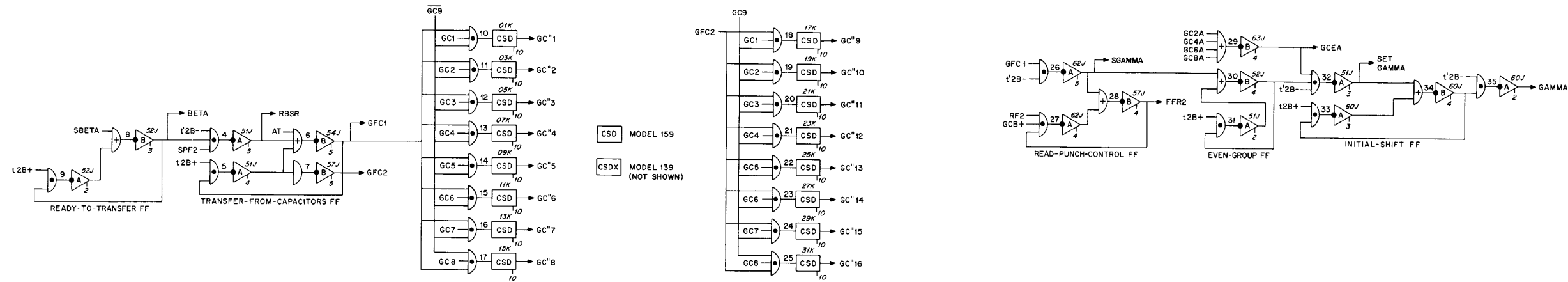
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PROCESSOR MODELS
131A AND 159

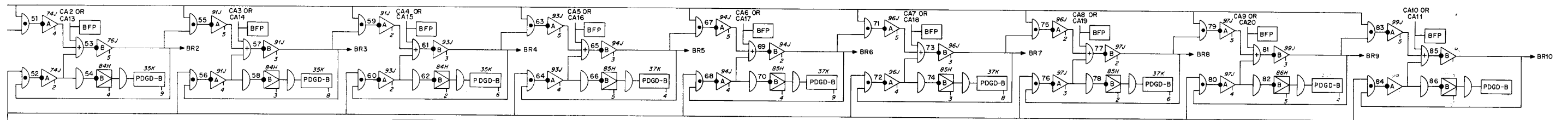


*PROCESSOR MODELS 159 AND 131A

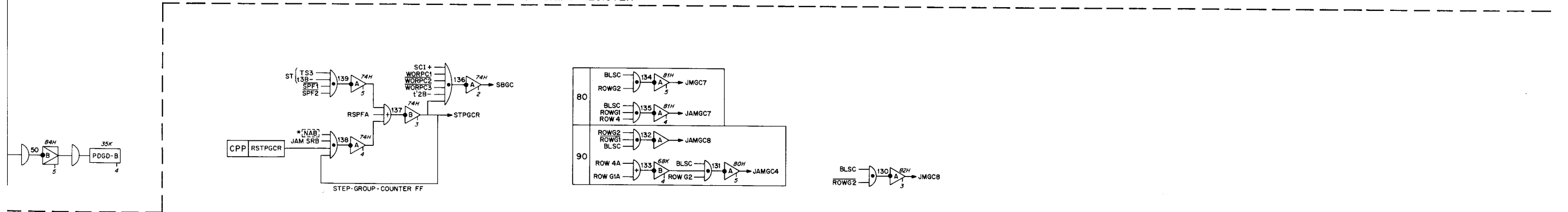
SENSE/PUNCH GROUP-COUNTER CIRCUITS



SENSE CIRCUITS



SENSE/PUNCH SHIFT REGISTER



SENSE/PUNCH GROUP - COUNTER CIRCUITS

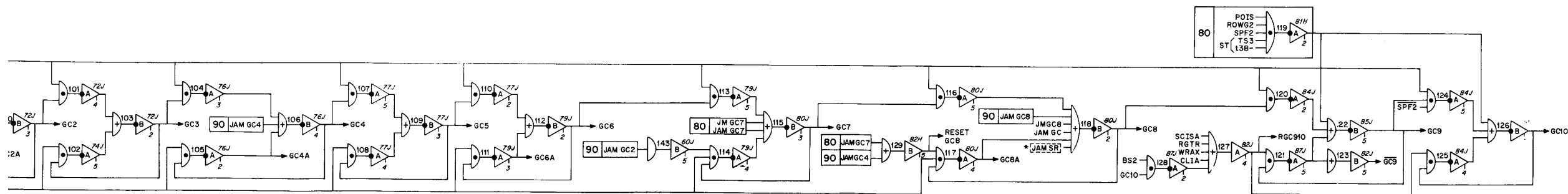
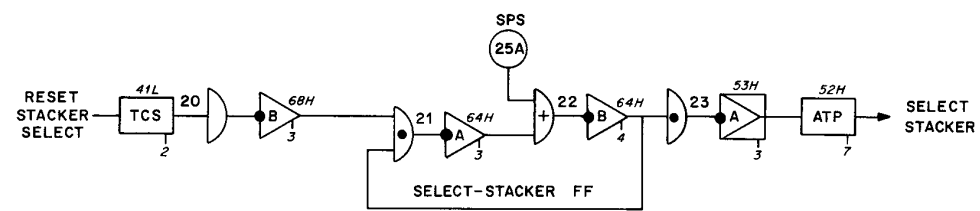
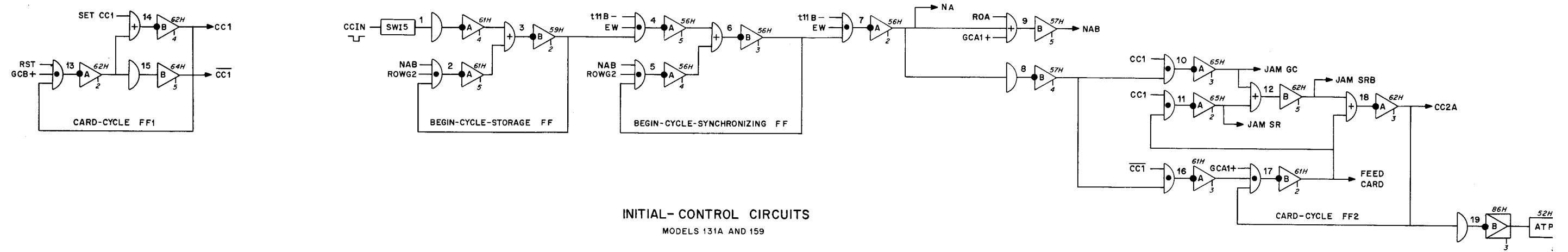
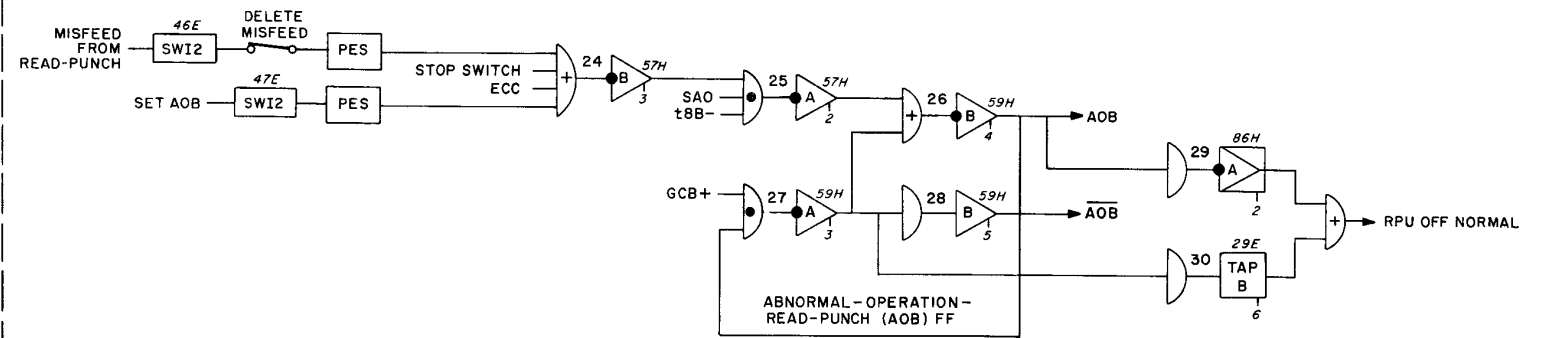


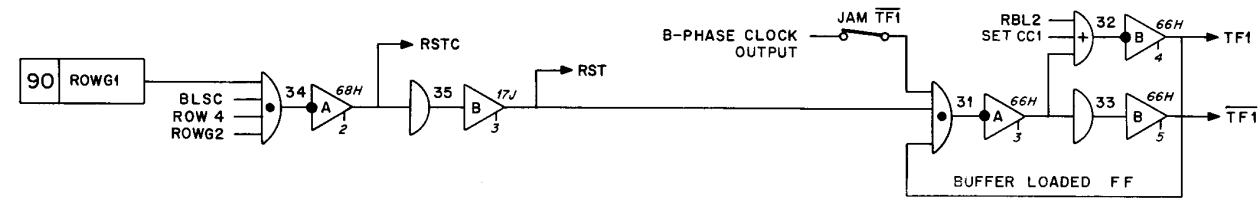
Figure 1-29B. Sense and Punch Logic, Part 2, Models 131A, 139, 159, and 184



MODELS 131A AND 159



MODELS 131A AND 159



END-CARD-CYCLE CIRCUIT
MODELS 131A AND 159

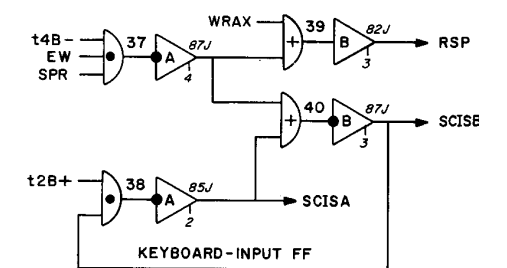
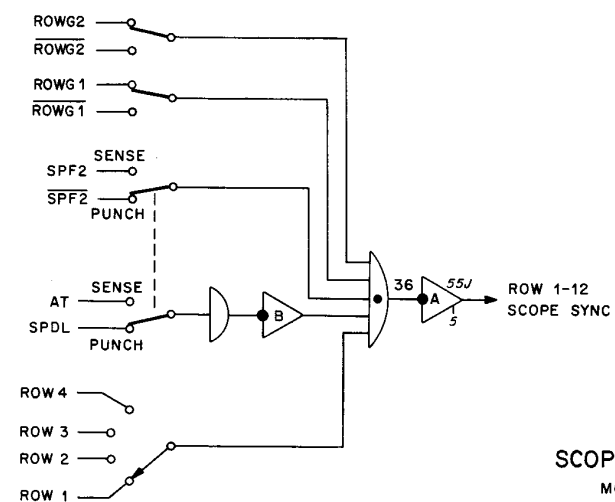


Figure 1-30B. Sense and Punch Logic, Par

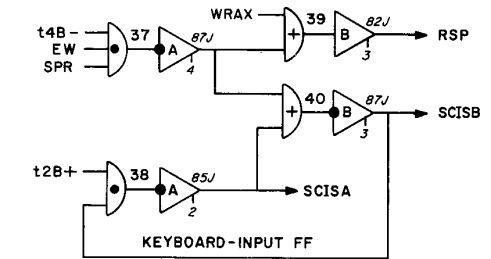
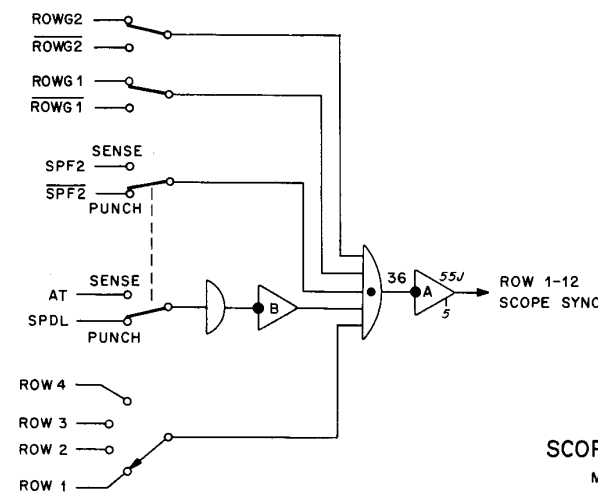
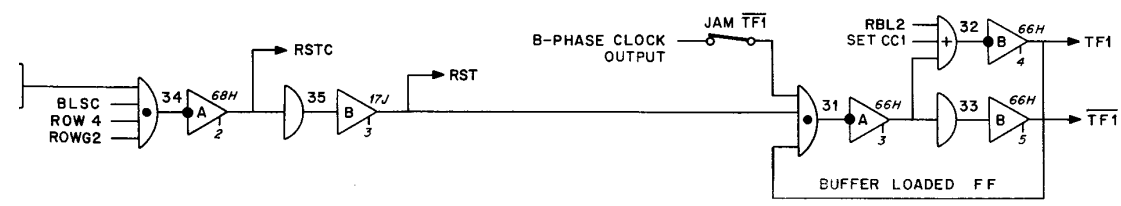
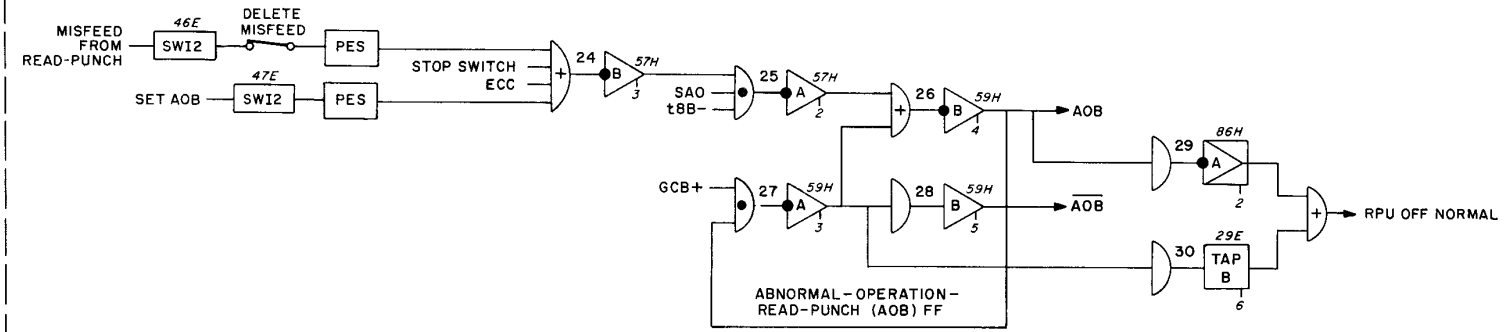
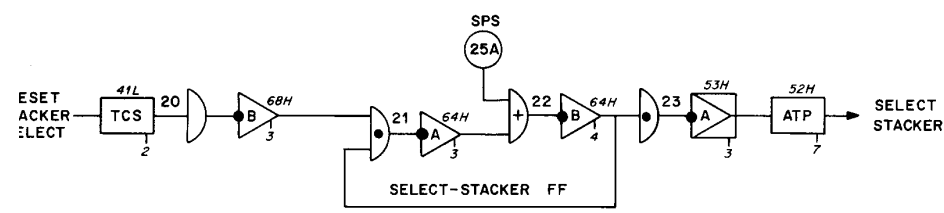
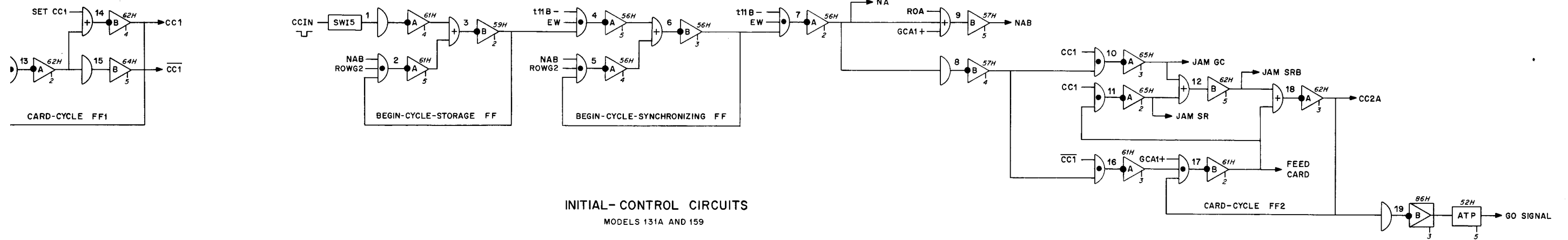
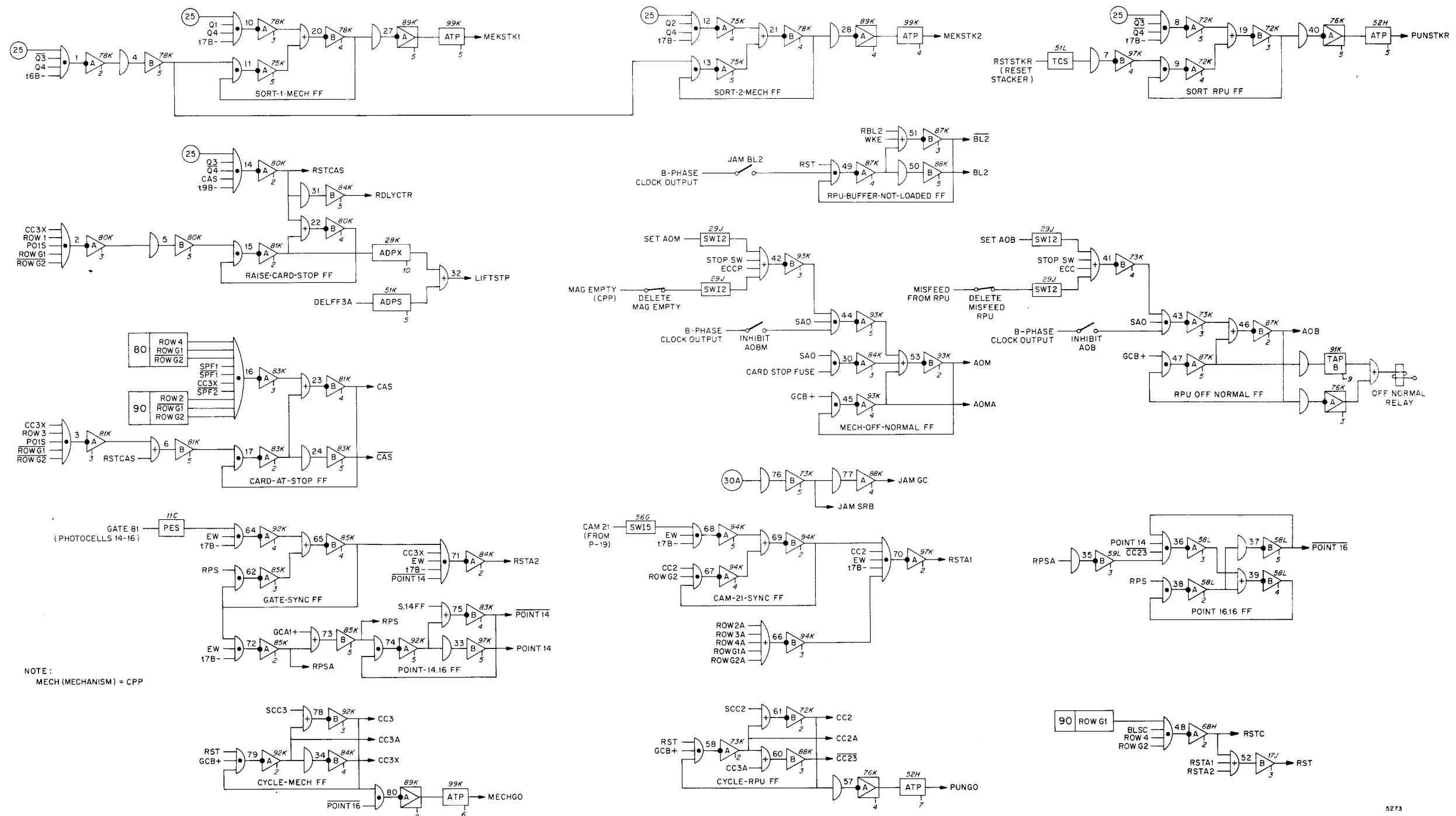


Figure 1-30B. Sense and Punch Logic, Part 3, Model 139

Basic System, All Processor Models



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Figure 1-30B. Sense and Punch Logic, Part 3, Model 139

Basic System, All Processor Models

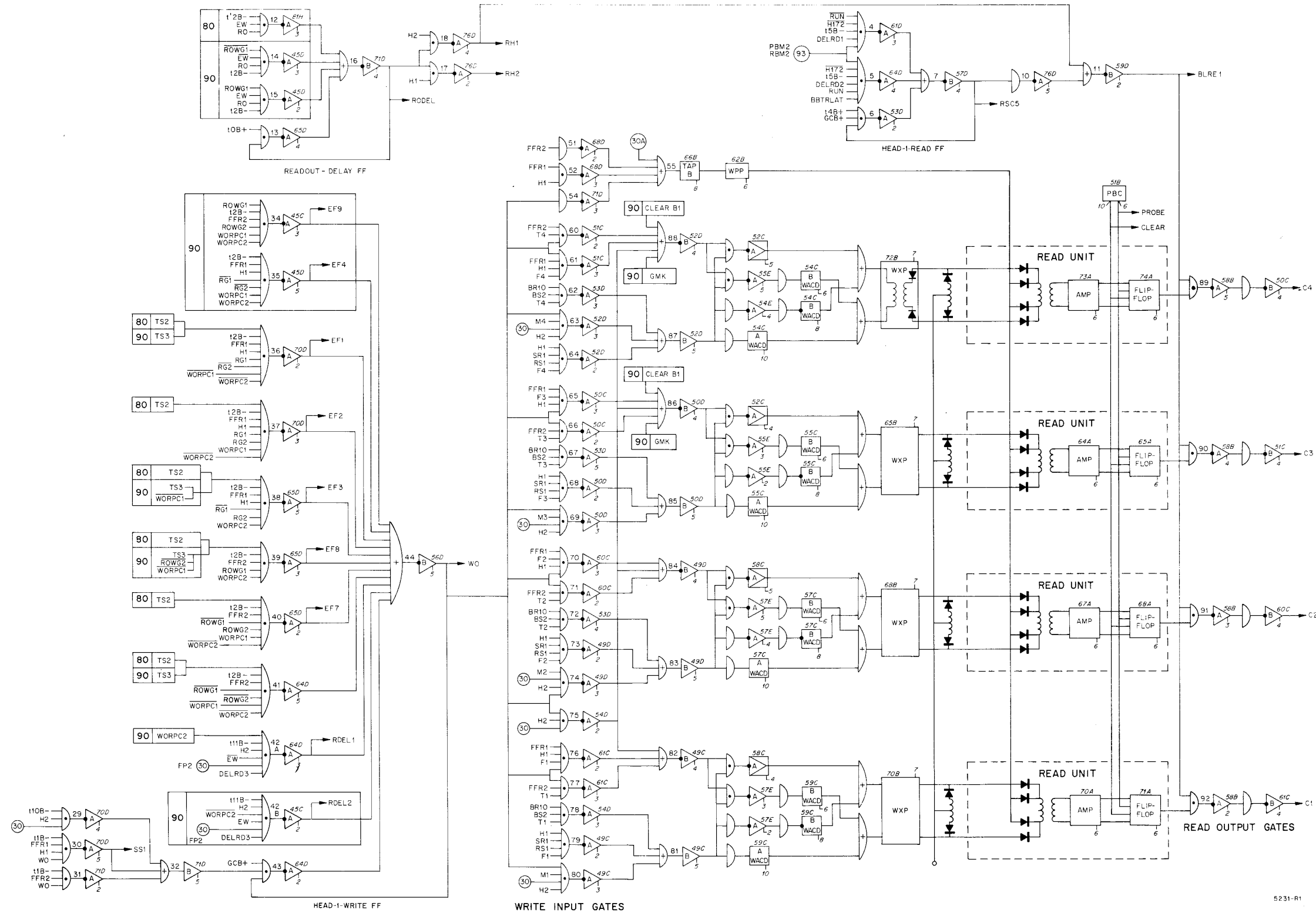


Figure 1-31B. Card-Buffer Head 1, Models 131A, 139, 159, and 184

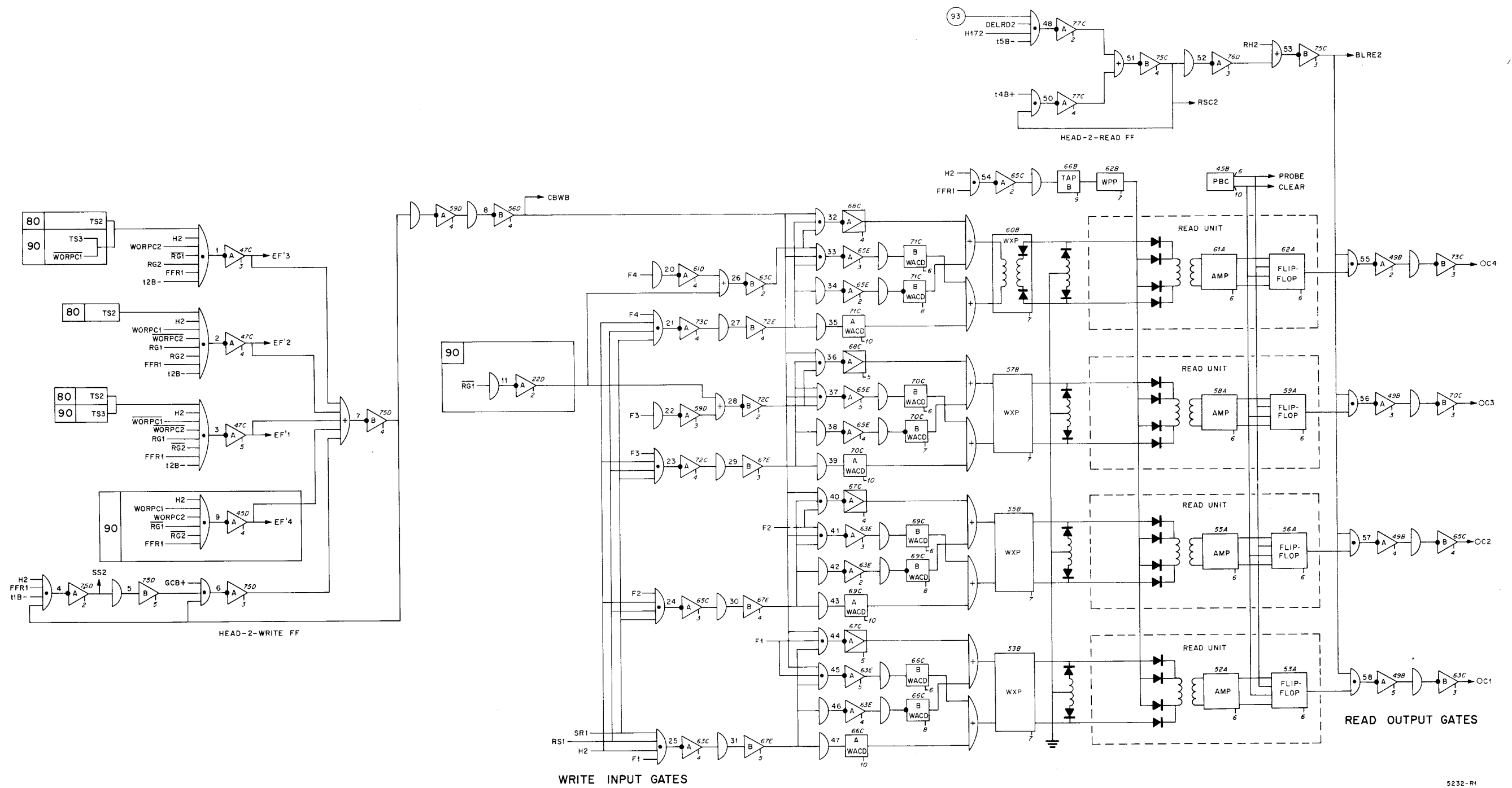
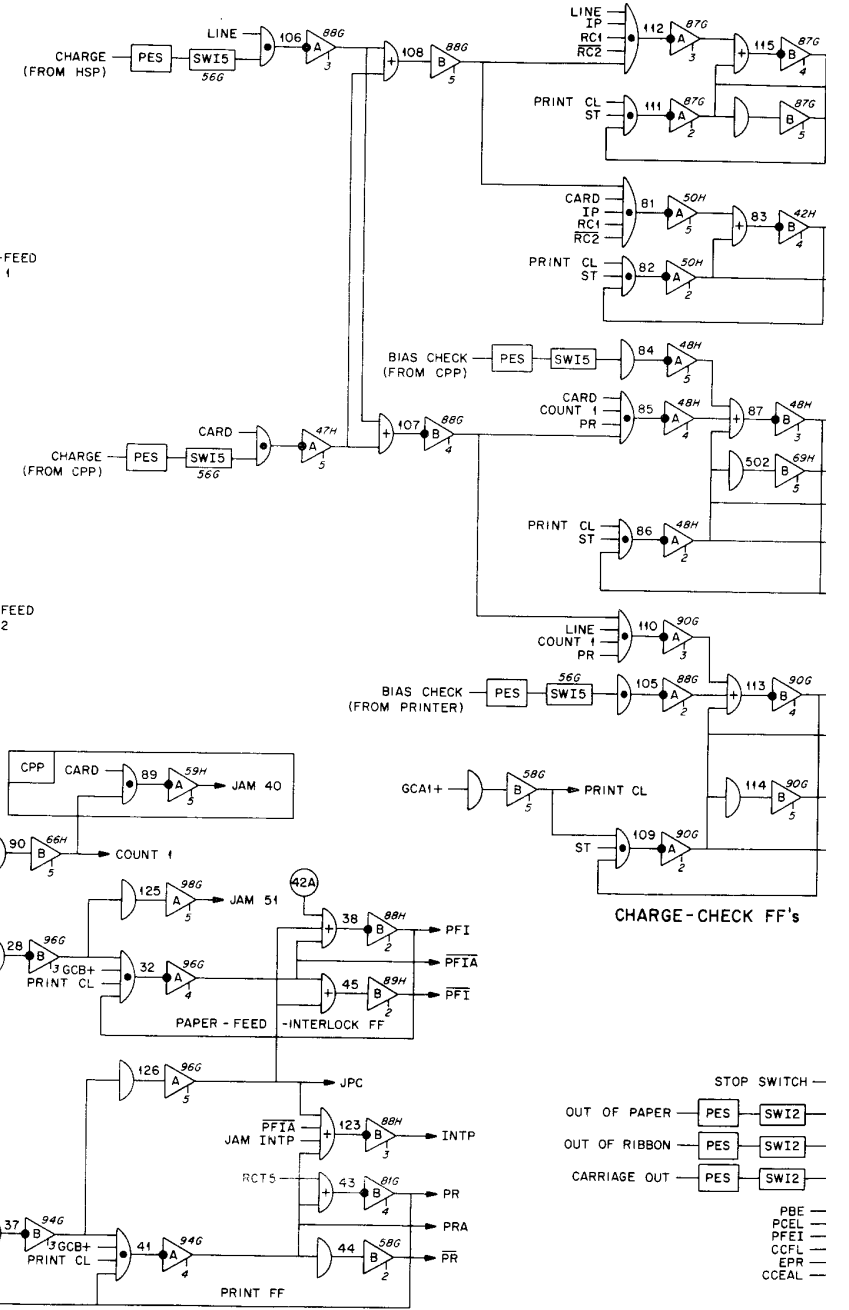
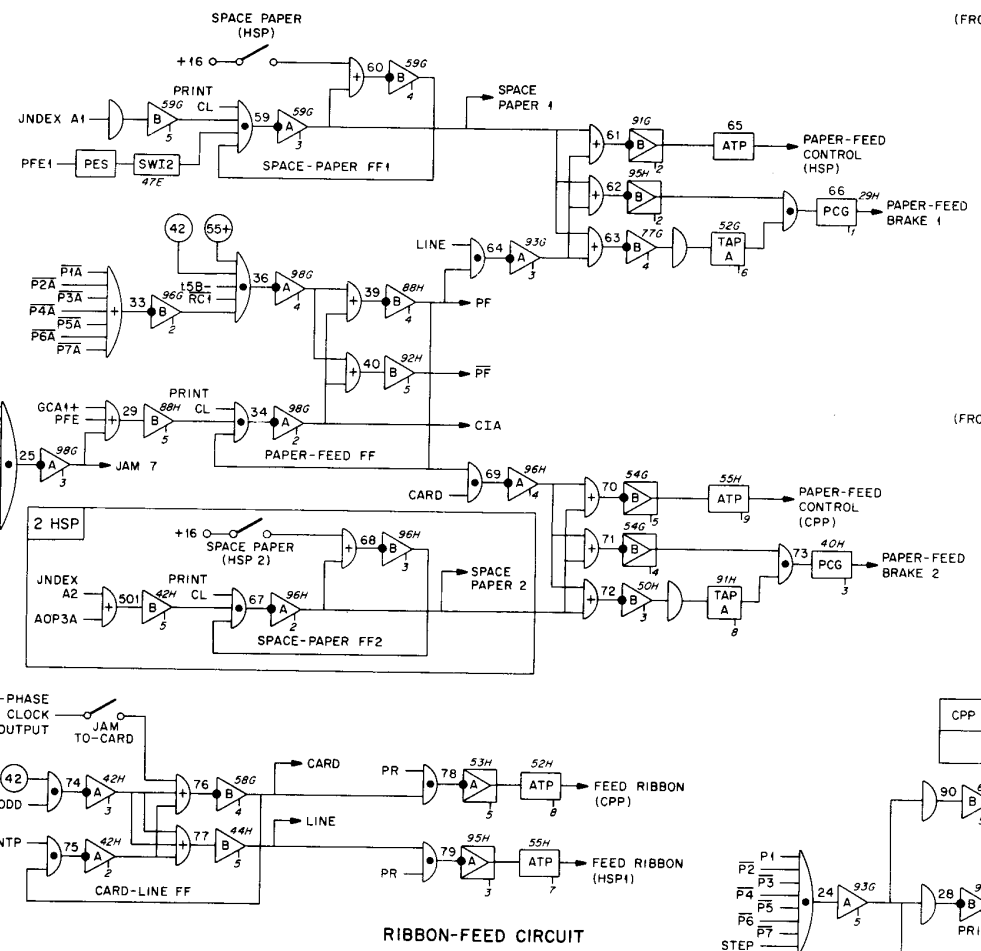
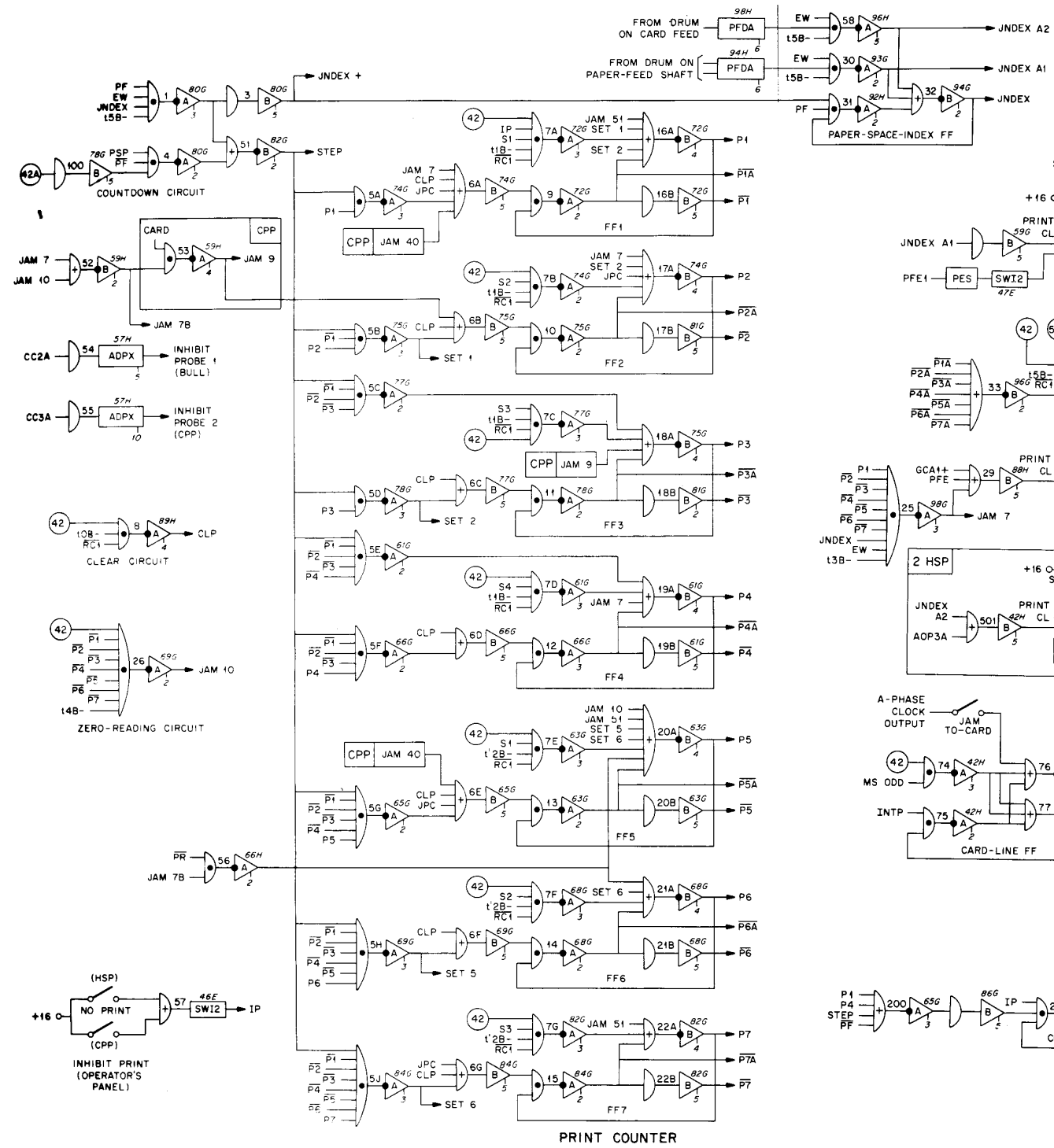


Figure 1-32B. Card-Buffer Head 2, Models 131A, 139, 159, and 184

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JNDEX A2

JNDEX A1

JNDEX

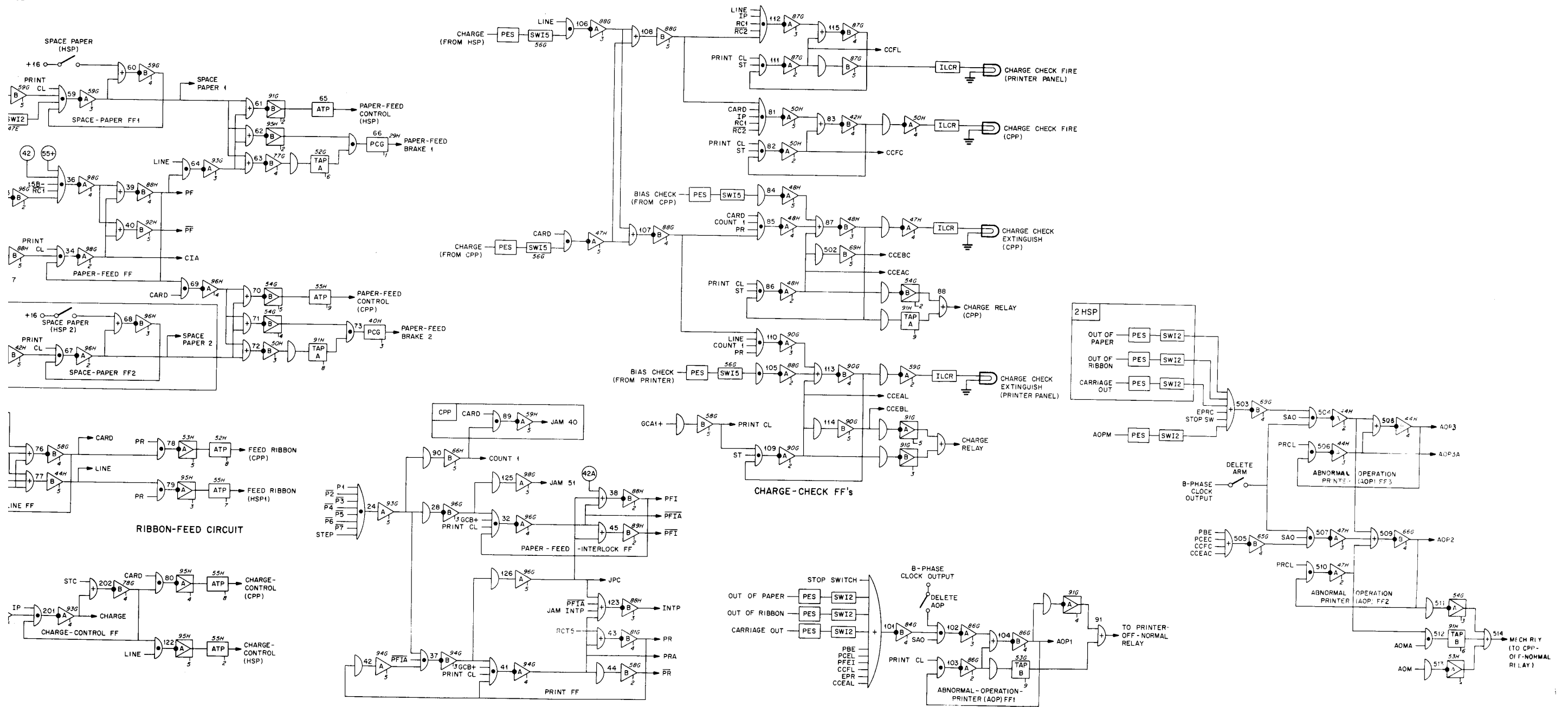
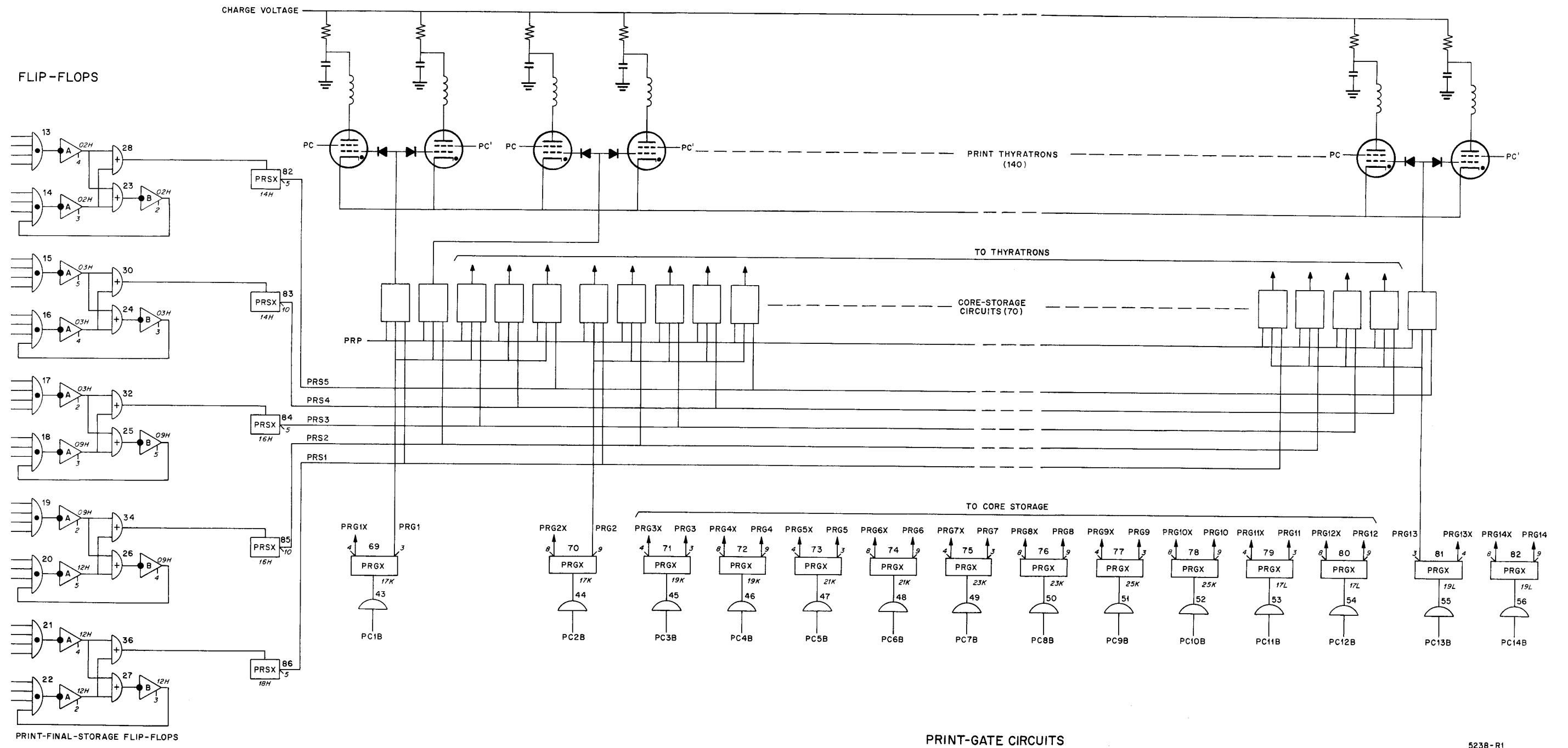


Figure 1-37B. Print Control, Model 139



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Figure 1-38B. Print Distributor, Model 139

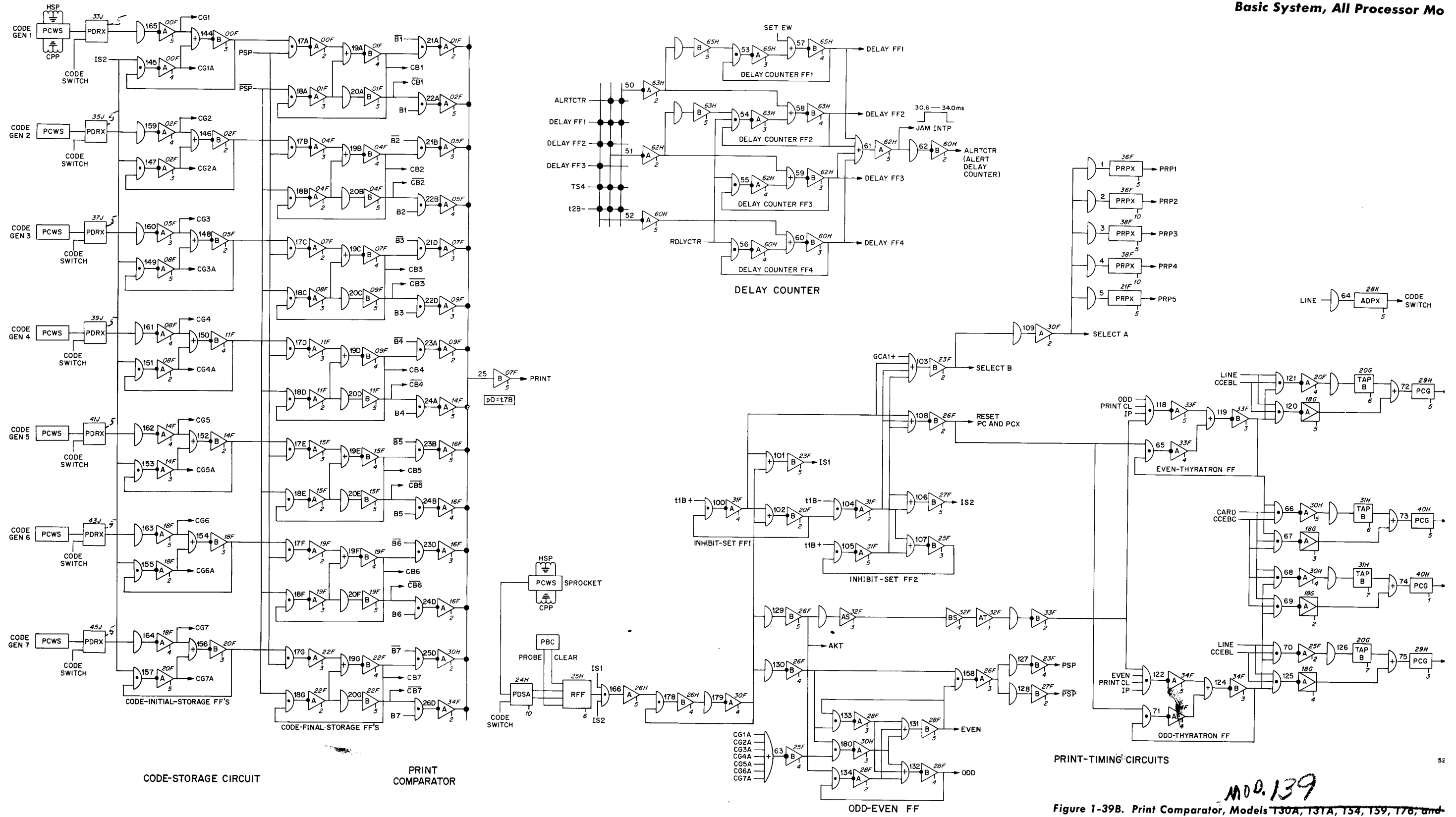
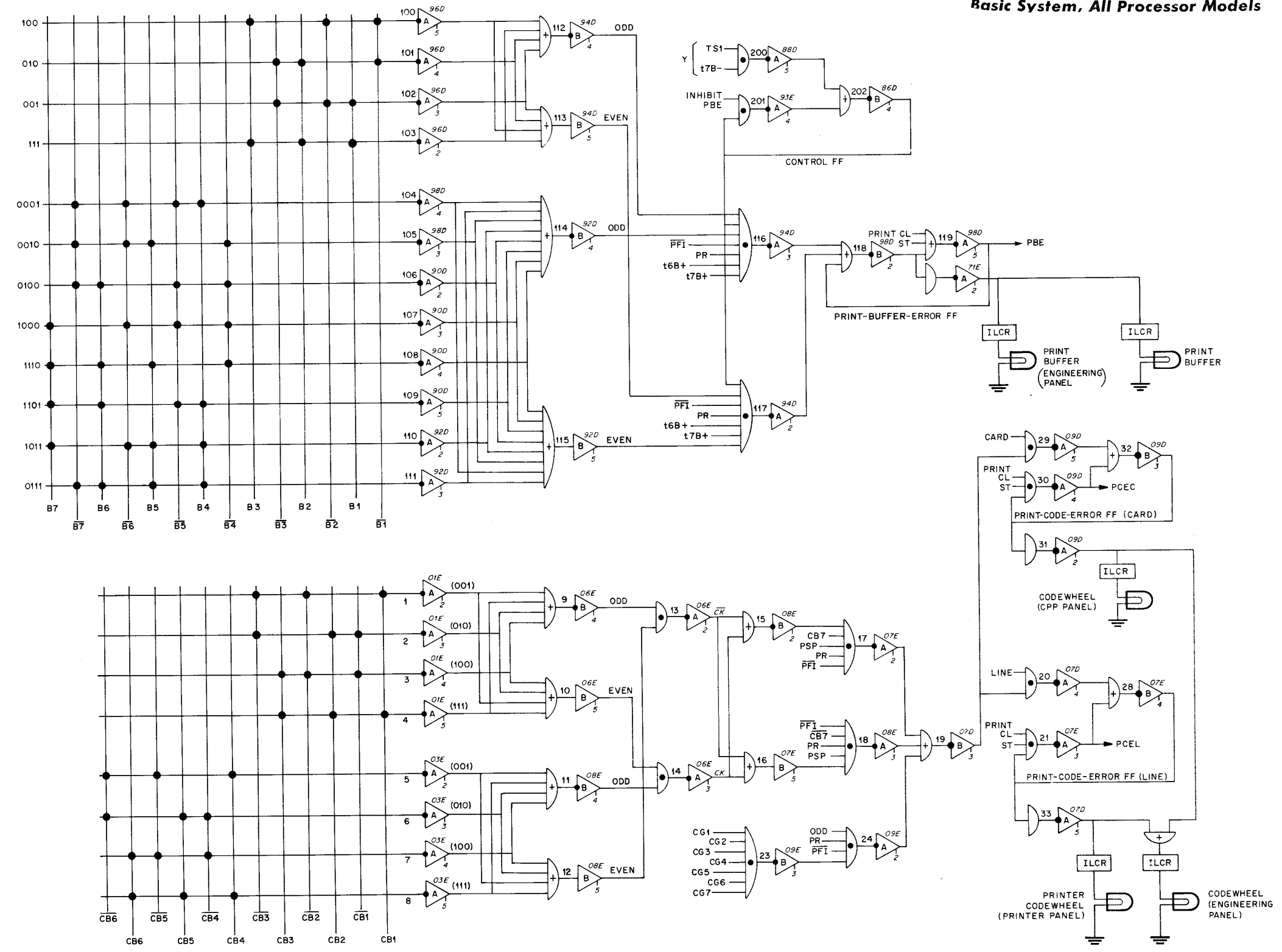


Figure 1-39B. Print Comparator, Models T30A, T31A, T54, T59, T76, and

MOD. 139

Basic System, All Processor Models



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Figure 1-40B. Print-Code and Print-Buffer Error Flip-Flops, Model 139