Copy No. 109

UNIVAC
Solid-State
COMPUTER

TYPE 7900 CENTRAL PROCESSOR 90
INPUT OUTPUT UNITS
Service Manual No. 3

COMPANY CONFIDENTIAL

REGISTERED CIRCULATION

Remington Rand Univac
DIVISION OF SPERRY RAND CORPORATION

NOTES

This manual should be read in conjunction with certain drawings under separate cover, listed on the next page. Throughout the manual, the symbol O designates the letter as distinguished from zero.

Suggestions for revision or correction of this manual should be forwarded to the Publications Engineering Group, Remington Rand Univac, Division of Sperry Rand Corporation, Post Office Box 5616, Philadelphia 29, Pa.

LIST OF DRAWINGS UNDER SEPARATE COVER

The following is a list of the logical drawings in Manual No. 2, appendix A of the central processor manual, and the equivalent engineering drawings. The engineering drawings forwarded with the system are the latest, correct drawings. Any differences between the logical drawings and the engineering drawings should be resolved in favor of the latter.

Appendix Figure	Title	Engineering Drawing
A-1	Register C	DX804 992
A-2	Static Register	DX805 001
A-3	Instruction Decoder	DX805 002
A-4	Function Encoder	DX805 003
A-5	Interrupted Operation	DX805 004
A-6	M Buffers	DX804 997
A-7	S Buffers	CX804 998
A-8	Register A	DX804 994
A-9	Register X	DX804 995
A-10	Register L	CX804 993
A-11	Quinary Adder	DX804 999
A-12	Comparator	DX805 000
A-13	Sign and Control Flip-Flops	DX804 991
A-14	Multiplier/Quotient Counter	CX804 996
A-15	IER-OR Flip-Flops	CX804 996
A-16	Cycling Unit	DX805 010
A-17	Timing-Band Read Circuits	CX805 009

Type 7901 High-Speed Printer

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I

INTRODUCTION

1-1. SCOPE OF THE MANUAL

This manual describes the type 7901 high-speed printer, one of the three input-output devices in the New Univac® system. The high-speed printer produces a single or multiple-copy record of computed or tabulated results under the control of the type 7900 central processor, to which it is directly connected. This manual describes the processor instructions that control the printer, as well as the circuitry that carries them out. The circuits that control the printer, located both in the processor and the printer, are known as the printer synchronizer. Since frequent reference is made to circuits within the central processor, the reader should be familiar with the information in Manual No. 1.

A physical description of the printer is presented in section II with functional descriptions of minor parts of the printer, the operations of which are not pertinent to an understanding of the theory of operation. The operations of the logical circuits and mechanical and electromechanical assemblies are described in section III as an introduction to detailed descriptions, also in section III, of the instructions that control the printer. Section IV describes the electronic circuitry.

1-2. GENERAL FUNCTIONAL DESCRIPTION

The high-speed printer prints computed or tabulated data from processor storage under the control of programmed instructions in the processor. A maximum of 130 alphanumeric characters can be printed on a line at a maximum rate of 600 lines per minute.

The printing mechanism contains 65 typewheels, each of which has two columns of type with 51 characters per column. One column on each of the 65 typewheels is designated as odd and the other column as even. As shown in figure 1-1, the columns of type are staggered, leaving four spaces around each character, so that only one character prints at a time. This prevents the act of printing one character from smudging on carbons or partially printing an adjacent character. The 51 characters in each column of type include the 26 alphabetic capitals, A through Z; the ten numerals, 0 through 9; and the following 15 symbols and punctuation marks:

- # $ % . , * ' + or @ ; : ( ) & /

A code wheel (figure 1-1) mounted on a common shaft with the typewheels contains the six-bit code combination for each of the 51 typewheel characters. The code combinations are

magnetically recorded on the surface of the code wheel. A parity check bit is stored on the code wheel with the six information bits.

A mode of printing is used known as "printing on the fly." Each type column on the typewheels is apposed by a solenoid-actuated print hammer, designed and positioned to drive a paper and inked ribbon against the typewheel at the required instant in a precise and rapid operation. A motor rotates the typewheel shaft continuously. As a character on the 65 type-wheels moves into print position, the code combination for that character is read from the code wheel and compared with 130 character combinations representing a line of output data read from a print buffer band on the processor drum. Each identity is stored to actuate the appropriate print hammer.

The 130 characters that can be printed on one line are divided into 13 ten-character words as shown in figure 1-2. The 13 words are initially stored in a main storage band on the processor drum. The band is specified in the m address of a print (11) instruction. Under the control of a print in-struction in the processor program the 13 words are read from the main storage section of the processor drum (figure 1-3) and are written on tracks of the drum that are reserved as print buffer storage. As the data is transferred to print buffer storage, the paper on the printer is advanced to the next line in preparation for printing. After the paper is advanced and the print buffer is loaded with output data, the code combination for the next character approaching print position is read from the code wheel into a comparator circuit in the printer synchronizer. There it is compared with each code combination in turn for the 130 characters of the words stored in the print buffer.

The printing cycle always begins with the printing of characters in the odd columns. Assuming that the character in print position is a U, all of the odd U's contained in the 13 words of output data are printed by comparing the digits of each of the 13 words with the code combination for a U read from the code wheel, and actuating the appropriate print hammers. Next, all of the even U's move into print position and, after another sequence of 130 comparisons, all of the even U's contained in the 13 words are printed. As the odd V's move into print position the code combination for V is read from the code wheel into the comparator circuit to replace the combination for U. The 130 characters of output data are compared, in turn, for identity with character combinations from the code wheel corresponding to successive character posi-tions on the typewheels. The comparison and printing process continues for one complete revolution of the typewheels to print a complete line, after which the print buffer may be loaded with new data and the paper advanced in preparation for printing the next line.

1-3. CHARACTERISTICS

The following list gives the mechanical and electrical characteristics of the high-speed printer:

Dimensions	
Width	32 in.
Length	72 1/4 in.
Height	52 1/2 in.
Weight	1613 lb
Lines per Minute	600
Characters per Line	130
Number of Characters	51
Paper Width	
Minimum	4 in.
Maximum	21 in.
Cooling	
Air current	550 cfm
Heat dissipated	198.5 BTU/min.
Room temperature at air intake	
Minimum	60°F
Maximum	100°F
Power Dissipation	3.5 kw

	Carriage Motor	Typewheel Motor
Voltage	115 v ac	115 v ac
Frequency	60 cps	60 cps
Phase	single	single
Horsepower	1/150 hp	1/6—1/18 hp
Current	0.4 amp	3.4—1.9 amp

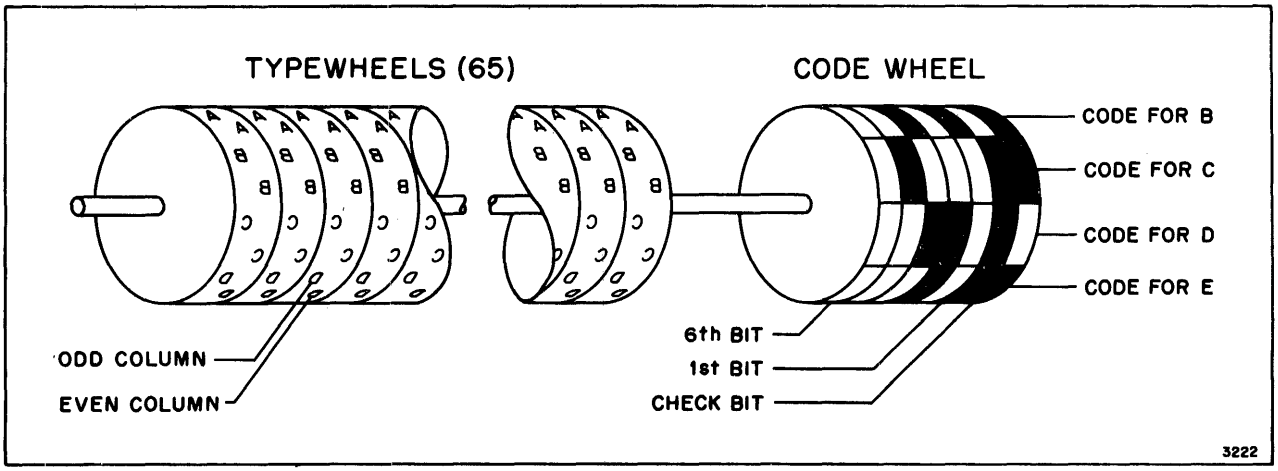


Figure 1-1. Typewheels and Code Wheel

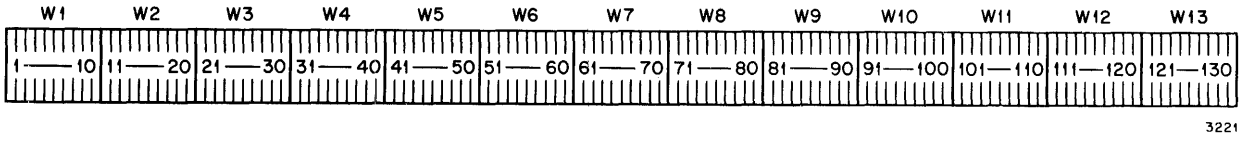


Figure 1-2. One Line of Print

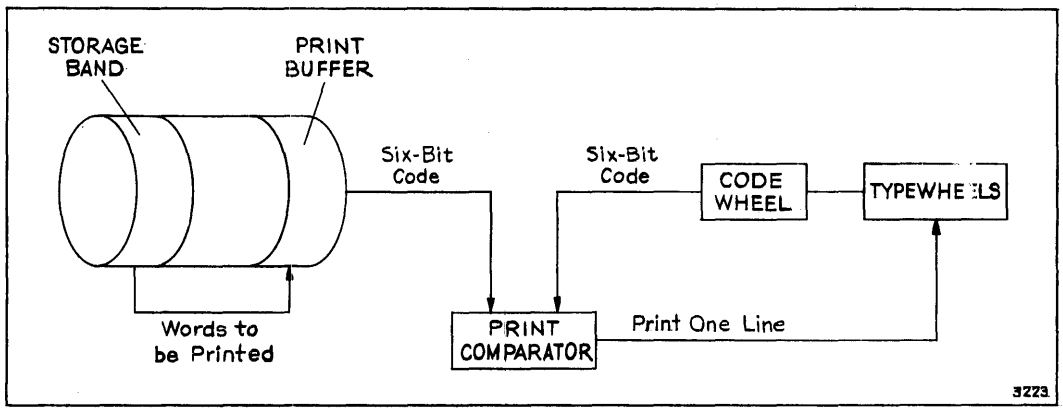


Figure 1-3. Print Instruction

SECTION II

PHYSICAL DESCRIPTION

2-1. SCOPE

This section contains the physical description and location of the components of the high-speed printer. All circuit packages used by the printer are located within the processor cabinet. Figures 2-1 and 2-2 show the location of the major components of the printer. To simplify the physical description, the printer is divided into two sections, the mechanical section and the power-supply section.

2-2. MECHANICAL SECTION

The mechanical section contains the printer mechanism and the ribbon-feed and paper-feed mechanisms. The mechanical section also houses the actuator capacitors (figure 2-2,2) and the actuator fuseboard.

2-3. PRINTER MECHANISM

2-4. TYPEWHEELS. Sixty-six typewheels (figure 2-3,2) are mounted on a shaft that is driven continuously by the typewheel motor (figure 2-4,5) and pulley belts. Only sixty-five typewheels are used for printing; one is a spare. The typewheel shaft is mounted on a movable carriage with the ribbon-feed mechanism. The carriage can be moved out by pressing the CARRIAGE OUT button on the control panel when a new ribbon is to be inserted.

Each typewheel contains two columns of type, each column consisting of 51 characters. The characters of the two columns, designated as odd and even columns, are staggered as shown in figure 1-1 to prevent smudging.

2-5. CODE WHEEL. The code wheel (figure 2-3,3) mounted on the typewheel shaft is a small magnetic drum containing eight tracks. The code for each of the 51 characters is magnetically recorded on the code wheel so that the code for each character is read from the drum as the character moves into print position. One hundred and two sprocket pulses are also recorded around the drum. They are used to synchronize the printing of the odd and even columns of the 51 typewheel characters. The eight tracks of the code wheel (six code-bit tracks, one check-bit track, and one sprocket track) are read continuously by eight read heads. The heads are mounted in two assemblies, each containing five heads. Two heads of one assembly are not used.

2-6. HAMMER AND ACTUATOR ASSEMBLIES. The printer mechanism employs 130 hammer and actuator assemblies (figure 2-4,4), one for each column of type. When the actuator coil is energized, an arm strikes the hammer, which pushes the paper and the ribbon against the typewheels. Section 3-25 describes the energizing of the coils and figure 3-2 illustrates hammer and actuator operation.

2-7. PAPER-FEED MECHANISM

The paper-feed mechanism consists of the clutch motor (figure 2-4,1), a magnetic clutch and brake (figure 2-4,2) and two tractor assemblies (figure 2-1,7), which hold and position the paper. The motor runs continuously whether the tractor shaft is engaged by the clutch or by the brake. When a signal is generated by a processor instruction, the clutch coil is energized and the brake coil deenergized. The brake is then released and the clutch engages the motor shaft.

The clutch shaft is connected to the tractor shaft by a belt so that as the clutch shaft rotates, the tractor shaft rotates. The pins of the tractor chain advance paper by engaging the perforations along each edge of the paper. Clamps on the tractor assemblies hold the paper in place against the tractor chains. The tractor assemblies can be positioned manually to accommodate various paper widths.

A paper-space index drum is mounted on the clutch shaft. Six magnetized areas are recorded around the drum at 60-degree intervals, and are read continuously by a head during paper feeding. During one revolution of the clutch shaft, six lines of paper are advanced and six signals are generated from the index drum, each signal indicating one line of paper advanced.

When the printer is out of paper, the no-paper switch closes, causing the printer to stop and lighting the NO PAPER and OFF NORMAL lamps on the printer control panel.

2-8. RIBBON-FEED MECHANISM

The ribbon-feed mechanism (figure 2-3) consists of a torque motor, knurled drive shaft, and supply and takeup mandrels. The torque motor holds the takeup spool of ribbon tightly against the drive shaft by means of a chain and gear assembly. The drive shaft is connected to the typewheel shaft by a series of gears and a solenoid-actuated pressure roller. When a print or paper-feed instruction is given, the solenoid is actuated to hold the pressure roller against the continuously rotating typewheel shaft, causing the ribbon to be advanced. The ribbon moves in one direction only. When it is completely wound on the takeup mandrel, it must be removed and rethreaded. When the ribbon is completely wound on the takeup mandrel, or if it is ripped or worn through, a switch closes, causing the printer to stop and lighting the NO RIBBON and OFF NORMAL indicators on the printer control panel.

2-9. POWER-SUPPLY SECTION

2-10. POWER-SUPPLY TRAY A

Tray A (figure 2-5) of the printer power-supply section contains components for the actuator-capacitor charge circuits and the print-thyratron circuits. Tubes V3 and V4 are part of the charge circuits for the actuator capacitors.

Twenty capacitors (C1 through C10 and C1A through C10A) constitute an actuator-capacitor reservoir which maintains d-c voltage while the actuator capacitors are charging. Transformer BT-178, the V1 and V2 tubes, and the printer density switch (figure 2-6,1) control the momentun of the hammers. To increase or decrease momentum, the potential developed across the actuator capacitors is altered by the adjustment of the switch. When many carbons are to be printed, the momentum is increased to make certain that printing is distinct. Capacitors C12, C13, C14 and transformer BC81 are part of the actuator-charge circuits. Transformers BT-198 and BT-94 supply voltages to various tubes in the power-supply section. Relays 4 and 4A are in the actuator-charge circuit. Relay 4 prevents extraneous printing by opening when power is disconnected from the printer, and allows the actuator capacitors to discharge slowly. Relay 4 also disconnects the charge thyratron when it does not extinguish correctly.

2-11. POWER-SUPPLY TRAY B

Tray B (figure 2-6) of the printer power-supply section contains components for the paper-feed circuits, actuator-capacitor charge circuits, and power-control circuits.

Five resistors (R1, R2, R3, R4 and R7), three capacitors (C16, C17 and C20), and relay 11 are part of the paper-feed circuitry. Relay 11 is the paper-feed error reset relay. Two resistors (R5 and R6), seven capacitors (C15, C18, C19, and four capacitors mounted on TB2), and the swinging choke BC69A are part of the actuator-capacitor charge circuits. Transformer BC69A is an input choke for the high-voltage supply to the actuator-capaciter charge circuits.

Transformer T-1 is part of the +117-volt d-c supply circuit. The contactor, relay 14, applies voltage to the printer motors when the MOTORS switch on the control panel is energized.

2-12. RELAY PANEL 2

Relay panel 2 (figure 2-6) contains components for the printer control circuits. The rectifier and filter capacitor are part of the +117-volt d-c supply circuit. Relays 8, 9, and 10 are the ribbon-feed, out-of-paper, and out-of-ribbon relays. Mounting board 12 contains miscellaneous power-control-circuit components.

2-13. RELAY PANEL 3

Relay panel 3 contains components for the printer control circuits.

Relays 5 and 6, (figure 2-4,7) are the carriage-in and carriage-out relays. Relay 5 controls only the carriage-in a-c circuits. Capacitors C21 and C22 are starting condensers for the clutch and carriage motors.

2-14. P1E CHASSIS

The P1E chassis (figure 2-2,7) contains components for the print, paper-feed, and charge circuits. The layout of the chassis is shown in engineering drawing DX601 083. The tube positions are numbered 1 through 10 from top to bottom.

Tubes V6 through V9 and four transformers (MT28-1, MT28-2, MT60-1 and MT60-2) are used in the print circuits. Tubes V1, V2, V4, transformer MT29-2, and the 80-mh choke are used in the paper-feed circuits. Tube V5 and transformer MT29-1 are used in the actuator-capacitor charge circuits.

2-15. P2E CHASSIS

The P2E chassis (figure 2-2,8) contains components for charge and paper-feed circuits. The layout of the chassis is shown in engineering drawing DX601 082. The tube positions are numbered 1 through 14 from top to bottom.

Tubes V10, V11, V12, and V13 are part of the paper-feed circuitry and tube V8 is part of the actuator-capacitor charge circuits. Relay 1 is the carriage-in relay and controls d-c circuits only. Relay 2 is the paper-feed error relay and relay 3 is part of the charge circuits.

2-16. P3E CHASSIS

Each of the 13 P3E chasses (figure 2-2,6) contains ten print-thyratron tubes and five magnetic cores. The magnetic cores store the set signals until sampling occurs, at which time the set signals trigger the print thyratrons. A total of 130 print thyratrons and 65 magnetic cores is mounted on the group of P3E chasses. The layout of the P3E chassis is shown in engineering drawing DX601 085.

2-17. CONTROL PANEL

The printer control panel (figure 2-7) contains the controls and indicators necessary to control the printer manually and to indicate abnormal conditions within the printer. Table 2-1 shows the function of each control and indicator.

Table 2-1. Control Panel Controls and Indicators

a. CONTROLS: Eight illuminated pushbuttons

Panel Marking	Function	Indication
CARRIAGE IN*	Pressed and held: moves ribbon and typewheel carriage in.	Lights green jewel-light when carriage fully in.
CARRIAGE OUT*	Pressed and held: moves ribbon and typewheel carriage out.	Lights amber jewel-light when carriage fully out.
CHANGE RIBBON**	Pressed: enables ribbon to wind completely past the normal reversing position onto the takeup shaft.	Lights while jewel-light when operated.
SPACE PAPER/ PAPER FEED CHECK*	Pressed and held: advances one line of paper.	Lights amber jewel-light to indicate paper-feed error.
CLEAR/SYSTEM OFF NORMAL*	Pressed and held: clears controls, indicators, and flip-flops.	Lights red jewel-light when any off-normal condition is present in the system.
COMPUTATION RUN*	Pressed: starts processing of instruction.	Lights green jewel-light when operated.
COMPUTATION STOP*	Pressed: stops processing of instruction.	Lights amber jewel-light when operated.
MOTORS**	Pressed: starts or stops all printer motors except the ribbon-feed motor.	Lights green jewel-light when operated.

* springloaded

**alternate action

Table 2-1. Control Panel Controls and Indicators (cont)

b. INDICATORS: Seven jewel-lights

Panel Marking	Function	Indication
CHARGE CHECK FIRE	Lights when charge thyratron is not fired on time.	Lights red.
CHARGE CHECK EXTINGUISH	Lights when charge thyratron is not extinguished on time.	Lights red.
NO RIBBON	Lights when printer is out of ribbon or when ribbon is ripped.	Lights amber.
NO PAPER	Lights when printer is out of paper or when paper is ripped.	Lights amber.
CODE WHEEL	Lights when check-bit error occurs while reading from the printer code wheel.	Lights red.
AIR FLOW	Lights when air flow falls below required rate.	Lights red.
OVERHEAT	Lights when temperature of air circulating within printer is above required limit.	Lights red.

2-18. MISCELLANEOUS COMPONENTS

2-19. FUSEBOARDS

There are three fuseboards on the printer. Fuseboards 1 and 2, on the right end of the printer, contain fuses for all of the circuits contained in the printer except the actuator circuits. The third fuseboard, on the left end of the printer, contains fuses for the actuator circuits.

2-20. CONNECTORS

The printer is connected to the processor by two connectors, CPC and CP52 (figure 2-2,3 and 4). Connector plug C (CPC) carries signals to and from the packages in the processor bays. Connector plug 52 (CP52) carries power from the processor to the printer.

2-21. BLOWER

A blower system is used to circulate air through the printer. The blower (figure 2-1,5) draws external air into the printer and blows it into an air duct (figure 2-2,5). If the rate of air flow falls below the required minimum, an air-vane switch closes, causing the printer to stop. If the air temperature rises above the required limit, a thermostat causes the printer to stop. Either condition, overheat or low rate of flow, causes an indicator to light on the printer control panel, and removes both ac and dc from all of the computer circuits except the drum and blower circuits.

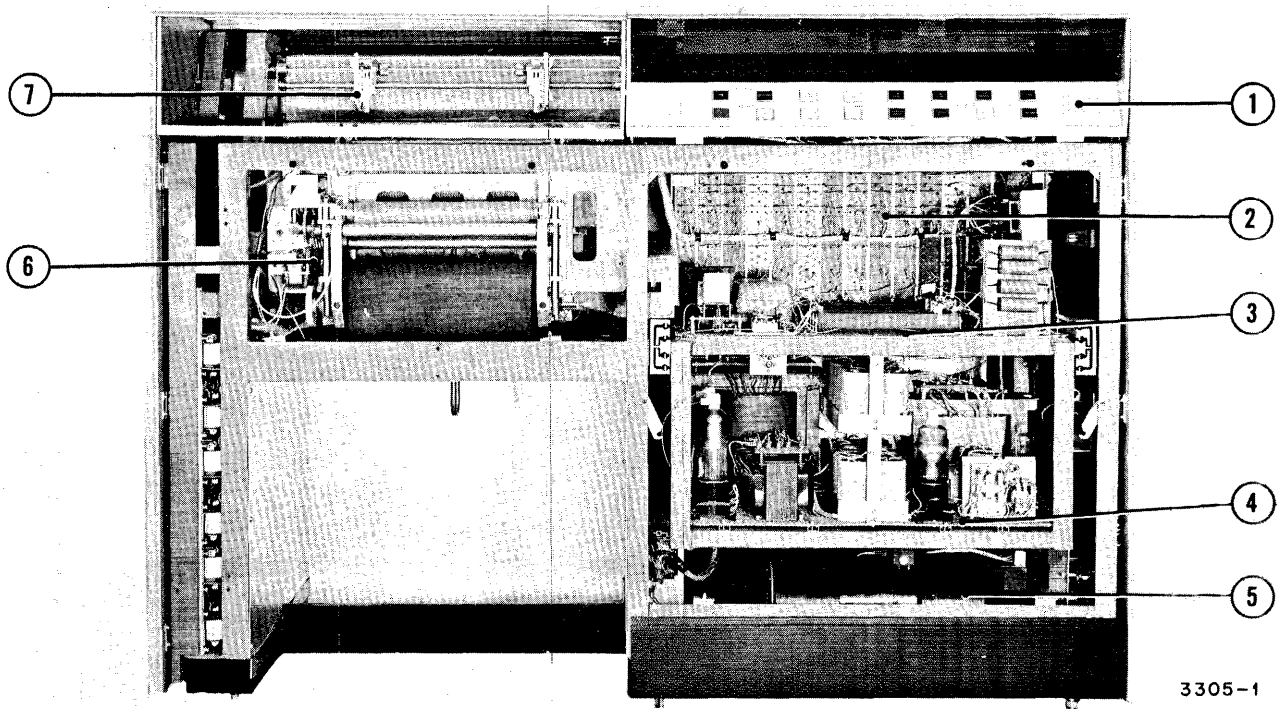


Figure 2-1. Type 7901 High-Speed Printer, Front View

KEY

1. Control panel
2. Chassis backboard
3. Power-supply tray B
4. Power-supply tray A
5. Blower and blower motor
6. Ribbon-feed mechanism
7. Tractor assembly

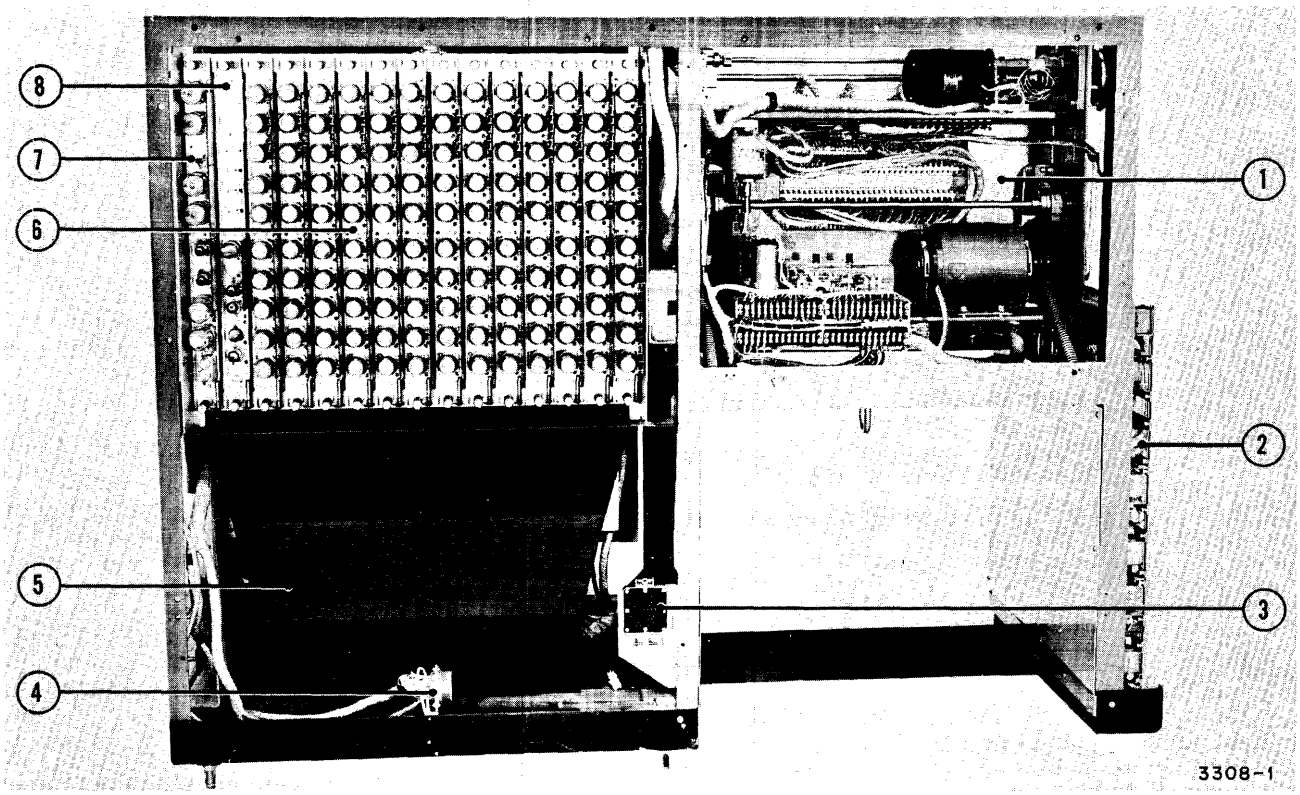


Figure 2-2. Type 7901 High-Speed Printer, Rear View

KEY

1. Printer mechanism (refer to figure 2-4)
2. Actuator capacitors
3. Connector plug C
4. Connector plug 52
5. Air duct
6. P3E chasses (one of thirteen)
7. P1E chassis
8. P2E chassis

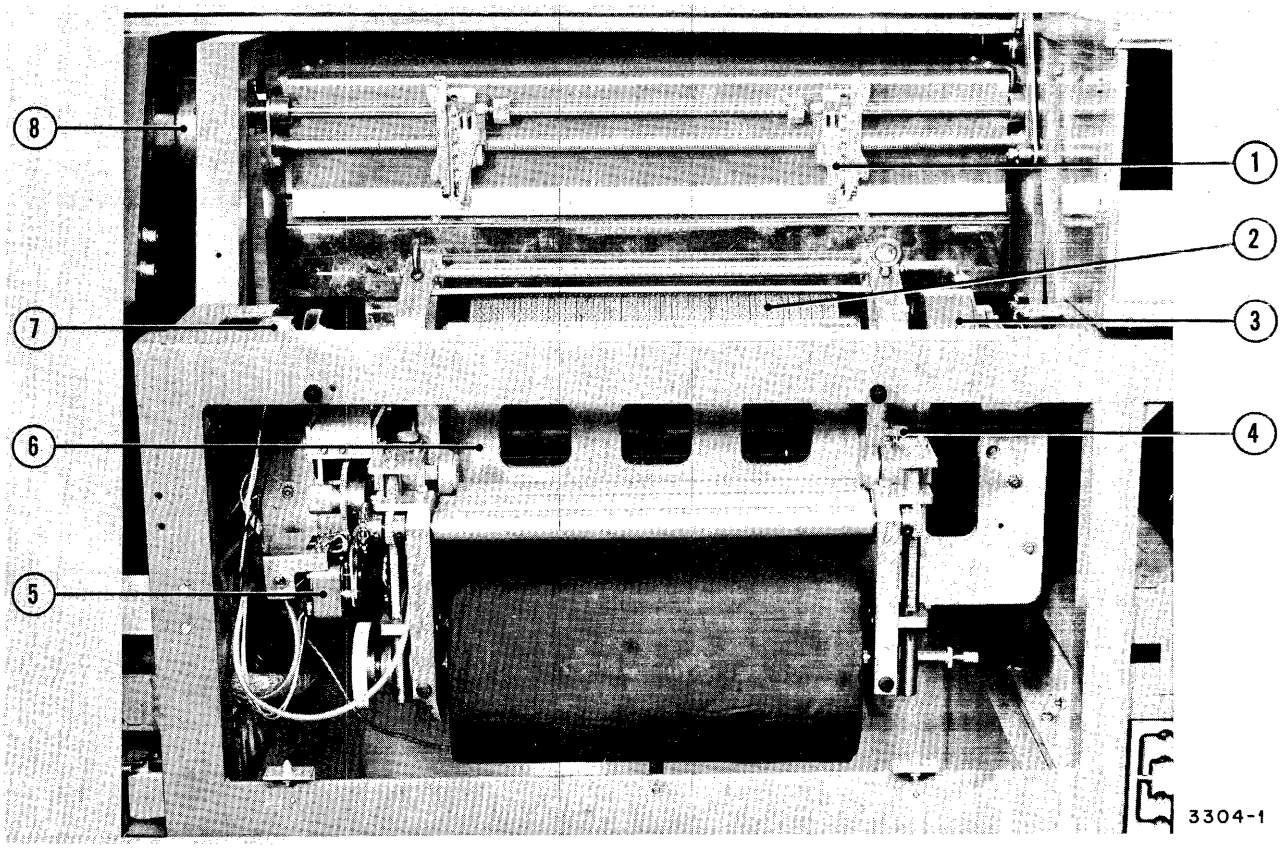


Figure 2-3. Ribbon-Feed and Print Mechanism, Front View

KEY

1. Tractor assembly
2. Typewheels
3. Code wheel
4. Takeup mandrel adjustment
5. Torque motor
6. Ribbon carriage
7. Carriage-stop adjustment
8. Paper-space index drum

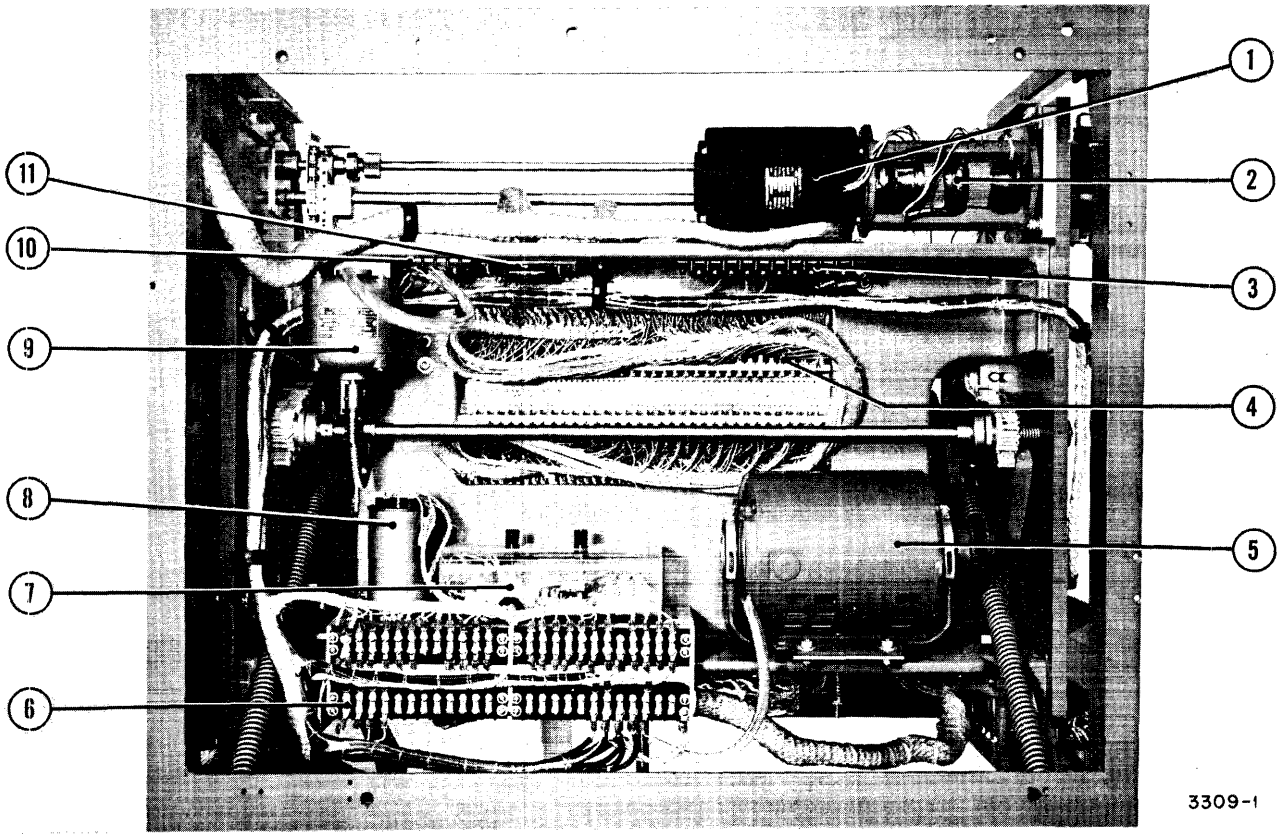
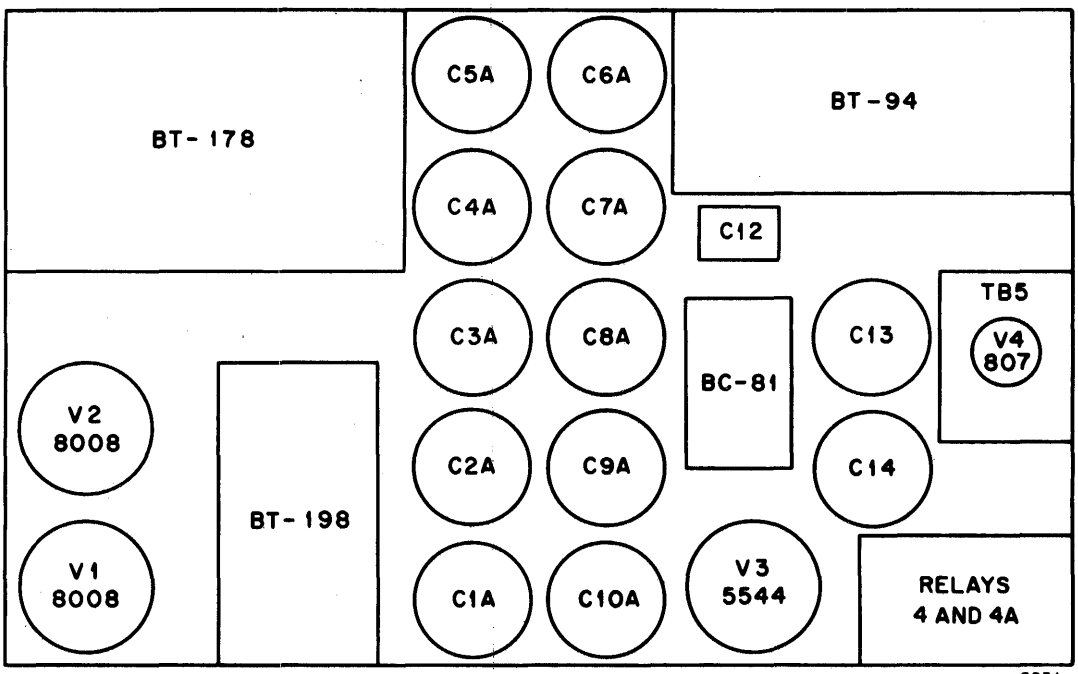


Figure 2-4. Printer Mechanism, Rear View

KEY

1. Clutch motor
2. Magnetic clutch and brake
3. Barrier strip JTM
4. Actuator assemblies
5. Typewheel motor
6. Barrier strip JTL
7. Relays 5 and 6
8. Capacitor C22
   (C21 hidden behind C22)
9. Carriage motor
10. Barrier strip JTM
11. Terminal board 6



NOTE: CAPACITORS C1 THROUGH C10 ARE MOUNTED DIRECTLY BELOW CAPACITORS C1A THROUGH C10A

Figure 2-5. Power-Supply Tray A

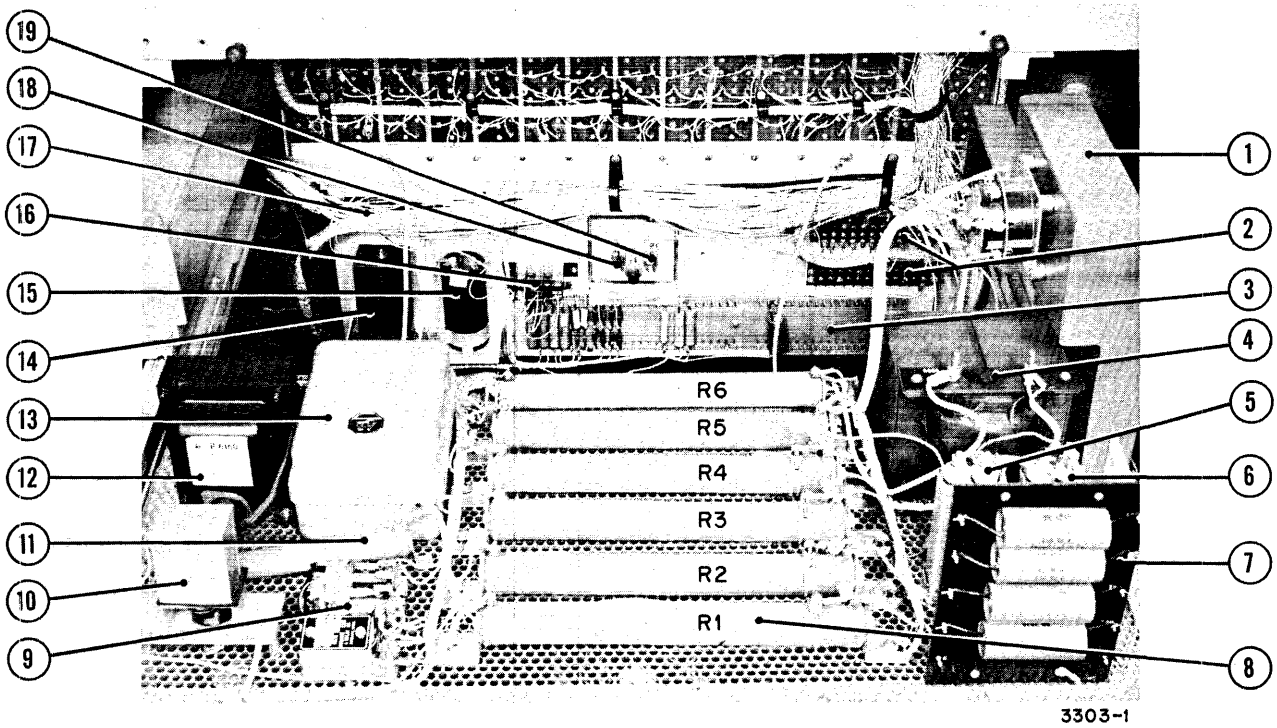


Figure 2-6. Power-Supply Tray B and Relay Panel 2

KEY

1. Printer density switch
2. Barrier strip JTH
3. Mounting board 12
4. Transformer BC69A
5. C16
6. C17
7. Terminal board 2
8. Resistors R1 to R6
9. Relay 13
10. Relay 11
11. R7
12. Auto transformer T-1
13. Contactor
14. Relay 8
15. Capacitor
16. Rectifier
17. Barrier strip JTS
18. Relay 9
19. Relay 10

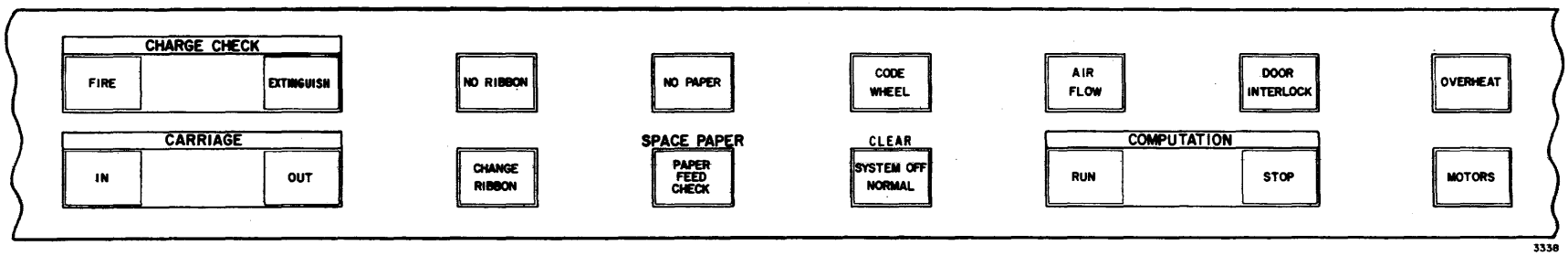


Figure 2-7. Printer Control Panel

SECTION III

THEORY OF OPERATION

3-1. SCOPE

This section is divided into two major parts. The first part includes detailed descriptions of the mechanical and electromechanical components and of each of the logical circuits controlling the printer. In the second part, the instructions which control the normal printing operations are described, assuming a working knowledge of the components. The second part also describes the abnormal conditions which can affect printer operations and the control of these conditions.

3-2. GENERAL DESCRIPTION

The operation of the printer is controlled by two instructions, 11 and 16.

The 11 instruction is as follows: Transfer the print words from the band specified by the p7 and p8 digits of the m address to the print buffer. Advance the paper the number of lines (up to 79) specified by the p5 and p6 digits of the m address. Upon completion of the transfer, clear the 11 instruction from the static register; upon completion of the paper advance, print one line under control of the printer synchronizer.

The 16 instruction is as follows: Advance the paper the number of lines (up to 79) specified by the p5 and p6 digits of the m address.

When the typewheel and paper-feed motors of the printer are operating, the 65 typewheels and the code wheel rotate and the character codes read from the code wheel are stored for the comparison operation required during printing. Printing and paper feeding, however, begin only when an 11 instruction occurs in the program. The function of the 11 instruction is to advance the paper a specified number of lines and to print a line of information which has previously been stored in a main-storage band. The p5 and p6 digits of the m address of the 11 instruction specify the number of lines paper is to be advanced before printing. This number is stored in a counter in the synchronizer, the paper-feed brake is released and the paper-feed clutch is engaged to advance the paper the required number of lines. Each line of paper fed reduces by one the number stored in the counter. When the count in the counter is zero, paper feeding ends.

The p7 and p8 digits of the m address of the 11 instruction specify the number of the band in which the print words are stored. In the first step of an 11 instruction, a search is made for the specified band. If the printer is available and is operating normally, the static register is stepped to the second step when the band is located.

During the second step, which requires three drum revolutions, the print words are read from the storage band and written into the print buffer. Paper begins to advance during the second step. Each print word is stored in two locations of the band because the word is in the six-bit Remington Rand code and must be split into two parts for storage. Registers A and X in the processor are used as intermediate storage to hold the two parts of each of the 13 words read from the storage-band locations. First one part of a word is read from its location into register A. Then the second part of the same word is read from its location into register X. A new check bit is computed for each character of the word and stored in register X. When both parts have been stored in the registers, the entire word is written into the print buffer in three places. The two parts of the next word are then read from the storage locations into registers A and X and are written into the print buffer. When all 13 words have been written into the buffer, the 11 instruction is cleared from the static register and the synchronizing circuits are notified that the buffer is loaded with the print words.

On completion of paper advance, a count of 51 is set up in the same counter which held the number of lines to advance the paper, and the synchronizing circuits are notified that the paper has been completely advanced and that printing can begin. Printing begins with the character which is moving into print position at the completion of paper advance and continues until the typewheels have completed a full revolution and all 51 characters have moved into print position.

If, for example, the odd-column F's are moving into print position, the six-bit code for F is stored temporarily, and compared with the code for each of the characters in turn in the line to be printed. A print signal is generated for each F to be printed in an odd position on the line, and these print signals set corresponding magnetic cores. There are 65 cores for the 130 print positions on a line, each core controlling an odd and an even print position. All 65 cores are sampled at one time, and the cores which are set control the printing of F's in the appropriate odd positions. The setting and sampling of cores is controlled by a sprocket pulse read from the code wheel.

Next, the even-column F's move into print position and all characters of the stored words are again scanned. Each character is compared with the F code from the code wheel.

For character positions that yield an identity, print signals set the magnetic cores for printing. As the typewheels rotate, all 51 characters are printed, first in the odd and then in the even positions. Printing ends when the 51-character count has been reduced to zero.

3-3. REMINGTON RAND CARD CODE

Output information sent to the printer and characters read from the printer code wheel employ the six-bit Remington Rand card code. If a word to be printed is in the four-bit processor code, a translate instruction must be given to convert it into the six-bit code before it is stored for printing. (Refer to section V of the central processor manual for a description of the translate instructions.) The result of the translation is stored in registers A and X. The first part of the translated word, known as the unprimed word, consists of four bits of the six-bit code for each character. The unprimed word is stored in register A. The second part of the translated word, known as the primed word, consists of the remaining two bits of the code for each character, and is stored in register X. The unprimed part is designated the W word, and the primed part the W' word, as W2, W'2.

The two parts of each translated word are transferred by 60 and 65 instructions from register A and register X to two locations of a main-storage band specified in the instruction word. Check bits are computed and stored with each of the two parts of the word. The specified storage locations for both parts of the 13 words to be printed on a line are shown in table 3-1. Note that the primed part is stored five locations after the unprimed part.

Table 3-1. Main-Storage Locations for Print Words

Print Word		Main-Storage Location	Print Word		Main-Storage Location
Unprimed Part	Primed Part		Unprimed Part	Primed Part	
W1		000	W8		041
	W'1	005		W'8	046
W2		081	W9		125
	W'2	086		W'9	130
W3		165	W10		009
	W'3	170		W'10	014
W4		050	W11		094
	W'4	055		W'11	099
W5		134	W12		178
	W'5	139		W'12	183
W6		018	W13		062
	W'6	023		W'13	067
W7		103			
	W'7	108			

Figure 3-1 shows the two parts of the card-coded word 7432159675, which are stored in locations 000 and 005 of the selected band. The numbers 0, 1, 3, 5, 7 and 9 to the left of the figure indicate the odd bit positions of a Remington Rand coded digit. A 1 bit in the appropriate bit position designates an odd digit. An even digit, such as a 4, is designated by a 1 bit in the preceding odd bit position, which is 3, plus a 1 bit in the ninth bit position. Every even digit, therefore, contains a 1 bit in the ninth bit position.

Table 3-2 shows the complete Remington Rand code for the numerics, alphabetics, and special characters which are provided for printing. To ascertain from the table what character the code combination 10 0010 represents, read down the column under XX10 of the primed part to the line opposite 0010 of the unprimed part. The character is 2. To ascertain the code combination for a given character, look at the head of its column for the primed part of the code word, and its line of the right-hand column for the unprimed part.

Table 3-2. Remington Rand Code

Primed Part (bit positions 97)				Unprimed Part (bit positions 5310)
XX00	XX01	XX10	XX11	
SPACE	7	9	8	0000
0	C	L	X	0001
1	R	2	F	0010
3	H	4	T	0100
5	G	6	Z	1000
*				0011
E	W	V		0101
M	U	N	(	1001
O	P	Y	:	0110
B	S	A	+ or @	1010
I	Q	K	/	1100
			'	0111
%	#			1011
D	-	,		1101
J	)	.	;	1110
	&	$		1111

3-4. PRINT BUFFER

The print buffer area on the drum stores one line of information to be printed. The information is read from a main-storage band and written into the print buffer under control of the print instruction (11). The print instruction is then cleared from the static register and the processor is free to process other instructions during the printing operation, in which the information is read from the buffer and printed.

The print buffer consists of two tracks, each divided into quadrants. One head writes or reads one bit at a time from each quadrant. Four heads write onto or read from each track, and eight heads serve the entire print buffer. Seven of the eight heads are energized simultaneously to write the seven bits of the code (six bits and the check bit) for each Remington Rand character onto the two tracks of the print buffer. The four bits of the unprimed part of each character of the word are stored temporarily in register A and written into the first track by its four heads. The remaining two bits of the primed part of each character and the check bit associated with each character are stored temporarily in register X and written into the second track by three of its four heads. As soon as writing is completed, the heads on the buffer begin reading the information from the buffer into the print circuits. The heads read continuously except when inhibited during the writing operation.

3-5. SENTINELS

Sentinels control the transfer of the print words from the main-storage band into the print buffer and the reading of these words from the print buffer into the print comparator during printing. Input-output sentinels are described in section 3-86 of the central processor manual. Each sentinel is made up of two types of signals: a timing signal from the cycling unit and one or more TS signals from one of the four tracks of the timing band. The sentinel is stored in one or more word locations of the timing band. For example, the Q4 sentinel is made up of the t11 signal from the cycling unit combined with the TS4 signal from the timing-band read circuit, and is stored in word locations 049 and 099. Table 3-3 shows the makeup of all the printer sentinels. The timing-band word locations of these sentinels are shown on the print-interlace patterns, tables 3-4, 3-5, 3-6, and 3-7.

The $\overline{G3}$ $\overline{G2}$ G1 sentinel clears the print instruction from the static register at gate 20 after the main-storage-to-print-buffer transfer is completed. For a complete list of the input-output sentinels and their functions, refer to appendix B of the central processor manual.

Table 3-3. Printer Sentinels

Timing Signals	Timing-Band Signals			
	TS4	TS3	TS2	TS1
t11	Q4	Q5	Q6	
t10	F	E	D	C
t9				A
t8			B	
t7				Y
t6				
t5			K	
t4		Q3	Q2	Q1
t3	J		I	H
t2	G3*	G2*	G1*	
t1				
t0				

*The one composite printer sentinel, $\overline{G3}$ $\overline{G2}$ G1, is a composite of t2 with $\overline{TS4}$, $\overline{TS3}$, and TS2.

3-6. PRINT-INTERLACE PATTERN 1

Table 3-4, print-interlace pattern 1, shows the W and W' words which are transferred from the print-interlace positions of the main-storage band into the print buffer during the first drum revolution, both in the original main-storage locations and in the print-buffer locations into which they are written. Both the primed and the unprimed portion of each word are written into the print buffer; the print-buffer column of the table shows W1 to represent both W1 and W'1. The first word written into the print buffer (W1) is shown in print-buffer location 156. The six bits and check bit for each character of the word are scattered in locations 006, 056, 106 and 156 of both tracks of the print buffer. The sentinels which control the transfer of the words are also shown in the table.

The A sentinel in timing-band location 198 is the first effective sentinel. This sentinel, with FS 41, operates gate 11 (figure A-2), which steps the static register to the second step of the print instruction. The Q4, Q5, and Q6 sentinels, at timing-band locations 049, 099, 149, and 199, step the quadrant counter each quarter of a drum revolution during writing into the buffer. The B and C sentinels appear one location

before the main-storage location in which one part (either primed or unprimed) of a W word is stored. The B sentinels set the main-storage read flip-flop (figure A-19) at gate 42C to read the word from its main-storage location. The C sentinels set the register-control flip-flop (gate 102, figure A-31) to generate signals to store the word in register A or register X. The F sentinel also appears with the B and C sentinels, but only before the primed portion of a word. The F sentinel sets a control flip-flop which controls gating of the unprimed word into register A and the primed word into register X. The H sentinels appear three times after both the primed and unprimed portions of a word are read and stored in registers A and X. The H sentinels set the write-control flip-flop of the print buffer (gate 900, figure A-29) to write both parts of the word into the two tracks of the print buffer.

The W1, W2, W3, W8, and W9 words are the only words transferred from main storage to buffer storage on the first drum revolution. All are written three times, except word W3, which is written twice. Word W3 is written into the buffer for the third time during the second revolution by the I sentinel. The A sentinel in timing-band location 198 steps the revolution counter (gate 113, figure A-31).

3-7. PRINT-INTERLACE PATTERN 2

Table 3-5, print-interlace pattern 2, shows the W and W' words which are transferred into the print buffer during the second drum revolution, both in the original locations and in the print-buffer locations into which they are written. The sentinels which control the transfer of the words are also shown in the interlace pattern.

The Q4, Q5, and Q6 sentinels, which appear in locations 049, 099, 149, and 199, step the quadrant counter. The B and D sentinels appear one location before a main-storage location in which one part (either primed or unprimed) of a word is stored. The B sentinels set the main-storage read flip-flop and the D sentinels set the register-control flip-flop (gate 103, figure A-31). The F sentinels appear with the D and B sentinels, but only before the primed portion of a word as in interlace pattern 1.

The I sentinels appear three times after both the primed and unprimed portions of a word are stored in registers A and X. The I sentinels set the write-control flip-flop of the print buffer (gate 901, figure A-29).

Word W3 is written for the third time by the first I sentinel. The W10, W4, W11, and W5 words are written three times into the buffer and the W12 word is written once. The A sentinel in timing-band location 198 steps the revolution counter (gate 117, figure A-31).

3-8. PRINT-INTERLACE PATTERN 3

Table 3-6, print-interlace pattern 3, shows the W and W' words which are transferred into the print buffer during the third drum revolution, both in the original locations and in the print-buffer locations into which they are written. The sentinels which control the transfer of the words are also shown in the interlace pattern.

The Q4, Q5, and Q6 sentinels, which appear in locations 049, 099, 149 and 199, step the quadrant counter. The B and E sentinels appear one location before a location in which one part (either primed or unprimed) of a word is stored. The B sentinels set the main-storage read flip-flop and the E sentinels set the register-control flip-flop (gate 104, figure A-31). The F sentinels appear with the B and E sentinels, but only before the primed portion of a word. The J sentinels appear three times after both the primed and unprimed portions of a word are stored in registers A and X. The J sentinels set the write-control flip-flop of the print buffer (gate 902, figure A-29).

Word W12 is written for the second and third times at the beginning of this drum revolution under the control of two J sentinels. The W6, W13, W7 and W14 words are written into the buffer three times. The W14 word is not printed. The $\overline{G3}$ $\overline{G2}$ G1 sentinel in timing-band location 187 ends the transfer by alerting ending-pulse gate 20, which clears the 11 instruction from the static register and generates RCT5 which sets the print flip-flop.

3-9. PRINT-INTERLACE PATTERN 4

Table 3-7, print-interlace pattern 4, shows the W words in the print-buffer locations. The sentinels which control reading these words from the print buffer into the comparator during printing are also shown. The Q1, Q2, and Q3 sentinels in locations 000, 050, 100, and 150 step the quadrant counter during reading from the buffer. The K sentinels, which appear at the beginning of each of the three groups of words, set the first flip-flop of the print word counter (gate 300, figure A-31). The word counter counts the 14 words being read from the buffer. The Y sentinels, which also appear at the beginning of each of the three groups of words, control the print-buffer error flip-flop so that testing for errors only occurs while information is being read from the buffer. The Y sentinels set a control flip-flop (gate 200, figure A-32). The flip-flop output, gated with signals indicating that a comparison and printing operation is taking place, set the print-buffer error flip-flop (section 3-57) if an error exists.

Table 3-4. Print-Interlace Pattern 1 (Memory-to-Buffer Transfer) (Revolution 1)

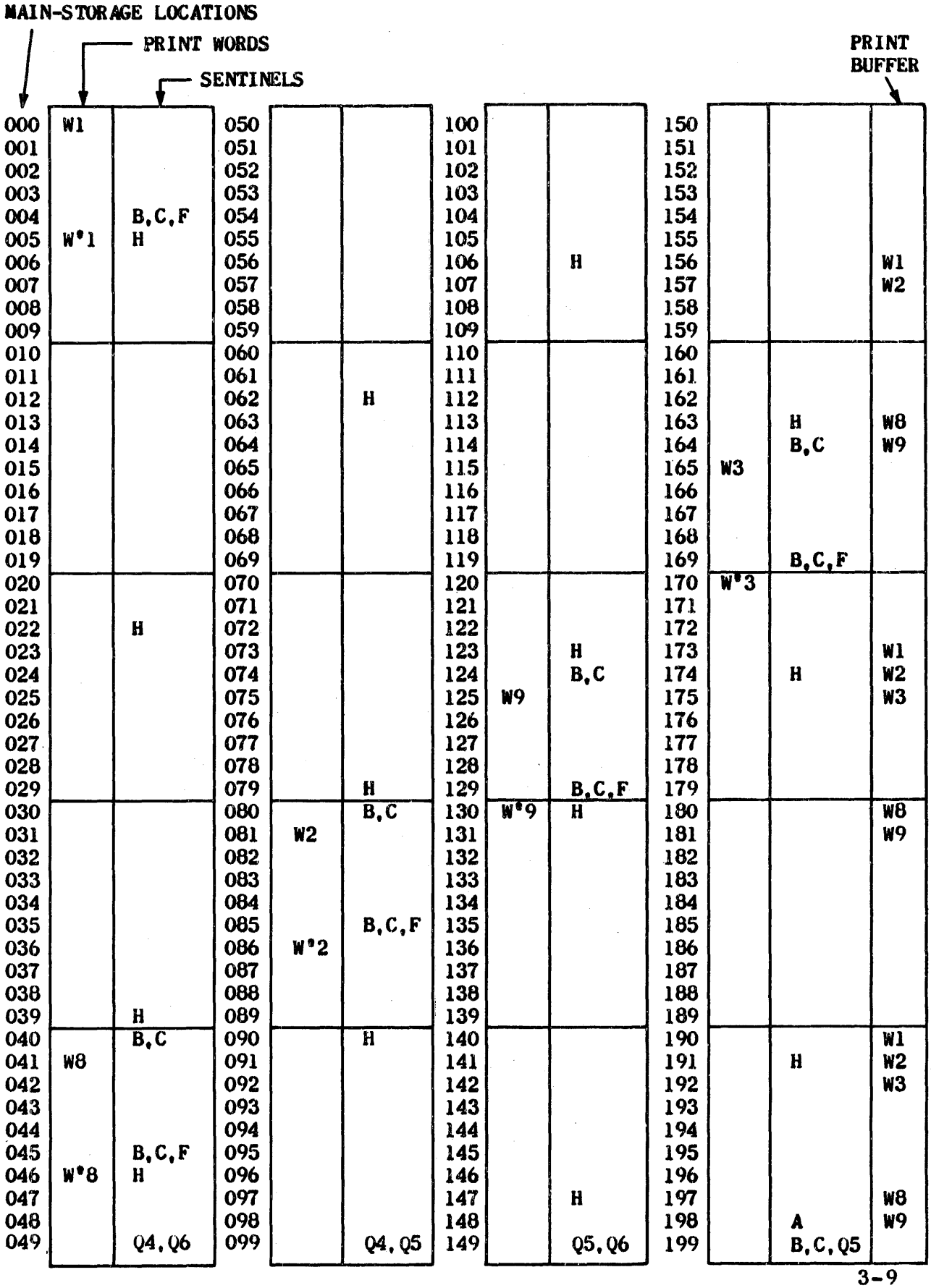


Table 3-5. Print-Interlace Pattern 2 (Memory-to-Buffer Transfer) (Revolution 2)

MAIN-STORAGE LOCATIONS

PRINT WORDS

SENTINELS

PRINT BUFFER

000			050	W4		100			150			W11
001			051			101			151			
002			052			102			152			
003			053			103			153			
004			054		B,D,F	104			154			
005			055	W*4		105			155			
006			056			106			156			
007		I	057			107			157			
008		B,D	058		I	108			158			W3
009	W10		059			109			159		I	W4
010			060			110			160			W5
011			061			111			161			
012			062			112			162			
013		B,D,F	063			113			163			
014	W*10	I	064			114			164			
015			065			115		I	165			W10
016			066			116			166			W11
017			067			117			167			
018			068			118			168			
019			069			119			169			
020			070			120			170			
021			071			121			171			
022			072			122			172			
023			073			123			173			
024			074			124			174			
025			075		I	125			175			
026			076			126			176		I	W4
027			077			127			177		B,D	W5
028			078			128			178	W12		
029			079			129			179			
030			080			130			180			
031		I	081			131			181			
032			082			132		I	182		B,D,F	W10
033			083			133		B,D	183	W*12	I	W11
034			084			134	W5		184			W12
035			085			135			185			
036			086			136			186			
037			087			137			187			
038			088			138		B,D,F	188			
039			089			139	W*5		189			
040			090			140			190			
041			091			141			191			
042			092		I	142			192			
043			093		B,D	143		I	193			W4
044			094	W11		144			194			W5
045			095			145			195			
046			096			146			196			
047			097			147			197			
048		I	098		B,D,F	148			198		A	
049		B,D,Q4 Q6	099	W*11	I,Q4, Q5	149		Q5,Q6	199		Q5	W10

Table 3-6. Print-Interlace Pattern 3
(Memory-to-Buffer Transfer) (Revolution 3)

MAIN-STORAGE LOCATIONS	PRINT WORDS	SENTINELS						PRINT BUFFER		
000		J	050			100			150			
001			051			101		J	151		B,E,F	W12
002			052			102		B,E	152	W*14	J	W13
003			053			103	W7		153			W14
004			054			104			154			
005			055			105			155			
006			056			106			156			
007			057			107		B,E,F	157			
008			058			108	W*7		158			
009			059			109			159			
010			060		J	110			160			
011			061		B,E	111		J	161			W6
012			062	W13		112			162			W7
013			063			113			163			
014			064			114			164			
015			065			115			165			
016		J	066		B,E,F	116			166			
017		B,E	067	W*13	J	117			167			W12
018	W6		068			118			168		J	W13
019			069			119			169			W14
020			070			120			170			
021			071			121			171			
022		B,E,F	072			122			172			
023	W*6		073			123			173			
024			074			124			174			
025			075			125			175			
026			076			126			176			
027		J	077			127			177			
028			078			128		J	178			W6
029			079			129			179			W7
030			080			130			180			
031			081			131			181			
032			082			132			182			
033			083			133			183			
034			084		J	134			184			
035			085			135			185		J	W13
036			086			136			186			W14
037			087			137			187		$\overline{G3}\,\overline{G2}$G1	
038			088			138			188			
039			089			139			189			
040			090			140			190			
041			091			141			191			
042			092			142			192			
043			093			143			193			
044		J	094			144			194			
045			095			145		J	195			W6
046			096			146		B,E	196			W7
047			097			147	W14		197			
048			098			148			198			
049		Q4,Q6	099		Q4,Q5	149		Q5,Q6	199			

Table 3-7. Print-Interlace Pattern 4
(Buffer-to-Comparator Transfer)

MAIN-STORAGE LOCATIONS	SENTINELS						PRINT BUFFER
000	Q2	050	01	100	Q2 Q3	150	Q1	W11
001		051		101		151		W12
002		052		102		152		W13
003		053		103		153		W14
004		054		104		154		
005		055		105		155		
006	Y	056	Y	106	Y	156	Y	W1
007	K	057	K	107	K	157	K	W2
008		058		108		158		W3
009		059		109		159		W4
010		060		110		160		W5
011		061		111		161		W6
012		062		112		162		W7
013		063		113		163		W8
014		064		114		164		W9
015		065		115		165		W10
016		066		116		166		W11
017		067		117		167		W12
018		068		118		168		W13
019		069		119		169		W14
020		070		120		170		
021		071		121		171		
022		072		122		172		
023	Y	073	Y	123	Y	173	Y	W1
024	K	074	K	124	K	174	K	W2
025		075		125		175		W3
026		076		126		176		W4
027		077		127		177		W5
028		078		128		178		W6
029		079		129		179		W7
030		080		130		180		W8
031		081		131		181		W9
032		082		132		182		W10
033		083		133		183		W11
034		084		134		184		W12
035		085		135		185		W13
036		086		136		186		W14
037		087		137		187		
038		088		138		188		
039		089		139		189		
040	Y	090	Y	140	Y	190	Y	W1
041	K	091	K	141	K	191	K	W2
042		092		142		192		W3
043		093		143		193		W4
044		094		144		194		W5
045		095		145		195		W6
046		096		146		196		W7
047		097		147		197		W8
048		098		148		198		W9
049		099		149		199		W10

3-10. MECHANICAL COMPONENTS

3-11. PAPER-FEED MECHANISM

The paper-feed mechanism, under control of the printer synchronizing circuits, advances the paper the number of lines called for in either the 11 or the 16 instruction. The mechanism consists of the paper-feed motor (figure 2-4,1), a magnetic clutch and brake (figure 2-4,2), and a tractor assembly (figure 2-3,1).

The paper-feed motor is normally running, with the clutch disengaged and the brake on. When a paper-advance instruction is given, the brake is released and the magnetic clutch is energized, engaging the motor shaft. When the clutch is engaged, the clutch shaft drives the tractor shaft by means of a belt. The pins on the tractor chains engage the perforations along each edge of the paper to advance it. Clamps on the tractor assembly hold the paper in place against the tractor chains. The paper continues to advance until the clutch is disengaged and the brake applied.

It takes less than one second to advance the maximum number of lines that can be designated by one instruction. In order to prevent runaway paper feeding, relay 2 is energized to disengage the clutch and apply the brake if paper continues to feed for more than one second.

3-12. RIBBON-FEED MECHANISM

Characters are printed by pressing the paper and ribbon against the typewheels. The ribbon-feed mechanism moves the ribbon so that the printed copy is inked uniformly. The mechanism consists of a motor, a drive shaft, and supply and takeup mandrels.

Ribbon feeding begins as soon as a paper-advance or print instruction steps to the second step. The ribbon feeds as long as either instruction remains in the static register.

3-13. ELECTROMECHANICAL COMPONENTS

3-14. CODE WHEEL

The code wheel is a small magnetic drum on which are recorded the six-bit code and check bit for each of the 51 characters, and the 102 sprocket signals which synchronize the print operation. Eight heads continuously read the eight tracks (six code-bit tracks, one check-bit track, and the sprocket track) of the code wheel. The code wheel is aligned with the typewheels mounted on the same shaft, so that the code being read is the code for the next character moving into

print position. The code of the character moving into print position is compared with the code of the characters to be printed. A complete description of the comparison and printing operations is given in section 3-47.

3-15. PAPER-SPACE INDEX DRUM

The paper-space index drum, mounted on the same shaft as the paper-feed clutch and brake, generates an index signal which is fed to the print counter to count the number of lines of paper advance. Six magnetized areas around the circumference of the drum are read continuously by a head during paper feeding. Each magnetized area generates an index signal which indicates that one line of paper has been advanced. The index signal generates the step signal which causes the count in the print counter (section 3-37) to be reduced by one.

3-16. ACTUATORS AND HAMMERS

The printing of a character begins with the firing of a specific print thyratron. When the thyratron fires, a solenoid is energized, causing the print hammer to push the paper and ribbon against the typewheel.

There are 130 actuator and hammer assemblies, two for each typewheel. Figure 3-2 shows one of the assemblies before and after the solenoid is energized. When the print thyratrons are fired, the capacitors are discharged through the solenoid and print thyratrons. The current energizes the solenoid, causing the actuator arm to strike the hammer. The hammer then pushes the paper and ribbon against the typewheel to print a character. The hammers bounce back from the paper and are held in position by springs.

3-17. LOGICAL COMPONENTS

The purpose of this section is to familiarize the reader with the logical components of the printer synchronizer circuits. The reader should be familiar with section II of the central processor manual, which explains the basic logical elements of the synchronizing circuits. The text in this section should be read with the appropriate logical drawings in Manual No. 2. A list of the logical drawings and the corresponding engineering drawings is given in the front of this manual.

3-18. PRINT-BUFFER CIRCUITS

The read and write circuits of the print buffer are shown in figures A-29 and A-30. The read and write circuits of the four heads of track 1, the write flip-flop for tracks 1 and 2, and the quadrant counter for both tracks are shown in figure A-29. The read and write circuits for the four heads of track 2 are shown in figure A-30.

When each word is to be transferred from main storage to the print buffer during the 11 instruction, the write-control flip-flop is set, blocking the buffer-read circuits. As shown in figure 3-3, the set output of the write-control flip-flop also sets the write flip-flop, which alerts the write circuits of both tracks of the print buffer. Under the control of the quadrant counter, the bits of the unprimed word from register A are written onto track 1 and the bits of the primed word from register X are written onto track 2. The write-control and write flip-flops of the print buffer are restored after the word has been written.

When the buffer has been loaded with words to be printed, the 11 instruction is cleared from the static register to remove the inhibition on the read circuits and alert them to read out the contents of the buffer. The information is transferred on the B lines, under control of the quadrant counter, to the print comparator for comparison with the codes from the printer code wheel.

3-19. TRACK 1 OF PRINT BUFFER. The unprimed portion of each of the 13 Remington Rand words to be printed on one line is read from main storage into register A. The contents of register A, ten four-bit groups, is then transferred over the A' lines and written in track 1 of the buffer by the four heads. (The two bits of the primed portion of the 13 words and the check bit from register X are written in track 2.) Each of the heads writes one bit of each four-bit group of the unprimed portion in one of the quadrants of track 1. As shown in figure 3-3, head 1 writes the bit on the $\overline{B1}$ line, head 2 the bit on the $\overline{B2}$ line, head 3 the bit on the $\overline{B3}$ line, and head 4 the bit on the $\overline{B4}$ line. The bits coming from register A are switched onto different B lines at the end of each quarter of the drum revolution to ensure that the ten bits occupying the same bit-position in the ten characters of the word are written into the same quadrant during a complete drum revolution. Four different heads do the writing under the control of the quadrant counter.

During writing, the read circuits for all four buffer heads of track 1 are blocked by the setting of the write flip-flop, and the read output gates, 21B, 22B, 23B, and 24B, are blocked by a high BLPR signal. After the 13 words are written into the buffer, the read circuits are no longer blocked and the information is read onto the B lines of the print buffer into the print comparator. See figure 3-4. The bits read by one head are switched onto a different B line at the end of each quarter of a drum revolution to ensure that the least significant bit (bit 1) of each character, read from one quadrant by four different heads, always reads out onto the B1 line; that bit 2 reads out on the B2 line; that bit 3 reads out onto the B3 line; and that bit 4 reads out on the B4 line. The quadrant-counter outputs control the switching of bits during reading as well as writing.

The logical components associated with track 1, shown in figure A-29, are as follows:

(1) INPUT GATES. The four bits of each character enter track 1 at gates 21A, 22A, 23A, and 24A, which are alerted by FS 42. The bits enter on the A'1, A'2, A'3, and A'4 lines from register A, with the p1 character arriving at t0B.

(2) READ OUTPUT GATES. The four read output gates are alerted by a low BLPR signal present when FS 42A at gate 133 (figure A-29) goes low after writing is completed. The bit read by head 1 reads out through gate 21B, the bit read by head 2 through gate 22B, the bit read by head 3 through gate 23B, and the bit read by head 4 through gate 24B.

(3) WRITE-CONTROL FLIP-FLOP. The write-control flip-flop inhibits the read circuits of the four heads on both track 1 and track 2. Set-gate 900 operates during the first drum revolution ($\overline{RC1}$, $\overline{RC2}$) of the main-storage-to-print buffer transfer whenever an H sentinel is present. The gate, alerted by FS 42, is made permissive by a low $\overline{STR4}$ signal, which indicates that an 11 instruction, rather than a 16 instruction, is in progress. Set-gate 901 operates during the second drum revolution (RC1, $\overline{RC2}$) whenever an I sentinel is present. Gate 902 operates during the third drum revolution (RC1, RC2) whenever the J sentinel is present. The set output of the write-control flip-flop alerts set-gate 1 of the write flip-flop at t4B and generates a high RI signal to block the read circuits of both tracks.

(4) WRITE FLIP-FLOP. The write flip-flop controls the write-input circuits. When set, this flip-flop permits simultaneous writing in the two tracks of the print buffer. The write flip-flop is set at t11B of the word time during which the write-control flip-flop is set. The set output of the write flip-flop, a low PWRB signal alerts the input gates of the write circuits for the eight heads of the two tracks (gates 6A, 6B, 6C, and 6D for track 1, and gates 120, 121, 122, and 123 for track 2). The PWRBA signal alerts the phase-modulation-coder input gates of both tracks, and the IR7 signal generates the RI signal to block the read circuits of both tracks.

(5) WRITE INPUT GATES. Information to be written enters the write input gates of tracks 1 and 2 on the $\overline{B}$ lines from the B-line input gates. The set output of the write flip-flop, signal PWRB, alerts the write input gates to receive the information.

(6) QUADRANT COUNTER. The quadrant counter counts the quarter-revolutions in each complete revolution of the drum in order to control the switching of bits onto the B lines. The counter operates when information from main storage is written onto the print buffer during the second step of a print instruction, and when information is read from the buffer into

the print comparator during printing. The counter, which consists of two flip-flops, has an output combination for each of the four quadrants: QC1 and QC2 (11), $\overline{QC1}$ and $\overline{QC2}$ (00), QC1 and $\overline{QC2}$ (01), and $\overline{QC2}$ and QC1 (10). During each quarter-revolution, one of these output combinations alerts one gate of each of the four groups of B-line input gates. For example, the 11 output combination alerts gates 47D, 48A, 49B, and 50C: a bit read from the print buffer into gate 21B would be switched onto the B2 line, because only gate 48A is alerted to receive the bit from buffer 31. Similarly, a bit read out at gate 22B would be switched to the B3 line, because only gate 49B is alerted to receive the bit. At the end of each quarter-revolution, the quadrant counter is stepped to a new output combination, alerting four new gates.

While information is written onto the buffer during the second step of the print instruction, FS 42 alerts quadrant-counter input gates 18B, 19A, and 20A. These gates are made permissive by combinations of the Q4, Q5, and Q6 sentinels, stepping the counter to the correct sequence for writing.

After the print instruction is cleared from the static register, while information to be printed is read from the print buffer to the print comparator, the set output of the print flip-flop, a low PR signal, alerts quadrant-counter gates 18A and 20B. These gates are made permissive by combinations of the Q2 and Q3 sentinels, stepping the counter to the correct sequence for reading. Gate 19B, controlled by only the Q1 sentinel, operates during both writing and reading. This gate has no effect during writing, however, because it sets FF1 after the Q6 sentinel has already set it at gate 19A.

Figures 3-5 and 3-6 show the sequence of head switching through the four quarter-revolutions of writing and reading. The stepping sequence of the quadrant counter during reading is the opposite of the writing sequence. During writing, corresponding bits must be switched onto successive heads over successive B lines at the end of each quadrant, to keep up with the rotation of the drum. During reading, each of the fixed B lines to the print comparator must be fed from successive heads. Table 3-8 shows the sequence in which the quadrant counter is stepped to control the transfer of information bits from register A onto the moving drum. Table 3-9 shows the sequence which controls the reading of information bits from the moving drum. Both tracks are included in the tables because the quadrant-counter outputs control the switching of bits on both tracks. Table 3-8 shows that, in preparation for the first quarter of a drum revolution, the Q5 sentinel in word location 199 of the timing band steps the quadrant counter at gate 20A to a reading of 00 by restoring FF1 and FF2. The resulting $\overline{QC1}$ and $\overline{QC2}$ outputs of the quadrant counter alert B-line input gates 47A, 48B, 49C, and 50D of track 1, and gates 151, 156, and 161 of track 2. The four bits of the unprimed word on the A'1 through A'4 lines enter the four alerted gates

Table 3-8. Writing into Print Buffer

a. Stepping Sequence of Quadrant Counter

Quarter of Drum Revolution	Sentinel	Location	Gate	Quadrant-Counter Reading	
				FF1	FF2
1	Q5	199	20A	0	0
2	Q4 Q6	049 049	18B 19A	1	1
3	Q4 Q5	099 099	18B 20A	0	1
4	Q5 Q6	149 149	20A 19A	1	0

of track 1 and are written into the quadrants. The two bits of the primed word and the check bit on the X'1, X'2, and X'4 lines enter the three alerted gates of track 2. Head 4 writes 0 bits because the X'3 line from register X contains no information. The table also shows the stepping of the quadrant counter during the last three quarters of the drum revolution, and the B-line input gates which are alerted to switch the bits onto different heads.

Table 3-9 shows that at the beginning of the first quarter of a drum revolution, the Q2 sentinel in word location 000 of the timing band steps the quadrant counter at gate 20B to a reading of 00 by restoring both FF1 and FF2. The resulting $\overline{QC1}$ and $\overline{QC2}$ outputs of the quadrant counter alert B-line input gates 47A, 48B, 49C, and 50D of track 1, and gates 151, 156, and 161 of track 2. The four bits of the unprimed word are read from track 1 of the buffer onto the B1 through B4 lines which feed the print comparator. The two bits of the primed word (bits 5 and 6) and the check bit are read from track 2 of the buffer onto the B5 through B7 lines, which also feed the print comparator. Head 4 reads 0 bits onto the B8 line but this line does not enter the comparator. The table also shows the stepping of the quadrant counter during the last three quarters of the drum revolution, and the B-line input gates which are alerted.

Table 3-8. Writing into Print Buffer (cont)

b. Transfer of Bits

Track 1				Track 2			
Bit	From Line	Through Gate	To Line	Bit	From Line	Through Gate	To Line
Quarter 1 of Drum Revolution							
1	A'1	47A	$\overline{B1}$	5	X'1	151	$\overline{B5}$
2	A'2	48B	$\overline{B2}$	6	X'2	156	$\overline{B6}$
3	A'3	49C	$\overline{B3}$	Check	X'4	161	$\overline{B7}$
4	A'4	50D	$\overline{B4}$	(Line $\overline{B8}$ writes 0 bits)			
Quarter 2 of Drum Revolution							
1	A'1	48A	$\overline{B2}$	5	X'1	155	$\overline{B6}$
2	A'2	49B	$\overline{B3}$	6	X'2	160	$\overline{B7}$
3	A'3	50C	$\overline{B4}$	Check	X'4	165	$\overline{B8}$
4	A'4	47D	$\overline{B1}$	(Line $\overline{B5}$ writes 0 bits)			
Quarter 3 of Drum Revolution							
1	A'1	49A	$\overline{B3}$	5	X'1	159	$\overline{B7}$
2	A'2	50B	$\overline{B4}$	6	X'2	164	$\overline{B8}$
3	A'3	47C	$\overline{B1}$	Check	X'4	153	$\overline{B5}$
4	A'4	48D	$\overline{B2}$	(Line $\overline{B6}$ writes 0 bits)			
Quarter 4 of Drum Revolution							
1	A'1	50A	$\overline{B4}$	5	X'1	163	$\overline{B8}$
2	A'2	47B	$\overline{B1}$	6	X'2	152	$\overline{B5}$
3	A'3	48C	$\overline{B2}$	Check	X'4	157	$\overline{B6}$
4	A'4	49D	$\overline{B3}$	(Line $\overline{B7}$ writes 0 bits)			

Table 3-9. Reading from Print Buffer

a. Stepping Sequence of Quadrant Counter

Quarter of Drum Revolution	Sentinel	Location	Gate	Quadrant-Counter Reading	
				FF1	FF2
1	Q2	000	20B	0	0
2	Q1	050	19B	1	0
3	Q2 Q3	100 100	20B 18A	0	1
4	Q1	150	19B	1	1

3-20. TRACK 2 OF PRINT BUFFER. The primed portion of a Remington Rand word consists of 20 bits, two for each of the ten characters in the word. The primed portion of each of the 13 Remington Rand words to be printed on one line is read from its main-storage location into the first and second subregisters of register X. A check bit is computed for each character of the word and is stored in the fourth subregister of register X. The third subregister contains 0 bits. The information from register X on the X' lines is switched to the correct B line and is written onto track 2 of the buffer by three of the four heads. Each of the heads writes one bit of each character into its respective quadrant. Head 1 writes the bit on the $\overline{B5}$ line, head 2 the bit on the $\overline{B6}$ line, head 3 the bit on the $\overline{B7}$ line, and head 4 the bit on the $\overline{B8}$ line. The outputs from the quadrant counter (figure A-29) switch the bits. The read circuits for all four heads are inhibited during writing by the setting of the write flip-flop (figure A-29), and the read output gates are inhibited by a high BLPR signal.

After all 13 words are written three times in the buffer, the read circuits are no longer inhibited and the information is read onto the B5, B6, and B7 lines into the print comparator. The quadrant counter controls the switching of bits onto different B lines.

Table 3-9. Reading from Print Buffer (cont)

b. Transfer of Bits

Track 1				Track 2			
Bit	From Head	Through Gate	To Line	Bit	From Head	Through Gate	To Line
Quarter 1 of Drum Revolution							
1	1	47A	B1	5	1	151	B5
2	2	48B	B2	6	2	156	B6
3	3	49C	B3	Check	3	161	B7
4	4	50D	B4	(Head 4 reads 0 bits)			
Quarter 2 of Drum Revolution							
1	2	47B	B1	5	2	152	B5
2	3	48C	B2	6	3	157	B6
3	4	49D	B3	Check	4	162	B7
4	1	50A	B4	(Head 1 reads 0 bits)			
Quarter 3 of Drum Revolution							
1	3	47C	B1	5	3	153	B5
2	4	48D	B2	6	4	158	B6
3	1	49A	B3	Check	1	159	B7
4	2	50B	B4	(Head 2 reads 0 bits)			
Quarter 4 of Drum Revolution							
1	4	47D	B1	5	4	154	B5
2	1	48A	B2	6	1	155	B6
3	2	49B	B3	Check	2	160	B7
4	3	50C	B4	(Head 3 reads 0 bits)			

The logical components associated with track 2 are as follows:

(1) INPUT GATES. The two bits of each character enter track 2 at gates 140 and 142 on the X'1 and X'2 lines from register X, and the check bit enters track 2 at gate 144 on the X'4 line. The p1 character arrives at t0B. All of these gates are alerted by FS 42.

(2) READ OUTPUT GATES. The four read output gates of track 2 are alerted by a low BLPR signal which is present when FS 42A goes low after writing is completed. The bit read by head 1 reads out through gate 141; the bit read by head 2 through gate 143; the bit read by head 3 through gate 145, and the bit read by head 4 through gate 146.

(3) WRITE INPUT GATES. The information on the $\overline{B5}$ line enters the write circuit of head 1 of track 2 at gate 120; the information on the $\overline{B6}$ line enters the write circuit of head 2 at gate 121; the information on the $\overline{B7}$ line enters the write circuit of head 3 at gate 122 and the information on the $\overline{B8}$ line enters the write circuit of head 4 at gate 123. All of these gates are alerted by the PWRB signal from the set-write flip-flop (figure A-29).

3-21. MEMORY-TO-PRINT-BUFFER CONTROL

The memory-to-print-buffer control (figure A-31) consists of the following components: the revolution counter, which counts the three drum revolutions required to transfer the print words from main storage into the buffer, the register-control flip-flop, which controls the storing of the unprimed word in register A and the primed word in register X, and the print-word counter which counts the words stored in the buffer.

3-22. REVOLUTION COUNTER. The revolution counter counts the three drum revolutions which are required for the transfer of the print words to the print buffer. The counter consists of two flip-flops which change state during each revolution. Both flip-flops are initially restored by an ending-pulse signal (EP) from a previous instruction to generate a low $\overline{RC1}$ and a low $\overline{RC2}$. These two signals are present at all gates which operate on the first drum revolution of the transfer.

At the end of the first drum revolution, FS 42 and the A sentinel in location 198 operate gate 113 to set the first flip-flop and change the reading to low RC1, $\overline{RC2}$ for the second drum revolution. The $\overline{STR4}$ signal inhibits the operation of gate 113 during a 16 instruction.

At the end of the second drum revolution, the A sentinel and the low signal from the first flip-flop which is set, operate gate 117 to set the second flip-flop and change the

reading to low RC1, RC2 for the third drum revolution. When the 11 instruction is cleared from the static register, the EP signal restores both flip-flops.

3-23. REGISTER-CONTROL FLIP-FLOP. The register-control flip-flop controls two operations: (1) storing the unprimed portion of the word in register A (figure 3-7), and (2) storing the primed portion of the word in register X (figure 3-8). The setting of the register-control flip-flop produces a high PRB signal if the associated control flip-flop is restored, or a high PRY signal if the control flip-flop is set. On the first drum revolution of an 11 instruction, the register-control flip-flop is set at gate 102 by FS 42 and a C sentinel. On the second drum revolution, the D sentinel sets the flip-flop at gate 103, and the E sentinel operates set-gate 104 on the third drum revolution. The F sentinel sets the control flip-flop at gate 100 on any one of the three revolutions, generating a PRY signal. The control flip-flop is set for one word time.

As shown in figure 3-7, the high PRB signal is sent to the function encoder to generate the function signals which read the unprimed word from a main-storage location into register A. Function signals 55+, 56+, 43, 77 and 82A are generated to open the path from the M lines into register A. The recirculation gates of register A are blocked by FS 55+. The input gates of register A, which carry information from the M and S buffers on both the M and S lines, are alerted by FS 77. The contents of register A is normally read out onto the S lines but since the S lines are held low by FS 82A, only the information on the M lines enters register A. The recirculation gates of register X are blocked by FS 56+. The check bits (DM5), which were read from the main storage with the unprimed word, are stored in the fourth subregister of register X at gate 22, alerted by FS 43. See figure 3-7.

The high PRY signal (figure 3-8) is sent to the function encoder to generate the function signals which read the primed word from a main-storage location into register X and also compute new check bits and store them in the same register. Function signals 56+, 76, and 65 are generated to open the path on the M lines into register X. The recirculation gates of register X are blocked by FS 56+. Function signal 76 alerts the input gates of all four subregisters to the information on all four M lines. Function signal 42B+, which is generated by 42A, is also present to inhibit the M3 and M4 input gates so that only information from the M1 and M2 lines reads into register X. Function signal 65 alerts the four check-bit computer gates (gates 23, 24, 25, and 26) to compute a new check bit from the four possible combinations of the check bit from the unprimed character, stored in register X, and the two bits of the primed character. If any one of these gates operates, a 1 bit is stored in the fourth subregister of register X because

the combined character, now stored in register A and register X, contains an even combination. Gate 23 operates if the unprimed character had no check bit ($\overline{X4}$) and the primed-character combination is odd (01 or $\overline{M2}$, M1). Gate 25 operates if the unprimed character had no check bit ($\overline{X4}$) and the primed-character combination is odd (10 or M2, $\overline{M1}$). Gate 24 operates if the unprimed character had a check bit (X4) and the primed character combination is even (11 or M2, M1). Gate 26 operates if the unprimed character had a check bit (X4) and the primed character combination is even (00 or $\overline{M2}$, $\overline{M1}$).

3-24. PRINT-WORD COUNTER. The print-word counter (figure A-31) counts the 14 words stored in the print buffer. The outputs of the counter, PC1 through PC14, are used during printing to gate the signals which set the cores to print characters on the line. The counter consists of a delay flip-flop and 14 flip-flops connected in series. The first flip-flop is set by the K sentinel (TS2/t5B) at gate 300. (As shown in table 3-6, the K sentinels are in the location following the location of the W1 word.) The print signals which set the cores are available one word time after the word that produces the signals is read from the buffer.

The first flip-flop of the print-word counter remains set for one complete word time but the high PC1A and PC1B signals are present only from t7 to t3, because gate 303 is alerted to the low output of the first flip-flop only as long as the delay flip-flop is set (from t6B to t2B). At t5B the first flip-flop is restored and the second flip-flop is set. The PC2A and PC2B signals are present from t7 to t3. The remaining flip-flops are also set at t5B of each word time. The PC14A and PC14B signals count the fourteenth word stored in the buffer but do not gate set signals to the cores because the fourteenth word is not printed. The counter remains cleared after counting to 14 until the next K sentinel occurs to begin counting the second group of the three repeated groups of 14 words stored in the buffer.

3-25. PRINT COMPARATOR

3-26. CODE-STORAGE CIRCUIT. The code-storage circuit (figure A-33), which consists of the seven initial-storage and seven final-storage flip-flops, temporarily stores the seven-bit codes for each of the code-wheel characters. The initial-storage flip-flops store each code for an even cycle, and the final-storage flip-flops store each code for both an odd and an even cycle. The codes are transferred from the code wheel to the initial-storage flip-flops at the beginning of the even cycles, and from the initial-storage flip-flops to final-storage flip-flops, at the beginning of the odd cycles, which are indicated by the low $\overline{PSP}$ signal. The CG1 through CG7 signals and the seven CB and $\overline{CB}$ signals are sent to the print-code error flip-flop (section 3-58).

During an even cycle, shown in figure 3-9, the code for the character currently in print position has been stored in the final-storage flip-flops and is being compared with the print words from the buffer in the comparator. During the same cycle, the code for the character approaching print position is entering the initial-storage flip-flops.

3-27. PRINT COMPARATOR. The print comparator (figure A-33) consists of 14 gates which compare the code for one character of a word at a time, as it is read from the buffer, with the character code stored in the final-storage flip-flops. The seven bits of each character are compared at the same time, each pair of gates comparing one bit. If all seven bits of the two characters are equal, the common output signal, Print, is low, signifying that the characters are alike. If any bit of the two characters is unequal, the Print signal is high, signifying unlike characters. The p0 character enters the comparator gates at t6B as it is read from the buffer on the B lines. The Print signal is high or low, depending upon equality or inequality of the p0 character, at t7B. Gates 21A and 22A compare bit 1, 21B and 22B bit 2, 21D and 22D bit 3, 23A and 24A bit 4, 23B and 24B bits, 23D and 24D bit 6, and 25D and 26D the seventh or check bit. If all gates are inhibited by one high input, all bits are equal. If any one of the 14 gates operates with two low inputs, the characters are unequal.

The ten characters of each of the 14 words enter the comparator serially. The Print signals from the comparator are stored in the print distributor initial-storage and final-storage flip-flops (figure A-34). The outputs of these flip-flops set the cores which print the characters on the line.

3-28. PRINT TIMING CIRCUITS. One hundred and two sprocket pulses are recorded around the circumference of the code wheel. The sprocket read head reads one of the pulses each time a character moves into print position on the 65 typewheels. The sprocket pulse generates control signals which sample the 65 cores to print the information set up as a result of the last sprocket signal and then enable the setting of other cores as a result of the comparison operation. The 65 cores are sampled, but only those previously set generate a signal to fire the associated thyratron and print the character.

The sprocket pulse generates the following control signals to sample the cores: IS1 and IS2, which inhibit setting the cores during sampling; the PRP1 through PRP5 sample signals, and the Select A and Select B signals which gate the sample signals to all cores. If the sprocket pulse is read while an odd character begins to move into print position, a PC' signal is generated to fire the even thyratrons because an even character is in print position. If the sprocket pulse is read as an even character begins to move into print position, a PC signal is generated to fire the odd thyratrons because an odd

character is in print position. These sampling control signals are generated for approximately two word times, as shown in figure 3-9.

The Even and Odd output signals of the sprocket circuit set the cores by alerting the gates of the print distributor (section 3-30) to the signals from the print comparator. If an odd sprocket is read, a low Odd signal is generated to alert one of the two print-distributor gates. If an even sprocket is read, a low Even signal alerts the other gate. Signals which set the cores to print in even position enter at gate 41 to be stored in the initial-storage flip-flops; signals which control printing in odd positions enter at gate 42.

If an odd sprocket is read, a low PSP signal and a high $\overline{\text{PSP}}$ signal are generated to transfer the code from the initial-storage into the final-storage flip-flops. These signals are generated for one-half pulse time. The Odd or Even signal is generated until the next sprocket pulse occurs so that setting up of the cores continues until the next sprocket is read.

The logical components that make up the print timing circuits are as follows:

(1) ODD-EVEN FLIP-FLOP. The odd-even flip-flop generates a signal to alert the print-distributor gates to the print signal from the comparator. The set output of the flip-flop, low Odd signal, alerts one print-distributor gate and the high Even signal blocks the other gate. When the flip-flop is restored, the Even signal is low and the Odd signal is high.

The flip-flop is initially set at gate 180, as the code is read from the code wheel and stored in the code initial-storage flip-flops. The first code containing a one check bit sets the seventh initial-storage flip-flop, alerting gate 180. The next odd sprocket pulse read from the code wheel makes gate 180 permissive, setting the flip-flop and generating a low Odd signal. The next sprocket pulse generates a high AKT signal which restores the flip-flop at gate 134 to generate a low Even signal. The following odd sprocket sets the flip-flop again at gate 133 and also makes gate 158 permissive to generate a low PSP and a high $\overline{\text{PSP}}$ signal. The PSP signal alerts the set gates of the code final-storage flip-flops and reduces by one the reading in the print counter (figure A-35 and section 3-37). The $\overline{\text{PSP}}$ signal restores the code final-storage flip-flops. Gates 133 and 134 operate alternately to set and restore the flip-flop as the sprocket pulses are read from the sprocket wheel.

(2) INHIBIT-SET FLIP-FLOPS. The two inhibit-set flip-flops produce signals which prevent the setting of any cores during core sampling. When the cores are sampled, these flip-flops block the print-distributor gates and the gates of the flip-flops which store the print signal from the comparator.

Because the sprocket pulse, which may occur at any time, is not synchronized with computer timing, the two flip-flops are used to ensure that a high IS signal is available for at least one word time. Inhibit-set FF1 is set at buffers 101 and 102 by the high sprocket signal from gate 179. The flip-flop is not restored until t1B, when gate 104 operates to set inhibit-set FF2. This flip-flop remains set for a complete word time.

(3) PRINT-SAMPLE CIRCUIT. The print-sample circuit controls the sampling of the 65 cores. Its two functions are to generate the Select A and Select B signals, which gate the sample signals to all 65 cores, and to generate the five sample signals, PRP1 through PRP5. (Figure A-34 shows the PRP signals sampling the 65 cores.) Buffer 103 operates to generate a high Select A and a high Select B signal as long as either one of the inhibit-set flip-flops is set. The Select A and Select B signals, in turn, generate the sample signals. Each of the five sample signals is sent to 13 of the cores so that all 65 cores are sampled at one time.

The Select A signal goes to even-numbered buffers 44 through 68 (figure A-34), and the Select B signal goes to odd-numbered buffers 43 through 67. The buffers generate the PRG1 through PRG13 signals which gate the sample signals to all 65 cores. The PRP sample signals are shown in figure A-34 sampling all of the cores.

(4) EVEN-THYRATRON FLIP-FLOP. The even-thyratron flip-flop generates a PC' signal which is sent to the shield (screen) grids of the even thyratrons during sampling, so that only the even thyratrons fire. The flip-flop is set at gate 118 by the Odd signal and a low, delayed AKT signal, both of which are generated by the odd sprocket pulse. The Print CL, IP, and CCEB signals inhibit the setting of the flip-flop. The flip-flop remains set until restored by a high Reset PC and PC' signal from the restored inhibit-set flip-flop.

(5) ODD-THYRATRON FLIP-FLOP. The odd-thyratron flip-flop generates a PC signal which is sent to the shield grids of the odd thyratrons during sampling in order that only the odd thyratrons fire. The flip-flop is set at gate 122 by the Even signal and a low, delayed AKT signal, both of which are generated by the even sprocket pulse. The Print CL, IP, and CCEB signals inhibit the setting. The flip-flop remains set until restored by a high Reset PC and PC' signal from the restored inhibit-set flip-flops.

3-29. PRINT DISTRIBUTOR

3-30. PRINT DISTRIBUTOR GATES. The two print distributor gates, 41 and 42, (figure A-34) select the Print signals from the comparator which are stored to set the cores. Gate 41 selects the Print signals which set the cores to print in the

even positions on the line and rejects the Print signals which set the cores for the odd positions. Gate 42 selects the odd and rejects the even.

The ten characters of a print word are read serially from the print buffer into the print comparator. If one or more of the ten characters is equal to the character being compared, low Print signals are sent to print distributor gates 41 and 42 to set up the cores. One of these gates is alerted at a given time by an Odd or an Even signal, depending upon the state of the odd-even flip-flop. Both gates require low $\overline{PFI}$ and PR signals which indicate that the paper-feed interlock flip-flop is restored and the print flip-flop is set. The IS1 and IS2 signals are high at both gates to inhibit them during sampling but are low during the setting up of the cores. If the Even signal is low, gate 41 operates to store the results of the five even-character comparisons in the initial-storage flip-flops. The results of the five odd-character comparisons are not stored because of the timing at the set gates of the initial-storage flip-flops, as explained in the next section. If the odd signal is low, gate 42 operates to store the results of the five odd-character comparisons.

3-31. PRINT INITIAL-STORAGE FLIP-FLOPS. The Print initial-storage flip-flops store the Print signals from the comparator. If even-gate 41 operates, the Print signal from the comparison of the p1 character, arriving at t8B, is stored in the first flip-flop because gate 1 operates at t10B. The Print signal from the p3 character, arriving at t10B, is stored in the second flip-flop because gate 3 operates at t0B. The p5 character, arriving at t0B, is stored in the third flip-flop because gate 5 operates at t2B. The p7 character, arriving at t2B, is stored in the fourth flip-flop because gate 7 operates at t4B. Because all of the set gates of the print final-storage flip-flops, numbered 13, 15, 17, 19, and 21, operate at t6B, no fifth initial-storage flip-flop is required. The Print signal of the p9 character, arriving at t4B, is stored in the fifth final-storage flip-flop because gate 21 operates at t6B. The Print signals from the p2, p4, p6, p8, and p10 characters enter even-gate 41 but are not stored because they are present at the set gates at t11B, t1B, t3B, t5B, and t7B when the gates are not alerted.

If odd-gate 42 operates, the Print signal from the comparison of the p2 character, arriving at t9B, is stored in the first flip-flop, which is set at t10B. The p4 character, at t11B, is stored in the second flip-flop at t0B. The p6 character, at t1B, is stored in the third flip-flop at t2B. The p8 character, at t2B, is stored in the fourth flip-flop at t4B and the p10 character, at t4B, is stored in the fifth final-storage flip-flop at t6B. The Print signals from the p1, p3, p5, p7, and p9 characters enter odd-gate 42 but are not stored because they are present at the set gates at t9B, t11B, t1B, t3B, and t5B when the gates are not alerted.

3-32. PRINT FINAL-STORAGE FLIP-FLOPS. The print final-storage flip-flops generate the set signals which select the characters to be printed. The four initial-storage flip-flops are restored at t6B. At the same time, set gates 13, 15, 17, and 19 of four final-storage flip-flops are alerted to the information which was initially stored, and set gate 21 is alerted to the Print signals from the p9 or p10 characters. Both the set and restore gates of the five final-storage flip-flops are inhibited by the IS1 or IS2 signals, which are high while the cores are sampled. The outputs of these final-storage flip-flops enter PRS packages. If the first flip-flop is set, the signal from the first PRS package, designated PRS1, is high (figure 3-10). This high signal is sent to the fifth of the five cores associated with each of the 13 words because it signifies that the p1 or p2 character of one of the words is to be printed (columns 9 or 10, 19 or 20, and so on, to 129 or 130).

Figure 3-10 shows the circuits which distribute the set and sample signals to the cores. Figures 3-11 and 3-12 show the setting and sampling circuits in block diagram form.

3-33. PRINT-GATE CIRCUIT. The print-gate circuit gates both the set and the sample signals to the core. Each PRS signal is sent to 13 cores but is gated into only one core by one of the 13 PRG signals, as shown in figure 3-10. The PRG signals select the half word to be stored in the five cores; the PRS signal selects, one by one, the characters of core storage. The print-gate circuit consists of 26 buffers, numbered 43 through 68. The inputs to these buffers are the PC1A through PC13A and the PC1B through PC13B signals from the print-word counter. If the print-word counter is counting the first word, the PC1A and PC1B signals are high, generating a high PRG1 signal which alerts the first five cores associated with the W1 word. If the PRS1 signal is high at the same time, the fifth core is set, preparing columns 9 or 10 for printing. During the setting up of the cores, only one PRG signal is high at a time, but during the sampling operation all 13 PRG signals must be high to gate the sample pulse (PRP) into all 65 cores. The Select A and Select B signals are sent to all 26 buffers to produce high PRG1 through PRG13 signals.

3-34. CORE-STORAGE CIRCUITS. The core-storage circuit stores the results of comparison for a given row of a character (odd or even) on the typewheels until sampling occurs to print the characters. Sixty-five cores control the 65 odd thyratrons and 65 even thyratrons which fire once to print one of the characters on a line. Each core controls one even and one odd thyratron and each core can be set up and sampled twice during the printing of one line to trigger both the odd and the even thyratrons. A core is set if it receives a PRS signal and a PRG signal simultaneously. The set core is sampled by PRP signals to generate a signal which is applied to the control grids of

both thyratrons. Only one of these two thyratrons is triggered by a PC or PC' signal on its shield grid to print a character.

3-35. PRINT THYRATRONS. One hundred and thirty thyratrons control the actuators which force the print hammers against the typewheels to print characters. Each thyratron can be triggered only once during the printing of one line. The capacitor in the plate circuit of each tube is charged while the print instruction is staticized (stored in the static register). Each core controls two thyratrons but only one of the thyratrons has a PC or PC' signal on its shield grid. If the core is set, a signal is applied to the control grids of both thyratrons when the core is sampled. The thyratron with the signal on its shield grid is triggered and the capacitor in the plate circuit is discharged, energizing the actuator in the plate circuit to force the hammer against the typewheel and print the character. See section IV for a description of the thyratron and charge circuits.

3-36. PRINT CONTROL

The print-control circuits (figure A-35) control paper feeding, printing, and abnormal operations. The circuits involved in abnormal operations are described in section 3-55.

3-37. PRINT COUNTER. The print counter (figure A-35) counts the lines of paper advance and the 51 characters printed. It consists of seven flip-flops, a clear circuit and a countdown circuit. If no paper advance is called for, the zero-reading circuit generates a Jam 4 signal which sets up a count of four in the print counter to allow time for the power supply to be disconnected from the print capacitors. If a paper advance is called for, the print counter is cleared and the number of lines the paper is to be advanced is stored in the print counter when the print instruction is staticized. As each line of paper is advanced, a paper-feed index signal is sent to the countdown circuit to reduce the reading by one. A reading of 7 is set up in the counter as the paper-feed flip-flop is restored, after completion of paper advance, to allow time for the paper to settle. This reading is reduced by each odd sprocket from the code wheel and a Jam 51 signal is generated to set the counter to a reading of 51. The 51 count is used during printing, and is reduced by one each time an odd sprocket pulse occurs. After all 51 characters have been printed, a JPC signal is generated to set the print counter to a reading of two to allow time for the last tubes triggered to de-ionize. See section 3-42 for the detailed operation of gate 24 for the 7, 51, and 2 countdown control.

The print counter is initially cleared by FS 42 at gate 8 at every tOB of the first drum revolution (RC1) of the memory-to-print-buffer transfer. The high CLP output signal is sent to buffers 6A, 6B, 6C, and 6D to restore flip-flops 1, 2, 3,

and 4 unless these flip-flops are set by the number of lines of paper advance. The CLP signal is also sent to buffers 6E, 6F, and 6G to restore flip-flops 5, 6, and 7. These flip-flops are then set by the number of lines of paper advances. The paper-advance reading is set up at each t2B and t3B of every word time of the first drum revolution and cleared at t1B of the next word time. The setting and clearing takes place 199 times during the first drum revolution. On the 200th time, the reading is not cleared because $\overline{RC1}$ is no longer present at gate 8.

The four bits of the p5 digit of the 11 or 16 instruction stored in register C are on the S1 through S4 lines at t1B. Function signal 42 alerts input gates 7A, 7B, 7C, and 7D at every t1B of the first drum revolution ($\overline{RC1}$) to store these bits in the first four flip-flops of the print counter. The four bits of the p6 digit are on the S1 through S4 lines at t2B. Function signal 42 alerts input gates 7E, 7F, and 7G at every t2B of the first drum revolution ($\overline{RC1}$) to store bits 1, 2, and 3 in the remaining three flip-flops of the print counter. Bit 4 is not stored. Because only three bits of the p6 digit are stored, the UCT code for the digits 5 (1000), 6 (1001), 7 (1010), 8 (1011), and 9 (1100) stored in the print counter is the same as the code for the digits 0 (0000), 1 (0001), 2 (0010), 3 (0011), and 4 (0100). This restricts the p6 digit to decimal 4 or less and limits the maximum lines of paper feeding to 49. If the programmer wishes to feed paper from 50 to 79 lines, he can write a K into the p6 digit position of the m address for a 5, a Y for a 6, or a T for a 7. When these are translated from Remington Rand code into UCT code, the K becomes 1101, the Y 0110, and the T 1111.

The countdown circuit for the counter has two input gates. Input gate 1 operates to count down the paper-advance reading by generating a step signal which reduces the reading by one. Gate 1 operates at t5B if the paper-feed flip-flop is set (PF signal), each time an Index signal is present as a result of one line of paper being fed. The low step signal is generated and a high signal is sent to gate 31 to restore the paper-space index flip-flop. Input gate 2 is inhibited by FS 42A and the high PF signal from the set paper-feed flip-flop. Gate 2 operates to count down the Jam 4, Jam 7, Jam 51, and JPC readings. Function signal 42A is low because the 11 instruction is no longer set up in the static register, and $\overline{PF}$ is low because the paper-feed flip-flop is restored. The PSP signal is present whenever an odd sprocket pulse is read from the code wheel to operate gate 2 and generate the step signal. Gate 1 is inhibited by the high PF and Index signals.

The step signal alerts gates 5A through 5J. One or more of these gates operates, according to the reading currently set up in the counter. If gate 5A operates, FF1 is restored. If gate 5B operates, FF2 is restored and the high Set 1 signal

Table 3-10. Print-Counter Countdown

Print-Counter Reading Before Countdown		Count Down p6 Digit		
Digits p6 p5	Flip-Flops 765 4321	FF7	FF6	FF5
79	111 1100			
78	111 1011			
77	111 1010			
76	111 1001			
75	111 1000			
74	111 0100			
73	111 0011			
72	111 0010			
71	111 0001			
70	111 0000			Gate 5G
70	111 0000			Gate 5G
60	110 0000		Gate 5H	Buff 20A Set 5
50	101 0000			Gate 5G
40	100 0000	Gate 5J	Buff 21A Set 6	Buff 20A Set 6
30	011 0000			Gate 5G
20	010 0000		Gate 5H	Buff 20A Set 5
10	001 0000			Gate 5G

Table 3-10. Print-Counter Countdown (cont)

Count Down p5 Digit				Print-Counter Reading After Countdown		
FF4	FF3	FF2	FF1	Flip-Flops 765	4321	Digits p6 p5
	Gate 5D	Buff 17A Set 2	Buff 16A Set 2	111	1011	78
			Gate 5A	111	1010	77
		Gate 5B	Buff 16A Set 1	111	1001	76
			Gate 5A	111	1000	75
Gate 5F	Gate 5C			111	0100	74
	Gate 5D	Buff 17A Set 2	Buff 16A Set 2	111	0011	73
			Gate 5A	111	0010	72
		Gate 5B	Buff 16A Set 1	111	0001	71
			Gate 5A	111	0000	70
Gate 5E	Gate 5C			110	1100	69
				110	0000	60
				101	0000	50
				100	0000	40
				011	0000	30
				010	0000	20
				001	0000	10
				000	0000	00

goes to buffer 16A to set FF1. If gate 5C operates, FF3 is set. If gate 5D operates, FF3 is restored and the high Set 2 signal goes to buffer 17A to set FF2. If gate 5E operates, FF4 is set. If gate 5F operates, FF4 is restored. If gate 5G operates, FF5 is restored. If gate 5H operates, FF6 is restored and the high Set 5 signal goes to buffer 20A to set FF5. If gate 5J operates, FF7 is restored and the high Set 6 signal goes to buffer 21A to set FF6, and to buffer 20A to set FF5.

Table 3-10 shows the countdown of the print counter from the maximum reading of 79 to a reading of zero. The table gives the gate or buffer which changes the state of each flip-flop of the print counter, and the signal which alerts each buffer (for example, Set 1). The countdown of the p5 digit from nine through zero is given only once, since it is performed the same way each time.

The Jam 4 reading is sent to buffer 18A (figure A-35) to set FF3 and create a p5 digit of 0100. The Jam 7 reading is sent to buffer 6A to restore FF1 which is still set because no index signal has restored it. Jam 7 also goes to buffers 17A and 19A to set FF2 and FF4 and create a p5 digit of 1010. The Jam 51 reading is sent to buffers 16A, 20A, and 22A to create a p5 digit of 0001 and a p6 digit of 101. The JPC reading is sent to buffer 17A to set FF2 and create a p5 digit of 0010. The JPC signal also goes to buffers 6A, 6E, and 6G to restore FF1, FF5, and FF7 to clear out the Jam 51 reading which is not needed.

If all signals are low because of a zero reading, the low $\overline{\text{P1A}}$ through $\overline{\text{P7A}}$ signals are sent only to gate 33 to inhibit the setting of the paper-feed flip-flop.

3-38. ZERO-READING CIRCUIT. The zero-reading circuit generates a delay signal which provides time to disconnect the power supply from the print capacitors. The p5 and p6 digits are completely set up in the print counter by t3B of the first word time of the first drum revolution. The barred outputs of the seven flip-flops are sampled at t4B by FS 42 at gate 26. If they are all low, indicating a zero reading, a Jam 4 signal is generated and stored in the print counter. The reading is counted down by the PSP signal.

3-39. PAPER-SPACE INDEX FLIP-FLOP. The paper-space index flip-flop stores the signal generated from the paper-space index drum each time one line of paper is fed. The low Index signal alerts gate 1 to step the print counter if paper is being fed as a result of an 11 or 16 instruction. The high signal from buffer 3 restores the flip-flop each time a step signal is generated.

3-40. SPACE-PAPER FLIP-FLOP. The space-paper flip-flop stores the signal generated by the SPACE PAPER button on the printer panel. When the button is pushed the flip-flop is set at buffer 121 and a signal is sent to buffer 124 to advance the

paper one line. The signal from the paper-space index drum sets the paper-space index flip-flop. The Index A signal restores the space-paper flip-flop at buffer 119 if paper is being fed manually.

3-41. PAPER-FEED FLIP-FLOP. The paper-feed flip-flop controls the feeding of paper. It is set at gate 36 by FS 42 at t5B of the first word time of the first drum revolution ($\overline{RC1}$) unless a zero reading ($\overline{P1A}$ through $\overline{P7A}$ low) has been set up in the print counter. The IP signal inhibits the set gate if the NO PRINT button on the central processor operator's panel has been pushed. Function signal 55+ also inhibits set gate 36 during the first drum revolution when the unprimed word is being sent into register A and the S lines are held low by FS 82A. The information on the S lines might otherwise set up a false reading in the print counter which could set the paper-feed flip-flop even though the program called for a zero paper advance. Function signal 55+, which is present at the same time that FS 82A is present, inhibits the setting of the paper-feed flip-flop.

The low PF signal alerts gate 1 and the high $\overline{PF}$ signal inhibits gate 2 of the print-counter countdown circuit when the flip-flop is set. The high PF signal inhibits gate 1 and restores the paper-space index flip-flop at gate 31. The low $\overline{PF}$ signal alerts gate 2 when the paper-feed flip-flop is restored. Signals are also sent to the paper-feed control circuits and to the paper-feed brake to move the paper while the flip-flop is set, and to stop advancing paper when the flip-flop is restored. The high C1A signal from the set paper-feed flip-flop goes to buffer 130 to keep the charge-control flip-flop set while paper is advancing. The paper-feed flip-flop is restored at gate 25 after the last line of paper has been fed. The P1, $\overline{P2}$, $\overline{P3}$, $\overline{P4}$, $\overline{P5}$, $\overline{P6}$, and $\overline{P7}$ signals at the gate indicate a reading of one in the print counter, and the Index signal indicates that the last line of paper has been fed. A high Jam 7 signal is generated to delay printing until the paper settles. The Jam 7 signal restores the paper-feed flip-flop. A PFE (paper-feed-error) signal, which indicates that paper has advanced for more than one second, restores the flip-flop at buffer 29, and the Print CL signal from the NO PRINT button on the operator's panel also restores it at gate 34.

3-42. PAPER-FEED INTERLOCK FLIP-FLOP. The paper-feed interlock flip-flop prevents a second 11 or 16 instruction from being processed while paper is being fed, and also inhibits printing while paper is advancing. The flip-flop is initially set by FS 42A at buffer 38. The set outputs of the flip-flop are a low PFI, a high $\overline{PFI}$, a high $\overline{PFIA}$, and a low INTP. The low INTP signal generates an ending pulse during the 27 instruction which tests the availability of the printer. If paper is advancing or printing is taking place, the INTP signal clears the 27 instruction from the static register. The high $\overline{PFI}$ signal

blocks gates 11 and 12 of the static register to keep the next 11 or 16 instruction staticized until the present 11 or 16 instruction is completed. The $\overline{PFI}$ signal also blocks print distributor gates 41 and 42 (figure A-34), which control printing, and inhibits gates 17, 18, 24, 116, and 117 (figure A-32) to prevent the generation of a print-code error or print-buffer error signal.

The paper-feed interlock flip-flop remains set while paper is advancing and also during the Jam 7 delay for paper settling. When the reading of seven has been counted down to a reading of one ($\overline{P1}$, $\overline{P2}$, $\overline{P3}$, $\overline{P4}$, $\overline{P5}$, $\overline{P6}$, $\overline{P7}$) and the step signal is generated to reduce the reading to zero, gate 24 operates to restore the flip-flop and a high Jam 51 signal is generated to prepare for printing. A low signal is also sent to gate 37 but it does not operate at this time. The 51 reading is counted down during the printing operation to a reading of one. Gate 24 operates for the second time and two low signals are sent to gate 37. The low PR signal from the set print flip-flop supplies the third low signal to make gate 37 permissive. Gate 37 restores the print flip-flop and generates a JPC signal which sets the paper-feed interlock flip-flop again and jams a reading of two into the print counter. Gate 24 operates for the third time to restore the flip-flop.

3-43. CHARGE-CONTROL FLIP-FLOPS. The charge-control flip-flop controls charging the actuator capacitors in the plate circuits of the 130 print thyratrons before printing begins. The flip-flop is set at buffer 131 by the high STC signal from the register-control flip-flop.

The power supply is connected to the capacitors while the charge-control flip-flop is set. When the C1A signal goes low, signifying that paper is no longer advancing, and 42A goes below, signifying that the transfer to the print buffer is completed, the flip-flop is restored. The IP signal from the NO PRINT button on the control panel can also restore the flip-flop.

3-44. PRINT FLIP-FLOP. The print flip-flop holds the indication that the printing operation is taking place. It is set by the RCT5 signal at buffer 43. The RCT5 signal is generated by the clearing of the 11 instruction from the static register at gate 20 (figure A-2) after the print words are completely stored in the buffer. The low PR signal from the set print flip-flop and the low $\overline{PFI}$ signal from the restored paper-feed interlock flip-flop alert the print distributor gates, 41 and 42 (figure A-34), to enable printing to begin. The high $\overline{PR}$ signal continues the inhibition of gates 11 and 12 of the static register to prevent the processing of a second print instruction while printing is in progress. The INTP signal is also generated while the print flip-flop is set to alert the ending-pulse gate of the 27 instruction. The print flip-flop is restored by the operation of gate 37 when the print counter is stepped from one to zero after the last of the 51 characters has been printed.

3-45. RIBBON-FEED CIRCUIT. Ribbon is fed as long as FS 42A is high at buffer 132 during the second step of the print instruction.

3-46. NORMAL OPERATIONS

The normal operations of the printer are controlled by two instructions: 11 and 16. These instructions are briefly discussed in section 3-2, and a detailed analysis of their operation is presented in the following sections.

In the first step of an 11 instruction, a search is made for the band in which the print words are stored. The number of the band is designated by the p7 and p8 digits of the m address. If the previous print or paper-advance instructions has been completed and the printer is operating normally, the static register is stepped to the second step when the band is located.

The second step requires three drum revolutions. During the three revolutions, the words to be printed are read from the storage band and written into the print buffer. The 13 words are written into the buffer in three places to shorten access time.

Registers A and X are used as intermediate storage to hold the unprimed and primed parts of each of the 13 words read from the storage-band locations as they are written into the buffer. The unprimed portion of one word is read from its storage-band location into register A, and the primed portion into register X. New check bits are computed for each character of the word and are stored in register X. When both parts of the word are stored in the registers, the entire word is written into the print buffer in three places. Paper advance also begins during the second step of the 11 instruction but continues after the instruction is cleared from the static register on completion of the transfer.

3-47. ADVANCE AND PRINT INSTRUCTION (11)

The functions of the 11 instruction are to transfer the print words from the storage band specified by the m address to the print buffer, to advance the paper the number of lines specified by the p5 and p6 digits, and to initiate the print operation. The two steps required to execute the 11 instruction are designated PR1 and PR2.

3-48. PR1 STEP. In the first step of the print instruction, a search is made for the band in which the print words are stored. Unlike the usual search for a specific address, the search is only for the band. The p7 and p8 digits of the instruction specify the number of the band. The staticized 11 instruction generates FS 41A which, in turn, generates function signals 1, 58+, 63, 30+, and 41 at t0B. Function signals 1,

58+, and 63 are some of the same functions signals which are generated during a search for a specific address. Function signal 30+ ensures that only the band is searched for by restoring TS FF at gate 100 (figure A-12). Function signal 30+ also keeps the band selected by blocking the restore gates, 62 and 63, of the band-selection flip-flops (figure A-18). If the storage band selected is one of the fast bands, only the 00 head, which corresponds to the head on the normal bands, is used to read from the band. Function signal 30+ keeps quadrant-selection flip-flops 1 and 2 restored at gates 34 and 38 (figure A-18).

Function signal 41 (with $\overline{\text{STR4}}$) alerts step-gate 11 of the static register to advance to the second step. The gate also requires the presence of the A sentinel (TS1 at t9B) which occurs in location 198, and low $\overline{\text{PR}}$ and $\overline{\text{PFI}}$ signals which indicate that the previous print instruction is completed. Gate 12 is also alerted by FS 41 but the STR4 signal blocks it. Function signal 41 also alerts gate 100 of the input-output abnormal-condition flip-flop (section 3-56). The operation of gate 11 sets the STR2 flip-flop to change the reading in the static register to 13, initiating the PR2 step.

3-49. PR2 STEP. The new reading in the static register, 13, generates FS 42A at t0A of word time 199. Function signal 42A sets the paper-feed interlock flip-flop, starts ribbon feeding, and blocks the read-input circuits of the print buffer by generating a high BLPR signal. Function signal 42A also inhibits step gate 2 of the print-counter countdown circuit so that only step-gate 1 operates to count down the paper-advance reading set up in the print counter.

The p5 and p6 digits of the m address, which specify the lines of paper advance, are sent from register C onto the S lines and stored in the flip-flops of the print counter. Function signal 63 alerts the output gates to keep the contents of register C reading onto the S lines, and FS 58+ blocks the contents of register A from reading onto the S lines.

The print counter is cleared at t1B and the input gates of the first four flip-flops are alerted to the p5 digit on the S lines from register C at t1B. The input gates of the last three flip-flops are alerted to the p6 digit at t2B. If the reading set up is a zero reading, a Jam 4 signal is set up in the print counter to be counted down by the odd sprocket pulses (PSP). If the reading set up is a non-zero reading, the paper-feed flip-flop is set, releasing the paper-feed brake and energizing the clutch.

(1) FIRST DRUM REVOLUTION. The interlace pattern for the first drum revolution during the writing of words into the buffer is shown in table 3-4. The B sentinel in location

199 sets the main-storage read flip-flop to prepare to read the W1 word from its 000 location onto the M lines. The C sentinel in the same location sets the register-control flip-flop to generate a PRB signal which opens up the path for the word into register A as described in section 3-23. The setting of the register-control flip-flop in turn sets the charge-control flip-flop to begin the charging of the actuator capacitors.

The B sentinel in location 004 sets the main-storage read flip-flop to prepare to read the W'1 word from its 005 location onto the M lines. The C sentinel in the same location sets the register-control flip-flop and the F sentinel sets the control flip-flop so that a PRY signal is generated instead of a PRB signal, as before. The PRY signal opens the path for the primed word into register X as described in section 3-23. Both parts of the W1 word are stored in registers A and X ready to be written into the two tracks of the buffer.

The H sentinel in location 005 sets the write-control flip-flop to inhibit the read circuits of both tracks. At t11B of word 005, the write flip-flop of the print buffer is set and the write circuits of both tracks are alerted to information on the $\overline{B}$ lines. Function signal 42 alerts the input gates of print-buffer track 1 to the A'1 through A'4 outputs of register A, and the input gates of track 2 to the X'1, X'2, and X'4 outputs of register X. The quadrant-counter reading is FF1 = 0 and FF2 = 0, as a result of the Q5 sentinel in location 199. The six bits of the W1 word and the check bit are written into the two tracks of the print buffer by the four heads on each track. Table 3-4 shows the W1 word stored in location 156 of the print buffer, but the bits are scattered into the 006, 056, 106, and 156 locations. The write flip-flop is restored at t11B of word 006. The W1 word is still circulating in registers A and X. The H sentinel in location 022 again sets the write-control flip-flop and the W1 word is written for the second time into the 023, 073, 123, and 173 locations of the buffer. The third H sentinel in location 039 initiates the third writing of the W1 word into the 040, 090, 140, and 190 locations of the buffer.

The B sentinel in location 040 sets the main-storage read flip-flop to read the W8 word from location 041 into register A, and the C sentinel sets the register-control flip-flop to open up the path into the register. The B, C, and F sentinels in location 045 read the W'8 word from its 046 location and open the path into register X. The H sentinel in location 046 writes the W8 word into the 047, 097, 147, and 197 locations of the print buffer. The Q4 and Q6 sentinels, in location 049, step the quadrant counter to a reading of FF1 = 1, FF2 = 1 so that different heads write similar bits into the same quadrants during the second quarter of the first drum revolution. The H sentinels in 062 and 079 write the W8 word two more times into

the buffer. The remaining B, C, and F sentinels (table 3-4) read the W2, W9, and W3 words from their locations, and the H sentinels control the writing of these words into the buffer. The Q4 and Q5 sentinels in 099 and the Q5 and Q6 sentinels in 149 step the quadrant counter. The A sentinel in location 198 steps the revolution counter to a reading of RC1, $\overline{RC2}$. The Q5 sentinel in location 199 steps the quadrant counter back to the 00 reading for the first quarter of the second drum revolution.

(2) SECOND DRUM REVOLUTION. The interlace pattern for the second drum revolution is shown in table 3-5. The W10, W4, W11, W5, and W12 words are read from their locations in main storage into registers A and X, and are written into the print buffer. The B sentinels control the setting of the main-storage read flip-flop, the D sentinel sets the register-control flip-flop, and the F sentinel sets the control flip-flop. The write-control flip-flop of the buffer is set by the I sentinel, and the Q sentinels in locations 049, 099, 149, and 199 step the quadrant-counter as in the first revolution. The A sentinal in location 198 steps the revolution-counter to a reading of RC1, RC2.

(3) THIRD DRUM REVOLUTION. The interlace pattern for the third drum revolution is shown in table 3-6. The W6, W13, W7, and W14 words are read from main storage into registers A and X, and are written into the buffer. The B sentinels again control the setting of the main-storage read flip-flop, the E sentinels set the register-control flip-flop, and the F sentinel again sets the control flip-flop. The write-control flip-flop of the buffer is set by the J sentinel and the Q sentinels again step the quadrant counter. The $\overline{G3}$ $\overline{G2}$ G1 sentinel in location 187 alerts static-register gate 20 to generate an ending pulse to clear the 11 instruction. A high RCT5 signal is generated by the operation of gate 20 to restore the CT flip-flop to search for the next instruction and staticize it. The RCT5 signal also sets the print flip-flop (figure A-35) to indicate that the buffer is fully loaded. Function signal 42A goes low to end ribbon feeding and to remove the inhibition from the read circuits of the buffer.

3-50. PAPER ADVANCE. Paper advance begins during the PR2 step but continues after the 11 instruction has been cleared from the static register. The actual printing of the line does not begin until the paper has advanced the full number of lines set up in the print counter. Each line of paper advanced sets paper-index flip-flop to reduce by one the reading in the print counter. When the counter is reading one and the last line is advanced, the paper-feed flip-flop is restored. Paper advance stops and a Jam 7 reading set up in the print counter allows the paper to settle. The charge-control flip-flop is restored and the actuator capacitors no longer charge. Gate 2 of the print counter, no longer inhibited by FS 42A and the high $\overline{PF}$ signal, operates to step down the reading of seven which is

jammed into the print counter by the restoring of the paper-feed flip-flop. The PSP signal steps the Jam 7 reading to a count of one. The next step signal restores the paper-feed interlock flip-flop and jams a reading of 51 into the print counter in preparation for printing.

The high $\overline{PR}$ signal from the set print flip-flop inhibits step gates 11 and 12 of the static register. The low PR and low $\overline{PFI}$ signals, which indicate that the buffer is completely loaded and the paper is completely advanced, alert the print distributor gates to the print signals.

3-51. PRINTING. The read circuits of the print buffer are blocked during the time that the print instruction is staticized. As soon as the words are written into the buffer and the 11 instruction is cleared from the static register, the read circuits read the stored information onto the B lines. The quadrant counter is stepped each quarter of a drum revolution during reading by the Q1, Q2, and Q3 sentinels which are shown in table 3-7 in locations 000, 050, 100, and 150. The stepping of the quadrant counter gates the information read from the same quadrant by four different heads onto the same B line. The six B lines which carry the six bits of each character and the seventh B line which carries the check bit enter the fourteen input gates of the print comparator.

The code for the character moving into print position is read from the code wheel and stored in the seven code initial-storage flip-flops on an even cycle. When the next odd sprocket pulse is read from the code wheel and a PSP signal is generated, the code is transferred into the code final-storage flip-flops. The 14 outputs of the code final-storage flip-flops enter the print comparator where they are compared for equality with the 14 outputs of the print buffer. If the characters are alike, a low Print signal is sent to the two print distributor gates. These gates are alerted by the low PR signal from the print flip-flops, which was set as the 11 instruction was cleared from the static register. The gates are inhibited by the high $\overline{PFI}$ signal from the paper-feed interlock flip-flop. This flip-flop remains set until the paper is completely advanced and the Jam 7 reading in the print counter has been reduced to zero.

The result of the odd sprocket (Step signal), which restores the paper-feed interlock (PFI) flip-flop, also sets the inhibit-set-1 flip-flop, so that the high IS1 signal can inhibit the print distributor gates which are no longer inhibited by the high PFI. As the paper-feed interlock flip-flop is restored, a reading of 51 is set up in the print counter to count the characters as they are printed. The PSP signal, generated from the same odd sprocket which restored the PFI flip-flop, alerts the input gates of the seven code final-storage flip-flops to the seven bits of the code for the odd character moving into print position.

The high IS signals from the odd sprocket inhibit the setting of any cores while the cores which were set up as a result of the last even sprocket are sampled. The Select A and Select B signals gate the sample pulse into the 65 cores. The PC' signals are sent to the grids of all even thyratrons. Because no cores are set up, none of the thyratrons fire.

The IS1 and IS2 signals from the inhibit-set flip-flops are high for approximately two word times after the sprocket pulse is read. When these signals go low, sampling ends and the print distributor gates are permissive to the print signals from the comparator. Because the odd sprocket pulse sets the odd-even flip-flop, gate 42 is alerted by the low Odd signal but gate 41 is inhibited by the high Even signal. Only the Print signals generated as a result of the comparison of the p2, p4, p6, p8, or p10 characters enter gate 42 and are stored in the print initial-storage flip-flops to set the cores. The Print signals from the comparison of the p1, p3, p5, p7, and p9 characters enter gate 42, but are not stored, because of the timing at the set gates of the Print initials storage flip-flops.

For example, assume that the odd character moving into print position is an M, as print distributor gate 42 becomes permissive to the Print signals, and that the p1 character of the W10 word is being read from the buffer into the comparator. The printing of a line may begin with any one of the 51 characters and with any one of the 13 words. If the p1 character of the W10 word is an M, a low Print signal is generated and arrives at gate 42 at t8B. The Print signal, however, is not stored in an print-initial-storage flip-flop because the p1 character of the W10 word is printed in even column 100 and only the cores for the odd print positions are set up. For example, if the p2 and p8 characters of the W11 word are both M's, the low Print signal from the p2 character arrives at gate 42 at t9B and is stored in the first Print initial-storage flip-flop at t10B. The low Print signal from the p8 character arrives at gate 42 at t3B and is stored in the fourth Print initial-storage flip-flop at t4B.

At t6B all set gates of the print final-storage flip-flops are alerted. The first and fourth final-storage flip-flops are set, generating PRS1 and PRS4 signals. The print-word counter counts the 11th word at the same time. The PC11A and the PC11B signals from the print-word counter to buffers 63 and 64 of the print distributor generate signal PRG11 to gate signals PRS1 and PRS4. Signal PRS1 is gated into the core which controls printing in columns 109 and 110, and PRS4 is gated into the core which controls printing in columns 103 and 104.

If no M's are to be printed in the W12 or W13 words, no more cores are set up as a result of reading these words from

the print buffer. The W14 word, which is stored in the buffer, is compared but the results of the comparison do not set up any cores.

When the W1 through W9 words are read from the buffer and compared with the code for M, cores are set up as previously described for words W10 through W14. The 13 words have been completely scanned for odd M's by the time that the cores for the W9 word are set up. Because scanning each word requires 17 microseconds, scanning the 13 words requires approximately 221 microseconds. An additional 34 microseconds is required at the beginning of the cycle to sample the cores, making a total of 255 microseconds. The time between sprocket pulses is approximately 800 microseconds. Consequently, the selected cores receive several set signals before the next sprocket pulse occurs to sample them.

The code for the next character, N, is stored in the seven code initial-storage flip-flops as the even sprocket pulse is read from the code wheel. The code for M remains stored in the code final-storage flip-flops because no PSP signal is generated by the even sprocket pulse. The even sprocket restores the odd-even flip-flop to generate a low Even signal which alerts gate 41, and a high Odd signal which inhibits gate 42. The IS signals inhibit both gates 41 and 42, and the cores are sampled. The cores which are set generate a signal to the grids of the associated thyratrons. Both the core which controls columns 109 and 110 and the core which controls columns 103 and 104 are set. As a result of the even sprocket pulse, a PC signal is applied to the grids of the thyratrons which print in odd columns 109 and 103. An M is printed in columns 109 and 103, but not in column 110 or column 104.

When the IS signals go low, the cores are set up to print the even M's. The Print signals from the comparison of the p1, p3, p5, p7, and p9 characters of the 13 words are stored because these characters are printed in even columns, but the Print signals from the p2, p4, p6, p8, and p10 characters are not stored.

The next odd sprocket pulse (PSP) transfers the code for N into the code final-storage flip-flops to replace the code for M. The PSP signal also reduces the 51 reading in the print counter to a reading of 50 because the character M has been completely printed. The cores set up to print the even M's are sampled and the cores are set up to print the odd N's.

All 51 characters are set up, sampled, and printed in the same manner as M and N. The PSP signal which transfers the code for the 51st character into the code final-storage flip-flops also generates a step signal for the print counter. The reading of one in the counter and the step signal restore the paper-feed interlock flip-flop and generate the JPC signal to

provide a delay while the last thyratrons to be fired deionize. Four sprockets later the JPC delay is counted down and another print instruction can be executed.

3-52. ADVANCE INSTRUCTION (16)

The function of the 16 instruction is to advance the paper the number of lines specified by the p5 and p6 digit positions (m address) of the instruction word. The two steps required to execute the instruction are designated PF1 and PF2.

3-53. PF1 STEP. During the PF1 step, the m address stored in register C is transferred to the S lines. The staticized 16 instruction generates FS 41A at t0A and function signals 1, 58+, 63, 30+, and 41 at t0B. Function signal 58+ blocks the normal output gates of register A to clear the S lines, and function signal 63 alerts the output gates of register C to send the m address onto the S lines. Function signals 1 and 30+ have no function during this instruction.

Function signal 41 and STR4 operate step-gate 12 of the static register at t9B to advance to the second step. The gate also requires low $\overline{PR}$ and $\overline{PFI}$ signals which indicate that the preceding print instruction has been completed. Gate 11 is also alerted by FS 41 but the high $\overline{STR4}$ signal blocks it. The operation of gate 12 sets the STR2 flip-flop to change the reading in the static register to 18, initiating the PF2 step.

3-54. PF2 STEP. The new reading in the static register generates FS 42A, which sets the paper-feed interlock flip-flop and blocks step-gate 2 so that only step-gate 1 operates to count down the paper-advance reading to be set up in the print counter. Function signal 42A also generates 58+, 30+, 63, 42B+, and 42 at t0B. Function signals 30+ and 42B+ have no function during this instruction. The p5 and p6 digits of the m address, which specify the number of lines paper is to be advanced, are sent from register C onto the S lines and stored in the flip-flops of the print counter. Function signal 63 continues to alert the output gates to keep the contents of register C reading onto the S lines, and FS 58+ continues to block the contents of register A from reading out onto the S lines.

Function signal 42 generates the CLP signal at t1A to clear the print counter and at t1B alerts the input gates of the first four flip-flops to the p5 digit on the S lines from register C. At t2B, the input gates of the last three flip-flops are alerted to the p6 digit by FS 42. At t3B, FS 42 alerts gate 21 of the static register to generate an ending pulse to clear the 16 instruction. A high RCT4 signal is also generated to restore the CT flip-flop, so that the next instruction word is obtained from storage and staticized.

Function signal 42, still present at t5B even though the 16 instruction is no longer staticized, sets the paper-feed flip-flop to start paper advance.

Each line of paper fed sets the paper-index flip-flop, and the Index signal alerts gate 1 to count down by one the reading in the print counter. When the reading in the counter is one and the last line is advanced, the paper-feed flip-flop is restored to stop advancing paper.

3-55. ABNORMAL OPERATIONS

All abnormal conditions in the printer are controlled by the abnormal-operation flip-flop. This flip-flop sends indications of these conditions to the input-output abnormal-condition flip-flop in the central processor. This section describes the abnormal-operation flip-flop and the conditions which influence it.

3-56. ABNORMAL-OPERATION FLIP-FLOP

The abnormal-operation flip-flop (figure A-35) is alerted if one or more of the following conditions generates a high input to buffer 101:

(1) Printer out of paper (OUT OF PAPER)

(2) Printer out of ribbon (OUT OF RIBBON)

(3) Carriage not in printing position (CARRIAGE OUT)

(4) Processor stopped by operator (STOP SWITCH)

(5) Processor stopped on first execution step of an 11 instruction because the operator has pushed the ONE LINE PRINT button on processor control panel (EPR)

(6) Parity error detected in Remington Rand code read from the print buffer (PBE)

(7) Parity error detected in Remington Rand code read from the code wheel (PCE)

(8) Paper advanced for more than one second (PFE)

(9) Capacitors not charging on second drum revolution (CCF)

(10) Capacitors charging as paper completes advance (CCE)

The input signal is shown in parenthesis.

A low output from buffer 101, indicating the presence of an abnormal condition, and a low SA0 (set abnormal operation) signal make gate 102 permissive, setting the abnormal-operation flip-flop. The SA0 signal (figure A-5) is low when either FS 1A is high, indicating that the processor is on search, or SPA is high, indicating that the processor is stopped (stop flip-flop set).

When the abnormal-operation flip-flop is set, it generates a low AOP signal and sends signals to the printer-off-normal relay, which lights the SYSTEM OFF NORMAL lamp on all three input-output equipments and the PRINTER OFF NORMAL lamp on the central processor panel.

The low AOP signal alerts gate 100 of the input-output abnormal-condition flip-flop (figure A-2). When the next 11 or 16 instruction is staticized, it does not advance to the second step. Under normal conditions, FS 41 alerts gate 11 of the static register at t9B of the first step of the 11 instruction or alerts gate 12 of the static register at t9B of the first step of the 16 instruction. If the AOP signal is present, gate 100, alerted by FS 41, also operates at t9B to set the input-output abnormal-condition flip-flop and generates high Jam I2A and Jam I2B signals at t10B. These signals nullify the effect of gate 11 or gate 12 by jamming the reading for the second step of a test instruction into the static register. The second step of the 11 or 16 instruction is not executed. The Jam I2A and Jam I2B signals transfer the 11 or 16 instruction from register C to register A and cause a search for the c + 1 address instead of the c address. (Refer to section 4-41 of the central processor manual.)

After the condition which set the abnormal-operation flip-flop is corrected, the operator must push the CLEAR button on the printer panel (same as SYSTEM OFF NORMAL light) to erase all effects of the abnormal condition before starting computation.

The ten abnormal conditions are described more fully in the following sections.

3-57. PRINT-BUFFER ERROR

The information read from the print buffer is checked for a parity error during printing when the print flip-flop is set (PR present), after the print buffer is loaded, and when the paper-feed interlock flip-flop is restored ($\overline{\text{PFI}}$ present) after the paper is fully advanced. If a parity error occurs, the print-buffer error flip-flop (figure A-32) is set to generate a high PBE signal. The six bits and the check bit of each character of the print words are read from the buffer on the B lines which are inputs to gates 100 through 111. All of the possible odd combinations of the three bits of the code on the

B1 through B3 lines are sent to input gates 100 through 103. If any one of these gates operates, a high signal is sent to buffers 112 and 113 to alert set-gate 116 and inhibit gate 117. All of the possible odd combinations of the remaining four bits, including the check bit, on the B4 through B7 lines, are sent to input gates 104 through 111. If any one of these gates operates, a high signal is sent to buffers 114 and 115 to alert set-gate 116 and block gate 117. Set-gate 116 operates if two odd combinations occur to indicate a parity error. Set-gate 117 operates if two even combinations occur to indicate a parity error. Both set gates are blocked at t6B and t7B when the space between words and the sign position are read.

The control flip-flop (figure A-32) must be set to ensure that the set gates operate only during the time that one of the characters of the print words is being read. The control flip-flop is set at gate 200 by the Y sentinel, which occurs in the same location as the W1 word, and is restored by the PC13B signal from the W13 word. The PBE signal sets the abnormal-operation flip-flop. The print-buffer error flip-flop is restored by the high ST signal generated when the operator pushes a RUN button to start computation or by the Print CL signal. The setting of the print-buffer error flip-flop lights the PRINT BUFFER lamp on the processor engineering panel.

3-58. PRINT-CODE ERROR

The Remington Rand code for the character read from the printer code wheel is checked for parity errors by the print-code error flip-flop (figure A-32). The six bits of the code for each character, excluding the check bit, are inputs to gate 1 through gate 8 on the CB1 through CB6 lines from the code final-storage flip-flops. All of the possible odd combinations of the three bits on the CB1 through CB3 lines are sent to gates 1 through 4. If any one of these gates operates, a high signal is sent to buffers 9 and 10 to alert gate 13 and block gate 14. All of the possible odd combinations of the remaining three bits, on the CB4 through CB6 lines, are sent to gate 5 through 8. If any one of these gates operates, a high signal is sent to buffers 11 and 12 to alert gate 14 and block gate 13. Gate 13 operates with a low signal from buffer 9, indicating an odd combination in the first three bits, and a low signal from buffer 12, indicating an even combination in the second three bits. Gate 14 operates with a low signal from buffer 11, indicating an odd combination in the second three bits, and a low signal from buffer 10, indicating an even combination in the first three bits. The high outputs from gates 13 and 14 are sent to both buffers 15 and 16.

If either gate 13 or gate 14 operates, buffer 15 operates to alert gate 17 and buffer 16 operates to block gate 18. Gate 17 operates if the six bits of the character form an odd combination (an odd plus an even) and the check bit is a 1 bit

(CB7 signal), comprising an even combination in the seven bits. Gate 18 operates if the six bits of the character form an even combination (two odds or two evens) and the check bit is a 0 bit ($\overline{CB7}$ signal), comprising an even combination in the seven bits. If either gate 17 or gate 18 operates, the print-code error flip-flop is set and a high PCE signal is generated. Both set gates require low PR, $\overline{PFI}$ and PSP signals to operate, indicating that printing is taking place and that an odd sprocket pulse has occurred.

The third set gate of the print-code error flip-flop, gate 24, operates if one or more of the CG1 through CG7 signals is high at the same time that the odd signal is low. This is an indication that a print sprocket signal has been missed or that two have been read instead of one. Under normal conditions, the CG signals are only present when the Even signal is low.

The setting of the print-code error flip-flop lights the PRINTER CODE WHEEL lamp on the processor engineering panel and the CODE WHEEL lamp on the printer panel. The flip-flop is restored by the operation of the CLEAR button (Print CL signal) or the RUN button (ST signal) which starts computation, on the printer panel.

3-59. OUT OF PAPER

A switch is set if no paper is available for printing. The signal generated sets the abnormal-operation flip-flop and lights the NO PAPER lamp on the printer panel.

3-60. OUT OF RIBBON

A switch is set if no ribbon is available. The signal generated sets the abnormal-operation flip-flop and lights the NO RIBBON lamp on the printer panel.

3-61. STOP SWITCH

When the operator presses a STOP button on any of the panels, a Stop Switch signal is generated, setting the abnormal-operation flip-flop and lighting the STOP lamp on all panels.

3-62. ONE LINE PRINT

When the operator presses the ONE LINE PRINT button on the processor operator's panel, an EPR signal is generated to set the abnormal-operation flip-flop, and the computer stops on the first step of the next 11 or 16 instruction. Refer to section 4-43 of the central processor manual.

3-63. CARRIAGE OUT

If the carriage is out of printing position, a switch is set and a signal is generated to set the abnormal-operation flip-flop and light the CARRIAGE OUT lamp on the printer panel.

3-64. PAPER-FEED CHECK

Normally paper should not feed for more than one second. If it continues to feed beyond this time limit, a relay is energized and a signal (PFE) is generated to set the abnormal-operation flip-flop and light the PAPER FEED CHECK lamp on the printer panel.

3-65. CHARGE CHECK FIRE

The charge thyratron is fired to begin the charging of the 130 actuator capacitors when the charge-control flip-flop is set by the STC signal generated on the first drum revolution of the memory-to-print buffer transfer. The charge-check-fire flip-flop is set at gate 112 if the charge thyratron has not yet been fired on the second drum revolution. The gate requires a high Charge signal from the printer and the RC1, $\overline{RC2}$ signals which indicate the second drum revolution. The high CCF signal generated from the set flip-flop sets the abnormal-operation flip-flop, and lights the CHARGE CHECK FIRE lamp on the printer panel. The set-gate is blocked by the IP signal if the NO PRINT button on the operator's panel has been depressed. The flip-flop is restored by operation of the CLEAR button, (Print CL signal) or the RUN button (ST signal) which starts computation, on the printer panel.

3-66. CHARGE CHECK EXTINGUISH

The charge thyratron should be extinguished by restoring the charge-control flip-flop after the paper has fully advanced. If it is not extinguished by the time the Jam 7 delay has been counted down to one, the charge-check-extinguish flip-flop is set at gate 110. The set-gate requires a low Charge signal from the printer, a reading of one in the print counter, a Step signal, and a low PR signal to operate. The high CCEA signal generated from the set flip-flop sets the abnormal-operation flip-flop, and the high CCEB signal inhibits the generation of either the PC or PC' signals so that the thyratrons do not fire while the capacitors are charging. The CHARGE CHECK EXTINGUISH lamp on the printer panel is lit and the charge relay is reset to stop charging the capacitors.

The charge-check-extinguish flip-flop is also set at gate 105 if there is no bias voltage on the control grids of the print thyratrons. The CCEA and CCEB signals are generated and the charge relay is reset.

The flip-flop is restored by operation of the CLEAR button (Print CL signal) or the RUN button (ST signal) which starts computation, on the printer panel.

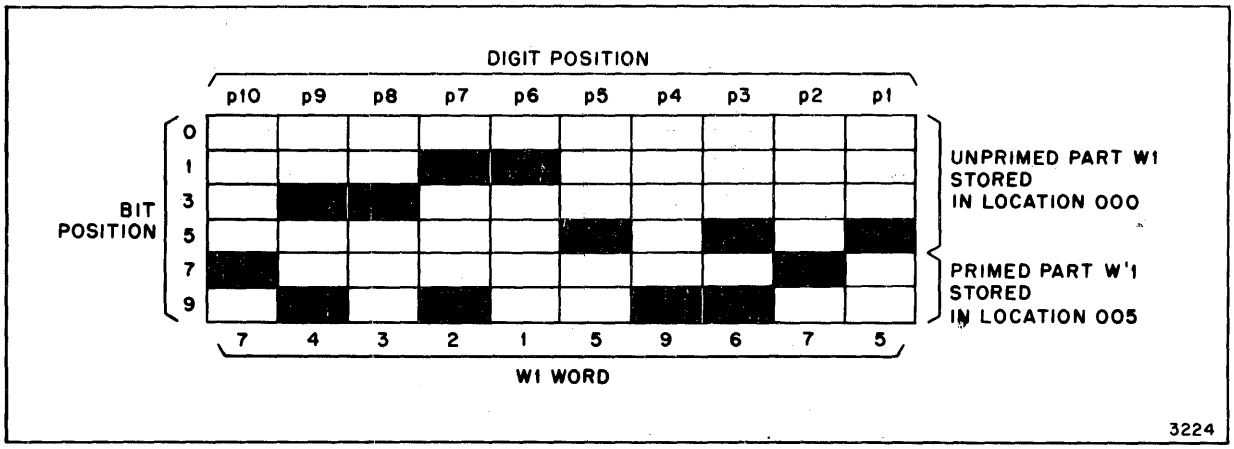


Figure 3-1. Bit Pattern of a Typical Remington-Rand Coded Word

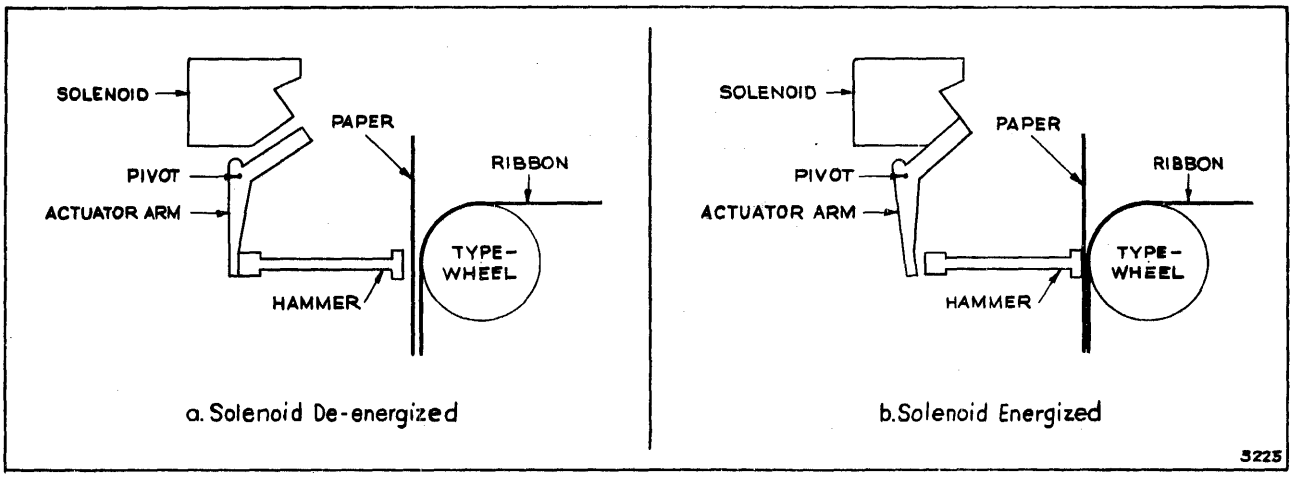


Figure 3-2. Actuator and Hammer Assembly

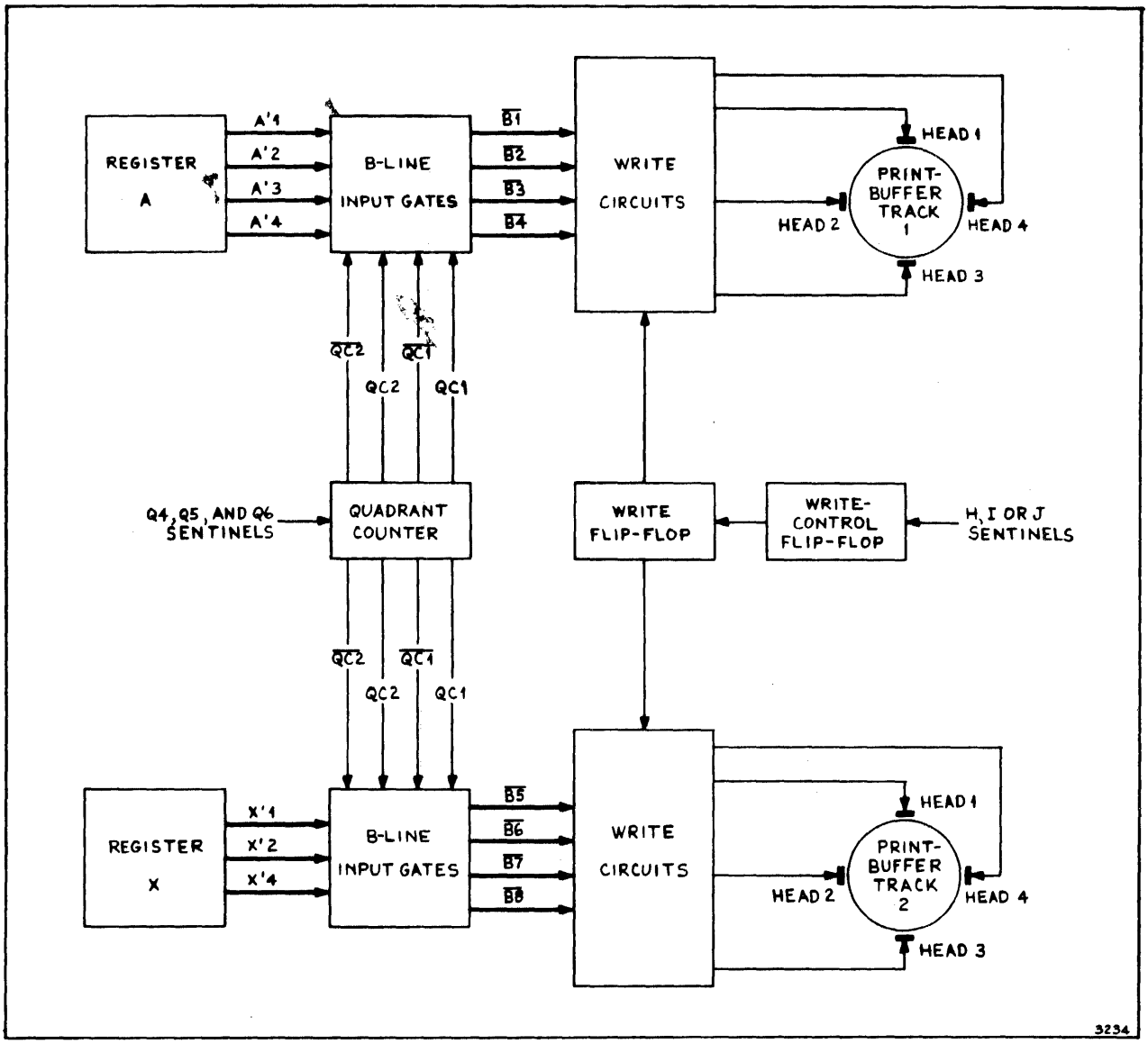


Figure 3-3. Writing in Print-Buffer Tracks

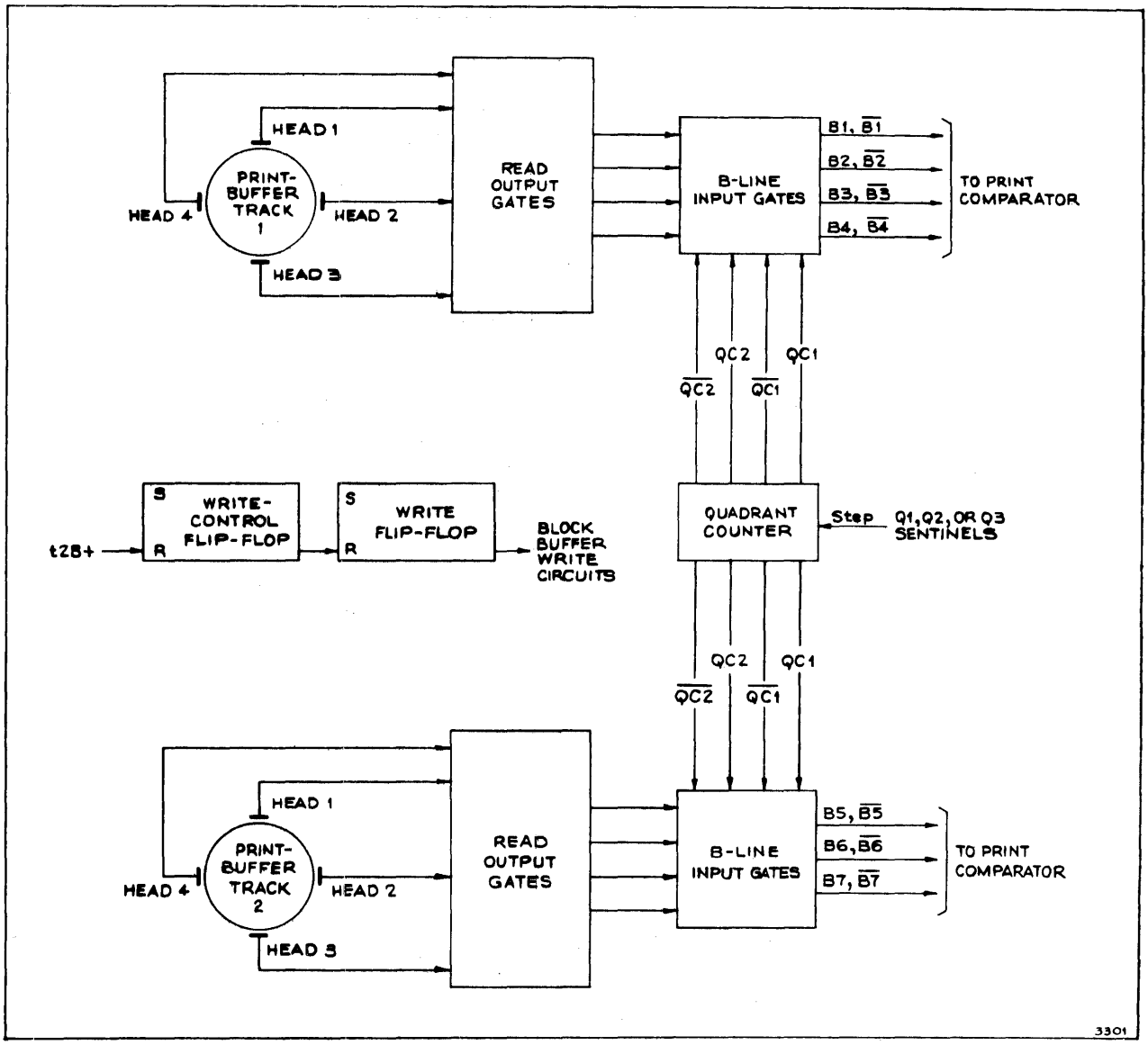


Figure 3-4. Reading from Print-Buffer Tracks

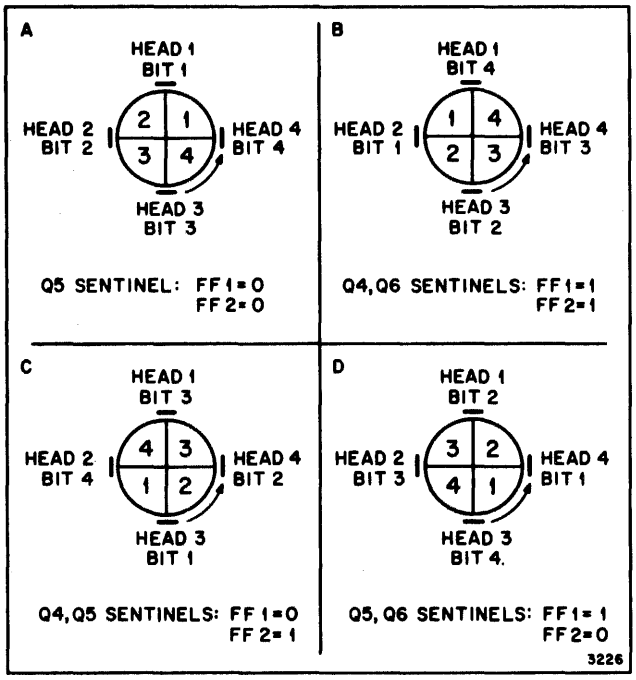


Figure 3-5. Switching of Bits on Track 1 During Writing

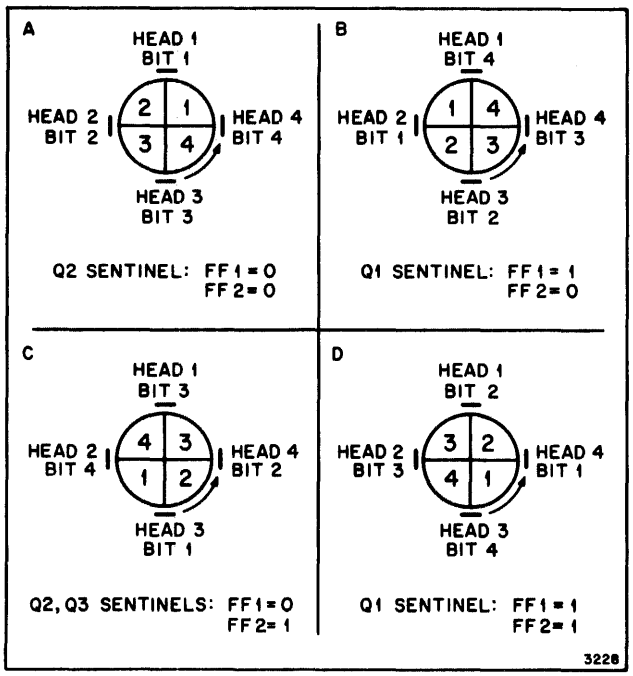


Figure 3-6. Switching of Bits on Track 1 During Reading

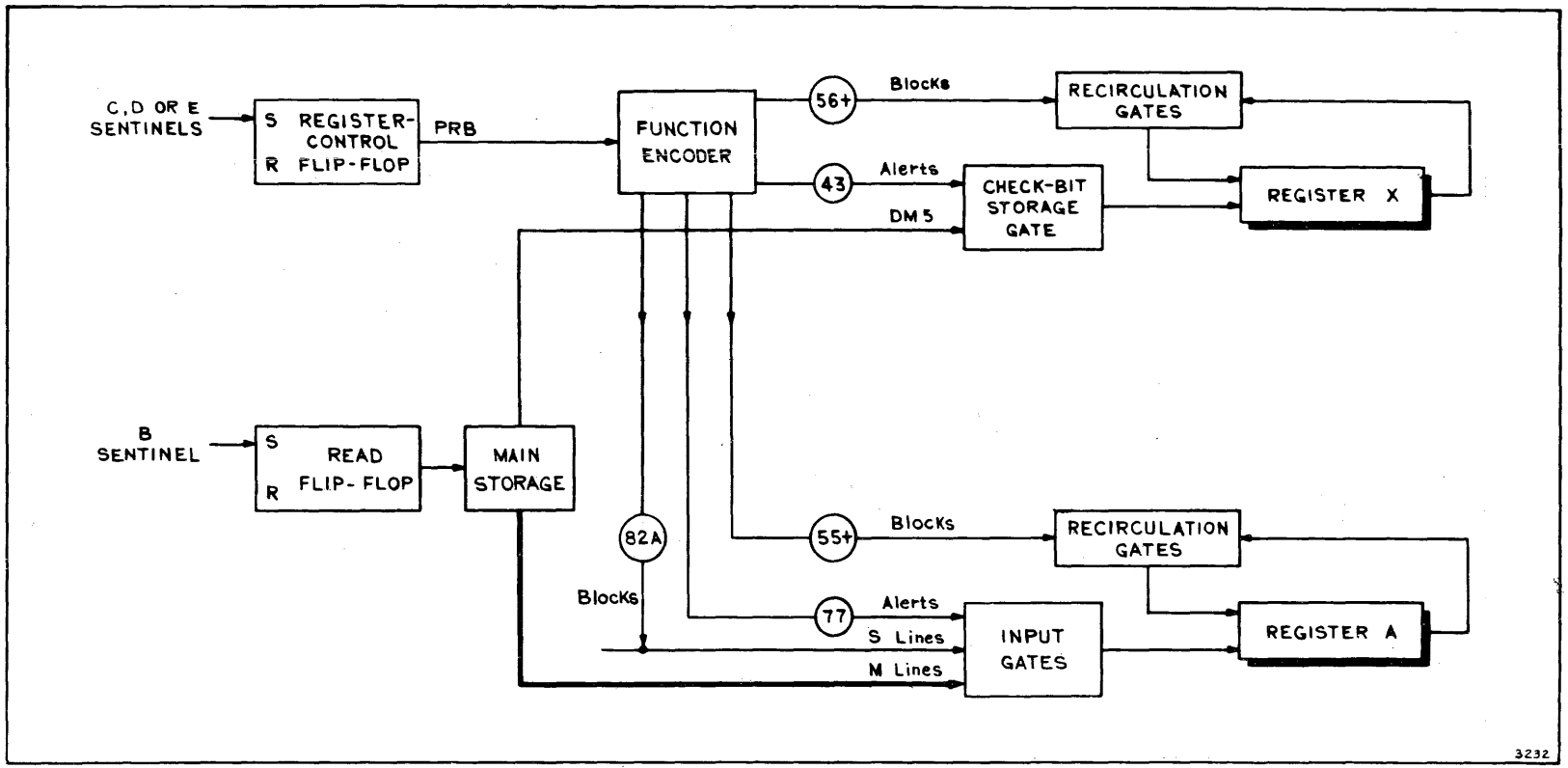


Figure 3-7. Storing Unprimed Word in Register A

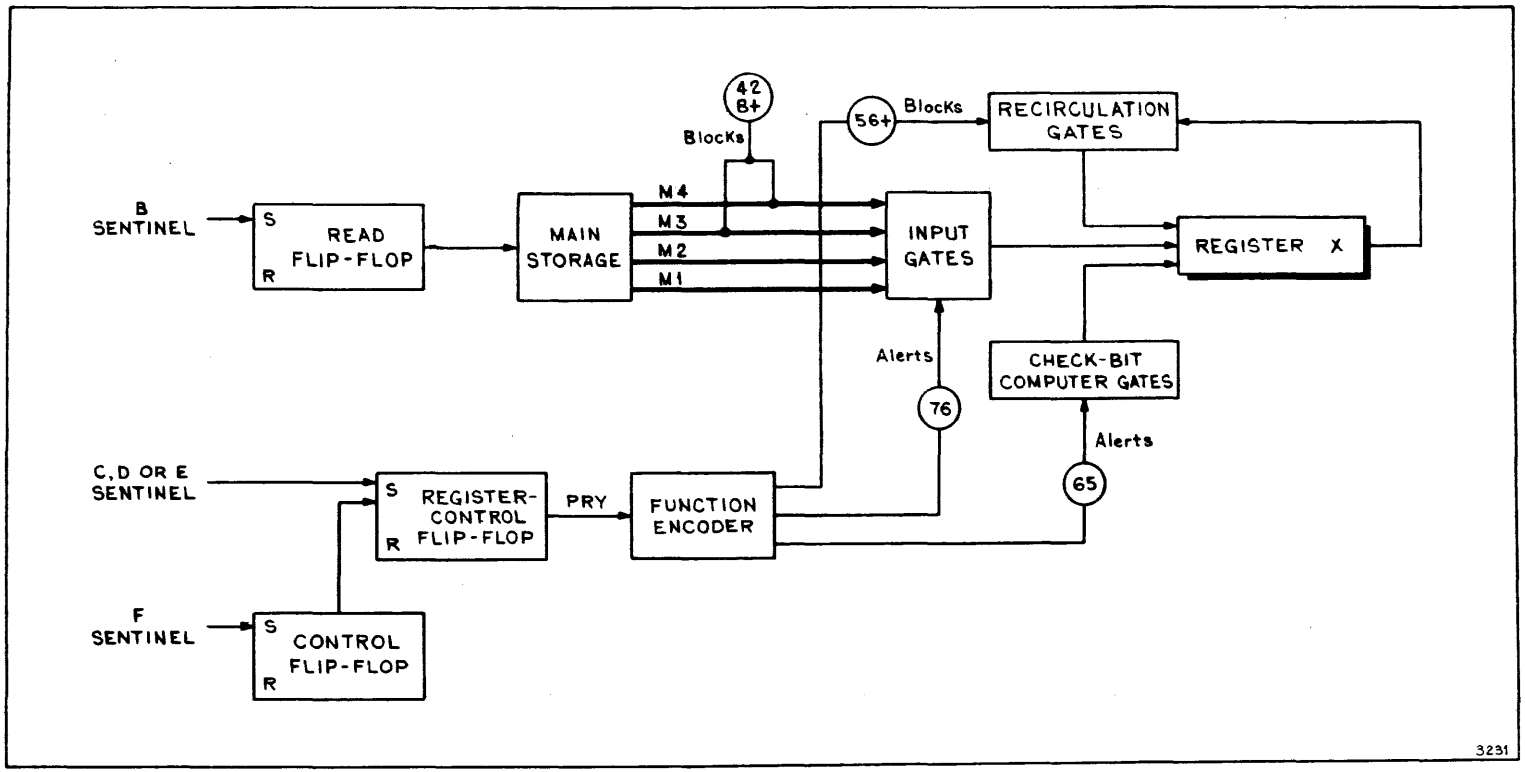


Figure 3-8. Storing Primed Word in Register X

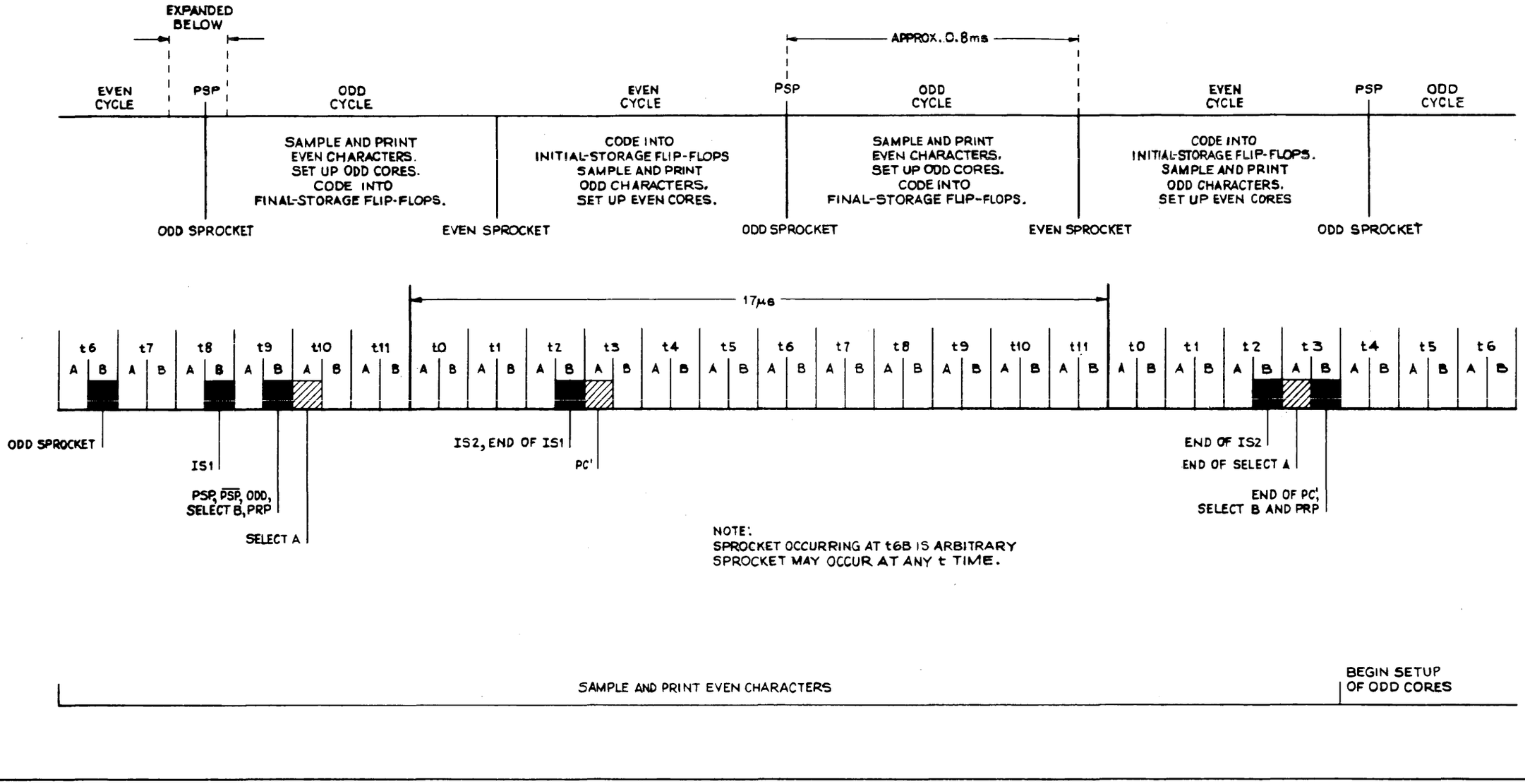


Figure 3-9. Sprocket-Signal Timing

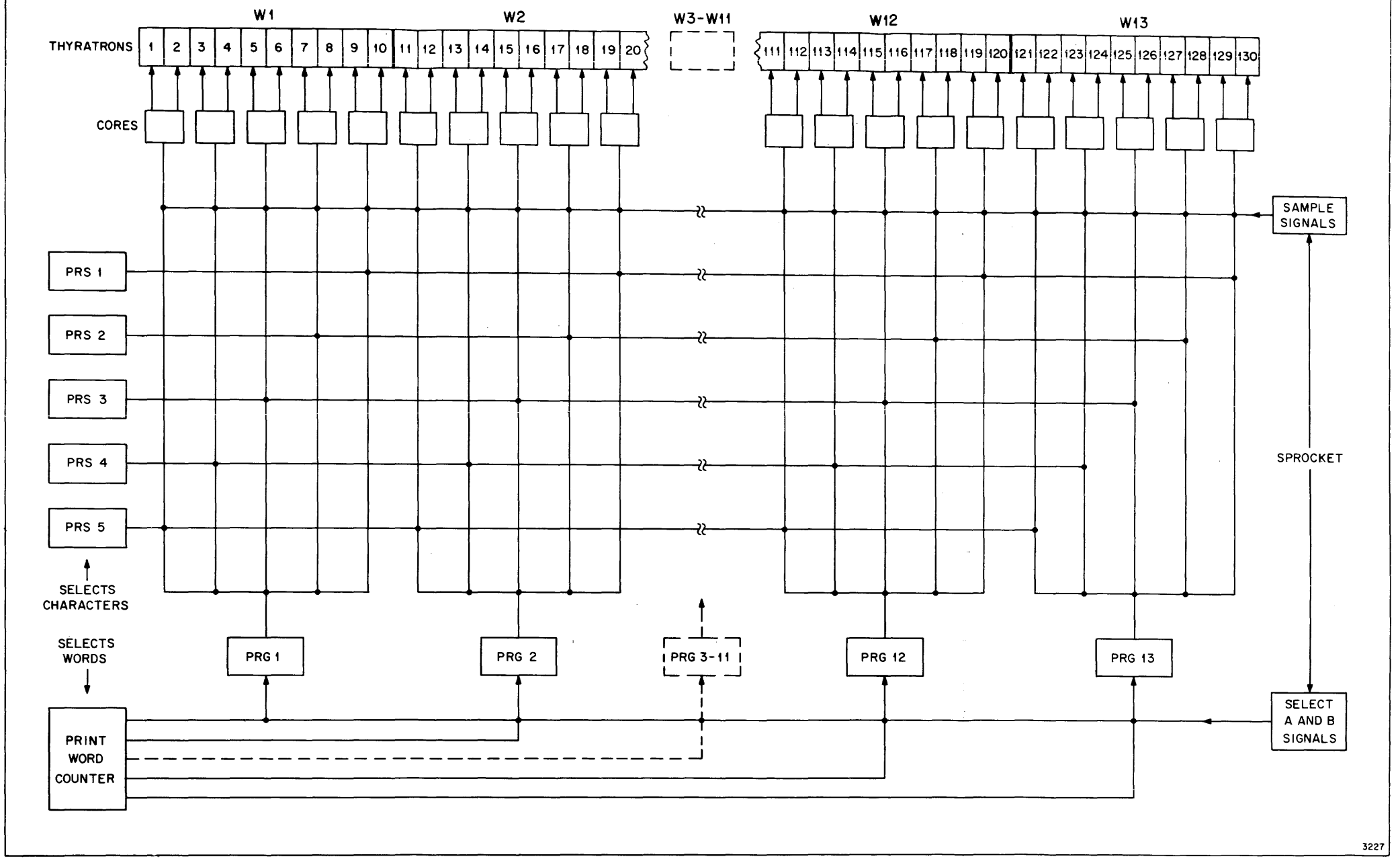


Figure 3-10. Distribution of Set and Sample Signals to Cores

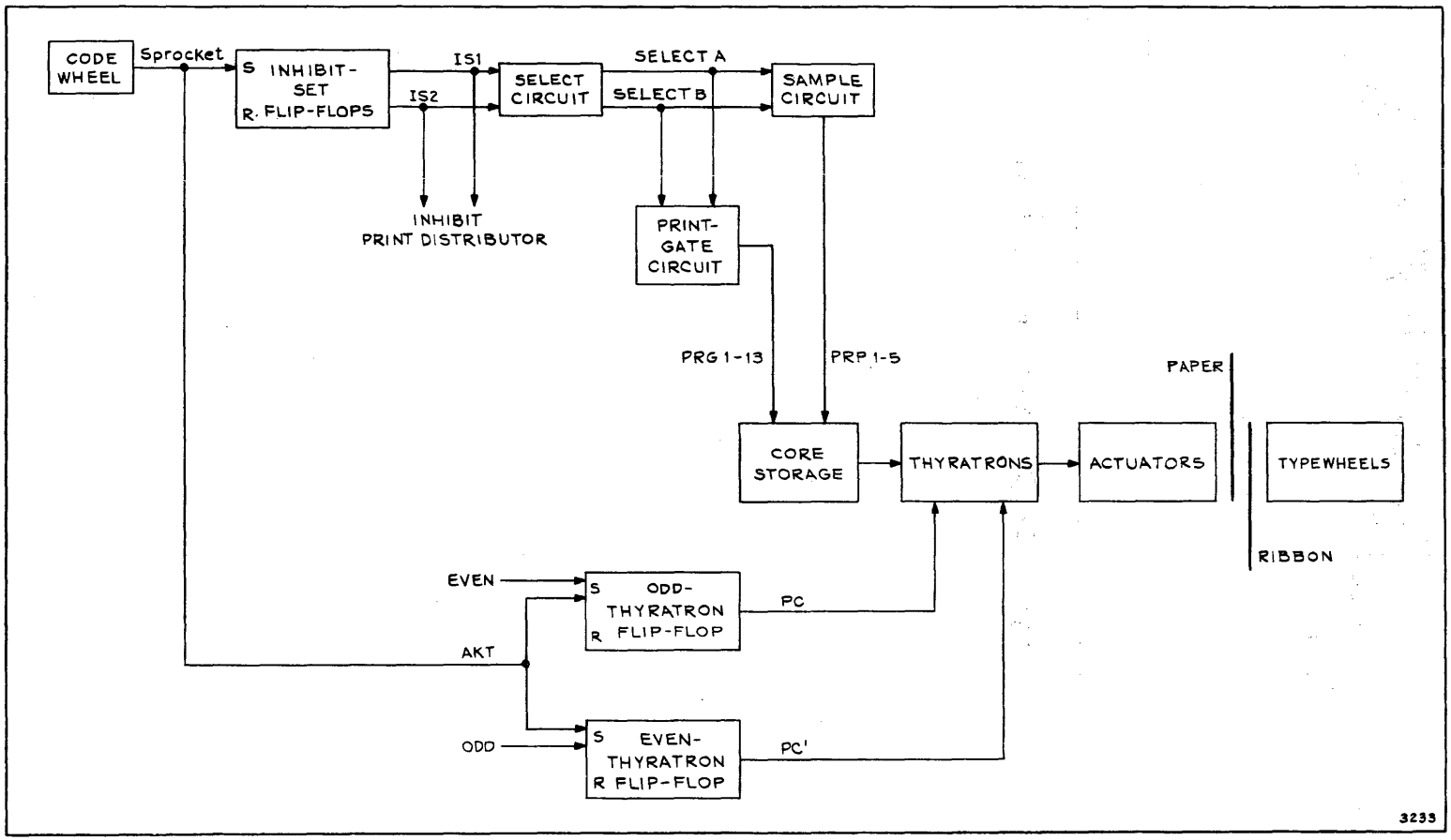


Figure 3-11. Sampling of Cores

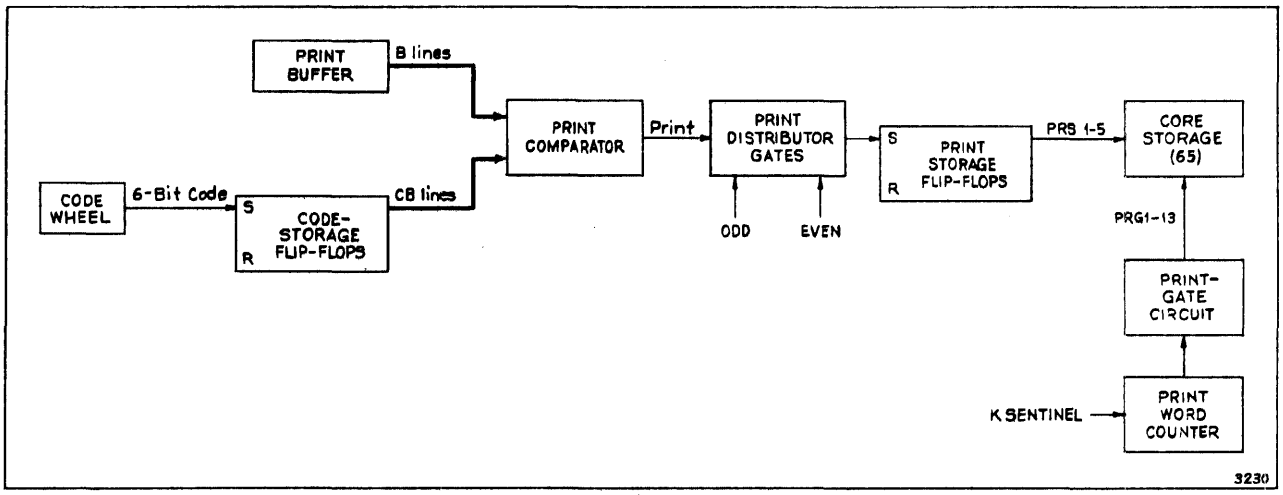


Figure 3-12. Setting of Cores

SECTION IV

CIRCUITRY

4-1. SCOPE

This section contains a detailed description of the theory of operation of the printer circuitry. Many of the printer circuits are the packaged type; several of the packages are shown on separate schematics in this section. Since the operation of much of the circuitry is closely related, several circuits, packaged and unpackaged, are shown on one schematic wiring diagram and explained as a group.

In order to understand the circuit descriptions in this section, a fundamental knowledge of the operation of semiconductor devices is necessary. Such information is contained in section VI of the central processor manual.

In this manual, as in the other New Univac® system manuals, current direction is taken as the direction of electron flow.

4-2. PRINT CIRCUITRY

4-3. GENERAL DESCRIPTION

Printing takes place when one or more of the print actuator coils is energized. One coil is associated with each of the 130 printing positions. The energy used to activate each coil at the correct printing time is supplied by the discharge of a capacitor through a thyratron and the actuator coil connected in series. See figure 4-1. The triggering of the thyratron initiates the capacitor discharge which energizes the actuator coil and causes printing. There is one thyratron for each of the 130 printing positions on a line. To trigger a thyratron, a positive pulse from the core-storage unit must be applied to the control grid at the same time that a positive PC or PC' signal is applied to the shield grid. A positive output signal from the storage unit occurs only after the simultaneous application of the print set and print gate signals to set the core, followed by the simultaneous application of the print sample and print gate signals to read out the storage-unit inputs.

The PC and PC' signals are developed in the PC generators (PCG) and then passed through two stages of amplification: V1 and V2 or V3 and V4. The PC signals are applied to the odd-numbered thyratrons and the PC' signals are applied to the even-numbered thyratrons. Since the PC and PC' signals occur at different times, printing in the odd-numbered positions does not occur at the same time as printing in the even-

numbered positions. Printing only in alternate positions prevents smudging when carbons are used.

The circuitry corresponding to the block diagram of figure 4-1 is shown in the schematic wiring diagram, figure 4-4.

4-4. PC GENERATOR AND AMPLIFIER CIRCUIT. The PCG packages are used to initiate the development of both the PC and the PC' signals, as shown in figure 4-4. When it is desired to print in the odd-numbered printing positions, a PCG package receives both A-phase and B-phase driving signals and develops a positive-going square-wave output. The A-phase and B-phase driving signals are each supplied by a separate transistor amplifier package (TAP), the operation of which is described in section VI of the central processor manual. (For simplicity only the outputs of the TAP packages are shown in figure 4-4.) The output signal is amplified in V1 and V2 and transformer-coupled to the shield grids of all the odd-numbered print thyratrons.

The Q1 emitter potential is normally clamped at +3 volts by a current from the -29-volt supply through R1, CR1, and CR30 to the +3-volt reference level in the TAP. Since the base is held at +6 volts, Q1 is biased for class C operation. Both V1 and V2 are also biased beyond cutoff for class C operation.

When the input signal from the TAP rises above +6 volts, Q1 conducts because of the current through the base and emitter of Q1 and through CR1 to the positive driving potential. Current then flows through R2 and Q1, raising the V1 grid potential from -29 volts to +6 volts. The negative-going V1 output signal is inverted in T1 and applied to the grid of V2 as a positive-going signal. When V2 conducts, the top of the T2 secondary winding goes positive with respect to the bottom and current flows from the -50-volt supply through R27, CR5, the T2 secondary, and C1 to ground. The positive-going PC signal developed across R27 is applied to the shield grid of V5. This positive PC signal is applied to the shield grids of all 65 odd-numbered print thyratrons, but for simplicity only V5 is shown in figure 4-4.

In the event of an open input circuit or removal of the TAP packages, a current through R1 and CR2 clamps the Q1 emitter potential at ground. The protector diode CR2 prevents the reverse bias between the base and emitter of Q1 from exceeding 6 volts. The phase inversion provided by T1 and T2 enables both V1 and V2 to be normally held cut off. If the top of the T1 secondary winding goes negative with respect to the bottom, CR3 conducts and increases the load on the transformer secondary, preventing the transformer from ringing after it is pulsed. The function of CR4 is similar to that of CR3.

The development of the PC' signal which is applied to the 65 even-numbered thyratrons, such as V6, is identical to the development of the PC signal just described.

4-5. PRINT GATE CIRCUIT. Neither a set nor a sample pulse can actuate a core-storage unit unless it is accompanied by a gate signal. Whenever it is desired to apply set or sample pulses to the cores, the print gate (PRG) packages receive both A-phase and B-phase driving signals from the TAP packages and develop negative-going square-wave output signals. The output signals lower the primary-winding centertap potential of the core units, such as T5, enabling the cores to accept either set or sample pulses. See figure 4-4.

The Q4 base potential is normally clamped at +3 volts by the current through R11 and CR12 to the +3-volt reference level in the TAP. Since the emitter is held at +6 volts, Q4 is biased for class C operation. When Q4 is nonconducting, the Q4 collector potential is clamped at +35 volts by the current from the +35-volt supply through CR14 and R12 to the +100-volt supply. The centertap of the T5 primary is also clamped at +35 volts by the current through R13, CR15, and R12.

When the input signal from the TAP rises above +6 volts, current from the +6-volt supply through the emitter and base of Q4 and through CR12 to the positive driving potential causes Q4 to conduct. Current then flows from the +6-volt supply through Q4 and R12 to the +100-volt supply, and the potential at the Q4 collector and T5 centertap falls from +35 volts to +6 volts.

The negative-going gate pulse from each PRG is applied to the centertaps of five core-storage units simultaneously, but for simplicity only one core unit is shown. Since there are 65 core units in the printer and each PRG drives five of them, there are 13 PRG packages in the printer.

In the event the TAP packages are removed, diode CR13 limits the reverse bias on Q4 to a maximum of 6 volts. Capacitors C3 and C4 are both filter capacitors.

4-6. PRINT SET CIRCUIT. When it is desired to print a character in a given printing position, a set pulse accompanied by a gate pulse must be applied to the core-storage unit associated with that printing position. The print set (PRS) package receives both A-phase and B-phase driving signals from the TAP packages and develops a positive-going square-wave output signal. The output (set) signal is used to set the operating point of the core unit at a predetermined position on the hysteresis loop of the core.

Current normally flows from the -29-volt supply through R14 and CR17 to the +3-volt level in the TAP and clamps one side of C5 at +3 volts, as shown in figure 4-4. The other side of C5 and the Q5 emitter are returned to +28.5 volts through R15. Therefore, the net charge on C5 is normally about 25.5 volts. Since the base of Q5 is held at +30 volts, a reverse bias of approximately 1.5 volts keeps Q5 biased off for class C operation. When Q5 is not conducting, a current from the -29-volt supply through R16 and CR20 to ground clamps

the Q5 collector voltage at ground potential. The +35-volt centertap potential keeps CR16 reverse-biased. Therefore, no current flows through the T5 primary at this time.

When the positive input signals from the TAP packages are applied, C5 discharges to approximately 15 volts. Enough of the C5 discharge current to cause Q5 to conduct flows through the base and emitter of Q5 and CR17 to the positive driving potential. Since the gate signal lowers the centertap potential to +6 volts, current flows through R13, half of the T5 primary, CR16, and Q5, and the Q5 collector voltage rises from ground potential to about +30 volts.

When the positive input signals are removed, C5 recharges to 25.5 volts through R14 and CR19. In addition to providing a fast charge path for C5, CR19 quickly restores the Q5 emitter potential to +28.5 volts and limits the peak inverse voltage between the Q5 base and emitter. Diode CR18 prevents the voltage on one side of C5 from going below ground potential, limiting the voltage across C5 to 28.5 volts. Capacitors C6 and C7 are both filter capacitors.

Each of the five PRS packages is used to drive 13 core units, one core at a time. Of the 13 cores connected to a PRS package, only the core which receives a gate pulse with the set pulse is set. Therefore, the maximum load on any PRS at any given time is one core.

4-7. PRINT SAMPLE CIRCUIT. Just before printing, each of the core-storage units receives a sample pulse accompanied by a gate pulse. If a given core has received a set pulse, the sample pulse causes the core to develop an output signal capable of triggering a thyratron. If the core has not been set, the sample pulse does not develop a significant output signal from the core.

Current normally flows from the -29-volt supply through R7 and CR6 to the +3-volt level in the TAP and clamps one side of C2 at +3 volts, as shown in figure 4-4. The other side of C2 and the Q2 emitter are returned to the +28.5-volt supply through R8. Therefore, the net charge on C2 is normally about 25.5 volts. Since the base of Q2 is held at +30 volts, a reverse bias of approximately 1.5 volts keeps Q2 biased off for class C operation. When Q2 is not conducting, a current from the -29-volt supply through R9 and CR9 to the -1.5-volt supply clamps the collector of Q2 and the base of Q3 at -1.5 volts. A current from the -29-volt supply through R10 and CR10 to ground clamps the emitter voltage at ground potential. The +35-volt centertap potential on the T5 primary winding keeps CR11 reverse-biased. Therefore, no current flows through the primary winding at this time.

When the positive input signals from the TAP packages are applied, C2 discharges to approximately 15 volts. Enough of the C2 discharge current to cause Q2 to conduct flows

through the base and emitter of Q2 and CR6 to the positive driving potential. Enough current to cause Q3 to conduct then flows from the -29-volt supply through R10, and the emitter base of Q3, and the collector and emitter of Q2 to the positive driving potential. Since the gate signal lowers the T5 primary centertap potential to +6 volts, when Q3 conducts current flows from the -29-volt supply through R13, half of the T5 primary, CR11, and the emitter and collector of Q3 to the +30-volt supply. This current raises the potential at the emitter of Q3 and the top of T5 to about +30 volts.

When the positive input signals are removed, C2 charges to 25.5 volts very quickly through R7 and CR8. In addition to providing a fast charge path for C2, CR8 quickly restores the Q2 emitter potential to +28.5 volts and limits the peak inverse voltage between the Q5 emitter and base. Diode CR7 prevents the voltage on one side of C2 from falling below ground potential, limiting the voltage across C2 to 28.5 volts.

The sample pulses from each of the five PRP packages are applied to 13 cores simultaneously. Since the PRP packages are more heavily loaded than the PRS packages, the emitter-follower stage Q3 has been added to the PRP to provide the additional current gain required to service the larger load.

4-8. CORE-STORAGE UNIT. Assume that it is desired to print the character C in all 65 odd-numbered print positions. The 13 words and the C's contained in each word are read from the drum serially, although all of the C's must be printed at the same time. The purpose of the core storage is to retain the print information until all 65 C's have been read from the drum and then, when the character C on the typewheels is in printing position, to trigger all of the odd-numbered thyratrons simultaneously.

The storage properties of a core unit are explained with reference to the schematic wiring diagram, figure 4-4, and the core hysteresis loop, figure 4-2. In figure 4-2 the magnetic flux density (B) of the core is plotted against the magnetizing force (H); hence the trace is frequently called a B-H curve.

Assume that the core (T5, figure 4-4) is originally in a state of zero flux density and that a sample and a gate signal are applied simultaneously to the primary winding. The current through the top half of the primary causes the flux density (B) to increase from zero to positive flux saturation ($+B_s$) as indicated by the dashed line on figure 4-2. At the termination of the sample pulse when the magnetizing current decreases to zero, the flux density, or measure of magnetization, is only partially reduced. The residual flux which remains when the magnetizing force is reduced to zero is called remanence and is designated B_r.

If a set and a gate signal are now applied simultaneously to the primary winding, the current through the lower half of the primary causes the flux density to decrease to zero and then build up to negative flux saturation ($-B_s$). During this switching time the operating point of the core traverses the loop from $+B_r$ to $-B_s$. At the termination of the set signal the operating point moves from $-B_s$ to $-B_r$. Upon the simultaneous application of another sample signal and gate signal, the operating point traverses the loop from $-B_r$ to $+B_s$. At the termination of the sample pulse the operating point moves back to $+B_r$.

If another sample signal and gate signal are now applied, before a set signal is applied to move the operating point down to $-B_s$, the operating point of the core moves only from $+B_r$ to $+B_s$. At the termination of the sample pulse, the operating point again moves back to $+B_r$.

During the time in which the core flux density is changing, the magnetic field about the primary winding links the turns of the secondary winding and induces an emf in the secondary. The magnitude of the induced emf is proportional to the rate of flux change ($d\phi/dt$). The flux change is maximum when the core is switching from $-B_r$ to $+B_s$ or from $+B_r$ to $-B_s$; hence, the induced emf is maximum during a switching operation. The polarity of the induced emf depends upon the direction in which the magnetic field is changing or, more specifically, the direction in which the core is switching.

If a set pulse is switching the core from $+B_r$ to $-B_s$, the induced emf is such that the top of the T5 secondary is negative with respect to the bottom. This negative signal reverses the biases of CR25 and CR26 so that effectively the signal terminates at the T5 secondary. If a sample pulse is switching the core from $-B_r$ to $+B_s$, a positive signal is induced in the top of the T5 secondary. The total secondary-winding current is then the sum of the current through R32 and CR26, and the current through R23 and CR25. The positive-going signals developed across R23 and R32 are applied to the control grids of V5 and V6. If either of these thyratrons also receives a PC or a PC' signal at its shield grid, it conducts. The output signal from a core does not cause conduction in a thyratron unless the output signal is accompanied by either a PC or a PC' signal.

If a sample pulse is applied to a core which has not previously been set, the operating point moves from $+B_r$ to $+B_s$ and then back to $+B_r$. While the flux density is building up to $+B_s$, a small positive emf is induced in the T5 secondary. The magnitude of this emf is small because the total flux

change is small. This small signal, although applied to the thyratrons, is insufficient to cause conduction even when accompanied by a PC or a PC' signal and can therefore be neglected.

In summary, a core produces a significant output signal only when the core is switching from $-B_r$ to $+B_s$. This occurs only when a sample pulse is applied to a core which has previously received a set pulse. Idealized waveforms associated with a core are shown in figure 4-3. It is assumed that the set and sample signals are each accompanied by a gate signal. The thyratron triggering potential indicated assumes the presence of a PC or a PC' signal on the shield grid.

4-9. PRINT THYRATRON CIRCUIT. The principal function of the print thyratrons is to provide a fast discharge path for the actuator capacitors through the actuator coils. (See figure 4-4.) When a thyratron is triggered it initiates a capacitor discharge which energizes an actuator coil.

The following fundamental properties of the type 2050 thyratron are presented as an aid to understanding the circuit operation:

(1) The control grid and the shield grid control only the starting of plate current. When both of these grids are driven positive, plate current flows. Once plate current is developed neither of the grids can stop it. The positive gas ions in the tube neutralize any negative charge placed on the grids, rendering the grids ineffective. The only way to stop plate current is to open the plate circuit, or to remove or reverse the plate potential.

(2) Conduction does not stop instantly. Ionization must be stopped first. In the 2050 thyratron, the de-ionization time is approximately 75 microseconds.

(3) The plate current is high and dependent upon the external circuit.

(4) During conduction the voltage drop across the tube is low and independent of the plate current. In the 2050 thyratron, the plate voltage drop is approximately 8 volts.

Plate voltage for the print thyratrons is developed in the following way. While the information to be printed is being transferred to the print-buffer band on the drum, a signal from the charge-control circuit is applied to the T6 primary winding. The induced emf in the T6 secondary winding is of such polarity that a positive-going signal is applied to the V7 grid and a negative-going signal is applied to the V8 control grid. The negative-going signal has no effect on V8. The positive-going signal causes V7 to conduct, completing the circuit for the capacitor-charging current from ground through K4-2, C13, R29, CR28, V7, L3, and K4-1 to the positive supply

voltage. Since the V7 plate voltage drop is approximately 16 volts, C13 charges nearly to full supply voltage.

As the plate current (i_{p7}) of tube V7 increases, the V7 plate voltage (e_{p7}) decreases because of the initial voltage drop across L3 as shown on the accompanying waveforms. The negative-going e_{p7} spike is coupled to the plate terminal of V8 through C15. A small positive-going voltage spike due to ringing among L3, C15, and C19 is also observed at the plate terminal of V8. After V7 turns on and i_{p7} reaches maximum value, i_{p7} decreases exponentially at the same time the actuator capacitors charge. However, i_{p7} does not decrease to zero, because of the current through R45, V9, and V7. After the occurrence of the initial negative-going voltage spike, e_{p7} rapidly rises nearly to full supply voltage because of the small voltage drop across L3 due to the presence of i_{p7}. The inductance of L3 functions primarily as a limiter which regulates the initial surge of i_{p7}.

When the information to be printed is ready for transfer from the buffer band to the printer, the output signal from the charge control circuit is terminated. When this signal is terminated, an electromotive force is induced in the T6 secondary of such polarity that a positive-going signal is applied to the V8 control grid. As i_{p8} increases, e_{p8} decreases nearly to ground (V8 cathode) potential. The negative-going voltage spike of e_{p8} is coupled to the plate terminal of V7 through C15, causing V7 to turn off. Simultaneously, C18 discharges through R43, R50, and V8. The negative-going signal developed across R43 turns off V9, interrupting i_{p7} and insuring that V7 turns off. When V8 turns on, i_{p8} assumes a relatively large amplitude for a period of approximately 1 millisecond. The i_{p8} surge is supplied by C19 which discharges through V8 and R47. The C19 discharge current soon falls below the level required to maintain conduction in V8 and the tube turns off rapidly. The short V8 conduction time is illustrated on the accompanying waveforms by the short duration of i_{p8}. The exponential rise of e_{p8} after V8 turns

off is due to the voltage across C19, which charges exponentially through R49. The C19 charging circuit has a time constant of 180 milliseconds.

The combination of V9 and V12 makes up a bleeder network. When V7 and V8 are off, a current through R45, V9, V12, and K4-2 clamps the cathodes of V7 and V12 at approximately -20 volts. This negative potential holds off Q7 and the CHARGE INDICATOR lamp.

When V7 turns on, V12 turns off and the V7-V12 cathode potential rises far above ground potential, turning on Q7 and the CHARGE INDICATOR lamp. When V8 turns on, V9 is momentarily cut off. Tubes V9 and V12 again conduct and reestablish the -20-volt V7-V12 cathode potential.

As shown in figure 4-4, the charging voltage is applied simultaneously to actuator capacitors C13 and C14. In fact, the charging voltage is applied to the 130 actuator capacitors simultaneously, but for simplicity only two capacitors are shown here, one odd-numbered and one even-numbered.

The a-c plate circuit of print thyratron V5 is from ground through V5, R25, R28-L1, the actuator coil, the charged capacitor C13, and K4-1 to ground. The voltage across C13 serves as the plate supply voltage for V5. Similarly the voltage across C14 serves as the plate supply voltage for V6.

When simultaneous positive signals at the control grid and the shield grid cause V5 to turn on, C13 discharges very quickly through K4-2, V5, R25, R28-L1, and the actuator coil. The C13 discharge current energizes the actuator coil, causing the print hammer to come in contact with the paper. The combination of R25 and R28-L1 is a peak-current limiter in the capacitor discharge circuit.

To prevent smudging when several carbon copies are printed, the hammers are actuated with increased energy. This is accomplished by increasing the potential developed across the actuator capacitors and, therefore, the magnitude of the capacitor discharge current. The potential developed across

he capacitors may be varied by adjusting the PRINTER DENSITY switch on the T7 primary winding.

The actuator capacitors retain their charge even when power is disconnected from the printer. When the power is disconnected, however, the bias voltages applied to the print thyratrons are reduced to zero. With the bias removed and the plate supply voltage maintained, the print thyratrons would normally conduct and cause extraneous printing. To prevent extraneous printing, K4 is deenergized and the K4-2 contacts open when power is disconnected from the printer. The actuator capacitors then discharge very slowly through R30 and the print hammers are not actuated.

Current normally flows through CR33 and R54, clamping the Q7 output terminal at +16 volts. Current also flows through R55 and CR31, clamping the Q7 base below ground potential to reverse the bias of this stage. When V7 turns on and the actuator capacitors begin charging, a current through the emitter and base of Q7, R53, and V7 causes Q7 to turn on. Current then flows through the emitter and collector of Q7, L5, CR32, and R54. Diode CR33 turns off and a negative-going Q7 output signal is developed. If, due to some abnormal condition, the actuator capacitors fail to charge or Q7 does not turn on, the +16-volt Q7 output signal stops the printer.

When V7 turns on and the V7 cathode voltage rises above ground potential, current flows through the CHARGE INDICATOR lamp and R52. The illumination of the CHARGE INDICATOR lamp is a visual indication that the actuator capacitors are being charged.

Capacitors C8 and C9 prevent noise impulses from triggering print thyratron V5. The 400-microfarad capacitors in the actuator-capacitor reservoir help maintain the line voltage while the actuator capacitors are charging.

4-10. PAPER-FEED CIRCUIT

Either the brake coil or the clutch coil is energized while the printer is in operation. When paper is not advancing through the printer, the brake coil is energized through V3 (figure 4-5), and the clutch coil is deenergized. Tubes V1 and V9 also conduct, as shown. When paper is advancing, the clutch coil is energized through V2 and the brake coil is deenergized. After the correct amount of paper has been advanced, the circuit reverts to its original state.

Assume that at the end of a print operation it is desired to advance the paper to the next line. A signal from the paper-feed flip-flop is applied to the T1 primary winding. The induced emf in the T1 secondary is of such polarity that a positive-going pulse is applied to the V2 control grid. When V2 conducts, current flows from ground through V2, L1 and C17, R17, the K2-1 normally closed contacts, the clutch coil, R13, and R12 to the +600-volt supply. The negative-going V2 plate signal is coupled to the plate of V3 through C6 and R23. This signal turns off V3, the clutch coil is energized, and the brake coil is deenergized.

Until V2 turns on, a small current is maintained from ground through R6, R8, CR2, R17, the K2-1 normally closed contacts, the clutch coil, R13, and R12 to the +600-volt supply. This current is not of sufficient amplitude to actuate the clutch but the voltage drop developed across R6 is sufficient to keep V1 conducting. When V1 conducts, the V1 plate voltage is low and the voltage across K2 is not sufficient to energize the relay. When V1 is on, it effectively shorts K2. When V1 turns off, current flows from the +45-volt supply through K2 and R2 to the +300-volt supply, and the K2-1

contacts open the V2 plate circuit. When V2 turns on, and the V2 plate voltage decreases, CR2 turns off and C4 starts discharging through R6 and R7. If V2 is not turned off before C4 discharges, V1 turns off, energizing K2 and opening the K2-1 normally closed contacts in the V2 plate circuit. Tube V1 turns off about one second after V2 turns on. If some abnormal condition holds V2 on too long, the K2-1 normally closed contacts open one second after V2 turns on, deenergizing the clutch and preventing the paper from advancing more than a few pages. If V2 is on for less than one second, V1 remains on and the K2-1 contacts remain closed.

Current normally flows through R45 and CR5, clamping the PFE output at ground potential. When K2 is energized, the K2-3 contacts switch and current flows through the PAPER FEED ERROR lamp, R44, R43, and K2-3. Diode CR5 turns off and a positive-going PFE signal is developed which stops the computer. The PAPER FEED ERROR lamp provides a visual indication of the cause of the shutdown.

The GENERAL CLEAR switch must be pressed before the computer will start again. The general clear signal energizes K11, causing the K11-2 contacts to change their position. The change of position puts both ends of K2 at +45 volts, deenergizing the relay. When the K2-1 contacts close, the circuit is again completed through R6, R8, CR2, R17, K2-1, the clutch coil, R13, and R12, putting a positive potential on the V1 control grid. At the termination of the general clear signal the K11-2 contacts open and current flows through V1 and K2 in parallel, and R2. Because of the positive V1 grid potential, the tube current increases much more rapidly than the relay current and again V1 effectively shorts out K2.

At the same time that the positive-going signal is applied to the V2 control grid a positive-going signal is also applied to the V7 grid. Tube V6 prevents this signal from rising above ground potential but, since the V7 cathode is normally clamped at ground potential through CR4, the positive-going grid signal is sufficient to turn on V7. The negative-going V7 plate signal is coupled to the V9 grid through C15 and R41. As V9 turns off, the positive-going V9 plate signal is coupled directly to the grids of both V5 and V8, turning both tubes on. Capacitor C15 continues charging through V8, R40, and R38. When C15 becomes charged, the negative signal across R40 no longer develops and V9 turns on. When V9 turns on, the negative-going V9 plate signal turns off V5 and V8. When the V5 plate voltage rises, C13 charges through R30, placing a positive signal on the V4 control grid. Current then flows from ground through C9, V4, R27, and R12 to the +600-volt supply until C9 charges. When C9 becomes charged, the voltage between the cathode and plate of V4 is insufficient to maintain ionization and V4 turns off.

The triggering of V4 is delayed approximately 750 microseconds by the V8-V9 delay-flop to provide sufficient time for V3 to turn off. Should both V3 and V4 be on together, V4

would effectively short out R14 and permit the current through both tubes and the brake coil to become excessively high.

When the paper has advanced to the next line, a positive-going signal from the paper-feed flip-flop is applied to the V3 control grid. To maintain uniform spacing among the printing lines, it is essential that the brake be actuated rapidly and positively. To satisfy this requirement, C9 supplies a surge current through the brake coil when V3 initially conducts. The surge current flows from C9 through V3, R25, and the brake coil to C9. The normal brake current flows from ground through V3, R25, and brake coil, R14, and R12 to the +600-volt supply.

When V3 conducts, the V3 plate voltage decreases to near ground potential. This negative-going signal is coupled to the plate of V4 through C8 and L1 to insure that V4 is off when V3 is on. The negative-going V3 plate signal is also coupled to the plate of V2 through C6 and R23. The V3 plate signal extinguishes V2 and deenergizes the clutch coil.

When V3 is on and the brake coil energized, the V3 plate voltage is near ground potential. The voltage across NE3 and R24 is not sufficient to support ionization in NE3 so NE3 does not glow. When V3 is off and the brake coil deenergized, the V3 plate voltage is approximately 600 volts. Neon NE3 conducts and a small current flows from ground through NE3, R24, R25, the brake coil, R14, and R12 to the +600-volt supply. The operation of NE2 is similar to that of NE3. When the clutch is energized, NE2 is off and NE3 is on. When the brake is energized, NE2 is on and NE3 is off. The two glow tubes provide a visual indication of the present state of the circuit.

When V1 is on (K2 deenergized), the V1 plate voltage is too low to support ionization in NE1 and this tube does not glow. When V1 turns off (K2 energized), NE1 conducts and current flows from the +45-volt supply through NE1, R3, and R2 to the +300-volt supply. Neon NE1 is on when K2 is energized and off when K2 is deenergized.

When power is applied to the printer, the development of the +600-volt potential is delayed approximately 5 seconds. This provides ample time for the bias voltages to develop before the application of plate voltages and prevents undesired paper spacing or other erratic operation.

Capacitor C10 provides the initial current through the clutch coil when V2 is turned on. Capacitor C16 keeps the +600-volt level relatively stable under varying load conditions.

4-11. PAPER-FEED-DRUM AMPLIFIER CIRCUIT

Every time the paper advances one line the paper-space index drum rotates 60 degrees. Since there are six magnetized areas at 60-degree intervals along the surface of the drum, one of these magnetized areas passes under the head when the paper advances one line. The signal which is induced in the head-winding is amplified and shaped in the paper-feed-drum amplifier (PFDA) circuit and then applied to the paper-space-index flip-flop. See figure 4-6.

When the PFDA is in the normal nondriven state, Q1, Q2, Q3, and Q5 are turned on because of the application of forward bias. The output current through CR2 and R9 is clamped at slightly over +16 volts. When a magnetized area passes under the head, the waveshape of the emf induced in the head-winding approaches that of one cycle of a sinusoid. The induced emf is transformer-coupled to the Q1 input circuit by T1, which also matches the head impedance to the Q1 input impedance. No phase inversion takes place in a common-base transistor amplifier stage. The Q1 output signal is an amplified replica of the input signal. The Q1 output is transformer-coupled to the Q2 input circuit and the Q2 output is transformer-coupled to the Q3 input circuit. Both T2 and T3 are stepdown transformers and, since the secondary current is greater than the primary current, they can be considered as current amplifiers.

Transistor Q2 can be considered a coupling device between two current amplifiers, T2 and T3. A simplified example which does not take transformer losses into account illustrate this point. Assume that an alternating current I flows through the Q1 input circuit. The T2 primary and Q1 collector current is then $\alpha_1 I$, where α_1 is the current-gain factor of Q1. Since T2 is an M:1 stepdown transformer, the T2 secondary and Q2 input current is $M(\alpha_1 I)$. The T3 primary and Q2 collector current is $\alpha_2 (M\alpha_1 I)$, where α_2 is the current gain factor of Q2. Since T3 is an N:1 stepdown transformer, the T3 secondary and Q3 input current is $N(M\alpha_1\alpha_2 I)$. The Q3 collector current is then $\alpha_3(MN\alpha_1\alpha_2 I)$, where α_3 is the current-gain factor of Q3. Since α_1, α_2, and α_3 are all very nearly equal to 1, the Q3 collector current is only slightly less than MNI. The Q3 output current is much greater than the Q1 input current.

The negative alternation of the Q3 output signal must appear before the positive alternation to charge C6 sufficiently to discharge through Q4. During the negative alternation, C6 charges through R4, CR1 and R8. During the positive alternation, enough of the C6 discharge current to turn on Q4 flows from ground through the emitter and base of Q4, C6, the collector and emitter of Q3, the T3 secondary winding, and C5 to ground. When Q4 turns on, C9 discharges from approximately 11 volts through Q4 and R7, developing a negative-going signal on the base of Q5. As Q5 turns off, the Q5 collector voltage

goes positive, CR1 turns on, and current flows from ground through the emitter and base of Q4, CR1, and R8 to the +10-volt supply. This feedback signal holds Q4 on until C9 discharges and Q5 turns on again. While Q5 is off and the Q5 collector voltage is positive, current flows from ground through the emitter and base of Q6 and R8 to the +10-volt supply. When Q6 turns on, current flows from ground through the emitter and collector of Q6 and R9 to the +45-volt supply. Diode CR2 turns off and the Q6 collector voltage (PFDA output) drops from +16 volts to ground potential. The duration of the negative-going output signal is determined by the length of time Q5 is off, which in turn is determined by the time required for C9 to discharge.

4-12. PRINT-DRUM READ-AMPLIFIER CIRCUIT

There is one print-drum read-amplifier (PDR) package for each of the seven tracks on the code wheel. The pulses induced in the head windings by the permanently recorded signals on the code wheel are amplified and shaped in the PDR packages and applied to the initial-storage flip flops. The waveshape of each signal induced in the head windings resembles the shape of one cycle of a sinusoid.

A PDR package is shown in figure 4-7. When the PDR circuit is in the normal nondriven state, Q1 and Q2 are turned on because of the application of forward bias. The PDR output voltage is clamped at +16 volts by the current from the +16-volt supply through CR2 and R8 to the +45-volt supply. The movable arm on R4 is clamped at ground potential by a current through CR1 and R5.

Signals induced in the head windings are transformer-coupled to the Q1 input circuit by T1 which is also an impedance-matching device. The Q1 output signal is then transformer-coupled to the Q2 input circuit. Both Q1 and Q2 are operated as conventional common-base class-A amplifiers. The phase of the Q2 output signal is shown in figure 4-7. During the first alternation of the Q2 output signal, C5 discharges almost to zero volts through CR1, R4, Q2, the T2 secondary winding, and C4. During the second alternation of the Q2 output signal, enough of the C5 charging current to turn on Q3 flows from the -10-volt supply through R3, C5, and the base and emitter of Q3 to ground.

The value of the C5 charging current, and hence the drive on Q3, depends upon the level to which C5 discharges on the first alternation. The more C5 discharges on the first alternation the greater the current required to charge C5 on the second alternation. Since C5 discharges through R4, moving the sliding contact on R4 upward decreases the time constant of the C5 discharge circuit and permits C5 to discharge to a lower level in the same increment of time. As the sliding contact moves upward the drive on Q3 increases.

When Q3 and Q4 are off, C6 charges to approximately 8.5 volts through R6 and CR3. When Q3 turns on, C6 discharges to about zero volts. Enough of the C6 discharge current to turn on Q4 flows from ground through the emitter and base of Q4, C6, and the collector and emitter of Q3 to ground. When Q4 turns on, CR2 turns off and the Q3 collector voltage (PDR output voltage) falls to ground potential.

Capacitors C1 and C4 are a-c bypass capacitors and C2, C3, C7, and C8 are filter capacitors.

4-13. PRINT-DRUM SPROCKET-AMPLIFIER CIRCUIT

During each revolution of the code wheel, each of the 102 permanently recorded signals on the sprocket track induces an emf in the head-windings. The waveshape of each of these induced signals approaches the shape of one cycle of a sinusoid. These signals are amplified and shaped in the print-drum sprocket-amplifier (PDSA) circuit and used in the generation of timing signals in the printer.

The PDSA circuit is shown in figure 4-8. When the PDSA is in the normal nondriven state, Q1 and Q2 are turned on because of the application of forward bias. Transistors Q1 and Q2 are operated class A, and Q3 and Q4 are operated class B. Signals induced in the head-windings are transformer-coupled to the Q1 input circuit, and the Q1 output signal is transformer-coupled to the Q2 input circuit. Both Q1 and Q2 are operated as conventional transformer-coupled common-base amplifier circuits. Transformer T3 is a coupling transformer and phase splitter which provides input signals to Q3 and Q4 equal in amplitude but opposite in phase.

The Q3-Q4 output circuit is designed to amplify the sprocket signals but suppress any random noise induced in the head windings. The output windings N1, N2, and N3 are wound on a toroidal core of magnetic material which exhibits a relatively square hysteresis loop similar to the one shown in figure 4-2. For correct operation of the PDSA, the phase of the input signals to Q3 and Q4 must be as shown in figure 4-8. During the first alternation of the input signal, Q3 remains off and Q4 turns on. Current then flows from the -10-volt supply through R3, N2, Q4, and the lower half of the T3 secondary winding to ground. Current in this direction drives the operating point of the core to $-B_s$ as shown in figure 4-2. When the driving signal is cut off, the operating point moves back to $-B_r$. During the second alternation of the input signal Q4 remains off and Q3 turns on. Current then flows from the -10-volt supply through N1, Q3, and the upper half of the T3 secondary winding to ground. This current drives the operating point of the core to $+B_s$. When this driving signal is cut off, the operating point moves back to $+B_r$.

The core requires a specific number of volt-seconds to switch from remanence to saturation. It is best analyzed as a voltage-operated device. For any given core the voltage-time (ET) product is a constant determined by the total number of flux linkages of the core. Regardless of the waveform of the applied voltage, the integral of voltage and time must equal the ET of the given core to switch that core. For this core ET is approximately 40 volt-microseconds.

Since ET is a constant, the time required for a switching operation is inversely proportional to the applied voltage. Because of the voltage drop across R3, the voltage across N2 when the core is switching to $-B_s$ is less than the voltage across N1 when the core is switching to $+B_s$. The time required to switch the core to $-B_s$ is, therefore greater than the time required to switch the core to $+B_s$. The flux change $d\phi/dt$ is greater when the core is switching to $+B_s$. Since the emf induced in N3 is proportional to $d\phi/dt$, the induced emf in N3 is maximum when the core is switching to $+B_s$. During the first alternation of the input signal, when the core is slowly switching to $-B_s$, the induced emf in N3 rises very slowly. During the second alternation of the input signal, when the core is rapidly switching to $+B_s$, a negative-going voltage spike of large amplitude is induced in N3. To develop this output signal, which is the required one, the core must always be reset to $+B_r$.

Most noise pulses induced in the head windings have a symmetrical waveshape. If the operating point of the core is at $+B_r$ when the noise pulse is received, the first alternation of the signal drives the core toward $-B_s$. Since Q3 has a greater gain than Q4, the core is driven past $+B_r$ on the second alternation of the noise pulse. This insures that the operating point of the core is always at $+B_r$ when a sprocket signal is induced in the head windings. The circuit, therefore, remains relatively unaffected by noise.

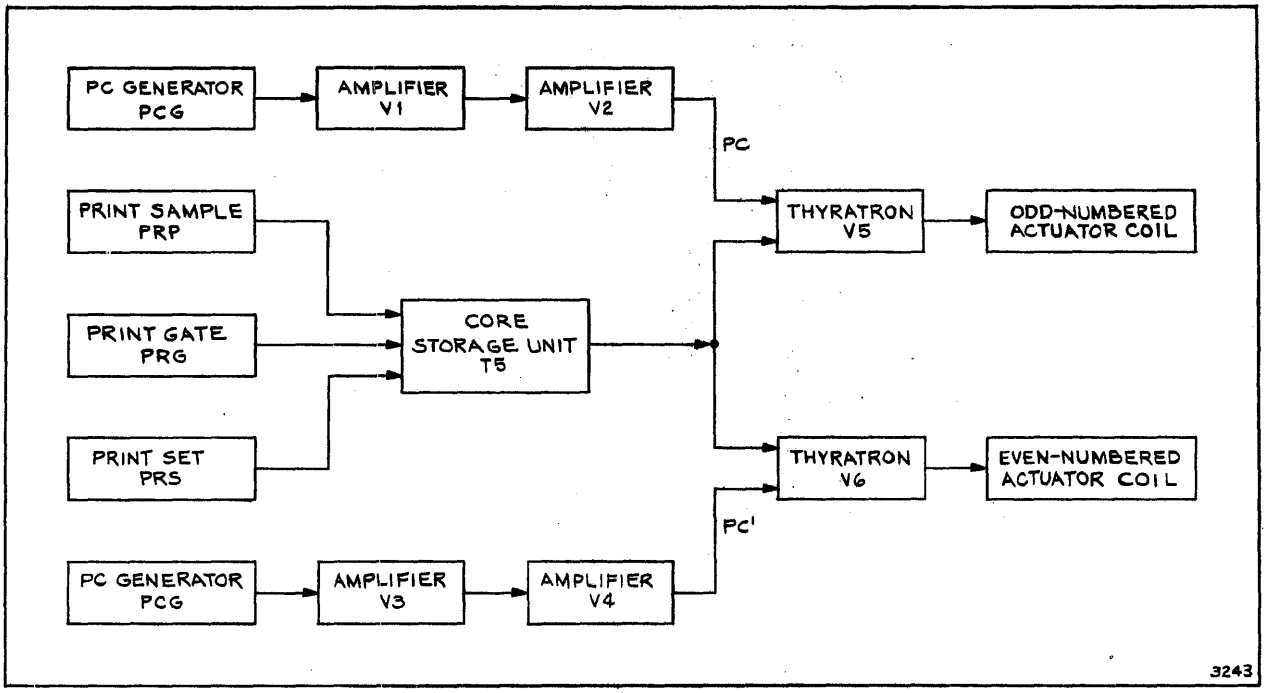


Figure 4-1. Print Circuitry, Block Diagram

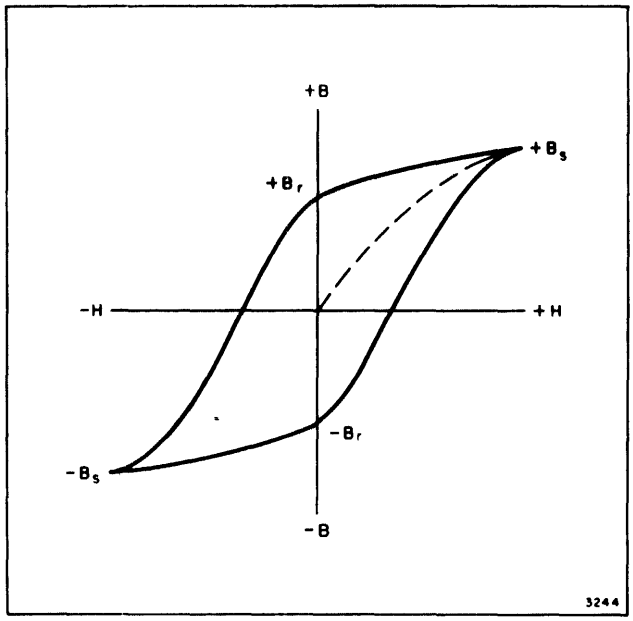


Figure 4-2. Core Hysteresis Loop

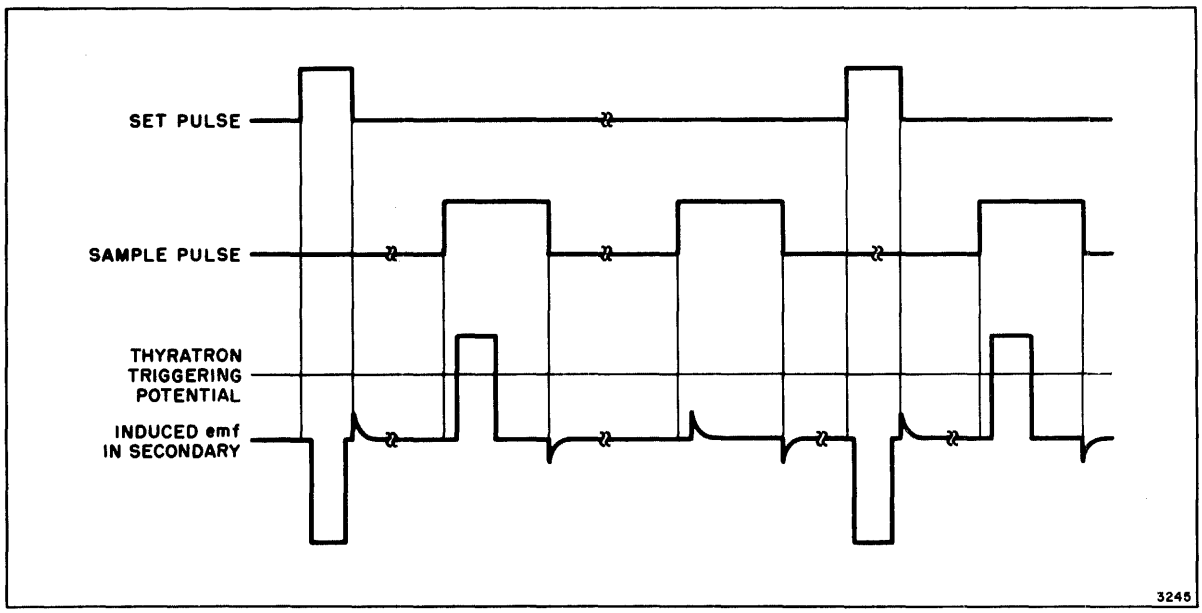
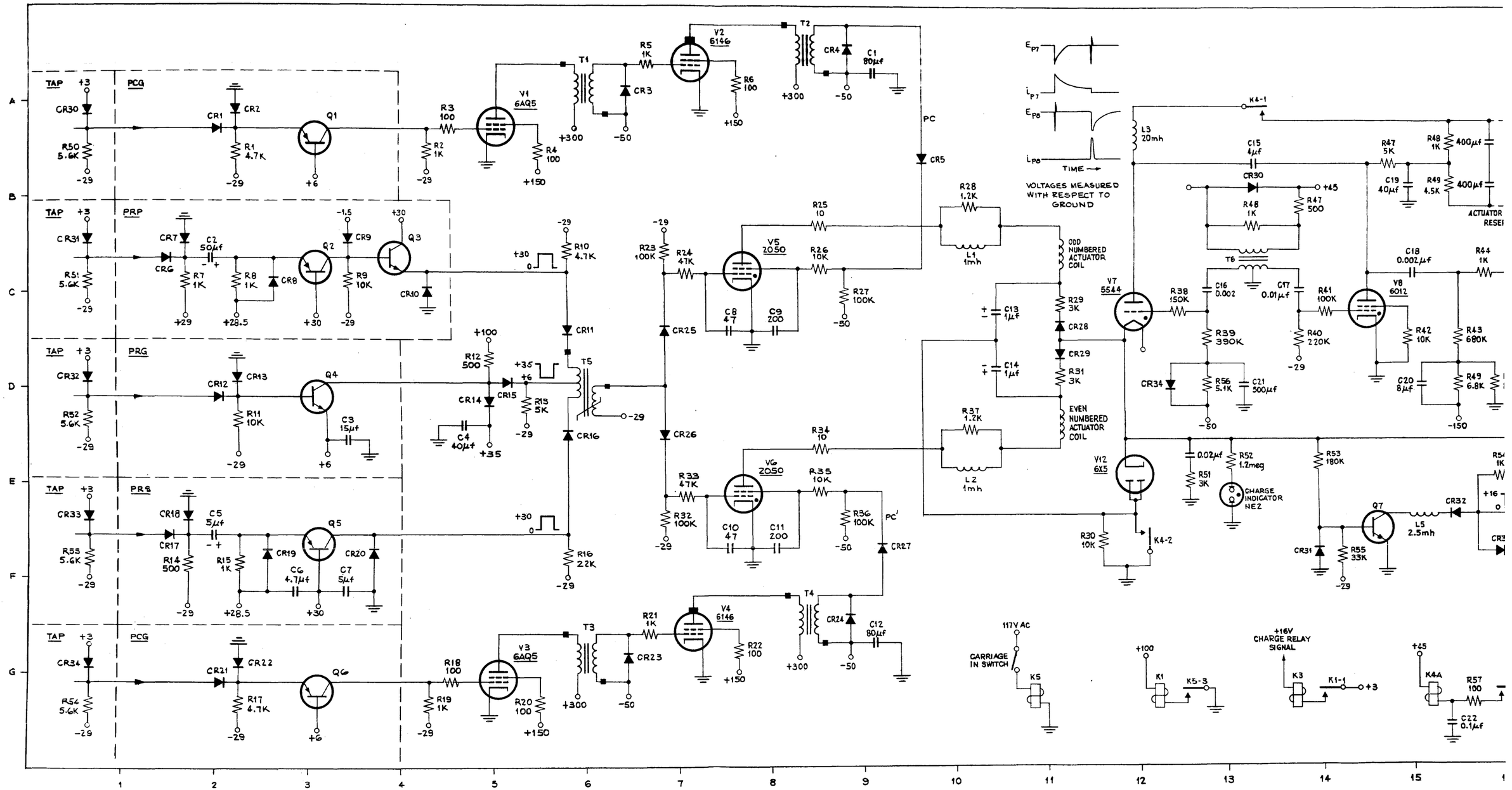
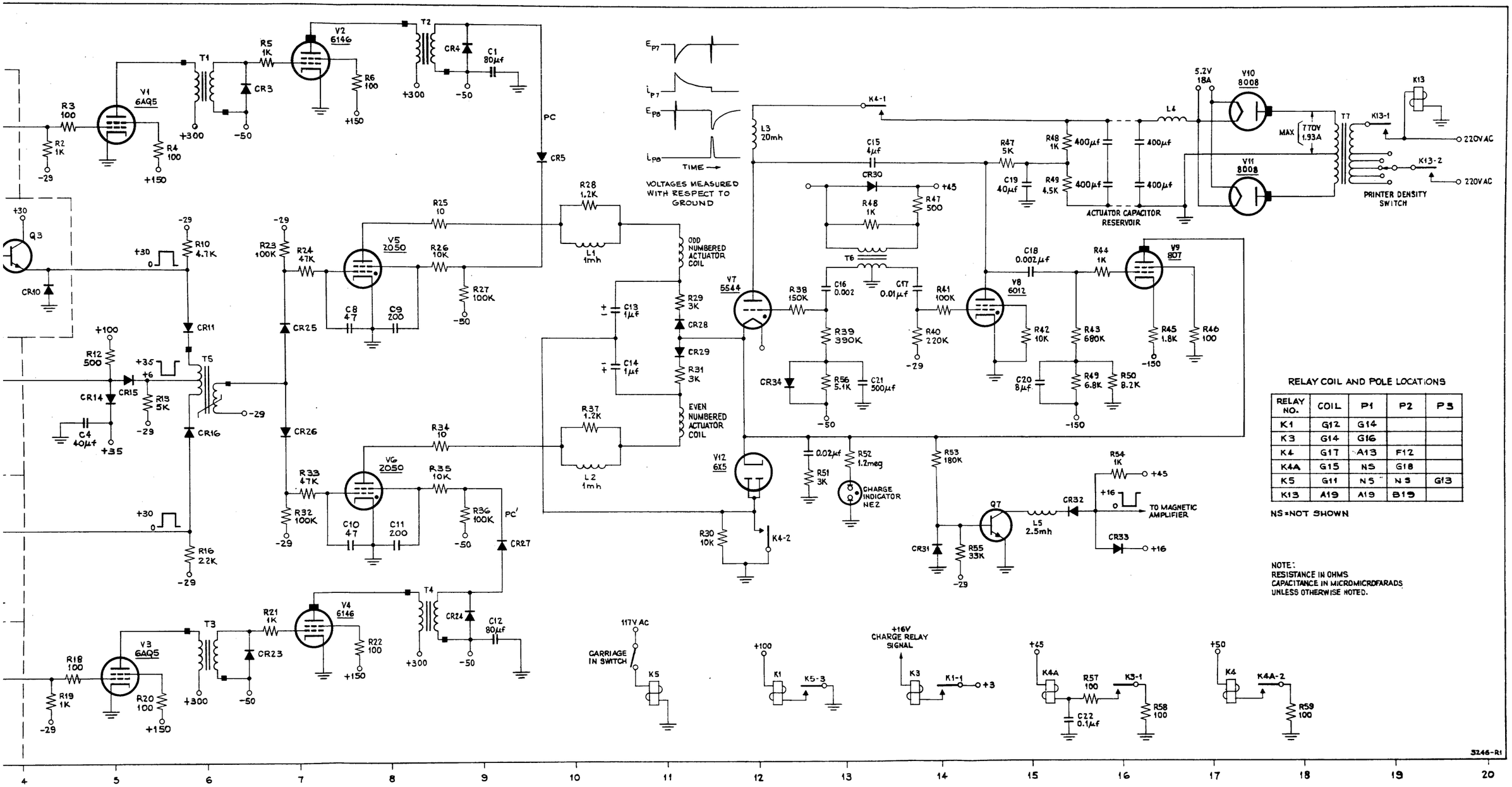


Figure 4-3. Core-Storage Unit Waveforms


TAP +3
PCG
CR30
R50 5.6K
-29
CR1
CR2
R1 4.7K
Q1
+6
R3 100
R2 1K
V1 6AQ5
R4 100
+150
T1
+300
-50
R5 1K
V2 6146
CR3
R6 100
T2
CR4
C1 80μf
PC
CR5
TAP +3
PRP
CR31
R51 5.6K
CR7
CRG
C2 50μf
R7 1K
+29
R8 1K
+28.5
CR8
Q2
+30
R9 10K
-29
-1.5
CR9
Q3
CR10
R10 4.7K
+30
0
CR11
R23 100K
R24 47K
R25 10
V5 2050
R26 10K
R27 100K
C8 47
C9 200
CR25
TAP +3
PRG
CR32
R52 5.6K
CR12
CR13
R11 10K
Q4
C3 15μf
+6
R12 500
+100
+35
CR14
CR15
R15 5K
C4 40μf
+35
T5
CR16
CR26
R28 1.2K
L1 1mh
ODD NUMBERED ACTUATOR COIL
R29 3K
CR28
CR29
R31 3K
EVEN NUMBERED ACTUATOR COIL
C13 1μf
C14 1μf
R34 10
R33 47K
R32 100K
V6 2050
R35 10K
C10 47
C11 200
R36 100K
PC'
CR27
R37 1.2K
L2 1mh
V12 6X5
R30 10K
K4-2
0.02μf
R51 3K
R52 1.2meg
CHARGE INDICATOR NE2
R53 180K
R55 33K
Q7
L5 2.5mh
CR32
CR31
+16
0
TAP +3
PRS
CR33
R55 5.6K
CR18
CR17
C5 5μf
R14 500
R15 1K
CR19
C6 4.7μf
Q5
CR20
C7 5μf
R16 2.2K
TAP +3
PCG
CR34
R54 5.6K
CR21
CR22
R17 4.7K
Q6
R18 100
R19 1K
V3 6AQ5
R20 100
+150
T3
+300
CR23
R21 1K
V4 6146
R22 100
T4
CR24
C12 80μf
E_{P7}
i_{P7}
E_{P8}
i_{P8}
TIME
VOLTAGES MEASURED WITH RESPECT TO GROUND
K4-1
L3 20mh
C15 4μf
CR30
+45
R48 1K
R47 500
T6
C16 0.002
C17 0.01μf
R38 150K
R39 390K
R40 220K
R41 100K
V7 5544
V8 6012
C18 0.002μf
R44 1K
R42 10K
R43 680K
R49 6.8K
C20 8μf
CR34
R56 5.1K
C21 500μf
R47 5K
C19 40μf
R48 1K
R49 4.5K
400μf
400μf
ACTUATOR RESE
117V AC
GARRIAGE IN SWITCH
K5
+100
K1
K5-3
+16V CHARGE RELAY SIGNAL
K3
K1-1
+3
+45
K4A
R57 100
C22 0.1μf
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
A
B
C
D
E
F
G



RELAY NO.	COIL	P1	P2	P3
K1	G12	G14		
K3	G14	G16		
K4	G17	A13	F12	
K4A	G15	NS	G18	
K5	G11	NS	NS	G13
K13	A19	A19	B19	

RELAY COIL AND POLE LOCATIONS

NS=NOT SHOWN

NOTE:
RESISTANCE IN OHMS
CAPACITANCE IN MICROMICROFARADS
UNLESS OTHERWISE NOTED.

Figure 4-4. Print Circuitry, Schematic

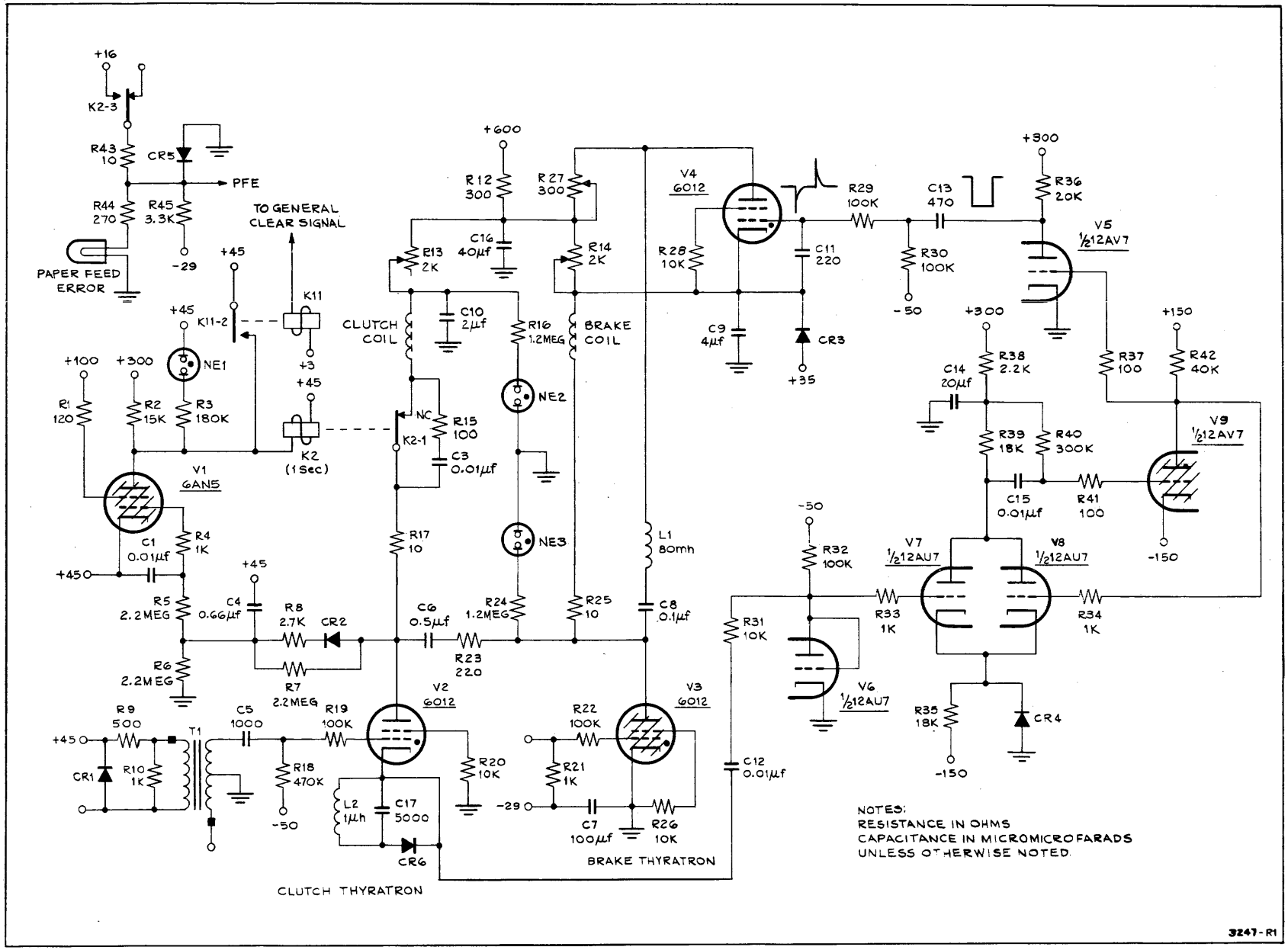


Figure 4-5. Paper-Feed Circuitry

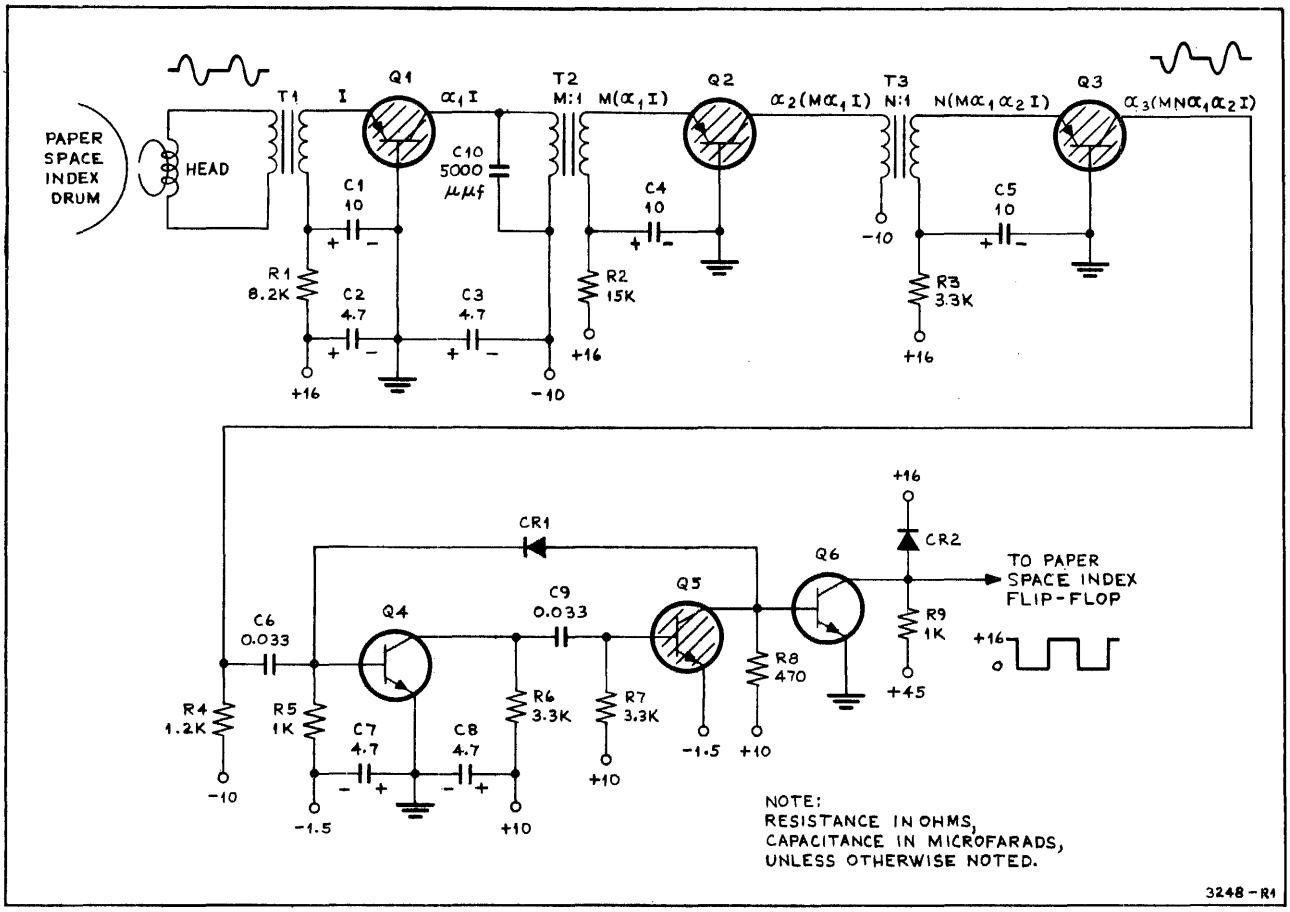


Figure 4-6. Paper-Feed-Drum Amplifier

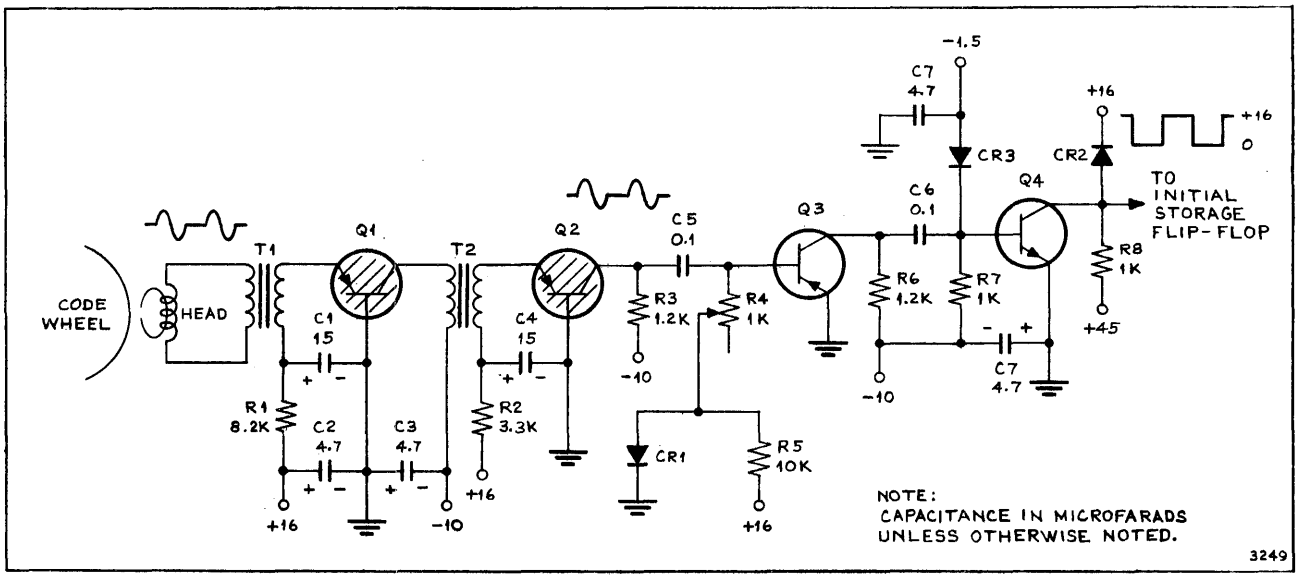


Figure 4-7. Print-Drum Read Amplifier

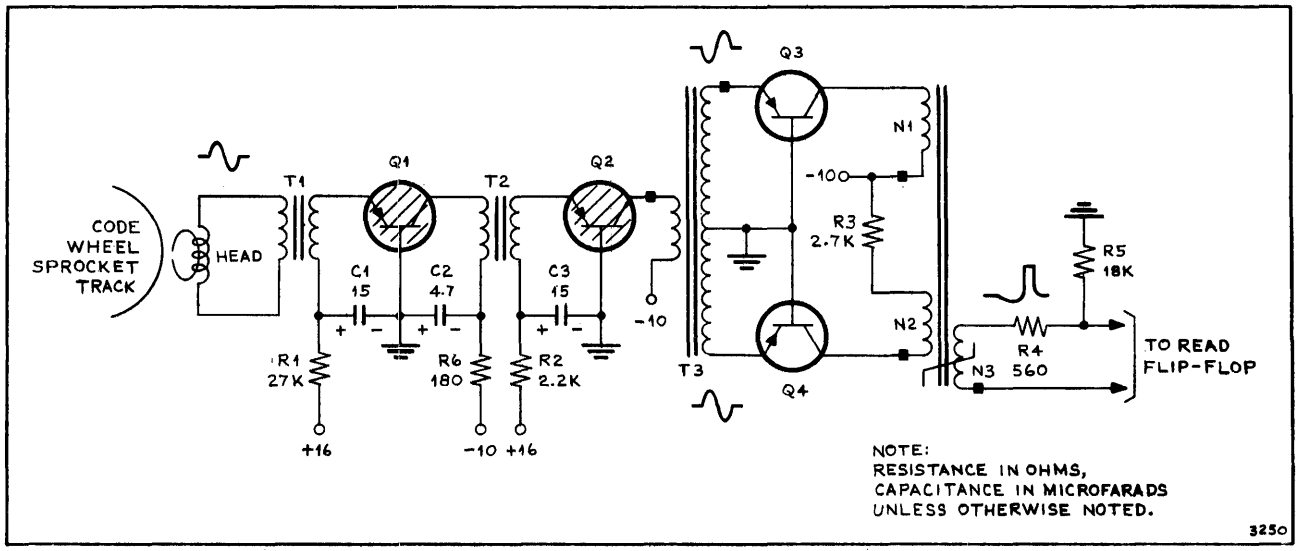


Figure 4-8. Print-Drum Sprocket Amplifier

Type 7904 Card-Sensing Unit
90 Column

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I

INTRODUCTION

1-1. SCOPE OF THE MANUAL

The purpose of this manual is to describe the type 7904 card-sensing unit, one of the three input-output devices in the New Univac system. The manual describes the mechanical and electromechanical components of the card reader, as well as the logical control circuits and instructions that control it. To understand the operation of the card reader, which involves logical circuits and the processing of instructions, familiarity with Manual No. 1 is necessary.

In section II, the physical layout of the card reader is described. Section II also includes functional descriptions of certain parts which are not directly involved in instructions from the processor. Section III, explains the operations of the mechanical, electromechanical, and logical components of the card reader, individually and then as applied to the instructions that control the device. Section IV describes the electronic circuitry.

1-2. REMINGTON RAND PUNCHED CARD

The information processed by the card reader is punched on Remington Rand cards. Information punched on cards is usually in card code. Information read by the card reader in card code must be translated into UCT code before the processor can perform arithmetic operations with the information.

The Remington Rand card, shown in figure 1-1, is divided into two fields: the upper field (UF) and the lower field (LF). Each field contains six rows of punching positions. Each row is 45 columns wide. Because there are 45 columns in each of the two fields, the card is referred to as a 90-column card. The 90 columns are numbered 1 through 45 for the upper field and 46 through 90 for the lower field. Each card has 540 possible hole positions (90 columns times six rows).

Each of the six rows of both the upper and lower fields is assigned a row number: 0, 1, 3, 5, 7, or 9. The row numbers are shown to the right of the card and indicate the decimal value of a single punch in a column. In the figure, the punch in the zero row of column 4 indicates a decimal value of zero. A single punch in row 1 of column 5 indicates a decimal value of one. In other words, a zero or an odd decimal number is indicated by a single punch in the appropriate row. To indicate an even number, two punches are required: one punch in row 1, 3, 5, or 7, and one punch in row 9 of the same column. In figure 1-1 a punch in row 1 and row 9 of the same column is

a 2, a punch in row 3 and row 9 of the same column is a 4, and so forth. Because a punch in the 1, 3, 5, or 7 row can indicate either an odd or an even number, according to whether there is also a punch in the 9 row of the same column, each of the 540 punch positions is marked with a notation (1_2, 3_4, 5_6, or 7_8) which indicates the two possibilities.

The card code for numerics is shown in table 1-1. This code duplicates the punch code for numerics shown punched in columns 9 through 13 on the card in figure 1-1, with a binary one to represent a punched hole.

Table 1-1. Card Code for Numerics

Decimal Value	Row 9 7	5 3 1 0
0	0 0	0 0 0 1
1	0 0	0 0 1 0
2	1 0	0 0 1 0
3	0 0	0 1 0 0
4	1 0	0 1 0 0
5	0 0	1 0 0 0
6	1 0	1 0 0 0
7	0 1	0 0 0 0
8	1 1	0 0 0 0
9	1 0	0 0 0 0

Figure 1-1 shows the 51 characters of the card code. The figure shows the punch positions of numerics, alphabetics, and special characters. For all characters, a punch indicates a 1 bit while a no punch indicates a 0 bit. Refer to table 3-2 in the high-speed printer manual for the complete code. The special characters are sometimes punched as shown in the printer code.

Ten words can be punched on the 90-column card, five in the upper field and five in the lower. Each field then contains four ten-digit words and one five-digit word.

1-3. GENERAL FUNCTIONAL DESCRIPTION

The card reader is an input device which reads information punched on cards and transfers the information to the processor. Basically, it consists of an input bin, two read stations, and three output stackers. The card is read at the first read

station, transported to the second read station, and read again. The information read from the card in the two read stations is transferred to a special area on the processor storage drum known as the card buffer. From the card buffer, the information is transferred into the main-storage area of the drum, where it is available for use according to the program.

The movement of a card through the fast reader is shown in figure 1-2. Under the control of a program instruction (72), a card is pushed from the input bin into the roller mechanism of the reader. Once the movement of the card is initiated, the card automatically is read at read station 1, then is read again at read station 2, and finally goes to one of the output stackers. The reading at read station 2 enables programmed comparisons of the two readings to provide complete identity and validity checks.

Normally, cards are fed continuously so that a card is read at read station 1 at the same time that another card is read at read station 2. Each row of a card is read as the card moves under the 45 brushes of each read station. The first row read consists of the least significant bits of all digits in the upper field. The next row read consists of the next higher order bits. Six rows of a card must be sensed before complete characters are read. After the six rows of the upper field have been read, the 45 brushes sense the six rows of the lower field.

Each time a row passes under the brushes, a pulse is placed on a sensing roll under the card. If a brush has a hole under it at the time the roll is pulsed, it receives a pulse from the roll. This pulse represents a 1 bit. If a brush does not have a hole under it, the card insulates it from the charged roll. The insulation prevents a pulse from being placed on the brush. This lack of a pulse represents a 0 bit for that hole position.

After a card is read at the second read station, it moves to one of the three output stackers shown in figure 1-2. The selection of stackers is made by a 47 instruction in the program. A detailed schematic of the card reader is shown in figure 3-4.

The information read at the read stations is first sent to a temporary storage device called intermediate storage, which is capable of storing one row from the first read station and one row from the second read station, as shown in figure 3-5. Before the next row is read in the read stations, the information in intermediate storage is recorded in a special area of the magnetic drum called the card buffer band. When the cards in both read stations have been completely recorded in the card buffer band under control of a 72 instruction, a

96 instruction transfers the information to a predetermined band in main storage. The transfer of information between the read stations and main storage is discussed in detail in section III.

1-4. CHARACTERISTICS

The following list gives the mechanical and electrical characteristics of the card reader:

Dimensions	
Width	47 in.
Length	48 in.
Height	26 in.
Weight	400 lb
Card Feed Rate	450 cpm

	Vacuum Motor	Feed Motor
Voltage	110 v ac	110 v ac
Frequency	60 cps	60 cps
Phase	single	single
Power	0.825 kva	0.385 kva

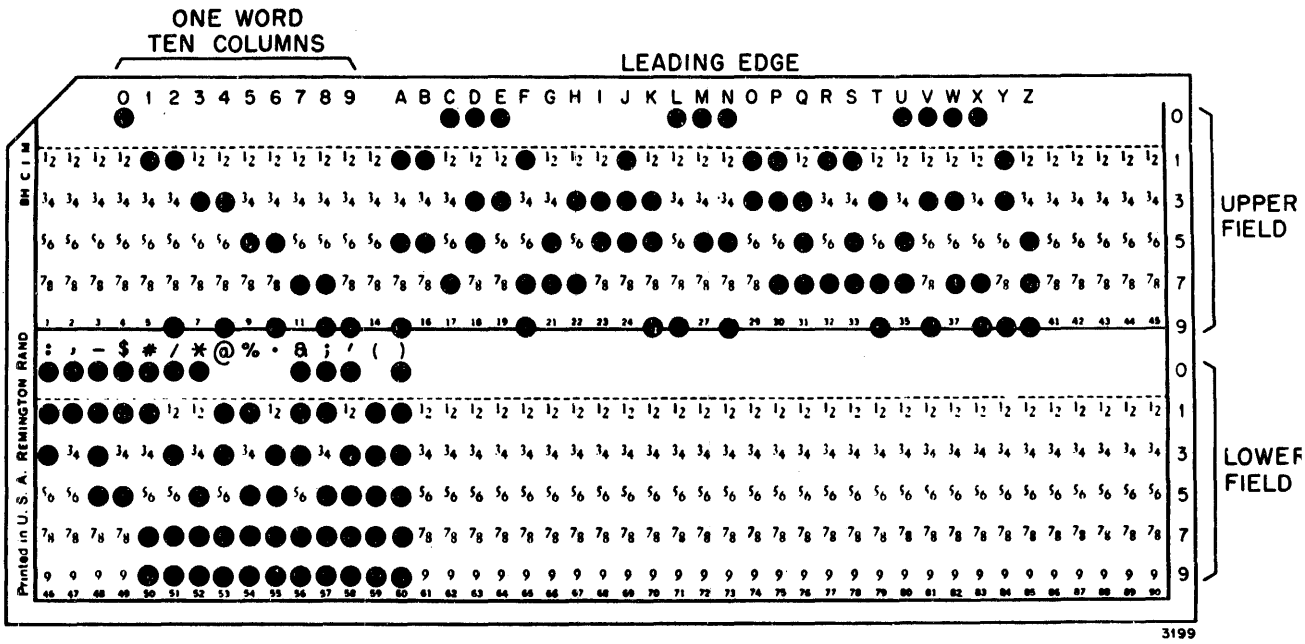


Figure 1-1. Remington Rand Punched Card and Card Code

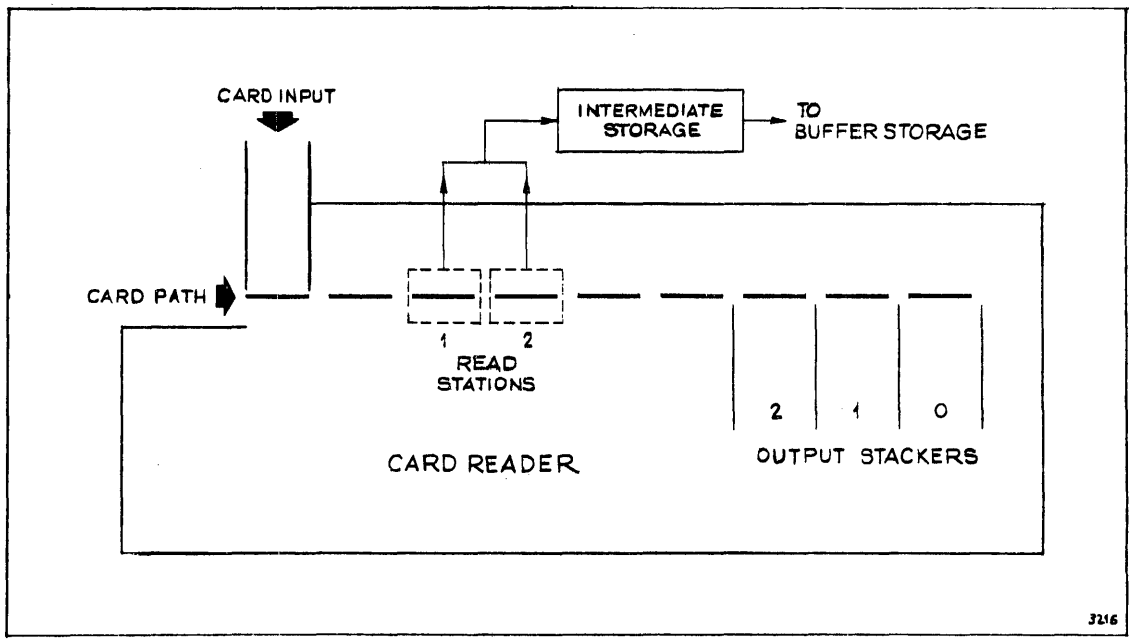


Figure 1-2. Card Reader with Card Path

SECTION II

PHYSICAL DESCRIPTION

2-1. SCOPE

This section is a description of the important mechanical components of the card reader. Only those parts which are essential to the general function of the card-reader are discussed. Most of the packages for the card-reader synchronizing circuits are located within the processor cabinet and are described in section 3-16. Designations like (2-3,5) refer to figures; for example, figure 2-3,5 is the lower-roller helical gear.

2-2. INPUT SYSTEM

2-3. INPUT BIN

The input bin at the right-hand side of the card reader, consists of two vertical card guides (2-3,3). It can hold 1000 cards. When the bin is empty, the empty-magazine switch (2-6,3) in the first read station causes the card reader to stop and lights the EMPTY MAGAZINE indicator on the card-reader control panel. The empty-bin switch is always open except when a card is passing through the first read station, closing it. If a card is not fed when a card-feed instruction is given, the switch remains open and indicates an empty bin.

2-4. THROAT KNIFE AND BLOCK

The deck of input cards rests on the throat block (2-3, 11) and the card support blades (2-3,10). The throat block is a rectangular plate with 16 small circular vacuum openings (2-3,6).

Mounted directly below the throat block is a hollow casting with two openings into the cavity. One of these openings meets the 16 circular openings of the throat block. A flexible, fiber, vacuum-intake tube (2-1,17) fits into the other opening. The vacuum system draws air through the openings on the throat block, tube, and cavity, thus gripping the leading edge of the bottom card on the input deck.

The throat knife (2-3,16) is a rectangular plate that allows only one card at a time to enter the reader. The clearance between the top of the throat block and the bottom edge of the throat knife is less than the thickness of two cards. The clearance between the throat block and throat knife is adjusted by an adjustment screw (2-3,17).

2-5. FEED-ARM ASSEMBLY

The feed-arm assembly is the mechanism that picks the bottom card of the input deck and forces it into the roller transport system.

The arm (2-1,22 and 2-7,3), is a channel-section casting with an internal cavity. The bottom of the arm is attached to a rectangular bar (2-1,16) which is mounted on pivots at both ends. The pickerknife head (2-3,7) is bolted to the top of the feed arm.

The feed-arm cavity has two openings, one on the lower right face and one through the top of the pickerknife head. A flexible, fiber intake tube (2-1,14) from the vacuum system is fitted to the hole in the lower right face of the arm.

The upper surface of the pickerknife head is level with the card bed when the feed arm is latched. The pickerknife head is slotted to accommodate the 15 card-support blades (2-3,10) and an opening (2-3,8) to the feed-arm cavity is located between each two slots. The vacuum system draws air through the 14 openings to grip the trailing edge of the bottom card of the input deck.

The pickerknife (2-3,9) is mounted on the right-hand face of the pickerknife head (2-3, 7). The pickerknife is adjusted so that its upper edge projects between 0.003 and 0.004 inch above the top of the knife head, allowing the pickerknife to engage approximately 5/7 of the thickness of the card.

The cam follower (2-7,2) is mounted in the center of the feed arm and rides on the cam (2-7,5). The cam and cam follower determine the movement of the feed arm and pickerknife.

Two feed springs are mounted on the feed arm, above the cam follower, one on each side (2-7,6). The other end of each spring is attached to a bar that is attached to the front and rear frames.

The feed-arm balance is a rectangular steel weight (2-1, 15) bolted to the lower surface of the pivot bar to counterbalance the feed arm.

The latch mechanism is mounted on the latch-support bar (2-1,21). The latch mechanism includes the pickerknife latch (2-1,19), a solenoid, and spring. The pickerknife latch engages the latch plate (figure 3-3a), which is mounted above the cam follower in the center of the feed arm.

The latch arm is held up by a small spring attached to its extreme right end. The opposite end of the spring is connected to a screw which is used to adjust its tension. The latch is actuated by a solenoid mounted directly below it.

The latch mechanism can be shifted to the right or left by an adjustable screw which turns against the right face of the latch-support bar. An adjustable screw at the bottom of the mechanism positions a stop below the latch arm and determines how far open the latch spring can pull the latch arm.

2-6. CAMSHAFT ASSEMBLY

The camshaft (2-7,4) rotates on ball bearings which are mounted on the frame. Several important parts attached to the camshaft are discussed in the following paragraphs. Figure 2-2,3 indicates the approximate location of the camshaft assembly; figure 2-7 shows the cam itself.

2-7. TIMING DIAL. The timing dial (2-2,2), mounted on the forward end of the camshaft, is six inches in diameter and is graduated to indicate the degree of cam rotation. When the dial reads 0 degree, the feed-spring tension-release bump (section 3-10) on the cam has moved the pickerknife as far back as possible.

2-8. FLYWHEEL. The flywheel (2-2,1) and (2-7,1) is located directly behind the timing dial. When the feed arm is riding on the cam, the camshaft receives a load which varies continuously because of the change in spring tension between the low and high lobe positions of the cam. A change in load necessarily causes a change in the speed of the camshaft. The flywheel acts as a damper to reduce the change in speed of the shaft and prevents any extra load from being transferred to the drive motor.

2-9. ANTI-BACKUP CLUTCH. The anti-backup clutch (2-1,18) is mounted on the camshaft directly behind the forward frame. The clutch is mounted by a special adapter sleeve and housed in an aluminum casting. A spring-loaded control rod (not shown) extends through the housing drum and engages a keyway on the clutch. When engaged, the clutch permits rotation counterclockwise only, viewed from the front of the reader. When the control rod is disengaged, the flywheel can be turned clockwise by hand to make adjustments.

CAUTION

Do not turn the flywheel clockwise when a card is in the rollers. Moving a card backward through the reader causes serious damage to the sensing brushes, which are oriented for forward motion only.

The spring loading of the control rod causes it, after being disengaged, to engage automatically within one rotation of the camshaft.

2-10. FEED CAM. The feed cam (2-7,5) is keyed to the camshaft midway between the frames. The cam is perfectly symmetrical (figure 3-3) and functions to move the feed arm, which rides on it, approximately 0.9 inch on every card cycle signal. A 0.01-inch hump on the cam causes the release of the feedspring tension from the pickerknife latch (section 3-10).

2-11. CAMSHAFT TIMING PULLEY. The timing pulley is mounted on the camshaft between the frame and the upper drive pulley. The pulley has 16 teeth and transmits power to the cardtransport rollers.

2-12. UPPER DRIVE PULLEY. The upper drive pulley (2-1,2) is mounted on the extreme rear of the camshaft. The drive pulley is driven by a V belt at an approximate speed reduction of 2:1 from the drive motor (2-1,13).

2-13. TIMING DISC. The timing disc, (2-1,3) is bolted to the rear flange of the upper drive pulley. The three holes through the disc for the mounting bolts are elongated curved slots (2-1,4) used for adjustment purposes. The timing disc has 12 slots at 24-degree intervals around its circumference.

A photocell (2-1,5) and exciter lamp are mounted on a bracket below the disc. The exciter lamp is behind the disc opposite the photocell. The disc rotates between the two units and produces a signal every time a slot allows the light from the lamp to excite the photocell. Section 3-21 describes the function of this signal in detail.

2-14. TRANSPORT SYSTEM

2-15. TRANSPORT ROLLERS

There are seven sets of transport rollers (figure 2-5), each set consisting of an upper and a lower roller.

The first set of transport rollers (2-3,14 and 12) has four steel segments on each roller. The card is moved by being gripped between the upper and lower segments. Each segment of each roller must grip the card with equal force in order to keep the card centered during its passage through the card reader. Tension between rollers is adjusted by two pairs of screws (2-3,1 and 2). The first pair of adjustments (2-3,1) consists of screw-adjusted spring-loaded blocks (2-3,15) on stationary rings (2-3,13). When the tension screw is tightened, the roller is forced downward, increasing the pressure between rollers. The lower roller has an identical pair of adjustments. The second pair of adjustments consists of screws (2-3,2) located on the ends of the upper roller. These screws are used to adjust the position of the upper roller with reference to the lower one, thus increasing or decreasing the tension between the rollers. This adjustment is on the upper roller only. The remaining six sets of transport rollers also

consist of an upper and lower roller. The upper rollers (2-4,11) have four rubber-fabric segments (2-4,7), and the lower rollers have four steel segments (2-4,8). An adjustment screw (2-4,3 and 12) is located on each end of the upper rollers. This adjustment is identical to the end adjustment on the first upper roller.

A mechanism known as the jam detector trips a switch (2-5,2) to stop the reader whenever a card jam occurs within the last four sets of rollers. The metal jam-detector beam (2-5,4) is adjusted so that when a card moves upward out of its normal path, the beam moves, energizing the switch.

Any static charge that the cards may have accumulated is eliminated by the static eliminator (2-4,9) located before the sixth set of rollers.

2-16. PULLEY SYSTEM

The transport rollers are driven by a pulley system connected to the main drive motor. Figure 2-5 shows the timing belt (9), pulley (8), and timing belt idler (7). The timing belt is connected to a pulley on the camshaft and then to all of the lower-roller pulleys (2-5,8). The lower rollers drive the upper rollers by helical gears (2-3,4; 2-3,5).

2-17. SENSING SYSTEM

2-18. BRUSH HOLDERS

The sensing system consists of two brush holders (2-3,18 and 19). A brush holder (figure 2-6) contains 45 brushes (2-6,2) which sense one row of a card, an empty-input-bin detector (2-6,3), and a connector (2-6,4). The position of the brush holders can be adjusted with the adjustment screw (2-4,2) and the vertical adjustment latch (2-4,1).

2-19. SENSING ROLLS

Two sensing rolls (2-4,5), one of each read station, carry the pulses necessary to sense the presence of punched holes in the cards. The sensing roll transfers the pulses to any sensing brushes which have detected a hole. The brushes which do not detect a hole are insulated from the roller by the card. The sensing roll rotates freely on ball bearings in the side frames.

2-20. REGISTRATION PHOTOCELLS

A registration photocell (2-4,13 and 6) and an exciter lamp are located after each read station to detect incorrect registration (section 3-53) or misfeed of the card in the read station. When a misfeed is detected, an indicator lamp is lighted on the control panel.

2-21. OUTPUT SYSTEM

2-22. OUTPUT STACKERS

The three output stackers of the reader, numbered 0, 1 and 2, are shown in figure 2-2 as items 16, 17, and 18. Each bin is capable of holding 850 to 1200 cards. When any bin is full, a switch is energized which stops the reader and indicates OUTPUT BIN FULL on the control panel.

The cards fall on spring-loaded platforms that settle as the number of cards increases. The capacity of the bins and the settling rate of the platforms is determined by adjusting the tension on the platform springs (2-2,13).

2-23. STACKER SELECTORS

Stacker 1 and 2 have stacker selectors (2-5,6) that are controlled by actuators to direct cards into the corresponding stackers. Stacker 0 has fixed card guides (2-5,5) and receives all cards not directed to the first two bins.

2-24. CONTROL PANEL

The card-reader control panel (figure 2-8) contains six illuminated pushbuttons and six indicator lights, described in table 2-1. Engineering drawing DX805 968 is a schematic of the control-panel circuits.

2-25. MISCELLANEOUS COMPONENTS

2-26. MOTORS

The reader contains three motors, the vacuum motor (2-1,9), the drive motor (2-1,13), and the blower motor located next to the package library. The vacuum motor drives the vacuum compressor (2-2,9). The drive motor drives the camshaft and rollers.

2-27. MOUNTING BOARDS

Electronic components for the card-reader circuits are mounted on seven component mounting boards, numbered MB1 through MB7. The circuits on the boards are listed in table 2-2. (See section II of the maintenance manual for addressing of mounting-board components.)

MB3 is mounted between the upright beams on lower right end of the card reader frame. The photocell-sensitivity controls (2-1,12), R12, R13, and R14 are located directly below MB2. Mounted directly below MB7 is the capacitor-storage clear-pulse adjustment, R11 (2-2,7) and the brush-probe-signal adjustment, R10 (2-2,8).

Table 2-1. Card-Reader Control Panel

a. CONTROLS: Six illuminated pushbuttons

Panel Marking	Function	Indication
RESET/CARD JAM	Resets card-jam relay when card jam is cleared.**	Red to indicate card jam.
CLEAR/SYSTEM OFF NORMAL	Clears internal controls, indicators, and flip-flops.**	Amber when any abnormal condition occurs in the processor, read-punch unit, or card reader.
COMPUTATION/RUN	Starts processor.**	Green when operated.
COMPUTATION/STOP	Stops processor.**	Amber when operated.
MOTOR/FEED	Turns feed motor on.*	Green when operated.
MOTOR/VACUUM	Turns vacuum motor on.*	Green when operated.

b. INDICATORS: Six jewel-lights

Panel Marking	Function
AIR FLOW	Lights amber when air vane switch closes. Indicates rate of air flow has fallen below required minimum.
INTERLOCK	Lights amber when top door of card reader is open.
OUTPUT BIN FULL	Lights amber when output bin is full.
REGISTRATION/ CHECK STATION	Lights red when incorrect registration is in check station.
REGISTRATION/ READ STATION	Lights red when incorrect registration is in read station.
INPUT MAGAZINE EMPTY	Lights amber when input is empty.

* springloaded
** alternate action

Table 2-2. Mounting-Board Circuits

Mounting Board	Figure	Circuit
MB1	2-1,6	Timing photocell (2-1,5); retriggerable delay-flop
MB2	2-1,7	Registration photocells (2-4,13 and 6)
MB3	—	Intermediate-storage clear; brush-probe generator
MB4	2-5,1	Control panel
MB5	2-2,4	Capacitor probe and clear; miscellaneous
MB6	2-2,5	Capacitor probe and clear; miscellaneous
MB7	2-2,6	Intermediate-storage clear; brush-probe generator

2-28. CONNECTORS

The card reader is connected to the central processor by two cables, a 100-conductor cable for signals and a 37-conductor cable for power. Connectors on these and other cables are named alphabetically; for example, CPE, CPD. Connector CPD (2-2,11) is a 100-pin connector carrying signals to and from the processor. Connector CP53 (2-2,12) is a 37-pin connector carrying power from the processor to the card reader.

The read stations are connected to the circuit packages in the card library by cables (2-1,1) with 80 pin connectors. The first read station uses connector CPE (2-3,18), and the second read station connector CPF (2-3,19).

The control-panel wiring terminates in a 33-pin connector, JP3 (2-5,3). All signals to and from the control panel pass through this connector.

2-29. BARRIER STRIPS

The card reader utilizes nine barrier strips, labeled BS1 through BS9. Strip BS1 (2-2,10) distributes motor and contactor voltage. Strip BS2, mounted on the bottom side of the pickerknife latch-support bar (2-1,21), distributes voltage to the pickerknife actuator. Strips BS3 and BS4, located below

the output bin selectors, (2-5,6) distribute voltage to the selector actuators on stacker bins 2 and 1, respectively. Strip BS5, located on the frame to the left of the connectors CPD and CP53 (2-2,12 and 11), distributes voltage to the card reader. Strips BS6 (2-1,20) and BS7 (located on frame opposite BS6) distribute power to the brushes. Strip BS8, located on top of the card library (2-1,8), serves as a distribution point for the empty magazine signal. Strip BS9 (not shown) distributes power to the blower motor.

2-30. PACKAGE LIBRARY

The package library (2-1,8) consists of two shelves, FA and FB, each capable of holding 24 packages. The packages are numbered 00 through 23 from left to right, viewed from the wiring side (2-2,14) of the library. Refer to the maintenance manual for package and connection addressing.

2-31. CONTACTORS

Two contactors are located in the base of the reader. Contactor 1 (2-1,10) is the feed-motor contactor and contactor 2, located next to contactor 1, is the vacuum-motor contactor.

2-32. TRANSFORMER

The transformer (2-1,11), located next to the contactors, is a step-down transformer which reduces the voltage from 115 volts to 5.2 volts for the exciter lamps of the photocell circuits.

2-33. RELAYS

Relays 2A and 2B (2-2,15) are the latching card-jam relays that stop the card reader and light the CARD JAM indicator on the control panel.

2-34. BLOWER

A blower, located in front of the package library, is used to cool the packages.

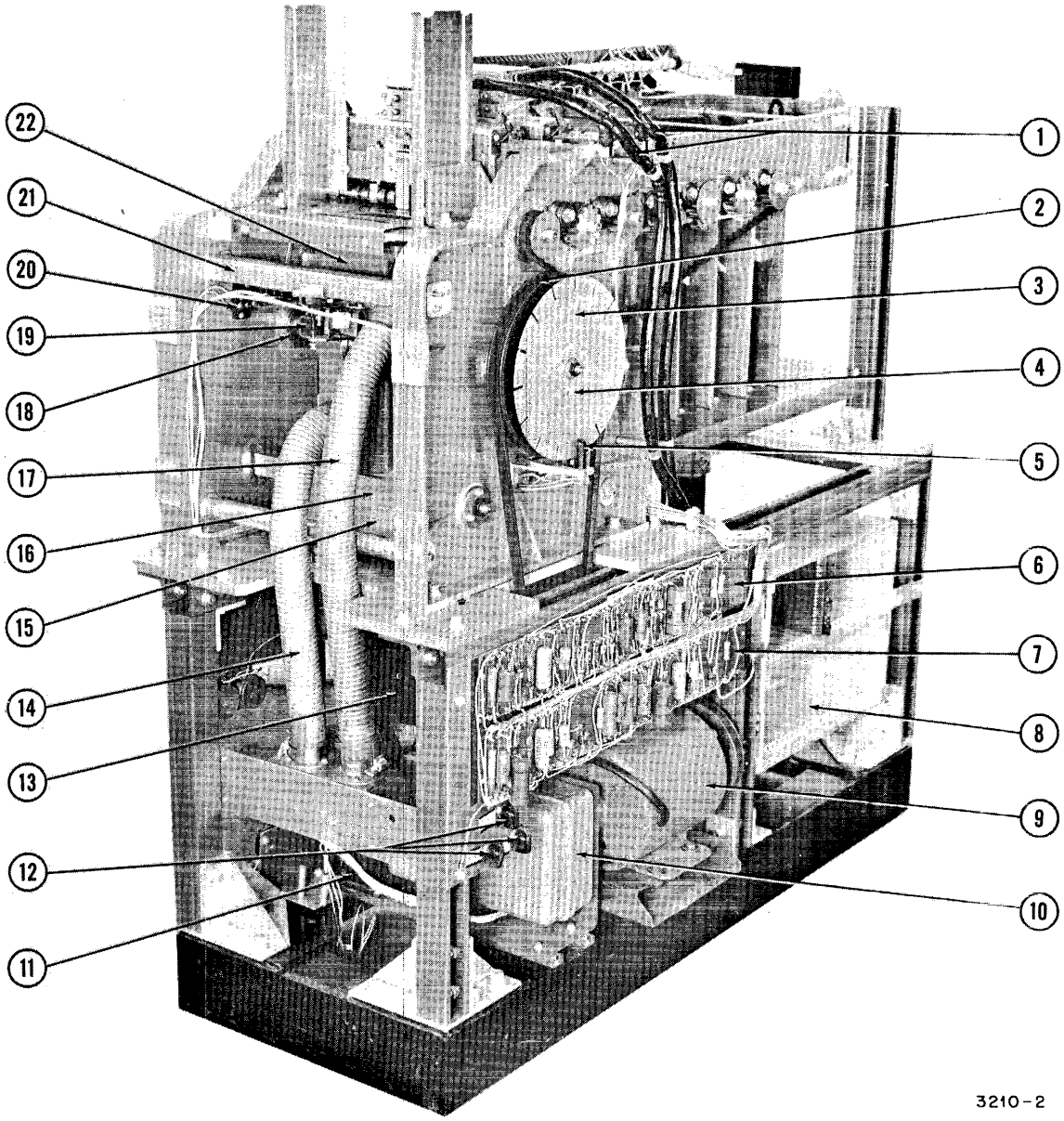


Figure 2-1. Card Reader, Right Rear View

1. Read-station cables
2. Upper drive pulley
3. Timing disc
4. Timing-disc adjustment
5. Timing photocell
6. Mounting board 1
7. Mounting board 2
8. Package library
9. Vacuum motor
10. Contactor 1
11. Transformer T1
12. Photocell sensitivity controls
13. Drive motor
14. Vacuum tubing
15. Feed-arm balance
16. Feed-arm pivot bar
17. Vacuum tubing
18. Anti-backup clutch
19. Pickerknife latch
20. Barrier latch
21. Latch-support bar
22. Feed arm

KEY

1. Flywheel
2. Timing dial
3. Feed cam assembly (figure 2-7)
4. Mounting board 5
5. Mounting board 6
6. Mounting board 7
7. Capacitor-storage clear-pulse adjustment
8. Brush-probe-signal adjustment
9. Vacuum compressor
10. Barrier strip 1
11. Connector plug D
12. Connector plug 53
13. Platform spring
14. Package spring
15. Card-jam relays 2A and 2B
16. Stacker 0
17. Stacker 1
18. Stacker 2

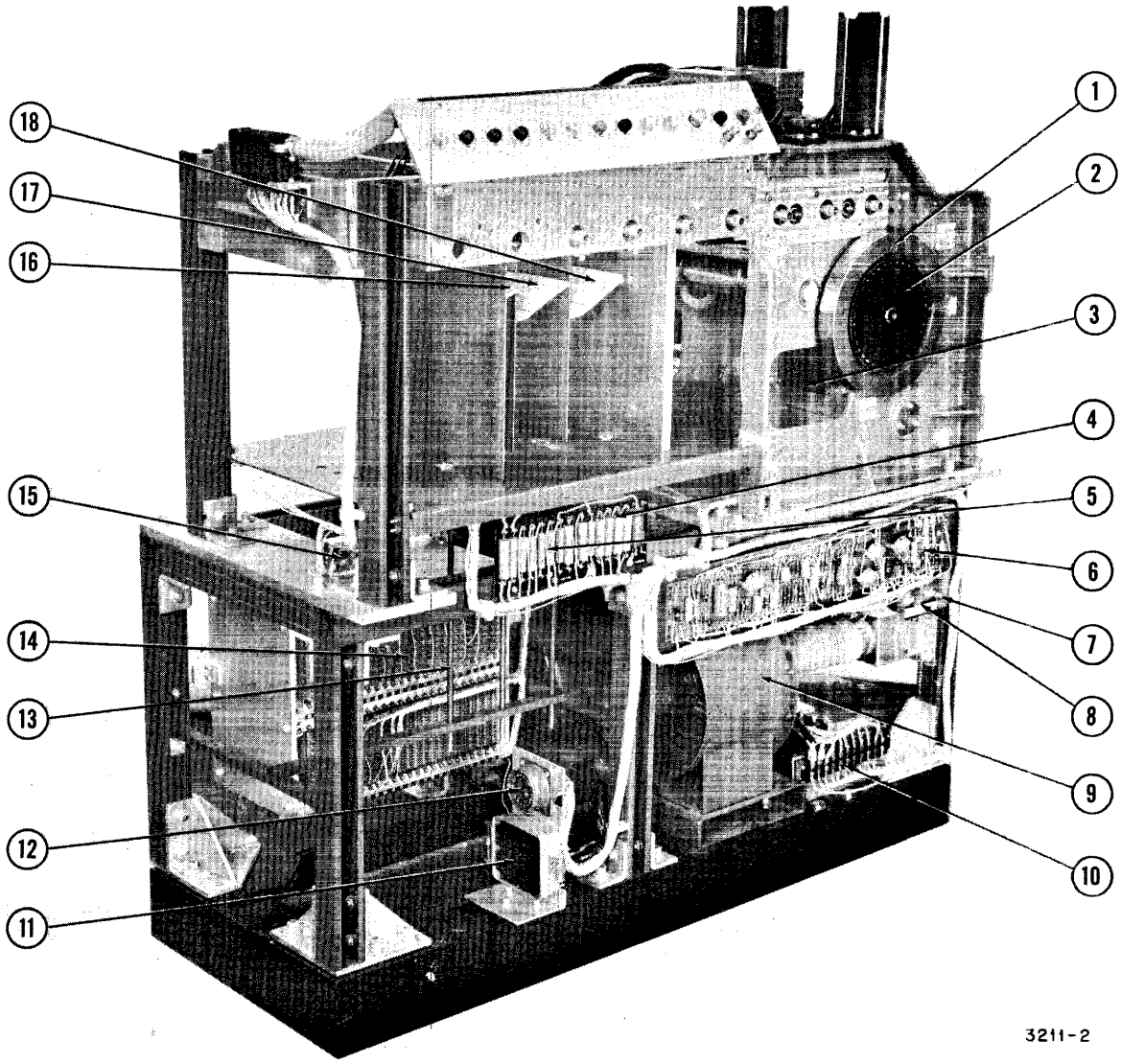


Figure 2-2. Card Reader, Left Front View

KEY

1. Upper-roller tension adjustment (center)
2. Upper-roller tension adjustment (end)
3. Input bin
4. Upper-roller helical gear
5. Lower-roller helical gear
6. Vacuum openings
7. Pickerknife head
8. Throat-block vacuum openings
9. Pickerknife
10. Card-support blades
11. Throat block
12. Lower-roller steel segment
13. Upper-roller tension-adjustment ring
14. Upper-roller steel segment
15. Upper-roller tension-adjustment block
16. Throat knife
17. Adjustment screw
18. Read station 1
19. Read station 2

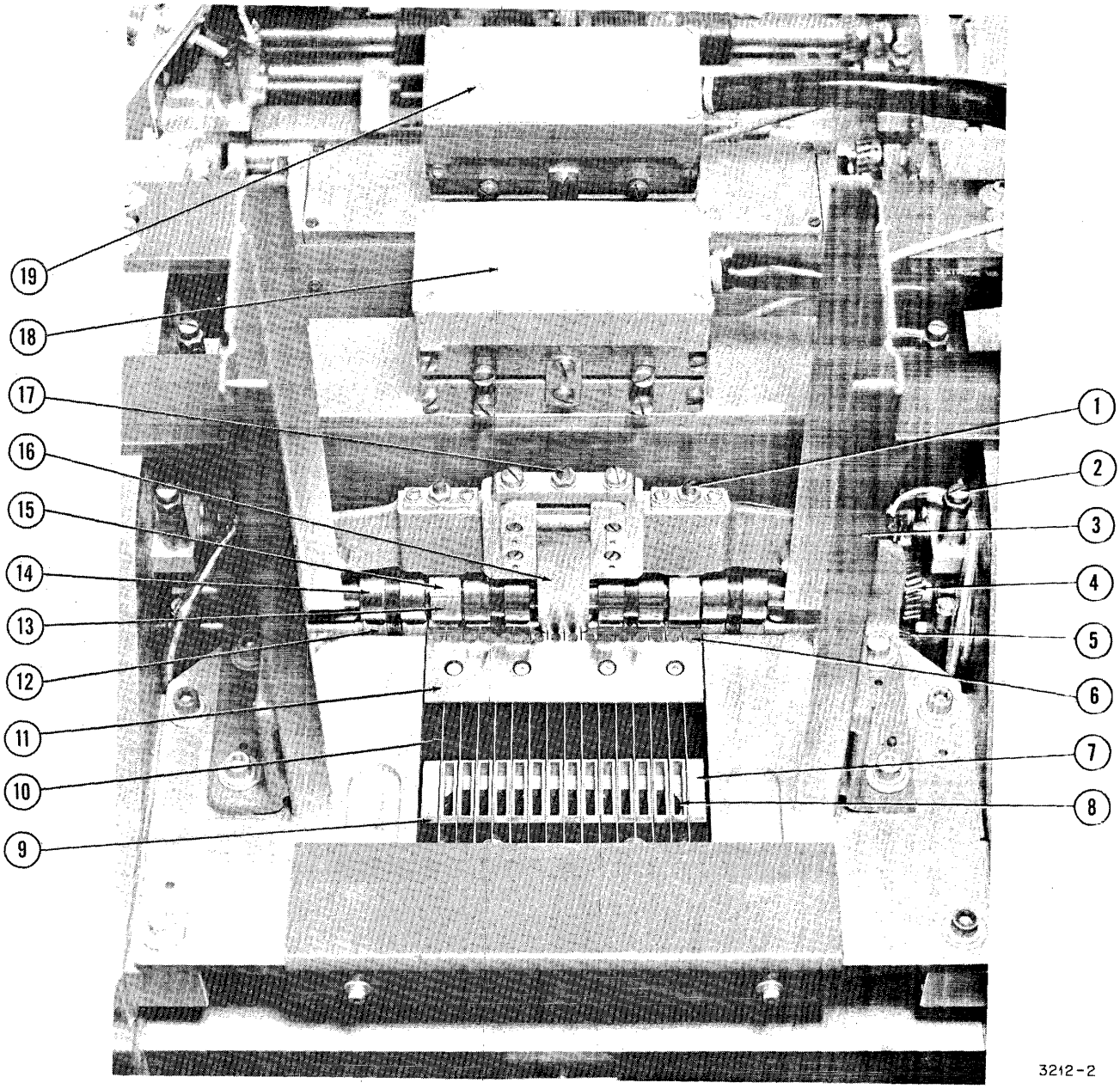


Figure 2-3. Input Bin and Feed Section

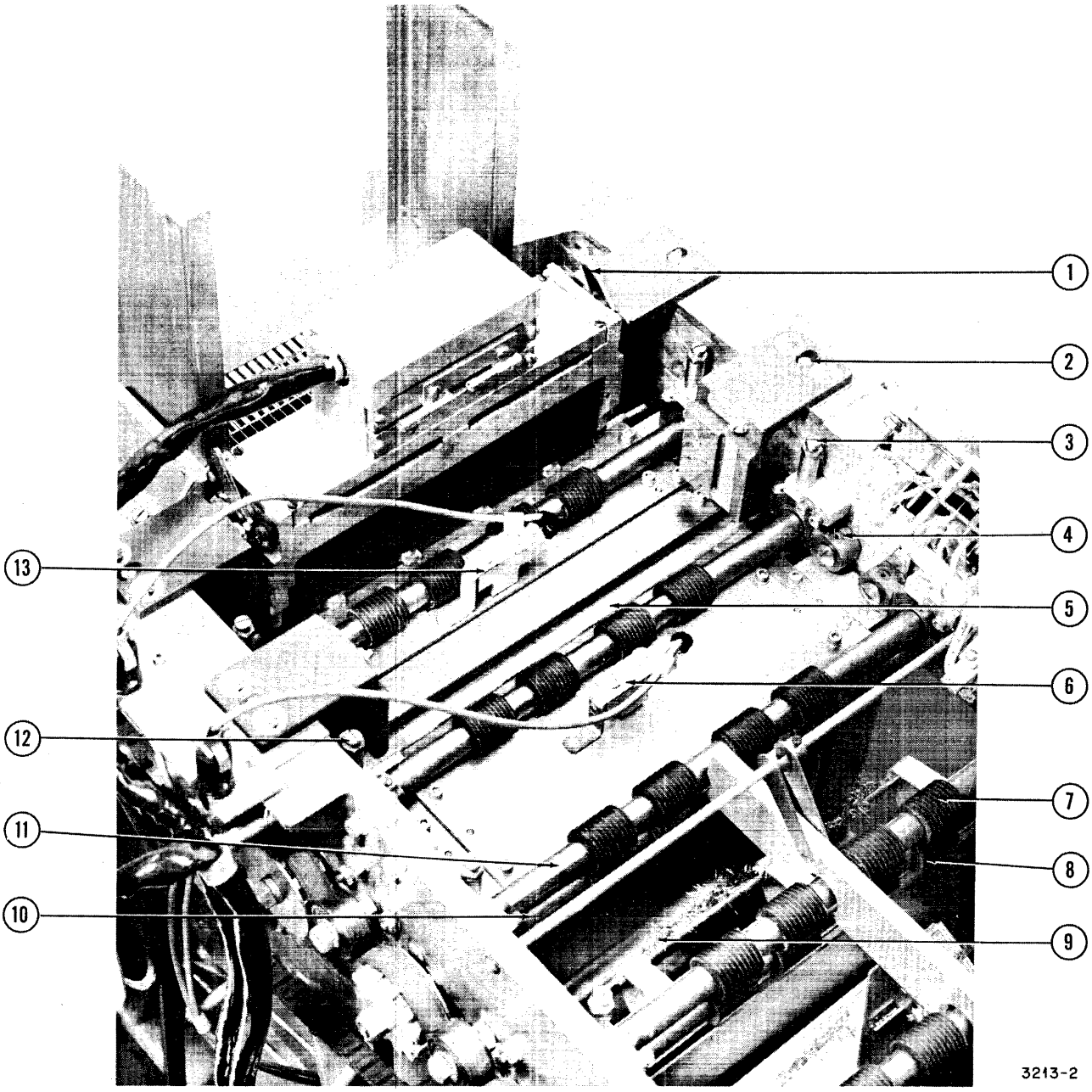


Figure 2-4. Read Stations and Transport Section

1. Brush-holder mounting latch
2. Brush-holder adjustment
3. Upper-roller tension adjustment
4. Upper-roller pivot
5. Sensing roll
6. Registration photocell 2
7. Upper-roller rubber-fabric segment
8. Lower-roller steel segment
9. Static eliminator
10. Lower-roller shaft
11. Upper-roller shaft
12. Upper-roller tension adjustment
13. Registration photocell 1

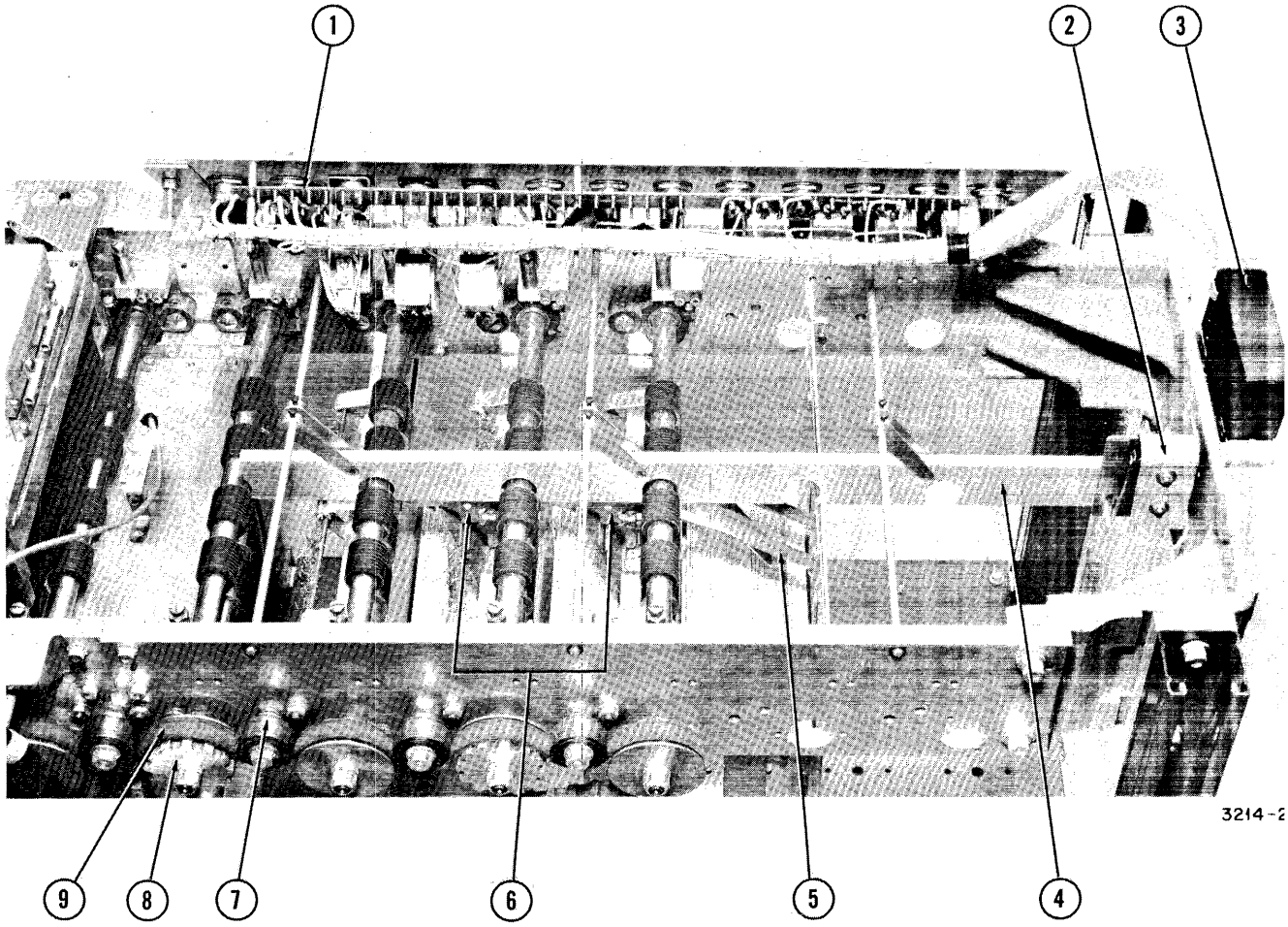


Figure 2-5. Transport Section and Output Stackers

1. Mounting board 4
2. Jam-detector switch
3. Connector JP3
4. Jam detector
5. Stacker card guides
6. Stacker selectors
7. Timing-belt idler
8. Timing pulley
9. Timing belt

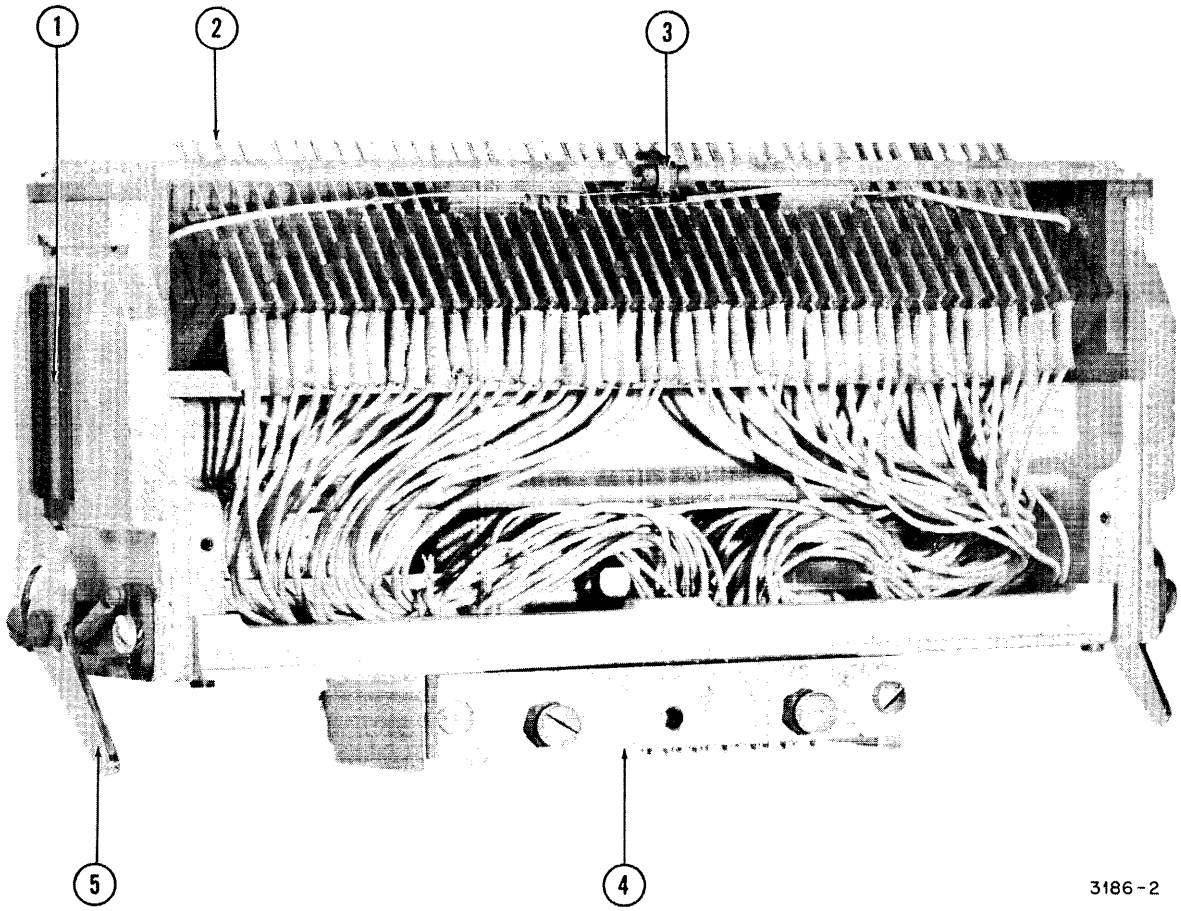


Figure 2-6. Sensing-Brush Holder

1. Mounting bracket
2. Sensing brush
3. Empty-magazine switch
4. Connector
5. Mounting latch

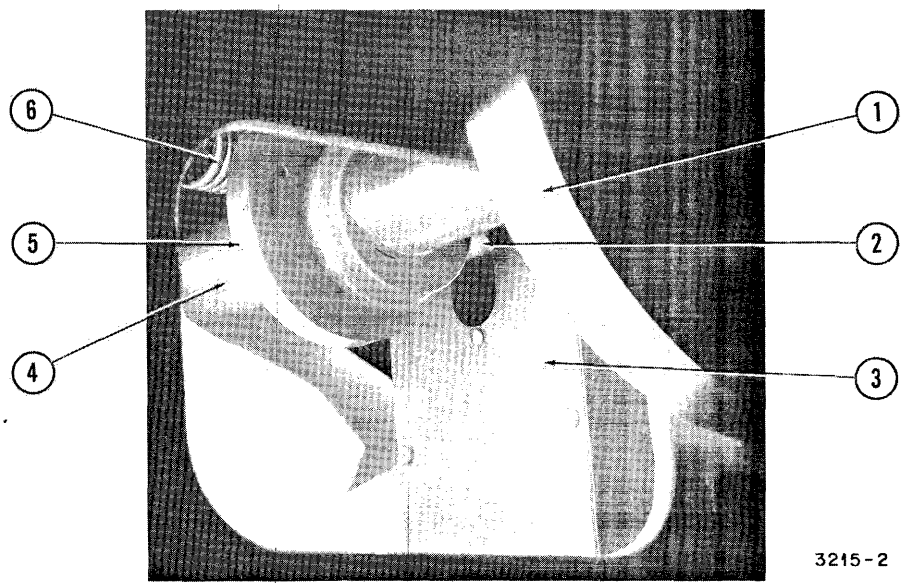
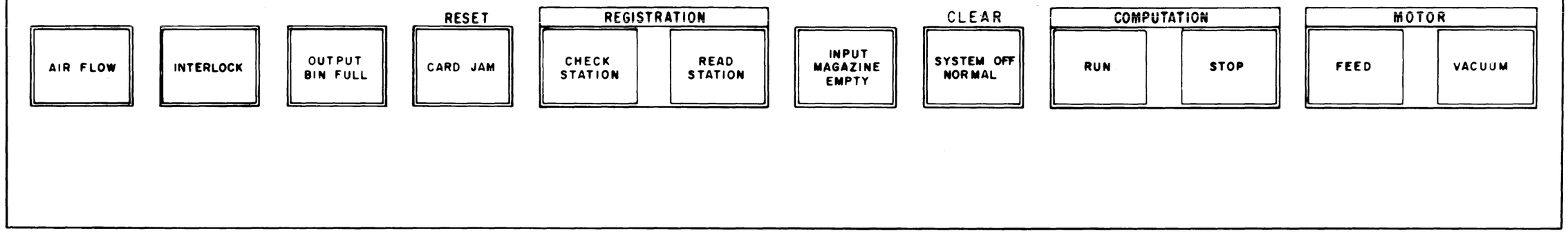


Figure 2-7. Feed Cam Assembly

1. Flywheel
2. Feed-cam follower
3. Feed arm
4. Camshaft
5. Feed cam
6. Feed-arm spring



3252

Figure 2-8. Card-Reader Control Panel

SECTION III

THEORY OF OPERATION

3-1. SCOPE

In order to simplify the treatment of the theory of operation of the card reader, the mechanical, electromechanical, and logical components are first described in detail. A working knowledge of these components is assumed in section 3-36, in which the card-reader instructions and timing are described. Section 3-47 describes the abnormal conditions which can take place in the card reader and its control circuits. As in section II, designations like (2-3,5) refer to figures.

3-2. GENERAL DESCRIPTION

When the card reader is turned on, the electromechanical system that moves the card through the unit begins to function. No card is sent through the machine, however, until a 72 (CC) instruction actuates the pickerknife which pushes one card from the input bin into the roller mechanism. Once the pickerknife starts it through the roller mechanism, the card is automatically read in read stations 1 and 2. It then goes to the output stacker specified by the program (figure 3-4).

Each time the brushes in a read station probe a row of a card, the roll under the card is pulsed (sections 2-18, 2-19). When the brushes are not probing a row or when there is no card in the read stations, the roll remains deenergized. The pulse placed on the roll when a row is to be read is the probe signal, generated by the card-reader synchronizing circuits (section 4-14).

In order to probe the roll (sense the card) at the correct time, the generation of the probing pulse must be synchronized with the movement of the card. This timing is maintained by the timing disc and the circuits of the synchronizer.

The timing disc (2-1,3) contains 12 slots at 24-degree intervals around its circumference. The 96-degree interval between the first and last slot, called the gap, does not contain slots. When the card reader is running, the timing disc rotates and generates a timing-disc photocell signal each time a slot passes between the photocell (2-1,5) and its lamp. The timing disc rotates once for each card pass and generates 12 photocell signals per card, one for each row. The photocell signals go to the synchronizing circuits to generate pulses which probe both read stations simultaneously and thus read the cards. If no card is in the read station, the photocell signals do not generate any probe signals. Details concerning the generation of the probe signals are discussed in section 3-14.

Information from the read stations is assembled row by row as a card image in the card-buffer band, where it remains until a 96 instruction transfers it into main storage. Both transfer operations, from the read stations to the card-buffer band and from the card-buffer band to main storage, are discussed in section 3-36.

General information necessary for an understanding of card reader operation is discussed in the sections immediately following.

3-3. CARD CODE

Information read from punched cards by the card reader is usually in the six-bit card code described in section 1-2. In order to store a card-coded word in a card-buffer or a main-storage location, either of which accommodates one ten-digit word in the four-bit UCT code, each six-bit digit of the card-coded word is divided into two parts, designated primed and unprimed. The unprimed part of each ten-digit card-coded word consists of the four lower order bits of each digit, the bits from rows 5, 3, 1, and 0 of the card. Because it is the same size as a ten-digit word in four-bit UCT code, the unprimed part of a card-coded word can be stored in one word location in the card buffer or main storage. The primed part of the word consists of the two higher order bits of each digit, the bits from rows 9 and 7, and two unused bits. It is stored in another main-storage location.

Table 3-2 in the high-speed printer manual shows the complete card code for numerics, alphabetics and special characters. The table separates the primed and unprimed parts of each character.

3-4. IDENTIFYING CARD WORDS

To enable the programmer to identify the primed or unprimed part of a word assigned to a given main-storage location, a card is divided into areas identified with a special notation. Figure 3-1 shows how each punched card is divided. The columns 1 through 45 and 46 through 90 are numbered individually. The punch positions (for example, 1_2) are indicated, in the columns at the extreme right and left. The card is divided into ten blocks numbered 0 through 9. Blocks 4 and 9 each store a five-digit word in card code; each of the others stores a ten-digit word.

Each block is divided into two sections, one of which contains the unprimed and the other the primed parts of the characters in a word. The notation Jxx appearing in each block is the means of identification. The letter J distinguishes words read by the card reader from words designated I read by the read-punch; J identifies the unprimed parts and J' the primed parts. The first numeral, either a 1 or a 2, identifies the read station in which the information was read. The second numeral identifies the block of a particular card

from which the word was read. Because a card contains ten blocks, the second subscript may have any value between 0 and 9.

3-5. CARD BUFFER

The card-buffer band on the storage drum is used to store information temporarily during input-output operations. The card-buffer band is necessary because of the difference in speed between the relatively slow input-output operations and the fast rate of computation. The card-buffer band also provides a storage area to assemble into complete words the information read row by row from the cards. While information read in the two read stations is recorded in the card-buffer band, the processor is free to carry out other instructions because the read-write circuits which serve main storage are not involved in a transfer of information from reader to buffer. After the information is recorded in the card buffer, it can be transferred to main storage in one drum revolution.

The card-buffer band consists of four tracks. It is served for reading and writing operations by two headbars, each consisting of four heads, one for each track. These headbars are referred to as head 1 and head 2. Head 1 and head 2 are displaced by 180 degrees, as shown in figure 3-2.

Both the card reader and the read-punch unit use the card-buffer band for buffer storage. The card-buffer band is not part of main storage, but it contains 200 word locations just as do each of the 25 main-storage bands. Locations 000-099 of the card-buffer band serve the card reader, while locations 100-199 serve the read-punch unit. Only those operations concerning the card-reader half of the band are discussed in detail in this manual.

Head 1 is used for reading and writing operations for both the card reader and the read punch. Head 2 can be used to read information from either half of the card-buffer band but can be used for writing only in the card-reader half. The circuits are discussed in detail in section 3-17.

3-6. SENTINELS

Sentinels control the transfer of information between the card reader and the card-buffer band, and between the card-buffer band and main storage. Refer to section 3-86 of the central processor manual for a complete description of a sentinel. Each sentinel consists of a timing signal from the cycling unit and one or more TS signals from one of the four tracks of the timing band, and is stored in one or more word locations of the timing band. For example, the R6 sentinel is made up of the t5B- signal from the cycling unit combined with the TS4 signal from the timing-band read circuit, and is stored in every fifth word location from 101, 106 through 196.

Table 3-1. Card-Reader Sentinels

Timing Signals	Timing-Band Signals			
	TS4	TS3	TS2	TS1
t9			BT	
t5	R6	R5		T0
t3		ST		
t2	G3*	G2*	G1*	

*Composite Sentinels:

R1 = $\overline{G1}$ G2 $\overline{G3}$
R2 = G1 G2 G3
R3 = $\overline{G1}$ $\overline{G2}$ G3
R4 = G1 $\overline{G2}$ G3

Table 3-1 shows all of the card-reader sentinels. The interlace patterns, tables 3-2 and 3-3, show the timing-band locations of these sentinels. Composite sentinels R1 to R4 combine several timing-band signals. For example, the R1 sentinel consists of three other sentinels: $\overline{G1}$, G2 and $\overline{G3}$. Sentinel G1 consists of the TS2 and t2 signals; sentinel $\overline{G1}$, therefore, consists of the $\overline{TS2}$ and t2 signal. Sentinel G2 consists of TS2 and t2. Sentinel G3 consists of TS4 and t2; sentinel $\overline{G3}$, therefore, consists of $\overline{TS4}$ and t2. A gate which is controlled by the R1 sentinel has the input signals $\overline{TS2}$, TS3, $\overline{TS4}$, and t2, as shown at gate 113, figure A-22.

3-7. CARD-INTERLACE PATTERN 1

Information words read in read stations 1 and 2 are recorded on the card-buffer band as shown in card-interlace pattern 1, table 3-2. The table shows the 200 storage locations of the card-buffer band, the locations in which the parts of card words are recorded, and the sentinels which control the writing. For example, J10, the unprimed part of the word in block 0 (figure 3-1) read in read station 1, is recorded in the 000 location of the card-buffer band. The primed part of the same block, J'10, is recorded in location 005. Sentinel R1 controls the writing of J10 into location 000; sentinel R2 controls the writing of J'10 into location 005. The information from the card reader is recorded in locations 000 through 099. Locations 100 through 199 are used for information from read punch. An ST sentinel initiates the transfer of information into the buffer. If the ST

Table 3-2. Card-Interlace Pattern 1 (Reader to Buffer-Band Transfer)

000	J10	R1	050	J22	R1	100		R1	150		R1
001	J15	R3	051	J27	R3	101		R3	151		R3
002			052			102			152		
003			053			103			153		
004			054			104			154		
005	J'10	R2	055	J'22	R2	105		R2	155		R2
006	J'15	R4	056	J'27	R4	106		R4	156		R4
007			057			107			157		
008			058			108			158		
009			059			109			159		
010	J20	R1	060	J13	R1	110		R1	160		R1
011	J25	R3	061	J18	R3	111		R3	161		R3
012			062			112			162		
013			063			113			163		
014			064			114			164		
015	J'20	R2	065	J'13	R2	115		R2	165		R2
016	J'25	R4	066	J'18	R4	116		R4	166		R4
017			067			117			167		
018			068			118			168		
019			069			119			169		
020	J11	R1	070	J23	R1	120		R1	170		R1
021	J16	R3	071	J28	R3	121		R3	171		R3
022			072			122			172		
023			073			123			173		
024			074			124			174		
025	J'11	R2	075	J'23	R2	125		R2	175		R2
026	J'16	R4	076	J'28	R4	126		R4	176		R4
027			077			127			177		
028			078			128			178		
029			079			129			179		
030	J21	R1	080	J14	R1	130		R1	180		R1
031	J26	R3	081	J19	R3	131		R3	181		R3
032			082			132			182		
033			083			133			183		
034			084			134			184		
035	J'21	R2	085	J'14	R2	135		R2	185		R2
036	J'26	R4	086	J'19	R4	136		R4	186		R4
037			087			137			187		
038			088			138			188		
039			089			139			189		
040	J12	R1	090	J24	R1	140		R1	190		R1
041	J17	R3	091	J29	R3	141		R3	191		R3
042			092			142			192		
043			093			143			193		
044			094			144			194		
045	J'12	R2	095	J'24	R2	145		R2	195		R2
046	J'17	R4	096	J'29	R4	146		R4	196		R4
047			097			147			197		
048			098		ST	148			198		ST
049			099			149			199		

SENTINEL

CARD WORD

STORAGE LOCATION

Table 3-3. Card-Interlace Pattern 2 (Buffer-Band to Main-Storage Transfer)

000		R5	050		R5	100			150		
001	J10		051	J22		101		R6	151		R6
002			052			102	J15		152	J27	
003			053			103			153		
004			054			104			154		
005		R5	055		R5	105			155		
006	J'10		056	J'22		106		R6	156		R6
007			057			107	J'15		157	J'27	
008			058			108			158		
009			059			109			159		
010		R5	060		R5	110			160		
011	J20		061	J13		111		R6	161		R6
012			062			112	J25		162	J18	
013			063			113			163		
014			064			114			164		
015		R5	065		R5	115			165		
016	J'20		066	J'13		116		R6	166		R6
017			067			117	J'25		167	J'18	
018			068			118			168		
019			069			119			169		
020		R5	070		R5	120			170		
021	J11		071	J23		121		R6	171		R6
022			072			122	J16		172	J28	
023			073			123			173		
024			074			124			174		
025		R5	075		R5	125			175		
026	J'11		076	J'23		126		R6	176		R6
027			077			127	J'16		177	J'28	
028			078			128			178		
029			079			129			179		
030		R5	080		R5	130			180		
031	J21		081	J14		131		R6	181		R6
032			082			132	J26		182	J19	
033			083			133			183		
034			084			134			184		
035		R5	085		R5	135			185		
036	J'21		086	J'14		136		R6	186		R6
037			087			137	J'26		187	J'19	
038			088			138			188		
039			089			139			189		
040		R5	090		R5	140			190		
041	J12		091	J24		141		R6	191		R6
042			092			142	J17		192	J29	
043			093			143			193		
044			094			144			194		
045		R5	095		R5	145			195		
046	J'12		096	J'24		146		R6	196		R6
047			097			147	J'17		197	J'29	
048			098			148			198		
049			099			149			199		BT TO

SENTINEL

CARD WORD

STORAGE LOCATION

sentinel in location 098 starts the transfer, the R1 sentinel in location 100 controls the writing of J10 into location 000; if the ST sentinel in location 198 starts the transfer, the R1 sentinel in location 000 controls the writing of J10 into location 000. The only difference between control by the R1 sentinel in location 100 and the one in location 000 is that they cause different heads to write into the card buffer. No matter which of the two ST sentinels starts the transfer, or which R1 sentinel controls writing J10, the J10 word is always recorded in location 000. Sentinels R1, R2, R3, R4 and ST control the transfer of information to the card buffer.

3-8. CARD-INTERLACE PATTERN 2

Information transferred from the card-buffer band to main storage is recorded in the band selected by the programmer as shown in card-interlace pattern 2 (table 3-3). The information which was recorded in 100 locations of the card-buffer band is recorded in the 200 locations of the selected main-storage band. As shown in interlace pattern 2, the sentinels which control the transfer of information from the card-buffer band to main storage are R5, R6, BT and T0. The BT sentinel controls the beginning of the transfer operation; the T0 sentinel indicates that transfer is over and controls the ending of the operation.

3-9. MECHANICAL COMPONENTS

The card reader consists of three interrelated mechanical systems: the card input system, the card transport system, and the output stacking system. A detailed discussion of the functions of the three systems follows.

3-10. INPUT SYSTEM

Input cards are placed in the input bin (2-3,3), which holds 1000 cards. Each time a 72 instruction is executed, the pickerknife pushes a card from the bottom of the stack in the input bin into the card transport system. Refer to section 2-2 for a physical description of the pickerknife mechanism.

The pickerknife (2-3,9) is a blade attached to the rear face of the feed arm, projecting approximately 0.005 inch above the card bed. The pickerknife mechanism is shown in figure 3-3. The pickerknife latch prevents the pickerknife from pushing a card into the transport system until a 72 instruction is given. When the instruction is given to feed one card to the card reader, the solenoid plunger attracts the pickerknife latch so that the pickerknife is pushed back by the cam, allowing it to pick up a card. Next, as the cam rotates, the pickerknife is pulled forward by the tension of the feed spring and pushes a card into the transport system.

As shown in figure 3-3a, the pickerknife latch is adjusted so that the cam touches the cam follower 42 degrees of rotation before the peak of the hump on the cam. At this point, the 0.010-inch symmetrical hump begins and continues to 42 degrees past the peak of the hump. Whenever the hump on the cam comes into the position shown in figure 3-3a, it makes contact with the cam follower. During the positions of the rotation of the cam when the hump does not make contact with the cam follower, the cam follower is held away from the cam by the pickerknife latch. In figure 3-3a, feed-spring tension holds the pickerknife latch plate against the latch arm. In figure 3-3b, the hump of the cam moves the feed arm, moving the latch plate away from the latch arm. Unless a 72 instruction is given, the pickerknife latch remains as shown in figure 3-3b and prevents contact between cam and cam follower during the remainder of the rotation of the cam. Thus, when the card reader is turned on, the pickerknife moves back and forth 0.010-inch each time the cam follower rides the hump on the cam.

If a 72 instruction is given when the peak of the cam hump engages the follower, the pickerknife latch is pulled to the solenoid as shown in figure 3-3c, and the tension of the feed spring causes the cam follower to follow the cam during the remainder of the rotation. The pickerknife comes in contact with the trailing edge of the bottom card in the input bin and pushes the card between the rollers. When the card reaches the rollers, it automatically goes through the two read stations and into the output stacker indicated by the program.

3-11. TRANSPORT SYSTEM

The card transport system consists of seven pairs of rollers equidistant along the horizontal card bed. One roller of each set is mounted above the card bed and the other below. The rollers are described in detail in section 2-15.

The feed motor supplies mechanical power to the feed rollers as well as the feed arm. Transmission is by a timing belt (2-5,9) looped over eight timing pulleys (2-5,8) and held taut by seven idler bearings (2-5,7). One timing pulley is fitted on the end of each of the seven lower rollers. Each lower roller has at one end a small helical gear (2-3,5) that meshes with a similar gear on the corresponding upper roller (2-3,4) and functions to drive the rollers in opposite directions. The upper roller moves counterclockwise, viewed from the front of the unit.

The pickerknife forces a card between the first set of pressure-loaded rollers. The rollers then transport the card through the reader to the output stackers.

3-12. OUTPUT SYSTEM

On the left side of the reader at the end of the card path are three 1000-card-bins called output stackers and designated stacker 2, stacker 1, and stacker 0 (2-2,18,17 and 16). The card reaches stacker 2 first.

Immediately below the card bed, above stacker 2 and stacker 1, are two solenoid-actuated stacker selectors (2-5,6). When a 47 instruction selects one of the output stackers, the selector of the chosen stacker pivots upward into the path of the card and directs the card into the stacker below. Once a selector has been actuated, the same stacker continues to receive cards until another 47 instruction selects a different stacker.

Cards fall on the stacker platform at the bottom of the output stacker. The stacker platforms are spring-loaded, and depress under the weight of the cards. When one of the stackers has received approximately 1000 cards, a bracket attached to the stacker platform trips a switch and produces a signal which stops the system.

3-13. ELECTROMECHANICAL OPERATIONS

While the mechanical system transports the card through the card reader as described in section 3-11, certain electromechanical functions take place. This section explains the two most important electromechanical operations of the card reader, which concern the read stations: the generation of the probe signals which pulse the rolls, and the sensing of punched holes by the brushes.

3-14. GENERATION OF PROBE SIGNALS

Each time a row of information is to be sensed in the read stations, a probe signal is sent to the two rolls in the sensing stations (figure 3-4). Twelve probe signals are needed to sense the 12 rows of a card. The roll in read station 1 receives a pulse at the same time as the roll in read station 2, because read station 1 senses row 1 of a card at the same time that read station 2 senses row 1 of another card.

The generation of the probe signals depends upon the timing disc. Each time one of the 12 slots on the rotating timing disc passes the photocell, a timing-disc photocell signal is generated. Each timing-disc photocell signal causes the generation of a probe signal each time a row of information is to be sensed in the read station. The 12 slots in the timing disc correspond to the 12 row positions of cards being read.

The delay-flop (DF) generates a PCS signal for every timing-disc photocell signal it receives, 12 PCS signals for each revolution of the timing disc. Each PCS signal steps the row counter, a circuit which counts from 1 through 12 to indicate which row is being read in the read stations.

The retriggerable delay-flop (RDF) generates only one signal, the clear-counter signal, generated when the gap in the timing disc passes the photocell. The clear-counter signal steps the card-cycle counter, which counts from one through four to indicate how far the card has progressed through the card reader (section 3-27).

The mechanical movement of the card is synchronized with the electrical signals necessary to sense a card. The Row 9 signal from the row counter sets the pickerknife flip-flop (figure 3-4), so that on the following Row 3 signal the pickerknife pushes a card into the roller mechanism. On the following Row 1 signal, row 1 of the card is under the brushes.

The pickerknife is actuated by the pickerknife flip-flop, which also sends a signal to the card-cycle counter. With the clear-counter signal, the pickerknife signal forces the card-cycle counter to one, indicating that a card is on its way to the first read station. The second clear-counter signal steps the card-cycle counter to a count of two, during which a CCC3 output from the counter indicates that a card is in the first read station. The 12 slots on the timing disc generate 12 PCS signals which make the row counter count from one through 12. The CCC3 signal and a row-counter signal are inputs to the probe generator. Each time a row-counter signal is sent to the probe generator, a probe signal pulses the rolls in read stations 1 and 2 to sense the 12 rows of the card in read station 1. If this card is the first to be fed, read station 2 is empty, and all of the brushes make contact with the pulsed roll under the card bed. The next time the gap on the timing disc passes the photocell, the clear-counter signal steps the card-cycle counter to a count of three, during which the output of the counter is the CCC4 signal. The next 12 PCS signals from the photocell step the row counter from one through 12 so that the 12 rows can be sensed. If cards are in both read stations, both the CCC3 and CCC4 signals are inputs to the probe generator.

The probe signal is generated, then, only when both the following conditions are fulfilled:

(1) An input to the probe generator is a CCC3 signal, a CCC4 signal, or both, indicating that there is a card in one or both read stations.

(2) An input to the probe generator is one of the 12 row-counter signals, indicating that one of the 12 rows of a card is under the brushes in one or both read stations.

3-15. BRUSH SENSING

As cards travel through the card reader they pass two sets of brushes, one in each read station. Read station 1 (2-3,18), the read station, is located between the first and second sets of transport rollers. Read station 2 (2-3,19), the check station, is located between the second and third sets of rollers.

The two stations are identical. Each consists of a conductive roll under the card bed (2-4,5) with a block of 45 small steel brushes above the bed (2-6,2). Each brush corresponds to a column of information on the card (section 1-2).

Under control of the card-reader synchronizing circuits, the brush probe generator places an electrical pulse on the roll while the brushes probe a card row. If there is no hole in the card at the position sensed by a given brush, the brush is insulated from the roll and does not receive a signal. The absence of a signal on any brush at the time of the probe signal corresponds to a 0 bit. A hole in the card allows a brush to make contact with the roll and receive a signal corresponding to a 1 bit. In this way, information is converted from holes punched in cards to electrical pulses.

3-16. LOGICAL COMPONENTS

This section of the manual explains the logical components of the card-reader synchronizing circuits. The reader should be familiar with section II of the central processor manual, which explains the basic logical elements of the synchronizing circuits. The text in this section should be read with the appropriate logical drawings in Manual No. 2. A list of the logical drawings and the corresponding engineering drawings is given in the front of this manual.

3-17. CARD-BUFFER CIRCUITS

The read and write circuits of the card buffer are shown in figures A-22 and A-23. These circuits are identical in operation to the read and write circuits of main storage, described in sections 3-87 and 3-93 of the central processor manual and shown in figures A-18 and A-19. Card-buffer band I (figure A-22) is composed of the circuits which control reading and writing with head 1. Card-buffer band II is composed of the circuits for head 2. These circuits are therefore referred to as head 1 and head 2.

The buffer circuits include the read and write circuits, the read and write flip-flops, and the head-indicator flip-flop. These circuits are shared by the read-punch unit. Only the read-punch unit uses the read stop flip-flop on card-buffer band I, which is described in the manual for that device.

3-18. HEAD-INDICATOR FLIP-FLOP. The head-indicator flip-flop (figure A-22) controls the selection of a head to read from or write into the card-buffer band. Because the card reader and read-punch unit share the card-buffer band, the time required for reading is minimized by alternating control between heads 1 and 2, which serve both buffer areas. While one head is energized to read or write from one buffer area, the other head can be energized to read or write from the other buffer area.

The head-indicator flip-flop is controlled by gate 413, which samples the most significant digit of each timing-band address. (Refer to the central processor manual, sections 3-82, 3-84, and figure 3-3.) The TS1 signal at t2B- indicates the value of the digit. If the 100-199 half of the drum is under the timing-band read head, the most significant digit of the timing-band address is a 1, converted by the timing-band read circuits to a low TS1 signal. If the 000-099 half of the drum is under the timing-band read head, the most significant digit is a 0, which becomes a high TS1 signal when read in the timing-band read circuits.

When the card-reader half of the card-buffer band is under head 1, as shown in figure 3-2a, the TS1 signal is high (0). The high TS1 signal blocks gate 413, restoring the head-indicator flip-flop and generating low H1 and high H2 signals. Successive TS1 signals keep the flip-flop restored for one-half drum revolution. At the end of this half of the drum revolution, the read-punch half of the card-buffer band is under head 1 as shown in figure 3-2b. During the next half of the drum revolution, the TS1 signal at t2B is low (1) making gate 413 permissive at t2B, setting the flip-flop. The head indicator flip-flop generates low H2 and high H1 signals for one-half drum revolution.

To summarize, the outputs of the head-indicator flip-flop indicate which half of the card-buffer band is under head 1. When the card-reader half of the card-buffer band (locations 000-099) is under head 1, the H1 signal is low; when the read-punch half of the card-buffer band is under head 1, the H2 signal is low.

In the head 1 circuits (figure A-22), the low H1 signal alerts gates which control reading from and writing into the card-reader buffer. The low H2 signal alerts gates which control the read-punch buffer read-write circuits. In the head 2 circuits (figure A-23), the low H1 signal alerts gates which control the read-punch buffer read circuits; the low H2 signal alerts gates which control the card-reader buffer read-write circuits.

3-19. HEAD 1. The circuits which control the read and write operations of head 1 are shown in figure A-22. Head 1 is used to write into and read from either half of the card-buffer band. Certain of the input gates of the write and read flip-flops and the write input circuits operate when head 1 is over the card-reader half; others operate when head 1 is over the read-punch half. To write with head 1 when it is over the card-reader buffer, the write flip-flop must be set, the write pedestal must be generated, and the write input gates must be alerted to the ten bits being shifted out of the shift register. The logical components associated with head 1 are as follows:

(1) WRITE FLIP-FLOP. When information is to be written into the card-reader half, gates 110 through 113 control the write flip-flop. When gate 113 operates, the write flip-flop is set to write the bits of the unprimed words from the upper field. The gate is made permissive by an R1 sentinel and the signal indicating rows 1 through 4, upper field. Gate 113 sets the write flip-flop 40 times (four rows times ten groups).

When gate 112 operates, the write flip-flop is set to write the bits of the primed words from the upper field. The gate is made permissive by an R2 sentinel and the signal indicating rows 5 and 6, upper field. Gate 112 sets the flip-flop 20 times (two rows times ten groups).

Gate 111 sets the flip-flop 40 times to write the bits of the unprimed words from the lower field. The gate is made permissive by an R3 sentinel and the signal indicating rows 1 through 4, lower field.

Gate 110 sets the flip-flop 20 times to write the bits of the primed words from the lower field. The gate is made permissive by an R4 sentinel and the signal indicating rows 5 and 6, lower field.

All four gates are alerted by the FFR1 signal and the low H1 signal which indicates that head 1 is over the card-reader half. The flip-flop is set at t3B, at which time the p0 digit is on the SR1 lines from the shift register. It is restored at gate 101, which operates at t1B.

(2) WRITE GATES. Sensed information enters the write circuits of head 1 at write input gates 210, 207, 204 and 201 on the SR1 line coming from the shift register. The coder input gates 241, 244, 246, and 247 must also be alerted to write the sensed information into the card-reader buffer.

Because the information is sensed from one row of the card, it is written into only one track of the buffer. Both a write input gate and a coder input gate must be made permissive to write information into one track. The other tracks are blocked from writing or are forced to write zeros. For example, if write input gate 210 and coder input gate 241 are both permissive, information is written into track 1. A 0-bit

input on the SR1 line is high at gate 210; a 1 bit is low at gate 210. If both gates are blocked, nothing is written into track 1.

Gates 207 and 244 are made permissive to write into track 2; gates 204 and 246 to write into track 3; and gates 201 and 247 for track 4.

All of the coder input gates are made permissive by the following signals:

(a) the set output of the write flip-flop

(b) the H1 signal from the head-indicator flip-flop indicating that the card-reader buffer (locations 000-099) is under head 1

(c) the FFR1 signal indicating that the card-reader circuits are in control of head 1

(d) row signals indicating the row being written.

The row signals and the H1 signal also alert the write input gates. Therefore, if either of these signals is high, both the write input gate and the coder input gate are blocked and nothing is written into a track.

The least significant bits of the primed or of the unprimed words (0$\underline{0}$ 000$\underline{0}$) from either card field are sent on the SR1 line to gate 210 to be written into track 1. The second lowest order bits of the primed or of the unprimed words (0$\underline{0}$ 00$\underline{0}$0) from either card field are sent to gate 207 to be written into track 2. The second highest order bits (00 0$\underline{0}$00) of the unprimed words from either card field are sent to gate 204 to be written into track 3. The most significant bits (00 $\underline{0}$000) of the unprimed words from either card field are sent to gate 201 to be written into track 4.

When information is written into track 2, the high signal from gate 244 is sent to the write circuits of track 3 and track 4 to write zeros in these tracks. This provision for writing of zeros insures that the two most significant bits of all primed words are 0 bits.

(3) READ FLIP-FLOP. After the card-reader half of the buffer is loaded with sensed information, a 96 instruction is given to transfer the information from the buffer to main storage. The information read from the card-reader half (000-099) of the buffer is written into the whole main-storage band (000-199) in one drum revolution. During the first half of the revolution, head 1 reads from the buffer; during the second half, head 2 reads from the buffer.

During reading from the card-reader buffer with head 1, the read flip-flop is controlled by gate 305. The gate is alerted by FS 98 which is generated by the 96 instruction. The gate is made permissive by the H1 signal from the head-indicator flip-flop and the R5 sentinel, which appears on card-interlace pattern 2 (table 3-3) before each primed or unprimed word which is to be recorded in the first half (000-099) of the selected main-storage band. The read flip-flop is set 20 times. Each time it is set a word is read from the buffer and written into a specific location in the first half of the main-storage band. The set output of the read flip-flop, low RSC5, sets the write flip-flop of main storage (figure A-19). The low BLRE1 signal alerts the read output gates. During the 96 instruction, the read flip-flop is restored at gate 302.

The function of the read flip-flop during reading by head 2 is discussed in section 3-20.

3-20. HEAD 2. The circuits which control the read and write operations of head 2 are shown in figure A-23. Head 2 is used to read from either the card-reader half or the read-punch half of the card buffer, and to write into the card-reader half.

To write with head 2 into the card-reader half of the card buffer the write flip-flop must be set, the write pedestal generated, and the write input gates alerted to the ten bits being shifted out of the shift register.

(1) WRITE FLIP-FLOP. The write flip-flop is set by gates 100 through 103, which are made permissive by the same signals as gates 110 through 113 on head 1 (section 3-19) except that the H2 signal is required to indicate that head 2 is over the card-reader buffer. The flip-flop is restored at gate 104, which operates at t1B.

(2) WRITE GATES. Sensed information enters the write circuits of head 2 at write input gates 108, 110, 112, and 114 on the SR1 line coming from the shift register. The coder input gates, 116 through 123, must also be alerted to write the sensed information into the card-reader buffer. Because the information is sensed from one row of the card, it is written into only one track of the buffer. Both a write input gate and two coder input gates must be made permissive to write information into a track. If all three gates are blocked, nothing is written; if only the write input gate is blocked, zeros are written.

For example, if write input gate 108 and coder input gates 116 and 117 are all permissive, information is written into track 1. A 0-bit input on the SR1 line is high at gate 108, and a 1 bit is low at the same gate. If all three gates are blocked, nothing is written into track 1; if gate 108 is blocked, zeros are written. Gates 110, 118 and 119 are made

Table 3-4. Head 2 Control

Information	Track			
	1	2	3	4
00 0000	Information	Nothing	Zeros	Zeros
00 0000	Nothing	Information	Zeros	Zeros
00 0000	Nothing	Nothing	Information	Zeros
00 0000	Nothing	Nothing	Nothing	Information

permissive to write information into track 2; gates 112, 120, and 121 to write into track 3, and gates 114, 122, and 123 for track 4.

Table 3-4 shows what is written into each track for a given transfer.

The least significant bits (00 0000) of the primed or unprimed words from either card field are sent on the SR1 line to gate 108 to be written into track 1. Gate 108 is made permissive by the low R1,5 signal, indicating that the row counter is on a count of one or five; a low H2 signal from the head-indicator flip-flop, and a low RS1 signal which indicates that information is being shifted out of the register into the SR1 line. Gates 116 and 117 are also made permissive by the low R1,5 signal and the low set output of the set write FF. When information is written into track 1, nothing is written into track 2 because all three gates are blocked by the high R2,6 signal. Zeros are written into track 3 because coder input gates 120 and 121 are made permissive by a low $\overline{R4}$ signal from the row counter and write input gate 112 is blocked by a high R3 signal. Zeros are written into track 4 because coder input gates 122 and 123, which require no row counter signal, are permissive. Write input gate 114 is blocked by the high R4 signal from the row counter.

The second lowest order bits (00 0000) of the primed or unprimed words from either card field are sent on the SR1 line to gate 110 to be written into track 2. Gate 110 is made permissive by the low R2,6 signal, indicating that the row counter is on a count of two or six; a low H2 signal, and a low RS1 signal. Gates 118 and 119 are also made permissive by the low R2,6 signal and the low set output from the set write FF. Again 0 bits are written into tracks 3 and 4, but nothing is written over the information on track 1 because all three gates are blocked by the high R1,5 signal.

The second highest order bits (00 0000) of the unprimed words from either card field are sent on the SR1 line to gate 112 to be written into track 3. Gate 112 is made permissive by the low R3 signal, indicating that the row counter is on a count of three; a low H2 signal, and a low RS1 signal. Gates 120 and 121 are also made permissive by the low R4 signal, indicating that the row counter is not on a count of four, and the low set output from the set write FF. Again 0 bits are written into track 4 and nothing on tracks 1 and 2.

The most significant bits (00 0000) of the unprimed words from either card field are sent on the SR1 line to gate 114 to be written into track 4. Gate 114 is made permissive by the low R4 signal, indicating that the row counter is on a count of four; a low H2 signal, and a low RS1 signal. Gates 122 and 123 are also permissive. Nothing is written into tracks 1, 2, or 3 because all gates are blocked by high signals from the row counter.

(3) READ FLIP-FLOP. After the card-reader buffer is loaded with sensed information, a 96 instruction is given to transfer the information from the buffer to main storage. Head 2 reads during the second half of the drum revolution needed to transfer the information. During the 96 instruction, gate 201 of the read flip-flop is alerted by FS 98. The gate is made permissive by the H2 signal from the head-indicator flip-flop and the R6 sentinel, which appears on interlace pattern 2 (table 3-3) before each primed or unprimed word which is to be recorded in the second half (100-199) of the selected main-storage band. The read flip-flop is set by gate 201 20 times; each time it is set a word is read from the buffer and written into a specific location in the second half of the main-storage band.

The set output of the read flip-flop, low RSC2, sets the write flip-flop of main storage (figure A-19). The low BLRE2 signal alerts the read output gates. During the 96 instruction the read FF is restored at gate 202.

3-21. CARD-READER CONTROL CIRCUITS

The card-reader control circuits described below are shown in figure A-24.

3-22. SYNCHRONIZING FLIP-FLOPS. Two flip-flops synchronize the photocell and clear-counter signals from the card-reader timing disc with processor timing.

(1) SYNCHRONIZING FLIP-FLOP 1. When the gap on the timing disc passes the photocell, a clear-counter signal makes gate 239 permissive at t8B of an EW word to set synchronizing flip-flop 1. Every other word, starting from location 001 on the timing band, is referred to as an EW word. (The every-other-word flip-flop is described in section 3-85 of the central processor manual.) At t7B of the next EW word, gate 302 is made permissive to generate a high signal which clears

the six flip-flops of the row counter and restores synchronizing flip-flop 2.

At t8B of the same EW word, gate 301 is made permissive to generate a high signal which forces the row counter to indicate row 12; that is, it generates low signals LF and R6 from the field flip-flop and the row counter. The row counter must be forced to indicate row 12 before it can be stepped to indicate row 1. When the first notch on the timing disc generates the first photocell signal, a stepping pulse steps the counter to 1. The high signal generated by gate 301 generates RPC through buffer 243. The RPC signal clears the card-cycle counter and restores synchronizing flip-flop 1. The high output of gate 301 generates a low SCCC signal to alert the set gates of the card-cycle counter flip-flops, which can then be made permissive by the set output of the pickerknife flip-flop.

(2) SYNCHRONIZING FLIP-FLOP 2. The first photocell signal after the gap on the timing disc makes gate 200 permissive at t10B of an EW word to set synchronizing flip-flop 2. The set output alerts restore gate 107 of the pickerknife flip-flop and alerts gate 203, which is made permissive at t10B of the next EW word.

The high signal generated by gate 203 becomes a low SRC (step row counter) signal. The SRC signal at gate 206 and gate 234 steps the row counter and field flip-flop, which are indicating row 12 (signals LF and R6), to the next count, indicating row 1 (signals R1 and UF). The high output from gate 205 restores synchronizing flip-flop 2 in preparation for the next photocell signal.

Each of the 12 photocell signals generated by the timing disc sets synchronizing flip-flop 2. As a result, the row counter is stepped from one through six (signals R1 through R6) with the UF signal present, indicating rows 1 through 6, and then from R1 through R6 with the LF signal present, indicating rows 7 through 12. The SRC signal also alerts set gate 256 of the probe flip-flop.

3-23. ROW COUNTER. The operation of the row counter depends upon the revolving timing disc rather than upon the feeding of cards. The counter operates as long as the card reader is turned on. The row counter indicates which of the 12 rows the read stations are reading. The row counter consists of six flip-flops, the outputs of which indicate rows 1 through 6 of either field on a card. The card-reader field flip-flop indicates which of the two fields is being read. Outputs R1 through R6 and UF indicate rows 1 through 6, while R1 through R6 outputs and LF indicate rows 7 through 12. A counter circuit similar to the row counter is described in section 2-34 of the central processor manual.

As long as the timing disc rotates, photocell signals are fed to gate 200, the set gate of synchronizing flip-flop 2. Each photocell signal, therefore, steps the row counter once. Each time the row counter is stepped, gate 256 is made permissive, provided that a card is in one or both of the read stations, and a generate-clear-and-probe pulse is placed on the sensing rollers.

The set outputs of the row-counter flip-flops, R1 through R6, alert the input gates of the buffer write circuits, and time the operations of various logical components of the card reader. The row indicator (figure A-24) converts the high R'1 through R'6 set output signals into combinations of row signals.

3-24. READER FIELD FLIP-FLOP. The card-reader field flip-flop (figure A-24) operates with the row counter to count rows 1 through 12 of a card. The row counter counts from one to six, the number of rows in one card field; the field flip-flop distinguishes which of the two card fields is being read. The set output, a low LF signal, indicates the lower field; the restore output, a low UF signal, indicates the upper field. The clear-counter signal at buffer 238 jams the flip-flop to the set condition (LF low). At the same time the row counter is jammed to six at buffer 233. The R6 signal and the set output (LF) restore the field flip-flop at gate 234, which is alerted by the SRC signal from the first photocell. The flip-flop stays restored (UF low) during row counts one through six. When the seventh photocell signal occurs, gate 206 is made permissive, setting the field flip-flop. The UF and LF signals, with the row counter outputs, control the timing of various logical components.

3-25. INTERLOCK FLIP-FLOP 1. Interlock flip-flop 1 stores the indication that a 72 instruction (feed one card) has been staticized until the pickerknife can be actuated to feed a card. Function signal 28 of the staticized 72 instruction alerts gate 119, which is permissive if the Jam I2B signal is low. Since the Jam I2B signal is high only when an abnormal condition exists, the low Jam I2B signal indicates that the reader is operating correctly. The low INT1 set output of the flip-flop alerts set gate 109, which is permissive at the time the row counter is stepping to ten, when the pickerknife can feed another card. When gate 109 operates, setting the pickerknife flip-flop, connecting diode 111 sends a high signal to gate 120, restoring the interlock 1 flip-flop. The IRC signal can also restore the flip-flop to prevent the feeding of cards if the cards are not registering correctly.

To minimize the time that a 72 instruction occupies the static register, the static-register flip-flops are cleared before FS 28 makes set gate 119 permissive at t11B. At t9B, FS 28 alerts gate 111 of the ending-pulse circuit (figure A-2) to generate an ending pulse, clearing the register.

If the previous 72 instruction has been staticized but not executed, the interlock flip-flop remains set and the high INT1 signal blocks gate 111 so that the 72 instruction is not cleared from the static register. At t9B, FS 28 and the low INT1 signal make gate 66 (figure A-4) permissive to generate a high CCT signal at t10A and FS 64 at t10B. The CCT signal is sent to buffer 105 (figure A-2) to generate a high Jam I2B signal at t10B. The Jam I2B signal and FS 64 change the reading in the static register from 72 (1010 0010) to 23 (0010 0011). The Jam I2B signal restores flip-flops 5 and 8, and FS 64 sets flip-flops 1 and 2. The reading of 23 is the second stage of the test instruction (22), which transfers the contents of register C into register A and sets the CT FF so that the next instruction is read from the storage location designated by m. (Refer to the analysis of instructions manual for a detailed description of the second stage of the 22 instruction.) The 72 instruction in register C is therefore transferred to register A and the next instruction is taken from the m address of the 72 instruction.

3-26. PICKERKNIFE FLIP-FLOP. The pickerknife flip-flop controls the actuation of the pickerknife. Each time this flip-flop is set, the pickerknife is actuated and a card is fed. When the INT1 signal at set gate 109 of the pickerknife flip-flop is low, it indicates that the interlock flip-flop is set; that is, that a 72 instruction has been given. The other inputs to set gate 109 are the LF and R3 signals, indicating row 9. The pickerknife flip-flop can be set only when the row counter is indicating row 9 and stepping to row 10, as indicated by the step-row-counter signal (SRC), so that when the card arrives at the first read station, row 1 of the card is under the brushes at the same time that the roll is pulsed.

The set output of the pickerknife flip-flop sets the card-cycle counter to a count of one, indicating that a card has been sent to the read station. The flip-flop can be restored at gate 107 at t10B of an EW word following the photocell signal for row 10 unless a new 72 instruction has not been given.

3-27. CARD-CYCLE COUNTER. The card-cycle counter counts the four card cycles of each card as it progresses from the input bin to one of the output stackers. When the first flip-flop of the card-cycle counter is set, generating a low CCC2 signal, the card is on its way to read station 1; when the second flip-flop is set (CCC3 is low), the card is in read station 1; when the third flip-flop is set (CCC4 is low), the card is in the read station 2; and when the fourth flip-flop is set (CCC5 is low), the card is on its way to one of the output stackers. More than one of the four flip-flops of the card-cycle counter can be set at one time.

The first flip-flop is set at gate 246 by the low set-output signal of the pickerknife flip-flop and an SCCC signal (step card cycle counter). Once per timing-disc revolution, when the gap between timing disc slots occurs, the SCCC signal

is generated whether or not a card has been fed. The pickerknife signal is present only when the pickerknife flip-flop is set, indicating that the pickerknife has fed a card. Because the card-cycle counter can be stepped to CCC3, CCC4, and CCC5 only if it first indicates CCC2, it operates only when a card has been fed.

The CCC3 and CCC4 signals from the card-cycle counter which indicate, respectively, that a card is in read station 1 or read station 2 are inputs to buffer 255. The output of the buffer is one of the two inputs to set-gate 256 of the probe flip-flop. A high RCCC3 input to gate 250 restores the CCC3 flip-flop of the card-cycle counter if read station 1 is empty because of an empty input bin. As a result, the probe signal is not generated.

3-28. PROBE FLIP-FLOP. The probe flip-flop generates the generate-clear-and-probe signal which pulses the sensing rolls whenever a row of information is to be sensed. The signal is generated only if there is a card in at least one read station and a row is in position to be read. Set-gate 256 requires a low signal from buffer 255 and a low SRC signal which is generated by each photocell signal. Buffer 255 generates a low if signal CCC3, signal CCC4, or both are present to indicate a card in one or both stations.

3-29. COLUMN-GROUP COUNTER. The column-group counter determines which of ten groups of bits is to be transferred from intermediate storage to the shift register. The group counter consists of ten flip-flops with outputs designated G1 through G10. Intermediate storage consists of 90 capacitors which store one row of information from read station 1 and one row of information from read station 2. Each row is 45 bits. The information is sent to the shift register ten bits at a time, in parallel. The group counter determines which group of ten bits is sent from intermediate storage to the shift register.

The counting sequence of the group counter is initiated by the intermediate-storage-loaded signal, which is an input to the first of the ten group-counter flip-flops. When intermediate storage is loaded, the intermediate storage loaded signal is low at gate 124, making the gate permissive at t3B of an EW word and setting the first flip-flop. The counter is stepped to indicate G2, G3, and so on, by stepping signals on the SS1 or SS2 line into buffers 155 and 156. The SS1 and SS2 signals are the restore outputs of the head-1 and the head-2 write flip-flop (figures A-22 and A-23). (The SCISA, SCISB, WRA and CLIA signals on buffers 155 and 156 are for keyboard input operations, which are described in section 4-48 of the central processor manual.) After ten bits are recorded in the card-buffer band the write flip-flop is restored and an SS1 or an SS2 signal is generated to step the column-group counter.

Signals G1 through G10 alert intermediate-storage gates 79 to 88 (figure A-25) to transfer a group of ten bits from intermediate storage into the shift register. Signals G2A, G4A, G6A, G8A, and G10A cause an initial shift on even groups of bits.

3-30. READER CONTROL FLIP-FLOP. The card-reader control flip-flop distinguishes between card-reader operations and the read-punch operations. The control flip-flop is set when head 1 or head 2 is to write information from intermediate storage into the card-reader half of the card-buffer band. It remains set for the one-half drum revolution between the ST sentinels in locations 98 and 198 of the timing band. Either ST sentinel alerts set-gate 104; the following ST sentinel alerts restore-gate 100. Set-gate 104 also requires the G1 signal which indicates that intermediate storage is loaded.

3-31. SAMPLE FLIP-FLOP. The sample flip-flop controls the transfer of sensed information from intermediate storage to the shift register. Because the reader-control flip-flop and the sample flip-flop share set-gate 104, the sample flip-flop is initially set by either of the ST sentinels, provided that intermediate storage is loaded. The Sample Pulse 1 signal is an input to gates 79 through 88 of the intermediate-storage circuit and, with one of the G1 through G10 signals, transfers a group of bits from intermediate storage to the shift register. After gate 104 sets it initially, the sample flip-flop is set by the stepping signals of the group counter, which are inputs to set-gate 123 at t2B. When sample flip-flop 1 is set initially, the SSP1 output is high; thereafter, the flip-flop is set at gate 123 and SSP2 is high. Both of these outputs clear the shift register at buffer 4 before each transfer from intermediate storage.

3-32. BUFFER-LOADED FLIP-FLOP. The state of the buffer-loaded flip-flop indicates whether the card-buffer band is loaded with information sensed as a result of a 72 instruction. The flip-flop is set, indicating that all rows have been written into the buffer, at gate 114 by the ST sentinel, a row-counter reading of 12 (signals LF, R6) and the FFR1 signal from the set reader-control flip-flop.

During the first step of the 96 instruction, given to transfer the buffer contents into a main-storage band, the state of the buffer-loaded flip-flop is tested at gate 10 of STR FF2. If the BL1 signal is low, indicating that the buffer is loaded, the 96 instruction steps to its second stage when the BT (begin transfer) sentinel arrives. When the transfer is completed, function signal 98 and the TO (transfer over) sentinel restore the buffer-loaded flip-flop.

During the 42 instruction, given to test whether a 96 instruction should be given, gate 113 of the static register is made permissive if the buffer-loaded flip-flop is restored (signal BL1 low).

3-33. INTERMEDIATE STORAGE

Information sensed by the brushes in the read stations is stored in intermediate storage, which consists of 90 capacitors, each storing one bit. The 45 brushes in read station 1 sense one row of information, 45 bits, at the same time that the 45 brushes in read station 2 sense the corresponding row of another card. The 90 bits sensed in the two read stations are stored in the 90 capacitors.

The 90 storage capacitors are divided into five odd and five even groups. As shown in figure 3-5, the five odd groups are bits sensed from the card in the first read station and the five even groups are bits sensed from the card in the second read station. Eight of the ten groups, J10 through J13 and J20 through J23, consist of ten bits each. The other two groups, J14 and J24, consist of 5 bits each.

From intermediate storage, the 90 bits sensed in the first row must be written into the first track of the card buffer before the second row is sensed. The writing requires one-half drum revolution.

The ten bits of each group in intermediate storage are transferred in parallel into the shift register, starting with the first odd group. After the odd group is shifted out of the shift register, an even group of ten bits is transferred to the shift register.

One of the odd groups of bits in the intermediate storage is shown in figure 3-6, with each bit identified by the digit position, p1 (LSB) through p10 (MSB), of which it is a part. The p10 bit of an odd group goes to FF10 of the shift register, p9 goes to FF9, and so on; that is, the bits of an odd group are transferred to the shift register in the order in which they are to be shifted out on the SR1 line.

The even groups of bits in intermediate storage, however, are not transferred to the shift register in the order in which they are shifted out. As shown in figure 3-7, the p10 digit of the even group goes to FF1 of the shift register, p9 goes to FF10, and so on. An initial shift pulse is required to shift all ten bits one flip-flop to the right before they are shifted out on the SR1 line to be written into the buffer. (Refer to section 3-34.)

When a card is read in the first read station the bits are sent to the shift register as odd groups. When the same card is read again in the second read station, the bits are sent as even groups. Sending the same bit over two different paths provides a check on the paths from intermediate storage.

Each group of ten bits is gated out of intermediate storage by a low Sample Pulse 1 signal and one of the signals G1 through G10 from the column-group counter. The first row is written into the card buffer within one-half drum revolution.

The second photocell signal senses the second row of both cards and the 90 bits are sent to intermediate storage. All 12 rows are transferred in this manner.

3-34. SHIFT REGISTER AND SHIFT FLIP-FLOP

The shift register converts the parallel input bits read from cards into serial form for storage in the card buffer. The ten input bits are sent to the ten flip-flops of the register, then shifted out one at a time into the buffer write circuits. Section 2-35 of the central processor manual describes a shift register.

A high, set output of the sample flip-flop, either signal SSP1 or signal SSP2, clears the shift register to receive each group of information bits from intermediate storage. If the group of bits from intermediate storage is an odd group, the bits are transferred in the order in which they are to be shifted out and no initial shift is necessary. If the group is an even group, however, an initial shift is necessary before the contents of the shift register can be written into the buffer. Initial shift takes place when a signal G2A, G4A, G6A, G8A, or G10A from the column-group counter indicates an even group of bits being transferred from intermediate storage. When any of these signals is high at buffer 100 (figure A-25), it makes gate 101 permissive. The R1 sentinel and signal FFR1 normally alert the gate, which operates only on even groups. The high output of gate 101 goes to buffers 4 and 5 to shift the bit of the p10 digit in FF1 (figure 3-7) to FF10 and to shift the other bits one flip-flop to the right. After initial shift, the bits can be sent to the buffer write circuits on the SR1 line.

When either of the write flip-flops of the card buffer is set, one of eight signals is generated according to which head is writing and which of the four set-gates of each flip-flop operates. One of these signals, EF1, EF2, EF3, EF4, EF'1, EF'2, EF'3, or EF'4, is sent to buffer 1 to set the card-reader shift flip-flop, which provides the shift pulses. The low RS1 signal from the set shift flip-flop alerts the write input gates of the card buffer.

The CLIA, SCISA, and SCI3, and WRA inputs are keyboard input signals. (Refer to section 4-48 of the central processor manual.)

3-35. SELECT-STACKER FLIP-FLOPS

The select-stacker flip-flops, shown in figure A-25, perform the following functions when set:

(1) FF1 holds the indication that a 47 instruction has been given to select stacker 2 until FF3 is set. Initially, FF1 is restored by high FS 33A at gate 63 whenever a 47 instruction is staticized. If the p7 digit of the 47 instruction is a 2, FS 33 and a Q2 signal set FF1 at gate 62. The

Q2 signal from the multiplier-quotient counter (figure A-14) indicates that stacker 2 is selected. The set output of FF1 alerts set-gate 65 of FF3.

(2) FF3 actuates the stacker-2 selector. The following signals set FF3 at gate 65: a CCC5 signal from the card-cycle counter, indicating that a card is moving toward the stackers; low signals SRC, LF, and R5, indicating that the row counter is stepping to 12; the set output of FF1, specifying stacker 2. All of the signals listed must be present. When FF3 is se the Select Stacker 2 signal causes the selector mechanism to pivot upward and drop the card into stacker 2. FF3 is restored at gate 39 when the row counter is stepped to row 3 as indicated by the low SRC, UF, and R2 signals at gate 37. If FF1 remains set, FF3 is again set.

(3) FF2 holds the indication that a 47 instruction has been given to select stacker 1 until FF4 is set. Initially, FF2 is restored by high FS 33A at gate 67 whenever a 47 instruction is staticized. If the p7 digit of the 47 instruction is a 1, FS33 and a Q1 signal set FF2 at gate 66. A low Q1 signal from the multiplier-quotient counter indicates that stacker 1 is selected. The set output of FF2 alerts set-gate 45 of FF5.

(4) FF5 delays the Select Stacker 1 signal until the card reaches stacker 1. The following signals set FF5 at gate 45: a CCC5 signal from the card-cycle counter, indicating that a card is moving toward the stackers: low signals SRC, LF, and R5, indicating that the row counter is stepping to row 12; the set output of FF2, specifying stacker 1. All of the signals listed must be present. FF5 remains set until row 8 is reached, providing a delay that enables the card to travel the added distance from stacker 2 to stacker 1 before the selector mechanism of stacker 1 operates. The indication of row 8, low signals Lf and R2, makes gate 41 permissive to set FF4 at buffer 44 and restore FF5 at gate 46.

(5) FF4 actuates the stacker-1 selector mechanism. A high signal from gate 41 sets FF4 at buffer 44, if FF5 is set. When FF4 is set, the Select Stacker 1 signal causes the selector mechanism to pivot upward to drop the card into stacker 1. FF4 is restored at gate 43 each time the row counter is stepped to row 3 as indicated by low signals SRC, UF, and R2.

3-36. NORMAL OPERATIONS

The normal operations of the card reader are controlled by three instructions: 72(CC); 96(W1); 47(Z). The 72 instruction feeds one card from the input bin into the continuously moving transport rollers and initiates reading and storing card information under the control of the synchronizing circuits. The control operations it initiates are included in the description of the instruction. The 96 instruction transfers the information from the card buffer to specific

locations in a main-storage band selected by the program. The 47 instruction selects an output stacker.

When a 72 instruction occurs in the program, one card is fed to the card reader. Read station 1 reads the card and transfers the information to the card-reader buffer. Before the same card is read in read station 2, a 96 instruction must be given to transfer the information from the card-reader buffer to a main-storage band specified by the program. When the first card is processed, read station 2 is empty. All of the brushes make contact with the sensing roll in read station 2, reading all ones, or meaningless information. The information from both read stations is transferred from the card-reader buffer to a main-storage band by the 96 instruction. The program ignores the main-storage location of the meaningless information.

When the first card is read again in read station 2, the information is automatically transferred to the card-reader buffer, as is the information from the second card read in read station 1. Another 96 instruction must be given to transfer the information from the card-reader buffer to main storage. The 47 instruction then selects the output stacker for the first card.

3-37. 72 INSTRUCTION

Under normal conditions, cards are processed through the card reader continuously. In order to show the synchronous control required for more than one card, this section describes the processing of two cards designated A and B.

After being read from main storage, the 72 instruction is staticized, generating FS 28 at t0B. If the interlock-1 flip-flop is restored, indicating that a card has been fed as a result of the previous 72 instruction, the low $\overline{\text{INT1}}$ output and FS 28 clear the static register. Function signal 28 also sets the interlock-1 flip-flop, which remains set until the pickerknife flip-flop is set, at the time shown in figure 3-8, to feed one card. The 72 instruction is staticized for only one word time, after which the processor is free to process other instructions. The synchronizing circuits which control and record the movement of the card through the reader, the sensing of the information in the two read stations, and the writing of the information into the card-reader buffer have been described in section 3-16. The following sections explain the use of these components as the card is processed.

3-38. FEED CARD A. When the pickerknife flip-flop is set, it alerts the first flip-flop of the card-cycle counter, restores the interlock 1 flip-flop, and actuates the pickerknife to feed card A. The tenth, 11th, and 12th photocell signals step the row counter. Next, the gap on the timing disc generates a clear-counter signal which first clears the row counter and then sets it to a reading of 12, restores synchronizing flip-flop 2, and sets the first flip-flop of the card-cycle

counter. The CCC2 signal generated from the cycle counter indicates that card A is on the way toward the first read station.

The next nine photocell signals step the row counter but do not generate probe signals because the read stations are empty. When the row counter again reads nine (second timing-disc revolution, figure 3-8), card B is fed if a new 72 instruction has been given. The tenth, 11th and 12th photocell signals step the row counter. The gap steps the card-cycle counter. As shown in figure A-24, both the first and second flip-flops of the card-cycle counter are now set. The CCC2 signal indicates that card B is moving toward read station 1, while the CCC3 signal indicates that card A is in read station 1. The gap also clears the row counter, sets it to 12, and restores synchronizing flip-flop 2.

3-39. READ AND TRANSFER CARD A. The treatment of row 1 and of subsequent rows will be discussed separately.

(1) ROW 1. The first photocell signal which occurs after card A reaches the first read station third timing-disc revolution (figure 3-8) steps the row counter to one and also generates a probe signal (section 3-14). Row 1 of card A is read in the first read station. Because the second read station is empty, the brushes sense all ones.

The information from both read stations is transferred to intermediate storage as shown in figure 3-9. The loading of intermediate storage sets the first flip-flop of the column-group counter to generate a G1 signal.

The first ST sentinel after intermediate storage is loaded sets both the reader-control flip-flop, which remains set for one-half drum revolution, and sample flip-flop 1. As shown in table 3-2, ST sentinels occur in locations 098 and 198. One ST sentinel begins the transfer of the information from intermediate storage and the other sentinel ends the transfer. If the sentinel in location 098 begins the transfer, head 2 is energized to write into the card buffer because it is over the card-reader half. If the sentinel in location 198 begins the transfer, head 1 is energized to write into the card buffer because it is over the card-reader half.

The shift register is cleared by the SSP1 signal generated when sample flip-flop 1 is set. The G1 signal and the sample-pulse signal transfer the first ten bits, the least significant bits of the J10 word, from intermediate storage into the shift register. No initial shift is required because the first group transferred in any row is always an odd group.

If the ST sentinel in location 198 begins the transfer, the R1 sentinel in location 000 sets the head-1 write flip-flop, generating an EF1 signal. If the ST sentinel is in location 098, the R1 sentinel is in location 100, the head is 2, and the signal is EF'1. The EF1 or EF'1 signal sets the

shift flip-flop to shift the ten bits out of the shift register. The bits enter the write circuits of either head 1 or head 2 and are written into location 000 in the first track of the buffer, as shown in table 3-2. Although interlace-pattern 1 shows the J10 word in location 000, only six of the bits are recorded there. The remaining four bits are recorded in the first four positions of location 001.

When all ten bits have been recorded, the write flip-flop is restored, generating either an SS1 or an SS2 signal. The SS1 or SS2 signal steps the column-group counter to the next reading, G2, and also sets sample flip-flop 1 for the second time.

The SSP2 signal generated by the SS1 or SS2 signal clears the shift register, and the G2 signal combined with the sample signal transfers the second group of ten bits from intermediate storage to the shift register. This group consists of ten 1 bits because no card was in read station 2. (When a card is read in read station 2, the group is the least significant bits of the J20 word.) Because the second group is an even group, an initial shift is required. The shift is generated by the G2A (even reading) signal from the group counter combined with the R1 sentinel in location 010 or 110. The same R1 sentinel sets the write flip-flop for either head 1 or head 2. The ten bits are shifted from the shift register and written into buffer location 010 (table 3-2) in the same manner that the J10 bits were written into location 000.

The remaining R1 sentinels write the least significant bits of the J11, J21, J22, J13, J23, J14, and J24 words (figure 3-1) in the first track of the buffer in locations 020, 030, 040, 050, 060, 070, 080, and 090 according to interlace-pattern 1. If the ST sentinel in 098 started the transfer, the ST sentinel in 198 ends the transfer, and vice versa. The ST sentinel restores the reader-control flip-flop, completing the transfer of the first row of information.

(2) ROWS 2 THROUGH 12. When the second photocell signal occurs, row 2 of card A is in position to be sensed, as shown in figure 3-8. The photocell signal steps the row counter to two and generates a probe signal. The bits from row 2 of card A and the ten 1 bits from empty read station 2 are transferred to intermediate storage. One of the ST sentinels sets sample flip-flop 1 and the reader-control flip-flop. Writing row 2 into the buffer is similar to writing row 1 except that the bits are written into track 2 instead of track 1.

The third photocell signal generates the probe signal to sense row 3. The bits from row 3 are written into track 3. The fourth photocell signal generates the probe signal to sense row 4. The bits from row 4 are written into track 4. This completes the writing of all four bits of the ten digits of the unprimed words (00 0000) on the upper field of the card.

The fifth and sixth photocell signals sense rows 5 and 6 of the upper field or the two bits (00 0000) of the primed words, J'10, J'20, J'11, J'21, J'12, J'22, J'13, J'23, J'14 and J'24 (figure 3-1 and table 3-2). The bits from row 5 are written into track 1 and the bits from row 6 are written into track 2 in locations 005, 015, 025, 035, 045, 055, 065, 075, 085 and 095. Zeros are written in tracks 3 and 4. The R2 sentinel controls writing rows 5 and 6.

The seventh, eighth, ninth, and tenth photocell signals sense rows 1 through 4 of the lower field of the card or the four bits of the ten digits which make up the unprimed words J15, J25, J16, J26, J17, J27, J18, J28, J19, and J29. The bits from row 1 are written into track 1, row 2 into track 2, row 3 into track 3, and row 4 into track 4. The R3 sentinel controls writing all four of these rows into locations 001, 011, 021, 031, 041, 051, 061, 071, 081, and 091 of the buffer.

The 11th and 12th photocell signals sense rows 5 and 6 of the lower field or the two bits of the ten digits which make up the primed words J'15, J'25, J'16, J'26, J'17, J'27, J'18, J'28, J'19 and J'29. The bits from row 5 are written into track 1 and the bits from row 6 into track 2.

Zeros are written in tracks 3 and 4 (section 3-17). The R4 sentinel controls writing row 5 and 6 into locations 006, 016, 026, 036, 046, 056, 066, 076, 086, and 096 of the buffer.

After all rows of card A have been written into the buffer, the row counter reads 12 (signals LF, R6). The ST sentinel which restores the reader-control flip-flop after row 12 has been written also sets the buffer-loaded flip-flop. At this point the program must include a 96 instruction to transfer the information from the buffer into a selected band of main storage. If the programmer does not give the 96 instruction before the first rows of card A in read station 2, and card B in read station 1, are sensed and transferred to intermediate storage, the information already stored in the buffer is lost because the newly read information is written over it.

3-40. READ AND TRANSFER CARDS B AND A. The gap on the timing disc following the 12th photocell signal of the third timing-disc revolution, figure 3-8, steps the card-cycle counter. Both the second and third flip-flops of the card-cycle counter are set. Signal CCC3 indicates that card B is in the first read station and signal CCC4 indicates that card A is in the second read station. The gap clears and sets the row counter to a count of 12 and restores synchronizing flip-flop 2. The first photocell signal steps the row counter to one and generates a probe signal. Row 1 of card B and row 1 of card A are read, and the information is transferred to intermediate storage. The reading and transfer of the information are identical to the operations described in section 3-39. After all 12 rows have been sensed and transferred to buffer storage, the buffer-loaded flip-flop is again set and a 96 instruction transfers the information from the buffer into main storage.

A programmed check to ensure that the information sensed from card A in the first read station is the same as the information sensed from card A in the second read station can be made by a series of comparison (82) instructions.

3-41. SEND CARD A TO OUTPUT STACKER. The timing-disc gap following the fourth timing-disc revolution, figure 3-8, steps the card-cycle counter. The CCC4 output signal indicates that card B is in the second read station; the CCC5 signal indicates that card A is on the way to the output stackers. Card A drops into stacker 0 unless a 47 instruction selects stacker 1 or 2 at the time that the card is moving toward the stackers.

3-42. 96 INSTRUCTION

The 96 instruction transfers the information from the card-reader half of the card buffer into the main-storage band specified in the instruction. Any one of the 25 bands can be selected to store the information by writing the number of the band (00, 02, 04 ... 48) in the p7 and p8 positions of the m address. If information is to be written into one of the five fast-access bands, only one of the four heads per band is energized. The 96 instruction should be given by the program as soon as the buffer is loaded as a result of a 72 instruction. If it is given before the buffer is completely loaded, the 96 instruction remains staticized and does not advance to the second step until the buffer-loaded flip-flop is set. If it is given after the next card is sensed, the information stored in the buffer is lost because the subsequent sensed information is written over it.

During the first step of the 96 instruction, a search is made for the selected band. If the buffer-loaded flip-flop is set and the BT (begin transfer) sentinel in location 199 is present, the instruction advances to the second step. (Refer to the analysis of instructions manual for the detailed description of the first step.)

During the second step, the transfer from buffer to main storage requires one drum revolution. As shown in figure 3-10, head 1 reads first because it is over the card-reader half of the buffer during the first half of the drum revolution; head 2 completes the reading during the second half of the drum revolution. The R5 sentinel in location 000 of the timing band (interlace pattern 2, table 3-3) sets the read flip-flop of head 1 to read the 40 bits of the J10 word from the 000 location of the card-buffer band. Function signal 98 alerts gates 3A, 3B, 3D, and 103 of the M buffers to information on the C lines. The information is transferred from the C lines to the M lines, which are inputs to the main-storage write circuits, figure A-19. Gate 100 of the main-storage write flip-flop is alerted by FS 98 and made permissive by the RSC5 signal, generated from the set output of the head-1 read flip-flop. Gate 100 operates to set the write flip-flop, the output of which alerts the write input circuits to input information on the M lines. The write pedestal (WPP) is

generated by FS 98A and the IR2D set output of the write flip-flop. All of the J10 word is written into location 001 of the chosen band.

Each subsequent R5 sentinel again sets the head-1 read flip-flop to read one of the primed or unprimed words from the card buffer and write it into the first half of the main-storage band. The R5 sentinel transfers only the words from the upper fields. The last word to be transferred is J'24, transferred by the R5 sentinel in location 095.

Head 2 is over the card-reader half of the buffer beginning with location 100. The first R6 sentinel, in location 101, sets the read flip-flop of the head-2 circuits (figure A-23) to read the 40 bits of the J15 word from the 001 location of the card-buffer band. The bits are transferred from the OC lines to the M lines by FS 98 at gates 102, 106, 109 and 112 of the M buffers. The write flip-flop of main storage is set at gate 5A by the RSC2 set output of the head-2 read flip-flop. The write pedestal is generated by FS 98A and the set output of the write flip-flop, IR2D. All 40 bits of the J15 word are written into location 102 of the selected band.

Each subsequent R6 sentinel again sets the head-2 read flip-flop to read one of the primed or unprimed words from the card buffer and write it into the second half of the main-storage band. The R6 sentinel transfers the words from the lower fields. The last word to be transferred is J'29, transferred by the R6 sentinel in location 196.

The T0 sentinel, with FS 98, restores the buffer-loaded flip-flop. With FS 93, the sentinel generates an ending pulse (EP) and a high RCT3 signal at gate 13 of the static register. The conditional-transfer flip-flop has been set to control the search for the m address during the 96 instruction. The RCT3 signal restores the conditional-transfer flip-flop (figure A-12) so that the next search is for the c address.

3-43. 47 INSTRUCTION

The 47 instruction actuates a stacker selector (section 3-12) so that the card drops into the desired output stacker. The programmer selects a stacker by writing zero, one, or two in the p7 digit position of the instruction word. When the 47 instruction (figure 3-11) is read from storage and staticized, the p7 digit is stored in the multiplier-quotient counter (MQC) as in any other instruction (section 4-8, central processor manual). The value of the p7 digit from MQC determines which of the three stackers is selected. After the select-stacker flip-flops have sampled the MQC outputs, the 47 instruction is cleared from the static register so that other instructions can be processed while the stacker is being selected. A stacker remains selected until another 47 instruction selects a different one. The following sections describe the selecting of each of the three stackers. Select-stacker

flip-flops 1 and 2 are restored prior to the sampling of the MQC outputs.

3-44. SELECT STACKER 2. If the p7 digit of the instruction word is a two, the Q2 signal is low, setting FF1. The flip-flop holds the indication that stacker 2 has been selected until the time to actuate the stacker selector. The time is determined by the CCC5 output of the card-cycle counter, the SRC (step row counter), and row 11 (R5, LF) signal at gate 45. The CCC5 signal indicates that a card has been read in read station 2 and is on its way to the output stackers. When the SRC and row 11 indication shows that the row counter is stepping from 11 to 12, provided that FF1 is set, FF3 is set to actuate the stacker selector, which pivots upward into the path of the oncoming card and directs it into stacker 2.

As the row counter steps from two to three on the next cycle, FF3 is restored. If another card arrives at the stackers before a new 47 instruction changes the stacker selection, FF1 remains set and FF3 is set again to direct the next card into the same stacker.

3-45. SELECT STACKER 1. If the p7 digit of the instruction word is a one, the Q1 signal is low, setting FF2. The flip-flop holds the indication that stacker 1 has been selected until the time to actuate the stacker selector. Flip-flop 5 is set by the same signals that set FF3 (section 3-44) but because the card must travel further before it reaches stacker 1 than stacker 2, the actuating of the stacker selector is delayed until the row counter reads 8. When it does, FF4 is set to actuate the stacker selector for stacker 1 and FF5 is restored. On the next cycle, FF4 is restored when the row counter steps from two to three. If another card arrives at the stackers before a new 47 instruction changes the stacker selection, FF2 remains set, and FF5 and FF4 are set again to direct the next card into stacker 1.

3-46. SELECT STACKER 0. Stacker 0 is selected by the absence of select-stacker 1 or 2 signals. If the p7 digit of the instruction word is a zero, the Q1 and Q2 outputs of MQC are high. As shown in figure 3-11, FF1 and FF2 are restored, and FF3, FF4, and FF5 cannot be set. The absence of select-stacker 1 and 2 signals causes the card to drop into the last of the three stackers, stacker 0.

3-47. ABNORMAL OPERATION

All abnormal conditions in the card reader are controlled by the abnormal-operation flip-flop. This flip-flop sends indications of such conditions to the input-output abnormal-condition flip-flop in the central processor. This section describes the abnormal-operation (AOR) flip-flop and the conditions which influence it.

3-48. ABNORMAL-OPERATION FLIP-FLOP

The abnormal-operation flip-flop (figure A-25) is alerted if one or more of the following conditions generates a high input to buffer 73:

(1) A card jam between read station 2 and the output stackers (CARD JAM)

(2) One or more of the stackers filled with cards (FULL STACKER)

(3) Processor stopped by operator (STOP SWITCH)

(4) Input bin empty

(5) Faulty movement of card through read station (REGISTRATION ERROR)

(6) Processor stopped on each 72 instruction because the operator has pushed the ONE CARD HSR button on the processor control panel (RECC)

The input signal is shown in parenthesis.

A low output from buffer 73, indicating the presence of an abnormal condition, and a low SA0 (set abnormal operation) signal make gate 70 permissive, setting the abnormal-operation flip-flop. The SA0 signal (figure A-5) is low when either FS 1A is high, indicating that the processor is on search, or SPA is high, indicating that the processor is stopped (stop flip-flop set).

When the abnormal-operation flip-flop is set, it generates low AOR and high $\overline{\text{AOR}}$ signals, and the card-reader-off-normal-relay signals which light the SYSTEM OFF NORMAL lamp on all three input-output equipments, and the CARD READER/OFF NORMAL lamp on the central processor panel.

The low AOR signal alerts gate 102 of the input-output abnormal-condition flip-flop (figure A-2). When the next 72 instruction is staticized, no card is fed. Normally FS 28 alerts gate 111 of the static register to generate an ending pulse which clears the 72 instruction from the static register. Gate 111 is blocked, however, when the high $\overline{\text{AOR}}$ signal is present. Gate 102, alerted by FS 28, sets the input-output abnormal-condition flip-flop and generates high Jam I2A and Jam I2B signals at t10B. At t11B, FS 28 normally sets the interlock-1 flip-flop, which actuates the pickerknife. The Jam I2B signal blocks the set gate of the interlock-1 flip-flop, however, so that no card is fed. The Jam I2A and Jam I2B signals also transfer the 72 instruction from register C to register A and cause a search for the c + 1 address instead of the c address. (Refer to section 4-41 of the central processor manual.)

After the condition which set the abnormal-operation flip-flop is corrected, the operator must push the GENERAL CLEAR button on the processor control panel to erase all effects of the abnormal condition before st.-ting computation. If the condition is a card jam, the operator must also push the RESET/CARD JAM button on the card-reader panel to set the relay.

The abnormal conditions which set the abnormal-operation flip-flop are described more fully in the following sections.

3-49. CARD JAM

If a card jam occurs within the last four sets of rollers, a mechanism known as the jam detector (2-5,4) operates a switch. The jam-detector beam is adjusted so that whenever a card moves upward and out of its normal path, the beam moves, energizing the jam-detector switch and setting the abnormal-operation flip-flop. The switch also lights the CARD JAM light on the card-reader control panel.

3-50. FULL STACKER

Each of the three stacker bins can hold 850 to 1200 cards. When any bin is full a switch is energized, setting the abnormal-operation flip-flop. The switch also lights the OUTPUT BIN FULL light on the card-reader control panel.

3-51. STOP SWITCH

If the operator has depressed a STOP button on any of the panels, a stop-switch signal is generated, setting the abnormal-operation flip-flop.

3-52. INPUT BIN EMPTY

The empty-input-bin switch in the first read station is normally open except when a card passes through the read station to close it. If a card is not fed when a 72 instruction is given, the switch remains open, setting the abnormal-operation flip-flop and lighting the INPUT MAGAZINE EMPTY light on the card-reader control panel.

The empty-bin flip-flops (figure A-25) store the indication of an empty input bin and set the abnormal-operation flip-flop. The first empty-bin flip-flop is set at gate 102 when low CCC2 and SCCC signals indicate that a 72 instruction has been given and a card should be fed. If a card does not pass the switch to close it, the Empty Mag Sw signal is low at gate 103, keeping the first flip-flop set. When the row counter is on row 1 (signals UF and R1), gate 106 sets the second empty-bin flip-flop and generates a high RCCC3 signal which restores the second flip-flop of the card-cycle counter so that no probe signals are generated. The second empty-bin flip-flop also sends a high signal to buffer 73 to set the abnormal-operation flip-flop.

On the other hand, if a card is fed, it closes the switch. The Empty Mag Sw signal is high at gate 103, restoring the first flip-flop, the second flip-flop remains restored, and there is no error indication.

3-53. REGISTRATION ERROR

A registration photocell and an exciter lamp are located after each read station to detect incorrect registration or misfeed of the card. When a card passes the first registration photocell, a low PC1 signal is generated. When a card passes the second registration photocell, a low PC2 signal is generated.

Registration-check flip-flop 1 (figure A-25) is initially set at gate 50, if there is a card in read station 1 (signal CCC3) and row 8 is being read (signals R2 and LF). If the card passes the first photocell at the correct time (low PC1 signal), gate 48 operates to restore the flip-flop. If the card does not pass the photocell (high PC1 signal) when row 9 is read (signals R3 and LF) the flip-flop remains set, and the REGISTRATION/READ STATION indicator on the card-reader panel lights.

The flip-flop also sends a high signal to buffer 61, which alerts gate 60 of the motor-control flip-flop. When the SCCC signal is low as a result of the clearing of the card-cycle counter, gate 60 sets the motor-control flip-flop. The set outputs of the flip-flop are sent to the card-feed controls to stop the motor.

The motor-control flip-flop also generates a high IRC signal which sets the abnormal-operation flip-flop at buffer 73. The IRC signal keeps the registration-check flip-flops set so that the indicator lamp remains lighted even if the next card registers correctly before the motor stops. The indicator informs the operator that a registration error has occurred. The IRC signal also restores the interlock-1 flip-flop to prevent feeding more cards.

Registration-check flip-flop 2 is set at gate 55 if there is a card in read station 2 (signal CCC4) and row 8 is being read (signals R2 and LF). It is restored if gate 53 operates, indicating that the card has passed the second photocell at the correct time. If an error occurs, the REGISTRATION/CHECK STATION indicator on the card-reader panel lights and the flip-flop sends a high signal to buffer 61, which controls the motor-control and abnormal-operation flip-flops.

3-54. ONE CARD READER

The READER/ONE CARD button on the processor panel stops the computer on the first step of the next card-cycle (72) instruction for the card reader. An RECC signal is generated and sent to buffer 73 of the abnormal-operation flip-flop. Refer to section 4-45 of the central processor manual.

3-55. CARD-CYCLE ERROR FLIP-FLOP

The card-cycle error flip-flop (figure A-24) is set if a buffer-transfer (96) instruction has been omitted from the program. Normally each 72 instruction, which loads the buffer with sensed information, is followed by a 96 instruction to transfer the information from the buffer to main storage.

If a 96 instruction is missed, the buffer is loaded (signal BL1 low) and the next 72 instruction loads the sensing brush. The BL1 and brush-storage-loaded signals make the set gate of the buffer-transfer-check flip-flop permissive to light the ALERT 96 CHECK lamp on the processor control panel and generate a low Set Stop signal. The Set Stop signal is sent to a set gate of the stop flip-flop (figure A-5) to stop the processor immediately.

The operation of the buffer-transfer-check flip-flop may be inhibited by the 96 CHECK switch on the processor control panel.

BLOCK 0	BLOCK 1	BLOCK 2	BLOCK 3	BLOCK 4
1 2 3 4 5 6 J_{10} J_{20}	J_{11} J_{21}	J_{12} J_{22}	J_{13} J_{23}	J_{14} J_{24} 1 2 3 4 5 6
7 8 J'_{10} J'_{20}	J'_{11} J'_{21}	J'_{12} J'_{22}	J'_{13} J'_{23}	J'_{14} J'_{24} 7 8
1 2 3 4 5 6 7 8 9 10	11 12 13 14 15 16 17 18 19 20	21 22 23 24 25 26 27 28 29 30	31 32 33 34 35 36 37 38 39 40	41 42 43 44 45
BLOCK 5	**BLOCK 6**	**BLOCK 7**	**BLOCK 8**	**BLOCK 9**
1 2 3 4 5 6 J_{15} J_{25}	J_{16} J_{26}	J_{17} J_{27}	J_{18} J_{28}	J_{19} J_{29} 1 2 3 4 5 6
7 8 9 J'_{15} J'_{25}	J'_{16} J'_{26}	J'_{17} J'_{27}	J'_{18} J'_{28}	J'_{19} J'_{29} 7 8 9
46 47 48 49 50 51 52 53 54 55	56 57 58 59 60 61 62 63 64 65	66 67 68 69 70 71 72 73 74 75	76 77 78 79 80 81 82 83 84 85	86 87 88 89 90

3188

Figure 3-1. Primed and Unprimed Parts of Card-Coded Word

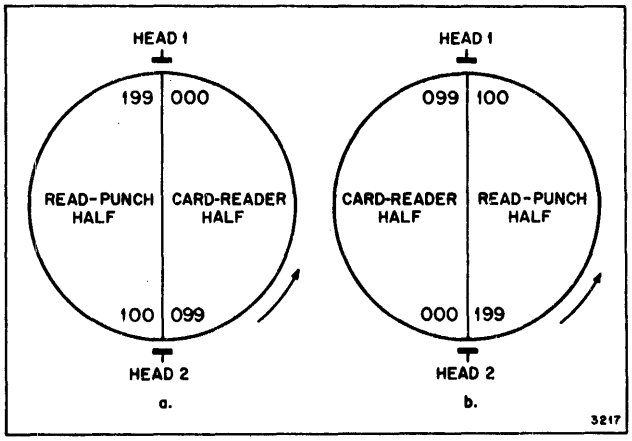


Figure 3-2. Card Buffer Band and Read-Write Heads

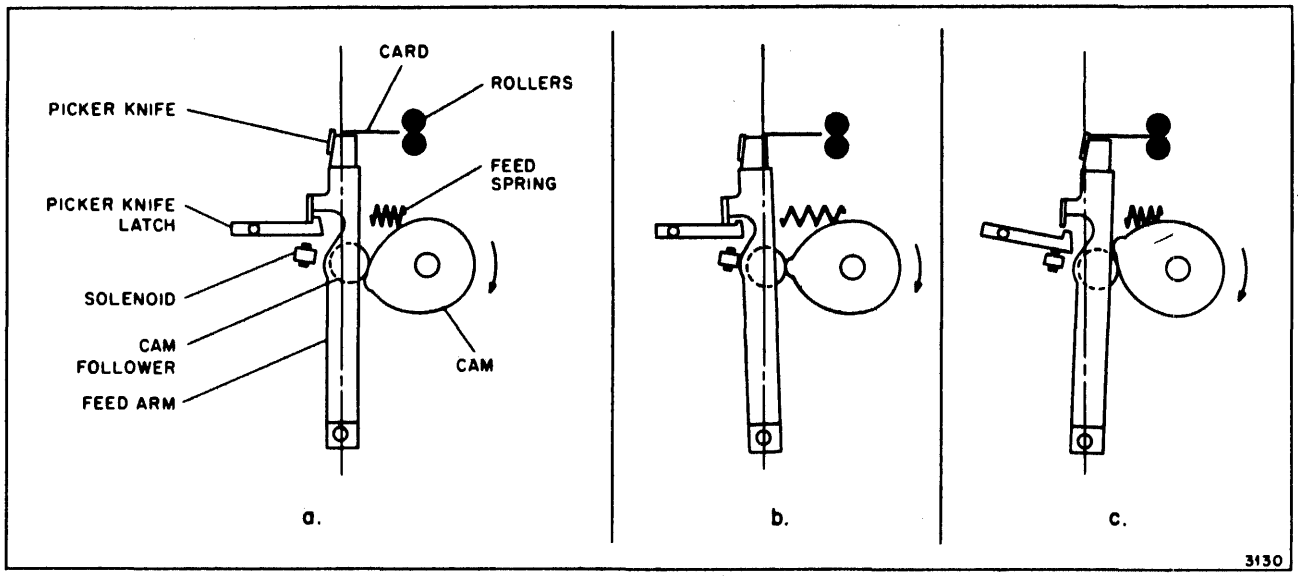


Figure 3-3. Pickerknife Actuation

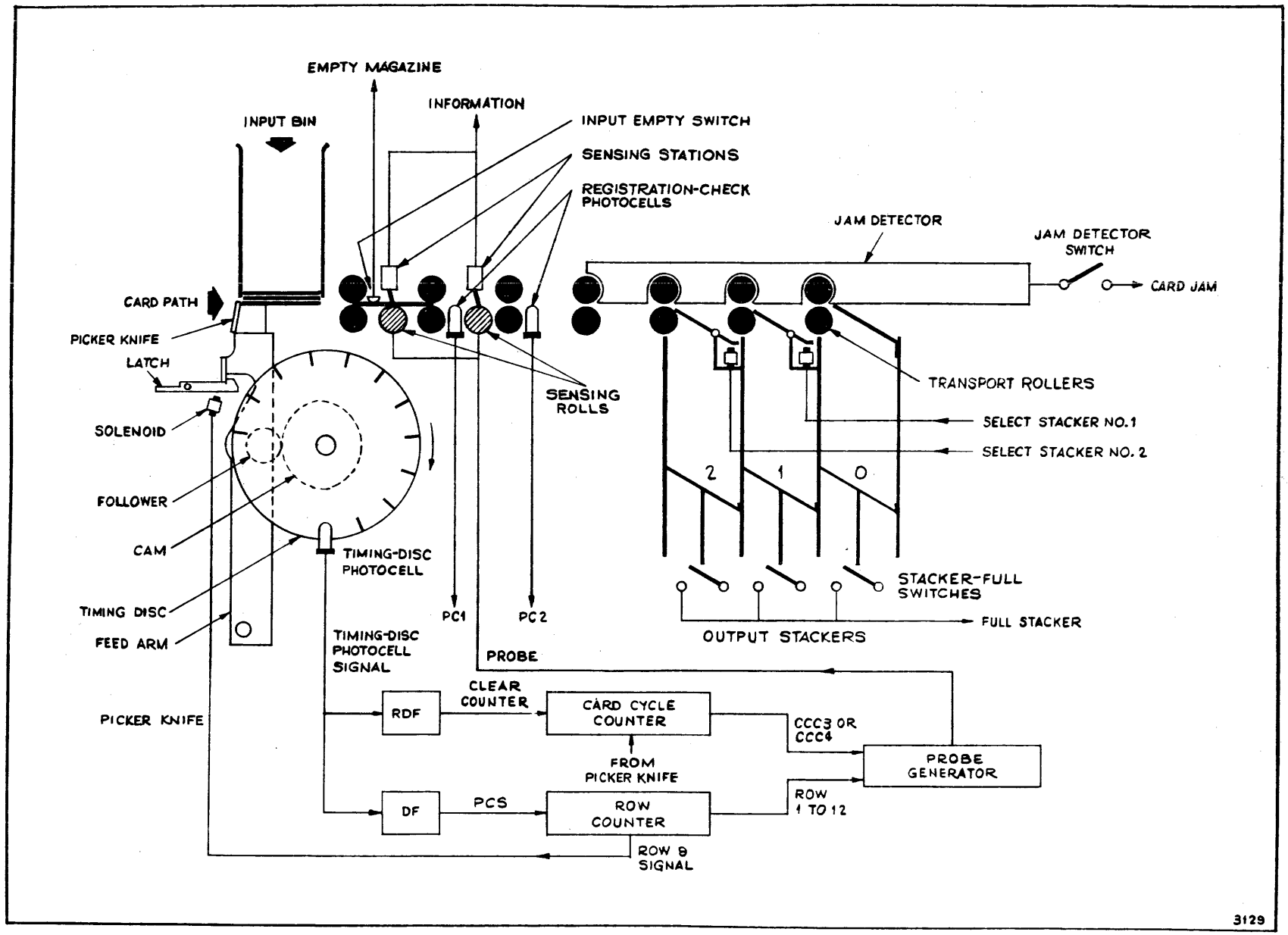


Figure 3-4. Card Reader, Electromechanical Schematic

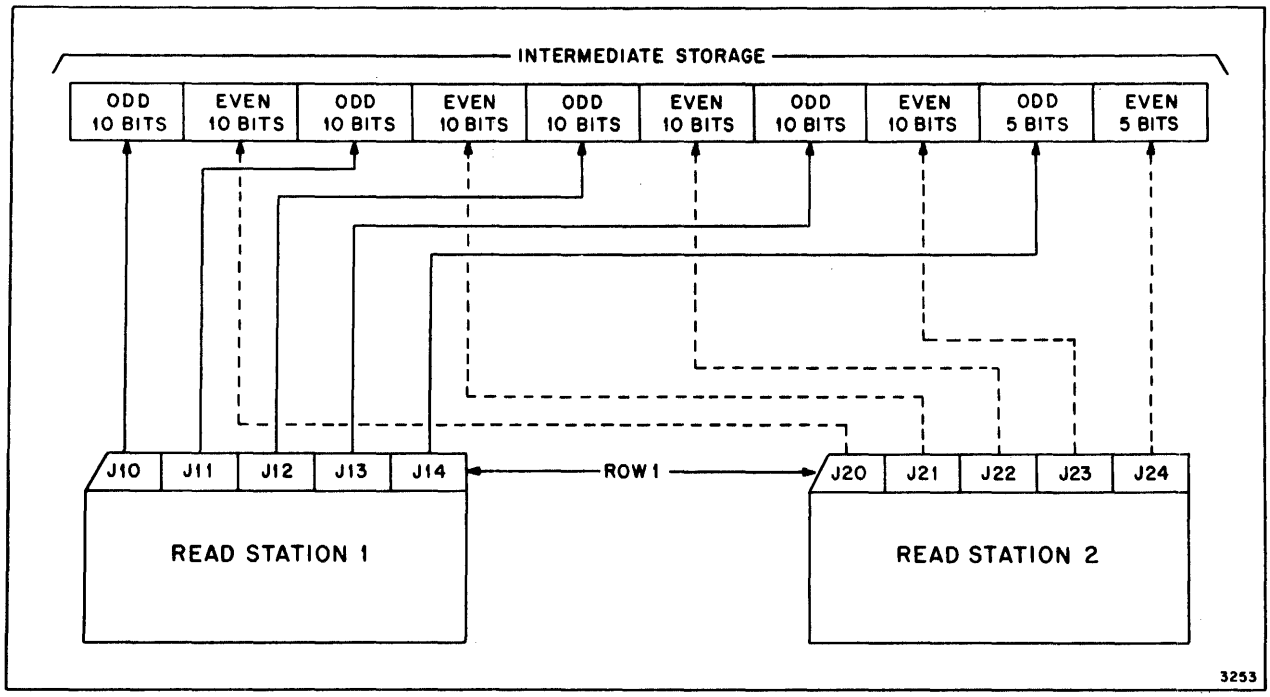


Figure 3-5. Transfer of Rows to Intermediate Storage

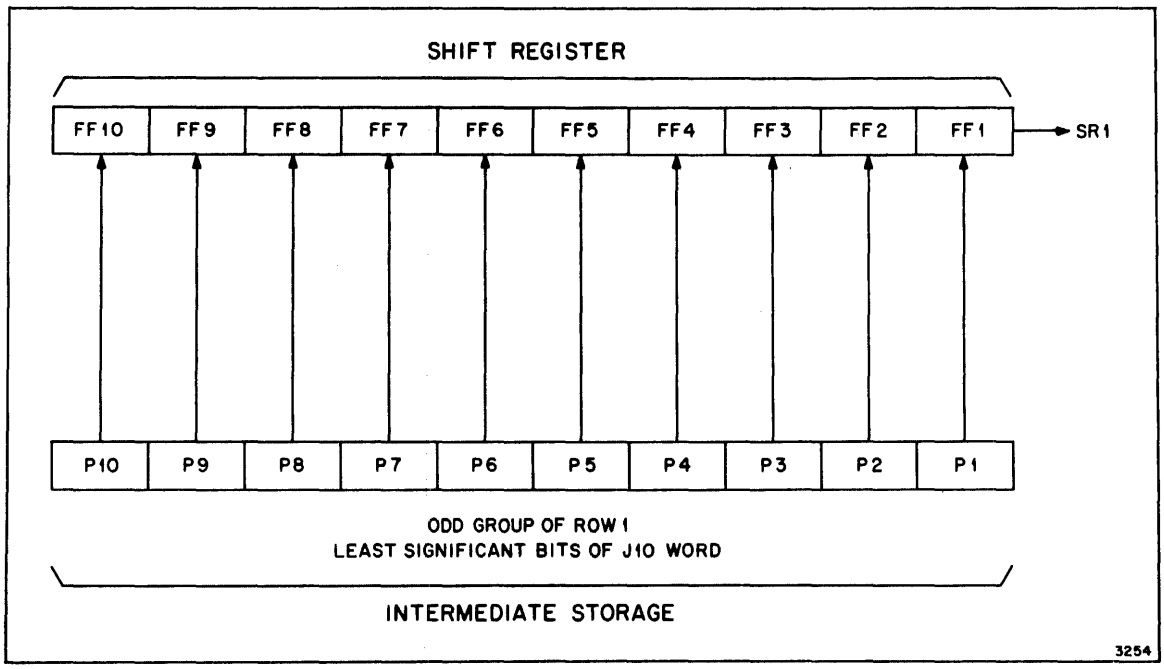


Figure 3-6. Transfer of Odd Groups

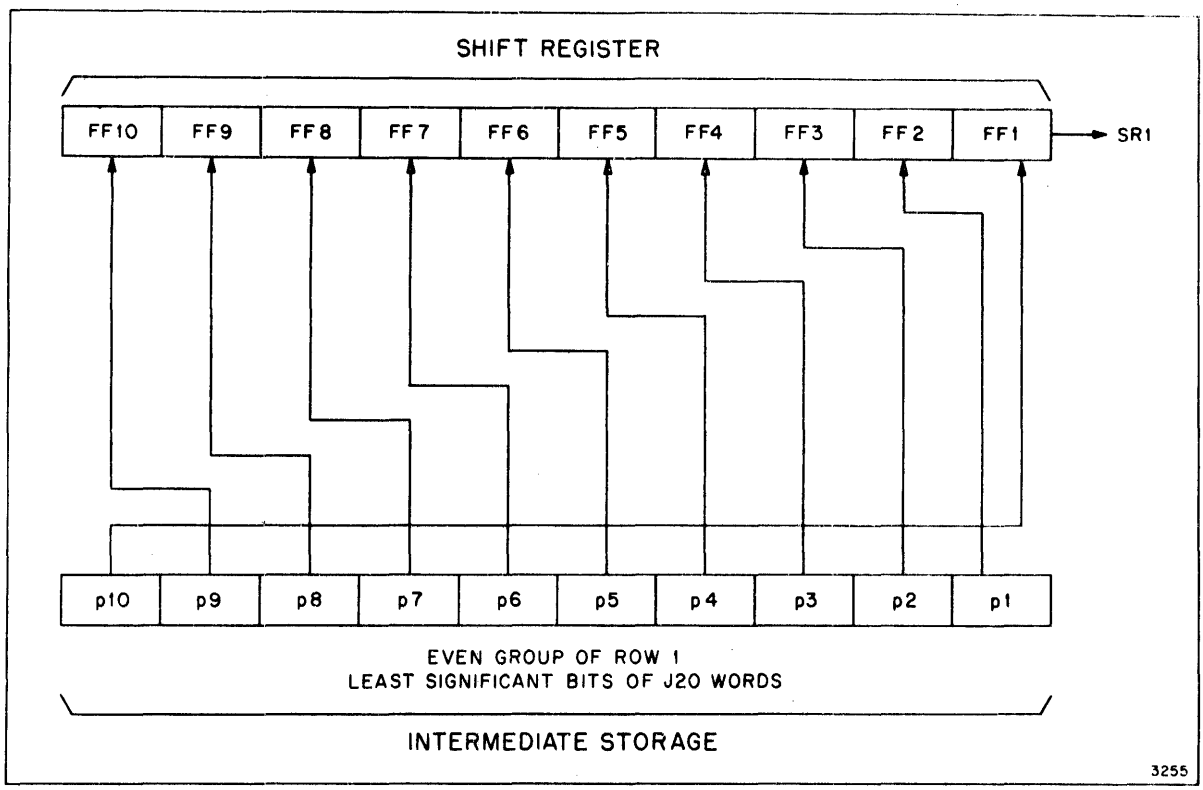


Figure 3-7. Transfer of Even Groups

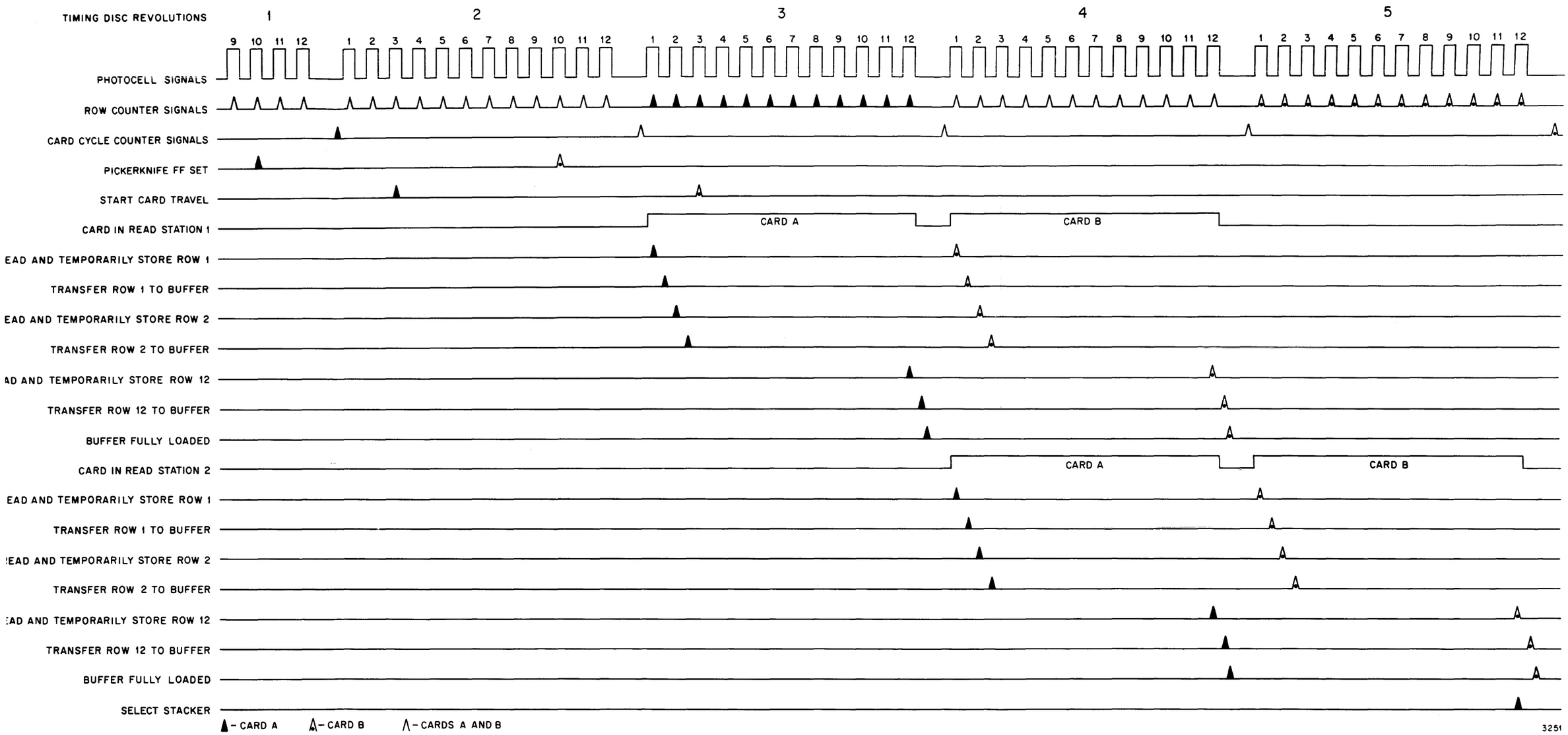


Figure 3-8. General Timing Diagram

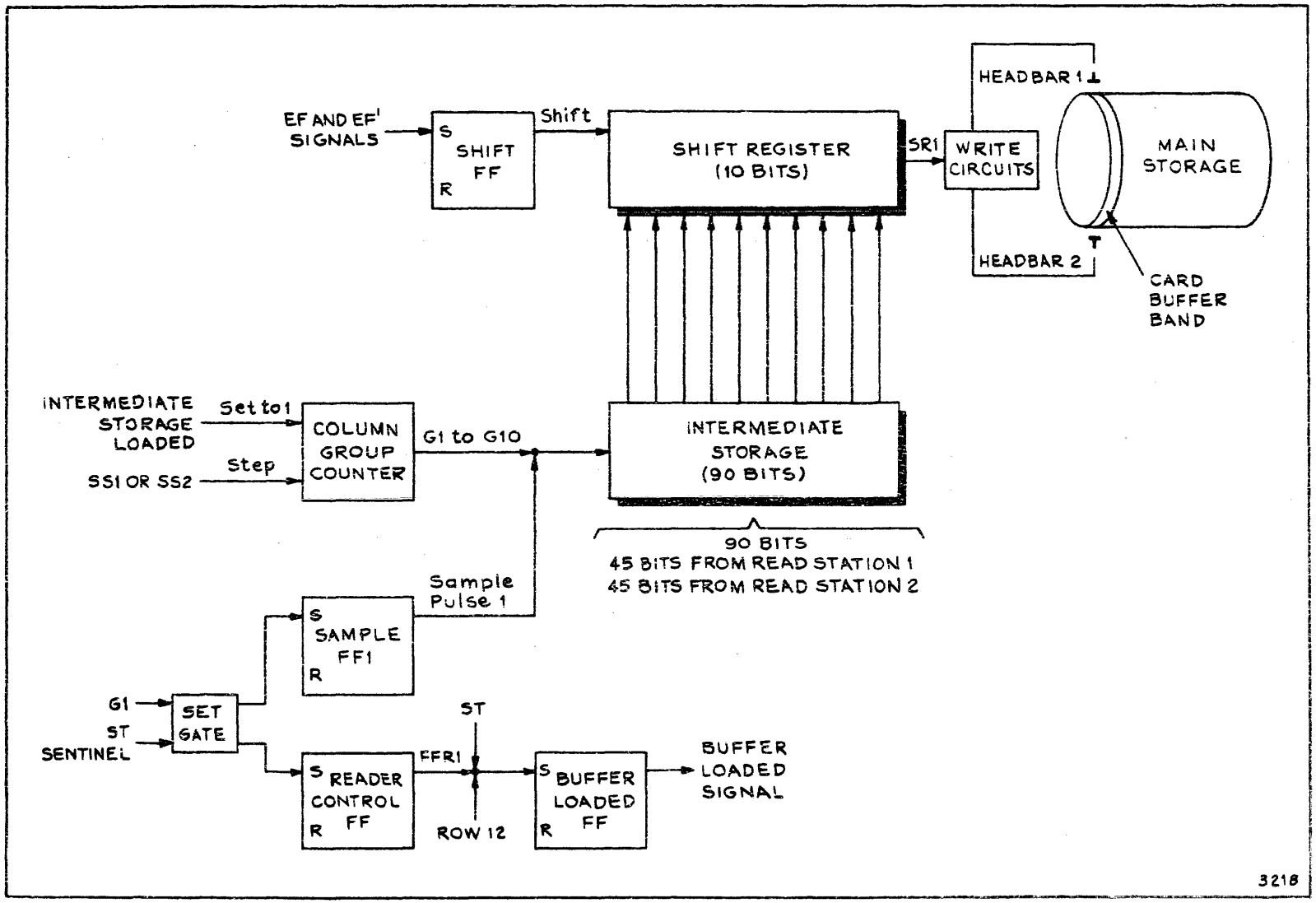


Figure 3-9. Transfer Operation

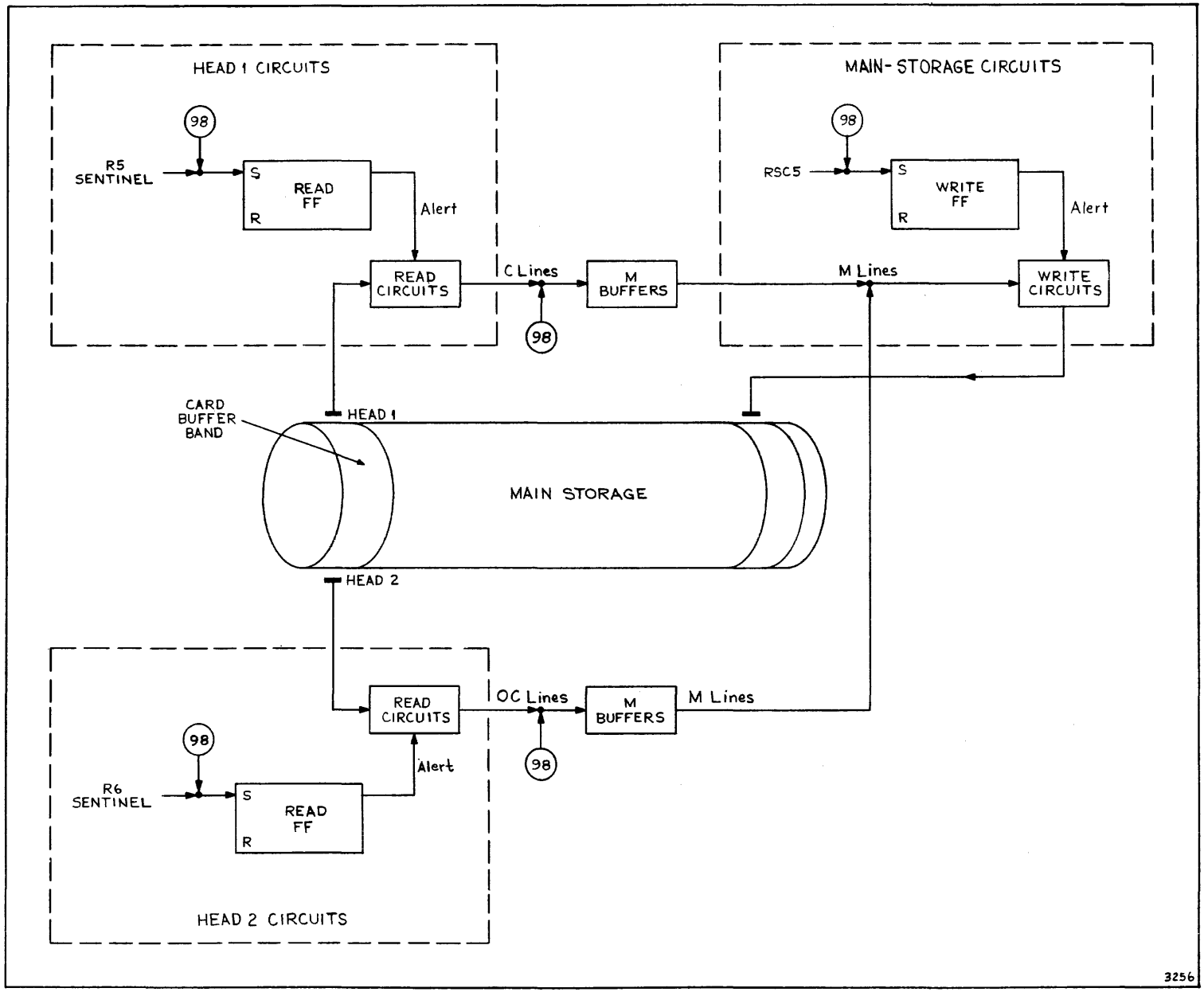


Figure 3-10. Buffer-to-Main-Storage Transfer (96 Instruction)

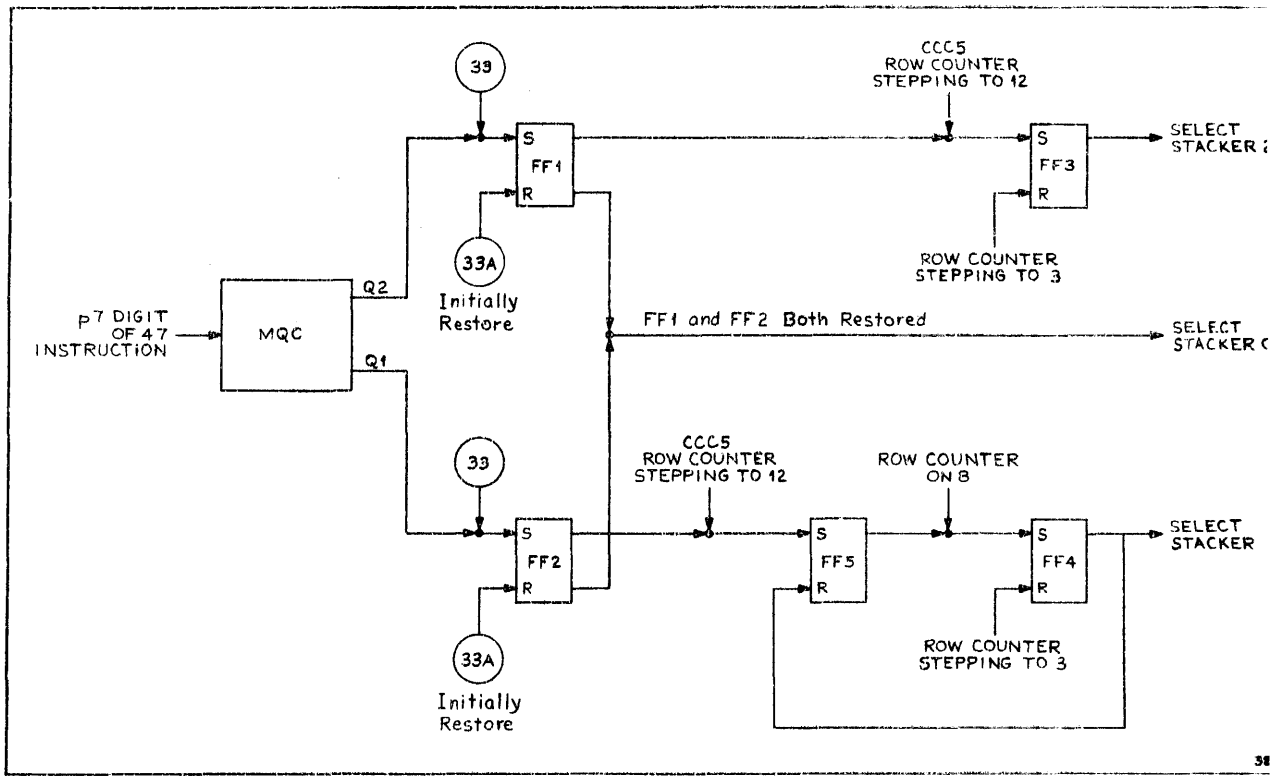


Figure 3-11. Stacker Selection (47 Instruction)

SECTION IV

ELECTRONIC CIRCUITRY

4-1. SCOPE

This section describes the card-reader circuitry, shown in block form in figure 4-1. After some general background on the type of photocell used, the operation of the two photocell circuits is explained in detail. The operation of each circuit which generates a signal, as well as that of the intermediate-storage circuit, is also treated in detail. It is not necessary to describe the operation of certain circuits, such as the counters and the shift register, which utilize only the typical magnetic-amplifier circuits described in the central processor manual.

Current direction is taken as the direction of electron flow (from negative to positive).

4-2. GENERAL DESCRIPTION

The operation of the circuits shown in figure 4-1 is as follows.

The timing-disc photocell develops electrical pulses synchronized with the mechanical operations of the reader. The photocell amplifier fixes both the amplitude and the duration of the signals before they are applied to the card-cycle counter and the row counter. If there is a card in either read station and a row is to be sensed, a generate-clear-and-probe signal is applied to the clear generator. The clear signal clears any previously stored information from intermediate storage, and the trailing edge of the clear signal triggers the probe signal in the probe generator. The probe signal is used to determine whether holes are present in the card positions being sensed. The information so sensed is then stored in intermediate storage through the sensing brushes in the read stations. The trailing edge of the probe signal triggers the brush-storage-loaded signal, which is applied to the column counter.

The signals which initiate the transfer of information from intermediate storage to the shift register are developed in the capacitor sense driver (CSD). Under the control of the column counter, the capacitor sense driver transfers the sensed information from ten columns in parallel from intermediate storage to the shift register. The information in the shift register is then transferred serially to the buffer band.

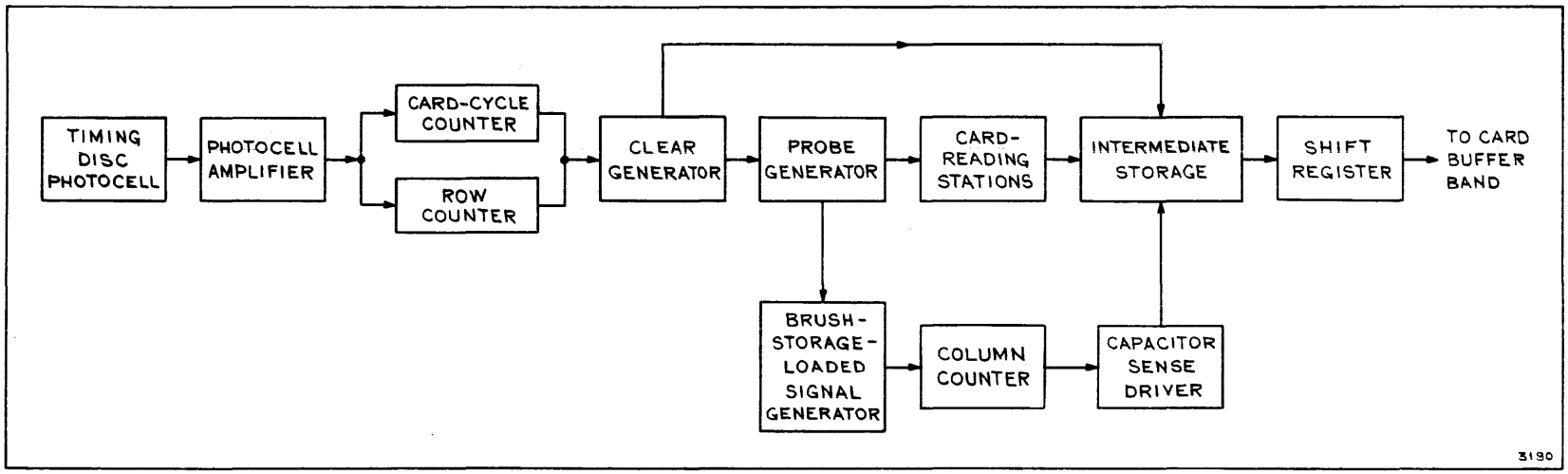


Figure 4-1. Card Reader Circuitry, Block Diagram

4-3. PHOTOCELL CIRCUITS

4-4. LEAD-SULPHIDE PHOTOCONDUCTIVE CELLS

Lead-sulphide photoconductive cells are utilized in the card reader. The basic description presented here parallels the introduction to transistors and semiconductor diodes in the central processor manual.

These photoconductive cells act as variable resistors whose value is a function of the applied light. Essentially, any photoconductive cell consists of two electrodes joined by a semiconductive element. The CE-A 702 A3 lead-sulphide cell consists of a thin film of photosensitive lead sulphide deposited upon an electrically conducting pair of spaced lines called a grid. The grid is drawn upon a suitable insulating surface and connected electrically to two metal pins extending through the glass envelope that isolates the photoconductive film from the atmosphere. The small grid, located on the side of the glass envelope, admits light into the side of the cell.

The light energy is used to excite electrons across the energy gap between the valence band and the conduction band in the semiconductive substance. Refer to section 6-2 of the central processor manual for a more detailed description of this process. Since the semiconductive substance of the lead-sulphide cell has a small energy gap, the cell is sensitive to low-frequency, or infrared, radiation. If this material were prepared without any junctions, it would have a low dark resistance at room temperatures because of the narrowness of the energy gap, and the dark current would be prohibitively high. In practice, the photosensitive film is prepared with a plurality of microscopic PN junctions in the body of the material. This series-parallel network of junctions creates a high dark resistance for the unit, and in consequence a low dark current. The resistance of these units is also temperature-sensitive.

When the cell is illuminated over the entire surface area of the grid, the PN junctions are supplied with enough minority carriers to cause a major reduction in the resistance of the cell. As the resistance of the cell decreases, both the current through the cell and the voltage drop across the load resistance increase.

The voltage sensitivity of the cell, expressed in volts per microwatt, is the ratio of the voltage available across the load resistance to the radiation impinging upon the photosensitive surface. For a fixed amount of incident energy, the voltage sensitivity of a lead-sulphide cell is proportional to the applied voltage and inversely proportional to the area of the surface. For a given cell and a fixed voltage, maximum sensitivity is obtained when the load resistance equals the light resistance of the cell.

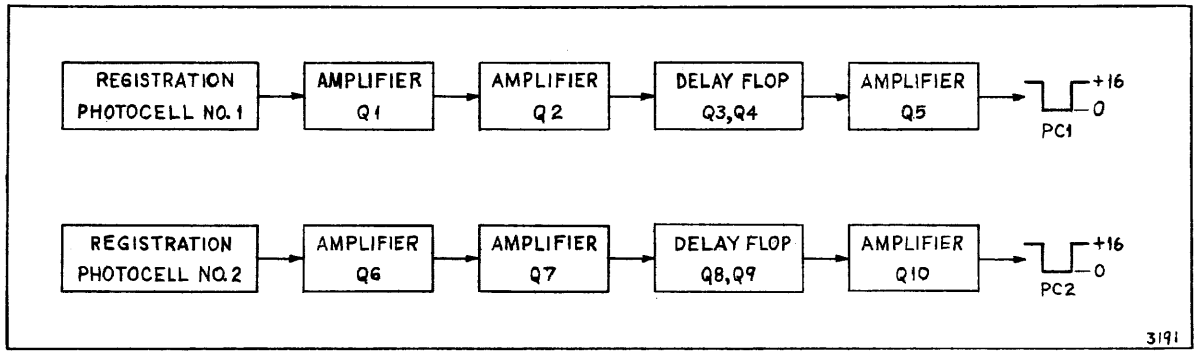


Figure 4-2. Registration Photocell Circuitry, Block Diagram

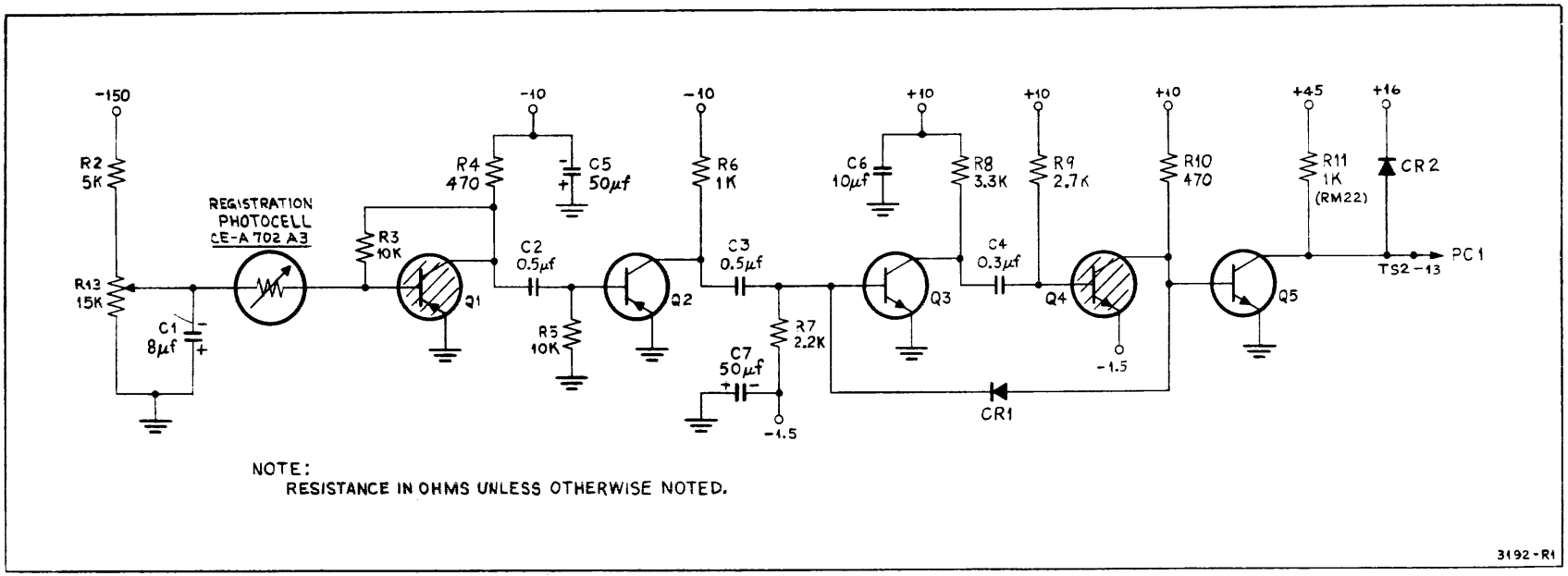


Figure 4-3. Registration Photocell Circuitry, Schematic

4-5. REGISTRATION-PHOTOCELL CIRCUITRY

4-6. GENERAL DESCRIPTION. The card reader contains two registration-photocell circuits (figure 4-2). Since the circuits are identical, only one is described.

When a card passes between the exciter lamp and the photocells, it prevents light from striking the photosensitive surfaces. During the interval between the trailing edge of one card and the leading edge of the next, light impinges upon the photocell, where the light energy is converted to an electrical pulse.

Each electrical pulse passes through two stages of amplification (transistors Q1 and Q2) and then triggers a delay-flop (Q3 and Q4). The delay-flop output is further amplified in Q5. The output of Q5 (signal PC1) is clamped at +16 volts. When an input signal is applied to Q5, the output signal falls to zero volts. Both outputs are suitable for application to a magnetic amplifier.

4-7. DETAILED DESCRIPTION. Light striking the photocell increases the current from the -150-volt supply through resistor R2, the top of R13, the photocell, and the base and emitter of Q1 to ground (figure 4-3). The increased current causes Q1 to conduct heavily, and keeps the Q1 collector voltage near ground potential.

When the leading edge of a card blocks the light from the photosensitive surface, the conductivity of the photocell decreases, decreasing the Q1 bias current through R2, R13, the photocell, and the base and emitter. When the bias current decreases, the collector current decreases, and the Q1 collector voltage falls toward -10 volts.

Amplifier Q1 is R-C coupled to Q2 through R5 and C2. When the Q1 collector voltage approaches -10 volts, part of the C2 charging current flows through the base and emitter of Q2, and Q2 turns on.

When Q2 turns on, current flows through R6 and Q2, and the Q2 collector voltage rises nearly to ground potential. As the Q2 collector voltage rises, capacitor C3 charges. Part of the C3 charge current flows through the emitter and base of Q3 and through the collector and emitter of Q2.

The combination of Q3 and Q4 makes up a delay-flop in which Q3 is normally reverse-biased, and Q4 forward-biased. The C3 charge current turns on Q3, increases the current through Q3 and R8, and decreases the Q3 collector voltage nearly to ground potential. Capacitor C4 discharges through Q3 and R9, developing a negative-going signal across R9.

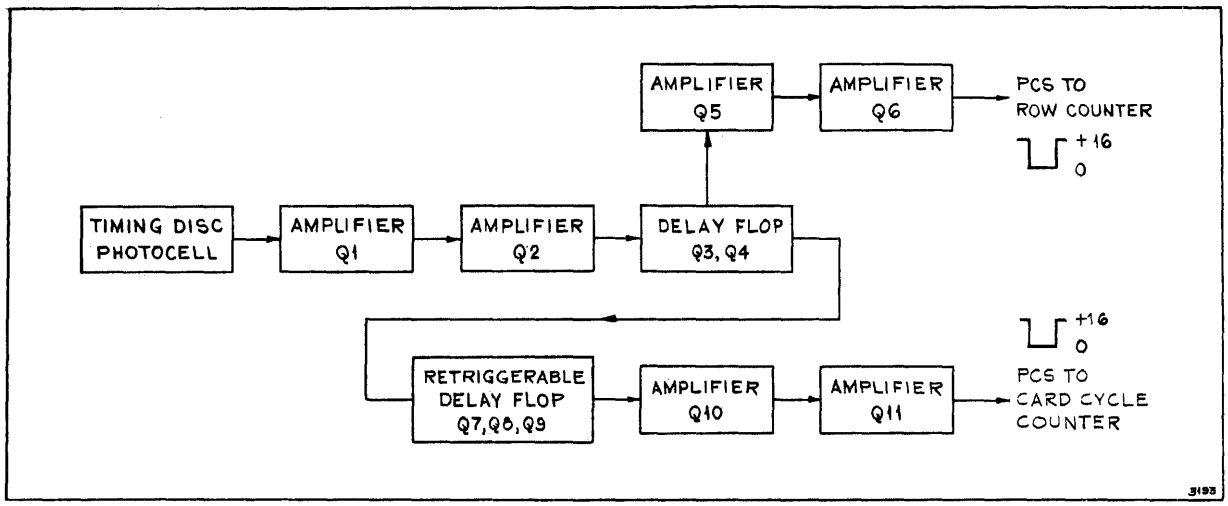


Figure 4-4. Timing-Disc Photocell Circuitry, Block Diagram

The negative-going signal blocks the Q4 emitter-to-base current, allowing the Q4 collector voltage to rise above ground. This positive collector voltage forward-biases diode CR1 to create a current through the emitter and base of Q3, CR1, and R10 to the +10-volt supply. The feedback signal holds Q3 on until C4 becomes discharged. As C4 discharges, the potential at the base of Q4 is restored to its initial value, causing a current through the emitter and base of Q4 and R9. Transistor Q4 turns on, and the Q4 collector voltage falls to about -1.5 volts. The negative collector potential turns off CR1, restoring reverse bias to Q3 and causing Q3 to turn off.

Since Q4 and Q5 are direct-coupled, Q5 is initially reverse-biased through Q4. When Q5 is off, a current from the +16-volt supply through CR2 and R11 to the +45-volt supply clamps the collector of Q5 to +16 volts through CR2. With the delay-flop in its driven state and the Q4 collector voltage above ground potential, current flows through Q5 and R11; the Q5 collector voltage drops to ground potential. As the voltage drops, the PC1 signal taken from the collector becomes negative-going. The duration of the PC1 signal is determined by the time constant of the C4 discharge circuit, which is greater than two word times but less than four word times.

4-8. TIMING-DISC PHOTOCELL CIRCUITRY

4-9. GENERAL DESCRIPTION. The timing disc contains 12 slots at 24-degree intervals around the circumference, and a 72-degree segment which is unslotted (figure 4-4). The timing disc is between an exciter lamp and a photocell. Light strikes the photocell whenever a slot on the rotating disc passes the exciter lamp. In the photocell circuit the light signals are converted to electrical pulses.

Each of these electrical pulses passes through two stages of amplification (Q1 and Q2) and then drives a delay-flop circuit (Q3 and Q4). For each driving signal received by the delay-flop two output signals are developed. One output signal, taken from Q3, is passed through two more stages of amplification (Q5 and Q6) before it is applied to the row counter. The other delay-flop output, taken from Q4, is applied to Q7, the input stage of the retriggerable delay-flop.

The output circuit of Q7 is so designed that it produces no output if Q7 receives a series of input signals in rapid succession. No input signals are applied to Q7 when the unslotted segment of the timing disc passes the exciter lamp and, at this time only, a driving signal which sets the retriggerable delay-flop is applied to Q8. For each driving signal received by the retriggerable delay-flop an output signal is taken from Q8 and passed through two stages of amplification (Q10 and Q11) before it is applied to the card-cycle counter.

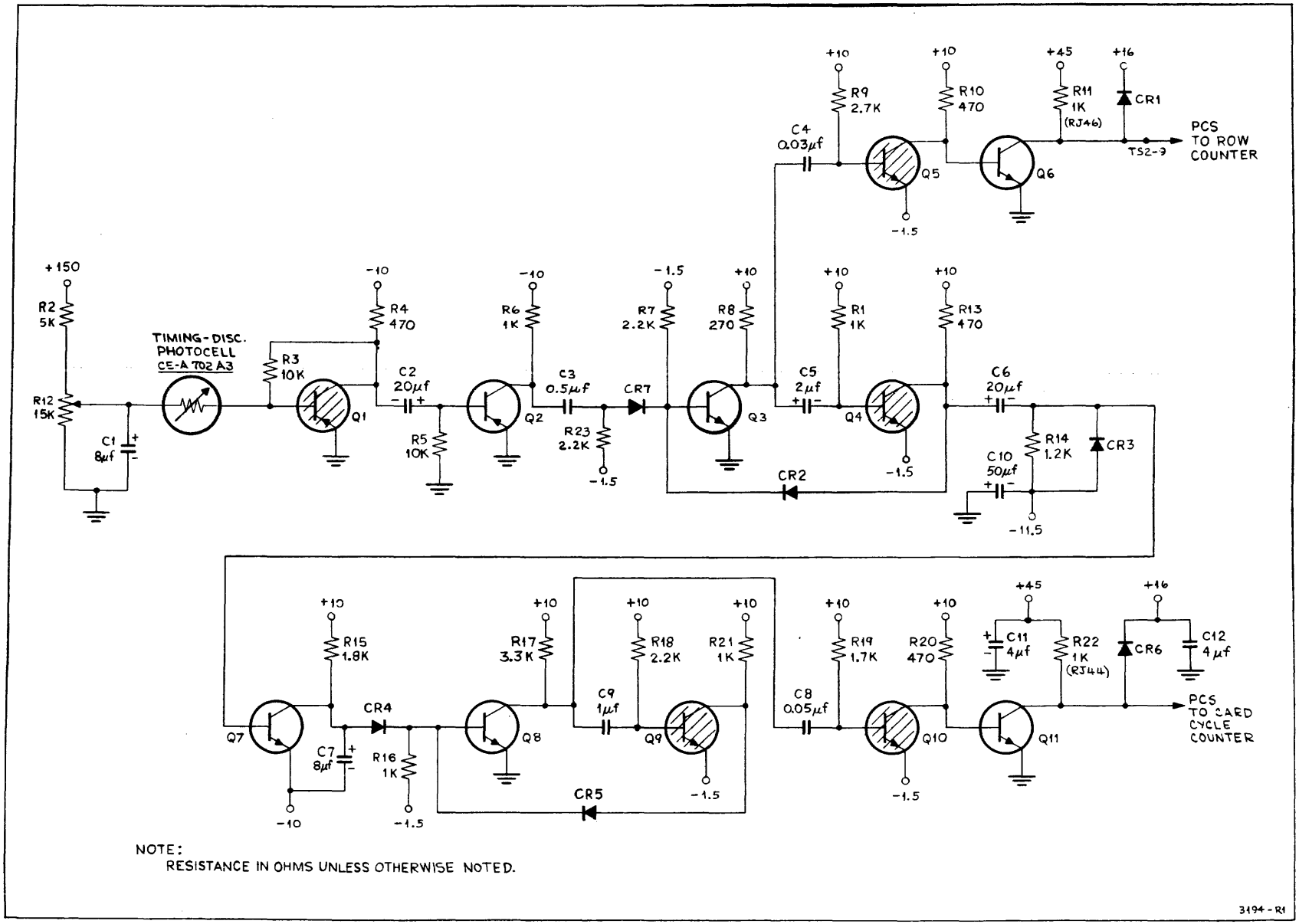


Figure 4-5. Timing-Disc Photocell Circuitry, Schematic

In both stages Q6 and Q11, the output is clamped at +16 volts. When an input signal is applied to either of these stages, an output signal suitable for application to a magnetic amplifier is developed below the 16-volt level.

4-10. DETAILED DESCRIPTION. When no light from the exciter lamp is applied to the photocell, a very small dark current flows through the photocell (figure 4-5). This small current flows from the -10-volt supply through R4, R3, the photocell, the top of R12, and R2 to the +150-volt supply. Most of the current through R4 and R3, however, flows through the base and emitter of Q1 and forward-biases Q1 for class A operation. The sensitivity control (R12) provides a means for varying the bias should changes in the photocell, transistor parameters, or both, require it.

When a slot on the timing disc passes the exciter lamp, a pulse of light impinges upon the photocell. The conductivity of the photocell increases and the amplitude of the current flowing through R4, R3, the photocell, R1, and R2 increases. The increased current raises the Q1 base potential, causing a reduction in both the base-to-emitter current and the collector-to-emitter current of Q1. As the collector current decreases, the Q1 collector voltage falls toward -10 volts.

When the Q1 collector voltage falls below ground potential, C2 charges through R4 and the base and emitter of Q2. The C2 charge current causes Q2 to turn on, current to flow from the -10-volt supply through R6 and Q2 to ground, and the Q2 collector voltage to rise to ground potential.

As the Q2 collector voltage rises to ground potential, C3 charges through the emitter and base of Q3, CR7, and the collector and emitter of Q2. The C3 charge current causes Q3 to turn on, current to flow through Q3 and R8, and the Q3 collector voltage to drop to ground potential. The output of Q3 is R-C coupled to both Q4 and Q5. As the output of Q3 approaches ground potential, C4 discharges through R9, blocking the Q5 emitter-to-base current; C5 discharges through R1, blocking the Q4 emitter-to-base current.

As Q5 turns off, and the Q5 collector voltage rises above ground potential, a current through the emitter and base of Q6 and R10 causes Q6 to turn on. The current through Q6 and R11 makes the Q6 collector voltage fall to ground potential.

When Q6 is in its normal nonconducting state, a current from the +16-volt supply through CR1 and R11 to the +45-volt supply clamps the collector of Q6 at +16 volts through CR1. Each time a pulse of light is applied to the photocell a negative-going output signal (PCS) from Q6 is applied to the row counter. Twelve such output signals are produced for each revolution of the timing disc.

Transistors Q3 and Q4 make up a delay-flop circuit. When Q3 turns on, C5 discharges through R12 and blocks the Q4 emitter-to-base current. Transistor Q4 turns off and the Q4 collector voltage rises above ground potential.

A feedback path is provided from Q4 to Q3 through CR2. As the Q4 collector voltage rises above ground potential, CR2 turns on and current flows through the emitter and base of Q3, CR2, and R13 to the +10-volt supply. The current holds Q3 on until C5 is discharged. As C5 discharges, the Q4 base potential rises above -1.5 volts, and current flows through the base and emitter of Q4 and R1. As Q4 turns on, the Q4 collector voltage falls to -1.5 volts, turning off both CR2 and Q3.

During the time Q4 is cut off, C6 charges through the emitter and base of Q7 and R13. When Q4 turns on, a d-c restorer, CR3, provides a fast discharge path for C6, to put the base of Q7 at -11.5 volts almost immediately.

The C6 charge current turns on Q7, increases the current through Q7 and R15, and lowers the Q7 collector voltage to -10 volts. When both the emitter and collector of Q7 are at -10 volts, no voltage develops across C7. When the Q7 input signal is removed, C7 charges through R15, allowing the collector potential of Q7 to rise above -10 volts at a rate determined by the time constant of the C7 charging circuit, which is greater than 7 milliseconds. If another positive input pulse is applied to Q7 before C7 has time to charge, no positive potential develops on the collector of Q7. Therefore no input signal is applied to Q8.

During each revolution of the timing disc, the unslotted segment of the disc blocks light from the photocell for a duration of three pulse times. When no light impinges upon the photocell no input signals are applied to Q7. Capacitor C7 has time to charge, a positive potential develops on the collector of Q7, and current flows from ground through the emitter and base of Q8, CR4, and R15 to the +10-volt supply. When Q8 turns on, its collector voltage drops to ground potential and the output signal is R-C coupled to both Q9 and Q10.

The combination of Q8 and Q9 makes up the delay-flop portion of a retriggerable delay-flop. When Q8 turns on, C9 discharges through Q8 and R18, blocking the Q9 emitter-to-base current. Transistor Q9 turns off, and the Q9 collector voltage rises above ground potential.

A feedback path is provided from Q9 to Q8 through CR5. As the Q9 collector voltage rises above ground potential, CR5 turns on and current flows through the emitter and base of Q8, CR5, and R21. The current holds Q8 on until C9 is discharged. As C9 discharges, the Q9 base potential rises above -1.5 volts, and current flows through the base and emitter of Q9 and R18. As Q9 turns on, the Q9 collector voltage falls to -1.5 volts, turning off both CR5 and Q8.

While Q8 is on, C8 discharges through Q8 and R19, blocking the Q10 emitter-to-base current. The signal developed blocks the current through Q10 and R20 so that the collector voltage of Q10 and the base voltage of Q11 rise above ground potential. When a positive potential is applied to the base of Q11, increasing the current through Q11 and R22, the Q11 collector voltage drops to ground potential. A negative-going input to the card-cycle counter is produced.

Normally Q11 is reverse-biased through Q10. When the Q11 collector current is cut off, a current from the +16-volt supply through CR6 and R22 to the +45-volt supply clamps the collector of Q11 at +16 volts. One negative-going output signal is produced for each revolution of the timing disc. It occurs when the unslotted segment of the timing disc blocks light from the photocell long enough for C7 to charge.

4-11. SIGNAL GENERATOR CIRCUITS

4-12. GENERAL DESCRIPTION

The circuitry for developing the clear signals is actuated by a generate-clear-and-probe signal applied to the actuator-transistor package (ATP) in the processor. The output of the ATP, shown in figure 4-6, is applied to the clear delay-flop circuit in the card reader. The duration of the clear pulses is set in the delay-flop, whose output is amplified by Q4. Amplifier Q4 provides the driving signals for the four clear signal output stages.

The clear 1 signal is applied to amplifier Q9. This stage is triggered by the trailing edge of the clear 1 signal so that the leading edge of the probe signal immediately follows the trailing edge of the clear signal. The output of Q9 drives the probe delay-flop which sets the duration of the probe signals. The delay flop provides the driving signals for the two probe-signal output stages.

The probe 1 signal is applied to amplifier Q14. This stage is triggered by the trailing edge of the probe 1 signal so that the leading edge of the brush-storage-loaded signal immediately follows the trailing edge of the probe signal. The output of Q14 drives a delay-flop which sets the duration of the brush-storage-loaded signal. The delay-flop output is amplified in the brush-storage-loaded signal output stage Q17.

The capacitor-sense signals are developed in the processor in the capacitor-sense-driver packages (CSD) shown in figure 4-1. A CSD package consists of two transformer-coupled transistor-amplifier stages. A steady flow of input signals keeps both stages cut off, with no output. When the input signals are removed, both stages conduct and a capacitor-sense signal is produced.

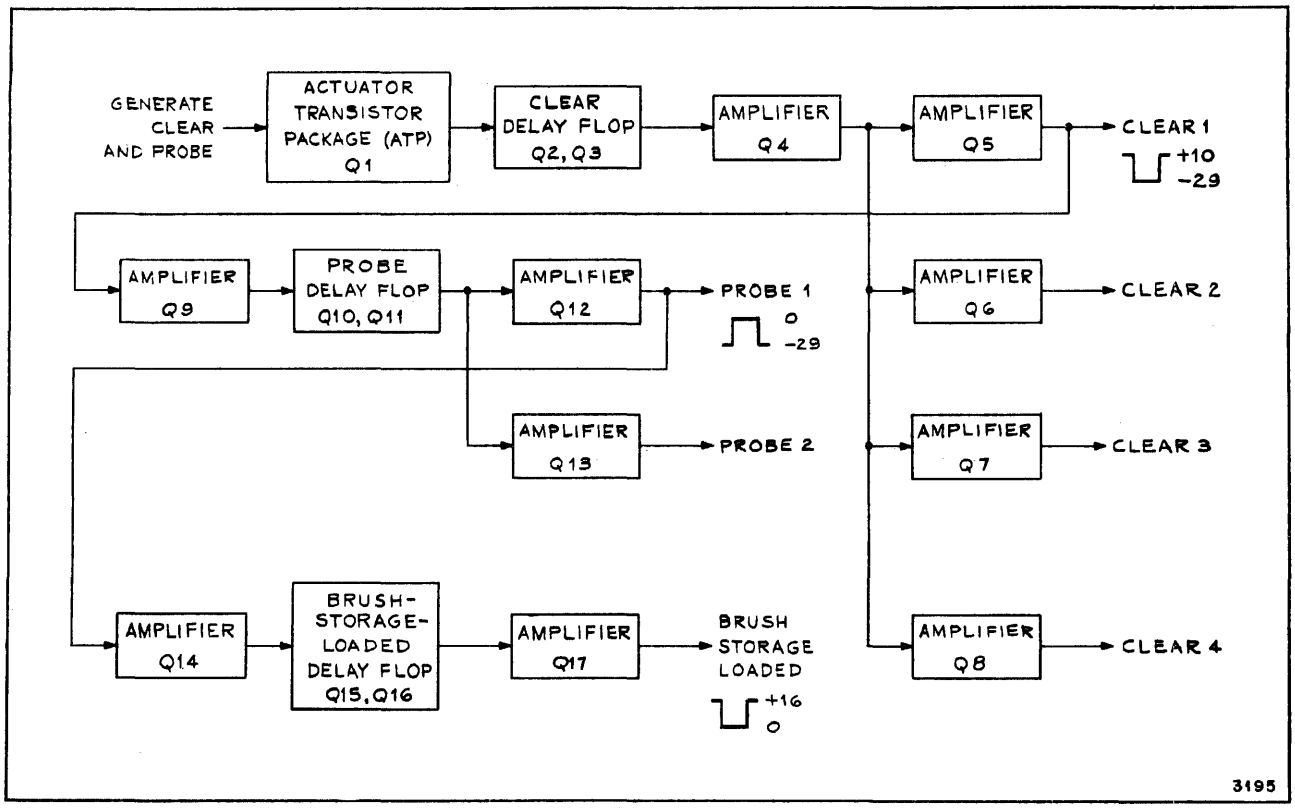


Figure 4-6. Clear, Probe, and Brush-Storage-Loaded Signal Generator, Block Diagram

4-13. CLEAR SIGNAL

In the actuator-transistor package shown in figure 4-7, the application of reverse bias normally holds Q1 off. A current through CR1 and R2 clamps both the collector of Q1 and one side of C1 to +16 volts. Another current, through CR2 and R3, clamps the other side of C1 to +6 volts. While Q1 is off, C1 charges to 10 volts through CR2 and R2.

When the positive generate-clear-and-probe signal is applied to the base of Q1, transistor Q1 turns on and the collector voltage decreases to +6 volts. The major part of the C1 discharge current flows through Q1, CR3, and the base and emitter of Q2, turning on Q2.

Transistors Q2 and Q3 make up a monostable delay-flop in which Q2 is normally off and Q3 is normally on. Current through R10, R5, CR4, and the base and emitter of Q3 holds Q3 on. When Q2 turns on, C3 discharges through Q2, R10, and R5. The cathode of CR4 becomes positive, turning off the diode to prevent the Q3 base potential from exceeding +6 volts. As the Q3 base potential rises to +6 volts, Q3 turns off and the collector voltage goes negative. The negative-going voltage allows a current through R6 and Q4 to turn Q4 on, completing another current path through R9 and Q2.

A feedback signal holds Q2 on until C3 discharges. Then CR4 turns on and current flows through R10, R5, CR4, and the base and emitter of Q3. The Q3 collector voltage rises to +3 volts, turning off both Q4 and Q2. Capacitor C3 charges through R4, CR4, and the parallel path provided by Q3 and R7. The delay-flop is now restored to its normal state.

When the delay-flop is in its driven or set state and the Q3 collector voltage is negative, a current through R8, R6, and the base and emitter of Q4 turns Q4 on. As the Q4 collector voltage rises toward ground potential, current flows through the emitter and base of Q5, R27, and Q4. The collector of Q4 and the base of Q5 are normally clamped slightly below -29 volts by a current through R12 and CR5. A current through CR6 and R13 clamps the collector of Q5 at +10 volts. When the Q4 collector voltage rises to ground potential, CR5 turns off; Q5 turns on. An amplified current through Q5, CR20, and R13 causes the Q5 collector voltage to drop to -29 volts. This negative-going signal is the clear signal.

The duration of the clear signals is determined by the time constant of the C3 discharge circuit, which is set by the adjustment of R10.

The output load is divided among four stages, all driven by Q4. The operation of Q6, Q7, and Q8 is identical with the operation of Q5.

4-14. PROBE SIGNAL

The circuit that generates the probe signal is shown in figure 4-7. A current through R24 and CR13 places a reverse bias on Q9 equal to the voltage drop across CR13. The clear-signal output of Q5 is applied to Q9 through C4 and R23. The leading edge of the clear signal, being in a negative direction, increases the current through R23 and CR13, charging C4 toward -29 volts. However, increasing the current through the diode has little effect on the voltage drop across it. The trailing edge of the clear signal causes CR13 to turn off. It also causes part of the C4 discharge current to flow through the emitter and base of Q9, and R23. The current through the Q9 input circuit turns Q9 on, so that current flows from the -1.5-volt supply through the emitter and collector of Q9 and through the base and emitter of Q10 to ground. Amplifier Q9 functions only on the trailing edge of an input clear signal.

Transistors Q10 and Q11 make up a delay-flop in which Q10 is normally off and Q11 is normally on. Current through R11, R26, CR14, and the base and emitter of Q11 holds Q11 on. The Q11 collector voltage, which is held at +3 volts, is applied to the base of Q10 through R29 to maintain reverse bias on Q10.

When the Q9 collector voltage drops to -1.5 volts, Q10 turns on, C7 discharges through R11, R26, and Q10, and diode CR14 turns off to prevent the Q11 base voltage from exceeding +6 volts. As the base voltage rises to +6 volts, Q11 turns off. The negative-going Q11 collector voltage permits current to flow through R30 and the parallel path consisting of R31 with Q12 and R29 with Q10.

The feedback signal holds Q10 on until C7 discharges. When C7 discharges, CR14 turns on and current flows through R11, R26, CR14, and the parallel path consisting of Q11 and R28. When Q11 turns on, the Q11 collector voltage rises to +3 volts, turning off both Q12 and Q10.

The collector of Q12 is normally clamped at -29 volts by a current through R32 and CR15. When Q11 turns off, a current through R30, R31, and the base and emitter of Q12 turns Q12 on. An amplified current through R32 and Q12 turns CR15 off. The Q12 collector voltage rises to ground potential, producing a positive-going probe signal.

The load is divided between stages Q12 and Q13, both of which are driven by Q11. Stages Q12 and Q13 are identical in operation.

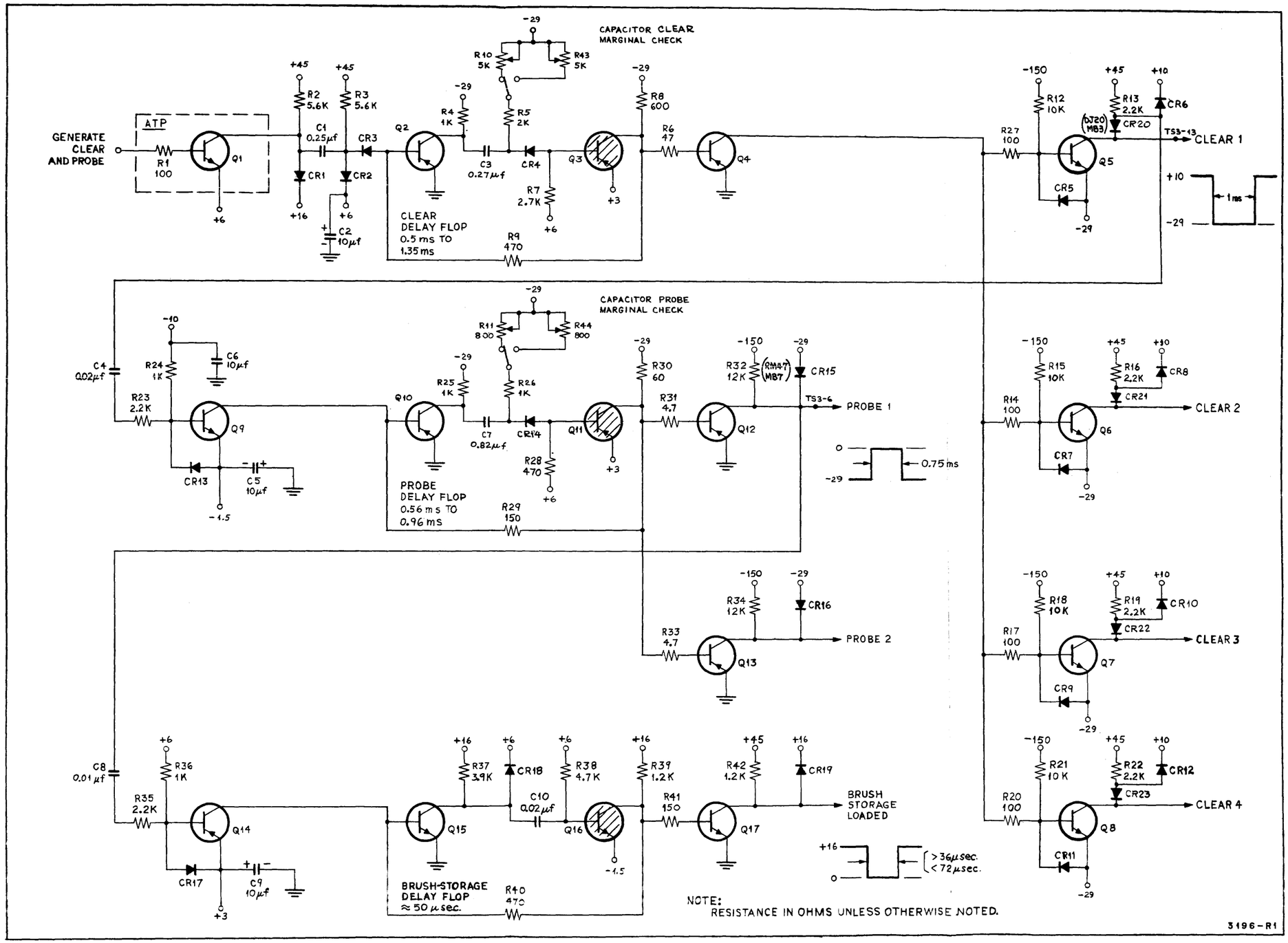


Figure 4-7. Clear, Probe, and Brush-Storage-Loaded Signal Generator, Schematic

4-15. BRUSH-STORAGE-LOADED SIGNAL

The circuit that generates the brush-storage-loaded signal is shown in figure 4-7. A current through CR17 and R36 normally places a reverse bias on Q14 equal to the voltage drop across CR17. The probe-signal output of Q12 is applied to Q14 through C8 and R35. The leading edge of the probe signal, being in a positive direction, increases the current through CR17 and R35 to discharge C8 to approximately zero volts. Increasing the current through the diode has very little effect upon the voltage across the diode. When the trailing edge of the probe signal turns CR17 off, part of the C8 charging current flows through R35 and the base and emitter of Q14. After the current through the Q14 input circuit turns Q14 on, current flows through the emitter and base of Q15 and through the collector and emitter of Q14 to the +3-volt supply. Amplifier Q14 functions only on the trailing edge of an input probe signal.

Transistors Q15 and Q16 make up a delay-flop circuit in which Q15 is normally off and Q16 is normally on. The collector of Q15 and one side of C10 are clamped at +6 volts by current through CR18 and R37. A current through the base-emitter circuit of Q16 and through R38 keeps Q16 conducting. The Q16 collector current flows through R39 to put the Q16 collector voltage at -1.5 volts, which is applied to the base of Q17 and Q15, maintaining reverse bias on both stages.

When the Q14 collector voltage rises to +3 volts, Q15 turns on and C10 discharges through Q15 and R38. The C10 discharge current blocks the Q16 emitter-to-base current and the Q16 collector voltage rises above ground potential. This positive collector voltage permits current to flow through the emitter and base of Q17 and R41, and through the emitter and base of Q15 and R40.

The feedback signal to Q15 holds that stage on until C10 discharges. When C10 discharges, letting the Q16 base potential rise above -1.5 volts, current flows through the base and emitter of Q16 and R38. The Q16 collector voltage falls to -1.5 volts, cutting off the input currents through both Q17 and Q15.

The collector of Q17 is normally clamped at +16 volts by current through CR19 and R42. When the Q16 collector voltage becomes positive, Q17 is turned on by current through R41; an amplified current flows through Q17 and R42. As Q17 collector voltage drops to ground potential, a negative-going brush-storage-loaded signal is developed.

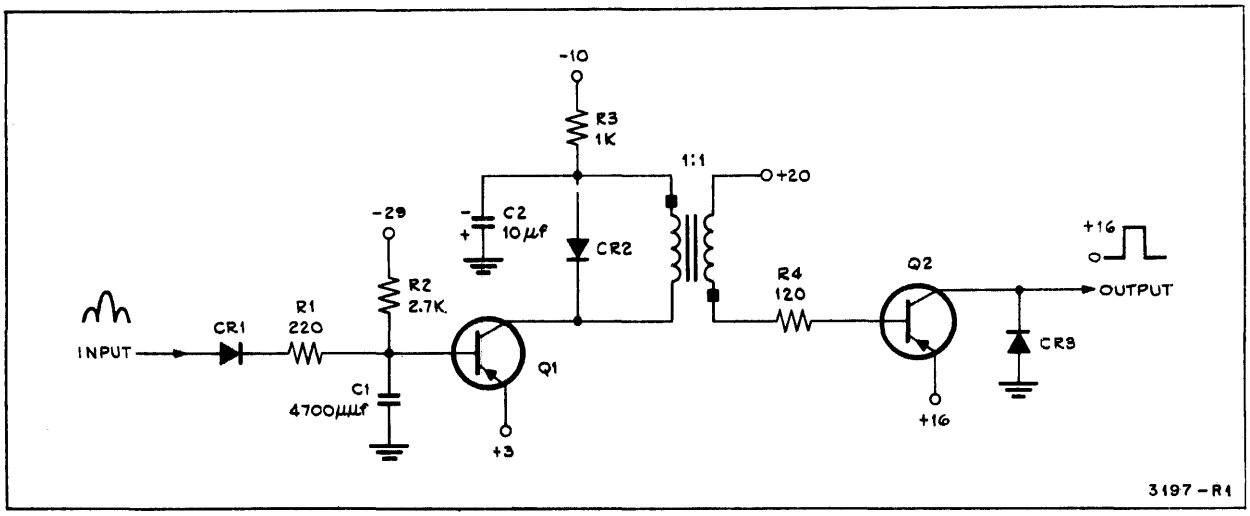


Figure 4-8. Capacitor-Sense-Driver Circuit

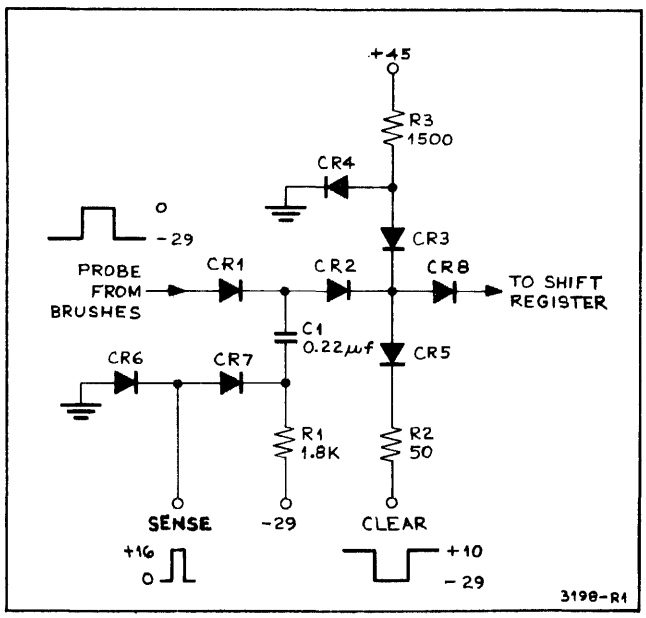


Figure 4-9. Intermediate Storage Circuit

4-16. CAPACITOR-SENSE SIGNAL

Normally a steady flow of input signals is applied to the capacitor-sense-driver circuit shown in figure 4-8. Capacitor C1 charges through R1 on the peaks of the input signals, and discharges through R2 during blocking-pulse time. Resistors R1 and R2 are chosen so that the base of Q1 is normally held above +3 volts, Q1 is biased beyond cutoff; Q2 is also biased beyond cutoff, and the Q2 collector voltage is clamped at ground potential through CR3.

In the absence of input signals, C1 discharges through R2. The resulting current through R2 and the base-emitter circuit of Q1 drives the stage to saturation. The 1:1 transformer produces signal inversion. When Q1 turns on, a negative-going signal developed at the base of Q2 drives Q2 to saturation. The Q2 collector voltage increases to +16 volts, and a sensing-signal output is produced.

At the end of the word time, when input signals again charge C1, transistor Q1 is again driven beyond cutoff. Diode CR2 prevents the collapsing-magnetic field from developing a large voltage across the transformer primary. Because of the action of CR2, the Q2 collector-voltage rating is not exceeded.

Any abnormal condition in which clock signals are absent for an extended period develops a high forward bias on Q1. The combination of R3 and C2 acts as a limiting device to prevent the Q1 collector dissipation from becoming excessive.

Resistor R1 limits the input current to prevent loading the driving magnetic amplifier. Resistor R4 limits the base current through Q2.

4-17. INTERMEDIATE-STORAGE CIRCUIT

The intermediate-storage circuit contains a separate capacitor for each sensing brush in the card reader. The information read from a punched card by a given brush is stored as an electrical charge on the corresponding capacitor.

The following description is for the circuit associated with one brush (figure 4-9). The operation of the storage circuits for the other brushes is identical.

The lower end of C1 is normally clamped to ground potential through CR6 and CR7 by the current through R1, CR7, and CR6. When a clear signal is applied, a charging current through R2, CR5, CR2, C1, CR7, and CR6 charges C1 to approximately 29 volts.

A positive-going probe signal is now applied to the sensing roll directly beneath the card being read. If the brush makes contact with the sensing roll through a hole in the card, C1 discharges to zero volts by a current through R1 and CR1. If there is no hole in the card at the position being read, the card insulates the brush from the roll, and C1 retains its 29-volt charge. Thus the state of charge on C1 indicates the presence or absence of a hole in the card at the position being read.

During capacitor read-out time, the +16-volt sense signal is applied between CR6 and CR7. Diode CR6 turns off, raising the potential at the bottom of C1 to +16 volts. If the brush has not read a hole in the card, the 29-volt charge on C1 is sufficient to keep CR2 reverse-biased and the circuit experiences no further change. If the brush has read a hole in the card, and C1 is discharged, the sense signal causes a current through CR8, CR2, C1, and CR7 to develop a signal in the shift register.

Diode CR2 is a buffer diode between the capacitor and a common line to which other capacitors are also buffed. A clamp circuit consisting of CR3, CR4, and R3 prevents diode leakage current among the capacitors. If a capacitor which had not been discharged through its associated brush were connected to a leaking CR2 diode, a current from the charged capacitor would distribute the charge among all of the discharged capacitors buffed to the same line through their CR2 diode. Because CR4, R3, and the +45-volt supply clamp one side of CR3 to ground, however, the leakage current flows through CR2, CR3, and R3 to prevent any undesired charging of the discharged capacitors.

NOTE

Section V, Maintenance, will be supplied at a later date.

Type 7902 Card-Sensing Punch Unit
90 Column

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I

INTRODUCTION

1-1. SCOPE OF THE MANUAL

The purpose of this manual is to describe the type 7902 card-sensing punch unit, one of the three input-output devices in the New Univac system. The manual describes the mechanical and electromechanical components of the read-punch unit (RPU), as well as the logical control circuits and instructions that control it. To understand the operation of the read-punch synchronizer which involves logical circuits and the processing of instructions, familiarity with Manual No. 1 is necessary.

In section II, the physical layout of the read-punch unit is described. Section II also includes functional descriptions of certain parts not directly controlled by instructions from the processor. Section III explains the operation of the mechanical, electromechanical, and logical components of the read-punch unit, individually and then as applied to the instructions that control the device. Section IV describes the electronic circuitry.

1-2. REMINGTON RAND PUNCHED CARD

The information processed by the read-punch unit is punched on Remington Rand cards. Information read by the read-punch unit in card code must be translated into UCT code before the processor can perform arithmetic operations with the information.

The Remington Rand card is described in section 1-2 and shown in figure 1-1 of the card reader manual.

1-3. GENERAL FUNCTIONAL DESCRIPTION

The read-punch unit is an input-output device which both reads and punches 90-column Remington Rand cards. As shown in figure 1-1, it consists of an input bin, two read stations, a punch station, and two output stackers. Under normal operating conditions, it processes cards at a speed of 150 per minute.

When either prepunched or blank cards are loaded into the unit, they are read at read station 1. The sensed information is temporarily stored in intermediate storage, then transferred to a special area on the storage drum known as the card-buffer band. From the buffer, the information is transferred to a main-storage band. After computations are made, new information is returned to the read-punch unit and punched into the cards. The cards are then read at read station 2 to enable a programmed check on the accuracy of both the first reading and the punching operation. If an error occurs, the

card involved may be separated from the output deck under program control.

The following three instructions control the functions of the read-punch unit:

81: Read, punch, and move cards.

46: Transfer sensed information from buffer storage to main storage.

57: Sort.

These instructions are explained in detail in section 3-43 of this manual.

1-4. CHARACTERISTICS

The following list gives the physical and electrical characteristics of the read-punch unit.

Dimensions

Width	31-7/8 in.
Length	45-1/16 in.
Height	68 in.

Approximate Weight	1100 lb
Card Feed Rate	150 cpm

	Motor	Blower	Relay Power-Supply
Voltage	110 v ac	110 v ac	110 v ac
Frequency	60 cps	60 cps	60 cps
Phase	single	single	single
Current	8 amp	3 amp	0.5 amp

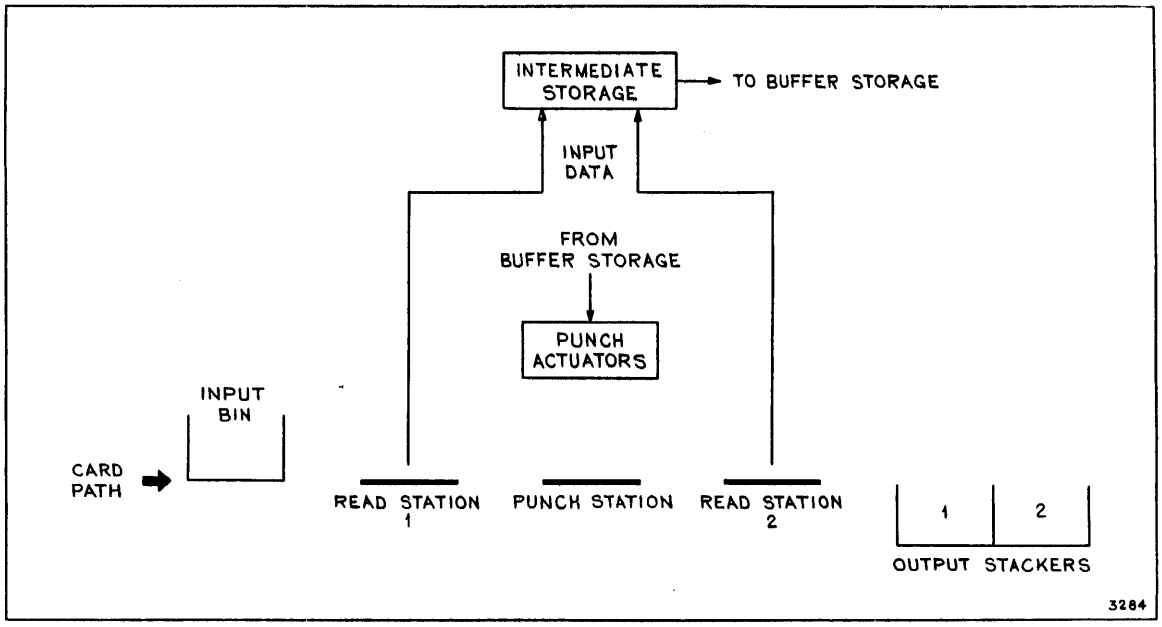


Figure 1-1. Read-Punch Unit, Block Diagram

SECTION II

PHYSICAL DESCRIPTION

2-1. SCOPE

This section is a description of the important mechanical components of the read-punch unit. Only those parts which are essential to the general function of the unit are discussed. Most of the packages of the read-punch synchronizing circuits are located within the processor cabinet and are described in section 3-23. Designations like (2-4,3) refer to figures; for example, figure 2-4,3 is connector plug B.

2-2. CARD INPUT SYSTEM

2-3. INPUT BIN

The input bin (2-1,1) at the right-hand side of the read-punch unit holds the deck of cards from which information is to be read and on which information is to be punched. Cards, placed face up in this bin with the top edge toward the unit, are fed from the bottom of the deck into read station 1.

The input bin, or card-feed magazine, consists of two vertical guides (2-1,2), and has a capacity of approximately 600 cards. When the last card in the deck enters the feed rollers, a pressure-operated microswitch (2-1,9) under the bin causes the read-punch unit to stop and lights the INPUT MAGAZINE indicator on the read-punch control panel. The empty-magazine switch is always open except when the presence of a card in the input bin closes it.

2-4. CARD-LIFTING LEVER. A card-lifting lever (2-1,3) in the right rear corner of the input bin can be depressed to aid in removing unprocessed cards.

2-5. CARD WEIGHT. A card weight must be fitted over the top card in the input deck to insure a positive, uniform feed down to and including the final card.

2-6. THROAT KNIFE AND BLOCK

The deck of input cards rests on a rectangular plate called the throat block. The throat knife (2-1,11) is a vertical plate mounted between the cards and the feed rollers, with a narrow slit between its bottom edge and the throat block. Because the slit is narrower than the thickness of two cards, only one card at a time can enter the read station. An adjusting screw is provided to adjust the width of the slit.

2-7. FEED-ARM ASSEMBLY

The feed-arm assembly is the mechanism that picks the bottom card of the input deck and pushes it into the transport system.

The feed arm (2-1,4) is mounted vertically under the input bin and pivots on the feed shaft (2-1,5), which is mechanically linked (2-2,5) to a cam on the front end of the main drive shaft under read station 1. A mechanical linkage also connects the feed arm to the feed slide and the pickerknife assembly, which moves back and forth under the deck of cards.

The pickerknife head forms a movable part of the card-feed bed. The pickerknife, mounted on the rear face of the pickerknife head, is adjusted so that its upper edge projects 0.005 inch above the head, engaging the card. Adjustment and locking screws are provided on the pickerknife assembly.

2-8. DRIVE ASSEMBLY

2-9. MOTOR

The drive motor (2-1,8; 2-5,8) which provides mechanical power for the read-punch unit is located in the lower right section of the unit under the input bin. It is connected by a V-belt drive (2-1,6; 2-3,13) to the clutch-and-brake solenoid assembly (2-2,3; 2-3,14). A flywheel encased in a protective housing (2-2,6) is attached to the motor shaft.

2-10. CLUTCH-AND-BRAKE ASSEMBLY

The motor is connected with an electromagnetic clutch-and-brake assembly on the rear of the unit (2-2,3; 2-3,14). The clutch-and-brake shaft runs the length of the rear of the read-punch unit. It is encased in a housing (2-3,15) which also contains gearing for the three main drive shafts and for the card-feed rolls.

2-11. DRIVE-SHAFT ASSEMBLIES

The three main drive shafts (2-3,1; 2-6,4,6 and 9) extend through the unit under the two read stations and the punch station. Several important parts attached to these shafts are discussed in the following paragraphs.

2-12. TIMING DIALS. A timing dial (2-3,2) graduated into 360 degrees is mounted on the back end of each of the three drive shafts. The dials are used to indicate what point of the card cycle the read-punch unit has reached at any given moment. The read-punch unit is at rest between 260 and 275 degrees.

2-13. CAM-SWITCH ASSEMBLIES. A set of cams and a cam-switch assembly (2-3,12) are mounted on the rear of the left-hand and of the center drive shaft, between the timing dial and the end of the shaft. The two switch assemblies, designated as switches 7 and 8, each include seven separate switches. Each switch is driven by its own cam. The cams and associated switches are lettered from A through G, reading from the timing dial outward. The switches control various electrical operations which must be synchronized with the mechanical timing of the unit.

Other cam assemblies attached to the drive shafts initiate mechanical actions required in reading and punching cards; they are discussed in the sections which follow.

2-14. TRANSPORT SYSTEM

2-15. GEARS AND ROLLER ASSEMBLIES

The four main feed-roller assemblies which move cards through the read-punch unit are located between the input bin and read station 1 (2-1,10), at the input and the output of the punch station, and at the output of read station 2 (2-5,4). Each assembly consists of an upper and a lower roller. Steel bands at the ends of each roller move the card by friction, and several adjusting screws are provided to set the tension between the upper and lower rollers. Each of the four lower rollers is driven by gears encased in the clutch-and-brake shaft housing at the rear of the unit.

There are two intermediate roller assemblies in each station. Each assembly consists of four rollers, an upper and lower pair at the front and at the rear. The pairs do not extend across the card path, as do the feed rollers, but grip the edges of the card so as not to interfere with punching and sensing. The lower of the feed rollers following each station drives gearing to the shafts of the two lower intermediate rollers at the front of the station. Figure 2-6,8 shows the shafts in read station 1. The shafts of the rear intermediate rollers are driven directly from the clutch-shaft housing.

2-16. CARD-JAM SWITCHES

Of the three card-jam microswitches in the read-punch unit, two are located above the card path, at the input and the output of the punch station, and the third is below the card path, just beyond the final set of feed rollers. Each microswitch is actuated by a metal beam. If a card moves out of its normal path or overlaps another card, the beam closes the switch at which the jam occurs.

A card jam must be corrected manually. Before operations can begin again, it is necessary to press the jam-clear switch

(2-5,7) on the front of the main frame of the unit, left of the relay panel and below the final feed rollers.

2-17. OUTPUT STACKERS

The output stacker assembly consists of two bins (2-5,13) and the mechanism used to select either of them. Copper brush static eliminators (2-5,5) remove any static charge that the cards may accumulate, before they reach the stackers.

2-18. BINS. The two output bins, designated stacker 1 and stacker 0, are mounted in a hinged assembly (2-4,5) which swings out for maintenance and removal of the chip box. Stacker 1 is the closer bin to the feed rollers. Each bin is capable of holding 850 to 1200 cards, depending upon the setting of the stacker platform spring. When either bin is full, a microswitch (2-5,12) under the bin stops the unit and lights the OUTPUT BIN FULL indicator on the read-punch control panel.

The cards fall onto a spring-loaded (2-4,4) platform (2-2,12) which settles as the number of cards increases. The tension on the platform springs determines the rate at which the platform settles.

3-19. SELECTOR. A selector mechanism containing movable sort fingers directs cards into stacker 1 when a sort solenoid (2-5,6), mounted on a bracket along the output bins, is actuated. If a card is not directed into stacker 1, it passes over the sort fingers, and fixed fingers (2-5,14) deflect it into stacker 0.

2-20. SENSING SYSTEMS

The two card sensing stations operate identically and have the same type of mechanical and electrical connections. When in position in a read station, a card rests between two metal plates which have openings over the punching area. A station consists of the sensing-pin box below the card track, and the setup-pin box, switch pin (2-1,12; 2-5,3), and sensing-switch box (2-1,13; 2-5,2) above the card track. Electrical connections to the sensing switches are made at the hinged top of the sensing-switch box. For a detailed description of the mechanism contained in these boxes, refer to section 3-13.

2-21. OPERATING CAMS

Cams which operate the sensing mechanism are attached to the drive shafts under the stations. Motion of the sensing-pin box is controlled by a cam and eccentric strap inside the main frame, under the read-station. The cam (2-6,7) that operates the read-station card stop is mounted on the front end of the main drive shaft.

2-22. EMPTY-STATION SWITCHES

Microswitches under each sensing station test for the presence of cards during the read operation. If the station is empty, the switches close, stopping the unit and lighting one of the EMPTY STATION indicators on the read-punch control panel.

2-23. PUNCH SYSTEM

A fixed die section which receives the punches lies directly under a card in the punch station. Above the card, the punch station consists of a fixed die section used to guide the punches, a movable stripper plate and punch assembly, a movable set-bar assembly (2-2,13; 2-6,2), and a large, fixed, two-section assembly (2-2,1) containing the tower rods (2-1,14; 2-5,1), rocker arms, interposers (2-6,11), and actuator magnets (2-6,10) used in the punching operation. For a detailed description of these components, refer to section 3-14.

2-24. OPERATING CAMS

Punch operations are controlled by cams mounted on the drive shafts under the punch station and read station 1. A cam mounted on the front end of the read-station shaft operates the interposer-retract mechanism through a large, boomerang-shaped arm (2-2,2; 2-6,1 and 3). The set-bar-pin lock-slide assembly, interposer assembly, and punch-station card stop are operated by cams and linkage (2-2,11; 2-6,5) on the front of the center drive shaft, while movement of the set-bar and stripper-plate sections is controlled by separate cams inside the main frame on the center drive shaft.

2-25. CHIP BOX

Chips punched from the cards fall into a large chip box (2-4,2) below the punch station. The chip box fits into the area shown in figure 2-5,9. It must be removed and emptied periodically; the hinged output stacker assembly swings aside to give access to the box. When the box is full, the weight of the chips against the platform spring operates a microswitch (2-5,10) below the box, stopping the unit and lighting the CHIP BOX FULL indicator on the read-punch control panel.

2-26. CONTROL PANEL

The read-punch control panel consists of six pushbuttons, some illuminated, and nine indicator lamps, as shown in figure 2-7. The purpose of each pushbutton and indicator is explained in table 2-1.

Table 2-1. Read-Punch Control Panel

a. CONTROLS: six pushbuttons

Note: All of the pushbuttons are spring-loaded except MOTOR, which is alternate action.

Panel Marking	Function	Indication
MOTOR	Turns read-punch motor on. Pressed a second time, turns motor off.	Lights when operated.
COMPUTATION RUN	Starts processor computation.	Lights when operated.
COMPUTATION STOP	Stops processor computation.	Lights when operated or if processor stops for any reason.
SYSTEM OFF NORMAL/ CLEAR	Clears all internal controls, indicators, and flip-flops.	Lights if any abnormal condition occurs in processor, printer, card reader, or read-punch unit.
FEED ONE CARD	Feeds a single card, moves cards through unit, or both. (Operates under any abnormal condition except card jam.)	None.
RESET	Resets empty-station relays after stop caused by empty read station so that unit can be restarted.*	None.

*Pushbutton which resets read-punch unit after a card jam is not located on the control panel. Refer to section 2-16.

Table 2-1. Read-Punch Control Panel (cont)

b. INDICATORS: nine jewel-lights

Panel Marking	Function
OVERHEAT	Lights if internal temperature exceeds 135°F. Indicates that thermostats have removed ac and dc from entire system except drum motor.
INTERLOCK	Lights when door on front of package library is opened. Indicates that clutcl circuit is open and AOT flip-flop is set
AIR FLOW	Lights if air flow into blower motor is insufficient. Indicates that air vane switch has removed ac and dc from entire system except drum motor.
EMPTY INPUT MAGAZINE	Lights when input magazine is empty.*
EMPTY READ STATION 1	Lights if there is no card in read station 1 during a read operation.*
EMPTY READ STATION 2	Lights if there is no card in read station 2 during a read operation.*
OUTPUT BIN FULL	Lights when either of the output stackers is filled. Unit stops.
CHIP BOX FULL	Lights when chip box is filled. Unit stops.
MISFEED	Lights when a card jam occurs at any of three points along the card path. Unit stops.

*When this indicator is lighted, the read-punch unit stops unless EMPTY STATION INHIBIT switch on processor control panel has been pressed.

2-27. MISCELLANEOUS COMPONENTS

2-28. CONNECTORS

The read-punch unit is connected to the processor by three connectors: CPA (2-3,7) and CPB (2-3,5; 2-4,3) are 100-pin connectors carrying signals to and from the processor; CP51 (2-3,6) is a 37-pin connector carrying power for the read-punch unit.

Connector CPB carries the column-switch and TR" lines; CPA carries the TB and CS lines, as well as miscellaneous control signals. Twelve toggle switches (2-3,10) on the rear of the main frame, designated as the ROW DELETE switches, are used to break the connections of the TR" lines between barrier strip 15 and the CPB connector.

2-29. TERMINAL BOARDS AND BARRIER STRIPS

Interconnections within the read-punch unit are made through 17 terminal boards or barrier strips. Table 2-2 lists the use and location of each terminal board. Type TB designates terminal board; type BS designates barrier strip. See section II of the maintenance manual for addressing of mounting-board components.

2-30. PACKAGE LIBRARY

The package library (2-5,15) consists of four shelves, TA, TB, TC, and TD (2-4,6 through 9), each capable of holding 30 circuit packages. The library swings out on hinges for maintenance.

2-31. TRANSFORMERS

Two transformers (2-2,7) used in the two +70-volt power supplies are mounted on the relay panel (2-2,10). With the stacked selenium rectifiers (2-2,9) mounted next to them, the transformers make up the two +70-volt bridge-rectifier circuits which supply coil voltage to the read-punch relays and solenoids.

2-32. RELAYS

Of the ten relays used in the read-punch unit, nine are mounted on the relay panel (2-2,10). Relay 10, the main power relay (2-2,4), is mounted on the front of the main frame just below the control panel.

2-33. BLOWER

A blower circulates air through the read-punch unit. The blower motor (2-5,11; 2-4,1) is located in the lower part of the unit under the output stackers. The blower draws in

Table 2-2. Terminal Boards

Board	Use	Location
TB1	Mounting board	Rear side of relay panel
TB2	Mounting board	Rear side of relay panel
TB3	Connections to relay panel	Rear side of relay panel
TB4	Connections to input panel	Input panel (2-3,8)
TB5	Mounting board	Input panel (2-3,3)
TB6	Mounting board	Input panel (2-3,4)
TB7	Connections to control panel	Rear side of control panel
TB8	Connections to control panel	Rear side of control panel
TB9	Clutch-and-brake solenoid wiring	Main frame near brake and clutch
TB10	Card-jam-switch 1 connections	Main frame above card track
TB11	Card-jam-switch 2 connections	Main frame above card track
TB12	Blower, air flow, thermostat connections	Box below motor flywheel housing (2-1,7; 2-2,8)
TB13	Blower control connections	Next to TB12 (2-1,7; 2-2,8)
TB14	Card-jam-switch 3 connections	Main frame above card track
BS15	Signal distribution	Input panel (2-3,11)
BS16	Power distribution	Input panel (2-3,9)
TB17	Blower motor wiring	Inside motor compartment

external air through an air filter and then forces it up through the unit. The operation of the blower is entirely under the control of power control circuits in the processor; no blower controls are provided on the read-punch control panel.

2-34. AIR VANE

An air vane switch is mounted on the blower motor assembly. Unless air flowing through the assembly operates the switch, no a-c or d-c power can be applied anywhere in the New Univac system with the exception of the drum motor.

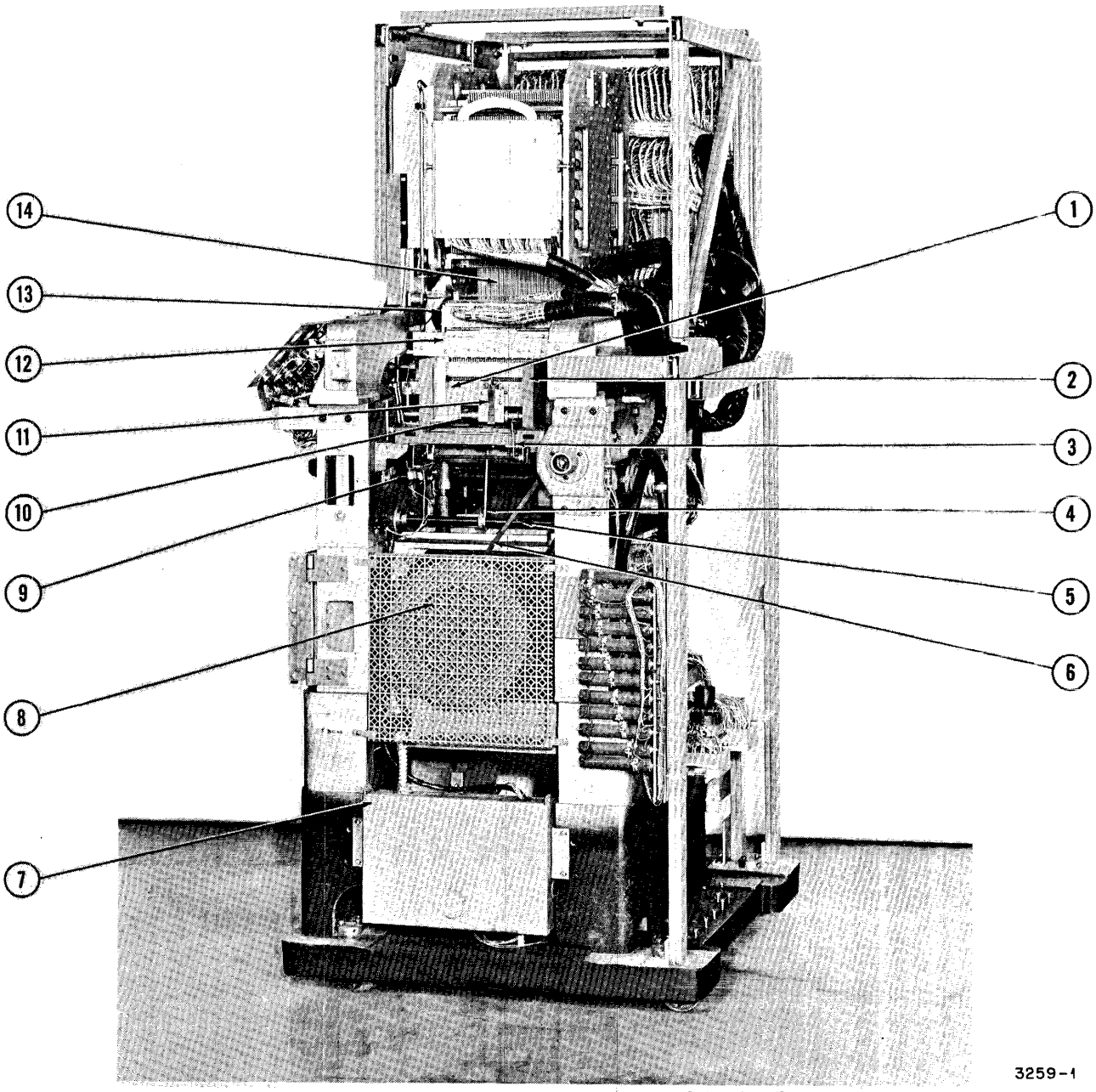


Figure 2-1. Read-Punch Unit, Input Side

1. Input bin
2. Vertical guide
3. Card-lifting lever
4. Feed arm
5. Feed shaft
6. Drive belt
7. Terminal boards 12 and 13
8. Drive motor
9. Empty-magazine switch
10. Main feed-roller assembly
11. Throat knife
12. Switch pin
13. Sensing-switch box
14. Tower rods

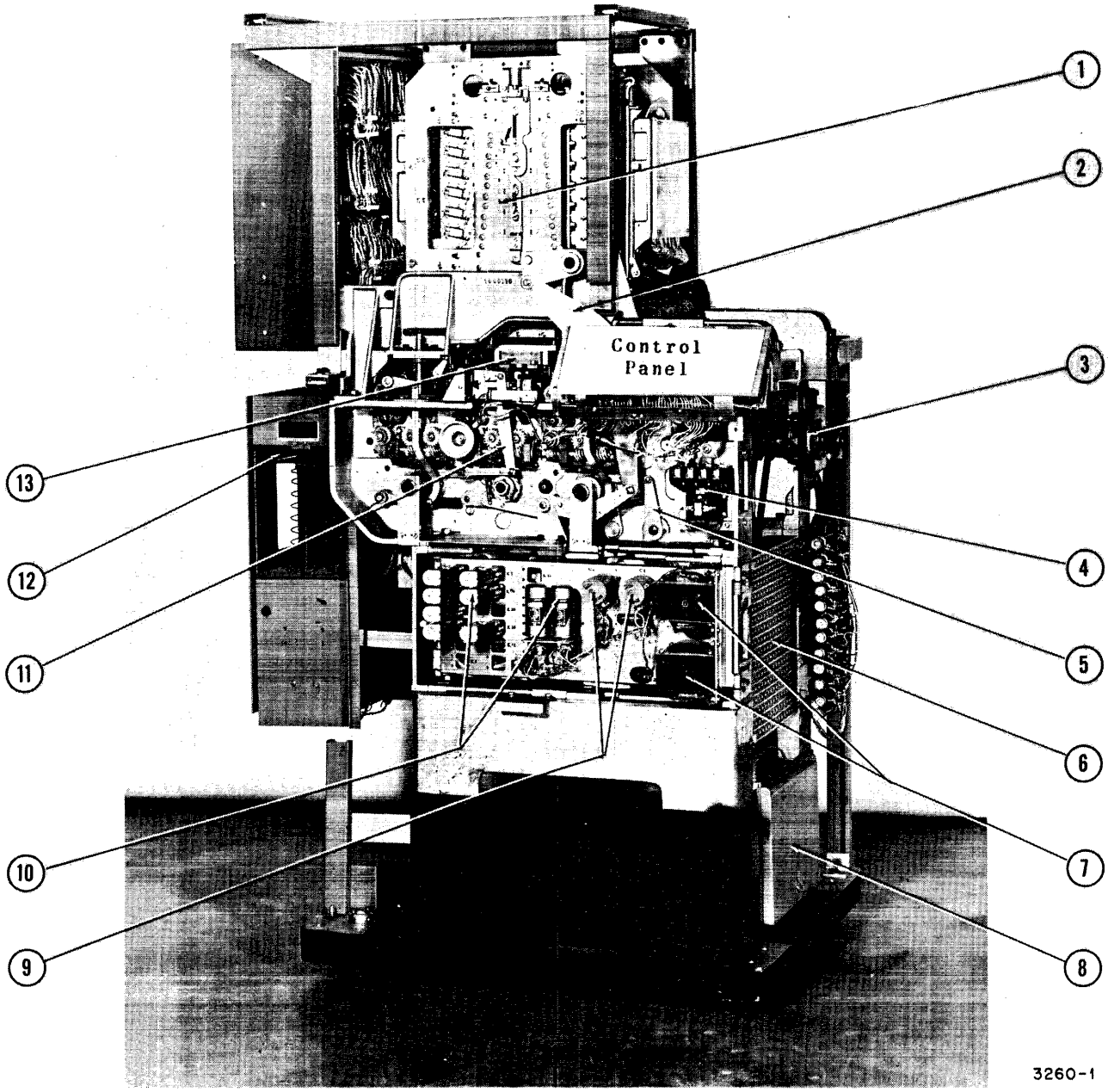


Figure 2-2. Read-Punch Unit, Front View

1. Tower-rod assembly
2. Interposer-retract-mechanism arm
3. Clutch-and-brake solenoid assembly
4. Relay 10 (main power relay)
5. Feed-shaft-link arm
6. Flywheel housing
7. Power-supply transformers
8. Terminal boards 12 and 13
9. Power-supply selenium rectifiers
10. Relay panel
11. Linkage, set-bar-pin lock slide
12. Output-bin platform
13. Set-bar assembly

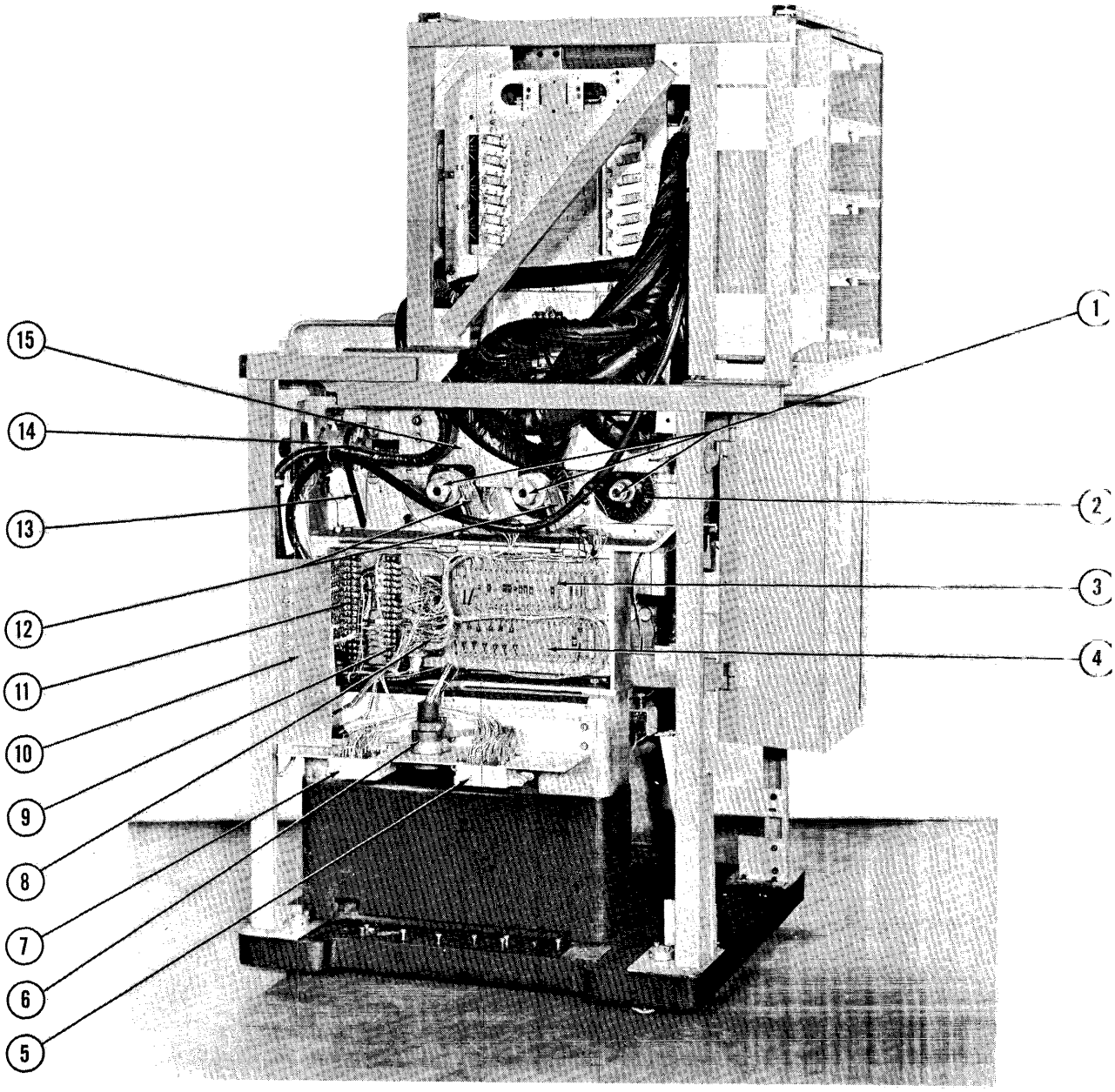


Figure 2-3. Read-Punch Unit, Rear View

1. Main drive shafts
2. Timing dial
3. Terminal board 5 (TB5)
4. Terminal board 6 (TB6)
5. Connector CPB
6. Connector CP51
7. Connector CPA
8. Terminal board 4 (TB4)
9. Barrier strip 16 (BS16)
10. ROW-DELETE switches (TR" lines)
11. Barrier strip 15 (BS15)
12. Cam-switch assembly
13. Drive belt
14. Clutch-and-brake solenoid assembly
15. Clutch-and-brake shaft housing

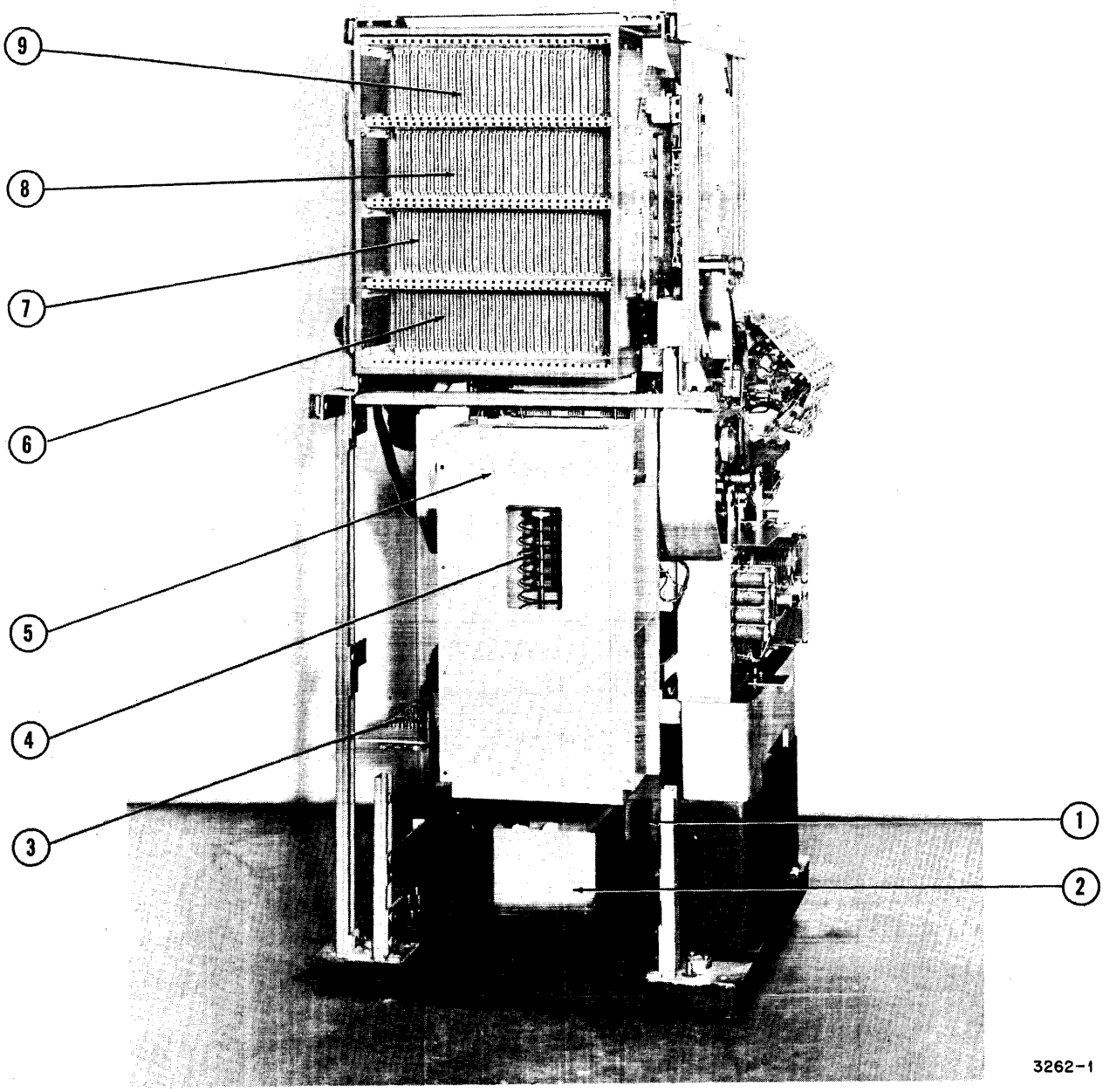


Figure 2-4. Read-Punch Unit, Output Side

1. Blower motor (not installed)
2. Chip box
3. Connector CPB
4. Platform springs
5. Output-bin assembly
6. Shelf TD
7. Shelf TC
8. Shelf TB
9. Shelf TA

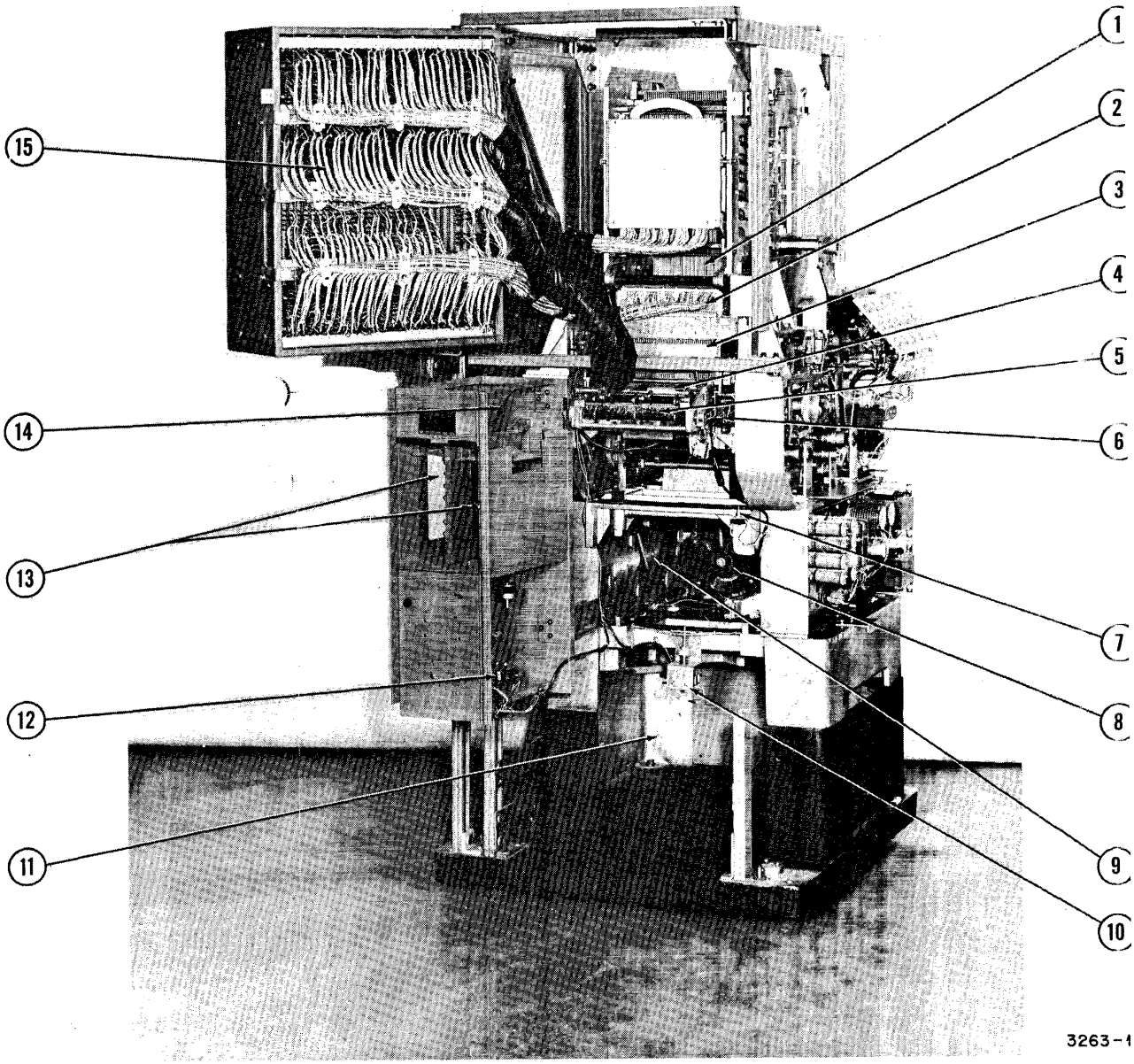


Figure 2-5. Read-Punch Unit, Output Side, Internal View

1. Tower rods
2. Sensing-switch box
3. Switch pin
4. Main feed-roller assembly
5. Static eliminators
6. Sort solenoid
7. Jam-clear switch
8. Drive motor
9. Chip-box area
10. Full-chip-box microswitch
11. Blower motor (not installed)
12. Full-output-bin microswitches
13. Output bins
14. Fixed fingers
15. Package library

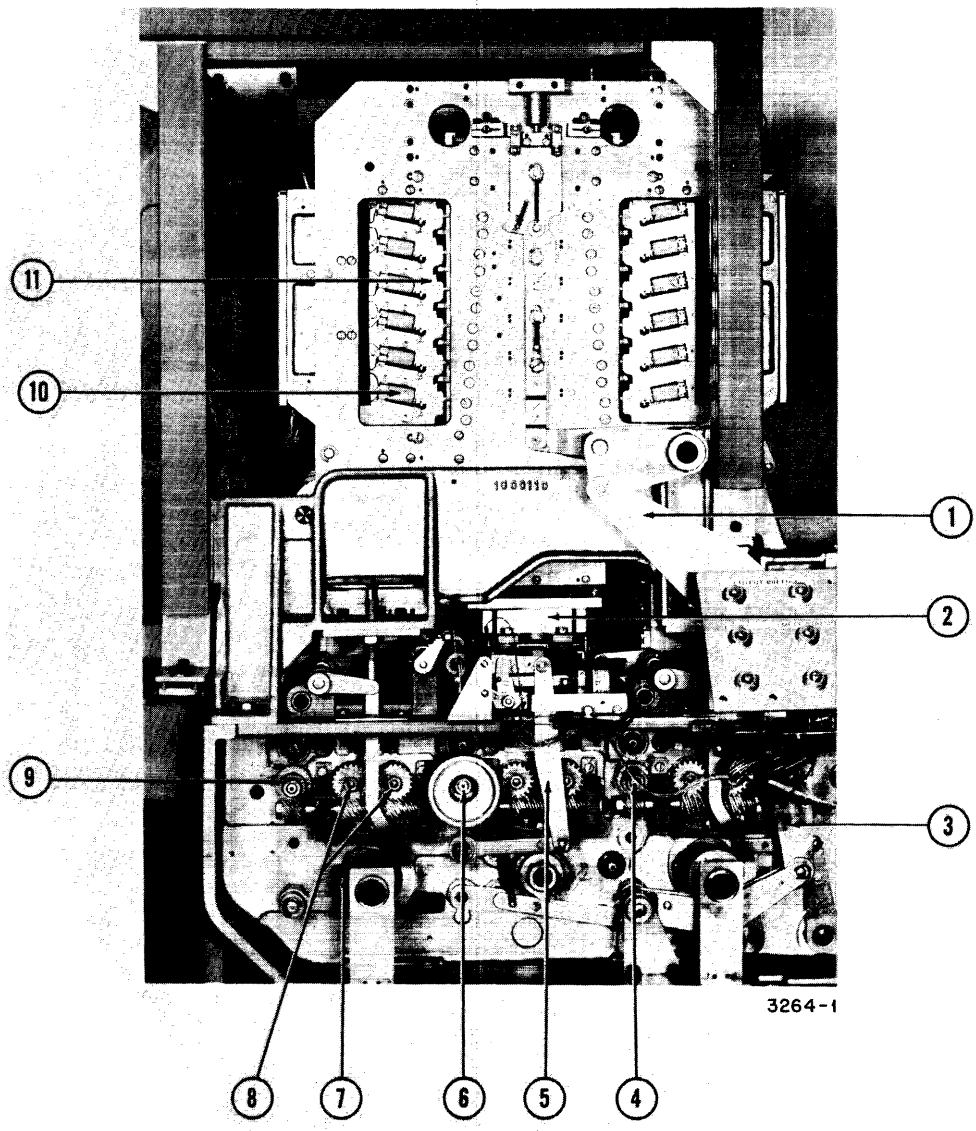


Figure 2-6. Punch Actuators and Feed-Roller Gears, Front View

1. Interposer-retract-mechanism arm
2. Set-bar assembly
3. Interposer-retract-mechanism arm
4. Main drive shaft
5. Linkage, set-bar-pin lock slide
6. Main drive shaft
7. Card-stop cam
8. Intermediate roller shafts
9. Main drive shaft
10. Actuator magnets
11. Interposer

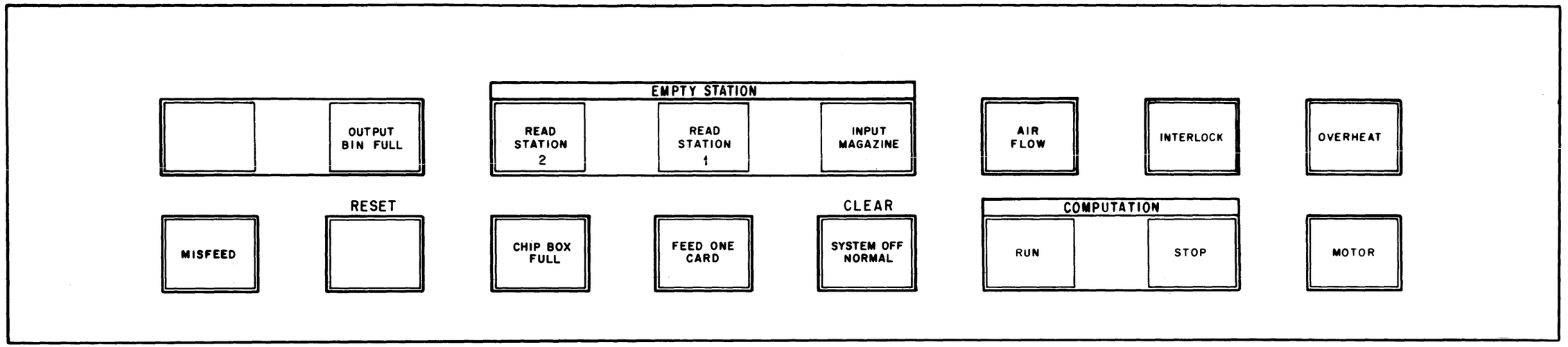


Figure 2-7. Read-Punch Control Panel

SECTION III

THEORY OF OPERATION

3-1. SCOPE

In this section, the mechanical, electromechanical, and logical components of the read-punch unit are first described in detail. Section 3-43 describes the instructions that control the normal operations of the unit, assuming a working knowledge of the components. Section 3-53 describes the abnormal conditions which can affect read-punch operations and the control of these conditions.

3-2. GENERAL DESCRIPTION

Operation of the read-punch unit is controlled by three instructions: 81, 46, and 57.

The 81 instruction is: Read the output words to be punched in a card from a main-storage band and write them onto the card buffer. Read the words from the card buffer and set up the punching mechanism accordingly. Feed a new card from the input bin and, at the same time, move each card into the next station, sending the end card into the output stackers. Read the card in each read station and write the input words from both cards onto the card buffer. Finally, punch the card in the punch station in accordance with the output words already set up.

The 46 instruction is: Transfer the input words from the card buffer to specified locations of a selected main-storage band.

The 57 instruction is: Operate the output stacker mechanism so that a given card falls into stacker 1, the first stacker, instead of into stacker 0, the last stacker.

Mechanical operation of the read-punch unit is initiated either by an 81 instruction in the program, or by operation of the FEED ONE CARD pushbutton on the control panel.

Normally, the operator depresses the FEED ONE CARD button three times to fill the three stations with blank cards before running a program. The three fill operations are completely mechanical, and no information is transferred to or from the processor. After the stations are loaded, an 81 instruction initiates card reading and punching. The 81 instruction, however, does not coincide with the beginning of a mechanical card cycle. It indirectly starts a card cycle, but, as shown in figure 3-2, it is given after approximately three-quarters of the card cycle initiated by the previous 81 instruction.

At the beginning of a mechanical card cycle, the cards in the two read stations (cards B and D in figures 3-1 and 3-2) are sensed. At 334 degrees of the card cycle, the sensed information from the two cards is transferred, in parallel and 90 bits at a time, from the sensing-switch matrix into intermediate storage. The information is then transferred ten bits at a time from intermediate storage into a shift register and written onto the card-buffer band. When the sensed information is completely written onto the buffer band, a 46 instruction is given to transfer the information from the buffer band to the main-storage band specified by the m address of the 46 instruction.

During the time the sensed cards are moving to the next stations, the processor carries out computations on the information read from the card moving into the punch station (card B). The information to be punched in that card is then stored in a main-storage band. Card C is punched with previously processed information, under control of the mechanical card cycle, while the data for card B is being computed.

The next 81 instruction is staticized in the static register, and output words are transferred from the main-storage band specified by the m address to the card-buffer band. When all of the output words are in the buffer, synchronizing circuits store the indication that an 81 instruction has been given, and the instruction is then cleared from the static register.

Starting at 134 degrees of the mechanical card cycle caused by the previous 81 instruction, the synchronizing circuits set up the punch actuators with the output words stored in the buffer. Groups of ten bits are transferred serially from the card buffer to the shift register. Next, the ten bits are transferred in parallel to the information-distribution matrix, and then to the actuator matrix to set up the punches for the card (card B) moving into the punch station. During punch setup time, the other cards are also moving as shown in figure 3-2. The card that was punched (card C) is moving into read station 2, and the card that was sensed (card D) in read station 2 is on its way to the output stackers. At this point in the program a 57 instruction must be given if card D is to fall into stacker 1 instead of stacker 0.

The first mechanical card cycle ends as the cards come to rest in their respective stations. The synchronizing circuits complete punch setup and generate a signal that starts the next mechanical card cycle. A new card is fed, the cards in the read stations are sensed, and card B is punched.

Each successive 81 instruction, then, sets up punches for the card moving into the punch station and initiates a new mechanical card cycle. The 46 instruction transfers the information sensed during a card cycle from the buffer to main storage. The 57 instruction need only be given to divert a card into stacker 1.

General information necessary for an understanding of read-punch operations is discussed in sections 3-3 through 3-9.

3-3. IDENTIFYING CARD WORDS

Information read from or punched into cards by the read-punch unit is in the six-bit card code described in section 1-2 of the card reader manual. Since a card-buffer or main-storage location has a capacity of only four bits, a card-coded word is divided into primed and unprimed parts of four bits each, as described in section 3-3 of the card reader manual, and stored in two locations. Table 3-2 of the high-speed printer manual gives the complete code.

If an output word is in the four-bit processor code, a 17 instruction must be given to translate it into the six-bit card code before it is stored for punching. The word to be translated is sent to register A. The resulting six-bit word requires the use of two four-bit registers for storage. The unprimed part of the translated word is stored in register A, and the primed part is stored in register X. Refer to sections 3-14 and 3-29 of the processor manual for a description of these registers.

The primed and unprimed parts of each output word are sent from registers A and X to two locations of the main-storage band specified by the m address of the 81 instruction. Table 3-2 gives the assigned storage locations for both parts of the ten output words, designated O10, O'10 through O19, O'19. Note that the primed part is stored five locations after the unprimed part.

The input words designated I10, I'10 through I29, I'29 are transferred by a 46 instruction from the card-buffer band to the main-storage locations shown in table 3-5. The primed part is stored five locations after the unprimed part.

To enable the programmer to identify the primed or unprimed part of a word assigned to a given main-storage location, a card is divided into areas identified with a special notation. Figure 3-3 shows how each punched card is divided. The columns 1 through 45 for the upper field and 46 through 90 for the lower field are numbered individually. Each card is divided into ten groups numbered 0 through 9. Groups 4 and 9 each store a five-digit word in card code; each of the other groups stores a ten-digit word.

Each group is divided into two sections, one of which contains the unprimed and the other the primed parts of the digits in a word. The notation Ixx or Oxx which appears in each section of each group is the means of identification. The letter I signifies input words from the read stations, and the letter O output words to be punched. The letters I and O identify the unprimed parts; the letters I' and O', the

primed parts. The first numeral, either a 1 or a 2, identifies the read station in which the information was read. (For an output word, the first numeral is always 1.) The second numeral, which may have any value from 0 through 9, identifies one of the ten groups on a card. For example, I'18 is the primed parts of the ten input words of group 8 read from the card in read station 1, as shown in figure 3-3a. The comparable bits from the card in read station 2 are designated I'28, as shown in figure 3-3c. The primed parts of ten output words to be punched in the same location on a card is designated O'18, as shown in figure 3-3b.

3-4. CARD BUFFER

During input-output operations, information read from cards or information transferred from main storage to be punched is stored temporarily in the card-buffer band on the storage drum. After the information is recorded in the card buffer, it can be transferred to main storage or to the punch actuators within one drum revolution.

The card-buffer band consists of four tracks. It is served for reading and writing operations by two headbars, each consisting of four heads, one for each track. These headbars are referred to as head 1 and head 2. Head 1 and head 2 are displaced by 180 degrees.

Both the card reader and the read-punch unit use the card-buffer band for buffer storage. Although the card-buffer band is not part of the main storage, it contains 200 word locations just as do each of the 25 main-storage bands. Locations 100-199 of the band serve the read-punch unit; locations 000-099 serve the card reader. Only those operations concerning the read-punch half of the band are discussed in this manual.

Head 1 is used for reading and writing operations for both the card reader and the read-punch unit. Head 2 can be used to read information from either half of the card-buffer band but can be used for writing only in the card-reader half. The circuits are discussed in detail in section 3-24.

3-5. SENTINELS

Sentinels control the transfer of information between the read-punch unit and the card-buffer band, and between the card-buffer band and main storage. Refer to section 3-86 of the central processor manual for a complete description of a sentinel. Each sentinel consists of a timing signal from the cycling unit and one or more TS signals from one of the four tracks of the timing band, and is stored in one or more locations of the timing band. For example, the R6 sentinel is made up of the t5 signal from the cycling unit combined with the TS4 signal from the timing-band read circuit, and is stored in every fifth word location from 101, 106 through 196.

Table 3-1. Read-Punch Sentinels

Timing Signal	Timing-Band Signal			
	TS4	TS3	TS2	TS1
t11	Q4	Q5	Q6	
t10				C
t9			BT	
t8	X	PS		QW
t7	M3	M2	M1	
t5	R6	R5		TQ
t3		ST		
t2	G3*	G2*	G1*	

*Composite Sentinels:

P1 = M1 $\overline{M2}$ $\overline{M3}$ R1 = $\overline{G1}$ G2 $\overline{G3}$
P2 = $\overline{M1}$ M2 $\overline{M3}$ R2 = G1 $\overline{G2}$ $\overline{G3}$
P3 = M1 $\overline{M2}$ $\overline{M3}$ R3 = G1 $\overline{G2}$ G3
P4 = $\overline{M1}$ $\overline{M2}$ M3 R4 = $\overline{G1}$ $\overline{G2}$ $\overline{G3}$

Table 3-1 shows the sentinels used in transferring input information from the read stations to the card-buffer band and then to main storage, and output information from main storage to the buffer band and then to the punches. The interlace patterns, tables 3-2 through 3-5, show the timing-band locations of these sentinels.

Composite sentinels P1 through P4, and R1 through R4, combine several timing-band signals. For example, the R1 sentinel consists of three other sentinels: G1, G2, and G3. Sentinel G1 consists of the TS2 and t2 signals; sentinel $\overline{G1}$, therefore, consists of the $\overline{TS2}$ and t2 signal. Sentinel G2 consists of TS3 and t2; sentinel $\overline{G2}$ consists of $\overline{TS3}$ and t2. Sentinel G3 consists of TS4 and t2; sentinel $\overline{G3}$ consists of $\overline{TS4}$ and t2. A gate controlled by the R1 sentinel has the input signals $\overline{TS2}$, TS3, $\overline{TS4}$, and t2, as shown at gate 109, figure A-22.

3-6. CARD-INTERLACE PATTERN 3

Output words to be transferred from main storage to the card buffer are stored as shown in card-interlace pattern 3, table 3-2. (Card-interlace patterns 1 and 2 are used for the card reader.) The table shows the 200 locations of a main-storage band, the locations in which the parts of output words are stored, and the sentinels which control transfer of words from these locations. For example, 010, which is the unprimed part of the output word in group 0 (figure 3-3) is stored in location 108 of main storage. The primed part of the same group, 0'10, is recorded in location 113. The OW (output word) sentinels control the reading of 010 and the other output words from main storage by setting the read flip-flop.

The transfer into the buffer is initiated by the BT (begin transfer) sentinel in location 199 during the time the 81 instruction is staticized. The TO (transfer over) sentinel in location 199 indicates that the transfer of output words from main storage to the buffer is over and clears the 81 instruction from the static register.

3-7. CARD-INTERLACE PATTERN 4

The output words to be transferred from the card-buffer band to the punch actuators are recorded in the buffer band as shown in card-interlace pattern 4, table 3-3. The card-buffer locations in which the output words are recorded are identical to the main-storage locations from which the words were transferred. The P1, P2, P3, and P4 sentinels control reading of the output words from the buffer. The PS sentinel in location 104 controls punch setup. The TO sentinel in 199 indicates that the buffer is loaded with output words and that punch setup can begin. The Q4 and Q6 sentinels in location 049 end punch setup. The Q4 and Q5 sentinels in location 099, with the Q4 and Q6 sentinels in location 049, are used in marginal checking circuits. The Q5 and Q6 sentinels in location 149 control the setting of the column-drive-reset flip-flop. The X sentinel in location 050 steps the row counter.

3-8. CARD-INTERLACE PATTERN 5

Input words read in both read stations are recorded in the buffer band as shown in card-interlace pattern 5, table 3-4. The BT sentinel in location 199 begins the transfer by clearing intermediate storage to receive the row-by-row transfer from the sensing switches. The Q4 sentinel in location 099 controls the storing of one row of information into intermediate storage. (The other Q sentinels are not used in this transfer.) The ST sentinel in location 098 initiates the transfer of each row from intermediate storage to the buffer. The ST sentinel in location 198 ends the transfer of each row from intermediate storage to the buffer.

Table 3-2. Card-Interlace Pattern 3
(Main-Storage to Buffer-Band Transfer)

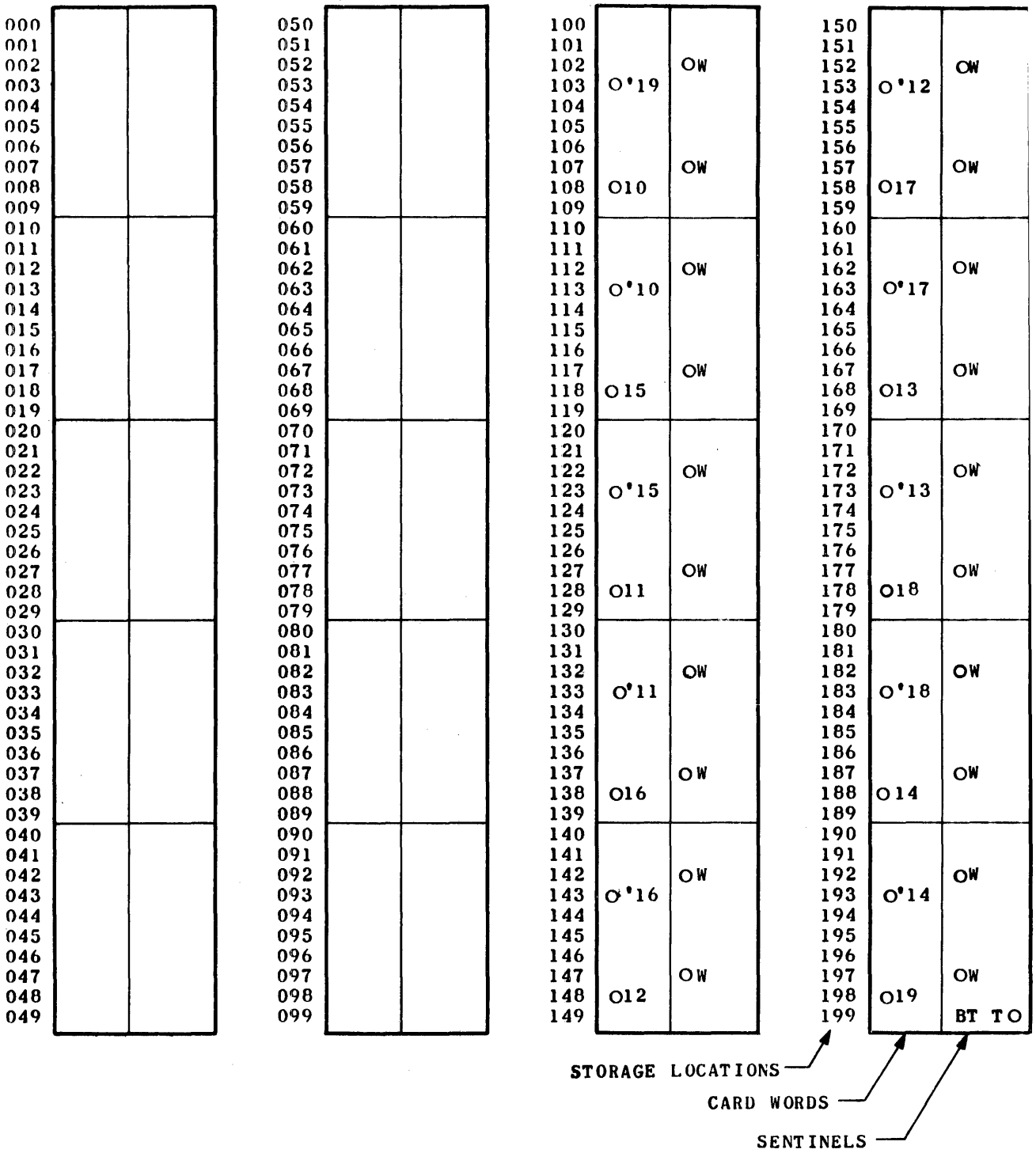


Table 3-3. Card-Interlace Pattern 4
(Buffer-Band to Punch Transfer)

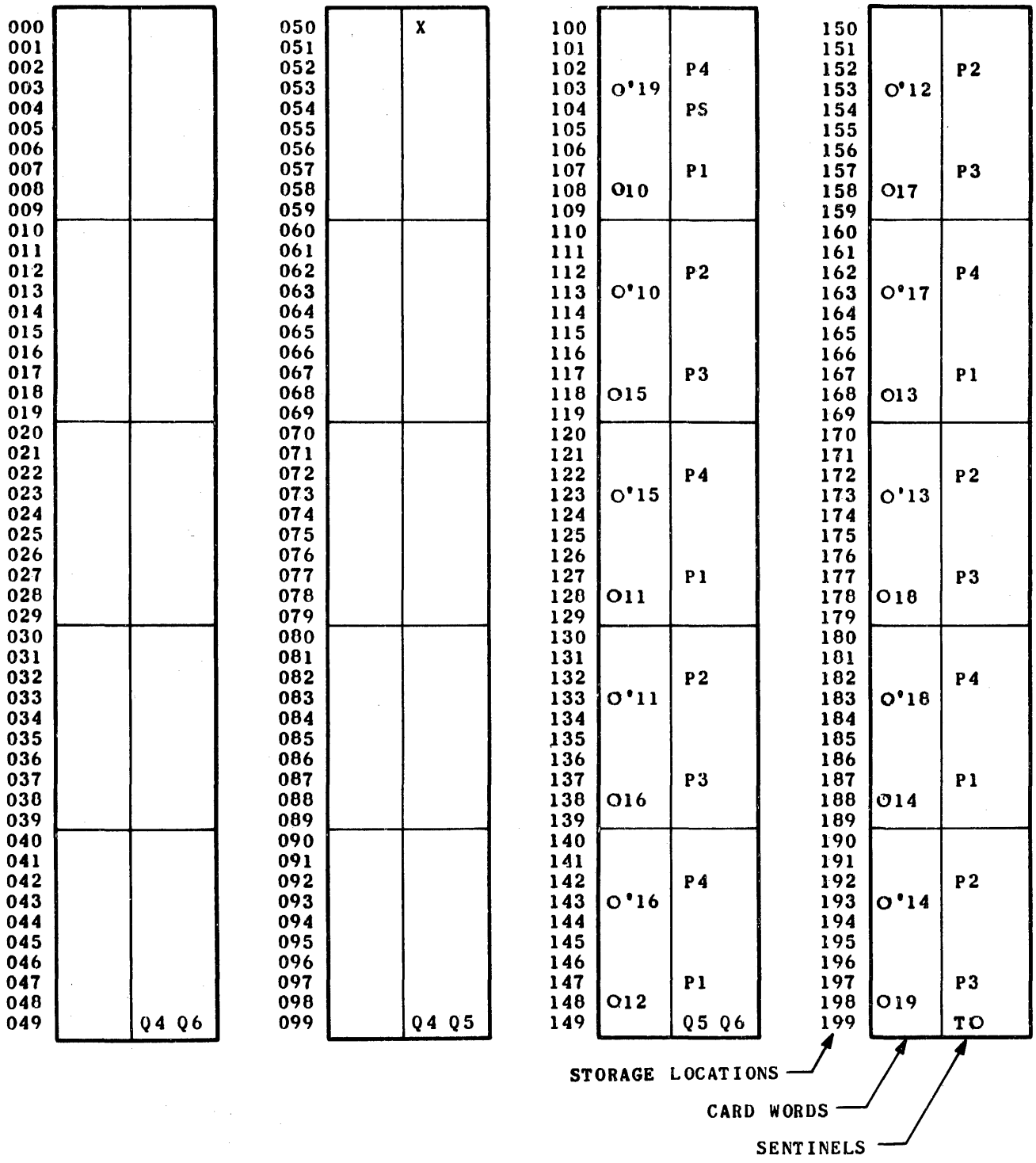


Table 3-4. Card-Interlace Pattern 5
(Read-Station to Buffer-Band Transfer)

000			050			100	I10	R1	150	I22	R1
001			051			101	I15	R3	151	I27	R3
002			052			102			152		
003			053			103			153		
004			054			104			154		
005			055			105	I'10	R2	155	I'22	R2
006			056			106	I'15	R4	156	I'27	R4
007			057			107			157		
008			058			108			158		
009			059			109			159		
010			060			110	I20	R1	160	I13	R1
011			061			111	I25	R3	161	I18	R3
012			062			112			162		
013			063			113			163		
014			064			114			164		
015			065			115	I'20	R2	165	I'13	R2
016			066			116	I'25	R4	166	I'18	R4
017			067			117			167		
018			060			118			168		
019			069			119			169		
020			070			120	I11	R1	170	I23	R1
021			071			121	I16	R3	171	I28	R3
022			072			122			172		
023			073			123			173		
024			074			124			174		
025			075			125	I'11	R2	175	I'23	R2
026			076			126	I'16	R4	176	I'28	R4
027			077			127			177		
028			078			128			178		
029			079			129			179		
030			080			130	I21	R1	180	I14	R1
031			081			131	I26	R3	181	I19	R3
032			082			132			182		
033			083			133			183		
034			084			134			184		
035			085			135	I'21	R2	185	I'14	R2
036			086			136	I'26	R4	186	I'19	R4
037			087			137			187		
038			088			138			188		
039			089			139			189		
040			090			140	I12	R1	190	I24	R1
041			091			141	I17	R3	191	I29	R3
042			092			142			192		
043			093			143			193		
044			094			144			194		
045			095			145	I'12	R2	195	I'24	R2
046			096			146	I'17	R4	196	I'29	R4
047			097			147			197		
048			098		ST	148			198		ST
049		Q4 Q6	099		Q4 Q5	149		Q5 Q6	199		BT

STORAGE LOCATIONS

CARD WORDS

SENTINELS

Table 3-5. Card-Interlace Pattern 6
(Buffer-Band to Main-Storage Transfer)

000			050			100		R5	150		R5
001		R6	051		R6	101	I10		151	I22	
002	I15		052	I27		102			152		
003			053			103			153		
004			054			104			154		
005			055			105		R5	155		R5
006		R6	056		R6	106	I'10		156	I'22	
007	I'15		057	I'27		107			157		
008			058			108			158		
009			059			109			159		
010			060			110		R5	160		R5
011		R6	061		R6	111	I20		161	I13	
012	I25		062	I18		112			162		
013			063			113			163		
014			064			114			164		
015			065			115		R5	165		R5
016		R6	066		R6	116	I'20		166	I'13	
017	I'25		067	I'18		117			167		
018			068			118			168		
019			069			119			169		
020			070			120		R5	170		R5
021		R6	071		R6	121	I11		171	I23	
022	I16		072	I28		122			172		
023			073			123			173		
024			074			124			174		
025			075			125		R5	175		R5
026		R6	076		R6	126	I'11		176	I'23	
027	I'16		077	I'28		127			177		
028			078			128			178		
029			079			129			179		
030			080			130		R5	180		R5
031		R6	081		R6	131	I21		181	I14	
032	I26		082	I19		132			182		
033			083			133			183		
034			084			134			184		
035			085			135		R5	185		R5
036		R6	086		R6	136	I'21		186	I'14	
037	I'26		087	I'19		137			187		
038			088			138			188		
039			089			139			189		
040			090			140		R5	190		R5
041		R6	091		R6	141	I12		191	I24	
042	I17		092	I29		142			192		
043			093			143			193		
044			094			144			194		
045			095			145		R5	195		R5
046		R6	096		R6	146	I'12		196	L'24	
047	I'17		097	I'29		147			197		
048			098			148			198		
049			099			149			199		BT TO

SENTINELS

CARD WORDS

STORAGE LOCATIONS

The R1 through R4 sentinels control the writing of input words into the buffer. The R1 sentinel controls the writing of unprimed words in rows 1 through 4 of both cards. The R2 sentinel controls the writing of primed words in rows 5 and 6, the R3 sentinel controls writing of the unprimed words in rows 7 through 10, and the R4 sentinel controls the writing of the primed words in rows 11 and 12.

3-9. CARD-INTERLACE PATTERN 6

Card-interlace pattern 6, table 3-5, shows the main-storage locations into which the 46 instruction transfers input words from the card buffer.

The R5 sentinel controls the transfer of input words from the buffer by head 1 into the second half (100-199) of the main-storage band. The R6 sentinel controls the transfer of input words from the buffer by head 2 into the first half (000-099) of the main-storage band. The BT sentinel in location 199 again initiates the transfer operation; the TO sentinel, in the same location, clears the 46 instruction from the static register.

3-10. MECHANICAL AND ELECTROMECHANICAL COMPONENTS

Various cams, rollers, levers, and other mechanical components transmit rotary motion from the read-punch unit motor to devices which move the cards from the input bin through the read and punch stations into one of the two output stackers. Cam-operated switches, relays, and mechanical linkages control the timing of the sensing and punching operations.

Both sensing operations are accomplished mechanically by pins which close switches corresponding to holes in the card. The card image is then electrically transmitted and stored. Electrical signals also determine which locations on the card are to be punched; the signals energize actuator magnets which lock specific punches into position. Punching is then performed mechanically. The INHIBIT PUNCH operation allows the operator to omit the punching function.

In the event of such conditions as jammed cards, full chip box, overheat, no air flow, or full output stackers, various abnormal-condition microswitches, thermostats, and other devices cause the unit to stop. The abnormal condition is indicated both on the read-punch panel (section 2-26) and on the processor panel.

3-11. MOTOR DRIVE, CLUTCH, AND BRAKE

The source of mechanical power in the read-punch unit is a constant-speed motor which operates continuously once power is supplied to it. The motor-shaft rotation is conveyed by a V-belt drive to the electromagnetic clutch-and-brake assembly, which is coupled directly to the drive shafts. The electromagnetic brake is energized when the electromagnetic clutch is disengaged. At other times the brake is deenergized.

Power for the read-punch unit is supplied from the a-c contactor in the processor to the MOTOR pushbutton on the read-punch control panel. Depressing the pushbutton operates switch 4, allowing current to flow through the coil of the main power relay and lighting the pushbutton. The contacts of the relay close the circuit to the motor; they also lock down the relay coil circuit so that the motor continues to operate after the pushbutton is released. Since the clutch and brake are normally deenergized, the main drive shafts of the unit do not rotate. None of the read-punch unit functions are performed until the clutch is engaged.

In order to make the following description of the clutch operation more meaningful, timing-cycle terminology is explained briefly here. The cycle is treated in detail in section 3-18.

A mechanical card cycle is defined as the sequence of operations which moves a card from a particular position in one of the stations in the read-punch unit and inserts the next card in the same position in that station. Four 360-degree cycles are necessary to move a card completely through the unit. At an operating speed of 150 cards per minute, each cycle requires 400 milliseconds; one degree of the cycle, therefore, corresponds to 1.11 millisecond.

The read-punch unit is stopped during the interval between 260 and 275 degrees of the cycle. During this interval, all cam switches are at rest and the clutch is disengaged, but the motor is running. In order to start the operations performed by the read-punch, the clutch must first be engaged, by operation of the FEED ONE CARD pushbutton on the control panel or by signals from the processor.

The feed-one-card circuit must be used for initial loading of cards. No card information is transferred to or from the processor when this single-cycle operation is employed.

Depressing the FEED ONE CARD pushbutton energizes the single-cycle relay, relay 3, shown in figure 3-4. Cam switch S7A provides a path to ground for the coil current of relay 3. Closing the contacts of relay 3 energizes relay 5 by completing its coil circuit to ground. Cam switch S7A is closed from 224 to 300 degrees, including stop time. Relays 3 and 5 remain energized from the time the pushbutton is depressed until S7A opens at 300 degrees.

Since the closed contacts of relay 3 provide a path to ground for the clutch-magnet-solenoid circuit, operation of the single-cycle relay engages the clutch. The clutch start cam switch (S8F) closes before the relay is deenergized at 300 degrees, and the clutch-magnet-solenoid circuit is not interrupted. The stop cam switch (S8G) opens the circuit at 214 degrees, disengaging the clutch. Thus, operation of the FEED ONE CARD pushbutton initiates a single mechanical cycle. The parallel start and stop cam switches overlap in their operation, so that independent timing adjustments can be made. If the potentiometer in the clutch-magnet-solenoid circuit is correctly set for a total current of 425 milliamperes through the two clutch-magnet solenoids, a 10-percent line-voltage fluctuation cannot exceed the power-supply rating of 500 milliamperes.

If a card jam occurs in the read-punch, the contacts of relay 1 open and the clutch cannot be engaged. Interlock switch S23A opens the clutch-magnet circuit as well.

Card cycling is program-controlled by an 81 instruction which generates a signal applied through synchronizing circuits to the coil of the card-cycle relay, relay 8. Relay 8 operates, providing a path to ground for the clutch-magnet-solenoid circuit. Clutch operation is thereafter identical with that described previously.

Since the clutch stop cam switch opens automatically after each card cycle, disengaging the clutch and stopping read-punch operation, a separate 81 instruction must initiate each card cycle.

Simultaneously with energizing the clutch, the transfer contact of relay 8 opens the brake-magnet-solenoid circuit so that the brake cannot be energized. The brake-release relay, relay 7, is energized, causing the capacitor in the brake-relay circuit to discharge. Relay 7, connected in parallel with the clutch-magnet solenoids, is energized at the same time. When the clutch is released, the brake-release relay deenergizes, causing the capacitor in the brake-relay (relay 6) circuit to charge. The charging current momentarily operates the brake relay, which closes the circuit of the brake-magnet solenoid.

The charging time of the capacitor is adjusted by the potentiometer in parallel with the brake-relay coil. When the adjustment is correct, the brake operates only from the time the clutch is disengaged until the unit stops. It is because of the slight uncertainty in the actual time of brake application that stop time is taken as the entire interval from 260 to 275 degrees of the card cycle.

3-12. PICKERKNIFE AND CARD CONVEYOR

The mechanisms shown in figure 3-5 transport a card from the input bin to the output stackers. When the clutch is engaged, the rotary motion of the motor shaft is transferred to the main drive shafts. Card feeding begins as the feed cam (3-5,1) on the front main drive shaft (2) commences to rotate.

The feed cam operates a cam-follower arm (3). The arm, held against the feed cam by a tension spring (4), translates the rotary motion of the cam to oscillatory motion. A link and arm transmit the motion to the feed arm (5); the feed link (6) further transmits it to the feed slide (7), which moves back and forth in a horizontal plane. Attached to the feed slide and projecting above it slightly less than the thickness of a single card is the pickerknife (8). On the forward excursion of the feed slide, the pickerknife pushes against the edge of the bottom card of the stack, carries it along, and then returns, riding under the bottom of the next card. When the pickerknife reaches the rear limit of its travel, the next card drops onto the card slide.

The pickerknife pushes the card through an aperture between the throat block (9) and throat knife (10) which is slightly wider than the thickness of a single card. Rotating feed rollers (11) grasp the card as it is pushed through the aperture, and the friction between the rollers and the card moves the card between a set of plates designated as read station 1. Intermediate rollers (12) ensure that the card moves with the correct speed and physical alignment. When a cam-operated card stop (13) halts the card, read operation takes place. The intermediate rollers continue to turn during the read operation to hold the card flush against the card stop.

After the card has been read, the card stop opens, and the intermediate rollers move the card into the punch-station feed rollers (14), which grasp the card and move it into the punching station. As in read station 1, a card stop (15) and intermediate rollers hold the card firmly in place during punching.

After the card has been punched, feed rollers, intermediate rollers, and a card stop similar to those used in the two previous card stations control the movement of the card into read station 2. After the card has been read for a second time, and the cam-operated card stop opens, the stacker feed rollers (16) move the card into the stacker.

The stacker feed rollers drop the card into either the front or the rear spring-loaded output stacker, according to the position of the sort fingers (17). If programmed signals from the processor raise the sort fingers, the card drops into the front output stacker, stacker 1; otherwise, the rear stacker, stacker 0, is selected.

When either output stacker is full, or when the last card has been fed from the input bin, the appropriate microswitch stops the read-punch unit, and indicates on the control panel which condition has occurred.

3-13. CARD SENSING

The sensing operation is identical in the two read stations. As shown in figure 3-6, when the card is in position in a read station and correctly held against the card stop by the intermediate feed rollers, a lower sensing-pin box moves up against the bottom of the card because of cam action. The sensing-pin box contains 540 spring-loaded pins, one for each hole position on the card.

As the box moves up, those pins which encounter a hole in the card pass through and those which do not are forced down by the card against the compression of the loading spring. The protruding pins of the sensing-pin box, corresponding to holes on the card, push up similar spring-loaded pins in the setup-pin box above the card. As a setup pin is forced up, it closes a sensing switch in the sensing-switch box above the setup-pin box. There are 540 sensing switches. Those sensing switches that close transfer the image of the card to the capacitor-storage circuitry, and the read-punch unit is ready to move on to the next cycle. If there is no card in the read station during sensing, a microswitch stops the unit and gives a control-panel indication.

3-14. CARD PUNCHING

While a card is moving from read station 1 to the punch station, the necessary punches for that card are set up. As described in section IV, electrical signals energize a set of actuator magnets. The actuators are arranged in a 540-magnet matrix, one magnet for each hole position on the card. The energized actuators (figure 3-7a) correspond to the positions which are to be punched.

As each actuator is energized, it pulls a spring-loaded armature against its pole faces to unlatch an interposer. The upper interposer shown in figure 3-7a is unlatched; the lower one is in the normal, latched position. The interposer is a spring-loaded lever with a cam-like arm projecting from its center. When it is unlatched, its spring tension causes it to rotate about its central pivot as far as a mechanical stop. The rotation places the central arm of the interposer under one end of a rocker arm to prevent the rocker arm from moving. A tower rod is connected to the other end of the rocker arm.

After all of the actuators which are to be energized have unlatched their interposers, cam action moves the set-bar assembly up against the tower-rod assembly, which contains spring-loaded vertical rods. The set-bar section contains spring-loaded set-bar pins.

As the set-bar section rises, the set-bar pins press up against the tower rods which, in turn, press against the rocker arms. If no unlatched interposer is blocking the other end of the rocker arm, the rising set-bar pin pushes the tower rod upward, pivoting the rocker arm. However, if the actuator has caused the interposer to unlatch, obstructing the motion of the rocker arm, neither the arm nor the tower rod moves. As the set-bar section continues to rise, the stationary tower rod presses against the set-bar pin, compressing its spring, and the set-bar pin projects below the set-bar section. A lock-slide assembly locks down each projecting set-bar pin. (As shown in figure 3-7b, the set-bar pins remain locked at all times except when the set-bar section is rising. When the set-bar section rises, mechanical linkages move the lock slide left, freeing the set-bar pins, which are relocked when the set-bar section reaches the high point of its travel.)

The set-bar section now moves down, and the set-bar pins which are locked down force the punches through the card into a die plate on the under side.

While the card is being punched, the interposer assemblies retract. A retract cam, mechanically connected to an interposer-restoring link, causes the link to pivot the interposer away from the rocker arm. The spring-loaded actuator armatures, which were released as the actuators deenergized, latch the interposers in their original positions.

As the set-bar section rises to its neutral position, the movable stripper plate pulls the punches from the dies and cards. Cam action then opens the card stop and the card moves on to read station 2.

3-15. INHIBIT PUNCH OPERATION

Card punching may be omitted by operating the INHIBIT PUNCH switch on the processor operator's panel. Closing this switch grounds one end of a cam-operated switch (S8B) in the read-punch unit. The other end of the skip cam switch is connected through the skip solenoid to 115 volts ac.

The skip cam switch operates just as the set-bar section begins to rise. If the INHIBIT PUNCH switch is closed, current through the skip solenoid causes its plunger arm to pull a skip interposer into the lock-slide assembly, preventing any motion of the slide. Because the slide is in the extended (unlocked) position when the set-bar assembly is moving up, the set-bar pins cannot lock. The skip cam switch does not open until after the punching operation. Hence the

punches are not forced down by locked set-bar pins and do not perforate the card.

3-16. STACKER SELECTION

When a programmed sort signal is received from the processor, the sort relay (relay 9) operates, provided sort cam switch S8D is closed (figure 3-8). Switch S8D is closed between 84 and 140 degrees of the card cycle, 140 degrees approximately corresponding to the time at which the card leaves the read station 2.

The contacts of relay 9 complete its coil circuit to ground so that the energized relay is independent of sort signals and S8D. The closed relay contacts also provide a path for current through the sort solenoid, provided sort pocket cam switch S7F is closed. Switch S7F is closed between 139 and 235 degrees of the card cycle, roughly the interval during which the card leaves read station 2 and comes to rest in an output stacker. When the sort solenoid operates, moving the sort fingers, mechanical linkages to a two-section microswitch (S20A, S20B) disconnect the coil circuit of relay 9, deenergizing it. Since the microswitch also closes the current path through the sort solenoid, its operation then depends only on cam switch S7F.

The sort-solenoid operating time is about 19.5 milliseconds, or 17.6 degrees of the card cycle. If the sort relay has operated by the correct time, 139 degrees, the sort solenoid actuates the mechanical linkage to the sort fingers at 156.6 degrees (139 + 17.6). By the time the card reaches the sort gate at 181.6 degrees, the mechanical linkage between the sort solenoid and the sort fingers has operated, and the card is deflected into output stacker 1.

Just as a separate 81 instruction is required to transport each card, a separate sort instruction is required to drop a given card into output stacker 1. The sorting operation is used, for example, to extract error cards. If a comparison of the data from read station 2 with the combination of the read-station 1 and punch-station data reveals an error, a sort signal may be generated to deflect the error card into output stacker 1. Timing is of extreme importance, however, as the sort relay must receive a signal between 84 and 140 degrees of the card cycle in order to operate the sort fingers.

3-17. ABNORMAL-OPERATION CIRCUITS

A number of abnormal-operation circuits, relays, and switches are contained in the read-punch unit. Figure 3-9 shows the indicator circuitry. Any abnormal condition sends a signal to the AOT (abnormal-operation) flip-flop in the processor to prevent the execution of further card-feed (81) instructions.

In the abnormal-operation circuits shown, the condition is first sensed by a microswitch. The microswitches either energize the abnormal-condition indicators directly, or, as in the case of the EMPTY READ STATION 1, EMPTY READ STATION 2, and MISFEED indicators, operate relays which energize the indicators. Any of three microswitches may energize the coil circuit of the card-jam relay. The relays must be reset either by the RESET button, for empty station, or the CARD JAM RESET button, for misfeed.

There are no fuses in the read-punch unit. All incoming power lines are fused in the processor.

3-18. CARD-CYCLE TIMING

This section presents a detailed description of the timing of the mechanical operations during the four 400-millisecond card cycles required to transport a card from the input magazine to the output stackers. Figure 3-10 relates the cycles to one another. Each card cycle begins at 275 degrees and continues through 260 degrees. The interval between 260 and 275 degrees, rather than a single point in time, is allowed for stop time, since the time at which the read-punch unit stops after the clutch is disengaged varies within these limits.

For use in the event of an abnormal stop, or during maintenance operations, timing dials graduated into 360 degrees, mounted on the rear of the main drive shaft, show the position of the read-punch unit in the card cycle.

3-19. CYCLE 1, ENTRY

During cycle 1, the card-entry cycle, the card is transported from the input bin to read station 1. A detailed timing breakdown follows.

Degrees	Mechanical Operation
275	Clutch is engaged by a Go signal from the synchronizing circuits or by operation of the FEED ONE CARD pushbutton.
279	Clutch start cam switch begins to close.
290	Start cam switch makes contact. Clutch remains energized until clutch stop cam switch opens at 214 degrees.
299	Start cam switch is fully closed.
311	Pickerknife begins to move in toward the edge of the bottom card in the input bin.
341	Pickerknife begins to push bottom card into feed rollers of read station 1.
17	Stop cam switch begins to close.
26	Stop cam switch makes contact.
37	Stop cam switch is fully closed.
102	Card enters feed rollers of read station 1.
106	Start cam switch begins to open.
112	Card stop of read station 1 begins to open.
116	Start cam switch breaks contact.
126	Start cam switch is fully open.
132	Pickerknife reaches limit of its travel and returns to pick next card.
133	Card stop of read station 1 is fully open. Card just sensed moves out of read station 1 to make room for card entering from feed rollers.
193	Card stop of read station 1 begins to close.
204	Stop cam switch begins to open.
211	Card stop of read station 1 is fully closed.
214	Stop cam switch breaks contact, and brake relay operates.
224	Stop cam switch is fully open. Entering card comes to rest against card stop of read station 1.
260-275	Stop.

3-20. CYCLE 2, SENSE

Timing of cycle 2, the data-sensing cycle, is shown below.

From 224 degrees of cycle 1 to 130 degrees of cycle 2, the card is held in place against the card stop in read station 1 by the moving intermediate feed rollers, which skid against the surface of the card.

The operation of clutch and clutch cam switches is identical with cycle 1.

Degrees	Mechanical Operation
275	Sensing-pin box begins to rise.
293	Sensing pins pass through holes in card and contact setup pins.
301	Setup pins are forced up and contact switch pins.
320	Sensing switches close.
334	Synchronizer transfers information from sensing switches to intermediate storage.
360	Sensing-pin box reaches top of its travel and begins to move down.
112	Card stop of read station 1 begins to open.
119	Punch-station card stop begins to open.
130	Intermediate feed rollers begin to move card out of read station 1.
133	Card stop of read station 1 is fully open.
141	Punch-station card stop is fully open. Card just punched moves out of punch station to make room for sensed card.
162	Sensed card enters punch-station feed rollers.
180	Sensing-pin box reaches low point and begins to move up.
193	Card stop of read station 1 begins to close.
209	Punch-station card stop begins to close.
210	Card leaves punch-station feed rollers.
211	Card stop of read station 1 is fully closed.
224	Punch-station card stop is fully closed.
255	Card comes to rest against punch-station card stop.
260-275	Stop.

3-21. CYCLE 3, PUNCH

Cycle 3, the punch cycle, begins with the card at rest in the punch station. Punch actuators are energized while the card is in transit from read station 1. The interposers operate between 254 degrees and stop.

The operation of clutch and clutch cam switches is identical with cycle 1.

Degrees	Mechanical Operation
275	Set-bar pins begin to unlock.
276	Skip cam switch begins to close.
282	Set-bar pins are unlocked.
287	Skip cam switch makes contact. If INHIBIT PUNCH switch has been operated, switch energizes skip relay.
291	Set-bar section begins to rise.
296	If operation of INHIBIT PUNCH switch has energized skip relay, relay is fully closed, and pins cannot lock.
300	Set-bar pins contact tower-rod assembly; rocker arms contact actuated interposers. Although the actuated interposers are in position at stop time of cycle 3, contact is delayed to allow for interposer bounce.
302	If INHIBIT PUNCH switch has been operated, lock slide is fully extended and latches into position.
313.5	If INHIBIT PUNCH switch has not been operated, lock slide begins to move in to lock set-bar pins.
331	Stripper plate begins to move down.
336	Set-bar section is fully up, and selected set-bar pins are projecting.
341	Projecting set-bar pins are locked by lock slide. Set-bar section begins to move down.
28	Interposer-restoring link begins to move up.
31	Stripper plate is at low point.
47	Card-jam switch tests for a jam.
52-60	Projecting set-bar pins force punches down through card and into die plate.
63	Skip cam switch begins to open.
76	Stripper plate begins to move up, pulling punches from die plate and card. Interposer-restoring link is fully up, and interposers are latched.

Degrees	Mechanical Operation
78	Skip cam switch breaks contact. If INHIBIT PUNCH switch has been operated, skip relay begins to open.
81	Set-bar section is at low point. Interposer-restoring link commences return to neutral position.
83	If INHIBIT PUNCH switch has been operated, skip relay is fully open.
86	Set-bar section begins to move up to neutral position.
112	Card stop of read station 2 begins to open.
119	Punch-station card stop begins to open.
129	Interposer-restoring link is fully retracted.
131.5	Intermediate rollers begin to move card out of punch station.
133	Card stop of read station 2 is fully open. Card just sensed moves out of read station 2 to make room for card just punched.
136	Stripper plate is fully up.
141	Punch-station card stop is fully open. Set-bar section is in neutral position.
163	Punched card enters feed rollers of read station 2.
193	Card stop of read station 2 begins to close.
195.7	Card leaves feed rollers of read station 2.
224	Card stop of read station 2 is fully closed. Card comes to rest against card stop of read station 2.
252	Lock slide begins to unlock set-bar pins.
260-275	Stop.

3-22. CYCLE 4, SENSE AND EJECT

The final cycle begins with the card at rest in read station 2. Since operation of the two read stations is identical, cycle 4 is identical with cycle 2 between 275 and 84 degrees. The following description concerns only the output operations from 84 degrees.

The operation of clutch and clutch cam switches is identical with cycle 1.

Degrees	Mechanical Operation
275-84	Identical with cycle 2.
84	Sort cam switch makes contact.*
128	Sort-pocket cam switch begins to close.
130	Card stop of read station 2 is fully open. Intermediate feed rollers begin to move card out of read station 2.
139	Sort-pocket cam switch makes contact. If a sort signal was received, the switch energizes sort solenoid.
140	Sort cam switch breaks contact.
148	Sort-pocket cam switch is fully closed.
151.6	Card enters stacker feed rollers.
156.6	Sort solenoid is energized and begins to move stacker sort fingers.
181.6	Card reaches sort fingers.
187.3	Card leaves stacker feed rollers.
217.3	If a sort signal was received, card is at rest in stacker 1.
225	Sort-pocket cam switch begins to open.
235	Sort-pocket cam switch breaks contact.
247.3	If no sort signal was received, card is at rest in stacker 0.
260-275	Stop.

*In order to select stacker 1, the read-punch unit must receive a sort signal before sort cam switch opens.

3-23. LOGICAL COMPONENTS

This section of the manual explains the logical components of the read-punch synchronizing circuits, most of which are located in the processor. The reader should be familiar with section II of the central processor manual, which explains the basic logical elements of the synchronizing circuits. The text of this section should be read with the appropriate logical drawings in Manual No. 2. A list of the logical drawings and the corresponding engineering drawings is given in the front of this manual.

3-24. CARD-BUFFER CIRCUITS

The read and write circuits of the card buffer are shown in figures A-22 and A-23. These circuits are identical in operation to the read and write circuits of main storage, described in sections 3-87 and 3-93 of the processor manual and shown in figures A-18 and A-19. Card-buffer band I (figure A-22) is composed of the circuits which control reading and writing with head 1. Card-buffer band II is composed of the circuits for head 2. These circuits are therefore referred to as head 1 and head 2.

The read-punch buffer circuits include the read and write circuits, the read and write flip-flops, the head-indicator flip-flop, and the read-stop flip-flop. With the exception of the read-stop flip-flop, all of these circuits are used by the card reader.

3-25. HEAD 1 CIRCUITS. The circuits which control the read and write operations of head 1 are shown in figure A-22. Head 1 is used to write into and read from either half of the card buffer. Certain of the input gates of the write and read flip-flops and the write input circuits operate when head 1 is over the card-reader half; others operate when it is over the read-punch half. To write with head 1 when it is over the read-punch half, the write flip-flop must be set, the write pedestal must be generated, and the write input gates must be alerted. The logical components associated with head 1 are as follows:

(1) READ-STOP FLIP-FLOP. It is possible to write output (O) words from main storage into the card-buffer band at the same time that input (I) words from intermediate storage are written. The read-stop flip-flop synchronizes these two operations.

Gate 105 sets the write flip-flop to write an O word; gate 102 restores the flip-flop after writing. Gates 106 through 109, with gates 900 through 903, set the write flip-flop to write an I word; gate 100 restores the flip-flop.

Each time the write flip-flop is set to write an 0 word, the read-stop flip-flop is set, generating a low RDSP signal that alerts restore gate 102 and a high $\overline{\text{RDSP}}$ signal that blocks restore gate 100. When the write flip-flop is set to write an I word, the read-stop flip-flop is restored and RDSP goes high, blocking restore gate 102.

(2) HEAD-INDICATOR FLIP-FLOP. The head-indicator flip-flop (figure A-22) controls the selection of a head to read from or write into the card-buffer band. Because the card reader and read-punch unit share the card-buffer band, the time required for reading is minimized by alternating control between heads 1 and 2. While one head is energized to read from the card-reader area (locations 000-099), the other head can be energized to read from the read-punch area (locations 100-199). Head 1 can write into either area, but head 2 can write only into the card-reader area.

The head-indicator flip-flop is controlled by gate 413, which samples the most significant digit of each timing-band address. (Refer to the central processor manual, sections 3-82, 3-84, and figure 3-3.) The TS1 signal at t2B- indicates the value of the digit. If the 100-199 half of the drum is under the timing-band read head, the most significant digit of the timing-band address is a 1, converted by the timing-band read circuits to a low TS1 signal. If the 000-099 half of the drum is under the timing-band read head, the most significant digit is a 0, which becomes a high TS1 signal when read in the timing-band read circuits.

When the card-reader half of the card-buffer band is under head 1, as shown in figure 3-2a of the card reader manual, the TS1 signal is high (0). The high TS1 signal blocks gate 413, restoring the head-indicator flip-flop and generating low H1 and high H2 signals. Successive TS1 signals keep the flip-flop restored for one-half drum revolution. At the end of this half of the drum revolution, the read-punch half of the card-buffer band is under head 1 as shown in figure 3-2b of the card reader manual. During the next half of the drum revolution, the TS1 signal at t2B is low (1) making gate 413 permissive at t2B-, setting the flip-flop. The head indicator flip-flop generates low H2 and high H1 signals for one-half drum revolution.

To summarize, the outputs of the head-indicator flip-flop indicate which half of the card-buffer band is under head 1. When the card-reader half of the card-buffer band (locations 000-099) is under head 1, the H1 signal is low; when the read-punch half of the card-buffer band (locations 100-199) is under head 1, the H2 signal is low.

In the head 1 circuits (figure A-22), the low H1 signal alerts gates which control reading from and writing into the card-reader buffer. The low H2 signal alerts gates which control the read-punch buffer read-write circuits. In the head 2 circuits (figure A-23), the low H1 signal alerts gates which control the read-punch buffer read circuits; the low H2 signal alerts gates which control the card-reader buffer read-write circuits.

(3) READ FLIP-FLOP. During punch setup, head 1 transfers output words from the buffer into the shift register. The head-1 read flip-flop is set at gate 306 by the set output of the read-out flip-flop, RO (figure A-22). The set output of the read flip-flop alerts the read circuits to the 40 bits of the unprimed output word or the 20 bits of the primed output word. The information read is transferred one track at a time into the shift register on the C lines. The read flip-flop is restored at gate 300 by the set output of the head-indicator flip-flop, H2, and the signal which indicates that the drum-revolution counter is on a count of one, FFP.

During a 46 instruction, head 1 transfers sensed information from locations 100-199 of the buffer to main-storage locations 100-199. The head-1 read flip-flop is set at gate 304 to alert the read-circuit output gates. Function signal 72 alerts the gate and the R5 sentinel which appears before each word, beginning with address 100, makes gate 304 permissive to set the read flip-flop 20 times (interlace pattern 6, table 3-5). The RSC5 output of the read flip-flop sets the main-storage write flip-flop to write the words head 1 is transferring from the buffer into the second half of the main-storage band. Gate 301 restores the flip-flop after each I word is read from the buffer. For the operation of the head-2 flip-flop during the transfer, refer to section 3-26.

(4) WRITE FLIP-FLOP. When sensed information is written into the read-punch half of the buffer, gates 900 through 903 and 106 through 109 control the write flip-flop.

Gates 900 through 903 control the flip-flop when the ETG signal is present, indicating that even groups (figure 3-11) from the card in read station 2 are written. When gate 900 operates, the write flip-flop is set to write the bits of the unprimed words from the upper field. The gate is made permissive by an R3 sentinel and the signals indicating rows 1 through 4, upper field. Gate 900 sets the write flip-flop 40 times (four rows times ten groups).

When gate 901 operates, the write flip-flop is set to write the bits of the upper-field primed words. The gate is made permissive by an R4 sentinel and the signal indicating rows 5 and 6, upper field. Gate 901 sets the flip-flop 20 times (two rows times ten groups).

Gate 902 sets the flip-flop 40 times to write the bits of the lower-field unprimed words. The gate is made permissive by an R1 sentinel and the signals indicating rows 1 through 4, lower field.

Gate 903 sets the flip-flop 20 times to write the bits of the lower-field primed words. The gate is made permissive by an R2 sentinel and the signals indicating rows 5 and 6, lower field.

Gates 106 through 109 control the write flip-flop when the OTG signal is present, indicating that odd groups from the card in read station 1 are written. Gate 109 sets the flip-flop 40 times to write the bits of the upper-field unprimed words. The gate is made permissive by an R1 sentinel and the signals indicating rows 1 through 4, upper field.

Gate 108 sets the flip-flop 20 times to write the bits of the upper-field primed words. The gate is made permissive by an R2 sentinel and the signals indicating rows 5 and 6, upper field.

Gate 107 sets the flip-flop 40 times to write the bits of the lower-field unprimed words. The gate is made permissive by an R3 sentinel and the signals indicating rows 1 through 4, lower field.

Gate 106 sets the flip-flop 20 times to write the bits of the lower-field primed words. The gate is made permissive by an R4 sentinel and the signals indicating rows 5 and 6, lower field.

All eight gates are alerted by the FFR2 signal. The flip-flop is set at t3B, at which time the p0 digit is on the SR2 line from the shift register. It is restored at gate 100, which operates at t1B, to generate a high SS*1 signal which steps the group counter. Note that RDSP is present at gate 100 from the restored read-stop flip-flop.

Each time the flip-flop is set, a signal is generated to shift the first bit out of the shift register onto the SR2 line. These signals, EF"1 through EF"4 and TEF1 through TEF4, also set the read-shift flip-flop. The set output shifts the remaining bits onto the SR2 line.

When punch information, read from the main-storage band by the 81 instruction, is written into the read-punch half, gate 105 controls the write flip-flop. This gate is made permissive by FS30 and the set output, RD, from the main-storage read flip-flop. The write flip-flop is restored at gate 102 which requires FS30 and an H2 signal from the head-indicator flip-flop. Note that the same signals which make set gate 105 permissive set the read-stop flip-flop to generate a low RDSP signal also required at restore gate 102.

(5) WRITE GATES. Sensed information enters the write circuits of head 1 at write input gates 200, 203, 206, and 209 on the SR2 line from the shift register. The coder input gates 240, 243, 245, and 248 must also be alerted to write the sensed information into the read-punch half.

Both a write input gate and a coder input gate are made permissive to write sensed information from a row into one track of the buffer. The other tracks are blocked from writing or are forced to write zeros. For example, if write input gate 209 and coder input gate 240 are both permissive, information is written into track 1. A 0 bit input on the SR2 line is high at gate 209; a 1 bit is low. If both gates are blocked, nothing is written into track 1.

Gates 206 and 243 are made permissive to write into track 2; gates 203 and 245 to write into track 3; and gates 200 and 248 for track 4.

All of the coder gates are made permissive by the following signals:

(a) the set output of the write flip-flop

(b) the FFR2 signal indicating that the read-punch circuits are in control of head 1

(c) row signals indicating the row being written.

A signal from the row counter is needed to alert both the coder input gate and the write input gate for a track. If this row signal is high, both gates are blocked and nothing is written into the track.

The least significant bits of the primed or of the unprimed words (00 0000) from either card field are sent on the SR2 line to gate 209 to be written into track 1. The second lowest order bits of the primed or of the unprimed words (00 0000) from either card field are sent to gate 206 to be written into track 2. The second highest order bits (00 0000) of the unprimed words from either card field are sent to gate 203 to be written into track 3. The most significant bits (00 0000) of the unprimed words from either card field are sent to gate 200 to be written into track 4.

When information is written into track 2, the high signal from gate 243 is sent to the write circuits of track 3 and track 4 to write zeros in these tracks. This provision for writing of zeros insures that the two most significant bits of all digits of the primed words are 0 bits.

Punch information enters the write circuits of head 1 at write input gates 211, 208, 205, and 202 on the M lines from main storage. The write input gates are made permissive by the set output of the write flip-flop and FS30. Coder input gate 242 is alerted to write punch information into the read-punch half. Gate 242 is made permissive by the set output of the write flip-flop, WO; FS30; the H2 signal; and the RDSP signal to control the writing of punch information on the M lines in parallel into the four buffer tracks.

3-26. HEAD-2 READ FLIP-FLOP. The write circuits of head 2 are not used in read-punch operations. The read flip-flop and the read circuits of head 2, shown in figure A-23, are used to read from the read-punch buffer. After the read-punch area of the buffer is loaded with sensed information, a 46 instruction is given to transfer the information from the buffer to main storage. Head 2 reads during the first half of the drum revolution needed to transfer the information. During the 46 instruction, gate 200 of the read flip-flop is alerted by FS72. The gate is made permissive by the H1 signal from the head-indicator flip-flop and the R6 sentinel, which appears on interlace pattern 6 (table 3-5) before each primed or unprimed word which is to be recorded in the first half (000-099) of the selected main-storage band. The read flip-flop is set 20 times at gate 200; each time it is set a word is read from the buffer and written into a specific location in the first half of the main-storage band. The output of the flip-flop alerts the read-out gates to information read from the buffer. The RSC2 signal alerts the main-storage write flip-flop which is set to write the information into locations 000-099 of the main-storage band.

3-27. READ-PUNCH CONTROL CIRCUITS

3-28. CARDS-TO-BUFFER TRANSFER CIRCUITS. The following logical components associated with the card-to-buffer transfer circuits are shown in figure A-26.

(1) READ-INITIAL-STORAGE FLIP-FLOP. The read-initial-storage flip-flop stores the F334^{0} signal from the timing cam until it is synchronized with a processor signal. The F334^{0} signal, which indicates that all the appropriate sensing switches in both read stations are closed, sets the read-initial-storage flip-flop at gate 13 (figure A-26). The flip-flop stores the signal until a low $\overline{EW}$ signal from the cycling unit makes gate 21 permissive (section 3-85, processor manual). The flip-flop is restored at gate 14 by the set output of the energize-capacitors flip-flop.

(2) READ-SYNCHRONIZING FLIP-FLOP. The read-synchronizing flip-flop ensures that the F334^{0} signal from the read-punch unit is synchronized with processor signals. When the low $\overline{EW}$

signal coincides with the low output signal of the read-initial-storage flip-flop, gate 21 is permissive, setting the read-synchronizing flip-flop, which remains set until all 12 rows have been sensed. The flip-flop is restored at gate 12 by signals which indicate the end of transfer of information from intermediate storage to the card buffer.

(3) CLEAR-CAPACITORS FLIP-FLOP. The clear-capacitors flip-flop controls the clearing of the 90-bit intermediate-storage circuit (figure A-27) before each row of card information is transferred from the sensing switches to the storage capacitors. The flip-flop is set at the beginning of each drum revolution in which a row of information is to be transferred. The BT sentinel (TS2 at t9B) in location 199, with the set output of the read-synchronizing flip-flop, sets the clear-capacitors flip-flop at gate 24. The output, the CLEAR CAP signal; clears the 90 storage capacitors so that a row of information can be stored. The flip-flop is set for one-quarter of a drum revolution and is restored at gate 25 by the set output of the energize-capacitors flip-flop.

(4) ENERGIZE-CAPACITORS FLIP-FLOP. The energize-capacitors flip-flop controls the storing of sensed information in intermediate storage. During every drum revolution in which a row of information is to be transferred from the sensing switches to intermediate storage, the Q4 sentinel in location 049, with the set output of the clear-capacitors flip-flop, sets the energize-capacitors flip-flop. When the energize-capacitors flip-flop is set, a low EC signal is generated at buffer 31. The EC signal goes to the row-combination gates (figure A-28) to initiate storage of information by generating the TR' signals. The TR' signals transfer information from 90 of the sensing switches into the 90 capacitors of intermediate storage. The shorten-capacitor-load-time flip-flop is also set each time the energize-capacitors flip-flop is set. The energize-capacitors flip-flop is set for one-quarter of a drum revolution and is restored at gate 29 by the output of buffer 37. If the maintenance switch to shorten capacitor load time is energized, the flip-flop is restored earlier.

(5) SHORTEN-CAPACITOR-LOAD-TIME FLIP-FLOP. The shorten-capacitor-load-time flip-flop is set each time the energize-capacitors flip-flop is set and remains set until the RPU control flip-flop is set. The set output alerts gate 83, which is made permissive when the next C sentinel (TS1 at t10B) occurs if the maintenance switch is energized to shorten load time of the intermediate-storage capacitors. The operation of gate 83 generates a signal to restore the energize-capacitors flip-flop earlier than usual, shortening the time to load intermediate storage with sensed information. The shorten-capacitor-load-time flip-flop is restored when the ST sentinel in 098 sets the RPU control flip-flop.

(6) RPU CONTROL FLIP-FLOP. The RPU (read-punch unit) control flip-flop differentiates between read-punch and card-reader operations which share the same circuits. The flip-flop is set when one row of information is to be transferred from intermediate storage to the read-punch half of the buffer, a transfer which requires one-half drum revolution. It is set by the JC1 signal from gate 35 (figure A-26), and remains set for the one-half drum revolution between the ST sentinels in locations 98 and 198 of the timing band. The set output, FFR2, alerts the write circuits of head 1 (figure A-22). Output FFR2 and the ST sentinel in location 198 restore the flip-flop at gate 32.

To set the flip-flop, gate 35 is made permissive by the ST sentinel in location 98 and the set output of the energize-capacitors flip-flop. When it is permissive, it generates a high JC1 signal which not only sets the flip-flop, but also jams the column-group counter to a count of one so that the column groups of the next row are correctly counted. The same signal clears the read-punch shift register between rows. Delayed one-half pulse time, the signal also restores the energize-capacitors flip-flop.

(7) BUFFER-LOADED FLIP-FLOP 2. Buffer-loaded flip-flop 2 (BL FF2) indicates to the static register whether all of the information read from cards has been transferred to the read-punch area of the buffer. The flip-flop is set at gate 12 by signals which indicate that the transfer is complete. (At the same time the signals at gate 12 also restore the read-synchronizing flip-flop.) The set output of BL FF2, a low BL2 signal, goes to static-register gate 107 (figure A-2). When the next 46 instruction is staticized, gate 107 operates to begin the unloading of the buffer into main storage.

Until the read-punch area of the buffer is fully loaded, BL FF2 is restored, generating a low $\overline{BL2}$ signal. When the next 22 (read-punch test) instruction in the program is staticized, FS26 alerts gate 16 of the ending-pulse buffer (figure A-2). If $\overline{BL2}$ is low, the ending-pulse buffer clears the static register and the next instruction is found in the c address. (See section 5-23 of the processor manual for a description of the 22 test instruction.)

During the second step of the 46 instruction, BL FF2 is restored at gate 17 by high FS46A. If the 46 instruction is not given at the correct time, BL FF2 is restored when the punch setup flip-flop is set.

(8) SAMPLE FLIP-FLOP 2. Sample flip-flop 2 controls the transfer of sensed information from intermediate storage to the read-punch shift register. The JC1 signal, which is present when a row of information is stored in the intermediate-storage capacitors, sets sample flip-flop 2 initially. Thereafter,

during the transfer of the row, the flip-flop is set ten times by the SC signal from the column-group counter (figure A-28), and restored by the t2B+ signal. The set output, a Sample Pulse 2 signal, with a TG signal from the group counter, controls the transfer. If the maintenance switch for shortening capacitor unload time is energized, the sample flip-flop 2 is restored at t11B instead of t2B.

3-29. BUFFER-TO-PUNCH TRANSFER CIRCUITS. The following logical components associated with the buffer-to-punch transfer circuits are shown in figure A-26.

(1) INTERLOCK FLIP-FLOP 3. Interlock flip-flop 3 stores the indication that an 81 instruction has been completed, all output words are stored in the buffer, and punch setup can begin. The TO sentinel in location 199, which clears the 81 instruction from the static register, and FS30 set interlock flip-flop 3 at gate 66. When the flip-flop is set, the high INT3 output blocks gate 109 of the static register (STR FF2) to prevent a subsequent 81 instruction from stepping to the second step until the punches are set up. The low set output of the interlock flip-flop alerts set gates 78 and 77 of the punch-setup flip-flop. If interlock flip-flop 3 is restored, a low INT3 output alerts gate 70 of the punch-final-storage flip-flop. (Gate 70 becomes permissive when it receives the 134° signal from the timing cam.) The interlock flip-flop remains set during the entire punch-setup time and is restored at gate 67 at the end of punch setup.

(2) PUNCH-FINAL-STORAGE FLIP-FLOP. The punch-final-storage flip-flop stores the 134° signal from the read-punch timing cam if it occurs before interlock flip-flop 3 is set. The punch-final-storage flip-flop is set initially by the GCA1+ signal at buffer 73 so that the first 81 instruction in the program can begin punch setup. Thereafter it is set by the 134° signal at gate 70. When the interlock flip-flop is set by the clearing of an 81 instruction from the static register, the set output of the interlock flip-flop sets the punch-setup flip-flop at gate 78. The punch-final-storage flip-flop is restored at gate 71 by the set output of the punch-setup flip-flop because the stored indication is no longer of use.

(3) GO FLIP-FLOP. The go flip-flop controls the mechanical card cycle of the read-punch unit. The flip-flop is initially restored at gate 75 by GCB+. The high CLSR signal, which indicates that punch setup has been completed, sets the flip-flop. The set output energizes relay 16, which deenergizes the brake and engages the clutch to begin the mechanical card cycle.

(4) PUNCH-SETUP FLIP-FLOP. The punch-setup flip-flop controls the setting up of the punches when the 81 instruction has been completed and the card to be punched is approaching

the punch station. The flip-flop is set at either gate 77 or gate 78,whichever is made permissive first. Gate 77 is alerted by the set output of interlock flip-flop 3 and is made permissive when the 134° signal is present. Gate 78 is alerted by the set output of the punch-final-storage flip-flop, which stores the 134° signal. The set output of the interlock flip-flop 3 makes gate 78 permissive.

The punch-setup flip-flop remains set until punch setup is completed, when it is restored by the End-Punch-Setup signal. The set output restores both buffer-loaded flip-flop 2 and the punch-final-storage flip-flop, and generates the EC signal at buffer 31. Either the CRD signal, generated when the flip-flop is set at gate 77, or the CRE signal, generated when it is set at gate 78, clears both the revolution counter and the row counter. The high CRC output jams the revolution counter to a count of two at buffer 47 and sets the row counter to a reading of one at buffers 212 and 112 (figure A-28). The low PSU signal alerts the input gates of the information-distribution matrix.

(5) READ-OUT FLIP-FLOP. The read-out flip-flop controls the transfer of output words from the read-punch area of the card buffer through the read-punch shift register to the information-distribution matrix. When the flip-flop is set, ten bits of a word are read out of the buffer into the shift register. The four input gates of the register are alerted by the FFP signal, which is generated only during the first drum revolution of punch setup for each row. Each P sentinel below makes its gate permissive only during the setup of punches for the rows listed:

Sentinel	Gate	Rows (Inclusive)	Words (Inclusive)
P1	62	1-4	010-014
P2	61	5-6	0°10-0°14
P3	60	7-10	015-019
P4	59	11-12	0°15-0°19

The low $\underline{RO}$ output signal sets the read flip-flop of card-buffer band I to read information from the buffer and alerts the punch-shift flip-flop to shift the information through the register. The high $\underline{RO}$ signal blocks the input gates of the information-distribution matrix during the shift.

(6) DRUM-REVOLUTION COUNTER. During punch setup, the revolution counter counts the three drum revolutions required to set up each row of punches. At the beginning of setup, the counter is cleared by either set output of the punch-setup flip-flop, CRD or CRE, and jammed to a reading of two by the

CRC signal from the same flip-flop. At the end of each drum revolution, the PS sentinel in location 104 steps the counter to the next reading, and generates a Quad+ signal which is sent to the every-other-word flip-flop (figure A-16). At the end of punch setup the CLSR signal clears the counter (figure A-26).

When the counter reads one, the JC2 output signal sets the group counter to one, and the FFP output signal alerts the set gates of the read-out flip-flop. The CTR-2 output signal, generated when the counter reads two, is used only during marginal checking. When the counter reads three, the CLC signal clears the group counter and the CTR-3 signal alerts the set gate of the column-drive-reset flip-flop, the stepping gate of the row counter, and the set gate of the end-punch-setup circuit (figure A-28).

(7) PUNCH-INITIAL-STORAGE FLIP-FLOP. The punch-initial-storage flip-flop (figure A-26) stores the F134° signal from the read-punch unit until it can be synchronized with processor timing. The F134° signal sets the flip-flop at gate 7. The delayed set output of the punch-synchronizing flip-flop restores it.

(8) PUNCH-SYNCHRONIZING FLIP-FLOP. The punch-synchronizing flip-flop synchronizes the F134° signal with processor timing. The set output of the punch-initial-storage flip-flop alerts gate 1, which is permissive when the EW signal from the every-other-word flip-flop is low. The 134° signal indicates that punch setup may begin.

(9) SELECT READ-PUNCH STACKER FLIP-FLOP. The select read-punch stacker flip-flop controls the stacker mechanism which causes a card to fall into stacker 1. A card automatically falls into stacker 0 unless a 57 instruction is given. When a 57 instruction is staticized, high FS25A sets the flip-flop at buffer 11 to operate relay 19. The relay operates the sort fingers to deflect the card into stacker 1.

3-30. READ-PUNCH COUNTERS

The read-punch counters are shown in figure A-28.

3-31. END-PUNCH-SETUP CIRCUIT. The end-punch-setup circuit controls the ending of punch setup. The X-sentinel-storage flip-flop stores the X sentinel from location 050 and alerts gate 102. Gate 102 is permissive when all of the following signals are present: the Q4 and Q6 sentinels, indicating that all 12 rows of punches have been set up, signal CTR-3, indicating that the revolution counter is on a count of three, and signals TR1 and UF', indicating that the row counter is on a count of one. The permissive gate generates high CLSR and End-Punch-Setup signals. The CLSR signal clears the drum revolution counter and sets the go flip-flop to begin the

mechanical card cycle. The End-Punch-Setup signal restores both the punch-setup flip-flop and interlock flip-flop 3.

3-32. ROW COUNTER. The row counter, with the RPU field flip-flop, counts the row-by-row setup of punches during punch setup and the transfer of each row of information from the sensing switches to intermediate storage during read operations. The row counter consists of six flip-flops, the outputs of which indicate rows 1 through 6 of the two card fields. (The field flip-flop indicates which of the two fields is being read, enabling the circuit to count rows 1 through 12 on a card.) A counter circuit similar to the row counter is described in section 2-34 of the central processor manual.

At the beginning of punch setup, the row counter is cleared by either the CRE or the CRD output of the punch-setup flip-flop at buffer 107. It is initially set to a reading of one by the CRC signal at buffer 212. Thereafter, all stepping signals step the counter from one through six and back again to a reading of one, since the output of the sixth flip-flop alerts the set gate of the first flip-flop. During punch setup the row counter is stepped at the end of every third drum revolution by the X sentinel and CTR-3 signal at gate 104. These signals indicate that one row of punches has been set up. The STRC signal, generated as the row counter is stepped, restores the column-drive-reset flip-flop.

At the beginning of the read operation, the row counter is initially set to a reading of one by the JTR signal at buffer 212. It is stepped at gate 105 by the high SS'1 output of the restored head-1 write flip-flop and a TG10 signal which indicates a reading of ten in the column-group counter. The reading often indicates the completion of the transfer of one row. The TR outputs of the row counter are sampled by the row-combination gates. The R" signals go to the row-indicator circuits. The SCI+ signal at gate 105, which is normally low, is effective only during keyboard-input operations.

RPU FIELD FLIP-FLOP. The RPU field flip-flop operates in conjunction with the row counter to indicate which field of the card is being read or set up. During punch setup, the field flip-flop is initially restored at buffer 112 by the CRC output of the punch-setup flip-flop. A low UF' signal is generated to indicate that the upper-field punches are being set up. The CRC signal that restores the flip-flop also sets the row counter initially to a reading of one (TR1 low). Stepping signals step the row counter through readings of one through six. Signal TR6, which indicates that the counter is reading six, and the stepping signal which steps the counter back to one, generate a high signal from gate 210 which sets the field flip-flop at buffers 114 and 115. The set output is a low LF' signal. The counter is stepped again through a count of six to indicate that the lower-field punches are being set up. The

next time the counter reads six, a stepping signal, together with the TR6 and LF' signals at gate 111 restore the flip-flop to generate a low UF' signal. The UFA set output is generated for marginal checking operations.

The row counter is again used during the sensing of the card which follows. Because the field flip-flop remains restored (UF' low) at the end of punch setup, no initial restoring is required. The row counter and field flip-flop operate in the same way during sensing as during punch setup.

3-33. COLUMN-GROUP COUNTER. The column-group counter counts the groups of ten bits which make up one row. During a read operation, the counter counts ten groups, five from the two cards being read. During punch setup, however, the counter is only required to count five groups because only one card is punched.

During punch setup, the counter (figure A-28) is cleared by the CLC signal at buffer 109, and set to a reading of one by the JC2 signal at buffer 312. Every time the punch-shift flip-flop (figure A-27) is set to shift a group of ten bits into the shift register, an SGC signal (step-group-counter) is generated to step the counter to the next reading at buffers 108 and 109. When the last group of a row is set up, the counter, which started on a count of one, has been stepped through a count of 6. Because the counter is stepped in advance, the TG2 controls the first group instead of the TG1 output.

When cards are being read, the column-group counter is jammed to a reading of one at buffer 312 by the JC1 signal, which is generated when the RPU control flip-flop is set. The SS'1 signal, which is generated each time the head-1 write flip-flop is restored, steps the counter at buffers 108 and 109. At the end of the transfer of ten groups (one row), the counter reads ten and the next SS'1 signal operates gate 310 to reset the counter to one for the next row. Each time the counter is stepped, an SC signal is generated at gate 110 and sent to sample flip-flop 2 (figure A-26). The sample flip-flop generates a Sample-Pulse-2 signal which transfers one group from intermediate storage into the shift register.

During a read operation, the TG1 through TG10 outputs of the column-group counter transfer a group of ten bits in parallel from intermediate storage to the shift register. During punch setup, the TG2 through TG6 signals transfer the bits in parallel from the shift register to the information-distribution matrix. The TG1A through TG10A outputs of the counter go to the group indicators.

The SCISA, SCISB, CLIA, SCI2 and WRA signals, which are normally low, are only effective during keyboard input operation.

3-34. GROUP INDICATORS. The odd-group and even-group indicators (figure A-28) sample the TG1A through TG10A outputs of the column-group counter to determine whether the group being transferred from intermediate storage to the shift register is an odd group from the card in read station 1, or an even group from the card in read station 2 (section 3-39). The indication that the group is an even group, signal ETG, goes to gate 229 of the read-shift flip-flop (figure A-27) to produce the initial shift required for even groups (section 3-40). The ETG or OTG signal alerts a set-gate of the head-1 write flip-flop so that the groups are written into the buffer in the correct order (figure 3-16).

3-35. ROW-COMBINATION GATES. The row-combination gates combine the row-counter signals, TR1 through TR6, with the field flip-flop outputs, LF' and UF', into TR'1 through TR'12 signals. These signals control the transfer of information from the sensing switches to intermediate storage during reading. They also control the transfer of information from the information-distribution matrix to the punch-actuator matrix during punch setup. The EC (energize capacitors) signal generated during reading alerts the row-combination gates to indicate that the capacitors are ready to receive information from the sensing switches. The EC signal is also generated during punch setup by the setting of the punch-setup flip-flop.

3-36. ROW INDICATORS. The row indicators, buffers 116 through 119, convert the R" signals from the row counter into signals which control the writing of information into the card buffer. The R'1-4 signal and the R'5,6 signal control set-gates of the head-1 and head-2 write flip-flops. The R'1,5 signal and the R'2,6 signal control the write input gates of both heads as described in section 3-24.

3-37. SHIFT-REGISTER CIRCUITS

The following paragraphs discuss the circuits shown in figure A-27.

3-38. SENSING-SWITCH MATRIX. The cards in the two read stations are block sensed simultaneously. The information is stored temporarily in the sensing-switch matrix. Ninety bits at a time, one row of information from each card, is transferred from the switches into intermediate storage by the TR"1 through TR"12 signals. The TR"1 signal transfers information sensed from row 1 of the card in read station 1 and from row 7 of the card in read station 2. The remaining TR" signals transfer the rows from the upper field of the first card with rows

from the lower field of the second card, followed by rows from the lower field of the first card with rows from the upper field of the second card (figure 3-11).

3-39. INTERMEDIATE STORAGE. The 90 intermediate storage capacitors are divided into five odd and five even groups. As shown in figure 3-11, the first transfer to intermediate storage consists of five odd groups sensed from row 1 of the card in read station 1 and five even groups sensed from row 7 of the card in read station 2. Groups I14 and I29 consist of only five bits; each of the others contains ten bits.

The ten bits of each group in intermediate storage are transferred in parallel into the shift register, starting with the first odd group. After the odd group is shifted out of the shift register, an even group of ten bits is transferred into the shift register.

One of the odd groups of bits in intermediate storage is shown in figure 3-12, with each bit identified by the position of the digit of which it is a part, from p1 (LSD) through p10 (MSD). The p10 bit of an odd group goes to FF10 of the shift register, p9 goes to FF9, and so on; that is, the bits of an odd group are transferred to the shift register in the order in which they are to be shifted out on the SR2 line.

The bits of an even group in intermediate storage, however, are not transferred to the shift register in the order in which they are shifted out. As shown in figure 3-13, the p10 digit of the even group goes to FF1 of the shift register, p9 goes to FF10, and so on. An initial shift pulse is required to shift all ten bits one flip-flop to the right before they are shifted out on the SR2 line. (Refer to section 3-40.)

When a card is read in the first read station, the bits are sent to the shift register as odd groups. When the same card is read again in the second read station, the bits are sent as even groups. Sending the same bit over two different paths provides a check on the paths from intermediate storage.

Each group of ten bits is gated out of intermediate storage by a low Sample-Pulse 2 signal and one of the signals TG1 through TG10 from the column-group counter. All ten groups of one row are sent to the shift register and written into the card buffer in one-half drum revolution.

3-40. SHIFT REGISTER. The shift register operates during either a read or a punch operation.

During a read operation, the shift register receives bits from intermediate storage in parallel and transfers them serially to the read-punch area of the card buffer. After the ten input bits of each group (five input bits per group in words I14, I19, I24, and I29) are sent to the ten flip-flops of the

register, they are shifted out one at a time into the buffer write circuits. Section 2-35 of the central processor manual describes a shift register.

The shift register is initially cleared at buffer 212 by the high JC1 signal which indicates that a row (90 bits) is stored in intermediate storage. If the bits transferred from intermediate storage make up an odd group, they are transferred in the order in which they are to be shifted out and no initial shift is necessary. If the bits transferred make up an even group, however, an initial shift is necessary before the contents of the shift register can be written into the buffer. Initial shift takes place when the ETG signal at gate 229 from the even-group indicator (figure A-28) indicates that the column-group counter is on an even count. The R1 sentinel and FFR2 signal normally alert the gate, which operates only when ETG is also present. The high output of gate 229 goes to buffers 212 and 213 to shift the bits as shown in figure 3-13. After the shift, the even group is transferred on the SR2 line to the buffer write circuits.

(1) READ-SHIFT FLIP-FLOP. When the head-1 write flip-flop of the card buffer is set, any one of the signals EF"1 through EF"4 or TEF1 through TEF4 is generated according to which set gate of the flip-flop operates. The signal is sent to buffer 209 to set the read-shift flip-flop, which provides shift pulses. The set output, a low $\overline{\text{TOS2}}$ signal, alerts the write input gates of the card-buffer circuits to indicate that information is being shifted out of the register.

During punch setup, information bits to be punched are read into the shift register serially from the card buffer on the C lines at gates 224 through 227. Only one of these gates is permissive during the setting up of punches for one row. Each input bit must be shifted through the register until it is full. The punch-shift flip-flop controls shifting through the register. The punch-delay flip-flop controls transfer from the shift register to the information-distribution matrix. Information is transferred from the information-distribution gates to the actuator matrix under control of the TR'1 through TR'12 signals from the row-combination gates (figure A-27).

(1) PUNCH-SHIFT FLIP-FLOP. The punch-shift flip-flop is set at gate 215 by the $\overline{\text{RO}}$ signal from the read-out flip-flop (figure A-26). The $\overline{\text{RO}}$ signal controls the transfer of information from the read-punch area of the card buffer. The SGC signal clears the shift register in preparation for reading in ten bits on one of the C lines. The SGC signal at buffers 212 and 213 shift the bits through the shift register. At the same time, the high $\overline{\text{RO}}$ signal blocks the input gates of the information-distribution matrix until the shift register is full.

(2) PUNCH-DELAY FLIP-FLOP. After the shift register is full, the $\overline{RO}$ signal goes low but the punch-delay flip-flop is set to block the input gates of the information-distribution matrix for one more word time. The punch-delay flip-flop is set at gate 200 by the low set output of the punch-shift flip-flop at t2B. The set output of the punch-delay flip-flop blocks gates 204 through 208 until the flip-flop is restored by a high t2B+ signal. The restore output makes the input gates of the information-distribution matrix permissive.

3-41. KEYBOARD-INPUT FLIP-FLOP. The keyboard-input flip-flop controls the read-punch shift register when it is used during manual input operation. The operation of the flip-flop is discussed in section 4-51, processor manual. Note that the SCI1, CLIA, WRA, and SCISA signals are not effective during normal read-punch operations.

3-42. COLUMN-DRIVE-RESET FLIP-FLOP. The column-drive-reset flip-flop clears the column-drive circuits of the punch actuators after each row of information has been transferred into the punch actuators. The flip-flop is set at gate 325 during the third drum revolution of punch setup for each row by the CTR-3 signal from the drum-revolution counter and the Q5 and Q6 sentinels in location 149. As a result the column-drive circuits (section 4-11) are cleared by the Column-Drive-Reset signal. Set gates 383 and 384 are alerted only if the maintenance switch that resets the column drivers early has been energized. The CRC signal initially sets the flip-flop. The flip-flop is restored by the high STRC signal generated each time the row counter is stepped.

3-43. NORMAL OPERATIONS

Normal operation of the read-punch unit is controlled by three instructions: 81, 46, and 57. The functions of these instructions are briefly discussed in section 3-1, and a detailed analysis of their operation is presented in the following sections.

3-44. 81 INSTRUCTION

The 81 instruction consists of two steps: W21 and W22. In the W21 step, a search is made for the main-storage band which contains the output words to be punched. The search operation is discussed in detail in sections 4-3 and 4-11 of the central processor manual. In the W22 step, the output words are read from the main-storage band and written into the read-punch buffer. The two steps are described in detail below.

3-45. W21 STEP. The p7 and p8 digit positions of the m address of the 81 instruction contain the number of the main-storage band in which the output words are stored. Since head selection is unnecessary during the search for the band, only the band-selection circuits are involved. The staticized 81 instruction generates FS28A which generates function signals 1, 58+, 63, 30+, and 29. Function signal 30+ insures that only the band is searched for by restoring the TS FF at gate 100 (figure A-12), and keeps the band selected by inhibiting restore gates 62 and 63 of the band-selection flip-flops (figure A-18). If the storage band selected is one of the fast-access bands, only the 00 head is used to read from the band. Function signal 30+ keeps quadrant-selection flip-flops 1 and 2 restored at gates 34 and 38 (figure A-18).

Function signal 29 alerts step gate 109 of the static register (figure A-2) to advance to the second step, W22. The gate is made permissive by the BT sentinel in location 199 of card-interlace pattern 3, table 3-2, and a low $\overline{\text{INT3}}$ signal which indicates that the punches are completely set up as a result of the previous 81 instruction. Setting the STR2 flip-flop changes the reading in the static register from 81 to 83. Function signal 29 also alerts gate 101 of the input-output abnormal-condition flip-flop in the processor (section 3-53).

3-46. W22 STEP. The W22 step generates FS30A which generates function signals 58+, 30+, 30 and 93. Function signals 30+ and 58+ keep the main-storage band selected. Function signal 30 alerts the set gate of the main-storage read flip-flop, and the head-1 card-buffer circuits. (Head 2 cannot be used to write into the read-punch half of the buffer.) Function signal 93 alerts the ending-pulse gate to clear the 81 instruction from the static register.

The reading of the output words from the main-storage band is controlled by the OW sentinels which appear before each part of the ten output words shown in interlace pattern 3, table 3-2. The first OW sentinel, in location 102, sets the main-storage read flip-flop as shown in figure 3-14. The set output of the read flip-flop, a low RD signal, sets the write flip-flop of head 1. (The same signals also set the read-stop flip-flop as described in section 3-25.) The set output of the write flip-flop alerts the head-1 write input gates and gate 242 to the two bits of the $\underline{0}$'19 word, the first word of the transfer, on the M1 and M2 $\overline{\text{lines}}$ and the zeros on the M3 and M4 lines. The write pedestal is generated at gate 402 by FS30 and a low H2 signal to inhibit the read circuits of head 1. The two bits of each digit of the $\underline{0}$'19 word are written by head 1 into buffer tracks 1 and 2 of location 103. Zeros are written into tracks 3 and 4. After the $\underline{0}$'19 word is completely recorded, the write flip-flop is restored and the main-storage read flip-flop is restored after one word time. Each

succeeding OW sentinel sets the main-storage read flip-flop, and the remaining $\underline{0}$ and $\underline{0}'$ words are written into the buffer in the same manner. Unprimed words are written into all four tracks of the buffer; primed words are written into tracks 1 and 2, with zeros in the remaining two tracks.

The last word to be written is the $\underline{0}19$ word, which is written into location 198 of the buffer. The $\underline{T0}$ (transfer over) sentinel in location 199 and FS93 operate ending-pulse gate 13 of the static register to clear the 81 instruction from the static register and generate a high RCT3 signal. The RCT3 signal restores the band-selection flip-flops at buffer 64 (figure A-18) and the conditional-transfer flip-flop at buffer 77 (figure A-12) so that the next search is for the c address of the 81 instruction.

The $\underline{T0}$ sentinel sets interlock flip-flop 3, which stores the indication that an 81 instruction has been completed and that the buffer contains all of the output information to be punched.

3-47. PUNCH SETUP. Punch setup in accordance with the output information stored in the buffer is controlled by the synchronizing circuits. Punch setup begins when the F134° signal from the timing cam is present at the set input of the punch-setup flip-flop, as shown in figure 3-15. After interlock flip-flop 3 is set by the 81 instruction, the synchronizing circuits assume control of the processing of each card.

The set output of interlock flip-flop 3 alerts the set gates of the punch-setup flip-flop, which initiates punch setup. If the interlock flip-flop is set before 134 degrees of the mechanical card cycle, the punch-setup flip-flop is set by the 134° signal at gate 77 (figure A-26). If the interlock flip-flop is set after 134 degrees, the punch-setup flip-flop is set at gate 78, alerted by the set output of the punch-setup flip-flop. In the latter case, the punch-final-storage flip-flop stores the 134° signal until the 81 instruction sets the interlock-3 flip-flop.

The setup of each row of punches takes place during three drum revolutions. As a result, approximately 36 drum revolutions are required to set up the 12 rows of the card to be punched. During the first of the three drum revolutions for each row, information is read from the buffer and the punches are set up. The bits of an output word are read ten at a time serially from one track of the card buffer into the read-punch shift register. These ten bits are then transferred in parallel into the information-distribution matrix and then into the punch-actuator matrix.

Row 2 of the card to be punched is set up first, followed by rows 3 through 12. Row 1 is the last row to be set up. A preliminary drum revolution is required before row 2 is set up, and a final revolution is required to end punch setup.

(1) PRELIMINARY DRUM REVOLUTION. The preliminary drum revolution prepares the synchronizing circuits for punch setup. Either a high CRD or a high CRE signal, generated at the time the punch-setup flip-flop is set, clears both the drum-revolution counter and the row counter. It also generates a high CRC signal, which sets the drum-revolution counter to a reading of two and the row counter to a reading of one. Signals restore the buffer-loaded 2 flip-flop and the punch-final-storage flip-flop. The set output of the punch setup flip-flop generates a low EC signal which alerts the row-combination gates.

The PS sentinel in location 104 steps the revolution counter to a reading of three (CTR-3), and generates a high CLC signal which clears the column-group counter. None of the P1 through P4 sentinels is effective on this revolution. The Q5 and Q6 sentinels in location 149 set the column-drive-reset flip-flop. At the end of the preliminary drum revolution the revolution counter reads three, the row counter reads one, and the group counter reads zero.

(2) SETUP OF ROW TWO. The first sentinel to be used during the setup of row 2 is the X sentinel, which sets the X-sentinel storage flip-flop and steps the row counter to a reading of two. The PS sentinel steps the revolution counter to a reading of one, and a high JC2 signal sets the group counter to a reading of one.

The P1 sentinel and the FFP output of the revolution counter set the read-out flip-flop. The set output of the read-out flip-flop sets the read flip-flop of head 1, which is over the read-punch buffer, and the punch-shift flip-flop. The set output of the punch-shift flip-flop clears the shift register and steps the group counter to two. All 40 bits of the $\underline{Q}10$ word are read from the card buffer into the shift-register input gates. Only the ten bits from track 2, at gate 226, enter the shift register because only this gate is alerted by the R'2,6 signal from the row-indicator circuit. Next, the set output of the punch-shift flip-flop shifts the ten bits into the register. The high $\underline{RQ}$ signal from the read-out flip-flop blocks all gates to the information-distribution matrix while the bits are being shifted into the register.

When the ten bits are completely stored in the register, the read flip-flop of the card buffer, the read-out flip-flop, and the punch-shift flip-flop are all restored. Restoring the read-out flip-flop removes the $\underline{RQ}$ inhibition from the gates of the information-distribution matrix, but these gates are

inhibited for one more word time by the set output of the punch-delay flip-flop. When the punch-delay flip-flop is restored, the ten bits are gated into the information-distribution matrix under control of the low TG2 signal from the group counter. The TG2 signal gates group 1 (columns 1 through 10). The TR'2 output of the row counter gates the bits into the actuator matrix to set up the punch-actuators with the first ten bits of row two.

The P1 sentinels set the read-out flip-flop as they occur, in locations 127, 147, 167, and 187. The bits of the 011, 012, 013, and 014 words are read from track 2 of the buffer and sent to the punch-actuator matrix in the same manner as were the bits of the 010 word. At the end of the first revolution, after the bits of the final word, 014, have been set up, the row counter reads one and the group counter reads six.

During the second drum revolution, the PS sentinel steps the drum-revolution counter to two. During the third drum revolution, the PS sentinel steps the revolution counter to three and the CLC signal clears the group counter to zero. The CTR-3 signal and the Q5 and Q6 sentinels in location 149 set the column-drive-reset flip-flop.

(3) SETUP OF ROW THREE. During the first drum revolution of punch setup for row 3, the X sentinel, with the revolution-counter reading of three, steps the row counter to three. The STRC signal restores the column-drive-reset flip-flop, the PS sentinel steps the revolution counter to one, and the JC2 signal sets the group counter to one. The P1 sentinel sets the read-out flip-flop to initiate the reading of ten more bits of the 010 through 014 words from track 3 of the buffer. The operations performed during the second and third drum revolutions of row-3 setup are identical to those of row-2 setup.

(4) SUBSEQUENT ROWS. The remaining rows of the card are set up in the same manner as rows 2 and 3, except that different P sentinels set the read-out flip-flop and different input gates to the shift register operate, as shown in table 3-6.

(5) END OF PUNCH SETUP. At the end of the third drum revolution of punch setup for the last row transferred (row 1) the revolution counter reads three, the group counter reads zero, and the row counter reads one. As shown in figure 3-15, the Q4 and Q6 sentinels cause the end-punch-setup circuit to generate a high CLSR signal and a high End-Punch-Setup signal. The CLSR signal restores the revolution counter and sets the go flip-flop. The output of the go flip-flop sends a signal to a relay that begins the mechanical card cycle. The End-Punch-Setup signal restores the punch setup flip-flop and interlock flip-flop 3.

Table 3-6. Shift-Register Gates Alerted During Punch Setup

Row	Output Words	Sentinel	Line	Gate
4	010-014	P1	C4	224
5	0'10-0'14	P2	C1	227
6	0'10-0'14	P2	C2	226
7	015-019	P3	C1	227
8	015-019	P3	C2	226
9	015-019	P3	C3	225
10	015-019	P3	C4	224
11	0'15-0'19	P4	C1	227
12	0'15-0'19	P4	C2	226
1	010-014	P1	C1	227

3-48. TRANSFER OF SENSED INFORMATION TO BUFFER. During the mechanical card cycle initiated by the set output of the go flip-flop, a new card is fed, both cards in the read stations are sensed, and the card in the punch station is punched with the information set up in the punch actuators. After the information is block-sensed from the cards and stored in the sensing-switch matrix, the F334° signal from the timing cam indicates that all sensing switches have been closed and the information is ready to be transferred into the buffer. Ninety bits are transferred in parallel into intermediate storage. Groups of ten bits are then transferred in parallel into the shift register, shifted serially out of the register, and written into one track of the buffer. The transfer of 90 bits requires a full drum revolution. During the first quarter of this revolution, the intermediate-storage capacitors are cleared. During the second quarter the capacitors are energized, and during the last half the 90 bits are transferred from intermediate storage through the shift register, and written into the buffer.

As shown in figure 3-16, the F334° signal from the timing cam is stored in the read-initial-storage flip-flop and is synchronized into processor timing by the read-synchronizing flip-flop. The JTR signal from the read-synchronizing flip-flop sets the row counter to one. The BT sentinel sets the clear-capacitors flip-flop to clear intermediate storage in preparation for the transfer of 45 bits from row 1 of the card in read-station 1 and 45 bits from row 7 of the card in read-station 2 (figure 3-11). The Q4 sentinel in location 049 sets the energize-capacitors flip-flop to transfer this information

into intermediate storage. The EC signal alerts the row-combination gates to generate a TR'1 signal to gate 90 bits from the sensing-switch matrix. Setting the energize-capacitors flip-flop restores both the clear-capacitors flip-flop and the read-initial-storage flip-flop; only the read-synchronizing flip-flop remains set.

The ST sentinel in location 098 sets the RPU control flip-flop, which remains set while information is written into the buffer. The JC1 signal jams the group counter to a count of one and sets sample flip-flop 2 so that ten bits from the I10 word are gated from intermediate storage into the shift register.

The information in the register must be shifted out onto the SR2 line and written into one track of the card buffer in location 100. The R1 sentinel sets the head-1 write flip-flop at gate 109. (Head 2 is not used to write into the read-punch buffer.) The write pedestal is generated at gate 400 (figure A-22) by the FFR2 signal from the set RPU control flip-flop. The EF"1 signal from the write flip-flop shifts the first bit out of the shift register onto the SR2 line and sets the read-shift flip-flop. The TOS2 signal from the read-shift flip-flop alerts the four write input gates 209, 206, 203, and 200 to the bits on the SR2 line. The ten bits enter the write circuits of track 1 at gate 209 because this gate is made permissive by the R'1,5 signal indicating row 1. Gate 240 operates to write the bits of the I10 word entering gate 209. After all ten bits have been shifted out onto the SR2 line, both the read-shift flip-flop and the head-1 write flip-flop are restored. The SS'1 signal from the write flip-flop steps the group counter to a count of two. The SC signal, generated by the stepping of the group counter, sets sample flip-flop 2 for the second time, gating ten bits of the I25 word from intermediate storage into the shift register. Because the I25 word is from the card in read-station 2, it is an even group, as shown in figure 3-11. Figure 3-13 shows the shift required for an even group after it is transferred to the shift register. The R1 sentinel provides this right shift.

The R3 sentinel sets the write flip-flop of head 1 at gate 900 to write the ten bits of I25 word into track 1. The TEF1 signal from the write flip-flop shifts the first bit out of the shift register onto the SR2 line and sets the read-shift flip-flop. The ten bits of the I25 word enter the write input circuits on the SR2 line and are written into track 1.

The R1 and R3 sentinels alternately control the writing of ten bits of the I11, I26, I27, I13, I28, I14, and I29 words from row 1 of the card in read-station 1 and row 7 of the card in read station 2 into track 1 of the buffer, in the locations shown in interlace pattern 5, table 3-4. The group counter is

stepped to the next reading each time the restoring of the write flip-flop generates an SS*1 signal. The ten bits of the I29 word are the last to be written into the buffer. The SS*1 signal, combined with the reading of ten in the group counter, sets the group counter to 1 and steps the row counter to 2. The ST sentinel restores the RPU control flip-flop to complete the transfer of the first 90 bits into the buffer.

The remaining rows of both cards are transferred in the same manner. The transfer of each row takes place during one complete drum revolution. The R1, R2, R3, and R4 sentinels control the write circuits during the transfer of the remaining rows into the card buffer.

After the twelfth row has been written into the buffer, the row counter is stepped to a count of 1, and the ST sentinel restores the RPU control flip-flop. The ST sentinel also restores the read-synchronizing flip-flop and sets the buffer-loaded flip-flop to indicate that the buffer is completely loaded with sensed information.

3-49. 46 INSTRUCTION

The function of the 46 instruction is to transfer input information from the buffer to the main-storage band specified in the p7 and p8 positions of the m address. During the transfer, first head 2 transfers the input words to be stored in the first half of the band; then head 1 transfers the input word to be stored in the second half. The transfer requires one complete drum revolution. After the 46 instruction is staticized, the two steps shown in figure 3-17 are required for the transfer. These steps are designated W11 and W12.

3-50. W11 STEP. During the W11 step, a search similar to a normal m-address search is made for the band specified in the m address. The staticized 46 instruction generates function signal 45A which generates function signals 1, 58+, 63, 30+, and 70. The search for the main-storage band, which is identical to that of the 81 instruction (section 3-44), is controlled by function signals 1, 58+, 63, and 30+. Function signal 70 alerts gate 107 of static-register flip-flop 2 (figure A-2). The gate is made permissive by the BT sentinel in location 199 and the low BL2 signal from buffer-loaded flip-flop 2, which indicates that the buffer is loaded. Step gate 107 sets static-register flip-flop 2, initiating the W12 step.

3-51. W12 STEP. During the W12 step, the input words are transferred from the card buffer through the M buffers to the selected band. When the transfer is completed, the 46 instruction is cleared from the static register. Function signal 46A restores buffer-loaded flip-flop 2 as soon as transfer begins.

The transfer takes place in one complete drum revolution. During the first half of the revolution, head-2 circuits read from the buffer; during the second half, the head-1 circuits read. As shown in figure 3-17, the head-2 read flip-flop is set by the R6 sentinels and FS72 during the first half of the revolution. Interlace pattern 6, table 3-5, shows the input words which are read during the first half, under control of the R6 sentinel.

The head-2 read flip-flop is set for the first time by the R6 sentinel in location 001. The set output of the read flip-flop, signal BLRE2, alerts the read circuits to the I15 word from the buffer, the first word transferred. The RSC2 signal sets the main-storage write flip-flop (figure A-19). The 40 bits of the I15 word are read by head 2 and transferred on the $\overline{0}$C lines to the M buffers (figure A-6). Function signal 72 alerts M-buffer input gates 101, 105, 108, and 111 to the I15 word on the $\overline{0}$C lines. The word is transferred on the M lines to the main-storage write circuits. The set output of the main-storage write flip-flop alerts the write input gates to the I15 word. The word is then written into location 002 of the selected band.

During the remainder of the first half of the drum revolution, the rest of the R6 sentinels control the writing of the remaining I and I' words into locations 000-099 of the selected band (table 3-5). At the beginning of the second half of the drum revolution, the head-indicator flip-flop is set (the H2 signal is low) and head 1 reads the remaining input words from the buffer. The R5 sentinel in location 100 sets the head-1 read flip-flop to alert the head-1 read circuits. The I10 word in location 101 is transferred from the read-punch buffer to the M buffers on the C lines. Function signal 72 alerts M-buffer input gates 100, 104, 107, and 110 to the I10 word on the C lines. The word is transferred on the M lines to the main-storage write circuits. The main-storage write flip-flop is set by FS72 and the set output of the read flip-flop, RSC5, at gate 101 (figure A-19). The set output of the main-storage write flip-flop alerts the write input gates to the I10 word, which is written into location 101 of the selected band. During the remainder of the second half of the drum revolution, the rest of the R5 sentinels control the transfer of the remaining I and I' words into locations 100 to 199 of the selected band (table 3-5).

The T$\overline{0}$ sentinel in location 199 and FS93 operate gate 13 of the ending-pulse circuit (figure A-2) to clear the 46 instruction from the static register. A high RCT3 signal is also generated to restore the conditional-transfer flip-flop at buffer 77 (figure A-12) so that the next search is for the c address.

3-52. 57 INSTRUCTION

The 57 instruction operates the sort fingers to divert one card into stacker 1 instead of stacker 0. Then the stacker mechanism returns to its normal condition, diverting all cards into stacker 0. A 57 instruction must therefore be given for each card to be diverted into stacker 1.

The staticized 57 instruction generates function signals 25A and 67. Function signal 25A sets the select read-punch stacker flip-flop (figure A-26) at buffer 11. The set output of the flip-flop operates the sort fingers. Function signal 67 alerts ending-pulse gate 17 to clear the instruction from the static register.

3-53. ABNORMAL OPERATIONS

All abnormal conditions in the read-punch unit are controlled by the RPU abnormal-operation flip-flop. The flip-flop sends indications of such conditions to the input-output (I-O) abnormal-condition flip-flop in the processor. This section describes the RPU abnormal-operation flip-flop (AOT FF) and the conditions which influence it.

3-54. ABNORMAL-OPERATION FLIP-FLOP

The abnormal-operation flip-flop (figure A-26) is alerted if one or more of the following conditions generates a high input to buffer 40:

1. No card in read station 1
2. No card in read station 2
3. Input bin empty (EMPTY MAG)
4. One or both stackers full (FULL RECEIVER 1, 0)
5. Chip box full
6. Card jam
7. Read-punch unit power off (TOWER POWER OFF)
8. Processor stopped by operator (STOP SWITCH)
9. Processor stopped on first step of an 81 instruction because the operator has pushed the ONE CARD R.P.U. button on the processor operator's panel (TECC).

The input signal is shown in parenthesis.

A low output from buffer 40, indicating the presence of one or more of these abnormal conditions, with a low SAO (set-abnormal-operation) signal makes gate 41 permissive, setting the AOT FF. The SAO signal (figure A-5) is low either when FS1A is high, indicating that the processor is on search, or when SPA is high, indicating that the processor is stopped and the stop flip-flop is set.

The set outputs of the AOT FF are the low AOT signal and the signals from the RPU-off-normal relay which light the SYSTEM OFF NORMAL lamp on the read-punch control panel and the READ PUNCH OFF NORMAL lamp on the processor operator's panel.

The low AOT signal alerts gate 101 of the I-O abnormal-condition flip-flop in the processor (figure A-2). Under normal conditions, FS29 makes only gate 109 of static-register flip-flop 2 permissive at t9B of the first step of the 81 instruction. When an abnormal condition is present (AOT signal present), FS29 also makes gate 101 permissive at t9B to set the I-O abnormal-condition flip-flop and generate high Jam I2A and Jam I2B signals. These signals nullify the effect of gate 109 by jamming the reading for the second step of a test instruction into the static register. The second step of the 81 instruction is not executed. The Jam I2A and Jam I2B signals transfer the 81 instruction from register C to register A, and cause a search for the c + 1 address instead of the c address. (Refer to section 4-41 of the central processor manual.)

After the condition which caused the AOT FF to be set is corrected, the operator must push the CLEAR button on the read-punch panel to erase all indications of the abnormal condition before starting computation.

The nine abnormal conditions are described more fully below.

3-55. EMPTY READ STATION

A microswitch below each read station tests for the presence of cards during sensing. If the station is empty, the switch opens, generating a signal which sets the AOT FF and lights either the EMPTY READ STATION 1 or the EMPTY READ STATION 2 lamp on the read-punch control panel. The operation of these switches can be inhibited by the EMPTY STATION INHIBIT switch on the processor operator's panel.

3-56. EMPTY INPUT BIN

The empty-magazine switch under the input bin is normally closed by the presence of cards. After the last card is fed from the bin, the switch opens, generating a signal which sets the AOT FF and lights the EMPTY INPUT MAGAZINE lamp on the read-punch control panel. The operation of this switch can be inhibited by the EMPTY STATION INHIBIT switch on the processor operator's panel.

3-57. FULL STACKER

The full-output-bin microswitch under each of the output stackers is normally open. When either stacker is full, the switch closes, generating a signal which sets the AOT FF and lights the OUTPUT BIN FULL lamp on the read-punch control panel.

3-58. FULL CHIP BOX

A microswitch mounted below the chip box operates when the box is filled with punch chips, setting the AOT FF and lighting the CHIP BOX FULL lamp on the read-punch control panel.

3-59. CARD JAM

Three card-jam switches are located along the card path. If a card moves out of its normal path, or overlaps another card, one of the switches is energized, setting the AOT FF and lighting the MISFEED lamp on the read-punch control panel.

3-60. READ-PUNCH UNIT POWER OFF

If the drive motor is turned off, a switch is energized to set the AOT FF.

3-61. STOP SWITCH

If the operator has depressed one of the STOP buttons on any of the panels, a stop switch signal is generated, setting the AOT FF and lighting the STOP lamp on all panels.

3-62. ONE CARD RPU

When the ONE CARD R.P.U. button on the processor operator's panel is pushed, a TECC signal is generated to set the AOT FF. The computer stops on the first step of the next 81 instruction (section 4-44, central processor manual).

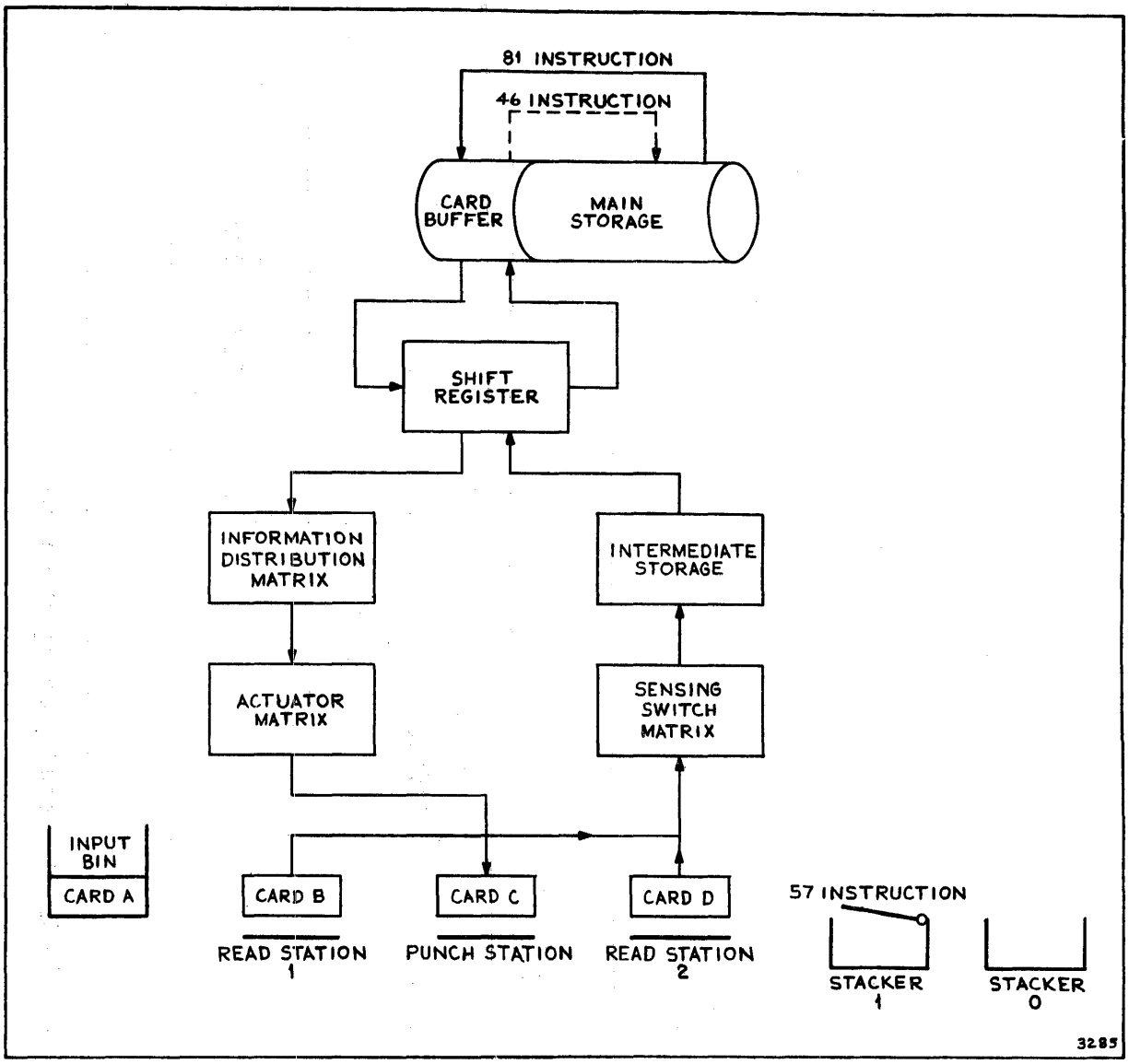


Figure 3-1. Information Path

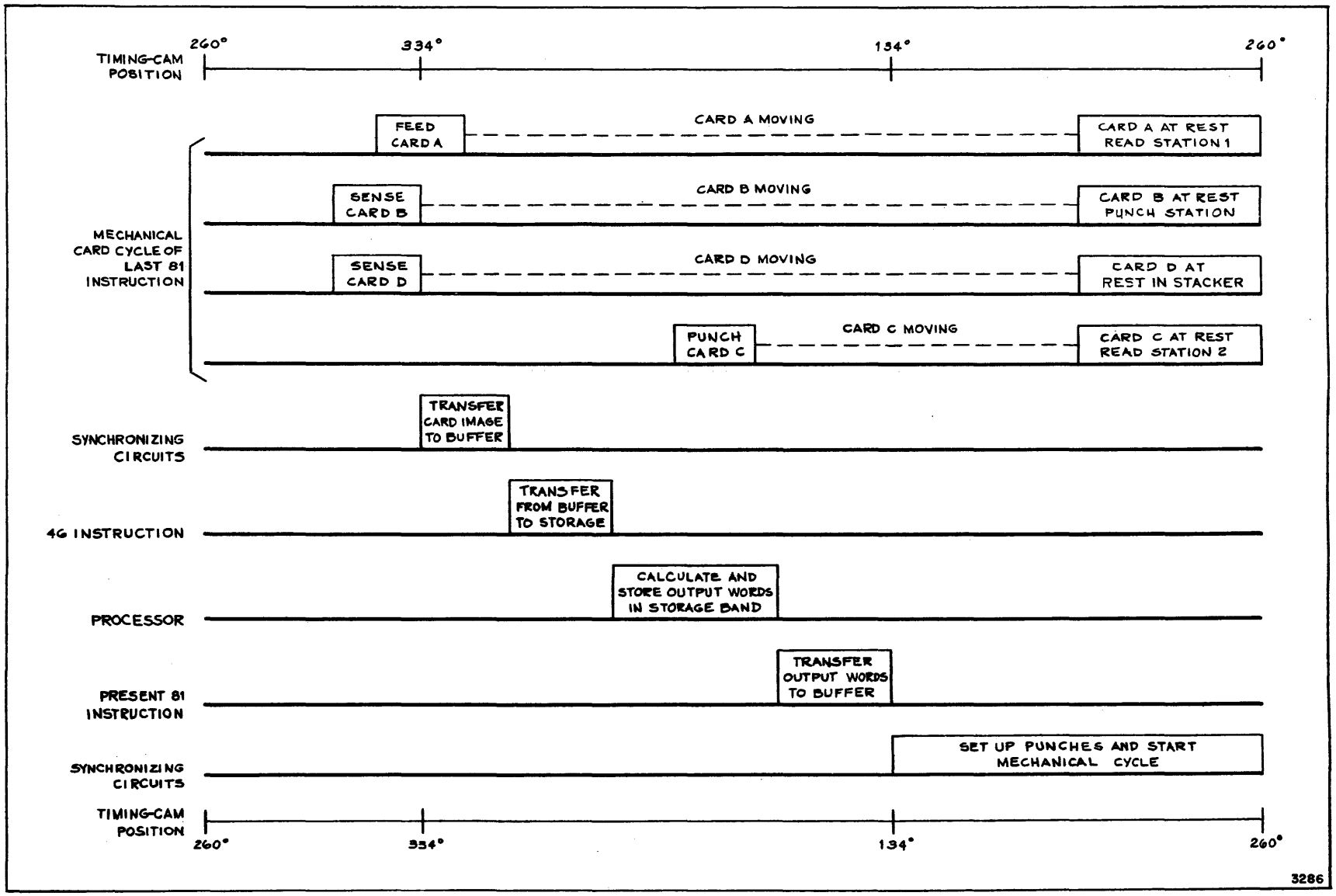


Figure 3-2. General Timing Diagram

a. INPUT FROM READ 1

GROUP 0	GROUP 1	GROUP 2	GROUP 3	GROUP 4
I_{10}	I_{11}	I_{12}	I_{13}	I_{14}
I'_{10} 1 2 3 4 5 6 7 8 9 10	I'_{11} 11 12 13 14 15 16 17 18 19 20	I'_{12} 21 22 23 24 25 26 27 28 29 30	I'_{13} 31 32 33 34 35 36 37 38 39 40	I'_{14} 41 42 43 44 45
GROUP 5	GROUP 6	GROUP 7	GROUP 8	GROUP 9
I_{15}	I_{16}	I_{17}	I_{18}	I_{19}
I'_{15} 46 47 48 49 50 51 52 53 54 55	I'_{16} 56 57 58 59 60 61 62 63 64 65	I'_{17} 66 67 68 69 70 71 72 73 74 75	I'_{18} 76 77 78 79 80 81 82 83 84 85	I'_{19} 86 87 88 89 90

b. OUTPUT FOR PUNCHING

GROUP 0	GROUP 1	GROUP 2	GROUP 3	GROUP 4
O_{10}	O_{11}	O_{12}	O_{13}	O_{14}
O'_{10} 1 2 3 4 5 6 7 8 9 10	O'_{11} 11 12 13 14 15 16 17 18 19 20	O'_{12} 21 22 23 24 25 26 27 28 29 30	O'_{13} 31 32 33 34 35 36 37 38 39 40	O'_{14} 41 42 43 44 45
GROUP 5	GROUP 6	GROUP 7	GROUP 8	GROUP 9
O_{15}	O_{16}	O_{17}	O_{18}	O_{19}
O'_{15} 46 47 48 49 50 51 52 53 54 55	O'_{16} 56 57 58 59 60 61 62 63 64 65	O'_{17} 66 67 68 69 70 71 72 73 74 75	O'_{18} 76 77 78 79 80 81 82 83 84 85	O'_{19} 86 87 88 89 90

c. INPUT FROM READ 2

GROUP 0	GROUP 1	GROUP 2	GROUP 3	GROUP 4
I_{20}	I_{21}	I_{22}	I_{23}	I_{24}
I'_{20} 1 2 3 4 5 6 7 8 9 10	I'_{21} 11 12 13 14 15 16 17 18 19 20	I'_{22} 21 22 23 24 25 26 27 28 29 30	I'_{23} 31 32 33 34 35 36 37 38 39 40	I'_{24} 41 42 43 44 45
GROUP 5	GROUP 6	GROUP 7	GROUP 8	GROUP 9
I_{25}	I_{26}	I_{27}	I_{28}	I_{29}
I'_{25} 46 47 48 49 50 51 52 53 54 55	I'_{26} 56 57 58 59 60 61 62 63 64 65	I'_{27} 66 67 68 69 70 71 72 73 74 75	I'_{28} 76 77 78 79 80 81 82 83 84 85	I'_{29} 86 87 88 89 90

3220

Figure 3-3. Input and Output Card Words

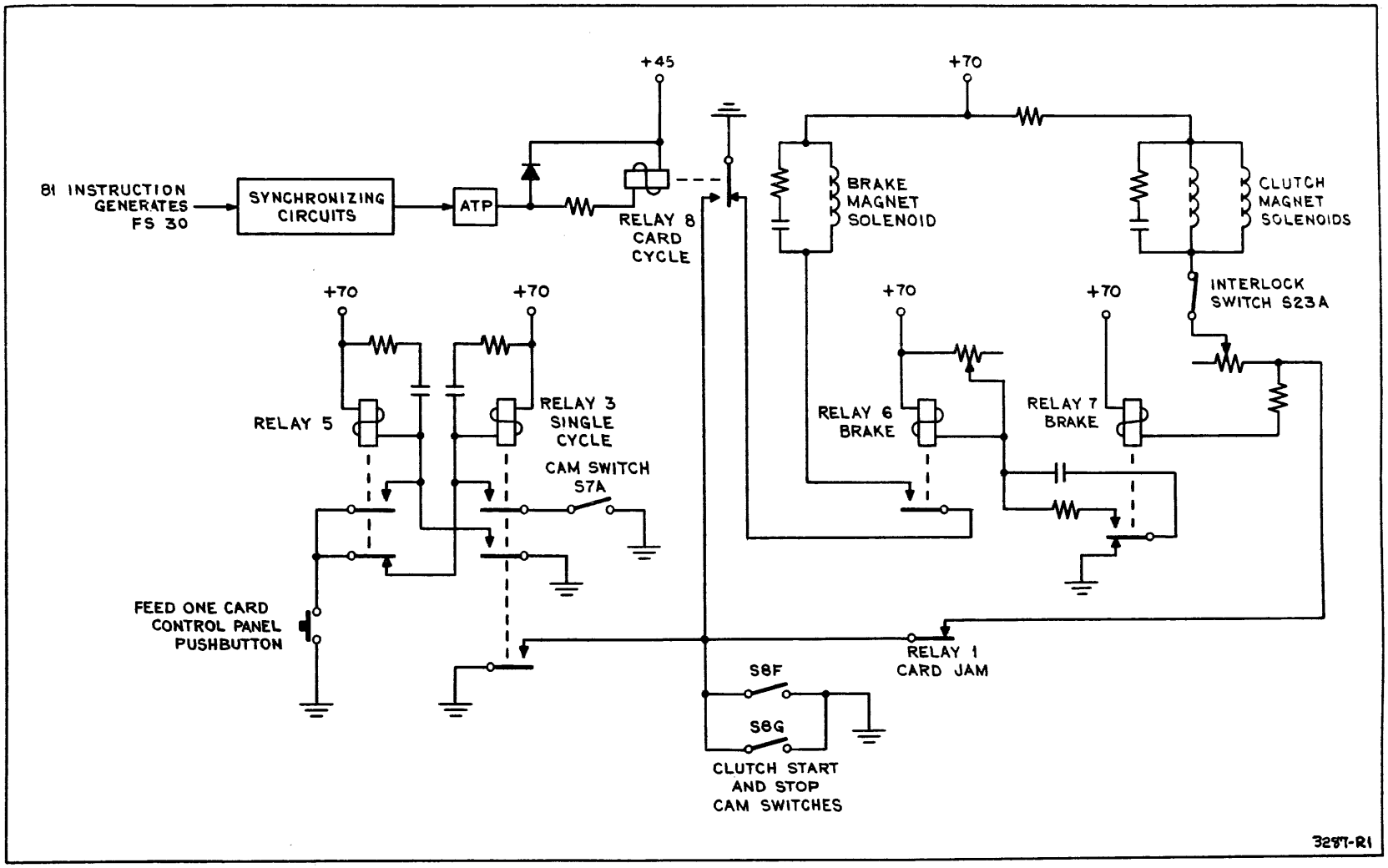


Figure 3-4. Clutch and Brake Control Circuitry

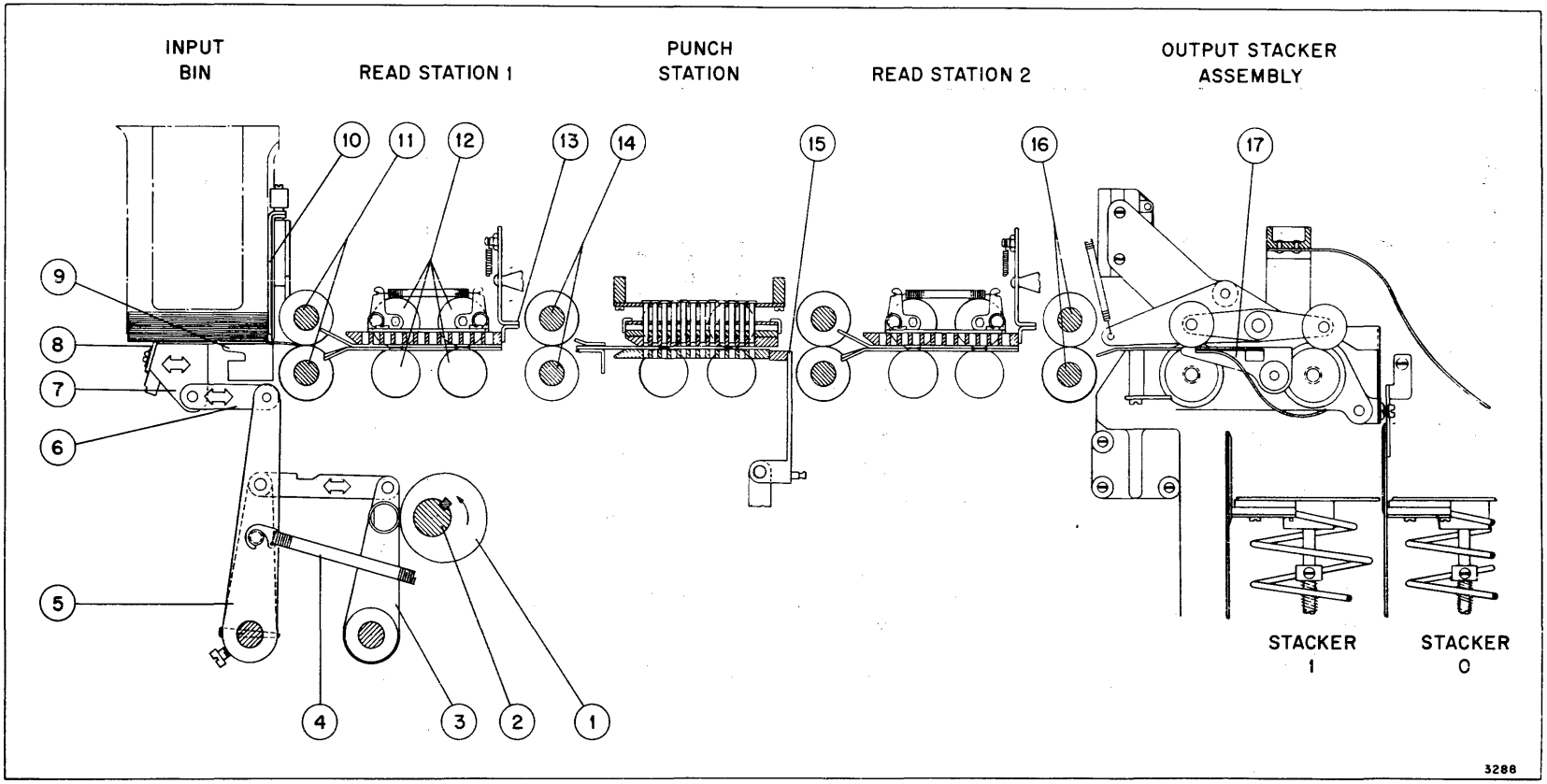


Figure 3-5. Transport Mechanism

1. Feed cam
2. Main drive shaft
3. Cam-follower arm
4. Tension spring
5. Feed arm
6. Feed link
7. Feed slide
8. Pickerknife
9. Throat block
10. Throat knife
11. Feed rollers, read station 1
12. Intermediate rollers, read station 1
13. Card stop, read station 1
14. Feed rollers, punch station
15. Card stop, punch station
16. Feed rollers, stacker
17. Sort fingers

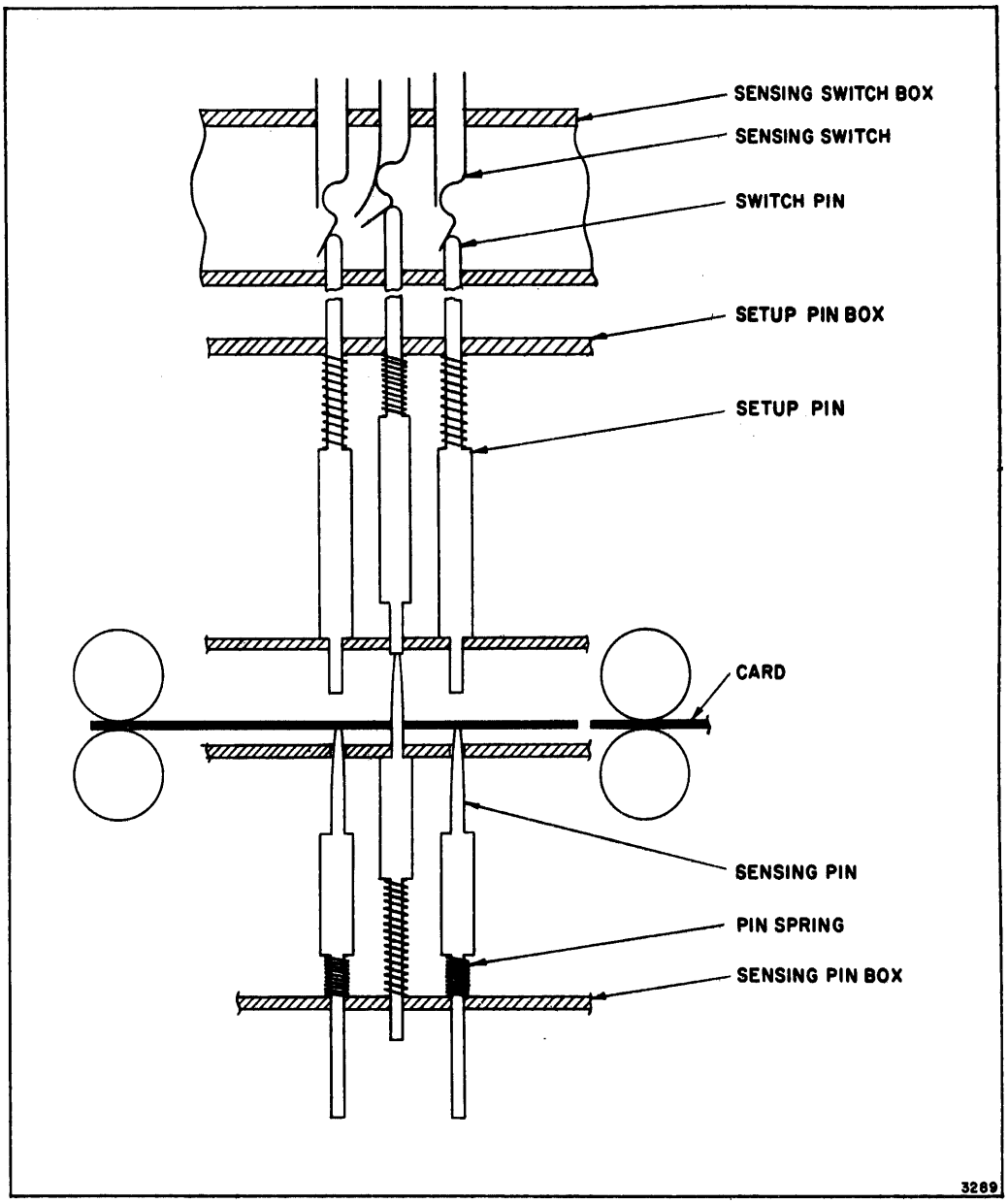


Figure 3-6. Sensing Mechanism

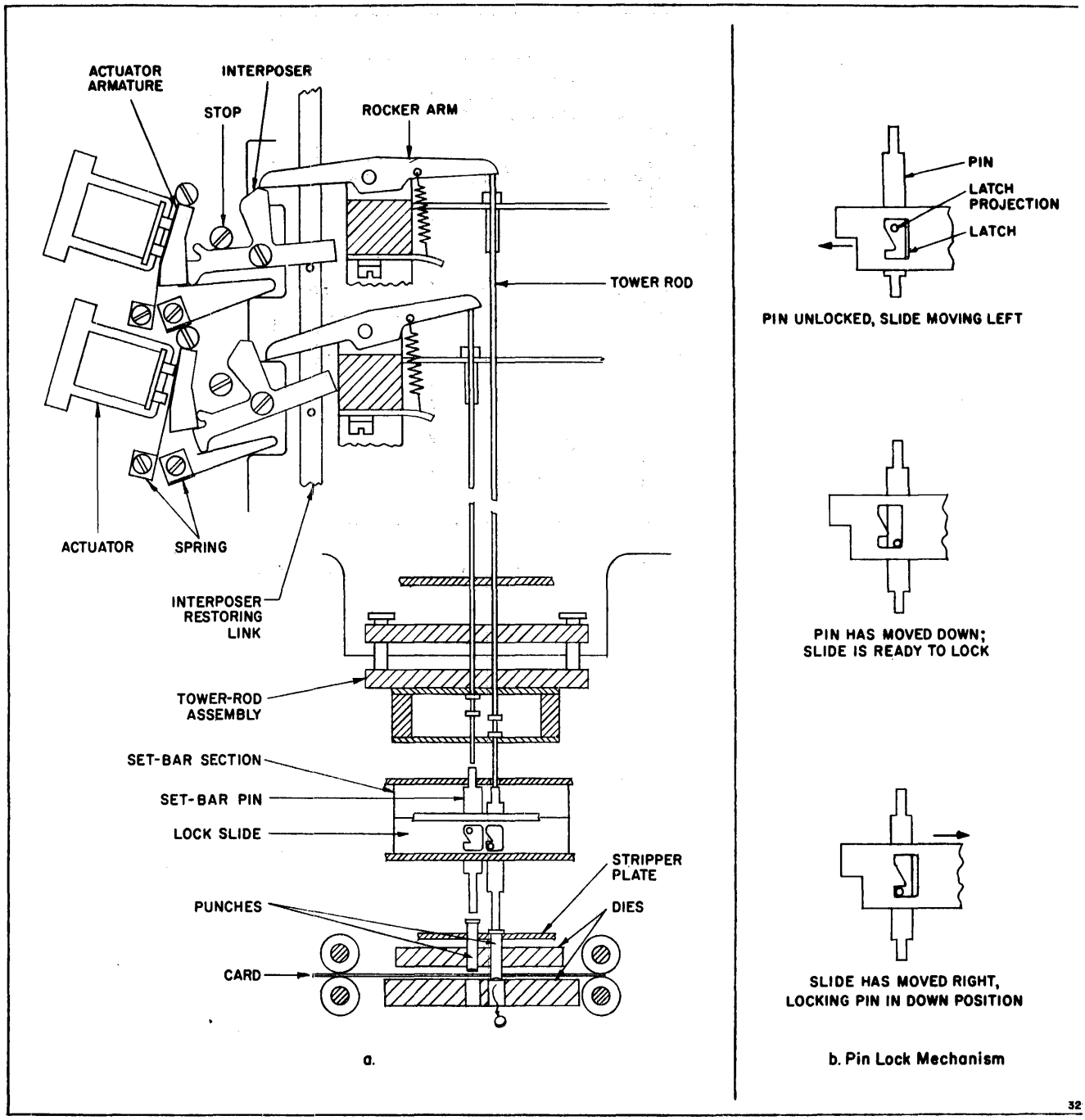


Figure 3-7. Punch Mechanism

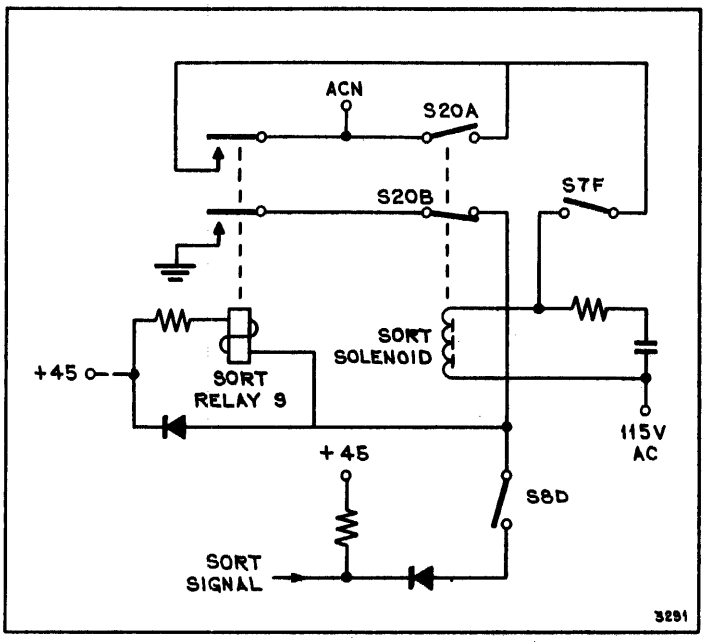


Figure 3-8. Stacker-Selection Relay Circuit

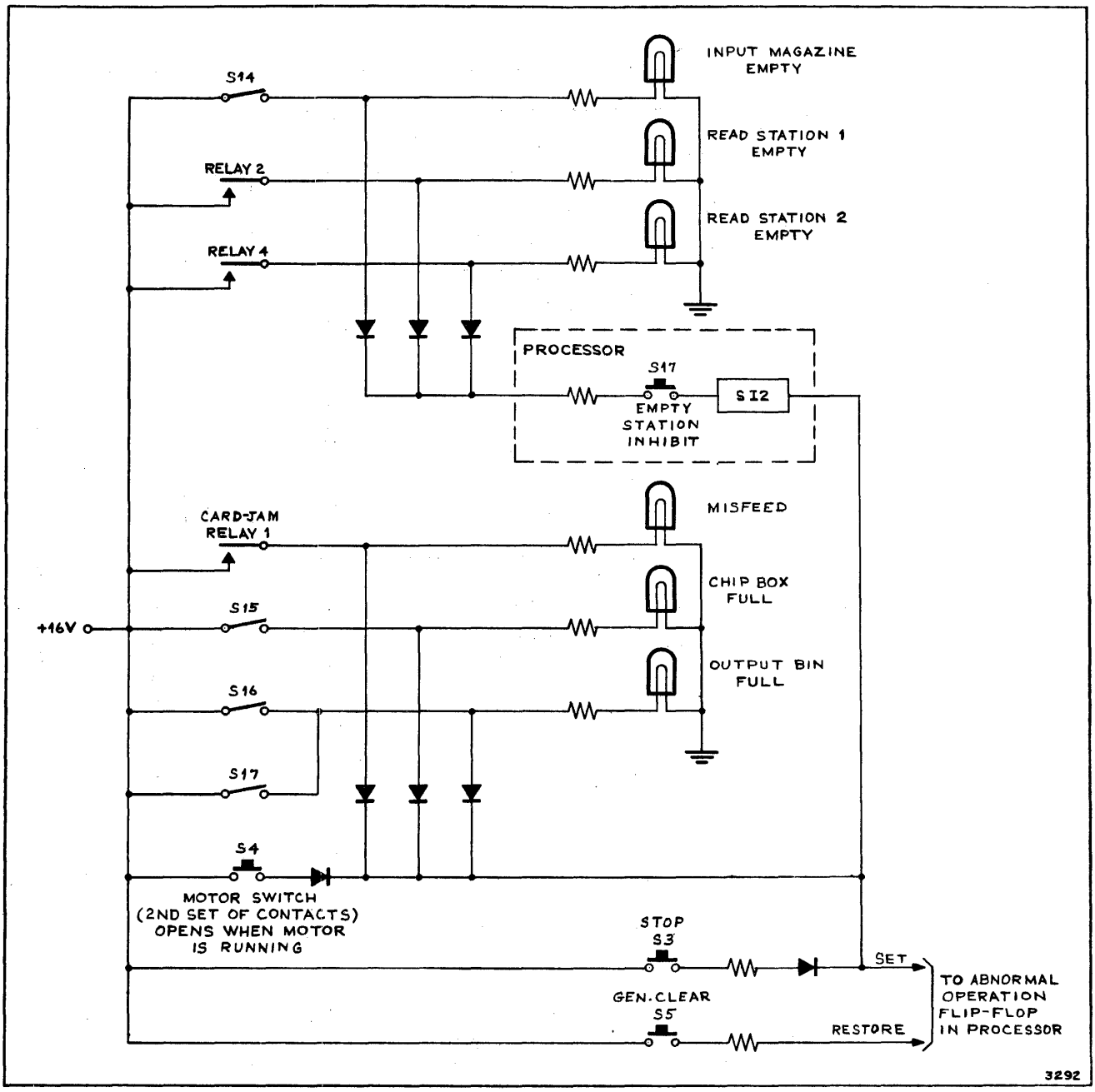


Figure 3-9. Abnormal Operations Circuit

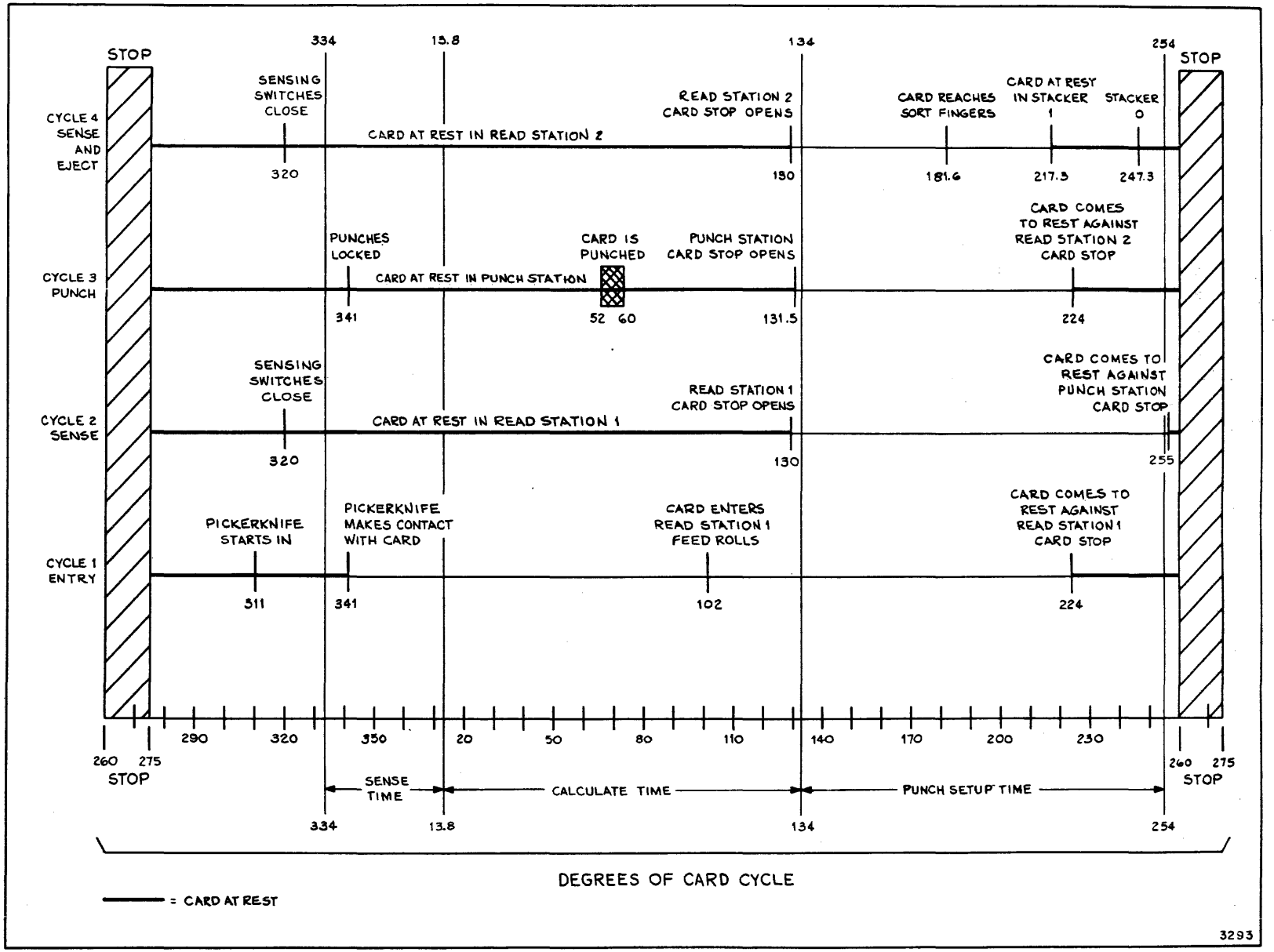


Figure 3-10. Read-Punch Unit Card Cycles

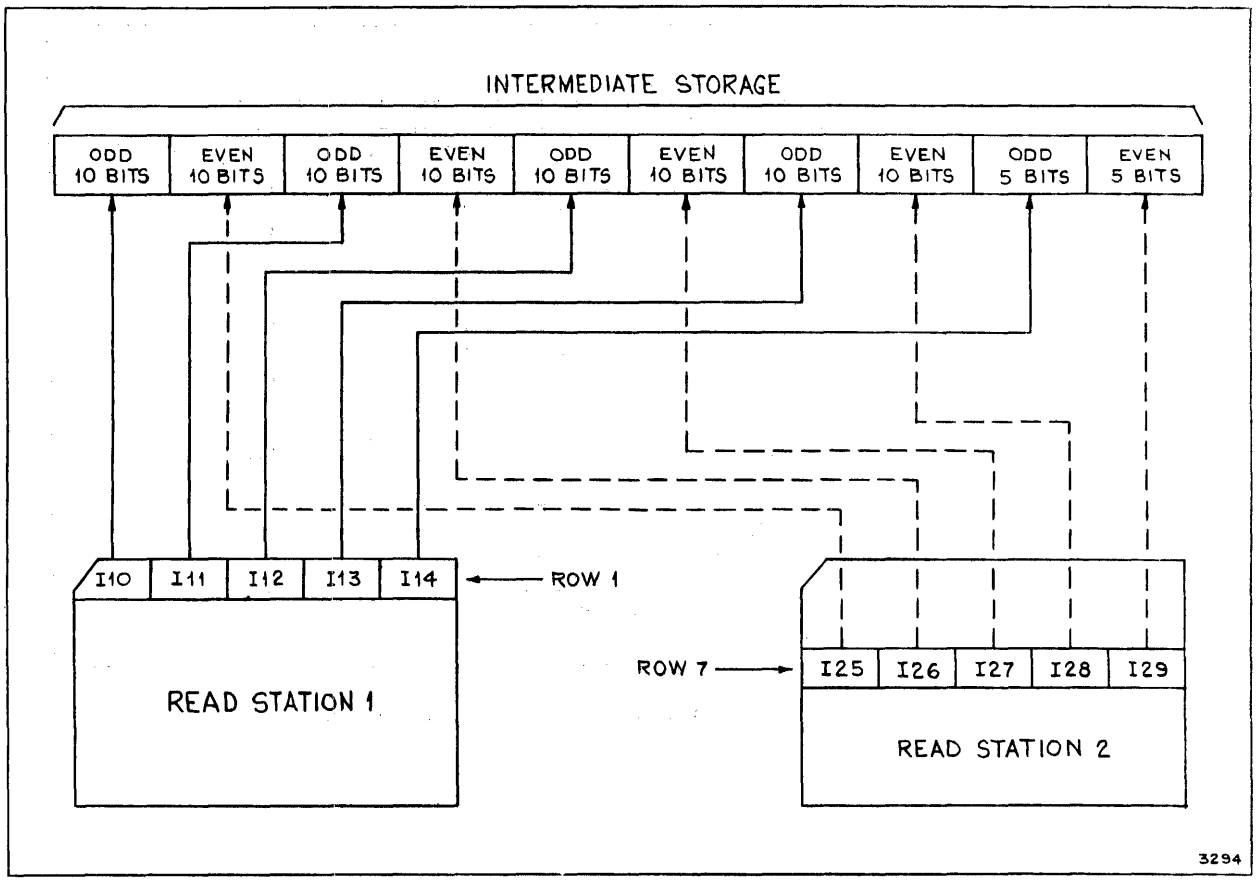


Figure 3-11. Transfer of Rows to Intermediate Storage

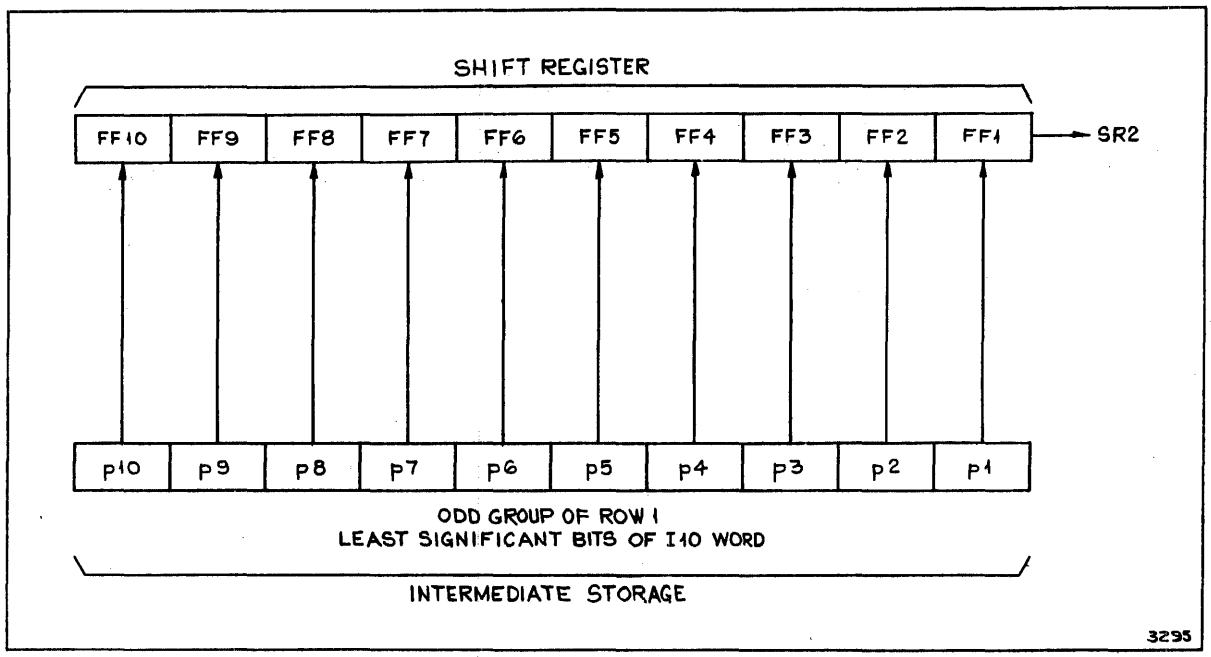


Figure 3-12. Transfer of Odd Groups

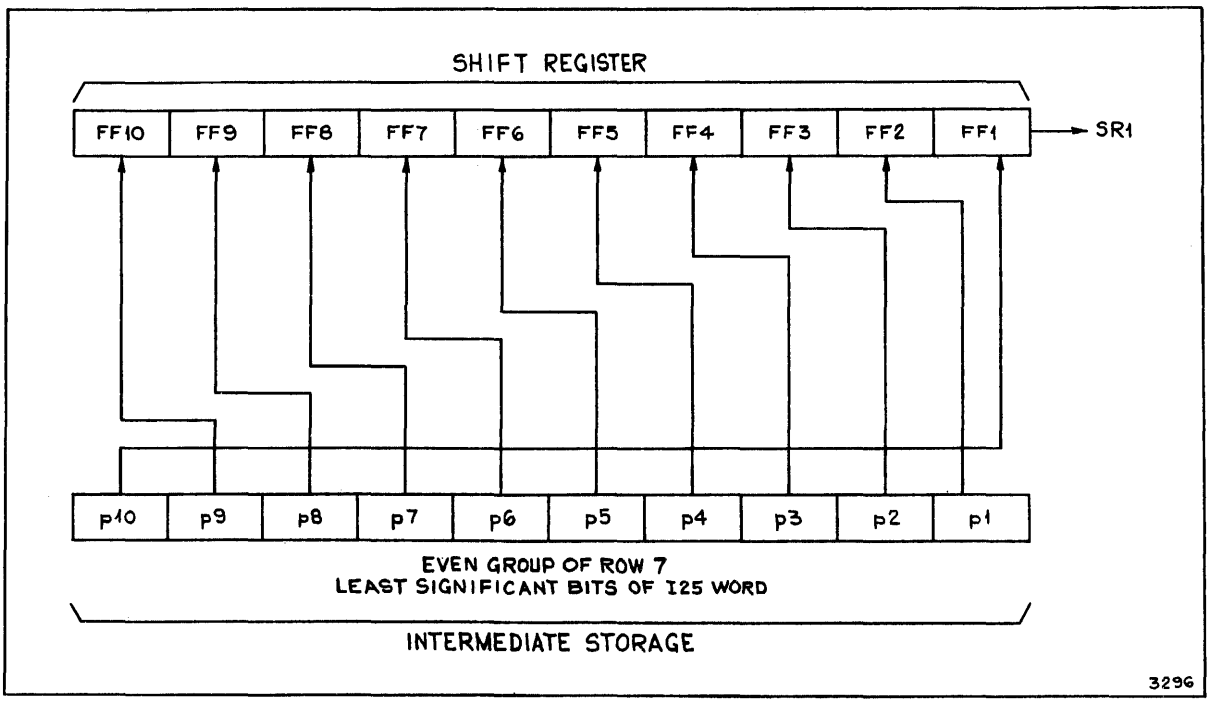


Figure 3-13. Transfer of Even Groups

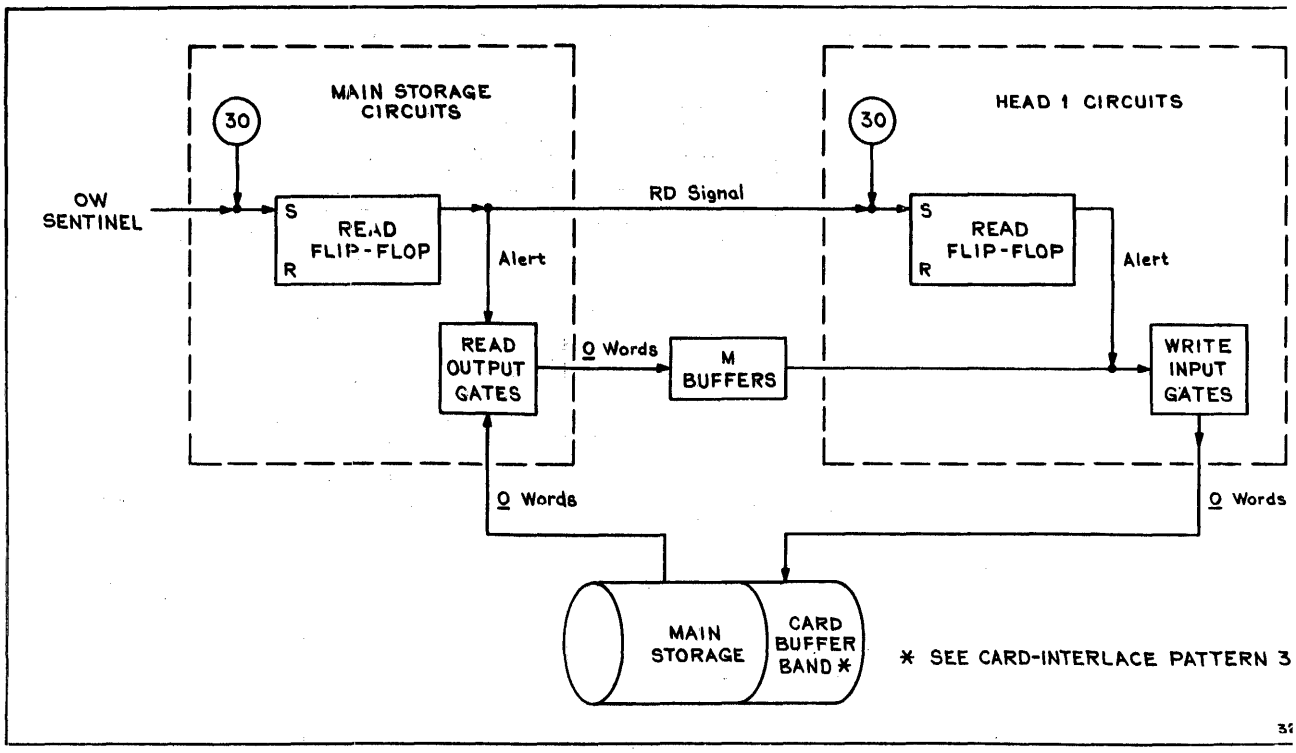


Figure 3-14. Main-Storage-to-Buffer Transfer (81 Instruction)

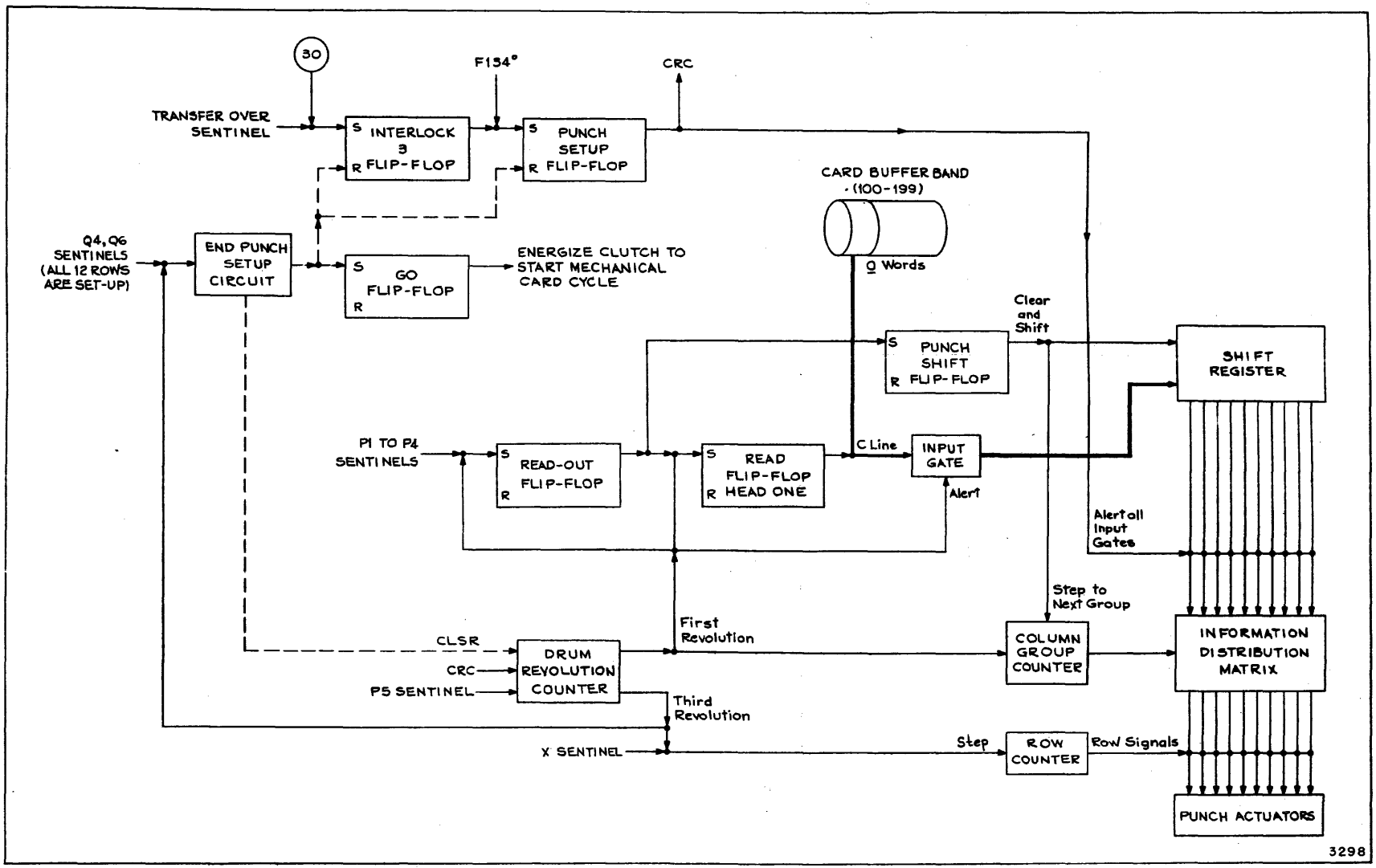


Figure 3-15. Punch Setup and End Punch Setup

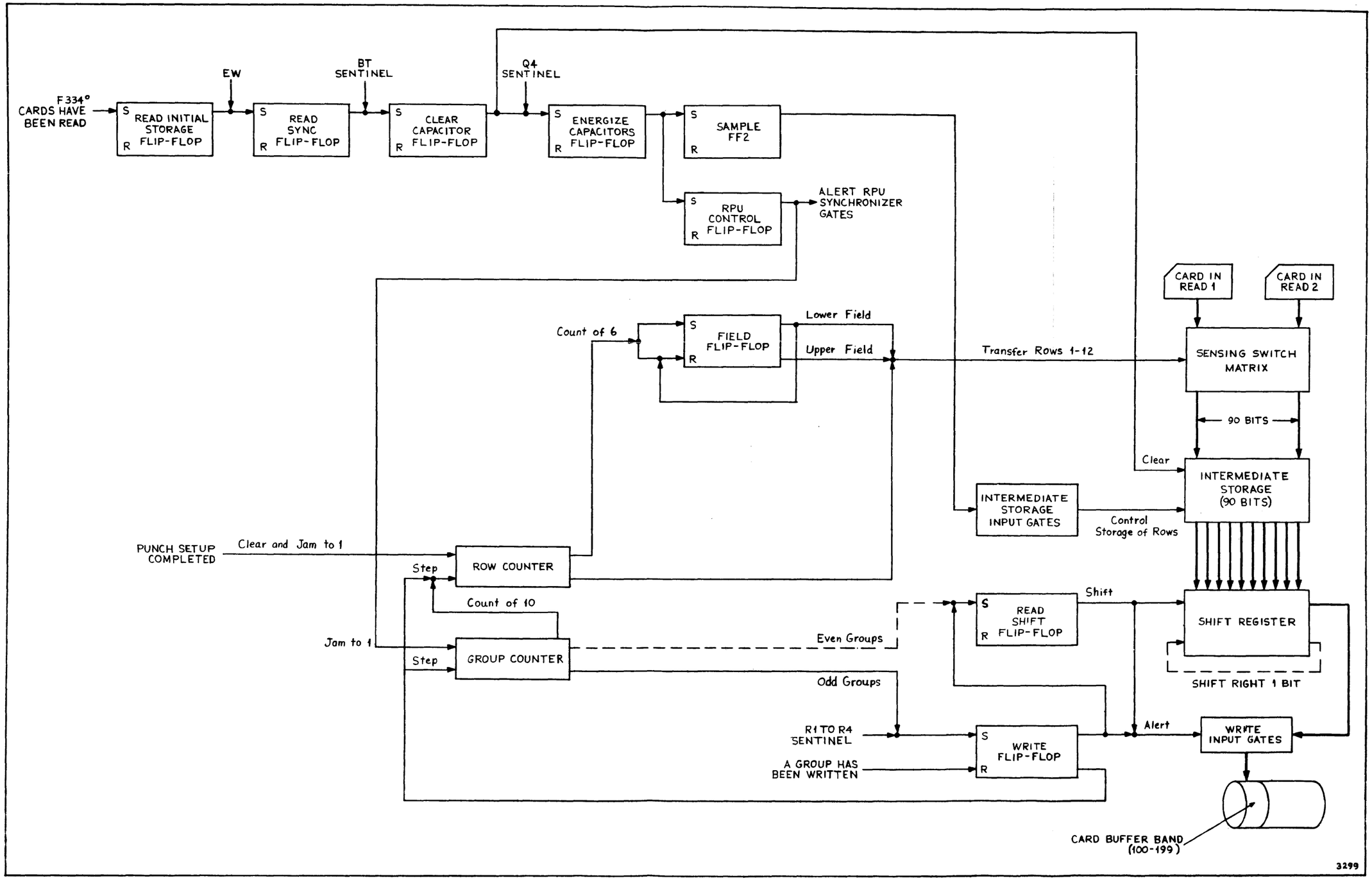


Figure 3-16. Transfer from Cards to Buffer

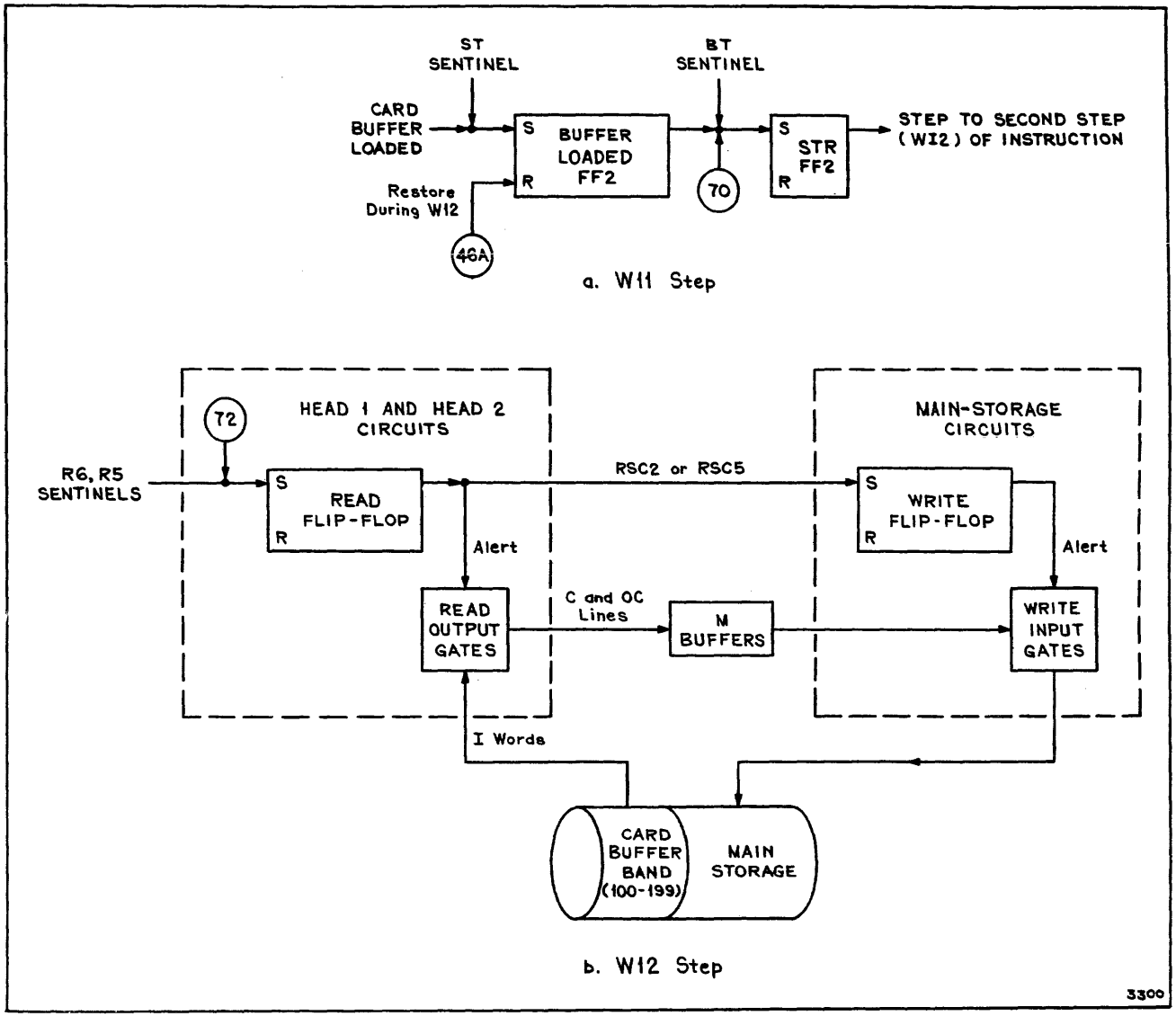


Figure 3-17. Buffer-to-Main Storage Transfer (46 Instruction)

SECTION IV

ELECTRONIC CIRCUITRY

4-1. SCOPE

The principal circuit elements used in the read-punch unit are semiconductor diodes, transistors, and magnetic amplifiers. Conventional vacuum tubes are not used.

This section treats only the circuitry of the read-punch unit which is not described in the central processor manual. Most of this circuitry is found in the intermediate-storage, information-distribution, and punch-actuator sections; the remainder of the circuitry is composed of conventional magnetic-amplifier and diode building blocks, familiarity with which is assumed.

Many of the circuits described in this section are located, not in the read-punch unit, but in the processor. They are included here because they function only during read-punch operations.

Current direction is taken as the direction of electron flow (from negative to positive).

4-2. GENERAL DESCRIPTION

The 540 positions of a punched card are pin-sensed simultaneously, and any pin which passes through a hole in the card mechanically closes a corresponding switch in one of the two 540-switch sensing-switch matrixes. As shown in figure 4-1, the input information is then transferred in parallel on 90 lines, one for each card column, into the intermediate storage circuits, where it is stored for a short time and then read out ten bits at a time into the ten-bit shift register. Control signals shift the information serially into buffer storage.

During punch setup time, output information is read serially from the buffer into the shift register, and then read out in parallel through the information-distribution matrix to the punch actuators. When all of the correct actuators for a card have been energized, all holes are punched simultaneously. The card travels on to read station 2 and then to the output stackers.

Figure 4-1 shows the relationship of various circuit-package types (PDGD, BFP, ATP, and TCS) to read-punch operation. These package types are described in the following sections.

4-3. SENSE CIRCUITS

4-4. INTERMEDIATE STORAGE

The intermediate-storage section of the read-punch unit contains 90 capacitors, one for each column. Information read from a card by a given sensing pin is stored as a charge on the corresponding capacitor until control signals cause the capacitor to discharge, transferring information into the ten-bit shift register.

Reference to the card-cycle timing (section 3-18) shows that sensing is done from 334° to 13.8°, an interval of 44.2 milliseconds, or from 12 to 13 drum revolutions. Each of the 12 rows of sensing switches is read during the time required for one drum revolution, capacitor clearing being accomplished during the first quarter revolution, card reading during the second, and readout of the capacitors to the drum buffer band during the third and fourth.

Figure 4-2 shows the intermediate-storage circuit associated with a single column. Each capacitor-storage package (CSP) contains the storage capacitors associated with five columns. Some of the circuitry associated with the capacitors is contained in the five-section capacitor-storage gating packages (CSGP). Each of the storage-capacitor circuits operates in the same manner as the one described below.

4-5. STORAGE AND READOUT. The lower end of storage capacitor C in the capacitor-storage package (CSP) is normally clamped to ground potential by current from the -29-volt supply through R1, CR3, and a ground-clamp diode in the final stage of the capacitor-sense-driver (CSD) package (figure 4-2). A negative-going clear signal from the clear-generator-driver (CGDT) or clear-generator (CGT) packages charges capacitor C to 29 volts through R2, CR6, and CR1.

The positions of the sensing switches corresponding to a row of the card are simultaneously determined by a signal applied to the corresponding TR" line in the sensing-switch matrix from one of the 12 row-switch (ARS) packages. This signal raises the normal -30-volt potential of the TR" lines to ground. If there is no hole in the card, the sensing switch is open and capacitor C retains its 29-volt charge. If the sensing pin encountered a hole, the sensing switch is closed, and capacitor C discharges through CR2 and the sensing-switch diode to the ground potential of the TR" line. (In the read-punch unit, sensing-switch diodes are in the (sensing-diode) TSD packages.) A charge on the capacitor, then, reflects the absence of a hole; the absence of a charge indicates a hole in that position.

To transfer the information from intermediate storage into the shift register, a positive signal from the CSD package raises the lower end of capacitor C to +16 volts. If the capacitor is charged to 29 volts, the +16-volt signal is insufficient to overcome the reverse bias on CR1, and no conduction takes place. If the capacitor is not charged, the CSD signal passes through CR3, C, and CR1 onto the TB lines to the shift register. The bit filter package (BFP) contains ten identical RC filters, one for each of the TB lines, the function of which is to filter out noise in the cable lines to the processor. These filters also provide a path to ground for any leakage currents through diodes which connect to the TB lines.

Diode CR1 in the CSP package is a buffer diode leading to a common line onto which other capacitors are buffed. If CR1 should leak, a bias circuit prevents the charge on capacitor C from flowing through CR1 and distributing itself among the other capacitors connected to the common line. Instead, any leakage currents flow through CR4, R3, and R4 to the +45-volt supply.

4-6. CAPACITOR CLEARING

Clearing the storage capacitors involves the actuator-transistor package (ATP), the clear-generator-tower (CGT) package, and the clear-generator-driver-tower (CGDT) package. The actuator-transistor package (figure 4-3a) consists of eight identical common-emitter transistors which drive various circuits in the read-punch unit. Figure 4-3b is a simplified composite schematic of the CGDT and CGT circuits, the function of which is to generate five separate, simultaneous Clear signals to clear the capacitor-storage unit. Transistor Q1 provides parallel drive for four other stages similar to Q2 which operate identically.

Current through CR1, R1, and R2 clamps the collector of the ATP transistor and one side of C1 to +16 volts. The other side of C1 and the base of Q1 are clamped to -10 volts by current through CR2 and R4. The normally low input to the ATP transistor keeps it cut off until a positive signal from the clear-capacitors flip-flop turns on the stage and causes the collector voltage to decrease to +6 volts. The negative-going 10-volt signal is applied through current-limiting resistor R3 and capacitor C1 to the base of Q1, turning on the stage and raising the collector voltage from -29 to -10 volts.

Transistor Q2, which is normally reverse-biased, is turned on by the positive-going signal. The output, which is normally clamped to +16 volts by current through CR4 and R7, falls to -29 volts. The negative-going 45-volt signal charges the capacitors in the CSP package.

4-7. CAPACITOR SENSE DRIVER (CSD)

Unlike most transistor packages in the system, the capacitor-sense-driver circuit does not require a special driving magnetic amplifier; that is, one in which the blocking pulses are removed from the output. Figure 4-4 shows that the input terminals of the capacitor sense drivers are connected to the ten TG lines from the group counter, which normally carry logically high signals, a steady flow of magnetic-amplifier power and blocking pulses. The values R1, R2, and C1 are chosen so that Q1 is reverse-biased when both power and blocking pulses are present at the input. When logically low signals, consisting of blocking pulses alone, are applied to the circuit, Q1 turns on.

A low signal at the input of the CSD package lowers the base voltage of Q1, turns it on, and causes current to flow through T1. The transformer produces an inversion of the signal, which is then applied to the base of Q2. Transistor Q2 is normally cut off, since its base is a positive 4 volts with respect to its emitter. When the signal is applied to its base, Q2 is turned on and a positive 16-volt signal is available at the output of the CSD package. This signal is applied to the capacitor storage packages to permit readout of their stored information.

Diode CR2 is a damping diode which prevents voltages from building up across the primary of T1 that might exceed the voltage rating of the collector of Q1. Resistor R1 prevents loading of the driving stage, and R4 is a current-limiting series resistor. Diode CR3 is a ground-clamp diode which maintains the output at zero volts until Q2 turns on.

4-8. PUNCH CIRCUITS

Normally, the 45 column lines of the punch-actuator matrix (figure 4-5) are at ground potential. Since the 12 row lines are at -30 volts, the actuator series diodes in the TAD packages prevent current from flowing through the actuators.

During punch setup time, information coming from the shift register passes through the punch-distribution-gate-driver (PDGD) packages into the diode information-distribution matrix. The diodes of the matrix are contained in punch-distribution-gate (PDG) packages. Other PDGD circuits, driven by outputs of the group counter, also feed the information-distribution matrix, which is constructed so that the 45 column lines are actuated in accordance with table 4-1.

Table 4-1. Information Distribution Matrix

Shift Register PDGD	Column Selected				
	Group Counter PDGD 2	Group Counter PDGD 3	Group Counter PDGD 4	Group Counter PDGD 5	Group Counter PDGD 6
1	1	11	21	31	41
2	2	12	22	32	42
3	3	13	23	33	43
4	4	14	24	34	44
5	5	15	25	35	45
6	6	16	26	36	not used
7	7	17	27	37	not used
8	8	18	28	38	not used
9	9	19	29	39	not used
10	10	20	30	40	not used

High signals on the SR1 through SR10 lines in parallel from the ten-bit shift register indicate that holes are to be punched in the columns selected by the group-counter PDGD packages. When the shift-register contents enters the ten selected column-switch flip-flops, any flip-flop which receives a high signal is set, and the potential of the corresponding column line is lowered to -30 volts. (Each column-switch flip-flop is marked ACDT in figure 4-5.) When an output from the row counter actuates any of the 12 row switches (ARS packages), the potential of the corresponding TR" line is raised to ground. Current then flows through the punch actuators and diodes at the intersections of the energized row and column lines, causing the correct punches to be set up and mechanically locked. (The row switches also energize the TR" lines consecutively at the appropriate time during card sensing.)

After each row of actuators is set up in ten-column groups, the column reset generator (CRG), driven by the column-reset flip-flop, supplies a signal to the column-switch flip-flops which clears them, permitting new information to set up the next row of actuators. When the row-by-row setup is completed, the energized actuators punch holes in the card simultaneously. The energized actuators are reset mechanically after the punching operation.

4-9. PUNCH-DISTRIBUTION GATE DRIVER (PDGD)

The punch-distribution gate driver (PDGD) circuits set the column-switch flip-flops through the information-distribution matrix diodes. Figure 4-6 is a schematic of the circuitry connected with a single column of the punch-actuator matrix. The 18 PDGD circuits, two to a package, used in the read-punch unit are identical in operation.

Normally, low inputs from the transistor-driver magnetic amplifiers, which are driven by either the shift register or the group counter, cause the emitter of Q1 to be maintained at approximately 3 volts, as the majority of the voltage developed by current from the -10-volt supply is developed across R2. Transistor Q1 is therefore reverse-biased, with no current in the collector circuit. Current from the -45-volt supply through R4 and the base and emitter of Q2 to the -10-volt supply biases Q2 in the forward direction, holding the base of Q2 and the collector of Q1 at -10 volts. The output of the PDGD circuit is normally about -10 volts, since most of the voltage developed by current from the -45-volt supply through R5, R6, and Q2 is developed across load resistor R5.

A positive input pulse from the shift register or group counter causes current to flow from the +6-volt supply through the base and emitter of Q1, R1 and CR1, turning Q1 on. Approximately +6 volts appears at the base of Q2, cutting it off and dropping the output to -45 volts.

As shown in figure 4-6, each set input of the 45 column-switch flip-flops (section 4-10) is connected to two information-distribution matrix diodes, one of which is driven by a shift-register PDGD and the other by a group-counter PDGD. Since the normal PDGD output is -10 volts, both diodes are conducting, and the set input of the column-switch flip-flop is at its normal -10 volts. To change the state of the set input line, the outputs of both PDGD packages must drop to -45 volts; that is, the information-distribution matrix acts as 45 gates, one for each card column.

4-10. COLUMN RESET GENERATOR (CRG)

Normally, a steady flow of magnetic-amplifier pulses rectified and smoothed by C3 provides an approximately constant +16-volt input to the column reset generator. This input reverse-biases Q3 and causes the -45-volt supply voltage to appear at the output. When negative-going input signals reverse-bias CR2, current flows from the -30-volt supply through R7 and the base and emitter of Q3 to the +6-volt supply, turning Q3 on, and raising the circuit output to about +6 volts. This positive-going signal is used to reset, through R9 and CR3, each of the 45 column-switch flip-flops which drive the punch-actuator matrix.

4-11. COLUMN-SWITCH FLIP-FLOP (ACDT)

The timing of inputs to the column-switch flip-flop is of considerable importance in understanding the operation of the circuit. The set input pulse can occur at various times during the interval from point A to point B (figure 4-6), according to which columns are selected.

When the flip-flop is reset, current flows from the -45-volt supply through R10 and the information-distribution matrix diodes to the -10-volt output of the PDGD circuits, keeping the set input line at -10 volts. Transistor Q4 is on, and a -32-volt potential between the collector of Q4 and the base of Q5 provides 2 volts of reverse bias to keep Q5 turned off. The collector of Q5 is clamped to ground by current flow through CR5 and R13 to the +45-volt supply. In the absence of reset pulses, the reset line is at -45 volts, which is sufficient to reverse-bias CR3.

To set the flip-flop, each of the two information-distribution matrix diodes must receive a -45-volt pulse from its PDGD driver. When the pulse occurs, current from the -45-volt supply through R10 is switched into the feedback circuit containing R14. The current drives the base of Q4 approximately 3 volts negative with respect to the emitter and turns the stage off. As the collector voltage of Q4 rises, current from the -30-volt supply through the emitter and base of Q5 and R12 to ground turns on Q5 and drops the output of the flip-flop to -30 volts. When the set pulse ends, current from the -45-volt supply through R10 is again switched back through the information-distribution matrix diodes, sufficient current flows from the -45-volt supply to the -30-volt output through R11 and R14 to keep the base of Q4 negative with respect to the emitter, and the flip-flop remains set.

In order to reset the flip-flop, the reset line is driven to +6 volts by the CRG output. Diode CR3 becomes forward-biased, sufficient current flows from the feedback circuit through CR3 and R9 to overcome the reverse bias on Q4, and the stage turns on. As Q4 turns on, the collector voltage drops to -32 volts. Because the collector of Q4 is directly coupled to the base of Q5, Q5 becomes reverse-biased and turns off. The output of the ACDT circuit rises to ground potential.

4-12. ROW SWITCHES (ARS)

Operating in conjunction with the column-switch flip-flops, row switches like the one shown in figure 4-7 reduce the potential on the TR" lines from -30 volts to ground, enabling the punch actuators to be energized during punch-setup time, and providing a discharge path for the charged storage capacitors during sense time.

Normally, high input pulses charge C1 to +16 volts, reverse-biasing Q1 and turning the stage off. Current through R3 and CR2 clamps the base of Q2 to slightly more than -10 volts. (The value exceeds -10 slightly because of the voltage drop across CR2.) Hence the Q2 stage is turned off as well. Transistor Q3 is also turned off, since the emitter is grounded and the base is clamped to +3 volts by current through R4 and CR3.

Negative-going signals from the row counter turn on Q1. Approximately +6 volts appears at the collector of Q1 and the base of Q2. Transistor Q2 turns on, placing -10 volts on the base of Q3, which also turns on, grounding the output TR" lines. The required actuator and capacitor discharging operations can then take place during punch setup time and sensing time.

4-13. TIMING-CAM SYNCHRONIZER (TCS)

During the basic cycle of the read-punch unit, two cam-operated switches determine the duration of sense time or punch setup time. At appropriate times, the switches ground the normally open input of the two identical circuits contained in the timing-cam synchronizer (TCS) package (figure 4-8). Since current through CR1 and R2 normally clamps the TCS output to +16 volts, and since no current flows through R1 because of the open input line, C1 is charged to -29 volts. When the input cam switch closes, the output decreases from +16 volts to -29 volts. Capacitor C1 reverses polarity and begins to charge to +16 volts because of current through R2. Since the time constant of the C1-R2 combination is 15 microseconds and the cam switch is closed for a period measurable in milliseconds, the output consists of a negative spike at the beginning of sense or punch time.

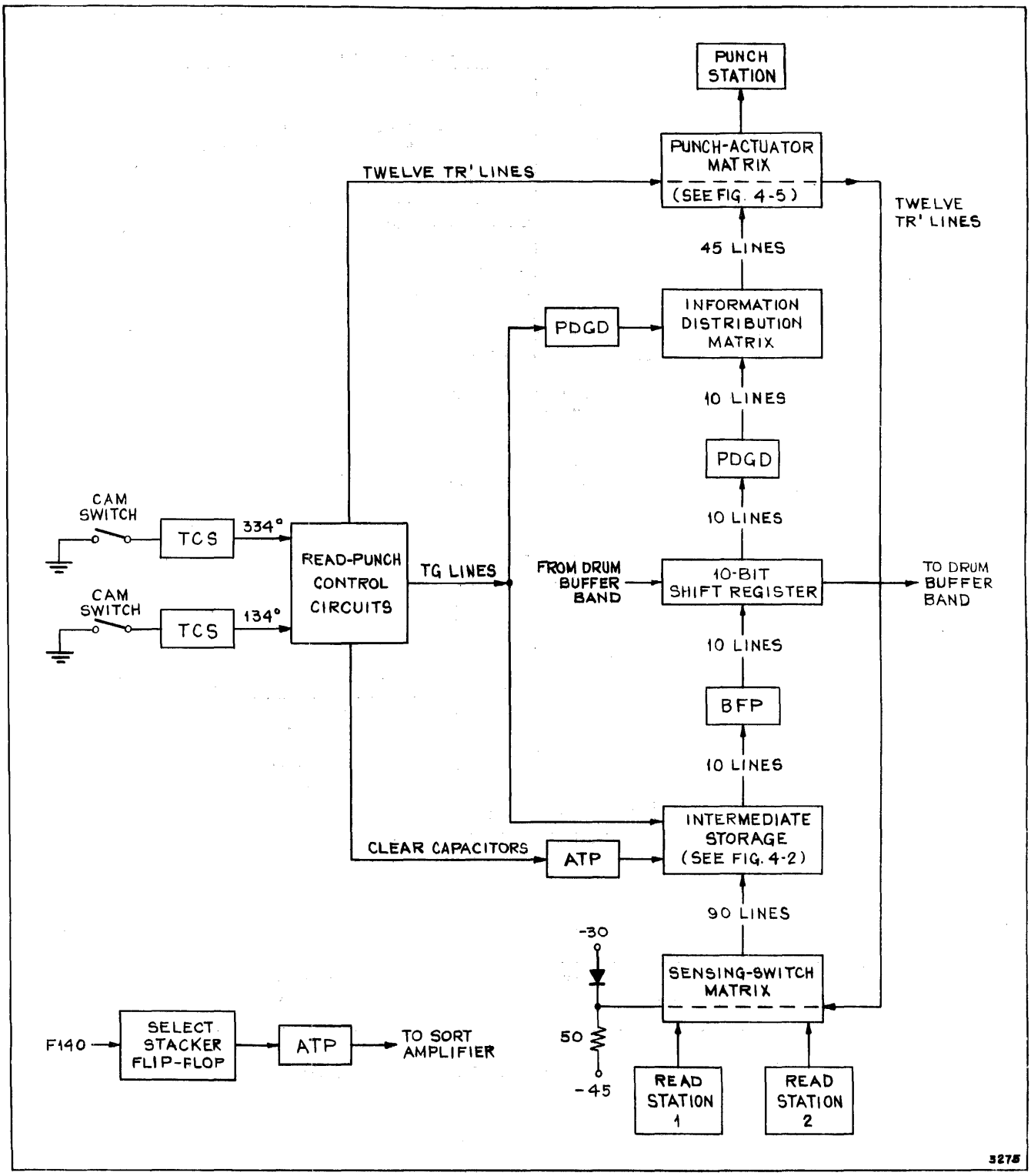


Figure 4-1. Read-Punch Circuitry

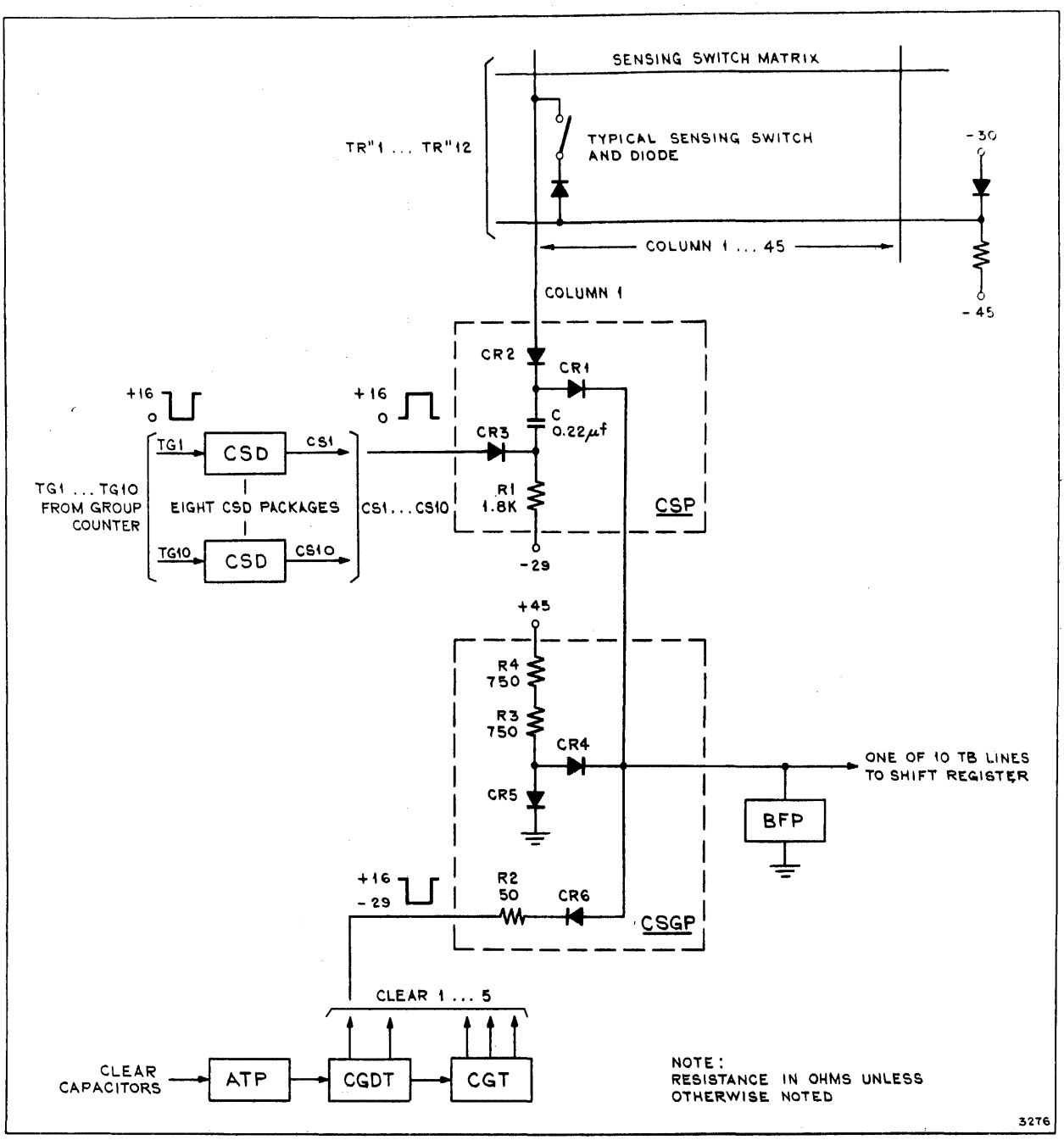


Figure 4-2. Intermediate Storage

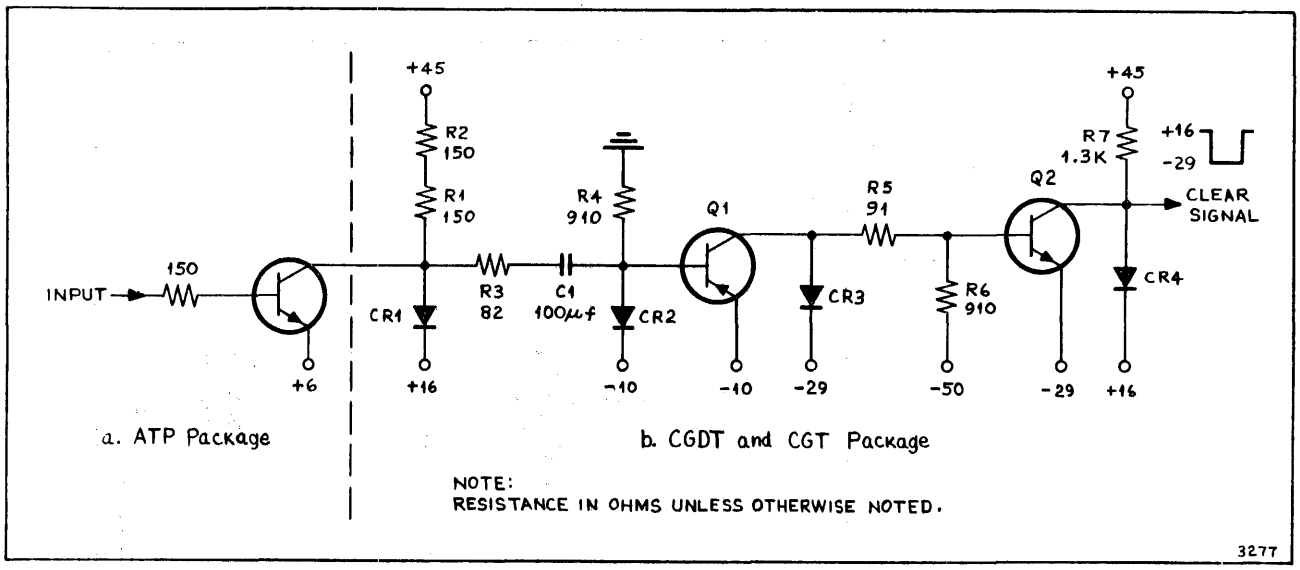


Figure 4-3. Capacitor Clearing

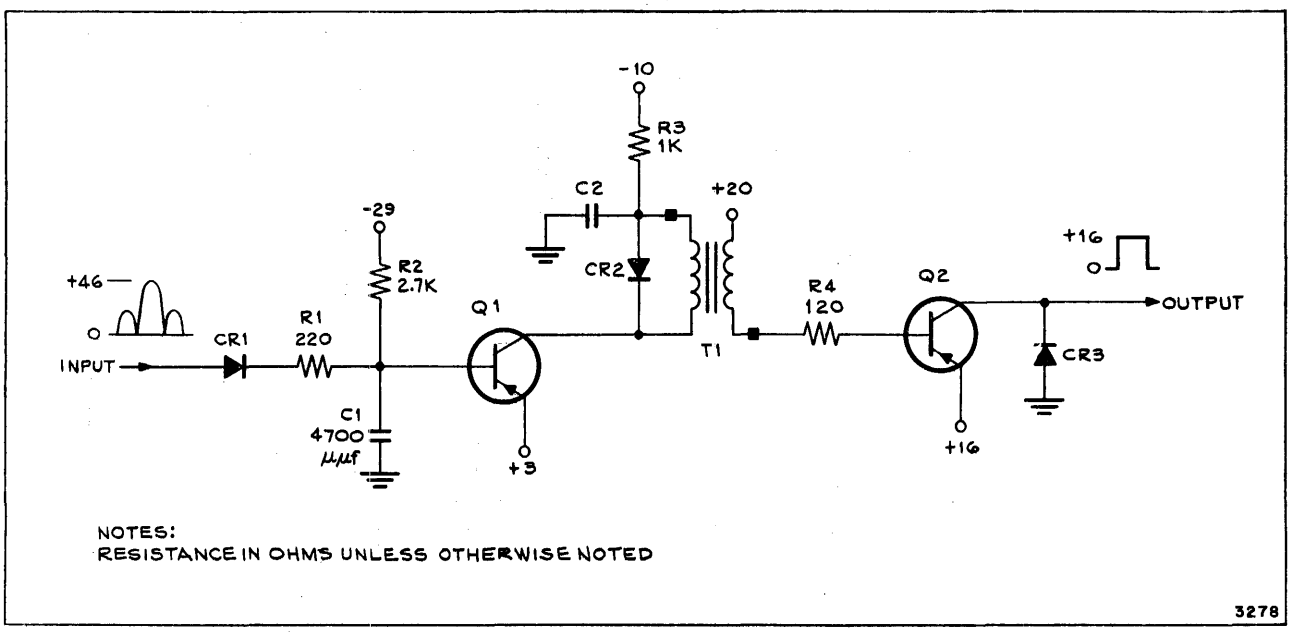


Figure 4-4. Capacitor Sense Driver

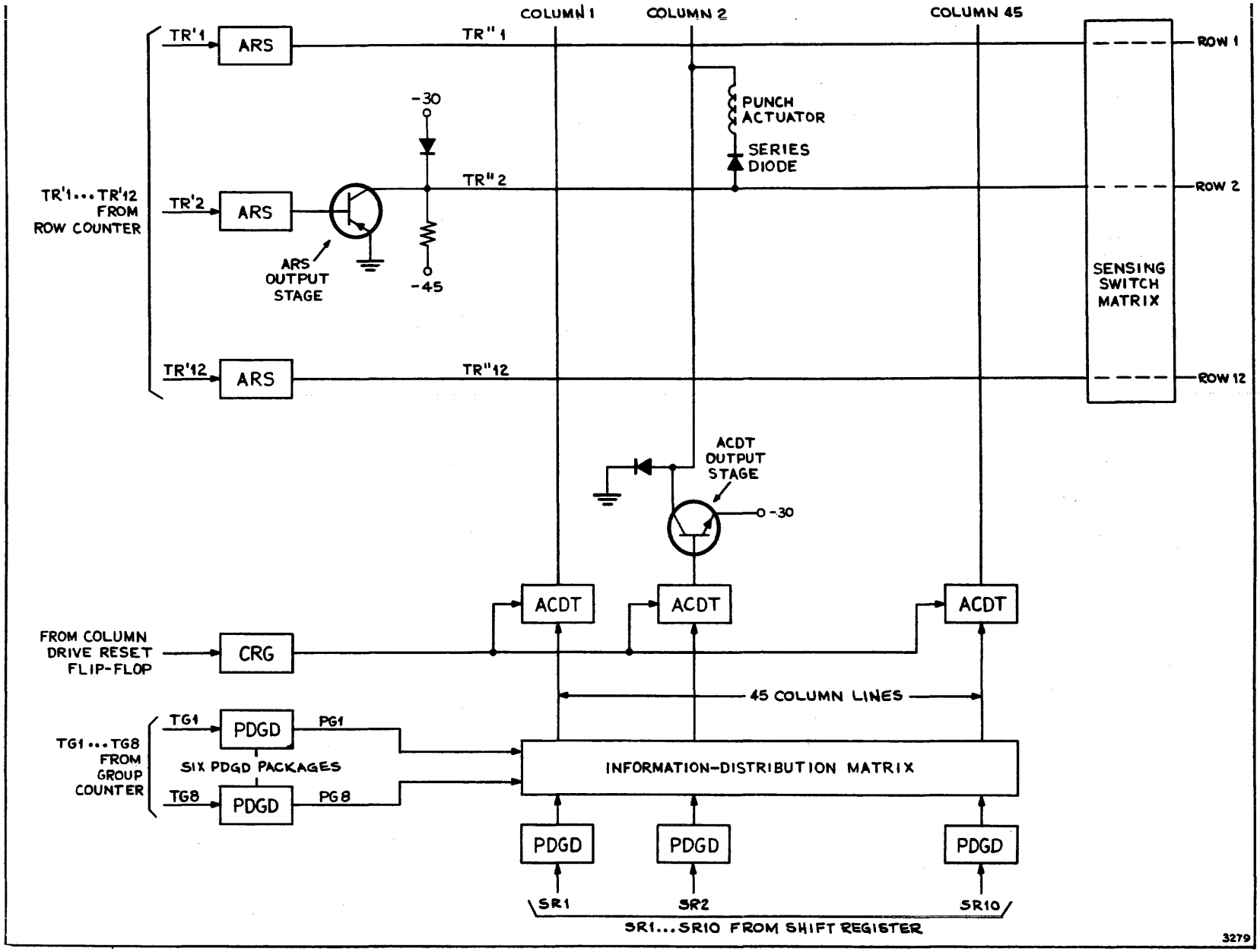


Figure 4-5. Punch-Actuator Matrix

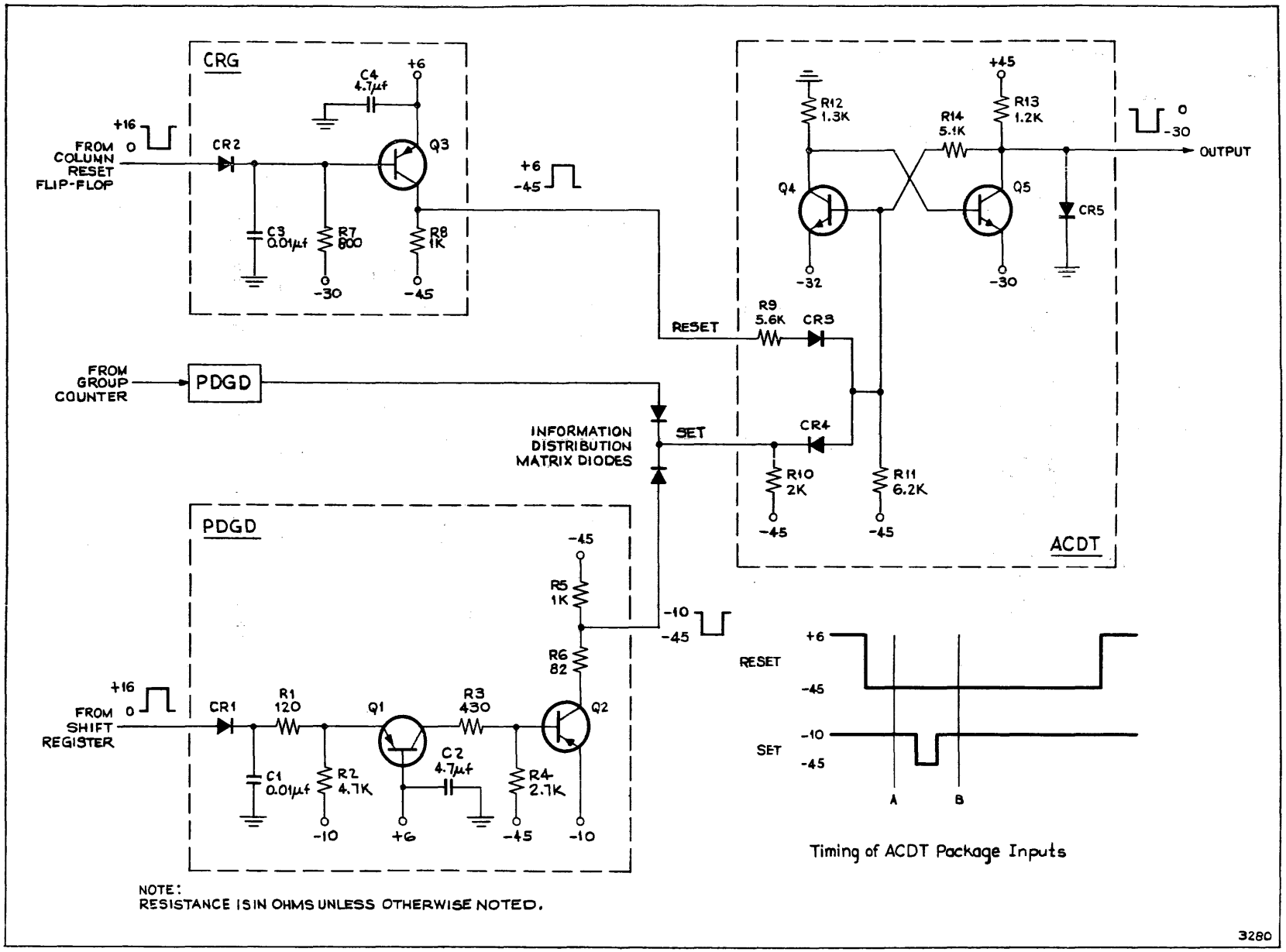


Figure 4-6. Punch Circuitry

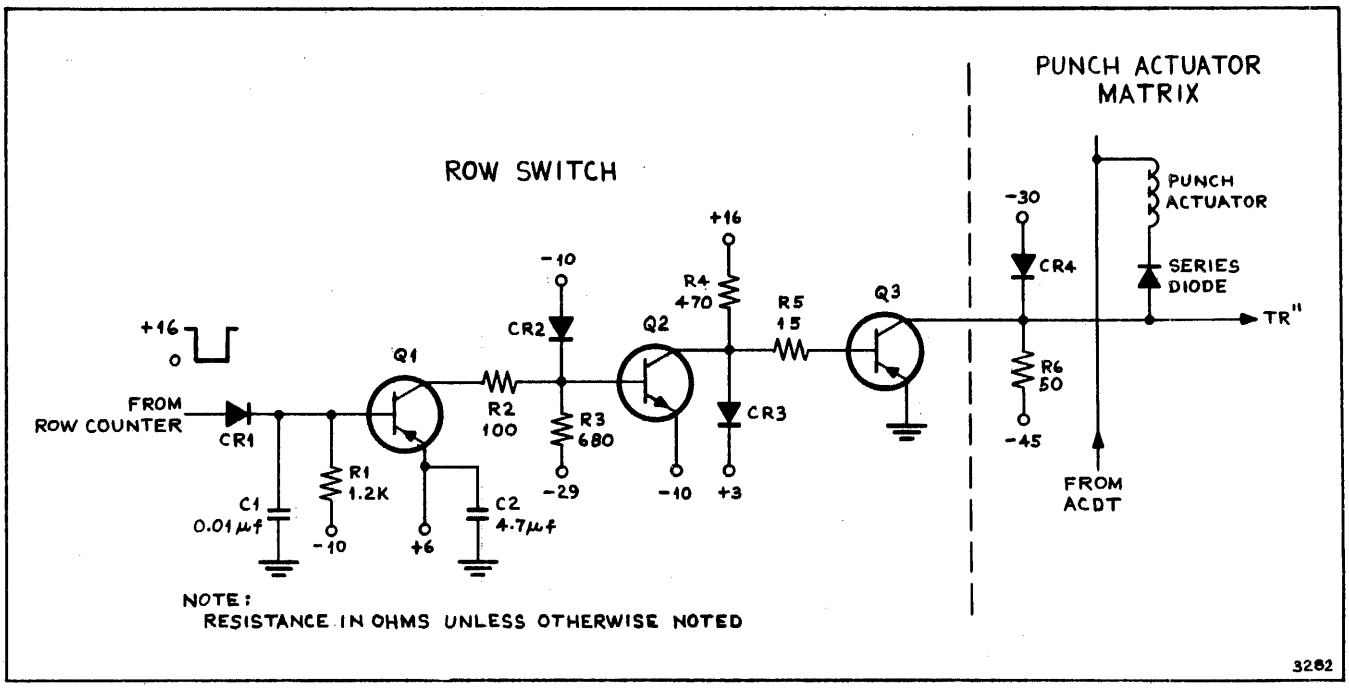


Figure 4-7. Row Switch

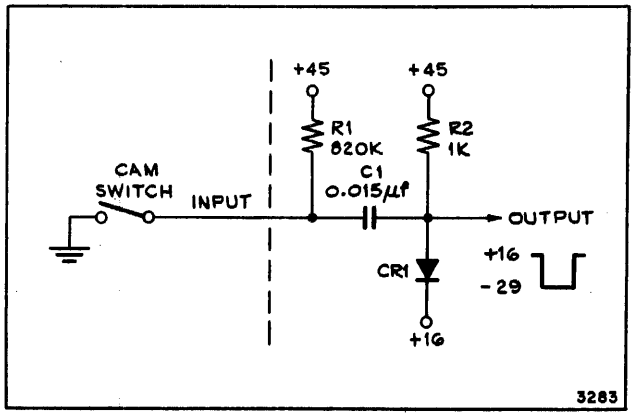


Figure 4-8. Timing-Cam Synchronizer