UNIVAC II

SUPPLEMENTAL MAINTENANCE

INFORMATION

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Remington Rand Univac®

DIVISION OF SPERRY RAND CORPORATION

UNIVAC PARK, ST. PAUL 16, MINNESOTA

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UNIVAC II
SUPPLEMENTAL MAINTENANCE INFORMATION MANUAL

1. GENERAL

An installation of the Univac II System consists of two major groups of equipment: the Central Computer group and the Input-Output Auxiliaries. The Central Computer group consists of the Central Computer, the Uniservos, the Power Supply, the Switchgear, the Motor-Generator Set, the Transformer, and the Supervisory Control Console with its Printer Dolly. All of these units are inter-related in function and cannot be treated separately. The Input Auxiliaries are those transcribing devices which receive information in the raw state (printed, written, or punched cards) and translate it into information on tape which is comprehensible to the Central Computer. The Output Auxiliaries receive information from the Central Computer, in the form of tape recordings, and translate it into printed matter or punched cards.

A typical Central Computer installation is shown in Figure 1-1. At the left are the three components of the Supervisory Control Console: the monitor oscilloscope, the control panel and keyboard, and the printer. At the rear is the Central Computer and at the right, lined up perpendicular to the length of the Central Computer, are the Uniservos. The Power Supply, which does not appear in the photograph, is behind the computer.

This manual includes a detailed physical description of the Central Computer group and an electrical description of the basic circuits. The remainder of the manual is devoted to maintenance and troubleshooting information.

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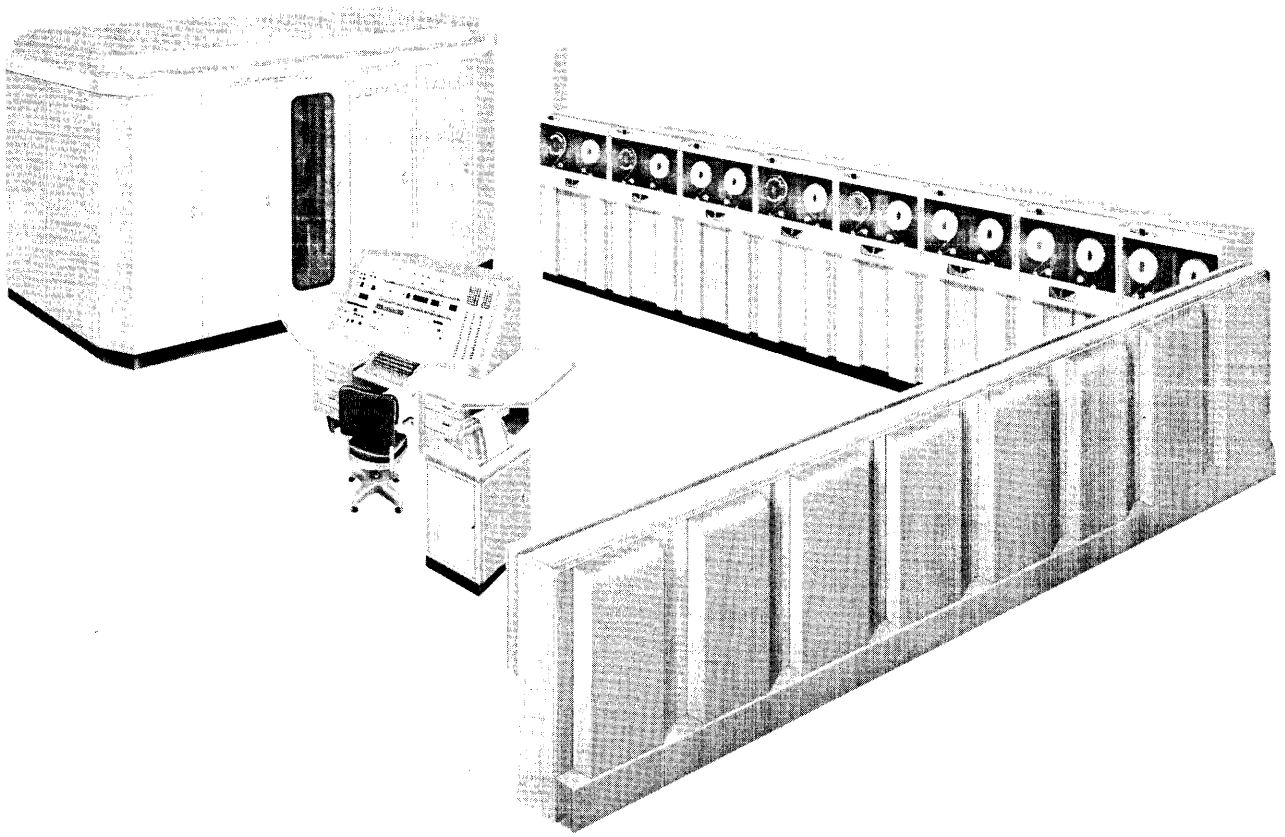

Figure 1-1. A Typical Central Computer Installation

(Continued from Page 1)

Maintenance information on the input-output auxiliaries are not given here, since they are covered in complete detail in the manuals for those equipments.

2. PHYSICAL DESCRIPTION OF CENTRAL COMPUTER

a. GENERAL. - The Central Computer group is composed of a number of modular units; this feature facilitates the location and replacement of components and the tracing of connections. The major modular unit is the "bay", of which there are a total of 28. The bays are assigned discrete alphabetic and numeric designations.

The larger bays of the Central Computer are divided into "sections". The sections of each bay are designated T, V and X, from top to bottom.

The smallest modular division of the Central Computer group is the "unit". Each section or bay is composed of a number of units, which are assigned alphabetical and numeric designations. A unit may be a chassis, a fuseboard, an indicator panel, or any externally-mounted componentof the Central Computer group.

b. MODULAR BREAKDOWN

(1) BAYS. - The Central Computer is divided into 18 bays, as shown in Figure 2-1. Thirteen of these bays, designated A, B, C, D, E, M, N, G, H, J, K, L & P consist of the unit chassis mounted on their backboards. The remaining bays are designated as follows: bay 0 is the access door, bays 1, 2, 3 and 4 are the corners.

A list of all the bays of the Central Computer, and the principal circuits contained in each, is provided in Table 2-1.

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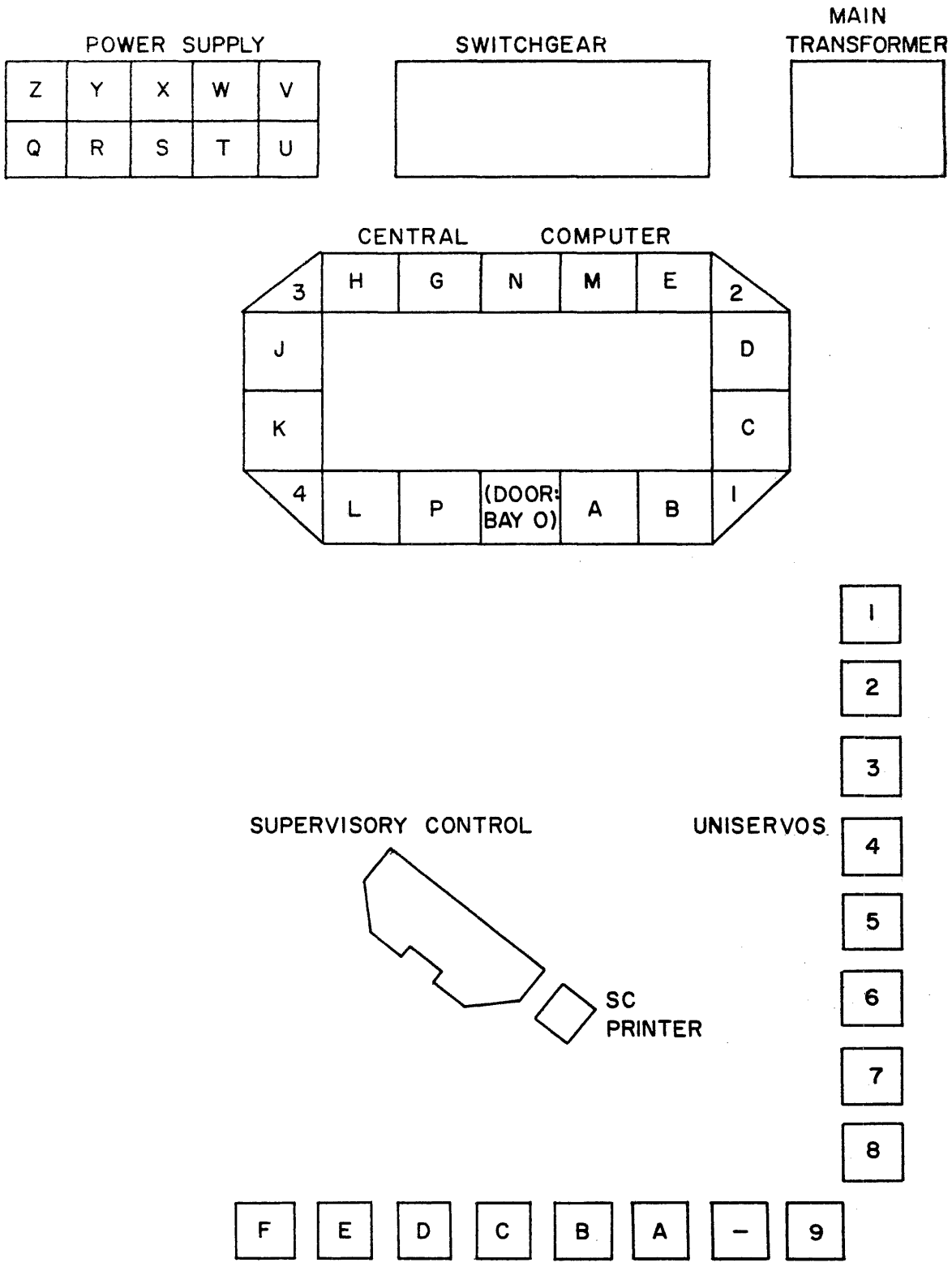

Figure 2-1. Bay Designations of Central Computer Group

TABLE 2-1

PRINCIPAL CIRCUITS IN EACH BAY OF CENTRAL COMPUTER

Bay	Circuits
A	Input and Output Circuits
B	Function Table
C	Function Table; Control Circuits
D	Static Register; Decorders
E	Register M Circuits
M	Register M and Register O Circuits
N	Register M and Register I Circuits
G	HSB & $\overline{\text{HSB}}$; X & $\overline{\text{X}}$; Register I Circuits
H	X & $\overline{\text{X}}$; Cycling Unit
J	L & $\overline{\text{L}}$; F & $\overline{\text{F}}$; A & $\overline{\text{A}}$; Cycling Unit
K	A & $\overline{\text{A}}$; AA & $\overline{\text{AA}}$; Cycling Unit
L	AA & $\overline{\text{AA}}$; Cycling Unit
P	CP & $\overline{\text{CP}}$; Cycling Unit
0	Access door
1	BC Box; FT Neons; Filament Transformers; Bypass Capacitors
2	Filament Transformers; Bypass Capacitors
3	Slow Heater Turn-on Relays; Bypass Capacitors
4	Filament Transformers; Fault Indicators; Maintenance Switches; Power Control Relays; Bypass Capacitors

(Continued from Page 3)

(2) SECTIONS. - The unit chassis bays of the Central Computer are each divided into three sections, designated T, V and X (from top to bottom). The three sections of bays A, B, C, D, H, J, K, L and P, and sections GT and GX, each provide mounting space for 12 conventional chassis, numbered from 1 to 12, and two fixed fuseboards, numbered 13 and 14. A front view of a typical section of this type is shown in Figure 2-2 (a). The three sections of bays E, M and N, and section GV, provide mounting space for 36 printed circuit chassis, numbered from 1 to 36, plus an indicator panel, numbered 37, and a fuseboard, numbered 38. A front view of a typical printed-circuit section is shown in Figure 2-2 (b).

The electrical connections to each section are made at the rear of the section and involve three types of wiring: power wiring, low-speed signal wiring, and high-speed signal wiring. The power wiring handles all a-c and d-c voltages from the Power Supply and Switchgear; the low-speed signal wiring transfers the slow rise-time signal voltages between the chassis, and the high-speed signal wiring transfers the fast rise-time signal voltages. The three types of wiring are described in detail in a later paragraph.

(3) UNITS. - The bays and sections of the Central Computer are composed of a large number of units which are mounted on the framework of the computer and connected by power and signal wiring. The principal unit of the Central Computer is the unit chassis; these chassis contain most of the circuitry of the computer and are of two types: conventional and printed-circuit.

(a) CONVENTIONAL UNIT CHASSIS. - The Central Computer uses a total of 335 conventional unit chassis of 245 different types. A typical conventional chassis is shown in Figure 2-3. The chassis consists of a prepunched aluminum

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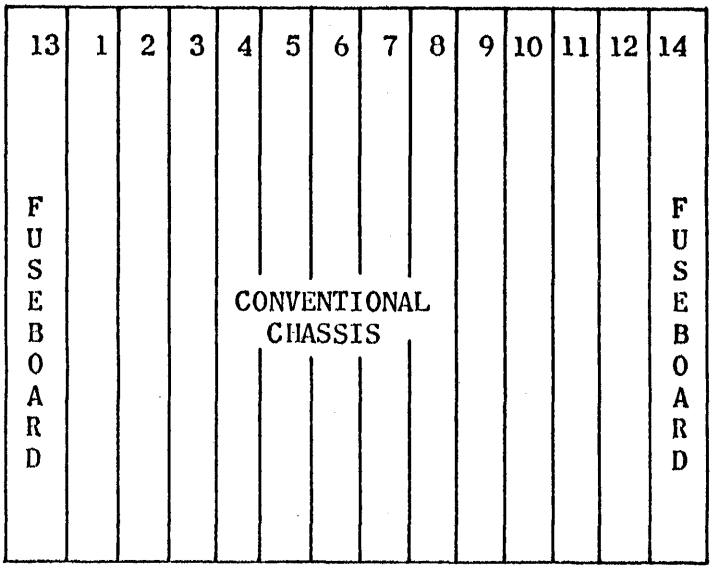
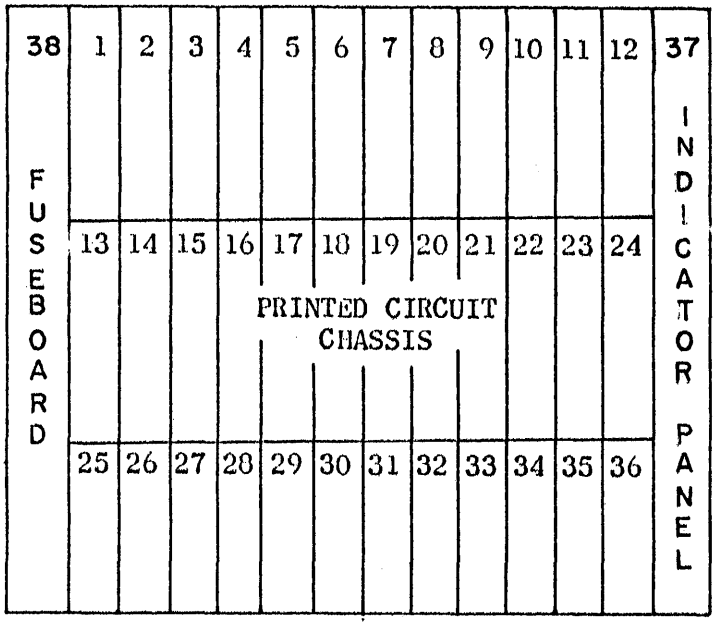


(a) Conventional Section, Front View



(b) Printed Circuit Section, Front View

Figure 2-2 . Typical Sections of Central Computer

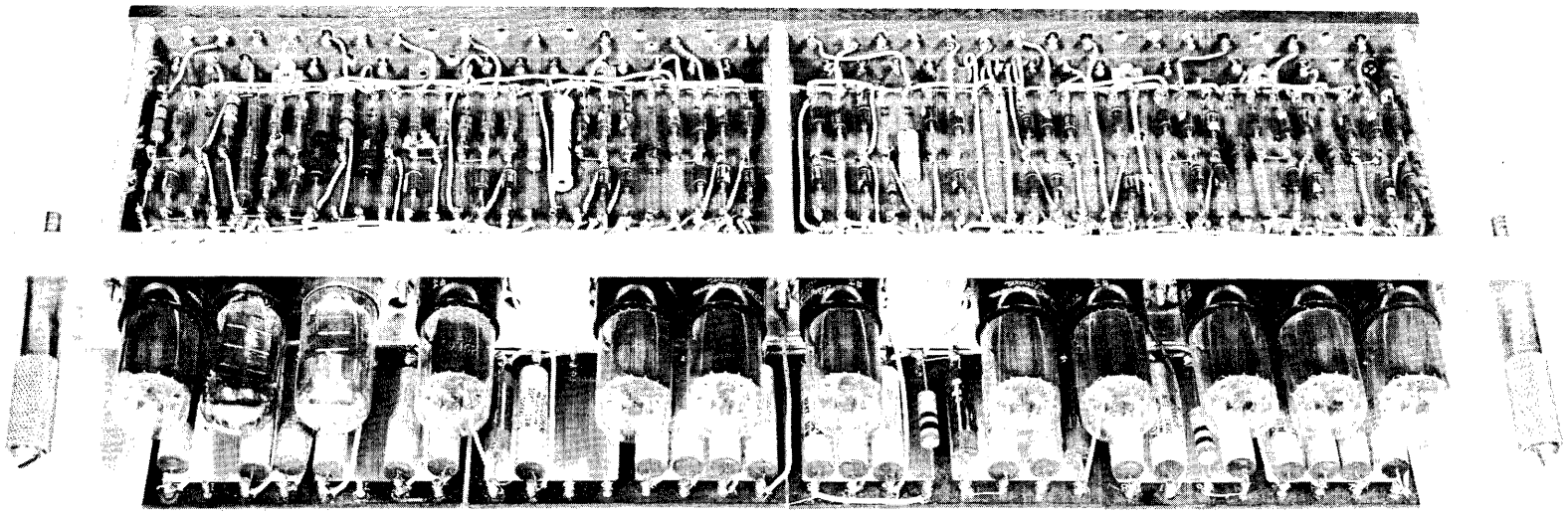


Figure 2-3. Typical Conventional Chassis

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channel with mounting positions for fourteen vacuum tubes. These positions are numbered one to fourteen. Mounted on the channel with 4 1/2 inch spacers is a terminal strip with 87 numbered tapered-contacts. Between the terminal strip and the channel are two component boards, mounted back-to-back. Along each long edge of the boards is a row of 52 mounting lugs, numbered 1 to 52. There may also be lugs along the center line of each board. The three rows of lugs on one board are designated J, H and K, respectively; those on the other are designated M, L and N. Components are mounted between lugs of like number on each board. The small components, such as diodes, are mounted between a center lug and an outer one; the large components, such as resistors and capacitors, are mounted between two outer lugs of like number. The component numbers are derived from their mounting positions: RN42 is a resistor (R), one end of which is connected to lug 42 of row N; CRM18 is a diode (CR), one end of which is connected to lug 18 of row M. Only low-wattage components are mounted on these component boards, since cooling is not effective in this area of the chassis.

The chassis are mounted on the bays in such a position that the vacuum tubes are located directly in the stream of cooling air. A maximum of four additional component boards can be mounted on the tube channel in such a location as to take advantage of the air stream. These additional boards accommodate high-wattage components which must be cooled. The boards are mounted on the right side of the tube channel, perpendicular to the channel. The seven possible locations for the boards are designated A through G.

Each external component board has two rows of 8 lugs. The lugs in one row are numbered 1 through 8; those in the other row are numbered 11 through 18. The components are mounted between corresponding lugs in each row; the component numbers are derived from the mounting positions, with the number of the outer

lug usually assigned to the component. As an example, RC12 is the resistor (R) connected between lugs 2 and 12 of component board C.

When the chassis is in position within the bay, the lugs of the external component boards are accessible for use as test points for meter and scope readings. Many important signals, such as gate and flip-flop outputs, appear on the test terminals. The test terminals are called out on the schematic diagrams, and circuit diagrams and the associated component board and lug numbers are also identified. (Example: TT E15 is lug 15 of component board E of a unit chassis.)

The tapered contacts of the terminal strip of each unit chassis mate with receptacles mounted on the section backboard of the computer. In order to identify each chassis of the Central Computer and to prevent its insertion into a wrong location, a system of coded key pins and holes is used. The key pins are mounted in the chassis terminal strip while the holes are contained in the section backboards. The location of the key pins and holes on a chassis is shown in Figure 2-4. The codes for all the chassis of the Central Computer is listed on Drawing XD142410. Just ahead of the number one terminal of the backboards are alphabetic positions, one for each bay plus S for Servo and T, V and X to designate the sections. At the other end of each backboard are 12 numerical positions where the chassis number is specified. Thus, a chassis with holes in positions B, T and 12 can be mounted only in the position whose pins are spaced accordingly. Duplicate chassis are exceptions to this rule.

Double-width chassis are used in the Central Computer when it is necessary to mount components which will not fit on a single-width chassis. The following chassis are double-width: A1&2T, A1&2X, B1&2X, C10&11TX, D11&12TX, H3&4V, and P3&4V.

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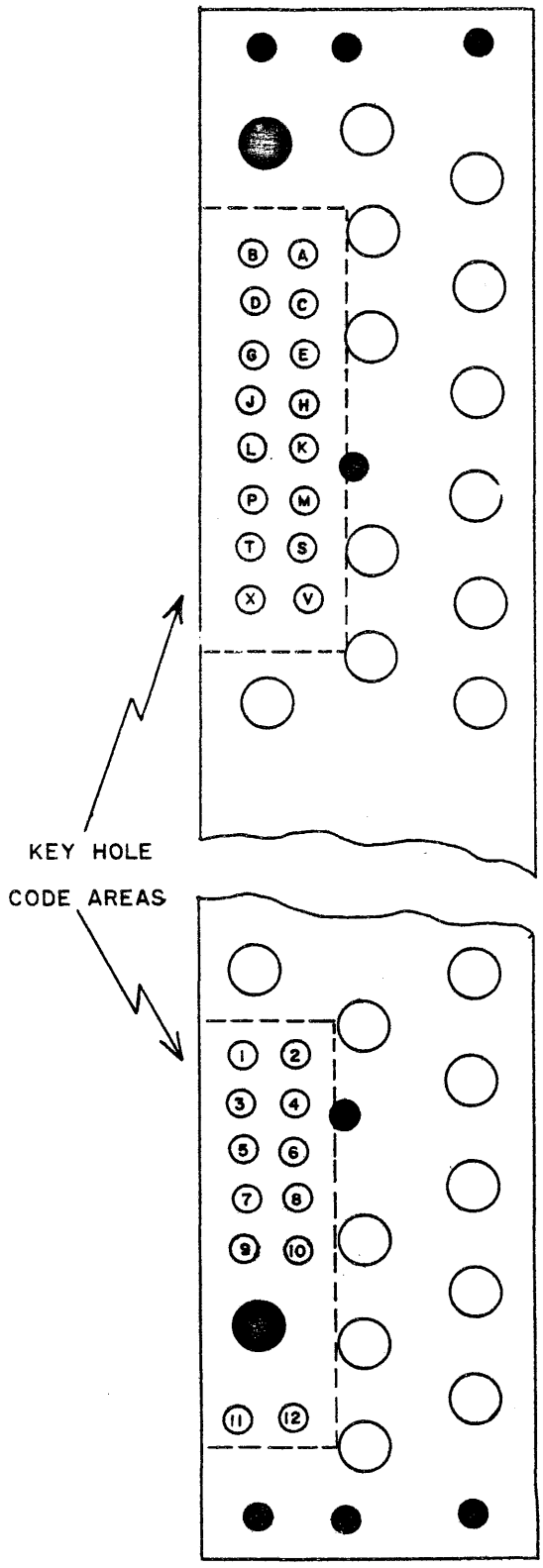

(BOTTOM VIEW OF CHASSIS TERMINAL BOARD)

Figure 2-4. Location of Key Holes on the Conventional Chassis

(Continued from Page 10)

(b) PRINTED CIRCUIT CHASSIS. - The Central Computer uses a total of 310 printed circuit chassis of 29 different types. A typical printed-circuit chassis is shown in Figure 2-5. A prepunched channel has mounting positions for four or five vacuum tubes. The printed circuit board is mounted perpendicular to the channel. The printed wiring is on one side of the board, while the components are mounted on the other. A 33 pin connector is mounted at the end of the printed-circuit board which is opposite the tube channel. This connector mates with the appropriate jack mounted on the section backboard.

(c) OTHER UNITS OF THE CENTRAL COMPUTER. - The units of the Central Computer, other than the unit chassis which were described in the preceding paragraphs, are listed in Table 2-2. The designation of each unit is provided in the table, along with a short description of the unit. (Continued on Page 22)

TABLE 2-2. UNITS OF CENTRAL COMPUTER

Unit	Designation	Description
Fuseboards	The left-hand and right-hand fuseboards of sections T, V and X of bays A,B,C,D,H,J,K L,P and sections GT and GX are designated as units 13 and 14, respectively. The fuseboards of sections T, V and X of bays E, M and N and section GV are designated as unit 38. The six additional fuseboards of bay P, which are mounted along the side nearest the access door, are designated as units 15 and 16 (in each section). (The complete designation of each fuseboard consists of the unit designation preceded by the bay designation and followed by the section designation.)	Each fuseboard contains 26 pairs of terminals, numbered from 1 to 26. The input terminals are labeled F and the output terminals are labeled W. Thus A13T-F25 is the input terminal of fuse-position 25 of fuseboard A13T. A center terminal, labeled Q, is also available for the alarm contacts of grasshopper fuses. Each fuseboard has a plastic cover to prevent personnel from coming in contact with the voltages. When the cover is properly in place, terminals 27 and 28 of the fuseboard are connected together. These terminals are wired into the interlock circuit of the Central Computer.

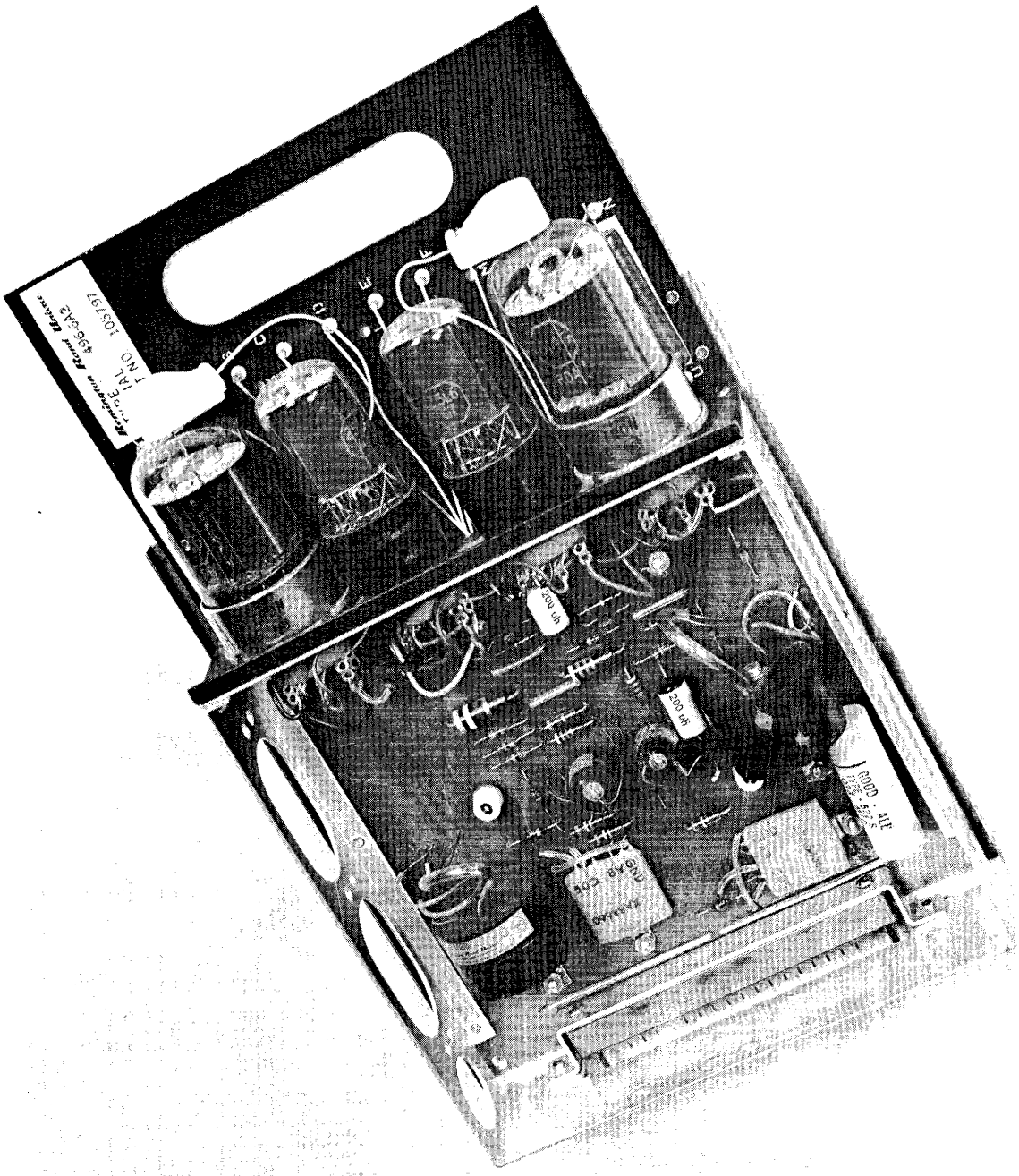

Figure 2-5. Typical Printed Circuit Chassis

TABLE 2-2. UNITS OF CENTRAL COMPUTER (Cont'd)

Unit	Designation	Description
Indicator Panels	The indicator panels of sections T, V and X of bays E,M,N and section GV are designated as unit 37. (The complete designation consists of the bay; unit, and section designations, in that order.)	Each indicator panel provides mounting for 23 indicator lights and a 33-pin connector (containing test terminals).
Jones Plugs	All Jones plugs are designated as unit J. The complete identification of a plug consists of the unit designation preceded by the bay designation and followed by a letter (A-Z) or a number 1-9) which identifies the particular plug within the bay.	Most of the Jones plugs have 33-pins; the protective rectifiers, however, are connected to the fuseboards via 12-pin and 18-pin Jones plugs.
Bypass and Cable Termination Boards	The boards at the top of each section are designated as unit U, those at the bottom as unit V. The layer position of the board is indicated by a digit (1-3) following the unit designation. The row position of the board is designated as A,B,C, or D, from left to right. This letter follows the layer designation.	(Refer to Figure 2-6.) The bypass and cable termination boards provide mounting space for the bypass capacitors for d-c inputs and for terminating networks for coaxial cables. The boards are identical to the external component boards of the unit chassis. The boards at the top of section T and the bottom of section X are mounted at right angles to the backboard and are in one layer, designated "1". The boards at the bottom of section T, the top and bottom of section V and the top of section X are mounted parallel to the backboard in three layers, the layer closest to the backboard is layer "1", the center layer is "2" and the outer layer is "3". (Note: The 3 layers on adjacent sections are staggered to permit interspacing the bypass boards.) The boards are mounted in horizontal rows within each section. The position of the boards in the rows are indicated as A,B,C or D, from left to right.

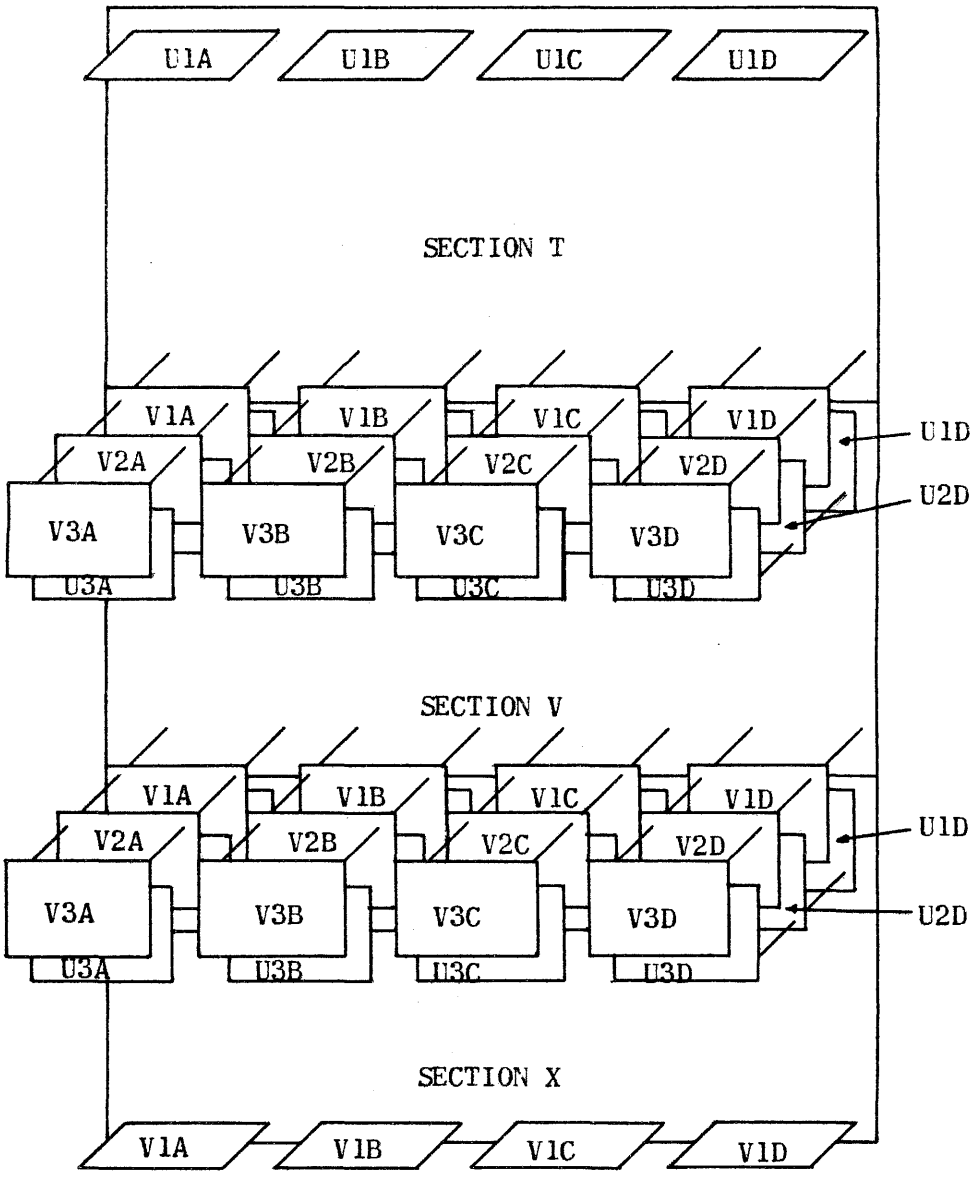

Figure 2-6 . Bypass Board Locations

TABLE 2-2. UNITS OF CENTRAL COMPUTER (Cont'd)

Unit	Designation	Description
Section Edge Terminal Boards (Sections T,V and X of bays A,B,C,D,H,J,K, L and P, and sections GT and GX).	The section edge terminal boards at the top of the conventional sections are designated A1, A2 and A3, from right to left facing the backboards. The terminal boards at the bottom of those sections are designated D1, D2 and D3, those on the left side K and M, from top to bottom, and those on the right side G and J.	(Refer to Figure 2-7.) The sections-edge terminal boards provide tie points for the high-speed wiring as it passes from one section to another. The boards at the sides of the sections have two rows of 16 terminals each. The terminals are numbered 1 through 32. The boards at the bottom of the sections have one row of 16 terminals, designated 17 through 32.
Section Edge Connectors (Sections T,V and X of Bays E,M and N, and Section GV)	The three connectors mounted along the left edge of the section backboard are designated K,L and M, from top to bottom; those along the right edge are designated G, H and J.	(Refer to Figure 2-8) Each connector is built up of strips of twenty pin connectors. The number of connections available at each location is listed in Table 2-3.
Commoning Strips	The commoning strips on the backboards of sections T, V and X of bays E, M and N, and section GV are designated A,B,C and D from top to bottom.	(Refer to Figure 2-8) Each commoning strip has four horizontal rows of 54 terminals each. The four terminals in each vertical row are electrically connected.
Transformers	Y1, Y2, ... Y61	Only the externally-mounted filament transformers are included in this group; all others are considered a part of the unit on which they are mounted.
Relays	R1, R2, ...	Only the externally-mounted relays are included in this group; all others are considered a part of the unit on which they are mounted.

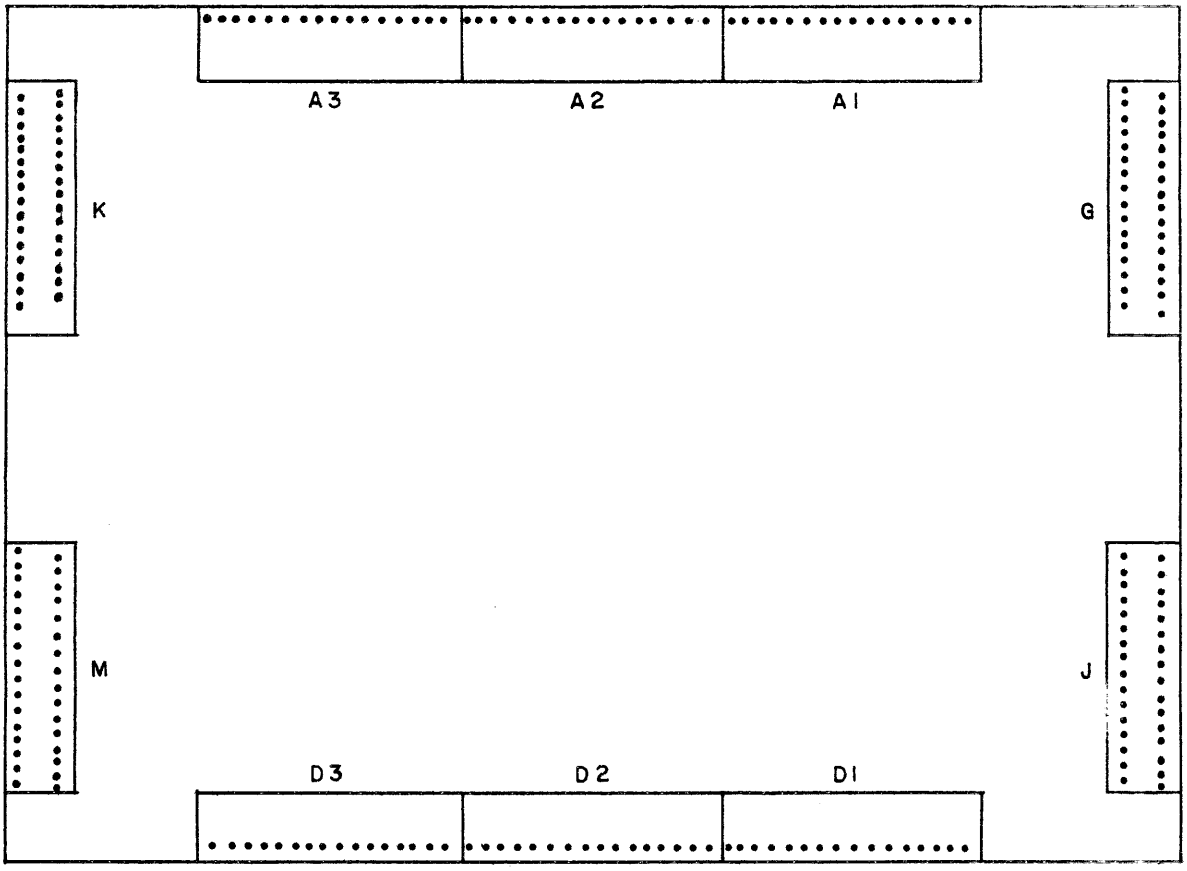

Figure 2-7. Section Edge Terminal Boards
(Bays A,B,C,D,GT,GX,H,J,K,L and P)

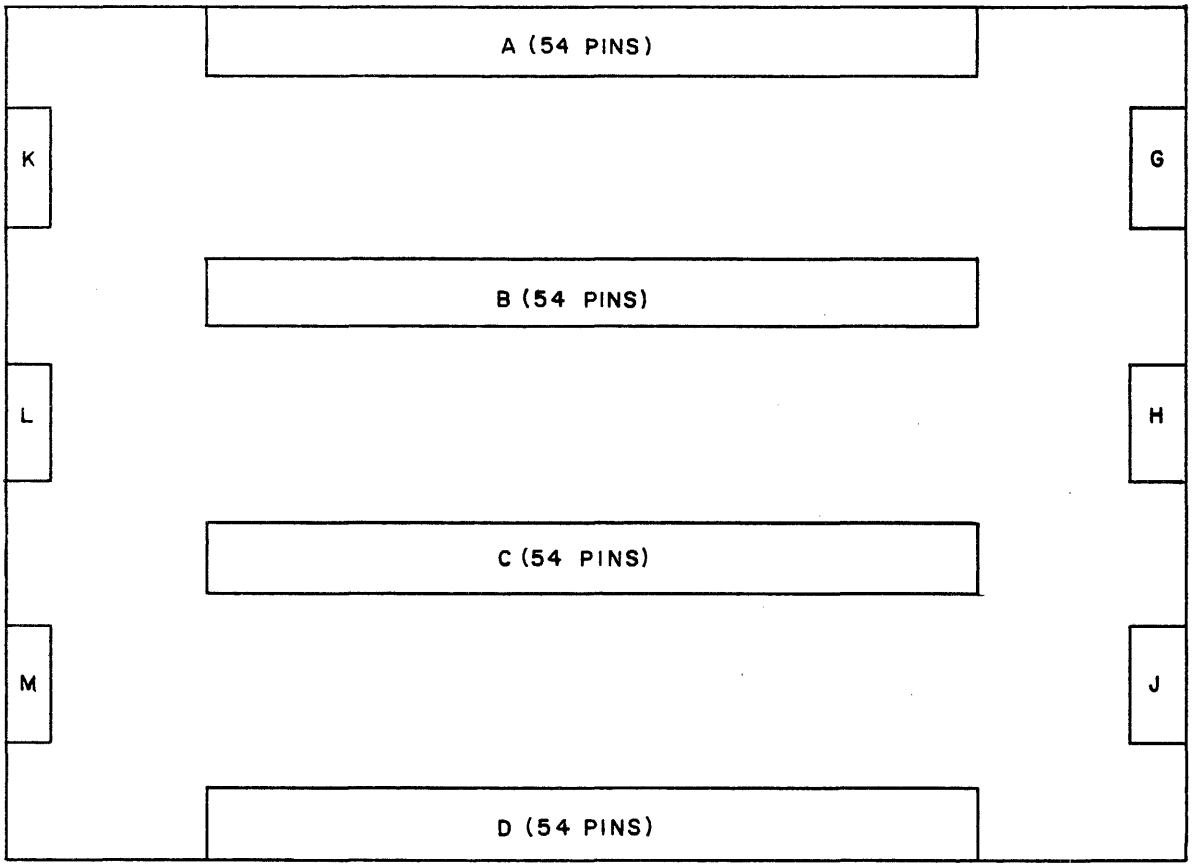

Figure 2-8. Section Terminal Boards (Bays E, M, N and GV)

TABLE 2-3

SECTION EDGE CONNECTIONS; BAYS E, M, N AND GV

Bay	Location	Connectors Available
ET	G	40
	H	-
	J	40
	K	20
	L	40
	M	40
EV	G	40
	H	20
	J	40
	K	20
	L	40
	M	40
EX	G	40
	H	-
	J	40
	K	40
	L	80
	M	20
MT	G	20
	H	40
	J	40
	K	120

TABLE 2-3

SECTION EDGE CONNECTIONS; BAYS E, M, N AND GV (Cont'd)

Bay	Location	Connectors Available
MT	L	140
	M	120
MV	G	40
	H	80
	J	20
	K	40
	L	20
	M	20
MX	G	40
	H	80
	J	20
	K	40
	L	20
	M	20
NT	G	100
	H	120
	J	120
	K	-
	L	-
	M	40
NV	G	80
	H	40

TABLE 2-3

SECTION EDGE CONNECTIONS; BAYS E, M, N AND GV (Cont'd)

Bay	Location	Connectors Available
NV	J	40
	K	40
	L	60
	M	60
NX	G	40
	H	20
	J	20
	K	20
	L	-
	M	20
GV	G	40
	H	60
	J	60
	K	-
	L	-
	M	-

(Continued from Page 12)

c. POWER DISTRIBUTION

(1) GENERAL. - Univac II system power is derived from a 3-phase, 60-cycle, 480 vac, 240 vac or 208 vac source depending upon installation site provisions. Line power enters the system through the main circuit breaker CB101, and thence is dispersed to the various sections of the equipment. The power system is comprised of four units: the Main Transformer, the Switchgear, the Motor-Generator Set and the Power Supply. The arrangement of these elements depends upon the type of line power available (see Section 8). Essentially; the Main Transformer provides for 440v when 208v or 240v line power is supplied or 208v when the line power is 440v, the Switchgear supplies the equipment a-c requirements, the Motor-Generator Set provides 400-cycle, 208 vac to the Power Supply primaries, and the Power Supply provides the d-c voltages needed by the system.

Generally, a total of nine conduits, ranging in size from 3/4 inch to 4 inches and designated A through I, distribute the power wiring between the units of the Central Computer group. A graphic presentation of the general interconnections between the units is shown in drawing 128907. Variation to this pattern necessary for the different serials is found on the print for the particular computer.

(2) DESIGNATION OF PRIMARY POWER LINES. - Power entering the computer system is described by the phase, Ø1, Ø2, Ø3, of the line on which it enters. The a-c lines within the equipment retain the basic phase number of the source line from which they are derived, but with additional notation to identify the particular circuits involved. Usually the nomenclature changes when the power line passes through some control element, e.g., a circuit breaker. The first two characters in the identification pertain to the phase line with which the line is associated; the succeeding characters isolate the particular line.

The exception to this type of call-out are the outputs from the alternators of the Motor-Generator Set. The 3-phase output of Alternator A is described ØA1, ØA2 and ØA3; the output of Alternator B is ØB1, ØB2 and ØB3. A pictorial presentation of the power system in which the primary power lines are noted is presented in Figure 2-9. Table 2-4 indicates the destination of the various primary a-c lines.

(3) INTERCONNECTING CABLES AND CABLE TERMINATIONS. - Two cables bring a-c and d-c power to the Central Computer from the Power Supply and Switchgear. Conduit "F", a 104-wire cable, carries all voltages and signals which originate at the Power Supply; conduit "E", a 48-wire cable, carries all voltages and signals which originate at the Switchgear.

The origins and terminations of the wires in Conduits "E" and "F" are shown in the drawing entitled "Interconnecting Cables, Univac II" supplied in the computer installation. The principal terminating point of the wires is at the Quadrangle (bay Q of the Central Computer). However, certain wires of conduit "E" terminate at terminal boards PT7 and PT8, and fuseboards PT16 and PV16, of bay P, and at the BC corner fuseboard.

(4) QUADRANGLE. - The Quadrangle is located under a removable floor panel just inside the entrance door of the computer. The Quadrangle, shown in Figure 2-10, consists of ten terminal strips, designated QT1 through QT10. QT1, QT2, QT9 and QT10 have 11 terminals each, while the remaining strips have 17 terminals each.

The output leads from the Quadrangle are connected to the barrier strips of bay Y and the fuseboards of bay P through the power harness which encircles the base of the computer. The connections are listed on 106192 (Base Harness and Bay "P" Fuseboard Assembly - Wired); sheets 1 through 5, of this manual.
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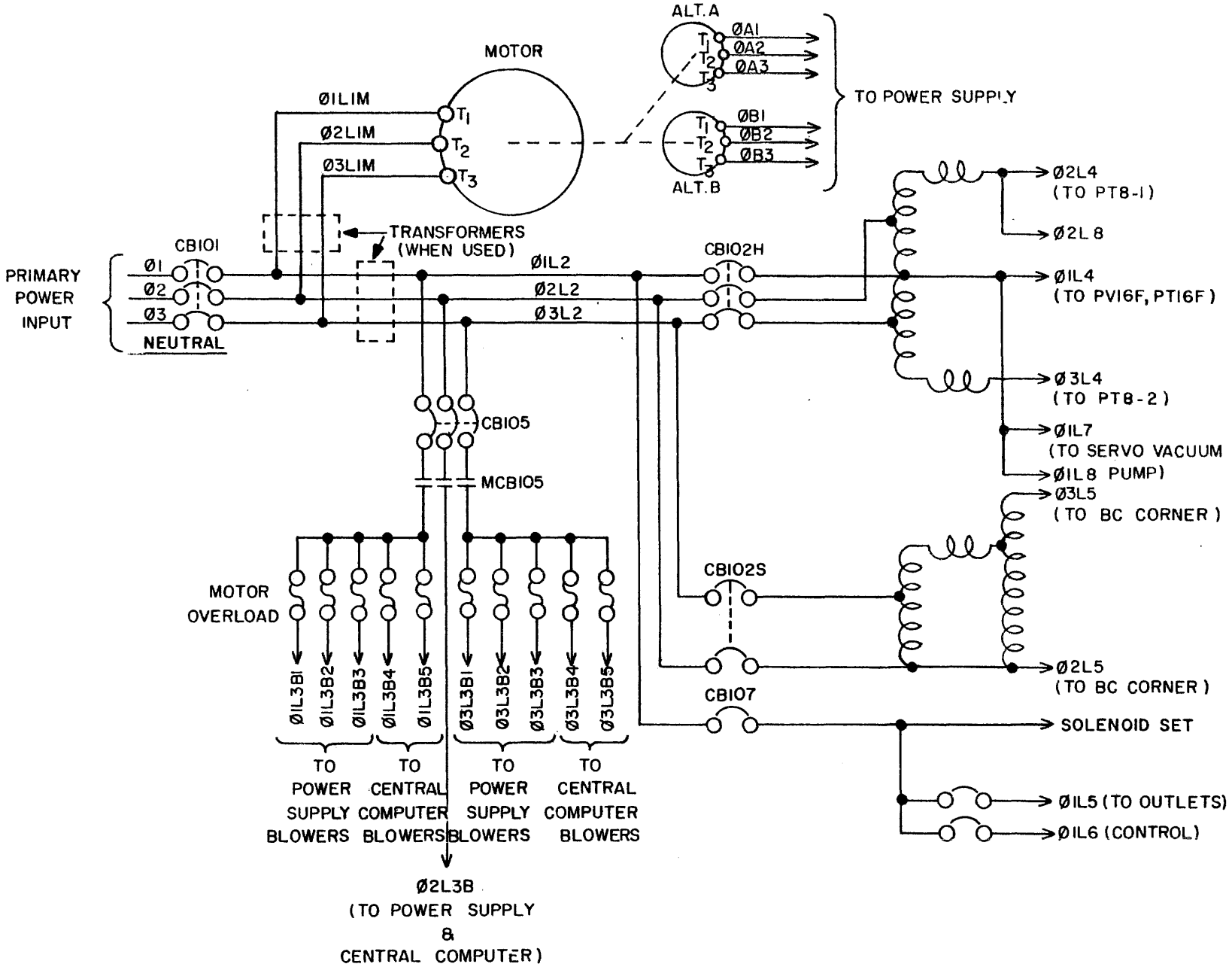


Figure 2-9. Designations of Primary Power Lines

TABLE 2-4. PRIMARY POWER DISTRIBUTION

Voltage	Origin	Destination
Ø2L5	Switchgear (CB1025)	BC Corner Fuseboard
Ø3L5	Switchgear (T104)	BC Corner Fuseboard
Ø1L6B	Switchgear (CB104)	QT10-2; LT7-9
Ø1L6SB	Switchgear (RP24)	QT10-3; LT7-4
Ø1L6A	Switchgear (CB102H)	PT7-8
Ø1L6	Switchgear (Control Power Switch)	QT10-1; LT7-1
Ø2L3B1	Switchgear (CB105)	QT7-15; PX15-F14
Ø1L5	Switchgear (CB107)	QT9-11, AT6-6, PT6-6, MT6-8, OJK-2
Ø2L4M	Switchgear (T101)	QT10-5; PX16-W8
Ø1L7 & 8	BC Corner	Uniservos
Ø1L4	Switchgear (CB102H)	PV16F; PT16F, BC Corner
Ø1L4	Switchgear (T101)	QT10-6; PT16-W26
Ø3L3B4	Switchgear (CB105)	QT7-9; PX15-F20
Ø3L3B5	Switchgear (CB105)	QT7-10; PX15-F22
Ø1L3B4	Switchgear (CB105)	QT7-11; PX15-F8
Ø1L3B5	Switchgear (CB105)	Qt7-12; PX15-F10
Neutral	Neutral Bus	QT10-10; AT6-7, PT6-7, MT6-9; OJB-15
AØA1(Ø1L1)	Power Supply	QT8-1; LJH-25
AØA2(Ø1L2)	Power Supply	QT8-2; LJH-26
AØA3(Ø1L3)	Power Supply	QT8-3; LJH-27
AØB1(Ø2L1)	Power Supply	QT8-4; LJH-28
AØB2(Ø2L2)	Power Supply	QT8-11; LJH-20
AØB3(Ø2L3)	Power Supply	QT8-12; LJH-21

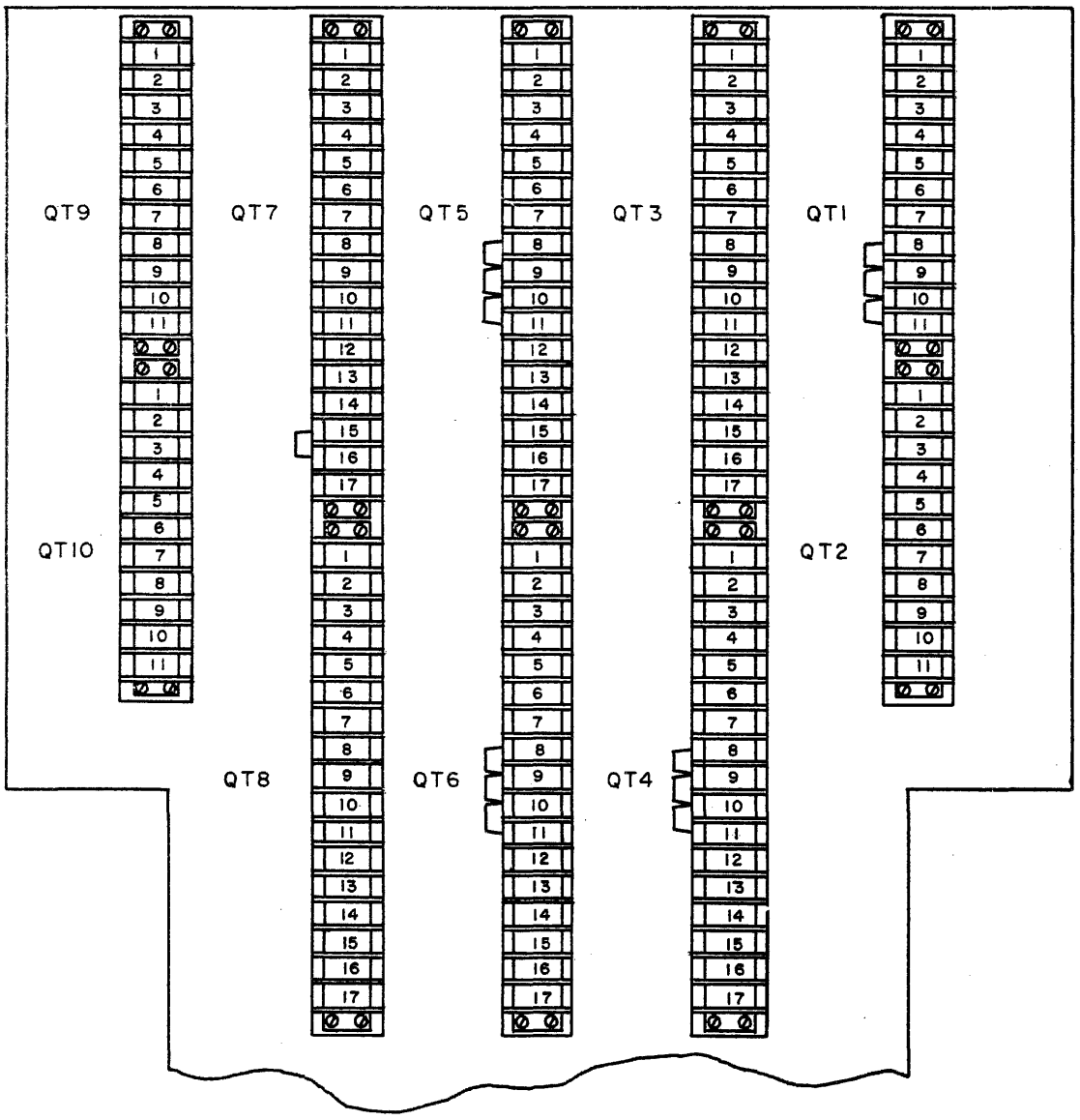


Figure 2-10. Quadrangle (Bay Q of Central Computer)

(Continued from Page 23)

(5) POWER HARNESS AND BARRIER STRIP RING. - The Power Harness and Barrier Strip Ring (bay Y of the Central Computer) distribute the voltages from the Quadrangle to the bays of the Central Computer. The output leads from the Quadrangle are bound into a cable, called the Power Harness. This harness, shown in Figure 2-11, completely encircles the base of the computer, delivering to barrier strips, Figure 2-12, at the bottom of each bay whatever voltages are required within that bay.

The barrier strip ring consists of six 13-pin terminal strips (designated YT1 through YT6) at the bottom of each bay, a 13-pin strip (designated LT7) at the bottom of KL Corner, a 17-pin strip (designated PT7) at the top of bay P, and a 33-pin Jones plug (designated 2J1) at the bottom of bay 2.

(6) FILAMENT POWER (Reference: Drawing XR106192-Modified Tray Assembly Wired). - The filament power for the Central Computer is supplied by three 230-volt lines from the Switchgear, designated as follows: Ø1L4, Ø2L4 and Ø3L4. The Ø1L4 line is connected directly to the F terminals of fuseboards PT16 and PV16. The Ø2L4 and Ø3L4 lines are connected to the F terminals of fuseboards PT15 and PV15, respectively, via the filament-dropping resistors of bay I. (Refer to Figure 2-13.)

Three contactors in the HJ corner (bay 3) control the connection of the filament-dropping resistors into the filament circuits. These contactors, in turn, are controlled by the #2, #3 and #4 contactor control signals from the Switchgear. These signals are applied to the contactors in succession, separated from each other by a variable time interval of from 0 to 1 minute. Initially, Ø2L4 and Ø3L4 are reduced to approximately 50% of full voltage by two parallel resistors in each line. The #2 control signal closes the #2 contactors, thus connecting a third resistor into each line and increasing the filament voltages to approximately 66% of full value. The #3 control

(Continued on Page 31)

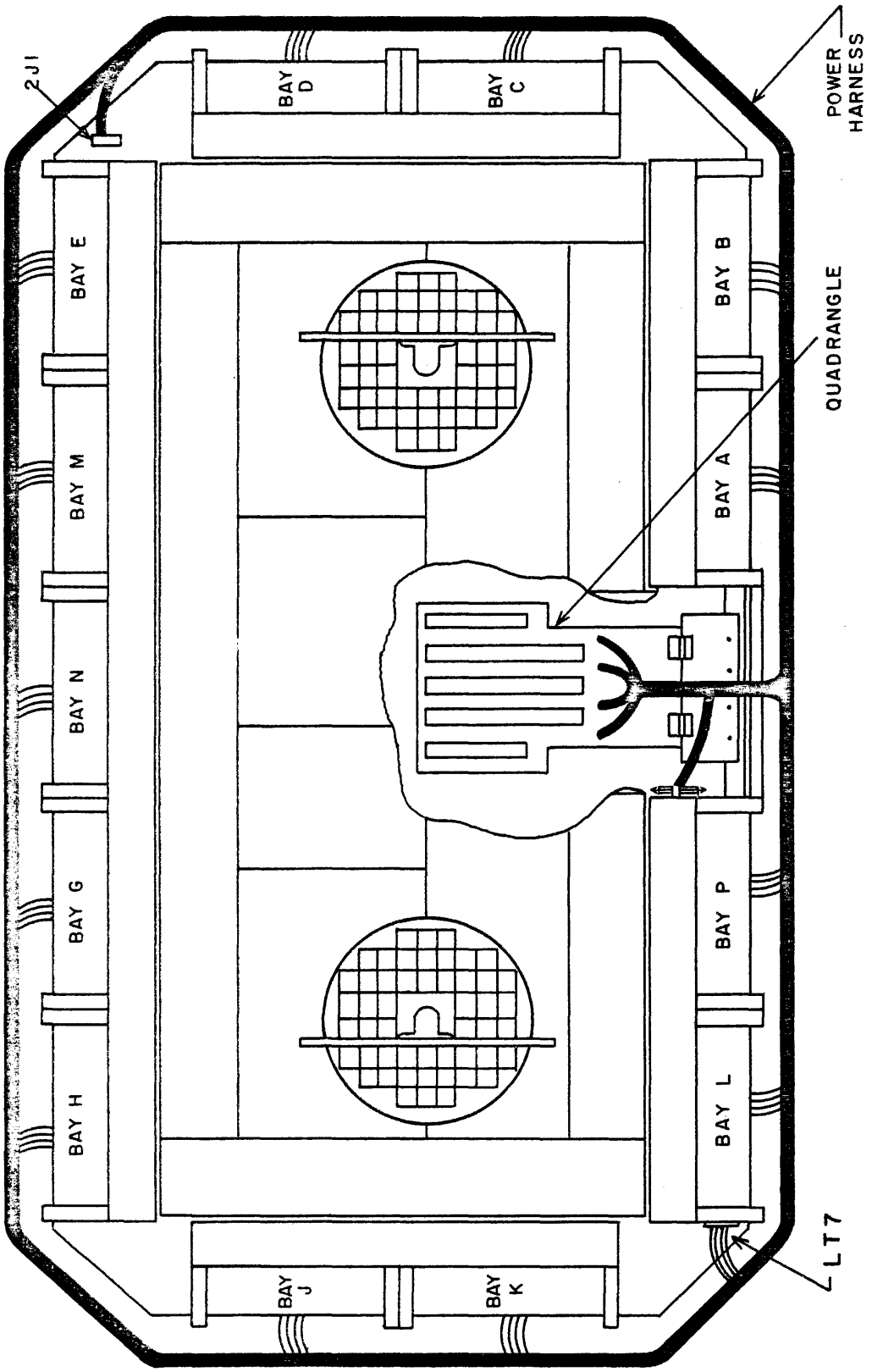


Figure 2-11. Power Harness at Base of Central Computer

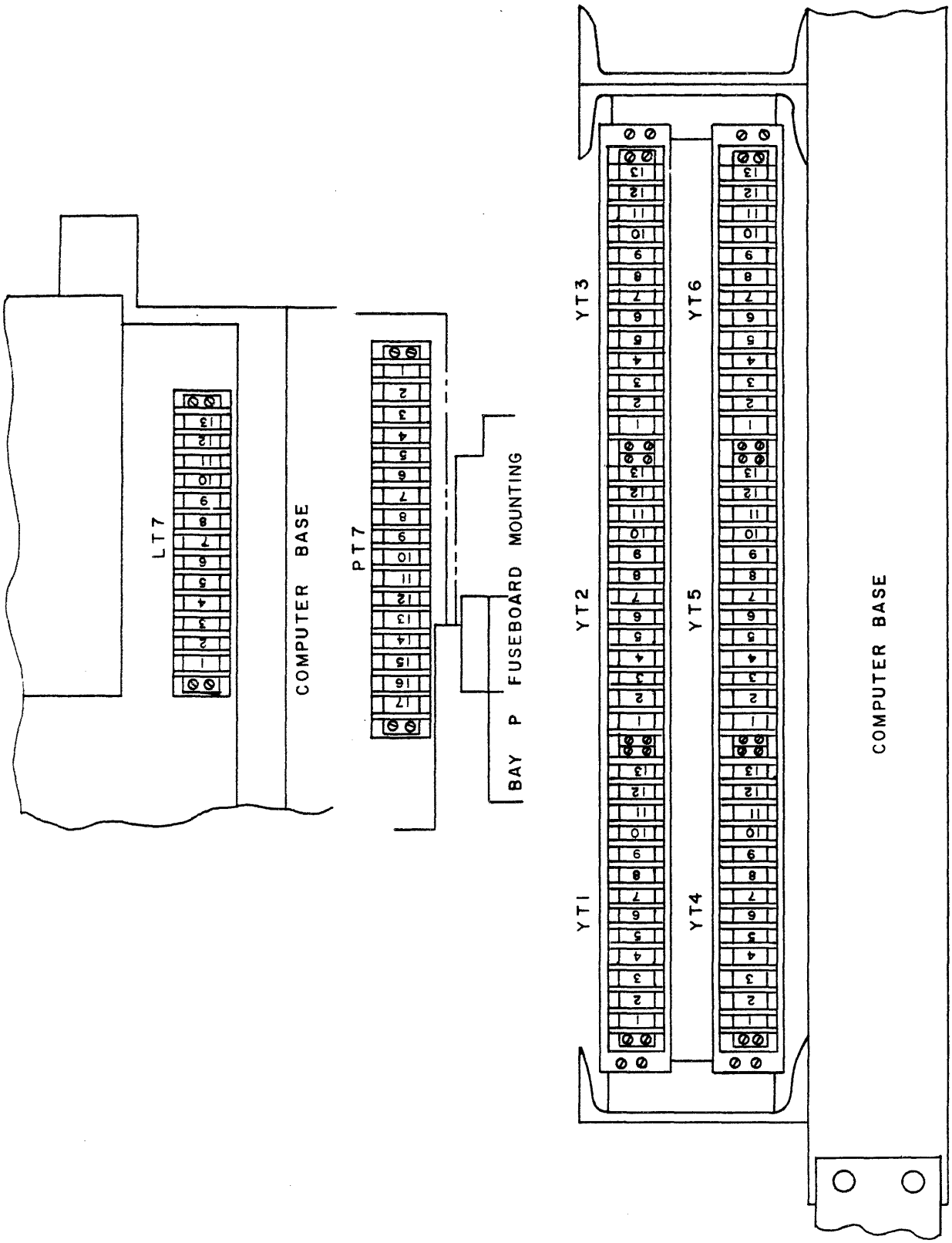


Figure 2-12. Barrier Strips of the Central Computer

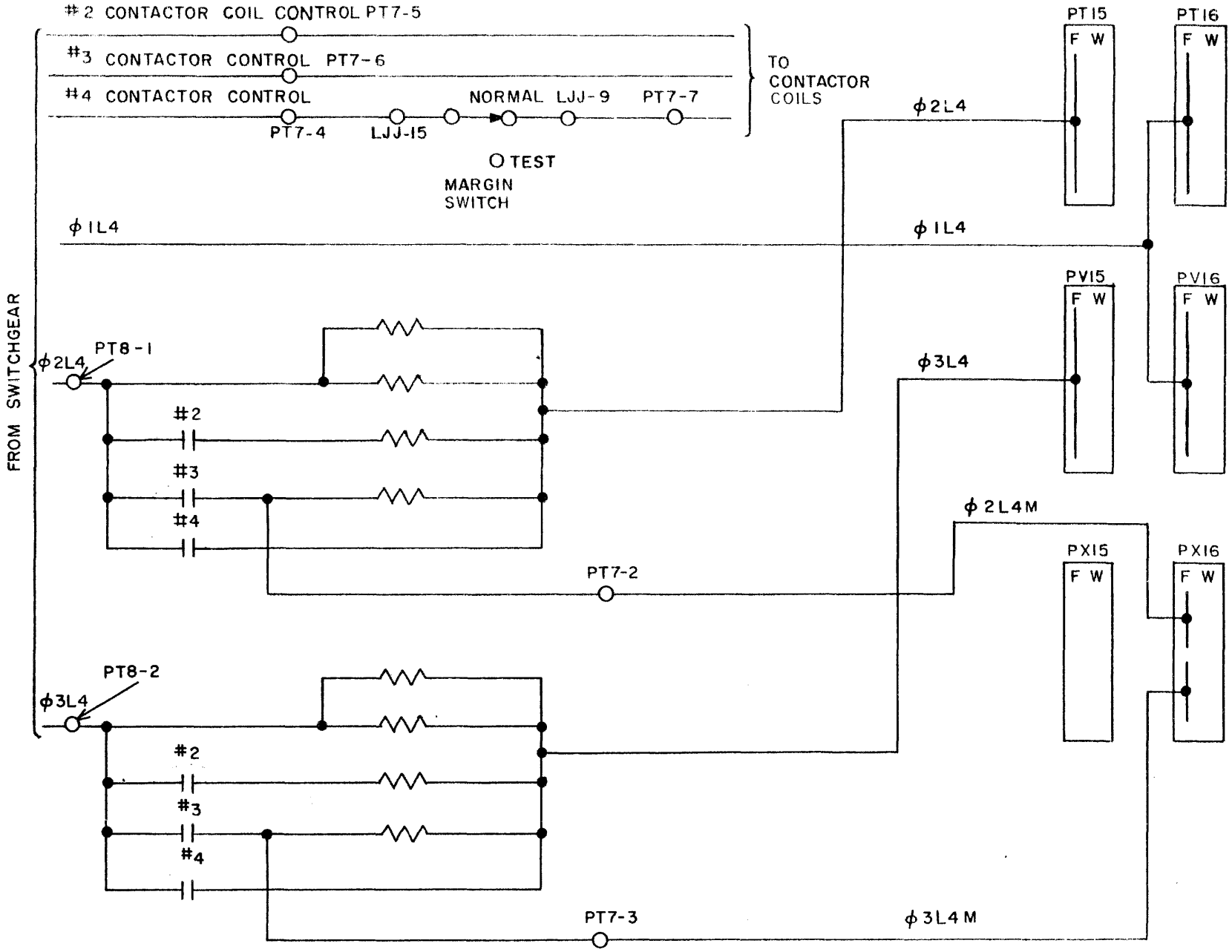


Figure 2-13. Filament Power Distribution to Bay P Fuseboards

(Continued from Page 27)
signal closes the #3 contactors, thus connecting a fourth resistor into each line and increasing the filament voltage to approximately 85% of full value. The #3 contactors also apply Ø2L4 directly to F terminals 1 through 10 of fuseboard PX16 and Ø3L4 directly to F terminals 21 through 26 of that fuseboard. The #4 control signal closes the #4 contactors, which bypass the voltages around the resistors and apply full voltage to fuseboards PT15 and PV15.

The W terminals of fuseboards PT15, PT16, PV15, PV16, and PX16 are connected to the T6 barrier strips at the bottom of the bays by heads which are routed through the power harness. The wiring connections between the fuseboards and the barrier strips are listed on 129031 (Base Harness and Bay P Fuseboards), sheets 6, 7, 8, 9 and 11.

The heater transformers are mounted on the channels between the bays of the computer. The locations and type designations of the transformers are shown in Figure 2-14. There are six mounting positions on each channel (except the channels between bays E, M, N and G), two above the access door, and nine above bays E, M, N and G. The transformers are numbered consecutively from top-to-bottom around the computer, starting from bay A.

The connections between the T6 barrier strips and the primary windings of the heater transformers are shown in the Bay Assembly Wiring Diagrams, supplied with the computer. In general, terminals 10 through 13 of the T6 barrier strips are reserved for the heater transformer lines. Ø1L4 and Ø2L4 are applied to the primary windings of the transformers of bays A, B, C, D, E and M; Ø1L4 and Ø3L4 are applied to the primary windings of the transformers of bays N, G, H, J, K, L and P.

The 13 different types of filament transformers provide heater voltages for all the different tubes of the computer. The voltages are designated by

the letter H, followed by an alphabetic code letter. The heater voltages, along with the code representation of each, are shown in Figure 2-15. In order to minimize the possibility of heater-to-cathode arcing, all heater voltages are tied to d-c potentials which are close to the associated cathode potentials.

A typical filament voltage wiring scheme is shown in Figure 2-16. The H_J output of transformer Y_5 is connected to the input (F) terminals of fuses 15 and 7, respectively, of fuseboards A13V and A13X. The output terminals of those fuses and the H_L output of the transformer are connected across the appropriate filaments of chassis A3V, A4X, A5X, A6X, A7X, A8X, A9X, A10X, A11X and A12X. The H_L output is also connected to the W terminal of the "grasshopper" fuse in the -74V line, thus establishing the required d-c reference potential.

(7) D.C. VOLTAGES. - The Central Computer receives 79 d-c voltages from the Power Supply via conduit "F", which connects the output terminals of the Section Q fuse panel assembly to the Quadrangle of the computer. The complete list of d-c voltages, along with the origin and destination of each, is provided in Table 2-5.

The d-c voltages are distributed to the barrier strips below the bays by means of the power harness. The connections between the Quadrangle and the Barrier Strip Ring are shown on 129031 (Base Harness and Bay P Fuseboard Assembly, Wired), sheets 1 through 5. The voltages on the barrier strips are arranged in descending order of magnitude, from left to right, in order to minimize the difference in potential between adjacent terminals. The upper strips (YT1, YT2 and YT3) contain positive voltages and low-value negative voltages. The lower strips (YT4 and YT5) continue the sequence from

(Continued on Page 41)

BAY-M		BAY-E		BAY-D		BAY-C		BAY-B		BAY-A		
		Y15 BT-89 -11	Y9 BT-104 -1				Y1 BT-89 -22			Y60 BT-93 -1	Y61 BT-104 -4
		Y16 BT-89 -14	Y10 BT-90 -6				Y2 BT-89 -23			MOUNTED ABOVE DOOR	
		Y17 BT-89 -26	Y11 BT-89 -27				Y3 BT-98 -2			BAY-0	
		Y18 BT-89 -16	Y12 BT-89 -15				Y4 BT-94 -1			-DOOR-	
		Y19 BT-94 -2	Y13 BT-95 -3			Y7 BT-90 -7	Y5 BT-89 -10				
		Y20 BT-95 -1	Y14 BT-105 -1			Y8 BT-95 -2	Y6 BT-105 -4				

KEY:
TABCODE TRANSFORMER TYPE AND NUMBER

Y00
BT-00 -0

Y51	Y52	Y53	Y54	Y55	Y56	Y57	Y58	Y59
BT-300 -8	BT-300 -7	BT-300 -6	BT-300 -5	BT-300 -4	BT-300 -3	BT-300 -2	BT-300 -1	BT-300 -9

BAY-P		BAY-L		BAY-K		BAY-J		BAY-H		BAY-G		BAY-N	
	Y45 BT-89 -1		Y39 BT-90 -2		Y32 BT-90 -8				Y21 BT-89 -21				
	Y46 BT-91 -1		Y40 BT-89 -7		Y33 BT-89 -9				Y22 BT-100 -1				
	Y47 BT-89 -3	Y47A BT-174 -4	Y41 BT-89 -5		Y34 BT-95 -4		Y28 BT-90 -3		Y23 BT-89 -25				
	Y48 BT-90 -1		Y42 BT-89 -4		Y35 BT-91 -3		Y29 BT-89 -19		Y24 BT-94 -3				
	Y49 BT-89 -6		Y43 BT-89 -8		Y36 BT-89 -18	Y37 BT-174 -5	Y30 BT-99 -1		Y25 BT-89 -24	Y26 BT-174 -4			
	Y50 BT-89 -2		Y44 BT-91 -2		-38 BT-89 -17		Y31 BT-89 -20		Y27 BT-104 -2				

Figure 2-14. Locations and Designations of Heater Transformers

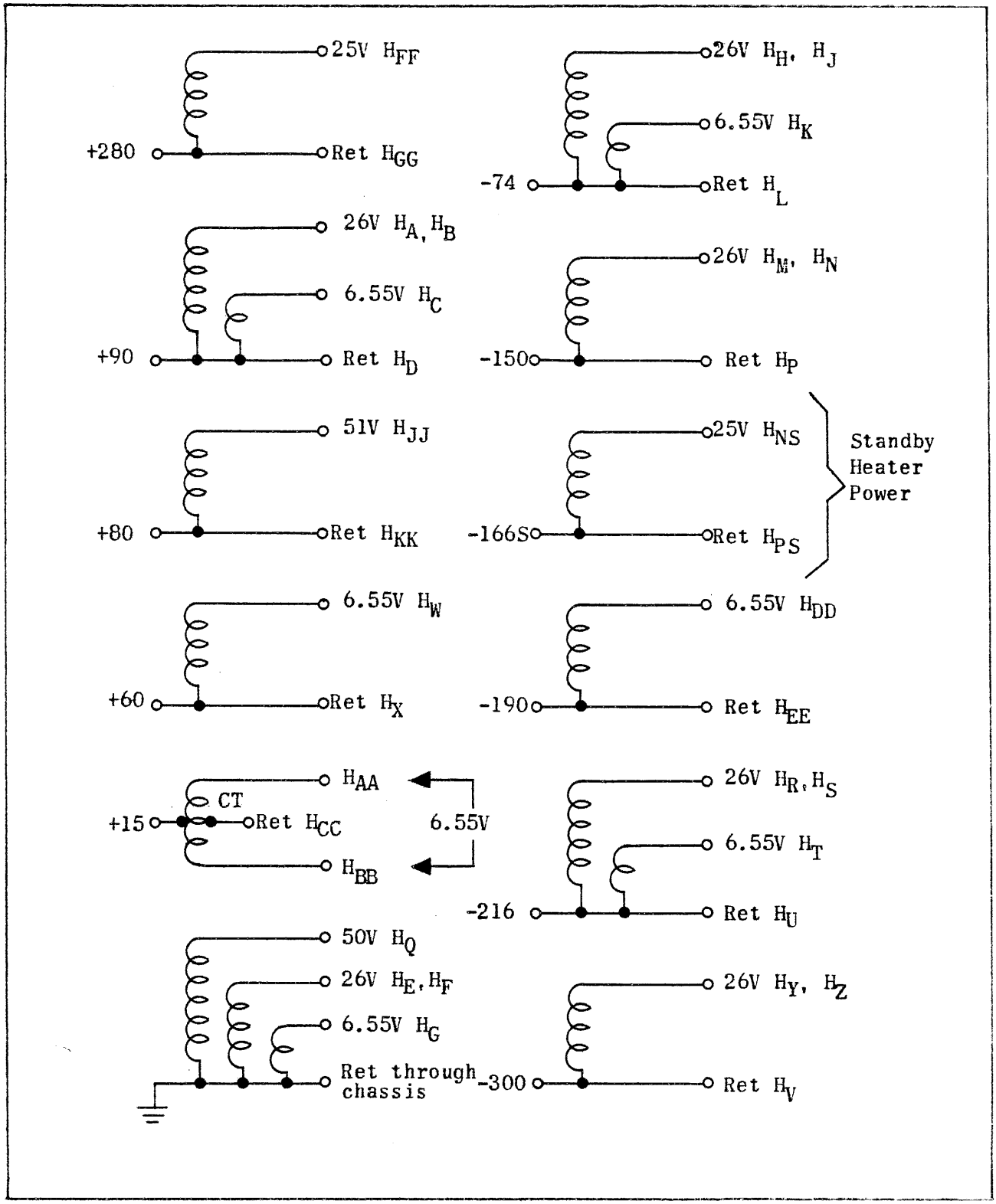


Figure 2-15. Heater Voltages Supplied to Central Computer

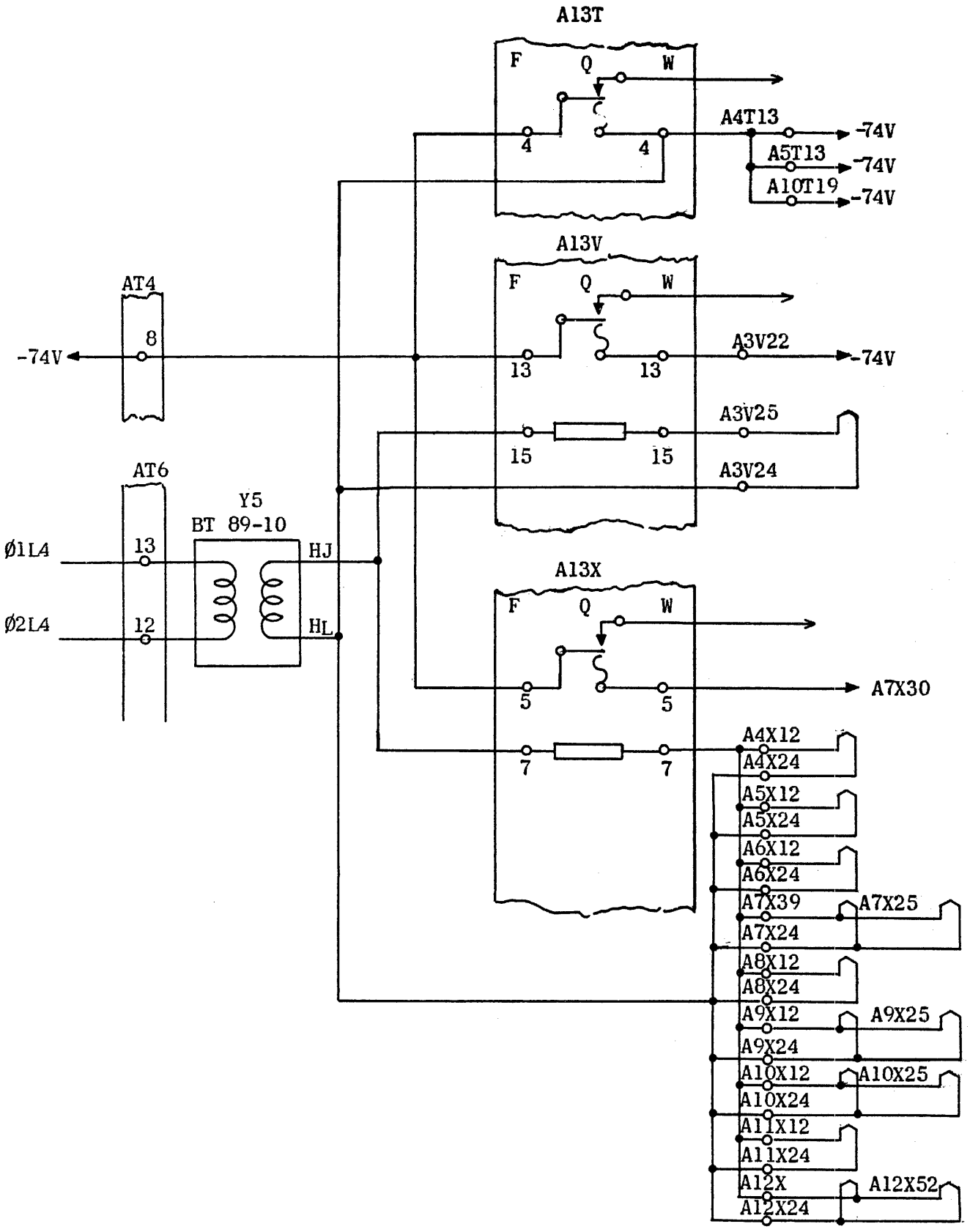


Figure 2-16. Typical Filament Voltage Wiring

TABLE 2-5

DC POWER INTERCONNECTIONS, (SERIALS 1 THRU 5)

POWER SUPPLY	COMPUTER QUADRANGLE TERMINAL	GAUGE	VOLTAGE
QT- A1	QT -10-8	16	+ 600
-A2	8-16	16	+ 410
-A3	8-17	16	+ 380
-A4	5-2	16	+ 285
-A5	5-3	16	+ 280
-A6	5-1	14	+ 255
-A7	5-6	12	+ 246
-A8	5-7	14	+ 200
-A9	5-8 to 11	6	+ 165
-A10	9-1	16	+ 358
-A11	5-12	16	+ 160
-A12	5-13	12	+ 150
-A13	5-15	10	+ 120
-A14	5-16	16	+ 105
-A15	5-17	16	+ 95
-A16	6-1	12	- 90
-A17	6-2	16	- 84
-B1	6-3	12	- 80
-B2	6-5	16	+ 75
-B3	6-6	10	+ 70
-B4	5-4	16	+ 306
QT -B5	QT 6-7	16	+ 66

TABLE 2-5 (Cont'd)

POWER SUPPLY	COMPUTER QUADRANGLE TERMINAL	GAUGE	VOLTAGE
QT -B6	QT -6-8 to 11	6	+ 60
-B7	6-12	16	+ 50
-B9	6-13	16	+ 48S
-B10	6-14	12	+ 40
-B11	6-15	16	+ 35
-B12	6-16	10	+ 30
-B13	6-17	14	+ 20
-B14	3-1	12	+ 18
-B15	3-2	4	+ 8
-B16	3-3	12	+ 5
-B17			
-C1	10-10	10	NEUTRAL
-C2			
-C3			
-C4			
-C5	3-4	16	- 1.75
-C6			
-C7	3-7	6	- 4
-C8	3-8	6	- 11
-C9	3-9	16	- 13
-C10	3-10	6	- 14
-C11	3-11	16	- 15
QT -C12	QT 3-12	16	- 16

TABLE 2-5 (Cont'd)

POWER SUPPLY	COMPUTER QUADRANGLE TERMINAL	GAUGE	VOLTAGE
QT -C13	QT -3-13	12	-17
-C14	3-14	16	-18
-C15	3-15	10	-20
-C16	3-16	16	-21
-C17	3-17	14	-25
-D1	4-1	16	-30
-D2	3-5	16	-28P
-D3	4-2	12	-34
-D4	4-3	8	-40
-D5	3-6	16	-48S
-D6	4-4	16	-50
-D7	4-5	16	-55
-D8	4-6	16	-60
-D9	4-7	16	-71
-D10	4-8 to 11	6	-74
-D11			
-D12	4-12	16	-80
-D13	4-13	16	-86
-D14	4-14	14	-88
-D15	4-15	16	-95
-D16	4-16	10	-100
-D17	4-17	10	-106

TABLE 2-5 (Cont'd)

POWER SUPPLY	COMPUTER QUADRANGLE TERMINAL	GAUGE	VOLTAGE
QT -E1	QT - 1-5	16	-117
-E2	10-7	16	-120
-E3	1-6	16	-125
-E4	1-7	16	-140
-E5	1-8 to 11	10	-150
-E6	2-1	16	-165
-E7	2-2	16	-166
-E8	2-3	16	-166S
-E9	2-4	16	-175
-E10	2-5	14	-190
-E11	2-6	16	-191S
-E12	2-7	16	-203
-E13	2-8	14	-216
-E14	2-9	16	-230S
-E15	2-10	16	-229
-E16	2-11	14	-300
-F1	7-8	16	-161
QT -F2	QT 7-14	16	-258

(Continued from Page 32)
contact points for primary power to the heater transformers and also standby voltage contact points (identified by an A).

The outputs from the upper barrier strips are bound together in a cable which runs up the right channel of the bay. Outputs from the lower strips run up the left channel. The lines for each section leave the cables and pass through holes in the outside of the channel to the input terminals (F) of the section fuseboards. The interconnections between the barrier strips and the fuseboards are shown on sheet 6 of the Bay Assembly Wiring Diagrams. The voltages on the various barrier strip terminals are shown in Table 2-6.

The output terminals (W) of the fuseboards are connected to the backboard terminals by cables which pass through the channels and into the d-c trough at the back of the bay. The interconnections between the fuseboard terminals and the chassis terminals of each section are shown on sheets 2, 3 and 4 of the Bay Assembly Wiring Diagrams.

The bypass capacitors for the d-c lines are located on the bypass boards (mounted on the section backboards) and also in the four corner bays. In general, the d-c voltages are bypassed at the barrier-strips nearest each corner, and also at the point of their entry into each chassis.

The connections made to the bypass capacitors located in the corner bays are listed in Drawing XD 105954: Filter Capacitor Wiring, BC, DE, HJ & KL Corners. The capacitors in BC corner are connected to the barrier strips of bay B; those in DE corner are connected to the barrier strips of bay E; those in HJ corner are connected to the barrier strips of bay H; those in KL corner are connected to the barrier strips of bay L. The other sides of all the capacitors are grounded.

The bypass boards for all sections of the computer are shown on the appropriate Bypass and Cable Termination Assembly drawings, supplied with the
(Continued on Page 55)

TABLE 2-6

BARRIER STRIP VOLTAGE

a. D.C. Voltages Common to Barrier Strips of all Chassis Bays

Terminal	Voltage	Source
T1-1	+410	QT8-16
-2	+380	QT8-17
-3	+280	Qt5-3
-4	+246	QT5-6
-5	+200	QT5-7
-6	+165	QT5-8,9 and 10
-7	+160	QT5-12
-8	+150	QT5-13
-9	+120	QT5-15
-10	+105	QT5-16
-11	+95	QT5-17
-12	+90	QT6-1
-13	+48S	QT6-13
T2-1	+84	QT6-2
-2	+80	QT6-3
-3	+75	QT6-5
-4	+70	QT6-6
-5	+66	QT6-7
-6	+60	QT6-8,9 and 10
-7	+50	QT6-12
-8	+40	QT6-14
-9	+35	QT6-15

TABLE 2-6 (Cont'd)

Terminal	Voltage	Source
T2-10	+30	QT6-16
-11	+20	QT6-17
-12	+18	QT3-1
-13	-1.75	QT3-4
T3-1	+8	QT3-2
-2	+5	QT3-3
-3	-4	QT3-7
-4	-11	QT3-8
-5	-13	QT3-9
-6	-14	QT3-10
-7	-15	QT3-11
-8	-16	QT3-12
-9	-17	QT3-13
-10	-18	QT3-14
-11	-20	QT3-15
-12	-21	QT3-16
-13	-25	QT3-17
T4-1	-30	QT4-1
-2	-34	QT4-2
-3	-40	QT4-3
-4	-50	QT4-4
-5	-55	QT4-5
-6	-60	QT4-6
-7	-71	QT4-7

TABLE 2-6 (Cont'd)

Terminal	Voltage	Source
T4-8	-74	QT4-8,9 and 10
-9	-80	QT4-12
-10	-86	QT4-13
-11	-88	QT4-14
-12	-95	QT4-15
-13	-100	QT4-16
T5-1	-106	QT4-17
-2	-117	QT1-5
-3	-125	QT1-6
-4	-140	QT1-7
-5	-150	QT-1, 9 and 10
-6	-165	QT2-1
-7	-166	QT2-2
-8	-175	QT2-4
-9	-190	QT2-5
-10	-203	QT2-7
-11	-216	QT2-8
-12	-229	QT2-10
-13	-300	QT2-11

TABLE 2-6 (Cont'd)

b. Barrier Strip Y-6 in Each Bay, LT-7 and PT-7

Terminal	Voltage	Source
AT6-1	-166S	LT7-6
-2	-191S	LT7-10
-3	-230S	LT7-11
-4	HNS	QT9-5
-5	HPS	QT9-6
-6	Ø1L5	QT9-11
-7	NEUTRAL	QT10-10
-8	-120	QT10-7
-9	Ø2L4M	PX16W-2
-10	Ø2L4	PT15W-2
-11	Ø1L4	PT16W-2
-12	Ø2L4	PT15W-3
-13	Ø1L4	PT16W-4
BT6-1	-166S	LT7-6
-2	-191S	LT7-10
-3	-230S	LT7-11
-4	HNS	QT9-5
-5	HPS	QT9-6
-6	+255	QT5-1
-7	+120	QT10-7
-8	+285	QT5-2
-9	SPARE	
-10	Ø2L4	PT15W-6

TABLE 2-6 (Cont'd)

Terminal	Voltage	Source
BT6-11	Ø1L4	PT16W-6
-12	SPARE	
-13	SPARE	
CT6-1	-166S	LT7-6
-2	-191S	LT7-10
-3	-230S	LT7-11
-4	HNS	QT9-5
-5	HPS	QT9-6
-6	+255	QT5-1
-7	-120	QT10-7
-8	+285	QT5-2
-9	+600	QT10-8
-10	Ø2L4	PT15W-10, 14
-11	Ø1L4	PT16W-10
-12	Ø2L4	PT15W-12
-13	Ø1L4	PT16W-12
DT6-1	SPARE	
-2	SPARE	
-3	SPARE	
-4	HNS	QT9-5
-5	HPS	QT9-6
-6	+255	QT5-1
-7	SPARE	
-8	+285	QT5-2

TABLE 2-6 (Cont'd)

Terminal	Voltage	Source
DT6-9	7AK7 Marginal	KT6-9
-10	Ø2L4	PT15W-14
-11	Ø1L4	PT16W-14
-12	Ø2L4	PT15W-16
-13	Ø1L4	PT16W-16
ET6-1	-166S	LT7-6
-2	-191S	LT7-10
-3	-230S	LT7-11
-4	HNS	QT9-5
-5	HPS	QT9-6
-6	-120	QT10-7
-7	SPARE	
-8	SPARE	
-9	Ø2L4-M	PX16W-4
-10	Ø2L4	PT15W-18
-11	Ø1L4	PT16W-18
-12	Ø2L4	PT15W-20
-13	Ø1L4	PT16W-20
MT6-1	-166S	LT7-6
-2	-191S	LT7-10
-3	-230S	LT7-11
-4	HNS	QT9-5
-5	HPS	QT9-6
-6	-120	QT10-7
-7	-30P	QT3-5

TABLE 2-6 (Cont'd)

Terminal	Voltage	Source
MT6-8	Ø1L5	QT9-11
-9	NEUTRAL	QT10-10
-10	Ø2L4	PT15W-22
-11	Ø1L4	PT16W-22
-12	Ø2L4	PT15W-24
-13	Ø1L4	PT16W-24
MT6-1	SPARE	
-2	SPARE	
-3	SPARE	
-4	HNS	QT9-5
-5	HPS	QT9-6
-6	-120	QT10-7
-7	-30P	QT3-5
-8	SPARE	
-9	SPARE	
-10	Ø3L4	PV15W-2
-11	Ø1L4	PV16W-2
-12	Ø3L4	PV15W-4
-13	Ø1L4	PV16W-4
GT6-1	-166S	LT7-6
-2	-191S	LT7-10
-3	-230S	LT7-11
-4	HNS	QT9-5
-5	HPS	QT9-6
-6	-120	QT10-7

TABLE 2-6 (Cont'd)

Terminal	Voltage	Source
GT6-7	+285	QT5-2
-8	+255	QT5-1
-9	Ø3L4M	PX16W-26
-10	Ø3L4	PV15W-6
-11	Ø1L4	PV16W-6
-12	Ø3L4	PV15W-8
-13	Ø1L4	PV16W-8
HT6-1	-166S	LT7-6
-2	191S	LT7-10
-3	-230S	LT7-11
-4	HNS	QT9-5
-5	HPS	QT9-6
-6	-120	QT10-7
-7	-258	QT7-14
-8	-161	QT7-8
-9	SPARE	
-10	Ø3L4	PV15W-10
-11	Ø1L4	PV16W-10
-12	+358	QT9-1
-13	+306	QT5-4
JT6-1	-166S	LT7-6
-2	-191S	LT7-10
-3	-230S	LT7-11
-4	HNS	QT9-5
-5	HPS	QT9-6

TABLE 2-6 (Cont'd)

Terminal	Voltage	Source
JT6-6	-48S	QT3-6
-7	+600	QT10-8
-8	Ø3L4M	PX16W-24
-9	Ø3L4	PV15W-14
-10	Ø3L4	PV16W-14
-11	Ø1L4	PV16W-14
-12	Ø3L4	PV15W-16
-13	Ø1L4	PV16W-16
KT6-1	-166S	LT7-6
-2	-191S	LT7-10
-3	-230S	LT7-11
-4	HNS	QT9-5
-5	HPS	QT9-6
-6	Ø3L4M	PX16W-24
-7	+285	QT5-2
-8	+255	QT5-1
-9	SPARE	
-10	Ø3L4	PV15W-18
-11	Ø1L4	PV16W-18
-12	Ø3L4	PV15W-20
-13	Ø1L4	PV16W-20
LT6-1	-166S	LT7-6
-2	-191S	LT7-10
-3	-230S	LT7-11
-4	HNS	QT9-5
-5	HPS	QT9-6

TABLE 2-6 (Cont'd)

Terminal	Voltage	Source
LT6-6	SPARE	
-7	SPARE	
-8	SPARE	
-9	SPARE	
-10	Ø3L4	PV15W-22
-11	Ø1L4	PV16W-22
-12	Ø3L4	PV15W-24
-13	Ø1L4	PV16W-24
LT7-1	Ø1L6	QT10-1
-2	-30	QT4-1
-3	+30	QT6-16
-4	Ø1L6SB	QT10-3
-5	+48	QT6-13
-6	-166S	QT2-3
-7	+120	QT5-15
-8	-15	QT3-11
-9	Ø1L6B	QT10-2
-10	-191S	QT2-6
-11	-230S	QT2-9
-12	-48S	QT3-6
-13	-30P	QT3-5
PT6-1	-166S	LT7-6
-2	-191S	LT7-10
-3	-230S	LT7-11
-4	HNS	QT9-5

TABLE 2-6 (Cont'd)

Terminal	Voltage	Source
PT6-5	HPS	QT9-6
-6	Ø1L5	QT9-11
-7	NEUTRAL	QT10-10
-8	SPARE	
-9	SPARE	
-10	Ø3L4	PV15W-26
-11	Ø1L4	PV16W-26
-12	SPARE	
-13	SPARE	
PT7-1	GROUND	QT10-11
-2	Ø2L4M	PX16
-3	Ø3L4M	PX16
-4	#4	TB2-11
-5	#2	TB2-12
-6	#3	TB2-14
-7	MARGIN CHECK	LJJ9
-8	AC ON	TB2-10
-9	A	TB2-28
-10	B 3-way valve	TB2-29
-11	C	TB2-30
-12	Ø1L6	TJH33
-13	MACHINE OVERHEAT	PJT25
-14	HI-TEMP	LJG28
-15	TEMP. CONTROLLER	QT7-2
-16	SPARE	
-17	SPARE	

TABLE 2-6 (Cont'd)

Terminal	Voltage	Source
2J1-1	SPARE	
-2	SPARE	
-3	SPARE	
-4	+410	QT8-16
-5	+246	QT5-6
-6	+200	QT5-7
-7	+95	QT5-17
-8	+90	QT6-1
-9	+70	QT6-6
-10	+60	QT6-9
-11	+50	QT6-12
-12	+48	QT6-13
-13	+48	QT6-13
-14	+30	QT6-16
-15	+5	QT3-3
-16	-14	QT3-10
-17	-20	QT3-15
-18	-34	QT4-2
-19	-55	QT4-5
-20	-74	QT4-9
-21	-100	QT4-16
-22	-117	QT1-5
-23	-150	QT1-9
-24	-166	QT2-2
-25	-190	QT2-5

TABLE 2-6 (Cont'd)

Terminal	Voltage	Source
2J1-26	-203	QT2-7
-27	-216	QT2-8
-28	-300	QT2-11
-29	SPARE	
-30	SPARE	
-31	SPARE	
-32	-30	QT4-1
-33	SPARE	

(Continued from Page 41)
computer. The connections made to the capacitors on these boards are indicated on sheets 2, 3 and 4 of the Bay Assembly Wiring diagrams. For example, the callout V1A7 on the diagram of a particular section specifies a connection to terminal 7 of bypass board V1A of that sections.

(8) LIGHTS AND AC OUTLETS. - The Central Computer is provided with three interior lights and numerous a-c convenience outlets. The lights and two double-receptacle outlets are mounted inside the computer on the tray assembly. The locations are shown on drawing XR 106192: Modified Tray Assembly, Wired.

Each of the following chassis bays is provided in the two single-receptacle outlets: A, B, C, D, H, J, K, L and P. The outlets are mounted on the channels and are accessible from the front of the bays. One outlet is mounted between sections T and V, the other between sections V and X. Bays E, M and N each have one single-receptacle outlet, mounted on the front of the left channel, between sections V and X. An outlet is also mounted at the bottom of each corner bay, accessible from outside the computer.

The wiring of the bay-mounted a-c outlets is shown in drawing XD 106023: Wiring of AC Outlets, Univac II and also on sheet 5 of the Bay Assembly Wiring diagrams. All the outlets are connected in parallel by wires which pass through the Jones ring. Terminals 28 through 33 of Jones plugs AJB, BJB, CJD, DJF, EJC, MJC, NJC, HJB, JJA, KJB, LJA and PJA are used for this purpose. Ø1L5 from Quadrangle terminal QT9-11 is distributed to terminals AT6-6, MT6-8 and PT6-6 of the barrier strip ring, and to terminal OJK-2 of the Jones ring. Neutral is distributed to terminals AT6-7, MT6-9 and PT6-7 of the barrier strip ring, and OJK-15 of the Jones ring. The barrier strips of bays A and P are connected to the outlets in those bays, thus supplying Ø1L5 and Neutral to all the bay-mounted outlets.

The wiring of the tray-mounted outlets and the lights is shown in drawing XR 106192. The outlets and lights, connected in parallel, are fed by Ø1L5 and Neutral from barrier strip MT6.

Ø1L5 and Neutral are connected to the a-c outlets of the SC Console via terminals OJK-2 and OJK-5 of the Jones Ring.

(9) BLOWERS (Reference: Drawing XG129029 - Blowers, Air Vane Switches and Door Interlocks, Wiring Layout). - The two blowers of the Central Computer, designated Blowers 4 and 5, are supplied with 3-Ø a-c power from the Switchgear. The power lines are fused at fuseboard PX15 before being connected to the blowers.

The $Ø1L3B_4$, $Ø2L3B_4$ and $Ø3L3B_4$ lines are terminated at Quadrangle terminals QT7-11, 15 and 9, respectively. These terminals are connected to fuseboard terminals PX15-F8, PX15-14 and PX15-20 respectively. The W terminals of these fuseboards are connected to Quadrangle terminals QT9-2, 3 and 4, respectively, and from there to Blower #4.

The $Ø1L3B_5$, $Ø2L3B_5$ and $Ø3L3B_5$ lines are terminated at Quadrangle terminals QT7-12, 16 and 10, respectively. These terminals are connected to fuseboard terminals PX15-F10, PX15-F2 and PX15-F22, respectively. The W terminals of these fuseboards are connected to Quadrangle terminals QT1-2, 3 and 4 respectively, and from there to Blower #5.

d. SIGNAL DISTRIBUTION

(1) GENERAL. - Two types of signals are generated within the Central Computer. The circuits over which each is transmitted differ according to the frequency response required of them. Low-speed signals, or those with long rise times (such as function signals and Supervisory Control Switch signals) are transmitted over the low-speed wiring system. High-speed signals, or those with short rise-times (such as timing and information pulses), are transmitted over a direct route, high-speed wiring system or by coaxial cables.

(2) LOW SPEED WIRING. - The low-speed signals are transmitted over the low-speed harness, which completely encircles the computer just above the bays. The wires of the harness are terminated at 128 33-pin Jones plugs mounted on the framework above the bays. The complete assembly, designated as bay X of the Central Computer is shown in drawing XG142661. The positions of the plugs above each bay are labeled alphabetically, from left to right. The complete designation of a Jones plug connection specifies the bay, connector, and pin number. As an example, XJB16 is terminal 16 of Jones plug B in Bay X. The Jones plug designations are stamped on the framework above the socket and also on the connectors.

The complete list of Jones plugs in Bay X is provided in Table 2-7. The interconnections between the Jones plug, as provided by the low-speed harness, are listed in the Jones ring wiring tabulations (A128733), provided with each Univac II installation. The connections between the backboard terminals and the Jones plug terminals are listed on the Bay Assembly Wired diagrams. The leads run down the interbay channel to the section troughs and, finally, to the chassis terminals. On the section backboard low-speed signal wires travel from terminal-to-terminal for short runs, but may go into the wiring trough and out again for longer runs.

(3) HIGH SPEED WIRING. - The high-speed wiring is of two types: point-to-point, and coaxial cables. If a high-speed signal is used in only a few places, it is usually transmitted over the high-speed wiring system. If the signal goes to many circuits, coaxial cabling is used to prevent overloading of the source. In most cases, cathode-followers drive the signals over the point-to-point wiring. The coaxial lines are usually driven by pulse transformers.

Point-to-point wires run from source to load by the shortest possible route. If the line is more than a few inches long, it passes across the backboard on standoff posts. In this manner, it may cross several sections before

(Continued on Page 59)

Table 2-7. Jones Plugs of Bay X

Bay	Jones Plugs
A	AJA, AJB, AJC, AJF, AJG, AJT, AJU, AJW
B	BJA, BJB, BJC, BJD, BJE, BJF, BJS, BJT, BJU, JBW
C	CJA, CJB, CJC, CJD, CJE, CJF, CJK, CJL, CJR, CJS, CJT, CJW
D	DJA, DJB, DJC, DJE, DJF, DJG, DJH, DJL, DJM, DJP, DJR, DJT
E	EJA, EJB, EJC, EJD, EJE, EJF, EJH, EJP, EJR
M	MJA, MJB, MJC, MJD, MJE
N	NJA, NJB, NJC
G	GJA, GJB, GJC, GJD, GJG, GJW
H	HJA, HJB, HJW
J	JJA, JJB, JJW
K	KJA, KJB, KJU, KJW
L	LJA, LJB, LJF, LJG, LJH, LJJ
P	PJA, PJT, PJU, PJW
O	OJA, OJB, OJC, OJD, OJE, OJF, OJG, OJH, OJCC, OJJ, OJK, OJM, OJN, OJDD, OJGG, OJP, OJEE, OJR, OJS, OJT, OJFF, OJU, OJW, OJX, OJY, OJZ, OJAA, OJBB, OJHH, OJJJ, OJRR, OJSS, OJMM, OJNN
1	1JA, 1JB, 1JC, 1JD, 1JE, 1JV, 1JW, 1JX, 1JY
2	2JP

(Continued from Page 57)
it reaches the load. At the edge of a section, the wires are connected to the section-edge terminal strips. See Figure 2-7. These strips are designated A1, A2 and A3 across the top of the section, D1, D2 and D3 across the bottom, K and M on the left side, and G and J on the right side. Removable jumpers connect the terminals of a strip in one section to the terminals of the adjacent to strip in another. (For example, strip D1 of section T of a bay is adjacent to strip A1 of section V of that bay; strips G of each section of bay A are adjacent to strips K of each section of bay B.) Table 2-8 shows the pin numbering system and the relative positions of the pins of two adjacent section-edge terminal boards.

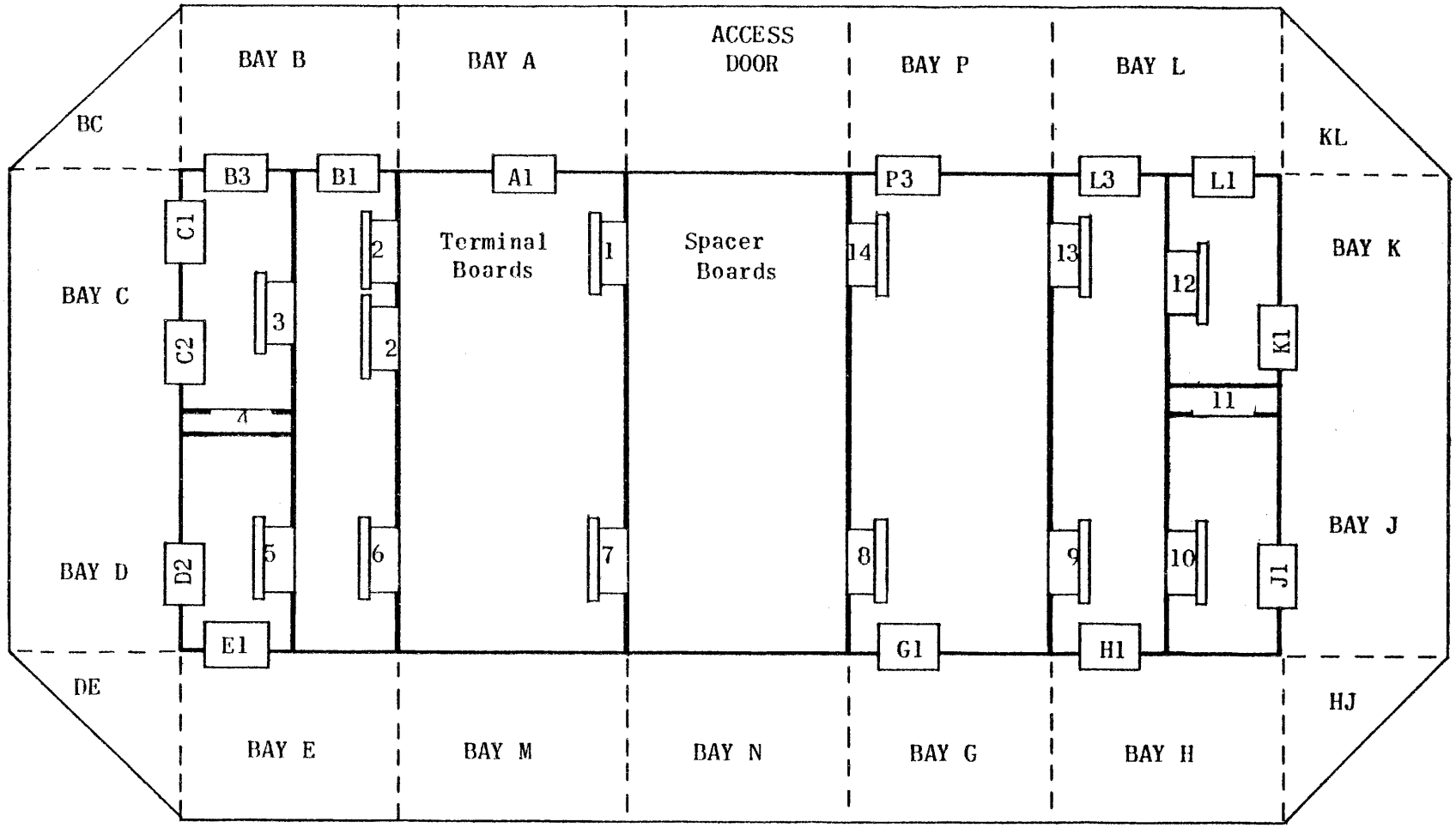
Table 2-8. Jumper Connections between Adjacent Section-Edge Terminal Boards

Terminal	Terminal	Terminal	Terminal
1	17	17	1
2	18	18	2
3	19	19	3
4	20	20	4
5	21	21	5
6	22	22	6
7	23	23	7
8	24	24	8
9	25	25	9
10	26	26	10
11	27	27	11
12	28	28	12
13	29	29	13
14	30	30	14
15	31	31	15
16	32	32	16

Frequently, the shortest route from source to load is across the top of the computer. A group of terminal boards and spacer boards, mounted on the tray assembly of the computer, carry the point-to-point wiring across the tray assembly. The terminal boards are identical to the section-edge terminal boards and are mounted on the tray directly opposite the A1, A2 and A3 boards of the "T" sections. The terminal boards of the tray section carry alphabetic and numeric designations, as shown in Figure 2-17. The jumper connections between the terminal boards of the bays and those of the tray are listed on 106192, sheets 10 through 13.

The spacer boards route the point-to-point wiring between the terminal boards. Each spacer board has 30 holes, numbered from 1 to 30, spaced at equal distances apart. A total of 14 boards are mounted around the outer edge of the tray assembly. The boards are designated 1 through 14, proceeding from the board above bay A through the board above bay P. In the case of board 2, above bay B, a pair of spacer boards are required to accommodate all the wires. The holes of these boards are designated 1 through 60. The routes of the wires between terminal boards of the tray assembly, through the spacer boards, is shown on 106192, sheets 1 through 9.

The coaxial cables go from source to load by the most convenient route. In some instances, a direct route is used; in others, the cables follow the route of the low speed wiring. The coaxial wiring is shown in the Bay Assembly Wiring diagrams. All cables are terminated in their characteristic impedance at the load; the terminating resistors are mounted on the Bypass Boards of each section.



NOTE

Refer to Drawing XR106180 for greater detail.

Figure 2-17. Terminal and Spacer Boards of Tray Assembly

e. CORNER BAYS OF CENTRAL COMPUTER. - The corner bays of the Central Computer contain miscellaneous power and control components. The equipment in each corner falls into the following groupings:

BC Corner - Uniservo Control Circuits (BC Box); Function Table Neon Assembly; Bypass Capacitors; Filament Transformers Y7 and Y8. DE Corner - DE Fuseboard; Bypass Capacitors; Filament Transformers Y15, Y16, Y17, Y18, Y19 and Y20.

HJ Corner - Contactors 2, 3 and 4; Bypass Capacitors; Filament Transformers Y28, Y29, Y30 and Y31.

KL Corner - KL Fuseboard; Relay Panel Assembly, Maintenance Panel Assembly; Bypass Capacitors; Filament Transformers Y39, Y40, Y41, Y42, Y43 and Y44.

f. EXTERNALLY-MOUNTED EQUIPMENT. - While most of the electronic components of the Central Computer are mounted on the chassis or in readily identifiable locations, because of size, certain components are mounted inside the computer on the backs of the bays. The locations of these components do not follow any standard system. Table 2-9 lists each of these components and the approximate location by bay and section. A description of each component, the circuitry to which it belongs, and where possible, a reference to the applicable drawings, is also provided.

TABLE 2-9

MISCELLANEOUS COMPONENTS OF CENTRAL COMPUTER

Component	Location	Description
HSB Resistors	Above Bay G Backboard	Cathode Load for HSB Output Drivers
HSB Diodes	On Backboard of Chassis involved	Input Diodes to Registers
Timing Relay	AV Backboard	Printer Thyratron Control
K Relay	AV Backboard	Keyboard (input) Control
Automatic Re-Read Counter	AT Backboard	Records total number of automatic rereads performed
Bay C Relays	Above Bay C Backboard	General Clear, IOS, O Error Clear, I Error Clear, Univac I, and Empty relays
Tape Amplifier Filters	On Unistrut above Roof Sheet	Provide filtered supply voltages for the tape amplifiers.

3. ELECTRICAL DESCRIPTION OF CONVENTIONAL CHASSIS CIRCUITS

a. GENERAL. - This section discusses the electrical operation of the basic circuits which make up the various elements of the computer. The entire Univac II system is composed of a great number of similar circuits in various combinations. Particular circuits may vary from case to case in so far as voltage and signal levels are concerned, but the actual operation remains the same. Thus, when unique circuits are encountered, the discussion of its basic group may be the basis for its electrical analysis. The emphasis of explanations is directed toward "how" the circuit operates rather than "what" the circuit does. Each circuit is presented in schematic form along with its accepted "logical" symbol. Values given are approximate and serve only as an aid in explanation.

b. GATES. - Signal or information flow within and between the various elements of the computer is controlled by many GATE circuits. The gates are classified as the logical "OR" type or the logical "AND" type. "OR" type gates, or mixing gates, introduce signals from several sources to a common signal line. "AND" type gates, or coincidence gates, require certain signal input conditions be met in order to secure an output signal from the gate.

Most gates in the computer are of the crystal diode type. Crystal diodes are used extensively because of their small size and their property of unilateral impedance. Vacuum tubes are used when current conditions within a circuit are too large to be adequately handled by crystal diodes.

(1) CRYSTAL DIODE "OR" TYPE GATES. - The circuit presented in Figure 3-1 illustrates a typical three input crystal diode "OR" gate. Normally Input 1, Input 2 and Input 3 are held at +90v. Since the crystal diodes offer negligible forward resistance, current is drawn through the 7.2K

resistor from the +246V source and point A is maintained at +90v. If the signal condition (+60) exists on any of the inputs its associated diode will conduct most heavily and will bring point A down to +60v. The output from the "OR" gate is a negative going signal of 30V amplitude. The input crystal diodes provide isolation by resisting current flow in the backwards direction; thus they prevent the appearance of the selected signal in the circuits responsible for the signals to the other inputs. The operation of this gate may be stated: Signal 1 or Signal 2 or Signal 3 yields an output.

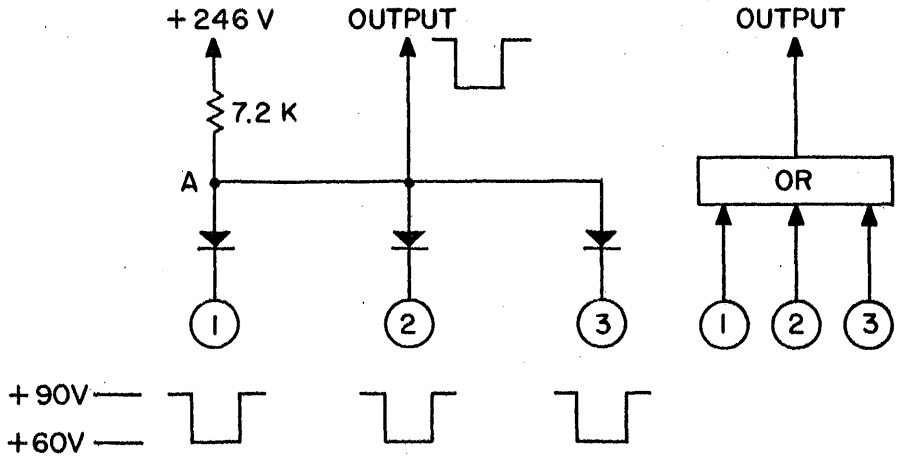


Figure 3-1. Typical Crystal Diode "OR" Gate

(2) CRYSTAL DIODE "AND" TYPE GATES. - Figures 3-2, 3-3 and 3-4 illustrate three types of crystal diode "AND", or coincidence, gates found in the computer. The logic of the "AND" gate is that certain signal input conditions must be met to secure an output from the gate.

The operation of the gate in Figure 3-2 requires the presence of three input (negative going) signals in order that a signal may be generated which will cut off vacuum tube V1. In this case assume the voltage level of the

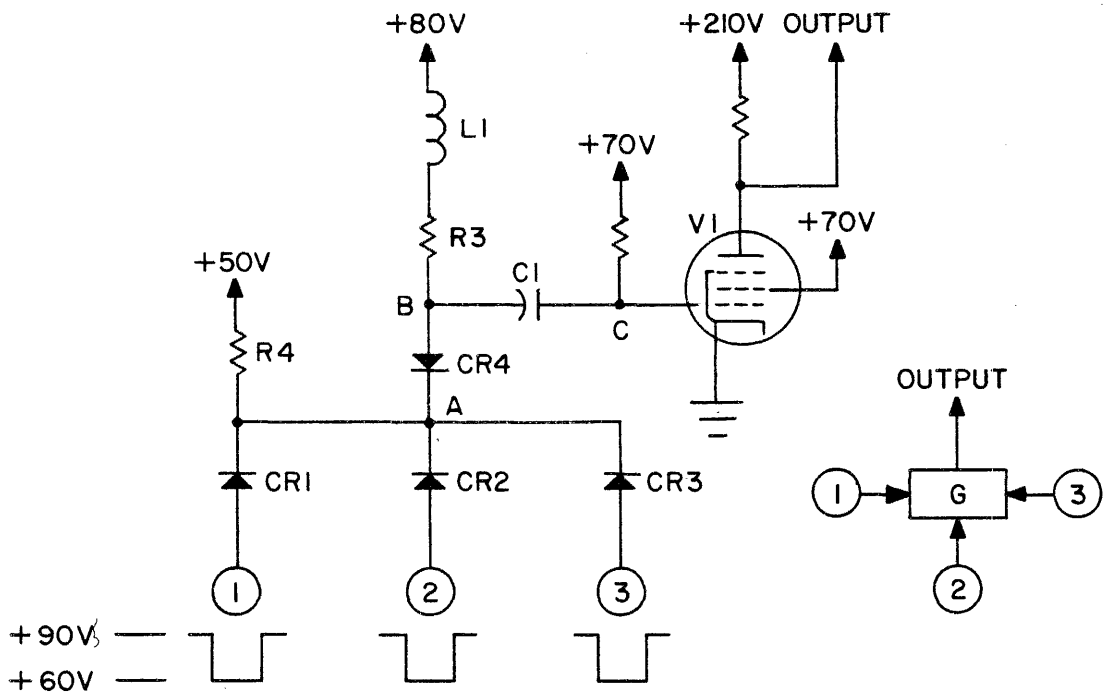


Figure 3-2. Typical Crystal "AND" Gate

no signal condition at the inputs 1, 2 and 3 is +90v. Diodes CR1, CR2 and CR3 will conduct, drawing current through R4, and hold point A at +90v. This will cut off diode CR4, thereby keeping point B at a high enough potential to maintain vacuum tube V1 in the state of conduction. As long as any one of the input levels remains "up" its diode will conduct most heavily maintaining point "A" at 90v. If inputs 1, 2 and 3 drop in potential level, indicating the presence of signals on all three inputs, point A will follow the drop. In the computer, signals entering such gates have a -30v swing. When point A reaches approximately +80v, diode CR4 begins to conduct and point B will follow the potential at point A to the +60v minimum. This signal passes coupling capacitance C1 and is applied to vacuum tube V1 as a 20v signal drop, which

is sufficient to cause V1 to cease conduction for the duration of the output of the gate. Stated in equation form: Signal 1 and Signal 2 and Signal 3, together, yield an output.

The gate illustrated in Figure 3-3 is a typical delete gate. Signal 1 will pass through unimpeded unless either Signal 2 or Signal 3 is present. The operation of the gate can be described as follows: Normally the inputs 2 and 3 are at a +60v potential. This allows the presence or absence of Signal 1 to control the potential at point A. A variation of ±30v at point A will appear as a variation of ± 20v at point B, thence through coupling capacitor C1 and into the output of the gate. However, if a signal (+90v) is present at input 2 or input 3, either diode CR1 or CR2 will conduct causing point A to remain at +90v thereby maintaining diode CR4 inoperative. This effectively stops any signal attempting to pass through the gate. This action can be stated as the equation Signal 1 and not Signal 2 or Signal 3 yields an output from the gate.

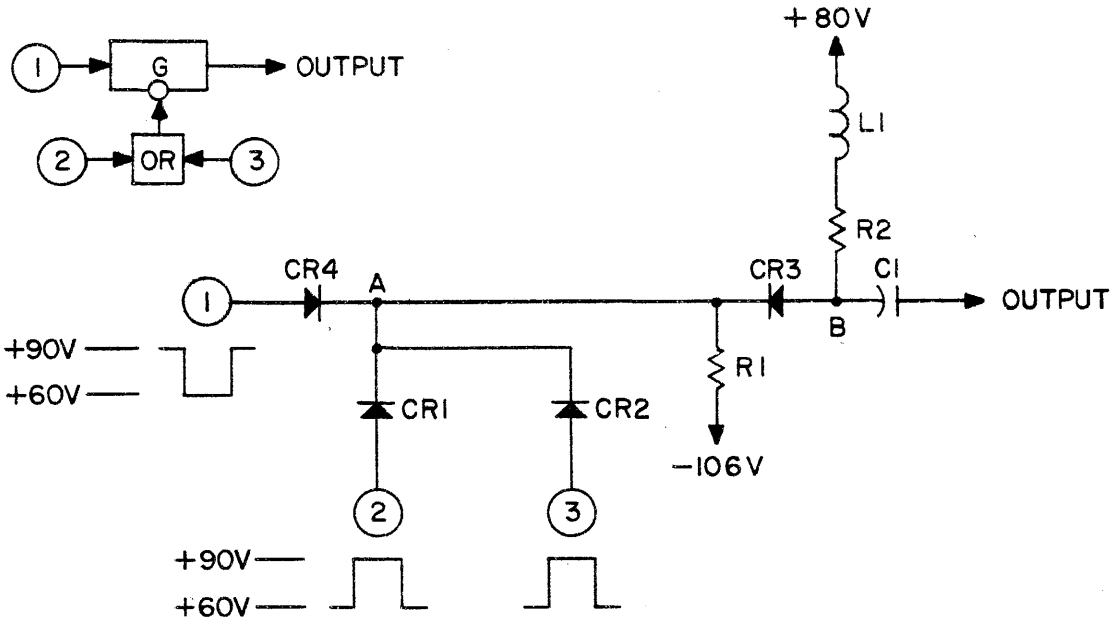


Figure 3-3. Crystal Diode Delete Gate, Type I

Figure 3-4 presents another gating configuration used extensively in the computer. In this case Signal 1 will appear at the output whenever Signal 3 is not present or if Signal 3 is present but its effect is suppressed by Signal 2. The signals at inputs 1 and 2 are negative-going (+90v to +60v) and at input 3 the signal is positive going (+60v to +90v). Thus, with the absence of Signal 3 or the presence of Signal 2, crystal diode CR3 will be cut off (+60v), enabling the presence or the absence of Signal 1 to control the voltage level at point A. The presence of Signal 3 and the absence of Signal 2 raises the potential level at point B (+90v). As the voltage at point B is raised,crystal diode CR3 conducts thereby raising the potential level at point A (+90v). This causes any signal appearing at input 1 to be deleted. Crystal diode CR2 will pass any negative going signals into the output of the gate. The purpose of the circuit containing coil L1 and resistor R1 is to give the output signal proper shaping.

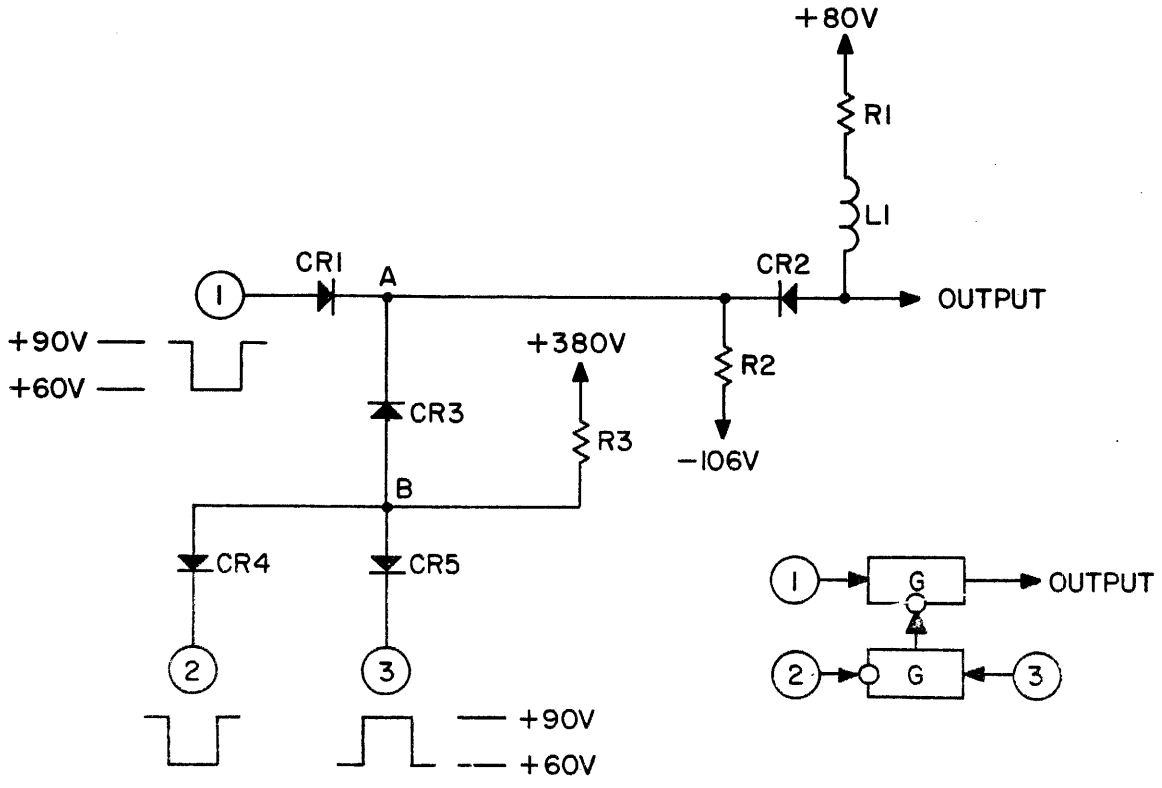


Figure 3-4. Crystal Delete Gate, Type II

(3) VACUUM TUBE "AND" TYPE GATES. - Figure 3-5 illustrates a typical 7AK7 vacuum tube gate. The tube is kept non-conducting by the low control grid and suppressor grid return voltages. The simultaneous presence of positive going Signal 1 (-20v to +5v) and positive going Signal 2 (-20v to +5v) causes the vacuum tube to conduct. The plate circuit of V1 contains a pulse transformer which, besides being an impedance matching device, makes it possible to select either a positive or a negative output from the gate.

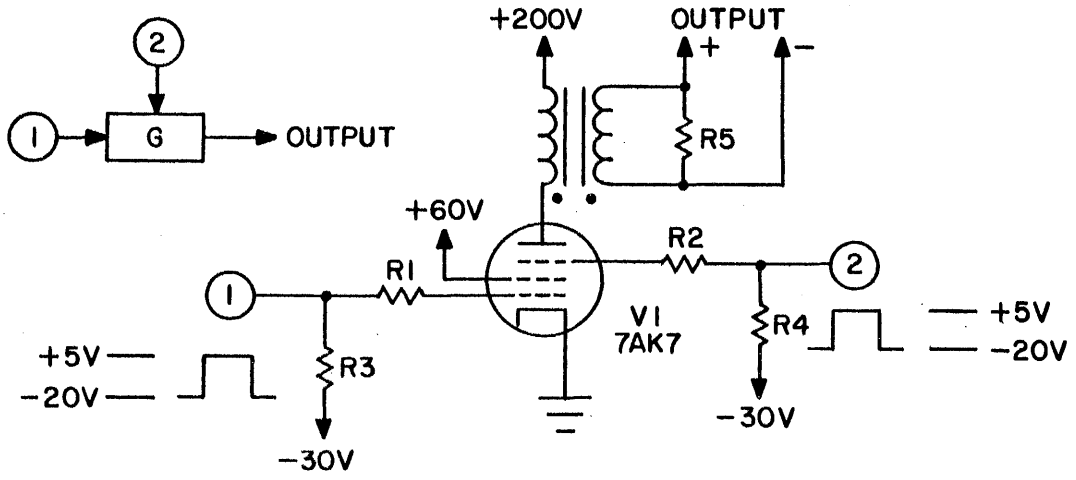


Figure 3-5. Schematic Diagram, Vacuum Tube "AND" Gate

(4) CLOCK GATES. - Figure 3-6 illustrates the crystal diode Clock Gate and its vacuum tube drivers. The Clock Gate is used wherever sharp, precisely timed pulses are needed in the computer circuitry. These pulses, referred to as TIMING PULSES, are used to reshape and retime information pulses and control signals, or they are used when extremely short duration input signals are required by a flip-flop. When it is used for reshaping and retiming, the Clock Gate is part of a larger element called a Pulse Former (see paragraph (d) this section).

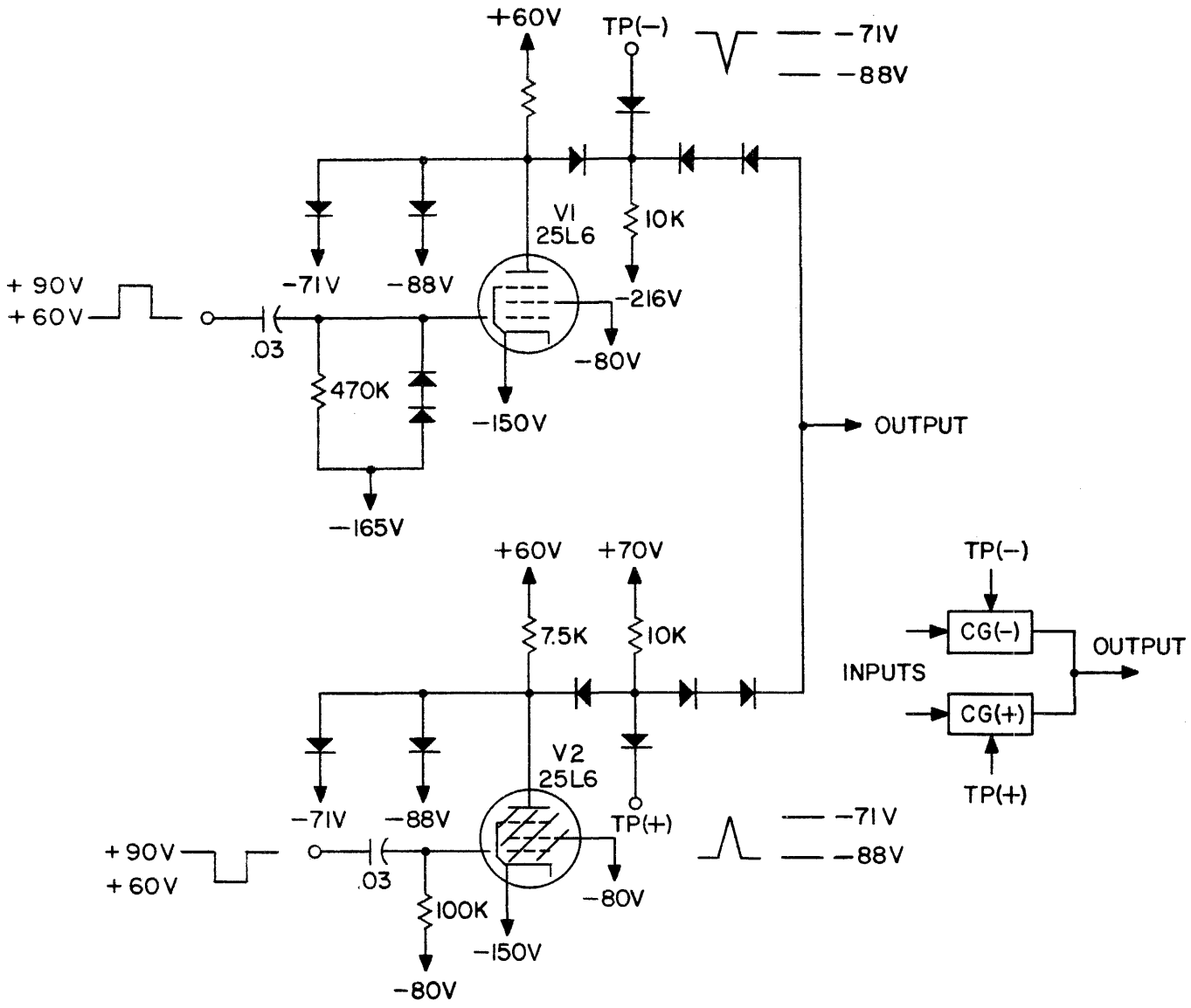


Figure 3-6. Schematic Diagram, Typical Clock Gate

The Clock Gate has two sections, positive and negative, which respond to TP's of corresponding polarity. Each section may have its own vacuum tube driver or the output of one driver may be connected to both sections. The outputs of both sections of the Clock Gate come together in "OR" gate fashion and are then supplied to the control grid of one tube of a flip-flop.

As long as no signal is present to drive normally cut-off tube V1 into conduction, the plate potential and therefore the output from V1 to the

negative section of the Clock Gate is held by clamping action at -71v. This level keeps the negative section of the gate inoperative. When V1 is driven to conduction the drop in plate potential to the lower clamped limit of -88v alerts the negative section of the Clock Gate. When the next TP- occurs a negative going signal (-71v to -88v) passes the output crystal diodes to the flip-flop. The negative section of the Clock Gate continues to pass TP's as long as V1 is held in conduction.

With no signal on its control grid V2 is maintained normally conducting. The -88v potential of its plate holds the positive section of the Clock Gate inoperative. When V2 is cut off the rise in its plate potential to -71v alerts the positive section of the Clock Gate. When the next TP+ occurs a positive going signal (-88v to -71v) passes the output crystal diodes to the flip-flop. The positive section of the Clock Gate continues to pass TP's as long as V2 is held cut-off.

The driver tubes respond to signals which are a minimum of one computer pulse time in width (.445 μsec). The output signal from a Clock Gate has a width of a TP (.08 μsec). The circuit is timed so that the TP will occur approximately one-half pulse time after the appearance of a signal on the control grid of the driver tube. This ensures the presence of the alerting signal on the Clock Gate. The difference in timing between the driver input and the TP introduces approximately one-half pulse time of delay to the signal passing through the Clock Gate.

c. FLIP-FLOPS. - Basically the flip-flop is a device composed of two vacuum tubes, or the two halves of a dual vacuum tube, which are so connected that only one tube can conduct at any one time. As a result the flip-flop may be used to store a single binary digit, or it may be the source for a pair of

control signals. The two conditions to which a flip-flop may be driven are generally referred to as the "reset" and "set" states. The reset side is arbitrarily designated as the side of the flip-flop which is normally non-conducting. In certain instances where the flip-flop is used specifically to store a binary digit the two conditions are referred to as the "0" and "1" states, corresponding to the side which will hold the particular bit.

Most flip-flops are supplied with two outputs, one from either side. These outputs are referred to as the RESET OUTPUT and the SET OUTPUT, depending on the half of the flip-flop to which they are connected.

The flip-flops in UNIVAC II are classified with regard to the time required for them to switch from one state to the other. The three recognized groups are the high speed, the medium speed and the low speed flip-flops. The make-up and operation of these different groups is essentially the same. A negative-going signal applied as an input to the conducting side of the flip-flop causes this side to cut off. The change in the plate potential of this tube as it cuts off is applied on the control grid of the other tube through an RC network and causes this cut-off tube to conduct. The RC network helps establish the switching time. As this tube goes into conduction the lowering of its plate potential appears on the control grid of the addressed tube hastening its cut off, and holds the tube cut off after the states of the tubes have been switched. The flip-flop remains in the reverse state until a negative going signal again is applied to the conducting tube, or if the circuit design is so modified that the cut-off tube can receive a positive-going signal. Most flip-flops have isolation crystals on their inputs and therefore can be addressed by negative-going signals only. Outputs are supplied from either one or both sides of the flip-flop depending on circuit

requirements. Most flip-flops have neon indicators mounted in the chassis in which they are located which light when the flip-flop is in the "set" condition. The more important flip-flops have neon indicators on the SC panel which light when they are set.

(1) HIGH SPEED FLIP-FLOPS. - The high speed flip-flop has a switching time of less than .08 μsec. The speed of these flip-flops is such that they re-act in less than one pulse time. High speed flip-flops are used wherever a word must pass through a flip-flop or wherever an extremely rapid response by a flip-flop to an input signal is required. A schematic diagram of a typical high speed flip-flop is presented in Figure 3-7. A high speed flip-flop is always composed of two 25L6 vacuum tubes. The plate circuit of the high speed flip-flop contains a choke which gives extremely fast rise time to the flip-flop output signal.

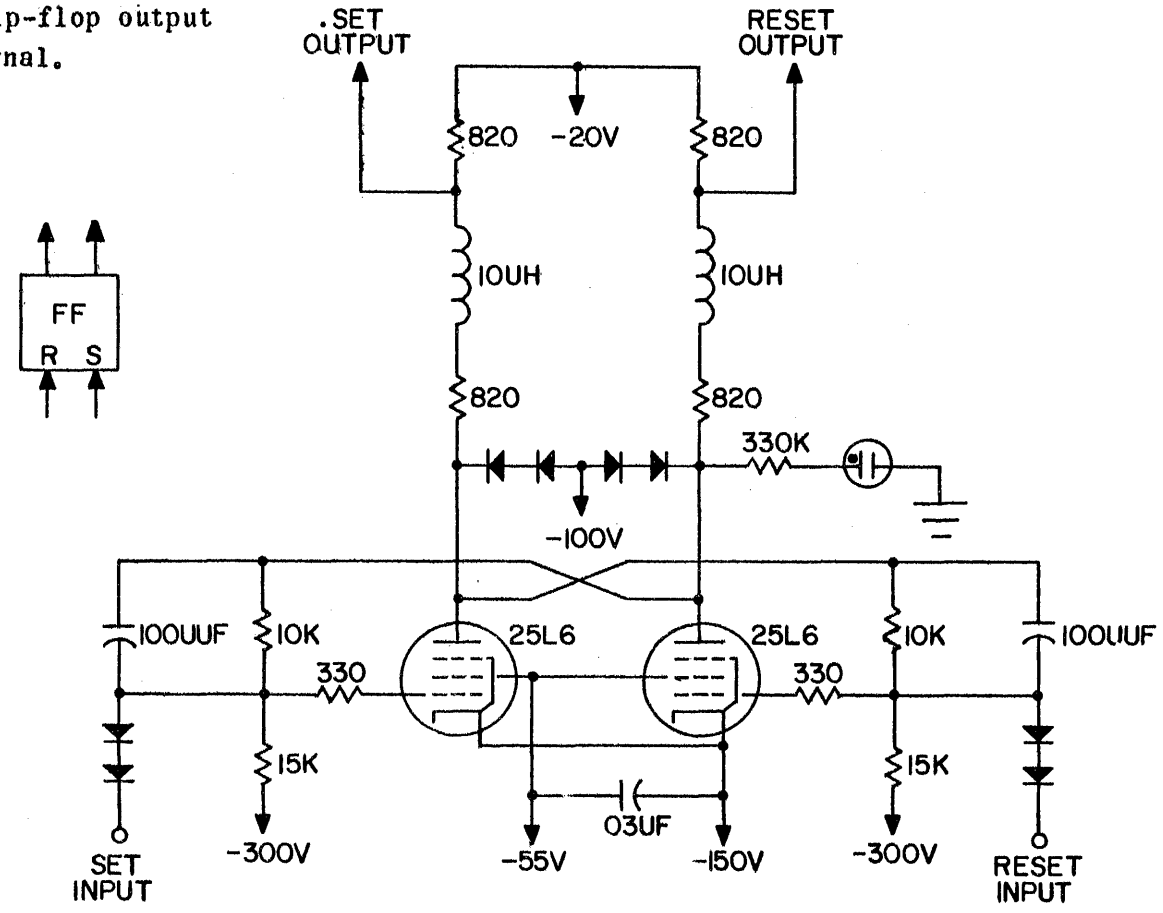


Figure 3-7. Typical High Speed Flip-Flop Circuit .08 μsec

(2) MEDIUM SPEED FLIP-FLOPS. - Medium speed flip-flops have a switching time of less than 5 μsec. The two halves of a medium speed flip-flop are either two 7AK7 vacuum tubes or one 28D7 dual pentode. The 28D7 medium speed flip-flop can supply relatively large amounts of power to succeeding circuits. Figure 3-8 presents, schematically, a typical medium speed flip-flop.

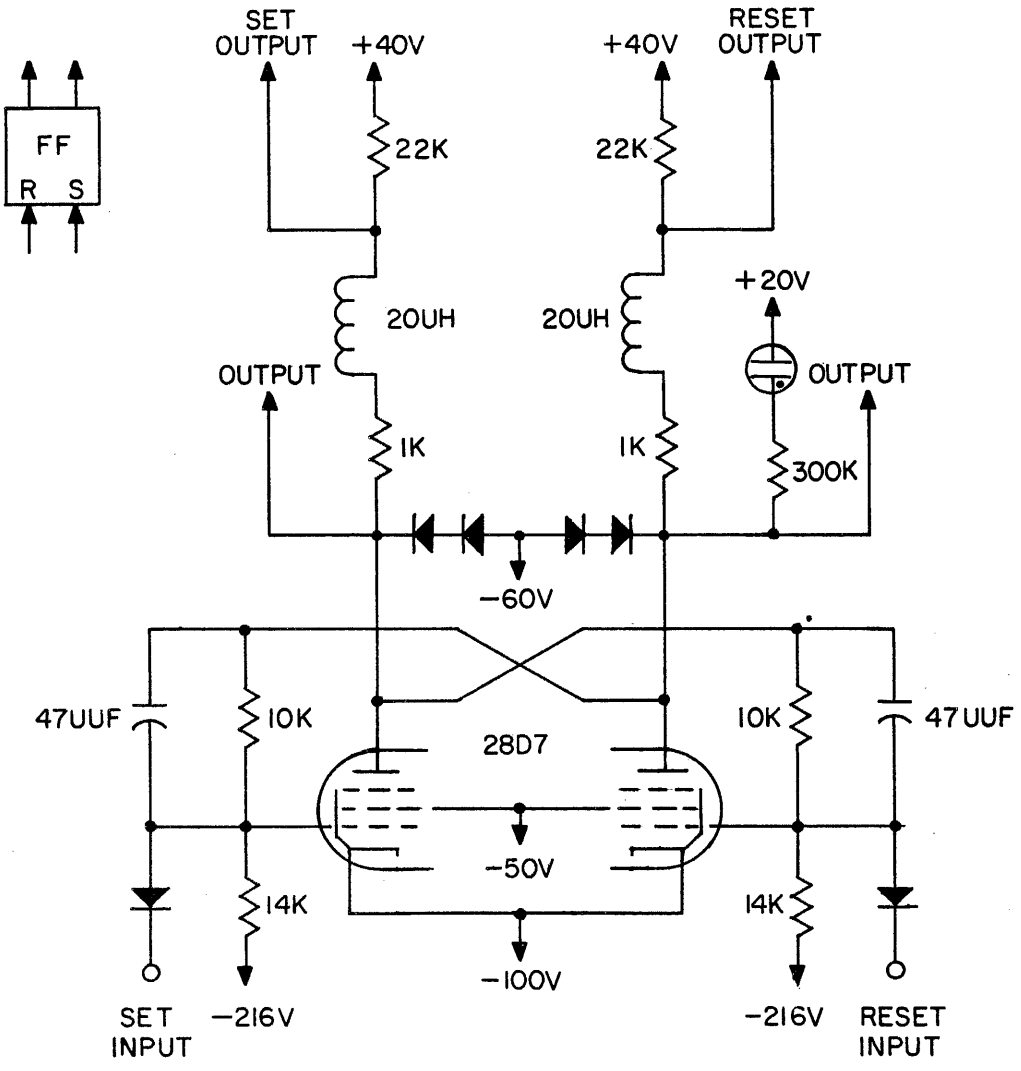


Figure 3-8. Typical Medium Speed Flip-Flop Circuit 2-4 μsec

(3) LOW-SPEED FLIP-FLOPS. - The switching time of the low-speed flip-flop is somewhere in the order of 20 μsec. The two halves of the low-speed flip-flop consists of two 6BE6 vacuum tubes. Figure 3-9 presents, schematically, a typical low-speed flip-flop.

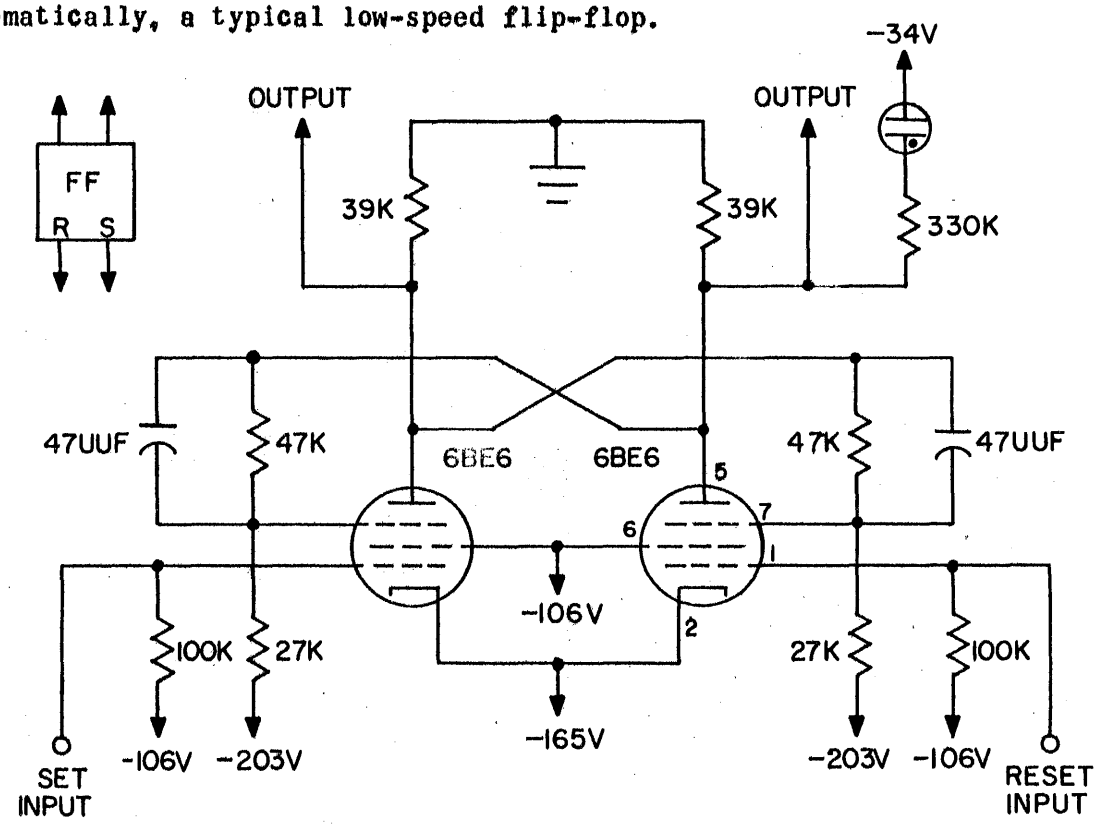


Figure 3-9. Typical Low Speed Flip-Flop Circuit -20 μsec

d. PULSE FORMERS. - The pulse former, PFR, is a device used to reshape decaying pulses and to restore exact computer timing to pulse trains or control signals. The PFR consists of a vacuum tube driver, a clock gate, and a high-speed flip-flop. A schematic diagram of a typical PFR is presented in Figure 3-10. The PFR shown responds to negative-going input pulses. Biasing the driver tube properly will make the PFR respond to positive input signals.

The PFR in Figure 3-10 is shown in the normal condition, i.e., there is no signal on its input and the FF section is in the "reset" state. With no input

signal the driver tube conducts holding its plate voltage to a clamped -88v. The potential of the control grid of V2 is held by the voltage divider action of the 18K and 31.7K resistors at approximately -90v. These two levels control the clock gate to the extent that there is no output from the section receiving TP+'s. Thus, the FF is maintained in the "reset" state. TP-'s will appear on the grid of V2, but since V2 is already cut off, they will have no effect on the status of the flip-flop.

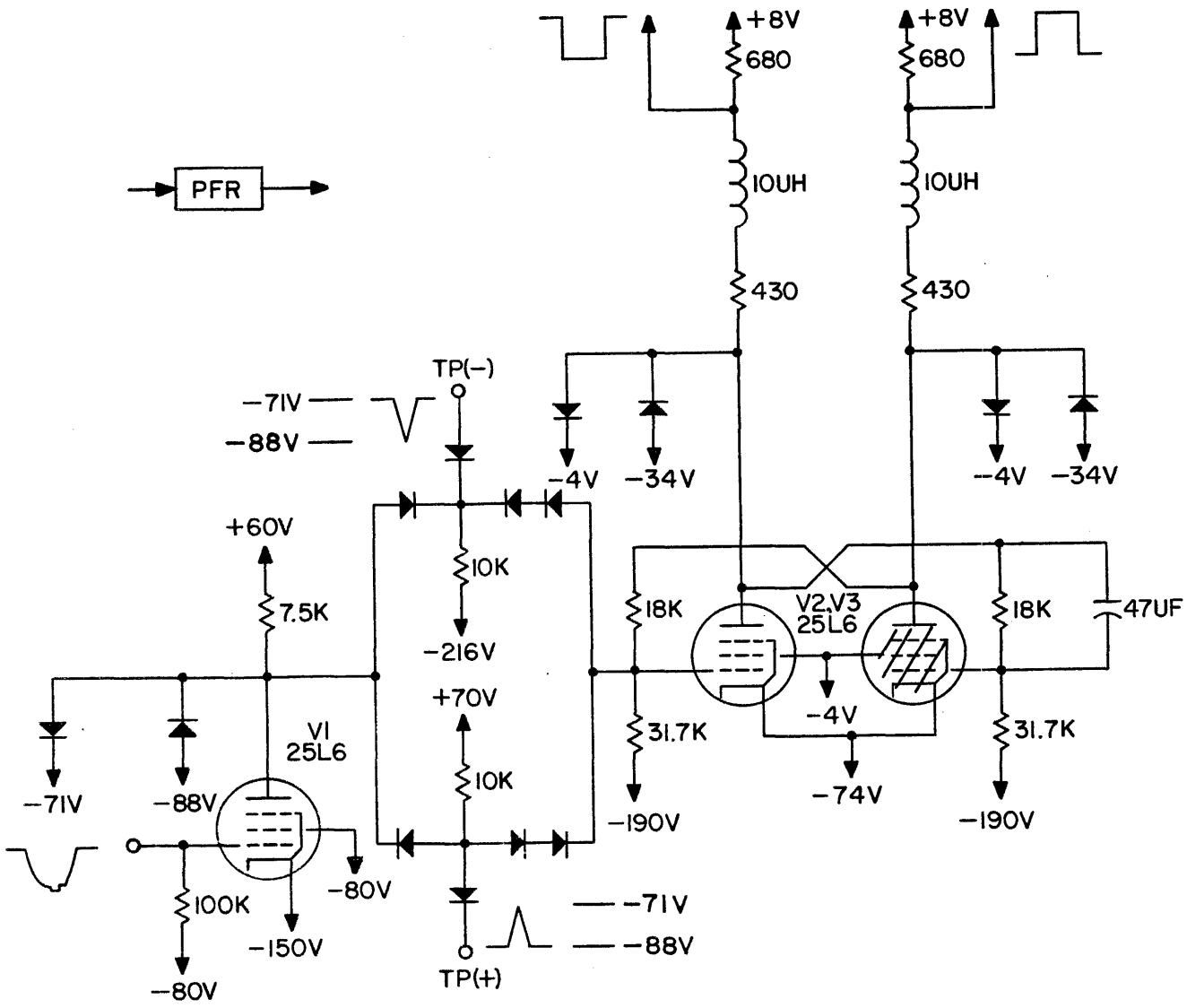


Figure 3-10. Schematic Diagram, Typical Pulse Former

The presence of the signal (negative-going) on the input to the PFR causes the driver tube to cease conduction. This raises the plate potential of V1 to the clamped level of -71v. This voltage alerts the positive section of the Clock Gate to rise to -71v upon the occurrence of the next TP+. This rise in potential appears on the control grid of V2 causing it to conduct. Normal flip-flop action cuts off V3. The -71v plate potential of V1 keeps the negative section of the Clock Gate inoperative, thus the TP-'s cannot affect the condition of the FF section of the PFR.

When the signal on the PFR input disappears, V1 again conducts, bringing its plate voltage down to -88v. The -88v level disables the positive section of the Clock Gate and it alerts the negative section. The next TP- will lower the voltage level of the control grid of V2 to -88v. This causes the FF to change state back to the original or normal condition.

Since the switching time of the FF section of the PFR is in the order of .08 μsec, and since both the upper and lower levels of the outputs are clamped, the signal output of the PFR can be considered a square wave whose leading and trailing edges are in exact timing with pulses from TPG. The PFR will reshape any decayed pulses applied to it; however, its prime function is to keep signal or information flow in synchronism with computer timing. Since the TP's which operate the FF follow the signal input to the PFR, there is a delay between the signal in and the signal out. Logically the PFR is treated as a delay with a period of one-half pulse time.

e. BINARY COUNTERS. - The Binary Counter, BC, is a bi-stable device which is used as a radix two counter. BC has only one input, but it changes state each time a pulse appears on this input. One BC indicates whether it has received an odd or even, 0 or 1, number of stepping pulses. BC is provided

with a carry pulse which may be supplied to a successive BC thereby increasing the maximum number of input pulses which may be accurately recorded. Figure 3-11 presents a schematic diagram of a typical Binary Counter. Vacuum tubes V1 and V2 form the bi-stable section and V3 is a Cathode Follower trigger tube for the counter.

The BC in Figure 3-11 is shown in the "1" condition. There is no input on V3, V1 is cut off and V2 is conducting. The crystal diodes between V3 and the plates circuits of both V1 and V2 are not conducting since the plate potentials of both tubes are below the cathode potential of V3 (-95V and -150V, respectively, vs. -90V). In this situation, the coupling capacitor between the plate of V2 and the control grid of V1 has a charge of approximately 60V and the coupling capacitor between the plate of V1 and the control grid of V2 is charged to approximately 95V. When the negative-going input signal of 65V, amplitude is applied to V3, the diodes between V3 and the flip-flop section conduct forcing the plate potential of both tubes down to about -155V. This lowers the reference potential of the charges on both coupling capacitors. Thus, when the input pulse disappears and the plate potentials tend to rise together, V1 will be driven into conduction first since its grid potential is at a higher level because of the original smaller charge on its control grid capacitor. When V1 conducts, V2 is held cut off by normal flip-flop action. The next input pulse (negative going) into V3 causes the routine to repeat itself except that the situation in the counters is reversed and as a result V2 conducts and V1 is cut-off.

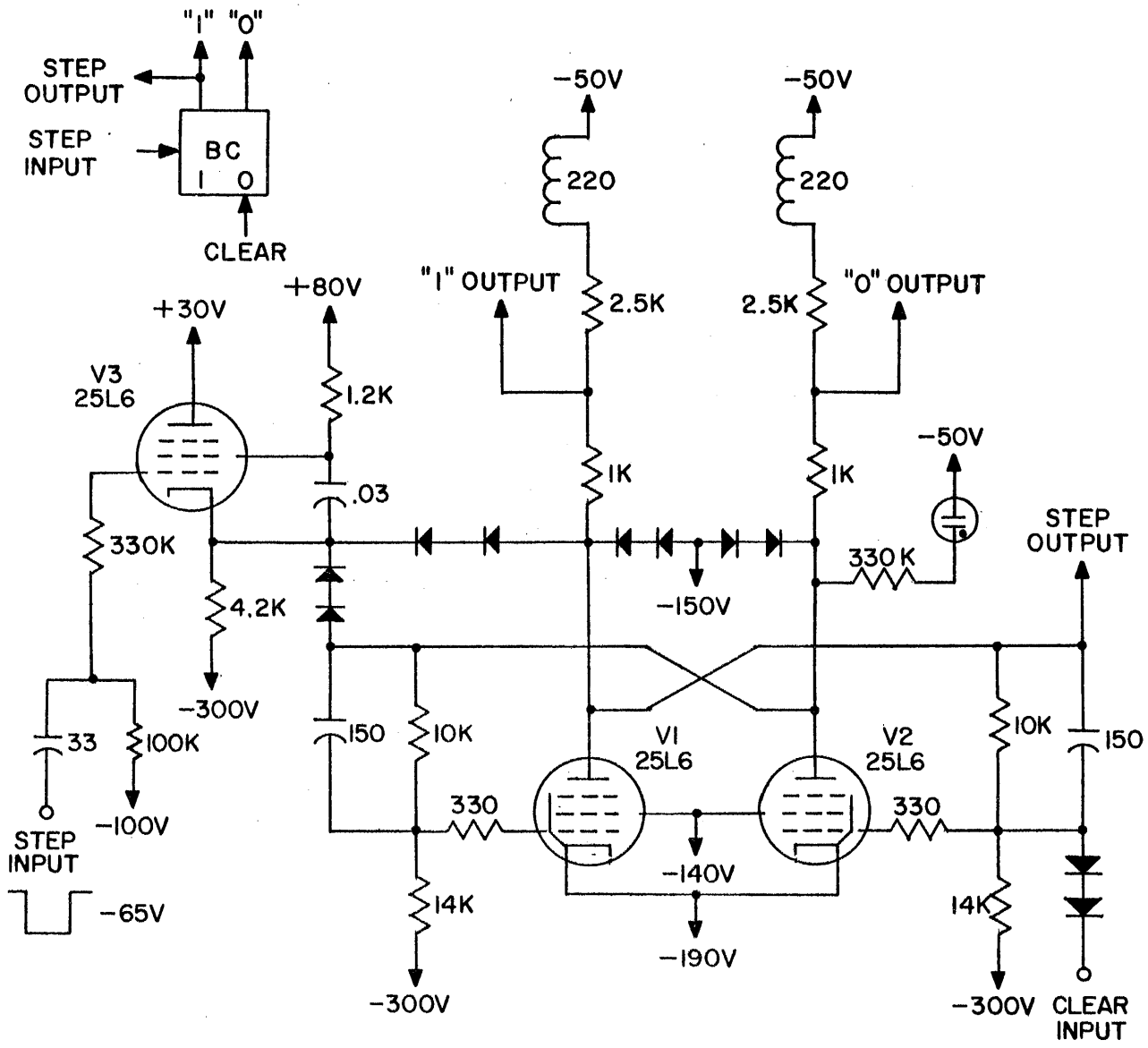


Figure 3-11. Schematic Diagram, Binary Counter

Outputs are provided from both the "0" and the "1" sides of the BC. In addition, the "1" side supplies an output which is connected to the next counting stage. This output supplies a stepping pulse to the next stage when BC is pulsed to the "0" state.

NOTE

THE STEPPING PULSE OUTPUT OF THE BC WILL PASS BOTH POSITIVE- AND NEGATIVE-GOING SIGNALS AS THE BI-STABLE SECTION OF BC CHANGES STATE. HOWEVER ONLY THE NEGATIVE-GOING SIGNAL WILL HAVE ANY EFFECT ON THE NEXT STAGE BECAUSE OF THE ISOLATION PROPERTIES OF THE CRYSTAL DIODES FOLLOWING THE CATHODE FOLLOWER TRIGGER TUBE.

Most BC's are provided with a CLEAR input. This permits the operator to force the BC's to "0" by depressing the proper switch on SC.

f. DELAY FLOPS. - The delay flop, DF, is similar to the flip-flop except that it has only one input and it resets itself at a predetermined time after it has been put into the "set" condition. The automatic resetting is controlled by circuit design. Figure 3-12 presents a schematic diagram of a typical delay flop. This delay flop has a period of 50 milliseconds.

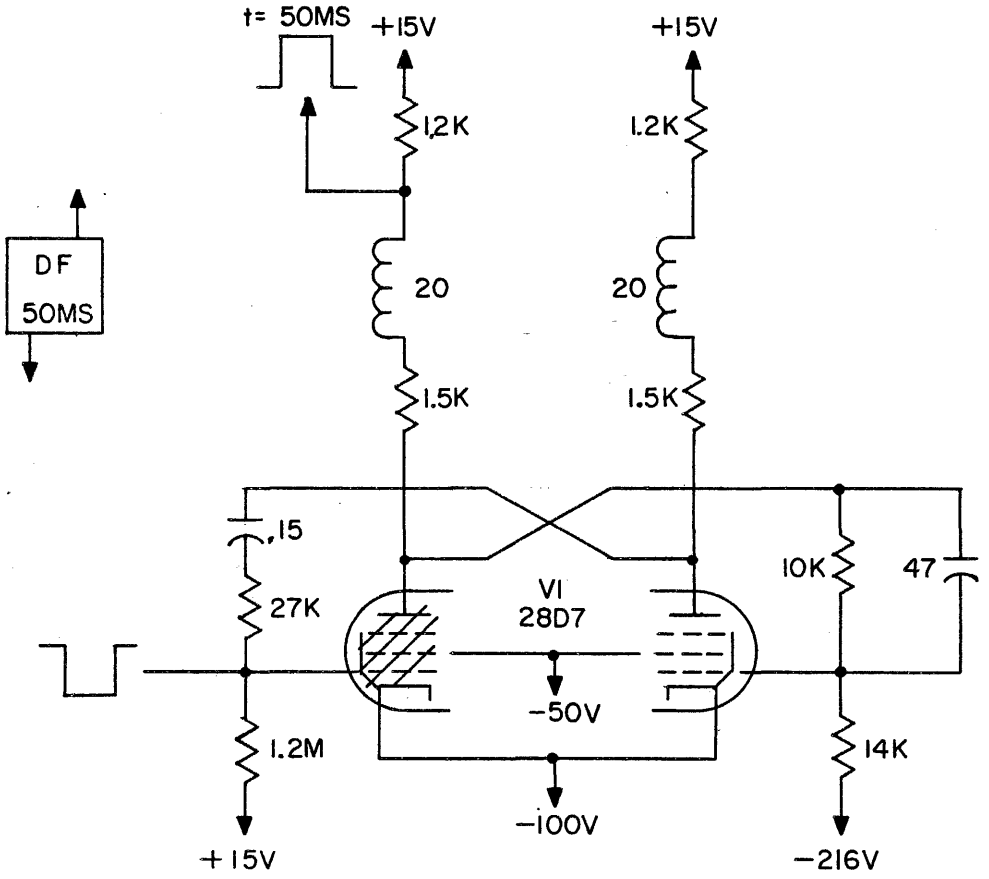


Figure 3-12. Schematic Diagram; Delay Flop - 50 Millisecond Delay Period

When a negative going signal appears on the input to DF, normal flip-flop action causes the conducting side to cut off and the non-conducting side to conduct. The change in the plate potentials applies a charge on the .15 μf capacitor which is in the control grid circuit of the input side of the DF. The time constant of the RC network involving the .15 μf capacitor and the 27K resistor is such that after 50 milliseconds have elapsed the capacitor will be charged to potential which is sufficiently positive to cause the DF to switch back to its original state.

Figure 3-13 presents another type of delay flop. This DF uses a twin triode 6SN7 vacuum tube. Normally the 15K cathode resistor keeps the cathode potential at about +65V, well above the +20V control grid potential of the input half of the DF. The input side is therefore normally cut-off. The high plate potential of the input side holds the control grid of the other side sufficiently high for it to conduct.

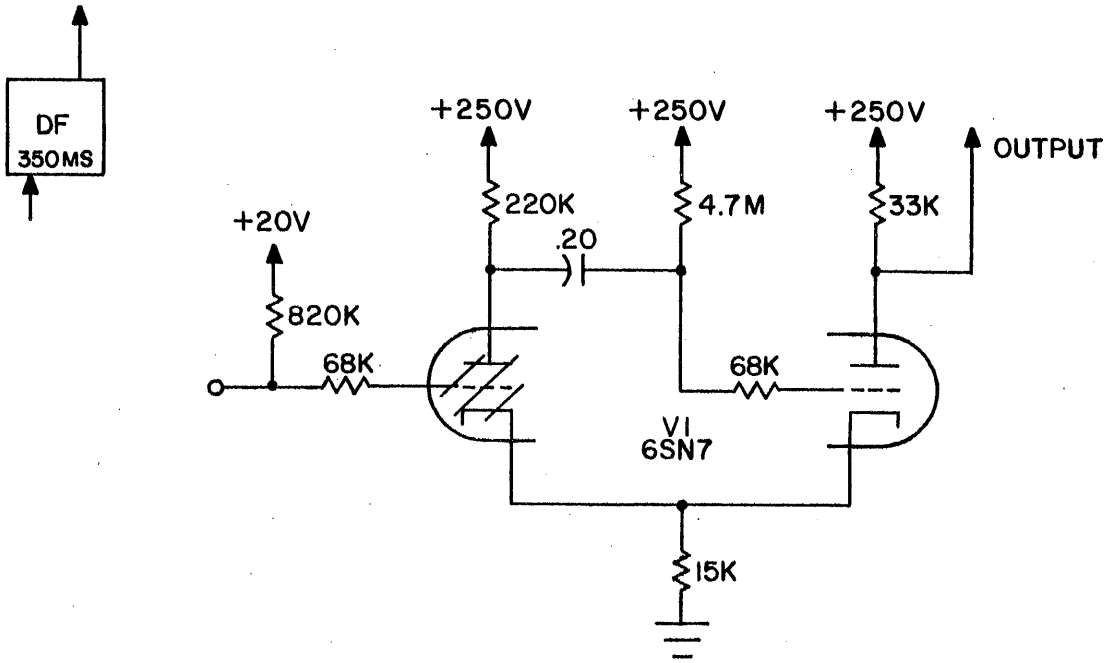


Figure 3-13. Schematic Diagram, Delay Flop - 350 Millisecond Delay Period

A sufficiently positive signal applied to the DF causes the input side to conduct. The plate voltage of this side drops from approximately +250V to about +40V. This drop is apparent on the control grid of the normally conducting side and causes it to cut off. The DF will remain in this condition until the .2 μf capacitor, drawing current through the 4.7M resistor, charges up to 250V. The time constant for this RC network is 350 milliseconds. The output of this DF is supplied by the normally conducting side.

g. THYRAFLOPS. - The thyraflop, TF, is a normally non-conducting thyratron which, when pulsed, produces an output for a predetermined period. The period of the thyraflop begins with the receipt of the input signal. This is true even if it has not recovered from the previous signal. Thus the thyraflop is referred to as a "retriggerable" delay element. Thyraflops are used frequently in the input circuits to DF's. This combination is referred to as the retriggerable delay flop, RDF, since the TF will hold the DF in its unstable state as long as TF continues to receive input signals. Figure 3-14 presents the Thyraflop circuit schematically.

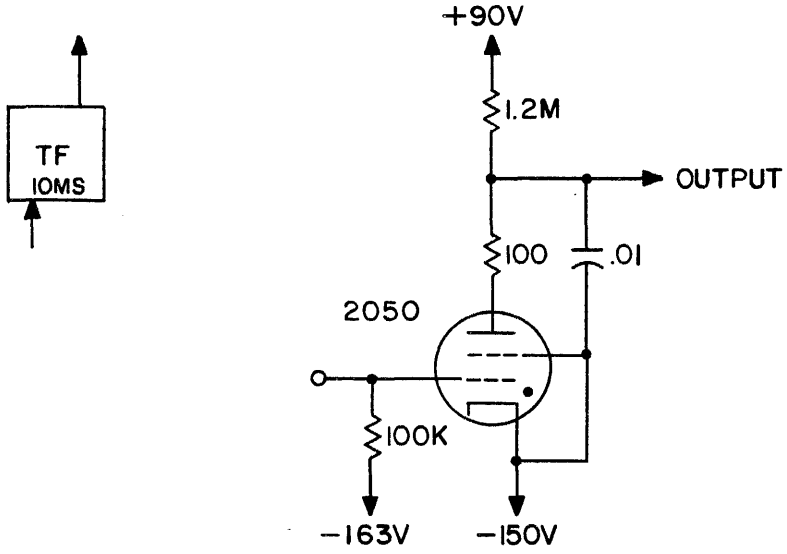


Figure 3-14. Schematic Diagram, Typical Thyraflop, 10 Millisecond Delay Period

A positive going pulse of approximately 60V amplitude on the control grid causes the thyratron to conduct. The plate potential drops from +90V to about -142V. When this occurs the .01 μf plate-cathode coupling capacitor which had an original charge of 240V immediately discharges to about 8V. This produces a negative-going signal on the thyraflop output of 232V amplitude. The -142V plate potential is not enough to maintain conduction and the thyratron cuts off. When the thyratron cuts off, its plate potential rises to +90V. The .01 μf capacitor draws current through the 1.2 M resistor until it is charged to 240V. The RC time constant is such that the .01 μf capacitor is fully charged 10 milliseconds after the thyratron is cut off. Thus the output of the circuit is a negative-going pulse, with an amplitude of 232V and a minimum duration of 10 milliseconds.

If the thyratron is fired while the .01 μf.capacitor is charging, it immediately discharges and the recovery period begins anew. For this reason the thyraflop is referred to as a retriggerable device.

h. RESISTOR-COMPARATOR CIRCUITS. - The Resistor-Comparator, RCP, is primarily a checking device. It recognizes the presence of two or more signals on its several inputs. Less than two input signals has no effect on the output condition of RCP. A typical RCP circuit is presented schematically in Figure 3-15.

The operation of RCP is dependent upon the voltage divider action between the potential of the input lines which are in the signal condition and the potential of the unselected inputs. Normally the potential of all inputs is held at -25V. This holds point A, and therefore the control grid of the 6SN7 output vacuum tube at -25V. The -25V control grid potential is far enough below the cathode potential, approximately -19.7V, to hold the vacuum tube non-conducting.

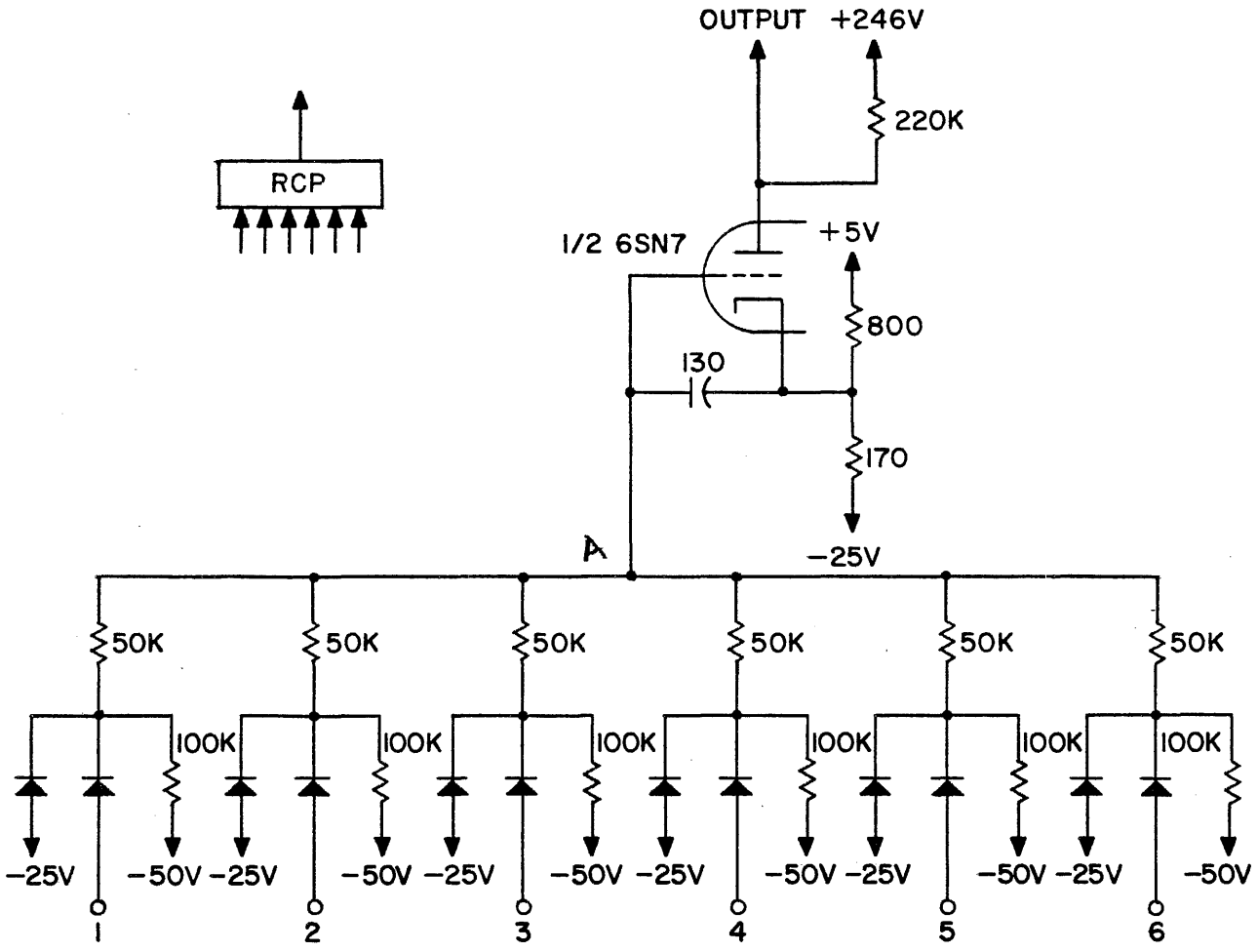


Figure 3-15. Schematic Diagram, Typical RCP

If a signal appears on one input, e.g., Input 1, its potential rises to +5V. The voltage divider action between +5V, across the 50K resistor on Input 1 and -25V across the 5-50K resistors in parallel of the other inputs raises the potential level of point A to approximately -20V. This is not enough to cause the vacuum tube to conduct. However, if signals appear on two of the inputs, the voltage divider action is between +5V, across a 50K resistor and -25V and only 4-50K resistors in parallel. As a result the potential of point A uses to -19V, enough to cause the vacuum tube to conduct

and produce the output signal condition from RCP. A similar situation exists if more than two of the inputs are selected.

i. DELAY ELEMENTS. - Ordinarily the transit time for an electrical effort through a conductor is too short to realize any practical storage capacity. Therefore means are devised to effect the space-time relationship necessary to preserve or retard serially moving information. Univac II utilizes two types of serial storage or delay elements, viz., the Short Mercury Tank or acoustic delay group and the electrical delay line.

(1) SHORT MERCURY TANK DELAY GROUP. - The Short Mercury Tank delay group is used where a relatively long delay with no tap-offs is required. It provides the main delay for the register elements. The delay in the short tank is effected by the slow transit time of an acoustic pattern of impulses through a column of mercury. The column of mercury together with its associated circuitry is referred to as the Main Delay Group, MDG. The circuit diagram of an MDG is presented in Figure 3-16.

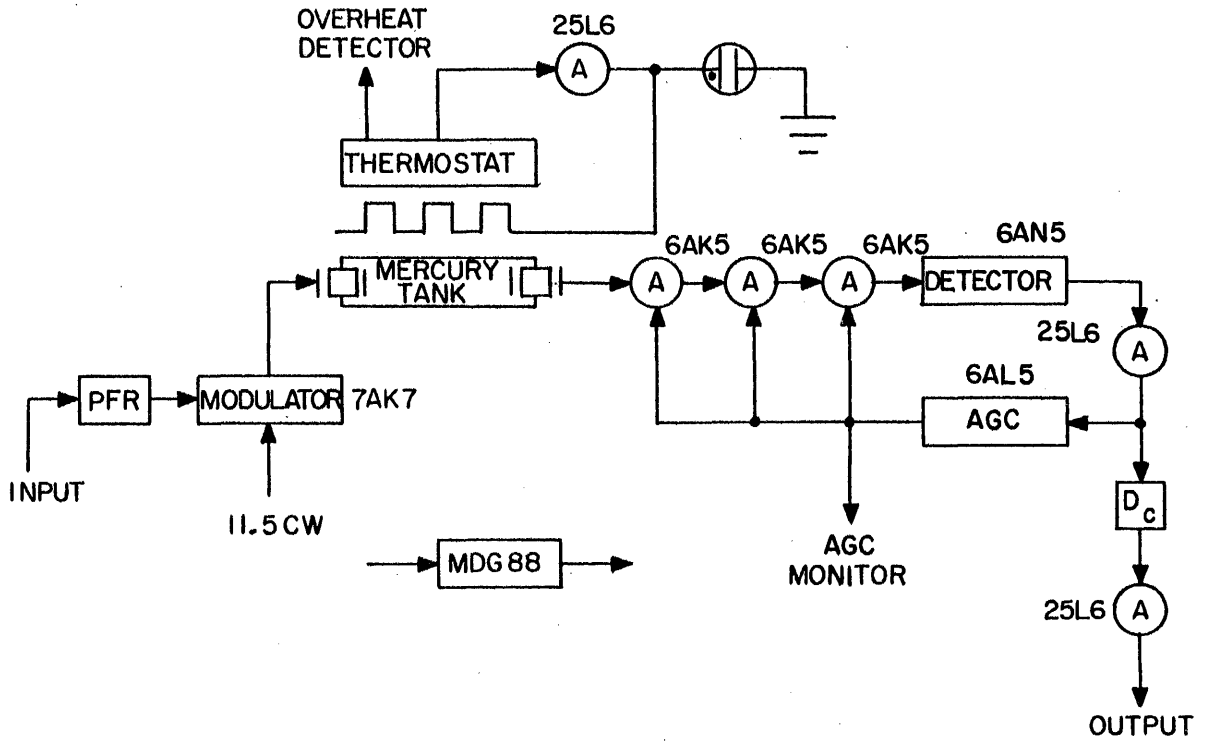


Figure 3-16. Short Mercury Tank Delay Group

The pulse train enters MDG through a PFR. The properly shaped and timed pulses are impressed on a 11.5 mc continuous wave by a 7AK7 modulator circuit. The modulated wave is applied to a transducing crystal which is in direct contact with the mercury column in the mercury tank. The acoustic wave pattern thus generated is beamed towards a receiving crystal at the other end of the mercury column. This crystal re-enters the wave pattern into the electrical circuitry. The modulated wave passes through three stages of amplification after which it is applied to a detector. The detector separates the pulse train from the continuous wave. The pulse train is amplified, adjusted to proper timing by an electrical D_C and amplified again; then it passes through the output of the MDG. AGC is provided between the detector and the three amplification stages following the mercury tank.

The tolerance of the mercury tank delay is acceptable while it is held at a temperature of between 62°C and 65°C. This temperature is maintained by a heating coil which is under control of a thermostat. When the temperature falls to 62°C, a signal is supplied from the thermostat to the control grid of a 25L6 amplifier tube, causing it to conduct. When this amplifier conducts it draws current through a coil which is wound around the mercury tank causing the necessary heat to be generated to maintain proper temperature. When the amplifier conducts, a neon on SC lights indicating heat is being applied to the particular mercury tank.

(2) ELECTRICAL DELAY LINES. - A transmission line involving a series of LC circuits requires a longer transit time by an electrical impulse than a straight wire. The total delay of such a line is dependent upon the number of LC circuits within it. The schematic presentation of an electrical delay line is shown in Figure 3-17. The input to the delay line has an impedance

compensating circuit composed of a coil, a resistor and a capacitor. This matches the impedance characteristics of the delay line with the plate circuit of the vacuum tube driver supplying the input signal. The delay line is terminated with a resistor and capacitor connected in parallel to prevent the reflection of any signal back into the delay line. The output of the delay line may be taken from any tap following an LC section, depending on the delay requirements of the circuit in which it is contained.

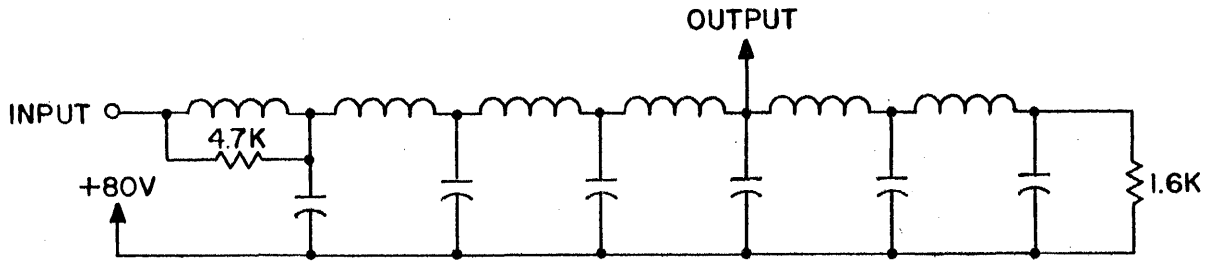


Figure 3-17. Electrical Delay Line

j. TIMING PULSE GENERATOR AND TIMING PULSE DRIVERS. - The Timing Pulse Generator (TPG) is a master oscillator which generates the standard timing pulses (TP's) for all circuits in the computer. The timing pulses from TPG occur at a 2.25 megacycle frequency, are .08 μseconds wide and have a 70V amplitude. Basically, the TP generation system operates as follows: a master oscillator produces a 2.25 mc sine wave; this sine wave is applied to a ringing circuit which produces a damped wave of a higher frequency; the damped wave enters a clipping circuit which passes only the first positive pulse; this pulse which is .08 μseconds wide and occurring at a frequency of 2.25 mc is supplied to a group of ten Clock Gate Drivers for distribution to the various circuits.

The TP generation system is presented schematically in Figure 3-18. The oscillator circuit composed of a 2.25 mc crystal and vacuum tube V1, produce a

pure sine wave. This sine wave is applied to the control grids of V4. Since V4 is biased well beyond cut-off, it is driven into conduction by only the positive-going sections of the sine wave. When V4 conducts, oscillations are produced in the 1 μh choke ringing section of the plate circuit. These oscillations are a damped wave, which is regenerated in synchronism with the positive sections of the original sine wave. The damped wave is applied to the control grids of the clipping tube V5. The low bias on this tube permits it to respond to only the first positive-going portion of the damped wave. The output of the clipper tube contains a transformer which changes the high voltage-low current vacuum tube output into a low voltage-high current signal. The output of the transformer is a succession of positive-going master timing pulses .08 μseconds wide, with an amplitude of 70V (-125V to -55) and occurring at a 2.25 mc rate. These pulses are communicated to the ten Clock Gate Driver circuits for distribution to the various computer elements. The master timing pulse is also applied to an AGC circuit for TPG. The signal enters the plate circuit of diode vacuum tube V6 via a 3300 $\mu\mu$f capacitor. V6 is normally held cut off by the -60V plate potential acquired by the voltage divider action between the -40V and the -74V. When the rise in its plate potential is sufficient, V6 conducts. The change in cathode potential raises the bias on amplifier V7. The output of V7, a negative-going signal, is applied to the screen grid of V5, reducing the gain of the clipper tube.

TUNING PROCEDURE

Adjust variable capacitor Ⓒ to produce a minimum voltage reading (node) at the screen grid of V5, point Ⓐ.

A typical Clock Gate Driver circuit is presented schematically in Figure 3-19. The master timing pulse from TPG is transmitted via a coaxial line to

(Continued on Page 91)

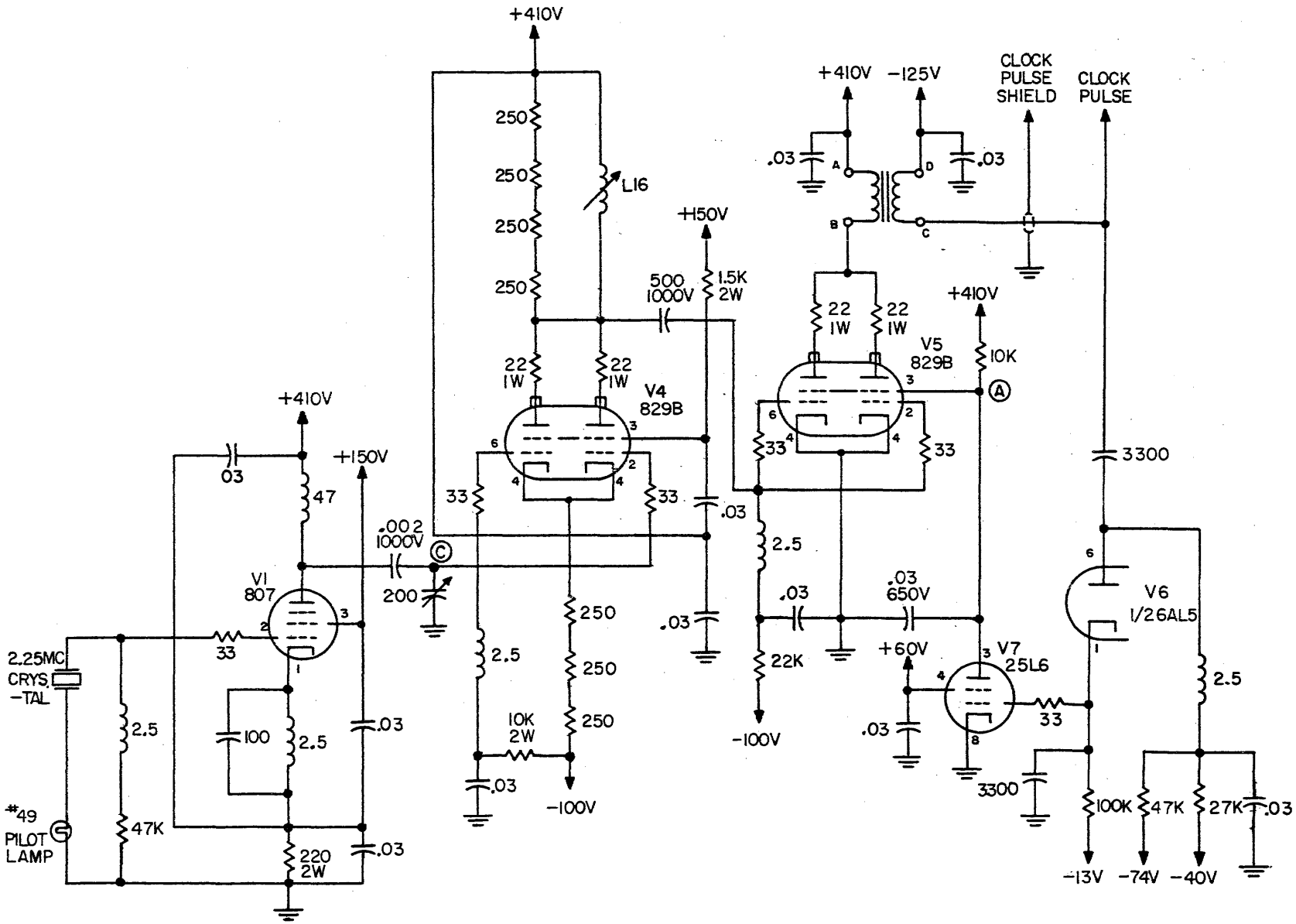


Figure 3-18. Schematic Diagram, Timing Pulse Generator

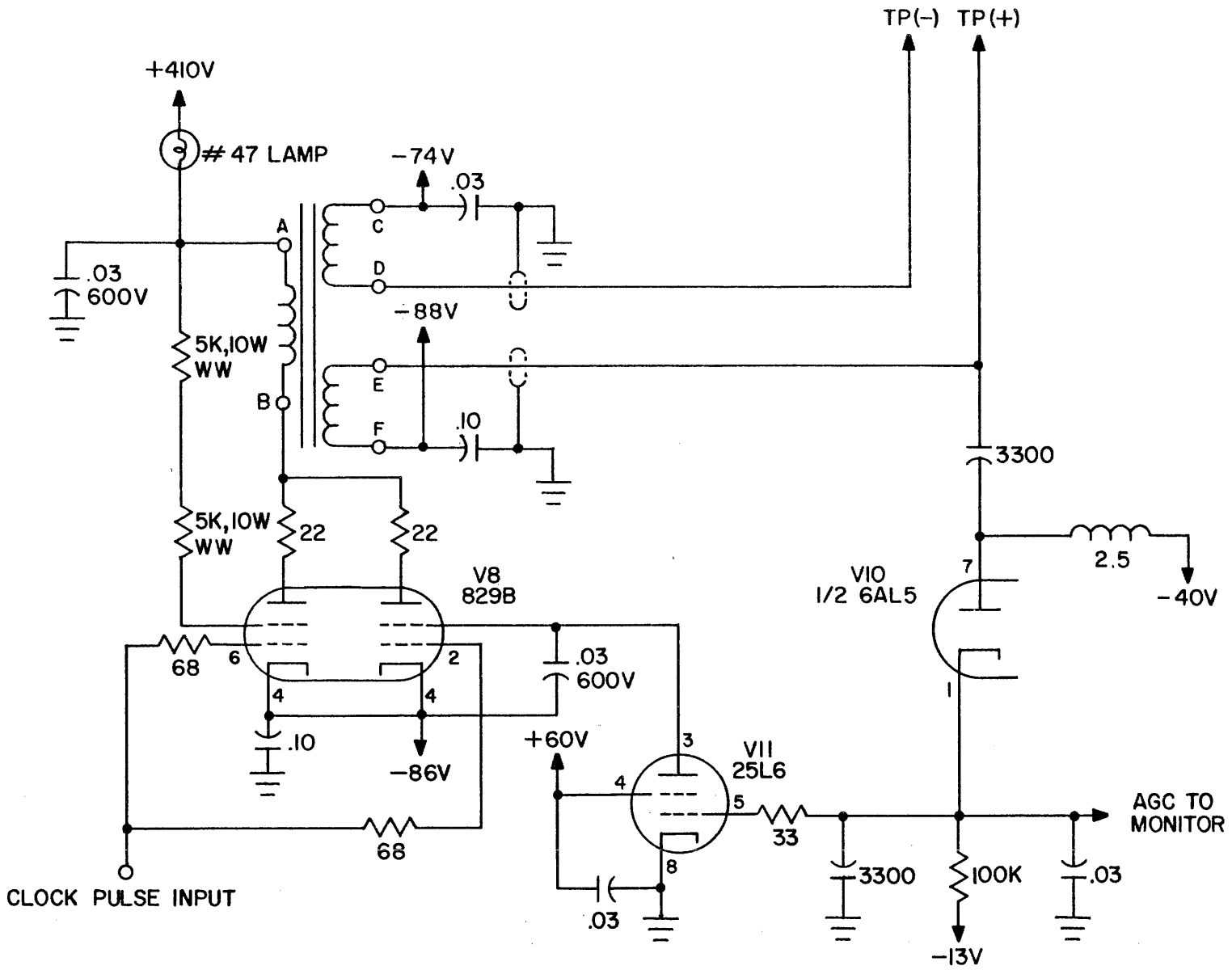


Figure 3-19. Schematic Diagram, Typical Clock Gate Driver

(Continued from Page 88)
the 9 Clock Gate Drivers. Each Clock Gate Driver consists of a voltage amplifier, a pulse transformer, and an AGC circuit. The pulse transformer has a double secondary which permits the selection of both positive and negative going TP's. The outputs should have a swing of approximately 38 volts (positive or negative) from their reference voltage. The Clock Gate Driver AGC reduces the voltage on the screen grid of the voltage amplifier tube in proportion to the level reached by the rms voltage of the TP+ section of the pulse transformer. An output from the AGC section is connected to a video monitor on SC. This permits the operator to check the performance of the Clock Gate Driver circuits in as much as the condition of the vacuum tubes determines the AGC developed. Switches on SC provide the means for selecting the AGC voltage to be monitored, which should be negative, but not exceeding -9 volts.

k. ADDERS. - Any device which reacts to input pulses to produce an output in a manner which corresponds to the performing of binary addition is termed an adder. Binary addition is accomplished according to the following laws:

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 0, \text{ carry } 1$$

This is the modus operandi of the adder; but with a signal condition substituted for a "1" and a no signal condition for a "0" in the equations.

There are three basic adder circuits in the computer: the Quarter Adder, the Half Adder and the Full Binary Adder. All three react to input pulses in the same fashion, their difference, logically, lies in how they are equipped to handle the carry pulse situation. The quarter adder does not generate a carry pulse; the half adder can produce a carry pulse; and the full adder not only produces a carry pulse, but it also accommodates a carry pulse from its previous addition, combining it together with the signals appearing on its addend and augend inputs into the sum.

(1) QUARTER ADDERS. - A typical quarter adder, QA, is presented schematically in Figure 3-20. The basic element of QA is a 28D7 twin pentode vacuum tube. Both halves normally conduct. The plate potentials of both sides are held by clamping action at +220v; the cathode potential at point B is approximately +200v; and the potential at point C, the output of QA, as a result of voltage divider action, is approximately +190v. When a positive going signal is applied to one of the control grids, but not to the other, its associated side conducts more heavily. The plate potential of the addressed side cannot drop because of the +22v lower limit clamping circuit. However, this heavier conduction will raise the voltage at point B to about +21v. The rise in cathode

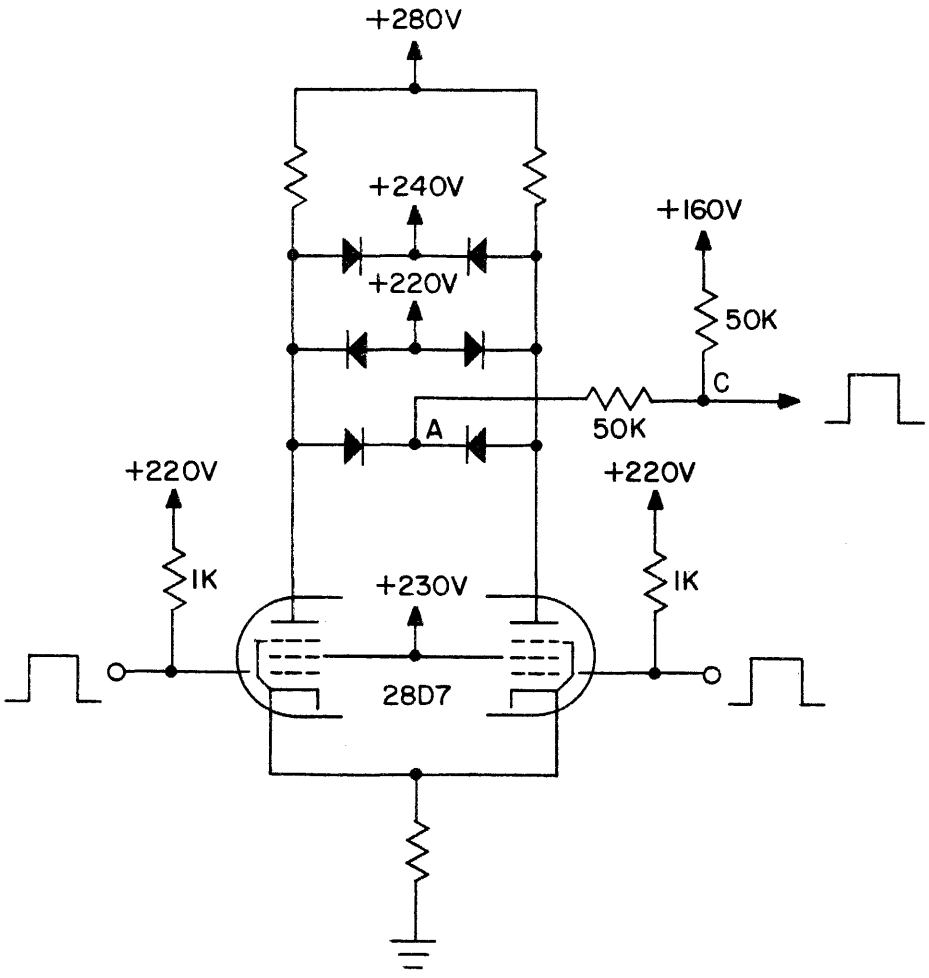


Figure 3-20. Typical Quarter Adder

potential is also apparent on the other side of the vacuum tube, and as a result, there is a decrease in the potential difference across this side. This tends to drive the unaddressed side to non-conduction, causing the plate potential to rise to the upper clamping limit of +240v. Point A follows this voltage rise and as a consequence, point C will rise to about +200v. The output of QA is, therefore a positive going signal of about 10v amplitude.

If both control grids of QA receive input signals simultaneously, both sides will attempt to conduct more heavily. This will attempt to raise the cathode potential, which in turn will cause both sides of QA to conduct less heavily. The two actions will, in effect, cancel each other and there will be no change in the output condition of QA.

(2) HALF ADDERS. - A Half Adder, HA, is an arrangement of "OR" and "AND" gates which will produce an output from signals on its two inputs in accordance with the laws of binary arithmetic. Provision is made in HA to produce a carry signal for the situation 1 + 1 = 0, carry 1. Figures 3-21 and 3-22 present, schematically, two types of half adders.

Points A, B and C on both schematic diagrams correspond, respectively, to points A, B and C on the logical diagram of HA presented in Figure 3-23. A signal at point B is the CARRY signal since it is generated only in the 1 + 1 condition. A half adder is so called because it requires an arrangement of two half adders to make a full adder. An inverter on the SUM output corrects the polarity of the SUM signal.

(3) FULL ADDERS. - The schematic diagram of a full Binary adder is presented in Figure 3-24. The Full Adder is able to combine any sequence of binary digits or signals, appearing on its three input lines simultaneously, and to supply a carry, if required, to the next binary place. The additions the Full Adder is capable of performing may be illustrated in the following manner:

(Continued on Page 97)

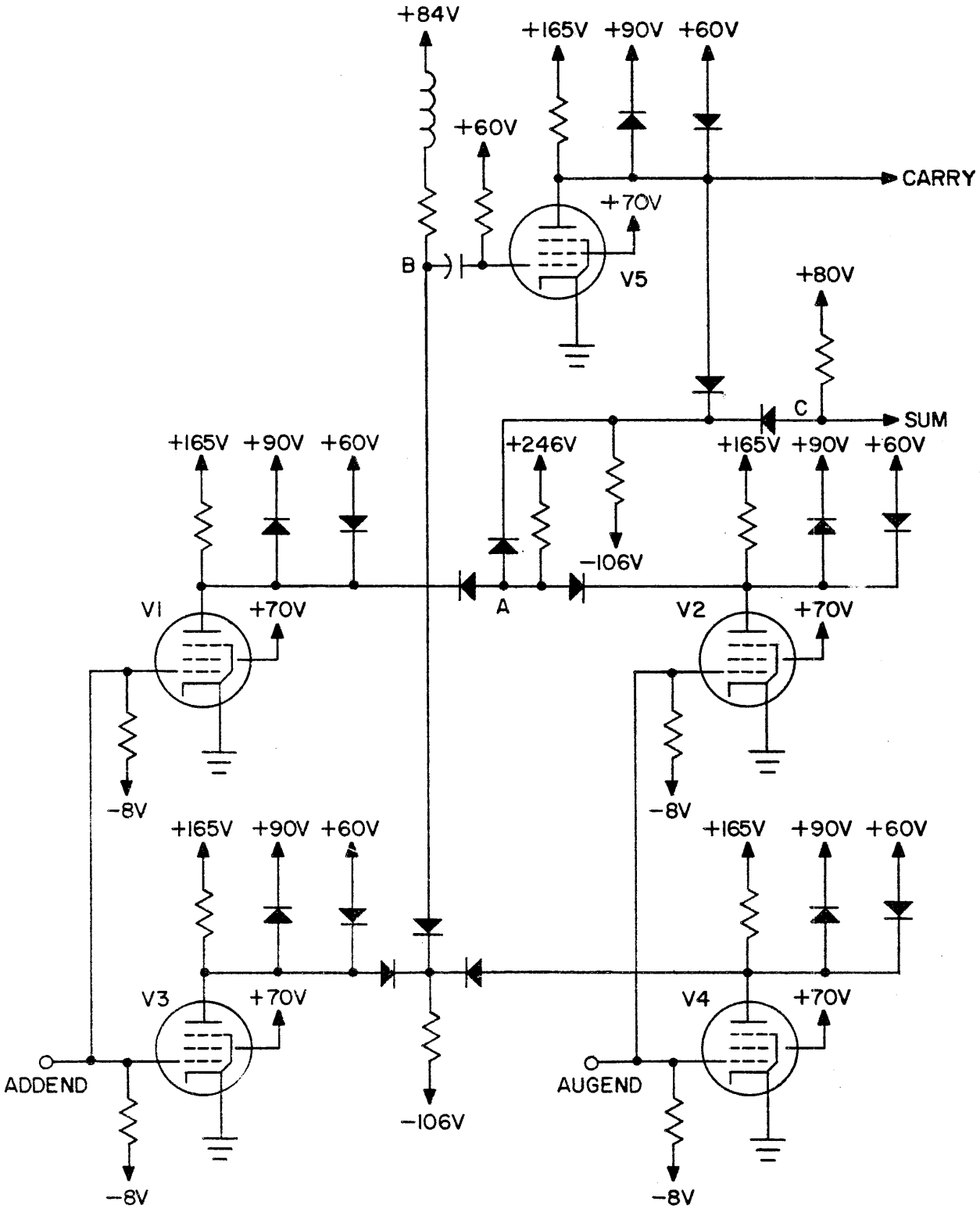


Figure 3-21. Typical Half Adder, Type I

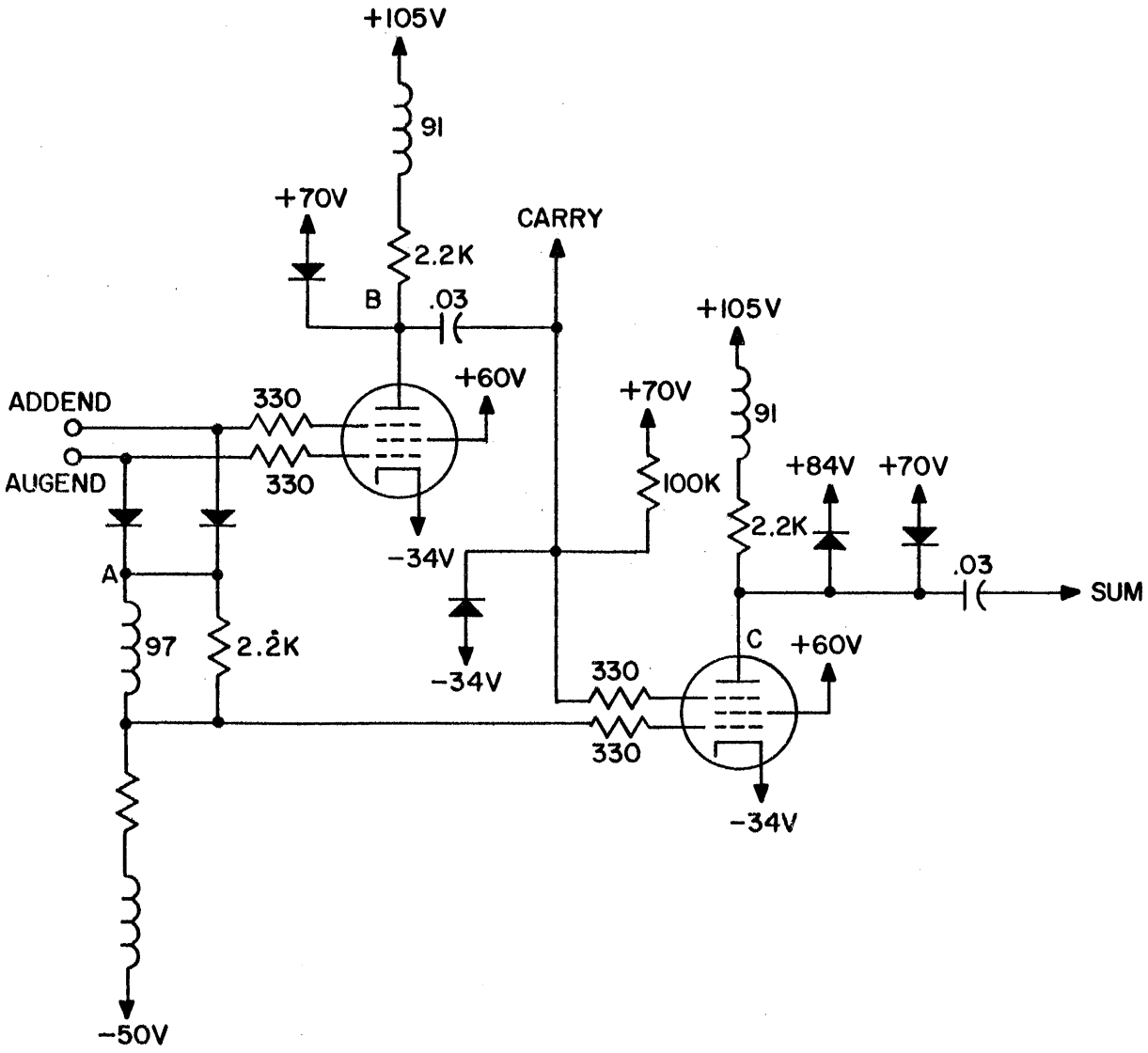


Figure 3-22. Half Adder, Type II

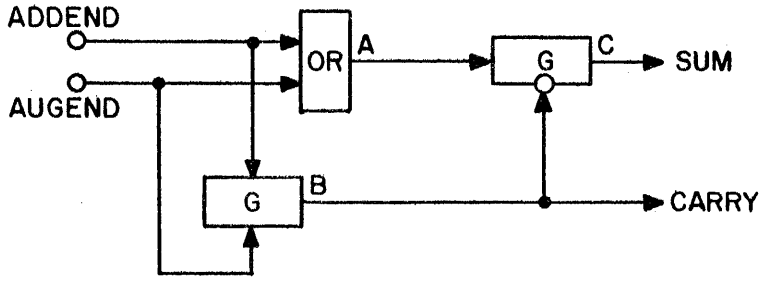


Figure 3-23. Logical Diagram, Half Adder

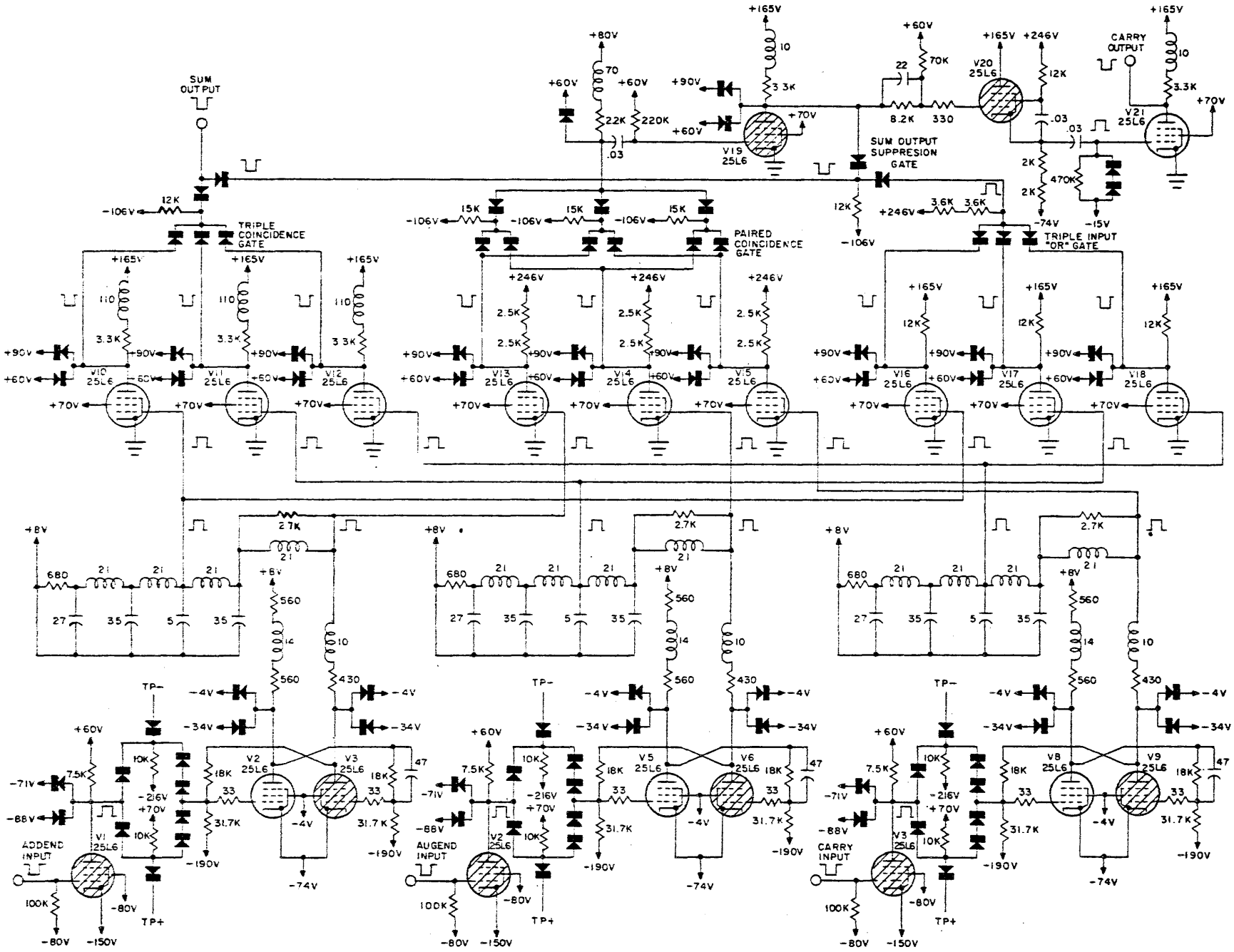


Figure 3-24. Schematic Diagram, Full Adder

(Continued from Page 93)

ADDEND	0	0	0	1	0	1	1	1
AUGEND	0	0	1	0	1	0	1	1
CARRY	0	1	0	0	1	1	0	1
SUM	0	1	1	1	10	10	10	11

Each signal entering the Full Adder is applied to a PFR. Each PFR has two outputs, one coming directly from the plate of the "reset" side of the FF and the other from a tap in a delay network in the plate circuit of the same vacuum tube. These outputs go, in various combinations, to nine amplifiers, V10 through V18. The amplifiers supply inputs to the different gating circuits of the Full Adder.

The operation of the Full Adder is considered in the cases of: a signal on one input only, signals on two of the inputs, or signals on all three inputs. A signal condition on one of the inputs causes a positive-going signal (-34v to -4v) to be generated by its associated PFR. If the signal appears on the Addend input, the undelayed output of the PFR is applied to the control grid of V13 causing it to conduct. The delayed output of the same PFR is applied to the control grids of V10 and V16 and causes them to conduct. (The purpose for using the delayed outputs of the PFR is to permit gates following V13 to produce outputs, if required, before a signal appears in the circuits following V16.)

When V10 conducts, a negative-going signal (+90v to +60v) alerts the Triple Coincidence Gate. However, the other two inputs to this gate supplied by V11 and V12, are held at +90v. Therefore, the output of the Triple Coincidence Gate is maintained at +90v, or the no signal condition.

When V13 conducts, negative-going (+90v to +60v) signals alert two of the Paired Coincidence Gates. However, neither of these gates can produce an output because their other inputs, coming from V14 and V15, are held at +90v and thus the gates remain disabled. Both inputs to the third Paired Coincidence Gate

remain at +90v. Since there is no output (+60v) from any of the Paired Coincidence Gates there is no inhibitory signal (+90v) on the Sum Suppression Gates, and in addition, the no signal condition exists on the Carry Output.

The negative-going (+90v to +60v) signal produced when V16 conducts is applied to the Triple Input "OR" Gate. The polarity of the crystal diodes in this gate is such that a negative going signal on any of its inputs will pass into the circuitry beyond. The Sum Output Suppression Gate will not interfere with the passage of the output from the Triple Input "OR" Gate because it is normally alerted by the lower limit (+60v) plate voltage of normally conducting amplifier V19. The signal will then pass through a crystal diode "OR" gate, the output of which is the Sum Output.

The same reactions within the Full Adder occur if the initial signal appears on the Augend or Carry inputs. Thus the combination of a signal on one input and no signals on the other two inputs yields a signal on the Sum Output and no signal on the Carry Output.

The second case considers the stimulation of two of the three inputs. If signals appear on the Addend and Augend inputs, for instance, positive-going (-34v to -4v) signals are generated by their respective PFR's. The undelayed output of Addend PFR causes V13 to conduct and the undelayed output of the Augend PFR causes V14 to conduct. While the negative-going (+90v to +60v) outputs of V13 and V14 both go to two of the Paired Coincidence Gates they are common to only one of them. This coincidence Gate, though, is properly alerted, causing a drop in its output potential which is communicated to V19 through an AC coupling capacitance as a -20v amplitude pulse. V19 cuts off. The rise in plate voltage (+90v) removes the enabling level from the Sum Output Suppression Gate. The change in the plate potential of V19 is applied to cathode follower

V20 and amplifier V21. The output of V21 is the Carry Output; any change (negative-going) in its normal condition indicates a situation exists in the signal combination on the inputs of the Full Adder which requires a carry pulse.

Signals are transmitted from the delayed outputs of the Addend and Augend PFR's to V16 and V17, causing them to conduct. The lowering of the plate potentials of V16 and/or V17 is also apparent on the output of the Triple Input "OR" Gate. However the effect of this potential change can appear no further since it is deleted by the +90v output of V19 on the Sum Output Suppression Gate.

The delayed outputs of the Addend and Augend PFR's also cause V10 and V11 to conduct. The negative-going outputs from V10 and V11 alert the Triple Coincidence Gate; however, it is held at +90v by the plate potential of non-conducting V12.

A similar situation exists within the adder regardless of which two of the three inputs are stimulated. Thus, a signal on two inputs to the Full Adder yields no signal on the Sum Output and a signal on the Carry Output.

The third case involves the presence of signals on each of the three inputs simultaneously. Each of the input PFR's produces positive-going signals (-34v to -4v) on both the undelayed and delayed outputs. The undelayed outputs cause amplifiers V13, V14 and V15 to conduct. The +60v plate level of these amplifiers alert all of the Paired Coincidence Gates. The output of any one of the Paired Coincidence Gates is sufficient to cut off V19, which in turn produces an inhibit (+90v) on the Sum Output Suppression Gate and supplies the carry signal through V20 and V21.

The delayed outputs of the PFR's cause V16, V17 and V18 to conduct. The +60v plate potential of these amplifiers is apparent on the output of the Triple

Input "OR" Gate. However, this signal cannot pass the Sum Output Suppression Gate because of the +90v inhibitory level generated when V19 is cut off.

The other destinations of the delayed outputs from the input PFR's are amplifiers V10, V11 and V12. A positive-going pulse from the PFR's causes these amplifiers to conduct. The +60v plate potentials of V10, V11 and V12 appearing on the inputs of the Triple Coincidence Gate causes its output to drop to +60v, or the signal condition. This signal passes into the Sum Output as the sum signal. Thus, with signals on all three inputs, indicating the addition of three binary "1's", the Full Adder produces a sum of "1" and a carry of "1".

4. ELECTRICAL DESCRIPTION OF PRINTED-CIRCUIT CHASSIS

a. GENERAL. - The circuits which directly control all of the internal storage of Univac II are provided by an arrangement of 310 printed-circuit chassis. The circuit design is such that only 29 different chassis types are required. These are designated types 1-27, 29 and 30. There is no chassis type 28. The 310 printed-circuit chassis are mounted in Bays E, M, N and GV of the Central Computer. Each bay section provides space for 36 chassis in three rows of 12 chassis positions each. Not all of the chassis positions are filled.

In addition to the circuits contained on the standard printed-circuit chassis, two types of printed-circuit cards are mounted within the packages that physically contain the core-storage planes. These are the diverter circuits. One type, the Buffer Diverter, serves the intermediate storage registers, rI, rO and rZW. There are six of these cards, a pair are found in the following chassis positions: M2-3T, M2-3V and N2-3V. A second type, the Translator Diverter, serves the main memory, rM. There are ten of this type located in the memory box inside the computer.

Table 4-1 indicates the chassis type found in each chassis position in Bays E, M, N and GV. A total of each of the various types found in each bay is provided, with the total number of chassis mounted in the particular bay. The symbol BD represents the location of the Buffer Diverter cards (actually this is the location of a particular intermediate storage register). The positions left blank are not used as chassis locations.

This section describes the electrical operation of each type of printed-circuits chassis and, the two diverter cards. The emphasis is on how the chassis operates rather than the logical function it performs. Signals

(Continued on Page 106)

PRINTED-CIRCUIT CHASSIS POSITIONS, TYPES, TOTALS

BAY E

SECTION T

POS	TYPE	POS	TYPE	POS	TYPE
1	24	13	25	25	19
2	24	14	1	26	16
3	24	15	25	27	19
4	24	16	1	28	16
5	24	17	24	29	19
6	24	18	1	30	6
7	24	19	25	31	19
8	24	20	1	32	19
9	24	21	25	33	19
10	24	22	1	34	2
11	24	23	24	35	19
12	24	24	1	36	24

SECTION V

1	15	13	15	25	
2	16	14	16	26	
3	23	15	18	27	
4	30	16	13	28	
5	30	17	13	29	
6	23	18	16	30	12
7	30	19	16	31	2
8	16	20	15	32	2
9	16	21	12	33	13
10	11	22	6	34	16
11	11	23	6	35	16
12	11	24	6	36	6

SECTION X

1		13		25	
2		14		26	
3		15		27	
4		16		28	
5		17		29	
6		18		30	
7		19		31	
8		20		32	
9		21		33	
10		22		34	
11		23		35	
12	11	24	16	36	16

TYPE	TOTAL
1	6
2	3
3	
4	
5	
6	5
7	
8	
9	
10	
11	4
12	2
13	3
14	
15	3
16	12
17	
18	1
19	7
20	
21	
22	
23	2
24	15
25	4
26	
27	
29	
30	3
BD	

TOTAL	70

TABLE 4-1 (Cont'd)

BAY M

SECTION T

POS	TYPE	POS	TYPE	POS	TYPE
1	5	13	5	25	5
2	BD	14	5	26	5
3	BD	15	5	27	27
4	20	16	8	28	17
5	20	17	8	29	9
6	20	18	8	30	10
7	20	19	8	31	17
8	20	20	8	32	9
9	20	21	8	33	10
10	20	22	8	34	17
11	20	23	8	35	9
12	20	24	8	36	10

SECTION V

1	4	13	5	25	5
2	BD	14	4	26	5
3	BD	15	4	27	21
4	4	16	4	28	21
5	4	17	4	29	11
6	4	18	4	30	11
7	4	19	4	31	15
8	4	20	4	32	15
9	4	21	4	33	6
10	4	22	4	34	6
11	4	23	4	35	6
12	4	24	4	36	6

SECTION X

1	21	13	30	25	6
2	1	14	18	26	6
3	21	15	30	27	6
4	1	16	18	28	2
5	23	17	12	29	6
6	29	18	12	30	15
7	15	19	16	31	15
8	15	20	16	32	6
9	11	21	12	33	16
10	16	22	13	34	13
11	16	23	21	35	16
12	21	24	1	36	2

TYPE	TOTAL
1	3
2	2
3	
4	21
5	9
6	9
7	
8	9
9	3
10	3
11	3
12	3
13	2
14	
15	6
16	6
17	3
18	2
19	
20	9
21	6
22	
23	1
24	
25	
26	
27	1
29	1
30	2
BD	4

TOTAL	108

TABLE 4-1 (Cont'd)

BAY N

SECTION T

POS	TYPE	POS	TYPE	POS	TYPE
1	20	13	8	25	17
2	20	14	8	26	9
3	20	15	8	27	10
4	20	16	8	28	17
5	20	17	8	29	9
6	20	18	8	30	10
7	20	19	8	31	17
8	20	20	8	32	9
9	20	21	8	33	10
10	20	22	8	34	17
11	20	23	8	35	22
12	20	24	8	36	22

SECTION V

1	3	13	5	25	5
2	BD	14	3	26	5
3	BD	15	3	27	21
4	3	16	3	28	21
5	3	17	3	29	21
6	3	18	3	30	21
7	3	19	3	31	14
8	3	20	3	32	14
9	3	21	3	33	26
10	3	22	3	34	26
11	3	23	3	35	26
12	3	24	3	36	26

SECTION X

1	11	13	15	25	12
2	11	14	15	26	12
3	1	15	15	27	12
4	21	16	15	28	23
5	1	17	16	29	23
6	18	18	16	30	
7	18	19	16	31	6
8	30	20	16	32	2
9	30	21	16	33	2
10	6	22	16	34	1
11	6	23	16	35	21
12	6	24	16	36	21

TYPE	TOTAL
1	3
2	2
3	21
4	
5	3
6	4
7	
8	12
9	3
10	3
11	2
12	3
13	
14	2
15	4
16	8
17	4
18	2
19	
20	12
21	7
22	2
23	2
24	
25	
26	4
27	
29	
30	2
BD	2

TOTAL	107

TABLE 4-1 (Cont'd)

BAY G

SECTION T

POS	TYPE	POS	TYPE	POS	TYPE
1		13		25	
2		14		26	
3		15		27	
4		16		28	
5		17		29	
6		18		30	
7		19		31	
8		20		32	
9		21		33	
10		22		34	
11		23		35	
12		24		36	

SECTION V

1	13	13	6	25	15
2	13	14	6	26	16
3	13	15	6	27	16
4		16	6	28	
5	7	17	6	29	7
6	7	18	6	30	7
7	7	19	6	31	7
8	7	20	6	32	7
9	7	21	6	33	7
10	7	22		34	7
11	7	23		35	7
12	7	24		36	7

SECTION X

1		13		25	
2		14		26	
3		15		27	
4		16		28	
5		17		29	
6		18		30	
7		19		31	
8		20		32	
9		21		33	
10		22		34	
11		23		35	
12		24		36	

TYPE	TOTAL
1	
2	
3	
4	
5	
6	9
7	16
8	
9	
10	
11	
12	
13	3
14	
15	1
16	2
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
29	
30	
BD	

TOTAL	31

(Continued from Page 101)
to and from each chassis are considered by potentials and duration rather than by their purpose. Illustrations are provided where it is deemed desirable to show voltage-time relationships. Reference should be made to the schematic diagrams for the various chassis types.

b. CHASSIS TYPE 1, MAGNETRON COUNTER. (Refer to XG188799). - This chassis is comprised of two 6700 beam switching tubes, four diode OR circuits, ten diode AND gate circuits and four 5915 gate circuits. There are two counters per chassis, whose outputs must match to produce an output from the chassis. Twelve of these chassis are utilized in the computer as high-speed decimal counters to select addresses in the main memory (rM) and provide for the consecutive addressing in the input and output storage sections (rI & rO).

In operation, the counter is initially cleared by lowering the spade supply from -20v to -100v; this produces no output from the chassis. The counter can then be preset to one of its ten stable states. For example, an input on pin D (see figure 4-1) lowers the potential of spade D from -14v to -140v. An electron beam is formed which flows from the cathode to target D, presetting the counter to D. Selecting target D causes its potential to drop from +40v to -24v. This potential is applied to gate A; the output of the duplicate counter should also be on a count of D, supplying the other input (-24v) to gate A, thus output 1 of the chassis is a count of D (-24v). All other inputs from the chassis are at +40v. To step the counter to its next stable state, E, a stepping pulse (-15v to +13v) is applied to both the "odd" gate, which is inhibited by the "D" output and is thus of no consequence, and the "even" gate which is alerted by the lack of an inhibit. The output of the "even" gate lowers the potential on grid E (and all even grids) from -90v to -175v. The low grid potential causes the beam to switch from target D to the next higher target, E. Since the duplicate counter will also be stepped to E,
(Continued on Page 108)

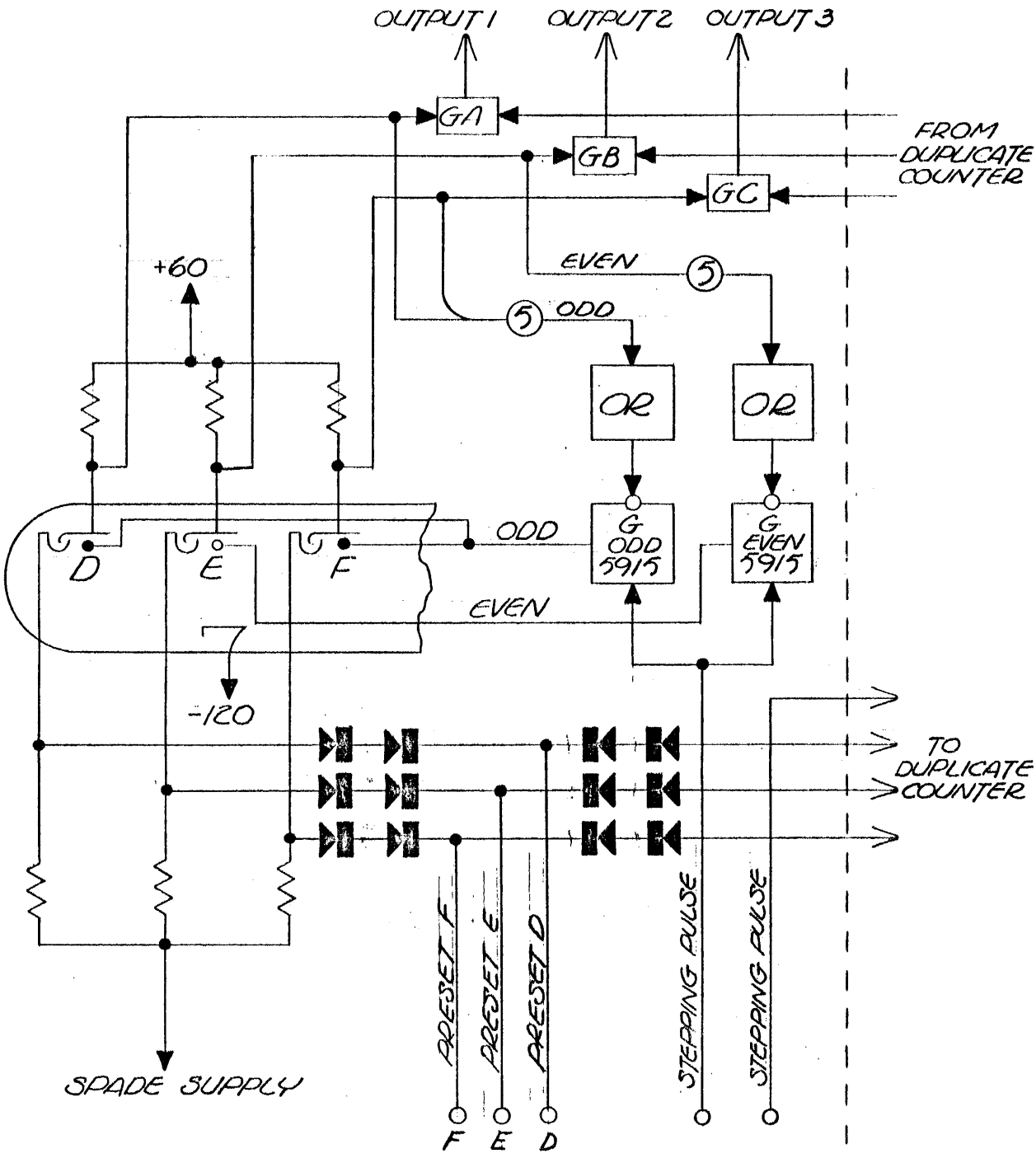


Figure 4-1 Magnetron Counter

(Continued from Page 106)
output 2 will be a count of E. The next stepping pulse will pass through the now alerted "odd" gate and cause the beam to switch to target F. The beam switched to target F instead of to target D because of the effect of magnetic field through the tube.

c. CHASSIS TYPE 2, CLEAR & PRESET. (Refer to XG105826). - The clear and preset chassis is comprised of three amplifiers, one cathode follower, three delay lines, two pulse transformers and one OR circuit. Seven of these chassis are utilized to produce a pair of control pulses for the various magnetron counters; a CLEAR for the counter, and, 4 μsec later, a PRESET for the counter.

In operation, an input is applied to T31 or T33. See figure 4-2. This is a negative-going (+5v to -35v) signal (TT-B). The signal passes through a 1 μsec delay to amplifier V2A. The output of V2A passes through cathode follower (V2B) to amplifier (V1) and a delay line. The output of V1 is applied to a pulse transformer from which it appears on pin 13. This output is a negative-going (-20v to -100v) signal (TT-F), and is the CLEAR (spade supply) for a counter. The other output from V2B goes through two 2-μsec delay lines (4 μsec delay) to amplifier V5. The output of V5 is applied to a pulse transformer and appears on T3. This output is a negative-going (-14v to -140v) signal (TT-H), and is the PRESET signal for a counter.

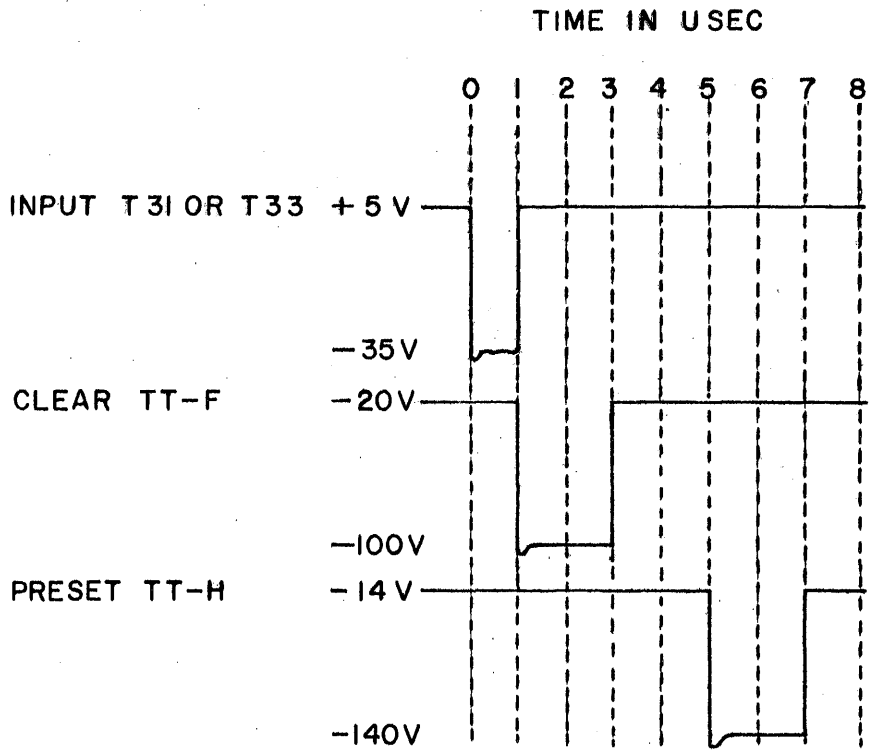


Figure 4-2. Clear & Preset Timing

d. CHASSIS TYPE 3, DIGIT PLANE CONTROL, rI. (Refer to XG105834). - This chassis contains two M2 cores, two sense amplifiers, and two pulse stretchers. The M2 cores function as intermediate storage for the input to and output from rI. The pulse stretchers produce inhibit currents for rI. There are twenty-one of these chassis providing 42-bit storage for the half-word mode of parallel transfer used by the computer.

(1) N5 TO M2. - Data is entered into rI from the N5 Input Distributor via the M2 cores. For example, if the N5 core contains a "0", the input on T31 is a positive-going (-30v to -10v) .2 μsec signal. This signal, due to its short duration, will not set the M2 core. Therefore, the M2 core will

remain in its cleared or "0" state. If the N5 core contains a "1", the input on T31 is a positive-going (-30v to 0v) 1 μsec signal. This signal is sufficient to set the M2 core to the "1" state.

(2) M2 TO rI. - All inputs to rI come from the M2 cores via the pulse stretchers. For example, a READ M2 signal and a TRANSFER M2 TO PS signal are applied to T17 and T9, respectively. Both of these are positive-going (-30v to +10v) signals. If the M2 core contains a "1", the READ M2 signal causes M2 to switch, producing a positive-going (-14v to 0v) 1 μsec signal which is seen on TT-L. The core read-out enables a gate whose other input is the TRANSFER M2 TO PS signal. The output from the gate enters the PS to produce an inhibit current which prevents the writing of a "1" (machine "1"'s, memory "0"'s) into the particular core in rI. If the M2 core contains a "0", the read-out will show a positive-going (-14v to 0v) .2 μsec signal on TT-L. This signal is not sufficient to alert the aforementioned gate, therefore the TRANSFER M2 TO PS signal is not impressed upon the input of the PS. The PS will not produce an inhibit current and a "1" (machine "0"'s, memory "1"'s) will be written into the particular core in rI. The inhibit current is terminated by the negative going (0v to -14v) DISCHARGER signal which appears on T7. This signal discharges capacitor C14; C14 is charged if there is an input to the PS.

(3) rI TO M2. - The M2 core is initially set by the UNCONDITIONAL SET signal applied to T30. This is a positive-going (-30v to +5v) signal. If the core in rI contains a "0", there will be no input to the sense amplifier, and the sense amplifier will hold disabled a gate whose other input is STROBE rI, a positive-going (-14v to +26v) signal. The M2 core thus retains a "1" (memory "0"'s, machine "1"'s). If the core in rI contains a "1", there will

be an input to the sense amplifier, and the sense amplifier alerts the aforementioned gate which will pass the STROBE rI to clear the M2 core. The M2 core now contains a "0" (memory "1"'s, machine "0"'s).

(4) M2 TO M1. - A transfer from rI to rM is accomplished via the M2 and the M1 cores. As an example to read out an M2 core, a READ M2 signal is applied to T17. If the M2 core contains a "1", positive-going (-14v to 0v) 1 μsec signal will appear at TT-L, this is the output (via T19) that will be transferred to M1. At this time, the bit that was read out of rI is restored in rI. The restoration is accomplished by the TRANSFER M2 TO PS signal which controls the inhibit current, as previously mentioned.

e. CHASSIS TYPE 4, DIGIT PLANE CONTROL, r0. (Refer to XG105836). - This chassis contains two M3 cores, two M4 cores, two sense amplifiers, and two pulse stretchers. The M3 cores function as intermediate storage for the input to and the output from r0. The M4 cores function as intermediate storage between the M3 cores and Uniservos and Supervisory Control. The sense amplifiers sense the output from r0. The pulse stretchers produce inhibit currents for r0. There are 21 of these chassis utilized to effect the half-word transfer.

(1) M1 TO M3. - A transfer to r0 from rM is via the M1 and M3 cores. For example, if the M1 core contains a "0", the input to M3 from M1 on T33 is a positive-going (-30v to 0v) .2 μsec signal. Due to its short duration, this pulse does not set the M3 core, and the M3 core will retain the preset "0". If the M1 core contains a "1", the input on T33 is a positive-going (-30v to 0v) 1 μsec signal. This signal is of sufficient duration to set the M3 core.

(2) M3 to r0. - All inputs to r0 are from the M3 cores via the pulse stretchers. For example, a READ M3 signal and a TRANSFER M3 TO PS signal are applied to T17 and T9 respectively. Both of these are positive-going

(-30v to +10v) signals. If the M3 core contains a "1", TT-E will show a positive-going (-14v to 0v) 1 μsec signal. The signal from M3 alerts a gate whose other input is the TRANSFER M3 TO PS signal. The output from the gate enters the PS to produce an inhibit current. The output of PS inhibits the writing of a "1" (machine "1"'s, memory "0"'s) into a particular core in r0. If the M3 core contains a "0", TT-E will show a positive-going (-14v to 0v) .2 μsec signal. This does not enable the aforementioned gate, therefore the TRANSFER M3 TO PS signal is not impressed upon the input of the PS. The PS will not produce an inhibit current and a "1" (machine "0"'s, memory "1"'s) will be written into that particular core in r0. The inhibit current is terminated by the negative-going (0v to -14v) DISCHARGER signal which appears on T7. This discharges capacitor C13; C13 is charged if there is an input to the PS.

(3) r0 TO M3. - The M3 core is initially set by the UNCONDITIONAL SET signal applied to T30 which is a positive-going (-30v to +5v) signal. If the core in r0 contains a "0", there is no input to the sense amplifier. Therefore the sense amplifier holds inhibited a gate whose other input is STROBE r0, a positive-going (-14v to +26v) signal. The M3 core remains set and contains a "1" (memory "0"'s, machine "1"'s). If the core in r0 contains a "1", there will be an input to the sense amplifier. Therefore the sense amplifier alerts the aforementioned gate to enable the STROBE r0 to clear the M3 core and the M3 core now contains a "0" (memory "1"'s, machine "0"'s).

(4) M3 TO M4. - A transfer from r0 to the Uniservos is made via the M3 and M4 cores. As an example to read out a M3 core, a READ M3 signal is applied to T17. If the M3 core contains a "1", a positive-going (-14v to 0v) 1 μsec signal will appear at TT-E. This signal probes a gate which is alerted

by the TRANSFER M3 TO M4 signal. Therefore the "1" that was in the M3 core now appears in the corresponding M4 core. If the M3 core contains a "0", a positive-going (-14v to 0v) .2 μsec signal will appear at TT-E. This signal will not alert the aforementioned gate, and the corresponding M4 core will retain a "0". Also at this time, the bit that was read out of r0 is restored in r0. This is accomplished by the TRANSFER M3 TO PS signal which controls the inhibit current, as was mentioned previously.

A TR0 signal, applied to T14 reads out the M4 core. This is a positive-going (-30v to +10v) 2 μsec signal. If the M4 core contains a "1", a positive-going (-14v to 0v) 2 μsec signal will appear on TT-N. If the M4 core contains a "0", a positive-going (-14v to 0v) .2 μsec signal will appear on TT-N. This output appears on T12. The output from M4 controls the condition of the "Write" flip-flops.

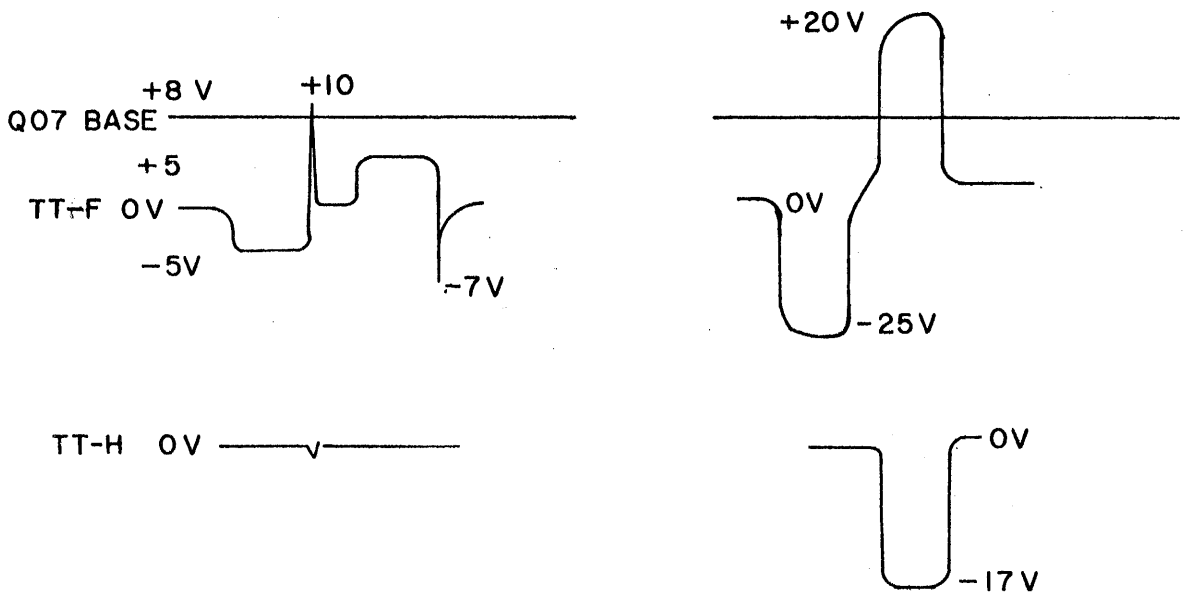
f. CHASSIS TYPE 5, LINE DRIVER. (Refer to XG188862). - This chassis contains three gates, two pulse formers, two pulse transformers, three amplifiers, and one delay line. Twelve of these chassis generate the read and write drive currents for rI, rM, rZW, and r0. Each storage section utilizes three of these chassis to provide the drive current for the X(R), the X(L), and the Y drive lines.

(1) Read/Write Y. - Initially the cores in a memory register are cleared before information is stored in them. This is accomplished through the Line Drivers by a 6 μsec negative-going (+5v to -20v) READ signal, applied to T29 for example. This signal, inverted by V01, is applied to V02. V02 conducts and induces current into the secondary windings of transformer T02. A representation of this current may be seen between TT-D and TT-G. Using TT-D for a reference, TT-G shows a positive-going signal of 350 millivolts amplitude.

To store (write) information in a core it is necessary to produce drive current of the opposite polarity (to the read current) on the Y drive line. This is accomplished by a negative-going (+5v to -20v) 6 μsec WRITE signal applied to T25. This signal, inverted by V04, is applied to V03. V03 conducts and induces current into the secondary windings of T02. A representation of this current may be seen between TT-D and TT-G. Using TT-D for a reference, TT-G shows a negative-going signal of 350 millivolts amplitude. This current is terminated 1.2 μsec after the positive-going (-30v to +5v) TRANSFER signal has been applied to T16. The TRANSFER signal, after a 1.2 μsec delay, turns on Q06, and subsequently turns off Q05. The TRANSFER signal also turned on Q01, Q02, Q03, and Q04, producing the negative-going (0v to -14v) DISCHARGER signal which may be seen at TT-K.

(2) Read/Write X(R) or X(L). - Operation is similar to that presented in the previous paragraph, the exception being that the inputs (READ and WRITE) are gated by signals on T30 and T26 respectively. If the input to T30 is an inhibit, so should the input on T26. This ensures that if there is no drive current for read X(R), then there also is no drive current for write X(R). The same situation prevails for X(L).

(3) NO ADDRESS ERROR CIRCUIT. - This circuit is comprised of Q07 and T01. The purpose for this circuit is to detect the no address condition, i.e., if the drive lines are not terminated. During a normal Read/Write cycle, the emitter of Q07 is never more positive than its base (+8v). See figure 4-3 (a). When there is no address, T02 is terminated in an open line, this causes excessive ringing in T02. This ringing produces a wave of sufficient amplitude to cause the emitter of Q07 to go more positive than its base, causing a signal to be developed on the primary of T01. The output ERROR signal may be seen at TT-H. See figure 4-3 (b).



a. address selected

b. no address selected

Figure 4-3. No Address Error Circuit

g. CHASSIS TYPE 6, 6146 DRIVER. (Refer to XG105668). - This chassis contains four amplifiers, six pulse transformers, two cores, and two OR circuits. There are twenty-seven of these chassis utilized in the computer to produce output signals, of either 1 μsec or 2 μsec duration, that may be applied to drive many circuits simultaneously.

As an example, a positive-going (-30v to +5v) signal may be applied to either T11 or T15. This input is coupled through pulse transformer T04 to amplifier V03 and core C502. V03 begins to conduct and C502 begins to switch.. The output from V03 is taken from pulse transformer T02. There are two outputs

from T02, one is a negative-going (0v to -45v) signal which appears on T12, the other is a positive-going (-40v to +5v) signal that is applied to amplifier V04 and C502. V04 conducts and causes C502 to complete its switch, this, in turn, increases the effect of the input to V03. V03 reaches saturation and the outputs from T02 begin to decay. C502 switches back to its initial state, causing V03 to cutoff, which in turn cuts off V04. While V04 conducts a negative-going (0v to -40v) output is taken from T05 and appears on T3 (TT-G).

The outputs on T3 and T12 may be either 1 μsec or 2 μsec in duration. To produce a 1 μsec output, the screen voltage on V03 is +90v and the bias on C502 is -20v. To produce a 2 μsec output, the screen voltage on V03 is +60v and the bias on C502 is -11v. The other half of chassis is identical in operation.

h. CHASSIS TYPE 7, PULSE FORMER, POSITIVE. (Refer to XG188851). - This chassis contains two amplifiers, one diode clock gate circuit, one flip-flop and one pulse transformer. There are sixteen of these chassis utilized to resynchronize and reshape "t" pulses.

Initially, amplifiers V01 and V04 do not conduct. V01 is held cutoff by the flip-flop whose initial state is V02 conducting and V03 cutoff. V04 is held cutoff by its bias voltage (-15v). The flip-flop is held in its initial state by the TP+ (-88v to -71v) pulses that it receives. See figure 4-4 for timing. When V04 is cutoff, its plate voltage(-71v) inhibits the clock gate to the TP- (-74v to -91v) pulses, and the state of the flip-flop remains unchanged. A t pulse is applied to T1. If it is at least 15v in amplitude, V04 conducts and its plate voltage (-88v) alerts the clock gate. The next TP- that appears on T12 passes through the clock gate to the flip-flop and cuts off V02, which causes V03 to conduct. The rise in plate

voltage of V02 also causes amplifier V01 to conduct producing an output from the pulse transformer. The output from the pulse transformer will continue until the next TP+ pulse is applied to T20. This TP+ pulse will pass through the clock gate and switch the flip-flop back to its initial state, cutting off V01 and terminating its output.

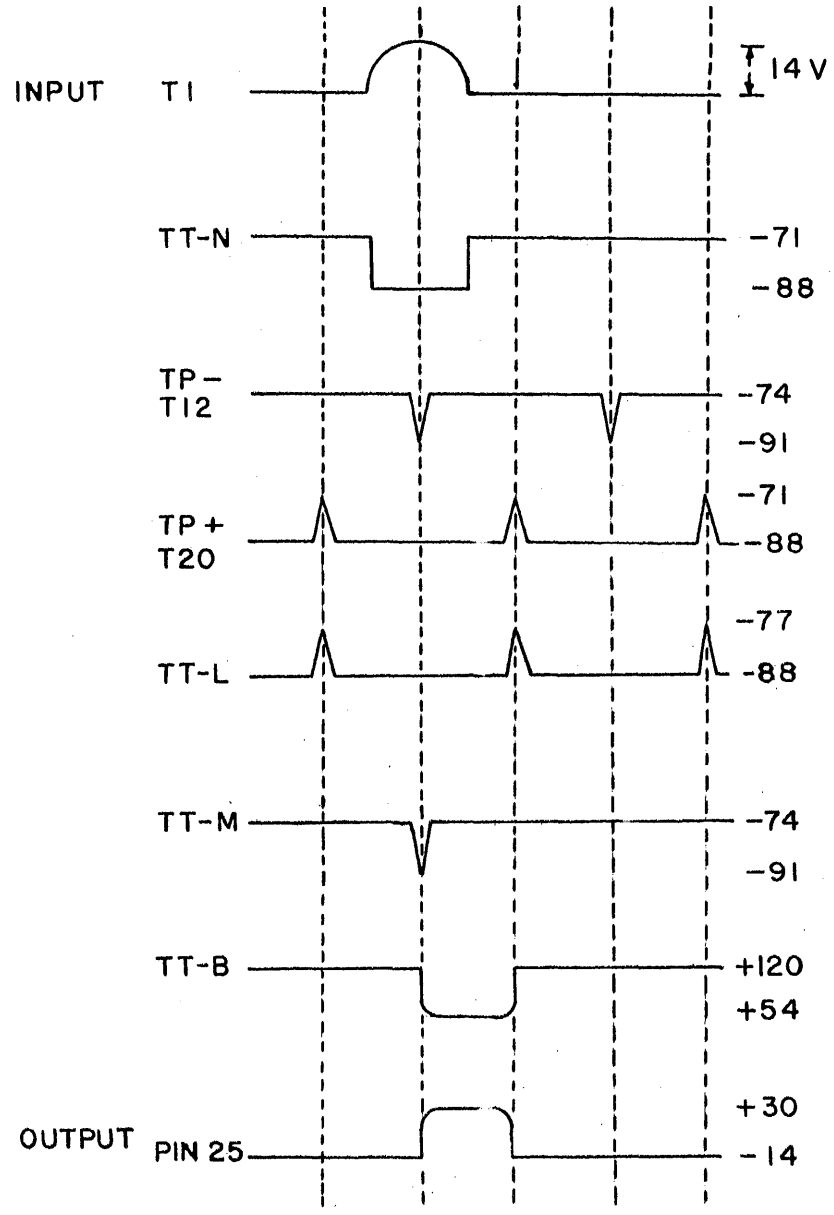


Figure 4-4. Pulse Former, Positive Timing

i. CHASSIS TYPE 8, STATICIZER - SERIALIZER GATES. (Refer to XG188906). - This chassis contains two 7AK7 gates, two type C cores, four amplifiers and two type M cores. Twenty-one of these chassis provide the necessary gating between the Staticizer - Serializer line and the M1 register. The M1 cores provide intermediate storage for the input to and the output from rM and rZW.

(1) STATICIZE. - Refer to Figure 4-5. A half-word enters the Staticizer-Serializer in serial form. When the entire half-word is in the Staticizer-Serializer, each bit is passed through a gate in the STATICIZER - SERIALIZER GATES chassis simultaneously. In operation, a "1" input may appear on T1 as a negative-going (+90v to +60v) signal inhibiting the 7AK7 gate V02. Consequently, the positive-going (+60v to +90v) STATICIZER PULSE appearing on T9 will not pass through the 7AK7 gate and the M core will retain its preset "1". The M1 core was initially set by the positive-going (-30v to +5v) SET UNCONDITIONALLY M CORES signal. If the bit applied to T1 is a "0" (+90v) the 7AK7 gate is enabled. The STATICIZER PULSE passes through the gate and pulse transformer T02 and clears the M1 core to "0". T02 is also connected to core CS01 and amplifier V01A. A circuit comprised of CS01, V01A and T02 forms a blocking oscillator which is used for pulse shaping purposes to ensure that the M core will be switched properly.

(2) M2 TO M1. - Information that is to be transferred from rI to rM and rZW is transmitted via the M2 and the M1 cores. A "1" from a M2 core appears on T10 as a positive-going (-10v to 0v) 1 μsec signal. This signal alerts a gate whose other input is the positive-going (-30v to +5v) TRANSFER M2 TO M1 signal. The output of the gate sets the M1 core. A "0" from a M2 core appears on T10 as a positive-going (-10v to 0v) .2 μsec signal. This signal does not have the duration to enable the aforementioned gate and the

TRANSFER M2 TO M1 signal is not allowed to set the M1 core and the M1 core retains a "0".

(3) M1 TO rM and rZW. - A positive-going (-30v to 0v) READ M1 CORES signal is applied to T25. If the M1 core contains a "1", TT-F will show a positive-going (-14v to 0v) 1 μsec signal. If the M1 core contains a "0", TT-F will show a positive-going (-14v to 0v) .2 μsec signal. In either instance, this is the M1 OUT TO PS signal and it appears on T31.

(4) rM or rZW TO M1. - Initially, a positive going (-30v to +5v) SET UNCONDITIONALLY M1 CORES signal, applied to T16, sets the M1 core. If the memory core in rM or rZW contains a "1", the input on T12 is a positive-going (0v to +30v) signal, and the M1 core is cleared to "0" (memory "1"'s, machine "0"'s). If the core in rM or rZW contains a "0", the input on T12 is no signal (0v) and the M1 core retains a "1" (memory "0"'s). Restoring a bit into rM or rZW is accomplished as was explained in the preceding paragraph.

(5) M1 TO M3. - A positive-going (-30v to 0v) READ M1 CORES signal is applied to T25. If the M1 core contains a "1", its output will be a positive-going (-14v to 0v) 1 μsec signal. This signal will enable a gate whose other input is a positive-going (-30v to +5v) TRANSFER M1 to M3 signal. The output from the gate is a positive-going (-14v to 0v) 2 μsec signal which is the M1 OUT TO M3 signal and it appears on T26.

(6) SERIALIZE. - A positive-going (-40v to +20v) TRANSFER M1 TO M3 signal, applied to T15, passes through a gate which is alerted by reading a "1" out of an M1 core. The output of the gate is coupled through transformer T01 to another gate whose other input is a positive-going (-14v to 15v) SERIALIZER PULSE. The output from the gate, amplified by V04, is coupled through T05 to T7. The output at T7 is the SERIALIZER OUT to the Staticizer - Serializer line.

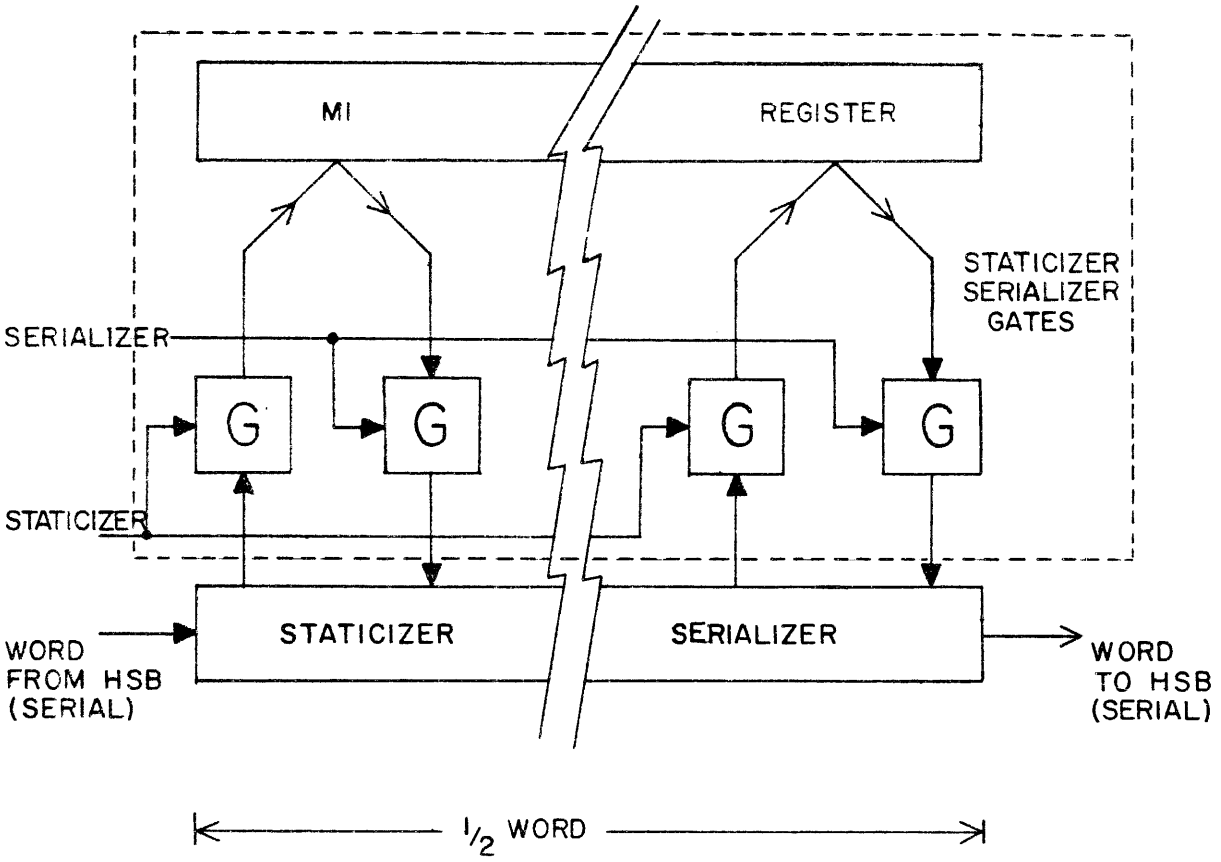


Figure 4-5. Staticizer - Serializer Gates (LSB & MSB Shown)

j. CHASSIS TYPE 9, AMPLIFIER DELAY LINE. (Refer to XG105830). - This chassis contains two amplifiers and a delay line. The two amplifiers are connected in parallel to provide power to drive the delay line. The delay line consists of a series of LC circuits with taps provided along its length for inputs and outputs. Six of these chassis comprise part of the Staticizer - Serializer line. Entrance is made on T33.

Initially, amplifiers V01 and V04 are held cutoff by the -20v which is felt through R04. A "1" appears on T33 as a positive-going (-20v to +8v) signal,

causing both V01 and V04 to go into conduction. The negative-going (+90v to +60v) output from these amplifiers passes through a RL circuit, R03 and L01, into the delay line. This signal will appear at the end of the delay line approximately 1.06 μsec (2.4 pulse times) later as a negative-going (+90v to +60v) decaying signal. The taps connected to outputs T6 and T11 are arbitrarily positioned at different points along the delay line depending upon timing considerations. The negative-going (+90v to +60v) outputs of T6 and T11 are sent to the Staticizer - Serializer Gates as part of the conversion of the serial to static representation. The negative-going (+90v to +60v) input signals applied to T4, T7 and T13 come from the Staticizer - Serializer Gates as bits to be serialized. The taps provided for inputs on T4, T7 and T11 are also positioned at different points along the delay line depending upon how the particular chassis is utilized.

k. CHASSIS TYPE 10, DELAY LINE. (Refer to XG195993). - This chassis contains a delay line composed of four delay sticks. There are six of these chassis utilized as a part of the Staticizer - Serializer. The negative-going (+90v to +60v) input on T33 is the output from T1 of the Amplifier Delay Line (Chassis Type 9). This chassis is a continuation of the Amplifier Delay Line.

l. CHASSIS TYPE 11, FLIP-FLOP. (Refer to XG105886). - This chassis contains two flip-flops and four cathode followers. There are nine of these chassis utilized to provide alerts and inhibits for various gate circuits. A SET or a RESET input may be a 1 μsec or a 2 μsec negative-going (+5v to -30v) signal. The flip-flop has a switching time of 1 μsec, i.e., it may be reset 1 μsec after it has been set, allowing the output voltage swing to reach its maximum magnitude. The output from a flip-flop passes through a cathode follower to prevent excessive loading on the flip-flop. The RESET output,

applied to T13, may be viewed at TT-H. This output will show a rise time of approximately 1.4 μsec and a fall time of 1 μsec. The SET output, applied to T11, may be viewed at TT-G. This will show a rise time of 1 μsec and a fall time of .8 μsec. The two output levels in both cases are +5v and -20v.

m. CHASSIS TYPE 12, SEQUENCER. (Refer to XG195939). - This chassis contains eight amplifiers, six delay lines and eight pulse transformers. There are eight of these chassis utilized to provide pulses of proper timing to operate the various register circuits.

An input, applied to T1, T3, T5 or T31, is a positive-going (-14v to +10v) signal. If an input signal is applied to T5 in Figure 4-6, a negative-going signal of 25v amplitude appears on T6; an output of 25v amplitude also appears between T4 and T7. An input signal applied to T1 or T3 produces a negative-going signal of 25v amplitude on T11; a positive-going (-14v to 10v) signal, delayed 2 μsec, also appears at T30. In many instances where additional delay is required, the output from T30 is connected as an input to T31, thence down the sequencer line. The same voltages and amplitudes prevail down the sequencer line.

n. CHASSIS TYPE 13, FLIP-FLOP. (Refer to XG188969). - This chassis contains two flip-flops and four cathode followers. There are eight of these chassis utilized to provide alerts and inhibits for various gate circuits. This circuit is similar to the Type 11 FLIP-FLOP except that because of the size of the cathode resistor (4.2K) this flip-flop is capable of driving a larger load.

o. CHASSIS TYPE 14, INPUT ODD-EVEN CHECKER SERIALIZER. (Refer to XG188925).- This chassis contains four gates, six amplifiers, four delay lines, four OR circuits and one cathode follower. Two of these chassis serialize the contents (seven bits) of the N5 register so that they may be applied to the Input Odd-Even Checker. (Continued on Page 124)

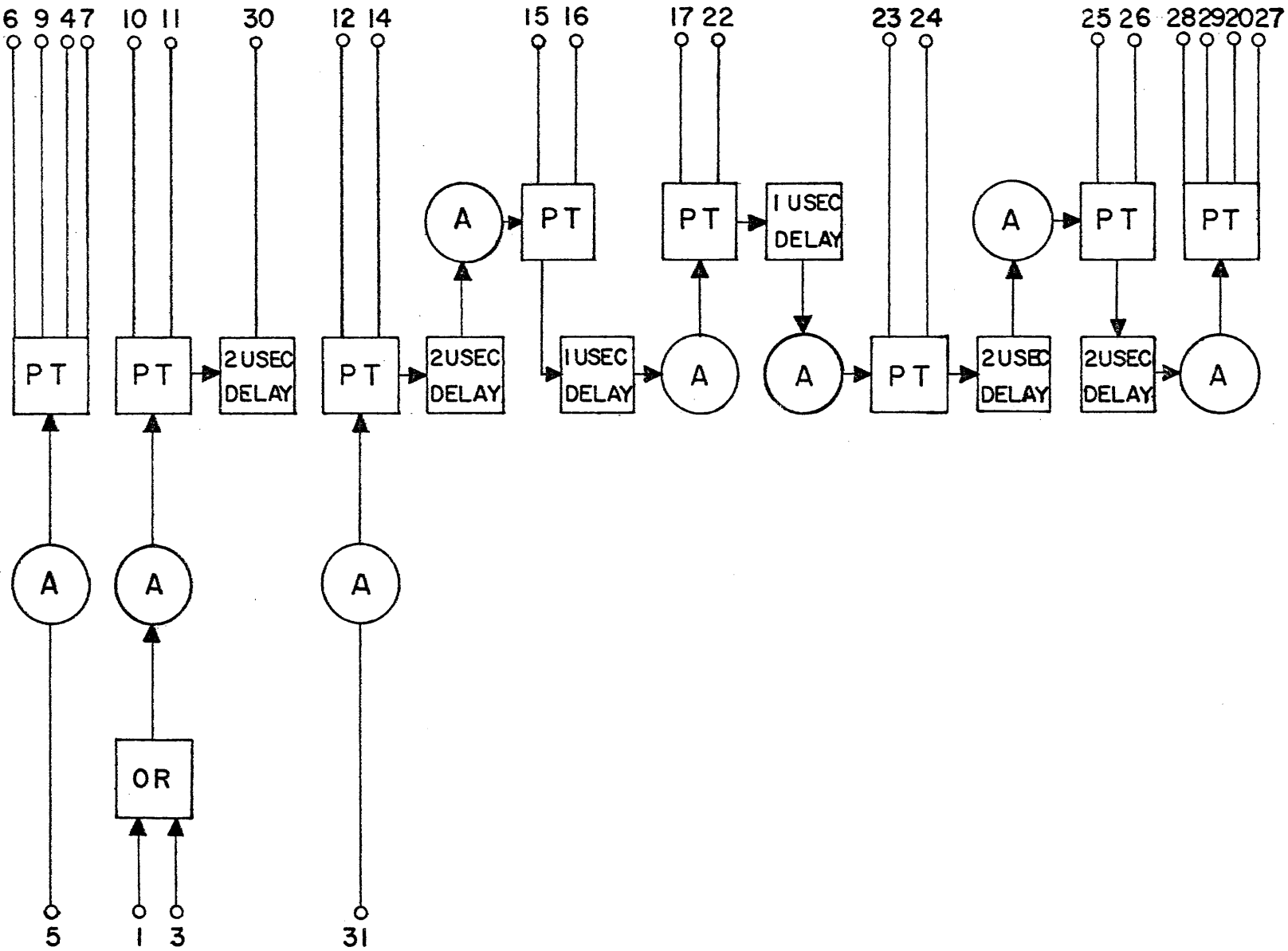


Figure 4-6. Sequencer

(Continued from Page 122)
The contents of the N5 register enter on T11, T21, T26 and T28. If the bit is a "0", the input is a positive-going (-14v to 0v) .2 μsec signal. This signal is not long enough to alert a gate whose other input is the TRANSFER N5 TO OEC signal. If the bit is a "1", the input is a positive-going (-14v to 0v) 1 μsec signal. This signal is sufficient to alert the gate so that the TRANSFER N5 TO OEC signal may pass and be applied to amplifier V03B. The output of V03 goes through an OR circuit and a 3 μsec delay line to amplifier V02B. The output from V02B appears on T7 as a positive-going (-20v to +5v) signal.

In normal operation, all inputs appear simultaneously at T11, T21, T26 and T28 and their resepctive gates. The other input to each of these gates is the TRANSFER N5 TO OEC signal. Wherever there is a "1" input, the gate is alerted and the TRANSFER N5 TO OEC is allowed to pass through the alerted gates to the amplifiers. The outputs of the amplifiers are fed to a common line but are separated in time by 3 μsec delays. In this manner the character is effectively serialized. The two chassis are interconnected to serialize all seven bits. This is accomplished by connecting the output (T7) from the first chassis to an input (T29) of the second chassis. Therefore, all seven bits appear serially on T7 of the second chassis. The output at T7 of the second chassis comes from a cathode follower, V04, an impedance matching device.

p. CHASSIS TYPE 15, OUTPUT DISTRIBUTOR GATES. (Refer to XG195986). - This chassis contains four 7AK7 gates, four diode OR circuits and four pulse transformers. There are fourteen of these chassis used wherever OR and gating action, together, are needed.

The signal applied to the suppressor grid of the 7AK7 is +5v or -14v, respectively an alert or inhibit. The second alert or inhibit is applied to

the control grid of the vacuum tube through a four input diode OR circuit. The inputs to the OR circuit are positive-going (-14v to +10v or -30v to +10v) signals. The output from the chassis comes from a pulse transformer in the plate circuit of the 7AK7. The pulse transformer is terminated with a resistive-inductive circuit for pulse-shaping purposes.

q. CHASSIS TYPE 16, UNIVERSAL GATING. (Refer to XG195990). - This chassis contains four 7AK7 gates, four diode AND circuits, and four pulse transformers. There are twenty-eight of these chassis utilized wherever the combination of the crystal diode and vacuum tube gating action are needed.

A signal is applied to the suppressor grid of the 7AK7 through a three input AND circuit. To alert the gate, all three inputs must be at approximately 0v. To inhibit the gate, any one of the three inputs is held at about -14v. The STROBE, or alerting signal, is applied to the control grid and is a positive-going (-14v to +10v) signal. The output from the chassis comes from a pulse transformer in the plate circuit of the 7AK7. The pulse transformer is terminated with a resistive-inductive circuit for pulse shaping purposes.

r. CHASSIS TYPE 17, PULSE FORMER, NEGATIVE. (Refer to XG188845). - This chassis contains an amplifier, a crystal diode clock gate, a flip-flop and a cathode follower. There are seven of these chassis utilized to resynchronize and reshape bits in a word as it passes through the Staticizer - Serializer.

Initially amplifier V04 is held in conduction by the bias voltage (0v) applied to its control grid. See figure 4-7 for Timing. Cathode follower V01 is held cutoff by the flip-flop whose reset state is V02 conducting and V03 cutoff. The flip-flop is maintained reset by the TP- (-74v to -91v) pulses that are applied to it, because when V04 conducts its plate voltage (-88v) inhibits the clock gate from passing the TP+ pulses. If an input of at least 15v appears on T1, V04 cuts off and its plate voltage (-71v) alerts the

clock gate. The next TP+ (-88v to -71v) that appears on T20 is able to pass through the clock gate to the flip-flop and cause V03 to conduct, which in turn causes V02 to cutoff by normal flip-flop action. The rise in plate voltage of V02 passes through cathode follower V01 and appears on T25 as a positive-going (-20v to +8v) signal. This signal will remain at +8v until the next TP- pulse appears on T12. This TP- will pass through the clock gate and reset the flip-flop. The decrease in plate voltage of V02 will pass through V01 and the signal on T25 will revert to -20v.

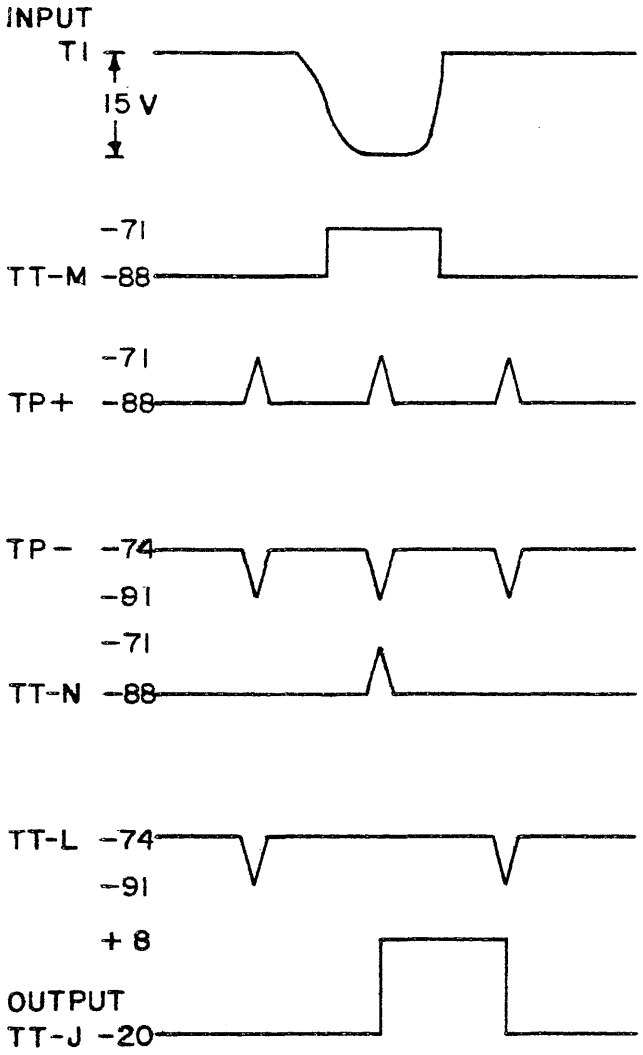
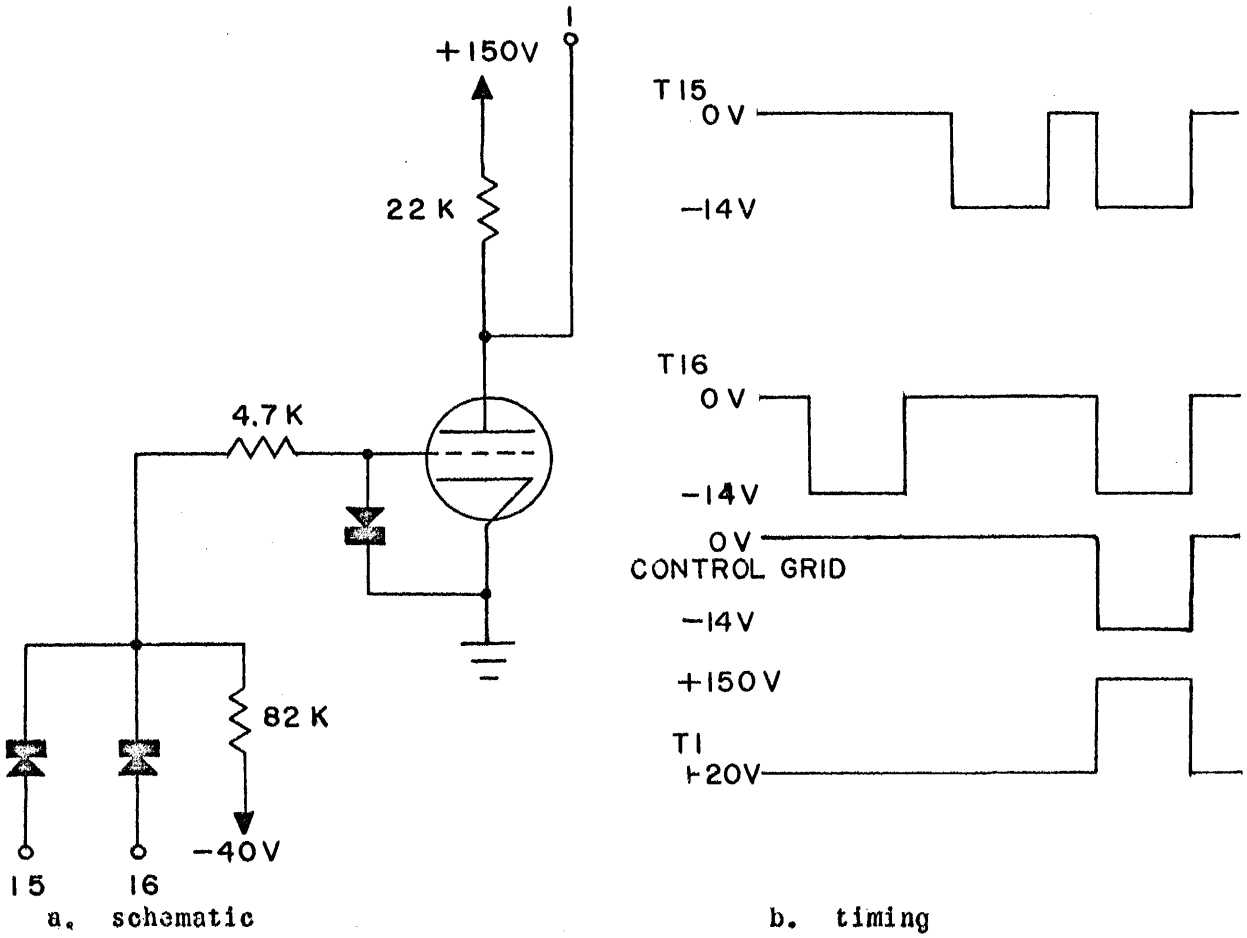


Figure 4-7. Pulse Former, Negative, Timing

s. CHASSIS TYPE 18, OR INVERTER. (Refer to XG189012). - This chassis contains eight diode OR circuits and eight inverter-amplifiers. There are five of these chassis used wherever the combination of a positive OR and an inverter is needed.

See Figure 4-8(a). The output from the OR is equal to its most positive input. For example, if T15 is at -14v and T16 is at -14v, then the output from the OR is at -14v. If T15 is at 0v and T16 is at -14v (or vice-versa), the output from the OR is 0v. When the output from the OR gate is 0v, the inverter will conduct. See figure 4-8(b). When the inverter is cutoff, the signal level at T1 is +150v. When the inverter is conducting, the signal level at T1 is +20v.



a. schematic b. timing

Figure 4-8. OR Inverter

t. CHASSIS TYPE 19, DECODER ENABLE. (Refer to XG105900). - This chassis contains eight diode gate circuits and eight amplifiers. There are seven of these chassis utilized for gating the pulses that preset the Magnetron Counters to the proper count.

All eight gates have two common inputs, one is the PRESET pulse on T29, the other enters either as a +5v alert or a -20v inhibit on T28. The other two inputs (+5v) are present at an appropriate time. See Figure 4-9. If the +5v enable is applied to T28 and if T15 and T16 are already at +5v, then the PRESET pulse (-30v to +5v) will pass through the gate to the amplifier causing it to conduct. The output from the amplifier is coupled through a capacitor to T1. The output that appears on T1 is a negative-going (-11v to -109v) signal which is applied to the Magnetron Counter as the PRESET signal.

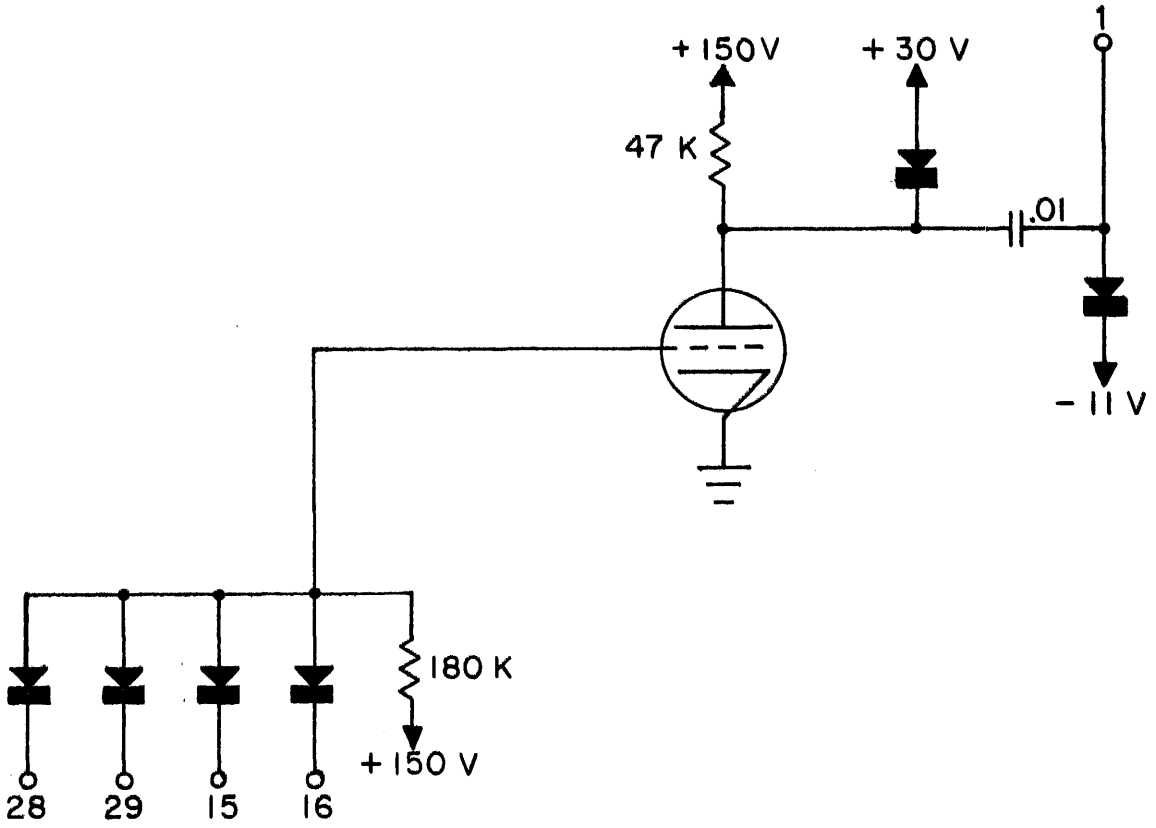


Figure 4-9. Decode Enable

u. CHASSIS TYPE 20, DIGIT PLANE CONTROL, rM and rZW. (Refer to XG189044). - This chassis contains six gates, four sense amplifiers, two pulse stretchers, two OR circuits and six pulse transformers. The sense amplifiers detect the output from rM and rZW. The pulse stretchers (PS) produce inhibit currents for rM and rZW. Four of the gates are used to sample the condition of rM and rZW, the other two transfer the contents of the M1 cores into the pulse stretchers. There are twenty-one of these chassis which contain the 42 circuits necessary for the half-word transfer.

(1) M1 TO rM and rZW. - All inputs to rM and rZW come from the pulse stretchers. For example, a TRANSFER M1 TO PS signal, applied to T9, coincides with the reading of the M1 cores. If the M1 core, whose output is applied to T10, contains a "0", the input on T10 is a positive-going (-40v to 0v) .2 μsec signal. This does not alert a gate whose other input is the TRANSFER M1 TO PS signal, and the TRANSFER M1 TO PS signal is not impressed upon the input to the PS. The PS does not produce an inhibit current and a "1" (machine "0"'s, memory "1"'s) is written into the particular core in rM and rZW. If the M1 core contains a "1", the input on T10 is a positive-going (-14v to 0v) 1 μsec signal. This signal is sufficient to alert the aforementioned gate and the TRANSFER M1 TO PS signal is impressed upon the input of the PS. The PS produces an inhibit current which prevents the writing of a "1" (machine "1"'s, memory "0"'s) into the particular core in rM and rZW. The inhibit current is terminated by the negative-going (0v to -14v) DISCHARGER signal which appears on T7. This discharges capacitor C14; C14 is charged if there is an input to PS.

(2) rM and rZW TO M1. - All information read out of rM and rZW is detected by the sense amplifiers then temporarily stored in M1. If the core

in rM or rZW contains a "0", there is no input to the sense amplifier. In this case, the sense amplifier inhibits a gate whose other input is the STROBE rM (or the STROBE rZW) signal. There will be no output from the sense amplifier to the M1 core and the M1 core retains a "1" (memory "0"'s, machine "1"'s). If the core in rM or rZW contains a "1", there is an input to the sense amplifier. The sense amplifier alerts the aforementioned gate which enables the STROBE rM (or the STROBE rZW) signal to clear the M1 core to "0" (memory "1"'s, machine "0"'s.

v. CHASSIS TYPE 21, MAGNETRON OUTPUT. (Refer to XG189041). - Chassis Type 21 contains eight transistor amplifiers, eight diode AND gates, four diode OR circuits and four vacuum tube amplifiers. Thirteen of these chassis distribute the outputs from the Magnetron Counters to the Diverters.

An input on T7, e.g., comes from a Magnetron Counter. If the Magnetron Counter is at a count that is not connected to T7, T7 is at a +40v level and amplifier V03B conducts. The output from V03B passes through cathode follower V03A. The output from V03A is -20v at this time. If the Magnetron Counter is at a count that is connected to T7 V03B is cutoff. See figure 4-10. The change in V03B is apparent at V03A, which produces a positive-going (-20v to +12v) signal. The output from V03A is applied to two diode AND circuits, to an indicator amplifier and directly from the chassis via T20. If the AND, consisting of diodes CR06 and CR14, is alerted by the +5v that appears on T18, then T19 will have -20v applied to it inhibiting the AND consisting of diodes CR05 and CR09. When the AND consisting of diodes CR06 and CR14 is alerted by +5v appearing on T18, the positive-going output from V03A will pass through this AND to the diverter amplifier consisting of transistors Q02 and Q06. When the AND consisting of diodes CR05 and CR09 is alerted by +5v appearing on

T19, the positive-going output from V03A passes through this AND to the diverter amplifier consisting of transistors Q01 and Q03. The output from either diverter amplifier is a negative-going (-4v to -15v) signal.

The condition of the inputs on T18 and T19 are determined by signals from the Input-Output Control which are generated by the direction of the Uniservo tape. For example, if the input on T7 is a count of nine, and the Uniservo tape is moving in a forward direction, T18 will be at +5v and T19 will be at -20v, therefore, diverter amplifiers Q02 and Q09 will produce the output that goes to a diverter as a count of nine. If the input on T7 is a count of nine, and the Uniservo tape is moving in a backward direction, T18 will be at -20v and T19 will be at +5v, therefore diverter amplifiers Q01 and Q03 will produce the output that goes to a diverter as a count of one.

The indicator amplifier consisting of Q401 and Q403 turns an indicator on and off at the Supervisory Control Panel indicating the count of a Magnetron Counter.

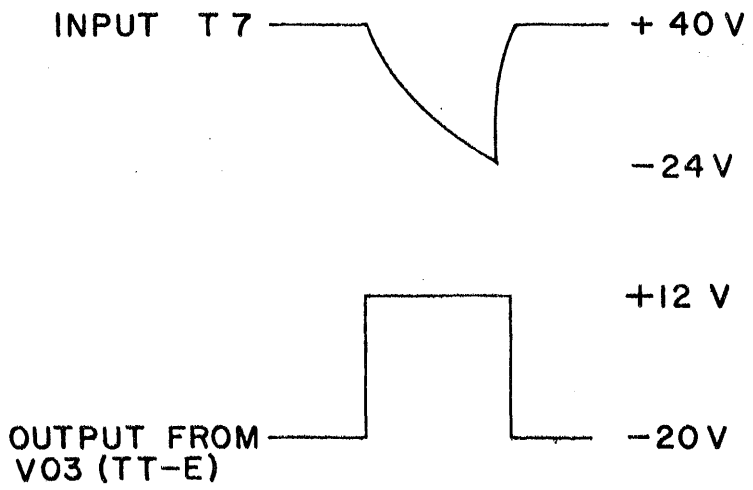


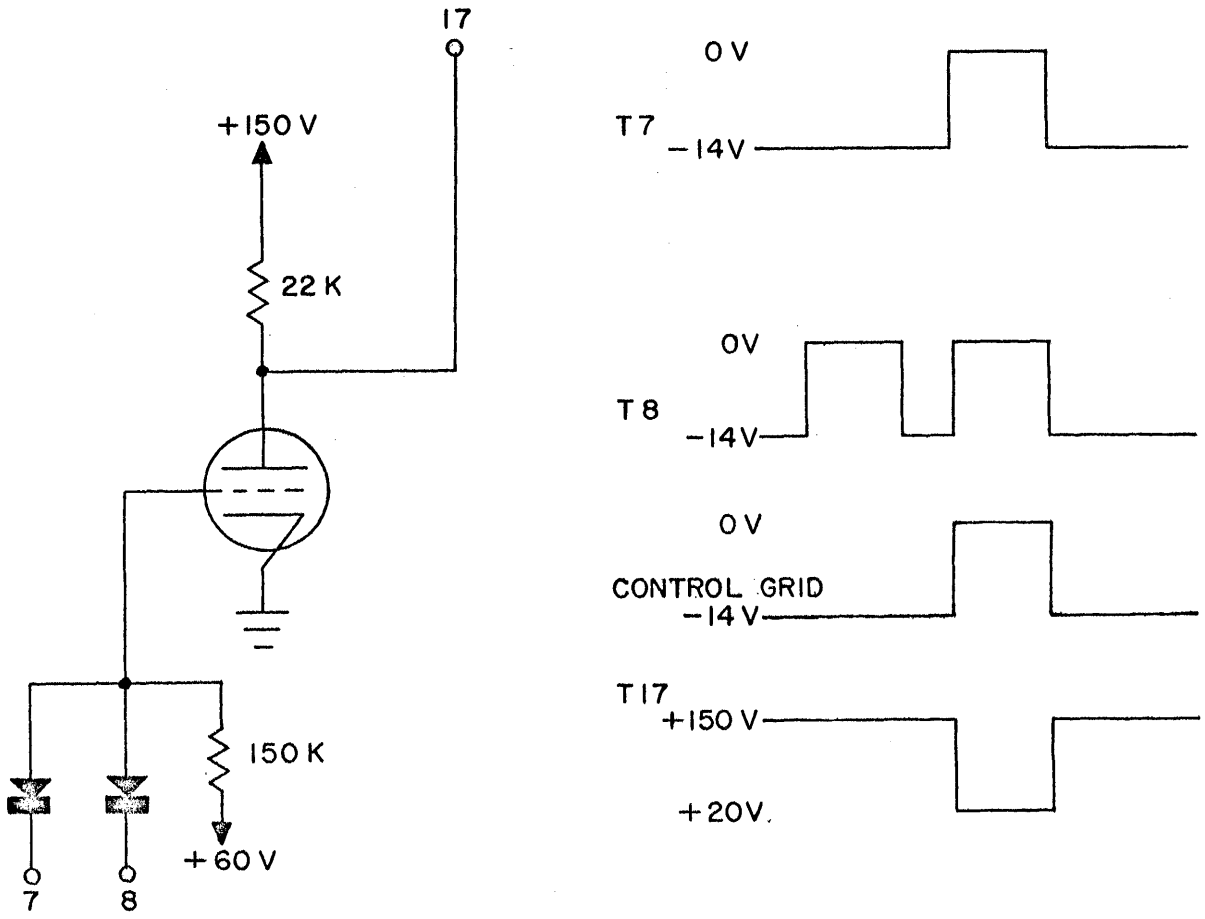
Figure 4-10. Magnetron Output Waveshape

w. CHASSIS TYPE 22, 6146 DRIVER. (Refer to XG188990). - This chassis is similar to the Type 6-6146 DRIVER, the difference being found in pulse transformers T05 and T06 and resistors R101 and R105. Two of these chassis produce output signals, of either 1 μsec or 2 μsec duration, that drive many circuits simultaneously.

On this chassis, T05 and T06 have a voltage step-down ratio of 5:1 as opposed to a 10:1 step-down ratio in the Type 6-6146 DRIVER, thus it delivers less power than the Type 6-6146 DRIVER. Resistors R101 and R105 are of a larger value (200 ohms as opposed to 47 ohms) to keep the load constant on the 6146 amplifiers by compensating for the change in the turns ratio of the pulse transformers.

x. CHASSIS TYPE 23, AND INVERTER. (Refer to XG189031). - This chassis contains eight diode AND circuits and eight inverter - amplifiers. There are five of these chassis utilized wherever the combination of an AND and an inverter is needed.

See figure 4-11(a). The output from the AND is equal to its most negative input. For example, if T7 is at 0v and T8 is at -14v, then the output from the AND is at -14v. If T7 is at 0v and T8 is at 0v, the output from the AND is at 0v, then the inverter conducts. See Figure 4-11(b). When the inverter is cutoff, the output at T17 is at +150v. When the inverter conducts, the output at T17 is at +20v.



a. Schematic b. Timing

Figure 4-11. AND Inverter

y. CHASSIS TYPE 24, MAGNETRON OUTPUT. (Refer to XG189060). - This chassis contains seven vacuum tube amplifiers (one of which may be used as a cathode follower) three diode OR circuits and six transistor amplifiers. Fifteen of these chassis distribute the outputs from the Magnetron Counters to the Diverters.

An input at T11 comes from a Magnetron Counter. If the Magnetron Counter is at a count that is not connected to T11 then T11 is at +40v. Amplifier V04A conducts. If the Magnetron Counter is at a count that is connected to T11, then a negative-going (+40v to -24v) signal appears at T11 cutting off V04A.

See figure 4-12. The positive-going output from V04A goes to amplifier V05 causing it to conduct. The negative-going (+5v to -20v) output from V05 goes to a diode OR, an indicator amplifier, and directly from the chassis via T12. The diode OR, consisting of diodes CR24 and CR25, produces a negative output if either input is negative. The input to CR25 from T9 comes from a Type 25 MAGNETRON OUTPUT chassis. The output from the diode OR goes through diverter amplifier Q06 and appears at T25 as a negative-going (-4v to -20v) signal. The purpose of the indicator amplifier consisting of transistors Q04 and Q05, is to turn on and off an indicator at the Supervisory Control Panel which indicates the count of a Magnetron Counter.

Vacuum tube V02B may be used as either an amplifier or a cathode follower. When V02B is used as an amplifier, the input is applied at T7 and the output appears at T6. When V02B is used as a cathode follower, the input is applied to T8 and the output appears at T20.

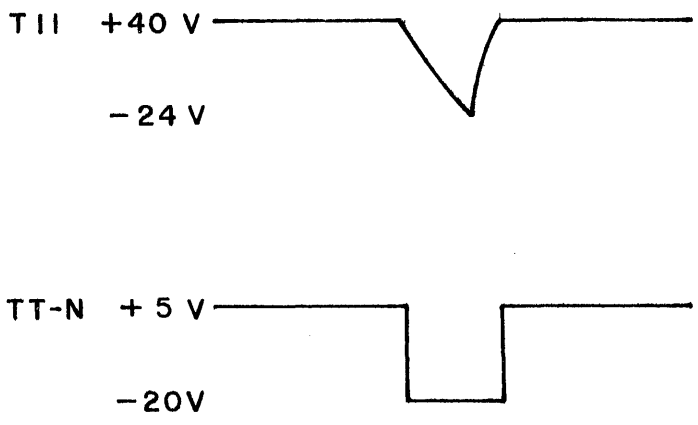


Figure 4-12. Magnetron Output Waveshape

z. CHASSIS TYPE 25, MAGNETRON OUTPUT. (Refer to XG189061). - This chassis contains seven vacuum tube amplifiers (one may be used as a cathode follower) a diode OR circuit, and six transistor amplifiers. Four of these chassis distribute the outputs from Magnetron Counters to the diverters.

An input at T15 comes from a Magnetron Counter. If the Magnetron Counter is at a count that is not connected to T15, then T15 is held at +40v. Amplifier V02A conducts. If the Magnetron Counter is at a count that is connected to T15, then a negative-going (+40v to -24v) signal appears at T15 cutting off V02A. See figure 4-13. The positive-going (+5v to -20v) output from V01 goes to a diode OR, an indicator amplifier, and directly from the chassis via T22. The diode OR, consisting of diodes CR21, CR22, CR24, CR25, CR26 and CR28, will produce a negative-going output for any negative-going input. The output from the diode OR goes through diverter amplifier Q09 and appears at T29 as a negative-going (-4v to -20v) signal. The purpose of the indicator amplifier, consisting of transistors Q07 and Q08, is to turn on and off an indicator at the Supervisory Control Panel which indicates the count of a Magnetron Counter.

Vacuum tube V02B may be used as either an amplifier or a cathode follower. When V02B is used as an amplifier, the input is applied to T7 and the output appears at T6. When V02B is used as a cathode follower, the input is applied at T8 and the output appears at T20.

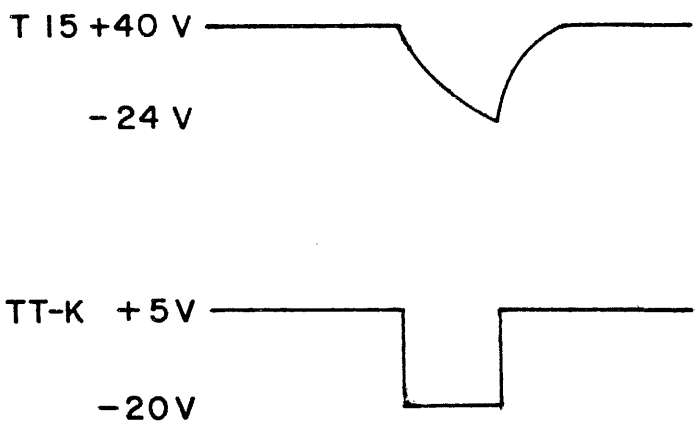


Figure 4-13. Magnetron Output Waveshape

aa. CHASSIS TYPE 26, N5 DISTRIBUTOR. (Refer to XG195997). - This chassis contains two N5 cores and 12 diode-resistor gates. There are four of these chassis utilized as intermediate storage between the Uniservos and the M2 register.

The N5 cores are held in the cleared state by the CLEAR HOLD signal, applied to T21, until reading of the Uniservo tape begins. The CLEAR HOLD signal is +5vdc, the absence of CLEAR HOLD is -40vdc. A reference voltage of -20v appears on T6. The purpose of the CLEAR HOLD signal is to prevent transients from being stored in the N5 cores. A "1" applied to T32 and T33 is fed through pulse transformer T01 and sets the N5 core. A "0", no signal, input causes the N5 core to retain a "0". A READ appearing on T19 is a positive-going (-30v to +5v) signal. If the core contains a "0" when the READ appears, the output of the core (at TT-A) is a positive-going (-14v to 0v) .2 μsec signal. If the core contains a "1" when the READ appears, the output of the core is a positive-going (-14v to 0v) 1 μsec signal. Appearing simultaneously with the READ signal is a positive-going (-30v to +5v) TRI signal.

The TRI signal is applied to two gates whose other inputs come from the cores. A "1" being read out of a core will alert six gates, one of which will be probed by the appropriate TRI signal. For example, a TRI-1 would pass through the gate consisting of diode CR20 and resistor R16, a TRI-2 would pass through the gate consisting of CR18 and R14, etc. An output from any gate is a positive-going (-30v to 0v) 1 μsec signal.

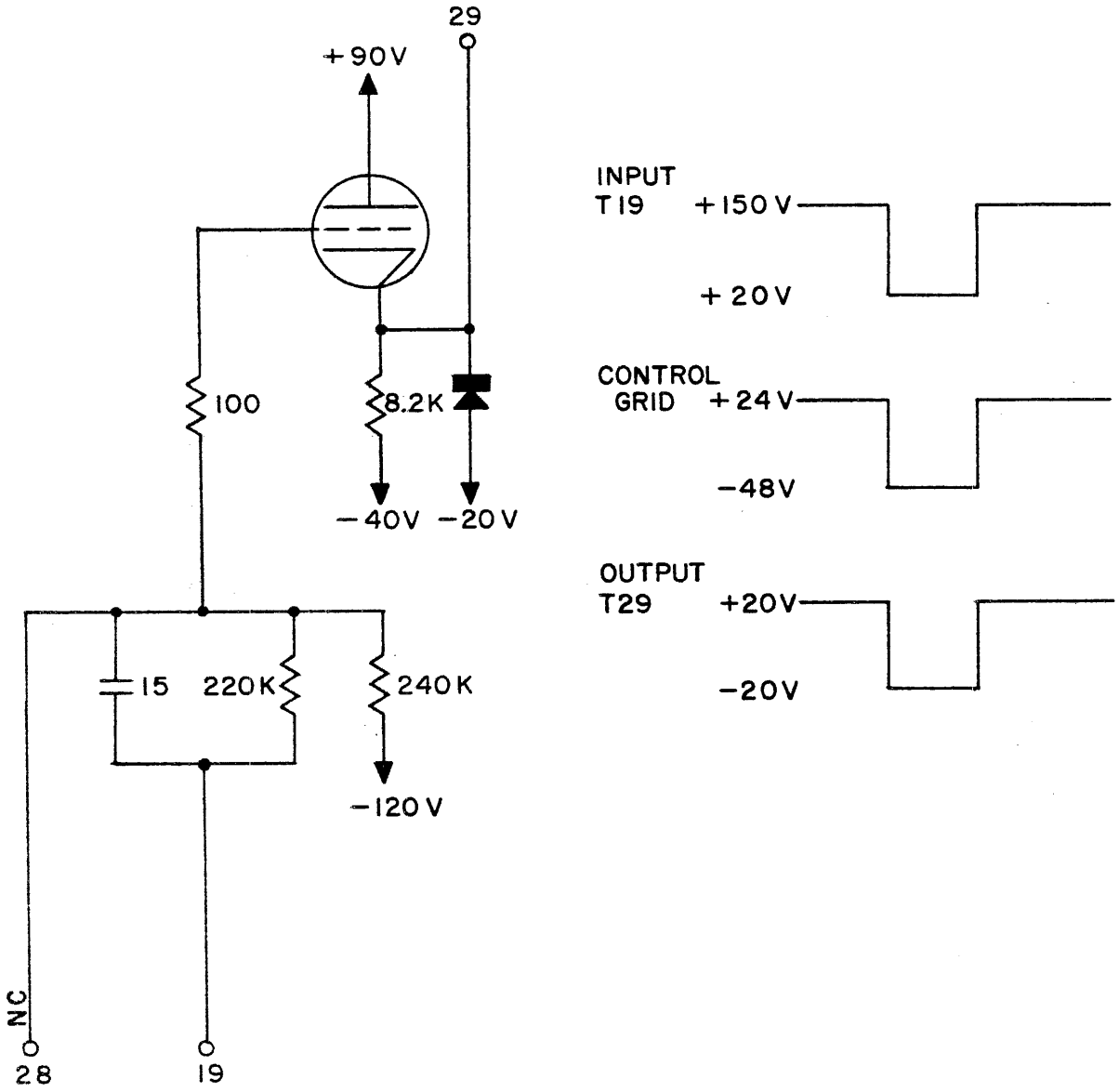
bb. CHASSIS TYPE 27, L & R DIVERTER BASE SWITCH. (Refer to XG196117). - This chassis contains four transistor switches, two transistor amplifiers and two emitter-followers. There is one of these chassis utilized to control current flow to rM "L" and rM "R".

The inputs appearing on T5 and T31 are from a flip-flop. Therefore, if the input on T5 is +5v then the input on T31 is -20v and vice-versa. If the input on T31 is +5v, it will pass through emitter-follower Q07 to amplifier Q01. Amplifier Q01 will conduct and its output at the collector will be -11v, which will turn off transistor switches Q03 and Q04. Turning off Q03 alerts the left (L) drive, while turning off Q04 inhibits the right (R) return. At this time -20v, appearing on T5 will pass through emitter-follower Q08 to amplifier Q02. This will prevent Q02 from conducting and its output at the collector (+30v) will alert transistor switches Q05 and Q06. Turning on Q05 alerts the "L" return while turning on Q06 inhibits the "R" drive. Thus, rM "L" is alerted and rM "R" is inhibited. To reverse this condition, it is necessary to change the state of the flip-flop so that T5 is +5v and T31 is -20v.

cc. CHASSIS TYPE 29, CATHODE-FOLLOWER. (Refer to XG105913). - This chassis contains eight cathode-followers. There is one of these chassis utilized to match impedance of an AND INVERTER with its destination.

See figure 4-14(a). The input appearing on T19 varies between +150v and +20v and is applied to a voltage-divider consisting of a 240K resistor and

a 220K resistor. The capacitor provides fast coupling of the input, thus, decreasing transient time of a signal through the chassis. See figure 4-14(b). The input to the control grid of the cathode-follower will vary between +24v and -48v. The output at the cathode will vary between +20v and -20v. The output from the chassis appears on T29.

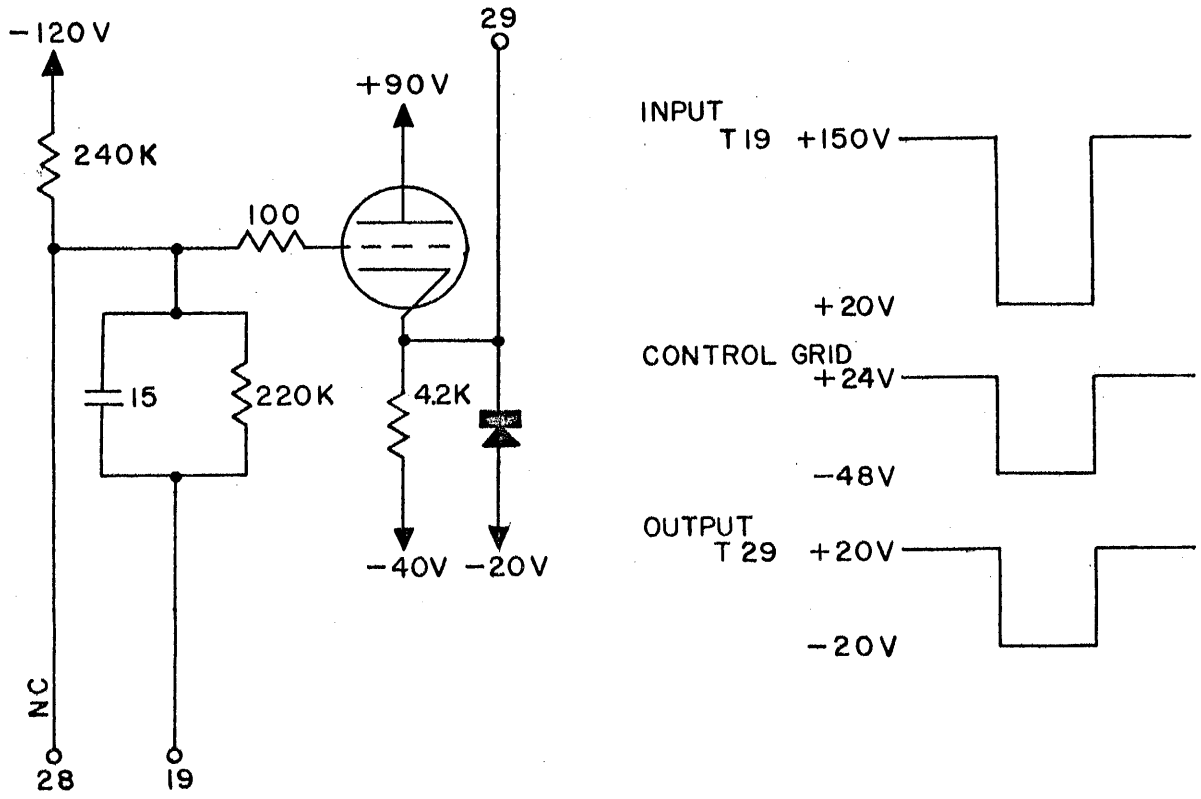


a. Schematic b. Timing

Figure 4-14. Cathode Follower

dd. CHASSIS TYPE 30, CATHODE-FOLLOWER. (Refer to XG106267). - This chassis contains eight cathode-followers. There are seven of these chassis utilized to match impedance of an AND INVERTER or an OR INVERTER with its destination.

See figure 4-15(a). The input appearing on T19 varies between +150v and +20v and is applied to a voltage-divider consisting of a 240K resistor and a 220K resistor. The capacitor provides fast coupling of the input, thus decreasing transient time of a signal through the chassis. See figure (4-15 (b). The input to the control grid of the cathode-follower will vary between +24v and -48v. The output at the cathode will vary between +20v and -20v. The output from the chassis appears on T29.



a. Schematic

b. Timing

Figure 4-15. Cathode Follower

ee. TRANSLATOR DIVERTER. (Refer to XG188871). - This chassis contains thirteen transistor gates, nine diode AND gates, nine transistor amplifiers and nine emitter-followers. Ten of these chassis decode the outputs of the addressing circuits into lines which select specific transistor gates which in turn will select specific cores in rM.

See figure 4-16. The inputs appearing on T9, T10 and T13 vary between -4v and -14v. If any one of the inputs is at -4v, the output of the AND will be -4v. The output of the AND is applied to the base of emitter-follower Q31. With -4v on the base of Q31, the signal at its emitter will be -4v. The output from Q31 is applied to the base of amplifier Q22. This will cause Q22 to conduct and the signal at its collector will be -11v. The output from Q22 is applied to the base of gates Q12 and Q13. Gates Q12 and Q13 will be inhibited with -11v on their bases. If the inputs appearing on T9, T10 and T13 are at -14v, then the output of the AND is -14v. With -14v on the base of Q31, its output, at its emitter, will be -14v. This will cut off Q22 and its output will go to +8v. Gates Q12 and Q13 will be alerted. Either T18 or T7 is terminated at ground, the other is terminated with an open circuit. For example, if T18 is terminated at ground, a Read or Write drive will appear at T1. This will cause Q13 to conduct. Current may flow in either direction through Q13 (from collector to emitter or from emitter to collector) depending on whether the drive line (T1) has a Read or Write drive applied to it.

ff. TRANSFER BUFFER DIVERTER. (Refer to XG188885). - This chassis contains thirteen transistor gates and nine transistor amplifiers. Six of these chassis are used to terminate the Y drive lines, right drive lines and the left drive lines in rI, rO and rZW.

See figure 4-17. The input appearing on T31 varies between the potentials of -4v and -14v. When -4v is applied to the base of Q13, Q14 conducts and its

collector will be at -11v. This will hold Q09 cut off. When -14v is applied to the base of Q14, Q14 will cut off and its collector will go to +30v. This allows Q09 to conduct. Current may flow in either direction through Q09 (from T18 to T32 from T32 to T18) depending on whether the drive line (T32) has a Read or Write drive applied to it. (Continued on Page 143)

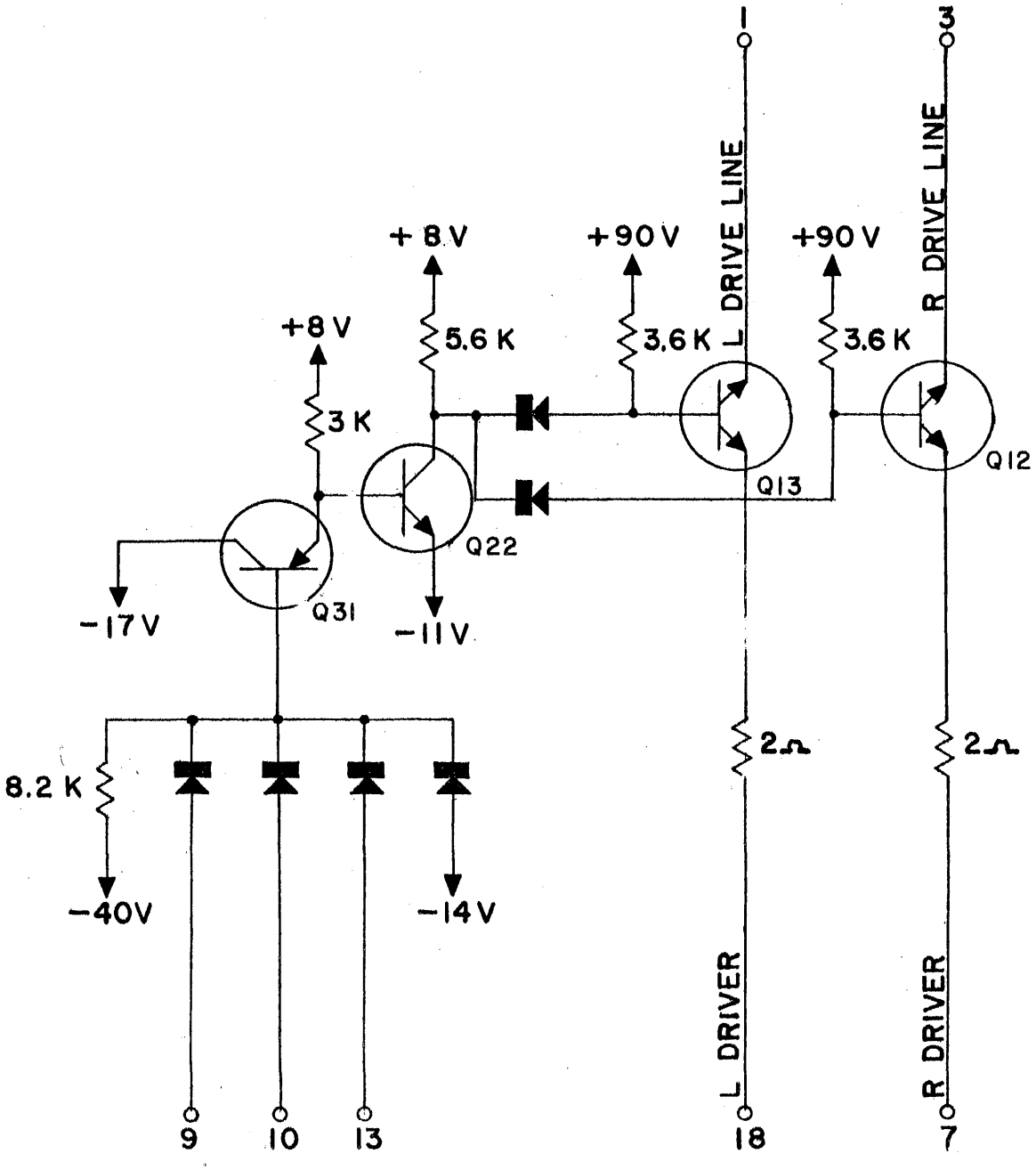


Figure 4-16. Translator Diverter

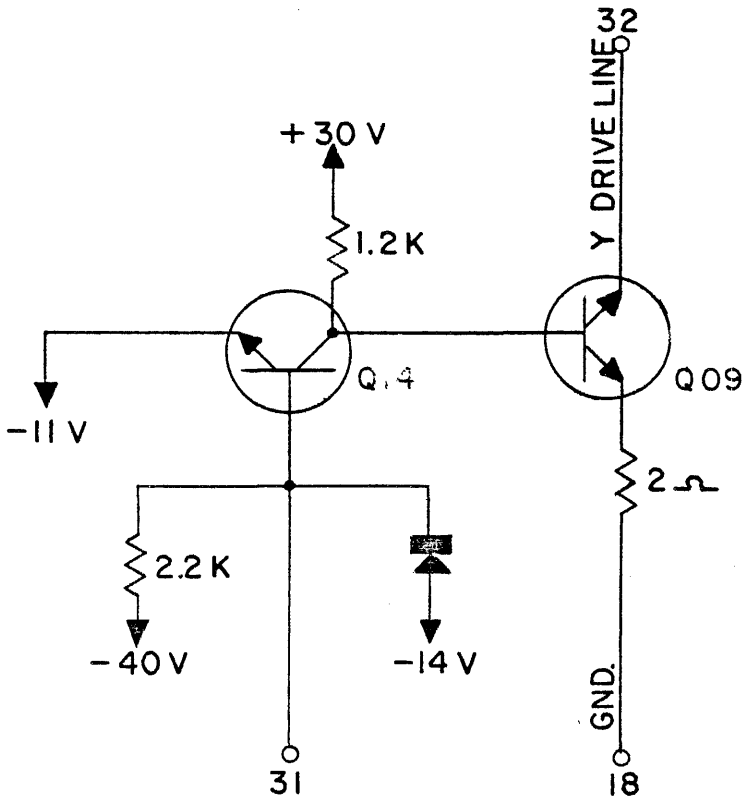


Figure 4-17. Buffer Diverter

(Continued from Page 141)

5. PROTECTIVE CIRCUITS OF CENTRAL COMPUTER

a. GENERAL. - The Central Computer is provided with numerous devices which protect the computer circuits against damage when malfunctions occur. These protective devices are described in the paragraphs which follow.

b. PROTECTIVE RECTIFIERS. - A protective rectifier is connected across each pair of clamping voltages used in a section. The rectifier is connected across the voltages at the W terminals of the section fuseboards. In the event that the clamping voltage that is further from ground becomes grounded, the rectifier shunts the initial surge of current around the clamping diodes to avoid diode overload. Shortly after such a short occurs, one of the fuses blows and turns off the d-c voltages.

The protective rectifiers are mounted on the tray assembly, directly above the bays they serve. As many as seven rectifiers may be mounted above a bay. The rectifiers of each bay are designated R1, R2, R3, etc., from left to right. The complete identification of a protective rectifier consists of its designation preceded by the bay designation. (Example: AR3 is protective rectifier R3 in bay A.) The locations and designations of all the protective rectifiers are shown in drawing XR106192: Modified Tray Assembly, Wired.

As part of computer maintenance, it is necessary to check the forward and backward resistances of the protective rectifiers. This check must be made with the rectifiers disconnected from the circuitry. A means for disconnecting the rectifiers above each bay has been provided in the form of Jones plugs in series with the cables connecting the rectifiers to the fuse panels of the bays. The connections between the rectifiers and the Jones plugs are shown in Appendix C , sheets 14 through 17. The connections from the Jones plugs to the W terminals of the fuseboards are shown in the Bay Assembly Wiring diagrams.

(Note: The Jones plugs are designated as IJQ and IJV in these diagrams; in Appendix C , sheets 14 through 17, the same plugs are designated as AJV, BJQ, BJV, etc.)

c. POWER FAULT CIRCUITS. - The Central Computer is provided with circuits which protect it against the occurrence of either a-c or d-c power faults. An a-c power fault occurs when excessive current is drawn from any a-c source by the circuits of the Central Computer or Power Supply. A d-c power fault occurs when excessive current is drawn from any d-c source by the circuits of the Central Computer.

(1) FUSES. - The a-c and d-c power lines of the Central Computer and Power Supply are fused by grasshopper-type fuses which initiate alarm action whenever a fault occurs. The fuses have three terminals, as illustrated in Figure 5-1. Normally, current from the power source passes from input terminal F to output terminal W through the fusing metal. When the fusing metal melts, the circuit from source to load is broken and the leaf spring is released. The leaf spring connects the source voltage to the alarm contacts, Q, of the

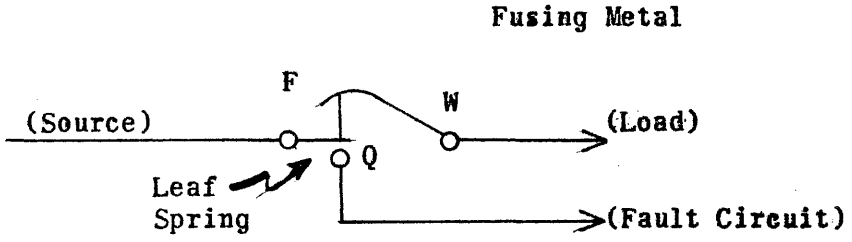


Figure 5-1. Grasshopper Fuse

fuseboard. Additionally, the upright position of the upper arm of the fuse gives a visual indication of the blown fuse.

In these cases where the maximum allowable load current exceeds the current rating of the largest available grasshopper fuse, a cartridge fuse of the

required size is connected in parallel with a grasshopper fuse of about I/10 the size. When the cartridge fuse blows, all the current is shunted through the grasshopper fuse, which also opens and closes the fault circuit.

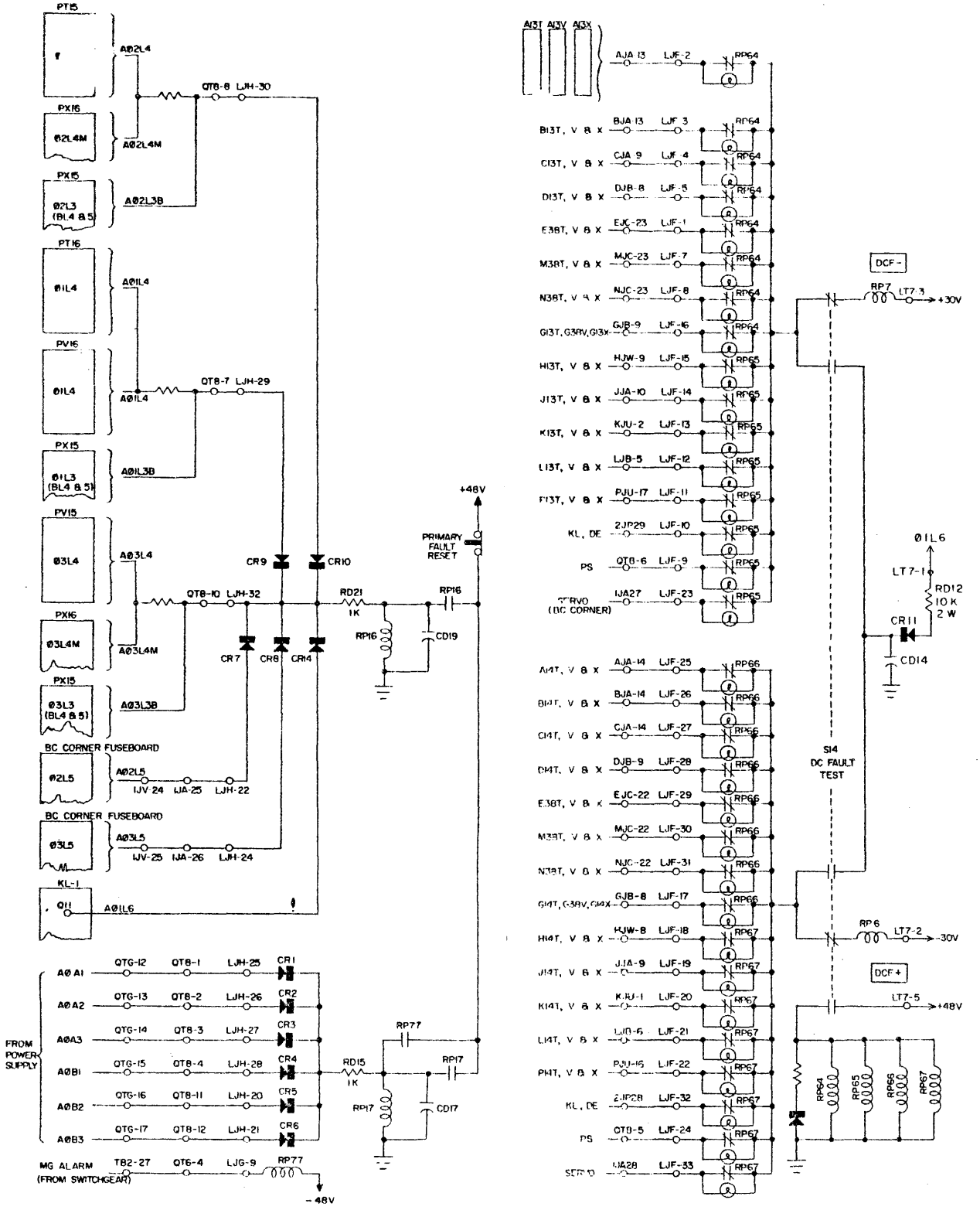
Tables 8-1 and 8-2 of Section 8 in this manual present the primary and secondary fusing of the power supply.

(2) AC FAULT CIRCUITS. - The primary circuits of all power transformers, in the Power Supply as well as the Central Computer, are fused. The transformers are divided into two groups: the a-c group and the d-c group. The a-c group consists of the transformers which provide power for heaters, blower motors, and Uniservos. The d-c group consists of the transformers of the Power Supply from which the rectifiers derive power. The a-c fault circuit is presented in Figure 5-2a.

The fuses of the a-c group are mounted on fuseboards PT15, PT16, PV15, PV16, PX15, and PX16 of the Central Computer. The a-c lines which are fused are as follows: Ø2L4, Ø2L4M, Ø2L3B, Ø1L4, Ø1L3B, Ø3L4, Ø3L4M and Ø3L3B. When a fuse in any of these lines blows, its alarm contact connects the line voltage to relay RP16 of KL corner. A set of normally-closed contacts of this relay opens the d-c interlock line to turn off d-c power. A set of normally-open contacts of the relay lights the HEATER PRIMARY indicator on the KL corner panel. The relay also has a set of holding contacts which close a "hold" circuit to +48v through the PRIMARY FAULT RESET pushbutton. Since this power source is not turned off by opening the d-c interlock, the alarm relay remains energized and the indicator lamp remains lit until the PRIMARY FAULT RESET pushbutton is depressed.

The fuses of the d-c groups are located inside the Power Supply and also inside the Alternator fuseboxes. The alarm lines of these fuses are designated

(Continued on Page 147)



a. AC Faults

b. DC Faults

Figure 5-2. Fault Circuits

(Continued from Page 145)
AØA1, AØA2, AØA3, AØB1, AØB2, AØB3 and MG ALARM, respectively. When a fuse of the d-c group blows, relay RP17 of KL Corner is actuated. A set of normally-closed contacts of this relay opens the d-c interlock line to turn off d-c power. A set of normally-open contacts of this relay lights the DC PRIMARY indicator on the KL Corner panel. The relay RP17 also has a set of holding contacts which close a "hold" circuit to +48v through the PRIMARY FAULT RESET pushbutton.

If the fuse in the output of either Alternator A or Alternator B blows, a rectified 400-cycle signal (MG ALARM) from the fuseboxes energizes relay RP77. When RP77 is energized a normally-open set of contacts cause RP17 to energize. RP17 performs the functions outlined in the preceding paragraph.

(3) DC FAULT CIRCUITS (Refer to Figure 5-2b). - The d-c voltages applied to each section of the Central Computer are fused by individual grasshopper fuses. The alarm contacts of all the negative voltage fuses of each bay (including the fuses for negatively-biased heater reference voltages) are connected to a common line, designated DCF-. The alarm contacts of all the positive-voltage fuses of each bay (including the fuses for positively-biased heater reference voltages) are connected to a common line, designated DCF+.

The d-c alarm lines from the section fuseboards, the KL and DE corner fuseboards, the BC corner fuseboards and from both the + and - fuseboards of the Power Supply are connected to the DC Fault circuit, in the KL corner. The DCF- lines are connected to relay RP7 through a normally-closed contact of the DC FAULT TEST switch and through normally-closed contacts of relays RP64 and RP65. The DCF+ lines are connected to relay RP6 through a normally-closed contact of the DC FAULT TEST switch and through normally-closed contacts of relays RP66 and RP67. When an alarm fuse opens, its contacts connect the alarm line to the supply voltage normally passed by the blown fuses. Either RP6

or RP7 is energized, and the normally open contacts of these relays open the d-c interlock circuit. As soon as d-c goes off, the alarm relay opens to close the interlock circuit again.

When the DC FAULT TEST switch is pushed down, it disconnects the alarm lines from the alarm relays and connects these lines to rectified and filtered Ø1L6. The normally open contacts of the switch connect +48v to relays RP64, RP65, RP66, and RP67. The normally closed contacts of these relays normally short out the d-c and heater fault indicator neons on the control panel. When the relays are energized, the short circuit is opened and any neon connected to a blown fuse will light, since it is bridged between Ø1L6 and ground through the Power Supply bleeder. The indicator neons are mounted in two horizontal rows on the KL corner panel. Those in the upper row are connected to the positive alarm system and those in the lower row to the negative alarm system. Therefore, by pushing down the DC FAULT TEST switch, the operator can determine in which bay the overload occurred, and also on which side of the bay the blown fuse is mounted.

d. INTERLOCK CIRCUITS. - The Central Computer and Power Supply is provided with an extensive interlock system which prevents d-c from being turned on unless the interlocks are closed. The interlock circuits are connected in series with relay contacts RP6, RP7, RP16, RP17, RP75 and RP51 of the Power Control System. An open-circuit in this line prevents RP47 from being energized; the contacts of this relay, in turn, prevent d-c from being applied to the Central Computer. (Reference: Paragraph 8-b (3g)

(1) PROTECTIVE RECTIFIER INTERLOCK CIRCUIT (Refer to Figure 5-3.) - The Jones plugs between the protective rectifiers and the section fuseboards are wired into an interlock circuit. Terminals 1 and 2 of the plugs are

(Continued on Page 150)

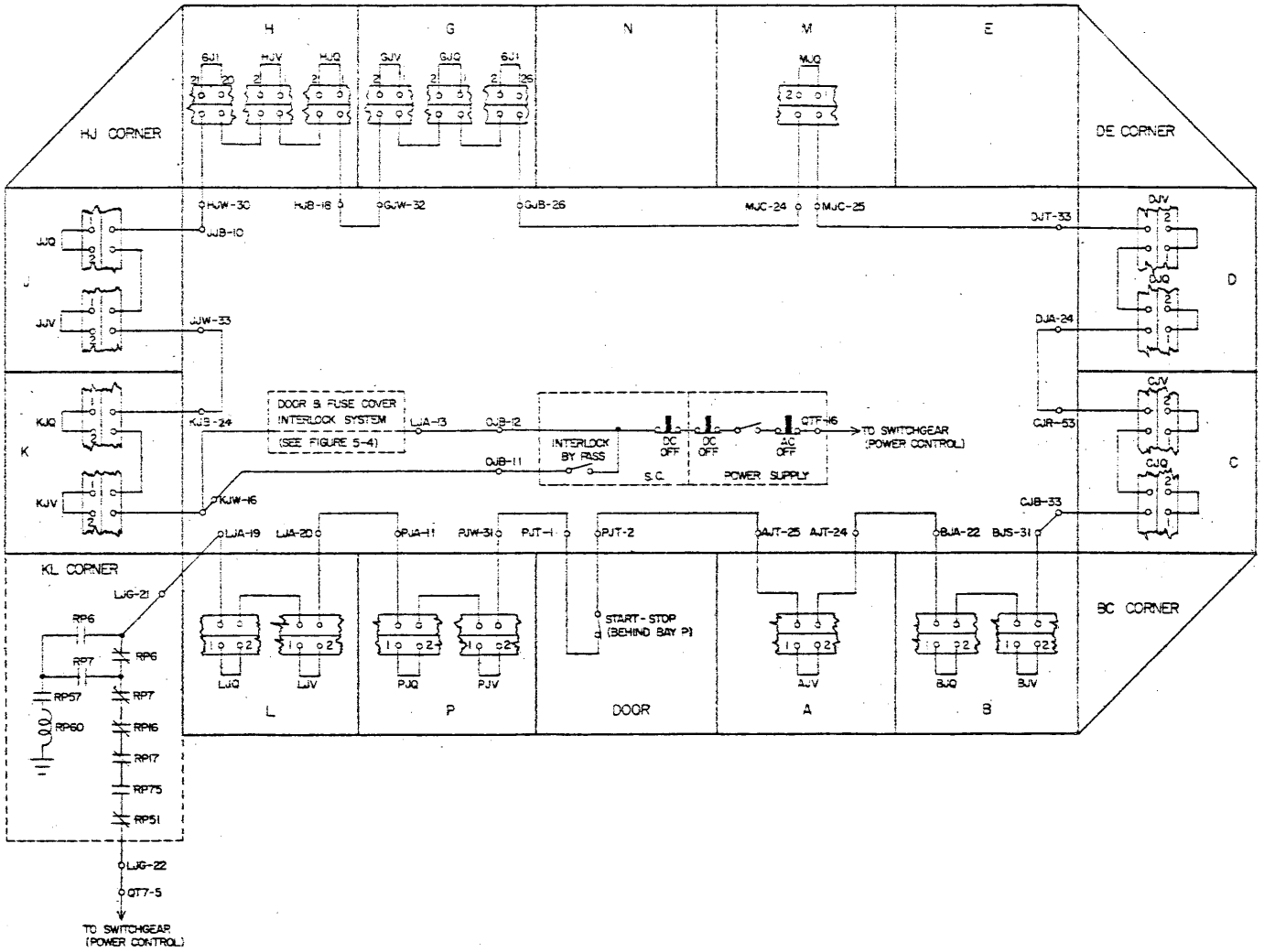


Figure 5-3. Protective Rectifier Interlock Circuit

(Continued from Page 148)
jumpered together while the corresponding terminals of the jacks are wired in series with those terminals of the other jacks. Thus, unless all the protective rectifier Jones plugs are connected properly the d-c interlock circuit will be opened.

(2) DOOR AND FUSE COVER INTERLOCK SYSTEM. - The fuse panels of the Central Computer and the Power Supply are covered by plastic covers for the protection of personnel. When a cover is properly in its place, a closed circuit is formed between terminals 27 and 28 of the fuse panel via a wire running the length of the cover.

A microswitch is mounted at the bottom of each door of the Central Computer and Power Supply in such a manner that when the door is open, the switch is open and when the door is closed, the switch is held closed.

The fuse covers and door switches of the Central Computer and Power Supply are wired in series in the manner shown in Figure 5-4. The door and fuse cover interlock circuit is, in turn, connected in series with the Protective Rectifier interlock circuit. Thus, if any fuseboard is uncovered, or if any door is open, d-c cannot be applied to the Central Computer.

The INTERLOCK BYPASS switch, on SC, is connected in parallel with the Door and Fuse Cover Interlock circuit. When this key-switch is closed, the Door and Fuse Cover Interlock circuit is disabled. This switch is provided for the benefit of maintenance personnel, and must be left open during all periods of normal operation of the machine.

e. OVERHEAT CIRCUITS. - A re-settable thermoswitch is mounted at the top of each bay of the Central Computer and Power Supply, and at the top of BC and HJ corners, to protect the equipment from local overheats. If an overheat condition develops within a bay, the thermoswitch of that bay opens to light

(Continued on Page 152)

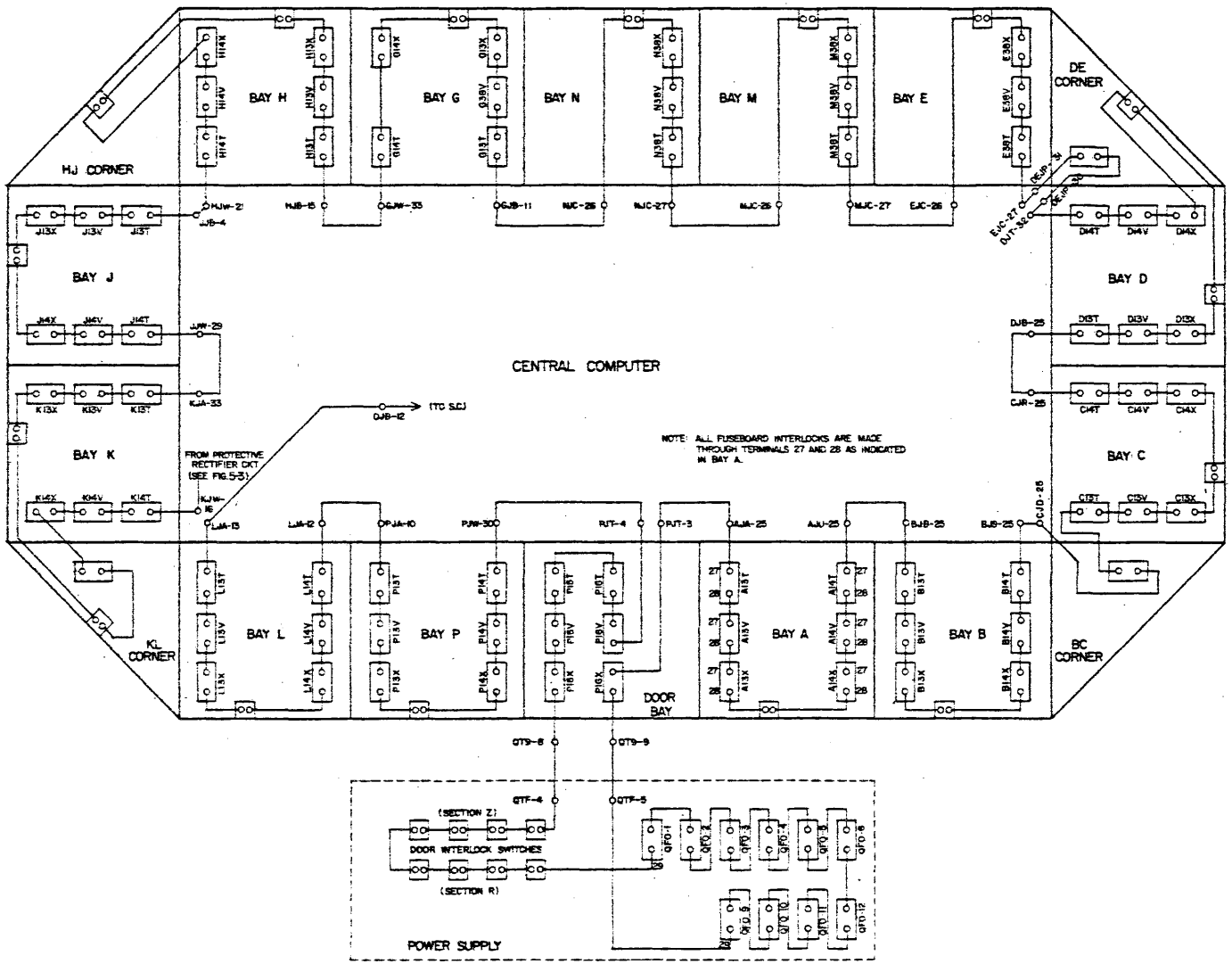


Figure 5-4. Door and Fuse Cover Interlock Circuit

(Continued from Page 150)
the HI TEMP indicator on SC and one or more of a group of indicators mounted on a channel of bay P. The temperature at which the bay thermoswitches open is preset and is not adjustable.

An adjustable temperature controller is mounted at the center of the Central Computer tray assembly to protect the equipment from a general overheat condition. This temperature controller is adjustable from $75^{o}F$ to $200^{o}F$. If the preset temperature is reached or exceeded, the thermoswitch opens to remove a-c and light the OVERHEAT indicator on SC.

The overheat circuits of the Central Computer and Power Supply are shown in Figure 5-5. The thermoswitches at the tops of the bays are wired in series. Thus, a bay overheat condition will cause its associated neon and all others above it to fire, the lower order neon being the only one of significance. The thermoswitches must be manually reset in order to re-apply power to the computer.

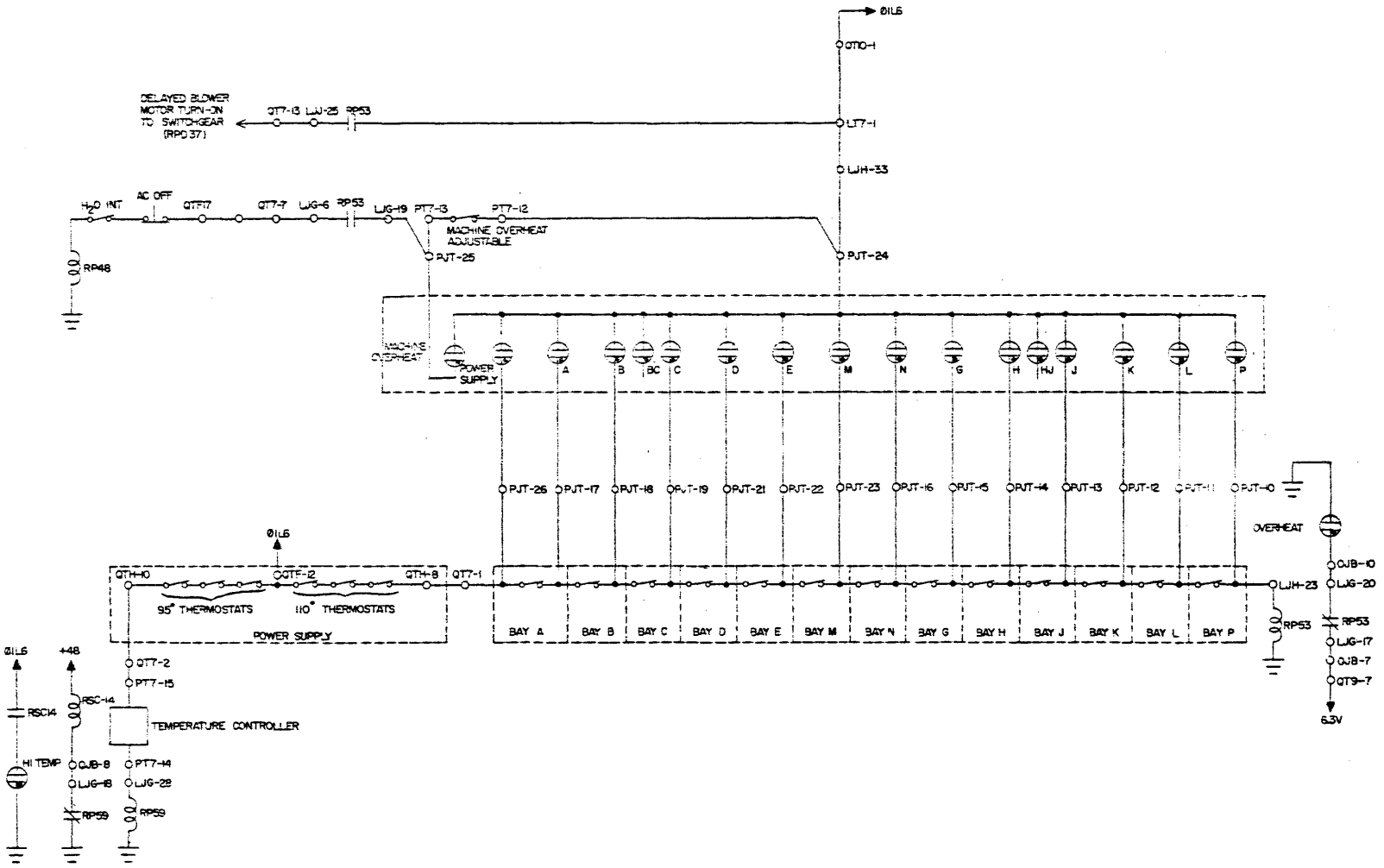


Figure 5-5. Bay Overheat and Hi Temp Circuits

6. SUPERVISORY CONTROL

a. GENERAL. - The Supervisory Control, SC, section of the Univac II system provides a means for supervising the processes of the computer. Through it the operator is able to monitor the routine being performed; determine if errors in the routine occur, and isolate most errors; and manually control the normal automatic program, if so desired. The controls for starting and stopping computer operation are also located on the SC console.

The SC Console, shown in Figure 6-1, is a standard office-type desk, on which is mounted the SC panel with its switches and indicators to the fore. Recessed into the console, in front of the panel is the SC Keyboard. A power receptacle and maintenance equipment jacks are located on the rear of the console. Drawers are provided for the convenience of the operator.

Generally, to the right of the console stands the SC Printer dolly, the SC output device. An interconnecting cable permits the intimate operation of the printer with SC.

Considered part of the SC group are three pieces of maintenance equipment: a monitor oscilloscope, a vacuum-tube voltmeter, and a multivibrator. The oscilloscope stands on a dolly to the left of the console and permits the operator to visually monitor the content of many circuits of the computer. A set of pushbuttons on the SC panel select the circuit to be viewed on the monitor oscilloscope. The vacuum-tube voltmeter operates with the TPG buttons, providing visual indication of the operation of the AGC of the various TPG's. The multivibrator operates the START circuits for certain maintenance routines.

Physically, the SC Console measures 4'3" high, 6'10" wide, and 2'9" deep. It weighs approximately 515 pounds. The SC Printer adjunct is 3'8" high, 2'5" wide and 1'9" deep; it weighs 270 pounds.

Figure 6-1. The Supervisory Control Console

In the computer group arrangement the SC section is positioned so the operator can observe the Central Computer, the Uniservos and the SC panel with ease. The only limitation on its position is the 25 foot maximum length permitted for the interconnecting cables between SC and the Central Computer.

b. SUPERVISORY CONTROL PANEL. - The Supervisory Control Panel provides mounting space for a number of control switches and indicators. The function and purpose of these switches and indicators are described in detail in Section 17 of the Theory of Operation manual, PX 695.

The Control Panel is hinged at the bottom allowing it to be tilted forward from its mounting to expose components mounted on its back. Retaining chains hold the panel in position such to facilitate access to the backs of all the switches and neons. A photograph of the rear of the SC Control panel is presented in Figure 6-2.

Doors on the back of the panel open to expose component locations within the panel mounting. Figure 6-3 shows the back of the panel mounting as seen with the access doors open. Along the bottom and the left side is a bank of connectors for the 37 cables which provide all of the interconnections for the SC.

Above the connectors are the mounting boards for much of the circuitry in SC. Facing the viewer and also perpendicular to the plane of vision toward the right are 16 terminal boards which provide mounting space for the filter networks of the SC circuits. These boards are identified TB01 through TB16.

Mounted perpendicular to the first four TB boards from the left are four decoder cards for the 1st and 2nd SR Instruction Digit Indicator panels. Two of the cards are associated with each digit; one card recognizes the zone setting, the other the numerical setting. An array of transistors compare the two signals and cause the aprropriate indicator to light. Schematic diagrams XG128648 and XG128672 show the decoding arrangement.

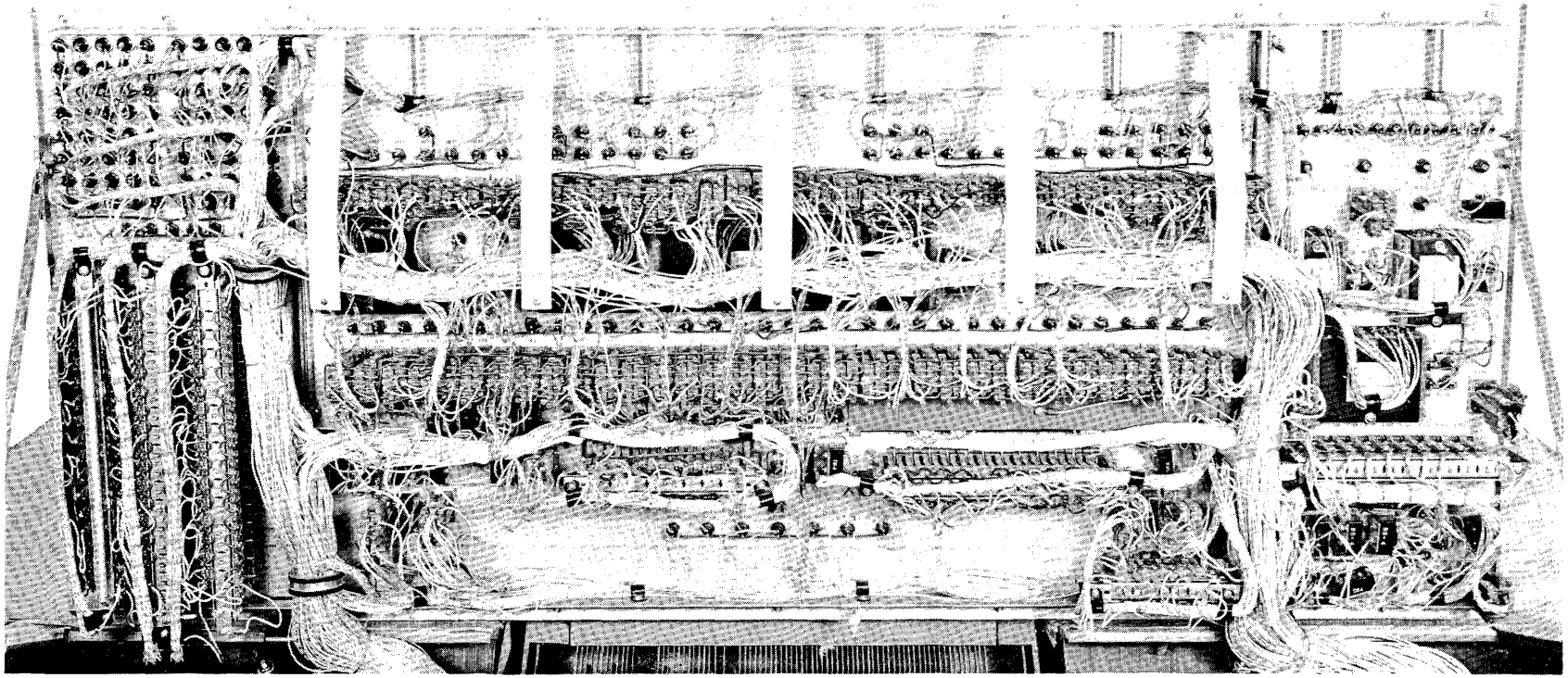


Figure 6-2. Supervisory Control Panel, Rear View

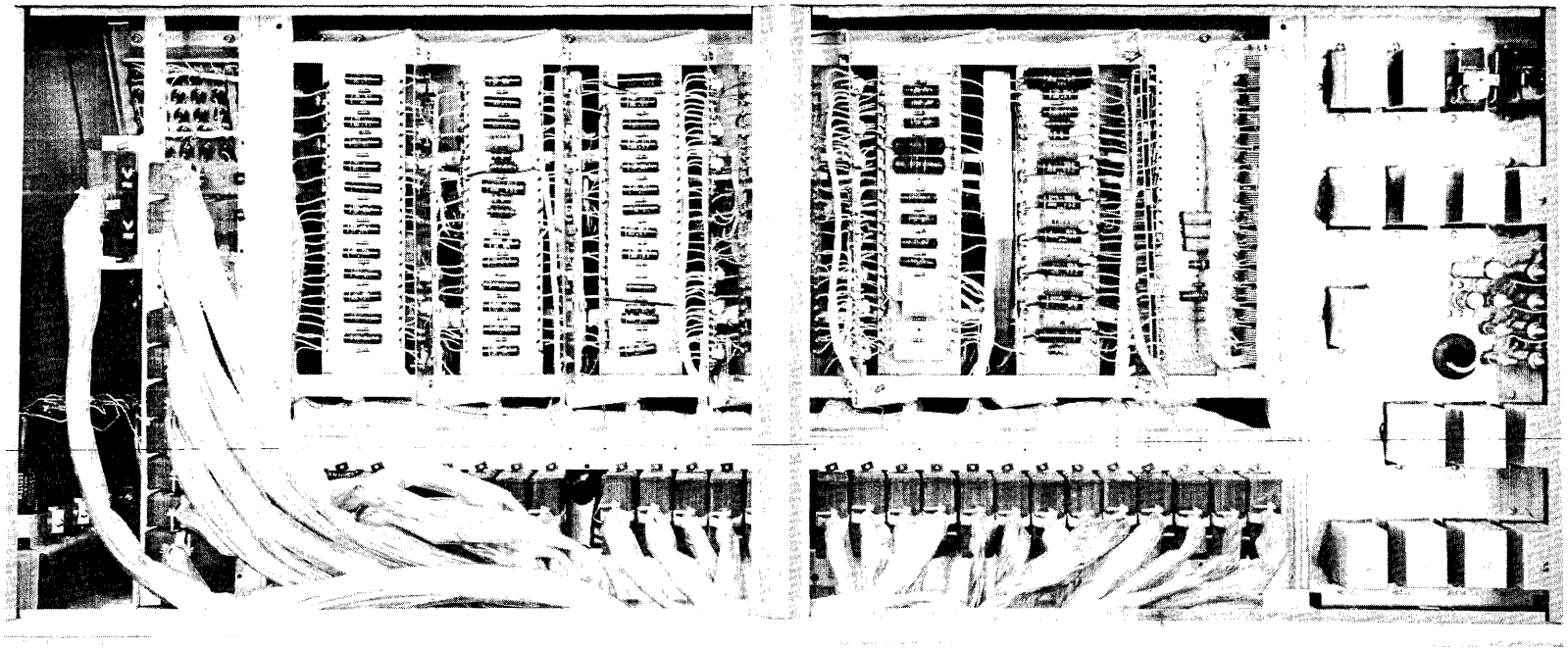


Figure 6-3. Supervisory Control Panel Mount, Rear View

To the right of the picture are shown sixteen relay boxes, numbered RSC1 through RSC16. These relays are identified by number, name and purpose in Table 6-1. To the left of the relay box panel is a bank of rectifiers which are involved in the relay circuits. In the midst of the relay boxes is located a group of special surge limiting resistors for the transistor circuits which control the numerical block indicators on the SC panel. In the extreme lower left hand corner are shown the large 500 uf capacitors which are used as filters for the COMMON KEYBOARD signal circuit.

TABLE 6-1

SUPERVISORY CONTROL MOUNTED RELAYS

NUMBER	NAME	FUNCTION
RSC1 RSC2	Clear C (A) Clear C (B)	Provide control for the performance of the CLEAR C function.
RSC3	Tank Clear (1)	Operate the Clear gate in the register re-circulation loops.
RSC4	Tank Clear (2)	Operate the stabilizing pulse insertion gates in the register re-circulation loops.
RSC5	CR Type-in	Initiates the SCI-CR operation.
RSC6	CU Clear	Operates gates in the 7 and 13-pulse loops in CU to clear and circulating pulses.
RSC7	CU Start	Operate circuits which introduce a single pulse into the 7 and 13-pulse loops in CU.
RSC8	SR Abnormal	Monitors the setting of the JAM SR switches.
RSC9	Error Delete	Monitors the setting of the ERROR DELETE switches.
RSC10	Type Out Register	Monitors the position of the TYPE OUT SELECTOR pushbuttons.

TABLE 6-1. SUPERVISORY CONTROL MOUNTED RELAYS (Cont'd)

NUMBER	NAME	FUNCTION
RSC11	Empty	Monitors the position of the CR INTERLOCK-FILL MEM switch and the EMPTY pushbutton.
RSC12	Servo Power	Applies +246 vdc to the Uniservos and applies power to the SC Uniservo control circuits.
RSC13	Retain Inst.	Fires the RETAIN INST or C indicator when the RETAIN C-RETAIN INST switch is operated.
RSC14	Hi Temp	Operates the HI TEMP neon for the condition of bay overheat.
RSC15	On Test	Causes the ON TEST indicator to light whenever any of the following maintenance switches are operated: MARGINAL CHECK, INPUT ERROR, RETAIN PC, WRITE END, READ END, SR 7AK7 MARGIN, STANDBY BELL LOCKOUT, VOLTAGE MONITOR LOCKOUT, VOLTAGE FAILURE BELL LOCKOUT, HI TEMP BELL LOCKOUT, NO RM RO, RM Bin 1, RM Bin 0, RZW Bin 1, RZW Bin 0, RI Bin 1, and RI Bin 0.
RSC16	Memory Clear	Provides signals which control the performance of the MEMORY CLEAR routine.
RSC61 (located behind the SC panel.)	Stand-by Power Monitor	Monitors the Stand-by Power circuits for the presence of -166S.

c. SUPERVISORY CONTROL KEYBOARD. - The SC Keyboard provides a means for manually entering words into the computer registers. The SC Keyboard unit is comprised of a 62 key keyboard, the keyboard switches and capacitors, and a resistor type encoding matrix. When one of the keys is depressed its switch is closed, causing the associated capacitor to discharge. The discharge is applied to the encoder. The pulse passes onto the output lines which are resistor connected to the switch line in the proper Univac coding combination for

the character. A signal is also transmitted along a line common to all 62 switches as the COMMON KEYBOARD PULSE. This signal controls the succession of characters from the keyboard. The seven lines carrying the character coding follow the course: Jones Plug LL to Jones Plug L in SC and thence to a 15 terminal Jones Plug in the base of Bay A in the Central Computer.

d. SUPERVISORY CONTROL PRINTER. - The SC Printer operates as an output device for limited quantities of register content. It also presents copy of the data entered into the computer via the SC Keyboard.

The SC Printer is a standard Remington Electric Typewriter and its mounting dolly. The unit stands to the right of the SC Console. The dolly contains two standard type chassis on which are located the relay decoding networks that actuate the type bars of the typewriter. A toggle switch on the right-hand chassis governs the print out when a non-printable character is coded. When in the "up" position the switch causes the printer to "hang-up" when a non-printable character is encountered. The "down" position causes a ; to be printed. The control circuits of the printer are located in the Central Computer. The printer is connected to the Central Computer via SC.

A panel of neon indicators on the left front of the printer dolly shows the code combination of the characters being printed. The bit significance of the neons is: the sprocket pulse lights the upper left-hand neon (this neon will always light) with the 1st, 2nd, and 3rd bits below it in that order; the second column of neons correspond to the 4th, 5th, 6th and 7th bits reading top to bottom. These neons can be an important aid in troubleshooting in that they will show improper pulses in any character being supplied to the printer.

To the right of the dolly top is a panel containing three switches and two neons. A two position rotary switch permits the operator to alter the normal

print-out routine in a manner that will cause the typewriter to print command characters but not respond to the commands. The typewriter fills each type-line at which time the carriage is automatically returned and shifted when it is operating in COMPUTER DIGIT. In normal operation the carriage return is a coded function.

A two-position toggle switch, labelled BRKPT, causes the printer circuits to react to the Breakpoint (β) symbol in the flow of type-out characters and at which event disengage the typewriter. A second toggle switch, SKIP, entirely disables the typewriter action. The SKIP switch does not interfere with the action of the printer relays and they continue to respond to pulses supplied to them by the Central Computer.

Two neons indicate the condition that has stopped the printer. The right neon fires when a BREAKPOINT has been decoded and the typewriter stops. The neon to the left fires when a STOP (Σ) has been decoded and the typewriter stops.

e. SUPERVISORY CONTROL INTERCONNECTIONS. - Communication between the SC group and the Central Computer is provided by a a group of 37 cables. These cables, containing a maximum of 33 individual wires, carry all voltages and signals required by SC. Thirty-five cables connect the Central Computer with SC and one cable each is supplied to the SC Keyboard and the SC Printer. The cables to the Central Computer terminate in a bank of Jones Plugs along the right side of the door bay and to the left of the bay A barrier strip. The cable terminations in SC are the Jones Plugs shown in Figure 6-2.

The Jones Plugs are called out alphabetically A through Z and AA through SS, omitting some of the letters. The content of the various wires within the interconnecting cables is identified in reference print XG142206. The cables are listed in the alphabetical order of the Jones Plug designation.

f. SUPERVISORY CONTROL MAINTENANCE EQUIPMENT. - Three pieces of equipment serve the operator and maintenance man in determining the proper operation of the computer via SC. These include a monitor oscilloscope, a vacuum tube voltmeter and a multivibrator. This equipment is not furnished with the system.

The monitor oscilloscope is a standard oscilloscope. The unit plugs into a receptacle located in the back of the console for power. Sweep-synchronizing signals and signals to be monitored are supplied by coaxial cables coming from the Central Computer. The SYNCH signal is the t90 pulse used for Synch around the Central Computer. The source of the signals to be examined is selected by a group of switches on the SC Panel (See Section 17i, PX 695).

The vacuum tube voltmeter is used to monitor the AGC of any one of the nine Timing Pulse Generators in the Central Computer. The set of pushbuttons used in the video monitor selection is also used to select the AGC circuit to be examined (See Section 17i, PX 695). The AGC is an indication of the condition of the tubes in the Timing Pulse Generator.

The multivibrator replaces the action normally provided by the Start Bar when a start pulse of a regular frequency is desired. When plugged into a jack on the rear of SC the multivibrator contacts parallel the Start Bar and provide entry for the substitute START signal generated by its flip-flop action. The frequency of the signal is regulated by a switch mounted on the multivibrator box.

7. UNISERVO II

a. GENERAL. - The principal external storage medium for the Univac II system is half-inch wide, .0011-inch thick metallic magnetic tape. Access to this storage is provided by the Uniservo II units. The Univac II system is designed to use up to sixteen Uniservos, designated 1, 2, 3, 4, 5, 6, 7, 8, 9, -, A, B, C, D, E, and F respectively as external storage devices. These function to move the tape past a read/write head; to receive information from the Central computer for recording on tape; and to read data on tape and transmit it to the Central Computer system. The Universo stores information on magnetic tape in the form of magnetized areas in eight channels across the width of the tape. Seven of these channels store data bits; the eighth contains sprocket, or timing signals.

b. PHYSICAL DESCRIPTION. - The Uniservo is composed of a tape-handling system, a magnetic read/write head, an erase head, a group of control relays, and a bad spot detector. The circuits and mechanisms involved are housed in a grey-wrinkle cabinet measuring 5' 2 1/4" high, 2' 5 1/8" wide, and 2' 8 15/16" deep. The weight of one unit is 725 pounds. A front view and rear view (with covers removed) of a Uniservo are presented in Figure 7-1 and 7-2. The location of major elements in the system are identified by callouts.

c. TAPE-HANDLING SYSTEM. - The main elements of the tape-handling system are the center-drive capstan, two tape reels, and two vacuum loops. The tape reels are rotated by their associated motors. For forward tape movement, the reels rotate in the clockwise direction while for backward tape movement, the reels rotate in the counter-clockwise direction. The center-drive capstan, connected to the center-drive motor by a clutch and brake system moves the tape past the magnetic read/write head at a speed of 100 inches per second. The low inertia of the center-drive capstan allows it to start and stop the

(Continued on Page 167)

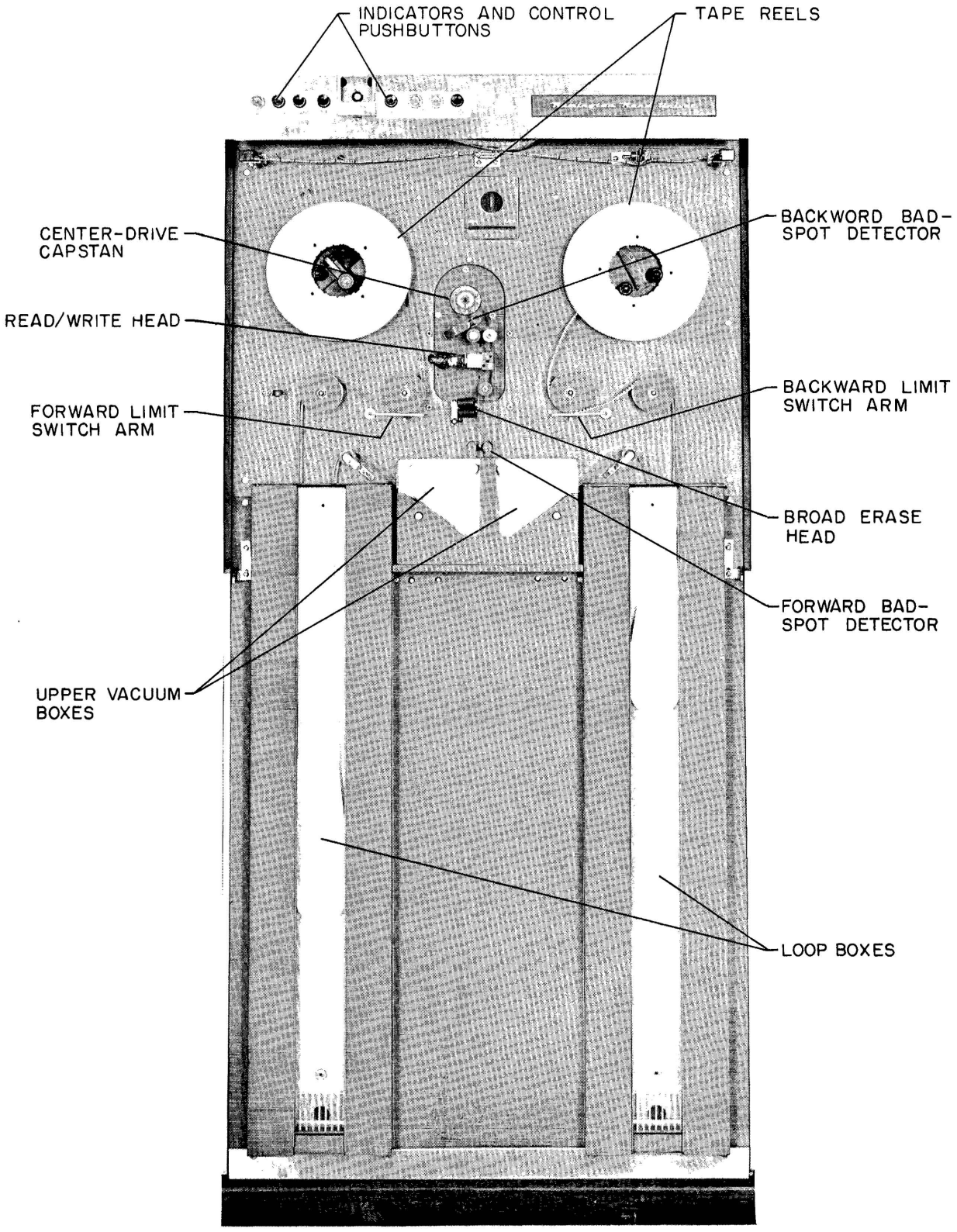


Figure 7-1. Uniservo II Front View (Cover Removed)

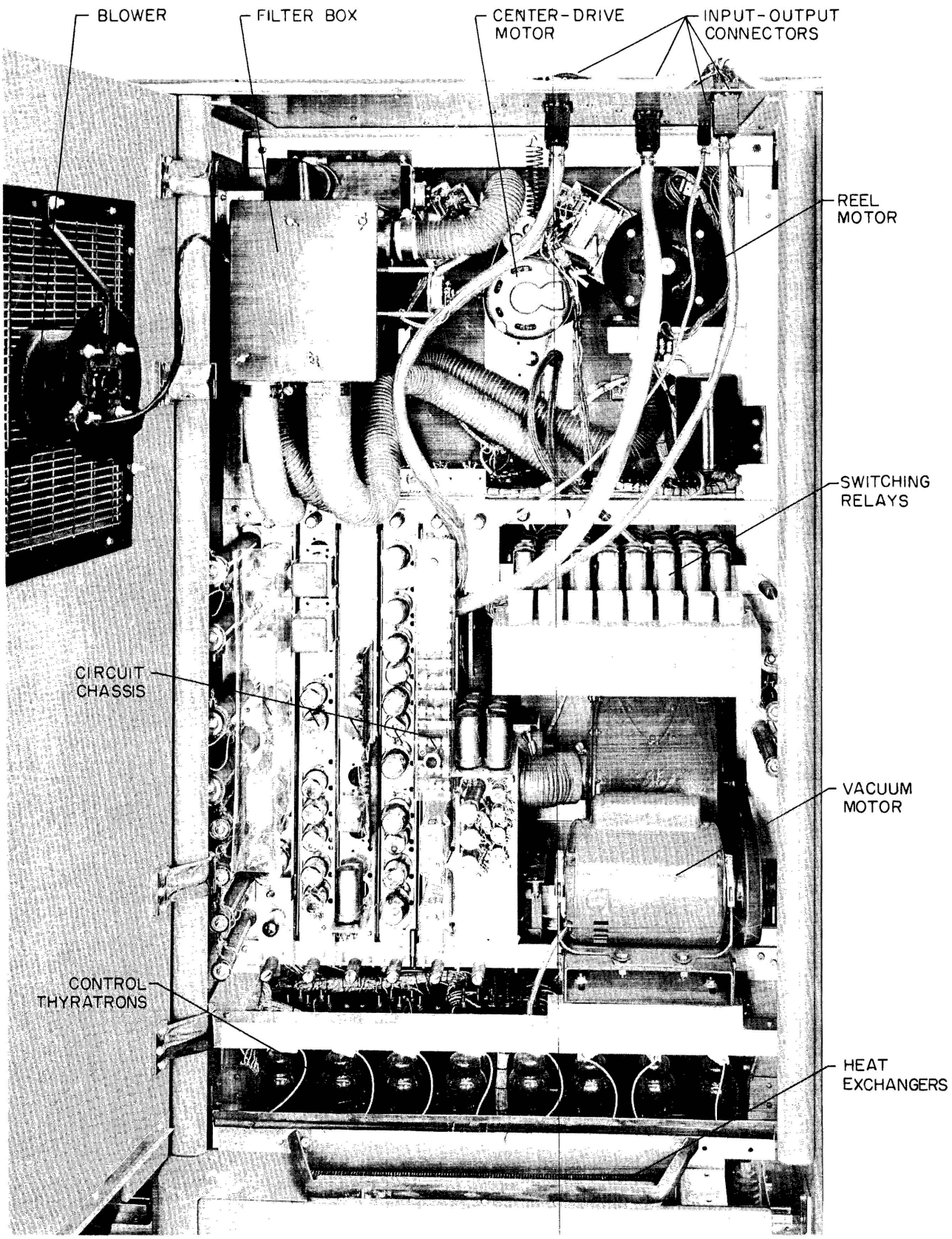


Figure 7-2. Uniservo II, Rear View (Door Open)

(Continued from Page 164)

tape more quickly than can the tape reels. The vacuum loops serve as buffer storage between the center-drive capstan and each tape reel, storing or supplying tape as necessary, to compensate for differences in speed between the center-drive and the tape reels.

d. READ/WRITE HEAD. - The read/write head of the Uniservo is made up of eight individual heads which are connected, via relay contacts, to respective reading and writing circuits in the computer. During write operation the write heads are connected to the "Write" flip-flops by the write relays, RW1 through RW16. During read operation the read relays RR1 through RR16 connect the read heads to the "Read" amplifiers in the Central Computer.

e. CONTROL RELAYS. - The Control Relays of the Uniservo II direct the performance of the reading, writing, and rewind operations. The principal control relays are listed below:

(1) MOTOR RELAY (RMO). - This relay is energized when the UNISERVO POWER ON pushbutton is depressed, and de-energized when the Main Interlock relay is energized. The normally-open contacts of the relay apply power to the Main Interlock relay circuit and to the Vacuum Motor relay - 2.

(2) MAIN INTERLOCK RELAY (RMI). - This relay is energized by the normally open contacts of RMO, if the left and right loop vacuum switches and thermal switch are closed, and if the backward and forward tape-limit switches are open. When this relay is energized, its normally-closed contacts de-energize RMO, while its normally-open contacts hold it self-energized and energize the Reel Motor relay.

(3) REEL MOTOR RELAY (RRM-1).- This relay is energized by the normally-open contacts of RMI. The normally-open contacts apply power to the Reel Motor Control system and the Center-drive motor.

(4) VACUUM MOTOR RELAY (RRM-2). - This relay is energized by the normally-open contacts of either RMO or RMI. The normally-open contacts apply power to the vacuum motors, and the lumilines.

(5) REWIND RELAY (RRE). - This relay is energized when the signals nS and REWIND are present at the Uniservo. The contacts initiate a Rewind operation within the Uniservo.

(6) REWIND INTERLOCK RELAY (RRI). - This relay is energized by the coincidence of the signals nS and RIR at the Uniservo. The contacts of the relay produce an interlock condition preventing further reference to the Uniservo.

(7) FORWARD RELAY (RF). - During normal operation this relay is energized by the coincidence of the signals nS and FP at the Uniservo. The contacts cause the Center-drive motor to rotate in the forward (clockwise) direction and place the loops in the forward static condition.

(8) BACKWARD RELAY (RB). - During normal operation this relay is energized by coincidence of the nS and BP signals at the Uniservo. The contacts cause the Center-drive motor to rotate in a backward (counter-clockwise) direction and place the loops in the backward static condition.

(9) READ RELAYS (RR-1 through RR20). - These relays are energized by the coincidence of the signals nS and RP at the Uniservo. The contacts of these relays connect the read/write heads of the Uniservo to the read amplifiers of the computer and place the Uniservo under Read control.

(10) WRITE RELAYS (RW1 through RW20). - These relays are energized by the coincidence of the signals nS and WP at the Uniservo. The contacts of these relays connect the read/write heads of the Uniservo to the write flip-flop of the computer and place the Uniservo under Write control.

(11) SERVO DIRECTION RELAY (RMF). - This relay communicates to the Input-Output Control section of the computer the direction of tape movement during a Read or Write operation. The normally-open contacts pass the forward signal, the normally-closed contact the backward signal.

f. BAD SPOT DETECTOR. - Uniservo II magnetic tape is inspected before it is to be used. Any areas in which recording may be unreliable are isolated by punching a series of holes 2 1/2 inches apart along their length on the tape. Two sets of detectors, one for forward tape motion and one for backward tape motion, recognize the presence of these holes and suppress the reading or recording operation while the "bad spot" area passes over the read/write head.

g. COOLING SYSTEM. - The Uniservo is air cooled by means of a closed cooling system. A centrifugal fan, mounted at the top of the rear door draws air from inside the Uniservo and forces it downward through a duct in the rear door and across heat exchangers located below the door. Cool water (45°F) is supplied to the heat exchangers to dissipate the heat. If the temperature of the air in the rear case exceeds 130°F, a temperature-sensitive switch in the main interlock system opens and removes a-c power from the Uniservo.

A small blower draws in some of the cool air and forces it through the filter chamber. The filtered air from this chamber flows through two ducts, supplying cooling for the two reel motors.

h. INTEGRATION OF THE UNISERVOS INTO THE SYSTEM. - Even though the Uniservos and the Central Computer have been individually checked out, certain additional checks must be made to insure their compatibility with the system. To become part of a system each Uniservo must be able to:

1. Read and write simultaneously in "continuous" for extended periods without error while first running systems test routines, and later sort routines.

2. Read tapes written by other Uniservos, in the same system or other systems, and by auxiliary equipment with a minimum of automatic rereads.

3. Write tapes readable on other Uniservos and auxiliary equipment with virtually no errors.

Some of the items to be checked in evaluating the effectiveness of a Uniservo in system are presented in the following paragraphs.

(1) PHASE SHIFT. - There must be no more than 2 microseconds time difference in the sprocket pulse and the pulse from any channel between writing and reading on the same Uniservo. This comparison is made at TT12 on chassis A4T and A5T (the positive-going portion of the signals).

Intraservo phase shift can be caused by poor quality heads, too much capacitance on the trellis, or by improper damping of the heads during a write. Poor read wave forms may cause trouble. Improper tape alignment along the tape path may be responsible for phase shift difficulties; however, this is considered doubtful. Write waveforms obtained in chassis A1 and 2X may be checked against those shown in Figure 7-3.

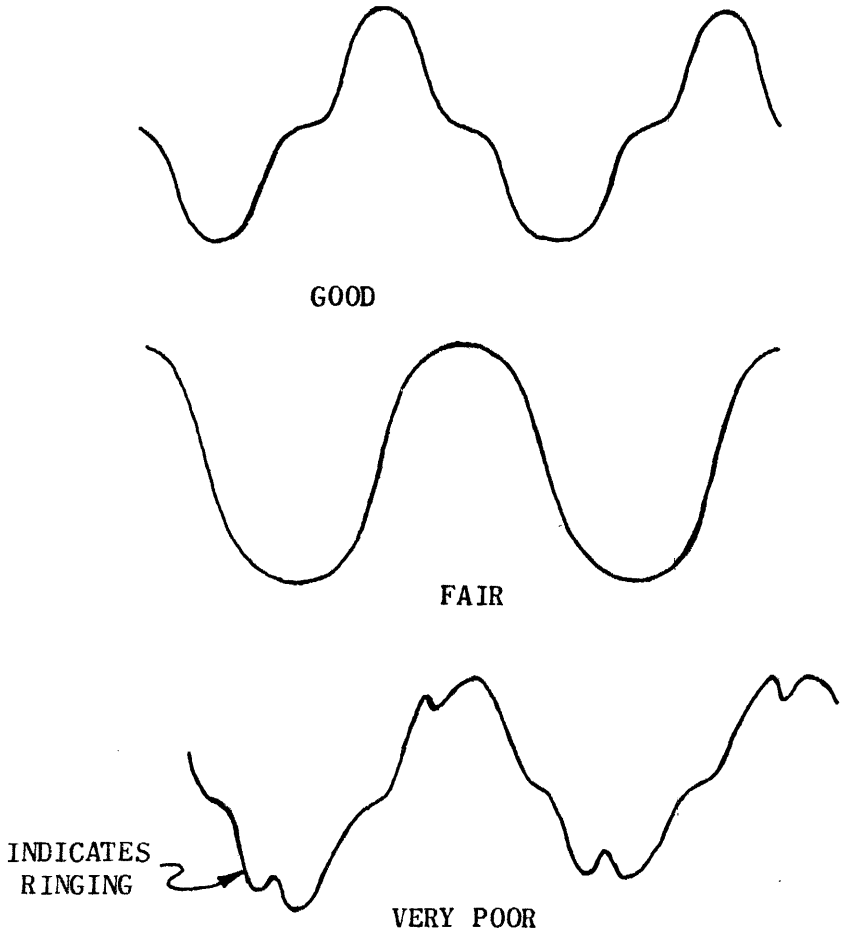


Figure 7-3. Write Voltage Waveforms

The following table may be used to record data for determining phase shift. Check proper read/write head damping and physical head gap by performing a read and a write on the same Uniservo. Record phase shift times microseconds. L = late, E = early. Place dual trace scope on "Chopped", sync on sprocket pulse at A5T, TT12 and compare the signal on other channel test terminals against the sprocket. Make sure the heads are clean. Maximum time variation $\pm 2\mu$ seconds.

		Channel Forward							Channel Backward						
Servo	Head	5	2	1	3	4	6	7	5	2	1	3	4	6	7
1															
2															
3															
4															
5															
6															
7															
8															
9															
-															
A															
B															
C															
D															
E															
F															

(2) SKEW CHECK. - A tape prepared on one Uniservo must have no more than 7 microseconds time difference between the sprocket pulse and the pulse from any accompanying channel when read by any of the other Uniservos. This comparison is made at TT12 on chassis A4T and A5T (the positive portions of the signals only).

Interservo phase shift, or skew, has the same causes as outlined above for Phase Shift, with poor tape path alignment a greater possibility.

The following table may be used for performing a check on phase shift compatibility of Uniservos within a system and also between Uniservos of different systems. Using a dual trace scope set on "Chopped", read a tape on all Uniservos. Sync on the sprocket signal at A5T, TT12, using a probe for a sync lead. Compare the channel pulses against their accompanying sprocket. Record the time variation on the chart. The maximum allowable time variation is ±4 microseconds. The read/write heads must be clean.

If the skew checks do not come within allowable tolerances it may be necessary to run a head selection check to determine if the trouble lies in the head switching box, the guiding system or the heads themselves. This routine should develop compatibility within any particular system. The procedure for the head selection test is as follows:

1. Select the head with the least phase shift and mount it in a good Uniservo.
2. Prepare an "All Ones" tape with this head and read this tape forward, recording the phase shift.
3. Using the prepared tape as a standard, tabulate the skew for all other heads by mounting them in place of the head used in preparing the tape. Measure skew while reading forward.
4. From data obtained, plot a distribution curve for each channel.
5. Select heads whose channel peaks fall within ±1 microsecond of the standard tape.

		Channel Forward							Channel Backward						
Servo Head		5	2	1	3	4	6	7	5	2	1	3	4	6	7
1															
2															
3															
4															
5															
6															
7															
8															
9															
-															
A															
B															
C															
D															
E															
F															

6. Determine the variations of all of the available read/write heads, grouping them by tolerances ±2, ±3 and ±4 μseconds. (The maximum allowable skew on a head is normally ±4 μseconds when tested by the manufacturer.)

7. If sufficient heads are available it should be possible to set up a system whose heads have a skew of less than ±3 μseconds from each other, ±4 μseconds is the maximum allowable.

(3) NOISE CHECK. - Total noise cannot be greater than 2 volts zero-to-peak, during any read; total hum no more than .6 volt, peak-to-peak. To accomplish a noise check, a write is performed on the most distant Uniservo without moving the tape. Every effort is then made to produce noise, such as; turn other Uniservos off and on, run the center-drive on other Uniservos, reverse direction on other Uniservos, and operate any Uniservo buttons. The noise level is checked at TT11, chassis A4T and A5T.

Four checks for noise are performed; two for operational noise and two for cross-talk. These checks are made after the system has been calibrated. The gain switch on SC is placed in the "HIGH" position. Oscilloscope patterns of the noise generated during each test are viewed and the voltage maximum for each channel of each Uniservo head is recorded on a chart. The particular procedure and chart for voltage tabulation of each test is presented below:

(a) OPERATIONAL NOISE CHECK 1. - Initially a "read" line is picked up on Uniservo "A". The other Uniservos turned on and off and the peak voltage values for each channel are recorded. Maximum permissible operational noise is 2 volts, zero-to-peak.

Servo Off And On	5	2	1	3	4	6	7	8
1								
2								
3								
4								
5								
6								
7								
8								
9								
-								
B								
C								
D								
E								
F								

(b) OPERATIONAL NOISE CHECK 2. - Uniservo "A" is turned on and off while the read line for each of the other Uniservos is picked up in turn. The peak voltage of noise created by turning Uniservo "A" off and on while observing each channel is recorded. Maximum permissible operational noise is 2 volts, zero-to-peak.

Read On Servo	Channel 5	2	1	3	4	6	7	8
1								
2								
3								
4								
5								
6								
7								
8								
9								
-								
A								
B								
C								
D								
E								
F								

(c) READ/WRITE CROSS-TALK 1. - This test is performed by picking up a "read" on the Uniservo under test and writing on the most distant Uniservo in the system. Set the oscilloscope on bright trace and sync on START WRITE. Record the hum on the read line in volts from peak-to-peak, and the cross-talk for each channel in zero-to-peak volts. Maximum voltage tolerance allowed between limits is 2 volts.

Write on _____

Read On Servo	Channel 5	2	1	3	4	6	7	8
1								
2								
3								
4								
5								
6								
7								
8								
9								
-								
A								
B								
C								
D								
E								
F								
hum								

(d) READ/WRITE CROSS-TALK 2. - With a "read" picked up on the Uniservo most distant, perform a "write" on the Uniservo under test. Synch the oscilloscope on START WRITE. Record the zero-to-peak voltage of the noise generated. Maximum permissible reading is 2 volts.

Read on _____

Write On Servo	Channel 5	2	1	3	4	6	7	8
1								
2								
3								
4								
5								
6								
7								
8								
9								
-								
A								
B								
C								
D								
E								
F								

Solving noise problems is a tedious process. It is necessary to first isolate the area in which the noise pick-up is made. If noise is picked up in the trellis, it will be necessary to check the grounding system, the shielding, the shield bonding and cable placement. Read cable shields should be grounded at A1 and 2T only.

If noise originates in the Uniservo, check out the relays individually, i.e., arrange the Uniservo so that RMO only will operate, then RMI, then the vacuum motor relay, etc., until the trouble source can be identified. Noise suppressors have been provided but these may be miswired or inadequate. Occasionally a Write or Read relay may fail allowing cross-talk into the read circuitry.

(4) SCALLOPING. - Scalloping of the read waveform must be checked during both reading and writing. Observe the read waveforms during a "Sort" routine, at which times various duty cycles are present. If any particular Uniservo is suspected of causing trouble use "nS" as an oscilloscope sync.

The most obvious causes for scalloping are friction, tape slippage and loss of contact with the head. Check the following items if friction is suspected:

1. Lubrication and cleanliness of the Idler and Roller shafts.
2. Mechanical alignment of the tape paths, which includes all idlers, the capstan, the loop boxes and the reels.
3. Conductivity of loop box side glass. Observe for a tendency of the tape to stick to the glass. The glass should have less than 2 megohms resistance measured across its length. Do not take the boxes apart for this measurement. Arrange a factory return.

Tape slippage problems generally result from too much friction everywhere except on the capstan. Clean the capstan with chlorothene. Check vacuum pressure to ensure that sufficient tension exists in the tape loops. Dirt must be kept from the vacuum hole screens.

Loss of tape contact with the read/write head is unlikely; however, it may occur if resonances occur in the tape tension system. Folds in the tape cause the tape to lose contact; these must be punched out.

(5) TAPE SPEED CHECK. - Tape speed must not vary more than 5% from the nominal 100 inches per second velocity. A tape speed check can be made with a Strobotac during steady tape motion. Nominal large idler speed is 955 rpm. Check forward and backward motion. Difference in direction speeds may be caused by a wrong side phase shift capacitor on the motor. Its normal size is 6 μf.

A maximum time of 5 milliseconds is permitted to accelerate tape to full speed or to decelerate it to a full stop. A special test tape in which channel 5 has been recorded solidly and the other channels have normal block spacing is prepared to test acceleration time. Using a dual trace oscilloscope on "Chopped", sync on the RCDC signal. Observe RCDC and Channel 5. The pattern should resemble the drawing below. Make certain the Uniservos are clear before performing this test.

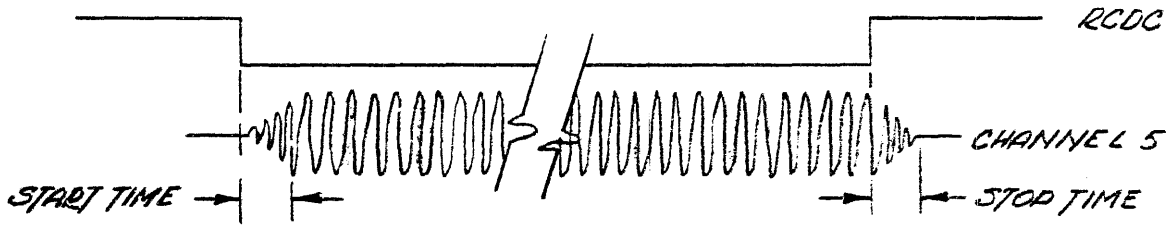


Figure 7-4. Tape Acceleration Test Pattern

Servo	C.D.No.	Fwd.Start	Fwd.Stop	Bwd.Start	Bwd.Stop
1					
2					
3					
4					
5					
6					
7					
8					
9					
-					
A					
B					
C					
D					
E					
F					

(6) TIMING CHECK. - The timing of the delay-flops in IOC must be within 5% of their nominal values to ensure proper spacings on the tape. A visimag spacing, blockette spacing, and block length. No difficulty should be experienced in meeting the below listed tolerances if delay flop timing, tape speed, and acceleration have been within their prescribed limits. The following tolerances are allowed:

Interblock spacing

250 ppi or 50 ppi density - nominal space - 1.05 inches; maximum - 1.32 inches; minimum - 0.81 inches

125 ppi density - nominal space - 2.4 inches; maximum - .219 inches; minimum - 2.0 inches

Block length

250 ppi density - 2.85 $\pm$ .14 inches

125 ppi density - 5.75 $\pm$ .29 inches

50 ppi density - 14.4 $\pm$ 1.16 inches

Blockette spacing

normal 1.0 $\pm$ 0.1 inches

short 0.1 $\pm$ .01 inches

i. OPERATIONAL ADJUSTMENTS. - Section 5 of the Uniservo II Manual, Philadelphia Publication U-1630.1 lists the procedures for the mechanical alignment and adjustments necessary to accomplish smooth and efficient Uniservo operation. In addition this section presents the regular schedules recommended for proper equipment maintenance.

j. UNISERVO II. - Final Operational Check List - A convenient check-off list for Uniservo condition, intended primarily for Installation personnel but also useful to maintenance, is presented in the publication "Acceptance Specification for Univac II Computer System", PX , Section 4.9.1.14.

k. ADDITIONAL INFORMATION. - Appendix G of this manual, entitled "Input-Output Adjustment Criteria" presents additional information on problems encountered in tying the Uniservos into the system.

PX 697A

8. POWER SYSTEM

a. GENERAL. - Univac II system power is provided by four units: (1) Main Transformer (2) Switchgear (3) Motor-Generator (or Alternator) and (4) Power Supply. The Power Supply assembly provides all d-c power requirements for the Central Computer and associated equipment; a-c voltage requirements are supplied from the Main Transformer (via the Switchgear) or by the Switchgear. The Motor-generators provide a 400-cycle a-c voltage for the Power Supply primaries and is connected to the latter via the Switchgear. The Switchgear acts as the central power station for all of the equipment (with the exception of d-c power leaving the Power Supply) and the control of power is provided at the Switchgear, a Switchgear control panel is located on the Power Supply but is not an integral part of the Power Supply.

A Univac II installation operating with sixteen Uniservos requires 135 kva, not including power for the chilled water system. The primary power source will be three-phase, 60 cycle, 480 vac (3- or 4-wire), 240 vac (4-wire), or 208 vac (4-wire). The line voltage is monitored for variation under all conditions. Voltage variations of not more than $\pm 5\%$ are optimum, with $\pm 9\%$ being acceptable based on voltages of 440, 230 or 208 vac.

The primary line input voltage affects the internal connections and components of the Switchgear unit and Main Transformer. In the case of 440 vac line voltage, a 112.5 kva transformer is used and the Switchgear is designed and built for an input of 440 vac. For 230 and 208 vac primary voltages a 75 kva transformer is used, and either of two different Switchgear units are used. Three block diagrams showing the various arrangements for the different primaries are shown in Figure 8-1. (Power Distribution from Various Sources).

b. SWITCHGEAR. - As indicated in Figure 8-1 line voltage is initially applied to the Switchgear assembly. The Switchgear then controls all incoming

(Continued on Page 184)

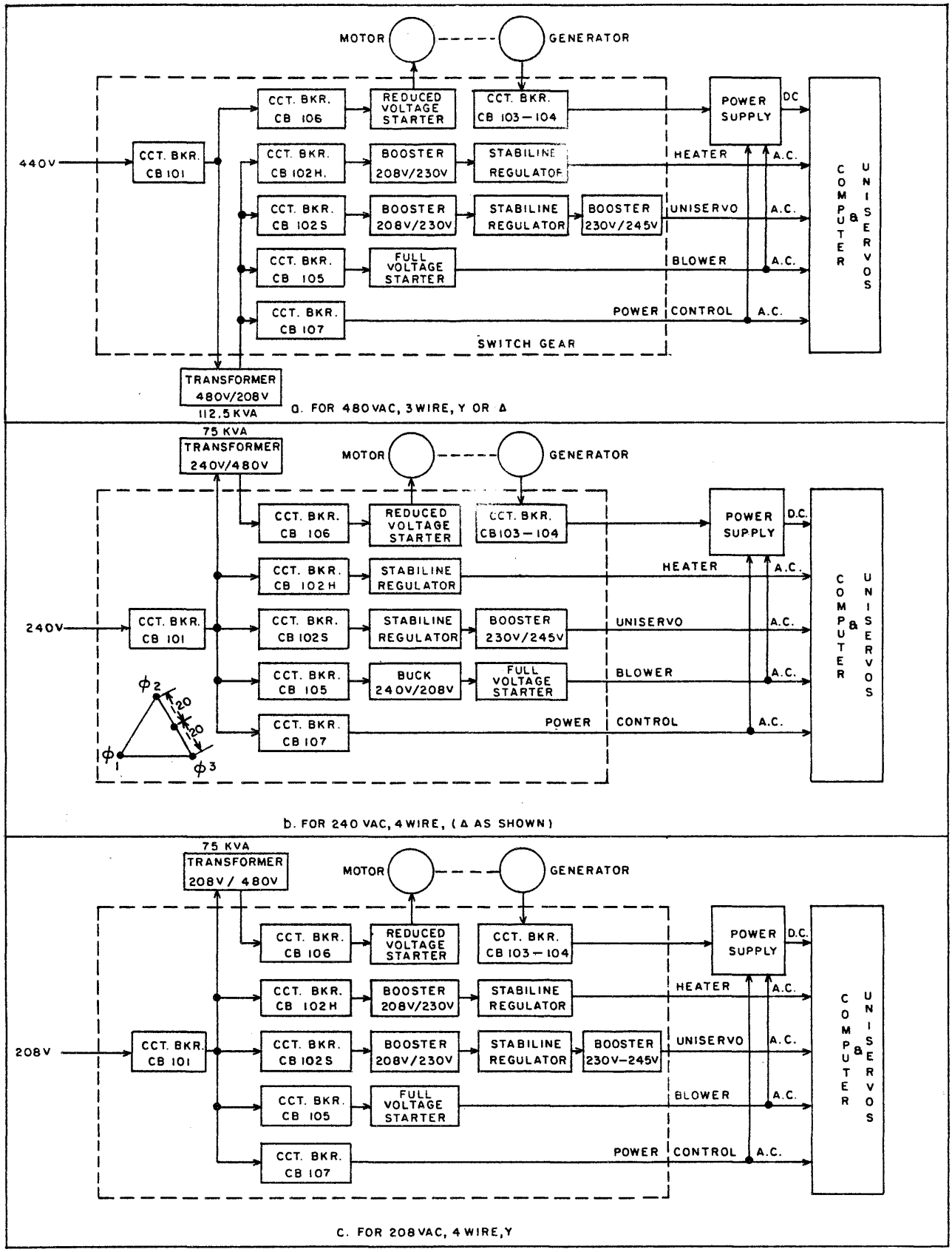


Figure 8-1. Power Distribution From Various Sources

PX 697A

(Continued from Page 182)
power to the Univac System and distributes this power between the Main Transformer, Motor-generator, Power Supply, Uniservos, Central Computer, Waterflow Detector, Three-way Valve, Indicating Lights, and Supervisory Control.

(1) PHYSICAL DESCRIPTION. - The Switchgear cabinet is 5'10 1/4" high, 6' 1/2" wide and 2'6" deep. Weight is approximately 3250 pounds. Figure 8-2 shows the physical position of components within the Switchgear.

NOTE

A complete description of the technical operation of the Switchgear will necessarily involve the equipment that it serves. For this reason the material that follows will mention, and occasionally describe in detail, various units and components beyond the physical limits of the Switchgear assembly.

(2) PRIMARY AC CIRCUITS. - The Main AC Circuit Breaker CB101 may be either electrically- or manually-operated.. Inasmuch as there is a possibility of six different operating types being installed, depending upon whether Manual or Electrical operation is used, and input voltage requirements, reference should be made to the particular drawing for specifications of the unit installed at any particular site.

With the closing of CB101, primary a-c power is directed to the Main Transformer and other Switchgear circuit breaker units in a manner depending upon input voltages used. In any event, the Main Transformer will be provided with a voltage source to the primary, with the other circuit breakers receiving primary power either from the Main Transformer or also from CB101 depending upon source voltages.

The following components will receive primary power when CB101 is closed:

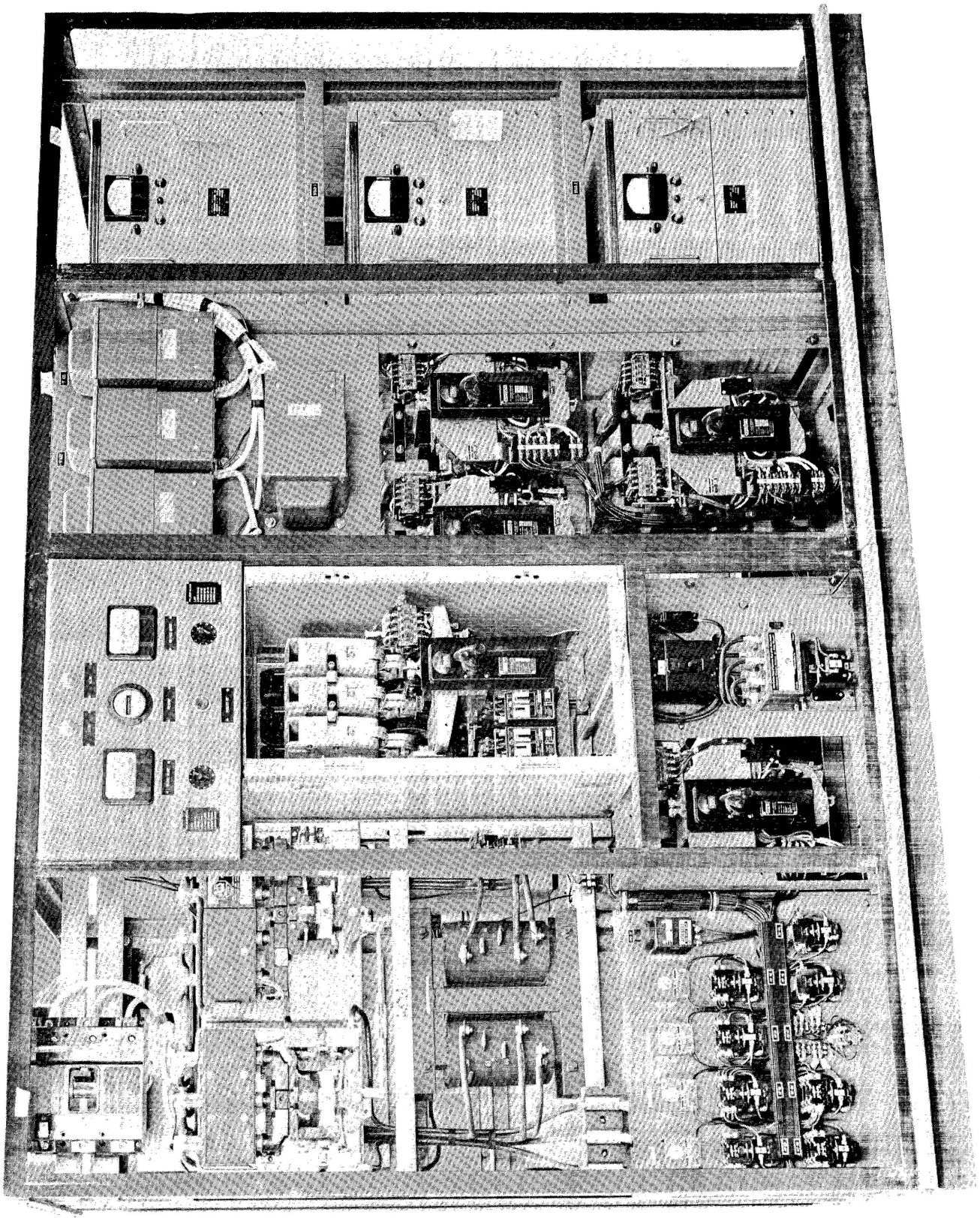


Figure 8-2. Switchgear, Front View (Cover Removed)

1. Circuit breaker CB101 auxiliary contacts are closed, providing a waiting current path for contacts of Emergency Off switch S103.

2. Circuit completed to servo circuit breaker CB102S.

3. Circuit completed to Heater circuit breaker CB102H.

4. Circuit completed to Motor-alternator circuit breaker CB106.

5. Circuit completed to No. 1 Transfer switch S101 and primary AC Voltmeter M101.

6. Circuit completed to 15 hp Motor Starter circuit breaker.

A description of the functional operation of the above-mentioned components now follows in the order listed. Internal operation of the units, where this applies, will be described under "Sequence of Operation".

(a) EMERGENCY OFF SWITCHES AND INDICATORS. - The EMERGENCY OFF switch at the Power Supply Control Panel is also duplicated in parallel at Supervisory Control. The full routing of the control lines for this switch is shown in Figure 8-3. Should an emergency arise whereby all primary power must immediately be removed from all equipment, the closing of this switch completes a direct circuit through a shunt winding of the Main circuit breaker CB101, thus causing the circuit breaker to trip. The EMERGENCY OFF indicating lamps, which are located at the Power Supply on the Control Panel, and at KL Corner control panel, apprise that power is available for the purpose of operating the EMERGENCY OFF switch functions, should this be required.

The Emergency-off controls, i.e., the contacts in CB101 and the switch in the Switchgear and the switch in the Power Supply, are equipped with sets of parallel contacts. This ensures a connection should the control be operated.

(b) SERVO AC CIRCUIT BREAKER CB102S. - Depending upon input requirements, a-c power for Uniservos may or may not require two Servo Boosters. An input of 480 a-c Wye or Delta requires a booster following the 480/208

(Continued on Page 188)

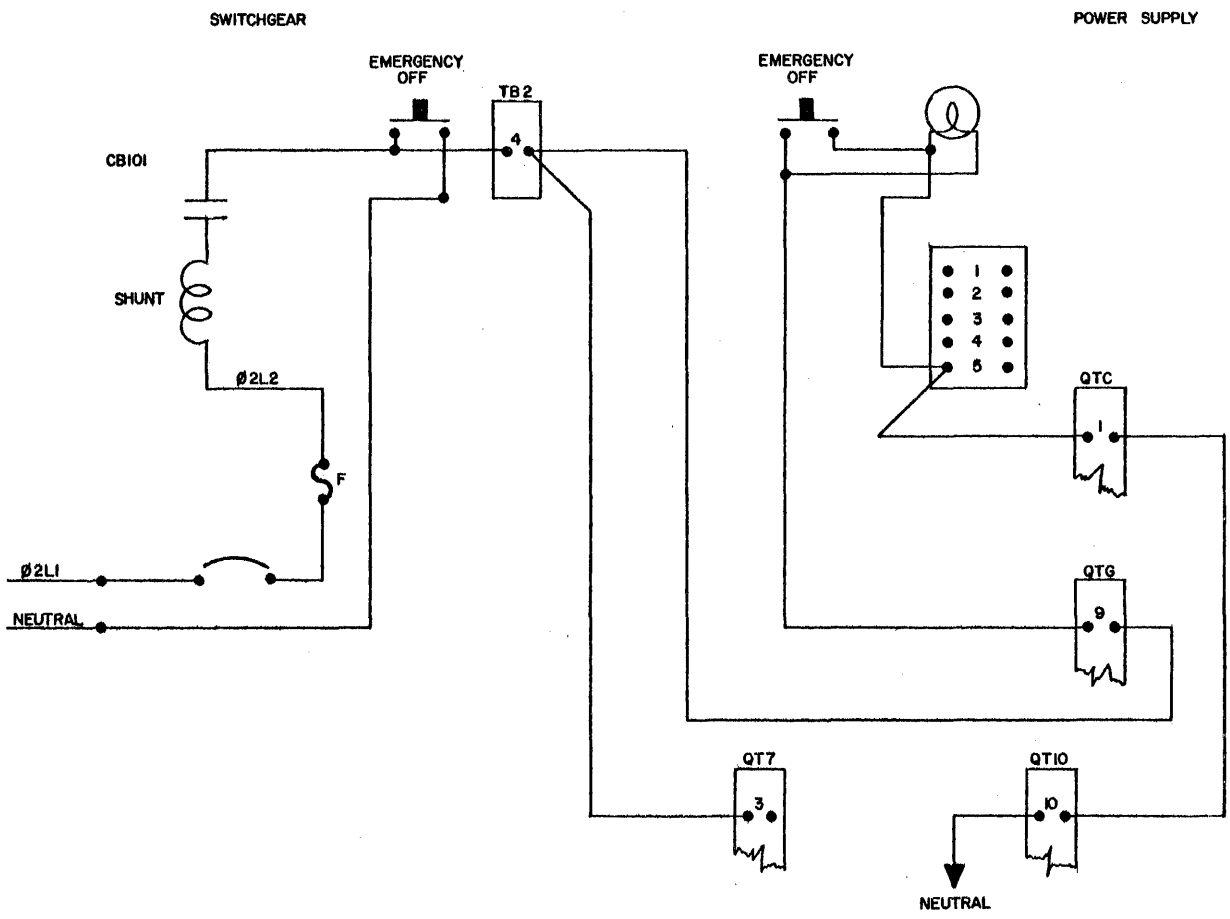


Figure 8-3. Emergency-off Switch and Indicator Circuit

(Continued from Page 186)
transformer, and again following the Stabiline Voltage Regulator whereas primary transformer inputs of 240 Delta do not. A 208 Wye input requires an additional booster. The circuit following CB102S performs the same function of routing power to the Uniservos regardless as to whether or not it is boosted.

(c) HEATER AC CIRCUIT BREAKER CB102H CIRCUITS. - As in the case of the Uniservo a-c supply, certain inputs require voltage boosters and others do not. A 480-volt a-c input requires a booster preceding the Stabiline regulator, as does a direct input of 208 volts.

Heater voltage for the Univac II System is derived from the Main Transformer in the case of the 480-volt system and directly from source voltage via CB101 in the case of 208 volt or 230 volt systems. The Heater Circuit Breaker (CB102H) then supplies the heater voltage to two 10% booster transformers (208v, 480v) or directly to the Stabiline equipment (230v). The output of the Stabiline equipment is applied to a delay network in the Central Computer. From the delay network the Heater power is applied to the primaries of the Heater Transformers via various fuse boards and barrier strips. The secondaries of the Heater transformers are connected to the various chassis and bays by fuse boards and barrier strips. This discussion will consider the Switchgear components of this system. Drawing 186616 indicates the Schematic representation of the Heater circuits within the Switchgear. Figure 8-4 and 8-5 (Heater AC CB102H Circuit) presents these circuits and the connections within this unit. The theory of operation of the different types of circuit breakers is given under "Sequence of Operation - Switchgear".

From CB102H, the Heater circuit breaker, Ø2L2 and Ø3L2 are connected to the booster transformers. The Ø1L4 line is also connected, but passes through to PV16F and PT16F in the Central Computer. The output of the two

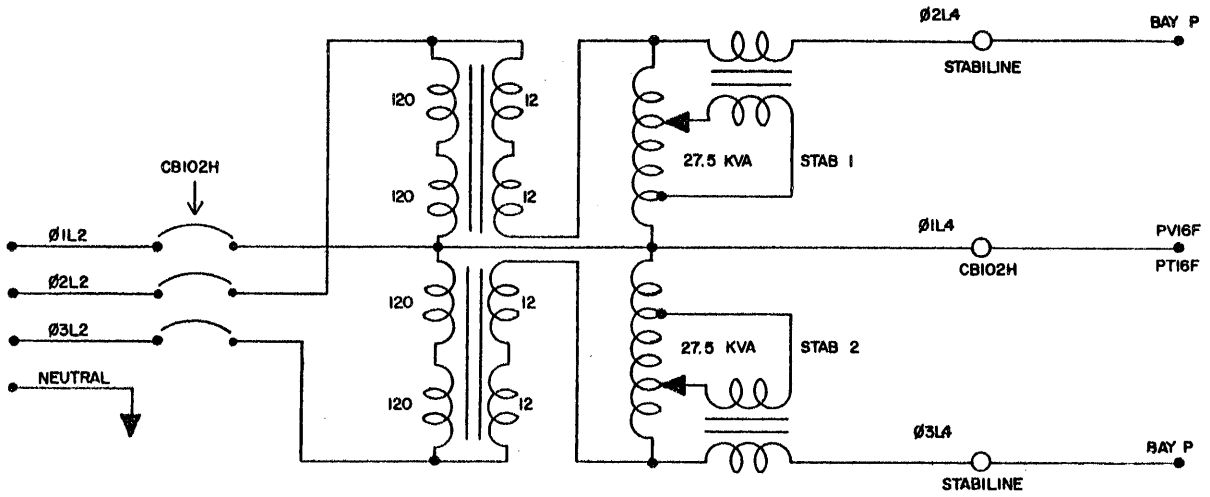


Figure 8-4. Heater AC CB102H Circuit (208V and 480V)

booster transformers is applied to the Stabiline units and is approximately 230 volts. The individual theory of operation of the Stabilines is described in a later paragraph. Output phases 2L4 and 3L4 are routed to the Modified Tray Assembly in the Central Computer. Phase 1L4 is routed directly to the Fuse Boards PV16 and PT16 in the Central Computer.

(d) MOTOR CIRCUIT BREAKER CB106. - The Motor Circuit Breaker CB106 provides line protection for the 75 hp Motor Starter assembly and motor only (thermal overloads are also provided on the Secondary of the Motor Starter as additional motor protection). The breaker is a 150-ampere unit, three-pole 600 volts, mounted on a 225-ampere "J" frame. As the Motor-Starter unit of the Switchgear will be discussed as a separate assembly further information will be omitted at this point.

(e) NO. 1 TRANSFER SWITCH S101 AND AC VOLTMETER M101. - With the supplying of a-c from CB101 on Ø1L2, Ø2L2 and Ø3L2, power is also applied to a 60-cycle AC voltmeter, M101, and Transfer Switch, S101. The voltmeter, which is a 0-300 volts range, 60-cycle unit, rated at 2% accuracy, measures the voltages given in the following list as they are received from the secondary side of CB101. The Transfer Switch, S101, is a ceramic rotary type

(Continued on Page 191)

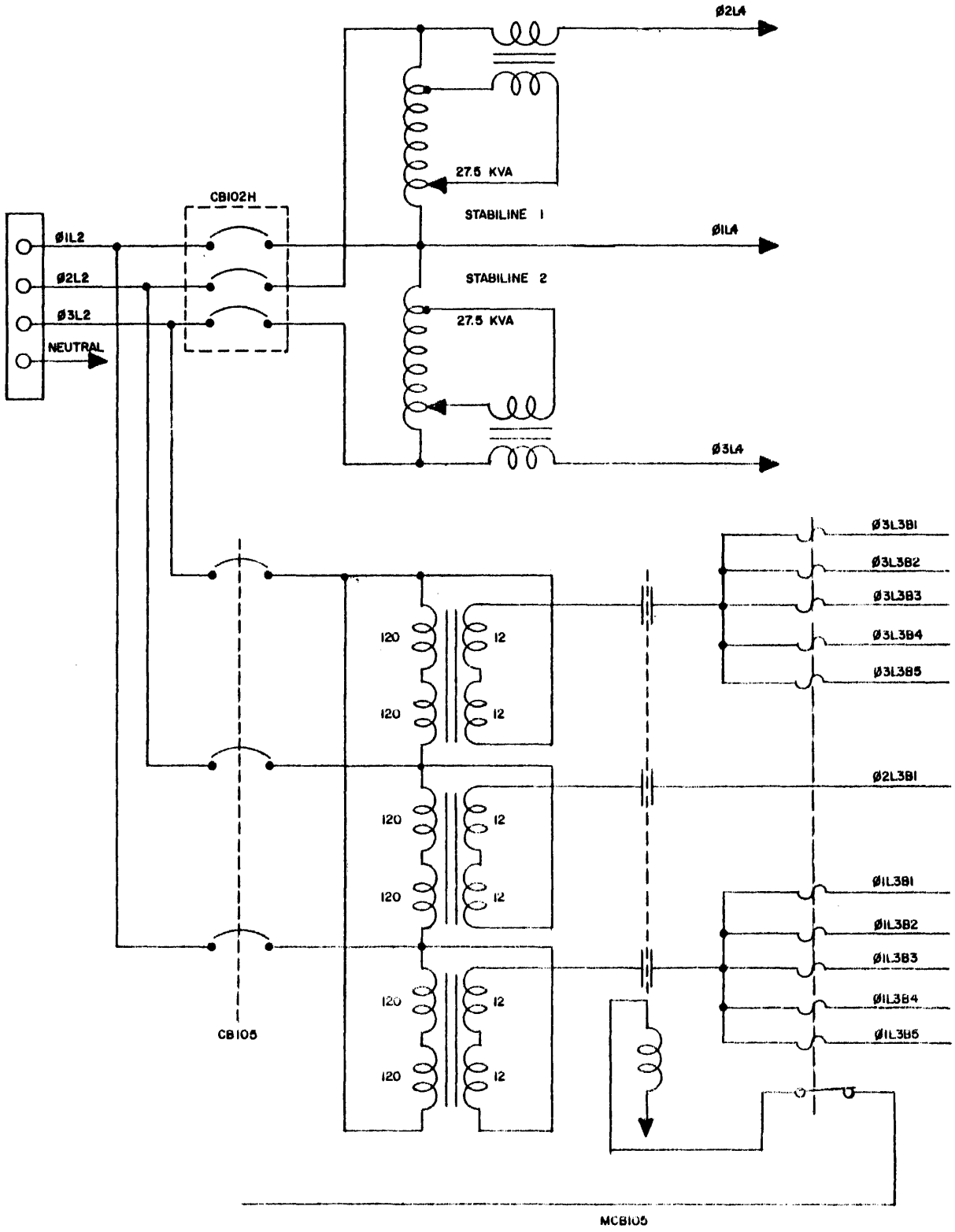


Figure 8-5. Heater AC CB102H Circuit (240V)

(Continued from Page 189)
two-pole, twelve-position switch rated at 300 volts, 10 amperes. The positions indicated below are the positions this switch assumes to read the indicated power lines.

Position 1: Off

2: Phase 1-2

3: Phase 1-3

4: Phase 2-3

5: Phase 1 - Neutral

6: Phase 2 - Neutral

7: Phase 3 - Neutral

8: Phase 3L5 - Phase 2L5

Each line being read is fused to the switch by 3AGC 1 ampere fuses, designated F101, F102, F103 and F110 (the latter being Ø3L5 fuse). The circuitry of the AC voltmeter and the transfer switch is shown in Figure 8-6 (AC Voltmeter and Switching Circuit).

(f) HP MOTOR STARTER CIRCUIT BREAKER CB105. - CB105, the 15 hp Motor Starter Breaker operates directly from Ø1L2, Ø2L2 and Ø3L2. This assembly, a three-pole 40-ampere 240 volt a-c unit mounted on a 100-ampere "E" frame, provides protection in the primary circuit for current drawn by blower equipment in the Power Supply and Central Computer. Thermal overload elements provide individual protection for the blower motors. Overload detection by any element will de-energize the coil of MCB105, thus opening the circuit for all of the blowers. The circuit breaker lines with the lines served by each are given below:

Phase 3 Line 2 - Phase 3 Line 3 B1

Phase 3 Line 3 B2

Phase 3 Line 3 B3

Phaee 3 Line 3 B4

Phase 3 Line 3 B5

(Continued on Page 193)

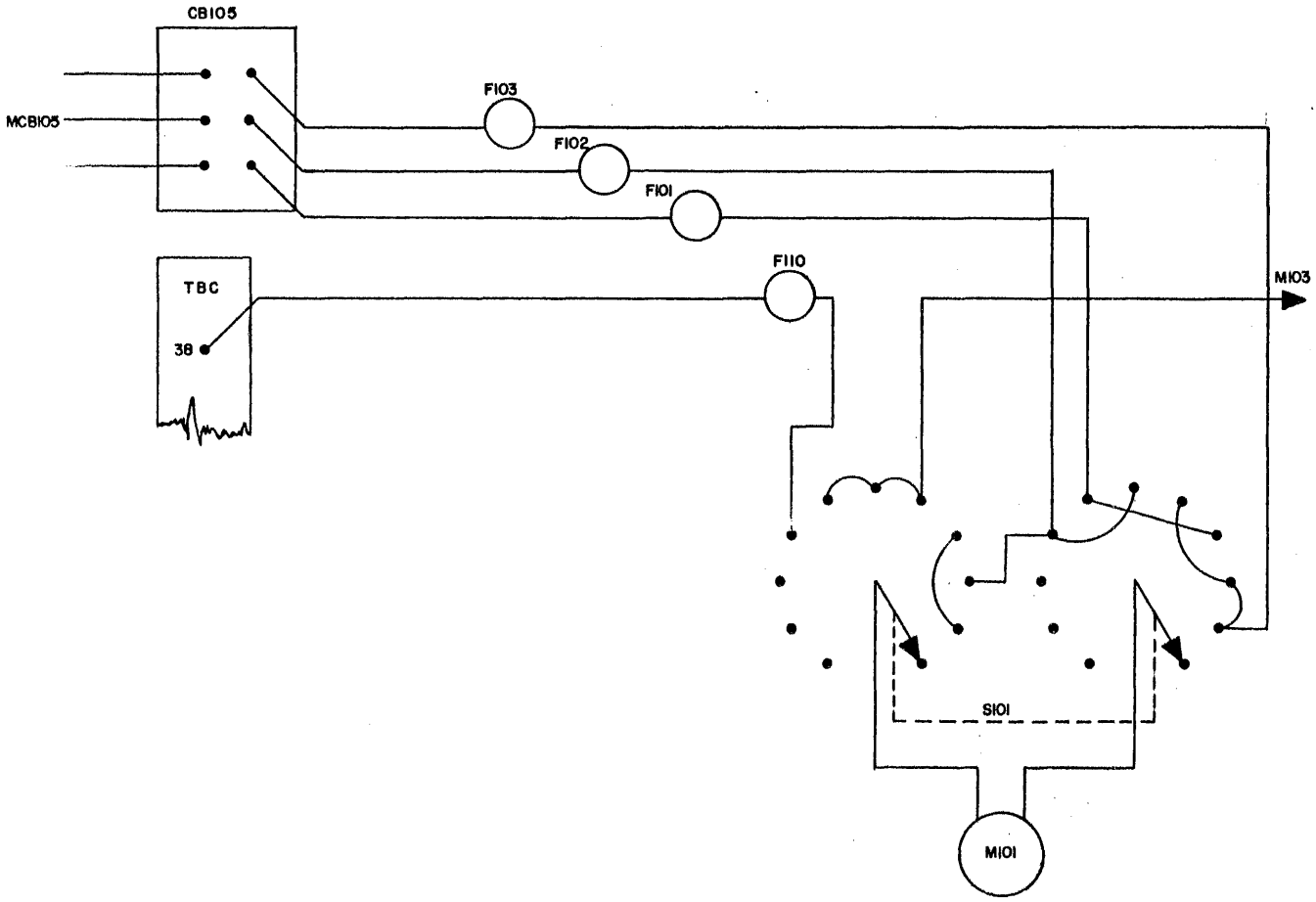


Figure 8-6. AC Voltmeter and Switching Circuit

(Continued from Page 191)

Phase 2 Line 2 - Phase 2 Line 3 B

Phase 1 Line 2 - Phase 1 Line 3 B1

Phase 1 Line 3 B2

Phase 1 Line 3 B3

Phase 1 Line 3 B4

Phase 1 Line 3 B5

(g) NO. 2 TRANSFER SWITCH 400 CYCLE AC VOLTMETER. - AC Voltmeter M102 and Transfer Switch S102 provide for the monitoring of alternator output voltages in a similar manner to that provided by M101, the input voltage meter. Each line monitored is fused by 1 ampere fuses F104 to F109. The voltmeter is 0-300 volts scale, 400 cycles, rated at 3% accuracy; the switch is the same as S101, two-pole, twelve-position, rated at 300 volts 10 amperes. The circuit of this meter and the switching assembly is shown in Figure 8 - 7 (400 Cycle AC Voltage Metering Circuit). Voltages monitored at the various switch positions are as follows:

Position 1: Off

Position 2: Phase B2-B3

Position 3: Phase B1-B3

Position 4: Phase B1-B2

Position 5: Phase A2-A3

Position 6: Phase A1-A3

Position 7: Phase A1-A2

(h) FREQUENCY METER. - A frequency meter of the vibrating reed type indicates a frequency of 380 to 420 cycles, and normally reads about 407 cycles. It is inserted across one phase to neutral at the meter transfer switch primary side.

(Continued on Page 195)

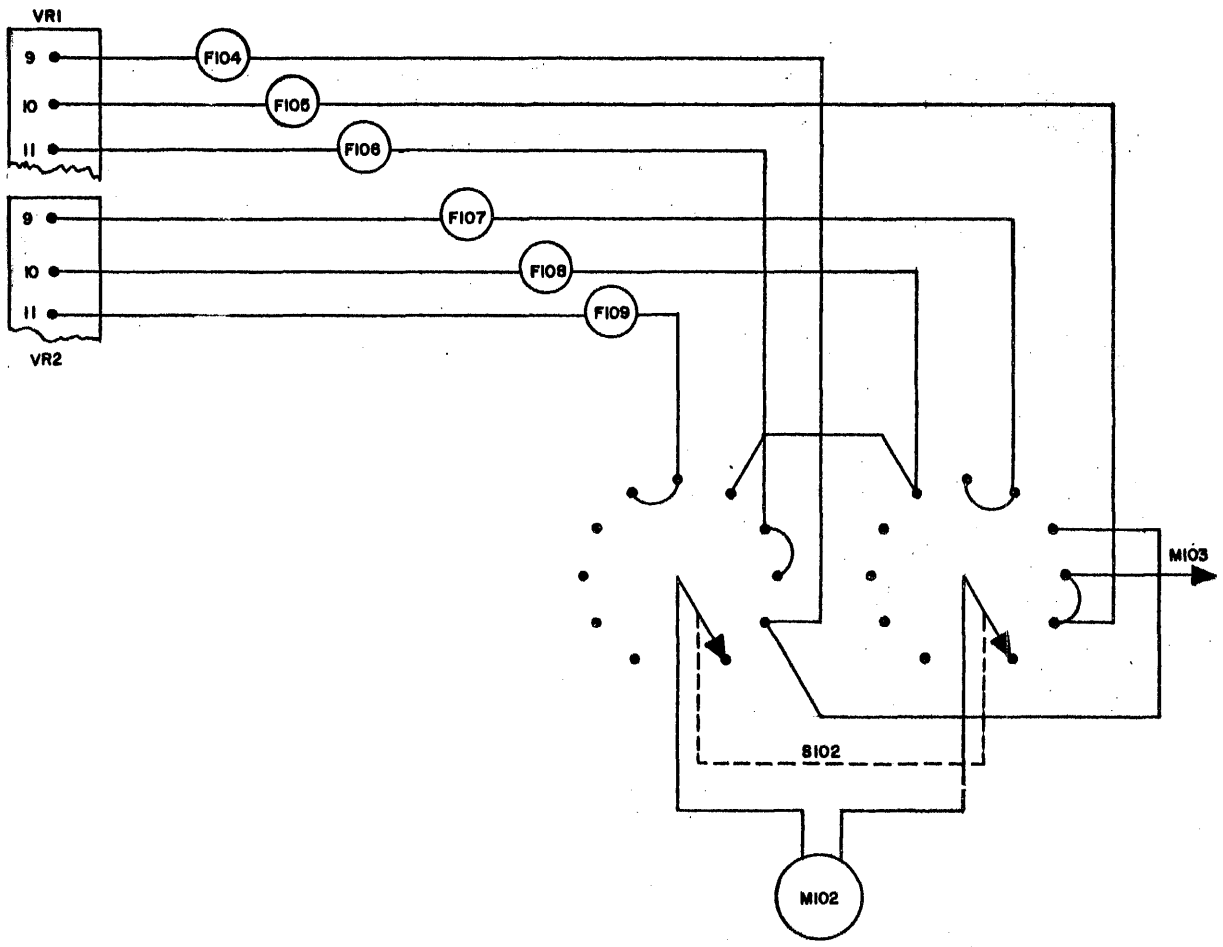


Figure 8-7. 400 Cycle AC Voltage Metering Circuit

(Continued from Page 193)

(i) ALTERNATOR OVERVOLTAGE MONITOR. - In order to protect the equipment from dangerous cumulative effects such as the failure of a magnetic amplifier sense circuit causing an overvoltage condition from the generators, an Alternator Overvoltage Monitor assembly is installed in the Switchgear, monitoring all three phases of each generator's output. The schematic representation of this assembly is shown in Figure 8-8 (Alternator Overvoltage Monitor), with complete details being given on Drawing 142682. Each monitor consists of three rectifiers, one capacitor and one three-contact relay.

Normally the rectifiers will pass a certain limited current when the voltage output from the generators is normal. This current, which is additive from each phase, is adjusted at R03 (and R06) to the point where relay RP41 (and RP42 for Alternator B) will not be sufficiently energized to close. Resistors R01, R02 and capacitor C01 (and R04, R05, C02) act as a filter network to the 400 cycle output of the alternators. With an increase of voltage from the generator beyond tolerable limits, current through the relay will increase to the point where the relay armature closes the contacts.

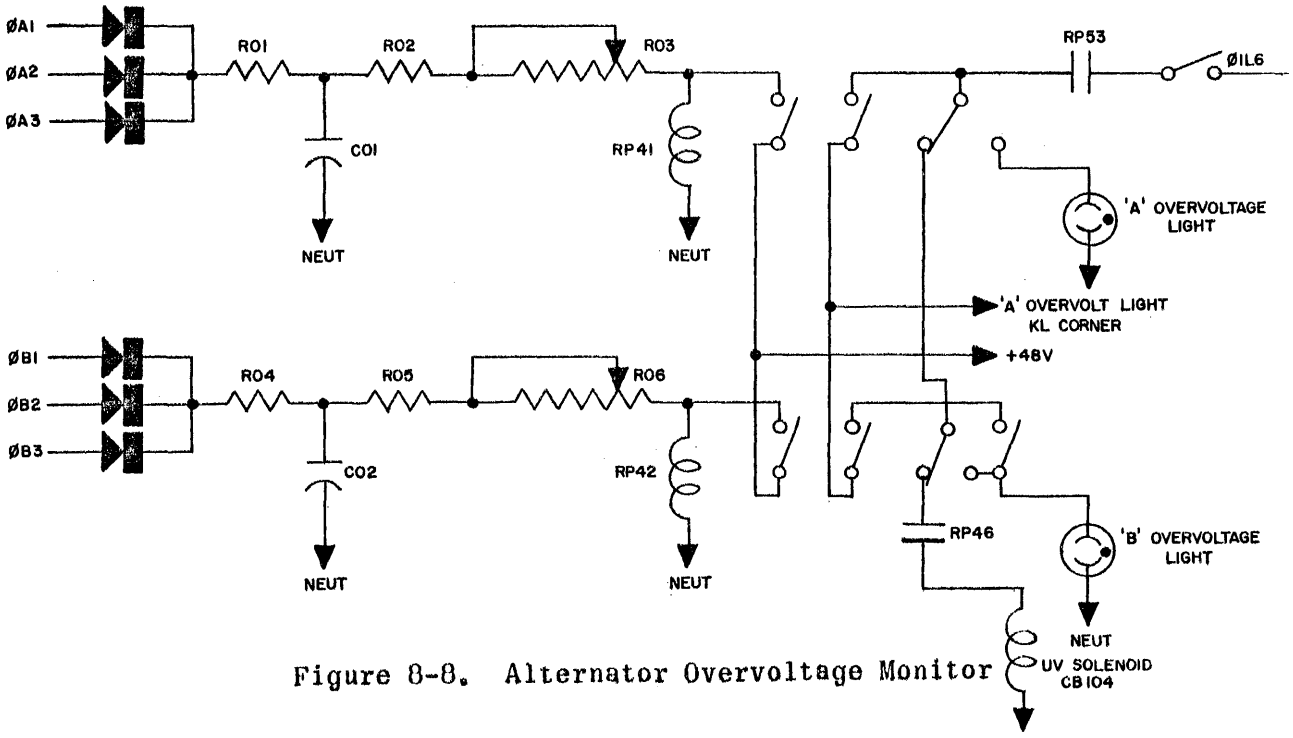


Figure 8-8. Alternator Overvoltage Monitor

As one set of the contac[illegible]lose, 48 volts d-c is applied via the Monitor Reset button in KL corner to the solenoid of the relay which has initiated the action, thus self-energizing the relay. One of the other closing contacts completes a 110 vac circuit from ØlL6 through the machine overheat contacts and RP53 (in KL corner) to the Overvoltage indicator. Which indicator lights depends upon whether RP41 or RP42 closed. If the A generator, the "A" lamp will light, if the B generator, the "B" lamp will light. Another relay contact duplicates the foregoing, but lights an indicator (overvoltage) at KL corner of the Central Computer. The final relay contact opens a normally - closed circuit which breaks the ØlL6 110 vac line through the closed contacts of RP46 to the Undervoltage solenoid of CB104 (DC breaker No. 2). The de-energization of the Undervoltage solenoid results in the opening of this breaker. Consequently, the alternator output voltage is removed from the Power Supply input, as the release of CB104 causes the release of CB103 (through No. 2 contacts of CB103, CB104, RP30 contacts, and CB103 No. 1 contacts to CB103 shunt solenoid). In this manner, <u>all</u> alternator output voltages are removed from the Power Supply and other equipment.

(j) MAGNETIC AMPLIFIER REGULATOR. - Each generator used in the Univac installation utilizes a magnetic amplifier type generator exciter regulator. A separate unit for each generator, designated "A" and "B" unit, is located in the Switchgear cabinet. Excitation voltage to the Magnetic regulator is obtained from the load side of CB104 and CB103 and is three-phase 208 volts at 400 cycles when operating at rated output. An additional 440-volt 60 cycle source from the motor starter is utilized for initial excitation.

A theoretical circuit of one of the magnetic amplifier regulators is shown in Figure 8-9 (Magnetic Amplifier Regulator). The complete schematic drawing and wiring diagram are on Dwg. 142618. (Continued on Page 198)

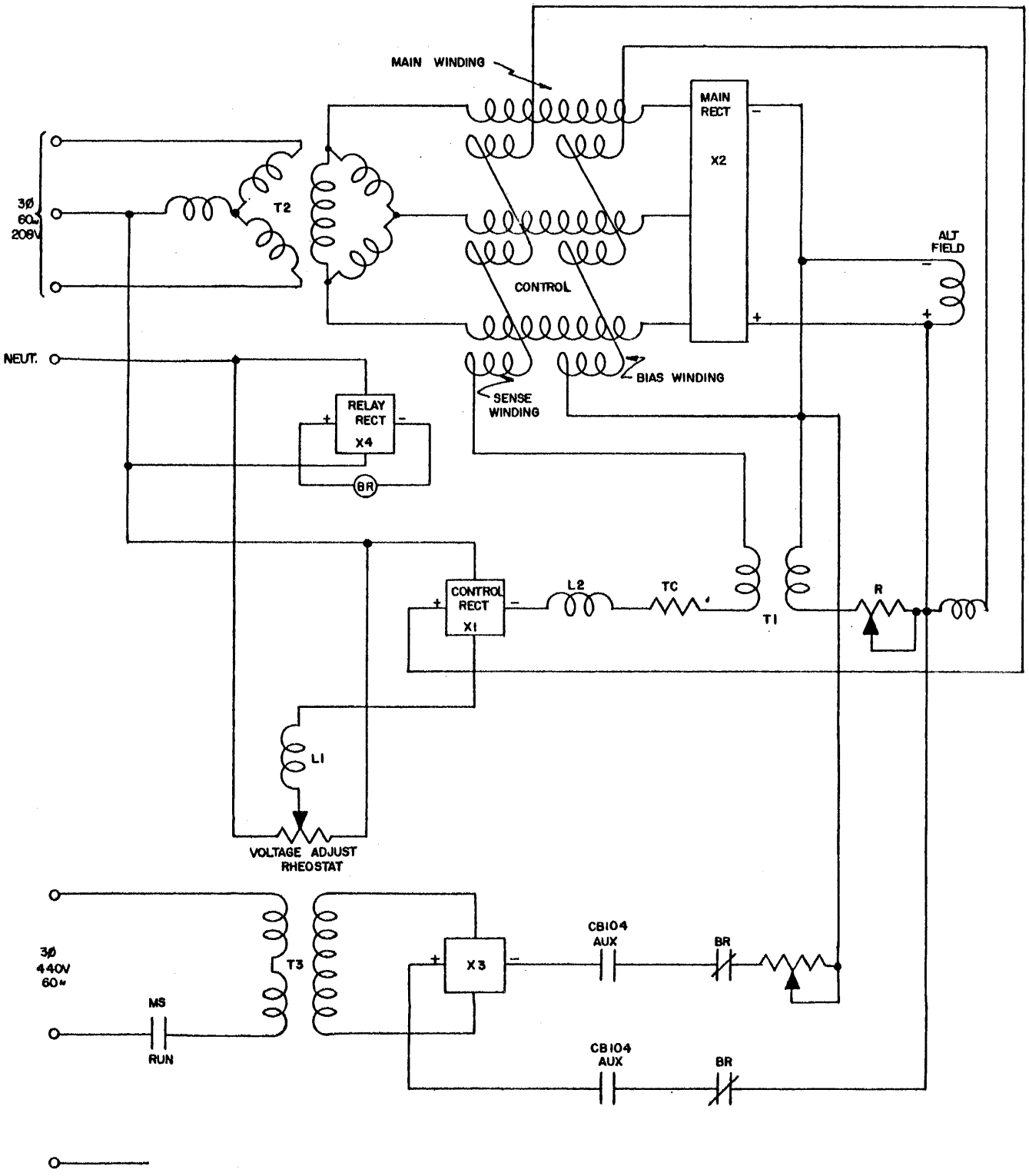


Figure 8-9. Magnetic Amplifier Regulator

(Continued from Page 196)

The saturable core reactors in Figure 8-9 which are in series with the main rectifier X2, form the excitation system. The impedance of the main windings of the reactors to the flow of alternating current to the main rectifier is controlled by the d-c control windings, indicated as "sense" and "bias" windings.

The impedance of L1, the reference reactor, changes sharply when the approximate or exactly rated voltage is across the primary of T2. T2 is a step-down transformer designed to reduce the voltage to the rectifiers to more nearly approximate the required excitation voltage.

An increase in voltage at the primary of T2 above a value previously selected through the Voltage Adjusting Rheostat will cause L1 to saturate, permitting the current flow to Control Rectifier X1 to increase sharply. The Control Rectifier output through choke L2 and the magnetic amplifier sense windings, also increases sharply, increasing the impedance of the main winding, thus decreasing the rectifier output.

In series with the sense windings is a Temperature Compensating resistance. This resistance is physically located above transformer T2. This location was selected as being an optimum position to register temperature increase. As the temperature increases from an initial value, this resistance effectively compensates for any lessened current reaching the alternator field through the effect it has on the amplifier reactances.

The sense winding of the magnetic amplifier reactor is wound in such a manner that a current increase from the Control Rectifier will increase the impedance of the reactor; thus lowering the output current of the main rectifier to the alternator field. The converse is, of course, also true. The results will be either a decrease or increase in the voltage output of the alternator.

Transformer T1 produces a secondary voltage which is applied to the reactors through a "bias" winding. The resultant effect of this current through the windings is relative to that produced by the sense windings. Resistance R, in series with the bias winding is used to adjust the bias voltage to a pre-selected value. Other resistances shown on Dwg. 142618 are also for initial adjustment by the manufacturer, with the exception of the voltage adjusting rheostat.

Until such time as a sufficient 400-cycle output is available from the generator to produce a suitable field current for the generator through the magnetic amplifier regulator, sufficient 60-cycle current is supplied to the field from the T3 - X3 supply. This power supply utilizes a single phase transformer with the primary connected between two phases of the three-phase 440 volt 60 cycle line. This power supply, which reduces the 440 volts a-c to approximately 20 volts d-c, in addition to providing field excitation, supplies voltage for the bias winding of the magnetic amplifier during the time the current is increasing through the reactors. The primary connection is completed through the RUN contact of the Motor Starter.

In order that the foregoing source of field current may be eliminated when sufficient excitation is available from the magnetic amplifier, the output passes via two auxiliary contacts on CB104 and two contacts on relay BR, (part of Magnetic Amplifier assembly). The contacts on CB104 continue to provide d-c excitation to the alternator field momentarily after CB104 closes and prior to the full 400-cycle source being available. As the 400-cycle voltage builds up, it reaches a point where the d-c output of rectifier X4 is sufficient to energize relay BR. As this occurs, the contacts of BR open, permitting the excitation source from X2 to supply the field.

(k) DC CIRCUIT BREAKERS CB103 - CB104. - Circuit breakers CB103 and CB104 provide for interruption of the 400-cycle voltage being supplied to the DC power supplies from the alternators.

As will be explained in greater detail later, CB104 closes after CB103 is closed during the initial turn on of the equipment. Both units are electrically-operated breakers with dead-front switchboard mounting.

(3) SEQUENCE OF OPERATION. - As part of a discussion of other large components within the Switchgear, a description of the sequence of operation is necessary. Considering that the equipment is being initially turned on, this sequence will be given with the components involved being described, if not done elsewhere in the Manual.

With the Main AC Circuit Breaker CB101 closed, the CONTROL POWER ON indicator lamp at the Power Supply Control Panel will light. Assume, at this point, that CB107, CB106, CB105, and the Control Power breaker (at the Power Supply control panel) are closed. In this case RP48 is energized, the circuit is shown in Figure 8-10 (RP48-RP53 Relay Circuit). The energizing of RP48 is dependent upon the waterflow indicator switch being closed (water is flowing) and upon RP53 being energized - RP53 is energized when the CB107 and the CONTROL POWER switch is in the ON position, and upon the Bay Overheat and Power Supply 110^{0} thermostats being closed - this condition will not exist if the ambient temperature exceeds the limit for which the thermostats are rated.

With the closing of RP48, the current path through the shunt-trip winding of CB102H will be broken by the contacts of RP48. The winding is available

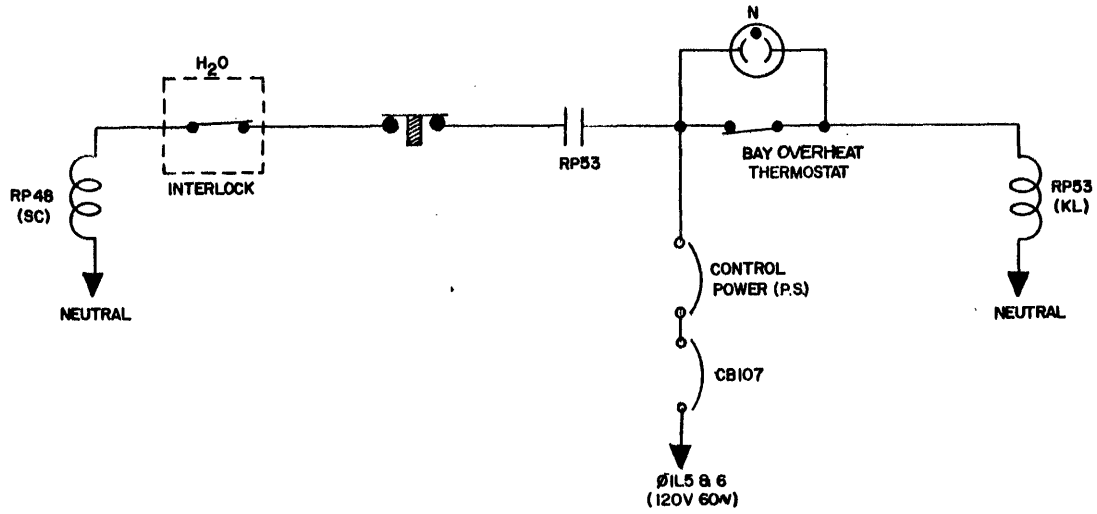


Figure 8-10. RP48-RP53 Solenoid Energizing Circuit

to permit the circuit breaker to be tripped if any of the conditions which follow are not present:

1. RP48 energized
2. Waterflow detector switch is closed
3. AC OFF switch not depressed
4. RP53 energized
5. Bay overheat switches closed
6. Control power circuit breaker switch closed

(a) OPERATION OF CIRCUIT BREAKERS. - For subsequent actions to be fully understood, the operation of the I-T-E Type KA, and General Electric Type AK-1-15-3 circuit breakers are briefly discussed at this point. The Type KA breaker is used for CB102H, CB102S, CB103 and CB104 in some Switchgear installations, while others use the General Electric equipment described later.

Although the breaker involved in the present sequence of operation is CB102H, the theory described will apply generally when the other breakers are mentioned, the differences being only in the quantity of contacts utilized and the function of these contacts. Physically, certain differences exist in ratings. Maintenance data for the breakers will follow the general discussion.

Figure 8-11. (I-T-E Type KA Breaker, Typical Wiring) shows a schematic representation of the Type KA I-T-E circuit breaker, and Figure 8-12 (Type KA Schematic diagram) presents a shorthand diagram of its connections. Drawing 186616 shows a typical installation of a GE AK-1-15-3 breaker in any of the circuit breakers positions shown in this drawing. Terminal connections to power lines and other equipment is indicated on the mechanical drawing pertaining to the installation.

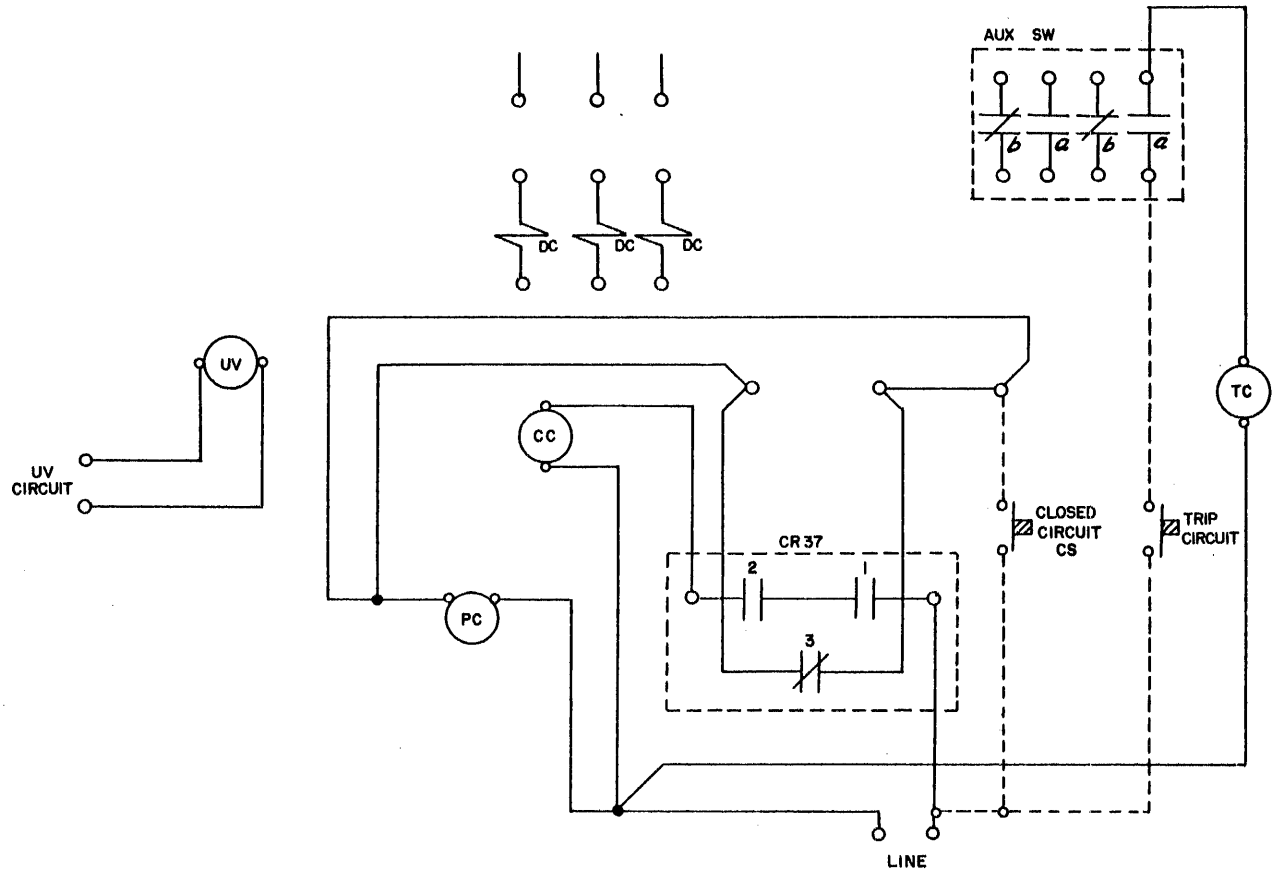


Figure 8-11. I-T-E Type KA Breaker, Typical Wiring

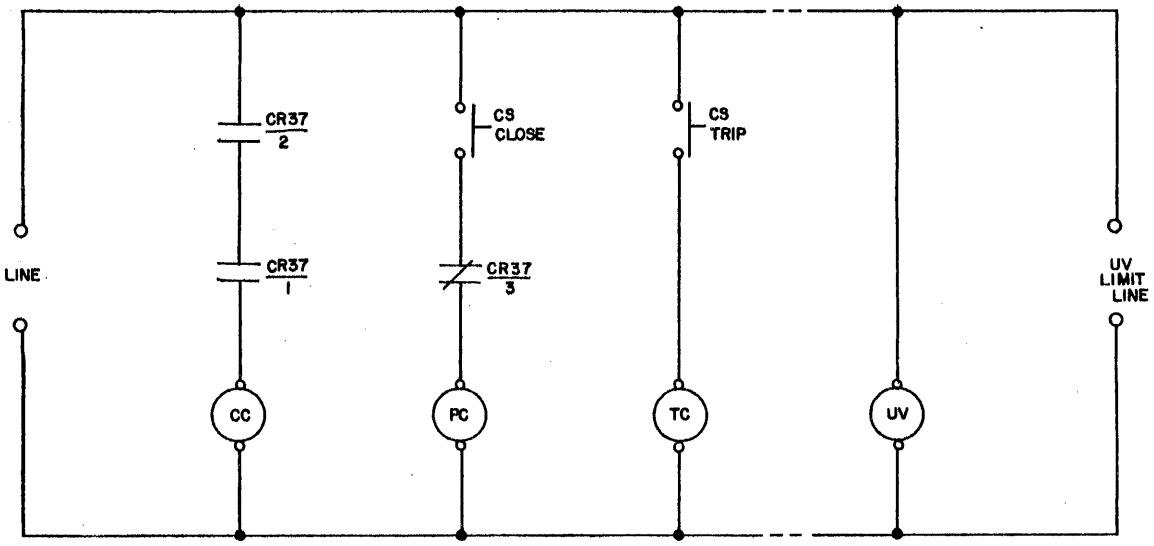


Figure 8-12. I-T-E Type KA Schematic Diagram

1 DESCRIPTION. - For electrically-operated KA breakers, a solenoid assembly is suspended under the mounting shelf below the operating mechanism and is removable as a unit, should this be required. Four springs between the solenoid magnet and the shelf absorb the shock of the plunger at the end of the closing stroke.

A Type R-37 control relay controls the current source of the solenoid closing coil, and is a single-pole double-break relay. The Type KA breaker is mechanically and electrically trip-free, which means that the breaker may be tripped at any point of the closing stroke by the operation of a tripping device. As soon as the contacts touch under fault conditions, the trip device operates the tripping mechanism, releases the tripping toggle, and permits the opening springs to return the contacts to the fully open position.

2 OPERATION. - Refer to the schematic circuit diagram shown in Figure 8-12. The closing of Control Switch CS (AC ON at the Power Supply Control Panel for Univac II) energizes pickup coil PC, attracting the relay armature and closing the main relay contacts CR37/1 and CR37/2. The closing of the main relay contacts energizes the solenoid closing coil CC and the plunger moves towards the closed position. At the end of the plunger travel, a trip lever attached to the plunger strikes the latch bar in the relay. As the latch bar rotates, it releases the latch lever permitting the lever to slide backwards under tension of the contact arm spring. In moving backward as far as the slot will permit, the latch lever rotates the contact lever about a fixed pin to mechanically open contacts CR37/1 and CR37/2. This de-energizes the solenoid closing coil, allowing the solenoid plunger to return to normal position. This action completes the closing cycle.

The circuit breaker will not attempt to reclose if a fault was present on the initial try and the closing switch is maintained in a closed position. This is because the relay armature remains attracted to the magnet of the pickup coil preventing the latch bar from resetting. Thus a second attempt cannot be made until the control switch is released. This will de-energize the pickup coil and allow the latch bar to reset. This action prevents continual re-cycling of the circuit breaker, and also prevents the burn-out of the momentarily rated pickup coil, should it remain energized for any length of time.

3 UNDERVOLTAGE TRIP. - When the voltage falls below a certain established value, it is desirable that the circuit breaker operate. For this purpose an Undervoltage Trip is provided on the Type KA circuit breaker. (This may also be a method of tripping the circuit breaker by purposely removing the voltage to trip the mechanism.) The UV trip device used with the KA

breaker consists of a magnet assembly, voltage coil, armature, spring lever, spring assemblies and trip link assembly, and is shown in Figure 8-13 UV Trip Device for KA Breakers.

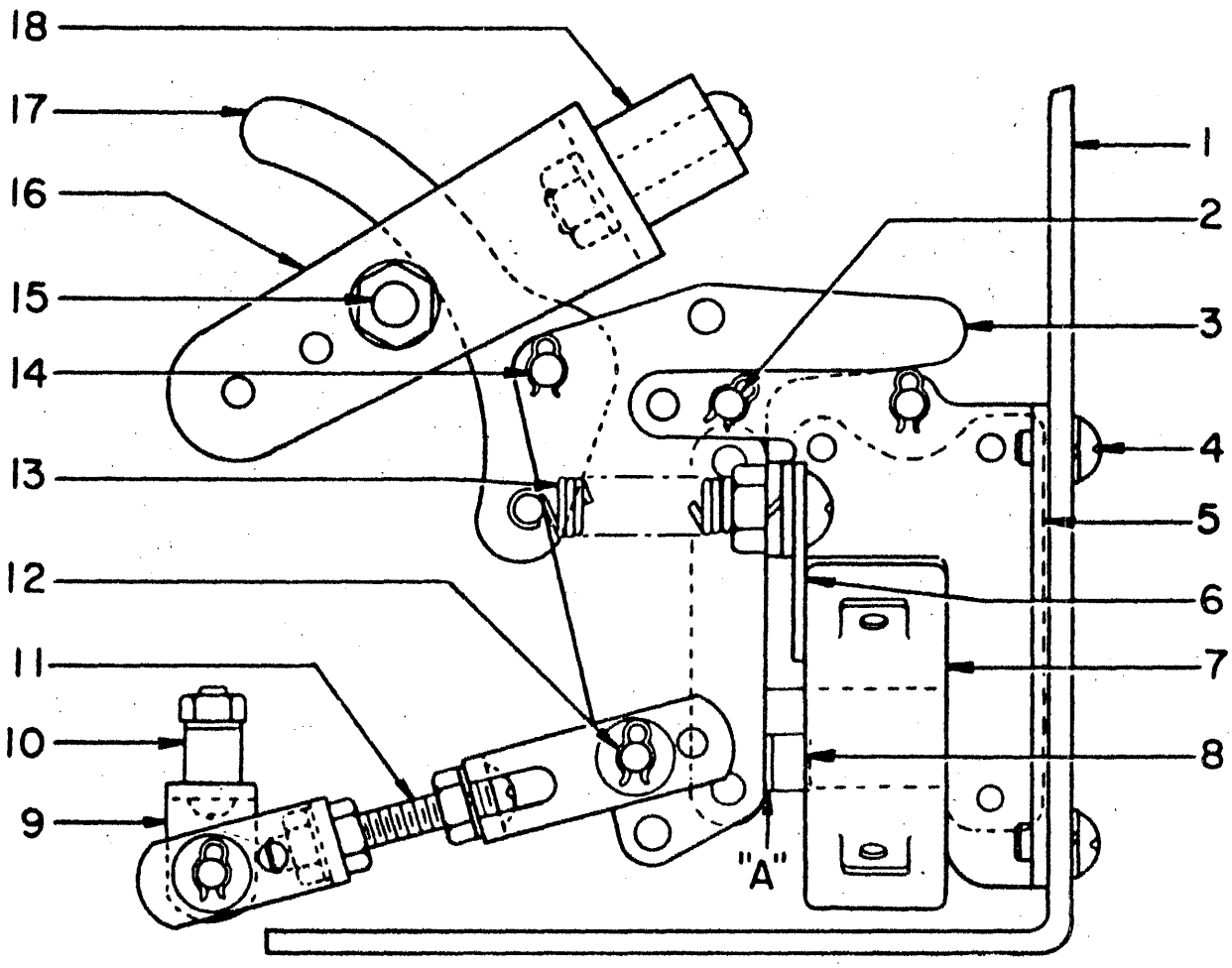
Under normal operation, the armature is held against the magnet pole face. When the operating voltage drops to approximately 30 to 60 per cent of the normal circuit voltage, the magnet will release the armature. The armature, rotating clockwise on a pivot pin, trips the circuit breaker by means of a force applied to the tripper bar through an adjustable linkage. The force is generated by two springs which have initial tension when the circuit breaker is open. Additional tension is supplied by the rotation of the spring lever as the circuit breaker is closed. The spring lever is actuated by the camming operating of an adjustable eccentric carried by a guide attached to the circuit breaker jack shaft.

4 SHUNT TRIP. - This accessory to the Type KA breaker is used for tripping the breaker remotely for any of many reasons, without regard to the existing load conditions.

The shunt trip device is shown in Figure 8-14, Shunt Trip Device and consists of a Magnet assembly, operating coil, armature, and trip link. When the circuit is energized, the tripping magnet attracts the armature, which actuates the trip link assembly. The armature and trip link assembly, during final movement, actuate the tripper bar which in turn disengages the latch to trip the circuit breaker. In order to prevent the operating coil of the shunt trip from burning out following the opening of the circuit breaker, an auxiliary contact is provided to disconnect the coil from the circuit as the circuit breaker opens.

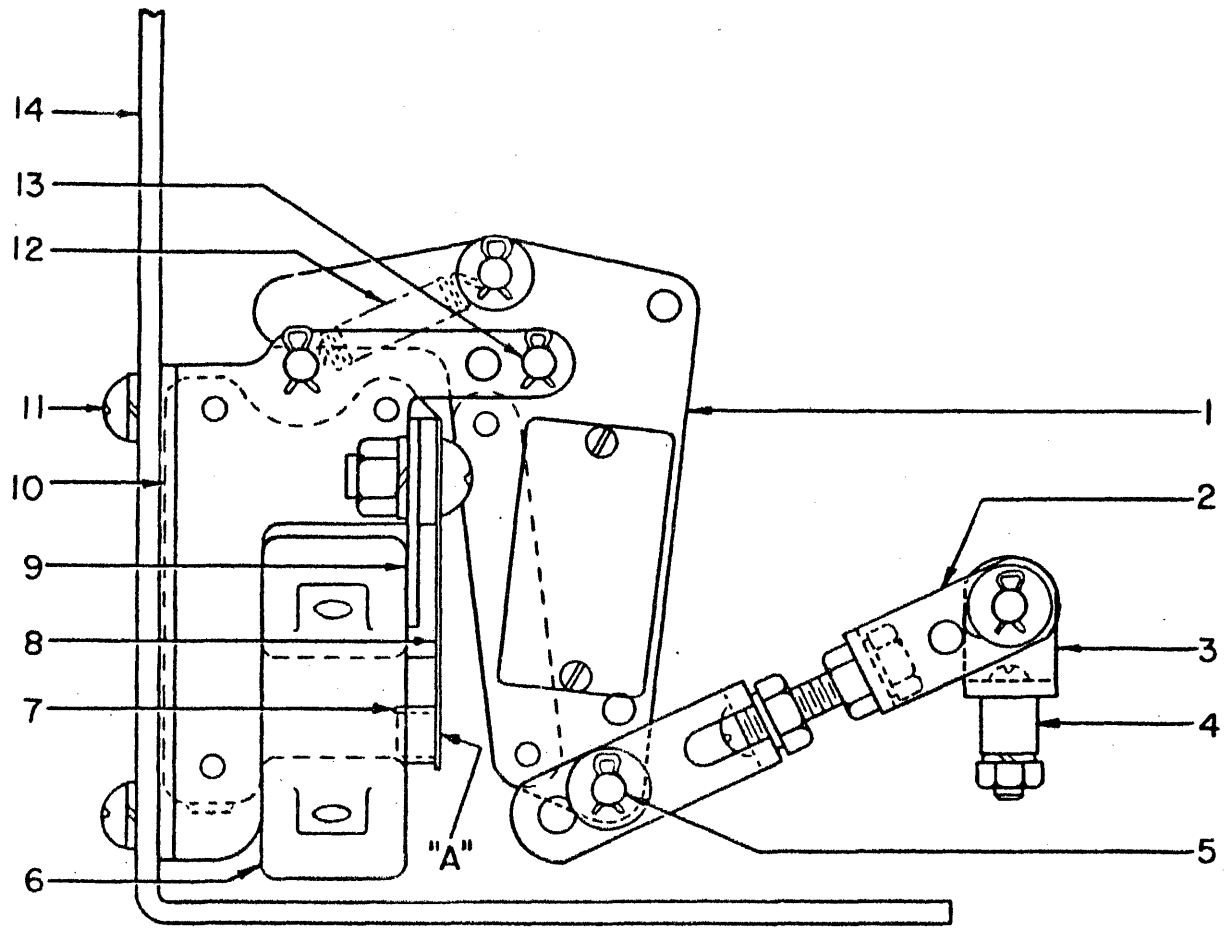
5 L2 AUXILIARY SWITCH. - The Auxiliary Switch device consists of additional contacts mounted as an assembly on the circuit breaker. The

(Continued on Page 208)



1 Shelf
2 Armature Pivot Pin
3 Armature
4 Mounting Screw
5 Magnet
6 Coil Retainer
7 Coil
8 Shading Ring
9 Tripper Bar Tripper
10 Tripper Bar
11 Trip Link
12 Link Head Pin
13 Spring
14 Spring Lever Pin
15 Eccentric Stud
16 Guide
17 Spring Lever
18 Jack Shaft

Figure 8-13. Undervoltage Trip Device for Type KA Circuit Breakers



1. Armature
2. Trip Link
3. Link
4. Tripper Bar
5. Link Head Pin
6. Coil
7. Shading Ring
8. Armature Shim
9. Coil Retainer
10. Magnet
11. Mounting Screw
12. Spring
13. Armature Pivot Pin
14. Shelf

Figure 8-14. Shunt Trip Device for Type KA Circuit Breakers

(Continued from Page 205)
contacts are closed (or opened as required) simultaneously with the closing of the Main contacts, by a Mechanical connecting link.

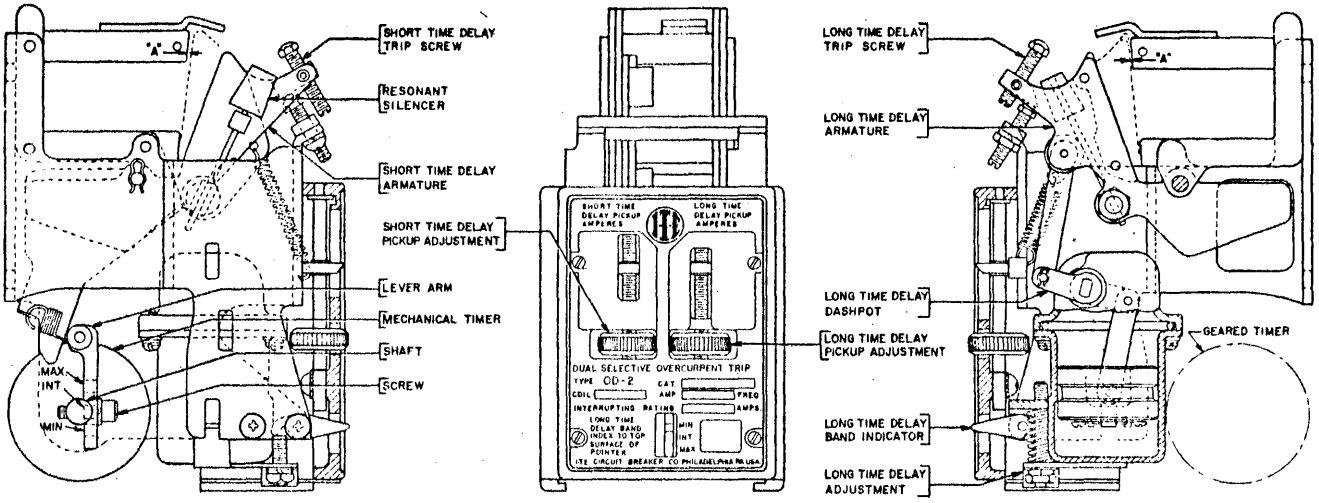
6. OVERCURRENT TRIP. - The Overcurrent Trip device used with the I-T-E Type KA circuit breaker is identified as Type OD-1 and is presented in Figure 8-15. The accessory has two basic features: an instantaneous trip element operating without manifest delay; and a long-time delay element using a fluid displacement dashpot. The latter element is factory calibrated and may be adjusted in field use for minimum pickup currents of 80 to 160 percent of the continuous current rating of the breaker. The instantaneous trip element is also factory calibrated to be adjustable in the field to minimum pickup currents of 500, 1000 and 1500 percent of the continuous-current rating of the breaker.

The action of this device hinges on the operation of the elements. In the case of the long-time delay element the armature has a fixed air-gap and a tensioning spring for current pickup calibration. The armature is connected through a linkage and crankshaft to a piston suspended in a fluid-displacement dashpot, the time delay occurring as the time required for the fluid to pass from one side of the piston to the other. The magnitude of the delay is a function of the distance that the piston moves in the restrained portion of the cylinder.

After the armature has completed not more than half of the total operating stroke, the piston enters an unrestrained portion of the cylinder. This permits the armature trip screw to strike the circuit breaker trip bar with some force. This action rotates the tripper bar, releases the mechanism latch, thus opening the circuit breaker.

A check valve allows the armature to reset rapidly (in less than one second) after either a partial or full stroke. Accordingly, in future

(Continued on Page 210)



LEFT SECTION VIEW FRONT VIEW RIGHT SECTION VIEW

Figure 8-15. Overcurrent Trip Device for Type KA Breakers

(Continued from Page 208)
tripping attempts the current and time delay are unvaried from calibrated values.

The instantaneous trip element has a fixed air gap and a tensioning spring for current pickup calibration. The armature is a directly acting unit, a trip screw striking the circuit breaker tripper bar tripper with some force. This rotates the tripper bar, releasing the latch, and opening the circuit breaker.

The individual armatures of the two elements pivot on a common pin. The current flowing through a series coil surrounding the upper leg of the magnet supplies the force to operate the Overcurrent Trip. The armature of either element is attracted towards the electromagnet when the current reaches, or exceeds, the previously adjusted value. The armature that moves depends upon the current values and time-delay characteristics of the elements. Essentially, the circuit breaker will trip when either of the armature trip screws strike the tripper bar tripper.

7 GENERAL ELECTRIC TYPE AK-1-15-3 BREAKER. - Although the purpose of the GE breaker is the same as the I-T-E breaker in the Switchgear installation, there are sufficient functional differences to warrant that it be separately described. Drawing 186616 shows the Schematic of this breaker as used within the Switchgear for breakers CB102H, CB102S, CB103, and CB104. The typical operation description of the GE breaker will be used as the basis for the continuing description of the Switchgear operational sequence.

The manual action of pressing the AC ON control will now result in the following. Figure 8-16 (Typical AK-1-15-3 Schematic). (Refer to Figure 8-17 CB102H Closing Sequence.) Ø1L6 power, passing through the contact of RP48, and the contacts of the AC ON switch located at the Power Supply, reaches CB102H. Passing through contacts bb (closed) and yc (closed), coil X is

(Continued on Page 212)

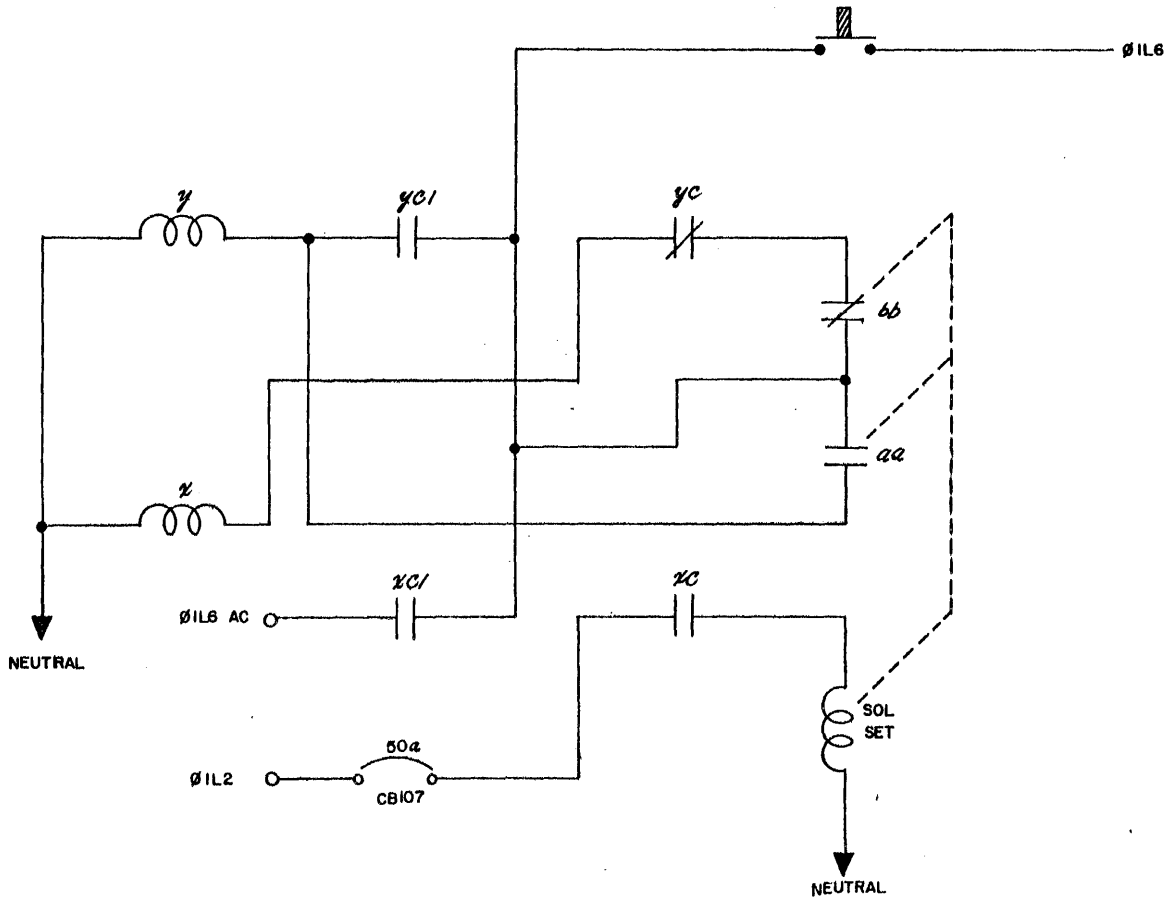


Figure 8-16. Typical G.E. AK-1-15-3 Schematic

(Continued from Page 210)
energized, which attracts the armature and energizes the breaker closing coil (solenoid set) through the relay contacts (xc,xcl). (Note that the solenoid set coil receives energy from Ø1L2 via the 50-ampere circuit breaker in that line.)

Similarly to the operation of the Type KA circuit breaker, at the end of the closing stroke, contacts bb will open the pickup coil circuit due to the mechanical action of a "prop" switch, permitting coil y (holding coil) to attract the armature through contacts aa, now closed. The closing of contacts ycl and opening of yc by coil y will now effectively prevent the relay from recycling. The release of the AC ON switch de-energizes coil y; however the breaker remains closed as long as sufficient voltage is available, through the action of the Undervoltage solenoid. If the closing switch is operated while the breaker is in the closed position, or is held closed after the breaker closes, the coil of the y relay will become energized through contact aa. This will open contact yc and thus prevent the x coil from energizing. It is therefore impossible to operate the closing solenoid when the breaker is already closed.

When coil x closes contact CR1, Figure 8-17 , the SOL SET coil closes the 150 amp circuit breakers and three-phase power is provided to Heater Booster T101/T102 and Stabiline 1 and 2. The exception to the above statement will be in the case of 240 volts a-c service, in which case the booster is eliminated. CB102H will be maintained in a closed position by mechanical latching, and contact CR1 will have opened as solenoid PC(x) was deenergized.

The green AC ON lamps on the Switchgear, at the Power Supply control panel and overhead will be turned on through the No. 2 contacts of CB102H from Ø1L6,

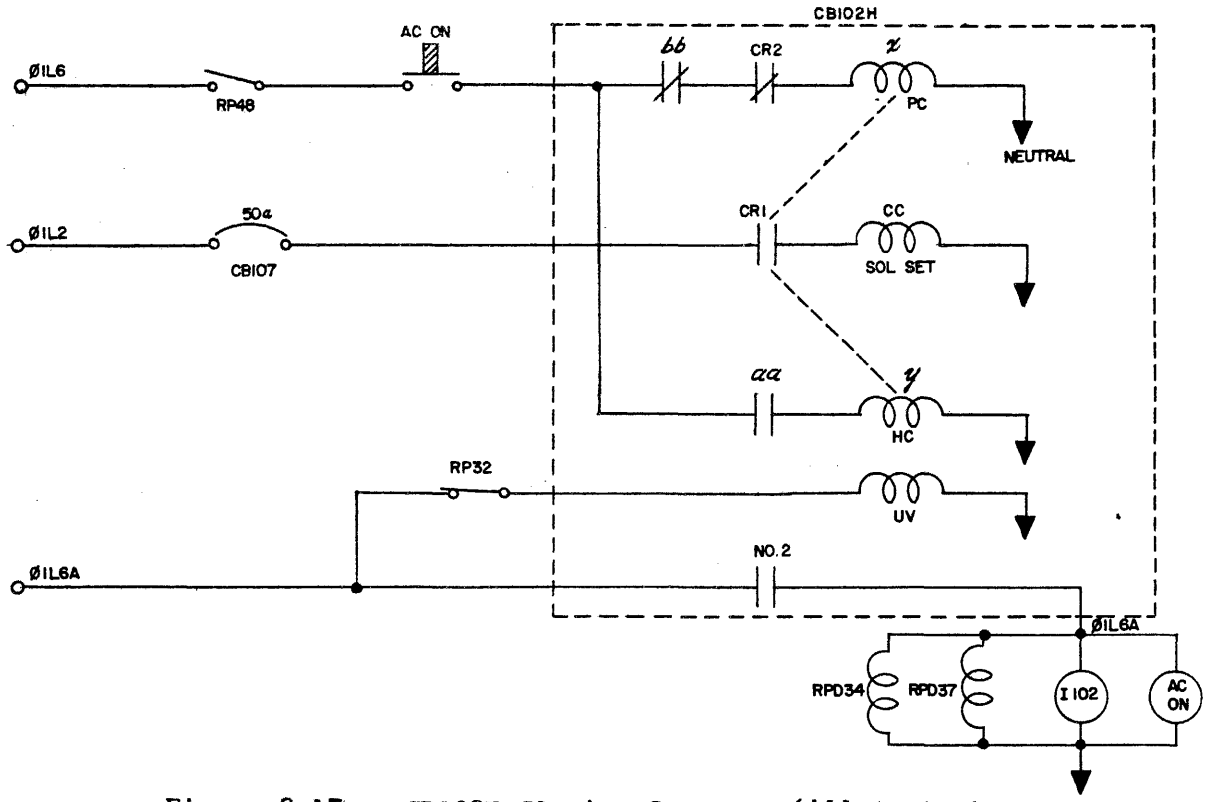


Figure 8-17 . CB102H Closing Sequence (All contacts shown in non-actuated position)

the line distributing this power being identified as ØlL6A. In addition to the foregoing, No. 1 contacts of CB102H will now be closed thus completing the Shunt Trip circuit within CB102H, should the external circuit to this contact be completed. Phase 1 Line 6A power also actuates RPD34 and RPD37 through the No. 2 contacts of CB102H. The functions of the contacts of RPD34 and RPD37 are described in a later paragraph. Furthermore, the shunt is removed from CB102S and 120 vac is applied to CB102S.

Summarizing the action of CB102H, the following functions are performed when this breaker closes:

1. Phases 1, 2 and 3 of line 2 are applied to the Heater Booster transformers and Stabiline. The subsequent three-phase output is applied to the Central Computer.

2. Phase 1 Line 6 power is applied to RPD34 and RPD37.

3. The CB102H shunt trip circuit is potentially prepared to operate.

4. All AC ON indicators are lit.

5. The No. 4 contacts of CB102H open the shunt trip path of CB102S.

6. The No. 2 contacts of CB102H apply Ø1L6A power to CB102S.

CB102S, the Servo Circuit Breaker, now operates in a similar manner to that which closed CB102H. As CB102S closes Phases 2 and 3 of line 2 are applied to Servo Booster transformers T103 and T104. Depending upon input rating, the exact assemblies will vary, the protected output of CB102S going to å Stabiline unit in the case of a 240-volt three-phase input service. The output is on Phases 2 and 3 of line 5.

(b) RPD37. - Refer to Figure 8-18 (RPD37 Contact Circuit). The actuating of RPD37, a time-delay relay adjusted for a release time of approximately five minutes, completes a circuit (Ø1L6) to the Blower Motor contactor coil and thence to neutral. The completion of this circuit from Ø1L6 is dependent upon the closure of contacts on relay RP53, located in KL corner of the Central Computer. The action of this relay is described later; however, RP53 will be closed only if an overheat condition does not exist in any of the bays or in the Power Supply. In the event of failure of either a-c of d-c power due to bay or Power Supply overheat, RPD37 continues closed for the delay of five minutes; however, the circuit itself will be opened at the RP53 contacts immediately when bay overheat occurs.

(c) RPD34, RPD35, RPD36. - Refer to Figure 8-19 RPD34-36 Solenoid and Contact Circuit). The closing of CB102H actuates RPD34, which is also a time delay relay, in this case adjusted for an approximate one minute delay before closing. As RPD34 closes (its solenoid in series with a normally-closed contact of RP49, described later) 110 vac on Ø1L6A is applied to No. 2 contactor in HJ corner, the action taking place at that location being described in the section of the manual discussing the Central Computer. In

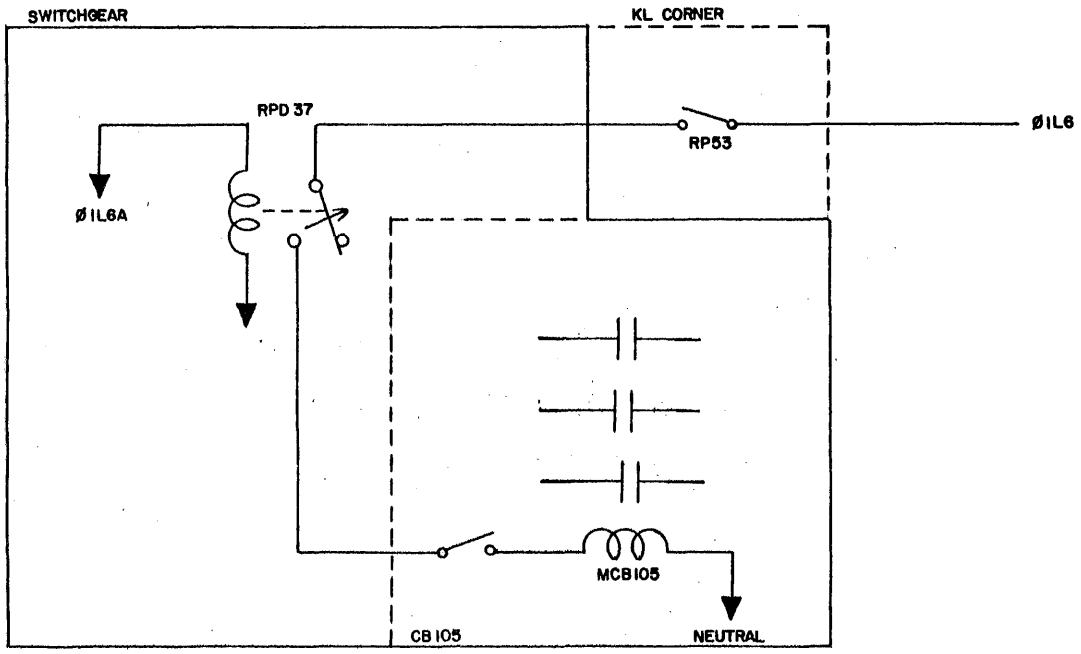


Figure 8-18. RPD37 Contact Circuit

addition to this, the same 110 vac is applied to the Solenoid of RPD35, again through a series contact of RP49.

As has been stated, the activation of Heater Booster T101, T102 and Stabiline, if used, provides power to certain portions of the Central Computer on three-phases. Phase 2 line 4 has been applied to HJ corner where it is reduced by dropping resistors so that only 50 percent of normal voltage is applied to the heater circuits. With the closing of RPD34, which follows one minute after the initial application of power, the energizing of the No. 2 contactor solenoid in HJ corner closes No. 2 contactor, which in turn shorts out some of the series resistance in Ø2L4 and Ø3L4 heater line, thus applying an additional step of voltage to bring it up to 66 percent of normal maximum.

RPD35 also adjusted for a delay of about one minute, energizes No. 3 contactor solenoid in HJ corner. This short-circuits

(Continued on Page 217)

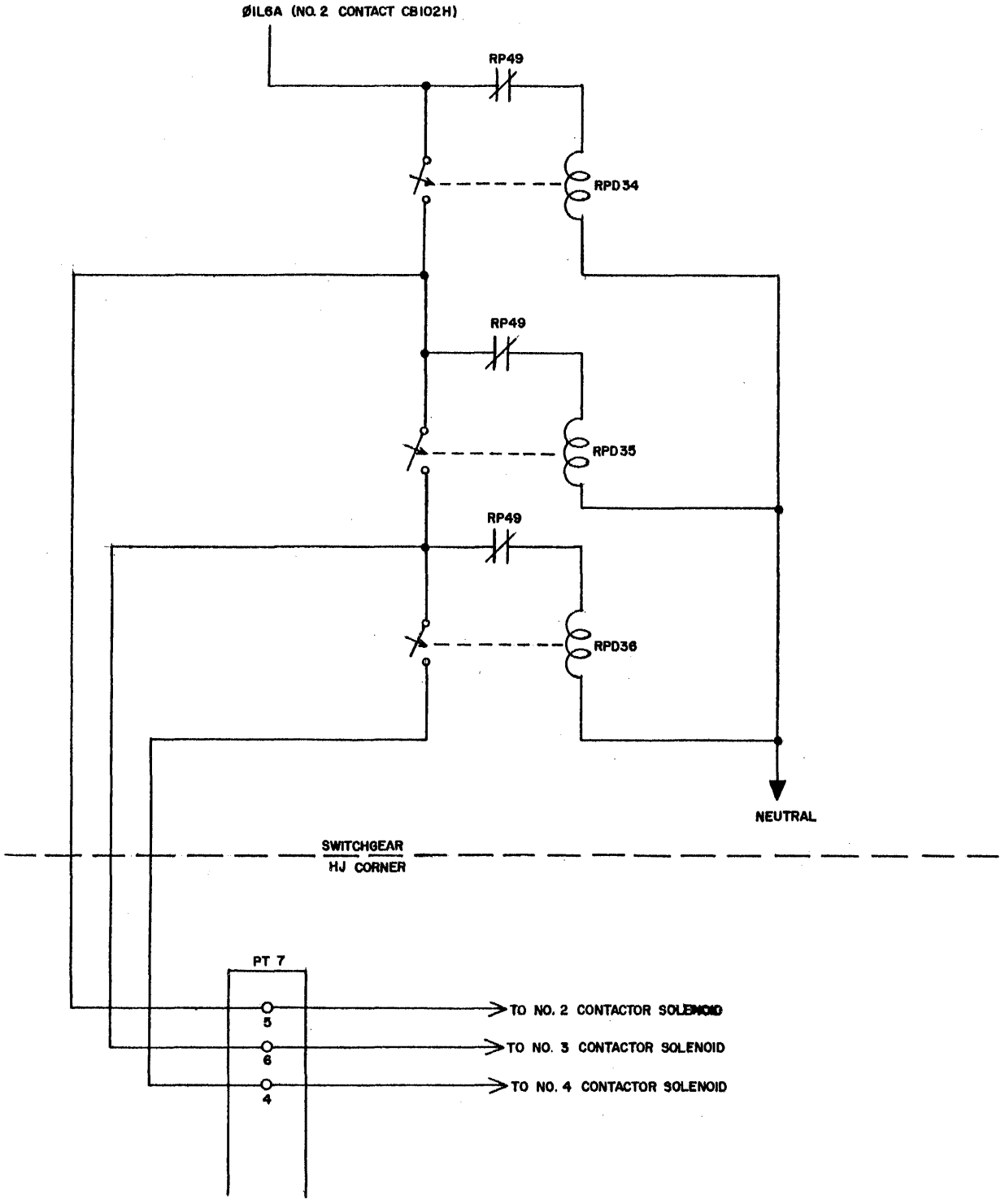


Figure 8-19. RPD34-36 Solenoid and Contact Circuit

(Continued from Page 215)
a further portion (via contactor No. 3) of the heater transformer series resistance bringing the applied power to 85 per cent of the total required. As RPD35 closes it also applies closing current to the solenoid of one minute time delay RPD36 (again via a normally closed contact of RP49).

The closing of RPD36 completes a 110 vac circuit to No. 4 contactor solenoid in HJ corner via the KL Corner Margin switch and the ultimate result is the full application of Ø2L4 heater power to the equipment. The 110 vac from the contacts of RPD36 is also applied to the solenoid of RP32, which closes the latter.

(d) RP32. - When RP32 closes, one set of contacts completes a circuit from Ø1L6 to the solenoid of RP49. RP49 utilizes closed contacts in the non-actuated state for series continuity of the solenoids of RPD34, 35 and 36. The opening of these series contacts, when RP49 is actuated, results in the resetting of the above three timing relays. Note in Figure 8-20 (RP45-RP49 Actuating Circuit) that the Undervoltage Solenoid of CB102H, which has been receiving this voltage from Ø1L6 via one set of RP32 contacts will now be receiving this voltage exclusively along the Airvane Interlock series line. (Thus if any of these interlocks remain open the lack of voltage on the under-voltage Solenoid will release CB102H.)

The same set of contacts that cause RP49 to energize also place 110 vac on the coil of RP45, providing that the "Lock Open" switch -- a safety feature at the motor-generator -- is in the closed position.

The remaining set of contacts on RP32 permit the energizing voltage to remain across the solenoid to "self-lock" the relay following the removal of the source voltage arriving via RPD36.

(e) 75 HP MOTOR STARTER. - The single contact closure of RP45 completes a circuit initiating the start of the Motor Starter unit. The Motor Starter unit type varies with the Switchgear in use and will depend upon the

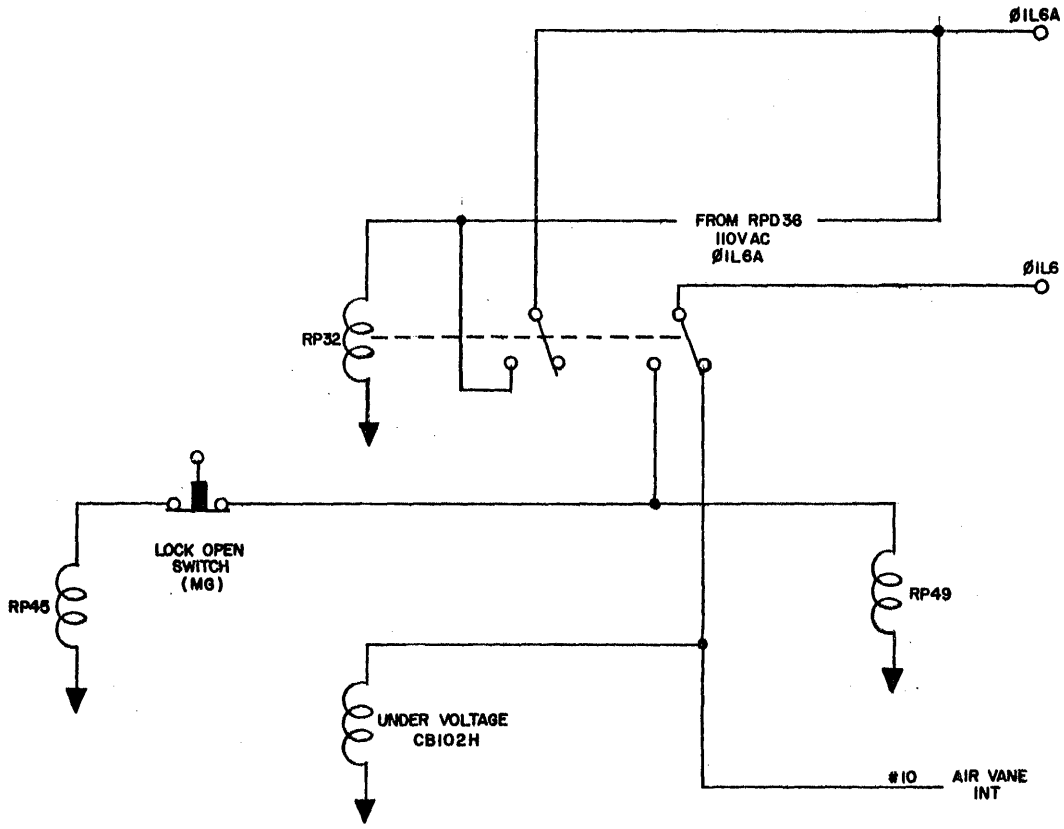


Figure 8-20. RP45, RP49 Actuating Circuit

installation mode. A typical and very generalized sequence of operation of this unit is given due to the varied types of Motor Starters installed.

The unit selected for this description is one employing a Motor-driven timer unit, such as is employed in Switchgears using General Electric Magnetic Starters. Other Switchgears employing Cutler-Hammer or Allan-Bradley motor starters differ in components and timer types but, theoretically, are the same.

Referring to Figure 8-21 (75 HP Motor Starter Circuit) it is seen that when RP45 closes, the Starter Solenoid circuit MS is sompleted from one side of the 440-volt line (A), through thermal overload contacts (1) (these

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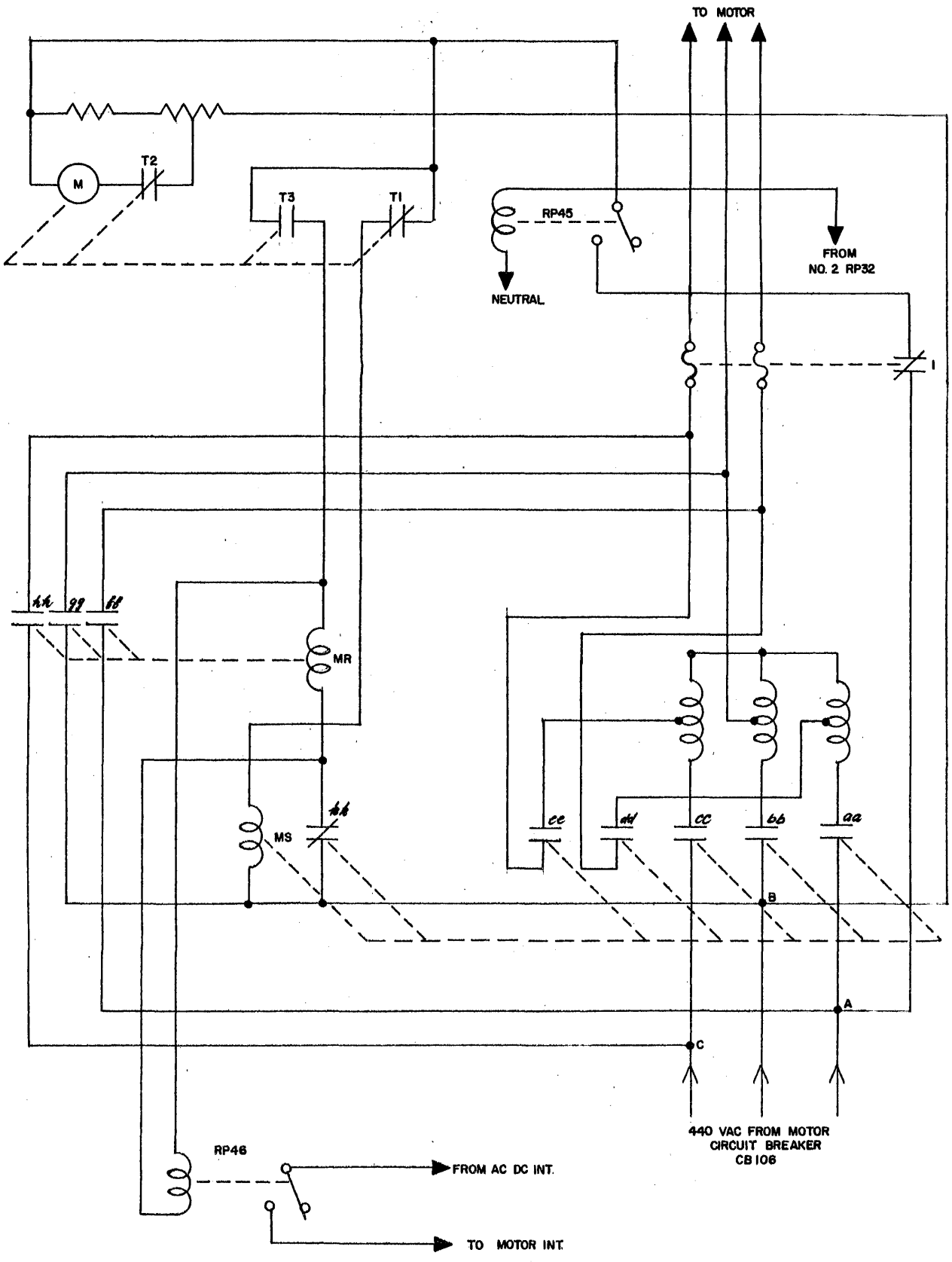


Figure 8-21. 75 HP Motor Starter Circuit

(Continued from Page 218)
contacts open during running if the current drawn by the alternator motor exceeds the rating of the heater elements), through the contacts of RP45, to the timer motor M and to the timer motor contact, (T1) which is closed. The solenoid circuit will be completed to the a-c line point B. The timer motor circuit is completed to point B through contacts T2. At this time, two occurrences will be taking place. One, the timer motor will commence operating, and the timing cam will not actuate any switch contacts within the timer until a delay of about eight seconds has occurred. Two, the Motor Start solenoid, MS, will actuate (in this example) six sets of contacts, closing five of these and opening one. The voltage path will be from points A, B and C through contacts aa bb and cc, respectively, to line impedances adjusted by variable taps for a voltage drop of 50 per cent. The voltage path to the motor from the impedance on line A will be via contact dd and the thermal protector; for line B directly to the motor; and for line C via contacts ee and the thermal protector.

The 50 per cent of normal voltage will continue to reach the motor in this manner for the duration of the time delay, previously adjusted to eight seconds. MS contact kk which is normally closed when MS is not energized, is now open.

Upon completion of the time delay, during which time the motor has been gradually accelerating, the timer will: open contact T2, disabling the timer motor circuit; and open contact T1, thus breaking the MS circuit, which again closes contact kk. Simultaneously contact T3 closes which permits a continuous path around the line impedances for the energizing of Motor Run solenoid MR, to line point B. The voltage path will now be observed to be from points A, B and C through contacts ff, gg and hh respectively to the Motor, the 100 per cent value of voltage is applied to the Motor. The mechanical as well as

electrical interlock feature of the Motor starter assures that one circuit will be completed before the other is released. As Solenoid MR is energized, relay RP46 will also be energized.

(f) RP46. - The contacts of RP46 complete a 110 volt a-c circuit which is shown in Figure 8-22 (RP46 Contact Circuit). Effectively, this circuit accomplishes the following:

1. Applies 120 vac to T106, a stepdown to 24 volts transformer for the purpose of interlock test series connection and actuation of relay RP47, should all interlocks be satisfactorily completed. As shown, the circuit passes via contacts in the Alternator Overvoltage Monitor; RP53 (KL Corner) and Machine Overheat interlocks.

2. Completes a 120 vac circuit to the Undervoltage Solenoid of CB104.

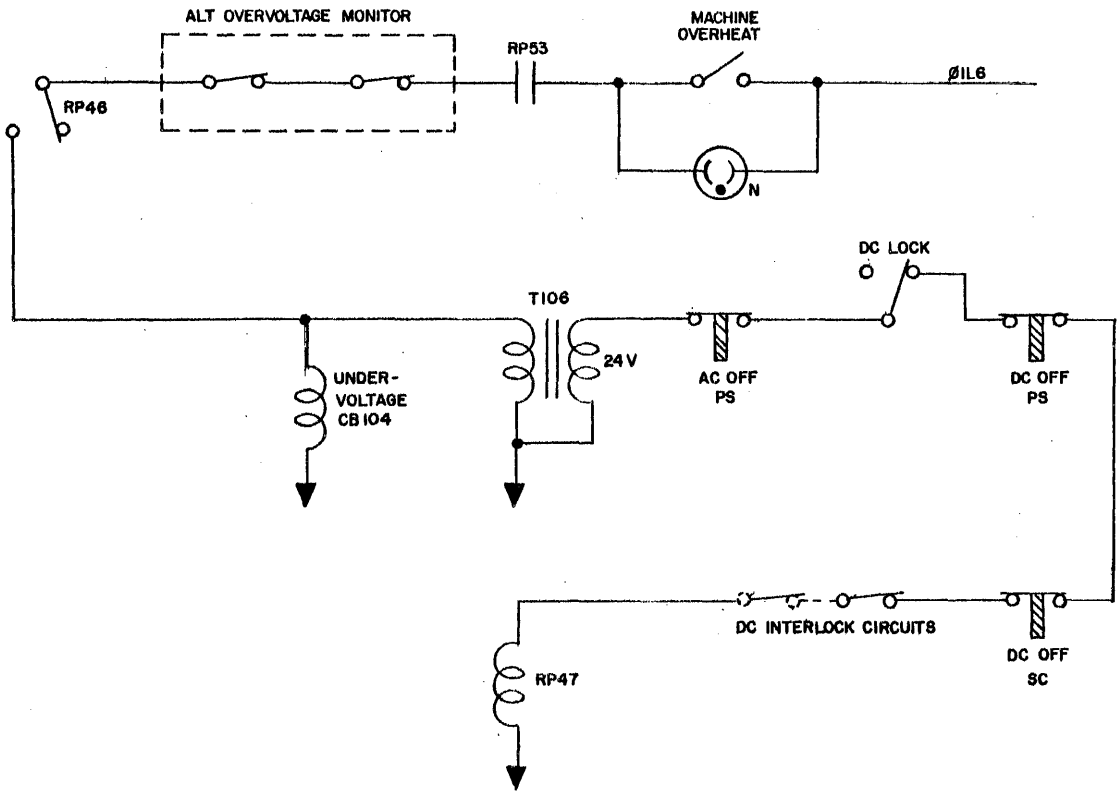


Figure 8-22. RP46 Contact Circuit - RP47 Energizing

The 24 volt ac circuit to RP47 is not completed unless a number of primary functions are also completed -- AC OFF switch closed (not impulsed), DC LOCK switch turned on with key provided, DC OFF switch closed (not actuated) both at the Power Supply control panel and Supervisory Control, and all d-c interlock switches closed.

(g) RP47, RP33, RPD38. - RP47, when energized, closes two circuits and opens one. One contact applies 120 vac to the movable contact of RP33, which, being in a non-energized position, completes a circuit energizing RPD38. RPD38, a time delay relay adjusted for five seconds, permits this period to elapse for the purpose of allowing the heater voltages to stabilize. At the end of thirty seconds, RPD38 closes, 120 vac passes through the contacts to the solenoid of RP33, which closes immediately.

The other closing circuit contact of RP47 also applies 120 vac to a movable contact of RP33, but, as the relay is not energized, no action occurs in this instance as the associated stationary contact is not connected.

The opening circuit contact of RP47 opens the shunt trip circuit of CB104 which would ordinarily be created when the No. 1 contacts of that circuit breaker are closed.

It must be clearly understood that a rapid sequence of operation is ensuing at this point, and for this reason a brief recapitulation is given. Reference should be made to Figure 8-23 (RP47-RP33-RPD38 Sequence) below in order to clearly understand the operation.

RP47 closes which, 1) opens CB104 shunt trip circuit, 2) places 120 vac on one contact of RP33 (without effect for thirty seconds) 3) energizes the solenoid of RPD38. The latter, after thirty seconds, closes energizing RP33. This action removes the energizing voltage from the solenoid of RPD38, restoring it; however, the same source of voltage is now placed on the solenoid of

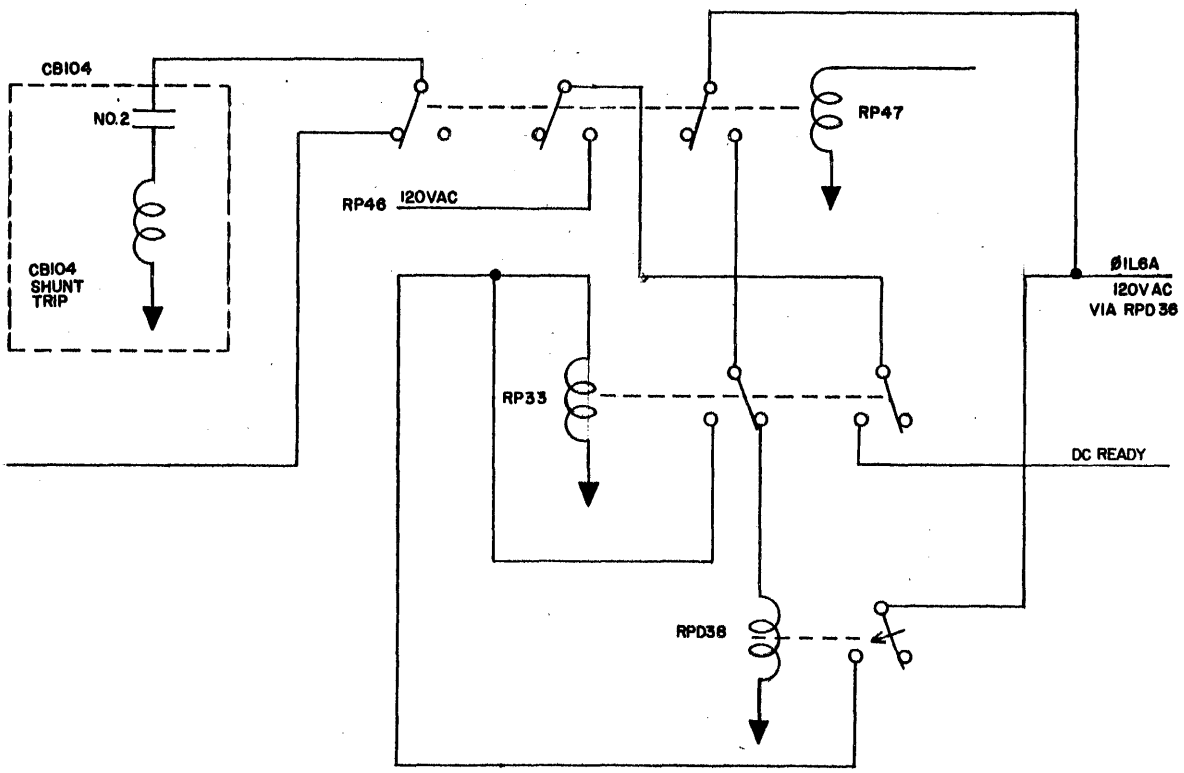


Figure 8-23. RP47-RP33-RPD38 Sequence

RP33, maintaining RP33 in a closed position through the self-energizing contact.

The remaining set of contacts on RP33 are utilized for routing 120 vac on the DC READY line to the yellow lamp which indicates DC READY at the Power Supply control panel. In addition, this voltage is routed to one side of the DC ON switch, also at the PS control panel. Further Switchgear function requires that the DC ON control switch be operated.

(h) CB103 ACTUATING CIRCUITS. - The DC ON control switch, located at the Supervisory Control, lights the red DC ON light at the Power Supply control panel, Switchgear and at the overhead position. This is accomplished through the same line that the DC READY indicator receives power, being a series continuance of this line. The switch continues the circuit back along the DC ON line to the Switchgear where the solenoid of RP30 is energized to the neutral side of the ac line.

As shown in Figure 8-24 (CB103 Actuating Circuits), RP30, the Shunt Trip Interrupt relay, opens the shunt trip circuit of DC Circuit Breaker CB103. The line energizing RP30 also energizes coil x of CB103 via closed internal contacts (bb,yc) of CB103. As coil x energizes, the armature is attracted and closes the main relay contacts xcl and xc, the latter contact completing a circuit to energize the Solenoid.

The undervoltage coil of CB103 was energized with ØlL6 power when control power was first applied. The solenoid plunger now moves towards the closed position, which, when reached, closes all normally open contacts and opens all normally closed contacts within CB103. As this occurs, a contact (aa) is closed which permits coil y to be energized. A contact of coil y (yc) opens the circuit to coil x, causing x to release and prevents recycling as long as y is energized. As contact xc was opened when coil x released, the main contacts of CB103 are maintained in a closed position by mechanical latching. Any decrease in the current through the UV coil will cause the breaker contacts to open, resulting in the disconnection of voltage to the Power Supply. The action described is identical to that described for CB102H.

(i) CB104 ACTUATING CIRCUITS. - DC Breaker No. 2 (CB104) closes similarly to DC Breaker No. 1, resulting in the output from the generators being connected to the Power Supply. Tapped lines from the outputs of the circuit breakers serve a protected switched metering circuit including a vibrating-reed type frequency meter with a indicating range of 380 to 420 cycles, and an 400 cycles a-c voltmeter, 0-300 volt scale. As soon as the output of the generators is available at the Power Supply, the DC ON switch will be released, thus releasing RP30. The shunt circuit of CB103 will be maintained open by the No.2 contacts of CB104. (Continued on Page 226)

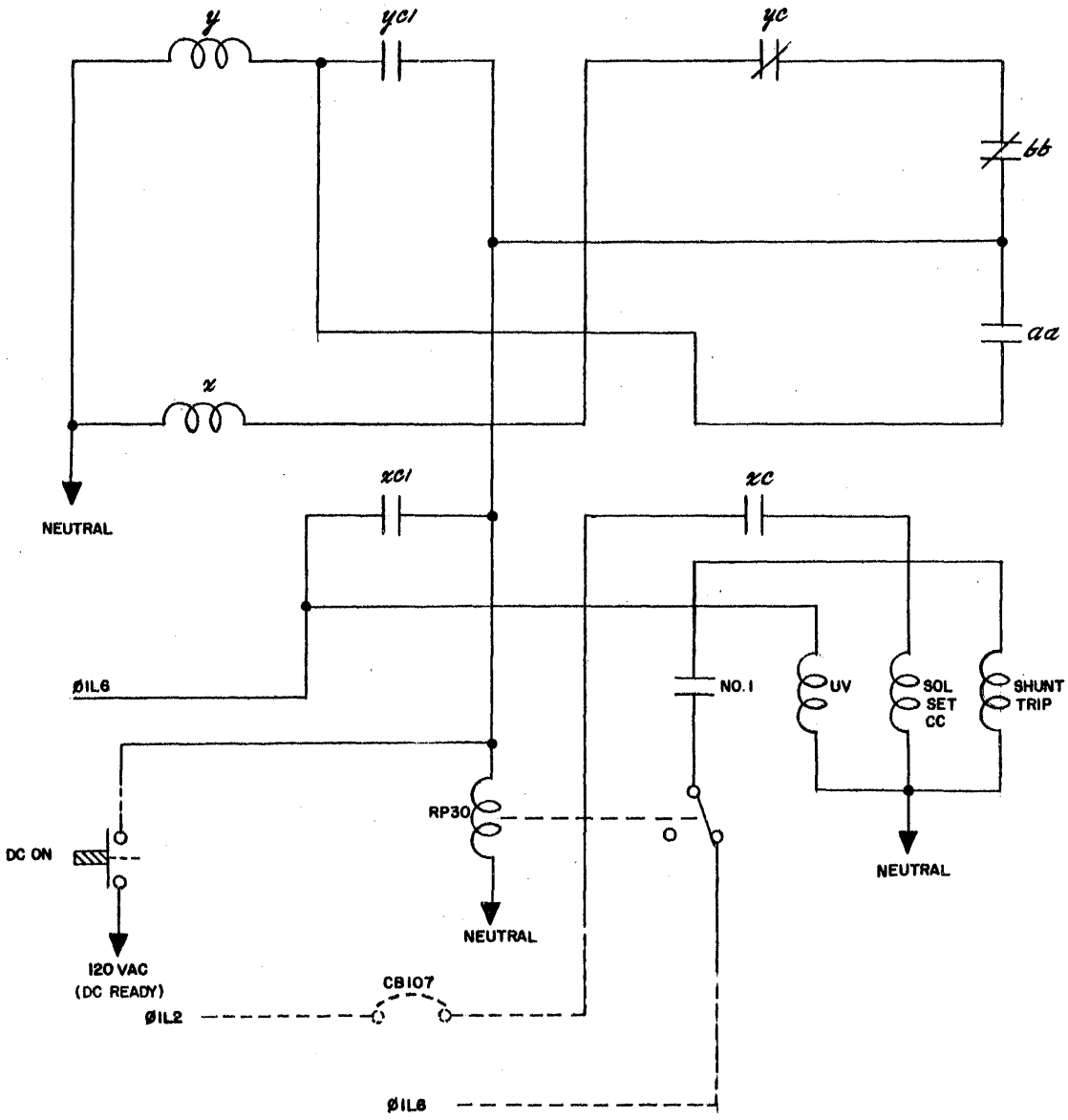


Figure 8-24. CB103 Actuating Circuits

(Continued from Page 224)

The foregoing paragraphs have given a detailed account of the sequence of operation of the Switchgear assembly from the point where voltage is received at the Main AC circuit breaker until 400 cycle a-c voltage is presented to the Power Supply from the Motor Alternators, with voltages being supplied to the Central Computer, the Uniservos, blowers and control circuits in the process. A brief resume' of this sequence of operation follows for quick reference purposes.

Condition: CB106, CB105, CB107, Power Supply control breaker - all closed.

1. Main circuit breaker CB101 closed

   CONTROL POWER orange light on

   RP48 closes.

2. AC ON switch closed

   Heater and Servo breakers CB102H and CB102S close

   AC ON green lamp on

   RPD37 closes

   MCB105 closes (blower motors start)

   RPD34 closes (approximately 1/2 heater voltage)

   RPD35 closes (approximately 7/8 heater voltage)

   RPD36 closes (full heater voltage)

   RP32 closes

   RP49 closes

   RP45 closes

   Reduced voltage contactor Motor Starter closes (75 hp motor)

   Full voltage contactor Motor Starter closes (MCB105)

   RP46 closes

   RP47 closes

   RPD38 closes

RP33 closes

DC READY light on

3. DC ON switch closed.

RP30 closes

CB103 closes (one line of each generator connected to Power Supply)

CB104 closes (all lines of each generator connected to Power Supply)

DC ON red light on

DC ON switch released

RP30 opens.

c. POWER SUPPLY. - The power supply system provides all d-c voltage requirements for the Central Computer. The a-c input voltages to the Power Supply rectifiers originate at the motor-alternators. The motor-alternator output is routed via the Switchgear to the Power Supply. As one output of the alternator leads the other by 30 degrees, there are actually two 3-phase inputs provided to the Power Supply.

The rectified d-c voltages are applied to a bleeder network, in addition to a direct connection to the Central Computer, permitting various voltages to be provided. Additionally, a 600-volt Uniservo brake and clutch power supply is housed in the Power Supply cabinet, and a standby power supply also within the cabinet provides control and indicating voltages in the event of failure of any of the Power Supply units.

Physically, the Power Supply measures 5'10 1/4" high by 6' 1/2" wide and 2'6" deep and weighs 3700 pounds approximately, the entire unit is divided into ten bays identified Q through Z. Forced air cooling is provided within the cabinet, with cool water circulating in the base, and blowers directing the cooled air upwards. The resulting average ambient temperature is 30C.

The blower motor control lines and air temperature thermostat switch connections are shown on Drawing 186571 up to the Power Supply terminal boards. Drawing 186571 does not show the original voltage source for the blower motors or the series arrangement of the thermostats and air switches. Since this discussion is confined to the Power Supply system, it is sufficient to say that this source is originally 3-phase, 208 vac. The two thermostats in the cabinet operate on approximate limits of 95F and 110F.

Three air switches in the Power Supply are part of the a-c interlock system. Air pressure directed against vanes on these switches hold the switches in a closed position. If the volume of air against the switch vane is insufficient for adequate cooling, the interlock circuit opens. Failure is indicated by loss of a-c and d-c power, and the failure of all lights, with the exception of the CONTROL power indicator and STANDBY power neon indicators. Air filters in the base of the Power Supply filter the air prior to use. Further details respecting the cooling system may be found under "Cooling System".

The interlock system at the Power Supply is part of the d-c interlock system which is an extension of, and in series with, the DC OFF control switches. Each bay door and the fuse covers have these interlocks. The bay door interlocks may be disengaged by manually pulling out the interlock switch shaft after the door or cover is removed. Replacing the door again places the interlock in a normal condition. The fuse covers complete a wired circuit which may be seen through the cover material from end-to-end of the cover. To cancel the effect of this interlock it is necessary to operate the Interlock By-pass key at SC (which also cancels the door interlock system). This system is described in the section discussing the interlock circuits.

The physical placement of the power supply chassis within the Main Power Supply cabinet are shown in Figures 8-25 and 8-26, with the specific chassis locations listed in Drawing 186481 - Power Supply Assembly,

(Continued on Page 231)

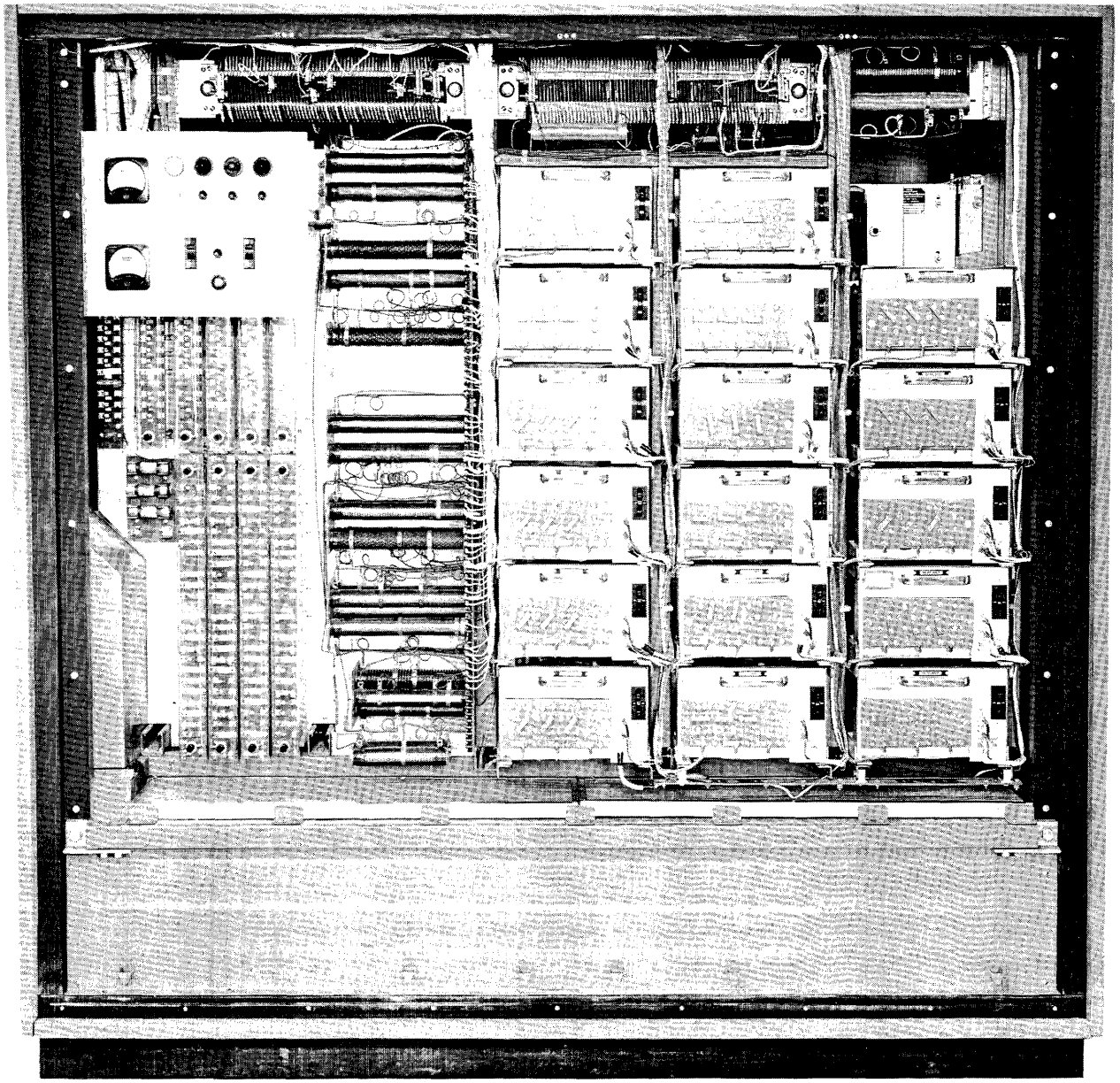


Figure 8-25. Power Supply, Front View (Cover Removed)

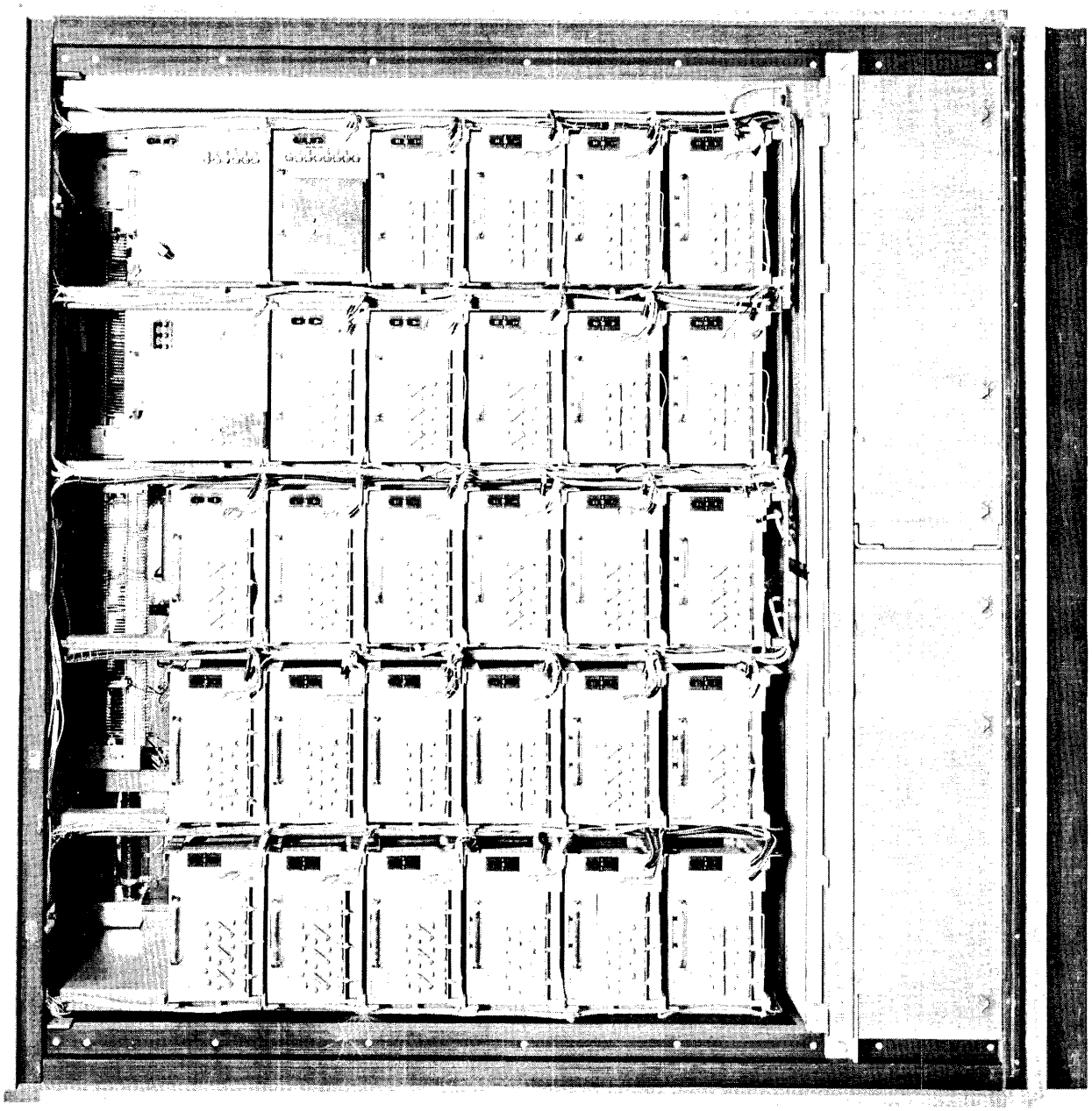


Figure 8-26. Power Supply, Back View (Cover Removed)

(Continued From Page 228)
Wired. Although each chassis (with the exception of Standby Chassis) is electronically identical; through the use of different transformer primary taps and subsequently different secondary voltages, variations in output voltages are provided by the use of three chassis types, differing only in transformer specifications and circuit breaker ratings. The three types of chassis are provided in multiplex.

The physical position of each resistor, the total series connection of which comprises the bleeder network, is shown in Drawing 186481. The circuit of the network will be considered later in the text.

(1) POWER SUPPLY CHASSIS. - Twenty-seven power supply chassis provide positive voltages, and eighteen provide negative voltages. Two additional chassis provide standby power and one other chassis provides power for the Uniservo brake-clutch requirements. Each chassis is identified by letter symbols depending upon the bay in which located. A complete listing of the various chassis follows:

(a) MAIN POSITIVE:

Chassis	Output (volts d-c)
V2	52
V3	52
V4	51
V5	55
V6	46
V7	40
W2	45
W3	45
W4	30
W5	30
W6	30

W7	30
X2	30
X3	55
X4	55
X5	30
X6	30
X7	30
Y3	35
Y4	30
Y5	30
Y6	30
Y7	30
Z4	40
Z5	40
Z6	30
Z7	30

(2) MAIN NEGATIVE:

Chassis	Output (volts d-c)
S2	55
S3	32
S4	34
S5	34
S6	40
S7	40
T2	42
T3	42
T4	55

T5	40
T6	30
T7	30
U2	40
U3	40
U4	31
U5	31
U6	54
U7	34

(3) STANDBY:

Z2 -230S, -191S, -166S, -48S, -28P

Z3 +48S, 28 (ac)

(4) SERVO:

Y2 +600

The distribution of the Main Negative Supply within the Power Supply cabinet is given on Drawing 105490, the Main Positive Supply on Drawing 105491. A schematic representation of a chassis power supply is shown in Figure 8-27. Values of components for the three different types of supply are given on Drawings 105623, 105624 and 105641.

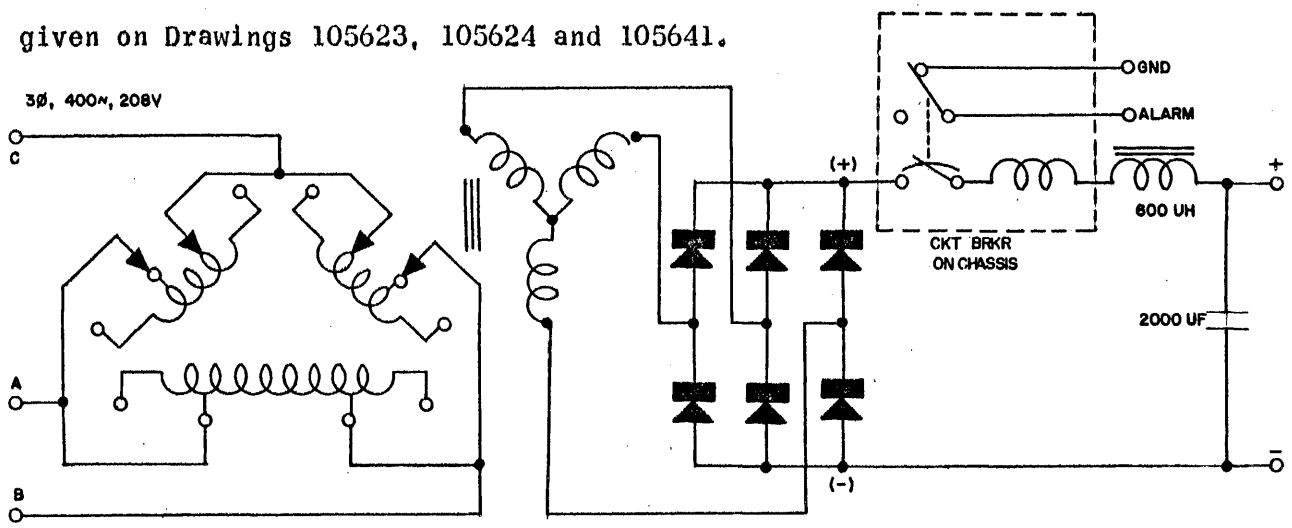


Figure 8-27. Schematic of Power Supply Chassis

The three-phase 208-volt 400-cycle input is provided to a Delta-Wye transformer in the power supply circuit shown. The primary windings of this transformer have various taps on each winding thus providing a variation in the secondary of from 13.0 to 17.0, 17.1 to 21.4, and 21.3 to 25.5 volts rms per-phase, depending upon chassis type.

The secondary voltage appears at a three-phase double-way germanium rectifier assembly. The output from a rectifier circuit of this type is at a high ripple frequency, in this case 2400 cycles, inasmuch as the input is 400 cycles. The single filter choke and large capacitor are sufficient to adequately filter this output.

The only unusual feature of the power supply is the breaker line between rectifiers and choke. In normal operation the circuit breaker provides a straight-through path for current passing from the rectifiers to the filter and beyond. An excessive current beyond the rating of the breaker will cause the breaker to open the circuit. An additional contact in the breaker completes the alarm circuit to ground. The breaker itself provides a visual indication of its opening by the position of the reset toggle.

The 600-volt Uniservo brake and clutch power supply, Chassis Y2, is almost identical electronically to the other power supply chassis. Physically, the components differ considerably, the various values are shown in Drawing 105494. The output of this power supply terminates with a bleeder resistor, and, whereas the circuit breaker of the previously described power supply is on the output side, the Uniservo supply has a circuit-breaker in the primary leads to the transformer. This breaker has a contact which completes the d-c alarm circuit to ground in the event of circuit overload.

The Standby Power Supplies, Figures 8-28 and 8-29, Chassis Z2 and Z3, provide a source of power for various functions (such as alarm) following the

(Continued on Page 236)

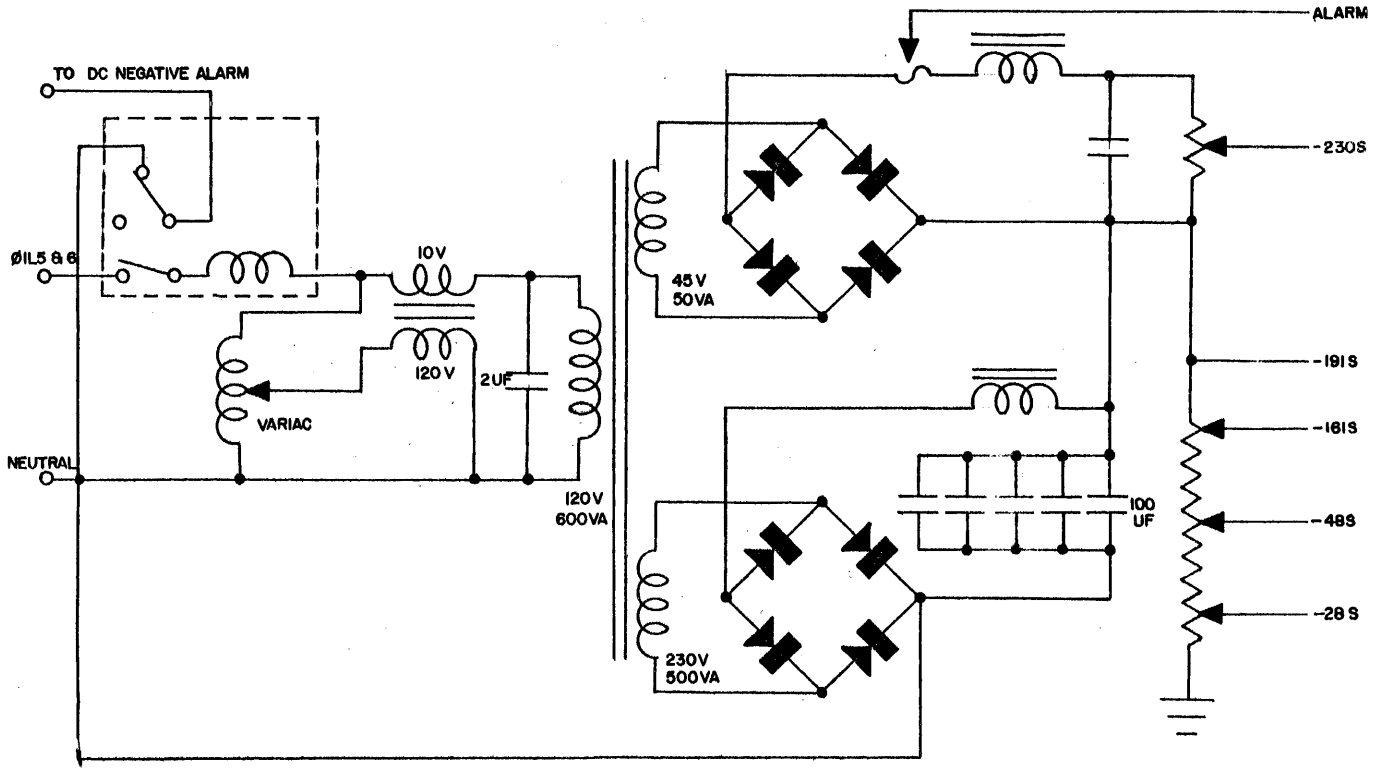


Figure 8-28. Standby Power Supply, Chassis Z2

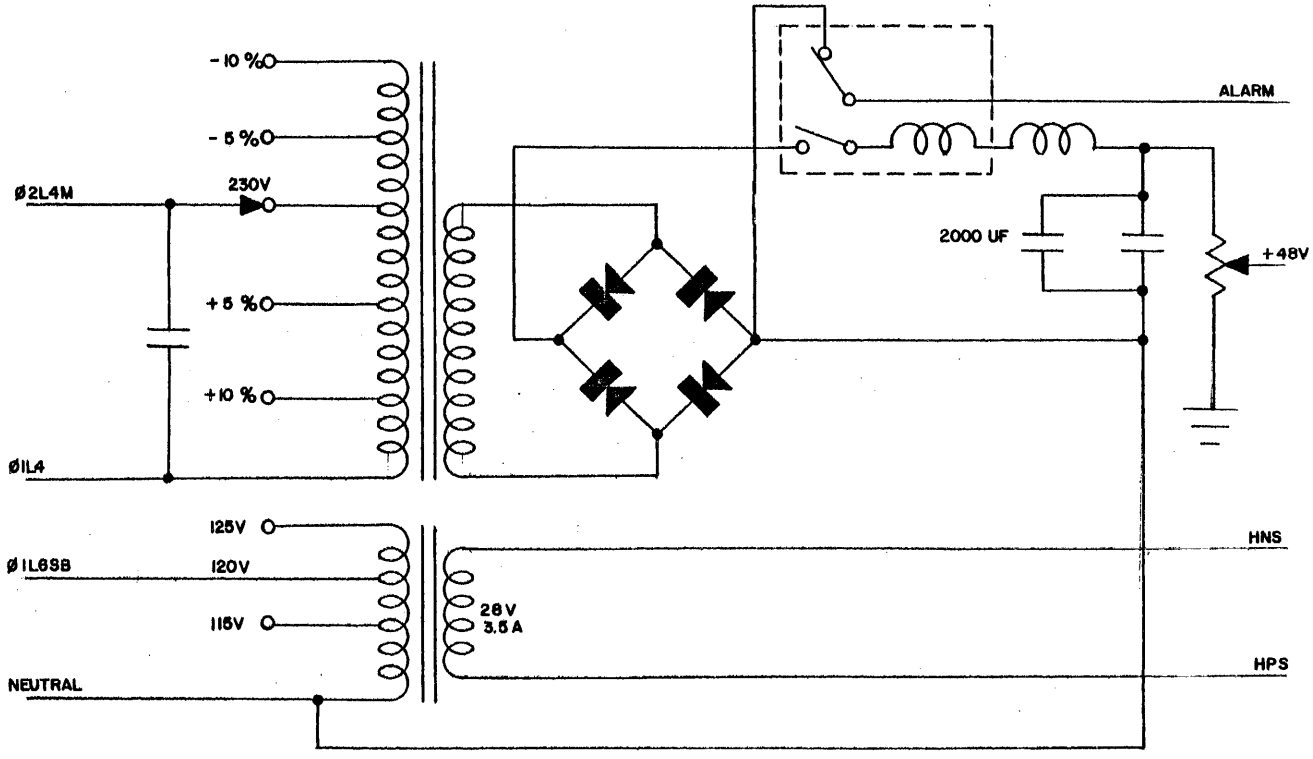


Figure 8-29. Standby Power Supply, Chassis Z3

(Continued from Page 234)
removal or failure of d-c supply. The Z2 chassis has, in the primary leads, a Variac assembly and a circuit-breaker. The transformer has two secondary windings, providing 45 volts at 50 va, and 230 volts at 500 va respectively, to two single-phase bridge-rectifier circuits. The output of this "dual" supply is fused with a 1/4-ampere grasshopper type fuse; the leaf-member contact of this fuse completes the alarm circuit in the event of failure. The output of each rectifier assembly is separately filtered, with the output of the 230-volt supply in series negative with the 45-volt supply. Thus, by the use of various bleeder taps the required negative voltages are made available.

The standby power supply on chassis Z3 also employs a single-bridge rectifier circuit and has an alarm type circuit breaker at the rectifier output. In addition to the 66-volt 500 va transformer used for rectification, this chassis also contains one 28 volt 3.5a transformer whose direct a-c output is used for the computer short tank heater supply.

(2) POWER SUPPLY FUSES. - Fusing of circuits within the power supply is performed at a central panel in Section Q of the Power Supply, directly behind and below the control panel. This fusing is in addition to that for each individual power supply chassis. The fuses placed at the fuse panel are in the primary side of the power supply transformers and also on the load side of the bleeder resistors.

Each column of fuses has received a "Q" designation. Table 8-I indicates the complete identification. Fuse values, types, and wiring circuits are shown on Drawings 125252 through 125257, 125260 through 125263, and 186580.

The two types of fuses used on the panels are Buss Mfg. Company Type BAF, and the grasshopper fuse, which is used extensively throughout the whole computer assembly. The BAF type, with higher current ratings, are used in instances where the normal current requirements would exceed the rated value

of standard grasshopper types. A grasshopper alarm fuse is placed in parallel with each BAF fuse. Should the BAF type open-circuit, the full current passes through the alarm fuse, causing it to open and actuate the alarm circuit.

The event that one of the d-c primary fuses (other than Stand-by) open-circuit under excessive current, the alarm contact of the fuse connects the primary source to the D-C Primary Fault neon and RP17 (external to power supply cabinet). Actuating RP17 causes the d-c interlock contacts of the relay to open, breaking the d-c circuit. Failure of a grasshopper fuse at any position on these panels is indicated by the upright condition of the fuse strip released by the failure of the fuse, in addition to the lighting of the D-C Primary Fault neon indicator. The upright "flag" indicates the supply in which the overload occurred, inasmuch as a label beside the fuse identifies it. For example, Z2 would refer to Position 2 of Bay Z. Figure 8-30 shows the schematic arrangement of the positive and negative d-c alarm circuits. All components other than the fuse and transformer are beyond the physical limits of the Power Supply cabinet; however, in order to clearly show the manner in which the alarm contacts actuate the various circuits, it has been necessary to show the other components. (The purpose of the rectifiers and RD15 is to operate RP17 on +48 vdc, as this relay is also operated by +48 vdc for other faults.)

The terminal strips within the left-hand end of the Power Supply route all control and voltage lines in and out of this unit. The strips are designated QTA, QTB, QTC, QTD, QTE, QTF, QTG, and QTH. Terminal wiring is shown on Drawing 186571.

Bleeder resistor schematic circuits are indicated on Drawings 105490 and 105491. Actual wiring connections are indicated on Drawing 186575. This

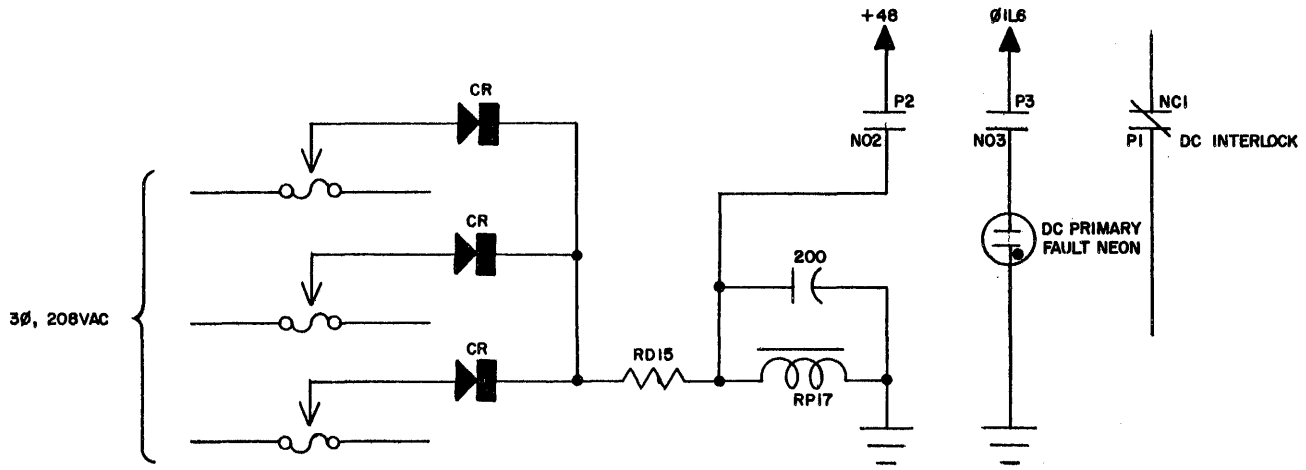


Figure 8-30. Positive and Negative DC Alarm Circuit

drawing also shows terminal voltages normally present at these resistors. The exact position of various taps on the resistors may be determined from Drawings 105490 and 105491.

The remaining unit contained within the Power Supply cabinet, the Control Panel, is not directly related to functions of the Supply. It is discussed in the Section which describes the Switchgear, of which it is an integral unit.

d. STABILINE TYPE EM(ELECTRO-MECHANICAL) VOLTAGE REGULATOR. - The Type EM Stabiline voltage regulator is an electro-mechanical type regulator, with a sensitive voltage change detector controlling a Motor-driven Powerstat variable transformer and auxiliary transformer. The control chassis is mounted as a separate chassis and plugs into a female receptacle on the Stabiline Main Chassis to facilitate rapid replacement if required.

(Continued on Page 253)

TABLE 8-1

POWER SUPPLY PRIMARY CIRCUITS

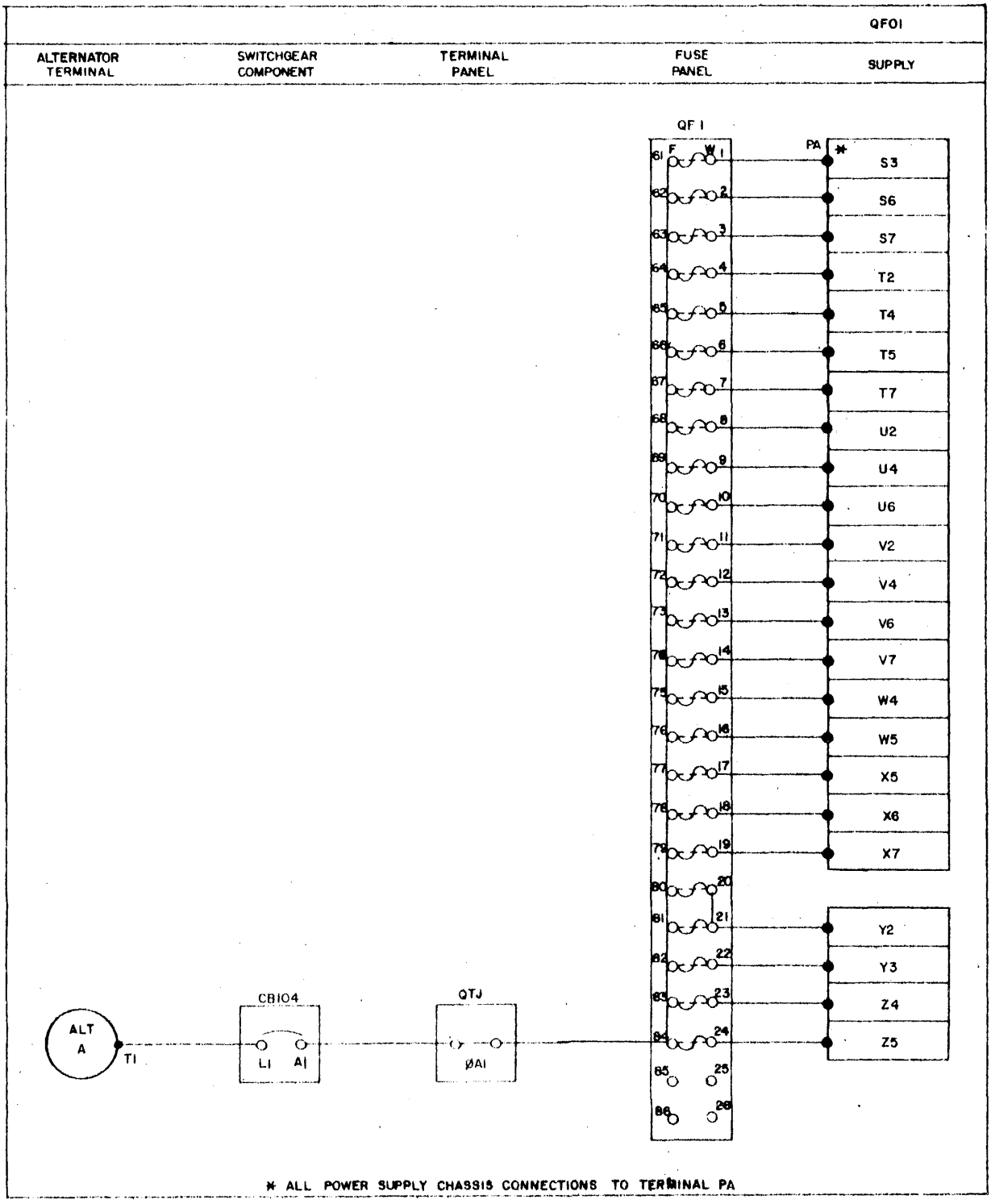


TABLE 8-1 (Cont'd)

POWER SUPPLY PRIMARY CIRCUITS

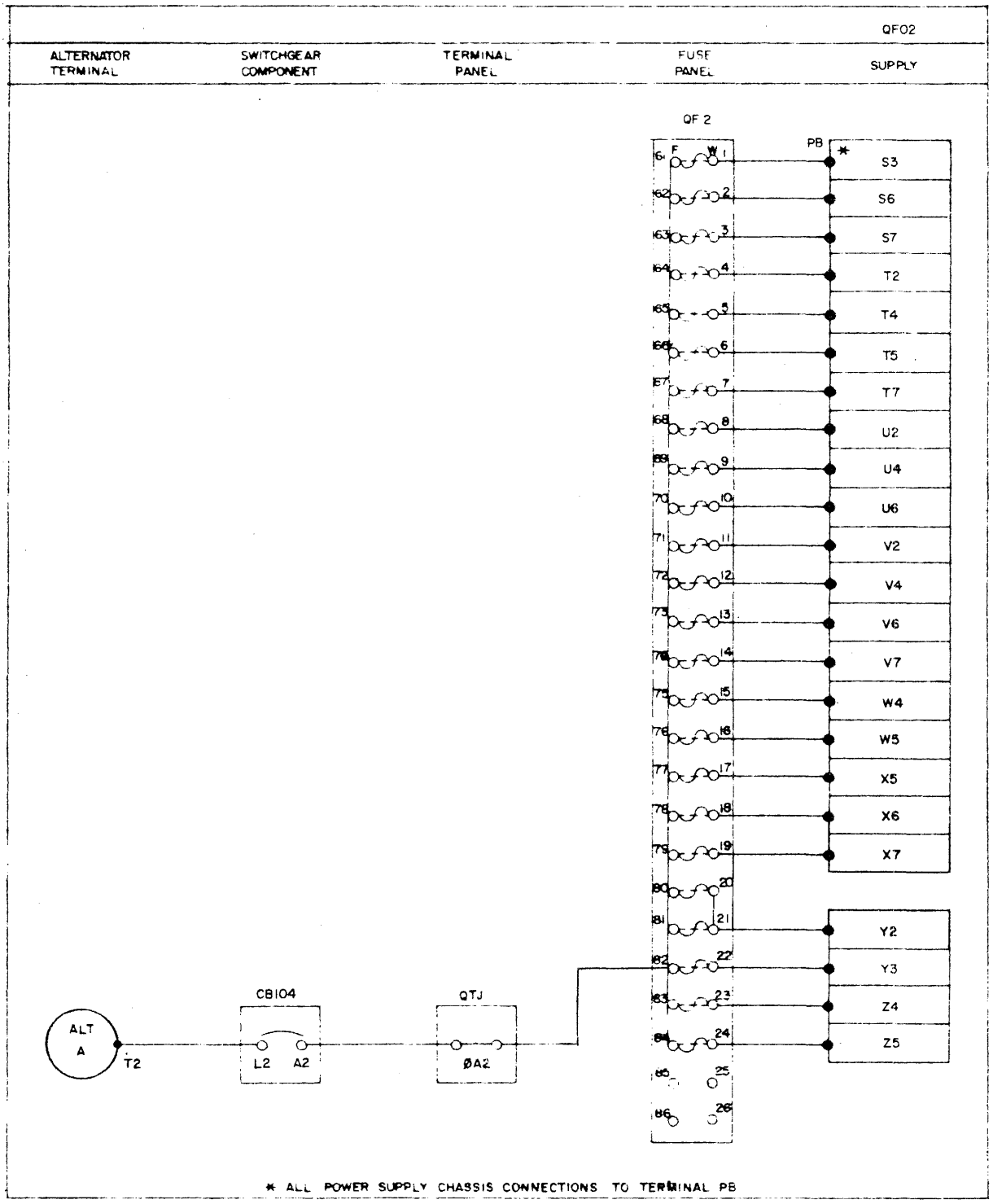


TABLE 8-1 (Cont'd)

POWER SUPPLY PRIMARY CIRCUITS

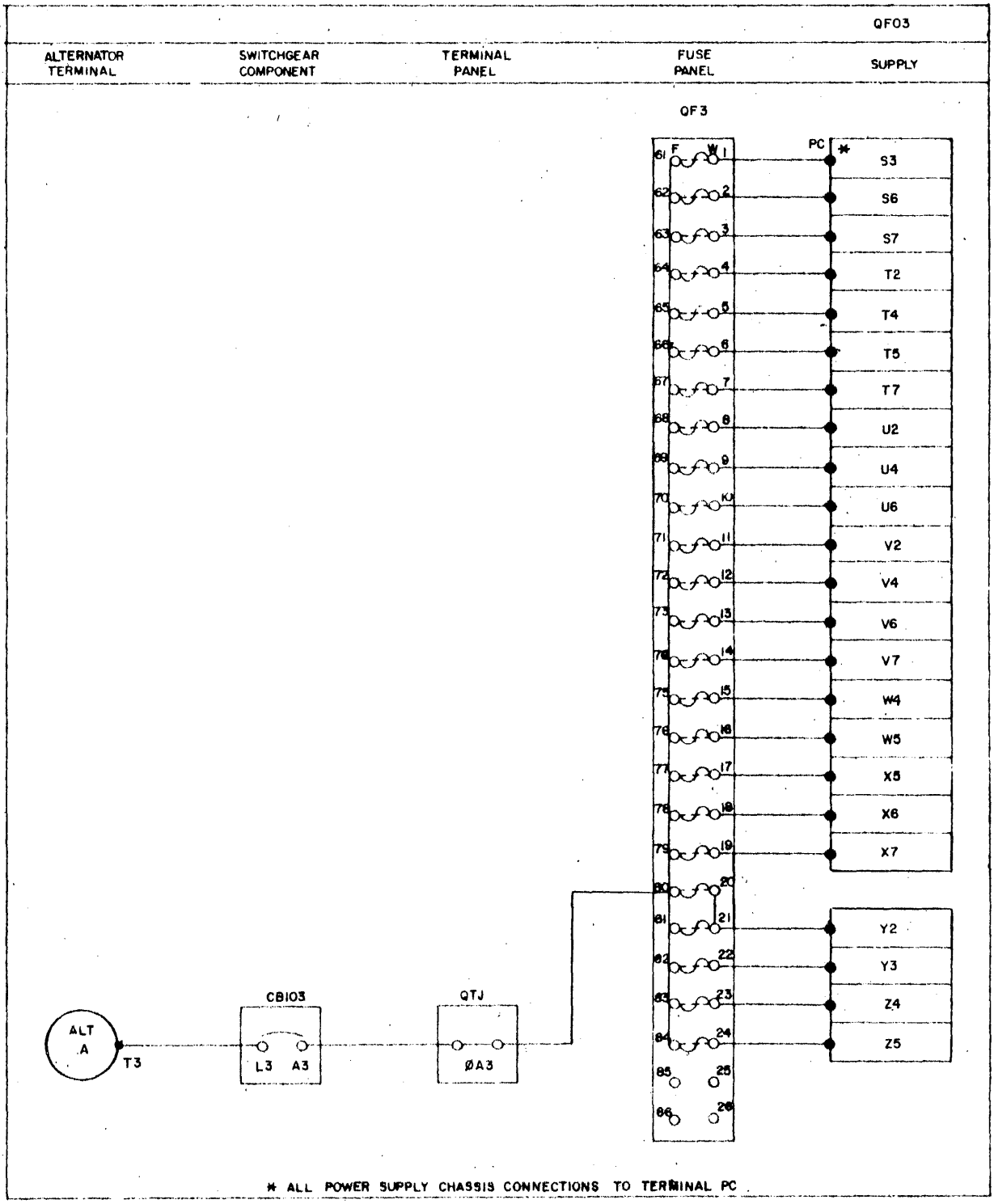


TABLE 8-1 (Cont'd)

POWER SUPPLY PRIMARY CIRCUITS

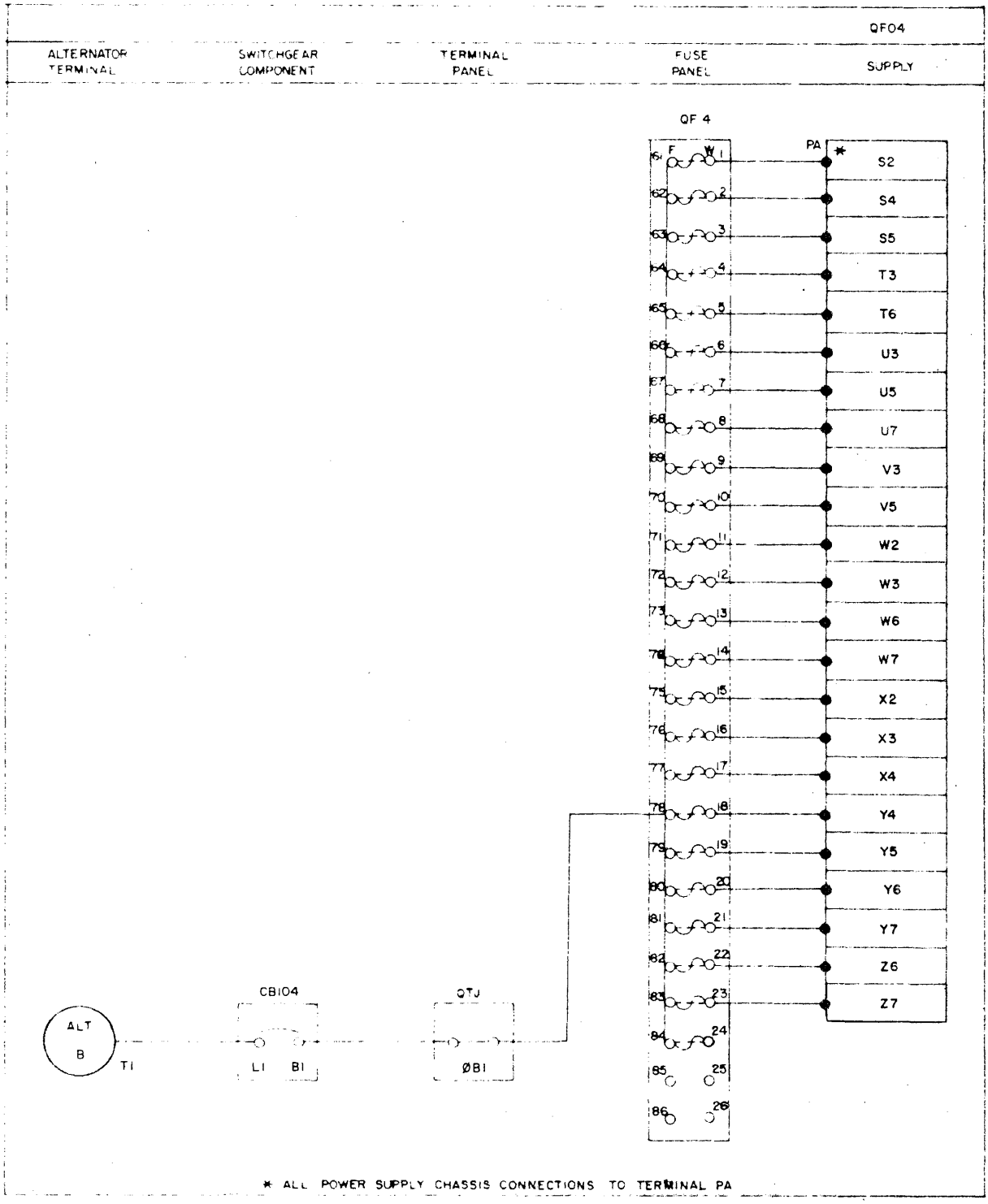


TABLE 8-1 (Cont'd)

POWER SUPPLY PRIMARY CIRCUITS

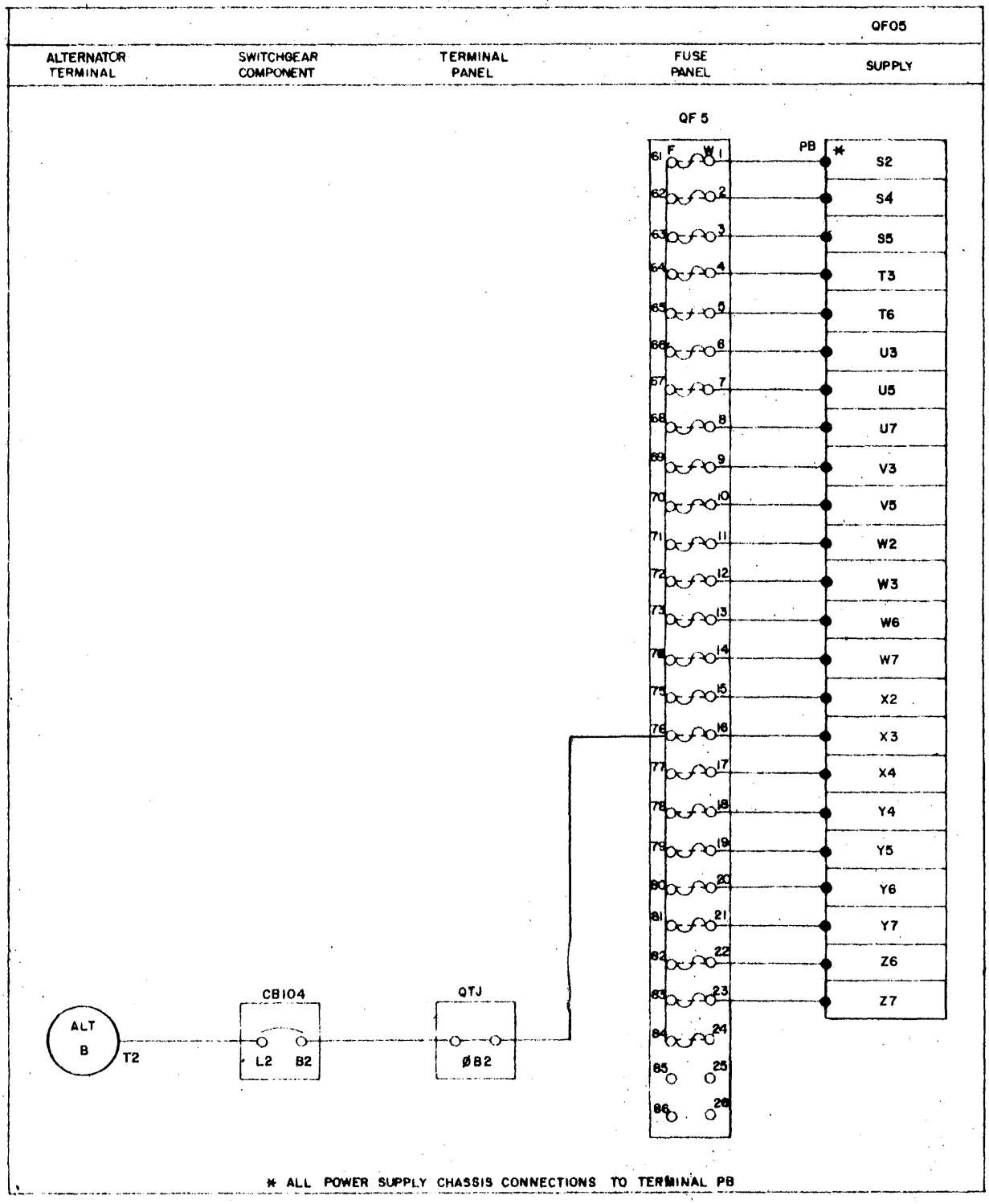


TABLE 8-1 (Cont'd)

POWER SUPPLY PRIMARY CIRCUITS

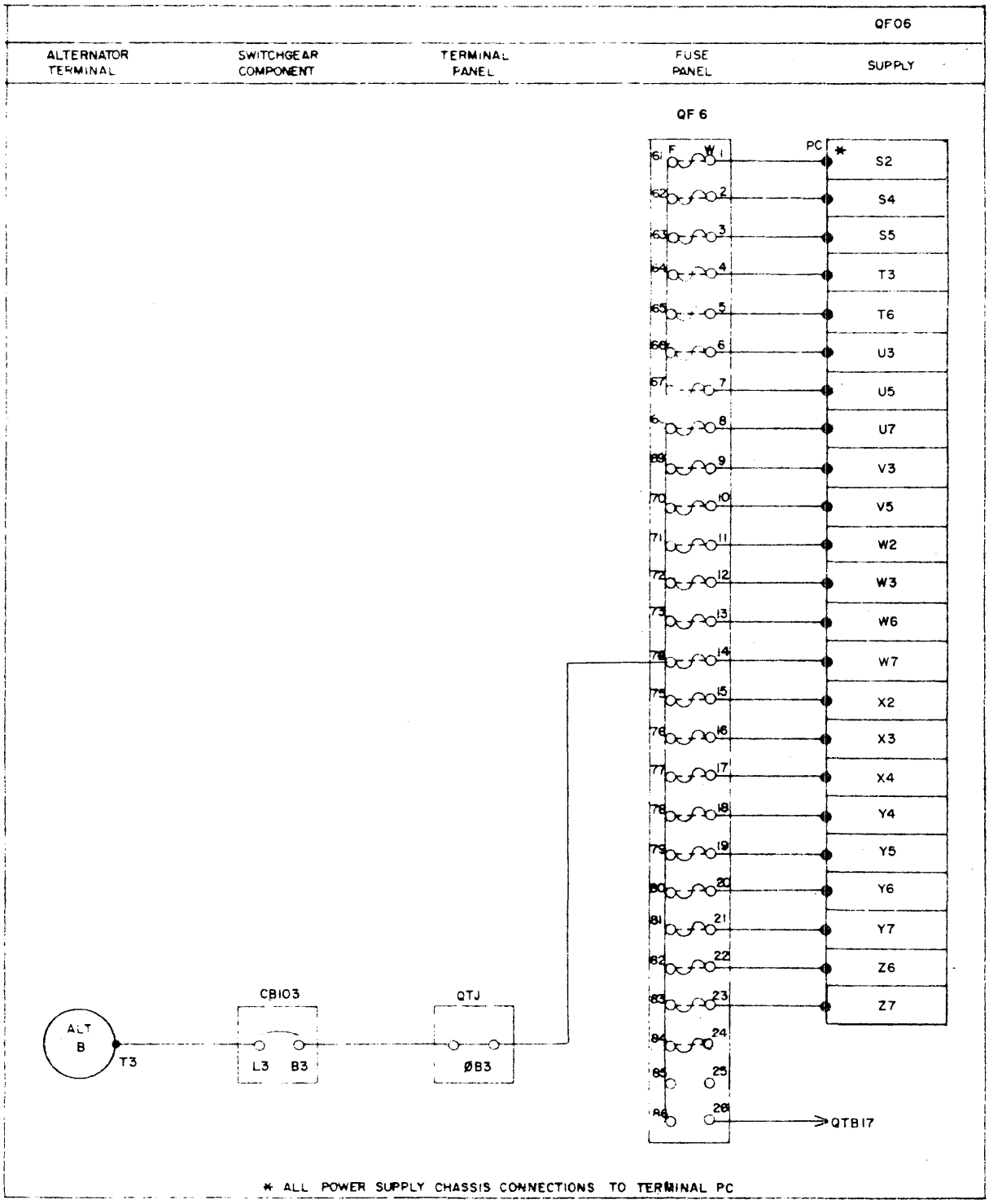
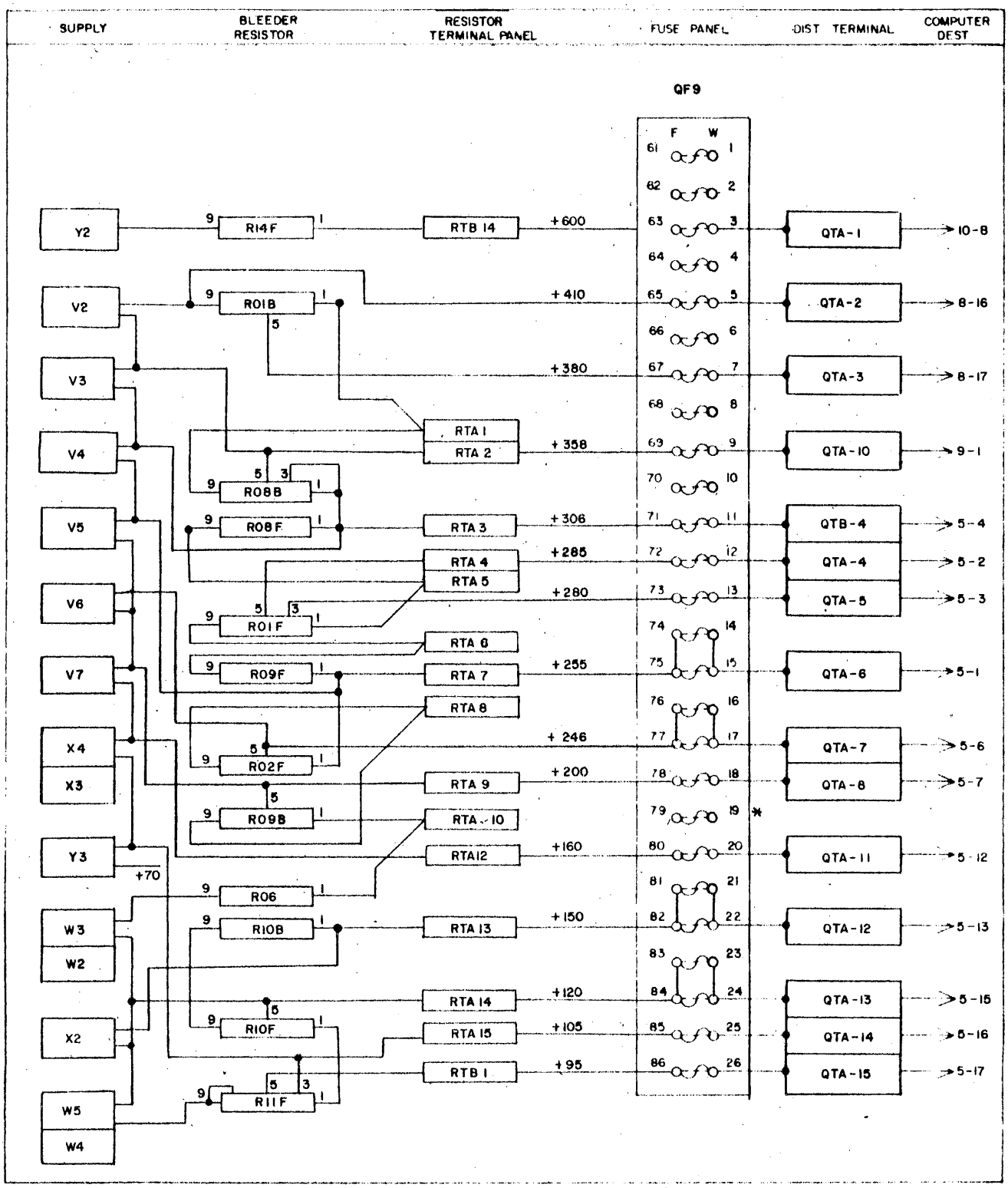


TABLE 8-2

POWER SUPPLY SECONDARY CIRCUITS



* RTA-11 DETAIL SHOWN ON NEXT PAGE

FUSE MAY BE EITHER GRASSHOPPER OR CARTRIDGE

TABLE 8-2 (Con't) Supp. A

POWER SUPPLY SECONDARY CIRCUITS

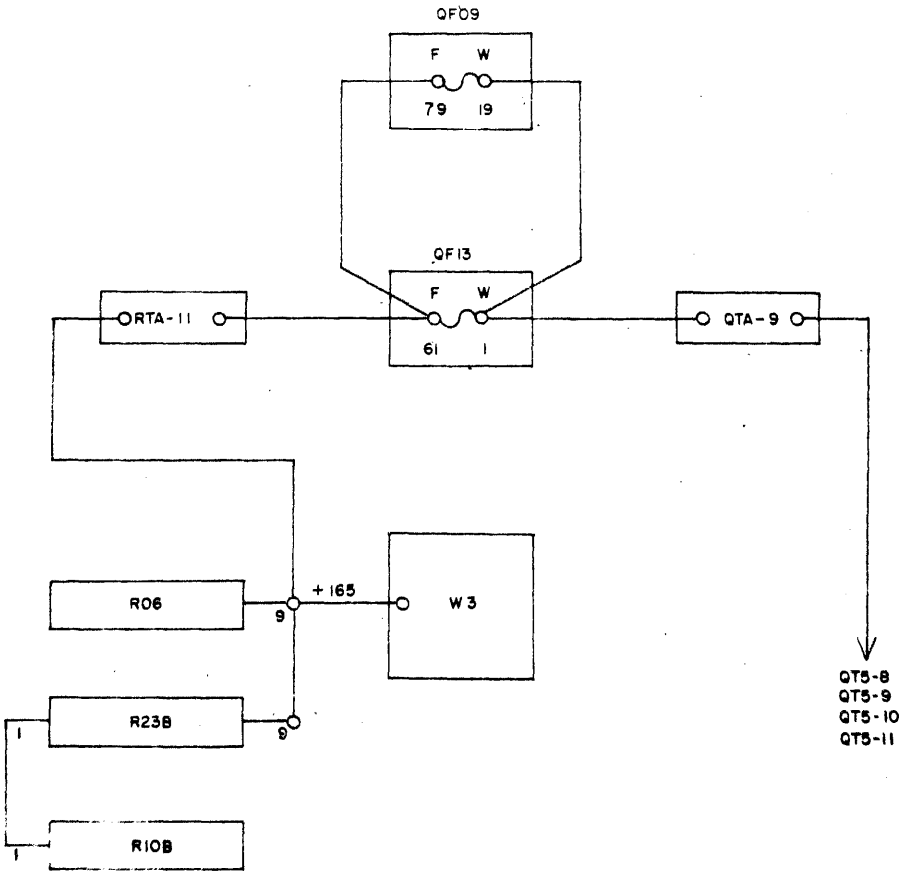
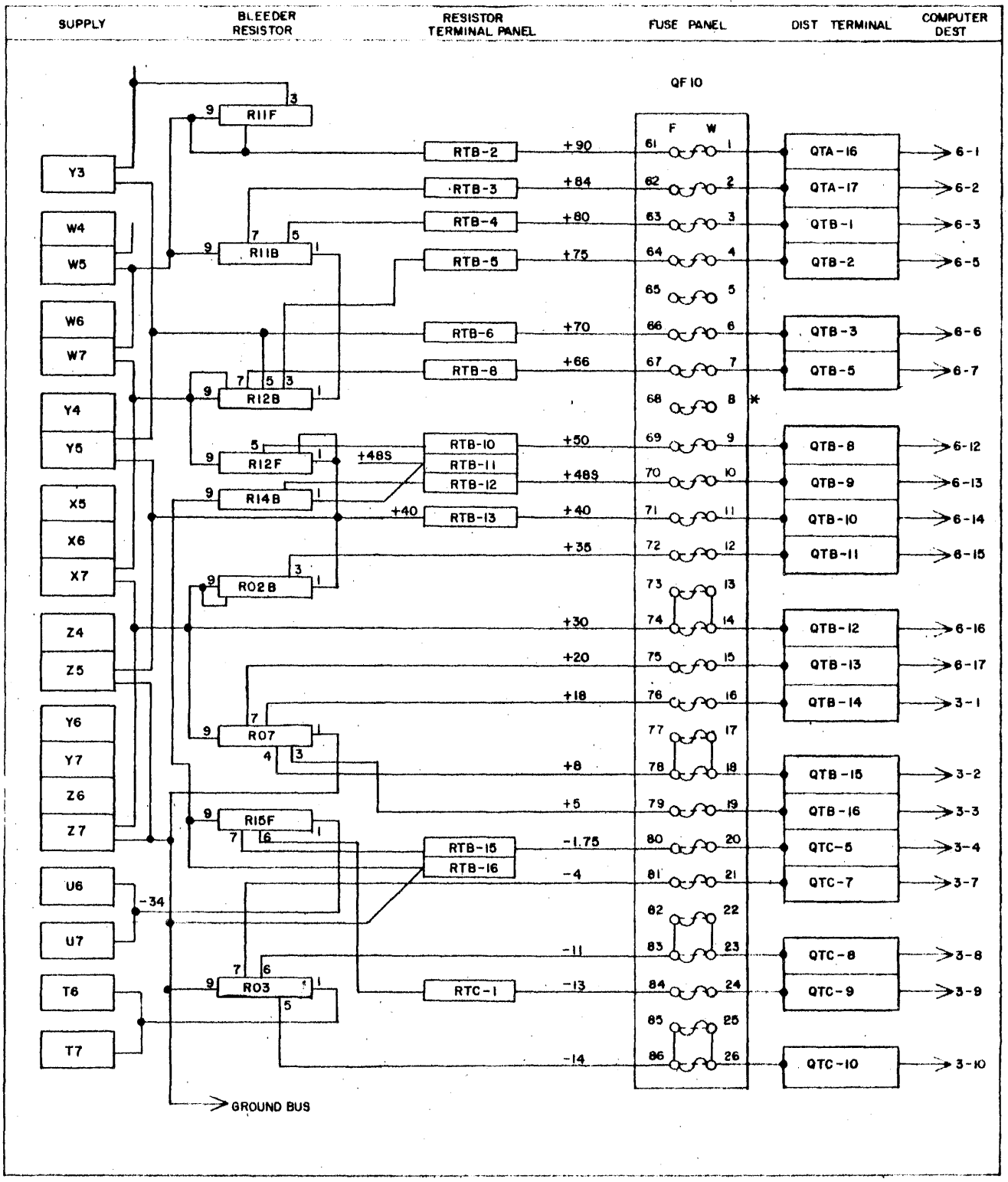


TABLE 8-2 (Cont'd)

POWER SUPPLY SECONDARY CIRCUITS



* RTB-9 DETAIL SHOWN ON NEXT PAGE

FUSE MAY BE EITHER GRASSHOPPER OR CARTRIDGE

TABLE 3-2 Supp. B

POWER SUPPLY SECONDARY CIRCUITS

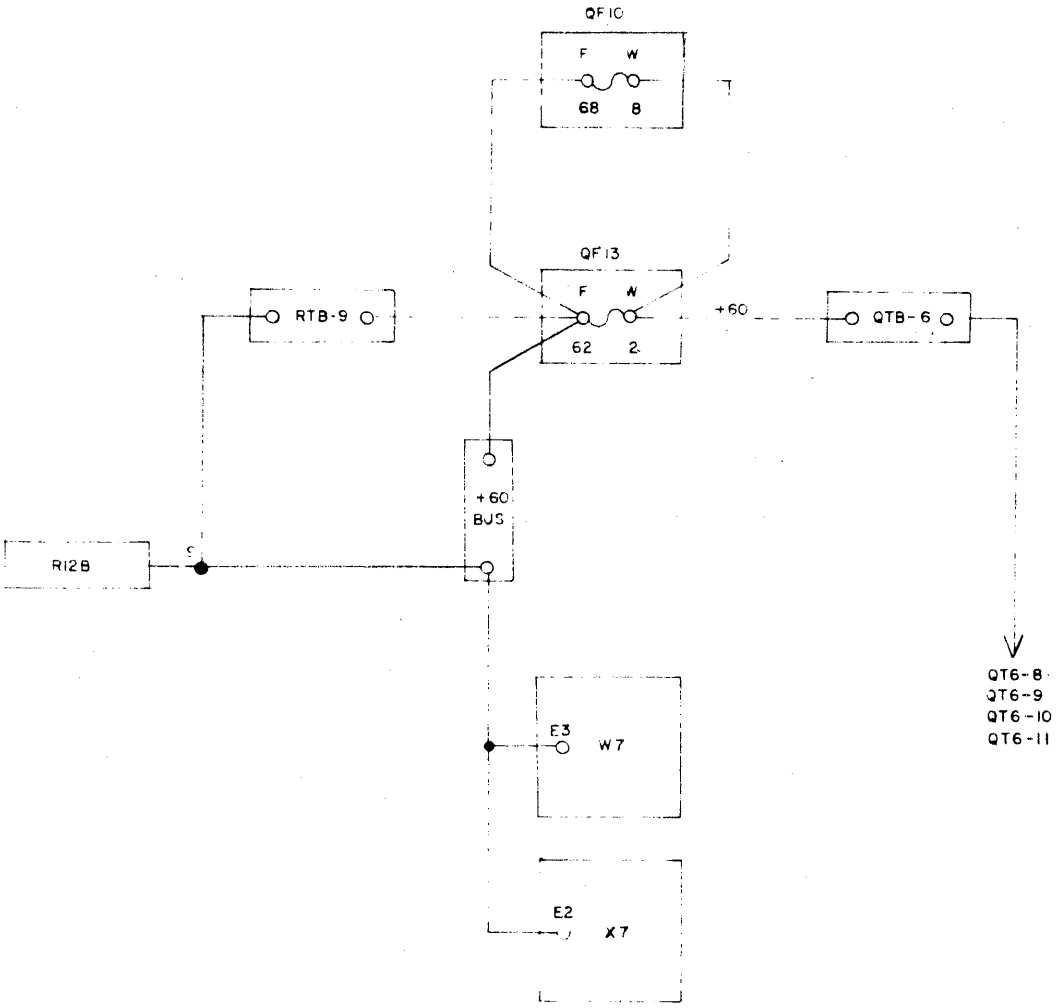


TABLE 8-2 (Con't)

POWER SUPPLY SECONDARY CIRCUITS

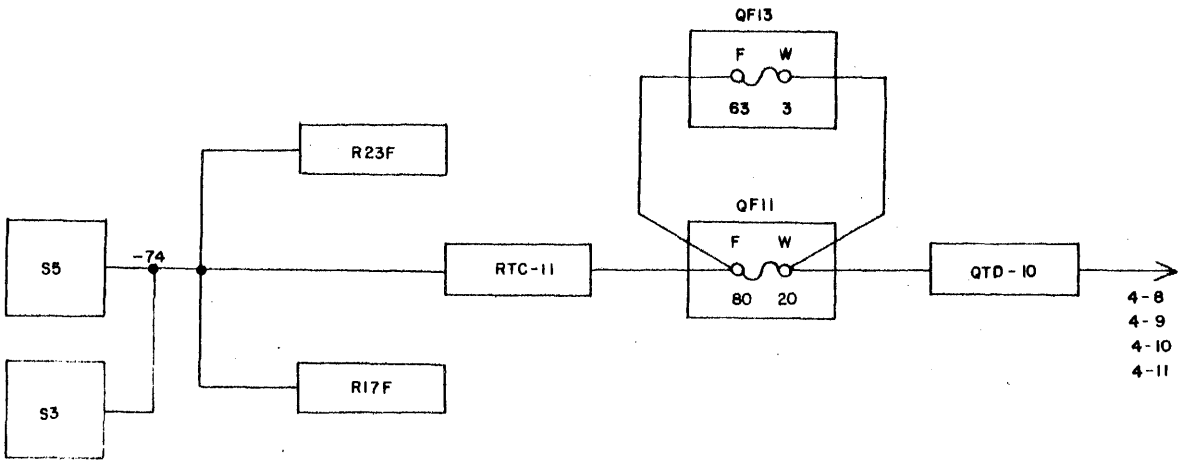
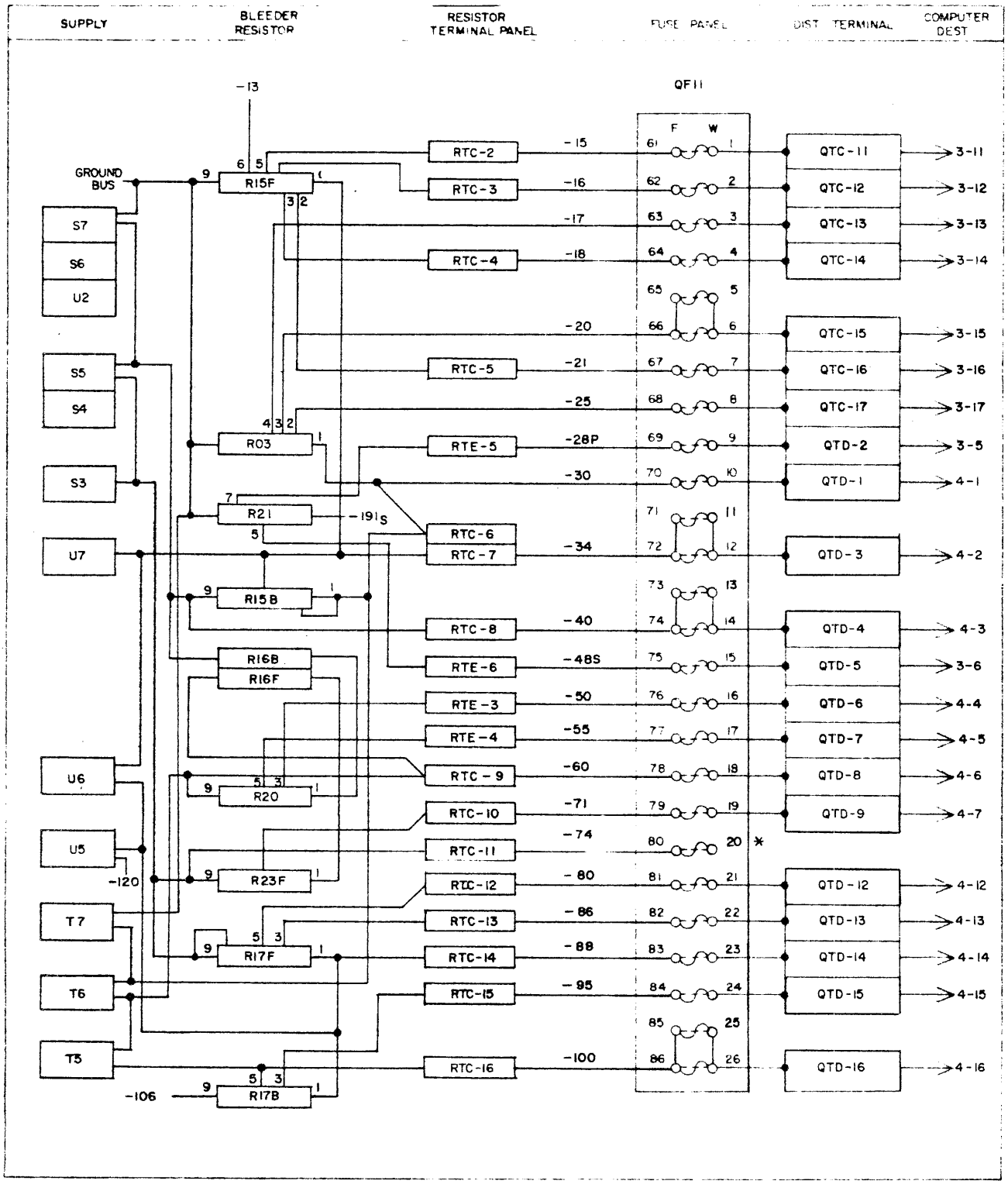


TABLE 8-2 (Cont'd)

POWER SUPPLY SECONDARY CIRCUITS

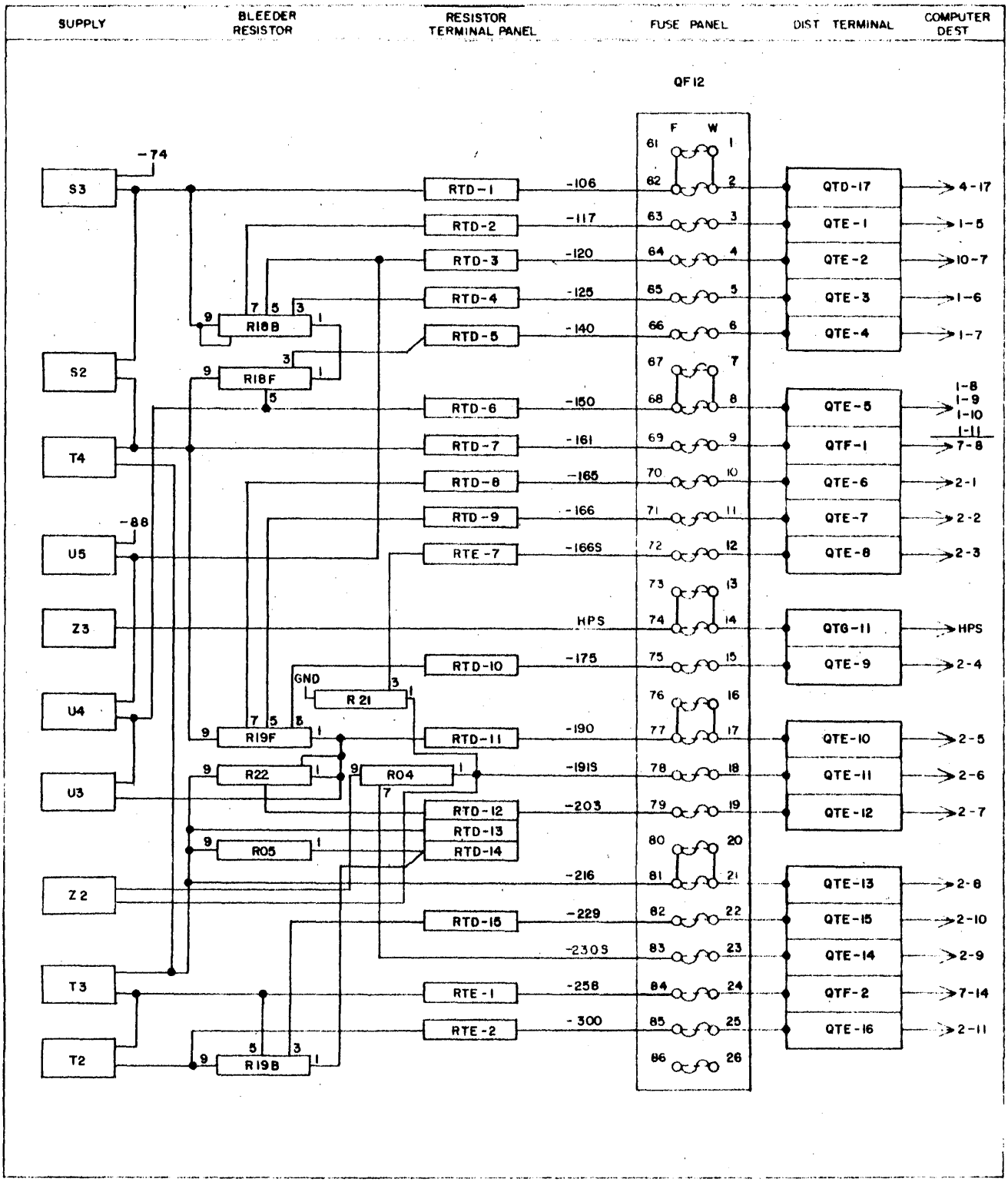


* RTC-11 DETAIL SHOWN ON NEXT PAGE

FUSE MAY BE EITHER GRASSHOPPER OR CARTRIDGE

TABLE 8-2 (Cont'd)

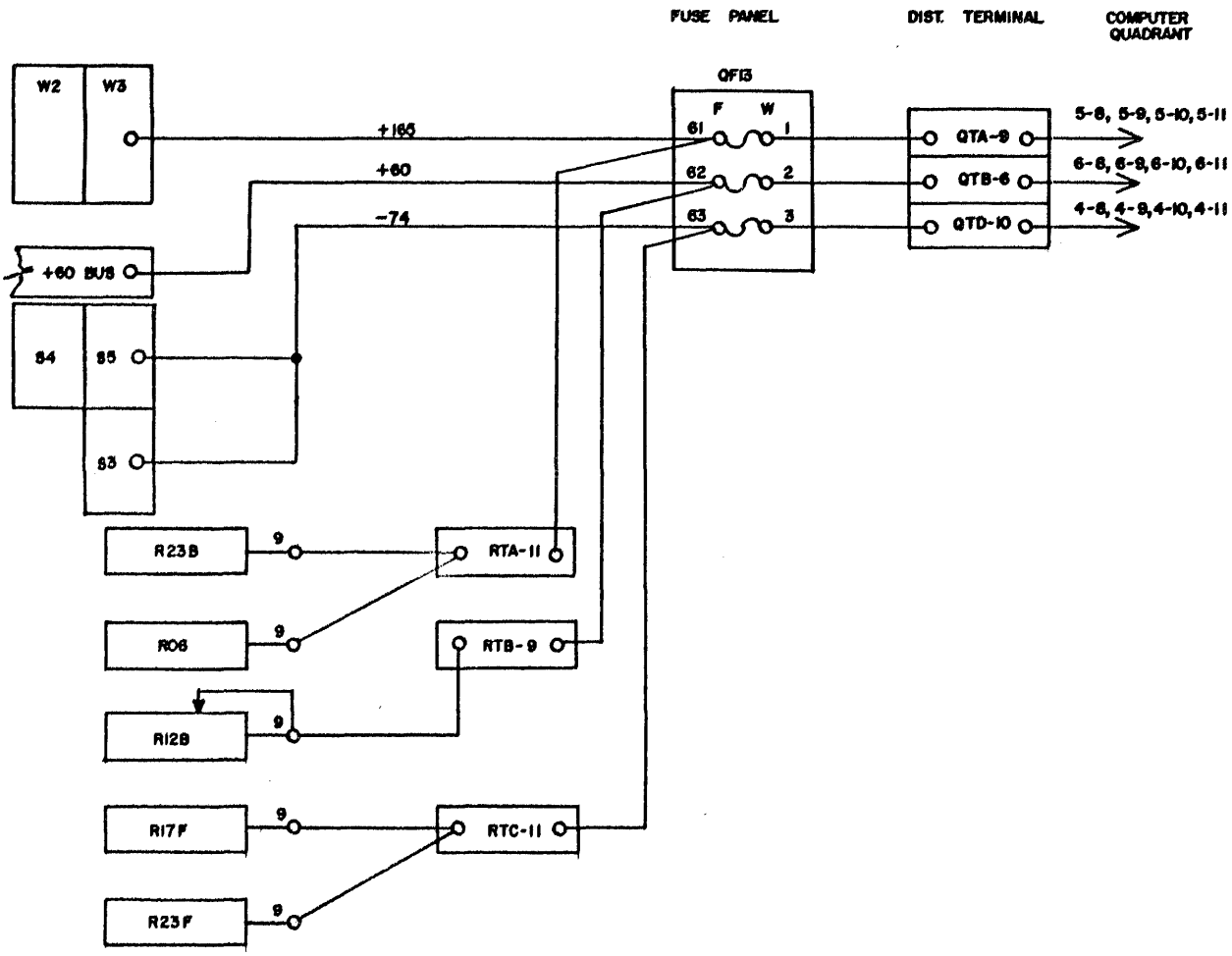
POWER SUPPLY SECONDARY CIRCUITS



FUSE MAY BE EITHER GRASSHOPPER OR CARTRIDGE

TABLE 8-2 (Con't)

POWER SUPPLY SECONDARY CIRCUITS



(Continued from Page 238)

With an input voltage range of 195-255 volts, the output voltage range may be stabilized at any point between 220 and 240 volts at a rated output of 0-120.0 amperes, 27.4 kva. The correction speed computed on a basis of input voltage range and regulator speed, will be at about 0.10 seconds per volt, with waveform distortion zero. The output voltage is adjustable by means of screwdriver slotted shaft on the front panel. A cover on this control discourages tampering or accidental changes. A sensitivity control is similarly provided. A voltmeter which reads output volts is provided on the front panel. Complete circuit protection for control and power circuits is provided.

(1) THEORY OF OPERATION. - The basic purpose of any voltage regulator is to maintain a constant output voltage regardless of line or load changes. In order to accomplish this, there must be some means of constantly monitoring the output of the regulator so that the slightest change, which may tend to become accumulative, will be detected; the detector causing some functional part to increase or decrease the output to compensate for the variation presenting itself, and thus maintain the preset value.

To accomplish their purpose the Stabiline regulators used in the Univac II Switchgear assembly contain a voltage-sensitive bridge, a thyratron control circuit, a motor-driven variable transformer and a buck-boost fixed-ratio transformer.

As seen in Figure 8-31, Simplified Schematic Diagram Stabiline Type EM, the basic elements of the Control Circuit are a voltage-sensitive bridge and a thyratron control circuit, with the bridge connected across the output of the regulator in order to sample the output. When the voltage output varies from the preset value, an unbalance will occur across the bridge -- the unbalance being the detected error voltage. The error voltage is fed to the thyratron control circuit, and, depending upon the direction of the error voltage from

the set output voltage of the regulator, one or the other of two thyratron tubes in the control circuit will permit current to flow through the winding of an associated control relay. The relay controls the operation of a motor which is mechanically linked to the variable transformer.

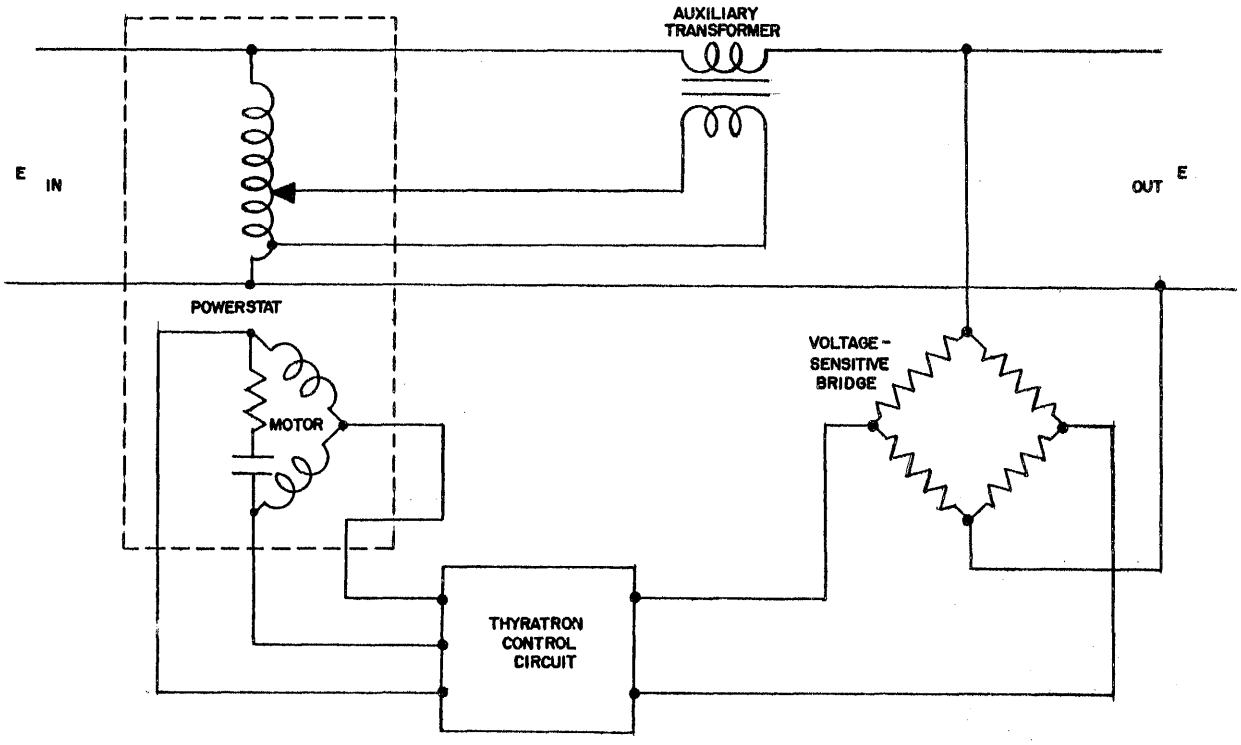


Figure 8-31. Simplified Schematic - Stabiline Type EM

The Power Circuit consists of the motor-driven variable transformer and an auxiliary transformer. When the relay of the control circuit is actuated, the circuit of one of the windings of the motor is completed, thus causing the motor to rotate in a direction which depends upon the winding that is impulsed. As the motor rotates, the brush element of the variable transformer rotates in synchronism. The variable transformer is tapped so that a voltage of the correct polarity and magnitude is delivered to the primary of the auxiliary

transformer. The primary of this fixed-ratio transformer, receiving a voltage of a certain magnitude and direction of current, causes the secondary to repulse or aid (buck or boost) the line voltage, to restore the output to the preset value.

A Wiring and complete Schematic diagram of the Stabiline unit is given on Drawing 177177, together with part specifications.

(2) ADJUSTMENT. - The ON-OFF toggle switch on the panel of the Stabiline unit controls the control circuit (including pilot lamp) only, the power circuit is controlled and protected by circuit-breakers separately installed. Approximately thirty seconds following the closing of the control circuit (power circuit also on) the raise or lower thyratron tube will conduct causing the regulator to operate if necessary.

The SENSITIVITY control on the right front panel determines the value of the voltage departure from the nominal output before the regulator begins to compensate. Increasing sensitivity (clockwise) causes the regulator to correct for progressively smaller voltage excursions. Remove the protective cap in order to make screwdriver adjustments to this control.

Initially, the control sensitivity should be increased to the point at which the regulator continuously hunts, the motor operating in either direction continuously with frequent direction changes. The control should then be turned to the left slightly, to the point where the regulator ceases to hunt.

The OUTPUT VOLTAGE control on the left side of the panel determines the nominal output voltage of the regulator. After removing the protective cover this control may be adjusted to produce the desired output voltage, the voltage being read on the panel meter.

(3) MAINTENANCE AND SERVICE INFORMATION. - Elements requiring occasional replacement are the 2050 thyratron tubes, the BU-1 voltage sensitive element

and the two relays type 41R, specification number 4585, and for this reason these are all plug-in components. Fuses are located in the input line, the brush lead, the control circuit and the motor circuit.

If a fault occurs which is not corrected by replacement of any of the above-described components, it is desirable to know whether or not the fault is present in the control circuit or motor circuit. In order that this may be determined the following procedure should be performed:

a. Remove the control circuit by unscrewing the hold-in screws located near the top and bottom of the chassis and pulling the unit from the mounting socket.

b. Locate the motor terminal board mounted on the motor mounting plate and remove the three motor connections, making note of each lead for correct replacement.

c. Apply 115 volts a-c from an external source to the common and green leads, and then to the common and red leads of the motor.

d. Under the above circumstances it should be possible to turn the variable transformer through its complete range, changing the output voltage as indicated on the meter as the transformer changes. It should be possible to select the correct output voltage in this manner. This test, if positive, indicates that the motor and power circuit are operating satisfactorily and replacement of the control circuit with a correctly functioning unit should be made.

If the fault appears to be in some other portion of the Stabiline unit, reference to the table of voltage and resistance measurements should be made.

e. MOTOR GENERATOR SET. - The Motor Generator, or Motor Alternator, is of the open, air-cooled type, and consists of a 75 hp motor and two 25 kva, 0.9 power factor, 400 cycle generators. The motor is rated at 440 volts, 3-phase, 60 cycle and is controlled by the motor starter in the Switchgear. The 400 cycle output is controlled by circuit breakers CB103 and CB104. Control of the 400-cycle voltage and excitation for the generators is performed by exiter regulator units in the Switchgear. Figure 8-32 presents, pictorially the back view of the Motor-Generator.

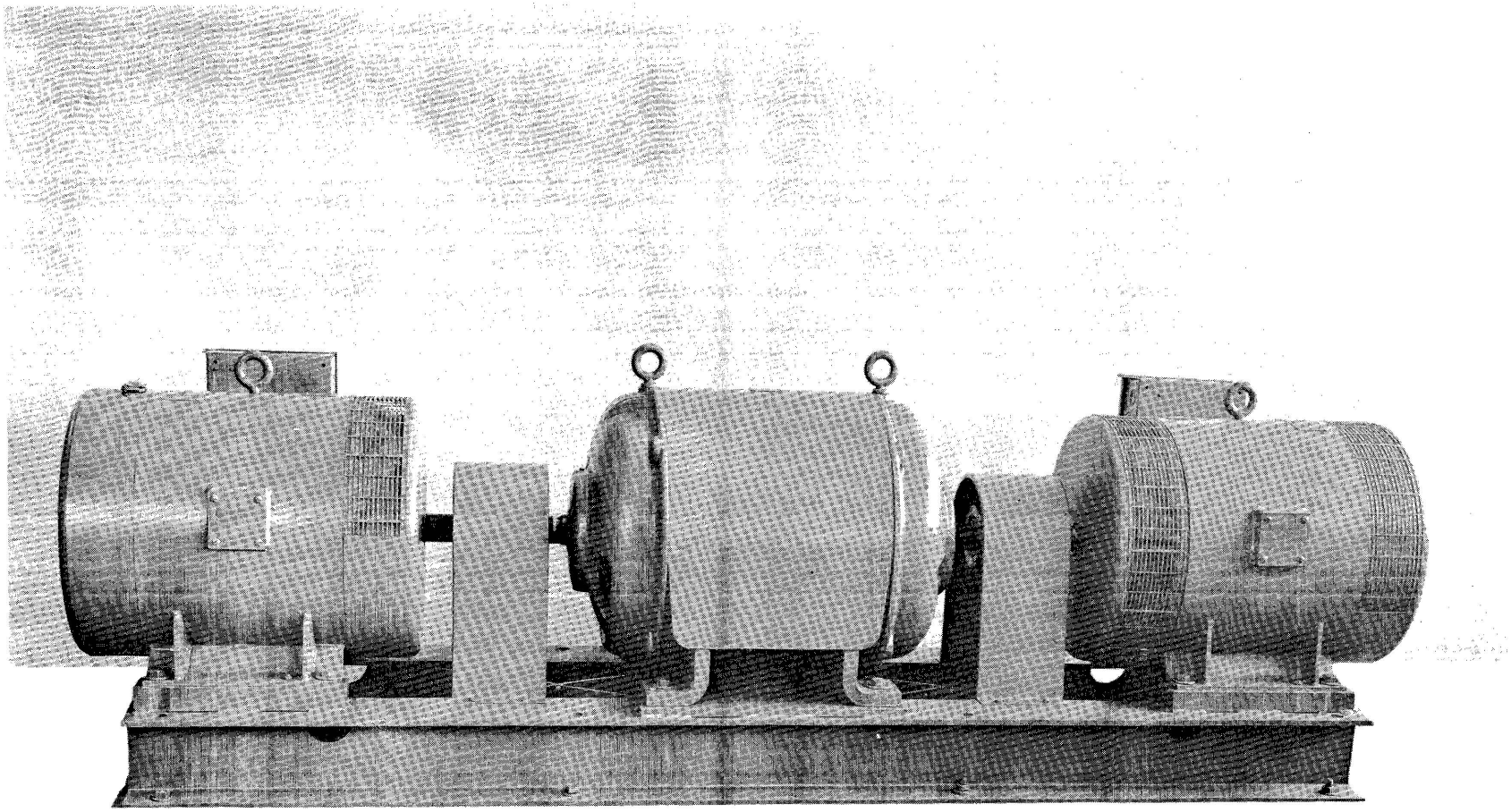


Figure 8-32. Motor Generator Set, Back View

(1) ELECTRICAL CONNECTIONS. - The motor section of the Motor-Generator is connected to 3-phase, 60-cycle, 440V power source, either directly from the 480V line, if such be supplied, or from a step-up transformer in the case of a 208V or 240V supply. Control of power to the motor is supplied by circuit breaker CB106 in the Switchgear.

The output of the Motor-Generator is connected to the Power Supply through DC Circuit Breakers No. 1 and No. 2, or CB103 and CB104. These circuit breakers were discussed in the section describing the Switchgear.

As a safety precaution to protect operating personnel, the frame of the Motor-Generator should be grounded. The ground connections should be made with a conductor of a size large enough to carry adequately any short circuit current in the event the windings become grounded. Do not rely upon the foundation bolts as a ground connection. The ground conductor lead should be fastened to the motor and generator frame at the hold-down bolts with suitable lug-type connectors. Remove the paint from the frame at the point of connection and make certain the hold-down bolts are clean to ensure a good electrical connection. The ground conductor should be connected to a grounding electrode or the plant grounding bus through a low resistance conductor.

(2) MAINTENANCE. - Performing periodic preventive maintenance cannot be overemphasized as a major contributing factor to dependable, continuous

operation of the Motor-Generator set. As an aid to systematic maintenance it is desirable to keep simple records of all maintenance procedures. These records as a log on the equipment, serve as a guide for proper maintenance, and aid in determining the spare parts inventory. The frequency of inspection, in general, is determined by the operating conditions. The fundamental principle of preventive maintenance is -- keep apparatus clean and dry.

(a) MOTOR. - Squirrel cage type motors are rugged and in general, give little trouble. The motor should run freely with little noise. If it should fail to start or if it produces a decided hum, it may be that the load has become to great for the motor. In this event check for localized heating, or improper connection. Repairing broken bars or end rings is a job for a competent person; it is recommended that a factory representative be consulted.

Starter troubles can usually be traced to one of the following causes: moisture, overloading, operating single phase, and poor insulation. Some forms of dust are highly conductive and contribute materially to insulation breakdown. The effect of dust on motor temperature through the restriction of ventilation is a principal reason for keeping the windings clean.

The following checks should be made at regular intervals:

1 Windings should be dry and free of dust, oil, and dirt. Winding may be cleaned by suction cleaners or wiping. Nozzles on suction type cleaners should be non-metallic. Gummy deposits should be removed by using carbon tetrachloride. Do not use flammable solvents.

CAUTION

CARBON TETRACHLORIDE IS TOXIC AND SHOULD BE USED WITH CAUTION.

2 Terminal connections, assembly screws, bolts and nuts should be tight. They may loosen and permit the motor to vibrate.

3 Insulation resistance of the motor should be checked periodically to determine if there has been any deterioration. If wide variation in resistance measurements made at regular intervals exist, the cause should be determined.

4 The air chambers within the motors must not become clogged with foreign material which would restrict ventilation.

5 The ball bearings are properly lubricated when shipped from the factory. Further lubrication may follow the routine that is standard practice at the installation, though it is recommended that the bearings be checked every two or three months.

When adding grease use a product that conforms to the manufacturer's specifications. Remove plug from the filling hole. With motor at rest or running force grease into filling hole until the grease appears along the shaft. Replace the plug. Wipe away the excess grease which appeared along the shaft.

With fan-cooled motors grease the end opposite the fan first, taking note of the quantity required before grease appears along the shaft. Then, in greasing the fan end, use only about two-thirds of this amount.

(b) GENERATOR. - The instructions which apply to the motor generally apply to the generator. Keep the generator clean and properly lubricated at all times. The generator is equipped with pre-lubricated cartridge type ball bearings which do not have grease filler or grease drain plugs. Under normal conditions they should give extensive service before relubrication is necessary; however, it is desirable to inspect them during the regular maintenance routines.

(c) COUPLINGS. - The following procedure is recommended when lubricating the couplings. Remove both lubricating plugs. When grease is

used the positioning of the lubricating holes is unnecessary. When a fluid lubricant is used it is recommended that the lubricating holes be positioned approximately 45° from the vertical to prevent loss of lubricant before the correct amount has been applied. Use grease instead of oil if the interval between lubrication exceeds two months. Before replacing lubrication plugs, check that the copper ring gaskets are in position and undamaged. Tighten the plugs.

9. COOLING

a. GENERAL. - The Central Computer is air-cooled by means of a closed cooling system. The air circulates in a closed loop inside the computer, as shown in cross section Figure 9-1. Two blowers, mounted under the computer floor, draw air from inside the computer through grills in the floor, and force it across heat exchanges mounted at the bottom of each bay. Cool water is forced through the heat exchangers to dissipate the heat.

The cooled air from the heat exchangers passes up across the front of each bay where the heat-prdducing elements are located. The heated air is then drawn over the top of each bay and into the hood, down through the roof sheets and back to the blowers.

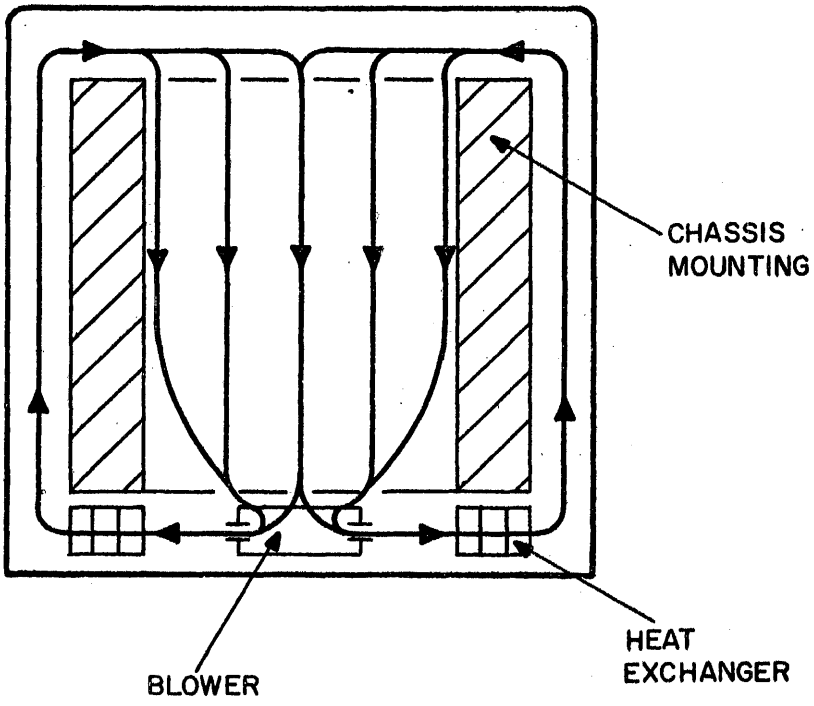


Figure 9-1. Univac II Closed Air Cooling System

The Central Computer, Power System and sixteen Uniservos dissipate about 115 kilowatts of power and require approximately 35 tons of refrigeration. This system requires approximately 158 gallons of 59° F water per minute with an 80-foot head loss. The recommended maximum pressure is 45 psi, with 50 psi the absolute maximum. The layout of the chilled water system is shown in planning drawing XG125294.

Because condensation does form on the heat exchangers a condensate drain is provided on the water cooled sections of the equipment. Air conditioning the area in which the computer is located is not normally necessary; however, it is often done for the comfort of operating personnel and it minimizes condensation in the units.

The cooling system is provided with a number of checks to determine and regulate its proper operation: 1) A cooling system interlock switch is connected into the main interlock circuit of the power system. This interlock prevents the application of power to any unit unless the cooling equipment is turned on. 2) The mass of the cooling equipment is sufficient to take care of limited demands for cooling, thus it provides modulation on the operation of the large compressor system. 3) The coolant is monitored for flow, temperature and pressure by gages in the intake and outlet of the system.

10. UNIVAC II MAINTENANCE DIAGRAMS

a. GENERAL. - The circuits of the Univac II are represented by the following types of diagrams, all intended for use by the maintenance personnel.

(1) SCHEMATIC DIAGRAMS. - A Univac II schematic diagram is the electrical representation of a single unit chassis. The schematic diagrams are intended to serve as a "reference library" for the maintenance technician, providing detailed electrical information concerning the chassis of the computer.

The schematic diagram is laid out about the schematic symbol for its jack, which is shown in Figure 10-1. All d-c voltages supplied to the chassis appear on terminals indicated on the lowest or shortest leg on the jack symbol. The terminals which receive "input" signals appear on the center leg of the jack. The terminals on which the output signals appear are located on the upper leg. Thus the pattern of signal movement across the schematic is from bottom to top, and generally from left to right. The Univac II schematic diagrams use the standard schematic symbols.

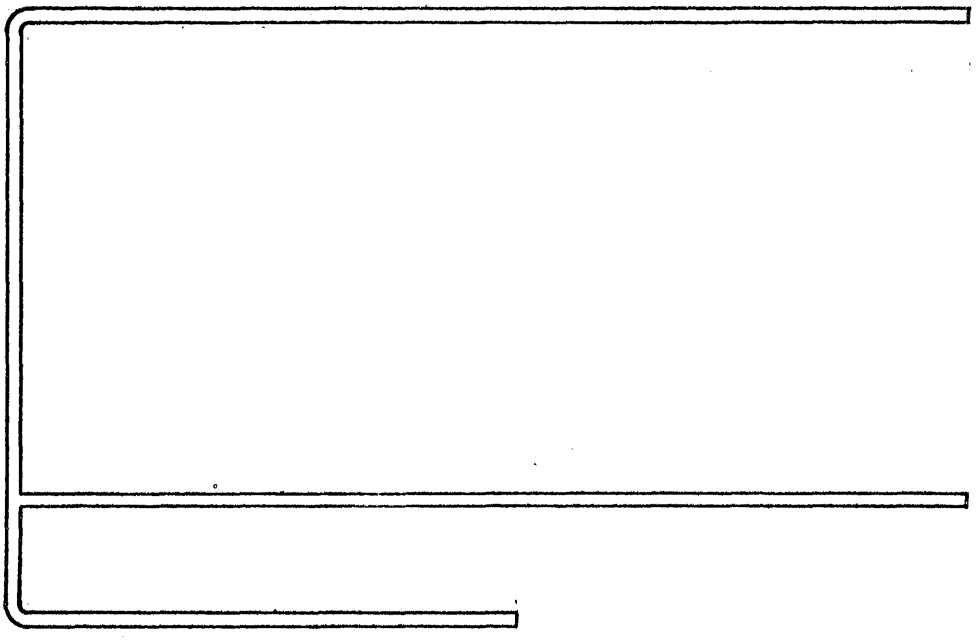


Figure 10-1. Basic Schematic Diagram Format

(2) LAYOUT DIAGRAMS. - A Univac II layout diagram is the physical representation of a unit chassis. The diagram shows the physical placement and connections of each component of the chassis. A parts list for the chassis is supplied on the diagram. The signals appearing on the utilized terminals are listed, facilitating signal tracing through the layout diagram. These diagrams are used as a guide during the replacement of chassis components.

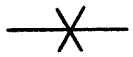
(3) CIRCUIT DIAGRAMS. - A Univac II circuit diagram provides electrical information concerning a functional circuit of the computer. Each functional circuit is usually distributed among several unit chassis and comprises most of the circuitry of those chassis.

The logical properties of the circuits are inherently included in the circuit diagram, but are usually obscured by the maze of electrical details.

The Univac II circuit diagrams divide the computer into approximately 73 functional circuits, showing all the electrical details of each circuit as well as the important physical details. Several of the larger circuits are represented on two or more diagrams; several of the small circuits are combined on one diagram.

The following electrical and physical information is provided on the circuit diagrams:

1. The electrical circuit, drawn with shorthand symbols which have direct schematic equivalents.
2. The type number of each vacuum tube.
3. The chassis divisions and the terminal connections between chassis. The chassis divisions are represented by dashed lines on the diagram; the chassis designation appears several times within each area bounded by dashed lines. The terminal connections are identified near the point where a signal enters or leaves a chassis.

4. All signals which enter or leave a functional circuit are named according to their logical function. Some of the flip-flops, delay-flops, etc., are also given logical names.
5. The source or destination of each signal which enters or leaves a functional circuit is provided.
6. All test terminals are indicated. The normal voltage levels at the test terminals are provided.
7. A-C coupling is indicated by the symbol 

In order to make the Univac II circuit diagrams consistent, certain basic rules were followed during their preparation. These rules are listed below:

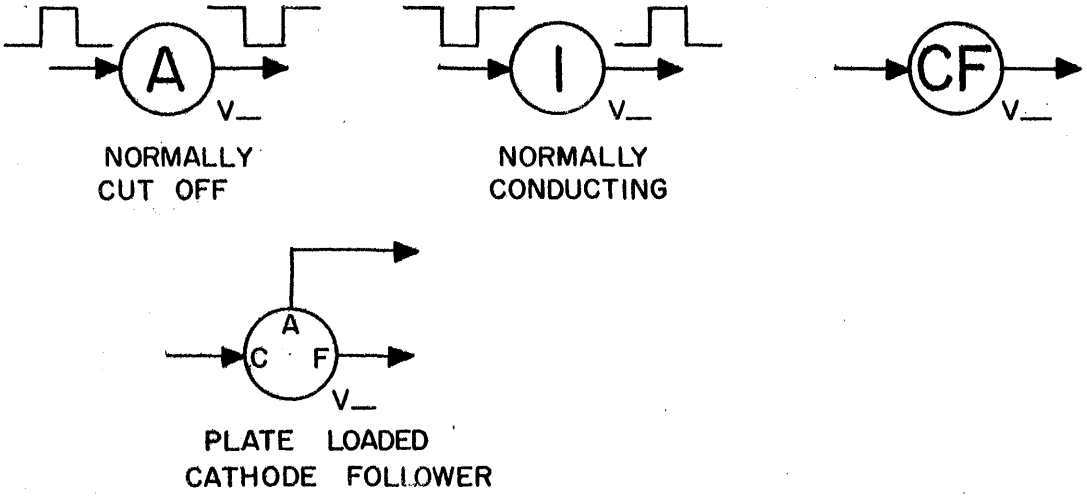
1. A negative pulse applied to its "set" input sets a flip-flop; a negative pulse applied to its "reset" input resets a flip-flop.
2. The set output of a flip-flop is at its most positive potential when the flip-flop is set, at its most negative potential when the flip-flop is reset. The reset output is at its most positive potential when the flip-flop is reset, at its most negative potential when the flip-flop is set.
3. An amplifier is a normally cut-off vacuum tube; an inverter is a normally-conducting vacuum tube; however, all d-c coupled stages are amplifiers.
4. A crystal gate is negative unless otherwise indicated. Negative signals alert a negative gate but inhibit a positive one. Positive signals inhibit a negative gate but alert a positive one. The output from a negative gate is a negative-going signal, the output from a positive gate is a positive-going signal.
5. A 7AK7 tube gate requires positive input signals. The output is negative-going. Some 7AK7 gates have transformer outputs; in this case, both positive-going and negative-going outputs are available.

6. A cathode-follower gate requires negative input signals and provides a negative output signal.

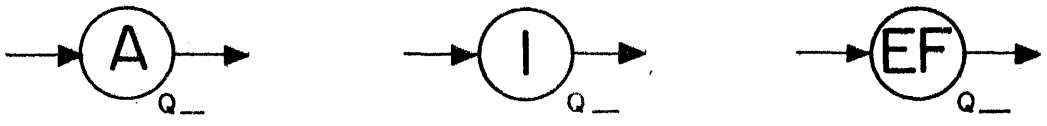
(4) LOGICAL DIAGRAMS. - A Univac II logical diagram describes the logical properties of a functional circuit without regard to physical boundaries. This type of diagram presents the "decision elements" only and uses block symbols to represent those elements. The logical diagrams accompany the text of the Theory of Operation manual, PX 695. These diagrams are intended as an aid to understanding the computer rather than for troubleshooting purposes.

b. LOGICAL SYMBOLS. - The following pages list the shorthand symbols used in the preparation of the circuit diagrams.

1. Vacuum Tubes.



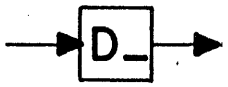
2. Transistors.



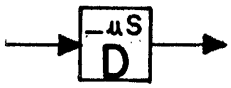
(a) State of conduction same as vacuum tube.

(b) Signal in, signal out depends on type, NPN, PNP.

3. Delays.

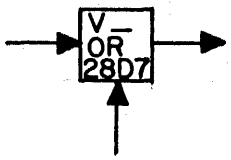


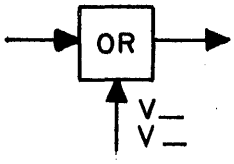
DELAY IN PULSE TIMES

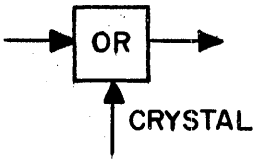


DELAY IN MICROSECONDS

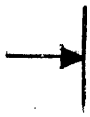
4. Buffers (OR)







5. Gates (AND)

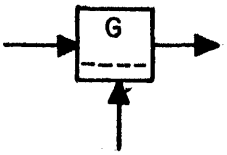


SIGNAL
PERMISSES

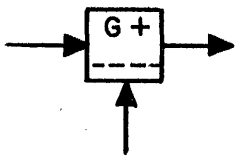
SIGNAL
INHIBITS

a. Crystal

NEGATIVE

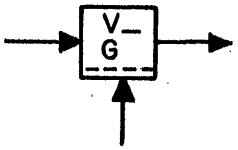


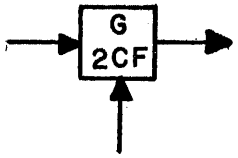
POSITIVE



b. Tube

7AK7





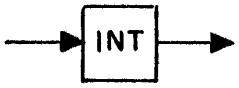
6. Shaping Circuits

a. Differentiators

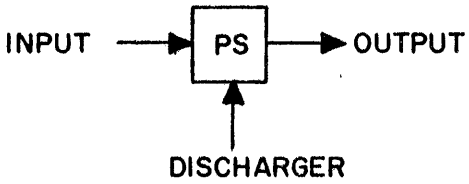
LEADING EDGE

TRAILING EDGE

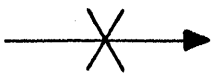
b. Integrator



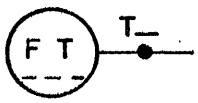
c. Pulse Stretcher

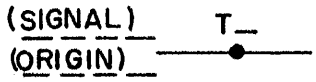


d. A.C. Coupling

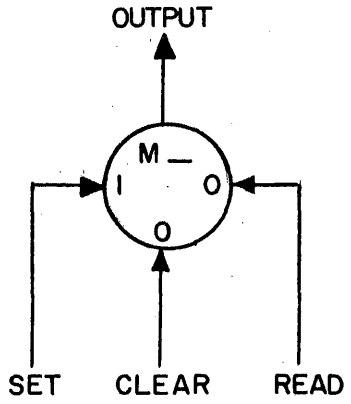


7. Signals Into Chassis.



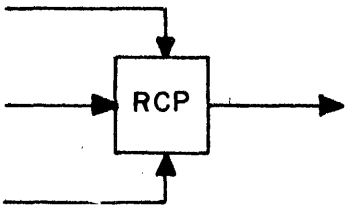


8. Switching Cores.

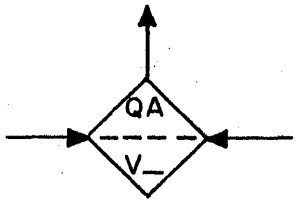


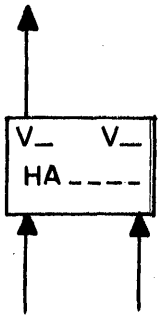
M_1
M_2
M_3
M_4
N_5

9. Resistor Comparator.

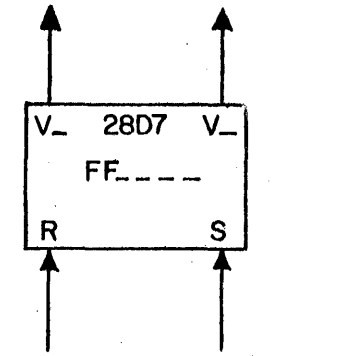


10. Adders.

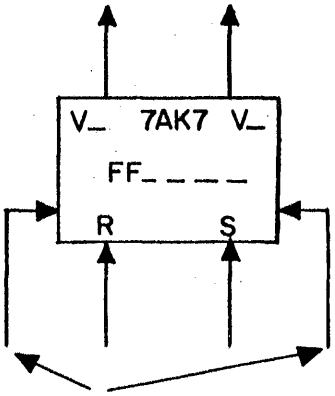




11. Flip Flops.



NEG. IN. GIVES POSITIVE OUT. ON SAME SIDE



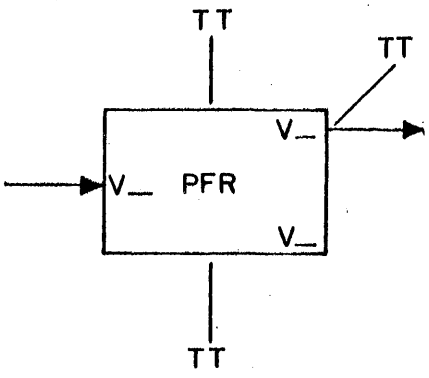
SCREEN GRIDS USED FOR JAMMING

NOTE

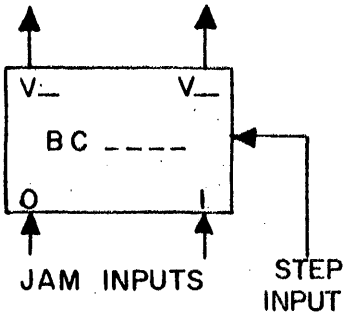
Negative in on set side sets,

positive in on set side resets

12. Pulse Former.



13. Binary Counter.

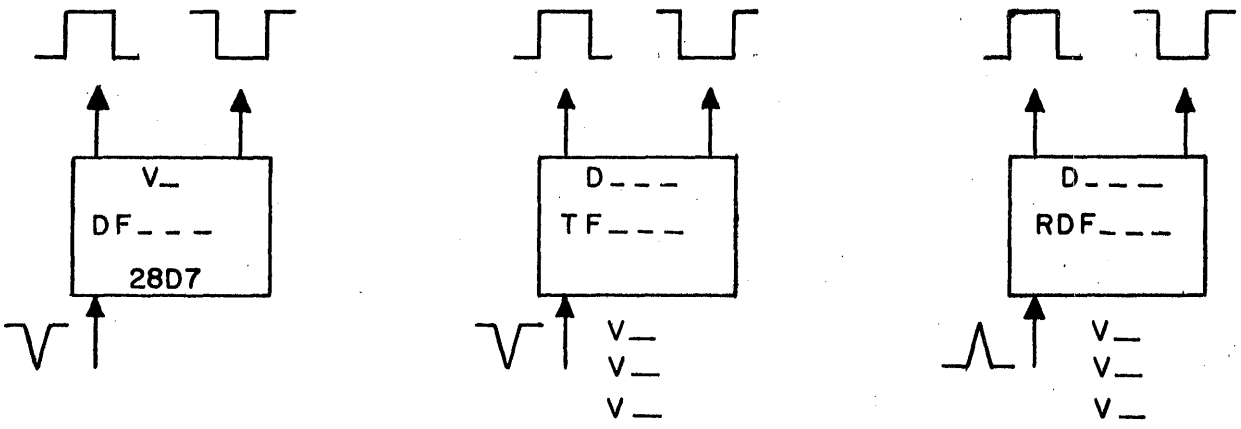


NEG. IN. GIVES POSITIVE OUT. ON SAME SIDE.

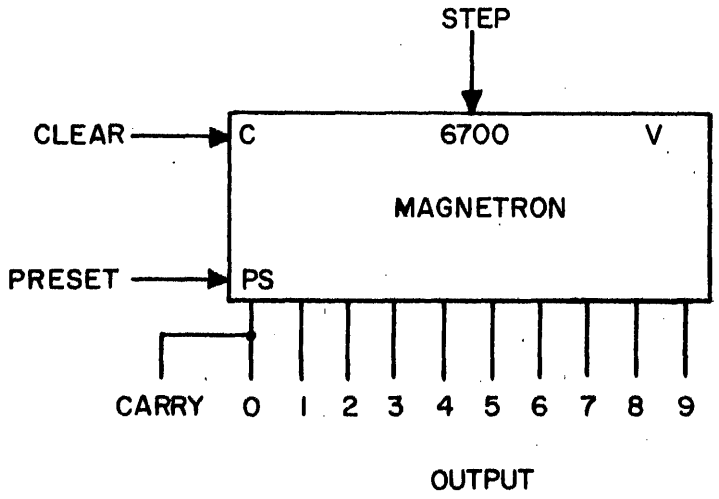
NEG. IN ON 0 SIDE JAMS TO 0

POS. IN ON 0 SIDE JAMS TO 1

14. Delay Flops.

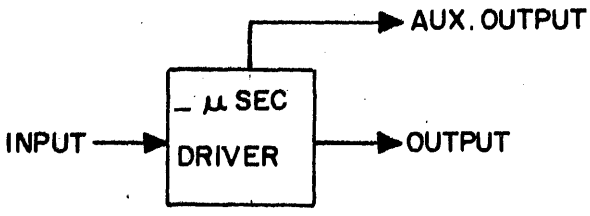


15. Magnetron.

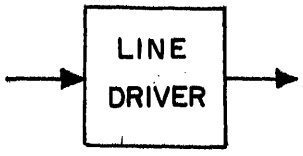


16. Driver.

a. 1 or 2 microsecond.



b. Line Driver



APPENDIX A

SUPPLEMENTAL MAINTENANCE INFORMATION

UNIVAC II

CHASSIS LOCATION CROSS INDEX

1. GENERAL. - This appendix provides a cross index for the Univac II chassis by physical placement about the computer; by schematic drawing; and by the circuit drawings on which elements of the chassis appear.

The data arrangement on each page indicates the physical placement of the unit chassis within each bay. The bay designation appears at the head of each page, the section designation to the left, and the chassis number is in the square within each unit position.

Each chassis position provides two areas of reference, one lists the number of the schematic diagram for the chassis; the other lists all of the logical circuit diagrams on which elements of the chassis appear.

Exceptions to the preceding paragraphs occur in the pages which reference the printed-circuit chassis. Here, only a bay-section appears on a page. Also, the abbreviations for the descriptive name assigned the chassis type appears with the schematic number, and the type number designation appears in a circle below the chassis location number.

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Bay A

Section X

Schematic	Circuit No.
1 182249	177201
2 182249	177201
3 182251	177280
4 182252	177201
5 182253	177201, 177203
6 182254	177205, 177202
7 182255	177200, 177202, 177206
8 182256	177202, 177203, 177206
9 182257	177202, 177203
10 182258	177202
11 182259	177200, 177202, 177203, 177288
12 182260	177200, 177202, 177203

Section V

Schematic	Circuit No.
1 182237	177201
2 182238	177201, 177280
3 182239	177205, 177202
4 182240	177205, 177202
5 182241	177205, 177206
6 182242	177200, 177202, 177205
7 182243	177200, 177202, 177203
8 182244	177200, 177202,
9 182245	177200, 177202
10 182246	177200, 177202, 177280
11 182247	177200, 177206, 177202, 177203
12 182248	177200, 177203, 177206

Section T

Schematic	Circuit No.
1 182225	177201
2 182225	177201
3 182227	177207, 177288
4 182228	177201
5 182229	177201
6 182230	177207, 177288
7 182231	177202, 177207, 177288
8 182232	177203, 177206, 177288, 177207
9 182233	177207
10 182234	177280, 177288
11 182235	177200, 177203, 177202
12 182236	177200, 177207, 177203

Section X

Schematic	Circuit No.	
1	182285	17228
2	182285	177228
3	182287	177228
4	182288	177237, 177200 177202
5	182289	177267
6	182290	177200, 177203
7	182291	177284
8	182292	177284
9	182293	177284
10	182294	177284
11	188295	177274
12	188296	177274

Section V

Schematic	Circuit No.	
1	182273	177223, 177228
2	182274	177232
3	182275	177232
4	182276	177231, 177232
5	182277	177231
6	182278	177232, 177200 177202, 177203
7	182279	177231, 177232, 177200, 177203
8	182280	177200, 177202, 177283, 177284, 177203
9	182281	177283, 177284
10	182282	177283
11	182283	177283
12	182284	177226

Section T

Schematic	Circuit No.	
1	182261	177222, 177228
2	182262	177230, 177231
3	182263	177229, 177230, 177231
4	182264	177231
5	182265	177229, 177230, 177231
6	182266	177229, 177230, 177231
7	182267	177230, 177231, 177232
8	182268	177208, 177229, 177230, 177231
9	182269	177230, 177231, 177232
10	182270	177229, 177230
11	182271	177229, 177230 177231
12	182272	177229, 177230

Bay B

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Section X

Schematic	Circuit No.
1 182321	177244
2 182322	177268
3 182323	177227
4 182324	177227
5 182325	177227, 177281 177282
6 182302	177216
7 182327	177244
8 182304	177216, 177287
9 182305	177216
10 182306	177216
11 182306	177216
12 182332	177225, 177224

Section V

Schematic	Circuit No.
1 182309	177229, 177230, 177232
2 182310	177230, 177231, 177216
3 182311	177229
4 182312	177229, 177230, 177231
5 182313	177229, 177230
6 182314	177222, 177225 177226
7 182315	177222, 177226
8 Spare	----
9 182317	177223
10 182318	177222
11 182319	177222
12 182320	177223

Section T

Schematic	Circuit No.
1 182297	177216
2 182298	177285, 177288
3 182299	177287, 177288, 177216
4 182300	177287, 177288
5 182301	177216
6 182302	177216
7 Spare	----
8 182304	177216, 177287
9 182305	177216
10 182306	177216
11 182306	177216
12 Spare	----

Bay C

Section X

Schematic	Circuit No.
1	182357	177282
2	182358	177224
3	182359	177224 177282
4	182360	177251
5	182337	177282, 177285
6	182338	177220
7	182339	177220
8	182338	177220
9	182339	177220
10	182337	177282, 177285
11	182343	177220
12	182343	177220

Section V

Schematic	Circuit No.
1	182345	177218
2	182346	177218
3	182347	177218
4	182348	177218
5	182349	177218
6	182350	177219
7	182348	177219
8	182347	177219
9	182353	177220, 177221 177246
10	182354	177219
11	182355	177219
12	182356	177224

Section T

Schematic	Circuit No.
1	182333	177226, 177274
2	182334	177225, 177285
3	182335	177222, 177285
4	182336	177266
5	182337	177282, 177285
6	182338	177221
7	182339	177221
8	182338	177221
9	182339	177221
10	182337	177282, 177285
11	182343	177221
12	182343	177221

Bay D

Section T

Schematic	Circuit No.	
25 (19)	105900 DE	177246
26 (16)	195990 UG	177246, 177251, 177247
27 (19)	105900 DE	177246
28 (16)	195990 UG	177246, 177251, 177247
29 (19)	105900 DE	177246 177247
30 (6)	105668 D(1)	177251
31 (19)	105900 DE	177247
32 (19)	105900 DE	177247
33 (19)	105900 DE	177251
34 (2)	105826 C & P	177251
35 (19)	105900 DE	177251
36 (24)	189060 MO(1A)	177252

Section T

Schematic	Circuit No.	
13 (25)	189061 MO(1B)	177246
14 (1)	188799 MC	177246
15 (25)	189061 MO(1B)	177246
16 (1)	188799 MC	177246
17 (24)	189060 MO(1A)	177247
18 (1)	188799 MC	177247
19 (25)	189061 MO(1B)	177247
20 (1)	188799 MC	177247
21 (25)	189061 MO(1B)	177247 177251
22 (1)	188799 MC	177252
23 (24)	189060 MO(1A)	177251 177252
24 (1)	188799 MC	177252

Section T

Schematic	Circuit No.	
1 (24)	189060 MO	177246
2 (24)	189060 MO(1A)	177246
3 (24)	189060 MO(1A)	177246
4 (24)	189060 MO(1A)	177246
5 (24)	189060 MO(1A)	177246 177247
6 (24)	189060 MO(1A)	177246 177247
7 (24)	189060 MO(1A)	177247
8 (24)	189060 MO(1A)	177247
9 (24)	189060 MO(1A)	177247 177252
10 (24)	189060 MO(1A)	177252
11 (24)	189060 MO(1A)	177252
12 (24)	189060 MO(1A)	177252

Bay E

Section V

Schematic		Circuit No.
25	Spare	
26	Spare	
27	Spare	
28	Spare	
29	Spare	
30 (12)	195939 SEQ	177251
31 (2)	105826 C & P	177251
32 (2)	105826 C & P	177251
33 (13)	188969 FF(4.2K)	177250
34 (16)	195990 UG	177216, 177250
35 (16)	195990 UG	177216, 177247 177250
36 (6)	105668 ODG	177250, 177251

Section V

Schematic		Circuit No.
13	195986 ODG	172246, 177237, 177250, 177252
14	195990	177246, 177247, 177252
15	189012 O-I	177250, 177251
16 (13)	188969 FF(4.2K)	177247, 177251
17 (13)	188969 FF(4.2K)	177250
18 (16)	195990 UG	177239, 177247, 177250
19 (16)	195990 UG	177250
20 (15)	195986 ODG	177250
21 (12)	195939 SEQ	177250
22 (6)	105668 D(1)	177250
23 (6)	105668 D(1)	177250
24 (6)	105668 D(1)	177250

Section V

Schematic		Circuit No.
1 (15)	195986 ODG	177246, 177252
2	195990 UG	177246, 177251 177252
3 (23)	189031 A-I	177250, 177252
4 (30)	106267 CF(2)	177251, 177252
5 (30)	106267 CF(2)	177250, 177252
6 (23)	189031 A-I	177250, 177252
7 (30)	106267 CF(2)	177250, 177252
8 (16)	195990 UG	177250
9 (16)	195990 UG	177250
10 (11)	105886 FF(8,2K)	177250
11 (11)	105886 FF(8.2K)	177250
12 (11)	105886 FF(8.2K)	177250

Bay E

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Bay E

Section X		Section X		Section X	
Schematic	Circuit No.	Schematic	Circuit No.	Schematic	Circuit No.
	Spare		Spare		Spare
	Spare		Spare		Spare
	Spare		Spare		Spare
	Spare		Spare		Spare
	Spare		Spare		Spare
	Spare		Spare		Spare
	Spare		Spare		Spare
	Spare		Spare		Spare
	Spare		Spare		Spare
	Spare		Spare		Spare
	Spare		Spare		Spare
	Spare		Spare		Spare
36 (16)	195990 UG	177240 177244	24 (16)	195990 UG	177240	12 (11)	105886 FF(8.2K)	177280

Section T

Schematic	Circuit No.
25 (5) 188862 LD	177250
26 (5) 188862 LD	177250
27 (27) 196117 L&R DBS	177245
28 (17) 188845 PFR-N	177248
29 (9) 105830 ADL	177248
30 (10) 195993 DL	177248
31 (17) 188845 PFN	177248
32 (9) 105830 ADL	177248
33 (10) 195993 DL	177248
34 (17) 188845 PFR-N	177249
35 (9) 105830 ADL	177249
36 (10) 195993 DL	177249

Section T

Schematic	Circuit No.
13 (5) 188862 LD	177250
14 (5) 188862 LD	177250
15 (5) 188862 LD	177250
16 (8) 188906 SSG	177248
17 (8) 188906 SSG	177248
18 (8) 188906 SSG	177248
19 (8) 188906 SSG	177248
20 (8) 188906 SSG	177248
21 (8) 188906 SSG	177248
22 (8) 188906 SSG	177248
23 (8) 188906 SSG	177249
24 (8) 188906 SSG	177249

Section T

Schematic	Circuit No.
1 (5) 188862 LD	177250
2	
3	rZW & Diverter Cards
4 (20) 189044 DPC(rM)	177248
5 (20) 189044 DPC(rM)	177248
6 (20) 189044 DPC(rM)	177248
7 (20) 189044 DPC(rM)	177248
8 (20) 189044 DPC(rM)	177248
9 (20) 189044 DPC(rM)	177248
10 (20) 189044 DPC(rM)	177248
11 (20) 189044 DPC(rM)	177249
12 (20) 189044 DPC(rM)	177249

Bay M

Section V

Schematic		Circuit No.
25 (5)	188862 LD	177242
26 (5)	188862	177242
27 (21)	189041 MO(2)	177240
28 (21)	189041 MO(2)	177240
29 (11)	105886 FF(8.2K)	177242
30 (11)	105886 FF(8.2K)	177242
31 (15)	195986 ODG	177243
32 (15)	195986 ODG	177243
33 (6)	105668 D(1)	177244
34 (6)	105668 D(1)	177244, 177241
35 (6)	105668 D(1)	177244, 177241
36 (6)	105668 D(1)	177244, 177242, 177241

Section V

Schematic		Circuit No.
13 (5)	188862 LD	177242
14 (4)	105836 DPC (r0)	177243, 177241
15 (4)	105836 DPC(r0)	177243, 177241
16 (4)	105836 DPC(r0)	177243, 177241
17 (4)	105836 DPC(r0)	177243, 177241
18 (4)	105836 DPC(r0)	177243, 177241
19 (4)	105836 DPC(r0)	177243, 177241
20 (4)	105836 DPC(r0)	177243, 177241
21 (4)	105836 DPC(r0)	177243, 177241
22 (4)	105836 DPC(r0)	177243, 177241
23 (4)	105836 DPC(r0)	177243, 177241
24 (4)	105836 DPC(r0)	177243, 177241

Section V

Schematic		Circuit No.
1 (4)	105836	177243, 177241
2	r0 & Diverter Cards	
3		
4 (4)	105836 DPC(r0)	177243, 177241
5 (4)	105836 DPC(r0)	177243, 177241
6 (4)	105836 DPC(r0)	177243, 177241
7 (4)	105836 DPC(r0)	177243, 177241
8 (4)	105836 DPC(r0)	177243, 177241
9 (4)	105836 DPC(r0)	177243, 177241
10 (4)	105836 DPC(r0)	177243, 177241
11 (4)	105836 DPC(r0)	177243, 177241
12 (4)	105836 DPC(r0)	177243, 177241

Bay M

Section X

Schematic		Circuit No.
25 / 6	105668 D(1)	177242
26 / 6	105668 D(1)	177242
27 / 6	105668 D(1)	177242
28 / 2	105826 C & P	177240
29 / 6	105668 D(1)	177244, 177280
30 / 15	195986 ODG	177244
31 / 15	195986 ODG	177242, 177244
32 / 6	105668 D(1)	177240, 177244
33 / 16	195990 UG	177240, 177244
34 / 13	188969 FF(4.2K)	177240, 177244
35 / 16	195990 UG	177240, 177242, 177244
36 / 2	105826 C & P	177244

Section X

Schematic		Circuit No.
13 / 30	106267 CF(2)	177240
14 / 18	189012 O-I	177240
15 / 30	106267 CF(2)	177240, 177242
16 / 18	189012 O-I	177240, 177242
17 / 12	195939 SEQ	177242
18 / 12	195939 SEQ	177235, 177242
19 / 16	195990 UG	177240, 177242
20 / 16	195990 UG	177240, 177242
21 / 12	195939 SEQ	177242, 177244
22 / 13	188969 FF(4.2K)	177244
23 / 21	189041 MO(2)	177244
24 / 1	188799 MC	177244

Section X

Schematic		Circuit No.
1 / 21	189041 MO(2)	177240
2 / 1	188799 MD	177240
3 / 21	189041 MO(2)	177240
4 / 1	188799 MC	177240
5 / 23	189031 A1	177240, 177242
6 / 29	105913 CF(1)	177240, 177242
7 / 15	195986 ODG	177240, 177242
8 / 15	195986 ODG	177240, 177242
9 / 11	105886 FF(8.2K)	177242, 177244
10 / 16	195990 UG	177244
11 / 16	195990 UG	177244
12 / 21	189041 MO(2)	177244

Bay M

Section T

Schematic	Circuit No.	
25 (17)	188845 PFR-N	177249
26 (9)	105830 ADL	177249
27 (10)	195993 DL	177249
28 (17)	188845 PFR-N	177249
29 (9)	105830 ADL	177249
30 (10)	195993 DL	177249
31 (17)	188845 PFR-N	177249
32 (9)	105830 ADL	177249
33 (10)	195993 DL	177249
34 (17)	188845 PFR-N	177249
35 (22)	188990 D(2)	177250
36 (22)	188990 D(2)	177250

Section T

Schematic	Circuit No.	
13 (8)	188906 SSG	177249
14 (8)	188906 SSG	177249
15 (8)	188906 SSG	177249
16 (8)	188906 SSG	177249
17 (8)	188906 SSG	177249
18 (8)	188906 SSG	177249
19 (8)	188906 SSG	177249
20 (8)	188906 SSG	177249
21 (8)	188906 SSG	177249
22 (8)	188906 SSG	177249
23 (8)	188906 SSG	177249
24 (8)	188906 SSG	177249

Section T

Schematic	Circuit No.	
1 (20)	189044 DPC(rM)	177249
2 (20)	189044 DPC(rM)	177249
3 (20)	189044 DPC(rM)	177249
4 (20)	189044 DPC(rM)	177249
5 (20)	189044 DPC(rM)	177249
6 (20)	189044 DPC(rM)	177249
7 (20)	189044 DPC(rM)	177249
8 (20)	189044 DPC(rM)	177249
9 (20)	189044 DPC(rM)	177249
10 (20)	189044 DPC(rM)	177249
11 (20)	189044 DPC(rM)	177249
12 (20)	189044 DPC(rM)	177249

Bay N

Section V

Schematic		Circuit No.
25 (5)	188862 LD	177239
26 (5)	188862 LD	177239
27 (21)	189041 MO(2)	177236
28 (21)	189041 MO(2)	177236
29 (21)	189041 MO(2)	177236
30 (21)	189041 MO(2)	177236
31 (14)	188925 OEC-S	177280
32 (14)	188925 OEC-S	177280
33 (26)	195997 N5	177300, 177238
34 (26)	195997 N5	177300, 177238
35 (26)	195997 N5	177300, 177238
36 (26)	195997 N5	177300, 177238

Section V

Schematic		Circuit No.
13 (5)	188862 LD	177239
14 (3)	105834 DPC(rI)	177300, 177238
15 (3)	105834 DPC(rI)	177300, 177238
16 (3)	105834 DPC(rI)	177300, 177238
17 (3)	105834 DPC(rI)	177300, 177238
18 (3)	105834 DPC(rI)	177300, 177238
19 (3)	105834 DPC(rI)	177300, 177238
20 (3)	105834 DPC(rI)	177300, 177238
21 (3)	105834 DPC(rI)	177300, 177238
22 (3)	105834 DPC(rI)	177300, 177238
23 (3)	105834 DPC(rI)	177300, 177238
24 (3)	105834 DPC(rI)	177300, 177238

Section V

Schematic		Circuit No.
1 (3)	105834 DPC(rI)	177300, 177238
2	rI & Diverter Cards	
3		
4 (3)	105834 DPC(rI)	177300, 177238
5 (3)	105834 DPC(rI)	177300, 177238
6 (3)	105834 DPC(rI)	177300, 177238
7 (3)	105834 DPC(rI)	177300, 177238
8 (3)	105834 DPC(rI)	177300, 177238
9 (3)	105834 DPC(rI)	177300, 177238
10 (3)	105834 DPC(rI)	177300, 177238
11 (3)	105834 DPC(rI)	177300, 177238
12 (3)	105834 DPC(rI)	177300, 177238

Bay N

Section X

Schematic	Circuit No.
25 (12) 195939 SEQ	177239, 177244
26 (12) 195939 SEQ	177239
27 (12) 195939 SEQ	177235
28 (23) 189031 A-I	177237, 177240
29 (23) 189031 A-I	177237, 177240
30 ( ) Spare	•
31 (6) 105668 D(1)	177235, 177244
32 (2) 105826 C & P	177236
33 (2) 105826 C & P	177235
34 (1) 188799 MC	177235
35 (21) 189041 MO(2)	177235
36 (21) 189041 MO(2)	177235

Section X

Schematic	Circuit No.
13 (15) 195986 ODG	177236, 177239
14 (15) 195986 ODG	177236, 177239
15 (15) 195986 ODG	177235, 177237, 177239
16 (15) 195986 ODG	177235, 177237, 177239
17 (16) 195990 UG	177236, 177239, 177280
18 (16) 195990 UG	177235, 177236, 177239
19 (16) 195990 UG	177237, 177239
20 (16) 195990 UG	177235, 177237, 177239
21 (16) 195990 UG	177237
22 (16) 195990 UG	177235
23 (16) 195990 UG	177235
24 (16) 195990 UG	177235

Section X

Schematic	Circuit No.
1 (11) 105886 FF(8.2K)	177239
2 (11) 105886 FF(8.2K)	177239
3 (1) 188799 MC	177236, 177237
4 (21) 189041 MO(2)	177237
5 (1) 188799 MC	177236, 177237
6 (18) 189012 O-I	177237, 177239
7 (18) 189012 O-I	177237, 177239
8 (30) 106267 CF(2)	177237, 177239
9 (30) 106267 CF(2)	177237, 177239
10 (6) 105668 D(1)	177235
11 (6) 105668 D(1)	177235
12 (6) 105668 D(1)	177235

Bay N

Section V

Schematic		Circuit No.
25 (15)	195986 ODG	177235, 177237
26 (16)	195990 UG	177235
27 (16)	195990 UG	17723, 177239
28	Spare	
29 (7)	188851 PFR-P	177271
30 (7)	188851 PFR-P	177271
31 (7)	188851 PFR-P	177271
32 (7)	188851 PFR-P	177271
33 (7)	188851 PFR-P	177271
34 (7)	188851 PFR-P	177271
35 (7)	188851 PFR-P	177271
36 (7)	188851 PFR-P	177271

Section V

Schematic		Circuit No.
13 (6)	105668 D(1)	177239
14 (6)	105668 D(1)	177239
15 (6)	105668 D(1)	177239
16 (6)	105668 D(1)	177235
17 (6)	105668 D(1)	177271, 177239
18 (6)	105668 D(1)	177235, 177271
19 (6)	105668 D(1)	177271
20 (6)	105668 D(1)	177271
21 (6)	105668 D(1)	177235, 177247
22	Spare	
23	Spare	
24	Spare	

Section V

Schematic		Circuit No.
1 (13)	188969 FF(4.2K)	177235
2 (13)	188969 FF(4.2K)	177237, 177239
3 (13)	188969 FF(4.2K)	177235
4	Spare	
5 (7)	188851 PFR-P	177271
6 (7)	188851 PFR-P	177271
7 (7)	188851 PFR-P	177271
8 (7)	188851 PFR-P	177271
9 (7)	188851 PFR-P	177271
10 (7)	188851 PFR-P	177271
11 (7)	188851 PFR-P	177271
12 (7)	188851 PFR-P	177271

Bay G

Section X

Schematic	Circuit No.
1	182369	177215, 177255, 177281
2	182370	177215, 177255
3	182384	177281
4	182384	177281
5	182373	177281
6	182386	177281
7	182375	177265, 177273, 177250
8	182376	177268, 177273
9	182377	177256
10	182378	177256
11	182379	177256
12	182380	177256

Section V

Schematic	Circuit No.
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		

Section T

Schematic	Circuit No.
1	182369	177215, 177255 177281
2	182370	177215, 177255
3	182371	177215
4	182372	177215
5	182373	177281
6	182374	177281
7	182375	177265, 177273, 177250
8	182376	177268, 177273
9	182377	177256
10	182378	177256
11	182379	177256
12	182380	177256

Bay G

Section X

Schematic	Circuit No.
182393	177256, 177267
182394	177256, 177261
182395	177261
182396	177261
182397	177261
182398	177261
182399	177261
182400	177261
182401	177261
182402	177261
182403	177261
182404	177261

Section V

Schematic	Circuit No.
182405	177274, 177271
182406	177274
182407	177266
182407	177266
182409	177268, 177247
182410	177247, 177271
182411	177217
182412	177217, 177267
182413	177217
182414	177217
182415	177217
182416	177217

Section X

Schematic	Circuit No.
182393	177256, 177267
182394	177256, 177261
182395	177261
182396	177261
182397	177261
182398	177261
182399	177261
182400	177261
182401	177261
182402	177261
182403	177261
182404	177261

Bay H

Section X

Schematic	Circuit No.
1 182429	177266, 177268 177273
2 182430	177268, 177237
3 Spare	
4 182432	177255, 177267
5 182433	177255
6 182434	177255
7 182435	177255
8 182436	177255, 177267
9 182437	177268, 177273
10 182438	177257
11 182439	177257
12 182440	177257

Section V

Schematic	Circuit No.
1 182441	177217
2 182442	177217, 177267
3 182443	177217, 177267
4 182444	177281, 177286
5 182445	177287
6 182446	177286
7 182447	177286
8 182448	177265
9 182446	177286
10 182447	177286
11 182448	177265
12 182452	177215, 177266

Section T

Schematic	Circuit No.
1 182429	177266, 177268 177273
2 182430	177268, 177273
3 182431	177266
4 182432	177255, 177267
5 182433	177255
6 182434	177255
7 182435	177255
8 182436	177255, 177267
9 182437	177268, 177273
10 182438	177257
11 182439	177257
12 182440	177257

Bay J

Section X

Schematic	Circuit No.
182465	177257
182466	177257, 177267
182467	177257, 177258
182468	177257, 177258
182469	177257, 177274
182470	177257, 177266
Spare	-----
182472	177258
182473	177258
182474	177258
182475	177258
182476	177258

Section V

Schematic	Circuit No.
182477	177274
182478	177273, 177274
182479	177274 177270
182480	177268, 177274
182481	177271, 177272
Spare	-----
182483	177286, 177287
182484	177268
182485	177268
Spare	-----
182487	177265, 177268
182488	177265, 177268

Section T

Schematic	Circuit No.
182465	177257
182466	177257, 177267
182467	177257, 177258
182468	177257, 177258
182469	177257, 177274
182470	177257, 177266
Spare	-----
182472	177258
182473	177258
182474	177258
182475	177258
182476	177258

Bay K

Section X

Schematic	Circuit No.
1	182501	177258, 177259 177265, 177286
2	182502	177259
3	182503	177259
4	182504	177259
5	182505	177259
6	182506	177258, 177260
7	182507	177260
8	182508	177260
9	182509	177260, 177265
10	182510	177260
11	182511	177265, 177273
12	182512	177265, 177273

Section V

Schematic	Circuit No.
1	182513	177270
2	182514	177270, 177274
3	182515	177270, 177274
4	182516	177270
5	182517	177270
6	182518	177270
7	182519	177270
8	182520	177266, 177268
9	182521,	177268, 177270 177272
10	182522	177270, 177274 177272
11	182523	177265, 177269 177270, 177274
12	182524	177265

Section T

Schematic	Circuit No.
1	182501	177258, 177259 177265, 177286
2	182502	177259
3	182503	177259
4	182504	177259
5	182505	177259
6	182506	177258, 177260
7	182507	177260
8	182508	177260
9	182509	177260, 177265
10	182510	177260
11	182511	177265, 177273
12	182512	177265, 177273

Bay L

Section X

Schematic	Circuit No.
1	182537	177265
2	182538	177265, 177268
3	182539	177265
4	182540	177268
5	182541	177256, 177262
6	182542	177262
7	182543	177262
8	182544	177262
9	182545	177262, 177271 177274
10	182546	177262, 177271
11	182547	177262
12	182548	177262

Section V

Schematic	Circuit No.
1	182549	177271
2	182550	177271
3	182551	177272
4	182551	177272
5	182553	177269
6	182554	177269
7	182555	177269
8	182556	177265, 177269 177274
9	182557	177269
10	182558	177269
11	182559	177269
12	182560	177287

Section T

Schematic	Circuit No.
1	182537	177265
2	182538	177265, 177268
3	182539	177265
4	182540	177268
5	182541	177256, 177262
6	182542	177262
7	182543	177262
8	182544	177262
9	182545	177262, 177271, 177274
10	182546	177262, 177271
11	182547	177262
12	182548	177262

Bay P

APPENDIX B

SUPPLEMENTAL MAINTENANCE INFORMATION

UNIVAC II

MAINTENANCE SWITCHES

1. GENERAL. - In addition to those on SC there are switches about the Central Computer which provide a means for the maintenance man to interrupt or modify the operation of various circuits within the Univac II system. This appendix locates these switches and identifies them by their type and the function they serve.

2. SWITCHES LOCATED INSIDE THE CENTRAL COMPUTER. - The number following the physical location identifies the Circuit Diagram on which this switch appears.

LOCATION	TYPE	PURPOSE
HV Backboard 177261	3-pole, 3-position wafer switch	Selects the circuit, MQC (left) or $\overline{\text{MQC}}$ (right), to operate the IER, OR and IER-OR drivers.
PV 106292, 106293 or 106294	Push button with lock	Drops d-c and when locked prevents d-c power from being turned on.
Roof Sheet 106292, 106293 or 106294	Trigger	(Trolley Line) Enables all power to be dropped in an emergency situation.

3. SWITCHES ABOUT THE CENTRAL COMPUTER PERIMETER. - The number following the physical location identifies the Circuit Diagram on which the switch appears.

LOCATION	TYPE	PURPOSE
A9T 177207	1-pole, double throw bat handle	Causes a pseudo-Read End (down) to be generated to test the Automatic Reread circuits. The up position is the normal operating position.

LOCATION	TYPE	PURPOSE
B5X 177267	1-pole, 10-position 1-pole, 12-position 2-pole, 3-position	Select the variable synch signals.
B7X 177284	1-pole, 2-position	Allow FTOC to function without a sample pulse
MV 177250	Toggle, 3-position	Force rZW to binary "1's" or binary "0's".
MV 177250		Force rM to binary "1's" or binary "0's".
NV 177239	Toggle, 3-position	Force rI to binary "1's" or binary "0's".
MX 177242	Toggle, 2-position	Disables the transfer of (rM) to r0 operation.

4. SWITCHES IN BC CORNER (BC BOX). - The circuits of the maintenance switches in BC Corner appear on print 166285.

NAME	TYPE	PURPOSE
MULTIVIBRATOR	Rotary, 3-position	Enables the control, either manual (RUN) or multivibrator (MULT), of the START READ (FF621A) or START WRITE (FF621B) flip-flops. (The condition of the Read-Write relay determines the action that will occur.)
SYNCH SELECTOR	Rotary, 4-position	Selects one of four available oscilloscope synchronization signals: START READ, READ END, WRITE FORWARD OR SPROCKET.
READ-WRITE CHANNEL SELECTOR	Rotary, 9-position	Permits the observation by oscilloscope of the pulse content of the eight tape channels, and the operation of the photocells in the Bad Spot Detectors.
SCOPE SELECTOR	Toggle, 2-position	Selects the circuit, Read or Write, to be viewed when the READ-WRITE CHANNEL SELECTOR switch is operated.

NAME	TYPE	PURPOSE
UNISERVO SELECTOR	16 push buttons, one for each Uniservo	Permits the manual selection of the Uniservo lines.
FUNCTION SELECTOR SWITCHES	6 push buttons	Operated in conjunction with the UNISERVO SELECTOR switches to complete the manual Uniservo instructions: Read (R) or Write (W), Forward (F) or Backward (B), and Rewind (RE) or Rewind with Interlock (REI).
FUNCTION SELECTOR SWITCHES	2 push buttons	Generate the Read Clear (RC) or Write Clear (WC) signal.
FT NEON TEST (located on FT indicator panel)	Toggle, 2-position	When depressed, all FT neon indicators fire. Detects defective neons.

5. SWITCHES IN KL CORNER. - The circuits of the maintenance switches in KL Corner appear on print 106291.

NAME	TYPE	PURPOSE
DC FAULT TEST	Toggle, 2-position	When depressed, neons light indicating the bay in which a fuse has blown.
PRI FAULT RESET	Push button	Removes +48 vdc from the AC FAULT holding relays (RP16 and RP17).
VOLTAGE BELL LO	Toggle	Controls voltage failure alarm bell. Normally the bell rings indicating that some d-c voltage has varied from its established tolerance. Depressing this switch causes the bell to cease ringing, and sound again when the voltage returns within the tolerance limits.
MARGIN CHECK	Toggle	Causes the filament voltages on all tubes except those in the Short Tank chassis and the SR 7AK7's to be reduced by 12% to check marginal operation.

NAME	TYPE	PURPOSE
RESET MONITOR	Push button	Resets the Voltage Monitor timer and the Switchgear overvoltage monitor.
SR 7AK7 MARGIN	Toggle	Reduces the filament voltage to the SR 7AK7's by 12%.
INPUT ERROR	Toggle	Disables the Channel 1 Schmitt Trigger circuit eventually causing an input error.
VOLTAGE MONITOR LO	Toggle	Locks out the Voltage Monitor timer, thus preventing voltage shut-down.
HI TEMP BELL LO	Toggle	Controls Hi Temp alarm bell. Normally the bell rings indicating a high temperature condition exists in one of the bays. Depressing the switch causes the bell to cease ringing, and sound again when the high temperature condition is gone.
RETAIN PC	Toggle	Prevents the Program Counter from being stepped.
WRITE ENDING	Toggle	Prevents the generation of a Write Ending.
READ ENDING	Toggle	Prevents the generation of a Read Ending.
MEMORY PRESET TEST	Toggle	In conjunction with a switch on SC performs a check on the rM Preset Checker. With special programming this switch can cause the transfer of the contents of rM to tape.
FT INT	Rotary, 8-position	Causes error conditions in FTIC to determine if the checker circuits are operating properly.
STAND-BY BELL LO	Toggle	Controls the stand-by power alarm bell. Normally the bell rings when stand-by power fails. Depressing this switch causes the bell to cease ringing and to sound again when stand-by power is restored.
S-12	Toggle	Spare

APPENDIX C

SUPPLEMENTAL MAINTENANCE INFORMATION

UNIVAC II

MAINTENANCE MULTIVIBRATOR

1. GENERAL. - This appendix presents the schematic for a multivibrator of the type used as a trigger device in certain maintenance routines. Normally the start circuits are activated by operating the START BAR on SC. However, if it is desired that the start circuits be triggered repetitively, or at a regular frequency, the multivibrator can be inserted into the system, parallel to the START BAR, to perform this function. The socket for the multivibrator is located on the rear of the SC Console.

In addition, the multivibrator provides a source for pulses to test the operation of the single pulse network and the delay lines in the Cycling Unit. A socket in P8V receives the multivibrator jack and introduces the pulses generated into the CU delay elements. This system is presented on Circuit Diagram 177269.

Control over the operation of the multivibrator network is provided by a number of switches. Switch-1 (S-1) applies or removes line power to the circuit. Switch-2 (S-2) when open, holds the multivibrator in the stable state of side "A" conducting and side "B" cut-off. The relay switch (S-3) disables the chassis output even though the multivibrator action continues. Switches 4 and 5 (S-4 and S-5) change the inter-section capacitance thereby regulating the recovery time of the flip-flop sections; thus, they control the frequency at which the multivibrator operates. S-4 and S-5 permit operating frequencies

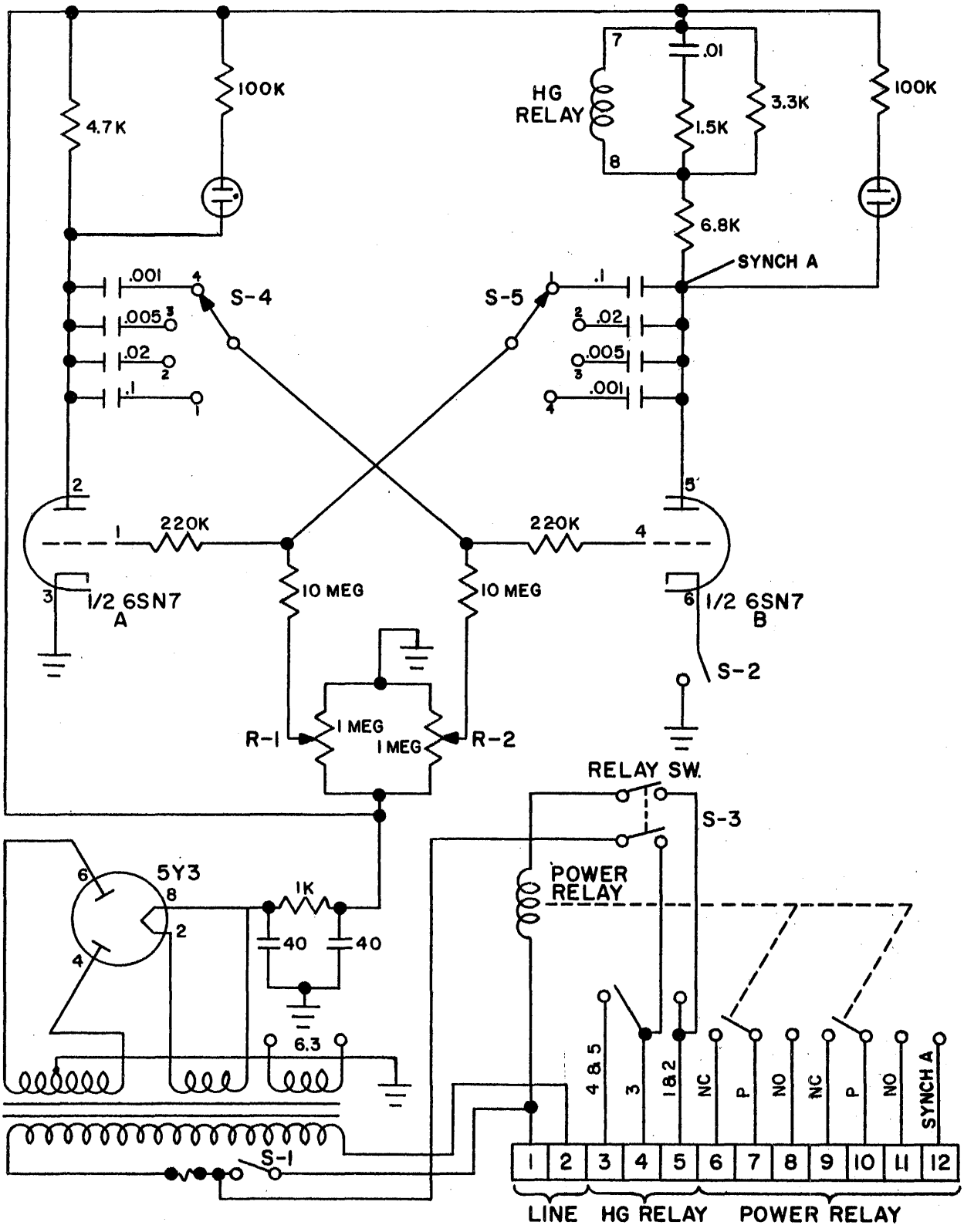


Figure C-1. Maintenance Multivibrator

in the range of .5 ms. to 3.5 sec. The fine frequency adjustment is provided by potentiometer R1 and R2. R1 and R2 provide the following ranges to the coarse frequency settings of S4 and S5.

S4 and S5 Positions	Range
1-1	.5 sec. to 3.5 sec.
2-2	.1 sec. to .7 sec.
3-3	25 ms. to 160 ms.
4-4	.5 ms. to 40 ms.

APPENDIX D

SUPPLEMENTAL MAINTENANCE PROCEDURES

UNIVAC II

MEMORY MARGIN TEST PROCEDURES

1. GENERAL. - This procedure was prepared as a guide in establishing margins for the memory circuits in both the main memory and in the buffer storage units. This supplements the procedure outlined for memory check-out in the Evaluation Report.

The purpose of the margin test is to: establish the limits of the tolerances for the drive currents, the inhibit currents, and the sense bias voltages in the core matrices; and ascertain that the memory is operating at a point within these limits. It is assumed that the computer is operational, that it can run the Buffer Test routine, and that the rM Worst Pattern routine is without error.

The services of two qualified persons are required to perform the test. One operates the computer, the other reads and records the test data. If a third person is available to record the data the test will be expedited.

2. EQUIPMENT. - The following equipment is required to perform the margin test:

1. Two 20,000 ohm/volt multimeters (Simpson 260 or equivalent).
2. One Tektronix oscilloscope with a standard wide-band input amplifier.
3. One Tektronix oscilloscope with a differential pre-amplifier (53/54D or equivalent).
4. One 33-pin buggie type chassis extender (RRU part #196022).
5. Prepared data sheets, Figure D-4, and cross-hatch paper, (K & E 359-5DG or equivalent).

6. A test routine tape which includes the Buffer Test routine and the rM Worst Pattern routine.

3. PRELIMINARY PROCEDURES. - Prior to performing the test, the equipment used for determining the test data is set up to perform its function. The following paragraphs describe the procedure that is recommended.

1. Set up the Multimeter to monitor the sense bias voltage (zero to plus eight volts) and the inhibit current control bias (about -10 to -25 volts) of the memory unit to be tested. These voltages can be monitored at the test points provided on the 38 board of the bay section concerned. Figure D-1 presents a representation of the various 38 boards on which the test terminal and the current adjusting Helipots are located.

2. Place any Digit Plane Control Chassis associated with the memory under test on a chassis extender. Connect the oscilloscope with the standard wide-band input amplifier to the collector of one of the 2N123 transistors (test terminal C or D) in the first stage of the sense amplifier (this circuit is presented in Figure D-2). The test made at this point checks the balance between the "read" and "write" currents by visually indicating the signals produced during the "read" and "write" times.

3. Calibrate the differential amplifier to read 100mv/cm. Figure D-3 indicates the differential amplifier controls. Set the mv/cm control to "1" and the multiplier control to "50". Set the Input Selector control to A-B (DC) and connect the input terminals to the oscilloscope Square-wave Calibrator output terminal. The Square-wave Calibrator control is set to .5 volts. Accurately

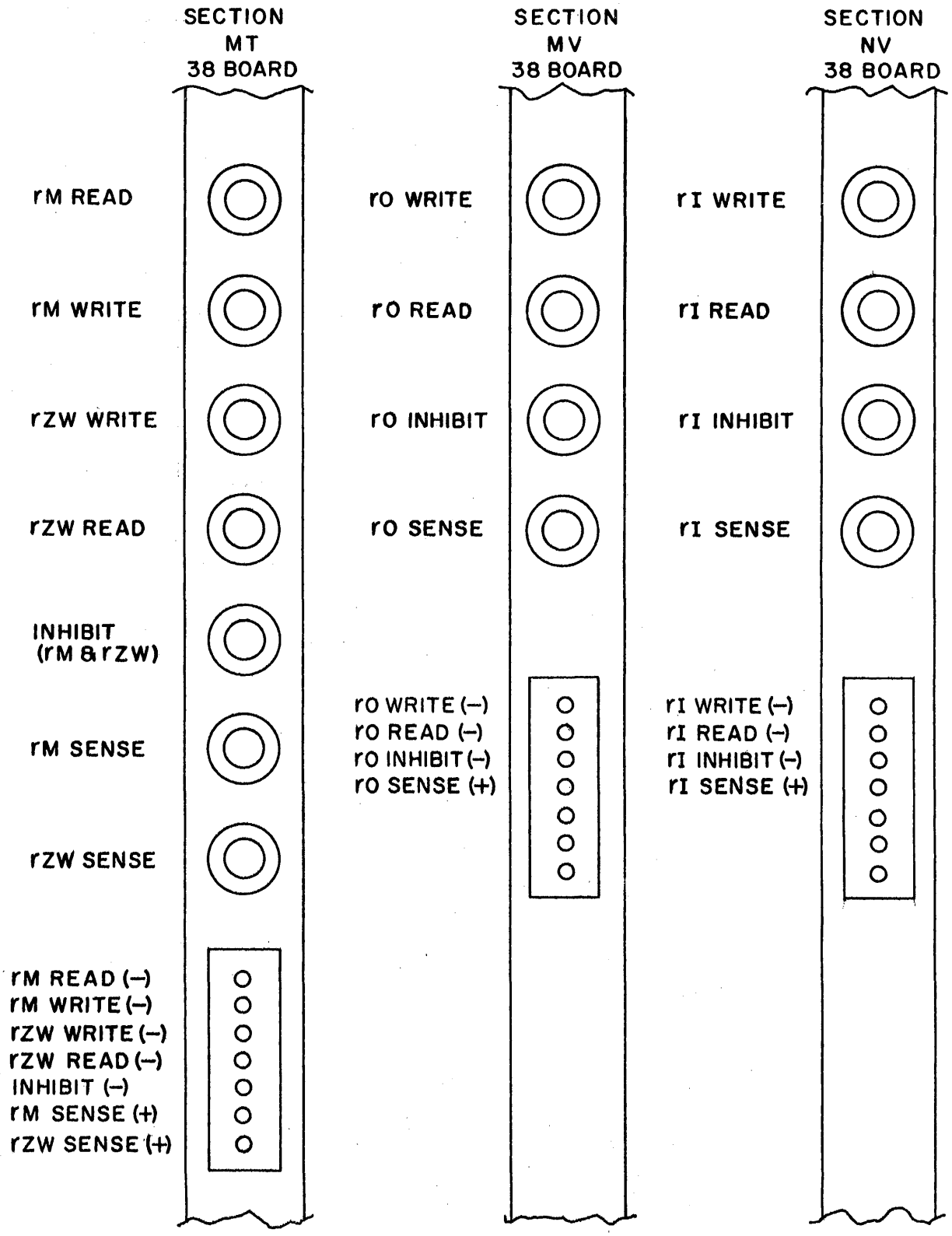
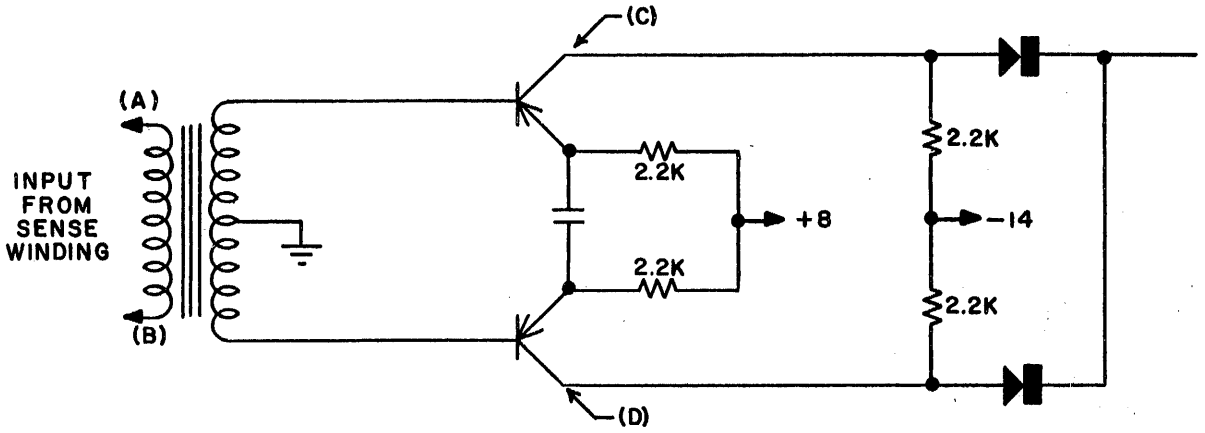
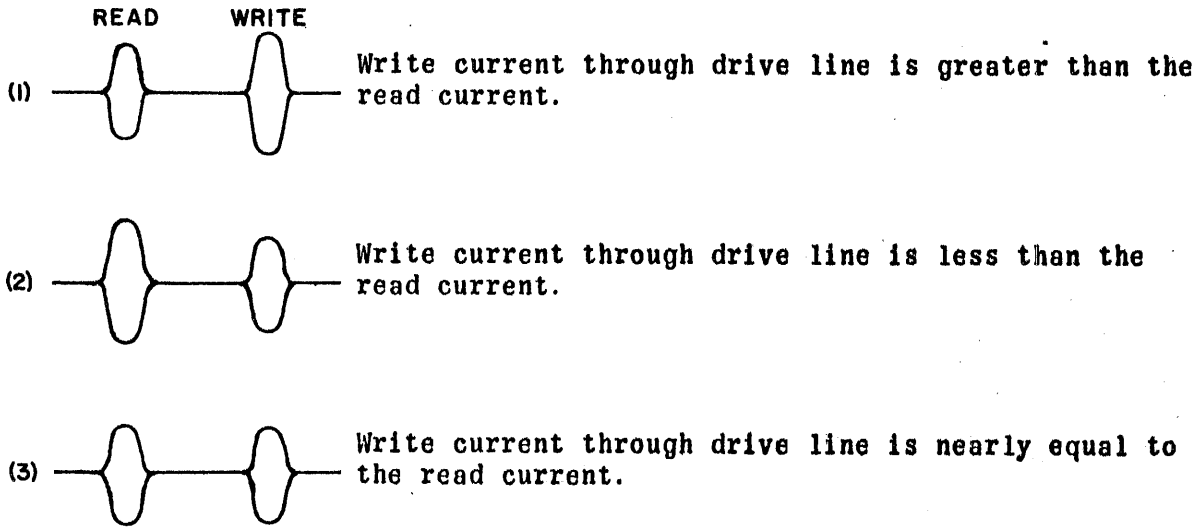


Figure D-1. Location of Control Helipots and Their Associated Bias Test Points.



Waveshapes

Sense output voltages across (A) and (B) with differential preamplifier.



Voltages across (C) and (D)

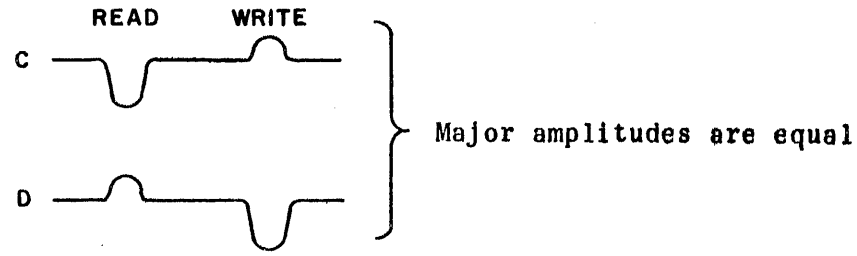


Figure D-2. Sense Amplifier Input of a DPC Chassis

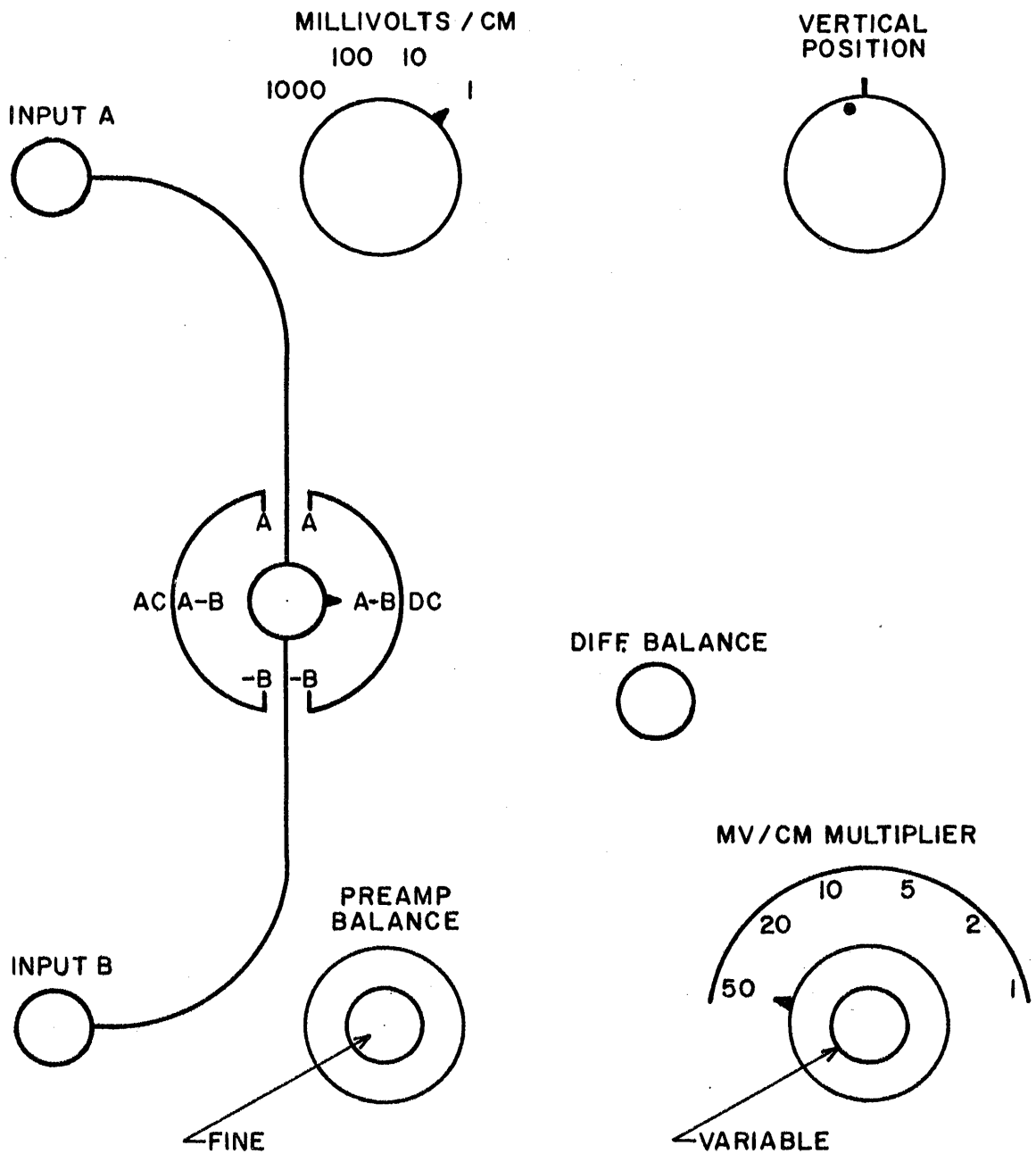


Figure D-3. Control Panel, 53/54D Preamplifier

adjust the Variable control for a deflection of 5 cm. When so adjusted the oscilloscope will indicate 50 ma.of pulse current across the 2-ohm current monitoring resistors on the diverter cards, the line drivers (type 5) and the diverter base switch (type 27) chassis.

To measure the drive currents in the main memory connect the twisted pair from the differential amplifier input terminals to the A and B test terminals or the G and H test terminals of the type 27 chassis. To measure the drive currents in rI, rO and rZW connect the twisted pair to test terminals D and G of any type 5 chassis associated with the memory being checked. For all buffer memories the drive currents can be best observed while running the buffer test routine with the subroutine associated with the buffer under test. To observe and accurately set up the main memory drive currents a SKIP instruction should be locked in on SC with the Master Delete switch depressed and the computer running in CONTINUOUS.

When the drive currents are to be adjusted always change the Read current first. This is necessary since the current overshoot caused by the Read current aids the Write current. The Write current can then be adjusted. Using the oscilloscope with the standard wide-band input amplifier observe the "write" current, setting the amplitude of the signal out at "write" time equal to the amplitude of the signal occurring during "read" time. With the signals balanced there will be approximately 20 ma.difference between the "read" and "write" currents in the drive chassis.

4. MEMORY MARGIN PROCEDURE. - The memory margin tests are described in the stages that follow:

1. Record the initial settings on the data sheet (Figure D-4) in the space provided.

MEMORY DATA SHEET

_____ MEMORY SERIAL # _____

INSTALLATION _____ SERIAL # _____

DATA BY _____ DATE _____

DRIVE MA / BIAS VOLTS						

INITIAL SETTING

READ CURRENT _____ MA. BIAS VOLTS _____ DIAL _____

WRITE CURRENT _____ MA. BIAS VOLTS _____ DIAL _____

INHIBIT CURRENT _____ MA. BIAS VOLTS _____ DIAL _____

SENSE BIAS _____ VOLTS. DIAL _____

Figure D-4. Memory Margin Test Data Recording Sheet

2. Place all Error Delete switches in the "normal" position.
3. Set the sense bias voltage to any whole number, preferably 3, 4 or 5, as point to determine the first set of limits.
4. Readjust the drive currents to the nearest multiple of 5 ma as an aid in determining readings.
5. The test routine is running.
6. Reduce the inhibit current until an induced error stops the computer. Record the inhibit bias control voltage at which the failure occurred. Increase the inhibit current (change the bias in .5 volt increments) while the operator attempts to restore the program. Record the inhibit bias reading at which the operation is restored.
7. The inhibit current is increased until an error again stops the computer. The inhibit bias control voltage, at point of failure, is recorded. The inhibit current is gradually reduced (lower the bias .5 volts at a time) while the operator tries to restore operation. Record the inhibit bias at the point information is restored. Return inhibit bias to initial value.
8. Change the sense bias voltage in increments of one volt from the starting value. For each value of sense bias repeat the process outlined in steps six and seven.
9. Change the line current reading by five or ten milliamperes to locate the widest range of drive current at which the computer will operate. For each different drive current reading repeat steps six, seven and eight.
10. Make a calibration of the inhibit current versus inhibit control bias (Figure D-5). All digit plane controls have one ohm current

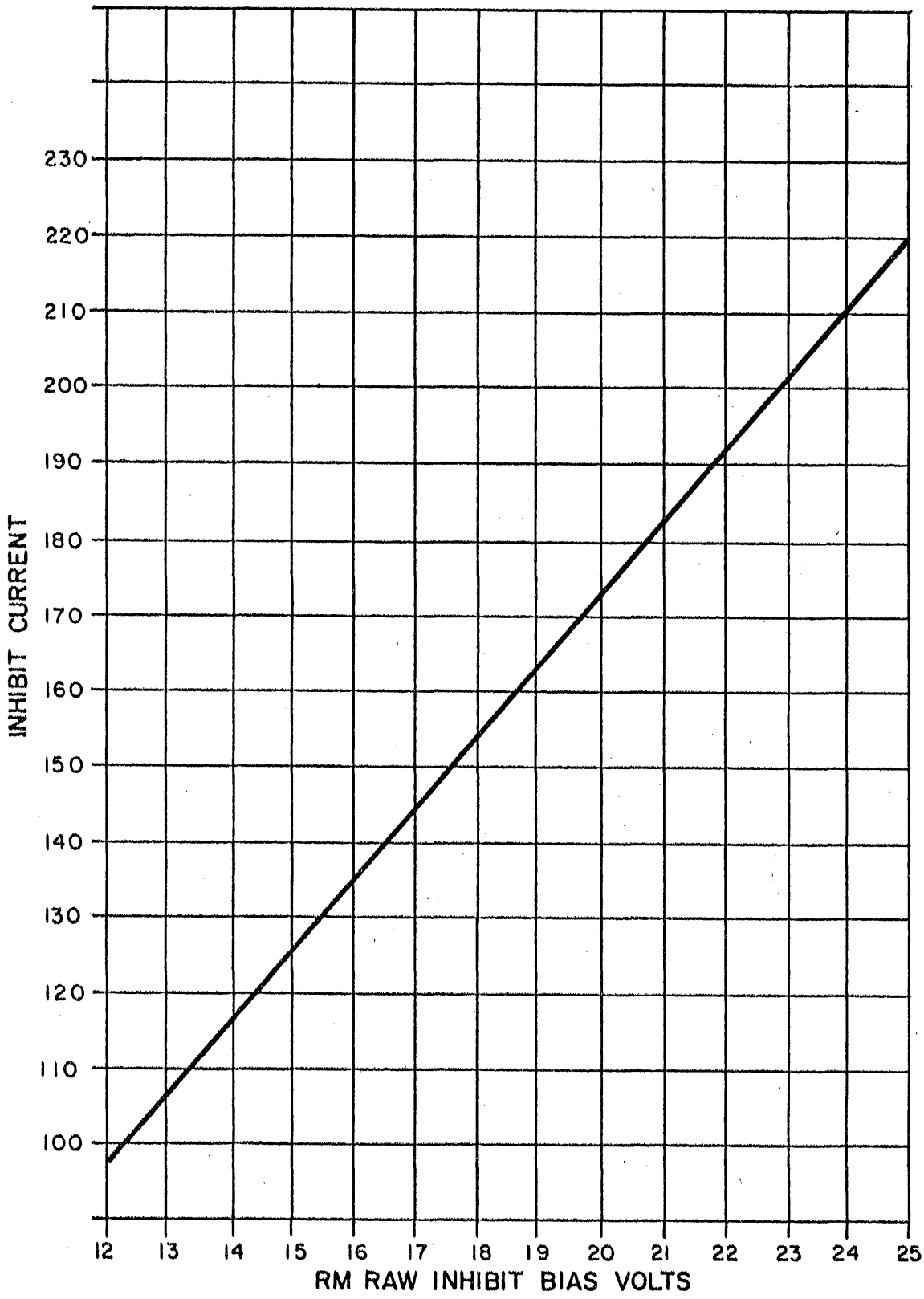


Figure D-5. Typical Example, Inhibit Current vs. Inhibit Control Bias

monitoring resistors, therefore, the oscilloscope will read 100 ma/cm unless it has been recalibrated. The inhibit current can be read by connecting the differential oscilloscope across the appropriate test points of the DPC chassis on the extender.

11. Plot the range of inhibit current at each drive current for each sense bias voltage. (See Figure D-6).
12. Select an operating point on the graph that will give a drive current with a $\pm$5% minimum range. The inhibit current should have a $\pm$10% minimum range from the nominal. The sense bias should have a range of 1.5 volts. (See Figure D-6).
13. The limits of inhibit current in rM should be noted, in terms of control voltage since these become the limits of the inhibit current when checking rZW. (See Figure D-6).
14. To perform the r0 margin test a continuous "write" operation is necessary. The tape should be taken off the capstan, or the Uniservo otherwise disabled.
15. While performing the test, the control bias necessary for the various read and write currents and their respective dial settings should be recorded. This provides data for a simple calibration curve.

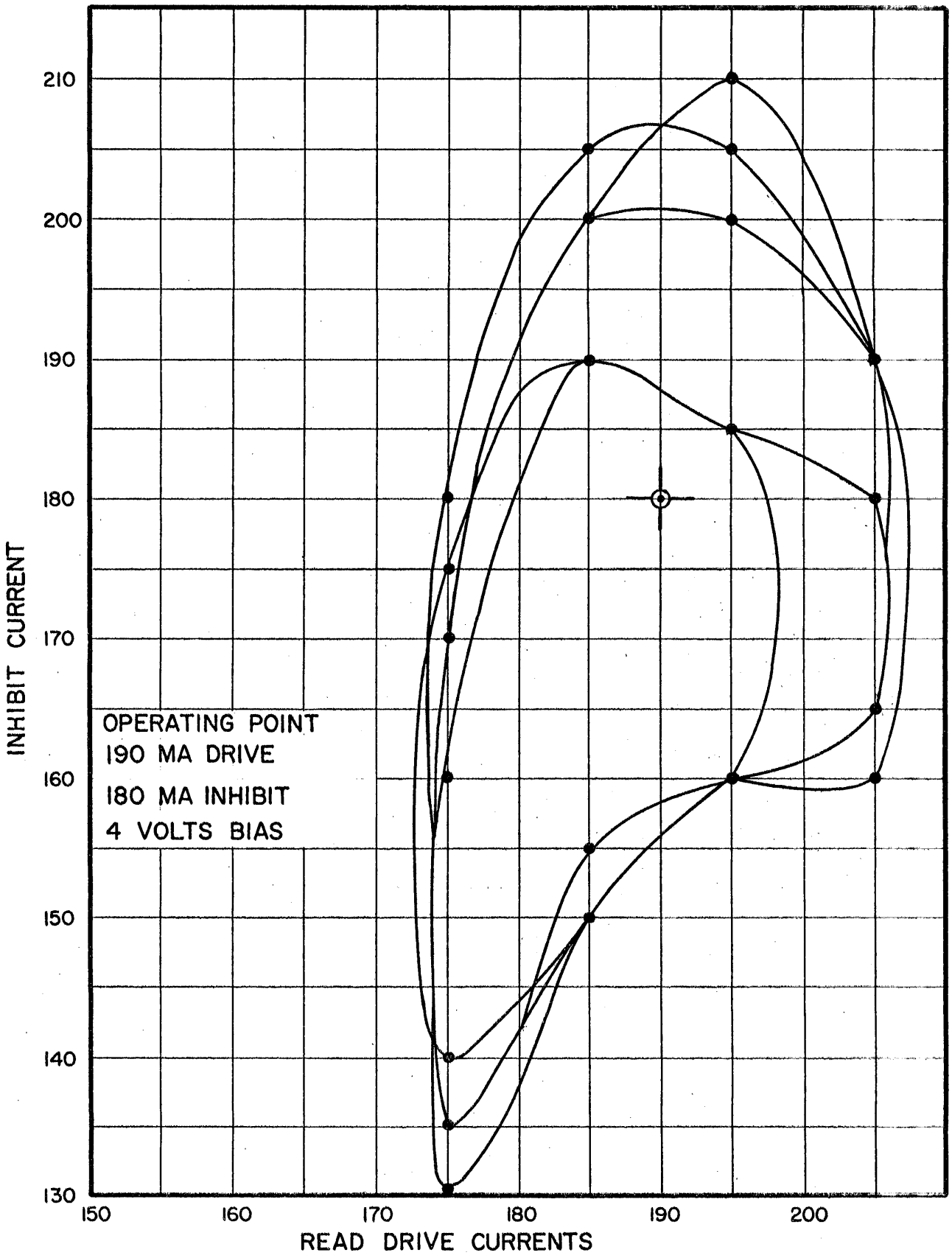


Figure D-6. Typical Example, Shmoo Diagram

PREVENTATIVE MAINTENANCE PROCEDURE

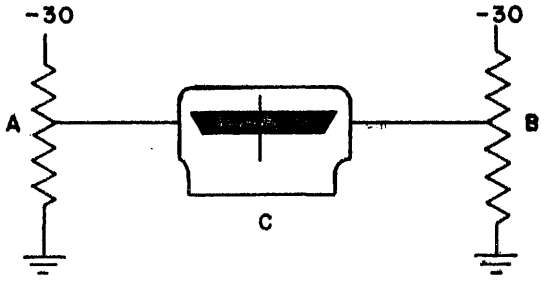
FOR MEMORY CIRCUITS IN UNIVAC II

A simple, but effective method of checking the memory in a preventative maintenance schedule can be performed by varying the read current, write current, inhibit current and sense bias. These parameters are varied independently with the memory worst pattern or buffer test routine running.

This check can be effected by varying each parameter to the specified operating tolerance. The operating tolerances set forth in the memory check out procedure are ±5% of the drive currents, ±10% of the inhibit current and a range of ±.75 volts of the sense bias.

A change of one volt of bias represents a change of ten ma. of pulse current. A method of monitoring the necessary deviation in operating currents is to measure the proportional change in bias voltage. A simple bridge can be formed to measure bias deviation.

The bridge and its use is outlined below:



A. Is an external potentiometer (about 5K),
B. Is the bias control potentiometer of the current to be varied,
C. Is a multimeter (Triplett or Simpson),

1. A is connected to ground and -30 at some convenient point.
2. The multimeter is connected between the arm of pot A and the test point of pot B.

3. Pot A is adjusted until the voltmeter reads a voltage (-8) about which it is convenient to deviate the voltage controlled by pot B.

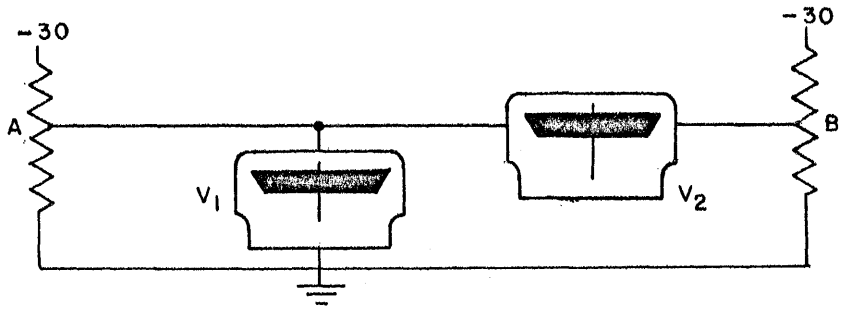
4. Pot B is then adjusted so the voltmeter reads a voltage, proportional to the change in current desired, above and below the voltage set up in step three.

5. The pot B is adjusted to return to the voltage initially set up in step 3.

6. It should be noted that all these voltage deviations are made with the proper test routine running.

Since it is desirable to know the control bias voltage more accurately than obtainable from a reading on a 50 or 60 volt scale of multimeter a means of reading the voltage on some form of expanded scale must be provided. This is readily accomplished if the voltage is read in addition to some reference voltage. Since the d.c voltages in the computer vary a volt meter must be used as a secondary standard to develop a reference voltage.

The circuit is a modification of the previous circuit shown.



1. Adjust A for a full scale reading on a ten or 12 volt scale of V1.*

2. The voltage at the arm of B is the sum of the voltage read on V1 & V2.

3. The measurements are restricted to voltage ranges equal to the sum of V1 and V2 readings.*

* Ten volts on Simpson #260 and 12 volts on Triplett #630.

A weekly log should be kept of each memory with the following heading.

Memory _____ Meter No. _____

	Sense Bias			Read Bias			Write Bias			In . Bias				
Date	Hi.	Nor.	Lo.	Hi.	Nor.	Lo.	Hi.	Nor.	Lo.	Hi.	Nor.	Lo.	Remarks	Initials

Each memory will require approximately one-quarter hour to be checked.

Each memory chassis requiring work should be checked by this method before being classified as a good spare.**

A procedure to "Schmoo" the memory is included in the maintenance manual.

** The chassis involved are the diverter cards and the types 3, 4, 5 and 20.

IDEALIZED WAVEFORMS
OF UNIVAC II MEMORY CIRCUITRY

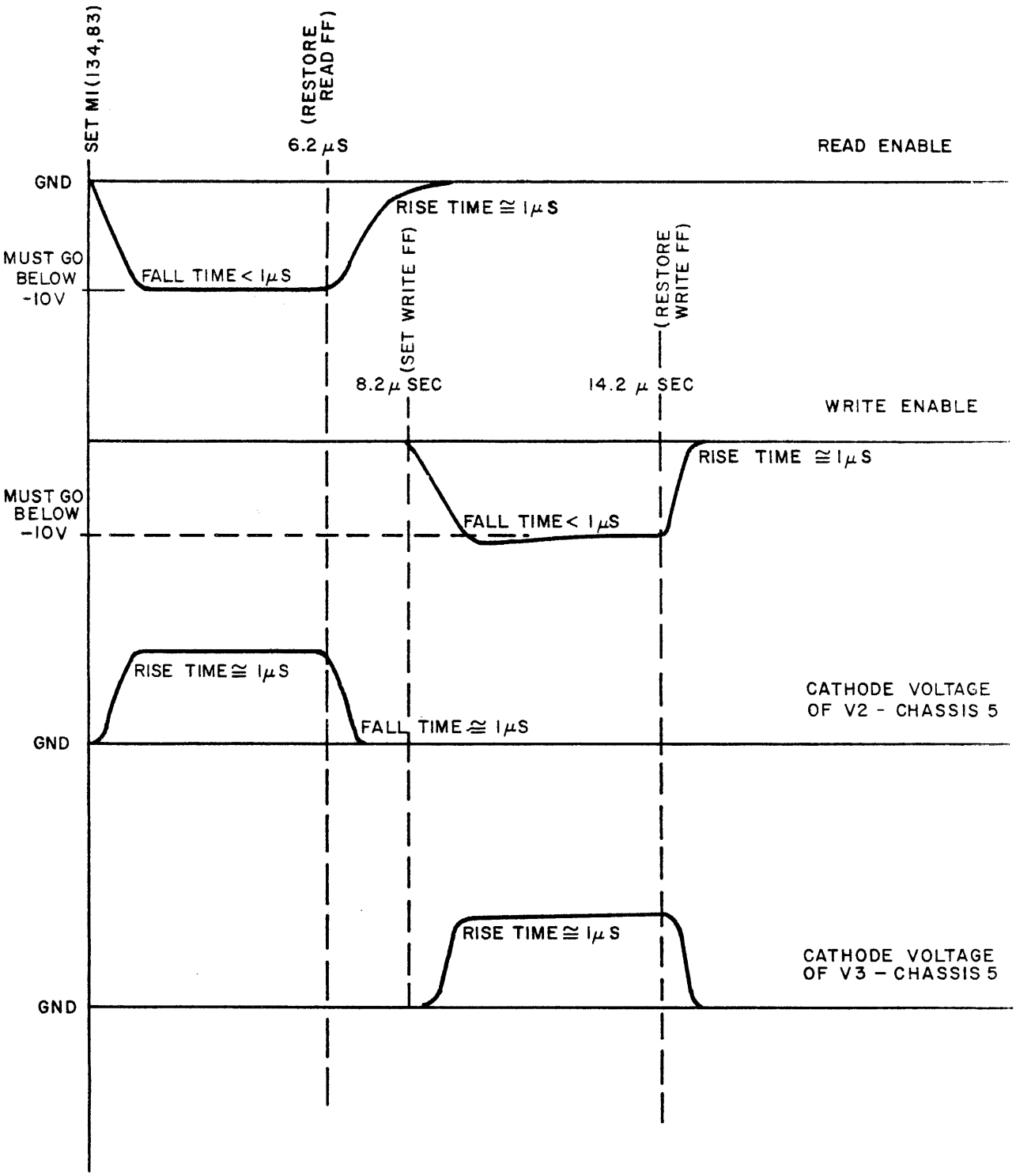


Figure D-7. Wave Shapes, Line Driver Chassis

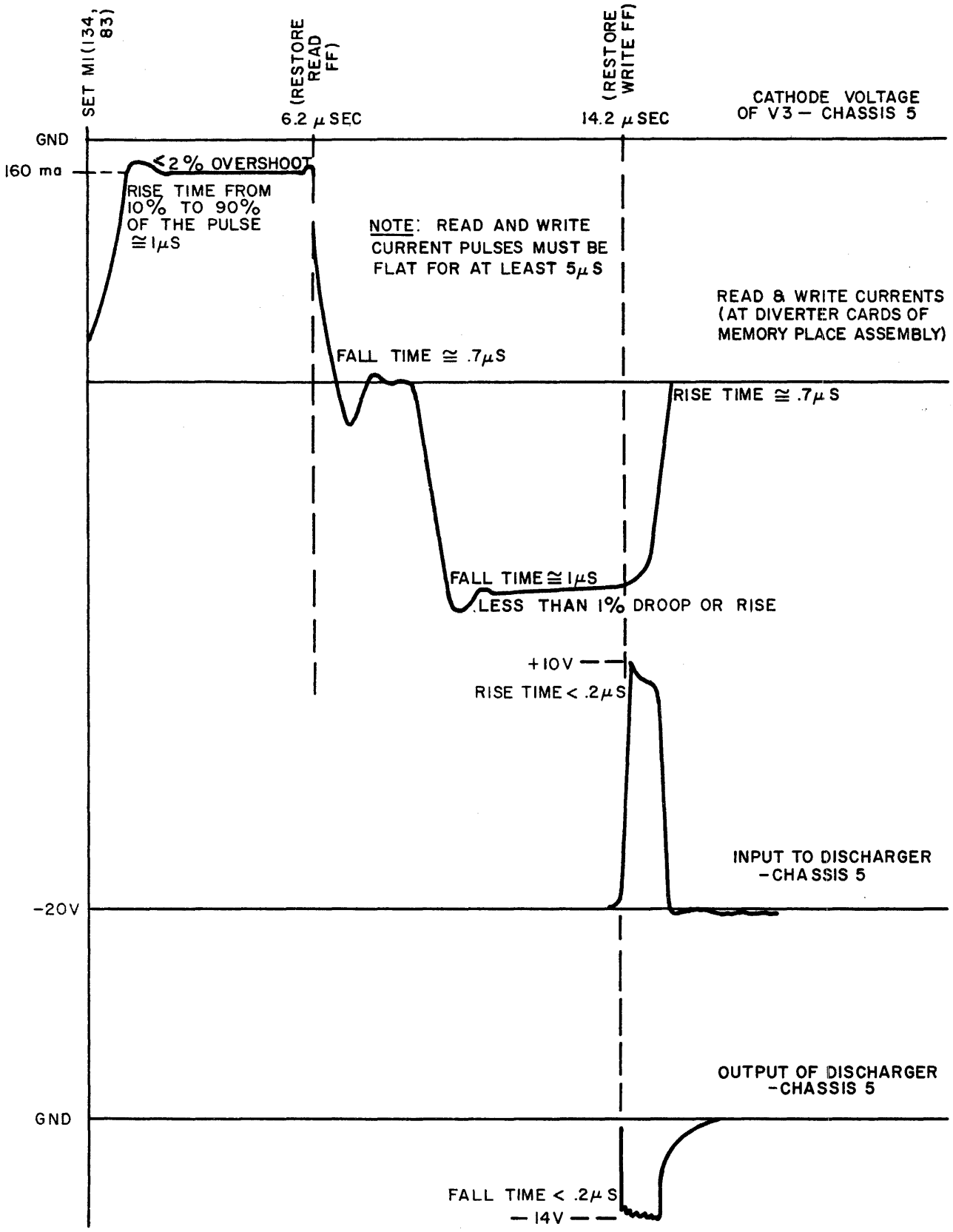


Figure D-8. Wave Shapes, Line Driver Chassis (Cont'd.)

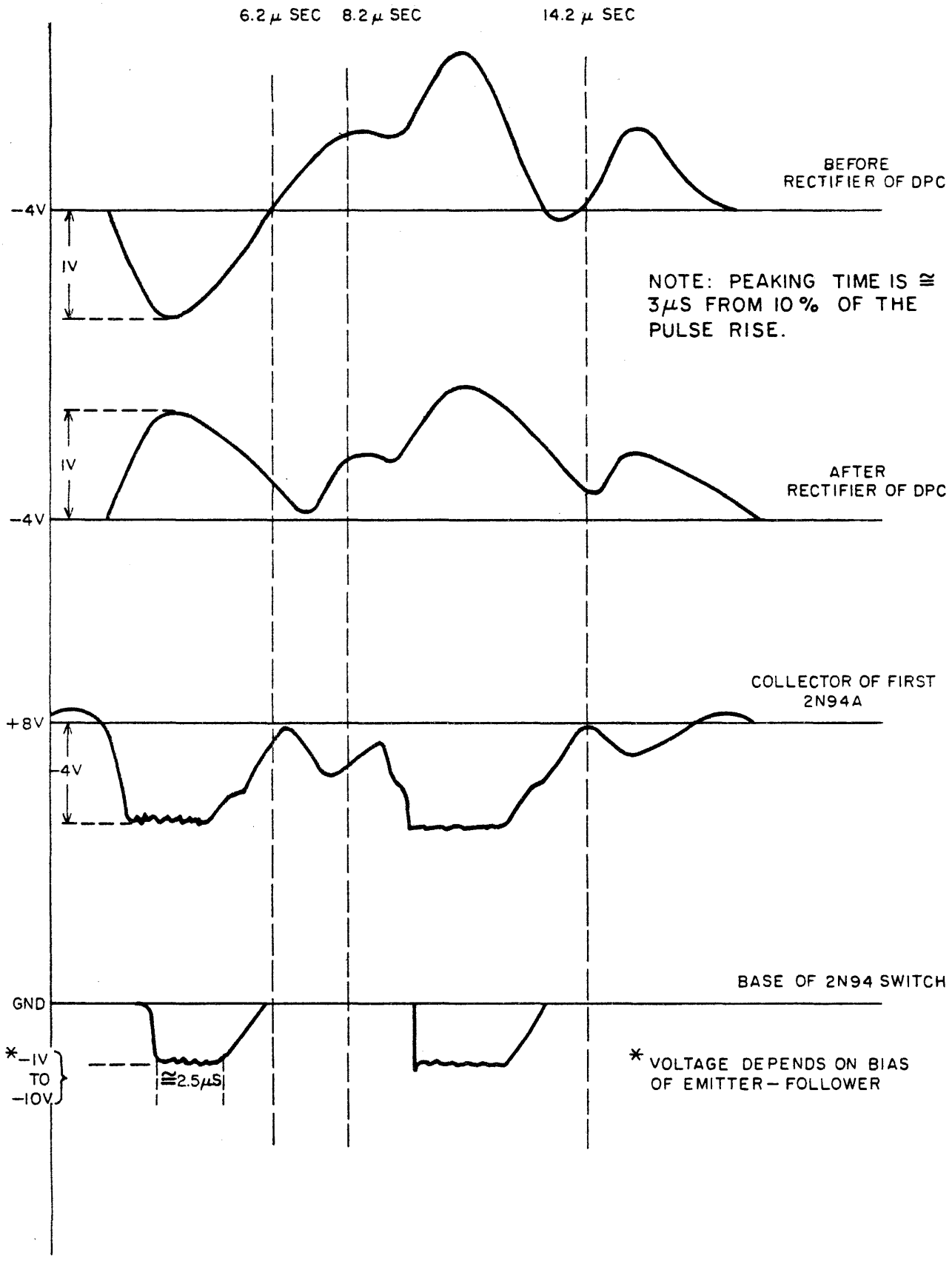


Figure D-9. Readout of a "1" From a Single Core

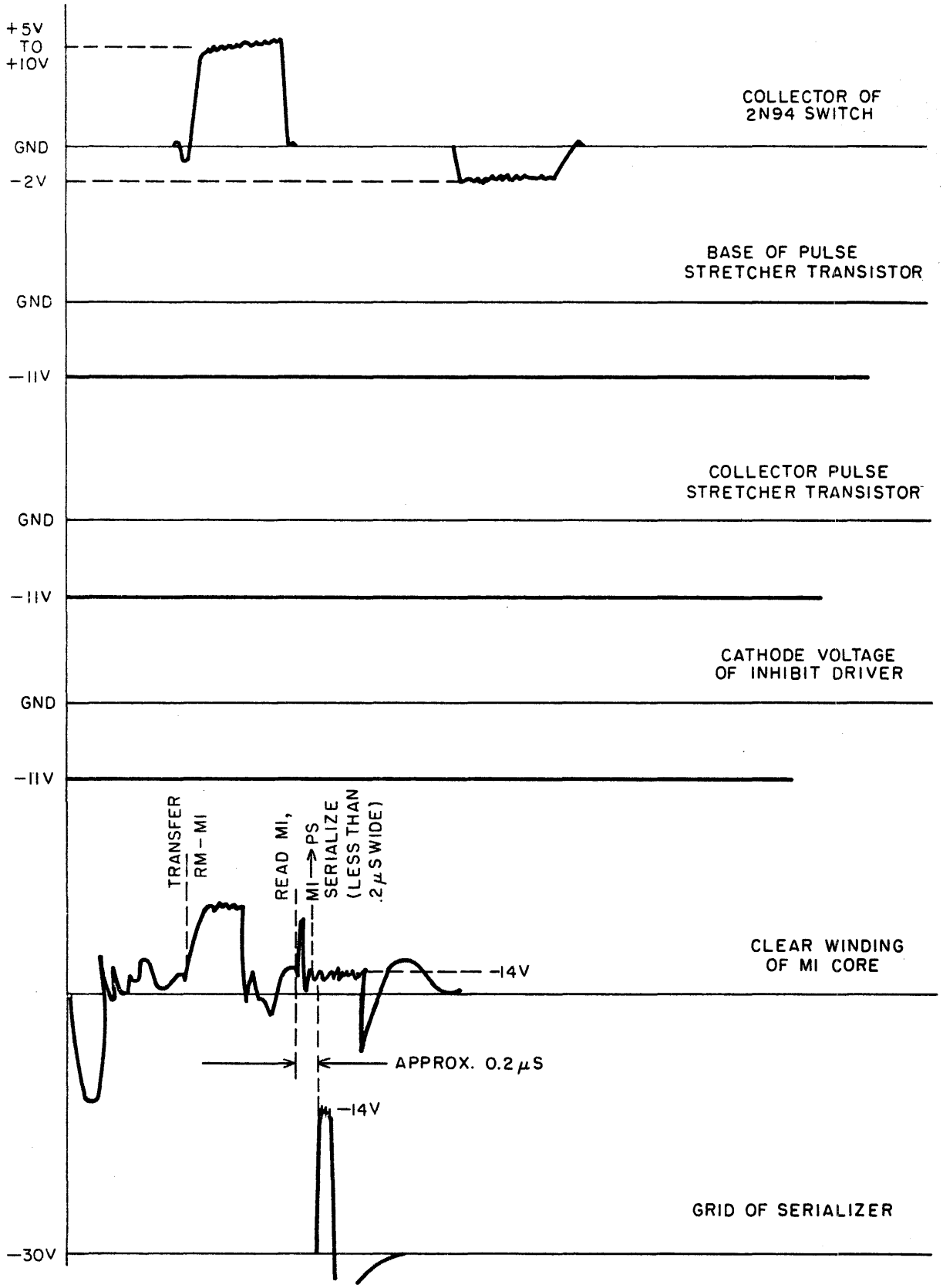


Figure D-10. Readout of a "1" From a Single Core (Cont'd.)

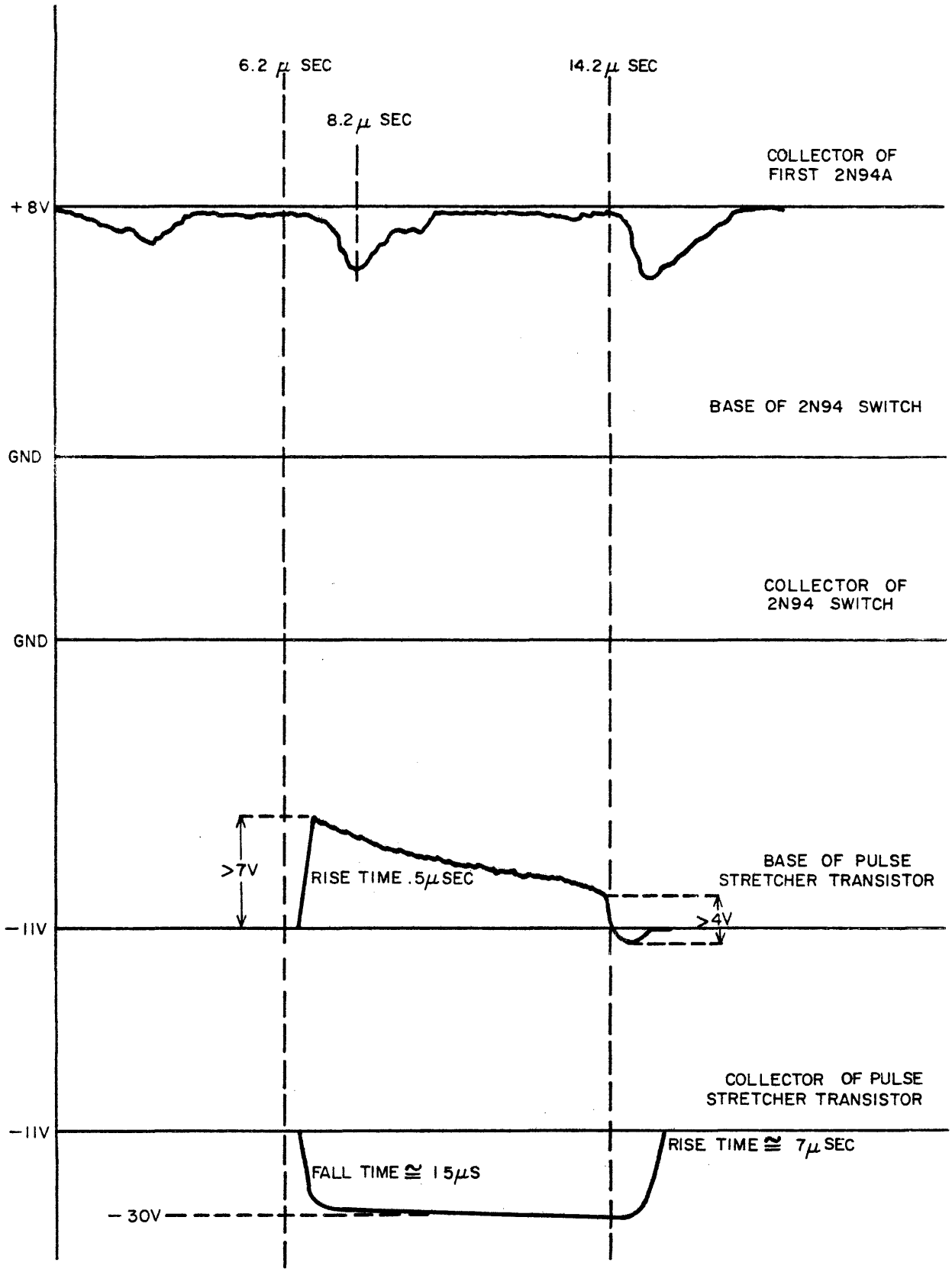


Figure D-11. Readout of a "0" From a Single Core

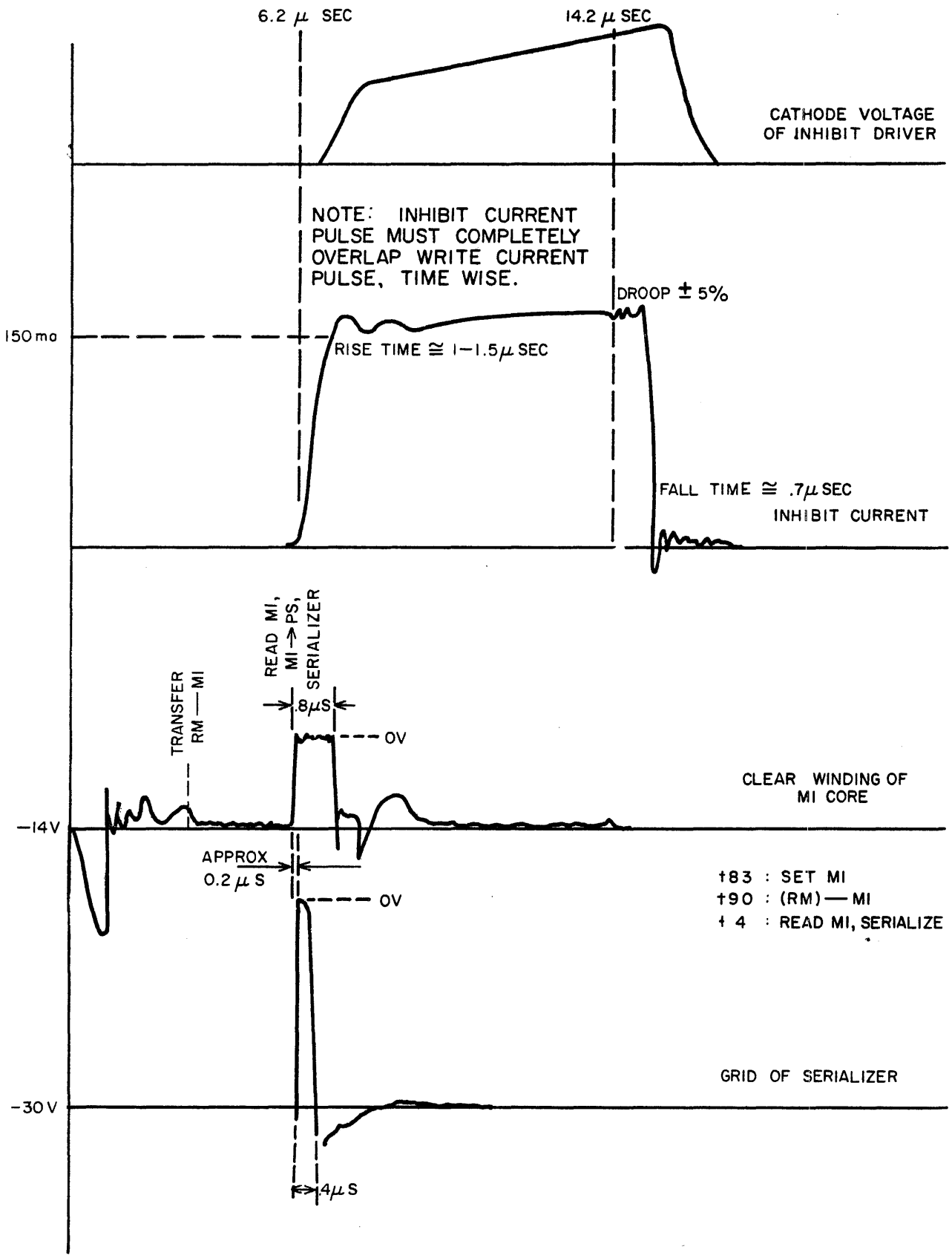
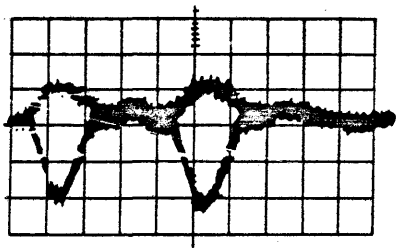


Figure D-12. Readout of a "0" From a Single Core (Cont'd.)

SENSE AMPLIFIER (2000 CORES) WAVEFORMS

-4V

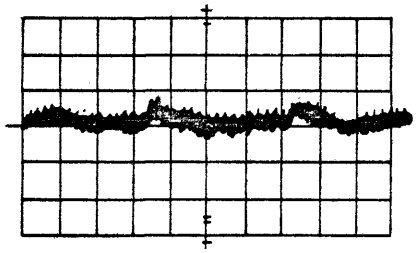
(Scale = 2V/cm.)



MEMORY "1"s (Machine "0"s)
BEFORE RECTIFIER
OF DPC

-4V

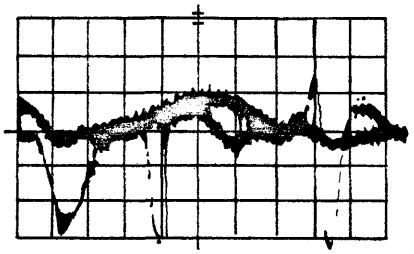
(Scale = 2V/cm.)



MEMORY "0"s (Machine "1"s)
BEFORE RECTIFIER
OF DPC

-4V

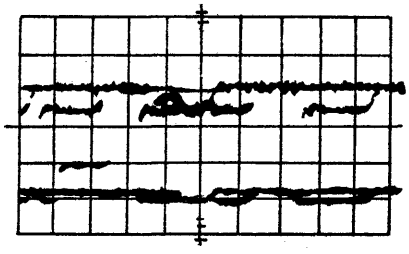
(Scale = 2V/cm.)



"WORST PATTERN" before rectifier of DPC.

(Scale = 10V/cm.)

(Scale = 5V/cm.)



"WORST PATTERN" at base of first 2N94A

"WORST PATTERN" at collector of 2N94 switch

APPENDIX E

SUPPLEMENTAL MAINTENANCE INFORMATION

UNIVAC II

SUGGESTED MAINTENANCE PROCEDURES

1. GENERAL.

The electronic components in the Univac II computer circuits were selected upon their individual merit based on tests that proved their satisfactory performance over a given period of time when used in the manner and for the purpose intended. In all cases only recommended replacements are to be utilized.

2. CAPACITORS.

Care should be taken during soldering so that excessive heat will not damage the insulation and weaken the plate-to-lead contact. Avoid bending the leads close to the case or otherwise imposing any strain on the capacitor body or the leads.

3. DIODES.

In all cases a heat sink, such as a pair of long-nose pliers as shown in Figure E-2, should be employed during, and for a short time after, soldering. Use extreme care in noting the polarity of the diode when mounting. The diodes used in Univac II have the color code nearer the cathode end. Diode lead length should be at least 1/4" long. Extra lead length should be used when possible as indicated in Figure E-2.

Diodes may be checked with an ohmmeter to determine whether they are good, bad, or marginal.

The indications of a bad diode are: no deflection of the meter, indicating the diode is an open circuit; or full scale deflection of the meter indicating

(Continued on Page E-4)

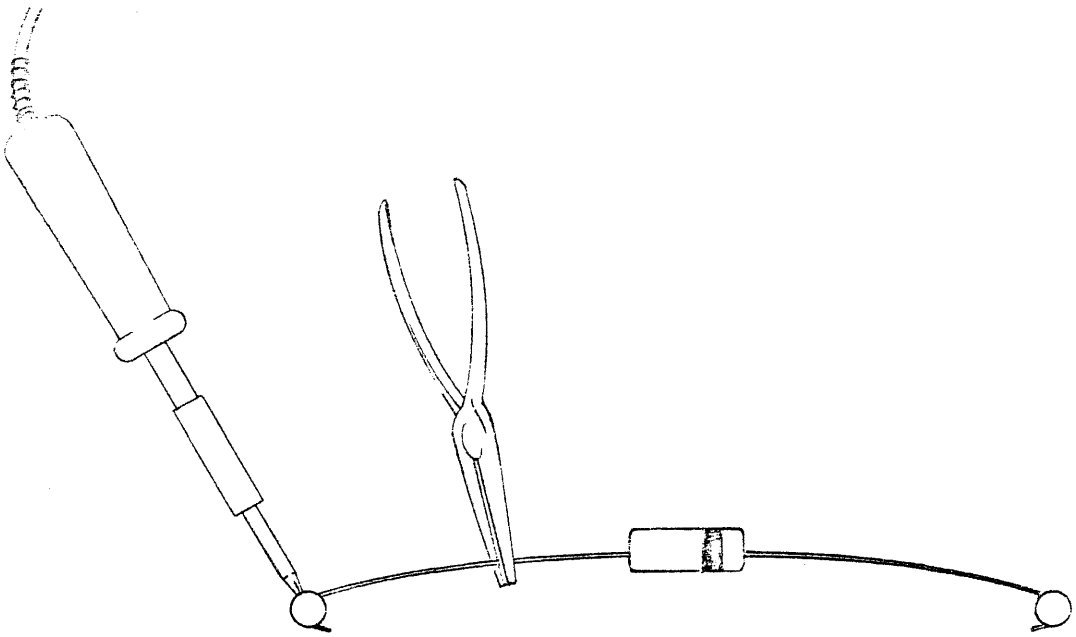


Figure E-1. Heat-Sinking a Diode

a. wrong

b. right

Figure E-2. Mounting Diodes

Table E-1 lists the limits that determine the acceptability of the various tested diodes. These limits were determined with a 20,000 ohms/volt meter. Diodes are to be replaced if they fail to meet these standards

TABLE E - 1

DIODE REPLACEMENT STANDARDS

DIODE TYPE	CLASSIFICATION	TRIPLETT				SIMPSON			
		FWD	SCALE	BWD	SCALE	FWD	SCALE	BWD	SCALE
HD2126 S144G S58 1N58	General Purpose Diode	1000	X1000	100K	X1000	500	X100	100K	X100
S1806 T7G 1N270	Low Enhancement Diode Used In Switch Core Logic On Printed Circuit Chassis	10	X1	50K	X1000	10	X1	50K	X100
1N48	General Purpose Diode Used In Arithmetic And Control Sections	1K	X1000	50K	X1000	300	X100	50K	X100
HD6589	High Back Resistance Silicon Diode	3K	X1000	250K	X1000	1K	X100	250K	X100

(Continued from Page E-1)
the diode is a short circuit. The indications of marginal diodes are: low back resistance, or a decreasing back resistance.

Diodes should also be replaced if, on measuring the back resistance on the highest scale (Triplett X100000 scale, Simpson X10000 scale) there is a definite drift in the reading.

NOTE

Do not grasp the diode with both hands while making resistance checks. Determine that no closed circuit exists between the diode leads. Resistance checks are not always conclusive since the diodes are not tested under operating conditions.

4. RESISTORS.

Avoid bending the leads too close to the resistor or otherwise imposing any strain on the resistor body or the leads. Keep wires away from high-wattage resistors. Resistor lead length should be from 1/4" to 1/2" long. Special care should be taken in handling precision film resistors to prevent nicks or scratches which may cause them to open. The use of insulating tubing is no longer recommended because of the resultant loss in power rating.

5. TRANSISTORS.

At the present time there is no recommended transistor checker other than an ohmmeter. In checking with an ohmmeter, the transistor is looked upon as two diodes with the cathodes tied together, or two diodes with the plates tied together. A check of the individual diode sections is made. A measurement is made assuming one diode exists between base and emitter, and a second between base and collector. Any measurement across these sections indicates whether a short exists. These checks detect only those transistors that are open or shorted.

As in the case of diodes, a heat sink should be used to prevent component damage while soldering, Figure E-1. The transistor leads should be covered with plastic tubing (approximately 1/4") to prevent leads from shorting together. Figure E-3 identifies the leads of the various transistor types.

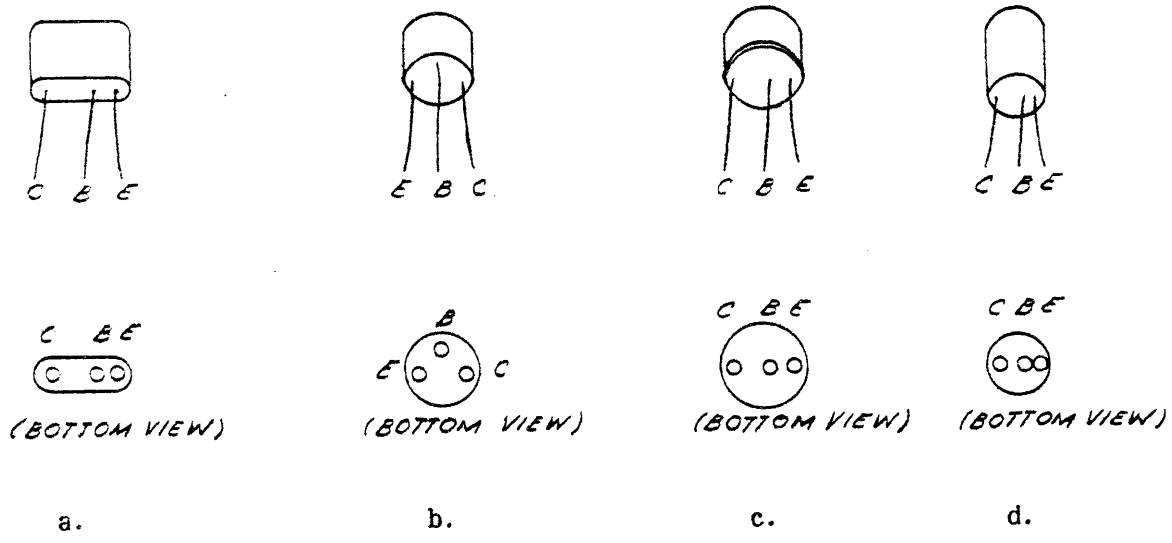


Figure E-3. Transistor Lead Identification

6. DELAY LINES.

Care should be taken when working on chassis containing delay lines to prevent breaking wires on the delay stick. If a wire breaks, and it is near a tap, a loop may be dropped to obtain sufficient wire to solder a new lead. If a tap is moved on a delay line, the capacitors associated with this tap must also be moved.

7. TUBES.

Failing tubes can best be detected by the use of the margin switch in KL corner. This drops filament voltage throughout the machine by approximately 12%, (with the exception of the SR 7AK7's, for which there is a special switch in KL corner). If the computer is well maintained it should be able to run any service routine for 30 minutes without any solid errors on margins. The machine should not be kept on margins for longer than 30 minutes.

If the machine is in such shape that so many errors are introduced that they mask each other, the filament stabilines can be used to lower filament voltage small increments at a time. Use of the stabilines has the disadvantage that it also decreases the servo lumiline supply with the result that loops may drop. An alternate method for lowering filament voltage is to adjust the taps on the large resistors on the roof of the Central Computer. This method permits filament voltage drops of less than the 12% drop produced by the margin switch in KL corner. Marginal checks should be done for at least one-half hour during each maintenance shift.

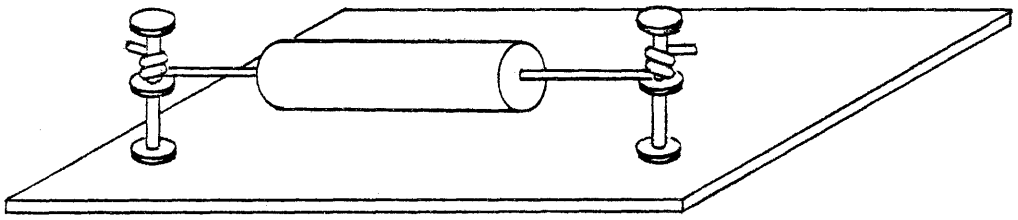
If intermittents develop it is wise to first check for poor solder connections. This is true for both the EM and printed-circuit chassis. If heater to cathode leakage is detected in a tube, the tube cannot be used as a cathode follower; however, it may be used as an amplifier.

8. SOLDERING.

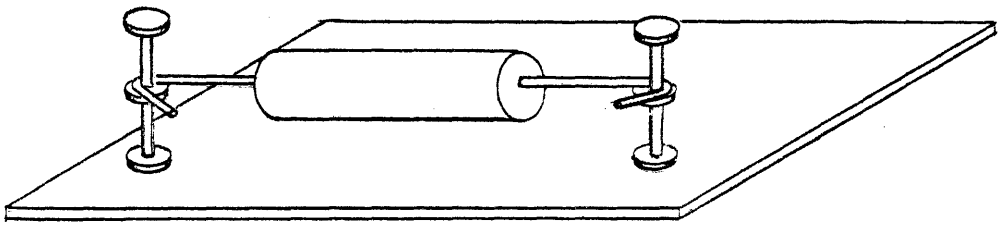
A pencil type soldering iron is recommended for use when soldering components or leads to a printed circuit chassis. A large soldering iron may ruin the copper wiring on the board. Enameled leads of transformers or chokes should be stripped of the enamel before attempting soldering. The recommended method of mounting components on EM chassis prior to soldering is shown in Figure E-4.

9. CONNECTORS.

Clean any dirty pins. It has been noted that damage has been caused to the female 33 pin buggie connectors by inserting test probes into them. For checking voltages or signals at the connectors, it is recommended that a chassis extender be used. Any crushed female pins should be replaced. In the EM chassis bent pins should be reformed. A pair of tube pullers will do this job if no reforming tool is available.



a. Conventional Method of Wrapping Leads Around Stud Terminals



b. Recommended Simplified Method of Attaching Leads to Stud Terminals

Figure E-4.

APPENDIX F

SUPPLEMENTAL MAINTENANCE INFORMATION

UNIVAC II

POWER SUPPLY ADJUSTMENT

1. GENERAL.

This adjustment is proposed as a maintenance procedure to be performed on a monthly basis. The points for monitoring the power supply voltages are located on the d-c voltage terminal board that is mounted in back of bays H and J. A 1/2% meter must be used, and all readings taken at more than 1/2 full scale, thus giving a reading accuracy that has a 1% maximum deviation. Since most circuits in the computer are designed to operate with no more than $\pm$4% voltage deviation, and if a 1% tolerance is allowed for metering error, all adjusted readings should be within $\pm$3%, as a maximum range. As a safety factor, all voltages should be set to within $\pm$2%. This allows a 2% difference for metering error and voltage changes caused by transients. Tolerances shown on the accompanying chart are the maximum allowable and should be reduced whenever possible.

2. ADJUSTMENT.

First adjust the generator voltage. The recommended generator voltage is 208 volts, line-to-line. This voltage should be maintained within 1 volt.

The supply points should be adjusted next. The chassis whose voltages are nearest ground must be set first because they in turn affect the entire stack. In cases where two, three, or four chassis are in parallel, all the supply points must be set on the same respective taps. If not, the current in the chassis becomes unbalanced and may cause a circuit breaker on the chassis to trip. The lower order taps of the chassis effect about a 1 volt change in the

d-c output. The higher order taps effect about a 2 volt change in the output voltage. By observing Figure F-1 and following the procedure outlined, the power supply can be set within Univac II tolerances.

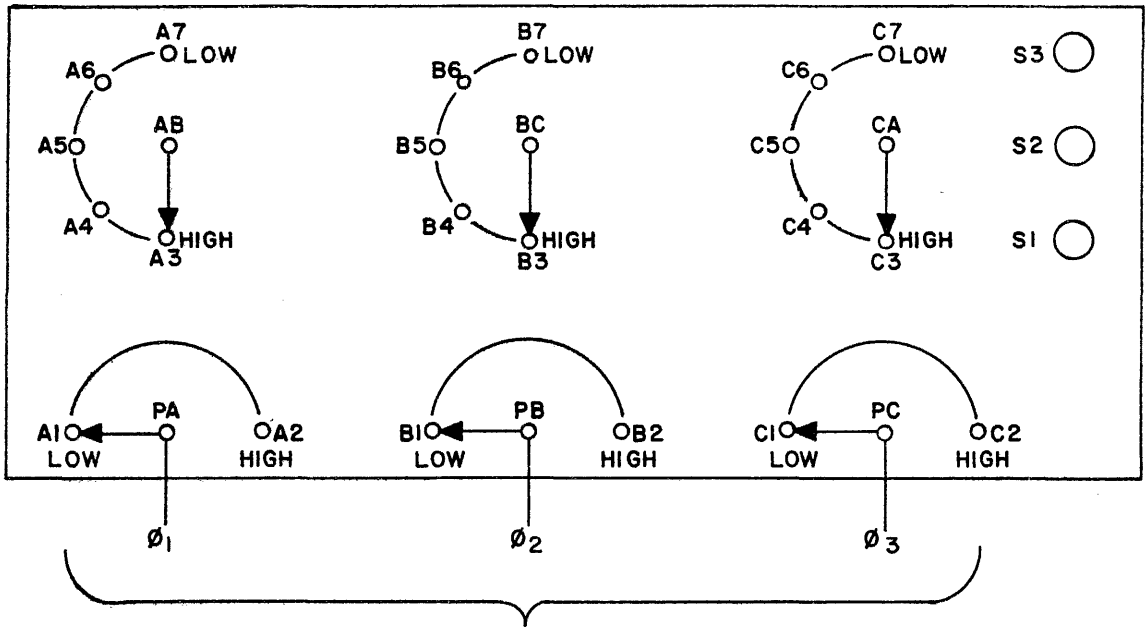


Figure F-1. Front View of Transformer Terminal Board

All 3 upper jumpers must be in the same position. All 3 lower jumpers must also be in the same position. Respective jumpers on parallel chassis must be in the same positions. See Load Lines chart, Figure F-2, for the approximate voltage output for all of the tap settings.

As a general rule, taps 1 to 2 provide 1 volt differences. Taps 3 to 7 provide 2 volt differences. For example, if taps are set at positions 2 and 5 and a 1 volt increase is desired, first move tap 5 to position 6, producing a

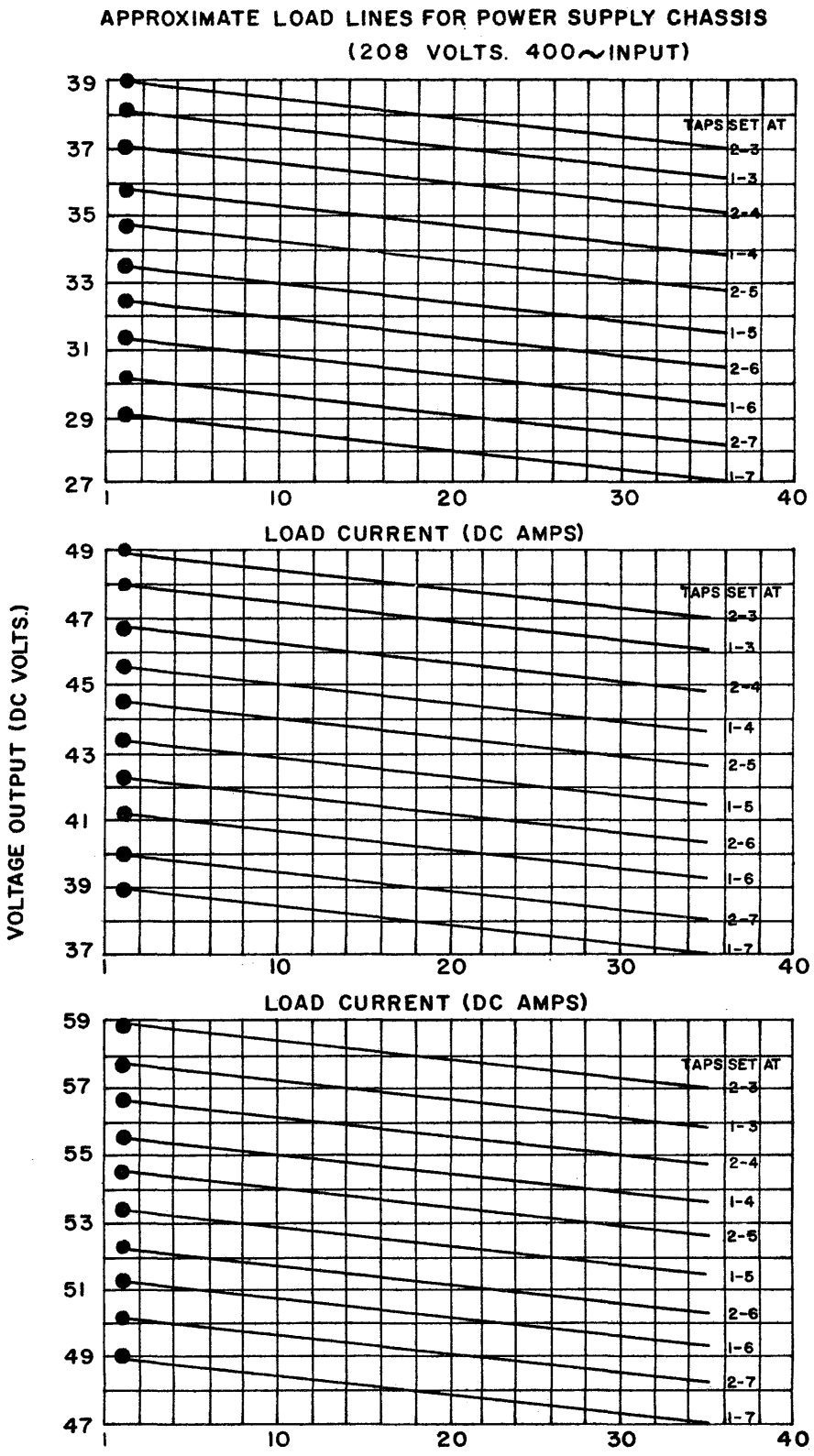


Figure F-2. Power Supply Chassis Load Lines

2 volt increase. Next move the lower tap to position 1, decreasing the output by 1 volt. The net change will be an increase of 1 volt.

Since variances will occur with differences in the number of Uniservos alerted, +600v, the Uniservo brake and clutch supply, is set with half of the Uniservo bank turned on. All other voltages should be adjusted with a minimum of half of the Uniservos turned on, and with the computer performing any service routine or program.

The standby voltages have a tolerance of $\pm$10%. Minus 28 volts is set while d-c is on, and is adjusted to a tolerance of $\pm$1/2 volt from ground.

After proper voltages have been established at the power supply chassis supply points, proper bleeder voltages are determined. This adjustment is performed by moving the slider to increase or decrease the reading as desired. Figures F-3 and F-4 present the voltages along the bleeder lines. Figure F-3 lists the voltages for the positive supplies, and Figure F-4 lists those for the negative supplies. In these charts the chassis supply voltage is first listed, followed by its associated bleeder (B) adjustments, going away from ground. The allowable tolerances for each tap are presented for quick reference. Two columns at the right of these charts are provided for recording pertinent data.

POWER SUPPLY RECORD

VOLTAGE CHECK PTS.		ADJUST CHASSIS OR BLEEDER	VOLTAGE READING		READINGS	DATE REMARKS
REF. VOLTAGE	ADJUST VOLTAGE		NOMINAL	TOLERANCE ±		
0	+30	Y6,Y7, Z6,Z7	30	1.2		
0	+5	B	5	0.2		
0	+8	B	8	0.5		
0	+18	B	18	0.7		
0	+20	B	20	0.8		
0	+40	Z4, Z5	40	1.6		
0	+35	B	35	1.4		
+30	+60	X5, X6, X7	30	1.2		
+40	+50	B	10	0.4		
+60	+70	Y4, Y5	10	0.5		
+60	+66	B	6	0.5		
+60	+90	W6, W7	30	1.2		
+90	+84	B	6	0.5		
+60	+75	B	15	0.6		
+70	+80	B	10	0.5		
+90	+105	Y3	15	0.6		
+105	+95	B	10	0.5		
+105	+120	W4, W5	15	0.6		
+120	+150	X2	30	1.2		
+150	+160	X3, X4	10	0.5		
+150	+165	W2, W3	15	0.6		
+165	+200	V7	35	1.4		
+200	+246	V6	46	1.8		
+200	+255	V5	55	2.2		
+255	+306	V4	51	2.0		
+246	+280	B	34	1.2		
+255	+285	B	30	1.2		
+306	+358	V3	52	2.0		
+358	+410	V2	52	2.0		
+358	+380	B	22	0.8		
0	+600	Y2	600	60.		
0	+48	B	48	4.8		
0	-191_S	Z2	191	19.0		
191_S	-166_S	B	25	2.5		
-191_S	-230_S	B	39	3.9		
0	-28_P	B	28	0.5		

Figure F-3. Positive Section Adjustments

POWER SUPPLY RECORD

VOLTAGE CHECK PTS.		ADJUST CHASSIS OR BLEEDER	VOLTAGE READING		READINGS	DATE
REF VOLTAGE	ADJUST VOLTAGE		NOMINAL	TOLERANCE±		REMARKS
0	−30	T7	30	0.8		
0	−34	U7	34	0.8		
0	−11	B	11	0.4		
0	−14	B	14	0.4		
−11	−14	B	3	0.4		
0	−4	B	4	0.4		
0	−17	B	17	0.6		
0	−20	B	20	0.8		
0	−25	B	25	1.0		
0	−1.75	B	1.75	0.05		
0	−13	B	13	0.5		
0	−15	B	15	0.6		
0	−16	B	16	0.6		
0	−18	B	18	0.7		
0	−21	B	21	0.8		
−34	−40	S6,S7, U2	6	0.5		
−40	−60	T6	20	0.8		
−34	−50	B	16	0.6		
−40	−55	B	15	0.6		
−60	−74	S4, S5	14	0.5		
−74	−88	U6	14	0.5		
−88	−71	B	17	0.6		
−74	−100	T5	26	1.0		
−74	−86	B	12	0.5		
−100	−80	B	20	0.8		
−100	−95	B	5	0.5		
−100	−106	S3	6	0.5		
−100	−120	U5	20	0.8		
−100	−117	B	17	0.6		
−120	−150	U4	30	1.2		
−150	−190	U3	40	1.6		
−100	−161	S2	61	2.4		
−150	−140	B	10	0.4		
−150	−125	B	25	1.0		
−150	−165	B	15	0.6		
−150	−166	B	16	0.6		
−190	−175	B	15	0.6		
−190	−216	T4	26	1.0		
−190	−203	B	13	0.5		
−216	−258	T3	42	1.7		
−216	−229	B	13	0.5		
−258	−300	T2	42	1.7		

Figure F-4. Negative Section Adjustments

APPENDIX G

INPUT-OUTPUT ADJUSTMENT CRITERIA

1. INTRODUCTION.

The information provided herein is submitted as a guide to the installation and field engineers and contains the criteria of adjustment of input-output for Univac II. It includes necessary guides for use of plastic tape. Background information is provided for use when questions arise which have not been covered.

Univac I input-output standards have been used where applicable, however, one cannot necessarily expect the same performance. In some ways there are improvements while in others there are not. For example: plastic tape will probably be noted immediately as being poorer with respect to drop-outs, also operation at doubled densities does not increase margins even with metal tape, etc.

It is expected that maximum performance will be obtained when the input-output system is adjusted as specified herein; if this is not the case, specific complaint should be made to Continuation Engineering, Univac II.

2. SYSTEM EVALUATION.

What should be checked, how often and for what values?

a. WRITE CURRENT. - The write currents should be checked weekly if plastic tape is being used and monthly if not. The method of checking:

(1) Pick up a metal tape write on any servo.

(2) Measure the voltage at the plate of the write driver (approximately +0.88V).

(3) Remove the associated 28D7; the voltage at the plate of the driver should remain the same except with a negative polarity. Adjustment is made with the cathode resistor of the driver.

(4) The tolerance is ±1% or approximately 0.01 volt. Use care in making these adjustments. The symmetrical write waveform which will result will improve resolution.

b. READ AMPLIFIER GAINS. - ALWAYS MAKE SURE THAT THE HEADS ARE CLEAN AND THAT THE DYNAVAR IS TIGHT IS TIGHT AND CLEAN BEFORE ADJUSTMENTS ARE MADE. The calibration tape to be used is a standard Univac calibration tape written at 128 ppi. Before use, the calibration tape should be checked by comparing the first recorded area with the second recorded area. (See ESD Service Manual Section USE 30.01.52). If the variation is any greater than 10% on any channel, the tape should be replaced. Read gains should be checked monthly.

(1) Make sure the amplifier noise is below the acceptable level (see Section C-1).

(2) Potentiometer V2 on A3T should be adjusted for +350V at A3T7 using A3T7 using a 1/2% meter. Potentiometer V4 on A3T should be adjusted for minimum ripple at A3T7 as observed on the scope.

(3) Check to see that the ratio of plastic to metal gain is 1.6:1. If the ratio has deviated by more than 10%, check the value of the feedback components in the cathode of the first tube of the amplifier. Be sure to include the switching transistor in your check.

(4) The amplifier should be capable of delivering 180V p-p without distortion.

(5) The calibration is accomplished by observing the amplifier output at the TT11's on A4 & 5T while running a calibration tape forward and adjusting the read attenuator in the Uniservo for metal calibration level.

(6) Calibration level is the percentage level of the calibration tape times the nominal level. Nominal level at metal gain is 70V p-p; a 120% calibration tape then would have a calibration level of 1.2 x 70 = 84V p-p.

(7) Heads which cannot be calibrated by using the Uniservo read attenuator should be returned for replacement. A check of the amplifier gain may be made by plugging the suspected channel into other channels and comparing gains.

c. NOISE

(1) READ AMPLIFIER

(a) 60 cycle hum at the input to the Schmitt triggers (TT11's, A4-5T) should be less than .6V p-p at normal gain with the Uniservo read relays picked up. If the hum is excessive try changing the amplifier tubes. The first tube should be a 6AU6 with an A on it. The second tube is a 6AU6 with an A or B stamped on it. The cathode follower may have excessive heater to cathode leakage - change it if necessary. Check gains after changing tubes. Shields should be on the first and second tubes.

(b) The pre-amp subchassis may be touching the main chassis. This can cause spurious noise and the pickup of ground noise. The subchassis should also be free to move to reduce vibrational pickup.

(2) LINE. - No more than 2V zero to peak of noise should be observed at the input to the Schmitts due to any cause. The items in this section indicate areas to investigate should this figure be exceeded.

(a) All Jones plugs and amplifier connectors should be locked in position firmly.

(b) There should be no grounds on the read cable shield except at A1 & 2T. The shields should be continuous. The inner and outer shield in the cable from A1 & 2T to the first servo should be insulated from each other

at the servo end. Only the inner shields should be continued into the trellis via JPR-18.

(c) Maximum separation should be maintained between the read cables and others, both on the trellis and in the gooseneck. See print XG142625 or XG142623 for cable placement in gooseneck.

(d) Each trellis section should be bonded firmly (2 places) to the preceeding section. The first trellis section should be firmly bonded to the computer frame.

(3) UNISERVO

(a) Measures should be taken to insure that all other cables are removed from the proximity of the read cable at all times.

(b) A considerable number of arc and/or noise suppressors are provided in the servo. The malfunction of any of these may result in system noise. Check for cold solder and no solder joints. Turning a servo off and on with a read picked on any other servo should not result in any more than the maximum noise.

(c) Excessive write crosstalk may occur due to a failure of a read relay in the writing servo. The read relays are required to short out the read transformers when non-energized. Occasionally the normally closed contacts do not make - write crosstalk results.

(d) Write crosstalk and servo operational noise should be checked semi-annually.

(e) Due to the short inter-block space the start read signal may occur before the read relays are settled. This usually results in a pickup in the first character read in. It can be eliminated by changing read relays. It is believed to be caused by contact bounce, ie. even though a closed circuit is made by the mercury, the platinum contacts bounce several times; this

bouncing produces a voltage in the order of 1/2 mv between the contacts. Check DF607 and DF605A & AA to make sure that the start read is not occurring too soon.

(f) The tape tension should be checked monthly. (See Uniservo Manual.) Dirt should be removed from the loop box screens. Check daily.

d. SKEW. - Detected during operation by a bit moving from one character to the adjacent one.

(1) Intra-system skew can be checked by writing on all ones tape and observing the time relationship between each channel and the sprocket on a dual trace scope while reading the tape on each servo in turn. Generally, no more than 7 microseconds time difference should be observed. The remaining portions of this section deal with methods of improving skew.

(2) The front panel of the Uniservo should be properly aligned.

(a) The complete slignment should be checked semi-annually. See Uniservo manual for procedure.

(b) The width of the tape guides should be checked every time the guide assembly is cleaned. A go no-go gauge is available for this purpose. See Uniservo manual.

(3) Check write currents per Section A1.

(4) If mechanical and electrical checks do not make a satisfactory improvement the heads can be checked roughly by repeating 1.4.1 using one Uniservo only and checking each head on that Uniservo. The time displacement should not be greater than 4 microseconds.

e. SCHMITT TRIGGER (should be checked monthly).

(1) The bias (measured at TT11) should be 37.5 volts and is best measured with a DC scope calibrated with machine voltages. The tolerance is $\pm$4%. If a deviation of greater than 4% is observed check machine voltages,

change the 6AL5 and try replacing the precision components in the divider.

(2) A Schmitt trigger exhibits hysteresis, i.e. it sets at one input voltage and resets at another. The first happens to be higher than the second. The bias mentioned in 1.5.1 is so adjusted that the Schmitt sets when the input AC signal reaches +7V and resets (produces an output) when the signal passes through zero from positive to negative. These levels must be maintained within a $\pm$5% tolerance in order to minimize skew, drop-out and noise. The set and reset should be checked monthly. They can be observed with a carefully calibrated DC scope (use machine voltages for calibration) by probing at the first grid of the input tube. Two notches will be observed on the positive going waveform. The top of the first is the set and the bottom of the second the reset. The set is 44.5V $\pm$5% and the reset 38.5V $\pm$5%.

f. DYNAVAR

(1) Dynavar is used to extend the life of the head, reduce dirt accumulation on the head and maintain a constant output and skew from the head.

(2) Dynavar necessitates higher amplifier gain and reduces resolution.

(3) Tension must be maintained on the dynavar. Dirt must be kept from beneath it. This should be checked daily.

(4) Care must be taken to align the dynavar so that it runs squarely across the head.

g. DELAY FLOP TIMING

(1) All delay flops should be adjusted as accurately as possible. The running tolerance is $\pm$5%. They have a tendency to drift toward longer delays, so that in adjusting the best procedure would dictate an adjustment slightly below nominal.

(2) When adjusting delay flops the time base of the scope should be calibrated with the 60 cycle power waveform or "t" pulses from the machine. Do not rely upon the scope calibrator or the markings upon the dials.

(3) Some delay flop times are very critical and should be examined twice a month. These are:

DF603B	DF605A
DF604B	DF605AA
DF607	DF679
DF607B	DF681
DF605B	TF612B
DF605BB	

(4) The rest of the delay flops should be checked monthly.

h. TAPE

(1) METAL

(a) The maximum tape noise allowable is 8% or .08 x 70 = 5.6V p-p.

(b) Tapes have a minimum signal output of 40% or .4 x 70-28V p-p.

(c) Tapes may exist with a maximum signal of 200%. Maximum level is now 125% but was not imposed on early tapes.

(d) Signal variation may be permitted on a single channel, from one channel to the next or both as long as the variation does not exceed the limits stated above.

(e) Resolution (the ratio of the amplitude of successive pulses to the amplitude of the first pulse) should not be less than 80% on a Univac II. The inspection level is 90%. However resolution is poorer on Univac II than on the tape tester.

(f) Bad spots should be marked in accordance with SP374.

(g) Splicing should be done in accordance with SP97.

(h) Tape Testing.

1 Where possible a tape tester should be used as tape testing is a very inefficient use of a computer.

2 If a tester is not available, computer test of metal tape can be accomplished by using an appropriate routine which writes as near solid information as possible. The test should be run three times on the same piece of tape to help insure a complete test of the tape i.e. to insure test of the space between blocks.

3 Tests should be run at the highest computer density with read back in the backward direction at low gain.

(2) PLASTIC

(a) The maximum allowable tape noise is 5%, which is better than for metal tape, making possible the use of a plastic gain switch.

(b) The inspection signal levels have 120% as the maximum and 40% as the minimum.

(c) The average signal level is generally much more constant with plastic tape.

(d) Resolution to be expected with plastic tape on Univac II is in excess of 60%.

(e) The oxide surface cannot withstand abuse, therefore extreme care should be used when handling the tape.

(f) Bad spots should be marked in accordance with SP284.

(g) Splicing should be done in accordance with SP283.

(h) Plastic tape can be field tested per 1h above.

i. HEADS

(1) READ-WRITE

(a) Read-write heads should be mounted with care. Make sure that there are no dirt or burrs which might tilt the head.

(b) Dirt should be removed from the head daily with a clean finger or a soft tissue.

(c) The head cables should be locked to the head and placed as far from the center-drive as possible.

(2) ERASE

(a) The top of the erase head should attract the North seeking point of a compass.

(b) The spacing between head and tape should be 1/32" and should be checked monthly.

(c) There should be no foreign material between the pole pieces. Check monthly.

3. INPUT-OUTPUT MAINTENANCE SCHEDULE (Extracted from the Preceding).

a. DAILY CHECKS

(1) Dynavar Tension.

(2) Clean Read-Write Head.

(3) Dirt in the Loop Box Screens.

b. WEEKLY CHECKS

(1) Write Current (if using plastic tape).

c. SEMI-MONTHLY CHECKS

(1) Delay Flops.

d. MONTHLY CHECKS

(1) Write Current (if plastic tape is not being used).

(2) Read Amplifier Gains.

(3) Schmitt Trigger.

(4) Delay Flops.

(5) Erase Head.

(6) Tape Tension.

e. SEMI-ANNUAL CHECK

(1) Uniservo mechanical alignment.

(2) Write crosstalk and Uniservo operational noise.

f. MISCELLANEOUS

(1) Width of tape guides should be checked whenever guides are cleaned.