DR2604

SPERRY
DCP FAMILY

MACRODIAGNOSTICS SOFTWARE DESCRIPTION

NOVEMBER 1985
CUSTOMER ENGINEERING

SPERRY

HC8-2	DR2610-01/-02/-03 DR2615-01/-02/-03 DR2611-01 DR2626-01

CAUTION

Semiconductors and assemblies which contain them can be damaged by static electricity. Therefore, handle all semiconductors and printed circuit assemblies as if they will be damaged by static electricity. Use cautions and procedures that are contained in maintenance manual SP4045.

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SPERRY

HANDBOOK CHANGE BULLETIN CUSTOMER ENGINEERING

BOOK: DR2604 SPERRY
DCP Family Macrodiagnostics
Software Description

EFFECTIVE DATE: April 10, 1987

HCB-2

DSTB/TDN REFERENCE:

None.

DIAGNOSTIC RESTRICTION NOTICE:

NOTICE

THIS HCB SUPPORTS DIAGNOSTICS ENHANCEMENTS AVAILABLE WITH THE MEDIA RELEASE LEVEL(S) INDICATED BELOW.

DO NOT

INCORPORATE THIS HCB INTO THE BOOK UNTIL THE DIAGNOSTIC MEDIA IS UPDATED TO THE RELEASE LEVEL(S) SUPPORTED.

BOOK	HCB LEVEL	MEDIA RELEASE LEVEL(S)
DR2604	2	5.1

DESCRIPTION OF CHANGES:

NOTE: Data change locators (vertical bars in margins) are not used in this revision to the book.

Changed diagnostic media numbers on title page.

Added references to DCP/15 and diagnostic release level and made minor editorial changes throughout the book.

DESCRIPTION OF CHANGES: (cont)

Section 1. Introduction
Changed description of program structure, updated document list and test media list, and revised glossary.

Section 2. Macrodiagnostic Program Load
Added new console procedure errors.

Section 4. Serial Line Module Diagnostic Test
Revised test procedure.

Section 5. Parallel Line Module Diagnostic Test
Added instructions for viewing buffers.

Section 6. Twisted Pair Line Module Diagnostic Test
Section 7. Cartridge Disk Diagnostic Test
Added to the book.

Section 9. System Test
Revised test procedure.

Section 11. U10 Magnetic Tape Diagnostic Test
Added to the book.

Section 12. Host Channel Interface Diagnostic Test
Revised test procedure.

Section 15. Copy Utilities
Revised IFDC copy procedure. Added diskette copy procedure.

INSTRUCTIONS:

All pages are labeled: Rev. HCB-2.

Replace the entire contents of DR2604 with the attached new pages. Retain this HCB cover sheet behind the book's title page.

INSERT THIS HCB COVER SHEET IN DR2604 IMMEDIATELY FOLLOWING THE TITLE PAGE.

SYSTEMS APPLICATION

90/25, 90/30, 90/30B, 90/40
90/60/70, 90/80, 90/80 Extended,
1106, 1108, 1100/10, 1100/20,
1110, 1100/40, 1100/80, 1100/80A
1100/60 (Vanguard)

HANDBOOK APPLICATION

HB2365 SPERRY DCP/20/40
Types 8597/8596
Primary Mode
Diagnostic Programs

REVISION STATUS

PAGE(S)	REVISION HCB
iii/iv	2
v thru x	2
1-1 thru 1-9	2
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SR 1741 - 3 block mux

ILLUSTRATIONS

TABLES

1. INTRODUCTION

1.1. General

This manual describes the DCP family macrodiagnostic software, Release 5.1. Software releases prior to 5.0 use DR2556, DCP/40 Type 8596 and DCP/20 Type 8597 Primary Mode Macrodiagnostic Software Description as the supporting document.

The manual is divided into the following sections:

- Section 1. Introduction

  Presents general information about the purpose and content of the document and how to use it. Includes an overview of the macrodiagnostics, general error information, a description of the equipment that is tested, and reference material.

- Section 2. Macrodiagnostic Program Load

  Describes the F1 menu, load sequence and load procedure, error isolation for load failures, the maintenance panels of the DCP/40 and the DCP/20, the operator panels of the DCP/10/10A and the DCP/15, and the console screen display.

- Sections 3 through 13. Individual Tests

  Describe the purpose and content of each diagnostic test, the test procedure, and the error codes and messages.

- Section 14. Local Language Translate

  Describes the local language translate program which facilitates the translation of diagnostic messages from Customer Engineering Technical English (CETE) into the language of the user.

- Section 15. Copy Utilities

  Describes the copy utilities for the integrated flexible diskette controller (IFDC) and the flexible diskette drive (Diskette Subsystem Type 8406-00/-03).

- Section 16. Resident Utilities

  Describes the numerous resident utility programs.

- Appendix A. Trouble Isolation Procedures

  Presents trouble isolation procedures that are keyed to the error codes and messages of the individual tests.

- Appendix B. Supplemental Information

  Contains information that is helpful in troubleshooting equipment failures. Includes Error Indicator Analysis (EIA) procedures and descriptions of the content of the error registers following hardware errors, specification exceptions, and process control conditions.

1.2. Diagnostic Overview

The DCP Family diagnostic package is divided into the following test levels:

- DCP/40

  Microlevel ROM routines which operate at the microcode level and perform the power-on confidence (POC) tests. The CP and CLC execute the tests whenever power is applied or the system is initialized by the SYSTEM RESET switch.

  Microdiagnostics which isolate errors in the CP, the CLC, the local storage module, the integrated diskette controller (IDC/IFDC), the BIOC line module, and the parallel line modules. The test programs are loaded from the integrated diskette.

  Macrodiagnostics which are used after successful completion of the microdiagnostics and include macrolevel routines for the CP, the CLC, local storage, and serial and peripheral line modules. The test programs are loaded from the integrated diskette.

- DCP/20

  Microlevel ROM routines as described for the DCP/40. Processing functions are handled by the CLC in the processor mode.

  Microdiagnostic tests as described for the DCP/40.

  Macrodiagnostic routines as described for the DCP/40.

- DCP/10/10A and DCP/15

  Microlevel ROM routines as described above. Processing and I/O functions are contained on a single PCA, the processor/storage PCA.

  Macrodiagnostic tests as described above.

1.3. Macrodiagnostic Program Overview

The macrodiagnostic software tests the peripherals (line modules and devices) and the communications interfaces. It verifies memory operations and tests the entire system under maximum load to trap failures. It is primarily a function test and does not isolate failures to a hardware component level. In addition to the diagnostic tests, the macrodiagnostic program provides copy utilities and resident utilities. Refer to the table of contents for a listing of the specific tests and utilities.

1.3.1. Macrodiagnostic Program Structure

The macrodiagnostic program has four main parts: the bootloader program, the system executive program, the diagnostic tests, and the utility programs. The equipment applications and media numbers of the macrodiagnostic program are:

- DCP/40/20: Diskette #1, DR2610-01
  Diskette #2, DR2610-02
  Diskette #3, DR2610-03

- DCP/10: Diskette #1, DR2615-01
  Diskette #2, DR2615-02
  Diskette #3, DR2615-03

- DCP/10A DR2611-01 (contains complete program)

- DCP/15 DR2626-01 (contains complete program)

1.3.2. General Error Information

The program reports errors in two ways: the maintenance panels of the DCP/40/20 and the operator panels of the DCP/10/10A/15 display hexadecimal error codes; the console displays error messages, which may include an error code.

Numbers which are preceded by an X are hexadecimal values. Unless indicated otherwise, bit numbering is defined from left to right, with the most significant bit (MSB) on the left and the least significant bit (LSB) on the right.

1.4. Equipment

The macrodiagnostic software tests the following types of equipment:

- DCP/40 Type 8596-00 (pre-serial split) and the DCP/40 Type 8596-01 (serial split with 64 kbytes of RAM and breakout panel)

  The maximum DCP/40 configuration contains the basic DCP/40 cabinet and three expansion cabinets Type 1945. It can handle up to 256 communications ports and can supply up to eight megabytes of memory.

- DCP/20 Type 8597-00 (basic cabinet) and the DCP/20 Type 8597-01 (expansion cabinet)

  The maximum DCP/20 configuration contains the basic DCP/20 cabinet and two expansion cabinets. It supports up to 48 communications ports and supplies up to 512 kilobytes of memory. Type 8597-02 provides memory expansion to two megabytes.

- DCP/10, which consists of the communications processor Feature K4035-00/-01 and the optional Cabinet Type 1986

  The DCP/10 has eight communications ports and up to 512 kilobytes of memory. It can be configured in a separate cabinet, or rack-mounted, or integrated into a host processor with the Front End Processor Interface (FEPI) Line Module F3882.

  The DCP/10A (Feature K4035-02, Cabinet Type 1986-01) provides memory expansion to two megabytes and contains the Multiple Device Line Module (MDLM) F3893 which supports a 5.25-inch diskette load device and a 5.25-inch rigid disk.

- DCP/15, which consists of the communications processor Feature K4035-03 and the optional Cabinet Type 1986-01

  The DCP/15 provides the same configuration possibilities as the DCP/10/10A. It contains up to 14 communications ports and provides a maximum of four megabytes of memory. The DCP/15 also supports an optional 5.25-inch diskette drive and an optional 5.25-inch rigid disk.

1.5. Reference Documents and Diagnostic Media

The reference documents are:

HB2345	SPERRY DCP/40 System Servicing
HB2346	SPERRY DCP/20 System Servicing
DA-3076	SPERRY Series 1100 Systems, Peripheral Test Sequencer (PTS) Test Description
DA-3077	SPERRY Series 1100 Systems, Peripheral Test Sequencer (PTS) Offline Operator's Reference
DA-3078	SPERRY Series 1100 Systems, Peripheral Test Sequencer (PTS) Online Operator's Reference
DR2547	SPERRY DCP/40 Type 8596 Microdiagnostics Software and Procedures Description
DR2555	SPERRY DCP/20 Type 8597 Microdiagnostics Software and Procedures Description
MR6328	SPERRY DCP/40 Type 8596 Troubleshooting Guide
MR6359	SPERRY Cabinet Type 1986 with DCP/10 Feature K4035 Servicing
MR6409	SPERRY Disk Subsytem Type 8409 Servicing
MR6419	SPERRY Cabinet Type 1986-01 with DCP/10A Feature K4035-02 Servicing
MR6471	SPERRY Cabinet Type 1986-01 with DCP/15 Feature K4035-03 Servicing
MR6472	SPERRY DCP Line Module Features Servicing
UP-9778	SPERRY DCP/10 System Trouble Isolation Guide
UP-10827	SPERRY Trouble Isolation Guide for the DCP/10, DCP/10A, and DCP/15

The diagnostic test media are:

DR2610	CPA Family Macrodiagnostics R5.1 (DCP/40/20)
DR2611	CPA Family Macrodiagnostics R5.1 (DCP/10A)
DR2615	CPA Family Macrodiagnostics R5.1 (DCP/10)
DR2626	CPA Family Macrodiagnostics R5.1 (DCP/15)

1.6. Glossary

The following terms and acronyms are used in this manual:

Associate	To connect related items together.
Bypass	To use an alternative path between two points.
BILM/BDBI	The byte interface line module, also known as the bidirectional byte interface line module
BIOC	The byte input/output controller line module
Configure	To establish a configuration.
CLC	The communications line controller which controls input/output between the terminal or peripheral device and the DCP memory. This processor is also called the input/output processor (IOP).
CP	Communications processor or central processor
CPA	Communications processor architecture
Data file	A file in the Series 1100 which contains one contiguous order of information. Usually a sym (print) file when referenced in this document.
Directory	A collection of items in a specified order, as in Disk Directory.
DCP	Distributed Communications Processor
DPER	Diagnostic Procedures for Error Resolution is a troubleshooting technique which uses non-loadable software and procedures to detect a hardware error when the EIA procedure does not indicate an error or solution.
ECC	Error correction code
EI	External interrupt
EIA	Error Indicator Analysis is a troubleshooting technique that does not require software. This procedure uses the maintenance panel to indicate possible PCA failures, taking advantage of hardware through-checking.
EOF	End of function
ESI	Externally specified index

Executive (Exec)	Diagnostic routine which controls loading and service requests for diagnostic tests.
FEPI	Front-end processor interface
ID	Identifier, as in line module ID.
IFDC	Integrated flexible diskette controller
Index	A sorted list of items, as in Message File Index.
IOP	Input/output processor (see CLC)
ISB	Interface Status Byte
ISI	Internally specified index
Logical block	Term used in documentation of the Small Computer System Interface (SCSI). A logical block is one sector of data. On the rigid disk, the logical block is 256 bytes. On the diskette subsystem, the logical block is 512 bytes.
Logical block number (LUN)	Term used in documentation of the SCSI. The LUN is the device which is connected to the target (controller).
Logical unit address	Term used in documention of the SCSI. The logical unit address is the device address.
Line module	One, two, or three PCAs that are used for either serial or parallel connections to peripheral devices or terminals. The PCAs are located in the CLC line module chassis.
Menu	A list of choices, as in Menu of Diagnostic Tests.
MDLM	Multiple device line module
P address	Program address
Port	The point of exit or entry of data in a microprocessor device. In the DCP, it is the logical position to which an I/O is addressed. It can be a hexadecimal line module ID. As such, the port number will automatically include the CLC number. For example, port number X25 is the same as CLC 2 port 5.
Port Processor (PP)	A line module which is supported by the processing power of the microcontroller in the CLC (IOP). Also referred to as a virtual processor.

Process Control Event	A condition which is not an error but must be resolved by the program executive before normal processing can continue.
Program file	A mass storage item that resides in a Series 1100 and contains one or more elements of either symbolic, relocatable, absolute, or omnibus type.
PSB	Peripheral Status Block
PTS	Peripheral Testing Sequencer (Series 1100 diagnostics package)
Resolution	A solution.
ROM	Read-only memory
SCSI	Small Computer System Interface
SDT	Start-data-transfer instruction
Segment	A part of a software program or of storage which has specific limits.
Specification Error	A condition that does not comply with the architectural requirements of the DCP.
Target	Term used in SCSI documentation to indicate the controller.
Time-out	A condition where a process was suspended because an input was not received in a specified period.
Troubleshoot(ing)	To locate trouble and make repairs in mechanical or electrical equipment.
WAR	Working Address Register

1.7. Diagnostic Software User Report (DSUR)

The diagnostic software user report (DSUR, Sperry form SCI-1943 shown in Figure 1-1) is the means of communication between the customer engineer and the diagnostic and prognostic development group. Use the DSUR to report problems in the diagnostic programs and procedures and to convey comments, ideas, or suggestions for improving their quality and accuracy. The form contains instructions for completing it and forwarding it to the diagnostic development group. Obtain the DSUR forms from the Sperry Customer Engineering branch offices.

INSTRUCTIONS ON REVERSE SIDE OF LAST PAGE
SEND PARTS 1, 2 & 4 WITH CARBON LEFT IN. PART 4 WILL BE RETURNED WITH REPLY

SPERRY

DIAGNOSTIC SOFTWARE USER REPORT

1. INITIATOR'S NAME	2. BRANCH LOCATION	3. PHONE AREA CODE, NO.	4. DATE PREPARED	5. NO. 67764
6. COMPUTER	7. FCO LEVEL	8. OPERATING SYSTEM IF ON-LINE	9. O.S. REV. LEVEL	10. HARDWARE COMPONENT	11. COMP. FCO LEVEL
12. MICROCODE SYSTEM ___ MICRO-DIAG ___	REV. LEVEL	13. EMULATOR	14. REV. LEVEL	15. DIAGNOSTIC SOFTWARE PROGRAM	16. COMPONENT NAME	17. REV. LEVEL

18. PROBLEM — DESCRIBE ONE PROBLEM ONLY. PLEASE PRINT.

19. MATERIALS ATTACHED — PLEASE ATTACH DETAILED BACK-UP MATERIALS THAT WOULD EXPEDITE RESOLUTION OF THE PROBLEM DESCRIBED ABOVE.

☐ SYSTEM DUMP ☐ PROGRAM DUMP ☐ CONSOLE PRINTOUT ☐ OTHER (LIST) _____

ORIGINATOR — DO NOT WRITE BELOW THIS LINE

20. CAUSE | 21. DATE RECEIVED

22. ACTION

23. CATEGORY

☐ BUG FIX ☐ ENHANCEMENT ☐ SUGGESTION ☐ TECHNICAL QUESTION

PROCESSED BY | DATE

SC1-1843 REV 7-83

1

64214

Figure 1-1. DSUR Form

2. MACRODIAGNOSTIC PROGRAM LOAD

2.1. Introduction

This section summarizes the information required for a successful program load. It describes the console screen format, the sequence of the program load, and the load procedure, followed by error information and analysis of load failures. The section concludes with descriptions of the DCP/40/20 maintenance panels and DCP/10/10A/15 operator control panel.

NOTE

For the DCP/10A and the DCP/15, the current release of the macrodiagnostics has the following restriction:

The load device is limited to SCSI target controller 7, logical unit number (L.U.N.) 2 (integrated diskette drive).

2.1.1. F1 Menu

The F1 menu is described first because it is part of all of the tests. Pressing the F1 key (FUNCTION key/F1 key or FUNCTION key/1 key on some consoles) displays the menu, illustrated here and at the bottom of Figure 2-1.

```
>1 = Continue the test.
>2 = Abort current activity and reinitialize the EXEC
>3 = Hold current activity and use the UTILITIES
>[]
```

The menu selections are detailed as follows:

When 1 is entered, the console displays:

```
RESUMING INTERRUPTED PROCEDURE
```

When 2 is entered, the console displays the first screen of the diagnostic test menu:

```
>1.  SYSTEM TEST
>2.  LOCAL LANGUAGE TRANSLATE
>3.  SERIAL LINE MODULE TEST
>4.  LOCAL STORAGE (Memory) TEST
>5.  RIGID DISK DRIVE (T-8409) TEST
>6.  MDLM MASS STORAGE TEST
>Press TRANSMIT key to display other selections. or
>Select a Test number from the Menu
>[]
```

When 3 is entered, the console displays:

```
>RESIDENT UTILITIES - ENTER COMMAND
```

When the command is entered, the screen displays a default system segment number (SSN) and the segment descriptor (SEG) for the SSN.

```
>SSN=0001     SEG-FF00201F
```

Refer to Section 16 for the command entries.

2.2. Diagnostics Console Screen Format

The screen of the console displays the menus, prompts, error messages, and test information of the diagnostic tests and the utilities. Figure 2-1 illustrates the format of the screen.

The title sector is at the top of the screen and the initial display sector is at the bottom. In between these two sectors are the fixed area and the free area of the screen. In general, new information, prompts, and instructions scroll onto the screen from the bottom with the initial display sector rolling up into the free area and then off the screen, six lines at a time. When the TRANSMIT key is pressed, six more lines are displayed.

```
-------------------------------------------------------

(LINE 1)     CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1
(LINE 2)                      Test Title
(LINE 3)                    (FIXED AREA)
(LINE 4)
(LINE 5)

                          (FREE AREA)

                    (INITIAL DISPLAY SECTOR)


     >1 = Continue the test.
     >2 = Abort current activity and reinitialize the EXEC   (F1 MENU)
     >3 = Hold current activity and use the UTILITIES
     >[]

-------------------------------------------------------
```

Figure 2-1. Console Screen Format with F1 Menu Included

2.3. Load Procedure

Load the macrodiagnostic software as follows:

1. Insert appropriate diagnostic diskette into integrated diskette drive:

   Diskette #1, DR2610-01 for DCP/20/40/
   Diskette #1, DR2615-01 for DCP/10
   Diskette DR2611-01 for DCP/10A
   Diskette DR2626-01 for DCP/15

2. Disable the CP maintenance panel of the DCP/40 by setting the PANEL ENABLE switch in the down position. Disable the CLC maintenance panel of the DCP/20 by setting the PANEL ENABLE/ DISABLE switch in the down position.

3. Enter the number of the console port into the load switches on the operator control panel of the DCP.

   For the DCP/10/10A: The load switches are numbered 0 through 4. Switch 0 is not used and is set down. The other switches are set up (UP) or down (DN) as follows:

Console Type	Switch 1	Console Port	Switches 2	3	4
Local	UP	0	DN	DN	DN
Host	DN	1	DN	DN	UP
		2	DN	UP	DN
		3	DN	UP	UP
		4	UP	DN	DN
		5	UP	DN	UP
		6	UP	UP	DN
		7	UP	UP	UP

   For the DCP/15: The load switches are numbered 0 through 4. Switch 0 is not used and is set down. The other switches are set up (UP) or down (DN) as follows:

Console Port	Switches 1	2	3	4	Console Port	Switches 1	2	3	4
0	DN	DN	DN	DN	8	UP	DN	DN	DN
1	DN	DN	DN	UP	9	UP	DN	DN	UP
2	DN	DN	UP	DN	10	UP	DN	UP	DN
3	DN	DN	UP	UP	11	UP	DN	UP	UP
4	DN	UP	DN	DN	12	UP	UP	DN	DN
5	DN	UP	DN	UP	13	UP	UP	DN	UP
6	DN	UP	UP	DN	14	UP	UP	UP	DN
7*									

*Port 7 does not exist on the DCP/15.

Load Procedure (cont)

4. Press SYSTEM RESET button on the operator panel. The LED indicator on the integrated diskette drive illuminates as the program loads.

   For the DCP/10/10A/15: Observe the display of the operator panel. If an error occurs during the load, the display reports a two-digit alphanumeric error code. The error reflects the contents of Register 0 (R0).

   Observe the CP maintenance panel of the DCP/40 or the CLC maintenance panel of the DCP/20. If an error occurs during the diagnostic load, enable the panel to view an error code in the lower 16 bits of the General Display of the DCP/40 or in bits 0 through 15 of the Register Display of the DCP/20. The display reflects the contents of Register 0 (R0).

   When the program load completes successfully, the DCP console begins polling. Also, the operator control panel of the DCP/10/10A/15 cycles through a series of alphanumeric characters for approximately two minutes and then the numbers 43 are superimposed on the display.

5. To begin the diagnostic routines, enter:

   >//DIAG <transmit>

   The resulting display, which differs slightly depending on the DCP, offers the option of checking (building) the CLCs/Ports or bypassing the build routine.

```
   CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1

        NOW BUILDING THE CONFIGURATION TABLE

>Enter the Number of CLCs to be checked (0-16)
>(default: 4 CLCs.     0: Abort Build Routine
>[]
```

Load Procedure (cont)

6. If you select 0 (zero), go to step 8. To check the CLCs/Ports, proceed as follows:

   a. DCP/40 - DCP/20:

      >Enter the Number of CLCs to be checked (0-16)
      >(default: 4 CLCs. 0: Abort Build Routine
      >[]

      (1) Enter any number between 1 and 16. The screen displays the following:

      NOW BUILDING THE CONFIGURATION TABLE

      PROCESSING CLC #: XXXX

   b. DCP/10/10A:

      >Enter the number of Ports to be checked (0-16)
      >(Default is 7 Ports. 0 : Abort Build Routine
      >[]

      (1) Enter the number 7.

   c. DCP/15:

      >Enter the Number of Ports to be checked (0-16)
      (Default is 7 ports. 0 : Abort build routine
      >[]

      (1) Enter the number 14.

   Since the DCP/10/10A/15 do not have CLCs, the screen displays the following message:

   NOW PROCESSING SYSTEM CHANNELS

7. When the build routine completes, another set of options appears:

   >To inspect the Configuration Table, use the
   >Display Routine which is in Resident Utilities.
   >Press TRANSMIT to continue
   >[]

   To access the resident utilities, described in Section 16, use the F1 menu.

   To proceed directly to the diagnostic test menu, press the TRANSMIT key.

Load Procedure (cont)

8. If the build routine is bypassed by entering 0 (zero), the console displays the first screen of the diagnostic test menu:

```
   CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1
              MENU OF DIAGNOSTIC TESTS

>1.  SYSTEM TEST
>2.  LOCAL LANGUAGE TRANSLATE
>3.  SERIAL LINE MODULE TEST
>4.  LOCAL STORAGE (Memory) TEST
>5.  RIGID DISK DRIVE (T-8409) TEST
>6.  MDLM MASS STORAGE TEST
>Press TRANSMIT key to display other selections, or
>Select a Test number from the Menu
>[]
```

Pressing the TRANSMIT key displays the second screen:

```
>7.  PARALLEL LINE MODULE TEST
>8.  HOST CHANNEL INTERFACE (SU00039/SU00208) TEST
>9.  CARTRIDGE DISK DRIVE (T-8408) TEST
>10. TAPE DRIVE (C10) TEST
>11. COPY UTILITY--INTEGRATED FLEXIBLE DISKETTE
>12. COPY UTILITY--FDS T8406-00 THRU -03
```

Pressing the TRANSMIT key again displays the third screen:

```
>13. TWISTED PAIR TERMINAL TEST
```

9. Enter a test number and refer to the section in this book where the test is described.

   When a test is selected, one or more of the following messages rolls into the scroll space:

```
LOADING SELECTED TEST

TEST PROCEDURE INITIALIZING

LOADING Test Port Processor Code

LOADING Test Message File
```

2.4. Error Isolation for Load Failures

If an error occurs during the initial program load, errors codes are displayed on the maintenance panels of the DCP/20/40 and on the operator panel display of the DCP/10/10A/15.

NOTE

If the diagnostic will not load or the loader CLC times out during the load, ensure that the R PCA (DCP/40/20) is strapped for the loader port.

In general, whenever an error occurs, first attempt a reload by pressing the SYSTEM RESET switch on the operator panel. Frequently, the system loads successfully without the error recurring.

2.4.1. Bootloader Error Stop Routine

Entry into the bootloader error stop routine indicates that the bootloader program found an illogical condition or that a forced call or a queued event (PN0 through PN8) occurred. If an event occurs prior to enabling the forced calls, the microcode attempts to reboot the DCP.

To determine the cause of a bootload failure in the DCP/40/20, run the microdiagnostics. To isolate an error in the DCP/10/10A/15 or the Integrated Communications Processor (ICP), carefully monitor the error display to record the last display. Interpretation of the display data should make it possible to isolate the failed component.

Register 0 (R0) contains the current error stop information and can be inspected at any time to determine the current progress of the bootload. Error stop information in R0 is updated as the program loads.

2.4.1.1. Bootloader Error Display

Error displays in the bootloader serve several purposes:

1. When no stops or error conditions are encountered, a changing display provides visual assurance that the DCP is functioning and that the load is progressing.

2. If a hardware error occurs, the error display provides information which helps in isolating the cause of the error.

3. Many error stops are not caused by a failing DCP. Some stops occur because of power-line noise or fluctuations, faulty load media, faulty diskette drives. In these cases it is necessary to have as much information as possible about the machine environment at the time of the stop to determine if the stop can be duplicated.

4. The ROM and the microcode perform some testing and provide information to the macrocode at system initialization, such as the occurrence of microcode load errors and indications of missing or faulty local storage arrays. This information is incorporated into the error displays whenever possible.

2.4.1.2. The DCP/10/10A/15 and the ICP Error Display

The display register reports error information one byte at a time. Every two bytes of data are preceded by a unique error index code. In the ICP, the Peripheral Testing Sequencer (PTS) program retrieves the data and displays it on the host console or dumps it to the printer. Observe the data directly using a display module (P/N 2819991-00) installed on J3 of the FEPI line module. Each byte is displayed for approximately two seconds.

2.4.1.3. The DCP/40 and the DCP/20 Error Display

The content of R0 is displayed in the LEDS to the right of the load path switches and in bits 16 through 31 on the general display of the maintenance panel. To observe R0, the PANEL ENABLE switch must be down when the DCP stops. When the PANEL ENABLE switch is up, set the DISPLAY SELECT switches for register display.

If the program enters the error stop routine, all registers are stored and the DCP stops. When the START button is pressed, all of the errors are displayed in sequence and the DCP stops again. R0 through R15 contain the displayed errors. The content of the registers is:

R0 always contains the upper and lower bytes of the EO error code.

R1 - R6 contain 0000 or supplementary error data associated with a specific error code.

R7 contains 0000 or 00B0 through 00B8, indicating a forced call or queued event (PN0 - PN8)

R8 - R11 contain 0000 or information pertinent to a forced call or queued event.

R12 - R15 contain 0000.

When START is pressed again, the next stop has R0 through R15 filled with the same data that they contained when the error stop routine was entered. R15 contains the address of the next instruction.

Press the START button continuously to toggle between the two error stops.

2.4.1.4. Bootloader Error Display Structure

The error codes can be divided into three groups. The groups are defined by the display index code preceding each byte of error display data:

- Group 1, E0 through EB, provides primary and supplemental error information.

  R0 always contains E0: E0 (upper byte) - upper hex digit = W
  - lower hex digit = X
  E0 (lower byte) - upper hex digit = Y
  - lower hex digit = Z

  E0, Upper Byte = all zeroes (00) if the bootloader was executing the main path. Non-zero value indicates that the bootloader was executing a subroutine.

  E0, Lower Byte = panel display of DCP/10/10A/15 and top cap LEDs of DCP/40/20 always contain the lower byte of E0. It shows the general progress of the load.

  E1 - E6 = same data as R1 through R6 (0000 or supplementary data)

  E7 = same data as R7 (0000 or 00B0 - 00B8)

  E8 - EB = same data as R8 through R11 (0000 or data related to forced call/queued event)
  EC - EF = same data as R12 through R15 (0000)

- Group 2 (DCP/10/10A/15 only), C0 through CF, provides the content of the general registers at the time the error routine was entered. The display toggles every two seconds through the codes as follows:

  C0 (1st display) = Upper byte of R0
  C0 (2nd display) = Lower byte of R0
  C1 (1st display) = Upper byte of R1
  C1 (2nd display) = Lower byte of R1
  C2 - CF etc.

- Group 3, B0 through B8, contains the forced call or queued event (PN0 - PN8).

The following figures aid in interpreting the error display:

Figure 2-2. Bootloader Error Code Structure

Figure 2-3. YZ Values of E0, Lower Byte

Figure 2-4. WX Values of E0, Upper Byte

Figure 2-5. YZ Values of E7, Lower Byte (B0 through B8)

DISPLAY CODES

E0 - EB = PRIMARY ERROR INFORMATION
E0 (upper) = WX where: W identifies specific subroutine
X identifies minor step in subroutine

E0 (lower) = YZ where: Y designates major step
Z designates minor step

E1 - E6 = 0000 or supplementary error data

E7 = 0000 or 00B0 - 00B8, indicating a forced call or queued event, PN0 - PN8

E8 - EB = 0000 or information related to forced call or queued event

C0 - CF = GENERAL REGISTER DISPLAY OF DCP/10/10A/15

B0 - B8 = E7, LOWER BYTE, FORCED CALL/QUEUED EVENT (PN0 - PN8)

Figure 2-2. Bootloader Error Code Structure

Figure 2-3 illustrates the YZ values of the display index code E0, lower byte, and any supplemental error data that is found in E1 through E6.

DISPLAY INDEX E0, LOWER BYTE = YZ
(SUPPLEMENTAL DATA FOR Y=3, Y=4, Y=5/Y=A)

Y = 2 = INSTRUCTION TEST (No Supplemental Data)
- Z = 0 = Test 'store' instruction (S)
- = 1 = Test jump instruction (J)
- = 2 = Jump register not zero (JNZ)
- = 3 = Load constant, jump equal, compare constant (LK, JE, CK)
- = 4 = Add nibble, jump register (AN, JR)
- = 5 = Verify store operation, compare register, load (S, CR, L)
- = 6 = Store zeros, jump reg. zero (SZ, JZ)
- = 7 = Store indexed (S)
- = 8 = Store system control register (SSCR)
- = 9 = Local jump forward and back (LJ)

Y = 3 = TESTING LOCAL STORAGE IN EXEC LOAD AREA
- Z = 0 = Set up transparent read address
- = 1 = Transparent read
- = 2 = Transparent write, zeros
- = 3 = Transparent read, zeros
- = 4 = Transparent write, ones
- = 5 = Transparent read, ones
- = 6 = Normal write, zeros
- = 7 = Normal read, zeros
- = 8 = No error occurred, but program reported one
- = 9 = Error code in R0 was not in range 30-3F: jump instruction failed or local storage problem in boot area.
- = A = Error routine improperly entered: jump instruction failed in memory test area or local storage problem in boot area.
- = B = Multiple bit error during write/read of all zeros
- = C = ECC logic failed during write/read of all zeros
- = D = ECC failed during write/read of all ones
- = E = Write of all zeros failed after ECC test
- = F = Either multiple bit error during write/read of all ones or program falsely detected error during write/read of all ones

Figure 2-3. YZ Values of E0, Lower Byte (Sheet 1 of 3)

SUPPLEMENTAL DATA FOR Y=3

E1, E2 = Diagnostic write/read instruction
E3, E4 = Diagnostic read data which was incorrect (should be all 1's or all 0's)
E5 = First 16 bits of the local storage bit map built by microcode (1 bit = 65K bytes of storage present)

Y = 4 = BUILDING ARCHITECTURE
- Z = 0 = Build bootloader virtual address (V.A.) space, no errors expected
- = 1 = Set up beginning of table area, no errors expected
- = 2 = Build SD and SST entries for SST, SCT, PCS, procedure table, CMAST, throttle table, no errors expected
- = 3 = Build ICT and set its length: unidentified processor type (not 10/10A, 15, 20, or 40), SCR failed
- = 4 = Build system queue area, no errors expected
- = 5 = Build first buffer pool, no errors expected
- = 6 = Create system information, no errors expected
- = 7 = Set up procedure table entries for PN0-PN8, no errors expected
- = 8 = Load data in SCT, no errors expected
- = 9 = Load process control registers and enable PN0-PN8, no errors expected
- = A = Enable SCT and RTC, no errors expected
- = B = RTC failed to increment, no supplemental data
- = C = Response bit (R bit) did not set when C bit was set in ICT for loader PP
- = D = Active bit did not set in ICT for loader PP after R bit was set
- = E = Loader PP could not read hardware ID (HWID) of line module in loader port
- = F = Unidentified line module in loader port

SUPPLEMENTAL DATA FOR Y=4

If Z = 0-A then E1, E2 = Current real address (R.A.)
E3 = Current V.A.
E4 = Processor type from SCR

= B-F then E6 (E1 upper) = Loader port
E7 (E1 lower) = Expected HWID
E9 (E2 lower) = HWID read
E3 = C bits for the loader CLC
E4 = R bits for the loader CLC
E5 = A bits for the loader CLC

Figure 2-3. YZ Values of E0, Lower Byte (Sheet 2 of 3)

Y = 5Z = LOAD EXEC BASE SEGMENT
6Z = LOAD EXEC CALL SEGMENT 1
7Z = LOAD EXEC CALL SEGMENT 2
8Z = LOAD EXEC LOAD TABLE
9Z = LOAD EXEC CONSOLE PP
AZ = LOAD EXEC LOADER PP
AA = LOAD COMPLETE, displayed for five seconds on DCP/10/10A/15

Z = 0 = Set up SDs for this load element
1 = IFDC - Reading subdirectory from diskette
FEPI - Sending load request to host
2 = IFDC - Translating subdirectory data
FEPI - Waiting for host to send load record
3 = Read load record
4 = Unpack load record
5 = Build SST entries for load segment
6 = FEPI - Data other than load record received from host
A = Same as 0
B = Same as 1
C = Same as 2
D = Same as 3
E = Same as 4
F = Same as 5

SUPPLEMENTAL DATA FOR Y=5/Y=A

E1 = Record NR expected/Record NR received
E2 = Load file ID expected/Load file ID received
Exec base = X60
Call element 1 = X61
Call element 2 = X62
Load table = X63
Console PP = X64
Loader PP = X65
E3 = Line module status from I/O operation
E4 = Track/sector in hex for IFDC loader; X0000 for FEPI loader

Figure 2-3. YZ Values of E0, Lower Byte (Sheet 3 of 3)

Figure 2-4 defines the WX value of the display index code E0, upper byte.

DISPLAY INDEX E0, UPPER BYTE = WX

WX = 2X = BUILD SEGMENT DESCRIPTOR, UPDATE SST AND CURRENT V.A.
4X = IFDC HANDLER
5X = MDLM HANDLER
6X = FEPI READ ROUTINE
7X = FEPI WRITE ROUTINE
8X = SUBDIRECTORY TRANSLATION FOR IFDC, MDLM
9X = UNPACK LOAD RECORDS
AX = BUILD SEGMENT DESCRIPTORS FOR ELEMENT TO BE LOADED
BX = CREATE SST ENTRIES FOR ELEMENT JUST LOADED

X = 1 = Make real address from next available virtual space and add R.A. of ICB to it
= 2 = Create length bits for new SD
= 3 = Make SST entry with new SD
= 4 = Increment next V.A. to next 128-byte boundary

NOTE

Error stops are not present in the W=2 subroutines. If an error occurs, the probable cause is a hardware failure and the error display was entered through a forced call or queued event (PN0 - PN8). See Figure 2-5.

Figure 2-4. WX Values of E0, Upper Byte

Figure 2-5 defines the YZ values of the display index code E7, B0 through B8.

DISPLAY INDEX CODE E7, LOWER BYTE
FORCED CALL/QUEUED EVENTS PN0 - PN8

```
Y = B = FORCED CALL/QUEUED EVENT
    Z = 0 = CP Hardware Error
            F1, F2, F3, F4 = SCR 14 (Appendix B)
            F5, F6, F7, F8 = SCR 15 (Appendix B)
        1 = CP specification error
            F1, F2, F3, F4 = SCR 13 (Appendix B)
            F5, F6, F7, F8 = Address following instruction
                             which caused error
        2 = Not enabled (should not occur)
        3 = Monitor clock interrupt:  not enabled (should not
            occur)
        4 = CP recoverable software error
            F1, F2, F3, F4 = SCR 11 (Appendix B)
            F5, F6, F7, F8 = CP specification error, same as
                             Z = 1
        5 = Instrumentation call:  not enabled (should not
            occur)
        6 = CP repressible hardware condition
        7 = PP hardware specification error
        8 = PP software specification error
```

Figure 2-5. YZ Values of E7, Lower Byte (B0 through B8)

2.4.2. Executive Error Codes

The maintenance panel (DCP/40/20) or the operator panel (DCP/10/10A/15) displays the error codes under the following conditions:

- The error occurs before console initialization
- The error occurs during console reinitialization
- The error occurs during console operation when reinitialization is impossible. If the console is functioning, then the screen displays the error code or the error is held until reinitialization is complete and then it is displayed.

There are two types of error codes: those that are displayed at the error stop (address) and those that are displayed when the program stops in mid-instruction (hangs). To distinguish between them, the following documentation identifies them at ES, displayed at the error stop, and PH, displayed if the program hangs.

NOTE

The error stops occur only when the executive cannot report the error to the console.

When the error stop occurs in the DCP/40/20, R0 through R7 store the following data:

R0 contains a four-digit hexadecimal code: lower two digits represent procedure number (PN) executing when the error occurred; upper two digits represent specific error number which relates to the PN that was executing

R1 thru R7 contain variable data (if any) related to specific error

When the error stop occurs in the DCP/10/10A/15, the alphanumeric display cycles continuously through the following sequence at two-second intervals:

1. E0
2. Two-digit number representing specific error (same as upper half of R0)
3. E0
4. Two-digit number representing procedure number (same as lower half of R0)
5. E1 through E7 - variable data, if any (the code alternating with data as above)
6. EF
7. Two-digit number representing the upper byte of data in R15
8. EF
9. Two-digit number representing the lower byte of data in R15

R15 contains the address where the error was detected. If there is no variable data, only E0 and EF are displayed.

If the program hangs, the only data available for the DCP/40/20 is stored in R0. The upper half contains the error code that describes what the executive was doing when the program stopped. The lower half contains the procedure which the executive was executing. The only data available in the DCP/10/10A/15 is the constant alphanumeric display of the procedure number.

NOTE

The two-digit number of the error code that represents the procedure number is PN + 30.

The following list defines the procedure numbers.

Procedure Number (PN)	Processor Instruction
0000	CP Hardware Forced Call
0001	CP Specification Exception
0003	Dispatcher (Monitor Clock Interrupt)
0004	CP Process Control Error
0006	CP Repressible Hardware Condition
0007	PP Hardware Condition
0008	PP Software Specification Exception
0009	Instrumentation Buffer
000A	IFDC Loader Call Routine
000B	Console Driver

Procedure Number (PN)	Processor Instruction
000C	Buffer Pool Threshold Handler
000D	Buffer Discard Process
000E	Console Interrupt
000F	Console Line Protocol Handler (L.P.H.)
0010	Translate ASCII/Binary
0011	Turn Off a PP
0012	Initialize a PP
0013	Load a Segment Descriptor (S.D.)
0014	Read/Write the Error Log
0015	Build S.D. Entry for SDT
0016	FEPI L.P.H.
0017	IFDC L.P.H.
0018	Build a Queue List
0019	Build/Add a Queue
001A	Get Visibility to a Queue
001B	Build a Subsegment Table
001C	Request a Timed Wait
001D	Load Hardware Register with 8-bit Code
001E	Add/Delete Static Storage
001F	Build and Display a Menu
0020	Build a Procedure Entry
0021	Parser Procedure
0022	Initialize Procedure by Queueing to Dispatch
0023	Get the Caller's ID
0024	Change Processes
0025	Save SDR's
0026	Build a Message Control Table (MCT)
0027	Return Message Entry to Console
0028	Console Overflow
0029	MDLM L.P.H.
002A	Storage Procedure for Executive
002B	Test Message and PP File Load Routine
002C	Console Initialization
002D	Message Wait Procedure
002E	Function Key 2 Procedure
002F	Function Key 3 Procedure
0030	Function Key 4 Procedure
0031	Resident Utilities
0032	Configuration Table Builder
0033	Display PP state item
0034	True Console Entry Point
0035	Get Visibility to Message

The error codes are divided into four categories: permanent executive error stops, console procedure errors, executive loader errors, and IFDC/MDLM handler errors. Locate the error code in the following list and then refer to Tables 2-1 through 2-4 for a description of the error.

Permanent Exec. Error Stops (Table 2-1)

X0155	X225A
X0156	X235A
X015A	X245A
X015C	X255A
X0161	X265A
X0255	X275A
X0256	X285A
X025A	X295A
X0261	X2A5A
X0356	X2B5A
X035A	X2C5A
X0456	X305A
X045A	X315A
X0556	X325A
X055A	X335A
X0656	X345A
X065A	X355A
X075A	X365A
X085A	X375A
X095A	X385A
X0A5A	X395A
X0B5A	X3A5A
X0C5A	X3B5A
X0D5A	X3C5A
X0E5A	X405A
X0F5A	X415A
X105A	X425A
X115A	X435A
X125A	X445A
X135A	X455A
X145A	X465A
X155A	X475A
X165A	X485A
X175A	X495A
X185A	X4A5A
X195A	X505A
X1A5A	X515A
X1B5A	X525A
X1C5A	X535A
X1D5A	X545A
X205A	X555A
X215A	X565A

Console Procedure Errors (Table 2-2)

X013B	X065C
X013F	X0665
X0157	X073B
X0157	X073F
X015C	X075C
X0164	X0764
X0165	X0765
X023B	X083F
X023F	X085C
X0255	X0864
X0257	X0865
X025C	X093F
X0264	X095C
X0265	X0964
X033B	X0965
X033F	X0A3F
X0355	X0A5C
X0357	X0A65
X035C	X0B3F
X0364	X0B5C
X0365	X0B65
X043B	X0C3F
X043F	X0C5C
X0455	X0C65
X045C	X0D3F
X0464	X0D5C
X0465	X0D65
X053B	X0E5C
X053F	X0E65
X0555	X0F5C
X055C	X0F65
X0564	X105C
X0565	X115C
X063B	X01065
X063F	

Executive Loader Errors (Table 2-3)

X013A
X023A
X043A
X053A
X073A
X093A

IFDC/MDLM Errors (Table 2-4)

X0447 (IFDC)
X0459 (MDLM)
X0C47 (IFDC)
X0C59 (MDLM)

NOTES

PH = Program stopped in mid-instruction
ES = Error stop (address)

R1 refers to the DCP/40/20; word 1 refers to the DCP/10/10A/15.

Table 2-1. Permanent Executive Error Stops

Description	Error Type
X015A The executive had started building the architecture. The program is setting up the initiation status in the System Information Table (SIT) and is rearranging the console address in local storage.	PH
X025A The program was in the process of rearranging the contents of the SDRs, invalidating the SCT (built by the bootloader), and setting up the ICB.	PH
X035A The executive has begun extending the 128-byte buffer pool and cannot recognize the processor type code which was placed in the ICB by the microcode bootloader. The code is in R1 or word 1. Currently recognizable codes are: DCP/40 - X40 DCP/20 - X20 DCP/10 - X10	ES
X045A The program is building the 128-byte buffer pool. The following instructions are used for the first time: MR = multiply registers ANDK = AND register with a constant ADR = add two sets of double registers SUK = subtract a constant from a register	PH

Table 2-1. Permanent Executive Error Stops (cont)

Description	Error Type
X055A The program is building the 4K buffer pool. The following instructions are used for the first time: ORK = OR the register with a constant SUDR = Subtract one set of registers from another	PH
X065A The program was building the Procedure Segment Table (PST), which has 256 entries and is identical to the System Segment Table (SST) that was built by the bootloader. Its lenght is X10000 bytes. There are no new instructions in this section of the code.	PH
X075A The program was building the executive Gated Procedure List (GPL). There are no new instructions in this section of the code.	PH
X085A The program was building the Test GPL. There are no new instructions in this section of the code.	PH
X095A An error occurred while obtaining visiblity for the queue area of local storage. The first System Segment Number (SSN) was set to 0 which is an invalid SSN. SSNs start with 1. The SSNs for the queue area are built by the bootloader and placed in the SIT. Either the SIT has been tampered with or the SD values in SDR5 are incorrect.	ES
X0A5A The program was building the queues. There are no new instructions in this section of the code.	PH
X0B5A The program was building the procedure tables (PT) for the executive and the procedures. A SSN of 0, which is invalid, was passed to the subroutine performing the build, indicating interference with the SIT. The bootloader built the SNs at the time of loading the file from the disk.	ES

Table 2-1. Permanent Executive Error Stops (cont)

Description	Error Type
X0C5A The program was searching the SIT for more SSNs to place in the procedure table entry. A maximum of four SSNs are allowed. There are no new instructions in this section of the code.	PH
X0D5A The program was building the Process Control Stacks (PCS). In doing so, it secured more local storage and assigned it to the stack area. The secured area may have initiated the program halt (if possible, check the indicators), or the SDR logic may not be working correctly.	ES
X0E5A The program loaded the Process Control Registers (PCR) and the System Control Registers (SCR) and then validated the SCT. The process involves using the LPCR and LSCR instructions. A fault at this point indicates problems in the PCR/SCR logic or a microcode timing error during validation of the SCR.	ES
X0F5A The program was setting up various registers in the SIT in preparation for system procedure initialization (ADSTORE). Possible causes of the halt are: 1. The Call routines were not executed properly by the microcode. 2. The Call table was not set up correctly because data contamination occurred during the load or during program execution.	ES
X105A An error occurred during exeuction of the Call instruction to the various procedures requiring initialization. See X0F5A.	PH

Table 2-1. Permanent Executive Error Stops (cont)

Description	Error Type
X115A An error occurred during execution of the PARSER routine which the executive called to load the Common Message file from the load media. This is the first time that PARSER has been called. The error code is in R1 and in word 1 of the error data.	ES
X125A An error status was returned after the LOADER routine attempted to load the file containing the console procedures code. R1/word 1 = Returned status	ES
X135A An error status was returned when the LDSDREG (load the SDRs) routine attempted to convert a General Segment Number (GSN) into a SSN. R1/word 1 = Returned status	ES
X145A An error occurred when the program was building a PT entry for each of the procedures in the console program file. BLDPROC (build procedure routine) returned error status. R1/word 1 = Returned status	ES
X155A An error occurred during the initialization of the Scheduler routines. The program required buffer space for the process independent queue banks and called a routine to build a subsegment buffer. R1/word 1 = Returned status	ES

Table 2-1. Permanent Executive Error Stops (cont)

Description	Error Type
X165A	ES
An error occurred during the initialization of the Scheduler routines. The program required buffer space for the process independent queue banks and called a routine to build a subsegment buffer.	
R1/word 1 = Returned status	
X175A	PH
The program was completing the initialization of the buffer space for the queue banks, which includes setting all banks to zero. An error occurred in the memory addressing logic, or in the SDR contents, or in the interpretation of the SDR flags.	
X185A	ES
An error occurred while the program was building a subsegmented table for timer storage. The procedure building the table returned an error status.	
R1/word 1 = Returned status	
X195A	PH
An error occurred while the program was initializing the timer buffer. The error was caused by the addressing logic, local storage control, or interpretation of the SDR flags.	
X1A5A	ES
An error occurred while the program was building the storage subsegment table for E.P.A.	
R1/word 1 = Returned status	
X1B5A	PH
An error occurred during execution of the timer call functions. The program sets up the information required for E.P.A. and for the queue-to-time bank program. To accomplish this, it calls a procedure to find the procedure ID of the procedure that called the Timer routine.	

Table 2-1. Permanent Executive Error Stops (cont)

Description	Error Type
X1C5A The program was removing an entry from the dispatch lists. There are no new instructions in this section of the code.	PH
X1D5A The program was removing an entry from the dispatch lists (miscellaneous and tests). There are no new instructions in this section of the code.	PH
X205A The program was executing a system check followed by the establishment of visibility to the scheduler buffers. There are no new instructions in this section of the code.	PH
X215A A search of System Queue list #1 indicated an entry on the queue. The entry was not found when the program tried to load it into the general register set. One of the following errors occurred: 1. The hardware removed the entry or made it imperceptible. 2. The get queue instruction is executing incorrectly. 3. The equal/negative flags are set incorrectly.	ES
X225A The result of a search of the timer banks indicated that an entry was found, but the corresponding flag was not found. One of the following faults has occurred: 1. The flag bit in flag storage would not set, or bit 15 in the flag storage area is stuck at 1. 2. The test of the equality bits in the PSW is not working. 3. The equality bits in the PSW will not set correctly.	ES

Table 2-1. Permanent Executive Error Stops (cont)

Description	Error Type
X235A Type 4 buffer is full. One of the following errors occurred: 1. The program has formed an endless loop. 2. Dispatcher is not dispatching the type 4 waits. 3. Flags are stuck. Probable cause is a hardware error.	ES
X245A The number of items in the wait type 4 buffer was added to the number of free items in the buffer. The total did not compare with the total number of items allowed in the buffer. One of the following errors occurred: 1. The add registers instruction did not give correct result. 2. The compare instruction was unable to set the correct status flags. 3. The code has been altered by a hardware fault.	ES
X255A The program was transferring an entry to the priority banks. After completion of entry, use count was incremented and free count was decremented. Sum of modified counts did not equal maximum number of entries. The count, which is part of the priority bank registers, was modified during program execution. Possible cause is faulty addressing logic in the CLC or CP. R1/word 1 = sum of use count and free count R2/word 2 = maximum number of entries	ES
X265A The program transferred a queue bank entry to the dispatch queue. The total number of free entries were added to the total number of entries in use. They did not equal the total number of possible entries. R1/word 1 = total number of entries R2 = total number of possible entries	ES

Table 2-1. Permanent Executive Error Stops (cont)

Description	Error Type
X275A The program was cleaning up in preparation for returning to start to check the rest of the queues.	PH
X285A The program was transferring an entry from a storage bank to a forced item bank for dispatch.	PH
X295A The program was establishing visibility to the storage banks for the timer and the queue lists. It had called a procedure to load the GSN into the SDRs. R1/word 1= returned status	ES
X2A5A See X295A	ES
X2B5A See X295A.	ES
X2C5A The subroutine to load the SDRs called the program to perform the load and the program returned an error status. R1/word 1 = returned status	ES
X305A The program is looking for a procedure to dispatch.	PH
X315A The dispatch flags indicated that the process-independent banks contained an item for dispatch but the program could not find it.	ES
X325A The program has found an item and is checking for more entries. If there are none, it will clear the entry flag.	PH

Table 2-1. Permanent Executive Error Stops (cont)

Description	Error Type
X335A	ES
The dispatch flags indicated that there was a type 4 item for dispatch but the type 4 wait buffer contains no items.	
X345A	ES
After finding an entry in the timer type 4 buffer and moving it to the dispatch buffer, the program decremented the total number used and incremented the free total. The totals were added together but did not compare with total number of possible entries in the buffer. R1/word 1 = the sum of the total number in use and the total number free R2/word 2 = the total number of possible entries	
X355A	PH
The program was moving a monitor clock entry to the dispatch buffer.	
X365A	ES
The dispatch flags indicate the existence of a time-out for dispatch, but the bank totals show no entries in that bank.	
X375A	ES
After moving the entry to the dispatch queue, the program decrements the number of entries in use and increments the number of free entries. Their sum does not equal the number of possible entries in timeout banks. R1/word 1 = the sum of the total number in use and the total number free R2/word 2 = the total number of possible entries	
X385A	ES
The program was transferring an executive miscellaneous queue entry to the dispatch queue.	

Table 2-1. Permanent Executive Error Stops (cont)

Description	Error Type
X395A The program was transferring a test queue to the dispatch queue.	ES
X3A5A The program transferred a queue bank item to the dispatch queue. The sum of items in use and the free items did not equal the number of items possible in the bank.	ES
X3B5A The program was transferring an item from the dispatch queue while restoring the environment.	PH
X3C5A The program was dispatching a procedure. The procedures may be returned to or called. Probable cause of error is an irregularity in the procedure stacks. Most of these errors are reported as PN1 errors. If interference with the stacks has occurred during a return, then the return may be to a nonexistent procedure or address.	ES
X405A The program was dispatching searches for timeouts in timeout banks.	ES
X415A The program was dispatching searches for timer entries corresponding to the current queue SAI from system queue list 1.	PH
X425A The program was comparing entries in one of the timer banks. An entry was found and moved to a temporary buffer. The sum of the decremented use count and the incremented free count does not compare with the number of possible entries in the buffer.	ES

Table 2-1. Permanent Executive Error Stops (cont)

Description	Error Type
X435A A process halt occurred during the search and entry transference from a type 1 timer buffer to a temporary buffer.	PH
X445A A processor halt occurred during the search of the type 1 timer buffers for timeouts and the transference of an entry to the temporary queue buffer.	PH
X455A The timer buffer has no more free entries. An infinite loop has occurred in the software. Probable cause is a hardware fault which has either pushed the software into the loop by its detection or caused the program to write over a portion of itself.	ES
X465A In establishing visibility to the timer buffer, the program called a routine to load the SDRs with the content of a general segment number (GSN). The routine (LDSDREG) returned error status. R1/word 1 = returned status	ES
X475A The timer buffer control register indicated the existence of an empty buffer but the program could not find it.	ES
X485A The program placed an entry in the timer banks, incremented the use count, and decremented the free count. Their sum does not equal the number of possible entries in the bank.	ES

Table 2-1. Permanent Executive Error Stops (cont)

Description	Error Type
X495A The program called a procedure to release its visibility to the timer banks. The procedure returned an error status. R1/word 1 = returned status	ES
X4A5A The program was executing the system check.	PH
X505A The program was setting up the parameters for visibility to the E.P.A. banks.	PH
X515A The program was saving the SDRs, the general registers, and the stack indicators.	PH
X525A The program was saving the Cmast, the Pmast, and the Call/Return stack entries.	PH
X535A The program was searching for free space using a bitmap of the E.P.A. buffer.	PH
X545A The current E.P.A. buffers are full so the program requested a new subsegment table to increase the table size. The process building the subsegment table returned an error status.	ES
X555A The procedure that was establishing visibility to the E.P.A. storage banks returned an error status when it tried to load a SDR with a designated SSN.	ES
X565A The program was restoring a procedure's environment prior to dispatching it.	PH

Table 2-1. Permanent Executive Error Stops (cont)

Description	Error Type
X0155	PH
The program attempted to save a set of SDRs. One of the following events may have caused the error: 1. A reference to an area of storage outside of the current program failed because the SDR is corrupted. 2. The instruction to store the SDR executed incorrectly.	
X0156	ES
The buffer pool contains no more 128-byte buffers. The program called the buffer pool manager to enlarge the buffer pool but the manager returned an error status. Probable cause of error is a hardware fault in the CPU or the CLC logic (or the logic which simulates their operation).	
X0161	ES
Received bad status from LDSDREG routine when attempting to load SDR 16 with the loader PP SSN.	
X015C	PH
Another routine called the timer routine and it attempted to transfer control to the permanent executive code. Probable cause of error is one of the following 1. The content of the SDRs 8 - 10 (Control Mode) were corrupted or totally cleared out. 2. Another program has tampered with the target address. 3. Another program has tampered with the code that resides at target address.	

Table 2-1. Permanent Executive Error Stops (cont)

Description	Error Type
X0255 The program attempted to restore a set of addresses to the SDRs. Probable cause of error is one of the following: 1. See item 1, error code X0155. 2. The instruction to load the SDR executed incorrectly.	PH
X0256 The program attempted to get a 4K buffer from the buffer pool. See X0156.	ES
X0261 Received bad status from MESSVIS procedure when getting visibility to the using SDR 29.	ES
X0356 See X0156 and X0256. This is the second buffer to be pulled from the buffer pool.	ES
X0456 See X0156 and X0256. This is the third buffer to be pulled from the buffer pool.	ES
X0556 See X0156 and X0256. This is the fourth buffer to be pulled from the buffer pool.	ES
X0656 The program attempted to load the last buffer into the SDRs and then to return to the calling program. Probable cause of error is the execution of the LSDR instruction or the execution of the return instruction.	PH

NOTES

PH = Program stopped in mid-instruction
ES = Error stop (address)

R1 refers to the DCP/40/20; word 1 refers to the DCP/10/10A/15.

Table 2-2. Console Procedure Errors

Description	Error Type
X013B The console is no longer executing and the executive is trying to reinitiate it.	ES
X023B The console transferred the parameters from the parameter buffer in the SIT to its own storage areas. It built an MCT for the message. Probable cause of halt is an error in the addressing logic or in the SDR logic.	PH
X033B A fatal error occurred while the program was calculating the message address. Probable cause of halt is an error in the SDR logic, or the addressing logic, or memory management.	PH
X043B The program was transferring a message from a message file to the MCT data area. Probable cause of halt is an error in one of the following: the SDR logic, the addressing logic, local storage control, or the byte load/store operations.	PH
X053B A message required the translation of data before it was appended. The translate routine returned an error status. R1/word 1 = returned status	ES

Table 2-2. Console Procedure Errors (cont)

Description	Error Type
X063B The data was appended to the message. The program generated a set of instructions for the LPH that were placed in the MCT. The MCT was queued to the LPH. See X033B and X053B for possible hardware problems.	PH
X073B The procedure entered a 'forced mode' and placed the message in the link area. Possible cause of problem is an error in one of the following: the link area logic and microcode, the storage and storage control logic, or the call logic.	PH
X015C The program was checking the content of the SIT to identify the processor type. This had been checked when in the ICB. Problems are associated with either the loader PP or fault which caused incorrect parity in the SIT storage locations.	PH
X025C The program was calculating the console queue addresses and changing their notification addresses to point to the initiation routine. See X015C for problems associated with this error.	PH
X035C Received bad status from BSDEBT routine when building an SSW for a temporary PP. R1/word 1 = returned status	ES
X045C ES The procedure that was called to initiate the console's port processor returned an error status. R1/word 1 = returned status	
X055C The PP was initiated and executing but did not set the bit in its status word that indicates a fetch of the line module ID was completed.	ES

Table 2-2. Console Procedure Errors (cont)

Description	Error Type
X065C The line module ID (LMID) is unknown to the program and cannot be used. Possible causes of problem are: 1. The line module is not working and cannot return its LMID. 2. The line module tried to return its LMID but the LMID was lost on the L-bus. 3. The LMID was placed in a storage location that could not be written. 4. The PP addressing is not functioning properly and the ID was written to the wrong location.	ES
X075C The parallel channel PP would not complete its initiation but did not find an error and send a PP state item.	ES
X085C During its initiation, the parallel channel PP returned a PP state item. See R1 through R5 for status. Possible causes of problem are: 1. Line module is not functioning correctly. 2. The console is not powered-on, not connected, or functionally unable to answer the host.	ES
X095C The serial PP did not complete its jump to the serial line module code, did not set the ready status in its status word, and did not send a PP state item.	ES
X0A5C The console serial PP posted a PP state item. See R1 through R5 for status.	ES

Table 2-2. Console Procedure Errors (cont)

Description	Error Type
X0B5C The program was establishing visibility to the microcode storage area of the PP. The process which was called to load SDR20 with the address returned an error status. R1/word 1 = returned status	ES
X0C5C Same as X0B5C. The program was establishing visibility to the microcode buffer.	ES
X0D5C The console PP attempted to load a section of the line module microcode into the line module and did not set the completion bit.	ES
X0E5C At the completion of the last line module microcode segment, the PP was told to fetch the line module status. It did not notify the CP code by setting a status bit in its status register.	ES
X0F5C The line module returned incorrect status after completing the microcode load. R1/word 1 = returned status	ES
X105C The program instructed the line module to complete the initialization of the serial line module by loading its registers with the correct values. The completion status bit was not set.	ES
X115C Initialization is complete. The initialization procedure now sends a message header to the console and then it restores the queue procedure addresses to their proper locations.	PH

Table 2-2. Console Procedure Errors (cont)

Description	Error Type
X013F The program called the line procedure to service an item posted to one of its queues, but the procedure could not identify the intended queue.	ES
X023F The program called the line procedure handler to service an item posted to one of its queues, but the procedure could not find an item in any of its queues. Note that in X013F, an item was found but could not be identified. In this case, no items were found.	ES
X033F One of the queues serviced by the LPH would not arm, even though there were not more items on that queue.	ES
X043F The program was processing an output message by adding the necessary headers to it. Any program hangs in this area of the code are probably caused by addressing problems.	PH
X053F The correct output MCT could not be queued to the PP queues and could not be queued to the link area of the LPLH. The program has entered a series of infinite loops. Possible causes of the error are a hardware fault in either the CLC/line module logic or the microcode routines which emulate the queue instructions.	ES
X063F The link area that is used to store the console messages is full, indicating a problem in communication with the serial terminal. As a result, the message transfer has slowed or has come to a complete stop.	ES

Table 2-2. Console Procedure Errors (cont)

Description	Error Type
X073F The serial PP did not complete the execution of the first output poll to the terminal, indicating a problem with one of the following: the serial line module, the L-bus, the modem or DCMS (if used), or their associated cables.	ES
X083F The PP completed the output poll and immediately looked for input. There was no answer so the poll was repeated. The procedure was retried until the search timer expired. 1. Check that the console terminal is powered-on and that it is attached to the line specified in the parameters (GR1).	ES
X093F The console has experienced at least 30 data transmission errors since beginning operation or since last making this report. 1. Check the line or change to a terminal on another line.	ES
X0A3F Errors in console operations have forced the executive to try a recovery program. If this error code is displayed on the console, then the recovery was successful. If the program stopped at the error stop address, then the recovery operation failed.	ES

Table 2-2. Console Procedure Errors (cont)

Description	Error Type
X0B3F	ES
The console PP was turned off during operation. If this error code is displayed on the console, then recovery was successful. If the program stopped at the error stop address, then recovery failed and a reboot is required. The error code presented in the PP state item is displayed on the console or the maintenance panels. Perform one of the folllowing actions: 1. Change to a console on another line. 2. Replace line components one at a time, beginning with the line module PCA.	
X0C3F	ES
The PP output queue was full and could not be cleared and is holding up operations until the PP catches up. If this error code is displayed on the console, then recovery was successful. If the program stopped at the error stop address, then recovery failed.	
X0D3F	ES
The console terminal sent a disconnect status to the program, indicating that it was going offline.	
X0157	PH
The program established visibility to the input MCT and checked its buffer for any expected input. If no input was expected, the message was queued to discard. Possible cause of problem is an error in one of the following: the SDR logic, the queue logic and instruction interpretation, the storage addressing. Also possible is microcode contamination.	
X0255	PH
The program calculated an index into the destination message and gained access to it through the SDRs. See X0157 for possible causes of error.	

Table 2-2. Console Procedure Errors (cont)

Description	Error Type
X0355 The program could not find an SOE on the front of the message. Possible problems are: 1. Line module hardware is losing the byte or deleting it from the message by interpreting a control bit incorrectly. 2. The L-bus is dropping data intermittently. 3. The storage area containing the MCT data area is experiencing intermittent data errors.	ES
X0455 The message was transferred to the message file and then the program tried to queue the MCT and its buffers to the discard queue. After calling discard to clear the queue, it still would not accept the item.	ES
X0555 The program set up a special destination address in the queue header to notify the procedure that was waiting for console input that it had arrived. The address was queued to the queue list which then sent the notification. Possible hardware problems associated with the error are either the queue control or the microcode and/or microprogram memory connected with the queue control.	PH
X0164 Entered the CONSOUT procedure.	PH
X0264 CONSOUT procedure was saving control and process mode SDRs and checking the screen buffer.	PH
X0364 State item found on console PP state item queue.	ES
X0464 Building new entry, transferring call parameters, saving the MCI, saving embedded message area, and checking the callers process ID.	PH

Table 2-2. Console Procedure Errors (cont)

Description	Error Type
X0564 Failed getting visibility to output message.	ES
X0764 Failed to queue output MCT to CONS LPH.	ES
X0864 Failed to build subsegment table for console stacks.	PH
X0964 Failed to load SDR 16 with SSN from previous build subsequent call.	ES
X0165 Received bad status from LDSDREG routine while attempting to get visibility to load file stacks.	ES
X0265 Nothing found in the message file stacks.	ES
X0365 Received bad status from PARSER routine after attempting to load a message ELT from load source.	ES
X0465 Verification bit not set after finding a match for a message ELT in the load file stacks.	ES
X0565 Could not find the stack pointer using the load file ID to find the match.	ES
X0665 Either an SSN is missing or the message index is too large to find an SSN to match it.	ES
X0765 Received bad status from LDSDREG routine when removing visibility to stacks using SDR 16.	ES

Table 2-2. Console Procedure Errors (cont)

Description	Error Type
X0865 Received bad status from LDSDREG routine when getting visibility to message ELT using callers SDR.	ES
X0965 Received bad status from BLDSSTAB when attempting to build a load file stack.	ES
X0A65 Received bad status from LDSDREG routine using the previously built SSN from BLDSSTAB.	ES
X0B65 ADSTORE routine failed to provide a 4K segment of memory.	ES
X0C65 LDSDREG routine failed to load control SDR 31 with the SSN provided by ADSTORE.	ES
X0D65 LDSDREG failed to load process mode SDR 31 with the SSN provided by ADSTORE.	ES
X0E65 Load file ID was not found in the load file stacks when asked to remove message ELT by caller.	ES
X0F65 The stack pointer provided by the ID match-up in the load file stacks was not valid.	ES
X0157 Failed to arm CONINLPH queue.	ES

Table 2-2. Console Procedure Errors (cont)

Description	Error Type
X0257 Unsatisfactory return from MESSVIS routine.	ES
X0357 SOE not found on input message.	ES
X01065 Received bad status from ADSTERE after attempting to remove a message ELT and returning memory to the system.	ES

The executive loader handles errors in two ways:

1. If the console is operative, the loader displays a single message or a combination of messages describing a specific error and recovery is attempted. If recovery is unsuccessful, then the executive is reinitialized.

2. If the console is inoperative, then an error stop occurs and the error code is displayed.

The error messages are listed first and a brief description follows each one. Table 2-3 summarizes the executive loader error codes.

* * * LOADER * * * module XX XXXXXX

This message precedes all loader messages. A 2-digit hexadecimal is given and a 6-character name is displayed.

PORT PROCESSOR DID NOT RESPOND

Indicates hardware problem. Two retrys are attempted

INPUT / OUTPUT FUNCTION DID NOT COMPLETE

Indicates hardware problem. Two retrys are attempted.

INPUT / OUTPUT ERROR

Indicates hardware problem. Two retrys are attempted.

ATTEMPTING RECOVERY

Self-explanatory.

THE TRACK / SECTOR OR LOGICAL BLOCK IS

Information will show on screen. For 8-inch diskette, a two-digit hexadecimal number gives track identification (TT), and a two-digit hexadecimal number gives sector (SS) identification. For 5-1/4 inch diskettes, the logical block (LLLL) is given.

LOAD MODULE NAME ERROR, CHECK MEDIA, MENU SELECTION

Directory name on the diskette did not match the name from the internal directory.

CANNOT ACQUIRE STORAGE. RETURNING TO CALLER

May be a normal occurrence under certain conditions, such as internal diskette copy utility.

CANNOT RELEASE SSN

Information shows on screen. XXXX - Executive function which returns storage to the unused pool failed. Usually indicates storage corruption in the executive program space.

LOAD RECORD SEQUENCE ERROR. CHECK MEDIA

Software detected error. Load records were out of sequence for the module being loaded. Usually indicates media or load device problem. May also be storage or hardware architectural problem.

LOAD FILE I.D. IS INCORRECT. CHECK MEDIA

Software detected error. File identifier code read from diskette did not match the internal directory for this load module. Usually indicates media or load device problem. May also be storage or hardware architectural problem.

LOAD RECORD LRC ERROR, CHECK MEDIA

Software detected error. The longitudal redundancy check character for the load record did not match the one calculated. Usually indicates media or load device problem. May also be storage or hardware architectural problem.

ILLOGICAL PARAMETERS FROM CALLING PROCEDURE

Information displays on screen. Parameters passed from the calling program module do not make sense. Indicates storage or storage addressing problems in the area addressed by control mode SDR5.

EXPECTED

Screen displays 16- or 32-bit data in hexadecimal. Supplemental to other messages.

RECEIVED

Screen displays 16 or 32 bit data in hexadecimal. Supplemental to other messages.

LOAD RECORD FORMAT ERROR / CHECK MEDIA

Software detected error. The record type was invalid or no end of record sentinal was found. Usually indicates media or load device problem. May also be storage or hardware architectural problem.

THE LOAD FILE ID / RECORD NUMBER IS LLRR

Screen shows information. Two-digit load file id and two-digit record number (hex) of the record currently being processed.

THE LOADER PP FLAG WORD IS XXXX

Screen shows information. Hexadecimal display of 16-bit PP flag word. Shows state of PP.

UNRECOVERABLE ERROR - RESTARTING EXECUTIVE

Self-explanatory.

Press TRANSMIT to continue

Self-explanatory.

STATUS (16 bits) is:

Self-explanatory. Screen shows information.

STATUS (32 bits) is:

Self-explanatory. Screen shows information.

The Error code (in hexadecimal) is:

Self-explanatory. Screen shows information.

ERROR...NO ENTRIES WERE FOUND IN THE DISK DIRECTORY

The module to be loaded, as requested by the calling program, could not be found in the internal directory. Indicates storage corruption.

PLEASE CHANGE THE DISKETTE IN THE INTERNAL DRIVE

Self-explanatory.

TO DISKETTE #

Self-explanatory. Screen shows information.

ERROR: P.P. STATE ITEM OCCURRED

State item display will follow.

The error codes for the executive loader and the IFDC/MDLM handler portions of the macrodiagnostic program contain four digits. Interpret the codes as follows:

- The first two digits identify the error and are contained in the upper part of R0 in the DCP/40/20 and in the first E0 display of the DCP/10/10A/15.
- The second two digits identify the procedure number (PN+30) in which the error occurred and are contained in the lower part of R0 and in the second E0 display.

Table 2-3. Executive Loader Error Codes

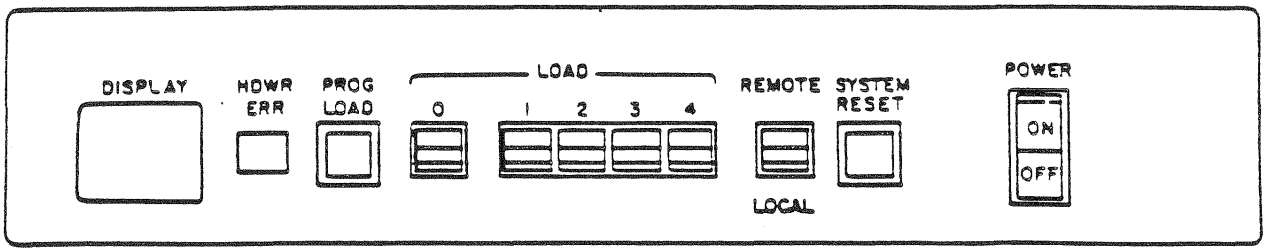
Error Code	Description
	NOTE Executive software timing problems can cause error X013A; however that error and error X023A are usually caused by a hardware failure: either a bit flips in storage or SDR logic problems occur.
X013A	Could not release storage segment to memory manager.
X023A	Could not get visibility to load table or loader PP. Indicates system information table in SDR5 has been corrupted.
X043A	Requested load module could not be found in the load table.
X053A	Illogical or invalid parameters were received from caller. Parameter passing area in system information has been corrupted, possibly due to a forced call.
X073A	Could not acquire working storage from memory manager.
X093A	Could not load an SDR. Invalid SSN received from memory manager.

Table 2-4. IFDC/MLDM Handler Error Codes

Error Code	Description
	NOTE E0/R0 LOWER = 47 (XX) for 8-inch diskette handler E0/R0 LOWER = 59 (XX) FOR MDLM loader
X0447	Directory entry not found on 8-inch diskette. Media may be defective.
X0459	Directory entry not found on 5 1/4-inch diskette. Media may be defective.
X0C47	PP would not start for 8-inch diskette.
X0C59	PP would not start for 5 1/4-inch diskette.

2.5. The Operator Panel of the DCP/10/10A/15

The operator panel of the DCP/10/10A/15 contains the controls to operate the macrodiagnostics and a two-digit display indicator that shows the status of the program load and the error conditions. The controls and indicators are explained in Figure 2-6.



POWER	Applies or removes primary power for all components within the cabinet and initiates microprogram load when power is switched on.
SYSTEM RESET	Reinitializes entire system processor and storage. Processor is returned to zero state, storage is cleared, and microcode and macrocode load is initiated.
REMOTE/LOCAL	Selects either operator panel or a remote device as controller for system reset, program load, or load path selection.
LOAD (0-4)	Selects load device for Telcon system software and macrodiagnostic software.
PROG LOAD	Initiates program load from local mass storage.
HDWR ERR	Indicates hardware failure.
DISPLAY	Indicates diagnostic code for microcode or macrocode error.

Figure 2-6. Operator Panel of the DCP/10/10A/15

2.6. The Maintenance Panels of the DCP/40 and the DCP/20

The CP maintenance panel of the DCP/40 and the CLC maintenance panel of the DCP/20 contain the controls and indicators to operate the microprograms and the macroprograms and to troubleshoot error conditions. To effectively utilize the macrodiagnostics, you must be familiar with the operation of the panels. The functions of the switch settings are summarized in the following figures:

Figure 2-7. CP Maintenance Panel Controls and Indicators
Figure 2-8. DCP/40 System Control Panel
Figure 2-9. CLC Maintenance Panel Controls and Indicators

Detailed descriptions of the DCP/40 processor panel are contained in MR6160, SPERRY DCP/40 Type 8596 and Expansion Cabinet Type 1945 Functional Analysis and Servicing and MR6328, SPERRY DCP/40 Type 8596 Troubleshooting Guide. The CLC maintenance panel is discussed in MR6170, SPERRY DCP/20 Type 8597-00 and Expansion Cabinet Type 8597-01 Functional Analysis and Servicing.

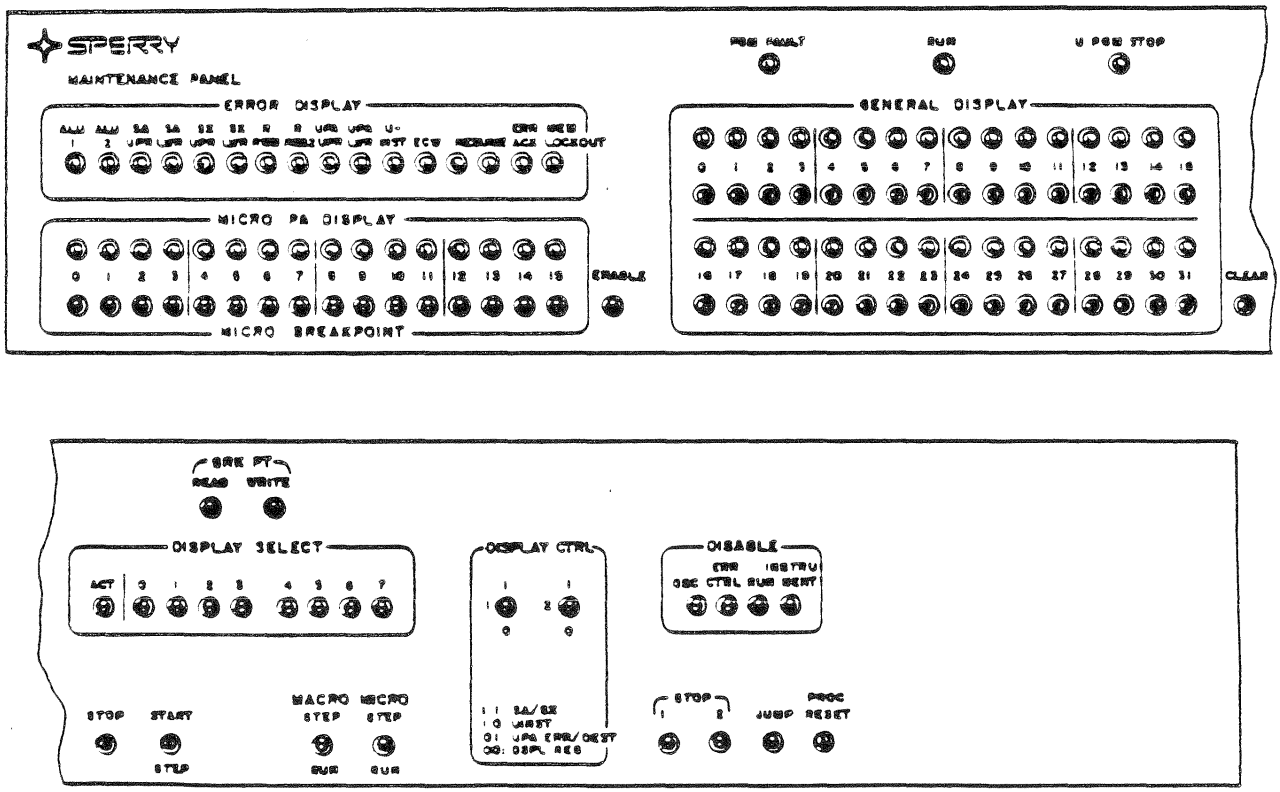


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Figure 2-7. CP Maintenance Panel Controls and Indicators (Sheet 1 of 7)

DISABLE — Four 2-position toggle switches which function as follows:

- OSC — This switch controls the microinterrupts to increase or decrease the real-time and monitor clocks. In the up position, switch inhibits the microlevel interrupts which increment the clocks. In the down position, this switch is inactive.
- ERR CTRL — This switch controls error reporting. In the up position, it disables hardware errors, microinterrupts, and error reporting to the software. Note that this switch does not disable error-detecting circuitry on buses and regulators of the processor. In the down position, this switch allows error reporting.
- RUN — This switch is used only for troubleshooting microcode. In the up position, this switch prevents the START/STEP switch from initiating a macrostart signal to allow microstepping without macrostart. In the down position, this switch is inactive.
- INSTRUMENTATION — This switch is not used.

PROC RESET — This momentary pushbutton switch initiates processor reset. Note that this switch does not initiate program reload or system reset.

JUMP — This two-position toggle switch is monitored by the macroprogram to control a program jump. In the up position, this switch is interrogated by the macroprogram to cause a program jump.

STOP 1 and 2 — These two-position toggle switches are interrogated by the macroprogram to control a program halt. In the up position, either switch can cause a program halt.

DISPLAY CONTROL — These two-position toggle switches select the display mode of the GENERAL DISPLAY indicators and switches. In the up position, the switches are set to 0's.

Figure 2-7. CP Maintenance Panel Controls and Indicators (Sheet 2 of 7)

DISPLAY CONTROL (cont) Codes used and their corresponding functions are:

Code	Label	Function
00	DISPL REG	Displays the contents of the R1/R2 register.
01	UPA ERR/DEST	Displays the contents of the microprogram address error register and the destination bus.
10	UINST	Displays the microinstruction being executed.
11	SA/SX	Displays the contents of the SA and SX buses.

DISPLAY SELECT These eight 2-position toggle switches enter a binary code into the processor. In the up position, the switches are set to 1. In the down position, the switches are set to 0. The microprogram interprets these codes to select the function of the the GENERAL DISPLAY indicators. The microprogram must be loaded and in control to perform these functions. Codes used and their corresponding displays are:

Code	Display
0000 XXXX	In the upper half of the GENERAL DISPLAY register displays the address of the last macroinstruction executed. In the lower half displays the address of the current macroinstruction.
0011 YYYY	Inspects and changes general register Y, addressed by DISPLAY SELECT switches 4 through 7. Program State Word (PSW) bit 17 selects which set of 16 general registers may be selected (in processor control register 0).

Figure 2-7. CP Maintenance Panel Controls and Indicators (Sheet 3 of 7)

DISPLAY SELECT (cont)	Code	Display
	0100 XXXX	Displays in bits 8 through 31 the macrobreakpoint address (24-bit absolute byte address), which can be changed as required. Displays in bits 0 through 3, the supplementary error status for memory lockout errors. Displays in bits 4 through 7, the hardware ID as established by strapping. Bits 0 through 7 cannot be changed.
	0101 XXXX	Displays the address of the last instruction executed in bits 0 through 15 of the display register and the instruction itself in bits 16 through 31. This display cannot be changed.
	0110 XXXX	Displays the segment descriptor register addresses in bits 24 through 31 of the working address register.
	0111 YYYY	Displays processor control register YYYY.
	1000 XXXD	Sets, inspects, and changes the working address register that supplies the address required by several functions selected by the DISPLAY SELECT switches.
	1001 XXXD	Inspects and changes micromemory at location specified in bits 16 through 31 of the working address register.
	1010 XXXD	Inspects and changes the emulation control word addressed by bits 24 through 31 of the working address register.

Figure 2-7. CP Maintenance Panel Controls and Indicators (Sheet 4 of 7)

DISPLAY SELECT (cont)

Code	Display
1011 XXXD	Inspects and changes the constant stack address entry addressed by bits 24 through 31 of working address register.
1101 XXXX	Inspects and changes local storage at the absolute byte address contained in bits 8 through 31 of the working address register. Addressing any byte within a word selects and displays the entire word.
1110 XXXD	Inspects and changes local storage at the virtual address contained in bits 16 through 31 of the working address register. Only the lower 16 bits of the display register may be changed.
1111 YYYY	Displays system control register YYYY. SCR 15 may not be changed.

NOTE

X = Disregard switch setting
D = Activation control. If D = 1, pressing the ACT switch decrements the working address register. If D = 0, pressing the ACT switch increments the working address register.

BRKPT READ — In the up-position, this switch stops the processor when a read operation is attempted at an address specified by the macrobreakpoint register.

BRKPT WRITE — In the up position, this switch stops the processor when a write operation is attempted at an address specified by the macrobreakpoint register.

Figure 2-7. CP Maintenance Panel Controls and Indicators (Sheet 5 of 7)

MICRO STEP/RUN	In the STEP position, this switch conditions the processor to microstop after the execution of each microinstruction. The processor executes the next microinstruction only when the START/STEP switch is pressed. In the RUN position, the switch conditions the processor to execute the microinstruction continuously.
MACRO STEP/RUN	In the STEP position, the switch conditions the processor to macrostop after the execution of each macroinstruction. The processor executes the next macroinstruction only when the START/STEP switch is pressed. In the RUN postion, the switch conditions the processor to execute macroinstructions continuously.
START/STEP	This pushbutton switch starts the processor when it is halted and steps the processor one micro-instruction or macroinstruction at a time if either the MICRO STEP/RUN or the MACRO STEP/RUN switch is set to step.
STOP	This switch causes the processor to stop executing the macroprogram at the end of the current macro-instruction and to execute the microinstruction utility routines that service the general display register.
U PGM STOP	This indicator (microprogram stop) lights when the processor is not executing microinstructions.
RUN	This indicator lights when the processor is in macrorun state.
PGM FAULT	This indicator (program fault) is lit by the microcode when an unrecoverable software error is detected. Note that during initialization of the system and during manual operation, this indicator may be lit when there is no error. Also, this indicator may flicker as recoverable errors are processed.

Figure 2-7. CP Maintenance Panel Controls and Indicators (Sheet 6 of 7)

CLEAR — This momentary pushbutton switch clears the GENERAL DISPLAY only when an inspect and change operation is performed.

ERROR DISPLAY — The indicators light to indicate a hardware-detected error condition. Errors corresponding to individual indicators are:

ALU 1	ALU comparison failure 1
ALU 2	ALU comparison failure 2
SA UPR	Parity error on upper byte of SA bus
SA LWR	Parity error on lower byte of SA bus
SX UPR	Parity error on upper byte of SX bus
SX LWR	Parity error on lower byte of SX bus
R REG 1	Parity error on R1
R REG 2	Parity error on R2
U PA UPR	Parity error on upper byte of microprogram counter
U PA LWR	Parity error on lower byte of microprogram counter
U-INST	Parity error on microinstruction
ECW	Parity error on emulation control word
RESUME	Reference to nonexisting or non-responding local storage
ERR ACK	Uncorrectable storage error
MEM LOCKOUT	Storage protection violation

MICRO PA DISPLAY — Address of the next microinstruction to be executed. Lighted indicators represent a value of 1 for corresponding bit.

MICRO BREAKPOINT — These two-position toggle switches allow the operator to specify a microprogram breakpoint. The up position selects 1 for the corresponding bit. The down position selects 0 for the same bit.

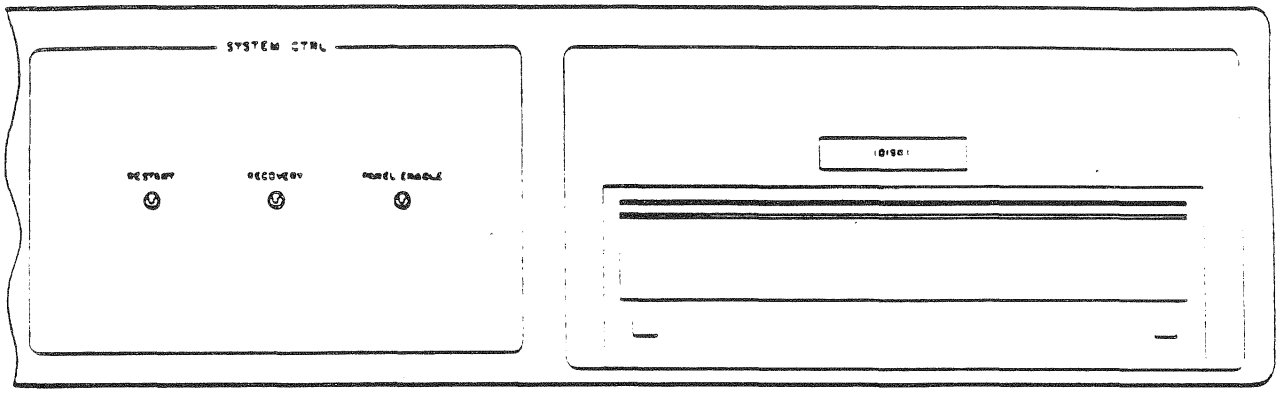
ENABLE — This two-position toggle switch controls the microprogram breakpoint function. In the up position, the switch enables the breakpoint action. In the down position, the breakpoint function is disabled.

Figure 2-7. CP Maintenance Panel Controls and Indicators (Sheet 7 of 7)

The CLC maintenance panel of the DCP/40 contains three areas: the integrated diskette, the system control panel, and the CLC maintenance panel.

The integrated diskette has no controls, but a busy light is located in the door. When a system reset command is initiated, the light is on during the loading of the microcode and macrocode programs.

The system control panel controls the automatic operation of the DCP/40 system. It also contains the PANEL ENABLE switch.



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NOTE

Set PANEL ENABLE in down position before locking the cabinet when maintenance is completed.

PANEL ENABLE — This two-position toggle switch selects the manual or automatic mode and enables or disables the controls of the processor and CLC panels. In the up position, the switch places the DCP/40 in manual mode and enables the maintenance panels. In the down position, the switch places the DCP/40 in automatic mode and disables the maintenance panels. In this position, the switch also enables the RESTART switch on the operator panel.

Figure 2-8. DCP/40 System Control Panel (Sheet 1 of 2)

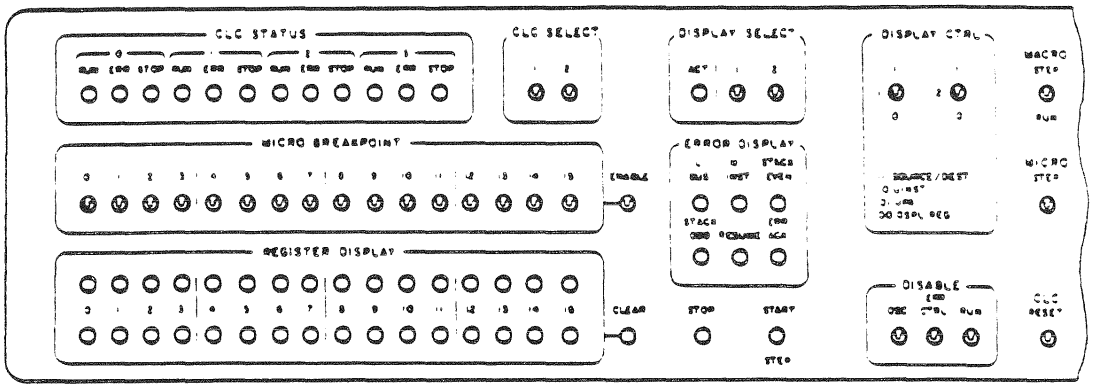
RECOVERY	This two-position toggle switch controls requests for software program recovery operations. In the up (recovery) position, this switch initiates a request for software program recovery operations. However, if program load occurs as a part of power-up or system reset operations, this recovery request is not initiated. In the down position, no recovery requests are initiated.
RESTART	This switch determines the action taken by the microprogram for certain software, hardware, and microprogram errors. In the up (restart position), this switch causes the microprogram to initiate automatic recovery from certain non-recoverable software, hardware, and microprogram errors. Note that the PANEL ENABLE switch must be down (disabled) to allow the RESTART switch to function. In the down position, this switch causes the system to stop when an error occurs.

Figure 2-8. DCP/40 System Control Panel (Sheet 2 Of 2)

In the DCP/40, the CLC maintenance panel controls the CLC portion of the system and can be shared by one to four CLC units. The panel provides the basic controls to operate the CLC which was selected by the CLC select switches. A thorough working knowledge of the panel is not required to operate the macrodiagnostics; however, the customer engineer should be aware of the error indicators and their functions. Refer to DR2547, for a detailed explanation of these indicators and the hardware errors associated with them.

In the DCP/20, the CLC maintenance panel controls all of the operations of the system. The figure that follows identifies the functions of the switch settings for both the DCP/20 and the DCP/40.

DCP/40



DCP/20

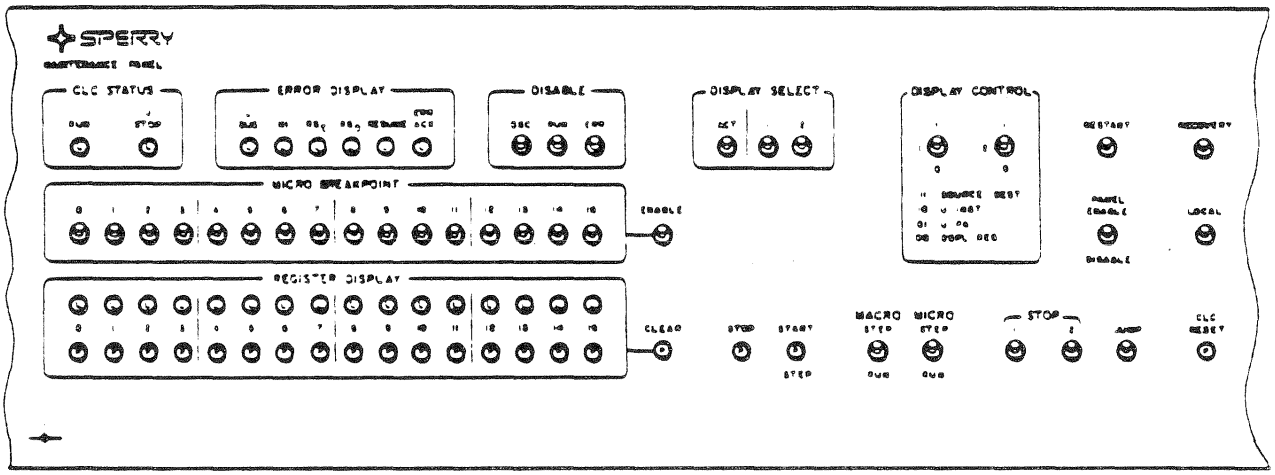


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Figure 2-9. CLC Maintenance Panel Controls and Indicators (Sheet 1 of 6)

CLC SELECT (DCP/40 only)

Select CLCs 0 through 3. Most of the switches and indicators are active only for the one CLC that is selected by these switches. The up position sets the switches 1; the down position sets them to 0:

Code	CLC Selected
00	0
01	1
02	2
03	3

CLC STATUS (DCP/40)

The 12 status indicators are divided into sets of three, one set for each CLC unit 0 through 3. These indicators operate at all times and are not dependent on the PANEL ENABLE switch or the CLC SELECT switches.

RUN — When lit, indicates that the CLC macroprogram is in the run mode.

ERR — When lit, indicates that the CLC has one or more hardware errors.

STOP — When lit, indicates that the CLC microprogram is stopped.

CLC STATUS (DCP/20)

The two status indicators operate at all times and are not dependent on the PANEL ENABLE switch.

RUN — When lit, indicates that the CLC macroprogram is in the run mode.

U STOP — When lit, indicates that the microinstruction sequencing in the CLC stopped. A microstop condition is caused by a microbreakpoint stop, a microstop from the maintenance panel, or a stop after execution of a stop microinstruction.

DISPLAY SELECT 1 and 2

Enter a code which identifies the display on the REGISTER DISPLAY indicators.

DISPLAY SELECT ACT

Steps the selected microprogram to the next address for display on the REGISTER DISPLAY indicators.

Figure 2-9. CLC Maintenance Panel Controls and Indicators (Sheet 2 of 6)

MACRO STEP/RUN — Controls the macro-operating mode of the CLC. In the STEP position, the switch stops the CLC and executes a single macroinstruction each time the START switch is pressed. In the RUN position, the switch allows the CLC unit to run continuously.

MICRO STEP/RUN — Controls the micro-operating mode of the selected CLC. In STEP position, this switch stops the CLC and executes a single microinstruction each time the START switch is pressed. In the RUN position, this switch allows the CLC unit to run continuously.

STOP — Causes the CLC to enter the macrostop mode

START/STEP — Microsteps the CLC when the MICRO STEP/RUN switch is set to STEP. It starts the CLC for the duration of one macroinstruction when the MACRO STEP/RUN switch is set to STEP. It also starts the macro-run mode when the MACRO STEP/RUN switch is set to RUN.

CLC RESET — Master clears the CLC. When this switch is pressed, the microprogram address is set to 0.

DISPLAY CTRL 1 and 2 — Select the data to be displayed for the CLC by the REGISTER DISPLAY indicators. The codes and the displays are:

Code	Label	Display
11	SOURCE/DEST	Contents of source and destination buses
10	UINST	Microinstruction currently executing
01	U PA	Microprogram address
00	DISP REG	Contents of CLC display register

Figure 2-9. CLC Maintenance Panel Controls and Indicators (Sheet 3 of 6)

DISABLE:	
OSC	Controls the clock signal in the CLC unit. In the up (disabled) position, it disables the clock signal. In the down position, the switch is inactive.
ERR CTRL	Controls the reaction of the CLC to hardware errors. In the up (disabled) position, it prevents hardware errors from interrupting the micro-program. However, these errors are still shown on the error indicators. In the down position, it is inactive.
RUN	Places the CLC unit in macrostop mode and holds it stopped, independent of the START switch. In the up (disabled) position, it stops the CLC unit and prevents the START/STEP switch from initiating a start signal. (If the CLC unit is in macrorun mode when this switch is set to the disabled position, the START and STOP switches must be pressed to place the CLC in macrostop mode.) In the down position, it is inactive.
ERROR DISPLAY	Lights when hardware errors occur in the CLC. Errors corresponding to the individual indicators are:
L BUS	Parity error on the L bus
MI/M INST	Parity error on microinstruction
RSE/STACK EVEN	Parity error on register stack (even byte)
RSO/STACK ODD	Parity error on regsiter stack (odd byte)
RESUME	Storage resume error
ERR ACK	Storage error acknowledgement
MICRO BREAKPOINT	Sets a microprogram address for breakpoint operations. The address is specified for all CLCs on the DCP/40, but is used only by the selected CLC unit. The address is used only if breakpoint enable is set. The up position selects a 1 value. The down position selects a 0 value.

Figure 2-9. CLC Maintenance Panel Controls and Indicators (Sheet 4 of 6)

MICRO BREAKPOINT ENABLE	Controls the microprogram breakpoint function. In the up position, it enables the breakpoint operation. In the down position, the function is disabled.
REGISTER DISPLAY	Provides display and input for the CLC unit. The displayed data is selected by the DISPLAY CNTRL switches. Pressing a given switch causes the corresponding indicator to light, but it will not stay lit after the switch is released unless the CLC display register content is modified by the CLC microprogram.
REGISTER switch	Clears the REGISTER DISPLAY for the CLC. The actual clearing of the CLC register is done by the microprogram, so the CLC must be operating when this switch is used.

NOTE

The following switches for the DCP/20 correspond to switches on the System Control Panel and the CP Maintenance Panel of the DCP/40.

STOP 1 and 2	In the up (active) position, either switch causes a program halt when interrogated by the macroprogram.
JUMP	In the up (active) position, causes a program branch to jump when the switch is interrogated by the macroprogram.
RECOVERY	When set to on (up) position, causes a macroprogram dump whenever an auto restart or program load sequence is initiated.
RESTART	When set to on (up) position, initiates an auto restart (initial macroload procedure). When set to off (down) position and PANEL ENABLE/DISABLE is in ENABLE position, causes the CLC to macrostop. When PANEL ENABLE/DISABLE is in DISABLE position, a restart is initiated, regardless of position of RESTART switch.

Figure 2-9. CLC Maintenance Panel Controls and Indicators (Sheet 5 of 6)

PANEL ENABLE/ DISABLE	When set to ENABLE postion, enables the controls on the maintenance panel and disables the LOAD switches on the operator panel. When set to DISABLE position, inhibits all controls on the maintenance panel except RESTART and enables LOAD switches on operator panel.
LOCAL (DCP/20 only)	When set to up position, inhibits both system reset and program load functions originating in other cabinets in the system.

Figure 2-9. CLC Maintenance Panel Controls and Indicators (Sheet 6 of 6)

3. LOCAL STORAGE DIAGNOSTIC TEST

3.1. Introduction

The local storage diagnostic test verifies the error correction code (ECC) logic and checks all of the local storage locations except the area where the diagnostic test resides.

3.2. Test Procedure

When the local storage test is selected, the console displays a series of requests for configuration and execution parameters.

```
CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1
            LOCAL STORAGE (Memory) TEST
256K


     *****WARNING*****
THE USE OF THE KEYBOARD KEYS TO INTERRUPT THIS PROGRAM OR THE USE
OF THE 4 OPTION AFTER AN ERROR MAY RESULT IN SOME PROGRAM INDUCED
PARITY ERRORS REMAINING IN MEMORY.  IF SO, IT WILL BE NECESSARY TO
USE THE SYSTEM RESET SWITCH TO CLEAR THE SYSTEM AND REBOOT THE EXEC
Press Transmit to Continue.
```

When the transmit key is pressed, the test selections scroll onto the screen six lines at a time, followed by the prompt:

```
PRESS TRANSMIT KEY TO DISPLAY OTHER SELECTIONS, OR
SELECT A TEST NUMBER FROM THE MENU
```

The complete test list for the DCP/20-DCP/40 is:

```
TEST NUMBERS ARE AS FOLLOWS:
 1. -  VERIFY ADDRESS
 2. -  TRANSPARENT READ
 3. -  ECC LOGIC
 4. -  STATUS LOG READ/WRITE
 5. -  WRITE ARRAY STATUS FLAGS
 6. -  TWO-BIT ERROR SYNDROME
 7. -  PORT NUMBER AND ERROR REGISTER
 8. -  FULL WORD WRITE-ZEROS
 9. -  FULL WORD WRITE-ONES
10. -  FULL WORD SLIDING ONES
11. -  FULL WORD SLIDING ZEROS
12. -  SINGLE BYTE WRITE ZEROS
13. -  SINGLE BYTE WRITE ONES
14. -  TWO BYTE WRITE ZEROS
15. -  TWO BYTE WRITE ONES
16. -  THREE BYTE WRITE ZEROS
17. -  THREE BYTE WRITE ONES
18. -  WRITE MEMORY BY BYTES WITH ONES
19. -  WRITE MEMORY BY BYTES WITH ZEROS
20. -  FULL WORD WRITE TEST
21. -  MARCH PATTERN TEST
22. -  SLIDING DIAGONAL TEST
```

The complete test list for the DCP/10/10A/15 is:

```
TEST NUMBERS ARE AS FOLLOWS:
 1 - Verify Address
 2 - Transparent Read
 3 - ECC Logic
 4 - Two-bit Error Syndrome
 5 - March Pattern Test
 6 - Sliding Diagonal Test
```

NOTE

Test 1, VERIFY ADDRESS, must be executed first.

1. Keep pressing TRANSMIT key, if necessary, to display all of the tests, or enter the test number. The next prompt follows.

```
>ENTER TEST NUMBER, OR 0 (ALL), OR (STRING OF TESTS)
>[]
```

2. To select a string of tests, enter the selection number separated by commas: 1,2,10,11,etc. The string must include test 1.

```
>DO YOU WISH TO RUN THE LONG TEST? (0=NO, 1=YES, DEFAULT=0)
>[]
```

3. Select the length of the test. The short test checks the first storage location in each array to verify instructions and data paths. The long test performs each test on every memory location and requires an extended time for operation (See Figure 3-1).

	DCP/40				DCP/20	
	512K Bank		2M Bank		512K BANK	
Test No.	Short	Long	Short	Long	Short	Long
1	-*	-	16 sec.	16 sec.	20 sec.	20 sec.
2	12 sec.	12 sec.	48 sec.	48 sec.	48 sec.	48 sec.
3	12 sec.	1 hr., 50 min.	48 sec.	6 hr., 20 min.	48 sec.	2 hr.
4	-	-	-	-	-	-
5	-	-	-	-	-	-
6	-	-	-	-	-	-
7	-	-	-	-	-	-
8	20 sec.	20 sec.	1 min., 40 sec.	1 min., 40 sec.	1.25 min.	1.25 min.
9	1 min., 20 sec.	1 min., 20 sec.	6 min.	6 min.	5.25 min.	5.25 min.
10	-	12 min.	12 min.	48 min.	-	15 min.
11	-	12 min.	12 min.	48 min.	-	15 min.
12	-	5 min.	5 min.+	20 min.	-	7 min.
13	-	2 min., 10 sec.	2 min.+	9 min.	-	3 min.
14	-	4 min.	4 min.	16 min.	-	5 min.
15	-	3 min.+	3 min.+	13 min.	-	4 min.
16	-	3 min.	3 min.+	13 min.	-	4 min.
17	-	3 min.	3 min.+	13 min.	-	10 min., 40 sec.
18						
19						
20						
21						
22						

*Negligible

Figure 3-1. Test Execution Times Per Bank of Memory (Sheet 1 of 2)

DCP/10/10A/15

Test No.	1M Bank DCP/10 Short	1M Bank Long	2M Bank DCP/10 Short	2M Bank DCP/15 Long	2-1/2M Bank DCP/10 Short	2-1/2M Bank Long
1	50 sec.		100 sec.	39 sec.	150 sec.	
2	2 min., 30 sec.		5 min.	1 min., 15 sec.	7 min., 30 sec.	
3	1 min. 30 sec.		3 min.		4 min. 30 sec.	
4	7 sec.		14 sec.	4 sec.	21 sec.	
5	1 min. 50 sec.		3 min., 40 sec.	1 min. 23 sec.	5 min., 30 sec.	
6	2 hrs., 12 min.		4 hrs., 24 min.	1 hr., 5 min.	6 hrs., 36 min.	

Figure 3-1. Test Execution Times Per Bank of Memory (Sheet 2 of 2)

```
>ENTER THE NUMBER OF CYCLES FOR WHICH EACH TEST IS TO BE
EXECUTED
>(0-FFFF, OR I (=INFINITE), D = 1)
>[]
```

4. Select the number of times the tests will execute.

As the diagnostic test executes, the screen displays test information. A sample display follows:

```
          CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1
                    LOCAL STORAGE (Memory) TEST
CURRENT BYTE ADDRESS RANGE FOR TESTS: START=00000000 END=00000000
                              (line 3)
NOW EXECUTING TEST 0003                          CYCLES = 0001
                              (line 4)
256K      1.0 MEG
                              (line 5)


TEST NUMBER COMPLETED 0001
TEST NUMBER COMPLETED 0002
```

The information on line 3 is updated as the test progresses through local storage. The cycle count is updated at the completion of each test. Line 5 provides configuration data for the DCP/10 or the DCP/10A.

The console displays the following message at the completion of all test cycles or when an error occurs:

```
>NEXT OPERATION?
>ENTER 1 (CONTINUE), 2 (REPEAT), 3 (START), 4 (EXIT)
>[]
```

where:

1 = At test completion, returns to test selection.
  = After an error, continues where the error occurred.
2 = Repeats the current test.
3 = Returns to start of diagnostic test.
4 = Exits diagnostic and returns to system executive.

3.3. Error Reporting

The console displays all of the errors. If an error occurs during test parameterization, you are informed of the error but there is no error code. If an error occurs during execution of a test, the console displays an error message and/or an error code. The format of the error code is:

```
***FATAL ERROR***
*ERROR CODE = XXXX
R0-R7 = XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
R8-R15= XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
```

CAUTION

When an error occurs, select option 1 (CONTINUE). If any other option is selected, program stops and SYSTEM RESET must be pressed to clear the system and reboot the executive.

The prompt, TELL ME WHAT TO DO, follows the display of the content of the registers.

The following list summarizes the error messages and codes. Perform the action recommended in the list or refer to Appendix A for the trouble isolation procedure associated with the error.

Error Message/Code Description	Isolation Procedure
INVALID INPUT, TRY AGAIN ILLEGAL DIGIT - RETRY OUT OF RANGE - RETRY A solicited input cannot be translated properly; for example, there is an alpha character in a decimal input.	- - -
THERE IS NO ANSWER FROM THAT ARRAY The array PCA is not present or cannot respond because a memory resume was received. Check memory configuration or go to isolation procedure.	00003
YOU MAY NOT TEST THE STORAGE AREA IN WHICH THE DIAGNOSTIC RESIDES. The diagnostic macrocode resides in the selected storage area. Select another array.	-
COULD NOT FIND ANY ARRAY CARDS IN LOCAL STORAGE The array PCA is not present or cannot respond. Check memory configuration or go to isolation procedure.	00003
RECEIVED AN UNEXPECTED MEMORY RESUME A memory resume occurred that was not part of the diagnostic design.	00003
*INCORRECT STATUS RECEVIED ON FORCED CALL PNO *STATUS = XXXX *ERROR CODE = XXXX The system executive received an unexpected status. Refer to Appendix B for status description.	-
*THE FORCED CALL PNO WAS NOT GENERATED BY THE CURRENT R/W INSTRUCTION *INSTRUCTION GENERATING HARDWARE FORCED CALL = XXXX *ERROR CODE = XXXX A forced call occurred during execution of the diagnostic but not during a read/write instruction. Refer to Appendix B for status description.	-

Error Message/Code Description	Isolation Procedure
001A (Test 1) Address verify failed during the first memory access. The upper 16 bits of the 32 bits of data returned by verify-address read instruction were all 0's. This instruction returns the address that is read in the lower bits and the data bank information in the higher order bits of the upper byte. In this case, bank information was not returned.	00001
001B (Test 1) Address verify failed. Same as 001A except this part of the routine executes the instruction on all other storage locations in the test area.	00001
001C (Test 1) Address verify failed. Bank ID in upper byte of returned data changed. See 001A.	00001
001D (Test 1) Address verify failed. Address returned was not the same as the one sent. See 001A. R4, R5 = returned address R12, R13 = expected address	00002
001E (Test 1) Unexpected memory-resume interrupt occurred.	00003
001F (Test 1) Address verify failed. Invalid bank ID of zero was returned.	00001
0020 (Test 1) Address verify failed. Either the bank ID (R4) was incorrect or the array PCAs are not in correct order.	00001
0021 (Test 1) Address verify failed. Local storage IC type was invalid. R4 = returned value	00004
0022 (Test 1) Data verify was incorrect. R5 = returned data value (should be all zeros)	00005

Error Message/Code Description	Isolation Procedure
0023 (Test 1) Storage initialization bits did not clear during initialization. R4, R5 = returned data Two MSBs of R4 contain initialization flip-flop states.	00006
0024 (Test 2) Data compare error occurred during transparent read routine. Test area was written to 0's or 1's. Read routine found one location that could not be set to 0's or 1's. R8, R9 = absolute byte address of location R4, R5 = received data R0, R11 = expected data.	00005
0025 (Test 3) Error occurred during ECC logic test. R4, R5 = received data Address TESPAT in memory plus offset in R14 = expected data pattern	00007
0026 (Test 3) ECC logic did not correct an error generated by diagnostic test. R4, R5 = received data R14 = expected data	00007
0027 (Test 3) ECC error log was not set after error correction. R8 and R9 contain the real address that the program was accessing during this test. Use the real address to determine the faulty array. Refer to Appendix A, Isolation Procedure 00002. R5 = log receive	00007
0028 (Test 3) After reading from a local storage address containing a specially created word with bad parity, the syndrome was incorrect even though the data was corrected.	00007

Error Message/Code Description	Isolation Procedure
0029 (Test 3) After reading from a local storage address containing a specially created word with bad parity, the check bits were incorrect. R3 = expected check bits R2 = received check bits	00007
002A (Test 3) When calculating the row address, the address given was not found in any of the legal memory banks. R8, R9 = given address	00008
002B (Test 3) When calculating the row address, the start address was not found in any of the rows. R8, R9 = expected data	00008
002C (Test 4) Write-log command wrote zeros to log. Read/verify detected that one of the locations was not set to zero. R5 = log bit in error. Expected data is zero R6, R7 = command and log address.	00009
002D (Test 4) All 1's written to status log. Error detected during log read (log bit was set). R5 = log bit R6, R7 = command and log address	00009
002E (Test 5) Write of all 0's to array card status flags failed. R4 = status flags R6, R7 = current storage address.	00010
002F (Test 5) Status flags were cleared and then written to 1's. One or both of the flags could not be set to 1. R4 = status flags (bits 4 - 7) R6, R7 = current storage address	00010

Error Message/Code Description	Isolation Procedure
0030 (Test 6) Two-bit error syndrome test wrote to first storage location of each storage bank and generated a two-bit error. Interrupt did not occur as expected. This test uses beginning address of each bank. R6, R7 = real storage address	00011
0031 (Test 6) Test checks error log to see if induced two-bit error was logged correctly. The log bit should be set. Either the error was logged incorrectly or the correct log entry could not be read. R5 = log bit R6, R7 = current storage address	00011
0032 (Test 6) Syndrome bits for test-induced two-bit error were incorrect. R4 = syndrome bits The bits are compared to the calculated syndrome bits found at address SYNDSV.	00011
0033 (Test 6) Two-bit error induced in storage location and error log syndrome bits verified. Check bits did not compare with computed check bits found in storage location CORCKB. R5 = check bits.	00011
0034 (Test 7) Port number and error register test did not detect interrupt for test-induced two-bit error. R6, R7 = command and address	00011
0035 (Test 7) Two-bit error induced in a storage location. Unrecoverable-read error code of 04 was not received as expected. R5 = error code	00011

Error Message/Code Description	Isolation Procedure
0036 (Test 7) Two-bit error induced in a storage location. Correct interrupt received but previous instruction did not clear port error register. R5 = content of port error register	00011
0037 (Test 7) Two-bit error induced in storage location. Error was not reported in error register. R2 = error register	00011
0038 (Test 8) Full-word-write to storage completed and syndrome checked. Syndrome should be zero. R4 = received syndrome R8, R9 = real storage address	00012
0039 (Test 8) Full-word-write-of-0's to storage completed with correct syndrome and incorrect check bits. R5 = received check bits R8, R9 = real storage address	00012
003A (Test 8) After clearing the log bit, a normal write to storage was executed and the error log was checked. The log reported an error following a normal write. R8, R9 = real storage address	00012
003B (Test 9) Full-word-write-of-all-1's to storage returned incorrect syndrome. R2 = expected syndrome R4 = received syndrome R8, R9 = real storage address	00012
003C (Test 9) Full-word-write-of-all-1's to storage returned correct syndrome and incorrect check bits. R2 = expected check bits R5 = received check bits	00012

Error Message/Code Description	Isolation Procedure
003D - 003E (Test 10) All 1's written to storage and syndrome and check bits verified. 003D indicates incorrect syndrome; 003E indicates incorrect check bits. R2 = expected syndrome R4 = received syndrome R8, R9 = real storage address	00013
0089 - 008A (Test 11) Sliding 0's written to storage and syndrome and check bits verified after each write. 0089 indicates incorrect syndrome; 008A indicates incorrect check bits. R2 = expected syndrome R4 = received syndrome R8, R9 = real storage address	00013
003F - 0040 (Test 12) Single-byte-write-of-0's to Byte 0 completed and syndrome and check bits verified. 003F indicates incorrect syndrome; 0040 indicates incorrect check bits. R2 = expected syndrome R4 = received syndrome R8, R9 = real storage address	00014
0041 - 0042 (Test 12) Single-byte-write-of-0's to Bytes 1 thru 3 completed and syndrome and check bits verified. 0041 indicates incorrect syndrome; 0042 indicates incorrect check bits. R2 = expected syndrome R4 = received syndrome R8, R9 = real storage address	00015
0043 - 0046 (Test 13) Single-byte-write-of-1's to Byte 0 completed and syndrome and check bits verified. 0043/0045 indicate incorrect syndrome; 0044/0046 indicate incorrect check bits. R2 = expected syndrome R4 = received syndrome R8, R9 = real storage address	00014

Error Message/Code Description	Isolation Procedure
004E - 0052, and 0059 (Test 14) Double-byte-write-of-0's to upper two bytes, middle two bytes, and lower two bytes completed and syndrome and check bits verified. For upper two bytes: 004E = incorrect syndrome 004F = incorrect check bits For middle two bytes: 0050 = incorrect syndrome 0059 = incorrect check bits For lower two bytes: 0051 = incorrect syndrome 0052 = incorrect check bits R2 = expected syndrome R4 = received syndrome R8, R9 = real storage address	00014
0053 - 00058 (Test 15) Double-byte-write-of-1's to upper two bytes, middle two bytes, and lower two bytes completed and syndrome and check bits verified. For upper two bytes: 0053 = incorrect syndrome 0054 = incorrect check bits For middle two bytes: 0055 = incorrect syndrome 0056 = incorrect check bits For lower two bytes: 0057 = incorrect syndrome 0058 = incorrect check bits R2 = expected syndrome R4 = received syndrome R8, R9 = real storage address	00014
0063 - 0066 (Test 16) Three-byte-write-of-0's to upper three bytes and lower three bytes completed and syndrome and check bits verified. For upper three bytes: 0063 = incorrect syndrome 0064 = incorrect check bits For lower three bytes: 0065 = incorrect syndrome 0066 = incorrect check bits R2 = expected syndrome R4 = received syndrome R8, R9 = real storage address	00014

Error Message/Code Description	Isolation Procedure
0067 - 006A (Test 17) Three-byte-write-of-1's to upper three bytes and to lower three bytes completed and syndrome and check bits verified. For upper three bytes: 0067 = incorrect syndrome 0068 = incorrect check bits For lower three bytes: 0069 = incorrect syndrome 006A = incorrect check bits R2 = expected syndrome R4 = received syndrome R8, R9 = real storage address	00014
0073 - 0074 (Test 18) Error log cleared and all-1's-written, one-byte-at-a-time. Log checked for any error correction. 0073 indicates incorrect data: R2, R3 = expected data R4, R5 = received data R8, R9 = real storage address 0074 indicates incorrect error log: R5 = log bit R6, R7 = real storage address	00014
0075 - 0076 (Test 19) Error log cleared and all 0's written, one-byte-at-a-time. Log checked for any error correction. 0075 indicates incorrect data: R2, R3 = expected data R4, R5 = received data R8, R9 = real storage address 0076 indicates incorrect error log: R5 = log bit R6, R7 = real storage address	00014

Error Message/Code Description	Isolation Procedure
0075 - 0076 (Test 19) Error log cleared and all 0's written, one-byte-at-a-time. Log checked for any error correction. 0075 indicates incorrect data: R2, R3 = expected data R4, R5 = received data R8, R9 = real storage address 0076 indicates incorrect error log: R5 = log bit R6, R7 = real storage address	00014
007F - 0080 (Test 20) Full-word-write of 0FF00FF00 pattern returned error. 007F indicates data error: R2, R3 = expected data R4, R5 = received data R8, R9 = real storage address 0080 indicates incorrect error log: R5 = log bit R6, R7 = real storage address	00014
0081 - 0083 (Test 21) March-data-pattern of 0's and 1's returned error. 0081 indicates location was not all 0's: R4, R5 = received data R8, R9 = real storage address 0082 indicates location was not all 1's: R4, R5 = received data R8, R9 = storage address 0083 indicates error correction occurred: R5 = log bit R6, R7 = real storage address	00014
0084 - 0085 (Test 22) Sliding 1's diagonal storage test returned error. 084 indicates error during 1's testing: 085 indicates error during 0's testing: R4, R5 = received data R4 should be all 1's R5 should be all 0's	00014

4. SERIAL LINE MODULE DIAGNOSTIC TEST

4.1. Introduction

The serial line module diagnostic test checks serial line modules of the DCP. The list that follows provides the type of line module, its feature number, and its line module ID.

Feature	Line Module	LMID
F1941	Asynchronous	40
F1942	Synchronous	50
F3163	Medium Speed Loadable (MSLLM)	
	- RS-449	60
	- X.21	61
	- RS-232C	67
	- Kintetsu	6B
	- No cable	6F
F3164	High Speed Loadable (HSLLM)	
	- RS-449	70
	- Bell 303	7D
	- V.35	7E
	- No cable	7F
F3165	Multiline (4X1) Asynchronous (MLALM)	
	- Asynchronous	44
	- Asynchronous Video Text	45
F3837	Multiline (4X1) Synchronous	54
F3847	Direct Connect Single Station (DCSS)	64
F4230	Twisted Pair (TPLM)	65

4.2. Test Procedure

When the serial line module test is selected from the system menu, the console displays a series of prompts which request the configuration and execution parameters of the diagnostic test:

```
CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1
SERIAL LINE MODULE TEST


>1 - TEST ALL SERIAL PORTS
>2 - TEST SINGLE PORT
>3 - TEST ALL PORTS ON A SINGLE IOP
>4 - TEST MULTIPLE PORTS (UP TO 16)
>MAKE SELECTION AND TRANSMIT
>[]
```

1. Enter selection number and press TRANSMIT key. The screen displays the following menu:

```
>ENTER MICROCODE TYPE TO BE TESTED
>1 = BASIC ASYNCH (LS/MS)
>2 = BASIC SYNCH (LS/MS)
>3 = UDLC (MS)
>4 = MULTILINE ASYNCH
>5 = X.21 SYNCH (MS)
>6 = X.21 UDLC (MS)
>TRANSMIT TO CONTINUE
>7 = HIGH SPEED SYNCH
>8 = HIGH SPEED UDLC
>9 = DCSS (UDLC)
>10 = TWISTED PAIR
>11 = 4X1 UNISCOPE
>12 = 4X1 UDLC
>13 = 4X1 N/ASYNCH
>[]
```

NOTES

LS = low speed, MS = medium speed. Multilayer printed circuit board (MLPC-2825982), medium speed, does not support X.21 types of microcode.

Do not select 1, 3, or 4 to test 4X1 UNISCOPE, 4X1 UDLC, 4X1 N/ASYNCH, or 4X1 ASYNCH.

2. Enter the selection number for the microcode type and press the TRANSMIT key. The next display shows the microcode type selected and requests the loopback mode:

```
MICROCODE TYPE BEING TESTED - XX

>CHOOSE LOOPBACK MODE
>1 = INTERNAL LOOPBACK
>2 = EXTERNAL LOOPBACK
>DEFAULT = 1
>[]
```

NOTES

EXTERNAL LOOPBACK mode cannot be selected for microcode types in items 4 through 6 and 9 through 13.

The external loopback function requires the loopback PCA (2818953), which plugs directly into the cable connector (J4) of the Medium Speed Loadable Line Module or into any DCM/modem with a loopback test switch. Refer to Figure 4-1 for the cable ID strapping and the test selection strapping of the loopback PCA.

3. Select the loopback mode. If external loopback is chosen, each line module tested requires connection to a loopback PCA.

```
>ENTER THE NUMBER OF CYCLES EACH TEST IS TO BE EXECUTED
>(0 = FFFF, or I (= INFINITE), D = 1)
>[]
```

4. Enter the number of times the test will execute.

5. The next parameter request depends on the type of testing selected from the initial menu.

   a. If item 2, TEST SINGLE PORT, was selected, the screen displays the request:

```
>ENTER PORT NUMBER (IN HEX)
>[]
```

After the port number is entered for the BASIC ASYNCH test the following is displayed:

```
>1 - STOP BITS
>2 - 1.5 STOP BITS
>3 - 2 STOP BITS
>[]
```

The selected stop bit is placed at the end of every character.

b. If item 3, TEST ALL PORTS ON A SINGLE IOP, was selected, the screen displays the request:

```
>ENTER IOP NUMBER ( HEX )
>[]
```

c. If item 4, TEST MULTIPLE PORTS (UP TO 16), was selected, the screen displays the request:

```
>ENTER UP TO 16 PORT NUMBERS
>(SEPARATED BY A COMMA, TERMINATED BY TRANSMIT)
>(ENTRIES ARE ASSUMMED TO BE HEXADECIMAL
>DO NOT PREFACE AN ENTRY WITH X OR ANY OTHER CHARACTER)
>[]
```

When all of the parameters are entered, the console displays the following message:

```
HIGHEST IOP NUMBER IN WHICH L.M.S ARE BEING TESTED - XXXX
LOADING MICROCODE AND INITIALIZING PPS
```

If no errors occur during the load and initialization sequence, the diagnostic executes the selected test. The cycle counter display, >CYCLES = XXXX, is updated at the end of each pass through the test. When the test is finished, the console displays a test complete message: TEST COMPLETE.

The following message is displayed at test completion or when an error occurs:

```
>NEXT OPERATION?
>1 (CONTINUE), 2 (REPEAT), 3 (START), 4 (EXIT)
>[]
```

where:

```
1 = At test completion, returns to test selection
  = After an error, continues where the error occurred
2 = Repeats the current test (if possible)
3 = Returns to the start of the diagnostic test
4 = Exits the diagnostic and returns to the executive
```

SW1
CABLE ID STRAPPING

1	2	3	4	5	6	Cable
X	X	1	1	1	1	RS-449 (ID = 0)
X	X	1	1	1	0	X.21 (ID = 1)
X	X	1	1	0	1	X.20 (ID = 2)
X	X	1	1	0	0	TREND (ID = 3)
X	X	1	0	0	0	RS-232 (ID = 7)
X	X	0	1	0	0	TWX (ID = 8)
X	X	0	0	0	0	None (ID = F)

TEST STRAPPING

Test Selections	SW2 1	2	3	4	5	6	7	8	SW1 1	2	3	4	5	6
RS-449 PCAs	0	1	1	1	1	1	1	1	X	X	0	0	0	0
RS-232/RS-423* PCAs	0	1	1	1	0	1	0	1	X	X	1	0	0	0
RS-232 PCAs	1	0	0	0	0	0	0	0	X	X	X	X	X	X

0 = OFF
1 = ON
X = EITHER

*RS-423 Drivers and Receivers

Figure 4-1. Cable ID and Test Selection Strapping for External Loopback PCA

4.3. Error Reporting

The console reports all of the errors with a statement of the error. If input or output status is pertinent to error isolation, then it is reported as follows:

```
INPUT STATUS = XXXX
OUTPUT STATUS = XXXX
```

Paragraph 4.4. defines the meaning of the status bits. (The lower half of the 32-bit word is reported.)

The error messages reported during test parameterization are summarized as follows:

INVALID INPUT, PLEASE TRY AGAIN

Invalid entry. Re-enter the parameter.

INCORRECT LINE MODULE I.D. FOR MULTILINE TEST

Invalid entry. Re-enter correct LMID for selected test.

MULTILINE L.M. NOT INITIALIZED FOR LOOPBACK

Select one of the loopback options and try again.

INVALID LINE MODULE I.D. FOR THIS PROTOCOL

Microcode type selected does not support line module in selected port. Re-enter port number.

USE OF THE CONSOLE PORT IS INVALID.

The selected port is the console port. Re-enter another value.

USE OF THE LOADER PORT IS ILLEGAL

The selected port is the integrated diskette port. Re-enter another value.

MICROCODE CANNOT BE LOADED INTO THE LINE MODULE

The PP chain responsible for loading the line module did not complete. Change the line module ID and try again.

The list that follows summarizes the test error messages. Refer to Appendix A for the trouble isolation procedure associated with the error.

NOTE

The error messages are preceded by information identifying the line modules being tested and the line module hardware IDs. Also, if appropriate, the PP status bytes are displayed.

Error Message Description	Isolation Procedure
CHARACTER DETECT TABLE TEST DID NOT COMPLETE Time-out occurred because character detect test did not complete.	00028
COULD NOT LOAD CHARACTER DETECT TABLE The PP chain which loads the character detect tables into the line module failed.	00028
A DATA COMPARE ERROR OCCURRED EXPECTED DATA = XXXX RECEIVED DATA = YYYY CHARACTER NUMBER = ZZZZ A difference was found during the comparison of the information in the data buffers. The character number indicates the position of the character in the buffer.	00028
PP NOT EXECUTING CORRECTLY. The PP is not setting the flags.	00028
PP DID NOT COMPLETE PP completion flags did not set.	00028
DATA COMPARE ERROR IN LOOPBACK A difference was found during the comparison of the expected and received data.	00028
TIMEOUT WITHOUT LOOPBACK COMPLETION The SDT did not complete.	00028

4.4. Input and Output Status Reporting

Error status is reported through the input and output SDT instructions, bits 16 (MSB) through 31 (LSB). If bits are reported that are not defined in the following lists, they are not errors.

Asynchronous SDT Output Status

Bit	Status	Description
20	Response Timer	Set if output response timer expires.
21	Message Timer	Set if output message timer expires.
22	DSR Off	Set any time DSR turns off with DTR on.
26	Asynch Status	Set if a break character (all zeroes with no stop bit) is detected, or when a space to mark transition is detected following a break character.
27	Monitor 1	Set if a Monitor 1 character, as defined in the character detect table, is detected in the output data stream. (Should not occur. No Monitor 1 character is defined in the character detect table used for this test.)
28	Monitor 2	Set if a Monitor 2 character, as defined in the character detect table, is detected in the output data stream. (Should not occur. No Monitor 2 character is defined in the character detect table used for this test.)
31	Status Branch	The CLC sets this bit if a status bit is set and its corresponding chain flag is clear. (This status bit should never be seen because the test sets all chain flags so that they can be reported.)

Asynchronous SDT Input Status

Bit	Status	Description
16	No Buffer	Set by the CLC when allocating input space and the zeroed buffer pool is empty.
17	Input Limit	Set by the CLC when the input limit is reached and the input chain flag 17 is set.
20	Response Timer	Set if the input response timer expires.
21	Message Timer	Set if the input message timer expires.
22	DSR off	Set any time DSR turns off with DTR on.
23	Message Error	Set if VRC/LRC, stop bit, or ADRD error is detected.
24	Carrier Off	Set if carrier went off during message reception.
25	Overrun	Set if overrun occurs. Indicates the CLC was unable to keep up with the required input message data rate.
26	Asynch Status	Set if a break character (all zeroes with no stop bit) is detected, or when a space to mark transition is detected following a break character. The break character is reported only once per long spacing signal.
27	Monitor 1	Set if a Monitor 1 character, as defined in the character detect table, is detected in the input message. (Should not occur. No Monitor 1 character is defined in the character detect table used in this test.)
28	Monitor 2	Set if a Monitor 2 character, as defined in the character detect table, is detected in the input message. (Should not occur. No Monitor 2 character is defined in the character detect table used in this test.)
31	Status Branch	The CLC sets this bit if a status bit is set and its corresponding chain flag is clear. (This bit should never be reported since the test sets all chain flags so that all of them can be reported.)

Synchronous SDT Output Status

Bit	Status	Description
20	Response Timer	Set if output response timer expires.
21	Message Timer	Set if output message timer expires.
22	DSR Off	Set any time DSR switches off with DTR on.
27	Monitor 1	Set if a Monitor 1 character, as defined in the character detect table, is detected. (Should not occur. No Monitor 1 character is defined in the character detect table used in this test.)
28	Monitor 2	Set if a Monitor 2 character, as defined in the character detect table, is detected. (Should not occur. No Monitor 2 character is defined in the character detect table used in this test.)
31	Status Branch	The CLC sets this bit if a status bit is set and its corresponding chain flag is clear. (This bit should never be reported because the test sets all chain flags so that all of them can be reported separately.)

Synchronous SDT Input Status

Bit	Status	Description
16	No Buffer	Set by the CLC when allocating input space and the zeroed buffer pool is empty.
17	Input Limit	Set by the CLC when the input limit is reached and chain flag 17 is set. The line module does not set this bit.
20	Response Timer	Set if the input response timer expired.
21	Message Timer	Set if the input message timer expired.
22	DSR Off	Set any time DSR switches off with DTR on.
23	Message Error	Set if a VRC or LRC error is detected.
24	Carrier Off	Set if carrier went off during message reception.
25	Data Overrun	Set if overrun occurs. Indicates the CLC was unable to keep up with the required input message data rate.
27	Monitor 1	Set if a Monitor 1 character, as defined in the character detect table, is detected in the input message. (This bit should not be set because the character detect table used in this test does not define a Monitor 1 character.)
28	Monitor 2	Set if a Monitor 2 character, as defined in the character detect table, is detected in the input message. (This bit should not be set because the character detect table used in this test does not define a Monitor 2 character.)
31	Status Branch	The CLC sets this bit if a status bit is set and its corresponding chain flag is not set. (This bit should not be set because the test sets all chain flags so that all of them are reported separately.)

UDLC Input SDT Status

Bit	Status	Description
16	No Buffer	Set by the CLC when allocating input space and the zeroed buffer pool is empty.
17	Input Limit	Set by the CLC when the input limit is reached and input chain flag 17 is set.
20	Response Timer	Set if the input response timer expired.
21	Message Timer	Set if the input message timer expired.
22	DSR Off	Set any time DSR switches off with DTR on.
23	FCS Error	Set if frame check error occurs. This status can be generated only at the end of the message and, therefore, is not really a termination condition.
24	Carrier Off	Set if carrier went off during message. This is of interest only during message reception.
25	Overrun	Set if overrun occurs. Indicates the CLC is unable to keep up with the required input message data rate.
27	Abort	Set if the input message is aborted. (Should not occur during this test.)
28	Idle	Set if the input line is in the idle state. (This bit should not be reported because the diagnostic test ignores this status.)
31	Status Branch	The CLC sets this bit if a status bit is set and its corresponding chain flag is clear. (This bit should not be reported because the test sets all chain flags so that each may be reported separately.)

UDLC Output SDT Status

Bit	Status	Description
20	Response Timer	Set if the output response timer expires.
21	Message Timer	Set if the output message timer expires.
22	DSR Off	Set any time DSR switches off with DTR on.
25	Underrun	Set if underrun occurs. Indicates the CLC was unable to keep up with the data rate required.
31	Status Branch	The CLC sets this bit if a status bit is set and its corresponding chain flag is clear. (This bit should not be set because the test sets all chain flags so that each may be reported separately.)

Multiline Asynchronous Output SDT Status

Bit	Status	Description
20	Response Timer	Set if the output response timer expires.
25	Buffer Error	Set if the output message contains more than 255 bytes or if an output SDT is issued to an asynchronous line that has not completed transmission of the previous output buffer. In the latter case, the transmission already in progress is continued and the new SDT is ignored.
31	Status Branch	The CLC sets this bit if a status bit is set and its corresponding chain flag is clear. This action occurs only after the output status has been passed to the CLC. (This bit should not be reported because the test sets all chain flags so that each may be reported separately.)

Multiline Asynchronous Input SDT Status

Bit	Status	Description
16	No Buffer	Set by the CLC when allocating input space and the zeroed buffer pool is empty. Any data remaining in the line module input block when this condition occurs is lost and input continues with the next input block.
17	Input Limit	Set by the CLC when the input limit is reached; causes unconditional termination of the burst transfer and loss of any data remaining in the line module input block.
20	Response Timer	Set if the input response timer expires.
21	Message Timer	Set if the input message timer expires.
22	DSR Off	Set any time DSR switches off with DTR on.
23	Message Error	Set if a VRC, stop bit, or ADRD error is detected.
24	Carrier Off	Set if carrier went off during message reception.
25	Data Overrun	Set if the input buffer is overrun, indicating the input block(s) exceeded the available buffer space on the line module and data was lost.
26	Asynch Status	Set if a break character (all zeroes with no stop bit) is detected, or when a space to mark transition is detected following a break character.
30	End Of Block	Set if the input block was terminated because the maximum number of characters allowed was reached before an EOM was detected or the message timer expired.
31	Status Branch	The CLC sets this bit if a status bit is set and its corresponding chain flag is clear. The line module does not set this bit. (This bit should not be reported because the test sets all chain flags so that each is set separately.)

X.21 Synchronous and UDLC SDT Status

Refer to either the synchronous status or UDLC status for the meaning of the status bits reported by these tests.

DCSS (UDLC) Output Status

Bit	Status	Description
20	Response Timer	Set if output response timer expires.
21	Message Timer	Set if output message timer expires.
23	Over-Current	Set if transmitter over-current condition is detected. Indicates that a transmission was attempted at the same time that the DCSS was transmitting.
25	Underrun	Set if underrun occurs. Indicates the CLC is unable to keep up with the data rate required.
31	Status Branch	The CLC sets this bit if a status bit is set and its corresponding chain flag is clear. (This status bit should never be seen because the test sets all chain flags so that they can be reported.)

DCSS (UDLC) Input Status

Bit	Status	Description
16	No Buffer	Set by CLC when allocating input space and the zeroed buffer pool is empty.
17	Input Limit	Set by CLC when the input limit is reached and input chain flag 17 is set.
20	Response Timer	Set if input response timer expires.
21	Message Timer	Set if message timer expires.
23	FCS Error	Set if frame check error occurs.
25	Overrun	Set if overrun occurs. Indicates that the CLC cannot keep up with the required input message data rate.
27	Abort	Set if the input message is aborted.
31	Status Branch	The CLC sets this bit if a status bit is set and its corresponding chain flag is clear. (This status bit should never be seen because the test sets all chain flags so that they can be reported.)

5. PARALLEL LINE MODULE DIAGNOSTIC TEST

5.1. Introduction

The parallel line module diagnostic test checks the C and B PCAs that provide the interface for the DCP to a parallel console, cartridge disk, magnetic tape, or Series 1100 host. The test runs in internal, loopback, or host mode. This section also provides a brief description of the Series 1100 Peripheral Test Sequencer (PTS).

Note that the DCP/10/10A/15 do not support 16-bit parallel line modules.

5.2. Test Procedure

When the parallel line module test is selected, the console displays a series of prompts which set the configuration and execution parameters of the test. Enter all data in hexadecimal.

```
CPA FAMILY DIAGNOSTIC ROUTINES  RELEASE - R5.1
PARALLEL LINE MODULE TEST

>INTERNAL, LOOPBACK OR HOST (0=INT,1=LOOP,2=HOST, D=0)
>[]
```

1. Select the type of test:

   0 = Internal test (peripheral mode) checks out the drivers of the PCA. No cables are required.

   1 = Loopback test (intercomputer mode) checks out the drivers of PCA. (For pre-serial split, also checks cables from the drivers.) The test requires loopback cables connected at the bulkhead of the DCP or 1100 cables connected together at the host side, loopback test modules (P/N 2818884) connected to the backplane of the B PCA, and strapping of the C PCA for loopback mode.

   2 = Host test (host mode) checks that the normal operating configuration functions across the channels. The test requires cables connecting the 1100 host and the Peripheral Test Sequencer (PTS) within the host, and strapping of the C PCA for loopback mode.

CAUTION

Ensure that input power is OFF before checking or changing switch settings on the C PCA.

NOTE

The loopback cable must not be connected to the bulkhead channel which forms a channel pair with the console channel. For example, if the console is on channel B, the loopback cannot be on channel A.

2. Set the DIP switches on the C PCA for the hardware mode of operation. The only DIP switch settings that affect the operation of the test are switches 1, 6, and 7. Switches 6 and 7 cannot both be in the ON position. The other switch positions (2, 3, 4, and 5) must be in the OFF position. Switch 1 controls the parity option.

Peripheral =	Set all DIP switches to OFF.
Host =	Set switch 6 to OFF and switch 7 to ON. Set switch 1 to ON for parity checking.
Intercomputer =	Set switch 6 to ON and switch 7 to OFF. Set switch 1 to ON for parity checking.

```
>16 BIT OR 32 BIT(0=16,1=32, D=0)
>[]
```

3. Select the number of bits that will be transferred.

```
>ENTER DESIRED PORT(0-FF, D=0)
>[]
```

4. Enter the number of the port where the C PCA is installed. Only one parallel interface is tested at one time.

   Once the port number is specified, the software reads the hardware ID of the operating mode that was set by the DIP switches, and one of the following messages is displayed:

```
ID=X10 - PERIPHERAL MODE
ID=X11 - HOST MODE
ID=X12 - INTERCOMPUTER OR EXTERNAL LOOPBACK MODE
```

```
>NUMBER OF CYCLES (0=INDEFINITE,0-FFFF,D=FF)
>[]
```

5. Select the number of test cycles. Each cycle consists of from one to six data patterns that are sent or received.

   During the test, the console displays the port number, the hardware ID, and the number of cycles to complete on fixed line 2:

   ```
   PORT: 0006        ID: 0010      CYCLES TO COMPLETE:  00FF
   ```

```
>STOP ON ERROR, (0=NO,1=YES,D=1)
>[]
```

6. Use stop-on-error options to continue the test even though errors are detected or to stop the test when an error occurs.

```
>NUMBER OF FIXED PATTERNS (1-4,D=4)
>[]
```

7. Select the number of fixed patterns that are sent and/or received over the port.

```
>ENTER PATTERN (0=FFFF,D=FFFF)
>[]
```

8. Following the number-of-fixed-pattern parameter the console requests a hexadecimal pattern of four digits for the fixed patterns that were selected. Enter one of following values: FFFF, AAAA, 5555, and 0000.

```
>USE RIPPLE PATTERN (0=NO,1=YES,D=1)
>[]
```

9. Enter 1 to select two pre-defined patterns (ripple pattern): all bits set but one, or all bits off but one. These patterns are shifted left one position for every two 16-bit words, producing the following display:

   ```
   FFFE FFFE FFFD FFFD FFFB FFFB FFF7 FFF7.....
   0001 0001 0002 0002 0004 0004 0008 0008 ....
   ```

   The total number of test patterns is the sum of the ripple patterns and the fixed patterns. The total must be greater than zero and cannot exceed six.

```
>BUFFER SIZE, (0=SMALL,1=LARGE,D=1)
>[]
```

10. Select the buffer size according to the system configuration. Two sizes are allowed. The small buffer is sixty-four DCP 16-bit words (thirty-two 1100 words with the host option). The large buffer is two thousand DCP 16-bit words (one thousand 1100 words with the host option).

11. The following request appears only when the host option is used with the PTS software program (see paragraph 5.5):

```
>RUN OPTION (0=OUTPUT,1=INPUT,2=BOTH, D=2)
>[]
```

This parameter defines either simplex (input or output only) operation or full-duplex operation of the diagnostic with the host software program.

5.3. Test Execution

When all of the test parameters are entered successfully, the console displays them. A sample of a successful execution of the parameters follows.

```
            CPA FAMILY DIAGNOSTIC ROUTINES  R5.1
                  PARALLEL LINE MODULE TEST
PORT:  0006  ID:  0010 CYCLES TO COMPLETE:  00FF        16 BIT
PERIPHERAL   INTERNAL  FULL DUPLEX   COMPLETE
*IN 0000 005FA OUT 0000 005FA INCYC 00FF OUTCYC 00FF ERR 0000

INTERNAL, LOOPBACK OR HOST (0=INT, 1=LOOP, 2=HOST, D=X0)  >
ENTER DESIRED PORT(0 - FFF, D=0)  >
   ID = 10 - 16 BIT PERIPHERAL
NUMBER OF CYCLES, 0=INDEFINITE (0-FFFF, D=FF)  >
STOP ON ERROR, (0=NO, 1=YES, D=1)  >
NUMBER OF FIXED PATTERNS (0-4, D=4)  >
ENTER PATTERN (0-FFF, D=FFFF)  >
ENTER PATTERN (0-FFF, D=AAAA)  >
ENTER PATTERN (0-FFF, D=5555)  >
ENTER PATTERN (0-FFF, D=0000)  >
USE RIPPLE PATTERN, 0=NO, 1=YES  >
BUFFER SIZE, (0=SMALL, 1=LARGE, D=1)  >
  1ST INPUT COMPLETE  EI:  X     *FFFF
  1ST 8 DCP I/P WORDS (HEX):
  >0000 07D0 FFFF .... FFFF
  1ST OUTPUT COMPLETE *
INTERNAL, LOOPBACK OR HOST (0=INT,1=LOOP,2=HOST, D=0)
```

The message in fixed line 3 of the display reports the type of test that is executing and in this sample, that the test is completed.

The message in fixed line 4 reports the input/output (IN/OUT) transfer counts, the input/output cycle (INCYC/OUTCYC) counts, and the error (ERR) count. In this sample, a non-zero cycle count was specified and that value was reached.

In the lines following the parameters, the console displays the successful completion of the input and output parameters. The input complete message is:

```
1ST INPUT COMPLETE.  EI:  FFFF *
1ST  8  DCP WORDS (HEX):  0000 07D0 FFFF FFFF FFFF FFFF FFFF
                          FFFF
```

The sample shows that the first input buffer was received. The first two buffer words are the word count (words 0 and 1). The received external interrupt (EI) is a copy of the third word of the buffer (word 2). This example assumes a default value of FFFF.

The following message indicates that the first output buffer was sent:

```
* 1ST OUTPUT COMPLETE *
```

Internal loopback does not update cycle counter on every pass, only at the end of the test.

5.4. Error Reporting

When a fatal error occurs, the console reports error messages and error codes. The error messages are:

ILLEGAL DIGIT RETRY

A hexadecimal value must be entered.

LINE MODULE ID IS INVALID

The LMID for the selected test is incorrect. The C PCA strapping determines the ID.

FATAL ERROR XXXX

The error codes and their meanings are given in the list that follows.

Following the error message and/or code, the screen displays the prompt:

```
>ENTER 1(CONTINUE), 2(REPEAT), 3(START), 4(EXIT)
>[]
```

NOTE

If a PP state item occurs, the port must be reinitialized. Enter 3 (START).

At this point you may want to view the actual input and output buffers to diagnose a bad pin on the backplane or a broken wire. To access the buffers, refer to paragraph 5.4.1, following the error code descriptions, for instructions.

The following list provides the error codes and their meanings. Refer to Appendix A for the trouble isolation procedure associated with the error.

Error Code	Description	Isolation Procedure
000A	The PP did not initialize.	00016
0001	Time-out waiting for the STB to complete.	00016
0003	I/P parity error: A parity error was detected on input.	00017
0004	Overflow word has been destroyed: Input is initiated with a buffer that allows one more word than the number that are sent by the output chain. The overflow word is set to a pre-defined value of XBAD1. If the content of this word changes, too much data was received. The overflow condition is not checked during internal testing.	00017
0005	I/P EI data is incorrect: The input external interrupt (EI) is a copy of the third word of the output buffer (word 2, counting from 0). The expected value for the first data transfer is XFFFF if the default is selected. Location X7012 and X7802 should contain the same values. X7012 contains the received EI value. X7802 contains the third word of the input buffer. (Paragraph 5.4.1 provides instructions for viewing buffers.)	00017
0006	First two I/P words incorrect: The first word of the input buffer must be X0000. The second word is the buffer size as seen from the DCP. This value is X0040 (decimal 64) for the small buffer and X07D0 (decimal 1000) for the large buffer	00017
0007	I/P data is incorrect: The remainder of the input buffer, excluding the first two words, was compared to the expected pattern and the data does not match.	00017
0008	I/P time-out with test in progress: See 0009.	00017
0009	O/P time-out with test in progress: Both input and output are timed by hardware response timers. If the timer expires after the first data is sent, a time-out with test in progress occurs. If the PTS software cycle is running, check the counts in both programs. The response timers are set to 2000 milliseconds (two seconds) for both input and output.	00017

5.4.1. Instructions for Viewing Buffers

1. Access the resident utilities using the F1 menu. The following prompt scrolls onto the screen:

```
>1 - CONTINUE THE TEST
>2 - ABORT CURRENT ACTIVITY AND REINITIALIZE THE EXECUTIVE
>3 - HOLD CURRENT ACTIVITY AND USE THE UTILITIES
>ENTER OPTION
>[]
```

2. Select option 3. The following prompt is displayed:

```
>RESIDENT UTILITIES - ENTER COMMAND
```

3. To view the contents of the input buffer, enter these commands:

```
>sec800 p <transmit>    (where:  se = segment command
                                 c800 = SDR25, input buffer
                                 p= process mode)

>dv0 8 <transmit>       (where:  dv = display virtual memory
                                 0 = from address 0
                                 8 = eight lines of data)
```

4. To view the content of the output buffer, enter these commands:

```
>sed000 p <transmit>    (where:  se = segment command,
                                 d000 = SDR26; output buffer
                                 p = process mode)

>dv0 8 <transmit>       (where:  dv = display virtual memory,
                                  0 = from address 0
                                  8 = eight lines of data
```

The buffer content scrolls onto the screen in this format:

```
   SSN=0001     SEG=FF03C21F
A000   0000  07D0  0001  0001  0002  0002  0004  0004  ................
A008   0008  0008  0010  0010  0020  0020  0040  0040  ..............@.@
A010   0080  0080  0100  0100  0200  0200  0400  0400  ................
A018   0800  0800  1000  1000  2000  2000  4000  4000  ..............@.@.
A020   8000  8000  0001  0001  0002  0002  0004  0004  ................
A028   0008  0008  0010  0010  0020  0020  0040  0040  ..........  @.@
A038   0800  0800  1000  1000  2000  2000  4000  4000  ..............@.@.
A040   8000  8000  0001  0001  0002  0002  0004  0004  ................
RESIDENT UTILITIES - ENTER COMMAND
>[]
```

5. To view the content of the External Interrupt (EI) word in the the PP code, enter these commands:

```
>sec000 p <transmit>    (where:  se = segment command
                                 c000 = SDR24; PP code
                                 p= process mode)

>dv12 1 <transmit>      (where:  dv = display virtual memory
                                 12 = from address 12
                                 1 = one line of data)
```

6. To exit the RESIDENT UTILITIES, enter the command:

```
>ex  <transmit>
```

5.5. Series 1100 Peripheral Test Sequencer (PTS)

The Series 1100 Peripheral Test Sequencer (PTS) resides in the 1100 computer. The PTS enables the transfer of data to and from the DCP over the ISI word channels connected between the 1100 and DCP.

The following paragraphs contain definitions, procedures, and operating instructions for the PTS test. For more detailed information on PTS, refer to DA-3076, SPERRY Series 1100 Systems, Peripheral Test Sequencer (PTS) Test Description; DA-3077, SPERRY Series 1100 Systems, Peripheral Test Sequencer (PTS) Offline Operator's Reference; and DA-3078, SPERRY Series 1100 Systems, Peripheral Test Sequencer (PTS) Online Operator's Reference.

NOTE

Use PTS/CEMAX (level 17R1T2 or later revision) software with the parallel line module test.

5.5.1. PTS Data Test Description

The purpose of the routine is to detect data transfer errors to and from a front-end processor and provide information for error isolation. Isolation indicates what data bits of the channel or what function of the channel is in error. Further hardware isolation is then obtained by offline microdiagnostics or macrodiagnostics.

The PTS software allows the user to describe the data pattern(s) that are sent to the 1100 from the front-end processor and provides input- or output-only options.

5.5.2. Test Procedure

Perform the local storage test and the parallel line module test before running the PTS. PTS solicits only numeric input. Range and default values are provided for any request. For example, the request HOW MANY FIXED PATTERNS? 0-4 (4) indicates a range of 0 to 4 with a default of 4. Inputs start with an X for hexadecimal numbers, an 0 for octal numbers, and any legal decimal digit for decimal number input. Therefore, XF, 017, and 15 are hexadecimal, octal, and decimal equivalents.

1. Load the PTS software in the processor.
2. Enter the parameters that were defined for the parallel line module test to ensure that the sending and receiving software uses the same cycles and data patterns.

5.5.3. Test Execution

If input is requested, PTS begins by opening for input. If no input is received within the allocated time, a time-out message is displayed, followed by a message that the system is ready to receive input. This procedure continues until the first data transfer occurs with its associated interrupt (EI). At that point, the routine checks 1100 status, EI data, non-significant bits (bits 35, 26, 17, and 5 from left to right, and numbering from 35 to 0 in the 1110 word), word 1 and data words 2 to N. The next expected pattern is processed in the same manner until the specified cycle count is reached.

The fixed patterns are the given values repeated for the entire buffer using the 16-bit or two-byte pattern for each half of the 1100 word. The ripple pattern uses a one-bit-on pattern for every two 16-bit words. Each subsequent pair of 16-bit words has the same pattern shifted circularly to the left. The second ripple pattern uses a one-bit-off pattern shifted in the same manner.

5.5.4. Output Messages

The output messages are summarized as follows:

```
TOTAL PATTERNS (D):  6  TOTAL CYCLES (D):  1
```

This message is displayed before any data transfer occurs. It indicates the number of patterns and cycles in decimal. When this message ends, PTS opens for input or starts output as a function or I/O control option.

```
FIXED PATTERN(S) USED:
FFFF FFFF AAAA AAAA 5555 5555 0000 0000
```

The four fixed patterns are four 1100 word patterns.

```
RIPPLE PATTERNS USED:
0001 0001 FFFE FFFE
```

The ripple patterns are two 1100 word patterns.

Error output messages provide numeric output in hexadecimal (HEX), decimal (D), or octal (OCTAL) notation. When a data buffer is printed in hexadecimal, it contains eight 1100 words per line.

Figure 5-1 shows a sample output from the O, P, D, and L options.

NOTE

When the L option is used, thirty-three 1100 words are printed. The extra word is the overflow word which is always X89AB CDEF. Also, each line contains eight 1100 words composed of eight hexadecimal characters which create a 36-bit 1100 word. The final summary information displays input, output, and cycle count in hexadecimal.

```
*  OUTPUT  *
0000 0040 FFFF FFFF  ...  FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF  ...  FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF  ...  FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF  ...  FFFF FFFF FFFF FFFF FFFF FFFF
89AB CDEF
*  OUTPUT EF  *
0000 FFFF

*  OUTPUT  *
0000 0040 AAAA AAAA  ...  AAAA AAAA AAAA AAAA AAAA AAAA
AAAA AAAA AAAA AAAA  ...  AAAA AAAA AAAA AAAA AAAA AAAA
AAAA AAAA AAAA AAAA  ...  AAAA AAAA AAAA AAAA AAAA AAAA
AAAA AAAA AAAA AAAA  ...  AAAA AAAA AAAA AAAA AAAA AAAA
89AB CDEF
*  OUTPUT EF  *
0000 AAAA

*  OUTPUT *
0000 0040 5555 5555  ...  5555 5555 5555 5555 5555 5555
5555 5555 5555 5555  ...  5555 5555 5555 5555 5555 5555
5555 5555 5555 5555  ...  5555 5555 5555 5555 5555 5555
5555 5555 5555 5555  ...  5555 5555 5555 5555 5555 5555
89AB CDEF
*  OUTPUT EF  *
0000 5555

*  OUTPUT  *
0000 0040 0000 0000  ...  0000 0000 0000 0000 0000 0000
0000 0000 0000 0000  ...  0000 0000 0000 0000 0000 0000
0000 0000 0000 0000  ...  0000 0000 0000 0000 0000 0000
0000 0000 0000 0000  ...  0000 0000 0000 0000 0000 0000
89AB CDEF
*  OUTPUT EF  *
0000 0000
```

Figure 5-1. Sample Output of O, P, D, and L Options (Sheet 1 of 2)

```
*  OUTPUT  *
0000 0040 FFFE FFFE  ...  FFEF FFEF FFDF FFDF FFBF FFBF
FF7F FF7F FEFF FEFF  ...  EFFF EFFF DFFF DFFF BFFF BFFF
7FFF 7FFF FFFE FFFE  ...  FFEF FFEF FFDF FFDF FFBF FFBF
FF7F FF7F FEFF FEFF  ...  EFFF EFFF DFFF DFFF BFFF BFFF
89AB CDEF
*  OUTPUT EF  *
0000 FFFE

*  OUTPUT  *
0000 0040 0001 0001  ...  0010 0010 0020 0020 0040 0040
0080 0080 0100 0100  ...  1000 1000 2000 2000 4000 4000
8000 8000 0001 0001  ...  0010 0010 0020 0020 0040 0040
0080 0080 0100 0100  ...  1000 1000 2000 2000 4000 4000
89AB CDEF
*  OUTPUT EF  *
0000 0001

*  INPUT - OUTPUT - CYCLE COUNT (HEX):  *
0000 0000 0000 0006 0000 00001
 DATA ERROR(S) (D):  0
```

Figure 5-1. Sample Output of O, P, D, and L Options (Sheet 2 of 2)

6. TWISTED PAIR LINE MODULE DIAGNOSTIC TEST

6.1. Introduction

The twisted pair line module diagnostic test checks and verifies the data sent through the signal distribution module (SDM) between the twisted pair line module (TPLM) and the terminals. A maximum of 24 UTS 30T terminals can be tested.

The test verifies line module functionality and also determines whether or not the SDM is communicating with the terminals; however, it does not isolate a failing SDM or terminal.

6.2. Test Procedure

When the twisted pair test is selected from the system menu, the console displays a series of prompts which request the configuration and execution parameters of the test.

```
CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE R5.1
        TWISTED PAIR TERMINAL TEST
  MICROCODE TYPE BEING TESTED--TWISTED PAIR


>LOADING TEST LOADER PORT PROCESSOR CODE
>LOADING TEST MESSAGE FILE
>ENTER THE NUMBER OF CYCLES EACH TEST IS TO BE EXECUTED
>(0-FFFF, or I(=Infinite),D=1)
>[]
```

1. Enter the number of times the test will execute.

NOTE

If infinite cycling is selected, the test can be terminated by pressing the FUNCTION/F1 keys.

```
>ENTER PORT NUMBER IN HEX
>[]
```

2. Enter the port number of the TPLM and press the TRANSMIT key. The program tests the line module ID for that port. If the TPLM is in the designated port and will initialize, the screen displays the line module port number and the microcode ID, followed by two configuration options:

```
LINE MODULE NUMBER - XXXX
LINE MODULE ID-0065


>LOOPBACK TEST
>LOOPBACK TEST COMPLETED
>DO YOU WISH TO SPECIFY TERMINAL IDS? (1=YES, 0=NO), D=YES
>[]
```

3. Enter 1 to select specific terminals for test. Enter 0 to configure all terminals.

   a. If 1 is entered, the next prompt is:

```
>ENTER UP TO 24 TERMINAL IDS (00-FF)--ID,ID
>[]
```

      (1) Enter the two-digit terminal link address(es). The following information appears on fixed line 6 and fixed line 7:

```
TERMINAL ID(S) CONFIGURED
xx, xx, xx,
```

      where: xx = terminal line address(es) selected.

   b. If 0 is selected, the console displays the message, AUTO CONFIGURATION IN PROGRESS. When the function is completed, the message, AUTO CONFIGURATION COMPLETE, is displayed and fixed line 8 contains the information:

```
AUTO CONFIGURATION
xx, xx, xx....
```

   where: xx = terminal link addresses identified by test.

NOTE

If no terminal link addresses are displayed, either the test found no terminals connected to the interface or the communications lines have bad connections. The test completes without errors because nothing was found to test

4. The last configuration request is the stop-on error option. If an error occurs, the first option stops the test, the second option places the terminal in a hold state, and the third option continues the test. Press the F2 key to clear the function.

```
>1 = STOP ON ERROR
>2 = SET INACTIVE AND CONTINUE
>3 = CONTINUE ON ERROR
>[]
```

6.3. Error Reporting

If an error occurs, the console displays an error message, which includes the address of the terminal that was sending or receiving data from the TPLM. The errors fall into one of three categories: status/transfer count errors (unexpected status), data compare errors, or frame count errors. All numeric values are reported in hexadecimal.

Status/transfer count errors are displayed on the screen in the following formats:

```
OUTPUT SDT ERROR
TERMINAL ADDRESS = XX

INPUT SDT ERROR
TERMINAL ADDRESS = XX
```

Data compare errors occur when input received by the terminal is different than expected. They have the format:

```
INPUT DATA ERROR
EXPECTED BYTE = XXXX
RECEIVED BYTE = XXXX
TERMINAL ADDRESS = XX
```

The format of frame count errors is:

```
FRAME COUNT ERROR
FRAME TERMINAL DID NOT RECEIVE = XXXX
TERMINAL ADDRESS = XX
```

possible input/output errors messages are:

- Input error messages
  - NO BUFFER
  - INPUT LIMIT
  - RESPONSE TIMER TIME-OUT
  - MESSAGE TIMER TIME-OUT
  - CALL CLEARED
  - FCS ERROR
  - OVERRUN
  - ABORT
  - STATUS BRANCH

- Output error messages
  - RESPONSE TIMER TIME-OUT
  - MESSAGE TIMER TIME-OUT
  - CALL CLEARED
  - UNDERRUN
  - CHECK STATE
  - STATUS BRANCH

7. CARTRIDGE DISK DIAGNOSTIC TEST

7.1. Introduction

This section describes the operating procedures and error indicators of the cartridge disk diagnostic test. The diagnostic test checks the functions of the SPERRY Cartridge Disk Subsytem (cartridge disk) Type 8408, specifically the C and B PCAs of the parallel line module, the cables to the cartridge disk, and the controller and disk drive in the cartridge disk.

7.2. General Information

When errors occur, the error information includes the status bits and the sense status bits returned by the disk controller. The bit numbering system for the cartridge disk status identifies bit 0 as the least significant bit (LSB); however, the display on the maintenance panel has register contents in bits 16 through 31 with bit 31 as the LSB.

Figure 7-1 relates the cartridge disk status bits to the maintenance panel bits. Figure 7-2 provides the same information for the sense status bits of the cartridge disk.

Status Bits	Description (If Set)	Maintenance Panel Bits
15	Abnormal completion	16
14	Command reject	17
13	Drive not ready	18
12	Write protect	19
11	Illegal cylinder	20
10	Format error	21
9	Unsuccessful search	22
8	Sector not found	23
7	Data error (CRC or BCA)	24
6	Write circuit malfunction	25
5	Overrun/underrun	26
4	Dropped ready	27
3	Drive number	28
2	Error recovery	29
1	Not used	30
0	Flag not zero (Illegal or defective track)	31

Figure 7-1. Cartridge Disk Status Bits

Sense Status Bits	Description (If Set)	Maintenance Panel Bits
15	Drive selected	16
14-13	Disk surfaces Upper, removable disk (0, 0) Lower, removable disk (0, 1) Upper, fixed disk (1, 0) Lower, fixed disk (1, 1)	17-18
12- 8	Sector address	19-23
7	Seek incomplete	24
6	Write protect	25
5	Cylinder overflow	26
4	Format error	27
3	Not used	28
2	Data overrun/underrun	29
1	Write circuit malfunction	30
0	Data error	31

Figure 7-2. Cartridge Disk Sense Status Bits

7.3. Test Procedure

NOTE

Perform the parallel line module micro-diagnostic and macrodiagnostic tests before running this diagnostic.

When the cartidge disk diagnostic test is selected from the system menu, the console displays a series of prompts which request the configuration and execution parameters of the test:

```
CPA FAMILY DIAGNOSTIC ROUTINES   RELEASE - R5.1
      CARTRIDGE DISK DRIVE (T-8408) TEST


>LEAVE DRIVES OPEN FOR ACCESS TO WRITE PROTECT SWITCHES
>ENTER CLC AND PORT NUMBER  (X00-XFF, OR  X0-XF      D = X00)
>[]
```

1. Enter the hexadecimal number of the parallel port to which the cartridge disk is attached or press TRANSMIT to select the default. A hexadecimal number must have a leading X. The first digit after the X is the CLC (0 - F) where the selected port resides and the second digit is the port number (0 - F).

```
>PORT XXXX LM I.D. XXXX
>[]
```

2. Enter the port number and the line module ID.

```
>ENTER THE NUMBER OF THE DRIVE TO BE TESTED OR BOTH
>(0, 1 OR B  D=0)
>[]
```

where:

0 = upper drive
1 = lower drive
B = both drives

3. Select the drive parameter. If you want to continue testing the same drive after the first selection, press TRANSMIT.

```
>ENTER THE SURFACE(S) (HEAD) NUMBER  (1, 2, 3, 4)
>[]
```

4. Enter the number or numbers of the surface (head), where:

   1 = top surface of removable disk
   2 = lower surface of removable disk
   3 = top surface of fixed disk
   4 = lower surface of fixed disk

   To continue testing the same head after the first selection, press TRANSMIT.

```
>ENTER LOOP COUNT (1-9999, X1-FFFF OR I = INFINITE  D = 1)
>[]
```

5. Select a specific loop count or the default value. Decimal values of 1 through 9999 or hexadecimal values of X1 through XFFFF can be entered. To repeat the diagnostic test for an infinite number of cycles, enter I. To repeat a previous selection, press TRANSMIT. This entry completes the parameter selections. The next display is the test list:

```
        CPA FAMILY DIAGNOSTIC ROUTINES   RELEASE  R5.1
             CARTRIDGE DISK DRIVE (T-8408) TEST


>ENTER TEST SELECTION OR TRANSMIT TO CONTINUE  (D=0)
>1 - DISK PREP ROUTINE
>2 - TEST DATA PATH
>3 - TEST MASTER CLEAR COMMAND
>4 - TEST WRITE PROTECT
>5 - TEST DRIVE, SURFACE, AND HEAD ADDRESSING
>6 - MAXIMUM SEEK TEST
>7 - WRITE/READ TEST
>[]
```

6. Enter the test selection number.

   a. In Test 1, the console displays a preparation (prep) verification prompt:

```
>PREPARE SURFACES X AND X OF DRIVE X  ( Y OR N, D=N)
>[]
```

NOTE

The disk must be prepped before executing any read/write operations.

(1) Enter Y to start the prep routine or press the TRANSMIT key to display another option.

During execution of Test 1, the console displays the drive, track, and head numbers as the routine progresses: PREP ON DRIVE: XX TRACK: XXXX HEAD: XX

b. In Test 2, the program checks the data path from the DCP to the cartridge disk by writing to and reading from the read/write RAM in the disk controller. The data patterns are: all 1's, all 0's, and then a 48-word buffer containing a section of program code. To verify a good data transfer, the received data is compared to the transmitted data.

c. In Test 3, the program checks the software master-clear command to ensure that the disk controller can be cleared. A write command is sent without data, which causes the disk controller to hang. A seek command is issued but will not execute because of the condition of the controller. A software master-clear command is issued to clear the controller, and another seek command is sent to determine if the master-clear command succeeded.

d. In Test 4, the program tests the write-protect function to ensure that each platter can be write-protected.

(1) When the following prompt appears, set the WRITE PROTECT switch for the selected platter (located inside the cartridge disk drawer) in the WRITE PROTECT position and enter the items requested:

```
>WRITE PROTECT DRIVE  X
>PLATTER  Y
>PRESS TRANSMIT WHEN READY
```

where X = Drive number 0, 1, 2, or 3
Y = Lower or upper

(2) Clear the WRITE PROTECT switch when the following prompt appears:

```
>WRITE PROTECT DRIVE  X
>PLATTER  Y
>PRESS TRANSMIT WHEN READY
```

e. In Test 5, the program checks the addressing function by writing the current drive, head, and track numbers to the selected surface and then reading and verifying the data. The console displays the drive and head numbers as the test progresses: ADDRESSING DRIVE XX HEAD XX

f. In Test 6, the read/write head transverses from minimum to maximum track and back to minimum track several times. Status is checked each time to ensure normal completion.

g. In Test 7, the write and read commands are checked and the accuracy of the data transfer is verified.

As each test is executed, the console displays the following message:

TEST XX IN PROGRESS

When the test is completed, the console displays the message:

XXXX CYCLES COMPLETED XXXX ERRORS DETECTED
TEST XX COMPLETED

Then the console displays the test menu again and another selection can be entered.

7.4. Error Reporting

The console reports all of the errors. The display includes the error code, the error type, the interrupt status bits (Figure 7-1), and the contents of the sense byte status word (Figure 7-2). Also, several error messages can be reported during initialization of the test and during the read of line module ID.

The error messages and error codes are summarized in the following list. Refer to Appendix A for the trouble isolation procedure associated with the error. Further trouble isolation information is available in MR6230, SPERRY Cartridge Disk Cabinet Type 8408-02 Troubleshooting Guide.

Error Message/Code Description	Isolation Procedure
REJECT ANSWER The channel selection was not a legal input. Re-enter a correct value.	-
PORT WILL NOT INITIALIZE The selected port is not communicating with the CLC.	00016
THE PORT IS NOT WITHIN LEGAL RANGE The selected port was less than 0 or greater than XFF (255).	00019
USE OF THE CONSOLE PORT IS INVALID The selected port is the console port.	00019
USE OF THE LOADER PORT IS INVALID The selected port is the IFDC port.	00019
THIS LM TYPE MAY NOT BE USED WITH THIS DIAG A line module with improper LMID was selected to run the test. Only a 16-bit LMID will be accepted. C PCA switches 6 and 7 must be off.	00019
THE PORT PROCESSOR CHAIN WOULD NOT EXECUTE The port processor completion flag was not set.	00016
BIT 5-I/P PARITY FROM PP (Tests 1-4, 6) Bad parity detected on input data transfer.	00018
BIT 6-O/P TIMEOUT FROM PP (Tests 1-4, 6) Write data command did not complete in specified time.	00019
BIT 7-I/P TIMEOUT FROM PP (Tests 1-4, 6) Read data command did not complete in specified time.	00020

Error Message/Code Description	Isolation Procedure
DATA PATH ERROR-DATA NOT TRANSFERRED OUTDATA XXXX INDATA NONE (Test 1) No data read on data transfer.	00020
DATA ERROR OUTDATA XXXX INDATA NONE (Test 1) Input data and output data did not compare.	00020
OUTPUT TIMEOUT DID NOT OCCUR (Test 2, 6) Disk controller did not hang on diagnostic write command.	00019
0010 (Test 0) Abnormal completion status during disk prep. R2 = controller status	00021
0011 (Test 1) No data transferred to cartridge disk RAM.	00020
0012 (Test 1) Input data and output data did not compare.	00020
0021 (Test 2) Disk controller did not hang diagnostic write command.	00019
0022 (Test 2) First seek command completed abnormally. R2 = status	00022
0023 (Test 2) Second seek command completed abnormally. Master-clear command did not clear controller.	00022
0031 (Test 3) Write protect bit was not set in status word.	00023

Error Message/Code Description	Isolation Procedure
0032 (Test 3) Data was written on disk when write protect was enabled.	00023
0033 (Test 3) Write protect was not reported in sense byte status.	00023
0041 (Test 4) Seek operation did not complete.	00022
0042 (Test 4) Write operation did not complete.	00019
0043 (Test 4) Read operation did not complete.	00020
0044 (Test 4) Addressing error was detected.	00019
0051 (Test 5) Seek did not complete to zero cylinder	00022
0052 (Test 5) Seek did not complete to maximum cylinder.	00022
0061 (Test 6) Write error: abnormal completion of cone write.	00021
0062 (Test 6) Read error: abnormal completion of cone read.	00021
0063 (Test 6) Data error: data received is incorrect. R6, R9 = expected data R2, R5 = received data	00020

Error Message/Code Description	Isolation Procedure
0064 (Test 6) Write error: abnormal completion on linear write.	00021
0065 (Test 6) Read error: abnormal completion on linear read.	00021
0066 (Test 6) Data error: data received is incorrect. R6, R9 = expected data R2, R5 = received data	00020

8. RIGID DISK SUBSYSTEM DIAGNOSTIC TEST

8.1. Introduction

The rigid disk subsystem diagnostic test checks the major functions of the SPERRY Disk Storage Subsystem Type 8409 (rigid disk) which connects to the Byte Interface Line Module (BILM), also referred to as the Bi-Directional Byte Interface (BDBI).

8.2. Test Procedure

When the rigid disk diagnostic is selected from the system menu, the console displays a series of prompts which request the configuration and execution parameters of the test.

```
CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1
        RIGID DISK DRIVE (T-8409) TEST


>ENTER PORT PROCESSOR NUMBER(HEXADECIMAL 00-FF,D=4)
>[]
```

1. Enter the port number of the BILM/BDBI and press the TRANSMIT key. The program tests the line module ID for that port. If the correct port was selected, the BILM/BDBI initializes. The screen displays the line module ID and the port number on fixed line four:

```
LM I.D. = 0007                          PORT = XXXX


>CONTROLLER PASSED POC
>SPECIFY DRIVE BY ENTERING 0(DRIVE 0),1(DRIVE 1),
>[]
```

2. Enter the number of the drive to be tested.

```
▶ENTER THE NUMBER OF CYCLES FOR WHICH EACH TEST IS TO BE EXECUTED
▶CYCLE VALUES MUST BE ENTERED IN HEXADECIMAL
▶0 THRU 9, A THRU F OR ANY COMBINATION UP TO FFFF
▶(0-0FFFF, I =INFINITE, D = 1)
▶[]
```

3. Enter the number of times the test will execute.

NOTE

If infinite cycling is selected, the test can be terminated by pressing the FUNCTION/F1 keys.

When parameterization is completed, the screen displays the diagnostic test menu:

```
CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1
        RIGID DISK DRIVE (T-8409) TEST


▶DIAGNOSTIC TEST LIST
▶1 - RUN ALL TESTS CONSECUTIVELY
▶2 - SELECT DRIVE
▶3 - CONTROLLER LOOPBACK
▶4 - PREP TEST
▶5 - SEEK TEST
▶6 - WRITE/READ TEST
▶ENTER TEST SELECTION
▶[]
```

NOTE

Test 2 must be executed first if any drive other than drive 0 is selected.

4. Enter the number of the desired test and press TRANSMIT.

   a. In Test 1, tests 2 through 6 run consecutively and the cycle counter is updated after all tests are executed.

   b. Test 2 tests the invalid selection capability of the controller. The test attempts to select the drive specified by the operator and then initiates a series of invalid hardware controller functions: drive select, head select, sector select, and cylinder select.

c. In Test 3, the diagnostic performs the controller loopback test. One byte of data is sent to the controller and the controller returns four bytes of data with parity.

d. In Test 4, the program performs the controller-format-track function. The test is restricted to the customer engineer cylinder 600, reserved for read/write diagnostic operations.

e. In Test 5, the test executes a number of seek patterns to verify the capability of the seek mechanism in the disk.

f. In Test 6, the test writes and then reads back and verifies four data patterns on sector 1 of each CE cylinder for every track of the selected drive.

As the tests are executed the screen displays the following information:

```
LM I.D. = 0000          PORT = 0000          CYCLES = 0000
                          (line 4)
                        Title of Test
                          (line 5)

                      Title of Subtest
                          (line 7)

DRIVE = 0000   SECTOR = 0000   HEAD = 0000   CYLINDER COUNT = 0000
                          (line 9)


**TEST IN PROGRESS**
subtests passed

****TEST LIST COMPLETE****
NEXT OPERATION?
ENTER 1 (CONTINUE), 2 (REPEAT), 3 (START), 4 (EXIT)
```

where:

1 = At test completion, returns to diagnostic test list.
  = After an error, continues from where error occurred.
2 = Repeats current test.
3 = Returns to port selection of diagnostic test.
4 = Exits the diagnostic and returns to the system executive.

NOTE

3 (START) must be selected when a change in test cycles or drive is required.

8.3. Error Reporting

The console reports all errors as general statements of the error. If a command error occurs, the peripheral status block (PSB) is displayed (see paragraph 8.4).

Errors in the write/read test are displayed on the screen in the following format:

```
DEVICE STATUS = XX
FUNCTION CODE = YYZZ
LINE MODULE STATUS = AA00
PERIPHERAL CONTROL BLOCK (PCB) = BBBB
DATA BYTES TRANSFERRED = CCCC
```

followed by:

```
>NEXT OPERATION?
>ENTER 1 (CONTINUE), 2 (REPEAT), 3 (START), 4 (EXIT)
>[]
```

The entries in the error format have the following meanings:

XX = interface status byte from the 8409 controller

YY = a primary command to the 8409 controller
- 2B = "read peripheral status block"
- 2F = extended function command

ZZ = 00 if YY is 2B
- = X40 if YY is 2F, for "write"
- = X20 if YY is 2F, for "read"

AA00 = 0000 for no line module error
- = 1000 if line module message timer timed out
- = 2000 if line module response timer timed out
- = 3000 if a parity error was detected on data or status from the 8409 controller

BBBB = the number of bytes of the PCB that were transferred to 8409 controller (normally 0000 or 0010)

CCCC = the number of bytes transferred between the line module and the 8409 controller on a read or write (variable)

The following list summarizes the error messages. Perform the action recommended in the list or refer to Appendix A for trouble isolation procedure associated with the error. Also see MR6409, SPERRY Disk Subsytem Type 8409 Servicing for troubleshooting information.

Error Message Description	Isolation Procedure
THIS CONFIGURATION = DRIVE 0 ONLY The rigid disk is configured with a single drive.	-
PLEASE WAIT FOR READ STATUS BLOCK An abnormal message condition called the peripheral status block (PSB). (See paragraph 8.4).	-
CONTROLLER DOES NOT ANSWER This message is displayed under the following conditions: • After a master-clear or MODE 2 command. • When the host fails to receive the 36 bytes of identification and configuration data. • The device has no input power. • The cabling is incorrect.	-
THE PORT PROCESSOR CHAIN WOULD NOT EXECUTE The port processor could not read the line module ID.	00034
THE CHANNEL NUMBER IS NOT WITHIN THE LEGAL RANGE The selected port was either less than 0 or greater than XFF (decimal 255).	00034
CHANNEL WILL NOT INITIALIZE Either the line module is not present for the selected channel or it cannot communicate with the CLC.	00035
USE OF THE CONSOLE PORT IS INVALID The selected port is the console port. Re-enter the correct port number.	-

Error Message Description	Isolation Procedure
USE OF THE LOADER PORT IS ILLEGAL The selected port is the integrated diskette drive port. Re-enter the correct port number.	-
THIS LINE MODULE TYPE MAY NOT BE USED BY THIS DIAGNOSTIC The line module ID is incorrect. Re-enter the ID for the BILM/BDBI.	-
TEST DID NOT COMPLETE A function command caused an abnormal termination in the controller interface status byte (ISB).	-
UNABLE TO COMPLETE PSB The controller cleared the PSB before it could be retrieved. This message causes the diagnostic to go to START in order to generate a master clear.	-
READ STATUS COMMAND DID NOT WORK The command that calls the PSB was unable to complete and caused an abnormal termination in the interface status byte. This message causes the diagnostic to go to START in order to generate a master clear.	-
CONTROLLER DID NOT DETECT INVALID DRIVE The controller failed to set X04 in byte two of the PSB. (See paragraph 8.4.)	-
CONTROLLER DID NOT DETECT INVALID HEAD ADDRESS The controller failed to set X20 in byte two of the PSB. (See paragraph 8.4.)	-
CONTROLLER DID NOT DETECT INVALID SECTOR ADDRESS The controller failed to set X80 in byte two of the PSB. (See paragraph 8.4.)	-

8.4. Command Errors

Command errors occur during the write/read test. If an error occurs, the following prompt appears on the screen:

```
>ABNORMAL TERMINATION OF WRITE/READ TEST
>PRESS XMIT FOR READ STATUS BLOCK
>[]
```

When the TRANSMIT (XMIT) key is pressed, the display clears and the peripheral status block (PSB) scrolls onto the screen.

PSB	0//1	2//3	4//5	6//7	8//9	A//B
	TSDS	FRFE	CCCC	HHSS	SCNT	OOSD
	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX

where:

PSB Byte 0 = Termination status
PSB Byte 1 = Detailed read error status
PSB Byte 2 = Detailed function reject status
PSB Byte 3 = Flag byte
PSB Byte 4 = Cylinder address
PSB Byte 5 = Cylinder address
PSB Byte 6 = Track/sector (head) address
PSB Byte 7 = Track/sector (head) address
PSB Byte 8 = Sector count
PSB Byte 9 = Sector count
PSB Byte A = Not used. Set to zero.
PSB Byte B = Search displacement
PSB Byte C
thru
Byte F = Not used. Set to zero.

The following figures aid in interpreting the peripheral status byte:

Figure 8-1. Interpretation of the 0//1 Entry in the PSB Display
Figure 8-2. Peripheral Status Block Byte 0
Figure 8-3. Peripheral Status Block Byte 1
Figure 8-4. Interpretation of the 2//3 Entry in the PSB Display
Figure 8-5. Peripheral Status Block Byte 2
Figure 8-6. Peripheral Status Block Bytes 3 through F

0//1
TSDS
XXXX

PSB-0		PSB-1
XX	HEXADECIMAL	XX
Y Y Y Y Y Y Y Y	BINARY	Y Y Y Y Y Y Y Y
(MSB)7 6 5 4 3 2 1 0	BIT	7 6 5 4 3 2 1 0(LSB)

Figure 8-1. Interpretation of the 0//1 Entry in the PSB Display

---

NOTE

In the figures that follow, the column headings represent functions of the rigid disk. An X in the column beneath any of the headings identifies which errors occur during that function. Except where noted, bit 7 is the most significant bit (MSB).

Use the following information to interpret Figure 8-2:

- Bits 7 through 4 provide detailed abnormal termination status.
- Bits 3 through 0 provide detailed status for unusual but normal termination.
- If command termination is reported (bits 6, 5, or 4), then PSB Bytes 4 through 7 (Figure 8-6) contain the address of the sector which could not be processed.
- When a recoverable error is also reported, the address of the recovered sector is located in Bytes 4 through 7 and the address of the bad sector can be deduced from Bytes 8 and 9 (Figure 8-6) which contain the remainder of the sector count (including the bad sector).

  A sector count of one indicates that the error occurred in the last sector. An incomplete or bad (unreadable) sector may be written if bit 6 and/or bit 5 are reported. (The command was write or format track.)

PSB-0 TERMINATION STATUS

SEARCH EQ	SEARCH HI/EQ	SEARCH LOW	FORMAT TRACK	WRITE DATA	TEST READ	READ DATA	READ ID	RECAL IBRATE	SEEK		(BIT)
X	X	X	X	X	X	X	X	X	X	FUNCTION REJECT	7 (MSB)
X	X	X	X	X	X	X	X	X	X	DRIVE FAULT	6
X	X	X	X	X	X	X	X	X	X	WDS CONTROLLER ERROR	5
X	X	X	X	X	X	X	X			UNRECOVERABLE READ ERROR	4
X	X	X			X	X				RECOVERABLE READ ERROR	3
X	X	X	X	X	X	X	X	X	X	HIGH OPERATING TEMPERATURE	2
X	X	X								DATA SEARCHED FOR NOT FOUND	1
X	X	X	X	X	X	X	X	X	X	DRIVE NOT OPERATIONAL	0 (LSB)

where:

PSB-0 X	PSB-0 X	BIT	FUNCTION
8	0	7	FUNCTION REJECT: The command received was rejected prior to execution because invalid function and/or parameter(s) were found in the PCB.
4	0	6	DRIVE FAULT: The command was terminated because a fault indication was received from the disk drive (recalibrate function was performed).
2	0	5	WDS CONTROLLER ERROR: The command was terminated because a controller error was detected.
1	0	4	UNRECOVERABLE READ ERROR: The command was terminated because an unrecoverable read error or a second Error Correction Code (ECC) error was encountered.
0	8	3	RECOVERABLE READ ERROR: An ID field error was detected and an error recovery successfully performed on the sector identified by Bytes 4 thru 7.
0	4	2	HIGH OPERATING TEMPERATURE: The temperature inside the cabinet is approaching the maximum operating limit.
0	2	1	DATA SEARCHED FOR NOT FOUND: The search operation completed but the data was not found.
0	1	0	DRIVE NOT OPERATIONAL: The selected drive either failed POC or stopped operating.

Figure 8-2. Peripheral Status Block Byte 0

When the errors in Figure 8-3 are reported, the command in process was terminated prior to completion. Interpret the information as follows:

- Bytes 4 through 7 (Figure 8-6) contain the address of the bad sector.
- When the error is followed by a successful error recovery, Bytes 4 through 7 contain the address of the recovered sector.
- The address of the bad sector is deduced from the remainder of the sector count located in Bytes 8 and 9. That sector count contains the number of sectors not processed, including the one with the error.

  A sector count of one indicates that the error occurred on the last sector.

SEEK ERROR	SEEK COMPLETE	SEEK HALT/SEEK ABORT	FORMAT TRACK	WRITE DATA	TEST READ DATA	RESERVED	RESERVED	RESERVED ALTERNATE TRACK	SPARE SECTOR	PSB-1 READ ERROR STATUS	
											(BIT)
X	X	X		X	X	X	X			ID FIELD ERROR	7 (MSB)
X	X	X		X	X	X	X			CYLINDER HEAD MISCOMPARE	6
X	X	X		X	X	X	X			ALTERNATE TRACK IS FLAGGED BAD	5
X	X	X		X	X	X	X			ALTERNATE TRACK ERROR	4
							X			ILLEGAL FORMAT	3
X	X	X			X	X				SECOND ECC ERROR	2
			X							FORMAT TRACK ERROR	1
X	X	X	X	X	X	X				DATA FIELD ERROR	0 (LSB)

where:

PSB-1	= BIT =	FUNCTION
X X 8 0	7	ID FIELD ERROR: Uncorrectable error was detected in the ID of the sector; however, the controller attempted to recover the data. If bit 1 of the interface status byte (ISB) bit and bit 3 of the PSB Byte 0 are set, the data was recovered. If they were not set, the data was not recovered.

Figure 8-3. Peripheral Status Block Byte 1 (Sheet 1 of 2)

where:	PSB-1 X	= BIT =	FUNCTION (cont)
	4 0	6	CYLINDER/HEAD MISCOMPARE: The command was terminated because cylinder miscompare or head address miscompare occurred.
	2 0	5	ALTERNATE TRACK IS FLAGGED BAD: The command was terminated because the alternate track was flagged bad.
	1 0	4	ALTERNATE TRACK ERROR: The command was terminated while operating on an alternate track.
	0 8	3	ILLEGAL FORMAT: The command was terminated because an unreadable track was found.
	0 4	2	SECOND ECC ERROR: The command was terminated because a second ECC error was detected. (The first error was corrected.) No attempt was made to recover from the second error condition.
	0 2	1	FORMAT TRACK ERROR: Read error on format track command occurred.
	0 1	0	DATA FIELD ERROR: An ECC error was detected in the data field; however, the controller attempted to recover the data. If bit 1 of the ISB and bit 3 of the PSB Byte 0 are set, the data was recovered. If they are not set, no recovery took place.

Figure 8-3. Peripheral Status Block Byte 1 (Sheet 2 of 2)

2//3
FRFE
XXXX

PSB-2		PSB-3
XX	HEXADECIMAL	XX
Y Y Y Y Y Y Y Y	BINARY	(FLAG BYTE)
(MSB) 7 6 5 4 3 2 1 0	BIT	

Figure 8-4. Interpretation of the 2//3 Entry in the PSB Display

One of the conditions described in Figure 8-5 is reported if bit 3 of the ISB and bit 7 of the PSB Byte 0 are set.

SEARCH EQ	SEARCH HI/EQ	SEARCH LOW	FORMAT TRACK	WRITE DATA	TEST READ DATA	READ DATA	READ ID	READ ALIBRATE	SEEK	PSB-2 FUNCTION REJECT STATUS	(BIT)
X	X	X		X	X	X				ILLEGAL SECTOR ADDRESS	7 (MSB)
X	X	X	X	X	X	X			X	ILLEGAL CYLINDER ADDRESS	6
X	X	X	X	X	X	X	X			ILLEGAL HEAD ADDRESS	5
										ILLEGAL FUNCTION	4
X	X	X	X	X	X	X	X			ILLEGAL FLAG BYTE	3
X	X	X	X	X	X	X	X	X	X	NON-EXISTENT DRIVE	2
X	X	X								INVALID SEARCH PARAMETER	1
X	X	X		X	X	X				INVALID SECTOR COUNT	0 (LSB)

where:

PSB-2		BIT	FUNCTION
X	X		
8	0	7	ILLEGAL SECTOR ADDRESS: The function was rejected because an illegal sector address was specified.
4	0	6	ILLEGAL CYLINDER ADDRESS: The function was rejected because the cylinder address specified in the PSB is out of range for the selected disk drive.
2	0	5	ILLEGAL HEAD ADDRESS: The function was rejected because a non-existent head was addressed.
1	0	4	ILLEGAL FUNCTION: The specified function was not valid.
0	8	3	ILLEGAL FLAG BYTE: The specified flag byte was not FA16 or FE16.
0	4	2	NON-EXISTENT DRIVE: Selected drive not present.
0	2	1	INVALID SEARCH PARAMETER: The sector count was invalid.
0	1	0	INVALID SECTOR COUNT: The sector count exceeds the maximum allowed.

Figure 8-5. Peripheral Status Block Byte 2

SEARCH EQ	SEARCH HI/EQ	SEARCH LOW	FORMAT TRACK	WRITE DATA	TEST READ DATA	READ DATA	READ ID	READ ALIB RATE	SEEK			
X	X	X		X	X	X	X		FLAG BYTE			PSB-3
X	X	X		X	X	X	X		CYLINDER ADDRESS	PSB-4 (MSB)		PSB-5
X	X	X		X		X	X		HEAD ADDRESS			PSB-6
X	X	X		X	X	X	X		SECTOR ADDRESS			PSB-7
X	X	X		X	X	X			SECTOR COUNT	PSB-8 (MSB)		PSB-9
-	-	-	-	-	-	-	-		NOT USED			PSB-A
X	X	X							SEARCH DISPLACEMENT BYTE			PSB-B
-	-	-	-	-	-	-	-		NOT USED		PSB-C,-D,-E,-F	

where: FLAG BYTE: Byte 3 contains the second byte of the address field of the last selected track.

CYLINDER ADDRESS: Bytes 4 and 5 contain the address for the last selected cylinder, or the address for the cylinder containing a bad sector which was corrected by the controller.

HEAD/SECTOR ADDRESS: Bytes 6 and 7 contain the address of the last selected head/sector, or the address of the bad sector which was corrected by the controller.

SECTOR COUNT: Bytes 8 and 9 contain the remainder of the peripheral control block (PCB) sector or track-count byte. Byte 8 is always zero when a read or write operation is completed successfully. If a command was terminated prior to completion, the sector/track count contains the number of unprocessed sectors or tracks. A count of one (1) indicates one unprocessed track or sector.

NOT USED: Byte A is not used (set to zero).

SEARCH DISPLACEMENT BYTE: Byte B is used for search operations only. The value of the byte represents the number of bytes preceding the key field of the sector which satisfied the search condition.

NOT USED: Bytes C through F are not used (set to zero).

Figure 8-6. Peripheral Status Block Bytes 3 Through F

9. SYSTEM TEST

9.1. Introduction

The system test exercises the complete system configuration . The test simulates Telcon with the advantage that the system test loads faster than Telcon and errors are more easily identified. The system test consists of four subtests:

- Serial Line Module Subtest
- Local Storage Subtest
- Cartridge Disk Storage Subsystem (T8408) Subtest
- Freestanding Diskette Subsystem (FDS) (T8406) Subtest

The serial line module subtest tests the same group of line modules as the serial line module diagnostic test (Section 4).

F1941	Asynchronous Line Module
F1942	Synchronous Line Module
F3163	Medium Speed Loadable Line Module
F3164	High Speed Loadable Line Module
F3165	Multiline Asynchronous Line Module
F3837	Multiline Line Module
F3847	Direct Connect Single Station Line Module
F4230	Twisted Pair Line Module

The subtest checks a selected port using a selected protocol. The autostart option randomly picks a protocol for a given port or a protocol can be selected by the operator. If necessary, the subtest loads the line module with microcode. The subtest checks the line module using internal loopback and keeps an error count.

The local storage subtest executes random read/write operations throughout the available local memory of the DCP and keeps an error count.

The disk storage subsystem and the diskette storage subsystem subtests perform random read/write operations and keep an error count.

9.2. Test Procedure

NOTE

Press the FUNCTION/F2 keys to stop execution of a subtest and return to the system test menu. To restart subtest execution without affecting accumulated test data, use option 5.

CAUTION

AUTOSTART (option 1) destroys all accumulated test data and resets all values, such as total run time, error log data, to zero.

When the system test is selected from the diagnostic test list, the console displays the system test menu:

```
CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1
SYSTEM TEST

>LOADING TEST MESSAGE FILE
>1.  AUTOSTART
>2.  INITIALIZE A PORT WITH A SUBTEST
>3.  CANCEL A SUBTEST ON A PORT
>4.  CANCEL ALL SUBTESTS
>5.  EXECUTE SUBTESTS ON INITIALIZED PORTS
>6.  DISPLAY ERROR LOG
>7.  DISPLAY PORT INFORMATION
>8.  EXIT
>PRESS TRANSMIT KEY TO DISPLAY OTHER SELECTIONS. OR
>SELECT A TEST NUMBER FROM THE MENU
>ENTER CHOICE
>[]
```

NOTE

If the configuration build routine was not completed during initialization of the diagnostic program, the screen displays the message:

CONFIGURATION TABLE NOT BUILT

The program returns to the diagnostic test menu. Execute the build routine using the Run Configuration (RC) command explained in Section 16.

The test options are summarized as follows:

1. AUTOSTART executes the subtests automatically. It provides the following choices: test line modules using several randomly selected protocols or using one randomly selected protocol; test a user-selected CLC or test all CLCs. The test also requests configuration information for the disk and diskette subsystems.

   AUTOSTART automatically initializes the line module(s), loading an appropriate subtest and, if applicable, an appropriate protocol. When initialization is completed, it executes the subtests.

2. INITIALIZE A PORT WITH A SUBTEST selects a specific port for testing with a specific protocol.

   If you select AUTOSTART to execute the subtests, the function does not change the user-selected protocol. It does destroy all previously gathered test data for that port.

3. CANCEL A SUBTEST ON A PORT stops communication with a user-selected line module.

4. CANCEL ALL SUBTESTS stops communication with all line modules and program returns to system test menu.

5. EXECUTE SUBTESTS ON INITIALIZED PORTS starts execution of the subtests. You must select option 1 or 2 before this option. Testing continues until the F2 key is pressed.

6. DISPLAY ERROR LOG displays error log information. The format is the same as DISPLAY PORT INFORMATION. Press MSG WAIT and XMIT to exit the error log. If no errors have occurred, the screen displays the system test menu.

7. DISPLAY PORT INFORMATION displays general port information in the following format:

PORT#	PROTOCOL	CYCLES	ERRORS	DAYS	HRS	MINS
XXX	XXXXXXX..	XXXX	XXXX	XX	XX	XX

   The entries are defined in paragraph 9.3.1.

   To exit from this display (without displaying all of the ports), press MSG WIT and XMIT. The program returns to the system test menu.

8. EXIT turns off all line modules and exits to the diagnostic test menu.

9.3. Test Execution

During execution of option 1 or option 5, the screen continuously updates the following display:

```
TOTAL RUN TIME IS XX DAYS  XX HOURS  XX MIN  XX SEC XX
TOTAL ERRORS DETECTED = XXXX

PORT  CYC  ERR  PORT  CYC  ERR  PORT  CYC  ERR  .......
XXXX  XXXX XXXX XXXX  XXXX XXXX XXXX  XXXX XXXX .......
XXXX  XXXX XXXX XXXX  XXXX XXXX XXXX  XXXX XXXX .......
```

where:

PORT = port number in hexadecimal
CYC = five data transactions per cycle count
ERR = number of errors detected

The diagnostic detects the following types of errors:

Data compare errors
Character detect table errors
Initialization errors: could not initialize port processor on this port
Port time-out errors

NOTE

Screen space limits the number of ports displayed. To view the next 32 ports, press MSG WAIT.

If option 5 is selected and a port is not initialized (options 1 and 2), the following message appears:

*** No ports are initialized ***

During execution of option 2 or 3, the console displays a port number request:

```
>ENTER PORT # (IN HEX) OR XMIT TO EXIT:
>[]
```

The next display confirms the port number and line module ID and requests the device. The example shows selection of port 0004.

```
>PORT = 0004
>LINE MODULE ID = 0002
> 1.  LOCAL STORAGE SUBTEST
> 2.  FREESTANDING DISKETTE (FDS) SUBTEST
>ENTER CHOICE:
>[]
```

If the FDS subtest is selected, then the screen displays further test selectiona:

```
>PLACE A WRITE ENABLED, PREPPED DISKETTE IN DRIVE(S)
>WARNING - DATA WILL BE DESTROYED
> 1.  TEST DRIVE 0
> 2.  TEST DRIVE 1
> 3.  TEST BOTH DRIVES
>ENTER CHOICE
>[]
```

If a port, such as port 0004 in the previous example, is already initialized, then the screen displays the message:

```
>PORT ALREADY INITIALIZED.  RE-INITIALIZE?
>(1 = YES, XMIT = NO)
>[]
```

9.3.1. Error Log and Port Information Screen Display

Both of these options produce the following display of test data:

PORT#	PROTOCOL	CYCLES	ERRORS	DAYS	HRS	MINS
XXXX	XXXXXXXX	XXXX	XXXX	XX	XX	XX

where:

PORT# = port number in hexadecimal
PROTOCOL = type of protocol:
- UDLC
- SYNCH
- ASYNCH
- 4X1 UDLC
- 4X1 UNISCOPE
- 4X1 ASYNCH
- HS UDLC
- HS SYNCH
- X.21 UDLC
- X.21 SYNCH
- ASYNCH 4X1
- DCSS
- L/S TEST

CYCLES = number of test cycles completed for selected port
ERRORS = number of errors detected on port
DAYS/HRS/MINS = period of time protocol has run for selected port

The protocols that are supported by the various line modules are summarized in the following list. The list includes the line module ID (LMID), and the line module acronym.

Feature	Line Module Name/Acronym	Electrical Interface	Protocol	LMID
F1941-00	Asynchronous (Asynch)	RS-232C	Asynchronous UNISCOPE	40
F1942-00	Synchronous (Synch)	RS-232C	Synchronous	50
F3163-00	Medium Speed Loadable (MSLLM)	RS-232C	Asynchronous Synchronous UDLC	67
F3163-01	MSLLM	X.21	Asynchronous UDLC	61
F3163-04	MSLLM	RS-449	Asynchronous Synchronous UDLC	60
F3164-00	High Speed Loadable (HSLLM)	Bell 303	Synchronous UDLC	7D
F3164-01	HSLLM	V.35	Synchronous UDLC	7E
F3165-00	Multiline Asynchronous (MLALM/4X1 Asynch)	RS-232C	Asynchronous	44
F3165-01	MLALM Video Text (4X1 Asynch Video Text)	RS-232C	Asynchronous	45
F3837-00	Multiline (MLLM/4X1 Synch)	RS-232C	Synchronous UDLC UNISCOPE	54
F3847-00	Direct Connect Single Station (DCSS)	Non-standard (Coaxial connection)	UDLC	64
F4230-00	Twisted Pair (TPLM)	Northern Telcom SL1-PBX	UDLC	65

10. MULTIPLE DEVICE LINE MODULE MASS STORAGE DIAGNOSTIC TEST

10.1. Introduction

The multiple device line module (MDLM) mass storage diagnostic test checks the major functions of the SPERRY Multiple Device Line Module F3893.

10.2. Test Procedure

CAUTION

All data on the rigid disk or the diskette will be destroyed during the format test and the write/read test. During the rigid disk diagnostics, a warning message is displayed prior to execution of the tests. No warning message is displayed during the diskette tests unless a diagnostic or Telcon diskette is loaded.

When the MDLM diagnostic test is selected from the system menu, the screen displays a series of prompts which request the test parameters.

```
CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1
MDLM MASS STORAGE TEST

>ENTER PORT PROCESSOR NUMBER IN HEX, 00-FF DEFAULT = 00XX*
>[]

*where XX = the loader port.
```

1. Enter the port number of the MDLM and press the TRANSMIT (XMIT) key. The program tests the line module ID for that port. If the MDLM is in the designated port and will initialize, the screen displays the line module ID, 0009, and the loader port number at the top of the screen.

```
>ENTER TARGET (CONTROLLER) X, L.U.N. (DEVICE) Y, (00-FF)
>[]
```

2. Enter the parameters as X for the controller and Y for the device, with a range of 00-77. Currently defined values are:

DCP/10A/:	Rigid Disk	- target = 7, L.U.N. = 0
DCP/15	Diskette	- target = 7, L.U.N. = 2
T8441:	1st Rigid Disk	- target = X*, L.U.N. = 0
	2nd Rigid Disk	- target = X*, L.U.N. = 1
	1st Diskette	- target = X*, L.U.N. = 2
	2nd Diskette	- target = X*, L.U.N. = 3

When the target and the L.U.N. are accepted, the console displays the map of the devices, the device configuration data, and the prompt:

```
>ENTER XMIT TO CONTINUE, (1) TO SELECT ANOTHER L.U.N.
>[]
```

If the diskette is selected, the screen displays the following warning message:

```
**WARNING**
INSERT SCRATCH DISKETTE IN DRIVE TO BE TESTED
ENTER XMIT TO CONTINUE, (1) TO SELECT ANOTHER L.U.N.
```

3. Insert a scratch diskette if you are testing the diskette device.

```
>ENTER THE NUMBER OF CYCLES FOR WHICH EACH TEST IS TO BE
>EXECUTED
>CYCLE VALUES MUST BE ENTERED IN HEXADECIMAL
>0 THRU 9, A THRU F OR ANY COMBINATION UP TO FFFF
>(0-0FFFF, I = INFINITE, D = 1)
>[]
```

4. Enter the number of times the test will execute.

NOTE

If you select multiple cycles, the disk warning message is displayed during the first cycle only.

*Defined by strapping switches in T8441.

When parameterization is complete, the screen displays the diagnostic test menu, six selections at a time.

```
CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1
MDLM MASS STORAGE TEST


>MDLM MASS STORAGE TEST LIST
>1 - RUN ALL TESTS CONSECUTIVELY
>2 - SELECT TEST
>3 - LINE MODULE LOOPBACK
>4 - FORMAT TEST
>5 - SEEK TEST
>6 - WRITE/READ TEST
>PRESS TRANSMIT KEY TO DISPLAY OTHER SELECTIONS, OR
>SELECT A TEST NUMBER FROM THE MENU
>[]
```

If the transmit key is pressed, the last selection is displayed:

```
>7 - PARK HEADS FOR SHIPPING
>ENTER TEST SELECTION NUMBER
>[]
```

NOTE

Pressing the the FUNCTION/F2 keys terminates the tests. Terminating the tests during the format sequence is not recommended.

5. Enter the test number (1 through 6) and press the TRANSMIT (XMIT) key.

NOTE

The format test checks each logical block using four data patterns. The write/read test uses one data pattern and random seeks. The format test identifies problems with the media but does not isolate timing problems. The write/read test does both. If your concern is the media, the write/read test may be bypassed.

a. In Test 1, the tests run consecutively and the cycle counter is updated after all tests are executed.

During the rigid disk tests, the console displays a warning message before the format and write/read tests:

```
**WARNING**DATA ON SELECTED DRIVE WILL BE DESTROYED
>ENTER (1) TO CONTINUE, PRESS XMIT TO ABORT
>[]
```

If you select 1, you are given a second chance:

```
>**ARE YOU SURE?** (1) TO CONTINUE, XMIT TO ABORT
>[]
```

If you choose to format the disk, the warning does not appear when the write/read test begins.

If you select the diskette test and a diagnostic or Telcon diskette is in the drive, the following warning appears before the format test:

```
**WARNING.  DIAGNOSTIC (TELCON) DISKETTE IS IN DRIVE.
>ENTER (1) TO CONTINUE, PRESS XMIT TO ABORT
>[]
```

If you chose to format the diskette, the warning does not appear during the write/read test.

b. In Test 2, the test selects the L.U.N. specified by the operator (if more than one is configured) and then initiates a series of hardware controller functions: target select, L.U.N. select, and cylinder select.

c. In Test 3, the diagnostic performs the line module loopback test. One byte of data is sent to the MDLM and it returns a byte of data which is compared with the one sent. All 256 possible bytes (00 - FF) are sent.

d. In Test 4, the program performs the controller-format-track (prep) function. There are two options: Type 0 and Type 1.

Type 0 uses new mode-select data. Select this format when you are installing a new drive. Type 0 formats 5-1/4 inch flexible diskettes for 512 bytes/sector, 9 sectors/track, DSDD, 96 tracks per inch (tpi). Rigid drives can be formatted for 10, 30, or 72 megabytes depending on the drive installed. The format is 256 bytes/sector, 32 sectors/track (Telcon format). If a 30- or 72-megabyte device is prepped at lesser capacity, the additional space is not available for use.

NOTE

Care must be taken when using the Type 0 format. The 10 megabyte drives will not return an error status if an attempt is made to format them at a higher capacity. Positive knowledge of drive capacity is essential when specifying a Type 0 format operation.

Type 1 formats the device using the existing mode-select data which the controller reads from the drive at 256 bytes/sector (logical block).

Approximate format times for the drives are:

10 MB	20 MB	30 MB	72 MB
15 mins.	30 mins.	40 mins.	90 mins.

NOTE

When the format test is completed, the console displays the sense bytes. A successful result is:

```
>sense bytes  vld   ky/   blocks      ecc/rtry
              F000  0900  0000 0000   0000 0000
```

e. In Test 5, the diagnostic executes a number of seek patterns to verify the capability of the seek mechanism in the disk.

NOTES

If the write read test is performed on the fixed disk, you must reformat the drive using a Type 0 format before the drive can be used by Telcon.

When the write read test is executed using the RUN ALL TESTS CONSECUTIVELY option, enquiry data written on the disk by FORMAT TEST is destroyed. When FORMAT TEST is executed on a subsequent pass, an error is generated because it uses Type 1 format and the enquiry data is invalid.

f. In Test 6, the test writes and then reads back and verifies one data pattern and performs random seeks of the data. The test checks the selected logical blocks of the L.U.N.

g. In Test 7, the heads are moved to a safe location in the drive in preparation for shipping (10 Mbyte drive only).

As each test is executed, the screen displays information about the test and the parameters. A sample display follows.

```
          CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1
                       MDLM MASS STORAGE TEST
PORT IS 0005  LM I.D. = 0009    TARGET/LUN = 7070
                              (line 3)
WRITE/READ TEST     ***TEST IN PROGRESS (or TEST COMPLETE)***
                              (line 4)
                    data pattern = 6DB6 DB6D B6DB
                              (line 5)



(Test information - up to 10 lines)
>RESPONSE FROM TARGET/LUN 0070
>RESPONSE FROM TARGET/LUN 0072
>RESPONSE SUB-TEST COMPLETE
>FORMAT COMPLETE
>[]
```

The upper two digits of the target/L.U.N. display identify the selected device. The lower two digits identify the target/L.U.N. that answered the last good command. The two sets of numbers should be the same. The data-pattern display applies to the write/read test and the loopback test.

At the end of the test or when an error occurs, the console displays the following message:

```
>NEXT OPERATION?
>ENTER 1 (CONTINUE), 2 (REPEAT), 3 (START), 4 (EXIT), 5 (RETRY)
>[]
```

where:

1 = At test completion, returns program to test selection.
  = After an error, continues from where error occurred.
2 = Repeats current test.
3 = Goes to the start of the diagnostic test. Must be selected when a change in test cycles or drive is required.
4 = Exits the diagnostic and returns to the system executive.
5 = Retries the last I/O when an error occurs.

10.3. Error Reporting

The console reports errors as general error statements or error codes. The code specifies what the program was doing when the error occurred. If a command error occurs, all available status is displayed.

The console displays the error information for all of the tests in the following format:

```
>Explanation message
>command descriptor block  CMD    LOG.BLK  COUNT'
>I/O status  CMD      DATA   FLAG    CNT     DEVC    SCSI
>expected:   (AAAA)  (BBBB)  (CCCC)  (DDDD)  (EEEE)  (FFFF)
>received:
>sense bytes, if available
```

where:

AAAA = Line module status for command transfer from MDLM to SCSI controller

BBBB = Line module status for data transfer to/from MDLM and SCSI

CCCC = Flag word which provides a trace of port processor operations

DDDD = The number of bytes transferred between the line module and the SCSI controller on a read or write (variable)

EEEE = Device error status

FFFF = SCSI error status

Following is a sample of an error information display and detailed descriptions of the command descriptor block, the I/O status, and the sense bytes.

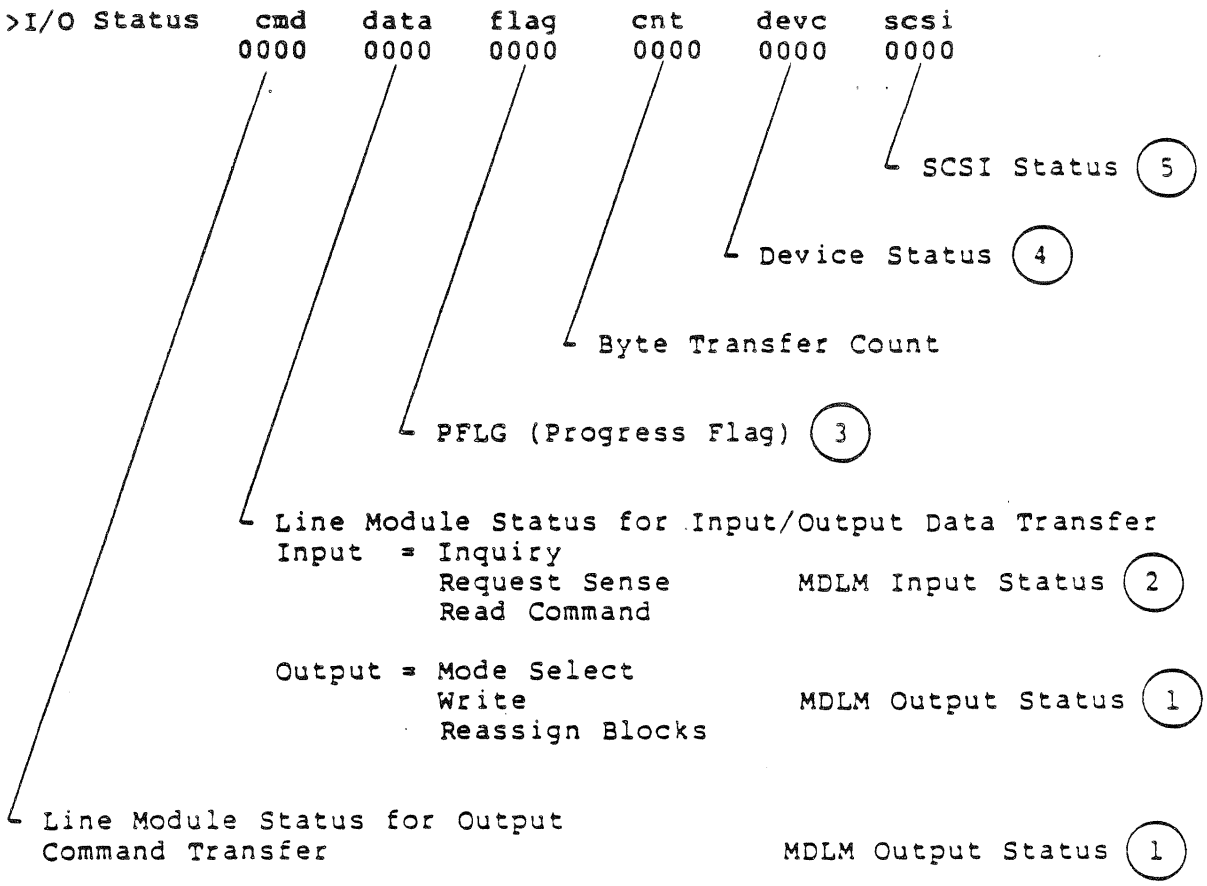
```
>BAD STATUS ON SEEK COMMAND
>command descriptor block     CMD     LOG.BLK    COUNT
                              0B00     C3A0      0000
>I/O status    cmd    data    flag    cnt    devc    scsi
 expected =   0000    0000    00A7    0000   0000    0000
 received =   0021    0000    00A7    0000   0200    0000
>sense bytes   vld    ky/     blocks        ecc/rtry
               F000   0500   00C3 A000    0000 0000
>seek was to logical block 0000C3A0
>last seek was to logical block 00000042
```

```
>command descriptor block     CMD   LOG.BLK   COUNT
                              0000  0000      0000

COMMAND                        0 1   2 3      4 5

Test Ready                    00L0  0000      0000
Rezero Unit                   01L0  0000      0000
Request Sense                 03L0  0000      ##00
Format 0                      04L0  0000      0000
                                                8000
Format 1                      04L0  0000      0000
Seek                          0BL/LBADR/      0000
Inquiry                       12L0  0000      2800
Mode Select                   15L0  0000      1000
Reassign Block                07L0  0000      0000
Reserve Unit                  16L0  0000      0000
Release Unit                  17L0  0000      0000
Stop Unit                     18L0  0000      0000
                                                7   8
Read Data                     28L0  /  LBADR /  #BLKS
Write Data                    24L0  /  LBADR /  #BLKS
```

where: L = logical unit (left-shifted one bit)
##: byte 4 = number of bytes allocated for sense data
Format 0: byte 4 (0000) = 256 bytes/logical block
Format 0: byte 4 (8000) = 512 bytes/logical block
Format 1: byte 4 (0000) = 256 bytes/logical block
Inquiry: byte 4 = 28
Mode Select: byte 4 = 10 (the length of parameter list)
LBADR = logical block address
#BLKS = number of blocks of data to be transferred (always 1)



Refer to the following lists, identified by the circled numbers, for the description of the status bits.

NOTE

The status is displayed in hexadecimal. The bits are numbered 0 through 15 as follows:

0				0				HEXADECIMAL	0				0			
X	X	X	X	X	X	X	X	BINARY	X	X	X	X	X	X	X	X
0	1	2	3	4	5	6	7	BITS	8	9	10	11	12	13	14	15

(1) MDLM OUTPUT STATUS

Bit	Status	Description
4*	Response Timer	Set if output response timer expires. Causes unconditional termination.
5	Message Timer	Set if output message timer expires. Causes unconditional termination.
6	Adapter Error	Set if error is detected by line module during output operation. Causes unconditional termination.
7	Wrong Path	Set if current physical path is established to a device other than the requested one. Causes unconditional termination.
8	Break Path	Set if disconnect message is received by the line module. To obtain the amount of valid data that was transferred, execute read transfer count instruction.
9	Buffer Active	Set if command complete message was received during output data transfer and the line module still has data in its output buffer. Causes unconditional termination. To obtain amount of valid data that was transferred, execute read transfer count instruction.
10	Check Sense	Set if sense data is available. Causes unconditional termination. To obtain sense data, excute input SDT instruction with request function flag set.
11	Device Busy	Set if device is busy or reserved. Causes unconditional termination.
12	Restore Pointers	Set if restore pointers message is received by the line module. Causes unconditional termination. To obtain amount of valid data transferred, execute read transfer count instruction.
14	Read Status	Set if command completion status received from device contains status bits other than Check Sense and Busy. Causes unconditional termination.
15**	Status Branch	Set by CLC if a status bit is set and its corresponding chain flag is clear. Occurs only after the line module status is passed to the CLC.

*MSB
**LSB

(2) MDLM INPUT STATUS

Bit	Status	Description
0*	No Buffer	Set by CLC when allocating input space and the zeroed buffer pool is empty. Causes unconditional termination.
1	Input Limit	Set by CLC when input limit is reached and input chain flag 17 is set.
4	Response Timer	Set if input response timer expires. Causes unconditional termination.
5	Message Timer	Set if input message timer expires. Causes unconditional termination.
6	Adapter Error	Set if error is detected by line module during input operation. Causes unconditional termination.
7	Wrong Path	Set if current physical path is established to a device other than the requested one. Causes unconditional termination.
8	Break Path	Set if disconnect message is received by the line module. To obtain the amount of valid data that was transferred, execute read transfer count instruction.
10	Check Sense	Set if sense data is available. Causes unconditional termination.
11	Device Busy	Set if device is busy or reserved. Causes unconditional termination.
12	Restore Pointers	Set if restore pointers message is received by the line module. Causes unconditional termination. To obtain amount of valid data transferred, execute read transfer count instruction.
14	Read Status	Set if command completion status received from device contains status bits other than Check Sense and Busy. Causes unconditional termination.
15**	Status Branch	Set by CLC if a status bit is set and its corresponding chain flag is clear. Occurs only after the line module status is passed to the CLC.

*MSB
**LSB

(3) PFLG (PROGRESS FLAG) WORD DEFINITIONS

Bit	SF Mask	Definition
15*	000	Read/Write Chain Started
14	040	Data Read Started
13	020	Data Write Started
12	010	Inquiry Chain Started
11	008	Sense Chain Started
10	004	Loopback Chain Started
9	002	Loopback Write Complete, Starting Read
8	001	Starting Variable Data Output Chain
7	080	Send CDB Chain Started
6	040	Not Used
5	020	CDB Transfer Complete (any command chain)
4	010	Data Transfer Complete, Loopback complete
3	008	Clear, Set Device Address Chain Complete
2	004	Read Status Chain Started
1	002	Device Status Valid
0**	001	I/O Chain Complete

(4) DEVICE STATUS

Bit	Status	Description
0*	Extended Status	Set if the second byte has valid data.
1	Vendor unique	
2	Vendor unique	
3	Intermediate Status	Set if any intermediate status is sent during a series of linked SCSI instructions. This bit is not set for any ending status. Linking of SCSI instructions is not supported by the MDLM, so bit 3 should never be set.
4	Device Busy	Set if device is busy or reserved.
5	Conditions Met	Set if a test condition is met.
6	Check Sense	Sense data is available.
7	Vendor Unique	
15**	Retry Occurred	A message, SCSI status, IPL command, or sense command was transferred successfully by the MDLM, but some recovery action was required.

*MSB
**LSB

(5) SCSI STATUS

Bit	Status	Description
0XXX		
0*	Parity Error	Set if parity error was detected by the line module during the transfer of an input data byte.
1	SCSI Timeout	Set if controller does not respond to selection sequence (or fails during reselection sequence). Usually occurs because controller is non-existent or has not completed POC.
2	SCSI Clear	Set if line module detected a SCSI interface clear.
3**	Hardware Error	Set if line module detected an unrecoverable parity error.

*MSB
**LSB

>sense bytes vld ky/ blocks ecc/rtry
0000 0000 0000 0000 0000 0000

COMMAND	0	1	2	3	4	5	6	7	8	9
Test Unit Ready	70	00	0K	00	00	00	00	00	00	00
Rezero Unit	70	00	0K	00	00	00	00	00	00	00
Request Sense	80/00	00	0K	00	00	00	00	00	00	00
Format 0 (256)	70	00	0K	#DEFECTVE BLKS				00	00	00
(512)	F0	00	0K	#DEFECTVE BLKS				00	00	00
Format 1 (256)	70	00	0K	#DEFECTVE BLKS				00	00	00
Seek	70	00	0K	00	00	00	00	00	00	00
Inquiry	70	00	0K	00	00	00	00	00	00	00
Mode Select	70	00	0K	00	00	00	00	00	00	00
Reassign Block	70	00	0K	BLK # NOT READ				00	00	00
Reserve Unit	70	00	0K	00	00	00	00	00	00	00
Release Unit	70	00	0K	00	00	00	00	00	00	00
Stop Unit	70	00	0K	00	00	00	00	00	00	00
Read Data	70	00	0K	LST BLK ERROR/				00	00	#ECC
Write Data	70	00	0K	LST BLK ERROR/				00	00	#RTRY

where: 70, F0, 80, or 00 = valid bit (upper bit can be 0 or 1)
K = sense key byte
#DEFECTVE BLKS = number of defective blocks, if any
BLK # NOT READ = block number that could not be read
LST BLK ERROR = last block where an error was found
#ECC = number of ECCs during a read operation
#RTRY = number of re-tries during a write operation

vld
0XXX If 70, sense command completed but only sense key is valid.
If F0, sense command completed and data is valid.
If 80, sense command did not complete but sense key is valid.
If 00, sense command did not complete or no sense data is available.

ky/
X0XX If the valid bit is set (F or 8), the sense key for the all of the commands is:

Search/No Find	0
Recoverable Error	1
Media Error	3
Hardware Error	4
Format Complete	9
Search/Found	C
Volume Overflow	D

If the valid bit is not set (0 or 7), the sense key for the command is:

SENSE KEY		COMMAND												
		TUR	REZERO	SENSE	FRMAT	READ	WRITE	SEEK	INQUIR	MDSEL	READS	RELSE	COPY	STOP
No Sense	0			X										
Recoverable Error	1					X	X	X			X		X	
Not Ready	2	X	X	X	X	X	X	X		X	X		X	X
Media Error	3			X	X	X	X		X	X	X		X	
Hardware Error	4	X	X	X	X	X	X	X	X	X	X	X	X	X
Illegal Request	5	X	X	X	X	X	X	X	X	X	X	X	X	X
Unit Attention	6	X	X	X	X	X	X	X			X	X	X	X
Format Complete	9				X									

The error information for the individual tests is summarized as follows:

- Select Test

  Error messages are:
  AN INVALID TARGET/L.U.N. WAS SELECTED AND RETURNED GOOD STATUS.

  COULD NOT RE-SELECT INITIALLY SELECTED TARGET/L.U.N.

  SEEK TO LAST VALID LOGICAL BLOCK ON THE DISK/DISKETTE RETURNED AN ERROR.

  SEEK TO 1 PAST LAST VALID LOGICAL BLOCK ON THE DISK/ DISKETTE DID NOT RETURN AN ERROR.

- Loopback Test

  Documented errors are limited to bad I/O status and miscompare of data sent and received. Reported in error information display.

- Format Test

  Sense bytes are displayed at the end of the prep. A successful completion is:

  ```
  >sense bytes  vld   ky/   blocks     ecc/retry
                F000  0900  0000 0000   0000
  ```

- Seek Test

  Documented errors are limited to bad status on seek command and are reported in error information display. Display includes following messages:

  SEEK WAS TO LOGICAL BLOCK XXXXXXXX
  LAST SEEK WAS TO LOGICAL BLOCK XXXXXXXX

- Write/Read Test

  Documented errors are limited to bad status and data compare errors and are reported in error information display. Display includes following messages:

  READ/WRITE WAS TO LOGICAL BLOCK XXXXXXXX
  LAST READ/WRITE WAS TO LOGICAL BLOCK XXXXXXXX

The list that follows summarizes the error messages and identifies the order to follow during trouble isolation procedure 00036 in Appendix A. Note that this listing differs from those in other sections of the book. It provides the isolation order (1, 2, 3, 4), not the isolation procedure. Only one isolation procedure, 00036, is defined for the MDLM.

Error Message Description	Isolation Order for 00036
Status Messages	-
The following status messages are part of the error information display. They are followed by the command descriptor block.	
BAD STATUS FROM READ DEVICE ID COMMAND	2, 1
BAD STATUS FROM REZERO UNIT COMMAND	2, 3/4
BAD STATUS FROM SEEK COMMAND	3/4
BAD STATUS FROM READ SENSE COMMAND	2, 3/4, 1
BAD STATUS FROM MODE 1 READ COMMAND	2, 3/4 1
BAD STATUS FROM MODE 1 WRITE COMMAND	2, 3/4 1
BAD STATUS FROM MODE 0 LOOPBACK READ COMMAND	2, 1
BAD STATUS FROM MODE 1 LOOPBACK READ COMMAND	2, 1
BAD STATUS FROM MODE SELECT COMMAND	1, 2
BAD STATUS FROM FORMAT COMMAND	3/4, 2, 1
BAD STATUS FROM INQUIRY COMMAND	2, 3/4
BAD STATUS FROM STOP COMMAND (Only valid on a head stop)	2, 3

Error Message Description	Isolation Order for 00036
General Error Messages	
INVALID INPUT, PLEASE TRY AGAIN An input cannot be translated properly (e.g., an alpha character was received when a numeric input was expected).	-
USE OF CONSOLE PORT IS INVALID Re-enter number of port where MDLM is installed.	-
CHANNEL WILL NOT INITIALIZE ENTER PP NUMBER (HEX 00-FF D=00XX) Selected port is not communicating with the CLC. Re-enter port number of MDLM.	1
THE LINE MODULE TYPE MAY NOT BE USED BY THIS DIAGNOSTIC	-
CHANNEL NUMBER IS NOT WITHIN THE LEGAL RANGE Port number entered is not the MDLM. Check configuration and enter correct number.	-
SCSI CLEAR, DEVICE SELECT FAILED Unable to access target/L.U.N. following clear.	2, 3/4
PP DID NOT RESPOND TO I/O REQUEST Port processor has stopped. See progress flag word to determine where hang occurred.	1
THE PORT PROCESSOR CHAIN WOULD NOT EXECUTE The port processor could not read the LMID.	2, 1, 3/4
ERROR WHILE RE-SELECTING ORIGINAL TARGET/LUN During the select test, bad status was received during attempt to re-select specified target/L.U.N.	2, 1, 3/4

Error Message Description	Isolation Order for 00036
ADVISORY - ERROR READING VOLUME LABEL Failure occurred during attempt to read volume label in logical block #1 to determine if media is diagnostic or Telcon software. Usually indicates that media is not formatted or has non-standard format.	-
A DATA COMPARE ERROR OCCURRED CHARACTER NUMBER = ERROR CODE = A discrepancy was found during a compare of the data buffers in write/read test. The character number specifies the position (offset) of the character in the buffer.	3/4
PP DID NOT COMPLETE IN SPECIFIED TIME. Command or data transfer did not complete in allotted time. See command or data transfer status to determine type of error. Use re-try option first.	1
CONTROLLER DID NOT DETECT INVALID DRIVE Test-Unit-Ready issued to L.U.N. (drive) in upper byte of target/L.U.N. display did not return bad status.	2, 1
SELECTED DRIVE SIZE IS NON-STANDARD If there were no logical blocks displayed for the indicated track, check that the media is formatted. Re-enter parameter.	-
SELECTED L.U.N. (DRIVE) IS NOT PRESENT The L.U.N. is not configured or cannot respond. Re-enter the parameter for the L.U.N.	-
ERROR DETECTED ON SEEK TO LAST VALID LOGICAL BLOCK XXXXXXXX Seek was done to the highest logical block (according to inquiry data returned) and an error was reported. Drive should be reformatted.	3/4
ERROR NOT DETECTED ON SEEK TO INVALID LOGICAL BLOCK Error induced by diagnostic was not reported.	3/4

11. U10 MAGNETIC TAPE DIAGNOSTIC TEST

11.1. Introduction

The U10 magnetic tape diagnostic test checks the major functions of the SPERRY U10 Magnetic Tape Subsystem Type 0871 (F2721).

11.2. General Information

When errors occur, the error information includes the interrupt status bits and the sense status bits returned by the tape controller. The bit numbering system for the controller status identifies bit 0 as the least significant bit (LSB); however, the display on the maintenance panel has register content in bits 16 through 31 with bit 31 as the LSB.

Figure 11-1 relates the tape controller status bits to the maintenance panel bits. Figure 11-2 provides the same information for the sense status bits.

The two matrices that follow the figures give the bit settings of the interrupt status word when the completion status is abnormal and when it is normal.

Status Bits	Description (if Set)	Panel Bits
15 (MSB)	Abnormal completion	16 (MSB)
14	Mode 0 = PE; 1 = NRZI	17
13	Write protected	18
12	BOT detected	19
11	EOT detected	20
10	MTU rewinding	21
9	MTU online	22
8	MTU ready	23
7	Command reject	24
6	Device end	25
5	File mark detected	26
4	Unit check/Not ready	27
3	Record Incomplete	28
2	Corrected error	29
1	MTU 1 selected	30
0	MTU 0 selected	31

Figure 11-1. Magnetic Tape Controller Status Bits

Sense Bits	Description (If Set)	Panel Bits
	Sense Word 0 Status	
15 (MSB)	Drive selected	16 (MSB)
14	Format	17
13	Tape runaway	18
12	Reverse motion fault	19
11	Not used (Zero)	20
10	Skew error	21
9	Overrun or underrun	22
8	Not used (Zero)	23
7	Not used (Zero)	24
6	No byte count	25
5	Noise detected	26
4	Not used (Zero)	27
3	Not used (Zero)	28
2	Not used (Zero)	29
1	Not used (Zero)	30
0	Not used (Zero)	31
	Sense Word 1 Status	
15-1	Residual byte count	16-31

Figure 11-2. Magnetic Tape Controller Sense Bits

Interrupt Status Word - Abnormal Completion

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Error
	ABNORMAL COMPL	MODE (1) NRZI (2) PE	FILE PROTECT	BOT	EOT	REWINDING	ONLINE	READY	COMMAND REJECT	DEVICE END	FILE MARK DETECT	UNIT CHECK	RECORD INCOMPL	CORRECTED ERROR	UNIT 1 SELECT	UNIT 2 SELECT	
1	X	X	1	0	0	1	1	0	0	0	0	X	X	S	S	Reverse Motion Fault
1	X	X	X	X	X	X	X	1	0	0	X	X	0	S	S	Command Reject
1	X	X	0	X	0	1	1	0	0	1	0	X	0	S	S	File Mark Detected/ Read or Space Block
1	X	X	0	X	0	1	1	0	0	0	X	X	0	S	S	Tape Runaway
1	X	X	X	X	0	1	1	0	0	0	0	X	X	S	S	Parity Error
1	1	X	X	X	0	1	1	0	0	0	0	X	0	S	S	Format Error
1	0	X	X	X	0	1	1	0	0	0	0	X	X	S	S	Skew Error
1	X	X	X	X	0	1	1	0	0	0	0	X	X	S	S	Overrun/Underrun
1	X	0	X	X	0	1	1	1	0	0	0	0	0	S	S	Zero Byte Count with Write Command
1	X	X	X	X	0	1	1	0	0	0	0	X	X	S	S	Noise Detected
1	X	X	0	1	0	1	1	0	0	X	0	X	X	S	S	EOT Marker Detected
1	X	X	X	X	0	X	X	1	0	0	1	0	0	S	S	Unit Check
1	0	0	0	X	0	1	1	0	0	0	0	0	1	S	S	Corrected Error During Write
1	X	X	X	X	0	1	1	0	0	0	0	1	X	S	S	Read Byte Count Exceeds Block Length
1	X	X	X	X	X	X	X	X	1	X	0	X	X	S	S	I/O Channel Parity Error

Legend: 0 = Bit 0 set
1 = Bit 1 set
X = Bit is 1 or 0 depending on operation
S = Bit 14 or bit 15 is 1 depending on drive selected

Interrupt Status Word - Normal Completion

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Command
0	X	X	0	0	1	1	0	0	1	0	0	0	0	S	S	Rewind
0	X	X	1	0	0	1	1	0	0	0	0	0	0	S	S	Rewind Complete
0	0	0	0	0	0	0	0	0	1	0	0	0	0	S	S	Rewind w/Interlock
0	X	X	0	0	0	1	1	0	1	0	0	X	X	S	S	Read Forward
0	X	X	0	X	0	1	1	0	1	0	0	X	X	S	S	Read Reverse
0	X	X	0	0	0	1	1	0	0	0	0	0	0	S	S	Forward Space Block
0	X	X	0	X	0	1	1	0	1	0	0	0	0	S	S	Reverse Space Block
0	X	X	0	0	0	1	1	0	1	1	0	0	0	S	S	Forward Space File
0	X	X	0	X	0	1	1	0	1	1	0	0	0	S	S	Reverse Space File
0	X	0	0	X	0	1	1	0	1	0	0	0	0	S	S	Write
0	X	0	0	X	0	1	1	0	1	0	0	0	0	S	S	Erase
0	X	0	0	X	0	1	1	0	1	1	0	0	0	S	S	Write File Mark
X	X	X	X	X	X	X	X	0	X	0	X	0	0	S	S	Sense
0	X	X	X	X	X	X	X	0	1	X	X	0	0	S	S	Status
0	0	0	X	X	0	1	1	0	0	0	0	0	0	S	S	Online

Legend: 0 = Bit 0 set
1 = Bit 1 set
X = Bit is 1 or 0 depending on operation
S = Bit 14 or bit 15 is 1 depending on drive selected

11.3. Test Procedure

CAUTION

Use scratch tapes throughout this test. Data is written on the tape, erasing any previous data.

NOTES

Perform the parallel line module micro-diagnostics and macrodiagnostics before running this diagnostic test.

Pressing the F2 key starts the program at the disk number request. Pressing the F3 key starts the program at the test selection.

The tape write ring can be removed for any of the tests to checkout the write-protect function.

A master-clear function is done at the beginning of each test and a set-mode function is done at the beginning of most of the tests. These functions rewind the tape to the beginning of tape (BOT) and write a file mark.

When the U10 magnetic tape diagnostic test is selected from the system menu, the console displays a series of prompts which request the configuration and execution parameters of the test.

```
CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - 5.1
      U10 MAGNETIC TAPE (T0871 :F2721)


**** MOUNT SCRATCH TAPE WITH WRITE RING ****
>PRESS TRANSMIT TO CONTINUE
```

1. Install the scratch tape in the drive, set the tape unit online, and press TRANSMIT key.

```
>ENTER THE PORT NUMBER ( IN HEX )
>[]
```

2. Enter the port number of the parallel line module for the magnetic tape unit (MTU). The program tests the line module ID (LMID) for that port, and if it is the correct port and will initialize, the screen displays the LMID and the port number on fixed line 4.

```
LM I.D.=  0010          PORT = XXXX
```

```
>ENTER THE NUMBER OF DRIVE TO BE TESTED (0, 1 or B, D=0)
>[]
```

3. Enter the number of the drive (0 or 1). The B selection tests both drives. The default is drive 0 (the first drive).

```
>ENTER CYCLE COUNT (1-9999,I=INFINITE,D=1)
>[]
```

4. Enter the number of times each test will run and press the TRANSMIT key. The next display is the U10 test list.

CPA FAMILY DIAGNOSTIC ROUTINES. RELEASE - 5.1
U10 MAGNETIC TAPE (T0871 :F2721)

```
U-10 TAPE DIAGNOSTIC TEST LIST
>1 - INDIVIDUAL FUNCTIONS
>2 - WRITE/READ DATA PATH
>[]
```

5. To test the capability of the MTU to perform various functions, select item 1. To test the write/read data path, select item 2.

   The individual functions test provides 14 subtests:

   1. READ STATUS
   2. READ SENSE
   3. BASIC COMMANDS
   4. SET MODE
   5. WRITE/READ
   6. WRITE FILEMARK
   7. MASTER CLEAR
   8. REWIND/W/ILOCK
   9. READ REV. DATA
   10. FWD. SP. BLK.
   11. REV. SP. BLK.
   12. FWD. SP. FILE
   13. REV. SP. FILE
   14. ERASE

Following selection of a subtest, the screen displays a test number on fixed-line 5.

```
TEST IN PROGRESS XXXX
```

The first digit is the test number. The third and fourth digits are the subtest number. For example, 1002 is test 1, subtest 2.

When the subtest completes, the console displays the number of completed cycles (in hexadecimal) on fixed-line 6 and the number of errors on fixed-line 7. At the beginning of each subtest, the cycle count and error count are zeroed.

11.4. Error Reporting

The console reports errors occurring during parameterization as error messages. The error messages are summarized as follows:

CHANNEL WILL NOT INITIALIZE

Parallel line module is not present for selected channel or it cannot communicate with the CLC.

THE CHANNEL NUMBER IS NOT WITHIN LEGAL RANGE

The selection was either less that 0 or greater than 255 (XFF). Enter correct value.

USE OF THE CONSOLE CHANNEL IS INVALID

The selected channel is the console port. Re-enter port selection.

USE OF THE LOADER CHANNEL IS ILLEGAL

The selected channel is the integrated diskette drive port. Enter another selection.

THE PORT PROCESSOR CHAIN WOULD NOT EXECUTE

The port processor chain-completion flag was not set.

THIS LM TYPE MAY NOT BE USED WITH THIS DIAGNOSTIC

The LMID is not correct for the parallel port where the magnetic tape unit is connected. Re-enter LMID.

Test errors are displayed in the format:

ERROR CODE XXXX

The first and second digits from the left identify the test and subtest; the third and fourth digits provide the error number.

Example:

ERROR CODE 1401

14 = test 1, subtest 4
01 = error 1 within the subtest

11.4.1. Individual Test Descriptions and Error Information

The descriptions that follow explain each subtest and the error code or codes associated with it. The fourteen subtests of test one are presented first.

1. Read Status

   After the master clear function completes, the subtest checks the following status: BOT, online, ready, file mark detected, drive 0 or 1 detected.

   ERROR CODE 1101 = Bad status received: status of drive 1 should be 1341.

2. Read Sense

   The subtest writes a block with a zero byte count of 'AAAA' data and then reads the sense data. Following master clear, the MTU writes a block of data with a zero byte count of 'AAAA' data.

   ERROR CODE 1201 = No abnormal completion after write block.

   ERROR CODE 1202 = No abnormal completion after read sense data.

   ERROR CODE 1203 = Sense data was not correct: sense word should be 0040

3. Basic Commands

   The subtest requests the mode, P.E. or NRZI, writes a corresponding file mark, checks the file mark status, and then rewinds the tape to BOT and checks status.

4. Set Mode

   The subtest writes a file mark in P.E. mode, checks status, and rewinds. It performs the same actions in NRZI mode and then repeats the activity in P.E. mode.

5. Write/Read Data

   The subtest requests the mode, P.E. or NRZI, and then writes three blocks of different data. It then reads the blocks, rewinds the tape, checks status, and verifies the data.

   ERROR CODE 1501 = Data error on first block: should be 5555.

   ERROR CODE 1502 = Data error on second block: should be AAAA.

   ERROR CODE 1503 = Data error on third block: should be 0000.

6. Write File Mark

The subtest requests the mode, P.E. or NRZI, and then writes a file mark and one block of data (AAAA), rewrites a file mark, and rewinds the tape. Next, it reads the file mark and the data, and rewinds the tape. The functions are performed again using two blocks of data.

ERROR CODE 1601 = Read file mark did not cause abnormal completion.

ERROR CODE 1602 = Bad status on reading first file mark.

ERROR CODE 1603 = Data error on reading first data block.

ERROR CODE 1604 = Data error on reading second data block.

ERROR CODE 1605 = Read file mark did not cause abnormal completion.

ERROR CODE 1606 = Bad status on reading file mark.

7. Master Clear

The subtest requests the mode, P.E. or NRZI, and then writes one block of data, attempts to write another block of data with one word over buffer size, performs a master clear, and then reads the status.

ERROR CODE 1701 = Oversize block did not cause abnormal completion.

ERROR CODE 1702 = Bad status after writing oversize block.

ERROR CODE 1703 = Abnormal completion status after master clear.

ERROR CODE 1704 = Bad status after master clear.

8. Rewind with Interlock

The subtest requests the mode, P.E. or NRZI, and then writes a file mark and five blocks of data, rewinds with interlock, and checks status. It then requests that the tape drive be placed online and checks status again.

ERROR CODE 1801 = Abnormal completion of rewind with interlock.

ERROR CODE 1802 = Bad status after rewind with interlock.

ERROR CODE 1803 = Bad status after tape drive is online.

9. Read Reverse

The subtest requests the mode, P.E. or NRZI, writes a file mark and one block of data, and then reads the block in reverse and verifies the data.

ERROR CODE 1901 = Abnormal completion of reverse read.

ERROR CODE 1902 = Data error on reverse read.

10. Forward Space Block

The subtest requests the mode, P.E. or NRZI, writes a file mark and two blocks of data, rewinds and advances one block, and then reads the second block.

ERROR CODE 1A01 = Abnormal completion of advance block.

ERROR CODE 1A02 = Bad status after advance block.

ERROR CODE 1A03 = Data error in second block.

11. Reverse Space Block

The subtest requests the mode, P.E. or NRZI, writes a file mark and two blocks of data, reverses one block, and then reads forward one block.

ERROR CODE 1B01 = Abnormal completion of reverse block.

ERROR CODE 1B02 = Bad status after reverse block.

ERROR CODE 1B03 = Data error on forward read.

12. Forward Space File

The subtest requests the mode, P.E. or NRZI, writes a file mark, one block of data and another file mark, writes another block of data and a file mark, rewinds and advances a file, and then performs a forward read of second file.

ERROR CODE 1C01 = Abnormal completion of forward space file.

ERROR CODE 1C02 = Bad status on forward space file.

ERROR CODE 1C03 = Data error on second file.

13. Reverse Space File

The subtest requests the mode, P.E. or NRZI, writes a file mark, one block of data and another file mark, and then repeats the process two more times. It reverses two files, advances one file, and does a forward read of the second file.

ERROR CODE 1D01 = Abnormal completion of reverse space file on first file.

ERROR CODE 1D02 = Bad status on reverse space file on first file.

ERROR CODE 1D03 = Abnormal completion of reverse space file on second file.

ERROR CODE 1D04 = Bad status on reverse space file on second file.

ERROR CODE 1D05 = Abnormal completion of advance file.

ERROR CODE 1D06 = Bad status on advance file.

ERROR CODE 1D07 = Data error in second file.

14. Erase

The subtest requests the mode, P.E. or NRZI, writes a file mark and one block of data, reads the block in reverse, erases one block, and then reads in reverse and checks status.

ERROR CODE 1E01 = Abnormal completion of reverse read.

ERROR CODE 1E02 = Data error on reverse read of file.

ERROR CODE 1E03 = Abnormal completion of erase.

ERROR CODE 1E04 = Bad status on erase.

ERROR CODE 1E05 = No abnormal completion after reverse read of erased block.

ERROR CODE 1E06 = Bad status on reverse read of erased block.

Test two has one subtest:

1. Write/Read Data Path

   The subtest requests the mode, P.E. or NRZI, writes a file mark and one block of data, and reads the data in reverse. Next it performs a forward space block, writes one block of data followed by a reverse space block, and reads forward one block. It then writes ten blocks of data with a file mark after each block, reads reverse space file for seven files, reads forward four files, and performs a forward read of the file. It repeats the whole process and when the end of tape (EOT) is reached, the file rewinds and continues.

   ERROR CODES 2101 thru 2107 = Bad status on reverse read of files.

   ERROR CODES 2108 thru 2111 = Bad status on forward read of files.

   ERROR CODE 2112 = Data error in forward read of block.

11.4.2. Common Error Codes

Several error codes are common to all of the subtests. They are summarized in the following list.

Error Code	Description
XX0X	Master clear error: XX00 = Incorrect status. XX01 = Tape drive did not rewind.
XX4X	Rewind error: XX40 = Rewind command has abnormal completion status. XX41 = Abnormal status after rewind command. XX42 = Tape is not at BOT.
XX5X	Set-mode function error: XX50 = Abnormal completion of write file mark within set-mode function. XX51 = Incorrect status on file mark within set-mode function.
XX70	Bad status with write-data function.
XX72	Bad status with read-data function.
XX74	Bad status with write file mark outside of set-mode function.

12. HOST CHANNEL INTERFACE DIAGNOSTIC TEST

12.1. Introduction

The host channel interface diagnostic test checks the operation of the byte channel (SU00039) or the block mux (SU00208) interface between the DCP and Series 90/Series 1100 hosts. The test verifies that the DCP front-end processor can functionally communicate with the host. The following diagnostic programs must be installed in the host:

Series 1100: PTS
Series 90: ONCOMM

The program performs the testing in the host processor: no checks occur in the DCP. The function of the DCP is to receive the data and to return it to the host.

12.2. Test Description

When the line module port number is entered, the program compares it with the line module ID (LMID). If the LMID does not equal 04 (SU00039 interface) or 014 (SU00208 interface), the console reports an error along with the options of leaving the test, or retrying with a new port number.

If the LMID is correct, the console displays the interface type. The test then requests that the loader program retrieve the appropriate microcode from the load device. If the load does not complete, the console displays an error message.

The microcode is loaded into the line module in 4K byte blocks. The microcode ID defines the microcode status of the line module. The status codes are:

ID = 00: The microcode has not loaded.
ID = 0EF: The microcode has loaded but is not operational (requires a command).
ID = 058: The SU00039 microcode is operational.
ID = 048: The SU00208 microcode is operational.

Once the microcode loads and the line module and is operational, the two device addresses (solicited from the operator) are loaded into the line module, and a command is issued to set the line module online to the host. The operator is asked what type of buffer to use (large or small), and then is asked what type of data to place in the buffer. This data does not have to be the same as the host data sent via PTS/ONCOMM, since the data checking is performed only in the host. If the host program solicits data from the DCP first, then this is what will be sent to the host for checking input.

The test informs the operator when the first data transfer has occurred. Thereafter, data is transferred to and from the DCP, using it as a turn-around program. Data is checked on the return from the host.

12.3. Test Procedure

All paramaterization for the DCP side of the test is performed through the console. If an error occurs while setting up the loopback (for example, turning on the port processor), then the operator is informed and is given a choice of aborting the program or restarting it.

Parameter requests occasionally provide default values. Select the default by pressing the TRANSMIT key. All entries are in hexadecimal unless specifically labeled otherwise.

The first display that appears on the console is:

```
CPA FAMILY DIAGNOSTICS ROUTINES.  RELEASE - R5.1
 HOST CHANNEL INTERFACE (SU00039/SU00208) TEST


>ENTER DESIRED PORT (In hexadecimal - 0-FF, D=0)
>[]
```

1. Enter port number in hexadecimal: for example, if the line module is connected to the 13th port of the second CLC, then the entry is 1D.

```
>Enter Input (to DCP) DEVICE ADDRESS in Hexadecimal (00-FF)
>[]
```

2. Enter the value for the input device address. This value is loaded into the line module and sent to the host in response to the host enquiry. The input device address is ODD and is usually the number of the input port.

```
>Enter Output (To Host) DEVICE ADDRESS in Hexadecimal (00-FF)
>[]
```

3. Enter the value for the output device ddress. Th value must be an even number and is usually (but not necessarily) the number of the output port.

   When steps 2 and 3 are completed, one of the following messages appears toward the top of the screen:

```
>ID=04 - SU00039 Host Interface (Primary Port)
or
>L.M. ID = 14 - SU00208 Host Interface (Primary Port)
```

   When the microcode load and initialization completes, the line module is set online to the channel.

```
>Enter buffer data (0 -0FFFF), Default is 0
>[]
```

4. Enter the desired data pattern. The pattern is placed in the data buffer that is sent to the host. It is not intended for data comparison within the DCP; however, for purposes of data parity during the transfer, it should be the same as the pattern that is set in the host.

```
>Buffer Size, (0=small, 1= Large, D=1)
>[]
```

5. The default is a large buffer of 4K bytes. The small buffer is 128 bytes in length. Note that the same size buffer must be used in the host.

During the diagnostic, two information messages are displayed:

```
>PROGRAM IS CYCLING WAITING FOR A COMMAND FROM THE HOST
```

This message appears in the top portion of the screen when the line module is online and waiting for instructions from the host.

```
>FIRST INPUT COMPLETED
```

This message is sent when the DCP has returned the first input buffer to the host.

12.4. Error Recovery

When an error is detected by the program, it is reported to the console in the form of a message in the lower part of the screen. The current program activity is reported in the upper half of the screen so that the operator may know what is going on at any time. These messages occasionally are displayed during execution at a faster pace than they can be read. This is not a problem since the only time they become significant is when an error is reported in the lower half of the console screen.

Once the message has been read, and the program action is known, pressing the TRANSMIT key provides the operator with a choice of options:

```
>WHAT DO YOU WANT TO DO (DEFAULT = 1)
<RETURN TO EXEC (0), OR RESTART THE TEST (1)?
>[]
```

12.5. Stopping the Test During Execution

Use one of the following methods to stop the test in mid-execution:

1. Perform the FUNCTION key 1 procedure explained in paragraph 2.1.

2. Function key 2: If a mistake is made during parameterization, press this key to begin again.

3. Function key 3: Once the test is online to the host, the only way to stop it is to press Function key 3.

NOTE

Press Function key 1 to exit the test.

12.6. Error Reporting

All errors are reported to the console. There are no error codes given. Instead, the current activity is displayed in the upper portion of the console screen, and the error itself is displayed in the lower part of the screen.

The errors messages that follow are grouped under each activity performed by the test. Find the activity listed and then the error message that is displayed.

12.6.1. Build Port Processor Parameters

Error messages for this activity are:

I DON'T UNDERSTAND THAT

The input sent to the console has been translated by the translate program which found an error in the input data. The data could have been corrupted almost anywhere between the console and the translate program. If this error occurs, then there was either a hit on the console line, or the data was corrupted in the host (use the microdiagnostics), or the input was accidentally changed by the operator. Rerun the program and if the error occurs again, then execute the microdiagnostics on the DCP/40 and DCP/20, followed by the local storage diagnostic (on all machines).

DESIRED PORT CONFLICTS WITH THE CONSOLE PORT.

The operator has inadvertantly selected the port used by the console. Enter the correct parameter.

DESIRED PORT CONFLICTS WITH THE LOAD DEVICE.

The operator has inadvertantly selected the port used by the loader. Enter the correct parameter.

12.6.2. Initializing the Port Processor (Hexadecimal) XX

Error messages in this category are:

MEMORY MANAGEMENT EXCEPTION ERROR

The program requests two 4K byte blocks of storage from memory management while initializing the port processor. If an error occurs, one of the following messages will follow this one.

REQUEST FOR 4K OF STORAGE DENIED

The memory management procedure would not provide 4K of storage to the test. The reason for this is reported in the returned status documented after the next display.

STATUS RETURNED INDICATES PARAMETER INTERFERENCE

The memory management procedure is indicating that the parameters received had an error in them. Since the parameters were error free when loaded into local storage, they must have been changed during the passing process.

Probable cause of error is either a local storage problem or an address bus problem.

RETURNED STATUS:

The value (in hexadecimal) at the end of the statement indicates the returned status. The possible bit settings and their meanings are:

XXXXX1 = Execution complete, no errors occurred.

XXXX1X = No storage available, or general segment table full.

XXX1XX = Block to be freed not found (should not be set).

XX1XXX = GSN to be freed is not a valid value.

X1XXXX = Permanent storage requested (program does not request permanent storage).

1XXXXX = Subsegment only needs 128 bytes. More than 128 bytes requested. This error should not be found. It indicates that the parameters were interferred with during the passing phase.

THE PORT PROCESSOR WILL NOT INITIALIZE

The port number given by the operator would not intialize with its accompanying program. If this error occurs, then one of the following items may have caused the failure:

THE RESPONSE BIT (R BIT) WAS NOT SET BY MICROCODE

The microcode thinks that there is no line module in the port that the program is accessing. Refer to the next error message for further clarification.

THE PP DID NOT BECOME ACTIVE (A BIT WAS NOT SET)

The PP program was not started by the microcode. Possible causes are:

1. Microcode could not find a line module in the designated port.

2. The line module is not working correctly and should be replaced.

3. The line module is not correctly strapped on the front or the back plane.

4. The wrong port was called for initialization. Note that there are three PCAs in the line module. The only port that the microcode can initialize as the port processor is the port containing the primary port interface.

LOAD SEGMENT DESCRIPTOR PROCEDURE ERROR
or
ERROR DURING SEGMENT DESCRIPTOR BUILD

A problem exists with the segment descriptor paramater passed to the initialization routine. Either the memory management procedure passed an illegal parameter, or the parameter was interferred with during its passage between the test and the initialization procedures.

UNRECOGNIZABLE STATUS

The status returned by the initialization routine could not be recognized by the test. This error is a prime indication of parameter interference.

12.6.3. Assign Device Addresses for Host Loopback

The error message associated with this command is:

I DON'T UNDERSTAND THAT

An error occurred in one of the following places:

1. Entering the device address at the console

2. Transmission from the console to the waiting procedure

3. Interference during passage between procedures

Retry the function. If the same error occurs, then perform one of the following actions:

1. If item 1 or 2 appear to be the cause the problem, then reboot the diagnostic executive using another console port (and a different terminal as a console).

2. If step 1 fails, item 3 is the probable cause of the problem, and the source is in one or more of the following areas:

   a. Address bus
   b. WAR register
   c. Local storage PCA (where program is executing)
   d. Local storage addressing/timing
   e. Data bus
   f. Emulation registers

3. To further isolate the problem in the DCP/40/20, run the microdiagnostics. In the DCP/10/10A/15, replace the processor PCA.

12.6.4. Fetch and Verify the Line Module ID

Error messages associated with this activity are:

NO RESPONSE FROM PORT AFTER 2 SECONDS FOR ID READ

The line module is not working correctly, replace it.

INVALID LINE MODULE ID RECEIVED IN PORT: XX
LINE MODULE ID IS: XX

The LMID was not recognized by the program. It must be either 04, (SU00039) or 014 (SU00208). If it was neither of these, perform the following steps:

1. Check the line module to ensure that it is the correct one.

2. Check the port slots to ensure that you are entering the correct port number.

3. If neither of the above steps solves the problem, do one of the following:

   a. Replace the line module and start again.

b. Run the appropriate test for one of the other line module types in the same CLC (or card rack) as the channel interface line module (and in the same half of the card rack (ports 0-7 or 8-15). If the LMID is reported correctly, then change the byte interface line module. The card rack backplane (L-bus) is the next likely suspect.

12.6.5. Fetch Microcode ID from the Line Module and Verify It

The program is attempting to read the microcode ID from the line module. Several codes can be returned, all of which are valid. If the line module is not working correctly, a time-out occurs. The error message is:

NO RESPONSE FROM PORT AFTER 2 SECONDS FOR I.D. READ

The probable cause is one the following conditions:

1. The line module is not working correctly. Replace it.

2. The timing chains for the L-bus are not working correctly. Change CLC timing or L-bus PCA.

Note that the microcode ID is read several times during initiation to verify each step that is performed. The valid IDs are:

00 = There is no microcode in the line module.

0EF = Microcode is loaded but has not been activated (started).

058 = Microcode is active (SU00039).

048 = Microcode ia active (SU00208).

12.6.6. Activate the Microcode in the Line Module

The command to go online is given to the line module. The resulting code should be either 058 or 048. The possible error message is:

TIME-OUT WHILE ACTIVATING MICROCODE IN LINE MODULE

The online instruction was sent to the line module, but the load instruction did not complete (or the port processor did not recognize the command).

12.6.7. Fetch Microcode from Load Source

A request is made to the loader procedure to load the microcode into local storage so that the program can transfer it to the line module. If there is an error during the load, the loader procedure reports it and then returns to the test. The diagnostic checks the error completion code and issues this statement:

MICROCODE NOT LOADED FROM LOAD SOURCE
LINE MODULE DID NOT LOAD THE MICROCODE

Check the loader report for reasons why the code was not loaded.

12.6.8. Load Microcode into the Line Module

The program is about to load the microcode from local storage into the line module in 4K byte blocks. The only check at this time is the absence of a time-out during the load of each block. If there is something wrong with the load, it surfaces when the microcode ID is retrieved from the line module. If a time-out occurs, the following message is displayed.

ERROR REPORT: TIME-OUT WHILE LOADING THE MICROCODE

12.6.9. Load Device Address into the Line Module

The device addresses, which were requested at the begining of paramaterization process, are now loaded into the line module. The only possible error at this time is a time-out while waiting for return status from the port processor.

TIME-OUT WHILE LOADING DEVICE ADDRESSES

The test waits two seconds for the port processor to set the "complete" flag, indicating that it has completed the action. The flag was not set so the port processor timed out while executing the instruction.

12.6.10. Set the Line Module Online

The line module and its microcode are ready to begin execution. The test tells the port processor to set the line module online by sending a command to the line module. If an error occurs, the possible error messages are:

TIME-OUT SETTING ONLINE

The port processor did not set the "complete" flag within two seconds, indicating that it timed out (hung) while trying to load the online command into the line module (or the line module timed out while accepting and executing the command).

LINE MODULE COULD NOT BE SET ONLINE.

The line module successfully completed the command to go online, and the port processor set the "complete" flag. When the status was retrieved from the line module, it indicated that the line module did not actually go online.

12.7. Online Execution Errors

These errors can occur once the line module is set online and is establishing communication with the host. Note that the console displays a message when the first transfer completes successfully; consequently, you can tell whether the errors occurred during the establishment of communication, or after the first transaction has taken place.

The list that follows summarizes the online execution error messages. Refer to Appendix A for the isolation procedure associated with the error.

Error Message Description	Isolation Procedure
INPUT - No Buffer available The input command terminated because no buffer was available to hold the input data.	00029
INPUT ERROR - Parity error on input The input command terminated with a parity error.	00030
INPUT ERROR - Overflow error The input command terminated with an overflow condition: for example, the line module could not transfer enough data to memory to stop the overlay of at least one input byte by another coming in from the channel behind it.	00030
INPUT - Offline error detected The input command terminated in an offline condition.	00031
INPUT LIMIT - The buffer is full The input command terminated because the limit specified for the input buffer (128 bytes/4K) was exceeded.	00031
INPUT TIMEOUT - No data transferred The input channel terminated with an input time-out on the channel.	00030
INPUT ERROR - System reset error detected The input command was terminated in a selective reset.	00032
INPUT ERROR - Selective reset error detected The input command was terminated in a selective reset from the host.	00032
INPUT ERROR - Interface disconnect The input command terminated because an interface disconnect was received from the channel.	00032

Error Message Description	Isolation Procedure
INPUT ERROR - No Command The input command terminated because no command was received from the host.	00032
INPUT DATA - Lost Data The input command terminated because data was lost on the channel.	00032
O/P TIMEOUT - No Data transferred The output command terminated with an output time-out.	00032
OUTPUT ERROR - Lost Data The output command terminated because data was lost on the channel.	00032
OUTPUT ERROR - Offline operation The output command terminated becuase an illegal offline operation occurred.	00032
OUTPUT ERROR - System Reset The output command terminated with a system reset command.	00032
OUTPUT ERROR - Selective Reset The output command terminated with a selective reset command.	00032
OUTPUT ERROR - Interface Disconnect The output command terminated because an interface disconnect was received from the channel.	00032
OUTPUT ERROR - No Command The output command terminated because no command was received from the host.	00032
SYSTEM RESET/ATTENTION FAILED STATUS ERROR The channel state byte indicated a system reset, or the attention-failed bit was set and was not expected.	00032

13. RCM/LSM TEST

13.1. Introduction

The remote control module/line switch module (RCM/LSM) test is a design verification routine (DVR) which checks the hardware from the DPC/40 processor. The DVR uses three diskettes:

DR2558-4: RCM/LSM Diagnostic Loader
DR2558-5: RCM/LSM Diagnostics
DR2558-6: RCM/LSM Contention Tests

In addition, either a parallel or serial console can be used for parameterization and error reporting.

13.2 Test Procedure

To load and run the diagnostics, proceed as follows:

1. Place the loader diskette (DR2558-4) in the integrated diskette drive and close the door.

2. Disable all switches on the maintenance panel, including the panel disable switch.

3. Enter the CLC number for the console in the first four switches of the top cap (7-4) and its port number in the lower four switches (3-0).

4. Press the SYSTEM RESET button located on the top cap. The system loads the diagnostic from the integrated diskette drive. Verify that the red busy light located on the drive door is illuminated.

5. After about 1 minute, the processor run light goes off. Enable the panel enable switch (up position). The display register displays the current stop address (0B08) in its lower half. The upper half contains the last address processed.

6. Remove the loader diskette and replace it with the diagnostic diskette (DR2558-5).

7. Enable JUMP STOP KEY 1 on the maintenance panel and press the processor START button. The processor run light goes on as the program loads. (Check the busy light again.)

8. After a short time the processor stops at address X07A00. Remove the diagnostic diskette (DR2558-5) and replace it with the loader diskette (DR2558-4). Press the CP START button on the CP maintenance panel. After a short time, a display appears on the console.

13.2.1. Parameterization

The console screen displays a list of parameters under the title PARAMETERIZATION.

1. To change any of the parameters, use the cursor direction keys on the console keyboard. The change can be placed over the default parameter or to the right of it, next to the edge of the screen. A zero normally implies no enable, while one (1) implies that the particular parameter is enabled. The exception to this is the parameter that specifies an address or a numeric value such as a port number.

2. The console displays the following parameter prompts:

   CONTINUE ON ERROR (default = 0)

   If an error is encountered, the program continues but logs the error on the console.

   BACKGROUND MODE (default = 0)

   This parameter is disabled. Do not change it.

   NUMBER OF CYCLES (default = continuous running)

   Enter the number of test cycles (in hexadecimal) by changing this number.

   PRIMARY PORT CLC HARDWARE NUMBER (default = CLC#0)

   Enter the number of the CLC to which the RCM/LSM is attached.

   IFDC PORT # (default = 0C)

   Change this parameter if necessary to the actual port number of the IFDC (integrated diskette drive).

   ACU (default = 0)

   Do not enable this parameter. It is reserved for implementation of a future option.

13.3. RCM/LSM Tests

There are six tests on the menu. None of them are enabled. Enter 1 in place of the disabling 0 to select a test. You can select from one to six tests at a time. The tests run consecutively.

The following tests are available:

- RCM commands

  The test sends the following basic commands to the RCM:

  1. Power up all processors.
  2. Set all load paths to 0.
  3. System reset all processors.
  4. Power down all processors.

  The test begins when the fourth command is sent. If no response is received from the RCM within 15 seconds, a re-try is issued.

- LSM commands (all switches)

  This test sends the basic commands to the LSM for execution. First, it sets all the odd-numbered switches and, then, it resets them, requesting status each time. It then repeats the test for the even-numbered group.

- LSM commands (select switches)

  This test sets and resets each switch beginning with the starting switch specified in the parameters and ending with the final switch.

- Invalid commands to the RCM/LSM

  This test checks for the correct responses to a set of invalid commands sent to the RCM/LSM. Note that the test will run in full-duplex mode only.

- Modem expander test

  This test asks the user for the device address and the type number. It then calls either test 1 for the RCM or test 3 for the LSM.

- User-generated messages

  This test allows the user to compose messages. After the message has been built by the user, the test transmits it to either the RCM or LSM as requested and displays the responses on the console. Except for special purposes, use the default values instead of trying to compose messages.

13.4. Test Procedure

1. The following parameters are displayed when test 1 is selected:

```
HALF OR FULL DUPLEX (0=FULL, 1=HALF).....0
(Select the appropriate transmission mode.)

WAIT FOR DCPS TO POWER UP (0=NO, 1=YES).....0

DEVICE ADDRESS (HEX).....66 66 96
(If necessary, change this to the appropriate address by
placing the change after the default value.)

MESSAGES TO SEND TO THE RCM (0=NO, 1=YES)

MESG1-ACCEPT PORT COMMANDS.....1
MESG2-SEND PORT COMMANDS.....1
MESG3-READ STATUS.....1
MESG4-SWITCH PORT STATES.....1
ESG5-READ STATUS.....1
MESG6-RECEIVE NOT READY/RECEIVE READY.....1
MESG7-ACCEPT PORT COMMANDS.....1
MESG8-SEND STORED PORT COMMANDS.....1
MESG9-SWITCH PORT COMMANDS.....1
MESG10-SEND STATUS.....1
MESG11-RECEIVE NOT READY/RECEIVE READY.....1
MESG12-DISCONNECT.....1
```

   The test performs more efficiently if the messages are not disabled.

2. When test 2 is selected, the console displays the following parameters:

```
HALF OR FULL DUPLEX (0=FULL, 1=HALF).....0

DEVICE INDEX.....66 66 96
(These parameters are the same as test 1.)
```

3. The parameters for test 3 are:

```
HALF OR FULL DUPLEX (0=FULL, 1=HALF).....0
DEVICE INDEX.....66 66 96
(These parameters are the same as test 1 and test 2.)

NUMBER OF SWITCH TO START WITH (0-7F).....0
NUMBER OF LAST SWITCH TO TEST (0-7F).....7F
DEVICE ADDRESS.....66 66 96
(The numbers must be entered in hexadecimal.)
```

4. The parameters for test 4 are the same as test 2.

5. The parameters for test 5 are:

NUMBER OF DEVICES TO TEST (1-4).....1

When the number of devices is entered, the test replies by asking for information about each of the devices:

```
DEVICE #1
DEVICE ADDRESS
   BYTE #1.....66
   BYTE #2.....66
   BYTE #3.....96

TYPE OF DEVICE (0=LSM, 1=RCM).....0
```

Change default values as necessary. When all parameters are entered, the progra selects test 2 or test 4 as indicated by the type of device being tested.

6. Execute test 6 as follows:

NOTE

Except for special purposes, use the default value for message assignment. The examples are hexadecimal.

In the following steps, the device address is assumed to be 66 66 96. If the actual address is different, vary the steps accordingly.

EXAMPLE: if the actual address is 67 89 BA, command messages begin: > 67 10 89 BA.... and the Set Normal Response mode format is: > 67 96

a. Set the RCM/LSM to Normal Response Mode: > 67 96

b. Enter the commands in the following formats:

RCM commands:

ACCEPT PORT COMMANDS (store commands to be executed at a later time): > 66 10 66 96 00 __ ...

REQUEST STORED PORT COMMANDS (request a list of port commands held for later execution): > 66 10 66 96 01

REQUEST PORT STATUS: > 66 10 66 96 02

SWITCH PORT STATES (execute stored commands):
> 66 10 66 96 03

RCM Port Commands:

Port Commands	RCM Port Number 0	1	2	3
Power off	00	40	80	C0
Power on	01	41	81	C1
System reset	10	50	90	D0
Program load	11	51	90	D1
Set upper load path to x	2x	6x	Ax	Ex
Set lower load path to y	3y	6Y	By	Fy

LSM commands:

ACCEPT PORT COMMANDS (store commands for execution at a later time): > 66 10 66 96 80 _ _ .....

REQUEST STORED PORT COMMANDS (request a list of port commands held for later execution): > 66 10 66 96 81

REQUEST SWITCH STATUS: > 66 10 66 96 82

SWITCH PORT STATES (execute any stored port commands): > 66 34 66 96 02

LSM Port Commands:

Set switch number XX = XX
Reset switch number XX = add 80 to XX

EXAMPLE: To set switch 3F, enter: > 3F
To reset switch 3F, enter > BF

NOTE

Actual output differs from the entries above as message numbers are assigned. For example, a REQUEST PORT STATUS message to the RCM may be sent as:
> 66 34 66 96 02

TEST PROCEDURE EXAMPLES

To request that the RCM power-on the DCP/40 in port 0, enter the following messages:

```
> 66 96                    SET NORMAL RESPONSE MODE
> 66 10 66 96 00 01        ACCEPT PORT COMMANDS (01=power on)
> 66 10 66 96 03           SWITCH PORT STATES
```

To read the status after the last command is executed, enter the following:

```
> 66 10 66 96 02
```

13.5. RCM/LSM Contention Test

This test runs up to three ports simultaneously. The test generates random messages to send to the RCM or LSM connected to those ports in order to check the capability of the devices to coexist without interferring with each other.

1. Load the test from the contention test diskette, DR2558-6. The screen displays the following message:

   NUMBER OF PORTS TO ENABLE (0 to 3).....1

   Enter the number of ports that have an RCM or an LSM attached to them.

2. The next message requests the parameters for each port, one at a time:

   ```
   PORT #1
     PORT ID.............................0B
     DEVICE ADDRESS......................66 66 96
     DEVICE TYPE (0=LSM, 1=RCM).........0
   ```

   The display is repeated for each port that the user wants to enable. When the parameters for the last port have been entered, the test begins execution. The console displays all of the errors and their explanations. Note that there is only one test on DR2558-6 so test selection is not required.

13.6. Error Reporting

The console displays the error codes generated by the tests and the error code definitions.

14. LOCAL LANGUAGE TRANSLATE

14.1. Introduction

Local language translate facilitates the translation of diagnostic messages which are written in Customer Engineering Technical English (CETE) into the language of the user.

NOTE

The translate cannot be used to change program logic: for example, to eliminate responses or control codes.

All of the screen prompts and error messages can be translated and the diagnostic diskette can be updated for future local language display. The prompts and messages are displayed one phrase at a time.

NOTE

The diskette to be translated must be in the integrated diskette drive. The utility writes message files on that diskette.

14.2. Translate Procedure

When the local language translate is selected from the diagnostic menu, the screen displays the following:

```
        CPA FAMILY DIAGNOSTIC ROUTINES - R5.1
             LOCAL LANGUAGE TRANSLATE


>SERVICE OPTIONS ARE:
>1 = TRANSLATE/DISPLAY
>2 = UPDATE MEDIA AND RETURN
>3 = EXIT UTILITY

>SELECT OPTION (1-3)
>[]
```

Following the selection of option 1 (TRANSLATE/DISPLAY), the screen displays the following:

```
>1.  EXECUTIVE MESSAGE ELEMENT
>2.  SYSTEM TEST
>3.  SERIAL LINE MODULE TEST
>4.  LOCAL STORAGE (Memory) TEST
>5.  RIGID DISK TEST
>6.  MDLM MASS STORAGE TEST
>Press TRANSMIT key to display other selections. or
>Select a Test number from the Menu
>7.  PARALLEL LINE MODULE TEST
>8.  HOST CHANNEL INTERFACE (SU00039/SU00208) TEST
>9.  COPY UTILITY - Integrated Flexible Diskette
>[]
```

When a test is selected, the screen first displays information for use of keys during translate procedures as follows:

```
>MSG WAIT = Press once and previous message is displayed each
            time TRANSMIT is pressed.  Press again and messages
            advance forward as TRANSMIT is pressed.
>F2 = FUNCTION TWO = redisplays the current message
>F3 = FUNCTION THREE = exit and update media
>F4 = FUNCTION FOUR = return to utility menu
```

As TRANSMIT is slowly pressed, the messages from the selected test (1 through 9) are advanced forward and displayed one at a time.

General guidelines for procedures are:

1. Make a back-up copy of the diskette that will be translated.

2. Insert the diskette into the IFDC.

3. Select one of the service options from the first menu.

4. Select the message file from the second menu.

5. If TRANSLATE/DISPLAY is selected, the coded version of the message file is displayed one line phrase at a time. The same phrase is repeated two lines below the first line and the cursor is positioned over the first character of that line.

6. Enter a maximum of 54 characters. The original version is still displayed so the user can correct any errors.

The F3 function is useful if there are interruptions before finishing the message file. When the translated phrase is completed, use the F3 key to update the media. The screen then displays:

```
>THE MESSAGE FILE LOADED HAS A CONTINUE INDEX OF:  0000
>Shall I continue with this index Y/N?
>[]
```

When y (yes) is selected, the utility returns to the previous position in the message file - at the next message that would have been displayed before exiting.

When n (no) is selected, the system goes back to the beginning of the file messages.

Service option 2 (UPDATE MEDIA AND RETURN) is similar to F3; but the index is not saved.

14.3. Error Message

An error message notifies the user of translation problems. An example of the error message is:

TRANSLATION IS TOO LONG

The number of characters in the phrase exceeds 54.

15. COPY UTILITIES

15.1. Introduction

This section describes the copy utilities of the DCP macrodiagnostics program. The available utilities and associated media are:

- Test 11 - Integrated Flexible Diskette (IFDC) Copy Utility
  Copies 8-inch and 5-1/4 inch flexible disks using a flexible diskette drive enclosed in a DCP cabinet.

- Test 12 - Diskette Copy Utility
  Copies 8-inch flexible disks using the Diskette Subsystem Type 8406-00/-03.

15.2. IFDC Copy Procedure

The copy utility for the IFDC reads an input diskette into DCP storage and copies the data to an output diskette from one to nine times. The procedure requires a single-sided, single-density, prepped diskette for the DCP/40/20/10 and a double-sided, double-density, prepped diskette for the DCP/10A/15.

When the copy utility is requested from the menu, the screen displays the following message for a DCP/10:

```
CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1
                IFDC COPY UTILITY


>LOADING Test Message File

                    **** NOTE ****
>THIS UTILITY REQUIRES A DISKETTE FOR OUTPUT WHICH HAS BEEN
>PREPPED FOR SINGLE-SIDED, SINGLE-DENSITY OPERATION.  DISKETTES
>CANNOT BE PREPPED USING THE IFDC.  DATA WHICH HAS BEEN
>MARKED AS DELETED ON THE DISKETTE TO BE COPIED WILL BE
>MARKED AS VALID DATA ON THE OUTPUT DISKETTE.
>WHEN READY TO PROCEED, PRESS XMIT KEY.
>[]
```

When the copy utility is requested from the menu, the screen displays the following message for the DCP/10A/15:

```
        CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1
                        IFDC COPY UTILITY


>LOADING Test Message File

                    ****  NOTE  ****
>THIS UTILITY REQUIRES A DISKETTE FOR OUTPUT WHICH HAS BEEN
>PREPPED FOR DOUBLE-SIDED, DOUBLE-DENSITY OPERATION.  DISKETTES
>MAY BE PREPPED USING THE MDLM MASS STORAGE TEST.
>WHEN READY TO PROCEED, PRESS XMIT KEY.
>[]
```

1. When XMIT is pressed as stated in the previous display, the screen displays:

```
>ENTER NUMBER OF OUTPUT COPIES (1-9) DEFAULT = 1
>[]
```

2. When the number of copies is entered, the screen displays:

```
>INSERT INPUT DISKETTE
>WHEN READY TO PROCEED, PRESS TRANSMIT KEY
```

3. Insert the diskette in the IFDC and press TRANSMIT. The screen displays the following:

```
        CPA FAMILY DIAGNOSTICS RELEASE. R5.1
                    IFDC COPY UTILITY

   Copy x of x       Track No. xxxxx

          ******READING THE DISKETTE*****
```

   As the diskette is read into storage, number of copies, such as COPY 0 of 4, and track number TRACK 0012 appear at the top of the screen.

4. The following message appears at partial or entire completion of the read:

```
>REMOVE INPUT DISKETTE. INSERT OUTPUT DISKETTE
>PRESS XMIT KEY WHEN READY
```

5. The write phase of the utility begins and the following message is displayed:

```
          *****WRITING TO THE DISKETTE*****
```

When the write phase completes, the screen displays the prompt:

TOTAL NUMBER OF COPIES ARE COMPLETED

15.3. General Error Reporting

The console reports the errors in a general error statement and/or an error code. If an error occurs while any option is executing or at the start of execution, the associated information is displayed and the communications processor (CP) stops register interrogation.

The two fatal error statements and associated error codes are explained as follows:

* * FATAL ERROR 0001 * *

A probable software problem in the JLR to PPINIT resulted in the failure of the port to initialize. Check the following:

1. The C PCA resides in the selected port and is strapped correctly;
2. The cables are correctly installed.

* * FATAL ERROR 0002 * *

No response to a port processor (PP) STB instruction caused a time-out during read of line module ID. Verify the configuration and check the C PCA cables and switch settings.

15.4. Error Reporting for the IFDC Utility

The IFDC utility errors are limited to the integrated diskette drive and the media (bad status following an I/O operation). The executive program reports port processor hardware errors and program errors.

If deleted data is found when reading the input diskette, it is written to the output diskette as valid data. The condition is not treated as an error and can affect later use of the output diskette, depending on the application. The condition is reported for each copy routine the first time it occurs:

```
*** WARNING *** DELETED SECTOR FOUND ON INPUT DISKETTE
```

When bad status is reported following an I/O operation, the screen displays the following message:

```
>IFDC ERROR REPORT,  SECTOR = XX  STATUS = XXXX
>IFDC - OPTION SELECTION
>(1) REPEAT LAST I/O OPERATION
>(2) CONTINUE, IGNORE ERROR
>(3) RETURN TO BEGINNING OF IFDC
>(4) RETURN TO BEGINNING OF WRITE ROUTINE
>(5) RETURN TO SYSTEM MENU
>IFDC - ENTER OPTIONS
>]
```

where:

(1) = Retries the last I/O operation. If successful, the program continues.
 2) = Continues as if no error had occurred.
(3) = Restarts from the beginning of the utility.
(4) = Restarts write routine from track 0, sector 1.
(5) = Cancels utility operation and returns control to the system executive.

STATUS = XXXX = Use Figure 15-1 to interpret the status during a read or write routine.

THE HEXADECIMAL X IS REPRESENTED BY THE FOUR BINARY BITS YYYY

```
                    X X X X

    Y  Y  Y  Y    Y  Y  Y  Y    Y  Y  Y  Y    Y  Y  Y  Y
   15 14 13 12   11 10  9  8    7  6  5  4    3  2  1  0
                      BITS
```

READ ROUTINE

Status Code	= Bit =	Description
8000	15	No buffer. Storage was altered in SDR11.
4000	14	Input limit. More than 128 bytes were read.
----	13-12	Illegal status bit (not used).
0800	11	Response timer. Drive did not activate within 10 seconds.
----	10-8	Illegal status bit (not used).
0080	7	Not ready. Drive motor stopped or door opened.
----	6-5	Illegal status bit (not used).
0010	4	Record not found. Track/sector address could not be found on the diskette. Diskette may be incorrectly formatted.
0008	3	IOP error. Read error.
----	2	Not used.
0002	1	Record type - 1 = deleted data, - 0 = valid data
0001	0	Status is non-zero.

WRITE ROUTINE

Status Code	= Bit =	Description
----	15-11	Not used.
0800	11	Response timer. Drive did not activate within 10 seconds.
----	10-8	Not used.
0080	7	Not ready. Drive motor stopped or door opened.
0040	6	Write protect. Write protect slot on diskette is uncovered.
----	5	Not used.
0010	4	Record not found. Track/sector address could not be found on the diskette. Diskette may be incorrectly formatted.
----	3-1	Not used.
0001	0	Status is non-zero.

Figure 15-1. Interpretation of IFDC Status

15.5. Diskette Copy Procedure

The diskette copy utility performs copy, prep, and verify functions using the Diskette Subsystem Type 8406-00/-03. The procedure requires a single-sided, single-density, prepped diskette.

When the copy utility is requested from the menu, the screen displays the following message:

```
CPA FAMILY DIAGNOSTIC ROUTINES.  RELEASE - R5.1
 DISKETTE COPY UTILITY - FDS T8406-00 THRU -03
```

```
>DISKETTE COPY UTILITY - T8406
>ENTER THE PORT NUMBER (0-F, D=4)
>[]
```

1. Enter the port number or press the TRANSMIT key. The screen displays the utility options:

```
>0=PREP, 1=COPY, 2=VERIFY, 3=EXIT (0-3), D=1)
>[]
```

2. Select the function desired and follow the screen prompts. Each function provides instructions for placement of the diskette or diskettes.

   As each function progresses, the screen displays the track number in line four of the fixed area.

16. RESIDENT UTILITIES

16.1. Introduction

Resident utilities perform various functions during diagnostic testing. They can only be accessed through the F1 menu.

Pressing the F1 key (FUNCTION key/F1 key on some consoles) displays the F1 menu:

```
 1 = Continue the test.
 2 = Abort current activity and reinitialize the EXEC
 3 = Hold current activity and use the UTILITIES
>[]
```

Select option 3 and the screen displays:

```
 RESIDENT UTILITIES - ENTER COMMAND
>[]
```

The paragraphs that follow describe the resident utilities. The information is presented in alphabetical order by acronym (command) name. To access a utility enter the two-character command name.

The resident utilties are comprised of the following programs:

- Abort disk patch (AB)
- Add two numbers (AD)
- Set base address for breakpoint (BA)
- Put ASCII string in memory (CA)
- Clear breakpoint (CB)
- Change data for disk patch (CH)
- Change real memory (CR)
- Change virtual memory (CV)
- Display configuration table (DC)
- Dump real memory (DR)
- Display data for disk patch (DS)
- Dump virtual memory (DV)
- Exit utilities (EX)
- Inspect real memory (IR)
- Inspect virtual memory (IV)
- Load file for disk patch (LD)
- Run configuration (RC)
- Replace patch (RP)
- Run from breakpoint (RU)

- Real to virtual conversion (RV)
- Set breakpoint (SB)
- Set segment specification (SE)
- Select system segment number (SN)
- Virtual to real conversion (VR)

16.2. Abort Disk Patch (AB)

This command is used with disk patch to abort the disk patch after a file is loaded. Any file that is loaded must be either aborted or written back to disk. The utility has the following format:

```
>AB <xmit>
```

16.3. Add Two Numbers (AD)

This command allows the user to add 16- or 24-bit numbers and displays the result. Adder does not check for overflow. AD is formatted as follows:

```
>ADxxxxxxxx yyyyyyyy <xmit>
```

where: xxxxxxxx and yyyyyyyy can be up to two 8-digit numbers.

16.4. Set Base Address for Breakpoint (BA)

This command must be used in conjuction with setting the software breakpoint. It sets the base address for an element so when the listing address is supplied, the breakpoint instruction is set in the correct memory location. The screen displays the current base address selected. The utility has the following format:

```
>BAxxxxxx <xmit>
```

where: xxxxxx is a real 24-bit address.

16.5. Put ASCII String in Memory (CA)

This command allows the user to place a string of ASCII characters in memory. The virtual address supplied must be within the 4k boundary described by the 24-bit base address supplied. The ASCII string cannot contain any imbedded control characters and can be a maximum of 73 characters long. It is formatted as follows:

```
>CAxxxx yyyyyyyyyyy...y <xmit>
```

where: xxxx is a virtual address followed by an ASCII string.

16.6. Clear Breakpoint (CB)

This command clears a previously set breakpoint. It has some basic rules. First, a breakpoint cannot be cleared until it has been used. Second, a breakpoint cannot be cleared until it has been set. CB has the following format:

```
>CBy <xmit>
```

where: y is the breakpoint number (0-f).

16.7. Change Data for Disk Patch (CH)

This command is used for disk patch to change data which is to be written back to the diskette. It has the same format as Change Virtual where up to eight words can changed at a time. CH is formatted as follows:

```
>CHyyyy xxxx/zzzz/.../etc. <xmit>
```

where: yyyy is the virtual address
xxxx are the contents to replace yyyy,
zzzz are the contents to replace yyyy+1
etc are the contents to replace yyyy+n.

16.8. Change Real Memory (CR)

This command allows the user to change up to eight locations using a 24-bit real address. CR has the format:

```
>CRxxxxxx yyyy <xmit>
```

where: xxxxxx is a 24-bit real address
yyyy is the contents to replace the the address specified

To change more than one location use the following format:

```
>CRxxxxxx yyyy/zzzz/etc. <xmit>
```

where: yyyy are the contents to replace xxxxxx
zzzz replaces xxxxxx+2
etc. replaces xxxxxx+4, etc.

16.9. Change Virtual Memory (CV)

The CV command changes the contents of one or more locations of memory. The memory locations must fall within the boundaries of word 20 of the segment descriptor register (SDR). This boundary is defined in the length of the segment descriptor, which is always 4k. CV has the format:

```
>CVxxxx yyyy <xmit>
```

where: xxxx is the location of memory to change
yyyy is the new contents

To change more than one location, use the following format:

```
>CVxxxx yyyy/zzzz/etc.
```

where: xxxx is the location of memory to change
yyyy/zzzz/etc. are the new contents to replace xxxx, xxxx+1,xxxx+2. etc. You may use up to eight parameters separated by slashes.

In both cases, the previous contents are displayed to the user as they are replaced.

16.10. Display Configuration Table (DC)

The memory map and line module configuration table display the type of line module in each configured port of the DCP. When DC is selected during resident utility procedures, the screen displays:

CPA FAMILY DIAGNOSTICS ROUTINES RELEASE R5.1

DISPLAY: CONFIGURATION TABLE

```
>DISPLAY OPTIONS
     1 - EXIT DISPLAY ROUTINE
     2 - DISPLAY THE MEMORY MAP
     3 - DISPLAY THE LINE MODULE COMPLEMENT
>Enter option (1-3)  Default is 2:
>Press TRANSMIT to continue
>[]
```

1. When 1 is entered, the screen displays:

```
>RESIDENT UTILITIES - ENTER COMMAND
>[]
```

2. Enter an EX to exit and the screen displays:

```
>RESUMING INTERRUPTED PROCEDURE
```

3. To return to an interrupted test, enter an SOE (>) character on the line following the display, move the cursor one space to the right, and press TRANSMIT.

4. When 2 is entered, the screen displays the storage map. The map reads from the left (lowest address) with each character representing 64K bytes of storage. A "1" entry indicates error-free storage; a "0" entry indicates storage errors, or non-existent storage.

RANGE	STORAGE	RANGE	STORAGE
000000 to 0FFFFF	1111111100000000	100000 to 1FFFFF	0000000000000000
200000 to 2FFFFF	0000000000000000	300000 to 3FFFFF	0000000000000000

   a. Each time the TRANSMIT key is pressed, the screen displays two lines (four entries) of the storage map. When the last entry is reached, the screen displays the message:

   END OF STORAGE MAP ENTRIES

5. When selection 3 is entered the screen displays the line module complement. Each number displayed in a port number column is a LMID code which identifies the line module type. Refer to the listing that follows the figure to find a specific line module type.

```
PORT:     00 01 02 03 04 05 06 07 08 09  A  B  C  D  E  F

CLC: 00   XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
CLC: 01   XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
>Press TRANSMIT to Continue
```

   a. When the TRANSMIT key is pressed, the screen displays four more CLCs. Following the last entry, the screen displays the message:

   LAST CLC FOUND WITH LINE MODULES

The following is an example of an eight-port DCP configuration:

```
COMMUNICATIONS LINE CONTROLLER/INPUT-OUTPUT PROCESSOR

  >CLC: 00  67 67 FF 50 07 01 44 11 00 00 00 00 00 00 00
00

CLC/IOP #
      PORT #0
         PORT #1
            PORT #2
               PORT #3
                  PORT #4
                     PORT #5
                        PORT #6
                           PORT #7
```

The line module identifiers (LMIDs) and associated microcode identifiers (MCID) are:

LMID	Line Module	MCID
01	Intergated Flexible Disk/Controller (256 KB) F1939	03
02	Byte Input/Output Controller (BIOC) F1949	02
04	SU00039 Host Interface (Primary Port) F1947	58
05	SU00039 Host Interface (Secondary Port) F1947	58
06	Front End Processor Interface (FEPI) - Host F3882	50 50
19	FEPI - Slave F3882	50
07	Bi-Directional Byte Interface (BDBI) F3878	07
08	Integrated Flexible Disk/Controller (1024 KB)	08
09	Multiple Device Line Module (MDLM) F3893	09
10	16-Bit Peripheral Channel F1948	10
11	SU00057 Host Channel (32 bit) F1946	11
12	Intercomputer Channel or loopback (16 bit)	12
14	SU00208 Block Mux (Primary Port) F1947	48
15	SU00208 Block Mux (Secondary Port) F1947	-
38	Automatic Dialer F1945	38
40	Asynchronous F1941	*
44	Multiline (4X1) Asynchronous F3165	59
45	Multiline (4X1) Asynchronous Video Text F3165	59
50	Synchronous F1942	*

*Both line modules return a hardware ID of 50 following either power-on or master-clear. After the operation parameters are loaded in the line module, an ID of 50 is returned if the parameters were synchronous and an ID of 40 is returned if the parameters were asynchronous.

LMID	Line Module	MCID
54	Multiline Synchronous F3837	
	- Uniscope	4E
	- UDLC	4F
60	Medium Speed Loadable (MSLLM) F3163 (RS-449)	
	- Basic Asynchronous	20
	- Basic Synchronous	24
	- UDLC	28
61	MSLLM (X.21)	
	- Basic Synchronous	25
	- UDLC	29
64	Direct Connect Single Station (DCSS) F3847	70
65	Twisted Pair (TPLM) F4230	27
67	MSLLM (RS-232C)	
	- Basic Asynchronous	20
	- Basic Synchronous	24
	- UDLC	28
6B	MSLLM (Kintetsu)	
	- Basic Asynchronous	22
6F	MSLLM (no cable)	-
70	High Speed Loadable (HSLLM) F3164 (RS-449)	
	- Basic Synchronous	26
	- UDLC	2A
71	HSLLM (X.21)	
	- UDLC	2B
	- 1100 FDX	33
7D	HSLLM (Bell 303)	
	- Basic Synchronous	26
	- UDLC	2A
7E	HSLLM (V.35)	
	- Basic Synchronous	26
	- UDLC	2A
7F	HSLLM (no cable)	-

Microcode ID 00 = line module microcode is not loaded.
Microcode ID EF = microprogram was loaded but requires an EOF entry (4 bytes of 00 and 1 byte of FF) to operate (i.e., ROM microcode still has control).
Microcode IDs F0 through FF = an error was detected during the microprogram load and the line module is not operational; or line module is used as console driver.

16.11. Dump Real Memory (DR)

The DR command allows a dump from anywhere in memory. It uses the same T option as the DV command. DR has the format:

```
>DRxxxxxx T <xmit>
```

where: xxxxx is a real address
T is the amount of eight-word sets to be dumped.

16.12. Display Data for Disk Patch (DS)

The DS command works like the display virtual command. This command must be used to display the data before any changes can be applied to memory for disk patch purposes. DS has the format:

```
>DSxxxx <xmit>
```

where: xxxx is a virtual (listing) address.

16.13. Dump Virtual Memory (DV)

The DV command displays eight memory locations on a single line of the screen. To the right of the displayed locations is the ASCII equivalent of the data. With the T option, up to eight lines can be displayed, providing a total of 64 words from one command string. DV is formatted as follows:

```
>DVxxxx T <xmit>
```

where: xxxx is a virtual address within the 4k boundary of the base
T is the number of eight-word sets

16.14. Exit Utilities (EX)

The EX command exits the utilities and returns to the procedure where the F1 interrupt was encountered. See paragraph 16.10 for details.

16.15. Inspect Real Memory (IR)

The IR command uses a 24-bit real address to access any memory location. It has the format:

```
>IRxxxxxx <xmit>
```

where: xxxxxx is a 24-bit real address.

16.16. Inspect Virtual Memory (IV)

The IV command allows the user inspect any location within the boundaries of memory that is currently loaded into word 20 of the SDR. The boundary is defined in the length of the segment descriptor, which is always 4k. IV has the format :

```
>IVxxxx <xmit>
```

where: xxxx is a virtual address

16.17. Load File for Disk Patch (LD)

The LD command loads a file into memory where disk patches can then be applied. It has the following format:

```
>LDxx <xmit>
```

where: xx is the file ID

The xx values of the file IDs for disk patch operations are:

ID	File
00	Bootloader
01	Executive base element
02	1st call element
03	2nd call element
04	Load table
05	Console PP
06	Loader PP
07	Executive common message element
08	Console CP loadable element
20	System test main body
21	System test message element
22	System test - Local storage test element
23	System test - Local storage test PP
24	System test - Serial line module subtest
25	System test - Serial line module subtest PP
26	System test - Parallel line module subtest
27	System test - Parallel line module subtest PP
28	System test - Diskette subtest
29	System test - Diskette subtest PP
2B	Local language translate

ID	File
2C	Configuration file
2E	System test - Cartridge disk
2F	System test - Cartridge disk PP
30	Serial line module test
31	Serial line module test message element
32	Serial line module test PP
33	Local storage test
34	Local storage test message element
35	Rigid disk test (T8409)
36	Rigid disk test message element
37	Rigid disk test PP
42	Parallel line module (PLM) test
43	PLM test message element
44	PLM test PP
45	SU00039/SU00208 line module test
46	SU00039/SU00208 test message element
47	SU00039/SU00208 test PP
48	Cartridge disk test
49	Cartridge message element
4A	Cartridge test test PP
4E	IFDC/MDLM copy utility
4F	IFDC/MDLM copy message element
53	MDLM mass storage test
54	MDLM test message element
55	MDLM test PP

16.18. Run Configuration (RC)

The RC command executes the "CNFG" procedure, creating the memory map and the configuration table.

16.19. Replace Patch (RP)

The RP command is used with disk patch to write data that has been altered with the CD command back to diskette. It has the following format:

```
>RP <xmit>
```

16.20. Run for Breakpoint (RU)

When a breakpoint is set, the RU command starts execution of the breakpoint and continues execution after the breakpoint is reached and the registers are displayed. RU has the format:

```
> RU <xmit>
```

16.21. Real to Virtual Conversion (RV)

This translation command takes the user's input, shifts it one bit to the right, and then displays it. RV has the format:

```
>RVxxxxxx <xmit>
```

where: xxxxxx is a 24-bit real address.

16.22. Set Breakpoint (SB)

The SB command sets software breakpoints. Up to 15 breakpoints can be set at any given moment. When a breakpoint is reached , the utility displays the breakpoint number and the listing address, followed by the register set the procedure was using. The SB command has the format:

```
>SBy xxxx <xmit>
```

where: y is the breakpoint count (0-F)
xxxx is the listing address.

Different breakpoints can set using different base addresses without changing the base address to clear them.

16.23. Set Segment Specification (SE)

The SE command, like the SN command, selects the base for the working SDR, but the user presents the base according to an SDR which is currently loaded and whether it is a process or control SDR. This command also displays the 24-bit address on the screen. SE has the format:

```
>SExxxx y <xmit>
```

where: xxxx is a virtual address
y is either "C" for control or "P" for process mode

16.24. Select System Segment Number (SN)

The SN command creates a base address for all virtual memory accesses. It uses the system segment number (SSN) to index into the system segment table and then loads the SSN into the working SDR. For convenience, the screen displays the 24-bit base address and the access flags. Note that a selected segment does not change the segment address displayed on the screen, it simply means that the segment is not used. The SN command has the format:

```
>SNxx <xmit>
```

where: xx can be any index within the boundaries of the system segment table

16.25. Virtual to Real Conversion (VR)

This translation command takes the user's input, shifts it one bit to the left, and then displays it. It has the following format:

```
>VRxxxx <xmit>
```

where: xxxx is a virtual address

A. TROUBLE ISOLATION PROCEDURES

A.1. Introduction

This appendix contains troubleshooting information for the DCP family macrodiagnostics. To find the pertinent isolation data, use the isolation numbers associated with the errors described in previous sections of this manual.

Isolation Procedure #	Isolation Information/Activity
00001	DCP/40 1. Ensure that microdiagnostic LSTOR test runs on all memory banks. 2. Ensure that all configuration PCAS are properly strapped. 3. Replace port control PCA. 4. Replace timing and control PCA. 5. Replace byte interface 0 PCA. 6. Replace byte interface 1 thru 3 PCAs. 7. Replace array 0 PCA 8. Check memory termination. DCP/20 1. Follow DCP/40 procedure but skip step 3. DCP/10/10A/15 NOTE The DCP/15 does not contain a memory expansion PCA. 1. Replace processor PCA. 2. Replace memory expansion PCA.

Isolation Procedure #	Isolation Information/Activity
00002	1. Determine the faulty array from memory address and replace. The arrays and their corresponding memory addresses are:

DCP/40

16K storage bank 0
array 0 = adr X0000 to adr X1FFFF 0.00 - 0.13M
array 1 = adr X20000 to adr X3FFFF 0.13 - 0.25M
array 2 = adr X40000 to adr X5FFFF 0.25 - 0.38M
array 3 = adr X60000 to adr X7FFFF 0.38 - 0.50M

16K storage bank 1
array 0 = adr X200000 to adr X21FFFF 0.50 - 0.63M
array 1 = adr X220000 to adr X23FFFF 0.63 - 0.75M
array 2 = adr X240000 to adr X25FFFF 0.75 - 0.88M
array 3 = adr X260000 to adr X27FFFF 0.88 - 1.00M

16K storage bank 2
array 0 = adr X400000 to adr X41FFFF 1.00 - 1.13M
array 1 = adr X420000 to adr X43FFFF 1.13 - 1.25M
array 2 = adr X440000 to adr X45FFFF 1.25 - 1.38M
array 3 = adr X460000 to adr X47FFFF 1.38 - 1.50M

16K storage bank 3
array 0 = adr X600000 to adr X60FFFF 1.50 - 1.63M
array 1 = adr X610000 to adr X61FFFF 1.63 - 1.75M
array 2 = adr X620000 to adr X62FFFF 1.75 - 1.88M
array 3 = adr X630000 to adr X63FFFF 1.88 - 2.00M

64K storage bank 0
array 0 = adr X00000 to adr X7FFFF 0.00 - 0.50M
array 1 = adr X80000 to adr XFFFFF 0.50 - 1.00M
array 2 = adr X100000 to adr X17FFFF 1.00 - 1.50M
array 3 = adr X180000 to adr X1FFFFF 1.50 - 2.00M

16K storage bank 1
array 0 = adr X200000 to adr X21FFFF 2.00 - 2.13M
array 1 = adr X220000 to adr X23FFFF 2.13 - 2.25M
array 2 = adr X240000 to adr X25FFFF 2.25 - 2.38M
array 3 = adr X260000 to adr X27FFFF 2.38 - 2.50M

16K storage bank 2
array 0 = adr X400000 to adr X41FFFF 2.50 - 2.63M
array 1 = adr X420000 to adr X43FFFF 2.63 - 2.75M
array 2 = adr X440000 to adr X45FFFF 2.75 - 2.88M
array 3 = adr X460000 to adr X47FFFF 2.88 - 3.00M

Isolation Procedure #	Isolation Information/Activity
00002 (cont)	16K storage bank 3 array 0 = adr X600000 to adr X61FFFF 3.00 - 3.13M array 1 = adr X620000 to adr X63FFFF 3.13 - 3.25M array 2 = adr X640000 to adr X65FFFF 3.25 - 3.38M array 3 = adr X660000 to adr X67FFFF 3.38 - 3.50M DCP/20 (2M byte) 64K storage bank 0 array 0 = adr X00000 to adr X7FFFF 0.00 - 0.50M array 1 = adr X80000 to adr XFFFFF 0.50 - 1.00M array 2 = adr X100000 to adr X17FFFF 1.00 - 1.50M array 3 = adr X180000 to adr X1FFFFF 1.50 - 2.00M 16K storage bank 1 array 0 = adr X200000 to adr X21FFFF 2.00 - 2.13M array 1 = adr X220000 to adr X23FFFF 2.13 - 2.25M array 2 = adr X240000 to adr X25FFFF 2.25 - 2.38M array 3 = adr X260000 to adr X27FFFF 2.38 - 2.50M 16K storage bank 2 array 0 = adr X400000 to adr X41FFFF 2.50 - 2.63M array 1 = adr X420000 to adr X43FFFF 2.63 - 2.75M array 2 = adr X440000 to adr X45FFFF 2.75 - 2.88M array 3 = adr X460000 to adr X47FFFF 2.88 - 3.00M DCP/20 (0.5M byte) 16K storage bank 0 array 0 = adr X0000 to adr X1FFFF 0.00 - 0.13M array 1 = adr X20000 to adr X3FFFF 0.13 - 0.25M array 2 = adr X40000 to adr X5FFFF 0.25 - 0.38M array 3 = adr X60000 to adr X7FFFF 0.38 - 0.50M DCP/10/10A/15 (1M byte) Processor PCA 64K RAM = adr X0000 to adr X1FFFF 0.00 - 0.125M 256K RAM = adr X0000 to adr X7FFFF 0.00 - 0.50M NOTE The DCP/15 does not contain a memory expansion PCA. Expansion PCA 64K RAM = adr X20000 to adr X1FFFFF 0.125 -2.00M 256K RAM = adr X80000 to adr X27FFFF 0.75 - 2.50M

Isolation Procedure #	Isolation Information/Activity
00003	DCP/40-DCP/20 (2M byte) 1. Ensure that microdiagnostics run successfully on all storage modules. 2. Ensure that macrodiagnostic utilities recognize the physical storage configuration. 3. Ensure that all configuration PCAs are strapped correctly. 4. If storage address causing RESUME cannot be identified, isolate cause of failure by disabling storage banks one at a time with configurator strap. If the RESUME persists, isolate error using EIA procedures (microdiagnostics manual or Appendix B.) DCP/20 1. Follow DCP/40 procedure but skip step 4. DCP/10/10A/15 1. Ensure that the macrodiagnostic utilities recognize the physical storage configuration. 2. If the RESUME persists, replace processor PCA. 3. Replace memory expansion PCA (DCP/10/10A).
00004	Possible IC type codes are: 2 3 = bit 0 0 = 64K storage devices - DCP/40/20 (2M byte) 0 1 = 16K storage devices 1 0 = DCP/20 storage 1 1 = not used DCP/40-DCP/20 (2M byte) 1. Ensure that memory configuration table (map) matches physical configuration. 2. Ensure that all arrays in any bank are the same. 3. Replace array in question. 4. Replace port control PCA in storage bank. 5. Replace byte interface 3 PCA. 6. Replace timing and control PCA.

Isolation Procedure #	Isolation Information/Activity
	DCP/20
00004 (cont)	1. Follow DCP/40 procedure but skip step 4.
	DCP/10/10A/15
	1. Ensure that memory configuration table (map) matches physical configuration. 2. Replace processor PCA and/or memory expansion PCA.
00005	DCP/40-DCP/20 (2M byte)
	1. Replace addressed array. (See Isolation Procedure #00002.) 2. Replace port control PCA. 3. Determine incorrect byte and replace corresponding byte interface PCA. 4. Replace timing and control PCA.
	DCP/20
	1. Follow DCP/40 procedure but skip step 2.
	DCP/10/10A/15
	1. Replace processor PCA and/or memory expansion PCA.

Isolation Procedure #	Isolation Information/Activity
00006	DCP/40-DCP/20 (2M byte) 1. Ensure that microdiagnostics LSTOR test runs on all memory banks. 2. Replace port control PCA. 3. Replace timing and control PCA. DCP/20 1. Follow DCP/40 procedure but skip step 2. DCP/10/10A/15 1. Replace processor PCA.
00007	DCP/40-DCP/20 (2M byte) 1. Determine incorrect byte and replace corresponding byte interface PCA. 2. Replace port control PCA. 3. Replace timing and control PCA. DCP/20 1. Follow DCP/40 procedure but skip step 2. DCP/10/10A/15 1. Replace processor PCA.
00008	DCP/40-DCP/20 (2M byte) 1. Ensure that microdiagnostics LSTOR test runs on all memory banks. 2. Replace byte interface PCA corresponding to address difference. 3. Replace port control PCA. 4. Replace timing and control PCA. DCP/20 1. Follow DCP/40 procedure but skip step 4. DCP/10/10A/15 1. Replace processor PCA. 2. Replace memory expansion PCA (DCP/10/10A).

Isolation Procedure #	Isolation Information/Activity
00009	DCP/40-DCP/20 (2M byte)

1. Possible status read conditions are:

Command: Read status register - do not clear register.

0 7	8 29	30 31
110001H0	main storage address	port #

Command: Read status register - clear status register

0 7	8 29	30 31
110010H0	main storage address	port #

The H bit (bit 6) is the priority hold bit and is used in conjunction with bit 3 to control the priority hold logic in the storage module.

Bits 3 6	Function
0 0	Clear priority hold
0 1	Set priority hold
1 0	Not used
1 1	Do not change priority hold

Results of read status:

0 1	2 3	4 7	8 15	16 23	24 28	29-31
00	A	B	C	D	E	F

where:

Field A = port number of requestor
Field B = array PCA status
- 04 = array 0 good
- 05 = array 1 good
- 06 = array 2 good
- 07 = array 3 good

Field C = syndrome bits
Field D = check bits

Isolation Procedure #	Isolation Information/Activity
00009 (cont)	Field E = log data and log address bit 24 = error log data of the associated address bit 25 - 28 = XXXX (no meaning) Field F = error code register Each memory port has its own error register. The error register reports only the last error. Error code formats are: 001 = address or control parity error 011 = write data parity error 100 = multiple uncorrectable data error 2. Compare command data with information in step 1. Compare R5 data with error code format in step 1. Replace array identified by address. 3. Replace port control PCA. 4. Replace timing and control PCA. DCP/20 1. Follow DCP/40 procedure but skip step 3. DCP/10/10A/15 1. Replace processor and/or memory expansion PCA.
00010	DCP/40-DCP/20 (2M byte) 1. Replace port control PCA. 2. Replace addressed array. DCP/20 1. Replace addressed array. DCP/10/10A/15 1. Replace processor and/or memory expansion PCA.

Isolation Procedure #	Isolation Information/Activity
00011	DCP/40-DCP/20 (2M byte) 1. Replace port control PCA. 2. Replace timing and control PCA. 3. Determine memory address and replace faulty array. (See Isolation Procedure #00002.) DCP/20 1. Follow DCP/40 procedure but skip step 1. DCP/10/10A/15 1. Replace processor and/or memory expansion PCA.
00012	DCP/40-DCP/20 (2M byte) 1. Replace port control PCA. 2. Determine incorrect byte and replace corresponding byte interface PCA. 3. Replace timing and control PCA. 4. Replace addressed array. (See Isolation Procedure #00002.) DCP/20 1. Follow DCP/40 procedure but skip step 1. DCP/10/10A/15 1. Replace processor and/or memory expansion PCA.
00013	DCP/40-DCP/20 (2M byte) 1. Replace addressed array. (Refer to Isolation Procedure 00002.) 2. Replace port control PCA. 3. Replace timing and control PCA. 4. Replace byte interface PCA. DCP/20 1. Follow DCP/40 procedure but skip step 2. DCP/10/10A/15 1. Replace processor and/or memory expansion PCA.

Isolation Procedure #	Isolation Information/Activity
00014	DCP/40-DCP/20 (2M byte) 1. Replace byte 0 interface PCA. 2. Replace port control PCA. 3. Replace timing and control PCA DCP/20 1. Follow DCP/40 procedure but skip step 2. DCP/10/10A/15 1. Replace processor and/or memory expansion PCA.
00015	DCP/40-DCP/20 (2M byte) 1. Determine incorrect byte and replace corresponding byte interface PCA. 2. Replace port control PCA. 3. Replace timing and control PCA. DCP/20 1. Follow DCP/40 procedure but skip step 2. DCP/10/10A/15 1. Replace processor and/or memory expansion PCA.
00016	DCP/40/20 1. Ensure that microdiagnostics run on this port. 2. Ensure that diagnostic configuration table is correct and the proper port is selected. 3. Is C PCA in the correct slot? 4. Replace the C PCA. 5. Replace the R PCA. DCP/10/10A/15 1. Ensure that the diagnostic configuration table is correct. 2. Replace processor PCA.

Isolation Procedure #	Isolation Information/Activity
00017	DCP/40/20 1. Ensure that microdiagnostics run on this port. 2. If internal loopback is running, replace the B PCA. 3. If external loopback is running, the diagnosis order is: a. Ensure that cables are connected to the proper B PCAs. b. Replace B PCA. c. Replace C PCA. d. Replace R PCA. e. Replace cables. DCP/10/10A/15 1. If internal loopback is running, replace the B PCA. 2 If external loopback is running, the diagnosis order is: a. Ensure that cables are connected to the proper B PCAs. b. Replace B PCA. c. Replace C PCA. d. Replace cables.
00018	DCP/40/20 1. Ensure that cable loopback is operational. 2. Replace parallel interface PCA in disk controller. 3. Replace B PCA. 4. Replace C PCA (check straps). DCP/10/10A/15 1. Follow the DCP/40/20 procedure.

Isolation Procedure #	Isolation Information/Activity
00019	DCP/40/20 1. This test runs on any valid DCP port. Hexadecimal selections are between X0 and XFF. Check screen display for selected port and LMID and ensure that LMID agrees with configuration table. Selected port must contain LMID which is legal for selected test (see system configuration table). 2. Check strapping. DCP/10/10A/15 1. Follow DCP/40/20 procedure.
00020	DCP/40/20 1. Ensure that parallel line module runs cable loopback. 2. Replace B PCA. 3. Replace C PCA. 4. Replace parallel interface PCA in disk controller. 5. Replace processor in disk controller. 6. Replace disk interface PCA in disk controller. DCP/10/10A/15 1. Follow the DCP/40/20 procedure.
00021	DCP/40/20 1. Check disk controller status. 2. Ensure that disk drive adjustments are within tolerance. 3. Ensure that cable is intact between drive and controller. DCP/10/10A/15 1. Follow the DCP/40/20 procedure.

Isolation Procedure #	Isolation Information/Activity
00022	DCP/40/20 1. Ensure that seek time adjustments of the disk are within tolerance. 2. Ensure that exerciser seeks properly. 3. Replace disk I/O PCA in controller. 4. Replace parallel I/O PCA in controller. 5. Replace processor PCA in controller. 6. Ensure that parallel line module runs cable loopback test. DCP/10/10A/15 1. Follow the DCP/40/20 procedure.
00023	DCP/40/20 1. Ensure that disk exerciser operates properly with write protect enabled. 2. Replace disk I/O PCA in controller. 3. Replace parallel I/O PCA in controller 4. Replace processor PCA in controller. 5. Ensure that parallel line module runs cable loopback. DCP/10/10A/15 1. Follow the DCP/40/20 procedure.
00024	DCP/40/20 1. If BIOC is installed, ensure that microdiagnostic BIOC test is operational. 2. If BDBI is installed, ensure that external controller loopback is functional. 3. Check cable to diskette controller. 4. Replace diskette controller. 5. Replace R PCA. DCP/10/10A/15 1. Ensure that BDBI external controller loopback is functional. 2. Check cable to diskette controller. 3. Replace diskette controller. 4. Replace processor PCA.

Isolation Procedure #	Isolation Information/Activity
00025	DCP/40/20 1. If BIOC is installed, ensure that microdiagnostic BIOC test is operational. 2. If BDBI is installed, ensure that external controller loopback is functional. 3. Replace BIOC/BDBI. DCP/10/10A/15 1. Ensure the BDBI external controller loopback is functional. 2. Replace BDBI.
00026	DCP/40/20 - DCP/10/10A/15 1. Replace diskette media. 2. Attempt to read in another drive. 3. Ensure that media has been prepped.
00027	DCP/40/20 1. If BIOC is installed, ensure that microdiagnostic BIOC test is operational. 2. If BDBI is installed, ensure that external controller loopback is functional. 3. Check cable to diskette controller. 4. Replace diskette controller. 5. Replace BIOC/BDBI. DCP/10/10A/15 1. Ensure that BDBI external controller loopback is functional. 2. Check cable to diskette controller. 3. Replace diskette controller. 4. Replace BDBI.
00028	DCP/40/20 1. Ensure that LMID is correct for diagnostic test. 2. Replace line module. 3. Replace R PCA. 4. Replace X PCA in CLC.

Isolation Procedure #	Isolation Information/Activity
00028 (cont)	DCP/10/10A/15 1. Ensure that LMID is correct for diagnostic test. 2. Replace line module. 3. Replace processor PCA.
00029	DCP/40/20 1. Ensure that proper port is selected for the test. 2. Check POC status of LEDs on memory 2nd port PCA of SU0039 line module. NOTE Lights are cleared during initialization and when MODE CLEAR is sent to line module. Indicator 1 2 3* — POC Status 0 0 0 — ALU failure 0 0 1** — Control store failure 0 1 0 — DDT failure 0 1 1 — Data RAM failure 1 1 0 — DMT failure 1 1 1 — POC successful *Indicator 3 is bottom LED and is MSB. **'1' signifies that indicator is ON. NOTE The I/O sequencer PCA causes failures of the ALU, control store, and data RAM. The L-bus interface PCA causes failures of the DDT and the DMT. The memory 2nd port PCA causes failures of the control store and the data RAM.

Isolation Procedure #	Isolation Information/Activity
00029 (cont)	3. Replace L-bus/channel interface PCA of SU00039 line module. 4. Replace I/O sequencer PCA of SU00039 line module. 5. Replace memory 2nd port PCA of SU00039 line module. 6. Replace R PCA. 7. Check for defective interconnection cables. 8. Check for defective line module backplane terminators. 9. Replace X PCA in CLC. DCP/10/10A/15 1. Follow DCP/40/20 procedure, steps 1 through 5, 7, and 8. 2. Replace processor PCA.
00030	DCP/40/20 - DCP/10/10A/15 1. Ensure that strapping of L-bus/channel interface and memory 2nd port PCAs is correct. 2. Replace memory 2nd port PCA. 3. Replace I/O sequencer PCA. 4. Replace I/O cable. 5. Replace channel terminators.
00031	DCP/40/20 - DCP/10/10A/15 1. Ensure that online/offline switch selection of operator control panel (SU00039 line module) is functioning properly. 2. Ensure that operator control panel cable is properly seated. 3. Ensure that online/offline relay of operator control panel is functioning properly. 4. Replace I/O sequencer PCA. 5. Replace memory 2nd port PCA. 6. Replace L-bus/channel interface PCA.

Isolation Procedure #	Isolation Information/Activity
00032	DCP/40/20 1. Ensure that bus and tag cables are oriented properly. 2. Ensure that channel is terminated properly. 3. Check interface connection to host connector plate. 4. Replace memory 2nd port PCA. 5. Replace I/O sequencer PCA. 6. Replace L-bus/channel interface PCA. 7. Replace R PCA. DCP/10/10A/15 1. Follow DCP/40/20 procedure except in step 7, replace processor PCA.
00033	DCP/40/20 1. Ensure proper diskette is installed in integrated diskette drive. 2. Ensure that IFDC microdiagnostic is operational. DCP/10/10A/15 1. Ensure proper diskette is installed in integrated diskette drive.
00034	DCP/40/20 - DCP/10/10A/15 1. This test runs on any valid DCP port. Hexadecimal selections are between X0 and XFF. Check screen display for selected port and LMID and ensure that LMID agrees with configuration table. Selected port must contain LMID which is legal for selected test (see system configuration table). 2. Check strapping.

Isolation Procedure #	Isolation Information/Activity
00035	DCP/40/20 1. Ensure that microdiagnostics run on this port. 2. Ensure that diagnostic configuration table is correct and that the proper port is selected. 3. Is the line module in the correct slot? 4. Replace the line module PCA. 5. Replace th R PCA. DCP/10/10A/15 1. Ensure that diagnostic configuration table is correct and that the proper port is selected. 2. Is the line module in the correct slot? 3. Replace the line module PCA. 4. Replace the processor PCA. DCP/10A/15
00036	1. Check the MDLM, the cable to the SCSI, and the line module bus. 2. Check the SCSI and the strapping. 3. Check the disk and the disk cabling 4. Check the diskette and the diskette cabling. GENERAL GUIDELINES If you can run the diskette tests but cannot run the hard disk tests, then the problem is the disk or the SCSI/Cable. If you cannot access the disk and the diskette, then the problem is the SCSI, or the MDLM, or the cable.

B. SUPPLEMENTAL INFORMATION

B.1. Introduction

This appendix provides information that is helpful in determining the causes of hardware and software errors. It includes the following:

- A summary of the Error Indicator Analysis (EIA) Procedure
- The format and content of System Control Registers 14, 15, 13, and 11.
- The format and content of the Port Processor State Item Buffer

B.1. Use of EIA to Isolate CP and CLC Hardware Problems

The Error Indicator Analysis (EIA) procedure can be used to isolate CP and CLC hardware problems. Parity checking detects approximately 90 percent of the CP hardware faults of the DCP/40 and enables 80 percent of all faults to be corrected by replacement of one or two PCAs. Isolation is at or near the source of the fault and avoids misleading propagated errors. In the DCP/20, as well as the DCP/40, parity checking detects approximately 70 percent of CLC hardware faults and enables 60 percent of all faults to be corrected by replacement of one or two PCAs.

This paragraph summarizes the EIA procedure. It provides the CP and CLC maintenance panel error displays and procedures to isolate the hardware fault. See DR2547, DCP/40 Type 8596 Microdiagnostics Software and Procedures Description and DR2555, DCP/20 Type 8597 Microdiagnostics Software and Procedures Description for a complete discussion of the procedure.

B.2. EIA Procedure for CP Hardware Faults

The following procedure assumes use of the correct CP maintenance panel associated with the faulty CP.

NOTE

DCP/40 systems with more than one CP have separate CP maintenance panels for each CP.

1. Set PANEL ENABLE switch up (enabled) and RESTART switch down (disabled). All other switches should be down, including LOAD switches on top cabinet.

2. Compare ERROR DISPLAY indicators on CP maintenance panel to those illustrated in Figure B-1. Where the indicators match the figure, note the procedure number.

3. Using the procedure number from Figure B-1 as an index into Figure B-2, perform the corrective action indicated.

ALU 1	ALU 2	SA UPR	SA LWR	SX UPR	SX LWR	R REG1	R REG2	U PA UPR	U PA LWR	U INST	ECW	RE-SUME	ERR ACK	MEM LOCK-OUT	Procedure Number Figure B-2
No lit indicators Any other combination of indicators not shown															23
L															19
L	L	L	L	L	L			L	L						1
L			L		L										11
	L														10
	L	L		L											2
															9
		L													18
		L	L												18
		L	L	L											13
		L	L	L	L										13
		L	L		L										13
		L	L			L									14
		L	L				L								14
		L	L					L							14
		L	L					L	L						12
		L	L						L						15
		L	L						L						12
		L		L	L										13
		L		L	L										13
		L			L										13
		L				L									14
		L					L								14
		L						L							6
		L						L	L						12
		L							L						12
			L												18
			L	L											13
			L	L	L										13
			L		L										13
			L			L									14
			L				L								14
			L					L							12
			L					L	L						12
			L						L						6
				L											18
				L	L										18
					L										18
						L									7
						L	L								8
							L								7
								L							5
								L	L						12
								L			L				4
									L						5
									L		L				4
										L					3
											L				4
												L			20
													L		22
														L	21

Note: L = Lit

64212

Figure B-1. CP Error Displays

Procedure Number	CP PCA Replacement Order or Other Procedures
1	A1(99%), K(1%)
2	A2(99%), K(1%)
3	M2(92%), K(3%), S(2%), C(1%), R2(1%), R1(1%)

NOTE

If DCP/40 has M1 PCAs, the M2 (92%) entry depends on the following U PA ERR value:

U PA ERR	SUSPECT PCAs
1000 - 13FF	M2(92%)
1400 - 17FF	M1-J31(82%), M2(10%)
1800 - 1BFF	M1-J32(82%), M2(10%)
1C00 - 1FFF	M1-J30(82%), M2(10%)

Note that U PA ERR is locked with the address of the instruction that was executed two instructions prior to the one causing the U INST error. If a jump from one M PCA to another occurred at this time, the value can point to the wrong PCA; however, that probability is small.

4	R1(48%), R2(48%), K(3%), S/E/C/D/X(1%)
5	S(97%), K(2%), E(1%), R1/R2(remote possibility)
6	R1(30%), R2(30%), M2(29%), A1(4%), A2(4%), S(2%), X/F1/F2/C(1%)

Figure B-2. Corrective Action for CP Hardware Faults (Sheet 1 of 7)

Procedure Number	CP PCA Replacement Order or Other Procedures
7	R1(45%), R2(45%), M1(7%), M2(7%), A1(1%), A2(1%), F1/F2/X/E(1%). Note this possible exception: If MICRO PA DISPLAY shows 00DA, set the ERR CTRL switch up, press SYSTEM RESET and, if the CP again stops with MICRO PA DISPLAY showing 00DA and the GENERAL DISPLAY bits 16-31 showing 00C3 (when both DISPLAY CTRL switches are down), then the faulty PCA is M2(90%). The micromemory instruction located at the address specified by U PA ERR (which should be greater than 1000) has a bit stuck high/low.
8	R1(45%), R2(45%), K(8%), S(2%)
9	A2(100%)
10	A1(100%)
11	K(80%), S(15%), A1(2%), A2(2%), M2(1%)
12	S(100%)
13	A1(50%), A2(50%)
14	R1(50%), R2(50%). If any microcode development is taking place, then: SOFTWARE(99%). Note this possible exception: If MICRO PA DISPLAY shows 00DA, set the ERR CTRL switch up, press SYSTEM RESET and, if the CP again stops with MICRO PA DISPLAY showing 00DA and the GENERAL DISPLAY bits 16-31 showing 00C3 (when both DISPLAY CTRL switches are down), then the faulty PCA is M2(90%). The micromemory instruction located at the address specified U PA ERR (which should be greater than 1000) has a bit stuck high/low.
15	R1(32%), R2(32%), K(20%), S(15%), M2(1%)
16	Not defined at present
17	Not defined at present

Figure B-2. Corrective Action for CP Hardware Faults (Sheet 2 of 7)

Procedure Number	CP PCA Replacement Order or Other Procedures
18	SA bus and/or SX bus error indicators

1. Error detection

   a. Note the exact errors and the address of the instruction being executed when the errors occurred. They are displayed in the ERROR DISPLAY and U PA ERR even though they may have been obtained from the error history table in micromemory, and even though any displayed status on the maintenance panel is cleared by subsequent operations.

   b. Source bus errors can occur for one of three reasons:

      (1) A hardware error exists in logic directly related to a sourced register.

      (2) A hardware error exists in some unsourced bus logic, causing a high signal on the bus, which interferes with the data from some other validly sourced register. This condition is known as bus interference.

      (3) A hardware error exists between the source bus and the logic which detects source bus parity errors. This is condition is known as A1/A2 interference.

2. Corrective Action

   Refer to Section 2 of DR2547.

19 Unexpected error combinations

1. Error detection

   This condition indicates that an unexpected combination of errors occurred or that multiple entries into the error-handling routine were made. The latter possiblity is more likely. Note that an intermittent DC power fault can cause multiple entries (SAL, SXU, SXL, MLO, ERR ACK).

Figure B-2. Corrective Action for CP Hardware Faults (Sheet 3 of 7)

Procedure Number	CP PCA Replacement Order or Other Procedures
19	Unexpected error combinations (cont)

2. Corrective action

Refer to DR2547 or locate ERROR DISPLAY most similar to those listed in Figure A-1 and perform corresponding procedure. Submit a DSUR to report information about unexpected error combination solution to problem.

20 Resume Error

1. Error detection

a. This error can be caused by software or by a hardware failure. In fact, when SYSTEM RESET is pressed, RESUME is an expected response during the first few seconds of execution in the CP PROM. At other times, software may initiate RESUME errors during attempts to access local storage (LS) array PCAs or banks which are not configured.

b. If SYSTEM RESET was pressed recently and bits 24 through 31 of the GENERAL DISPLAY continually show hexadecimal values 11, 21, or 31, then the CP, LS, or LOADER CLC may be experiencing a hardware fault.

c. If several CPs and CLCs are experiencing unexpected faults, then LS is the most likely source of the problem. For such faults, execute the LS micro- diagnostic LSTOR in DLI mode (see Section 9 of DR2547).

NOTE

Faults which appear to be in one CP can be in the ribbon cable interconnecting LS ports of different LS banks in different DCP/40 cabinets, or in either terminator at the ends of the LS-port bus.

Figure B-2. Corrective Action for CP Hardware Faults (Sheet 4 of 7)

Procedure Number	CP PCA Replacement Order or Other Procedures
20	Resume error (cont)

2. Corrective action

If it appears that the CP is the only processor experiencing a fault, or if the microdiagnostics do not find any hardware problems, the PCA replacement order is: E(70%), K(20%), LS-B1(6%), LS-A2(4%). Also check the corresponding ribbon cables and LS-port bus terminators.

21 Memory (local storage) lockout (MLO) error

1. Error detection

This error can be caused by a hardware error or by macrolevel software. As a software problem, it relates to unauthorized attempts to access specified segments of code, to write where a read-only is permitted, to read where a write-only is permitted, etc.

2. Corrective action

If software is not the source of the problem, the CP PCA replacement order is: E(80%), B(15%), K(4%), X(1%).

22 Error acknowledge from local storage

1. Error detection

a. Unlike RESUME and MEM LOCKOUT, ERR ACK is never an indication of a software problem. There are three hardware errors which result in an ERR ACK being passed to a processor from local storage (LS). They are:

(1) A multiple-bit flip is detected in an LS word (32 data bits plus 7 check bits).

(2) A parity error is detected in address/control information passed from the processor to LS.

Figure B-2. Corrective Action for CP Hardware Faults (Sheet 5 of 7)

Procedure Number	CP PCA Replacement Order or Other Procedures
22	Error acknowledge from local storage (cont)

(3) A parity error is detected in write-data passed from the processor to LS.

b. For LS-detected, multiple-bit flip errors, the hardware fault is in LS rather than the CP. Execute the LS microdiagnostic LSTOR in DLI mode (see Section 9 of DR2547) and specify the parameter requesting a display of all single- and multiple-bit flips.

c. For LS-detected parity errors in CP-to-LS address/control information or write-data, the hardware fault can be in the LS or CP. If several CPs and/or CLCs are experiencing faults, then LS is the most likely problem source. For such faults, execute the LS microdiagnostic STOR in DLI mode (see Section 9 of DR2547).

NOTE

Faults which appear to be in one CP can be in the ribbon cable interconnecting the LS ports of different LS banks in different DCP/40 cabinets, or in either terminator at the ends of the LS-port bus.

2. Corrective Action

a. If it appears that this CP is the only processor experiencing a fault, or if the microdiagnostics do not find any hardware problems, check the corresponding ribbon cables and LS-port bus terminators are suspect, as well as the PCAs which are noted in one of the following conditions:

Figure B-2. Corrective Action for CP Hardware Faults (Sheet 6 of 7)

Procedure Number	CP PCA Replacement Order or Other Procedures
22	Error acknowledge from local storage (cont)

(1) If the ERR ACK is caused by bad parity in the address/control information and the ERR ACK occurs during normal operation (assumes that relative/virtual addressing is taking place), PCA replacement order is: D(28%), F1(22%), F2(22%), B(15%), LS-B1(4%), LS-B0(2%), LS-B2(2%), LS-B3(2%), K(2%), E/X/A1/A2(1%).

(2) If the ERR ACK is caused by bad parity in the address/control information and the ERR ACK occurs early in a boot operation (assumes absolute addressing is taking place), or if the ERR ACK is caused by bad parity in the write-data, the PCA replacement order is: F1(36%), F2(36%), D(15%), LS-B1(4%), LS-B0(2%), LS-B2(2%), LS-B3(2%), K(2%), E/A1/A2/(1%).

23	No lit ERROR DISPLAY indicators

Refer to the microdiagnostics manual, DR2547.

Figure B-2. Corrective Action for CP Hardware Faults (Sheet 7 of 7)

B.3. EIA Procedure for CLC Hardware Faults

The following procedure assumes use of the correct CLC maintenance panel and the correct setting of the CLC SELECT switches associated with the faulty CLC.

NOTE

DCP/40 systems with more than four CLCs have separate CLC maintenance panels for each group of four CLCs.

DCP/20 systems with more than one CLC have separate CLC maintenance panels.

1. Set PANEL ENABLE switch up (enabled) and RESTART switch down (disabled). All other switches should be down.
2. Compare ERROR DISPLAY indicators on CLC maintenance panel to those listed in Figure B-3. Where the indicators match the figure, note the procedure. The first item in columns 2 through 4 refer to the DCP/20.
3. Using the procedure number from Figure B-3 as an index into Figure B-4, perform the corrective action indicated.

L BUS	MI/or U INST	RSE/or STACK EVEN	RSO/or STACK ODD	RESUME	ERR ACK	Procedure Number Figure B-4
		No lit indicators Multiple errors				8
L						7
	L					1
		L				2
			L			3
				L		4
					L	5
						6

Note: L = Lit.

Figure B-3. DCP/20 and DCP/40 CLC Error Displays

Procedure Number	CLC PCA Replacement Order or Other Procedures
1	L-bus error LM(40%), R(30%), X(20%), X-R cable(10%). LM represents the one-to-three PCA line module which was sending data to the CLC when the error was detected. Error information in the error history table indentifies the specific LM in the bottom four bits of TR. Execute the appropriate LM microdiagnostic to determine whether the LM is, in fact, the source of the fault. If an attempt to load microdiagnostics is unsuccessful, the LM probability is greatly reduced because L-bus errors are disabled during PROM execution. (Other errors can be encountered; in particular, PROM-indicated checksum or type errors are likely.)
2	Microinstruction error M(60%), L(30%), X(5%), E(5%)
3	Stack-even error CE(60%), SPE-Q(12%), LS-B1(8%), LS-B0(4%), LS-B2(4%), LS-B3(4%), SPE-U(3%), X(3%), P(2%). If several CPs and/or CLCs are experiencing faults, LS is the most likely source of the problem. For such faults, execute the LS microdiagnostic LSTOR in DL1 mode (see Section 9 of DR2547 for DCP/40 and Section 6 of DR2555 for DCP/20). If a storage port expander (SPE) is common to all failing processors, check the SPE PCAs for faults. Re-cable to run only CLC0, bypassing the SPE for isolation. NOTE Faults which appear to be in one SPE or in one CLC not attached to any SPE) can be in the ribbon cable from that SPE (CLC) to the corresponding LS port, or in the ribbon cable interconnecting the LS ports of different LS banks in different DCP/20 or DCP/40 cabinets, or in either terminator at the ends of the LS-port bus.

Figure B-4. Corrective Action for CLC Hardware Faults (Sheet 1 of 5)

Procedure Number	CLC PCA Replacement Order or Other Procedures
4	Stack-odd error

CE(60%), SPE-Q(12%), LS-B1(8%), LS-B0(4%), LS-B2(4%), LS-B3(4%), SPE-U(3%), X(3%), P(2%).

If several CPs and/or CLCs are experiencing faults, LS is the most likely source of the problem. Execute the LS microdiagnostic LSTOR in DL1 mode (see Section 9 of DR2547 for DCP/40 or Section 6 of DR2555 for DCP/20). If a storage port expander (SPE) is common to all of the failing processors, then check the SPE PCAs for faults.

NOTE

Faults which appear to be in one SPE (or in one CLC not attached to any SPE) can be in the ribbon cable from that SPE (CLC) to the corresponding LS port, or in the ribbon cable interconnecting the LS ports of different LS banks in different DCP/20 or DCP/40 cabinets, or in either terminator at the ends of the LS-port bus.

5 Resume error

1. Error detection

   a. This error can be caused by software or by a hardware failure. In fact, when SYSTEM RESET is pressed, RESUME is an expected response during the first few seconds of execution in the CLC PROM. (Note: This is true only for LOADEE CLCs.)

   b. If SYSTEM RESET was pressed recently and bits 8 through 5 of the REGISTER DISPLAY continually show hexadecimal 03, then the CLC, LS, or the LOADER CLC may be experiencing a hardware fault.

Figure B-4. Corrective Action for CLC Hardware Faults (Sheet 2 of 5)

Procedure Number	CLC PCA Replacement Order or Other Procedures
5	Resume error (cont)

c. If several CPs and/or CLCs are experiencing faults, LS is the most likely source of the problem. Execute the LS microdiagnostic LSTOR in DL1 mode (see Section 9 of DR2547 for DCP/40 and Section 6 of DR2555 for DCP/20). If an SPE is common to all failing processors, then check the SPE PCAs for faults.

NOTE

Faults which appear to be in one SPE (or in one CLC not attached to any SPE) can be in the ribbon cable from that SPE (CLC) to the corresponding LS port, or in the ribbon cable interconnecting the LS ports of different LS banks in different DCP/20 or DCP/40 cabinets, or in either terminator at the ends of the LS-port bus.

2. Corrective action

If it appears that this CLC is the only processor experiencing a fault, or if the microdiagnostics do not find any hardware problems, the PCA replacement order is: E(30%), P(25%), CE(20%), CO(10%), L(6%), SPE-U(3%), LS-B1(3%), LS-A2(2%), X(1%). Also check the corresponding ribbon cables and LS-port bus terminators.

6 Error acknowledge from local storage

1. Error detection

a. Unlike RESUME, ERR ACK is never an indication of a software problem. There are three hardware errors which result in an ERR ACK being passed to a processor from local storage (LS). These are:

(1) A multiple-bit flip is detected in an LS word (32 data bits plus 7 check bits).

Figure B-4. Corrective Action for CLC Hardware Faults (Sheet 3 of 5)

Procedure Number	CLC PCA Replacement Order or Other Procedures
6	Error acknowledge from local storage (cont)

(2) A parity error is detected in address/control information that was passed from the processor to LS.

(3) A parity error is detected in write-data that was passed from the processor to LS.

b. For LS-detected, multiple-bit flip errors, the hardware fault is in LS rather than the CLC. Execute the LS microdiagnostic LSTOR in DL1 mode (see Section 9 of DR2547 or Section 6 of DR2555) and specify the parameter requesting a display of all single- and multiple-bit flips.

c. For LS-detected parity errors in CLC-to-LS address/control information or write-data, the hardware fault can be in LS, an SPE, or the CLC. If several CPs and/or CLCs are experiencing faults, LS is the most likely source of the problem. Execute the LS microdiagnostic LSTOR in DL1 mode (see Section 9 of DR2547 or Section 6 of DR2555). If an SPE is common to all failing processors, then check the SPE PCAs for faults.

NOTE

Faults which appear to be in one SPE (or in one CLC not attached to any SPE) can be in the ribbon cable from that SPE (CLC) to the corresponding LS port, or in the ribbon cable interconnecting the LS ports of different LS banks in different DCP/20 or DCP/40 cabinets, or in either terminator at the ends of the LS-port bus.

Figure B-4. Corrective Action for CLC Hardware Faults (Sheet 4 of 5)

Procedure Number	CLC PCA Replacement Order or Other Procedures
6	Error acknowledge from local storage (cont)

2. Corrective action

If it appears that this CLC is the only processor experiencing a fault, or if the microdiagnostics do not find any hardware problems, the PCA replacement order is: CE(35%), CO(25%), SPE-Q(12%), LS-B1(8%), LS-B0(4%), LS-B2(4%), LS-B3(4%), E(4%), SPE-U(3%), X(1%). Also check the corresponding ribbon cables and LS-port bus terminators.

7 Unexpected error combinations

This condition indicates that an unexpected combination of errors occurred or that multiple entries into the error-handling routine were made. The latter is more likely and can be isolated as follows:

Locate ERROR DISPLAY most similar to those listed in Figure A-3 and perform corresponding procedure. Submit a DSUR to report the unexepected error combination and solution. If further isolation is required, refer to Section 9 of DR2547 for the DCP/40 or Section 6 of DR2555 for the DCP/20.

8 No lit ERROR DISPLAY indicators

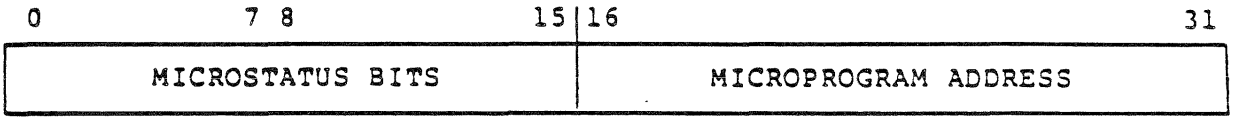
Refer to DR2547 for the DCP/40 or DR2555 for the DCP/20.

Figure B-4. Corrective Action for CLC Hardware Faults (Sheet 5 of 5)

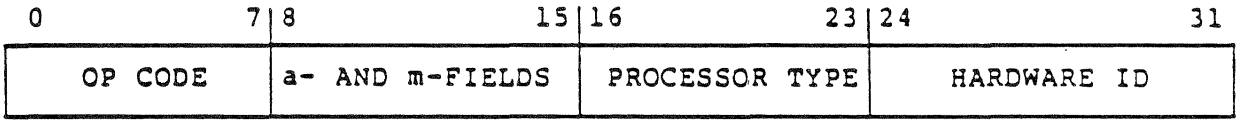
B.4. SCR 14 and SCR 15 (CP Exigent Hardware Conditions - PNO)

Communications processor exigent hardware conditions are unrecovered hardware errors that must be analyzed before processing continues. They result in a forced call to procedure number 0 (PNO). Equipment-dependent supplementary status is loaded into SCR 14 and SCR 15, provided that the hardware error condition does not disable micro level operation. The bit formats of SCR 14 and SCR 15 are illustrated in Figure B-5. SCR 14 bit definitions are given in Figure B-6.

SCR 14



SCR 15



OP CODE AND a- AND m-FIELDS OF THE MACROINSTRUCTION THAT FAILED

Figure B-5. SCR 14 and SCR 15 Bit Format

NOTE

See paragraph describing DCP/40 error OP code changes for SCR 15 and SCR 13.

SCR 14 Bits	DCP/10	DCP/20*	DCP/40
0	Master ALU compare error	Translator register**	ALU compare error 1 (bits 4-7 or 12-15)
1	Master ALU A register parity error	Translator register	ALU compare error 2 (bits 0-3 or 8-11)
2	Master ALU B register parity error	Translator register	Source A, bus upper parity error
3	Master ALU microinstruction error	Translator register	Source A, bus lower parity error
4	Checker ALU compare error	Translator register	Source X, bus upper parity error
5	Checker ALU A register parity error	Translator register	Source X, bus lower parity error
6	Checker ALU B register parity error	Translator register	R1 error (R upper) parity error
7	Checker ALU microinstruction error	Translator register	R2 error (R lower) parity error
8	B-chip microinstruction error	Not Used	Microprogram address upper parity error
9	C-chip microinstruction error	L-bus parity error	Microprogram address lower parity error

*If bits 9 - 14 on the DCP/20 are all zero, then an illegal hardware vector occurred as defined by the microprogram address.

Microprogram Address	Description
0148C	Power fault interrupt
01483	Old-mode I/O interrupt
0358B	Illegal emulate next instruction vector
03593	Illegal emulate next instruction vector
0359B	Illegal emulate next instruction vector

**Bit 0 is set for processor mode. AF (hex) is the normal setting.

Figure B-6. SCR 14 Bit Definitions (Sheet 1 of 2)

SCR 14 Bits	DCP/10	DCP/20*	DCP/40
10	C-chip microinstruction error address parity error	Microinstruction parity error	Microinstruction parity error
11	D-chip local storage range error	Register stack byte 0 or 2 parity error	Emulation control word parity error
12	D-chip local storage double-bit error	Register stack byte 1 or 3 parity error	Micro mark stack error
13	D-chip memory data register write error	Storage resume/ time-out (unimplemented/non-responding storage)	Storage resume/time-out(unimplemented/ non-responding storage)
14	D-chip microinstruction error	Storage error acknowledge (uncorrectable storage/ storage I/F error	Storage error acknowledge (uncorrectable storage/ storage I/F error
15	G-chip micorinstruction error	Not Used	Memory lockout error**
16-31	Address of microinstruction that encountered error	Address of microinstruction that encountered error	Address of microinstruction that encountered error

*If bits 9 - 14 on the DCP/20 are all zero, then an illegal hardware vector occurred as defined by the microprogram address.

Microprogram Address	Description
0148C	Power fault interrupt
01483	Old-mode I/O interrupt
0358B	Illegal emulate next instruction vector
03593	Illegal emulate next instruction vector
0359B	Illegal emulate next instruction vector

**Storage protection violation; actually reported through PN1 unless combined with other errors.

Figure B-6. SCR 14 Bit Definitions (Sheet 2 of 2)

B.5. SCR 13 (CP Specification Exceptions - PN1)

Communications processor specification exceptions are conditions which do not comply with architectural requirements. To provide analysis of these exceptions, status is passed to software by a forced call to procedure number 1 (PN1). Identical supplementary status is provided for all models. The status is contained in SCR 13, illustrated in Figure B-7. Definitions of exception conditions are provided in Figure B-8.

Type 2 specification exceptions are detected by hardware in the DCP/40 and by microcode with hardware assistance in the DCP/20 and the DCP/10. That difference can produce some unpredicatable model-dependent results with type 2 specification exceptions. All other conditions are detected by the microcode and are treated the same in all models. When multiple errors occur in the same instruction, each implementation checks for conditions in a different (although architecturally correct) sequence; consequently, the error condition that is detected first can differ, resulting in different status information.

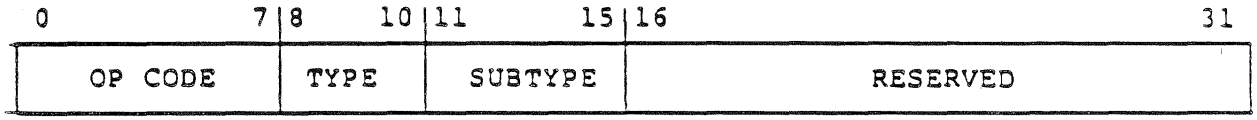


Figure B-7. SCR 13 Bit Format

NOTE

See paragraph describing DCP/40 error OP code changes for SCR 15 and SCR 13.

Exception Type	Condition Subtype*	Description
1	1	Illegal instruction
1	2	Privileged instruction
2	10000	Storage protection length violation
2	11XXX	Storage protection segment not present violation
2	1X1XX	Storage protection execution violation
2	1XX1X	Storage protection read violation
2	1XXX1	Storage protection write violation
3	1	Procedure segment table length violation
3	2	System segment table length violation
3	3	Procedure table length violation
3	4	Gated procedure list length violation
3	5	Queue list length violation
3	6	Link area length violation
3	7	Process control stack underflow
3	8	Process control stack overflow
3	9	Lock length violation
3	10	Lock length violation
4	1	Procedure blocked
4	4	Segment descriptor present (should not be)
4	5	Segment descriptor registers 0 thru 3 (SDR0 - SDR3) illegally specified
4	6	Static segment mask bit not set by this procedure
4	7	Segment descriptor not present (should be)
4	8	Segment descriptor not allocatable
4	10	Queue access violation
4	11	Queue type wrong for activity
4	12	Message control table wrong segment descriptor structure
4	19	Allocate/deallocate illegal length
4	20	Return/subroutine return illegal for process control stack
4	24	Cannot unlock, not locked
4	25	Cannot lock, locked by another
4	26	Lock count overflow/underflow
4	29	Wrong segment structure
4	30	Address not on 128/4K-byte boundary

*Subtypes for Type 2 are binary notation. All others are decimal equivalents.

Figure B-8. SCR 13 Bit Definitions

B.6. SCR 11 (CP Process Control Conditions - PN4)

Communications processor process control conditions are not real errors but require operating system intervention for continued operation. They result in a forced call to procedure number 4 (PN4) and include the inability to satisfy a dynamic procedure linkage during call, return, and load segment instructions, the inability to allocate space from a specified buffer pool through an allocate instruction, or the inablity to satisfy lock conditions while executing LOK or Clok instructions. Identical supplementary status is provided for all models. Status is contained in SCR 11, which is illustrated in Figure B-9 and defined in Figure B-10.

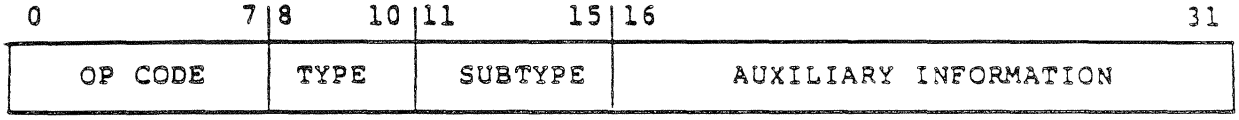


Figure B-9. SCR 11 Bit Format

Type	Subtype	Instruction/Exception Condition	Auxiliary Information
0	1	ICALL/Call/RTN: [SST{SSN}.SD] not present	Procedure number
0	2	Reserved	
0	3	LSEG: [SST{SSN}.SD] not present	System segment mber
0	4	ALLOC: no space in buffer pool	0
0	5	LOK: lock is locked by another	Lock ID
0	6	Clok: wait bit is set	Lock ID
0	7	Software breakpoint	AM

Figure B-10. SCR 11 Bit Definitions

B.7. DCP/40 Error OP Code Changes

To improve performance, the CP instruction operation (OP) code can be changed during the emulation of an instruction by taking advantage of routines used by other instructions. Because of this manipulation, the OP code that is reported in SCR 15 (hardware error), SCR 13 (specification exception), and SCR 9 (restart condition) can differ from the actual operation causing the error. Figure B-11 itemizes the OP codes which are changed and the corresponding OP codes which appear in the status register.

Instruction	Original OP Code	Reported OP Code
SBU	0E	23
SBL	16	23
RTN	1D a = 0	80
CALL	1F a = 0	80
ICALL	1F a = 8	80
JWB	1F a = 9	80
PC	1F a = A	86
REX	76	Any
various jumps	82	80
various jumps	83	80 or 63
XJ	87	86
JLR	8B	8A
JZ	93	92
JNZ	97	96
JP	9B	9A
JN	9F	9E
LSDM	D6	80
LGRM	D7	80
LPCR E4	80	
LPC	E6	80
LPCM	F6	80
Forced Call	Any	80 or 00
Interruptible by clock (MBMI, SBMI, CIBMI)	BC, B1, B4	80 or 00

Figure B-11. DCP/40 CP Error OP Code Changes

B.7. Port Processor State Item (PP Hardware Error Conditions and Specification Exceptions)

The port processor state item buffer holds status information for unrecovered PP hardware errors and PP specification exceptions. The state item is queued to SQL3 for hardware errors and to SQL4 for exception conditions. Figure B-12 illustrates the format of the buffer and Figure B-13 defines its content. Note the differences for the DCP/10.

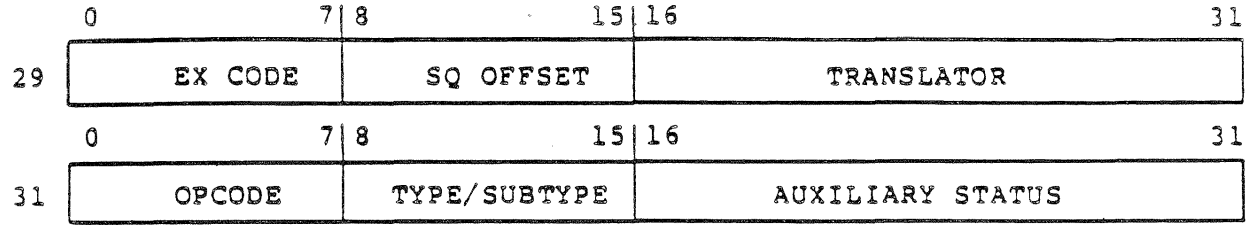
If the supplementary status indicates a hardware error and the error status is non-zero, isolate the cause of the problem with the EIA procedures. If a hardware error is indicated and the status is zero, note the microprogram address and the PPID (word 30). They identify the failing port.

	0 7	8 15	16 31
0	PROGRAM ADDRESS OUTPUT (PAO)		RESERVED
1	OUTPUT INSTRUCTION		
2	RESERVED		
3	RESERVED	OUTPUT INDEX	RESERVED
4	PROGRAM ADDRESS INPUT (PAI)		RESERVED
5	INPUT INSTRUCTION		
6	RESERVED		
7	RESERVED	INPUT INDEX	RESERVED
8	BIO	OUTPUT MESSAGE CONTROL TABLE	
9	BII	INPUT MESSAGE CONTROL TABLE	
10	RESERVED	LINE OUTPUT	
11	RESERVED	LINE INPUT	
12 THRU 23	RESERVED		
24 25 26 27	SD0 SD1 SD2 SD3	(FIXED SPACE)	
28 29	RESERVED		
30	PORT PROCESSOR ID	MICROPROGRAM ADDRESS	
31	SUPPLEMENTARY STATUS (SEE BELOW)		

0 7	8 10	11 15	16 23	24 31
OP CODE	TYPE	SUBTYPE	TRANSLATOR	STATUS INFORMATION

Figure B-12. Port Processor State Item Buffer Format
(Sheet 1 of 2)

DCP/10 CHANGES TO WORDS 29 AND 31



EX CODE: Exception Code
0 - Specification exception (same as DCP/40, DCP/20)
1 - Hardware error
2 - Illegal line module vector
3 - Recovery condition (details not included)

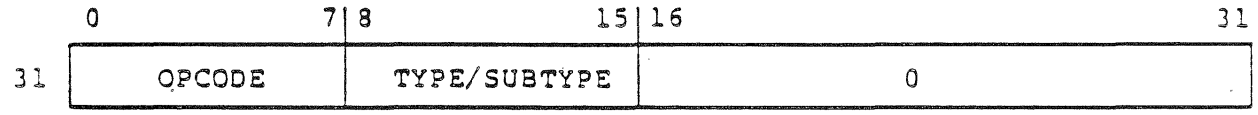
SQ OFFSET: Byte offset to system queue where item is posted.

TRANSLATOR: Translator register

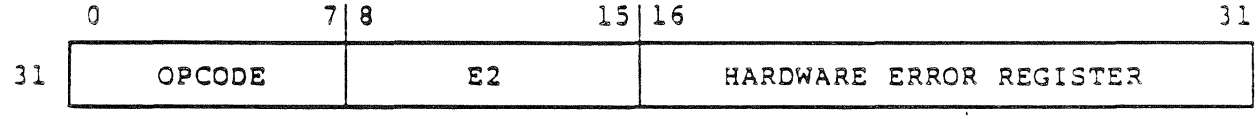
TYPE/SUBTYPE: Determined by EX CODE

AUXILIARY STATUS: Determined by EX CODE

EX CODE 0:



EX CODE 1:



EX CODE 2:

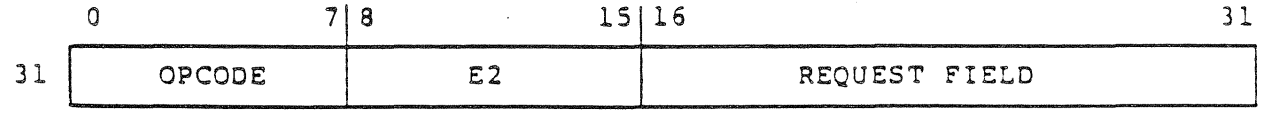


Figure B-12. Port Processor State Item Buffer Format
(Sheet 2 of 2)

Term	Definition
Reserved	Area can contain equipment-dependent microprocessor registers.
PAO	Program address (output chain) of current instruction when error occurred and either four or eight bytes depending on error and equipment type.
Output Instruction	Macroinstruction being executed in output chain
Output Index	Queue list index associated with output chain
PAI	Program address (input chain) of current instruction when error occurred and either four or eight bytes depending on error and equipment type.
Input Instruction	Macroinstruction being executed in input chain
Input Index	Queue list index associated with input chain
BIO	Output back item flag. Non-zero if output message control table (MCT) is a back item on a queue.
Output MCT	Real address of the output MCT, if non-zero.
BII	Input back item flag. Non-zero if input MCT is a back item on the queue.
Input MCT	Real address of input MCT, if non-zero.
Line Output	Non-zero value represents an MCT re-queued by RIX or RAOX instruction if one of them was executing in output chain and the error status is for specification exception of type 4/subtype 10, type 4/subtype 11, type 4/subtype 13, or type 3/ subtype 5.
Line Input	Non-zero value represents an MCT re-queued by RIX or RAOX instruction if one of them was executing in input chain and the error status is for specification exception of type 4/subtype 10, type 4/subtype 11, type 4/subtype 13, or type 3/ subtype 5.

Figure B-13. Port Processor State Item Definitions (Sheet 1 of 6)

Term	Definition
SD0 thru SD3	Segment descriptors defining port processor's fixed space (from the interface control table)
PPID	Port processor identifier
Microprogram Address	Microprogram address where error occurred
Translator	Bit 16: Set for CLC processor mode; clear for I/O mode. Bit 17: L-bus transfer direction. Set for L-bus input; clear for L-bus output. Bit 18: clear for line module data mode; set for line module command mode. Bit 19: Set for input port; clear for output port. Bits 20 - 23: Port number
Supplementary Status	Status indicating the cause for posting the state item: a specification exception or a port processor hardware error.

Figure B-13. Port Processor State Item Definitions (Sheet 2 of 6)

Supplementary Status (cont)	Type	Subtype	Status Information	Description
		DCP/10, DCP/20, DCP/40 Specification Exceptions		
	1	1		Illegal instruction
	2	10000		Storage protection length violation
	2	11XXX		Storage protection segment not present
	2	1X1XX		Storage protection execution violation
	2	1XX1X		Storage protection read violation
	2	1XXX1		Storage protection write violation
	3	5		Queue list length violation
	3	7		Call/return stack underflow
	3	8		Call/return stack overflow
	4	10		Queue access violation
	4	11		Queue type wrong for activity
	4	13		MCT on wrong side for re-queue
	4	14		MCTs are both the same (Q0I, QII)
	4	15		MCT in use and not a back item
	4	16		Designated MCT nonexistent
	4	17		Designated MCT is a back item
	4	18		MCT not the same
	4	21		"C" bit switched off
	4	22		Halt instruction executed
	4	23		Change environment instruction executed
	4	28		Buffer reference error
	4	31		Background mode removed buffer with address of zero.

Figure B-13. Port Processor State Item Definitions (Sheet 3 of 6)

Supplementary Status (cont)	Type	Subtype	Status Information	Description
		DCP/20 and DCP/40 Hardware Errors		
	7	2	Bit 25 set	L-bus parity error
	7	2	Bit 26 set	Microinstruction parity error
	7	2	Bit 27 set	Register stack (byte 0 or 2) parity error
	7	2	Bit 28 set	Register stack (byte 1 or 3) parity error
	7	2	Bit 29 set	Storage resume/time-out (unimplemented/non-responding storage
	7	2	Bit 30 set	Storage error acknowledge (uncorretable storage/ storage interface errors)

Bits 24 and 31 are not used. If bits 25 through 30 are all zero, then an illegal hardware vector occurred. The microprogram address indicates the error source.

Microprogram Address	Description
01402	Line module generated error-out vector
0140A	Illegal IOP vector
01412	Line module generated error-in vector
01414	Line module raised illegal chain or data request
0141A	Illegal IOP vector
01422	Illegal IOP vector
0142A	Illegal IOP vector
01432	Illegal IOP vector
0143A	Illegal IOP vector
0146A	Illegal IOP vector
01472	Illegal IOP vector
01478	Illegal IOP vector
0148C	Power fault
014AC	Processor clock
014B3	Old-mode I/O vector
01512	Illegal IOP vector (emulate branch)
01522	Illegal IOP vector (emulate branch)
01532	Illegal IOP vector (emulate branch)

Figure B-13. Port Processor State Item Definitions (Sheet 4 of 6)

Supplementary Status (cont)	Type	Subtype	Status Information	Description
			DCP/10 Hardware Errors	
			EX CODE = 1	
			Hardware Error Reg.	
	-	-	All bits=0	L-bus parity error
	-	-	Bit 16 set	Master ALU compare error
	-	-	Bit 17 set	Master ALU A register parity
	-	-	Bit 18 set	Master ALU B register parity
	-	-	Bit 19 set	Master ALU microinstruction error
	-	-	Bit 20 set	Checker ALU compare error
	-	-	Bit 21 set	Checker ALU A register parity
	-	-	Bit 22 set	Checker ALU B register parity
	-	-	Bit 23 set	Checker ALU microinstruction error
	-	-	Bit 24 set	B-chip: microinstruction error
	-	-	Bit 25 set	C-chip: microinstruction error
	-	-	Bit 26 set	C-chip: microprogram address parity
	-	-	Bit 27 set	D-chip: local storage range error
	-	-	Bit 28 set	D-chip: local storage double-bit error
	-	-	Bit 29 set	D-chip: MDR write error
	-	-	t 30 set	D-chip: microinstruction error
	-	-	Bit 31 set	G-chip: double-bit micro-memory error

Figure B-13. Port Processor State Item Definitions (Sheet 5 of 6)

Supplementary Status (cont)	Type	Subtype	Status Information	Description
			DCP/10 Illegal Line Module Vector	
			EX CODE = 2	
			Request Field	(LM Vector)
	-	-	00 (0000)	Not implemented
	-	-	01 (0001)	Not implemented
	-	-	02 (0010)	Not implemented
	-	-	03 (0011)	Not implemented
	-	-	04 (0100)	Not implemented
	-	-	05 (0101)	Not implemented
	-	-	06 (0110)	LM hardware error
	-	-	07 (0111)	L-bus parity error
	-	-	08 (1000)	Not implemented
	-	-	09 (1001)	Not implemented
	-	-	0A (1010)	Not implemented
	-	-	0B (1011)	Not implemented
	-	-	0100 (XXXX)	LM request is imple-mented but illegal

Figure B-13. Port Processor State Item Definitions (Sheet 6 of 6)