UNISYS

BT 3200 Series 324X/326X/328X Magnetic Tape Controller

Theory of Operation Manual

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EDITION RECORD		
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Model Number Cross Reference Table

UNISYS Model No.	Description Model No.
3241	F617A1
3242	F617A2
3244	F617B
3243	F617E
3261	F618A1
3262	F618A2
3266	F618B
3265	F618E
3281	M2436-1
3282	M2436-2
3288	M2436-8

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CHAPTER 1 INTRODUCTION

1.1 Functions

The 324X/326X/328T magnetic tape subsystems are used as an external storage of the data processing unit. This manual describes only the magnetic tape control unit in the magnetic tape subsystem. Refer to the other manual for the magnetic tape unit. The magnetic tape control unit and tape unit are referred to after this as "MTC" and "MTU".

A MTC located logically between the channels and the MTUs receives and decodes control signals - commands, MTU addresses, etc. - from the channels.
It also controls read and write operation, rewind, erase and other operations for a specified MTU.

A MTU can control up to eight MTUs.

1.2 Unit Types

Table 1.1 Types of units

Unit name	Configuration
3241	MTCx1 + MTU (6250/1600 BPI, 75/125 IPS)x1
3242	MTCx2 + MTU (6250/1600 BPI, 75/125 IPS)x1 for device cross-call feature
3244	MTU (6250/1600 BPI, 75/125 IPS)x1
3243	MTU (1600/800 BPI, 75/125 IPS)x1
3261	MTCx1 + MTU (6250/1600 BPI, 125/200 IPS)x1
3262	MTCx2 + MTU (6250/1600 BPI, 125/200 IPS)x1
3266	MTU (6250/1600 BPI, 125/200 IPS)x1
3265	MTU (1600/800 BPI, 125/200 IPS)x1
3281	MTCx1 + MTU (6250/1600 BPI, 200 IPS)x1

Unit name	Configuration
3282	MTCx2 + MTU (6250/1600 BPI, 200 IPS)x1
3288	MTU (6250/1600 BPI, 200 IPS)x1

* Each MTC/MTU contains its own power supply unit.

1.3 Characteristics

Table 1.2 shows the characteristics of each unit type.

Table 1.2 Characteristics

Item \ Unit type		3241/3242	3244	3243	3261/3262	3266	3265	3281/3282	3288
Number of built-in MTCs (CH)		1/2	None		1/2	None		1/2	None
Recording density (BPI)		6250/1600		1600/800	6250/1600		1600/800	6250/1600	
Tape speed	Normal	125			75			200	
	High	200*			125*			-	
Data transfer rate (KB/S)	Normal	781/200		200/100	469/120		120/60	1250/320	
	High	1250/320		320/-	781/200		200/-	-	
IBG length (inch.)		6250 BPI; 03 1600/800 BPI: 0.6						6250 BPI; 04 1600/800 BPI; 0.6	
Tape load time (sec.)		12							
Tape rewind time (sec.)		55							
Unload time (sec.)		65							
Tape length (feet)		2400 (full reel)							
Loading feature		Auto-sledding							
Reel locking feature		Auto-hub							
Window mechanism		Auto-window							
Cartridge		Usable							
Error marker		Preset							
Maximum configuration		Up to 8 tape units							
Unit address		Fixed							
MTC cross-call		Possible with 2CH-SW option							
MTC cross-call		Possible for 2-MTC type							

* 800 BPI has no high speed function.

1.4 Configuration

Figures 1.1 and 1.2 show the subsystem configuration with a single MTC and dual MTCs, respectively.

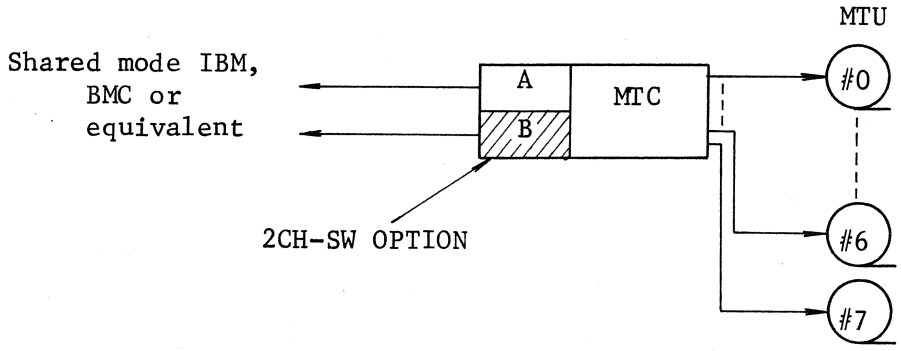


Figure 1.1 Single controller system

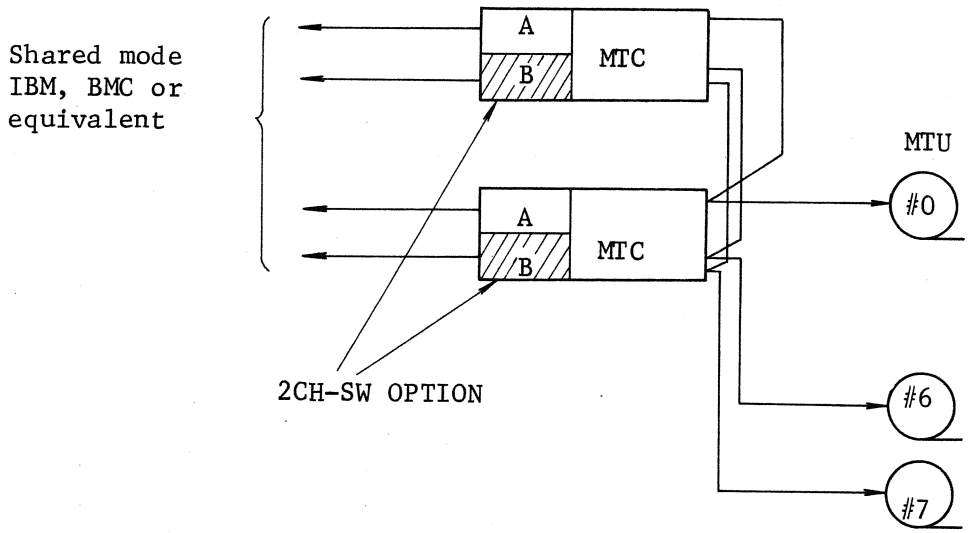


Figure 1.2 Dual controller system

CCHAPTER 2 COMMAND OPERATION

2.1 Outline

This chapter explains the logical specifications of command operations, statuses, and sense bytes in MTC.

2.2 I/O Instructions

I/O Instructions associated with subsystem are:

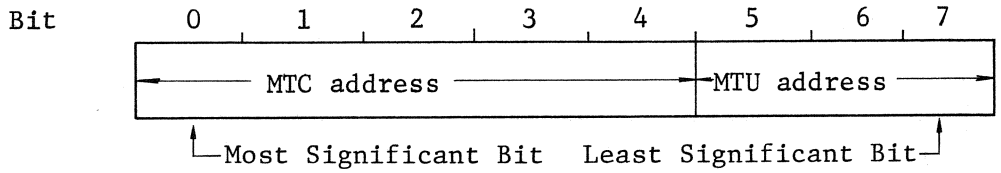
(1) SIO/SIOF .... Initiating command operation

(2) TIO .... Testing subsystem status

(3) HIO/HDV/CLRIO ... Halting I/O operation

2.3 Device Address

The device address area consists of a five-bit MTC address field and a three-bit MTU address field.



2.4 Commands

Table 2.1 outlines the types, codes, and operations of commands. TIO is a CPU Instruction, but it treats as a command in the operation between BMC and MTC.

The meanings of abbreviations used in Table 2.1 are:

. DSB .... Status byte

. TWA .... Tape warning area (the range between the EOT mark and the termination)

. UEX .... Unit exception (the unit exception bit for bit 7 of the DSB)

Table 2.1 Command operation (1/3)

Name	Hex. code	Command type	Operation
Test IO (TIO)	00		Tests the MTC/MTU for status. The result is indicated at the DSB.
Write (WRT)	01	Burst	Writes data. If data is written to the TWA, then the UEX bit is set on. A recording density flag is set up in a MTU in which a BOT is detected. The recording density is then determined on the basis of the density stored in the MTC.
Read (RD) Read Backward (BRD)	02 0C	Burst	Reads data forward (RD) and backwards (BRD). If a tape mark block is detected, then the unit exception bit is set on.
Sense (SNS)	04	Burst	Transfers 24 bytes of sense bytes indicating the cause of UCK and the status of the MTU.
Sense & Controller Reserve (CNTRSV) Sense & Controller Release (CNTRLS)	F4	Burst	Operates similarly to the SNS command after reserving/releasing a MTC from a channel if the 2CH-SW option is mounted.
Sense & Tape Unit Reserve (TURSV) Sense & Tape Unit Release (TURLS)	B4 94	Burst	Operates similarly to the SNS command after reserving/releasing a MTU from a particular path in a system with the 2CH-SW option or 2 MTCs. (*1)
Unconditional Reserve (UR)	14	Burst	Ignores and resets the exclusive control information between channel switches or MTCs, then reserves the specified MTU for its own path. Then, it operates similarly to the SNS command. (*1)

Table 2.1 Command operation (2/3)

Name	Hex. code	Command type	Operation
No Operation (NOP)	03	Non motion control	Reports CHE and DVE is the MTU is ready when it is activated.
Set 6250 BPI Mode Set 1600 BPI Mode Set 800 BPI Mode	D3 C3 CB	Non motion control	Updates the density mode register of the MTC.
Diagnostic Mode Set (DMS)	0B	Non motion control	Sets the MTC to the diagnostic mode.
Loop Write-To-Read (LWR)	8B	Burst	Reads/writes data in order to diagnose the data path of the MTC/MTU with no tape motion.
Request Track-In-Error (RTIE)	1B	Burst	Transfers error track information for one byte to the MTC. On the basis of this information, the MTC corrects the read data in next Read command operation.
Set Diagnose (SDIA)	4B	Burst	Transfers the diagnostic flag bytes (four bytes). It modifies the subsequent Write/Read command.
Sense I/O Type (SNSIO)	E4	Burst	Transfers seven-byte data to the channel unit according to the type of the MTU. (*1)
Rewind (REW)	07	Motion control dis-connect	Rewinds the tape until a BOT is encountered.
Data Security Erase (DSE)	97	Motion control dis-connect	Erases the tape until an EOT is encountered.
Space File (SPF) Backspace File (BSPF)	3F 2F	Motion control dis-connect	Moves the tape forwards/backwards until a tape mark is detected.

Table 2.1 Command operation (3/3)

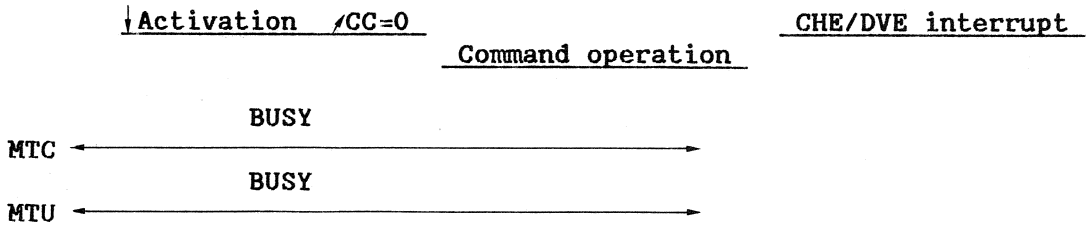
Name	Hex. code	Command type	Operation
Rewind Unload (UNL)	0F	Motion control non dis-connect	Rewinds the tape to the BOT, and unloads other tape from the columns and the machine reel. When the MTU begins to rewind, posts the DSB with DVE/UCK/CUE.
Erase Gap (ERS)	17	Motion control non dis-connect	Erases the tape by about 3.5 inches. (about 10 cm including IBG).
Write Tape Mark (WTM)	1F	Motion control non dis-connect	Erases the tape by about 3.5 inches and writes a tape mark in the rear of it.
Space (SP) Back Space (BSP)	37 27	Motion control non dis-connect	Moves the tape forwards or backwards by one block.
Set Normal Speed (SNP) Set High Speed (SHP)	83 E3	Motion control non dis-connect	Switches the MTU to the normal or high speed mode and corrects the stop position. (*2)

*1 If the MTC is set to the IBM compatible mode, these commands are rejected.

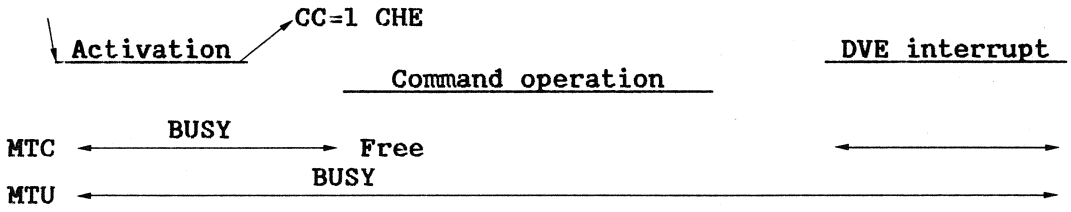
*2 If the MTU is not plugged into the High Speed support mode, these commands operate as equivalent to the NOP command.

The following outlines command operations resulting from the respective command types in Table 2.1:

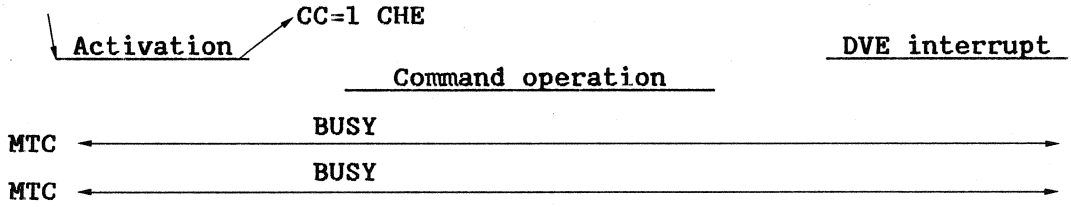
Burst command: Transfers data



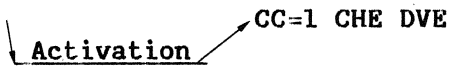
. Motion control disconnect: Transfers no data, though accompanied with tape motion



. Motion control non disconnect: Transfers no data, though accompanied with tape motion



. Non motion control: Accompanies neither tape motion nor data transfer.



2.5 Status Byte

Table 2.2 shows the bit configuration and description of the status byte. The status byte indicates the statuses of the MTC and MTU. The attention bit (bit 0) is not used in the magnetic tape subsystem.

Table 2.2 Status byte (1/2)

Bit	Name	Description
0	Attention	The magnetic tape subsystem does not use this bit. It always contains '0'.
1	Status modifier (STM)	This bit is set to '1' along with the BSY bit when a new command is issued while the MTC is busy or pending the status byte or sense byte for another MTU. (Control unit busy)
2	Control unit end (CUE)	(a) A control unit end is sent when the status is reset after a control unit busy status is responded. (b) This bit is set on when the end status byte contains a unit check or unit exception after a channel end is reported at the initial status byte.
3	Busy (BSY)	(a) This bit is set to '1' along with the status modifier bit when a new command is issued while the MTC is busy or pending the status byte or sense byte for another MTU. (b) This bit is set to '1' along with the status modifier bit when a command other than the TIO is issued to the MTU with the same address while the status byte is stacked. (c) This bit is set, when selected MTU is busy by the following reason. ° Performing the REW, DSE, SPF or BSPF command operation. ° Used by another MTC. ° Reserved by any other path. (d) This bit is set to '1' along with the DVE bit when a command other than the TIO is issued for the first time since the MTU in an intervention required status became ready, with no inquiries mode.

Table 2.2 Status byte (2/2)

Bit	Name	Description
4	Channel end (CHE)	This bit indicates that data transfer is no longer required through the interface for a channel. It is set to '1' when a burst type command is terminated or a control type command is initiated.
5	Device end (DVE)	This bit is set on when: (a) A command other than the Unload command has completed on the MTU level. (b) The Unload command has completed on the MTC level. (c) The MTU has become ready after reporting a busy or intervention required status. (d) The MTU has failed in load operation after reporting an intervention required status. (e) The MTU has become into an intervention required status after the MTU has responded a busy status or is operating by a command. (f) A command is issued for the first time since the MTU in an intervention required status becomes ready with no inquiries made.
6	Unit check (UCK)	This bit indicates that an abnormal condition is detected in a MTC or MTU. The cause of the unit check is stored into a sense byte.
7	Unit exception (UEX)	This bit indicates that a tape mark was detected while a Read/Read Backward/Space/Backspace command. It is set on when a Write/Write Tape Mark/Erase command is executed in the tape warning area.

2.6 Sense Bytes

Table 2.3 lists sense bytes.
The sense bytes consisting of 24 bytes indicate the secondary statuses of MTC and MTU.

Table 2.3 Sense bytes (1/3)

Byte	Bit 0	1	2	3	4	5	6	7
0	Command Reject (U)	Intervention Required (U)	Bus Out Check (U)	Equipment Check (U)	Data Check (U)	Overrun (U)	Word Count Zero (U)	Data Converter Check "Zero" (Not Used)
1	Noise (E) (D)	TU Status A	TU Status B	7 Track "Zero" (Not Used)	Load Point (U)*	Write Status	File Protect	Not Capable (U)
2	Error track 0-7							
3	VRC Check (D)	Multiple Track Error LRC Check (D)	Skew Error (D)	End Data/ CRC Check (D)	Envelope Check (D)	1600 BPI	Backward	P-Compare (D)
4	MP Hard-ware Error (E)	Reject TU (E)	Tape Indicator	Write Trigger VRC (D)	Not Used	Loop Write-to-Read	TU Check (E)**	Not Used
5	New Subsystem "Zero"	"1"	Write Tape Mark Check (E)	ID Burst Check (U)	Start Read Check (D)	Partial Record (D)	Postamble Error (D)	Error Count Overflow (D)

Note: (U) Sets "Unit Check"
(E) Sets "Equipment Check"
(D) Sets "Data Check"
(U)* Becomes a cause of "Unit Check" while commands belonging to Back category are being executed.
(E)** Becomes a cause of "Equipment Check" except Load Failure.

Table 2.3 Sense bytes (2/3)

Byte	Bit 0	1	2	3	4	5	6	7
6	7 Track "Zero" (Not Used)	Write Circuit Alarm (E)	Dual Density	TU Not set 1600 BPI	6250 BPI TU	Tape Unit Model 101: 200 ips MTU 100: 125 ips MTU 011: 75 ips MTU		
7	Misc. Error	Tape Loop Alarm Left	Tape Loop Alarm Right	Reset Key	DSE	Fuse Alarm	Air Bearing Alarm	Load Failure
8	IBG Detect (D)(E)	Error Track P	Not Used	Early Begin Readback Check (D)	SAGC Check (E)(D)	Slow Begin Readback Check	Slow End Readback Check (D)	Velocity Retry
9	1- or 2- Track Correction	Velocity Change (D)	Channel Buffer Check (D)	CRC III Check (D)	6250 BPI MTC	Always "One"	TU Reserved	CU Reserved
10	Status Tag Response Check (E)	Command Tag Response Check (E)	Control Tag Response Check (E)	No Block Detected (E)	Dynamic Reversal (E)	Tacho Start Failure (E)	Not Used	Velocity Check (E)
11	Read/Write Overrun (E)	Missing Position (E)	TAG In Response Check (E)	Register Parity Error (E)	MP Detect Error (E)	CU ROM Parity Error (E)	MP Trapped	TU ROM Parity Error

Table 2.3 Sense bytes (3/3)

Byte	Bit 0	1	2	3	4	5	6	7
12	Erase Current on	TU Action	Inner Backward	Write Current on	ARA 65% slice	High speed Mode	Inner 1600 BPI	Tape Mark Detected
13	Error Count							
14	Not Used							
15	High Speed Feature	Skip File Feature	Not Used	Not Used	TU Unique ID (High Order)			
16	TU Unique ID (Low Order)							
17	2-Channel Switch Feature	800 BPI Feature	16-Drive Option	Not Used	CU EC Level			
18	SAGC Count				TU EC Level			
19	TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0
	Primed For Device End							
20	Not Used							
21	MTU Error Code							
22	Field Replaceable Unit							
23	Field Replaceable Unit							

Description of the Sense Bytes. (Table 2.3)

a. Sense Byte 0 (Any bit set causes "Unit Check" status)

Bit 0 COMMAND REJECT (CRJ). Command Reject is set:

- If a Write, Write Tape Mark, or Erase command is issued to a file protected tape unit.
- If an undefined command is issued.
- If a Data Security Erase command is issued without being chained to an Erase command.
- If a Sense & Controller Reserve or Sense & Controller Release command is issued to a control unit which does not have the Two-Channel Switch feature, or is not the first command in a chain.
- If a Sense & Tape unit Reserve command, Sense & Tape Unit Release command or Unconditional Reserve command is not issued by the channel as first command in a chain.
- If one of following commands is issued to the controller in a "Compatible Mode".

  Sense & Tape Unit Reserve command
  Sense & Tape Unit Release command
  Unconditional Reserve command
  Sense I/O type command

Bit 1 INTERVENTION REQUIRED (IRQ). Intervention Required is set:

- If the selected tape unit is "Off Line".
- If a nonexistent tape unit is selected.
- If a tape unit becomes "Not Ready" during an operation.

Bit 2 BUS OUT CHECK (BOC). Bus Out Check is set: If a parity error is detected in a command or Data Byte received from the channel. If the control unit detects a temporary error, BOC may be set with MP hardware error (sense byte 4, bit 0).

Bit 3 EQUIPMENT CHECK (EQC). Equipment Check is set if an abnormality is detected in the selected control unit, tape unit, or the magnetic tape, and an operation cannot be continued. Equipment Check is set:

- If Bit 1 of Byte 1 (Noise) is set during an erase operation.
- If Bit 0 or 1 of Byte 4 (MP Error, Reject TU) is set.
- If Bit 2 of Byte 5 (Write TM Check) is set.

- If Bit 1 of Byte 6 (Write Circuit Alarm) is set.

- If DBOB signal is not detected while ARA Burst is read/written.

- If Bit 0, 1, 2, 3, 4, 5 or 7 of Byte 10 is set. (Status Tag Response Check, Command Tag Response Check, Control Tag Response Check, No Block Detected, Dynamic Resersal, Tach Start Failure, or Velocity Check).

- If Bit 0 of Byte 8 (IBG Detected) is set during a read operation from load point.

- If Bit 0, 1, 2, 3, 4 or 5 of Byte 11 is set. (Read/Write Overrun, Missing Position, Tag In Response check, Register Parity Error, MP Detector Error, CU ROM Parity Error).

Bit 4 DATA CHECK (DCK). Data Check is set if an error is detected on the data read from the tape during a read, read backward, write, or loop-write-to-read operation. Data Check is set:

- If Bit 0 of Byte 1 is set (Noise) except during an erase operation.

- If Bit 0, 1, 2, 3, 4 or 7 of byte 3 is set. (VRC Check, Multiple Track Error, Skew Error, End Data CRC Check, Envelope Check or P-Compare).

- If Bit 3 of Byte 4 is set. (Write Trigger VRC).

- If Bit 4, 5, 6 or 7 of Byte 5 is set. (Start Read check, Partial Record, Postamble Error, Error Count Overflow).

- If Bit 0, 3, 4, 5 or 6 of Byte 8 is set. (IBG Detect, Early Begin Readback Check, SAGC Check, Slow Begin Readback Check, or Slow End Readback Check).

- If Bit 1, 2 or 3 of Byte 9 is set. (Velocity Change, Channel Buffer Check or CRC III Check).

Bit 5 OVERRUN (OVRN). Overrun is set if a data service request cannot be serviced fast enough in a write, loop write-to-read, read or read backward operation. If Data Check is true, overrun is suppressed. . Data transfer is terminated upon detection of overrun, the operation continues to a normal conclusion.

Bit 6 WORD COUNT ZERO (WCZ). Word Count Zero is set if data transfer is stopped before the first data is received during a Write or Loop-Write-to-Read command.

Bit 7 DATA CONVERTER CHECK. Not used. Always false.

b. SENSE BYTE 1

Bit 0 NOISE. Noise is set:

- If a Data Check is set during a 1600 BPI or 6250 BPI read or read backward.
- If a Noise Block is detected in the Read or Read Backward command of 800 BPI.
- If some data is detected during Stop Delay Transient in 800 BPI mode.
- If data is detected during the erase portion of an Erase, Write Tape Mark, or Write command.

Bit 1 TU STATUS A.
Bit 2 TU STATUS B. TU Status A/B indicates the status of the MTU.

TU STATUS A	TU STATUS B	MTU STATUS
OFF	OFF	Nonexistent or Power OFF
OFF	ON	Power ON and Offline
ON	OFF	Ready

Both bits are set if no data block or tape mark is detected within 20 meters in a read, space or space file operation.

Bit 3 SEVEN TRACK. Not used, always false.

Bit 4 LOAD POINT. Load Point is set when the selected tape unit is at the beginning of tape.

Bit 5 WRITE STATUS. Write Status is set when the selected tape unit is conditioned to write.

Bit 6 FILE PROTECT. File Protect is set when the selected tape unit cannot write because there is no write enable ring in the file reel or manual file protect has been set by the operator.

Bit 7 NOT CAPABLE. Not Capable is set:

- If an attempt is made to read 800 BPI tape through the MTC or MTU without 800 BPI Feature or function.
- If an attempt is made to read 6250 BPI tape with the MTU without 6250 BPI function.
- If MTU tape speed is not suitable for the MTC.

c. SENSE BYTE 2, Error Track 0 thru 7. The Sense Byte contains the track-in-error indicator bits which set for any track containing an error, and/or is "Dead Tracked" during a Write, Loop-Write-To-Read, Read or Read Backward command in 6250/1600 BPI mode.

In 800 BPI mode, bit 6 and 7 are made "1" if there is no error or there is some error but its track is not identified.

If there is some error on one track, the erroneous track is indicated by setting the corresponding bit to "1".

In the error-retry of Read or Read Backward Command, the data to be transferred to the control unit using the Request Track In Error Command should be identical to this Sense Byte.

d. SENSE BYTE 3.

Bit 0 VERTICAL REDUNDANCY CHECK (VRC) ERROR

- VRC Error is set if an uncorrectable VRC Error is detected in a read of read backward operation.

- VRC Error is set if a VRC Error is detected in a write or loop-write-to-read operation.

Bit 1 MULTIPLE TRACK ERROR/LONFITUDINAL REDUNDANCY CHECK (LRC) ERROR. Multiple Track Error is set if multiple tracks in error are detected in 6250/1600 BPI mode.

LRC Error is set if a parity error is detected in horizontal tracks in 800 BPI mode.

Bit 2 SKEW ERROR. Skew Error is set if excessive skew is detected.

- If a postamble cannot be detected or is detected erroneously in a 1600 BPI read operation.

- If a CRC error is detected in a 6250/800 BPI read or write operation.

- If a CRC III error is detected.

Bit 4 ENVELOPE CHECK. Envelope check is set:

- If a drop-out is detected in a 6250 BPI write operation. Data Check is not set.

- If a drop-out is detected in a 1600 BPI write operation. Data Check is also set.

Bit 5 1600 BPI. 1600 BPI is set when the selected tape unit is in 1600 BPI (PE) mode.

Bit 6 BACKWARD. Backward is set when the selected tape unit is in a backward status.

Bit 7 P COMPARE. P Compare is set if a parity error or compare error is detected.

- On the Write Data Bus during write.
- On the Channel Bus In Register (A/B Register) during read or read backward.
- On the Deskewing Buffer Read Out Counter.
- On the Channel Buffer Input Register.
- If the input data to the Channel Buffer does not compare to the output data as determined by a CRC Check at the input and output.

e. SENSE BYTE 4

Bit 0 MP HARDWARE ERROR. MP Hardware Error is set if a microprogram hardware error is detected. The details are defined in both Sense Bytes 11.

- This bit may set Bus Out Check, if temporary hardware error is detected.

Bit 1 REJECT TAPE UNIT. Reject tape unit is set if the selected tape unit condition becomes abnormal, for example Not Ready during execution of a tape motion command or file protected condition during execution of write, write tape mark, erase operation, or 800 BPI MTU.

Bit 2 TAPE INDICATE. Tape Indicate is set when the selected tape unit is beyond the end-of-tape marker.

Bit 3 WRITE TRIGGER VRC. Write Trigger VRC is set if the byte written by the write triggers have incorrect parity.

Bit 4 SPARE. Always false.

Bit 5 LOOP-WRITE-TO-READ. Loop-Write-to-Read is set when the last command was Loop-Write-to-Read.

Bit 6 TAPE UNIT CHECK. Tape Unit Check is set if an abnormality is detected in the selected tape unit. The details are defined in Sense Byte 7 and 21.

Bit 7 SPARE. Always false.

f. SENSE BYTE 5

Bit 0 NEW SUBSYSTEM. Always false on this Subsystem.

Bit 1 NEW SUBSYSTEM. Always true on this Subsystem.

Bit 2 WRITE TAPE MARK CHECK. Write Tape Mark Check is set if the tape mark is not written correctly.

Bit 3 ID BURST CHECK. ID Burst Check is set if an identification (ID) burst is not written correctly in 1600 or 6250 BPI mode, or ARA burst is not written correctly in 6250 BPI mode.

Bit 4 START READ CHECK. Start Read Check is set if an IBG is detected during preamble, or the first data byte is not detected within the prescribed time in 1600 BPI or 6250 BPI mode.

Bit 5 PARTIAL RECORD. Partial Record is set if an IBG is detected within a data block in 1600 or 6250 BPI mode.

Bit 6 POSTAMBLE ERROR. Postamble Error is set if:

- The postamble length is longer or shorter than normal.
- The 1600 BPI postamble is not all '0's.
- The 6250 BPI postamble is not all '1's.

Bit 7 ERROR COUNT OVERFLOW. Indicates Error Count (Sense Byte 8) is overflowing.

g. SENSE BYTE 6

Bit 0-7 TRACK TAPE UNIT. Always false.

Bit 1 WRITE CIRCUIT ALARM. Write Circuit Alarm is set if:

- The write current source voltage is less than a specified value during write status.
- The Erase current source voltage is less than a specified value during write or erase status.
- There is write or erase current during read status.

Bit 2 DUAL DENSITY. Always true.

Bit 3 NOK SET 1600 BPI. Set when the tape unit is in 6250 BPI mode.

Bit 4 6250 BPI TAPE UNIT. Set when the selected tape unit has a 6250 BPI Capability.

Bit 5-7 TAPE UNIT MODEL. For 3243/44 or 3262, 125 IPS Bit 5 is true and Bits 6 and 7 are false. For 3241/42 or 3262, 75 IPS, Bits 6 and 7 are true and Bit 5 is false.

h. SENSE BYTE 7

Bit 0 MISC. ERRORS. Set if either tape loop sensor of true left or right column detects an error.

Bit 1 TAPE LOOP ALARM LEFT. Set if a tape loop is in the warning area of the left column.

Bit 2 TAPE LOOP ALARM RIGHT. Set if a tape loop is in the warning area of the right column.

Bit 3 RESET KEY. Set when the reset switch on the selected tape unit is pressed or the door is opened and is reset when the selected tape unit returns to Online status.

Bit 4 DATA SECURITY ERASE. Set if the selected tape unit fails to perform data security erase operation properly.

Bit 5 SPARE. Always false.

Bit 6 AIR BEARING ALARM. Set if the air pressure to the air bearings has dropped below a threshold value.

Bit 7 LOAD FAILURE. Set if the selected tape unit has failed in auto-load.

i. SENSE BYTE 8

Bit 0 IBG DETECTED.

- Set if an IBG is detected with the data portion of a block during a write operation.

- Set if an IBG is not detected within the prescribed time from a load point during read operation.

Bit 1 ERROR TRACK P. Track P continuation of Sense Byte 2.

Bit 2 SPARE. Always false.

Bit 3 EARLY BEGIN READBACK CHECK. Set if the beginning of the data block or the end of the data block is detected too early in a write operation.

Bit 4 SAGC CHECK. Set if the ARA (Automatic Read Amplification) burst is not written or read properly in a 6250 BPI mode operation from load point.

Bit 5 SLOW BEGIN READBACK CHECK. Set if the beginning of a block was detected too late in a write operation.

Bit 6 SLOW END READBACK CHECK. Set if the end of a block was detected too late in a write operation.

Bit 7 VELOCITY RETRY. Set if a Write operation is delayed due to the capstan velocity being outside the specified tolerance.

j. SENSE BYTE 9

Bit 0 1- OR 2-TRACK CORRECTION. Set if:

- One track error correction is performed during a 6250 BPI write operation or during a 1600 BPI read operation.

- One or two track error correction was performed in a 6250 BPI read operation.

Bit 1 VELOCITY CHANGE. Set if the capstan speed goes out of tolerance during a write operation.

Bit 2 CHANNEL BUFFER CHECK. Set if the input data and the output data of the channel buffer do not match. A CRC is made on the input data and B CRC is made on the output data. This bit is set if the two CRC's do not compare equal. P-Compare is set at the same time.

Bit 3 CRC III ERROR. Set if a CRC III error is detected.

Bit 4 6250 BPI CONTROL UNIT. Always true.

Bit 5. Always true.

Bit 6 TAPE UNIT RESERVED. Becomes "1" if the tape unit is reserved from the Sense Execution path.

Bit 7 CONTROL UNIT RESERVE. Set when the selected control unit is in reserve status and there is a 2-channel switch.

k. SENSE BYTE 10

Bit 0 STATUS TAG RESPONSE CHECK. Set if the selected tape unit fails to respond appropriately with TAG IN to the Status Tag.

Bit 1 COMMAND TAG RESPONSE CHECK. Set if the selected tape unit fails to respond appropriately with TAG IN to the Command Tag.

Bit 2 CONTROL TAG RESPONSE CHECK. Set if the selected tape unit fails to respond appropriately with TAG IN to the Control Tag.

Bit 3 NO BLOCK DETECTED. Set if no block is detected in a write operation.

Bit 4 DYNAMIC REVERSAL. Dynamic Reversal is set:

- If the selected tape unit runs in reverse for a distance longer than is prescribed.

- If the load point is not detected within the prescribed time after ARA correction burst is detected during the execution of a Backward Motion command.

Bit 5 TACHO START FAILURE. Set if the capstan tacho pulse or Gap Control signal is not detected within the specified time after the capstan drive signal is set on.

Bit 6 SPARE. Always false.

Bit 7 VELOCITY CHECK. Set if the capstan speed fails to reach a satisfactory value within the specified time in a write or write tape mark operation.

l. SENSE BYTE 11

Bit 0 READ/WRITE OVERRUN. Set if an attempt is made to read or write a data block of more than 15 m.

Bit 1 MISSING POSITION.

- Set if the tape position becomes unclear in a repositioning of Read/Write error recovery.

- Set to "1" together with Read/Write Overrun if the tape unit does not indicate the TM status, when the tape unit performing a disconnect Skip file operation becomes ready.

Bit 2 TAG IN RESPONSE CHECK. Set if TAG IN response of the selected tape unit is abnormal.

Bit 3 REGISTER PARITY ERROR. Set if a parity error is detected in the Local storage Registers.

Bit 4 MP DETECT ERROR. Set if the microprogram detects a hardware abnormality during the execution.

Bit 5 CU ROM PARITY ERROR. Set if a ROM parity error in the control unit is detected.

Bit 6 MP TRAPPED. Set to "1" if command operation is terminated by some MP trap.

Bit 7 TU ROM PARITY ERROR. Set if a ROM parity error of the selected tape unit is detected.

m. SENSE BYTE 12.

Internal Status of the tape unit is indicated in the Sense Byte.

Bit 0 ERASE CURRENT ON. Indicates that the erase current is ON. (internal status of the tape unit.)

Bit 1 TU ACTION. Indicates that the tape unit is operating.

Bit 2 INNER BACKWARD. Indicates that operating direction of the tape unit is true.

Bit 3 WRITE CURRENT ON. Indicates that write head current is ON.

Bit 4 ARA 65% SLICE. Indicates that the 90% slice failed and the 65% slice was attempted in the SAGC operation of ARA.

Bit 5 HIGH SPEED MODE. Set to "1" when the tape unit is set to the High Speed Mode.

Bit 6 INNER 1600 BPI. Set to "1" when the inner mode of the tape unit is at 1600 BPI.

Bit 7 TAPE MARK DETECTED. Set to "1" if the tape unit has correctly detected a tape mark in the Space File or Back Space File.

n. SENSE BYTE 13

Bits 0-7 ERROR COUNT. Every tape unit has an error counter. A count of the errors detected during all write operations for each selected tape unit is kept. The counter associated with the selected tape unit is reset, if a Rewind, Unload, or Read Backward command is issued. Error count indicates the contents of the counter associated with the selected tape unit. If the count exceeds the value of 96 for GCR mode or 32 for PE mode, the tape unit's error marker will be primed and when the tape is unloaded an error mark is printed on the backside of the reel.

Note: Write Error recovery routines should use space backward block, not read backward in order to maintain a proper error count.

o. SENSE BYTE 14

Not defined.

p. SENSE BYTE 15

Bit 0 HIGH SPEED FEATURE. Set when the selected tape unit has High Speed feature.

Bit 1 SKIP FILE FEATURE. Set when the selected tape unit has Skip file feature.

Bit 2. Not Used.

Bit 4-7 TU UNIQUE ID (HIGH ORDER). Indicates the high order 4 bits of the selected tape unit serial number.

q. SENSE BYTE 16

Bits 0-7 TU UNIQUE ID (LOW ORDER). Indicates the low order of the selected tape unit serial number.

r. SENSE BYTE 17

Bit 0 TWO CHANNEL SWITCH. Set when the selected control unit has 2-Channel Switch feature.

Bit 1 800 BPI FEATURE. Set when the selected control unit has 800 BPI feature.

Bit 2-3. Not Used.

Bits 4-7 CU EC LEVEL. Indicates the control unit EC level.

s. SENSE BYTE 18

Bit 0-3 SAGC COUNT. Indicates the SAGC count value maintained in the selected tape unit.
Bit 0 - SAGC Count 0. Indicates the SAGC count value of any one of 9 tracks is E or F (Decimal 14 or 15).
Bit 1 - SAGC Count 1. Indicates the SAGC count value of any one of 9 tracks is C or D (Decimal 12 or 13).
Bit 2 - SAGC Count 2. Indicates the SAGC count value of any one of 9 tracks is A or B (Decimal 10 or 11).
Bit 3 - SAGC Count 3. Indicates the SAGC count value of any one of 9 tracks is 8 or 9.
Always false for PE/NRZI mode.

Bits 4-7 TU EC LEVEL. Indicates the EC level of the selected tape unit.

t. SENSE BYTE 19

Bits 0-7. Primed for Device End for tape unit 7 through 0, respectively. Bit 0 is for tape unit 7 and bit 7 is for tape unit 0.

u. SENSE BYTE 20

Bit 0-7. Not used.

v. SENSE BYTE 21

Indicates various MTU error codes.

Bits 0-7 MTU ERROR CODE. To be defined.

w. SENSE BYTE 22

Field Replaceable Unit

x. SENSE BYTE 23

Field Replaceable Unit

These two bytes, and the Sense Bits EQC, CRJ, BOC and DCK, form a matrix of error conditions as an aid to the customer engineer. See the Maintenance Manual for details.

CHAPTER 3 INTERFACE

3.1 Channel Interface

Any channel to be connected to a controller must have the data-in/data-out function and the disconnect-in function as equivalent to the IBM BMC in the shared mode. This section outlines the interface for such a channel.

3.1.1 Signal lines

Table 3.1 lists the channel interface signal lines.

Table 3.1 Channel interface signal lines (1/2)

Name	Direction/ number of lines BMC-MTC	Meaning
Bus Out (BOs 0 to 7,p)	9 ⟹	Sends commands/addresses/data from a channel to an MTC.
Bus In (BIs 0 to 7,p)	9 ⟸	Sends data/status byte/addresses from an MTC to a channel.
Address Out (ADO)	1 ⟶	Indicates that the contents of BOs 0 to 7,p are an address. It is also used to direct to disconnect the interface along with SLO.
Command Out (CMO)	1 ⟶	Indicates that the contents of BOs 0 to 7,p are a command code. It is also used to direct to proceed/stack/stop.
Service Out (SVO)	1 ⟶	Sends data to BOs 0 to 7,p, receives data from BIs 0 to 7,p, and receives a status.
Data Out (DTO)	1 ⟶	Sends data to BOs 0 to 7,p and receives data from BIs 0 to 7,p.
Address In (ADI)	1 ⟵	Indicates that address information has been sent to BIs 0 to 7,p.
Status In (STI)	1 ⟵	Indicates that the status byte has been sent to BIs 0 to 7,p.

Table 3.1 Channel interface signal lines (2/2)

Name	Direction/ number of lines BMC-MTC	Meaning
Service In (SVI)	1 ←	Indicates that a request to send data is issued to a channel and data has been sent to BIs 0 to 7,p.
Data In (DTI)	1 ←	Indicates that a request to send data is issued to a channel and data has been sent to BIs 0 to 7,p.
Select Out (SLO)	1 →	Requests to connect a channel to the I/O device.
Select In (SLI)	1 ←	Replies to the SLO.
Hold Out (HLO)	1 →	Indicates that the SLO is valid, used along with the SLO.
Request In (RQI)	1 ←	Requests to start the MTC polling sequence.
Operational Out (OPO)	1 →	Indicates that the channel is operating. It directs a system reset or a selective reset, along with the SPO signal.
Operational In (OPI)	1 ←	Indicates that the MTC is connecting to a channel.
Suppress Out (SPO)	1 →	Suppresses status sending/data transfer; directs a command chain; directs a selective reset.
Disconnect In (DSI)	1 ←	Notifies the abnormal status that has occurred during connection to the channel.
Metering Out (MTO)	1 →	Unused by MTC.
Metering In (MTI)	1 ←	Is set to '1' while a command is operating.
Clock Out Mark In Mark Out	1 → 1 ← 1 →	Unused by MTC.

3.1.2 Interface sequence

Figures 3.1 to 3.4 show typical interface sequence.

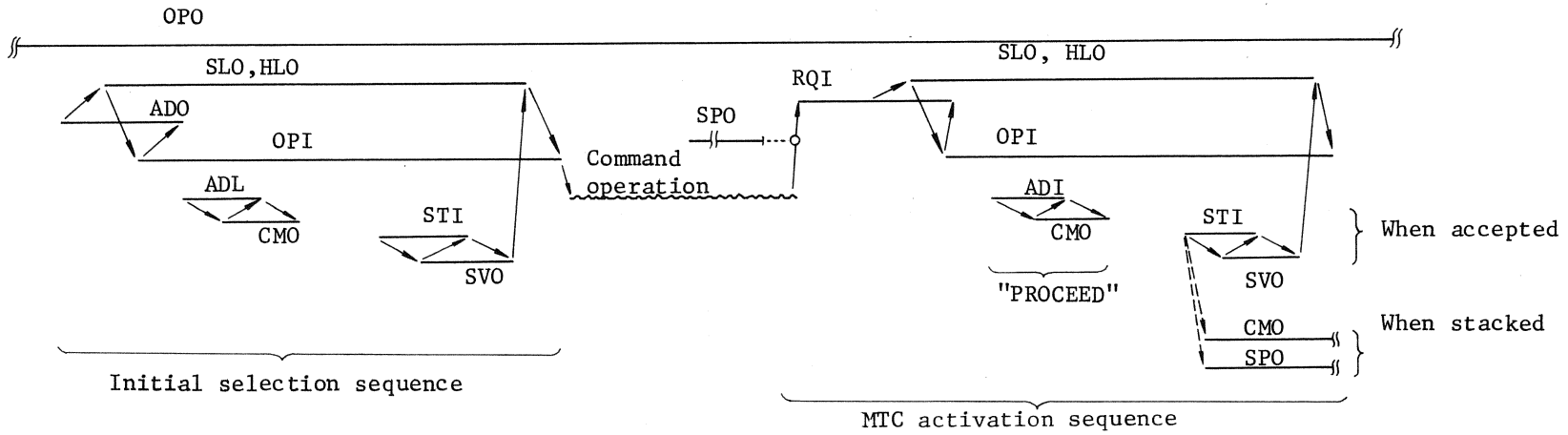


Figure 3.1 An example of the interface sequence for control commands

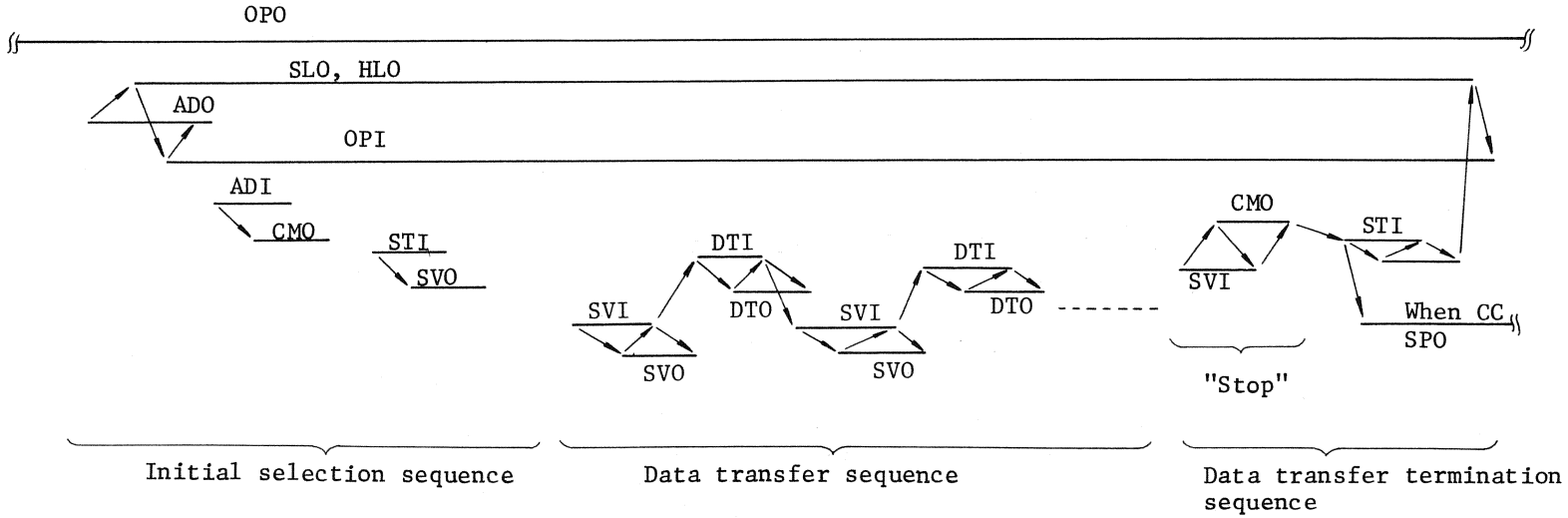


Figure 3.2 An example of the interface sequence for burst commands

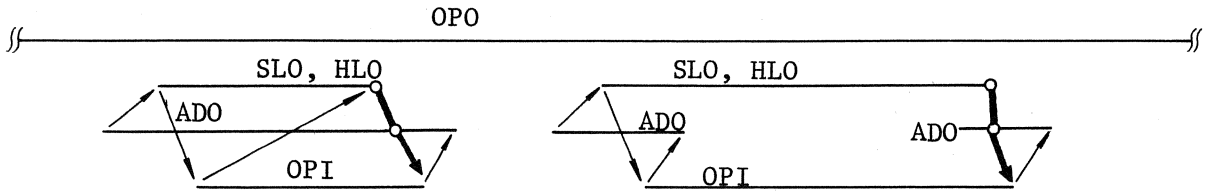


Figure 3.3 Interface disconnect sequence

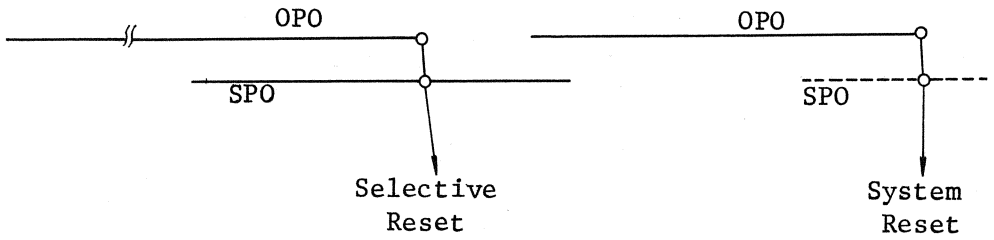
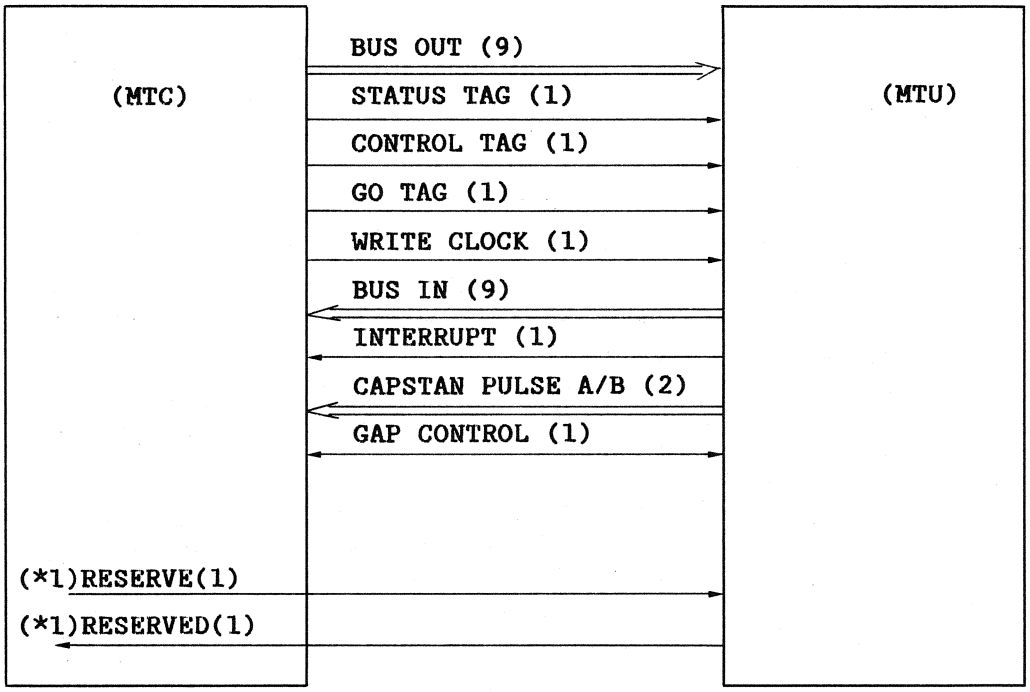


Figure 3.4 Reset

3.2 MTC-MTU Interface

This section summarizes the definitions of logical signal lines between an MTC and an MTU.

3.2.1 Interface signal lines



*1 No Reserve nor Reserved signal is used on the MTU level. However, the MTU must be terminated by a terminal resistor.

Figure 3.5 Interface signal lines

Table 3.2 MTU interface signal lines

Signal name	Meaning
Status Tag	Indicates that Bus out data is the status information to be set, and directs MTU to set the status information on Bus-in lines.
Control Tag	Indicates that Bus out data is the control information and directs MTU to set control information on Bus-in lines. If both the Control Tag and the Status Tag are '1', then it operates as the Command Tag.
Go Tag	Causes to drive the tape in the MTU for reading or writing data.
Bus Out	Indicates the information, modified through the three Tag signal lines. If the three Tag signal lines are set to all '0's, a request to send the MTU sense bytes corresponding to the Bus Out bits is issued.
Bus In	If any one of the Status Tag, Control Tag, or Go Tag is '1' or both the Status Tag and Control Tag are '1', the respective information is set on the Bus In lines. If these three Tag signal lines are all '0's, then each sense byte for each Bus Out bit is set on the Bus In lines.
Write Clock	Strobes the contents of the Bus Out, with the Write Clock as well as the Status Tag/Control Tag/Command Tag set to '1'.
Interrupt	Issues an interrupt to the MTC while the MTU is onlined.
Capstan Pulse A/B	Conveys the tape driving information detected from the capstan to the MTC.
Gap Control	Conveys the block access enable signal from the MTU to the MTC.

Table 3.3 Bus Out/Bus In Definitions

	BUS OUT					BUS IN			
TAG BIT	STATUS	CONTROL	COMMAND	GO		STATUS	CONTROL	COMMAND	GO
0	Set Erase	Level Test 0	BUS OUT 0123 4567 / COMMAND	WDT0/RDL0		ERS	Level Test 0	BUS IN CONTENT	RD0
1	Set Read Forward	Level Test 1	0 2 Set Streaming Mode	WDT1/RDL1		FWD	Level Test 1	BO / BUS IN: (OX)16	RD1
2	Set Read Backward	Level Test 2	0 3 Reset Streaming Mode	WDT2/RDL2		BWD	Level Test 2	0 STRMF (Streaming Feature)	RD2
3	Set Write Status	Set Test Mode	0 4 Space File	WDT3/RDL3		Write Status	Test Mode	1 SKIPF (Skip File Feature)	RD3
4	Reset	Set EMK	0 5 Backspace File	WDT4/RDL4		TU Check	EMK	2 Spare	RD4
5	Set 6250 & SAGC or Set NRZI	Set DSE	0 6 Spare	WDT5/RDL5		SAGCON	DSE	3 LWSL (Low Slice)	RD5
6	Set 1600	Set REW	0 7 Spare	WDT6/RDL6		1600	REW	4 STRMD (Streaming Mode)	RD6
7	Set LWR	Set UNL	0 8 Set LWR2	WDT7/RDL7		LWR	UNL	5 LWR2 (Loop W&R2)	RD7
8	Parity	Parity	0 9 Reset LWR2	WDT8/RDL8		TAG IN	TAG IN	6 HACT	RD8
			0 A Set Low Slice					7 RDY (Ready)	
			0 B Reset Low Slice					BO / BUS IN: 8X 9X / AX BX / CX DX / EX FX	
			COMMUNICATION REG					0~7: Reg. 0 / Reg. 1 / Reg. 2 / Reg. 3	
			8 0~F Reg 0 high order 4 bits						
			9 " " low order 4 bits						
			A " Reg 1 high order 4 bits						
			B " " low order 4 bits						
			C " Reg 2 high order 4 bits						
			D " " low order 4 bits						
			E " Reg 3 high order 4 bits						
			F " " low order 4 bits						
			8 Parity						

Table 3.4 Communication registers

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Reg 0	← Write Error Count Memo →							
Reg 1			Retry CNT0	Retry CNT1			Long IBG0	Long IBG1
Reg 2	Valid Position CNT	← Position Counter Upper →						
Reg 3	← Position Counter Lower →							

Table 3.5 TU sense bytes

SENSE BYTE	0	1	2	3	4	5	6	7	8
BUS OUT BIT / BUS IN	7(01) (8, all 0)	6(02)	5(04)	4(08)	3(10)	2(20)	1(40)	0(80)	3&5(14) (STS & GO TAG)
0	BWD	EXIF	MISC Error	VEL 0	Tape Unit Unique ID Low Order 2^7	SAGC COUNT 0	Read Data 0	Error Code 1 (Load RWD)	Handler Erase Current ON
1	NOT FP	Reset Key	Tape Loop Alarm Left	VEL 1	" 2^6	SAGC COUNT 1	Read Data 1	Error Code 1 (LR turning)	Handler Action
2	TWA	DSE	Tape Loop Alarm Right	Ready Hold	" 2^5	SAGC COUNT 2	Read Data 2	Error Code 2 (RR turning)	Handler Backward Status
3	BOT	7 Track	ROM Parity Error	(Not use) 2^{12}	" 2^4	SAGC COUNT 3	Read Data 3	Error Code 2 (Tape present)	Handler Write current ON
4	Write Status	Test Mode	Write Circuit Alarm	(MD1[1] Con-version)2^{11}	" 2^3	EC Level 2^3 ("1")	Read Data 4	Error Code 4 (Reel Loaded)	Handler 65% Slice
5	Online	Dual Density	Not used	Tape Unit Unique ID High Order 2^{10}	" 2^2	EC Level 2^2 (TUID2)	Read Data 5	Error Code 5 (Column Loaded)	Handler Over Run
6	TU Check	High Density	Air bearing Alarm	" 2^9	" 2^1	EC Level 2^1	Read Data 6	Error Code 6 (Search BOT)	Handler PE Mode
7	Ready	6250	Load Failure	" 2^8	" 2^0	EC Level 2^0	Read Data 7	Error Code 7 (Load CHK)	Tape Mark
8	TAG IN	TAG IN	TAG IN	TAG IN	TAG IN	TAG IN	Read Data 8	Error Code 8	TAG IN

CHAPTER 4 HARDWARE

4.1 Outline

Figure 4.1 is a block diagram of the MTC section. In this diagram, each block corresponds to a single PCA whose identification number is shown in brackets. The CH-A/CH-B interface control section, write control section, read control section, 800 BPI control section, demodulation section, microprocessor section, and device interface section are inserted in the MTC shelf.

This chapter describes how the above control sections operate. Figure 4.2 shows the PCAs mounting positions in the MTC shelf.

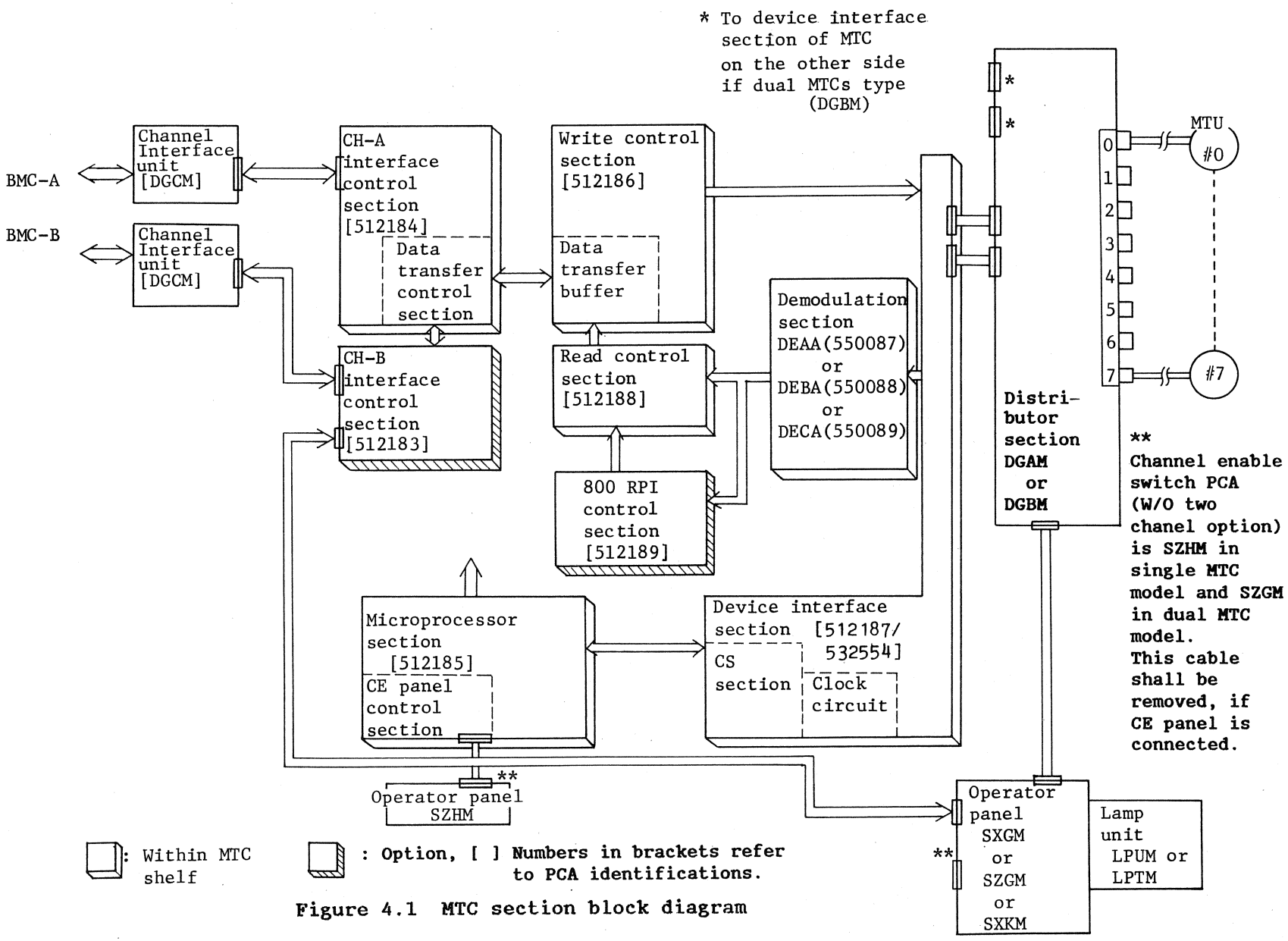
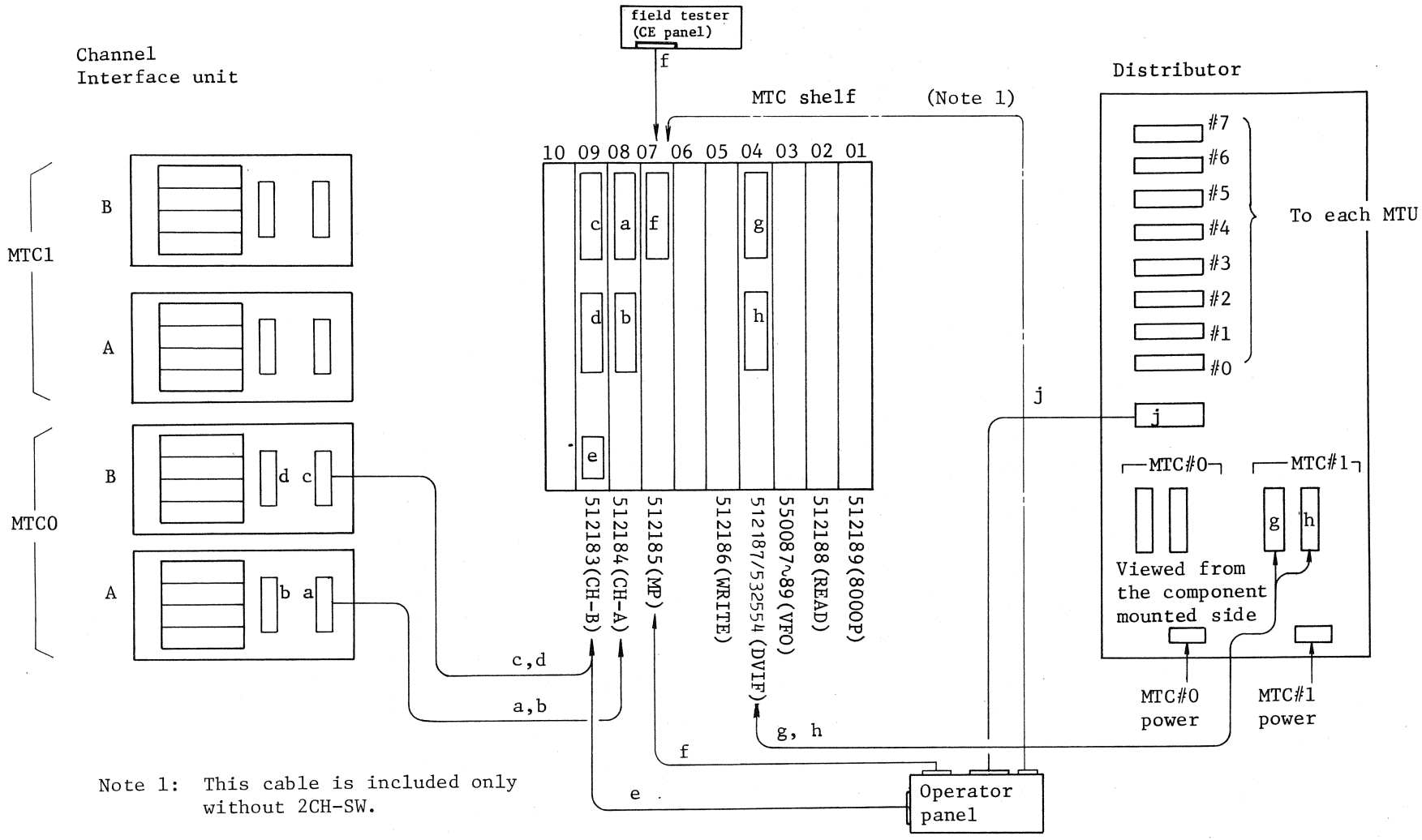


Figure 4.1 MTC section block diagram



Note 1: This cable is included only without 2CH-SW.

Figure 4.2 PCAs mounting positions

4.2 Reset System

The reset function is activated when:

(a) Power is applied.

(b) The ONL/OFL switch on the CE panel is switched or a CE-reset operation done.

(c) The Interface On/Off switch on the operator panel is switched.

(d) A system Reset is directed from a channel.

(e) A Selective Reset is directed from a channel.

(f) An Unconditional Reserve (UR) command is issued from the other MTC.

(g) A microprocessor error (PERR) has occurred.

Figure 4.3 is a functional block diagram of the reset function. The reset function generates three levels of signals as Reset Signals System Reset (SYRT), Selective Reset (SERT), and Hardware Clear (HCLR). Table 4.1 lists the conditions under which these three levels of Reset signals generate.

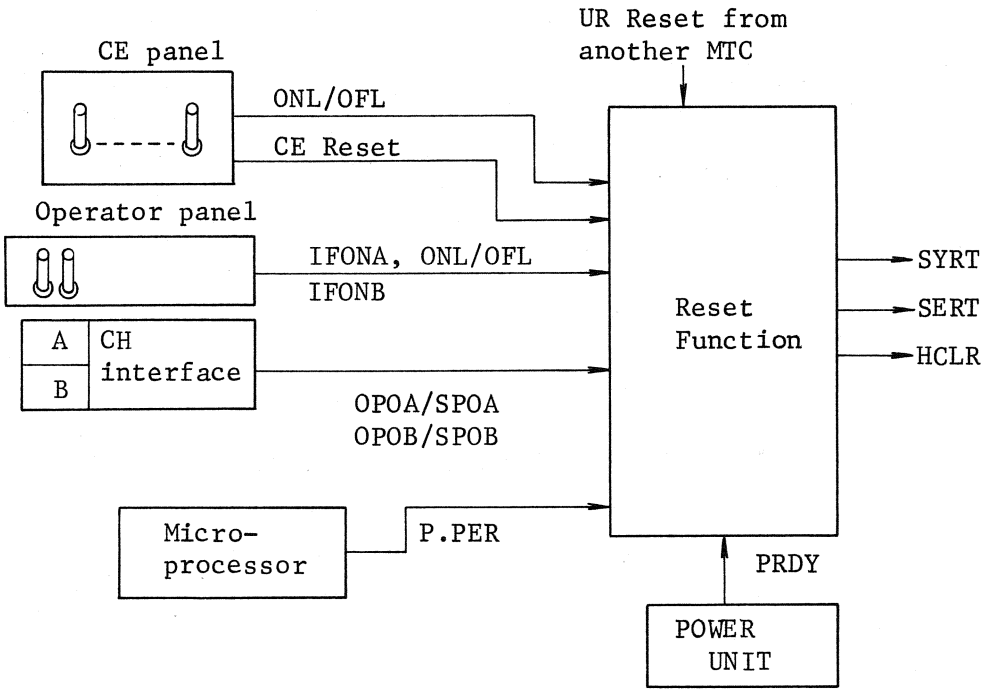


Figure 4.3 Reset function

The HCLR signal acts on the Demodulation section, Write Control section, Read Control section, 800 BPI Control section, etc., so that these circuits can be reset to their initial status.

The SERT signal resets these circuits within the restrictions under which the MTC maintains a link with the selected MTU. The SYRT signal restores the MTC to an idle status.

Table 4.1 Conditions to generate reset signals

Condition	SYRT	SERT	HCLR
Power On/Off (PRDY)	Yes	Yes	Yes
ONL/OFL SW on CE panel (R.OFL)	Yes	Yes	Yes
Interface On/Off SW on operator panel	Yes	Yes	Yes
System Reset from channel	Yes	Yes	Yes
Selective Reset from Channel	No	Yes	Yes
UR Reset from another MTC	Yes	Yes	Yes
PERR	No	No	Yes

4.2.1 UR Reset

The UR Reset signal is directed by an Unconditional Reserve (UR) command. This signal interacts between two MTCs linked in the cross-call mode. The MTC to which a UR command is directed issues a System Reset to the other MTC and forcibly reserves an aimed MTU when the MTU cannot be reserved on its own side because the aimed MTU with a specified address is still used by the other MTC.

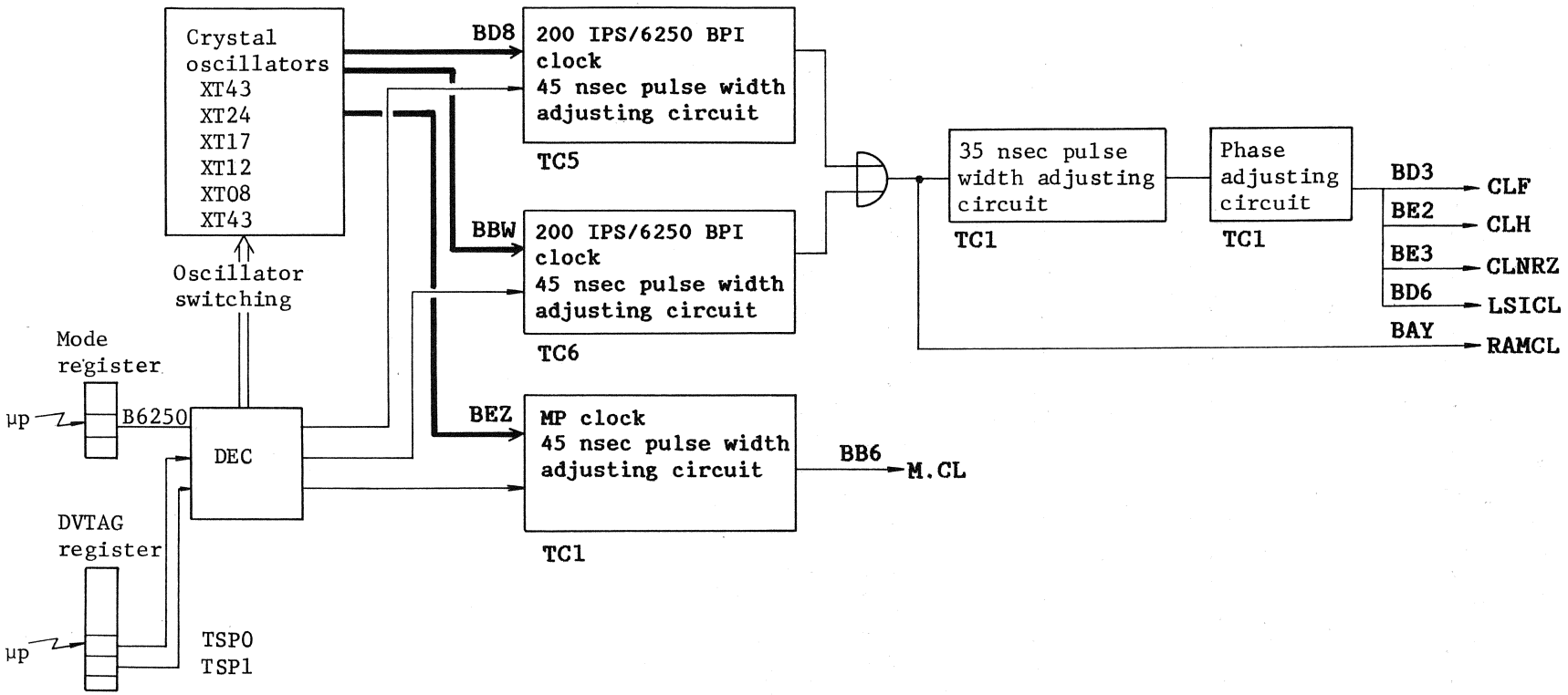
A UR Reset is directed to the other MTC only if a microprogram sets bits 6 and 7 of the IFSTA register to on.

On the other hand, a U.RST signal is set on if the UR Reset signal from the other MTC is continuously set on for a definite period. The U.RST signal acts as a System Reset signal.

4.3 Clock System

The clock circuit in the MTC section is so configured that the MTU can operate in a recording density of 6250/1600/800 BPI at a running speed of 50/75/125/200 IPS, respectively. As shown in Table 4.2, the clock circuit is provided with six types of crystal oscillators. The signals oscillated from these crystal oscillators are devided and corrected for their phase so that five types of basic clock pulses as shown on the next page are generated.

Figure 4.4 shows the configuration of the clock circuit.



Note: Card pins BD8, BBW, and BEZ are input pins for clock margins.

Figure 4.4 Clock circuit configuration

(1) CLF (Clock Full), CLH (Clock Half)

These clock pulses are fed to the formatter. Table 4.2 shows the crystal oscillators used and their clock pulse widths.

(2) CLNRZ (Clock NRZI)

This clock pulse is fed to the PCA for the 800 BPI option.

(3) LSICL (LSI Clock)

This clock pulse is fed to the LSI of the formatter. It helps the phase adjusting circuit adjust the phase difference between CLF and CLH.

(4) RAMCL (RAM Clock)

This clock pulse is fed to the dequeuing buffer in the read formatter.

(5) M.CL (Micro Clock)

This clock pulse is fed to the microprocessor. Its pulse width is 45 nsec; its period is 208 nsec.

* formatter means Write control, Read control, 800 BPI control, Demodulation sections.

Table 4.2 Clock pulse period for each running speed/recording density

Clock / Mode	CLF ns (35 ns)	CLH ns (35 ns)	CLNRZ ns (35 ns)	LSICL ns (35 ns)	RAMCL ns (45 ns)	Used oscillator ns
200 IPS 6250 BPI	184.4	92.2	92.2	92.2	184.4	XT43 92.16
200 IPS 1600/ 800 BPI	520.8	260.4	130.2	260.4	520.8	XT12 65.11
125 IPS 6250 BPI	294.4	147.2	147.2	147.2	294.4	XT24 73.73
125 IPS 1600/ 800 BPI	833.2	416.6	208.3	416.6	833.2	XT08 104.17
75 IPS 6250 BPI	494.4	247.2	494.4	247.2	494.4	XT17 123.40
75 IPS 1600/ 800 BPI	1388.8	694.4	347.2	694.4	1388.8	XT48 86.81
50 IPS 6250 BPI	737.6	368.8	368.8	368.8	737.6	XT43 92.17
50 IPS 1600/ 800 BPI	2083.2	1041.6	520.8	1041.6	2083.2	XT12 65.11

Note: Figure in parentheses refer to pulse widths.

4.4 Microprocessor

4.4.1 Microprocessor configuration

Figure 4.5 is a block diagram of the microprocessor configuration. Table 4.3 shows the major performance characteristics of the microprocessor. This microprocessor, a 32-bit fixed/variable length instruction type processor, is so configured that it can execute a microprogram of up to 4K steps. The microprocessor fetches an instruction from the control storage (CS) section into the CS register (CSR); decodes the instruction; processes and evaluates data on the LSR/EXR; stores the data; jumps to a specified step. The sequencer controls the program flow by advancing steps one by one, jumping or branching to a specified step, and stacking control information and data upon a Subroutine Call/Return. The sequencer also contains the microprogram address register (CSAR: CS address register).

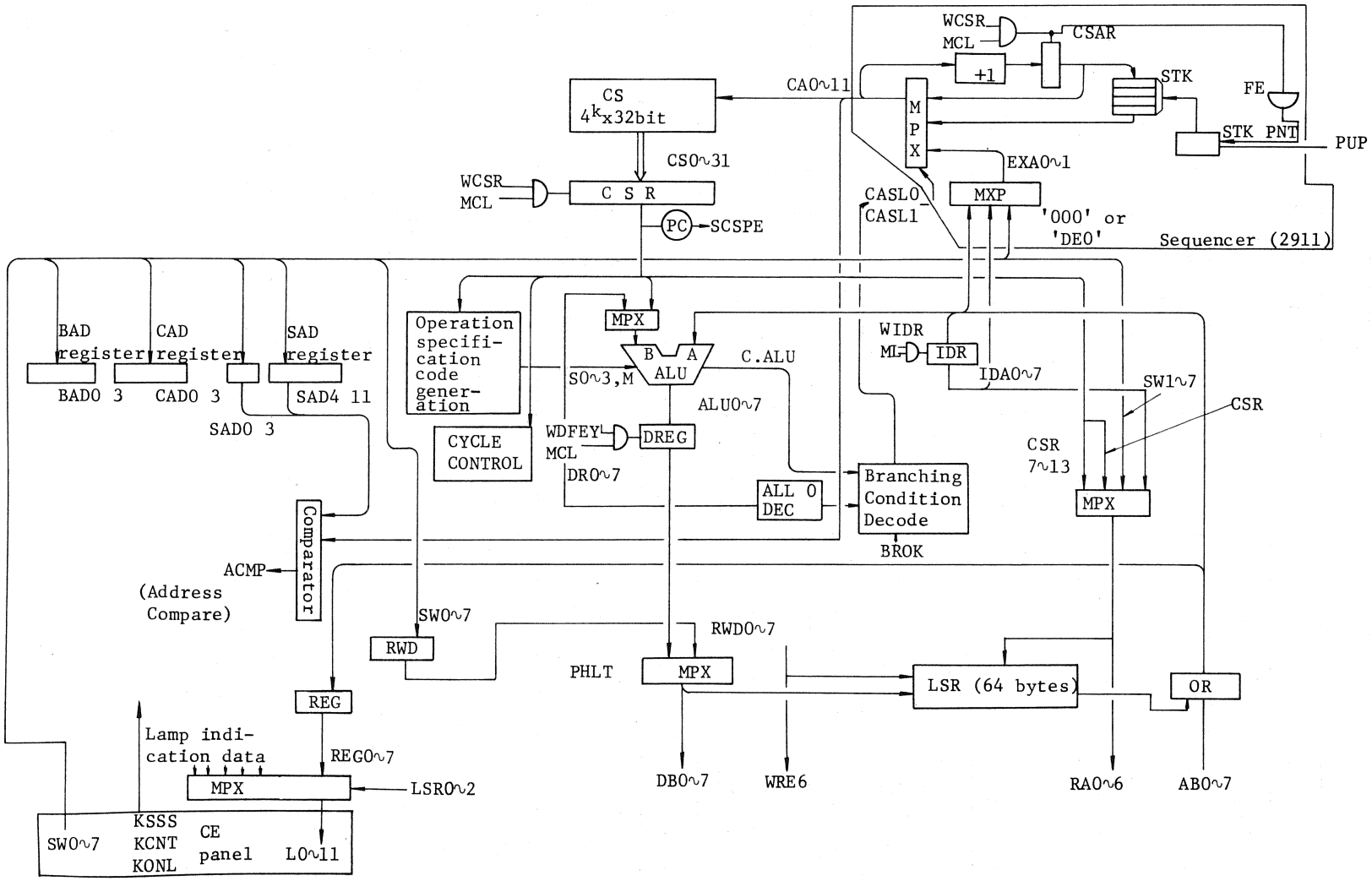


Figure 4.5 Microprocessor configuration

Table 4.3 Major performance characteristics of processor

Item	Performance
Basic clock	208 ns (ϕ)
Instruction execution time	416 ns (2ϕ), 624 ns (3ϕ) 832 ns (4ϕ), 1.04 μs (5ϕ)
Number of instruction types	38 types
Instruction bit length	32 bits (including parity bits)
Instruction counter	12 bits (maximum of 4 K steps)
External register (EXR)	Up to 64 bytes
Internal register (LSR)	64 bytes
Number of interrupt sources	5
Interrupt mask	Possible for each interrupt
CS access time	200 ns or less
Subroutine nesting	Up to 4 levels
Others	CS parity check, LSR parity check, Address Compare, CS scan, step function, CE panel functions, etc.

4.4.2 Processor cycle control

Figure 4.6 shows the cycle timing controller of the processor. The Read Cycle (RCY) signal conveys the timing to access the LSR/EXR, etc. The Write Cycle (WCY) signal conveys the timing to operate, evaluate, and store data. The Extend Cycle 1 (EXCY1) and Extend Cycle 2 (EXCY2) signals control the extended cycle when Extend Cycle instruction is executed. The WCY signal can be extended by one clock by a Branch Condition OK (BCOK) signal to be generated when control is branched by a Branch instruction to an address other than the next address.

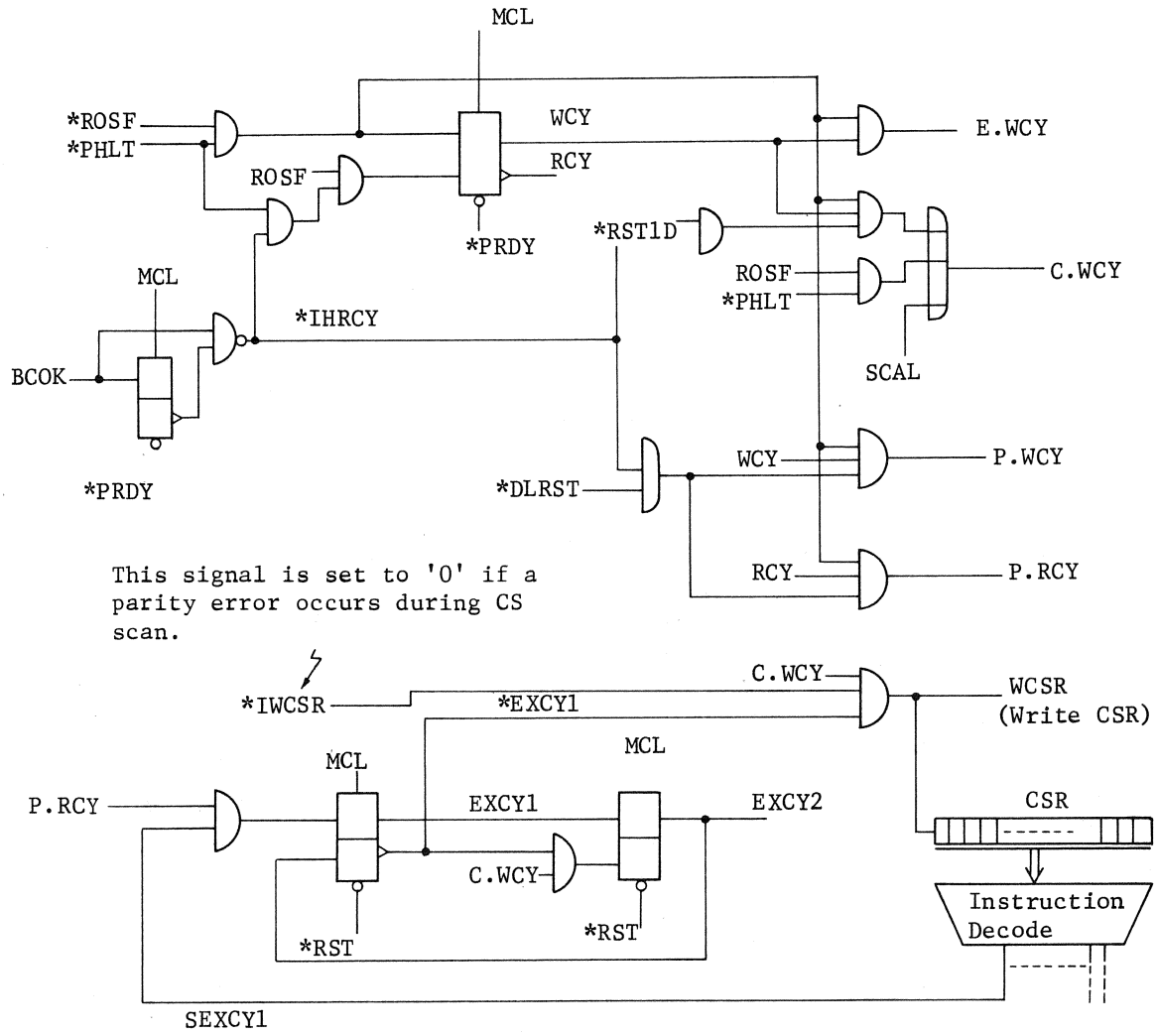


Figure 4.6 Processor timing control circuit

The C.WCY signal conveys the timing to fetch an instruction to the CSR. The instruction is set on the CSR at the timing of the trailing edge of the C.WCY signal (the trailing edge of the WCSR signal). The P.WCY signal conveys the timing to store data into the EXR or LSR.

Figure 4.7 is a timing chart showing when the processor will start with address '0' after resetting the circuit by a Reset (S.CLR) signal.

Table 4.4 shows the bit assignment (configuration) of each instruction for the processor: the timing operation within the processor is controlled by the I, S, RTN, T, and DE bits.

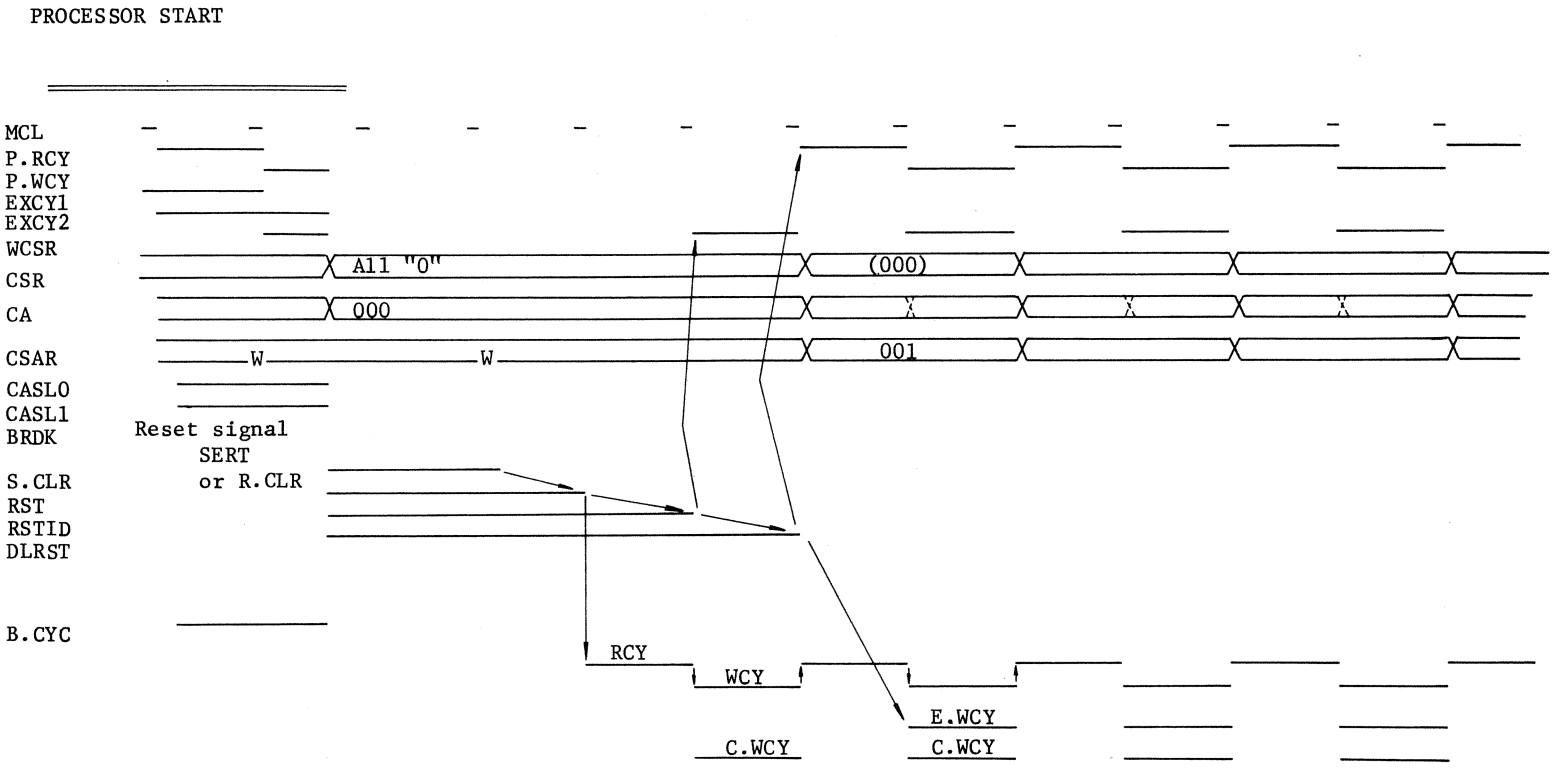


Figure 4.7 Processor start timing chart

Table 4.4 Instruction code configuration

Kind of Instruction	OP			EOP				Source Reg	Immediate data	Branch Adrs/ Destinating Reg			P	Mnemonic
	0	1	2	3	4	5	6	7 8 9 10 11 12 13	14 15 16 17 18	19 20 21 22 23 24 25 26 27 28 29 30			31	
Branch Uncondition	1	0	0	I	S			Source Reg if I = '1'		Branch Adrs	Invalid if I='1'		P	B, CALL, BI, CALLI
Branch on Condition	1	0	1	I	S	RV	C	SourceReg if I = '1'		Branch Adrs	Invalid if I='1'		P	BOC, COC BOCI, COCI
Test Bit & Branch	1	1	0/1	I	S	RV	C	Source Reg	Immediate data	Branch Adrs			P	TBB,TBC TBBI,TBCI / BEQ,BNE, CEQ,CNE, BEQI, BNEI, CEDI, CNEI
ALU Immediate	0	0	RTN	I	A	L	U	Source Reg	Immediate data	T	DE	Destination Reg if I='0'	P	MV,MV*,MVHI, MVHI*,MVFI, MVFI*,LD,LDI, LD*,LDI*
ALU Register	0	1	RTN		A	L	U	Source Reg		T		Destinating Reg	P	MF,MF*, MFD,MFD*

I : Indirect bit
S : Adrs Stack; '1' if Subroutine Call
RTN : Return; '1' if returned from a subroutine
T : Test; ALU output data is not stored in the destination register if T='1'
DE : Stored in the source register if '1'

4.4.3 Interrupt (Trap)

A trap to the microprocessor results from any of five types of sources to each of which a trap vector address is assigned, as shown in Table 4.5.

Table 4.5 Sources of trap

Trap signal		Trap address (Hex.)	Mask bit
Name	Description		
DVINT	Device interrupt. Is an interrupt signal from an MTU and is set to '1' if a BOT is detected while the MTU is running in the reverse direction or a SAGC error has occurred.	'100'	M.INT bit (TMSK bit)
TMINT	Timer interrupt. Is an overflow signal from the timer circuit; the timer circuit stops operating after this signal is generated.		M.TMR bit (TMSK bit)
ISINT	Initial selection interrupt. Is an interrupt signal from the channel interface circuit and is generated at the beginning of the initial selection sequence; it is reset when a microprogram sets the operational in (OPI) bit to on. Besides, an interrupt results from an activation from the CE panel while the MTC is offlined.		M.INS bit (TMSK bit)
TCSTP	Tacho-Stop. This interrupt signal is generated when the period of arrival of tacho pulses from an MTU has increased abnormally.		M.TCS bit (TMSK bit)
PERR	This interrupt signal is set on when a ROM parity error or a LSR parity error has occurred.	'0E0'	None (TMSK bit)

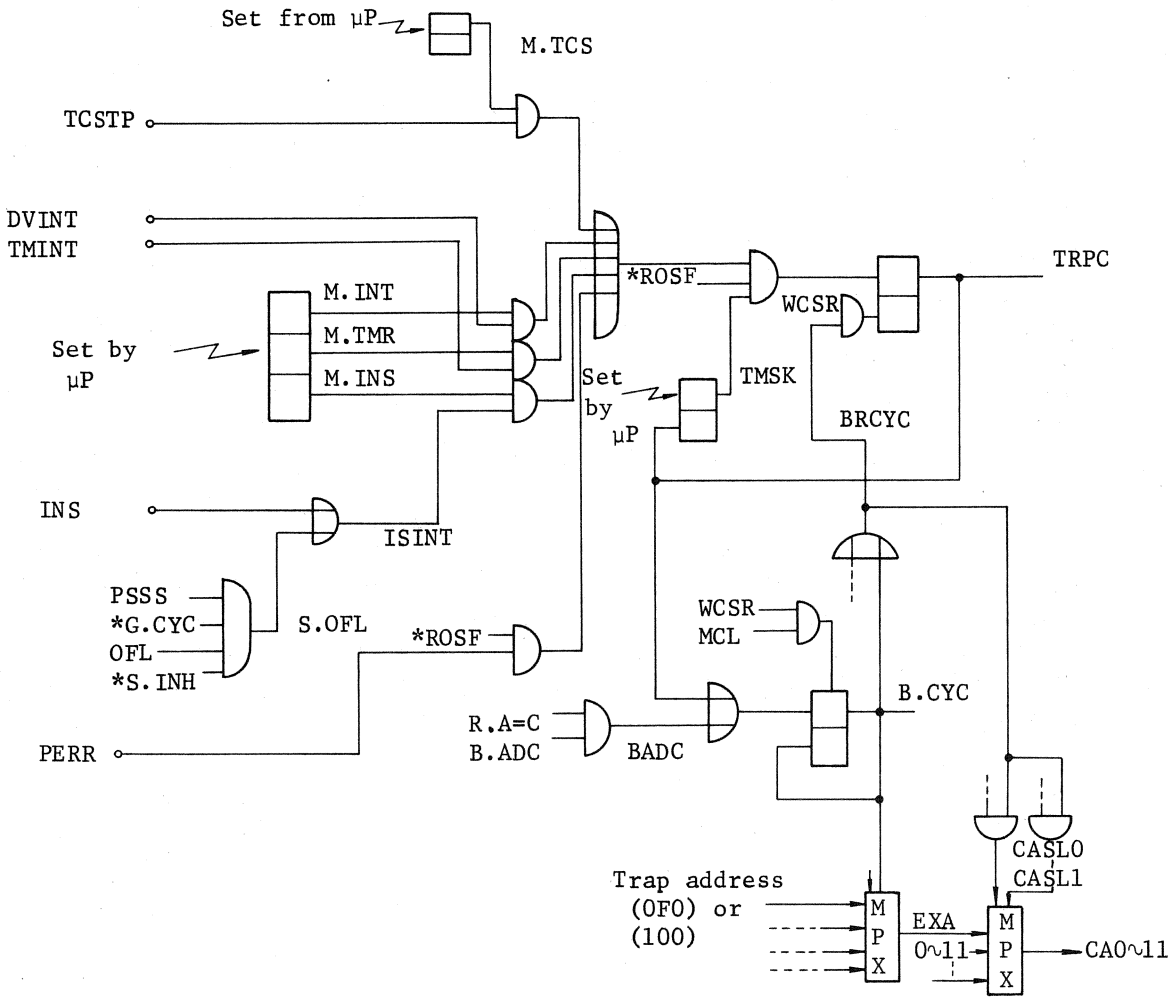


Figure 4.8 Trap control circuit

The processor can be interrupted while a Trap Mask (TMSK) signal is set on. The TMSK signal is set to '1' so that the interrupt is accepted. The TMSK signal is reset after the interrupt has been accepted, then no other interrupts can be accepted until it is set on by the microprogram. After the TRPC signal is set on, a Branch Cycle (B.CYC) signal is generated at the timing of a WCSR signal (end of executing an instruction). The B.CYC signal acts on the sequencer circuit so that the microprogram address is switched to the trap address.

Thus, the instruction stored at the trap address begins to perform with the second instruction cycle since the cause of a trap took place.

4.4.4 CE panel controller

The CE panel, a control panel for maintenance, consists of switches and lamps. It will stop/advance/start the processor, rewrite the contents of the LSR/EXR/microprogram address register, scan the contents of the CS, and realize various indication functions by connecting it to the connector on the processor PCA.

Indicating lamps L0 to L11 light when the SW0 to SW7 switches are to specified statuses. To specify a particular function to the CE panel controller, set the SW0 to SW7 switches under the Specifications, then set the control (CNT) switch to on. Also, to send various control information, such as stop address, branch address, program address, and write data, to the CE panel controller, set the SW0 to SW7 switches to this information and set the Start/Stop/Set (SSS) switch to an appropriate status. While this control information is being requested by the SW0 to SW7 switches, each of S.BAD, S.CAD, S.SAD, W.REG, and S.MOD signals is set on. These signals show that the SW0 to SW7 switches are operating in the control information input mode until they are reset by a PSSS signal (timing pulse generated at the rise of the SSS switch). This subsection describes major operations of the CE panel controller.

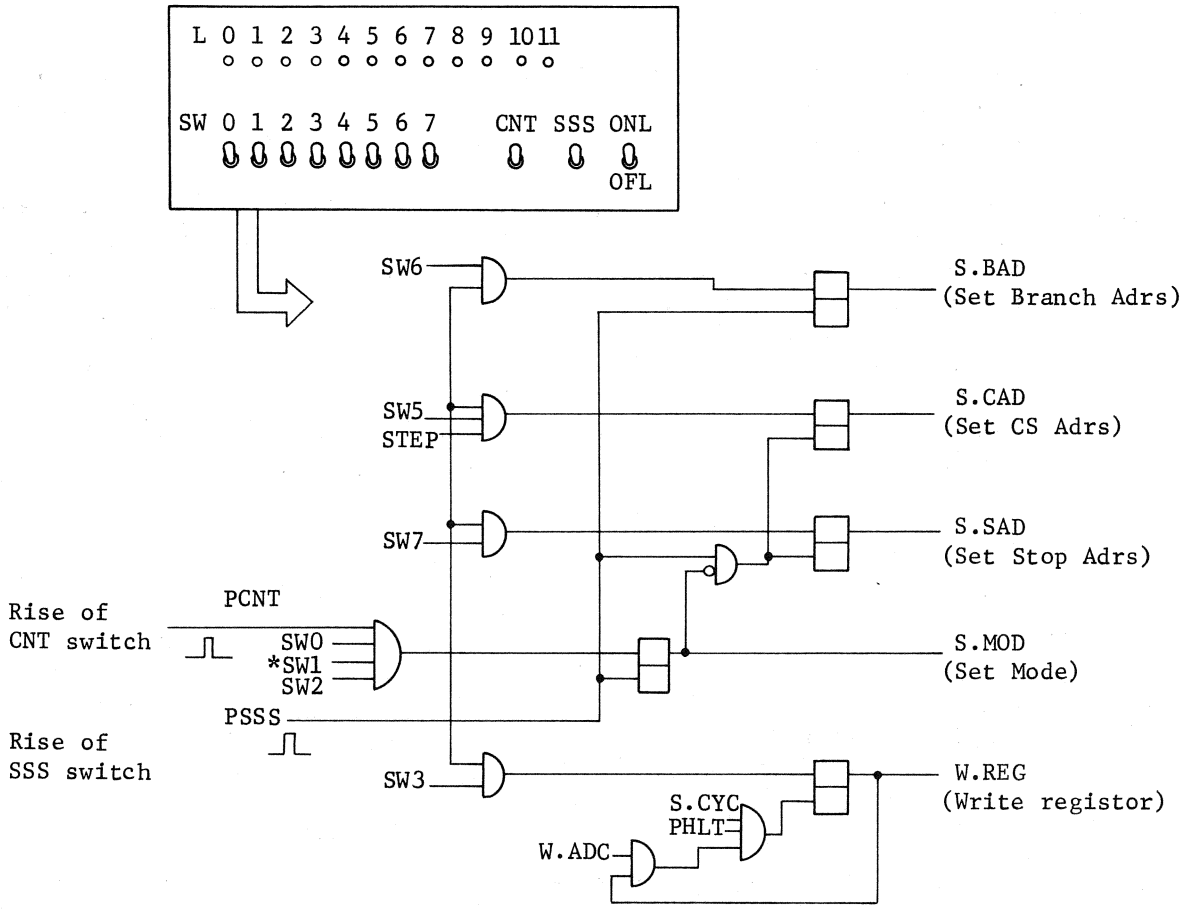


Figure 4.9 Input mode control over switches

(1) Step

As shown in Figure 4.10, if the CNT switch is set on, with the SW0, SW1, and SW2 switches set to ON, then a Set MP-Control (S.MPC) signal is set on. If the SW4 switch has then been set on, the STEP bit is set on. The Step signal generates a Processor Halt (PHLT) signal at the timing of fetching an instruction so that the processor is halted under the condition of the RCY (See Subsection 4.4.2.). Then, the PHLT signal is reset for one instruction period whenever the SSS switch is operated. Thus, instructions are executed one by one. The G.CYC signal becomes '1' while the SW0 to SW7 switches are operating in the control information input mode. Even if the SSS switch is then set on, no PHLT signal is reset and the processor does not step further.

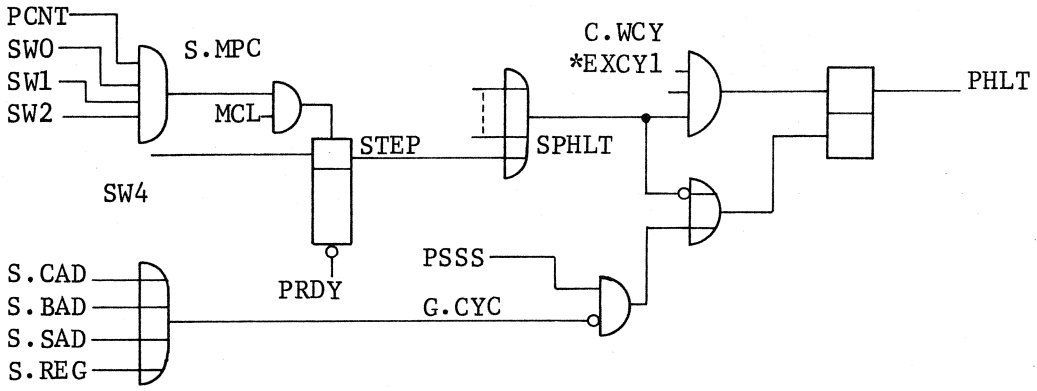


Figure 4.10 Halt control

(2) Address Compare/Address Compare Stop

If the CNT switch is set on, with the SW0 to SW2 switches set to '101' and the SW7 switch set to '1', then S.SAD and S.MOD signals are set on and the SW0 to SW3 switches are set to the high order compare address input mode. Then, data is entered to stop addresses 0 to 3 (SAD0 to SAD3) by the SSS switch, then the S.MOD signal is reset so that the low order compare address (SAD4 to SAD11) can be entered. Thus, the address set in the SAD register is compared with CA0 to CA11 within the comparator. If the result of the comparison (P.C=S signal) is output and the S.ADC bit has been set on, then a PHLT signal is set on. Then, if the SSS switch is set on, the address compare latch signal (F.C=S) and the PHLT signal are reset.

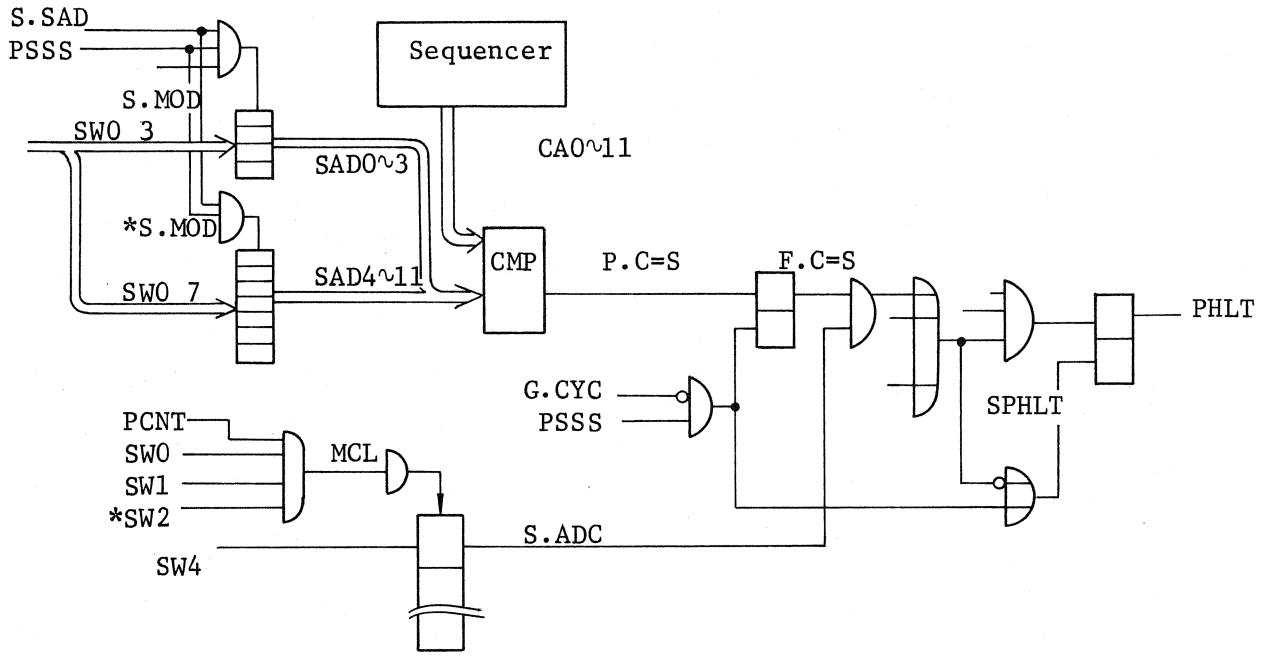


Figure 4.11 Address Compare & Stop

(3) Register Write/Register Display

As shown in Figure 4.12, if a PHLT signal is set on, then the contents of SW1 to SW7 are output to register addresses RA0 to RA6 and the contents of the RWD register are output to the output data bus of the processor. While the PHLT signal is set on, data is written and displayed on the register. Data is set on the read/write data (RWD) register in the following way: set the SW0 to SW3 switches to '1011' and set the CNT switch to '1' (this operation causes the SW0 to SW7 switches to be set to the RWD register input mode); set the SW0 to SW7 switches to desired data; set the SSS switch to ON. The W.REG signal directs the register write mode. The Steal Cycle (S.CYC) signal serves as a write strobe (W.REG) signal for Register Write/Display.

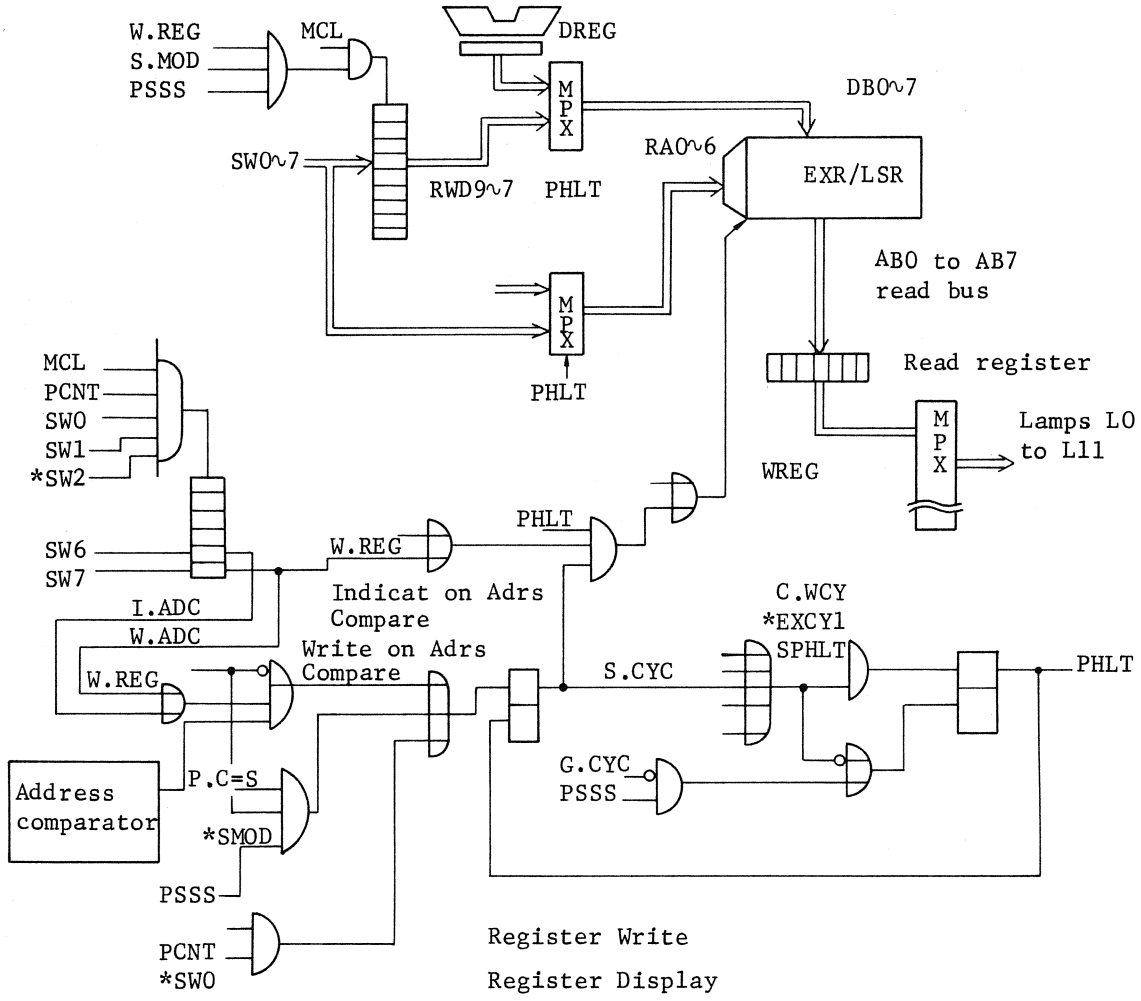


Figure 4.12 Register Write/Display

(4) Microprogram Address Set

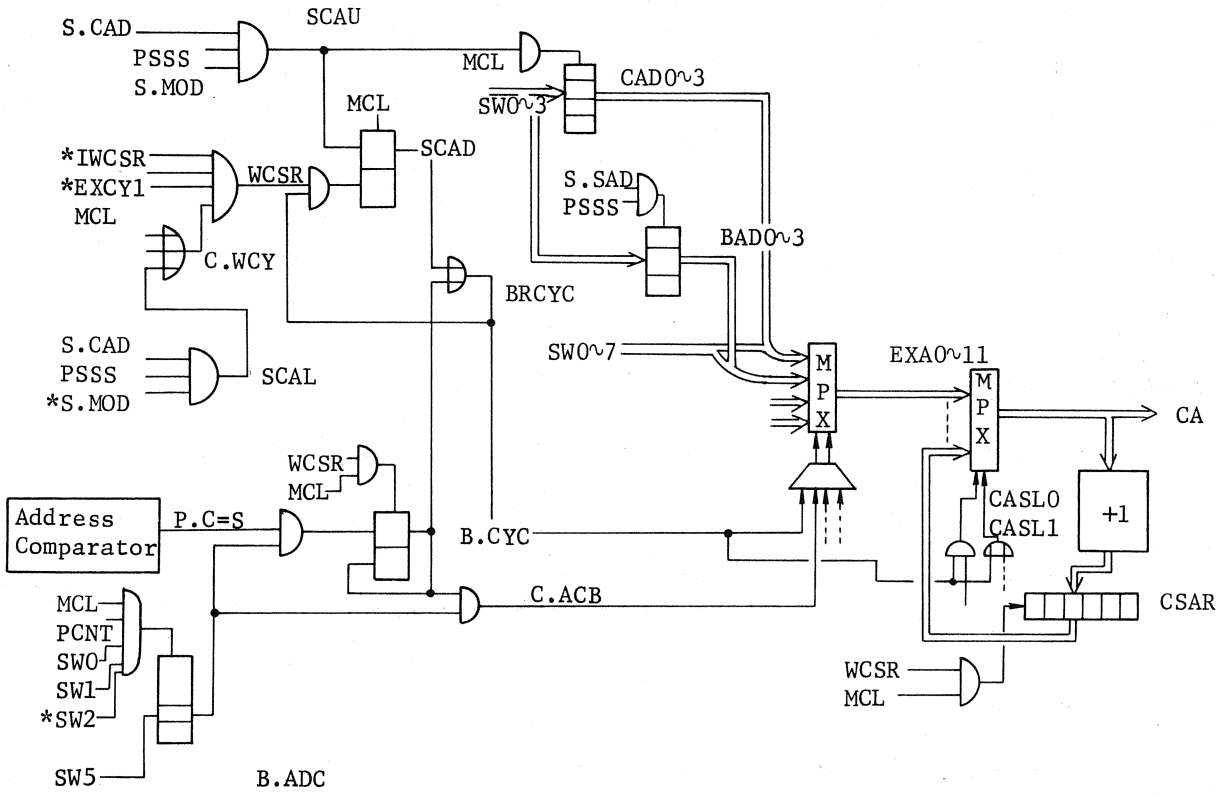


Figure 4.13 CA Set

As shown in Figure 4.13, if the CNT switch is set on, with the SW0 to SW3 switches set to '101', then S.CAD and S.MOD signals are set on, the CA set mode resulting. Then, if the SSS switch is set on, with SW0 to SW3 set to the high order four bits of the CS address (microprogram address), then the CAD register is set to the data in SW0 to SW7. The S.MOD signal is then reset. Then, if SW0 to SW7 are set to the contents of the low order eight bits of the CS address, then the CA signal is switched to the contents of the BAD register and SW0 to SW7. Finally, if the SSS switch is set on, then the instruction at the specified address is loaded on the CSR, the address register being updated.

(5) Address Compare Branch

If the CNT switch is set on, with SW0, SW1, and SW2 set to '110', then the B.ADC bit is set on so that this function is activated. If address comparison is successful when the B.ADC bit is '1', then a B.CYC signal is set on and the CA signal (microprogram address) is switched to the contents of the high order four bits of the BAD register set beforehand and the contents of SW0 to SW7 (low order eight bits). Then, the branch function is activated so that the instruction stored at the address specified by the BAD register and SW0 to SW7 can be executed next. Figure 4.25 shows the associated circuits.

(6) CS Scan

If the ROS function (ROSF) bit is set on, then a ROSF signal is set on and the C.WCY signal always becomes '1'. This causes the contents of the CS to be read into the CSR at every clock (MCL) pulse, the address register being counted up one by one. If a parity error occurs during scanning, then an Inhibit Write-CSR (IWCSR) signal is set on to halt the processor.

4.4.5 Microprogram instructions

Every instruction to be executed in the microprocessor is of 32-bit fixed length format. The processor provides 38 types of mnemonic instructions each of which can perform branching/conditional branching/operating and storing data in a register. This subsection describes the functions, bit patterns, and cycle lengths of the respective instructions.

Also, ASSEMBLER coding schemes are inserted for referring to the assemble list.

Unconditional Branch instructions

[1] B (Branch Uncondition)

```
B    destination
```

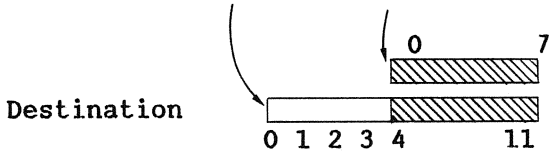
Unconditionally branches to the destination.

```
Example: B   LABEL1
         B   *
         B   X'256'
```

2 BI (Branch Indirect)

BI destination, register specification.

Branches to the address resulting from replacing the low order eight bits of the destination address represented by the above destination operand with the contents of the register specified by the register specification operand.



Example: B CMDDEC, R1

3 CALL (Call Subroutine)

CALL subroutine name.

Branches to the subroutine, with the next address stacked.

Example: CALL SUB1

4 CALLI (Call Subroutine Indirect)

CALLI subroutine name, register specification.

Branches to the subroutine address resulting from replacing the low order eight bits of the destinated subroutine address value with the contents of the register specified by the register specification operand, with the next address stacked before the branching.

Example: CALLI SUBX, R0

Conditional Branch instructions

5 BOC (Branch On Condition)

BOC condition specification, destination.

Branches to the destination if the condition register is in the status specified by the condition specification operand.

Condition register =DREG — Method of specifying conditions

ALL0	all bit = 0
CAR	CAR bit on
ANY1	any bit = 1
NCAR	CAR bit off

Example:
```
BOC   ALL0, RDEND
BOC   ANY1, STOPWT
```

6 BOCI (Branch On Condition Indirect)

BOCI condition specification, destination, register specification.

Conforms to BOC except that the destination address depends on the high order four bits of the destination and the contents (eight bits) of the specified register.

Example:
```
BOCI   CAR, LABEL1, R3
```

7 COC (Call Subroutine On Condition)

COC condition specification, subroutine name.

Branches to the subroutine specified by the subroutine name operand if the condition register is in the status specified by the condition specification operand.

Example:
```
COC   ANY1, GOUP
```

8 COCI (Call Subroutine On Condition Indirect)

COCI condition specification, subroutine name, register specification

Conforms to COC except that the called subroutine address depends on the high order four bits of the address specified by the subroutine name operand and the contents (eight bits) of the register specified.

Example:
```
COCI   NCAR, SUB1, R6
```

Test Bit system instructions

[9] TBB (Test Bit & Branch)

TBB condition specification, register specification, test bit specification, destination within page. (Note)

Branches to the destination if the bit corresponding to the test bit specification = '1' among contents of the register specified by the register specification operand is in the status specified by the condition specification operand.

ALL0	all bit 0
ALL1	all bit 1
ANY1	any bit 1
ANY0	any bit 0

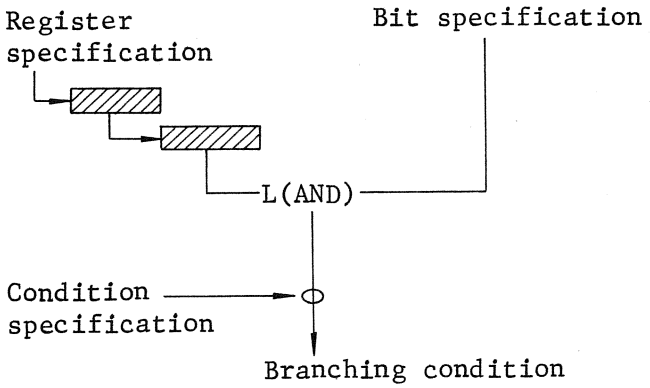
```
Example:   TBB   ANY1, WREG, X'0F', LABEL1
           TBB   ALL0, RL, 4, GOON1
```

Note; "Page" means 512 adrs boundary.

[10] TBBI (Test Bit & Branch Indirect)

TBBI condition specification, register specification, test bit specification, destination within page

Branches to the destination if the bit corresponding to the test bit specification = '1' among contents of the register specified by the register specification operand is in the status specified by the condition specification operand. For the condition specification operand, conform to TBB.

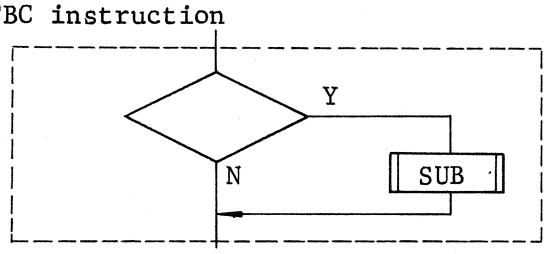



```
Example:   TBBI   ANY0, R1, X'=0', LABEL2
           TBBI   ALL1, REG1, 4+2+8+16, START1
```

11 TBC (Test Bit & Call Subroutine)

TBC condition specification, register specification, test bit specification, subroutine name within page

Executes the subroutine specified by the subroutine name operand if the result of ANDing the contents of the register specified by the register specification operand with the test bit specification becomes the status specified by the condition specification operand. If the condition is not satisfied or a Return instruction in encountered in the subroutine, then the next instruction is executed.



For the condition specification operand, conform to the TBB instruction. Also, the ANDed result remains in the DREG (condition register).

Example: TEC ANY1, AREG, X'24', SUBABC
TEC ALL0, R1, B(456-8), GOUPSUB

12 TBCI (Test Bit & Call Indirect)

TBCI condition specification, register specification, mask data, subroutine name within page

Executes the subroutine specified by the subroutine name operand if the result of ANDing the contents of the register indirectly specified by the contents of the register specified by the register specification operand with the mask data becomes the status specified by the condition specification operand. The ANDed result remains in the DREG. For the condition specification operand, conform to the TBB instruction.

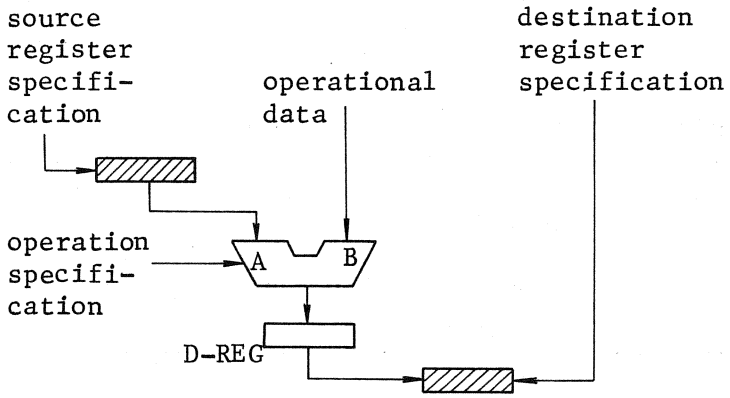
Example: TBC1 ANY0, R0, 80+40, SUB0

MV system (register-constant operation system) instructions

13 **MV (Move)**
MV* (Move & Return)

MV / MV*	source register specification	operation specification	constant	destination register specification
	,	,	,	

Performs the operation specified by the operation specification operand between the contents of the register specified by the source register specification operand and the operational data, then stores the result of the operation in the register specified by the destination register specification operand.



- The operated result remains in the DREG.
- The MV* instruction is accompanied with a return from the subroutine.
- The operation specification operand conforms to the Table 4.6

Table 4.6

	Operation specification	Data to be stored	Abbreviation
F=B	IMD	Data written in the operational data operand	C
	DREG	DREG contents	D
F=A.B	AND	(Source register contents)* (Operational data)	A
F=AVB	OR	(Source register contents) V (Operational data)	O
F=A+B	EOR	(Source register contents) + (Operational data)	E
F=A	SREG	Source register contents	S
F=A+B	PLS	(Source register contents) + (Operational data)	P
F=A-B	MNS	(Source register contents) - (Operational data)	M

where A and B refer to source data.

```
Example:  MV    R1, AND, X'F2', R1
          MV*   R2, PLS, 31, R3
```

13a STR (Store Register)
STR* (Store Register & Return)

```
STR
STR*    data, register
```

Sets the register specified by the second operand to the data specified by the first operand.

These instructions conform to the following MV and MV* instructions:

```
MV
MV*     0, IMD, data, register
```

```
Example:  STR    X'30', R1
          STR*   D(256-38), W0
```

13b MVR (Move Register)
MVR* (Move Register & Return)

```
MVR
MVR*    source register, destination register
```

Stores the contents of the source register into the destination register.

The contents of the source register remain in the DREG.

These instructions conform to the following MV and MV* instructions:

```
MV
MV*     source register, S, 0, destination register
```

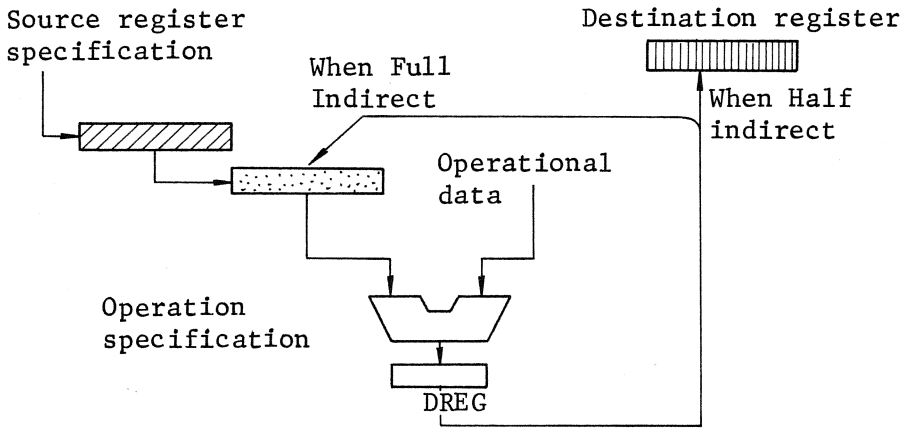
Example: MVR R1, R2

14 MVFI (Move Full Indirect)
MVHI (Move Half Indirect)
MVFI* (Move Full Indirect & Return)
MVHI* (Move Half Indirect & Return)

```
MVFI    source     operation   operational  [ destination  ]
MVHI    register   specifi-    data         | register     |
MVFI*   specifi-   cation                   | specification|
MVHI*   cation   ,           ,              ,[ (*1)        ]
```

1 Write this operand only for MVHI and MVHI instructions.

Performs the operation specified by the operation specification operand between the contents of the register specified indirectly by the contents of the register specified by the source register specification operand and the operational data, then stores the operated result into the register indirectly specified by the contents of the register specified by the source register specification operand for a MVFI or MVFI* instruction; into the register specified by the destination register specification operand for a MVHI or MVHI* instruction.



The operated result remains in the DREG.
The MVFI* and MVHI* are accompanied with a return from the subroutine.
The operation specification operand conforms to that of the MV instruction.

```
Example:  MVFI    R0, OR, 512
          MVHI    R0, PLS, B(310), REGABC
          MVFI*   AREG, EOR, X'32'
          MVHI*   X, MNS, 32-5+8, R4
```

15 LD (Load D-register)
LD* (Load D-register & Return)

```
   LD    source
   LD*   register     operation     operational
         specifi-     specifi-      data
         cation     , cation      ,
```

Performs the operation specified by the operation specification operand between the contents of the register specified by the source register specification operand and the operational data, then sets the DREG to the operated result.

The contents of registers other than the DREG do not change.

The operation specification operand conforms to that of the MV instruction.

The LD* instruction is accompanied with a return from the subroutine.

```
Example:  LD    XREG, IMD, X'43'
          LD*   W0, PLS, 1
```

16 LDI (Load D-register Indirect)
LDI* (Load D-register Indirect & Return)

```
IDI     source
IDI*    register      operation      operational
        specifi-      specifi-       data
        cation      , cation       ,
```

Performs the operation specified by the operation specification operand between the contents of the register indirectly specified by the contents of the register specified by the source register specification operand, then sets the DREG to the operated regults.

These instructions alter no contents of registers other than the DREG.

The operation specification operand conforms to the MV instruction.

The LDI* instruction is accompanied with a return operation.

```
Example: LDI    EXR0, SREG, X'80'
         LDI*   W0, AND, B(40+80)
```

MF system (inter-register operation system) instructions

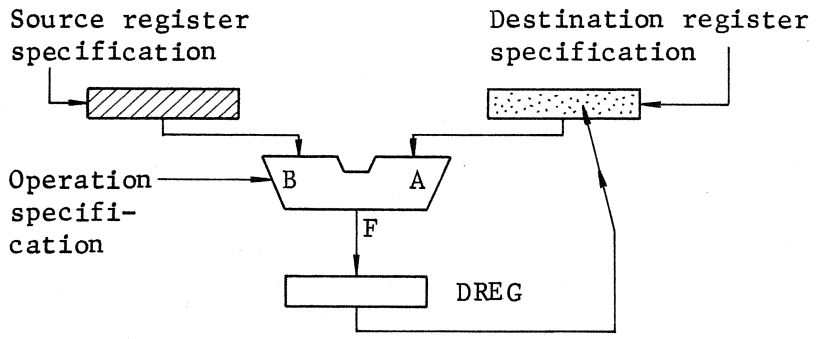
17 MF (Modify)
MF* (Modify & Return)

```
MF      source
MF*     register      operation      destination
        specifi-      specifi-       register
        cation      , cation       , specification
```

Performs the operation specified by the operation specification operand between the contents of the register specified by the source register specification operand and the register specified by the destination register specification operand, then stores the operated result into the destination register.

The operated result remains in the DREG.

The MF* instruction is accompanied with a return from the subroutine.



The operation specification operand of any MF system instruction can be specified as follows:

Table 4.7

	Specification	Operation
F=$\bar{A}$.B	NA	$\overline{\text{(Source register)}}$ * (Destination register)
F=$\bar{A}$VB	NO	$\overline{\text{(Source register)}}$ V (Destination register)
F=A.B	AND or A	(Source register) * (Destination register)
F=AVB	OR or O	(Source register) V (Destination register)
F=A ⊕ B	EOR or E	(Source register) ⊕ (Destination register)
F=$\overline{\text{A ⊕ B}}$	EN	$\overline{\text{(Source register) ⊕ (Destination register)}}$
F=A+B	PLS or P	(Destination register) + (Source register)
F=A-B	MNS or M	(Destination register) - (Source register)

where A: destination
B: source

```
Example:    MF    R1, A, BREG
            MF    R0, NO, R1
```

18 MFD (Modify D-register)
MFD* (Modify D-register & Return)

```
MDF   source
MFD*  register      operation      destination
      specifi-      specifi-       register
      cation      , cation       , specification
```

Performs the operation specified by the operation specification operand between the contents of the source register and those of the destination register, then stores the operated result into the DREG.

Conforms to the MF and MFD* instructions except that the operated result is not stored into the destination register.

The MFG* instruction is accompanied with a return operation.

The operation specification operand conforms to that of the MF and MF* instructions.

Example: MFD R1, NA, R2

Replational instructions

19 BEQ (Branch If Equal)

```
BEQ     register specification, relational data, destination
        within page
```

Branches to the destination if the contents of the register specified by the register specification operand coincide with the relational data.

The result of EORing the contents of the register with the relational data remains in the DREG.

Example: BEQ W0, X'43', LABEL2

20 BEQI (Branch If Equal Indirect)

```
BEQI    register specification, relational data, destination
        within page
```

Branches to the destination if the relational data coincides with the contents of the register with the address contained in the register specified by the register specification operand.

The result of the EOR operation remains in the DREG.

Example: BEQ I0, 100, AAA01

21 CEQ (Call Subroutine If Equal)

CEQ register specification, relational data, subroutine name within page

Branches to the subroutine specified by the subroutine name operand if the relational data coincides with the contents of the register specified by the register specification operand.

The result of the EOR operation remains in the DREG, similar to the BEQ instruction.

Example: CEQ W2, 523, SUB1

22 CEQI (Call Subroutine If Equal Indirect)

CEQI register specification, relational data, subroutine name within page

Branches to the subroutine specified by the subroutine name operand if the relational data coincides with the contents of the register with the address contained in the register specified by the register specification operand.

The result of the EOR operation remains in the DREG.

Example: CEQI R1, X'3A', SUBX

23 BNE (Branch If Not Equal)

BNE register specification, relational data, destination within page

Branches to the destination specified by the destination operand if the relational data does not coincide with the contents of the register specified by the register specification operand.

The result of the EOR operation remains in the DREG.

Example: BNE R1, X'01', LABEL3

24 BNEI (Branch If Not Equal Indirect)

BNEI register specification, relational data, destination within page

Branches to the destination specified by the destination operand if the relational data does not coincide with the contents of the register specified by the register specification operand.

The result of the EOR operation remains in the DREG.

25 CNE (Call Subroutine If Not Equal)

CNE register specification, relational data, subroutine name within page

Branches to the subroutine specified by the subroutine name operand if the relational data does not coincide with the contents of the register specified by the register specification operand.

The result of the EOR operation remains in the DREG.

26 CNEI (CNE Indirect)

CNEI register specification, relational data, subroutine name within page

Branches to the subroutine specified by the subroutine name operand if the relational data does not coincide with the contents of the register with the address contained in the register specified by the register specification operand.

The result of the EOR operation remains in the DREG.

MLI instruction

27 MLI (Machine Language Immediate)

MLI instruction code (bits 0 to 31)

Generates the instruction specified by the instruction code operand. Specify this instruction optionally if a code other than the codes specified in ASSEMBLER is to be assembled. Try to avoid using this instruction except in special cases, such as remodeling ROMs, etc.

Parities are automatically generated.

Example: MLI X'40235136'

ASSEMBLER instructions

ORG (Origin)

ORG address value specification

Sets the location counter to the value specified by the address value specification operand.

Example: ORG X'300'

EQU (Equivalence)

symbol definition EQU equivalent representation

Declares that the representation specified by the symbol definition operand matches the equivalent representation operand.

Define the equivalent representation before this instruction.

```
Example:   LABEL1     EQU       LABEL3
           R0         EQU       0
           ZERO       EQU       X'00'
           ALLONE     EQU       X'FF'
```

Do not use the representations used in ASSEMBLER: ALL1, ANY1, OR, AND, etc.

SPACE (Space): List control

```
    SPACE   line count specification
```

Leaves out space for the line count specified by the line count specification operand on the assemble list.

```
Example:       SPACE   10
```

EJECT (Eject)

```
    EJECT
```

Slews the top-of-page on the assemble list.

DS (Define Storage)

```
    DS   address reservation specification
```

Leaves out free space for the number of addresses specified by the address reservation specification operand.

The address reservation specification operand conforms to the following:

```
       nH  :    REserves 2xn addresses
       nC  :    Reserves n addresses
       nX  :    Reserves n addresses
       0B  :    256 boundaries
       nB  :    2^n boundaries (1≤n≤16)
```

```
Example:    DS   4H
            DS   0B
```

Table 4.8 Bit patterns (1/3)

Mnemonic	0 1 2	3 4	5 6	7 8 9 10 11 12 13	14 15 16 17 18	19 20 21 22 23 24 25 26 27 28 29 30	31
B	1 0 0	0 0		Source register address		Branch address	P
BI		1 0				Branch address	
CALL		0 1				Subroutine address	
CALLI		1 1				Subroutine address	
BOC	1 0 1		RV C			Branch address	P
BOCI		1 0				Branch address	
COC		0 1				Subroutine address	
COCI		1 1				Subroutine address	
TBB	1 1 0	0 0	RV C	Source register address*	Mask data (Test bit data)	Branch address	P
TBBI		1 0					
TBC		0 1				Subroutine address	
TBCI		1 1					
BEQ	1 1 1	0 0	0 0	Source register-address*	Mask data	Branch address	P
BEQI		1 0					
CEQ		0 1				Subroutine address	
CEQI		1 1					

Table 4.8 Bit patterns (2/3)

Mnemonic	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
BNE	1	1	1	0	0	1	0	Source register address*							Mask data								Branch address									P
BENI				1	0																											
CNE				0	1																		Subroutine address									
CNEI				1	1																											
MV	0	0	0	0	A	L	U	Source register address							Operation data								0	0	Destination address							P
MV*			1	0																												
MVHI			0	1																												
MVHI*			1	1																												
MVFI			0	1																				1								
MVFI*																																
LD	0	0	0	0																			1	0								P
LDI			0	1																												
LD*			1	0																												
LDI*			1	1																												

Table 4.8 Bit patterns (3/3)

Mnemonic	0	1	2	3	4	5	6	7	8 9 10 11 12 13	14 15 16 17 18 19 20 21	22	23	24 25 26 27 28 29 30	31
MF			0								0			
MF*			1						Source register address		0		Destination address	
MFD	0	1	0		A	L	U				1			P
MFD*			1								1			

* Each source register address marked an asterisk takes an indirectly specified register address for an indirectly specified instruction.

▨ The shaded sections contain all '0's.

▩ The dotted sections are replaced with indirect addresses.

Table 4.8 Bit patterns (continued)

Specification code		
MV system	MF system	ALU
IMD, C	NA	0 0 0
DREG, D	NO	0 0 1
AND, A	AND, A	0 1 0
OR, O	OR, O	0 1 1
EOR, E	EOR, E	1 0 0
SREG, S	EN	1 0 1
PLS, P	PLS, P	1 1 0
MNS, M	MNS, M	1 1 1

Specification condition	RV C
ALL0	0 0
NCAR	0 1
ANY1	1 0
CAR	1 1

Specification condition	RV C
ALL0	0 0
ALL1	0 1
ANY1	1 0
ANY0	1 1

Format and cycle count

Table 4.9 Format and cycle count (1/2)

Mnemonic operation code	Operands	Cycle count (*1)
B	Destination	2ø
CALL	Subroutine name	2ø
BI	Distination, register	3ø
CALLI	Subroutine name, register	3ø
BOC	Condition, destination	3ø
COC	Condition, subroutine name	3ø
BOCI	Condition, destination	3ø
COCI	Condition, subroutine name	3ø
TBB	Condition, register, test bit, destination within page	3ø
TBBI	Condition, register, test bit, destination within page	5ø
TBC	Condition, register, test bit, subroutine name within page	3ø
TBCI	Condition, register, test bit, subroutine name within page	5ø
BEQ	Register, data, destination, within page	2ø
BEQI	Register, data, destination, within page	4ø
BNE	Register, data, destination, within page	2ø
BNEI	Register, data, destination, within page	4ø
CEQ	Register, data, subroutine name within page	2ø
CEQI	Register, data, subroutine name within page	4ø
CNE	Register, data, subroutine name within page	2ø
CNEI	Register, data, subroutine name within page	4ø

Table 4.9 Format and cycle count (2/2)

Mnemonic operation code	Operands	Cycle count (*1)
MV	Source register, operation, data, destination register	
MV*	Source register, operation, data, destination register	
MVHI	Source register, operation, data, destination register	
MVHI*	Source register, operation, data, destination register	
MVFI	Source register, operation, data	4ø
MVFI*	Source register, operation, data	4ø
STR STR*	Data, register	2ø
MVR MVR*	Source register, destination register	2ø
LD	Source register, destination register	2ø
LD*	Source register, destination register	2ø
LDI	Source register, destination register	4ø
LDI*	Source register, destination register	4ø
MF	Source register, operation, destination register	
MF*	Source register, operation, destination register	
MFD	Source register, operation, destination register	
MFD*	Source register, operation, destination register	

*1: The cycle counts take values from the EPROM mode, where ø is 208 ns.

4.5 Registers

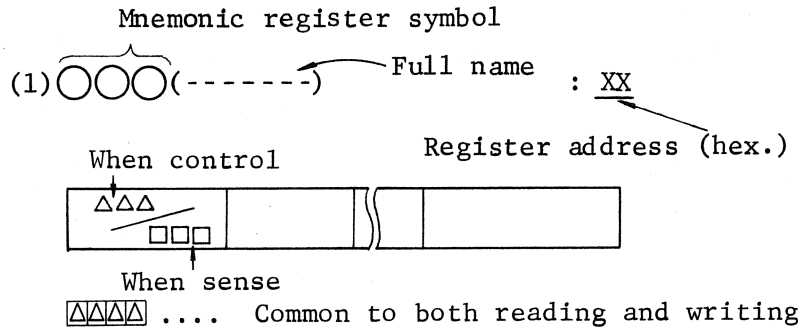
This section describes the registers to control the microprocessor. The microprocessor has seven bits of address lines RA0 to RA6 with which up to 128 bytes of registers are addressed.

The leading 64 bytes of the registers are known as the local storage register (LSR) area; the tailing 64 bytes are known as the external register (EXR) area.

The LSR area with register addresses X'00' to X'3F' consists of a RAM (9 bits x 64 bytes) whose each byte has its own parity bit. The EXR area with register addresses X'40' to X'7F', i.e. the control registers area for the interface control section, write/read control section, etc. has no parity bits.

Register addresses X'68' to X'7F' are unused by the MTCs.

The following shows the notation of these registers:



Abbreviations:

µP:	Microprogram
FTP:	Full Tacho-pulse signal
QTP:	Quarter Tacho-pulse signal
MCY:	Machine Cycle signal
VFO:	Variable frequency oscillator; this chapter refers to the demodulation section.

4.5.1 LSR

(1) DVENQ0 to DVENQ7 (Device enquiry #0 to #7): 00 to 07

These registers store the status of reserved MTUs (RSVA0 to RSVA7 and RSVB0 to RSVB7) and the presence of inquiries for each MTU and channel interface.

Bits 0 to 7 of local enquiry A/B (LENQA/B) are set on when the channel is reported that the IRQ bit of the sense byte is set to '1', then is used to post a DVE status interrupt when the MTU has no longer been in any IRQ status. Bits 0 to 7 of busy enquiry A/B are set when a BSY status is responded and becomes a source of a later DVE status interrupt. See Subsections 5.5.1 and 5.5.2.

(2) MODEM (Mode memo): 08

This register stores the recording density mode of the MTC for each channel interface. CUB memory A/B (CUBMA/B) stores that a CUB status is responded so that it can be used to report a CUE status later.

(3) SCANP (Scan Pointer): 09

Bit 5, 6, 7 is device address for Idle Scan routine.
CCF is flag memory for Command chain.

(4) DSB (Device status byte): 0A

This register helps generate a response status to a channel.

(5) LCMD (Last command): 0B

This register stores temporarily the last command issued to the MTC.

(6) DVS0, 1, 3, 8 (Device status 0, 1, 3, 8): 0C to 0F

These registers store temporarily the sense bytes information of MTUs to be controlled by the MTC. This saves the MTC from fetching MTU sense bytes information repeatedly.

(7) W0 to W7 (Work registers 0 to 7): 10 to 17

These are work registers.

4.5.2 EXR

(1) TMCTL (Timer control): 40

0	1	2	3	4	5	6	7
MCT0	MCT1	CQTP	FLAG	R.CNT/ S.CNT	RCTRU/ CTRU	R.FTP/ DFTP	R.QTP/ DQTP

(a) MCT0, MCT1, CQTP (Mode controls 0 and 1, count QTP)

These registers specify timer count modes.

Table 4.10 Timer control modes

MCT0	MCT1	CQTP	Count mode
0	0	x	1.66 µsec clock timer
1 1	0 0	0 1	FTP counter QTP counter
x x	1 1	0 1	FTP period counter (*1) QTP period counter (*1)

*1: The following shows the count clock of the FTP/QTP period counter.

Table 4.11

Speed (IPS)	Count clock (ns)	Normal FTP period (µs)
200	208	47.1
125	208	75.4
75	208	125.66
50	208	188

These registers are reset by SERT signals or directions from a microprogram.

(b) ERRF (Error flag)

If this bit is set on, then the ERRF lamp (lamp 8) is lit. This flag shows errors to the CE panel operator. This flag is reset by a microprogram or a SERT signal.

(c) R.CNT/S.CNT (Reset counter/Start counter)

These counters control the start/Stop of the timer. If data is set in the upper area of the timer, then the S.CNT bit is set to '1' so that the timer can start to count. If the timer is then generating no overflow output (T.TMR='0'), then counting starts. Counting continues until an overflow results. However, even before an overflow, if only this bit is set to '1' (R.CNT='1'), then the S.CNT bit is reset to stop counting. A SERT signal also resets the S.CNT bit.

(d) R.CTRU/CTRU (Reset counter upper entry mode/Counter upper entry mode)

A CTRU signal is set on when data is read/written from/to the timer in the upper R/W mode. If the CTRU signal is reset, the lower R/W mode results.

If this bit is set to '1' (R.CTRU '1'), then the CTRU signal is reset.

A SERT signal also resets the CTRU signal. If data is read/written from/into the upper area of the timer (data is read/written at address '41' when CTRU='0'), then a CTRU signal is set to '1'. Thus a microprogram can read/write continuously data from/into the timer in ascending order.

(e) R.FTP/DFTP

If a FTP is detected after a MCY signal is set on, then the DFTP bit is set on. The DFTP bit is reset if this bit is set to '1' (R.FTP='1') or the MCY signal is reset.

(f) R.QTP/DQTP

If a QTP is detected after a MCY signal is set on, then the DQTP bit is set to '1'. If this bit is set to '1' (R.QTP '1') or the MCY signal is reset, then the DQTP bit is reset.

(2) Time (Timer data): 41

This register contains data to be read/written from/into the timer. The above CTRU signal controls switching between the upper and lower R/W modes.

The timer starts to count (S.CNT '1') when data is set on the upper area. Counting continues until a count overflow (carry output) results and T.TMR becomes '1'.

0	1	2	3	4	5	6	7
CT0(CT8)	CT1(CT9)	CT2(CTA)	CT3(CTB)	CT4(CTC)	CT5(CTD)	CT6(CTE)	CT7(CTF)

Counters in parentheses apply to the lower R/W mode.

Data is set on the read register once at the timing of QTP or FTP (only while the timer is operating in the QTP or FTP period counter mode: MCT1 = '1') and is read later.

Figure 4.14 shows the timer circuit (16-bit counter).

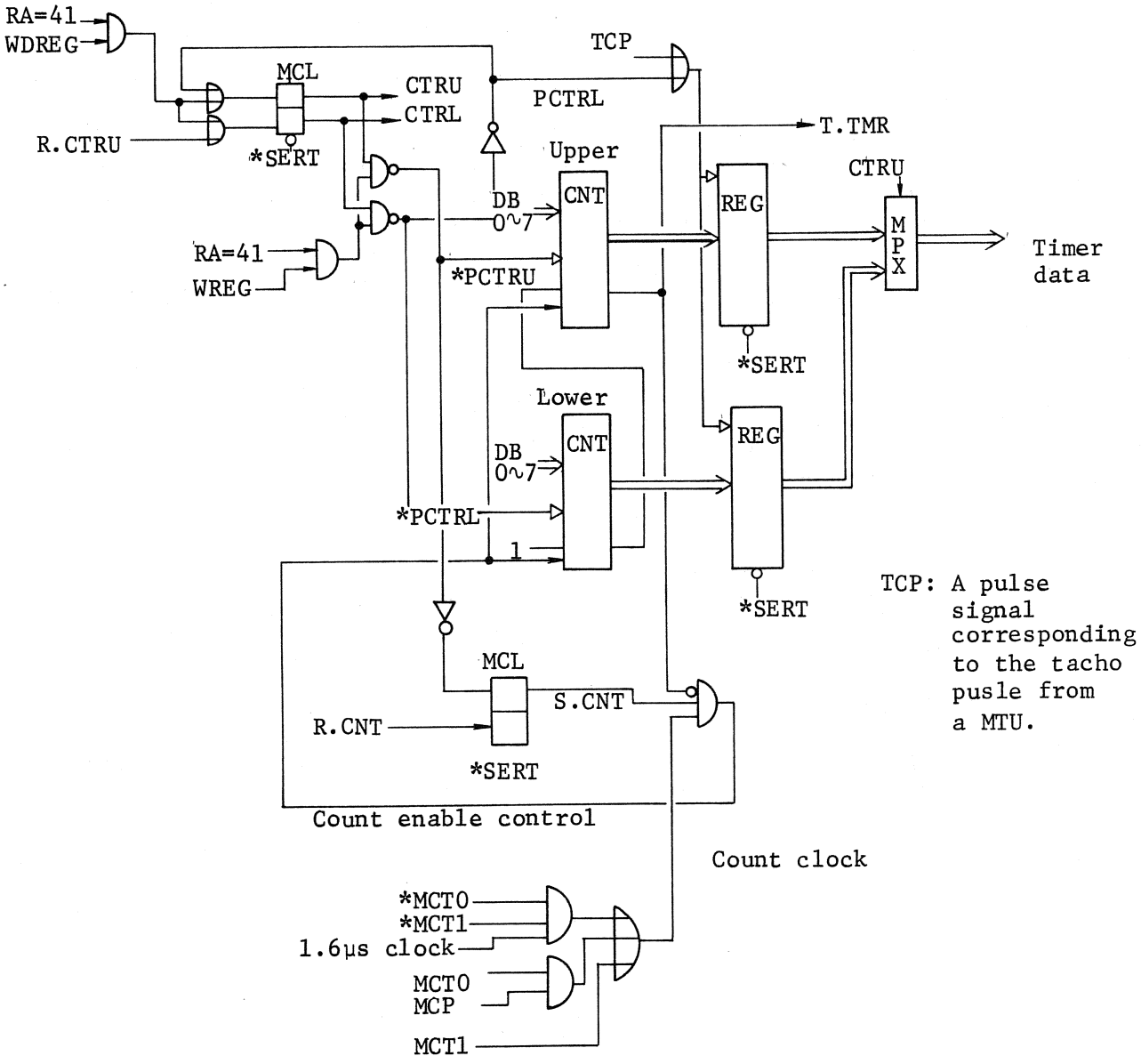


Figure 4.14 Timer circuit

(3) DVSEL (Device select): 42

0	1	2	3	4	5	6	7
$\overline{\text{TAGI}}$	$\overline{\text{XCAL}}$	*$\overline{\text{DVENB}}$	SLTAG	$\overline{\text{DVBSY}}$	DVA0	DVA1	DVA2

(a) TAGI (Tag-in)

A Tag In signal for a selected MTU.

(b) XCAL (X-call)

The XCAL signal, showing that the device cross-call feature is enabled, is '1' while the distributer is operating in the dual MTCs mode (When DGBM is equipped).

(c) *DVENB (Not Device Enable)

This bit is '0' while the Device Enable switch on the operator panel for the MTU selected by the DVA0 to DVA2 bits of the SLTAG as shown later is set to 'Enable'. This bit is always set to '0' if the operator panel is not equipped.

(d) DVBSY (Device busy)

This bit is '1' while a device cannot be selected from the corresponding channel because the device is being selected by the other MTC or has been reserved since it was selected by the other MTC.

(e) SLTAG (Select tag)

This bit is set to '1' when the MTU with the device address indicated at DVA0 to DVA2 is selected. If DVBSY='0', then the corresponding device remains selected by the corresponding MTC until the SLTAG bit is set to '0'. The SLTAG bit is reset by a SYRT signal.

(f) DVA0 to DVA2 (Device addresses 0 to 2)

These bits indicate a device address (absolute address) to be selected. They remain unchanged until they are set once more by a microprogram or reset to '000' by a SYRT signal.

(4) DVRSV (Device reserve): 43

0	1	2	3	4	5	6	7
RSV0	RSV1	RSV2	RSV3	RSV4	RSV5	RSV6	RSV7

This register controls the reserve/release status of devices. All bits of this register are reset when powering on or switching the ONL/OFL switch on the CE panel.

While a device is occupied by one MTC, the RSV bit for the device must be set on. In such a case, the other MTC cannot use the device (DVBSY='1').

The RSV bits remain unchanged until a microprogram resets them. All RSV bits are reset when powering on or switching the ONL/OFL switch on the CE panel.

Each RSV bit is generally set on while the corresponding device is successfully selected (SLTAG='1').

(5) DVTAG (Device tag): 44

0	1	2	3	4	5	6	7
GO	TAGVL	TAG0	TAG1	DBMPX	TSP0	TSP1	VHSP

(a) GO (Device go)

This bit conveys a GO signal to a selected device.
This bit is reset while MCY is off.

(b) TAGVL (Tag valid)

This bit is valid only while DBMPX='0'. While DBMPX='0', A TAGVL signal is sent as a strobe signal to a device. The contents of DB00 to DB07 are strobed on the device side (at the rise of the TAGVL signal).

This bit is reset while MCY is off.

(c) TAG0 (Tag 0)

This bit conveys a Status Tag signal to a selected device. The MTC detects and sets the status of the selected device with this signal: set DBMPX to '0'; set DB00 to DB07 to status information; Set the TAGVL bit to on/off.

The TAG0 bit is reset while MCY is off.

(d) TAG1 (Tag 1)

This bit conveys a Control Tag signal to a selected device. The MTC detects control information and directs operations: set DBMPX to '0'; set control information to DB00 to DB07; set the TAGVL bit to on/off. The TAG1 bit is reset while MCY is off.

(e) DBMPX (Device bus multiplex)

This bit assigns any of device-bus-outs 0 to 7 to a selected device and switches Write Clock signals.

Table 4.12

	Device-Bus-out	WCL	
DBMPX="1"	WMDT0~7	WTPL	When writing
DBMPX="0"	DB00~7	TAGVL	When reading Interfacing with MTUs

This bit is reset by a SERT signal.

(f) TSP0, 1 (Tape speed codes 0 and 1)

These two bits specify a tape speed. These bits are cleared by a SERT signal (TSP0, 1='00').

Table 4.13

TSP0	TSP1	Speed
0	0	50 IPS
0	1	75 IPS
1	0	125 IPS
1	1	200 IPS

These bits switch the timing of the read/write circuit and the MTC clocking.

(g) VHSP (VFO high speed)

The VFO can accommodate itself to two levels of speed. If this bit is set to '1' the VFO operates at the faster of the two.

This bit is reset by a SERT signal.

(6) DVBO (Device bus-out): 45

0	1	2	3	4	5	6	7
DBO0	DBO1	DBO2	DBO3	DBO4	DBO5	DBO6	DBO7

This register conveys a Bus Out signal to a selected device. Information set on DBO0 to DBO7 is given meanings by three tag signals (GO, TAG0, and TAG1). If the GO tag is set to '1', then DBO0 to DBO7 contain status specification information. If TAG1 is set to '1', then DBO0 to DBO7 contain control operation specification information.

If the three tags are all '0's, then the sense byte of an MTU for each of DBO0 to DBO7 is requested to be sent. (The sense information is obtained on the bus-in.)

Information set on this register is sent to the device only when DBMPX='0'. This register is reset by a SERT signal.

(7) DVBI (Device bus-in): 46

0	1	2	3	4	5	6	7
DBI0	DBI1	DBI2	DBI3	DBI4	DBI5	DBI6	DBI7

Three tags (GO, TAG0, and TAG1) give meanings to the bus-in information. If the GO tag is set to '1', then DBIs 0 to 7, p contain read data.

If TAG1 is set to '1', then DBIs 0 to 7 contain MTU control detection information.

If the three tags are all '0's, then the sense byte of an MTU corresponding to each of DBOs 0 to 7 is sent to each of DBIs 0 to 7.

DBIs 0 to 7 contain all '0's while SERT='1'.

(8) DVSNS (Device sense): 47

0	1	2	3	4	5	6	7
GAPC	CPFWD	MPXBO	M.TCS	VLOK	R.VLC / VLCHG	TCSG	TCSP

(a) GAPC (Gap control)

This bit conveys a GAPC signal to a selected device. If the GO tag is set to '1' during a read/write operation or when an IBG is passed over from the end of a block. This bit is always '0' while a SERT signal is set on.

(b) CPFWD (Capstan forward)

This bit is set on while the capstan motor of a selected device is rotating forwards (or the CPA is delayed 90 degrees). This bit is reset while MCY is off.

(c) MPXBO (Multiplex bus-out)

If this bit is set to '1', the contents of DBOs 0 to 3 (upper area) are read into DBOs 4 to 7 (lower area). When the contents of the upper four bits of byte data are shifted to the lower four bits, this bit is set on. This bit is reset while MCY is off.

(d) M.TCS (Mask tacho-pulse-stop trap)

This bit masks the occurrence of a trap due to a TCSP signal (Tach Stop), as will be described later, that occurs when the period of arrival of tach pulses from an MTU has increased. The above trap is enabled while this bit is '1'. This bit is reset while MCY is off.

(e) VLOK (Velocity OK)

This bit is set to '1' while the period of arrival of FTPs from a selected device falls within a specified range. This bit is reset while MCY is off.

(f) R.VLC (CLCHG) (Reset velocity change/Velocity change)

This bit is set to '1' when the period of arrival of FTPs from a selected MTU during a write operation of the MTC falls without a specified range. This bit remains unchanged until MCY is off or it is reset by setting it to '1' (R.VLC='1').

(g) TCSG (Tacho-stop gate)

This bit gates the set entry of a TCSP signal, as will be described later. If this bit is set to '1', then no TCSP signal is set even if the period of arrival of FTPs from a selected device increases. This bit is reset while MCY is off.

(h) TCSP (Tacho-stop)

The TCSP bit becomes '1' when the FTP period counter within the MTC overflows and the TCSG bit is set to '1' as a result of an increase of the period of arrival of FTPs from a selected device.

The TCSP signal remains unchanged until it is reset by MCY OFF.

The following shows overflow times.

Table 4.14 TCSP overflow time

Tape speed	Nominal period	TCSP detection time
200 IPS	47.1 µs (100%)	208 µs x 1 x (2^{12}-1)= 851 µs (5.5%)
125 IPS	75.4 µs (100%)	208 µs x 2 x (2^{12}-1)=1703 µs (4.4%)
75 IPS	125.7 µs (100%)	208 µs x 3 x (2^{12}-1)=2555 µs (4.9%)
50 IPS	188 µs (100%)	208 µs x 4 x (2^{12}-1)=3406 µs (5.5%)

(9) MASK (Mask): 48

0	1	2	3	4	5	6	7
MASK0	MASK1	MASK2	MASK3	MASK4	MASK5	MASK6	MASK7

Bits containing '1' of this register are masked without sending write data if the mask bit as will be described later is '1'. Also, if the ISPHE bit is set to '1', then a PHE (Phase Error) signal is generated at each bit containing '1'. This register is reset by a HCLR signal.

(10) DACTL (Diagnostic control): 49

0	1	2	3	4	5	6	7
DMW	DMR	IHPRE	IHPOS	INVLD	ALMSK	MASK	MASK8

(a) DMW (Diagnostic mode write)

This bit is set to '1' when data is written in the diagnostic mode.

This bit is reset by a HCLR signal.

Table 4.15 Functions of DMW

Mode	When INVLD = '0'	When INVLD = '1'
6250	When a sub data group contains data '11xx', the entire sub data group is masked. (*)	When a sub data group contains data '11xx', the sub data group data is replaced with invalid data. (*1)
1600/800	As long as tracks (bits) contain write data '1's in succession, the tracks (bits) are masked.	

*1 Invalid for a residual data group and a CRC data group in the 6250 mode.

(b) DMR (Diagnostic mode write)

This bit is set to '1' when data is read in the diagnostic mode.
This bit is reset by a HCLR signal.

Table 4.16 Functions of DMR

Mode	Function
6250	Check bytes and data are transferred to memory.
1600	Invalid.
800	CRC byte, LRC byte, and data are sent to memory.

(c) IHPRE (Inhibit preamble)

This bit is set to '1' if the preambles of all tracks are masked when data is written in the 6250 or 1600 BPI mode. For the 800 BPI mode, this bit is invalid. This bit is reset by a HCLR signal.

(d) IHPOS (Inhibit postamble)

This bit is set to '1' when the postambles of all tracks are masked during a write operation in the 6250 or 1600 BPI mode. This bit is invalid for the 800 BPI mode. This bit is reset by a HCLR signal.

(e) INVLD (Invalid code)

This bit qualifies the details of DMW operation when data is written in the 6250 BPI diagnostic mode. It is valid only when DMW '1'. (See DMW.) This bit is reset by a HCLR signal.

(f) ALMSK (All mask)

If this bit is set to '1', then write data sending from the MTC to an MTU is masked. Masking is effected at the same time as this bit is set to '1', without synchronizing with the write clock. This bit is reset by a HCLR signal.

(g) MASK (Mask enable)

If this bit is set to '1', then write data sending at bits containing '1' of MASK0 to MASK8 is masked. Masking is effected as soon as this bit is set to '1', without synchronizing with the write clock. This bit is reset by a HCLR signal.

(h) MASK8 (Mask 8)

This bit directs to mask parity bits. See Item (9) also.

(11) WTCTL (Write Control): 4A

0	1	2	3	4	5	6	7
WTM	IBW	WEC	AL1WT	WOK	-	$\overline{\text{BFUL}}$	$\overline{\text{R.BCY}}$ / $\overline{\text{BCY}}$

(a) WTM (Write Tape Mark)

This bit is set of '1' to execute a Write Tape Mark operation in 6250/1600/800 BPI modes. The format counter sequence is set to tape mark write sequence when this bit is set to '1'.

In 6250/1600 BPI modes, ALIWT, WOK and WEC bits must also be set along with this bit (bits 1, 3, 4 must be masked).

The WEC bit is reset to '0' after the required length of data has been entered. (Bit count is done by microprogram using R.BCY/BCY bits).

The processing in 800 BPI mode is the same as in 6250/1600 BPI modes except that WEC bit is not set for Tape Mark Write Operation. (There is no need to count the data length with microprogram).

WTM bit is reset by HCLR signal.

(b) IBW (IB Write)

This bit is set to '1' for 6250/1600 ID Burst Write Operation. The data transmitted to MTU is in 1600 BPI IB format. Bits WEC, WOK, and ALIWT must be set along with this bit to execute an IB write processing. WEC bit will be reset after entering the required length of data.

This bit is reset by HCLR signal.

(c) WEC (Write End Control)

In Write operation if this bit is set to '1', the format counter stops at '13' and the processing stops till this bit is reset to '0'. This bit is set in operations like 6250/1600 BPI mode IB Write, tape mark write etc. and is used to control the data length.

In such cases IB, ARA, ARAID and tape mark data is sent till the format counter reaches 13.

This bit is reset by HCLR signal.

(d) ALlWT (All 1 Write)

This bit is set to '1' to specify a all '1' Write operation format of 9042 fci/3200 fci/800 fci. In 6250/1600 BPI mode IB Write, tape mark write operation, this bit must be set along with IBW and WTM bits respectively. This bit is reset by HCLR signal.

Now 3014 fci '1000' pattern is employed in 6250 IB Write operation.

(e) WOK (Write OK)

This bit is set to '1' to enable the Write circuit and to start a Write operation. Modulation circuit, slip check circuit, noise check circuit and the format counter are started when this bit is set to '1'. WOK is reset when the format count reaches '15' (upon entering postamble or LRCC). This bit is reset if MCY is turned OFF.

(f) Bit 5 is a spare bit and is permanently set to 0.

(g) BFUL (Buffer Full)

This bit is set to '1' to indicate that the channel Buffer (64 bytes) on the data transfer control side is full. (This does not apply if the CBR (channel buffer read) bit is also set to '1'). This bit is always '0' if CBR bit is set to '1'.

(h) R.BCY/BCY (Reset Byte Cycle/Byte Cycle)

Set this bit to '1' to reset the BCY signal. Now BCY signal will be set again to '1' after 8 bit cells in 6250 BPI mode, 4 bit cell in 1600 BPI mode, and 2 bit cells in 800 BPI mode. The status of this signal will then remain unchanged, until this bit is set again to '1'. Microprogram use this bit to count and control write data length.

(12) RDCTL (Read Control): 4B

0	1	2	3	4	5	6	7
ROK	STPHK	VFOS	IHDXF	IHCOR	*HIG	ISPHE	SKWMG

(a) ROK (Read OK)

Read circuit is set to Enable when this bit is set to '1'. This bit is reset by HCLR signal.

(b) STPHK (Stand-By Phase OK)

This bit is set to '1' to permit setting of PHOK signal. PHOK signal is reset immediately if this bit is set to '0'. Therefore PHOK signal may be set only if this bit has been set (It is set by HBLK). The above mentioned SLIPC and NOISE signals are set only while STPHK bits are ON.

*PHOK signal is reset after detection of postamble (EPOSA signal=1) in 6250/1600 BPI modes. However in 800 BPI mode, it is not reset till STPHK is reset.

STPHK bit is reset by HCLR signal.

(c) VFOS (VFO Start)

The loop filter condenser of the VFO circuit discharges while this bit is OFF. This bit should be set to '0' for a certain period of time to completely discharge the capacitor. The VFO circuit is set to Enable status when this bit is set to '1'. The VFO circuit is controlled by WTCLK signal till the receipt of time sense signal. Upon receipt of the time sense signal, VFO is reset for 1 peak pulse period to resynchronise with the data peak pulse. Then it is controlled by the data. (ROK must be set to '1' to generate a time sense signal).

(d) INDXF (Inhibit Data Transfer)

This bit is set to '1' to mask the data transfer request signal (DXRQ signal) from the Read/Write control section to data transfer control section even if conditions for generating the DXRQ signal have been established in the Read/Write control section.

Now DXRQ signal may be generated only if this bit is set to '0'.

This bit is employed in 800 BPI read operation to mask TM, CRC, LRC byte transfer and to start the control related to data transfer between the channel buffer and read/write control section. This bit is reset by HCLR signal.

(e) IHCOR (Inhibit Correction)

This bit is turned ON to inhibit error correction operation in 6250/1600 BPI mode. This bit reset or set along with the ROK bit (it should at least be set during data byte detection operation). This bit is reset by HCLR signal.

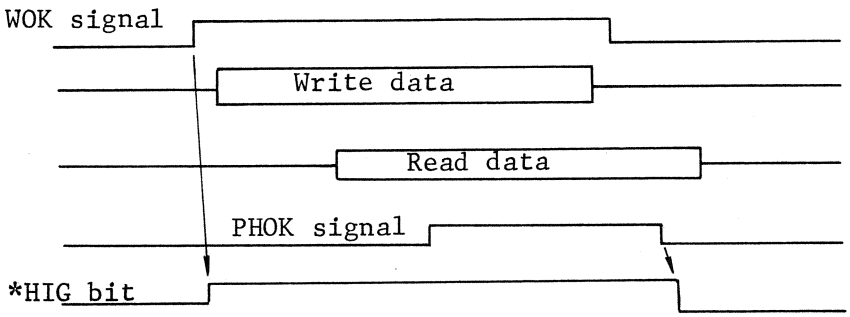
(f) *HIG (Not High Gain)

This bit is employed to alter the synchronization of the clock with data in a VFO circuit (increases the VFO loop gain). The VFO loop gain is high while this bit is set to '0'. This indicates that the synchronization capacity has increased. By setting this bit to '1' (low gain), VFO loop gain is set to normal level thus generating a very stable (low jitter) cell clock. This bit is reset by HCLR signal which sets it to a low gain status.

This bit must be set to '1' in 1600 BPI mode Read/Write operation.

In 6250 BPI mode, this bit should be controlled as shown in the following figure.

(1) Write operation



(2) Read operation

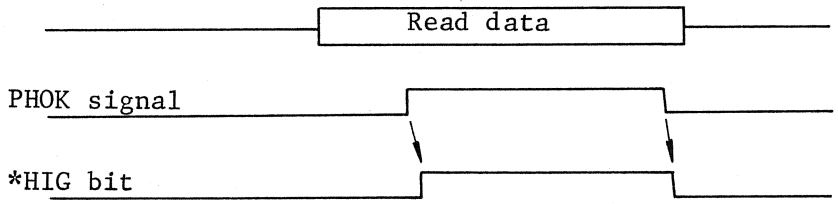


Figure 4.15 *HIG bit control in 6250 BPI mode

(g) ISPHE (Issue Phase Error)

This bit is used to generate a phase error. A phase error is (PHE) generated in the track corresponding to the MASK bit 0-9 which have been turned ON. (For further details refer to Chapter 9).

This bit is reset by HCLR signal.

(h) SKWMG (Skew Marginal)

The skew check condition is set to marginal as soon as this bit is turned ON. This bit may be used only in 1600 mode.

This bit is reset by HCLR signal.

(13) MODE (Mode Select): 4C

0	1	2	3	4	5	6	7
MCY	BWD	WKS	ZRD	6250	1600	CMCY	CBR

(a) MCY (Machine cycle)

The MCY signal is turned ON to enable Read, Write, Device Control Circuits. In this stage these circuits may be controlled from microprogram while MCY signal is ON.

This bit is reset by HCLR signal.

(b) BWD (Backward)

This bit is turned 'ON' (set to 1) to set the MTC Read circuit to Backward Mode. This bit is read by HCLR signal.

(c) WRS (Write Status)

This bit is turned ON (set to '1') to set the MTC R/W circuit to Write Mode.

The following check conditions may be affected by this bit: HNIS (Noise Block) check condition.

Postamble Read End (EPOSA) condition. STRCK (Start Read Check) condition. HTM (tape mark detection, skew mark, error correction and other control conditions. Read status is set when this bit is '0'. This bit is reset by HCLR signal.

(d) NRD (NRZ Read)

This bit is set to execute 800 BPI, Read/write operation. When this bit is on the modulation circuit will generate a peak pulse as the data rises if the BWD bit is '1' and a peak pulse as the input data falls if the BWD bit is '0'. Both the pulses are generated as peak pulses.

This bit is reset by HCLR signal.

(e) 6250 (6250 mode)

This bit is set to '1' to execute 6250 BPI Read/Write operation. This bit is reset by HCLR signal.

(f) 1600 (1600 mode)

This bit is set to '1' to execute read/write operation in 1600 BPI mode.

This bit is reset by the HCLR signal.

(g) CMCY (Complete MCY)

This bit is not used. This bit is reset by HCLR signal.

(h) CBR (Channel Buffer Read)

This bit is set to '1' to execute a channel buffer Read operation. As soon as this bit is set to '1', the data transmit control section repeatedly transfers the channel buffer data. This bit is reset by HCLR signal.

(14) RDSNS (Read Format Sense): 4D

0	1	2	3	4	5	6	7
HNIS	HBLK	HTM	WIND	PHOK	PREA	POSA	EPOSA

(a) HNIS (Noise Block Detected)

If a noise pattern is detected (DNois=1) for a duration described in Table 4.17 this bit is set to '1'. This bit remains unchanged till ROK is turned OFF. ROK is OFF.

Table 4.17 HNIS set condition

Mode		Condition
6250	WRS	46 ± 2 Bit cell period, continuous PNOIS
	RDS	22 ± 2 Bit cell period, continuous PNOIS
1600	WRD	23 ± 2 Bit cell period, continuous PNOIS
	RDS	11 ± 1 Bit cell period, continuous POINS

This bit is not set in 800 BPI mode.

(b) HBLK (Block Detected)

If a block pattern (DBOB='1') is detected for a duration in excess of the specified bit cell period, this bit is set to '1'. This bit remains unchanged till it is reset when ROK is turned OFF. This bit is in Reset status while ROK is OFF.

Table 4.18 HBLK set condition

Mode		Condition
6250	WRS	25 ± 1 Bit cell period, continuous DBOB
	RDS	25 ± 1 Bit cell period, continuous DBOB
1600	WRS	12.5 ± 0.5 Bit cell period, continuous DBOB
	RDS	12.5 ± 0.5 Bit cell period, continuous DBOB

This bit is not set in 800 BPI mode.

(c) HTM (Tape Mark Block Detected)

If a tape mark block pattern (DTM='1') is detected continuously in excess of the specified bit cell period, this bit is set to '1'. This bit remains unchanged till reset when ROK is OFF. This bit is reset while ROK is OFF.

Table 4.19 HTM setting condition

Mode		Condition
6250	WRS	304 ± 8 Bit cell period, continuous DTM
	RDS	42 ± 2 Bit cell period, continuous DTM
1600	WRS	84 ± 4 Bit cell period, continuous DTM
	RDS	21 ± 1 Bit cell period, continuous DTM

This bit is not set in 800 BPI mode.

(d) WIND (Window)

In Write operation, this signal becomes '1' during a specified period after specified delay time has elapsed from starting Write operation. The leading of the block recorded in the corresponding write operation should be detected while this signal is '1'. The data bytes (800) or DBOB detected between

the period from starting the Write Operation till rise of this signal. Will set NOISC signal (described later) to '1'.

The SLIPC (described later) will be set to '1' if Wind Signal is set to '0' without detecting a data byte (800) or DNOIS signal. Figure 4.15 shows set and reset timing of WIND signal.

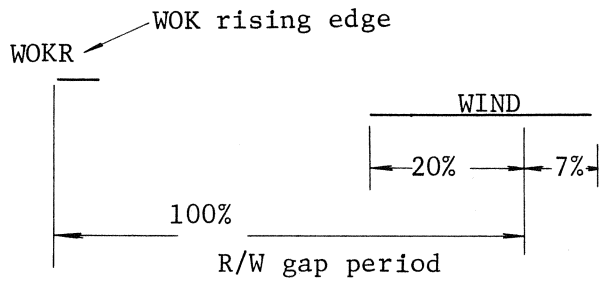


Figure 4.16 WIND signal

(e) PHOK (Phase OK)

This signal is set while HBLK signal rises when STPHK has been set. This signal is reset when the EPOSA signal rises (described later) or STPHK is reset. While this signal is ON, Write data error check and correction are available.

(f) PREA (Preamble Detected)

This signal is set to '1' upon detection of the first data byte in the 6250, 1600 BPI Read Circuit. The status of this signal remains unchanged till PHOK is reset. This bit is in reset status while PHOK is '0'.

(g) POSA (Postamble Detected)

This signal is set to '1' upon detection of the last data byte (Head of Postamble) in 6250, 1600 BPI Read Circuit. This bit remains unchanged till PHOK is reset. This bit remains in reset status while PHOK is '0'.

(h) EPOSA (End of Postamble)

This bit is set to '1' after the specified length of postamble is confirmed in 6250, 1600 BPI Read/Write operation. This bit is reset ('0') when DIBG signal rises. This bit is in reset status while MCY is OFF.

Table 4.20 EPOSA set condition

Mode		Condition
6250	WRS	After POSA=1 and after a delay of 34 ± 2 bit cells.
	RDS	After POSA=1 and after a delay of 6 ± 2 bit cells.
1600	WRS	After POSA=2 and after a delay of 31 ± 1 bit cells.
	RDS	After POSA=1 and after a delay of 21 ± 1 bit cells.

(15) CRCST (CRC Status): 4E

0	1	2	3	4	5	6	7
*MCRC	*MCRCZ	*EP=CR	*B=D	*B=C	*MCRCC	*A=B	*XBIC

(a) *MCRC (Unmatch CRC)

This bit is when the CRC pattern generated as a result of operating on the Read Data (including CRC byte) is not normal (bits other than 2, 4 of CRC register are ON). This bit is employed in Read, Write, and Back Read operations in 6250, 800 mode. This bit is ON ('1') when MCY is OFF.

(b) *MCRCZ (Unmatch CRC zero)

This bit is '1' when the CRC pattern generated as a result of operating on Read data (including CRC pattern) is not all '0's. This bit is employed in Read, Write and Back Read Operations in 800 mode. This bit is '0' when MCY is OFF.

(c) *EP=CR (EP≠CR)

This bit is '1' if the pattern obtained by reversing the pattern (except bits 2, 4) generated by operating on the Read data (including CRC byte) does not match with the error pattern register. It is used for detecting errors along with the *MCRCZ signal in 800 mode. This bit is set to '1' while MCY is OFF.

(d) *B=D (CRCB≠CRCD)

This bit is employed in Read, Write operations (excluding Back Read) in 6250 mode. This bit is turned ON ('1') when the Aux-CRC byte (CRCD) does not match with the CRCB pattern (CRC generated from transfer Buffer output). This bit is '1' while MCY is OFF.

(e) *B=C (CRCB≠CRCC)

This bit is employed in 1600, 800 mode write operation. This bit is turned ON when the Write Data CRC pattern (obtained from CRCB - XFR buffer output) does not match with the After Read data (excluding CRC byte) CRC pattern. This bit is set to '0' while MCY is OFF.

(f) *MCRCC (Unmatch CRCC)

This bit is '1' when the CRC pattern obtained from Read Data (excluding CRC byte) is not normal. This bit is employed in Back Read processing in 6250 mode. This bit is '1' while MCY is off.

(g) *A=B (CRCA≠CRCB)

This bit is '1' when the pattern generated from the input data to XFR buffer does not match with the CRC pattern generated from XFR register output data. This bit is '0' while MCY is OFF.

(h) *XBIC (*XBF Bus In Check)

This bit is set when illegal XFR Buffer Input data pattern is detected. This bit is not reset until MCY is turned OFF. This bit is '0' while MCY is OFF.

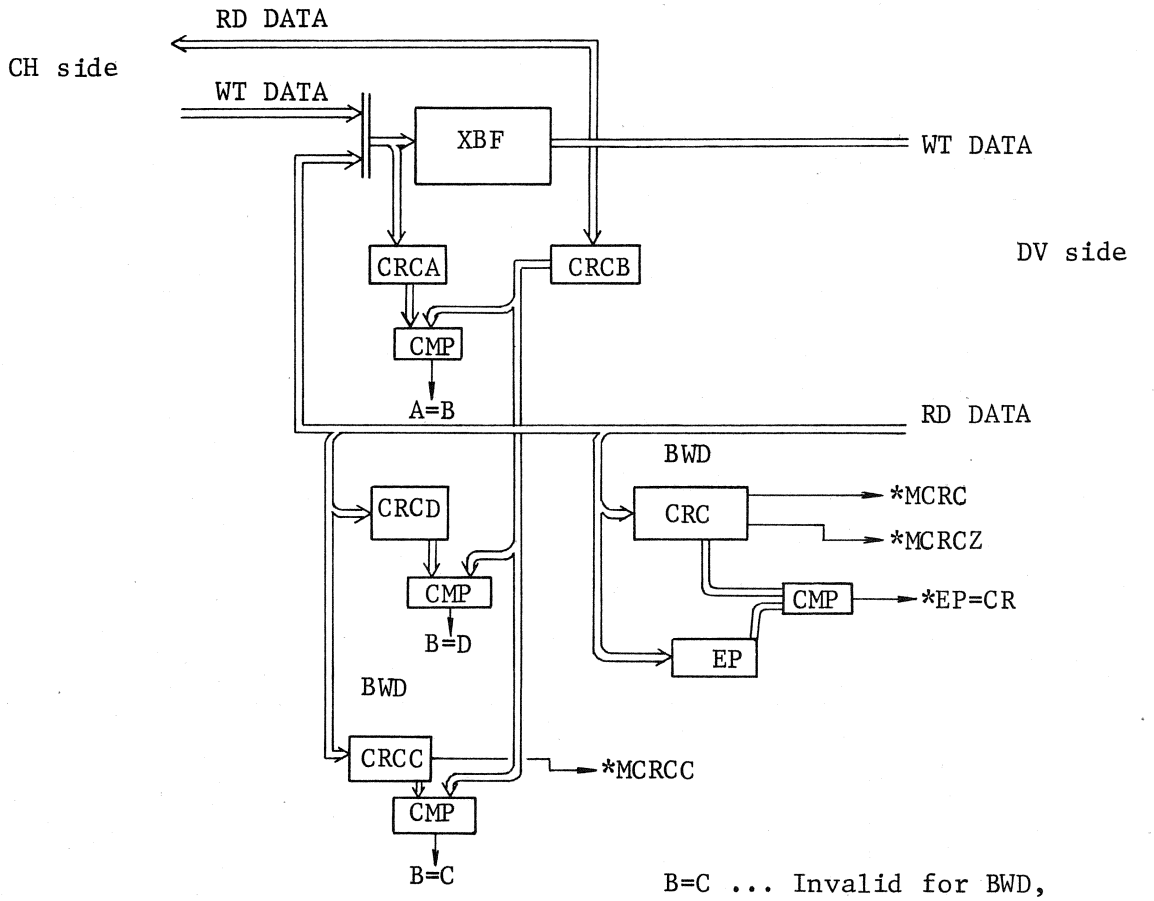


Figure 4.17

Table 4.21

Mode	Input Byte Operation				
	CRCA	CRCB	CRC	CRCC	CRCD
6250	XBF Input data (Write→Write Data, Read→Read Data)	XBF Output data (Write→Write Data, Read→Read Data)	Data, Pad, Aux. CRC CRC Byte, 1 Byte	Data, Aux. CRC (BRD only)	Aux, CRC (BRD not feasible)
1600				Data	
800			Data, CRC	Data	

(16) FMERR (Format Error): 4F

0	1	2	3	4	5	6	7
/*SRDC	/*EDCK	/*SLIPC	/*NOISC	/*WTBOC	/*WTVRC	/*OVRN	/*CMP

(a) *SRDC (Not Start Read Check)

This bit is turned ON, if the PREA signal (Start of Data Field Detection Signal) is not set within the specified delay time after PHOK. This signal remains at '0' till MCY is OFF. This bit is '1' while MCY is OFF. This bit, '1', means that Start Read Check error has not been detected in the Read Operation.

Table 4.22 SRDC Set condition

Mode		Condition
6250	WRS	When PREA=0 upon specified delay of 120 ± 8 bit cells after PHOK set.
	RDS	When PREA=0 upon specified delay of 168 ± 8 bit cells after PHOK set.
1600	WRS	When PREA=0 upon specified delay of 52 ± 4 bit cells after PHOK set.
	RSD	When PREA=0 upon specified delay of 63 ± 4 bit cells after PHOK Set.

This bit is not available in 800 BPI mode.

(b) *EDCK (Not End Data Check)

This bit is turned ON if DIBG signal cannot be detected within the specified time after EPOSA (see Table 4.23 for a specified time delay after preamble). Once set to '0' it is not reset ('1') till MCY is OFF. It is '1' while MCY is OFF. This bit, '1' may be assumed that End Data Check Error has not occurred in the Read Operation.

Table 4.23 EDC Condition

Mode		Condition
6250	WRS	When DIBC=0 upon delay of 88 ± 8 bit cells after EPOSA=1.
	RDS	When DIBC=0 upon delay of 248 ± 8 bit cells after EPOSA=1.
1600	WRS	When DIBC=0 upon delay of 20 ± 4 bit cells after EPOSA=1.
	RDS	When DIBC=0 upon delay of 36 ± 4 bit cells after EPOSA=1.

Not available in 800 BPI mode.

(c) *SLIPC (Not Slip Check)

This bit is set to '0' upon detection of data write (800 BPI) or DNOIS signal (6250/1600 BPI) while the above mentioned WIND signal (section (14), d) is '1'. Once set to '0', the status of this signal remains unchanged till MCY is turned OFF. This bit is '1' while MCY is '1'.

This bit, '1', may be assumed that no slip check error has occured in Write Operation. This bit is '1' when MCY or STPHK is '0'.

(d) *NOISC (Not Noise Check)

This bit is set to '0' when data byte (800 BPI) or DBOB signal (6250/1600 BPI) is detected within the specified delay time after starting Write Operation (WOK Rise). Once set to '0' the status of this signal remains unchanged till MCY is turned OFF. This bit is '1' when MCY is OFF. This bit is '1' when MCY or STPHK signal is '0'.

(e) *WTBOC (Not Write Data Bus-Out Check)

This bit is set to '0' when a parity error is detected in the Write Bus Data to be entered to the Write Circuit. This bit is not set to '0' when the above mentioned WTCTL register ALIWT bit is set to '0'.

This bit remains in '0' status while MCY is OFF. This bit is set to '1' by HCLR signal. When this bit is '1' it may be assumed that no parity error has occurred in Write Circuit during Write Operation.

(f) *WTVRC (Not Write VRC)

This bit is set to '0' when a parity error is detected in the modulated Write Data . Once set to '0' the status of this byte remains unchanged till MCY is turned OFF. When this bit is '1' it may be assumed that no parity error has occurred in modulated data in Write Operation.

(g) *OVRN (Not Over Run)

This bit is set to '0' when overrun is detected in Read/Write Operation. Once set to '0' the status of this bit remains unchanged till MCY is turned OFF. This bit is '0' when MCY is OFF. When this bit is '1', it may be assumed that overrun error has not been detected in Read/Write Operation.

- OVRN Set Condition -

1. When DXF1=1 (Read Operation)

   . If XFR Buffer is Full (BFUL=1)

2. DXFO=1 (Write Operation)

   . If XFR Buffer became empty (CMP=1) before receiptor "transfer STOP" from the channel interface during Write Operation.

   . If the data left in the XFR buffer was less than 6 bytes before the "transfer STOP" was issued by the channel interface in 6250 mode Write operation.

(h) *CMP (Not Compare)

This bit is set to '0' if the XFR buffer Read-In count and Read Out count do not match. This bit indicates the presence or absence of data in XFR buffer. There is no data in XFR buffer if this bit is '0' and there is data in the buffer if this bit is '1'. This bit is '0' when MCY is OFF.

(17) TSNS (Time Sense): 50

0	1	2	3	4	5	6	7
*TSNS0	*TSNS1	*TSNS2	*TSNS3	*TSNS4	*TSNS5	*TSNS6	*TSNS7

Each of these bits is '0' when the peak pulse of the tracks rising and falling and falling edgepulse of Read Data, corresponding to these bits has been coming with required period and with specified cycles. *TSNS0~7 are all '1's while MCY is OFF. Peak pulse may only be generated if ROK=1.

(18) POINT (Pointer): 51

0	1	2	3	4	5	6	7
*DET0	*DET1	*DET2	*DET3	*DET4	*DET5	*DET6	*DET7

DET ... Detect Error Track

This is an error track pointer used in Read write operation in 6250/1600 BPI mode. All the bits are '1' while MCY is OFF. DET0~8 are set by dead track (skew, persistant track, drop out) valid pointer or ECC group buffer pointer.

(19) BLFMT (Block Format): 52

0	1	2	3	4	5	6	7
*1O2CR	*DET8	*TSNS8	*DIBG	*DNOIS	*DBOB	*DRRA	*DTM

(a) *1O2CR (No 1 or 2 track correction)

This bit is set to '0' if 1 or 2 track error correction has been executed in 6250/1600 BPI read operation. Once set to '0' this bit remains in this status till MCY is OFF. This bit is '1' while MCY is OFF.

When SCAN bit is '1', this bit represents a scan out signal of LSI chips related to read operation.

(b) *DET8 (No Detect Error Track 8)

Refer to section (18), *DET0~7.

(c) *TSNS8 (No Time Sense 8)

Refer to section (17). TSNS0~7.

(d) *DIBG (Not Detect IGB)

This bit is '1' when TSN0~8 represents IBG pattern.

(e) *DNOIS (Not Detect Noise)

This bit is '0' when TSNS0~8 represents NOIS pattern.

(f) *DBOB (Not Detect BOB)

This bit is '0' when TSNS0~8 represents BOB pattern.

(g) *DARA (Not Detect ARA)

This bit is '0' when TSNS0~8 represents ARA pattern.

(h) *DTM (Not Detect TM)

This bit is '0' when TSNS0~8 represents TM patten. It is also '0' when TM byte is detected in 800 BPI mode.

$$DIBG = \overline{0 + 1 + 2 + 3 + 4 + 5 + 6 + 7 + 8}$$

$$DNOIS = A + B$$

$$A = (0.5.8)+(2.6.7)+(1.3.4)$$

$$B = (0+5+8).(2+6+7).(1+3+4)$$

$$DBOB = A.B$$

$$DTM = \overline{(1+3+4)}\{(0.5.8)(2.6.7) + PE.R\ DS[(0.5.8)+(2.6.7)] + GCR.RDS[(2.6.7)(0+5+8)+(0.5.8)(2+6+7)]\}$$

$$DARA = \overline{(0+8+5)}\{(1.3.4)(2.6.7) + RDS[(1.3.4)(2+6+7)+(1+3+4)(2.6.7)]\}$$

0~8, TSNS0~8

(20) RDERR (Read Error): 53

0	1	2	3	4	5	6	7
*VRCE	*MLTE (*LRCE)	*SKWE	*DBCK	*DROE	PNMLT	*POSAE	"0"

(a) *VRCE (No VRC Error)

This bit is set to '0' when a Read Data Parity Error is detected and cannot be recovered by the pointer or ECC. Once this bit is set to '0' it remains in this status till MCY is turned OFF. This bit is '1' while MCY is OFF. This bit, '0', indicates an incorrectable VRC error. Error is not corrected if the above IHCOR bit has been set.

(b) *MLTE (*LRCE) (No Multiple Track Error or no LRC Error)

This bit is set to '0' under the following conditions:

a) When more than 2 DET0~8 bits are set in 6250/1600 BPI Write operation or 1600 BPI read operation.

b) When more than three DET0~8 bits are set in 6250 BPI mode Read operation.

c) When LRC error is detected in 800 BPI mode write/read operation. Once set to '0' the status of this bit remains unchanged till MCY is turned OFF. This bit is set to '1' when more than one error tracks are detected or when incorrectable LRC error is detected in 800 BPI mode.

(c) *SKWE (No Skew Error)

This bit is set to '0' when multiple skew errors are detected in read data. Once set to '0' this bit remains in this status till MCY is turned OFF. This bit is '1' only if MCY is OFF. When this bit is ON it may be assumed that skew error has not occurred.

(d) *BDCK (No Deskewing Buffer Check)

This bit is set to '0' in 6250 BPI mode Write and forward Read operations if the Deskewing Buffer read out count is not all '0's when resynchronous burst is detected. Once this bit is set to '0', it will remain in this status till MCY is turned OFF. This bit is therefore '1' when MCY is OFF. When this bit is '1' it may be assumed that skew buffer error has not occurred. This bit may not be used in 1600/800 BPI modes.

(e) *DROE (No Drop Out Error)

This bit is set to '0' when one of the TSNS0~8 signal is '0' while PHOK signal is '1' in Write operation (WRS=1). Once this bit has been set to '0' it will remain in this status till MCY is turned OFF. This bit is therefore '1' while MCY is OFF. When this bit is '1', it may be assumed that drop out error has not been detected in the 6250/1600 BPI Write Operation.

(f) PNMLT (Pointer Multiple)

This bit is set to '1' to indicate that more than two track pointers in 1600/6250 BPI mode Read/Write Operation.

(g) *POSAE (No Postamble Error)

This bit is set to '0' when illegal postamble byte (all '1's:6250, all '0's:1600) follows the postamble head (POSA=1). Once set to '0', it will remain in this status till MCY is turned OFF. It is '1' when MYC is OFF. When this bit is '1', it may be assumed that postamble error has not been detected. This bit is not available in 800 BPI mode.

(21) ZETK (NRZ Error Track): 54

0	1	2	3	4	5	6	7
ETK0	ETK1	ETK2	ETK3	ETK4	ETK5	ETK6	ETK7

This register is employed to correct errors in 800 BPI mode Read Operation. The data corresponding to the bit set to '1' is reversed for read operation. This register is also reset by HCLR signal.

(22) ZCTL (NRZ Control): 55

0	1	2	3	4	5	6	7
SFCRC	LRC	CRC	HBLKN	BLKED	CRCHG	CRCRG	R.RDB/RDB.S

(a) SFCRC (Shift CRC Register)

Set this bit to '1' to cause a shift of CRC register, and 1 CRC data pattern is processed. This bit is reset ('0') after CRC register has been shifted. This bit is '0' while MCY is OFF. In the 800 BPI mode, to set this bit cause a shift of CRC pattern register upon detecting a data byte.

(b) LRC (LRC Cycle)

This bit is set to '1' in FWD operation after CRC byte has read. If a CRC byte has not been detected, this bit will be set to '1' after a period equivalent to 5.3 bit cells from the last data byte. Once set, the status of this bit remains unchanged till ROK is turned OFF.

In BWD operation this bit is set to '1' as ROK rises and is reset to '0' upon the detection of the first data byte (LRC byte). This bit is '0' while ROK is OFF.

This bit indicate that the current data byte is a LRC byte. This bit is valid only in 800 BPI mode.

(c) CRC (CRC Cycle)

In FWD processing this bit is set to '1', if data bytes are not detected in the length of 2 bit cells after the last data byte. This bit remains in this status till 3.3 bit cells or till the detection of a LRC byte. In BWD operation this bit is set to '1' upon detection of LRC byte. (first byte) This bit remains '1' till the detection of data byte. If data byte can't be detected within 5.3 bit cell from LRC byte, this bit will reset to '0'. This bit is '0' while ROK is off. This bit indicate that the byte detected is a CRC byte. It is valid only in 800 BPI mode.

(d) HBLKN (NRZ Block)

This bit is set to '1' upon detection of 1 Byte when WRS=1 and upon detection of 8 bytes (including CRC and LRC bytes) when WRS=0. The byte remains in this status till MCY is turned OFF. This bit is therefore '0' while MCY is OFF. This bit represents detecting of an 800 BPI block.

(e) BLKED (NRZ Block End)

This bit is turned ON ('1') to indicate that data or check byte was not detected during 10.7 bit cell period in 800 BPI mode processing. Once turned ON, the status of this bit remains unchanged till R. RBD is set to '1' or MCY is turned OFF. This bit is therefore '0' while MCY is 'OFF'.

(f) CRCHG (CRC Horizon Gap)

In a 800 BPI mode read operation, this bit is turned ON ('1') when a data byte is not detected for a period of 5.3 bit cells after the last data byte. This bit, '1', indicate that a gap exceeding the permissible recording gap for CRC byte has been detected. Therefore a CRC byte is either not present or CRC byte is all '0's when this bit is '1'. This bit is reset by turning ON R.RDB bit ('1') or by turning OFF MCY bit.

(g) CRCRG (CRC Recording Gap)

This bit is turned ON to indicate that a recording gap longer than 2 bit cells has been detected. CRC byte should be detected after this bit has been turned ON and before the CRC HG is set.

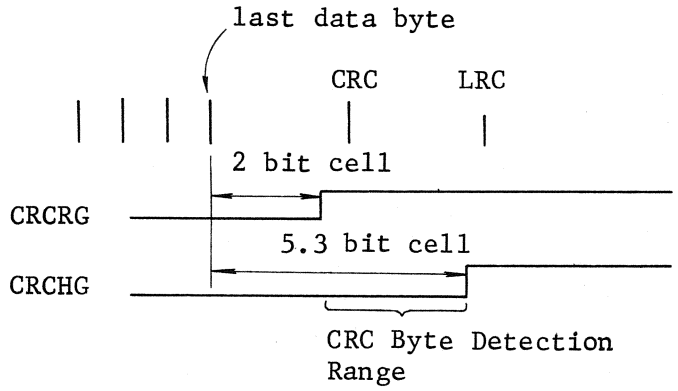


Figure 4.18

This bit is reset under the same conditions as that of CRCHG bit.

(h) R.RDB/RDB.S (Reset Read-Data-Byte/Read-Data-Byte Set)

In 800 BPI mode, this bit is set to '1' by the sampling pulse. Once set, this bit may not be reset till turning R.RDB bit ON or till MCY is turned OFF. This bit is therefore '0' while MCY is OFF. Set RDB.S bit to '1' to reset RDB.S to '0'. Then CHCHG, CHCRG and BLKCD bits are also reset to '0'. This bit may be used for counting read data byte in 800 BPI mode.

(23) ZMRG (NRZ Marginal Code): 56

0	1	2	3	4	5	6	7
$\overline{\text{*NVRCE}}$	ETK8	$\overline{\text{*NSKWE}}$	SDNT / $\overline{\text{*LRCE}}$	TM0	TM1	TM2	TM3

(a) *NVRCE (No NRZ-VRC-Error)

This bit indicate that VRC error has not been detected in the 800 BPI Read Operation. This bit is set to '0' as soon as a VRC error has detected. This bit may be reset to '0' by SDRST bit. This bit is also '1' while MCY is OFF.

(b) ETK8 (NRZ Error Track 8)

Comforms with ETK bits 0~7 in section (21).

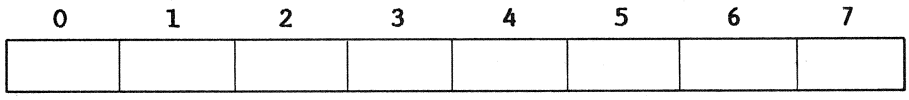
(c) *NSKWE (No NRZ Skew Error)

In 800 BPI write operation, this bit is set to '0' when multiple skew errors are detected in the data read from the Read Head. This bit is not reset to '1' till the SDRST bit is turned ON or MCY bit is turned OFF.

(d) SDRST/*LRCE (Sense Data Reset/Not LRC Error)

This bit with '0' indicate that a parity error has been detected in LRC byte (LRC error). *LRCE bit is reset ('1') when MCY is turned OFF. Setting this bit to '1' by up (SDRST='1'), the above *NSKWE, *NWRCE bits will be reset to '1'.

(24) ZOP (NRZ OPTION): 57



This register indicates whether the 800 BPI optional PCA (1A01: 512189) has been mounted. One of the bits in this register is '1' when the above optional board is mounted. If all the bits in this register are '0', the registers 54~56 are not available.

(25) TCADA (MTC Address CH-A): 58

0	1	2	3	4	5	6	7
/CADA0	/CADA1	/CADA2	/CADA3	/CADA4	/SBMC	/CPBL	/NOFS
				(CM0)	(CM1)	(CM2)	(CM3)

(a) CADA0~CADA4 (MTC Address CH-A 0~4)

These are the MTC address set by shoot plug for CH-A side.

(b) When the CMROM bit (see (32), 5) is '1', bits 4~7 represent CM0~3.

CM0~3 is obtained by converting the 8 bit code from CHBI register into a four bit code. When CMROM bit is '0', bits 4~7 represent CADA4 and following CH interface control bit.

SBMC; '1' when special MBC interface.
CPBL; '1' when IBM compatible mode.
NOFS; '1' when normal interlock handshake (not offset interlock)

(26) OUTAG (Out Tag Sense): 59

0	1	2	3	4	5	6	7
/ADO	/CMO	/SVO	/SLIG	/OPOA	/RQSPE	/OIS	/INS

(a) ADO (Address Out)

This is the address out signal from the channel interface to which MTC is logically connected. If MTC is not connected either to CH-A or CH-B or if CE panel ONL/OFL switch is set to OFL side, this bit is '0'.

If this bit is '1' and if the CMROM bit is '0', the CHBO register represents the I/O address specified by the channel.

(b) CMO (Command Out)

This is a CMO signal from the CH-B or CH-A side. If MTC does not logically connect to any CH interface or if the CE panel ONL/OFL switch is set to OFL side, this bit is '0'. If this bit is '1', the above mentioned CHBO register, when CMROM=0, indicates the command code specified by channel.

(c) SVO (Service Out)

This is the SVO signal from channel interface. This bit is '0' if none of the channels is logically connected to MTC. This signal is the same to the SVI signal when the CE panel ONL/OFL switch is set to OFL side. When this bit is '1', it indicates that either the linked channel has received the Bus-In data or that the data requested by SVI is present on Bus-Out.

(d) SLIG (Select in Gate)

This signal is '1' if MTC is selected by the channel. It is '0' when the select out signal is released. This bit is turned ON to indicate that MTC has been selected. The SLO signal gates the passing signals to the control device. This bit is '0' if none of the channels is linked or if the CE panel switch set to OFL. This bit is reset by the SERT signal.

(e) OPOA (Operational OUT CH-A)

This is the OPO signal from the channel interface A side (basic side) channel.

(f) RQSPE (Request-In Suppress Enable)

Set this bit to '1' so that the channel interface RQI signal may be suppressed by the SPO signal. RQI signal to CH interface will be generated only when this bit is OFF, RQIAF (RQIBF) is set to '1' and SPOA (SPOB) is not ON. This signal is reset by the SERT signal.

(g) QIS (Request-in Initial Selection)

This bit is '1' when the initial selection sequence is started with the linked channel as a response to a Request-In. Upon set of OPI bit this bit is reset to '0'. This bit is not '1' when MTC is not linked to any channel or when CE panel ONL/OFL switch is set to 'OFL'.

(h) INS (Initial Selection)

This bit is '1' when the initial selection sequence (ADO=1, select-out ON) is started in the selected channel. When the channel has linked in this sequence (OPI=1) this bit is '0'. An interruption may be created when this bit is turned ON. This bit is not set to '1' when the CE panel ONL/OFL switch is set to OFL side.

(27) CHBO (Channel Bus Out): 5A

0	1	2	3	4	5	6	7
CBO0	CBO1	CBO2	CBO3	CBO4	CBO5	CBO6	CBO7
(RCT0)	(RCT1)	(RCT2)	(RCT3)	(RCT4)	(RCT5)	(RCT6)	(RCT7)

These are interface Bus Out signals from the connected channel. This register is set to all '1' when both CH-A and CH-B are not connected or the CE panel ONL/OFL switch is set to OFL. Moreover these bits are all '1's when the SERT signal is '1'. CBO0~7 data is available in preset of the outbound tag (ADO, CMO, SVO, DTO) and represent I/O device address, command code, write data etc.

This register represents position check FTP counter status (RCT0~7) when CMROM (described later) is '1'.

(28) IFSTA (Interface Status of CH-A): 5B

0	1	2	3	4	5	6	7
CUBSA	SPOA	SERA	SYRA	IFONA	ETA	URTO / RTB	URTO2 / URRT

(a) CUBSA (CUB-Send Memory of CH-A)

This bit is '1' when a Short Busy Sequence CUB status is sent to Bus-In and STI is raised) is sent to Channel A. This bit indicates CUB status has been sent or is being sent on CH-A side. This bit is reset when STI signal is generated while CH-A side is linked (RTA=1, OPIA=1) to MTC. This bit is also reset when the power supply is turned ON or when the CH-A side system reset is executed. (SYRT)

(b) SPOA (Suppress Out of CH-A)

This is SPO signal of CH-A side interface. This bit is '0' when CH-A is in DISABLE of the MTC operator panel.

(c) SERA (Selective Reset of CH-A)

This bit is set to '1' when Selective Reset is received from CH-A side while MTC is linked to CH-A. Once set to '1' the status of this bit remains unchanged till a System Reset is received from CH-A or the R-RSTA (described later) bit is set to '1' (Normally UP count mode sets R.RSTA to '1' upon completion of Selective Reset operation). UP count mode is restarted from address '000' once this bit is turned ON.

(d) SYRA (System Reset of CH-A)

This bit is set to '1' when a system reset is received from CH-A. Once this bit is set to '1' it will not be reset till the R.RSTA (described later) bit is set to '0'. If MTC has linked to CM-B upon receiving System-Reset from CH-A, SYRA bit will not be set till MTC has been released. When this bit is set to '1', UP count mode is restarted from address '000'.

(e) IFONA (Interface ON of CH-A)

This bit is '1' when the CH-A side interface switch of MTC operator panel is in Enable. The driver/receiver circuits on the CH-A side interface is not active when this bit is '0'. Moreover this bit will also be set to '0' if CE panel ONL/OFL switch is set to OFL side. This bit is turned OFF ('0') upon completion of the operation being executed if the interface switch is changed to DISABLE.

(f) RTA (Root A), RTB (Root B)

MTC may have two channel interfaces. Here RTA, RTB signals are used to indicate the logical interface status of the Channel interface and MTC. Now RTA signal is '1' if MTC is linked to A side channel, while RTB is '1' if MTC is linked to B side channel. Both RTA and RTB signals are '0' when MTC is in neutral status, that is not linked to any interface. Now RTA and RTB signals are reset to '0' by the SYRT signal.

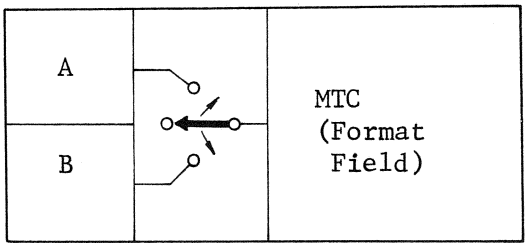


Figure 4.19 2 Channel Switch Concept

(h) URTO1, URTO2 (Unconditional Reset Out)

When both WRTO1 and URTO2 bits are set to '1', UR reset request is generated for another MTC. At this stage the URRT bit is set to '1'. This bit can not be set to '1' while MCY is OFF.

(i) URRT (Unconditional Reset)

This bit, '1', indicates that there is a UR reset request from another MTC or from its own MTC (URTO 1/2 are set to '1' for this purpose).

(29) INTAG (Channel-In Tag): 5C

0	1	2	3	4	5	6	7
OPI	M.ADI	M.SVI	M.STI	RQIAF	RQIBF	DSI	DCN

(a) OPI (Operation-IN)

It is employed as OPI signal for the linked channel. When this bit is set to '1', MTC and channel will be linked. This bit may be reset directly or is reset if Select Out is released and if EBOP bit is '1' (this bit is described later). This bit may also be reset by the SERT signal and disconnect request (DCN=1).

(b) M.ADI (Microprogram Address-IN)

This is an ADI signal for the channel. This bit may be set to '1' only if OPI bit is also '1'. In this case I/O device address must be stored in CHBO register. This bit may be reset ('0') by UP count mode. It may also be reset by the SERT signal and disconnect request (DCN=1).

(c) M.STI (Microprogram Status-IN)

This is an STI signal for the channel. This bit ('1') resets the CUBSA, CUBSB bits described earlier. This bit may also be reset by the SERT signal or by a disconnect request.

(d) M.SVI (Microprogram Service-IN)

This is an SVI signal for the channel. As SVI signal for data transfer is generated in the internal circuit, this bit has to be reset to '0' in such cases (when DTF0, DTF1 bits are '1'). This bit may be reset by the SERT signal or by a disconnect request.

(e) RQIAF (RQI Flag for CH-A)

RQI signal is caused to the channel interface when this bit is 1. This signal is however suppressed by the SPO signal on CH-A side when RQSPE bit is '1'. This bit is reset by the SERT signal or a disconnect request.

(f) RQIBF (RQI flag for CH-B)

This is a RQI signal for CH-B side. For further details refer to RQI AF.

(g) DSI (Discount IN)

Disconnect-IN signal for channel interface is caused when this bit is set to '1'. This bit may be set by UP count mode or by PERR (processor error) signals. This bit should be reset by UP count mode in the selective reset routing initiated by SERT signal.

(h) DCN (Disconnect)

This bit is set to '1' when a disconnect sequence occuered. Bits M.ADI, M.SVI, M.STV, RQIAF and RQIBF are '0' when this bit is '1'. Set this bit to '0' to clear DCN bit. This bit is also reset by the SERT signal.

(30) CHBI (Channel Bus-In): 5D

0	1	2	3	4	5	6	7
CBI0	CBI1	CBI2	CBI3	CBI4	CBI5	CBI6	CBI7
(A)	(*B)	(SDI)					

This is a register to send Bus-In signals for the channel. I/O address (with M.ADI bit), status byte (with M.STI bit), sense data (with M.SVI bit), etc. may be stored in this register. This register is cleared by SERT signal. CBI0-2 are assigned to Scan Clock A, Scan Clock B and the Scan Data when the SCAN bit is set to '1'.

(31) IFCTL (Interface Control): 5E

0	1	2	3	4	5	6	7
R.RSTA / OVRN2	S.BCT / *XTAG	SHBC / DXFE	S.UCT / DXRQ	S.DCT / BIBSY	CTSTP / *ABRPC	R.RCT / *BOPC	R.CRY / C.RCT

(a) R.RSTA (Reset RSTA)/OVRN2 (over-run 2)

Setting this bit to '1', the above mentioned signals SERA, SYRA are reset ('0'). They should be reset upon completion of selective reset or system reset operation. The OVRN2 signal is turned ON if overrun is detected in data transfer in offset interlock mode (refer to section 4.7.2).

(b) S.BCT (Set Byte Counter)/*XTAG (No Transfer Tag)

Setting this bit to '1', content of the CHBI register is preset in the upper 8 bits of the 12 bit byte counter. Now '1' is entered in the lower 4 bits. If SHBC is '0', the CHI7 bit correspond to 2^4LSB. If SHBC is '1' (described later), the CBI7 bit corresponds to 2^0 LSB. In the case the byte counter becomes an 8 bit counter and is capable of counting upto 255 bytes.

This function may be employed only if MTC is in offline status. *XTAG '1' indicates that in-tag and out-tag signal for data transfer to and from the channel have not been generated. Those signals are SVI signal (service in), DTI (data in) signal and SVO (service out), DTO (data out) signals respectively.

(c) SHBC/DXFE (Short Byte Counter/Data Transfer End)

SHBC is employed to make the byte counter act as 8 bit counter.

DXFE signal is provided to indicate any data transfer with format circuit has finished. This signal is set to '1' by 'SIOP' (CMO=1), DISCONNECT from CH linked to the MTC or by the carry from the above byte counter (in case of MTC offline). DXFE is '0' when MCY is turned OFF.

(d) S.UCT/DXRQ (Start Up Count/Data XFR Request)

Setting this bit to '1', the Position Check FTP counter starts counting FTP in UP count mode.

DXRQ is a data transfer request signal from the formatter circuit. Now DXRQ=1 indicates that SFR buffer is not full (when DTFO=1) or data is still left in SFR buffer (when DTF1=1).

If both DTFO and DTFI are '0', DXRQ is '0'. It may also be '0' if IHDRQ bit is '1'.

(e) S.DCT/BIBSY (Start Down Count/Bus In Busy)

Setting this bit to '1', the Position Check FTP counter start counting FTP in Down Count Mode.

BIBSY is '1' if the data stored in CHBI register does not move to XFR buffer data from up to the XFR buffer is stored (Via CHBI Register). MP should confirm that BIBSY=0 before setting the next data in CHBI register.

(f) CTSTP/*ABRPC (Counter Stop/No A,B Register Parity Check)

The Position Check FTP counter is stopped when CTSTP is set to '1'. *ABRPC is set to '0' if a parity check has detected in A and B registers during data transfer from MTC to the channel. Once set to '0' it remains in this status till MCY is turned OFF. This bit, '1', indicate that parity error was not detected in A or B registers during data transfer from MTC to CH.

(g) R.RCT/*BOPC (Reset Reposition Counter/No Bus Out Parity Check)

R.RCT is set to '1' to clear position check FTP counter to all '0's. *BOPC is '0' if a Bus Out parity error has detected in data transfer from the channel.

Once set to '0', *BOPC remains in this status until MCY is turned OFF. While MCY is OFF, this bit is '0' if there is a parity error in the Bus-Out data and is 1 if no parity error is found in the Bus Out data.

While MCY is ON, *BOPC = '0' indicates that no Bus Out Parity error has detected during data transfer. While MCY is OFF, it indicates that there is no parity error in the present Bus Out data.

(h) R.CRY/C.RCT (Reset Carry/Carry of Reposition Counter)

R.CRY is set to '1' to reset overflow of the position check FTP counter.

C.RCT is changed to '1' upon detection of carry in the above mentioned counter. It remains in this state till MCY is turned OFF or R.CRY is set. C.RCT is therefore '0' while MCY is OFF.

(32) XFCTL (Transfer Control): 5F

0	1	2	3	4	5	6	7
DXFI	DXFO	MPFD	SCAN	EBOPI	CMROM	ROM2	ROM1

(a) DXFI (Data Transfer In)

Set this bit to '1' for data transfer from MTC to a channel. This sets the data transfer circuit to enable in the required direction. This bit is reset by SERT signal.

(b) DXFO (Data Transfer Out)

Set this bit to '1' to enable data transfer from the channel to MTC. This sets the data transfer circuit to enable in the required direction. This bit is reset by SERT signal.

(c) MPRD (Microprogram Read)

Set this bit to '1' to store MP data to XFR buffer. This bit is reset by SERT signal.

(d) SCAN (Scan Mode)

Setting this bit to '1', all the LSI FFS in the formatter circuit are in serial scan mode. Scan operation is countrolled by CBIO~2 bits described earlier. SCAN function is used with diagnose operations. This bit is reset by SERT signal.

(e) EBOPI (Enable OPI - OFF)

Setting this bit to '1', the OPI signal is immediately reset when 'Select Out' from the channel linked with MTC is released.

If this bit is '0', the OPI signal will remain unchanged even if the above 'Select Out' is released.

(f) CMROM (Command ROM Select)

When this bit is '1', converted command code (CM0~3) is represented in bits 4~7 of the above mentioned TCADA resister (58).

Moreover CHBO register (5A), bits CBOO-7, is represented position check counter output RCTO-7. This bit is reset by SERT signal.

(g) ROM2, ROM1

This bit is used to specify, the conversion table (ROM) for converting a content of the CHBI register (CBI0-7) into CM0-3 code. This bit is reset by SERT signal.

(33) TRAP (Trap Control): 60

0	1	2	3	4	5	6	7
T.INT	T.TMR	T.INS	T.PER	M.INT	M.TMR	M.INS	TMSK

(a) T.INT (Trap by Device Interruption)

This is a DVINT signal from the selected MTU.

(b) T.TMR (Trap by Timer Carry)

This bit represents MTC timer overlfow. Timer stops counting while this bit is ON.

(c) T.INS (Trap by Initial Selection)

This bit is set to '1' when MTC is in ONL status and the channel linked to MTC is requesting an initial selection sequence. (When both address out and select out have been specified simultaneously).

This bit is reset when address out and select out are released or the OPI bit has been set to '1'. This bit is set to 1 for a period of clock when PSSS switch is operated under the following condition:

a) MTC is set to OFL
b) PSSS switch is in data input mode.

(d) T.PER (Trap by Processor Error)

This bit is set to '1' when the PERR signal has become '1' (excluding the case in which MTC is in ROSF mode (ROS function).

(e) M.INT (Device Trap Mask)

Set this bit '1' to enable a device trap. Device trap can occur when the above T.INT='1' and M.INT='1'. This bit is reset by SERT signal.

(f) M.TMR (Timer Trap Mask)

This bit is set to '1' to enable timer overflow trap. This trap can occur when the above T.TMR='1' and M.TMR='1'. This bit is reset by the SERT signal.

(g) M.INS (INS Trap Mask)

This bit is set to '1' to enable an INS trap. This trap can occur when the above T.INS is '1', and M.INS=1. This bit is reset by SERT signal.

(h) TMSK (Trap Mask)

This bit, '1', enables all the microprocessor traps. As soon as a trap is accepted, TMSK signal is reset ('0'). Set TMSK to '1' to enable trap after trap reason has been recognized.

(34) MPERR (Microprocessor Error): 61

0	1	2	3	4	5	6	7
M.RER / RENB	R.PER / OFL	CSPE	REGE	MEC0	MEC1	MEC2	MEC3

(a) M.RER (Mask Register Error)/RENB (Register Enable)

The RENB bit is reset ('0') by the reset signal when power supply is turned ON. Parity check is invalid before microprocessor intializes LSR.

MP should initialize all LSRs when power on. After this, set M.RER bit to '1' to validate the above parity check. Once set, RENB is '1', and may not be reset unless power supply is turned off (MP cannot reset RENB).

(b) R.PER (Reset Processor Error)/OFL (Offline)

Setting R.PER bit to '1,' the PERR signal is reset Simultaneously. ALU carry register is also cleared. PERR is caused by CS parity error or LSR read parity error, and also reset by the SERT signal. OFL signal is '1' when the CE panel ONL/OFL switch is set to OFL.

(c) CSPE (CS Parity Error)

This bit indicates a parity error has taken place in CS read. PERR is generated if this bit is '1'. This bit is reset either by the SERT signal or above mentioned R.PER bit CS: control storage where MP is stored.

(d) REGE (Register Error)

This bit represents a parity error detected when MP makes an access to LSR data (after the above M.RER bit has been set to '1'). This generates PERR interruption. The reset condition of this bit is the same as that of CSPE.

(e) MEC0~3

This is the EC level set in MTC.

(35) VFSNS (VFO Sense): 62

0	1	2	3	4	5	6	7
/SINH	/SP2	/F.C=S	/M	/SM7	/VFOH	/VFOM	/VFOL

(a) SINH (Start Inhibit)

This bit is '1' when SINH function in CE panel MP control is selected from CE panel.

(b) SP2 (Spare 2)

This bit is '1' when SP2 function in MP Control is selected from CE panel.

(c) F.C=S

'1' when address compare is successful.

(d) M

Normally this bit is '0'.

(e) SW7

This bit is '1' when the CE panel switch 7 is ON.

(f) VFOH/VFOM/VFOL

These three bits select the VFO processing mode.

Table 4.25

VFOH	VFOM	VFOL	Available Speed Mode			
			200	125	75	50
0	0	0				0
0	0	1			0	0
0	1	0		0		0
0	1	1		0	0	
1	0	0	0			0
1	0	1	0		0	
1	1	0	0	0		
1	1	1	-	-	-	-

0 ... available

(36) FID (MTC Function ID): 63

0	1	2	3	4	5	6	7
/FID0	/FID1	/FID2	/FID3	/FID4	/FID5	/FID6	/FID7

This register indicates the function selected for MTC.

FID0 : Normally set to '0'.

FID1 : '1' when No IB-Retry.
Specifies the retry function in case of IB write error.

FID2 : '1' when No Gap Length Addition.
If this bit is '0', the IBG length is increased by 0.03 inch in GCR write processing.

FID3 : '1' when IBM mode NRZ.
When this bit is '1' along with CPBL bit, data block which comprises less than 6 bytes of data is allowable in NRZ Read/write operation.

When this bit is '0', such a data block will be processed as noise.

FID4-7: Reserved.

(37) TCADB (MTC Address for CH-B): 64

0	1	2	3	4	5	6	7
/CADB0	/CADB1	/CADB2	/CADB3	/CADB4	/(SP7)	/(SP8)	/SHARB

This register specifies the MTC address for CH-B. All other explanations are the same as in section (25) on TCADA. This register is set to all '0's unless the optional 2-CH SW is mounted.

SP7, SP8 and SHARB represent setting unit output.

(38) IFSTB (Interface Status for CH-B): 65

0	1	2	3	4	5	6	7
/CUBSB	/SPOB	/SERB	/SYRB	/IFONB	/OPOB	/"0"	/2CHSW

(a) CUBSB (CUB Send Memory for CH-B)

(b) SPOB (Supress Out in CH-B)

(c) SERB (Selective Reset in CH-B)

(d) SYRB (System Reset in CH-B)

(e) IFONB (Interface On in CH-B)

(f) OPOB (Operational-out in CH-B)

These are provided for CH-B. All other explanations are the same as that for CH-A (item 28).

(g) 2CHSW (2-CH Switch)

This bit is '1' when the 2-CH SW option is equipped. Registers with addresses 64~70 are valid only if this bit is '1'.

(39) RTSNS (Root Control Sense): 66

0	1	2	3	4	5	6	7
/INHA	/INHB	/*BUSE	/BFRE	/RQIB	/"0"	/SINHB	/GINHA

These signals are provided for channel interface switching. Refer to Subsection 4.6.6.

(40) RTCTL (Root Control): 67

0	1	2	3	4	5	6	7
DSOKA	DSOKB	CRVA	CRVB	S.SW / SW	R.USE / *USE	R.RSTB /	

(a) DSOKA (Disable OK for CH-A)

This bit '1' is necessary to disable channel A. The IFONA signal may only be reset to '0' if this bit is ON. Therefore MP should set DSOKA only if there is no communication between CH-A and MTC, there is no pending status, when CH-A disable request is received from the operator panel.

(b) DSOKB (Disable OK for CH-B)

Disables CH-B. Other points are the same as DSOKA.

(c) CRVA (Channel Reserve A)

If this bit is set to '1', CH-B response is always 'CUB' status for initial selection. This prevents MTC from being linked to CH-B. This bit is reset by SYRT signal (SYRA) from CH-A.

(d) CRVB (Channel Reserve B)

When this bit is set to '1', CUB status is replied in response from CH-A for initial selection. This prevents MTC from being connected to CH-A side. This bit is reset by the SYRT signal (SYRB) from CH-B.

(e) S.SW (Set Switch)/SW (Switch enable)

Setting S.SW bit to '1', SW signal is changed to '1'. Short busy sequence will not be able to initiate upon receiving an Initial Selection from opposite channel interface, if SW=1 and MTC is linked with current channel interface. None of status being posted to another channel, this channel keeps waiting for completion of current channel working. As soon as MTC has been free with current, MTC links another channel again. Normally, MP should set SW bit when posting CUE status.

SW signal is reset to '0' when initial selection sequence has been initiated with another channel interface.

(f) R-USE (Reset Use)/*USE (No Use)

Setting this bit to '1' when CH-A or CH-B is linked to MTC, the interface is released and MTC becomes free. *USE is therefore normally '0' when either CH-A or CH-B is linked to MTC. This bit is '1' if MTC is not linked to any channel.

(g) R.RSTB (Reset RSTB)

Signals SERB and SYRB are released when this bit is set to '1'. Refer to R.RSTA (31)-(a).

(41) Register Address from 68 to 6F ..... not used.

4.6 Channel Interface Control

4.6.1 Selection

Channel selects MTC by activating Select Out, Select In or Hold Out Channel Interface signal lines. Select Out and Select In are constructed in loop mode. MTC therefore receives one of the these selection signals. This selection is done by priority selection circuit in the MTC Interface Unit (DGCM). For the purpose of explanation it is assumed here that the selection circuit is connected to Select Out. Channel Interface Control Circuit is shown in Figure 4.20. This figure shows the Channel A side. Channel B circuit (2CH-SW option is additional) is the same as that on channel A side. Hereinafter the explanation will be with reference to channel A side.

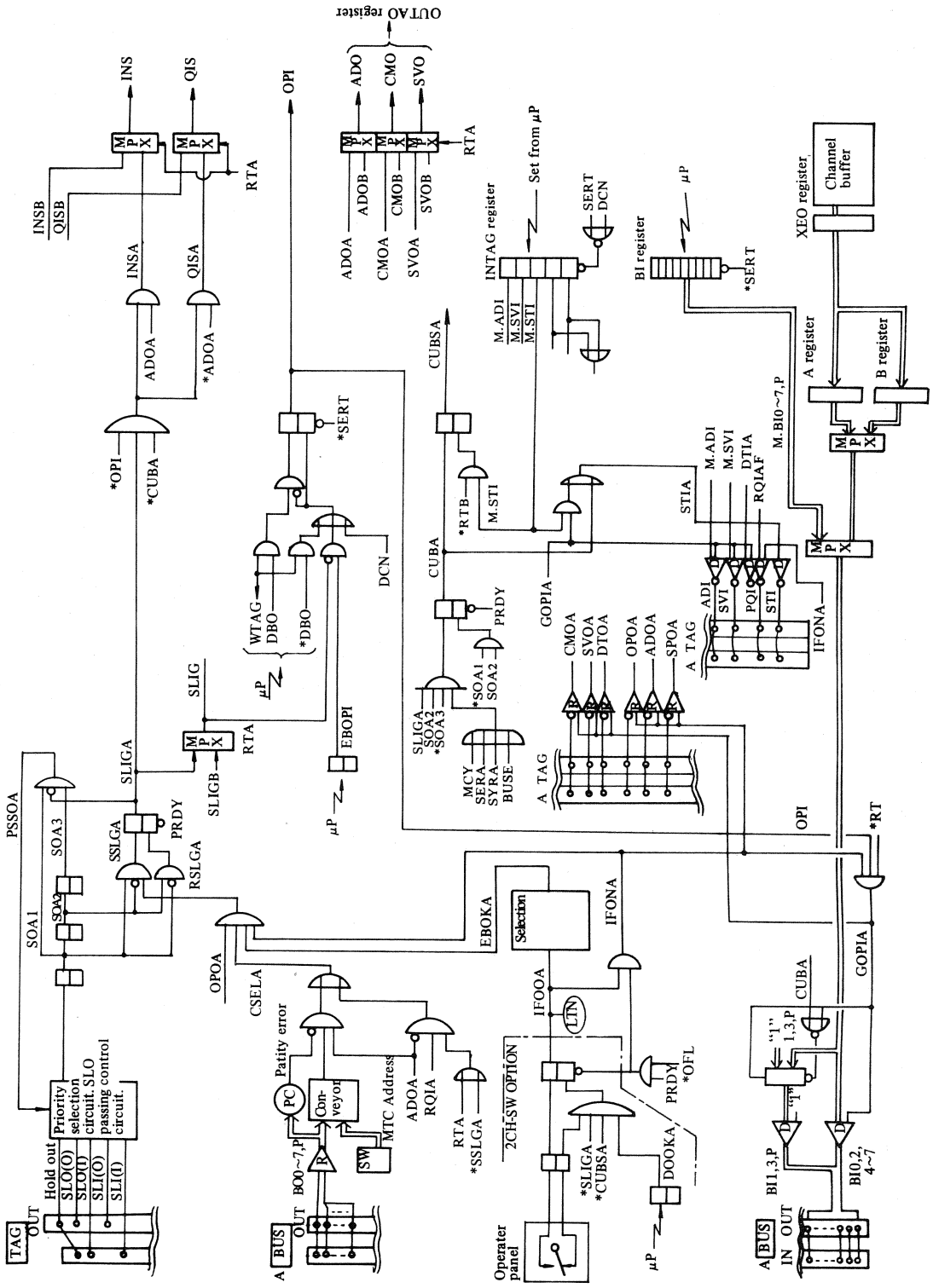


Figure 4.20 Channel Interface circuit diagram

SOA 1, 2, 3 (Selection Out 1, 2, 3) timing signals are generated by INSOA (Initial Select Out A) signal which is itself set by the AND obtained from Select Out and Hold-out signals. (For further details refer to Figure 4.41). Along with ADOA (Address Out A) signal the I/O Address sent out to the BO0~7P (Bus Out 0~7), including the MTC address, are compared at the SOA1 signal rise timing. If the controller address matches, SLIGA signal is set. The SLIGA signal suppresses the PSSOA (Pass Select Out A) and also suppresses the transmission of Select Out Signal to the next control unit. If the control address does not match, the PSSOA signal is generated at the SOA3 signal rise timing and the Select Out Signal is passed to the next control unit. In addition to matching controller address, it is necessary to set OPOA signal (operational out A) from the Channel in order to suppress transmission of Select Out signal after selecting MTC.

IFONA signal indicates that MTC is connected logically to the channel interface. If 2CH-SW option is provided it is reset under one of these two conditions.

(1) Operator panel Interface switch is set to OFF.

(2) The CE panel ONL/OFL switch is set to OFL. (when equipped)

EBOKA signal controls the Select Out signal transmission. MTC is thus selected and SLIGA signal gives rise to INSA (Initial Selection A) signal for initial selection sequence.

This TNSA signal is multiplexed with the INSB signal which represents the beginning of initial selection sequence from the B-interface circuit. When MTC is linked to A-side (RTA signal='1'), INSA generates INS and interrupt to the microprogram.

In the MTC polling sequence, QISA signal is set instead of INSA signal and therefore QIS signal is generated instead of the INS signal. The QIS signal does not generate interruption in the microprogram.

4.6.2 Interface sequence

When the microprogram detects an interruption from INS signal, it sets the OPI bit and activates the selection sequence. The OPI signal enables the intag signal transmission driver for Bus-In 0~7P, Address-In, Status-In etc. and outtag signal receivers for command out, service out signals etc. The Intag signals can be sensed in corresponding INTAG register bits. Ontag signals are multiplexed with the B side interface Outtag signal. At this stage, if RTA signal is ON ('1'), the Outtag signal from A-Side is detected by the microprogram as the Outtag Register Bit. Sensing these INTAG register bits and controlling OUTAG register bits, microprogram proceeds the interface sequence with the channel. Timing chart of this process is shown in Figures 4.21 and 4.22.

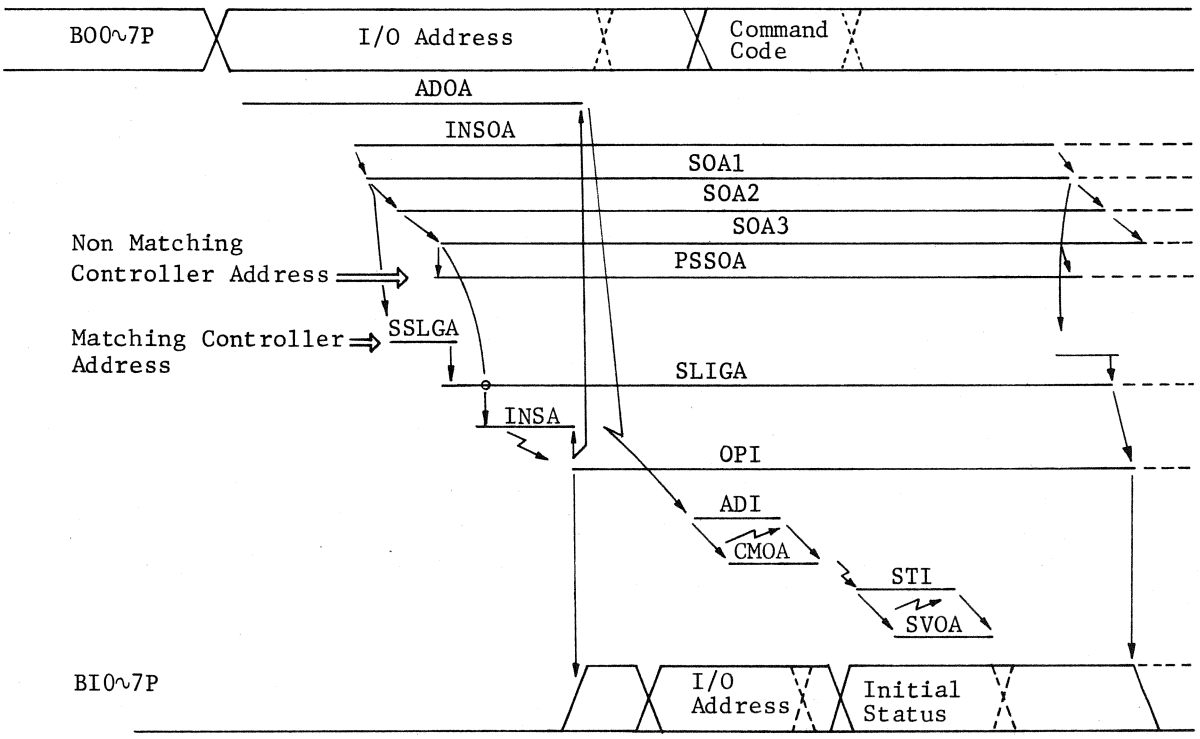


Figure 4.21 Initial selection sequence

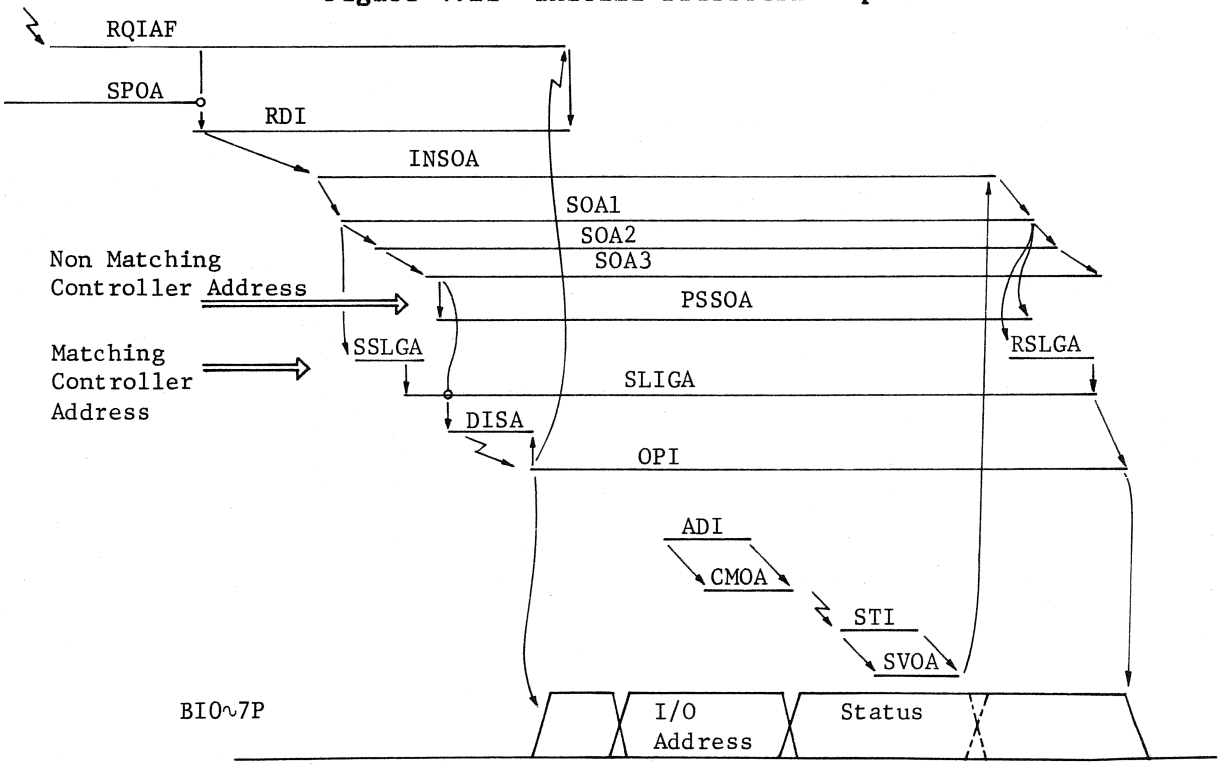


Figure 4.22 MTC polling sequence

4.6.3 Short busy sequence

If the MTC selected by the channel is in the following status, CUB status response is generated in the short busy sequence.

(1) Executing a command operation (MCY='1').

(2) While executing a system reset or selective reset operation.

(3) When 2CH-SW option is equipped and the channel switch is logically linked to the channel interface on the opposite side making the channel interface on this side unusable.

If CUB status response is received in short busy sequence, CUBSA (CUB Status Send Memory A) or CUBSB (CUB Status Send Memory B) signals are set. The signals remain set till the following CUE status. (CUE bit must be included in the first status following the CUB status). The short busy sequence circuit is shown in Figure 4.20. Short busy sequence timing is shown in Figure 4.23.

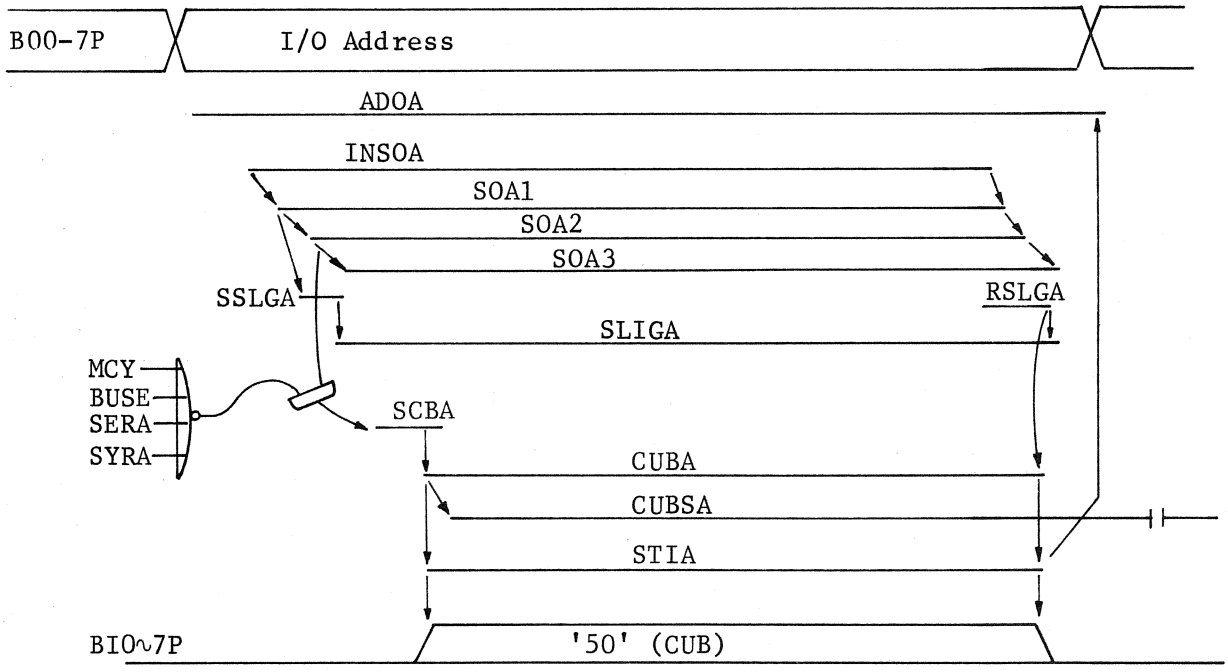


Figure 4.23 Short busy sequence

4.6.4 Interface disconnect

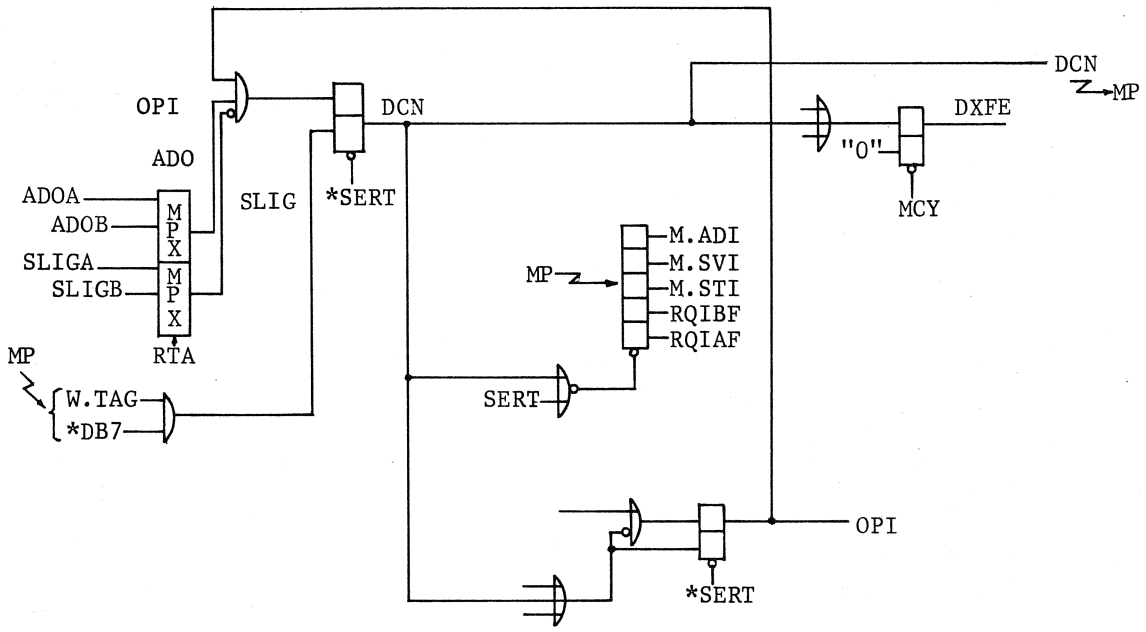


Figure 4.24 Interface disconnect circuit

Interface Disconnect request from the channel is activated when address out is true and select out is false. At this stage, MTC sets the DCN signal (disconnect) as shown in Figure 4.24. The DCN signal sets DXFE (data transfer end) signal, interface register and OPI signals.

4.6.5 Disconnect-In

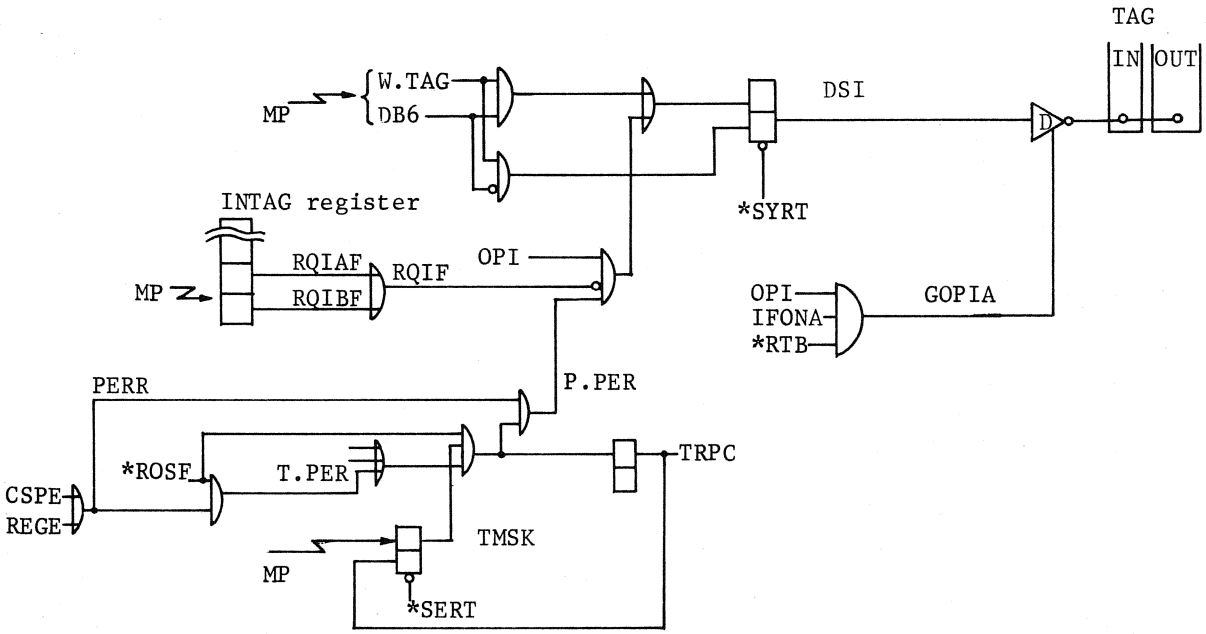


Figure 4.25 DSI signal set/reset circuit

If CSPE (CS Parity Error) and REGE (Register Parity Error) are detected while a channel and MTC are being linked (OPI signal='1'), the PERR (Process Error) signal will be generated. As soon as this PERR signal is generated, DSI signal is set in the microprocessor trap cycle, a Disconnect-In signal is sent to the Channel and error alarm is activated.

If the above signals are detected during operations other than linking or if errors other than PERR error are detected during interface operation, the microprogram sets DSI signal. The DSI signal is reset only by system reset or by the microprogram.

4.6.6 Route control

The route control circuit is provided for logically and dynamically switching between MTC formatter and channel interface circuits. This is only feasible when the two channel switch option has been equipped.

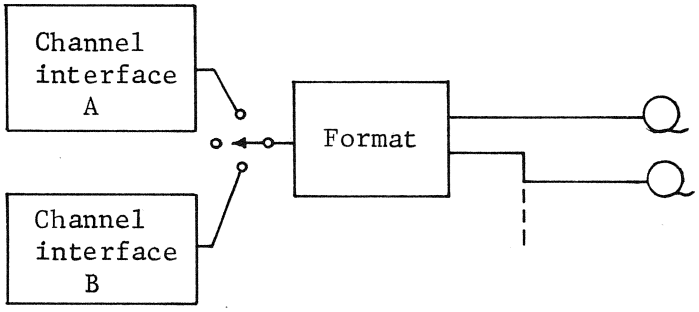


Figure 4.26 Route control

This circuit is placed in the two channel switch option. If this option is not provided, the channel interface switch is permanently set to A-side.

Route control circuit is shown in Figure 4.27. The two channel switch status is identified by RTA (Route A), RTB (Route B) and USE (Use A or B) signals. USE signal indicates the channel interface route has been set and reserved. In neutral status, USE signal is in reset status. If the USE signal is set from either side (SSLGA/B signal and INSA/B signals), the RTA or RTB signal is also set simultaneously. Thus the formatter section and the channel interface section are linked logically and command operation is executed. The microprogram sets RUSE bit if the Route need not be held in its present status upon completion of command operation.

If a subsequent selection request is not received from the channel, the USE signal is reset and the switch is reset to neutral. SW bit is set to suppress CUB status response, if the other channel selection request is received during an MTC start sequence for establishing a channel interface to send CUE status. If the SW bit has been set by the microprogram prior to CUE send sequence, INHB (Inhibit B) or INHA (Inhibit A) signals are set at the time of starting selection for interrupt polling. Now, INHA or INHB signals suppress SSCUB or BUSE signals respectively, and gate CUB status, thus stopping the progress of short busy sequence. The SW bit is reset, when the CUE sequence is completed.

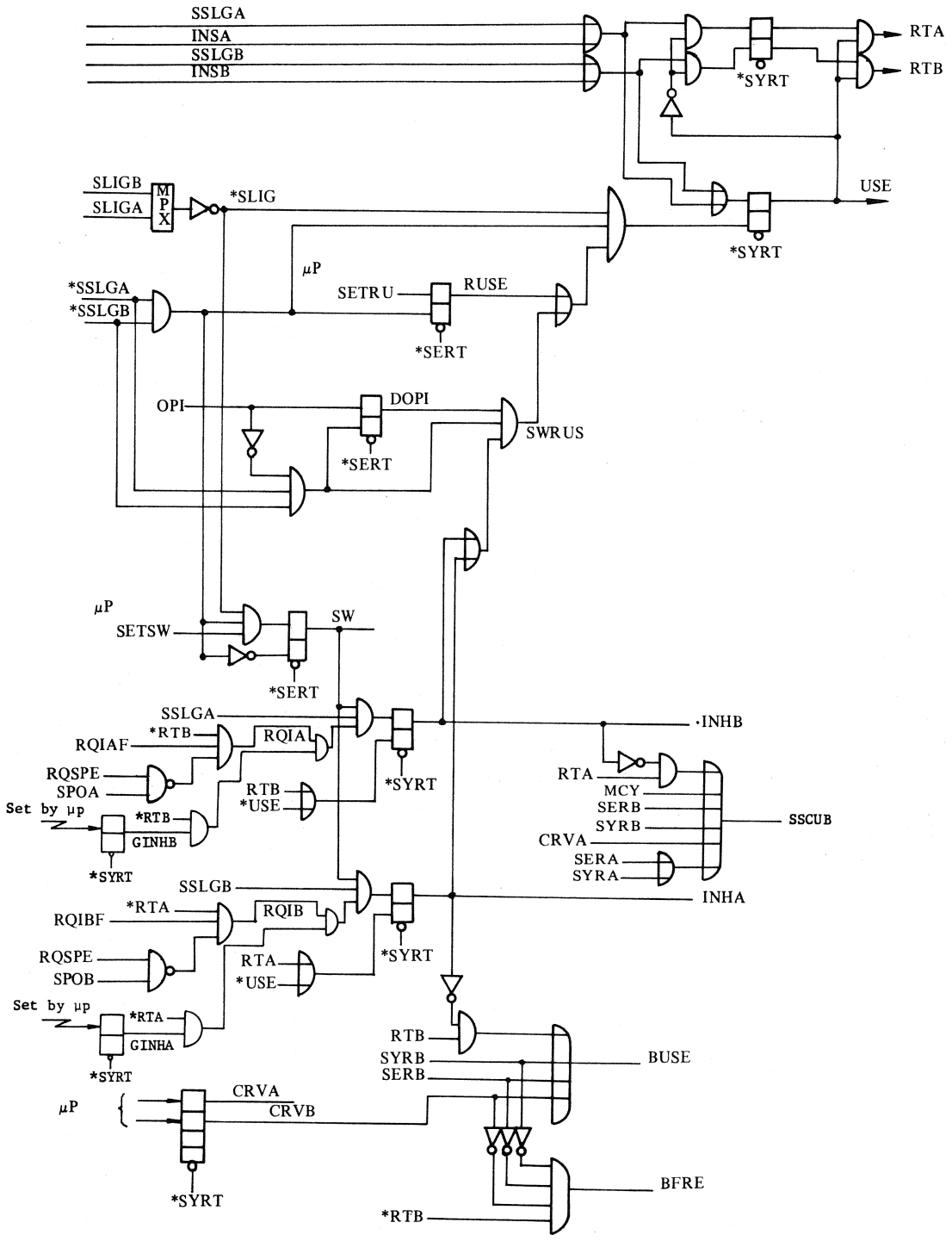


Figure 4.27 Root control circuit diagram

The USE signal is reset at OPI signal fall timing unless there is a request for next selection. At this stage the route is set to neutral status. If there is pending selection sequence on the other side, the channel switch is set to the opposite side and selection procedure is initiated. Then, signals INHA or INHB are reset as soon as the channel switch has been alternated.

CRVA (controller reserve A) or CRVB (controller reserve B) signal is set by the microprogram to reserve the MTC for one of the Channel Interfaces.

4.7 Data Transfer Control

4.7.1 Data transfer control

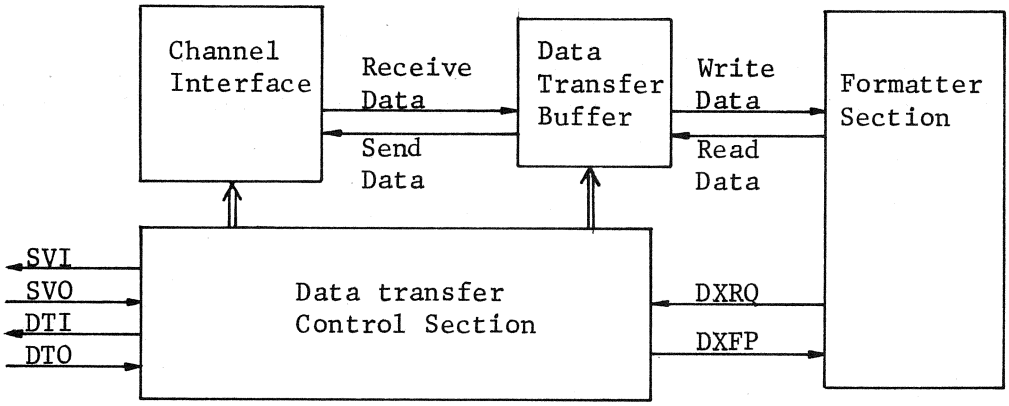


Figure 4.28 Data transfer block diagram

As shown in Figure 4.28, data transfer control section deals with control of data flow; Channel Interface ↔ Data Transfer Buffer ↔ Formatter Section. This control involves SVI (Service In) and DTI (Data In) signal control for the channel interface, and DXFP (data transfer pulse) signal control and DXRQ signal control for the formatter. The direction of data transfer is controlled by the DXFO (data transfer out) and DXF1 (data transfer in) bits in the XFCTL (transfer control) register. If the former bit is set, data is transferred from the channel to MTC. If the latter is set, data is transferred from MTC to channel. If DXFO bit is set when formatter section starts Write operation, DXRQ signal is set. Thus, the formatter section requests data to the data transfer control section. The data transfer control section requests a data to the channel by sending SVI or DTI signals, and then transfers the data to the data transfer buffer. Data XFR control section issues DXFP signal to the formatter section to transfer data from the data transfer buffer to the formatter section.

Reading data while DXFI bit has been set, the formatter section sets the DXRQ signal to the data transfer control section to transfer data. Upon receipt of this signal, the data transfer control section transfers data to the buffer along with the DXFP signal, and then issues SVI and DTI signals to the channel to request data transfer. Thus, the data from the data transfer buffer is transferred to the channel by executing the data transfer handshake sequence.

The data transfer section controls data via the transfer buffer. Data flow through the transfer buffer is illustrated in Figure 4.29. Here CL.BO is a timing signal for transfer of data from the channel to Bus Out Register. WTBX (Write Transfer Buffer) is a timing signal for entering data to the transfer buffer. CL.AR (clock for A-Register), CL.BR (clock for B Register) are timing signals for transferring data from the transfer buffer to the A or B register.

If MPRD bit is set, the data set in the M-BI register may be sent to the channel via the transfer buffer. This feature is used to transfer sense data or measuring data in diagnostic functions.

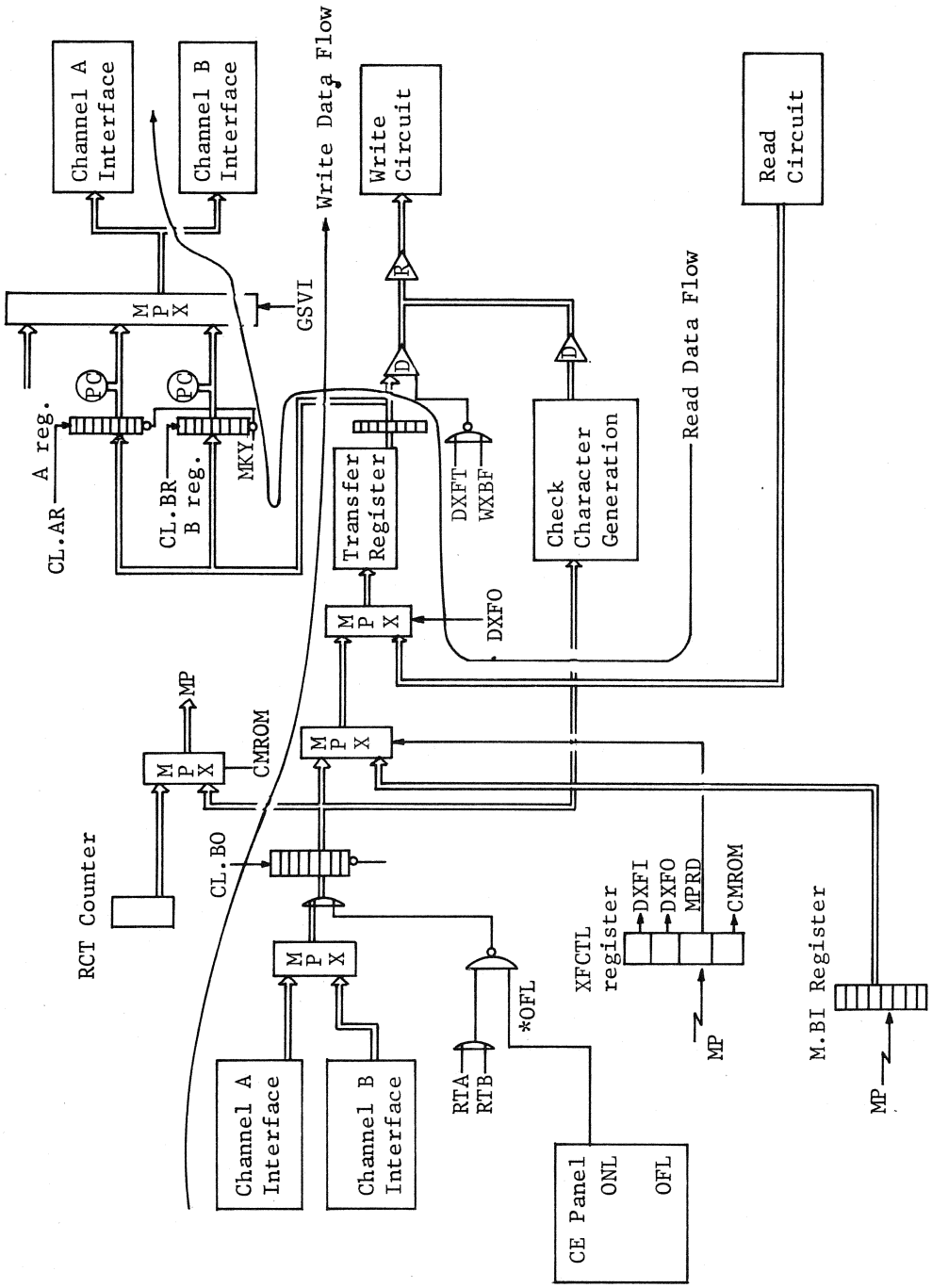


Figure 4.29 Data transfer circuit

SVI (DTI) signal may be reset upon receipt of SVO (DTO) signal from the channel. This is the normal interlock mode. On the other hand SVI (DTI) signal may be reset after a specified delay time even if SVO (DTO) signal is not received. This is called the offset interlock mode. The interlock mode for operation depends on the status of the setting unit. If the length of the cable between the channel and MTC becomes too long, the time required for the signal to travel between them becomes unacceptably long. This results in increased hand shake time and reduced speed. In such cases offset interlock mode is more suitable.

Offset interlock mode may be employed only if the channel features the data streaming function.

4.7.2 Overrun

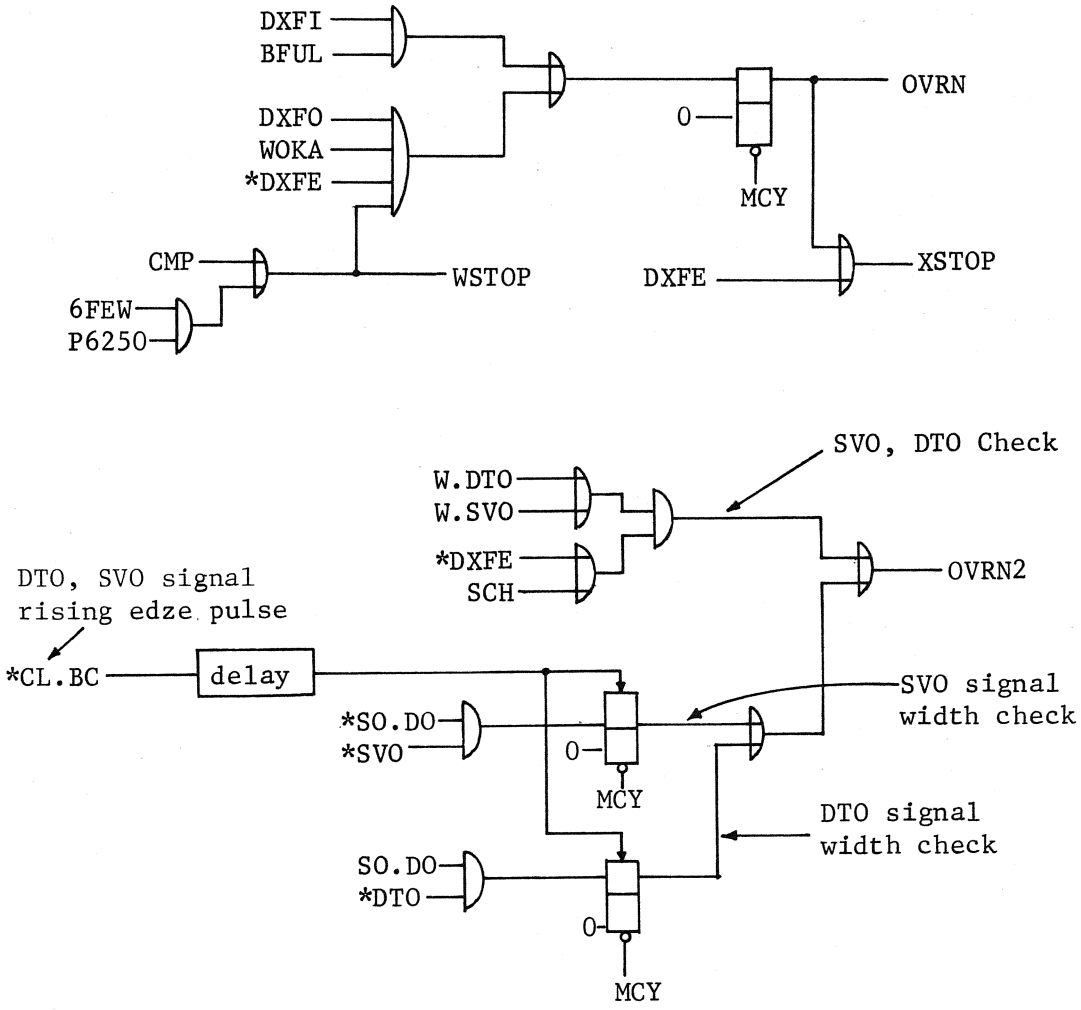


Figure 4.30 Overrun detection circuit

Overrun detection circuit is illustrates in Figure 4.30. The OVRN signal is an overrun signal detected with reference to the data transfer buffer status (refer to section 4.5.2 (16) OVRN signal). The OVRN2 signal is a check signal in the offset interlock mode. Overrun error occurs when a microprogram detects the basic signal upon completion of read or write operations.

4.8 Write Control

4.8.1 Formatter clock

As shown in Table 4.26 the clock cycle of the formatter verying with the tape speed and recording density. The number of clocks per bit cell are 3τ in 6250 mode, 6τ in 1600 mode and 12τ in 800 mode.

Table 4.26 Formatter clock

Speed (IPS)	Mode (RPI)	Full Clock (ns)	Half Clock (ns)
200	6250	184	92
	1600/800	521	260
125	6250	295	147
	1600/800	833	417
75	6250	494	247
	1600/800	1389	694
50	6250	738	369
	1600/800	2083	1042

Timing is controlled by the C and D counters. The relationship between C, D counters and bit cells is shown in Figures 4.31, 4.32 and 4.33. The C-counter is operational during idle scan status also.

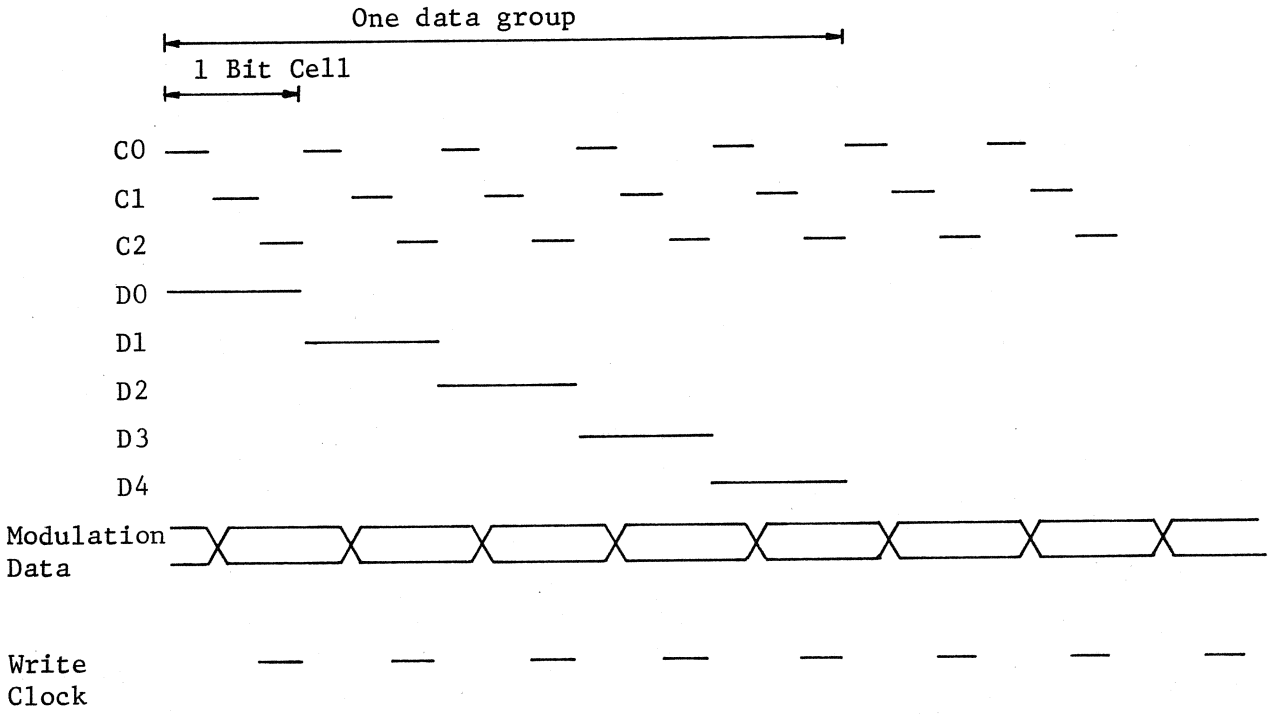


Figure 4.31 C, D counters in 6250 mode

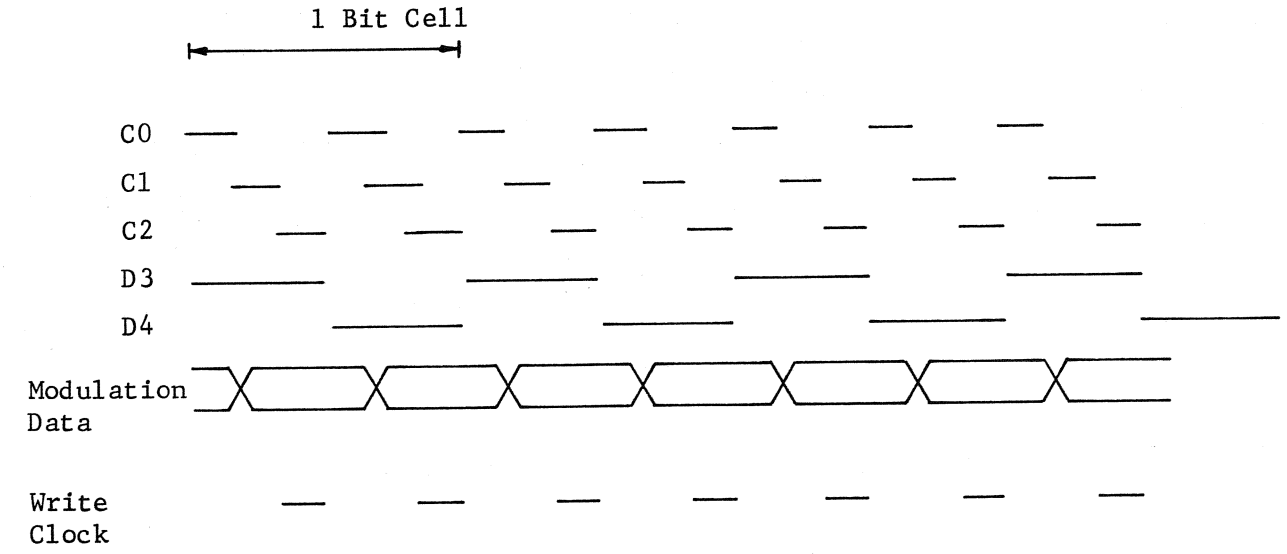


Figure 4.32 C, D counters in 1600 mode

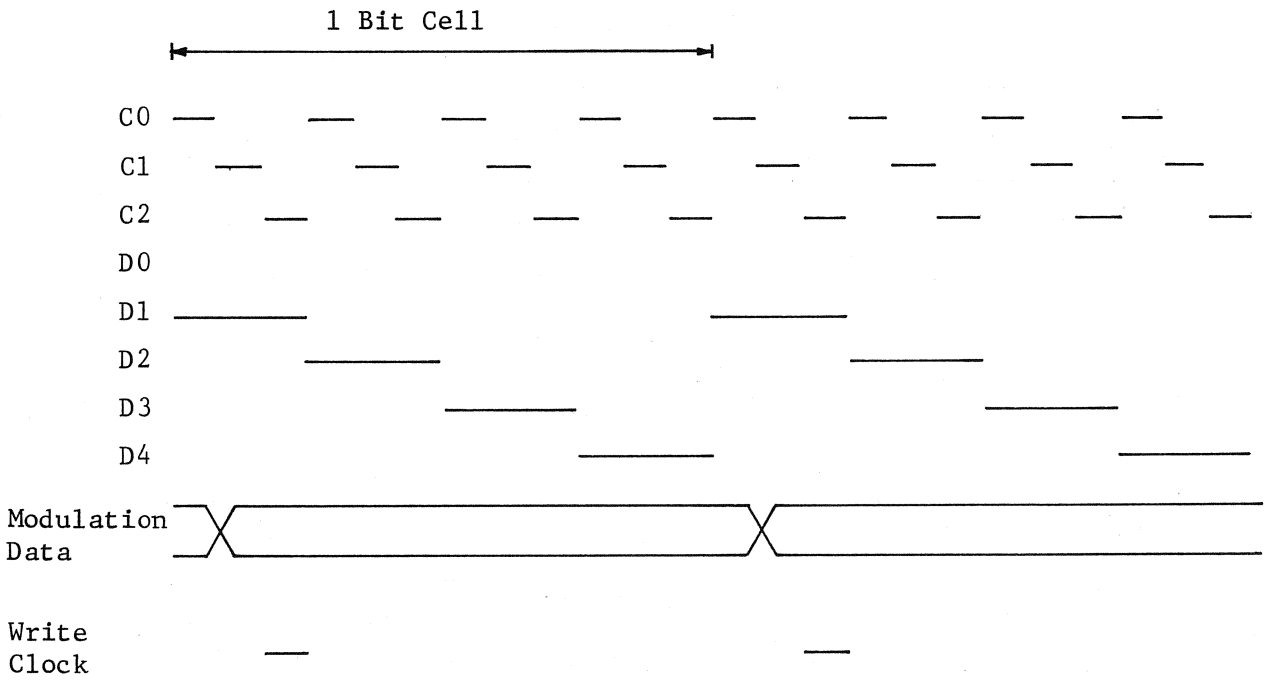


Figure 4.33 C, D counters in 800 mode

4.8.2 Start write operation

Write processing is started when MP sets a Write OK signal (WOKA). As soon as the WOKA signal is set, the WOKD signal synchronized with the formatter clock is set. Now D counter starts as soon as WOKD signal is set. At this stage the format counter starts. The Write format is controlled by this format counter. Now WOKDD signal is set as in D4 (D Counter) timing as follows: FC0 Format in 6250 mode, FC1 in 1600 mode, FC4 in 800 mode. The Write clock sent to MTU is gated by WOKDD signal.

4.8.3 Format control

Write operation of preamble, postamble and data field are controlled by the format counter and the Group Counter used to count data groups.

Table 4.17 Format counter

Format Counter	6250	1600	800
FC 0	TERM	PREA ALL"0" x 1	START
FC 1	SECOND	PREA ALL"0" x 1	-
FC 2	SYNC	PREA ALL"0" x 38	-
FC 3	MARK1	PREA ALL"1"	-
FC 4	DATA GROUP	DATA	DATA
FC 5	MARK2	-	-
FC 6	END MARK	POSA ALL"1"	CRC GAP 1
FC 7	RESIDUAL A	POSA ALL"0" x 1	CRC GAP 2
FC 8	RESIDUAL B	POSA ALL"0" x 1	CRC GAP 3
FC 9	CRC A	POSA ALL"0" x 1	CRC
FC10	CRC B	POSA ALL"0" x 1	LRC GAP 1
FC11	MARK2	POSA ALL"0" x 1	-
FC12	SYNC	POSA ALL"0" x 32	-
FC13	SECOND	POSA ALL"0" x 1	LRC GAP 2
FC14	TERM	POSA ALL"0" x 1	LRC GAP 3
FC15	(WOK RESET)	POSA ALL"0" x 1	LRC

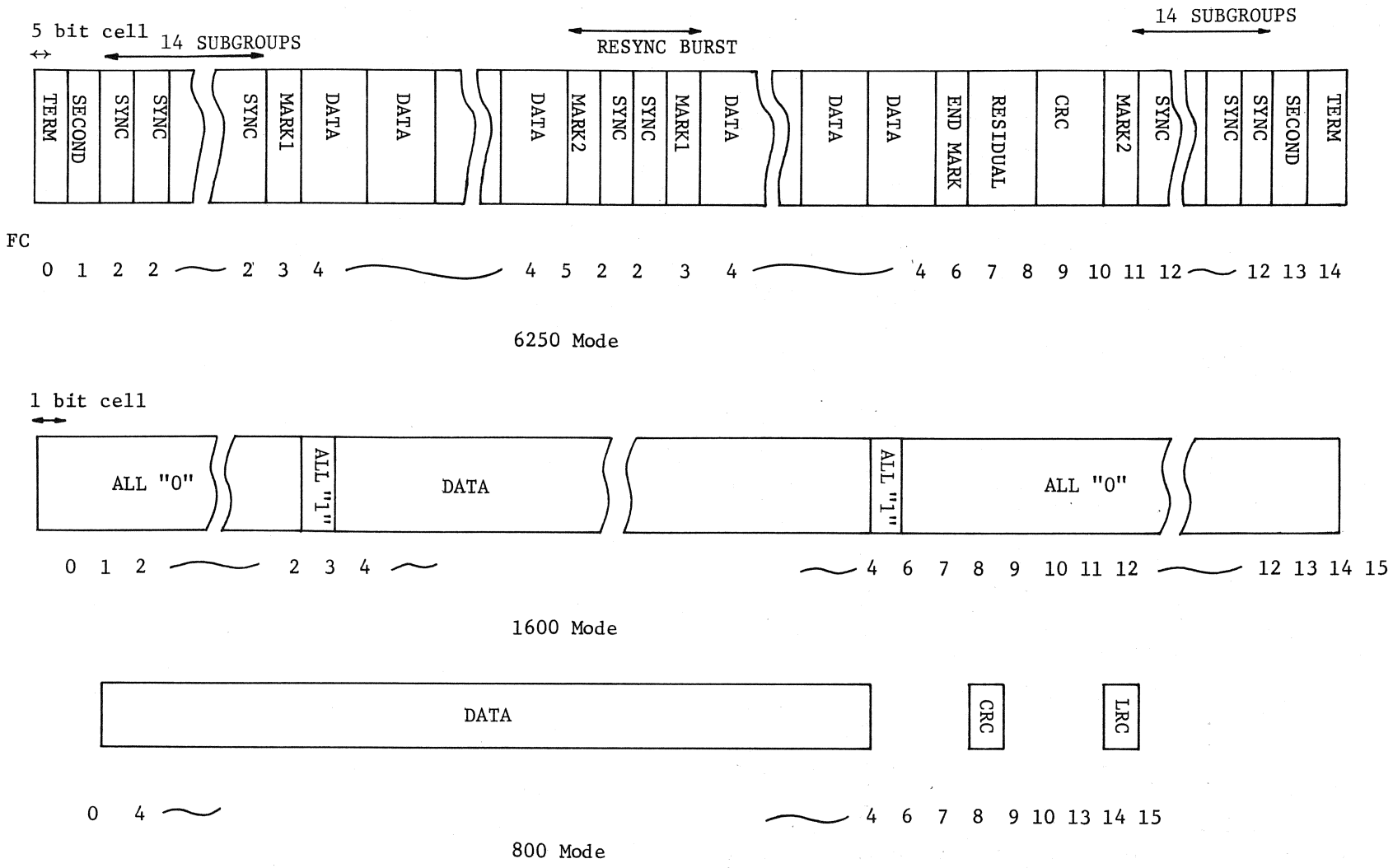


Figure 4.34 Data format

4.8.4 Data bus

The write data received from the channel is entered into the transfer buffer when the WTXB signal obtained by delaying DXFP signal by 1τ is set ON. First DXFO signal is set by the microprogram, and after data is stored in the transfer buffer and the WOK signal is set. Only then the Write operation is started. First preamble is written, and data is read out form the buffer at C2 timing after format counter becomes "4" and RO+1W signal becomes "1". The data read out from the buffer is entered CRC LSI.

In CRC LSI the data passes through Write Bus Multiplexor. Here ECC characters, padding characters etc. are added and is output from the LSI by both direction buses. The relationship between Selector signals WBSL1, 2, 4 on Write Bus Multiplexor and WDAT0~8 signals is shown in Table 4.28.

When WBSL1, 2, 4 are all '1's, CRC check circuit status passes through Write Bus Multiplexor instead of Write Data.

The parity bit of Write data obtained from Write Bus Multiplexor output. This bit is compared with the parity bit from the buffer out register. If they do not match, the Write Bus Out Check signal (WTBOC) is set to '1'.

(c) VFOS (VFO Start)

The loop filter condenser of the VFO circuit discharges while this bit is OFF. This bit should be set to '0' for a certain period of time to completely discharge the capacitor. The VFO circuit is set to Enable status when this bit is set to '1'. The VFO circuit is controlled by WTCLK signal till the receipt of time sense signal. Upon receipt of the time sense signal, VFO is reset for 1 peak pulse period to resynchronise with the data peak pulse. Then it is controlled by the data. (ROK must be set to '1' to generate a time sense signal).

(d) INDXF (Inhibit Data Transfer)

This bit is set to '1' to mask the data transfer request signal (DXRQ signal) from the Read/Write control section to data transfer control section even if conditions for generating the DXRQ signal have been established in the Read/Write control section.

Now DXRQ signal may be generated only if this bit is set to '0'.

This bit is employed in 800 BPI read operation to mask TM, CRC, LRC byte transfer and to start the control related to data transfer between the channel buffer and read/write control section. This bit is reset by HCLR signal.

(e) IHCOR (Inhibit Correction)

This bit is turned ON to inhibit error correction operation in 6250/1600 BPI mode. This bit reset or set along with the ROK bit (it should at least be set during data byte detection operation). This bit is reset by HCLR signal.

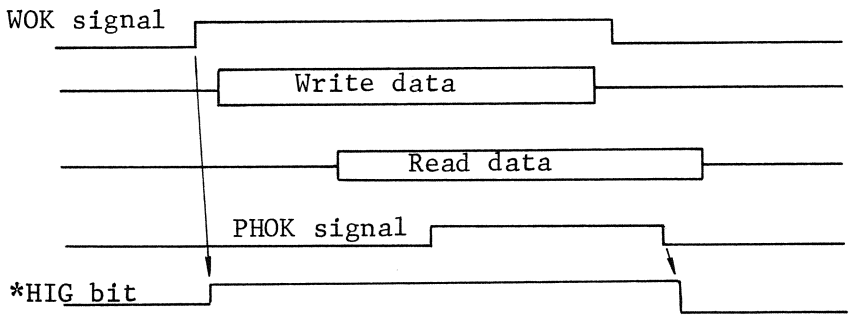
(f) *HIG (Not High Gain)

This bit is employed to alter the synchronization of the clock with data in a VFO circuit (increases the VFO loop gain). The VFO loop gain is high while this bit is set to '0'. This indicates that the synchronization capacity has increased. By setting this bit to '1' (low gain), VFO loop gain is set to normal level thus generating a very stable (low jitter) cell clock. This bit is reset by HCLR signal which sets it to a low gain status.

This bit must be set to '1' in 1600 BPI mode Read/Write operation.

In 6250 BPI mode, this bit should be controlled as shown in the following figure.

(1) Write operation



(2) Read operation

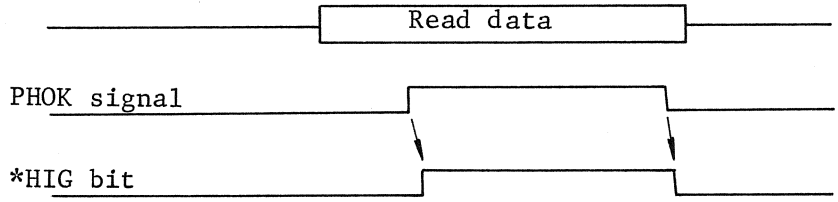


Figure 4.15 *HIG bit control in 6250 BPI mode

(g) ISPHE (Issue Phase Error)

This bit is used to generate a phase error. A phase error is (PHE) generated in the track corresponding to the MASK bit 0-9 which have been turned ON. (For further details refer to Chapter 9).

This bit is reset by HCLR signal.

(h) SKWMG (Skew Marginal)

The skew check condition is set to marginal as soon as this bit is turned ON. This bit may be used only in 1600 mode.

This bit is reset by HCLR signal.

(13) MODE (Mode Select): 4C

0	1	2	3	4	5	6	7
MCY	BWD	WKS	ZRD	6250	1600	CMCY	CBR

(a) MCY (Machine cycle)

The MCY signal is turned ON to enable Read, Write, Device Control Circuits. In this stage these circuits may be controlled from microprogram while MCY signal is ON.

This bit is reset by HCLR signal.

(b) BWD (Backward)

This bit is turned 'ON' (set to 1) to set the MTC Read circuit to Backward Mode. This bit is read by HCLR signal.

(c) WRS (Write Status)

This bit is turned ON (set to '1') to set the MTC R/W circuit to Write Mode.

The following check conditions may be affected by this bit: HNIS (Noise Block) check condition.

Postamble Read End (EPOSA) condition. STRCK (Start Read Check) condition. HTM (tape mark detection, skew mark, error correction and other control conditions. Read status is set when this bit is '0'. This bit is reset by HCLR signal.

(d) NRD (NRZ Read)

This bit is set to execute 800 BPI, Read/write operation. When this bit is on the modulation circuit will generate a peak pulse as the data rises if the BWD bit is '1' and a peak pulse as the input data falls if the BWD bit is '0'. Both the pulses are generated as peak pulses.

This bit is reset by HCLR signal.

(e) 6250 (6250 mode)

This bit is set to '1' to execute 6250 BPI Read/Write operation. This bit is reset by HCLR signal.

(f) 1600 (1600 mode)

This bit is set to '1' to execute read/write operation in 1600 BPI mode.

This bit is reset by the HCLR signal.

(g) CMCY (Complete MCY)

This bit is not used. This bit is reset by HCLR signal.

(h) CBR (Channel Buffer Read)

This bit is set to '1' to execute a channel buffer Read operation. As soon as this bit is set to '1', the data transmit control section repeatedly transfers the channel buffer data. This bit is reset by HCLR signal.

(14) RDSNS (Read Format Sense): 4D

0	1	2	3	4	5	6	7
/HNIS	/HBLK	/HTM	/WIND	/PHOK	/PREA	/POSA	/EPOSA

(a) HNIS (Noise Block Detected)

If a noise pattern is detected (DNois=1) for a duration described in Table 4.17 this bit is set to '1'. This bit remains unchanged till ROK is turned OFF. ROK is OFF.

Table 4.17 HNIS set condition

Mode		Condition
6250	WRS	46 ± 2 Bit cell period, continuous PNOIS
	RDS	22 ± 2 Bit cell period, continuous PNOIS
1600	WRD	23 ± 2 Bit cell period, continuous PNOIS
	RDS	11 ± 1 Bit cell period, continuous POINS

This bit is not set in 800 BPI mode.

(b) HBLK (Block Detected)

If a block pattern (DBOB='1') is detected for a duration in excess of the specified bit cell period, this bit is set to '1'. This bit remains unchanged till it is reset when ROK is turned OFF. This bit is in Reset status while ROK is OFF.

Table 4.18 HBLK set condition

Mode		Condition
6250	WRS	25 ± 1 Bit cell period, continuous DBOB
	RDS	25 ± 1 Bit cell period, continuous DBOB
1600	WRS	12.5 ± 0.5 Bit cell period, continuous DBOB
	RDS	12.5 ± 0.5 Bit cell period, continuous DBOB

This bit is not set in 800 BPI mode.

(c) HTM (Tape Mark Block Detected)

If a tape mark block pattern (DTM='1') is detected continuously in excess of the specified bit cell period, this bit is set to '1'. This bit remains unchanged till reset when ROK is OFF. This bit is reset while ROK is OFF.

Table 4.19 HTM setting condition

Mode		Condition
6250	WRS	304 ± 8 Bit cell period, continuous DTM
	RDS	42 ± 2 Bit cell period, continuous DTM
1600	WRS	84 ± 4 Bit cell period, continuous DTM
	RDS	21 ± 1 Bit cell period, continuous DTM

This bit is not set in 800 BPI mode.

(d) WIND (Window)

In Write operation, this signal becomes '1' during a specified period after specified delay time has elapsed from starting Write operation. The leading of the block recorded in the corresponding write operation should be detected while this signal is '1'. The data bytes (800) or DBOB detected between

the period from starting the Write Operation till rise of this signal. Will set NOISC signal (described later) to '1'.

The SLIPC (described later) will be set to '1' if Wind Signal is set to '0' without detecting a data byte (800) or DNOIS signal. Figure 4.15 shows set and reset timing of WIND signal.

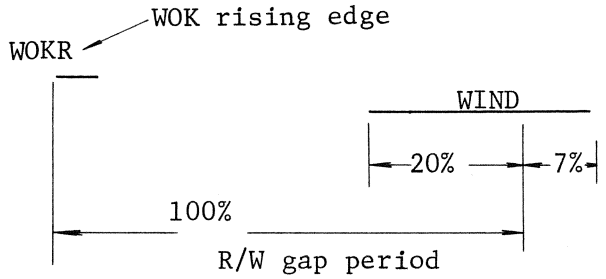


Figure 4.16 WIND signal

(e) PHOK (Phase OK)

This signal is set while HBLK signal rises when STPHK has been set. This signal is reset when the EPOSA signal rises (described later) or STPHK is reset. While this signal is ON, Write data error check and correction are available.

(f) PREA (Preamble Detected)

This signal is set to '1' upon detection of the first data byte in the 6250, 1600 BPI Read Circuit. The status of this signal remains unchanged till PHOK is reset. This bit is in reset status while PHOK is '0'.

(g) POSA (Postamble Detected)

This signal is set to '1' upon detection of the last data byte (Head of Postamble) in 6250, 1600 BPI Read Circuit. This bit remains unchanged till PHOK is reset. This bit remains in reset status while PHOK is '0'.

(h) EPOSA (End of Postamble)

This bit is set to '1' after the specified length of postamble is confirmed in 6250, 1600 BPI Read/Write operation. This bit is reset ('0') when DIBG signal rises. This bit is in reset status while MCY is OFF.

Table 4.20 EPOSA set condition

Mode		Condition
6250	WRS	After POSA=1 and after a delay of 34 ± 2 bit cells.
	RDS	After POSA=1 and after a delay of 6 ± 2 bit cells.
1600	WRS	After POSA=2 and after a delay of 31 ± 1 bit cells.
	RDS	After POSA=1 and after a delay of 21 ± 1 bit cells.

(15) CRCST (CRC Status): 4E

0	1	2	3	4	5	6	7
*MCRC	*MCRCZ	*EP=CR	*B=D	*B=C	*MCRCC	*A=B	*XBIC

(a) *MCRC (Unmatch CRC)

This bit is when the CRC pattern generated as a result of operating on the Read Data (including CRC byte) is not normal (bits other than 2, 4 of CRC register are ON). This bit is employed in Read, Write, and Back Read operations in 6250, 800 mode. This bit is ON ('1') when MCY is OFF.

(b) *MCRCZ (Unmatch CRC zero)

This bit is '1' when the CRC pattern generated as a result of operating on Read data (including CRC pattern) is not all '0's. This bit is employed in Read, Write and Back Read Operations in 800 mode. This bit is '0' when MCY is OFF.

(c) *EP=CR (EP≠CR)

This bit is '1' if the pattern obtained by reversing the pattern (except bits 2, 4) generated by operating on the Read data (including CRC byte) does not match with the error pattern register. It is used for detecting errors along with the *MCRCZ signal in 800 mode. This bit is set to '1' while MCY is OFF.

(d) *B=D (CRCB≠CRCD)

This bit is employed in Read, Write operations (excluding Back Read) in 6250 mode. This bit is turned ON ('1') when the Aux-CRC byte (CRCD) does not match with the CRCB pattern (CRC generated from transfer Buffer output). This bit is '1' while MCY is OFF.

(e) *B=C (CRCB≠CRCC)

This bit is employed in 1600, 800 mode write operation. This bit is turned ON when the Write Data CRC pattern (obtained from CRCB - XFR buffer output) does not match with the After Read data (excluding CRC byte) CRC pattern. This bit is set to '0' while MCY is OFF.

(f) *MCRCC (Unmatch CRCC)

This bit is '1' when the CRC pattern obtained from Read Data (excluding CRC byte) is not normal. This bit is employed in Back Read processing in 6250 mode. This bit is '1' while MCY is off.

(g) *A=B (CRCA≠CRCB)

This bit is '1' when the pattern generated from the input data to XFR buffer does not match with the CRC pattern generated from XFR register output data. This bit is '0' while MCY is OFF.

(h) *XBIC (*XBF Bus In Check)

This bit is set when illegal XFR Buffer Input data pattern is detected. This bit is not reset until MCY is turned OFF. This bit is '0' while MCY is OFF.

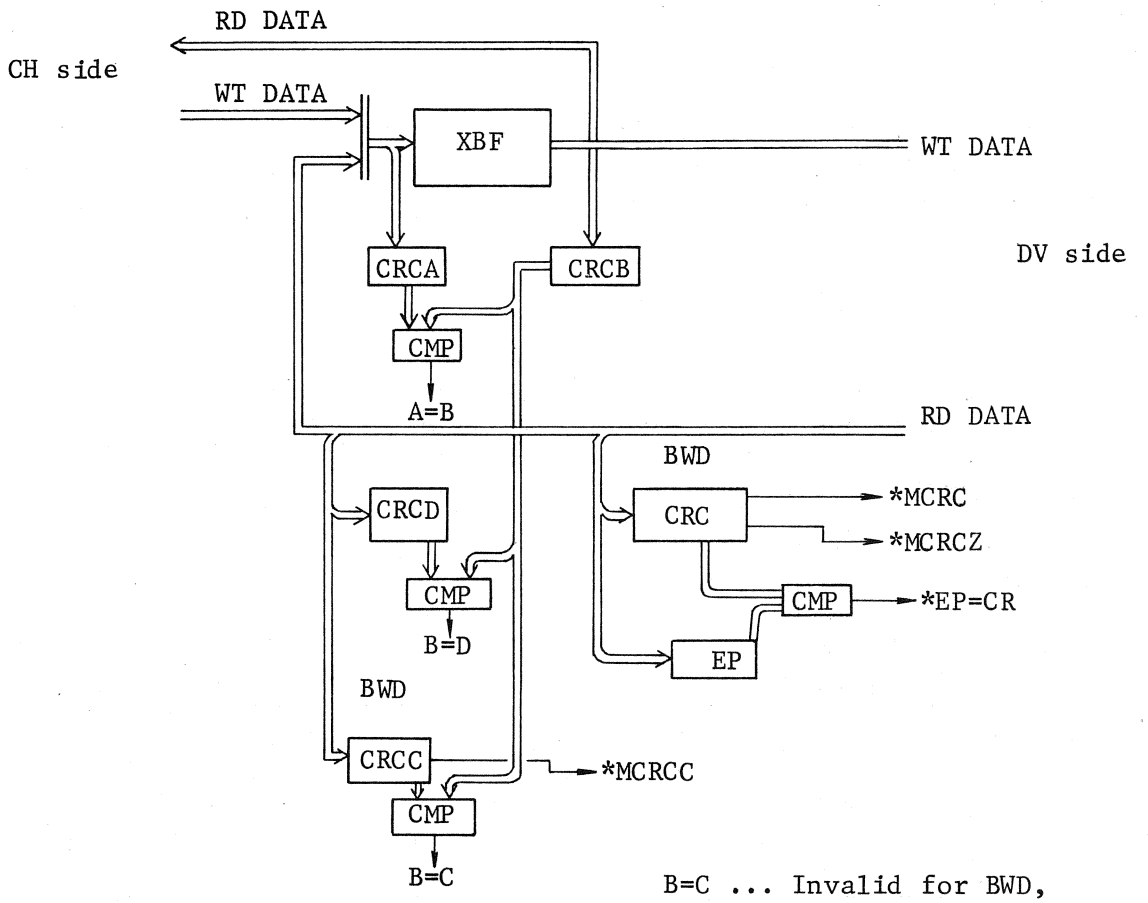


Figure 4.17

Table 4.21

Mode	Input Byte Operation				
	CRCA	CRCB	CRC	CRCC	CRCD
6250	XBF Input data (Write→Write Data, Read→Read Data)	XBF Output data (Write→Write Data, Read→Read Data)	Data, Pad, Aux. CRC CRC Byte, 1 Byte	Data, Aux. CRC (BRD only)	Aux, CRC (BRD not feasible)
1600				Data	
800			Data, CRC	Data	

(16) FMERR (Format Error): 4F

0	1	2	3	4	5	6	7
/*SRDC	/*EDCK	/*SLIPC	/*NOISC	/*WTBOC	/*WTVRC	/*OVRN	/*CMP

(a) *SRDC (Not Start Read Check)

This bit is turned ON, if the PREA signal (Start of Data Field Detection Signal) is not set within the specified delay time after PHOK. This signal remains at '0' till MCY is OFF. This bit is '1' while MCY is OFF. This bit, '1', means that Start Read Check error has not been detected in the Read Operation.

Table 4.22 SRDC Set condition

Mode		Condition
6250	WRS	When PREA=0 upon specified delay of 120 ± 8 bit cells after PHOK set.
	RDS	When PREA=0 upon specified delay of 168 ± 8 bit cells after PHOK set.
1600	WRS	When PREA=0 upon specified delay of 52 ± 4 bit cells after PHOK set.
	RSD	When PREA=0 upon specified delay of 63 ± 4 bit cells after PHOK Set.

This bit is not available in 800 BPI mode.

(b) *EDCK (Not End Data Check)

This bit is turned ON if DIBG signal cannot be detected within the specified time after EPOSA (see Table 4.23 for a specified time delay after preamble). Once set to '0' it is not reset ('1') till MCY is OFF. It is '1' while MCY is OFF. This bit, '1' may be assumed that End Data Check Error has not occurred in the Read Operation.

Table 4.23 EDC Condition

Mode		Condition
6250	WRS	When DIBC=0 upon delay of 88 ± 8 bit cells after EPOSA=1.
	RDS	When DIBC=0 upon delay of 248 ± 8 bit cells after EPOSA=1.
1600	WRS	When DIBC=0 upon delay of 20 ± 4 bit cells after EPOSA=1.
	RDS	When DIBC=0 upon delay of 36 ± 4 bit cells after EPOSA=1.

Not available in 800 BPI mode.

(c) *SLIPC (Not Slip Check)

This bit is set to '0' upon detection of data write (800 BPI) or DNOIS signal (6250/1600 BPI) while the above mentioned WIND signal (section (14), d) is '1'. Once set to '0', the status of this signal remains unchanged till MCY is turned OFF. This bit is '1' while MCY is '1'.

This bit, '1', may be assumed that no slip check error has occured in Write Operation. This bit is '1' when MCY or STPHK is '0'.

(d) *NOISC (Not Noise Check)

This bit is set to '0' when data byte (800 BPI) or DBOB signal (6250/1600 BPI) is detected within the specified delay time after starting Write Operation (WOK Rise). Once set to '0' the status of this signal remains unchanged till MCY is turned OFF. This bit is '1' when MCY is OFF. This bit is '1' when MCY or STPHK signal is '0'.

(e) *WTBOC (Not Write Data Bus-Out Check)

This bit is set to '0' when a parity error is detected in the Write Bus Data to be entered to the Write Circuit. This bit is not set to '0' when the above mentioned WTCTL register ALIWT bit is set to '0'.

This bit remains in '0' status while MCY is OFF. This bit is set to '1' by HCLR signal. When this bit is '1' it may be assumed that no parity error has occurred in Write Circuit during Write Operation.

(f) *WTVRC (Not Write VRC)

This bit is set to '0' when a parity error is detected in the modulated Write Data . Once set to '0' the status of this byte remains unchanged till MCY is turned OFF. When this bit is '1' it may be assumed that no parity error has occurred in modulated data in Write Operation.

(g) *OVRN (Not Over Run)

This bit is set to '0' when overrun is detected in Read/Write Operation. Once set to '0' the status of this bit remains unchanged till MCY is turned OFF. This bit is '0' when MCY is OFF. When this bit is '1', it may be assumed that overrun error has not been detected in Read/Write Operation.

- OVRN Set Condition -

1. When DXF1=1 (Read Operation)

   . If XFR Buffer is Full (BFUL=1)

2. DXFO=1 (Write Operation)

   . If XFR Buffer became empty (CMP=1) before receiptor "transfer STOP" from the channel interface during Write Operation.

   . If the data left in the XFR buffer was less than 6 bytes before the "transfer STOP" was issued by the channel interface in 6250 mode Write operation.

(h) *CMP (Not Compare)

This bit is set to '0' if the XFR buffer Read-In count and Read Out count do not match. This bit indicates the presence or absence of data in XFR buffer. There is no data in XFR buffer if this bit is '0' and there is data in the buffer if this bit is '1'. This bit is '0' when MCY is OFF.

(17) TSNS (Time Sense): 50

0	1	2	3	4	5	6	7
*TSNS0	*TSNS1	*TSNS2	*TSNS3	*TSNS4	*TSNS5	*TSNS6	*TSNS7

Each of these bits is '0' when the peak pulse of the tracks rising and falling and falling edgepulse of Read Data, corresponding to these bits has been coming with required period and with specified cycles. *TSNS0~7 are all '1's while MCY is OFF. Peak pulse may only be generated if ROK=1.

(18) POINT (Pointer): 51

0	1	2	3	4	5	6	7
*DET0	*DET1	*DET2	*DET3	*DET4	*DET5	*DET6	*DET7

DET ... Detect Error Track

This is an error track pointer used in Read write operation in 6250/1600 BPI mode. All the bits are '1' while MCY is OFF. DET0~8 are set by dead track (skew, persistant track, drop out) valid pointer or ECC group buffer pointer.

(19) BLFMT (Block Format): 52

0	1	2	3	4	5	6	7
*1O2CR	*DET8	*TSNS8	*DIBG	*DNOIS	*DBOB	*DRRA	*DTM

(a) *1O2CR (No 1 or 2 track correction)

This bit is set to '0' if 1 or 2 track error correction has been executed in 6250/1600 BPI read operation. Once set to '0' this bit remains in this status till MCY is OFF. This bit is '1' while MCY is OFF.

When SCAN bit is '1', this bit represents a scan out signal of LSI chips related to read operation.

(b) *DET8 (No Detect Error Track 8)

Refer to section (18), *DET0~7.

(c) *TSNS8 (No Time Sense 8)

Refer to section (17). TSNS0~7.

(d) *DIBG (Not Detect IGB)

This bit is '1' when TSN0~8 represents IBG pattern.

(e) *DNOIS (Not Detect Noise)

This bit is '0' when TSNS0~8 represents NOIS pattern.

(f) *DBOB (Not Detect BOB)

This bit is '0' when TSNS0~8 represents BOB pattern.

(g) *DARA (Not Detect ARA)

This bit is '0' when TSNS0~8 represents ARA pattern.

(h) *DTM (Not Detect TM)

This bit is '0' when TSNS0~8 represents TM patten. It is also '0' when TM byte is detected in 800 BPI mode.

$$DIBG = \overline{0 + 1 + 2 + 3 + 4 + 5 + 6 + 7 + 8}$$

$$DNOIS = A + B$$

$$A = (0.5.8)+(2.6.7)+(1.3.4)$$

$$B = (0+5+8).(2+6+7).(1+3+4)$$

$$DBOB = A.B$$

$$DTM = \overline{(1+3+4)}\{(0.5.8)(2.6.7) + PE.R\ DS[(0.5.8)+(2.6.7)] + GCR.RDS[(2.6.7)(0+5+8)+(0.5.8)(2+6+7)]\}$$

$$DARA = \overline{(0+8+5)}\{(1.3.4)(2.6.7) + RDS[(1.3.4)(2+6+7)+(1+3+4)(2.6.7)]\}$$

0~8, TSNS0~8

(20) RDERR (Read Error): 53

0	1	2	3	4	5	6	7
*VRCE	*MLTE (*LRCE)	*SKWE	*DBCK	*DROE	PNMLT	*POSAE	"0"

(a) *VRCE (No VRC Error)

This bit is set to '0' when a Read Data Parity Error is detected and cannot be recovered by the pointer or ECC. Once this bit is set to '0' it remains in this status till MCY is turned OFF. This bit is '1' while MCY is OFF. This bit, '0', indicates an incorrectable VRC error. Error is not corrected if the above IHCOR bit has been set.

(b) *MLTE (*LRCE) (No Multiple Track Error or no LRC Error)

This bit is set to '0' under the following conditions:

a) When more than 2 DET0~8 bits are set in 6250/1600 BPI Write operation or 1600 BPI read operation.

b) When more than three DET0~8 bits are set in 6250 BPI mode Read operation.

c) When LRC error is detected in 800 BPI mode write/read operation. Once set to '0' the status of this bit remains unchanged till MCY is turned OFF. This bit is set to '1' when more than one error tracks are detected or when incorrectable LRC error is detected in 800 BPI mode.

(c) *SKWE (No Skew Error)

This bit is set to '0' when multiple skew errors are detected in read data. Once set to '0' this bit remains in this status till MCY is turned OFF. This bit is '1' only if MCY is OFF. When this bit is ON it may be assumed that skew error has not occurred.

(d) *BDCK (No Deskewing Buffer Check)

This bit is set to '0' in 6250 BPI mode Write and forward Read operations if the Deskewing Buffer read out count is not all '0's when resynchronous burst is detected. Once this bit is set to '0', it will remain in this status till MCY is turned OFF. This bit is therefore '1' when MCY is OFF. When this bit is '1' it may be assumed that skew buffer error has not occurred. This bit may not be used in 1600/800 BPI modes.

(e) *DROE (No Drop Out Error)

This bit is set to '0' when one of the TSNS0~8 signal is '0' while PHOK signal is '1' in Write operation (WRS=1). Once this bit has been set to '0' it will remain in this status till MCY is turned OFF. This bit is therefore '1' while MCY is OFF. When this bit is '1', it may be assumed that drop out error has not been detected in the 6250/1600 BPI Write Operation.

(f) PNMLT (Pointer Multiple)

This bit is set to '1' to indicate that more than two track pointers in 1600/6250 BPI mode Read/Write Operation.

(g) *POSAE (No Postamble Error)

This bit is set to '0' when illegal postamble byte (all '1's:6250, all '0's:1600) follows the postamble head (POSA=1). Once set to '0', it will remain in this status till MCY is turned OFF. It is '1' when MYC is OFF. When this bit is '1', it may be assumed that postamble error has not been detected. This bit is not available in 800 BPI mode.

(21) ZETK (NRZ Error Track): 54

0	1	2	3	4	5	6	7
ETK0	ETK1	ETK2	ETK3	ETK4	ETK5	ETK6	ETK7

This register is employed to correct errors in 800 BPI mode Read Operation. The data corresponding to the bit set to '1' is reversed for read operation. This register is also reset by HCLR signal.

(22) ZCTL (NRZ Control): 55

0	1	2	3	4	5	6	7
SFCRC	LRC	CRC	HBLKN	BLKED	CRCHG	CRCRG	R.RDB/RDB.S

(a) SFCRC (Shift CRC Register)

Set this bit to '1' to cause a shift of CRC register, and 1 CRC data pattern is processed. This bit is reset ('0') after CRC register has been shifted. This bit is '0' while MCY is OFF. In the 800 BPI mode, to set this bit cause a shift of CRC pattern register upon detecting a data byte.

(b) LRC (LRC Cycle)

This bit is set to '1' in FWD operation after CRC byte has read. If a CRC byte has not been detected, this bit will be set to '1' after a period equivalent to 5.3 bit cells from the last data byte. Once set, the status of this bit remains unchanged till ROK is turned OFF.

In BWD operation this bit is set to '1' as ROK rises and is reset to '0' upon the detection of the first data byte (LRC byte). This bit is '0' while ROK is OFF.

This bit indicate that the current data byte is a LRC byte. This bit is valid only in 800 BPI mode.

(c) CRC (CRC Cycle)

In FWD processing this bit is set to '1', if data bytes are not detected in the length of 2 bit cells after the last data byte. This bit remains in this status till 3.3 bit cells or till the detection of a LRC byte. In BWD operation this bit is set to '1' upon detection of LRC byte. (first byte) This bit remains '1' till the detection of data byte. If data byte can't be detected within 5.3 bit cell from LRC byte, this bit will reset to '0'. This bit is '0' while ROK is off. This bit indicate that the byte detected is a CRC byte. It is valid only in 800 BPI mode.

(d) HBLKN (NRZ Block)

This bit is set to '1' upon detection of 1 Byte when WRS=1 and upon detection of 8 bytes (including CRC and LRC bytes) when WRS=0. The byte remains in this status till MCY is turned OFF. This bit is therefore '0' while MCY is OFF. This bit represents detecting of an 800 BPI block.

(e) BLKED (NRZ Block End)

This bit is turned ON ('1') to indicate that data or check byte was not detected during 10.7 bit cell period in 800 BPI mode processing. Once turned ON, the status of this bit remains unchanged till R. RBD is set to '1' or MCY is turned OFF. This bit is therefore '0' while MCY is 'OFF'.

(f) CRCHG (CRC Horizon Gap)

In a 800 BPI mode read operation, this bit is turned ON ('1') when a data byte is not detected for a period of 5.3 bit cells after the last data byte. This bit, '1', indicate that a gap exceeding the permissible recording gap for CRC byte has been detected. Therefore a CRC byte is either not present or CRC byte is all '0's when this bit is '1'. This bit is reset by turning ON R.RDB bit ('1') or by turning OFF MCY bit.

(g) CRCRG (CRC Recording Gap)

This bit is turned ON to indicate that a recording gap longer than 2 bit cells has been detected. CRC byte should be detected after this bit has been turned ON and before the CRC HG is set.

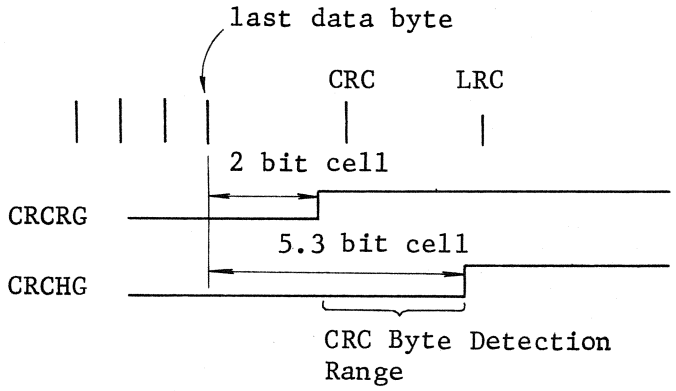


Figure 4.18

This bit is reset under the same conditions as that of CRCHG bit.

(h) R.RDB/RDB.S (Reset Read-Data-Byte/Read-Data-Byte Set)

In 800 BPI mode, this bit is set to '1' by the sampling pulse. Once set, this bit may not be reset till turning R.RDB bit ON or till MCY is turned OFF. This bit is therefore '0' while MCY is OFF. Set RDB.S bit to '1' to reset RDB.S to '0'. Then CHCHG, CHCRG and BLKCD bits are also reset to '0'. This bit may be used for counting read data byte in 800 BPI mode.

(23) ZMRG (NRZ Marginal Code): 56

0	1	2	3	4	5	6	7
*NVRCE	ETK8	*NSKWE	SDNT / *LRCE	TM0	TM1	TM2	TM3

(a) *NVRCE (No NRZ-VRC-Error)

This bit indicate that VRC error has not been detected in the 800 BPI Read Operation. This bit is set to '0' as soon as a VRC error has detected. This bit may be reset to '0' by SDRST bit. This bit is also '1' while MCY is OFF.

(b) ETK8 (NRZ Error Track 8)

Comforms with ETK bits 0~7 in section (21).

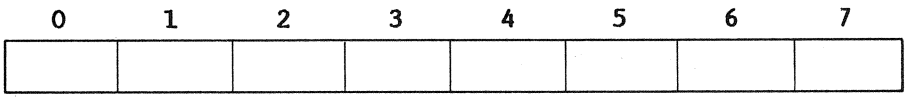
(c) *NSKWE (No NRZ Skew Error)

In 800 BPI write operation, this bit is set to '0' when multiple skew errors are detected in the data read from the Read Head. This bit is not reset to '1' till the SDRST bit is turned ON or MCY bit is turned OFF.

(d) SDRST/*LRCE (Sense Data Reset/Not LRC Error)

This bit with '0' indicate that a parity error has been detected in LRC byte (LRC error). *LRCE bit is reset ('1') when MCY is turned OFF. Setting this bit to '1' by up (SDRST='1'), the above *NSKWE, *NWRCE bits will be reset to '1'.

(24) ZOP (NRZ OPTION): 57



This register indicates whether the 800 BPI optional PCA (1A01: 512189) has been mounted. One of the bits in this register is '1' when the above optional board is mounted. If all the bits in this register are '0', the registers 54~56 are not available.

(25) TCADA (MTC Address CH-A): 58

0	1	2	3	4	5	6	7
/CADA0	/CADA1	/CADA2	/CADA3	/CADA4	/SBMC	/CPBL	/NOFS
				(CM0)	(CM1)	(CM2)	(CM3)

(a) CADA0~CADA4 (MTC Address CH-A 0~4)

These are the MTC address set by shoot plug for CH-A side.

(b) When the CMROM bit (see (32), 5) is '1', bits 4~7 represent CM0~3.

CM0~3 is obtained by converting the 8 bit code from CHBI register into a four bit code. When CMROM bit is '0', bits 4~7 represent CADA4 and following CH interface control bit.

SBMC; '1' when special MBC interface.
CPBL; '1' when IBM compatible mode.
NOFS; '1' when normal interlock handshake
(not offset interlock)

(26) OUTAG (Out Tag Sense): 59

0	1	2	3	4	5	6	7
/ADO	/CMO	/SVO	/SLIG	/OPOA	/RQSPE	/OIS	/INS

(a) ADO (Address Out)

This is the address out signal from the channel interface to which MTC is logically connected. If MTC is not connected either to CH-A or CH-B or if CE panel ONL/OFL switch is set to OFL side, this bit is '0'.

If this bit is '1' and if the CMROM bit is '0', the CHBO register represents the I/O address specified by the channel.

(b) CMO (Command Out)

This is a CMO signal from the CH-B or CH-A side. If MTC does not logically connect to any CH interface or if the CE panel ONL/OFL switch is set to OFL side, this bit is '0'. If this bit is '1', the above mentioned CHBO register, when CMROM=0, indicates the command code specified by channel.

(c) SVO (Service Out)

This is the SVO signal from channel interface. This bit is '0' if none of the channels is logically connected to MTC. This signal is the same to the SVI signal when the CE panel ONL/OFL switch is set to OFL side. When this bit is '1', it indicates that either the linked channel has received the Bus-In data or that the data requested by SVI is present on Bus-Out.

(d) SLIG (Select in Gate)

This signal is '1' if MTC is selected by the channel. It is '0' when the select out signal is released. This bit is turned ON to indicate that MTC has been selected. The SLO signal gates the passing signals to the control device. This bit is '0' if none of the channels is linked or if the CE panel switch set to OFL. This bit is reset by the SERT signal.

(e) OPOA (Operational OUT CH-A)

This is the OPO signal from the channel interface A side (basic side) channel.

(f) RQSPE (Request-In Suppress Enable)

Set this bit to '1' so that the channel interface RQI signal may be suppressed by the SPO signal. RQI signal to CH interface will be generated only when this bit is OFF, RQIAF (RQIBF) is set to '1' and SPOA (SPOB) is not ON. This signal is reset by the SERT signal.

(g) QIS (Request-in Initial Selection)

This bit is '1' when the initial selection sequence is started with the linked channel as a response to a Request-In. Upon set of OPI bit this bit is reset to '0'. This bit is not '1' when MTC is not linked to any channel or when CE panel ONL/OFL switch is set to 'OFL'.

(h) INS (Initial Selection)

This bit is '1' when the initial selection sequence (ADO=1, select-out ON) is started in the selected channel. When the channel has linked in this sequence (OPI=1) this bit is '0'. An interruption may be created when this bit is turned ON. This bit is not set to '1' when the CE panel ONL/OFL switch is set to OFL side.

(27) CHBO (Channel Bus Out): 5A

0	1	2	3	4	5	6	7
CBO0	CBO1	CBO2	CBO3	CBO4	CBO5	CBO6	CBO7
(RCT0)	(RCT1)	(RCT2)	(RCT3)	(RCT4)	(RCT5)	(RCT6)	(RCT7)

These are interface Bus Out signals from the connected channel. This register is set to all '1' when both CH-A and CH-B are not connected or the CE panel ONL/OFL switch is set to OFL. Moreover these bits are all '1's when the SERT signal is '1'. CBO0~7 data is available in preset of the outbound tag (ADO, CMO, SVO, DTO) and represent I/O device address, command code, write data etc.

This register represents position check FTP counter status (RCT0~7) when CMROM (described later) is '1'.

(28) IFSTA (Interface Status of CH-A): 5B

0	1	2	3	4	5	6	7
CUBSA	SPOA	SERA	SYRA	IFONA	ETA	URTO / RTB	URTO2 / URRT

(a) CUBSA (CUB-Send Memory of CH-A)

This bit is '1' when a Short Busy Sequence CUB status is sent to Bus-In and STI is raised) is sent to Channel A. This bit indicates CUB status has been sent or is being sent on CH-A side. This bit is reset when STI signal is generated while CH-A side is linked (RTA=1, OPIA=1) to MTC. This bit is also reset when the power supply is turned ON or when the CH-A side system reset is executed. (SYRT)

(b) SPOA (Suppress Out of CH-A)

This is SPO signal of CH-A side interface. This bit is '0' when CH-A is in DISABLE of the MTC operator panel.

(c) SERA (Selective Reset of CH-A)

This bit is set to '1' when Selective Reset is received from CH-A side while MTC is linked to CH-A. Once set to '1' the status of this bit remains unchanged till a System Reset is received from CH-A or the R-RSTA (described later) bit is set to '1' (Normally UP count mode sets R.RSTA to '1' upon completion of Selective Reset operation). UP count mode is restarted from address '000' once this bit is turned ON.

(d) SYRA (System Reset of CH-A)

This bit is set to '1' when a system reset is received from CH-A. Once this bit is set to '1' it will not be reset till the R.RSTA (described later) bit is set to '0'. If MTC has linked to CM-B upon receiving System-Reset from CH-A, SYRA bit will not be set till MTC has been released. When this bit is set to '1', UP count mode is restarted from address '000'.

(e) IFONA (Interface ON of CH-A)

This bit is '1' when the CH-A side interface switch of MTC operator panel is in Enable. The driver/receiver circuits on the CH-A side interface is not active when this bit is '0'. Moreover this bit will also be set to '0' if CE panel ONL/OFL switch is set to OFL side. This bit is turned OFF ('0') upon completion of the operation being executed if the interface switch is changed to DISABLE.

(f) RTA (Root A), RTB (Root B)

MTC may have two channel interfaces. Here RTA, RTB signals are used to indicate the logical interface status of the Channel interface and MTC. Now RTA signal is '1' if MTC is linked to A side channel, while RTB is '1' if MTC is linked to B side channel. Both RTA and RTB signals are '0' when MTC is in neutral status, that is not linked to any interface. Now RTA and RTB signals are reset to '0' by the SYRT signal.

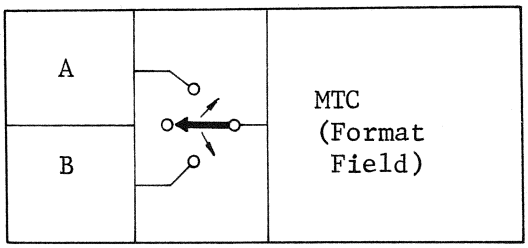


Figure 4.19 2 Channel Switch Concept

(h) URTO1, URTO2 (Unconditional Reset Out)

When both WRTO1 and URTO2 bits are set to '1', UR reset request is generated for another MTC. At this stage the URRT bit is set to '1'. This bit can not be set to '1' while MCY is OFF.

(i) URRT (Unconditional Reset)

This bit, '1', indicates that there is a UR reset request from another MTC or from its own MTC (URTO 1/2 are set to '1' for this purpose).

(29) INTAG (Channel-In Tag): 5C

0	1	2	3	4	5	6	7
OPI	M.ADI	M.SVI	M.STI	RQIAF	RQIBF	DSI	DCN

(a) OPI (Operation-IN)

It is employed as OPI signal for the linked channel. When this bit is set to '1', MTC and channel will be linked. This bit may be reset directly or is reset if Select Out is released and if EBOP bit is '1' (this bit is described later). This bit may also be reset by the SERT signal and disconnect request (DCN=1).

(b) M.ADI (Microprogram Address-IN)

This is an ADI signal for the channel. This bit may be set to '1' only if OPI bit is also '1'. In this case I/O device address must be stored in CHBO register. This bit may be reset ('0') by UP count mode. It may also be reset by the SERT signal and disconnect request (DCN=1).

(c) M.STI (Microprogram Status-IN)

This is an STI signal for the channel. This bit ('1') resets the CUBSA, CUBSB bits described earlier. This bit may also be reset by the SERT signal or by a disconnect request.

(d) M.SVI (Microprogram Service-IN)

This is an SVI signal for the channel. As SVI signal for data transfer is generated in the internal circuit, this bit has to be reset to '0' in such cases (when DTF0, DTF1 bits are '1'). This bit may be reset by the SERT signal or by a disconnect request.

(e) RQIAF (RQI Flag for CH-A)

RQI signal is caused to the channel interface when this bit is 1. This signal is however suppressed by the SPO signal on CH-A side when RQSPE bit is '1'. This bit is reset by the SERT signal or a disconnect request.

(f) RQIBF (RQI flag for CH-B)

This is a RQI signal for CH-B side. For further details refer to RQI AF.

(g) DSI (Discount IN)

Disconnect-IN signal for channel interface is caused when this bit is set to '1'. This bit may be set by UP count mode or by PERR (processor error) signals. This bit should be reset by UP count mode in the selective reset routing initiated by SERT signal.

(h) DCN (Disconnect)

This bit is set to '1' when a disconnect sequence occuered. Bits M.ADI, M.SVI, M.STV, RQIAF and RQIBF are '0' when this bit is '1'. Set this bit to '0' to clear DCN bit. This bit is also reset by the SERT signal.

(30) CHBI (Channel Bus-In): 5D

0	1	2	3	4	5	6	7
CBI0	CBI1	CBI2	CBI3	CBI4	CBI5	CBI6	CBI7
(A)	(*B)	(SDI)					

This is a register to send Bus-In signals for the channel. I/O address (with M.ADI bit), status byte (with M.STI bit), sense data (with M.SVI bit), etc. may be stored in this register. This register is cleared by SERT signal. CBI0-2 are assigned to Scan Clock A, Scan Clock B and the Scan Data when the SCAN bit is set to '1'.

(31) IFCTL (Interface Control): 5E

0	1	2	3	4	5	6	7
R.RSTA / OVRN2	S.BCT / *XTAG	SHBC / DXFE	S.UCT / DXRQ	S.DCT / BIBSY	CTSTP / *ABRPC	R.RCT / *BOPC	R.CRY / C.RCT

(a) R.RSTA (Reset RSTA)/OVRN2 (over-run 2)

Setting this bit to '1', the above mentioned signals SERA, SYRA are reset ('0'). They should be reset upon completion of selective reset or system reset operation. The OVRN2 signal is turned ON if overrun is detected in data transfer in offset interlock mode (refer to section 4.7.2).

(b) S.BCT (Set Byte Counter)/*XTAG (No Transfer Tag)

Setting this bit to '1', content of the CHBI register is preset in the upper 8 bits of the 12 bit byte counter. Now '1' is entered in the lower 4 bits. If SHBC is '0', the CHI7 bit correspond to 2^4LSB. If SHBC is '1' (described later), the CBI7 bit corresponds to 2^0 LSB. In the case the byte counter becomes an 8 bit counter and is capable of counting upto 255 bytes.

This function may be employed only if MTC is in offline status. *XTAG '1' indicates that in-tag and out-tag signal for data transfer to and from the channel have not been generated. Those signals are SVI signal (service in), DTI (data in) signal and SVO (service out), DTO (data out) signals respectively.

(c) SHBC/DXFE (Short Byte Counter/Data Transfer End)

SHBC is employed to make the byte counter act as 8 bit counter.

DXFE signal is provided to indicate any data transfer with format circuit has finished. This signal is set to '1' by 'SIOP' (CMO=1), DISCONNECT from CH linked to the MTC or by the carry from the above byte counter (in case of MTC offline). DXFE is '0' when MCY is turned OFF.

(d) S.UCT/DXRQ (Start Up Count/Data XFR Request)

Setting this bit to '1', the Position Check FTP counter starts counting FTP in UP count mode.

DXRQ is a data transfer request signal from the formatter circuit. Now DXRQ=1 indicates that SFR buffer is not full (when DTFO=1) or data is still left in SFR buffer (when DTF1=1).

If both DTFO and DTFI are '0', DXRQ is '0'. It may also be '0' if IHDRQ bit is '1'.

(e) S.DCT/BIBSY (Start Down Count/Bus In Busy)

Setting this bit to '1', the Position Check FTP counter start counting FTP in Down Count Mode.

BIBSY is '1' if the data stored in CHBI register does not move to XFR buffer data from up to the XFR buffer is stored (Via CHBI Register). MP should confirm that BIBSY=0 before setting the next data in CHBI register.

(f) CTSTP/*ABRPC (Counter Stop/No A,B Register Parity Check)

The Position Check FTP counter is stopped when CTSTP is set to '1'. *ABRPC is set to '0' if a parity check has detected in A and B registers during data transfer from MTC to the channel. Once set to '0' it remains in this status till MCY is turned OFF. This bit, '1', indicate that parity error was not detected in A or B registers during data transfer from MTC to CH.

(g) R.RCT/*BOPC (Reset Reposition Counter/No Bus Out Parity Check)

R.RCT is set to '1' to clear position check FTP counter to all '0's. *BOPC is '0' if a Bus Out parity error has detected in data transfer from the channel.

Once set to '0', *BOPC remains in this status until MCY is turned OFF. While MCY is OFF, this bit is '0' if there is a parity error in the Bus-Out data and is 1 if no parity error is found in the Bus Out data.

While MCY is ON, *BOPC = '0' indicates that no Bus Out Parity error has detected during data transfer. While MCY is OFF, it indicates that there is no parity error in the present Bus Out data.

(h) R.CRY/C.RCT (Reset Carry/Carry of Reposition Counter)

R.CRY is set to '1' to reset overflow of the position check FTP counter.

C.RCT is changed to '1' upon detection of carry in the above mentioned counter. It remains in this state till MCY is turned OFF or R.CRY is set. C.RCT is therefore '0' while MCY is OFF.

(32) XFCTL (Transfer Control): 5F

0	1	2	3	4	5	6	7
DXFI	DXFO	MPFD	SCAN	EBOPI	CMROM	ROM2	ROM1

(a) DXFI (Data Transfer In)

Set this bit to '1' for data transfer from MTC to a channel. This sets the data transfer circuit to enable in the required direction. This bit is reset by SERT signal.

(b) DXFO (Data Transfer Out)

Set this bit to '1' to enable data transfer from the channel to MTC. This sets the data transfer circuit to enable in the required direction. This bit is reset by SERT signal.

(c) MPRD (Microprogram Read)

Set this bit to '1' to store MP data to XFR buffer. This bit is reset by SERT signal.

(d) SCAN (Scan Mode)

Setting this bit to '1', all the LSI FFS in the formatter circuit are in serial scan mode. Scan operation is countrolled by CBIO~2 bits described earlier. SCAN function is used with diagnose operations. This bit is reset by SERT signal.

(e) EBOPI (Enable OPI - OFF)

Setting this bit to '1', the OPI signal is immediately reset when 'Select Out' from the channel linked with MTC is released.

If this bit is '0', the OPI signal will remain unchanged even if the above 'Select Out' is released.

(f) CMROM (Command ROM Select)

When this bit is '1', converted command code (CM0~3) is represented in bits 4~7 of the above mentioned TCADA resister (58).

Moreover CHBO register (5A), bits CBO0-7, is represented position check counter output RCT0-7. This bit is reset by SERT signal.

(g) ROM2, ROM1

This bit is used to specify, the conversion table (ROM) for converting a content of the CHBI register (CBI0-7) into CM0-3 code. This bit is reset by SERT signal.

(33) TRAP (Trap Control): 60

0	1	2	3	4	5	6	7
T.INT	T.TMR	T.INS	T.PER	M.INT	M.TMR	M.INS	TMSK

(a) T.INT (Trap by Device Interruption)

This is a DVINT signal from the selected MTU.

(b) T.TMR (Trap by Timer Carry)

This bit represents MTC timer overlfow. Timer stops counting while this bit is ON.

(c) T.INS (Trap by Initial Selection)

This bit is set to '1' when MTC is in ONL status and the channel linked to MTC is requesting an initial selection sequence. (When both address out and select out have been specified simultaneously).

This bit is reset when address out and select out are released or the OPI bit has been set to '1'. This bit is set to 1 for a period of clock when PSSS switch is operated under the following condition:

a) MTC is set to OFL
b) PSSS switch is in data input mode.

(d) T.PER (Trap by Processor Error)

This bit is set to '1' when the PERR signal has become '1' (excluding the case in which MTC is in ROSF mode (ROS function).

(e) M.INT (Device Trap Mask)

Set this bit '1' to enable a device trap. Device trap can occur when the above T.INT='1' and M.INT='1'. This bit is reset by SERT signal.

(f) M.TMR (Timer Trap Mask)

This bit is set to '1' to enable timer overflow trap. This trap can occur when the above T.TMR='1' and M.TMR='1'. This bit is reset by the SERT signal.

(g) M.INS (INS Trap Mask)

This bit is set to '1' to enable an INS trap. This trap can occur when the above T.INS is '1', and M.INS=1. This bit is reset by SERT signal.

(h) TMSK (Trap Mask)

This bit, '1', enables all the microprocessor traps. As soon as a trap is accepted, TMSK signal is reset ('0'). Set TMSK to '1' to enable trap after trap reason has been recognized.

(34) MPERR (Microprocessor Error): 61

0	1	2	3	4	5	6	7
M.RER / RENB	R.PER / OFL	CSPE	REGE	MEC0	MEC1	MEC2	MEC3

(a) M.RER (Mask Register Error)/RENB (Register Enable)

The RENB bit is reset ('0') by the reset signal when power supply is turned ON. Parity check is invalid before microprocessor intializes LSR.

MP should initialize all LSRs when power on. After this, set M.RER bit to '1' to validate the above parity check. Once set, RENB is '1', and may not be reset unless power supply is turned off (MP cannot reset RENB).

(b) R.PER (Reset Processor Error)/OFL (Offline)

Setting R.PER bit to '1,' the PERR signal is reset Simultaneously. ALU carry register is also cleared. PERR is caused by CS parity error or LSR read parity error, and also reset by the SERT signal. OFL signal is '1' when the CE panel ONL/OFL switch is set to OFL.

(c) CSPE (CS Parity Error)

This bit indicates a parity error has taken place in CS read. PERR is generated if this bit is '1'. This bit is reset either by the SERT signal or above mentioned R.PER bit CS: control storage where MP is stored.

(d) REGE (Register Error)

This bit represents a parity error detected when MP makes an access to LSR data (after the above M.RER bit has been set to '1'). This generates PERR interruption. The reset condition of this bit is the same as that of CSPE.

(e) MEC0~3

This is the EC level set in MTC.

(35) VFSNS (VFO Sense): 62

0	1	2	3	4	5	6	7
/SINH	/SP2	/F.C=S	/M	/SM7	/VFOH	/VFOM	/VFOL

(a) SINH (Start Inhibit)

This bit is '1' when SINH function in CE panel MP control is selected from CE panel.

(b) SP2 (Spare 2)

This bit is '1' when SP2 function in MP Control is selected from CE panel.

(c) F.C=S

'1' when address compare is successful.

(d) M

Normally this bit is '0'.

(e) SW7

This bit is '1' when the CE panel switch 7 is ON.

(f) VFOH/VFOM/VFOL

These three bits select the VFO processing mode.

Table 4.25

VFOH	VFOM	VFOL	Available Speed Mode			
			200	125	75	50
0	0	0				0
0	0	1			0	0
0	1	0		0		0
0	1	1		0	0	
1	0	0	0			0
1	0	1	0		0	
1	1	0	0	0		
1	1	1	-	-	-	-

0 ... available

(36) FID (MTC Function ID): 63

0	1	2	3	4	5	6	7
/FID0	/FID1	/FID2	/FID3	/FID4	/FID5	/FID6	/FID7

This register indicates the function selected for MTC.

FID0 : Normally set to '0'.

FID1 : '1' when No IB-Retry.
Specifies the retry function in case of IB write error.

FID2 : '1' when No Gap Length Addition.
If this bit is '0', the IBG length is increased by 0.03 inch in GCR write processing.

FID3 : '1' when IBM mode NRZ.
When this bit is '1' along with CPBL bit, data block which comprises less than 6 bytes of data is allowable in NRZ Read/write operation.

When this bit is '0', such a data block will be processed as noise.

FID4-7: Reserved.

(37) TCADB (MTC Address for CH-B): 64

0	1	2	3	4	5	6	7
/CADB0	/CADB1	/CADB2	/CADB3	/CADB4	/(SP7)	/(SP8)	/SHARB

This register specifies the MTC address for CH-B. All other explanations are the same as in section (25) on TCADA. This register is set to all '0's unless the optional 2-CH SW is mounted.

SP7, SP8 and SHARB represent setting unit output.

(38) IFSTB (Interface Status for CH-B): 65

0	1	2	3	4	5	6	7
/CUBSB	/SPOB	/SERB	/SYRB	/IFONB	/OPOB	/"0"	/2CHSW

(a) CUBSB (CUB Send Memory for CH-B)

(b) SPOB (Supress Out in CH-B)

(c) SERB (Selective Reset in CH-B)

(d) SYRB (System Reset in CH-B)

(e) IFONB (Interface On in CH-B)

(f) OPOB (Operational-out in CH-B)

These are provided for CH-B. All other explanations are the same as that for CH-A (item 28).

(g) 2CHSW (2-CH Switch)

This bit is '1' when the 2-CH SW option is equipped. Registers with addresses 64~70 are valid only if this bit is '1'.

(39) RTSNS (Root Control Sense): 66

0	1	2	3	4	5	6	7
/INHA	/INHB	/*BUSE	/BFRE	/RQIB	/"0"	/SINHB	/GINHA

These signals are provided for channel interface switching. Refer to Subsection 4.6.6.

(40) RTCTL (Root Control): 67

0	1	2	3	4	5	6	7
DSOKA	DSOKB	CRVA	CRVB	S.SW / SW	R.USE / *USE	R.RSTB /	

(a) DSOKA (Disable OK for CH-A)

This bit '1' is necessary to disable channel A. The IFONA signal may only be reset to '0' if this bit is ON. Therefore MP should set DSOKA only if there is no communication between CH-A and MTC, there is no pending status, when CH-A disable request is received from the operator panel.

(b) DSOKB (Disable OK for CH-B)

Disables CH-B. Other points are the same as DSOKA.

(c) CRVA (Channel Reserve A)

If this bit is set to '1', CH-B response is always 'CUB' status for initial selection. This prevents MTC from being linked to CH-B. This bit is reset by SYRT signal (SYRA) from CH-A.

(d) CRVB (Channel Reserve B)

When this bit is set to '1', CUB status is replied in response from CH-A for initial selection. This prevents MTC from being connected to CH-A side. This bit is reset by the SYRT signal (SYRB) from CH-B.

(e) S.SW (Set Switch)/SW (Switch enable)

Setting S.SW bit to '1', SW signal is changed to '1'. Short busy sequence will not be able to initiate upon receiving an Initial Selection from opposite channel interface, if SW=1 and MTC is linked with current channel interface. None of status being posted to another channel, this channel keeps waiting for completion of current channel working. As soon as MTC has been free with current, MTC links another channel again. Normally, MP should set SW bit when posting CUE status.

SW signal is reset to '0' when initial selection sequence has been initiated with another channel interface.

(f) R-USE (Reset Use)/*USE (No Use)

Setting this bit to '1' when CH-A or CH-B is linked to MTC, the interface is released and MTC becomes free. *USE is therefore normally '0' when either CH-A or CH-B is linked to MTC. This bit is '1' if MTC is not linked to any channel.

(g) R.RSTB (Reset RSTB)

Signals SERB and SYRB are released when this bit is set to '1'. Refer to R.RSTA (31)-(a).

(41) Register Address from 68 to 6F ..... not used.

4.6 Channel Interface Control

4.6.1 Selection

Channel selects MTC by activating Select Out, Select In or Hold Out Channel Interface signal lines. Select Out and Select In are constructed in loop mode. MTC therefore receives one of the these selection signals. This selection is done by priority selection circuit in the MTC Interface Unit (DGCM). For the purpose of explanation it is assumed here that the selection circuit is connected to Select Out. Channel Interface Control Circuit is shown in Figure 4.20. This figure shows the Channel A side. Channel B circuit (2CH-SW option is additional) is the same as that on channel A side. Hereinafter the explanation will be with reference to channel A side.

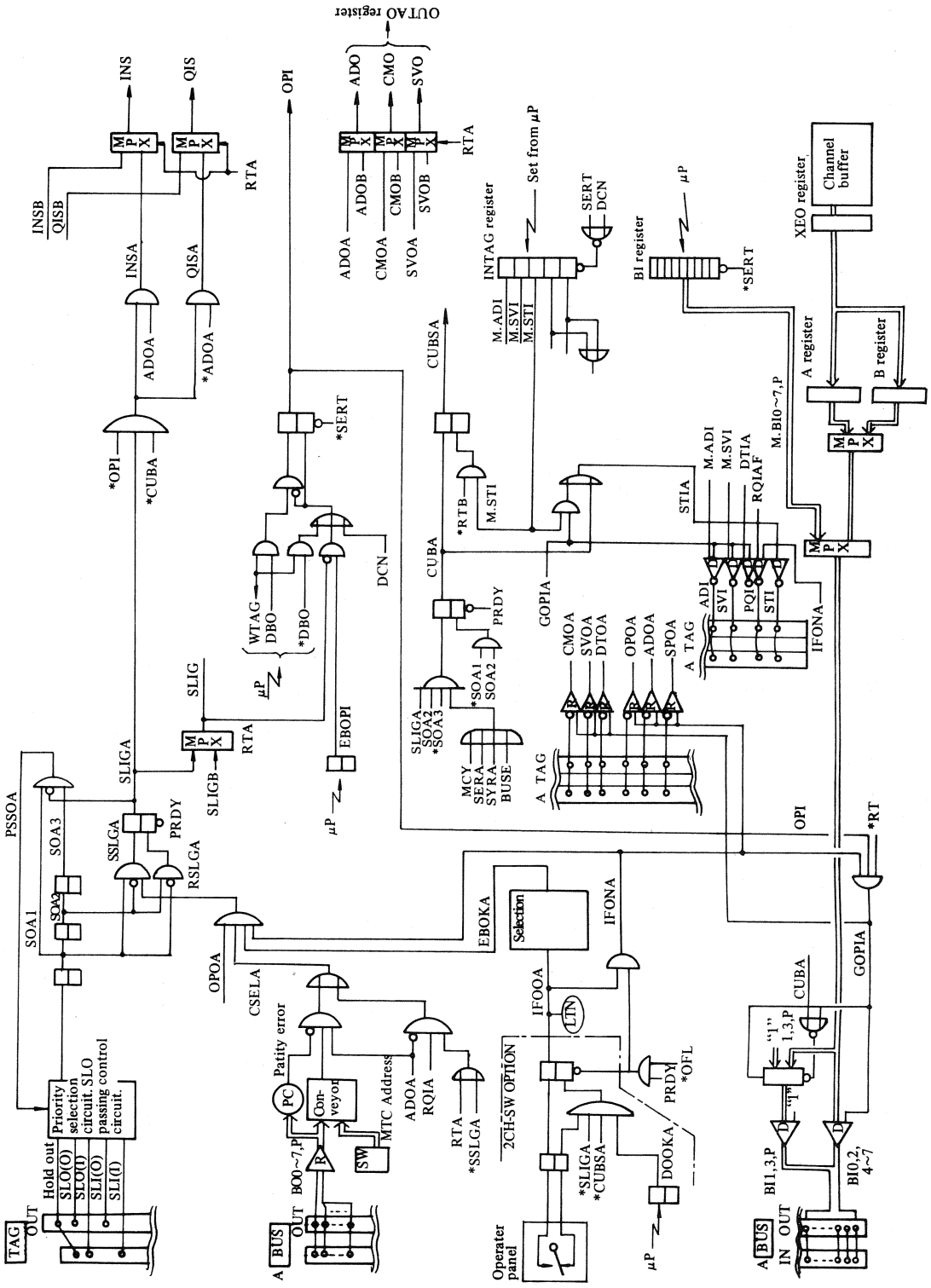


Figure 4.20 Channel Interface circuit diagram

SOA 1, 2, 3 (Selection Out 1, 2, 3) timing signals are generated by INSOA (Initial Select Out A) signal which is itself set by the AND obtained from Select Out and Hold-out signals. (For further details refer to Figure 4.41). Along with ADOA (Address Out A) signal the I/O Address sent out to the BO0~7P (Bus Out 0~7), including the MTC address, are compared at the SOA1 signal rise timing. If the controller address matches, SLIGA signal is set. The SLIGA signal suppresses the PSSOA (Pass Select Out A) and also suppresses the transmission of Select Out Signal to the next control unit. If the control address does not match, the PSSOA signal is generated at the SOA3 signal rise timing and the Select Out Signal is passed to the next control unit. In addition to matching controller address, it is necessary to set OPOA signal (operational out A) from the Channel in order to suppress transmission of Select Out signal after selecting MTC.

IFONA signal indicates that MTC is connected logically to the channel interface. If 2CH-SW option is provided it is reset under one of these two conditions.

(1) Operator panel Interface switch is set to OFF.

(2) The CE panel ONL/OFL switch is set to OFL. (when equipped)

EBOKA signal controls the Select Out signal transmission. MTC is thus selected and SLIGA signal gives rise to INSA (Initial Selection A) signal for initial selection sequence.

This TNSA signal is multiplexed with the INSB signal which represents the beginning of initial selection sequence from the B-interface circuit. When MTC is linked to A-side (RTA signal='1'), INSA generates INS and interrupt to the microprogram.

In the MTC polling sequence, QISA signal is set instead of INSA signal and therefore QIS signal is generated instead of the INS signal. The QIS signal does not generate interruption in the microprogram.

4.6.2 Interface sequence

When the microprogram detects an interruption from INS signal, it sets the OPI bit and activates the selection sequence. The OPI signal enables the intag signal transmission driver for Bus-In 0~7P, Address-In, Status-In etc. and outtag signal receivers for command out, service out signals etc. The Intag signals can be sensed in corresponding INTAG register bits. Ontag signals are multiplexed with the B side interface Outtag signal. At this stage, if RTA signal is ON ('1'), the Outtag signal from A-Side is detected by the microprogram as the Outtag Register Bit. Sensing these INTAG register bits and controlling OUTAG register bits, microprogram proceeds the interface sequence with the channel. Timing chart of this process is shown in Figures 4.21 and 4.22.

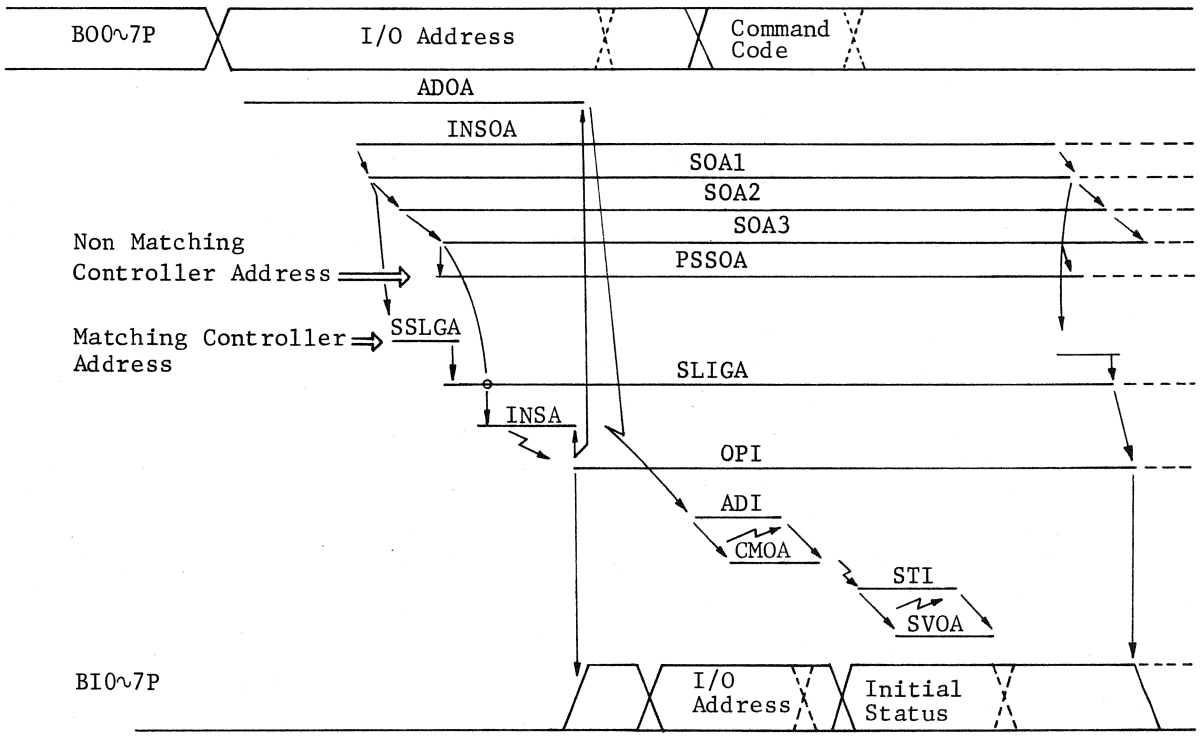


Figure 4.21 Initial selection sequence

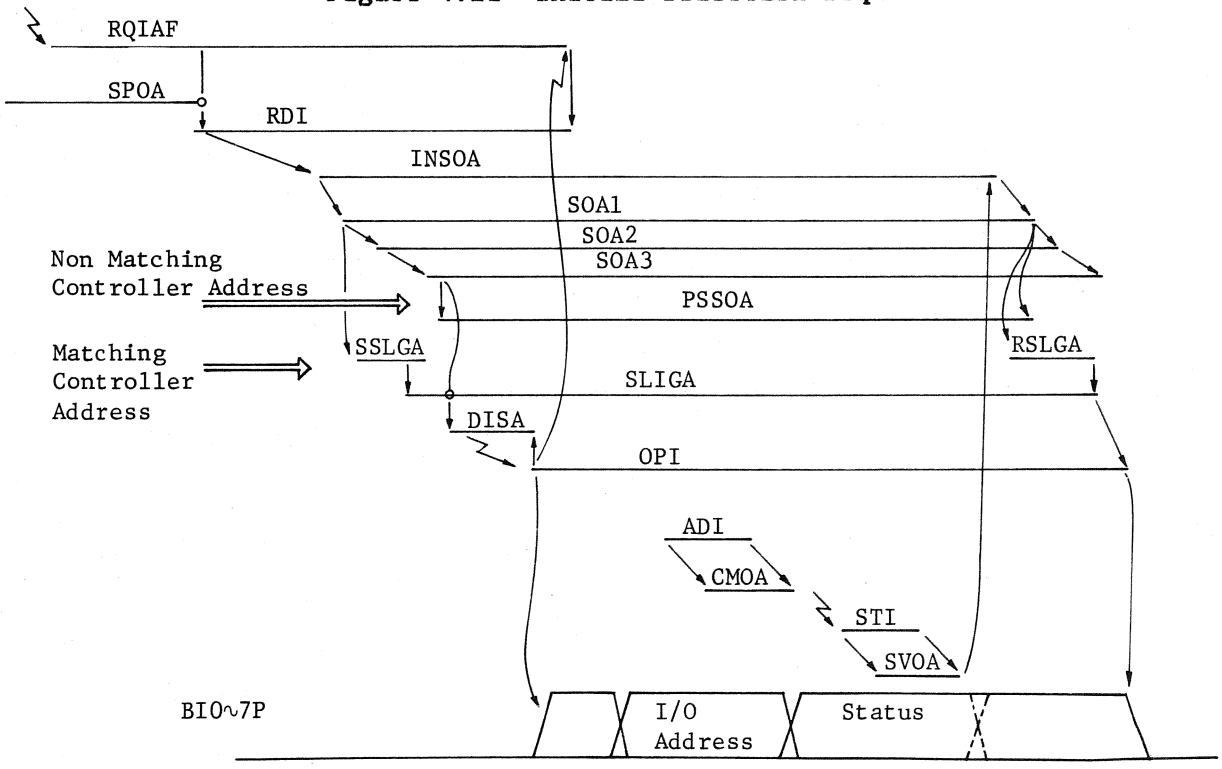


Figure 4.22 MTC polling sequence

4.6.3 Short busy sequence

If the MTC selected by the channel is in the following status, CUB status response is generated in the short busy sequence.

(1) Executing a command operation (MCY='1').

(2) While executing a system reset or selective reset operation.

(3) When 2CH-SW option is equipped and the channel switch is logically linked to the channel interface on the opposite side making the channel interface on this side unusable.

If CUB status response is received in short busy sequence, CUBSA (CUB Status Send Memory A) or CUBSB (CUB Status Send Memory B) signals are set. The signals remain set till the following CUE status. (CUE bit must be included in the first status following the CUB status). The short busy sequence circuit is shown in Figure 4.20. Short busy sequence timing is shown in Figure 4.23.

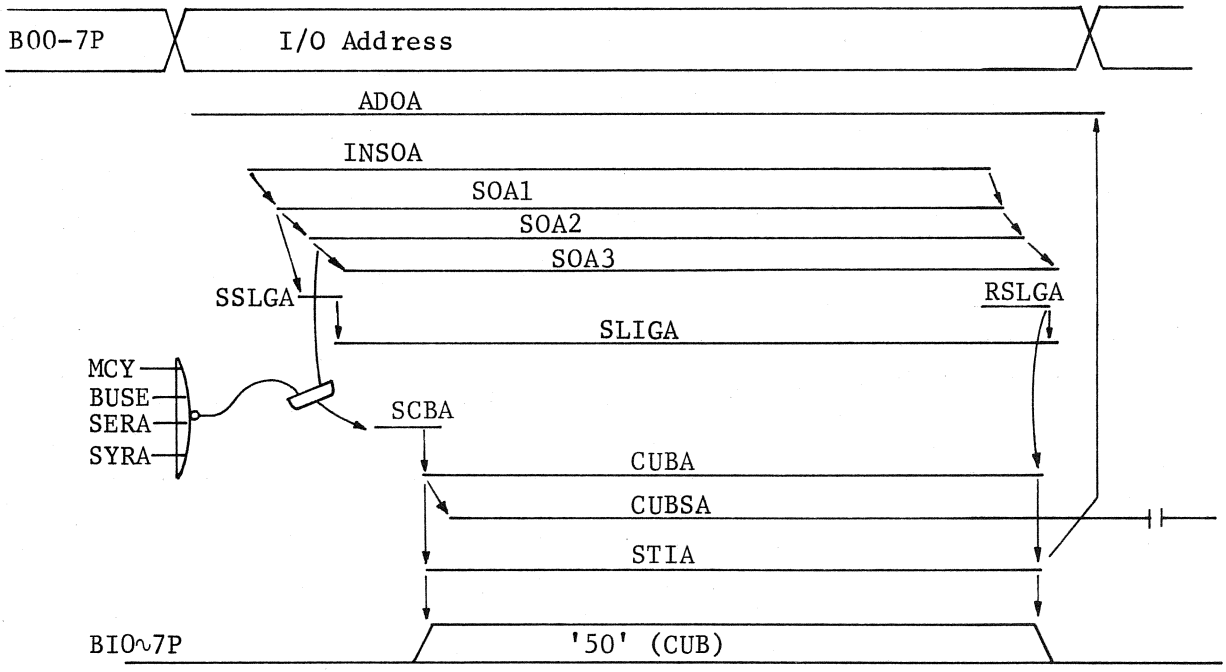


Figure 4.23 Short busy sequence

4.6.4 Interface disconnect

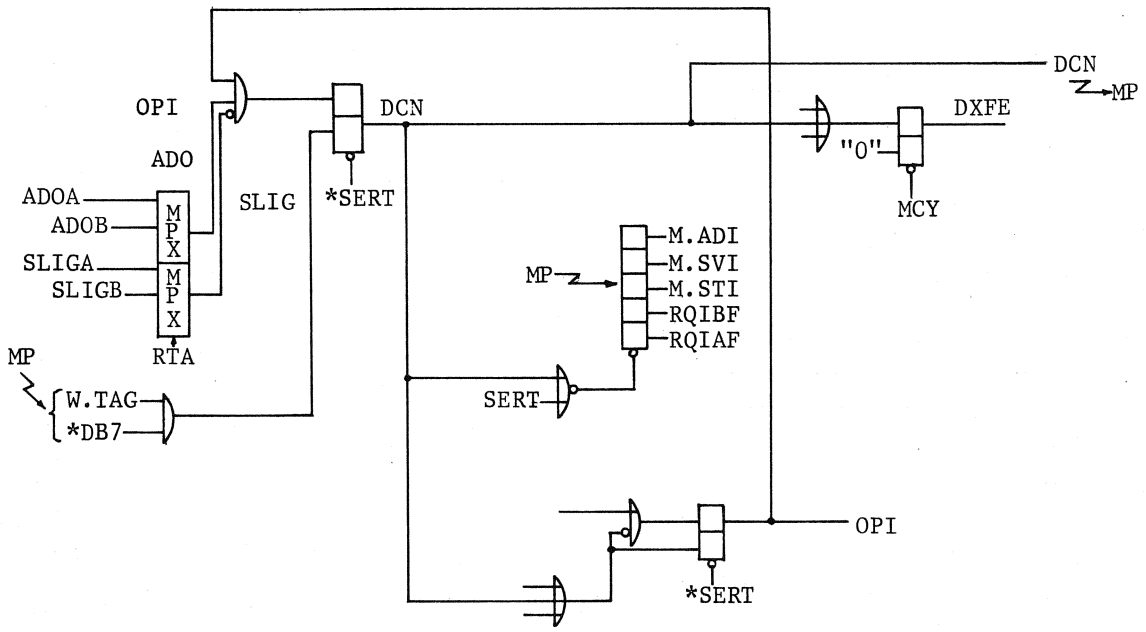


Figure 4.24 Interface disconnect circuit

Interface Disconnect request from the channel is activated when address out is true and select out is false. At this stage, MTC sets the DCN signal (disconnect) as shown in Figure 4.24. The DCN signal sets DXFE (data transfer end) signal, interface register and OPI signals.

4.6.5 Disconnect-In

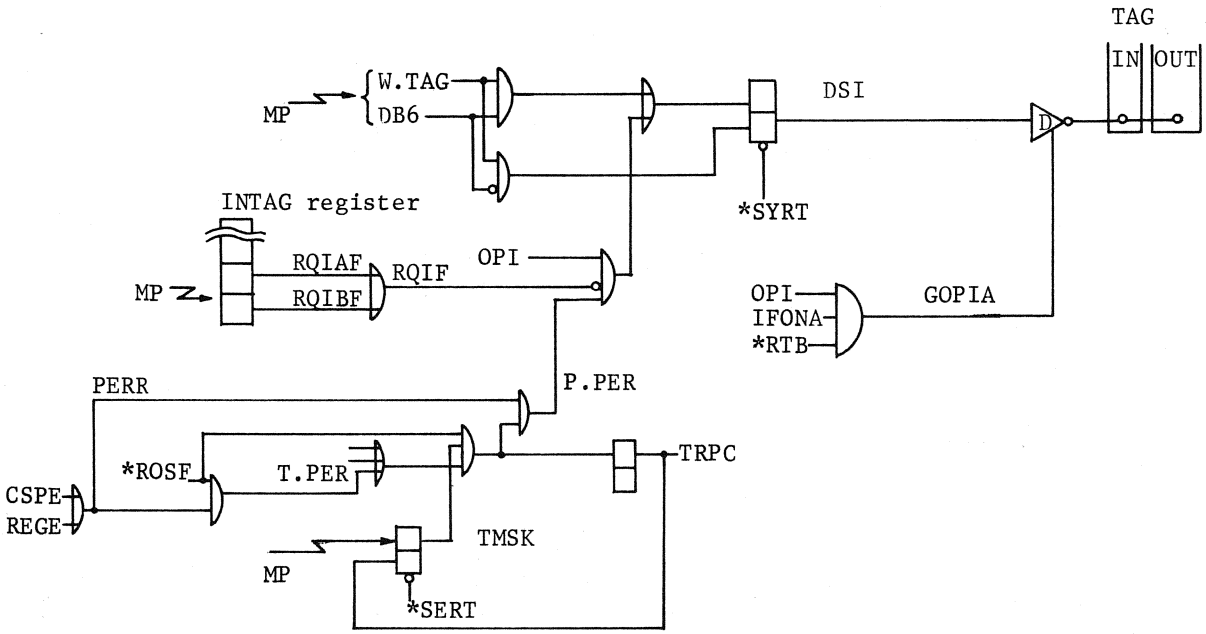


Figure 4.25 DSI signal set/reset circuit

If CSPE (CS Parity Error) and REGE (Register Parity Error) are detected while a channel and MTC are being linked (OPI signal='1'), the PERR (Process Error) signal will be generated. As soon as this PERR signal is generated, DSI signal is set in the microprocessor trap cycle, a Disconnect-In signal is sent to the Channel and error alarm is activated.

If the above signals are detected during operations other than linking or if errors other than PERR error are detected during interface operation, the microprogram sets DSI signal. The DSI signal is reset only by system reset or by the microprogram.

4.6.6 Route control

The route control circuit is provided for logically and dynamically switching between MTC formatter and channel interface circuits. This is only feasible when the two channel switch option has been equipped.

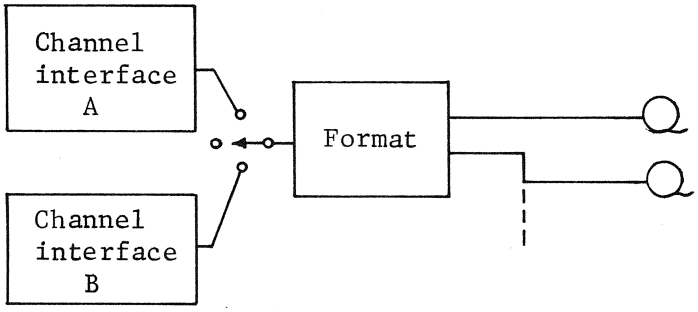


Figure 4.26 Route control

This circuit is placed in the two channel switch option. If this option is not provided, the channel interface switch is permanently set to A-side.

Route control circuit is shown in Figure 4.27. The two channel switch status is identified by RTA (Route A), RTB (Route B) and USE (Use A or B) signals. USE signal indicates the channel interface route has been set and reserved. In neutral status, USE signal is in reset status. If the USE signal is set from either side (SSLGA/B signal and INSA/B signals), the RTA or RTB signal is also set simultaneously. Thus the formatter section and the channel interface section are linked logically and command operation is executed. The microprogram sets RUSE bit if the Route need not be held in its present status upon completion of command operation.

If a subsequent selection request is not received from the channel, the USE signal is reset and the switch is reset to neutral. SW bit is set to suppress CUB status response, if the other channel selection request is received during an MTC start sequence for establishing a channel interface to send CUE status. If the SW bit has been set by the microprogram prior to CUE send sequence, INHB (Inhibit B) or INHA (Inhibit A) signals are set at the time of starting selection for interrupt polling. Now, INHA or INHB signals suppress SSCUB or BUSE signals respectively, and gate CUB status, thus stopping the progress of short busy sequence. The SW bit is reset, when the CUE sequence is completed.

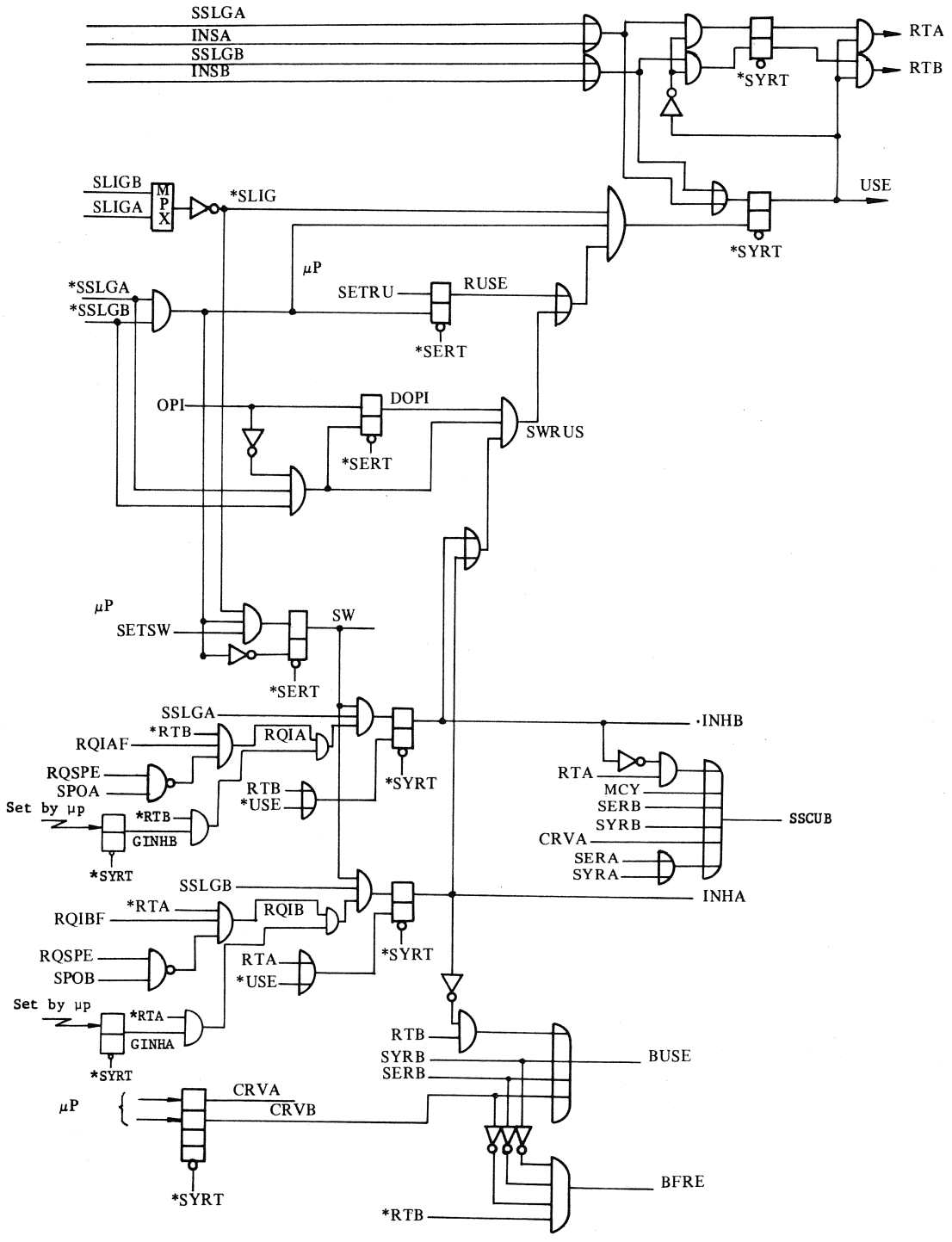


Figure 4.27 Root control circuit diagram

The USE signal is reset at OPI signal fall timing unless there is a request for next selection. At this stage the route is set to neutral status. If there is pending selection sequence on the other side, the channel switch is set to the opposite side and selection procedure is initiated. Then, signals INHA or INHB are reset as soon as the channel switch has been alternated.

CRVA (controller reserve A) or CRVB (controller reserve B) signal is set by the microprogram to reserve the MTC for one of the Channel Interfaces.

4.7 Data Transfer Control

4.7.1 Data transfer control

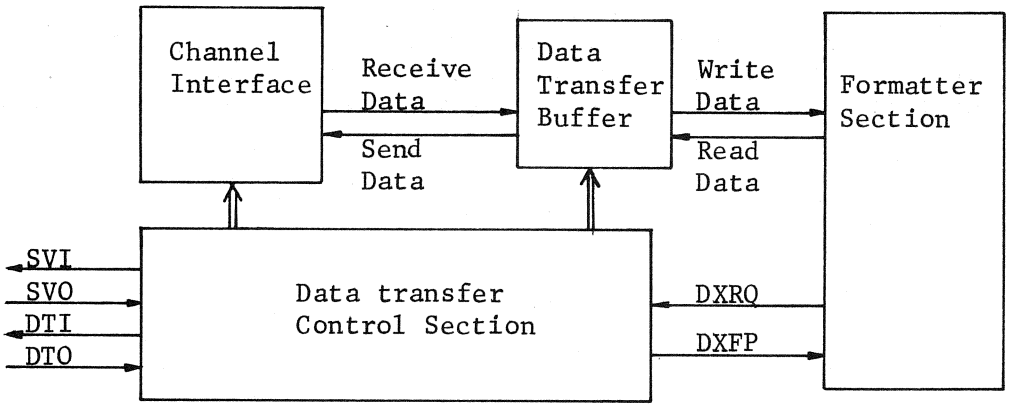


Figure 4.28 Data transfer block diagram

As shown in Figure 4.28, data transfer control section deals with control of data flow; Channel Interface ↔ Data Transfer Buffer ↔ Formatter Section. This control involves SVI (Service In) and DTI (Data In) signal control for the channel interface, and DXFP (data transfer pulse) signal control and DXRQ signal control for the formatter. The direction of data transfer is controlled by the DXF0 (data transfer out) and DXF1 (data transfer in) bits in the XFCTL (transfer control) register. If the former bit is set, data is transferred from the channel to MTC. If the latter is set, data is transferred from MTC to channel. If DXF0 bit is set when formatter section starts Write operation, DXRQ signal is set. Thus, the formatter section requests data to the data transfer control section. The data transfer control section requests a data to the channel by sending SVI or DTI signals, and then transfers the data to the data transfer buffer. Data XFR control section issues DXFP signal to the formatter section to transfer data from the data transfer buffer to the formatter section.

Reading data while DXFI bit has been set, the formatter section sets the DXRQ signal to the data transfer control section to transfer data. Upon receipt of this signal, the data transfer control section transfers data to the buffer along with the DXFP signal, and then issues SVI and DTI signals to the channel to request data transfer. Thus, the data from the data transfer buffer is transferred to the channel by executing the data transfer handshake sequence.

The data transfer section controls data via the transfer buffer. Data flow through the transfer buffer is illustrated in Figure 4.29. Here CL.BO is a timing signal for transfer of data from the channel to Bus Out Register. WTBX (Write Transfer Buffer) is a timing signal for entering data to the transfer buffer. CL.AR (clock for A-Register), CL.BR (clock for B Register) are timing signals for transferring data from the transfer buffer to the A or B register.

If MPRD bit is set, the data set in the M-BI register may be sent to the channel via the transfer buffer. This feature is used to transfer sense data or measuring data in diagnostic functions.

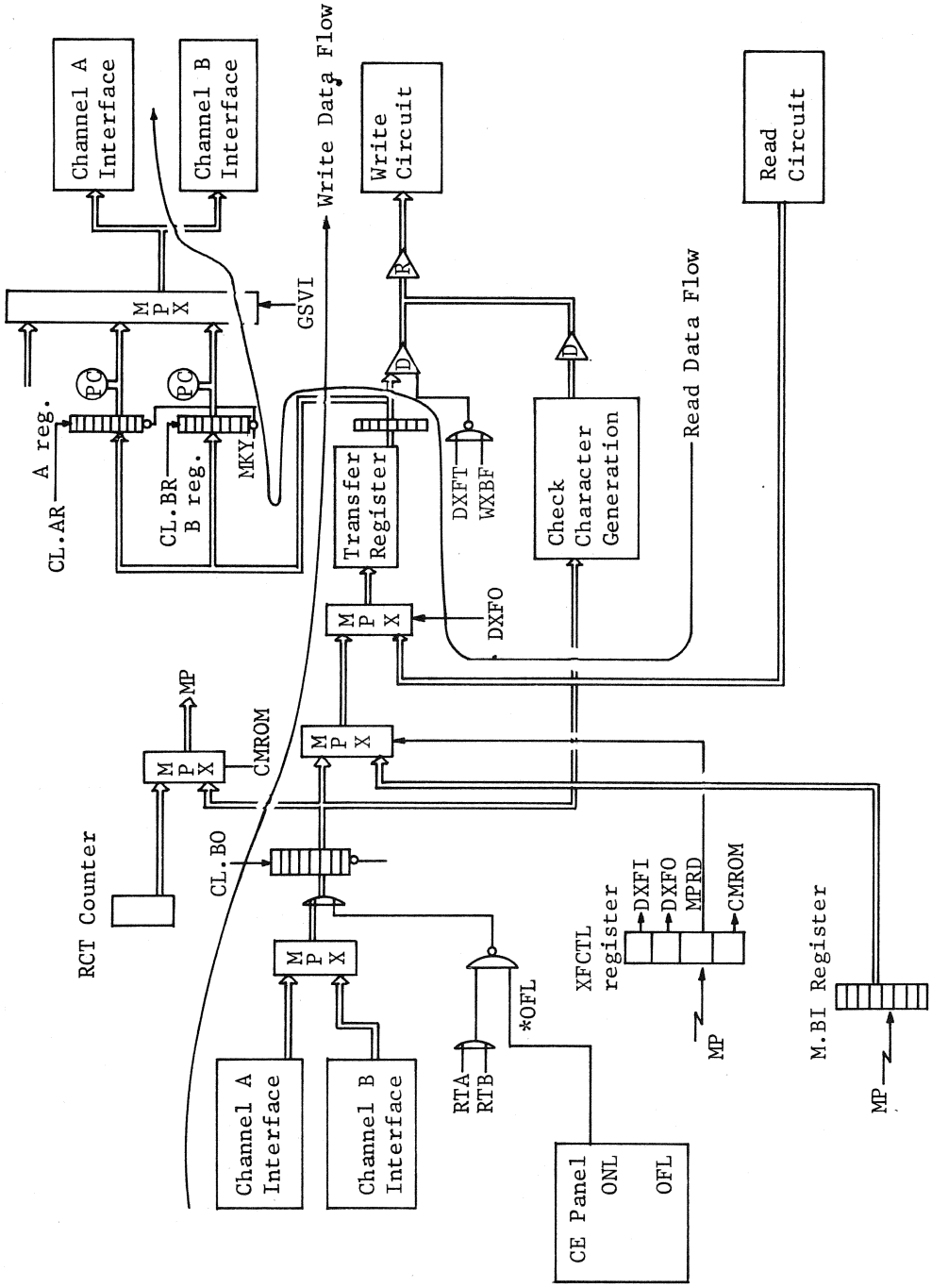


Figure 4.29 Data transfer circuit

SVI (DTI) signal may be reset upon receipt of SVO (DTO) signal from the channel. This is the normal interlock mode. On the other hand SVI (DTI) signal may be reset after a specified delay time even if SVO (DTO) signal is not received. This is called the offset interlock mode. The interlock mode for operation depends on the status of the setting unit. If the length of the cable between the channel and MTC becomes too long, the time required for the signal to travel between them becomes unacceptably long. This results in increased hand shake time and reduced speed. In such cases offset interlock mode is more suitable.

Offset interlock mode may be employed only if the channel features the data streaming function.

4.7.2 Overrun

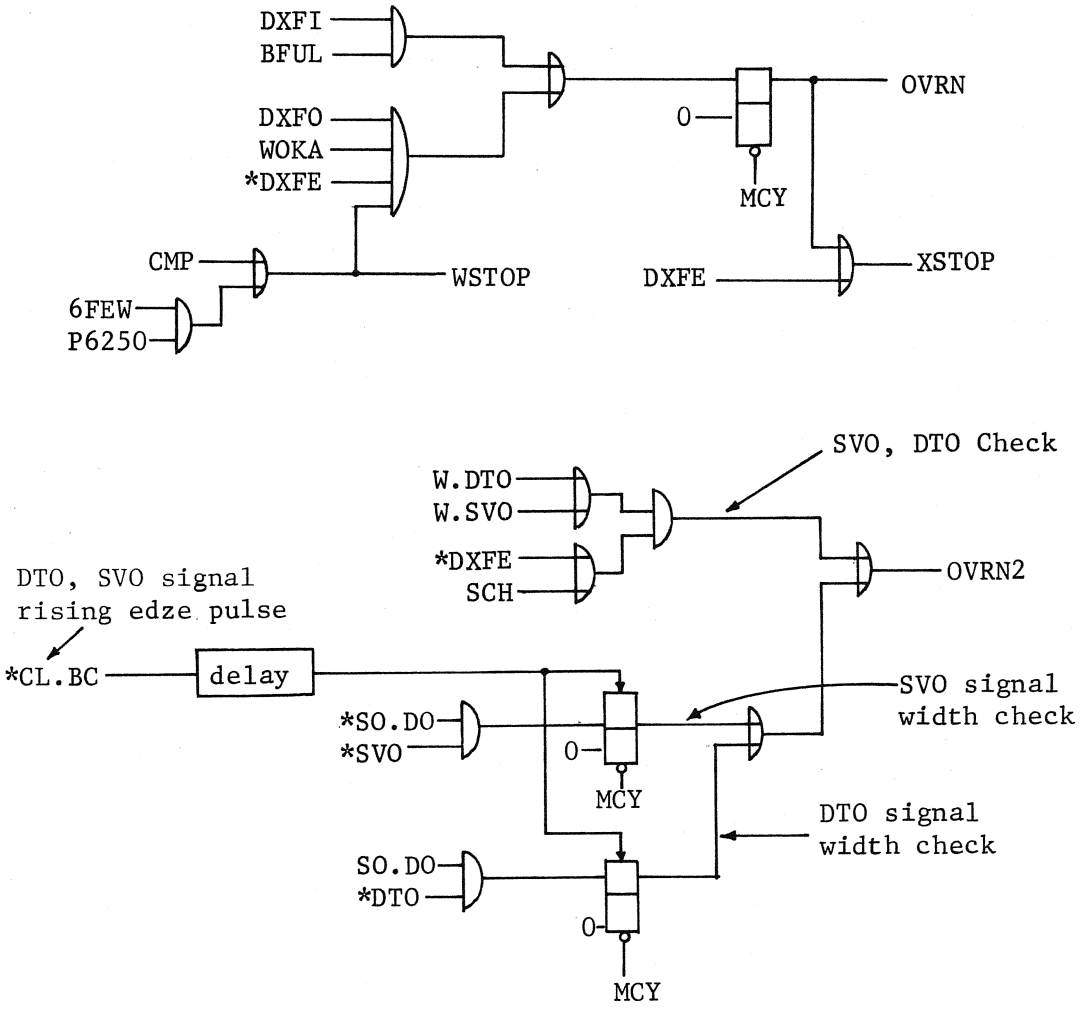


Figure 4.30 Overrun detection circuit

Overrun detection circuit is illustrates in Figure 4.30. The OVRN signal is an overrun signal detected with reference to the data transfer buffer status (refer to section 4.5.2 (16) OVRN signal). The OVRN2 signal is a check signal in the offset interlock mode. Overrun error occurs when a microprogram detects the basic signal upon completion of read or write operations.

4.8 Write Control

4.8.1 Formatter clock

As shown in Table 4.26 the clock cycle of the formatter verying with the tape speed and recording density. The number of clocks per bit cell are 3τ in 6250 mode, 6τ in 1600 mode and 12τ in 800 mode.

Table 4.26 Formatter clock

Speed (IPS)	Mode (RPI)	Full Clock (ns)	Half Clock (ns)
200	6250	184	92
	1600/800	521	260
125	6250	295	147
	1600/800	833	417
75	6250	494	247
	1600/800	1389	694
50	6250	738	369
	1600/800	2083	1042

Timing is controlled by the C and D counters. The relationship between C, D counters and bit cells is shown in Figures 4.31, 4.32 and 4.33. The C-counter is operational during idle scan status also.

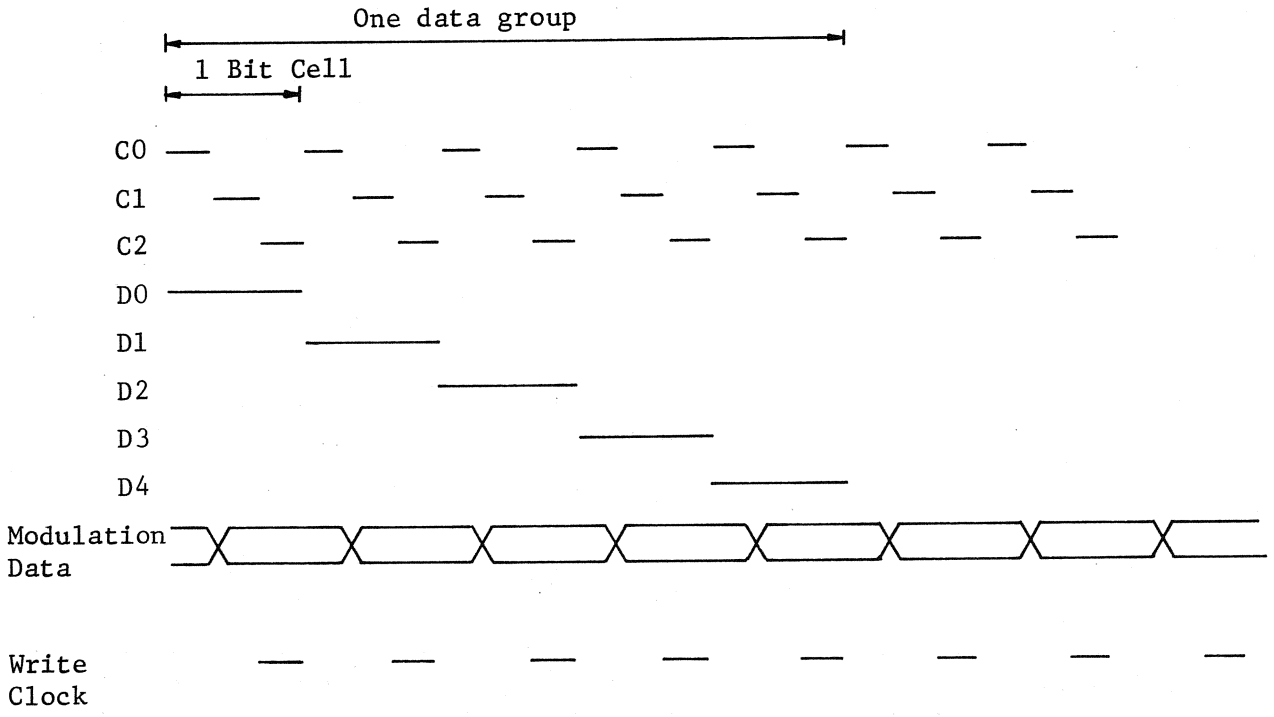


Figure 4.31 C, D counters in 6250 mode

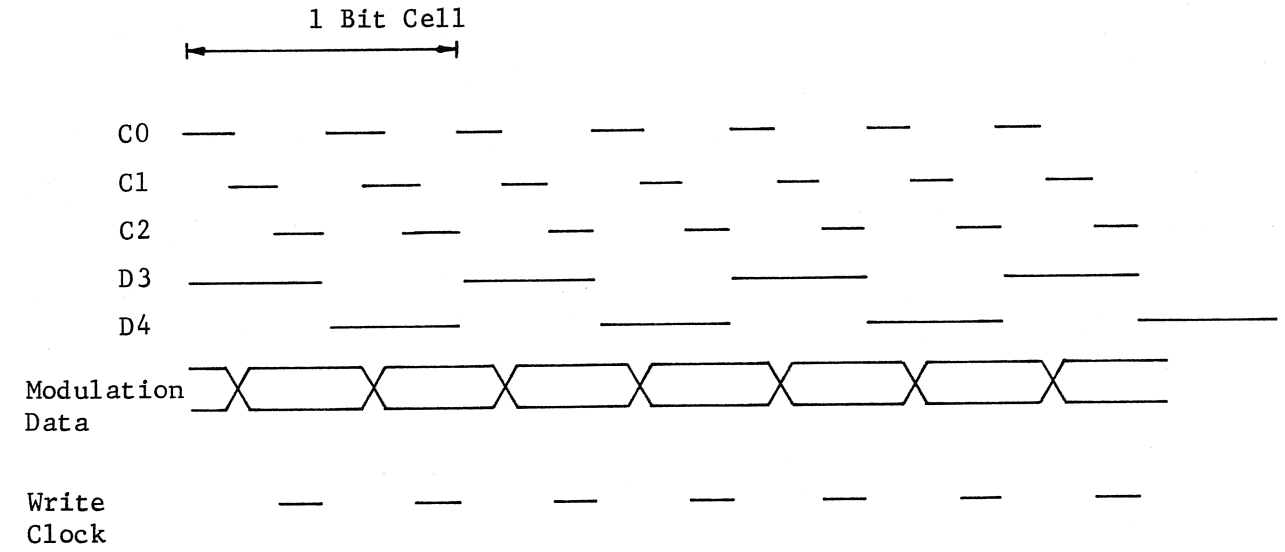


Figure 4.32 C, D counters in 1600 mode

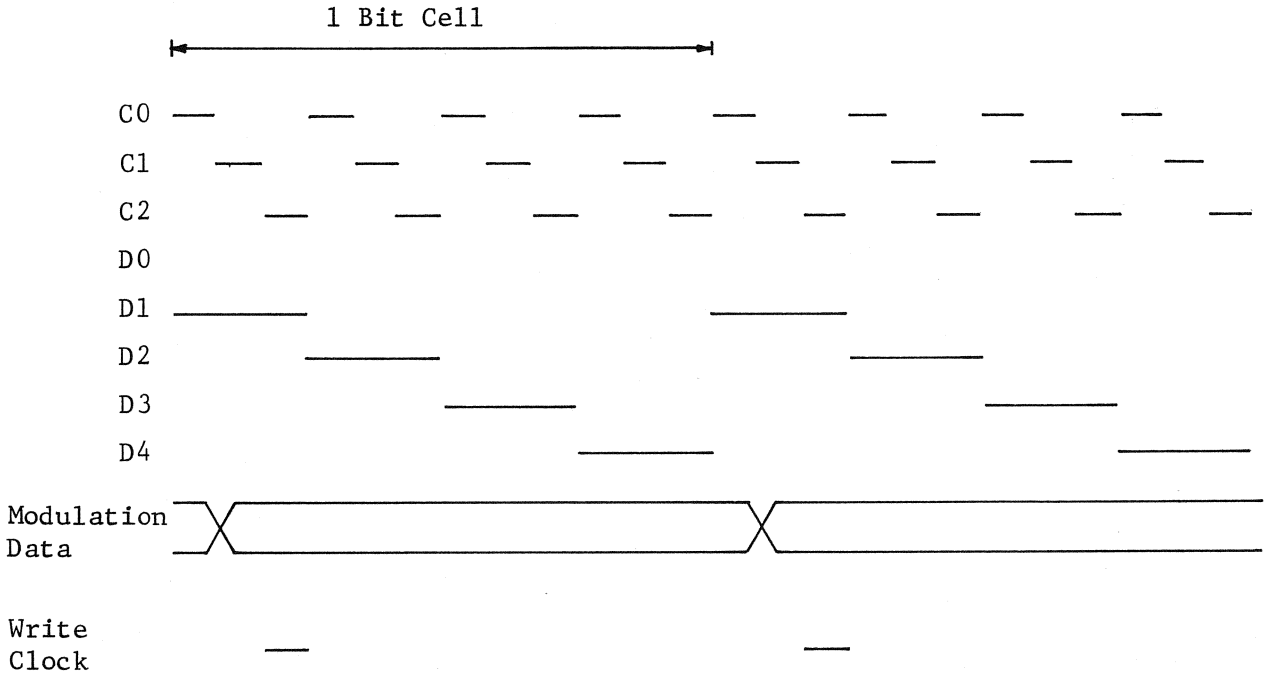


Figure 4.33 C, D counters in 800 mode

4.8.2 Start write operation

Write processing is started when MP sets a Write OK signal (WOKA). As soon as the WOKA signal is set, the WOKD signal synchronized with the formatter clock is set. Now D counter starts as soon as WOKD signal is set. At this stage the format counter starts. The Write format is controlled by this format counter. Now WOKDD signal is set as in D4 (D Counter) timing as follows: FC0 Format in 6250 mode, FC1 in 1600 mode, FC4 in 800 mode. The Write clock sent to MTU is gated by WOKDD signal.

4.8.3 Format control

Write operation of preamble, postamble and data field are controlled by the format counter and the Group Counter used to count data groups.

Table 4.17 Format counter

Format Counter	6250	1600	800
FC 0	TERM	PREA ALL"0" x 1	START
FC 1	SECOND	PREA ALL"0" x 1	-
FC 2	SYNC	PREA ALL"0" x 38	-
FC 3	MARK1	PREA ALL"1"	-
FC 4	DATA GROUP	DATA	DATA
FC 5	MARK2	-	-
FC 6	END MARK	POSA ALL"1"	CRC GAP 1
FC 7	RESIDUAL A	POSA ALL"0" x 1	CRC GAP 2
FC 8	RESIDUAL B	POSA ALL"0" x 1	CRC GAP 3
FC 9	CRC A	POSA ALL"0" x 1	CRC
FC10	CRC B	POSA ALL"0" x 1	LRC GAP 1
FC11	MARK2	POSA ALL"0" x 1	-
FC12	SYNC	POSA ALL"0" x 32	-
FC13	SECOND	POSA ALL"0" x 1	LRC GAP 2
FC14	TERM	POSA ALL"0" x 1	LRC GAP 3
FC15	(WOK RESET)	POSA ALL"0" x 1	LRC

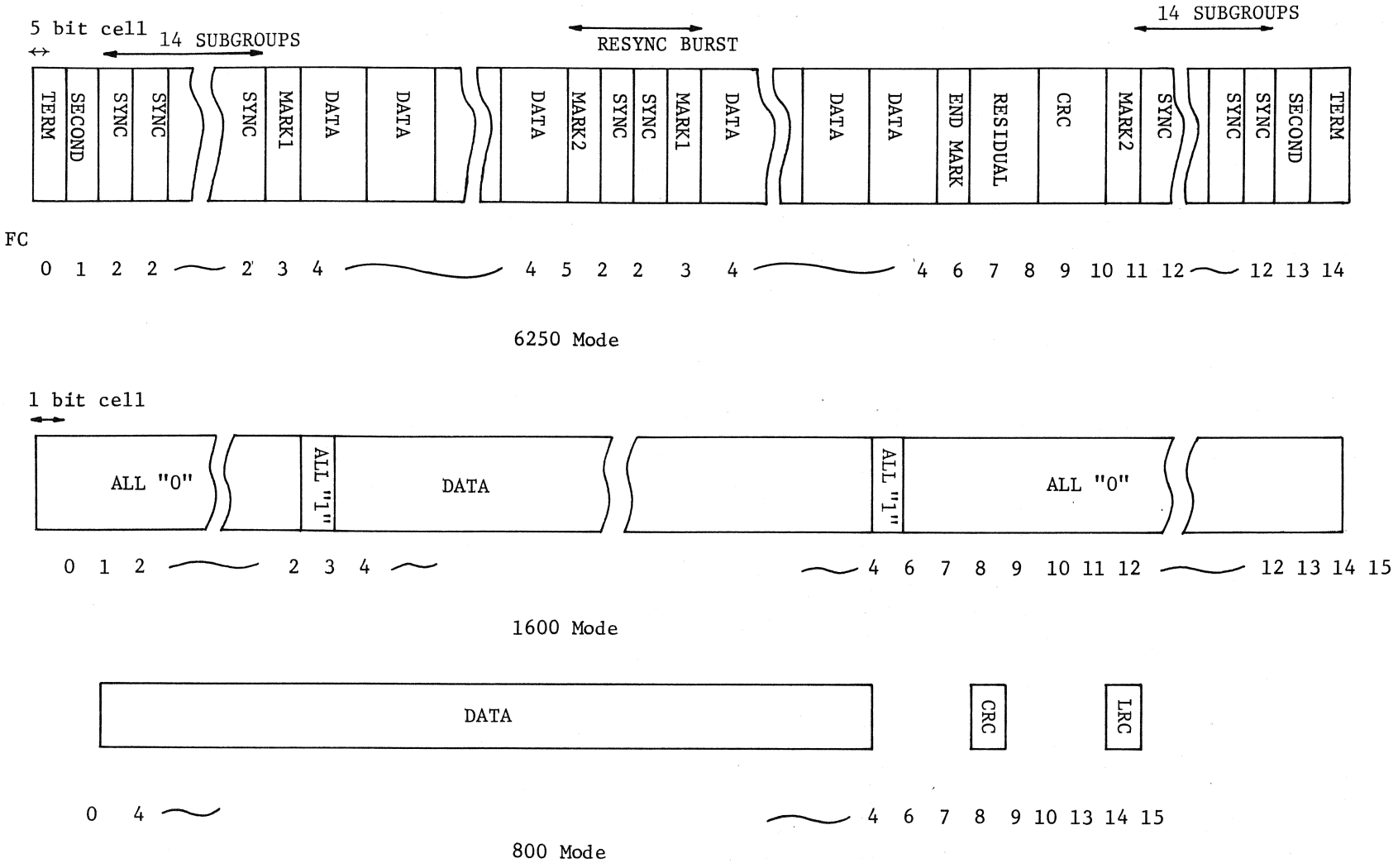


Figure 4.34 Data format

4.8.4 Data bus

The write data received from the channel is entered into the transfer buffer when the WTXB signal obtained by delaying DXFP signal by 1τ is set ON. First DXFO signal is set by the microprogram, and after data is stored in the transfer buffer and the WOK signal is set. Only then the Write operation is started. First preamble is written, and data is read out form the buffer at C2 timing after format counter becomes "4" and RO+1W signal becomes "1". The data read out from the buffer is entered CRC LSI.

In CRC LSI the data passes through Write Bus Multiplexor. Here ECC characters, padding characters etc. are added and is output from the LSI by both direction buses. The relationship between Selector signals WBSL1, 2, 4 on Write Bus Multiplexor and WDAT0~8 signals is shown in Table 4.28.

When WBSL1, 2, 4 are all '1's, CRC check circuit status passes through Write Bus Multiplexor instead of Write Data.

The parity bit of Write data obtained from Write Bus Multiplexor output. This bit is compared with the parity bit from the buffer out register. If they do not match, the Write Bus Out Check signal (WTBOC) is set to '1'.

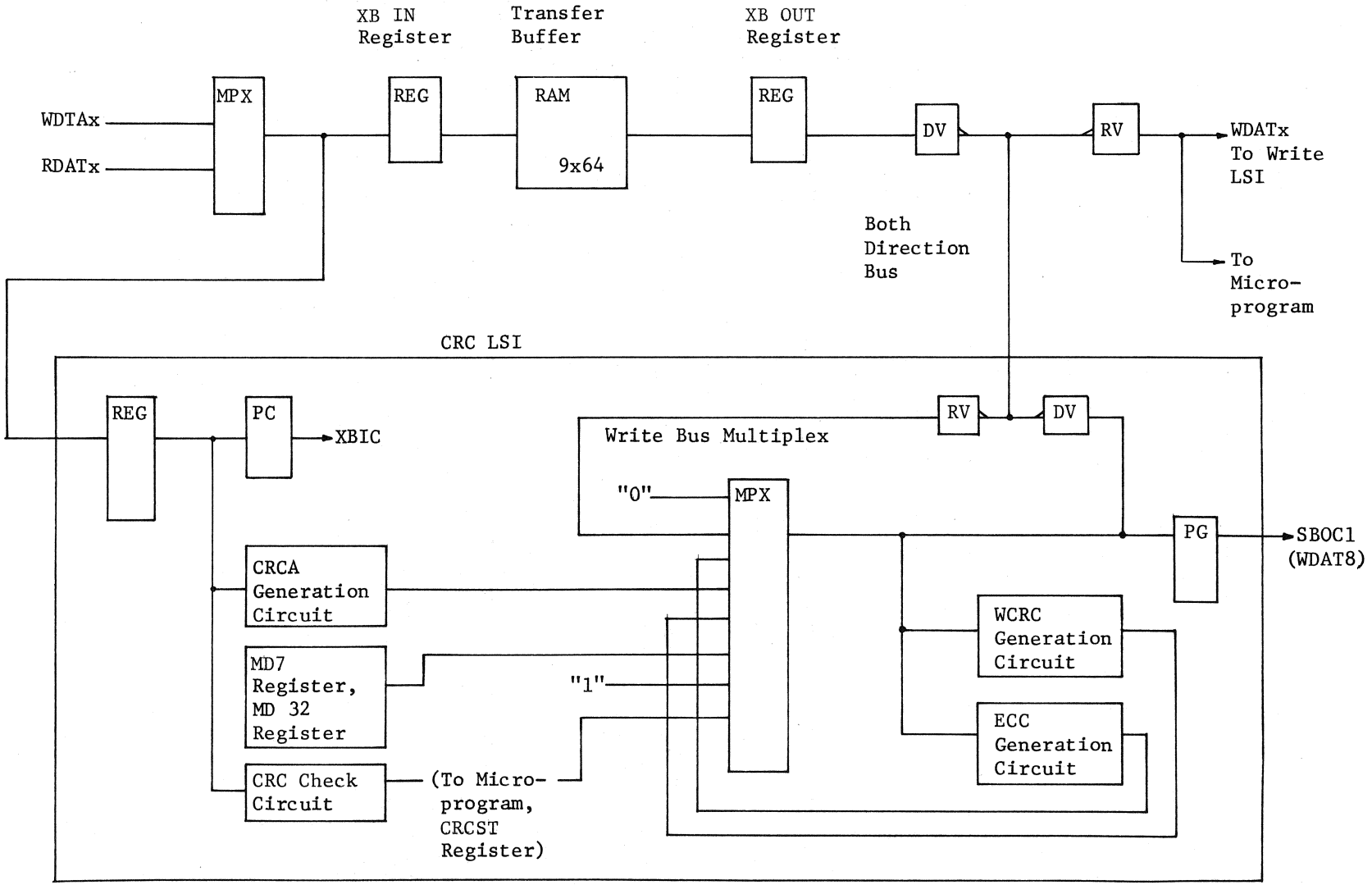


Figure 4.35 Transfer buffer and write bus selection

Table 4.28 Write bus selection

WBSL 421	Input data	WDATX Description
000	"0"	Padding Character
001	XBOx (Transfer Buffer Output)	Data Character
010	ECC Register	ECC Character
011	CRC Register	Aux, CRC Character
100	WCRC Register	CRC Character
101	MD7, MD32 Register	Residual Character
110	"1"	1600 mode Preamble, Postamble All'1's
111	CRC Check Circuit Error	Data Sensed by the Microprogram, CRCST Register

Transfer Buffer input data is subject to parity check in CRC LSI. Parity bit is not generated but bit 8 in channel Bus Out register (CHBO) is entered to the transfer buffer.

4.8.5 Write modulation circuit

In 6250 BPI mode, the data output by Write Bus Multiplexor is fed to WRT LSI. The first four bits, it is one subdata group, are set in the sub-group register. The four bit data is converted into five bits and is set in parallel in the five-bit shift register. The data is then read out serially and fed to the modulation register. The data from the modulation register, it is the JK flip flop, is applied to JK Input to generate NRZ data.

MSEL at signal is set to '1' for writing SYNC, MARK1, MARK2, TERM, SECOND and END MARK. In this case the FM0~4 signal is preset in the shift register instead of 4-5 conversion data.

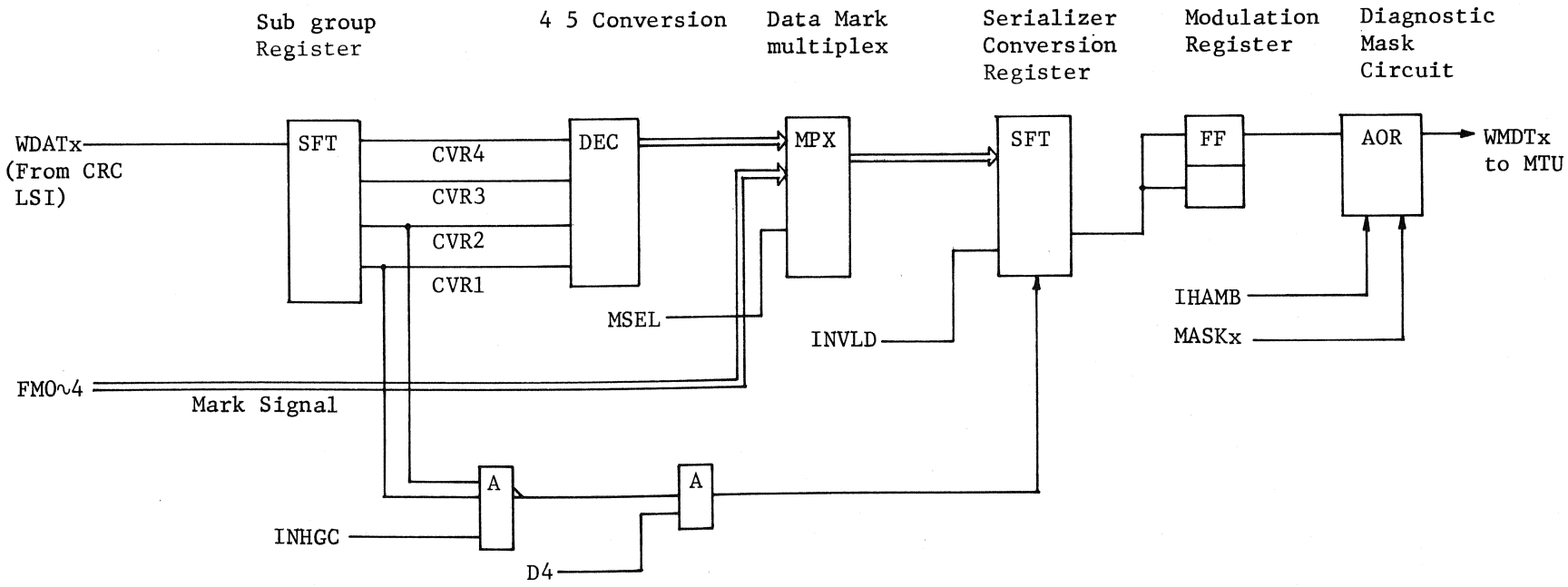
INHGC signal in the data field is set ('1') when DMW mode is specified. At this stage subgroup register bits 1, 2 (CVR1, 2) are also set to '1' simultaneously. All '0' is set in the serializer to inhibit entry of subdata group. If INVLD signal is ON under the above conditions, all '1's is preset and invalid code of all '1's is entered in its subdata group.

When a Mask is specified, modulation register output is gated and all '0's is entered.

If inhibit preamble or inhibit postamble is specified, the IHAMB signal is set to '1' during preamble or postamble processing and the modulation register output is gated as in Mask processing.

In 1600 BPI mode, MSEL signal is set to '1' when the format counter is between 0~2 or 7~15. When the counter 3 or 4 is '1', '1' is set in the lower two serializer bits. MSEL signal is '0' when the format counter is 3, 4, or 6. At this stage the data from Write Bus Multiplexor is set in the subgroup register, bits 3~4 are subjected to PE conversion and are set in the lower two serializer bits (if D4 signal is '1').

In 800 BPI mode, MSEL signal is turned ON ('1') when the format counter is at 6, 7, 8, 10, 13, 14, or 15. At this stage CRC gap, LRC gap '0' is preset in the serializer. When format counter is 4 or 9, the data or CRC Byte from the Write Bus Multiplexor is set in the subgroup register. Bit 4 will be set in the lowest bit of the serializer if signal D4 is '1'. The data in modulation register is entered as LRC byte.


Sub group
Register
4 5 Conversion
Data Mark
multiplex
Serializer
Conversion
Register
Modulation
Register
Diagnostic
Mask
Circuit
WDATx
(From CRC
LSI)
SFT
CVR4
CVR3
CVR2
CVR1
DEC
MPX
SFT
FF
AOR
WMDTx
to MTU
MSEL
INVLD
IHAMB
MASKx
FM0∿4
Mark Signal
A
A
INHGC
D4

4.8.6 Write VRC check

Parity check on Write Modulation Waveform is carried out when the Write Pulse is '1' (WTPL signal) and AL1WT signal is '0'.

In 6250 BPI mode, the 9 track parity at the end of NRZI subdata group (D4 signal = '1') conforms with predetermined conditions. The subdata groups of residual data and CRC data have Odd parity. While the subdata group of the data has even parity. SYNC in the Mark field is a repeatation of Even and Odd parities. Other Mark fields may have uniform parity depending how they are entered.

In 1600 BPI mode, when, when the subdata group of the data is transferred, a check is executed to confirm Odd parity after inverting the phase. At PE Mode, data is '1' when Write Modulation Waveform change to '0' from '1'. So, data '1' is checked to be level '1'.

In 800 BPI mode, only the data field is checked (format count: 4). Odd bytes are at odd parity while even bytes are at Even parity. Now, DEVN signal is set to '1' for odd bytes.

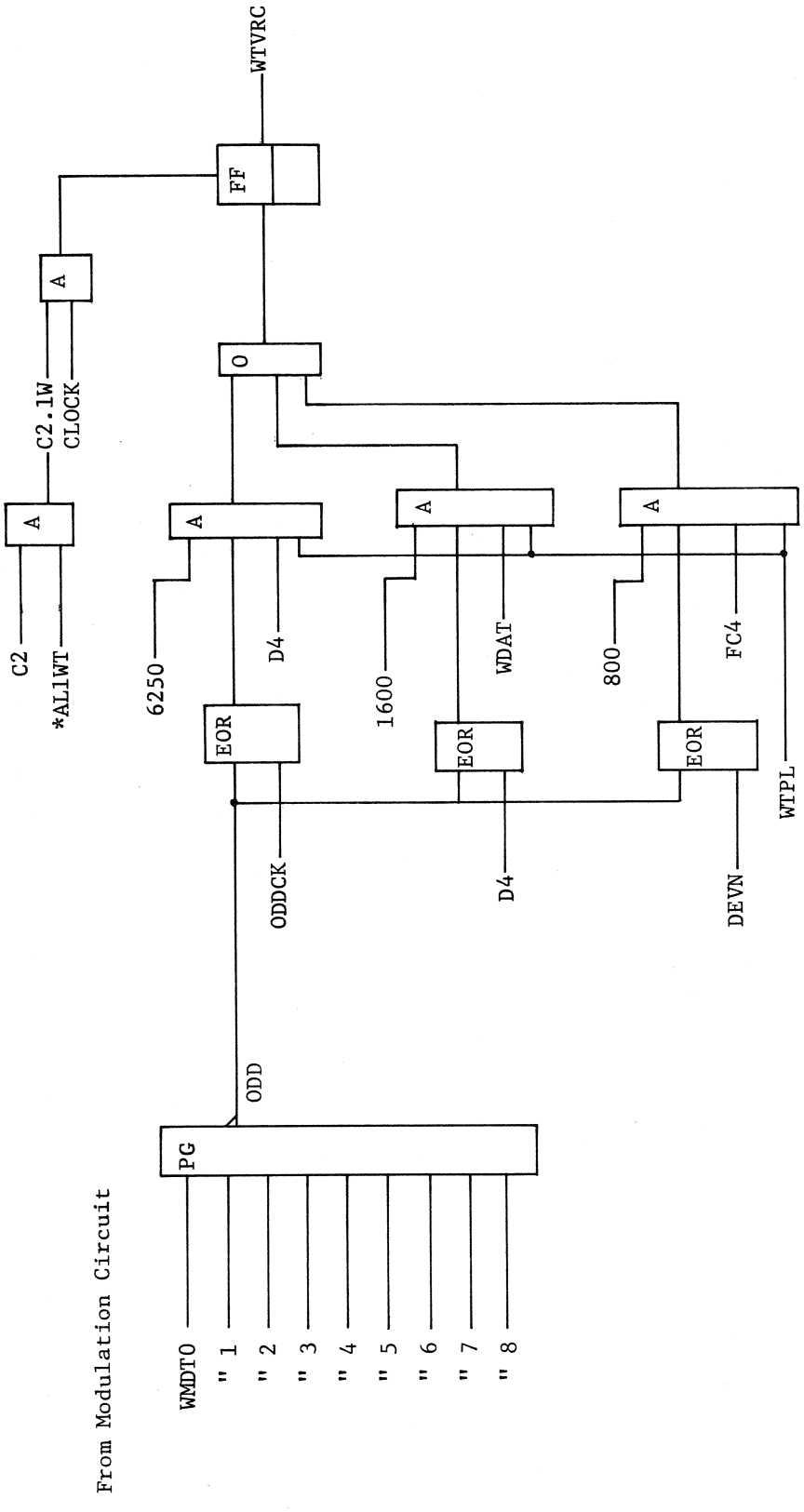


Figure 4.37 Write trigger VRE circuit

4.9 Read Control

It will be described in this section to operation of Read command, Read Back ward command and Read after Write Check of Write command. The Bus In Data (CVBI0~8) passes through the analog circuit, and is converted into Modulated Data (DEMD0~8), Read Clock (SRIC0~8) Phase Error (PHER0~8) and Beak Bulse (PEKP0~8) signals respectively.

As shown in Figure 4.38, these signals are transfer to Read Circuit, it is beto blocks, check format, modulate datas, check datas and error correction.

Mark detection circuit, Skew detection circuit and 5-4 conversion circuit correspond to three tracks each and are made up of 3 LSIs.

Pointer circuits are made of three LSIs (3 tracks) while the error correction and detection circuits consist of one LSI each.

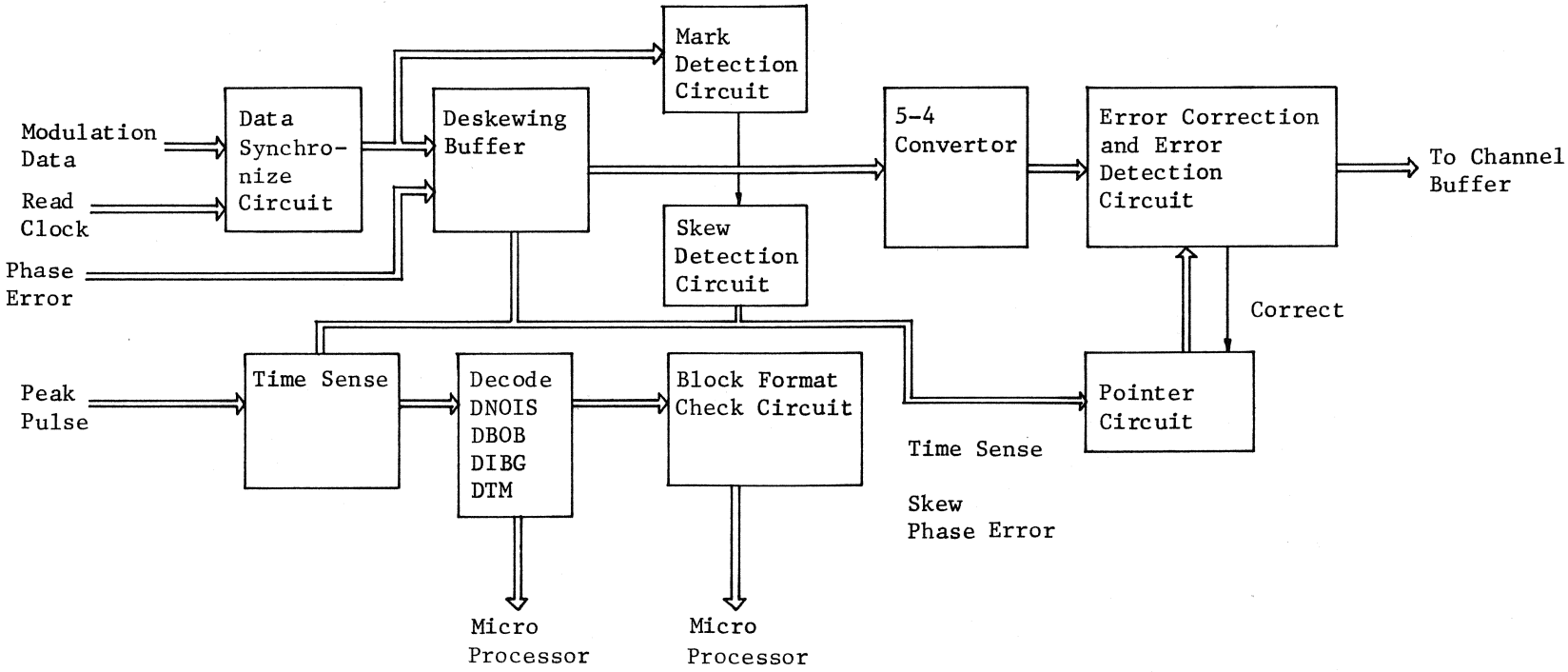


Figure 4.38 Read block diagram

4.9.1 Time sense

As soon as the Read OK signal (ROK) is set, the Peak Pulse signal (PEKP0~8) which is the differential signal from Bus In data (DVBI0~8) is generated. In 6250 BPI mode, if the peak pulse is detected for ten bit cell period, Time Sense signal is set (TSNS0~8). On the other hand, if the peak pulse is not detected for 5 bit cell period, the time sense signal is reset. In 1600 BPI mode the time period for setting sense signal is 5 bit cells and for resetting it is 2.5 bit cells. The time sense values of each tracks are decoded to generate Clock detection (DBOB), IBG detection (DIBG) or Tape Mark Detection signals (DTM). Signal detection logic is shown below in the form of a logical equation.

0 to 8 in following formula means TSNS0 to TSNS8.

DBOB = (4.1.3+6.2.7+0.8.5).(4+1+3).(6+2+7).(0+8+5)

DIBG = $\overline{0}.\overline{1}.\overline{2}.\overline{3}.\overline{4}.\overline{5}.\overline{6}.\overline{7}.\overline{8}$

DTM (For Write) = $0.\overline{1}.2.\overline{3}.\overline{4}.5.6.7.8$

DTM (For Read in 1600 BPI mode) = $\overline{1}.\overline{3}.\overline{4}(2.6.7+0.5.8)$

DTM (For Read in 6250 BPI mode) = $1.3.4\{2.6.7.(0+5+8)+(2+6+7).0.5.8\}$

DARA (For Write) = $\overline{0}.1.2.3.\overline{4}.5.6.7.\overline{8}$

DARA (For Read) = $\overline{0}.\overline{5}.\overline{8}\{1.3.4(2+6+7)+(1+3+4).2.6.7\}$

DNOIS = 0.4.6+1.2.8+3.5.7+(0+4+6)(1+2+8)(3+5+7)

4.9.2 Block format check

The following will be described in this subsection:

a) HNIS signal for identifying a block in Write command, and Back Read type command after write command.

b) HBLK signal for detecting a block in Read type command.

c) HTM signal for detecting a Tape Mark.

d) EPOSA signal that resets the PHOK signal.

e) End Data Check Counter.

f) Start Read Check Counter.

g) Slip Check Counter.

h) Noise Check Counter.

4.9.3 Basic read timing

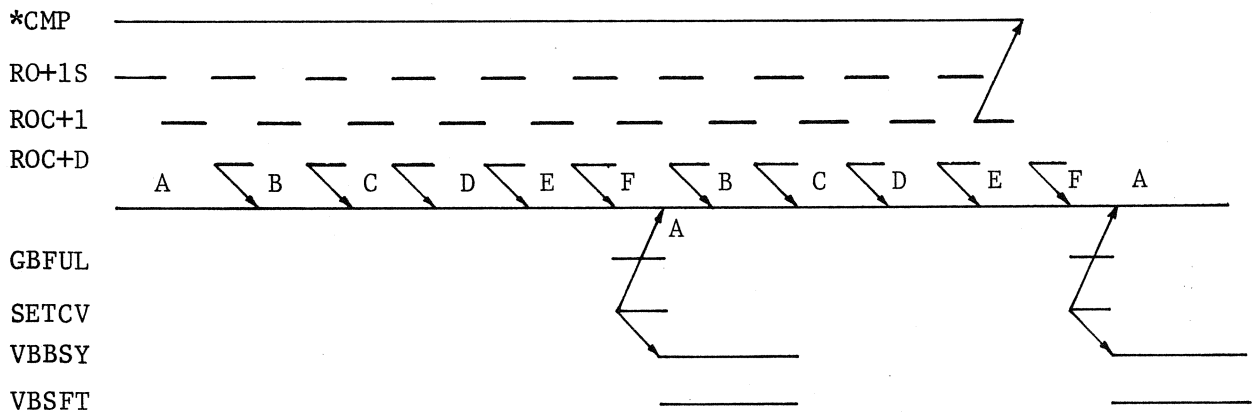


Figure 4.41 6250 BPI basic timing (1/2)

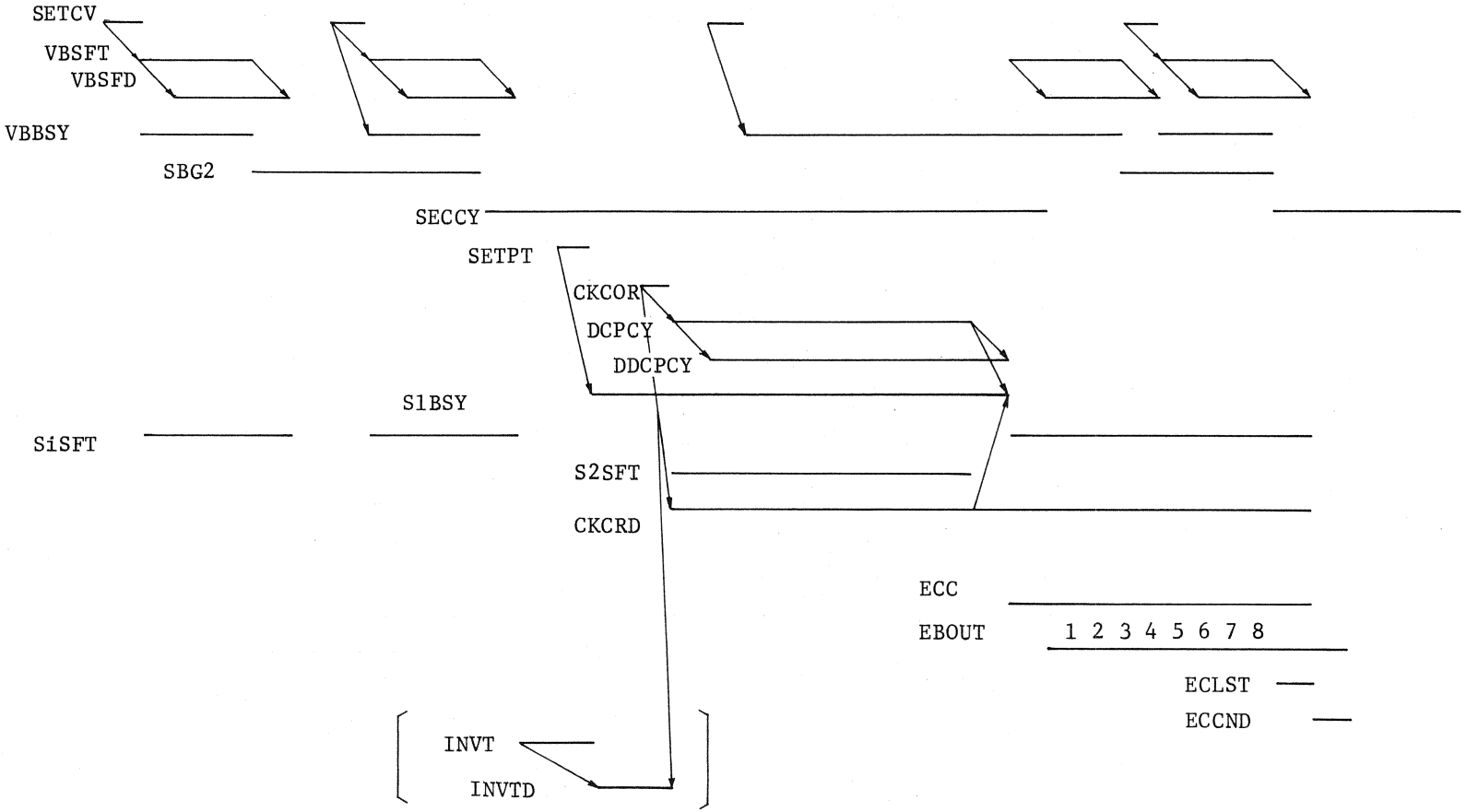


Figure 4.41 6250 BPI basic timing (2/2)

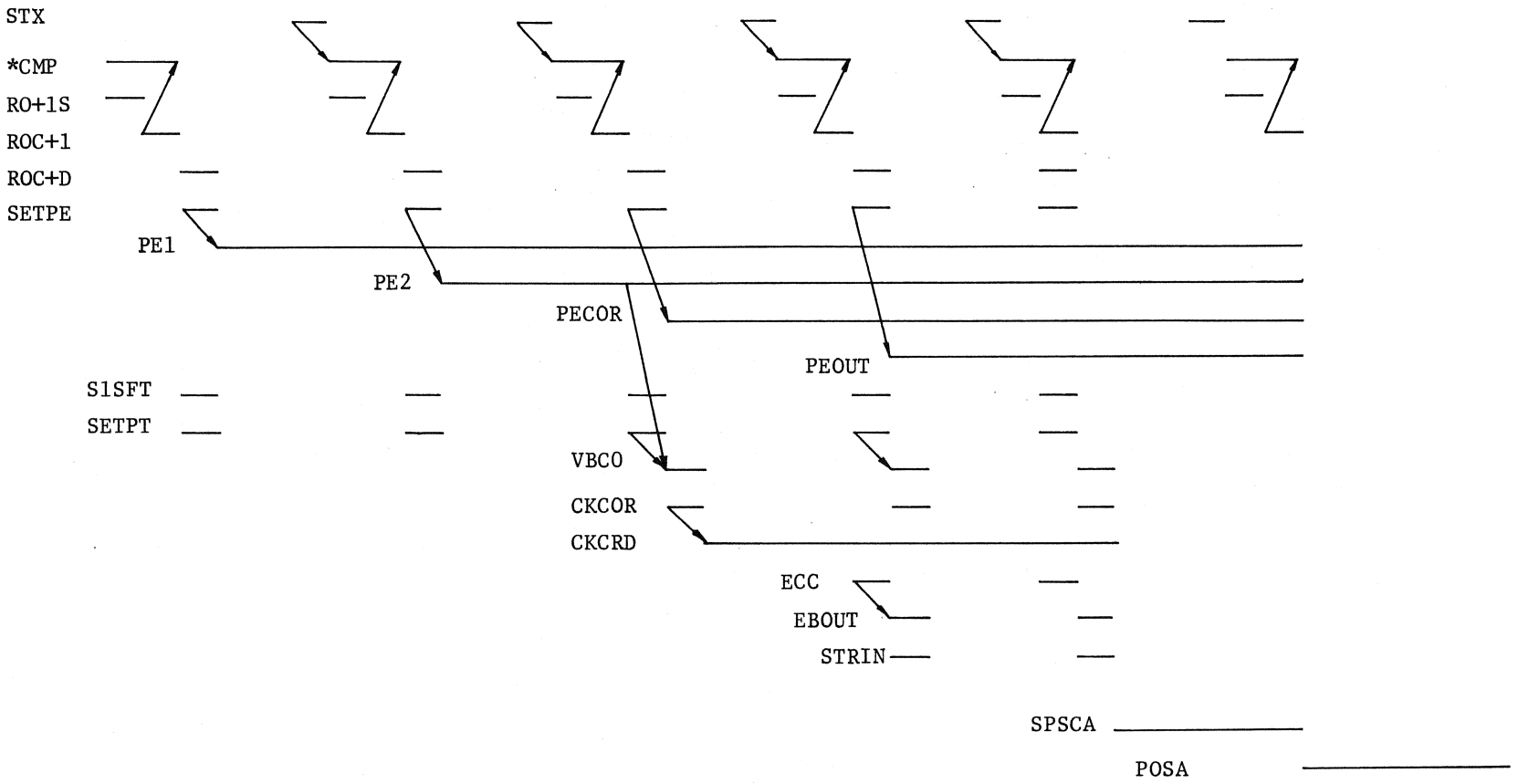


Figure 4.42 1600 BPI basic timing

4.9.4 Deskewing buffer

Modulation data is set in the deskewing buffer after synchronization with formatter clock. Phase Error detection signal is stored at the same timing as the data.

Data is entered into the buffer trackwise. However, it is read out simultaneously. The buffer capacity is equivalent to 32 bit cells.

The Read In Cycle signal (RICY) will be set after mark '1' is detected after a series of '1's (for 10 bit cells) in 6250 BPI mode, or if 00001 pattern is detected in 1600 BPI mode. When data is detected after RICY signal has been set, the Read In Counter is advanced and the CMP signal of the track is reset. CMP signal is reset as soon as the Dead Track Pointer is set. Read Out Counter is activated as soon as the CMP signals of all the tracks are reset.

4.9.5 Skew control

Pointer and skew errors are set in the up/down counter used for indicating the volume of data in the deskewing buffer.

(1) Pointer in 6250 Mode Read Command

The Dead Track Pointer for indicating skew of less than 2 bits is set if a track with skew in excess of 26 bits (STMP signal: '1') and seven tracks with skew of more than 4 bits (LAG signal: '1') are detected. If less than 6 tracks are involved (LED: 1), the Dead Track Pointer for skew in excess of 26 bits is set.

(2) Pointer in 1600 mode Read Command

Dead Track Pointer indicating skew of under 2 bits is set if a track with skew exceeding 14 bits and more than 7 tracks with skew exceeding 4 bits are detected. Dead Track Pointer indicating skew of over 26 bits is set if less than 6 tracks are involved.

(3) Skew Error

Skew Error is set in the following cases:

1600 mode Write: over 2 bits
6250 mode Write: over 14 bits.

When skew marginal has been specified, skew error is set under the following conditions:

1600 mode Read: over 4 bits
1600 mode Write: over 1 bit

Skew marginal is invalid in 6250 mode.

4.9.7 Pointer

(1) 1600 Mode

There are two types of pointers in 1600 BPI mode. They are Dead Track and Valid Track Pointers.

a) Dead Track Pointer

- Track in which time sense signal has been reset while PHOK signal is '1'.
- Track with excessive skew.
- Track (read only) subjected to 8 byte serial correction with reference to the valid pointer data (this correction is carried out after the valid pointer has been set).

If any of the above three conditions are set, they will not be reset during the processing.

b) Valid Pointer

Normally this pointer is set in a track in which a phase error has been detected and is set unconditionally in Write Operation. It is set during preamble and postamble in Read operation. It is also set unconditionally if other track pointers have been set, but it may only be set in data if parity error has been detected.

Once the valid pointer is set, it may only be reset if 8 bytes (or more) serial error correction is not executed and the data is changed from 0 to 1 or 1 to 0 (in read only).

(2) 6250 Mode

Three types of pointers, Dead Track Pointer, Valid Pointer and ECC Group Buffer Pointer are available in 6250 mode.

a) Dead Track Pointer

The conditions for setting this pointer are the same as that in 1600 mode. In Read Operation, if the time sense is '1' when resynchronous burst is detected, this dead track pointer is reset.

b) Valid Pointer

- Track subjected to error correction.
- A track in which invalid data pattern and mark is not detected in the mark field.

This pointer is set under any of the above two conditions. If a pointer is set in a track in which a dead track pointer has already been set, it will be reset automatically. It is also reset if 8 data groups or more of serial error correction are not carried out in Read Operation.

c) ECC Group Buffer Pointer

This pointer is set if a phase error is detected in a data group to be processed. If dead or valid track pointers of more than three tracks have been set, the ECC group buffer pointer is not employed as a pointer.

In Read Operation, this pointer is reset upon detection of resynchronous burst and upon completion of processing of a data group.

4.9.8 Data flow

The data deskewed at the deskewing buffer (PD0~8) is set in the sub group buffer when the ROC+D signal (which is a step delayed from ROC+1) is set ('1'). As soon as the five bit data counted by the group counter is set in the buffer, the group buffer full signal (GBFUL) is set.

The five bit output from the group buffer is subjected to 5-4 conversion to obtain 4 bit data.

At this stage, Mark 1, Mark 2 or All 1 mark is detected. The 5-4 conversion data is preset in the conversion buffer at SECTV '1' timing when GBFUL signal is '1' and conversion buffer busy signal (VBBSY)is '0'. The data from conversion buffer shift signal (VBSFT) is output serially by the conversion buffer shift signal. This CVD0~8 output data is stored in the ECC buffer by the S1SFT signal (S1 register shift timing signal). This buffer is made of 8 bit serial in/serial out requester. The ECC register output data is subjected to error correction and then set in the ECC buffer out register. The output data (EO0~8) from this register, is set in the transfer buffer as Read Data when STR1N signal is '1'.

Read system data flow is shown in Figure 4.45.

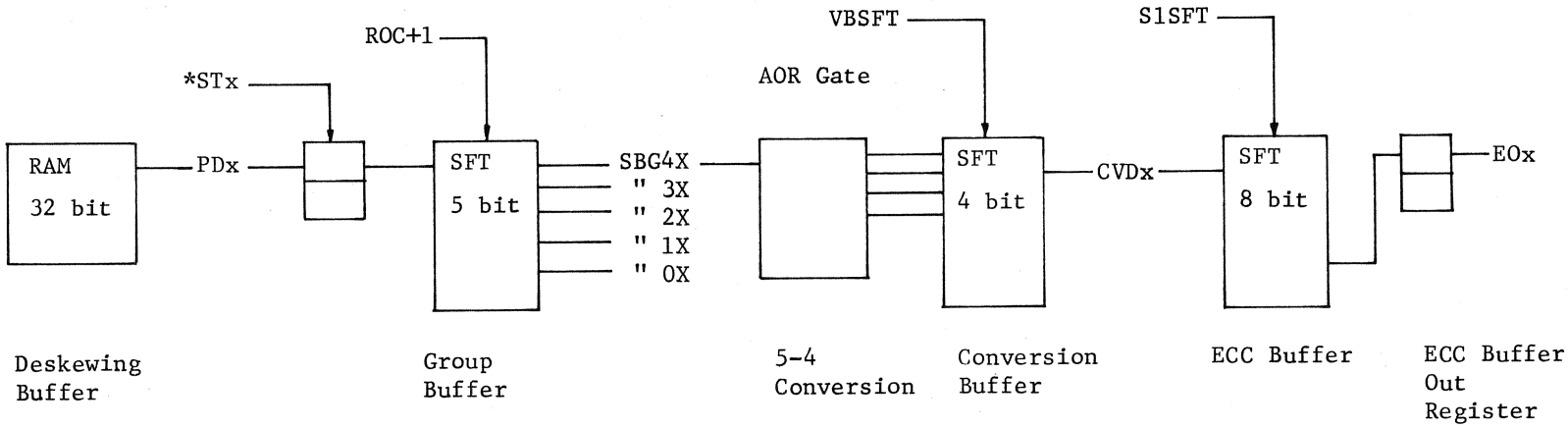


Figure 4.45 Read circuit data flow

4.9.9 CRC check

The following data check circuits are provided: CRCA, CRCB, CRCC, CRCD and CRC. CRCA is generated from the transfer buffer input data.

CRCB is generated from the transfer buffer output data.
CRCC is generated from the data and Aux-CRC byte.
CRCD is generated from Aux-CRC byte.

CRC is generated from data, padding characters, Aux CRC byte and one CRC byte.

Details on checks in each mode are given in Table 4.30.

Table 4.30 CRC Check

		6250			1600			800			Sense Data
		WT	RD	BR	WT	RD	BR	WT	RD	BR	
CRCA ≠ CRCB	Transfer Buffer Input/Output does not match	o	o	o	o	o	o	o	o	o	P Compare Transfer Buffer Check
CRCB ≠ CRCC	Write Data and Read after write Data do not match				o			o			CRC CRC III
CRCB ≠ CRCD	R/W data and the Aux-CPC Data read out do not match	o	o								CRC CRC III
Unmatch CRC	Required pattern not obtained in Read data CRC Check.	o	o					o	o	o	CRC
Unmatch CRCC	CRCC generated from Read data does not have the required pattern			o							CRC CRC III

4.10 800 BPI Read Circuit

As soon as ROK signal is set ('1'), the Read data from MTU is integrated in the Analog circuit and thus converted into a peak pulse (PEKP0-8). An OR of PEKPX of nine tracks is obtained to generate a Read Clock signal (RCL signal). It is then synchronized with internal clocks to obtain a RCVD signal.

The 800 BPI circuit internal clock is equivalent to one quarter of formatter full clock. One bit cell in 800 BPI mode is equivalent to 48 clocks. Count is started after RCVD signal is set to '1'. Sampling pulse (SMPP), skew gate (SKWG), HRCRG, HRCHG and block end (BLKED) is generated by decoding the counter value. In write status SMPP signal is set ('1') at 33% of the bit cell. It is executed at 48% of the bit cell in read status. If skew is detected and RCL signal is set again ('1') (after TRCD signal), the signal will also be '1' (MLTB signal). In this case sampling pulse will slip by 9% and will therefore be set ('1') at 57%.

Table 4.31 NRZI clock

Tape Speed (IPS)	Clock Cycle (ns)
200	130
125	208
75	347
50	521

Marginal sampling timing varies with TM0-3 specification. HRCRG signal is turned ON ('1') and CRC signal is set in forward status, if RCVD signal is not set ('1') within two bit cell period.

HRCHG signal is turned ON, if the RCVD signal is not set ('1') during 5.33 bit cell period. If this signal or the NSPT signal is set ('1'), the CRC and LRC signals will be reset.

NSPT1, CRC, and LRC signals are synchronized with formatter full clock. STRIN signal is set ('1') if both LRC and CRC signals have been set '1'. At this stage data is stored in the transfer buffer.

Data is set in RA register so that the track, (the peak pulse of which is '1') is also set to '1'. EOR of the RAx, output from RA register and ETRKx signal (error track register signal set by RTIE command) is set in RD register when SMPP signal is '1'. The NRZDx signal from RD register is stored in transfer buffer when STRIN signal is set ('1').

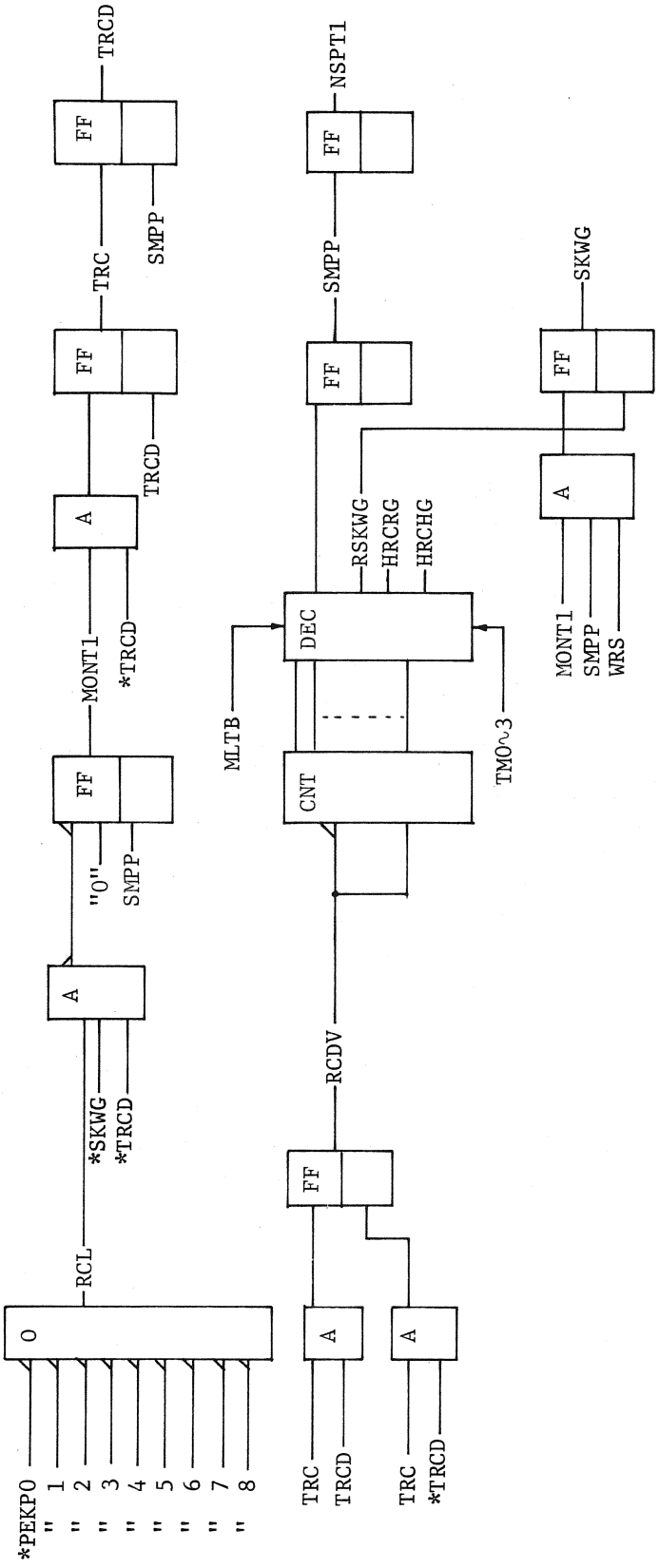


Figure 4.46 800 BPI Basic circuit

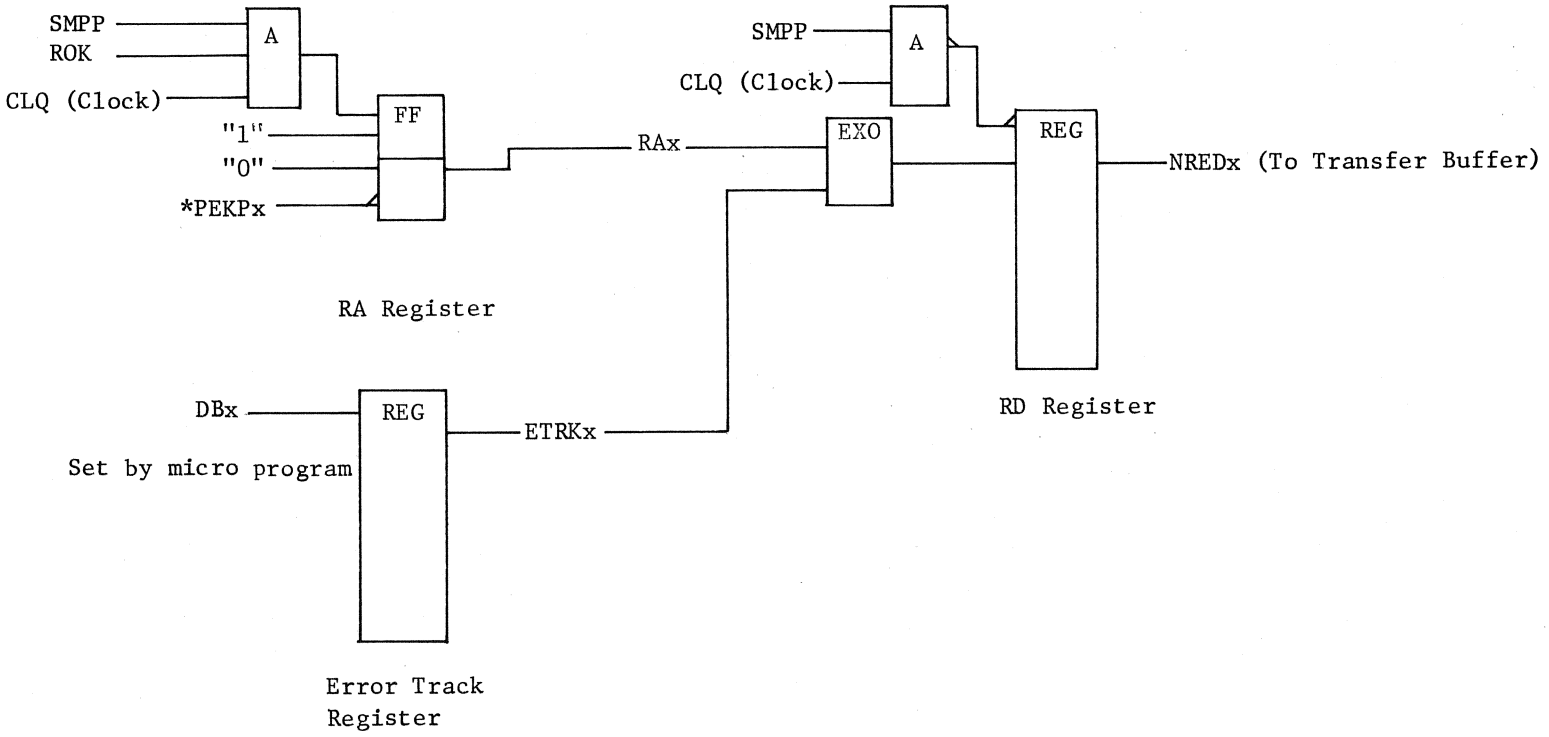


Figure 4.47 800 BPI Read data flow

4.11 Demodulation Circuit

4.11.1 Principle

The peak signal that indicates the position of the peak of the read signal in MTU is sent to MTC after being gated by the amplitude sense signal. The peak signal is inputted to the variable frequency oscillator (here after referred to as VFO) and the VFO output the reference signal. The phase of this reference signal is compared with that of the peak signal to check the phase difference, and then the information (1, 0) is demodulated.

PE and GCR mode timing charts are shown in Figures 4.49 and 4.50 respectively while the block diagram is shown in Figure 4.48.

Numbered waveforms in the timing chart, represent the waveforms on the signal lines of the same number in block diagrams.

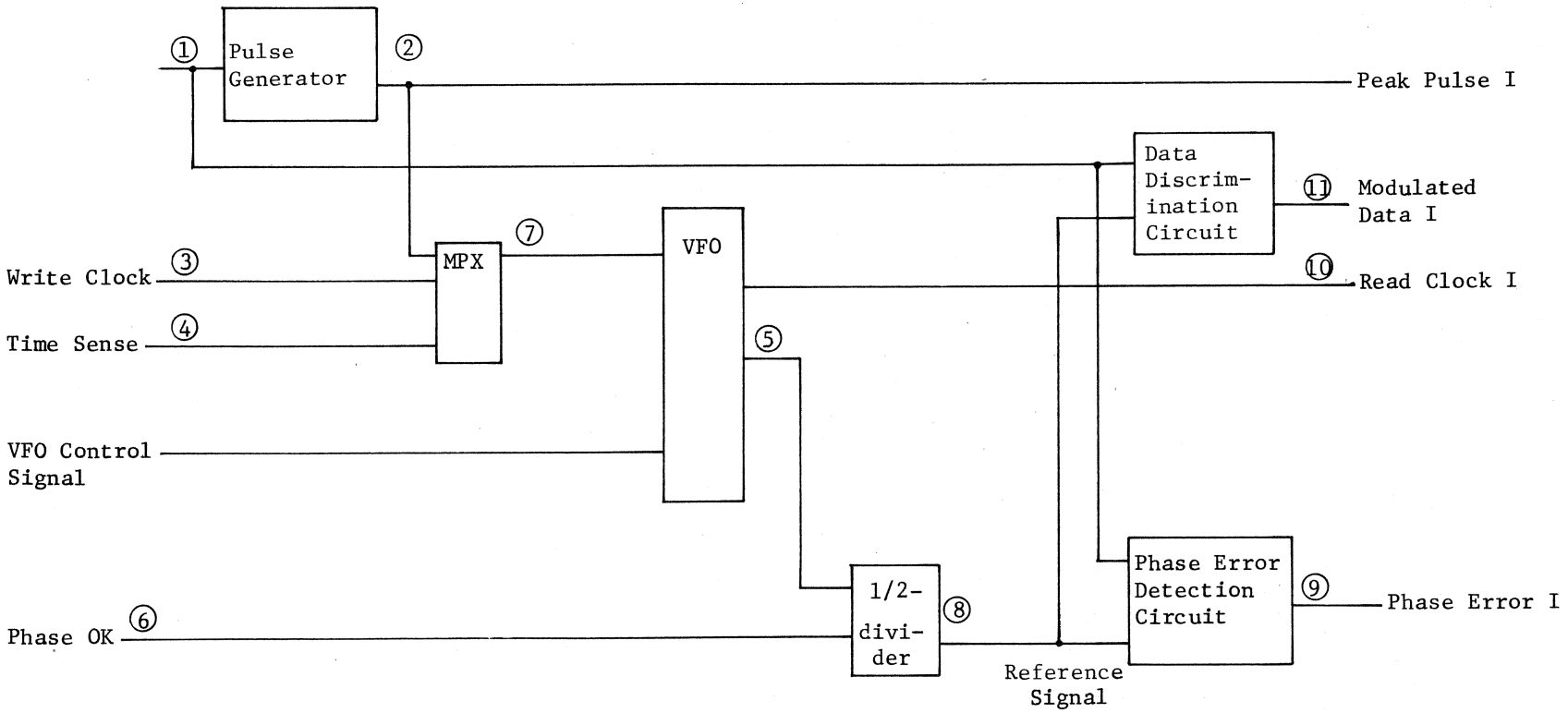


Figure 4.48 Block diagram of demodulation circuit in GCR and PE mode

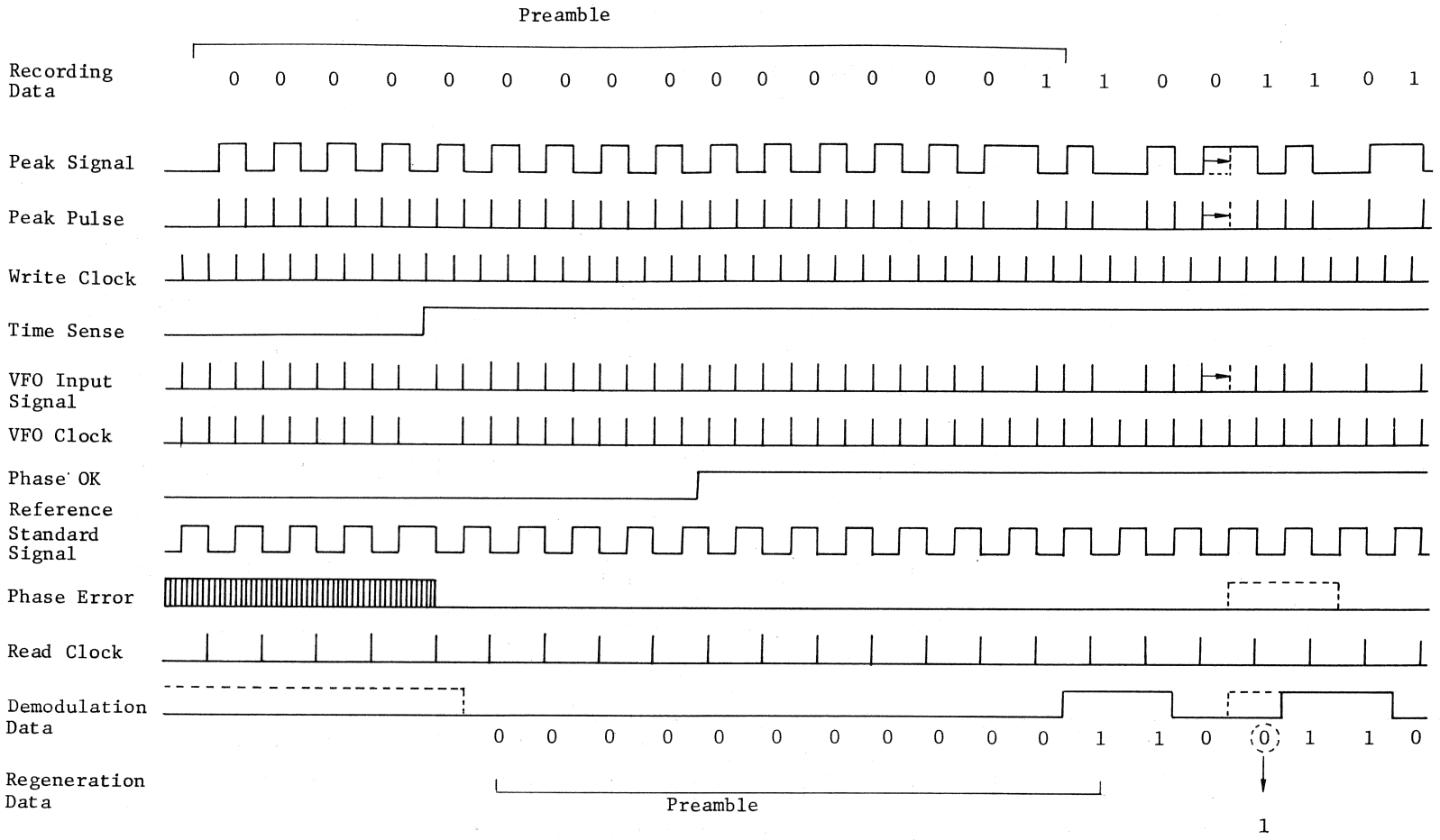


Figure 4.49 Demodulation timing in PE Mode

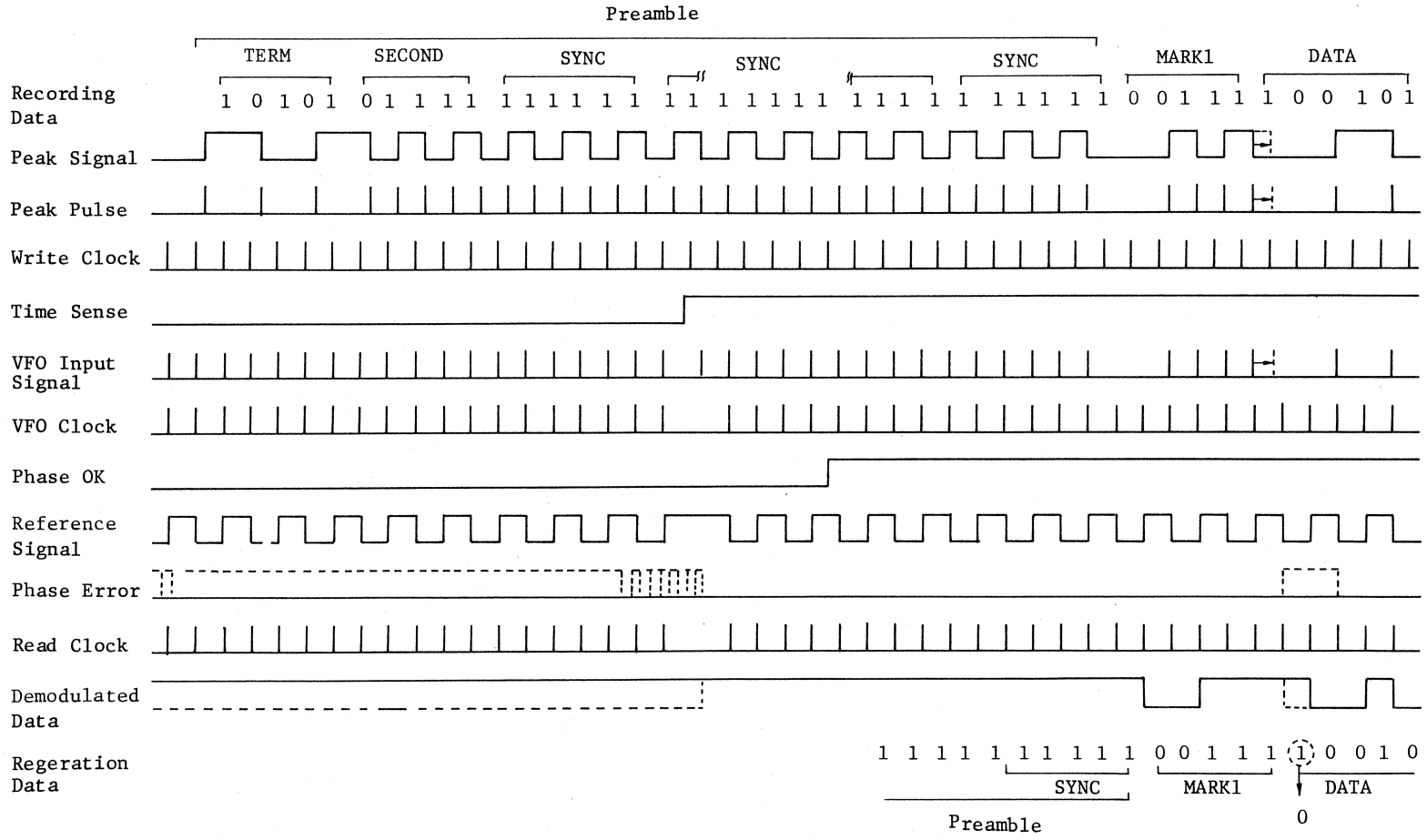


Figure 4.50 Demodulation timing in GCR mode

4.11.2 Demodulation circuit signals

(1) Peak Signal 0~8

These signals indicate the peak of read data from a magnetic tape.

(2) Peak Pulse 0~8

Pulse corresponded to leading and trailing edge of Peak Signal (1).

(3) Write Clock

Standard clock for holding VFO in normal condition.

(4) Time Sense 0~8

This signal rises if the peak pulse (2) continues over a specified time period. It is used to alter VFO input signals.

(5) VFO Clock 0~8

VFO clock synchronized with VFO input.

(6) Phase OK

Demodulated data and phase errors become effective after this signal is issued.

(7) Reference Signal 0~8

Signal divided VFO Clock.

(8) Phase Error

This signal indicates that the peak pulse is missing or the phase of Reference signal and that of Peak Signal are remarkably different.

(9) Read Clock 0~8

Clock signal for processing Demodulated Data (10) data.

(10) Demodulated Data 0~8

Data identified by 1, 0 codes.

4.11.3 Demodulation in PE mode

The data in 1600 BPI mode is recorded on magnetic tape in PE format.

The VFO is synchronized with the Write Clock (3) in order to adjust the free-running frequency while waiting for data block Peak Signal.

As soon as a data block is detected, peak signal (1) is transformed into peak pulse (2) by the pulse generator. And the time sensor generates time sense (4). Then the VFO input signal (7) is converted from Write Clock (3) to a peak pulse (2). Thus the VFO which has been synchronized with Write Clock (3) is made to synchronize with peak pulse (2), and a VFO clock (5) synchronized with peak pulse (2) is generated. Reference signal (8) is generated by subdividing this VFO Clock (5).

By comparing the phase of peak signal (1) with the Reference signal (8) at each bit cell, the data is identified as "1", "0". The demodulated data (11) is output at the read clock to obtain regenerated data.

Phase error signal (9) is generated if the phases of peak signal (1) and Reference signal (8) are remarkably different due to phase shift, missing bit etc.

4.11.4 Demodulation in GCR mode

In 6250 BPI mode, the data is subjected to GCR processing and recorded on magnetic tape in NRZI mode. In NRZI mode, '1' represents reversed pole while 0 represents original polarity.

As in PE mode, VFO generates VFO clock (5) in synchronization with peak pulse (2). Peak signal (1) and Reference signal (8) phases are compared (from the center of a bit cell to the center of the next bit cell) to identify data (1 or 0).

Regenerated data is then obtained by outputting this Demodulated data (11) at Read Clock (10).

Phase error signal (9) is generated if the phases of peak signal (7) and Reference signal (8) are remarkably different due to phase shift etc.

4.12 MTU Interface Circuit

Interface circuit for interface with MTU is shown in Figure 4.51. The interface signals to various MTUs are illustrated in Figure 4.52. Distributor and MTUs are connected by a signal flat cable. Two types of distributors are available. They are the distributor for MTU cross call (DGBM) and for signal MTC (DGAM). A Distributor is used to logically link one of the 8 MTUs and one of the two MTCs. An MTU is selected by DVSEL register, SLTAG (select tag) and DVA0-2 (device address 0-2) bits. As soon as SLTAG bit is set, the DVA0 2 bits are decoded. Then, HSLNA or HSLNB signal corresponding MTU is set and control signal is transmitted. Selection ratch is employed for controlling MTU cross call operation. If a MTC from the opposite side has been selected first, the ratch is not set and therefore control signal is not sent to MTU. This ratch also enables MTU reserve/release and online/offline control from the operator panel.

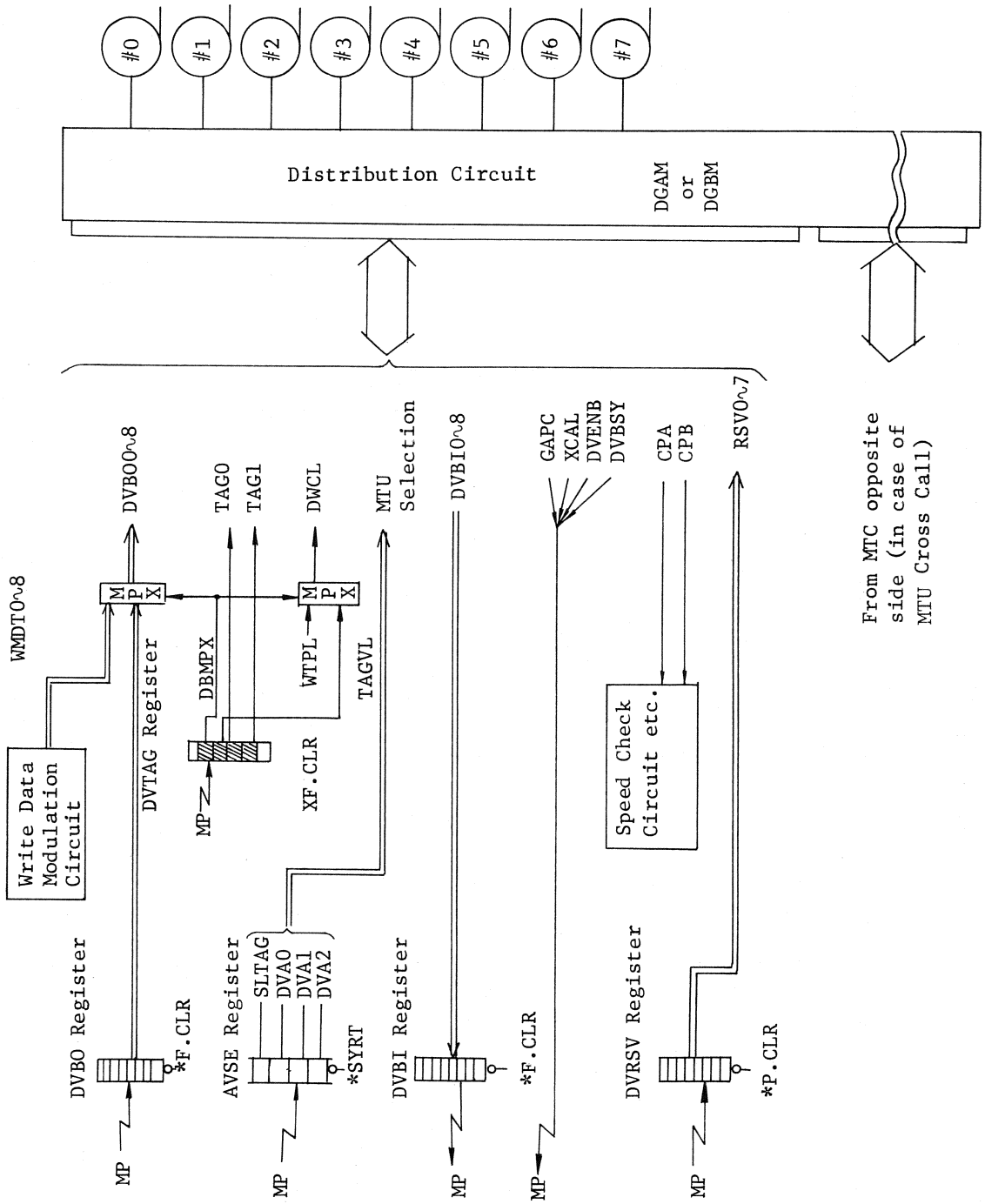
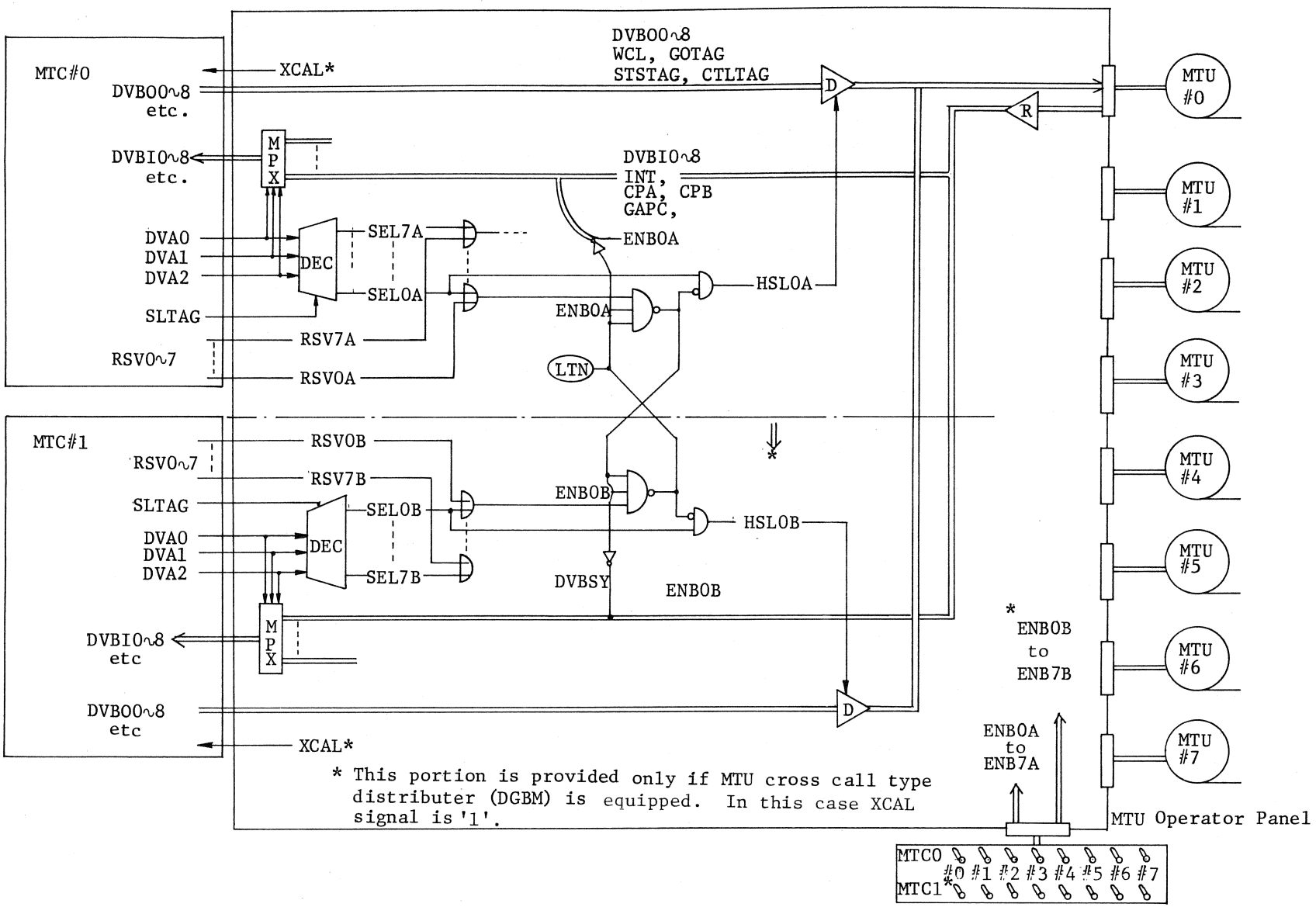


Figure 4.51 MTU interface circuit



* This portion is provided only if MTU cross call type distributer (DGBM) is equipped. In this case XCAL signal is '1'.

Figure 4.52 Distributor section

4.13 Power Supply Section

The MTC power supply supplies the required AC and DC power to the MTC section of the magnetic tape subsystem.

4.13.1 Function

(1) Acceptable AC power input specification is shown in Table 4.36. This input power is converted to a stable DC power (+5, -5.2 V).

Table 4.36 Input standards

Item	UL power supply			
Input voltage (V)	200	208	220	240
Phase	Single-phase			
Frequency (Hz)	50/60	60	50	50
Input current (A)	3.6	3.4	3.2	2.9
Rush current (A)	25			

(2) Provided with an overload protection circuit.

(3) Features DC output sequence operation function as well as a warning display for abnormal power supply.

(4) Features a power supply control interface.

(5) Automatic breaker activated by temperature alarm etc.

(6) Emergency breaking by UEPO switch.

(7) Illustrated in Figure 4.53.

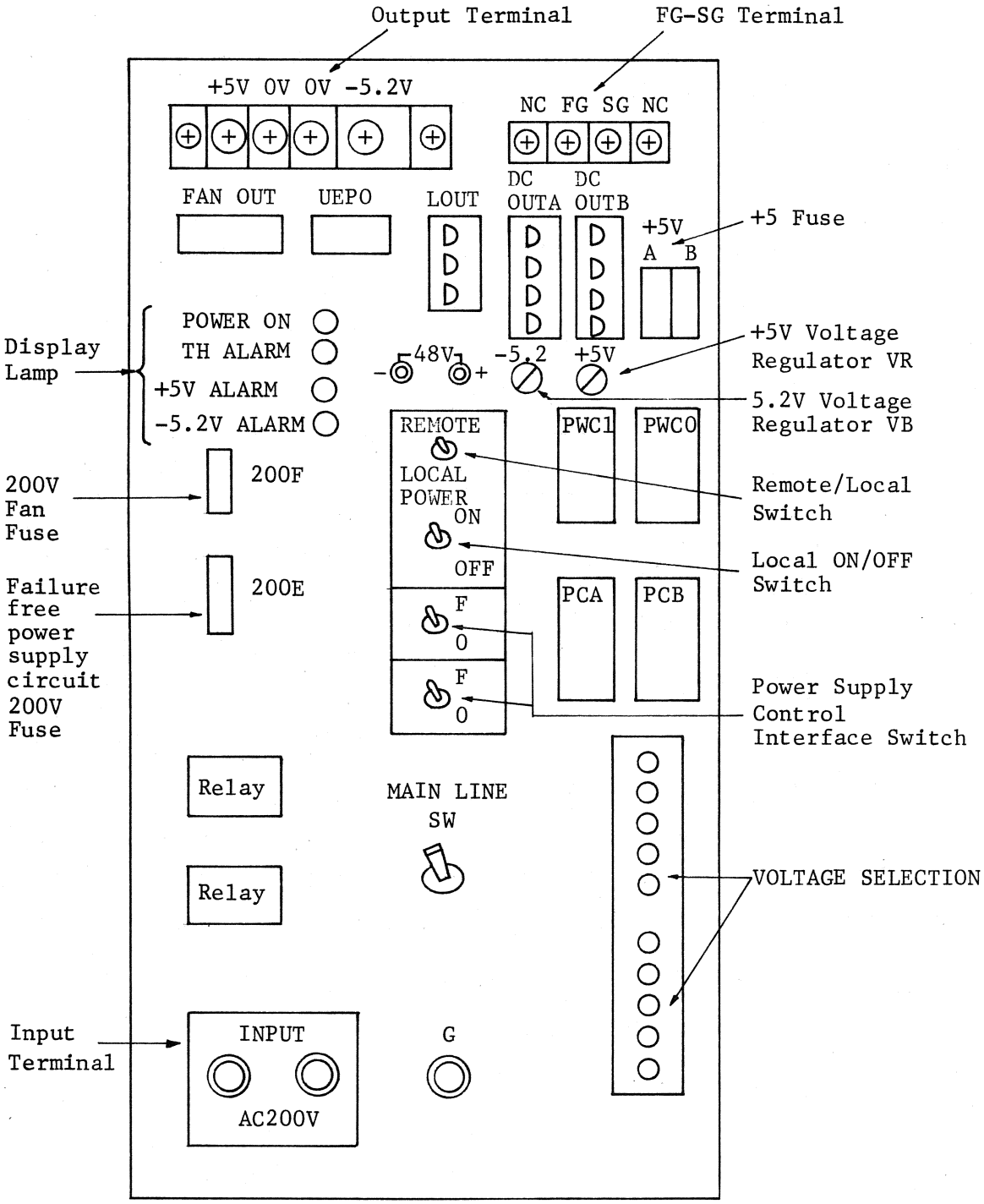


Figure 4.53 External view of power supply operation panel

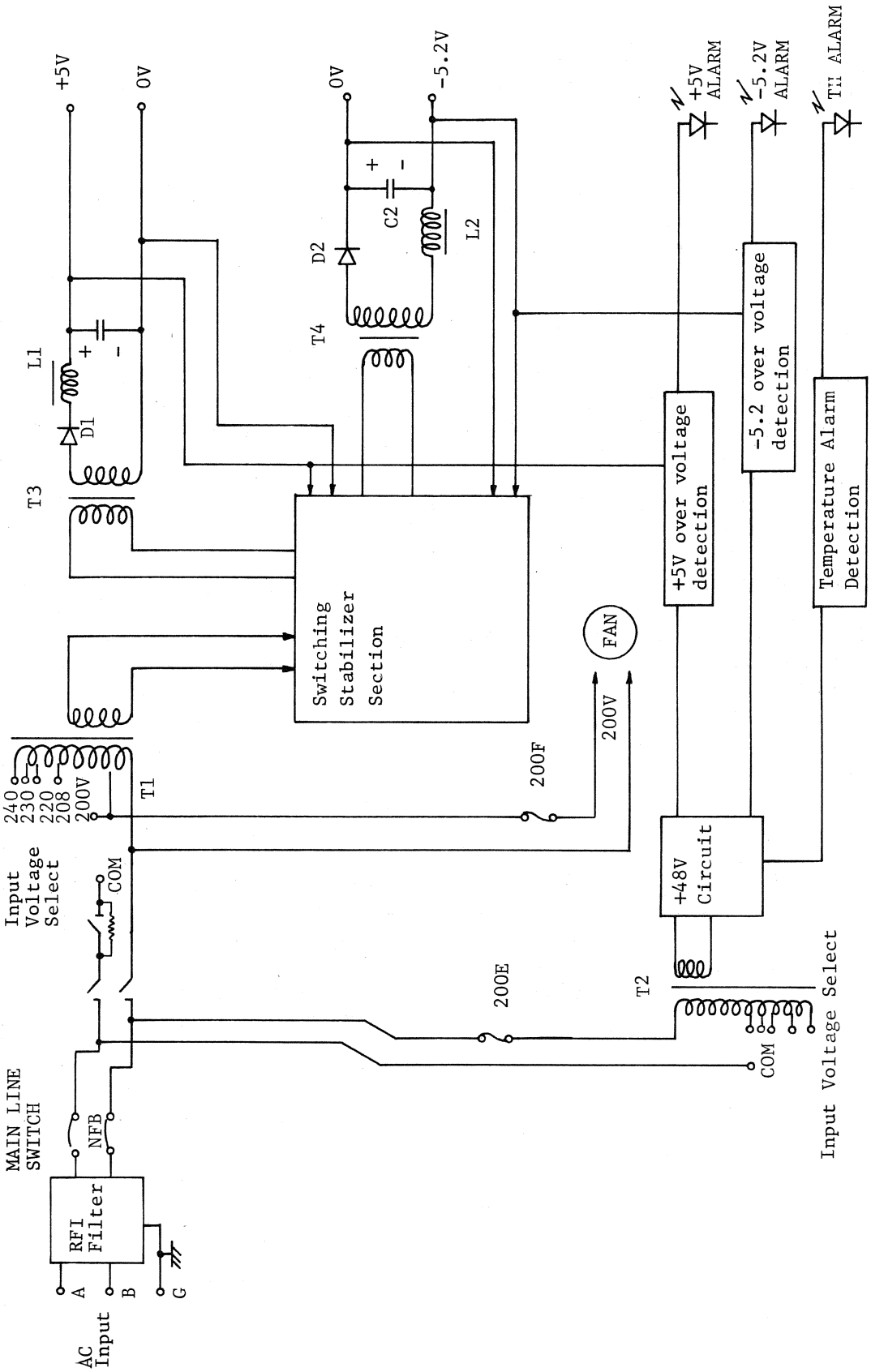


Figure 4.54 Power supply functional block diagram

4.13.2 Configuration

Configuration of the power supply section is shown in Figure 4.54.

(1) +48 V circuit

The input power is applied to transformer T2, then rectified and smoothed to obtain a +48 V supply. The +48 V power supply is used as failure free supply for driving relays.

(2) +5 V/-5.12 V circuit

The input 50/60 Hz, is applied to transformer T1 then rectified and smoothed to obtain a DC supply. This DC supply is then switched by the transistor at 50 kHz to obtain a high frequency AC supply. This high frequency AC power is transformed, rectified and smoothed by T2 and T4 to obtain +5 V and -5.2 V supply. The output voltage is stabilized by feed back to the above switching section to meet load fluctuation in +5 V, -5.2 V supply.

4.13.3 Power Ready signal

This power supply section generates PRDY signal to be sent to MTC for resetting. The timing chart of this output signal is shown in Figure 4.55.

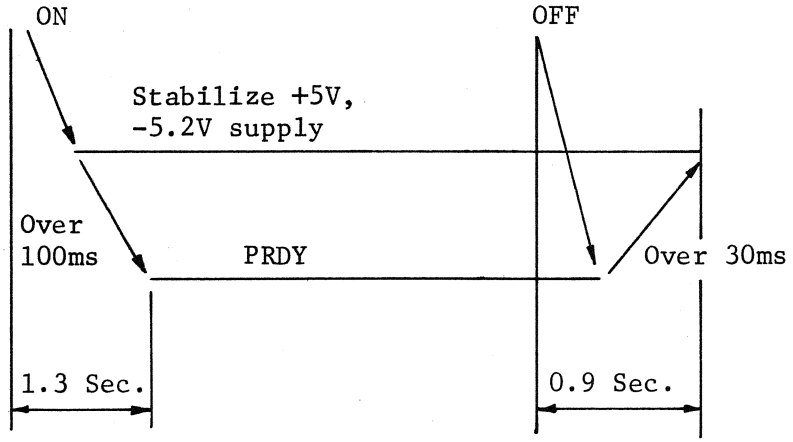


Figure 4.55 Power Ready timing

CCHAPTER 5 MICROPROGRAM

5.1 Outline

MTC microprogram will be described in this chapter. MTC microprogram includes 4K steps. It is designed to control all the MTC operations. The signals and bits handled by the microprogram are LSR, EXR bits described in Section 4.5. For the purpose of description in this section it is assumed that the reader is familiar to a certain extent with the hardware and the magnetic tape control unit described earlier.

Overall outline of the microprogram is shown in Figure 5.1. The microprogram starts from address '000' (hexadecimal) in the following cases: power supply is turned ON, selective Reset system reset form the channel, CE panel ON/OFF switch operation etc. At this stage the program executes the self test routine, followed by the reset routine. As soon as all the reset procedures are completed, the subsystem environment is checked by the SETUP routine and the system is initialized. Next, as the device scanning is completed by the device scan routine, the system becomes ready to receive commands.

At this stage, MTC goes into idle status till the channel starts the initialize selection sequence. As soon as this sequence is started, INS trap is generated and initial status is transmitted by the initial selection routine and status handling routine.

At this stage, if commands are ready for execution, command operation is carried out by the MCY group of routines.

UPON completion of command operation, sense data is stored, end status is generated and the status handling routine again transmits a new status.

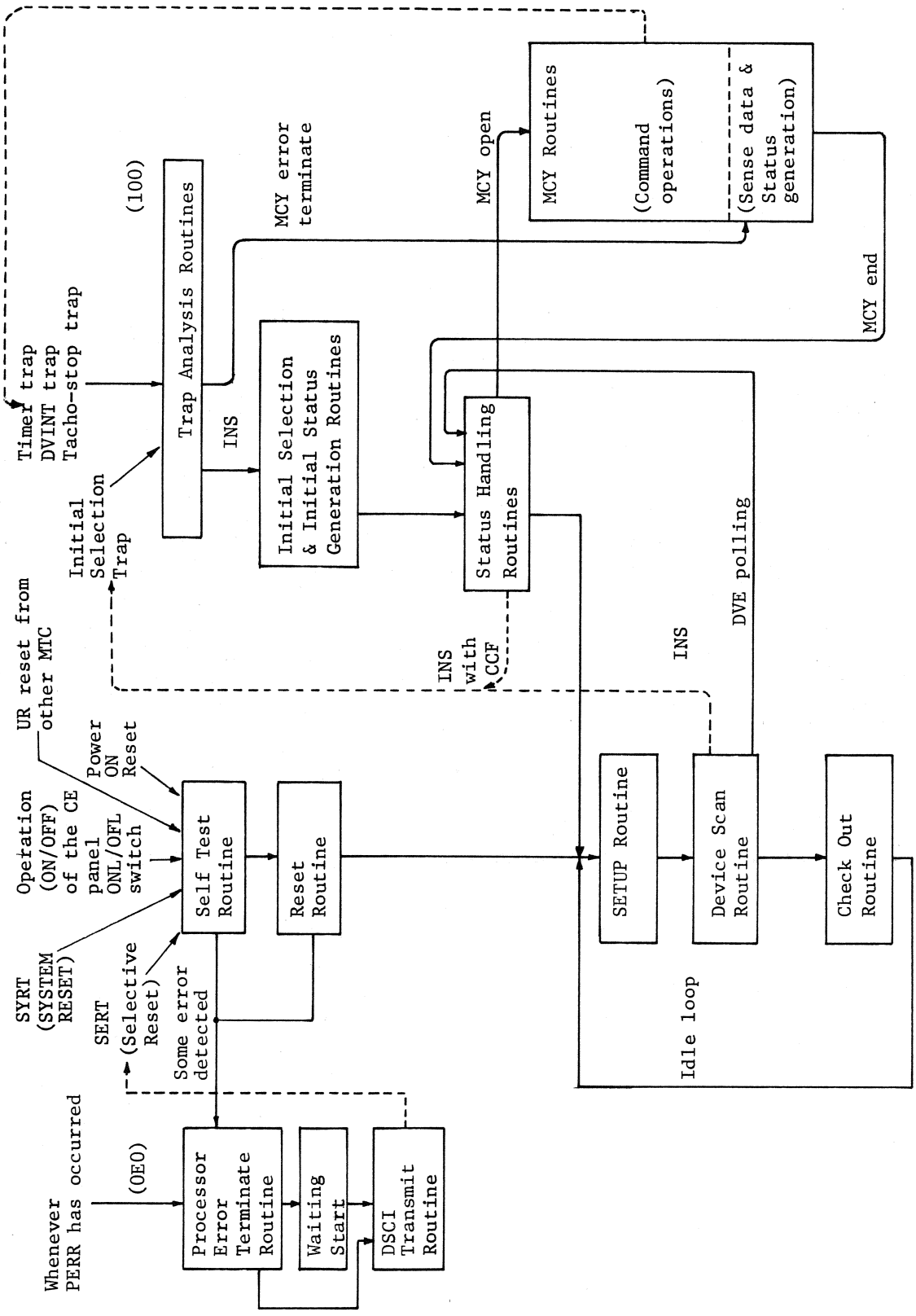


Figure 5.1 Microprogram structure

5.2 Self Test Routine

This routine is provided to confirm normal operation of the processor prior to starting micro processor control.

(1) All commands are attempted in the test (various combinations of OP code and EOP code field).

(2) Tests on the hardware related to the processor.

(3) Tests source register address field, destination address field, immediate data field etc. by altering the field values to confirm normal detection of address line, register address line, processor write bus, and processor read bus.

(4) Tests all ALU operation codes branch codes etc.

(5) This test routine confirms error mode which affects only the processor hardware. This test is so designed that EXR is not used and registers using LSR are limited to the minimum.

(6) Carries out tests starting with basic branching systems to complicated command systems (systems which involve extensive hardware).

(7) This routine displays the errors thus detected on FRU (sense bytes 22, 23). However, Disconnect-In sequence is employed for the following operations in on-line mode.

5.3 Reset Routine

The conditions for execution of reset routine and its operation are shown in Table 5.1.

Table 5.1 Reset routine execution conditions (1/2)

Cause / Operation destination	Power ON	CE Panel ONL↔OFL	UR Reset by other MTC's	Channel Interface	
				System Reset	Selective Reset
Inquiry Register 00; DVENQ#0 ~ 07; #7	Resets all the inquiry flags about all MTUs.				Resets inquiry flags about the channel interface side to which the MTC linked.
Mode memo 08; MODEM	Resets the flags.				Not Changed.

Table 5.1 Reset routine execution conditions (2/2)

Operation destination \ Cause	Power ON	CE Panel ONL OFL	UR Reset by other MTC's	Channel Interface	
				System Reset	Selective Reset
MTC Reserve CRVA, CRVB	Releases the MTC reserved from the channel.				Not Changed
MTU Reserve RSVA/B,0~7 DVRSV	Releases all MTUs reserved from the channel.				
Sense hold of MTU	Resets all MTUs, except the MTUs that cannot be selected by the MTC (MTU's linked to other MTC).				Not Released
Ready hold of MTU High speed mode of MTU	Resets MTUs in READY status. Moreover, reset operation is not executed when the SP2 bit on the CE panel is ON.				Not Released
Sense Byte Stack Area	Cleared				Cleared
Error Count (for LSR)	Cleared				Not Cleared
Diagnostic Flag Byte Stack	Cleared	Not Cleared			Not Cleared
Offline Service Control Register	Cleared	Not Cleared			Not Cleared
Power on Diagnose Routines	Executed	Not Executed			Not Executed
Other LSR	Cleared				

(1) Once the reset operation is completed, IFCTL register bit R.RSTA, and RTCTL register bit R.RSTB, are set to complete the reset cycle. During this period, the response to initial selection request from the channel will be CUB status.

(2) If the microprogram detects an error during reset cycle, the cycle is aborted and the MTC waits subsequenct initial selection. Then Disconnect-in will be sent to channel.

(3) Power ON Diagnose Routines execute the following tests:

a) Write/Read tests with specific patterns to LSR.

b) Scan In/Scan Out test for all LSI's.

c) External register bit ON/OFF test.

d) Timer function Test.

5.4 Setup Routine

The following operations are carried out by Setup routine.

(1) Sending CUE status

When CUB status has been sent and CUE status has not been posted to the channel, MTC generates CUE interruption as soon as an MTC becomes available to the channel.

(2) Inspect the status of operator panel

Interface ON/OFF switch (hereafter referred to as IF ON/OFF switch):

Checks the status of IF ON/OFF switch and executes the following operations if it is OFF.

a. If an MTC is reserved from the channel interface, this routine releases such an MTC.

b. If no pending information left in the MTC, this routine sets bits DSOKA and DSOKB to enable MTC changing OFFLINE.

(3) Checks the status of MTU Enable switches on the operator panel.

If the above switch is on DISABLE side, the routine releases a reservation about such an MTU.

5.5 Device Scan

This routine scans the status of MTU and generates DVE interruption if necessary.

(1) After this routine has been entered and untill the scanning of the MTU specified by the SCAN pointer register, the processing cannot be started. In overload conditions, scanning of particular MTUs may be delayed (DVE interruption is delayed).

(2) MTU being used by another MTC is not scanned.

(3) After scanning all MTUs, check out routine and Setup routine are executed.

(4) Disabled MTU is not scanned.

(5) SCANP register is employed as a pointer for the MTU to be scanned.

5.5.1 DVE interruption

The causes of DVE interruption in the device scan routine are given in Table 5.2.

Table 5.2 Causes of DVE interruption

Inquiry			MTU Status	Remarks
BENQ	LENQ	SENQ		
1	X	X	o When the MTU is disabled by corresponding MTC operator panel. o When the MTU becomes IRQ status. o Upon detection of Load Fail (TUC). o When the MTU becomes Ready Status.	After DVE interrupt, TURST should be done.
X	1	X	o Upon detection of Load Fail. o When the MTU becomes Ready Status.	After DVE interrupt, TURST should be done.
X	X	1	o When the MTU is disabled by MTC operator panel. o When the MTU becomes IRQ Status. o When the MTU is in Ready Status and DVINT=0, DTM=0 (Ready before MTU detecting a tape mark). o When the MTU is in Ready Status and DVINT=0, DTM=1 (When MTU detects a tape mark). o When the MTU is in Ready Status and DVINT=1, BOT=1. o When the MTU is in Ready Status and DVINT=1, TOVR=1. o When the MTU is in Ready Status and DVINT=1, BOT=0. TOVR=0.	CUE, DVE, UCK(IRQ) " CUE, DVE, UCK (EQC, MISP, RWOVR) DVE CUE, DVE, UCK (BOT) CUE, DVE, UCK (TOVR) CUE, DVE, UCK (EQC, MISP, RWOVR)

5.5.2 Inquiry Set, Reset

Under the following conditions, the ENQ bits provided to each MTU or Interface are set or reset.

Table 5.3 Inquiry Set/Reset

Inquiry	Set/Reset Conditions
BENQ (Busy enquiry)	o This bit is set if the selected MTU is Busy and as a result Busy Status is sent to the channel. o This bit is set when execution of an unchained Rewind or DSE command has been initiated. o This bit is reset if status including DVE is posted to the channel with the corresponding MTU address.
LENQ (Local enquiry)	o This bit is set when the sense byte in which IRQ bit has been set is sent to the channel. (After executing the sense command). o This bit is reset if status including DVE is posted to the channel with the corresponding MTU address.
SENQ (Skip enquiry)	o This bit is set only if the MTU features the skip file function. o This bit is set when an MTU (Ready=0) starts the execution of Unchained Space File and Back Space File commands. o This bit is reset when status including DVE is posted to the channel with the corresponding MTU address as a result of completion or abortion of Skip file operation.

5.6 Initial Selection

5.6.1 Recognition of initial selection

As soon as an MTC detected Select-out, as a result of initial selection sequence executed from the channel, the INS (refer to Section 4.6) is set. At this stage, if MINS bit has also been set, T.INS bit is set to '1' (refer to Subsection 4.5.2 (26),(33)) and trap occurs with address '100' (hexadecimal). The trap decoding routine gives highest priority to the trap set by INS bit and the control is transferred to initial selection routine. Initial selection routine checks the status of the MTU or MTC to be selected, and determines if a command can be executed or not, then generates the required status (Initial Status).

On the other hand, if MTC is pending a status or sense information, the microprogram checks the INS bit, and passes the control to the initial selection routine without trap.

If CUB status is notified to the channel in short busy sequence, INS bit is not set to '1'. This is because route (reserved or another channel interface has been linking to MTC) may not be available.

5.6.2 MTU selection

As soon as an Initial selection request is detected, CHBO register data (IO Address) is set in DVA register and OPI bit is set. Thus MTC is linked to the channel. The lower three bits of DVA register are set in DVSEL register. Finally MTU is selected as the SLTAG bit is set. The following operations are carried out for the MTU thus selected.

(1) MTU is assumed to be 'Not operational' when DVENB bit = 0 (Disable Status) or MTU Sense Byte 2 is All '0's.

(2) MTU is assumed to be Busy when DVBSY bit is '1'.

(3) In all other cases, MTU sense bytes 0, 1, 3 are fetched to registers DVS0, DVS1 and DVS3. At this stage, if DVRDY bit is '0' along with DVONL bit, the processing is carried out for IRQ status. If DVRDY bit = '0' and DVDNL bit = '1', the processing is carried out for Busy status. If DVRDY bit is '1' and TAGIN response is normal, command decoding will be started.

5.7 Initial Generating

5.7.1 Generating Initial Status

Initial status is as follows if there is no pending status and sense data.

(1) Asynchronous DVE Status

If the MTU status changes during trap decoding or executing initial selection routine, DVE status corresponding to the DVE interruption for the inquiry described in Subsection 5.5.1 is reported. At this stage BSY status is added (except in TIO command). (DVE+BSY status).

(2) DVE Status by Ready-Hold

If MTU is in Ready status and Read-Hold, the MTU is assumed to have been set to OFFLINE. Therefore DVE is reported. In case of commands other than TIO commands, BSY bit is added. This results in BSY+DVE status.

(3) BSY Status

BSY status is reported if the selected MTU is loading, rewinding, executing a DSE or is executing a skip file operation. This does not apply to UR command.

(4) UCK Status

UCK status is reported under the following conditions.

Table 5.4 Causes of UCK status during Selection

Cause	Description
BOC (Bus out check)	o Parity Error in the command code. o Disconnect-In transmitted in the preceding command operation followed by selective reset. This BOC will be set in the first command after selective reset (includes the error code indicating the cause of Disconnect-In).
IRQ (Intervention Required)	o This status is set if MTU is in IRQ status in commands other than SNS, TURSV, TURLS, MTCRSV, MTCRLS, UR and SNSIO commands.
CRJ (Command Reject)	o When invalid command code is received. o When write kind command is attempted for a file protected MTU. o When MTCRSV, MTCRLS command is attempted for an MTC not provided with 2CH-SW option. o When TURSV, TURLS, UR or SNS I/O command is attempted for an MTC set in CPBL mode. o When MTCRSV, MTCRLS, TURSV, TURLS commands are not a first command in command chain. o When a DSE command not chained to ERS command is attempted. o When diagnostic transfer request is attempted for a MTU in BOT or TWA status. o When a undefined diagnostic transfer code is received.
NCAP (Not capable)	o When diagnostic transfer operation other than channel buffer transfer is specified to an MTU in 800 BPI mode. o If an attempt is made to read 800 BPI tape through the MTC or MTU without 800 BPI Feature or function. o If an attempt is made to read 6250 BPI tape with the MTU without 6250 BPI function.
EQC (Equipment check)	o When there is abnormal MTU Tag-In Response (excluding SNS, MTC RSV/RLS, TURSV/RLS, UR commands). o When there is hardware error like abnormal command decode, etc.

(5) CHE + DVE Status

Except for above (1)~(4), CHE, DVE status is (DSB = OC) reported immediately after a command is executed.

- o NOP command
- o DMS command

- Mode Set 800 BPI command
- Mode Set 1600 BPI command
- Mode Set 6250 BPI command

(6) Zero Status

Except above (1)~(4), DSB = 00 status (zero status) is reported for the following commands.

- TIO command
- Commands with data transfer

(7) CHE Status

CHE status is reported for commands other than above listed (control commands).

5.7.2 Initial status in case there is a pending status

(1) The status for an opposite side channel interface is pending;

a) BSY+CUE status is reported when CUE is pending. However BSY bit is not added in case of TIO command.

b) In all other cases, a status described in Subsection 5.7.1 will be generated. MTC will keep the pending status.

(2) If the status for a same channel interface is pending;

a) BSY bit is added to the pending status, and then it will be reported in case of same IO address. However BSY bit is not added in TIO command.

b) When the pending status is for a different device, CUB status is reported (if such a pending status is not CUE status. If the pending status is CUE status the processing is the same as in above (2) a).

5.7.3 Initial status in case sense data is pending - MTC keeps the pending status in this case.

(1) Initial selection from the interface side different from the pending interface side.

MTC fixes the channel interface switch to pending channel interface side, therefore the hardware generates CUB status in short busy same sequence to the opposite channel interface.

If the pending interface side channel is selected at the time of reporting such opposite side CUB status, CUB status will also be generated for the selection from pending side channel interface. However MTC will generate a CUE status consequently after a specified time delay for the pending side channel interface.

(2) Initial selection from sense data pending interface side

a) If sense data concerned with the same MTU address are pending, those sense data are cleared and the status given in Subsections 5.7.1 and 5.7.2 will be generated. The status generation is effected by the presence/absence of pending status.

If there is no pending status, the sense data is reset and the command is executed.

b) If Sense Data concerned with different MTU address is pending:

In this case CUB status is reported. However, the same processing as in above a) may be executed if CSPE, REGE bit has been set ('1').

5.8 End Status

Command operation is started if CHE (Control command), or ZERO (Burst command) status is generated as the initial selection status.

DVE status is generated upon completion of a command operation.

In addition to the Device End bit the following bits are added.

a) CHE bit: If Zero status was posted in initial selection.

b) UCK Bit: When an error is detected during the operation or when MTU starts normal unload operation in response to an Unload command.

c) UEX Bit: When a tape mark block is detected in Read, Read Backward, Space, and Back Space commands or when Write, Write Tape Mark, Erase commands are executed on TWA.

d) CUE Bit: When CHE status has been reported in initial selection and UCK or UEX bit is added in the End status.

5.9 CUB Status

CUB status obtained by adding STM bit to the BSY bit is reported in the following cases:

(1) During executing Reset routine.

(2) During command operation (MCY signal=1).

(3) When MTC is Busy with another channel interface.

(4) When there is pending status for other MTU (excluding CUE status). (Refer to Subsection 5.7.2)

(5) When there is pending sense data for other MTU (refer to Subsection 5.7.3).

(1)~(3) are sent by the hardware. (Short busy sequence)

5.10 CUE Status

If CUB status has been sent beforehand, the CUE status is sent as soon as MTC is free.

(1) Device address to be posted with CUE status should be '0'.

(2) RTCTL register's S.SW bit will be set (refer to Subsection 4.5.2 (40) when CUE status is reported to the channel. As a result, selection is stopped till CUE status sending sequence is completed.

(3) CUE status may be reported periodically (as explained earlier) while sense data is pending.

5.11 Interface Disconnect during Initial Selection

INTAG register DCN bit is set if interface disconnect request is received from the channel after MTC has set OPI bit (channel and MTC has linked). Microprogram executes the following operations if it detects that DCN bit has been set ('1') prior to send initial status to the channel.

(1) Stops transmission of initial status and clears INTAG register. In actual practice, INTAG and OPI signals are already reset by the hardware when the DCN bit is set.

(2) Does not start command operation and MTC status (status pending, sense pending) is not affected.

(3) Disconnect operation in initial selection sequence will not create a new status itself.

5.12 Command Chain

When initial status or end status has been received by channel, the microprogram checks SPOA bit in IFSTA register or SPOB bit in IFSTB register. If the bits have been set, the microprogram identifies it as a command chain and sets SCANP register CCF bit. On the other hand if the bits have been reset, CCF bit is also be reset. Microprogram executes the following operations after sending the status when CCF bit is set:

MTC waits for the next initial selection request without executing Device-Scan and Setup routines, Moreover, MTC doesn't release the MTU, and channel interface is not released. However, if bits SPOB or SPOA are reset during this wait the CCF bit will also be reset and the MTC will move to idle status.

5.13 Machine Cycle

In this cycle, a command is executed for the selected device and the result is set in the device status byte. MCY signal remains '1' while this cycle is executed. CUB status is reported if an initial selection request is received during this period.

Format Clock should be set depending on the tape speed and the mode of the selected device.

5.13.1 Command operation in RTIE, SDIA, LWR

Track-in-data for RTIE command is received using a M.SVI bit by the microprogram. Microprogram checks the value of CHBO register. If the value is X'00', the microprogram will set ETP bit and if the value is X'03', will set ZETK register to all '0's. In all other cases, microprogram sets CHBO register data into ZETK register.

Diagnose flag bytes for SDIA command are also received using a M.SVI bit by the Microprogram and accept the 4 byte data into SDIA0~3 registers. When GDT flag is specified, a time delay from 50 µs to 3.3 sec (approx.) can be elapsed. The time delay is determined by the status of flag bytes 2 and 3.

LWR command sets MTU to LWR mode and executes a write operation. Write data is returned by the MTU without moving tape. The data thus returned is received by MTC as read data.

All the error checks except slip check, like show begin, early begin check, etc., are the same as in Write command.

5.13.2 Command operation in REW, UNL

When REW or UNL commands are started, these commands reset the Write Error Count. If the preceding status is a Write Status, a fixed length (additional erase) erasing is executed. REW command sets BINQ flag bit and branch to DVSCAN routine when not command chain. UNL command sets intervention required (IRQ) bit in SBO and reports UCK.

If command chain has been specified, REW command awaits MTU ready status. While waiting, this command checks if MTU became offline or if tape unit check is activated (TUCK).

5.13.3 Forward type commands

This type of command includes WRT, WTM and ERS command as well as RD, SP and SPF commands. The former are Write type commands while the latter are Read type commands. If any of these commands are received at the beginning of tape (BOT) point, they are executed after BOT processings (IB, ARA etc). If a Write type command is received at a point other than BOT while MTU is in Read Status, these commands are executed after positioning.

WTM command writes the tape mark after erasing a fixed length.

In WRT type commands, velocity retry procedure is executed (after receiving GAPC signal) and then WOK signal is set for the required Write operation. In Read type command, the tape is moved by 20 QTP in the same direction and then ROK signal is set for executing the Read operation.

5.13.4 Backward type commands

UCK is generated if BRD, BSP and BSF commands are received on BOT.

If a Backward type command is issued to an MTU in Write status, the required operation is carried out after erasing the fixed length (additional erase).

In these commands, the tape is driven through 20 QTP before setting the ROK signal.

5.13.5 Positioning

When a Write command is issued to an MTU stopped in backward status or forward status, the area to which data is to be recorded is erased by the erase head as follows.

MTU is set to backward status. Then the write head is moved backward to a point to cover the entire length to be erased by the erase head. Next the device is set to erase status and erase operation is carried out with erase head only up to the block of the data to be retained. Device is then set to Write status and short erase is executed by write head or erase head. This erase is carried out so that the erased length is slightly longer than normal IBG. Then block write operation is started.

5.13.6 Velocity retry

This feature is provided to confirm that the tape speed has reached the required level prior to starting Write operation in WRT or WTM. Moreover Tach pulse is counted after GAPC in order to assure normal IBG.

If the tape speed is not normal, velocity retry is repeated up to the specified count. In this case sense data velocity retry is set. However this does not cause data check.

If the speed has not reached the required level even after the designated retry count, velocity check and equipment check are set and Write operation is not executed. Tape speed is continuously measured by the SPOK signals while in write operation.

5.13.7 BOT processing

When a Write type command is received at BOT, recording density is determined by Mode memory (MODEM register) and MTU model, then the recording density identify burst is recorded.

If the MODEM register is in conflict with MTU model or MTC option, the write operation will be carried out in a higher recording density.

In case of Write type commands, the tape is moved back the fixed length. The status is then changed to Write status and the length is erased by write head or erase head.

IB is then recorded in the length of 15 cm. In 6250 BPI mode only bit 1 is recorded. Only bit 8 will be recorded in 1600 BPI mode. All other bits are masked in both cases. All the bits are masked in 800 BPI mode.

If ALlWT, IBW and WOK bits are set by the microprogram, write operation will be executed in 3014 FCI (repetition of '100') in case of 6250 BPI mode, and in 1600 FCI (repetition of '10') in case of 1600 BPI mode.

In 6250 mode, GO is released and SAGC is specified to MTU as soon as WOK is released. Then ARA burst (all '1's) is recorded in all the tracks for a length of approx. 15 cm. This is followed by ARAID burst for approx. 5 cm. MTU starts processing after the specified time delay when SAGC is specified. As soon as SAGC check is generated, the DVINT signal is set ('1') and the microprogram is trapped. After the trap decording, Write processing is terminated and the tape is stopped. At this stage ID Burst check and SAGC checks are set as sense data.

GO tag is reset upon completion of IB, ARA, and ARAID processing. If CPBL bit is '0' when the next WRT and WTM commands are executed, approx. 45 cm are erased prior to executing such commands.

Both MTC and MTU are set in 1600 BPI mode and driven in forward direction when a read command is to be executed. When the Read Head reaches a point approx. 43 cm before the BOT mark, ROK signal is set and IB read operation is commenced. Microprogram checks the time sense signals of all the tracks. The program detects IB when the time sense of a particular track remains '1' for a particular length.

Both MTC and MTU are set to NRZI mode if IB is not detected. However, Not Capable will be set if MTU model or MTC option does not allow setting of this status.

Not Capable is also set if GCRIB is detected with not 6250 TU. In all other cases, after the tape is driven forward by 7cm from the BOT, Go Tag is reset, and SET SAGC is specified to MTU. Then Go Tag is set again and a check is made to determine if DBOB signal is detected (after approx. 3 cm passing). During this period MTU executes SAGC operation. If SAGC check is generated, DVINT signal will be set. At this stage, the microprogram sets the trap to stop the tape and execute a retry. MTC may retry ARA Reading for up to three times independently by itself. IB read operation will be resumed again after Rewind is executed and after the MTU becomes ready upon detection of BOT. If DBOB has been detected until retry limit, SAGC check, also data check, is set and UCK is generated.

If DBOB signal has not been detected, Not Capable and SAGC checks are set and UCK is generated.

MTC is set to 6250 BPI mode when set SAGC is specified.

If IBG is not detected within a designated period after PEIB or ARA burst, IBG-detect and equipment-checks in sense bytes are set, and UCK is generated.

5.13.8 Read operation

As soon as RD and BRD commands complete preprocessing, Go Tag is set, the tape is moved for by 20 QTP in the same direction, DBMPX bit is reset ('0'), All '0's is set in DVBO register, not zero threshold status is specified and ROK signal is set. STPHK signal is also set in 1600 or 6250 modes. If HBLK signal is detected, data block is assumed to have been detected and DXFI signal is set.

At this stage, all '1's is set in DVBO register and zero threshold is specified for MTU. If DIBG signal is found prior to detecting preamble, partial-record-check error will be set. If SRDC signal is set prior to detecting preamble, start Read Read check error will be set.

If DIBG signal is set after preamble is detected but before PHOK signal is reset by the hardware, partial-record error will be set. Zero threshold will be specified when PHOK signal is reset ('0'). At this stage, the system waits for DIBG signal. If EDCK signal is set before DIBG signal, postamble error will be set. In 1600 BPI mode, end-data-check is set in addition to the above. If all the above checks turn out to be normal, ROK signal is set along with the Go Tag. Crease check operation is executed if an error is detected.

If HTM and DIBG signals are detected prior to HBLK signal, UEX is set and crease check operation is executed. If HBLK signal is detected during this processing, it is assumed to be a data block and DXFI signal is set. (cancel tape mark block)

SP and BSP commands execute crease check operation after detecting HBLK signal. Processing is same as that in RD command operation when HTM signal is detected.

In SPF and BSPF commands, the tape is driven till DTM signal is detected.

In a forward type command, if HTM or HBLK are not detected within 20 m, tape-overrun error is set, and UCK is generated.

In 6250 BPI mode Backward command, if BOT is not detected within the specified length and thus the trap is not set (after DARA signal has been detected), dynamic reversal and equipment check error will be set. The tape is stopped and UCK is generated if BOT is detected.

5.13.9 Crease check

This check is executed if block format error is detected in RD, BRD commands and if HBLK signal is detected in SP, BSP commands.

When DIBG is detected due to tape crease etc, the tape should be moved to correct IBG.

In the BSP command following the Write command, the tape is moved till detecting IBG. (continuous DIBG signal of approx. 5 mm in 6250 mode and approx. 7 mm in 1600 mode) In this case the tape may have passed IBG. Therefore, the tape is run back through a few TP's and the head is stopped at mid point in IBG. In all other cases crease check is carried out for approx 2 mm. In this case, IBG is confirmed while MTU-stop-delay.

5.13.10 NRZI read

If it is not a tape block, data transfer request will be issued. Identification of data, CRC and LRC bytes, is carried out by the hardware.

5.13.11 Write operation

Detecting a GAPC signal, also may execute a velocity retry. WOK signal is set and then the Write processing is started.

First the timer is set to tachpulse count mode, overflow of this timer occurs if WOK signal is not reset ('0') within 15 m.

If HNOIS signal is not set within 70 QTP after WOK signal has been reset, No-Block-Detect error and Equipment Check is set. After detecting NHOIS signal, microprogram waits for PREA signal '1'. If DBOB signal is reset before PREA signal, STRDC signal is set ('1'). Start Read Check is set in this case.

If DBOB signal is reset after PREA signal but before POSA signal, partial-record error is set and Write operation is terminated.

Postamble error will be set, if DBOB is reset after POSA signal but before EPOSA signal, or if EDC signal is set after EPSOA signal but before DIBG signal.

Upon completion of a Write operation, if SLIPC signal is found to have been set, Slow Begin Read Back check will be set. On the other hand Early Begin Read Back Check will be set if NOISC signal has been set.

All the tracks are masked and the tape is stopped if a format error is detected during Read Back checking. And envelope-check and IBG-detect is added in the sense data.

5.13.12 Write tape mark operation

In write tape mark operation, WTM, ALlWT, WEC and WOK bits are set for 18 QTP (378 bit cells) in 6250 mode and for 36 QTP (126 bit cells) in 1600 mode, bits 1, 3, 4 are masked and the tape mark code is recorded.

A check is then carried out to make sure that HTM signal is detected within 70 QTP.

Here the retry operation is done up to 7 times, if an error is detected. In case of Retry Over, Write Tape Mark Check and Equipment Check are set and also UCK is generated.

In the 800 BPI mode, the two bytes of tape mark code are recorded by the hardware. Bits 0, 1, 2, 4, 5 and 8 are masked, and WTM and WOK bits are set for this purpose.

5.13.13 Sense data generation

All the hardware bits related to execution of WT, LWR, RD and BRD command are checked. Then the appropriate sense bits for the recording density and commands (as shown in Table 5.5) are set in the sense byte stack area (SB0~SB23 Register).

Table 5.5 Summary of sense generating (1/4)

Register Bit	Check Description	6250			1600			800			Consequent Sense Bits	Note -( ): Release Check, +( ): Additional Check
		WT LWR	RD	BRD	WT LWR	RD	BRD	WT LWR	RD	BRD		
BOPC	(Bus out parity check) Parity Error in Channel Data	o			o			o			BOC	
	Parity Error in the feed back data via interface receiver		o	o		o	o		o	o	DCK, PCMP	-(VRCE)
ABRPC	(A/B Reg parity check) Parity Error in Send Data		o	o		o	o		o	o	DCK, PCMP	-(VRCE)
XBIC	(XFR Buffer input data check) Parity Error in Buffer Input Data	o	o	o	o	o	o	o	o	o	DCK, PCMP	-(BOC) for WT, LWR, -(VRCE) for RD
WBOC	(Write bus out check) Parity Error in Write Data Bus	o			o			o			ACK, PCMP	-(BOC)
WTVRC	(Wright Trigger VRC) Parity Error in Modulated Data	o			o			o			DCK, WVRC	
DROE	(Drop out error) TSNS=0 with more than 1 Track while PHOK=1.	⊖			o						DCK, EVC	⊖ : does not cause DCK

Table 5.5 Summary of sense generating (2/4)

Register Bit	Check Description	6250			1600			800			Consequent Sense Bits	Note -( ): Release Check, +( ): Additional Check
		WT LWR	RD	BRD	WT LWR	RD	BRD	WT LWR	RD	BRD		
DBCK	(Deskewing Buffer Check) R0 Counter ≠ 00 at the time of resynchronization.	o	o								DCK, PCMP	
SKWE	(Skew error) Skew greater than 14 bit cells	o									DCK, SKWE	
	Skew greater than 2 bit cells				o							
	Excessive skew on 1st Bit							o				
	Skew greater than 30 bit cells		o	o		o	o					
MLTE	(Multi track error) Pointer = 1 for more than 2 tracks	o			o	o	o				DCK MLTE	
	Pointer = 1 for more than three tracks		⊖	⊖								⊖ : does not cause DCK.
FSAE	(Postamble error) More than 3TRK of '0' data detected within 35 bit cells after POSTA.	o	o	o							DCK POSAG	
	Data '1' detected within. 31 bit cells for WT, LWR and 22 bit cells for RD/BRD after POSTA.				o	o	o					

Table 5.5 Summary of sense generating (3/4)

Register Bit	Check Description	6250			1600			800			Consequent Sense Bits	Note -( ): Release Check, +( ): Additional Check
		WT LWR	RD	BRD	WT LWR	RD	BRD	WT LWR	RD	BRD		
VRC	(VRC) Uncorrectable data byte	o	o	o		o	o				DCK VRCE	
	Parity Error in data after correction								o	o		
	Parity Error in Data				o			o				
LRCE	(LRC error) Track Direction Parity Error							o	o	o	DCK LRCE	
1 or 2	When 1, 2 track correction is executed	⊖	⊖	⊖		⊖	⊖				1 or 2	⊖ : Does not cause DCK
A ≠ B	(CRCA ≠ CRCB) Input/Output data from the buffer does not match.	o	o	o	o	o	o	o	o	o	DCK XBCK PCMP	-(OVRN) -(BOC) When WT, UCK.
B ≠ C	(CRCB ≠ CRCC) Write data does not match with after read data.				o			o			DCK CRC CRC III	
B ≠ D	(CRCB ≠ CRCD) Aux CRC read out does not match with Write/Read Data.	o	o								DCK CRC CRC III	-(OVRN)
*MCRC	(Unmatch CRC) CRC Error in Read Data	o	o	o				o	o	o	DCK CRC	
*MCRCC	(Unmatch CRCC) CRCC Error in Read Data.			o							DCK CRC CRC III	

Table 5.5 Summary of sense generating (4/4)

Register Bit	Check Description	6250			1600			800			Consequent Sense Bits	Note -( ): Release Check, +( ): Additional Check
		WT LWR	RD	BRD	WT LWR	RD	BRD	WT LWR	RD	BRD		
OVRN	(Over Run) Lock of data in XFR buffer before completion of data transfer.	o			o			o			OVRN	-(DCK)
	Buffer Overflow		o	o		o	o		o	o		
OVRN2	Abnormal handshake in Offset Interlock Mode.	o	o	o	o	o	o	o	o	o		

5.13.14 Sense command operation

SNS command (04), SNS & CNTRSV commands (F4), SNS & CNTRLS (D4), SNS & TURSV (B4), SNS & TURLS (94) and UR command (14) transfer the sense data stored in MTC and the sense data about MTU status to the channel. In order to execute this operation the MTC microprogram sets DXF1 and MPRD bits in XFCTL register and sets sense data bytes sequentially in the CHBI register. Moreover, in SNS & CNTRSV, or in SNS & CNTRLS commands, the RTCTL register's CRVA or CRVB bits are set and reset to reserve and release the MTC prior to transmitting sense data. In SNS & TURSV and SNS & TURLS commands, the DVRSV bit of the DVRSV register is set/reset in order to reserve or release required MTU.

(1) Transfer clock

The channel buffer clock for sense data transfer, is generated in the clock mode; 6250 BPI, 200 IPS mode.

This keeps the sense data transfer time to the minimum.

The original clock mode is restored after the sense command has been completed.

(2) Not Operational

MTU is assumed to be in Not Operational status in the following cases.

- o Operator panel MTU Enable/Disable switch is set to Disable side (DVSEL register *DVENB Bit = 1).
- o DUAL, Hidencity bits of MTU Sense Byte 1 are both '0' (MTU not connected to the MTC or power supply OFF).

Some MTC sense data bits may be unpredictable when MTU is in Not-Capable status. In this case the IRQ bit (of sense byte 0) is set and TUSTA, TUSTB bits (sense byte 1) are reset ('0').

(3) LENQ Set

Corresponding LENQ bit is set (refer to subsection 5.5.2) when sense data IRQ bit (of sense byte 0), is transmitted.

(4) MTU Sense Data

In all cases other than (2) above, current MTU status is checked and the corresponding sense bit is set/reset as required.

(5) TUCK Reset

When the MTU TUCK bit is '1', MTU error code is stored in sense byte 2.

EQC bit is set if Load Failure (LDF) is not set in MTU error code. After fetching MTU error code, MTU and TUCK status are reset.

(6) MTC sense data

In addition to the sense data bits set in the previous operations, the following bits showing the status of MTC are generated.

- New Subsystem (SSB5, Bit 0, 1)
  Permanently '0', '1'.
- 6250 RPI MTC (SSB9, Bit 4)
  Permanently '1'
- SMTC (SSB9, Bit 5)
  Permanently '1'
- MTU Reserved, MTC Reserved (SSB9, Bits 6, 7)
- Error Count (SSB13)
- 2CHSW, 800FT, MTCEC LEVEL (SSB17)
- PFD (SSB19); Primed for DVE

(7) Sense Byte Stack Area Clear

Sense Byte Stack Area (LSR SB0~SB23 registers) is cleared upon completion of sense operation.

5.13.15 UR command operation

The SNS commands described in Subsection 5.13.14 are executed after the following operations.

(1) If the operator panel ENABLE/DISABLE switch of the MTU to be reserved is set to DISABLE, MTU Reserved bit (SSB9, bit 6) is reset and only SNS command is executed. If the switch is set to ENABLE, operations from (2) onwards are carried out.

(2) If another MTC is using the MTU or has reserved the MTU (DVBSY bit = 1), a "UR reset" is issued to another MTC. If DUBSY bit is not reset within designated seconds, EQC error is assumed and SNS command operation is executed.

UR reset request is released when DVBSY bit is reset '0' and the following operation is executed.

(3) If the required MTU has been reserved by its own channel interface, only SNS command operation is executed.

(4) If the required MTU is reserved from the interface on the opposite side, the RSV bit (RSVA or RSVB) of the interface on the opposite side and the inquiry bit are reset. Then, RSV bit of its own interface is set.

(5) If the required MTU, has not been reserved by any of its own MTC interface routes, the RSV bit of the inquiry register is set (RSVA or RSVB). Simultaneously DVRSV bit of the DVRSV register corresponding to the MTU is also set.

Table 5.6 UR command

Environment at the time UR command is issued	UR Command Operation
Sense Data or Status at the device with a different MTU address is pending	'CUB'
Status is pending at the same MTU address	BSY + Pending Status
MTC is linked to the interface route on the opposite side	'CUB'
MTC has been reserved by the interface route on the opposite side	'CUB'
Issued during Command Chain	'UCK'
Issued in CPBL Mode	'UCK'
Required MTU is disabled	(1) Cannot be Reserved
Busy with other MTC	(2) Using "UR reset", reserved to its own route forcedly.
MTU has been reserved by its own interface route	(3) Nothing
MTU has been reserved by the opposite side interface route	(4) Reservation from opposite side released and reserved by its own route
MTU not reserved by any route	(5) Reserved by its own route.

5.13.16 Sense I/O command operation

This command fetches the MTU sense byte, identifies the type of device by reference to EXTF, VEL0, VEL1, 6250 TU, DUAL sense bits and then transmits the I/O type code (7 bytes) as shown in Table 5.7.

Table 5.7

MTU Device Type Name	Identification Condition					Block Detected						
	EXTF	VEL0	VEL1	6250 TU	DUAL	1	2	3	4	5	6	7
3241/42/44	1	1	1	1	X	FF	38	03	02	F6	17	AB
3243	1	1	1	0	X	FF	38	03	02	F6	17	E0
3261/62/66	1	0	0	1	X	FF	38	03	02	F6	18	AB
3265	1	0	0	0	X	FF	38	03	02	F6	18	E0
Not equipped	0	0	0	1	X	FF	38	03	02	00	00	00

MTC sense byte stack area is cleared (SB0~SB23 register) after sending I/O type code.

5.14 High Speed Mode

An MTU with High-Speed feature, upon receipt of a set-high-speed command (SHSP), sets the MTU to high speed mode.

An MTU is in normal mode when the power supply is turned ON. High speed mode is reset after unloading or if load button is pressed after the vacuum has dropped. If a system reset request is issued when an MTU is ready, the high speed mode will be reset. The tape speed in start/stop mode (normal speed mode) is increased to 125 IPS in a 75 IPS device and to 200 IPS in a 125 IPS device. The speed is also increased for Read/Write processing. If a command is reissued within the reinstruction time, the processing is not stopped as IBG but streaming operation is continued.

5.14.1 Start/Stop characteristics

The time and distance required by a tape to achieve stable speed from stop position to normal speed and vice a versa are shown in Table 5.8.

Table 5.8 Start/Stop characteristics

MTU Type	Operation Mode	Start Characteristics		Stop Characteristics	
		Time(ms)	Length(QTP)	Time(ms)	Length(QTP)
200/125 IPS	Normal Mode	1.2	32	1.4	36
	High speed Mode	2.5	106	2.5	106
125/75 IPS	Normal Mode	2.0	32	2.3	36
	High speed Mode	3.3	88	2.7	106
200 IPS	Normal Mode		59		51

In normal speeds, the write or read head may be stopped in IBG area. However in the high speed mode, as the braking distance is greater (start/stop), repositioning of the head must be carried out (unless streaming operation is continued). In this case the Write head stops within 0.5 inches from the starting point of the next block towards BOT side.

5.14.2 High speed operation

(1) Read status

If the next command is received within the time required to pass IBG, streaming operation can be continued without repositioning cycle. However if the next command is not received till the Read head detects the next block, repositioning cycle is activated and the tape is wound back to wait point. Moreover, if the next block cannot be detected within 0.6 inches, repositioning cycle is activated.

MTC reads data only while the gap control signal (GAPC) is '1'. A data block transmitted to MTC from MTU while GAPC signal is '0' should not be object of operation. These are reappeared data block during reposition cycle.

(2) Write status

As End Status is not reported till the read head detects IBG (in Write processing), the command reinstruction time equals the time required to run the distance obtained by deducting R/W head gap from IBG length.

The tape is stopped after a certain length when command overrun condition occurs. At this stage, the current applied to the write or erase head is cut off and degause operation is carried out for about 3 ms. This degause point is such that the erase head will be capable of erasing the write head trace of the degause when the erase current is turned on at the next operation.

Then the tape is move back to the wait point. At this stage MTU external and internal status are Write and Read respectively. If Go Tag is set after command instruction time has elapsed, the tape is then driven forward. Erase current is turned ON at this time. As the tape runs through predetermined length, the read head passes over the previous block, IBG is detected and write current is turned ON. Thus, MTC may start Write operation after WOK signal and the GAPC signal.

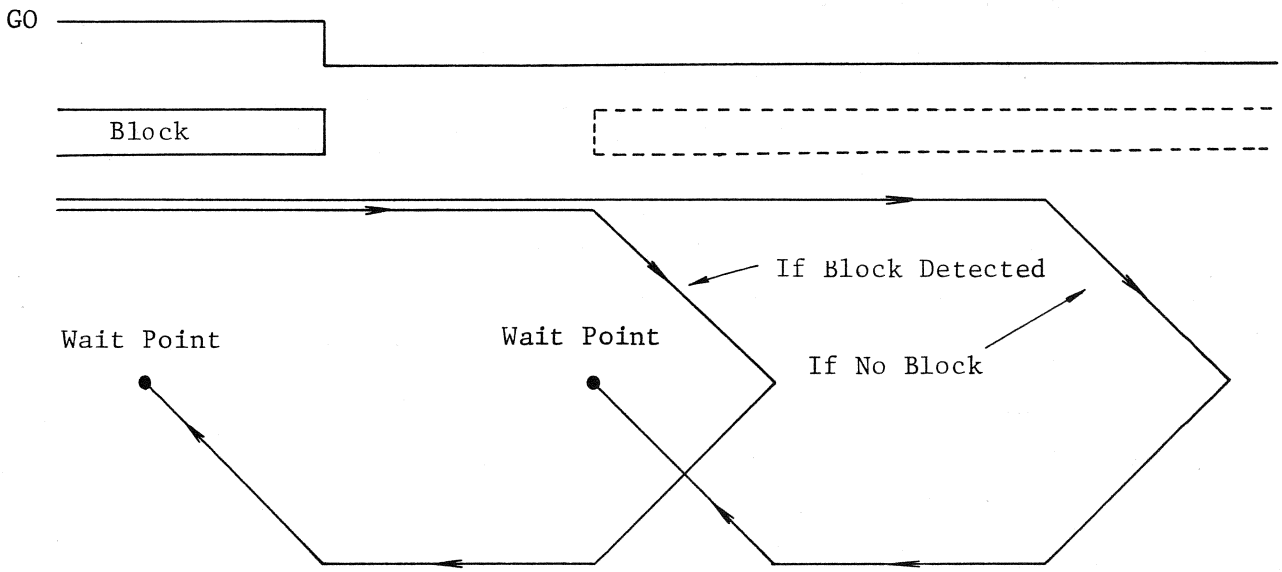


Figure 5.2 Reposition cycle (Read operation)

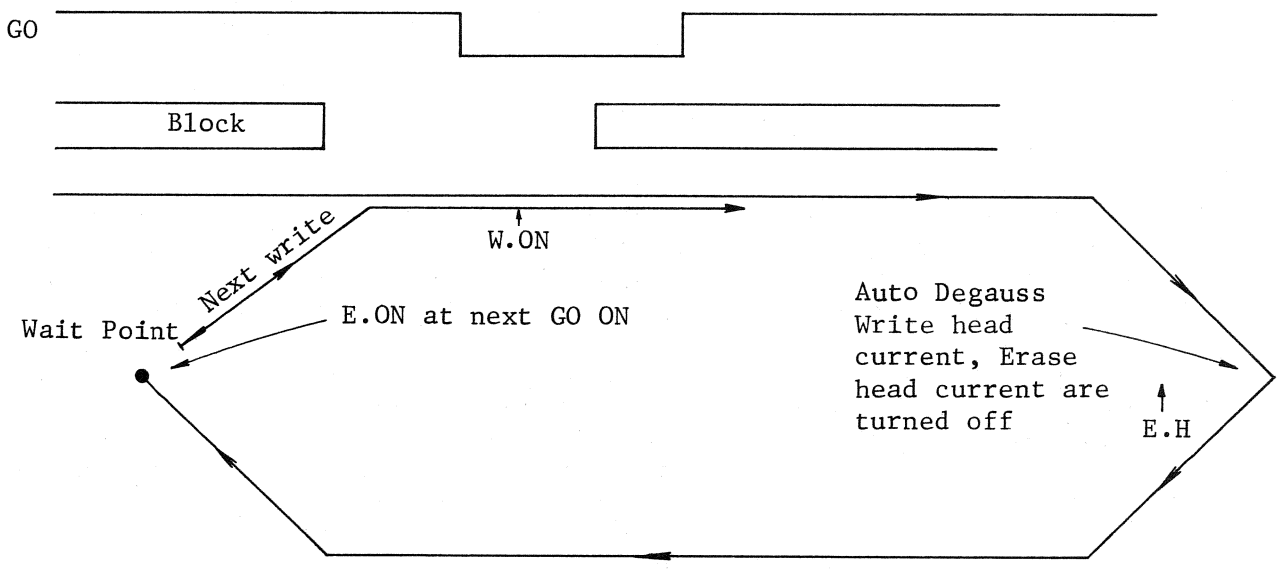


Figure 5.3 Reposition cycle (Write operation)

5.14.3 Changing status in high speed mode

In high speed mode, the Tape is stopped and a response to a change of status request is sent to MTC. Then the operations shown in Figures 5.4 and 5.6 are executed when the Go Tag is set.

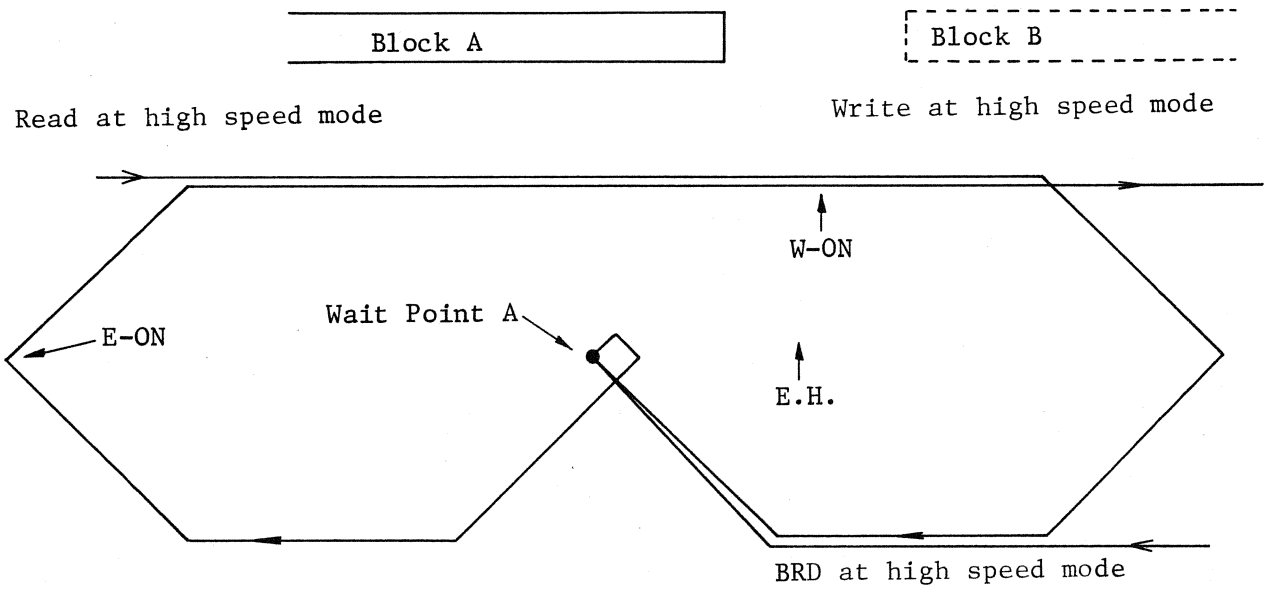


Figure 5.4 Upon changing from Read to Write status

(1) Operation as shown in Figure 5.4 is executed if a Write type command is issued to an MTU which has just processed a Read type command. For example, if set-write-status is specified to the MTU after reading block A, the MTU runs for 6 inches after MTC Go flag is reset. If a block is detected within this length, MTU decelerates and returns to wait point A. Response is sent to MTC (for Set Write Status) from this point. Now, forward hitch is executed when the Go Tag is set. Then the tape is run backwards so that the erase head covers the entire block B (to be erased). After this, the tape is run forward with erase current ON. Write current is off till this point. Write current is turned ON after read head passes over the above block A.

(2) If a Read Backward type command is issued to an MTU after processing a Write type command, Auto degause is executed after running for a specific length, the tape is run back to the wait point and then a normal backward operation is executed. Therefore additional erase in a normal operation is not required.

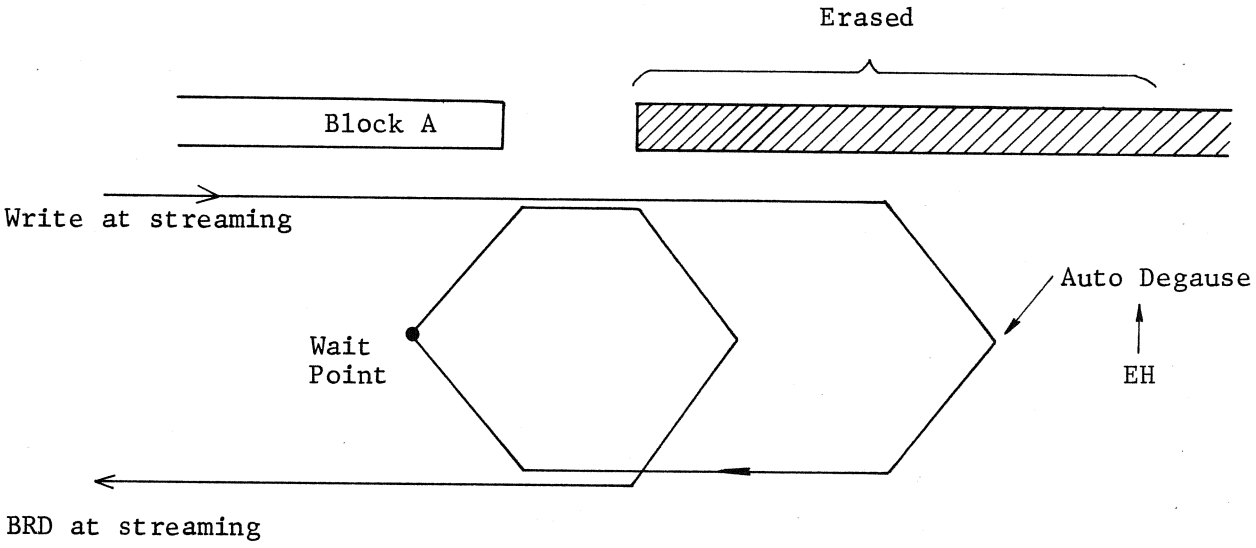


Figure 5.5 Backward Read after Write

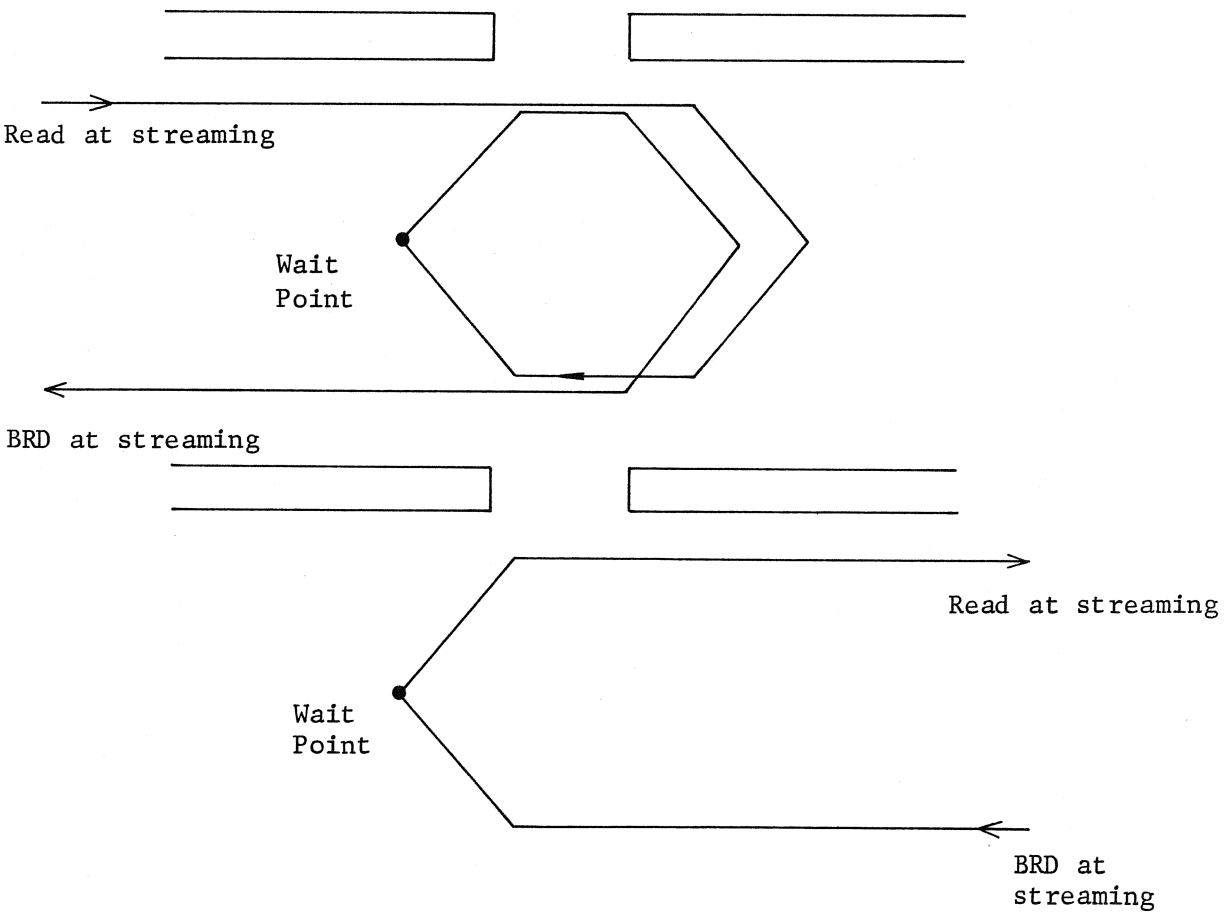


Figure 5.6 Changing from FWD→BWD, BWD→FWD

5.14.4 Command operations in high speed mode

(1) Write operations

In case of Write type commands, the gap control signal is set at the point of 11 QTPs before normal IBG end in 6250 BPI mode and 360 QTPs before normal IBG end in 1600/800 BPI mode. Therefore WOK signal should be set after QTPs from the above gap control signal. However, if streaming is not continued, repositioning operation is carried out from the time the GO Tag is set till the Gap Control Signal.

(2) Read operation

In a normal Read operation, ROK signal is set at the point of 20 QTPs after the Go Tag is set. Block Read operation is started then. However ROK signal should be set after the gap control signal. If there is no repositioning cycle, the gap control signal will be set when the read head is in intermediate IBG position.

5.15 MTU Communication Register

Four registers that can be accessed by MTC are provided in MTU. These registers are used as a common memory in device. Application of these registers are described in this section.

MTC accesses these registers using command-tag operation. The register can then be read in Bus-In register. Data is entered in half byte units. Register address is entered in the upper four bits while Write data is entered in the lower four bits. This is illustrated in Figure 5.7.

This register is reset (All '0's) when the power supply is turned ON. It remains unchanged even if reset key is pressed.

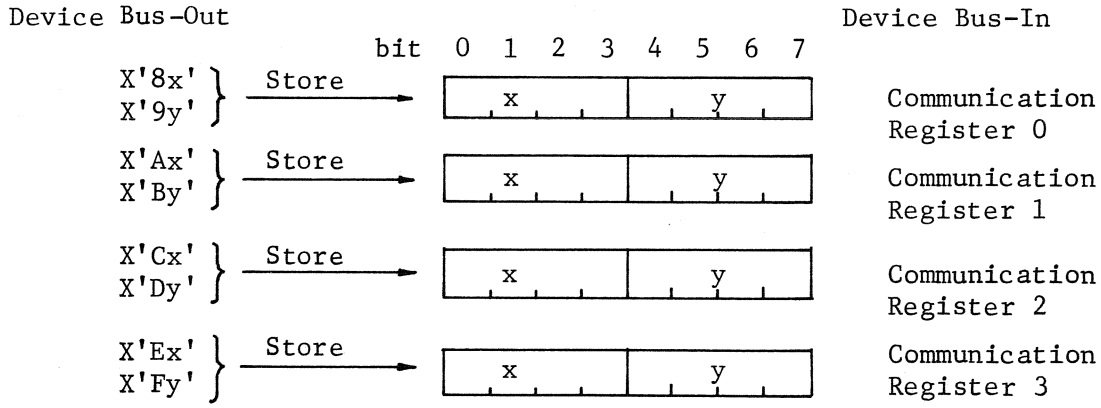


Figure 5.7 Communication register

5.15.1 Register definition

Registers are assigned as in Figure 5.8.

Communication Register	Bit 0	1	2	3	4	5	6	7
Register 0	Write Error Counter							
Register 1	Not used		Retry Counter		Not Used		Long IBG	
Register 2	VLDCNT	Position Counter (Upper)						
Register 3	Position Counter (Lower)							

VLDCNT: Valid Position Count

Figure 5.8 Register assignment

5.15.2 Write Error Counter (WEC)

In the 6250/1600 BPI mode, the counter is advanced by +1 when drop out error is detected in a write command operation.

Set-error-mark is issued to MTU at a count of 96 in 6250 BPI mode and a count of 32 in 1600/800 BPI mode.

This counter is cleared when BRD, REW and UNL commands are executed. It is reset when starting a BOT operation.

In the 800 BPI mode, this counter is used to count Write errors (VRC, LRC, or CRC).

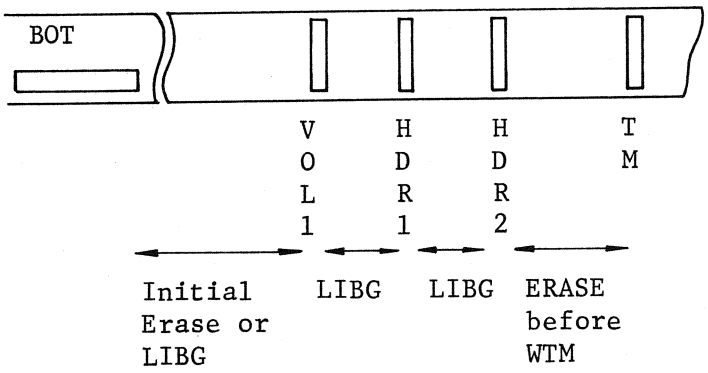
5.15.3 Retry Counter (RCNT)

This is a two bit counter used for error retry count in read or read backward commands in high speed mode.

This counter is set to '00' when there are no errors in a Read operation. This counter is advanced by +1 when UCK is generated. Read operation may be executed in high speed mode when the retry counter is at '00' or '01'. However, if this counter is at '10' or '11', MTC issues a reset high speed mode request, and the Read operation is executed in normal mode. As soon as the Read operation is completed, MTC issues a set high speed mode request. At this stage, high speed mode is restored.

5.15.4 Long IBG Counter (LIBG)

This counter enables to lengthen the IBG of volume label, header label, EOF label etc. This counter is set to '11' when starting Write from BOT. The counter is decreased 1 when a Write command is completed normally. However the counter will not be underflowed from '00'. Unless this long IBG counter is set to '00', the IBG length is longer than normal IBG by one inch.



Note: One inch tape erase is executed instead of initial erase in compatible mode (CMPBL = 1).

Figure 5.9 Long IBG

5.15.5 Position counter

This counter is used to check if the head has been positioned correctly in Back Space and Space commands executed for error retry in Read, Read Backward and Write commands. The positioning is checked by the length through which the tape has run. This checking can improve the reliability of error retry processing. This counter counts the Tps during RD, BRD and WRT commands, and MTC stores them in DCK, OVRN and BOC.

Count is started in Read commands after detecting HBLK signal. The count is continued till the end of crease check after detecting DIBG signal. Count is started in the Write command when WOK signal is set and continued till Go Tag is reset.

In SP or BSP (error retry) commands, the counter is started after GAPC signal is set. The counting is continued till the end of crease checking. At this stage, the count is compared with the count from position counter. If the difference between the two (difference in crease length, R/W Head Gap, Add erase etc.) is greater than $\pm$64 TP, Missing Position error is set (sense byte 11, bit 1).

This counter is a 15 bit counter and is capable of counting upto 32 KTP. If the counter overflows, VLDCNT is reset ('0').

VLDCNT is reset after executing RD and BRD commands in high speed mode. VLDCNT count is reset ('0') if the command to be executed has the same direction as the preceding command. Counter value may not be compared if VLDCNT is '0'.

5.16 Tag Control

MTC controls the MTU using three tag lines (Status Tag, Control Tag and Go Tag), nine control data lines (DVB00 to DVB08) and one strobe signal line (TAGVL). Microprogram uses these to specify the required operation.

Various subroutines have been provided for control and check of the selected MTU. These subroutines are used by the command operation routines repeatly. These subroutines set control data in DVB0 register and generate the required Tag signals. They also scan the MTU to make sure that the required operations are started and completed within the specified time. If an error is detected in MTU Tag control operation, the error data is stored in the sense data and the processing is branched to command operation terminate routine.

Tag Control details are given in Table 5.9.

Table 5.9 Tag control

Function	Manipulation			Response Confirmation	Time out	Sense Byte in Case of Errors
	DVBO	STSTAG	CTLTAG			
Set Write Status	10	1	0	ERS=FWD=WRS=1 BWD=LWR=0	1500 ms	STRJ
Set Erase Status	80	1	0	ERS=FWD=1 BWD=LWR=0	"	"
Set Forward Read	40	1	0	FWD=1 ERS=BWD=WRS=LWR=0	"	"
Set Backward Read	20	1	0	BWD=1 ERS=FWD=WRS=LWR=0	"	"
Set LWR Status	01	1	0	LWR=1	500 ms	"
Reset LWR Status	00	1	0	LWR=0	"	"
Set GCR Status	04	1	0	1600=0	"	"
Set PE Status	02	1	0	1600=1, SAGC=0	"	"
Set NRZ Status	04	1	0	1600=0	"	"
Set LWR2 Status	08	1	1	LWR2=1	500 ms	CMRJ
Reset LWR2 Status	09	1	1	LWR=0	"	"
Set Low Slice Level	0A	1	1	LWSL=1	"	"
Reset Low Slice Level	0B	1	1	LWSL=0	"	"
Set High Speed	02	1	1	STRMD=1	1513 ms	"
Reset High Speed	03	1	1	STRMD=0	"	"
Set Space File	04	1	1	RDY=0	"	"
Set Backspace File	05	1	1	RDY=0	"	"
Set Rewind	02	0	1	REW=1, RDY=0	500 ms	CTRJ
Set DSE	04	0	1	DSE=1, RDY=0	"	"
Set Unload	01	0	1	UNL=1, RDY=0	"	"
Set Error Mark	08	0	1	EMK=1	"	"
Reset TU	08	1	0	TUC=0, WT=0	10 µs (100 µs)	STRJ

5.17 Offline Service Routine

CE panel may be employed to manually execute various commands. Moreover this routine allows to repeat commands, automatic retry upon detection of particular end status, stopping of processing and scanning to enable serial execution of command in MTU. The offline service routine is provided to control these functions. The offline service cycle is started when the CE panel ONL/OFL switch is set to OFL and the SSS switch is turned ON. At this stage, a trap is set at address '100' in the microprogram. The control is then transferred to the trap decode routine. The trap decoding routine starts offline service if no other traps are found.

As shown in Figure 5.10, when a command operation is completed and end status is generated, this status is checked by branching to the offline service routine prior to going into idle status. The next command operation is started in accordance with the specified control function (command code changing, MTU address increment, Go Down Time etc), or the system goes into idle status upon completion of the service cycle.

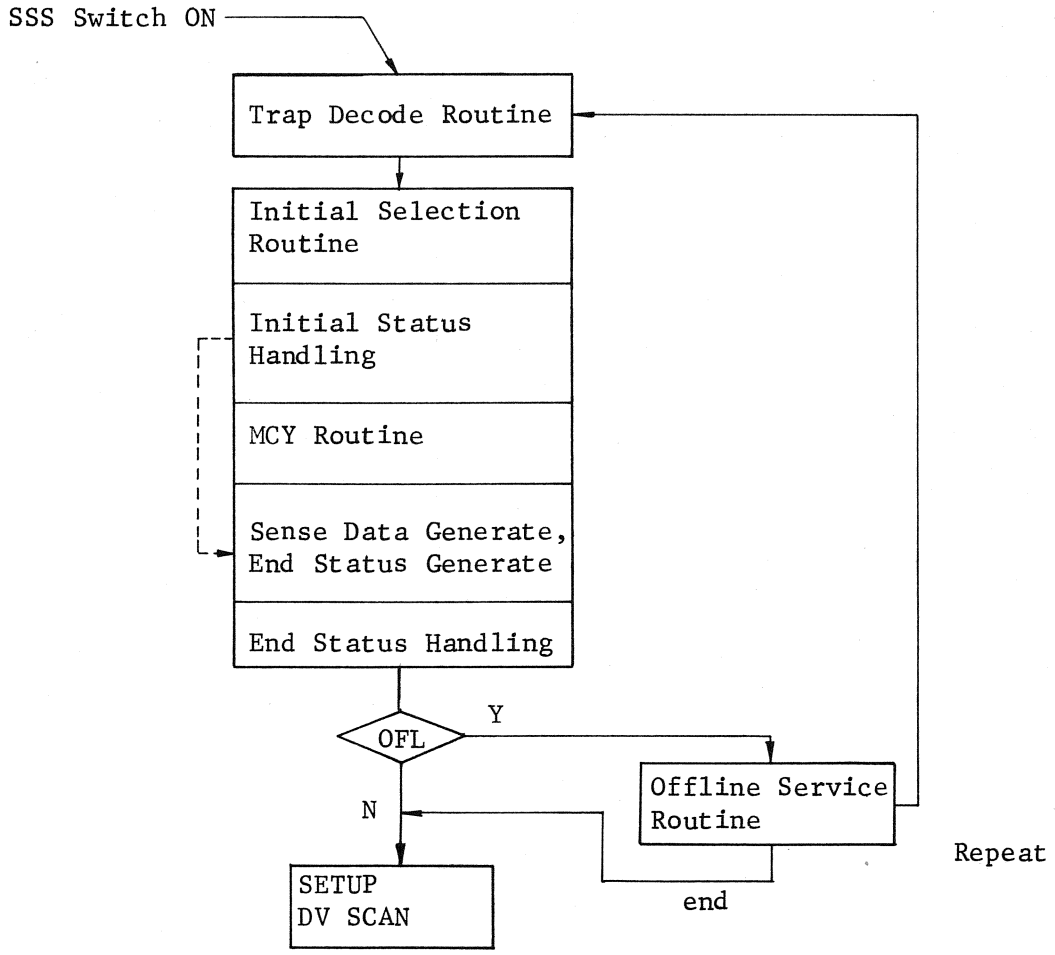


Figure 5.10 Offline service cycle

Table 5.10 Offline service function specification register

Register Name	SDIA0	SDIA1	SDIA2	SDIA3	OFLCNT	OFLCMD	OFLDVA	BCT
Address	38	39	3A	3B	3C	3D	3E	3F
Bit 0	DMW/DMR				STP.UCK		SBC	
1	MARG	INV	.MASK track		RPS.UCK			Byte Count
2	IPOST/XFR		.Marginal Code	GDT lower	STP.UEX	CMD Code	(RPSCY)	
3	GDT				REW.UEX		(REVCY)	
4	IPRE/MARA		.GDT Upper		REV.UEX		(OFSCY)	
5	SLWR	MASKP			RPS		OFDVA0	
6	MASK				REPEAT		OFDVA1	
7	TMTC				TUSCAN		OFDVA2	

Offline service function is specified by storing the required data in the registers shown in Table 5.10.

(1) SDIA0 to SIDA3 are the same as the 4 byte diagnostic flag specified in Set-Diagnose command.

When MTC is in offline status, the specified diagnostic operation may be carried out by executing the command operation without chaining by SDIA command. The SDIA data once set, is not to be altered till MTC is set to online status.

(2) Tape unit scan

When the OFLCNT register TUNCAN bit is set to '1', the OFLDVA register OFLDVA0-2 bits are advanced by +1. If repeat bit has also been set '1', commands are issued serially to all MTUs.

(3) Repeat

When OFLCNT register, REPEAT bit is reset '0', a command is executed everytime the SSS switch is pressed.

Unless this bit is reset ('0'), (while REPEAT bit is '1')), the command execution activated by SSS switch is repeated continuously.

(4) Reposition

The following offline repositioning operation is carried out irrespective of the end status when the OFLCNT register RPS bit is set.

The commands and addresses entered in OFLCMD and OFLDVA0-2 remain unchanged even after offline repositioning operation.

Table 5.11 Offline reposition

Commands set in OFLCMD register	Offline Reposition Operation
01 (Write)	Back Space command is executed after a Write command. However if IDBCK (ID Burst Check) at sense byte 5 bit 3 is activated, Rewind command will be executed instead of the Back Space command. And then, ERS command is executed.
02 (Read)	Back Space command follows the Read command.
0C (Backward Read)	Space command follows the Backward Read command.
Other commands	No operation.

(5) UEX function

The following operation is executed when UEX bit is included in the END status by using combinations of STP.UEX, REW.UEX, REV.UEX in OFLCNT register.

Table 5.12 UEX functions

<table>
<tr><th>STP
.UEX</th><th>REW
.UEX</th><th>REV
.UEX</th><th>UEX Function Description</th></tr>
<tr><td>1</td><td>X</td><td>X</td><td>Processing is looped within the offline service routine from the time UEX bit is turned ON till STP.UEX bit is reset ('0') or SINH is specified.</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No operation (UEX bit is not checked)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>When UEX bit is included in the end status, the OFLCMD register command codes are replaced by Reverse commands as follows:

<table>
<tr><th>Old OFLCMD</th><th>→</th><th>New OFLCMD</th></tr>
<tr><td>WT(01)</td><td>→</td><td>BRD(0C)</td></tr>
<tr><td>RD(02)</td><td>→</td><td>"</td></tr>
<tr><td>BRD(0C)</td><td>→</td><td>RD(02)</td></tr>
<tr><td>SP(37)</td><td>→</td><td>BSP(27)</td></tr>
<tr><td>BSP(27)</td><td>→</td><td>SP(37)</td></tr>
<tr><td>ERS(17)</td><td>→</td><td>BRD(0C)</td></tr>
<tr><td>WTM(1F)</td><td>→</td><td>BSPF(2F)</td></tr>
<tr><td>DSE(97)</td><td>→</td><td>BSPF(2F)</td></tr>
<tr><td>NOP(03)</td><td>→</td><td>BRD(0C)</td></tr>
<tr><td>Others</td><td>→</td><td>Not changed</td></tr>
</table>
</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Rewind Command is issued when UEX bit is included in the end status.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Rewinds MTU by issuing a Rewind command when UEX bit is included in the end status. Then, MTUs are reversed from Normal Speed to High Speed or from High Speed Mode to Normal Speed.</td></tr>
</table>

(6) UCK function

If UCK bit is included in End Status, the operations shown in the following Table 5.13 are carried out. The operations are specified by combinations of STP.UCK, RPS.UCK bits. ERRF lamp is turned ON when the UCK bit is set.

Table 5.13 UCK functions

STP .UCK	RPS .UCK	UCK Function Description
0	0	UCK bit is not checked.
0	1	The repositioning operation described in (4) is executed when the UCK bit is set. Any errors in the repositioning operations are ignored.
1	0	When UCK bit is included in End status, Processing is looped within the offline service routine till STP.UCK bit is reset or SINH is specified.
1	1	The repositioning operation in (4) is executed when the UCK bit is set. Any new errors (UCK) during repositioning operation cause μP loop in the offline service routine till STP.UCK bit is reset '0' or SINH is specified.

(7) SINH (Start Inhibit)

When SINH bit on the CE panel is ON, commands issuing from SSS switch are inhibited.

A loop created by STP.UCK or STP.UEX bits may be released by setting the SINH bit. If SINH is turned OFF again, commands will be issued again (in case of Repeat).

Commands may be temporarily inhibited if SINH bit is set (ON) when Repaet has been specified. This facilitates temporary stopping or starting of commands in manual mode (without resetting Repeat bit).

CHAPTER 6 MAINTENANCE PANEL

6.1 Maintenance Panel

Maintenance panel is made up of eleven switches and twelve luminous diodes and does not feature a power supply. It is connected to MTC for maintenance or checking purposes. A fifty signal line flat cable is used to connect MTC. The useful operations carried out by the maintenance panel (CE panel) are as follows:

(1) Display status of signal lines and registers.

(2) Rewrites Microprogram Address Counter.

(3) Rewrite of data to registers.

(4) Address Compare and Stop µP.

(5) Address Compare and Branch µP.

(6) Address Compare and Display (register data).

(7) Address Compare and Write (to register).

(8) Microprogram stop, step and run.

(9) CS Scan.

(10) Starting offline Service Routine, specifying and execution of commands (Refer to section 5.17).

Related hardware has been described in Subsection 4.4.4. Related software is described in Section 5.17.

CHAPTER 7 DIAGNOSIS

MTC is provided with microprogram routines and hardware required for diagnosis.

MTC microprograms carry out the following diagnose operations.

7.1 Diagnostic Routine

(1) Diagnosis upon turning On the power supply

Power-on diagnose routine tests the MTC hardware when the power supply is turned ON.

The purpose of this diagnostic operation is to detect and notify the system hardware errors. As soon as the power supply is turned ON the self test routine (described in Section 5.2) is executed to verify the microprocessor. If no errors are detected, the Power-On Diagnose routine is executed. (Refer Section 5.3 (3))

(2) Processor self test

If the microprogram starts from address '000' after the power supply is turned ON, processor self test is executed. This test is also started by system reset, selective reset, CE panel ONL/OFL switch transition, and CE reset by the operator from the CE panel. Details on the tests are given in Section 5.2.

(3) Reset routine

If no errors are detected in the processor self test, the specified reset routine is executed. When LSR is reset by the reset routine, the operation is checked to make sure that LSR is cleared.

(4) Check out routine

Everytime eight MTUs have been scanned (when MTC is in idle status), the check out routine is executed. The major purpose of this routine is to test the ALU.

7.2 Diagnostic Error Termination

The errors detected in the diagnostic tests described in Section 7.1 are treated as follows.

(1) If an error is detected in MTC online mode, the system goes into wait status till the next Initial selection request is received (INS bit = '1').

At this stage, the error codes have been stored in SB22, SB23 registers (FRU code). When the next selection request is received, the desconnect-in signal is sent out to notify an error to the channel. When the channel specifies Selective Reset, disconnect-in signal is reset and Selective Reset Routine is executed.

Selective Reset is completed normally if the error is of a temporary nature. The error code indicating the cause of the error is not cleared by the selective reset routine, but ERRF bit is set (ERRF bit on the CE panel is turned ON). If a selection request is received from the channel while the ERRF bit is set, UCK status (BOC error) will be notified of commands other than the ones with sending sense data. The sense data including the error code is normally sent in response to the commands for sending sense data.

The cause of these temporary errors is thus indicated in the sense byte. ERRF bit is reset when the UCK status (Bus Out Error) is posted.

(2) MTC in offline status

MTC microprogram operation is the same as in (1). As the ERRF bit on the CE panel is turned ON in offline status, errors may be detected visually. As the cause of the error is set in registers SB22, SB23 in the form of error codes, details can be obtained by using the register display function. Error status may be reset by operation similar to online mode (this is done by executing command subsequently) or by resetting the system (e.g. CE reset).

7.3 Diagnostic Operation using CE Panel

7.3.1 Command trial

To verify various function of MTC, execute MTC command using the CE panel. Offline service routine is described in detail in Section 5.17. For details on CE panel operation procedures, refer to other manual, e.g., Maintenance Manual.

When a command is executed from the CE panel, the results of processing may be displayed by L10 ERRF lamps (set CE panel to Interface Display Mode). Offline Service Routine sets ERRF bit when the UCK is included in END status. Error details are set in SB0-SB23 sense byte stack area and may be displayed by using the register display function. The ERRF lamp will be reset when a new END status is generated (ERRF lamp indicates the results of the immediately preceding command).

UCK reposition function provided with OFL service routines may be useful to check the UCK.

7.3.2 Issuing Test MTC

Tests on the basic MTC hardware as well as tests on Read/Write data bus to MTC may be executed if necessary. These tests are carried out by executing the diagnostic command 'Test MTC' function from the CE panel.

As explained in Section 5.17, the diagnostic flag byte may be specified anytime in offline mode. Therefore SDIA command with TMTC bit (SDIA0 register bit 7) causes comprehensive diagnostic operations.

Results of those diagnostic operations are indicated in SB0-SB23 registers as sense bytes.
If some error has been detected, EQC error (UCK) is generated.

All MTUs may be tested serially by the TUSCAN function.

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