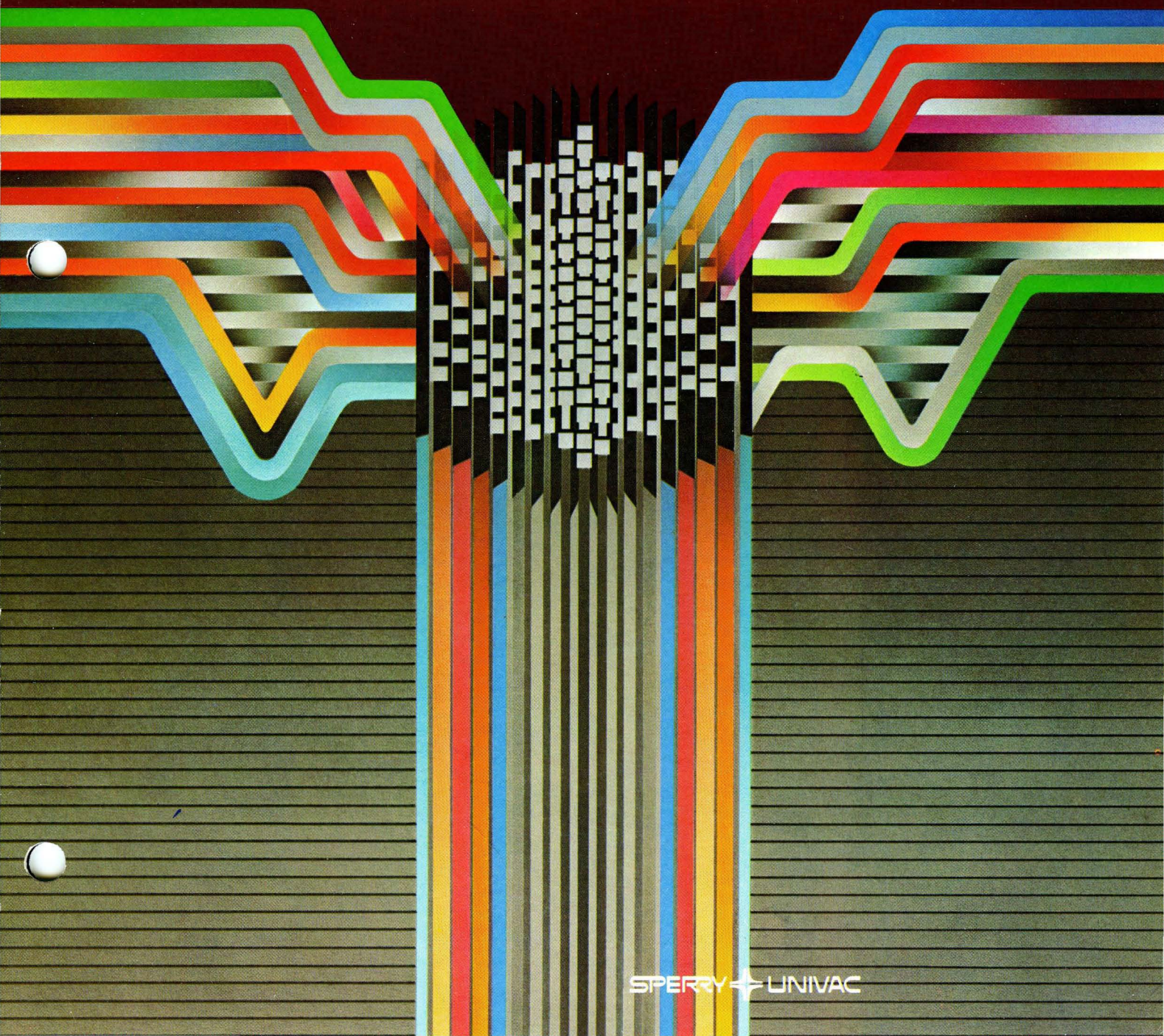
SPERRY UNIVAC
Series 1100
Vector Processing System



SPERRY UNIVAC

SPERRY UNIVAC Series 1100 systems have led the way in scientific computing for over three decades. The SPERRY UNIVAC 1100/80 Array Processing System (APS) established a new level of performance by combining the speed of vector processing with the flexibility of general purpose computing.

Based on the VPS, the SPERRY UNIVAC Series 1100 Vector Processing System (VPS) now expands that capability by providing, in a *single* system, high performance vector processing, direct support of interactive graphics and program development terminals, and sophisticated database technology.

The Vector Processing System's outstanding high performance/low cost ratio makes it the *total system solution* for:

- Seismic Data Processing
- Reservoir Simulation
- Real-Time Radar/Sonar Studies
- Circuit Design
- Frequency Spectrum Analysis
- Image Processing

GENERAL DESCRIPTION

The Vector Processing System is a high-performance scientific multi-processor available for the SPERRY UNIVAC 1100/80 computer family. This family has been widely accepted by hundreds of customers since its first delivery in 1977.

The VPS features two separate logical and physical units for scalar processing (CPUs), one or two input/output and communications processor(s) (IOU), and two vector/array processors (APUs), plus main storage of two million words (8 Mbytes) expandable to 8 million words (32 Mbytes). With two IOUs the system may be split into two separate 1X systems for uninterrupted processing during maintenance and testing. See Figure 1.

Each functional unit is attached to, and operates directly on the large central memory via high-speed Buffer Memories which operate as caches for data. The caches serve not only to transfer often used data to and from the functional units at very high speeds, but also to buffer the central memory bandwidth against extreme data request rates by the functional units. Each CPU has an 8K word buffer (32K bytes) which is expandable to 16K words, and can transfer data to the CPU and IOU logic units at 10 million words per second.

The two APUs in the VPS operate at a combined speed of up to 240 million floating point operations per second (Mflops).

Buffer memories for the two APUs are known as Array Processor Control Units (APCU) and can transfer data to and from each APU at 40 million words per second. Each IOU in the system can accommodate up to 26 high speed I/O channels.

In multiple, redundant unit configurations, the system exhibits maximum resiliency and user availability, allowing redundant units to be isolated from the configuration and restored during production without system reboot.

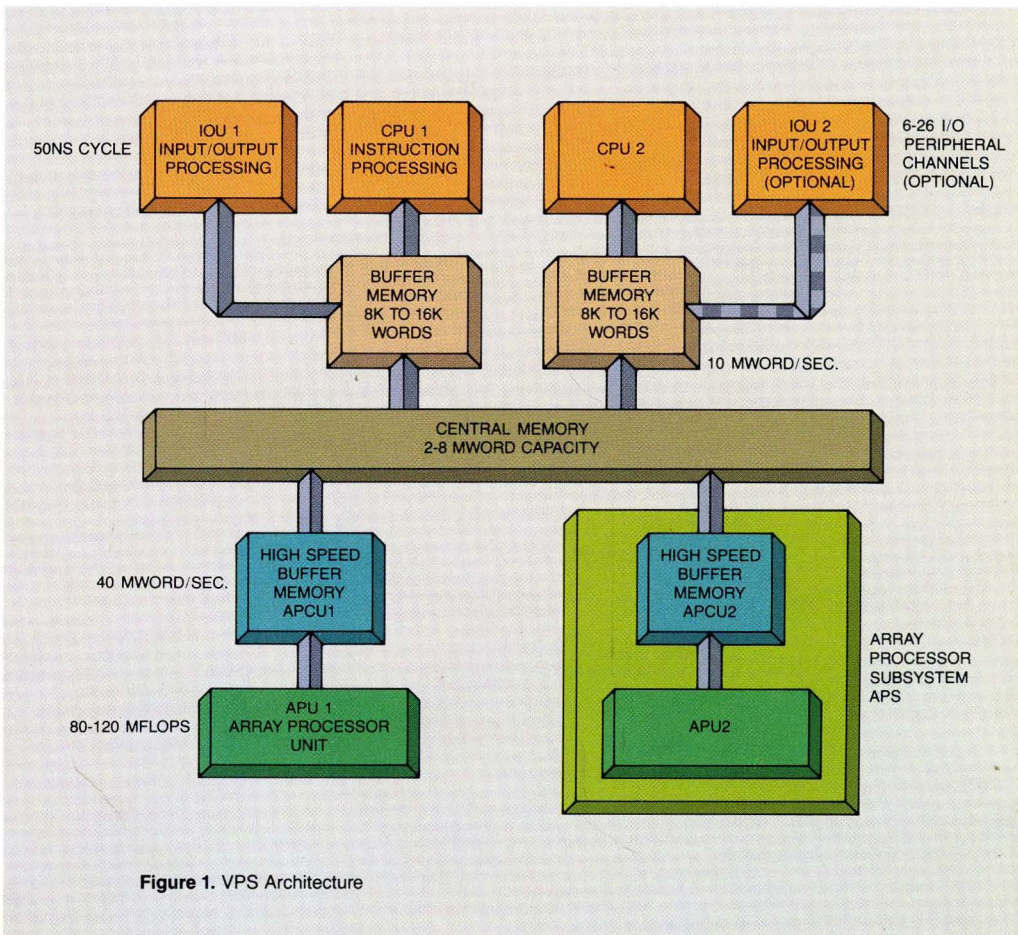


Figure 1. VPS Architecture

The CPU and IOUs are versatile functional units that directly support scalar processing and advanced peripheral configurations. See Figure 2. The entire system operates under control of the Series 1100 Operating System. The 1100 OS provides a proven, stable platform for the high vector performance of the VPS. Under control of the 1100 OS, the VPS directly supports interactive timesharing/graphics, remote job entry, real-time and batch modes of user access to any component of the system.

Each VPS contains two array processors with four major components: two Array Processor Units (APU), that connect directly to an 1100/80 system (Figure 1), and two Array Processor Control Units (APCU).

APU Architecture

The APUs consist of four control sections which interpret instructions and complete addresses; program (instruction) memory; scratchpad memory; and four pipeline arithmetic sections. (Figure 3.) Each parallel pipeline has one floating point multiplier and two Arithmetic Logic Units. (Figure 4.)

APU Specifications Summary

- Basic speed is effective 25 nanoseconds (NS) 36-bit floating point multiply-add time (four multiply and four addition results each 100 nanoseconds in correlation and convoluting multiply operations) for each APU.
- Four pipelined array arithmetic sections (Figure 4) each having one floating point multiplier and two Arithmetic Logic Units (ALU), which perform 60 arithmetic and Boolean operations on two 36-bit inputs in six categories:
  - Control
  - Logic
  - Floating Point Arithmetic
  - Fixed Point Arithmetic
  - Conversion
  - Comparison

Magnetic Tape Subsystems Characteristics

	UNISERVO 30	UNISERVO 32	UNISERVO 34	UNISERVO 36
Recording density (PE)	1600 bpi	1600 bpi	1600 bpi	1600 bpi
(NRZI)	200, 556, 800 bpi	–	–	–
(GCR)	–	6250 bpi	6250 bpi	6250 bpi
Transfer rate (PE)	320,000 fps	120,000 fps	200,000 fps	320,000 fps
(NRZI)	40,000, 111,200, 160,000 fps	–	–	–
(GCR)	–	468,750 fps	781,250 fps	1,250,000 fps
Tape speed	200 ips	75 ips	125 ips	200 ips

Legend:
bpi = bits per inch
fps = frames per second
ips = inches per second

Disk Subsystems Characteristics

CHARACTERISTIC	8430	8433	8450	8470	7053 CACHE DISK	7053 SOLID STATE DISK
Drives per subsystem	2-16	2-16	2-32	2-32	2-16	1-4
Capacity per disk pack (BYTES)	100,000,000	200,000,000	302,000,000	562,000,000	302,000,000/645,000,000	16,500,000
Average access time (in milliseconds)	27	30	23	23	1	.2
Data transfer rate (BYTES per second)	806,000	806,000	1,260,000	2,097,000	1,260,000/2,097,000	5,000,000

Figure 2. VPS Peripheral Options

Each pipeline is capable of producing a result every 100NS for effective sustainable performance levels of up to 80 megaflops (80 million floating point operations per second) per APU in suitable algorithms, with maximum performance of 120 megaflops in bursts.

- Four control processors to decode instructions, generate addressing and collect statistics
- User microprogrammable by means of 288-bit microinstructions—8K word instruction memory (expandable to 16K words)
- 65K words of vector scratchpad data memory (36-bit words plus parity, expandable to 262K words)
- Data bandwidth of up to 40 million words/second (up to 80 million words/second if local data memory is used simultaneously)
- Addressing capability of up to 6 million words per APU application (algorithm)

Floating Point Numerical Representation

The APU Arithmetic Logic Units and Multipliers produce normalized 36-bit floating point results that are identical to the 1100/80 CPU(s). This format provides a range of 10^{38} to 10^{-38} with eight decimal digit precision.

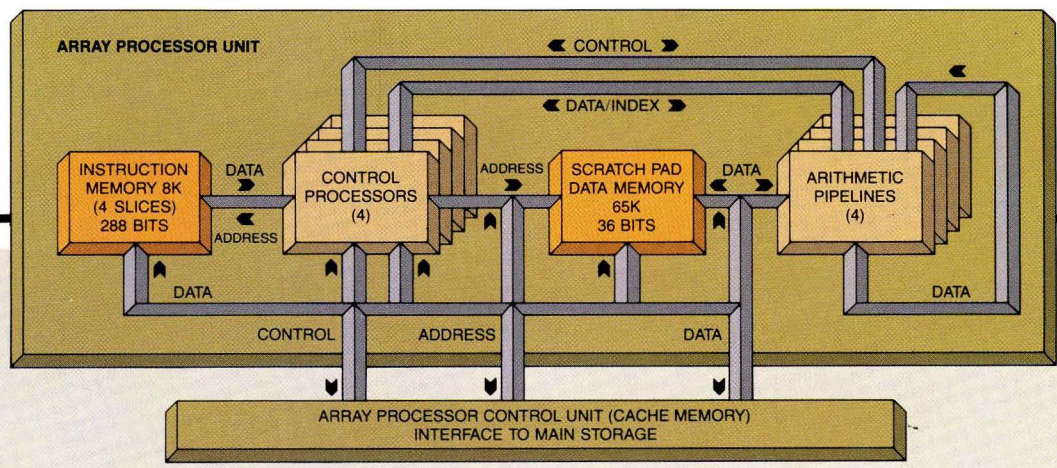


Figure 3. Array Processor Unit Architecture

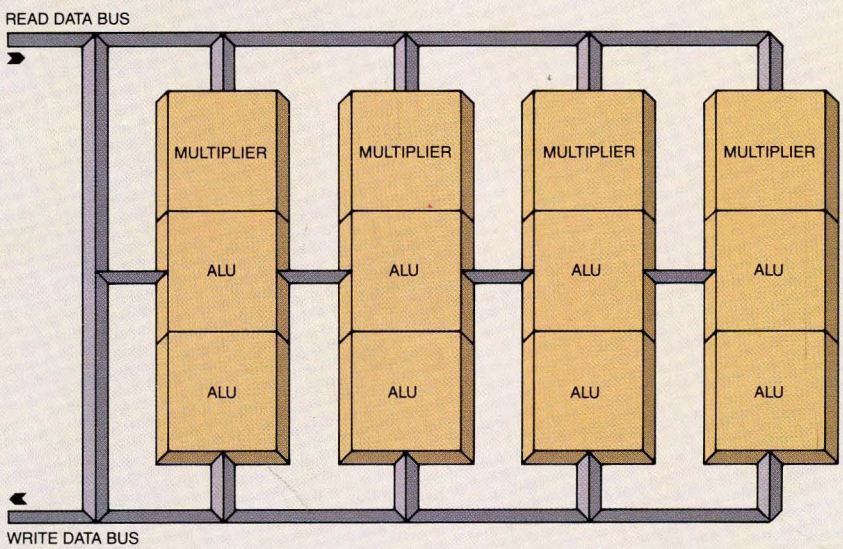


Figure 4. APU Parallel Pipeline Architecture

Seismic Performance

The VPS performs at a system throughput in excess of 190 traces per second processed in a representative seismic processing job sequence of trace input, AGC application, deconvolution, normal moveout, and stack. Figure 5. The processes operated on 2MS sample rate, 4 second records, 48 fold CDP (Common Depth Point) input data.

Reservoir Simulation Performance

The VPS can perform important computational kernels of the reduction of a D4-ordered Sparse Matrices at a system effective rate in excess of 140 Mflops. See figure 6.

Spectrum/Signal Analysis

The signal processing operation of Fast Fourier Transform operates at VPS effective system speeds of 350μs for 1024 pt. real transforms, 540μs for 1024 pt. complex transforms (two 1024 pt. complex FFTs, including unscramble operations in 1.08 milliseconds). The VPS is performing at a system effective rate of 200 Mflops during computation of the FFT inner butterflies.

In filtering operations, such as correlation and convolving multiply, each of the two APUs produce 4 36-bit multiply-add results every 100NS—a VPS system effective rate of 12.5NS/multiply-add.

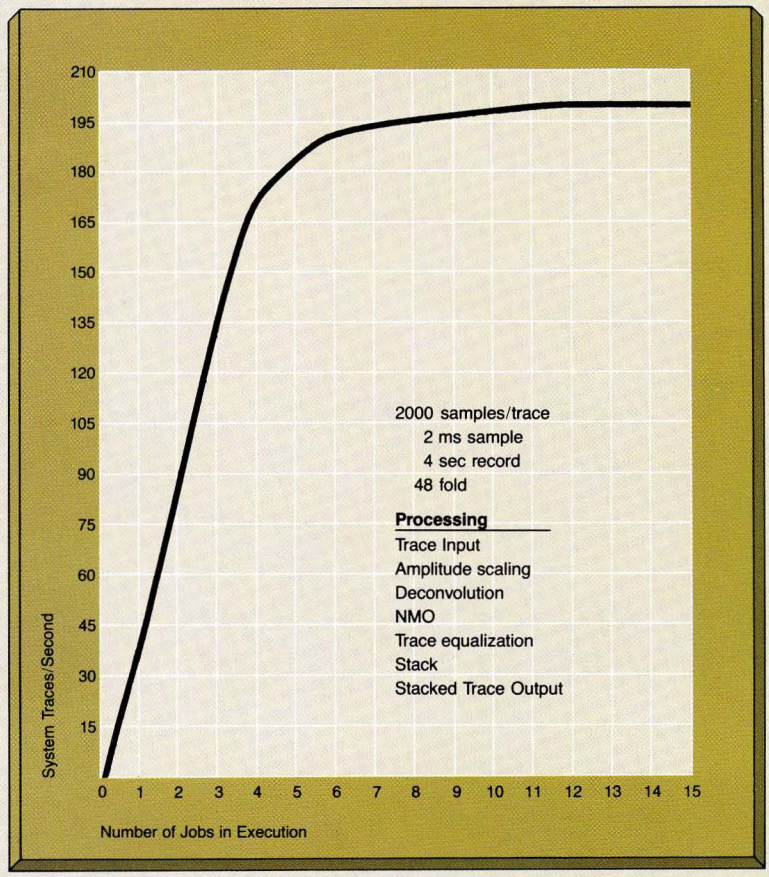


Figure 5. VPS Seismic Performance

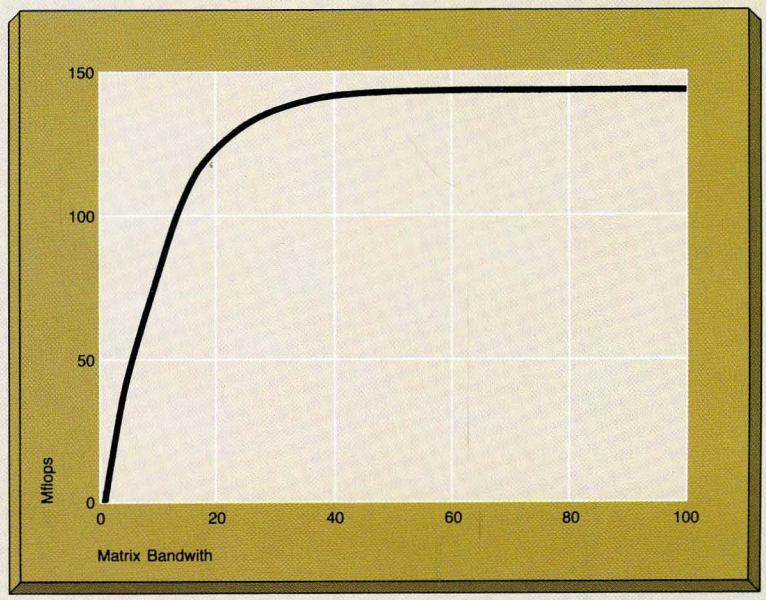


Figure 6. Inner Kernel of the Solution Routine for D4-Ordered Matrices

Computer-generated color displays help scientist identify subsurface geological formations.

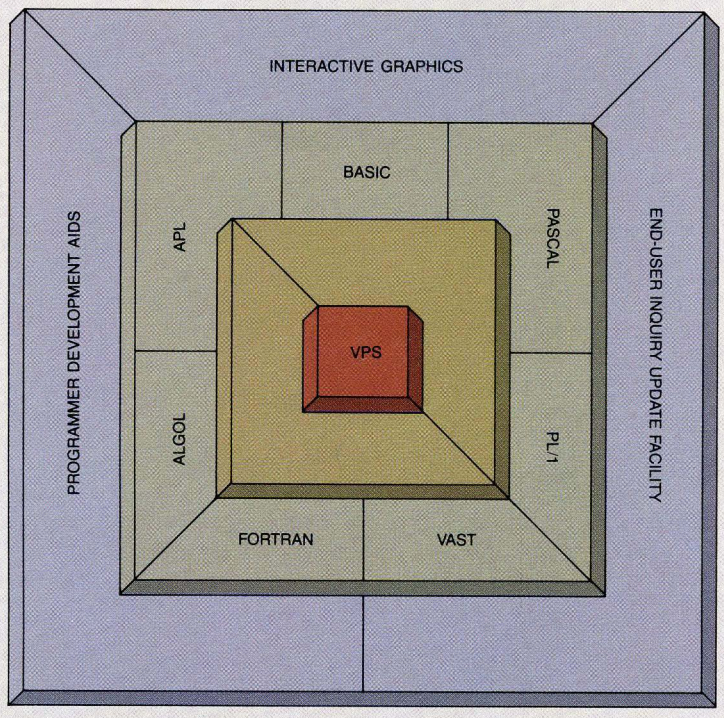


Figure 7. Applications Development Environment

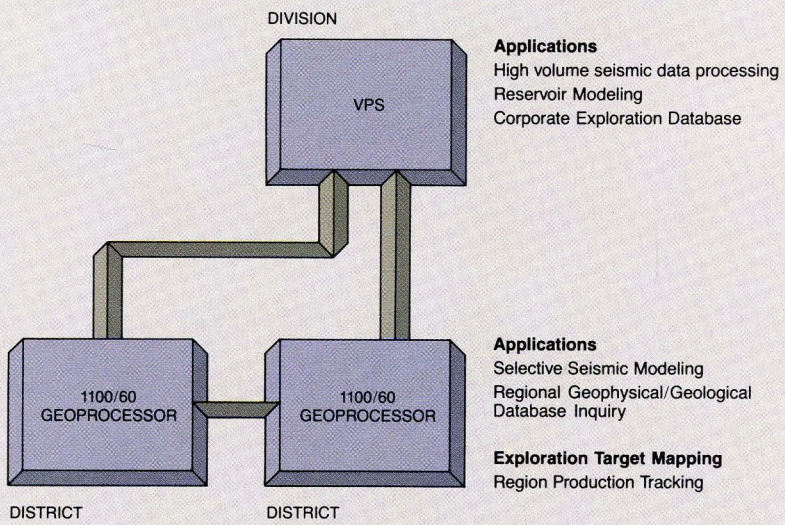


Figure 8. Distributed Petroleum Exploration/ Production Environment

Applications Development

Application developers utilizing the VPS Scalar Complex may elect to utilize FORTRAN, ALGOL, PL/1, Pascal, or any number of standard languages available (Figure 7). Using FORTRAN 77, users may also make use of VAST™, the Vector and Array Syntax Translator, which assists the user in VPS vectorization of certain FORTRAN constructs while maintaining source code integrity.

Besides FORTRAN, the Vector Processing System's power may also be directly accessed from other languages via direct function subroutines inserted in application code to perform specific mathematical operations sequences.

For ease of program development, VPS interactive text-editing, syntax scanning, and debugging aids are available.

VAST is a trademark of Pacific Sierra Corp.

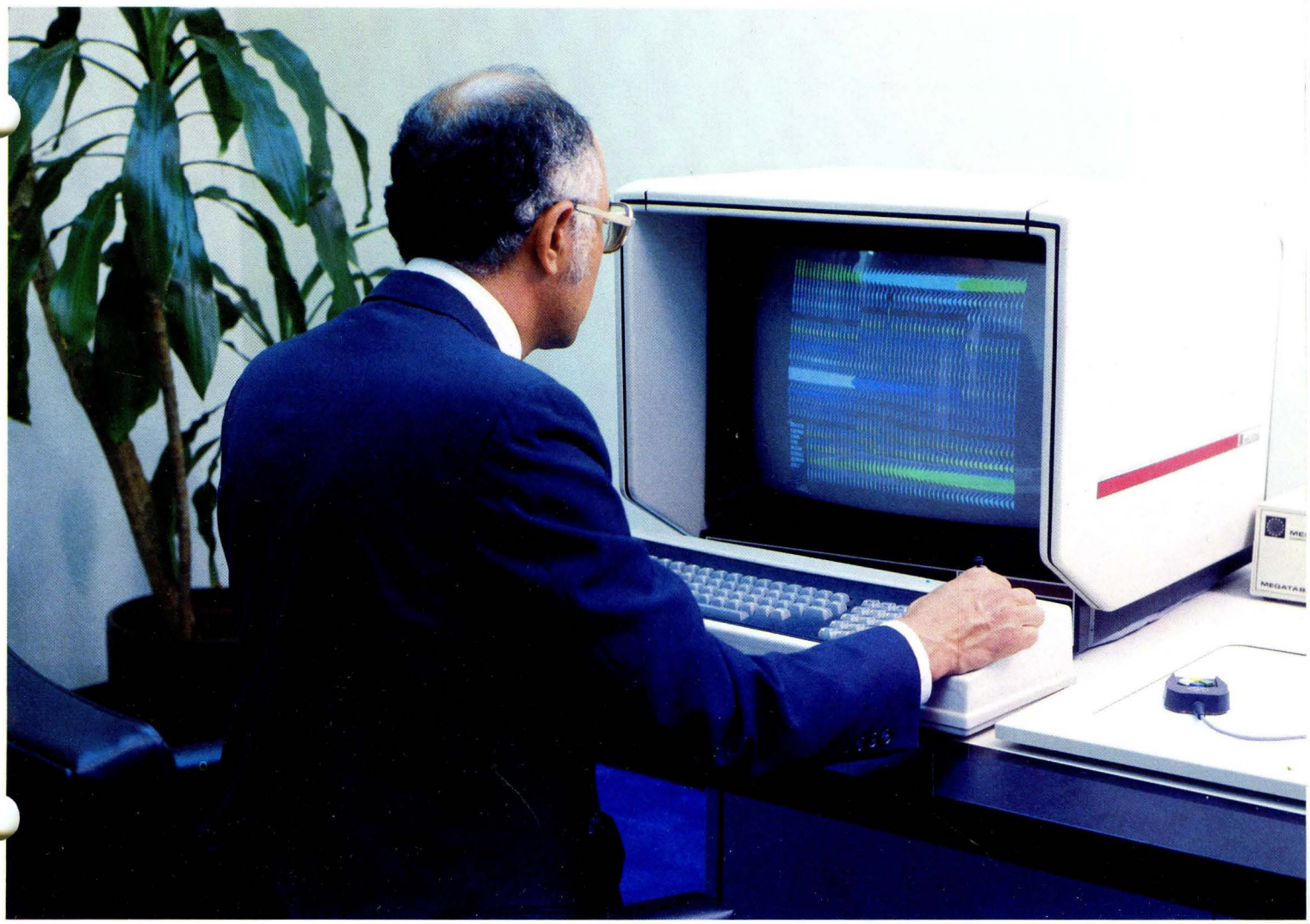
The VPS is just one model of a large family of 1100 Series compatible systems. Distributed exploration and production systems can be configured to meet a wide range of computing requirements at different sites, while still operating similar function applications software. An example is a large central VPS site for centralized high-volume seismic processing, and smaller 1100/60 Geoprocessors in district offices to provide compatible, more selective processing needs in areas of seismic, interactive modeling, etc. (Figure 8.)

Through direct support of interactive graphics, the benefits of immediate, on-line viewing and manipulation of seismic data, engineering structures, maps, and digital images are available to all VPS Scalar Complex users. All popular graphic display devices are supported, including Tektronix™, Adage, Megatek, and others.

By coupling interactive graphics with integrated data base support, the enormous computing power of the VPS can provide a *total* design and analysis tool for the end user, whether geophysicist, engineer, or scientist.

For Seismic Applications users, the VPS offers a library of Geophysical Algorithms, especially tailored to the arithmetic pipelines of the APU for optimum performance. These operations include:

- Wiener-Levinson Decon Filter (general and spiking)
- Normal Move-out/Quadratic Interpolation
- Ramp Scaling
- Trace Clipping Function
- Toeplitz equations solution
- Linear Interpolation
- Trace non-zero location
- Fast Fourier Transformation Suite
- Correlation
- Convolving Multiply
- Square Root
- Exponential Function
- Migration



Because the VPS is entirely air cooled, the expense of installation is minimal. In addition, the floor space needed for maximum configuration of the mainframe is less than 600 square feet. Figure 9. The minimum configuration is about half that amount. The Array Processor System is shown in figures 10 and 11. The APS is contained in two cabinets, each six feet high, five feet long and 2.5 feet wide. As seen in Figure 11, the single APU logic deck occupies only eight cubic feet of the APU cabinet.

The VPS has been designed with sustained high speed in mind. Unique reliability and maintenance features include:

- Parity checks throughout data paths in the processor and semiconductor memories.
- A special maintenance control computer scans and sets gates in the APCU/APU, checking the expected against the observed conditions.
- System redundancy and "fail-safe" capability are provided through the use of multiple-function units and data paths.

The Vector Processing System represents a dramatic increase in the power, functionality, and flexibility available to solve complex, multi-dimensional problems—today and in the future. Your Sperry Univac representative can show you how to put it to work for you.

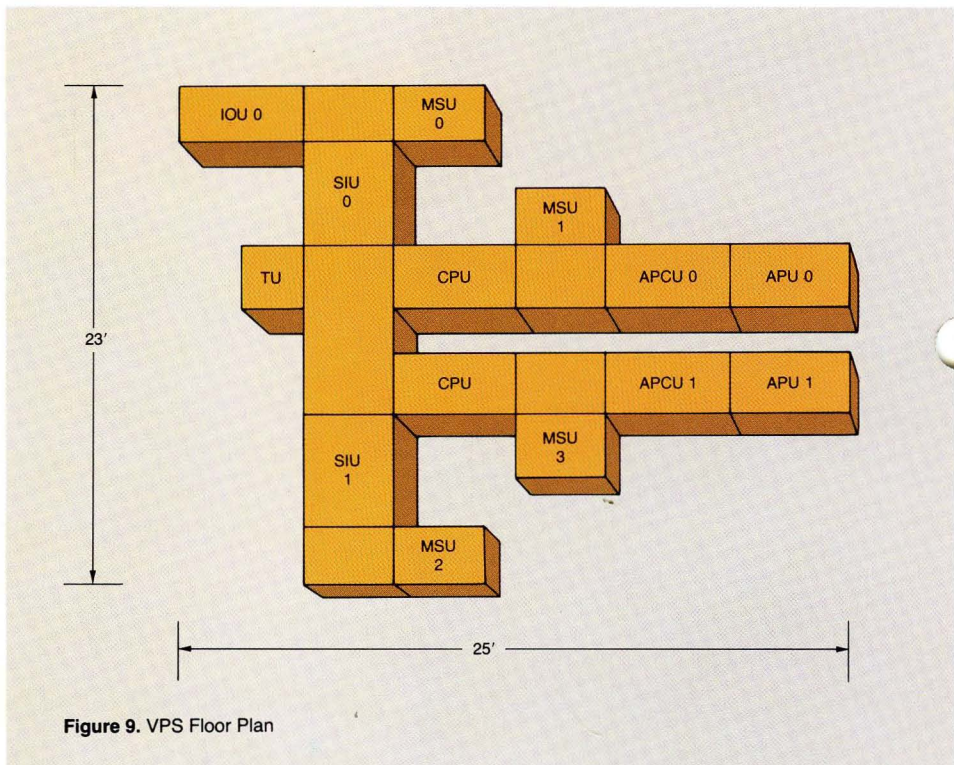


Figure 9. VPS Floor Plan

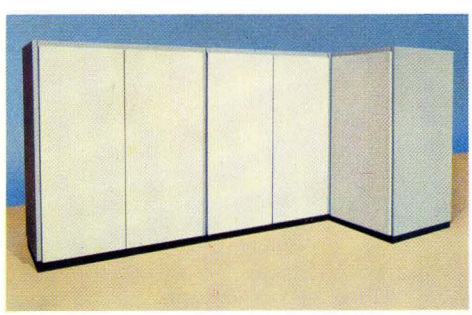


Figure 10. Array Processing System External View

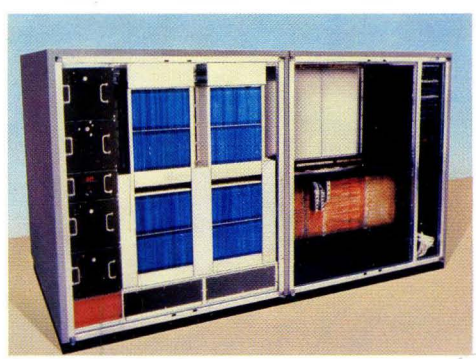


Figure 11. Array Processing System Internal View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SPERRY UNIVAC

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