SPERRY UNIVAC 1100/10 Systems

Hardware

System Description

SPERRY UNIVAC
COMPUTER SYSTEMS

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1. Introduction

SPERRY UNIVAC 1100/10 Systems provide lower cost extensions to the proven SPERRY UNIVAC 1100 Series of processors. Their modular design provides growth potential within the 1100/10 Systems as well as possible upgrading to a larger SPERRY UNIVAC 1100 Series System. An 1100/10 Systems Central Processor and Operator's Console is shown in Figure 1–1. The 1100/10 Systems comprise the 1100/11 (unit processor) and the 1100/12 (multiprocessor) Systems.

The 1100/10 Systems permit the user to tailor his operating system to his needs. The SPERRY UNIVAC 1100 Series Operating System has real-time, multiprogramming, demand, and batch processing ability.

In addition to the versatile operating system, the 1100/10 Systems utilize all the SPERRY UNIVAC 1100 Series family of software, application packages, and peripheral subsystems.

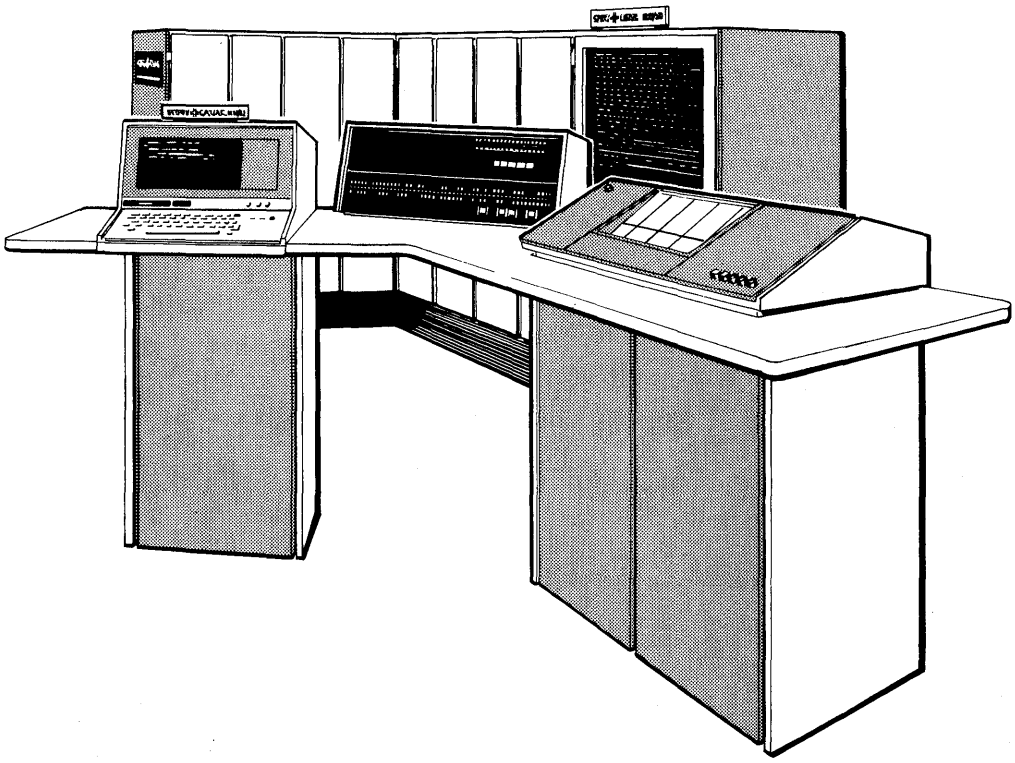


Figure 1–1. SPERRY UNIVAC 1100/10 Systems Central Processor and Operator's Console

2. Systems Description

2.1. GENERAL

The SPERRY UNIVAC 1100/10 Systems are a general purpose, high performance unit processor (1100/11) or a multiprocessor (1100/12) system, incorporating the latest advances in computer design, systems organization, and programming technology. Their modular structure permits the selection of systems components to fulfill most efficiently the speed and capacity requirements for applications of varying complexity.

As the workload increases, this modularity also enables the addition of more input/output subsystems and main storage. Among the principal features of the 1100/10 Systems are:

- Large, modular, high speed main storage with single bit error correction and double bit error detection
- Program address relocation
- Storage protection
- Partial-word addressability in 6-, 9-, 12-, and 18-bit portions as well as full-word (36 bits) and double-word (72 bits) addressing
- High speed, random access, auxiliary storage
- Privileged mode for the executive system
- Guard mode for user programs
- Half-word parity on input/output data transfers

2.2. 1100/11 UNIT PROCESSOR SYSTEM COMPONENTS

The 1100/11 Unit Processor System is organized to allow a number of tasks to be performed under the direction of a common executive control system.

The 1100/11 System is composed of four types of components:

- Central Processor Unit (CPU)
- Main Storage
- Auxiliary storage and peripheral subsystems
- Console

2.2.1. Central Processor Unit

The CPU can perform all functions required for the execution of instructions including arithmetic, input/output, and executive control. Included in the processor is a set of 125-nanosecond integrated circuit control registers providing multiple accumulators, index registers, input/output access control registers, and special-use registers.

2.2.2. Main Storage

The main storage of the 1100/11 System is a high performance, fast access, semiconductor storage for instructions and data, with a cycle time of 1125 nanoseconds. Available main storage capacity ranges from a system minimum of 131K words to the system maximum of 524K words. (The storage unit is available in 131K expandable to 262K modularity.)

2.2.3. Auxiliary Storage

The auxiliary storage subsystems are an integral part of the 1100/11 System. The types of auxiliary storage available are:

- Magnetic disc
- Magnetic tape
- Magnetic drum

2.2.4. Operator's Control Console

The console provides the means for communications with the operating system. The system is capable of supporting one system console and one to three auxiliary consoles. Only one day clock will be supported by the system. The basic console consists of the following major components:

- The CRT/keyboard consists of a UNISCOPE 100 Display Terminal. The display format is 16 lines with 64 characters per line. The seven-bit ASCII character set, consisting of 95 characters plus the space, is used. The keyboard provides all of the operator controls required for entering data and initiating transfers.
- The incremental printer operates at 30 characters per second and provides a hard copy of console messages. The cabinet containing the printer also contains the power supplies and logic required to control the CRT and incremental printers. (Up to five additional incremental printers may be connected to the console.) This unit also contains the interface between the console and an internally specified index (ISI) channel, through which the console communicates with the CPU.
- The fault indicator, located on the incremental printer, provides the operator with a visual indication of a fault condition in a major system component. The actual component and nature of the fault may then be determined from indicators on the CPU maintenance panel.
- The interface for remote console operation by means of the Total Remote Assistance CEnter (TRACE) system. Sperry Univac customer engineers have the capability of analyzing system problems remote from the site.
- The operator's panel containing all the switches and indicators necessary for the operator to initiate operation of the CPU from the console.

2.3. 1100/12 MULTIPROCESSOR SYSTEM COMPONENTS

An 1100/10 System may be configured as a multiprocessor system. The basic component requirements for the 1100/12 System multiprocessor configuration are:

- Two Central Processor Units
- 262K Storage (minimum)
- One Multiprocessor Capability feature
- One Availability Control Unit (optional)
- One Operator's Console per CPU required (maximum of two per CPU in the system, including auxiliary consoles)
- Auxiliary Storage

Most components used in the multiprocessor configuration are identical to those in the unit processor configuration; differences are described in 2.3.1 through 2.3.4.

2.3.1. Main Storage

The multiprocessor system requires a minimum of 262K words of main storage, consisting of two 131K cabinets.

2.3.2. Availability Control Unit (Optional)

The availability control unit (ACU) performs the following functions:

- Partitions the multiprocessor system hardware into independent systems.
- Takes units offline for maintenance without disrupting operation of the remainder of the system.
- Protects main storage in event of a power failure in a CPU.
- Automatically initiates a recovery sequence after an interruption.

The ACU partitions the hardware into specific configurations by disabling and enabling storage units, CPUs, and the word channel interface between the CPU and peripheral subsystem control units. The ACU can also take units offline for maintenance.

2.3.3. Multi-Module Access (MMA)

The multi-module access feature provides the second central processor interface to each storage module for the multiprocessor configuration.

2.3.4. Shared Peripheral Interface

The shared peripheral interface (SPI) allows the access of up to four input/output channels to units in auxiliary storage or peripheral subsystems.

Input/output subsystems may be either single- or dual-access. Single-access subsystems perform one I/O operation at a time and therefore require one control unit, one I/O channel, and in multiprocessor systems, only one SPI. Dual-access subsystems require two control units and can execute two operations simultaneously using different peripheral units in the subsystem. Both of these operations may originate in the same processor or they may come from different processors.

Different processors can be connected to a dual-access subsystem through two SPI units. Two input/output channels from each processor take separate paths. The failure of an SPI or one of the pair of control units affects only one of the two paths to a peripheral subsystem. Therefore, all peripheral units are still accessible through the second SPI and control unit.

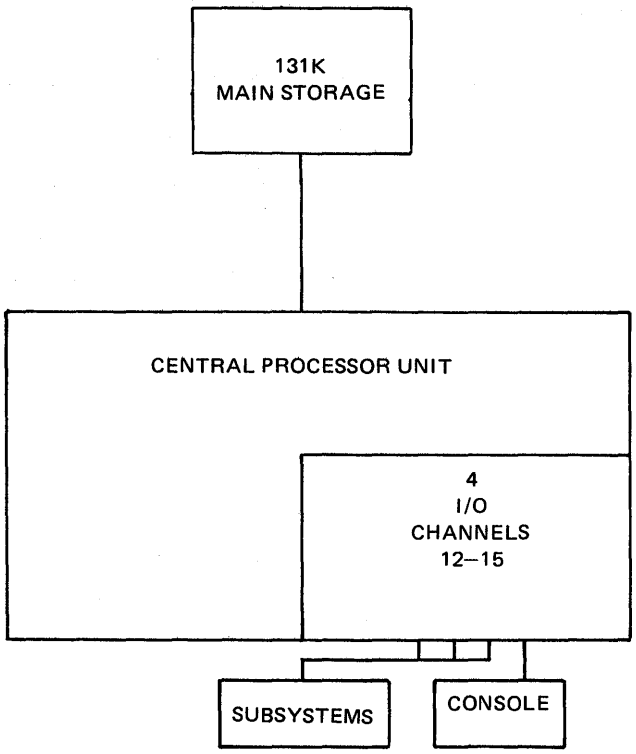
2.4. CONFIGURATIONS

Figure 2–1 depicts the minimum configuration for the unit processor system. The basic CPU consists of the command/arithmetic section and an input/output section with four I/O channels. Main storage provides 131K 36-bit words. The minimum peripheral subsystems needed to support the software offered are:

- one SPERRY UNIVAC Disc Subsystem with two 8430 Disc Units, two 8433 Disc Units, or two 8425 Disc Units;
- one UNISERVO Magnetic Tape Subsystem with two tape units; and
- one subsystem with a 0770 Printer and a 0716 Card Reader, or one C/SP with a 0770 Printer and a 0716 Card Reader.

Figure 2–2 illustrates the 524K storage configuration for a unit processor system.

A multiprocessor system configuration is illustrated in Figure 2–3.



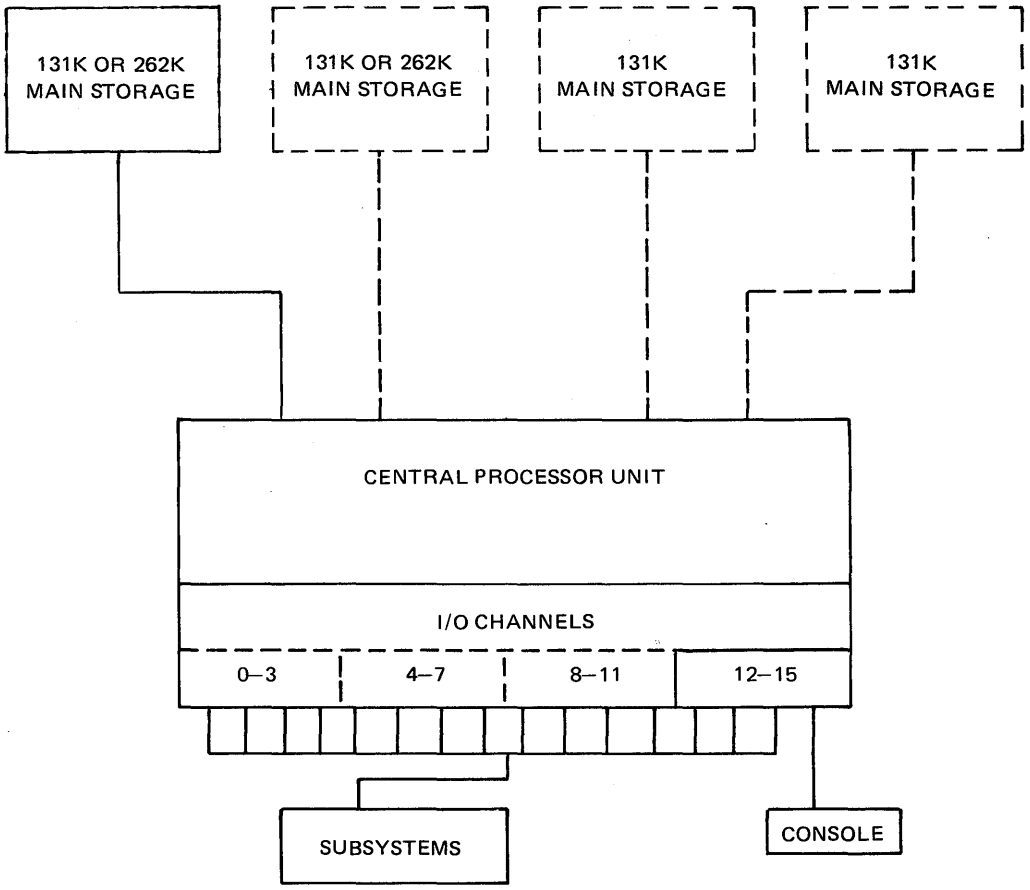
NOTE:

The 1100 Series Executive supports a minimum of 131K main storage.

CONSOLE AND MINIMUM PERIPHERAL SUBSYSTEMS FOR 1100/11 SYSTEM:

One Operator's Console with display terminal and incremental printer
One Magnetic Disc Subsystem with: two 8430 Disc Units, two 8433 Disc Units, or two 8425 Disc Units
One UNISERVO Magnetic Tape Subsystem with: two UNISERVO 12, two UNISERVO 14, two UNISERVO 16, or two UNISERVO 20 Magnetic Tape Units
One 0770 Printer and one 0716 Card Reader operating via MSA or C/SP

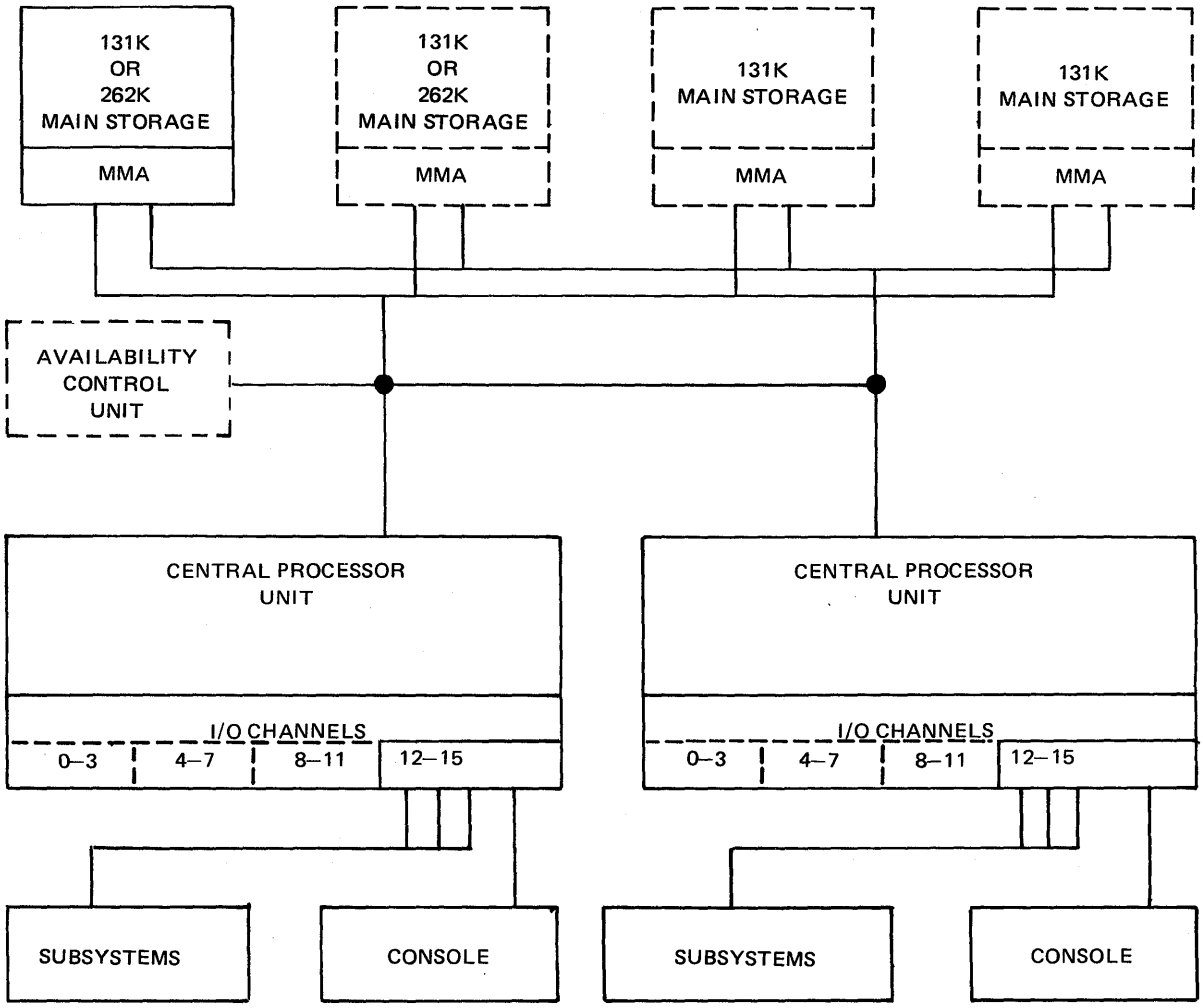
Figure 2–1. SPERRY UNIVAC 1100/11 System Unit Processor Minimum Configuration



NOTES:

1. The 1100 Series Executive supports a minimum of 131K main storage.
2. Dashed lines indicate options.
3. Maximum 524K Main Storage can be two 262K storage units, or one 262K storage unit plus two 131K storage units, or four 131K storage units.

Figure 2–2. SPERRY UNIVAC 1100/11 System Unit Processor Expanded Configuration



NOTES:

1. The 1100 Series Executive supports a minimum of 262K main storage.

2. Dashed lines indicate options.

3. Maximum 524K main storage can be four 131K storage units, two 262K storage units, or one 262K storage unit plus two 131K storage units.

MINIMUM CONFIGURATION:

Two Central Processor Units
Two Consoles
One Disc Subsystem with two 8430 Disc Units, two 8433 Disc Units, or two 8425 Disc Units
One UNISERVO Magnetic Tape Subsystem with: two UNISERVO 12, two UNISERVO 14, two UNISERVO 16, or two UNISERVO 20 Magnetic Tape Units
One 0770 Printer and one 0716 Card Reader operating via MSA or C/SP
262K main storage (two 131K storage units)

Figure 2–3. SPERRY UNIVAC 1100/12 System Multiprocessor Configuration

3. Central Processor Unit

3.1. GENERAL

The central processor unit (CPU) is the principal component of the SPERRY UNIVAC 1100/10 Systems and, generally, the one by which the entire system is identified. It can operate under executive or user program modes of control; it performs both arithmetic and logical operation; and it accommodates and supervises up to 16 input/output channels.

3.2. PRINCIPAL SECTIONS

The processor is logically divided into six interacting sections, each of which is identified and briefly described below.

- Control Registers — The CPU has 128 program-addressable control registers used for arithmetic operations, indexing, input/output access control, and special uses. These registers are grouped for use by the user, or for the exclusive use of the executive system, as described in 3.4.

- Arithmetic Section — This section contains the adder registers, and control circuits necessary for performing fixed and floating-point arithmetic, partial-word selection, shifting, logical operations, and tests.

- Control Section — This section provides the basic control and logic for instruction decoding and execution. It includes the program address counter used in accessing sequential instructions, the program control register in which instructions are staticized for execution, and the processor state register (PSR) which determines various processor operating modes. The control section also initiates the servicing of interrupts.

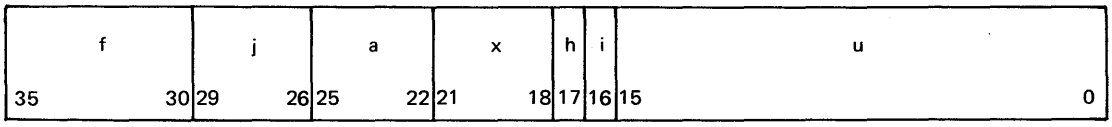
- Input/Output Section — This section controls and multiplexes data flow between the input/output channels and main storage. It includes an interrupt priority network and paths to peripheral subsystems for both control signals and data.

- Indexing Section — This section contains parallel index adders and threshold test circuitry. It is used generally for processor control functions, operand address development, program relocation, and input/output transfer control.

- Storage Class Control Section — The storage class control section receives the final operand address from the index adder and establishes address and data paths to one of four possible storage modules. Storage class control also determines whether a final address refers to a control register.

3.3. INSTRUCTION WORD FORMAT

The format of the 1100/10 Systems instruction word is illustrated below followed by an explanation of each field. Some fields have more than one meaning depending on the class of instruction.



3.3.1. Function Code – f-Field

These six bits specify the operation to be performed. For function codes above 70_8, the f- and j-fields are combined to produce a 10-bit function code. In certain instances, the f-, j-, and a-fields are combined to form a 14-bit function code. An invalid function code generates an interrupt.

3.3.2. Partial-Word or Immediate-Operand Designator – j-Field

For function codes less than 70_8, the 4-bit j-field specifies partial-word or immediate operand selection (see 3.5.3).

3.3.3. Control Register Designator – a-Field

The four-bit a-field designates which control register, within a group selected by the function code, is involved in the operation. For some operations, the a-field refers to an arithmetic register; for others, it refers to either an index register or some other control register. In input/output instructions, it specifies the channel and its associated input or output access control register. For function code 70_8 the a- and j-fields together address one of the 128 control registers.

3.3.4. Index Register Designator – x-Field

The 4-bit x-field specifies one of the 15 index registers to be used in address modification. When the x-field is set to 00_8, indexing is suppressed.

3.3.5. Index Modification Designator – h-Field

The 1-bit h-field controls modification of the index value (Xm) by the increment field (Xi) after indexing (see 3.4.1). If h=1, the right half of the index register is modified by the contents of its left half; if h=0, modification is suppressed.

3.3.6. Indirect Address Designator – i-Field

The 1-bit i-field controls the use of indirect addressing during instruction execution. If i=0, the instruction functions normally. If i=1, the 22 least significant bit positions of the instruction (x-, h-, i- and u-fields) are replaced in the instruction register with the contents of the 22 least significant bit positions of the word at the effective address. Indirect addressing continues as long as i=1 with full indexing capability at each level.

3.3.7. Address Field — u-Field

The 16-bit u-field normally specifies the operand address. However, for certain instructions it holds constants. For example, the shift instructions use the seven least significant bit positions to hold the shift count. In all instructions, the value in the u-field may be modified by the contents of an index register.

3.4. CONTROL REGISTERS

The 128 program-addressable control registers are grouped to provide multiple index registers, accumulators, input/output access control registers, and special registers (see Figure 3–1).

The control registers are 36-bit integrated-circuit registers, with a basic cycle time of 125 nanoseconds. Two parity bits are included with each control register.

Effective use of multiple accumulators and index registers for the development and use of constants, index values, and operands substantially improves performance. SPERRY UNIVAC 1100 Series Compilers, for example, perform significantly better through multiple register usage, and can produce highly efficient code.

In the following descriptions only programmable registers are discussed. The executive system, through modes established by the processor state register, has exclusive use of the duplicate set of control registers as well as the access control registers indicated by the shaded areas in Figure 3–1.

Four of the index (X) registers (addresses 014_8–017_8) overlap with four of the arithmetic accumulator (A) registers thus providing additional versatility in the use of A and X registers.

3.4.1. Index Registers

Control register locations 1_8–17_8 are index registers and have the following format:

X_i			X_m	
35	MODIFIER INCREMENT OR DECREMENT	18	17 INDEX MODIFIER	0

The X_m portion of the index register is an 18-bit modifier to be added to the base operand address of the instruction. The X_i portion of the index word updates the X_m portion, *after* base operand address modification.

Index register modification is specified by a 1 bit in the h-field of the instruction, while indexing itself is specified by a nonzero value in the x-field. Both the indexing and modifying functions take place within the basic instruction execution cycle adding no additional instruction execution time.

When cascaded indirect addressing is used in an operation, full indexing capabilities are provided at each level. Indirect addressing replaces the x-, h-, i- and u-fields of the instruction, beginning with a new indexing cycle for each cascaded sequence. This process continues until the i-field is zero.

The control register at address 0, while program addressable, stores the contents of the processor state register (PSR), when an interrupt occurs. Since the contents of this control register are overwritten at each interrupt, it is not generally useful for programming purposes.

3.4.2. Arithmetic Accumulators

Control register locations 14_8–33_8 are arithmetic accumulators for programmed storage of arithmetic operands and results. The computation is performed in nonaddressable transient registers within the arithmetic section.

Depending upon the instruction, the accumulators are used to hold a variety of word formats. Double-precision instructions and a number of logical instructions reference two contiguous accumulators, i.e., A and A+1. In arithmetic operations, A+1 always holds the least significant part of an operand or result. Some instructions, such as single-precision floating-point operations, call on a one-word operand from main storage but produce a two-word result in the specified A and A+1 registers.

3.4.3. Access Control Registers

Control register locations 40_8–77_8 are input and output access control registers (ACRs). They are guard mode protected and may be written only by the executive system. Formats of the access control words are detailed in Section 5.

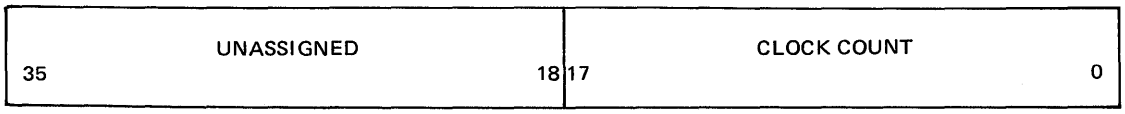
The word-by-word transmission of data over an I/O channel is governed by the contents of the ACRs. Two ACRs, one for input and one for output, are assigned to each of the sixteen channels. Input ACRs (locations 40_8–57_8) control input data transfers while output ACRs (locations 60_8–77_8) govern the transmission of output data and function words.

When an input/output operation is initiated, the programmed access control word (ACW) is loaded into the ACR corresponding to the channel associated with the specified peripheral control unit.

3.4.4. R Registers

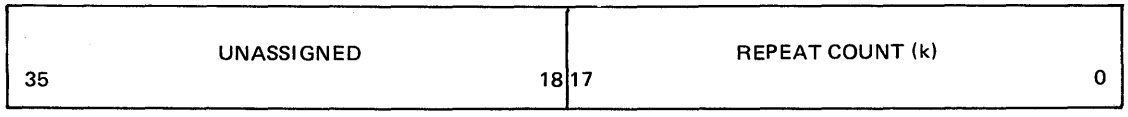
The sixteen control register locations 100_8–117_8 are R registers. The first three of these (R0, R1, R2) have specified functions and formats as described below. The remaining R registers are not specifically assigned; typically they are used as loop counter, transient registers, or storage for intermediate values or constants.

3.4.4.1. R0 – Real Time Clock



This register is initially loaded by the program. The contents are then decremented once each 200 microseconds. A real time clock interrupt occurs when the clock count goes through zero. Thus, if the clock is initially loaded with the value 5000, an interrupt occurs in one second.

3.4.4.2. R1 – Repeat Counter



The repeat counter controls repeated operations such as Block Transfer and search instructions. To execute an instruction k times, the repeat counter is loaded with k prior to the execution of the instruction.

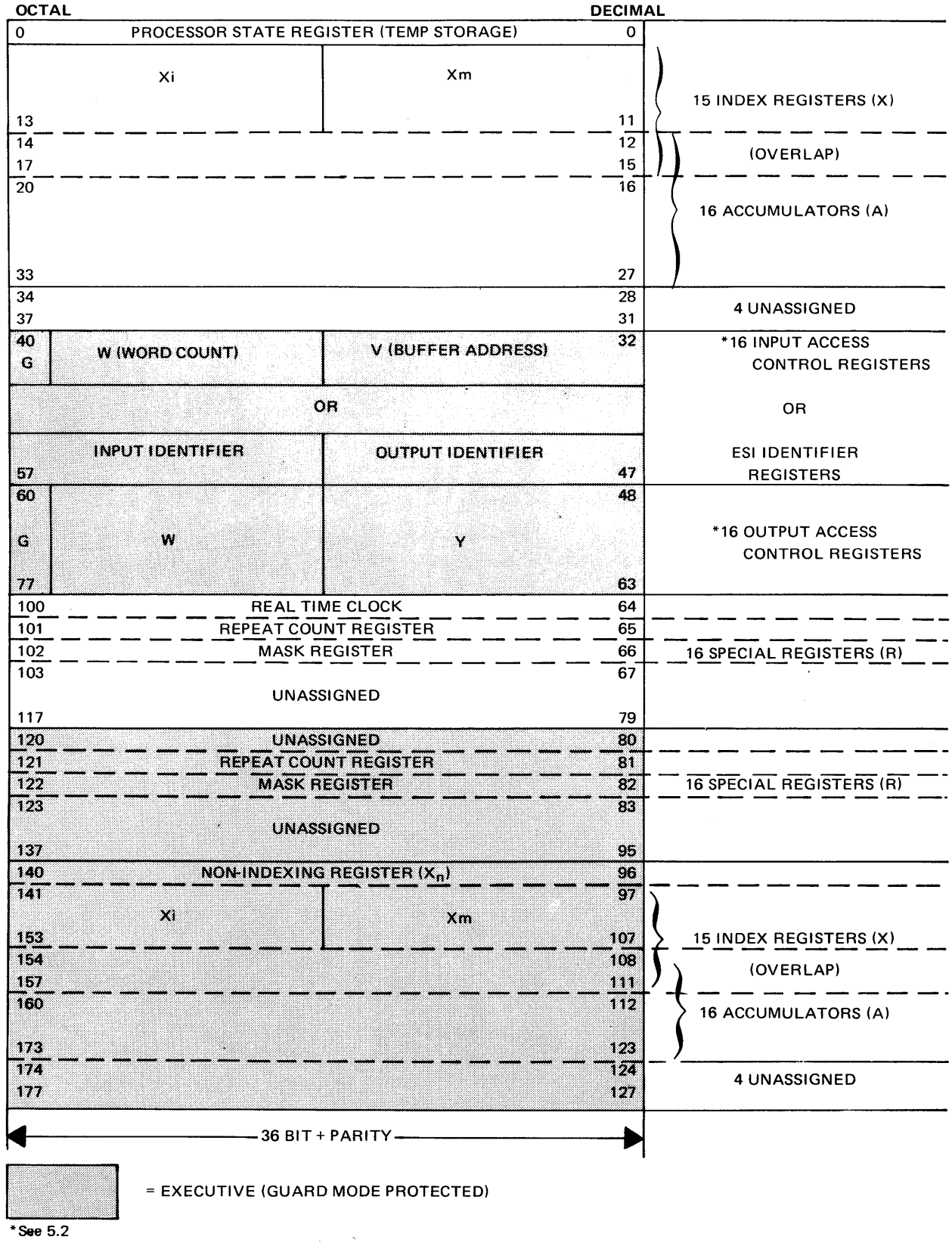


Figure 3–1. Control Register Address Assignments

3.4.4.3. R2 – Mask Register

The mask register functions as a filter in determining which portions of words are to be tested in repeated masked search operations. The contents of the effective address are compared to the contents of the arithmetic register only with respect to those positions which contain one's in the mask register. Both the mask register and the repeat counter are loaded prior to executing a masked search instruction.

3.5. ARITHMETIC SECTION

In the 1100/10 Systems the manipulation of data (addition, subtraction, multiplication, division, shifting) takes place in the arithmetic section of the central processor. During the execution of an arithmetic instruction, storage registers within the arithmetic section itself are used for actual computation. The arithmetic section has the following characteristics:

- On fixed-point, single-precision instructions, the j-designator selects all or a portion of one of the operands (half-, third-, quarter- or sixth-word) for use in the arithmetic operation.
- Special split-word arithmetic instructions provide for simultaneous addition or subtraction of corresponding half- or third-words of the two operands.
- A multiposition shift with the shift matrix requires the same time as a one place shift. Right and left shifts of single or double-length operands can be specified. Left shifting is logical (zeros are filled to the right) or circular (end around). Right shifts may be either logical, algebraic (sign bits are filled to the left), or circular.
- Sixteen registers in the control section, acting as sixteen accumulators, allow parallel and cumulative computation. Full double-precision floating-point arithmetic is provided.
- When the results of arithmetic operations are in double-length form, they are automatically stored in consecutive control registers and are available for retrieval as double-length results.
- Alphanumeric comparisons utilizing the mask register allow any selection of bits in one 36-bit word to be directly compared with corresponding bits of another word.

3.5.1. The Adder

The adder in the CPU is a ones complement subtractive adder for 36-bit or 72-bit operations. For purposes of analysis and debugging, the programmer may manually simulate the processor operation by simple binary or octal addition.

Two special internal designators associated with the arithmetic adder are the overflow designator and the carry designator. The fixed-point addition and subtraction instructions, single and double precision, are the only instructions which affect these two designators.

Before the execution of any of these instructions, both designators are cleared. The overflow designator is set when a significant bit is generated in the sign position. Thus, a positive result from two negative quantities or a negative result from two positive quantities sets the overflow designator. The carry designator is set whenever an end-around carry is generated.

After the instruction has been performed, the settings of the designators remain unchanged until another of the designated arithmetic instructions is initiated. Both designators are set in time to be tested immediately after the specified instruction has been executed.

When an interrupt occurs, the hardware stores the settings of the carry and overflow designators in the processor state register (see 4.2) and control passes to the executive system. This information is automatically returned to the designators when the executive system returns control to the interrupted program.

3.5.2. Arithmetic Accumulators

The sixteen arithmetic accumulators can be addressed directly by the programmer and are available for storing operands and results of arithmetic computation. These arithmetic accumulators should not be confused with the nonaddressable transient registers that are used in actual computation and are contained within the arithmetic section itself.

With the Add to X and Add Negative to X instructions, the index registers also act as accumulators in the same manner as the arithmetic registers.

3.5.3. Partial-Word Transfers

To minimize shifting and masking and allow computation based on selected portions of words, the 1100/10 Systems permit the transfer of partial words into and out of the arithmetic section in a varying pattern (see Table 3–1).

By selecting the coding of the j-field instruction word and bit 17 of the processor state register a programmer may transfer a chosen portion of an operand to or from a control register or the arithmetic section. The transfer to an arithmetic register may also be accompanied by sign extension for subsequent arithmetic operations, depending on the j-field.

3.5.4. Split-Word Arithmetic

The system can perform addition and subtraction of half-words or third-words simultaneously. The right halves of two operands, for example, are added and the sum is stored in the right half of the selected accumulator. At the same time, the left halves of the same two operands are added and the result is stored in the left half of the same accumulator. There is no carry interaction between the halves. The same holds true for thirds of words.

3.5.5. Shifting

The system can perform both single-length shifting (36 bits) or double-length shifting (72 bits), treating the latter as if operating with a single 72-bit register. A high speed shift matrix makes execution time independent of the number of places involved in the shift, which means that an operand can be shifted from 1 to 72 positions in one main storage cycle time.

Six types of shift operations are provided.

- Right Circular – bits shifted out at the right reappear at the left.
- Left Circular – bits shifted out at the left reappear at the right.
- Right Logical – bits shifted out at the right are lost; zeros replace bits shifted out of the most significant positions.
- Left Logical – bits shifted out at the left are lost; zeros replace bits shifted out of the least significant positions.

Table 3–1. j-Determined Partial-Word Operation

j (Octal)	PSR Bit 17	Bit Positions of (U) → A, X, or R	Bit Positions of (A), (X), or (R) → U
00	–	35–00 → 35–00	35–00 → 35–00
01	–	17–00 → 17–00	17–00 → 17–00
02	–	35–18 → 17–00	17–00 → 35–18
03	–	17–00 → S 17–00	17–00 → 17–00
04	0	35–18 → S 17–00	17–00 → 35–18
	1	26–18 → 08–00	08–00 → 26–18
05	0	11–00 → S 11–00	11–00 → 11–00
	1	08–00 → 08–00	08–00 → 08–00
06	0	23–12 → S 11–00	11–00 → 23–12
	1	17–09 → 08–00	08–00 → 17–09
07	0	35–24 → S 11–00	11–00 → 35–24
	1	35–27 → 08–00	08–00 → 35–27
10	–	05–00 → 05–00	05–00 → 05–00
11	–	11–06 → 05–00	05–00 → 11–06
12	–	17–12 → 05–00	05–00 → 17–12
13	–	23–18 → 05–00	05–00 → 23–18
14	–	29–24 → 05–00	05–00 → 29–24
15	–	35–30 → 05–00	05–00 → 35–30
16	–	18 bits* → 17–00	NO TRANSFER
17	–	18 bits* → S 17–00	NO TRANSFER

*If x = 0: h, i, and u are transferred
If $x \neq 0$: $u + (X_x)_m$ is transferred

S = Sign extension, where the sign is that of the j-determined final contents of A.

- Right Algebraic – sign bits replace bits shifted out of the most significant positions.
- Scale-Factor Shift – single or double accumulator left shift which positions the word and simultaneously counts the number of shifts required until the most significant bit of the accumulator is unequal to the next most significant bit.

3.5.6. Double-Precision Fixed-Point Arithmetic

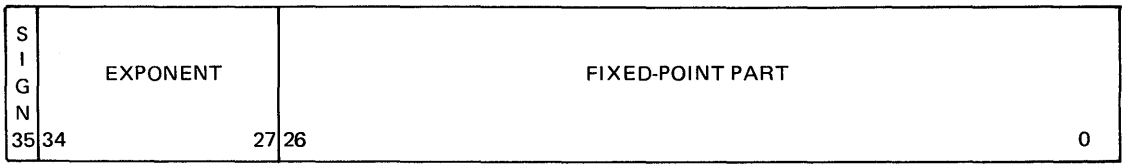
The system provides 72-bit, double-precision fixed-point addition and subtraction. Operands are processed as if they occupied a single 72-bit register. Bit 71, the high order bit, is the sign bit.

In addition, several arithmetic instructions produce two-word results. With fixed-point multiplication, a double-length product is stored in two arithmetic registers for integer and fractional operations. Integer and fractional division is performed upon a double-length dividend with the quotient retained in A and the remainder retained in A+1.

3.5.7. Floating-Point Arithmetic

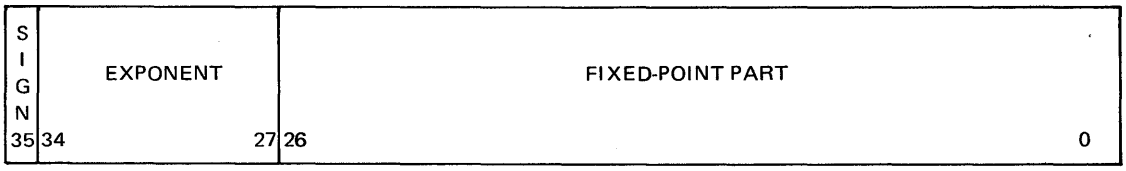
The system is equipped with an extensive hardware repertoire of floating-point instructions. If the arithmetic is single-precision, the range is from 10^{38} to 10^{-38} with eight-digit precision. The word formats are given below.

Source Operand Format

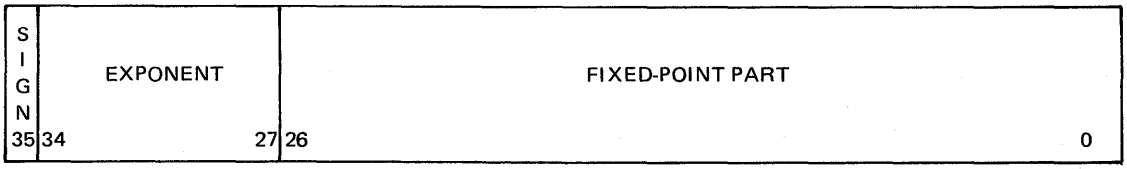


Result Format

WORD 1



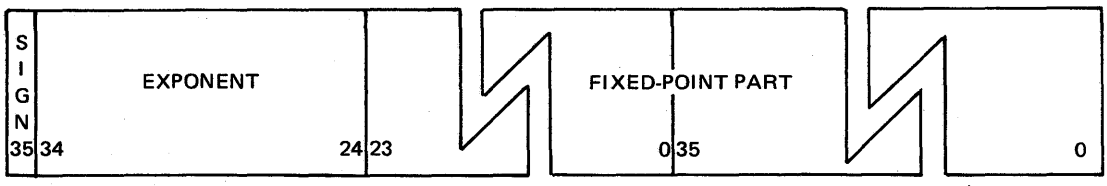
WORD 2



In a single-precision floating-point operation, word 1 is the more significant portion of the result. Word 2 contains the less significant portion. Mathematical error tracing can determine how much accuracy is being lost in calculations using this format. The least significant word is displaced 27 bits to the right of the binary point in the most significant word. Hence, its exponent is always adjusted by −27. The two-word result of this single-precision operation is stored in two contiguous arithmetic registers.

If the arithmetic is double-precision, the range is from 10^{307} to 10^{-308} with 18-digit precision. The values are expressed in two adjacent words, as shown in the following format.

Source and Result Format



Full double-precision operations do not require a repeated sign and exponent in the 36 least signficiant bits.

If any of the floating-point formats the exponent can assume a range of values as follows:

Single-precision:	(8 bits):	000–255
Double-precision:	(11 bits):	0000–2047

To express negative exponents, the hardware biases (floats) the exponent on a midvalue. The sign bit of the floating-point word applies to the fixed-point part. The true and biases ranges of the exponent are as follows:

	True	Biased
Single-precision:	-128_{10} to $+127_{10}$	$0 - 255_{10}$
Double-precision:	-1024_{10} to $+1023_{10}$	$0 - 2047_{10}$

The positive fixed-point part is normally assumed to be in range ½ to 1. Such a value places a 1 bit in the most significant position. When this condition exists, the floating-point number is said to be normalized. A negative fixed-point part causes the entire floating-point word to be complemented, and a 0 appears in this position.

Floating-point instructions are also provided for the following operations.

- Determining differences in exponents.
- Packing and unpacking exponents and fixed-point parts (single- and double-precision).
- Conversion – Single- to double-precision
  Double- to single-precision

3.6. INSTRUCTION REPERTOIRE

The 1100/10 Systems CPU is provided with an unusually powerful and flexible instruction repertoire. Many of the instructions are effectively accessed and completed in one main storage cycle. Included in the complete set of instructions is a group which permits fast and simplified control by the executive system.

In the following discussion, the instructions in the 1100/10 Systems repertoire are grouped by functional class to illustrate the power of the repertoire. Appendix C lists the instructions numerically by octal function code, stating exactly what each one does and giving the execution time.

3.6.1. Data Transfer Instructions

To load the arithmetic registers:

Load A
Load Negative A
Load Magnitude A
Load Negative Magnitude A

To load the index and R registers:

Load R
Load X Modifier
Load X
Load X Increment

To load two arithmetic registers with one instruction:

Double Load A
Double Load Negative A
Double Load Magnitude A

To store the arithmetic registers:

Store A
Store Negative A
Store Magnitude A

To store other control registers:

Store R
Store X

To store two arithmetic registers with one instruction:

Double Store A

Two special purpose transfers:

Store Zero
Block Transfer

All transfer instructions, except double-length transfers, move selected parts of words. That is, the partial-word feature allows any sixth-, quarter-, third-, or half-word to be loaded into the lower portion of an arithmetic register when using load instructions. Similarly, when using a store instruction, any sixth-, quarter-, third-, or half-word can be transmitted from the lower portion of an arithmetic register, index register, or R register to main storage.

3.6.2. Fixed-Point Arithmetic

Single-word operations on arithmetic registers:

Add to A
Add Negative to A
Add Magnitude to A
Add Negative Magnitude to A
Add Upper
Add Negative Upper
Add to X
Add Negative to X
Multiply Integer
Multiply Single Integer
Multiply Fractional
Divide Integer
Divide Single Fractional
Divide Fractional

Double-length operations on two arithmetic registers:

Double Precision Fixed Point Add
Double Precision Fixed Point Add Negative

Special format operations:

Add Halves
Add Negative Halves
Add Thirds
Add Negative Thirds

3.6.3. Floating-Point Arithmetic

The repertoire includes both single- and double-precision floating-point operations, using one-word and two-word operands, respectively. Ones complement arithmetic is used.

Single-precision operations:

Floating Add
Floating Add Negative
Floating Multiply
Floating Divide
Load and Unpack Floating
Load and Convert to Floating

Double-precision operations:

Double Precision Floating Add
Double Precision Floating Add Negative
Double Precision Floating Multiply
Double Precision Floating Divide
Double Load and Convert to Floating

Miscellaneous

- Magnitude of Characteristic Difference to Upper
- Characteristic Difference to Upper
- Floating Expand and Load
- Floating Compress and Load

3.6.4. Index Register Instructions

The a-field of these instructions can be used when modifying, loading, or storing the contents of index registers.

- Store X
- Add to X
- Add to Negative X
- Load X Modifier
- Load X
- Load X Increment
- Test Less Than or Equal to Modifier
- Jump Modifier Greater and Increment
- Load Modifier and Jump

These instructions address the appropriate index register. Four of the index registers are overlapped with the arithmetic registers; thus all arithmetic instructions, such as multiply or shift, can operate directly on these four index registers.

3.6.5. Logical Instructions

The logical instructions are:

- Logical OR
- Logical Exclusive OR
- Logical AND
- Masked Load Upper

Several other instructions such as the repeated masked search instructions employ logical operations in combination with other functions.

3.6.6. Shift Instructions

The twelve shift functions include circular, logical, and algebraic shifts. Circular shifts are end-around. Logical shifts fill in zeros on the end opposite the shift direction, whereas algebraic shifts fill in sign bits. The shift count (from 0 through 72 places) is taken from the address field (indexed when specified) of the shift instruction.

Right shift instructions:

Single Shift Circular
Double Shift Circular
Single Shift Logical
Double Shift Logical
Single Shift Algebraic
Double Shift Algebraic

Left shift instructions:

Load Shift and Count
Double Load Shift and Count
Left Single Shift Circular
Left Double Shift Circular
Left Single Shift Logical
Left Double Shift Logical

3.6.7. Repeated Search Instructions

Search instructions operate as repeated comparison operations, comparing the value at the base address of the operand with that in the arithmetic register. They skip the next instruction when a specified condition is met or take the next instruction in sequence when the repeat count in R1 has been decremented to zero.

Algebraic (Sign considered):

Search Equal
Search Not Equal
Search Less Than or Equal
Search Greater
Search Within Range
Search Not Within Range

Masked Algebraic (Sign considered):

Mask Search Equal
Mask Search Not Equal
Mask Search Less than or Equal
Masked Search Greater
Masked Search Within Range
Masked Search Not Within Range

Masked Alphanumeric (Unsigned):

Masked Alphanumeric Search Less Than or Equal
Masked Alphanumeric Search Greater

3.6.8. Unconditional Jump Instructions

These instructions transfer control to the location specified by the indexed u-address.

Store Location and Jump
Load Modifier and Jump
Load D Bank Base and Jump*
Load I Bank Base and Jump*

3.6.9. Conditional Jump Instructions

These instructions make a comparison and, if a specific condition is met, they transfer program control to the instruction location specified by the base address of the operand. If the specific condition is not met, the next instruction in sequence is executed.

Jump Greater and Decrement**
Double Precision Zero Jump
Jump Positive and Shift
Jump Negative and Shift
Jump Zero
Jump Nonzero
Jump Positive
Jump Negative
Jump Keys
Halt Keys and Jump
Jump No Low Bit
Jump Low Bit
Jump Modifier Greater and Increment
Jump Overflow
Jump No Overflow
Jump Carry
Jump No Carry
Jump Input Channel Busy
Jump Output Channel Busy
Jump Function in Channel

3.6.10. Test (Or Skip) Instructions

These instructions make a comparison and if the specified condition is met, the next instruction is skipped. If not, the next instruction is executed.

Test Even Parity
Test Odd Parity
Test Less Than or Equal to Modifier
Test Zero
Test Nonzero
Test Equal
Test Not Equal

**Simulated by the executive system*

***The j- and a-fields together serve to specify one of the 128 control registers.*

Test Less Than or Equal
Test Greater
Test Within Range
Test Not Within Range
Test Positive
Test Negative
Double Precision Test Equal

3.6.11. Executive System Control Instructions

This group of instructions enables the executive system to maintain proper control of the operating system.

Executive Return
Prevent All I/O Interrupts and Jump
Store Channel Number
Load Processor State Register
Load Storage Limits Register
Initiate Interprocessor Interrupt
Enable Day Clock
Disable Day Clock
Select Interrupt Locations
Load Channel Select Register/Load Last Address Register
Allow All I/O Interrupts and Jump

These instructions are used for establishing processor state, storage limits boundaries, interrupt locations, and identification of I/O channels.

3.6.12. Input/Output Instructions

This group of instructions allows the executive system to initiate, test and control input/output operations. Monitored instructions interrupt the program when the indicated transfer is completed.

Load Input Channel
Load Input Channel and Monitor
Jump Input Channel Busy
Disconnect Input Channel
Load Output Channel
Load Output Channel and Monitor
Jump Output Channel Busy
Disconnect Output Channel
Load Function in Channel
Load Function in Channel and Monitor
Jump Function in Channel
Allow All Channel External Interrupts
Prevent All Channel External Interrupts

3.6.13. Other Instructions

Execute
Test and Set
No Operation
Store Processor Designators
Load Processor Designators

3.7. DAY CLOCK

Each CPU includes a 36-bit day clock. The day clock is incremented once each 200 microseconds. A clock interrupt occurs at 6.5536-second intervals. The day clock can be enabled and disabled under program control; in addition, the day clock can be manually disabled.

The dayclock can be used to give a visual display of the time-of-day via the CRT display of the system console. Also, the day clock can be used by the executive system to control time-of-day dependent program execution.

3.8. BREAKPOINT REGISTER

A breakpoint register is provided as a debugging aid. This register is operational on the instruction address (P register) and for read, write, and input/output main storage references, for all main storage configurations.

4. Operating System Control Features

4.1. GENERAL

The SPERRY UNIVAC 1100 Series Operating System has complete control of the entire SPERRY UNIVAC 1100/10 System. Special hardware features are provided to permit this control to be both efficient and reliable.

The integrity of the system is maintained by guard mode operation. In this mode, certain instructions, registers, and storage locations are available for the exclusive use of the executive system.

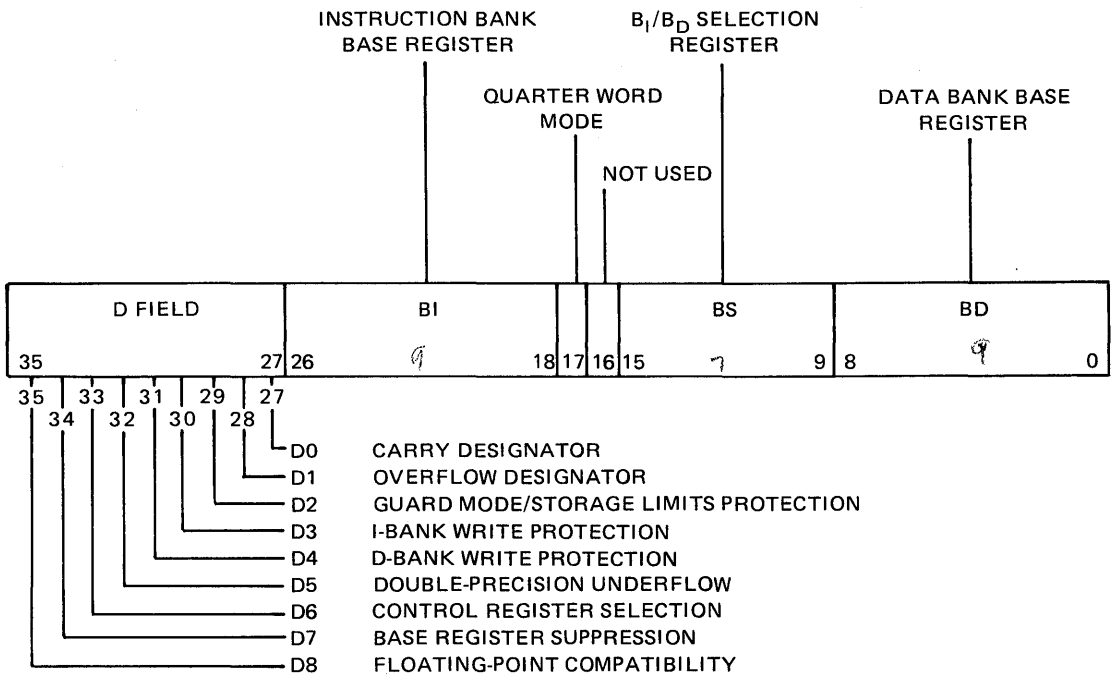
4.2. PROCESSOR STATE REGISTER

The processor state register (PSR) stores a 36-bit representation of various states and conditions affecting the current operations of the processor. By means of this register the executive system sets up control modes for itself, governs the operation of worker programs, and registers status information concerning worker programs when it regains control as a result of an interrupt. Two PSR formats apply; one for 262K addressing, and one for 524K addressing. Figures 4–1 and 4–2 explain in detail the significance of each bit for the two PSR formats.

The executive system uses a special instruction, Load Processor State Register, to load the PSR and to govern the following functions and conditions:

- Program base addresses
- Quarter-word operations in the processor
- Carry and overflow status
- Guard mode
- Storage protection mode
- Double-precision floating-point underflow mode (double-precision operations)
- Base register suppression
- Control register process selection

The contents of the PSR are transferred to control register location 0 automatically as soon as an interrupt occurs. The PSR is then initialized in preparation for executive system operations. The executive system saves the contents of control register 0 so that it can reinstate conditions when control is returned to the program that was interrupted.



D FIELD

D8 FLOATING-POINT COMPATIBILITY
- =0 Clears exponent to zero when a fixed-point part equal to zero is generated
- =1 Produces relative floating-point 0

D7 BASE REGISTER SUPPRESSION
- =0 Allows contents of base registers to be added to every U address.
- =1 Base register addition on storage reference is suppressed when instruction i-designator = 1.

D6 CONTROL REGISTER SELECTION
- =0 Selects user program control register set (locations 00_8–37_8, 101_8–117_8)
- =1 Selects executive control register set (locations 120_8–177_8)

The executive passes control to user programs with D6 = 0, which selects the worker set. An interrupt forces this bit to 1 after (PSR) has been transferred to control register X0, making the upper control registers available to the executive.

D5 DOUBLE-PRECISION UNDERFLOW – Double-Precision Floating-Point Operations
- =0 Interrupts on double-precision, floating underflow
- =1 Clears results to zero and continues

This is a program-requestable option which is set up for the program by the executive.

D4 D-BANK WRITE PROTECTION
- =0 Read, write and storage protection under guard mode D2.
- =1 D-bank write inhibit. Guard mode interrupt if write attempted in D-bank.

D3 I-BANK WRITE PROTECTION
- =0 Read, write and jump storage protection under guard mode D2.
- =1 I-bank write inhibit. Guard mode interrupt if write attempted in I-bank.

D2 GUARD MODE/STORAGE LIMITS PROTECTION
- =0 Guard mode off. All instructions and all store reference to access control registers (40_8–77_8), the real time clock (100_8) and executive control registers (120_8–177_8) are permitted.
- =1 Guard mode on. Invalidates all instructions and control register reference described above to enforce the integrity of the system. Only when guard mode is one can the contents of the storage limits register be fully effective in storage protection.

D1 OVERFLOW DESIGNATOR
- =1 Overflow (fixed-point add or subtract)

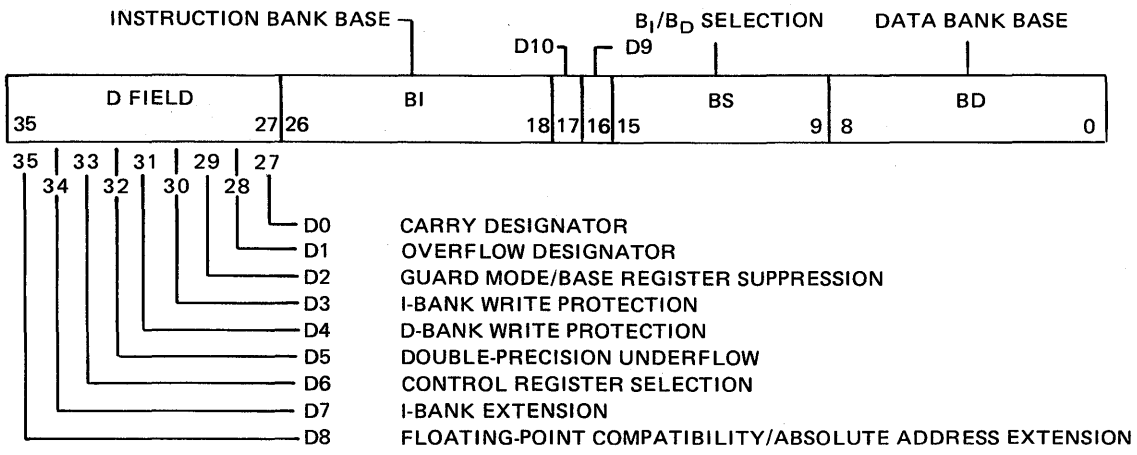
D0 CARRY DESIGNATOR
- =1 Carry (fixed-point add or subtract)

OTHER FIELDS

8–0, 15–9, 26–18 BASE REGISTERS. These registers provide the absolute base address values on which programs "float" in main storage during execution.

17 QUARTER-WORD MODE BIT
- =1 Quarter-word mode effective
- =0 Quarter-word mode not effective

Figure 4–1. Processor State Register Format–262K Addressing



D10 QUARTER-WORD MODE
=0 Quarter-word mode not effective
=1 Quarter-word mode effective

D9 D-BANK EXTENSION
=0 D-bank contained in lowest 262K of main storage
=1 D-bank contained in highest 262K of main storage

D8 (When D2=0) ABSOLUTE ADDRESS EXTENSION
=0 Absolute address specified by instruction with i=1 is in lowest 262K of main storage
=1 Absolute address specified by instruction with i=1 is in highest 262K of main storage

(When D2=1) FLOATING-POINT COMPATIBILITY
=0 Clears exponent to zero when a fixed-point part equal to zero is generated
=1 Produces relative floating-point 0

D7 I-BANK EXTENSION
=0 I-bank contained in lowest 262K of main storage
=1 I-bank contained in highest 262K of main storage

D6 CONTROL REGISTER SELECTION
=0 Selects user program control register set (locations 00_8–37_8, 101_8–117_8)
=1 Selects executive control register set (locations 120_8–177_8)
The executive passes control to user programs with D6=0, which selects the worker set. An interrupt forces this bit to 1 after (PSR) has been transferred to control register X0, making the upper control registers available to the executive.

D5 DOUBLE-PRECISION UNDERFLOW –
Double-Precision Floating-Point Operations
=0 Interrupts on double-precision, floating underflow
=1 Clears results to zero and continues
This is a program-requestable option which is set up for the program by the executive.

D4 D-BANK WRITE PROTECTION
=0 Read, write and storage protection under guard mode D2
=1 D-bank write inhibit. Guard mode interrupt if write attempted in D-bank.

D3 I-BANK WRITE PROTECTION
=0 Read, write and jump storage protection under guard mode D2.
=1 I-bank write inhibit. Guard mode interrupt if write attempted in I-bank.

D2 GUARD MODE/BASE REGISTER SUPPRESSION
=0 Guard mode off. All instructions and all store reference to access control registers (40_8–77_8), the real time clock (100_8) and executive control registers (120_8–177_8) are permitted.

Base register suppression in effect. Base register addition on storage reference is suppressed when instruction i-designator=1.

=1 Guard mode on. Invalidates all instructions and control register reference described above to enforce the integrity of the system. Only when guard mode is one can the contents of the storage limits register be fully effective in storage protection.

Base register suppression not in effect. Allows contents of base register to be added to every U address.

D1 OVERFLOW DESIGNATOR
=1 Overflow (fixed-point add or subtract)

D0 CARRY DESIGNATOR
=1 Carry (fixed-point add or subtract)

OTHER FIELDS

8–0	BASE REGISTERS. These registers provide
15–9	the absolute base address values on which
26–18	programs "float" in main storage during execution.

Figure 4–2. Processor State Register Format – 524K Addressing

4.3. INTERRUPTS

The interrupt network of the 1100/10 Systems is extensive. An interrupt is a control signal generated by either a peripheral subsystem (external interrupt) or the control section of the central processor. Specific interrupt locations are assigned within the lower address regions of main storage for each condition. These interrupt locations are programmed to capture the interrupted address and enter interrupt response subroutines in the executive system. The synchronization of input/output activities and response to real time situations is accomplished through some of these interrupts.

Other interrupts are provided for certain error conditions within the central processor. These may result from a programming fault such as an illegal instruction, a main storage parity error, or a user program violation such as an attempt to write into a protected area of storage or a violation of guard mode. These fault interrupts signal the executive system to initiate remedial or terminating action when they are encountered. Table 4–1 lists the fixed-address assignments. Note that all assigned locations are interrupt locations except for 200_8 and 201_8, which receive status words, and 216_8, which stores the day clock count.

Table 4–1. Fixed-Address Assignments

Decimal Address	Octal Address	Fixed Assignment
128	200	Status Word for External Interrupt on CPU 0
129	201	Status Word for External Interrupt on CPU 1*
130	202	Unassigned
131–133	203–205	Unassigned
134	206	Main Storage Operand Error Correction Interrupt
135	207	Main Storage Instruction Error Correction Interrupt
136	210	Power Loss Interrupt
137	211	ESI Access Control Word Parity Error Interrupt
138	212	ISI Access Control Word Parity Error Interrupt
139	213	Output Data Parity Error Interrupt
140	214	Input Data Parity Error Interrupt
141	215	Unassigned
142	216	Day Clock Input
143	217	Day Clock Interrupt
144	220	ISI Input Monitor Interrupt
145	221	ISI Output Monitor Interrupt
146	222	ISI Function Monitor Interrupt
147	223	ISI External Interrupt
148	224	ESI Input Monitor Interrupt
149	225	ESI Output Monitor Interrupt
150	226	Unassigned
151	227	ESI External Interrupt
152	230	Unassigned
153	231	Real Time Clock Interrupt
154	232	Interprocessor Interrupt 0
155	233	Interprocessor Interrupt 1
156	234	Unassigned
157	235	Main Storage Parity Error Interrupt (MEM 2)
158	236	Main Storage Parity Error Interrupt (MEM 3)
159	237	Main Storage Parity Error Interrupt (MEM 4)
160	240	Control Register Parity Error Interrupt
161	241	Invalid Instruction Interrupt
162	242	Executive Return Interrupt
163	243	Guard Mode/Storage Limits Protection Fault Interrupt
164	244	Test and Set Interrupt
165	245	Floating-Point Characteristic Underflow Interrupt
166	246	Floating-Point Characteristic Overflow Interrupt
167	247	Divide Fault Interrupt
168–255	250–377	Unassigned
(Last address –1)		Main Storage Parity Error Interrupt (MEM 1)

*Unassigned in Unit Processor System

4.4. GUARD MODE

The guard mode prevents user programs from executing any of the instructions listed below. These instructions are reserved for the executive system. It also protects certain locations in main storage reserved for executive system operations.

Guard mode is established by the Load Processor State Register instruction. Execution of this instruction with the appropriate PSR bit pattern is the only way the guard mode can be made operative and provides the only direct access to the PSR. Under guard mode, an attempt to perform any of the privileged instructions or functions listed below results in a processor interrupt.

- Load Processor State Register
- Load Storage Limits Register
- Initiate Interprocessor Interrupt
- Select Interrupt Location
- Load Channel Select Register
- All I/O Instructions
- Prevent all I/O Interrupts and Jump
- Cascading indirect addressing for more than 100 microseconds
- Cascading the Execute instruction for more than 100 microseconds
- Attempting to write into any of the executive control registers (40_8–100_8 or 120_8–177_8)
- Attempting to write in violation of PSR bits 30 or 31
- Disable Day Clock
- Enable Day Clock
- Load Last Address Register
- Load PSR Designators
- Store PSR Designators

Guard mode is disabled by the occurrence of any interrupt.

5. Processor Input /Output Control Section

5.1. GENERAL DESCRIPTION

The input/output (I/O) control section of the SPERRY UNIVAC 1100/10 Systems Central Processor Unit (CPU) controls transmission of data between main storage and the peripheral subsystems. It communicates with a peripheral subsystem over one of 16 bidirectional I/O channels. Data is transmitted with all 36 bits of a word in parallel; thus each channel has 72 data lines (36 input and 36 output) plus control signal lines. Although most peripheral subsystems use both input and output lines, data flows in only one direction on a channel for a specific I/O instruction. Parity is generated and checked at the main storage and subsystem levels.

The I/O control section acts as a small processor to operate many peripheral subsystems concurrently. A programmed I/O instruction selects a specified channel and I/O device on the selected channel, and sets up the required conditions for a given activity. From that point on, the I/O control section automatically controls transmission of data to or from the subsystem at its natural speed. When a subsystem requests a word, the I/O control section refers to an access control word which specifies the location in main storage to or from which data is to be transferred.

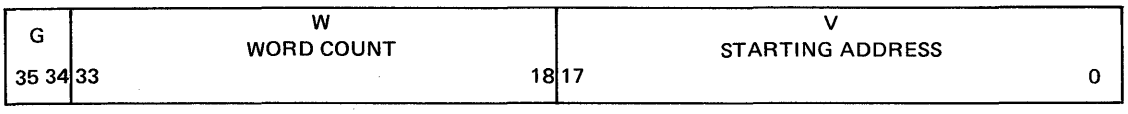
5.2. INTERNALLY SPECIFIED INDEX MODE

Each channel operates in one of three states: input, output, or function. Input and output are the data transmission states. The function state is actually an output state during which the processor sends one or more function words to the subsystem. Each function word specifies an operation to be performed by the subsystem.

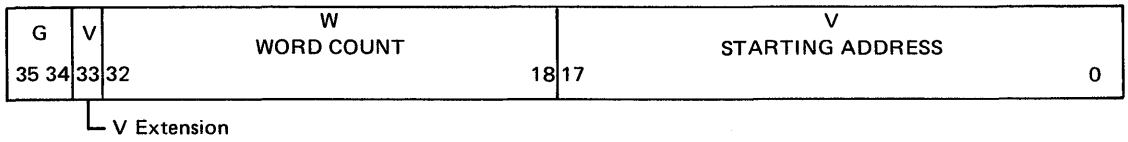
The actual word-by-word transmission (regardless of transfer state) is governed by an access control word stored in an access control register. Two of these registers, one for input and one for output, are assigned to each I/O channel (see Figure 3–1, registers 40_8 to 77_8).

Two formats of the ISI access control word apply depending on whether the system provides for 262K addressing or 524K addressing. These formats are as follows:

262K ADDRESSING



524K ADDRESSING



V 18 or 19 bits, the starting of next address in main storage for data transfer.
W 16 or 15 bits, the number of words to be transferred. It decreases by 1 each time a word is transferred.
G 2 bits, the incrementation control for V.
=00, increment V by 1 after each word is transferred
=10, decrement V by 1 after each word is transferred.
=01 or 11, do not change V.

In initiating an input/output operation, the processor stores an access control word in the input or output access control register associated with a given channel. Depending on the contents of G, the I/O control section transfers subsequent words to or from successive locations in main storage (increasing or decreasing addresses) or to or from a single location. After each transfer, the word count is decreased by one and tested for zero. A nonzero calls for transfer of the next word in the block; a zero terminates the transfer; and if the instruction calls for monitoring, the input/output monitor interrupt is set.

5.3. EXTERNALLY SPECIFIED INDEX MODE

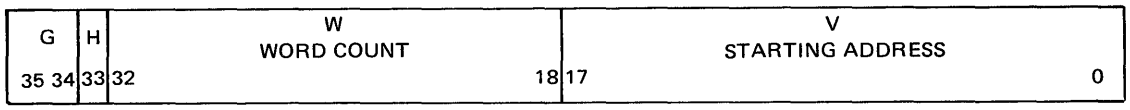
The externally specified index (ESI) mode, in conjunction with data communications equipment, allows multiplexed remote communication devices to communicate with main storage over a single I/O channel on a self-controlled basis without disturbing the main program. Each such remote device communicates with its own area of main storage.

Any I/O channel can be set to the ESI mode by means of a switch. Furthermore, by means of a patch card, an ESI channel can be set to operate in either half-word (18-bit) or quarter-word (9-bit) mode.

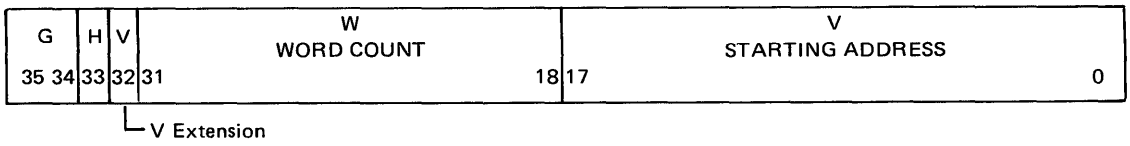
Because any channel can be used by many devices in ESI mode, data flow must be goverened by an access control word unique to the device currently in operation rather than to the channel as in ISI. These access control words are stored in main storage at addresses assigned to the devices. As a device transfers data, it presents the address of its own access control word; thus, no complicated program monitoring is necessary to control data flow.

As for the ISI mode, two ESI access control word formats also apply depending on addressing. The formats for the ESI access control word differs somewhat from that for ISI to enable control of half- and quarter-word transfers. The half-word access control word is as follows:

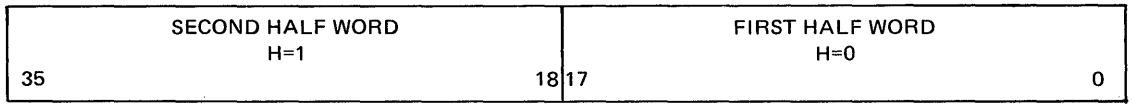
262K ADDRESSING



524K ADDRESSING



The G, W, and V fields have the same meaning as in the ISI access control word except that W is reduced to 15 or 14 bits and counts the characters to be transferred. There is also an H field, of one bit; this field is used to indicate which half of location V is to be used, as follows:

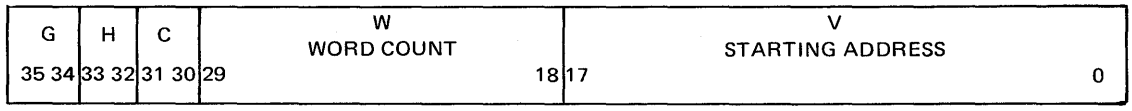


H=0; use first half-word of location V and switch H to 1.
H=1; use second half-word of location V, change V address as specified by G, and switch H to 0.

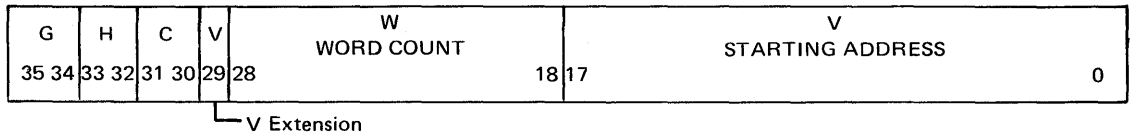
On input, the first half-word of an incoming message causes the associated ESI access control word to be transferred from main storage to the I/O control section. Since the H bit is zero the data goes to the lower half of location V. V is not altered, but H is set to 1 and W is decremented. The access control word is then returned to main storage until the next data from the same source arrives. At that time, the access control word is again transferred from main storage. Since H now equals 1, the data goes to the upper half of location V, address V is changed as specified by G, W is decremented, H is set to 0, and the access control word is stored. A similar sequence applies for output transfers.

Quarter-word operations are similar except that additional programmed control is provided in terminating transmission. For this purpose the access control word includes two extra control bits (C field).

262K ADDRESSING



524K ADDRESSING



G, W, and V have the same meanings as for ISI, though W is now only 12 or 11 bits long and now counts quarter words. H is the quarter-word designator designating the portion of V that is being addressed as follows:

FIRST QUARTER WORD		SECOND QUARTER WORD		THIRD QUARTER WORD		FOURTH QUARTER WORD	
35	H=00 27	26	H=01 18	17	H=10 9	8	H=11 0

Notice that the data is stored in reverse of the order used in half-word operation.

C is a two-bit control field that prevents loss of data by generating an extra monitor interrupt, if required, and an end-of-transmission bit during ESI output operation. The normal monitor interrupt occurs when W goes from 1 to 0. However, when bit 30 is set to 1, a monitor interrupt is generated as W decreases from 2 to 1. Similarly, if bit 31 is set to 1, the CPU I/O section sends an end-of-transmission bit with the data as W goes from 2 to 1.

5.4. BUFFER MODE DATA TRANSFERS

A buffer mode data transfer which occurs independently of the CPU control section is used to transfer data between main storage and the communication subsystem. Before the transfer, the CPU performs the following steps under control of the executive system:

1. Loads access control words into the locations specified by the ESI address.

2. Activates the channel to be used.

3. Sends a function word to the communication subsystem. This step is not required to effect transfers from low or medium speed communication terminal modules.

Step 2 is accomplished by one of the four instructions listed below. The access control word should specify a one-word dummy buffer since such a buffer is not normally used in the ESI mode.

LIC	Load Input Channel
LICM	Load Input Channel and Monitor
LOC	Load Output Channel
LOCM	Load Output Channel and Monitor

Step 3 is performed by a Load Function in Channel instruction. In the ESI mode this instruction loads the access control word for the function into the output access control register for the channel and forces one external function transfer.

Data is then transferred in quarter-words between main storage and the subsystem without CPU intervention. Each time a partial word is transferred to or from storage, 1 is automatically subtracted from the count field of the access control word. When this count becomes zero, the transfer is complete. If monitor is specified, an internal I/O monitor interrupt is set.

5.5. INPUT/OUTPUT INFORMATION WORDS

Four types of information words are transmitted between the CPU and the peripheral subsystems. Each is accompanied by a control signal which identifies it for the receiving unit. The four types of information words are:

- Data words, which go either direction.
- Function words, which go from CPU to subsystem.
- Identifier words, which go from CPU to subsystem.
- Status words, which go from subsystem to CPU.

5.5.1. Data Words

Data is transmitted all bits in parallel, the number of bits depending on the mode of operation. That is, for ISI, 36-bit parallel; for ESI, 18-bit or 9-bit parallel.

To identify an input word as data, the subsystem sends an input data request signal with the word. The I/O section acknowledges receipt by returning an input acknowledge signal. Similarly, on output the subsystem requests data by means of an output request. As soon as data is available, the I/O control section sends the data and supplies an output acknowledge signal to the subsystem.

5.5.2. Function Words

The 36-bit function word contains operating instructions for the peripheral subsystem. This includes a function code specifying what is to be done and a unit select code if the subsystem controls more than one peripheral device.

The I/O control section identifies the information as a function word by sending an external function signal after placing the word on the data lines.

5.5.3. Identifier Words

The identifier word is used as a search key for any of the search functions. When such a word is sent to a subsystem that is set to perform a search operation, an accompanying external function signal identifies it as an identifier word. The subsystem stores the identifier word in a special register and compares it with each word read at the peripheral device until it finds an identical word. It then terminates the search and stores the location of the matching word in the status word for further use by the program. On a search/read function the subsystem starts reading as soon as the matching word is found.

5.5.4. Status Words

The 36-bit status word, generated by the subsystem, indicates whether an I/O instruction has been completed normally. Indicators within the word indicate any abnormal or error conditions. The CPU stores the word in its external interrupt status location for analysis and further action (see 4.3).

5.6. PRIORITY CONTROL

Input/output operations are arranged in sequence by a priority control network within the input/output section of the CPU. Although all sixteen I/O channels may be available for data transmissions between the processor and peripheral units at the same time, only one channel can communicate with the central processor at any given instant. Priority control circuits resolve situations in which two or more I/O channels simultaneously seek to communicate with the CPU. The following lists the priorities in descending sequence. If two or more requests have the same priority, priority is based on the I/O channel number (lower numbered channel first).

1. Output Data Request (ODR)
2. Input Data Request (IDR)
3. Real Time Clock Decrement
4. Power Loss Interrupt
5. I/O Parity Error Interrupt
6. External Interrupt (ESI)
7. Input Monitor Interrupt (ESI)
8. Output Monitor Interrupt (ESI)
9. Real Time Clock Interrupt
10. External Interrupt (ISI)
11. Input Monitor Interrupt (ISI)
12. Output Monitor Interrupt (ISI)
13. Function Monitor Interrupt
14. Interprocessor Interrupt

5.7. INPUT/OUTPUT INSTRUCTIONS

The I/O instructions allow the program to activate, test, deactivate, and control I/O operations.

The following two instructions condition the I/O section of the CPU to send one or more function words to the specified subsystem.

Load Function in Channel
Load Function in Channel and Monitor

The following four instructions condition the I/O section to accept input data words from, or to send output data words to the specified subsystem, as requested by the subsystem. The maximum number of words is specified by the operand for the instruction for ISI operation.

Load Input Channel
Load Input Channel and Monitor
Load Output Channel
Load Output Channel and Monitor

The following two instructions have no effect upon the operation of the I/O channels but test the specified channel to determine if it is active in the specified mode.

Jump Input Channel Busy
Jump Output Channel Busy

Similarly, the following instruction does not have any effect upon the operation of the specified channel but tests the specified output channel to determine if the first function word has been sent to the subsystem after the channel has been activated in the function mode.

Jump Function in Channel

The following two instructions enable and disable the servicing of external interrupts by the I/O section.

Allow All Channel External Interrupts
Prevent All Channel External Interrupts

The following two instructions enable the program to terminate operation of an I/O channel. They are used principally when initiating operations on a channel that has not terminated properly.

Disconnect Input Channel
Disconnect Output Channel

5.7.1. Monitored Instructions

Input mode, output mode, or function mode can be activated on a channel either with or without monitor.

At the end of a monitored operation after all of the desired data has been transferred in the ISI mode, the channel is deactivated and the I/O section generates a monitor interrupt for the CPU; this informs the executive system that the transfer is complete. This is not the case in ESI mode. The Load Function in Channel and Monitor (LFCM) instruction never results in a monitor interrupt when it specifies a channel conditioned for ESI operation.

6. Main Storage

6.1. GENERAL

The main storage of the SPERRY UNIVAC 1100/10 Systems is a high performance, fast access semiconductor storage for instructions and data. Its design fully supports the concepts of multiprogramming, modularity, and reliability around which an entire 1100/10 System is constructed. Among the featured characteristics are:

- 1125 nanosecond cycle time
- 131K; 262K; 393K; or 524K 36-bit words
- Parity checking on all storage references
- Error checking and correction — provides correction of single bit errors
- Error correction interrupts — allows logging of operand and instruction error corrections
- Hardware storage protection — lockout boundaries establishable in 512-word increments
- Relative addressing and dynamic program relocatability through program base registers
- Online serviceability — storage modules may be placed offline for servicing without stopping the entire system.

Each main storage unit performs the following functions:

- Accepts an address from the processor
- Stores or retrieves a word at the address
- Issues an acknowledgement signifying that a storage reference has been completed
- Generates or checks parity on all data read from storage and delivers an interrupt signal to the processor if a parity error occurs.
- Provides single bit error correction, and double bit error detection.

The modular storage concept has significant advantages for the immediate as well as the future needs of the system. Addition of banks of storage is simplified.

6.2. STORAGE UNIT

Each storage unit includes 131,072 (131K) words which may be expanded to 262,144 (262K) words. Each word is 45 bits long; consisting of 36 data bits, two bits for half-word parity checking, and seven internal error correcting code bits. The main components of each type of module are an address register, a 36-bit read/restore register, parity checking circuits, error checking and correction circuits, and request/acknowledge circuits.

The 17-bit address register of each storage module provides addressing for 262K words. Since an 18-bit address is generated within the processor at each storage reference, two bits are available for selection of one of the four possible storage modules. An optional 131K addressing mode is selectable in which the 18th bit of the address is used to select one of the two possible 131K storage modules. In addition, optional 524K addressing provides a bank selection bit which is used to select modules above or below 262K, thus permitting up to 524K of main storage.

For each word to be written in storage, a 7-bit error correcting code is generated from the write data (36 data bits and two parity bits) and the resultant 45-bit word stored. If during a read or partial write, a single bit error is detected in the stored data, the error correcting code is used to correct the data. If multiple errors are detected in the stored data, the processor is notified with a data parity error interrupt signal.

6.3. PACKAGING

A basic cabinet may contain 131K words of storage or 262K words of storage. Each cabinet contains its own power supply and cooling. The multi-module access (MMA) feature provides a second path to the storage unit for multiprocessor configurations. The MMA is housed in the basic cabinet.

6.4. STORAGE CAPACITY

Available main storage capacity ranges from the system minimum of 131,072 words to the system maximum of 524,288 words and is available in any combination of 131K and 262K storage units. Examples of some storage unit combinations are given below.

262,144 words – one 262K storage unit, or two 131K storage units

524,288 words – four 131K storage units, two 262K storage units, or one 262K storage unit plus two 131K storage units

6.5. STORAGE PROTECTION

To prevent inadvertent program reference to out-of-range storage addresses, the 1100/10 Systems CPU includes a hardware storage protection feature. The controlling element in this feature is the storage limits register, the contents of which are as follows:

INSTRUCTION AREA		DATA AREA	
UPPER BOUNDARY	LOWER BOUNDARY	UPPER BOUNDARY	LOWER BOUNDARY
35 27	26 18	17 9	8 0

The storage limits register (SLR) is loaded by the executive system to establish allowable operating areas for the program currently in execution. These areas are termed the program instruction (I) and data (D) areas. Before control is given to a particular program, the executive system loads the SLR with the appropriate I and D boundaries.

Before each main storage reference for operand acquisition or result storage, the processor performs a limits check on the address, comparing it against the limits of either the I- or D-field of the SLR. An out-of-limits address generates a guard mode interrupt, thereby allowing the executive system to regain control and take appropriate action. Additional storage protection is provided by allowing an inhibit of writing in either, or both, the I- and D-bank as controlled by PSR bits 30 and 31. With 524K addressing, bit 18 is appended to the absolute address after the storage limits are checked.

6.5.1. Storage Protection Modes

The executive system can establish two different modes of storage protection by means of control fields in the processor state register (PSR) described in Section 4. Normally, the executive system itself operates in open mode; that is, the SLR may be loaded but the PSR is set to disregard this, and the executive system can reference any location in main storage.

6.5.1.1. User Program Mode

In the user program mode, read, write and jump storage protection is in effect. Therefore, user programs are limited to those areas assigned by the executive system. If the user program attempts to read, write or jump to an out-of-limits address, an interrupt returns control to the executive system for remedial action.

Read/jump protection allows the executive system to stop the program at the point of error, terminate it, and provide diagnostic information to the programmer thereby minimizing wasted time and smoothing the checkout process.

6.6. RELATIVE ADDRESSING

Relative addressing is a feature of great significance in multiprogramming time-sharing, and real time operations, for it allows storage assignments for any program to be changed dynamically by the executive system to provide continuous storage for operation of another program, and it permits programs to dynamically request additional main storage according to processing needs. An additional advantage is that system programs stored in auxiliary storage may be brought in for operation in any available area without complicated relocation algorithms.

Relative addressing is provided by base registers contained within the CPU. Two separate registers control the basing of the program instruction (I-bank) and data banks (D-bank), and a third register controls the selection of the appropriate base register.

6.7. OVERLAPPING

Overlapping enables the CPU to retrieve the current operand and the next instruction simultaneously. The CPU can determine whether the current operand and the next instruction lie in the same main storage unit, and if they do not, it retrieves the two words in parallel, thereby increasing performance nearly 100 percent.

Overlapping is made possible by dividing the program elements into logical structures called banks. A bank may be defined as an I-bank or as a D-bank. By convention, but not necessity, the instructions of a program are placed in I-banks while the data portions (operands) are placed in D-banks. This allows the executive system to appropriately separate the instructions and operands.

7. Auxiliary Storage and Peripheral Subsystems

7.1. AVAILABLE AUXILIARY STORAGE AND PERIPHERAL EQUIPMENT

Auxiliary storage and peripheral subsystems are attached to the SPERRY UNIVAC 1100/10 Systems Central Processor Unit (CPU) through general purpose input/output (I/O) channels, which have no restriction as to the manner in which peripheral subsystems may be attached. The governing factor for peripheral attachment is the transfer rate of the devices in the subsystem. Since the channels are numbered in order of priority, real-time operations with very high transfer rates should be attached to the lower numbered channels which have the higher priority.

The SPERRY UNIVAC 1100/10 Systems Auxiliary Storage and Peripheral Subsystems are:

- Mass Storage

  SPERRY UNIVAC 8425 Disc Subsystem
  SPERRY UNIVAC 8405 Disc Subsystem
  SPERRY UNIVAC 8430 Disc Subsystem
  SPERRY UNIVAC 8433 Disc Subsystem

- High Performance Drum

  FH–432/FH–1782 Magnetic Drum Subsystem

- Magnetic Tape

  UNISERVO 14 Magnetic Tape Subsystem
  UNISERVO 12 Magnetic Tape Subsystem
  UNISERVO 16 Magnetic Tape Subsystem
  UNISERVO 20 Magnetic Tape Subsystem

- Bytes Interface Paper Peripheral Subsystems

  UNIVAC 0770 Printer
  UNIVAC 0716 Card Reader
  UNIVAC 0604 Card Punch
  UNIVAC 0920 Paper Tape via the C/SP

- UNIVAC Multi-Subsystem Adapter (MSA)
- UNIVAC Communications/Symbiont Processor (C/SP)

Auxiliary storage and peripheral subsystems used on earlier model SPERRY UNIVAC 1100 Series Systems can be configured, but Sperry Univac will not develop any new software for these destandardized subsystems.

7.2. SPERRY UNIVAC DISC SUBSYSTEMS

Sperry Univac offers a variety of disc storage subsystems for use on the 1100/10 Systems. Basic subsystems can include:

SPERRY UNIVAC 8425 Disc
SPERRY UNIVAC 8405 Fixed Head Disc
SPERRY UNIVAC 8430 Disc
SPERRY UNIVAC 8433 Disc

The 8405 Fixed Head Disc Subsystem is the primary disc subsystem for higher performance systems.

The operating system disc pack includes a 2000-word bootstrap block, executive system overlays and tables, and a swap area for active demand. The disc pack would also be used for storing processor libraries and symbionts.

Additional disc subsystems can be used for the higher activity user program data files. This may be an extreme case, however, since the operating system uses a small percentage of the capacity of a disc pack. A more normal balance would incorporate the total system on one disc, the batch symbiont data pool on a second, and user files on the remainder. Once the system is loaded, the additional space could be used for user program files. For example, the disc would contain the executive system resident, as indicated previously, and the remaining area could be loaded with the user program and/or data files.

A disc subsystem under the executive system greatly facilitates file handling with or without a high speed drum subsystem. One reason for this is the capability within the executive system to pre-position read/write heads. Essentially, the executive system accesses the disc request queue and pre-positions the reading mechanism for each request when the request involves an inactive disc pack. The level of pre-positioning is equal to the number of disc packs within the subsystem. This, of course, optimizes accessing time.

The advantages achieved by implementing disc subsystems include:

- substantially increased throughput performance over older type disc subsystems
- provision for incremental growth
- expanded potential for online processing
- enhanced capabilities for real time and multiprogramming
- intermix of 8405 (fast access) and 8430 or 8433 (large capacity) on same subsystem
- error correction code
- command retry

Disc subsystems provide the 1100/10 Systems with an expandable, fixed or removable direct access, external storage medium.

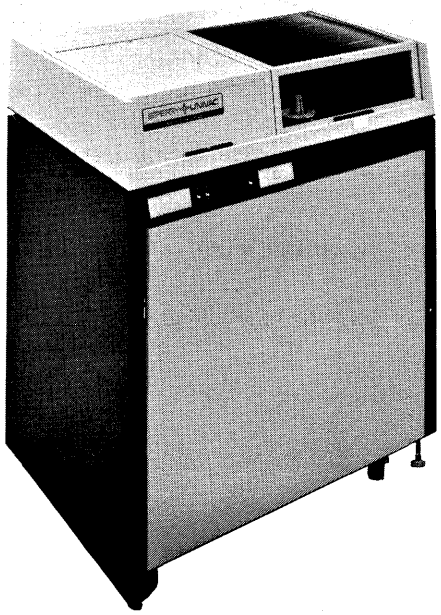
Data is transferred between the CPU and the disc subsystems one word at a time. The control units for the 8405, 8430, 8433, and 8425 Disc Subsystems provide for connection to the word channels of the 1100/10 Systems. They also provide for data translation, function chaining, and command chaining.

The disc subsystems offer many processing advantages, especially in applications where rapid file processing and sort/merge routines are prevalent. The removability characteristics of the disc packs (except 8405 Disc) permit virtually unlimited offline storage and easy interchange of information without conversion to other media.

The disc subsystems also provide for simultaneous dual access operation and prepositioning of access arms where applicable. This implies:

- Simultaneous read/read, read/write, write/read, write/write concurrent with positioning functions.
- Alternate data and command paths available to any component of the system.

7.2.1. SPERRY UNIVAC 8425 Disc Subsystem



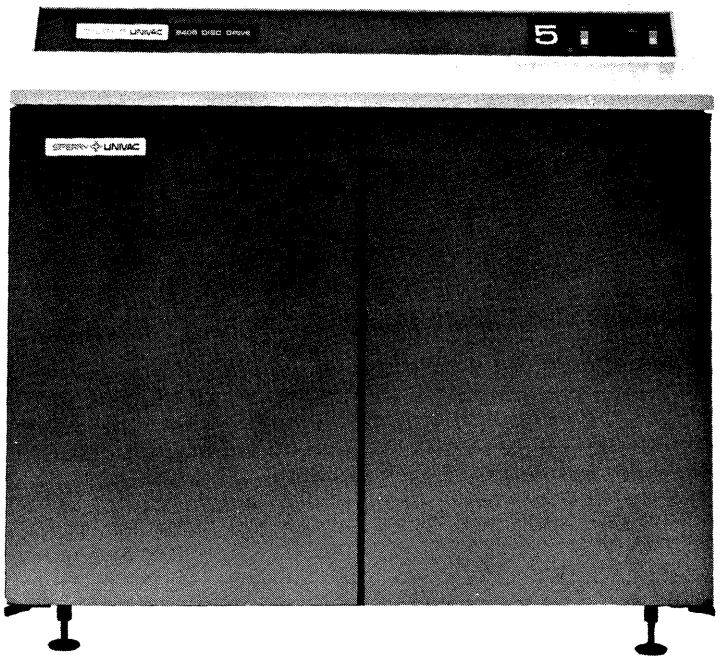
The SPERRY UNIVAC 8425 Disc Subsystem offers a large storage capacity of up to 466 million bytes or up to 87.3 million 36-bit words of data online. A single disc pack provides for up to 49 million bytes or 10.9 million 36-bit words. Maximum capacity using free format, one record per track, is 58 million bytes.

Each disc pack contains 11 discs. Twenty read/write heads are mounted on a single accessor mechanism which moves the 20 heads in unison between the periphery and the central area of the disc. The accessor mechanism can assume one of 406 tracks across the disc surface. The simultaneous head movement creates 406 addressable data recording cylinders in the disc pack. Each cylinder contains twenty tracks, numbered 0 through 19. The addressing of an individual track in the pack is by track number (000—405) and by read/write head number (0—19).

Access to different tracks within a cylinder is faster than access to tracks in different cylinders since changing tracks requires only electronic switching whereas accessing a different cylinder requires physical movement of the accessor mechanism. There are 8120 (406 x 20) tracks in a disc pack assembly.

SPERRY UNIVAC 8425 DISC SUBSYSTEM CHARACTERISTICS	
NUMBER OF DISC STORAGE UNITS PER CONTROL UNIT	2–8
NUMBER OF DISC PACKS PER STORAGE UNIT	1
NUMBER OF R/W ACCESSOR MECHANISMS	1
NUMBER OF R/W HEADS PER DISC PACK	20 (one per surface)
NUMBER OF TRACKS PER DISC SURFACE	406
NUMBER OF RECORDING SURFACES PER DISC PACK	20
NUMBER OF ADDRESSABLE TRACKS PER SURFACE	406
NUMBER OF ADDRESSABLE TRACKS PER DISC PACK	8120
NUMBER OF WORDS PER RECORD	112
NUMBER OF 112 WORD RECORDS PER TRACK	12
CAPACITY PER DISC PACK	10,913,280 36-bit words 49,109,760 bytes
MINIMUM ACCESS TIME	7.5 milliseconds
AVERAGE ACCESS TIME	29 milliseconds
MAXIMUM ACCESS TIME	55 milliseconds
DISC PACK SPEED	2400 rpm
DATA TRANSFER RATE	69,333 words per second 312,000 bytes per second

7.2.2. SPERRY UNIVAC 8405 Fixed Head Disc Subsystem

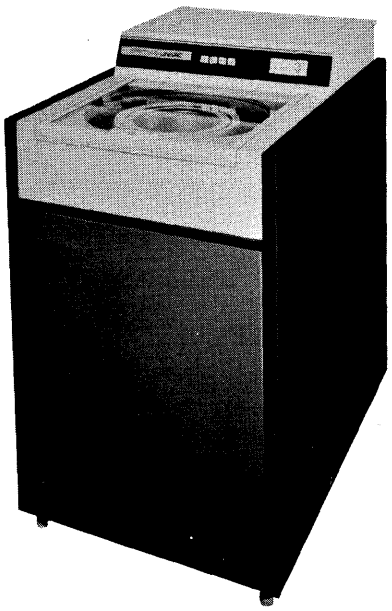


The SPERRY UNIVAC 8405 Fixed Head Disc Subsystem offers a fast access storage capacity of up to 24.7 or 49.5 million bytes, or up to 5.5 or 11.0 million 36-bit words of data online.

The 1100/10 Systems are capable of retrieving specific records without a sequential search through the record files. This retrieval permits direct access to active files and gives more efficient throughput for the processor. Random inquiries also can be made while records are being processed, or the records can be supplied sequentially for processing. Fixed heads are used in the 8405 disc storage unit. Each disc surface has eight read/write head pads, each pad containing nine read/write elements (or channels). This arrangement provides 72 read/write channels per disc surface. Each disc surface has 72 tracks, and each track is addressed by a fixed read/write head. Each disc storage unit contains 6 or 12 recording surfaces; 432 or 864 read/write heads are mounted in fixed positions for these recording surfaces. Because the heads are fixed and switched electronically, access time is reduced to an average of 8.3 milliseconds. The disc pack is non-removable. The 8405 disc storage unit may be mixed with 8430 and 8433 disc storage units on the same control unit.

SPERRY UNIVAC 8405 FIXED HEAD DISC SUBSYSTEM CHARACTERISTICS		
	8405–00	**8405–04**
NUMBER OF DISC STORAGE UNITS PER CONTROL UNIT	1–8	1–8
NUMBER OF DISC DRIVES PER STORAGE UNIT	1	1
NUMBER OF R/W HEAD ACCESSOR MECHANISMS	1 (fixed head)	1 (fixed head)
NUMBER OF R/W HEAD PADS (9 R/W ELEMENTS EACH)	96	48
NUMBER OF TRACKS PER DISC SURFACE	72	72
NUMBER OF RECORDING SURFACES PER DISC UNIT	12	6
NUMBER OF ADDRESSABLE TRACKS PER SURFACE	72	72
NUMBER OF TRACKS PER DISC UNIT	864	432
NUMBER OF 36-BIT WORDS PER RECORD	112	112
MAXIMUM NUMBER OF RECORDS PER TRACK	16	16
CAPACITY 36-BIT WORDS PER DISC UNIT	1,376,256	688,128
AVERAGE LATENCY TIME	8.3 milliseconds	8.3 milliseconds
DISC DRIVE SPEED	3,600 rpm	3,600 rpm
STORAGE TRANSFER RATE	622,000 bytes per second 138,222 36-bit words per second	622,000 bytes per second 138,222 36-bit words per second
DUAL ACCESS	Feature available	Feature available

7.2.3. SPERRY UNIVAC 8430 Disc Subsystem



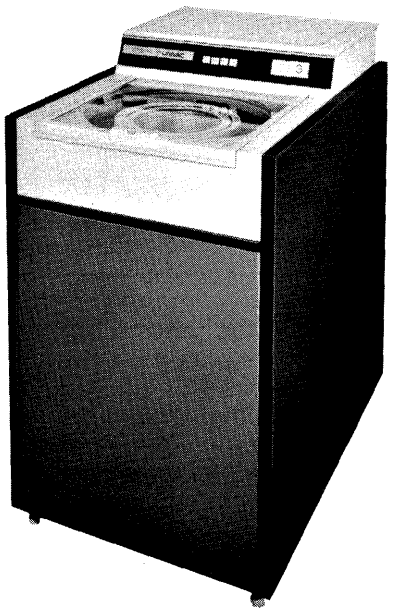
The SPERRY UNIVAC 8430 Disc Subsystem offers a large storage capacity of up to 1600 million bytes or up to 275 million 36-bit words of data online. A single disc pack provides for 77.3 million bytes or 17.1 million 36-bit words using 112-word records. Maximum capacity using free format, one record per track, is 100 million bytes or 22.2 million 36-bit words.

Each disc pack contains 11 discs. Nineteen read/write heads are mounted on a single accessor mechanism which moves the 19 heads in unison between the periphery and the central area of the disc. The accessor mechanism can assume one of 411 tracks across the disc surface. The simultaneous head movement creates 411 addressable data recording cylinders in the disc pack. Each cylinder contains nineteen tracks, numbered 0 through 18. The addressing of an individual track in the pack is by track number (000–410) and by read/write head number (0–18).

Access to different tracks within a cylinder is faster than access to tracks in different cylinders since changing tracks requires only electronic switching whereas accessing a different cylinder requires physical movement of the accessor mechanism. There are 7809 (411 x 19) tracks in a disc pack assembly. The 8430 disc storage unit may be mixed with 8405 and/or 8433 disc storage units on the same control unit.

SPERRY UNIVAC 8430 DISC SUBSYSTEM CHARACTERISTICS	
NUMBER OF DISC STORAGE UNITS PER CONTROL UNIT	1–16
NUMBER OF DISC PACKS PER STORAGE UNIT	1
NUMBER OF R/W HEAD ACCESSOR MECHANISMS	1
NUMBER OF R/W HEADS PER DISC PACK	19 (one per surface)
NUMBER OF TRACKS PER DISC SURFACE	411
NUMBER OF RECORDING SURFACES PER DISC PACK	19
NUMBER OF ADDRESSABLE TRACKS PER SURFACE	411
NUMBER OF ADDRESSABLE TRACKS PER DISC PACK	7809
NUMBER OF WORDS PER RECORD	112
NUMBER OF 112 WORD RECORDS PER TRACK	20
CAPACITY PER DISC PACK USING 112 WORD RECORDS	17,194,240 36-bit words 77,374,084 bytes
MAXIMUM CAPACITY PER DISC PACK USING FREE FORMAT–ONE RECORD PER TRACK	22,226,284 36-bit words 100,018,280 bytes
MINIMUM ACCESS TIME	7 milliseconds
AVERAGE ACCESS TIME	27 milliseconds
MAXIMUM ACCESS TIME	50 milliseconds
DISC PACK SPEED	3600 rpm
DATA TRANSFER RATE	179,111 36-bit words per second 806,000 bytes per second
DUAL ACCESS	Feature available

7.2.4. SPERRY UNIVAC 8433 Disc Subsystem



The SPERRY UNIVAC 8433 Disc Subsystem offers a large storage capacity of up to 3200 million bytes or up to 550 million 36-bit words of data online. A single disc pack provides for 154.7 million bytes or 34.3 million 36-bit words using 112-word records. Maximum capacity using free format, one record per track, is 200 million bytes or 44.4 million 36-bit words.

Each disc pack contains 11 discs. Nineteen read/write heads are mounted on a single accessor mechanism which moves the 19 heads in unison between the periphery and the central area of the disc. The accessor mechanism can assume one of 815 tracks across the disc surface. The simultaneous head movement creates 815 addressable data recording cylinders in the disc pack. Each cylinder contains nineteen tracks numbered 0 through 18. The addressing of an individual track in the pack is by track number (000—814) and by read/write head number (0—18).

Access to different tracks within a cylinder is faster than access to tracks in different cylinders since changing tracks requires only electronic switching whereas accessing a different cylinder requires physical movement of the accessor mechanism. There are 15,485 (815 x 19) tracks in a disc pack assembly. The 8433 disc storage unit may be mixed with 8405 and/or 8430 disc storage units on the same control unit.

SPERRY UNIVAC 8433 DISC SUBSYSTEM CHARACTERISTICS	
NUMBER OF DISC STORAGE UNITS PER CONTROL UNIT	1–16
NUMBER OF DISC PACKS PER STORAGE UNIT	1
NUMBER OF R/W HEAD ACCESSOR MECHANISMS	1
NUMBER OF R/W HEADS PER DISC PACK	19 (one per surface)
NUMBER OF TRACKS PER DISC SURFACE	815
NUMBER OF RECORDING SURFACES PER DISC PACK	19
NUMBER OF ADDRESSABLE TRACKS PER SURFACE	815
NUMBER OF ADDRESSABLE TRACKS PER DISC PACK	15,485
NUMBER OF WORDS PER RECORD	112
NUMBER OF 112 WORD RECORDS PER TRACK	20
CAPACITY PER DISC PACK USING 112 WORD RECORDS	34,388,480 36-bit words 154,748,160 bytes
MAXIMUM CAPACITY PER DISC PACK USING FREE FORMAT–ONE RECORD PER TRACK	44,452,555 36-bit words 200,036,500 bytes
MINIMUM ACCESS TIME	10 milliseconds
AVERAGE ACCESS TIME	30 milliseconds
MAXIMUM ACCESS TIME	55 milliseconds
DISC PACK SPEED	3600 rpm
DATA TRANSFER RATE	179,111 36-bit words per second 806,000 bytes per second
DUAL ACCESS	Feature available

7.3. FLYING HEAD DRUMS

The flying head (FH) series of high speed large capacity magnetic drum storage units, offered by Sperry Univac, provide modular auxiliary storage essential for the operation of large and complex systems. These units vary from the high speed FH–432 Magnetic Drum (with an average access time of 4.3 milliseconds) to the large capacity (2 million 36-bit words) FH–1782 Magnetic Drum which provides extensive fast access storage that can be used for large data files that have to be referenced frequently. Flying head magnetic drum subsystems have an individual read/write head for each track.

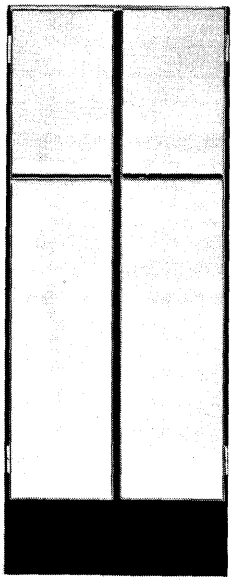
7.3.1. FH–432/1782 Magnetic Drum Subsystem

A valuable characteristic of the 1100/10 Systems Magnetic Drum Subsystem is the ability to associate, in the same subsystem, the high speed FH–432 Magnetic Drum with the fast high capacity FH–1782 Magnetic Drum. Any combination of eight drums may be mixed on a subsystem.

This subsystem arrangement is of significant importance in the 1100/10 Systems storage configuration. An efficient blend can be made of high speed storage (for rapidly required software, program segments, tables, and indices) with greater access time but large capacity storage (for less frequently used program segments, data files, and message assembly/disassembly areas). A judicious mix of speed, capacity, and economy can be planned and the mix can readily be altered as requirements change. Character transfer rates are identical for the FH–432 and FH–1782 Magnetic Drums. The only functional difference is the difference in access time and in capacity.

This subsystem is available in both single- and dual-channel versions to provide a hierarchy of auxiliary storage for the CPU. The dual-channel version includes two electrically and logically independent control units, each on a different I/O channel. This enables simultaneous operation of any two drums in the subsystem.

7.3.1.1. FH–432 Magnetic Drum



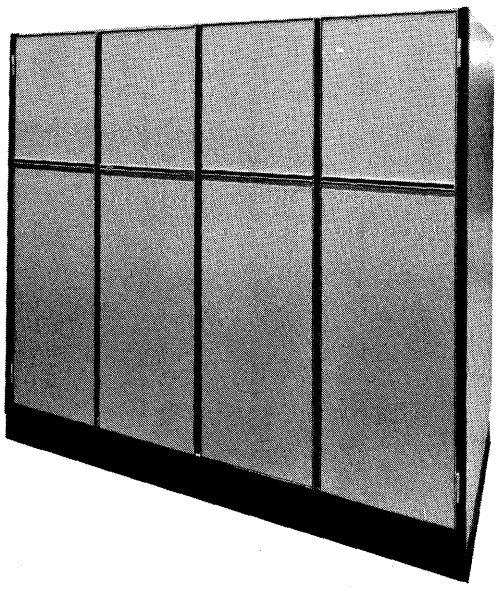
The FH–432 Magnetic Drum contains 262,144 36-bit words of storage. To augment the systems, cabinets may be added, each containing one drum with a storage capacity of 262,144 36-bit words. Of the 486 tracks on each drum, 384 are used for data; the remaining tracks are used for spares, parity, and timing functions. There are 2,048 words of data per three tracks. Reading and writing are 3-bit parallel operations on all three tracks of a band simultaneously. Thus the maximum transfer rate is 240,000 words or 1,440,000 alphanumeric characters per second.

Up to eight FH–432 Magnetic Drums may be accommodated in a single subsystem, affording a maximum subsystem capacity of 2,097,152 words or 12,582,912 alphanumeric characters.

FH–432 Magnetic Drums may be intermixed with FH–1782 Magnetic Drums in the same subsystem to provide a power blend of ultrahigh speed and large capacity storage.

FH–432 MAGNETIC DRUM CHARACTERISTICS	
STORAGE CAPACITY	262,144 computer words of 36 data bits plus parity bits, or 1,572,864 alphanumeric characters per drum
AVERAGE ACCESS TIME	4.3 milliseconds
DRUM SPEED	7,200 revolutions per minute
NUMBER OF READ/WRITE HEADS FOR DATA	384 – one per track
CHARACTER TRANSFER RATES	1,440,000; 720,000; 360,000; 180,000; 90,000
WORD TRANSFER RATES	240,000; 120,000; 60,000; 30,000; 15,000
I/O CHANNELS REQUIRED	1 or 2 per subsystem
NUMBER OF DRUMS PER SUBSYSTEM	1 to 8 (12,582,912 characters maximum)

7.3.1.2. FH–1782 Magnetic Drum



The FH–1782 Magnetic Drum is similar to the FH–432 Magnetic Drum except that average access time is four times greater and the storage capacity is eight times greater; this increase is achieved partly by an increase in the number of data tracks to 1,536 and partly by an increase in the recording density. Each track has its own read/write head, and average access time is 17 milliseconds.

A single FH–1782 Magnetic Drum stores 2,097,152 words, equivalent to 12,582,912 alphanumeric characters. Up to eight FH–1782 Magnetic Drums can be accommodated in a single subsystem giving a subsystem capacity of 100,663,296 characters.

The data transfer rate of the FH–1782 Magnetic Drum is equal to that of the FH–432 Magnetic Drum; this arrangement enables FH–1782 Magnetic Drums to be associated with FH–432 Magnetic Drums, in the same subsystem.

FH–1782 MAGNETIC DRUM CHARACTERISTICS	
STORAGE CAPACITY	2,097,152 computer words of 36 data bits plus parity bits, or 12,582,912 alphanumeric characters per drum
AVERAGE ACCESS TIME	17 milliseconds
DRUM SPEED	1,800 revolutions per minute
NUMBER OF READ/WRITE HEADS FOR DATA	1,890 (35 blocks with 54 heads per block)
CHARACTER TRANSFER RATES	1,440,000; 720,000; 360,000; 180,000; 90,000
WORD TRANSFER RATES	240,000; 120,000; 60,000; 30,000; 15,000
I/O CHANNELS REQUIRED	1 or 2 per subsystem
NUMBER OF DRUMS PER SUBSYSTEM	1 to 8 (100,663,296 characters maximum)

7.4. UNISERVO MAGNETIC TAPE SUBSYSTEMS

Four SPERRY UNIVAC Magnetic Tape Subsystems are available with the 1100/10 Systems. These subsystems may include:

UNISERVO 14 Magnetic Tape Units
UNISERVO 12 Magnetic Tape Units
UNISERVO 16 Magnetic Tape Units
UNISERVO 20 Magnetic Tape Units

The advantages provided by these magnetic tape subsystems include:

- wide range of performance
- intermix of UNISERVO 12/16/20 Magnetic Tape Units
- simultaneous dual access
- cartridge capability
- data translator features
- PE, NRZI – 7 and 9 track – variety of densities

Two basic methods of operation are available. These methods of operation are:

- Nonsimultaneous (single channel operation) – In this method of operation, one or more tape units are connected to a single I/O channel through the appropriate control unit. Only one function, on any one of the tape units, may be active at any single instant.
- Simultaneous Operation (two channel operation) – In this method of operation, two or more tape units are connected to two I/O channels through two control units.

The basic UNISERVO 14 Magnetic Tape Subsystem contains a single cabinet housing a control unit and two tape units. It is an industry compatible subsystem capable of normal operations using a recording mode of 9-track phase encoding at a density of 1600 bits per inch (bpi), and extended operations using recording modes of 7-track and 9-track non-return-to-zero inverted (NRZI) at densities up to 800 bpi. These recording modes can be used in any combination. Data rates with 9-track phase encoding are up to 96 kb per second.

Up to three optional auxiliary cabinets may be added to the basic subsystem unit, each auxiliary cabinet containing either one or two tape units. Other optional features further broaden the versatility of the subsystems. Also, the UNISERVO 14 can be mixed with paper peripherals on the same MSA.

A UNISERVO 12 Magnetic Tape Subsystem (partial-simultaneous subsystem) provides for read/read, read/write, write/read on any two individual UNISERVO 12 Magnetic Tape Units. All other tape units may be rewound concurrently. Write/write simultaneity operation is available only through separate master units. Appropriate simultaneous features must be added to the UNISERVO 12 Master Tape Units but are not software supported.

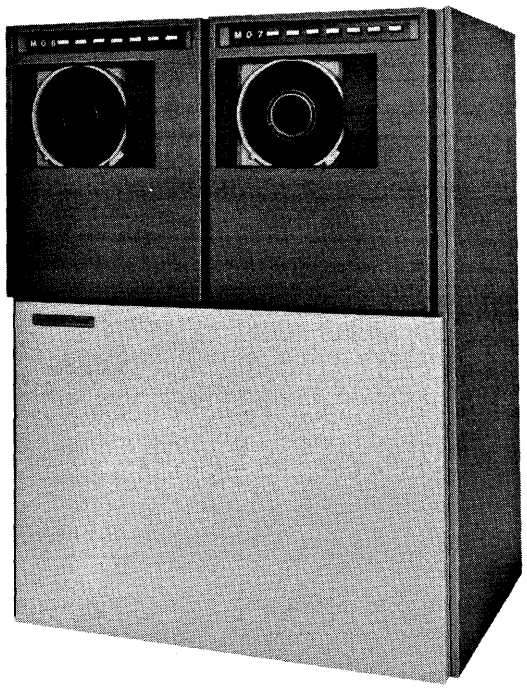
UNISERVO 16 Magnetic Tape Subsystems and UNISERVO 20 Magnetic Tape Subsystems (fully simultaneous dual access subsystems) provide for read/read, read/write, write/read and write/write operation on any two individual tape units. All other tape units may be rewound concurrently. Dual access provides two independent access paths to each UNISERVO 16 or UNISERVO 20 Magnetic Tape Unit. Tape units in these configurations must contain the appropriate dual access features. In addition to doubling the performance of the subsystem; simultaneous, dual access operation, includes complete power redundancy by virtue of individual power supplies per control unit. UNISERVO 12 Magnetic Tape Subsystems are not permitted in this configuration.

"On the fly" single-track mode error correction is standard for phase tapes. On 9-track NRZI tapes, single-track read error correction is provided by a second attempt of an operation after error detection and repositioning. This provides the ability to correct tape errors in either the forward or backward direction. This simplifies the error correction programming routines and assists in the recovery of unusual error conditions which otherwise would result in a nonrecoverable error. A programmable low gain read assists in the reading of tape records containing high noise levels.

Magnetic tape subsystems may consist of 16 tape units with the appropriate control units. Subsystems are available for both 7- and 9-track operation. The 7- and 9-track options permit data recorded in industry compatible form to be handled and records upgraded in line with the ASCII code and packed-decimal formats at the same time.

The control unit translates EBCDIC code to and from BCD code for the tape unit. Also, the control unit includes an integral MSA capability, and provides for optional data translators (Fieldata code to/from a 64-character subset of ASCII and Fieldata code to/from a 64-character subset of EBCDIC) and shared peripheral interface (SPI). The control unit can also accommodate UNISERVO 12 and 16 Magnetic Tape Units and thus provide for optional 7- and 9-track NRZI tape operation.

7.4.1. UNISERVO 14 Magnetic Tape Subsystem



The UNISERVO 14 Magnetic Tape Subsystem contains a basic cabinet which houses a control unit and two tape units capable of 9-track phase encoded recording at a density of 1600 bits per inch (bpi). A maximum subsystem configuration contains one basic cabinet and three auxiliary cabinets, with eight tape units. Each auxiliary cabinet always provides the distribution circuits for either one or two tape units. The subsystem can intermix recording modes provided the appropriate optional features are included. The dual density version permits 9-track phase encoded (PE) and non-return-to-zero-inverted (NRZI) recording at densities of 1600 bpi for PE and 800 bpi for NRZI when this feature is included. Also, 7-track NRZI recording at densities up to 800 bpi can be added when this feature is included.

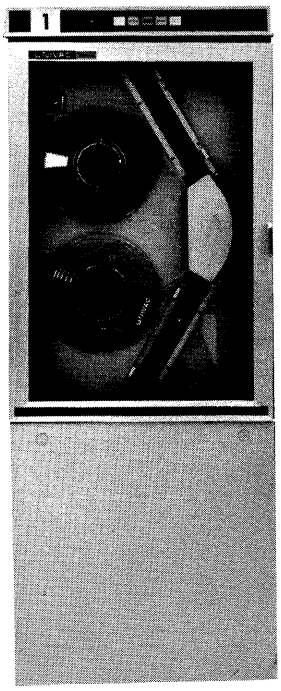
Industry-new features incorporated into the standard UNISERVO 14 Magnetic Tape Subsystem include: the automatic load and threading feature, and the capability of loading from either the standard reel or cartridge. No special adapters are required for either of these two advanced design features.

The subsystem may also be operated in conjunction with paper handling peripheral equipments at a transfer rate which is established by the speed of the associated peripheral.

Various configurations of the UNISERVO 14 Magnetic Tape Subsystem can be implemented to meet specific user requirements.

UNISERVO 14 MAGNETIC TAPE SUBSYSTEM CHARACTERISTICS	
RECORDING DENSITY (PE)	1600 bpi
RECORDING DENSITY (NRZI)	200, 556, or 800 bpi
TRANSFER RATE (PE)	96,000 frames per second
TRANSFER RATE (NRZI)	12,000; 33,360; or 48,000 frames per second
TAPE SPEED	60 inches per second
TAPE WIDTH	0.5 inch
TAPE LENGTH (MAX.)	2400 feet
BLOCK LENGTH	Variable
INTERBLOCK GAP	0.75 inch (7-track) 0.6 inch (9-track)
INTERBLOCK GAP TIME (7-TRACK)	17.0 milliseconds (nonstop) 25.0 milliseconds (start/stop)
INTERBLOCK GAP TIME (9-TRACK)	7.0 milliseconds (nonstop) 12.6 milliseconds (start/stop)
REVERSAL TIME	6.3 milliseconds
REWIND TIME	3 minutes (2400 feet)
DUAL DENSITY	Feature available

7.4.2. UNISERVO 12 Magnetic Tape Subsystem

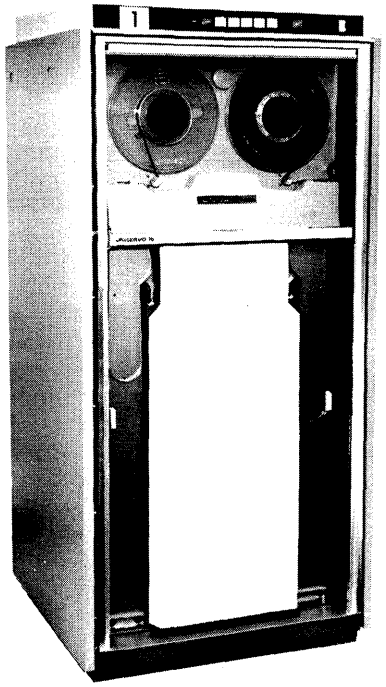


The UNISERVO 12 Magnetic Tape Subsystem is a low-cost medium performance subsystem with 7- or 9-track, 200, 556, or 800 bpi NRZI and 1600 bpi phase encoding as the available tape formats. One master tape unit, with a power supply and control circuits, controls up to three slave units. Up to 16 tape units are synchronously controlled by a UNISERVO 12/16 Control Unit.

This subsystem offers a peak transfer rate of 68,000 frames per second in phase encoding recording. The 7- or 9-track NRZI formats with a peak transfer rate of 34,000 frames per second also can be incorporated. Tape data validity checking facilities include read check while writing, longitudinal redundancy check, vertical parity check (9-track phase tapes) and cyclic redundancy check (diagonal, 9-track NRZI tapes).

UNISERVO 12 MAGNETIC TAPE SUBSYSTEM CHARACTERISTICS	
RECORDING DENSITY (PE)	1600 bpi
RECORDING DENSITY (NRZI)	200, 556, or 800 bpi
TRANSFER RATE (PE)	68,320 frames per second
TRANSFER RATE (NRZI)	8,540; 23,741; or 34,160 frames per second
TAPE SPEED	42.7 inches per second
TAPE WIDTH	0.5 inch
TAPE LENGTH (MAX.)	2,400 feet
BLOCK LENGTH	Variable
INTERBLOCK GAP	0.75 inch (7-track) 0.6 inch (9-track)
INTERBLOCK GAP TIME (7-TRACK)	17.6 milliseconds (nonstop) 23.6 milliseconds (start/stop)
INTERBLOCK GAP TIME (9-TRACK)	14.1 milliseconds (nonstop) 20.1 milliseconds (start/stop)
REVERSAL TIME	25 milliseconds
REWIND TIME	3 minutes (2,400 feet)

7.4.3. UNISERVO 16 Magnetic Tape Subsystem



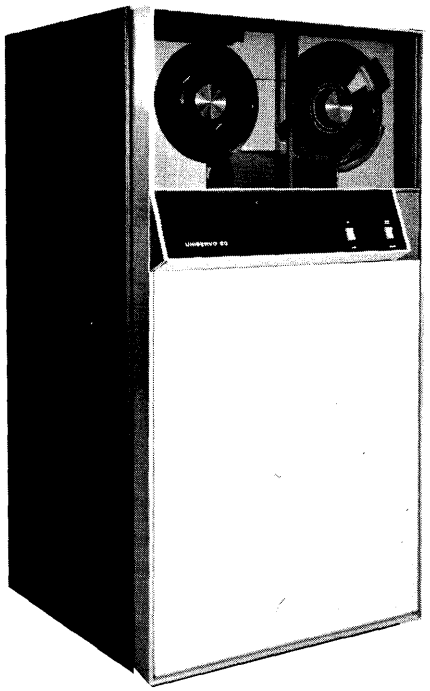
The UNISERVO 16 Magnetic Tape Subsystem consists of a control unit and from one to sixteen magnetic tape units. Another control unit may be used to achieve simultaneous dual access operation when appropriate features are present on the magnetic tape units.

The UNISERVO 16 Magnetic Tape Unit also provides a power window as an additional operator convenience. The 120-inch-per-second tape speed provides for a transfer rate of 192,000 frames per second.

Data may be recorded in variable-length blocks under program control with character and block (horizontal and vertical) parity. A read-after-write head allows immediate verification of all data written. Under the control of the software input/output handler, repeated read and write operations are undertaken in an attempt to recover from an error.

UNISERVO 16 MAGNETIC TAPE SUBSYSTEM CHARACTERISTICS	
RECORDING DENSITY (PE)	1600 bpi
RECORDING DENSITY (NRZI)	200, 556, or 800 bpi
TRANSFER RATE (PE)	192,000 frames per second
TRANSFER RATE (NRZI)	24,000; 66,720; 96,000 frames per second
TAPE SPEED	120 inches per second
TAPE WIDTH	0.5 inch
TAPE LENGTH (MAX.)	2400 feet
BLOCK LENGTH	Variable
INTERBLOCK GAP	0.75 inch (7-track) 0.6 inch (9-track)
INTERBLOCK GAP TIME (7-TRACK)	6.25 milliseconds (nonstop) 9.25 milliseconds (start/stop)
INTERBLOCK GAP TIME (9-TRACK)	5.0 milliseconds (nonstop) 8.0 milliseconds (start/stop)
REVERSAL TIME	10 milliseconds
REWIND TIME	2 minutes (2400 feet)
DUAL DENSITY	Feature available

7.4.4. UNISERVO 20 Magnetic Tape Subsystems



The UNISERVO 20 Magnetic Tape Subsystem consists of a control unit and from one to sixteen magnetic tape units. Another control unit may be used to achieve simultaneous dual access operation when appropriate features are present on the magnetic tape units.

The UNISERVO 20 Magnetic Tape Units provides operational conveniences such as power window, automatic tape threading, and the ability to use a wrap-around tape cartridge. The 200-inch-per-second tape speed provides for a transfer rate of 320,000 frames per second. Rewind rate is 500 inches per second providing a rewind time of 60 seconds for a full 2400-foot reel of tape.

The UNISERVO 20 Control Unit contains all the necessary logic and storage facilities for data control transfer between the 1100/10 Systems I/O channel and the tape units; the word and command formats are compatible with those required by the 1100/10 Systems and the tape units.

UNISERVO 20 MAGNETIC TAPE SUBSYSTEM CHARACTERISTICS	
TRANSFER RATE (PE)	320,000 frames per second
RECORDING DENSITY (PE)	1600 bpi
TAPE SPEED	200 inches per second
TAPE WIDTH	0.5 inch
TAPE LENGTH (MAX.)	2400 feet
BLOCK LENGTH	Variable
INTERBLOCK GAP	0.6 inch
TRACKS ON TAPE	9 tracks, 8 data, 1 parity
UNITS PER CONTROL	16
STANDARD FEATURES	Backward read, automatic tape threading, power window, cartridge loading, quick release hub
INPUT/OUTPUT CHANNELS REQUIRED	1 or 2
REWIND TIME	1 minute (2400 feet)

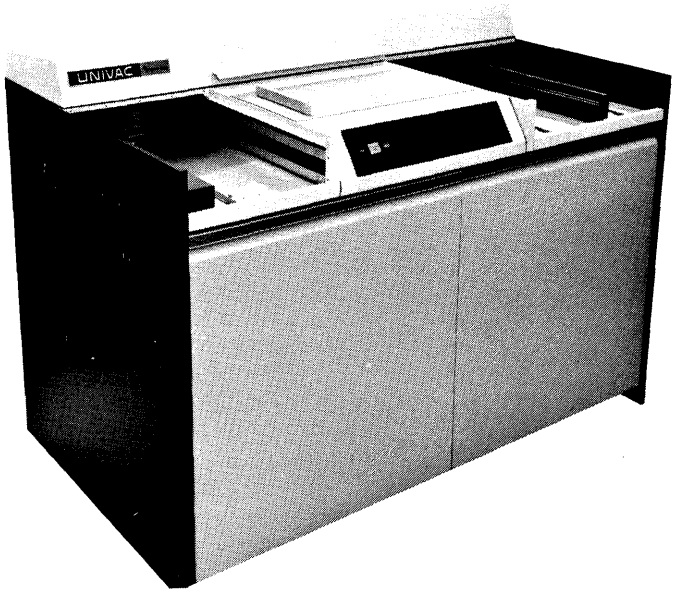
7.5. BYTE INTERFACE PAPER PERIPHERALS

The following paper peripherals are connected to the 1100/10 Systems via the UNIVAC Communications/Symbiont Processor (C/SP), or the UNIVAC Multi-Subsystem Adapter (MSA):

0716 Card Reader	– MSA, or C/SP
0770 Printer	– MSA, or C/SP
0604 Card Punch	– MSA, or C/SP
0920 Paper Tape Reader and Punch	– C/SP

The UNISERVO 14 Magnetic Tape Subsystem may be mixed with paper peripherals on the same MSA.

7.5.1. UNIVAC 0716 Card Reader Subsystem



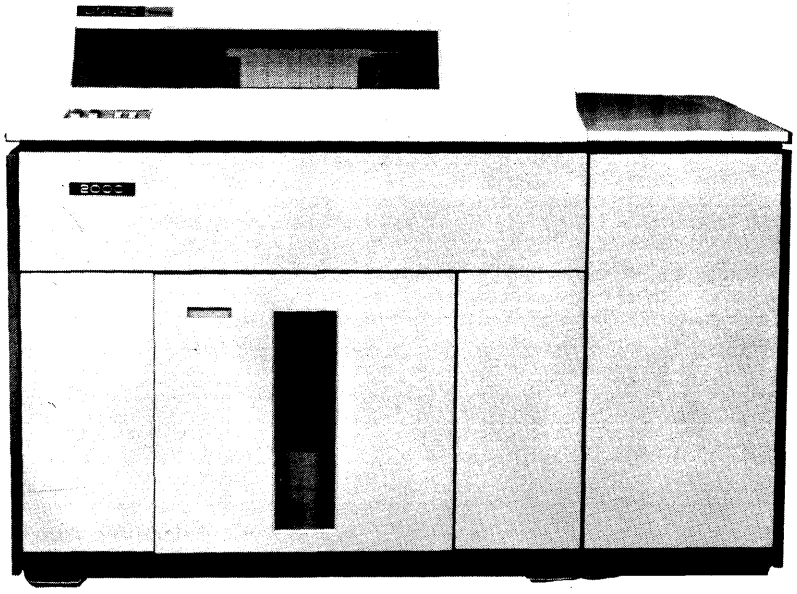
The 0716 Card Reader Subsystem includes a self-contained control unit and synchronizer that regulates flow of data and control signals to and from the reader mechanism. This control unit is attached to an MSA or to a C/SP by means of the multiplexer channel.

The 0716 Card Reader Subsystem operates at a rate of 1000 cards per minute on a column-by-column basis. The read-check feature is standard to ensure correct input. Information read from the card is transferred to the processor in either image mode or translate mode, which includes EBCDIC, ASCII, or compressed code. Image mode and selection of any one of the translate modes are standard features. The optional dual translate feature permits an additional selection from the two remaining choices offered by the translate mode. A validity check feature, checks for multiple punches in row one through seven.

Two output stackers provide the means for error selection as a standard feature in addition to the capability of stopping on error. An optional feature, alternate stacker fill, provides the capability of stacking 4000 cards: when stacker A is filled, the reader automatically begins to fill stacker B. The stop-on-error feature may be used with alternate stacker fill. The stacker carrousel wheel decelerates and stacks the cards at a rate which maximizes card handling care.

UNIVAC 0716 CARD READER SUBSYSTEM CHARACTERISTICS	
CARD READING SPEED	1000 cards per minute
INPUT HOPPER CAPACITY	2400 cards
OUTPUT STACKER CAPACITY	2 stackers — 2000 cards each
READ MODES	Image Mode: 160 6-bit characters per card Translate mode: EBCDIC — 80 characters per card ASCII — 80 characters per card Compressed code — 80 characters per card Fieldata — 80 characters per card
OPTIONAL FEATURES	Validity check Alternate stacker fill Dual translate End of file Read buffer (when used on MSA)

7.5.2. UNIVAC 0770 Printer Subsystem



The 0770 Printer Subsystem is a freestanding, self-contained unit, that interfaces with the 1100/10 Systems via an MSA, or a C/SP.

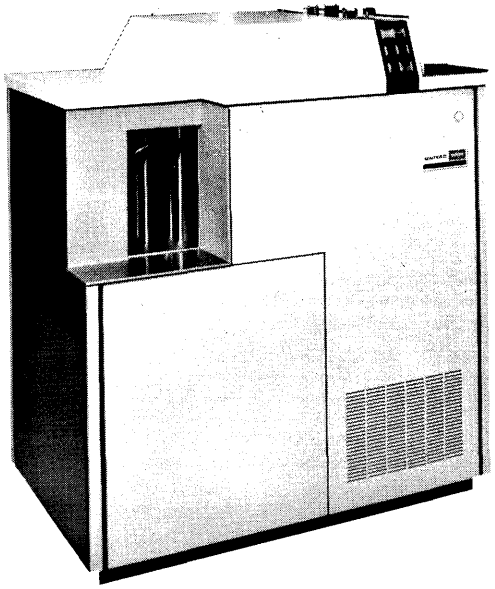
The 0770 Printer Subsystem is a family of printers that feature an easily replaceable print band cartridge. The family is comprised of three printers that print at a rate of 800, 1400, or 2000 lines per minute using a standard 48-character set. Other character sets are available, including a 24-character set used for high speed numeric applications to a 177-character set used for international applications. More than 20 standard print cartridges are available. The character set is located on a continuous metal band which travels in a horizontal direction across the front of the printed form. This printing method assures optimum print quality through close control of print registration. The metal band contains 384 characters which are usually grouped in repeating arrays. For example, a 48-character set is repeated on the band eight times.

In addition to the standard 132 print position, the subsystem can be ordered with an optional 160-print-position feature. The 160 print positions offer more opportunities for increasing throughput with the use of "two-up" and "three-up" forms.

The print cartridge case serves as the means for the operator to remove and replace the character set used on the printer in a manner similar to operations performed with magnetic disc pack covers.

UNIVAC 0770 PRINTER SUBSYSTEM CHARACTERISTICS			
	0770–00 PRINTER SUBSYSTEM	**0770–02 PRINTER SUBSYSTEM**	**0770–04 PRINTER SUBSYSTEM**
PRINTING SPEED (SINGLE-LINE SPACING)	800 lpm – 48 character set 1435 lpm – 24 character set	1400 lpm – 48 character set 2320 lpm – 24 character set	2000 lpm – 48 character set 3000 lpm – 24 character set
MAXIMUM FORMS SLEW RATE	50 inches per second	75 inches per second	100 inches per second
CHARACTERS PER PRINT CARTRIDGE	384		
PRINT POSITIONS PER LINE	132 or 160		
SINGLE LINE SPACE TIME	8.75 milliseconds		
HORIZONTAL SPACING OF CHARACTERS	10 per inch		
VERTICAL LINE SPACING	6 or 8 lines per inch under program control		
FORM WIDTH	3.5 to 22 inches		
FORM LENGTH	To 24 inches		
FORM ADVANCE CONTROL	Vertical format buffer under program control		

7.5.3. UNIVAC 0604 Card Punch Subsystem



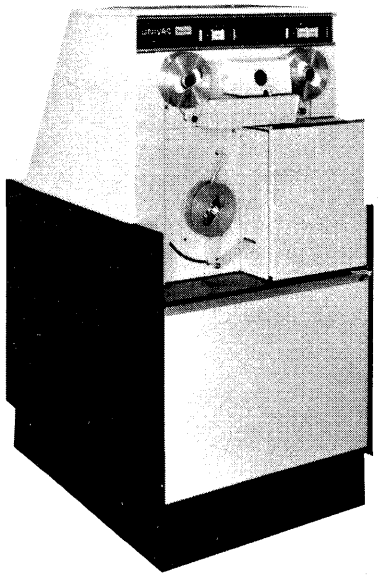
The card punch operates at a rate of 250 cards per minute on a row-by-row basis (12 punching positions per card). Standard features include processing 80-column cards in either punched card code or main storage image code modes. Output cards can be directed to either stacker under control of program.

The card punch includes a self-contained control unit and a synchronizer which regulates the flow of data and control signals to and from the punch mechanism. The control unit is connected via an MSA or a multiplexer channel of a C/SP.

An optional feature is the inclusion of the read/punch feature. The read/punch option allows prepunched cards to be sensed and read into the punch buffer from a prepunch station.

UNIVAC 0604 CARD PUNCH SUBSYSTEM CHARACTERISTICS	
CARD PUNCHING SPEED	250 cards per minute
INPUT HOPPER CAPACITY	1000 cards
OUTPUT STACKER CAPACITY	3 stackers — 1000 cards per stacker
PUNCH MODES	Image mode — 160 6-bit characters per card Translate mode — 80 characters per card
OPTIONAL FEATURE	Read before punching (not software supported)

7.5.4. UNIVAC 0920 Paper Tape Subsystem



The 0920 Paper Tape Subsystem consists of a control unit, a paper tape reader with a reader synchronizer and/or a paper tape punch with a punch synchronizer. The control unit provides the necessary synchronization and interface between the reader and/or punch synchronizer and the C/SP multiplexer channel. The synchronizer unit regulates the transfer of data between the tape reader or tape punch and the control unit. The entire subsystem is housed in a freestanding cabinet and is connected by means of one of the eight physical connections provided in the standard multiplexer I/O channel.

The control unit handles paper tape codes of five, six, seven, or eight levels. During the reading or punching of less than eight levels, all data is enclosed in the least significant bit positions of the byte, and the control unit zerofills any unused most significant bit positions. The reading and punching of binary data from paper tape is possible and is selected by program option. When reading and punching binary data, the program connector is bypassed and all eight levels of the tape character are transferred to main storage with tape channels 1 through 8 corresponding to bit positions 7 through 0, respectively. The translation of all paper tape codes to internal code is performed by the software.

Simultaneity of read and punch operations is accomplished by connecting two control units to the paper tape subsystem.

Spooling features are optional for both the tape reader and tape punch. The tape spooler hubs for the tape reader can accommodate snap-on supply and take-up reels of 5-inch diameter (300-foot capacity). The tape take-up spooler hub for the tape punch can accommodate snap-on reels of 5-inch diameter; a larger hub is used to accommodate snap-on reels of 8-inch diameter (1000-foot capacity).

UNIVAC 0920 PAPER TAPE SUBSYSTEM CHARACTERISTICS	
TAPE READING SPEED	300 characters per second (with tape punched 10 characters per inch)
TAPE PUNCHING SPEED	110 characters per second (with tape punched 10 characters per inch)
TAPE WIDTH	11/16 inch or 1 inch
PAPER TAPE CODES	5-level (11/16 inch tape) 5-, 6-, 7-, or 8-level (1 inch tape)
AVERAGE REWIND ON TAPE SPOOLER	40 inches per second

7.6. UNIVAC MULTI-SUBSYSTEM ADAPTER

The MSA enables byte-oriented peripheral devices to operate with the word oriented 1100/10 Systems input/output channels.

Mixtures of up to eight paper peripherals may be attached to the MSA.

UNISERVO 14 Magnetic Tape Subsystems and paper peripheral may be mixed on a single MSA. Mixtures of disc subsystems and paper peripherals on a single MSA are not recommended due to throughput considerations.

The basic MSA can interface one 1100/10 Systems I/O channel with up to eight peripheral control units. The MSA can be expanded by use of the SPI feature to interface with up to four 1100/10 Systems I/O channels (useful in 1100/12 Multiprocessor System configuration). A second independent MSA and all associated features can be added to the original MSA cabinet.

A function buffer expansion feature is required for operation with the SPERRY UNIVAC 8425 Disc Subsystems. This feature provides six function buffers which allows expanded command chaining capability.

Another feature required for the 8425 Disc Subsystem is the search identifier register. This feature provides storage for twelve bytes of search data.

Four translation features are available for the MSA. The Fieldata translator provides translation of Fieldata code to and from a 6-bit subset of ASCII. The EBCDIC-FD translator provides translation of Fieldata code to and from a 64-character subset of EBCDIC. Two translators may be installed in an MSA. Each translator may be connected to from one to four I/O channels, but is restricted to one type of translator per channel. The BCD code to and from EBCDIC code translator is included in the tape subsystem control unit.

7.7. UNIVAC COMMUNICATION/SYMBIONT PROCESSOR

When the C/SP is used as a symbiont processor, it controls the transfer of data between the peripheral subsystems and the 1100/10 Systems. In this application, the I/O subroutines (symbionts) are run in the C/SP thus removing this burden from the host system. This results in a saving of both time and storage in the 1100/10 Systems.

Concurrent with controlling the peripherals, the C/SP can control communications between the 1100/10 Systems and remote terminals.

8. Communications Equipment

8.1. GENERAL

There is a wide variety of methods for communicating with the SPERRY UNIVAC 1100/10 Systems. Data transfer rates can vary widely, and many communications terminals can be multiplexed to one remote terminal which has direct high speed access to the processor. The following lists typify the wide range of equipment available for data communications with a 1100/10 System.

- Onsite Communications Equipment
  - General Communications Subsystem
  - Communications/Symbiont Processor
- Remote Communications Equipment
  - Data Communications Terminal (DCT) 1000
  - Data Communications Terminal (DCT) 500
  - UNISCOPE 100 Display Terminal
  - UNISCOPE 200 Display Terminal
  - 9200/9300 System

8.2. ONSITE COMMUNICATIONS EQUIPMENT

8.2.1. SPERRY UNIVAC General Communications Subsystem

The General Communications Subsystem (GCS) enables a 1100/10 System to receive and transmit data by way of any common carrier at any of the standard rates of transmission up to 50,000 bits per second. It can receive data from or transmit data to the various speed lines in any combination consistent with system throughput.

The GCS Subsystem, as illustrated in Figure 8–1, consists of three principal elements:

1. Communications Terminal Controller (CTC)

   The CTC is a multiplexing device that provides the means for the processor to communicate over transmission facilities with a number of terminals. By switching quickly from one line to another (within 4 microseconds), the CTC can be compared to a switchboard in selecting and multiplexing data exchange between the processor and communications devices.

2. Communications Terminal (CT)

   The CT performs the communications functions; such as serializing, staticizing, character recognition, synchronization, character parity check and generation, block parity check and generation, and dialing. The CTC can accommodate from 1 to 32 CTs. Each CT contains two (one input and one output) communications circuits. All CTs require a communications interface (CI) to provide interconnection to the data sets, automatic calling units, or telegraph lines. The CT will arrange data in the format required by the processor or in the format demanded by the circuit with which the terminal is designed to operate.

3. Communications Interface (CI)

   The CI makes the necessary conversion between the electrical operating levels of the CTs and those of the communications line with which the CIs are designed to operate. The type of CIs required are dependent on the type of communications circuit or service to be used.

A GCS Subsystem may be connected to any input/output (I/O) channel for multiplexing up to 32 CT/CI pairs to that channel.

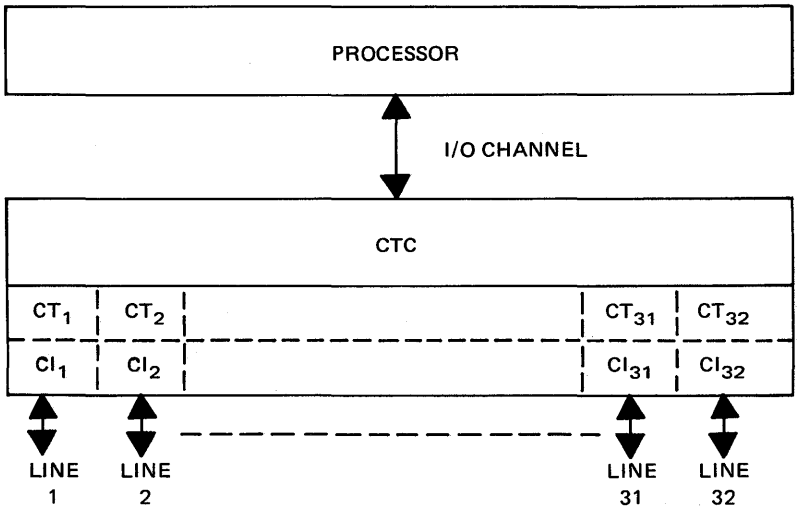


Figure 8–1. SPERRY UNIVAC GCS Subsystem

There are three basic types of CTs:

1. Synchronous
2. Asynchronous
3. Dial

There are four basic types of CIs:

1. Telegraph (dc loop)
2. Modem
3. Dial
4. High Speed (wideband)

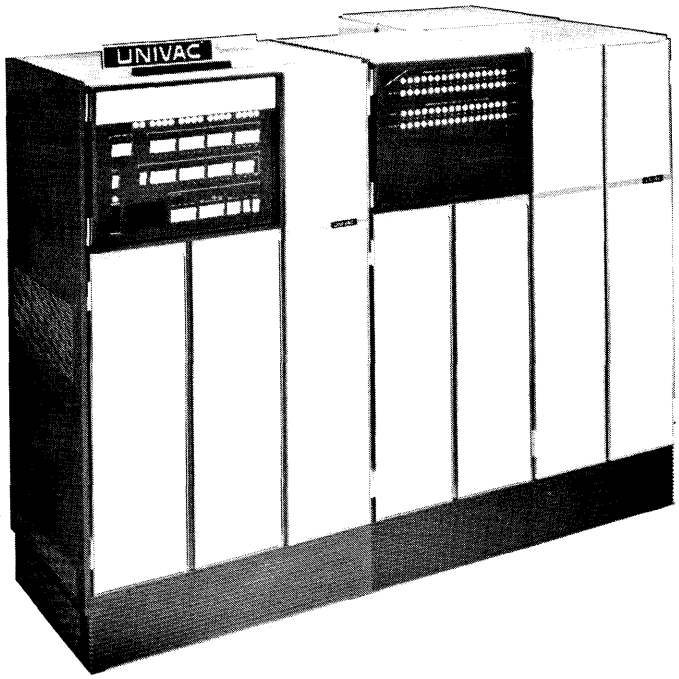
Each CT/CI combination is readily adaptable to the speed and character size of the type of line with which it is to operate. With the exception of the CT/CI Dial type, each CT/CI pair may operate in simplex, half duplex, or full duplex mode. The CT/CI enables the processor to establish communications with remote terminals through the common carrier's switching network.

Characteristics of the subsystem are summarized below.

TYPE	SPEED	MODE	LEVEL
Asynchronous	45.45 bps to 2400 bps	Asynchronous	5, 6, 7 or 8
Synchronous	Up to 50,000 bps	Synchronous	5, 6, 7 or 8
Dial	Variable	Bit Parallel	4

bps = bits per second

8.2.2. UNIVAC Communications/Symbiont Processor



The Communications/Symbiont Processor (C/SP) is a high performance, internally programmed system which is intended to absorb the function of communications control in addition to interfacing the systems paper peripherals (see 7.5). Its high speed internal operation and multipurpose I/O channels provide high throughput rates and interface with communications facilities and terminals.

In assuming control of all communications operation, the C/SP relieves the host computer of storage allocated to terminal handler programs and of time associated with communications interrupt processing, data formatting, data editing, data translation, and other communications tasks.

System throughput is increased and user turnaround time is decreased by virtue of the improved system performance offered by isolated, dedicated processor elements.

The concept of front-end processing offers efficiency by simplifying the interface between the host system and its peripheral subsystems. All communications lines appear as a common intelligent subsystem to the host. The C/SP effectively buffers the host from the infinite variety of remote terminal and communications line transmission disciplines.

The C/SP hardware was designed to be modular and flexible. A multifunction subsystem includes special emphasis on high volume throughput. Special channels accommodate, with a high degree of efficiency, the varying needs of communication terminals. The configuration (see Figure 8–2) includes the following:

- Processor Unit
  - Processor
  - 16 general purpose registers

- Maintenance panel
- Interval timer
- Special device channel
- SPERRY UNIVAC 1100 Series adapter channel

- Storage Unit
  - 32K to 131K bytes storage
  - Storage protection feature

- Optional Features
  - Expansion to 131K bytes
  - One additional 1100 Series adapter channel
  - Multiplexer channel (for the paper peripherals, if used)
  - Selector channel (tape or disc subsystems, if used)
  - One or two general purpose communications channels (GPCC)
  - Dialing adapters (uses one CLT position)
  - Asynchronous timing assemblies

The SPERRY UNIVAC 1100 Series Operating System fully supports the following peripherals connected to the C/SP multiplexer channel:

- UNIVAC 0604 Card Punch Subsystem
- UNIVAC 0716 Card Reader Subsystem
- UNIVAC 0770 Printer Subsystem
- UNIVAC 0920 Paper Tape Subsystem

The SPERRY UNIVAC 1100 Series Operating System fully supports either of the following peripherals connected to the C/SP selector channel:

- SPERRY UNIVAC 8425 Disc Subsystem
- UNISERVO 16 Magnetic Tape Subsystem

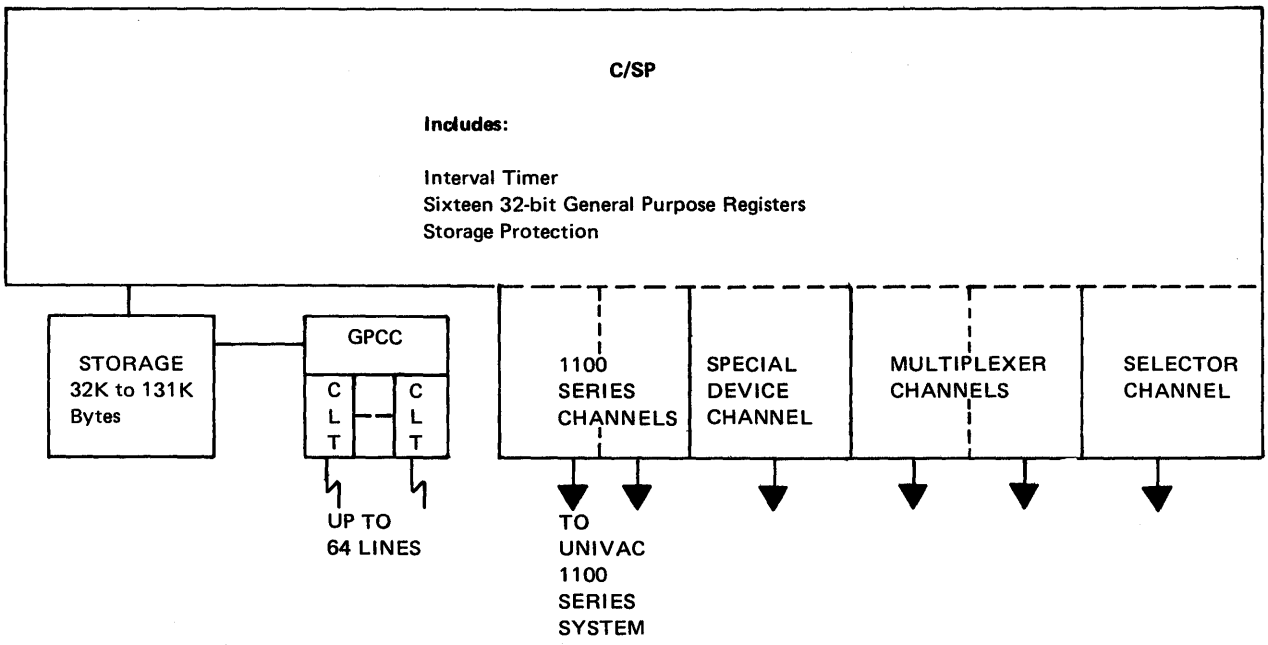


Figure 8–2. UNIVAC Communications/Symbiont Processor (C/SP) Configurator

8.2.2.1. Processor

The processor portion of the C/SP provides the flexibility that is required to control the I/O data flow and to perform message processing, as necessary, in an online peripheral or a communications environment. Major features of the processor include the following:

- 52 half-word and full-word instructions;
- sixteen 32-bit general purpose registers, external to storage;
- attached processor maintenance panel;
- I/O interrupt and data priority controls;
- variable interval timer;
- halfword basic data path;
- multilevel interrupt;
- 630-nanosecond cycle time;
- basic binary add (register to indexed storage) instruction time of 2.52 microseconds (four cycles);
- binary add instruction (register to register) time of 1.26 microseconds (two cycles);
- zero time indexed base and displacement calculation; and
- double indexing.

The control section of the processor regulates the sequence in which instructions are executed, interprets and controls the execution of each individual instruction, initiates cycling of main storage, performs required storage address modification and indexing, and determines the different processor modes of operation. All of the hardware aspects of interrupt handling, error checking, and protection are also performed by the control section.

The arithmetic section performs all data manipulations including logical and numerical arithmetic, data comparisons, and shifting. The arithmetic section also performs single or double indexing of operand addresses. Arithmetic operations are performed in the two complement form. A fixed-point arithmetic operand can be either a 32-bit fullword or a 16-bit halfword. The sign of a fixed-point operand is always the leftmost bit of the operand. When accessed from storage, a half-word fixed-point number is always expanded to a right-justified fullword; the sign is extended to the left.

Logical operations on fixed-length operands are performed in registers. Logical operations include comparing, bit setting, bit testing, and bit manipulation.

The C/SP utilizes a set of 52 basic instructions that vary in format and length. The format, in general, is dictated by the operation to be performed and the location of the operands. Operands may be located in storage, in general purpose registers, or in the instruction itself. The length of an instruction is dictated by the format and is either a halfword or a fullword. All processor instructions must be on half-word boundaries in storage. Operand addresses in storage are on byte, half-word or full-word boundaries, depending upon the instruction. For example, if an operand for a particular instruction is a fullword, the operand address in storage must be on a full-word boundary.

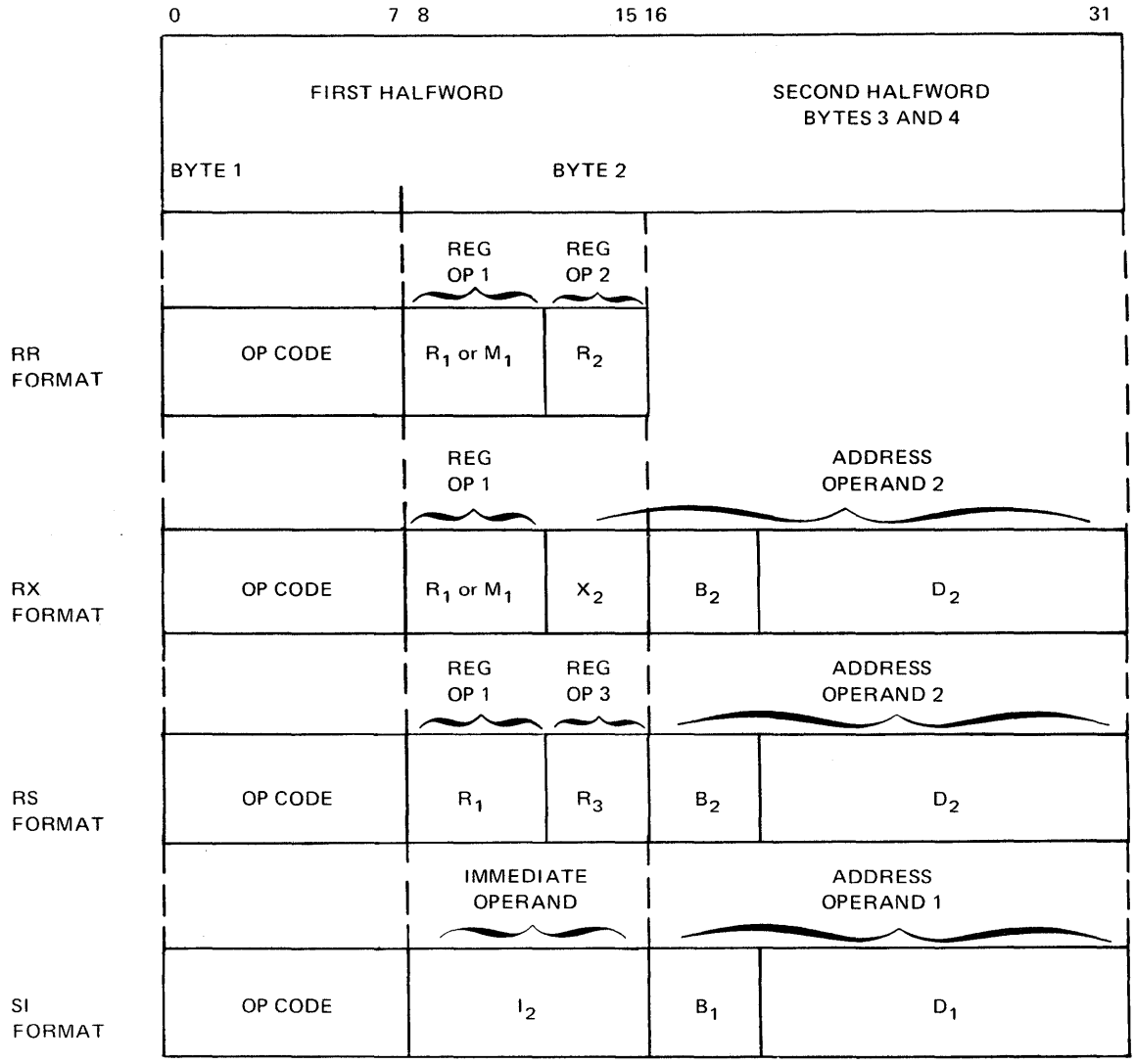
The four basic instruction formats that are used in the C/SP are illustrated in Figure 8–3 and are designated as follows:

- RR (Register to Register) Instructions
- RX (Register to Indexed Storage) Instructions
- RS (Register to Storage) Instructions
- SI (Storage and Immediate Operand) Instructions

Each format consists of an operation code (OP code) and two or more fields which specify, among other things, the addresses of operands (in storage or in the general purpose registers). Each field is identified by a letter followed by a subscript numeral. The numeral, in general, denotes the operand (1, 2, or 3) to which the field applies.

The C/SP instruction repertoire is listed in Table 8–1. The operation codes are expressed in hexadecimal (base 16); each code appears as two hexadecimal digits in the eight-bit OP code field of each instruction.

The interval timer, which utilizes a fixed-word location in storage, is a processor feature which provides interval timing and time of day information. Interval timer requests for service are made every 6 milliseconds. The interval timer provides an interrupt to the processor at a software specified interval in 6-milliseconds multiples. Interval timer requests may be serviced only at the end of a processor instruction execution prior to the processor staticizing the next instruction.



OP CODE	– Instruction operation code
R_1	– The number of the register addressed as operand 1, or a register which is the first register of a multiregister group
R_2	– The number of the register addressed as operand 2
R_3	– An expression representing a register which is the last register in a multiregister group
X_2	– The number of the register to be used as an index for operand 2 of an RX instruction
I_2	– The immediate data or device address used as operand 2 of a SI instruction
B_1	– The base register for operand 1
B_2	– The base register for operand 2
D_1	– The displacement for operand 1
D_2	– The displacement for operand 2
OP1	– Operand 1
OP2	– Operand 2
OP3	– Operand 3 (extended mnemonic repertoire)
M1	– Mask (extended mnemonic repertoire)

Figure 8–3. UNIVAC C/SP Instruction Formats

Table 8–1. Basic UNIVAC C/SP Instruction Repertoire (Part 1 of 2)

Functional Description	Mnemonic	OP Code (Hexadecimal)	Format*	Execution Time (Cycles)**
Add	A	5A	RX	4
Add Half-word	AH	4A	RX	4
Add	AR	1A	RR	2
Compare	C	59	RX	4
Compare Half-word	CH	49	RX	4
Compare	CR	19	RR	2
Divide Half-word	DH	53	RX	22
Load	L	58	RX	4
Load Half-word	LH	48	RX	4
Load	LR	18	RR	2
Multiply Half-word	MH	52	RX	20
Shift Left Single	SLA	8B	RS	3 + N1 (Note 2)
Shift Right Single	SRA	8A	RS	3 + N1 (Note 2)
Subtract	S	5B	RX	4
Subtract Half-word	SH	4B	RX	4
Subtract	SR	1B	RR	2
Store	ST	50	RX	5
Store Half-word	STH	40	RX	4
LOGICAL				
AND	N	54	RX	4
AND	NI	94	SI	5 (Note 1)
AND	NR	14	RR	2
Compare Logical	CL	55	RX	4
Compare Logical	CLI	95	SI	5 (Note 1)
Compare Logical	CLR	15	RR	2
Divide Polynomial	DP	81	RS	3 + N (Note 2)
Exclusive OR	X	57	RX	4
Exclusive OR	XI	97	SI	5 (Note 1)
Exclusive OR	XR	17	RR	2
Insert Character	IC	43	RX	3
Load Address	LA	41	RX	4
Move	MVI	92	SI	5 (Note 1)
OR	O	56	RX	4
OR	OI	96	SI	5 (Note 1)
OR	OR	16	RR	2
Shift Left Single Logical	SLL	89	RS	3 + N1 (Note 2)
Shift Right Single Logical	SRL	88	RS	3 + N1 (Note 2)
Store Character	STC	42	RX	4
Test Under Mask	TM	91	SI	5 (Note 1)

Table 8–1. Basic UNIVAC C/SP Instruction Repertoire (Part 2 of 2)

Functional Description	Mnemonic	OP Code (Hexadecimal)	Format*	Execution Time (Cycles)**
Branch and Link	BAL	45	RX	4
Branch and Link	BALR	05	RR	3
Branch on Condition	BC	47	RX	2
Branch on Condition	BCR	07	RR	1/2 NB/B
Branch on Count	BCT	46	RX	4
Branch on Count	BCTR	06	RR	2/3 NB/B
Branch on Index High	BXH	86	RS	6
Branch on Index Low or Equal	BXLE	87	RS	6
STATUS SWITCHING				
Halt and Proceed	HPR	99	SI	***3 (If No Halt)
Load PSW	LPSW	82	SI	***5 (Note 1)
Set Storage Key	SSK	08	RR	***3
Set System Mask	SSM	80	SI	***4 (Note 1)
Supervisor Call	SVC	0A	RR	8
INPUT/OUTPUT				
Start I/O	SIO	9C	SI	***6–24

*RR – Register to Register
RX – Register to Indexed Storage
RS – Register to Storage
SI – Storage and Immediate Operand

**1 storage cycle = 630 nanoseconds, all RX instructions add one cycle if double indexing

***Denotes Privileged Instruction

NOTES:

1. Number of cycles is one less if not indexing.

2. N = Number of shifts up to 16, N_1 = Number of shifts up to 31 (Module 16).

The interrupt system provides an automatic means of altering the C/SP processor to conditions arising from errors, end of I/O operations, specified time intervals, and unexpected conditions relating to abnormal system operation. The interrupt system directs the processor to the appropriate program which is responsible for interrogation and action upon the cause of the specific class of interrupt generated. The system permits the interruption of any task to process an interrupt of higher priority. Among the features of the interrupt system are:

- automatic tabling of communications channel interrupts;
- a dynamically alterable priority structure;
- automatic dispatch by interrupt class; and
- automatic program switching by interrupt class.

8.2.2.2. Storage

High performance storage is a basic part of the C/SP. Storage is located in one or two freestanding cabinets, depending upon the size of the storage capacity. Major features of main storage include the following:

- Capacity – 32,768 bytes minimum; 131,072 bytes maximum
- Cycle Time – 630-nanosecond read/write cycle
- Operating Mode – Nondestructive readout
- Storage Data Path – 18 bits wide (two eight-bit bytes and two parity bits)
- Parity – Odd parity (one parity bit per byte)
- Addressing – Zero time indexed base and displacement
  – Double indexed
- Storage Protection – Program and I/O transfer

The addressing hardware accommodates a 17-bit address field which permits one-cycle addressing of 131,072 bytes. While the address field permits the addressing of each byte, the least significant bit of the address is not used to access the data from storage.

On a read cycle, the storage presents two bytes to the processor. If the particular reference requires byte addressing, the processor selects the appropriate byte based upon the least significant bit of the address field. The capability for partial write is provided; that is, one byte may be written without altering the other byte in the storage halfword.

The parity bit associated with each byte provides odd parity for that byte. Parity generation and checking are performed in storage. The parity bits are, however, presented to the C/SP processor or an appropriate channel on a read cycle.

Indexing is accomplished by creating the operand address through the addition of the contents of the registers specified in the X_2 and B_2 portions of the instruction (see Figure 8–3) to the value contained in the displacement portion (D_2). Double indexing, (that is, use of both X_2 and B_2) requires one additional storage cycle. When single indexing, the use of X_2, rather than B_2 (B_2=0), to obtain the operand consumes no additional time. Use of the general purpose registers for indexing involves an 18-bit add; the displacement in this add is right-justified. Access to 131K of storage is therefore achieved through indexing in this manner.

In addition to the fixed storage assignment, there may be several programs resident in C/SP main storage at any one time. It becomes necessary to restrict storage accesses by a program to the storage limits assigned to it.

Associated with main storage are a maximum of 64 three-bit registers called key storage registers. The storage is divided into a maximum of 64 blocks, each of which contain 2048 bytes. To each of these blocks is assigned a key storage register. The six most significant bits of a storage address are used to define the address of the key storage register associated with the block containing the storage address.

Storage is segmented by grouping together all blocks whose associated key storage registers have the same setting. Since there are three bit positions in a key storage register, a maximum of eight storage segments can be defined.

When a program is loaded, the program is assigned a unique program number. This number is then loaded into the key storage register that is associated with each 2048-byte block assigned to the program.

Storage protection against improper storage accessing is provided for during instruction execution and I/O transfers.

- Instruction Execution Protection

  When a program is scheduled for execution, the program number is loaded into a program status word (PSW) register that is uniquely identified with the program currently in operation. On each access to storage during processing, the program number in this register is compared with the contents of the key storage register that is associated with the storage address. If a match is made, the storage access is allowed; otherwise an error interrupt occurs.

- I/O Transfer Protection

  The number of the program requesting the I/O transfer is presented to the I/O channel. Upon transfer, the contents of the key storage register that is associated with the address to which the transfer is to be made is checked against the program number associated with the I/O channel. Again, a match of the key storage register and program number permits the transfer to take place; otherwise, an error interrupt occurs.

8.2.2.3. Channels

All information transmission in and out of the C/SP is handled by channels. A channel controls the operation of I/O devices and the transfer of data between devices and storage.

Among the outstanding features of the C/SP channels are:

- direct access to storage;
- independent operation;
- simultaneous operation;
- priority interchangeability.

The C/SP may contain up to seven channels, numbered 0 to 6. Priority of these channels increases in descending channel number order, with channel 0 having the highest priority. The C/SP is equipped with the following channel types:

- Special Device Channel (SDC)

  The primary function of the SDC is to provide the means for local program loading and maintenance of the C/SP by using the optional serial 80-column, 80 cards per minute, card reader device.

- 1100 Series Adapter Channel

  The 1100 Series Adapter Channel (intercomputer adapter channel) provides an interface for direct connection of the C/SP to an I/O channel of a 1100/10 Systems Processor. The maximum transfer rate is in the excess of 300,000 words (36 bits each) per second.

- Multiplexer Channel

  The multiplexer channel provides the capability of attaching all currently available UNIVAC 9000 Series peripheral devices, which operate on this channel, to the C/SP.

- Selector Channel

  The selector channel provides the capability of attaching the SPERRY UNIVAC 8425 Disc Subsystems or the UNISERVO 16 Magnetic Tape Subsystems, which operate on this channel, to the C/SP.

- General Purpose Communications Channel (GPCC)

  The GPCC performs such functions as multiplexing the various CLTs so that one CLT may be serviced at a time, recognizing special characters and sequences of characters, checking character parity, coordinating all data transfers to and from storage, and executing other necessary operations.

  The CLTs perform the function of assembly and disassembly of data characters for proper reception from and transmission to a communication line; detection of certain conditions of the communications line such as loss of carrier, a ringing indication, and others; and establishment of character synchronization.

  The CLTs handle a wide range of communications with rates up to 50 kilobytes per second. However, the CLTs must be selected so that the total combined rate of service requests (one per byte) is no more than 50,000 per second. When the GPCC is operated at this maximum rate, somewhat less than 40 percent of all available storage cycles are utilized for this purpose.

  The GPCC is the link between storage and the CLTs and provides the data path and control for CLTs as they communicate with storage. The single data path can be time shared by as many as 64 positions, which need not have identical CLTs. A full duplex CLT uses two multiplexer positions; a half duplex or simplex CLT utilizes only one multiplexer position.

  The GPCC is equipped to analyze each data character or sequence of characters which is transmitted through the GPCC and to act upon these characters in a manner that is a program-changeable function of the line to which the GPCC is connected. The GPCC also interfaces with the C/SP processor to service Start I/O (SIO) instructions and interrupts. Associated with the GPCC is a display panel which contains two active line indicators (output and input) for each CLT. The indicator is on when the corresponding CLT data line is in a spacing condition.

  The multiplexer portion of the GPCC accepts up to 64 simultaneously presented service requests from the CLTs plus an external function (XF) request from another portion of the GPCC. The multiplexer selects one request by connecting the selected CLT to the GPCC. When all necessary information has been interchanged, the multiplexer is cleared and can immediately accept another request. The multiplexer can accommodate a maximum of 32 full-duplex CLTs or 64 half-duplex CLTs. An area in storage called a buffer control word (BCW) is associated with each position on the multiplexer and is used to store status, control information, and data address information for the particular position.

When information is to be transferred during an I/O operation, the CLT requests service from the GPCC and, when priority permits, sends the CLT address to GPCC. The GPCC uses the address to select the associated BCW which is loaded into the channel and now controls the channel operation until the information is transferred. Then the BCW, in general changed by the channel operation (for example, address incrementation), is returned to main storage and the GPCC facilities are released. The BCWs remember the current state of the various positions.

The C/SP is intended to operate in an environment which can involve many different line discipline procedures. Many such procedures have been long established and must be handler unchanged by the C/SP. To avoid a multiplicity of tailored CLTs operating through the GPCC, the BCW is permitted to access a message discipline word (MDW). A chain of MDWs can be considered as a description of a given procedure, and the currently active MDW represents the position reached by a given line within that procedure. The chain of MDWs should not be modified once it has been loaded. Hence all lines with the same line discipline procedure may share a common chain of MDWs. An MDW contains, for example, parameters which control character parity checking, special character recognition (single or multiple), special character insertion, and other operations.

At various points throughout a procedure, it is necessary to present certain information to the controlling program. Since this information is dynamically changing, it must be stored at the desired point immediately. A normal interrupt is not sufficient since the processor is not always in a condition to accept an interrupt request. Four interrupt lists are provided in storage where communication interrupt words (CIWs) are stored. These lists are controlled by CIW list controls which are in fixed storage locations. A list is selected by a BCW or MDW and is usually assigned on a priority basis.

8.2.2.4. Programmed Systems Support

The software support provided for the C/SP is designed to provide complete flexibility for handling communications configurations with all types of terminal hardware while maintaining an expedient user interface. Coding efficiency is achieved by the utilization of a powerful instruction set at the assembly level. System macros are also provided to facilitate the user's requirements.

Software to integrate the C/SP effectively with the host processor system is included in the SPERRY UNIVAC 1100 Series Operating System and is controlled by system generation parameters.

The software package is divided into the following two segments:

- C/SP Operating System

  The C/SP operating system comprises various program modules which are specified by the user at system generation. When supplied elements are used, the following are included:

  - Terminal Management Supervisor (TMS)
  - Message Control Program (MCP)
  - Terminal Management Control Routine (TMCR)
  - Communication Control Routines (CCR)

  System interface is provided for inclusion of user versions of, or additions to, any element specified under the operating system.

- Support Programs – operating under the SPERRY UNIVAC 1100 Series Operating System

The following programs operate under control of the host processor executive system and are described in the paragraphs that follow.

– C/SP Assembler

– C/SP Element Collector

– C/SP Simulator

– C/SP Service Routines

The C/SP assembler is one-phase two-pass bootstrap assembler. The assembler is an efficient, easy-to-use, processor with macro capabilities. Each machine instruction and data form has simple, convenient representations in assembly language. The assembler translates this language into a form that can be executed by the processor. The rules that govern the use of the language are uncomplicated and can be easily applied by the programmer.

The C/SP element collector provides a means of collecting independent relative binary elements to produce an absolute program for execution in the C/SP. A relative binary element is an output of the assembler, as a result of translating C/SP assembler instructions. An absolute program is a program unit with no unresolved references which can be relocated in C/SP storage as an executable program.

The C/SP simulator is a SPERRY UNIVAC 1100 Series Assembler Language user program which runs under the operating system. The simulator accepts C/SP object code, simulates execution on the C/SP processor, and provides diagnostic printout to aid in debugging the C/SP program.

The following C/SP service routines are provided on the host processor.

– Initial Load of C/SP

– Program Load of C/SP

– Logging of Data for C/SP

– Console Communications

– Sign-on

– C/SP Storage Dump

8.3. REMOTE COMMUNICATIONS EQUIPMENT

8.3.1. UNISCOPE Display Terminals

Two UNISCOPE Display Terminal types are available with the 1100/10 Systems. These display terminals are:

UNISCOPE 200 Display Terminals
UNISCOPE 100 Display Terminals

The UNISCOPE Display Terminal is a alphanumeric display designed for a broad range of applications which require direct operator interaction with a centralized processor system. Due to its modular construction, the UNISCOPE Display Terminal can operate either as a data entry or as a display device. It can be conveniently located at the central processor site or at a remote station where it is connected to the system by way of telephone lines.

The UNISCOPE Display Terminal is a self-contained unit consisting of a cathode-ray-tube display screen, refresh storage, character generator, control logic, operator keyboard, and communications interfaces. A special interface for direct processor connection is available. Also available is an auxiliary interface that is used to connect up to eight devices to the UNISCOPE Display Terminal, such as the UNIVAC Communications Output Printers or SPERRY UNIVAC Tape Cassettes. A variety of presentation formats are offered which provide a total display capacity of 480, 512, 1960, 1024, 1536, or 1920 USA Standard Code for Information Interchange (ASCII) characters. Each of these units is capable of displaying the complete ASCII set of 96 characters which include upper and lower case alphabetics. Hardware editing features enable the operator to completely edit any message prior to transmitting it to the processor.

Multiple UNISCOPE Display Terminals may be connected to a single communications line by means of a multiplexer. This general-purpose multiplexer is available with all the communications line interfaces available on the UNISCOPE Display Terminal, thus permitting a mixture of single units and multiple units on one communications system. The multiplexer also provides broadcasting of output messages to multiple devices.

The keyboard has been functionally designed to approximate the conventional electric typewriter, with its keyboard appearance, touch pressure, key travel, and slope characteristics. Typewriting speeds in excess of eighty words per minute can be accommodated by the keyboard. Because of its similarity to the standard typewriter, little additional training is required to operate it.

The keyboard includes cursor controls and editing keys, and the layout is right-left assignment balanced to efficiently distribute the work load. The keys are arranged for convenient function discrimination.

8.3.1.1. UNISCOPE 200 Display Terminal

The UNISCOPE 200 Display Terminal offers a variety of presentation formats which provide a total display capacity of 1536 or 1920 USA Standard Code for Information Interchange (ASCII) characters.

UNISCOPE 200 Display Terminals may be mixed in any combination with UNISCOPE 100 Display Terminals and UNIVAC Data Communications Terminals (DCT) 1000 on a single line.

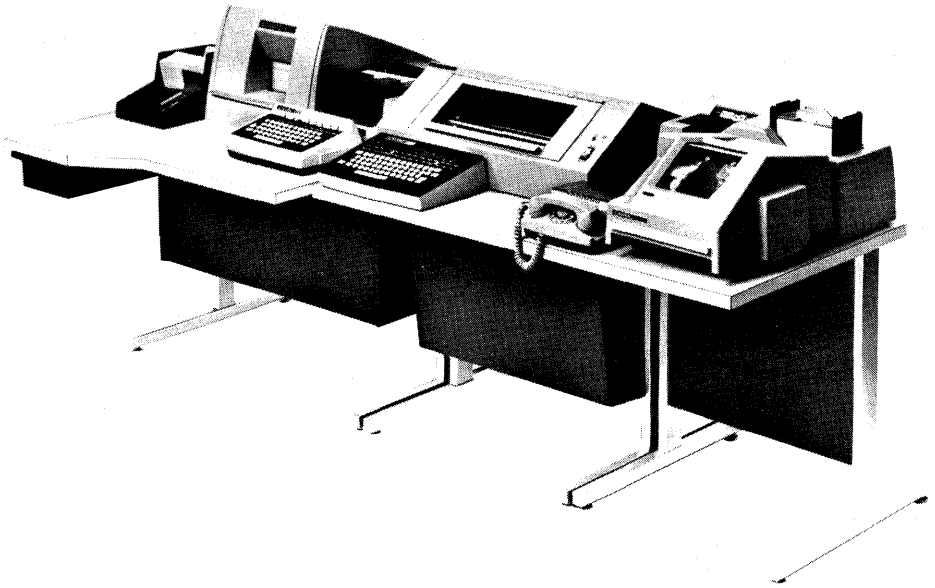
8.3.1.2. UNISCOPE 100 Display Terminal

The UNISCOPE 100 Display Terminal offers a variety of presentation formats which provide a total display capacity of 480, 512, 960, or 1024 USA Standard Code for Information Interchange (ASCII) characters.

UNISCOPE 100 Display Terminals may be mixed in any combination with UNISCOPE 200 Display Terminals and UNIVAC Data Communications Terminals (DCT) 1000 on a single line.

UNISCOPE DISPLAY TERMINALS CHARACTERISTICS		
	UNISCOPE 200 Display Terminal	**UNISCOPE 100 Display Terminal**
DISPLAY	1536 or 1920 characters (64 per line, 24 lines; 80 per line, 24 lines) on 12-inch wide and 8-inch high screen. Characters are ASCII, and also include both upper and lower case alphabetics.	480, 512, 960 or 1024 characters (80 per line, 6 lines; 32 per line, 16 lines; 80 per line, 12 lines; 64 per line, 16 lines) on 10-inch wide and 5-inch high screen. Characters are ASCII, and also include both upper and lower case alphabetics.
KEYBOARD	Alphanumeric and symbolic with 8 cursor control keys and 5 editing keys	
STORAGE	7.2 microseconds cycle time, 7-bit ASCII code plus parity bit	
DATA TRANSMISSION	Up to 9,600 bits per second Half or full duplex Party line polling Nonsignificant space suppression Block transmission Message segmentation	
POWER	Standard office receptacles	

8.3.2. UNIVAC Data Communications Terminal (DCT) 1000



The Data Communications Terminal (DCT) 1000 is a fully buffered 30 character per second incremental printer which can be expanded to include a keyboard, card reader, card punch, paper tape reader/punch, and an auxiliary printer. The DCT 1000 transmits data or receives data from a local or remote processor or to a remote DCT 1000 in conversational or batch mode.

Two 160-character buffers are standard on the DCT 1000. These buffers facilitate the following:

- Automatic Blocking

  This eliminates complicated and time comsuming operator functions and minimizes training.

- Automatic Error Correction

  This eliminates manual correction protection procedures such as reloading cards and retyping input data.

- Error Free Output

  All messages are completely checked for character errors, block errors, duplicate blocks, or lost blocks. The result is that no errors are entered into the output medium.

- High Transmission Speeds

  The full capability of the line can be utilized since the transmission rate can be much higher than the I/O rate. On party line systems, this yields data throughput on a line which is the sum of the throughputs of the individual terminals.

The DCT 1000 has complete polling and address recognition capabilities allowing the processor to completely control multiple DCT 1000s on a single line. The terminals may be connected in a series string in different geographical locations or at a single point on the UNIVAC Terminal Multiplexer.

The DCT 1000 can be tailored to complement the transmission facility which fits the application best. The following options are available:

Line Type	– Switched or private
Private Line	– Two-wire or four-wire
Mode	– Synchronous or asynchronous
Transmission Speed	– Asynchronous 300, 1200, or 1800 baud – Synchronous up to 4800 baud
Interface	– EIA RS-232 (synchronous or asynchronous) – MIL STD 188B (synchronous)
Direct Connection	– To CT or Data Communications Set without modems
I/O Channel	– Direct to processor I/O channel via terminal multiplexer.

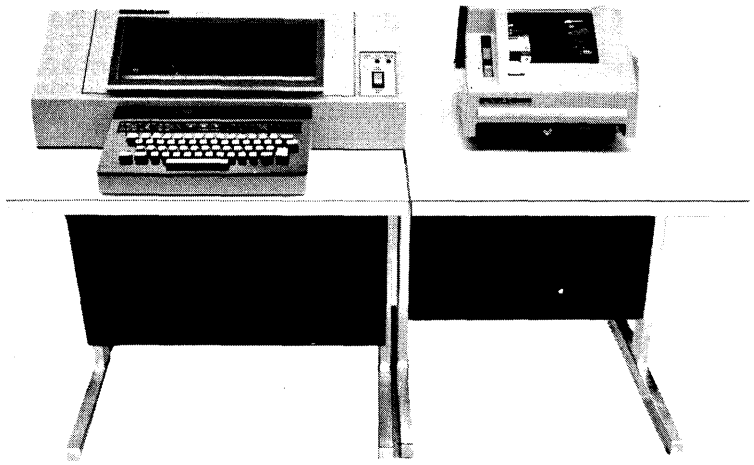
The DCT 1000 transmission control procedures are completely compatible with those for the UNISCOPE 200 and UNISCOPE 100 Display Terminals. Therefore, these terminals can be intermixed on the same transmission line or on the same multiplexer. This mix and match capability yields an almost limitless number of configurations. Control can be achieved at the central processor with a single common handler.

DCT 1000 (printer only) stations can be used to furnish hard copy for the UNISCOPE 200 and UNISCOPE 100 Display Terminals. The printing operation is not dependent on the display hardware and does not delay any operator functions at the display stations.

When the DCT 1000 is not transmitting or receiving data, it need not be idle. The DCT 1000 can be used offline to generate paper tapes, list cards, or for media conversion. Additionally, while the DCT 1000 is receiving or transmitting data online, the punch can be used offline.

UNIVAC DATA COMMUNICATIONS TERMINAL (DCT) 1000 CHARACTERISTICS	
CARD READING SPEED	40 cards per minute
CARD PUNCHING SPEED	35 cards per minute
PRINTING SPEED	30 characters per second
PRINTING POSITIONS PER LINE	132 (adjustable tractor)
PRINTABLE CHARACTERS	63 plus space
PAPER TAPE SPEEDS	50 characters per second
BUFFER STORAGE	320 character capacity in two buffers, 160 characters each
TRANSLATOR SELECTIONS	ASCII H (Scientific) code A (Business) code Binary with additional feature
TRANSMISSION METHOD	Block by block
TRANSMISSION MODE	Half duplex; 2- or 4-wire (nonsimultaneous; two-way transmission)
TRANSMISSION FACILITIES	Voice-grade telephone toll exchange, or private line
TRANSMISSION RATE	Asynchronous 300, 1200, or 1800 bits per second; Synchronous 4800 bits per second
POWER	Standard office receptacle

8.3.3. UNIVAC Data Communications Terminal (DCT) 500



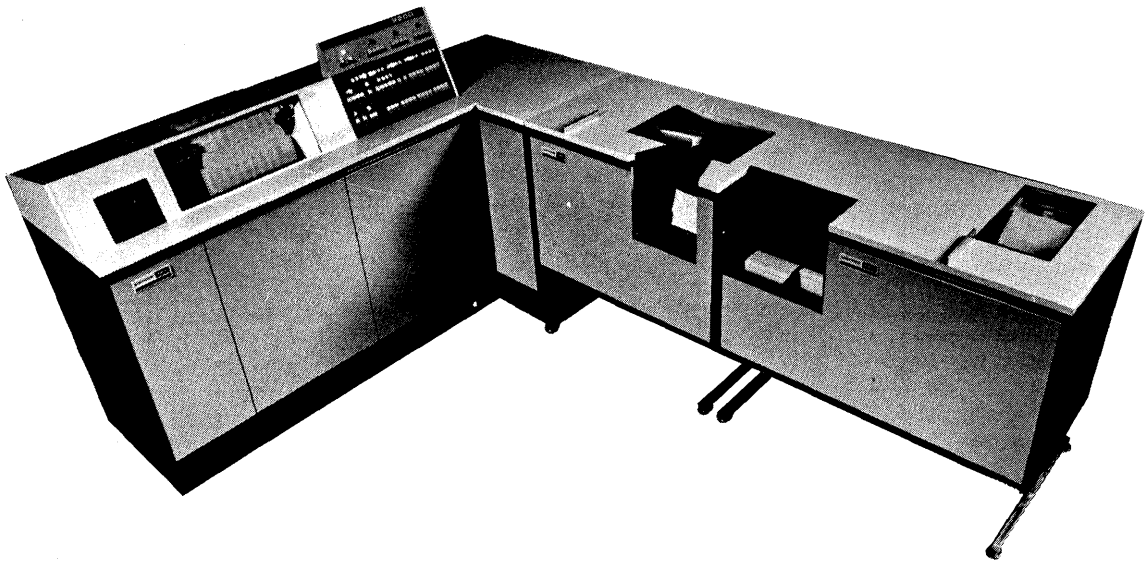
The Data Communications Terminal (DCT) 500 is an unbuffered, asynchronous keyboard/printer terminal similar in operation to a teletypewriter. The DCT 500 is, however, two to three times faster than a teletypewriter and it provides up to 132 print positions and five carbons. The DCT 500 can replace existing teletypewriters with little or no changes in the software handlers for point-to-point communications networks over voice-grade telephone toll lines or private lines. In a multiparty, polled environment, the DCT 500 operates in accordance with ASCII procedures.

The DCT 500 can operate in a receive-only mode, a keyboard send/receive mode, or an automatic send/receive mode. The basic printer system (minimum equipment) can be expanded to include a keyboard and a 1-inch paper tape read/punch unit at any time. Additional optional equipment is available to allow for multi-station operation and the following optional features.

- Automatic Answering
- Automatic Operation
- Remote Control
- Master/Slave Operation
- Print Monitor
- Internal Modem
- Paper Tape

UNIVAC DATA COMMUNICATIONS TERMINAL (DCT) 500 CHARACTERISTICS	
TRANSMISSION CODE	8-level ASCII
INTERFACES	EIA Standard RS-232/CCITT Internal Modem
TRANSMISSION MODE	Half duplex or full duplex (2- or 4-wire)
TRANSMISSION RATE	110, 150, or 300 bits per second (selectable)
PRINTING RATE	30 characters per second
FONT SELECTIONS	ASCII, EBCDIC A (Business)/G (Scientific)
PRINTABLE CHARACTERS	63 plus space
PRINT POSITIONS PER LINE	132 (adjustable tractor)
PAPER TAPE READER/PUNCH RATE	50 characters per second
POWER	Standard office receptacle

8.3.4. Remote UNIVAC 9200/9300 System



The minimum 9200/9300 System consists of a central processor unit, 8K of main storage, and a printer. All other peripherals are options and must be specially ordered.

The remote 9200/9300 System requires a UNIVAC Data Communications Subsystem (DCS) to enable it to communicate with the 1100/10 Systems.

The DCS provides communications capability for the 9000 Series Processors. Connected to a multiplexer channel, the DCS enables synchronous data transmission at speeds up to 50,000 bits per second between the 9200/9300 System and a 1100/10 System over standard communications circuits. The unit is physically small so that two of them can be mounted in space available in the 9200/9200 Processor's main frame.

The DCS is modular, permitting field modifications as demands for various options arise. As communications needs grow, different interfaces can be substituted to upgrade capabilities.

Its many features include the following:

- Automatic Error Checking

  The DCS checks character and message parity by sending either odd or even parity bits. Longitudinal redundancy can be checked by hardware or by user software.

- Self Testing

  The DCS may be tested under program control by connecting the output line to the input line to verify transmission and reception of data.

- Unattended Answering

  The subsystem responds to incoming calls from dialed lines without operator intervention.

- Variable Message Length

  A message may be of any length, from one character up to available storage size.

UNIVAC 9200/9300 SYSTEM CHARACTERISTICS				
	9200	9200 II	9300	9300 II
SYSTEM ORIENTATION*	Card/Disc	Card/Tape/Disc	Card/Tape/Disc	Card/Tape/Disc
BASIC MAIN STORAGE	8192 bytes	8192 bytes	8192 bytes	16,384 bytes
MAXIMUM MAIN STORAGE	16,384 bytes	32,768 bytes	32,768 bytes	32,768 bytes
MAIN STORAGE CYCLE TIME	1200 nanoseconds per byte	1200 nanoseconds per byte	600 nanoseconds per byte	600 nanoseconds per byte
ADD (DECIMAL) INSTRUCTION TIME (TWO 5-DIGIT NUMBERS)	104 microseconds	104 microseconds	52 microseconds	52 microseconds
MULTIPLY, DIVIDE, AND EDIT CAPABILITY	Optional	Optional	Standard	Standard
PRINT SPEED (INTEGRAL PRINTER)	250, 300, 500, or 600 lines per minute	250, 300, 500, or 600 lines per minute	600 or 1200 lines per minute	600 or 1200 lines per minute
MULTIPLEXER CHANNEL TRANSFER RATE	85,000 bytes per second	85,000 bytes per second	85,000 bytes per second	85,000 bytes per second
DATA COMMUNICATION SUBSYSTEM	Up to 8 duplex lines	Up to 8 duplex lines	Up to 8 duplex lines	Up to 8 duplex lines
REGISTERS	8 for processor functions 8 for I/O functions	8 for processor functions 8 for I/O functions	8 for processor functions 8 for I/O functions	8 for processor functions 8 for I/O functions

*Only card systems (not disc or tape) are supported by the SPERRY UNIVAC 1100 Series Executive System.

Characteristics for the DCS follow.

UNIVAC DATA COMMUNICATIONS SUBSYSTEM CHARACTERISTICS	
SPEED AND FACILITIES	Low speed line — up to 300 bits per second Dial voice lines — 2000 bits per second Private voice lines — 2400 bits per second Broad-band lines — 50,000 bits per second
DATA CODING	Five to eight levels, plus parity
CHECKING	Odd or even message and character parity Longitudinal redundancy check is optional
MULTIPLEXER CHANNELS REQUIRED	One per subsystem

The SPERRY UNIVAC 1100 Series Executive System fully supports the following UNIVAC peripherals connected to the 9200/9300 System multiplexer channel:

- 0716 Card Reader Subsystem
- 0770 Printer Subsystem
- 0920 Paper Tape Subsystem

Also software supported are the following card subsystems which are connected directly to the 9200/9300 System:

- 0603 Card Punch Subsystem
- 0711 Card Reader Subsystem

Appendix A. Abbreviations and Symbols

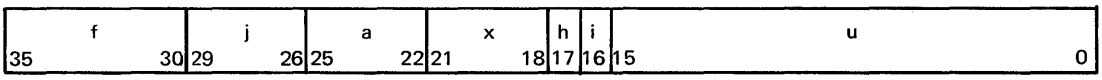
Abbreviations and symbols frequently used in the description of the SPERRY UNIVAC 1100/10 Systems instructions are given below:

( )	Contents of a register or a main storage location
( )'	Complement of the contents of a register or of a main storage location
|( )|	Absolute value (or magnitude) of the contents of a register or location
$( )_{17-0}$	Subscripts indicating the bit position or positions involved. A full word usually is not subscripted. (Subscripts also are used to designate binary, octal, or decimal notation.)
AND	Logical AND (logical product)
OR	Inclusive OR (logical sum)
XOR	Exclusive OR (logical difference)
→	Indicates replacement of the current value of the operand to the right of the symbol with the value of the operand on the left
A	Arithmetic register (accumulator)
a	Arithmetic register designator of an instruction word. (In input/output instructions, "a" is used in specifying an I/O channel.)
BI	Instruction bank base register
BS	BI/BD selection register
BD	Data bank base register
CSR	Channel select register
ESI	Externally specified index
f	Function designator of an instruction word
h	Index register incrementation designator of an instruction word. (A value of 1 specifies incrementation.)

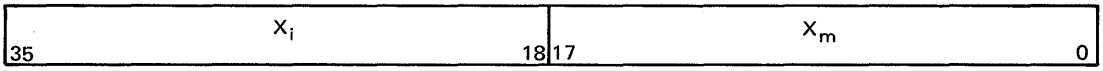
IACR	Input access control register
ISI	Internally specified index
i	Indirect address designator of an instruction word. (A value of 1 specified indirect addressing.)
j	Partial word designator or minor function designator of an instruction word
K	Represents the repeat count of R1
MSR	Memory select register
NI	Next (sequential) instruction
OACR	Output access control register
P	Program address register
PSR	Processor state register
R	R register (special register)
R_a	R register specified by the a-field of an instruction word
SLR	Storage limits register
U	The address or value of the operand after application of indexing and indirect addressing
u	The address or operand designator of an instruction word
X	Index register
X_a	Index register specified by the a-field of an instruction word
x	Index register designator of an instruction word

Appendix B. Summary of Word Formats

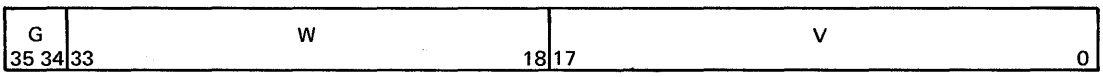
INSTRUCTION WORD



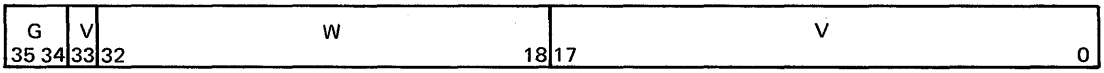
INDEX REGISTER WORD



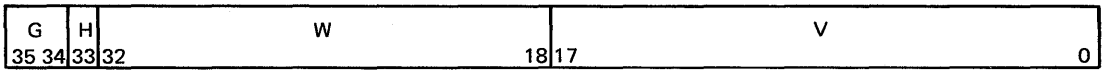
ISI ACCESS CONTROL WORD — 262K ADDRESSING



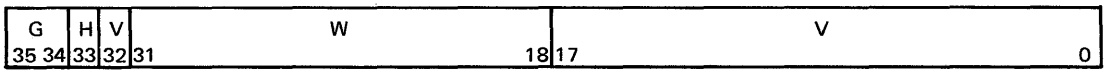
ISI ACCESS CONTROL WORD — 524K ADDRESSING



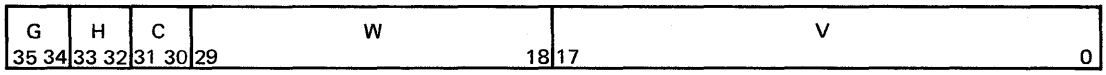
ESI ACCESS CONTROL WORD (HALF WORD) — 262K ADDRESSING



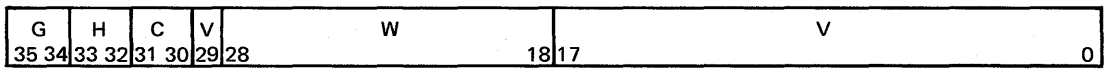
ESI ACCESS CONTROL WORD (HALF WORD) — 524K ADDRESSING



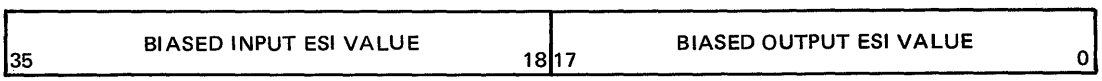
ESI ACCESS CONTROL WORD (QUARTER WORD) — 262K ADDRESSING



ESI ACCESS CONTROL WORD (QUARTER WORD) — 524K ADDRESSING



BIASED ESI VALUES IN IACR'S



SINGLE-PRECISION FIXED-POINT WORD

DOUBLE-PRECISION FIXED-POINT WORD

A

A+1

FIXED-POINT INTEGER MULTIPLY RESULT

A

A+1

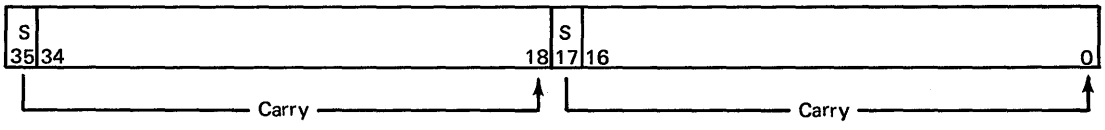
FIXED-POINT MULTIPLY SINGLE INTEGER RESULT

FIXED-POINT FRACTIONAL MULTIPLY RESULT

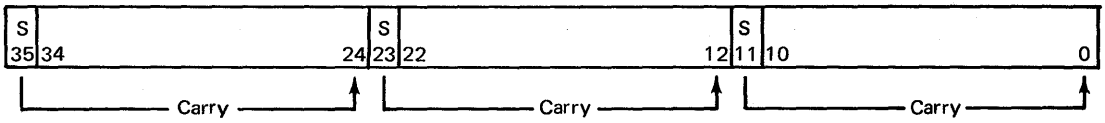
A

A+1

ADD HALVES WORD FORMAT



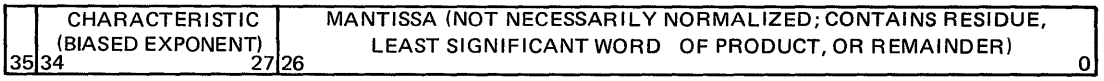
ADD THIRDS WORD FORMAT



SINGLE-PRECISION FLOATING-POINT OPERAND

SINGLE-PRECISION FLOATING-POINT RESULT

A



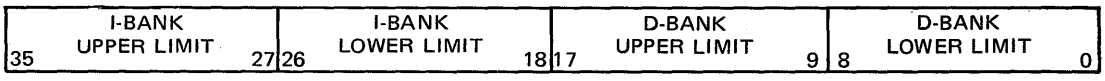
A+1

DOUBLE-PRECISION FLOATING-POINT OPERAND OR RESULT

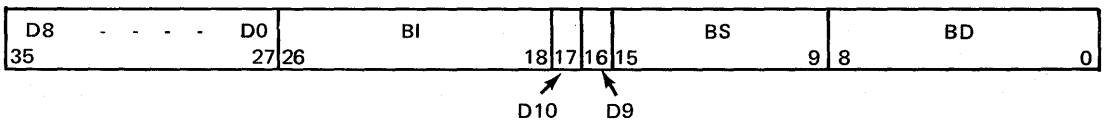
A

A+1

STORAGE LIMITS WORD



PROCESSOR STATE WORD



Appendix C. Instruction Repertoire by Function Code

Function Code (Octal)		Mnemonic	Instruction	Description[2]	Execution Time[1] in μsec.	
f	j				Storage With Overlap	Storage Without Overlap
00	–	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	–	–
01	0–15	S,SA	Store A	(A) → U	1.125	2.025
02	0–15	SN,SNA	Store Negative A	(A) → $\overline{U}$	1.125	2.025
03	0–15	SM,SMA	Store Magnitude A	|(A)| → U	1.125	2.025
04	0–15	S,SR	Store R	(R_a) → U	1.125	2.025
05	0–15	S,SZ	Store Zero	ZEROS → U	1.125	2.025
06	0–15	S,SX	Store X	(X_a) → U	1.125	2.025
07	0–11	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	–	–
07	12	LDJ*	Load D Bank Base and Jump	Transfer the portions of the BDW specified by the BDP plus the BDI specified by (Xa) to PSR, SLR; P + 1 → Xa modifier; jump to address U (on new PSR, SLR); P + 1 → Xa modifier	–	–
07	13	LIJ*	Load I Bank Base and Jump	Transfer the portions of the BDW specified by the BDP plus the BDI specified by (Xa) to PSR, SLR; P + 1 → Xa modifier; jump to address U (on new PSR, SLR); P + 1 → Xa modifier	–	–
07	14	LPD	Load PSR Designators	$(U)_{3-1}$ → PSR; U_1, U_2, U_3 → D5, D8, D10	1.125	1.125
07	15	SPD	Store PSR Designators	PSR D-bits → U_{3-1}; D5, D8, D10 → U_1, U_2, U_3	1.125	2.025
07	16–17	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	–	–
10	0–17	L,LA	Load A	(U) → A	1.125	2.25
11	0–17	LN,LNA	Load Negative A	–(U) → A	1.125	2.25
12	0–17	LM,LMA	Load Magnitude A	|(U)| → A	1.125	2.25
13	0–17	LNM,LNMA	Load Negative Magnitude A	–|(U)| → A	1.125	2.25
14	0–17	A,AA	Add to A	(A) + (U) → A	1.125	2.25

*Simulated in software by the Executive system

Function Code (Octal)		Mnemonic	Instruction	Description [2]	Execution Time[1] in μsec.	
f	j				Storage With Overlap	Storage Without Overlap
15	0–17	AN,ANA	Add Negative To A	(A)−(U) → A	1.125	2.25
16	0–17	AM,AMA	Add Magnitude To A	(A)+|(U)| → A	1.125	2.25
17	0–17	ANM,ANMA	Add Negative Magnitude To A	(A)−|(U)| → A	1.125	2.25
20	0–17	AU	Add Upper	(A)+(U) → A+1	1.125	2.25
21	0–17	ANU	Add Negative Upper	(A)−(U) → A+1	1.125	2.25
22	0–15	BT	Block Transfer	$(X_x+u) \rightarrow X_a+u$, repeat K times	2.625+2.025K	2.625+2.025K
23	0–17	L,LR	Load R	$(U) \rightarrow R_a$	1.125	2.25
24	0–17	A,AX	Add To X	$(X_a)+(U) \rightarrow X_a$	1.125	2.25
25	0–17	AN,ANX	Add Negative To X	$(X_a)-(U) \rightarrow X_a$	1.125	2.25
26	0–17	LXM	Load X Modifier	$(U) \rightarrow X_{a_{17-0}}$; $X_{a_{35-18}}$ unchanged	1.25	2.375
27	0–17	L,LX	Load X	$(U) \rightarrow X_a$	1.125	2.25
30	0–17	MI	Multiply Integer	(A)·(U) → A,A+1	2.75	3.875
31	0–17	MSI	Multiply Single Integer	(A)·(U) → A	2.75	3.875
32	0–17	MF	Multiply Fractional	(A)·(U) → A,A+1	2.75	3.875
33	–	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	–	–
34	0–17	DI	Divide Integer	(A,A+1)÷(U)→A; REMAINDER → A+1	10.5	11.625
35	0–17	DSF	Divide Single Fractional	(A)÷(U) → A+1	10.5	11.625
36	0–17	DF	Divide Fractional	(A,A+1)÷(U) → A; REMAINDER → A+1	10.5	11.625
37	–	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	–	–
40	0–17	OR	Logical OR	(A) OR (U) → A+1	1.125	2.25
41	0–17	XOR	Logical Exclusive OR	(A) XOR (U) → A+1	1.125	2.25
42	0–17	AND	Logical AND	(A) AND (U) → A+1	1.125	2.25
43	0–17	MLU	Masked Load Upper	[(U) AND (R2)] OR [(A) AND (R2)′] → A+1	1.125	2.25
44	0–17	TEP	Test Even Parity	Skip NI if (U) AND (A) has even parity	2.75/1.625	4.25/3.125
45	0–17	TOP	Test Odd Parity	Skip NI if (U) AND (A) has odd parity	2.75/1.625	4.25/3.125
46	0–17	LXI	Load X Increment	$(U) \rightarrow X_{a_{35-18}}$; $X_{a_{17-0}}$ unchanged	1.375	2.5
47	0–17	TLEM	Test Less Than or Equal to Modifier	Skip NI if $(U)_{17-0} \leqslant (X_a)_{17-0}$; always $(X_a)_{17-0}+(X_a)_{35-18} \rightarrow (X_a)_{17-0}$	2.5/1.375	3.625/2.5
		TNGM	Test Not Greater Than Modifier			

Function Code (Octal)		Mnemonic	Instruction	Description [2]	Execution Time[1] in μsec.	
f	j				Storage With Overlap	Storage Without Overlap
50	0–17	TZ	Test Zero	Skip NI if (U) = ±0	2.375/1.25	3.5/2.375
51	0–17	TNZ	Test Nonzero	Skip NI if (U) ≠ ±0	2.375/1.25	3.5/2.375
52	0–17	TE	Test Equal	Skip NI if (U) = (A)	2.375/1.25	3.5/2.375
53	0–17	TNE	Test Not Equal	SKIP NI if (U) ≠ (A)	2.375/1.25	3.5/2.375
54	0–17	TLE TNG	Test Less Than or Equal Test Not Greater	Skip NI if (U) ⩽ (A)	2.375/1.25	3.5/2.375
55	0–17	TG	Test Greater	Skip NI if (U) > (A)	2.375/1.25	3.5/2.375
56	0–17	TW	Test Within Range	Skip NI if (A)<(U)⩽(A+1)	2.5/1.375	3.265/2.5
57	0–17	TNW	Test Not Within Range	Skip NI if (U)⩽(A) or (U)>(A+1)	2.5/1.375	3.625/2.5
60	0–17	TP	Test Positive	Skip NI if $(U)_{35} = 0$	2.25/1.125	3.375/2.25
61	0–17	TN	Test Negative	Skip NI if $(U)_{35} = 1$	2.25/1.125	3.375/2.25
62	0–17	SE	Search Equal	Skip NI if (U) = (A), else repeat	2.625+1.125K	2.625+1.125K
63	0–17	SNE	Search Not Equal	Skip NI if (U)≠(A), else repeat	2.625+1.125K	2.625+1.125K
64	0–17	SLE SNG	Search Less Than or Equal Search Not Greater	Skip NI if (U)⩽(A), else repeat	2.625+1.125K	2.625+1.125K
65	0–17	SG	Search Greater	Skip NI if (U)>(A), else repeat	2.625+1.125K	2.625+1.125K
66	0–17	SW	Search Within Range	Skip NI if (A)<(U)⩽(A+1), else repeat	2.625+1.125K	2.625+1.125K
67	0–17	SNW	Search Not Within Range	Skip NI if (U)⩽(A) or (U)>(A+1), else repeat	2.625+1.125K	2.625+1.125K
70	3	JGD	Jump Greater and Decrement	Jump to U if $(\text{Control Register})_{ja} > 0$; go to NI if $(\text{Control Register})_{ja} \leqslant 0$; always $(\text{Control Register})_{ja} - 1 \rightarrow \text{Control Register}_{ja}$	2.25/1.125	2.25/1.125
71	00	MSE	Mask Search Equal	Skip NI if (U) AND (R2) = (A) AND (R2), else repeat	2.625+1.125K	2.625+1.125K
71	01	MSNE	Mask Search Not Equal	Skip NI if (U) AND (R2) ≠ (A) AND (R2), else repeat	2.625+1.125K	2.625+1.125K
71	02	MSLE MSNG	Mask Search Less Than or Equal Mask Search Not Greater	Skip NI if (U) AND (R2) ⩽ (A) AND (R2), else repeat	2.625+1.125K	2.625+1.125K
71	03	MSG	Mask Search Greater	Skip NI if (U) AND (R2) > (A) AND (R2), else repeat	2.625+1.125K	2.625+1.125K
71	04	MSW	Masked Search Within Range	Skip NI if (A) AND (R2) < (U) AND (R2) ⩽ (A+1) AND (R2), else repeat	2.625+1.125K	2.625+1.125K
71	05	MSNW	Masked Search Not Within Range	Skip NI if (U) AND (R2) ⩽ (A) AND (R2) or (U) AND (R2) > (A+1) AND (R2), else repeat	2.625+1.125K	2.625+1.125K
71	06	MASL	Masked Alphanumeric Search Less Than or Equal	Skip NI if (U) AND (R2) ⩽ (A) AND (R2), else repeat	2.625+1.125K	2.625+1.125K

Function Code (Octal)		Mnemonic	Instruction	Description [2]	Execution Time[1] in μsec.	
f	j				Storage With Overlap	Storage Without Overlap
71	07	MASG	Masked Alphanumeric Search Greater	Skip NI if (U) AND (R2) > (A) AND (R2), else repeat	2.625+1.125K	2.625+1.125K
71	10	DA	Double Precision Fixed Point Add	(A,A+1) + (U,U+1) → A,A+1	2.375	3.5
71	11	DAN	Double Precision Fixed Point Add Negative	(A,A+1) − (U,U+1) → A,A+1	2.375	3.5
71	12	DS	Double Store A	(A,A+1) → U,U+1	2.025	2.925
71	13	DL	Double Load A	(U,U+1) → A,A+1	2.25	3.375
71	14	DLN	Double Load Negative A	−(U,U+1) → A,A+1)	2.25	3.375
71	15	DLM	Double Load Magnitude A	|(U,U+1)| → A,A+1	2.25	3.375
71	16	DJZ	Double Precision Zero Jump	Jump to U if (A,A+1) = ±0; go to NI if (A,A+1) ≠ ±0	2.375/1.25	2.375/1.25
71	17	DTE	Double Precision Test Equal	Skip NI if (U,U+1) = (A,A+1)	3.5/2.375	4.625/3.5
72	00	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	–	–
72	01	SLJ	Store Location and Jump	(P)−Base Address Modifier[BI or BD] → U_{17-0}; jump to U+1	2.875	2.875
72	02	JPS	Jump Positive and Shift	Jump to U if $(A)_{35}$=0; go to NI if $(A)_{35}$=1; always shift (A) left circularly one bit position	2.25/1.125	2.25/1.125
72	03	JNS	Jump Negative and Shift	Jump to U if $(A)_{35}$=1; go to NI if $(A)_{35}$=0; always shift (A) left circularly one bit position	2.25/1.125	2.25/1.125
72	04	AH	Add Halves	$(A)_{35-18}+(U)_{35-18} \rightarrow A_{35-18}$; $(A)_{17-0}+(U)_{17-0} \rightarrow A_{17-0}$	1.125	2.25
72	05	ANH	Add Negative Halves	$(A)_{35-18}-(U)_{35-18} \rightarrow A_{35-18}$; $(A)_{17-0}-(U)_{17-0} \rightarrow A_{17-0}$	1.125	2.25
72	06	AT	Add Thirds	$(A)_{35-24}+(U)_{35-24} \rightarrow A_{35-24}$; $(A)_{23-12}+(U)_{23-12} \rightarrow A_{23-12}$; $(A)_{11-0}+(U)_{11-0} \rightarrow A_{11-0}$	1.125	2.25
72	07	ANT	Add Negative Thirds	$(A)_{35-24}-(U)_{35-24} \rightarrow A_{35-24}$; $(A)_{23-12}-(U)_{23-12} \rightarrow A_{23-12}$; $(A)_{11-0}-(U)_{11-0} \rightarrow A_{11-0}$	1.125	2.25
72	10	EX	Execute	Execute the instruction at U	1.125	1.125
72	11	ER	Executive Return	Causes executive return interrupt to address 242_8	1.75	1.75
72	12	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	–	–
72	13	PAIJ	Prevent All I/O Interrupts and Jump	Prevent all I/O interrupts and jump to U	1.125	1.125
72	14	SCN	Store Channel Number	If a=0, CHANNEL NUMBER→U_{3-0}, If a=1, CHANNEL NUMBER→U_{3-0}, CPU NUMBER → U_4	1.125	2.025

Function Code (Octal)		Mnemonic	Instruction	Description [2]	Execution Time[1] in μsec.	
f	j				Storage With Overlap	Storage Without Overlap
72	15	LPS	Load Processor State Register	(U) → PSR	1.125	2.25
72	16	LSL	Load Storage Limits Register	(U) → SLR	1.125	2.25
72	17	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	–	–
73	00	SSC	Single Shift Circular	Shift (A) right circularly U places	1.125	1.125
73	01	DSC	Double Shift Circular	Shift (A,A+1) right circularly U places	1.25	1.25
73	02	SSL	Single Shift Logical	Shift (A) right U places; zerofill	1.125	1.125
73	03	DSL	Double Shift Logical	Shift (A,A+1) right U places; zerofill	1.25	1.25
73	04	SSA	Single Shift Algebraic	Shift (A) right U places; signfill	1.125	1.125
73	05	DSA	Double Shift Algebraic	Shift (A,A+1) right U places; signfill	1.25	1.25
73	06	LSC	Load Shift and Count	(U)→A; shift (A) left circularly until $(A)_{35} \neq (A)_{34}$, NUMBER OF SHIFTS → A+1	1.5	2.625
73	07	DLSC	Double Load Shift and Count	(U,U+1)→A,A+1; Shift (A,A+1) left circularly until $(A,A+1)_{71} \neq (A,A+1)_{70}$; NUMBER OF SHIFTS → A+2	2.875	4.0
73	10	LSSC	Left Single Shift Circular	Shift (A) left circularly U places	1.125	1.125
73	11	LDSC	Left Double Shift Circular	Shift (A,A+1) left circularly U places	1.25	1.25
73	12	LSSL	Left Single Shift Logical	Shift (A) left U places; zerofill	1.125	1.125
73	13	LDSL	Left Double Shift Logical	Shift (A,A+1) left U places; zerofill	1.25	1.25
73	14	III (a=0)	Initiate Interprocessor Interrupt	Initiate interprocessor Interrupt	1.125	1.125
		NOP ($a=10_8$)	No Operation	Proceed to next instruction, or causes guard mode interrupt to 243_8 if guard mode set	1.125	1.125
		EDC ($a=11_8$)	Enable Day Clock	Enable day clock	1.125	1.125
		DDC ($a=12_8$)	Disable Day Clock	Disable day clock	1.125	1.125
73	15	SIL	Select Interrupt Location	$(a\text{-field})_{2-0}$ → MSR	1.125	1.125
73	16	LCR (a=0)	Load Channel Select Register	$(U)_{3-0}$ → CSR	1.25	2.375
		LLA (a=1)	Load Last Address Register	$(U)_{2-0}$ → LAR	1.25	2.375
73	17	TS	Test and Set	If $(U)_{30}=1$, interrupt to address 244_8; if $(U)_{30}=0$, go to NI; always $01_8 \rightarrow U_{35-30}$; U_{29-0} unchanged	2.375/1.25	2.375/2.375

Function Code (Octal)		Mnemonic	Instruction	Description [2]	Execution Time[1] in μsec.	
f	j				Storage With Overlap	Storage Without Overlap
74	00	JZ	Jump Zero	Jump to U if (A) = +0; go to NI if (A) ≠ ±0	2.25/1.125	2.25/1.125
74	01	JNZ	Jump Nonzero	Jump to U if (A) ≠ +0; go to NI if (A) = ±0	2.25/1.125	2.25/1.125
74	02	JP	Jump Positive	Jump to U if $(A)_{35}$=0; go to NI if $(A)_{35}$ = 1	2.25/1.125	2.25/1.125
74	03	JN	Jump Negative	Jump to U if $(A)_{35}$=1; go to NI if $(A)_{35}$ = 0	2.25/1.125	2.25/1.125
74	04	JK J	Jump Keys Jump	Jump to U if a = 0 or if a = lit SELECT JUMPS indicator; go to NI if neither is true	1.125	1.125
74	05	HKJ HJ	Halt Keys and Jump Halt Jump	Stop if a = 0 or if [a AND lit SELECT STOPS indicators] ≠ 0; on restart or continuation, jump to U	1.125	1.125
74	06	NOP	No Operation	Proceed to next instruction	1.125	1.125
74	07	AAIJ	Allow All I/O Interrupts and Jump	Allow all I/O interrupts and jump to U	1.125	1.125
74	10	JNB	Jump No Low Bit	Jump to U if $(A)_0$ = 0; go to NI if $(A)_0$ = 1	2.25/1.125	2.25/1.125
74	11	JB	Jump Low Bit	Jump to U if $(A)_0$ = 1; go to NI if $(A)_0$ = 0	2.25/1.125	2.25/1.125
74	12	JMGI	Jump Modifier Greater and Increment	Jump to U if $(X_a)_{17-0}>0$; go to NI if $(X_a)_{17-0}\leq 0$, always $(X_a)_{17-0}+(X_a)_{35-18}\rightarrow X_{a_{17-0}}$	2.25/1.125	2.25/1.125
74	13	LMJ	Load Modifier and Jump	(P) – Base Address Modifier [BI or BD] → $X_{a_{17-0}}$; jump to U	1.25	1.25
74	14	JO	Jump Overflow	Jump to U if D1 of PSR = 1; go to NI if D1 = 0	2.25/1.125	2.25/1.125
74	15	JNO	Jump No Overflow	Jump to U if D1 of PSR = 0; go to NI if D1 = 1	2.25/1.125	2.25/1.125
74	16	JC	Jump Carry	Jump to U if D0 of PSR = 1; go to NI if D0 = 0	2.25/1.125	2.25/1.125
74	17	JNC	Jump No Carry	Jump to U if D0 of PSR = 0; go to NI if D0 = 1	2.25/1.125	2.25/1.125
75	00	LIC	Load Input Channel	For channel [a OR CSR]: (U) → IACR; set input active; clear input monitor	1.125	2.25
75	01	LICM	Load Input Channel and Monitor	For channel [a OR CSR]: (U) → IACR; set input active; set input monitor	1.125	2.25
75	02	JIC	Jump Input Channel Busy	Jump to U if input active is set for channel [a OR CSR]; go to NI if input active is clear	1.125	2.25
75	03	DIC	Disconnect Input Channel	For channel [a OR CSR]: clear input active; clear input monitor	1.125	2.25

Function Code (Octal)		Mnemonic	Instruction	Description [2]	Execution Time[1] in μsec.	
f	j				Storage With Overlap	Storage Without Overlap
75	04	LOC	Load Output Channel	For channel [a OR CSR]: (U) → OACR; set output active; clear output monitor; clear external function (ISI only)	1.125	2.25
75	05	LOCM	Load Output Channel and Monitor	For channel [a OR CSR]: (U) → OACR; set output monitor; clear external function (ISI only)	1.125	2.25
75	06	JOC	Jump Output Channel Busy	Jump to U if output active is set for channel [a OR CSR]; go to NI if output active is clear	1.125	1.125
75	07	DOC	Disconnect Output Channel	For channel [a OR CSR]: clear output active; clear output monitor; clear external function	1.125	1.125
75	10	LFC	Load Function in Channel	For channel [a OR CSR]: (U) → OACR; set output active (ISI only), external function, and force external function; clear output monitor (ISI only)	1.125	2.25
75	11	LFCM	Load Function in Channel and Monitor	For channel [a OR CSR]: (U) → OACR; set output active (ISI only), external function, force external function, and output monitor (ISI only)	1.125	2.25
75	12	JFC	Jump Function in Channel	Jump to U if force external function is set for channel [a OR CSR]; go to NI if force external function is clear	1.125	1.125
75	13	–	Invalid Code	If guard mode is set, causes guard mode interrupt to address 243_8. If guard mode is not set, same as NOP	1.125	1.125
75	14	AACI	Allow All Channel External Interrupts	Allow all external interrupts	1.125	1.125
75	15	PACI	Prevent All Channel External Interrupts	Prevent all external interrupts	1.125	1.125
75	16	–	Invalid Code	If guard mode is set, causes guard mode interrupt to address 243_8. If guard mode is not set, same as NOP	–	–
75	17	–	Invalid Code		–	–
76	00	FA	Floating Add	(A) + (U) → A; RESIDUE → A + 1	2.25	3.375
76	01	FAN	Floating Add Negative	(A) – (U) → A; RESIDUE → A + 1	2.25	3.375
76	02	FM	Floating Multiply	(A) · (U) → A, A + 1	3.0	4.125
76	03	FD	Floating Divide	(A)÷(U)→A; REMAINDER→A + 1	8.625[4]	9.750[4]
76	04	LUF	Load and Unpack Floating	$\|(U)\|_{34-27} \rightarrow A_{7-0}$, zerofill; $(U)_{26-0} \rightarrow A + 1_{26-0}$, signfill	1.125	2.25

Function Code (Octal)		Mnemonic	Instruction	Description [2]	Execution Time[1] in μsec.	
f	j				Storage With Overlap	Storage Without Overlap
76	05	LCF	Load and Convert To Floating	$(U)_{35} \rightarrow A+1_{35}$; [NORMALIZED $(U)]_{26-0} \rightarrow A+1_{26-0}$; if $(U)_{35}=0$, $(A)_{7-0} \pm$ NORMALIZING COUNT $\rightarrow A + 1_{34-27}$; if $(U)_{35} = 1$, ones complement of $[(A)_{7-0} \pm$ NORMALIZING COUNT$] \rightarrow A+1_{34-27}$	1.5	2.625
76	06	MCDU	Magnitude of Characteristic Difference To Upper	$\|(A)\|_{35-27} - \|(U)\|_{35-27} \rightarrow A+1_{8-0}$; ZEROS $\rightarrow A + 1_{35-9}$	1.125	2.25
76	07	CDU	Characteristic Difference To Upper	$\|(A)\|_{35-27} - \|(U)\|_{35-27} \rightarrow A+1_{8-0}$; SIGN BITS $\rightarrow A + 1_{35-9}$	1.125	2.25
76	10	DFA	Double Precision Floating Add	$(A,A+1) + (U,U+1) \rightarrow A, A + 1$	3.375	4.5
76	11	DFAN	Double Precision Floating Add Negative	$(A,A+1) - (U,U+1) \rightarrow A, A + 1$	3.375	4.5
76	12	DFM	Double Precision Floating Multiply	$(A,A+1) \cdot (U,U+1) \rightarrow A, A + 1$	5.0	6.125
76	13	DFD	Double Precision Floating Divide	$(A,A+1) \div (U,U+1) \rightarrow A, A + 1$	18.0[5]	19.125[5]
76	14	DFU	Double Load and Unpack Floating	$\|(U)\|_{34-24} \rightarrow A_{10-0}$, zerofill; $(U)_{23-0} \rightarrow A + 1_{23-0}$, signfill; $(U+1) \rightarrow A + 2$	2.25	3.375
76	15	DFP	Double Load and Convert to Floating	$(U)_{35} \rightarrow A+1_{35}$; [NORMALIZED $(U, U+1)]_{59-0} \rightarrow A+1_{23-0}$ and $A + 2$. If $(U)_{35}=0$, $(A)_{10-0} \pm$ NORMALIZING COUNT $\rightarrow A+1_{34-24}$. If $(U)_{35}=1$, ones complement of $[(A)_{10-0} \pm$ NORMALIZING COUNT$] \rightarrow A+1_{34-24}$	2.875	4.0
76	16	FEL	Floating Expand and Load	If $(U)_{35}=0$, $(U)_{35-27}+1600_8 \rightarrow A_{35-24}$; if $(U)_{35}=1$, $(U)_{35-27} - 1600_8 \rightarrow A_{35-24}$; $(U)_{26-3} \rightarrow A_{23-0}$; $(U)_{2-0} \rightarrow A+1_{35-33}$; $(U)_{35} \rightarrow A+1_{32-0}$	1.375	2.5
76	17	FCL	Floating Compress and Load	If $(U)_{35}=0$, $(U)_{35-24} - 1600_8 \rightarrow A_{35-27}$; if $(U)_{35}=1$, $(U)_{35-24} + 1600_8 \rightarrow A_{35-27}$; $(U)_{23-0} \rightarrow A_{26-3}$; $(U+1)_{35-33} \rightarrow A_{2-0}$	2.375	3.5
77	0–17	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	–	–

NOTES:

1 Execution times given are calculated for a CPU clock cycle time of 125 nanoseconds.

"Overlap" implies that the current operand and the next instruction lie in different storage units and allows the CPU to retrieve both simultaneously.

For all comparison instructions, the first number represents the skip or jump condition, the second number is for a no-skip or no-jump condition.

The execution time for a Block Transfer or any of the search instructions depends on the number of repetitions (K) required; that is, the number of words in the block being transferred or the number of words searched before a find is made.

For f = 10–21, 23–32, 34–36, and 40–61, and if j = 16 or 17, then, U instead of (U) is used. No operand fetch is made to storage, and the execution time is as shown in the word overlap column.

2 NI stands for next instruction.

3 The a- and j-fields together serve to specify any of the 128 control registers when f = 70.

4 If 28 rather than 27 subtractions are performed, add 0.25 microseconds.

5 If 61 rather than 60 subtractions are performed, add 0.25 microseconds.