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FINAL TEST REPORT

ILLIAC IV COMPUTER SYSTEM

ACCEPTANCE TEST

Contract No. AF 30(602)-4144

BURROUGHS CORPORATION
Defense, Space and Special Systems Group

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FOREWARD

The procedure and requirements for this acceptance test, along with a description of the equipment under test and the software used in the test are delineated in the Acceptance Test Procedure for ILLIAC IV Computer System dated 15 November 1972.

The purpose of this report is to present the results of that test with any variances from the original test plan and some general conclusion.

1. OVERVIEW

1.1 General

The Acceptance Test for the ILLIAC IV computer system was begun 0800 hours, 27 November 1972, and was terminated 1202 hours, 8 December 1972. The Acceptance Test procedure for the ILLIAC IV computer system, Burroughs Document No. IL4-TP14/15 Rev. A, dated 15 November 1972, was used as a basis for conducting the test.

1.2 Requirements

The test procedure required:

(1) that the array subsystem shall have a minimum clock rate of 15.0 MHz, and

(2) that the system (excluding the B6700) shall demonstrate an availability of at least 70% for a 75-hour operating period.

1.3 Results

Table I summarizes the individual results for each day as well as the cumulative availability and test hours. After the third day, the system showed an increase in availability reaching a peak of 95.2% on the final day. A total of 103.3 hours of accountable operating time (either uptime or downtime) was achieved over the test period. The 4th through 11th day of testings resulted in 80.7 hours of operating time and an average accumulated availability of 82.6%. A copy of the System Event Log for the total test period is attached to this report as Appendix A. The clock frequency measurements are presented in Section 6. These results verify that the system operated at an average clock frequency of 15.75 MHz and at no time was operating at or below 15.0 MHz. These results exceed both

the minimum requirement of 70% availability for 75 hours and the minimum clock rate of 15.0 MHz. and are submitted herein as evidence of compliance with these objectives.

DATE	DAY	UPTIME UT(min)	TOTAL UPTIME Σ UT (min)	DOWNTIME DT (min)	OPERATING TIME OT (min) (UT+DT)	TOTAL OT (min)	DAILY AVAILABILITY (A%)	CUMULATIVE AVAILABILITY (A% CUM)	CUMULATIVE TIME(Hours)
11/27	1	348	348	241	589	589	59.1%	59.1	9.8
11/28	2	157.5	505.5	295.5	453	1042	34.7	38.9	17.4
11/29	3	111	616.5	206	317	1359	35.0	38.0	22.6
11/30	4	321	937.5	170	491	1850	65.4	45.3	30.8
12/1	5	502	1439.5	203	705	2555	71.2	44.6	42.6
12/2	6	628	2067.5	115	743	3298	84.5	59.6	54.9
12/4	7	582	2649.5	80	662	3960	87.9	64.4	66.0
12/5	8	569	3218.5	70	639	4599	89.0	67.8	76.7
12/6	9	592	3810.5	103	695	5294	85.2	70.1	88.2
12/7	10	549	4359.5	86	635	5929	86.5	71.8	98.8
12/8	11	256	4615.5	13	269	6198	95.2	72.8	103.3
11/30 to 12/8	4-11		3999	SUMMARY OF LAST 80.7 HOURS		4839		82.6	80.7

1.4 CONCLUSIONS

An examination of the test results permits the following general conclusion:

During a simulated operating situation, the ILLIAC IV hardware exhibited an MTBF* from "hard" permanent type failures of 3.1 hours and an MTTR** for these hard failures of .5 hours. Using this data as a base, an availability of 86% can be calculated. The difference between this figure and the 82% figure reported above lies primarily in the addition of down time penalties resulting from transient errors.

* MTBF - Mean Time Between Failures, determined by dividing a given period of up time by the number of failures occurring in this time.

** MTTR - Mean Time To Repair, determined by dividing a given amount of down time by the corresponding number of failures that caused that down time.

2. SUMMARY OF SYSTEM MALFUNCTIONS

Table II is a summary of system malfunctions occurring during the operating test period and contributing to the system down time. This summary encompasses the period of 30 November through completion of the test on 8 December 1972. It lists by date the event and failure tag of each malfunction, the test(s) failed, the corrective action and the resulting down time.

Table III (CAUSES OF FAILURES) lists by failure tag number any subsequent repair action and the probable cause of the failure. Of the 14 failures listed, there are 4 resulting from failed integrated circuits*; 1 from a failed transistor, 1 from a faulty delay line, 1 from clock adjustment, 3 relating to connections (one of which was a human error) and 4 for which no apparent cause could be identified. Except for the unidentified failures, the causes approximate what was expected.

*For the integrated circuits this would indicate a failure rate of .2 per million hours during the 80-hour operating period. Just prior to beginning the test, the integrated circuit failure rate for the system was, on a weekly basis, ranging between .1 to .4 failures per million hours.

TABLE II - SUMMARY OF SYSTEM MALFUNCTIONS

Date	Daily Event Log Item No.	Failure Tag No.	Where Failure Occurred	Symptom(s) Test Failed	Corrective Action (Cause of Failure)	System Down Time (Min.)	Comments
11/30/72	105		PU 74 & 36	IDIAP	**	1 (T)	(T) = Transient malfunction; not isolated. Downtime based on a penalty.
	106		PU 7, 69 & 25	PE-PEM		9 (T)	
	112		PU 35_8,41_8,44_8	IDIAP		2 (T)	
	118		DISK	IDIAP		1 (T)	
	136	42416	PU S/N 72	AIDS NORM	Rpl S/N 72 w/64	125 (H)	(H) = Hard failure. Down Time includes isolation and repair of malfunction.
	137	42418	PU MEM	OPAL-MEM PROB	Rpl S/N 47 w/60	29 (H)	
	143-144		DISK	IDIAP	Recycle Sub Test	3 (T)	
12/1/72	161	42421	PU S/N 59	IDIAP	Rpl S/N 59 w/74	86 (H)	
	167		DISK System	I/O PATH	One Disk Sys. Off-line	12 (H)	25% Penalties Included for one DISK System being down.
	168		DISK System	I/O Path	One Disk Sys. Off-line	1 (H)	
	*110		DISK System	CU ROM	One Disk Sys. Off-line	3 (T)	
	113		DISK System	IDIAP	One Disk Sys. Off-line	1 (T)	
	115		DISK/CU	IDIAP	Intermittent Delay Line	6 (H)	
	117-123	42422	DISK	PE-PEM	On DISK System	63 (H)	
	130	42428	PU MEM	I/O PATH	Rpl S/N 47 w/37	10 (H)	
	147		PUC 3	PE-PEM	Reseat PUC IRM Card	2 (H)	
	152	42430	PUC 3 PU/#60	IDIAP	Rpl S/N 60 w/36	17 (H)	
	153		DISK	IDIAP		2 (T)	

* Error in sequence numbering of events, 169 was followed by 110.

** When no positive action is indicated, the recycle of test indicated proper functioning of the hardware in question.

TABLE II SUMMARY OF SYSTEM MALFUNCTIONS (

Date	Daily Event Log Item No.	Failure Tag No.	Where Failure Occurred	Symptom(s) Test Failed	Corrective Action (Cause of Failure)	System Down Time (Min.)	Comments
12/2/72	171		PU S/N 25	IDIAP (HIIDR)	Rpl RC504 Card	1 (T)	
	174		PU S/N 25	IDIAP (HIIDR)	Rpl DVR03 Card	105 (H)	Debugged on Pu Extenders by card swapping.
	-		S/N 24	IDIAP (HIIDR)			
	203		PU 57_8	IDIAP (HAPE)		1 (T)	
	210		PU S/N 8	PE-PEM (DVN)		2 (T)	
	-		PU S/N 59	PE-PEM (MUTPC)			
	216		PU S/N 24	PE-PEM (1 error)		1 (T)	
	222		CU	CU-ROM		5 (T)	
12/4/72	231	42977	CU/PU S/N 32	IDIAP	Rpl S/N 32 w/30	56 (H)	Prime power loss. B6700, I/O & Quad down. Came up w/B6700 MEM,CU,PU,S/N 32, & I/O problems.
	233	42978	DISK Controller	IDIAP	Rpl Transistor	4 (H)	Possibly a result of power loss.
	247		PU S/N 74	IDIAP		1 (T)	
	249		PU S/N 74	PE-PEM	Declared Spare	0 (T)	
	-		PU S/N 62	PE-PEM(ADEX)		1 (T)	
	254		PU (23_8)	IDIAP		1 (T)	
	264		PU S/N 74	PE-PEM (NORM)		1 (T)	
	266		PU S/N 62	PE-PEM(ADEX)		2 (T)	
	268		PU S/N 71	PE-PEM(ILE IME)		2 (T)	
	278		PU S/N 62	PE-PEM (ADEX)	Declared Spare	0	
	-		PU S/N 74	PE-PEM(NORM etc)	Declared Spare	0	
	-		PU S/N 8	PE-PEM(RAB,SAB)		2 (T)	
	298		PU S/N 59	PE-PEM(MLTPL)			
	-		PU S/N 60	PE-PEM(ADEX)		5 (T)	
	-		PU S/N 71	PE-PEM(ILE IME)			

TABLE II SUMMARY OF SYSTEM MALFUNCTIONS (Continued)

Date	Daily Event Log Item No.	Failure Tag No.	Where Failure Occurred	Symptom(s) Test Failed	Corrective Action (Cause of Failure)	System Down Time (Min.)	Comments
12/4/72 (Cont'd)	302		PU S/N 60	PE-PEM (ADEX)		2 (T)	
	308		PU S/N 71	PE-PEM (IME)		2 (T)	
	318		PU S/N 59	IDIAP (HAPE)		1 (T)	
12/5/72	331		ROM (CU)	IDIAP(HACPM)		3 (T)	
	332		PU S/N 59	IDIAP (HAPE)		3 (T)	
	-		S/N 20	IDIAP (HAPE)			
	339		PU S/N 59	PE-PEM(MULTPL)		1 (T)	
	343		PU S/N 47	PE-PEM(MEM 1&2)	Recycle Sub Tests (H)	4 (H)	Problem cleared up under recycle, see event 347.
	-		S/N 59	PE-PEM(MULTPL)		1 (T)	
	347	42988	PU S/N 47	PE-PEM(MEM 1&2)	Rpl S/N 47 w/71 (H)	26 (H)	PU S/N 47 tested in PEMX
	357	42986	PU S/N 71	PE-PEM(ILE, IME, etc)	Rpl during PM period	No DT	Designated as spare per ground rules.
			S/N 24	PE-PEM(MULTPL)		1 (T)	
			S/N 59	PE-PEM(MULTPL)			
	370	-	-	-	-	23	No spare PU's.Could not come up after PM. (DT=23)
	377		PU S/N 71	PE-PEM(ILE IME)	-	1 (T)	Designated Spare.
	379		SU 03	IDIAP (HIIDR)	Parity Error Recycle Sub Test	1 (T)	
	383		PU S/N 71	PE-PEM(ILE IME)	-		Designated Spare.
			S/N 59	PE-PEM(MULTPL)		4 (T)	
		42999	S/N 25	PE-PEM(MULTPL)			
	290		PU S/N 59	PE-PEM(MULTPL)		2 (T)	

TABLE II SUMMARY OF SYSTEM MALFUNCTIONS (continued)

Date	Daily Event Log Item No.	Failure Tag No.	Where Failure Occurred	Symptom(s) Test Failed	Corrective Action (Cause of Failure)	System Down Time (Min.)	Comments
12/6/72	299	*	PU S/N 17	IDIAP (HAPE)	Rpl PU 17 w/71 (H)	63 (H)	
	-	42998	PU S/N 40	IDIAP (HAPE)	Rpl card RSG13 (H)		
	309		Unknown	IDIAP (HACPM)		3 (T)	
	313		PU S/N 71	PE-PEM (ILE,IME)	Recycle Sub Tests (H)	5 (H)	Declared Spare.
	-		PU S/N 55	PE-PEM (SHABR)		0 (T)	Less than 30 sec. on initial run.
	320		CU	CU-ROM		1 (T)	
	321		CU	CU-ROM		1 (T)	
	350		PU S/N 71	PE-PEM (ILM,IME)			Declared Spare.
	-		S/N 60	PE-PEM(MULT 8)		4 (T)	
	-		S/N 24	PE-PEM (ADEX)			
	352		Unknown	IDIAP (MEMORY)		3 (T)	
	371		PU S/N 10	PE-PEM (MANY)	Recycle Sub Tests (H)	19 (H)	No errors found on recycl of tests.
	-		PU S/N 71	PE-PEM (IB)		2 (T)	
	373		PU S/N 10 (PUC)	PE-PEM (MANY)	Reseat PUC/PE Paddle Board (H)	3 (H)	
	381		PU (14_8)	IDIAP (HAPE)		1 (T)	

* See event 393 Failure Tag 42281 below.

TABLE II SUMMARY OF SYSTEM MALFUNCTIONS

Date	Daily Event Log Item No.	Failure Tag No.	Where Failure Occurred	Symptom(s) Test Failed	Corrective Action (Cause of Failure)	System Down Time (Min.)	Comments
12/7/72	389	42279	PUC 6	IDIAP (HACPM)	Clean & swap cub logic boards in PUC 6 (H)	9 (H)	
	390		PU S/N 8	IDIAP (HAPE)	Rpl S/N 8 w/S/N 22	12 (H)	While debugging S/N 8, S/N 22 went bad.
	391		PU S/N 22	IDIAP (HAPE)	Rpl card in PU	13 (H)	
	393	42281	PU S/N 17	IDIAP (HAPE)	Rpl I.C.	0	Occurred during other repair (391 above)
	402		PU S/N 59	PE-PEM(MULTPL)			
	-		S/N 75	PE-PEM(NAND)			
	-		S/N 52	PE-PEM(NAND)			
	-		S/N 63	PE-PEM(NAND)			
	-		S/N 12	PE-PEM(NAND)			
	-		S/N 43	PE-PEM(NAND)		0 (T)	No transient penalty required. Single non-repeated error; probable CU bug.
	-		S/N 41	PE-PEM(NAND)			
	-		S/N 50	PE-PEM(NAND)			
	-		S/N 25	PE-PEM(NAND)		3 (T)	
	-		S/N 65	PE-PEM(MULTPL)			
	407		Apparent Software	(HACIA)		2 (T)	
	408		PU S/N 59	PE-PEM(MULTPL)		1 (T)	
	410		PU S/N 59	PE-PEM(MULTPL)		3 (T)	3 Recycles of Sub Test.
	414		CU	(HACIA)	Design Fix on CU Board (H)	3 (H)	
	426		PU S/N 55	IDIAP(HAPE)		3 (T)	
	430		PU S/N 55	IDIAP(HAPE)		1 (T)	Recycle 4 times. Passed 3 times.
	431		PU S/N 55	IDIAP(HAPE)		8 (T)	Recycle 4 times. Passed 3 times.
	432		PU S/N 55	IDIAP(HAPE)		1 (T)	Recycle 4 times. Passed 3 times.
	436		PU S/N 59	PE-PEM(MULTPL)	No Recycle--only 1 error. LEADER PU FAILS NAND--Recycled tests.	2 (T)	

Date	Daily Event Log Item No.	Failure Tag No.	Where Failure Occurred	Symptom(s) Test Failed	Corrective Action (Cause of Failure)	System Down Time (Min.)	Comments
12/7/72	*440		Unknown	IDIAP(HICQ)	Recycle failed.	2 (T)	
	*443		Unknown	IDIAP(HAPE)	Possible software pblm. Recycle HIIDR.	3 (T)	
	+444		SU 02	IDIAP(HICQ HAPE)	Took Su 02 off line passed HICQ, fails result descriptor. Cleared I/O-reran OK.	5 (H)	
	+420		PU S/N 72	IDIAP (ROUTE)	Rpl S/N 72 w/SN 24	15 (H)	Technician interpreted printout improperly. Called in another tech. who solved pblm in 15 min
	429		I/O	IDIAP(HACIA)	Recycle Sub Test 4 times - Intermittent between I/O & Quad.	9 (T)	
	440		PU S/N 41	PE-PEM(MULTPL)	Designated Spare	1 (T)	

* Printout did not provide enough data to determine the problem area.

+ Log sequence error--revised sequence numbers over again, went from 444 to 415.

TABLE III

CAUSES OF FAILURES

FAILURE TAG	FAILURE	ACTION	CAUSE
42416	PU S/N 72 failed Ames Norm Test	Debug in Quad. Failure disappeared	Unknown
42418	PU S/N 47 failed Memory Test	Test on PEMX 1.5 hrs. Did not reoccur	Unknown
42421	No response to IDIAP	Debug in Quad. Plug in connectors	PE to MLU Paddle boards not connected
42422	PE-PEM TEST	Trace failure in Quad. Adjust delay line.	Intermittent delay line
42428	PU S/N 47 failed MEM test	Test on PEMX and PEX. No failure isolated	Unknown
42430	PUC 3, PU S/N 60 Failed IDIAP	Debug in Quad.	Adjusted clocks
42977	PU S/N 32 failed IDIAP	Test on PEX. Replaced I.C.	Internal short in Integrated Circuit
42978	Unable to load queuer after power fault due to bad clocks	Trace failure in Disk Controller	Failed transistor
42988	PU S/N 47 failed AIDS MEM test	Test on PEMX Clean and tighten connection	Poor contact on voltage bus
42986	PU S/N 71 failed AIDS test	Test on PEX O.K. on test	Unknown
42999	PU S/N 25 failed MULT8 test	Test on PEX Replace I.C.	Internal short in Integrated Circuit

TABLE III (Cont'd)

FAILURE TAG	FAILURE	ACTION	CAUSE
42998	PU S/N 40 failed route	Test on PEX Replaced Card	Internal short in Integrated Circuit
42279	PUC 6 failed IDIAP test	Debug on-line Clean and swap logic boards	Apparently poor contacts
42281	PU S/N 17 failed OPAL test MFIND	Test on PEX Replaced I.C.	Failed Integrated Circuit. (one pin stuck low)

3. AVAILABILITY CALCULATION

In accordance with the acceptance test procedure, system availability is determined by the following rule:

> "Availability (A) is defined as uptime (Tu) divided by the sum of uptime (Tu) and downtime (Td)"

$$A = \frac{Tu}{Tu+Td}$$

The test requirement was for an availability of 70% or better for a minimum of 75 hours of system operating time (uptime plus downtime).

The period selected for the availability calculation was from 30 November to 8 December, encompassing 66 hours and 39 minutes of uptime, and 14 hours of downtime, with a total operating time of 80 hours and 39 minutes.

Therefore: $$A = \frac{66\ hr.39min.}{66hr.\ 39min.+14hr.} = 82.6\%$$

4. MTBF AND MTTR FOR SYSTEMS COMPONENTS

Table IV lists by system components, the number of "hard" failures, the corresponding downtime, and the resulting MTBF and MTTR. In several cases, no fault was isolated and the resulting MTTR includes the time spent in attempting to isolate the non-recurring fault.

In addition to the "hard" failures, there were 53 cases in which more than one test error occurred but was not repeated on subsequent tests. These failures were considered to be "transient" failures. An additional downtime of 1 hour and 21 minutes was added as a penalty for these failures as specified in the Acceptance Test procedure for ILLIAC IV Computer System, Burroughs Document No. IL4-TP14/15 Rev. A dated 15 November 1972.

TABLE IV

MTBF and MTTR for System Components

COMPONENT	FAILURES	DOWNTIME	MTBF	MTTR
Processing Units	15	420 min	4.9 hrs	.47 hrs
Control Unit	2	9 min	40.2 hrs	.08 hrs
Control Unit Power Supplies	0	0	--	--
Processing Unit Cabinets				
Logic	3	27 min	26.8 hrs	.15 hrs
Power Supplies	0	0	--	--
Cables & Connections	1	2 min	80.6 hrs	.03 hrs
I/O Subsystem	1	9 min	80.6 hrs	.15 hrs
Parallel Disk System				
Disks	1	5 min	80.6 hrs	.08 hrs
Disk File Controller	1	4 min	80.6 hrs	.07 hrs
Electronic Unit	1	63 min	79.7 hrs	1.05 hrs

5. SUMMARY OF B6700 MALFUNCTIONS

Approximately 2 hours of non-productive time during the acceptance test was charged against the B6700. Table V lists the B6700 malfunctions that occurred during the test.

TABLE V

LIST OF MALFUNCTIONS AND RESULTING NON-PRODUCTIVE TIME

Date	Event	Non-Productive Time
11-27-72	1. One B6700 Memory Off-line	---
	2. Memory Parity Error	2 min.
11-28-72	1. B6700 Down; recovered O.K. No halt load required.	3 min.
	2. B6700 Down; halt loaded 4 times between 2230 to 2330	20 min.
11-29-72	1. B6700 Memory; CM 1/N down	7 min.
	2. B6700 Down; memory parity error	15 min.
11-30-72	1. B6700 Down with directory damage causing delay in starting test	33 min.
12-2-72	1. Memory parity error	5 min.
12-4-72	1. Prime power drop caused B6700 to go down. Lost memory during transient Quadrant power off also.	---
	2. B6700 halt load	4 min.
12-5-72	1. B6700 halt load	15 min.
	2. B6700 halt load	9 min.
12-6-72	1. B6700 halt load	3 min.
	2. B6700 halt load	4 min.
12-8-72	1. B6700 halt load Lost part of test.	14 min.
	2. B6700 halt load	3 min.

6. QUADRANT CLOCK FREQUENCY

The Quadrant clock frequency was measured daily prior to the beginning of the test period. The measurement was accomplished using a Tektronic Model 454 oscilloscope.

The scope was calibrated against a Tektronix constant amplitude signal generator type 190A, with an accuracy of 2 percent. The scope measurements were within .8 percent of the generator setting, hence the accuracy of the daily clock period measurement is approximately ± 2.8 percent (both equipments used were within their current calibration periods).

The daily measurements (recorded on the daily check list) were as follows:

Date	Clock Period	Frequency (MHz)
11-27	63.5 n sec	15.75 ± .44
11-28	63.5	15.75 ± .44
11-29	63.8	15.67 ± .44
11-30	63.8	15.67 ± .44
12-1	63.0	15.87 ± .44
12-2	63.0	15.87 ± .44
12-4	63.5	15.75 ± .44
12-5	63.5	15.75 ± .44
12-6	63.5	15.75 ± .44
12-7	63.5	15.75 ± .44
12-8	63.5	15.75 ± .44

The above data substantiates that the Quadrant clock operated at frequency greater than 15 MHz at all times (the lowest probable level being 15.23 MHz and the highest 16.31 MHz). The nominal operating level for the test period is approximately 15.75 MHz.

7. ENVIRONMENTAL CONDITIONS

A record of readings for the environmental conditions is included in the Daily Check List. The list includes the Quadrant and room temperature and humidity as well as the line voltage readings.

In general, the environment was such that it had no deleterious affect on the system operation and performance, with the exception of power drops on 3 and 4 December which resulted in 2 hours 24 minutes of non-productive time during the prime shift on 4 December and hampering maintenance and corrective action efforts on the evening of 3 December and early morning of 4 December. The Quadrant line voltages remained within the test specification of 208 vac $\pm$ 10%, with lowest reading being 205.7 vac (ØA-B), and the highest reading being 210.9 vac (ØB-C).

The room temperature remained within the specified level of 65°F to 80°F throughout the test. However, the room humidity remained below the specified level (40% R.H. to 60% R.H.) in the range from 36% to 37% for most of the test except on 3 December when there was a rise to 64%. This latter condition was immediately corrected. The condition of the low humidity is not considered to have caused any problems.

Low humidity also occurred in the Quadrant going down to 39% R.H. This is not considered to have been any problem as the specified levels were 45% to 55% R.H., with a recommended change of 40% to 55% R.H. in order to provide a lower nominal humidity.

Quadrant temperature specified to be held within 68°F to 72°F, fell to 65°F on the morning of 5 December. This occurred during the scheduled maintenance period and caused no known delays.

Recording charts for the room and Quadrant temperature and humidity are on file with the NASA/Ames Operations Office. Charts for an auxillary temperature and humidity recorder operated in the room near the Quadrant are attached to the original copies of the System Event Logs.

TABLE VI

PRODUCT ASSURANCE
DAILY CHECK LIST

DATE	TIME	QUAD TEMP °F	QUAD HUMID %	ROOM TEMP °F	ROOM HUMID %	QUAD FREQ MHZ	QUAD ØA-B	LINE ØB-C	VOLT ØC-A	Q.A. INIT	REMARKS
/27/72	0646	68	45	60	50	15.7MHZ 63.5NS	207	207	207	F.D.	
/28/72	0640	66	40	68°	38%	15.7MHZ 63.5NS	205.7	205.6	209.4	F.D.	Temp in Quad below test spec. 68-72
/29/72	0635	66	44	70°	38%	63.8NS	207.7	206.0	209.7	S.K.	Humid in roo below spec. 40%-60%
/30/72	0640	68°	40	70°	36%	63.8NS	205.7	209.0	207.2	F.D.	"
/1/72	0642	68°	42	70°	38%	63.0NS	207.4	208.0	207.0	R.A.S.	
/2/72	0645	68	42	69°	39%	63.0NS	207.4	210.4	208.9	R.A.S.	
/4/72	0640	68	44	69	39	63.5NS	206.4	209.5	207.7	R.A.S.	
/5/72	0645	65	42	69	36	63.5NS	206.0	208.9	209.3	R.A.S.	
/6/72	0705	68	44	70	38	63.5NS	206.9	210.0	208.3	R.A.S	
/7/72	0650	69	43	69	37	63.5NS	207.8	210.9	209.2	R.A.S.	
/8/72	0720	69	42	68	38	63.5NS	206.7	209.7	208.0	R.A.S	

APPENDIX

SYSTEM EVENT LOG

GENERAL

The attached System Event Log provides a history of each operation or event in sequence by item number; with the time of occurrence, the corresponding UP, DOWN or NON-PRODUCTIVE time. It was maintained by Burroughs Quality Assurance representatives and each event is initialed by the Q.A. representative in attendance at that time. A carbon copy of the original of this log was provided to NASA/Ames upon completion of the test.

Determination of UP, DOWN, and NON-PRODUCTIVE Time

Variances to the Acceptance Test Procedure in determination of up, down and non-productive time were agreed upon by Burroughs and NASA/Ames Representatives subsequent to the initiation of the test. Application of the variances were made where circumstances produced situations anticipated by the variances.

1. Equipment which is being maintained at the beginning of the test will not contribute to down time until maintenance has been satisfactorily completed.

2. Transient failures are non-repeatable and non-verifiable errors. Transient down times penalties varied from 10% to 50% of the duration of the subtest during which the non-repeatable error occurred.

3. Hard failures were defined as more than one error on a single test or one or more errors occurring on the same hardware on a repeated test. In this case, the following procedure is implemented: cycle failing test for two(2) minutes in error print option -- a) if NO errors occur in the two(2)-minute cycle, then test is complete. Down time penalty in this case is equal to the initial subtest time. The two(2)-minute cycle is considered up time, b) if ERRORS occur during the two(2)-minute cycle, then the test must be stopped and the failure must be fixed by on-line repair or spares substitution. Down time penalty is for initial subtest time plus the two(2)-minute cycle, plus any additional cycles, plus on-line repair or replacement time, plus all verification time.

4. No penalty was issued for a single error in the ROM test if the test was cycled twice without further error.

5. Inasmuch as the full complement of debugged spare PUs was not available at the start of the test, it was determined that up to eight PUs could fail without resultant down time. During this test the situation never arose which required invoking this no penalty provision for more than two PUs. It should be further noted that in the last half of the 80 operating hours, there were always 64 PUs operating.