TOSHIBA AMERICA INC.

C²MOS

INTEGRATED CIRCUITS

TECHNICAL DATA

JANUARY 1985

TOSHIBA AMERICA, INC.

FOREWORD

Toshiba C^2MOS IC Family

The Toshiba C^2MOS family is a group of all-purpose CMOS digital ICs which are composed of materials having various logic functions. They not only can be used for industrial electronics equipment and home electronics equipment but also have applications in a variety of fields.

CMOS devices have such features as low power consumption, a single power supply, a wide operating voltage range and a high noise margin. In addition, they have epoch-making characteristics which conventional ICs do not have. They have recently established a firm position as all-purpose logic elements in conjunction with TTL and LSTTL.

Since the introduction of the C^2MOS IC in 1972, Toshiba has made every effort to develop products which are more reliable and less expensive.

Meanwhile, with respect to product standardization, Toshiba marketed B series products (conform to EIA/JEDEC international standards) domestically for the first time in April 1978. Then in January 1982, Toshiba became the first in Japan to develop and mass produce a compact, thin type, mini flat C^2MOS and has continued to be a world leader in the field of CMOS IC development.

Currently, in the Toshiba C^2MOS family, in addition to 149 types of standard dual inline devices, 55 types of mini flat devices are available.

In addition to this publication, there is a separate edition available which contains High Speed C^2MOS data book. Please use it along with this publication.

IMPORTANT NOTICES

The circuit examples illustrated herein are presented only as a guide for the performances or the applications of our products.

Keep in mind that no responsibility is assumed by TOSHIBA for its use, nor for any infringements of patents or other rights of the third parties which may result from its use, and that no license is granted by implication or otherwise under any patent or patent rights of TOSHIBA.

Toshiba reserves the right to make changes to any product for improving reliability, function or other characteristics.

CONTENTS

NUMERICAL INDEX

TC4000 Series

PRODUCT NAME	FUNCTION	Page
TC4000BP	DUAL 3 INPUT NOR GATE PLUS INVERTER	75
TC4001BP/TC4001BF	QUAD 2 INPUT NOR GATE	80
TC4001UBP	QUAD 2 INPUT NOR GATE	83
TC4002BP/TC4002BF	DUAL 4 INPUT NOR GATE	80
TC4006BP	18-STAGE STATIC SHIFT REGISTER	86
TC4007UBP	DUAL COMPLEMENTARY PAIR + INVERTER	90
TC4008BP	4-BIT FULL ADDER	94
TC4009UBP	HEX BUFFER/CONVERTER (Inverting Type)	97
TC4010BP	HEX BUFFER/CONVERTER (Non-Inverting Type)	97
TC4011BP/TC4011BF	QUAD 2 INPUT NAND GATE	101
TC4011UBP	QUAD 2 INPUT NAND GATE	83
TC4012BP/TC4012BF	DUAL 4 INPUT NAND GATE	101
TC4013BP/TC4013BF	DUAL D-TYPE FLIP FLOP	104
TC4014BP	8-STAGE STATIC SHIFT REGISTER	108
TC4015BP/TC4015BF	DUAL 4-STAGE STATIC SHIFT REGISTER	112
TC4016BP/TC4016BF	QUAD BILATERAL SWITCH	115
TC4017BP/TC4017BF	DECADE COUNTER/DIVIDER	119
TC4018BP	PRESETTABLE DIVIDE-BY-"N" COUNTER	124
TC4019BP/TC4019BF	QUAD AND/OR SELECT GATE	129
TC4020BP/TC4020BF	14 STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDERS	132
TC4021BP	8-STAGE STATIC SHIFT REGISTER	135
TC4022BP	OCTAL COUNTER/DIVIDER	139
TC4023BP/TC4023BF	TRIPLE 3 INPUT NAND GATE	101
TC4024BP/TC4024BF	7 STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDERS	144
TC4025BP/TC4025BF	TRIPLE 3 INPUT NOR GATE	80
TC4027BP/TC4027BF	DUAL J-K MASTER-SLAVE FLIP-FLOP	147
TC4028BP/TC4028BF	BCD-TO-DECIMAL DECODER	151
TC4029BP	PRESETTABLE UP/DOWN COUNTER	154
TC4030BP/TC4030BF	QUAD EXCLUSIVE-OR GATE	160
TC4032BP	TRIPLE SERIAL ADDER (Positive Adder)	163
TC4034BP	8-STAGE STATIC BIDIRECTIONAL PARALLEL/SERIAL IN/OUT BUS REGISTER	168
TC4035BP	4-STAGE PARALLEL IN/PARALLEL OUT SHIFT REGISTER	173
TC4036BP	4 WORD × 8 BIT STATIC RAM	178
TC4038BP	TRIPLE SERIAL ADDER (Negative Adder)	163
TC4039BP	4 WORD × 8 BIT STATIC RAM	178

TC4000 Series (Continued)

PRODUCT NAME	FUNCTION	Page
TC4040BP/TC4040BF	12 STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDERS	184
TC4042BP/TC4042BF	QUAD CLOCKED "D" LATCH	187
TC4043BP	QUAD 3-STATE NOR R/S LATCH	191
TC4044BP/TC4044BF	QUAD 3-STATE NAND R/S LATCH	195
TC4047BP	LOW-POWER MONOSTABLE/ASTABLE MULTIVIBRATOR	199
TC4049BP/TC4049BF	HEX BUFFER/CONVERTER (Inverting Type)	206
TC4050BP/TC4050BF	HEX BUFFER/CONVERTER (Non-Inverting Type)	206
TC4051BP/TC4051BF	SINGLE 8-CHANNEL MULTIPLEXER/DEMULTIPLEXER	209
TC4052BP/TC4052BF	DIFFERENTIAL 4-CHANNEL MULTIPLEXER/DEMULTIPLEXER	209
TC4053BP/TC4053BF	TRIPLE 2-CHANNEL MULTIPLEXER/DEMULTIPLEXER	209
TC4054BP	LIQUID-CRYSTAL DISPLAY DRIVER (4-Segment)	213
TC4055BP	LIQUID-CRYSTAL DISPLAY DRIVER (BCD TO 7-Segment)	217
TC4056BP/TC4056BF	LIQUID-CRYSTAL DISPLAY DRIVER (BCD TO 7-Segment)	217
TC4063BP/TC4063BF	4-BIT MAGNITUDE COMPARATOR	222
TC4066BP/TC4066BF	QUAD BILATERAL SWITCH	226
TC4068BP/TC4068BF	8 INPUT NAND/AND GATE	230
TC4069UBP/TC4069UBF	HEX INVERTER	233
TC4071BP/TC4071BF	QUAD 2 INPUT OR GATE	236
TC4072BP/TC4072BF	DUAL 4 INPUT OR GATE	236
TC4073BP/TC4073BF	TRIPLE 3 INPUT AND GATE	239
TC4075BP/TC4075BF	TRIPLE 3 INPUT OR GATE	236
TC4076BP	4-BIT D-TYPE REGISTER	242
TC4077BP/TC4077BF	QUAD EXCLUSIVE-NOR GATE	247
TC4078BP/TC4078BF	8 INPUT NOR/OR GATE	250
TC4081BP/TC4081BF	QUAD 2 INPUT AND GATE	239
TC4082BP	DUAL 4 INPUT AND GATE	239
TC4085BP	DUAL 2-WIDE 2 INPUT AND-OR-INVERT GATE	253
TC4086BP	4-WIDE 2 INPUT AND-OR-INVERT GATE	256
TC4093BP/TC4093BF	QUAD 2 INPUT NAND SCHMITT TRIGGER	260
TC4094BP/TC4094BF	8-BIT SHIFT-AND-STORE BUS REGISTER	263
TC4099BP/TC4099BF	8-BIT ADDRESSABLE LATCH	269
TC40102BP	8-STAGE PRESETTABLE DOWN COUNTER (2-Decode BCD Type)	274
TC40103BP	8-STAGE PRESETTABLE DOWN COUNTER (8-Bit Bynary Type)	274
TC40104BP	4-BIT BIDIRECTIONAL SHIFT REGISTER WITH 3-STATE OUTPUTS	283
TC40107BP	DUAL 2 INPUT NAND BUFFER/DRIVER	289

TC4000 Series (Continued)

PRODUCT NAME	FUNCTION	Page
TC40117BP	PROGRAMMABLE DUAL 4-BIT TERMINATOR	292
TC40160BP	PROGRAMMABLE DECADE COUNTER WITH ASYNCHRONOUS CLEAR	297
TC40161BP	PROGRAMMABLE BINARY COUNTER WITH ASYNCHRONOUS CLEAR	297
TC40162BP	PROGRAMMABLE DECADE COUNTER WITH SYNCHRONOUS CLEAR	297
TC40163BP	PROGRAMMABLE BINARY COUNTER WITH SYNCHRONOUS CLEAR	297
TC40174BP/TC40174BF	HEX "D"-TYPE FLIP-FLOP	305
TC40175BP/TC40175BF	QUAD "D"-TYPE FLIP-FLOP	309
TC40192BP	PRESETTABLE BCD UP/DOWN COUNTER	313
TC40193BP	PRESETTABLE BINARY UP/DOWN COUNTER	313
TC40194BP	4-BIT BIDIRECTIONAL SHIFT REGISTER WITH RESET	283

TC4500 Series

PRODUCT NAME	FUNCTION	Page
TC4501BP	TRIPLE GATE (Dual 4 Input NAND + 2 Input NOR/OR)	320
TC4502BP	STROBED HEX INVERTER/BUFFER	324
TC4508BP	DUAL 4-BIT LATCH	328
TC4510BP/TC4510BF	PRESETTABLE BCD UP/DOWN COUNTER	333
TC4511BP/TC4511BF	BCD TO 7-SEGMENT LATCH/DECODER/DRIVER	339
TC4512BP/TC4512BF	8-CHANNEL DATA SELECTOR	343
TC4514BP	4-BIT LATCH/4-TO-16 LINE DECODER (High)	346
TC4515BP	4-BIT LATCH/4-TO-16 LINE DECODER (Low)	346
TC4516BP/TC4516BF	PRESETTABLE BINARY UP/DOWN COUNTER	351
TC4518BP/TC4518BF	DUAL BCD UP COUNTER	357
TC4519BP	4-BIT AND/OR SELECTOR	363
TC4520BP/TC4520BF	DUAL BINARY UP COUNTER	357
TC4521BP	24-STAGE FREQUENCY DIVIDER	366
TC4522BP	PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (BCD)	371
TC4526BP/TC4526BF	PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (Binary)	371
TC4527BP	BCD RATE MULTIPLIER	379
TC4528BP/TC4528BF	DUAL MONOSTABLE MULTIVIBRATOR	385
TC4530BP	DUAL 5-INPUT MAJORITY LOGIC GATE	389
TC4531BP	12-BIT PARITY TREE	392
TC4532BP	8-BIT PRIORITY ENCODER	395
TC4538BP/TC4538BF	DUAL PRECISION MONOSTABLE MULTIVIBRATOR	399
TC4539BP/TC4539BF	DUAL 4-CHANNEL DATA SELECTOR/MULTIPLEXER	404

TC4500 Series (Continued)

PRODUCT NAME	FUNCTION	Page
TC4543BP/TC4543BF	BCD TO 7-SEGMENT LATCH/DECODER/DRIVER	407
TC4555BP	DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER (High)	412
TC4556BP/TC4556BF	DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER (Low)	412
TC4560BP	NBCD ADDER	416
TC4561BP	9'S COMPLEMENTER	421
TC4572BP/TC4572BF	HEX GATE (4 INVERTER + 2 Input NOR + 2 Input NAND)	425
TC4583BP	DUAL SCHMITT TRIGGER	428
TC4584BP/TC4584BF	HEX SCHMITT TRIGGER	432
TC4585BP	4-BIT MAGNITUTE COMPARATOR	435

TC5000 Series

PRODUCT NAME	FUNCTION	Page
TC5001P	4-DIGIT DEGADE COUNTER	439
TC5002BP	BCD TO 7-SEGMENT DECODER/LED DRIVER	449
TC5012BP/TC5012BF	HEX NON-INVERTING 3-STATE BUFFER	454
TC5018P	4-BIT BINARY COUNTER/CLOCK GENERATOR	457
TC5020BP	HEX LOW-TO-HIGH VOLTAGE TRANSLATOR	461
TC5022BP	BCD TO 7-SEGMENT DECODER/LED DRIVER	449
TC5023BP	16-CHANNEL MULTIPLEXER	464
TC5024BP	QUAD 3-STATE NON-INVERTING BUFFER	467
TC5025BP	QUAD 3-STATE NON-INVERTING BUFFER	467
TC5026BP	DECADE COUNTER	471
TC5027BP	BINARY COUNTER	475
TC5029BP	QUAD 2-INPUT NAND OPEN DRAIN GATE (N-CHANNEL)	479
TC5032P	6-DIGIT DECADE COUNTER	482
TC5036P	17-STAGE HIGH SPEED FREQUENCY DIVIDER (DYNAMIC)	491
TC5037P	4-DIGIT DECADE COUNTER	495
TC5043P	CR TIMER	502
TC5048P	17-STAGE HIGH SPEED FREQUENCY DIVIDER (DYNAMIC)	491
TC5050P	DUAL 50/64-STAGE STATIC SHIFT REGISTER	509
TC5051P	4-DIGIT DECADE COUNTER	511
TC5052P	4-DIGIT DECADE COUNTER	511
TC5053P	4-DIGIT UP/DOWN DECADE COUNTER	518
TC5054P	4-DIGIT UP/DOWN DECADE COUNTER	518
TC5064BP	HEX HIGH VOLTAGE BUFFER WITH INHIBIT	523

TC5000 Series (Continued)

PRODUCT NAME	FUNCTION	Page
TC5065BP	HEX HIGH VOLTAGE BUFFER WITH INHIBIT	523
TC5066BP	7-LINE HIGH VOLTAGE BUFFER	527
TC5067BP	7-LINE HIGH VOLTAGE BUFFER	527
TC5068BP	BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER	531
TC5069BP	BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER	531
TC5070P	6 DIGIT UNIVERSAL COUNTER "999999"	537
TC5071P	6 DIGIT UNIVERSAL TIMER "995959"	537
TC5072P	6 DIGIT UNIVERSAL TIMER "595999"	537
TC5090AP	8-BIT A/D CONVERTER	551
TC5091AP	8-BIT A/D CONVERTER (WITH ANALOG MPX.)	563
TC5092AP	13-BIT A/D CONVERTER (WITH ANALOG MPX.)	576

TC7400 Series

PRODUCT NAME	FUNCTION	Page
TC7400BP	QUAD 2-INPUT POSITIVE NAND GATE	587
TC7404UBP	HEX INVERTING BUFFER	590
TC7476BP	DUAL J-K MASTER SLAVE FLIP FLOP	593

FUNCTION SELECTION TABLE

FUNCTION			DEVICES
GATES BUFFERS	NAND		TC4011BP/BF,TC4011UBP,TC4012BP/BF,TC4023BP/BF,TC4068BP/BF,TC7400BP
	NOR		TC4000BP,TC4001BP/BF,TC4001UBP,TC4002BP/BF,TC4025BP/BF,TC4078BP/BF
	AND		TC4068BP/BF,TC4073BP/BF,TC4081BP/BF,TC4082BP
	OR		TC4071BP/BF,TC4072BP/BF,TC4075BP/BF,TC4078BP/BF
	INVERTER		TC4007UBP,TC4009UBP,TC4049BP/BF,TC4069UBP/UBF,TC7404UBP
	BUFFERS		TC4009UBP,TC4010BP,TC4049BP/BF,TC4050BP/BF
		3-STATE	TC4502BP,TC5012BP/BF,TC5024BP,TC5025BP
		OPEN DRAIN	TC40107BP,TC5029BP,TC5064BP,TC5065BP,TC5066BP,TC5067BP
	MULTIFUNCTION		TC4019BP/BF,TC4030BP/BF,TC4077BP/BF,TC4085BP,TC4086BP,TC4501BP, TC4519BP,TC4530BP,TC4572BP/BF
	SCHMITT TRIGGER		TC4093BP/BF,TC4583BP,TC4584BP/BF
	LEVEL SHIFTER		TC4009UBP,TC4010BP,TC4049BP/BF,TC4050BP/BF,TC5020BP
FLIP-FLOP			TC4013BP/BF.TC4027BP/BF,TC40174BP/BF,TC40175BP/BF,TC7476BP
LATCHES			TC4042BP/BF,TC4043BP,TC4044BP/BF,TC4099BP/BF,TC4508BP
MULTIVIBRATORS			TC4047BP,TC4528BP/BF,TC4538BP/BF
DECODERS			TC4028BP/BF,TC4514BP,TC4515BP,TC4555BP,TC4556BP/BF
DISPLAY DRIVER		LED	TC4511BP/BF,TC5002BP,TC5022BP
		LCD	TC4054BP,TC4055BP,TC4056BP/BF,TC4543BP/BF
		DIGITRON	TC5068BP,TC5069BP
ENCODER			TC4532BP
REGISTERS		SHIFT	TC4006BP,TC4014BP,TC4015BP/BF,TC4021BP,TC4034BP,TC4035BP,TC4094BP/BF, TC40104BP,TC40194BP,TC5050P
		STORAGE	TC4076BP
COUNTERS		BINARY	TC4029BP,TC40161BP,TC40163BP,TC40193BP,TC4516BP/BF,TC4520BP/BF, TC5018BP,TC5027BP
		DECADE	TC4029BP,TC40160BP,TC40162BP,TC40192BP,TC4510BP/BF,TC4518BP/BF, TC5026BP
		DIVIDER	TC4020BP/BF,TC4024BP/BF,TC4040BP/BF,TC4521BP,TC5036P,TC5048P
		DIVIDE-BY-"N"	TC4018BP,TC40102BP,TC40103BP,TC4522BP,TC4526BP/BF
		N-DIGIT DECADE	TC5001P,TC5032P,TC5037P,TC5051P,TC5052P,TC5053P,TC5054P, TC5070P
		OTHER	TC4017BP/BF,TC4022BP
TIMERS			TC5043P,TC5071P,TC5072P
MULTI-PLEXERS		ANALOG	TC4051BP/BF,TC4052BP/BF,TC4053BP/BF
		DIGITAL	TC4512BP/BF,TC4539BP/BF,TC5023BP
ARITHMETIC CIRCUITS	ADDER		TC4008BP,TC4032BP,TC4038BP,TC4560BP
	COMPARATOR		TC4063BP/BF,TC4585BP
	PARITY TREE		TC4531BP
	RATE MULTIPLIER		TC4527BP
	9'S COMPLEMENTER		TC4561BP
MEMORIES (RAM)			TC4036BP,TC4039BP
A/D CONVERTERS			TC5090AP,TC5091AP,TC5092AP
ANALOG SWITCH			TC4016BP/BF,TC4066BP/BF
OTHER			TC40117BP

EXPLANATION

OUTLINE

1. C^2MOS IC Family

1.1 CMOS and C^2MOS

"CMOS" is an abbreviation of "Complementary Metal Oxide Semiconductor", and "Complementary" means to combine P-channel type MOS FET and N-channel type MOS FET complementarily. The CMOS circuit configuration, since its announcement at ISSCC in 1963, attracted a large expectation for its performance with super-low power consumption and operation at low voltage, and after such process as settlement of production problems through the ion implantation process, reduction in pattern size through circuit research, etc., has now been established as one field of integrated circuits.

At present, use of CMOS LSI in electronic calculators, clocks, etc. is remarkable. In addition to these LSI, the features of CMOS are also very attractive in the field of so-called industrial electronic equipment including measuring and control equipment, business machines, etc., and it may be said to be a matter of course that CMOS logic family is demanded.

To respond these need promptly, TOSHIBA has put CMOS logic element on sale as C^2MOS IC Family.

C^2MOS is an abbreviation of "Clocked CMOS", which is one of the CMOS circuit configurations. This type of circuit was made public by Toshiba at ISSCC in 1973 and since then, it has been applied to mainly sequential circuits of TOSHIBA's MSI and LSI as it becomes an extremely powerful circuit means.

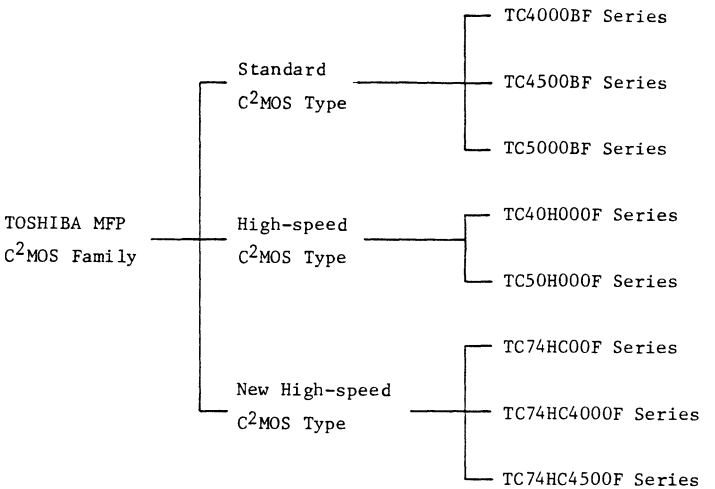
Therefore, C^2MOS is used as the general name of TOSHIBA CMOS ICs including combined circuits without clocked gate used.

1.2 TOSHIBA C^2MOS Family

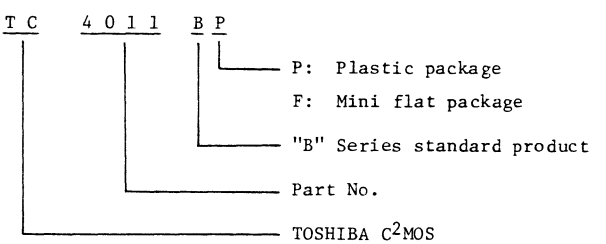
C^2MOS Family products shown below are made available from TOSHIBA for use in all sorts of equipment.

- TOSHIBA C^2MOS
  - Standard C^2MOS
    - TC4000B Series
      Compatible with RCA's CD4000B Series
    - TC4500B Series
      Compatible with MOT's MC14500B Series
    - TC5000B/TC5000 Series
      TOSHIBA's original series
    - TC7400B Series
      Compatible with TTL 54/74 Series
  - High-speed C^2MOS
    - TC40H000 Series
      Compatible with TTL 54/74 Series
    - TC50H000 Series
      TOSHIBA's original series
  - New High-speed C^2MOS
    - TC74HC00 Series
      Compatible with TTL 54/74 Series
    - TC74HC4000 Series
      Compatible with RCA's CD4000B Series
    - TC74HC4500 Series
      Compatible with MOT's MC14500B Series
    - TC74HCT000 Series
      Input level is compatible with TTL

Further, the Mini-Flat Package (MFP) C^2MOS Family products are also available from TOSHIBA to satisfy demands of equipment for compact size and light weight.



1.3 Standard Construction of Model No. of C^2MOS Family Products



1.4 TOSHIBA B Series C^2MOS

TOSHIBA B Series C^2MOS have ratings and characterisitcs satisfying EIA/JEDEC standards; definitely speaking, they have basic characteristics shown below:

- o A wider operating supply voltage range of 3 ~ 18V.
- o Guaranteed electrical characteristics under 3 supply voltage conditions of 5V, 10V and 15V.
- o Buffer structure adopted for all outputs
- o 2 inputs of LTTL (Low Power TTL) and 1 input of LSTTL (Low Power Shottkey TTL) can be directly driven.

Noise Immunity:

1V (Min)	@ V_{DD} = 5V	*1
2V (Min)	@ V_{DD} = 10V	
2.5V (Min)	@ V_{DD} = 15V	

*1 "UB" Series products and some products including analog switch, level shifter, etc. have different noise margines.

2. Operational Principle and Features of CMOS

2.1 Basic circuit and structure of CMOS

Inverter circuit is taken as an example of CMOS basic circuit. CMOS inverter, as shown in Fig. 2-1, consists of the common input terminal shared by P-channel enhancement (normally off) type MOS FET and N-channel enhancement type MOS FET and the common output terminal shared by each drain.

As shown in the same figure, CMOS inverter uses P-channel and N-channel MOS FETs complementarily.

Usually, the source of P-channel MOS FET is connected to V_{DD} (+supply) and the source of N-channel MOS FET is connected to V_{SS} (usually GND).

Fig. 2-2 illustrates the cross section using the basic process. N-type silicon is used as substrate for CMOS basic process.

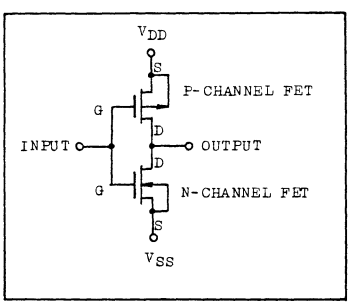


Fig. 2-1 Circuit Diagram of CMOS Inverter

For normal P-channel MOS FETs, P-type impure material is selectively diffused in the domain of N-type substrate to form the source and the drain. For CMOS, however, since N-channel MOS FET is also required to be formed in same substrate, after forming P-type island domain (P-well) in N-type substrate by means of ion implanation, N-channel MOS FET is formed in this P-well. And P-channel MOS FET is formed in the substrate outside of this island domain.

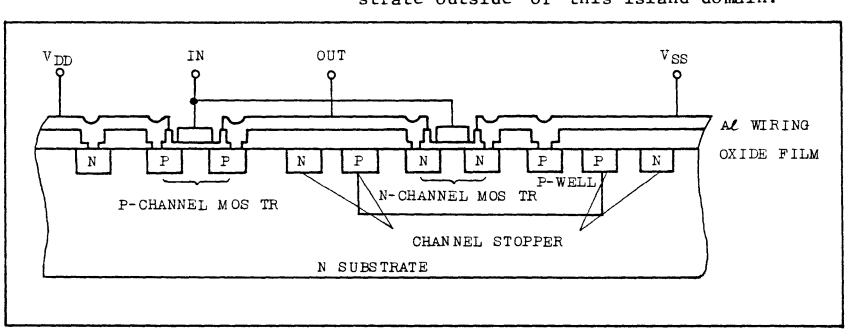


Fig. 2-2 Structural Cross Section of Al Gate CMOS

N-type substrate and P-well are separated (reverse biased) by V_{DD} and V_{SS}. Therefore, P-channel and N-channel FETs operate independently each other with no mutual interferences.

Fig. 2-2 is the basic cross section of CMOS inverter. The static protection circuit is inserted in the input gate as shown in Fig. 2-3 for the actual products.

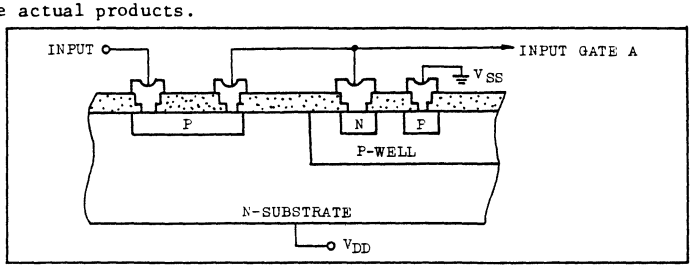


Fig. 2-3 CMOS Input Protection Circuit

Fig. 2-4 shows the equivalent circuit of CMOS inverter including the input protection circuit and the parasitic circuits. Fig. 2-4 actually represents the circuits of TC4069 UBP and TC7404 UBP.

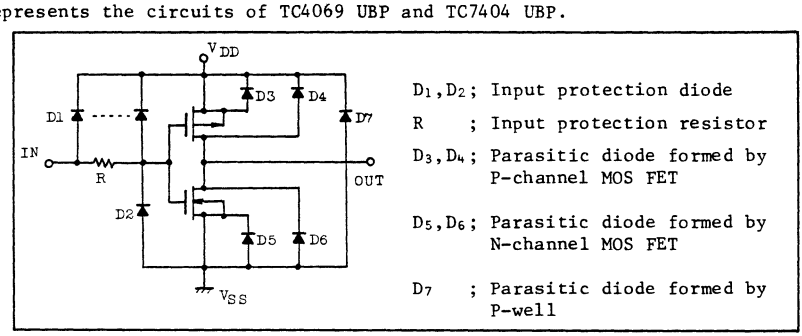


Fig. 2-4 CMOS Inverter taking Parasitic Circuits into Consideration

Although the diodes inserted in the equivalent circuit are all reverse bias during operation without causing any interferences for normal circuit operation, caution should be observed since degradation and damage of the elements may be resulted by making those diodes forward biased when the power supply is connected with reverse polarity or the interface is driven roughly.

2.2 Basic characteristics of CMOS

CMOS is a classification based on the circuit configuration and the characteristics of each MOS FET actually used are equal to common enhancement type FETs.

Therefore, in the case of CMOS also, the characteristics of P-channel and N-channel MOS FETs can be basically approximated by Shockley's equation.

$$I_{DS} = K\,[2V_{DS}(V_{GS} - V_T) - V_{DS}^2], \quad V_{DS} < V_{GS} - VT \quad \cdots\cdots (2.1)$$

$$I_{DS} = K\,(V_{GS} - V_T)^2, \quad V_{DS} \geq V_{GS} - V_T \quad \cdots\cdots (2.2)$$

$$I_{DS} = 0, \quad V_{GS} \leq V_T \quad \cdots\cdots (2.3)$$

Where the constant K is

$$K = \frac{W}{2L} \cdot \frac{Eox}{t_{ox}} \cdot \mu$$

- L ; Channel length
- W ; Channel width
- E_{ox} ; Dielectric constant of gate oxide film
- t_{ox} ; Thickness of gate oxide film
- μ ; Mobility of electron or positive hole
- V_{DS} ; Potential difference between drain and source
- V_{GS} ; Potential difference between gate and source
- V_T ; Threshold voltage

Using the above approximation equations (2.1) ∿ (2.3), the basic characteristics are explained below taking inverter as an example.

(1) Transfer characteristic of inverter

The input voltage, the output voltage and the power supply voltages are assumed to be V_{IN}, V_{OUT} and $+V_0$ volts respectively. The threshold voltages are assumed to be V_{TP} for P-channel FET and V_{TN} for N-channel FET respectively.

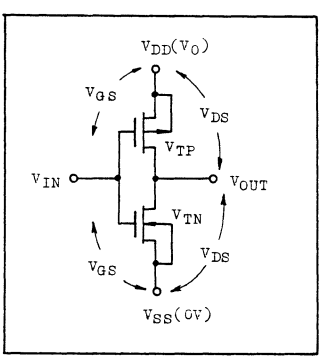


Fig. 2-5 Relationships of ·Various Bias

Here, V_{TP} is considered to have negative value and V_{TN} to have positive value. As it is clear from Fig. 2-5, V_{DS} and V_{GS} which appeared in equations (2.1) ∿ (2.3) are

$$V_{DS} = V_{OUT} \ , \ V_{GS} = V_{IN}$$

for N-channel FET.
So, equations (2.1) ∿ (2.3) can be rewritten as shown below.

$$I_{DSN} = K_N [2V_{OUT}(V_{IN}-V_{TN})-V_{OUT}^2], \quad V_{OUT} < V_{IN} - V_{TN} \quad \cdots (2.4)$$

$$I_{DSN} = K_N (V_{IN} - V_{TN})^2 \quad , \quad V_{OUT} \geqq V_{IN} - V_{TN} \quad \cdots (2.5)$$

$$I_{DSN} = 0 \quad , \quad V_{IN} \leqq V_{TN} \quad \cdots (2.6)$$

On the other hand, since

$$V_{DS} = V_O - V_{OUT} \quad \text{AND} \quad V_{GS} = V_O - V_{IN}$$

for P-channel, equations (2.1) ∿ (2.3) can be rewritten as follows.

$$I_{DSP} = K_P[2(V_O-V_{OUT})(V_O-V_{IN}-|V_{TP}|)-(V_O-V_{OUT})^2],$$

$$V_{OUT} > V_{IN} + |V_{TP}| \quad \cdots\cdots (2.7)$$

$$I_{DSP} = K_P(V_O-V_{IN}-|V_{TP}|)^2, V_{OUT} \leqq V_{IN} + |V_{TP}| \quad \cdots\cdots (2.8)$$

$$I_{DSP} = 0 \quad , V_{IN} + |V_{TP}| \geqq V_O \quad \cdots\cdots (2.9)$$

When the input voltage of inverter varies from 0 volts to V_O volts, the operating range of each MOS FET can be classified into the following five regions.

① $0_V \leqq V_{IN} \leqq V_{TN}$

② $V_{TN} < V_{IN} < V_{OUT} - |V_{TP}|$

③ $V_{OUT} - |V_{TP}| \leqq V_{IN} \leqq V_{OUT} + V_{TN}$

④ $V_{OUT} + V_{TN} < V_{IN} < V_O - |V_{TP}|$

⑤ $V_O - |V_{TP}| \leqq V_{IN} \leqq V_O$

The currents in the above five regions for each FET forming the inverter can be represented by equations (2.4) ∿ (2.9) respectively.

When the input/output transfer characteristic is to be obtained, since the current carried by P-channel, I_{DSP} is equal to the current carried by N-channel, I_{DSN}, the transfer characteristic in each region is obtained by making $I_{DSN} = I_{DSP}$.

Especially, by making $I_{DSN} = I_{DSP}$ in the equations (2.5) and (2.8) of current in the region of 2 , the following equation is obtained.

$$V_{IN} = \frac{V_{TN}\left(\sqrt{\frac{K_N}{K_P}}\right) + V_O - |V_{TP}|}{1 + \left(\sqrt{\frac{K_N}{K_P}}\right)}$$

Fig. 2-6 shows the comparison between the theoretical values obtained by those equations and the measuring values.

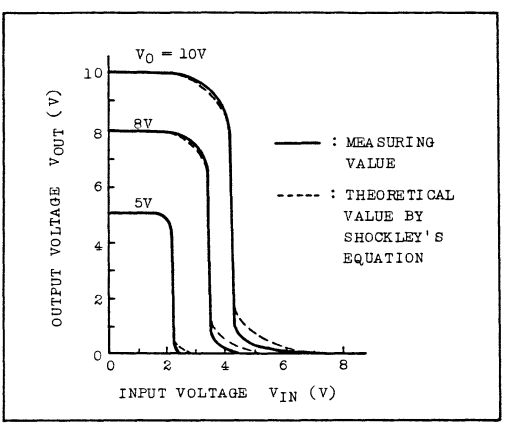


Fig. 2-6 Input/Output Transfer Characteristics

(2) Step response of inverter

When step input which varies from 0 volts to $+V_O$ volts is applied to the inverter input, P-channel FET is turned off and N-channel FET is turned on. As a result, electrical charge stored in the load capacitor C_{OUT} is discharged through N-channel FET and the output voltage V_{OUT} varies from $+V_O$ volts to 0 volts as the discharge proceeds.

a) When $V_{OUT} \geqq V_O - V_{TN}$

The equation for current is given by (2.5) and since C_{OUT} is discharged by this current,

$$- I_{DSN} = C_{OUT} \frac{d V_{OUT}}{dt}, \quad V_{OUT} = V_O \text{ at } 5 = 0$$

When this is integrated,

$$\int_o^t dt = -\int_{V_O}^{V_{OUT}} \frac{C_{OUT}}{K_N(V_O - V_{TN})^2} \cdot dV_{OUT}$$

Namely,

$$t = \frac{C_{OUT}}{K_N(V_O - V_{TN})^2} (V_O - V_{OUT}) \quad \cdots\cdots \quad (2.10)$$

If t_0 is defined at $V_{OUT} = V_O - V_{TN}$,

$$t_0 = \frac{C_{OUT} \cdot V_{TN}}{K_N(V_O - V_{TN})^2}$$

b) When $V_{OUT} \leqq V_O - V_{TN}$

If integrated similarly as a) using equation (2.4),

$$\int_o^t dt = \frac{-C_{ONT}}{2K_N(V_O - V_{TN})} \times \int_{V_O - V_{TN}}^{V_{OUT}} \left\{ \frac{1}{V_{OUT}} + \frac{1}{2(V_O - V_{OUT}) - V_{OUT}} \right\} dV_{OUT}$$

Then,

$$t = \frac{C_{OUT}\ V_{TN}}{K_N(V_O - V_{TN})} + \frac{C_{OUT}}{2K_N(V_O - V_{TN})} \ell_n \left[\frac{2(V_O - V_{TN}) - V_{OUT}}{V_{OUT}} \right] \quad \cdots\cdots \quad (2.11)$$

As the fall time t_f is the time required for the output voltage to vary from 90% to 10%, if t_1 is assumed to be the time for the output voltage to reach 90% of V_O and t_2 is assumed to be the time to reach 10% of V_O, t_1 and t_2 are given from equations (2.10) and (2.11) as follows.

$$t_1 = \frac{C_{OUT}}{K_N(V_O - V_{TN})^2} \times 0.1V_O$$

$$t_2 = \frac{C_{OUT}\ V_{TN}}{K_N(V_O - V_{TN})^2} + \frac{C_{OUT}}{2K_N(V_O - V_{TN})} \ell_n \left[\frac{2(V_O - V_{TN}) - 0.1V_O}{0.1V_O} \right]$$

Therefore,

$$t_f = t_2 - t_1 = \left\{ \frac{V_{TN} - 0.1V_O}{V_O - V_{TN}} + 1/2 \ \ell n \ [20(1 - \frac{V_{TN}}{V_O}) - 1] \right\} \times \gamma_N \quad \ldots (2.12)$$

$$\text{where} \quad \left\{ \begin{array}{l} \tau N = \dfrac{C_{OUT}}{K_N(V_O - V_{TN})} \\ K_N = 1/2 \cdot \dfrac{\varepsilon_{OX} \ \mu_N}{t_{OX}} \cdot \dfrac{W_N}{L_N} \end{array} \right\}$$

The rise time t_r can be obtained similarly and the result will be the same as equation (2.12) except that N is replaced by P.

2.3 Features of CMOS

Table 2-1 compares the characteristics of logic families including CMOS. From this table it is clear that although the speed is slower than others, the power dissipation in quiescent state and the noise immunity are far superior to others.

And since CMOS has wider operating supply voltage range, the supply voltage can be flexibly set according to the applications and where to be used.

Table 2-1 Comparison of Various Logic Families

Parameter (typical values)	Standard TTL	Low power TTL	Low power Schottky TTL	CMOS (5V)	CMO S (10V)
Propagation Delay Time(ns)	10	33	5 ∿ 10	70	35
F/F Toggle Frequency (MHz)	35	3	40 ∿ 80	3	6
Quiescent Power Dissipation (mW)	10	1	8.5	5×10^{-6}	2×10^{-5}
Noise Immunity (V)	1	1	0.8	2	4
Fanout	10	10	20	50	50

(1) Propagation delay time and F/F toggle frequency

As shown by equation (2.12) in 2.2, the propagation delay time of CMOS is proportional to C_{OUT} (load capacitance) and inversely proportional to the constant K_N which is determined by design and process.

Therefore, in order to make the propagation delay time shorter, it is necessary to make C_{OUT} smaller and W/L in design considerations. However, since the internal diffusion cpapcitance in CMOS is included in C_{OUT}, the internal capacitance increases proportionally to W/L and actually the propagation delay time tends to have a limitation.

In the standard C^2MOS ICs the propagation delay time is determined by balancing other electrical parameters since there are other limitations such as the output current and the breakdown voltage causing to have larger value than other logic elements as shown in Table 2-1.

However, the products for specific applications and CMOS ICs having the capabilities of high speed operations for the high speed frequency divider are currently being developed, and the speed of around 10ns delay per internal stage of CMOS at 5 volts has been obtained providing the expectation that the product range of such CMOS will be expanded for the systems requiring the high frequency operations in the feature.

(2) Quiescent (Static) power dissipation and operating power dissipation

In the standard CMOS, when the input holds "L" (V_{SS}) level or "H" (V_{DD}) level, N-channel FET or P-channel FET is kept turned off. So, the current from V_{DD} to V_{SS} is limited to the reverse direction saturation current of PN junction and the surface leakage current caused mainly by contamination on the chip surface; consequently, the value is only 1nA $\sim$ 2nA at the normal temperature for gate ICs.

In the case of other logic circuits except CMOS, when the output driving transistor is turned on, direct current flows down from V_{CC} to GND through the load causing the power dissipation in the quiescent state to be approximately equal to the operating power dissipation.

The operating power dissipation of CMOS can be considered to be only the switching power loss which is generated to charge/discharge the load capacitance while inverting the logical levels, so that the operating power dissipation is proportional to the switching frequency.

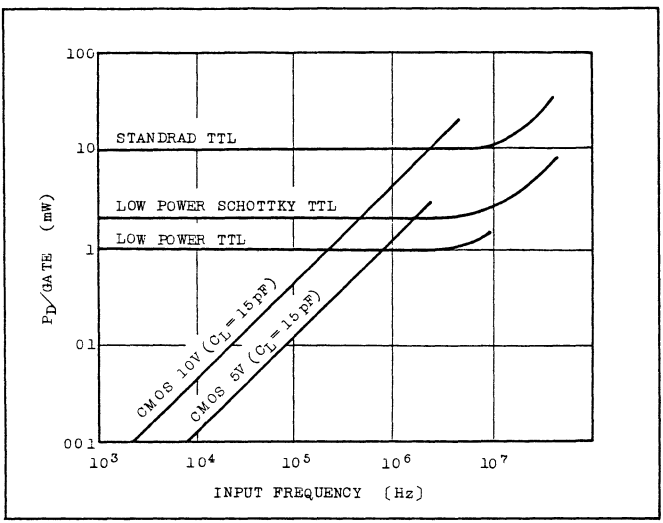


Fig. 2-7 Operating frequency VS Power Dissipation of CMOS/TTL

Fig. 2-7 shows the relationship between the operating frequency and the power dissipation of TTL and CMOS, As shown in the figure, the advantages of CMOS will be fully utilized at the operating frequency lower than 10^6Hz.

(3) Noise immunity

For CMOS circuits as shown in Fig.2-6, since the device threshold voltage is ideally set to the mid-point of supply voltage, the maximum noise immunity can be obtained among the various logic devices. It can be seen from the same figure that the standard value of noise immunity for CMOS is 2 volts (at V_{DD} = 5V) or 4 volts (at V_{DD} = 10V), which are considerably larger than the value of 1 volt for TTL.

The device threshold voltage of CMOS, however, is determined by On-resistance ratio of P-channel and N-channel MOS FETs and directly affected by the variations of those values. Therefore, the noise immunity guaranteed in the catalog of "B Series" products is 1 volt (at V_{DD} = 5V) or 2 volts (at V_{DD} = 10V), and attention should be paid to this point.

(4) Fanout

Since the protection diodes are reversely biased as long as rating voltages ($V_{SS} \sim V_{DD}$) are applied, CMOS input has extremely high DC impedance ($R_{IN} \doteqdot 10^{11}\Omega$).

Furthermore, since the gate of MOS FET equivalently functions as one of electrodes of parallel plate capacitor, AC characteristic indicates the capacitive value of approximately 5pF.

This situation can be illustrated as shown in Fig. 2-8. These resistive component and capacitive component are insertes in parallel to V_{DD} side and V_{SS} side.

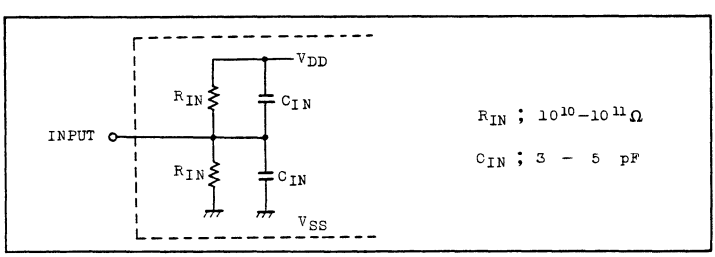


Fig. 2-8 Equivalent Circuit of CMOS Input

Therefore, in order to drive CMOS input, only very little current is required electrically to supply or to drain. This fact means that the output impedance of normal CMOS is around 200 - 1K Ω which makes it possible to drive the almost unlimited number of CMOS in DC operation.

However, as the number of fanout increases (n, for example), all of input capacitance C_{IN} are connected in parallel, increasing the load capacitance of output. So, the load capacitance viewed from the driving side is,

$$C_L = n \cdot C_{IN} + C_S \quad \text{..... (2.13)}$$

C_S : Stray capacitance generated by wiring, etc.

and this C_L causes the propagation delay time to increase.

Considering these situations, the practical number of fanout for C^2MOS has been determined to be 50. The fact that 50 fanouts can be actually provided eliminates almost all restrictions in the wiring arrangements of wired logic circuits.

3. Basic Circuit of CMOS

3.1 Positive logic and negative logic

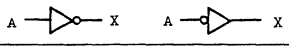
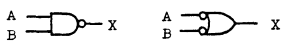
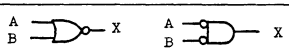
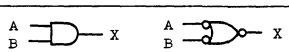
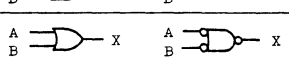
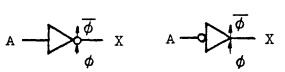
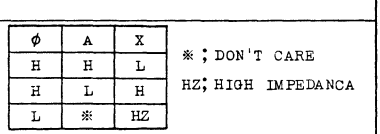
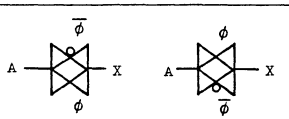
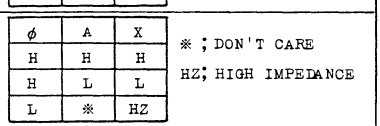
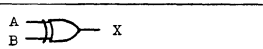
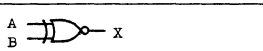
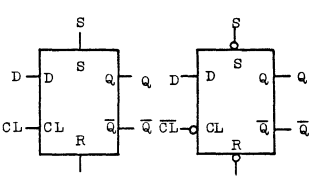
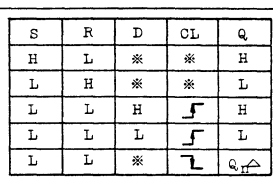
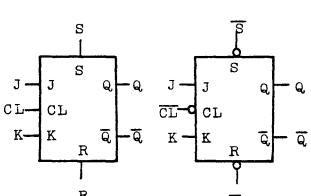
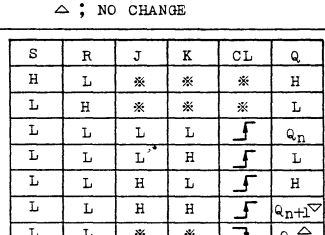
The difference between positive logic and negative logic is only conceptual difference and it can not be said that the positive logic should be sued for CMOS.

The netative logic is easier to consider about P-channel MOS device due to the fact that negative supply voltages are used and that FET is turned on when negative potential is applied. However in CMOS both P channel and N-channel are the driving MOS and also the load MOS, so the conditions are same for the positive logic and the negative logic.

It has been decided that C^2MOS family is described in the positive logic in the catalog because of the facts that the positive logic is easier to handle for the design engineers who are familiar with the design works of wired logic circuits especially with TTL and that recently N-channel LSI become more and more popular and the positive logic is more convenient for the interfaces.

In order to avoid any confusion on the positive logic and the negative logic of the truth table, the potentially high logic level is described to be "H" level and the low logic level to be "L" level. Therefore, "H" in the truth table corresponds to "1" of the positive logic and "L" corresponds to "0" of the same posotive logic.

Table 3-1 Basic Logical Circuits

Circuit Function	Logical Symbol	Logical Equation or Truth Table
Inverter		$X = \overline{A}$
NAND Gate		$X = \overline{A \cdot B} = \overline{A} + \overline{B}$
NOR Gate		$X = \overline{A + B} = \overline{A} \cdot \overline{B}$
AND Gate		$X = A \cdot B = \overline{\overline{A} + \overline{B}}$
OR Gate		$X = A + B = \overline{\overline{A} \cdot \overline{B}}$
Clocked Inverter		
Transmission Gate		
EXCLUSIVE-OR Gate		$X = (A + B) \cdot (\overline{A} + \overline{B})$
EXCLUSIVE-NOR Gate		$X = (A \cdot B) + (\overline{A} \cdot \overline{B})$
D - Type Flip - Flop		
J/K Type Flip - Flop		

3.2 Basic logic circuits

The basic logic blocks used in C^2MOS are shown in Table 3-1. The logic diagrams illustrated in the technical bulletin of each product and the logic diagrams in this manual are configured by the basic blocks shown in Table 3-1. With partial exceptions, these logic diagrams are based on MIL-STD806(C). (Special symbols are used for the clocked inverter, the transmission gate, etc.)

3.3 Configuration of basic circuit

(1) NAND/NOR

CMOS NAND gate, as illustrated in Fig. 3-1 i), is formed by connecting P-channel FETs in parallel between V_{DD} and the output and by connecting N-channel FETs in series between V_{SS} and the output.

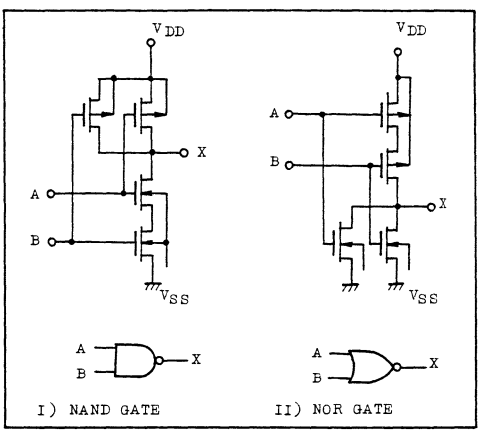


Fig. 3-1 NAND/NOR Gate

When both inputs A and B are "H", both of N-channel FETs in series are turned on, causing the impedance between X and V_{SS} to be low. At this time, both of P-channel FETs are turned off cutting off X from V_{DD}. Therefore, the output becomes nearly equal to V_{SS} generating "L" level. In the case of other input modes, at last one of P-channels FETs is turned on and one N-channel FETs are turned off causing the output to be "H" level.

NOR gate of ii) in Fig. 3-1 is fabricated in the reversed way of NAND gate i) to generate "H" output only when both of inputs A and B are "L".

The gates with 3 inputs or more can be realized with the same configuration simply by increasing the number of stages of P-channel or N-channel FETs in series or in parallel. In the case of C^2MOS up to around four inputs the device can be configured with one stage, but the gates with more inputs are realized by combining the basic circuits.

(2) AND/OR

Since the output is always inverted by one stage of CMOS gate, AND gate and OR gate are realized by adding an inverter to the output of NAND/OR of (1).

Therefore, it is important for CMOS MSI/LSI to effectively combine NAND/NOR rather than to fabricate the gates with AND/OR, in order to reduce the number of elements.

(3) Transmission gate

Fig. 3-2 illustrates the basic circuit of transmission gate. This circuit provides the function of reed switch which transmits the data when both of P-channel and N-channel are "ON" (c="H") and separates the output from the input when those are "OFF" (C="L").

Since both of P-channel and N-channel are used, the capability of cancelling the back gate bias effect is one of advantages and the capability of keeping the low impedance over the wide signal range of $V_{SS} \sim V_{DD}$ is another advantage.

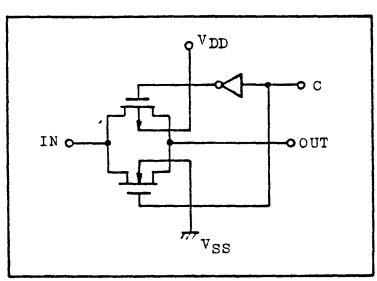


Fig. 3-2 Transmission Gate

The applications would be as follows.

i) Switching functions of sequencial circuits, such as shift registers, counters, etc.

ii) Analog switches

iii) 3-stage gates*

*3-state gates: 3-state is named for the capability of providing three states of output which are normal "H", normal "L" and high impedance condition not being connected to V_{DD} or V_{SS}, namely not "H" nor "L". This characteristic can be applied for the intervace with bus line of process control systems and multiplexers.

(4) Clocked gate

When a delay circuit or a switching circuit is required, the transmission gate is usually used. However, this circuit has a disadvantage that the pattern becomes more complicated with increased area when the circuit is to be integrated in LSI. The one which overcomes this disadvantage keeping the characteristics of conventional transmission gate is the clocked gate (clocked inverter) shown in Fig. 3-3.

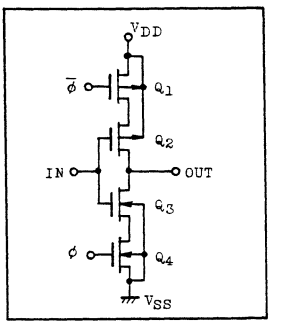


Fig. 3-3 Clocked Gate

Q2 and Q3 are normal configuration of inverter, however by serially inserting Q1 and Q4 in the circuit, the function of normal inverter can be obtained when Q1 and Q4 are "ON" (ϕ="H") and the output has high impedance when Q1 and Q4 are "OFF" (ϕ="L").

Although this circuit does not have the functions of analog switch, all the other functions of transmission gate are provided.

If the concept of this clocked inverter is expanded, clocked NAND and clocked NOR can be realized.

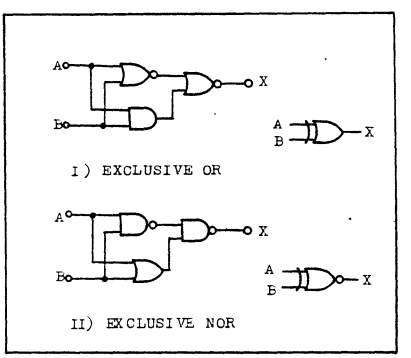


Fig. 3-4 Exclusive OR/NOR

(5) Exclusive OR/Exclusive NOR

Exclusive OR is also called coincidence circuit which gives the output of "L" when all the inputs are at "H" or "L" level and gives the output of "H" when at least one of inputs differs from others.

Exclusive NOR is the one with the inverted output of the above exclusive OR and gives the output of "H" when all the inputs coincide at "H" or "L" level.

Fig. 3-4 illustrates the configurations of these circuits.

(6) D-type flip-flop/ J-K type flip-flop

These will be explained in the chapter of Flip-Flops.

4. Maximum Ratings and Recommended Operating Conditions

4.1 Maximum ratings

The maximum ratings are specified for each C^2MOS product. Nor only for C^2MOS, the maximum ratings are the values which should not be exceeded in order to guarantee the life and the reliability of integrated circuits, and usually considered to be the absolute maximum ratings.

The absolute maximum ratings are the values which may not be exceeded even for a short instance and none of any rating values may not be exceeded When the circuits are used exceeding the maximum ratings, their characteristics may not be recovered and in extreme cases permanent damage may be resulted.

Therefore, when a circuit is designed, extreme attention should be paid to variations of supply voltages, characteristics of connected components, surges of input/output signal lines, environment temperature, etc. Table 4-1 lists the common maximum ratings of B series C^2MOS.

When the maximum ratings of each product differ from the common ratings, the former takes precedence.

Table 4-1 Common Maximum Ratings of B Series C^2MOS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS} - 0.5 ∿ V_{SS} + 20	V
Input Voltage	V_{IN}	V_{SS} - 0.5 ∿ V_{DD} + 0.5	V
Output Voltage	V_{OUT}	V_{SS} - 0.5 ∿ V_{DD} + 0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temp. Range	Tstg.	-65 ∿ 150	°C
Lead Temp./Time	Tsol.	260°C·10 sec	

(1) DC Supply voltage

This is DC supply volt age applied between V_{DD} terminal and V_{SS} terminal. Usually biased to satisfy $V_{DD} > V_{SS}$ and the reverse bias due to the undershoot of DC power supply, etc. should be limited to -0.5 volts. If higher voltage than this vlaue is given in the condition of $V_{SS} > V_{DD}$, the parasitic diode D_7 shown in Fig. 2-4 is forward biased causing excessive current to flow from V_{SS} to V_{DD} and in extreme cases, the element may be damaged.

The upper limit of 20 volts is established based on the breakdown voltages of parasitic diodes and transistors of various circuits, and the value should never be exceeded. If voltage applied exceeding the rating, CMOS device may reach to the secondary breakdown region of latch-up, etc. from the primary breakdown region. Since V_{SS} is set to GND (0 volts) in most cases, the voltage of V_{DD} terminal should be considered to be in the range of -0.5 ∿ 20 volts.

(2) Input voltage and output voltage

The electrostatic protection diodes are inserted in the input as shown in Fig. 2-3 and Fig. 2-4. These diodes are not installed to absorb the current fed from outside but installed to protect the input oxide film from

the destruction caused by electrostatic charge. Therefore, the input voltage is limited to the range that input protection diodes are not forward biased. The lower limit is V_{SS} -0.5 volts and the upper limit is V_{DD} +0.5 volts.

The output terminal is used usually to drive CMOS and other electronic components and although any voltage is not applied from outside, situations where the voltage transiently varies due to the external surge or driving of a capacitive load or an inductive load may possibly exist. If the output voltage exceeds the range of V_{SS}-V_{DD} in this case, D_4 and D_6 of Fig. 2-4 are forward biased causing excessive current to flow from the output to V_{DD} or from V_{SS} to the oupput.

As this current possibly causes primary damage of opening the output line and secondary damage of latch-up, the output voltage is similarly as the input specified as a rating to be in the range of V_{SS} - 0.5 volts - V_{DD} + 0.5 volts to prevent the parasitic diode to be forward biased.

(3) DC Input current

This item may seem to be contradictory with the rating of input voltage (2), but this indicates the critical value at which the input protection diodes and other elements will not be destroyed or degraded when voltages exceeding the ratings are applied due to surges caused by interfaces. Therefore it is not recommended to design circuits which flow DC current through the input protection diodes. Even when it can not be avoided to apply voltage causing current to flow to the input, the current should be limited to 1 mA or less.

(4) Power dissipation

As far as CMOS is used in a normal manner, the power dissipation is extremely small not causing any problems concerning the allowable loss. However, When LED is driven or big current is driven by the buffer, power is consumed in CMOS. For C^{2}MOS, the power dissipation is specified to be 300 mW* per package. (* ; Except Mini Flat Package.)

Since the power dissipation in the internal circuit can be neglected for C^2MOS in most cases comparing with that of the output stage, the power dissipation can be calculated only considering the output stage.

(5) Storage temperature range

This indicates the ambient temperature at which degradation of characteristics or reliability is not resulted even if the products are exposed in the environment for long time without applying the supply voltage. In the case of C^2MOS, the storage temperature range of -65°C ~ 150°C is specified as the rating.

(6) Lead temperature and time

These are conditions which should be limited when soldered after mounting C^2MOS on the printed circuit board. Regardless whether a solder pot is used or a soldering iron is used, the lead temperdture should be limited up to 260°C and soldering should be completed within 10 sec. When a solder pot is used, the area which is allowed to dip into solder is up to the stopper of IC lead frame.

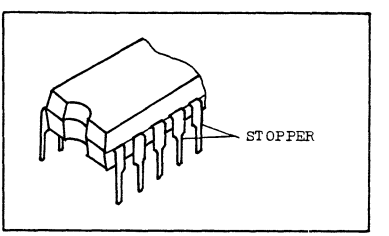


Fig.4-1 External appearance

4.2 Recommended operating conditions

These are the ranges where the operations of C^2MOS IC are guaranteed and when the ranges are exceeded the operations are not guaranteed even if such ranges are inside of the maximum ratings. Therefore, it is important to use the products inside of these ranges.

Table 4-2 Common Recommended Operating Conditions of C^2MOS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}	3	-	18	V
Input Voltage	V_{IN}	0	-	V_{DD}	V
Operating Temp. Range	Topr	-40	-	85	°C

Table 4-2 lists the common recommended operating conditions of B series C^2MOS. When the recommended operating conditions of each product differ from the common recommended operating conditions, the former takes precedence.

(1) DC supply voltage

Wide range of operating DC supply voltage, 3 volts ∿ 18 volts from V_{SS} is guaranteed for B series C^2MOS. The lower limit of 3 volts is determined by V_T of P-channel and N-channel FETs and when the voltage becomes lower than this value, V_{GS} gets so small that the normal operations of CMOS can not be expected. The upper limit of 18 volts is determined by the breakdown voltage.

(2) Operating temperature range

This is the temperature range where the normal operations and characteristics of IC are guaranteed. The operations of B series C^2MOS are guaranteed in the wide range of -40°C - 80°C.

Table 5-1 Static Electrical Characteristics of TC4001BP (V_{SS}=0V)

HARACTERISTIC	SYM-BOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
igh-Level utput Voltage	V_{OH}	$\|I_{OUT}\|$<1μA, $V_{IN}=V_{SS}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
ow-Level utput Voltage	V_{OL}	$\|I_{OUT}\|$<1μA, $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
utput igh Current	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16	-0.5	-	-0.12	-	mA
		V_{OH}=9.5V	10	-0.5	-	-0.4	-1.2	-	-0.3	-	
		V_{OH}=13.5V, $V_{IN}=V_{SS}$	15	-1.4	-	-1.2	-6.0	-	-1.0	-	
utput ow Current	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44	1.5	-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1	3.5	-	0.9	-	
		V_{OL}=1.5V, $V_{IN}=V_{SS},V_{DD}$	15	3.6	-	3.0	15	-	2.4	-	
nput igh Voltage	V_{IH}	V_{OUT}=0.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V, $\|I_{OUT}\|$<1μA	15	11.0	-	11.0	8.25	-	11.0	-	
nput ow Voltage	V_{IL}	V_{OUT}=0.5V,4.5V	5	-	1.5	-	22.5	1.5	-	1.5	
		V_{OUT}=1.0V,9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V, $\|I_{OUT}\|$<1μA	15	-	4.0	-	6.75	4.0	-	4.0	
put "H"Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
rrent "L"Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
iescent evice Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$	5	-	1.0	-	0.001	1.0	-	7.5	μA
			10	-	2.0	-	0.001	2.0	-	15	
			15	-	4.0	-	0.002	4.0	-	30	

5. Static Electrical Characteristics and Dynamic Electrical Characteristics

5.1 Static Electrical characteristics

Table 5-1 lists the static electrical characteristics of TC4001BP.

Excluding the products with special specifications, the guaranty of static electrical characteristics and the specifications are standardized, so that each characteristic of TC4001BP (QUAD 2-INPUT NOR GATE) will be explained here.

(1) High-level output voltage/low-level output voltage (V_{OH}/V_{OL})

Fig. 5-1 illustrates the test circuits of V_{OH}/V_{OL}. Each input terminal is connected to V_{SS} or V_{DD} to get the specified logic level at the output. When the output level can not be determined in the cases of counters, etc. the output logic is determined by applying pulses in advance. Since the load conditions are I_{OH}=-1μA and I_{OL}=1μA, and the measurement is taken in th region where I_{DS} of FET is extremely small, usually $V_{OH} \fallingdotseq V_{SS}$, and $V_{OL} \fallingdotseq V_{SS}$.

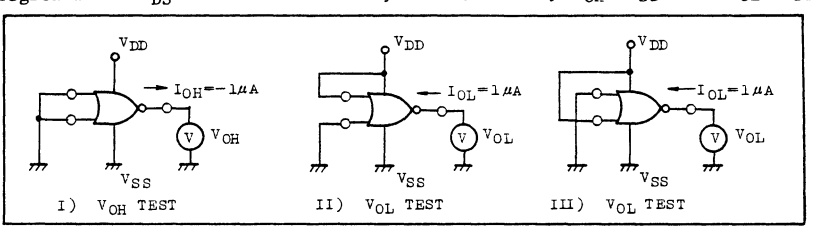


Fig. 5-1 Test Circuits of V_{OH}/V_{OL}

In the cases of interfacing CMOSs each other, the input/output conditions will be approximately equal to the above values. This fact indicated that the switching operation gives the ideal swing from V_{SS} for "L" level of logic signal to V_{DD} for "H" level in CMOS circuits.

(2) Output high current / Output low current (I_{OH}, I_{OL})

Fig. 5-2 illustrates the test circuits of I_{OH}/I_{OL}. The input conditions are set in the same manner as for measuring V_{OH}/V_{OL}. In this case, connecting a constant supply voltage to the output to be measured, the current flowing out (I_{OH}) through P-channel FET is measured for high level

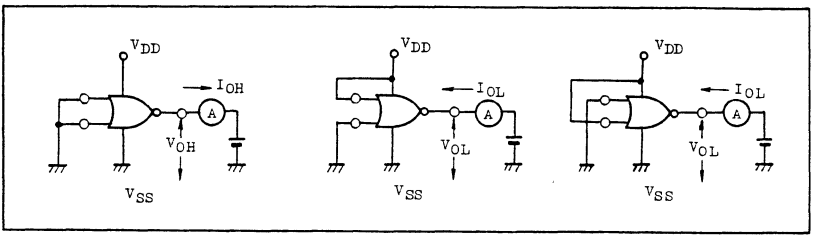


Fig. 5-2 Test Circuits of I_{OH}/I_{OL}

output and the current flowing in through N-channel FET is measured for low level output. These currents are guaranteed at one point in the non-saturation region (also called triode region) of each FET, and the minimum values are guaranteed in the specification table for both I_{OH} and I_{OL}. These can be a guidance to achieve current driving by CMOS output.

(3) Input high voltage / Input low voltage (V_{IH}/V_{IL})

Fig. 5-3 illustrates the test circuits of V_{IH}/V_{IL}. V_{IH} and V_{IL} are the voltages which can be recognized as "H" level and "L" level at the input of IC being measured, and the minimum value is guaranteed for V_{IH}

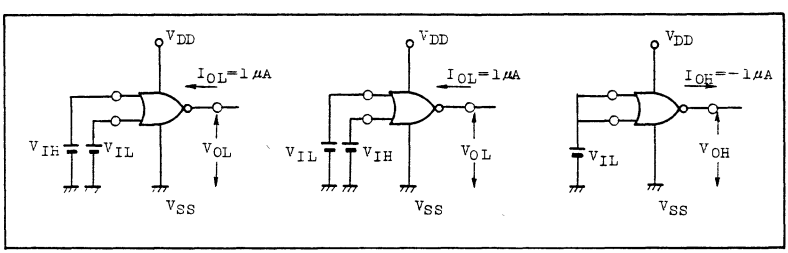


Fig. 5-3 Test Circuits of V_{IH}/V_{IL}

and the maximum value is guaranteed for V_{IL}. Whether or not IC being measured has correctly recognizes the input level is confirmed by the fact that the output level is at the specified level (higher than V_{OH} or lower than V_{OL} listed in the measurement conditions).

(4) Hihg-level input current/low-level input current (I_{IH}/I_{IL})

The input current in the range of the ratings of CMOS is considered to be the sum of the reverse current of input protection diode and the sutface leakage current. Since both of these leakage currents are extremely small at the normal temperature { $10^{-5} \sim 10^{-4}$(uA)}, the operating maximun voltage is applied for the tests. However, the specified value of ±0.3uA (maximum) is guaranteed considering stability of automatic testing. Other inputs except one being measured are usually connected to V_{SS} for testing V_{IH} and to V_{DD} for testing V_{IL}.

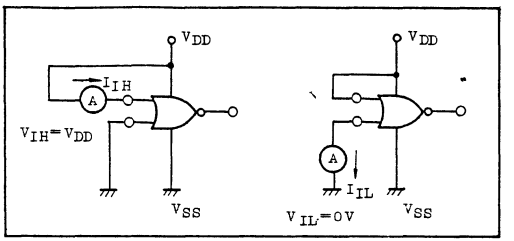


Fig. 5-4 Test Circuit of I_{IH}/I_{IL}

(5) Quiescent device current (I_{DD})

When CMOS input holds V_{DD} level or V_{SS} level, as described in the paragraph of Features of CMOS, P-channel FET or N-channel FEI is always turned off. So, the quiescent device current is total of the reverse leakage currents at PN junctions in the chip. This value is also extremely small at room temperature reaching only 1 nA (10^{-9} A) (standard value at Ta=25°C, V_{DD}=5V) for gate IC. Since this quiescent device current is guaranteed over all possible combinations of logic conditions of input pins, the combinations will be of very large number and usually such quiescent

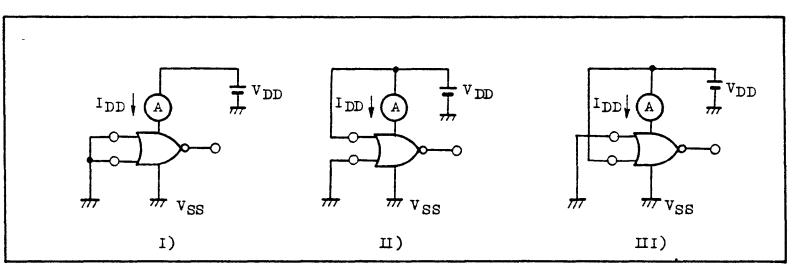


Fig. 5-5 Test Circuit of I_{DD}

device current is guaranteed at the point where the distribution is higher than the actual situations taking a certain degree of margins for test precision and test method.

Fig. 5-5 illustrates examples of test circuits of I_{DD}. Since I_{DD} with both of two inputs holding "H" can be estimated by measuring at the conditions ii) and iii), the test is omitted in many cases.

(6) 3-State output leakage current (I_{DH}/I_{DL})

This characteristic is not required for TC4001BP but it is required for the products having 3-state output and the products with open drain to specify the leakage current when the output is placed in the high impedance state.

I_{DH} is the leakage current when the signal of "H" level is applied to the OFF output and I_{DL} is the leakage current when the signal of "L" level is applied.

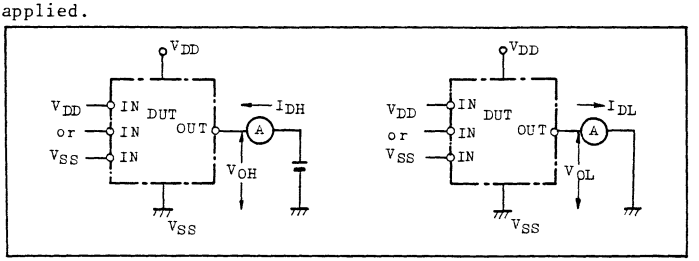


Fig. 5-6 Test Circuit of I_{DH}/I_{DL}

Fig. 5-6 illustrates the test circuits of 3-state output leakage. Naturally, the inputs are connected to generate the high impedance state at the output to be measured.

5.2 Dynamic electircal characteristics

The dynamic electrical characteristics are to guarantee the transient characteristics of C^2MOS and specified with the load capacitance of 50pF at the ambient temperature of 25°C.

As the test circuits and the test waveforms are described in the technical material for each product, only the basic characteristics are explained here comitting the detail explanations.

(1) Conditions of applying input pulse

Unless otherwise specified, pulse swinging completely from V_{SS} to V_{DD} shall be applied as the input waveform. The rise time and the fall time are the time required for the waveform to vary from 10% to 90%, and both of tr and tf are adjusted to 20ns. (Fig. 5-7)

(2) Output transition time (t_{TLH}/t_{THL})

The output transition time are the time required for the waveform swining from V_{OH} to V_{OL} to vary from 10% to 90%. (Fig. 5-8)

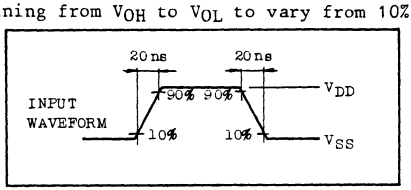


Fig. 5-7 Input Conditions

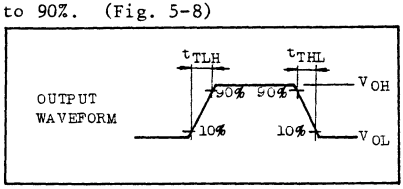


Fig. 5-8 t_{TLH}/t_{THL}

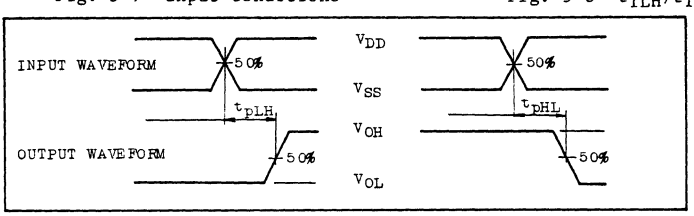


Fig. 5-9 t_{PLH}/t_{PHL}

(3) Propagation delay time (t_{PLH}/t_{PHL})

These are the propagation delays from the time when signal is given to the input of IC being measured until the output responds. The time delay from varying the input level to the output to respond varying from "L" to "H" is called t_{PLH} and on the contrary the time delay required for the output to vary from "H" to "L" is called t_{PHL}. In practice, howéver, since the circuit threshold voltage of CMOS is $1/2.V_{DD}$ (theoretical value), the time delay is specified to be the time period between

50% point of the input waveform to 50% point of the output waveform . (Fig. 5-9)

It may be easy to understand concerning the gate ICs since the measurement conditions are less complicated, but MSI has higher number of input/output terminals and the delay time is specified designating the input pins and the output pins.

(4) Minimum pulse width (tw)

The counters and the registers have the reset and the preset inputs to determine the initial state in many cases.

The minimum pulse width is the critical value of pulse width with which these terminals recognize it as the normal signal, and since the maximum value of distribution is specified, it is required to apply pulse with the width wider than the value. The pulse width is specified by the time period between 50% point of the leading edge and 50% point of the trailing edge.

(5) Maximum clock frequency (f_{CL})

This is the maximum clock frequency at which the flip-flops and the counters perform normal operations, and the minimum value of distribution is specified. It is required to design applications with the condition of the minimum value or lower of the value specified.

Unless otherwise specified, the duty cycle of clock input is 50%.

(6) Maximum clock input rise time/fall time (t_{rcL}/t_{fcL})

When the clock input waveform of a sequencial circuit, such as flip-flop or counter becomes dull, the possibility of racing or mis-counting (abnormal counting operations) arises. The critical values of t_{rcL} and t_{fcL} are specified in the catalog and the clock inputs having rise time and fall time shorter than the minimum value are required.

(7) Minimum data set-up time (t_{su})

The outputs of flip-flops and shift registers are determined by the conditions of data inputs at the time of clock input transition. Therefore, if the transitions of clock and data input occur at the same time, the output may not be definite, so that the data inputs require to be settled before the transition of clock input, and this required settling time is called minimum data set-up time.

The maximum value of distribution is specified in the catalog and it is required to keep the set-up time longer than this value for applications.

6. Cautions on Handling

By reason of its configuration, C^2MOS IC behaves itself in the manner different from Bipolar Logic centering around the conventional TTL. Although C^2MOS IC has many advantages over TTL, unsuitable method of use may result in the failure of full use of these advantages. In this chapter explanation is made on the cautions in handling C^2MOS IC and the cautions in designing circuits by using C^2MOS IC.

6.1 Configuration of C^2MOS necessary to know before handling and designing

C^2MOS IC input is connected to the gate electrode of MOS configuration having extremely thin oxide. As shown in Fig. 6-1, MOS configuration is defined in general as the sandwich configuration consisting of metal, oxide and semiconductor.

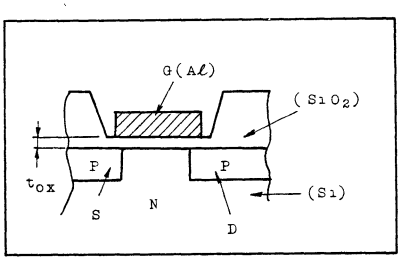


Fig. 6-1 MOS Configuration (Example of P-Channel MOS)

The thickness (tox) of oxide insulator located directly under the gate electrode is usually as thin as 0.1-0.2μ; therefore, even when the voltage of 100V-200V is applied between gate and N-substrate the electric field strength of oxide insulator just under the gate reaches as large as 10^7V/cm, causing dielectric breakdown by discharge.

For protecting the gate from the above-mentioned dielectric breakdown. TOSHIBA C^2MOS IC is provided at each input terminal with the protective circuit consisting of diode and resistor as shown in Fig. 6-2. According to the same figure, the voltage applied to the input terminal is clamped by D_1 and D_2 at V_{DD} and V_{SS}, whereby the input gate is protected. However, the input protective circuit has its limit.

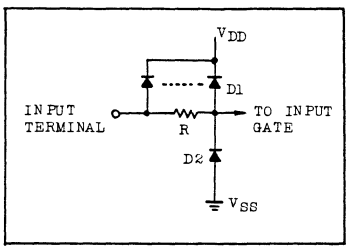


Fig. 6-2 Input Protection Circuit

As an example, the static electricity remaining in the fibers by the friction of fibers and needle of injustrical sewing machine for synthetic fibers or that generated by men and women walking on a carpet may reach several kV~~ some dozen kV, though the voltage differs depending on relative humidity and surface condition.

The above-mentioned static electricity is stored in the storing case of fibers or in human body, which is equivalent to the fact that the above-mentioned voltage is charged to the electrostatic capacity or human body capacity (200 ~ 300PF). When this electric charge discharges to C^2MOS input, it is transformed into the energy sufficient to break down C^2MOS input.

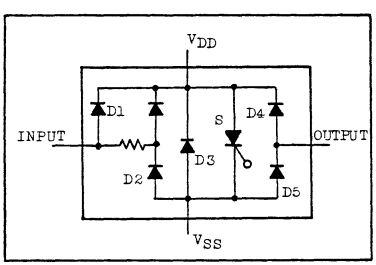


Fig.6-3 Parasitic circuit of C^2MOS IC

In addition to the input protective diode, parasitic diodes are formed between each terminal in C^2MOS IC, and all these diodes are of inverse bias at the voltage within the max. rating. However, when the voltage exceeding the max. rating is applied between each terminal, excessively large current flows to these diodes.

Fig. 6-3 shows the parasistic circuit formed between each terminal of C^2MOS IC. In same figure, D_1 and D_2 are the input protective diodes, D_3 is the diode formed by P-well diffusion, D_4 is the diode by the drain formation

of P-channel MOS FET, and D_5 is the diode by the drain formation of N-channel MOS FET. S is the parasistic thyristor formed between each diffusion area.

For example, when the voltage exceeding the range of V_{SS} - V_{DD} is applied to C^2MOS input or output and the excessively large current flows to these diodes, firstly the fusing of input and output wiring or power supply wire will occur and secondly, short-circuit phenomenon between V_{DD} - V_{SS} (this is generally called the Latch-up, resulting in fusing of power supply wire as the destruction mode) will be induced by the "ON" working of parasistic thyristor.

Therefore, it is necessary to use the voltage on input and output terminals within the rating without fail.

7. Cautions on Handling C^2MOS IC

7.1 Transportation and storing

The input and output of C^2MOS IC which is not actually installed are in the state of high impedance. It is, therefore, necessary to protect the C^2MOS IC from the external electric stress, such as the discharge from ambient charged body, the induction from space electric field, etc.

Therefore, in transporting and storing C^2MOS IC, it is necessary to use the conductive mat, metallec box, the box lined with aluminum foil, etc. so that each terminal of IC may become the same electric potential.

TOSHIBA C^2MOS IC is inserted in the conductive case or conductive mat at the time of shipment. Therefore, IC should not be removed from the case or mat with the exception of the case where the removal is required. In particular, refrain from using plastic cases or vinyl bags on which static electricity is liable to be generated.

Store the IC at the location where it is not exposed ro the direct sunlight. Pay careful attention to store at the location of the relative humidity which should be neither extremely high not extremely low.

7.2 Acceptance inspection

In case of conducting acceptance test on C^2MOS IC, first of all it is necessary to ascertain that there is no transient phenomenon as overshoot or undershoot etc. between each terminal of test system by using synchroscope. Next, conduct test by using the calibration IC for ascertaining that there is no error in the test program. In the case of giving test pulses, it is necessary to give input signal after turning on the power supply.

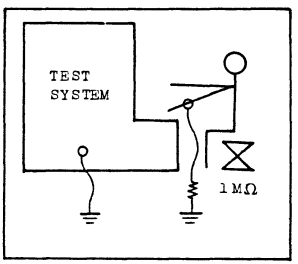


Fig. 7-1 Grounding

It is necessary to take out the IC on the grounded work table. In conducting the test, ground the test system and inspector. For preventing the electric shock accident by the electricity leak from electric equipment, ground the inspector through approx. 1MΩ resistor without fail.

Be sure to turn off the power supply when IC is inserted in IC socket or IC is drawn out of the socket. The accedent of test system may give fatal damage to IC. It is, therefore, advisable to carry out the self-diagnosic program in advance before test.

7.3 Assembling

As mentioned in 2.2, in case of installing C^2MOS IC on the printed base board, it is necessary to make protection from the static electricity by grounding electric equipment, work tables (desks), and work men. It is advisable to ground a work table by putting metal plate or aluminum foil on the surface. Refrain as practicable as possible from wearing chemical fiber work cloth. Electricity leak from electric equipment shall be prevented by reason of safety. So, it is necessary to periodically check to see that there is no leak in the electric equipment.

In case of shaping the lead frame for installing IC, it is recommended that pincette and other jigs be used for preventing the stress from being imposed on the root.
It is ideal that the jigs are grounded.

7.4 Soldering and cleaning

In case of carrying out soldering by using soldering iron and soldering tank, perform the soldering work within 10 seconds at the temperature 260°C below. It is confirmed that TOSHIBA C^2MOS IC has no problem on reliability even in case the temperature stress is given to the stopper or lead at 260°C for 10 seconds.

Use the soldering iron with no leak on its tip. It is advisable to use A class soldering iron, the dielectric resistance of which is over 10 MΩ.

In using the soldering tank, it is necessary to ground the tank for preventing the unstable electric potential. After soldering IC to a printed base board, for removing flux and others, accelerating cleaning method is adopted in many cases by using detergent and ultrasonic wave.

In this case, full attention should be given to the selection of solvent so that the cleaning may have no influence on the outer case and mark of C^2MOS IC. In general, it is advisable to use FUREON series.

In the ultrasonic cleaning, consideration should be given to the cleaning method so that the main body may form a shadow to the oscillator. This is for preventing IC and base board from the stress by resonance. At the same time, concideration should be given to the cleaning time which shall be within 30 seconds

7.5 Adjustment and test

In conducting adjustment and test of set on completion of printed base board, before turning on the power supply it is advisable to ascertain that there are no errors in polarity and others of power supply, etc. As to the printed base board, ascertain that there are no solder bridge, cracks, etc. Usually, the C^2MOS system requires only a small supply current, so that the abnormality of system can be checked, from the excessive supply current. In case of conducting test by using the commercially available constant-voltage power supply, it is recommended that the current limit be imposed on the power supply.

For the system consisting of several sheets of printed base boards, the printed base boards should be drawn out of and insert in the mother board for checking the system. In this case, the work shall be made after turning off the power supply.

In observing each part of printed base board with an oscilloscope at the time of test, it is necessary to be careful so that the tip of probe may not contact other signal wires and supply wire. In case the location to be observed is decided in advance, it is one of the methods to stand the test pin for exclusive use. Do not lead out this test pin directly from the signal wire. It is advisable to protect C^2MOS circuit from static electricity and erroneous connection by inserting over 10KΩ resistance in series.

In case of conducting test at high temperature and low temperature, it is necessary to ground the thermostatic oven. The set in the oven should be installed on the conductors.

8. Mini Flat Package (MFP) C^2MOS

8.1 Features and Applications

When compared with existing DIP, Toshiba MFP C^2MOS IC has the following features:

- o Small in size and a space factor at time of installation can be made small.
- o Installation to thin type equipment is possible
- o It is possible to assemble to both sides of a printed base board.

In addition, when compared with use of IC chip, MFP C^2MOS IC has the following features:

- o Easy to handle and reliability is improved.
- o It becomes easy to automate the assembly process.
- o Easy to replace defective parts.
- o Electrical characteristics guaranteed at the same level as DIP assure safe use.
- o Dimensions are in accordance with EIAJ General Provisions.

TOSHIBA MFP C^2MOS IC Family can be used for not only hybrid IC but also various equipment having limited printed base board area, set weight, thickness, etc. In addition, it will become possible to use MFP C^2MOS IC Family on equipment in the fields to which the application was not feasible so far.

- o Hybrid ICs
- o Portable VTRs
- o Video cameras
- o Portable measuring instruments
- o Electric/electronic instruments for motor cars
- o Small-sized business machines

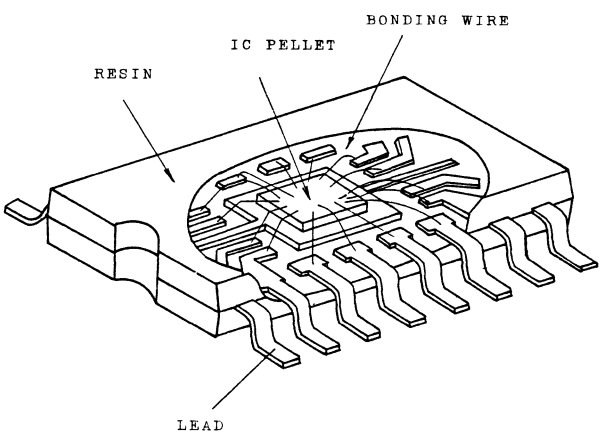
- o Hand-held computers
- o Cameras
- o Remote & radio control equipment
- o Telephones
- o Various equipment
- o Others

8.2 Structure

Shown in Fig. 8-1 is the internal structural diagram of MFP C^2MOS IC. IC chip is attached to the central section which is called the bed, and is connected to the load frame from the electrode on the chip by Au wires. The enclosure is transfer molded by epoxy resin.

The lead frame is tinned, allowing the easy soldering in installing a substrate.

Fig. 8-1 Internal Structure (In case of 16-pin IC)

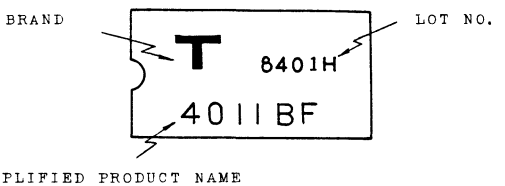


8.3 Product Name

MFP C^2MOS IC product is named in accordance with general plastic type DIP product name, but the last character (alphabet) of product name is changed from "P" of plastic to "F" of Flat.

Example: TC4011BP → TC4011BF

However, "TC" is omitted for the marking on actual ICs for the limited space. Therefore, please order ICs under formal product names as exampled in the above.



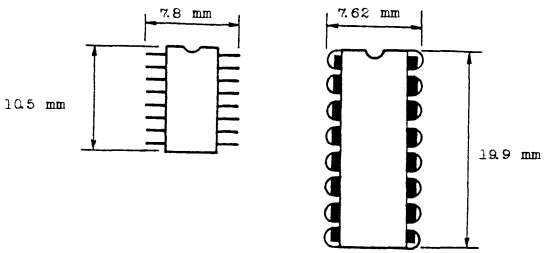
8.4 Comparison with Standard DIP (miniaturized effect)

Miniaturized effect of the mini flat package (MFP) when compared with the standard dual in-line package (DIP) is shown in Fig. 8-2.

When MFP C^2MOS IC is used, it is possible to make a printed base board small in size and light in weight to 1/2 in occupied space, 1/2.5 in height and 1/5.5 in weight.

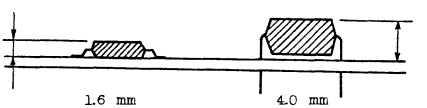
Fig. 8-2 Comparison of DIP and MFP C^2MOS IC

Occupied space (typ.) of printed base board

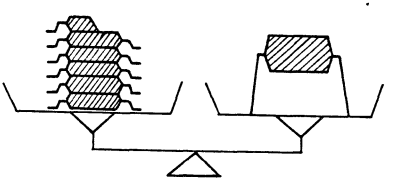


(WHEN A 1.25ϕ LAND IS USED.)

: Height (typ.)



Weight (typ.)



180 mg/IC 1000 mg

8.5 Maximum Ratings and Electrical Characteristics

(1) Maximum ratings

The maximum ratings of MFP C^2MOS IC are the same as those of ordinary DIP products except power dissipation (P_D).

(2) Electrical characteristics

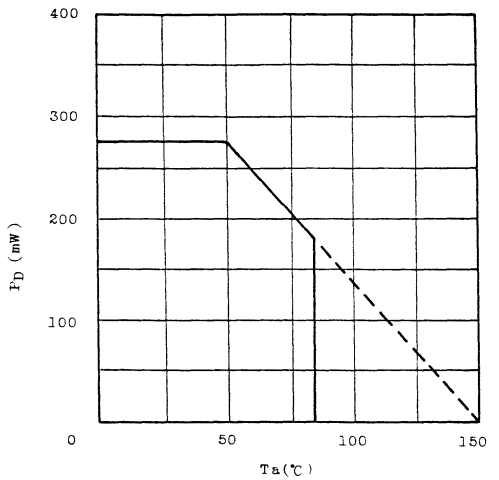
The electrical characteristics of MFP C^2MOS IC are the same as those of ordinary DIP products.

(3) Power dissipation (P_D)

The enclosure of MFP C^2MOS IC is small, and the power dissipation during the natural radiation is as less as 180 mW (at 85°C). Shown in Fig. 8-3 is the power dissipation characteristic of MFP C^2MOS IC. Since heat radiation from leads to a substrated becomes large when actually mounted, the power dissipation may be larger than that of a single unit. It is, however, necessary to examine the actual heat radiation of MFP C^2MOS IC thoroughly with it actually mounted.

However, power consumption of MFP C^2MOS IC when not in operation is minimum for its structure and even when in operation, it is possible to suppress power consumption below several tens mW unless an extermely severe method of use is employed, for instance, to drive large current by its output. Therefore, except special cases, it is considered not necessary to take much care of power dissipation.

Fig. 8-3 Power Dissipation of MFP C^2MOS IC (14/16 pins)



8.6 Mounting Method

To mount MFP C^2MOS IC, the conventional mini-mold transistor/super mini-mold transistor mounting methods can be applied. Various mounting methods are available for selective use according to purpose.

(1) Reflow soldering method

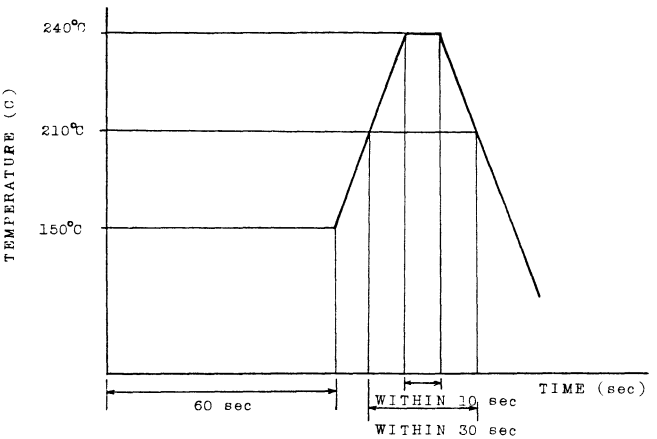
The reflow soldering method is the most general method for mouting chip components (resistor, capacitor, transistor, etc.) on a substrate and needless to say, can be applied to MFP C^2MOS IC.

In the reflow soldering, a preliminary soldering and flux are applied to a printed base board in advance. Further, a printed base board may be applied with solder paste selectively in the screen printing. In the preliminary slodering, flux may be applied to the terminal side of IC instead of a printed base with a brush or sponge.

ICs are temporarity fixed at fixed locations by flux or solder paste. If it is desirable to temporarily fix ICs more quickly, fix ICs by applying a small amount of bonding agent on their back sides.

Then, when a substrate with component parts fixed temporarily is passed over a hot plate or through a tunnel kiln, or conveyor type heater, the solder preliminary applied is melted (reflow) and the soldering is made. Effective temperature at this time is 210 to 240°C.
Fig. 8-4 shows the recommended temprature profile of the reflow soldering method.

Fig. 8-4 Recommended Temperature Profile of Reflow Soldering Method



In this case, a preheating must be carried out in order to avoid thermal strain of a substrate, etc.

(2) Method by sodering iron

A package is fixed by flux, bonding agent, etc. using a soldering iron with the thin finished tip and a thin solder of 0.5 mmφ or below. The soldering work with a soldering iron shall be performed within 10 seconds at 260°C or below.

This method is not suited to mass production but is used for experiment and repair.

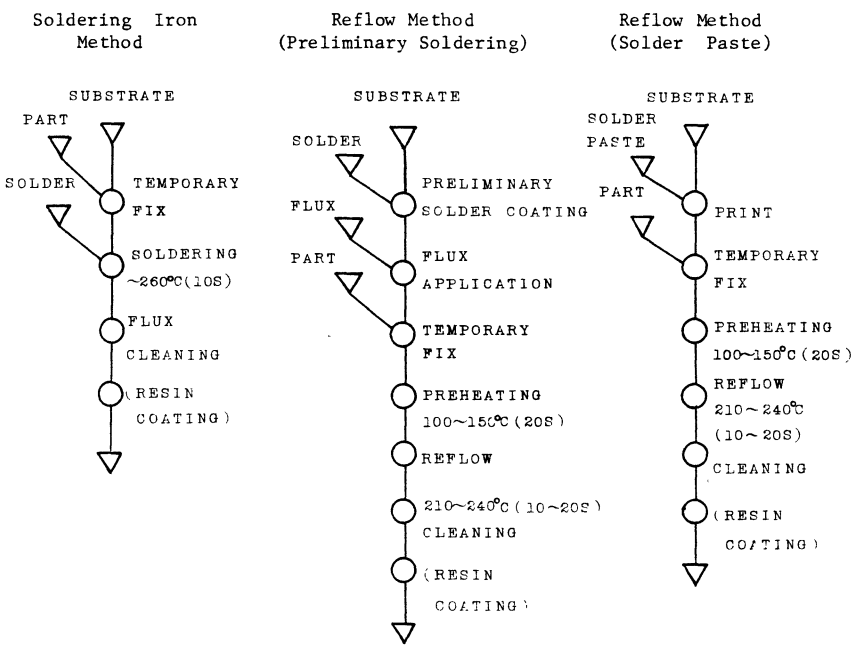
(3) Conductive paste method

This method uses conductive paste instead of solder for installing component parts.

This paste is epoxy resin with gold or silver mixed. First, apply paste to the contact section, arrange component parts and leave them for 1 to 3 hours at 100 to 150°C for curing. However, when compared with the method using solder, this method has the weakness in reliability of adhesion and therefore, it is necessary to take the utmost care.

Shown in Fig. 8-5 are examples of flowcahrts in various mounting methods.

Fig. 8-5 Various Mounting Flowcharts

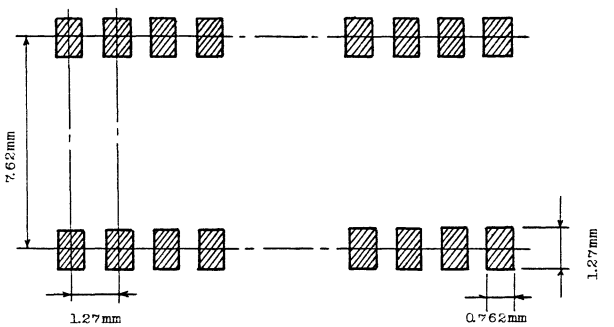


8.7 Mount Pad Dimensions (for 300 mil type)

An example of size of mount pads for MFP C^2MOS IC is shown in Fig. 8-6 for reference in designing printed base board.

This size is in accordance with EIAJ General Provisions.

Fig. 8-6 Diagram of Mount Pad Size



8.8 Cautions for Use

For effective use of MFP C^2MOS IC it is necessary not only to strictly observe instructions (handling, static electricity, etc.) for use of ordinary DIP package C^2MOS IC but also to pay attention to the following points.

(1) Tmeperature at time of soldering

IC is exposed to high temperature at time of soldering.

Basically, however, the soldering can be carried out at lead temperature 350°C for 3 sec or less in case of the soldering iron method, and at atmospheric temperatures on the resin surface 240°C for 10 sec or less and lead temperature 260°C for 10 sec or less in case of the reflow method.

However, except an unavoidable case it is desirable to use a method to complete soldering in a short time as could as possible.

(2) Type of flux and cleaning

Flux in activated resin composition is most extensively used for soldering. It is recommended to avoid use of chloric flux as reliability may be adversely affected by residual chlorine, etc. If soldering flux is left, leads may be corroded, marks on IC may become hard to be read and other troubles may be cause, and it is therefore necessary to wash and remove flux completely. It is advisable to use FUREON Series solvents for cleaning.

(3) Moisture resistance

When compared with ordinary DIP package products, MFP C^2MOS IC has a thin mold resin and a short distance between the external leads to IC chips and therefore, shows a slight difference in the marginal test of moisture resistance. Therefore, it is advisable to avoid use ICs with their surfaces exposed to air after mounted on a printed base board and to apply a moisture roof coating of liquid hard resin, etc. to ICs after mounted on a printed base board.

In case of hybrid IC which is sealed in an airtight case, no moisture proof coating is necessary. When ICs are to be sealed by resin after mounted, it is necessary to select a resin having a small coefficient of thermal expansion. It is however effective to employ a method to apply a buffer coating with a viscous resin to suppress effect of thermal expansion.

In any case, it is recommended to select sealing resins or coating materials by consuting their purposes with resin makers.

(4) Formation of leads

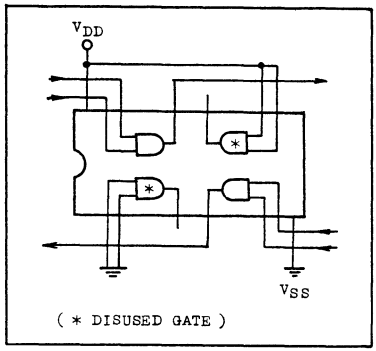
Leads of MFP C^2MOS IC are formed in the L-shape to facilitate mounting to a flat substrate. If they are straightened, their strength can be reduced.

Further, if stress is applied to leads and they are deformed during they are handled, it is more difficult to reshape them to the original shape than ordinary DIP type IC.

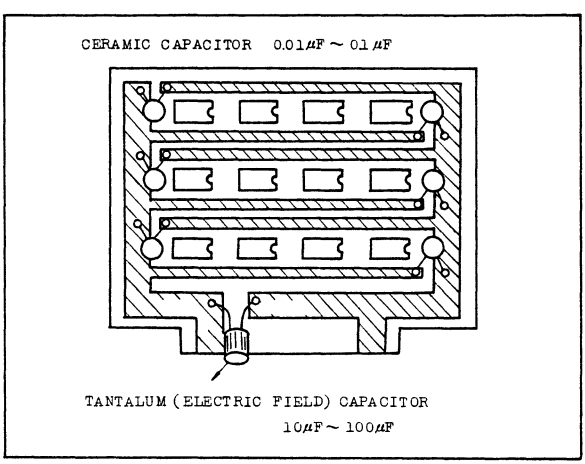
9. Cautions on Designing Circuits

9.1 Input processing

As the input of CMOS IC is very high impedance ($R_{IN} \doteqdot 10^{12}\Omega$), the logic level is not constant in the open state. In this case, if the input is in the medium level, both P-channel and N-channel transistors are in the state of connection, whereby the unnecessary supply current flows.



Therefore, be sure to connect the unnecessary input line to V_{DD}, V_{SS} or other input/output wires, for which logic level is decided, as shown in Fig. 9-1. Unstable contact of soldered parts causes erroneous working of CMOS system or increase in supply current. Therefore, care should be taken to wiring.



9.2 Designing power supply

In general, CMOS is small in current dissipation as compared with other bipolar digital IC; therefore, it can be used by the small capacity power supply. By reason of its operation, however, CMOS consumes electric power in the form of spike. This makes it necessary to make the high-frequency impedance of power supply lower. Concretely speaking, it is necessary to make supply (V_{DD}) wire and GND (V_{SS}) wire thick and short and insert 0.01μF∿0.1μF capacitor as the high-frequency filters in the inportant areas between power supply and GND on the printed base board. As to the low-frequency filter. 10μF∿100μF/printed base board will do for the purpose. Fig. 9-2 shows an example, of printed base boards.

And average supply current varies considerably depending on such factors as the working frequency, load on capacitor, supply voltage, rise and fall of input signals, etc. Therefore, particular attention is required in the case of driving by simple power supply of Zenor diode of battery driving. In case there are overshoot and undershoot at the transient time of power supply, arrangement shall be made by using filters, etc. so as to avoid exceeding the max. rating.

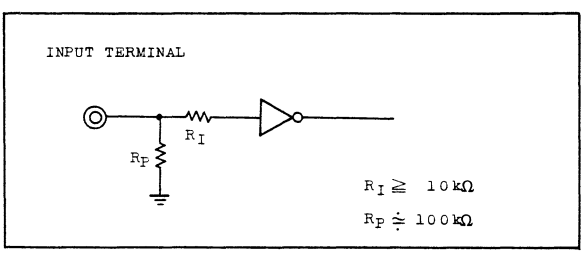


Fig.9-3 Input Processing of Printed Base Board

9.3 Input processing of printed base board

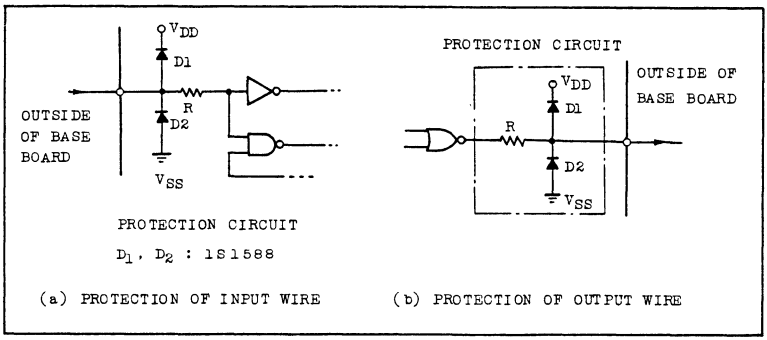


Fig.9-4 Protection of Input/Output Wires

When the input terminal of printed base board consists of C^2MOS input only, like the individual CMOS device, the input terminal is in electrically floating condition, whereby there is a possibility of receiving damage by static electricity, etc. Therefore, as shown in Fig. 9-3, by inserting over 10kΩ resistance in series in advance, it is possible to protect C^2MOS from the overcurrent.

And, it is more effective if the input terminal can be pulled up or down by approx 100kΩ resistance.

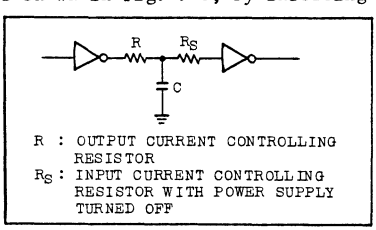


Fig.9-5 Method of Inserting Capacitor

9.4 Measures for noise and surg of signal input/output wire

In many cases the signal input wire coming in the printed base board and the control output wires coming out the printed base board are connected with other electronic parts. In general, it can be said that the signal wire is long in many cases. In case the surge is applied to these input/output wires by induction, there is a possibility of deterioration or breakdown of CMOS IC being caused by overcurrent (overvoltage). Therefore, in case the input/output signal wires are long and when the

high voltage wire exists in the outside printed base board, it is necessary to insert the protective circuit as shown in Fig.9-4. The method of separating the base board through photocoupler and lead relay contact is also effective.

In case of making test pin, it is advisable to make protection in advance as shown in Fig. 9-1 to Fig. 9-4.

9.5 Signal wire and capacitor to be connected to V_{DD} or V_{SS}

In case the capacitor is connected directly to signal wire for removing the delay and noise in signal, the capacitor up to 500pF in capacity can be connected directly, but capacitors larger in capacity shall be connected through such resistors as shown in Fig. 9-5. These resistors are used for restricting the flow of current to the parasitic circuit of CMOS input/output at the time of "ON" and "OFF" of power supply and for preventing CMOS output from short-circuiting for a long time. It can be said that 10kΩ or over will be suitable as the resistance value for both R and R_S.

9.6 Output short-circuiting

In C^2MOS IC, buffer is added to the output, whereby it is possible to carry out the current driving of both source (I_{OH}) and sink (I_{OL}). Therefore, in case "H" level output wire is short-circuited with GND (V_{SS}) wire or "L" level output wire is short-circuited with V_{DD} wire, overcurrent flows to C^2MOS output. In particular, if supply voltage is high, this current may cause the package to exceed the permissible power disipation; therefore, attention shall be given to prevention of the output short-circuit.

Of course, it is impossible to connect normal outputs together, but concerning the C^2MOS which has three-state output, wired OR is permitted under the condition that more than two-wire outputs do not come to enable simultaneously.

9.7 Influence of input slow in rise or fall time

In case the waveform slow in rise time or fall time is applied to CMOS input, the output of gate IC, etc. may tend to oscillate in the neighborhood of V_{TH} (device threshold voltage) of input waveform. This is because, in the neighborhood of V_{TH}, CMOS gate becomes equivalently linear amplification, whereby the minute supply ripples and noise appear on the output after amplification.

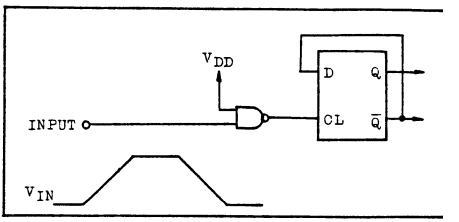


Fig.9-6 Example of Clock Input Shaped by Waveform

For suppressing the above phenomenon, consideration should be taken to insert the high-frequency filter capacitor between V_{DD} and V_{SS} of oscillating IC or to use Schmitt trigger IC. In particular, attention should be given to the clock input of sequence circuit.
Fig. 9-6 shows an example of clock shaping.

9.8 Variation of various characteristics

(1) Circuit threshold voltage

The circuit threshold voltage of C^2MOS is designed for 1/2 V_{DD} ideally, but in reality the voltage is influenced directly by the variations of both P/N FETs because the voltage is decided by the voltage dividing effect of both P/N MOS FETs. As compared with the bipolar IC, therefore, the variation is considerably large. For example, differentiation circuit/integration circuit by CR and timer circuit are greatly influenced in terms of time by this variation, and in reality compensation effect is required by the use of variable resistors.

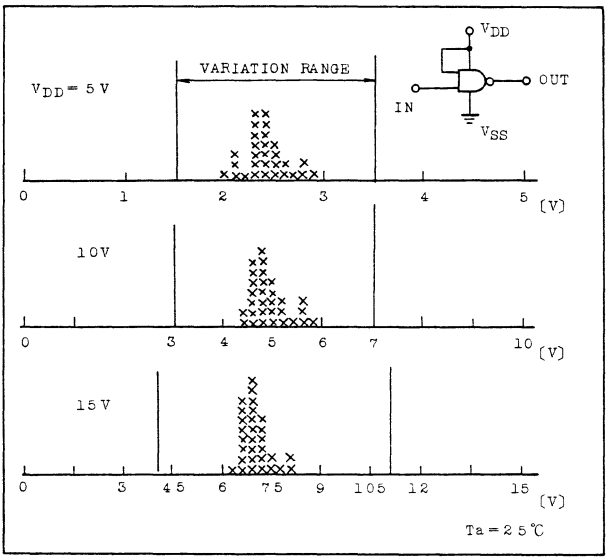


Fig.9-7 Variation Data of TC4011BP V_{TH}

Fig. 9-7 shows the variation data for TC4011BP circuit threshold voltage. As to other types, variations can be considered to be similar to TC4011BP.

(2) Output current

The variation of output current can be considered to be Max. ±30% to the standard value. Fig. 9-8 shows the output current characteristics (standard value) of TC4007UBP. So far as this figure is concened, it follows that considerable drain current flow at the domain where V_{DD} is high. However, if output current is large, internal loss of FET becomes large at the same time, resulting in lowering the thermal reliability. In reality, therefore, it is suitable to use at the non-saturation domain up to $|V_{DS}| < 1.5V$.

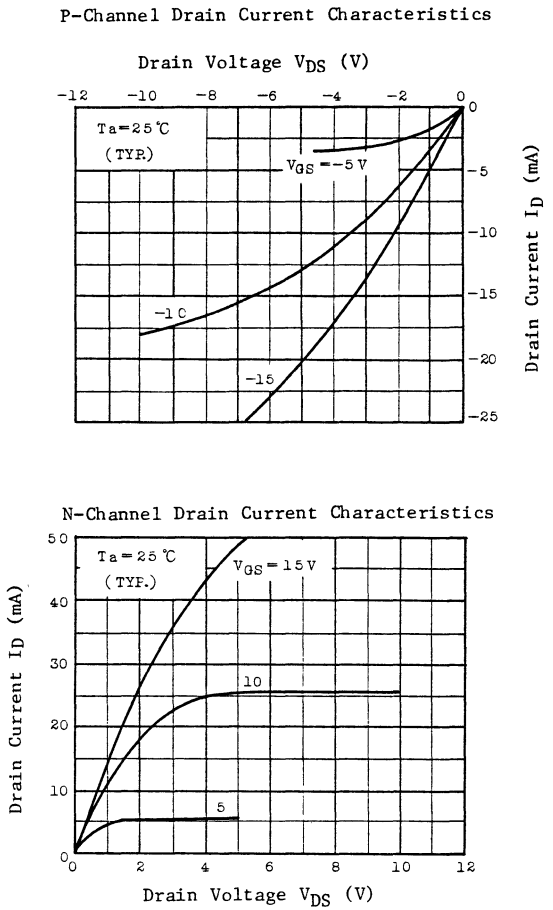


Fig. 9-8 Output Current Characteristics of TC4007UBP

(3) Switching time

Propagation delay times such as t_{PLH}, t_{PHL}, etc., toggle frequency of counter, etc. have max. ±30% variation to the standard value. However, these parameters vary depending on the interface conditions of load capacitance, etc., therefore, it is necessary to consider fanout at the portion where operating speed is high.

9.9 Temperature parameters of various characteristics

(1) Device threshold voltage

The device threshold voltage is considerably stable to the temperature because the temperature coefficients of ON resistance of P-channel and N-channel FETs become the puls values. The temperature coefficients are approx. $-2 \sim -3$ mV/°C at V_{DD}=5V and approx. $-4 \sim -5$ mV/°C at V_{DD}=10V.

(2) Output current

The output current has the minus temperature coefficients for both P/N FETs, which are approx. -0 4%/°C. Namely, under the temperature condition of approx. 85°C the current value becomes small by about 25% as compared with the normal temperature (about 25°C). This is an important point in deciding the overdrive coefficient in case of driving transistor, etc. by current.

(3) Input current, Quiescent device current and 3-state output leakage current

These leak currents are theoretically the leak currents in the opposite direction of PN junction, and are extremely small in value at normal temperature. With the rise in temperature, however, the values increase at exponential function.

In reality, it is convenient to remember that with the rise in ambient temperature by 25°C the leak current increases by about 1 digit.

Howeve, in reality the input current is approx. $10^{-10} \sim 10^{-11}$ [A] at normal temperature and the quiescent device current is approx. 10^{-9} [A] at gate IC. These are the levels which have no problems on the practical use at high temperature.

(4) Propagation delay time and max. clock frequency

As the propagation delay time may be regarded as the time for charging and discharging the internal capacitance and load capacitance of ON resistance of FET, the propagation dealy time is considered to be equivalent to the temperature coefficient of ON resistance. Therefore, the temperature coefficient becomes approx. 0.4%/°C, while, in the neighborhood of 85°C, t_{PLH} and t_{PHL} increase by approx. 25% to the normal temperature value. on the contrary, the max. clock frequency decreases by approx. 25%.

DATA SHEETS

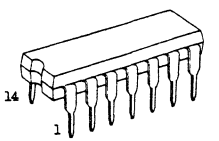
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4000BP

TC4000BP DUAL 3-INPUT NOR GATE PLUS INVERTER

The TC4000BP is a combined gate which contains dual 3-input positive NOR gate plus inverter in one package.

Since all the outputs of this gate are provided with the buffers of inverters, the input/output transmission characteristics have been improved and the noise immunity has been elevated, Thus, an increase inpropagation delay time caused by an increase in load capacity is kept to a minimum.

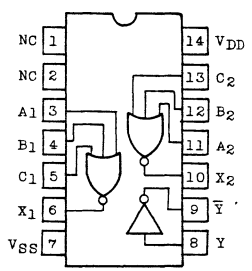


DIP 14(3D14A-P)

MAXIMUM RATINGS

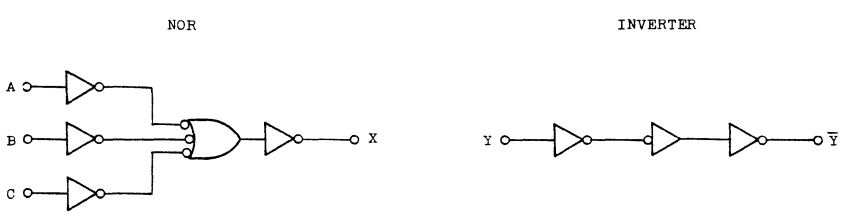
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Ambient Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TC4000BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

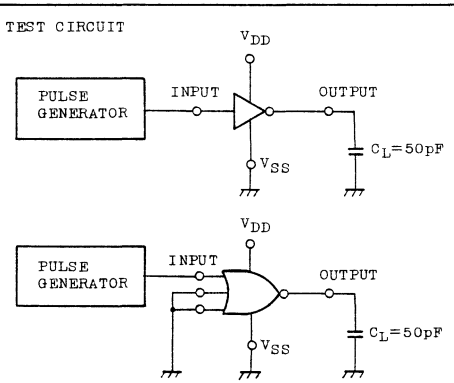
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$, $V_{IN}=V_{SS}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$, $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V,4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V,9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\| < 1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V,4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V,9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\| < 1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	0.25	-	0.001	0.25	-	7.5	μA
			10	-	0.5	-	0.001	0.5	-	15	
			15	-	1.0	-	0.002	1.0	-	30	

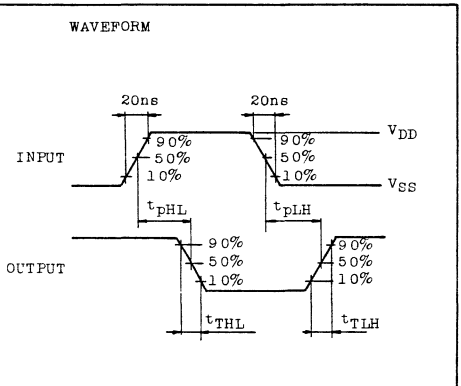
* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

	CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
	Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
				10	-	50	100	
				15	-	40	80	
	Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
				10	-	50	100	
				15	-	40	80	
INVERTER	Propagation Delay Time (Low to High)	t_{pLH}		5	-	90	180	ns
				10	-	50	100	
				15	-	40	80	
	Propagation Delay Time (High to Low)	t_{pHL}		5	-	90	180	
				10	-	50	100	
				15	-	40	80	
NOR	Propagation Delay Time (Low to High)	t_{pLH}		5	-	100	200	ns
				10	-	50	100	
				15	-	40	80	
	Propagation Delay Time (High to Low)	t_{pHL}		5	-	100	200	
				10	-	50	100	
				15	-	40	80	
	Input Capacitance	C_{IN}			-	5	7.5	pF

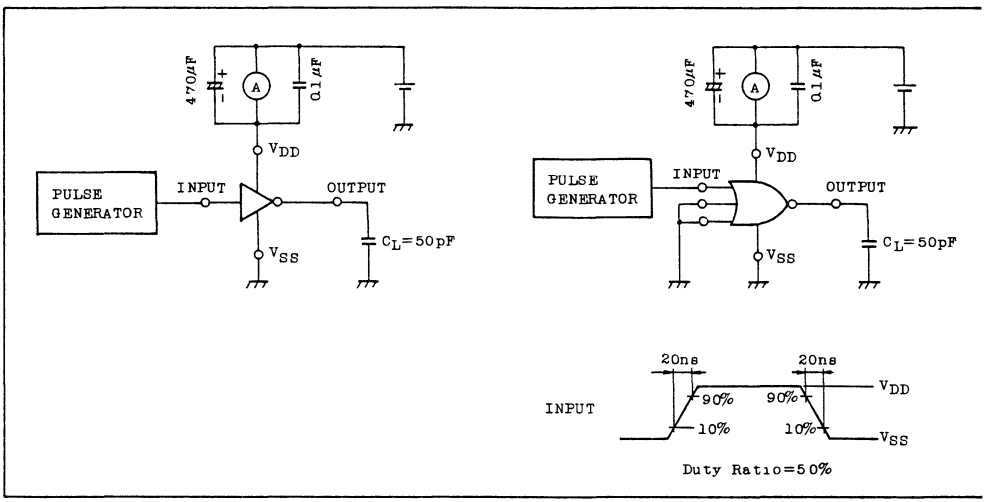
CIRCUITS AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



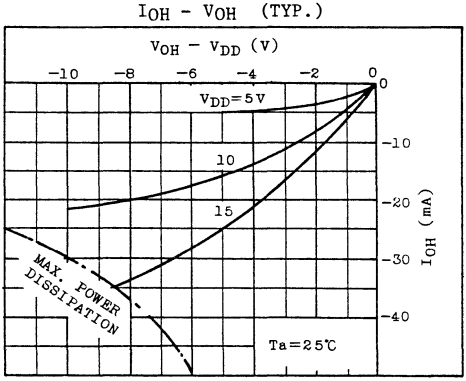


TC4000BP

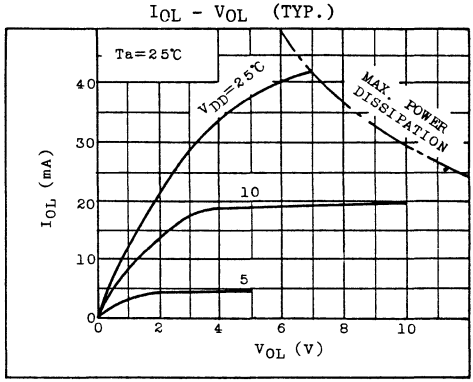
OPERATING SUPPLY CURRENT TEST CIRCUIT



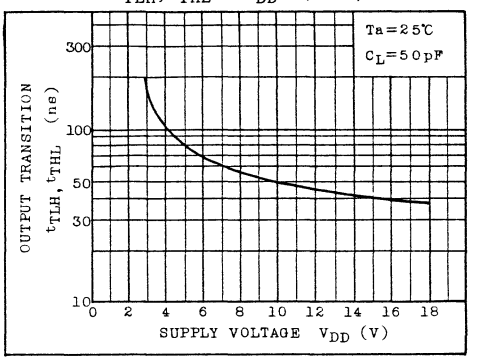
I_{OH} - V_{OH} (TYP.)



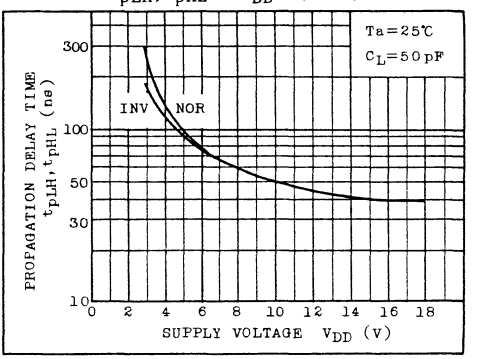
I_{OL} - V_{OL} (TYP.)



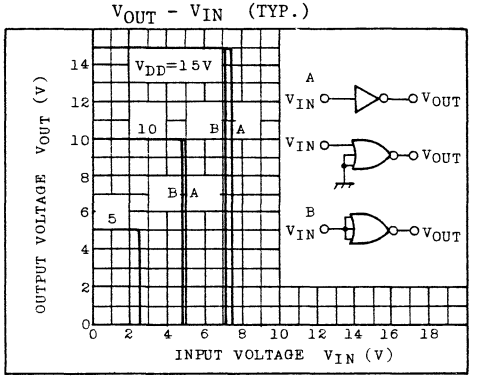
t_{TLH}, t_{THL} - V_{DD} (TYP.)



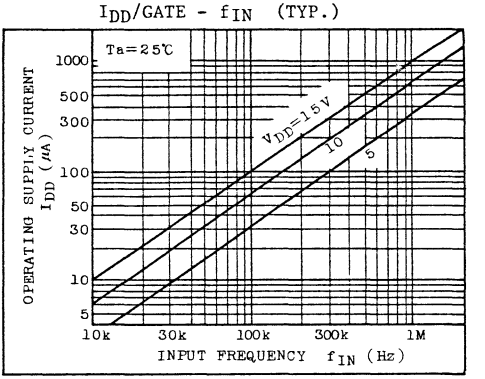
t_{pLH}, t_{pHL} - V_{DD} (TYP.)



V_{OUT} - V_{IN} (TYP.)



I_{DD}/GATE - f_{IN} (TYP.)



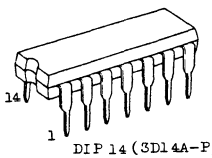
TC4001BP/BF, TC4002BP/BF TC4025BP/BF

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

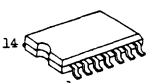
TC4001BP/TC4001BF QUAD 2 INPUT NOR GATE
TC4002BP/TC4002BF DUAL 4 INPUT NOR GATE
TC4025BP/TC4025BF TRIPLE 3 INPUT NOR GATE

The TC4001BP/BF, the TC4025BP/BF and TC4002BP/BF are 2-input, 3-input, 4-input positive NOR gate, respectively.

Since the outputs of these gates are equipped with the buffers, the input/output transmission characteristics have been improved and the variation of transmission time due to an increase in the load capacity is kept minimum.



DIP 14 (3D14A-P)

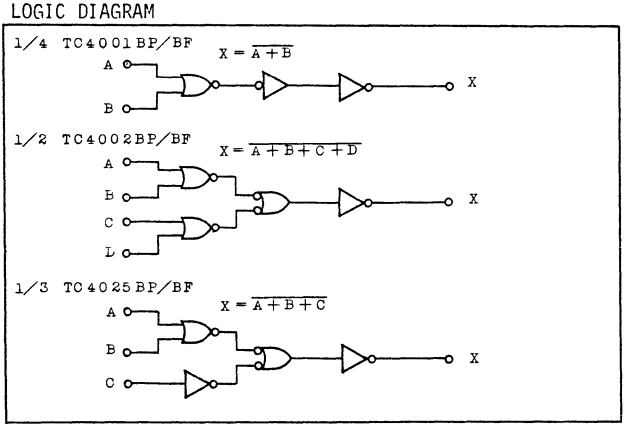


MFP 14 (F14GB-P)

ABSOLUTE MAXIMUM RATINGS

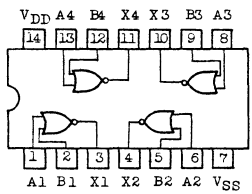
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

LOGIC DIAGRAM

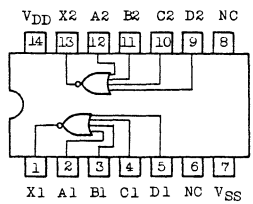


PIN ASSIGNMENT (TOP VIEW)

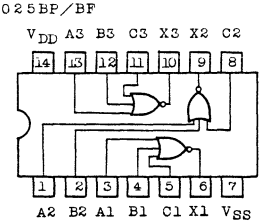
TC4001BP/BF



TC4002BP/BF



TC4025BP/BF



TC4001BP/BF, TC4002BP/BF, TC4025BP/BF

ECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
C Supply Voltage	V_{DD}		3	-	18	V
nput Voltage	V_{IN}		0	-	V_{DD}	V

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

HARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
igh-Level utput Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS}$, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
ow-Level utput Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS}$, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
)utput High Current (TC4002BP/BF)	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS}$									
)utput Low Current (TC4002BP/BF)	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
)utput High Current (TC4001BP/BF), (TC4025BP/BF)	I_{OH}	V_{OH}=4.6V	5	-2.0	-	-0.16		-	-0.21	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V	15	-1.4	-	-1.2		-	-1.0	-	
		$V_{IN}=V_{SS}$									
)utput Low Current (TC4001BP/BF), (TC4025BP/BF)	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}	5	-	0.25	-	0.001	0.25	-	7.5	μA
			10	-	0.5	-	0.001	0.5	-	15	
		*	15	-	1.0	-	0.002	1.0	-	30	

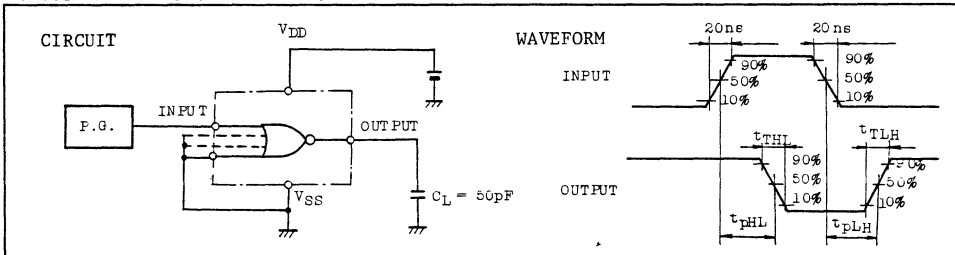
* All valid input combinations.

TC4001BP/BF, TC4002BP/BF, TC4025BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTICS	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (TC4002BP/BF)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (TC4002BP/BF)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Output Transition Time (TC4001BP/BF), (TC4025BP/BF)	t_{TLH}		5	-	130	400	
			10	-	65	200	
			15	-	50	160	
Output Transition Time (TC4001BP/BF), (TC4025BP/BF)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (TC4001BP/BF)	t_{pLH}		5	-	170	300	
			10	-	70	150	
			15	-	60	125	
Propagation Delay Time (TC4001BP/BF)	t_{pHL}		5	-	130	250	
			10	-	60	125	
			15	-	45	100	
Propagation Delay Time (TC4002BP/BF)	t_{pLH}		5	-	100	250	
			10	-	40	120	
			15	-	30	90	
Propagation Delay Time (TC4002BP/BF)	t_{pHL}		5	-	100	250	
			10	-	40	120	
			15	-	30	90	
Propagation Delay Time (TC4025BP/BF)	t_{pLH}		5	-	220	400	
			10	-	100	200	
			15	-	80	160	
Propagation Delay Time (TC4025BP/BF)	t_{pHL}		5	-	160	350	
			10	-	80	175	
			15	-	65	125	
Input Capacitance	C_{IN}			-	5	7.5	pF

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



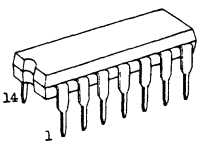
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4001UBP
TC4011UBP

C4001UBP QUAD 2 INPUT NOR GATE
C4011UBP QUAD 2 INPUT NAND GATE

TC4001UBP and TC4011UBP are 2 input NOR gate and input NAND gate respectively. The pin connections re same as TC4001B and TC4011B but the internal ircuits consist of only basic NAND (NOR) circuit ithout the waveform shaping inverters.

herefore, these are suitable for the applications n linear circuits such as oscillator circuits and mplifier circuits, and these have advantage in the pplications of logical processing systems with aster operating speed.



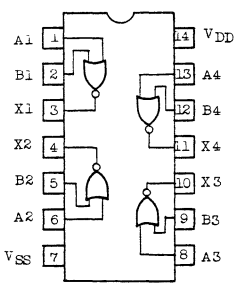
DIP14(3D14A-P)

ABSOLUTE MAXIMUM RATINGS

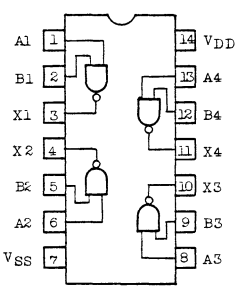
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT

TC4001UBP



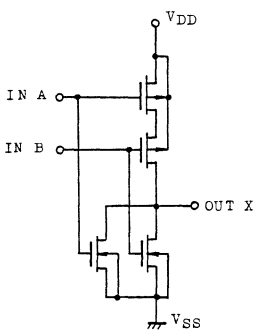
TC4011UBP



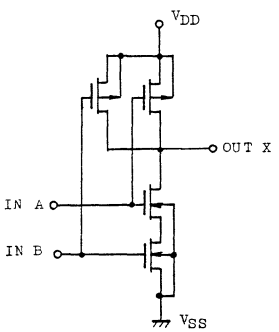
(TOP VIEW)

LOGIC DIAGRAM

1/4 TC4001UBP



1/4 TC4011UBP



TC4001UBP, TC4011UBP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
		V_{IN}=V_{SS}, V_{DD}	15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
		V_{IN}=V_{SS}, V_{DD}	15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	mA
		V_{OH}=2.5V	5	-	-	-		-	-	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V	15	-1.4	-	-1.2		-	-1.0	-	
		V_{IN}=V_{SS}, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
		V_{IN}=V_{SS}, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	4.0	-	4.0	3.0	-	4.0	-	V
		V_{OUT}=1.0V, 9.0V	10	8.0	-	8.0	6.5	-	8.0	-	
		V_{OUT}=1.5V,13.5V	15	12.0	-	12.0	9.5	-	12.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.0	1.0	-	1.0	
		V_{OUT}=1.0V, 9.0V	10	-	2.0	-	3.5	2.0	-	2.0	
		V_{OUT}=1.5V,13.5V	15	-	3.0	-	5.5	3.0	-	3.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD}	5	-	1.0	-	0.001	1.0	-	7.5	
			10	-	2.0	-	0.001	2.0	-	15	
		*	15	-	4.0	-	0.002	4.0	-	30	

* All valid input combinations

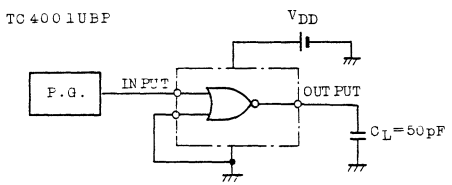
TC4001UBP, TC4011UBP

'NAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

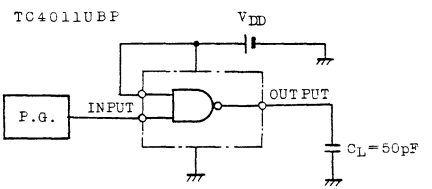
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
ıtput Transition Time (Low to High)	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
ıtput Transition Time (High to Low)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
ropagation Delay Time (TC4001UBP)	t_{pLH}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
ropagation Delay Time (TC4001UBP)	t_{pHL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
ropagation Delay Time (TC4011UBP)	t_{pLH}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
ropagation Delay Time (TC4011UBP)	t_{pHL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
nput Capacitance	C_{IN}			-	5	7.5	pF

IRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTIC

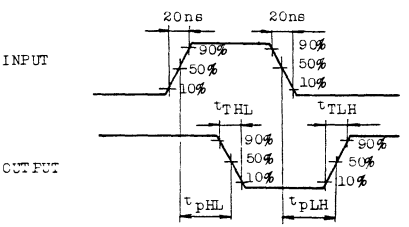
CIRCUIT 1



CIRCUIT 2



WAVEFORM

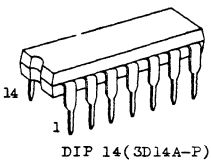


TC4006BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4006BP 18-STAGE STATIC SHIFT REGISTER

TC4006BP is static shift register of 18 bits maximum which consists of two 4 bit shift registers and two 5 bit shift registers, and the clock is supplied from the common $\overline{CLOCK}$ input for all the shift registers, Since 5 bit shift register is provided with 4 bit output D_n+4 in addition to serial data output D_n+5, the shift register with arbitrary number of stages of 4,5,8,9,10,12,13,14,16,17 and 18 can be obtained by the combination of inputs and outputs of 4 bit and 5 bit shift registers.
Each register is shifted by the falling edge of $\overline{CLOCK}$.

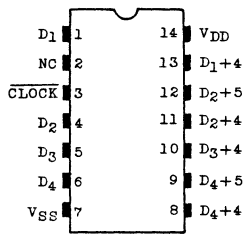


DIP 14(3D14A-P)

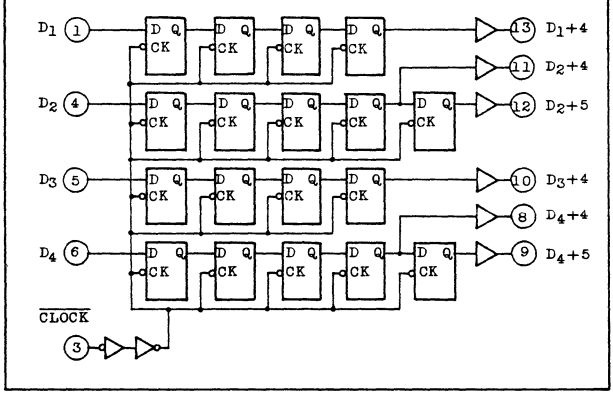
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Ambient Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGMENT



LOGIC DIAGRAM



TRUTH TABLE (SINGLE STAGE)

INPUTS		OUTPUT
D_n	$\overline{CLOCK}$	D_n+1
L	↓	L
H	↓	H
*	↓	D_n

* Don't care

COMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
ɔut Voltage	V_{IN}		0	-	V_{DD}	V

ATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

HARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
gh-Level tput Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
w-Level tput Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
tput High rrent	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
tput Low rrent	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
put High ltage	V_{IH}	V_{OUT}=0.5V,4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V,9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
put Low ltage	V_{IL}	V_{OUT}=0.5V,4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V,9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
put "H" Level rrent	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
iescent Device rrent	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

All valid input combinations.

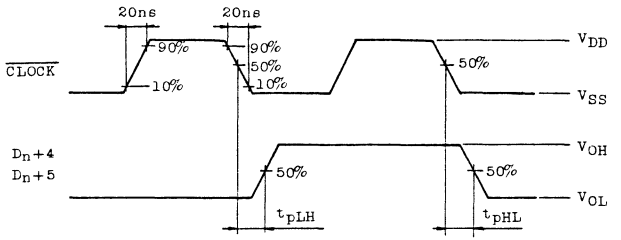
TC4006BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

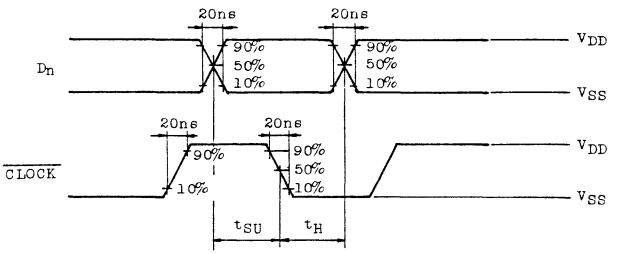
CHARACTERISTIC	SYMBOL	TEST CONDITION V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}	5	-	80	200	ns
		10	-	50	100	
		15	-	40	80	
Output Transition Time (High to Low)	t_{THL}	5	-	80	200	
		10	-	50	100	
		15	-	40	80	
Propagation Delay Time	t_{pLH} t_{pHL}	5	-	170	400	ns
		10	-	75	200	
		15	-	65	160	
Max. Clock Frequency	f_{CL}	5	2.5	8	-	MHz
		10	5	17	-	
		15	7	20	-	
Min. Clock Pulse Width	t_w	5	-	60	180	ns
		10	-	30	80	
		15	-	25	50	
Max. Clock Rise Time Max. Clock Fall Time	t_{rCL} t_{fCL}	5	20	-	-	μs
		10	2.5	-	-	
		15	1.0	-	-	
Min. Set-up Time (DATA - $\overline{CLOCK}$)	t_{SU}	5	-	20	100	ns
		10	-	8	50	
		15	-	5	40	
Min. Hold Time (DATA - $\overline{CLOCK}$)	t_H	5	-	-2	60	ns
		10	-	4	40	
		15	-	5	30	
Input Capacitance	C_{IN}		-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1.



WAVEFORM 2.

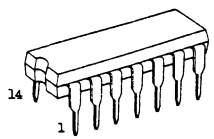


TC4007UBP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4007UBP DUAL COMPLEMENTARY PAIR PLUS INVERTER

TC4007UBP contains three elements of P-channel enhancement type MOS FET and three elements of N-channel enhancement type MOS FET. One pair of P-channel and N-channel functions as inverter and remaining two pairs provide the respective outputs of source and drain separately. Depending on how connections are made, the versatile applications such as inverter, waveform shaping circuits, NAND(NOR) gatys, linear amplifiers, clocked gates, transmission gates and high fan-out buffers are easily obtainable.



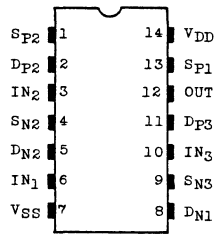
DIP 14(3D14A-P)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage *	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Ambient Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

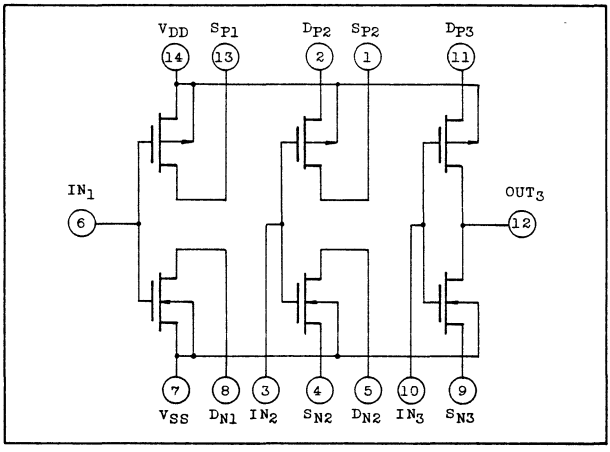
* Applicable for D_P, D_N, S_P, S_N and OUT terminals.

PIN ASSIGMENT



(TOP VIEW)

LOGIC DIAGRAM



ECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C Supply Voltage	V_{DD}		3	-	18	V
nput Voltage	V_{IN}		0	-	V_{DD}	V

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
ligh-Level utput Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
ow-Level utput Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
utput High urrent	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS}$									
utput Low urrent	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V	5	4.0	-	4.0	3.0	-	4.0	-	V
		V_{OUT}=1.0V	10	8.0	-	8.0	6.5	-	8.0	-	
		V_{OUT}=1.5V	15	12.0	-	12.0	9.5	-	12.0	-	
		$\|I_{OUT}\| < 1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-	3.0	1.0	-	1.0	
		V_{OUT}=9.0V	10	-	2.0	-	3.5	2.0	-	2.0	
		V_{OUT}=13.5V	15	-	3.0	-	5.5	3.0	-	3.0	
		$\|I_{OUT}\| < 1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}, V_{DD}$ *	5	-	0.25	-	0.001	0.25	-	7.5	μA
			10	-	0.5	-	0.001	0.5	-	15	
			15	-	1.0	-	0.002	1.0	-	30	

* All valid input combinations.

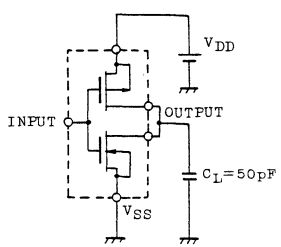
TC4007UBP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF, INVERTER)

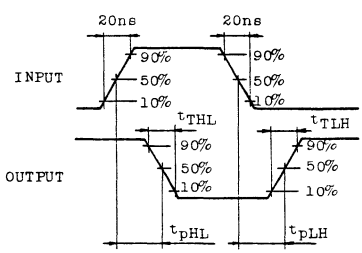
CHARACTERISTIC	SYMBOL	TEST CONDITION V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}	5	-	80	200	ns
		10	-	50	100	
		15	-	40	80	
Output Transition Time (High to Low)	t_{THL}	5	-	80	200	
		10	-	50	100	
		15	-	40	80	
Propagation Delay Time (Low to High)	t_{pLH}	5	-	55	110	ns
		10	-	25	60	
		15	-	20	50	
Propagation Delay Time (High to Low)	t_{pHL}	5	-	40	110	
		10	-	20	60	
		15	-	15	50	
Input Capacitance	C_{IN}		-	5	7.5	pF

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

TEST CIRCUIT

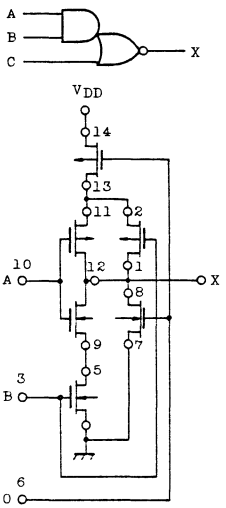


WAVEFORM

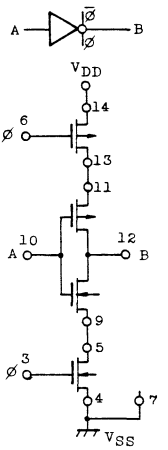


YPICAL APPLICATION

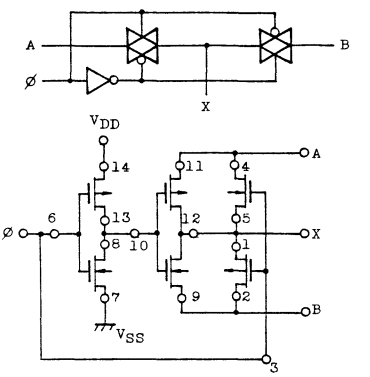
1. TREE LOGIC



2. CLOCKED INVERTER



3. ANALOG DATA SELECTOR

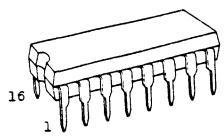


TC4008BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4008BP 4-BIT FULL ADDER

TC4008BP is full adder of 4 bit parallel processing type equipped with high speed parallel carry circuit. The sum of binary inputs applied to four augend data input lines (A_1-A_4), four addend data input lines (B_1-B_4) and carry input (C_{IN}) from the lower order is obtained in binary code from added data output (S_1-S_4) and carry output (C_{OUT}) to the higher order. Adders of 4 × n bits with cascade connections and add/substract circuits with simple external circuits can be easily obtained.

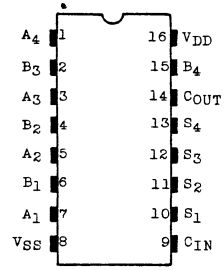


DIP 16(3D16A-P)

MAXIMUM RATINGS

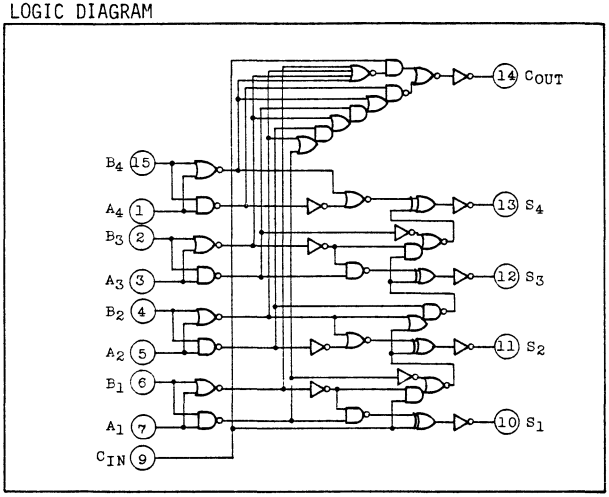
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Ambient Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT

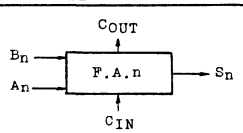


(TOP VIEW)

LOGIC DIAGRAM



TRUTH TABLE



INPUTS			OUTPUTS	
B_n	A_n	C_{IN}	S_n	C_{OUT}
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

TC4008BP

ECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C Supply Voltage	V_{DD}		3	-	18	V
nput Voltage	V_{IN}		0	-	V_{DD}	V

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
igh-Level utput Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
ow-Level utput Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
utput High urrent	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
utput Low urrent	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
nput High oltage	V_{IH}	V_{OUT}=0.5V,4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V,9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\| < 1\mu A$									
nput Low oltage	V_{IL}	V_{OUT}=0.5V,4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V,9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\| < 1\mu A$									
nput urrent "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
nput urrent "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
uiescent evice Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

All valid input combinations.

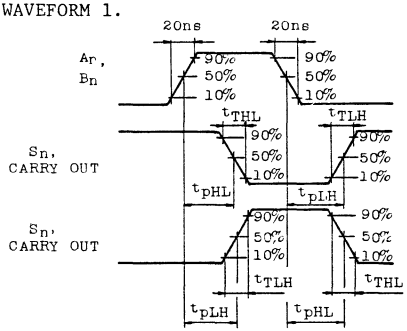
TC4008BP

DYNAMIC ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{SS}=0V, C_L=50pF)

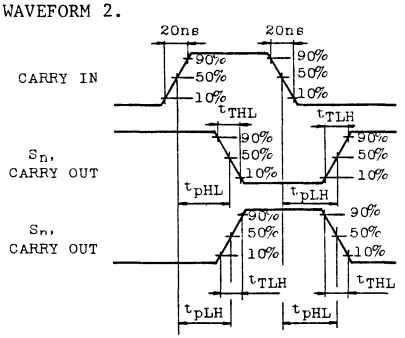
CHARACTERISTIC	SYMBOL	TEST CONDITION V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}	5	-	80	200	ns
		10	-	50	100	
		15	-	40	80	
Output Transition Time (High to Low)	t_{THL}	5	-	80	200	
		10	-	50	100	
		15	-	40	80	
Propagation Dealy Time (A_n,B_n - S_n)	t_{pLH} t_{pHL}	5	-	300	800	ns
		10	-	120	320	
		15	-	80	230	
Propagation Delay Time (A_n,B_n - CARRY OUT)	t_{pLH} t_{pHL}	5	-	270	540	ns
		10	-	110	220	
		15	-	75	150	
Propagation Delay Time (CARRY IN - S_n)	t_{pLH} t_{pHL}	5	-	260	740	ns
		10	-	100	310	
		15	-	70	230	
Propagation Delay Time (CARRY IN - CARRY OUT)	t_{pLH} t_{pHL}	5	-	120	240	ns
		10	-	50	100	
		15	-	40	80	
Input Capacitance	C_{IN}		-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1.



WAVEFORM 2.

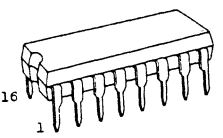


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4009UBP
TC4010BP

·009UBP HEX BUFFER/CONVERTER (INVERTING TYPE)
·010BP HEX BUFFER/CONVERTER (NON-INVERTING TYPE)

·009UBP and TC4010BP contain six circuits of buffers
:h the level shift function. TC4009UBP provides
'erted outputs and TC4010BP provides non-inverted
:puts. Large output current enables to directly
.ve one TTL/MDTL input. Furthermore, since the
;ical amplitude of V_{DD}-V_{SS} can be converted to the
;ical amplitude of V_{CC}-V_{SS} by supplying two separate
/er supplies with the condition of ($V_{DD} > V_{CC}$), these
: suitable for the interface from C²MOS system
:rating with the power supply voltage of 5 volts or
;her to TTL/MDTL system.



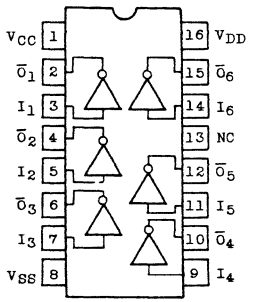
DIP 16(3D16A-P)

(IMUM RATINGS

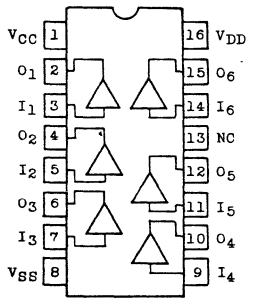
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
	V_{CC}	V_{SS}-0.5 ~ V_{DD}+0.5	V
›ut Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
tput Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{CC}+0.5	V
Input Current	I_{IN}	±10	mA
ver Dissipation	P_D	300	mW
erating Ambient mperature Range	T_A	-40 ~ 85	°C
orage Temperature nge	T_{stg}	-65 ~ 150	°C
ad Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT

TC4009UBP



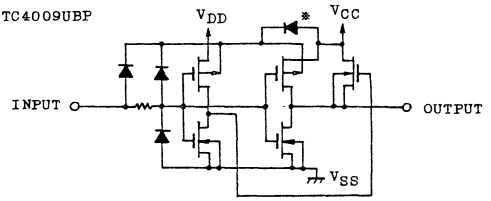
TC4010BP



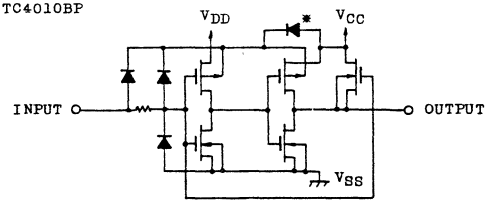
(TOP VIEW)

RCUIT DIAGRAM

1/6 TC4009UBP



1/6 TC4010BP



* Parasitic Diode

TC4009UBP, TC4010BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNI
DC Supply Voltage	V_{DD}		3	-	18	V
	V_{CC}		3	-	V_{DD}	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V, V_{DD}=V_{CC})

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UN
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.73	-	-0.65	-1.2	-	-0.58	-	mA
		V_{OH}=2.5V	5	-2.4	-	-2.1	-4.5	-	-1.9	-	
		V_{OH}=9.5V	10	-1.8	-	-1.65	-2.8	-	-1.35	-	
		V_{OH}=13.5V	15	-4.8	-	-4.3	-11	-	-3.5	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	3.8	-	3.2	7	-	2.9	-	
		V_{OL}=0.5V	10	9.6	-	8.0	13	-	6.6	-	
		V_{OL}=1.5V	15	25.0	-	24.0	47	-	20.0	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage (TC4009UBP)	V_{IH}	V_{OUT}=0.5V	5	4.0	-	4.0	2.5	-	4.0	-	
		V_{OUT}=1.0V	10	8.0	-	8.0	5.0	-	8.0	-	
		V_{OUT}=1.5V	15	12.0	-	12.0	7.5	-	12.0	-	
		$\|I_{OUT}\|<1\mu A$									
Input Low Voltage (TC4009UBP)	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-	1.7	1.0	-	1.0	V
		V_{OUT}=9.0V	10	-	1.5	-	2.3	1.5	-	1.5	
		V_{OUT}=13.5V	15	-	1.5	-	2.5	1.5	-	1.5	
		$\|I_{OUT}\|<1\mu A$									
Input High Voltage (TC4010BP)	V_{IH}	V_{OUT}=4.5V	5	3.5	-	3.5	2.75	-	3.5	-	
		V_{OUT}=9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									

TC4009UBP, TC4010BP

TIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V, V_{DD}=V_{CC})

ARACTERISTIC		SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
ut Low tage 4010BP)		V_{IL}	V_{OUT}=0.5V	5	-	1.5	-	2.25	1.5	-	1.5	V
			V_{OUT}=1.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
ut rent	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
escent Device rent		I_{DD}	**	5	-	1.0	-	0.002	1.0	-	30	μA
			V_{IN}=V_{SS},V_{DD}	10	-	2.0	-	0.004	2.0	-	60	
			*	15	-	4.0	-	0.008	4.0	-	120	

ll valid input combination. ** Include I_{CC}.

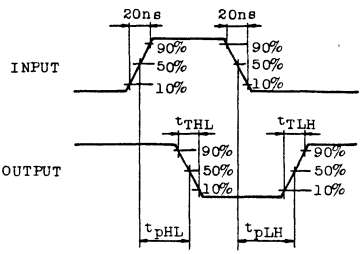
NAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF, V_{DD}=V_{CC})

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
put Transition Time w to High)	t_{TLH}		5	-	75	350	ns
			10	-	30	150	
			15	-	20	110	
put Transition Time gh to Low)	t_{THL}		5	-	25	70	
			10	-	15	40	
			15	-	12	30	
Propagation Delay Time (Low to High)	t_{pLH}		5	-	40	140	ns
			10	-	25	80	
			15	-	15	60	
Propagation Delay Time (High to Low)	t_{pHL}		5	-	25	60	
			10	-	15	40	
			15	-	15	30	
Propagation Delay Time (Low to High)	t_{pLH}		5	-	45	200	ns
			10	-	25	100	
			15	-	15	70	
Propagation Delay Time (High to Low)	t_{pHL}		5	-	50	130	
			10	-	25	70	
			15	-	15	50	
put Capacitance	C_{IN}	TC4009UBP		-	15	22.5	pF
		TC4010BP		-	5	7.5	

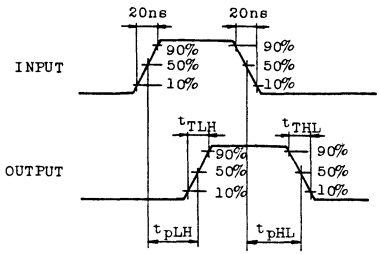
TC4009UBP, TC4010BP

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

TC4009UBP



TC4010BP



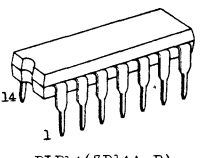
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4011BP/BF, TC4012BP/BF TC4023BP/BF

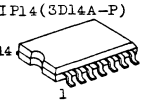
4011BP/TC4011BF QUAD 2 INPUT NAND GATE
4012BP/TC4012BF DUAL 4 INPUT NAND GATE
4023BP/TC4023BF TRIPLE 3 INPUT NAND GATE

The TC4011BP/BF, TC4023BP/BF, and TC4012BP/BF are input, 3-input, and 4-input positive logic NAND tes respectively.

nce all the outputs of these gates are provided th the inverters as buffers, the input/output aracteristics have been improved and the variation propagation delay time due to the increase in load pacity is kept down to the minimum.



DIP14(3D14A-P)



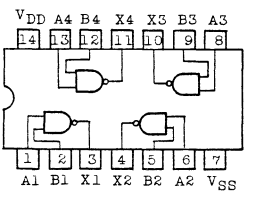
MFP14(F14GB-P)

SOLUTE MAXIMUM RATINGS

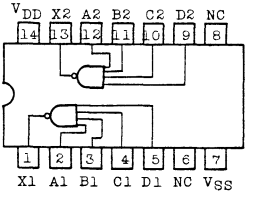
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
put Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
tput Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	±10	mA
wer Dissipation	P_D	300(DIP)/180(MFP)	mW
erating mperature Range	T_A	-40 ~ 85	°C
orage mperature Range	T_{stg}	-65 ~ 150	°C
ad Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT (TOP VIEW)

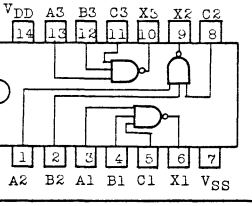
TC4011BP/BF



TC4012BP/BF

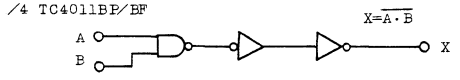


TC4023BP/BF

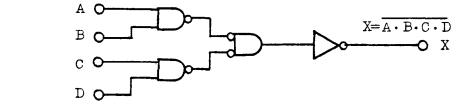


OGIC DIAGRAM

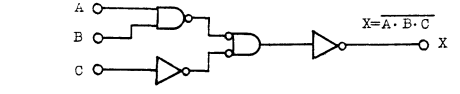
/4 TC4011BP/BF



/2 TC4012BP/BF



/3 TC4023BP/BF



TC4011BP/BF, TC4012BP/BF, TC4023BP/BF

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNI
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	
			10	9.95	-	9.95	10.00	-	9.95	-	
		V_{IN}=V_{SS}, V_{DD}	15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	V
			10	-	0.05	-	0.00	0.05	-	0.05	
		V_{IN}=V_{DD}	15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current (TC4012BP/BF)	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		V_{IN}=V_{SS}, V_{DD}									
Output High Current (TC4012BP/BF)	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	mA
		V_{IN}=V_{DD}									
Output High Current (TC4011BP/BF), (TC4023BP/BF)	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V	15	-1.4	-	-1.2		-	-1.0	-	
		V_{IN}=V_{SS}, V_{DD}									
Output Low Current (TC4011BP/BF), (TC4023BP/BF)	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
		V_{IN}=V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	V
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD}	5	-	0.25	-	0.001	0.25	-	7.5	μA
			10	-	0.5	-	0.001	0.5	-	15	
		*	15	-	1.0	-	0.002	1.0	-	30	

* All valid input combinations.

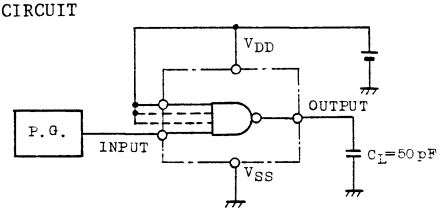
TC4011BP/BF, TC4012BP/BF, TC4023BP/BF

NAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

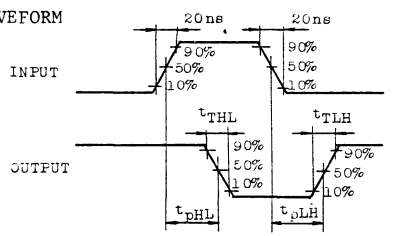
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
utput Transition Time (TC4012BP/BF)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
utput Transition Time (TC4012BP/BF)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
utput Transition Time (TC4011BP/BF) (TC4023BP/BF)	t_{TLH}		5	-	130	400	
			10	-	65	200	
			15	-	50	160	
utput Transition Time (TC4011BP/BF) (TC4023BP/BF)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
ropagation Delay Time (TC4011BP/BF)	t_{pLH}		5	-	150	300	
			15	-	70	150	
			15	-	60	125	
ropagation Delay Time (TC4011BP/BF)	t_{pHL}		5	-	125	250	
			10	-	60	125	
			15	-	45	90	
ropagation Delay Time (TC4012BP/BF)	t_{pLH}		5	-	95	250	
			10	-	45	120	
			15	-	30	90	
ropagation Delay Time (TC4012BP/BF)	t_{pHL}		5	-	95	250	
			10	-	45	120	
			15	-	30	90	
ropagation Delay Time (TC4023BP/BF)	t_{pLH}		5	-	250	400	
			10	-	110	200	
			15	-	85	160	
ropagation Delay Time (TC4023BP/BF)	t_{pHL}		5	-	180	350	
			10	-	90	175	
			15	-	75	125	
nput Capacitance	C_{IN}			-	5	7.5	pF

RCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

CIRCUIT



WAVEFORM



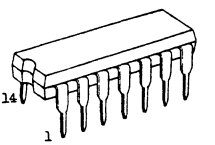
TC4013BP/BF

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

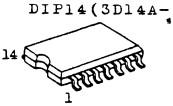
TC4013BP/TC4013BF DUAL D-TYPE FLIP FLOP

TC4013BP/BF contains two independent circuits of D type flip-flop. The input level applied to DATA input are transferred to Q and $\overline{Q}$ output by rising edge of the clock pulse. When RESET input is placed at "H", Q output becomes "L" regardless of other inputs and when RESET input is placed at "L" and SET input is placed at "H", Q output becomes "H" regardless of CLOCK or DATA.

When both of RESET and SET are at "H", RESET takes precedence resulting Q="L" and $\overline{Q}$="H".



DIP14(3D14A-P)

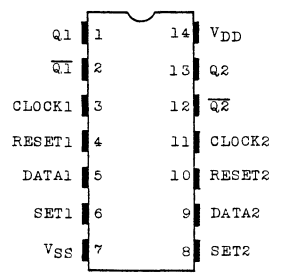


MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

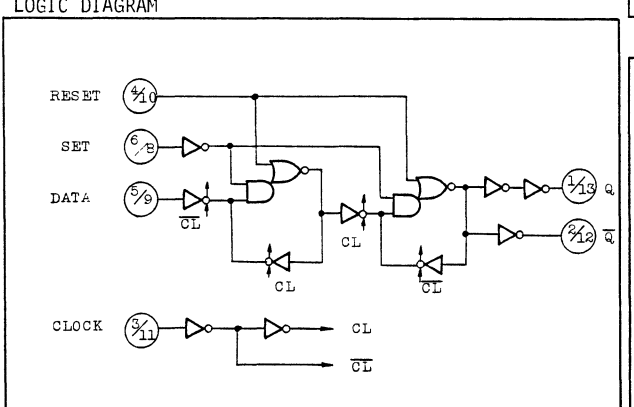
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ∿ 85	°C
Storage Temperature Range	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT

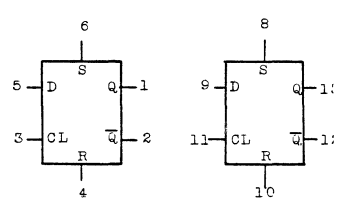


(TOP VIEW)

LOGIC DIAGRAM



BLOCK DIAGRAM



RUTH TABLE

INPUTS				OUTPUTS	
RESET	SET	DATA	CLOCK△	Qn+1	Qn+1
L	H	*	*	H	L
H	L	*	*	L	H
H	H	*	*	L	H
L	L	L	↓	L	H
L	L	H	↓	H	L
L	L	*	↓	Qn •	Qn •

* : DON'T CARE
△ : LEVEL CHANGE
• : NO CHANGE

ECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA, $V_{IN}=V_{SS}$, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA, $V_{IN}=V_{SS}$, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	mA
		V_{OH}=2.5V, V_{OH}=9.5V	5	-	-	-		-	-	-	
		V_{OH}=13.5V	10	-0.5	-	-0.4		-	-0.3	-	
		$V_{IN}=V_{SS}$, V_{DD}	15	-1.4	-	-1.2		-	-1.0	-	
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V, V_{OL}=1.5V	10	1.3	-	1.1		-	0.9	-	
		$V_{IN}=V_{SS}$, V_{DD}	15	3.6	-	3.0		-	2.4	-	
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V V_{OUT}=1.5V,13.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
		$\|I_{OUT}\|$<1μA	15	11.0	-	11.0	8.25	-	11.0	-	
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V V_{OUT}=1.5V,13.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			10	-	3.0	-	4.5	3.0	-	3.0	
		$\|I_{OUT}\|$<1μA	15	-	4.0	-	6.75	4.0	-	4.0	

TC4013BP/BF

STATIC ELECTRICAL CHARACTERISTICS (Continued)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNITS
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	4	-	0.002	4	-	30	μA
				10	-	8	-	0.004	8	-	60	
				15	-	16	-	0.008	16	-	120	

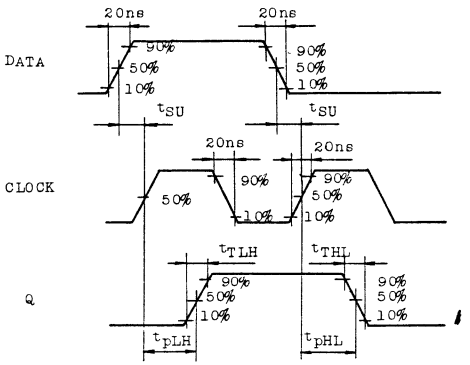
* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

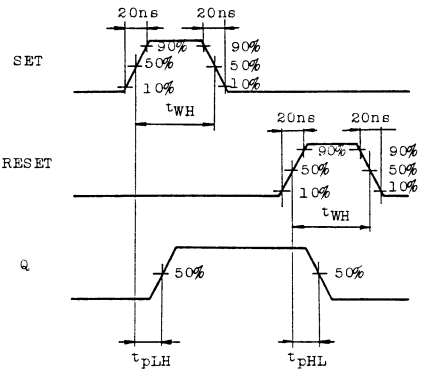
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Transition Time (High to Low)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5	-	250	400	
			10	-	120	250	
			15	-	80	200	
Propagation Delay Time (SET, RESET - Q, $\overline{Q}$)	t_{pLH}		5	-	200	400	
			10	-	80	200	
			15	-	60	150	
Propagation Delay Time (SET, RESET - Q, $\overline{Q}$)	t_{pHL}		5	-	220	400	
			10	-	90	200	
			15	-	75	150	
Max. Clock Frequency	f_{CL}		5	2	3.5	-	MHz
			10	5	10	-	
			15	7	15	-	
Max. Clock Input Rise Time Max. Clock Input Fall Time	t_{rCL} t_{fCL}		5	20	-	-	μs
			10	2.5	-	-	
			15	1.0	-	-	
Min. Pulse Width (SET, RESET)	t_{WH}		5	-	125	250	ns
			10	-	50	100	
			15	-	35	70	
Min. Set-up Time (DATA - CLOCK)	t_{SU}		5	-	20	80	
			10	-	10	40	
			15	-	5	20	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1



WAVEFORM 2

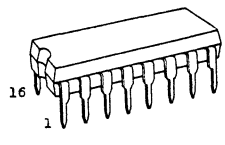


TC4014BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4014BP 8-STAGE STATIC SHIFT REGISTER
(SYNCHRONOUS PARALLEL OR SERIAL INPUT/SERIAL OUTPUT)

TC4014BP is 8 stage shift register having PARALLEL IN/SERIAL OUT operation, which can also perform SERIAL IN/SERIAL OUT operation. In both parallel operation and serial operation, the input data is obtained on the output of each F/F by rising edge of CLOCK input. (SYNCHRONOUS PARALLEL OR SYNCHRONOUS SERIAL INPUT)
Switching of parallel operation and serial operation is achieved by P/$\overline{S}$ CONTROL input. PARALLEL operation is performed when P/$\overline{S}$ CONTROL is "H" and SERIAL operation is performed when it is "L".

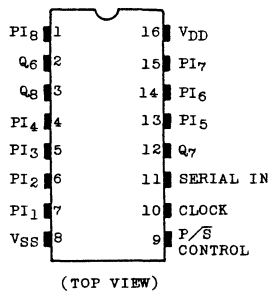


DIP 16(3D16A-P)

MAXIMUM RATINGS

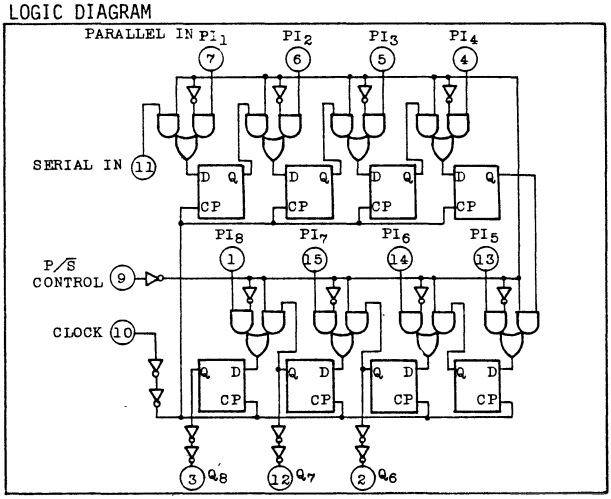
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Ambient Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TRUTH TABLE

INPUTS					OUTPUTS △	
CLOCK △△	P/$\overline{S}$	PI_1	PI_n	SI	Q_1	Q_n
↑	L	*	*	L	L	Q_{n-1}
↑	L	*	*	H	H	Q_{n-1}
↑	H	L	L	*	L	L
↑	H	H	L	*	H	L
↑	H	L	H	*	L	H
↑	H	H	H	*	H	H
↓	*	*	*	*	No Change	

n ; 2~8
△ ; Q_1~Q_5=Internal
△△ ; Level Change
* ; Don't Care

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V,4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V,9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\| < 1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V,4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V,9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\| < 1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

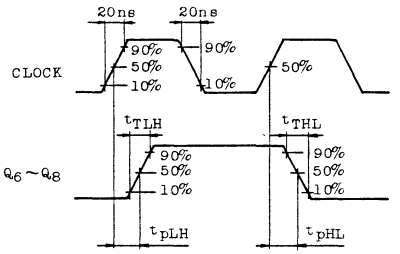
TC4014BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

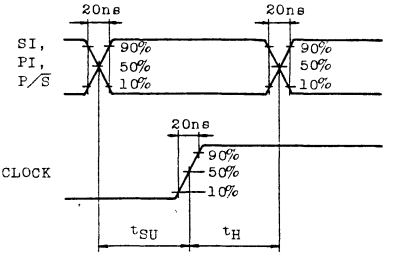
CHARACTERISTIC	SYMBOL	TEST CONDITION V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}	5	-	80	200	ns
		10	-	50	100	
		15	-	40	80	
Output Transition Time (High to Low)	t_{THL}	5	-	80	200	
		10	-	50	100	
		15	-	40	80	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}	5	-	160	320	ns
		10	-	70	160	
		15	-	50	120	
Max. Clock Frequency	f_{CL}	5	3	7.5	-	MHz
		10	6	20	-	
		15	8.5	26	-	
Min. Clock Pulse Width	t_w	5	-	65	180	ns
		10	-	25	80	
		15	-	20	50	
Max. Clock Rise Time Max. Clock Fall Time	t_{rCL} t_{fCL}	5	20	-	-	μs
		10	2.5	-	-	
		15	1.0	-	-	
Min. Set-Up Time (SI - CLOCK)	t_{SU}	5	-	40	120	ns
		10	-	15	80	
		15	-	10	60	
Min. Set-Up Time (PI - CLOCK)	t_{SU}	5	-	35	80	
		10	-	15	50	
		15	-	10	40	
Min. Set-Up Time ($P/\overline{S}$ - CLOCK)	t_{SU}	5	-	80	180	
		10	-	30	80	
		15	-	20	60	
Min. Hold Time (SI, PI, $P/\overline{S}$ - CLOCK)	t_H	5	-	-10	60	ns
		10	-	-2	30	
		15	-	0	20	
Input Capacitance	C_{IN}		-	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1.



WAVEFORM 2.

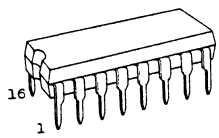


TC4015BP/BF

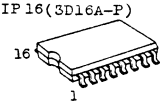
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4015BP/TC4015BF DUAL 4-STAGE STATIC SHIFT REGISTER (With Serial Input/Parallel Output)

TC4015BP/BF contains two circuits of 4 stage shift registers and the independent output is derived from each stage. As all the D type flip-flops of every stage have common RESET input, asynchronous clear operation can be achieved by an external signal at arbitrary timing. The flip-flop of each stage is triggered by rising edge of CLOCK input.
RESET input of "H" level resets the contents of all the stages to "L" regardless of CLOCK and DATA inputs and all of data outputs Q1 through Q4 become "L".
This can be used for converting serial data to parallel one and for ring counters of any numbering systems.



DIP16(3D16A-P)

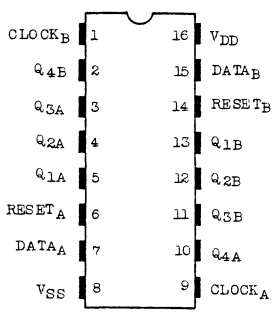


MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

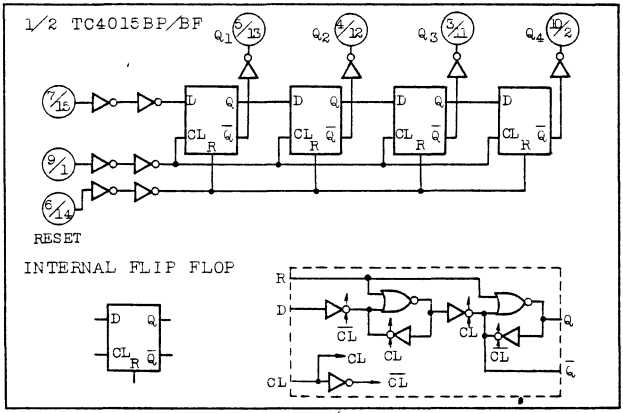
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS			
CLOCK△	DATA	RESET	Q_1	Q_2	Q_3	Q_4
↑	L	L	L	Q_1	Q_2	Q_3
↑	H	L	H	Q_1	Q_2	Q_3
↓	*	L	NO CHANGE			
*	*	H	L	L	L	L

△ : LEVEL CHANGE

* : DON'T CARE

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$ <1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		V_{IN}=V_{SS}, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$ <1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		V_{IN}=V_{SS}, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	mA
		V_{OH}=2.5V	5	-	-	-		-	-	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V	15	-1.4	-	-1.2		-	-1.0	-	
		V_{IN}=V_{SS}, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
		V_{IN}=V_{SS}, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$ <1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$ <1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD}	5	-	20	-	0.005	20	-	150	μA
			10	-	40	-	0.010	40	-	300	
		*	15	-	80	-	0.015	80	-	600	

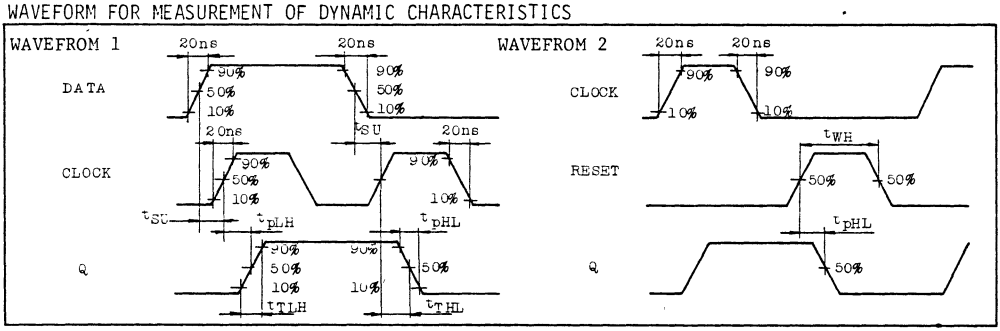
* All valid input combinations.

TC4015BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Transition Time (High to Low)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOSE - Q)	t_{pLH}		5	-	280	600	
			10	-	130	300	
			15	-	110	250	
Propagation Delay Time (CLOSE - Q)	t_{pHL}		5	-	240	600	
			10	-	115	300	
			15	-	90	250	
Propagation Delay Time (RESET - Q)	t_{pHL}		5	-	350	700	
			10	-	150	300	
			15	-	120	200	
Max. Clock Frequency	f_{CL}		5	1.0	2.5	-	MHz
			10	2.5	7.0	-	
			15	3.0	8.0	-	
Min. Pulse Width (RESET)	t_{WH}		5	-	150	300	ns
			10	-	75	150	
			15	-	60	130	
Min. Set-up Time (DATA - CLOCK)	t_{SU}		5	-	150	300	
			10	-	100	200	
			15	-	70	150	
Max. Clock Input Rise Time	t_{rCL}		5	20	-	-	μs
Max. Clock Input Fall Time	t_{fCL}		10	2.5	-	-	
			15	1.0	-	-	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

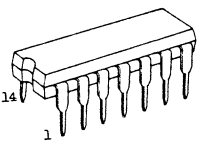
TC4016BP/BF

TC4016BP/TC4016BF QUAD BILATERAL SWITCH

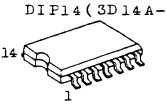
TC4016BP/BF contains for circuits of independent bidirectional switches. When control input CONT is placed at "H" level, the impedance between the input and output of switch becomes low and when CONT is placed at "L" level, it becomes high. This can be used for switching analog and digital signals.

Resistance during ON, R_{ON}
$5 \times 10^2\Omega$(TYP.) ..... V_{DD}-V_{SS}=10V
$2.5 \times 10^2\Omega$(TYP.) ..... V_{DD}-V_{SS}=15V

Resistance during OFF, R_{OFF}
R_{OFF}(TYP.) > $10^9\Omega$



DIP14(3D14A-P)

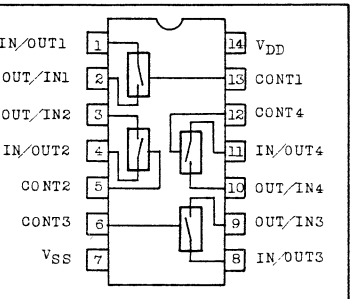


MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNITS
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ∿ V_{SS}+20	V
Control Input Voltage	V_{CIN}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Switch I/O Voltage	$V_{I/O}$	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Control Input Current	I_C	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ∿ 85	°C
Storage Temperature Range	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

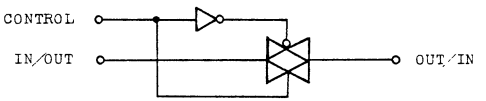
PIN ASSIGNMENT



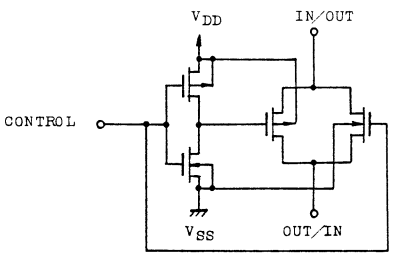
(TOP VIEW)

LOGIC DIAGRAM

o LOGIC SYMBOL(1/4 TC4016BP/BF)



o CIRCUIT SCHEMATIC(1/4 TC4016BP/BF)



TRUTH TABLE

CONTROL	IMPEDANCE BETWEEN IN/OUT - OUT/IN ※
H	2 ~ 20x10²Ω
L	> $10^9\Omega$

※ SEE STATIC ELECTRICAL CHARACTERISTICS

TC4016BP/BF

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input/Output Voltage	V_{IN}/V_{OUT}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (In case not specifically appointed, V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{SS} (V)	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
Control Input High Voltage	V_{IH}	|Iis|=10μA		5	3.5	-	3.5	2.4	-	3.5	-	V
				10	7.0	-	7.0	4.8	-	7.0	-	
				15	11.0	-	11.0	7.2	-	11.0	-	
Control Input Low Voltage	V_{IL}	|Iis|=10μA		5	-	1.0	-	1.7	1.0	-	1.0	
				10	-	1.0	-	1.7	1.0	-	1.0	
				15	-	1.0	-	1.7	1.0	-	1.0	
On-State Resistance	R_{ON}	V_{IN}=5V		5	-	-	-	600	-	-	-	Ω
		V_{IN}=2.5V		5	-	-	-	6000	-	-	-	
		V_{IN}=0.25V		5	-	-	-	600	-	-	-	
		V_{IN}=10V		10	-	600	-	250	700	-	900	
		V_{IN}=5V		10	-	1300	-	600	1500	-	2000	
		V_{IN}=0.25V		10	-	600	-	250	700	-	900	
		V_{IN}=15V		15	-	430	-	200	500	-	650	
		V_{IN}=7.5V		15	-	800	-	300	950	-	1200	
		V_{IN}=0.25V		15	-	430	-	200	500	-	650	
		V_{IN}=5V	-5	5	-	600	-	250	700	-	900	
		V_{IN}=±0.25V	-5	5	-	1300	-	600	1500	-	2000	
		V_{IN}=-5V	-5	5	-	600	-	250	700	-	900	
		V_{IN}=7.5V	-7.5	7.5	-	430	-	200	500	-	650	
		V_{IN}=±0.25V	-7.5	7.5	-	800	-	300	950	-	1200	
		V_{IN}=-7.5V	-7.5	7.5	-	430	-	200	500	-	650	
ΔOn-State Resistance Between Any 2 Switches	$R_{ON}\Delta$		-5	5	-	-	-	15	-	-	-	
			-7.5	7.5	-	-	-	10	-	-	-	
Input/Output Leakage Current	I_{OFF}	V_{IN}=10V, V_{OUT}=0V		10	-	-	-	±0.01	±125	-	-	nA
		V_{IN}=0V, V_{OUT}=10V		10	-	-	-	±0.01	±125	-	-	
		V_{IN}=18V, V_{OUT}=0V		18	-	±250	-	±0.1	±250	-	±1000	
		V_{IN}=0V, V_{OUT}=18V		18	-	±250	-	±0.1	±250	-	±1000	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{DD}, V_{SS}$		5	-	1.0	-	0.001	1.0	-	7.5	μA
				10	-	2.0	-	0.001	2.0	-	15	
		*		15	-	4.0	-	0.002	4.0	-	30	
Input Current	I_{IH}	V_{IH}=18V		18	-	0.3	-	10^{-5}	0.3	-	1.0	
	I_{IL}	V_{IL}=0V		18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITION	V_{SS}(V)	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Propagation Delay Time (IN - OUT)	t_{pLH} t_{pHL}	R_L=10kΩ C_L=50pF	0	5	-	50	100	ns
			0	10	-	20	40	
			0	15	-	16	30	
Propagation Delay Time (CONTROL - OUT)	t_{pLH} t_{pHL}	R_L=10kΩ C_L=50pF	0	5	-	100	140	
			0	10	-	40	60	
			0	15	-	35	50	
Max. Control Input Repetition Rate	f_{MAX} (CONT)	C_L=15pF	0	5	-	4.0	-	MHz
			0	10	-	10.0	-	
			0	15	-	12.0	-	
-3dB Cutoff Frequency	f_{MAX} (I-O)	R_L=2kΩ C_L=15pF (*1)	-5	5	-	8.5	-	
		R_L=10kΩ C_L=15pF (*1)	-5	5	-	7.5	-	
		R_L=100kΩ C_L=15pF (*1)	-5	5	-	5	-	
Total Harmonic Distortion	-	R_L=10kΩ f=1MHz (*2)	-5	5	-	0.3	-	%
-50dB Feedthrough Frequency	-	R_L=1kΩ (*3)	-5	5	-	600	-	kHz
Crosstalk (CONTROL - OUT)	-	R_{IN}=1kΩ R_{OUT}=10kΩ C_L=15pF	0	5	-	50	-	mV
			0	10	-	100	-	
			0	15	-	150	-	
Input Capacitance	C_{IN}	Control Input			-	5	-	pF
		Switch I/O			-	4	-	

*1. The frequency at 20 log $10\frac{V_{os}}{V_{is}}$=-3dB shall be f_{MAX}(I-O) using sine wave of $\pm 2.5V_{p-p}$ for Vis.

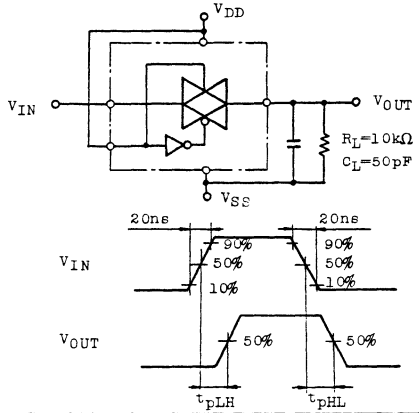
*2. V_{is} shall be sine wave of $\pm 2.5V_{p-p}$.

*3. The frequency at 20 log $10\frac{V_{os}}{V_{is}}$=-50dB shall be the feed through using sine wave of $\pm 2.5V_{p-p}$

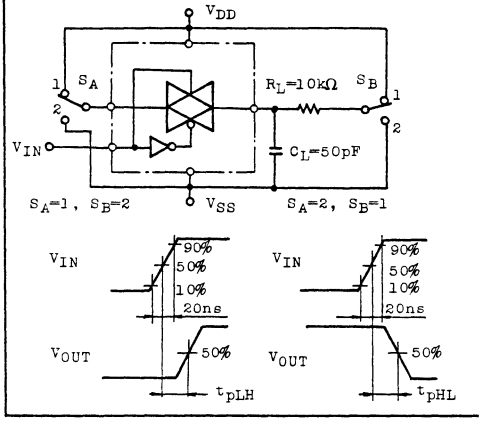
TC4016BP/BF

CIRCUIT FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

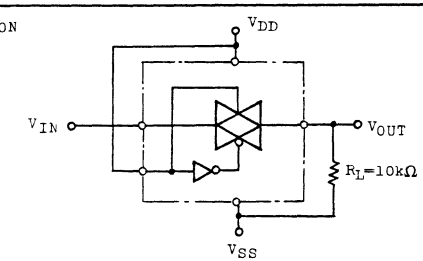
1 t_{pLH} , t_{pHL} (IN - OUT)



2 t_{pLH} , t_{pHL} (CONTROL - OUT)

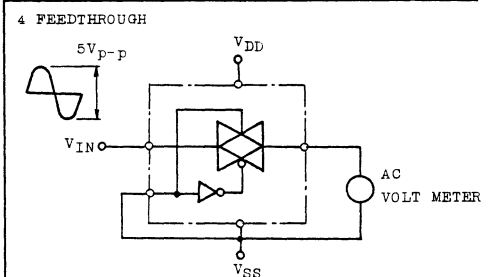


3 R_{ON}

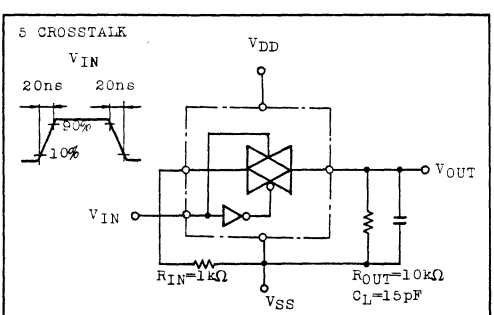


$$R_{ON} = 10 \times \frac{(V_{IN} - V_{OUT})}{V_{OUT}} \quad [k\Omega]$$

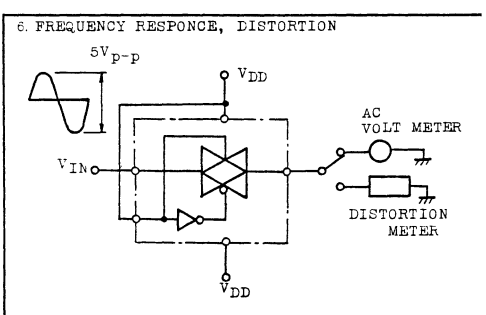
4 FEEDTHROUGH



5 CROSSTALK



6. FREQUENCY RESPONCE, DISTORTION

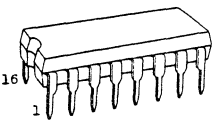


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

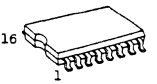
TC4017BP/BF

TC4017BP/TC4017BF DECADE COUNTER/DIVIDER

TC4017BP/BF is decimal Johnson counter consisting of 5 stage D-type flip-flop equipped with the decoder to convert the output to decimal.
Depending on the number of count pulses fed to CLOCK or CLOCK INHIBIT one output among 10 output lines "Q_0" through "Q_9" becomes "H" level.
The counter advances its state at rising edge of CLOCK (CLOCK INHIBIT="L") or falling edge of CLOCK INHIBIT (CLOCK="H"). RESET input to "H" level resets the counter to Q_0="H" and Q_1 through Q_9="L" regardless of CLOCK and CLOCK INHIBIT.



DIP 16(3D16A-P)

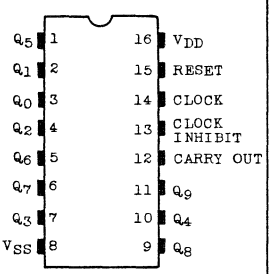


MFP 16(F16GC-P)

MAXIMUM RATINGS

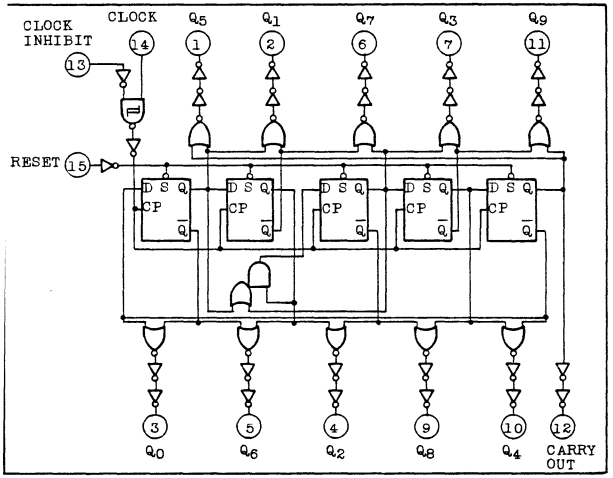
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Ambient Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



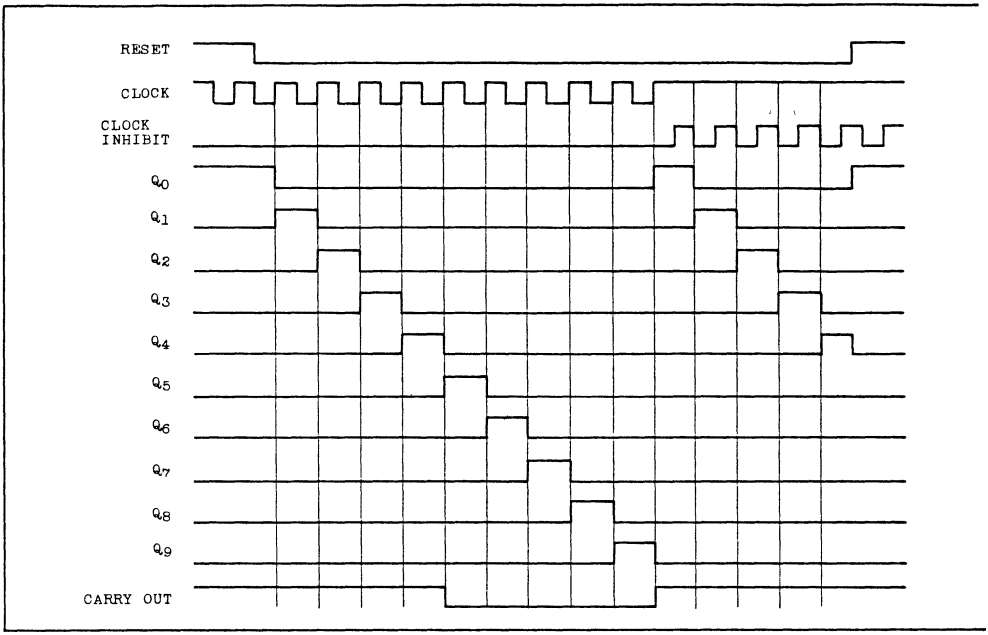
TRUTH TABLE

INPUTS			SELECTED OUTPUT
CLOCK △	CLOCK INHIBIT △	RESET	
*	*	H	Q_0
*	H	L	Q_n (NC)
L	*	L	Q_n (NC)
↓	L	L	Q_n+1
↑	L	L	Q_n (NC)
H	↓	L	Q_n (NC)
H	↑	L	Q_n+1

△ ; Level Change
* ; Don't Care
NC ; No Change
CARRY OUT { "H" ·· Q_0~Q_4 = "H" / "L" ··· Q_5~Q_9 = "H"

TC4017BP/BF

TIMING CHART



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		V_{IN}=V_{SS},V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		V_{IN}=V_{SS},V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H"Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L"Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combination.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	

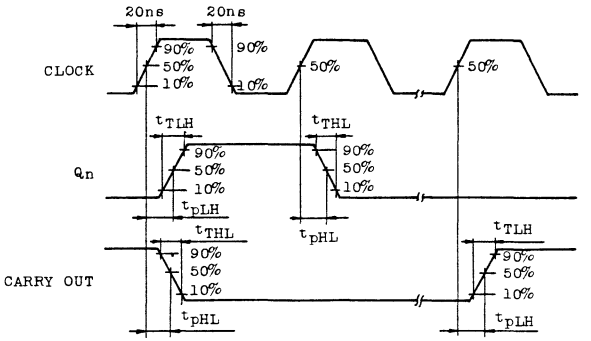
TC4017BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

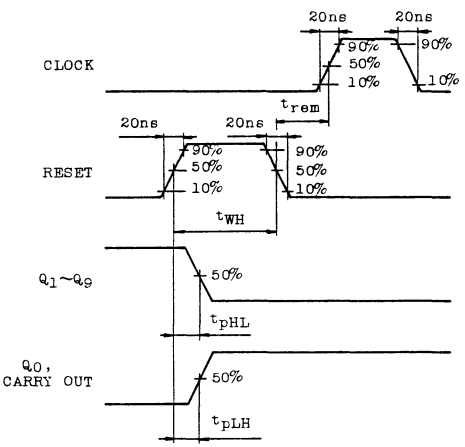
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (CLOCK - Q_n)	t_{pLH} t_{pHL}		5	-	325	650	ns
			10	-	135	270	
			15	-	85	170	
Propagation Delay Time (CLOCK - CARRY OUT)	t_{pLH} t_{pHL}		5	-	280	600	
			10	-	110	250	
			15	-	75	160	
Propagation Delay Time (RESET - Q_n / RESET - CARRY OUT)	t_{pLH} t_{pHL}		5	-	265	530	
			10	-	115	230	
			15	-	85	170	
Max. Clock Frequency	f_{CL}		5	2.5	6	-	MHz
			10	5	12	-	
			15	5.5	13.5	-	
Min. Clock Pulse Width	t_w		5	-	85	200	ns
			10	-	40	100	
			15	-	35	90	
Min. Pulse Width (RESET)	t_{WH}		5	-	50	260	
			10	-	20	110	
			15	-	15	60	
Max. Clock Rise Time Max. Clock Fall Time	t_{rCL} t_{fCL}		5	No Lomit			μs
			10				
			15				
Min. Set-up Time (CLOCK INHIBIT - CLCOK)	t_{SU}		5	-	30	230	ns
			10	-	15	100	
			15	-	10	70	
Min. Removal Time (RESET - CLOCK)	t_{rem}		5	-	-55	400	ns
			10	-	-20	280	
			15	-	-15	150	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

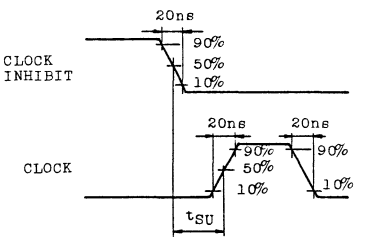
WAVEFORM 1.



WAVEFORM 2.



WAVEFORM 3.

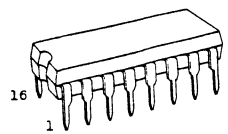


TC4018BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4018BP PRESETTABLE DIVIDE-BY-"N" COUNTER

TC4018BP is frequency division counter consisting of 5 bit Johnson counter having capability of frequency division by the factors of 1/2, 1/4, 1/6, 1/8 and 1/10 by connecting outputs $\overline{Q}_1$ through $\overline{Q}_5$ to DATA input. Similarly by connecting the outputs of $\overline{Q}_1$ through $\overline{Q}_5$ to DATA input through gates, frequency division by the factors of 1/3, 1/5, 1/7 and 1/9 can be achieved.
RESET and PRESET are asynchronous type and when RESET="H", all of $\overline{Q}_1$ through $\overline{Q}_5$ are "H". When PRESET ENABLE="H", $\overline{Q}_n$ is complement of IN_n.
The counter advances its state by rising edge of clock input.

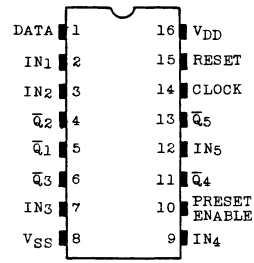


DIP 16(3D16A-P)

MAXIMUM RATINGS

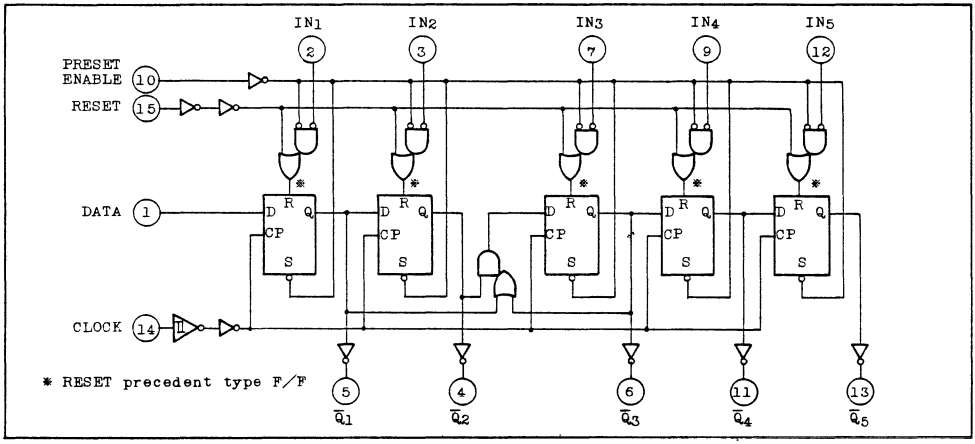
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Ambient Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	26°C · 10sec	

PIN ASSIGNMENT

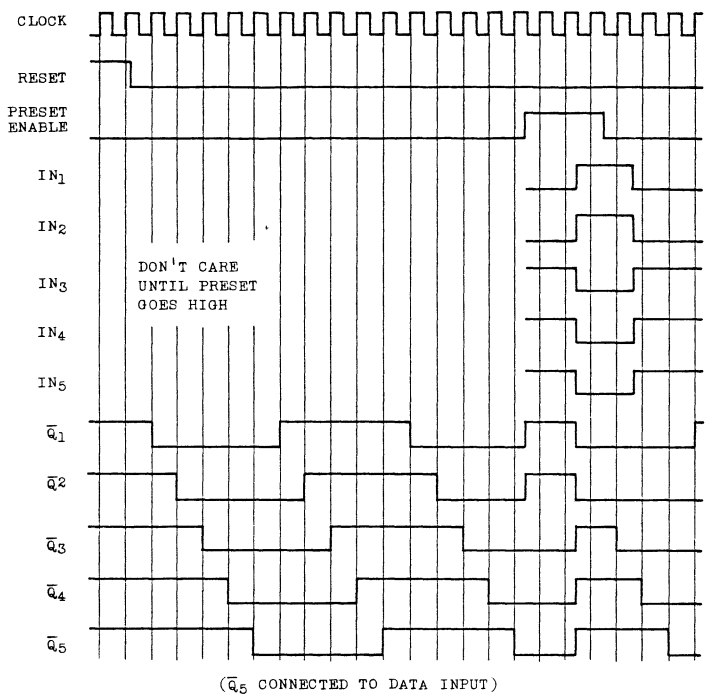


(TOP VIEW)

LOGIC DIAGRAM



IMING CHART



($\overline{Q}_5$ CONNECTED TO DATA INPUT)

FUNCTION SELECTION, TRUTH TABLE

FUNCTION SELECTION

COUNTER MODE	CONNECT DATA INPUT (Pin 1) to :	COMMENTE
10 (Division)	$\overline{Q}_5$	
8 "	$\overline{Q}_4$	
6 "	$\overline{Q}_3$	–
4 "	$\overline{Q}_2$	
2 "	$\overline{Q}_1$	
9 "	$\overline{Q}_5$, $\overline{Q}_4$	USE AND GATE
7 "	$\overline{Q}_4$, $\overline{Q}_3$	
5 "	$\overline{Q}_3$, $\overline{Q}_2$	
3 "	$\overline{Q}_2$, $\overline{Q}_1$	

TRUTH TABLE

CLOCK	RESET	PE	IN_n	$\overline{Q}_n$
↓	L	L	*	$\overline{Q}_n$ △
↑	L	L	*	$\overline{D}_n$
*	L	H	L	H
*	L	H	H	L
*	H	*	*	H

* Don't care

△ No Change

TC4018BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V,4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V,9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V,4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V,9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valied input combinations.

)YNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
)utput Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
)utput Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
'ropagation Delay Time (CLOCK - $\overline{Q}$)	t_{pLH} t_{pHL}		5	-	280	560	ns
			10	-	110	220	
			15	-	80	160	
'ropagation Dealy Time ('PRESET ENABLE - $\overline{Q}$)	t_{pLH} t_{pHL}		5	-	300	600	
			10	-	110	250	
			15	-	80	180	
'ropagation Delay Time ('RESET - $\overline{Q}$)	t_{pLH}		5	-	300	600	
			10	-	110	250	
			15	-	80	180	
1ax. Clock Frequency	f_{CL}		5	2	4	-	MHz
			10	5.5	11	-	
			15	8	16	-	
1in. Clock Pulse Width	t_w		5	-	125	250	ns
			10	-	45	90	
			15	-	30	60	
1ax. Clock Rise Time 1ax. Clock Fall Time	t_{rCL} t_{fCL}		5	No Limit			μs
			10				
			15				
1in. Set-up Time (DATA - CLOCK)	t_{SU}		5	-	35	70	ns
			10	-	15	30	
			15	-	10	20	
1in. Hold Time (DATA - CLOCK)	t_H		5	-	-20	140	ns
			10	-	-5	80	
			15	-	-5	60	
1in. Removal Time ('PE, 'RESET - CLOCK)	t_{rem}		5	-	35	80	ns
			10	-	15	30	
			15	-	10	20	

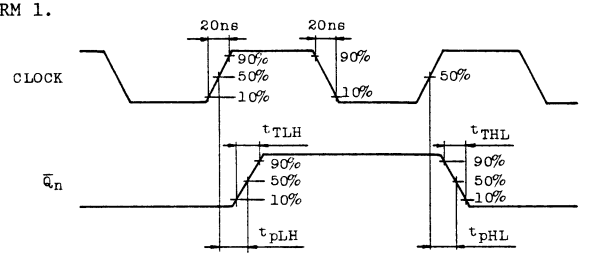
TC4018BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

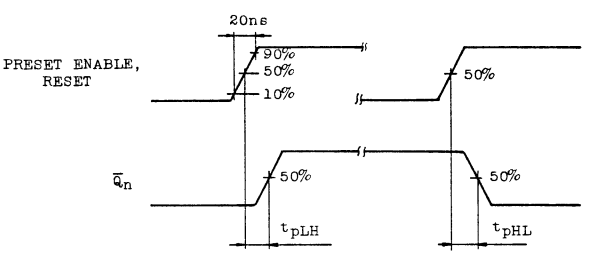
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Min. Pulse Width (PRESET ENABLE, RESET)	t_{WH}		5	-	110	220	ns
			10	-	40	80	
			15	-	30	60	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

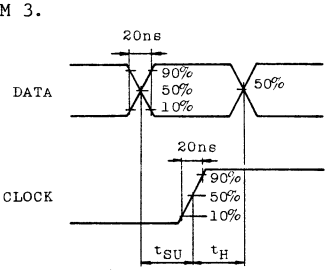
WAVEFORM 1.



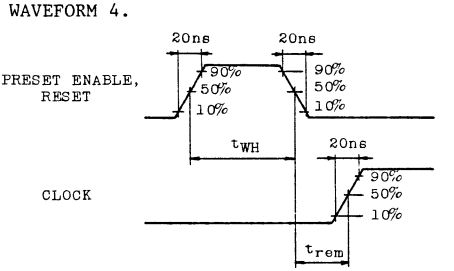
WAVEFORM 2.



WAVEFORM 3.



WAVEFORM 4.



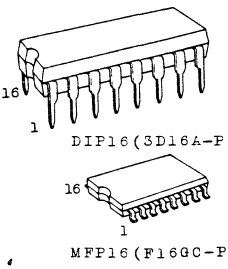
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4019BP/BF

)19BP/TC4019BF QUAD AND/OR SELECT GATE

TC4019BP/BF is four circuit AND-OR SELECT GATE.
: basic circuit consists of two 2 input AND gates
l an OR gate receiving two outputs from the AND
:es. The input signals applied to An and Bn (n=
4) are selected by the common selection input to
l the four circuits, KA and KB and the outputs are
:ained at Dn.

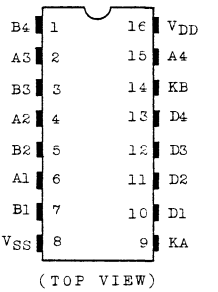
This is suitable for data selectors and
ltiplexers of 4 bits 2 channels.



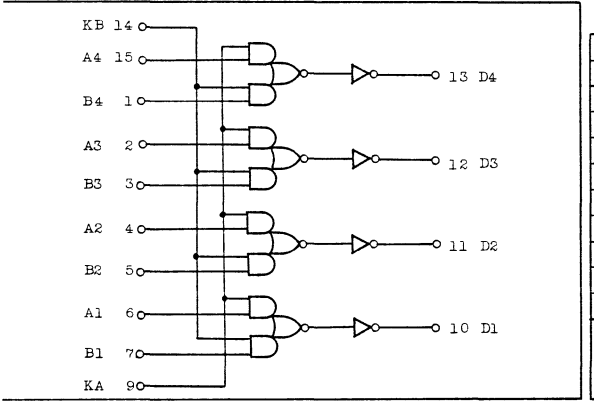
OLUTE MAXIMUM RATINGS

HARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
ut Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
put Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	±10	mA
er Dissipation	P_D	300(DIP)/180(MFP)	mW
rating perature Range	T_A	-40 ∼ 85	°C
rage perature Range	T_{stg}	-65 ∼ 150	°C
d Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



IC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUT
KA	KB	An	Bn	Dn
H	L	H	*	H
H	L	L	*	L
L	H	*	H	H
L	H	*	L	L
L	L	*	*	L
H	H	L	L	L
H	H	L	H	H
H	H	H	L	H
H	H	H	H	H

L : LOW LEVEL
H : HIGH LEVEL
* : DON'T CARE

TC4019BP/BF

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNI
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}$, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	V
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}$, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	
		V_{OH}=2.5V	5	-	-	-		-	-	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V	15	-1.4	-	-1.2		-	-1.0	-	
		$V_{IN}=V_{SS}$, V_{DD}									mA
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	V
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}	5	-	1	-	0.002	1	-	7.5	
			10	-	2	-	0.004	2	-	15	μA
		*	15	-	4	-	0.008	4	-	30	

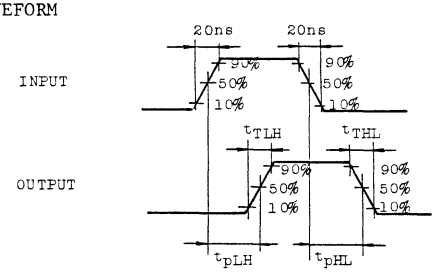
* All valid input combinations.

AMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
tput Transition Time (Low to High)	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
tput Transition Time (High to Low)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
opagation Delay Time (A, B - D)	t_{pLH}		5	-	250	500	
			10	-	100	250	
			15	-	80	200	
opagation Delay Time (A, B - D)	t_{pHL}		5	-	300	500	
			10	-	125	250	
			15	-	100	200	
opagation Delay Time (KA, KB - D)	t_{pLH}		5	-	300	600	
			10	-	140	300	
			15	-	100	250	
opagation Delay Time (KA, KB - D)	t_{pHL}		5	-	350	600	
			10	-	150	300	
			15	-	120	250	
put Capacitance	C_{IN}	An, Bn Input		-	5	7.5	pF
		KA, KB Input		-	12	20	

EFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM

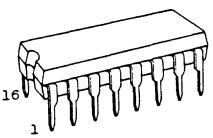


TC4020BP/BF

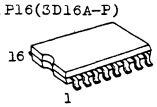
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4020BP/TC4020BF 14 STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDERS

TC4020BP/BF is 14 stage ripple carry binary counter having asynchronous clear function. The counter advances its counting stage by falling edge of $\overline{CLOCK}$ input. When RESET input is placed "H", all the circuits are reset regardless of $\overline{CLOCK}$ input making all the outputs (Q1, Q4 ∿ Q14) to be "L".
This is most suitable for frequency dividers, control circuits and timing circuits.



DIP16(3D16A-P)

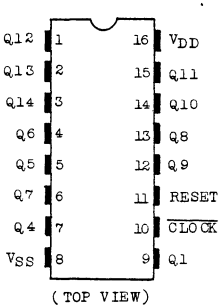


MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNITS
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ∿ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ∿ 85	°C
Storage Temperature Range	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



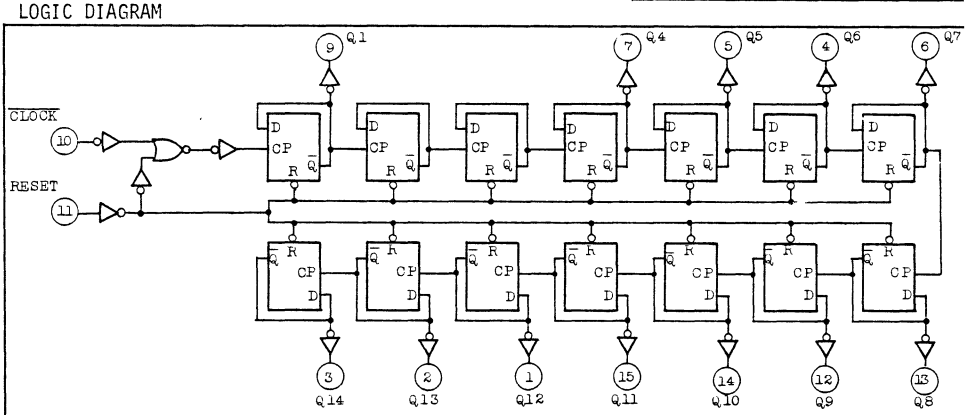
(TOP VIEW)

TRUTH TABLE

$\overline{CLOCK}$ △	RESET	OUTPUT STATE
*	H	ALL OUTPUTS = "L"
⌐	L	NO CHANGE
⌐	L	ADVANCE TO NEXT STATE

△ : LEVEL CHANGE, * : DON'T CARE

LOGIC DIAGRAM



OMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}		3	-	18	V
put Voltage	V_{IN}		0	-	V_{DD}	V

TIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
gh-Level tput Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS}$, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
w-Level tput Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS}$, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
tput High rrent	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	mA
		V_{OH}=2.5V	5	-	-	-		-	-	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V	15	-1.4	-	-1.2		-	-1.0	-	
		$V_{IN}=V_{SS}$, V_{DD}									
tput Low rrent	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
		$V_{IN}=V_{SS}$, V_{DD}									
put High ltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
put Low ltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
ut "H" Level rrent	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
iescent evice Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}	5	-	20	-	0.005	20	-	150	μA
			10	-	40	-	0.010	40	-	300	
		*	15	-	80	-	0.015	80	-	600	

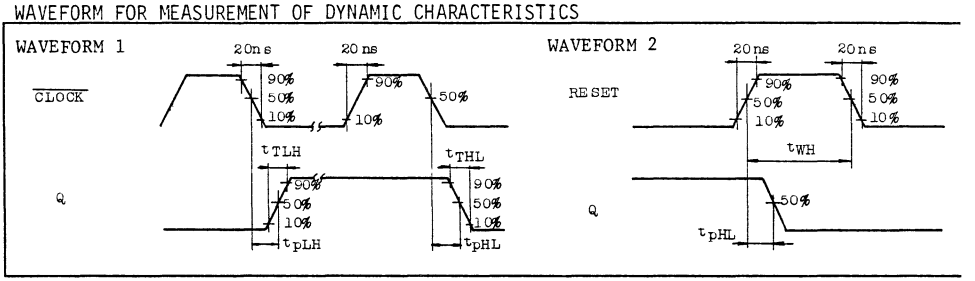
All valid input combinations.

TC4020BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	100	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time ($\overline{CLOCK}$ - Q1)	t_{pLH}		5	-	160	360	
			10	-	80	160	
			15	-	65	130	
Propagation Delay Time ($\overline{CLOCK}$ - Q1)	t_{pHL}		5	-	160	360	
			10	-	80	160	
			15	-	65	130	
Propagation Delay Time ($\overline{CLOCK}$ - Q14)	t_{pLH}		5	-	1000	2000	ns
			10	-	500	1000	
			15	-	400	800	
Propagation Delay Time ($\overline{CLOCK}$ - Q14)	t_{pHL}		5	-	1000	2000	
			10	-	500	1000	
			15	-	400	800	
Propagation Delay Time (RESET - Q)	t_{pHL}		5	-	150	280	ns
			10	-	70	120	
			15	-	50	100	
Max. Clock Frequency	f_{CL}		5	3.5	10	-	MHz
			10	8	20	-	
			15	12	25	-	
Min. Pulse Width (RESET)	t_{WH}		5	-	100	200	ns
			10	-	40	80	
			15	-	30	60	
Max. Clock Input Rise Time	t_{rCL}		5	20	-	-	μs
			10	2.5	-	-	
Max. Clock Input Fall Time	t_{fCL}		15	1.0	-	-	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

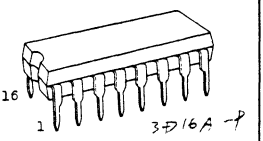


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4021BP

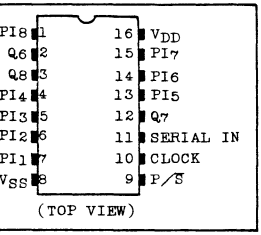
4021BP 8-STAGE STATIC SHIFT REGISTER
SYNCHRONOUS PARALLEL INPUT OR SYNCHRONOUS SERIAL
NPUT/SERIAL OUTPUT)

4021BP is 8 stage parallel in/serial out shift
gister, which can be used also for serial in/serial
t operations.
the case of parallel operation, the data of
RALLEL IN is input to each F/F asynchronously with
OCK and the output is obtained. In the case of
rial operation, each F/F is triggered by rising edge
CLOCK. (ASYNCHRONOUS PARALLEL OR SYNCHRONOUS
RIAL INPUT)
itching of PARALLEL operation and SERIAL operation
achieved by P/$\overline{S}$ CONTROL input. When P/$\overline{S}$ CONTROL
put is "H", PARALLEL operation is designated and
en it is "L", SERIAL operation is designated.



DIP 16(3D16A-P)

PIN ASSIGNMENT



(TOP VIEW)

XIMUM RATINGS

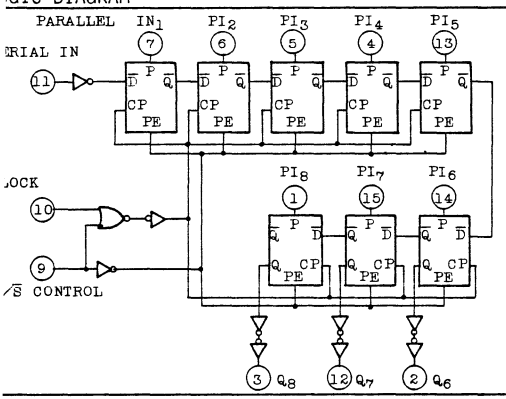
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
put Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
tput Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
wer Dissipation	P_D	300	mW
erating Ambient mperature Range	T_A	-40 ~ 85	°C
orage Temperature nge	Tstg	-65 ~ 150	°C
ad Temp./Time	Tsol	260°C · 10sec	

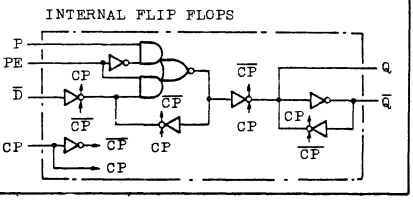
TRUTH TABLE

INPUTS					OUTPUTS △	
CLOCK △△	P/$\overline{S}$	PI_1	PIn	SI	Q_1	Qn
↑	L	*	*	L	L	Qn-1
↑	L	*	*	H	H	Qn-1
↓	L	*	*	*	No Change	
*	H	L	L	*	L	L
*	H	L	H	*	L	H
*	H	H	L	*	H	L
*	H	H	H	*	H	H

n ; 2~8
△ ; Q_1~Q_5 Internal
△△ ; Level Change
* , Don't Care

IGIC DIAGRAM





TC4021BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNI
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UN
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	m
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V,4.5V	5	3.5	-	3.5	2.75	-	3.5	-	
		V_{OUT}=1.0V,9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V,4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V,9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μ
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	5	-	0.005	5	-	150	μ
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		5	-	150	320	ns
			10	-	65	160	
			15	-	45	120	
Propagation Delay Time ($P/\overline{S}$ - Q)	t_{pLH} t_{pHL}		5	-	230	460	ns
			10	-	90	180	
			15	-	60	120	
Max. Clock Frequency	f_{CL}		5	3	6.5	-	MHz
			10	6	18	-	
			15	8.5	24	-	
Min. Clock Pulse Width	t_w		5	-	80	180	ns
			10	-	30	80	
			15	-	20	50	
Max. Clock Rise Time Max. Clock Fall Time	t_{rCL} t_{fCL}		5	20	-	-	μs
			10	2.5	-	-	
			15	1.0	-	-	
Min. Set-up Time (SI - CLOCK)	t_{SU}		5	-	40	120	ns
			10	-	20	80	
			15	-	15	60	
Min. Set-up Time (PI - $P/\overline{S}$)	t_{SU}		5	-	25	50	ns
			10	-	15	30	
			15	-	10	20	
Min. Hold Time ($\begin{pmatrix} SI, \\ PI, \\ P/\overline{S} \end{pmatrix}$ - CLOCK)	t_H		5	-	35	70	ns
			10	-	20	40	
			15	-	15	30	
Min. Pulse Width ($P/\overline{S}$ - CONTROL)	t_{WH}		5	-	90	180	ns
			10	-	30	80	
			15	-	10	50	

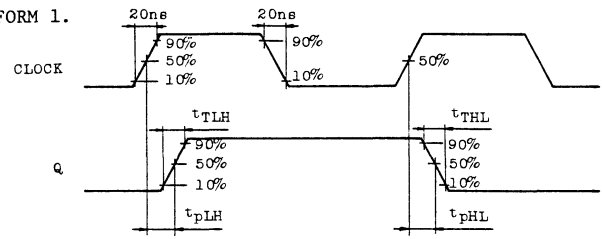
TC4021BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

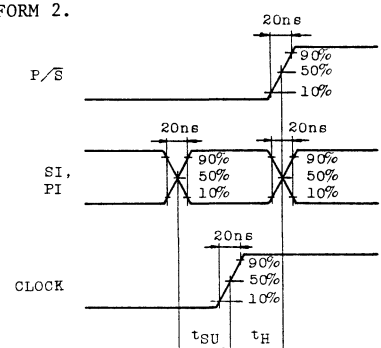
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Min. Removal Time (P/$\overline{S}$ - CLOCK)	t_{rem}		5	-	45	280	ns
			10	-	20	140	
			15	-	15	100	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

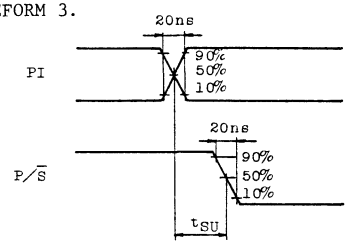
WAVEFORM 1.



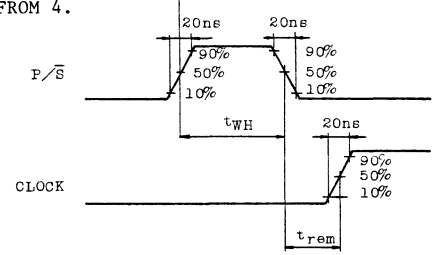
WAVEFORM 2.



WAVEFORM 3.



WAVEFROM 4.

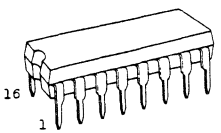


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4022BP

TC4022BP OCTAL COUNTER/DIVIDER

TC4022BP is octal Johnson counter consisting of 4 stage D-type flip-flops and equipped with decoder which convert the output to octal.
Depending on the number of count pulses applied to CLOCK or CLOCK INHIBIT input, one of eight outputs Q_0 through Q7 becomes "H". The counter advances its counting state by rising edge of CLOCK when CLOCK INHIBIT="L" and by falling edge of CLOCK INHIBIT when CLOCK="H".
RESET input with "H" level resets the counter to Q_0="H" and $Q_1 \sim Q_7$="L" regardless of CLOCK and CLOCK INHIBIT.

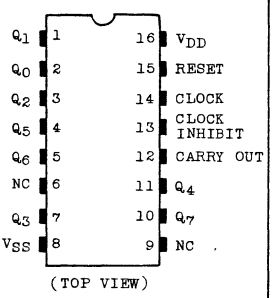


DIP 16(3D16A-P)

MAXIMUM RATINGS

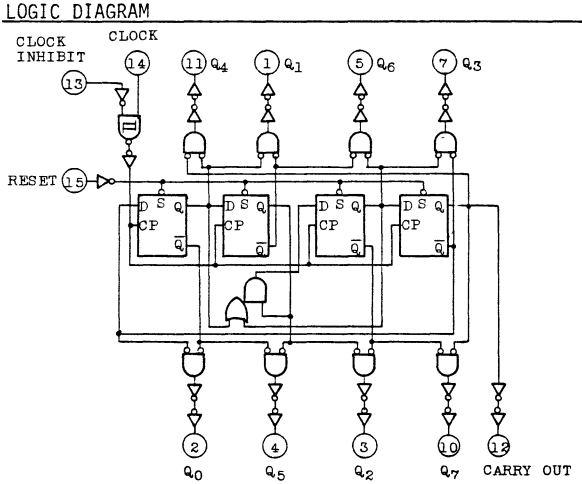
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Ambient Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C ·10sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



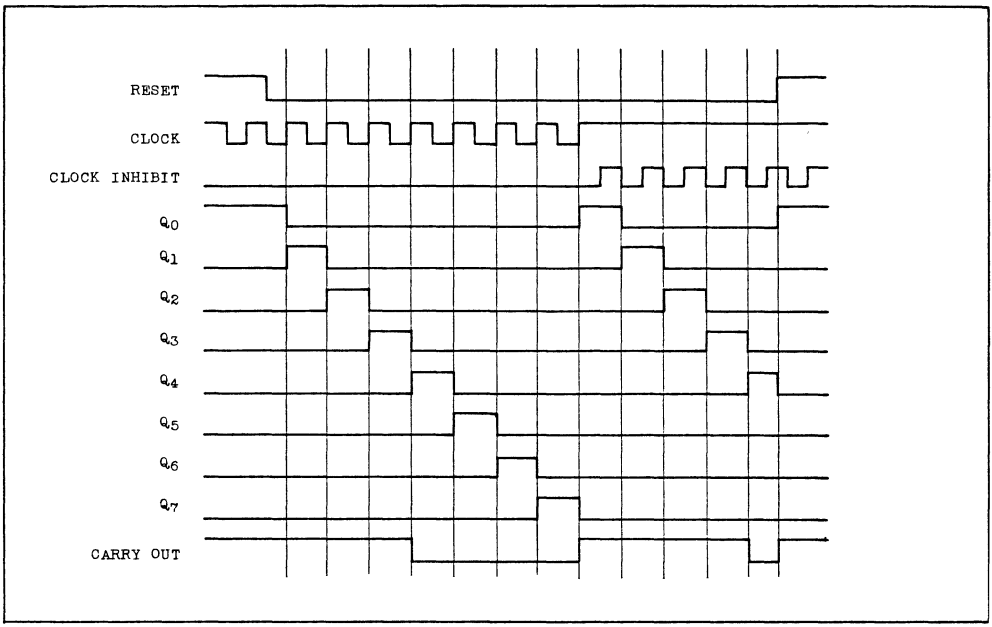
TRUTH TABLE

INPUTS			SELECTED OUTPUT
CLOCK △	CLOCK INHIBIT△	RESET	
*	*	H	Q_0
*	H	L	Q_n(NC)
L	*	L	Q_n(NC)
↑	L	L	Q_n + 1
↓	L	L	Q_n(NC)
H	↑	L	Q_n(NC)
H	↓	L	Q_n + 1

△ ; Level Change
* ; Don't Care
NC ; No Change
CARRY OUT {"H" ··· $Q_0 \sim Q_3$="H" / "L" ··· $Q_4 \sim Q_7$="H"

TC4022BP

TIMING CHART



RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ V_{IN}=V_{SS},V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ V_{IN}=V_{SS},V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		V_{IN}=V_{SS},V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		V_{IN}=V_{SS},V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V,4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V,9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\| < 1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V,4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V,9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\| < 1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	

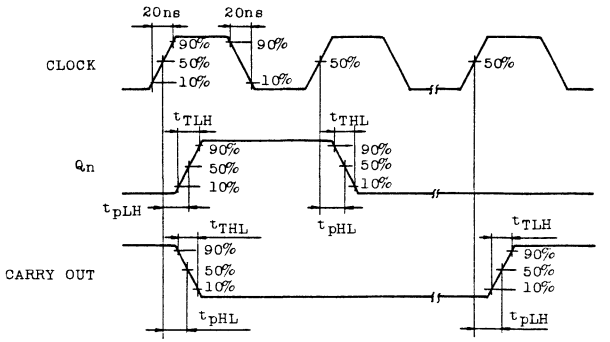
TC4022BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

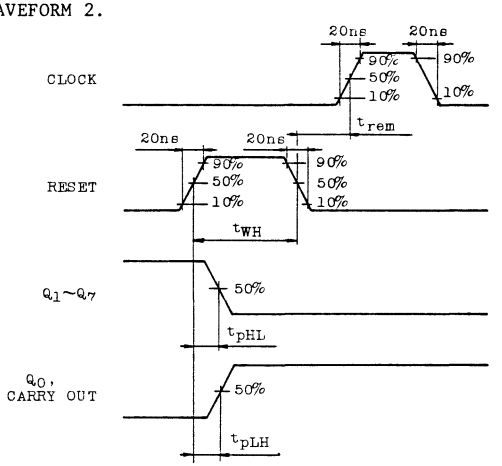
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (CLOCK - Qn)	t_{pLH} t_{pHL}		5	-	325	650	ns
			10	-	135	270	
			15	-	85	170	
Propagation Delay Time (CLOCK - CARRY OUT)	t_{pLH} t_{pHL}		5	-	280	600	
			10	-	110	250	
			15	-	75	160	
Propagation Delay Time (RESET - Q, RESET - CARRY OUT)	t_{pLH} t_{pHL}		5	-	265	530	
			10	-	115	230	
			15	-	85	170	
Max. Clock Frquency	f_{CL}		5	2.5	6	-	MHz
			10	5	12	-	
			15	5.5	13.5	-	
Min. Clock Pulse Width	t_w		5	-	85	200	ns
			10	-	40	100	
			15	-	35	90	
Min. Pulse Width (RESET)	t_{WH}		5	-	50	200	
			10	-	20	110	
			15	-	15	60	
Max. Clock Rise Time Max. Clock Fall Time	t_{rCL} t_{fCL}		5	No Limit			μs
			10				
			15				
Min. Set-up Time (CLOCK INHIBIT - CLOCK)	t_{SU}		5	-	30	230	ns
			10	-	15	100	
			15	-	10	70	
Min. Removal Time (RESET - CLOCK)	t_{rem}		5	-	-55	400	ns
			10	-	-20	280	
			15	-	-15	150	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

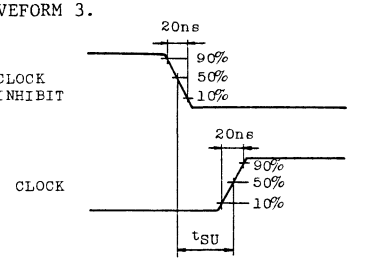
WAVEFORM 1.



WAVEFORM 2.



WAVEFORM 3.

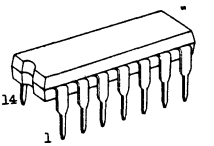


TC4024BP/BF

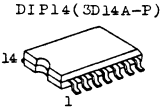
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4024BP/TC4024BF 7 STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDERS

TC4024BP/BF is 7 stage ripple carry type binary counter having asynchronous clear function.
The counter advances its counting state by falling edge of $\overline{\text{CLOCK}}$ input.
When RESET input is placed at "H", all the internal flip-flops are reset making all the outputs Q1 through Q7 to be "L" regardless of $\overline{\text{CLOCK}}$ input.
This is suitable for frequency divider circuits and control circuits.



DIP14(3D14A-P)

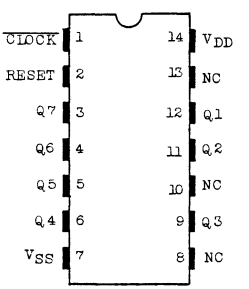


MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ∼ 85	°C
Storage Temperature Range	T_{stg}	-65 ∼ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



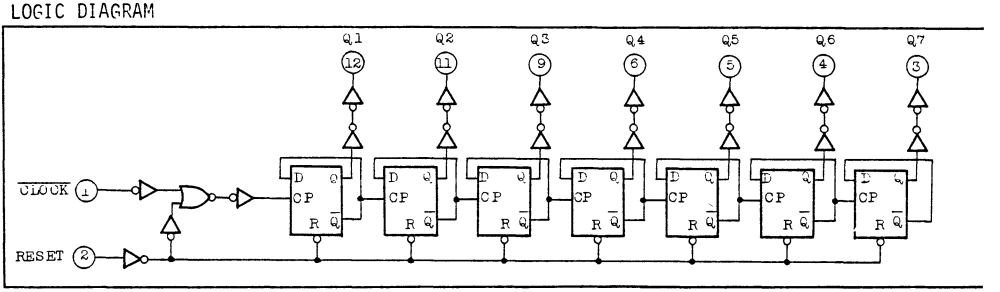
(TOP VIEW)

TRUTH TABLE

$\overline{\text{CLOCK}}$ △	RESET	OUTPUT STAGE
*	H	All Outputs = "L"
⌐	L	No Change
⌐	L	Advance to Next State

△ : Level Change, * : Don't Care

LOGIC DIAGRAM



ECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS}$, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS}$, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	mA
		V_{OH}=2.5V	5	-	-	-		-	-	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V	15	-1.4	-	-1.2		-	-1.0	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}	5	-	20	-	0.005	20	-	150	μA
			10	-	40	-	0.010	40	-	300	
		*	15	-	80	-	0.015	80	-	600	

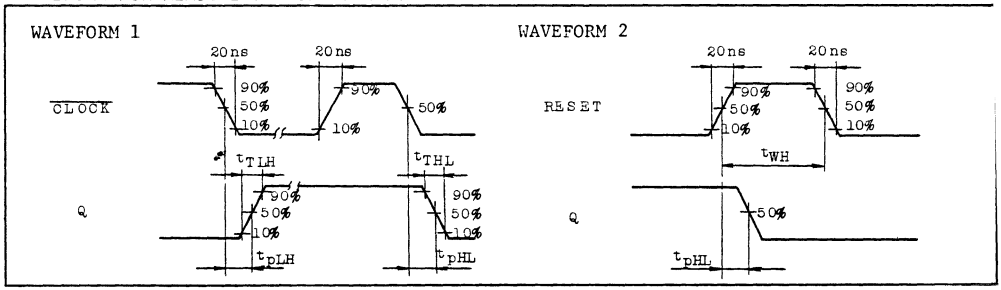
* All valid input combinations.

TC4024BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	100	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time ($\overline{CLOCK}$ - Q1)	t_{pLH}		5	-	180	360	
			10	-	80	160	
			15	-	65	130	
Propagation Delay Time ($\overline{CLOCK}$ - Q1)	t_{pHL}		5	-	180	360	
			10	-	80	160	
			15	-	65	130	
Propagation Delay Time ($\overline{CLOCK}$ - Q7)	t_{pLH}		5	-	600	1200	ns
			10	-	260	520	
			15	-	215	430	
Propagation Delay Time ($\overline{CLOCK}$ - Q7)	t_{pHL}		5	-	600	1200	
			10	-	260	520	
			15	-	215	430	
Propagation Delay Time (RESET - Q)	t_{pHL}		5	-	140	280	ns
			10	-	60	120	
			15	-	50	100	
Max. Clock Frequency	f_{CL}		5	3.5	8	-	MHz
			10	8	20	-	
			15	12	25	-	
Max. Clock Input Rise Time	t_{rCL}		5	20	-	-	μs
Max. Clock Input Fall Time	t_{fCL}		10	2.5	-	-	
			15	1.0	-	-	
Min. Pulse Width (RESET)	t_{WH}		5	-	100	200	ns
			10	-	40	80	
			15	-	30	60	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

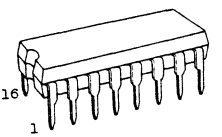
TC4027BP/BF

C4027BP/TC4027BF DUAL J-K MASTER-SLAVE FLIP-FLOP

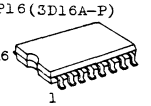
TC4027BP/BF is J-K master-slave flip-flop having ESET and SET functions.

n the case of J-K mode, when the clock input is given ith both RESET and SET at "L", the output changes at ising edge of the clock according to the states of J nd K.

hen RESET is placed at "H", output Q becomes "L" egardless of other inputs and when SET is placed at H" and RESET at "L", Q becomes "H" regardless of ther inputs. (R-S mode)
hen both of RESET and SET are at "H", takes precence resulting Q="L" and Q="H".



DIP16(3D16A-P)

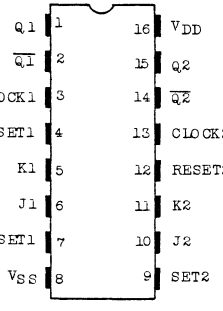


MFP16(F16GC-P)

BSOLUTE MAXIMUM RATINGS

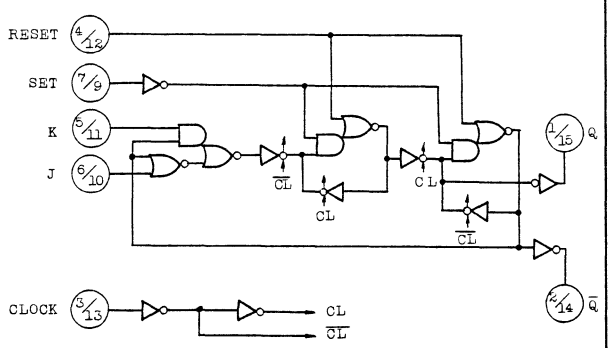
CHARACTERISTIC	SYMBOL	RATING	UNIT
C Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
nput Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
utput Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
C Input Current	I_{IN}	±10	mA
ower Dissipation	P_D	300(DIP)/180(MFP)	mW
perating emperature Range	T_A	-40 ∿ 85	°C
torage emperature Range	T_{stg}	-65 ∿ 150	°C
ead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT

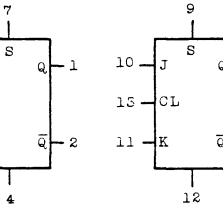


LOGIC DIAGRAM

1/2 TC4027BP/BF



BLOCK DIAGRAM



TC4027BP/BF

TRUTH TABLE

INPUTS					OUTPUTS	
RESET	SET	J	K	CLOCK△	Qn+1	$\overline{Q}$n+1
L	H	*	*	*	H	L
H	L	*	*	*	L	H
H	H	*	*	*	L	H
L	L	L	L	↓	Qn	Qn•
L	L	L	H	↓	L	H
L	L	H	L	↓	H	L
L	L	H	H	↓	$\overline{Qn}$	Qn••
L	L	*	*	↑	Qn	$\overline{Qn}$•

* : DON'T CARE
△ : LEVEL CHANGE
• : NO CHANGE
•• : CHANGE

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA, $V_{IN}=V_{SS}$, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA, $V_{IN}=V_{SS}$, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V, $V_{IN}=V_{SS}$, V_{DD}	5	-0.2	-	-0.16		-	-0.12	-	mA
		V_{OH}=2.5V, V_{OH}=9.5V	5	-	-	-		-	-	-	
		V_{OH}=13.5V	10	-0.5	-	-0.4		-	-0.3	-	
			15	-1.4	-	-1.2		-	-1.0	-	
Output Low Current	I_{OL}	V_{OL}=0.4V, $V_{IN}=V_{SS}$, V_{DD}	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V, $\|I_{OUT}\|$<1μA	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	

ATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
put Low ltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	V
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V $\|I_{OUT}\|$<1μA	15	-	4.0	-	6.75	4.0	-	4.0	
put rrent	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
iescent evice Current		I_{DD}	V_{IN}=V_{SS}, V_{DD}	5	-	4	-	0.002	4	-	30	μA
				10	-	8	-	0.004	8	-	60	
			*	15	-	16	-	0.008	16	-	120	

All valid input combinations.

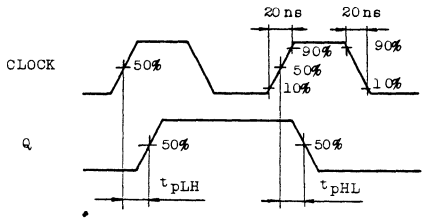
/NAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
utput Transition Time (Low to High)	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
utput Transition Time (High to Low)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
ropagation Delay Time (CLOCK - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5	-	250	500	
			10	-	110	300	
			15	-	80	260	
ropagation Delay Time (SET, RESET - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5	-	250	600	
			10	-	110	300	
			15	-	80	260	
lax. Clock Frequency	f_{CL}		5	1.0	3.0	-	MHz
			10	3.0	8.0	-	
			15	3.5	12.0	-	
lax. Clock Input Rise Time lax. Clock Input Fall Time	t_{rCL} t_{fCL}		5	20	-	-	μs
			10	2.5	-	-	
			15	1.0	-	-	
lin. Pulse Width (SET, RESET)	t_{WH}		5	-	100	500	ns
			10	-	50	250	
			15	-	40	200	
lin. Set-up Time (J, K - CLOCK)	t_{SU}		5	-	100	250	
			10	-	40	125	
			15	-	30	100	
Input Capacitance	C_{IN}			-	5	7.5	pF

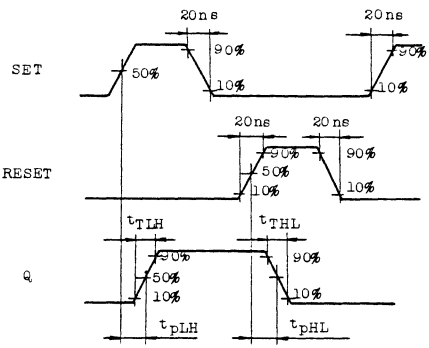
TC4027BP/BF

WAVEFROM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

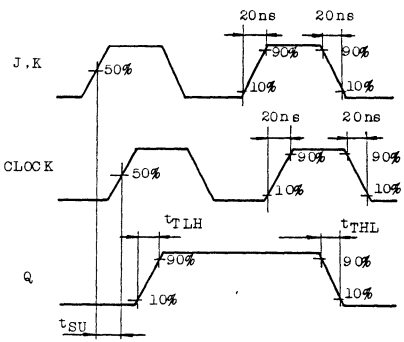
WAVEFORM 1



WAVEFORM 2



WAVEFORM 3



C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

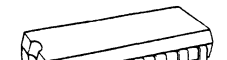
TC4028BP/BF

TC4028BP/TC4028BF BCD-TO-DECIMAL DECODER

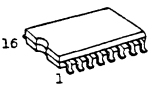
The TC4028BP/BF is a BCD-to-DECIMAL decoder which converts BCD signal into DECIMAL signal.

If ten outputs from Q_0 to Q9, one output corresponding to input BCD code goes to the "H" level and all the others remain at the "L" level.

When D is used as inhibit input by use of three input lines from A to C, this decoder can be served as a BINARY-to-OCTAL decoder.



DIP 16(3D16A-P)

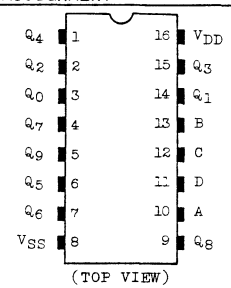


MFP 16(F16GC-P)

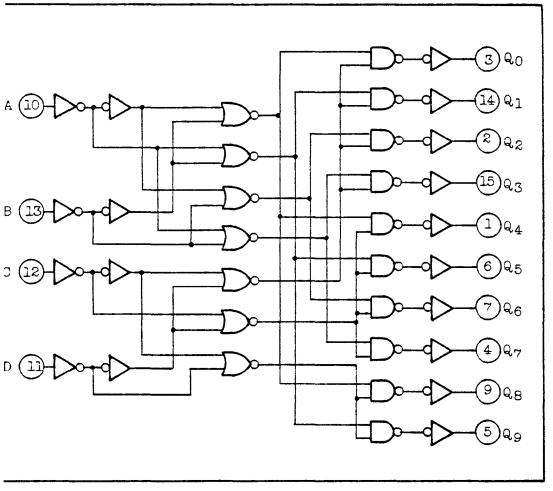
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS									
D	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	L	L	H	L	H	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	H	L	L	L	L	L	L	H	L	L	L	L	L
L	H	L	H	L	L	L	L	L	H	L	L	L	L
L	H	H	L	L	L	L	L	L	L	H	L	L	L
L	H	H	H	L	L	L	L	L	L	L	H	L	L
H	L	L	L	L	L	L	L	L	L	L	L	H	L
H	L	L	H	L	L	L	L	L	L	L	L	L	H
H	L	H	L	L	L	L	L	L	L	L	L	L	L
H	L	H	H	L	L	L	L	L	L	L	L	L	L
H	H	L	L	L	L	L	L	L	L	L	L	L	L
H	H	L	H	L	L	L	L	L	L	L	L	L	L
H	H	H	L	L	L	L	L	L	L	L	L	L	L
H	H	H	H	L	L	L	L	L	L	L	L	L	L

H = HIGH LEVEL L = LOW LEVEL

TC4028BP/BF

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UN
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									mA
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									V
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

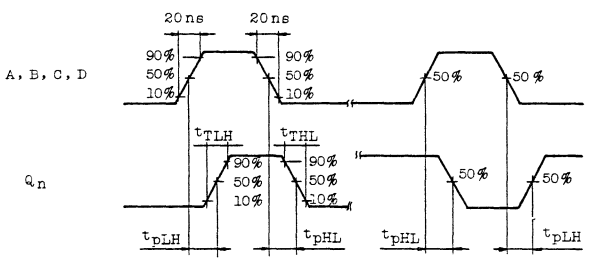
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
)uiescent Device :urrent	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

)YNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
)utput Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
)utput Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time	t_{pLH} t_{pHL}		5	-	150	350	ns
			10	-	65	160	
			15	-	50	120	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

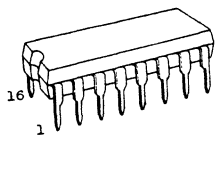


TC4029BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4029BP PRESETTABLE UP/DOWN COUNTER

TC4029BP is up/down counter having the capabilities of preset operation, parallel carry connection and decimal/binary switching.
Switching of decimal counter and binary counter is controlled by BINARY/$\overline{\text{DECADE}}$ input ("H"-Binary and "L"-Decimal), and switching of UP/$\overline{\text{DOWN}}$ is controlled by UP/$\overline{\text{DOWN}}$ input ("H"-Count up and "L"-Count down).
As PRESET ENABLE input at "H" level causes input information at A_{IN} through D_{IN} to be directly input to the flip-flops, any arbitrary count can be set.
The counter advances its counting state by rising edge of CLOCK input.

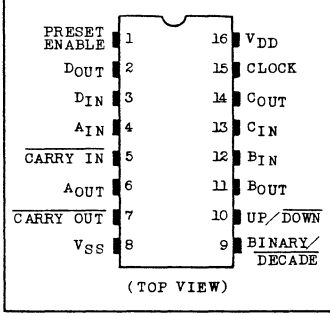


DIP16 (3D16A-P)

MAXIMUM RATINGS

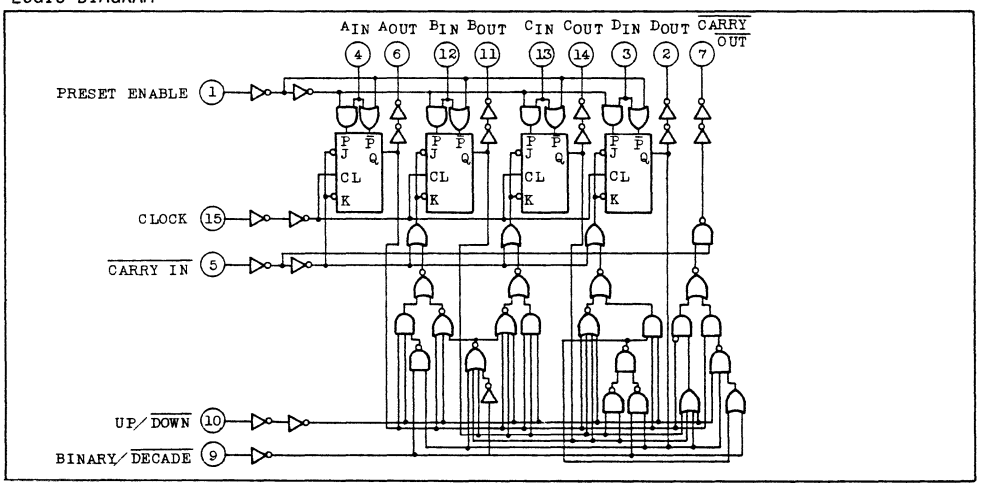
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	Tstg	-65 ~ 150	°C
Lead Temp./Time	Tsol	260°C · 10sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



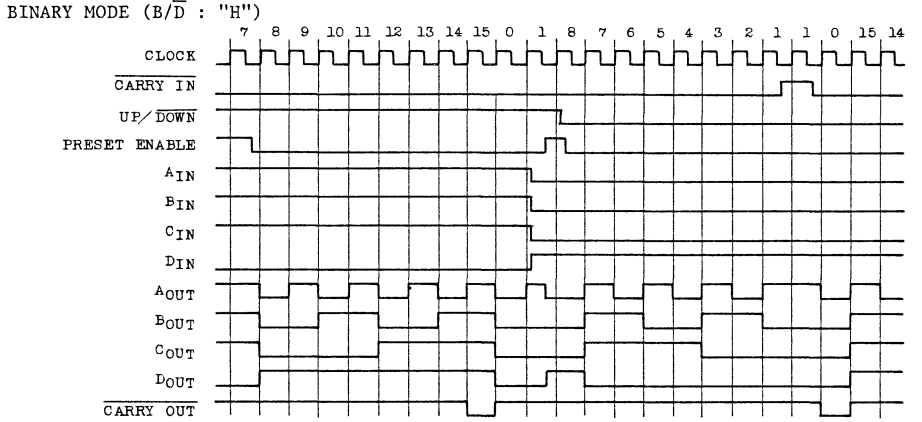
TC4029BP

RUTH TABLE

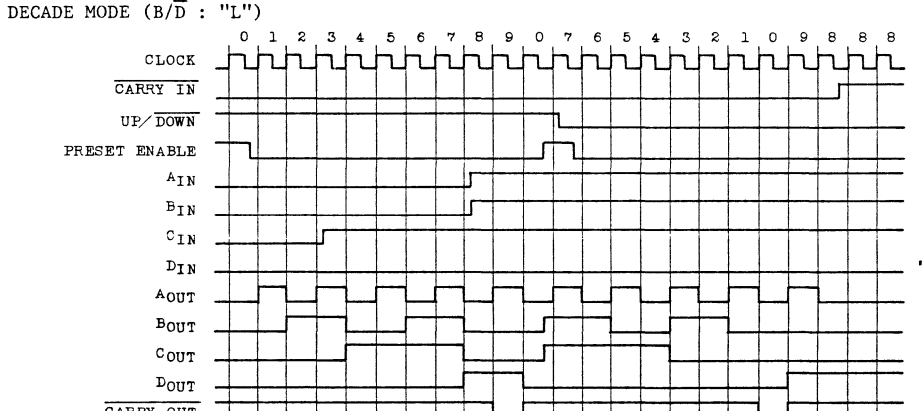
$\overline{\text{CARRY IN}}$	PRESET ENABLE	UP/$\overline{\text{DOWN}}$	BINARY/$\overline{\text{DECADE}}$	OPERATION	
L	L	H	*	UP COUNT	* Don't Care
L	L	L	*	DOWN COUNT	
*	H	*	*	PRESET	
H	L	*	*	NO COUNT	
L	L	*	H	BINARY COUNT	
L	L	*	L	DECADE COUNT	

IMING DIAGRAM

BINARY MODE (B/$\overline{\text{D}}$: "H")



DECADE MODE (B/$\overline{\text{D}}$: "L")



TC4029BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\| < 1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\| < 1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\| < 1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\| < 1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Quiescent Device Current	I_{DD}	V_{ID}=V_{SS},V_{DD}	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
		*	15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK-A,B,C,D_{OUT})	t_{pLH} t_{pHL}		5	-	250	500	ns
			10	-	100	200	
			15	-	70	180	
Propagation Delay Time (CLOCK-$\overline{\text{CARRY OUT}}$)	t_{pLH} t_{pHL}		5	-	360	720	ns
			10	-	145	290	
			15	-	100	200	
Propagation Delay Time (PRESET ENABLE -A,B,C,D_{OUT})	t_{pLH} t_{pHL}		5	-	240	480	ns
			10	-	90	200	
			15	-	65	160	
Propagation Delay Time (PRESET ENABLE -$\overline{\text{CARRY OUT}}$)	t_{pLH} t_{pHL}		5	-	350	700	ns
			10	-	130	290	
			15	-	90	210	
Propagation Delay Time ($\overline{\text{CARRY IN}}$ - $\overline{\text{CARRY OUT}}$)	t_{pLH} t_{pHL}		5	-	130	340	ns
			10	-	55	140	
			15	-	40	100	
Min. Clock Pulse Width	t_W		5	-	150	300	ns
			10	-	60	120	
			15	-	40	80	

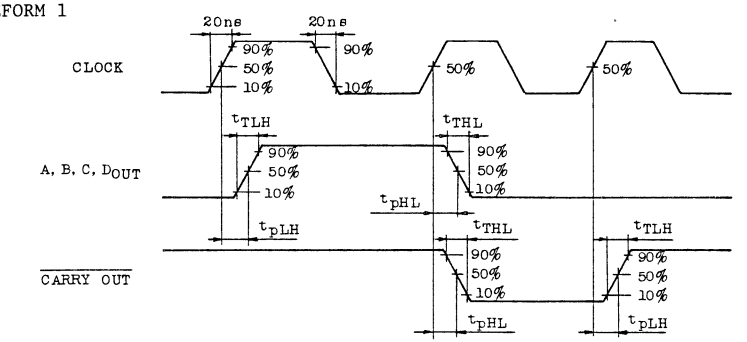
TC4029BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

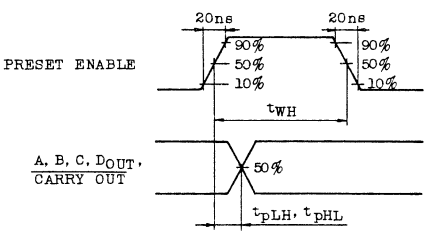
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Min. Pulse Width (PRESET ENABLE)	t_{WH}		5	-	80	160	ns
			10	-	25	70	
			15	-	10	50	
Max. Clock Frequency	f_{CL}		5	1.6	3.3	-	MHz
			10	4	8.6	-	
			15	5.5	12.8	-	
Max. Clock Input Rise Time. Max. Clock Input Fall Time.	t_{rCL} t_{fCL}		5	20	-	-	μs
			10	2.5	-	-	
			15	1.0	-	-	
Min. Set-up Time ($\overline{\text{CARRY IN}}$ - CLOCK)	t_{SU}		5	-	80	160	ns
			10	-	30	60	
			15	-	10	30	
Min. Set-up Time (B/$\overline{D}$, U/$\overline{D}$-CLOCK)	t_{SU}		5	-	170	340	ns
			10	-	65	130	
			15	-	45	90	
Min. Hold Time ($\overline{\text{CARRY IN}}$ - CLOCK)	t_H		5	-	-65	50	ns
			10	-	-20	30	
			15	-	-5	25	
Min. Removal Time (PRESET ENABLE-CLOCK)	t_{rem}		5	-	65	150	ns
			10	-	20	80	
			15	-	10	60	
Input Capacitance	C_{IN}			-	5	7.5	pF

WITCHING TIME TEST WAVEFORMS

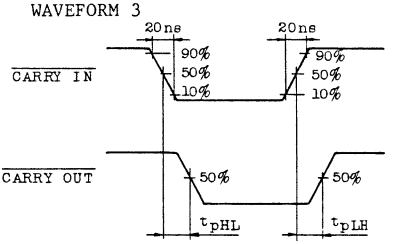
WAVEFORM 1



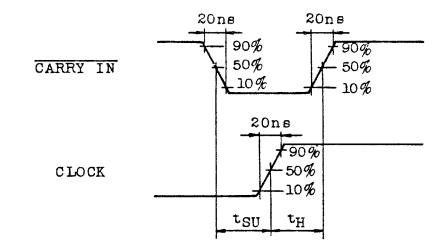
WAVEFORM 2



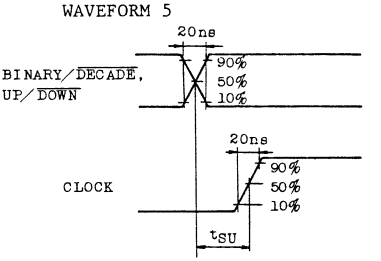
WAVEFORM 3



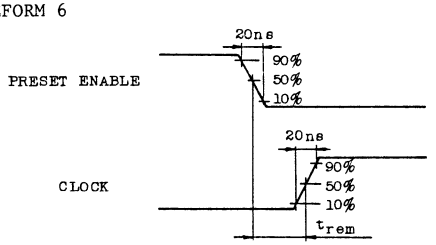
WAVEFORM 4



WAVEFORM 5



WAVEFORM 6



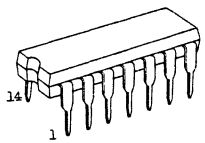
TC4030BP/BF

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

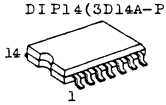
TC4030BP/TC4030BF QUAD EXCLUSIVE-OR GATE

TC4030 contains four circuits of exclusive OR gates. Since the buffers of two stage inverters are provided for all the outputs, the input/output voltage characteristic has been improved and the noise immunity has been also improved. And increase of transmission time due to load capacity increase is kept minimum.

Wide variety of applications are offerred, such as digital comparators and parity circuits.



DIP14(3D14A-P)

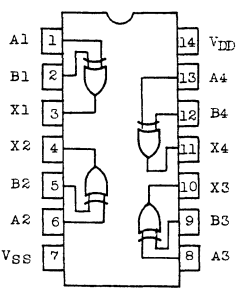


MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

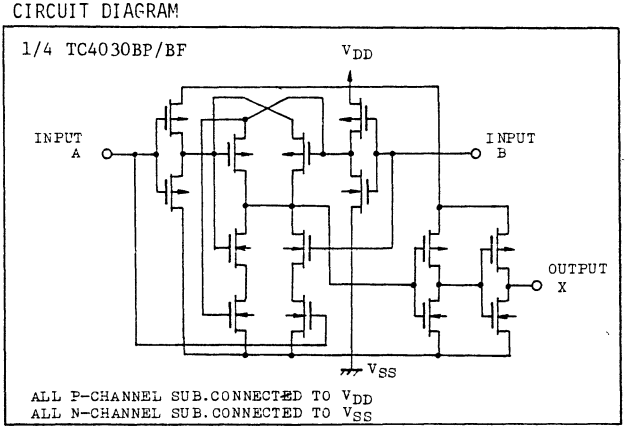
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ∿ 85	°C
Storage Temperature Range	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

CIRCUIT DIAGRAM



TRUTH TABLE

INPUTS		OUTPUT
A	B	X
L	L	L
L	H	H
H	L	H
H	H	L

:OMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
: Supply Voltage	V_{DD}		3	-	18	V
ıput Voltage	V_{IN}		0	-	V_{DD}	V

ATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

HARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
igh-Level ıtput Voltage	V_{OH}	$\|I_{OUT}\|$<1μA, $V_{IN}=V_{SS}$, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
ow-Level ıtput Voltage	V_{OL}	$\|I_{OUT}\|$<1μA, $V_{IN}=V_{SS}$, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
utput High urrent	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	mA
		V_{OH}=2.5V	5	-	-	-		-	-	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V	15	-1.4	-	-1.2		-	-1.0	-	
		$V_{IN}=V_{SS}$, V_{DD}									
utput Low urrent	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
		$V_{IN}=V_{SS}$, V_{DD}									
nput High oltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
nput Low oltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
put "H" Level rrent "L" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
uiescent evice Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}	5	-	1	-	0.001	1	-	7.5	μA
			10	-	2	-	0.001	2	-	15	
		*	15	-	4	-	0.002	4	-	30	

All valid input combinations.

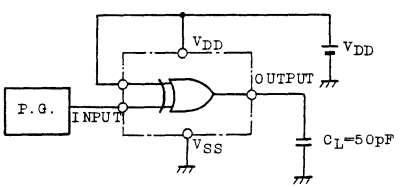
TC4030BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

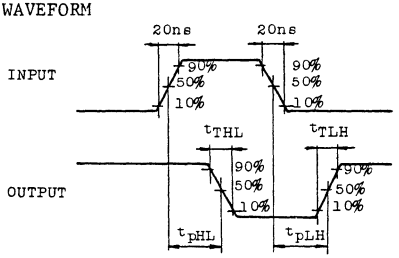
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNI
Output Transition Time (Low to High)	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Transition Time (High to Low)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time	t_{pLH} t_{pHL}		5	-	200	400	ns
			10	-	80	150	
			15	-	60	120	
Input Capacitance	C_{IN}			-	5	7.5	pF

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

CIRCUIT



WAVEFORM

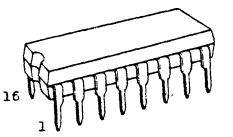


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4032BP
TC4038BP

032BP TRIPLE SERIAL ADDER (POSITIVE LOGIC ADDER)
038BP TRIPLE SERIAL ADDER (NEGATIVE LOGIC ADDER)

032BP and TC4038BP are tripple serial adders
ing common CLOCK input and CARRY RESET input to
the adders.
h adder has two SERIAL DATA inputs (An and
n=1 - 3), INVERT input and SUM output. When
'ERT input is "L", both TC4032BP and TC4038BP
form positive addition and when it is "H", negative
lition is performed.
:RY of TC4032BP is triggered by rising edge of
)CK and CARRY of TC4038BP is triggered by falling
;e of CLOCK.

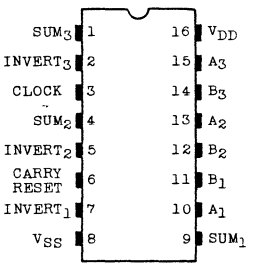


DIP16(3D16A-P)

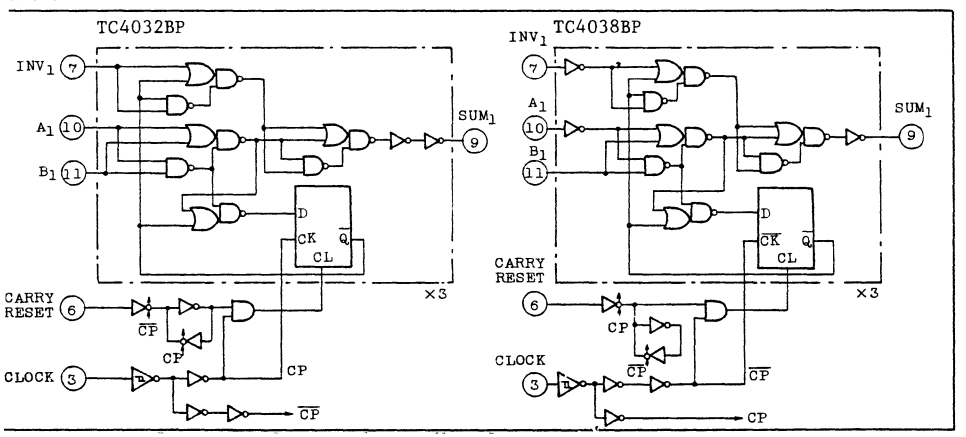
SOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
ɔut Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
:put Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
ɯer Dissipation	P_D	300	mW
ɛrating Temperature ŋge	T_A	-40 ~ 85	°C
ɔrage Temperature ŋge	T_{stg}	-65 ~ 150	°C
ad Temp./Time	T_{sol}	260°C . 10 sec	

PIN ASSIGNMENT



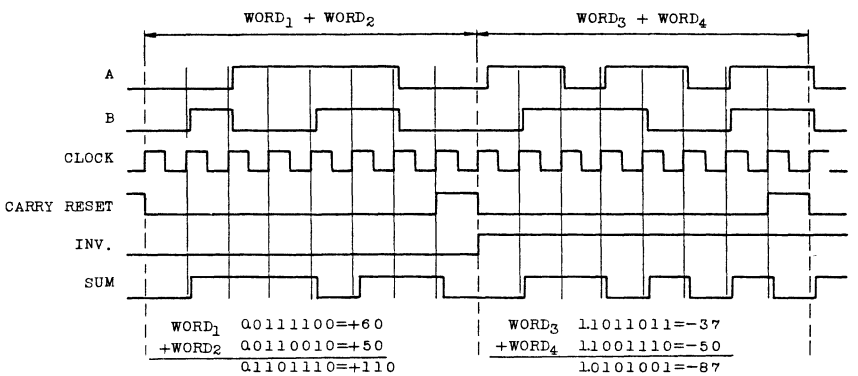
GIC DIAGRAM



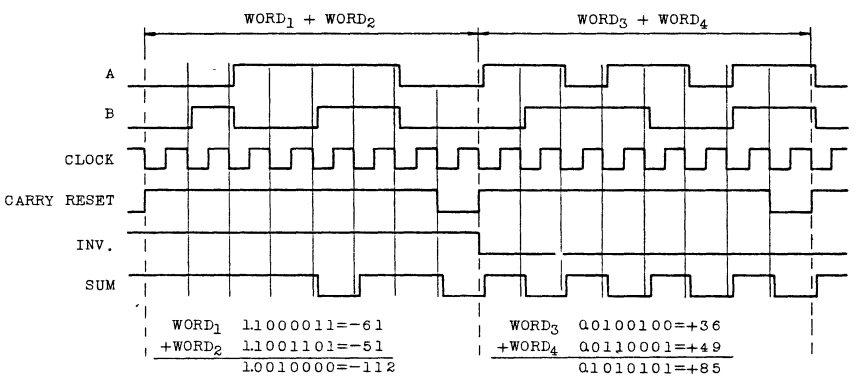
TC4032BP, TC4038BP

TIMING DIAGRAM

TC4032BP



TC4038BP



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

ITIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
h-Level put Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
-Level put Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
put High rent	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
:put Low :rent	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
ɔut High ltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
put Low ltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
put rrent "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
iescent Device rrent	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

All valid input combinations.

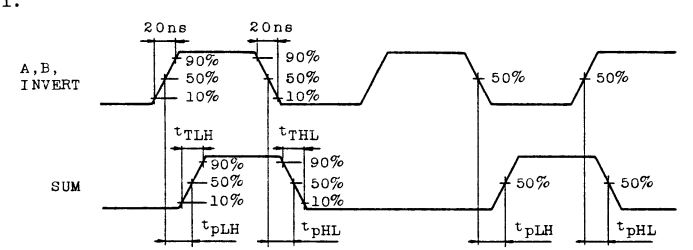
TC4032BP, TC4038BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - SUM)	t_{pLH} t_{pHL}		5	-	240	650	ns
			10	-	95	350	
			15	-	70	300	
Propagation Delay Time (A,B,INV - SUM)	t_{pLH} t_{pHL}		5	-	330	660	
			10	-	130	260	
			15	-	95	190	
Max. Clock Frequency	f_{CL}		5	2.5	5	-	MHz
			10	5	10	-	
			15	6	12	-	
Max. Clock Input Rise Time Max. Clock Input Fall Time	t_{rCL} t_{fCL}		5 10 15	No Limit			μs
Min. Set-up Time (A,B - CLOCK)	t_{SU}		5	-	80	200	ns
			10	-	30	80	
			15	-	20	60	
Input Capacitance	C_{IN}			-	5	7.5	pF

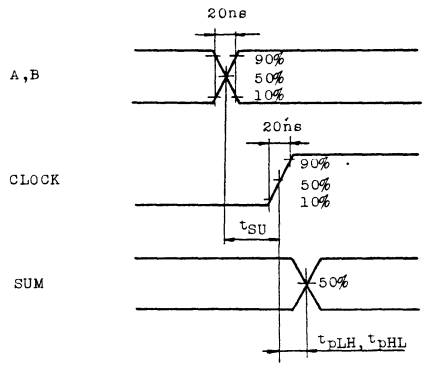
WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1.

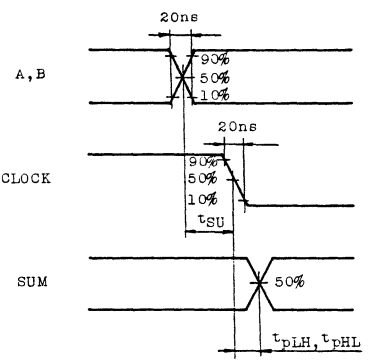


VEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS (Continued)

AVEFORM 2 (TC4032BP)



WAVEFORM 3 (TC4038BP)



TC4034BP

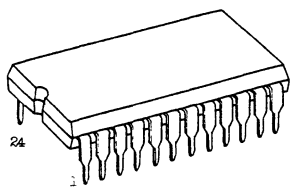
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4034BP 8-STAGE STATIC BIDIRECTIONAL PARALLEL/SERIAL INPUT/OUTPUT BUS REGISTER

TC4034BP is bidirectional 8 bit bus register having eight data input/output lines A_1 through A_8 and another set of eight data input/output lines B_1 through B_8. Switching of input/output for A data lines and B data lines is controlled by $A/\overline{B}$ input terminal and selection of serial operation/parallel operation is controlled by $P/\overline{S}$ input terminal.

(PARALLEL OPERATION)
When $P/\overline{S}$ input is placed at "H", synchronous or asynchronous parallel data can be input.

(SERIAL OPERATION)
When $P/\overline{S}$ input is placed at "L", serial data can be read synchronously.

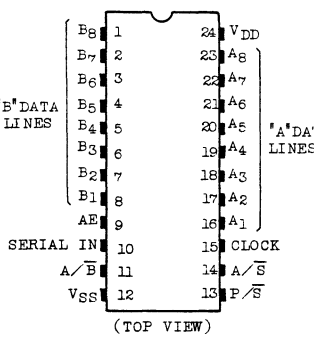


DIP 24(6D24A-P)

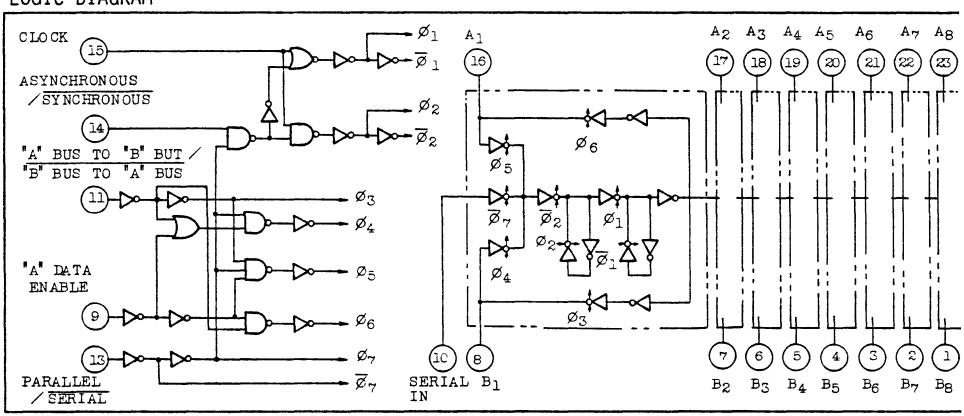
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

AE	P/$\overline{S}$	A/$\overline{B}$	A/$\overline{S}$	MODE	OPERATION
L	L	L	*	Serial	Synchronous Serial data input, "A" Parallel data outputs disabled
L	L	H	*	Serial	Synchronous Serial data input, "B" Parallel data output
L	H	L	L	Parallel	"B" Synchronous Parallel data inputs, "A" Parallel data outputs disabled
L	H	L	H	Parallel	"B" Asynchronous Parallel data inputs, "A" Parallel data outputs disabled
L	H	H	L	Parallel	"A" Parallel data inputs disabled, "B" Parallel data outputs, Synchronous data recirculation
L	H	H	H	Parallel	"A" Parallel data inputs disabled, "B" Parallel data outputs, Asynchronous data recirculation
H	L	L	*	Serial	Synchronous Serial data input, "A" Parallel data outputs
H	L	H	*	Serial	Synchronous Serial data input, "B" Parallel data outputs
H	H	L	L	Parallel	"B" Synchronous Parallel data inputs, "A" Parallel data outputs
H	H	L	H	Parallel	"B" Asynchronous Parallel data inputs, "A" Parallel data outputs
H	H	H	L	Parallel	"A" Synchronous Parallel data inputs, "B" Parallel data outputs
H	H	H	H	Parallel	"A" Asynchronous Parallel data inputs, "B" Parallel data outputs

* Don't care

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

TC4034BP

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{CC} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
3-State Output Leakage Current "H" Level	I_{DH}	V_{OUT}=18V	18	-	0.4	-	10^{-5}	0.4	-	12	μA
3-State Output Leakage Current "L" Level	I_{DL}	V_{OUT}=0V	18	-	-0.4	-	-10^{-4}	-0.4	-	-12	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	5	-	0.010	5	-	150	μA
			10	-	10	-	0.020	10	-	300	
			15	-	20	-	0.030	20	-	600	

* All valid input combinations.

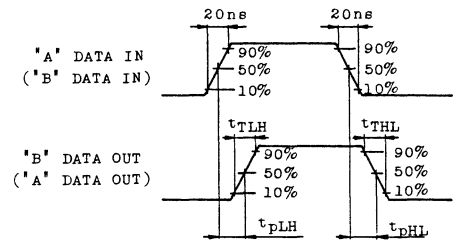
DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time $(A(B)_{IN} - B(A)_{OUT})$	t_{pLH} t_{pHL}		5	-	260	700	ns
			10	-	100	240	
			15	-	65	170	
Propagation Delay Time $(AE - A_{OUT})$	t_{pLZ} t_{pZL} t_{pHZ} t_{pZH}	R_L=1kΩ	5	-	130	400	ns
			10	-	55	160	
			15	-	30	120	
Max. Clock Frequency	f_{CL}		5	1.4	2.9	-	MHz
			10	3.5	7.1	-	
			15	5.1	10.2	-	
Max. Clock Input Rise Time Max. Clock Input Fall Time	t_{rCL} t_{fCL}		5	20	-	-	μs
			10	2.5	-	-	
			15	1.0	-	-	
Min. Clcok Pulse Width	t_W		5	-	175	350	ns
			10	-	70	140	
			15	-	50	100	
Min. Pulse Width (AE, P/$\overline{S}$, A/$\overline{S}$)	t_{WH}		5	-	145	290	ns
			10	-	55	110	
			15	-	40	80	
Min. Set-up Time (SERIAL IN - CLOCK)	t_{SU}		5	-	80	160	ns
			10	-	30	60	
			15	-	20	40	
Min. Set-up Time $(A(B)_{IN}$ - CLOCK)	t_{SU}		5	-	60	150	ns
			10	-	20	50	
			15	-	10	25	
Input Capacitance	C_{IN}			-	5	7.5	pF

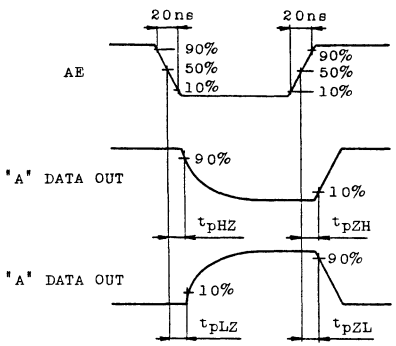
TC4034BP

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

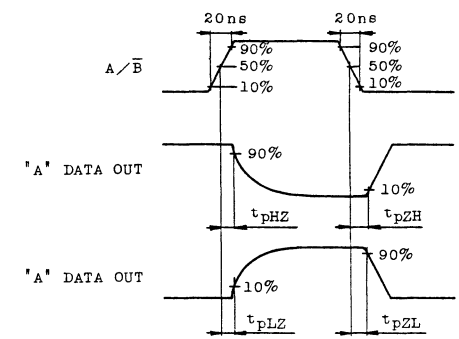
WAVEFORM 1.



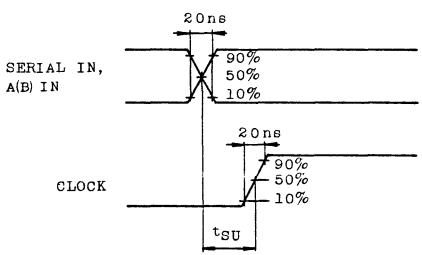
WAVEFORM 2.



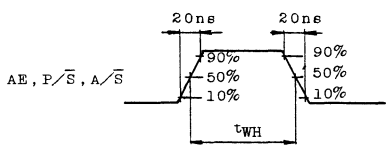
WAVEFORM 3. (AE="H")



WAVEFORM 4.



WAVEFORM 5.

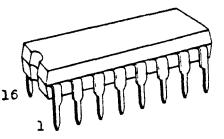


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4035BP

TC4035BP 4-STAGE PARALLEL IN/PARALLEL OUT SHIFT REGISTER

TC4035BP is 4 bit shift register having SERIAL mode and PARALLEL mode.
When PARALLEL/$\overline{\text{SERIAL}}$ CONTROL input is placed at "H", the parallel mode operation is designated and when it is placed at "L", the serial mode operation having J,$\overline{\text{K}}$ logical inputs is designated.
The outputs are changed by rising edge of CLOCK input for both modes. When TRUE/$\overline{\text{COMPLEMENT}}$ Terminal is placed at "H", non-inverted signal is output and when it is placed at "L", inverted signal is output.
When RESET input is placed at "H", the content of register is reset regardless of other inputs.
In the case of SERIAL input, J and $\overline{\text{K}}$ are connected for the data inputs.

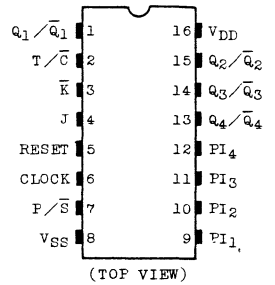


DIP 16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

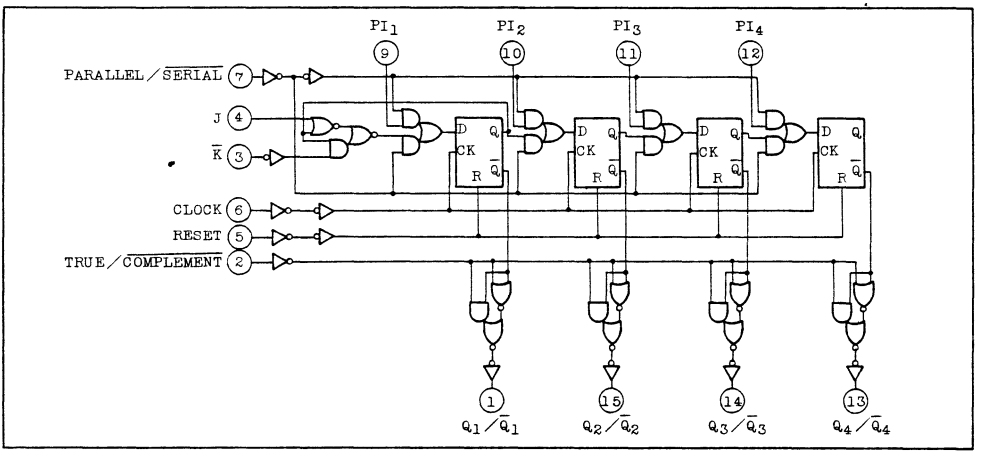
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



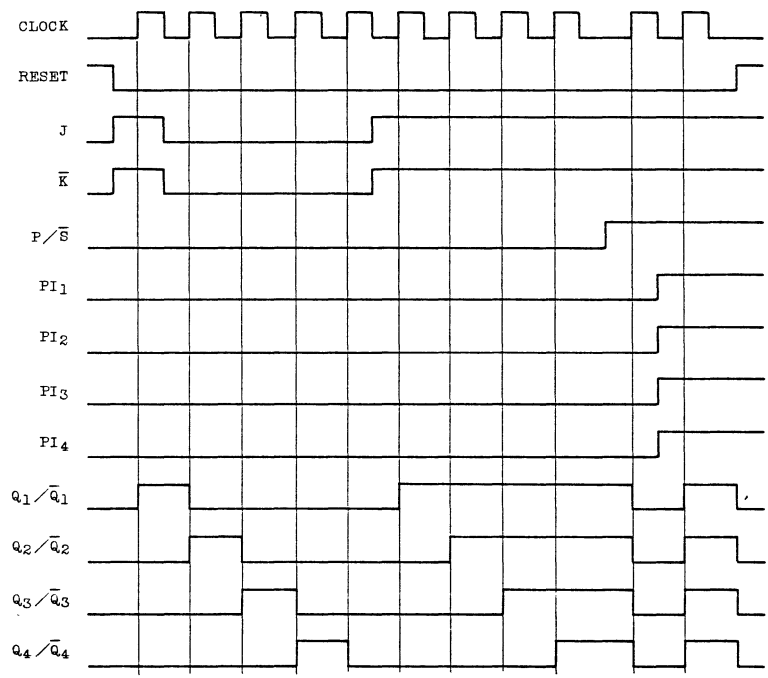
TC4035BP

TRUTH TABLE

INPUTS							OUTPUTS (T/$\overline{C}$="H")		OUTPUTS (T/$\overline{C}$="L")	
RESET	CLOCK$^{\Delta}$	P/$\overline{S}$	J	$\overline{K}$	PI_1	PI_n	$Q_1/\overline{Q}_1$	$Q_n/\overline{Q}_n$	$Q_1/\overline{Q}_1$	$Q_n/\overline{Q}_n$
H	*	*	*	*	*	*	L	L	H	H
L	↓	H	*	*	L	L	L	L	H	H
L	↓	H	*	*	H	H	H	H	L	L
L	↓	L	L	L	*	*	L	Q_{n-1}	H	$\overline{Q_{n-1}}$
L	↓	L	L	H	*	*	$Q_1^{\cdot}$		$\overline{Q}_1^{\cdot}$	
L	↓	L	H	L	*	*	$\overline{Q}_1^{\cdot\cdot}$		$Q_1^{\cdot\cdot}$	
L	↓	L	H	H	*	*	H		L	
L	↑	*	*	*	*	*	$Q_1^{\cdot}$	$Q_n^{\cdot}$	$\overline{Q}_1^{\cdot}$	$\overline{Q}_n^{\cdot}$

* Don't care
Δ Level change
. No change
.. Change
n:2~4

TIMING DIAGRAM (T/$\overline{C}$="H").



TC4035BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	μA
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

TC4035BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

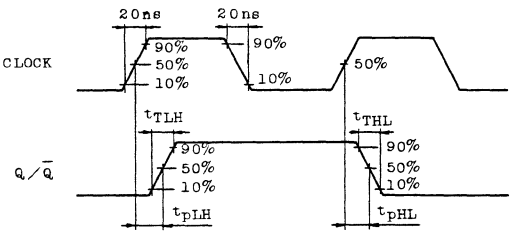
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Trnasition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q/$\overline{Q}$)	t_{pLH} t_{pHL}		5	-	190	500	ns
			10	-	75	200	
			15	-	55	150	
Propagation Delay Time (RESET - Q/$\overline{Q}$)	t_{pLH} t_{pHL}		5	-	160	460	ns
			10	-	65	200	
			15	-	45	160	
Max. Clock Frequency	f_{CL}		5	2	4	-	MHz
			10	6	12	-	
			15	8	16	-	
Max. Clock Input Rise Time. Max. Clock Input Fall Time	t_{rCL} t_{fCL}		5	20	-	-	μs
			10	2.5	-	-	
			15	1.0	-	-	
Min. Clock Pulse Width	t_w		5	-	125	250	ns
			10	-	45	90	
			15	-	30	60	
Min. Pulse Width (RESET)	t_{WH}		5	-	110	250	ns
			10	-	45	110	
			15	-	30	80	
Min. Set-up Time (J,$\overline{K}$ - CLOCK)	t_{SU}		5	-	55	220	ns
			10	-	20	80	
			15	-	15	60	
Min. Set-up Time (PI - CLCOK)	t_{SU}		5	-	40	140	ns
			10	-	15	50	
			15	-	10	40	

YNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

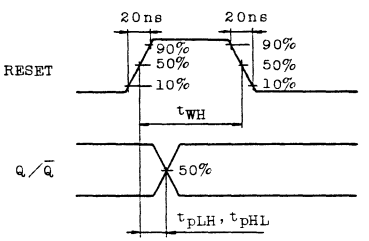
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
in. Set-up Time (P/$\overline{S}$ - CLOCK)	t_{SU}		5	-	40	500	ns
			10	-	15	200	
			15	-	10	150	
nput Capacitance	C_{IN}			-	5	7.5	pF

AVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

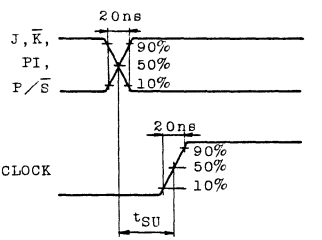
WAVEFORM 1.



WAVEFORM 2.



WAVEFORM 3.



TC4036BP
TC4039BP

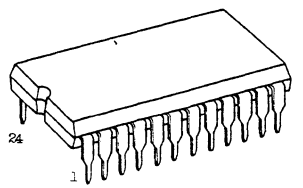
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4036BP 4 WORD × 8 BIT STATIC RAM (BINARY ADDRESSING)
TC4039BP 4 WORD × 8 BIT STATIC RAM (DIRECT WORD-LINE ADDRESSING)

TC4036BP/TC4039BP are static RAM of 4 × 8 bits and since eight data input/output lines are mutually independently provided for one word, wide variety of applications are expected for scratch pad memories, channel preset memories of digital frequency synthesizer systems, etc.

TC4036BP Each word is binarily selected by two lines of address inputs A_0 and A_1.

TC4039BP Each word is directly selected by mutually independent four lines of address inputs WORD 1 through WORD 4.

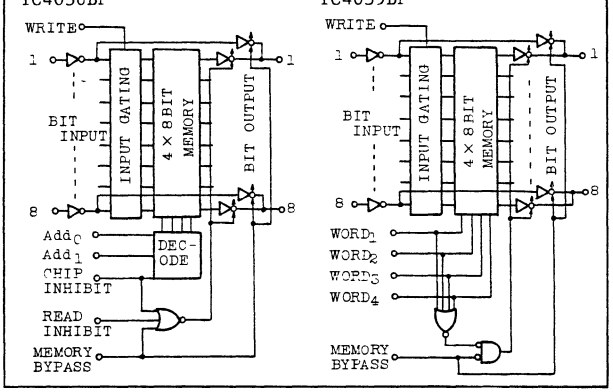


DIP 24 (6D24A-P)

ABSOLUTE MAXIMUM RATINGS

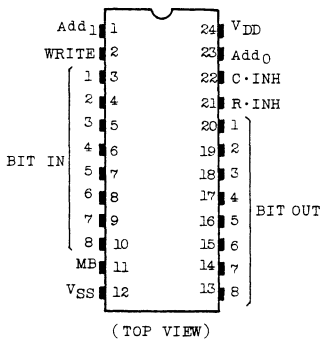
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

BLOCK DIAGRAM



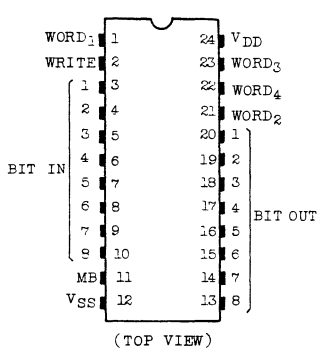
PIN ASSIGNMENT

TC4036BP



(TOP VIEW)

TC4039BP



(TOP VIEW)

UNCTION TABLE

TC4036BP

WRITE	READ INHIBIT	MEMORY BYPASS	CHIP INHIBIT	OPERATIONAL MODEL
*	*	L	H	Each bit output has high impedance generating floating condition. Writing into the memory is not performed.
*	*	H	H	Bit input data is directly output to the corresponding bit output. The memory retains the content of bit input data written in previous write mode.
L	*	H	L	
H	*	H	L	Bit input data is directly output to the corresponding bit output. But input data is written into the word memory designated by address inputs A_0 and A_1.
L	L	L	L	Memory data is read from the word designated by address inputs A_0 and A_1. Writing into the memory is not performed.
L	H	L	L	Each bit output has high impedance generating floating condition. Writing into the memory is not performed.
H	L	L	L	As well as each bit input data is written into the word memory designated by address inputs A_0 and A_1, the input data is read out.
H	H	L	L	Each bit output has high impedance generating floating condition. Each bit input data is written into the word memory designated by address inputs A_0 and A_1.

TC4039BP

WRITE	MEMORY BYPASS	WORD1 ~ WORD4	OPERATIONAL MODE
*	L	all L	Each bit output has high impedance generating floating condition. The memory retains the content of bit input data written in previous write mode.
*	H	all L	Bit input data is directly output to the corresponding bit output. The memory retains the content of bit input data written in previous write mode.
L	H	△△	
H	H	△△	Bit input data is directly output to the corresponding bit output. Each bit input data is written into the memory designated by the word input.
L	L	△△	Memory data designated by the word input is read out. Writing into the memory is not performed.
H	L	△△	As well as each bit input data is written into the memory designated by the word input, the input data is read out.

* Don't care △△ Only one WORD input has "H" level.

TC4036BP, TC4039BP

ADDRESS TRUTH TABLE

TC4036BP

Add_1	Add_0	ADDRESSED WORD
L	L	WORD 1
L	H	WORD 2
H	L	WORD 3
H	H	WORD 4

TC4039BP

WORD 1	WORD 2	WORD 3	WORD 4	ADDRESSED WORD
H	L	L	L	WORD 1
L	H	L	L	WORD 2
L	L	H	L	WORD 3
L	L	L	H	WORD 4
L	L	L	L	NONE
OTHER STATES				*

* Inhibit mode

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS}, V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS}, V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS}, V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS}, V_{DD}$									

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
nput High oltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
nput Low oltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
nput urrent	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
-State utput eakage urrent	"H" Level	I_{DH}	V_{OUT}=18V	18	-	0.4	-	10^{-4}	0.4	-	12	μA
	"L" Level	I_{DL}	V_{OUT}=0V	18	-	-0.4	-	-10^{-4}	-0.4	-	-12	
uiescent Device urrent		I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
				10	-	10	-	0.010	10	-	300	
				15	-	20	-	0.015	20	-	600	

* All valid input combinations.

YNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
utput Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
utput Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	

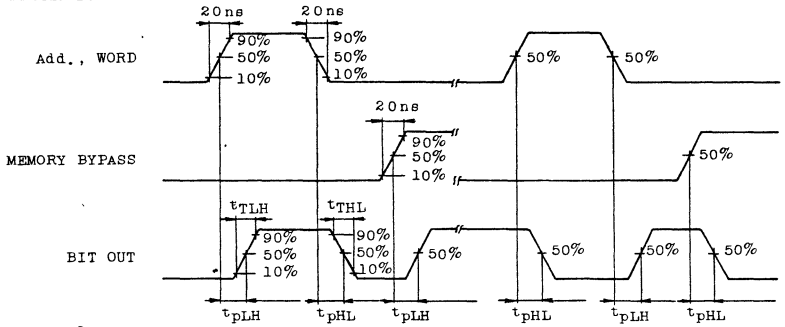
TC4036BP, TC4039BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

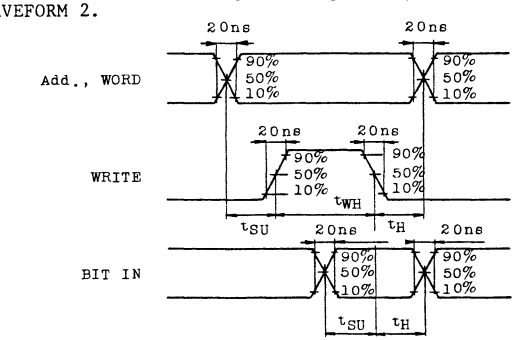
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (R·INH - BIT OUT) (TC4036BP)	t_{pZL} t_{pZH}	R_L=1kΩ	5	-	200	750	ns
			10	-	90	350	
			15	-	70	300	
Propagation Delay Time (C·INH - BIT OUT) (TC4036BP)	t_{pZL} t_{pZH}	R_L=1kΩ	5	-	250	750	ns
			10	-	120	350	
			15	-	90	300	
Propagation Delay Time (M·B - BIT OUT)	t_{pLH} t_{pHL}		5	-	210	750	ns
			10	-	100	350	
			15	-	80	300	
Propagation Delay Time (Add.WORD - BIT OUT)	t_{pLH} t_{pHL}		5	-	260	750	ns
			10	-	110	350	
			15	-	80	300	
Min. Set-up Time (Add. WORD - WRITE)	t_{SU}		5	-	45	200	ns
			10	-	25	110	
			15	-	20	60	
Min. Hold Time (Add. WORD - WRITE)	t_H		5	-	-60	100	ns
			10	-	-35	70	
			15	-	-25	40	
Min. Pulse Width (WRITE)	t_{WH}		5	-	60	150	ns
			10	-	20	60	
			15	-	15	50	
Min. Set-up Time (BIT IN - WRITE)	t_{SU}		5	-	-20	100	ns
			10	-	-15	50	
			15	-	-10	40	
Min. Hold Time (BIT IN - WRITE)	t_H		5	-	40	200	ns
			10	-	25	90	
			15	-	20	60	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

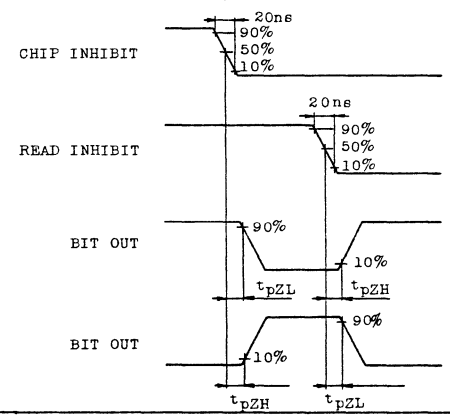
WAVEFORM 1.



WAVEFORM 2.



WAVEFORM 3. (TC4036BP)

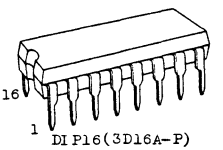


TC4040BP/BF

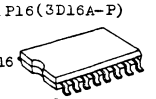
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4040BP/TC4040BF 12 STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDERS

TC4040BP/BF is 12 stage ripple-carry binary counter with the asynchronous clear function.
The counter advances its counting state by falling edge of $\overline{CLOCK}$ input. When RESET input is placed at "H", all the circuits are reset making all the outputs (Q1 through Q12) to be "L" regardless of $\overline{CLOCK}$ input.
This is most suitable for frequency dividers, control circuits and timing circuits.



DIP16(3D16A-P)

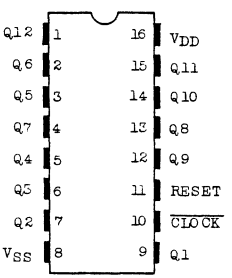


MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNITS
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ∿ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ∿ 85	°C
Storage Temperature Range	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



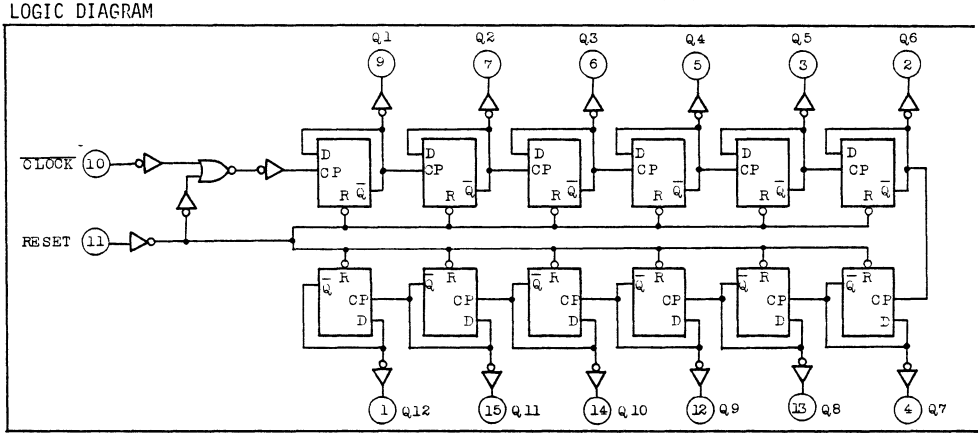
(TOP VIEW)

TRUTH TABLE

CLOCK △	RESET	OUTPUT STAGE
*	H	ALL OUTPUTS = "L"
↓	L	NO CHANGE
↓	L	ADVANCE TO NEXT STAGE

△: LEVEL CHANGE *: DON'T CARE

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS}$, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS}$, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	mA
		V_{OH}=2.5V	5	-	-	-		-	-	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V	15	-1.4	-	-1.2		-	-1.0	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}	5	-	20	-	0.005	20	-	150	μA
			10	-	40	-	0.010	40	-	300	
		*	15	-	80	-	0.015	80	-	600	

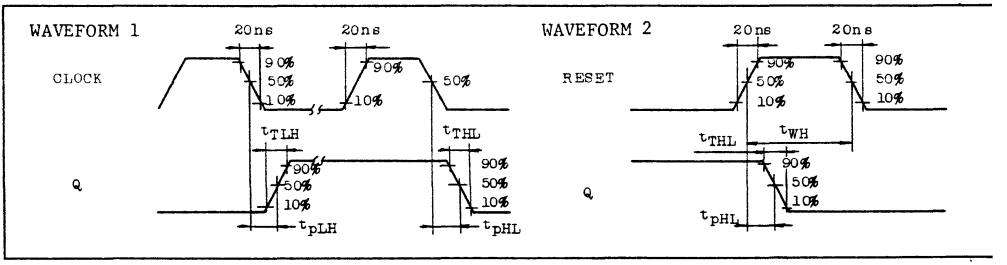
* All valid input combinations.

TC4040BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	100	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time ($\overline{CLOCK}$ - Q1)	t_{pLH}		5	-	160	360	
			10	-	80	160	
			15	-	65	130	
Propagation Delay Time ($\overline{CLOCK}$ - Q1)	t_{pHL}		5	-	160	360	
			10	-	80	160	
			15	-	65	130	
Propagation Delay Time ($\overline{CLOCK}$ - Q12)	t_{pLH}		5	-	900	1800	ns
			10	-	450	900	
			15	-	360	720	
Propagation Delay Time ($\overline{CLOCK}$ - Q12)	t_{pHL}		5	-	900	1800	
			10	-	450	900	
			15	-	360	720	
Propagation Delay Time (RESET - Q)	t_{pHL}		5	-	150	280	ns
			10	-	70	120	
			15	-	50	100	
Max. Clock Frequency	f_{CL}		5	3.5	10	-	MHz
			10	8	20	-	
			15	12	25	-	
Min. Pulse Width (RESET)	t_{WH}		5	-	100	200	ns
			10	-	40	80	
			15	-	30	60	
Max. Clock Input Rise Time	t_{rCL}		5	20	-	-	μs
Max. Clock Input Fall Time	t_{fCL}		10	2.5	-	-	
			15	1.0	-	-	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

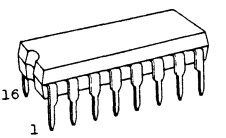
TC4042BP/BF

C4042BP/TC4042BF QUAD CLOCKED "D" LATCH

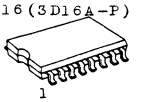
TC4042BP/BF contains four circuits of "D" type latches having common CLOCK input and POLARITY input.

When POLARITY input is placed at "H" level, D input appears as it is at Q output during CLOCK input stays high and D input at the time of falling edge of CLOCK input is retained at Q output. As long as CLOCK input stays low, Q output is not changed even when D input varies.

When POLARITY input is placed "L", D input appears as it is at Q output during CLOCK input stays at "L" level and the latch operation is seen as long as CLOCK input is "H".



DIP16(3D16A-P)

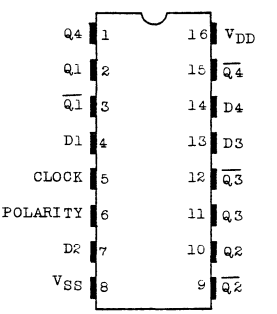


MFP16(F16GC-P)

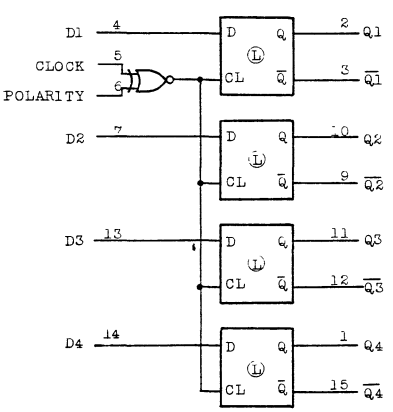
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNITS
DC Supply Voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input Voltage	V_{IN}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output Voltage	V_{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



BLOCK DIAGRAM



TRUTH TABLE

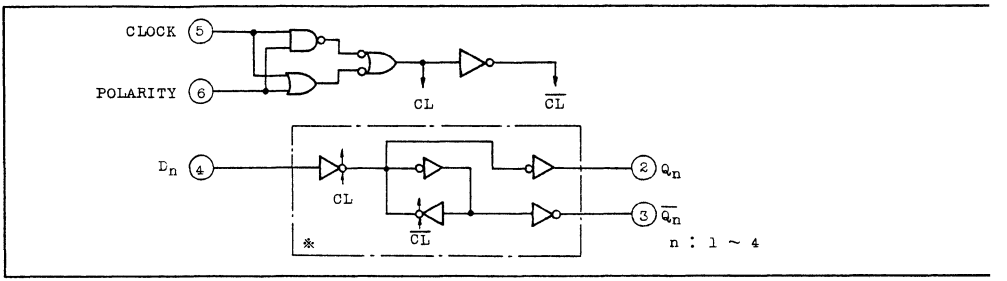
INPUTS		OUTPUT
CLOCK△	POLARITY	Q_n•
H	H	D_n
L	L	D_n
↑	L	LATCH
↓	H	LATCH

△ Level Change

• : 1 ~ 4

TC4042BP/BF

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage			0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$ <1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS}$, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$ <1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS}$, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	mA
		V_{OH}=2.5V									
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V									
		$V_{IN}=V_{SS}$, V_{DD}	15	-1.4	-	-1.2		-	-1.0	-	
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V									
		$V_{IN}=V_{SS}$, V_{DD}	15	3.6	-	3.0		-	2.4	-	
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V									
		$\|I_{OUT}\|$ <1μA	15	11.0	-	11.0	8.25	-	11.0	-	
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V									
		$\|I_{OUT}\|$ <1μA	15	-	4.0	-	6.75	4.0	-	4.0	

STATIC ELECTRICAL CHARACTERISTICS (Continued)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	uA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS}, V_{DD}	5	-	20	-	0.005	20	-	150	
				10	-	40	-	0.010	40	-	300	
			*	15	-	80	-	0.015	80	-	600	

* All valid input combinations.

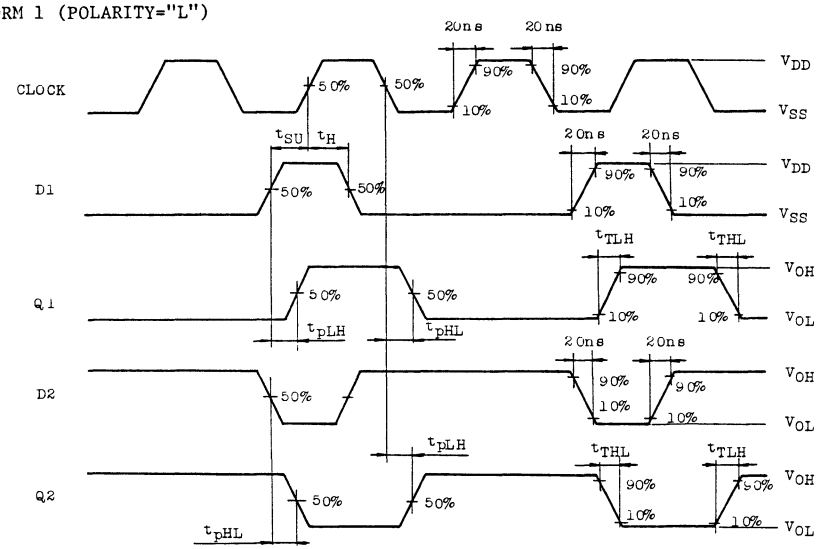
DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Transition Time (High to Low)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	t_{pLH}		5	-	400	800	
			10	-	170	350	
			15	-	140	300	
Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	t_{pHL}		5	-	370	800	
			10	-	150	350	
			15	-	125	300	
Propagation Delay Time (DATA - Q, $\overline{Q}$)	t_{pLH}		5	-	200	400	
			10	-	80	200	
			15	-	60	150	
Propagation Delay Time (DATA - Q, $\overline{Q}$)	t_{pHL}		5	-	180	400	
			10	-	75	200	
			15	-	55	150	
Min. Clock Pulse Width	t_w		5	-	150	300	
			10	-	70	150	
			15	-	60	120	
Min. Hold Time (DATA - CLOCK)	t_H		5	-	-50	50	
			10	-	-20	20	
			15	-	0	20	
Min. Set-up Time (DATA - CLOCK)	t_{SU}		5	-	50	150	
			10	-	20	60	
			15	-	0	30	
Input Capacitance	C_{IN}	D Input		-	5	7.5	pF
		CLOCK/POLARITY Input		-	8	15	

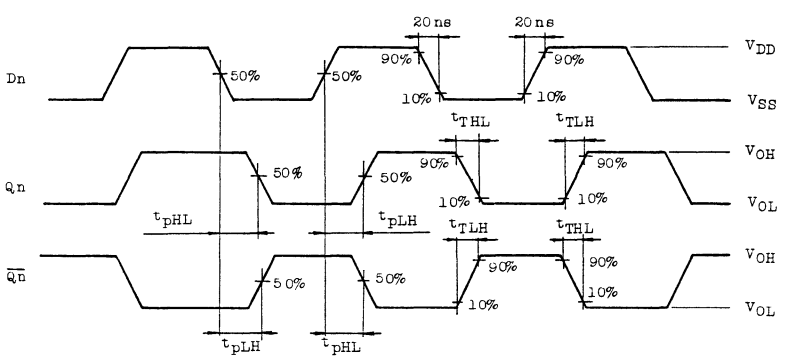
TC4042BP/BF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1 (POLARITY="L")



WAVEFORM 2 (CLOCK=POLARITY="H")

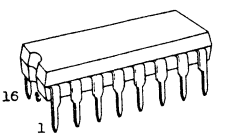


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4043BP

'C4043BP QUAD 3-STATE R/S LATCH (Quad NOR R/S Latch)

'C4043BP is the latches composed by four independent :/S flip-flop circuits. TC4043BP fabricated with NOR ;ates is suitable for data processing of four bits :onfiguration. Four output lines can have high .mpedance regardless of the contents of latches by ieans of common ENABLE input to make connection to :he bus lines easy.

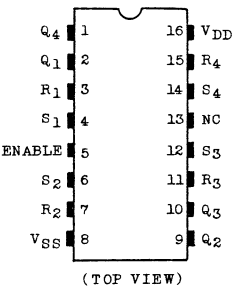


DIP16 (3D16A-P)

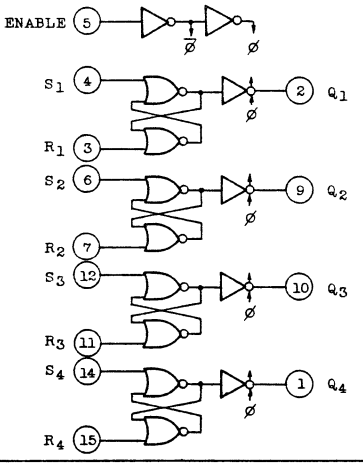
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
)C Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
.nput Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
)utput Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
)C Input Current	I_{IN}	±10	mA
'ower Dissipation	P_D	300(DIP)/180(MFP)	mW
)perating Temperature :ange	T_A	-40 ~ 85	°C
;torage Temperature :ange	T_{stg}	-65 ~ 150	°C
.ead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



.OGIC DIAGRAM



TRUTH TABLE

S	R	E	Q
*	*	L	HZ
L	L	H	No Change
L	H	H	L
H	L	H	H
H	H	H	H

* : Don't Care

HZ : High Impedance

TC4043BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

'ATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

:HARACTERISTIC		SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
·State ıtput :akage ırrent	"H" Level	I_{DH}	V_{OH}=18V	18	-	0.4	-	10^{-4}	0.4	-	12	μA
	"L" Level	I_{DL}	V_{OL}=0V	18	-	-0.4	-	-10^{-4}	-0.4	-	-12	
ıiescent Device ırrent		I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	1	-	0.002	1	-	30	μA
				10	-	2	-	0.004	2	-	60	
				15	-	4	-	0.008	4	-	120	

All valid input combinations.

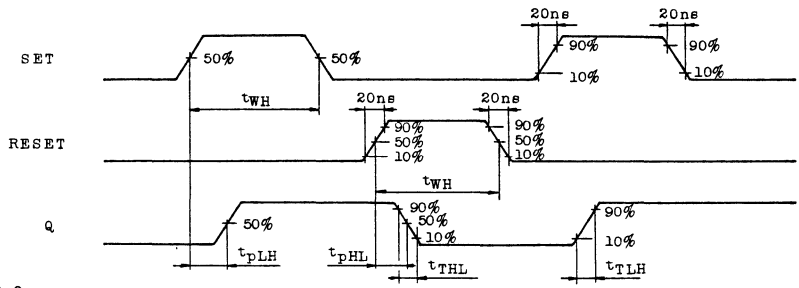
'NAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
ıtput Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
ıtput Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
ropagation Delay Time (SET, RESET - Q)	t_{pLH} t_{pHL}		5	-	150	300	ns
			10	-	60	140	
			15	-	40	100	
-State ropagation Delay Time (ENABLE - Q)	t_{pHZ} t_{pZH}	R_L=1kΩ	5	-	60	230	ns
			10	-	25	110	
			15	-	20	80	
-State ropagation Delay Time (ENABLE - Q)	t_{pLZ} t_{pZL}	R_L=1kΩ	5	-	80	180	
			10	-	35	100	
			15	-	25	70	
in. Pulse Width (SET, RESET)	t_{WH}		5	-	30	160	ns
			10	-	15	80	
			15	-	10	40	
nput Capacitance	C_{IN}			-	5	7.5	pF

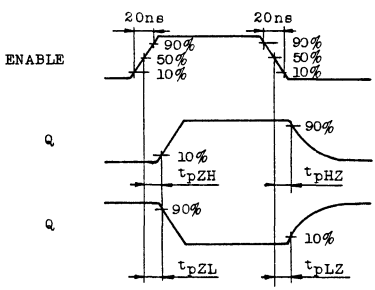
TC4043BP

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1.



WAVEFORM 2.



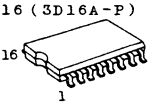
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4044BP/BF

C4044BP/TC4044BF QUAD 3-STATE R/S LATCH (Quad NAND R/S Latch)

C4044BP/BF the latches composed by four independent /S flip-flop circuits. TC4044BP/BF fabricated with AND gates is suitable for data processing of four its configuration. Four output lines can have high mpedance regardless of the contents of latches by eans of common ENABLE input to make connection to he bus lines easy.

DIP16 (3D16A-P)

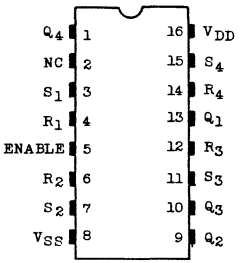


MFP16 (F16GC-P)

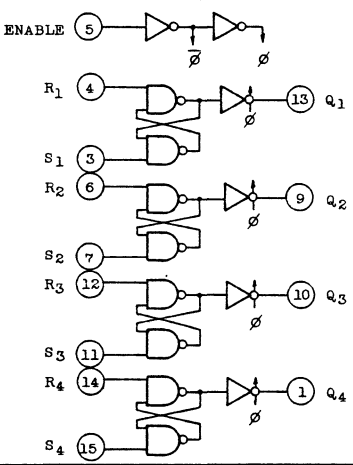
BSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
C Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
nput Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
utput Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
C Input Current	I_{IN}	±10	mA
ower Dissipation	P_D	300(DIP)/180(MFP)	mW
perating Temperature ange	T_A	-40 ~ 85	°C
torage Temperature ange	T_{stg}	-65 ~ 150	°C
ead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



OGIC DIAGRAM



TRUTH TABLE

R	S	E	Q
*	*	L	HZ
L	L	H	L
L	H	H	L
H	L	H	H
H	H	H	No Change

* : Don't Care

HZ : High Impedance

TC4044BP/BF

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
				10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
				10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16	-	-	-0.12	-	mA
			V_{OH}=2.5V	5	-	-	-	-	-	-	-	
			V_{OH}=9.5V	10	-0.5	-	-0.4	-	-	-0.3	-	
			V_{OH}=13.5V	15	-1.4	-	-1.2	-	-	-1.0	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44	-	-	0.36	-	
			V_{OL}=0.5V	10	1.3	-	1.1	-	-	0.9	-	
			V_{OL}=1.5V	15	3.6	-	3.0	-	-	2.4	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

ATIC ELECTIRCAL CHARACTERISTICS (V_{SS}=0V)

HARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
State tput	"H" Level	I_{DH}	V_{OH}=18V	18	-	0.5	-	10^{-4}	0.5	-	30	μA
akage rrent	"L" Level	I_{DL}	V_{OL}=0V	18	-	-0.5	-	-10^{-4}	-0.5	-	-30	μA
uiescent evice Current		I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	4	-	0.002	4	-	30	μA
				10	-	8	-	0.004	8	-	60	
				15	-	16	-	0.008	16	-	120	

All valid input combinations.

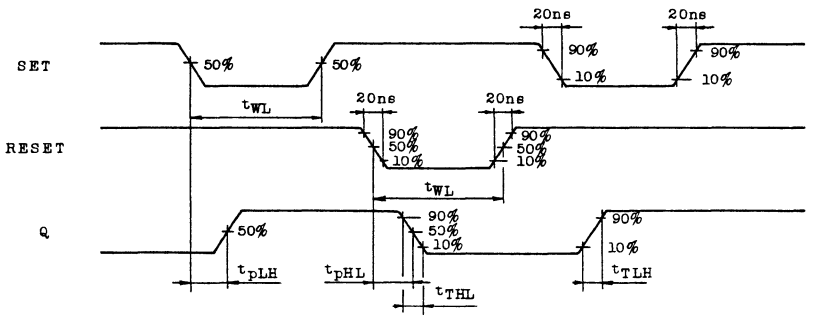
NAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
utput Transition Time (Low to High)	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
utput Transition Time (High to Low)	t_{THL}		5	-	230	200	
			10	-	5-	100	
			15	-	40	80	
ropagation Delay Time (SET, RESET - Q)	t_{pLH} t_{pHL}		5	-	230	460	
			10	-	110	220	
			15	-	75	150	
ropagation Delay Time (SET, RESET - Q)	t_{pLH} t_{pHL}		5	-	180	360	
			10	-	90	180	
			15	-	60	120	
-State ropagation Delay Time (ENBLE - Q)	t_{pHZ}	R_L=1kΩ	5	-	100	250	
			10	-	80	200	
			15	-	75	160	
-State ropagation Delay Time (ENABLE - Q)	t_{pLZ}	R_L=1kΩ	5	-	130	300	
			10	-	90	250	
			15	-	80	200	
-State ropagation Delay Time (ENABLE - Q)	t_{pZH}	R_L=1kΩ	5	-	100	250	
			10	-	60	200	
			15	-	50	160	
-State ropagation Delay Time (ENABLE - Q)	t_{pZL}	R_L=1kΩ	5	-	140	300	
			10	-	80	250	
			15	-	70	200	
in. Pulse Width (SET)	t_{WL}		5	-	105	200	
			10	-	50	100	
			15	-	40	80	
in. Pulse Width (RESET)	t_{WL}		5	-	120	200	
			10	-	55	100	
			15	-	45	80	
nput Capacitance	C_{IN}			-	5	7.5	pF

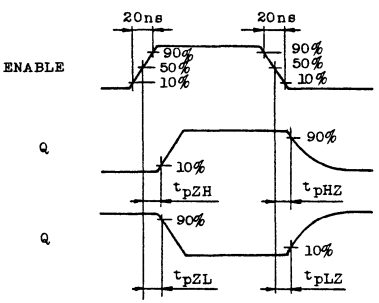
TC4044BP/BF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1.



WAVEFORM 2.

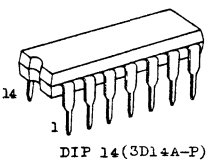


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4047BP

TC4047BP LOW-POWER MONOSTABLE/ASTABLE MULTIVIBRATOR

TC4047BP is the multivibrator equipped with both astable function and mono-stable function, and retrigger operation and reset operation are also achievable.
For both operational modes, the pulse width can be varied by externally connected capacitor (C) and resistor (R).
Establish RETRIG="L". +TRIG="L", -TRIG="H" for astable operation and AST="L", $\overline{AST}$="H" for mono-stable operation. (Refer to FUNCTION TABLE and OPERATING CONSIDERATIONS).
When EXTERNAL RESET input is set at "H", both operational modes of astable and mono-stable operations are reset to Q="L" and $\overline{Q}$="H".

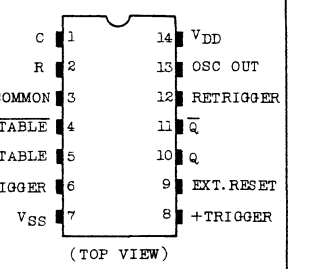


DIP 14(3D14A-P)

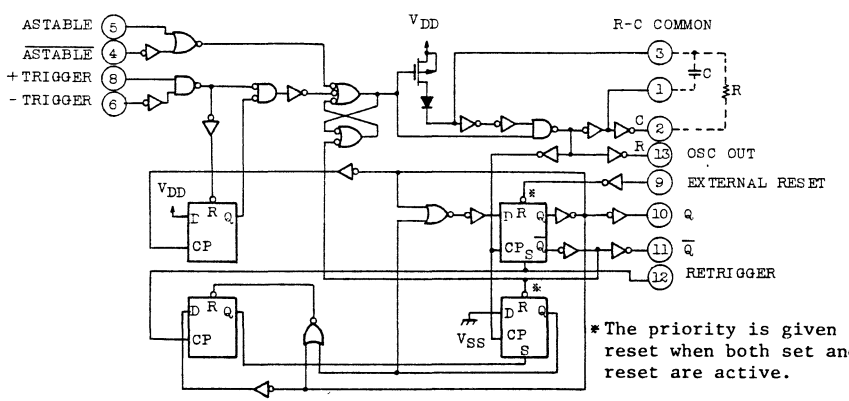
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	Tstg	-65 ~ 150	°C
Lead Temp./Time	Tsol	260°C · 10 sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



*The priority is given to reset when both set and reset are active.

TC4047BP

FUNCTION TABLE

FUNCTION	$\overline{AST.}$	AST.	-TRIG.	+TRIG.	RETRIG.	EXT. RESET	OUTPUT PERIOD OR PULSE WIDTH
ASTABLE MULTIVIBRATOR							Q, $\overline{Q}$
Free Running	*	H	H	L	L	L	T=4.40RC
	L	*	H	L	L	L	OSC OUT
Inhibit	H	L	H	L	L	L	T=2.20RC
MONOSTABLE MULTIVIBRATOR							
Positive-Edge Trigger	H	L	L	⌐¯_	L	L	Q, $\overline{Q}$
Negative-Edge Trigger	H	L	_/¯	H	L	L	t_w=2.48RC
Retrigger	H	L	L	_/¯_		L	

Note : External registor and capacitance as LOGIC DIAGRAM
* Don't care

OPERATING CONSIDERATION

1. Astable Operation
   By connecting inputs of -TRIGGER, +TRIGGER, RETRIGGER AND EXTERNAL RESET as shown in FUNCTION TABLE, stable operation of astable multivibrator can be obtained.
   - When ASTABLE input is placed at "H", oscillation is continued regardless of $\overline{ASTABLE}$ input. When $\overline{ASTABLE}$ input is placed at "L", oscillation is continued regardless of ASTABLE input. (Free Running).
   - Having ASTABLE input at "H", if ASTABLE input is set at "L", oscillation stops as long as it is at "L". (True Gating)
   - Having ASTABLE input at "L". if ASTABLE input is set at "H", oscillation stops as long as it is at "H". (Complement Gating)

   The oscillating period is determined by the external resistor and capacitor to be approximately T=2.2RC. This oscillation waveform is obtained as it is at OSC OUT and the oscillation waveform with double period and 50% duty cycle is obtained at outputs Q and $\overline{Q}$.

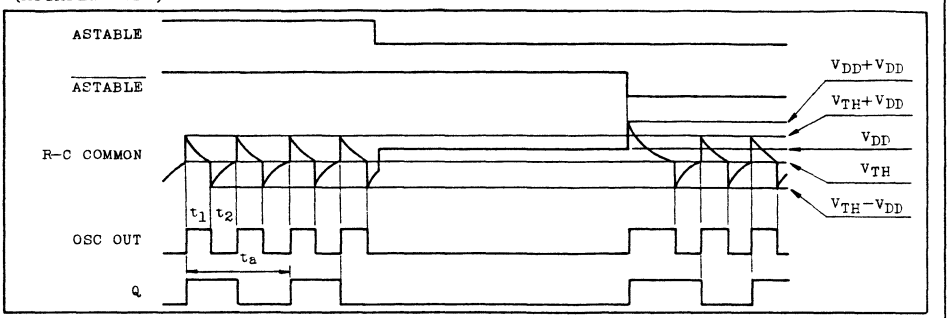
2. Mono-Stable Operation
   By connecting ASTABLE and $\overline{ASTABLE}$ inputs to "L" level and "H" level respectively, mono-stable multivibrator with the capabilities of retrigger operation and external asynchronous reset operation is obtained. This is normally used with RETRIGGER input and EXTERNAL RESET input connected to "L" level.
   - When -TRIGGER input is set to "L", mono-stable pulse is obtained at the rising edge of +TRIGGER input at Q and $\overline{Q}$ outputs. (Positive-edge Trigger)
   - When +TRIGGER input is set to "H", mono-stable pulse is obtained at the falling edge of -TRIGGER input at Q and $\overline{Q}$ outputs. (Negative-edge Trigger)
   - Keeping-TRIGGER input at "L", if the same pulse input($T < 2.48RC$) is applied to both +TRIGGER input and RETRIGGER input, retrigger operation is achieved. However, the last transition of this pulse input must be negative going. (Retrigger)

   The width of mono-stable pulse is determined by the external resistor and capacitor to be approximately t_w=2.48RC.

Note : The external resistor and capacitor should be connected as shown by broken lines in the logical diagram for both mono-stable and astable operations.
The capacitor used should be non-directional.

TIMING DIAGRAM

(ASTABLE MODE)

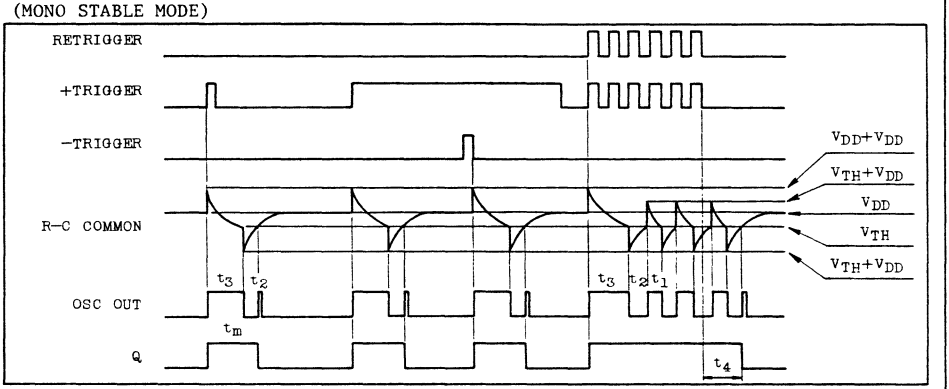


$$t_1 = -RC\,\ell n\,\frac{V_{TH}}{V_{DD}+V_{TH}}\quad,\quad t_2 = -RC\,\ell n\,\frac{V_{DD}-V_{TH}}{2V_{DD}-V_{TH}}$$

$$t_a = 2(t_1+t_2) = -2RC\,\ell n\,\frac{V_{TH}(V_{DD}-V_{TH})}{(V_{DD}+V_{TH})(2V_{DD}-V_{TH})}$$

TYPICAL : $V_{TH} = 1/2\,V_{DD}$ $\quad t_a = 4.40\,RC$

(MONO STABLE MODE)



$$t_1 = -RC\,\ell n\,\frac{V_{TH}}{V_{DD}+V_{TH}}\quad,\quad t_2 = -RC\,\ell n\,\frac{V_{DD}-V_{TH}}{2V_{DD}-V_{TH}}$$

$$t_3 = -RC\,\ell n\,\frac{V_{TH}}{2V_{DD}}\quad,\qquad t_1+t_2 < t_4 < 2(t_1+t_2)$$

$$t_m = t_3+t_2 = -RC\,\ell n\,\frac{V_{TH}(V_{DD}-V_{TH})}{2V_{DD}(2V_{DD}-V_{TH})}$$

TYPICAL : $V_{TH} = 1/2\,V_{DD}$ $\quad t_m = 2.48\,RC$

Note : V_{TH} : Threshold Level

TC4047BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
External Resistance	R_X		5	-	1000	kΩ
External Condenser	C_X		No Limit			μF

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8		
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	1	-	0.005	1	-	30	μA
				10	-	2	-	0.010	2	-	60	
				15	-	4	-	0.015	4	-	120	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (ASTABLE, $\overline{\text{ASTABLE}}$ - OSC OUT)	t_{pLH} t_{pHL}		5	-	290	580	ns
			10	-	110	220	
			15	-	70	160	
Propagation Delay Time (ASTABLE, $\overline{\text{ASTABLE}}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5	-	480	960	ns
			10	-	170	350	
			15	-	110	250	
Propagation Delay Time (+TRIGGER, -TRIGGER - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5	-	550	1100	ns
			10	-	200	450	
			15	-	130	300	
Propagation Delay Time (RETRIGGER - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5	-	250	600	ns
			10	-	100	300	
			15	-	65	200	
Propagation Delay Time (EXTERNAL RESET - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5	-	270	540	ns
			10	-	100	200	
			15	-	65	140	

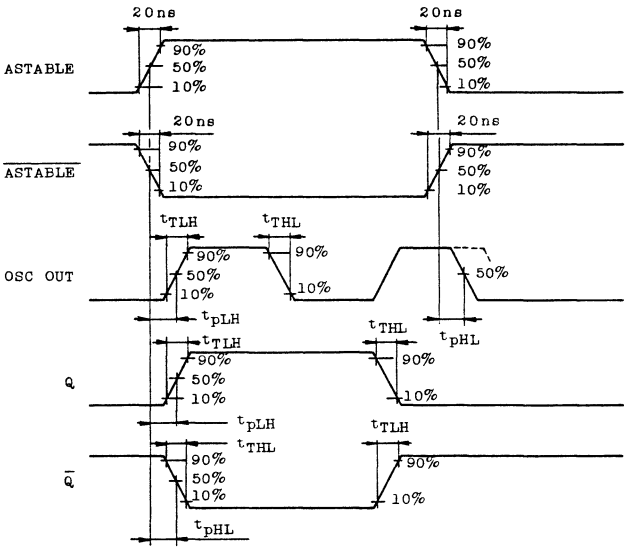
TC4047BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

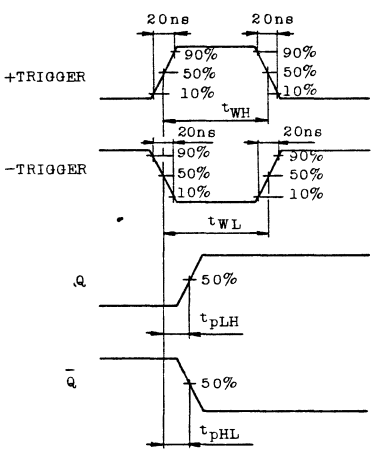
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Min. Pulse Width (+TRIGGER, -TRIGGER)	t_{WH} t_{WL}		5	-	370	740	ns
			10	-	130	260	
			15	-	70	140	
Min. Pulse Width (EXT. RESET)	t_{WH}		5	-	100	200	ns
			10	-	35	100	
			15	-	25	60	
Min. Pulse Width (RETRIGGER)	t_{WH}		5	-	95	600	ns
			10	-	40	230	
			15	-	25	150	
Max. Clock Input Rise Time Max. Clock Input Fall Time	t_r t_f		5	20	-	-	μs
			10	2.5	-	-	
			15	1.0	-	-	
Deviation from 50% Duty Facter (Q, $\overline{Q}$)		$\frac{t_w(H)-t_w(L)}{t_w(L)} \times 100$ (%)	5	-	±0.2	-	%
			10	-	±0.2	-	
			15	-	±0.1	-	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

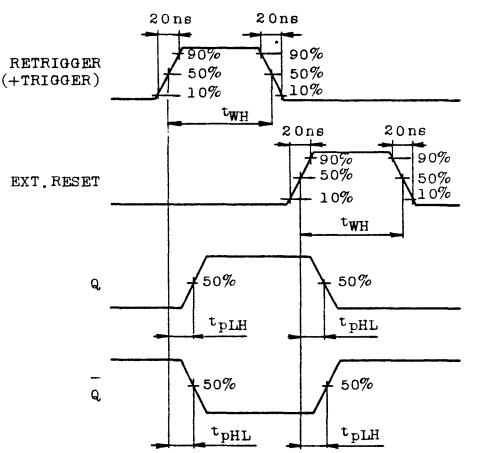
WAVEFORM 1.



WAVEFORM 2.



WAVEFORM 3.

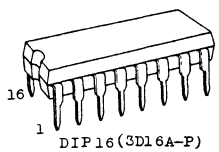


TC4049BP/BF
TC4050BP/BF

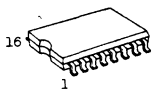
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4049BP/TC4049BF HEX BUFFER/CONVERTER (Inverting Type)
TC4050BP/TC4050BF HEX BUFFER/CONVERTER (Non-Inverting Type)

TC4049BP/BF, TC4050BP/BF contain six circuits of buffers. TC4049BP/BF is inverter type and TC4050BP/BF is non-inverter type.
Since one TTL or DTL can be directly driven having large output current, these are useful for interfacing from CMOS to TTL or DTL. As voltage up to $V_{SS}+18$ volts can be applied to the input regardless of V_{DD}, these can be also used as the level converter IC's which converts CMOS logical circuits of 15 volts or 10 volts system to CMOS/TTL logical circuits of 5 volts system.
Ideal switching characteristic has been obtained by the circuit diagram of three stage inverters for TC4049BP/BF and two stage inverters for TC4050BP/BF.



DIP16(3D16A-P)

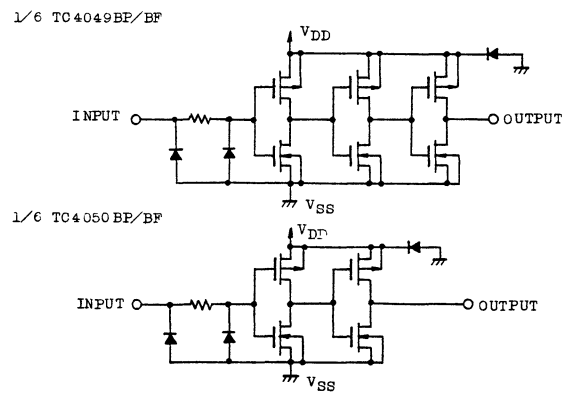


MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

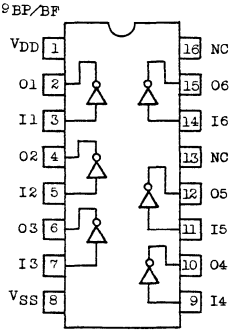
CHARACTERISTIC	SYMBOL	RATING	UNITS
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	-10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ∿ 85	°C
Storage Temperature Range	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

CIRCUIT DIAGRAM

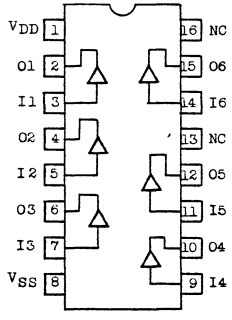


PIN ASSIGNMENT

TC4049BP/BF



TC4050BP/BF



(TOP VIEW)

ECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	18	V

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS}$, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS}$, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-	-	-		-	-	-	mA
		V_{OH}=2.5V	5	-1.4	-	-1.25		-	-1.0	-	
		V_{OH}=9.5V	10	-1.4	-	-1.25		-	-1.0	-	
		V_{OH}=13.5V	15	-4.0	-	-3.75		-	-3.0	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	3.5	-	3.2		-	2.5	-	
		V_{OL}=0.5V	10	6.0	-	5.0		-	3.6	-	
		V_{OL}=1.5V	15	26.0	-	24.0		-	18.0	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}	5	-	4	-	0.002	4	-	30	μA
			10	-	8	-	0.004	8	-	60	
		*	15	-	16	-	0.008	16	-	120	

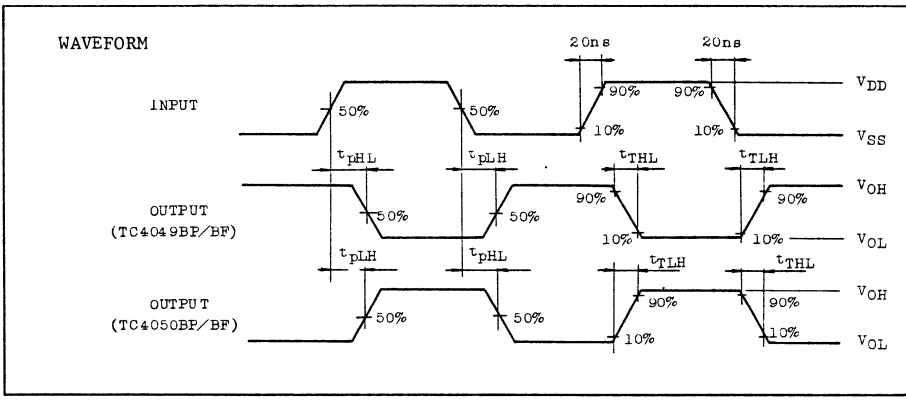
* All valid input combinations.

TC4049BP/BF, TC4050BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
	Output Transition Time (Low to High)	t_{TLH}		5	-	100	200	ns
				10	-	50	100	
				15	-	40	80	
	Output Transition Time (High to Low)	t_{THL}		5	-	50	100	
				10	-	25	50	
				15	-	20	40	
TC4049BP/BF	Propagation Delay Time (Low ot High)	t_{pLH}		5	-	140	220	
				10	-	70	110	
				15	-	50	80	
	Propagation Delay Time (High to Low)	t_{pHL}		5	-	110	220	
				10	-	50	110	
				15	-	40	80	
TC4050BP/BF	Propagation Delay Time (Low to High)	t_{pLH}		5	-	80	180	
				10	-	40	100	
				15	-	25	80	
	Propagation Delay Time (High to Low)	t_{pHL}		5	-	80	180	
				10	-	40	100	
				15	-	25	80	
	Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4051BP/BF, TC4052BP/BF TC4053BP/BF

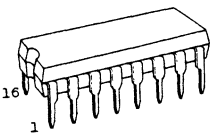
TC4051BP/TC4051BF SINGLE 8-CHANNEL MULTIPLEXER/DEMULTIPLEXER
TC4052BP/TC4052BF DIFFERENTIAL 4-CHANNEL MULTIPLEXER/DEMULTIPLEXER
TC4053BP/TC4053BF TRIPLE 2-CHANNEL MULTIPLEXER/DEMULTIPLEXER

TC4051BP/BF, TC4052BP/BF and TC4053BP/BF are multiplexers with capabilities of selection and mixture of analog signal and digital signal. TC4051BP/BF has 8 channels configuration. TC4052BP/BF has 4 channel × 2 configuration and TC4053BP/BF has 2 channel × 3 configuration.

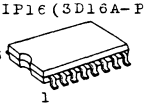
The digital signal to the control terminal turns "ON" the corresponding switch of each channel, with large amplitude (V_{DD}-V_{EE}) can be switched by the control signal with small logical amplitude (V_{DD}-V_{SS}).

For example, in the case of V_{DD}=5V, V_{SS}=0V and V_{EE}=-5V, signals between -5V and +5V can be switched from the logical circuit with single power supply of 5 volts.

As the ON-resistance of each switch is low, these can be connected to the circuits with low input impedance.



DIP16 (3D16A-P)



MFP16 (F16GC-P)

ABSOLUTE MAXIMUM RATINGS

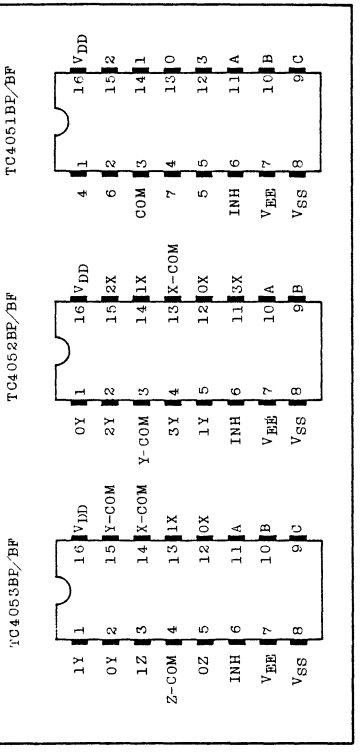
CHARACTERISTIC	SYMBOL	RATING	UNITS
DC Supply Voltage	V_{DD}-V_{SS}	-0.5 ~ 20	V
DC Supply Voltage	V_{DD}-V_{EE}	-0.5 ~ 20	V
Control Input Voltage	V_{CIN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Switch I/O Voltage	V_I/V_O	V_{EE}-0.5 ~ V_{DD}+0.5	V
Control Input Current	I_{CIN}	±10	mA
Potential difference across I/O during ON	V_{I-O}	-0.5 ~ 0.5	V
Power Dissipation	P_D	300 (DIP)/180 (MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

TRUTH TABLE

CONTROL INPUTS				"ON" CHANNEL		
INHIBIT	C△	B	A	TC4051BP TC4051BF	TC4052BP TC4052BF	TC4053BP TC4053BF
L	L	L	L	0	0X, 0Y	CX, 0Y, 0Z
L	L	L	H	1	1X, 1Y	1X, 0Y, 0Z
L	L	H	L	2	2X, 2Y	0X, 1Y, 0Z
L	L	H	H	3	3X, 3Y	1X, 1Y, 0Z
L	H	L	L	4	—	0X, 0Y, 1Z
L	H	L	H	5	—	1X, 0Y, 1Z
L	H	H	L	6	—	0X, 1Y, 1Z
L	H	H	H	7	—	1X, 1Y, 1Z
H	*	*	*	NOTE	NOTE	NOTE

* DON'T CARE △ EXCEPT TC4052

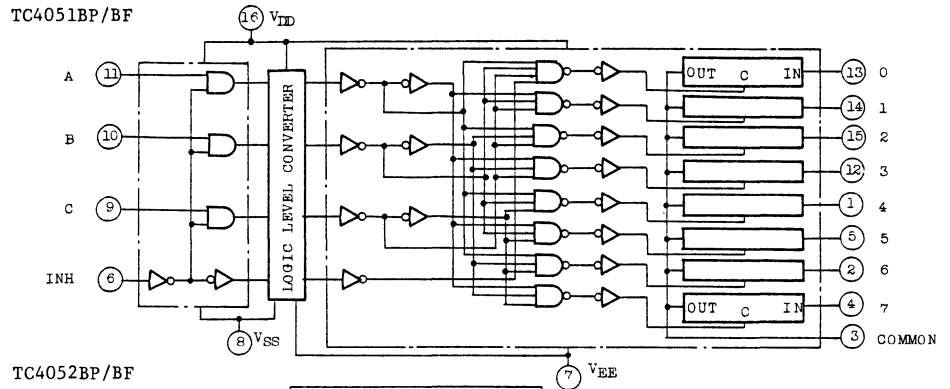
PIN ASSIGNMENT (TOP VIEW)



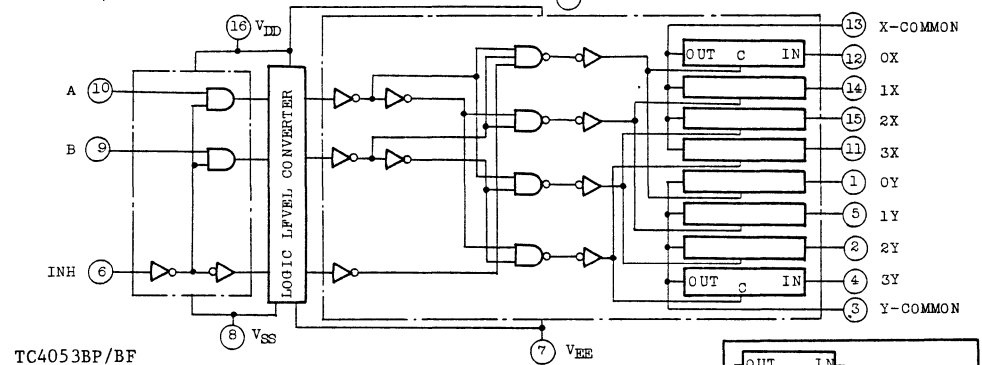
TC4051BP/BF, TC4052BP/BF, TC4053BP/BF

LOGIC DIAGRAM

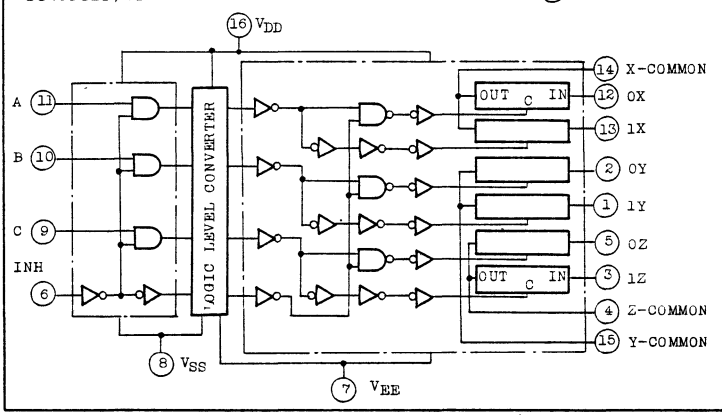
TC4051BP/BF

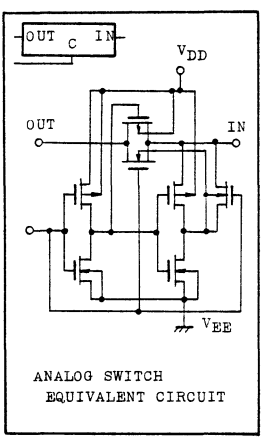


TC4052BP/BF



TC4053BP/BF





ANALOG SWITCH
EQUIVALENT CIRCUIT

TC4051BP/BF, TC4052BP/BF, TC4053BP/BF

ECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}-V_{SS}		3	-	18	V
	V_{DD}-V_{EE}		3	-	18	V
Control Input Voltage	V_{CIN}		V_{SS}	-	V_{DD}	V
Input/Output Voltage	V_{IN}/V_{OUT}		V_{EE}	-	V_{DD}	V

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V, In case not specifically appointed, V_{SS}=V_{EE})

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{EE} (V)	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
Control Input High Voltage	V_{IH}	|Iis|=10μA		5	3.5	-	3.5	2.75	-	3.5	-	V
				10	7.0	-	7.0	5.50	-	7.0	-	
				15	11.0	-	11.0	8.25	-	11.0	-	
Control Input Low Voltage	V_{IL}	|Iis|=10μA		5	-	1.5	-	2.25	1.5	-	1.5	
				10	-	3.0	-	4.5	3.0	-	3.0	
				15	-	4.0	-	6.75	4.0	-	4.0	
On-State Resistance	R_{ON}	V_{IN}=5V		5	-	500	-	200	600	-	800	Ω
		V_{IN}=2.5V		5	-	850	-	500	950	-	1300	
		V_{IN}=0.25V		5	-	500	-	120	600	-	800	
		V_{IN}=10V		10	-	210	-	120	250	-	300	
		V_{IN}=5V		10	-	210	-	100	250	-	300	
		V_{IN}=0.25V		10	-	210	-	100	250	-	300	
		V_{IN}=15V		15	-	140	-	80	160	-	200	
		V_{IN}=7.5V		15	-	140	-	60	160	-	200	
		V_{IN}=0.25V		15	-	140	-	60	160	-	200	
		V_{IN}=5V	-5	5	-	210	-	120	250	-	300	
		V_{IN}=±0.25V	-5	5	-	210	-	100	250	-	300	
		V_{IN}=-5V	-5	5	-	210	-	100	250	-	300	
		V_{IN}=7.5V	-7.5	7.5	-	140	-	80	160	-	200	
		V_{IN}=±0.25V	-7.5	7.5	-	140	-	60	160	-	200	
		V_{IN}=-7.5V	-7.5	7.5	-	140	-	60	160	-	200	
ΔOn-State Resistance Between Any 2 Switches	R_{ON}^{Δ}		-2.5	2.5	-	-	-	30	-	-	-	Ω
			-5	5	-	-	-	15	-	-	-	
			-7.5	7.5	-	-	-	10	-	-	-	
Input/Output Leakage Current	I_{OFF}	V_{IN}=10V, V_{OUT}=0V		10	-	-	-	±0.01	±125	-	-	nA
		V_{IN}=0V, V_{OUT}=10V		10	-	-	-	±0.01	±125	-	-	
		V_{IN}=18V, V_{OUT}=0V		18	-	±250	-	±0.1	±250	-	±1000	
		V_{IN}=0V, V_{OUT}=18V		18	-	±250	-	±0.1	±250	-	±1000	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD} *		5	-	20	-	0.005	20	-	150	μA
				10	-	40	-	0.010	40	-	300	
				15	-	80	-	0.015	80	-	600	
Input Current	I_{IN}	V_{IH}=18V		18	-	0.3	-	10^{-5}	.0.3	-	1.0	
		V_{IL}=0V		18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	

* All valid input combinations.

TC4051BP/BF, TC4052BP/BF, TC4053BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{EE}(V)	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Propagation Delay Time (A, B, C - OUT)	t_{pLH}	R_L=10kΩ	0	5	-	450	1000	ns
			0	10	-	200	500	
			0	15	-	150	400	
	t_{pHL}	C_L=50pF	-5	5	-	250	700	
			-7.5	7.5	-	200	500	
Propagation Delay Time (INH - OUT)	t_{pLH}	R_L=10kΩ	0	5	-	600	1400	
			0	10	-	250	700	
			0	15	-	200	500	
	t_{pHL}	C_L=50pF	-5	5	-	300	900	
			-7.5	7.5	-	200	500	
Propagation Delay Time (Switch IN - OUT)	t_{pLH}	R_L=10kΩ	0	5	-	15	45	
			0	10	-	8	30	
	t_{pHL}	C_L=50pF	0	15	-	5	20	
-3dB Cutoff Frequency	f_{MAX} (I - O)	R_L=10kΩ, C_L=15pF (*1)	-5	+5	-	16	-	MHz
Total Harmonic Distortion	-	R_L=10kΩ, f=1kHz (*2)	-5	+5	-	0.1	-	%
-50dB Feedthrough Frequency	-	R_L=1kΩ (*3)	-5	+5	-	500	-	kHz
Crosstalk (CONTROL - OUT)	-	R_{IN}=1kΩ	0	5	-	100	-	mV
		R_{OUT}=10kΩ	0	10	-	200	-	
		R_L=15pF	0	15	-	300	-	
Input Capacitance	C_{IN}	Control Input			-	5	7.5	pF
		Switch I/O			-	10	-	

*1 Sine wave of ±2.5Vp-p shall be used for V_{is} and the frequency of 20 log $10\frac{V_{is}}{V_{os}}$=-3dB shall be f_{MAX}.

*2 V_{is} shall be sine wave of ±2.5Vp-p.

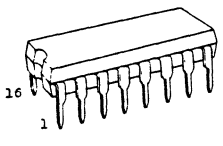
*3 Sine wave of ±2.5Vp-p shall be used for V_{is} and the frequency of 20 log $10\frac{V_{os}}{V_{is}}$=-50dB shall be feed-through.

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4054BP

C4054BP LIQUID-CRYSTAL DISPLAY DRIVER (4-SEGMENT DISPLAY DRIVER)

C4054BP contains four circuits of liquid crystal field effect type) drivers.
Then pulse is applied to DF input, the output with 80° out of phase from DF pulse is obtained at OUT if nput IN is "H". If input IN is "L", OUT and DF ulse become in-phase.
y applying DF input pulse to the common terminal back plane) of liquid crystal, the liquid crystal lement can be directly driven by the input signal ith "H" level. This is suitable for illuminating he segments of decimal point and positive or egative sign. If $V_{EE} < V_{SS}$, the level conversion peration which lowers only "L" side of logical ignal can be achieved.

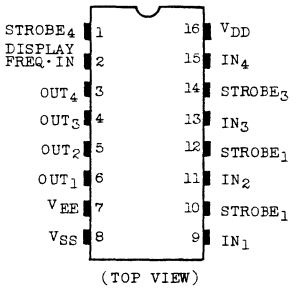


DIP 16(3D16A-P)

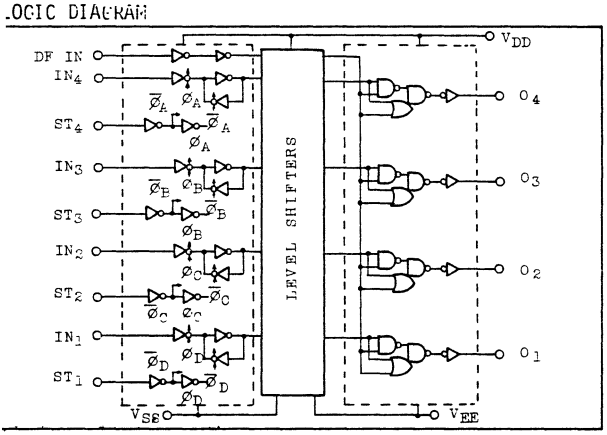
BSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
C Supply Voltage	V_{DD}-V_{SS}	-0.5 ~ 20	V
	V_{DD}-V_{EE}	-0.5 ~ 20	V
nput Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
utput Voltage	V_{OUT}	V_{EE}-0.5 ~ V_{DD}+0.5	V
C Input Current	I_{IN}	±10	mA
ower Dissipation	P_D	300	mW
perating Temperature ange	T_A	-40 ~ 85	°C
torage Temperature ange	T_{stg}	-65 ~ 150	°C
ead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

DF IN	IN_n	$STROBE_n$	OUT_n
L	L	H	L
H	L	H	H
L	H	H	H
H	H	H	L
*	*	L	△△

* : Don't care

△△ : Depends upon the INPUT mode previously applied when STROBE "H".

TC4054BP

RECOMMENDE OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}-V_{SS}		3	-	18	V
	V_{DD}-V_{EE}		3	-	18	V
Input Voltage	V_{IN}		V_{SS}	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

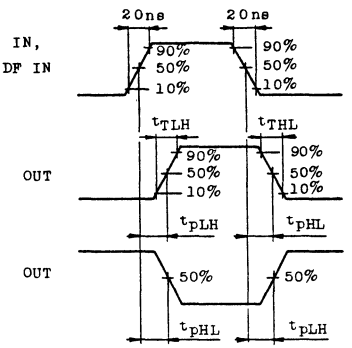
DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
			V_{DD}(V)	V_{EE}(V)				
Output Transition Time	t_{TLH} t_{THL}		5	0	-	80	200	ns
			5	-5	-	50	100	
			10	0	-	50	100	
			15	0	-	40	80	
Propagation Delay Time (NI - OUT)	t_{pLH} t_{pHL}		5	0	-	660	1800	ns
			5	-5	-	250	800	
			10	0	-	210	680	
			15	0	-	140	500	
Propagation Delay Time (DF IN - OUT)	t_{pLH} t_{pHL}		5	0	-	720	1800	ns
			5	-5	-	260	800	
			10	0	-	240	680	
			15	0	-	150	500	
Propagation Delay Time (STROBE - OUT)	t_{pLH} t_{pHL}		5	0	-	660	1800	ns
			5	-5	-	250	800	
			10	0	-	210	680	
			15	0	-	140	500	
Min. Clcok Pulse Width (STROBE)	t_{WH}		5	0	-	60	220	ns
			5	-5	-	70	220	
			10	0	-	20	100	
			15	0	-	15	70	
Min. Set-up Time (IN - STROBE)	t_{SU}		5	0	-	50	220	ns
			5	-5	-	60	220	
			10	0	-	15	100	
			15	0	-	10	70	
Input Capacitance	C_{IN}				-	5	7.5	pF

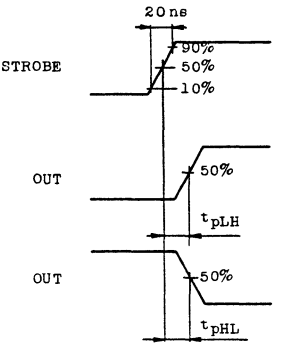
TC4054BP

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

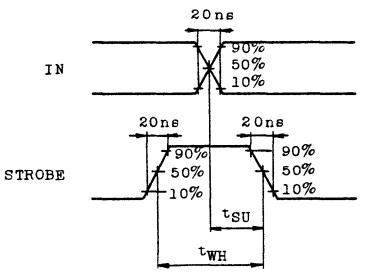
WAVEFROM 1. (ST="H")



WAVEFORM 2.



WAVEFORM 3.



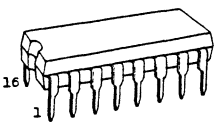
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4055BP
TC4056BP/BF

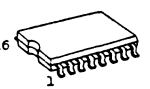
TC4055BP LIQUID-CRYSTAL DISPLAY DRIVER
(BCD TO 7-Segment Decoder/Driver with "Display-Frequency" Output)

TC4056BP/TC4056BF LIQUID-CRYSTAL DISPLAY DRIVER
(BCD TO 7-Segment Decoder/Driver with Strobed-Latch Function)

TC4055BP, TC4056BP/BF are LC drivers which drive the field effect type liquid crystal with seven segments by BCD input.
If DF input="L", a selected output among segment outputs of a through g becomes "H" level and if DF input="H", a selected output becomes "L" level.
Seven segment liquid crystal element can be directly driven by applying the pulse in-phase with DF input to the common terminal (back plane) of liquid crystal.
TC4055BP is equipped with DF output for the common terminal and TC4056BP/BF is equipped with the latch.
If $V_{EE} < V_{SS}$, the level conversion operation which lowers only "L" side of logical signal can be achieved.



DIP 16(3D16A-P)

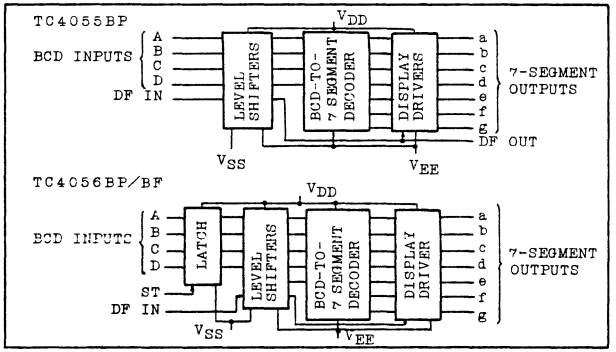


MFP 16(F16GC-P)

MAXIMUM RATINGS

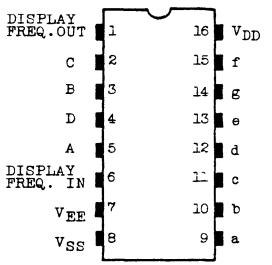
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}-V_{SS}	-0.5 ~ 20	V
	V_{DD}-V_{EE}	-0.5 ~ 20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{EE}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

BLOCK DIAGRAM

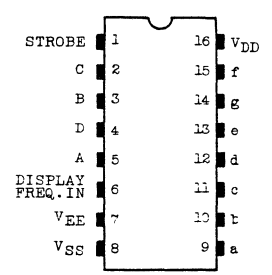


PIN ASSIGNMENT

TC4055BP



TC4056BP/BF



(TOP VIEW)

TC4055BP, TC4056BP/BF

TRUTH TABLE

BCD INPUTS				7-SEGMENT OUTPUTS (DF IN="L")							7-SEGMENT OUTPUTS (DF IN="H")							DISPLAY CHARACTER
D	C	B	A	a	b	c	d	e	f	g	a	b	c	d	e	f	g	
L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L	L	H	0
L	L	L	H	L	H	H	L	L	L	L	H	L	L	H	H	H	H	1
L	L	H	L	H	H	L	H	H	L	H	L	L	H	L	L	H	L	2
L	L	H	H	H	H	H	H	L	L	H	L	L	L	L	H	H	L	3
L	H	L	L	L	H	H	L	L	H	H	H	L	L	H	H	L	L	4
L	H	L	H	H	L	H	H	L	H	H	L	H	L	L	H	L	L	5
L	H	H	L	H	L	H	H	H	H	H	L	H	L	L	L	L	L	6
L	H	H	H	H	H	H	L	L	L	L	L	L	L	H	H	H	H	7
H	L	L	L	H	H	H	H	H	H	H	L	L	L	L	L	L	L	8
H	L	L	H	H	H	H	H	L	H	H	L	L	L	L	H	L	L	9
H	L	H	L	L	L	L	H	H	H	L	H	H	H	L	L	L	H	L
H	L	H	H	L	H	H	L	H	H	H	H	L	L	H	L	L	L	T
H	H	L	L	H	H	L	L	H	H	H	L	L	H	H	L	L	L	F
H	H	L	H	H	H	H	L	H	H	H	L	L	L	H	L	L	L	J
H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	—
H	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	BLANK

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}-V_{SS}		3	-	18	V
	V_{DD}-V_{EE}		3	-	18	
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=V_{EE}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$ <1μA V_{IN}=V_{SS},V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$ <1μA V_{IN}=V_{SS},V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	

TC4055BP, TC4056BP/BF

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=V_{EE}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		V_{IN}=V_{SS},V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		V_{IN}=V_{SS},V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION V_{DD}(V)	TEST CONDITION V_{EE}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}	5	0	-	80	200	ns
		5	-5	-	50	100	
		10	0	-	50	100	
		15	0	-	40	80	

TC4055BP, TC4056BP/BF

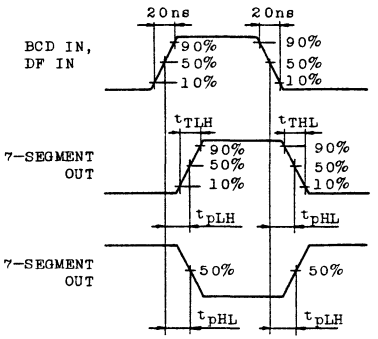
DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	V_{EE}(V)	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (BCD IN - 7-SEGMENT OUT)	t_{pLH} t_{pHL}		5	0	-	980	2000	ns
			5	-5	-	380	900	
			10	0	-	320	750	
			15	0	-	210	500	
Propagation Delay Time (DF IN - 7-SEGMENT OUT)	t_{pLH} t_{pHL}		5	0	-	620	1800	ns
			5	-5	-	240	900	
			10	0	-	200	750	
			15	0	-	130	500	
* Propagation Delay Time (DF IN - DF OUT)	t_{pLH} t_{pHL}		5	0	-	570	1500	ns
			5	-5	-	220	800	
			10	0	-	180	700	
			15	0	-	110	550	
** Propagation Delay Time (STROBE - 7-SEGMENT OUT)	t_{pLH} t_{pHL}		5	0	-	1000	3100	ns
			5	-5	-	400	1300	
			10	0	-	340	1150	
			15	0	-	210	750	
** Min. Pulse Width (STROBE)	t_{WH}		5	0	-	55	220	ns
			5	-5	-	60	220	
			10	0	-	25	100	
			15	0	-	20	70	
** Min. Set-up Time (BCD IN - STROBE)	t_{SU}		5	0	-	50	220	ns
			5	-5	-	50	220	
			10	0	-	25	100	
			15	0	-	20	70	
Input Capacitance	C_{IN}				-	5	7.5	pF

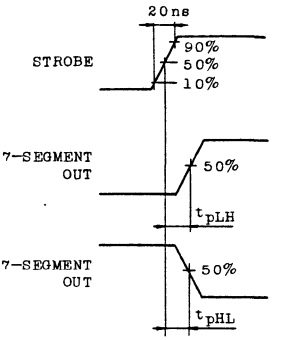
* TC4055BP, ** TC4056BP/BF

AVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

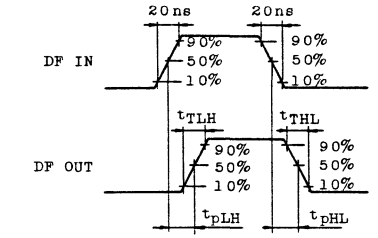
WAVEFORM 1



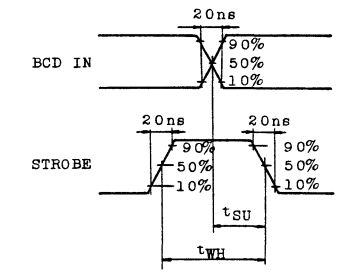
WAVEFORM 2 (TC4056BP/BF)



WAVEFORM 3 (TC4055BP)



WAVEFORM 4 (TC4056BP/BF)

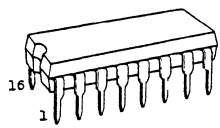


TC4063BP/BF

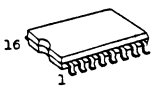
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4063BP/TC4063BF 4-BIT MAGNITUDE COMPARATOR

TC4063BP/BF is weighted comparator which compares magnitude of 4 bits input data B_0 through B_3. When TC4063BP/BF is used, the signals of larger, smaller and equal can be obtained at three output lines by the cascade input mode of three lines of (A>B)IN, (A=B)IN and (A<B)IN.
Cascade connection of n number of TC4063BP/BF's easily realizes magnitude comparator of 4 × n bits.



DIP 16(3D16A-P)

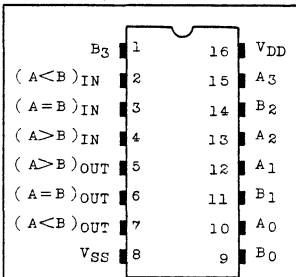


MFP 16(F16GC-P)

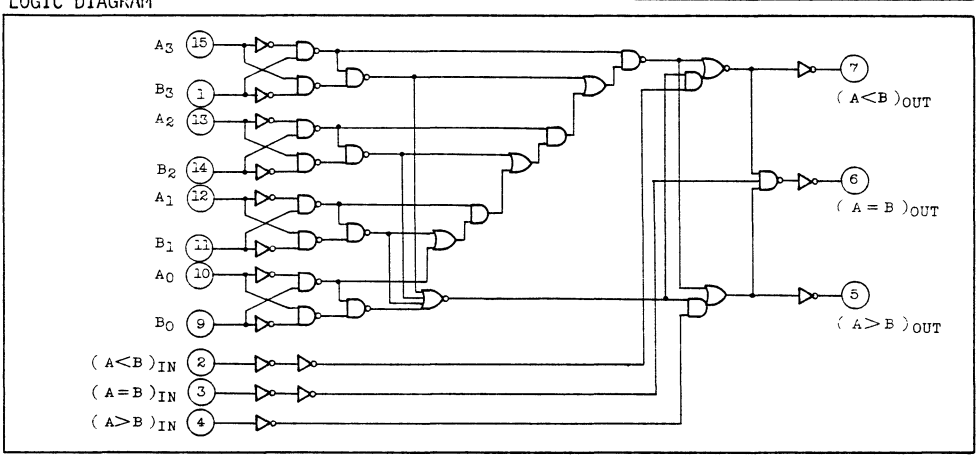
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_N	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TC4063BP/BF

TRUTH TABLE

INPUTS							OUTPUTS			
COMPARING				CASCADING						
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	A<B	A=B	A>B	A<B	A=B	A>B	
$A_3>B_3$	*	*	*	*	*	*	L	L	H	
$A_3=B_3$	$A_2>B_2$	*	*	*	*	*	L	L	H	
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	*	*	*	*	L	L	H	
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	*	*	*	L	L	H	
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H	
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L	
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L	
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	*	*	*	H	L	L	
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	*	*	*	*	H	L	L	
$A_3=B_3$	$A_2<B_2$	*	*	*	*	*	H	L	L	
$A_3<B_3$	*	*	*	*	*	*	H	L	L	* Don't care

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									

TC4063BP/BF

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	mA
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		V_{IN}=V_{SS},V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\| < 1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\| < 1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

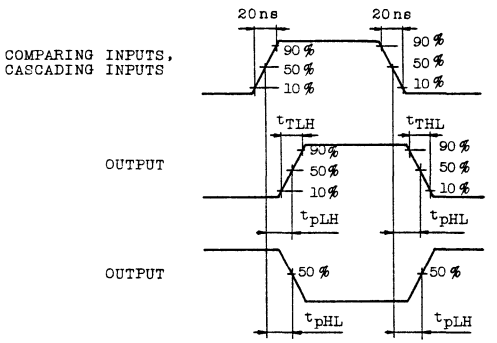
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (COMPARING INPUTS - OUTPUTS)	t_{pLH} t_{pHL}		5	-	340	1250	ns
			10	-	140	500	
			15	-	100	350	

TC4063BP/BF

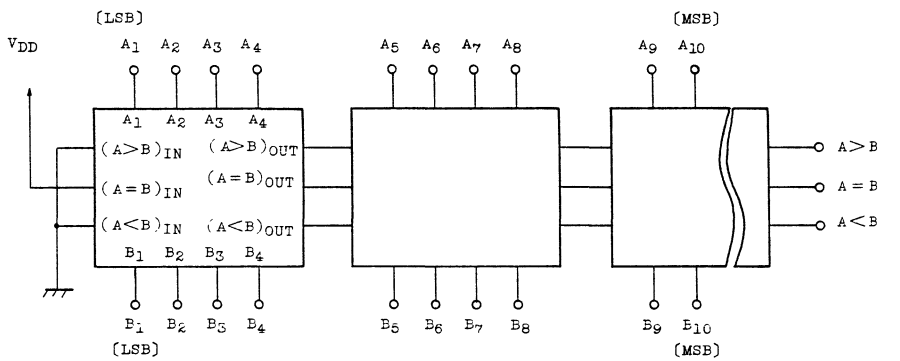
YNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
ropagation Delay Time (CASCADING INPUTS - OUTPUTS)	t_{pLH} t_{pHL}		5	-	280	1000	ns
			10	-	110	400	
			15	-	90	280	
nput Capacitance	C_{IN}			-	5	7.5	pF

AVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



PPLICATION CIRCUIT



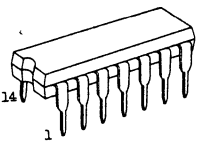
TC4066BP/BF

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

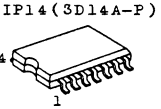
TC4066BP/TC4066BF QUAD BILATERAL SWITCH

TC4966BP/BF contains four independent circuits of bidirectional switches. When control input CONT is set to "H" level, the impedance between input and output of the switch becomes low and when it is set to "L" level, the impedance becomes high. This can be applied for switching of analog signals and digital signals.

- ON-resistance, R_{ON}
  - 300Ω (TYP.) ..... V_{DD}-V_{SS}=5V
  - 110Ω (TYP.) ..... V_{DD}-V_{SS}=10V
  - 70Ω (TYP.) ..... V_{DD}-V_{SS}=15V
- OFF-resistance, R_{OFF}
  - R_{OFF} (TYP.) > 10^9Ω



DIP14(3D14A-P)

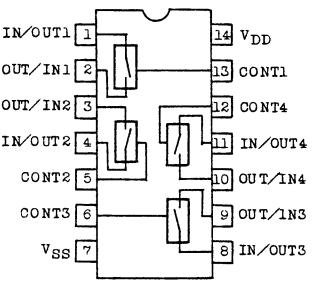


MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

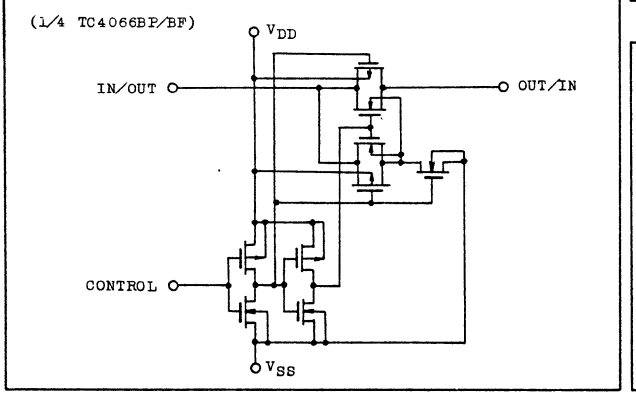
CHARACTERISTIC	SYMBOL	RATING	UNITS
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ∿ V_{SS}+20	V
Control Input Voltage	$V_{C\ IN}$	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Switch I/O Voltage	$V_{I/O}$	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Potential difference across I/O during ON	V_I-V_O	±0.5	V
Control Input Current	$I_{C\ IN}$	±10	mA
Operating Temperature Range	T_A	-40 ∿ 85	°C
Storage Temperature Range	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

CIRCUIT DIAGRAM



TRUTH TABLE

CONTROL	Impedance Between IN/OUT-OUT/IN ※
H	05 ~ 5×10²Ω
L	>10⁹Ω

※ See Static Electrical Characteristics

ECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
C Supply Voltage	V_{DD}		3	-	18	V
nput/Output Voltage	V_{IN}/V_{OUT}		0	-	V_{DD}	V

TATIC ELECTRICAL CHARACTERISTICS (In case not specifically appointed, V_{SS}=0V)

HARACTERISTIC	SYMBOL	TEST CONDITION	V_{SS} (V)	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
ontrol Input igh Voltage	V_{IH}	$\|I_{is}\|$=10μA		5	3.5	-	3.5	2.75	-	3.5	-	V
				10	7.0	-	7.0	5.50	-	7.0	-	
				15	11.0	-	11.0	8.25	-	11.0	-	
ontrol Input ow Voltage	V_{IL}	$\|I_{is}\|$=10μA		5	-	1.5	-	2.25	1.5	-	1.5	
				10	-	2.0	-	4.5	2.0	-	2.0	
				15	-	2.5	-	6.75	2.5	-	2.5	
n-State esistance	R_{ON}	V_{IN}=5V		5	-	500	-	200	600	-	800	Ω
		V_{IN}=2.5V		5	-	850	-	500	950	-	1300	
		V_{IN}=0.25V		5	-	500	-	150	600	-	800	
		V_{IN}=10V		10	-	210	-	120	250	-	300	
		V_{IN}=5V		10	-	210	-	100	250	-	300	
		V_{IN}=0.25V		10	-	210	-	100	250	-	300	
		V_{IN}=15V		15	-	140	-	90	160	-	200	
		V_{IN}=7.5V		15	-	140	-	60	160	-	200	
		V_{IN}=0.25V		15	-	140	-	60	160	-	200	
		V_{IN}=5V	-5	5	-	210	-	120	250	-	300	
		V_{IN}=±0.25V	-5	5	-	210	-	100	250	-	300	
		V_{IN}=-5V	-5	5	-	210	-	100	250	-	300	
		V_{IN}=7.5V	-7.5	7.5	-	140	-	90	160	-	200	
		V_{IN}=±0.25V	-7.5	7.5	-	140	-	60	160	-	200	
		V_{IN}=-7.5V	-7.5	7.5	-	140	-	60	160	-	200	
On-State esistance etween Any Switches	$R_{ON}{}^{\Delta}$		-2.5	2.5	-	-	-	30	-	-	-	
			-5	5	-	-	-	15	-	-	-	
			-7.5	7.5	-	-	-	10	-	-	-	
nput/Output eakage Current	I_{OFF}	V_{IN}=10V, V_{OUT}=0V		10	-	-	-	±0.01	±125	-	-	nA
		V_{IN}=0V, V_{OUT}=10V		10	-	-	-	±0.01	±125	-	-	
		V_{IN}=18V, V_{OUT}=0V		18	-	±250	-	±0.1	±250	-	±1000	
		V_{IN}=0V, V_{OUT}=18V		18	-	±250	-	±0.1	±250	-	±1000	
uiescent evice Current	I_{DD}	$V_{IN}=V_{DD}, V_{SS}$ *		5	-	1.0	-	0.001	1.0	-	7.5	μA
				10	-	2.0	-	0.001	2.0	-	15	
				15	-	4.0	-	0.002	4.0	-	30	
nput urrent "H" Level	I_{IH}	V_{IH}=18V		18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
"L" Level	I_{IL}	V_{IL}=0V		18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	

All valid input combinations.

TC4066BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{SS}(V)	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (IN - OUT)	t_{pLH} t_{pHL}	R_L=10kΩ C_L=50pF	0	5	-	15	45	ns
			0	10	-	8	30	
			0	15	-	5	20	
Propagation Delay Time (CONTROL - OUT)	t_{pLH} t_{pHL}	R_L=10kΩ C_L=50pF	0	5	-	100	200	
			0	10	-	40	70	
			0	15	-	35	60	
Max. Control Input Repetition Rate	f_{MAX} (C)	C_L=15pF	0	5	-	3	-	MHz
			0	10	-	9	-	
			0	15	-	11	-	
-3dB Cutoff Frequency	f_{MAX} (I-O)	R_L=10kΩ C_L=15pF (*1)	-5	5	-	16	-	
Total Harmonic Distortion	-	R_L=10kΩ f=1kHz (*2)	-5	5	-	0.1	-	%
-50dB Feedthrough Frequency	-	R_L=1kΩ (*3)	-5	5	-	500	-	kHz
Crosstalk (CONTROL - OUT)	-	R_{IN}=1kΩ R_{OUT}=10kΩ C_L=15pF	0	5	-	200	-	mV
			0	10	-	400	-	
			0	15	-	600	-	
Input Capacitance	C_{IN}	Control Input			-	5	7.5	pF
		Switch I/O			-	10	-	

*1. The Frequency at 20 log $10\frac{V_{os}}{V_{is}}$ = -3dB shall be f_{MAX}(I-O) using sine wave of $\pm 2.5V_{p-p}$ for V_{is}.

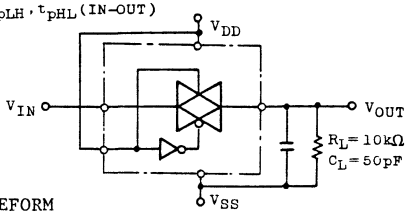
*2. V_{is} shall be sine wave of ±2.5V.

*3. The frequency at 20 log $10\frac{V_{os}}{V_{is}}$ = -50dB shall be the feed through using sine wave of $\pm 2.5V_{p-p}$.

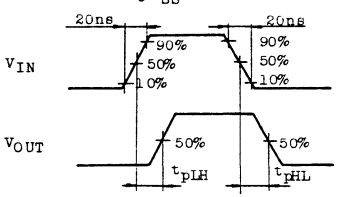
CIRCUIT FOR MEASUREMENT OF ELECTRICAL CHARACTERISTICS

CIRCUIT

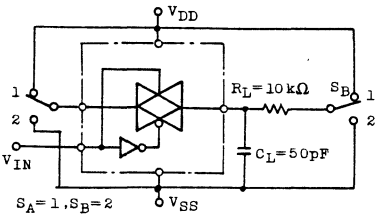
t_{pLH}, t_{pHL} (IN-OUT)



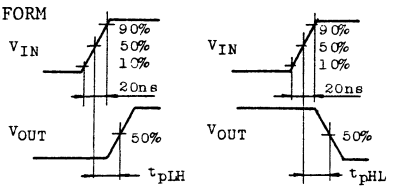
WAVEFORM



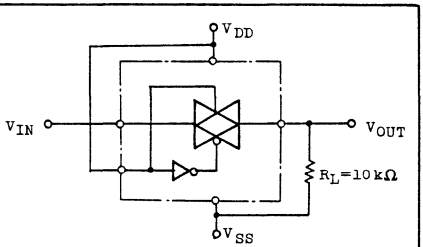
CIRCUIT 2 t_{pLH}, t_{pHL} (CONTROL-OUT)



WAVEFORM

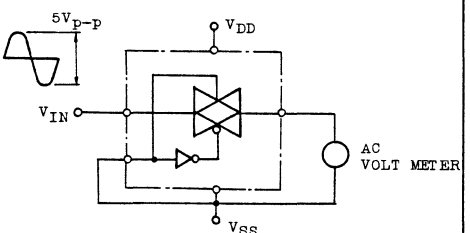


R_{ON}

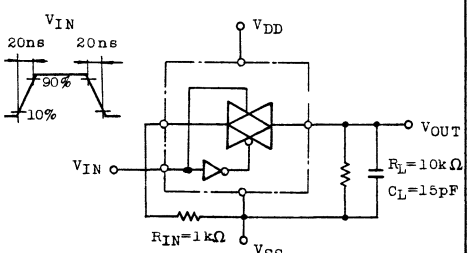


$$R_{ON} = 10 \times \frac{(V_{IN} - V_{OUT})}{V_{OUT}} \ [k\Omega]$$

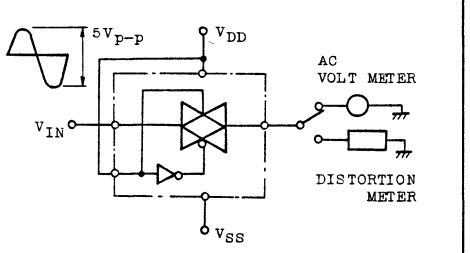
4 FEEDTHROUGH



CROSSTALK



5 FREQUENCY RESPONCE, DISTORTION

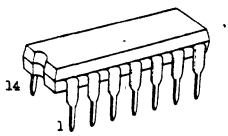


TC4068BP/BF

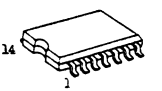
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4068BP/TC4068BF 8-INPUT NAND/AND GATE

The TC4068BP/BF is 8-input positive logic NAND/AND gate.
Since each output of this gate is provided with a buffer, the input/output voltage characteristics have been improved, allowing noise immunity to be elevated; thus, the variation of propagation delay time due to the increase in load capacity is kept down to the minimum.



DIP14(3D14A-P)

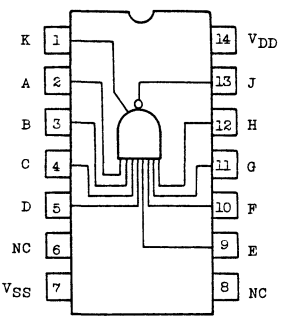


MFP14(F14GB-P)

MAXIMUM RATINGS

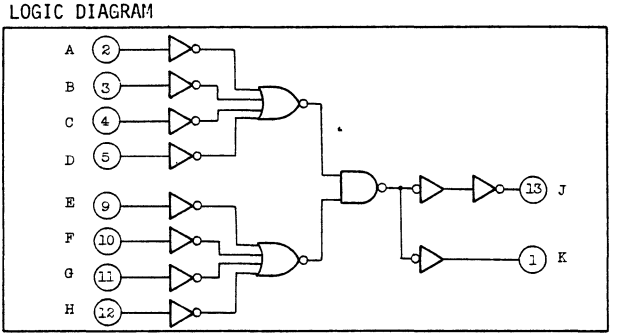
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

HARACTERISTIC		SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
igh-Level utput Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
				10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
ow-Level utput Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
				10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
utput High urrent		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
utput Low urrent		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
nput High oltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
nput Low oltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
nput urrent	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
uiescent Device urrent		I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	0.25	-	0.001	0.25	-	7.5	μA
				10	-	0.5	-	0.001	0.5	-	15	
				15	-	1.0	-	0.002	1.0	-	30	

* All valid input combinations.

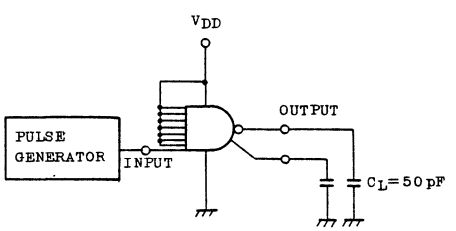
TC4068BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

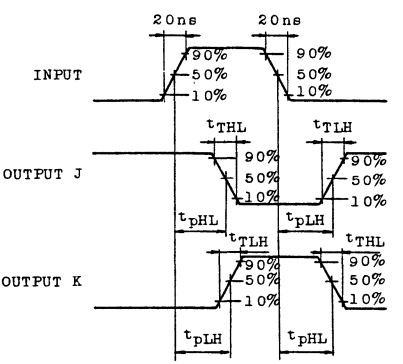
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time	t_{pLH} t_{pHL}		5	-	160	320	ns
			10	-	70	150	
			15	-	45	110	
Input Capacitance	C_{IN}			-	5	7.5	pF

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

CIRCUIT



WAVEFORM



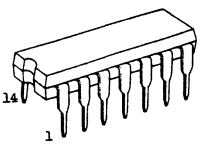
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4069UBP/UBF

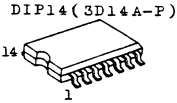
TC4069UBP/TC4069UBF HEX INVERTER

TC4069UBP/UBF contains six circuits of inverters. The pin allocation is same as TC7404UB and since the operating current consumption is smaller, this is suitable for the applications of CR oscillator circuits, crystal oscillator circuits and linear amplifiers in addition to its application as inverters.

Because of one stage gate configuration, the propagation time has been reduced.



DIP14(3D14A-P)

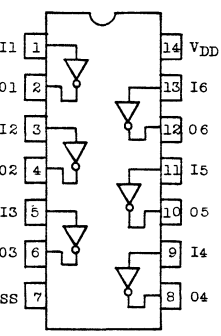


MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ∿ 85	°C
Storage Temperature Range	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

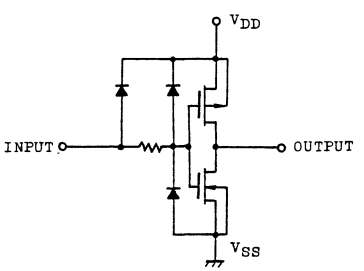
PIN ASSIGNMENT



(TOP VIEW)

CIRCUIT DIAGRAM

1/6 TC4069UBP/UBF



TC4069UBP/UBF

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

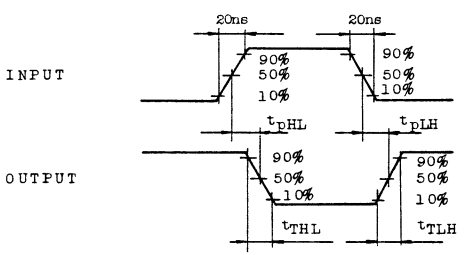
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	mA
		V_{OH}=2.5V	5	-	-	-		-	-	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V	15	-1.4	-	-1.2		-	-1.0	-	
		$V_{IN}=V_{SS}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
		$V_{IN}=V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V	5	4.0	-	4.0	-	-	4.0	-	V
		V_{OUT}=1.0V	10	8.0	-	8.0	-	-	8.0	-	
		V_{OUT}=1.5V	15	12.0	-	12.0	-	-	12.0	-	
		$\|I_{OUT}\|$ <1μA									
Input Low Voltage	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-	-	1.0	-	1.0	
		V_{OUT}=9.0V	10	-	2.0	-	-	2.0	-	2.0	
		VOUT=13.5V	15	-	3.0	-	-	3.0	-	3.0	
		$\|I_{OUT}\|$ <1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD} *	5	-	1	-	0.001	1	-	7.5	μA
			10	-	2	-	0.001	2	-	15	
			15	-	4	-	0.002	4	-	30	

* All valid input combinations.

)YNAMİC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Transition Time (High to Low)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (Low to High)	t_{pLH}		5	-	100	180	
			10	-	60	120	
			15	-	50	100	
Propagation Delay Time (High to Low)	t_{pHL}		5	-	75	150	
			10	-	40	100	
			15	-	35	80	
Input Capacitance	C_{IN}			-	7.5	15	pF

/AVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

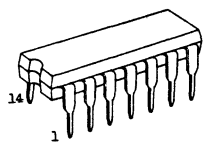


TC4071BP/BF, TC4072BP/BF TC4075BP/BF

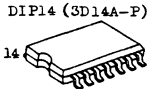
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4071BP/TC4071BF QUAD 2 INPUT OR GATE
TC4072BP/TC4072BF DUAL 4 INPUT OR GATE
TC4075BP/TC4075BF TRIPLE 3 INPUT OR GATE

TC4071BP/BF, TC4075BP/BF and TC4072BP/BF are positive logic OR gates with two inputs, three inputs and four inputs respectively. As all the outputs of gates are equipped with the buffer circuits of inverters, the input/output propagation characteristic has been improved and the variation of propagation time caused by increase of load capacity is kept minimum.



DIP14 (3D14A-P)

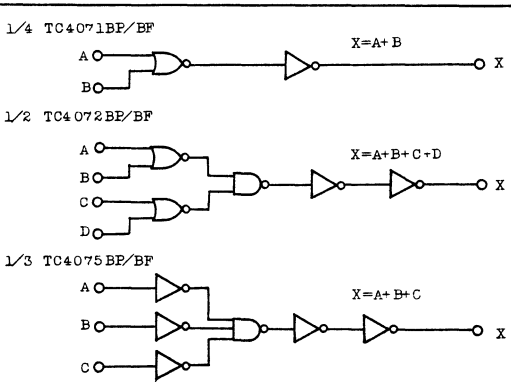


MFP14 (F14GB-P)

ABSOLUTE MAXIMUM RATINGS

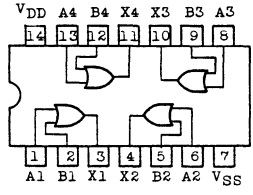
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ∿ 85	°C
Storage Temperature Range	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C • 10 sec	

LOGIC DIAGRAM

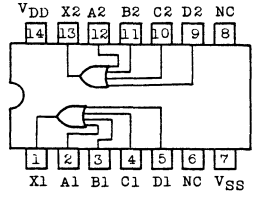


PIN ASSIGNMENT (TOP VIEW)

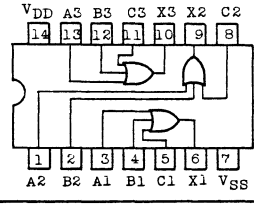
TC4071BP/BF



TC4072BP/BF



TC4075BP/BF



TC4071BP/BF, TC4072BP/BF, TC4075BP/BF

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS}$, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current (TC4072BP/BF) (TC4075BP/BF)	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output Low Current (TC4072BP/BF) (TC4075BP/BF)	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS}$									
Output High Current (TC4071BP/BF)	I_{OH}	V_{OH}=4.6V	5	-2.0	-	-0.16		-	-0.12	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V	15	-1.4	-	-1.2		-	-1.0	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output Low Current (TC4071BP/BF)	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
		$V_{IN}=V_{SS}$									
Input High Voltage	V_{IH}	V_{OUT}=4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	μA
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}	5	-	0.25	-	0.001	0.25	-	7.5	μA
			10	-	0.5	-	0.001	0.5	-	15	
		*	15	-	1.0	-	0.002	1.0	-	30	

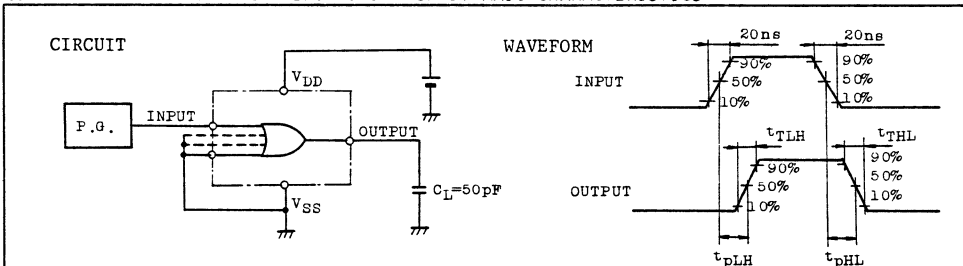
* All valid input combinations.

TC4071BP/BF, TC4072BP/BF, TC4075BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (TC4072BP/BF) (TC4075BP/BF)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (TC4072BP/BF) (TC4075BP/BF)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Output Transition Time (TC4071BP/BF)	t_{TLH}		5	-	130	400	
			10	-	65	200	
			15	-	50	160	
Output Transition Time (TC4071BP/BF)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (TC4071BP/BF)	t_{pLH}		5	-	150	300	
			10	-	75	150	
			15	-	65	130	
Propagation Delay Time (TC4071BP/BF)	t_{pHL}		5	-	150	300	
			10	-	75	150	
			15	-	65	130	
Propagation Delay Time (TC4072BP/BF)	t_{pLH}		5	-	115	250	
			10	-	45	120	
			15	-	30	90	
Propagation Delay Time (TC4072BP/BF)	t_{pHL}		5	-	115	250	
			10	-	45	120	
			15	-	30	90	
Propagation Delay Time (TC4075BP/BF)	t_{pLH}		5	-	95	250	
			10	-	40	120	
			15	-	30	90	
Propagation Delay Time (TC4075BP/BF)	t_{pHL}		5	-	95	250	
			10	-	40	120	
			15	-	30	90	
Input Capacitance	C_{IN}			-	5	7.5	pF

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



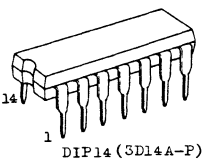
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4073BP/BF, TC4081BP/BF TC4082BP

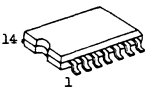
C4073BP/TC4073BF TRIPLE 3 INPUT AND GATE
C4081BP/TC4081BF QUAD 2 INPUT AND GATE
C4028P DUAL 4 INPUT AND GATE

TC4081BP/BF, TC4073BP/BF and TC4082BP are positive logic AND gates with two inputs, three inputs and four inputs respectively.

Since all the outputs of these gates are equipped with the buffer circuits of inverters, the input/output propagation characteristic has been improved and variation of propagation time caused by increase of load capacity is kept minimum.



DIP14 (3D14A-P)



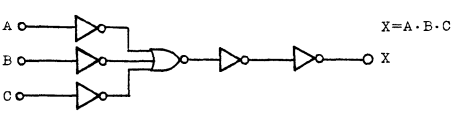
MFP14 (F14GB-P)

ABSOLUTE MAXIMUM RATINGS

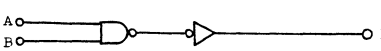
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300 (DIP) / 180 (MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

LOGIC DIAGRAM

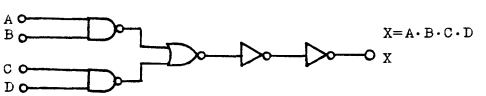
'3 TC4073BP/BF



'4 TC4081BP/BF

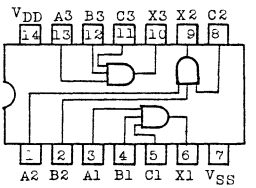


'2 TC4082BP

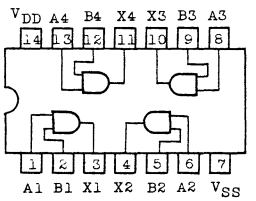


PIN ASSIGNMENT (TOP VIEW)

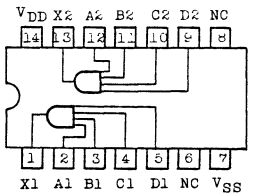
TC4073BP/BF



TC4081BP/BF



TC4082BP



TC4073BP/BF, TC4081BP/BF, TC4082BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS}$, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current (TC4073BP/BF) (TC4082BP/BF)	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{DD}$									
Output Low Current (TC4073BP/BF) (TC4082BP/BF)	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output High Current (TC4081BP/BF)	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V	15	-1.4	-	-1.2		-	-1.0	-	
		$V_{IN}=V_{DD}$									
Output Low Current (TC4081BP/BF)	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}	5	-	0.25	-	0.001	0.25	-	7.5	μA
		*	10	-	0.5	-	0.001	0.5	-	15	
			15	-	1.0	-	0.002	1.0	-	30	

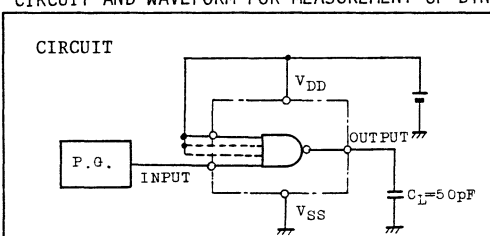
*All valid input combinations.

TC4073BP/BF, TC4081BP/BF, TC4082BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (TC4073BP/BF) (TC4082BP/BF)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (TC4073BP/BF) (TC4082BP/BF)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Output Transition Time (TC4081BP/BF)	t_{TLH}		5	-	130	400	
			10	-	65	200	
			15	-	50	160	
Output Transition Time (TC4081BP/BF)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (TC4073BP/BF)	t_{pLH}		5	-	115	250	
			10	-	50	120	
			15	-	35	90	
Propagation Delay Time (TC4073BP/BF)	t_{pHL}		5	-	115	250	
			10	-	50	120	
			15	-	35	90	
Propagation Delay Time (TC4081BP/BF)	t_{pLH}		5	-	160	300	
			10	-	80	150	
			15	-	70	130	
Propagation Delay Time (TC4081BP/BF)	t_{pHL}		5	-	160	300	
			10	-	80	150	
			15	-	70	130	
Propagation Delay Time (TC4082BP)	t_{pLH}		5	-	110	250	
			10	-	50	120	
			15	-	35	90	
Propagation Delay Time (TC4082BP)	t_{pHL}		5	-	110	250	
			10	-	50	120	
			15	-	35	90	
Input Capacitance	C_{IN}			-	5	7.5	pF

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

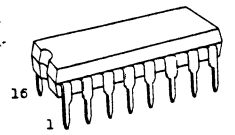


TC4076BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4076BP 4-BIT D-TYPE REGISTER

TC4076BP is the register which consists of four D type flip-flops having 3-stage outputs, and these four flip-flops are controlled by common CLOCK input and RESET input.
When both of INPUT DISABLE inputs G1 and G2 are at "L", data inputs D1 through D4 are stored in F/F's at the rising edge of CLOCK input, and with other combination of G1 and G2, the previous conditions of F/F's are retained even if the rising edge of CLOCK occurs, When both of OUTPUT DISABLE inputs M and N are at "L", the outputs of flip-flops appear at Q1 through Q4 outputs, and with any other combinations of M and N, the outputs have high impedance. RESET is active with "H" level.

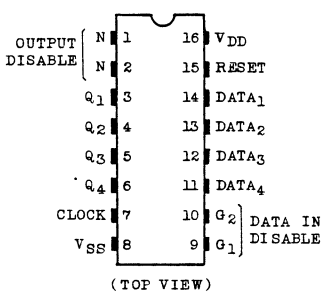


DIP 16(3D16A-P)

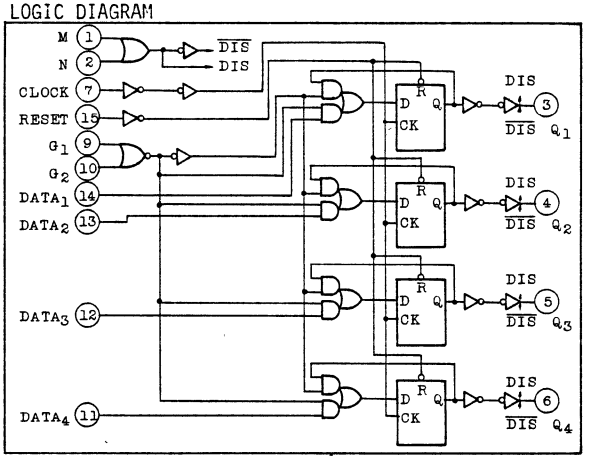
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

RESET	CLOCK	DATA IN DISABLE G_1	DATA IN DISABLE G_2	DATA	OUTPUT DISABLE M	OUTPUT DISABLE N	Q_{n+1}
*	*	*	*	*	H	*	HZ
*	*	*	*	*	*	H	HZ
H	*	*	*	*	L	L	L
L	L	*	*	*	L	L	Q_n
L	↑	H	*	*	L	L	Q_n
L	↑	*	H	*	L	L	Q_n
L	↑	L	L	H	L	L	H
L	↑	L	L	L	L	L	L
L	H	*	*	*	L	L	Q_n
L	↓	*	*	*	L	L	Q_n

Q_{n+1} : NEXT STATE of Q_n
HZ : HIGH IMPEDANCE
* : Don't care

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{CC} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

TC4076BP

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Leakage Current	"H" Level	I_{DH}	V_{OUT}=18V	18	-	0.4	-	10^{-4}	0.4	-	12	μA
	"L" Level	I_{DL}	V_{OUT}=0V	18	-	-0.4	-	-10^{-4}	-0.4	-	-12	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
				10	-	10	-	0.010	10	-	300	
				15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

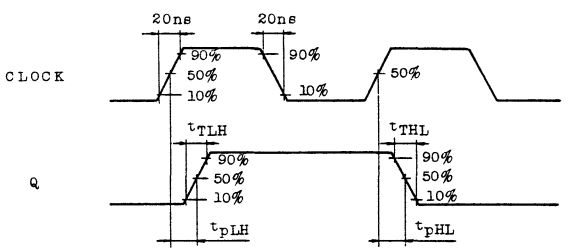
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		5	-	250	600	ns
			10	-	95	250	
			15	-	65	180	
Propagation Delay Time (RESET - Q)	t_{pHL}		5	-	230	460	ns
			10	-	90	200	
			15	-	60	150	
Three State Disable Time (OUTPUT DISABLE - Q)	t_{pHZ} t_{pLZ}	R_L=1kΩ	5	-	100	300	ns
			10	-	45	120	
			15	-	35	90	
Three State Disable Time (OUTPUT DISABLE - Q)	t_{pZH} t_{pZL}	R_L=1kΩ	5	-	110	300	
			10	-	40	150	
			15	-	30	120	
Max. Clock Frequency	f_{CL}		5	3	7	-	MHz
			10	6	21	-	
			15	8	24	-	

)YNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
lin. Clock Pulse Width	t_w		5	-	70	200	ns
			10	-	25	100	
			15	-	20	80	
lin. Pulse Width (RESET)	t_{WH}		5	-	100	200	ns
			10	-	40	80	
			15	-	30	60	
lax. Clock Input Rise ime. lax. Clock Input Fall ime.	t_{rCL} t_{fCL}		5	20	-	-	μs
			10	2.5	-	-	
			15	1.0	-	-	
lin. Set-up Time (DATA - CLOCK)	t_{SU}		5	-	75	150	ns
			10	-	30	60	
			15	-	20	40	
lin. Set-up Time (DATA INPUT DISABLE - CLOCK)	t_{SU}		5	-	100	200	ns
			10	-	40	80	
			15	-	25	50	
Input Capacitance	C_{IN}			-	5	7.5	pF

/AVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

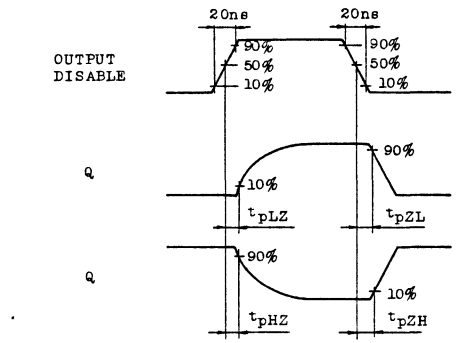
WAVEFORM 1



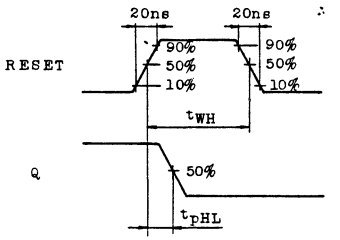
TC4076BP

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

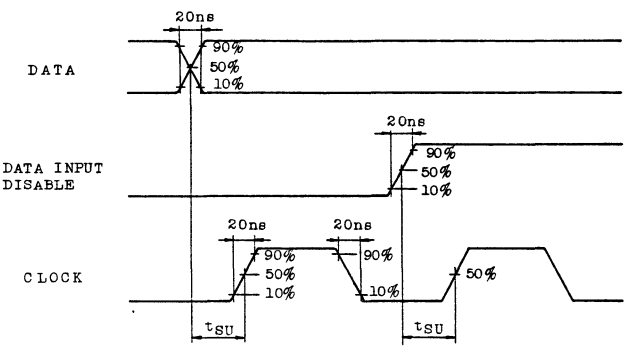
WAVEFORM 2



WAVEFORM 3



WAVEFORM 4



C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4077BP/BF

TC4077BP/TC4077BF QUAD EXCLUSIVE-NOR GATE

The TC4077BP/BF is quad exclusive-NOR gate.
Since all the outputs are provided with the buffers of two stage inverters, the input/output voltage characteristics have been improved. Thus an increase in propagation delay time caused by an increas in load capacity is kept to a minimum.
Therefore, this gate can be widely applied to digital comparators, parity circuits, etc.

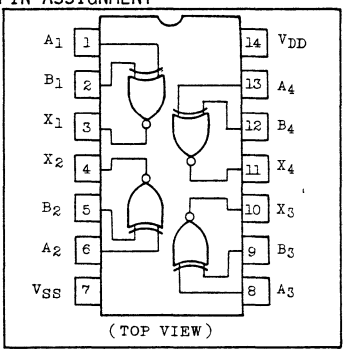
DIP14(3D14A-P)

MFP14(F14GB-P)

MAXIMUM RATINGS

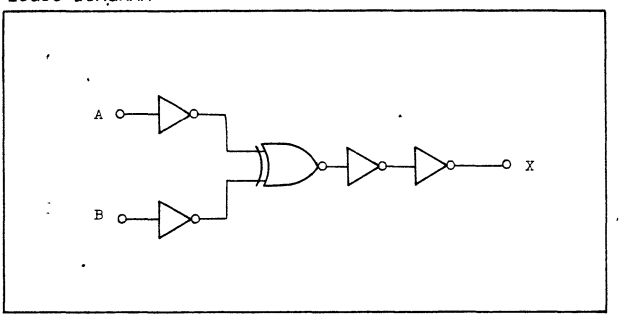
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TRUTH TABLE

INPUTS		OUTPUT
A	B	X
L	L	H
L	H	L
H	L	L
H	H	H

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

TC4077BP/BF

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	1	-	0.001	1	-	7.5	μA
			10	-	2	-	0.001	2	-	15	
			15	-	4	-	0.002	4	-	30	

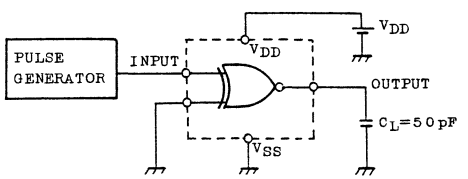
* All valid input combinations.

)YNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

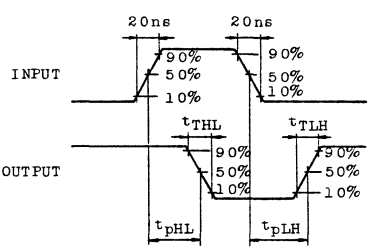
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
)utput Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
)utput Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
?ropagation Delay Time	t_{pLH} t_{pHL}		5	-	130	280	ns
			10	-	60	130	
			15	-	50	100	
Input Capacitance	C_{IN}			-	5	7.5	pF

:IRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

CIRCUIT



WAVEFORM

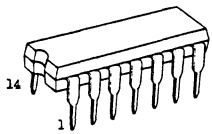


TC4078BP/BF

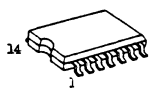
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4Q78BP/TC4078BF 8-INPUT NOR/OR GATE

The TC4078BP/BF is 8-bit positive logic NOR/OR gate. Since each output of this gate is provided with a buffer, the input/output voltage characteristics have been improved, allowing noise immunity to be elevated; thus, the variation of propagation delay time due to the increase in load capacity is kept to the minimum.



DIP14(3D14A-P)

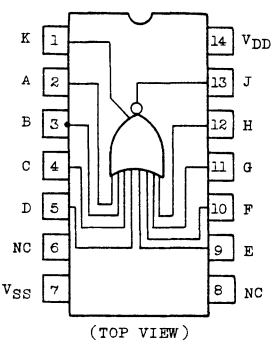


MFP14(F14GB-P)

MAXIMUM RATINGS

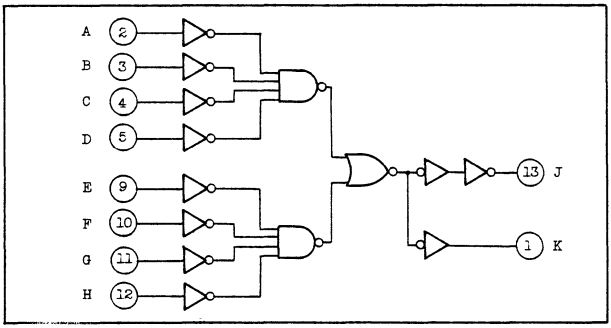
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	Tsol	260°C · 10sce	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\| < 1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\| < 1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	0.25	-	0.001	0.25	-	7.5	μA
			10	-	0.5	-	0.001	0.5	-	15	
			15	-	1.0	-	0.002	1.0	-	30	

* All valid input combinations.

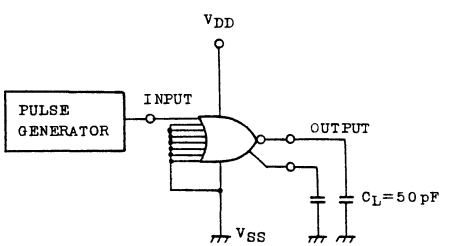
TC4078BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

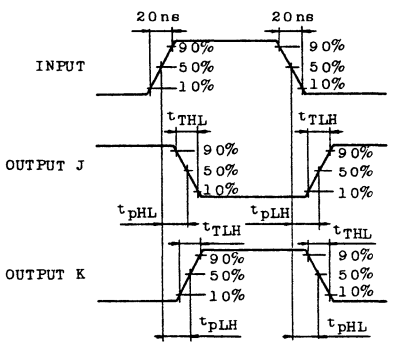
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time	t_{pLH} t_{pHL}		5	-	170	340	ns
			10	-	70	140	
			15	-	50	110	
Input Capacitance	C_{IN}			-	5	7.5	pF

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

CIRCUIT



WAVEFORM



C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

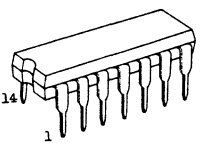
TC4085BP

TC4085BP DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

TC4085BP contains two circuits of AND-OR select gates and the outputs are inverted. The circuit consists of two 2 input AND gates and one NOR gate, and the logical equation of the output is as follows.

$$OUT = \overline{A \cdot B + C \cdot D + INH}$$

If INH input is set at "H", the select operation is inhibited having OUT="L", so that this input can be used as an expander terminal for connecting TC4081B, etc.

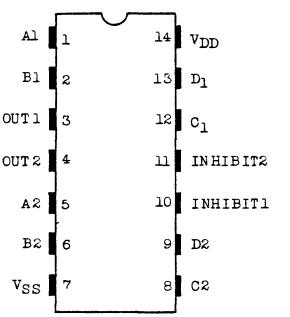


DIP14(3D14A-P)

ABSOLUTE MAXIMUM RATINGS

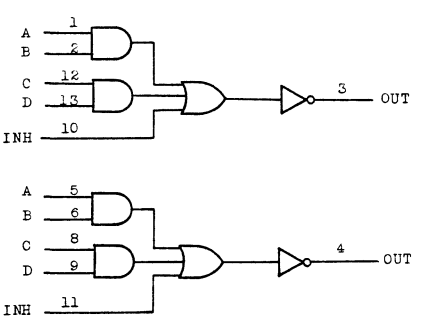
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input Voltage	V_{IN}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output Voltage	V_{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



$$OUT = \overline{A \cdot B + C \cdot D + INH}$$

TC4085BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

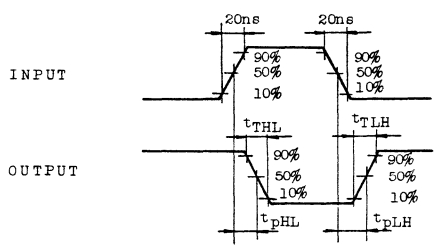
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}$, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	15.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}$, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	mA
		V_{OH}=2.5V	5	-	-	-		-	-	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V	15	-1.4	-	-1.2		-	-1.0	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}	5	-	1	-	0.001	1	-	7.5	μA
			10	-	2	-	0.001	2	-	15	
		*	15	-	4	-	0.002	4	-	30	

* All valid input combinations.

)YNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNITS
)utput Transition Time (Low to High)	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
)utput Transition Time (High to Low)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
'ropagation Delay Time (A, B, C, D - OUT)	t_{pLH}		5	-	290	600	
			10	-	110	220	
			15	-	75	160	
'ropagation Delay Time (A, B, C, D - OUT)	t_{pHL}		5	-	275	600	
			10	-	100	220	
			15	-	70	160	
'ropagation Delay Time (INH - OUT)	t_{pLH}		5	-	230	460	
			10	-	90	180	
			15	-	60	120	
ropagation Delay Time (INH - OUT)	t_{pHL}		5	-	210	460	
			10	-	80	180	
			15	-	55	120	
nput Capacitance	C_{IN}			-	5	7.5	pF

AVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

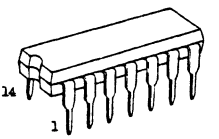


TC4086BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4086BP EXPANDABLE 4-WIDE 2-INPUT AND-OR-INVERT GATE

TC4086BP contains four 2 input AND gates and one OR gate which logically adds (OR) all the AND gates having an expander input to form AND-OR-select gate, and the output is inverted.
INH/$\overline{EXP}$ input and ENABLE/EXP input are the expander inputs to connect other AND gates and select gate and these can be used as INHIBIT input to inhibit the select operation besides of the expander function.

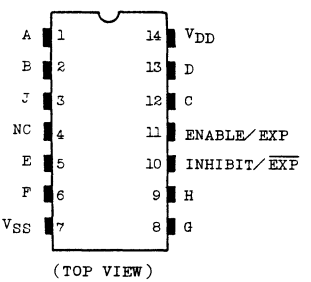


DIP 14 (3D14A-P)

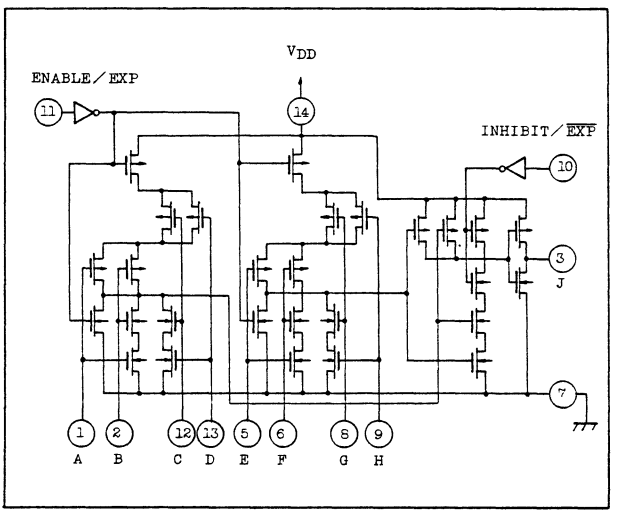
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

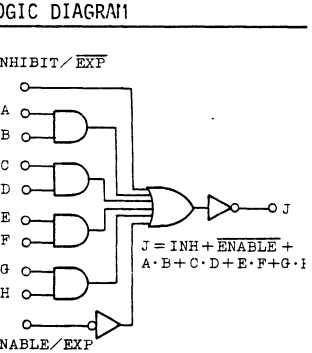
PIN ASSIGNMENT



CIRCUIT DIAGRAM



LOGIC DIAGRAM



COMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
ɔut Voltage	V_{IN}		0	-	V_{DD}	V

ATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

HARACTERISTIC		SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
gh-Level tput Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
w-Level tput Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
tput High rrent		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
tput Low rrent		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
put High ltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
ɹput Low ɹltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
ɹput ɪrrent	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

TC4086BP

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

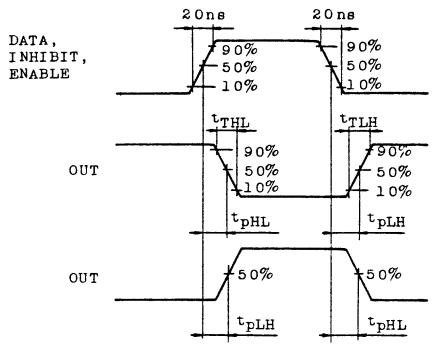
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	1	-	0.001	1	-	7.5	μA
			10	-	2	-	0.002	2	-	15	
			15	-	4	-	0.004	4	-	30	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (DATA - OUT)	t_{pLH}		5	-	110	450	ns
			10	-	45	180	
			15	-	30	120	
Propagation Delay Time (DATA - OUT)	t_{pHL}		5	-	110	450	
			10	-	45	180	
			15	-	35	120	
Propagation Delay Time (INHIBIT - OUT)	t_{pLH}		5	-	75	300	ns
			10	-	35	120	
			15	-	25	80	
Propagation Delay Time (INHIBIT - OUT)	t_{pHL}		5	-	70	300	
			10	-	30	120	
			15	-	25	80	
Propagation Delay Time (ENABLE - OUT)	t_{pLH}		5	-	95	300	ns
			10	-	40	120	
			15	-	30	80	
Propagation Delay Time (ENABLE - OUT)	t_{pHL}		5	-	90	300	
			10	-	40	120	
			15	-	30	80	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

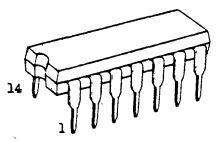


TC4093BP/BF

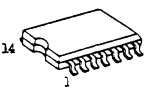
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4093BP/TC4093BF QUAD 2-INPUT NAND SCHMITT TRIGGERS

The TC4093BP/BF is a quad 2-input NAND gate having Schmitt trigger function for all the input terminals. Since the circuit threshold voltage varies with rising time and falling time of the input waveform (V_P and V_N), this gate can be used for a wide variety of applications to line receivers, waveform shaping. astable multivibrators, monosatable multivibrators, etc. in addition to requalar NAND gates.
As the TC4093BP/BF and the TC4011B are identical in pin assignment, they are compatible each other.



DIP14(3D14A-P)

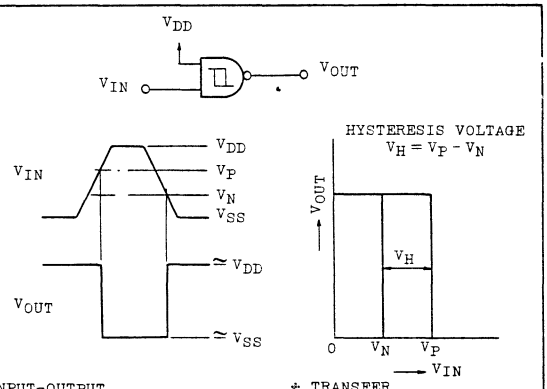


MFP14(F14GB-P)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

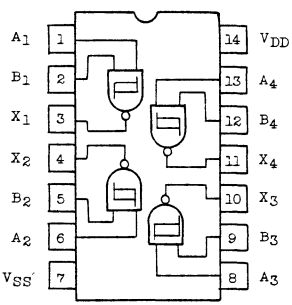
INPUT-OUTPUT CHARACTERISTIC



* INPUT-OUTPUT VOLTAGE WAVEFORM

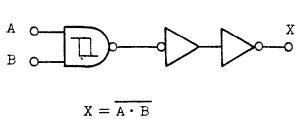
* TRANSFER CHARACTERISTICS

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



$X = \overline{A \cdot B}$

:OMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
›ut Voltage	V_{IN}		0	-	V_{DD}	V

ATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

IARACTERISTIC		SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
;h-Level :put Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
›-Level :put Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
:put High :rent		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
:put Low :rent		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{DD}$									
gh Threshold ltage		V_P	V_{OUT}=0.5V, 4.5V	5	-	-	2.05	2.8	3.55	-	-	V
			V_{OUT}=1.0V, 9.0V	10	-	-	4.1	5.3	7.0	-	-	
			V_{OUT}=1.5V,13.5V	15	-	-	6.2	7.8	10.4	-	-	
w Threshold ltage		V_N	V_{OUT}=0.5V, 4.5V	5	-	-	1.5	2.3	3.15	-	-	
			V_{OUT}=1.0V, 9.0V	10	-	-	3.2	4.5	6.3	-	-	
			V_{OUT}=1.5V,13.5V	15	-	-	4.8	6.6	9.3	-	-	
steresis ltage		V_H		5	-	-	0.2	0.5	0.85	-	-	
				10	-	-	0.3	0.8	1.4	-	-	
				15	-	-	0.45	1.2	1.9	-	-	
put rrent	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

TC4093BP/BF

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	1	-	0.001	1	-	7.5	μA
			10	-	2	-	0.002	2	-	15	
			15	-	4	-	0.004	4	-	30	

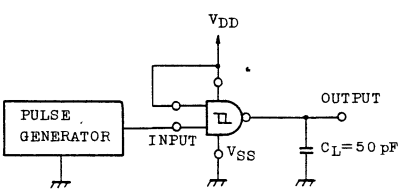
* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time	t_{pLH} t_{pHL}		5	-	130	260	ns
			10	-	60	120	
			15	-	40	80	
Input Capacitance	C_{IN}			-	5	7.5	pF

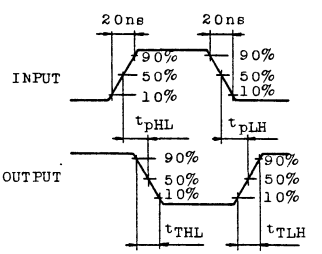
CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

CIRCUIT



DUTY RATIO=50%, f=500kHz

WAVEFORM

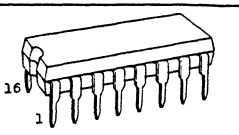


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

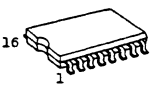
TC4094BP/BF

TC4094BP/TC4094BF 8-STAGE SHIFT-AND-STORE BUSREGISTER

TC4094BP/BF is a SHIFT and STORE REGISTER that consists of an 8-bit shift register and an 8-bit latch. The read data in the shift register can be taken in the latch through the asynchronous STROBE input; therefore, the data transfer mode can hold output. And, since the parallel output is of 3-state construction, it can be directly connected to the 8-bit busline.
This register can be applied to Serial-to-parallel conversion, data receivers, etc.



DIP 16(3D16A-P)

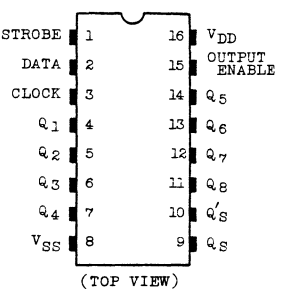


MFP 16(F16GC-P)

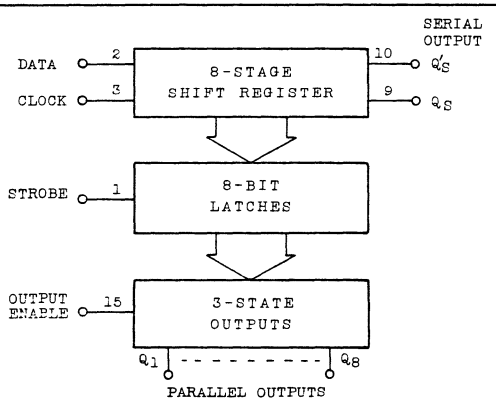
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



BLOCK DIAGRAM



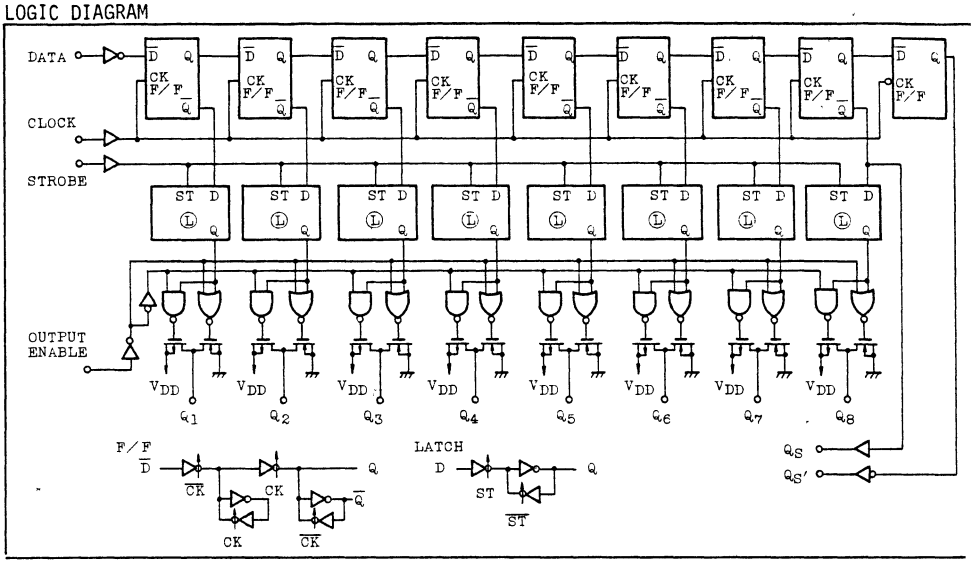
TRUTH TABLE

CK	OE	ST	D	PO		SO	
				Q_1	Q_n	Q_S	Q'_S
↑	H	H	L	L	Q_{n-1}	Q_7	NC
↑	H	H	H	H	Q_{n-1}	Q_7	NC
↑	H	L	*	NC	NC	Q_7	NC
↑	L	*	*	HZ	HZ	Q_7	NC
↓	H	*	*	NC	NC	NC	Q_S
↓	L	*	*	HZ	HZ	NC	Q_S

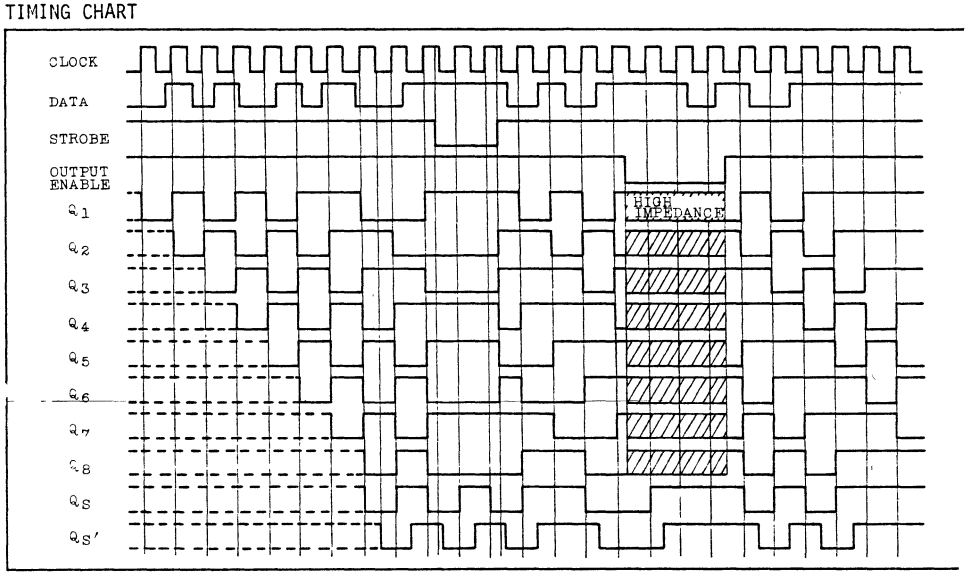
CK = Clock
OE = Output Enable
ST = Strobe
D = Data
PO = Parallel Outputs
SO = Serial Output
* = Don't care
NC = No Change
HZ = High Impedance

TC4094BP/BF

LOGIC DIAGRAM



TIMING CHART



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

TC4094BP/BF

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Leakage Current	"H" Level	I_{DH}	V_{OH}=18V	18	-	0.4	-	10^{-4}	0.4	-	12	μA
	"L" Level	I_{DL}	V_{OH}=0V	18	-	-0.4	-	-10^{-4}	-0.4	-	-12	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
				10	-	10	-	0.010	10	-	300	
				15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

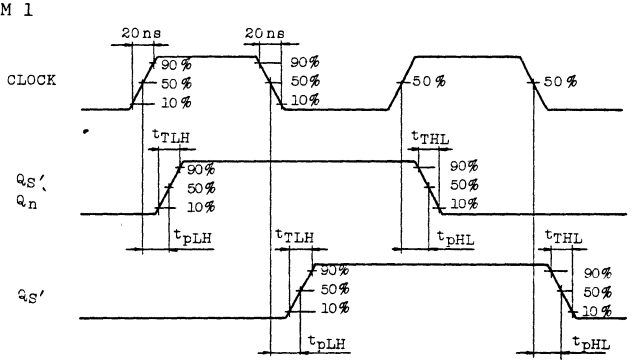
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Qs)	t_{pLH} t_{pHL}		5	-	200	600	ns
			10	-	80	250	
			15	-	55	190	
Propagation Delay Time (CLOCK - Qs')	t_{pLH} t_{pHL}		5	-	200	460	ns
			10	-	80	220	
			15	-	55	150	
Propagation Delay Time (CLOCK - Qn)	t_{pLH} t_{pHL}		5	-	290	840	ns
			10	-	110	390	
			15	-	75	270	
Propagation Delay Time (STROBE - Qn)	t_{pLH} t_{pHL}		5	-	230	580	ns
			10	-	90	290	
			15	-	60	200	
Three State Disable Time (OUTPUT ENABLE - Qn)	t_{pHZ} t_{pZL}	R_L=1kΩ	5	-	100	280	ns
			10	-	40	150	
			15		30	110	

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Three State Disable Time (OUTPUT ENABLE - Qn)	t_{pLZ} t_{pZH}	R_L=1kΩ	5	-	90	450	ns
			10	-	45	190	
			15	-	35	140	
Min. Clock Pulse Width	t_w		5	-	65	200	ns
			10	-	25	100	
			15	-	20	80	
Min. Pulse Width (STROBE)	t_{WH}		5	-	65	200	ns
			10	-	25	80	
			15	-	15	70	
Max. Clock Frequency	f_{CL}		5	1.25	8	-	MHz
			10	2.5	19	-	
			15	3	25	-	
Max. Clock Input Rise Time. Max. Clock Input Fall Time.	t_{rCL} t_{fCL}		5	20	-	-	μs
			10	2.5	-	-	
			15	1	-	-	
Min. Set-up Time (DATA - CLOCK)	t_{SU}		5	-	20	125	ns
			10	-	8	55	
			15	-	6	35	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

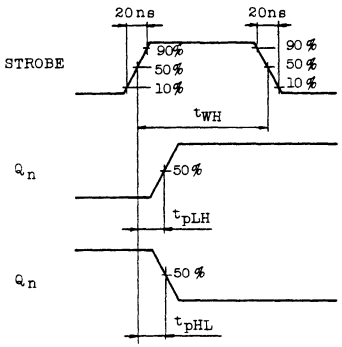
WAVEFORM 1



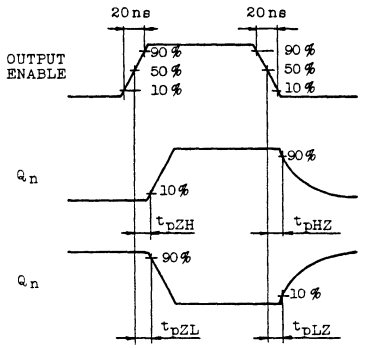
TC4094BP/BF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

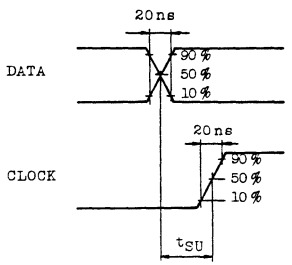
WAVEFORM 2



WAVEFORM 3



WAVEFORM 4

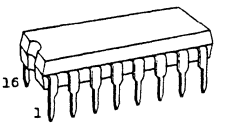


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

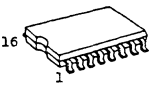
TC4099BP/BF

TC4099BP/TC4099BF 8-BIT ADDRESSABLE LATCH

TC4099BP/BF is eight bit latch having one common data input line and eight independent output lines and the latches are controlled by three bit binary address inputs (A_0, A_1 and A_2).
When WRITE DISABLE input and RESET input is "L", the data is written into the bit selected by the binary address input and other bits retain their previous conditions. When W. DISABLE input becomes "H", write into any bits is inhibited. When W. DISABLE input and RESET input are "H", all the bits are reset to "L".



DIP 16(3D16A-P)

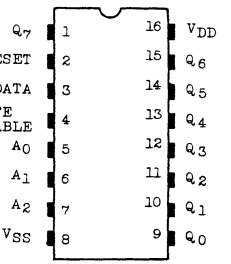


MFP 16(F16GC-P)

MAXIMUM RATINGS

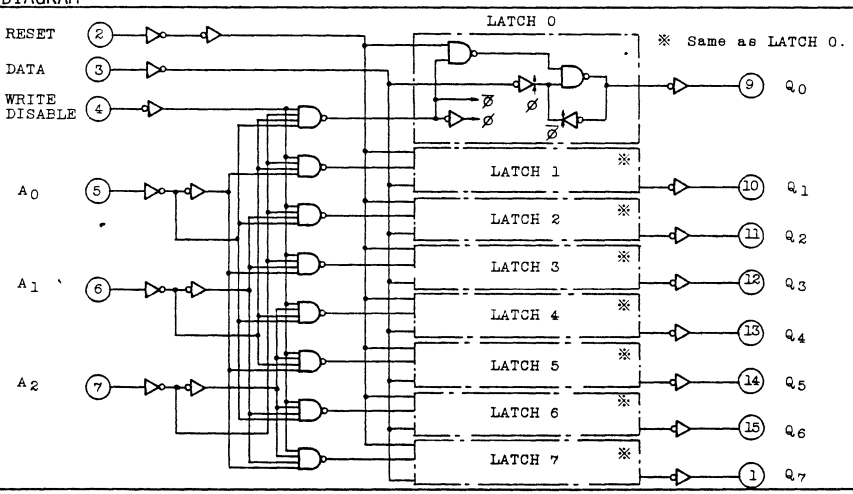
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TC4099BP/BF

TRUTH TABLE

CONTROL INPUTS		ADDRESS INPUTS			OUTPUTS							
RESET	WRITE DISABLE	A_2	A_1	A_0	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
H	H	*	*	*	L	L	L	L	L	L	L	L
L	H	*	*	*	-	-	-	-	-	-	-	-
H	L	L	L	L	D	L	L	L	L	L	L	L
H	L	L	L	H	L	D	L	L	L	L	L	L
H	L	L	H	L	L	L	D	L	L	L	L	L
H	L	L	H	H	L	L	L	D	L	L	L	L
H	L	H	L	L	L	L	L	L	D	L	L	L
H	L	H	L	H	L	L	L	L	L	D	L	L
H	L	H	H	L	L	L	L	L	L	L	D	L
H	L	H	H	H	L	L	L	L	L	L	L	D
L	L	L	L	L	D	-	-	-	-	-	-	-
L	L	L	L	H	-	D	-	-	-	-	-	-
L	L	L	H	L	-	-	D	-	-	-	-	-
L	L	L	H	H	-	-	-	D	-	-	-	-
L	L	H	L	L	-	-	-	-	D	-	-	-
L	L	H	L	H	-	-	-	-	-	D	-	-
L	L	H	H	L	-	-	-	-	-	-	D	-
L	L	H	H	H	-	-	-	-	-	-	-	D

*: Don't care D : Data input - : Holds previous data

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	V
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\| < 1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\| < 1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	μA
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

*All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	

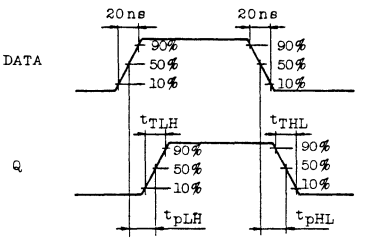
TC4099BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

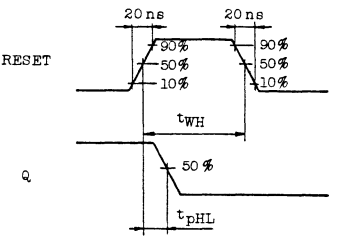
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (DATA - Q)	t_{pLH} t_{pHL}		5	-	160	400	ns
			10	-	65	150	
			15	-	50	100	
Propagation Delay Time (WRITE DISABLE - Q)	t_{pLH} t_{pHL}		5	-	200	400	ns
			10	-	80	160	
			15	-	55	120	
Propagation Delay Time (ADDRESS - Q)	t_{pLH} t_{pHL}		5	-	240	480	ns
			10	-	95	200	
			15	-	70	150	
Propagation Delay Time (RESET - Q)	t_{pHL}		5	-	170	350	ns
			10	-	70	160	
			15	-	50	130	
Min. Pulse Width (DATA)	t_w		5	-	120	240	ns
			10	-	50	100	
			15	-	35	80	
Min. Pulse Width (ADDRESS)	t_w		5	-	60	400	ns
			10	-	20	200	
			15	-	15	125	
Min. Pulse Width (RESET)	t_{WH}		5	-	70	150	ns
			10	-	25	75	
			15	-	20	50	
Min. Set-up Time (DATA - WRITE DISABLE)	t_{SU}		5	-	15	100	ns
			10	-	7.5	50	
			15	-	5	35	
Min. Hold Time (DATA - WRITE DISABLE)	t_H		5	-	15	150	ns
			10	-	7.5	75	
			15	-	5	50	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

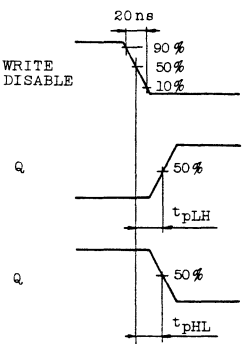
WAVEFORM 1



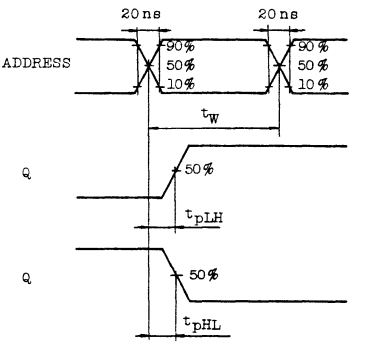
WAVEFORM 2



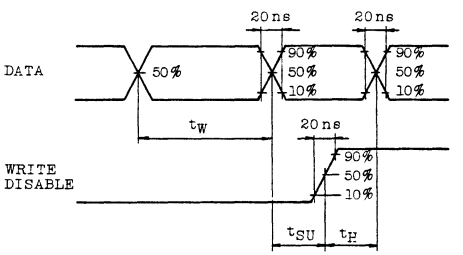
WAVEFORM 3



WAVEFORM 4



WAVEFORM 5



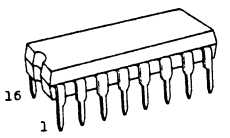
TC40102BP
TC40103BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40102BP 8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTER (2-Decade BCD Type)

TC40103BP 8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTER (8-Bit Bynary Type)

The TC40102BP and TC40103BP are 8-stage presettable synchronous down counters. Output terminal $\overline{CO/ZD}$ is placed in active mode at "L" level when the contents of count become zero.
As the TC40102BP adopts BCD binary coded decimal notation, setting up to 99 counts is possible. The TC40103BP, with 8-bit binary construction, can set up to 255 counts. Each type has $\overline{CI/CE}$ inhibiting clock, $\overline{APE}$ asynchronous preset control input, $\overline{SPE}$ synchronous preset control input and $\overline{CLEAR}$ control input setting counter to maximum counting mode.
Clock input, with Schmitt function, can accept clock waveform with slow rise and fall edge.

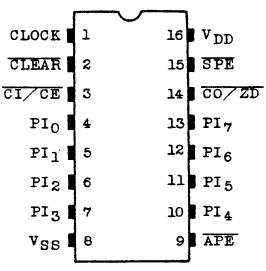


DIP 16(3D16A-P)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

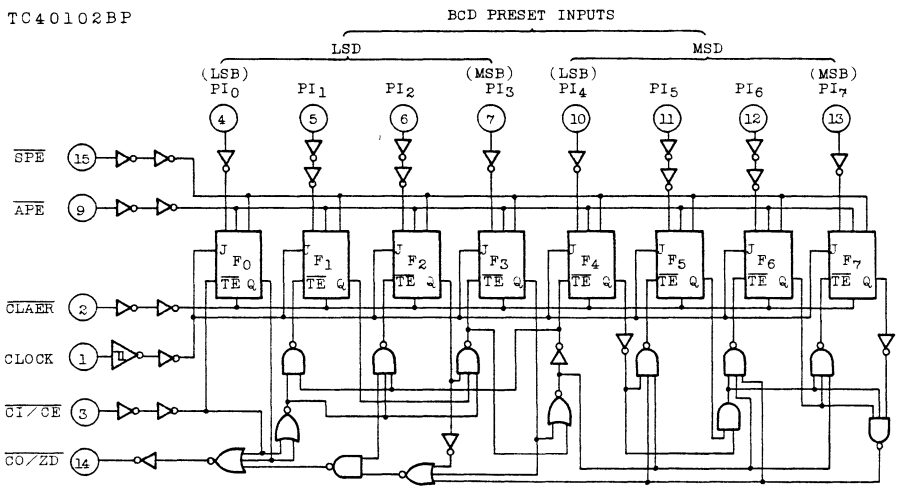
CONTROL INPUT				MODE	FUNCTIONAL DESCRIPTION
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$		
H	H	H	H	Count inhibit	Even if clock is given, no count is made.
H	H	H	L	Regular count	Down count at rising edge of clock.
H	H	L	*	Synchronous preset	Data of PI terminal is preset at rising edge of clock.
H	L	*	*	Asynchronous preset	Data of PI terminal is asynchronously preset to clock.
L	*	*	*	Clear	Counter is set to maximum count.

Note 1. * : Don't care
2. Maximum count: "99" for TC40102BP and "255" for TC40103BP.

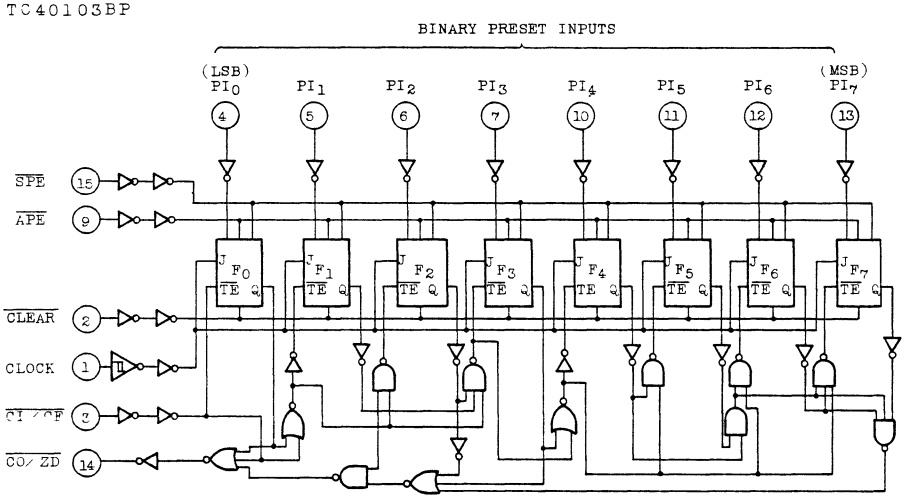
TC40102BP, TC40103BP

LOGIC DIAGRAM

TC40102BP

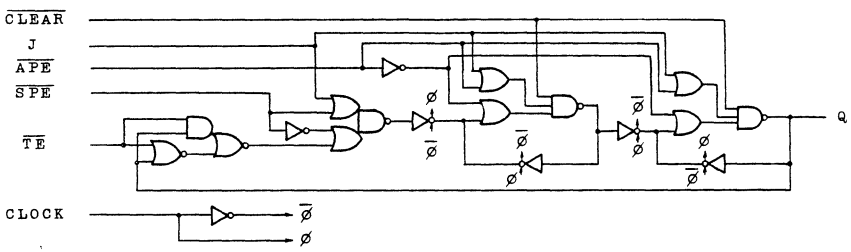


TC40103BP



TC40102BP, TC40103BP

INTERNAL FLIP-FLOP (F0~F7) CIRCUIT DIAGRAM AND TRUTH TABLE OF COUNTER



INTERNAL FLIP-FLOP TRUTH TABLE

INPUT						OUTPUT
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	J	$\overline{TE}$	CLOCK	Q_{n+1}
L	※	※	※	※	※	H
H	L	※	L	※	※	H
H	L	※	H	※	※	L
H	H	L	L	※	↓	H
H	H	L	H	※	↓	L
H	H	L	※	※	↑	Q_n
H	H	H	※	L	↓	$\overline{Q_n}$
H	H	H	※	H	※	Q_n

FUNCTIONAL DESCRIPTION

The TC40102BP and TC40103BP are 8-stage presettable synchronous down counters. Carry Out/Zero Deffect ($\overline{CO/ZD}$) is output at the "L" level for the period of 1 bit when the readout becomes "0". The TC40102BP adopts binary coded decimal notation, making setting up to 99 counts possible. While the TC40103BP adopts 8-bit binary counter and can set up to 255 counts.

COUNT OPERATION

At the "H" level of control input of $\overline{CLEAR}$, $\overline{SPE}$ and $\overline{APE}$, the counter carries out down count operation one by one at the rise of pulse given to CLOCK input. Count operation can be inhibited by setting Carry Input/Clock Enable ($\overline{CI/CE}$) to the "H" level. $\overline{CO/ZD}$ is output at the "L" level when the readout becomes "0", but is not output even if the readout becomes "0" when $\overline{CI/CE}$ is at the "H" level, thus maintaining the "H" level.

Synchronous cascade operation can be carried out by using $\overline{CI/CE}$ input and $\overline{CO/ZD}$ output.

FUNCTION DESCRIPTION (Cont'd)

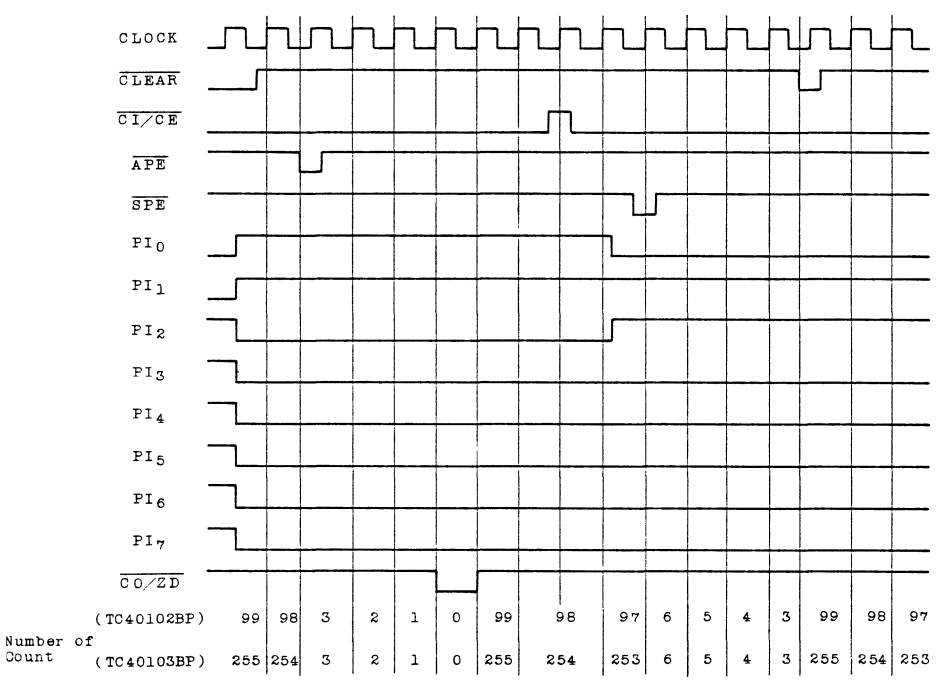
The contents of count jump to maximum count (99 for the TC40102BP and 255 for the TC40103BP) if clock is given when the readout is "0". Therefore, operation of 100-frequency division and that of 256-frequency division are carried out for the TC40102BP and TC40103BP, respectively, when clock input alone is given without various kinds of preset operations. To clock input is attached Schmitt gate.

PRESET OPERATION AND RESET OPERATION

When Clear ($\overline{CLEAR}$) input is set to the "L" level, the readout is set to the maximum count independently of other inputs. When Asynchronous Preset Enable ($\overline{APE}$) input is set to the "L" level, readouts given on P.10 to P.17 can be preset asynchronously to counter independently of inputs other than $\overline{CLEAR}$ input. When Synchronous Preset Enable ($\overline{SPE}$) is set to the "L" level, the readouts given on P.10 to P.17 can be preset to counter synchronously with the rise of clock.

As to these operation modes, refer to the truth table.

TIMING CHART



TC40102BP, TC40103BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - $\overline{CO/ZD}$)	t_{pLH} t_{pHL}		5	-	400	800	ns
			10	-	150	300	
			15	-	110	220	
Propagation Delay Time ($\overline{CI/CE}$ - $\overline{CO/ZD}$)	t_{pLH} t_{pHL}		5	-	200	400	ns
			10	-	90	180	
			15	-	65	130	
Propagation Delay Time ($\overline{APE}$ - $\overline{CO/ZD}$)	t_{pLH} t_{pHL}		5	-	350	1300	ns
			10	-	130	600	
			15	-	100	400	
Propagation Delay Time ($\overline{CLEAR}$ - $\overline{CO/ZD}$)	t_{pLH}		5	-	300	750	ns
			10	-	120	360	
			15	-	90	200	
Min. Clock Pulse Width	t_w		5	-	100	300	ns
			10	-	40	180	
			15	-	30	80	
Min. Pulse Width ($\overline{CLEAR}$)	t_{WL}		5	-	140	320	ns
			10	-	60	160	
			15	-	45	100	

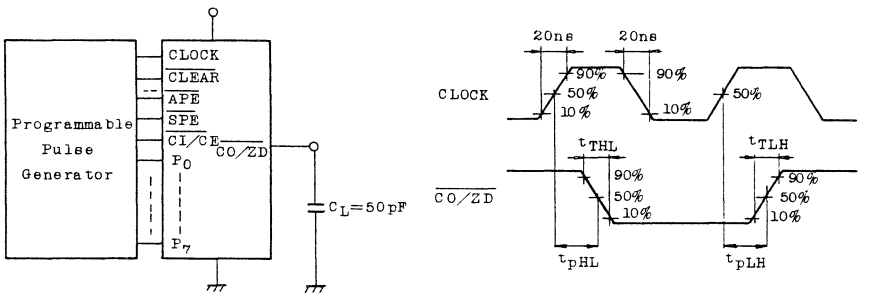
TC40102BP, TC40103BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

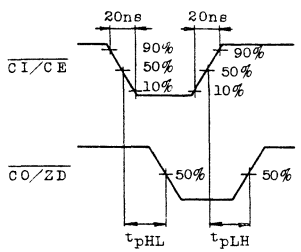
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Min. Pulse Width ($\overline{APE}$)	t_{WL}		5	-	120	360	ns
			10	-	45	160	
			15	-	35	120	
Max. Clock Frequency	f_{CL}		5	0.7	2	-	MHz
			10	1.8	5	-	
			15	2.4	8	-	
Max. Clock Input Rise Time. Max. Clock Input Fall Time.	t_{rCL} t_{fCL}		5	No Limit			μs
			10				
			15				
Min. Set-up Time ($\overline{SPE}$ - CLOCK)	t_{SU}		5	-	120	280	ns
			10	-	75	150	
			15	-	70	140	
Min. Set-up Time (PI - CLOCK)	t_{SU}		5	-	30	100	ns
			10	-	10	50	
			15	-	5	40	
Min. Set-up Time ($\overline{CI/CE}$ - CLOCK)	t_{SU}		5	-	300	600	ns
			10	-	100	250	
			15	-	70	150	
Min. Set-up Time (PI - $\overline{APE}$)	t_{SU}		5	-	150	300	ns
			10	-	60	120	
			15	-	40	80	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

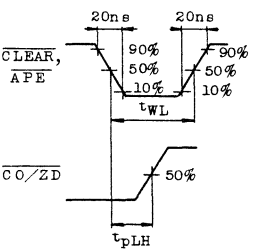
WAVEFORM 1



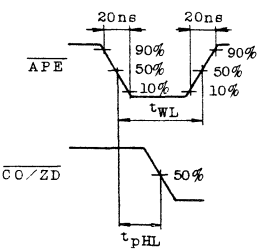
WAVEFORM 2



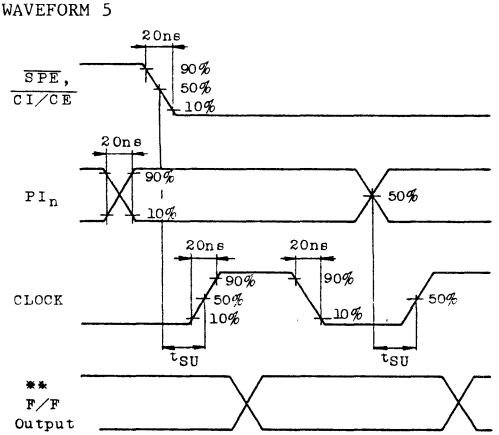
WAVEFORM 3



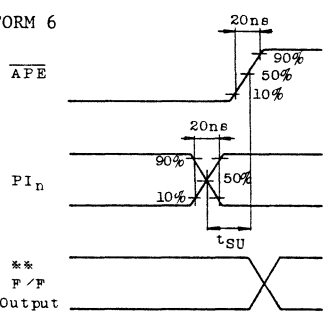
WAVEFORM 4



WAVEFORM 5



WAVEFORM 6

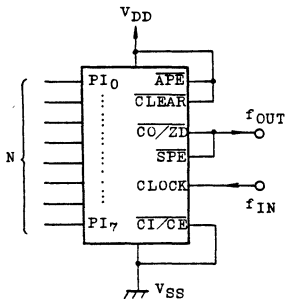


(** F/F output is internal signal of IC.)

TC40102BP, TC40103BP

APPLICATION CIRCUIT

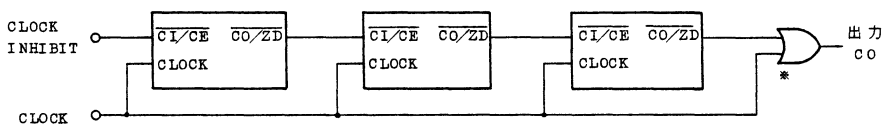
PROGRAMMABLE DIVIDE-BY-N COUNTER



- $f_{OUT} = \frac{f_{IN}}{N+1}$
- Timing chart when N="3" (PIO, PI1=V_{DD}, PI2 ~ PI7=V_{SS})

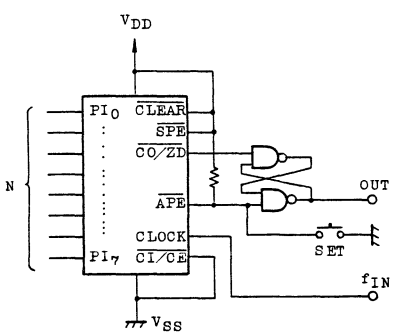
- TC40102BP...1/2 to 1/100 are dividable.
- TC40103BP...1/2 to 1/256 are dividable.

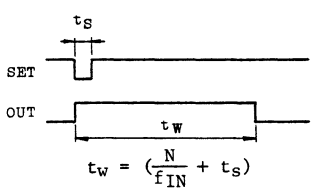
PARALLEL CARRY CASCADING



* At synchronous cascade connection, buzzard occurs at CO output after its second stage when digit place changes, due to delay arrival. Therefore, take gate from TC4071BP or the like, not from CO output at the rear stage directly.

PROGRAMMABLE TIMER





$$t_W = \left(\frac{N}{f_{IN}} + t_S\right)$$

Note: The above formula does not take into account the phase of clock input. Therefore, the real pulse width is the distance between the above formula-1/f_{IN}~ the above formula.

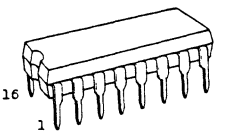
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40104BP
TC40194BP

TC40104BP 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE OUTPUTS

TC40194BP 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH ASYNCHRONOUS MASTER RESET

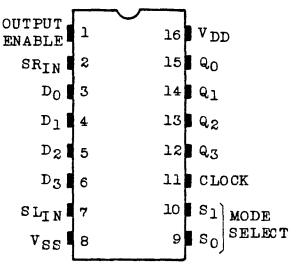
The TC40104BP and TC40194BP are 4-bit shift registers with parallel output, parallel input, shift right and shift left inputs.
To the TC40104BP is attached OUTPUT ENABLE input which can place output terminal into high impedance.
Also, to the TC40194BP is attached $\overline{\text{RESET}}$ input which can clear the contents of registers asynchronously.
In parallel data preset mode, data of $D_0 \sim D_3$ are not only preset in the internal register, but output to each Q output, at the rise of clock, Shift right and shift left inputs are inhibited during the time.
In shift right and shift left modes, data from shift right and shift left inputs are shifted to the right and to the left by 1 bit, respectively, synchronously with the rise of clock.
The TC40194BP is function and pin compatible with the 74194 of TTL.



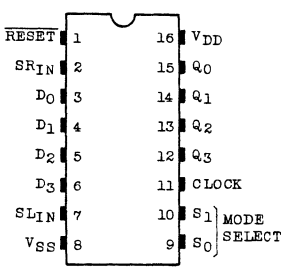
DIP 16(3D16A-P)

PIN ASSIGNMENT (TOP VIEW)

TC40104BP



TC40194BP



TRUTH TABLE

TC40104BP

CLOCK	MODE SELECT		OUTPUT ENABLE	OPERATION MODE
	S_0	S_1		
↑	L	L	H	RESET
↑	H	L	H	SHIFT RIGHT($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$)
↑	L	H	H	SHIFT LEFT ($Q_3 \rightarrow Q_2 \rightarrow Q_1 \rightarrow Q_0$)
↑	H	H	H	PARALLEL DATA PRESET
*	*	*	L	OUTPUT HIGH IMPEDANCE

* : Don't care

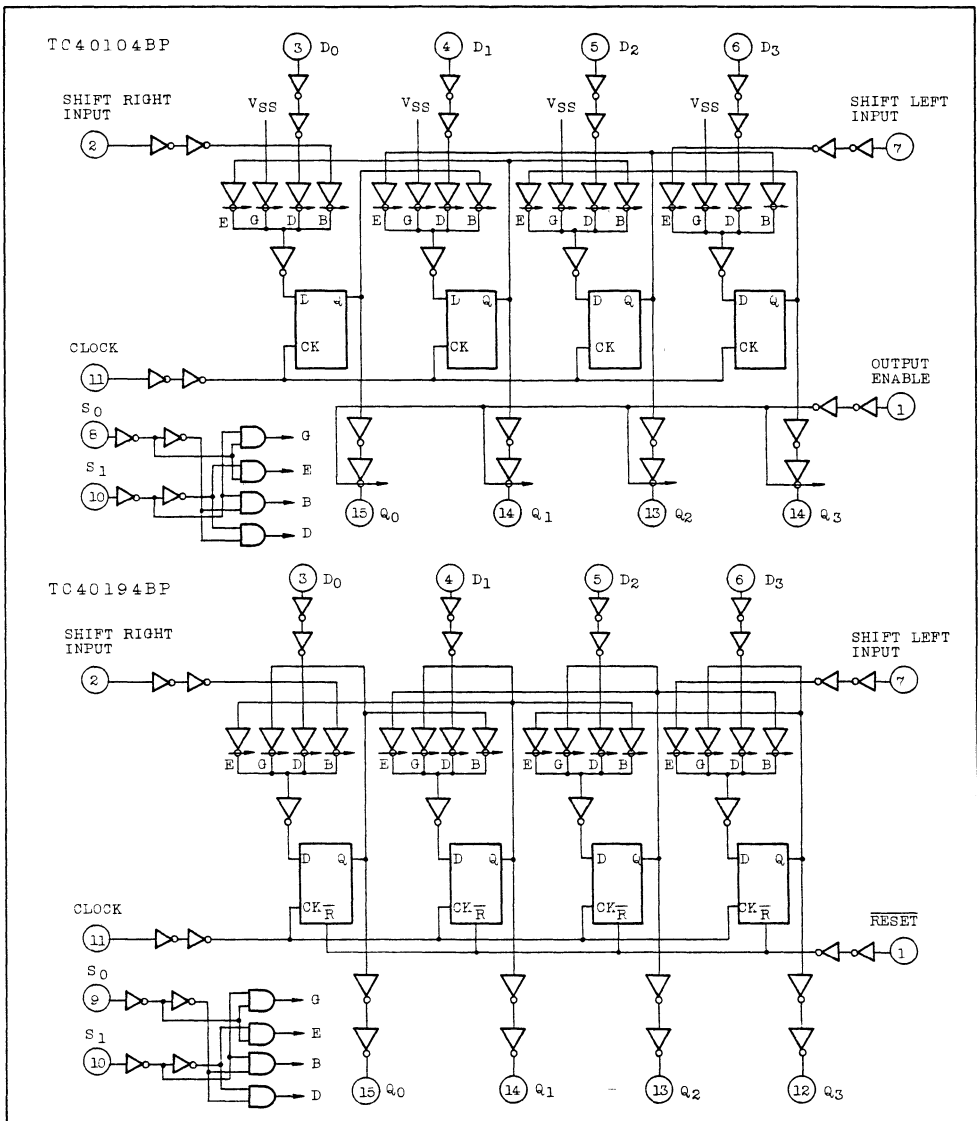
TC40194BP

CLOCK	MODE SELECT		$\overline{\text{RESET}}$	OPERATION MODE
	S_0	S_1		
*	L	L	H	HOLD
↑	H	L	H	SHIFT RIGHT($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$)
↑	L	H	H	SHIFT LEFT ($Q_3 \rightarrow Q_2 \rightarrow Q_1 \rightarrow Q_0$)
↑	H	H	H	PARALLEL DATA PRESET
*	*	*	L	RESET

* : Don't care

TC40104BP, TC40194BP

LOGIC DIAGRAM



TC40104BP, TC40194BP

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									

TC40104BP, TC40194BP

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
3-State ◎ Output Leakage Current	"H" Level	I_{DH}	V_{DH}=18V	18	-	0.4	-	10^{-4}	0.4	-	12	μA
	"L" Level	I_{DL}	V_{DL}=0V	18	-	-0.4	-	-10^{-4}	-0.4	-	-12	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
				10	-	10	-	0.010	10	-	300	
				15	-	20	-	0.015	20	-	600	

◎ Only TC40104BP * All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		5	-	220	440	ns
			10	-	90	200	
			15	-	60	140	
Three State Disable Time (OUTPUT ENABLE - Q) ◎	t_{pZH} t_{pZL}	R_L=1kΩ	5	-	80	160	ns
			10	-	35	70	
			15	-	25	50	

YNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

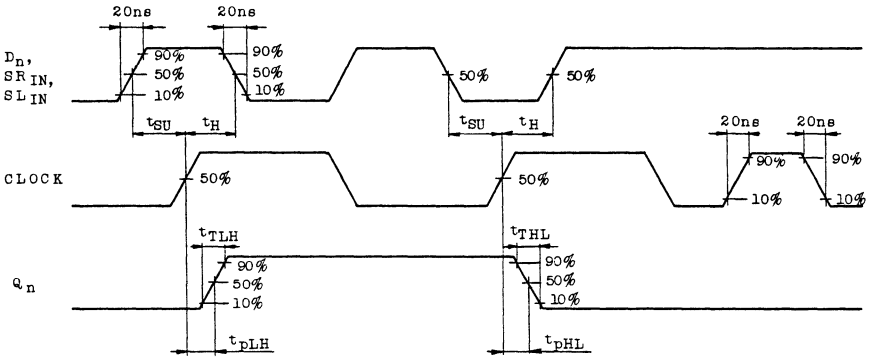
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
hree State Disable ime (OUTPUT ENABLE - Q) ©	t_{pLZ} t_{pHZ}	R_L=1kΩ	5	-	55	110	ns
			10	-	30	60	
			15	-	25	50	
ropagation Delay Time ($\overline{RESET}$ - Q) *	t_{pHL}		5	-	160	460	ns
			10	-	65	180	
			15	-	50	130	
in. Clock Pulse Width	t_w		5	-	70	180	ns
			10	-	40	80	
			15	-	25	50	
in. Pulse Width ($\overline{RESET}$) *	t_{WL}		5	-	100	200	
			10	-	40	80	
			15	-	25	50	
ıx. Clock Frequency	f_{CL}		5	1.5	3	-	MHz
			10	4	8	-	
			15	6	11	-	
ıx. Clock Input Rise .me. ıx. Clock Input Fall .me.	t_{rCL} t_{fCL}		5	20	-	-	μs
			10	2.5	-	-	
			15	1.0	-	-	
.n. Set-up Time)0 ~D3, SR_{IN}, SL_{IN}- CLOCK)	t_{SU}		5	-	160	320	ns
			10	-	65	70	
			15	-	40	80	
.n. Set-up Time (S_0, S_1 - CLOCK)	t_{SU}		5	-	200	400	
			10	-	80	160	
			15	-	60	120	
n. Hold Time '0~D3, SR_{IN}, SL_{IN} - CLCOK)	t_H		5	-	-145	0	ns
			10	-	-55	0	
			15	-	-35	0	
n. Hold Time (S_0, S_1 - CLOCK)	t_H		5	-	-185	0	
			10	-	-70	0	
			15	-	-55	0	
put Capacitance	C_{IN}			-	5	7.5	pF

Only TC40104BP * Only TC40194BP

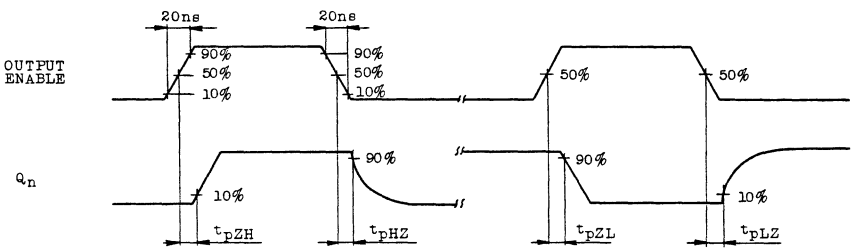
TC40104BP, TC40194BP

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

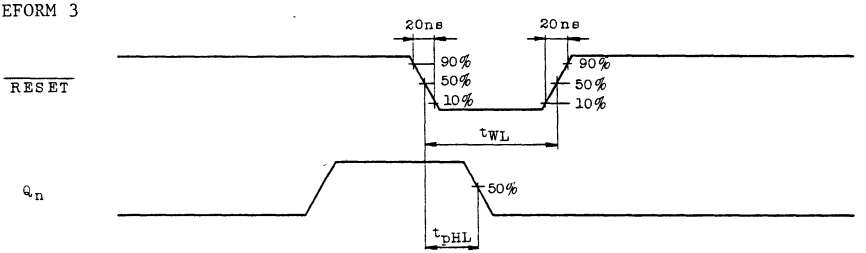
WAVEFORM 1



WAVEFORM 2



WAVEFORM 3

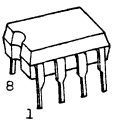


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40107BP

C40107BP DUAL 2-INPUT NAND BUFFER/DRIVER

C40107BP is a dual 2-input NAND gate, of which
utput is of open-drain structure by use of N-channel
OS FET. Being capable of driving a large current,
t can be directly connected to a relay, a lamp, a
ight-emitting diode (LED), etc. Wired OR can be
lso made.
I_{OL}=74mA(Typ.) at V_{DD}=10V and V_{OL}=0.5V)
he package is a compact DIP 8-pin unit, which is
asily mounted.
ince its output current is large, if the capacitor
f an output line exceeds 500pF, a resistor of 25Ω
r more should be used in series with the capacitor.

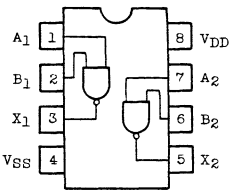


DIP 8(3D8A-P)

AXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
C Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
nput Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
utput Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
C Input Current	I_{IN}	±10	mA
ax. GND Current	I_{SS}	125	mA
ower Dissipation	P_D	300	mW
perating Temperature ange	T_A	-40 ~ 85	°C
torage Temperature ange	T_{stg}	-65 ~ 150	°C
ead Temp./Time	T_{sol}	260°C · 10 sec	

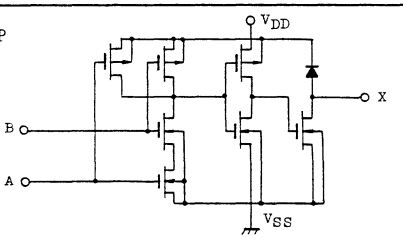
PIN ASSIGNMENT



(TOP VIEW)

IRCUIT DIAGRAM

L
2 TC40107BP



TRUTH TABLE

INPUT		OUTPUT
A	B	X
L	L	HZ
L	H	HZ
H	L	HZ
H	· H	L

HZ : High impedance

ECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
put Voltage	V_{IN}		0	-	V_{DD}	V
ad Capacitance	C_L		-	-	500	pF

TC40107BP

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IH}=V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	V
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output Low Current	I_{OL}	V_{OL}=0.4V	5	20	-	16	32	-	14	-	mA
		V_{OL}=1.0V	5	42	-	34	68	-	30	-	
		V_{OL}=0.5V	10	46	-	37	74	-	32	-	
		V_{OL}=1.0V	10	85	-	68	136	-	60	-	
		V_{OL}=0.5V	15	63	-	50	100	-	44	-	
		$V_{IH}=V_{DD}$									
Input High Voltage	V_{IH} *	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
Input Low Voltage	V_{IL} *	V_{OUT}=4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
3-State Output Leakage Current	I_{DH}	V_{OH}=18V	18	-	2	-	10^{-4}	2	-	20	
Quiescent Device Current	I_{DD} **	$V_{IN}=V_{DD},V_{SS}$ Outputs Open	5	-	1	-	0.001	1	-	7.5	
			10	-	2	-	0.001	2	-	15	
			15	-	4	-	0.002	4	-	30	

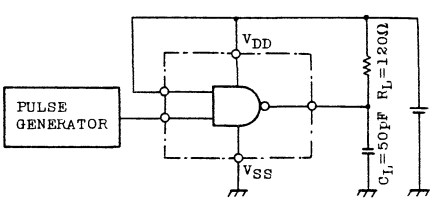
* Required external pull-up register R (=20kΩ)
** All valid input combinations.

IAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

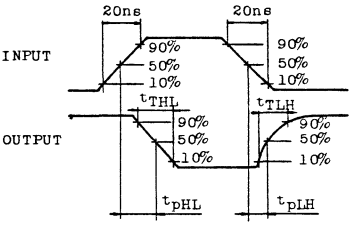
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
:put Transition Time (Low to High)	t_{TLH}	R_L=120Ω	5	-	35	100	ns
			10	-	25	70	
			15	-	20	50	
:put Transition Time (High to Low)	t_{THL}	R_L=120Ω	5	-	35	100	ns
			10	-	10	40	
			15	-	7	20	
›pagation Delay Time (Low to High)	t_{pLH}	R_L=120Ω	5	-	60	200	ns
			10	-	35	120	
			15	-	30	100	
›pagation Delay Time (High to Low)	t_{pHL}	R_L=120Ω	5	-	70	200	ns
			10	-	30	90	
			15	-	20	60	
›ut Capacitance	C_{IN}			-	5	7.5	pF
:put Capacitance	C_{OUT}			-	30	-	pF

:CUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

:IRCUIT



WAVEFORM

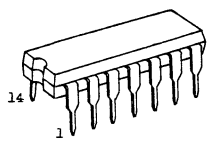


TC40117BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

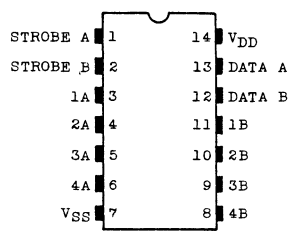
TC40117BP PROGRAMMABLE DUAL 4-BIT TERMINATOR

TC40117BP contains independent two 4-bit Pragrammable Terminators that are capable of terminating a data bus to a high or low state. They can also terminate any open or unused CMOS logic input to the last driven logic state when used with 3-state logic or during a power down condition. The terminator reduces power consumption by eliminating pull up or pull down resisters. When the STROBE input is held low, the terminated input/output latches the last DATA input until the terminated input/output changes state. When STROBE input is held high and DATA input is kept high or low, the terminated input/output stay in a high or low logic state respectively.
It also has a wide operating voltage range of 2 ~ 18 Volt that allows designers to use it in the battery driving system.



DIP 14 (3D14A-P)

PIN ASSIGNMENT

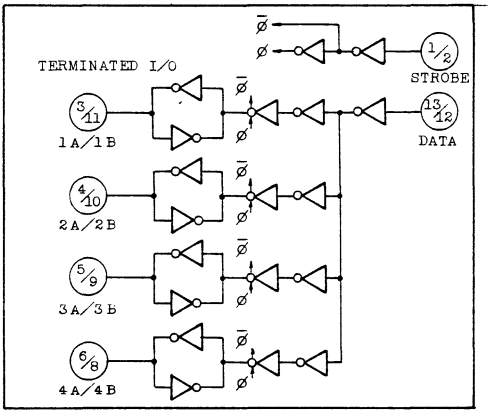


(TOP VIEW)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C . 10 sec	

LOGIC DIAGRAM



TRUTH TABLE

INPUTS		TERMINATED I/O			
STROBE	DATA	1A(B)	2A(B)	3A(B)	4A(B)
H	L	L*	L*	L*	L*
H	H	H**	H**	H**	H**
L	X	*	*	*	*

H=High Level
L=Low Level
X=Don't Care
*Terminator retains the last data state during strobo if its inputs are high impedance state.
If inputs are not in high impedance state. Then Terminator follows tne last driven state ("H" or "L" on its input/output)
. Equivalent to pull-down resistor
.. Equivalent to pull-up resistor

COMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2	-	18	V
put Voltage	V_{IN}		0	-	V_{DD}	V
erating Temperature	T_A		-40	-	85	°C

ATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
gh-Level tput Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
w-Level tput Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
tput High rrent	I_{OH}	V_{OH}=4.6V	5	-12	-	-12	-35	-	-9	-	μA
		V_{OH}=9.5V	10	-30	-	-30	-70	-	-25	-	
		V_{OH}=13.5V	15	-125	-	-125	-260	-	-102	-	
		$V_{IN}=V_{SS},V_{DD}$									
tput Low rrent	I_{OL}	V_{OL}=0.4V	5	12	-	12	35	-	9	-	
		V_{OL}=0.5V	10	30	-	30	85	-	25	-	
		V_{OL}=1.5V	15	125	-	125	320	-	102	-	
		$V_{IN}=V_{SS},V_{DD}$									
put High ltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
put Low ltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
put "H" Level rrent "L" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
iescent evice Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$	5	-	0.25	-	0.001	0.25	-	7.5	μA
		*	10	-	0.5	-	0.001	0.5	-	15	
			15	-	1.0	-	0.002	1.0	-	30	

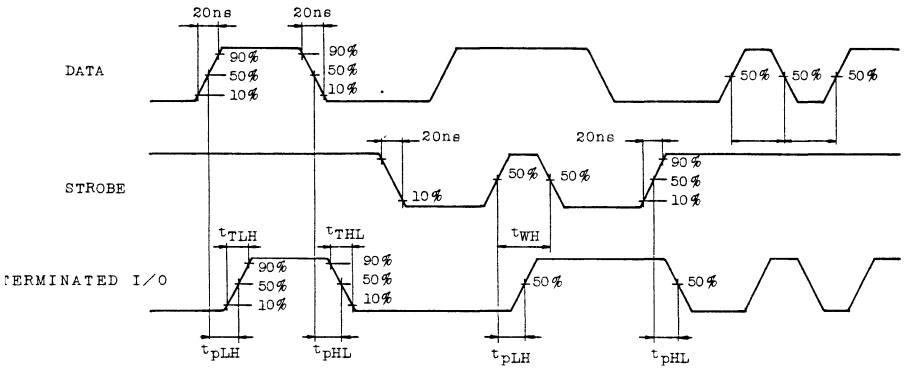
All valid input combinations

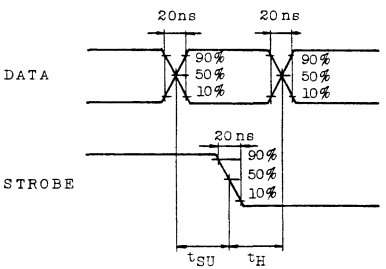
TC40117BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

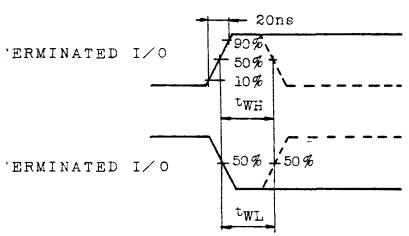
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	2.1	6.6	μs
			10	-	1.0	3.2	
			15	-	0.8	2.2	
Output Transition Time (High to Low)	t_{THL}		5	-	2.1	6.6	
			10	-	1.0	3.2	
			15	-	0.8	2.2	
Propagation Delay Time (STROBE, DATA-A,B)	t_{pLH}		5	-	0.9	3.0	μs
			10	-	0.45	1.25	
			15	-	0.35	1.0	
Propagation Delay Time (STROBE, DATA-A,B)	t_{pHL}		5	-	1.25	3.4	
			10	-	0.55	1.7	
			15	-	0.35	1.15	
Minimum Pulse Width (STROBE)	t_{WH}		5	-	0.9	3.0	μs
			10	-	0.35	1.2	
			15	-	0.25	0.95	
Minimum Pulse Width (DATA)	t_{WH} t_{WL}		5	-	3.6	7.2	
			10	-	1.8	3.6	
			15	-	1.35	2.7	
Minimum Pulse Width (TERMINATED I/O)	t_{WH} t_{WL}		5	-	30	-	ns
			10	-	45	-	
			15	-	55	-	
Minimum Set-Up Time (DATA-STROBE)	t_{SU}		5	-	930	1860	ns
			10	-	380	760	
			15	-	230	460	
Minimum Hold Time (DATA-STROBE)	t_H		5	-	-6	-	ns
			10	-	-4	-	
			15	-	-3	-	
Input Capacitance	C_{IN}			-	5	7.5	pF

/EFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS





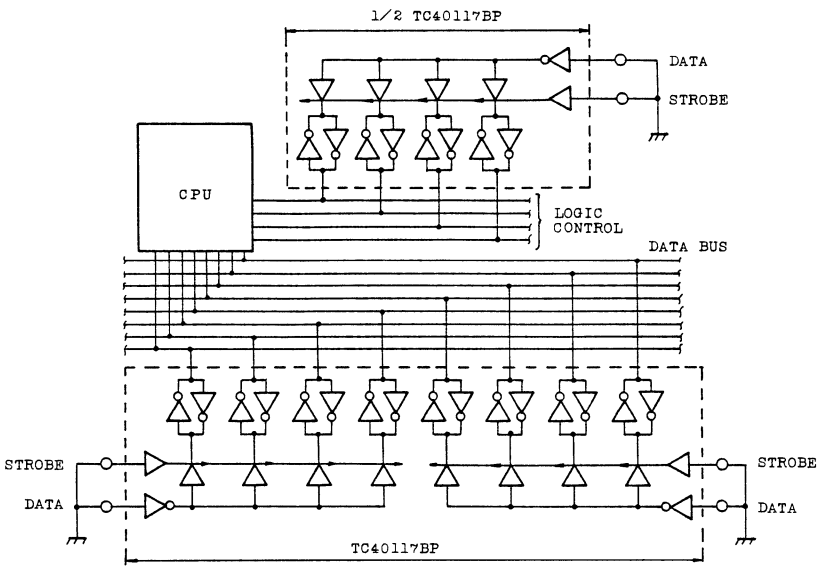
(STROBE = "L")



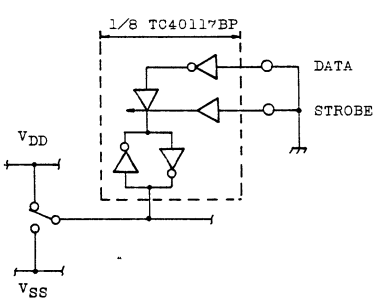
TC40117BP

TYPICAL APPLICATIONS

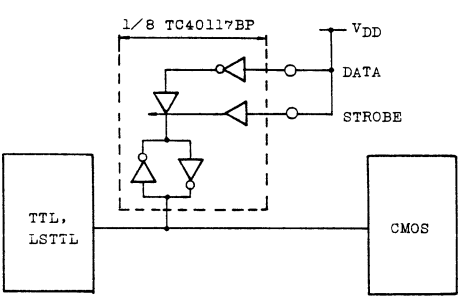
(1) APPLICATION FOR TERMINATING AN 8-BIT DATA BUS LINE OF CPU



(2) APPLICATION FOR ANTI-BOUNCE CIRCUIT



(3) APPLICATION FOR INTERFACE CIRCUIT BETWEEN TTL OUTPUT AND CMOS INPUT



C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40160BP, TC40161BP
TC40162BP, TC40163BP

YNCHRONOUS PROGRAMMABLE 4-BIT COUNTER

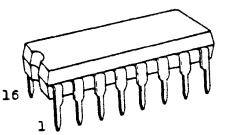
TC40160BP DECADE WITH ASYNCHRONOUS CLEAR

TC40161BP BINARY WITH ASYNCHRONOUS CLEAR

TC40162BP DECADE WITH SYNCHRONOUS CLEAR

TC40163BP BINARY WITH SYNCHRONOUS CLEAR

The TC40160BP, TC40161BP, TC40162BP, and TC40163BP are synchronously programmable 4-bit counters. The TC40160BP and TC40161BP are decimal counter and 4-bit binary counter respectively having asynchronous clear function which directly clears all the flip-flop outputs. The TC40162BP and TC40163BP are decimal counter and 4-bit binary counter respectively which are synchronous at the rising edges of clocks. CLEAR and LOAD of these counters are active at the "L" level. Further, these counters are functionally compatible with the 74160, 74161, 74162, and 74163 of TTL.

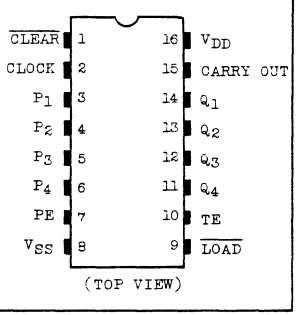


DIP 16(3D16A-P)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



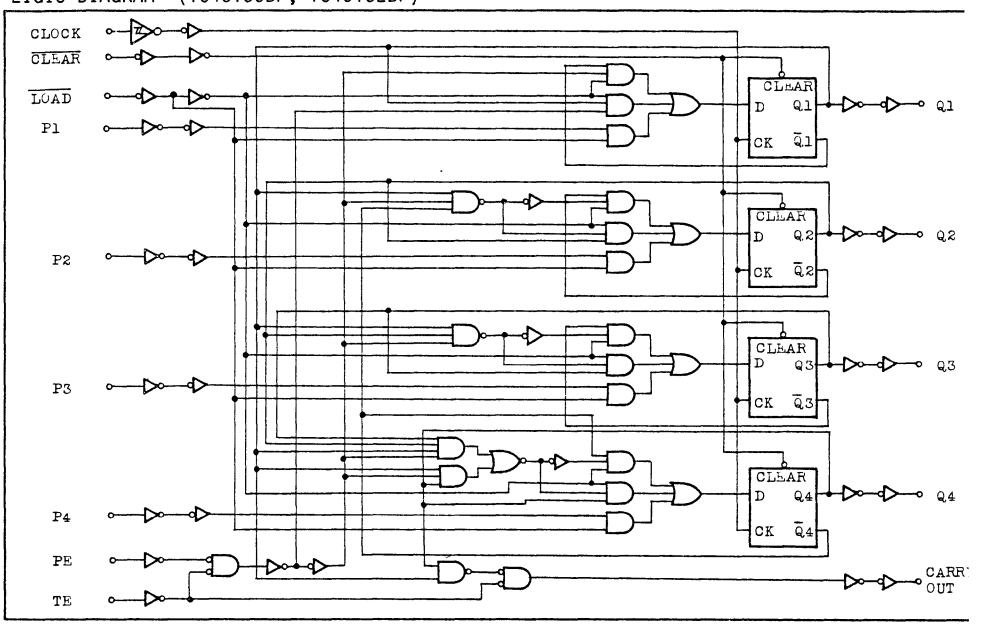
TRUTH TABLE

INPUT									OUTPUT			
CLOCK	CLEAR	LOAD	PE	TE	P_1	P_2	P_3	P_4	Q_1	Q_2	Q_3	Q_4
☆	L	*	*	*	*	*	*	*	L	L	L	L
△ ∫	H	L	*	*	D_1	D_2	D_3	D_4	D_1	D_2	D_3	D_4
△ ∫	H	H	L	L	*	*	*	*	·	·	·	·
△ ∫	H	H	L	H	*	*	*	*	·	·	·	·
△ ∫	H	H	H	L	*	*	*	*	·	·	·	·
△ ∫	H	H	H	H	*	*	*	*	COUNT			
△ ⌉	H	*	*	*	*	*	*	*	·	·	·	·

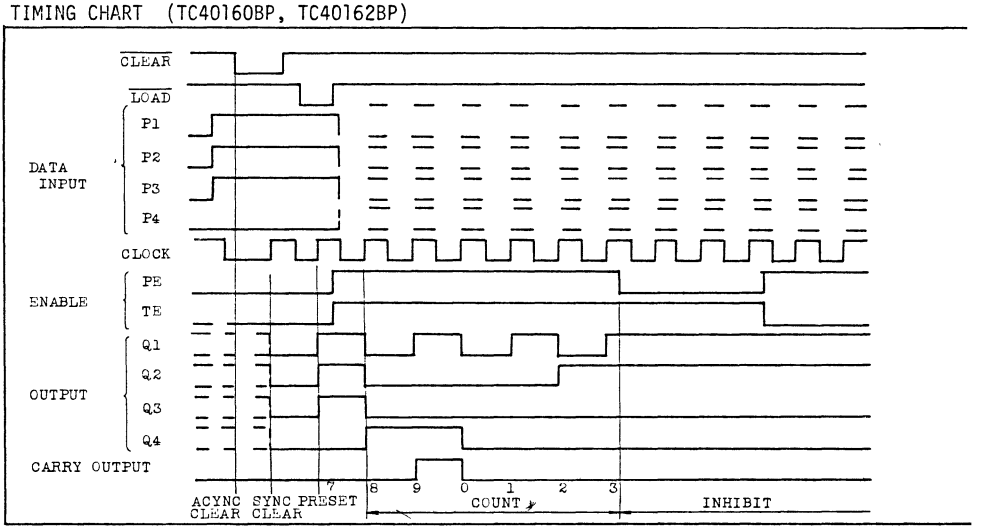
* : Don't care
△ : Level change
· : No change
D : Data "H" or "L"
☆ : { Don't care (TC40160, TC40161) / Rise edge (TC40162, TC40163) }

TC40160BP, TC40161BP, TC40162BP, TC40163BP

LIGIC DIAGRAM (TC40160BP, TC40162BP)

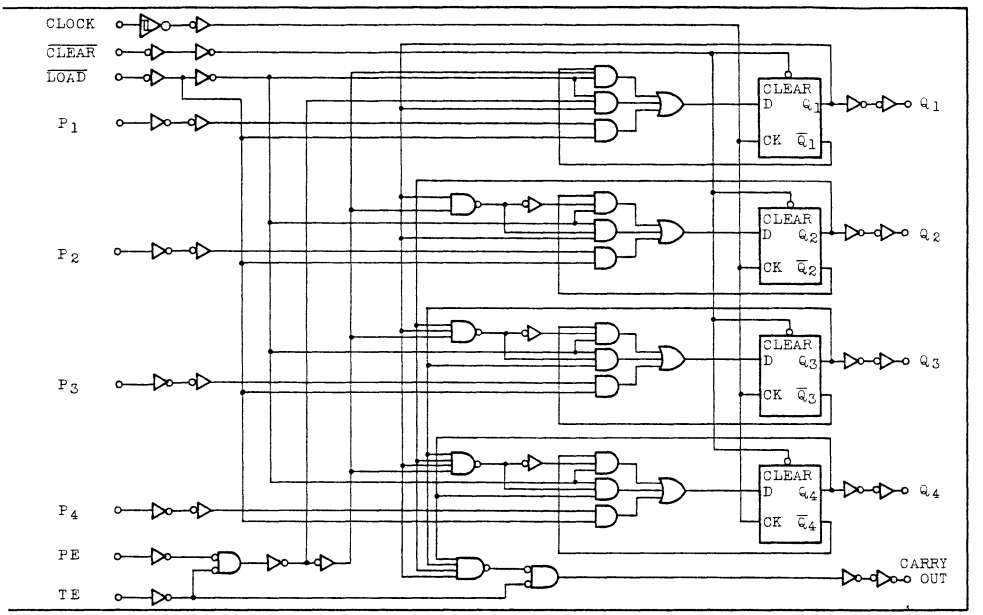


TIMING CHART (TC40160BP, TC40162BP)

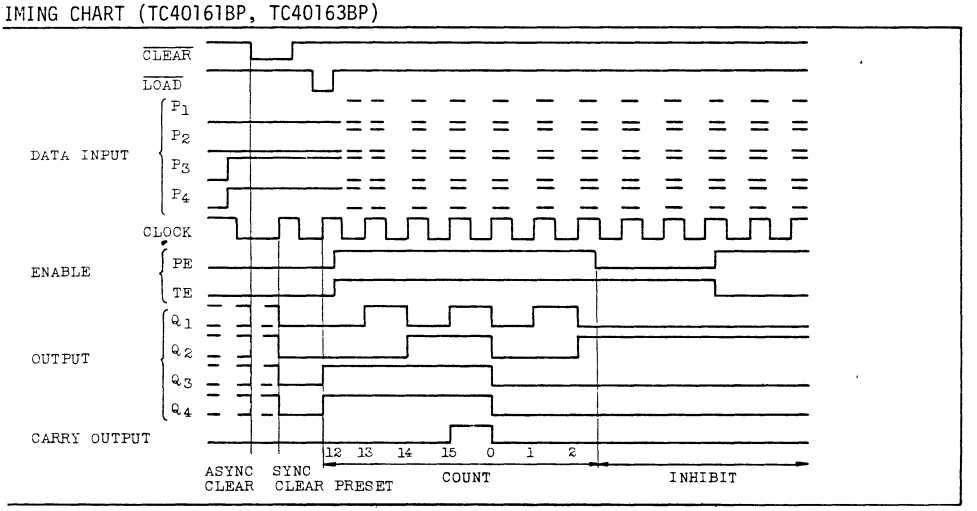


TC40160BP, TC40161BP, TC40162BP, TC40163BP

LOGIC DIAGRAM (TC40161BP, TC40163BP)



TIMING CHART (TC40161BP, TC40163BP)



TC40160BP, TC40161BP, TC40162BP, TC40163BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

TC40160BP, TC40161BP, TC40162BP, TC40163BP

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All Valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		5	-	250	500	
			10	-	100	200	
			15	-	70	140	
Propagation Delay Time (CLOCK-CARRY OUT)	t_{pLH} t_{pHL}		5	-	300	600	
			10	-	120	240	
			15	-	80	160	
Propagation Delay Time (TE-CARRY OUT)	t_{pLH} t_{pHL}		5	-	170	340	
			10	-	65	130	
			15	-	45	90	
Propagation Delay Time ($\overline{CLEAR}$ - Q) 40160, 40161 Only	t_{pHL}		5	-	180	500	
			10	-	75	220	
			15	-	55	160	
Min. Clock Pulse Width	t_w		5	-	130	260	ns
			10	-	45	90	
			15	-	30	60	
Min. Pulse Width ($\overline{CLEAR}$) 40160, 40161 Only	t_{WL}		5	-	140	280	
			10	-	55	110	
			15	-	35	70	

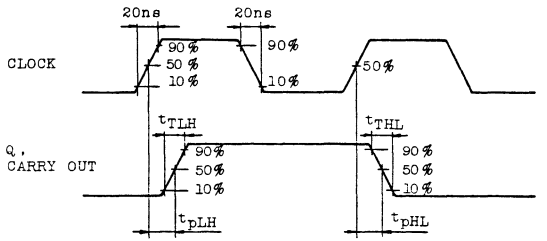
TC40160BP, TC40161BP, TC40162BP, TC40163BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

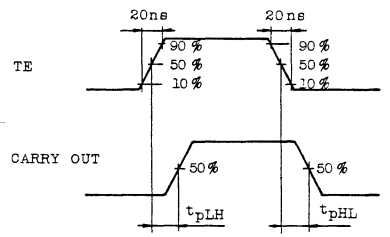
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Max. Clock Frequency	f_{CL}		5	2	4	-	MHz
			10	5.5	11	-	
			15	8	16	-	
Max. Clock Input Rise Time. Max. Clock Input Fall Time.	t_{rCL} t_{fCL}		5	No Limit			μs
			10				
			15				
Min. Set-up Time (P_n - CLOCK)	t_{SU}		5	-	55	240	ns
			10	-	20	90	
			15	-	15	60	
Min. Set-up Time ($\overline{LOAD}$ - CLOCK)	t_{SU}		5	-	75	240	
			10	-	30	90	
			15	-	20	60	
Min. Set-up Time (PE, TE - CLOCK)	t_{SU}		5	-	190	380	
			10	-	70	140	
			15	-	50	100	
Min. Set-up Time ($\overline{CLEAR}$ - CLOCK) 40162, 40163 Only	t_{SU}		5	-	50	310	
			10	-	20	110	
			15	-	15	70	
Min. Hold Time (P_n, $\overline{LOAD}$, PE, TE- CLOCK)	t_H		5	-	-	0	ns
			10	-	-	0	
			15	-	-	5	
Min. Hold Time ($\overline{CLEAR}$ - CLOCK) 40162, 40163 Only	t_H		5	-	-30	0	
			10	-	-10	0	
			15	-	-5	0	
Min. Removal Time ($\overline{CLEAR}$ - COLCK) 40160, 40161 Only	t_{rem}		5	-	80	200	ns
			10	-	25	100	
			15	-	15	70	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

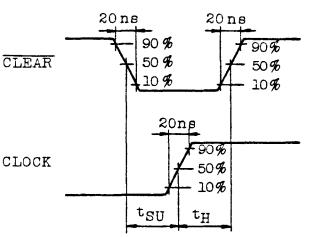
WAVEFORM 1



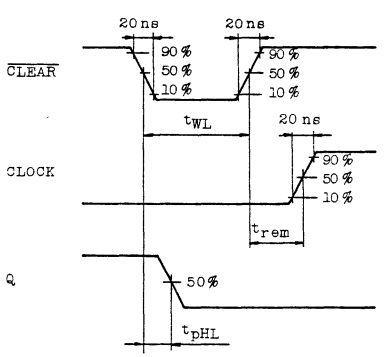
WAVEFORM 2



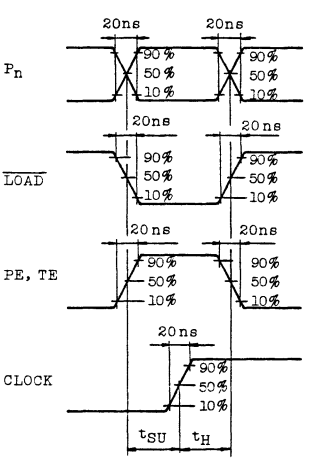
WAVEFORM 3 (40162, 40163)



WAVEFORM 4 (40160, 40161)



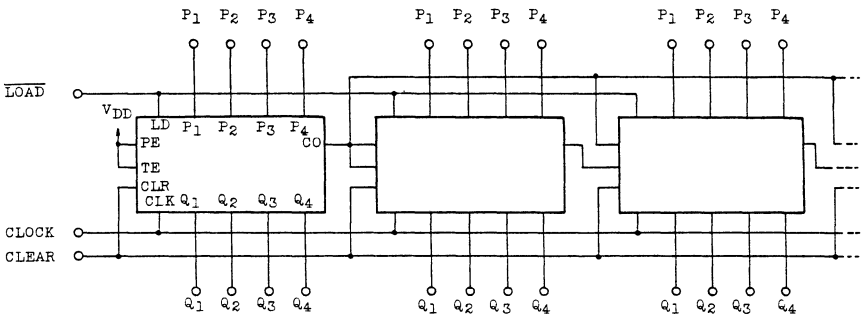
WAVEFORM 5



TC40160BP, TC40161BP, TC40162BP, TC40163BP

APPLICATION CIRCUIT

1. Cascaded counter packages in the parallel-clocked mode.

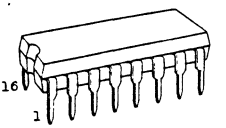


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

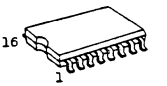
TC40174BP/BF

TC40174BP/TC40174BF HEX D-TYPE FLIP-FLOP

TC40174BP/TC40174BF contains six circuits of D type flip-flops having common clock terminal and clear terminal. The logical input applied to Dn input is transferred to Qn output by the rising edge of CLOCK input.
$\overline{\text{CLEAR}}$ input is active with "L" level. This has the same functions as TTL 54174/74174 and the pin assignment is also same.



DIP 16 (3D16A-P)

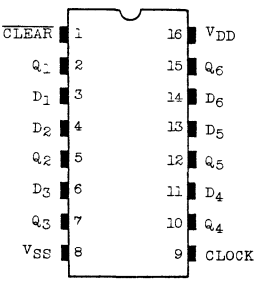


MFP 16 (F16GC-P)

MAXIMUM RATINGS

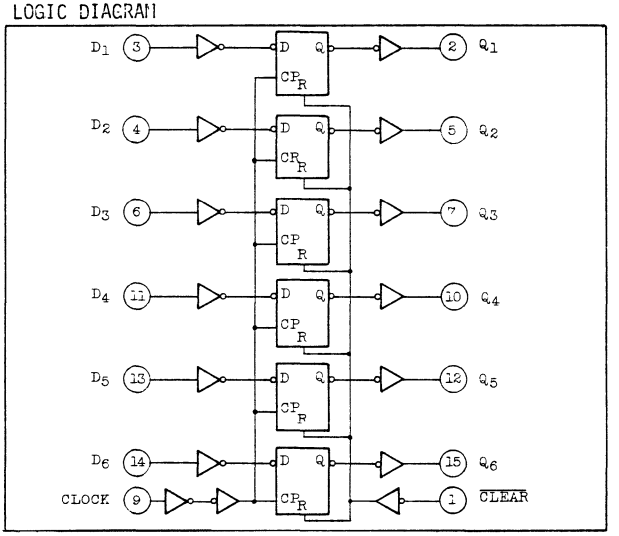
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	Tsol	260°C · 10sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUT
CLOCK△	Dn	$\overline{\text{CLEAR}}$	Qn+1
↑	H	H	H
↑	L	H	L
↓	*	H	Qn·
*	*	L	L

△ : Level change
· : No change
* : Don't care

TC40174BP/BF

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	1	-	0.005	1	-	30	μA
			10	-	2	-	0.010	2	-	60	
			15	-	4	-	0.015	4	-	120	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

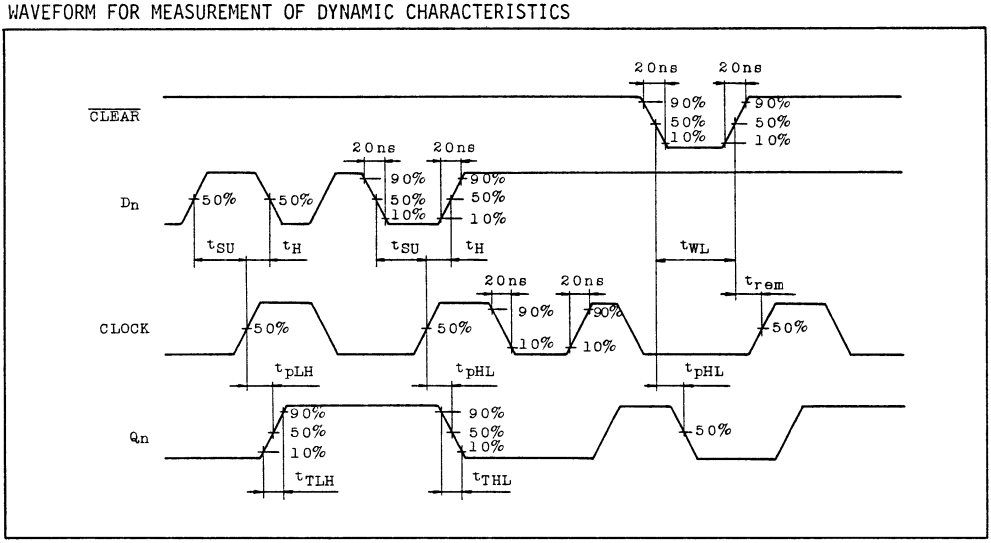
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		5	-	150	300	ns
			10	-	65	140	
			15	-	45	100	
Propagation Delay Time ($\overline{CLEAR}$ - Q)	t_{pHL}		5	-	170	340	
			10	-	70	140	
			15	-	50	100	
Min. Clock Pulse Width	t_w		5	-	55	130	ns
			10	-	20	60	
			15	-	15	40	
Min. Pulse Width ($\overline{CLEAR}$)	t_{WL}		5	-	45	100	
			10	-	20	50	
			15	-	10	40	
Max. Clock Frequency	f_{CL}		5	3.5	9	-	MHz
			10	6	25	-	
			15	8	34	-	
Max. Clock Input Rise Time. Max. Clock Input Fall Time.	t_{rCL} t_{fCL}		5	20	-	-	μs
			10	15	-	-	
			15	15	-	-	

TC40174BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Min. Set-up Time (DATA - CLOCK)	t_{SU}		5	-	25	50	ns
			10	-	12	25	
			15	-	7	15	
Min. Hold Time (DATA - CLOCK)	t_H		5	-	-8	80	ns
			10	-	0	40	
			15	-	3	30	
Min. Removal Time ($\overline{\text{CLEAR}}$ - CLOCK)	t_{rem}		5	-	7	40	ns
			10	-	4	20	
			15	-	3	15	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

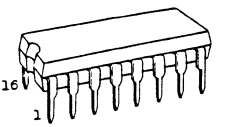


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

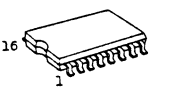
TC40175BP/BF

TC40175BP/TC40175BF QUAD D-TYPE FLIP-FLOP

TC40175BP/TC40175BF contains four circuits of D type flip-flop having common clock terminal and clear terminal. The logical input applied to D_n input is transferred to Q_n output by the rising edge of CLOCK input.
$\overline{CLEAR}$ input is active with "L" level. This has the same functions as TTL 54175/74175 and the pin assignment is also same.



DIP 16(3D16A-P)

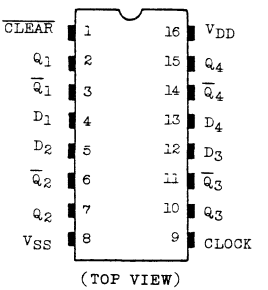


MFP 16(F16GC-P)

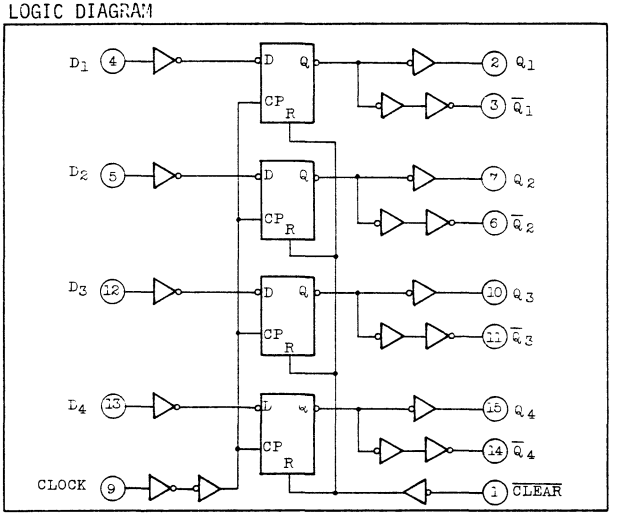
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS	
CLOCK	D_n	$\overline{CLEAR}$	Q_{n+1}	$\overline{Q_{n+1}}$
⏌	H	H	H	L
⏌	L	H	L	H
⏋	*	H	Q_n ·	$\overline{Q_n}$ ·
*	*	L	L	H

⏌ : Level change
· : No change
* : Don't care

TC40175BP/BF

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	1	-	0.005	1	-	30	μA
			10	-	2	-	0.010	2	-	60	
			15	-	4	-	0.015	4	-	120	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

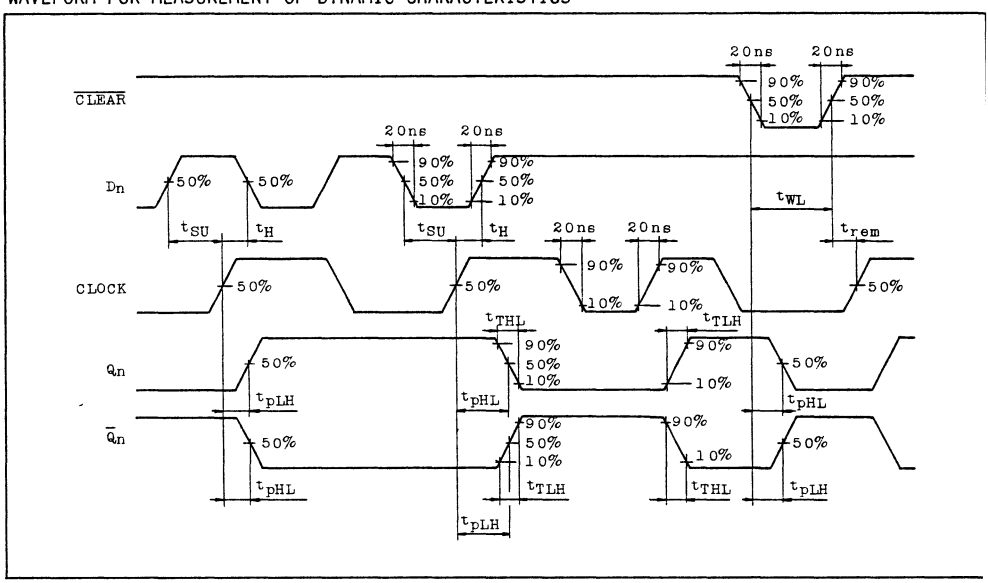
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5	-	170	340	ns
			10	-	70	140	
			15	-	50	100	
Propagation Delay Time ($\overline{CLEAR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5	-	190	380	
			10	-	80	160	
			15	-	55	110	
Min. Clock Pulse Width	t_w		5	-	55	130	ns
			10	-	20	60	
			15	-	15	40	
Min. Pulse Width ($\overline{CLEAR}$)	t_{WL}		5	-	40	100	
			10	-	20	50	
			15	-	15	40	
Max. Clock Frequency	f_{CL}		5	3.5	9	-	MHz
			10	6	25	-	
			15	8	34	-	
Max. Clock Input Rise Time. Max. Clock Input Fall Time.	t_{rCL} t_{fCL}		5	20	-	-	μs
			10	15	-	-	
			15	15	-	-	

TC40175BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Min. Set-up Time (DATA - CLOCK)	t_{SU}		5	-	30	60	ns
			10	-	15	30	
			15	-	10	20	
Min. Hold Time (DATA - CLOCK)	t_H		5	-	-5	80	ns
			10	-	0	40	
			15	-	3	30	
Min. Removal Time ($\overline{CLEAR}$ - CLOCK)	t_{rem}		5	-	7	40	ns
			10	-	4	20	
			15	-	3	15	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



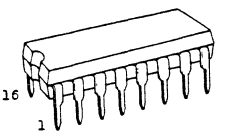
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40192BP
TC40193BP

TC40192BP PRESETTABLE BCD UP/DOWN COUNTER (Dual Clock with Reset)

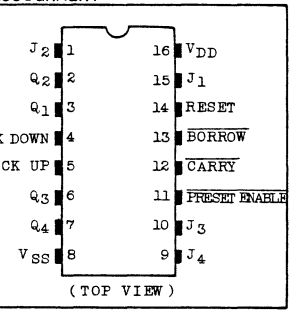
TC40193BP PRESETTABLE BINARY UP/DOWN COUNTER (Dual Clock with Reset)

TC40192BP/TC40193BP is a synchronous 4-bit up/down counter.
The RESET input is active at "H" level, and the $\overline{\text{PRESET ENABLE}}$ input is active at "L" level; both of them perform asynchronous operation.
In the clock, the up-count input and the down-count input are independent each other, and each input performs count operation at the rising edge of the pulse. And the clock in the counter takes the logic sum of counting up and counting down; therefore, one clock input can be used as a clock inhibit input.
The functions and pin assignment of TC40192BP and TC40193BP are compatible with those of 74192 and 74193 of TTL.



DIP 16(3D16A-P)

PIN ASSIGNMENT



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

TRUTH TABLE

(TC40192BP, TC40193BP)

CLOCK UP	CLOCK DOWN	$\overline{\text{PRESET ENABLE}}$	RESET	ACTION
⎍	H	H	L	COUNT UP
⎏	H	H	L	NO COUNT
H	⎍	H	L	COUNT DOWN
H	⎏	H	L	NO COUNT
*	*	L	L	PRESET
*	*	*	H	RESET

* . Don't care

(TC40192BP)

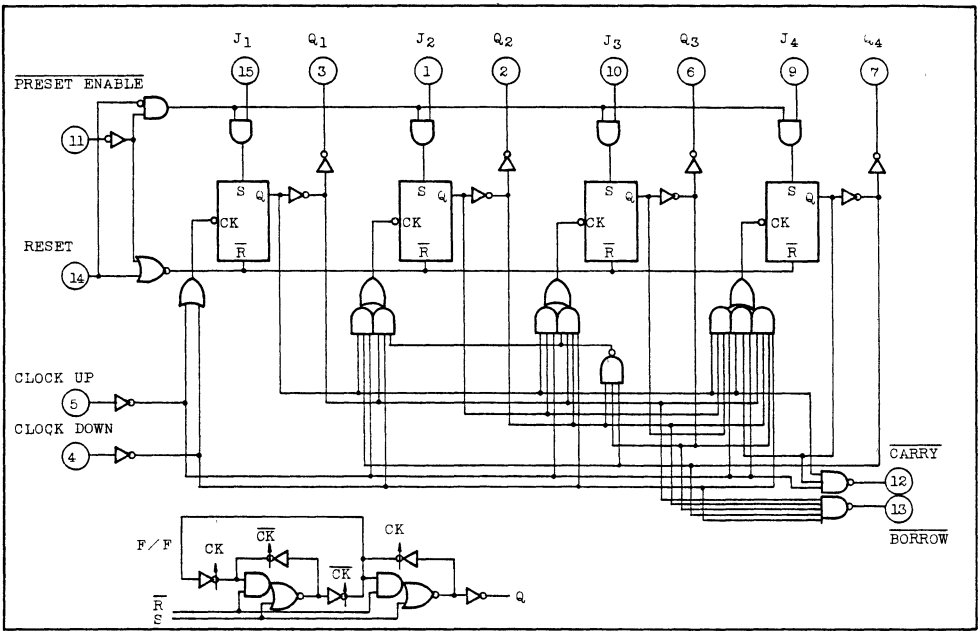
COUNT	Q_1	Q_2	Q_3	Q_4
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

(TC40193BP)

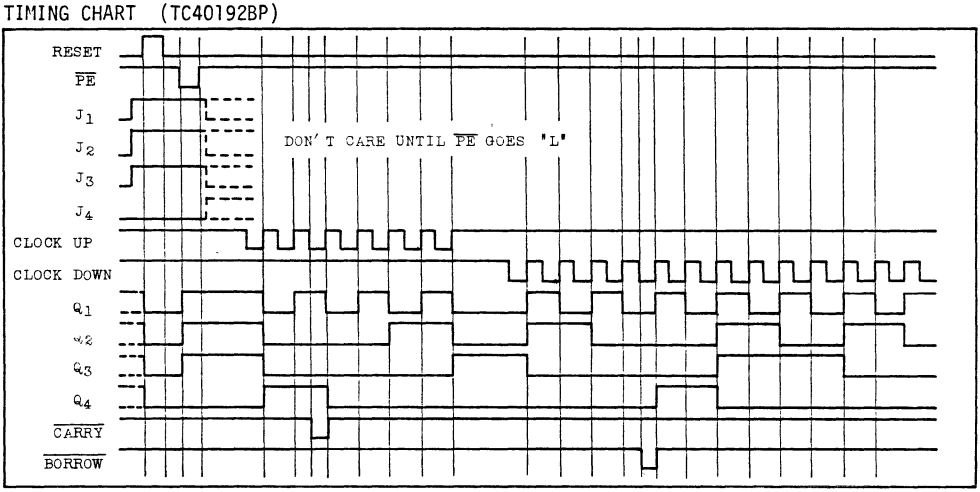
COUNT	Q_1	Q_2	Q_3	Q_4
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
A	L	H	L	H
B	H	H	L	H
C	L	L	H	H
D	H	L	H	H
E	L	H	H	H
F	H	H	H	H

TC40192BP, TC40193BP

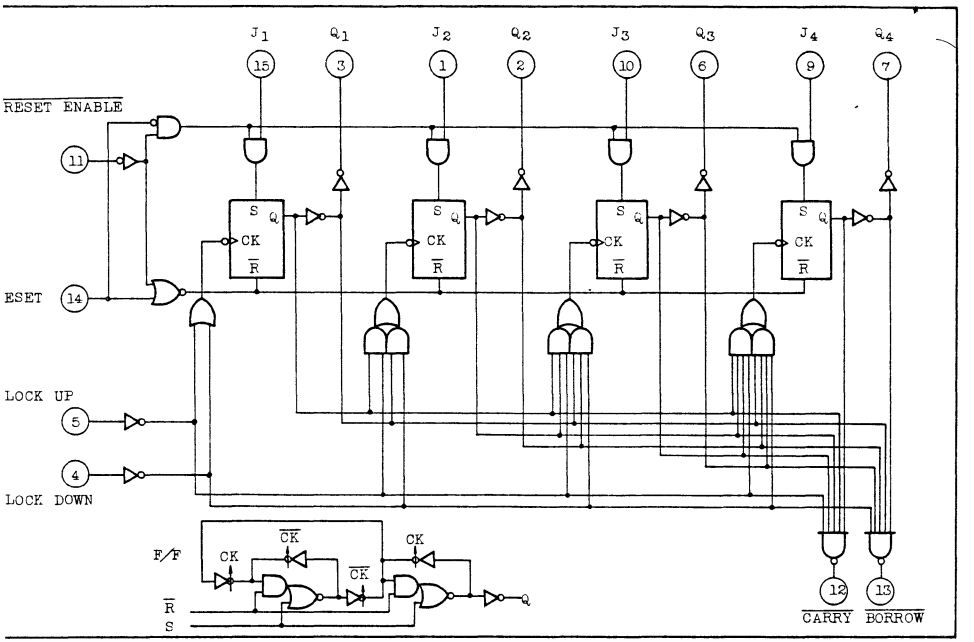
LOGIC DIAGRAM (TC40192BP)



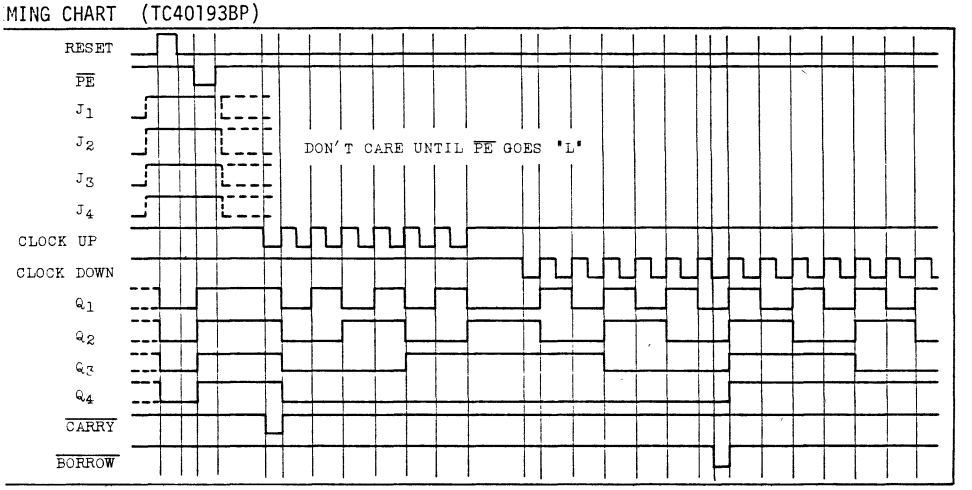
TIMING CHART (TC40192BP)



ǀGIC DIAGRAM (TC40193BP)



MING CHART (TC40193BP)



TC40192BP, TC40193BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	-0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	0.1	-	-10^{-5}	-0.1	-	-1.0	

ATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

HARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
iescent Device rrent	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

All valid input combinations.

NAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
tput Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
tput Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
opagation Delay Time CLOCK UP, CLOCK DOWN - Q)	t_{pLH} t_{pHL}		5	-	450	900	
			10	-	180	360	
			15	-	130	260	
opagation Delay Time (RESET - Q)	t_{pHL}		5	-	400	800	
			10	-	160	320	
			15	-	120	240	
opagation Delay Time ($\overline{PE}$ - Q)	t_{pLH} t_{pHL}		5	-	420	840	
			10	-	170	340	
			15	-	120	240	
opagation Delay Time LCOK UP - $\overline{CARRY}$, LOCK DOWN - $\overline{BORROW}$)	t_{pLH} t_{pHL}		5	-	220	440	
			10	-	95	190	
			15	-	70	140	
opagation Delay Time RESET, $\overline{PE}$ - BORROW, CARRY)	t_{pLH} t_{pHL}		5	-	490	980	
			10	-	190	380	
			15	-	130	260	
n. Clock Pulse Width	t_w		5	-	250	500	ns
			10	-	100	200	
			15	-	70	140	

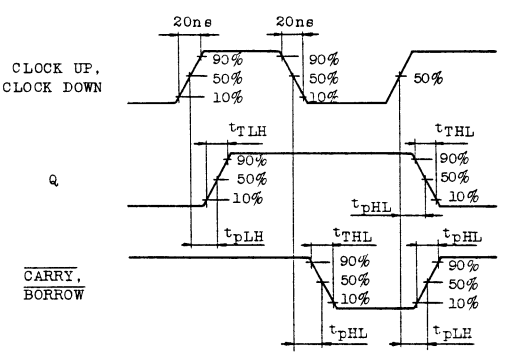
TC40192BP, TC40193BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Min. Pulse Width (RESET)	t_{WH}	5	-	100	480	ns
		10	-	40	300	
		15	-	35	260	
Min. Pulse Width ($\overline{PE}$)	t_{WL}	5	-	80	240	
		10	-	30	170	
		15	-	25	140	
Max. Clcok Frequency	f_{CL}	5	1	2	-	MHz
		10	2.5	5	-	
		15	3.5	7	-	
Max. Clock Input Rise Time. Max. Clock Input Fall Time.	f_{rCL} f_{fCL}	5	20	-	-	μs
		10	2.5	-	-	
		15	1	-	-	
Min. Removal Time (RESET, $\overline{PE}$ - CLOCK)	t_{rem}	5	-	-40	80	ns
		10	-	-16	40	
		15	-	-14	30	
Input Capacitance	C_{IN}		-	5	7.5	pF

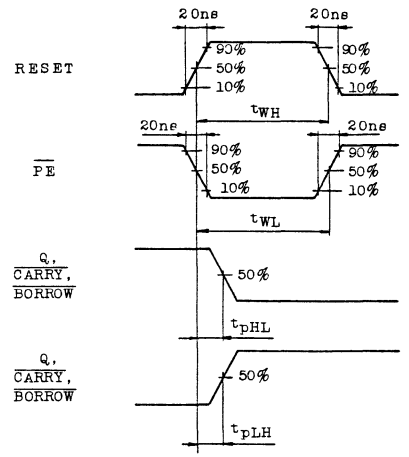
WAVEFROM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1

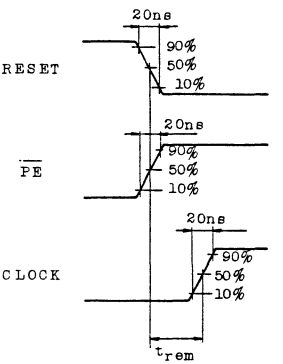


\VEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 2



WAVEFORM 3



TC4501BP

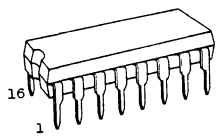
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4501BP TRIPLE GATE (Dual 4-Input NAND Gate and 2-Input NOR/OR Gate or 8-Input AND/NAND Gate)

The TC4501BP is a combined gate which contains dual 4-input NAND gate and 2-input NOR/OR gate in one package.

Since all the outputs of these gates are provided with the buffers of inverters, the input/output transmission characteristics have been improved and the noise immunity has been elevated. Further, an increase in propagation delay time caused by an increase in load capacity is kept to a minimum.

The TC4501BP can be used as 8-input positive AND/NAND gate by externally connecting the output of NAND gate to the input of NOR/OR gate.

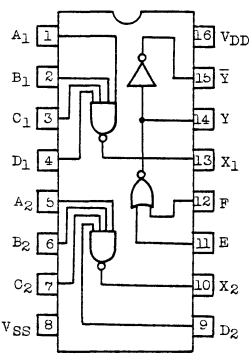


DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

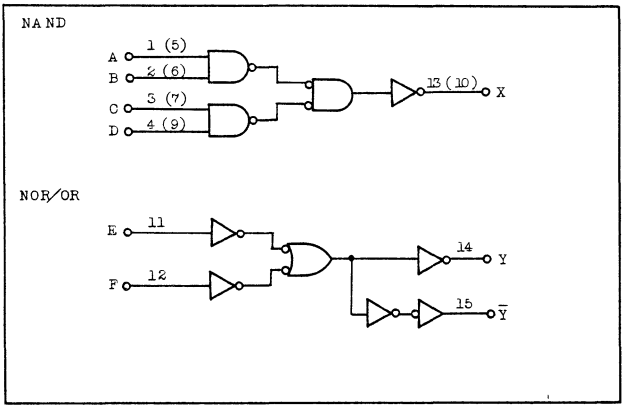
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ∼ 85	°C
Storage Temperature Range	T_{stg}	-65 ∼ 150	°C
Lead Temp./Time	T_{sol}	260°C • 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



ECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS}$, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95		
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS}$, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
nput Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
urrent "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}	5	-	0.25	-	0.001	0.25	-	7.5	μA
			10	-	0.5	-	0.001	0.5	-	15	
		*	15	-	1.0	-	0.002	1.0	-	30	

All valid input combinations.

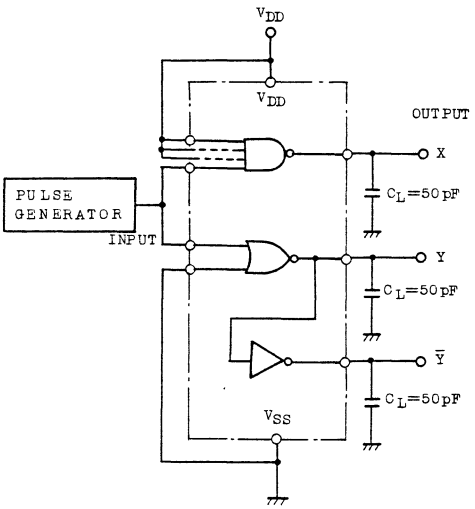
TC4501BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

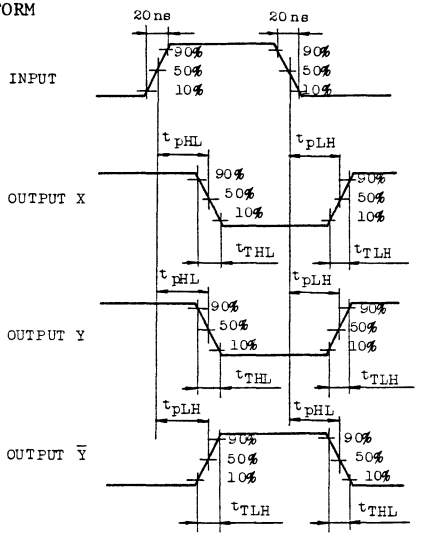
	CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
	Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
				10	-	50	100	
				15	-	40	80	
	Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
				10	-	50	100	
				15	-	40	80	
NAND	Propagation Delay Time (Low to High)	t_{pLH}		5	-	80	260	
				10	-	50	140	
				15	-	40	100	
NAND	Propagation Delay Time (High to Low)	t_{pHL}		5	-	80	260	
				10	-	50	140	
				15	-	40	100	
NOR	Propagation Delay Time (Low to High)	t_{pLH}		5	-	100	230	
				10	-	50	130	
				15	-	40	90	
NOR	Propagation Delay Time (High to Low)	t_{pHL}		5	-	100	230	
				10	-	50	130	
				15	-	40	90	
NOR-Inverter	Propagation Delay Time (Low to High)	t_{pLH}		5	-	130	260	
				10	-	70	140	
				15	-	50	100	
NOR-Inverter	Propagation Delay Time (High to Low)	t_{pHL}		5	-	130	260	
				10	-	70	140	
				15	-	50	100	
	Input Capacitance	C_{IN}			-	5	7.5	pF

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

CIRCUIT



WAVEFORM

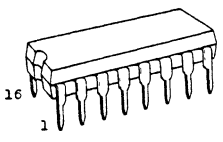


TC4502BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4502BP STROBED HEX INVERTER/BUFFER

The TC4502BP is a strobed hex inverter/buffer with 3-state output. When DISABLE input is set to "H" level, six outputs become high impedance independently of the other inputs/when DISABLE input is set to "L" level and INHIBIT input "H" level, all the outputs go to "L" level.
Further, since each output is capable of directly driving one standard TTL, the TC4502BP is suited for a bus interface, a data transmission circuit, a multiplexer, etc.

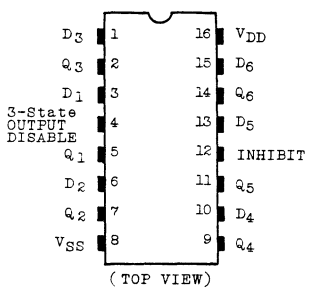


DIP 16(3D16A-P)

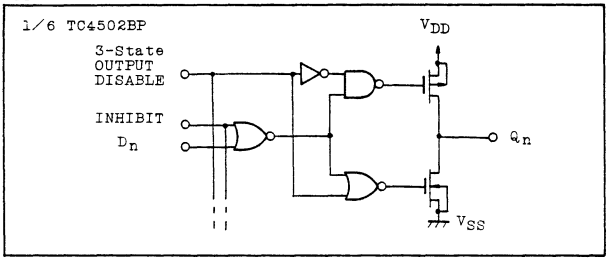
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

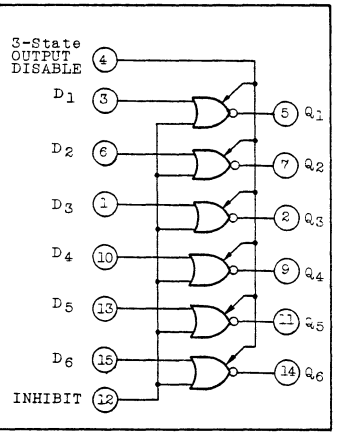
PIN ASSIGNMENT



CIRCUIT DIAGRAM



LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUT	
DISABLE	INHIBIT	D_n	Q_n	
H	*	*	HZ	HZ: High impedance
L	H	*	L	* : Don't care
L	L	L	H	
L	L	H	L	

ECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
C Supply Voltage	V_{DD}		3	-	18	V
nput Voltage	V_{IN}		0	-	V_{DD}	V

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
igh-Level utput Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
ow-Level utput Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
utput High urrent	I_{OH}	V_{OH}=4.6V	5	-0.73	-	-0.65	-1.4	-	-0.58	-	mA
		V_{OH}=2.5V	5	-2.4	-	-2.1	-1.3	-	-1.9	-	
		V_{OH}=9.5V	10	-1.8	-	-1.65	-3.2	-	-1.35	-	
		V_{OH}=13.5V	15	-4.8	-	-4.3	-1.1	-	-3.5	-	
		$V_{IN}=V_{SS},V_{DD}$									
utput Low urrent	I_{OL}	V_{OL}=0.4V	5	3.8	-	3.2	7.3	-	2.9	-	
		V_{OL}=0.5V	10	9.6	-	8.0	1.7	-	6.6	-	
		V_{OL}=1.5V	15	25.0	-	24.0	5.7	-	20.0	-	
		$V_{IN}=V_{SS},V_{DD}$									
nput High oltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
nput Low oltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
nput urrent "H" Level	I_{IH}	V_{IH}=0V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
nput urrent "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	μA

TC4502BP

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Leakage Current	"H" Level	I_{DH}	V_{OUT}=18V	18	-	0.4	-	10^{-4}	0.4	-	12	μA
	"L" Level	I_{DL}	V_{OUT}=0V	18	-	-0.4	-	-10^{-4}	-0.4	-	-12	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	1	-	0.002	1	-	30	μA
				10	-	2	-	0.004	2	-	60	
				15	-	4	-	0.008	4	-	120	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

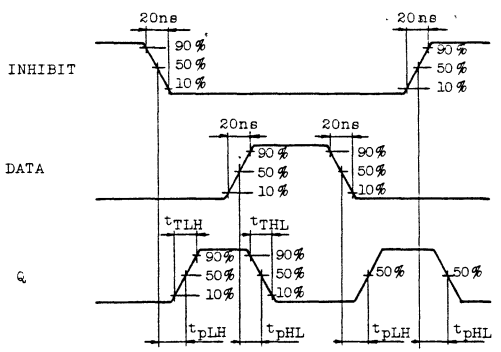
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	40	100	
			15	-	30	80	
Output Transition Time (High to Low)	t_{THL}		5	-	35	80	
			10	-	15	40	
			15	-	10	30	
Propagation Delay Time (DATA, INHIBIT - Q)	t_{pLH}		5	-	200	400	
			10	-	80	180	
			15	-	60	130	
Propagation Delay Time (DATA, INHIBIT - Q)	t_{pHL}		5	-	135	270	
			10	-	55	110	
			15	-	40	80	
Three State Disable Time (DISABLE - Q)	t_{pHZ}	R_L=1kΩ	5	-	65	130	ns
			10	-	30	60	
			15	-	25	50	
Three State Disable Time (DISABLE - Q)	t_{pZH}	R_L=1kΩ	5	-	80	220	
			10	-	30	100	
			15	-	20	80	
Three State Disable Time (DISABLE - Q)	t_{pLZ}	R_L=1kΩ	5	-	100	250	
			10	-	50	130	
			15	-	40	110	

/NAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

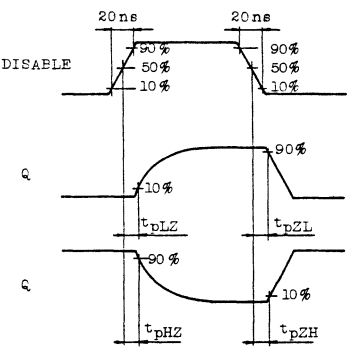
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
ıree State Disable ime (DISABLE - Q)	t_{pZL}	R_L=1kΩ	5	-	80	250	ns
			10	-	30	110	
			15	-	20	80	
ıput Capacitance	C_{IN}			-	5	7.5	pF

AVEFROM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1



WAVEFORM 2

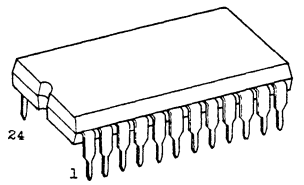


TC4508BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4508BP DUAL 4-BIT LATCH

TC4508BP contains two independent circuits of latches having output disable function and clear function.
When STROBE input is "H", the data input appears at the output as it is and if STROBE input is changed from "H" to "L", the output retains the data input existed at the time of falling edge of STROBE.
When STROBE is "L", the outputs are not affected by DATA inputs.
If RESET input is set to "H", Q outputs are cleared to "L" level regardless of STROBE. If DISABLE input is set to "H", Q outputs have high impedance regardless of other inputs.

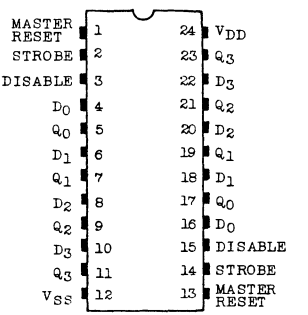


DIP24(6D24A-P)

ABSOLUTE MAXIMUM RATINGS

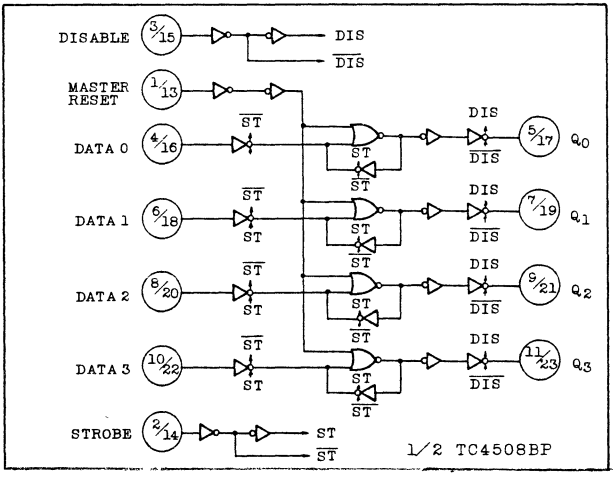
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-60 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



1/2 TC4508BP

TRUTH TABLE

RESET	STROBE	DISABLE	DATA INPUTS				OUTPUTS			
			D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3
*	*	H	*	*	*	*	HZ			
H	*	L	*	*	*	*	L	L	L	L
L	L	L	*	*	*	*	LATCHED			
L	H	L	A	B	C	D	A	B	C	D

* : Don't Care

HZ : High Impedance

ECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
C Supply Voltage	V_{DD}		3	-	18	V
nput Voltage	V_{IN}		0	-	V_{DD}	V

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
igh-Level utput Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
ow-Level utput Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
utput High urrent		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
utput Low urrent		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

TC4508BP

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Leakage Current	"H" Level	I_{DH}	V_{OUT}=18V	18	-	0.4	-	10^{-4}	0.4	-	12	μA
	"L" Level	I_{DL}	V_{OUT}=0V	18	-	-0.4	-	-10^{-4}	-0.4	-	-12	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS},V_{DD}	5	-	5	-	0.005	5	-	150	μA
				10	-	10	-	0.010	10	-	300	
			*	15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

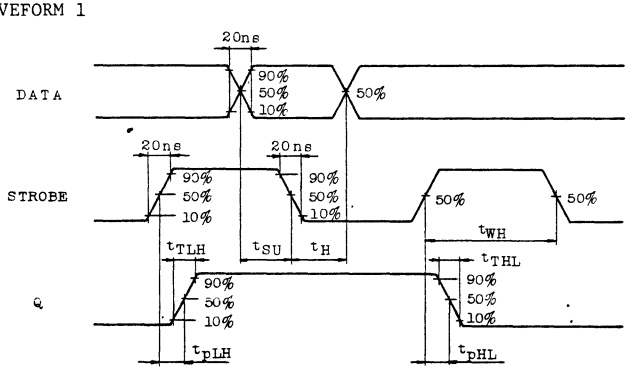
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (STROBE - Q)	t_{pLH} t_{pHL}		5	-	180	360	
			10	-	75	150	
			15	-	55	110	
Propagation Delay Time (DATA - Q)	t_{pLH} t_{pHL}		5	-	160	320	
			10	-	65	130	
			15	-	45	90	
Propagation Delay Time (RESET - Q)	t_{pLH} t_{pHL}		5	-	160	320	
			10	-	65	130	
			15	-	45	90	
Three State Disable Time (DISABLE - Q)	t_{pHZ}	R_L=1kΩ	5	-	45	170	ns
			10	-	25	100	
			15	-	20	70	
Three State Disable Time (DISABLE - Q)	t_{pZH}	R_L=1kΩ	5	-	55	170	
			10	-	25	100	
			15	-	15	70	

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Three State Disable Time (DISABLE - Q)	t_{pLZ}	R_L=1kΩ	5	-	50	130	ns
			10	-	30	80	
			15	-	25	60	
Three State Disable Time (DISABLE - Q)	t_{pZL}	R_L=1kΩ	5	-	70	170	
			10	-	30	100	
			15	-	20	70	
Min. Pulse Width (RESET)	t_{WH}		5	-	50	200	ns
			10	-	20	100	
			15	-	15	70	
Min. Pulse Width (STROBE)	t_{WH}		5	-	40	140	
			10	-	20	70	
			15	-	15	40	
Min. Set-up Time (DATA - STROBE)	t_{SU}		5	-	30	60	ns
			10	-	15	30	
			15	-	10	20	
Min. Hold Time (DATA - STROBE)	t_H		5	-	-10	10	ns
			10	-	-5	10	
			15	-	0	10	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

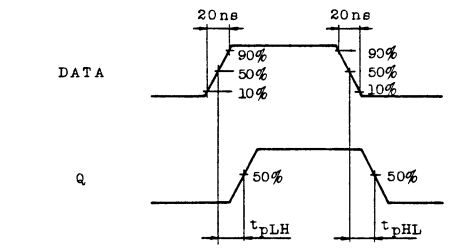
WAVEFORM 1



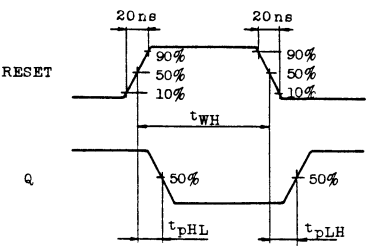
TC4508BP

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

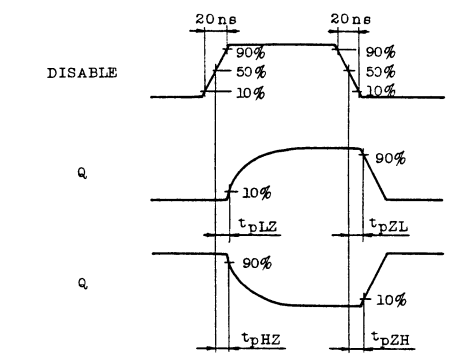
WAVEFORM 2



WAVEFORM 3



WAVEFORM 4

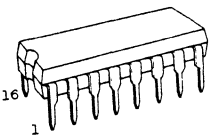


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

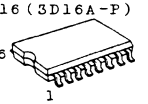
TC4510BP/BF

TC4510BP/TC4510BF PRESETTABLE BCD UP/DOWN COUNTER

TC4510BP/BF is UP/DOWN decade counter having asynchronous RESET and PRESET functions.
When RESET input is set to "H" level, the content of counter is reset to "0" and when RESET is set to "L" and P.E. to "H", inputs A_{IN} through D_{IN} are preset to the counter.
If TC4510BP/BF's are connected in cascade using $\overline{\text{CARRY INPUT}}$ and $\overline{\text{CARRY OUTPUT}}$, decimal counter of N digits with the parallel carry capability can be composed. Switching of counting up or down is achieved by UP/$\overline{\text{DOWN}}$ INPUT. The counter advances its counting condition at the rising edge of CLOCK.



DIP16 (3D16A-P)

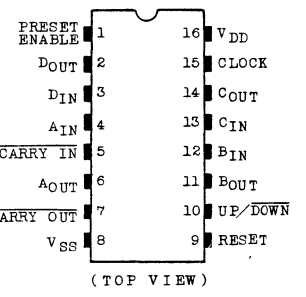


MFP16 (F16GC-P)

ABSOLUTE MAXIMUM RATINGS

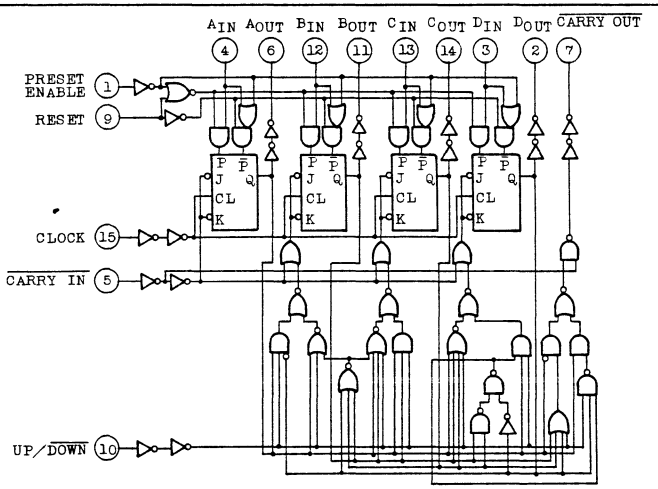
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40~85	°C
Storage Temperature Range	Tstg	-65~150	°C
Lead Temp./Time	Tsol	260°C · 10sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



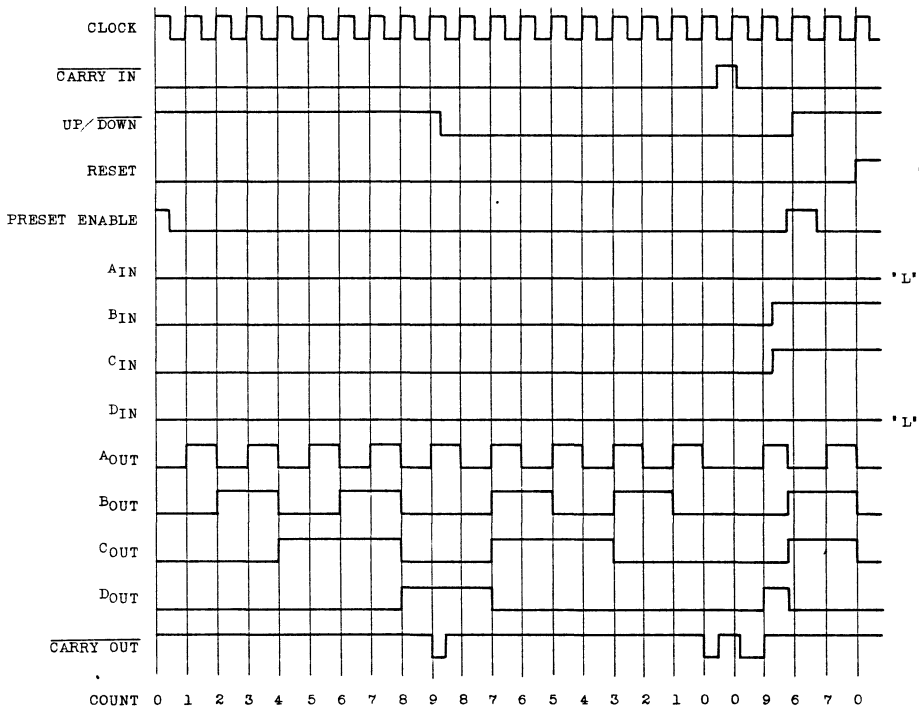
TC4510BP/BF

TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/$\overline{\text{DOWN}}$	PRESET ENABLE	RESET	FUNCTION
H	*	L	L	NO COUNT
L	H	L	L	UP COUNT
L	L	L	L	DOWN COUNT
*	*	H	L	PRESET
*	*	*	H	RESET

* Don't care

TIMING DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V,9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

TC4510BP/BF

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

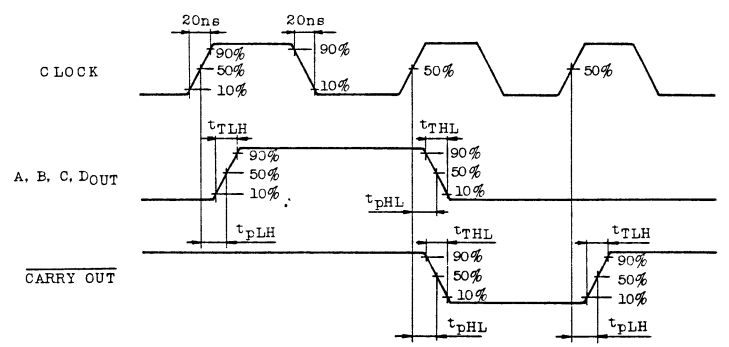
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transistion Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transistion Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK-A,B,C,DOUT)	t_{pLH} t_{pHL}		5	-	210	420	ns
			10	-	85	200	
			15	-	60	150	
Propagation Delay Time (CLOCK-$\overline{\text{CARRY OUT}}$)	t_{pLH} t_{pHL}		5	-	310	620	ns
			10	-	115	240	
			15	-	80	180	
Propagation Delay Time (PRESET ENABLE, RESET-A,B,C,DOUT)	t_{pLH} t_{pHL}		5	-	240	480	ns
			10	-	90	210	
			15	-	65	160	
Propagation Delay Time (PRESET ENABLE, RESET-$\overline{\text{CARRY OUT}}$)	t_{pLH} t_{pHL}		5	-	350	700	ns
			10	-	130	320	
			15	-	90	250	
Propagation Delay Time ($\overline{\text{CARRY IN}}$ - $\overline{\text{CARRY OUT}}$)	t_{pLH} t_{pHL}		5	-	110	250	ns
			10	-	45	120	
			15	-	35	100	
Max. Clock Frequency	f_{CL}		5	1.9	3.8	-	MHz
			10	4	10.3	-	
			15	5.5	15.1	-	

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Max. Clock Input Rise Time	t_{rCL}		5	20	-	-	μs
			10	2.5	-	-	
Max. Clock Input Fall Time	t_{fCL}		15	1.0	-	-	
Min. Clock Pulse Width	t_W		5	-	130	260	ns
			10	-	50	100	
			15	-	35	70	
Min. Pulse Width (PRESET ENABLE, RESET)	t_{WH}		5	-	80	200	ns
			10	-	25	100	
			15	-	10	75	
Min. Set-up Time (UP/$\overline{\text{DOWN}}$-CLOCK)	t_{SU}		5	-	170	360	ns
			10	-	65	160	
			15	-	45	110	
Min. Set-up Time ($\overline{\text{CARRY IN}}$ - CLOCK)	t_{SU}		5	-	80	160	ns
			10	-	30	60	
			15	-	10	45	
Min. Removal Time (PRESET ENABLE, RESET-CLOCK)	t_{rem}		5	-	65	150	ns
			10	-	20	80	
			15	-	10	60	
Input Capacitance	C_{IN}				5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

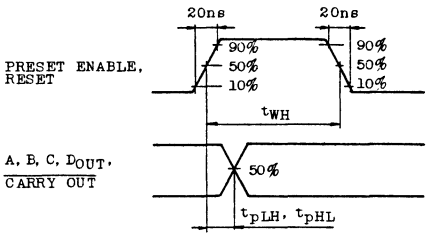
WAVEFORM 1



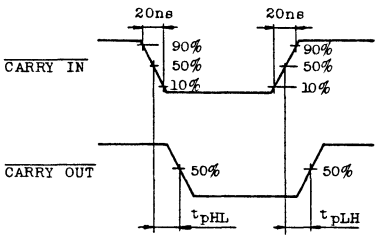
TC4510BP/BF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

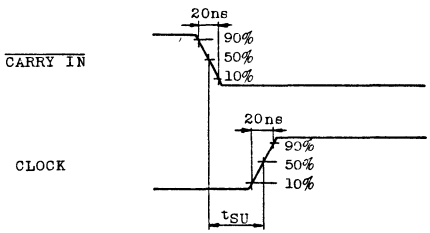
WAVEFORM 2



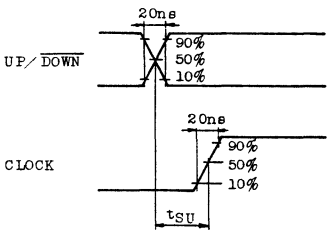
WAVEFORM 3



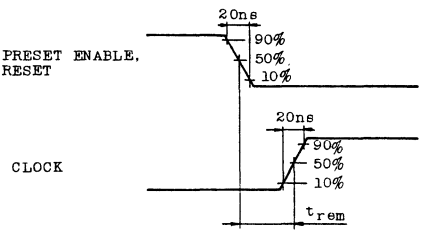
WAVEFORM 4



WAVEFORM 5



WAVEFORM 6

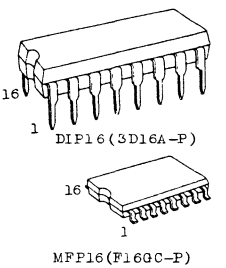


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4511BP/BF

C4511BP/TC4511BF BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

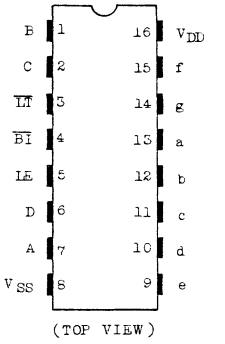
TC4511BP/BF is decoder which converts the input f BCD code into the 7 segment display element driving ignal and the output has complementary connection of PN bipolar transistor and N-channel MOS FET. Therefore, not only capability of directly driving cathode ommon type LED, this has capability of driving various isplay elements with simple interface circuits.
T input and $\overline{BI}$ input are to force all the outputs to e "H" (illuminated) and "L" (not illuminated) respectively regardless of BCD input. As the latch conrolled by common LE input is inserted in each of four nput lines, static display of dynamic information can e achieved. When an invalid BCD input, "10" or higher s applied, all the outputs become "L"(not illuminated).



BSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
C Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
nput Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
utput Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
C Input Current	I_{IN}	±10	mA
utput High Current	I_{OH}	-50	mA
ower Dissipation	P_D	300(DIP)/180(MFP)	mW
perating emperature Range	T_A	-40 ~ 85	°C
torage emperature Range	Tstg	-65 ~ 150	°C
ead Temp./Time	T_{sol}	260°C • 10 sec	

PIN ASSIGNMENT

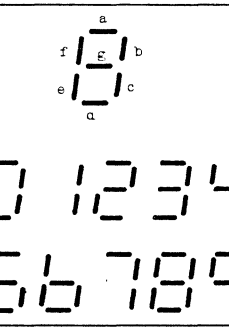


TRUTH TABLE

INPUT							OUTPUT							DISPLAY
E	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	MODE
<	*	L	*	*	*	*	H	H	H	H	H	H	H	8
<	L	H	*	*	*	*	L	L	L	L	L	L	L	BLANK
J	H	H	L	L	L	L	H	H	H	H	H	H	L	0
J	H	H	L	L	L	H	L	H	H	L	L	L	L	1
J	H	H	L	L	H	L	H	H	L	H	H	L	H	2
J	H	H	L	L	H	H	H	H	H	H	L	L	H	3
J	H	H	L	H	L	L	L	H	H	L	L	H	H	4
J	H	H	L	H	L	H	H	L	H	H	L	H	H	5
J	H	H	L	H	H	L	L	L	H	H	H	H	H	6
J	H	H	L	H	H	H	H	H	H	L	L	L	L	7
J	H	H	H	L	L	L	H	H	H	H	H	H	H	8
J	H	H	H	L	L	H	H	H	H	L	L	H	H	9
J	H	H	H	L	H	L	L	L	L	L	L	L	L	BLANK
J	H	H	H	L	H	H	L	L	L	L	L	L	L	BLANK
J	H	H	H	H	*	*	L	L	L	L	L	L	L	BLANK
1	H	H	*	*	*	*	△△							△△

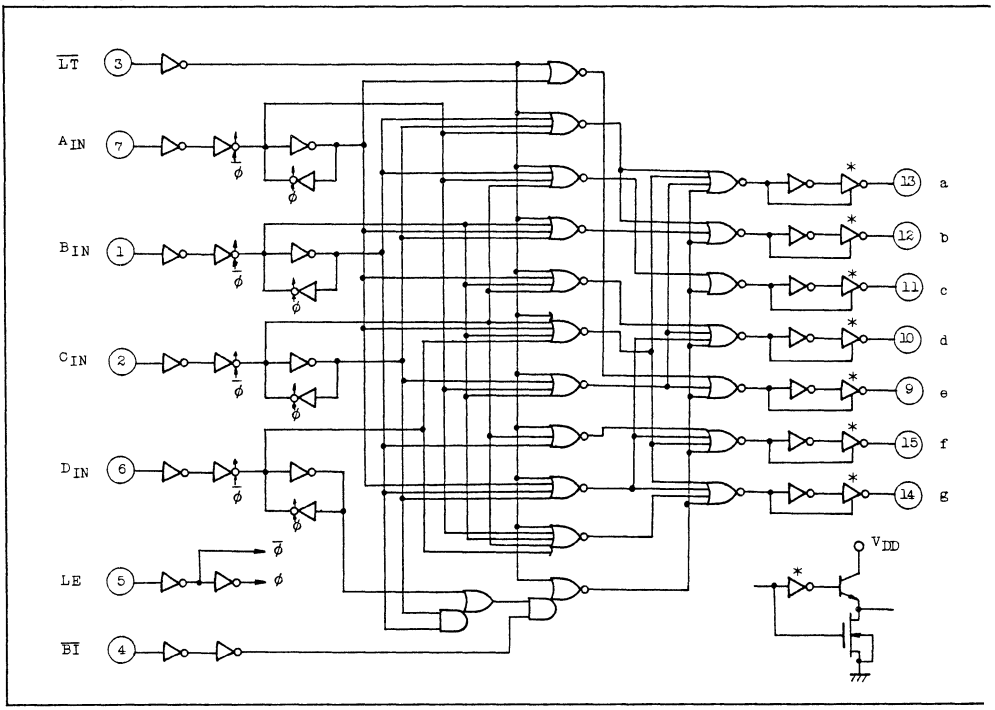
* : DON'T CARE △△ : DEPONDS UPON THE BCD CODE PREVIOUSLY APPLIED WHEN LE 'L'

DISPLAY



TC4511BP/BF

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.0	-	4.0	4.5	-	4.0	-	V
			10	9.0	-	9.0	9.5	-	9.0	-	
		V_{IN}=V_{SS}, V_{DD}	15	14.0	-	14.0	14.5	-	14.0	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
			1.0	-	0.05	-	0.00	0.05	-	0.05	
		V_{IN}=V_{SS}, V_{DD}	15	-	0.05	-	0.00	0.05	-	0.05	

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

HARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
utput High Current	I_{OH}	V_{ON}=3.5V	5	20	-	20		-	15	-	mA
		V_{ON}=8.5V	10	25	-	25		-	20	-	
		V_{ON}=13.5V	15	30	-	30		-	25	-	
		V_{IN}=V_{DD}, V_{SS}									
utput Low Current	I_{OL}	V_{ON}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{ON}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{ON}=1.5V	15	3.6	-	3.0		-	2.4	-	
		V_{IN}=V_{DD}, V_{SS}									
nput High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.50	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
nput Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.50	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
nput "H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
urrent "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
uiescent Device Current	I_{DD}	V_{IN}=V_{DD}, V_{SS}	5	-	20	-	0.005	20	-	150	μA
			10	-	40	-	0.010	40	-	300	
		*	15	-	80	-	0.015	80	-	600	

All valid input combinations.

'NAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF, R_L=10kΩ)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
utput Transition Time (Low to High)	t_{TLH}		5	-	40	80	ns
			10	-	25	60	
			15	-	20	50	
utput Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	40	100	
			15	-	30	80	
opagation Delay Time (DATA - OUT)	t_{pLH}		5	-	550	1100	
			10	-	240	480	
			15	-	170	340	
opagation Delay Time (DATA - OUT)	t_{pHL}		5	-	550	1100	
			10	-	240	480	
			15	-	170	340	

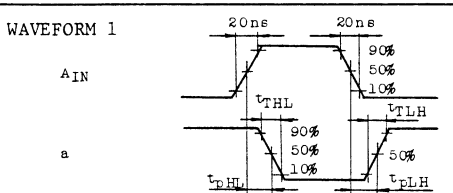
TC4511BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Continued)

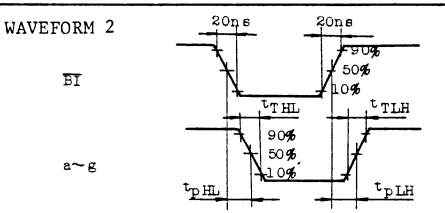
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Propagation Delay Time ($\overline{BI}$ - OUT)	t_{pLH}		5	-	350	700	ns
			10	-	140	280	
			15	-	100	200	
Propagation Delay Time ($\overline{BI}$ - OUT)	t_{pHL}		5	-	350	700	
			10	-	140	280	
			15	-	100	200	
Propagation Delay Time ($\overline{LT}$ - OUT)	t_{pLH} t_{pHL}		5	-	350	700	
			10	-	150	300	
			15	-	120	240	
Propagation Delay Time (LE - OUT)	t_{pLH} t_{pHL}		5	-	300	600	
			10	-	130	300	
			15	-	100	250	
Min. Pulse Width (LE)	t_{WL}		5	-	100	300	
			10	-	50	150	
			15	-	40	120	
Min. Set-up Time (DATA - LE)	t_{SU}		5	-	80	200	
			10	-	40	100	
			15	-	30	75	
Min. Hold Time (DATA - LE)	t_H		5	-	-80	50	
			10	-	-40	20	
			15	-	-30	15	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

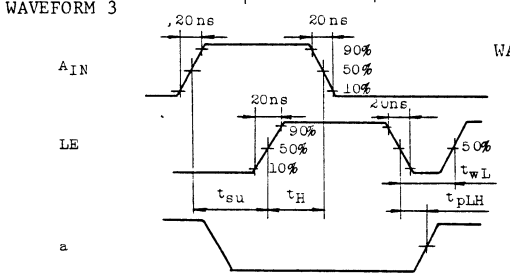
WAVEFORM 1



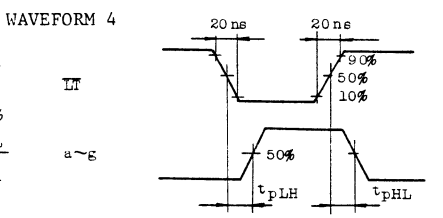
WAVEFORM 2



WAVEFORM 3



WAVEFORM 4



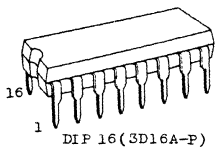
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4512BP/B

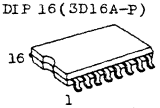
TC4512BP/TC4512BF 8-CHANNEL DATA SELECTOR

TC4512BP/BF is data selector which selects 8 channel data inputs (X0 through X7) according to binary address inputs A, B and C.

Since high impedance can be given to output Z by setting DISABLE input to "H", the wired-OR arrangement can be achieved. DISABLE input takes precedence over other inputs giving the output high impedance. If DISABLE = "L" and INHIBIT = "H", the data select operation is inhibited and output Z becomes "L" Level.



DIP 16(3D16A-P)

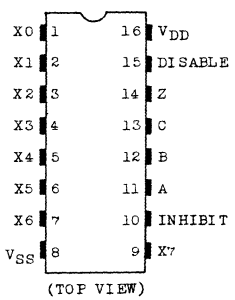


MFP 16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

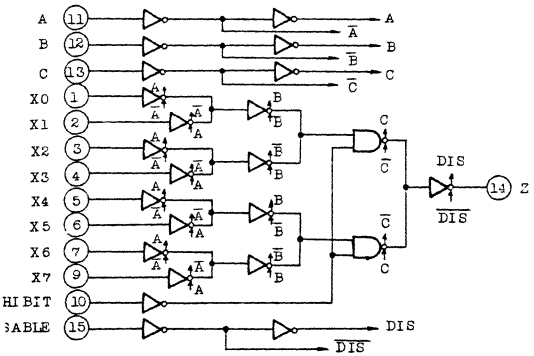
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TRUTH TABLE

INPUTS					OUTPUT
A	B	C	INHIBIT	DISABLE	Z
L	L	L	L	L	X0
H	L	L	L	L	X1
L	H	L	L	L	X2
H	H	L	L	L	X3
L	L	H	L	L	X4
H	L	H	L	L	X5
L	H	H	L	L	X6
H	H	H	L	L	X7
*	*	*	H	L	
*	*	*	*	H	

* : DON'T CARE
HZ: HIGH IMPEDANCE

4512BP/BF

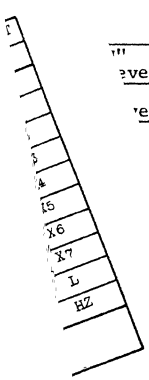
OMMENDED OPERATING CONDITION (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
: Supply Voltage	V_{DD}		3	-	18	V
ıput Voltage	V_{IN}		0	-	V_{DD}	V

ATIC ELECTRICAL CHARACTERISTIC (V_{SS}=0V)

:HARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS}$, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	V
		$V_{IN}=V_{SS}$, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V V_{OH}=9.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=13.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		$V_{IN}=V_{SS}$, V_{DD}	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V V_{OL}=1.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		$V_{IN}=V_{SS}$, V_{DD}	15	4.0	-	3.4	15.0	-	2.8	-	
t High ge	V_{IH}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V V_{OUT}=1.5V,13.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
		$\|I_{OUT}\|$<1μA	15	11.0	-	11.0	8.25	-	11.0	-	
w	V_{IL}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V V_{OUT}=1.5V,13.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			10	-	3.0	-	4.5	3.0	-	3.0	
		$\|I_{OUT}\|$<1μA	15	-	4.0	-	6.75	4.0	-	4.0	
evel	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
vel	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
l	I_{DH}	V_{OUT}=18V	18	-	0.4	-	10^{-4}	0.4	-	12	μA
	I_{DL}	V_{OUT}=0V	18	-	-0.4	-	-10^{-4}	-0.4	-	-12	
DD		$V_{IN}=V_{SS}$, V_{DD}	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
		*	15	-	20	-	0.015	20	-	600	

mbinations.

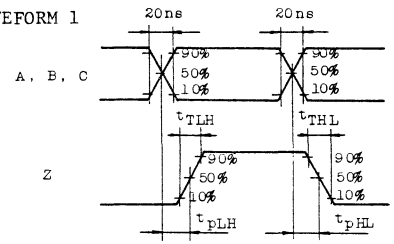


NAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

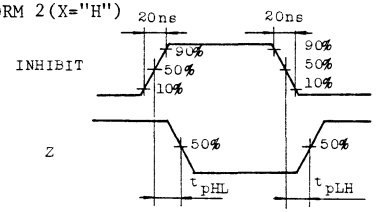
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
utput Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
utput Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
ropagation Delay Time (INHIBIT - Z)	t_{pLH} t_{pHL}		5	-	140	280	
			10	-	60	140	
			15	-	40	100	
ropagation Delay Time (A, B, C - Z)	t_{pLH} t_{pHL}		5	-	240	480	
			10	-	95	190	
			15	-	65	130	
ropagation Delay Time (X - Z)	t_{pLH} t_{pHL}		5	-	210	420	
			10	-	85	170	
			15	-	60	120	
hree State Disable Time (DISABLE - Z)	t_{pZL}, t_{pLZ} t_{pHZ}, t_{pZH}	R_L=1kΩ	5	-	60	120	
			10	-	25	60	
			15	-	20	40	
nput Capacitance	C_{IN}			-	5	7.5	pF

.VEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

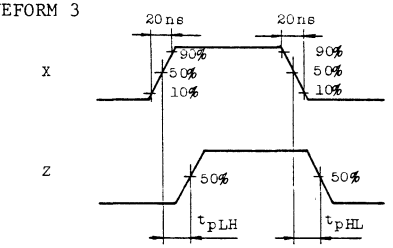
WAVEFORM 1



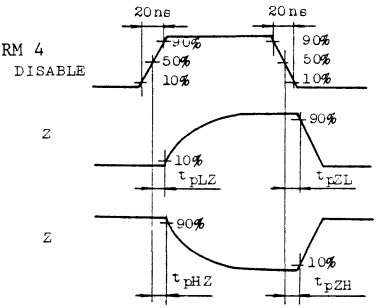
WAVEFORM 2(X="H")



WAVEFORM 3



WAVEFORM 4

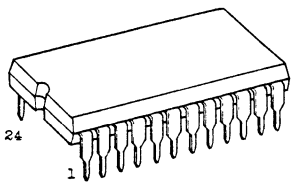


TC4514BP
TC4515BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4514BP 4-BIT LATCH/4-TO-16 LINE DECODER (Output Active High Option)
TC4515BP 4-BIT LATCH/4-TO-16 LINE DECODER (Output Active Low Option)

TC4514BP and TC4515BP are decoders which convert 4 bit binary input signal to hexadecimal output signal and these have the decode inhibit input and the latch function.
TC4514BP gives "H" level only to the selected output among 16 outputs and TC4515BP gives "L" only to the selected output. When INHIBIT input is "H", the selected output does not exist making all the outputs "L" for TC4514BP and all the outputs "H" for TC4515BP. When STROBE input is "H", the output corresponding to DATA 1 through DATA 4 are selected and latched by the transition of STROBE from "H" to "L".

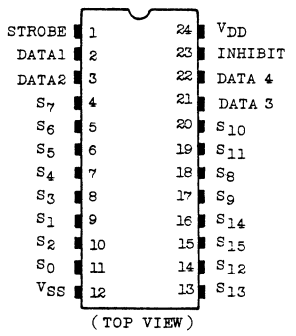


DIP 24 (6D24A-P)

ABSOLUTE MAXIMUM RATINGS

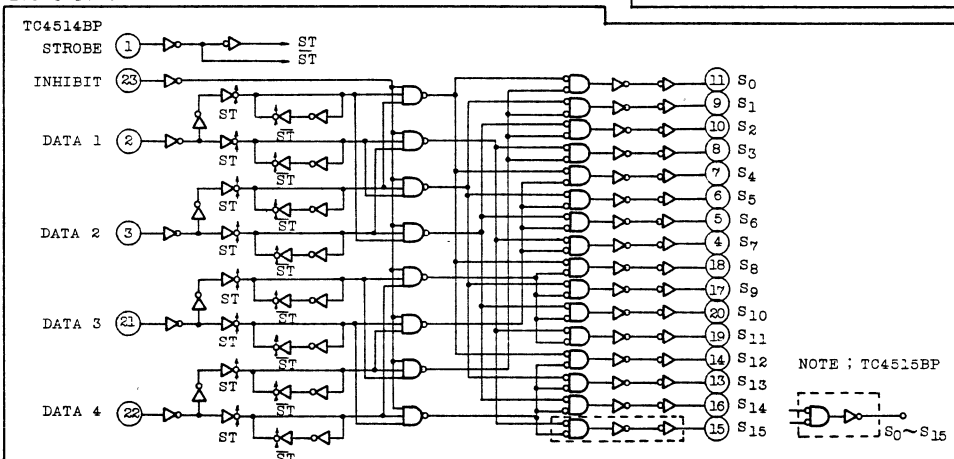
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



(TOP VIEW)

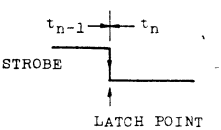
LOGIC DIAGRAM



TH TABLE

HIBIT	DATA INPUT				SELECTED OUTPUT TC4514BP - "H" TC4515BP - "L"
	$DATA_1$	$DATA_2$	$DATA_3$	$DATA_4$	
L	L	L	L	L	S_0
L	H	L	L	L	S_1
L	L	H	L	L	S_2
L	H	H	L	L	S_3
L	L	L	H	L	S_4
L	H	L	H	L	S_5
L	L	H	H	L	S_6
L	H	H	H	L	S_7
L	L	L	L	H	S_8
L	H	L	L	H	S_9
L	L	H	L	H	S_{10}
L	H	H	L	H	S_{11}
L	L	L	H	H	S_{12}
L	H	L	H	H	S_{13}
L	L	H	H	H	S_{14}
L	H	H	H	H	S_{15}
H	*	*	*	*	TC4514BP-ALL OUTPUTS "L" TC4515BP-ALL OUTPUTS "H"

- STROBE="H" ; See Truth table
- STROBE="L" ; Outputs hold the data when STROBE goes "LOW"



- * Don't care

OMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
ut Voltage	V_{IN}		0	-	V_{DD}	V

TIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
h-Level put Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
-Level put Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	

TC4514BP, TC4515BP

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNI
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	1.13	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		V_{IN}=V_{SS},V_{DD}									mA
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		V_{IN}=V_{SS},V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$ <1μA									V
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$ <1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	μA
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	
			10	-	10	-	0.010	10	-	300	μA
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

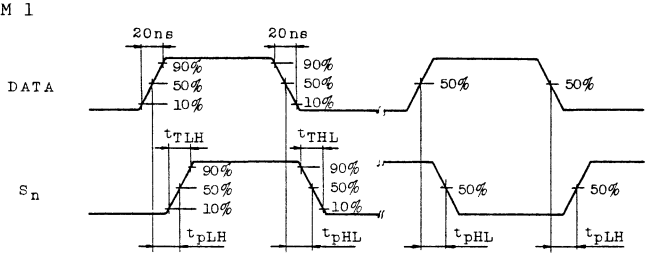
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	

NAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

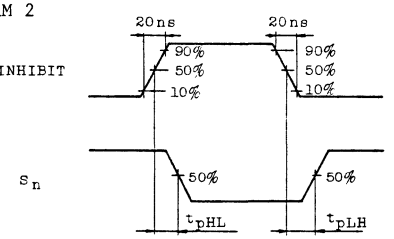
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
tput Transition Time (High to Low)	t_{THL}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
›pagation Delay ne (STROBE, DATA - Sn)	t_{pLH} t_{pHL}		5	-	260	970	ns
			10	-	110	370	
			15	-	80	270	
›pagation Delay ne (INHIBIT - Sn)	t_{pLH} t_{pHL}		5	-	150	500	
			10	-	65	220	
			15	-	50	170	
ı. Pulse Width (STROBE)	t_{WH}		5	-	40	250	ns
			10	-	20	100	
			15	-	15	75	
ı. Hold Time (DATA - STROBE)	t_{SU}		5	-	20	150	ns
			10	-	10	70	
			15	-	5	40	
›ut Capacitance	C_{IN}			-	5	7.5	pF

VEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

AVEFORM 1



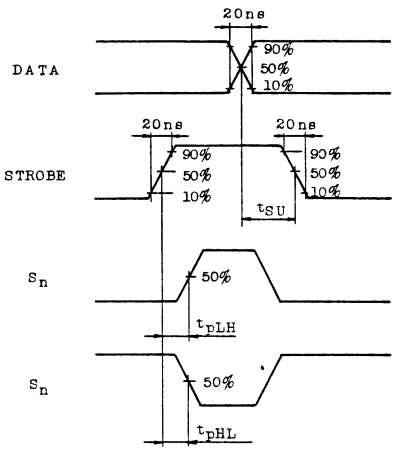
AVEFORM 2



TC4514BP, TC4515BP

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 3

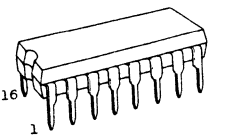


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

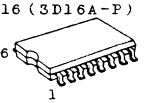
TC4516BP/BF

516BP/TC4516BF PRESETTABLE BINARY UP/DOWN COUNTER

516BP/BF is UP/DOWN 4 bit binary counter having
nchronous and PRESET functions.
n RESET input is set to "H" level, the content of
nter is reset to "O" and when RESET is set to "L"
P.E. to "H", inputs AIN through DIN are preset
o the counter.
TC4516BP/BF'S are connected in cascade using
$\overline{\text{RY INPUT}}$ and $\overline{\text{CARRY OUTPUT}}$, 4 × N bits binary
nter with parallel counter can be composed.
tching of counting up or down is achieved by
$\overline{\text{DOWN}}$ input. The counter advances its counting
dition at the rising edge of CLOCK.



DIP16 (3D16A-P)

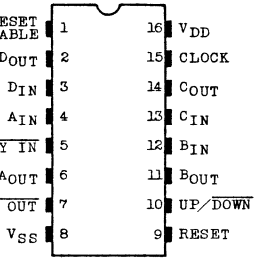


MFP16 (F16GC-P)

OLUTE MAXIMUM RATINGS

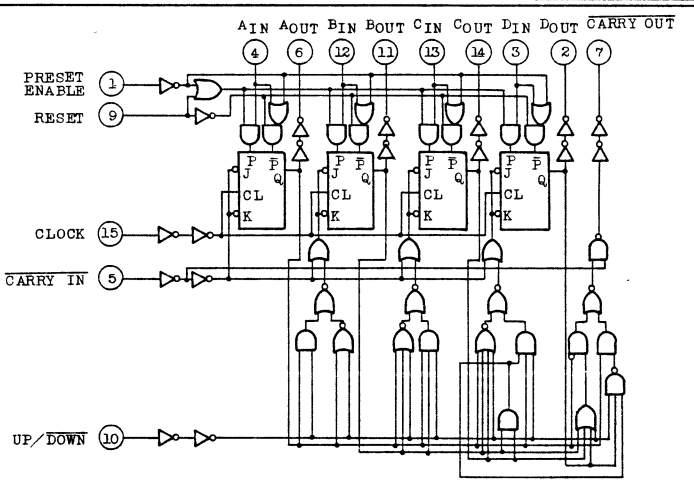
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
ut Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
put Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
er Dissipation	P_D	300(DIP)/180(MFP)	mW
rating Temperature ge	T_A	-40 ~ 85	°C
rage Temperature ge	T_{stg}	-65 ~ 150	°C
d Temp./Time	T_{sol}	260 · 10	°C·sec

PIN ASSIGNMENT



(TOP VIEW)

IC DIAGRAM



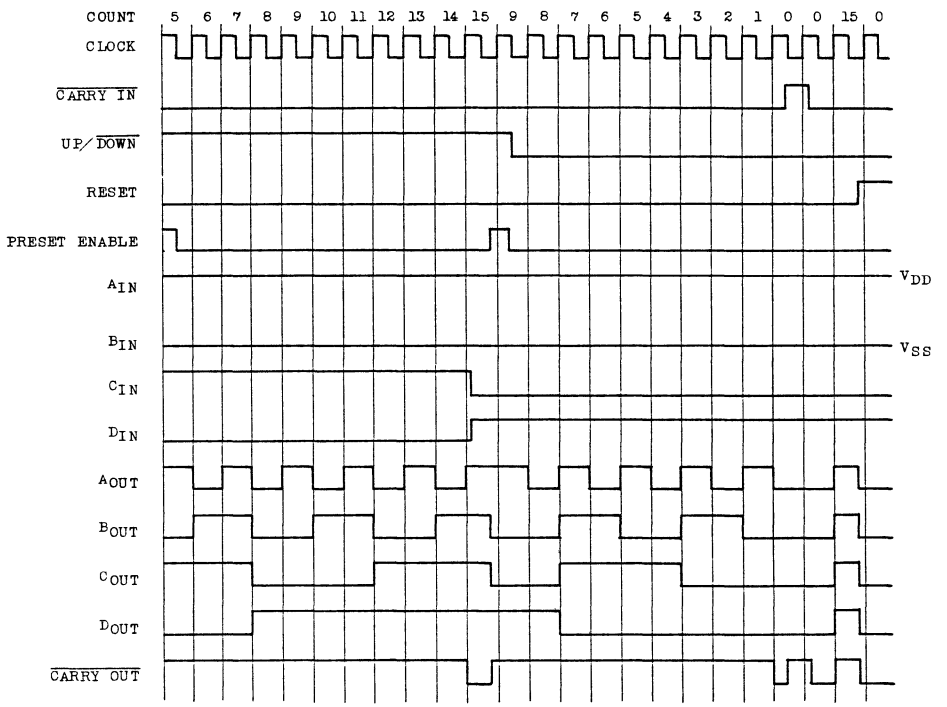
TC4516BP/BF

TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/$\overline{\text{DOWN}}$	PRESET ENABLE	RESET	FUNCTION
H	*	L	L	NO COUNT
L	H	L	L	UP COUNT
L	L	L	L	DOWN COUNT
*	*	H	L	PRESET
*	*	*	H	RESET

* Don't Care

TIMING DIAGRAM



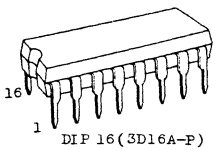
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4512BP/BF

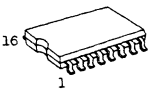
C4512BP/TC4512BF 8-CHANNEL DATA SELECTOR

TC4512BP/BF is data selector which selects 8 hannel data inputs (X0 through X7) according to inary address inputs A, B and C.

ince high impedance can be given to output Z by sett- ng DISABLE input to "H", the wired-OR arrangement can e achieved. DISABLE input takes precedence over ther inputs giving the output high impedance. f DISABLE = "L" and INHIBIT = "H", the data select peration is inhibited and output Z becomes "L" Level.



DIP 16(3D16A-P)

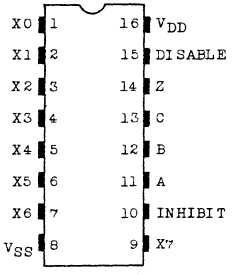


MFP 16(F16GC-P)

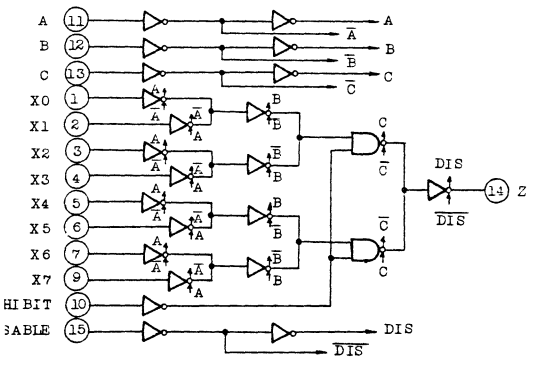
ISOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
put Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
tput Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	±10	mA
wer Dissipation	P_D	300(DIP)/180(MFP)	mW
erating mperature Range	T_A	-40 ∿ 85	°C
orage mperature Range	T_{stg}	-65 ∿ 150	°C
ad Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



GIC DIAGRAM



TRUTH TABLE

INPUTS					OUTPUT
A	B	C	INHIBIT	DISABLE	Z
L	L	L	L	L	X0
H	L	L	L	L	X1
L	H	L	L	L	X2
H	H	L	L	L	X3
L	L	H	L	L	X4
H	L	H	L	L	X5
L	H	H	L	L	X6
H	H	H	L	L	X7
*	*	*	H	L	L
*	*	*	*	H	HZ

* : DON'T CARE
HZ: HIGH IMPEDANCE

TC4512BP/BF

RECOMMENDED OPERATING CONDITION (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTIC (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		V_{IN}=V_{SS}, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		V_{IN}=V_{SS}, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		V_{IN}=V_{SS}, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		V_{IN}=V_{SS}, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
3-State Output Leakage Current "H" Level	I_{DH}	V_{OUT}=18V	18	-	0.4	-	10^{-4}	0.4	-	12	μA
3-State Output Leakage Current "L" Level	I_{DL}	V_{OUT}=0V	18	-	-0.4	-	-10^{-4}	-0.4	-	-12	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD}	5	-	5	-	0.005	5	-	150	μA
		*	10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

:OMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
ut Voltage	V_{IN}		0	-	V_{DD}	V

TIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ARACTERISTIC		SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
h-Level put Voltage		V_{OH}	$\|I_{OUT}\| < 1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
-Level put Voltage		V_{OL}	$\|I_{OUT}\| < 1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
put High rent		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
put Low rent		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
ut High tage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 2.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\| < 1\mu A$									
ut Low tage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 2.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\| < 1\mu A$									
ut rrent	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

TC4516BP/BF

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNI
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μ
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

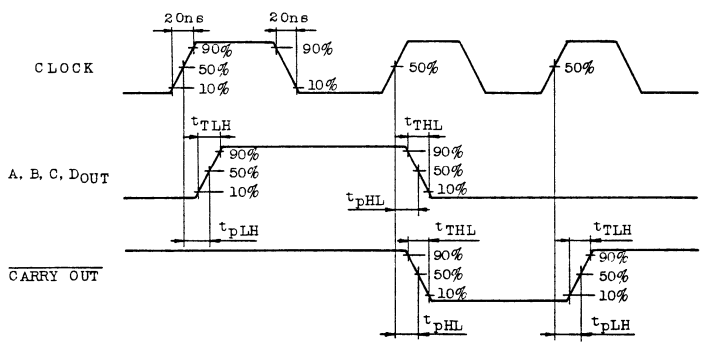
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK-A,B,C,D_{OUT})	t_{pLH} t_{pHL}		5	-	210	420	ns
			10	-	85	200	
			15	-	60	150	
Propagation Delay Time (CLOCK-$\overline{\text{CARRY OUT}}$)	t_{pLH} t_{pHL}		5	-	310	620	ns
			10	-	115	240	
			15	-	80	180	
Propagation Delay Time (PRESET ENABLE, RESET-A,B,C,D_{OUT})	t_{pLH} t_{pHL}		5	-	240	480	ns
			10	-	90	210	
			15	-	65	160	
Propagation Delay Time (PRESET ENABLE, RESET-$\overline{\text{CARRY OUT}}$)	t_{pLH} t_{pHL}		5	-	350	700	ns
			10	-	130	320	
			15	-	90	250	
Propagation Delay Time ($\overline{\text{CARRY IN}}$ - $\overline{\text{CARRY OUT}}$)	t_{pLH} t_{pHL}		5	-	110	250	ns
			10	-	45	120	
			15	-	35	100	
Max. Clock Frequency	f_{CL}		5	1.9	3.8	-	MHz
			10	4	10.3	-	
			15	5.5	15.1	-	

AMIC ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
. Clock Input Rise e	t_{rCL}		5	2.0	-	-	
			10	2.5	-	-	μs
. Clock Input Fall e	t_{fCL}		15	1.0	-	-	
			5	-	130	260	
. Clock Pulse Width	t_W		10	-	50	100	ns
			15	-	35	70	
. Pulse Width			5	-	80	200	
RESET ENABLE, RESET)	t_{WH}		10	-	25	100	ns
			15	-	10	75	
. Set-up Time			5	-	170	360	
P/$\overline{\text{DOWN}}$-CLOCK)	t_{SU}		10	-	65	160	ns
			15	-	45	110	
. Set-up Time			5	-	80	160	
$\overline{\text{ARRY IN}}$ - CLOCK)	t_{SU}		10	-	30	60	ns
			15	-	10	45	
. Set-up Time			5	-	65	150	
RESET ENABLE, ESET-CLOCK)	t_{rem}		10	-	20	80	ns
			15	-	10	60	
ut Capacitance	C_{IN}				5	7.5	pF

EFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

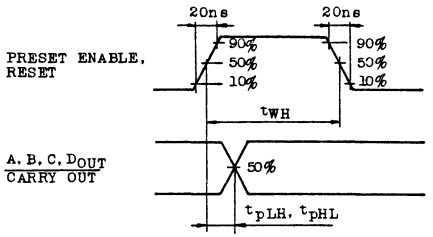
VEFORM 1



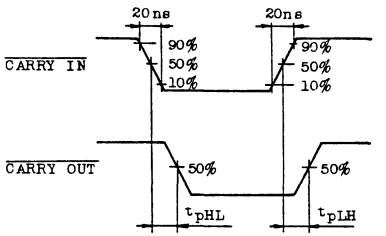
TC4516BP/BF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

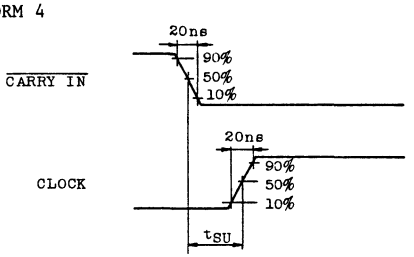
WAVEFORM 2



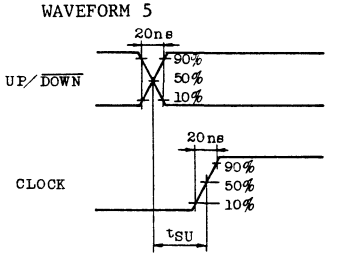
WAVEFORM 3



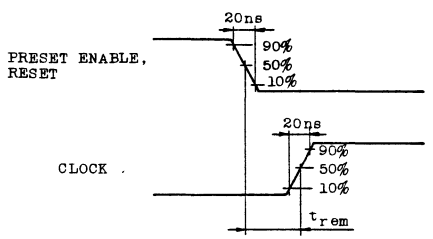
WAVEFORM 4



WAVEFORM 5



WAVEFORM 6

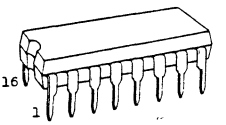


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

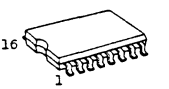
TC4518BP/BF
TC4520BP/BF

4518BP/TC4518BF DUAL BCD UP COUNTER
4520BO/TC4520BF DUAL BINARY UP COUNTER

4518BP/BF and TC4520BP/BF are up counters of BCD or bit binary.
ince both of TC4518BP/BF and TC4520BP/BF contain two lependent circuits of counters with the same nctions in one package, counting or frequency vision of two BCD digits or eight binary bits can be nieved with one IC. The counters can be reset to ' ($Q_0 \sim Q_3$="L") by giving "H" level signal to RESET out regardless of other inputs.
e counting condition is changed by the rising edge CLOCK input if ENABLE="H" or by the falling edge ENABLE if CLOCK="L".



DIP16 (3D16A-P)

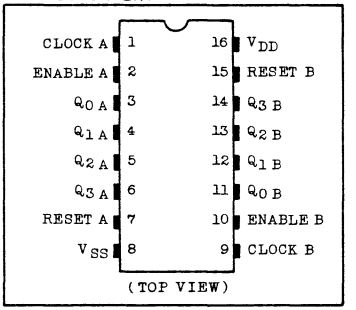


MFP16 (F16GC-P)

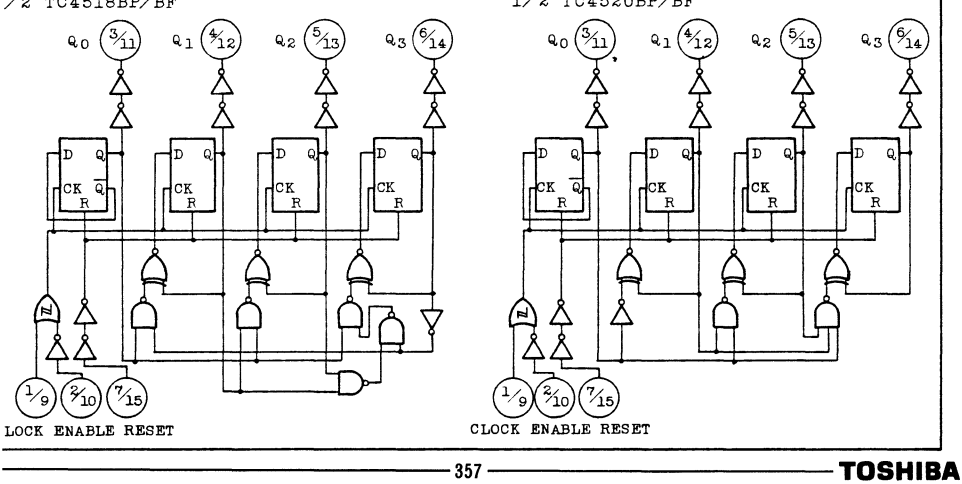
SOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
out Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
tput Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
wer Dissipation	P_D	300(DIP)/180(MFP)	mW
erating Temperature nge	T_A	-40 ~ 85	°C
orage Temperature nge	T_{stg}	-65 ~ 150	°C
ad Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



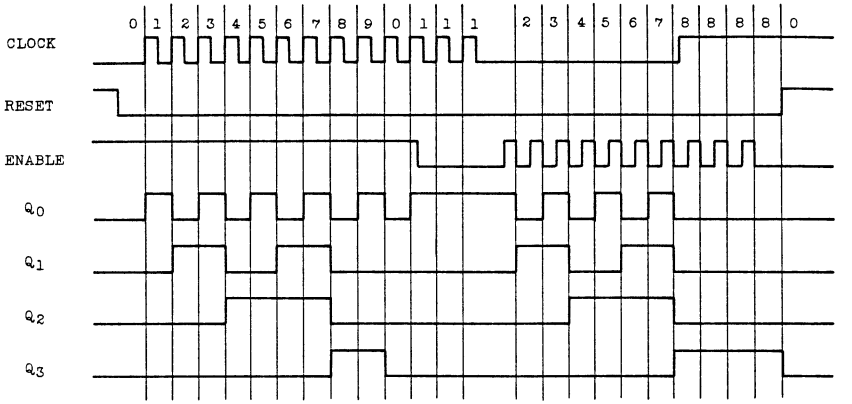
LOGIC DIAGRAM



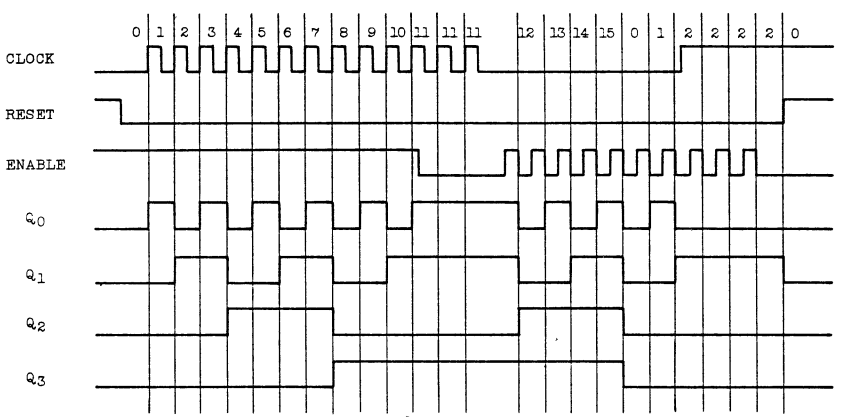
TC4518BP/BF, TC4520BP/BF

TIMING CHART

TC4518BP/BF



TC4520BP/BF



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

ATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

HARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
gh-Level tput Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
w-Level tput Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.05	0.05	-	0.05	
tput High rrent	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
tput Low rrent	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
put High ltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
put Low ltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.-	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
put rrent "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
put rrent "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
iescent Device rrent	I_{DD}	$V_{IN}=V_{SS},V_{DD}$	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
		*	15	-	20	-	0.015	20	-	600	

All valid input combinations.

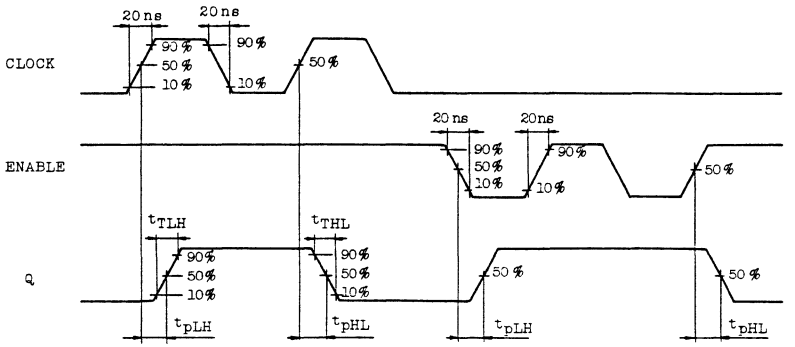
TC4518BP/BF, TC4520BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

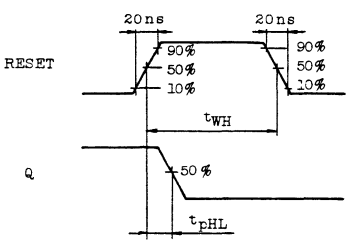
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK, ENABLE - Q)	t_{pLH} t_{pHL}		5	-	280	560	ns
			10	-	110	230	
			15	-	80	160	
Propagation Delay Time (RESET - Q)	t_{pHL}		5	-	160	650	
			10	-	70	225	
			15	-	50	170	
Max. Clock Frequency	f_{CL}		5	1.5	5	-	MHz
			10	3	14	-	
			15	4	18	-	
Max. Clock Input Rise/ Fall Time	t_{rCL} t_{fCL}		5	No Lomits			μs
			10				
			15				
Max. Input Rise/ Fall Time (ENABLE)	t_r t_f		5	20	-	-	
			10	2.5	-	-	
			15	1.0	-	-	
Min. Clock Pulse Width	t_W		5	-	100	200	ns
			10	-	35	100	
			15	-	30	70	
Min. Pulse Width (ENABLE)	t_W		5	-	100	400	
			10	-	35	200	
			15	-	30	140	
Min. Pulse Width (RESET)	t_{WH}		5	-	55	250	
			10	-	25	110	
			15	-	20	80	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1

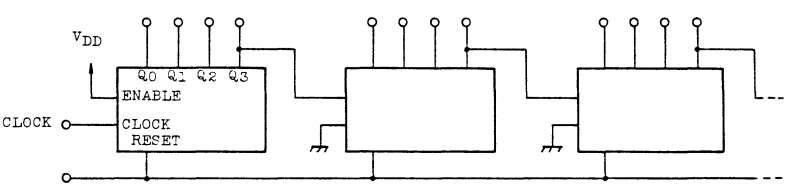


WAVEFORM 2



APPLICATION CIRCUIT

(1) RIPPLE CARRY UP COUNTER

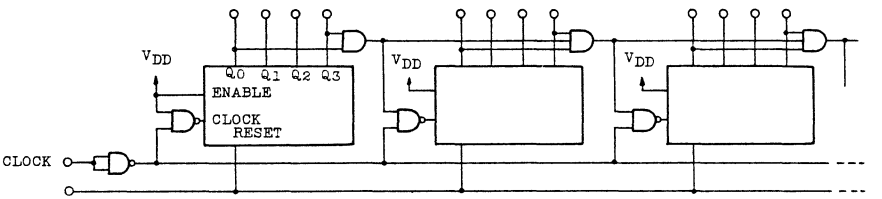


TC4518BP/BF, TC4520BP/BF

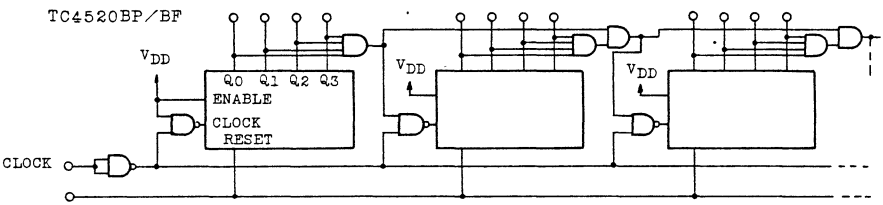
APPLICATION CIRCUIT

(2) PARALLEL CARRY UP COUNTER

TC4518BP/BF



TC4520BP/BF



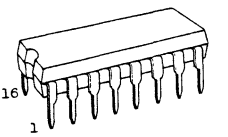
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4519BP

TC4519BP 4-BIT AND/OR SELECTOR

The TC4519BP is a combined gate available as 4-bit AND/OR select gate, quad 2-channel data selector or quad exclusive-NOR gate according to the conditions of two control inputs A and B.

Since all the outputs are provided with the buffers of two-stage inverters, the input/output transmission characteristics have been improved and the noise immunity has been elevated. Thus, as increase in propagation delay time caused by an increase in load capacity is kept to a minimum.

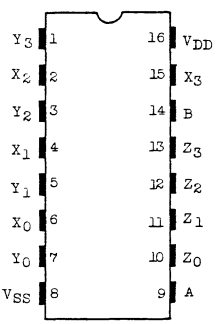


DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

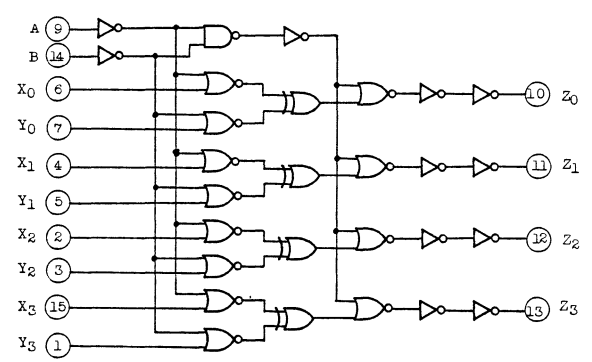
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ∿ 85	°C
Storage Temperature Range	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C • 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TRUTH TABLE

CONTROL INPUTS		OUTPUT
A	B	Z_n
L	L	L
L	H	Y_n
H	L	X_n
H	H	$X_n \odot Y_n$

$X_n \odot Y_n \equiv X_n$ (Exclusive-NOR) Y_n

$= X_n \cdot Y_n + \overline{X}_n \cdot \overline{Y}_n$

TC4519BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

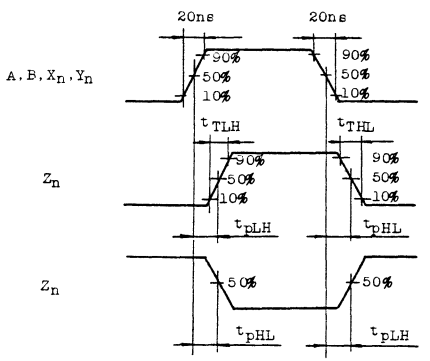
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}$, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}$, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
		*	15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (A, B, Xn, Yn - Zn)	t_{pLH}		5	-	190	500	
	t_{pHL}		10	-	80	225	
			15	-	60	165	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



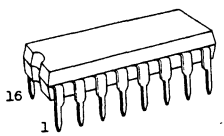
TC4521BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4521BP 24-STAGE FREQUENCY DIVIDER

TC4521BP is frequency divider consisting of 24 stages of flip-flops. The input section is equipped with an inverter to enable to use either RC oscillator circuit or crystal oscillator circuit and to accept pulse from external clock source.

Each flip-flop is inverted by the falling edge of the output of previous stage flip-flop and this can count up to the maximum of 2^{24}=16,777,216.
Since six outputs, 2^{18}, 2^{19}, 2^{20}, 2^{21}, 2^{22} and 2^{23} are available besides of 2^{24}, adjustment of frequency divided output can be achieved.

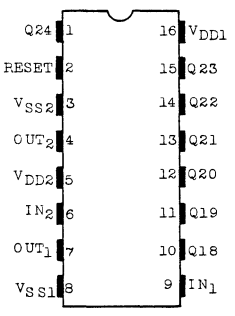


DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

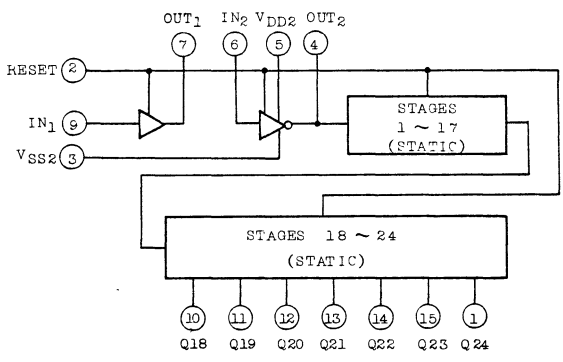
CHARACTERISTIC	SYMBOL	RATING	UNITS
DC Supply Voltage	V_{DD1}	V_{SS1}-0.5 ∿ V_{SS1}+20	V
	V_{DD2}	V_{SS1}-0.5 ∿ V_{DD1}+0.5	
Input Voltage	V_{IN}	V_{SS1}-0.5 ∿ V_{DD1}+0.5	V
Output Voltage	V_{OUT}	V_{SS1}-0.5 ∿ V_{DD1}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ∿ 85	°C
Storage Temperature Range	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C • 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

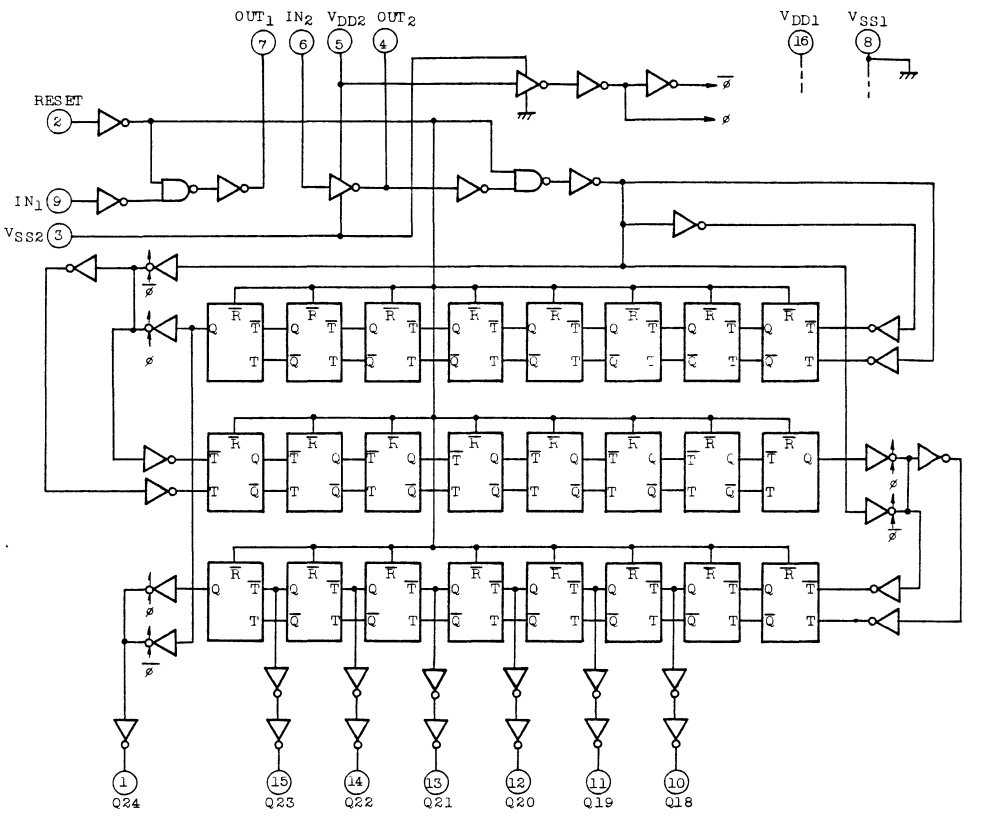
BLOCK DIAGRAM



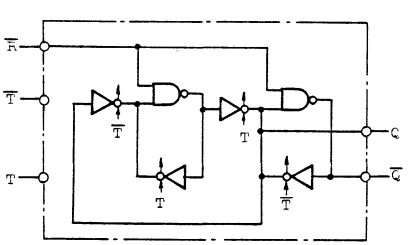
COUNT CAPACITY

OUTPUT	COUNT CAPACITY
Q18	2^{18} = 262,144
Q19	2^{19} = 524,288
Q20	2^{20} = 1,048,576
Q21	2^{21} = 2,097,152
Q22	2^{22} = 4,194,304
Q23	2^{23} = 8,388,608
Q24	2^{24} = 16,777,216

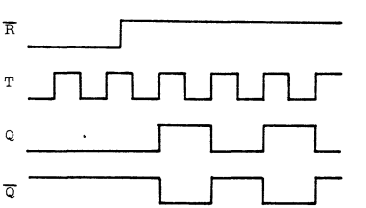
LOGIC DIAGRAM



INTERNAL FLIP FLOP LOGIC DIAGRAM



FLIP FLOP TIMING CHART



TC4521BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD1}, V_{DD2}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD1}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS1}=V_{SS2}=0V, V_{DD1}=V_{DD2})

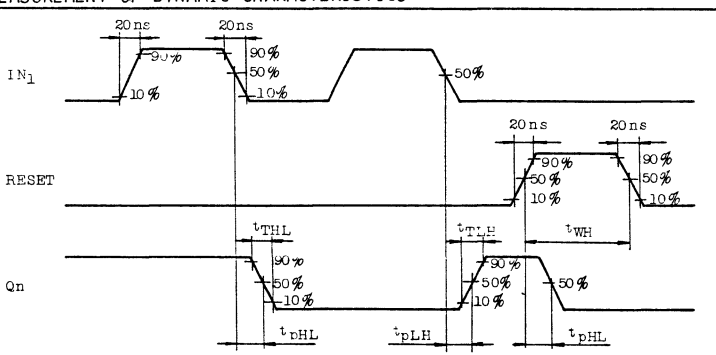
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		V_{IN}=V_{SS}, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		V_{IN}=V_{SS}, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		V_{IN}=V_{SS}, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		V_{IN}=V_{SS}, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	μA
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD}	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
		*	15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, $V_{SS1}=V_{SS2}=0V$, $V_{DD1}=V_{DD2}$, $C_L=50pF$)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (IN2 - Q18)	t_{pLH} t_{pHL}		5	-	1.8	9.0	μs
			10	-	0.6	3.5	
			15	-	0.4	2.7	
Propagation Delay Time (IN2 - Q24)	t_{pLH} t_{pHL}		5	-	1.9	12	
			10	-	0.7	4.5	
			15	-	0.5	3.5	
Propagation Delay Time (RESET - Qn)	t_{pHL}		5	-	250	2600	ns
			10	-	100	1000	
			15	-	65	750	
Max. Clock Frequency	f_{CL}		5	3	10	-	MHz
			10	6	25	-	
			15	8	30	-	
Max. Clock Input Rise Time	t_{rCL}		5	20	-	-	μs
			10	5	-	-	
Max. Clock Input Fall Time	t_{fCL}		15	4	-	-	
Min. Clock Pulse Width	t_W		5	-	50	385	ns
			10	-	20	150	
			15	-	15	120	
Min. Pulse Width (RESET)	t_{WH}		5	-	100	1400	
			10	-	40	600	
			15	-	30	450	
Input Capacitance	C_{IN}			-	5	7.5	pF

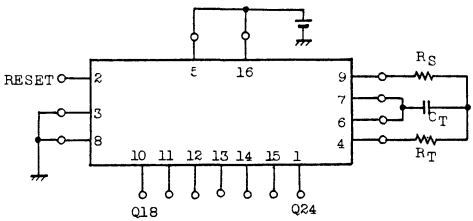
WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



TC4521BP

APPLICATION CIRCUIT

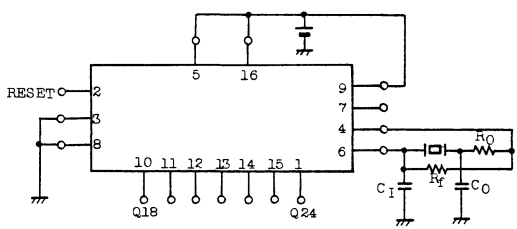
☆ When CR oscillation is used as time reference



$R_S \geqq 2\ R_T$

$f_{OSC} \fallingdotseq \frac{1}{2.2 R_T C_T}$

☆ When crystal oscillation circuit is used as the time reference



Typical data

X'tal (Hz)	C_I, C_O (pF)	R_O (Ω)
32.768k	15 ※	500k ※
100k	60	50k
1M	50～55	1k
4.194304M	15	0

R_f = 1～10MΩ

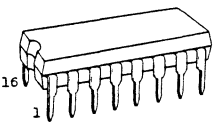
※ : A CASE OF LESS THAN V_{DD}=10V

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

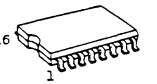
TC4522BP
TC4526BP/BF

TC4522BP PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (BCD)
TC4526BP/TC4526BF PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (Binary)

TC4522BP, TC4526BP/BF is a 4-bit, synchronus, dwon counter having clear, preset and inhibit function. The counting operation of each counter is made at the rising edge of CLOCK. The counter can advance its counting operation at the falling edge of INHIBIT input by setting the CLOCK input to "H" level. The programmable frequency division circuit can be formed by using the PRESET ENABLE input. Also the circuit can be expanded by means of cascade connection by use of the CASCADE FEEDBACK input and "0" output. (Refer to application circuit). This counter is suitable to programmable frequency-dividers, synthesizers, etc.



DIP16 (3D16A-P)

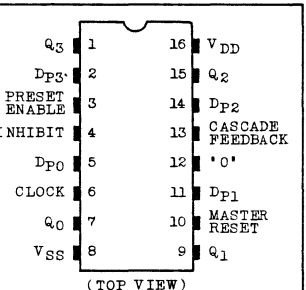


MFP16 (F16GC-P)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40~85	°C
Storage Temperature Range	T_{stg}	-65~150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

(TC4522BP, TC4526BP/BF)

CLOCK	INHIBIT	PRESET ENABLE	MASTER RESET	ACTION
L	*	L	L	NO COUNT
↓	L	L	L	COUNT
*	H	L	L	NO COUNT
H	↑	L	L	COUNT
*	*	H	L	PRESET
*	*	*	H	RESET

* Don't Care

(TC4522BP)

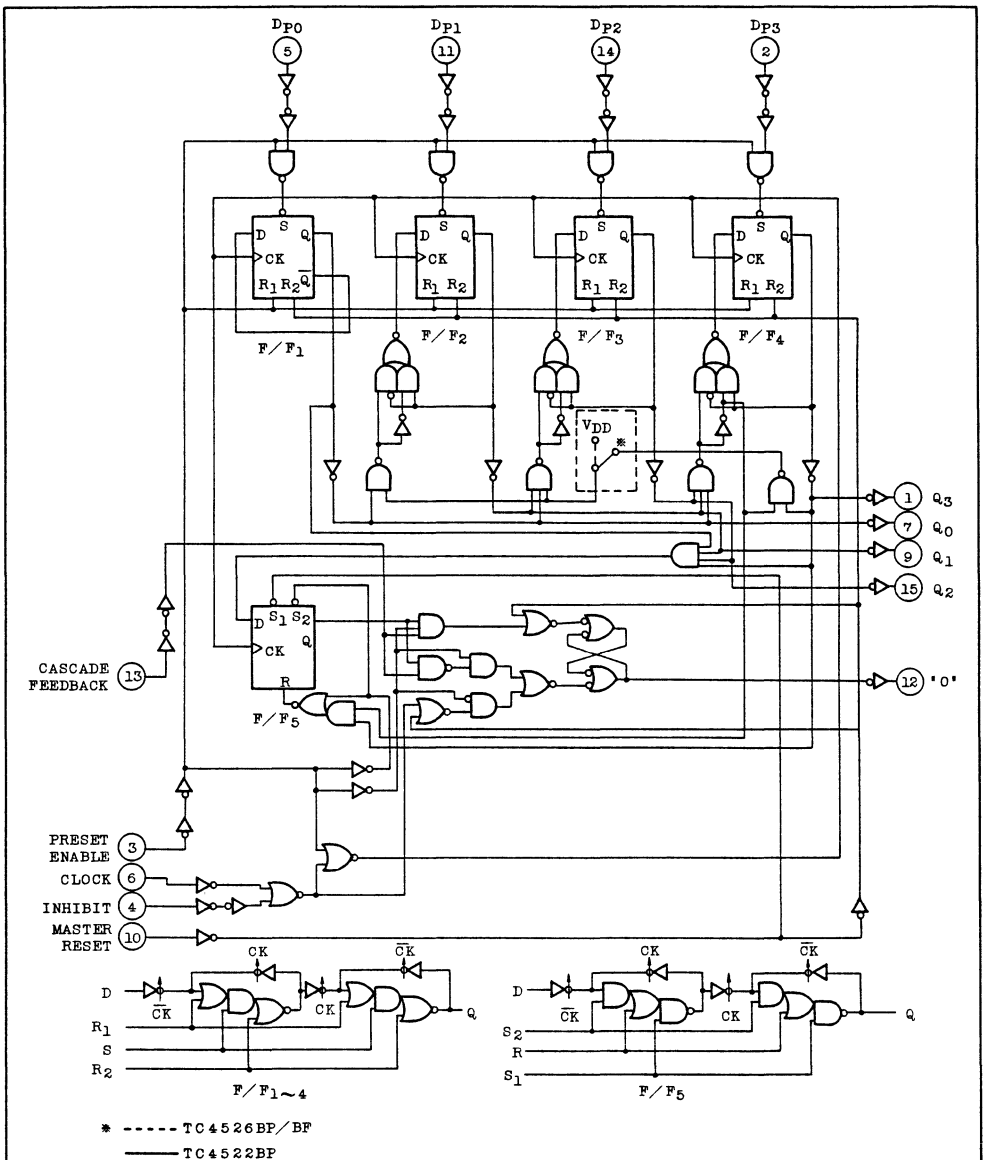
Count	Q_0	Q_1	Q_2	Q_3
9	H	L	L	H
8	L	L	L	H
7	H	H	H	L
6	L	H	H	L
5	H	L	H	L
4	L	L	H	L
3	H	H	L	L
2	L	H	L	L
1	H	L	L	L
0	L	L	L	L

(TC4526BP/BF)

Count	Q_0	Q_1	Q_2	Q_3
15	H	H	H	H
14	L	H	H	H
13	H	L	H	H
12	L	L	H	H
11	H	H	L	H
10	L	H	L	H
9	H	L	L	H
8	L	L	L	H
7	H	H	H	L
6	L	H	H	L
5	H	L	H	L
4	L	L	H	L
3	H	H	L	L
2	L	H	L	L
1	H	L	L	L
0	L	L	L	L

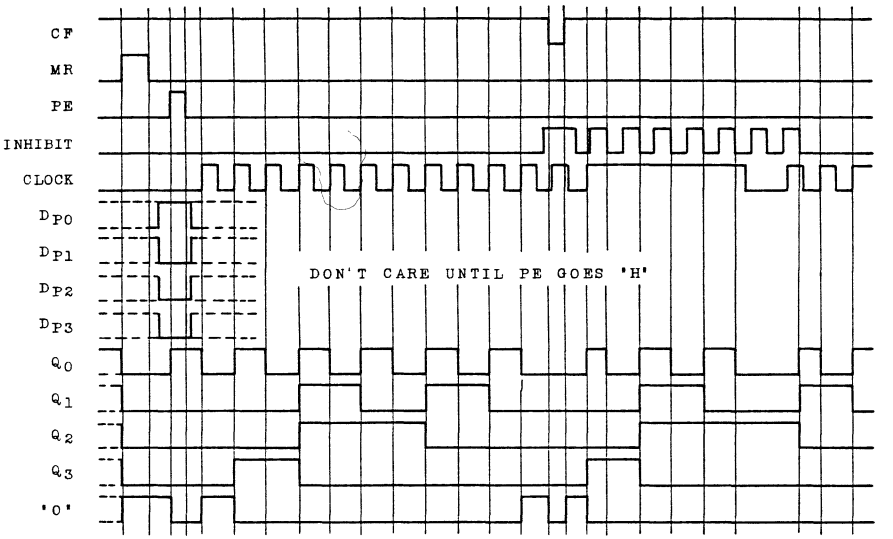
TC4522BP, TC4526BP/BF

LOGIC DIAGRAM

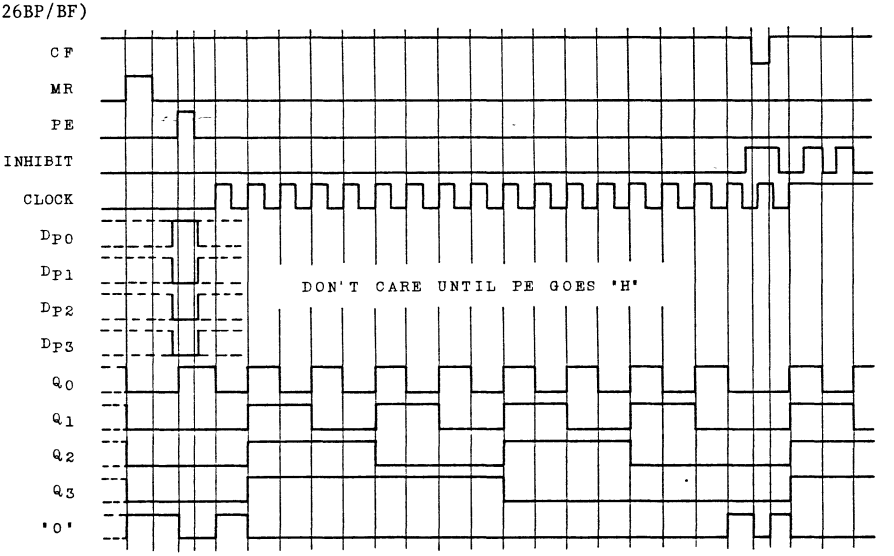


TIMING CHART

(TC4522BP)



(TC4526BP/BF)



TC4522BP, TC4526BP/BF

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	0.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

TC4522BP, TC4526BP/BF

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK, INHIBIT - Q_n)	t_{pLH} t_{pHL}		5	-	450	1100	ns
			10	-	170	450	
			15	-	120	320	
Propagation Delay Time (CLOCK - "0")	t_{pLH} t_{pHL}		5	-	500	1100	
			10	-	190	450	
			15	-	130	320	
Propagation Delay Time (PE - Q_n)	t_{pLH} t_{pHL}		5	-	470	1100	
			10	-	190	450	
			15	-	130	320	
Propagation Delay Time (D_{pn} - Q_n)	t_{pLH} t_{pHL}		5	-	280	1100	
			10	-	120	450	
			15	-	80	320	
Propagation Delay Time (RESET - Q_n)	t_{pHL}		5	-	430	1100	
			10	-	170	450	
			15	-	125	320	
Propagation Delay Time (CF - "0")	t_{pLH} t_{pHL}		5	-	160	480	
			10	-	100	260	
			15	-	70	200	

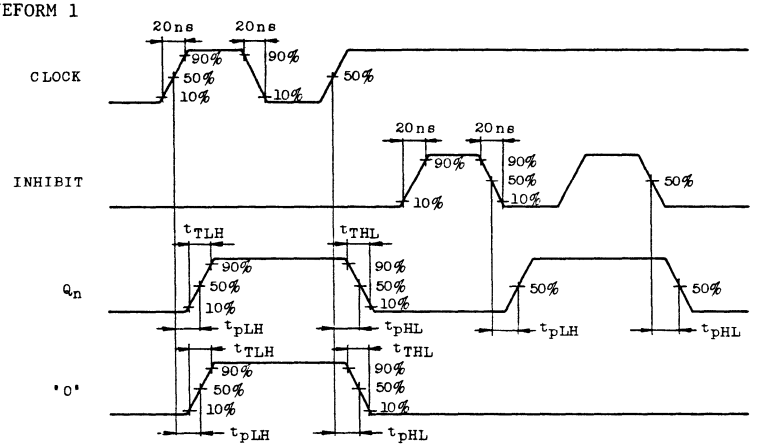
TC4522BP, TC4526BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

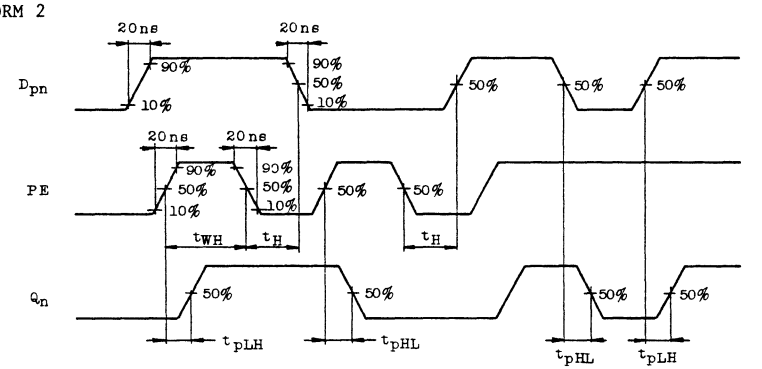
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Max. Clock Frequency	f_{CL}		5	1.0	2	-	MHz
			10	3.0	6	-	
			15	4.0	9	-	
Max. Clock Input Rise/ Fall Time	t_{rCL} t_{fCL}		5	20	-	-	μs
			10	2.5	-	-	
			15	1.0	-	-	
Max. Input Rise/ Fall Time (INHIBIT)	t_r t_f		5	20	-	-	
			10	2.5	-	-	
			15	1.0	-	-	
Min. Clock Pulse Width	t_W		5	-	250	500	ns
			10	-	85	170	
			15	-	55	110	
Min. Pulse Width (PRESET ENABLE)	t_{WH}		5	-	330	660	
			10	-	140	280	
			15	-	100	200	
Min. Pulse Width (RESET)	t_{WH}		5	-	270	540	
			10	-	110	250	
			15	-	80	200	
Min. Hold Time (D_{pn} -P_E)	t_H		5	-	30	150	ns
			10	-	20	50	
			15	-	15	40	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

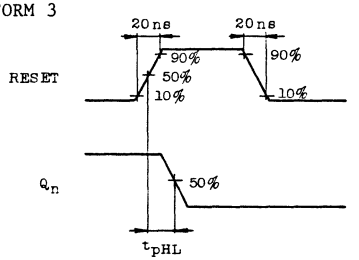
WAVEFORM 1



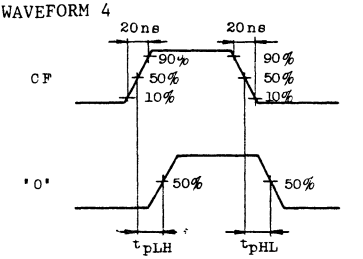
WAVEFORM 2



WAVEFORM 3

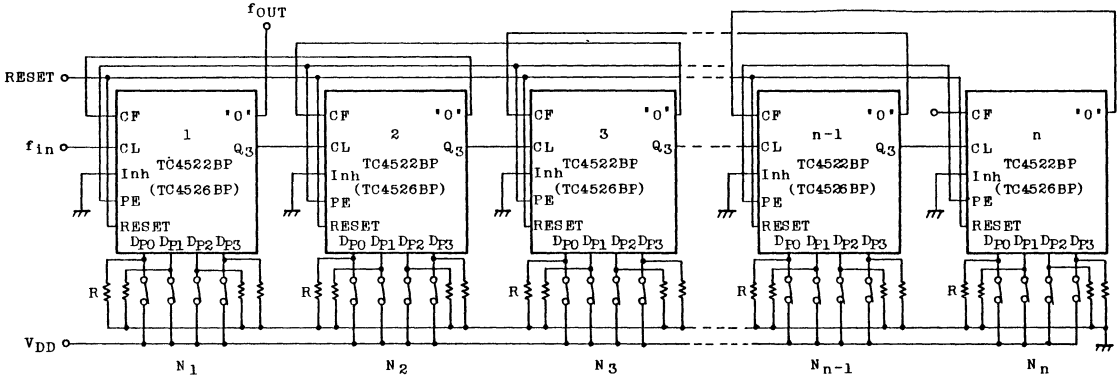


WAVEFORM 4



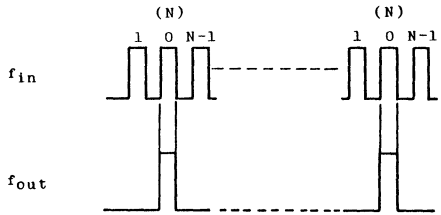
APPLICATION CIRCUIT

N-STAGE PROGRAMMABLE FREQUENCY DIVIDER



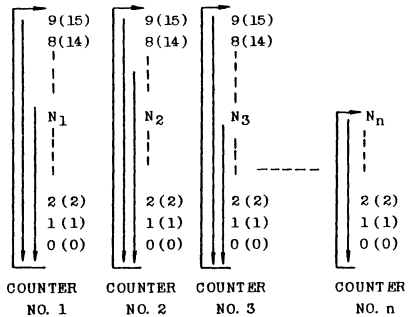
R : 10kΩ ~ 100kΩ

TIMING CHART



$$f_{out} = \frac{f_{in}}{N}, \quad N \neq 0$$

COUNTING CYCLE

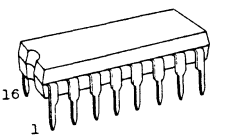


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4527BP

TC4527BP BCD RATE MULTIPLIER

TC4527BP is BCD rate multiplier from which arbitrary number of output pulses determined by BCD inputs (A_{IN} through D_{IN}) can be obtained by supplying ten clock inputs.
For example, setting BCD input to "7" (A = B = C = "H" and D = "L"), if ten counting pulses are applied to CLOCK input, seven pulses are output to OUT ($\overline{OUT}$) terminals. Usually, when used alone, $\overline{ENABLE}$, STROBE AND CASCADE inputs are kept at "L" level but when used in the cascade connection, refer to the example of applications.
Besides of its original purpose of arithmetic circuits, this TC4527BP can be utilized for digital filters, frequency synthesizers and programmable pulse generators.

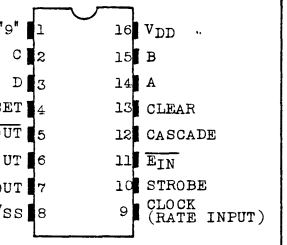


DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

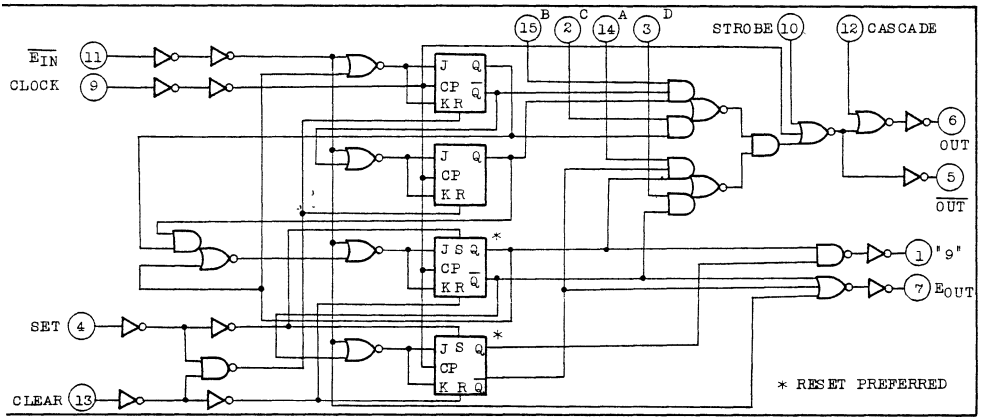
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input Voltage	V_{IN}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output Voltage	V_{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ∼ 85	°C
Storage Temperature Range	T_{stg}	-65 ∼ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



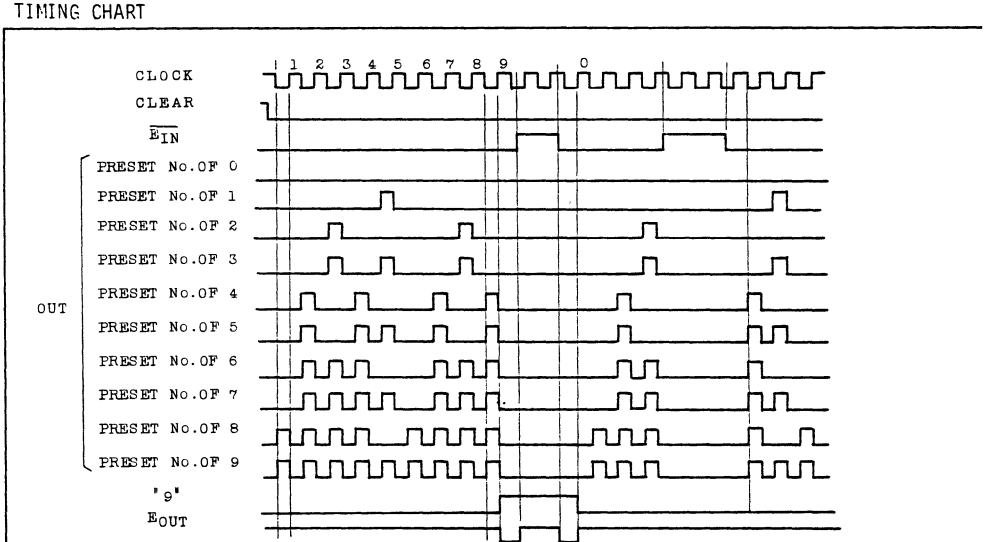
TC4527BP

TRUTH TABLE

INPUTS										OUTPUTS			
D	C	B	A	NO. OF CLOCK PULSES	$\overline{E_{IN}}$	STROBE	CASCADE	CLEAR	SET	OUT	$\overline{OUT}$	"9"	E_{OUT}
L	L	L	L	10	L	L	L	L	L	L	H	1	1
L	L	L	H	10	L	L	L	L	L	1	1	1	1
L	L	H	L	10	L	L	L	L	L	2	2	1	1
L	L	H	H	10	L	L	L	L	L	3	3	1	1
L	H	L	L	10	L	L	L	L	L	4	4	1	1
L	H	L	H	10	L	L	L	L	L	5	5	1	1
L	H	H	L	10	L	L	L	L	L	6	6	1	1
L	H	H	H	10	L	L	L	L	L	7	7	1	1
H	L	L	L	10	L	L	L	L	L	8	8	1	1
H	L	L	H	10	L	L	L	L	L	9	9	1	1
H	L	H	L	10	L	L	L	L	L	8	8	1	1
H	L	H	H	10	L	L	L	L	L	9	9	1	1
H	H	L	L	10	L	L	L	L	L	8	8	1	1
H	H	L	H	10	L	L	L	L	L	9	9	1	1
H	H	H	L	10	L	L	L	L	L	8	8	1	1
H	H	H	H	10	L	L	L	L	L	9	9	1	1
*	*	*	*	10	H	L	L	L	L	▲	▲	▲	H
*	*	*	*	10	L	H	L	L	L	L	H	1	1
*	*	*	*	10	L	L	H	L	L	H	▲	1	1
H	*	*	*	10	L	L	L	H	L	10	10	L	H
L	*	*	*	10	L	L	L	H	L	L	H	L	H
*	*	*	*	10	L	L	L	L	H	L	H	H	L

* DON'T CARE ▲ UNDETERMINED 1~10 : NO OF PULSES

TIMING CHART



TC4527BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}$, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}$, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V V_{OUT}=1.5V,13.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V VOUT=1.5V,13.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			10	-	3.0	-	4.5	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

TC4527BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - OUT)	t_{pLH} t_{pHL}		5	-	230	460	
			10	-	95	190	
			15	-	70	140	
Propagation Delay Time (CLOCK - $\overline{OUT}$)	t_{pLH} t_{pHL}		5	-	190	380	
			10	-	80	160	
			15	-	60	120	
Propagation Delay Time (CLOCK - E_{OUT})	t_{pLH} t_{pHL}		5	-	340	680	
			10	-	140	280	
			15	-	100	200	
Propagation Delay Time (CLOCK - "9")	t_{pLH} t_{pHL}		5	-	260	600	
			10	-	150	300	
			15	-	100	200	
Propagation Delay Time (STROBE - OUT)	t_{pLH} t_{pHL}		5	-	150	300	
			10	-	65	150	
			15	-	55	120	
Propagation Delay Time (CASCADE - OUT)	t_{pLH} t_{pHL}		5	-	95	190	
			10	-	45	90	
			15	-	30	70	
Propagation Delay Time (SET, CLEAR - OUT)	t_{pLH} t_{pHL}		5	-	320	660	
			10	-	130	300	
			15	-	100	220	
Propagation Delay Time ($\overline{E_{IN}}$ - E_{OUT})	t_{pLH} t_{pHL}		5	-	140	280	
			10	-	60	120	
			15	-	50	100	
Max. Clock Frequency	f_{CL}		5	1.0	2	-	MHz
			10	2.5	6	-	
			15	3.5	8	-	
Max. Clock Input Rise Time Max. Clock Input Fall Time	t_{rCL} t_{fCL}		5	20	-	-	μs
			10	15	-	-	
			15	15	-	-	
Min. Clock Pulse Width	t_w		5	-	250	500	ns
			10	-	85	170	
			15	-	60	100	
Min. Pulse Width (SET, CLEAR)	t_{WH}		5	-	110	220	
			10	-	45	90	
			15	-	35	70	

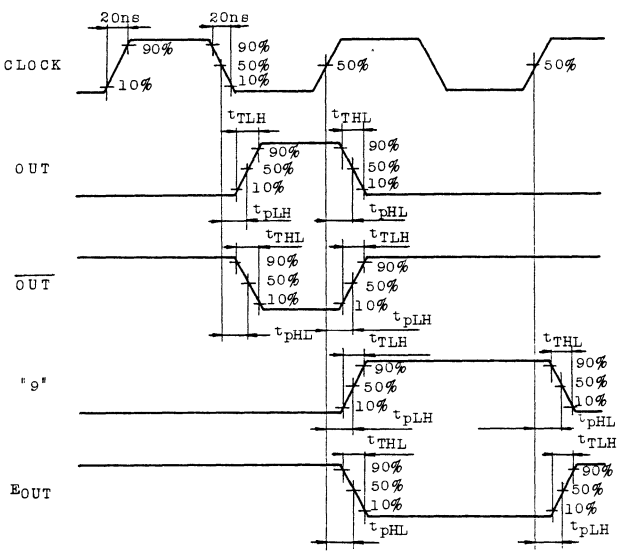
TC4527BP

YNAMIC ELECTRICAL CHARACTERISTICS (Continued)

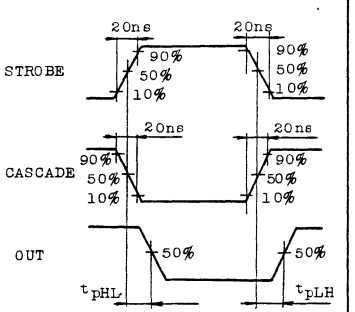
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{CC}(V)	MIN.	TYP.	MAX.	UNITS
Min. Set-up Time ($\overline{E_{IN}}$ - CLOCK)	t_{SU}		5	-	160	320	ns
			10	-	60	120	
			15	-	50	100	
Min. Removal Time ($\overline{E_{IN}}$ - CLOCK)	t_{rem}		5	-	120	240	
			10	-	45	130	
			15	-	25	110	
Min. Removal Time (SET - CLOCK)	t_{rem}		5	-	-50	0	
			10	-	-20	0	
			15	-	-10	0	
Min. Removal Time (CLEAR - CLOCK)	t_{rem}		5	-	-35	60	
			10	-	-15	40	
			15	-	-10	30	
Input Capacitance	C_{IN}			-	5	7.5	pF

AVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

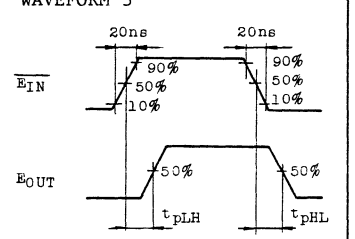
WAVEFORM 1



WAVEFORM 2



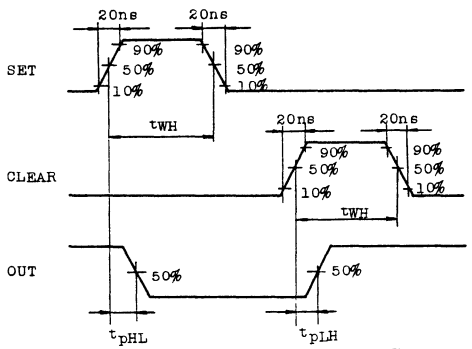
WAVEFORM 3



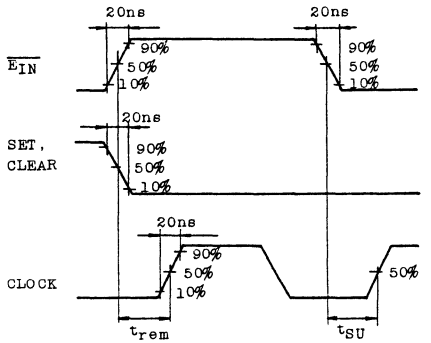
TC4527BP

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 4

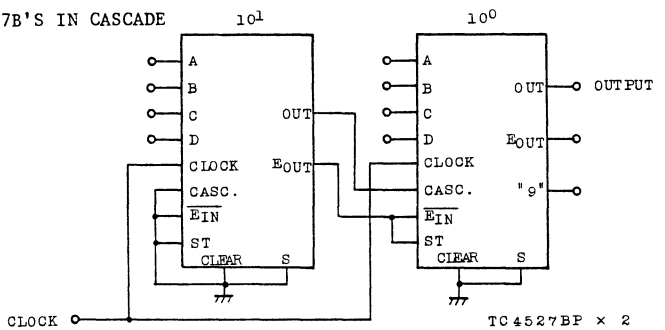


WAVEFORM 5



APPLICATION CIRCUIT

TWO TC4527B'S IN CASCADE

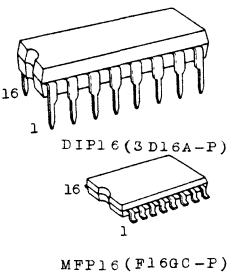


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4528BP/BF

:4528BP/TC4528BF DUAL MONOSTABLE MULTIVIBRATOR

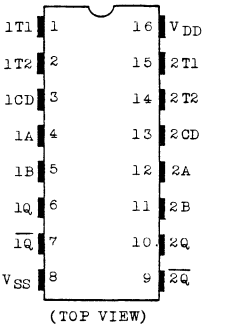
TC4528BP/BF contains two circuits of monostable
ıltivibrators with the capabilities of retrigger
eration and reset operation in one chip.
e trigger operation can be achieved either by rising
ge or falling edge if one of two inputs A and B are
lected. As the pulse width of mono-stable multi-
brator output is determined by the time constant of
:ternal resistor (Rx) and external capacitor (Cx),
de range of output pulse width can be obtained.
e asynchronous reset operation from outside can be
hieved by setting CD input to "L" level, and this CD
put can be also applied for inhibiting the trigger
eration and for shortening the time period from
rning the power on the time when TC4528B becomes
le to perform the mono-stable operation.



SOLUTE MAXIMUM RATINGS

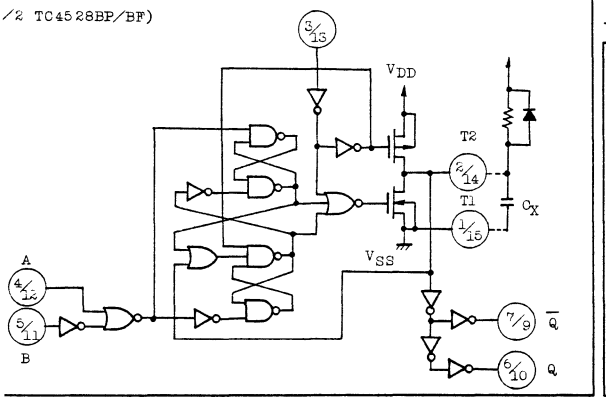
CHARACTERISTIC	SYMBOL	RATING	UNITS
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
put Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
tput Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	±10	mA
wer Dissipation	P_D	300(DIP)/180(MFP)	mW
erating Temperature Range	T_A	-40 ∿ 85	°C
orage Temperature Range	T_{stg}	-65 ∿ 150	°C
ad Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



GIC DIAGRAM

/2 TC4528BP/BF)



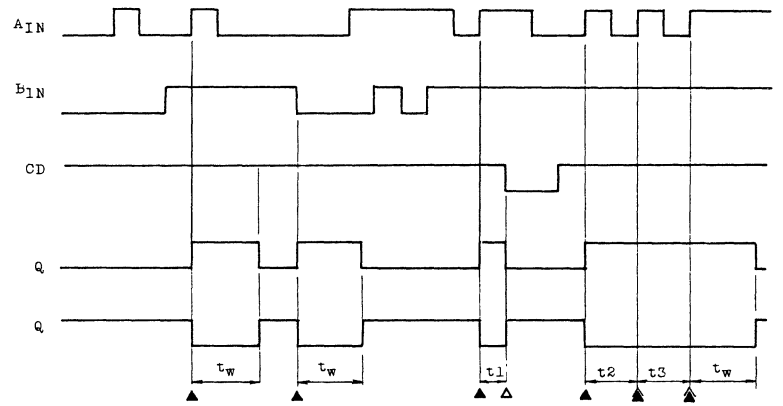
TRUTH TABLE

INPUT			OUTPUT		NOTE
A	B	CD	Q	$\overline{Q}$	
↓	H	L	⎍	⎎	OUTPUT PULSE
↓	L	H	L	H	INHIBIT
H	↑	H	L	H	INHIBIT
L	↑	H	⎍	⎎	OUTPUT PULSE
※	※	L	L	H	INHIBIT

※ Don't Care

TC4528BP/BF

TIMING CHART



▲ : TRIGGER
▲ : RETRIGGER
△ : RESET

t_w : $(C_X > 001\mu F)$ $t_w = \{ 02 + 015 \frac{(V_{DD}-V_{SS})}{5} \} \cdot R_X C_X$

t1, t2, t3 : $t1, t2, t3 < t_w$

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
External Resistance	R_X		5	-	1000	kΩ
External Capacitance	C_X		No Limits			μF

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS}$, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS}$, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V V_{OH}=2.5V V_{OH}=9.5V V_{OH}=13.5V	5	-0.2	-	-0.61		-	-0.12	-	mA
			5	-	-	-		-	-	-	
			10	-0.5	-	-0.4		-	-0.3	-	
		$V_{IN}=V_{SS}$, V_{DD}	15	-1.4	-	-1.2		-	-1.0	-	

TATIC ELECTRICAL CHARACTERISTICS (Continued)

HARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
utput Low Current	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	mA
		V_{OL}=0.5V V_{OL}=1.5V	10	1.3	-	1.1		-	0.9	-	
		V_{IN}=V_{SS}, V_{DD}	15	3.6	-	3.0		-	2.4	-	
nput High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.5V,13.5V	10	7.0	-	7.0	5.5	-	7.0	-	
		$\|I_{OUT}\|$<1μA	15	11.0	-	11.0	8.25	-	11.0	-	
nput Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.5V,13.5V	10	-	3.0	-	4.5	3.0	-	3.0	
		$\|I_{OUT}\|$<1μA	15	-	4.0	-	6.75	4.0	-	4.0	
nput "H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
urrent "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
uiescent evice Current	I_{DD}	V_{IN}=V_{SS}, V_{DD}	5	-	20	-	0.005	20	-	150	μA
			10	-	40	-	0.010	40	-	300	
		*	15	-	80	-	0.015	80	-	600	

All valid input combinations.

/NAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

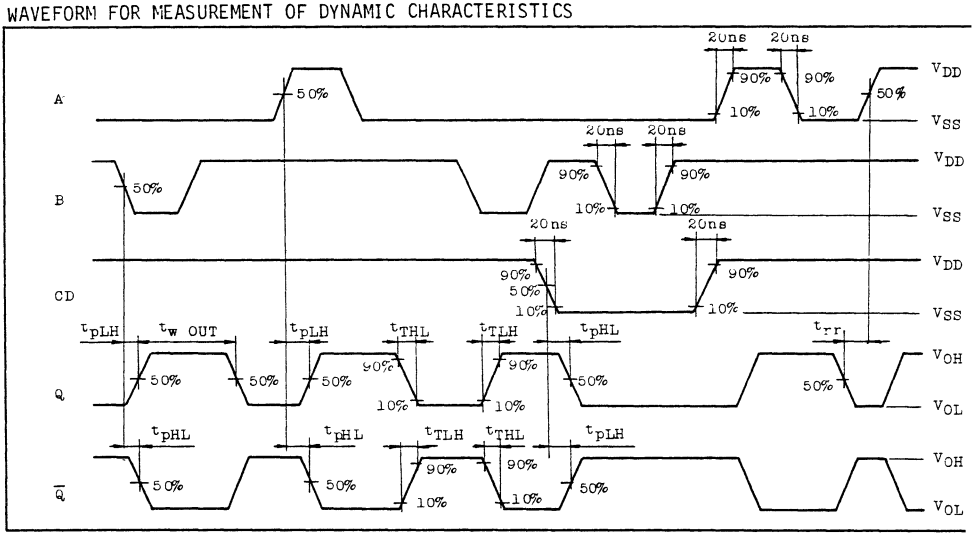
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
itput Transition Time (Low to High)	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
itput Transition Time (High to Low)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
opagation Delay Time (A, B - Q, $\overline{Q}$)	t_{pLH}	R_X=5kΩ C_X=15pF	5	-	850	1600	
			10	-	300	600	
			15	-	200	400	
opagation Delay Time (A, B - Q, $\overline{Q}$)	t_{pHL}	R_X=5kΩ C_X=15pF	5	-	850	1600	
			10	-	300	600	
			15	-	200	400	
opagation Delay Time (A, B - Q, $\overline{Q}$)	t_{pLH}	R_X=10kΩ C_X=10000pF	5	-	6.0	12	μs
			10	-	2.0	5	
			15	-	1.3	3	
opagation Delay Time (A, B - Q, $\overline{Q}$)	t_{pHL}	R_X=10kΩ C_X=10000pF	5	-	6.0	12	
			10	-	2.0	5	
			15	-	1.3	3	

TC4528BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Continued)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (CD - Q, $\overline{Q}$)	t_{pLH} t_{pHL}	R_X=5kΩ C_X=15pF	5	-	600	1200	ns
			10	-	210	500	
			15	-	160	400	
Propagation Delay Time (CD - Q, $\overline{Q}$)	t_{pLH} t_{pHL}	R_X=10kΩ C_X=10000pF	5	-	5.5	-	μs
			10	-	4.6	-	
			15	-	4.0	-	
Min. Input Pulse Width (A, B)	t_{WH} t_{WL}	R_X=5kΩ C_X=15pF	5	-	130	450	ns
			10	-	65	200	
			15	-	60	150	
Min. Retrigger Time	t_{rr}	R_X=5kΩ C_X=15pF	5	-	0	-	
			10	-	0	-	
			15	-	0	-	
Min. Retrigger Time	t_{rr}	R_X=10kΩ C_X=10000pF	5	-	0	-	
			10	-	0	-	
			15	-	0	-	
Output Pulse Width	$t_{w\ OUT}$	R_X=5kΩ C_X=15pF	5	-	450	-	
			10	-	450	-	
			15	-	450	-	
Output Pulse Width	$t_{w\ OUT}$	R_X=10kΩ C_X=10000pF	5	15	35	55	μs
			10	25	50	75	
			15	40	65	90	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

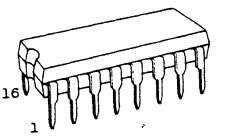


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4530BP

C4530BP DUAL 5-INPUT MAJORITY LOGIC GATE

The TC4530BP is dual 5-input majority logic gate. Each majority logic gate decides whether or not the input at "H" level is more than that at "L" level. The polarity of decision output Z can be selected by using control input W.

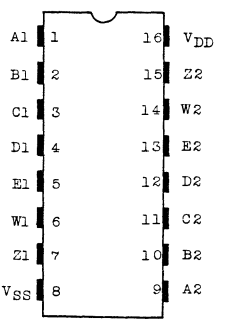


DIP16(3D16A-P)

BSOLUTE MAXIMUM RATINGS

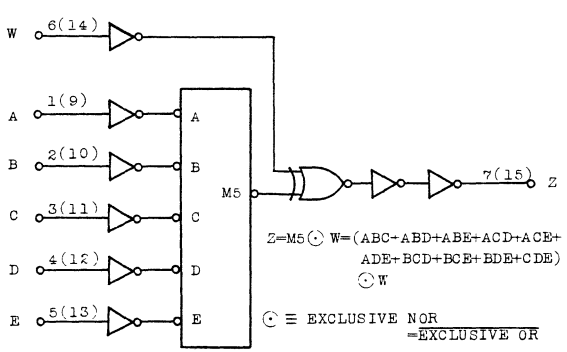
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
put Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
tput Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	±10	mA
wer Dissipation	P_D	300	mW
erating mperature Range	T_A	-40 ~ 85	°C
orage mperature Range	T_{stg}	-65 ~ 150	°C
ad Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



Z=M5 ⊙ W=(ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE) ⊙ W

⊙ ≡ EXCLUSIVE NOR
=EXCLUSIVE OR

TRUTH TABLE

INPUTS A B C D E	W	OUTPUT Z
IF ANY THREE OR MORE OF A,B,C,D AND E INPUT ARE AT "L".	L	H
	H	L
IF ANY THREE OR MORE OF A,B,C,D AND E INPUT ARE AT "L".	L	L
	H	H

TC4530BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}$, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}$, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\|$<1μA	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V VOUT=1.5V,13.5V $\|I_{OUT}\|$<1μA	5	-	1.5	-	2.25	1.5	-	1.5	
			10	-	3.0	-	4.5	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD} *	5	-	1	-	0.001	1	-	7.5	μA
			10	-	2	-	0.001	2	-	15	
			15	-	4	-	0.002	4	-	30	

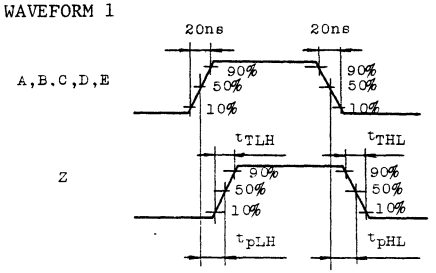
* All valid input combinations.

)YNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

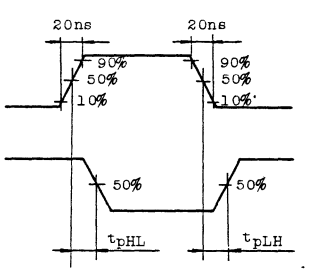
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (D - Z)	t_{pLH}		5	-	240	960	
			15	-	100	400	
	t_{pHL}		15	-	70	300	
Propagation Dealy Time (A, B, C, D, E - Z)	t_{pLH}		5	-	150	640	
			10	-	60	300	
	t_{pHL}		15	-	40	210	
Propagation Dealy Time (W - Z)	t_{pLH}		5	-	100	575	
			10	-	50	265	
	t_{pHL}		15	-	40	190	
Input Capacitance	C_{IN}			-	5	7.5	pF

\AVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1



WAVEFORM 2

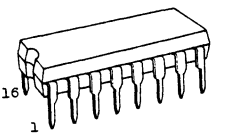


TC4531BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4531BP 12-BIT PARITY TREE

TC4531BP is 12 bit parity tree consisting of 12 exclusive OR gates.
When ODD/EVEN input is set to "L", "H" level is output if the parity of data inputs (D0 through D11) is odd and when ODD/EVEN input is set to "H", "H" level is output if the parity of data inputs is even.
This has wide range of applications such as generating the parity code of n bits data and detecting parity errors.

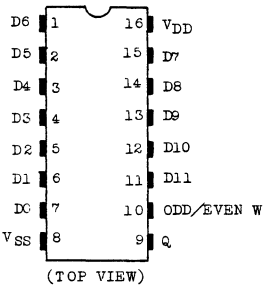


DIP16 (3D16A-P)

ABSOLUTE MAXIMUM RATINGS

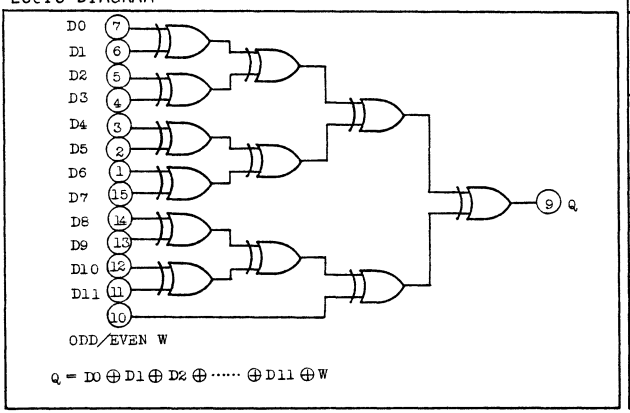
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



$Q = D0 \oplus D1 \oplus D2 \oplus \cdots\cdots \oplus D11 \oplus W$

TRUTH TABLE

IN							*	OU
W	D11	D10	···	D2	D1	D0	D·E	Q
L	L	L	···	L	L	L	0	L
L	L	L	···	L	L	H	1	H
L	L	L	···	L	H	L	2	H
L	L	L	···	L	H	H	3	L
L	L	L	···	H	L	L	4	H
L	L	L	···	H	L	H	5	L
L	L	L	···	H	H	L	6	L
L	L	L	···	H	H	H	7	H
:	:	:	···	:	:	:	:	:
H	H	H	···	L	L	L	8184	L
H	H	H	···	L	L	H	8185	H
H	H	H	···	L	H	L	8186	H
H	H	H	···	L	H	H	8187	L
H	H	H	···	H	L	L	8188	H
H	H	H	···	H	L	H	8189	L
H	H	H	···	H	H	L	8190	L
H	H	H	···	H	H	H	8191	H

* D·E = DECIMAL EQUIVALENT

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA, $V_{IN}=V_{SS}$, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA, $V_{IN}=V_{SS}$, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		VOUT=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		VOUT=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
		*	15	-	20	-	0.015	20	-	600	

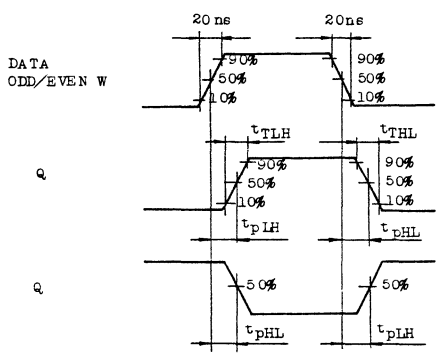
* All valid input combinations.

TC4531BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (DATA - Q)	t_{pLH}		5	-	320	1320	
	t_{pHL}		10	-	120	525	
			15	-	80	360	
Propagation Delay Time (ODD/EVEN W - Q)	t_{pLH}		5	-	210	750	
	t_{pHL}		10	-	80	300	
			15	-	60	210	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

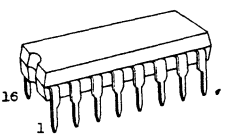
TC4532BP

TC4532BP 8-BIT PRIORITY ENCODER

TC4532BP is eight bit encoder which detects "H" level of the highest order among eight input signals and outputs the corresponding signal position in binary code.

The inputs are eight input signals of D0 through D7 and E_{IN}, and when E_{IN} is set to "L" level, the encode operation is inhibited making all the outputs at "L" level.

The encoded output appears on three signal lines Q0 through Q2 in binary. E_{OUT} and G_S are the outputs to indicate the operational mode of encoder and used when the number of bits is to be increased by cascade connection.

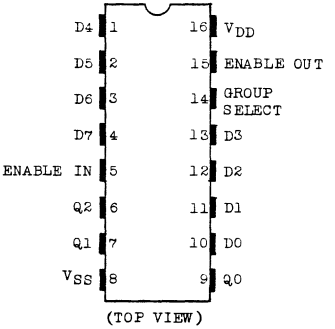


DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

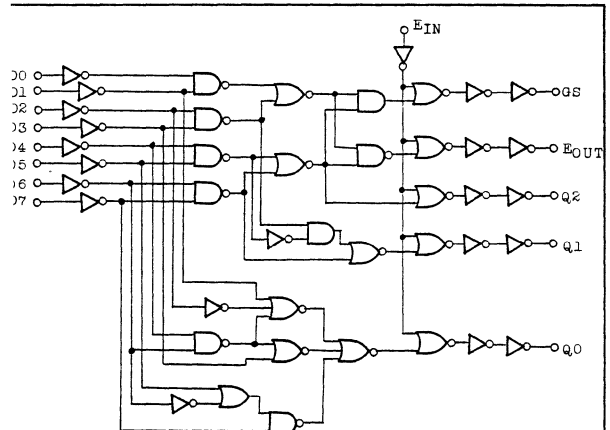
CHARACTERISTIC	SYMBOL	RATING	UNITS
DC Supply Voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input Voltage	V_{IN}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output Voltage	V_{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ∿ 85	°C
Storage Temperature Range	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TRUTH TABLE

INPUT									OUTPUT				
E_{IN}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_{OUT}
L	*	*	*	*	*	*	*	*	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	L	L	H
H	H	*	*	*	*	*	*	*	H	H	H	H	L
H	L	H	*	*	*	*	*	*	H	H	H	L	L
H	L	L	H	*	*	*	*	*	H	H	L	H	L
H	L	L	L	H	*	*	*	*	H	H	L	L	L
H	L	L	L	L	H	*	*	*	H	L	H	H	L
H	L	L	L	L	L	H	*	*	H	L	H	L	L
H	L	L	L	L	L	L	H	*	H	L	L	H	L
H	L	L	L	L	L	L	L	H	H	L	L	L	L

* Don't Care

TC4532BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS}, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS}, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		V_{IN}=V_{SS}, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		V_{IN}=V_{SS}, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

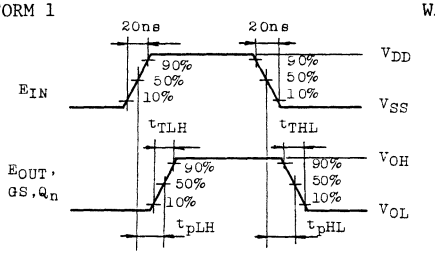
* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

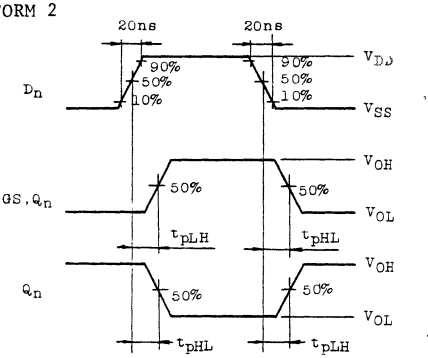
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (E_{IN} - E_{OUT})	t_{pLH} t_{pHL}		5	-	140	280	
			10	-	60	120	
			15	-	45	90	
Propagation Delay Time (E_{IN} - GS)	t_{pLH} t_{pHL}		5	-	150	300	
			10	-	65	130	
			15	-	50	100	
Propagation Delay Time (E_{IN} - Qn)	t_{pLH} t_{pHL}		5	-	150	340	
			10	-	60	170	
			15	-	45	125	
Propagation Delay Time (Dn - Qn)	t_{pLH} t_{pHL}		5	-	270	540	
			10	-	90	220	
			15	-	65	160	
Propagation Delay Time (Dn - GS)	t_{pLH} t_{pHL}		5	-	200	400	
			10	-	90	180	
			15	-	70	140	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1



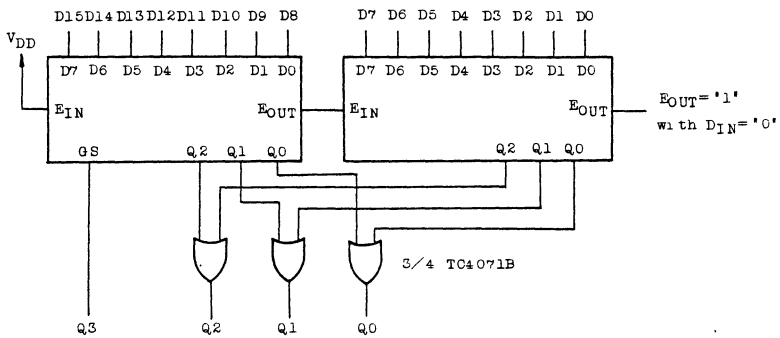
WAVEFORM 2



TC4532BP

APPLICATION CIRCUIT

Two TC4532B's Cascaded for 4-Bit Output



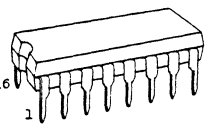
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4538BP/BF

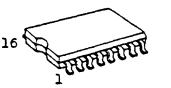
TC4538BP/TC4538BF DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

The TC4538BP/BF is the retriggerable/resettable monostable multivibrator and the trigger operation can be made at either the leading or trailing edge by 2 inputs of A and B. Since the output monostable pulse width is decided by time constant of the external resistor (R_X) and the external capacitor (C_X), it becomes possible to set a broad range of output pulse widths.
Further, since the pin connection and function are compatible with the TC4528B, the substitution is possible.

FEATURE:
t_{wOUT}=10ms±5% (at R_X=100kΩ, C_X=0.1μF, V_{DD}=10V)



DIP16 (3D16A-P)

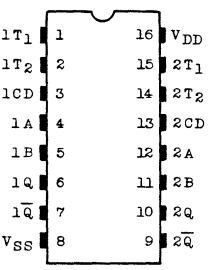


MFP16 (F16GC-P)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

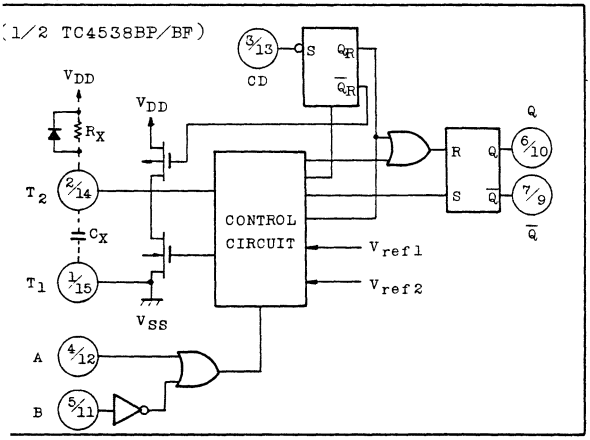
PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM

(1/2 TC4538BP/BF)



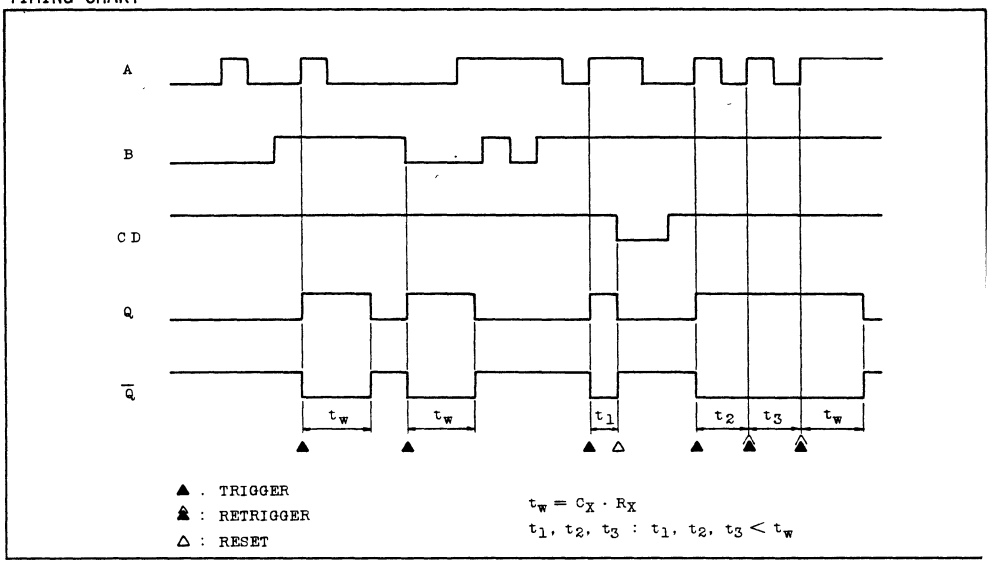
TRUTH TABLE

INPUT			OUTPUT		NOTE
A	B	CD	Q	Q̄	
↓	H	H	⎍	⎎	OUTPUT ENABLE
↓	L	H	L	H	INHIBIT
H	↑	H	L	H	INHIBIT
L	↑	H	⎍	⎎	OUTPUT ENABLE
*	*	L	L	H	INHIBIT

* Don't Care

TC4538BP/BF

TIMING CHART



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
External Resistance	R_X		5	-	1000	kΩ
External Capacitance	C_X		No Limits			μF

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		V_{IN}=V_{SS},V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		V_{IN}=V_{SS},V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS},V_{DD} ※	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

※ All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	

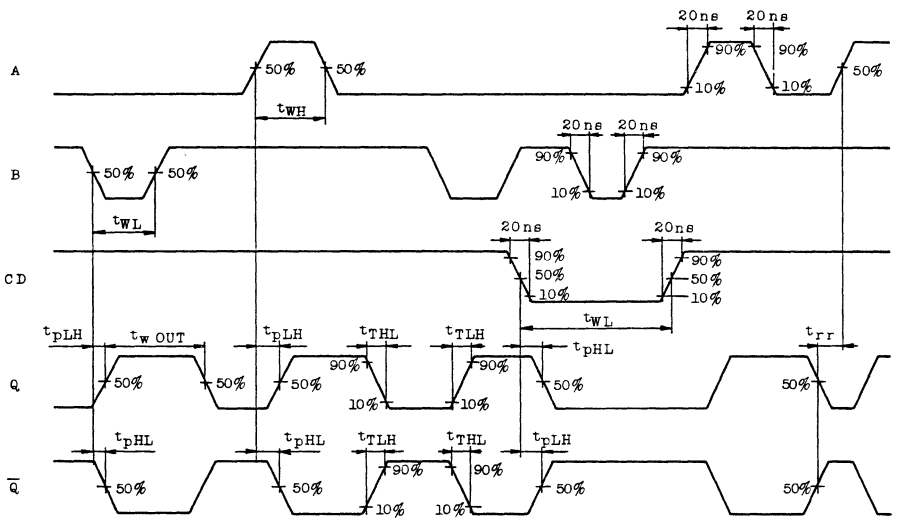
TC4538BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (A,B - Q,$\overline{Q}$)	t_{pLH} t_{pHL}		5	-	380	760	ns
			10	-	150	300	
			15	-	100	220	
Propagation Delay Time (CD - Q,$\overline{Q}$)	t_{pLH} t_{pHL}		5	-	280	560	
			10	-	110	250	
			15	-	75	190	
Min. Input Pulse Width (A, B)	t_{WH} t_{WL}		5	-	60	120	ns
			10	-	30	60	
			15	-	25	50	
Min. Pulse Width (CD)	t_{WL}		5	-	95	190	
			10	-	45	90	
			15	-	35	70	
Min. Retrigger Time	t_{rr}		5	-	0	-	ns
			10	-	0	-	
			15	-	0	-	
Output Pulse Width	t_{w} OUT	R_X=100kΩ C_X=0.002μF	5	-	206	-	μs
			10	-	204	-	
			15	-	205	-	
		R_X=100kΩ C_X=0.1μF	5	9.3	9.95	10.4	ms
			10	9.5	10	10.5	
			15	9.55	10.05	10.65	
		R_X=100kΩ C_X=10μF	5	-	0.98	-	s
			10	-	1.00	-	
			15	-	1.01	-	
Pulse Width Match between circuits in the same package	Δt_{wOUT}	$\frac{t_{w(Q2)} - t_{w(Q1)}}{t_{w(Q1)}} \times 100$	5	-	±1	-	%
			10	-	±1	-	
			15	-	±1	-	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM



TC4539BP/BF

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

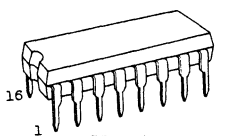
TC4539BP/TC4539BF DUAL 4-CHANNEL DATA SELECTOR/MULTIPLEXER

TC4539BP/BF contains two circuits of data selectors which select data according to common address inputs A and B.

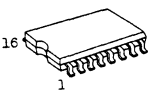
Four channel data X0 through X3 are selected to be output Z according to inputs A and B and four channel data Y0 through Y3 are selected by the same A and B to generate output W.

When input St (ST') is set at "H", the output becomes "L" regardless other inputs.

This can be widely applied in composition of signals, parallel to serial conversion and selection of signals.



DIP16(3D16A-P)

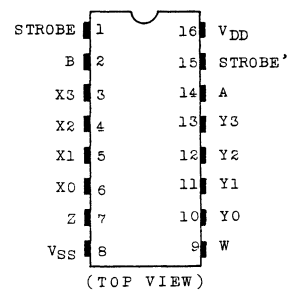


MFP16(F16GC-P)

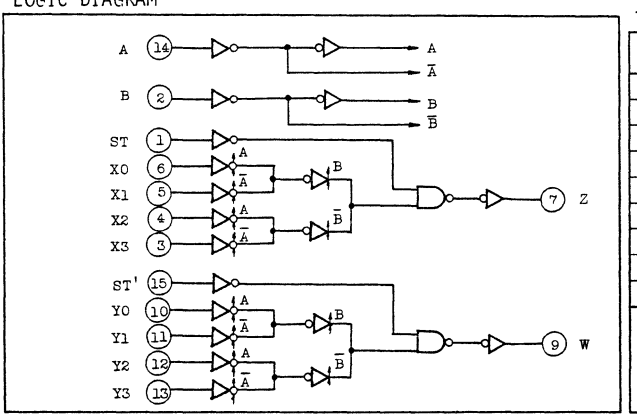
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ∼ 85	°C
Storage Temperature Range	T_{stg}	-65 ∼ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

A	B	ST ST'	X0 Y0	X1 Y1	X2 Y2	X3 Y3	Z W
*	*	H	*	*	*	*	L
L	L	L	L	*	*	*	L
L	L	L	H	*	*	*	H
H	L	L	*	L	*	*	L
H	L	L	*	H	*	*	H
L	H	L	*	*	L	*	L
L	H	L	*	*	H	*	H
H	H	L	*	*	*	L	L
H	H	L	*	*	*	H	H

* . DON'T CARE

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}$, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}$, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\|$<1μA	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V VOUT=1.5V,13.5V $\|I_{OUT}\|$<1μA	5	-	1.5	-	2.25	1.5	-	1.5	
			10	-	3.0	-	5.5	3.0	-	3.0	
			15	-	4.0	-	8.25	4.0	-	4.0	
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD} *	5	-	5	-	0.001	5	-	150	μA
			10	-	10	-	0.002	10	-	300	
			15	-	20	-	0.004	20	-	600	

* All valid input combinations.

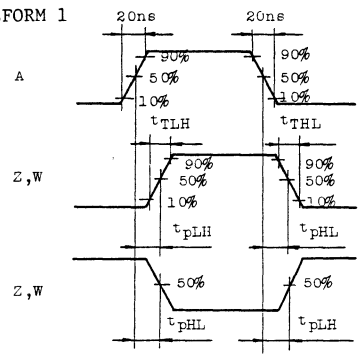
TC4539BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

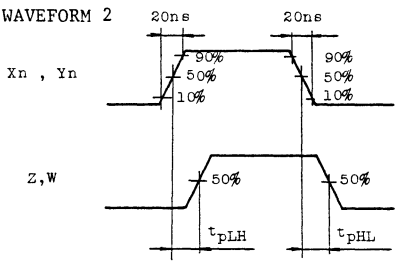
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (A - Z, W)	t_{pLH} t_{pHL}		5	-	150	450	
			10	-	60	220	
			15	-	40	170	
Propagation Delay Time (Xn, Yn - Z, W)	t_{pLH} t_{pHL}		5	-	130	420	
			10	-	60	180	
			15	-	40	140	
Propagation Delay Time (STROBE - Z, W)	t_{pLH} t_{pHL}		5	-	85	290	
			10	-	40	150	
			15	-	30	120	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

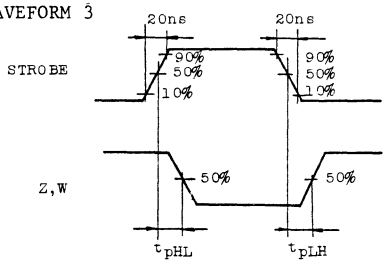
WAVEFORM 1



WAVEFORM 2



WAVEFORM 3



C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4543BP/BF

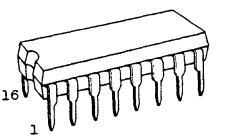
TC4543BP/TC4543BF BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER (For Liquid Crystals)

TC4543BP/BF is 7 segment latch/decoder/driver which can directly drive field effect type liquid crystal display element (FEM type) and equipped with BLANKING input, PHASE input and LATCH DISABLE input.

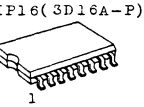
If erroneous BCD code is input, and when BI is "H", all the outputs are blanked.

When FEM type liquid crystal is driven, common pulse should be applied to the back plane of display element and the PHASE input of TC4543BP/BF.

When LED display element is to be driven, drivers should be added to the outputs.



DIP16(3D16A-P)

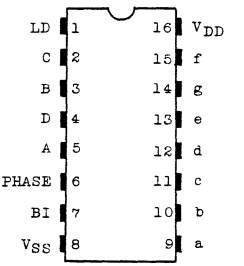


MFP16(F16GC-P)

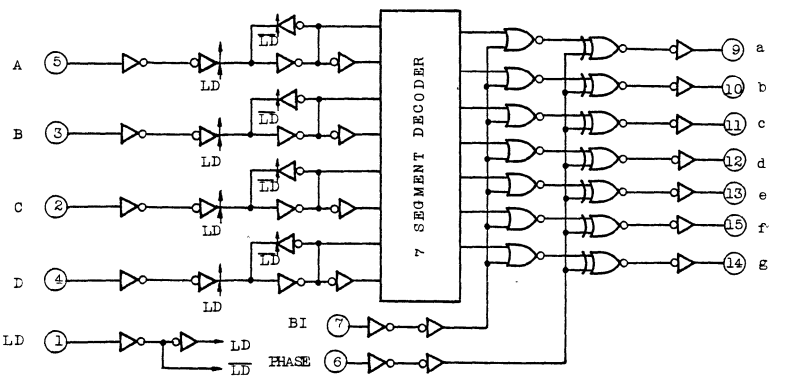
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ∿ 85	°C
Storage Temperature Range	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



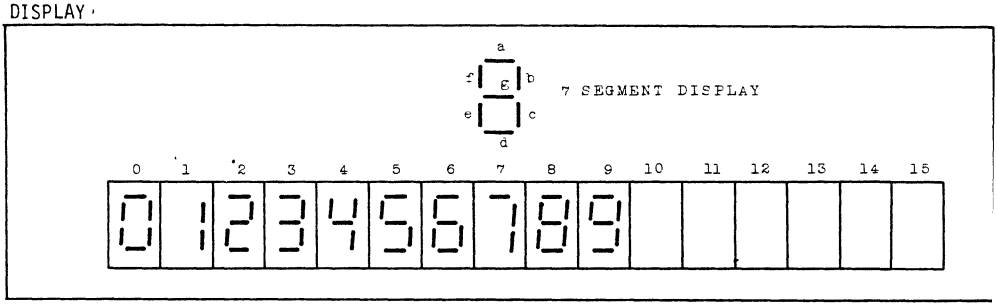
TC4543BP/BF

TRUTH TABLE

INPUTS							OUTPUTS							DISPLAY	NOTE
LD	BI	PHASE	A	B	C	D	a	b	c	d	e	f	g		
*	H	H	*	*	*	*	H	H	H	H	H	H	H	BLANK	
*	H	L	*	*	*	*	L	L	L	L	L	L	L	BLANK	
L	L	H	*	*	*	*	LATCH								
L	L	L	*	*	*	*	LATCH								
H	L	H	L	L	L	L	L	L	L	L	L	L	H	0	
H	L	H	H	L	L	L	H	L	L	H	H	H	H	1	
H	L	H	L	H	L	L	L	L	H	L	L	H	L	2	
H	L	H	H	H	L	L	L	L	L	L	H	H	L	3	
H	L	H	L	L	H	L	H	L	L	H	H	L	L	4	
H	L	H	H	L	H	L	L	H	L	L	H	L	L	5	
H	L	H	L	H	H	L	L	H	L	L	L	L	L	6	
H	L	H	H	H	H	L	L	L	L	H	H	H	H	7	
H	L	H	L	L	L	H	L	L	L	L	L	L	L	8	
H	L	H	H	L	L	H	L	L	L	L	H	L	L	9	
H	L	H	L	H	L	H	H	H	H	H	H	H	H	BLANK	
H	L	H	H	H	L	H	H	H	H	H	H	H	H	BLANK	
H	L	H	L	L	H	H	H	H	H	H	H	H	H	BLANK	
H	L	H	H	L	H	H	H	H	H	H	H	H	H	BLANK	
H	L	H	L	H	H	H	H	H	H	H	H	H	H	BLANK	
H	L	H	H	H	H	H	H	H	H	H	H	H	H	BLANK	
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0	
H	L	L	H	L	L	L	L	H	H	L	L	L	L	1	
H	L	L	L	H	L	L	H	H	L	H	H	L	H	2	
H	L	L	H	H	L	L	H	H	H	H	L	L	H	3	
H	L	L	L	L	H	L	L	H	H	L	L	H	H	4	
H	L	L	H	L	H	L	H	L	H	H	L	H	H	5	
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6	
H	L	L	H	H	H	L	H	H	H	L	L	L	L	7	
H	L	L	L	L	L	H	H	H	H	H	H	H	H	8	
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9	
H	L	L	L	H	L	H	L	L	L	L	L	L	L	BLANK	
H	L	L	H	H	L	H	L	L	L	L	L	L	L	BLANK	
H	L	L	L	L	H	H	L	L	L	L	L	L	L	BLANK	
H	L	L	H	L	H	H	L	L	L	L	L	L	L	BLANK	
H	L	L	L	H	H	H	L	L	L	L	L	L	L	BLANK	
H	L	L	H	H	H	H	L	L	L	L	L	L	L	BLANK	

* : DON'T CARE

DISPLAY



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		V_{IN}=V_{SS}, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		V_{IN}=V_{SS}, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	mA
		V_{OH}=2.5V	5	-	-	-		-	-	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V	15	-1.4	-	-1.2		-	-1.0	-	
		V_{IN}=V_{SS}, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V	15	3.6	-	3.0		-	2.4	-	
		V_{IN}=V_{SS}, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|$<1μA									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|$<1μA									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD}	5	-	20	-	0.005	20	-	150	μA
			10	-	40	-	0.010	40	-	300	
		*	15	-	80	-	0.015	80	-	600	

All valid input combinations.

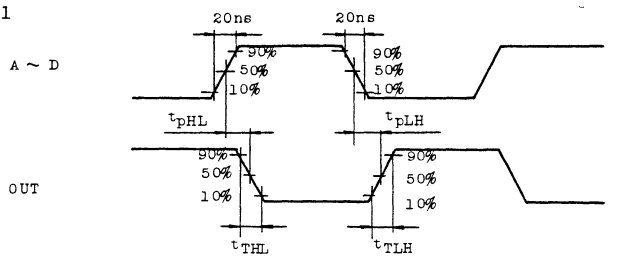
TC4543BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

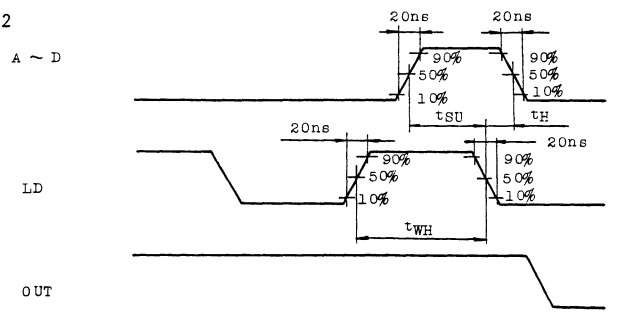
CHARACTERISTICS	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Transition Time (High to Low)	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (A∿D - OUT)	t_{pLH}		5	-	650	1650	
			10	-	230	660	
			15	-	160	495	
Propagation Delay Time (A∿D - OUT)	t_{pHL}		5	-	800	1650	
			10	-	300	660	
			15	-	200	495	
Propagation Delay Time (BI - OUT)	t_{pLH}		5	-	550	1200	
			10	-	200	600	
			15	-	180	400	
Propagation Delay Time (BI - OUT)	t_{pHL}		5	-	450	1200	
			10	-	160	600	
			15	-	115	400	
Propagation Delay Time (PHASE - OUT)	t_{pLH}		5	-	750	1600	
			10	-	330	700	
			15	-	230	480	
Propagation Delay Time (PHASE - OUT)	t_{pHL}		5	-	580	1600	
			10	-	220	700	
			15	-	150	480	
Min. Pulse Width (LD)	t_{WH}		5	-	-	500	
			10	-	-	200	
			15	-	-	150	
Min. Set-up Time (LD - A∿D)	t_{SU}		5	-	-	100	
			10	-	-	50	
			15	-	-	30	
Min. Hold Time (LD - A∿D)	t_H		5	-	-	120	
			10	-	-	60	
			15	-	-	40	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

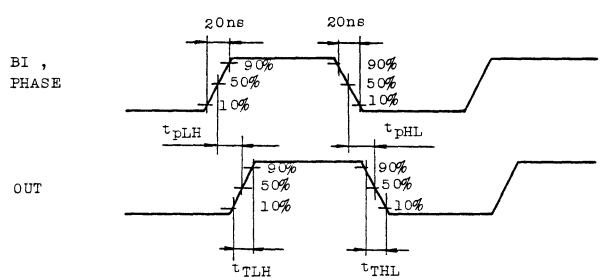
WAVEFORM 1



WAVEFORM 2



WAVEFORM 3

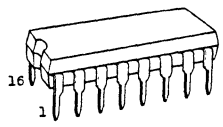


TC4555BP
TC4556BP/BF

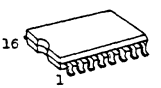
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4555BP DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER (Active High Outputs)
TC4556BP/TC4556BF DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER (Active Low Outputs)

TC4555BP and TC4556BP/BF contain two circuits of decoders/multiplexers.
When $\overline{\text{ENABLE}}$="L", arbitrary one of four outputs is selected by two binary inputs A and B.
The selected output is "H" for TC4555BP and "L" for TC4556BP/BF.
When $\overline{\text{ENABLE}}$ is set to "H", the selection is inhibited making all the output at "L" for TC4555BP and "H" for TC4556BP/BF.



DIP16 (3D16A-P)

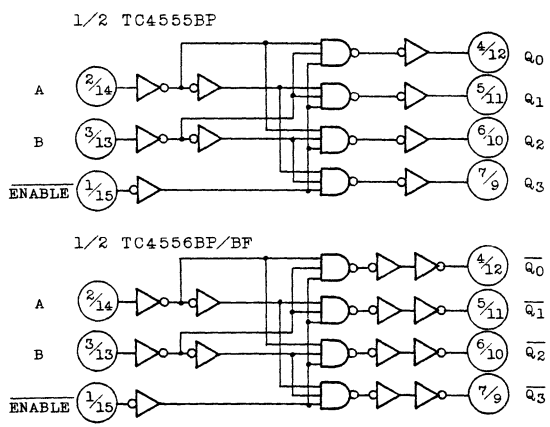


MFP16 (F16GC-P)

ABSOLUTE MAXIMUM RATINGS

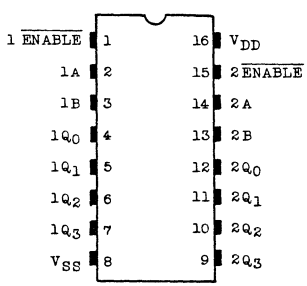
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

LOGIC DIAGRAM

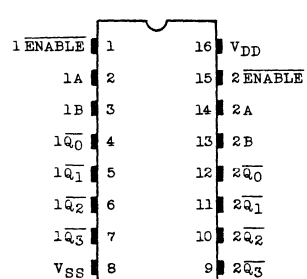


PIN ASSIGNMENT

TC4555BP



TC4556BP/BF



(TOP VIEW)

TC4555BP, TC4556BP/BF

TRUTH TABLE

INPUTS			OUTPUTS TC4555BP				OUTPUTS TC4556BP/BF				
$\overline{E}$	B	A	Q_3	Q_2	Q_1	Q_0	$\overline{Q}_3$	$\overline{Q}_2$	$\overline{Q}_1$	$\overline{Q}_0$	
L	L	L	L	L	L	H	H	H	H	L	
L	L	H	L	L	H	L	H	H	L	H	
L	H	L	L	H	L	L	H	L	H	H	
L	H	H	H	L	L	L	L	H	H	H	
H	*	*	L	L	L	L	H	H	H	H	

*: Don't Care

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\| < 1\mu A$									

TC4555BP, TC4556BP/BF

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	V
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V, 13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|$<1μA									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	4.0	-	0.002	4.0	-	30	μA
				10	-	8.0	-	0.004	8.0	-	60	
				15	-	16.0	-	0.008	16.0	-	120	

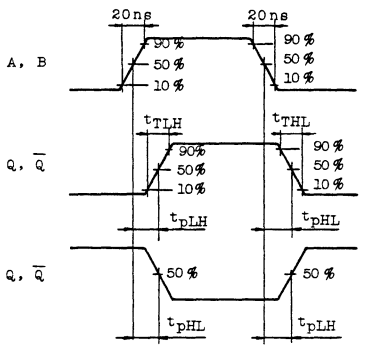
* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

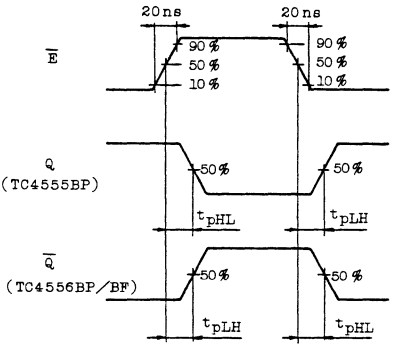
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (A,B - Q,$\overline{Q}$)	t_{pLH} t_{pHL}		5	-	140	440	ns
			10	-	65	190	
			15	-	50	140	
Propagation Delay Time ($\overline{E}$ - Q,$\overline{Q}$)	t_{pLH} t_{pHL}		5	-	110	400	
			10	-	45	170	
			15	-	40	130	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1



WAVEFORM 2

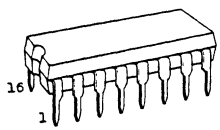


TC4560BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4560BP NBCD ADDER

TC4560BP is NBCD (natural BCD) adder which adds two binary coded decimal numbers (BCD code).
The sum of BCD inputs applied to four data input lines (A_1 through A_4) and another set of four data input lines (B_1 through B_4) and carry input C_{IN} from the lower order digit is output to S_1 through S_4 in the same BCD code.
When the sum is 10 or larger, "H" level is output to carry output C_{OUT}. When the sum is smaller than 10, C_{OUT} is kept at "L" level. By connecting with TC4561BP (9's complementer), the add/subtract circuit can be easily obtained.

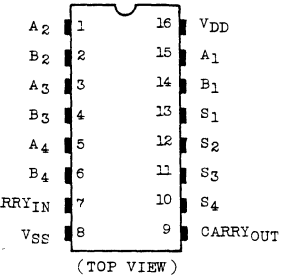


DIP 16 (3D16A-P)

ABSOLUTE MAXIMUM RATINGS

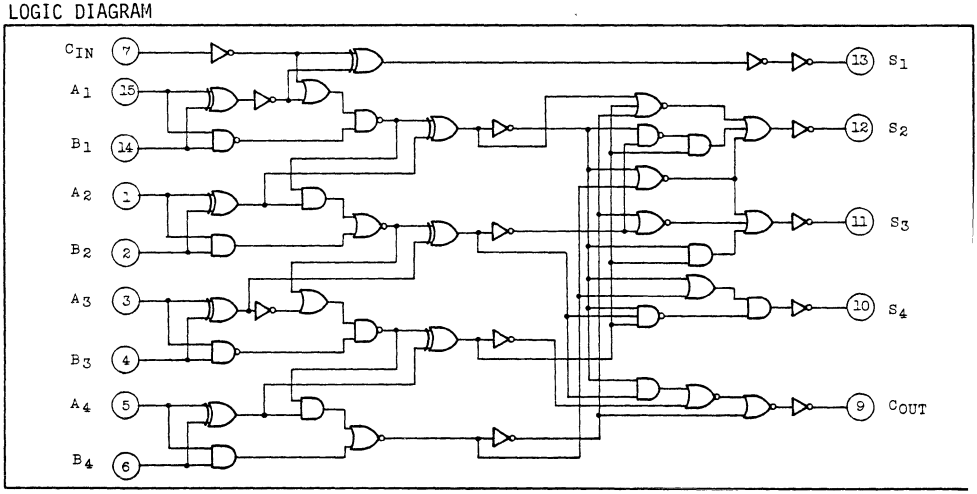
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



RUTH TABLE

INPUTS									OUTPUTS				
A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	C_{IN}	S_4	S_3	S_2	S_1	C_{OUT}
L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	H	L	L	L	H	L
L	H	L	H	L	L	H	L	L	L	H	H	H	L
L	H	L	L	L	L	H	H	H	H	L	L	L	L
L	H	H	L	L	H	L	H	L	L	L	L	H	H
L	L	H	H	H	L	L	L	H	L	L	H	L	H
H	L	L	H	L	H	L	L	L	L	L	H	H	H
L	H	L	H	H	L	L	L	H	L	H	L	L	H
H	L	L	H	H	L	L	H	H	H	L	L	H	H

COMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
put Voltage	V_{IN}		0	-	V_{DD}	V

ATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

HARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
gh-Level tput Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
w-Level tput Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
tput High rrent	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
tput Low rrent	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									

TC4560BP

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\| < 1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\| < 1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
				10	-	10	-	0.010	10	-	300	
				15	-	20	-	0.015	20	-	600	

* All valid input combinations.

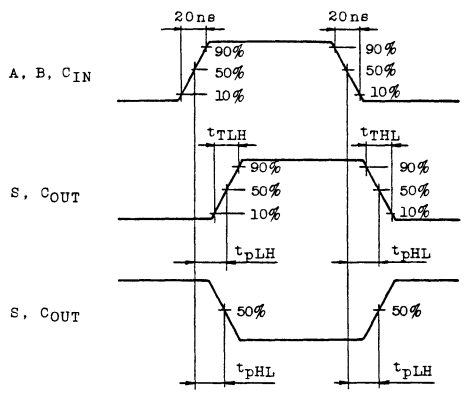
DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (A,B - S)	t_{pLH} t_{pHL}		5	-	660	2100	ns
			10	-	250	900	
			15	-	170	675	
Propagation Delay Time (A,B - C_{OUT})	t_{pLH} t_{pHL}		5	-	500	1800	
			10	-	190	600	
			15	-	130	450	

YNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
ropagation Delay Time (C_{IN} - C_{OUT})	t_{pLH} t_{pHL}		5	-	430	1500	ns
			10	-	160	600	
			15	-	110	450	
ropagation Delay Time (C_{IN} - S)	t_{pLH} t_{pHL}		5	-	550	1800	
			10	-	230	600	
			15	-	160	450	
nput Capacitance	C_{IN}			-	5	7.5	pF

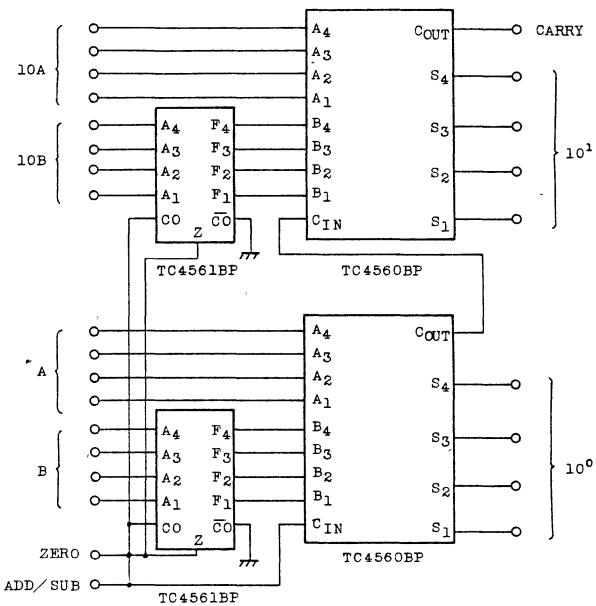
AVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



TC4560BP

APPLICATION CIRCUIT

· PARALLEL ADD/SUBTRACT CIRCUIT



FUNCTION TABLE

ZERO	ADD/SUB	RESULT
L	L	A + B
L	H	A - B
H	*	A

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

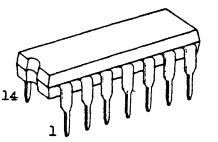
TC4561BP

C4561BP 9's COMPLEMENTER

TC4561BP is 9's complementer which generates 9's complement of BCD signal.

Keeping Z input at "L", if COMP="H" and $\overline{COMP}$="L", 9's complement of input BCD code (A1 through A4) is obtained at outputs F1 through F4. (When the input code is 2, the output will be 7.) If COMP input="L" or $\overline{COMP}$ input="H", the output becomes equal to the input.

If Z="H", outputs F1 through F4 become "L" regardless of other inputs. By connecting with TC4560B, the add/subtract circuit can be easily obtained.

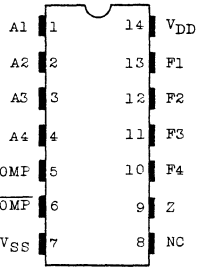


DIP14(3D14A-P)

ABSOLUTE MAXIMUM RATINGS

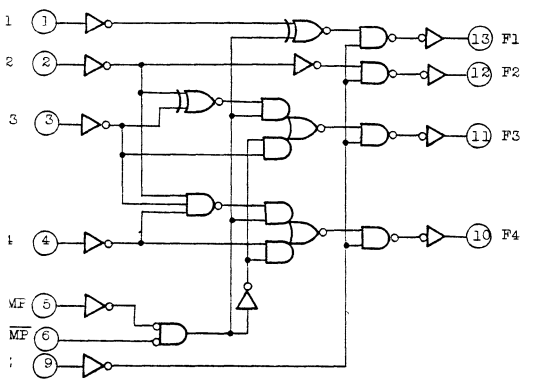
CHARACTERISTIC	SYMBOL	RATING	UNITS
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ∿ 85	°C
Storage Temperature Range	Tstg	-65 ∿ 150	°C
Lead Temp./Time	Tsol	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TRUTH TABLE

Z	COM	$\overline{COM}$	F1	F2	F3	F4	MODE
L	L	※	A1	A2	A3	A4	Fn=An
L	※	H					
L	H	L	$\overline{A1}$	$\overline{A2}$	A2⊕A3	$\overline{A2}\cdot\overline{A3}\cdot\overline{A4}$	COMP
H	※	※	L	L	L	L	ZERO

$A2 \oplus A3 \equiv A2$ (EXCLUSIVE - OR) $A3$
$\equiv A2\cdot\overline{A3}+\overline{A2}\cdot A3$

TC4561BP

TRUTH TABLE (COMPLEMENT MODE: Z, $\overline{COMP}$="L", COM="H")

DECIMAL INPUT CODE	ILLEGAL BCD INPUT CODE	INPUTS A4	A3	A2	A1	DECIMAL OUTPUT CODE	OUTPUTS F4	F3	F2	F1
0		L	L	L	L	9	H	L	L	H
1		L	L	L	H	8	H	L	L	L
2		L	L	H	L	7	L	H	H	H
3		L	L	H	H	6	L	H	H	L
4		L	H	L	L	5	L	H	L	H
5		L	H	L	H	4	L	H	L	L
6		L	H	H	L	3	L	L	H	H
7		L	H	H	H	2	L	L	H	L
8		H	L	L	L	1	L	L	L	H
9		H	L	L	H	0	L	L	L	L
	10	H	L	H	L	7	L	H	H	H
	11	H	L	H	H	6	L	H	H	L
	12	H	H	L	L	5	L	H	L	H
	13	H	H	L	H	4	L	H	L	L
	14	H	H	H	L	3	L	L	H	H
	15	H	H	H	H	2	L	L	H	L

※ DON'T CARE

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNI
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	m
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V, V_{IN}=V_{SS}, V_{DD}	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V, V_{IN}=V_{SS}, V_{DD}	15	4.0	-	3.4	15.0	-	2.8	-	

STATIC ELECTRICAL CHARACTERISTICS (Continued)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V, 13.5V									
			$\|I_{OUT}\|$<1μA	15	11.0	-	11.0	8.25	-	11.0	-	
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V, 13.5V									
			$\|I_{OUT}\|$<1μA	15	-	4.0	-	6.75	4.0	-	4.0	
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	4.0	-	0.002	4.0	-	30	μA
				10	-	8.0	-	0.004	8.0	-	60	
				15	-	16.0	-	0.008	16.0	-	120	

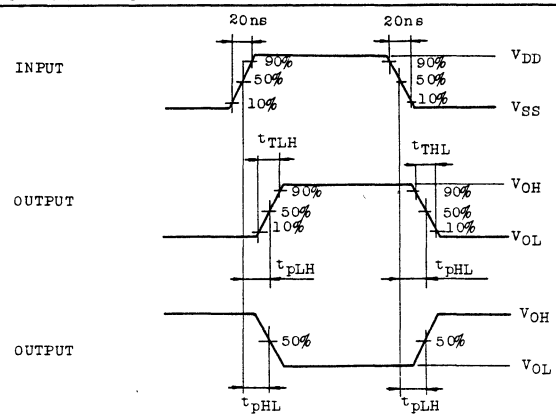
All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (A - F)	t_{pLH}		5	-	220	1000	
	t_{pHL}		10	-	80	400	
			15	-	55	300	
Propagation Delay Time (COMP, $\overline{COMP}$ - F)	t_{pLH}		5	-	230	1000	
	t_{pHL}		10	-	85	400	
			15	-	60	300	
Propagation Delay Time (Z - F)	t_{pLH}		5	-	140	1000	
	t_{pHL}		10	-	50	400	
			15	-	40	300	
Input Capacitance	C_{IN}			-	5	7.5	pF

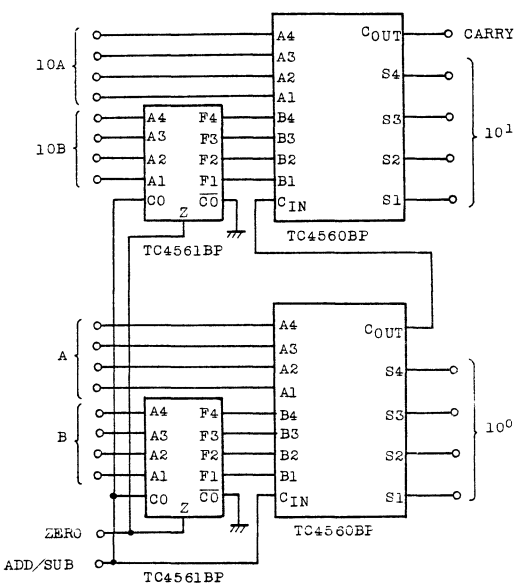
TC4561BP

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



APPLICATION CIRCUIT

• Parallel Add/Subtract Circuit



FUNCTION TABLE

ZERO	ADD/SUB	RESULT
L	L	A + B
L	H	A − B
H	※	A

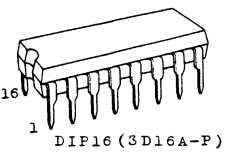
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4572BP/BF

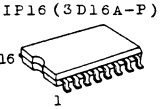
'C4572BP/TC4572BF HEX GATE
(4 INVERTERS Plus 2-Input NOR Gate Plus 2-Input NAND Gate)

TC4572BP/BF is a multiple gate that contains -circuit inverters, 1 circuit 2-input NOR GATE, and . circuit 2-input NAND GATE in one package.

Since each gate is of "B" type equipped with a buffer consisting of 2-stage inverters, it has high noise immunity.



DIP16(3D16A-P)

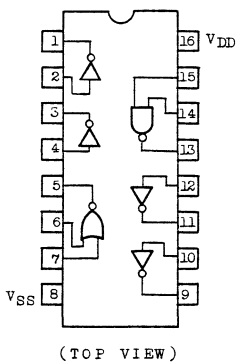


MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

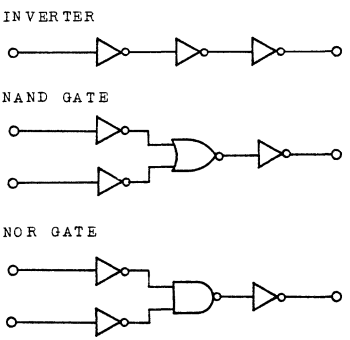
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ∼ 85	°C
Storage Temperature Range	T_{stg}	-65 ∼ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TC4572BP/BF

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS}, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS}, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V V_{OH}=2.5V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=9.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=13.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{IN}=V_{SS}, V_{DD}	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
Output Low Current	I_{OL}	V_{OL}=0.4V V_{OL}=0.5V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=1.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{IN}=V_{SS}, V_{DD}	15	4.0	-	3.4	15.0	-	2.8	-	
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.5V,13.5V	10	7.0	-	7.0	5.5	-	7.0	-	
		$\|I_{OUT}\|$<1μA	15	11.0	-	11.0	8.25	-	11.0	-	
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V	5	-	1.5	-	2.25	1.5	-	1.5	
		VOUT=1.5V,13.5V	10	-	3.0	-	4.5	3.0	-	3.0	
		$\|I_{OUT}\|$<1μA	15	-	4.0	-	6.75	4.0	-	4.0	
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	0.25	-	0.001	0.25	-	7.5	μA
			10	-	0.5	-	0.001	0.5	-	15	
			15	-	1.0	-	0.002	1.0	-	30	

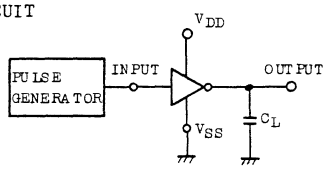
* All valid input combinations.

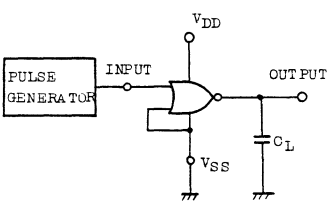
DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

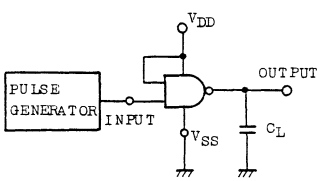
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (INVERTER)	t_{pLH} t_{pHL}		5	-	90	200	
			10	-	40	110	
			15	-	30	85	
Propagation Delay Time (NAND)	t_{pLH} t_{pHL}		5	-	95	200	
			10	-	45	110	
			15	-	35	85	
Propagation Delay Time (NOR)	t_{pLH} t_{pHL}		5	-	95	200	
			10	-	45	110	
			15	-	35	85	
Input Capacitance	C_{IN}			-	5	7.5	pF

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

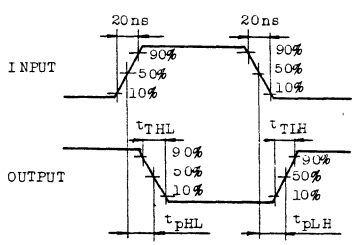
CIRCUIT







WAVEFORM



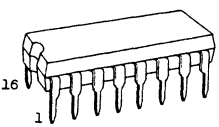
TC4583BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4583BP DUAL SCHMITT TRIGGER

TC4583BP consists of two independent Schmitt trigger circuits.

By externally connecting resistors between POSITIVE terminal and COMMON terminal and between NEGATIVE terminal and COMMON terminal, hysteresis can be given to two inputs A_{IN} and B_{IN}. Furthermore, the width of hysteresis and the threshold voltage between high level and low level can be varied by varying the resisters. The outputs are available in the forms of positive outputs and inverted three-state outputs from both circuits. Exclusive-OR of both inputs is also output.
This is most suitable for line receivers.

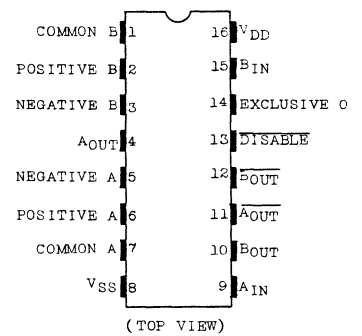


DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

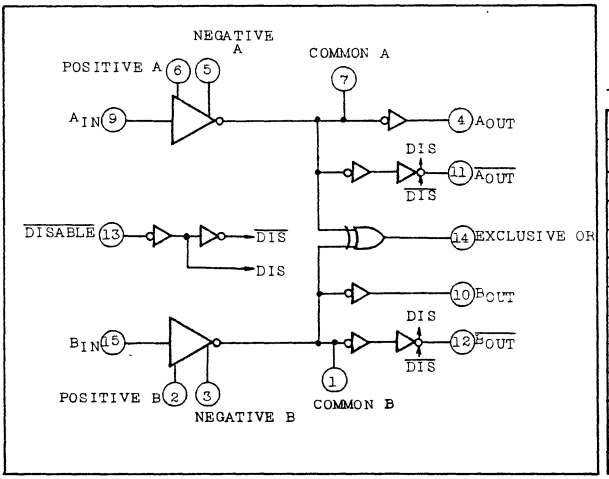
CHARACTERISTIC	SYMBOL	RATING	UNITS
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TRUTH TABLE

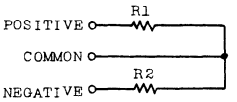
INPUTS			OUTPUTS				
A	B	DISABLE	A_{OUT}	$\overline{A_{OUT}}$	B_{OUT}	$\overline{B_{OUT}}$	EX.
L	L	L	L	HZ	L	HZ	L
L	L	H	L	H	L	H	L
L	H	L	L	HZ	H	HZ	H
L	H	H	L	H	H	L	H
H	L	L	H	HZ	L	HZ	H
H	L	H	H	L	L	H	H
H	H	L	H	HZ	H	HZ	L
H	H	H	H	L	H	L	L

HZ: HIGH IMPEDANCE

TC4583BP

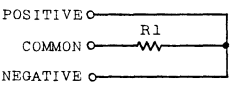
EXTERNAL RESISTER CONNECTION

(A)



Negative Threshold Voltage, V_N can be varied by changing R2 and Positive Threshold Voltage, V_P can be varied by changing R1.

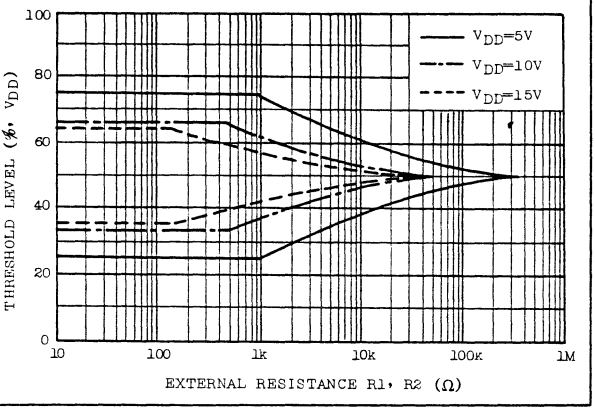
(B)



Hysteresis Voltage, V_H can be varied by changing R1.

Hysteresis Voltage $V_H = V_P - V_N$

External Resistance - Threshold Level (TYP.)



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
External Resistance	R1, R2		No Limits			Ω

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS}$, V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS}$, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									

TC4583BP

STATIC ELECTRICAL CHARACTERISTICS (Continued)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V									
			$\lvert I_{OUT}\rvert$<1μA	15	11.0	-	11.0	8.25	-	11.0	-	
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	5.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V									
			$\lvert I_{OUT}\rvert$<1μA	15	-	4.0	-	6.75	4.0	-	4.0	
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
3-State Output Leakage Current	"H" Level	I_{DH}	V_{OUT}=18V	18	-	0.4	-	10^{-4}	0.4	-	12	μA
	"L" Level	I_{DL}	V_{OUT}=0V	18	-	-0.4	-	-10^{-4}	-0.4	-	-12	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS}, V_{DD}	5	-	1	-	0.002	1	-	30	μA
				10	-	2	-	0.004	2	-	60	
			*	15	-	4	-	0.008	4	-	120	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

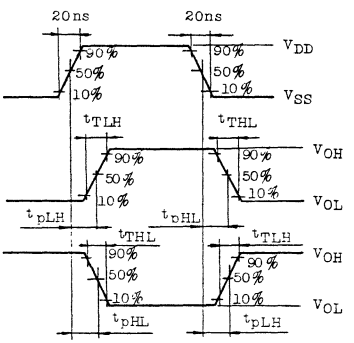
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (A_{IN}, B_{IN} - A_{OUT}, B_{OUT})	t_{pLH} t_{pHL}		5	-	200	1300	
			10	-	80	460	
			15	-	60	300	
Propagation Delay Time (A_{IN}, B_{IN} - $\overline{A_{OUT}}$, $\overline{B_{OUT}}$)	t_{pLH} t_{pHL}		5	-	200	2200	
			10	-	80	760	
			15	-	60	520	
Propagation Delay Time (A_{IN}, B_{IN} - EX, OR)	t_{pLH} t_{pHL}		5	-	210	1500	
			10	-	80	560	
			15	-	60	340	
3-State Disable Time ($\overline{DISABLE}$ - $\overline{A_{OUT}}$, $\overline{B_{OUT}}$)	t_{pLZ},t_{pHZ} t_{pZL},t_{pZH}	R_L=1kΩ	5	-	110	450	
			10	-	50	180	
			15	-	35	110	

DYNAMIC ELECTRICAL CHARACTERISTICS (Continued)

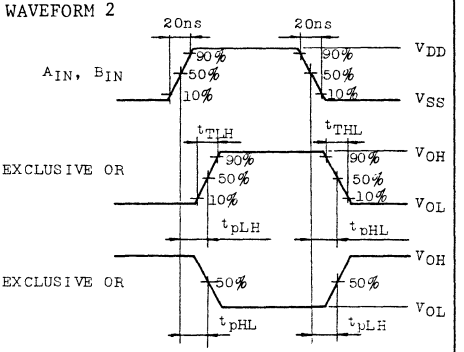
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Positive Threshold Voltage	V_P	Rl, R2=5kΩ	5	-	3.2	-	V
			10	-	5.55	-	
			15	-	8.0	-	
Negative Threshold Voltage	V_N	Rl, R2=5kΩ	5	-	1.8	-	
			10	-	4.45	-	
			15	-	7.0	-	
Hysteresis Voltage	V_H	Rl, R2=5kΩ	5	0.5	1.4	3.0	
			10	0.3	1.1	1.9	
			15	0.2	1.0	1.8	
Threshold Voltage Variation (A - B)	ΔV_T	Rl, R2=5kΩ	5	-	0.1	-	
			10	-	0.15	-	
			15	-	0.2	-	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

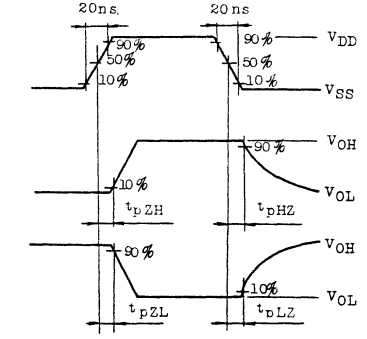
WAVEFORM 1



WAVEFORM 2



WAVEFORM 3



TC4584BP/BF

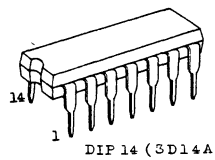
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4584BP/TC4584BF HEX SCHMITT TRIGGER

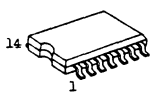
The TC4584BP/BF is the 6-circuit inverter having the Schmitt trigger function at the input terminal.

That is, since the circuit threshold level voltages at the leading and trailing edges of input waveform are different (V_P, V_N), the TC4584BP/BF can be used in the broad range application including line receiver, waveform shaping circuit, astable multivibrator, monostable multivibrator, etc. in addition to ordinary inverter.

Since the pins are compatible with the TC4069UB, the substitution is also possible.



DIP 14 (3D14A-P)

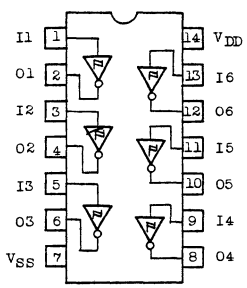


MFP 14 (F14GB-P)

ABSOLUTE MAXIMUM RATINGS

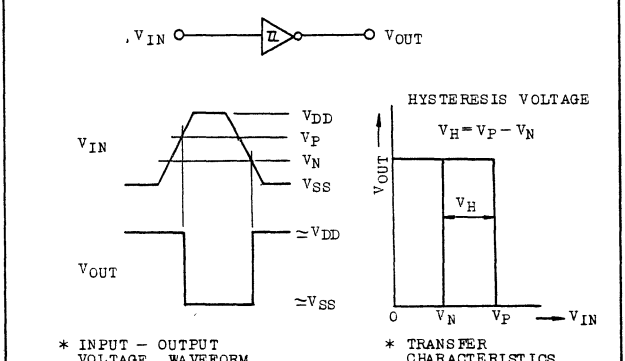
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

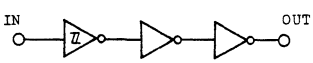
INPUT/OUTPUT VOLTAGE CHARACTERISTIC



* INPUT – OUTPUT VOLTAGE WAVEFORM

* TRANSFER CHARACTERISTICS

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
		V_{IN}=V_{SS}, V_{DD}	15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
		V_{IN}=V_{SS}, V_{DD}	15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		V_{IN}=V_{SS}, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		V_{IN}=V_{SS}, V_{DD}									
Positive Trigger Threshold Voltage	V_P	V_{OUT}=0.5V	5	2.05	3.75	2.15	3.0	3.75	2.15	3.85	V
		V_{OUT}=1.0V	10	4.8	7.6	4.9	6.4	7.6	4.9	7.7	
		V_{OUT}=1.5V	15	7.8	11.6	7.9	9.9	11.6	7.9	11.7	
Negative Trigger Threshold Voltage	V_N	V_{OUT}=4.5V	5	1.25	2.95	1.25	2.3	2.85	1.15	2.85	
		V_{OUT}=9.0V	10	2.4	5.2	2.4	3.8	5.1	2.3	5.1	
		V_{OUT}=13.5V	15	3.4	7.2	3.4	5.2	7.1	3.3	7.1	
Hysteresis Voltage	V_H		5	0.10	1.25	0.25	0.65	1.25	0.25	1.40	
			10	1.8	3.5	1.9	2.6	3.5	1.9	3.6	
			15	3.7	5.6	3.8	4.7	5.6	3.8	5.7	
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD}	5	-	1	-	0.001	1	-	7.5	μA
			10	-	2	-	0.002	2	-	15	
		*	15	-	4	-	0.004	4	-	30	

* All valid input combinations.

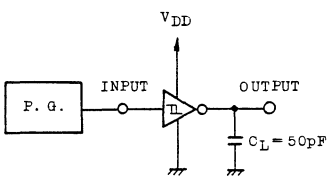
TC4584BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERITIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time	t_{pLH} t_{pHL}		5	-	170	340	
			10	-	80	160	
			15	-	60	120	
Input Capacitance	C_{IN}			-	5	7.5	pF

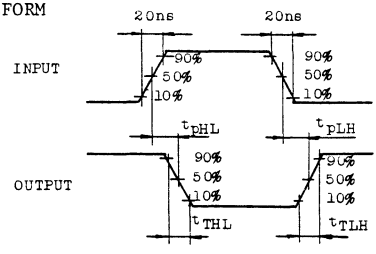
CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

CIRCUIT



P G. : PULSE GENERATOR

WAVEFORM

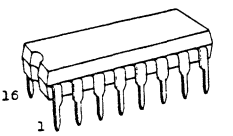


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4585BP

TC4585BP 4-BIT MAGNITUDE COMPARATOR

TC4585BP is weighted comparator which compares the magnitudes of input data of four bits A_0 through A_3 and another input data of four bits B_0 through B_3. If TC4585BP is used, signal of larger, smaller or equal is obtained at one of three output lines depending on the cascade inputs $(A>B)I_N$, $(A=B)I_N$ and $(A<B)I_N$.
It is easy to fabricate the magnitude comparators of 4 × n bits with cascade connection of n number of TC4585BP.

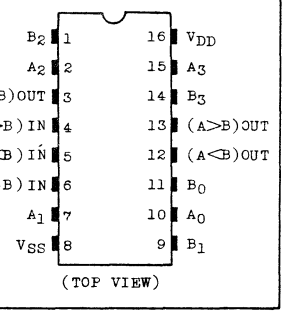


DIP 16(3D16A-P)

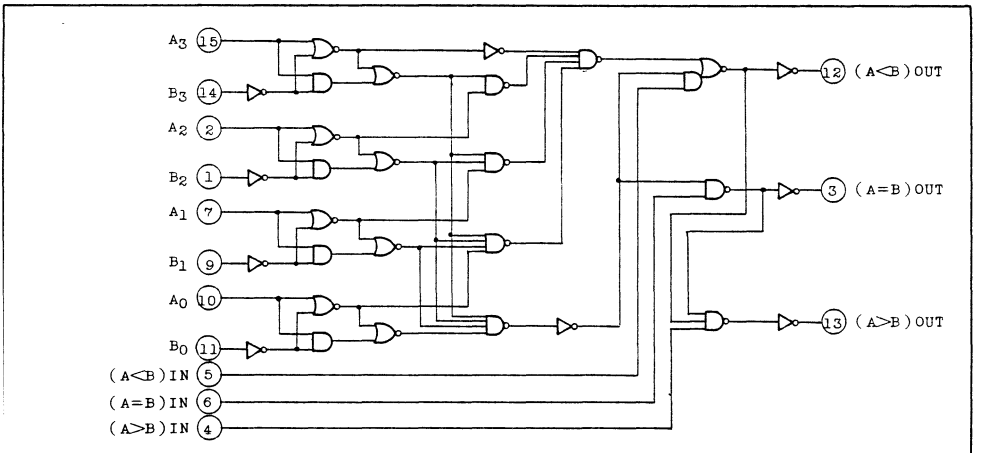
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TC4585BP

TRUTH TABLE

INPUTS							OUTPUTS			
COMPARING				CASCADING						
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	A<B	A=B	A>B	A<B	A=B	A>B	
$A_3>B_3$	*	*	*	*	*	H	L	L	H	
$A_3=B_3$	$A_2>B_2$	*	*	*	*	H	L	L	H	
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	*	*	*	H	L	L	H	
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	*	*	H	L	L	H	
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H	
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	*	L	H	L	
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	*	H	L	L	
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	*	*	*	H	L	L	
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	*	*	*	*	H	L	L	
$A_3=B_3$	$A_2<B_2$	*	*	*	*	*	H	L	L	
$A_3<B_3$	*	*	*	*	*	*	H	L	L	* Don't care

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	mA
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		V_{IN}=V_{SS},V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\| < 1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\| < 1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	-0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	μA
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS},V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

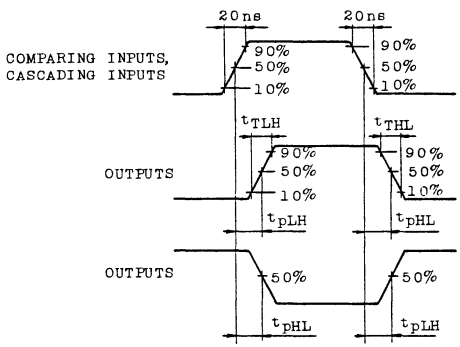
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (COMPARING INPUTS - OUTPUTS)	t_{pLH} t_{pHL}		5	-	340	680	ns
			10	-	140	280	
			15	-	100	200	

TC4585BP

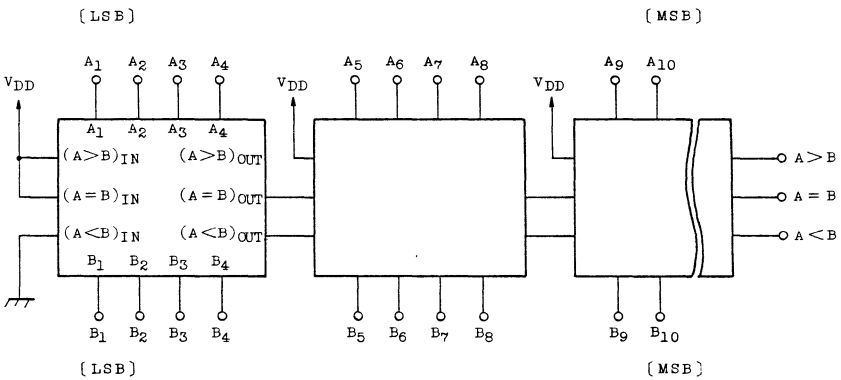
DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (CASCADING INPUTS - OUTPUTS)	t_{pLH} t_{pHL}		5	-	280	560	ns
			10	-	110	220	
			15	-	90	180	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



APPLICATION CIRCUIT

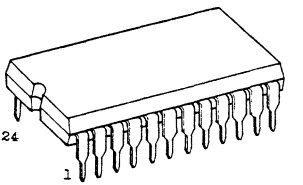


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5001P

TC5001P 4-DIGIT DECADE COUNTER

TC5001P is four digit decimal counter containing latches and multiplexer circuits and equipped with the terminals of digit signal outputs for dynamic display, blanking input (for zero suppress operation) and transfer input (latch operation).
The maximum count of this counter is 9999 and three CARRY terminals are provided for carry operations required in some applications.
Refer to TRUTH TABLE, TIMING CHART and OPERATING CONSIDERATION for the operations.

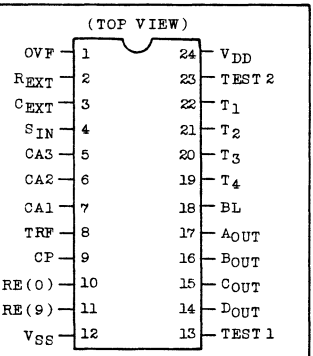


DIP 24 (6D24A-P)

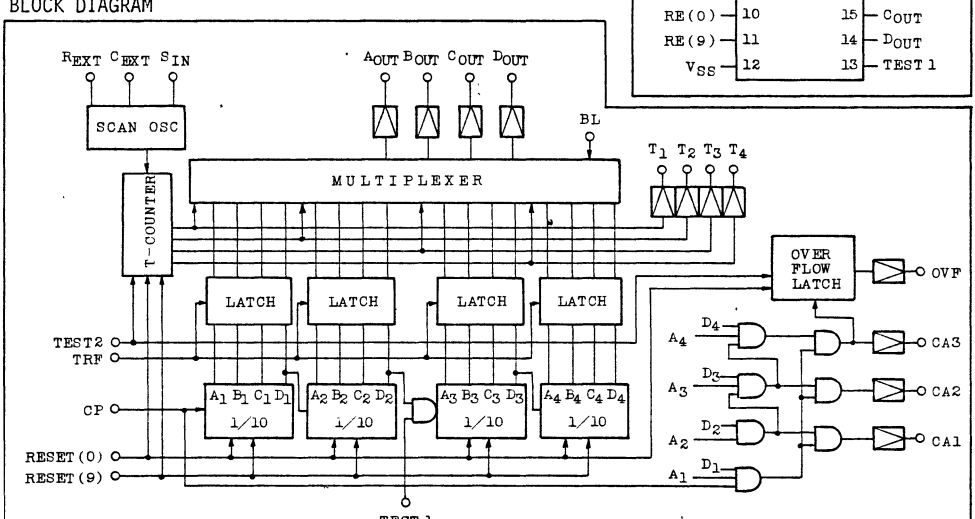
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-55 ~ 125	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



BLOCK DIAGRAM



TC5001F

DESCRIPTION OF PIN FUNCTION

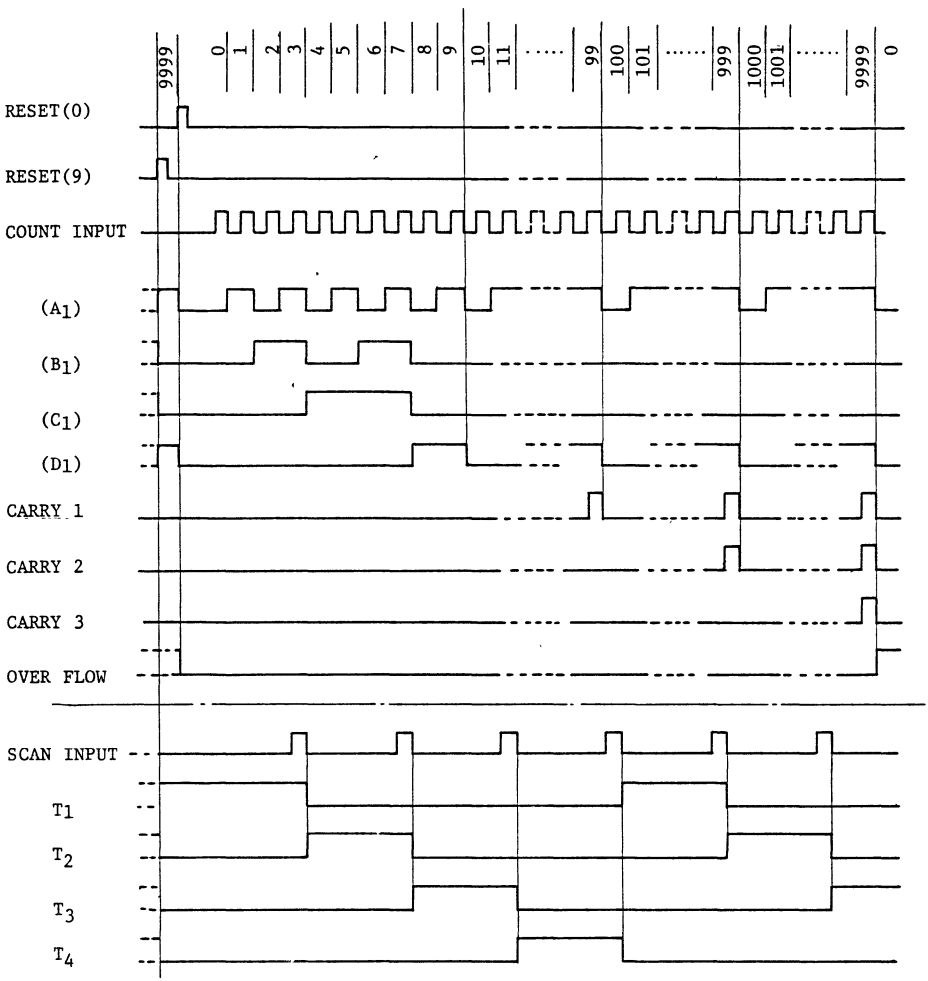
PIN No.	SYMBOL	NAME	FUNCTION
1	OVF	OVER FLOW	Terminal to detect OVER FLOW condition of the counter which generates "H" level when COUNT is incremented from"9999". Once set to "H", only RESET (0) can clear it to "L".
2	R_{EXT}	RESISTER EXTERNAL	This is opened when external CLOCK is supplied from S_{IN}. If external CLOCK is not available, CLOCK can be generated by externally connecting a resistor across S_{IN} and R_{EXT} and a capacitor across S_{IN} and C_{EXT}.
3	C_{EXT}	CAPACITANCE EXTERNAL	
4	S_{IN}	SCAN INPUT	T-COUNTER CLOCK input and T-COUNTER is changed its condition at the falling edge of S_{IN}.
5	CA3	CARRY-3	CARRY output from n-th digit: COUNTER "9999" / "X999" / "xx99" — "H" during CP= "H" in COUNT shown at the left,"L" otherwise.
6	CA2	CARRY-2	
7	CA1	CARRY-1	
8	TRF	TRANSFER	"H": Decimal COUNTER output is transferred to MULTIPLEXER as it is. "L": COUNTER output at the time of falling edge of TRF is latched.
9	CP	COUNT INPUT	Lowest order decimal COUNTER CLOCK input and COUNTER is counted by the falling edge of CP.
10	RE (0)	RESET (0)	"H": Decimal COUNTER output is reset to "0000". This takes precedence over RE (9). "L": If RE (9) = "L", normally counted.
11	RE (9)	RESET (9)	"H": If RE (0) = "L", COUNTER output is set to "9999". "L": If RE (0) = "L", normally counted.
12	V_{SS}	V_{SS}	(GND)

DESCRIPTION OF PIN FUNCTION

PIN No.	SYMBOL	NAME	FUNCTION	
13	$TEST_1$	$TEST_1$	"H"	If TEST (2) = "H", normally counted.
			"L"	If TEST (2) = "H", only lower order two digits are counted.
14	D_{OUT}	D-OUTPUT	Decimal COUNTER BCD outputs. When T_1="H", the lowest order digit (first digit) is output, when T_2 = "H", the second digit is output, ... and when T_4 = "H", the fourth digit is output. During BLANKING all the outputs become "H".	
15	C_{OUT}	C-OUTPUT		
16	B_{OUT}	B-OUTPUT		
17	A_{OUT}	A-OUTPUT		
18	BL	BLANKING	If BL = "H", only all A_{OUT} through D_{OUT} (BCD OUT) become "H".	
19	T_4	T_4	Output to indicate the digit position of output signals A_{OUT} through D_{OUT} (BCD OUT) and corresponds in descending order from T_1.	
20	T_3	T_3		
21	T_2	T_2		
22	T_1	T_1		
23	$TEST_2$	$TEST_2$	"H"	Normally counted.
			"L"	Causes T_1 = "L", $T_2 \sim T_4$ = "H", OVF = "H".
24	V_{DD}	V_{DD}	V_{DD} Power Supply (3$\sim$8 volt)	

TC5001P

TIMING CHART



* Waveforms marked with ( ) are timings of LSI's internal signals.

A_{OUT}, B_{OUT}, C_{OUT} and D_{OUT} are output in the timings in synchronism with T_1, T_2, T_3 and T_4 respectively.

RUTH TABLE

RESET (0)	RESET (9)	TRAN-SFER	BLAN-KING	$TEST_1$	$TEST_2$	A_{OUT}	B_{OUT}	C_{OUT}	D_{OUT}	T_1	T_2	T_3	T_4	OVER FLOW	
H	*	H	L	*	H	L	L	L	L	H	L	L	L	L	Note-1
L	H	H	L	*	H	H	L	L	H	H	L	L	L	X	Note-1
L	L	H	L	H	H	C	C	C	C	S	S	S	S	X	
L	L	H	L	L	H	C'	C'	C'	C'	S	S	S	S	X	
*	*	L	L	*	*	LA	LA	LA	LA	X	X	X	X	X	
*	*	*	H	*	*	H	H	H	H	X	X	X	X	X	
*	*	*	*	*	L	X	X	X	X	L	H	H	H	H	

* Don't Care

X Not defined

C Count operation (all digits)

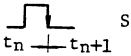
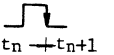
C' Count operation (only lower order two digits)

LA Latch operation

S Scan operation

Note 1. SCAN INPUT = "L"

o All the inputs/outputs (except COUNT INPUT and SCAN INPUT) are activated by "H" level.

o COUNT INPUT  SCAN INPUT 

o When used, $TEST_1$ = "H" and $TEST_2$ = "H" should be satisfied.

ERATING CONSIDERATION

1. RESET Operation

(1) When the level of RESET (0) terminal is set to "H", BCD output of COUNTER is set to "0". The four digit display becomes 0000.

(2) When the level of RESET (9) terminal is set to "H", BCD output of COUNTER is set to "9". The four digit display becomes 9999.

(3) When both of RESET (0) terminal and RESET (9) terminal are "H", RESET (0) terminal takes precedence.

2. SCAN Operation

(1) SCAN signal for dynamic display applied to SCAN INPUT terminal controls the multiplexer circuit and transfers four digit information in the latches to BCD outputs one digit at a time in sequence.

TC5001P

OPERATING CONSIDERATION

(2) Arbitrary digit can be made real time output (completely static) by making SCAN signal DC.

(3) The digit pulses in synchronism with SCAN signal for dynamic display appear at the digit output terminals (T_1, T_2, T_3 and T_4). The digit output terminals (T_1, T_2, T_3 and T_4) are used for the digit selection circuit and for arbitrary digit zero suppress.

(4) The digit pulse is activated by the falling edge of SCAN INPUT signal.

(5) SCAN signal is supplied from the internal oscillator as shown in Fig. 1 or from the external one as shown in Fig. 2.

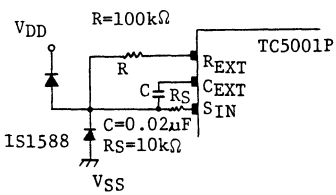


Fig. 1

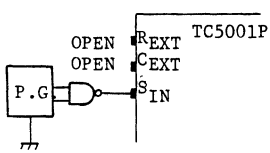


Fig. 2

$$f_{SCAN} \fallingdotseq \frac{1}{2.2CR} \text{ [Hz]}$$

3. Latch Operation

(1) When the level of TRANSFER terminal is "H", COUNTER information is transferred to the latches.

(2) When the level of TRANSFER terminal is charged from "H" to "L", the information transferred from COUNTER is latched.

4. Count Operation

(1) Set input terminals $TEST_1$, $TEST_2$ and TRANSFER to "H" and BLANKING terminal to "L".

(2) COUNTER is set by applying "H" level to RESET (0) or RESET (9) terminal and two RESET terminals are returned to "L".

PERATING CONSIDERATION

(3) When the count pulse is applied to COUNT INPUT terminal, COUNTER performs its COUNT operation at the falling edge of count pulse.

(4) The maximum count is 9999 and if 9999 is exceeded, "H" level appears at OVER FLOW terminal. Removal of OVER FLOW signal can be achieved by applying"H" to RESET (0) terminal.

(5) The carry signals from 100's and 1000's digits appear at output terminals $CARRY_1$, $CARRY_2$ and $CARRY_3$.

(6) When $TEST_1$ terminal is "L", only lower order two digits of COUNTER are counted.

5. BLANKING Operation

When BLANKING terminal is set to "H", all the BCD outputs of COUNTER become "H" and this signal is used to achieve the zero suppress operation.

TC5001P

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	8	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temp.	Topr		-30	-	85	°C
External Registance	R_{EXT}		10	100	1000	kΩ
External Capacitance	C_{EXT}		10^{-4}	0.02	1.0	μF

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

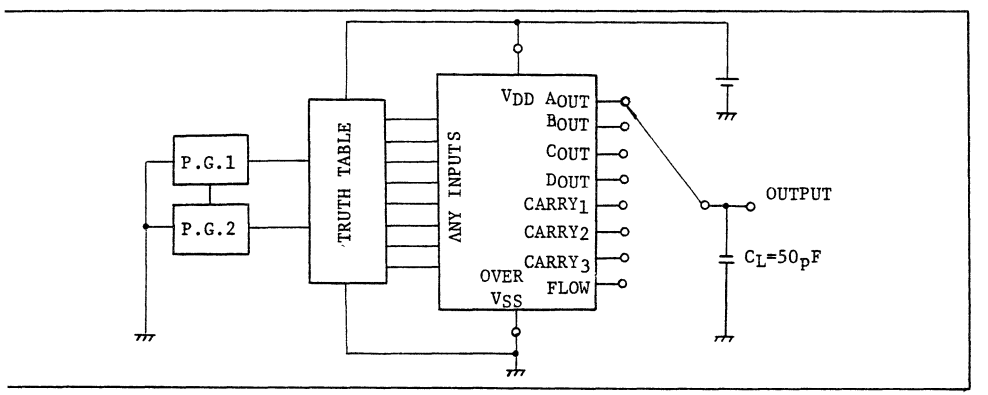
CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-30°C MIN.	-30°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage		V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{DD},V_{SS}$	5	4.95	-	4.95	-	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{DD},V_{SS}$	5	-	0.05	-	-	0.05	-	0.05	V
High Level Output Current	AOUT,BOUT COUT,DOUT	I_{OH}	V_{OH} = 2.5V $V_{IN}=V_{DD},V_{SS}$	5	-1.2	-	-1.0		-	-0.75	-	mA
	CARRY1,2,3 OVER FLOW T1,T2,T3, T4	I_{OH}		5	-1.2	-	-1.0		-	-0.75	-	
	REXT CEXT	I_{OH}		5	-0.3	-	-0.25		-	-0.2	-	
Low Level Output Current	AOUT,BOUT COUT,DOUT	I_{OL}	V_{OL} = 0.4V $V_{IN}=V_{DD},V_{SS}$	5	2.4	-	2.0		-	1.6	-	mA
	CARRY1,2,3 OVER FLOW T1,T2,T3, T4	I_{OL}		5	0.52	-	0.44		-	0.36	-	
	REXT CEXT	I_{OL}		5	0.28	-	0.24		-	0.2	-	
Input Voltage	"H" Level	V_{IH}	V_{OUT}=0.1V,4.9V	5	3.8	-	3.8	2.75	-	3.8	-	V
	"L" Level	V_{IL}	$\|I_{OUT}\| < 1\mu A$	5	-	1.2	-	2.25	1.2	-	1.2	
Input Current	"H" Level	I_{IH}	V_{IH} = 8V	8	-	0.2	-		0.2		1.0	μA
	"L" Level	I_{IL}	V_{IL} = 0V	8	-	-0.2	-		-0.2		-1.0	
Quiescent Current Consumption		I_{DD}	$V_{IN}=V_{DD},V_{SS}$ *	8	-	50	-	-	50	-	500	μ

* All valid input combinations

WITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L = 50pF)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
(LOW-HIGH) Propagation Delay Time		t_{pLH}	COUNT INPUT — A,B,C,D_{OUT} (Waveform 1)	5	-	600	1000	ns
(HIGH-LOW) Propagation Delay Time		t_{pHL}		5	-	600	1000	
(LOW-HIGH) Propagation Delay Time		t_{pLH}	TRANSFER — A,B,C,D_{OUT} (Waveform 2)	5	-	400	1000	
(HIGH-LOW) Propagation Delay Time		t_{pHL}		5	-	400	1000	
(LOW-HIGH) Propagation Delay Time		t_{pLH}	COUNT INPUT — $CARRY_{1,2,3}$ — OVER FLOW (Waveform 3)	5	-	400	1000	
(HIGH-LOW) Propagation Delay Time		t_{pHL}		5	-	400	1000	
Max. Clock Rise Time		$t_{r\phi}$,$t_{f\phi}$		5	20	-	-	μs
Min. Clear Pulse Width		$t_{w(RE)}$	RESET(0),(9)	5	-		1000	ns
Min. Transfer Pulse Width		$t_{w(TR)}$	TRANSFER	5	-		1000	
Input Capacity	9, 10, 11, 18 PIN	C_{IN}			-	5	7.5	pF
	4, 13, 23 PIN	C_{IN}			-	7	10	
	8 PIN	C_{IN}			-	9	15	
Max. Clock Frequency		$f_{MAX\phi}$		5	0.5	2.0	-	MHz

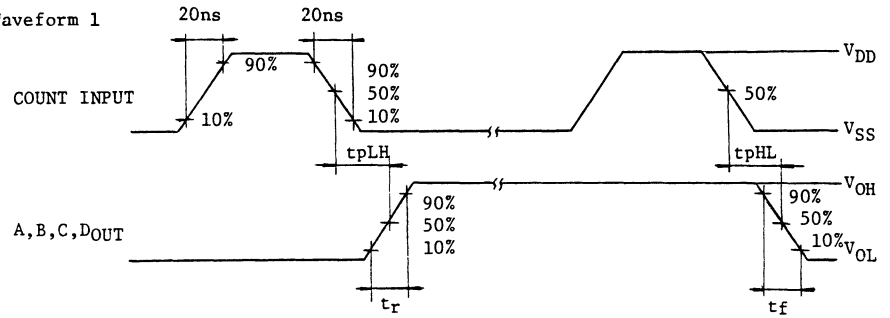
WITCHING TIME TEST CIRCUIT



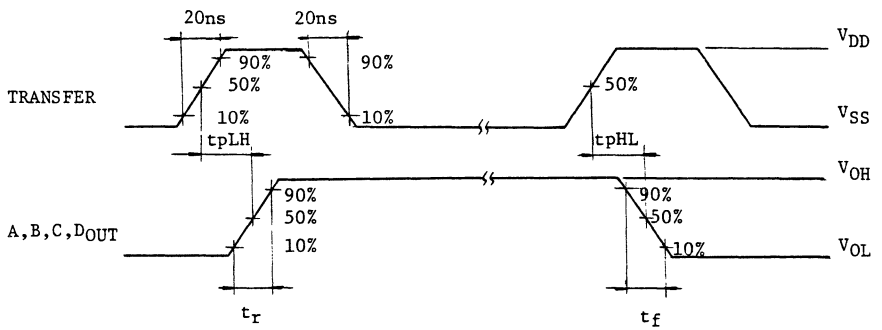
TC5001P

SWITCHING TIME TEST WAVEFORMS

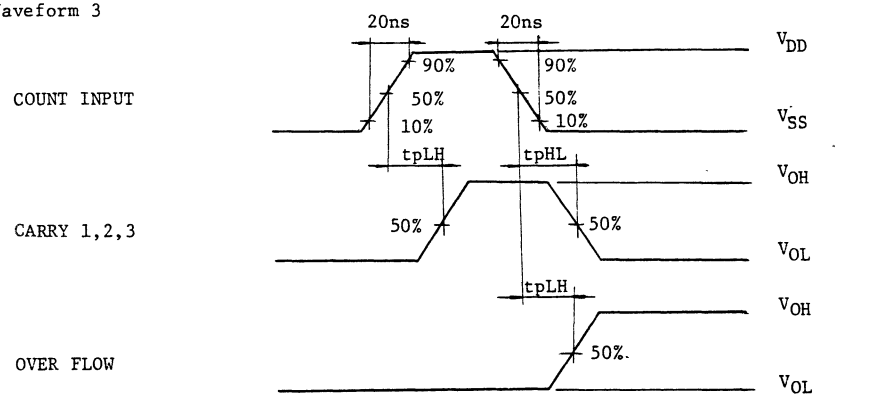
Waveform 1



Waveform 2



Waveform 3

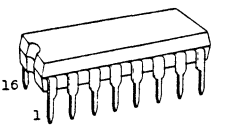


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5002BP
TC5022BP

C5002BP, TC5022BP BCD TO 7-SEGMENT DECODER/DRIVER

C5002BP and TC5022BP are decoders to convert BCD
ode input to the driving signal for 7-segment
isplay element and equipped with NPN transistors as
he output buffers enabling direct driving of common
athode type LED.
hen BI input is set at "H" level, all the segment
utputs are turned "OFF" (not illumination) regardless
f other inputs.
BI input is to turn the output "OFF" and RBO input
s to generate "H" level output only for "0" code
nput and these are used for leading zero suppress
hen connected in cascade.

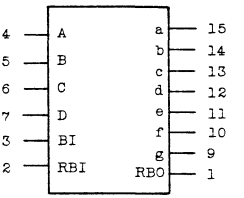


DIP 16 (3D16A-P)

BSOLUTE MAXIMUM RATINGS

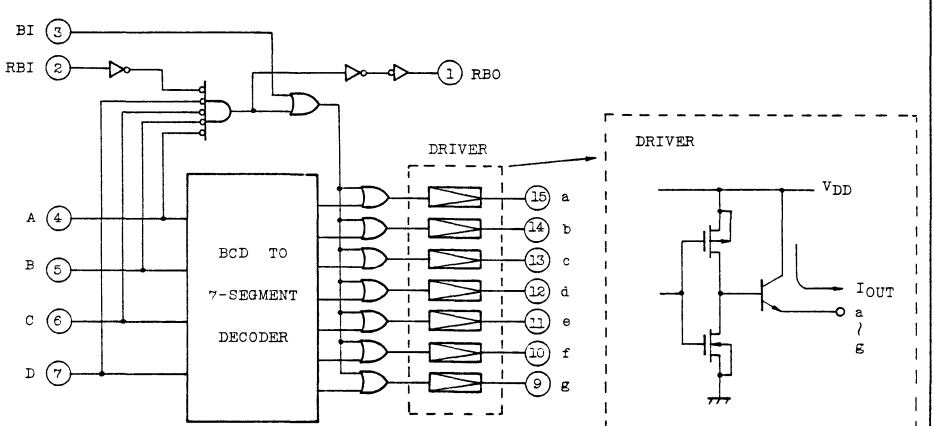
CHARACTERISTIC	SYMBOL	RATING	UNIT
C Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
nput Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
utput Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
C Input Current	I_{IN}	±10	mA
ower Dissipation	P_D	300	mW
torage Temperature ange	T_{stg}	-65 ~ 150	°C
ead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



V_{DD} : 16, V_{SS} 8

OGIC DIAGRAM



TC5002BP, TC5022BP

TRUTH TABLE

(TC5002BP)

INPUT						OUTPUT								
BI	RBI	A	B	C	D	a	b	c	d	e	f	g	RBO	NOTE
H	*	*	*	*	*	L	L	L	L	L	L	L	☆	
L	H	L	L	L	L	L	L	L	L	L	L	L	H	
L	L	L	L	L	L	H	H	H	H	H	H	L	L	
L	*	H	L	L	L	L	H	H	L	L	L	L	L	
L	*	L	H	L	L	H	H	L	H	H	L	H	L	
L	*	H	H	L	L	H	H	H	H	L	L	H	L	
L	*	L	L	H	L	L	H	H	L	L	H	H	L	
L	*	H	L	H	L	H	L	H	H	L	H	H	L	
L	*	L	H	H	L	L	L	H	H	H	H	H	L	1
L	*	H	H	H	L	H	H	H	L	L	L	L	L	2
L	*	L	L	L	H	H	H	H	H	H	H	H	L	
L	*	H	L	L	H	H	H	H	L	L	H	H	L	3
L	*	L	H	L	H	H	H	H	H	H	H	L	L	
L	*	H	H	L	H	L	H	H	L	L	L	L	L	
L	*	L	L	H	H	H	H	L	H	H	L	H	L	
L	*	H	L	H	H	H	H	H	H	L	L	H	L	
L	*	L	H	H	H	L	H	H	L	L	H	H	L	
L	*	H	H	H	H	H	L	H	H	L	H	H	L	

NOTE 1 : TC5022BP, ——→ a = "H"

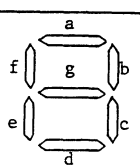
2 : TC5022BP, ——→ f = "H"

3 : TC5022BP, ——→ d = "H"

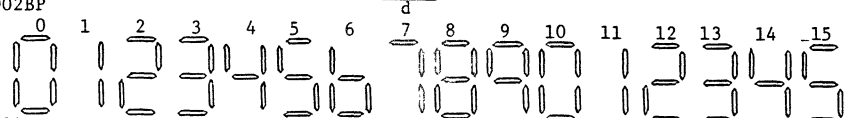
☆ : Undetermined

* : Don't Care

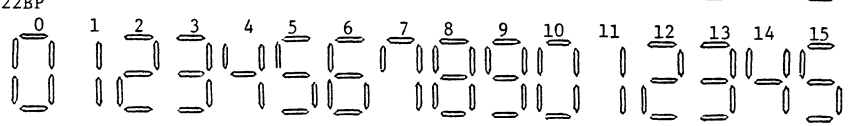
DISPLAY INDICATE MODE



TC5002BP



TC5022BP



COMMENDED OPERATING CONDITIONS (V_{SS}= 0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temp.	Topr		-40	-	85	°C

ECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage (RBO)	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}$, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low Level Output Voltage (RBO)	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}$, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
High Level Output Voltage (a - g)	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}$, V_{DD}	5	4.0	-	4.0	4.5	-	4.0	-	V
			10	9.0	-	9.0	9.5	-	9.0	-	
			15	14.0	-	14.0	14.5	-	14.0	-	
High Level Output Current (RBO)	I_{OH}	V_{OH}=4.6V V_{OH}=9.5V V_{OH}=13.5V $V_{IN}=V_{SS}$, V_{DD}	5	-0.2	-	-0.16		-	-0.12	-	mA
			10	-0.5	-	-0.4		-	-0.3	-	
			15	-1.4	-	-1.2		-	-1.0	-	
Low Level Output Current (RBO)	I_{OL}	V_{OL}=0.4V V_{OL}=0.5V V_{OL}=1.5V $V_{IN}=V_{SS}$, V_{DD}	5	0.52	-	0.44		-	0.36	-	
			10	1.3	-	1.1		-	0.9	-	
			15	3.6	-	3.0		-	2.4	-	
High Level Output Current (a - g)	I_{OH}	V_{OH}=3.5V V_{OH}=8.5V V_{OH}=13.5V $V_{IN}=V_{SS}$, V_{DD}	5	-20	-	-20		-	-15	-	mA
			10	-25	-	-25		-	-20	-	
			15	-30	-	-30		-	-25	-	
High Level Input Voltage	V_{IH} **	V_{OUT}=0.5V,4.0V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\| < 1\mu A$	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
Low Level Input Voltage	V_{IL} **	V_{OUT}=0.5V,4.0V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\| < 1\mu A$	5	-	1.5	-	2.25	1.5	-	1.5	
			10	-	3.0	-	4.5	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
Disable Current (a - g)	I_{DL}	V_{OL}=0V	18	-	-3.0	-	-10^{-4}	-3.0	-	-30	μA
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Current Consumption	I_{DD}	$V_{IN}=V_{SS}$,V_{DD} *	5	-	20	-	0.005	20	-	150	μA
			10	-	40	-	0.010	40	-	300	
			15	-	80	-	0.015	80	-	600	

* All valid input combinations. Outputs open.

** Required pull down register R_L = 20 kΩ (a ~ g outputs).

TC5002BP, TC5022BP

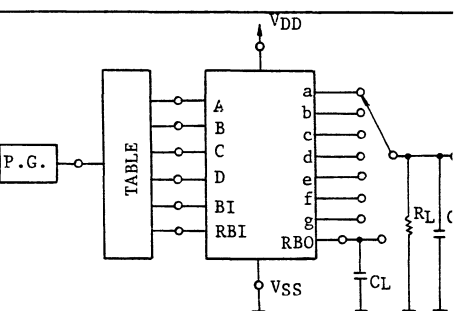
SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50 pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time (SEGMENT OUT)	t_r	R_L=1 kΩ	5	-	100	200	ns
			10	-	50	100	
			15	-	40	80	
Output Rise Time (RBO)	t_r		5	-	130	400	
			10	-	65	200	
			15	-	50	160	
Output Fall Time (RBO)	t_f		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
(LOW-HIGH) Propagation Delay Time (A,B,C,D-SEGMENT OUT)	t_{pLH}	R_L=1 kΩ	5	-	500	1000	ns
			10	-	150	400	
			15	-	120	300	
(HIGH-LOW) Propagation Delay Time (A,B,C,D-SEGMENT OUT)	t_{pHL}	R_L=1 kΩ	5	-	1000	2000	
			10	-	450	1000	
			15	-	320	700	
(LOW-HIGH) Propagation Delay Time (A,B,C,D - RBO)	t_{pLH}		5	-	1000	2000	ns
			10	-	370	1000	
			15	-	250	750	
(HIGH-LOW) Propagation Delay Time (A,B,C,D - RBO)	t_{pHL}		5	-	500	1000	
			10	-	200	500	
			15	-	140	300	
(LOW-HIGH) Propagation Delay Time (RBI - RBO)	t_{pLH}		5	-	800	1600	ns
			10	-	270	700	
			15	-	190	500	
(HIGH-LOW) Propagation Delay Time (RBI - RBO)	t_{pHL}		5	-	180	700	
			10	-	70	350	
			15	-	50	250	
Propagation Delay Time (BI - SEGMENT OUT)	t_{pLH} t_{pHL}	R_L=1 kΩ	5	-	500	1500	ns
			10	-	200	600	
			15	-	150	500	
Input Capacity	C_{IN}			-	5	7.5	pF

SWITCHING TIME TEST CIRCUIT

TABLE (t_{pLH}, t_{pHL} Test Codition)

TEST	P.G.	"H"	"L"	OUTPUT	Wave-form
A,B,C,D - SEGMENT OUT	A	-	Other Inputs	a	1
A,B,C,D - RBO	A	RBI	Other Inputs	RBO	2
RBI - RBO	RBI	-	Other Inputs	RBO	3
BI - SEGMENT OUT	BI	A,B	Other Inputs	a	4



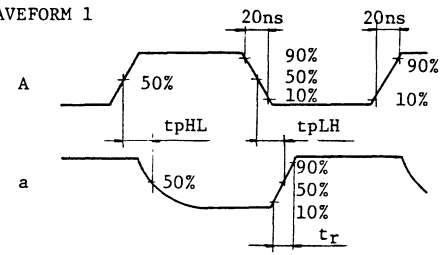
P.G.: PULSE GENERATOR

C_L=50pF

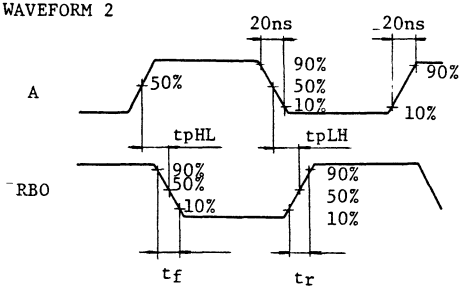
R_L=1kΩ

WITCHING TIME TEST WAVEFORMS

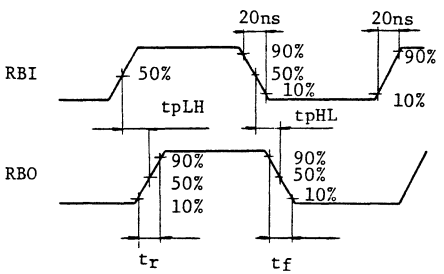
WAVEFORM 1



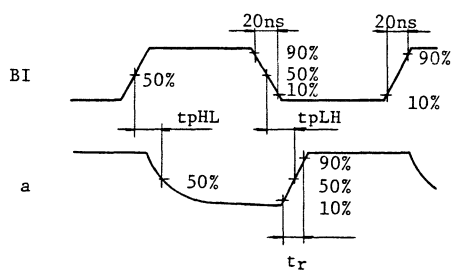
WAVEFORM 2



WAVEFORM 3



WAVEFORM 4

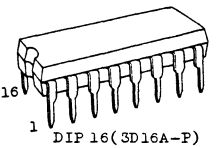


TC5012BP/BF

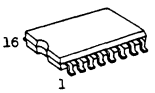
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5012BP/TC5012BF HEX NON-INVERTING 3-STATE BUFFER

TC5012BP/BF contains six circuits of non-inverting buffers having three state output.
Since DISABLE inputs to disable the outputs are provided separately, one common for four circuits and another common for other two circuits, this is suitable for controlling four bit data lines.
Large output current enables to directly control one TTL input.



DIP 16(3D16A-P)

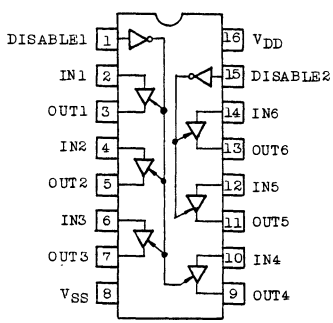


MFP 16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

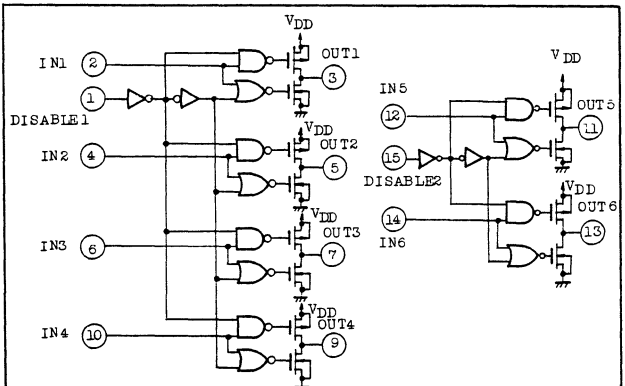
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ∼ 85	°C
Storage Temperature Range	T_{stg}	-65 ∼ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

CIRCUIT DIAGRAM



TRUTH TABLE

DISABLE INPUT	INPUT	OUTPUT
L	L	L
L	H	H
H	*	HZ

* . DON'T CARE

HZ : HIGH IMPEDANCE

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS}, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
				10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS}, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
				10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V V_{OH}=2.5V V_{OH}=9.5V V_{OH}=13.5V V_{IN}=V_{SS}, V_{DD}	5	-	-	-		-	-	-	mA
				5	-1.4	-	-1.25		-	-1.0	-	
				10	-1.4	-	-1.25		-	-3.0	-	
				15	-4.0	-	-3.75		-	-3.0	-	
Output Low Current		I_{OL}	V_{OL}=0.4V V_{OL}=0.5V V_{OL}=1.5V V_{IN}=V_{SS}, V_{DD}	5	3.5	-	3.2		-	2.5	-	
				10	6.0	-	5.0		-	3.6	-	
				15	26.0	-	24.0		-	18.0	-	
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\|$<1μA	5	3.5	-	3.5	2.75	-	3.5	-	V
				10	7.0	-	7.0	5.5	-	7.0	-	
				15	11.0	-	11.0	8.25	-	11.0	-	
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V V_{OUT}=1.0V, 9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\|$<1μA	5	-	1.5	-	2.25	1.5	-	1.5	
				10	-	3.0	-	4.5	3.0	-	3.0	
				15	-	4.0	-	6.75	4.0	-	4.0	
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
3-State Output Leakage Current	"H" Level	I_{DH}	V_{OUT}=18V	18	-	0.5	-	10^{-4}	0.5	-	30	
	"L" Level	I_{DL}	V_{OUT}=0V	18	-	-0.5	-	-10^{-4}	-0.5	-	-30	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS}, V_{SS} *	5	-	4.0	-	0.002	4.0	-	30	
				10	-	8.0	-	0.004	8.0	-	60	
				15	-	16.0	-	0.008	16.0	-	120	

* All valid input combinations.

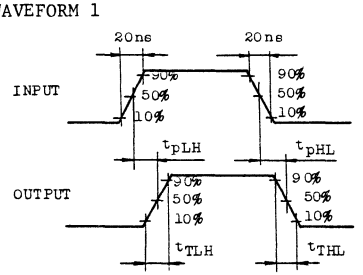
TC5012BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

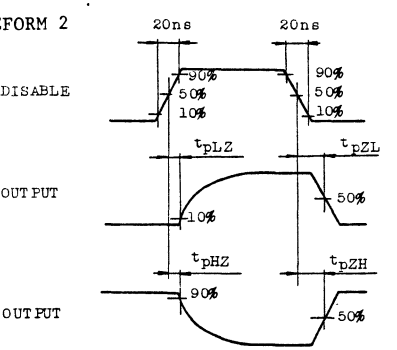
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	100	
Output Transition Time (High to Low)	t_{THL}		5	-	70	200	
			10	-	40	100	
			15	-	35	80	
Propagation Delay Time (IN - OUT)	t_{pLH}		5	-	320	430	
			10	-	150	220	
			15	-	110	200	
Propagation Delay Time (IN - OUT)	t_{pHL}		5	-	280	380	
			10	-	130	220	
			15	-	100	200	
Three State Disable Time (DISABLE - OUT)	t_{pHZ}	R_L=1kΩ	5	-	320	500	
			10	-	280	450	
			15	-	250	400	
Three State Disable Time (DISABLE - OUT)	t_{pLZ}	R_L=1kΩ	5	-	420	600	
			10	-	320	500	
			15	-	270	450	
Three State Disable Time (DISABLE - OUT)	t_{pZH}	R_L=1kΩ	5	-	280	400	
			10	-	140	200	
			15	-	120	180	
Three State Disable Time (DISABLE - OUT)	t_{pZL}	R_L=1kΩ	5	-	300	450	
			10	-	150	225	
			15	-	130	200	
Input Capacitance	C_{IN}			-	7.5	15	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1



WAVEFORM 2

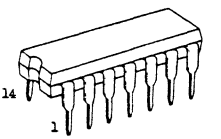


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5018P

TC5018P 4 BIT BINARY COUNTER WITH CLOCK GENERATOR

TC5018P is four digit binary counter equipped with CR oscillator circuit to automatically generate the clock pulse and RS flip-flop to provide the clock input by mechanical contact points.
The outputs are buffered by N-channel open-drain structure which enables to directly drive two TTL IC's or LED components.
Usually, binary codes are obtained at four output with SELECT input being "H", but if SELECT input is set to "L", scan output which shifts "L" level on Q_1-Q_4 in sequence is obtained. This is suitable for applications such as channel scanner.

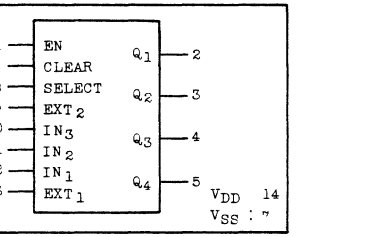


DIP 14 (3D14A-P)

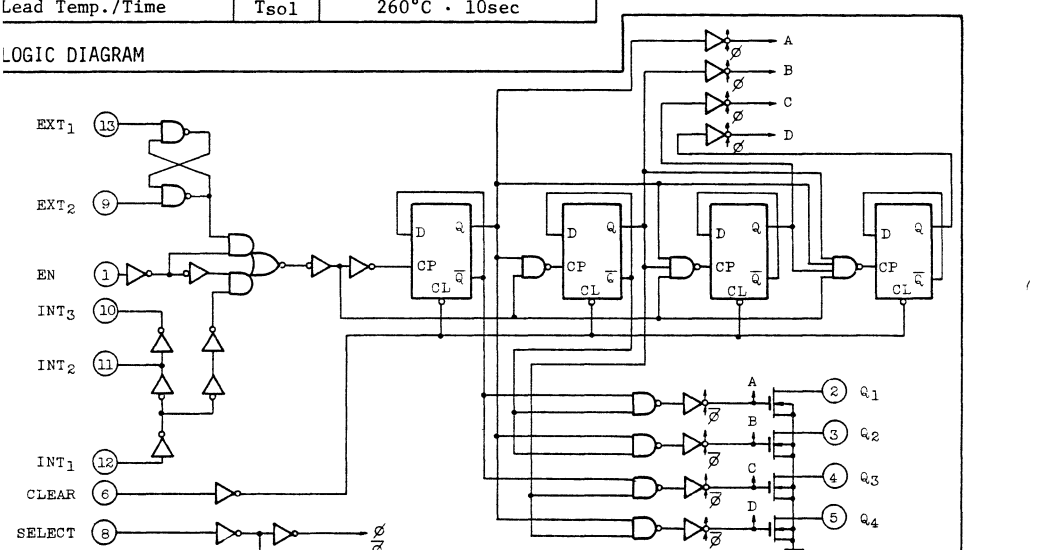
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+14	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	Tstg	-65 ~ 150	°C
Lead Temp./Time	Tsol	260°C · 10sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TC5018P

TRUTH TABLE

INPUTS						OUTPUTS			
IN_1	EXT_1	EXT_2	EN	SELECT	CLEAR	Q_1	Q_2	Q_3	Q_4
*	$\overline{CP}$	CP	L	L	L	S	S	S	S
CP	*	*	H	L	L	S	S	S	S
*	$\overline{CP}$	CP	L	H	L	C	C	C	C
CP	*	*	H	H	L	C	C	C	C
*	*	*	*	L	H	L	H	H	H
*	*	*	*	H	H	L	L	L	L

C ; Count operation
S ; Clean Operation
CP; Clock Pulse
* ; Don't care
(Note) Outputs change the state at the rising edge of CLOCK.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	12	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temp.	Topr		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	V
		$V_{IN}=V_{SS}$, V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
Low Level Output Current	I_{OL}	V_{OL} = 0.4V	5	4.5	-	4.5	9.0	-	3.2	-	mA
		V_{OL} = 0.5V	10	9.0	-	9.0	20.0	-	6.0	-	
		$V_{IN}=V_{SS}$, V_{DD}									
High Level Input Voltage	V_{IH}	V_{OUT}=0.5V,4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V,9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
	△	$\|I_{OUT}\| < 1\mu A$									
Low Level Input Voltage	V_{IL}	V_{OUT}=0.5V,4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V,9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
	△	$\|I_{OUT}\| < 1\mu A$									
Output Off Leakage Current	I_{DH}	V_{DH} = 12V	12	-	0.5	-	10^{-4}	0.5	-	30	μA
Input Current H Level	I_{IH}	V_{IH} = 12V	12	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current L Level	I_{IL}	V_{IL} = 0V	12	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Current Consumption	I_{DD}	$V_{IN}=V_{SS}$, V_{DD} *	5	-	20	-	0.005	20	-	150	μA
			10	-	40	-	0.010	40	-	300	

* All valid input combinations
△ R_L = 10 kΩ

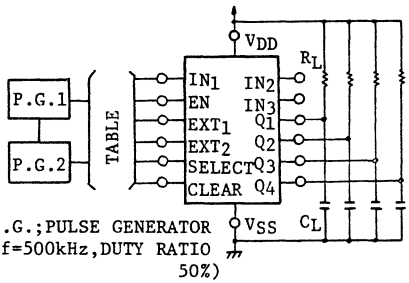
WITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
)utput Fall Time	t_f	R_L = 5kΩ	5	-	-	200	ns
		C_L = 50pF	10	-	-	100	
(LOW-HIGH) 'ropagation Delay Time (INT_1 - Q)	tpLH	R_L = 5kΩ	5	-	750	1800	ns
		C_L = 50 pF	10	-	380	900	
(HIGH-LOW) 'ropagation Delay Time (INT_1 - Q)	tpHL	R_L = 5kΩ	5	-	500	1500	
		C_L = 50pF	10	-	200	600	
(LOW-HIGH) 'ropagation Delay Time (EXT_2 - Q)	tpLH	R_L = 5kΩ	5	-	750	1800	ns
		C_L = 50pF	10	-	380	900	
(HIGH-LOW) 'ropagation Delay Time (EXT_2 - Q)	tpHL	R_L = 5kΩ	5	-	500	1500	
		C_L = 50pF	10	-	200	600	
(LOW-HIGH) 'ropagation Delay Time (SELECT - Q)	tpLH	R_L = 5kΩ	5	-	380	1000	ns
		C_L = 50pF	10	-	140	500	
(HIGH-LOW) 'ropagation Delay Time (SELECT - Q)	tpHL	R_L = 5kΩ	5	-	200	600	
		C_L = 50pF	10	-	90	300	
(LOW-HIGH) 'ropagation Delay Time (CLEAR - Q)	tpLH	R_L = 5kΩ	5	-	550	1500	ns
		C_L = 50pF	10	-	300	900	
(HIGH-LOW) 'ropagation Delay Time (CLEAR - Q)	tpHL	R_L = 5kΩ	5	-	400	1500	
		C_L = 50pF	10	-	150	900	
lax. Clock Rise Time	$t_{r\phi}$	{EXT1, EXT2}, INT_1	5	1000	-	-	μs
lax. Clock Fall Time	$t_{f\phi}$		10	1000	-	-	
lin. Clear Pusle Width	t_w (CLEAR)		5	-	-	400	ns
			10	-	-	200	
lax. Clock Frequency	$f_{MAX\phi}$	R_L = 5kΩ	5	1.0	2.0	-	MHz
		C_L = 50pF	10	1.0	2.0	-	
lax. Clock Frequency	$f_{MAX\phi}$	R_L = 1kΩ	5	1.0	2.0	-	MHz
		C_L = 15pF	10	2.0	5.0	-	
)utput Off Capacity	C_{OUT}			-		-	pF
nput Capacity	C_{IN}			-	5	7.5	pF

TC5018P

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

TEST CIRCUIT

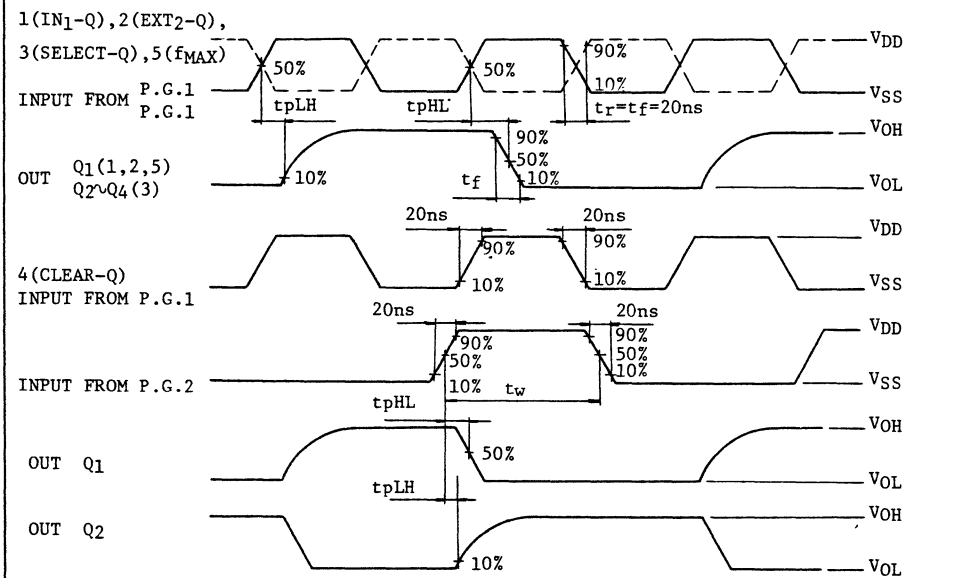


P.G.;PULSE GENERATOR
(f=500kHz,DUTY RATIO 50%)

TABLE

MEASURE MODE		INPUT MODE					
		EN	CLEAR	SELECT	EXT_1	EXT_2	INT_1
$(INT_1\text{-}Q)$ DELAY		H	L	H	L	L	P.G.1
$(EXT_2\text{-}Q)$ DELAY		L	L	H	P.G.1	$\overline{\text{P.G.1}}$	L
(SELECT-Q) DELAY		H	H	P.G.1	L	L	L
(CLEAR-Q)	t_{pLH}	H	P.G.2	L	L	L	P.G.1
	t_{pHL}	H	P.G.2	H	L	L	P.G.1
f_{MAX}		H	L	H	L	L	P.G.1

WAVEFORM

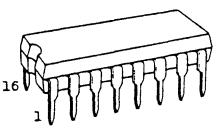


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5020BP

TC5020BP HEX LOW-TO-HIGH VOLTAGE TRANSLATOR (INVERTING)

TC5020BP contains six circuits of level converters which convert the signals from low power supply voltage logical systems to the logical signals for high power supply voltage C²MOS systems.
This is most suitable for interfacing between TTL, MDTL systems and C²MOS systems, and between two power supply voltage C²MOS systems.
Normally, V_{CC} is connected to low voltage power supply and V_{DD} is connected to high voltage power supply, however this can also operate having V_{CC} and V_{DD} common.
When the input is "H", some amount of I_{CC} flows because of circuit structure.

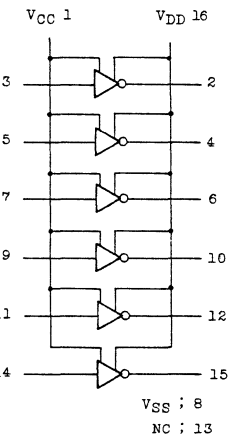


DIP16(3D16A-P)

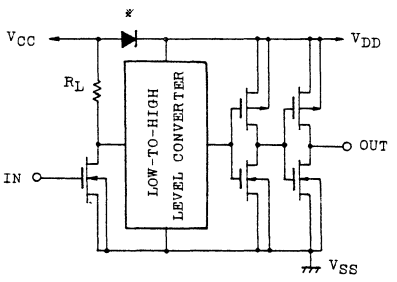
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
	V_{CC}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{CC}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

LOGIC DIAGRAM



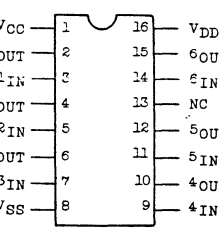
CIRCUIT DIAGRAM



$R_L \fallingdotseq 160k\Omega$

※ PARASITIC DIODE

PIN ASSIGNMENT



TC5020BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage (1)	V_{CC} V_{DD}	$V_{CC} = V_{DD}$	3	-	18	V
Supply Voltage (2)	V_{CC}	$V_{CC} < V_{DD}$	5	-	V_{DD}	V
	V_{DD}		5	-	18	
Input Voltage	V_{IN}		0	-	V_{CC}	V
Operataing Temp.	Topr		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V, V_{CC}=V_{DD})

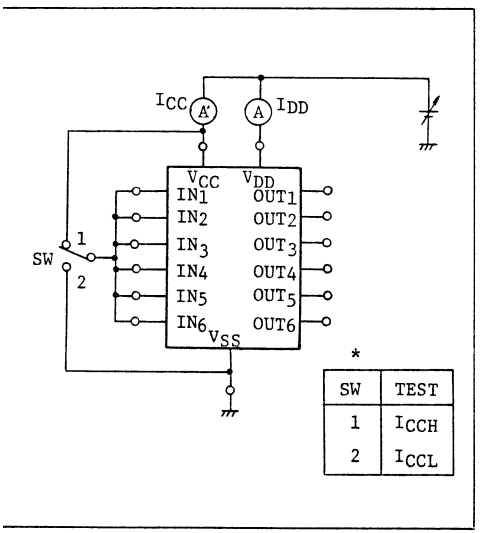
CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage		V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}$	5	4.95	-	4.95	5.00	-	4.95	-	V
				10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
				10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
High Level Output Current		I_{OH}	V_{OH} = 4.6V	5	-0.2	-	-0.16		-	-0.12	-	mA
			V_{OH} = 9.5V	10	-0.5	-	-0.4		-	-0.3	-	
			V_{OH} = 13.5V $V_{IN} = V_{SS}$	15	-1.4	-	-1.2		-	-1.0	-	
Low Level Output Current		I_{OL}	V_{OL} = 0.4V	5	0.52	-	0.44		-	0.36	-	
			V_{OL} = 0.5V	10	1.3	-	1.1		-	0.9	-	
			V_{OL} = 1.5V $V_{IN} = V_{DD}$	15	3.6	-	3.0		-	2.4	-	
High Level Input Voltage		V_{IH}	V_{OUT} = 0.5V	5	4.0	-	4.0		-	4.0	-	V
			V_{OUT} = 1.0V	10	7.0	-	7.0		-	7.0	-	
			V_{OUT} = 1.5V $\|I_{OUT}\| < 1\mu A$	15	10.0	-	10.0		-	10.0	-	
Low Level Input Voltage		V_{IL}	V_{OUT} = 4.5V	5	-	1.0	-		1.0	-	1.0	
			V_{OUT} = 9.0V	10	-	1.2	-		1.2	-	1.2	
			V_{OUT} = 13.5V $\|I_{OUT}\| < 1\mu A$	15	-	1.5	-		1.5	-	1.5	
Input Current	H Level	I_{IH}	V_{IH} = 18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	L Level	I_{IL}	V_{IL} = 0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Current Consumption		I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ *	5	-	1.0	-	0.001	1.0	-	7.5	μA
				10	-	2.0	-	0.001	2.0	-	15.0	
				15	-	4.0	-	0.002	4.0	-	30.0	
Quiescent Current Consumption		I_{CCH}	$V_{IN} = V_{DD}$	5	-	0.9	-	0.2	0.48	-	0.9	mA
				10	-	1.6	-	0.4	0.96	-	1.6	
				15	-	2.1	-	0.6	1.5	-	2.1	
Quiescent Current Consumption		I_{CCL}	$V_{IN} = V_{SS}$	5	-	1.0	-	0.001	1.0	-	7.5	μA
				10	-	2.0	-	0.001	2.0	-	15.0	
				15	-	4.0	-	0.002	4.0	-	30.0	

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	CONDITIONS	V_{CC}(V)	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_r		-	5	-	130	400	ns
			-	10	-	65	200	
			-	15	-	50	160	
Output Fall Time	t_f		-	5	-	100	200	
			-	10	-	50	100	
			-	15	-	40	80	
(LOW-HIGH) Propagation Delay Time	t_{pLH}		5	5	-	780	1600	ns
			10	10	-	330	800	
			15	15	-	230	600	
			5	10	-	750	1600	
			5	15	-	850	1800	
			10	15	-	330	800	
(HIGH-LOW) Propagation Delay Time	t_{pHL}		5	5	-	220	600	
			10	10	-	75	300	
			15	15	-	50	200	
			5	10	-	130	300	
			5	15	-	150	400	
			10	15	-	60	200	
Input Capacity	C_{IN}				-	5	7.5	pF

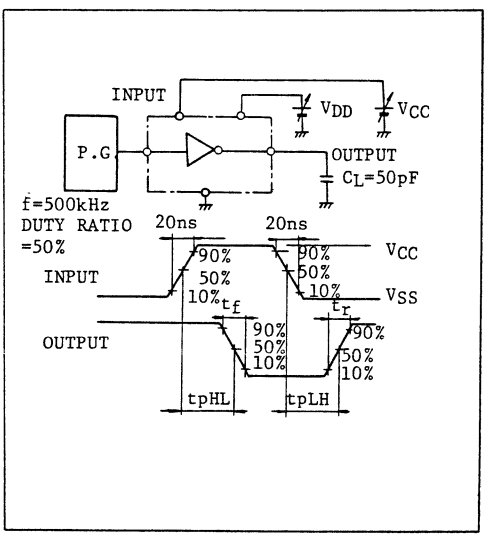
I_{DD}, I_{CC} TEST CIRCUIT



*

SW	TEST
1	I_{CCH}
2	I_{CCL}

SWITCHING TIME TEST CIRCUIT AND WAVEFORM



TC5023BP

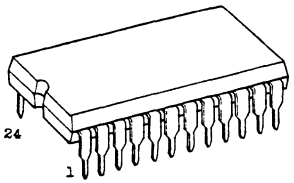
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5023BP 16-LINE DATA SELECTOR/MULTIPLEXER

TC5023BP is data selector which selects one of 16 input signals $X_0 \sim X_{15}$ according to binary address inputs A, B, C and D.

The data input (X_n) which corresponds to the binary address appears inverted on output $\overline{Z}$.

If STROBE input is set to "H", output $\overline{Z}$ becomes "H" regardless of other inputs.

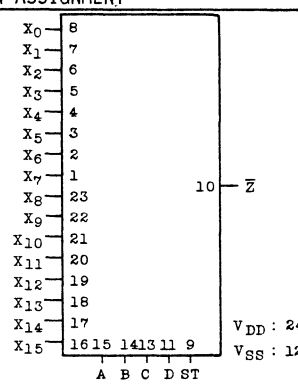


DIP 24 (6D24A-P)

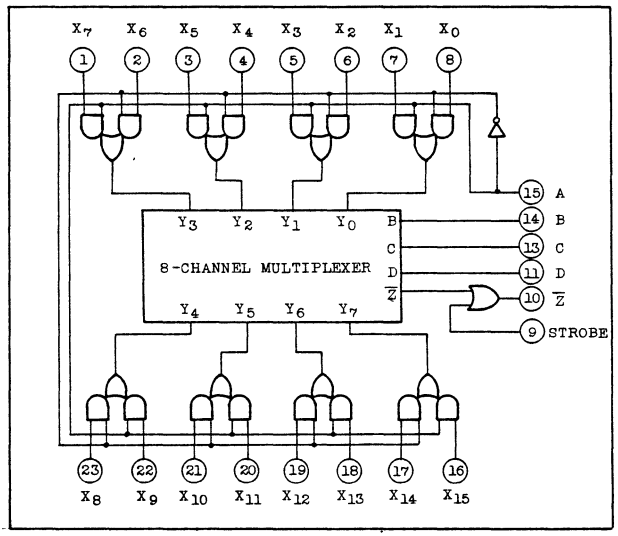
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	Tstg	-65 ~ 150	°C
Lead Temp./Time	Tsol	260°C · 10sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

INPUTS					OUTPUT
D	C	B	A	ST	$\overline{Z}$
*	*	*	*	H	H
L	L	L	L	L	$\overline{X_0}$
L	L	L	H	L	$\overline{X_1}$
L	L	H	L	L	$\overline{X_2}$
L	L	H	H	L	$\overline{X_3}$
L	H	L	L	L	$\overline{X_4}$
L	H	L	H	L	$\overline{X_5}$
L	H	H	L	L	$\overline{X_6}$
L	H	H	H	L	$\overline{X_7}$
H	L	L	L	L	$\overline{X_8}$
H	L	L	H	L	$\overline{X_9}$
H	L	H	L	L	$\overline{X_{10}}$
H	L	H	H	L	$\overline{X_{11}}$
H	H	L	L	L	$\overline{X_{12}}$
H	H	L	H	L	$\overline{X_{13}}$
H	H	H	L	L	$\overline{X_{14}}$
H	H	H	H	L	$\overline{X_{15}}$

* Don't Care

TC5023BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temp.	Topr		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
High Level Output Current	I_{OH}	V_{OH} = 4.6V V_{OH} = 9.5V V_{OH} = 13.5V $V_{IN} = V_{SS}, V_{DD}$	5	-0.2	-	-0.16		-	-0.12	-	mA
			10	-0.5	-	-0.4		-	-0.3	-	
			15	-1.4	-	-1.2		-	-1.0	-	
Low Level Output Current	I_{OL}	V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V $V_{IN} = V_{SS}, V_{DD}$	5	0.52	-	0.44		-	0.36	-	
			10	1.3	-	1.1		-	0.9	-	
			15	3.6	-	3.0		-	2.4	-	
High Level Input Voltage	V_{IH}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\| < 1\mu A$	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
Low Level Input Voltage	V_{IL}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\| < 1\mu A$	5	-	1.5	-	2.25	1.5	-	1.5	
			10	-	3.0	-	4.5	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
Input Current High Level	I_{IH}	V_{IH} = 18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current Low Level	I_{IL}	V_{IL} = 0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ *	5	-	20	-	0.005	20	-	150	μA
			10	-	40	-	0.010	40	-	300	
			15	-	80	-	0.015	80	-	600	

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	tr		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Fall Time	tf		5	-	100	200	
			10	-	50	100	
			15	-	40	80	

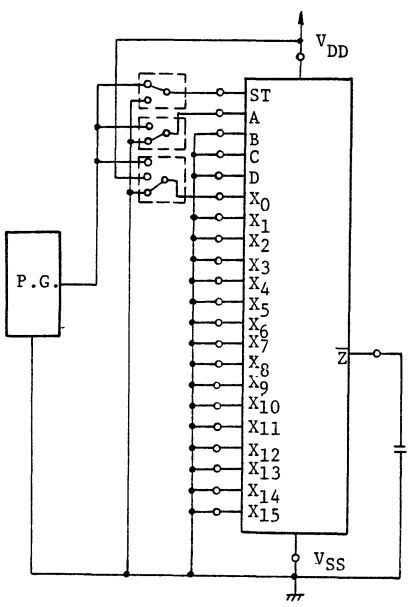
TC5023BP

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
(LOW-HIGH) Propagation Delay Time (X_n,A,B,C,D - $\overline{Z}$)	tpLH		5	-	900	1800	ns
			10	-	370	800	
			15	-	250	550	
(HIGH-LOW) Propagation Delay Time (X_n,A,B,C,D - $\overline{Z}$)	tpHL		5	-	650	1400	
			10	-	260	600	
			15	-	190	400	
(LOW-HIGH) Propagation Delay Time (STROBE - $\overline{Z}$)	tpLH		5	-	280	600	ns
			10	-	130	300	
			15	-	100	250	
(HIGH-LOW) Propagation Delay Time (STROBE - $\overline{Z}$)	tpHL		5	-	800	1600	
			10	-	340	700	
			15	-	230	500	
Input Capacity	C_{IN}	All Inputs		-	5	7.5	pF

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

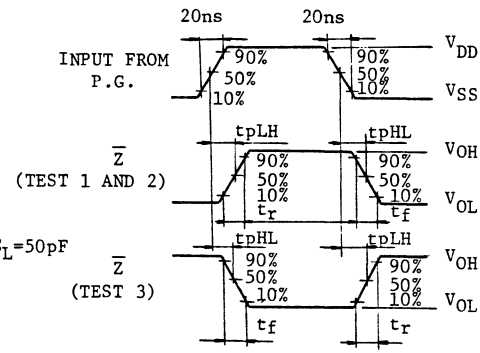
TEST CIRCUIT



TEST CONDITION

TEST	STROBE	A	X0
1	P.G.	V_{SS}	V_{DD}
2	V_{SS}	P.G.	V_{DD}
3	V_{SS}	V_{SS}	P.G.

WAVEFORM



P.G.: PULSE GENERATOR DUTY RATIO = 50%,

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

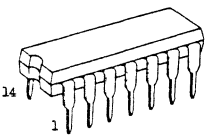
TC5024BP
TC5025BP

TC5024BP QUAD BUS BUFFER WITH 3-STATE OUTPUT ("H"-DISABLE)
TC5025BP QUAD BUS BUFFER WITH 3-STATE OUTPUT ("L"-DISABLE)

TC5024BP/TC5025BP contain four circuits of buffers having tri-state outputs. As all the buffers are controlled by four independent DISABLE inputs, any buffer outputs can be placed in the high impedance state.

The output becomes high impedance with DIS="H" for TC5024BP and $\overline{DIS}$="L" for TC5025BP.

Large output current enables to directly drive one TTL. These can be utilized as interfaces with system bus lines, multiplexers, etc.

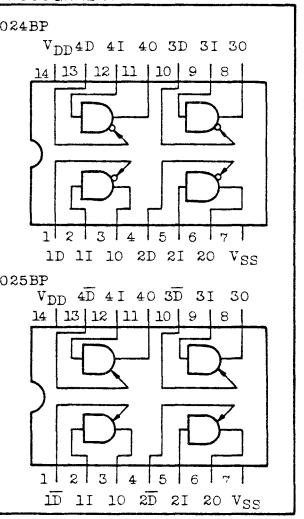


DIP 14 (3D14A-F)

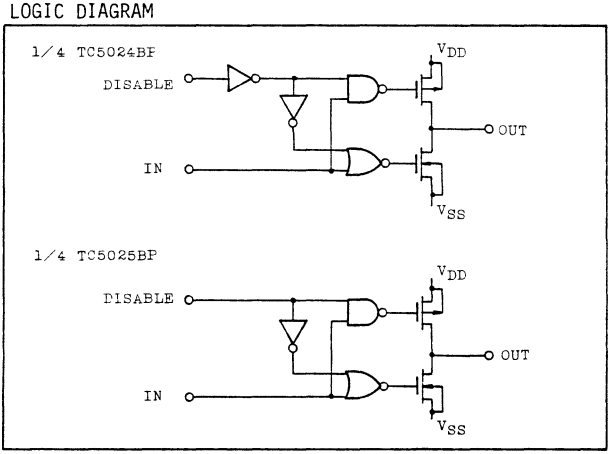
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

TC5024BP			TC5025BP		
INPUTS		OUTPUT	INPUTS		OUTPUT
IN	DIS	OUT	IN	$\overline{DIS}$	OUT
L	L	L	L	L	HZ
H	L	H	H	L	HZ
L	H	HZ	L	H	L
H	H	HZ	H	H	H

HZ ; HIGH IMPEDANCE

TC5024BP, TC5025BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temp.	Topr		-40	-	85	°C

ELECTRICAL CHARACTERISCS (V_{SS}=0V)

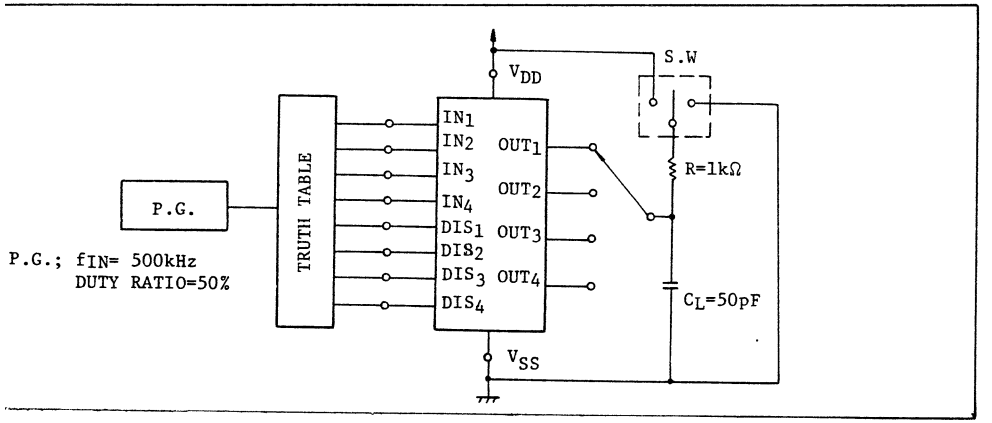
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ V_{IN} = V_{SS},V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ V_{IN} = V_{SS},V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
High Level Output Current	I_{OH}	V_{OH} = 2.5V V_{OH} = 9.5V V_{OH} = 13.5V V_{IN} = V_{SS},V_{DD}	5	-1.40	-	-1.25		-	-1.0	-	mA
			10	-1.40	-	-1.25		-	-1.0	-	
			15	-4.00	-	-3.75		-	-3.0	-	
Low Level Output Current	I_{OL}	V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V V_{IN} = V_{SS},V_{DD}	5	3.5	-	3.2		-	2.5	-	
			10	6.0	-	5.0		-	3.6	-	
			15	26.0	-	24.0		-	18.0	-	
High Level Input Voltage (IN, TC5024BP DISABLE)	V_{IH}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\| < 1\mu A$	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
Low Level Input Voltage (IN, TC5024BP DISABLE)	V_{IL}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\| < 1\mu A$	5	-	1.5	-	2.25	1.5	-	1.5	
			10	-	3.0	-	4.5	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
High Level Input Voltage (TC5025BP DISABLE)	V_{IH}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\| < 1\mu A$	5	4.0	-	4.0		-	4.0	-	V
			10	8.0	-	8.0		-	8.0	-	
			15	12.5	-	12.5		-	12.5	-	
Low Level Input Voltage (TC5025BP DISABLE)	V_{IL}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\| < 1\mu A$	5	-	1.0	-		1.0	-	1.0	
			10	-	2.0	-		2.0	-	2.0	
			15	-	2.5	-		2.5	-	2.5	
Input Current H Level	I_{IH}	V_{IH} = 18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current L Level	I_{IL}	V_{IL} = 0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Disable Current H Level	I_{DH}	V_{OH} = 18V	18	-	0.5	-	10^{-4}	0.5	-	30	μA
Disable Current L Level	I_{DL}	V_{OL} = 0V	18	-	-0.5	-	-10^{-4}	-0.5	-	-30	
Quiescent Current Consumption	I_{DD}	V_{IN} = V_{SS},V_{DD} *	5	-	4.0	-	0.002	4.0	-	30	μA
			10	-	8.0	-	0.004	8.0	-	60	
			15	-	16.0	-	0.008	16.0	-	120	

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD} (V)	TC5024BP MIN.	TC5024BP TYP.	TC5024BP MAX.	TC5025UBP MIN.	TC5025UBP TYP.	TC5025UBP MAX.	UNIT
Output Rise Time		t_r		5	-	130	400	-	130	400	ns
				10	-	65	200	-	65	200	
				15	-	50	160	-	50	160	
Output Fall Time		t_f		5	-	100	200	-	100	200	
				10	-	50	100	-	50	100	
				15	-	40	80	-	40	80	
(LOW-HIGH) Propagation Delay Time (IN - OUT)		t_{pLH}		5	-	150	300	-	150	300	ns
				10	-	75	150	-	75	150	
				15	-	60	100	-	60	100	
(HIGH-LOW) Propagation Delay Time (IN - OUT)		t_{pHL}		5	-	180	300	-	180	300	
				10	-	75	150	-	75	150	
				15	-	60	100	-	60	100	
Three State Propagation Delay Time	H-HZ	t_{pHZ}		5	-	95	200	-	70	150	ns
				10	-	50	120	-	50	100	
				15	-	40	100	-	40	80	
	L-HZ	t_{pLZ}		5	-	300	600	-	130	200	
				10	-	200	400	-	70	150	
				15	-	190	300	-	60	120	
	HZ-H	t_{pZH}		5	-	100	200	-	70	150	ns
				10	-	40	120	-	40	80	
				15	-	30	100	-	30	70	
	HZ-L	t_{pZL}		5	-	210	600	-	130	200	
				10	-	90	300	-	60	150	
				15	-	60	200	-	40	120	
Input Capacity		C_{IN}			-	5	7.5	-	5	7.5	pF
Output Disable Capacity		C_{OUT}			-	30	-	-	30	-	pF

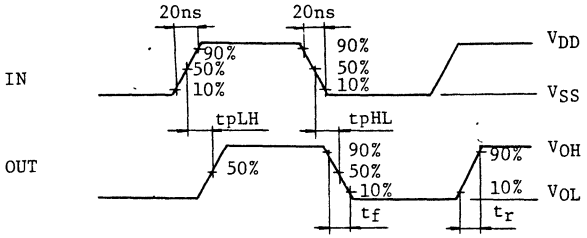
SWITCHING TIME TEST CIRCUIT



TC5024BP, TC5025BP

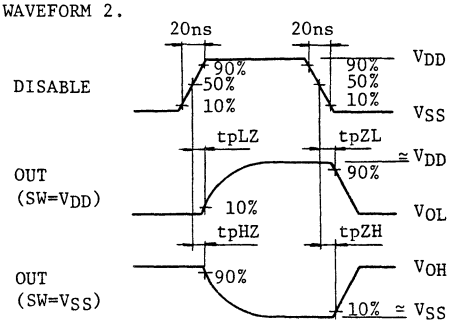
SWITCHING TIME TEST WAVEFORMS

WAVEFORM 1.



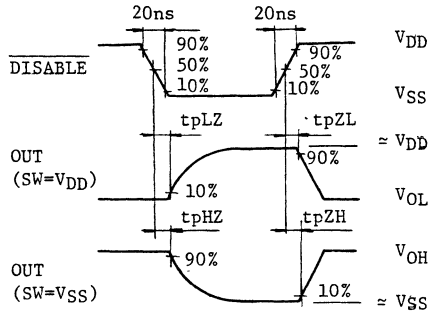
TC5024BP; DISABLE="L"/TC5025BP; $\overline{\text{DISABLE}}$="H"

WAVEFORM 2.



TC5024BP

WAVEFORM 3.



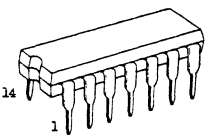
TC5025BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5026BP

TC5026BP DECADE COUNTER

TC5026BP is DECADE UP COUNTER with two reset functions, RESET (9) and RESET (0) and can be used as binary counter, quinary counter or decimal counter. When two inputs of RESET (0) are set to "H", the content of counter is reset to 0 regardless of the clock and when two inputs of RESET (9) are set to "H", it is set to 9.
RESET (9) takes precedance over RESET (0).
The outputs change their states at the falling edge of count inputs (IN_A and IN_B).

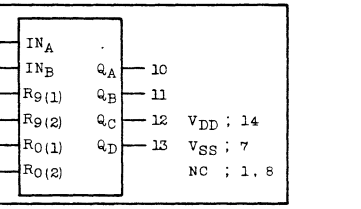


DIP 14 (3D14A-P)

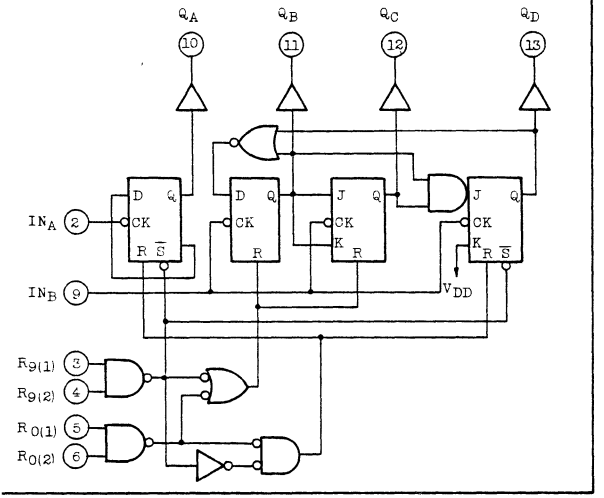
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

RESET / COUNT MODE

INPUTS					OUTPUTS			
IN_A, IN_B	$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
*	H	H	L	*	L	L	L	L
*	H	H	*	L	L	L	L	L
*	*	*	H	H	H	L	L	H
↓	*	L	*	L	COUNT			
↓	L	*	L	*	COUNT			
↓	L	*	*	L	COUNT			
↓	*	L	L	*	COUNT			

* Don't care

COUNT MODE A

COUNT NO.	OUTPUTS		
	Q_D	Q_C	Q_B
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L

A ; Separate mode.
B ; IN_B should be connected to Q_A

COUNT MODE B

COUNT NO.	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

TC5026BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temp.	Topr		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|$< 1μA V_{IN} = V_{SS}, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|$< 1μA V_{IN} = V_{SS}, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
High Level Output Current	I_{OH}	V_{OH} = 4.6V V_{OH} = 9.5V V_{OH} = 13.5V V_{IN} = V_{SS},V_{DD}	5	-0.2	-	-0.16		-	-0.12	-	mA
			10	-0.5	-	-0.4		-	-0.3	-	
			15	-1.4	-	-1.2		-	-1.0	-	
Low Level Output Current	I_{OL}	V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V V_{IN} = V_{SS},V_{DD}	5	0.52	-	0.44		-	0.36	-	
			10	1.3	-	1.1		-	0.9	-	
			15	3.6	-	3.0		-	2.4	-	
High Level Input Voltage	V_{IH}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\|$< 1μA	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
Low Level Input Voltage	V_{IL}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\|$< 1μA	5	-	1.5	-	2.25	1.5	-	1.5	
			10	-	3.0	-	4.5	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
Input Current "H" Level	I_{IH}	V_{IH} = 18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL} = 0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Current Consumption	I_{DD}	V_{IN} = V_{SS},V_{DD} *	5	-	20	-	0.005	20	-	150	μA
			10	-	40	-	0.010	40	-	300	
			15	-	80	-	0.015	80	-	600	

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

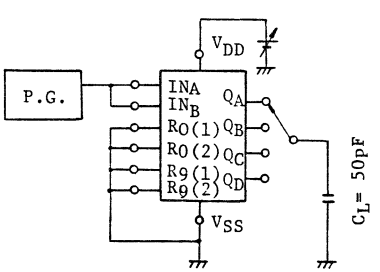
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_r		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Fall Time	t_f		5	-	100	200	
			10	-	50	100	
			15	-	40	80	

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

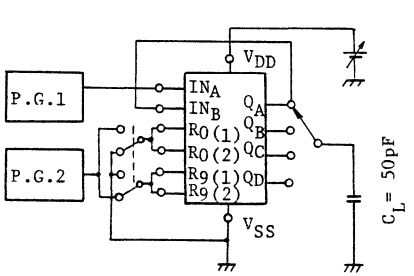
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
(LOW-HIGH) Propagation Delay Time (IN_A, IN_B - Q)	tpLH		5	-	340	750	ns
			10	-	160	350	
			15	-	130	280	
(HIGH-LOW) Propagation Delay Time (IN_A, IN_B - Q)	tpHL		5	-	310	650	
			10	-	150	330	
			15	-	120	250	
(LOW-HIGH) Propagation Delay Time ($R_{(0)}$, $R_{(9)}$ - Q)	tpLH		5	-	350	700	ns
			10	-	150	300	
			15	-	120	250	
(HIGH-LOW) Propagation Delay Time ($R_{(0)}$, $R_{(9)}$ - Q)	tpHL		5	-	350	700	
			10	-	150	300	
			15	-	120	250	
Max. Clock Rise Time	trØ		5	20	-		μs
Max. Clock Fall Time	tfØ		10	2.5	-		
			15	1.0	-		
Max. Clock Frequency (IN_A, IN_B)	fMAXØ		5	0.8	1.2	-	MHz
			10	1.5	2.5	-	
			15	2.0	3.2	-	
Min. Reset Pulse Width	t_w (RESET)		5	-	250	500	ns
			10	-	100	200	
			15	-	75	150	
Input Capacity	C_{IN}			-	5	7.5	pF

SWITCHING TIME TEST CIRCUIT

TEST CIRCUIT 1 tpLH,tpHL(IN_A,IN_B-Q) $f_{MAXØ}$



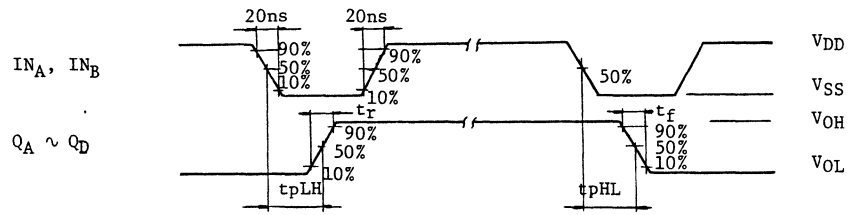
TEST CIRCUIT 2 tpLH,tpHL(R_0,R_9-Q) t_w



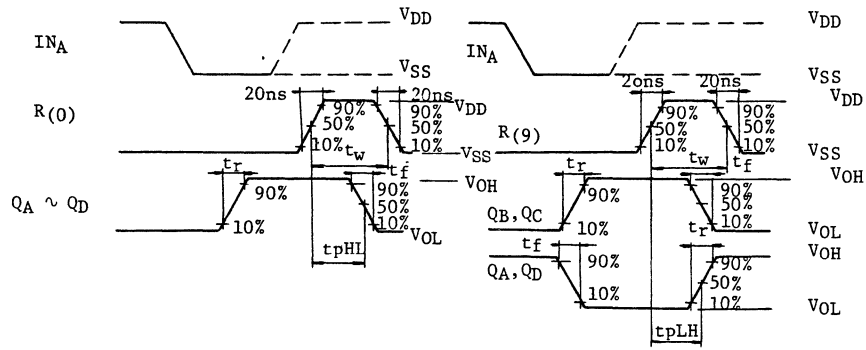
TC5026BP

SWITCHING TIME TEST WAVEFORMS

WAVEFORM 1. tpLH, tpHL (IN_A,IN_B - Q), $f_{MAX\emptyset}$



WAVEFORM 2. tpLH, tpHL [R(0),R(9) - Q], t_w



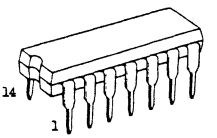
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5027BP

TC5027BP BINARY COUNTER

TC5027BP is four bit binary up counter with the reset function and since the clock for the first stage is independent from the clock for the second through the fourth stages, this can be used as binary, octal or hexadecimal counter/divider.

When two inputs of RESET(0) are set to "H", the content of counter is reset to 0 regardless of the clock. The outputs change their states at the falling edge of count inputs (IN_A, IN_B).

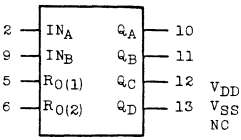


DIP 14 (3D14A-P)

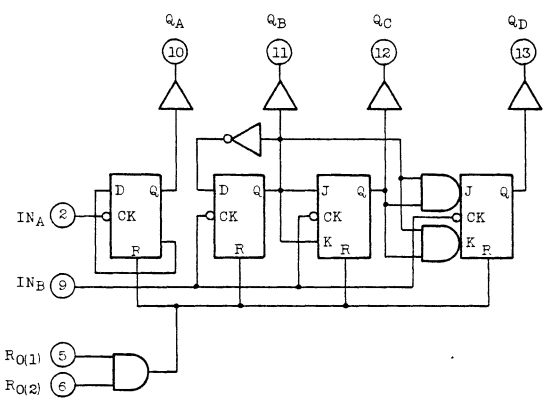
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

RESET / COUNT MODE

INPUTS			OUTPUT			
IN_A . IN_B	$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
*	H	H	L	L	L	L
↓	L	*	COUNT			
↓	*	L	COUNT			

* Don't care

COUNT MODE A

COUNT NO.	OUTPUTS		
	Q_C	Q_B	Q_A
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L
5	H	L	H
6	H	H	L
7	H	H	H

A ; Separate mode.

B , IN_B should be connected to Q_A.

COUNT MODE B

COUNT NO.	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

TC5027BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	3	-	18	V
Input Voltage	V_{IN}	0	-	V_{DD}	V
Operating Temp.	Topr	-40	-	85	°C

ELECTRICAL CHALACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
High Level Output Current	I_{OH}	V_{OH} = 4.6V V_{OH} = 9.5V V_{OH} = 13.5V $V_{IN}=V_{SS},V_{DD}$	5	-0.2	-	-0.16		-	-0.12	-	mA
			10	-0.5	-	-0.4		-	-0.3	-	
			15	-1.4	-	-1.2		-	-1.0	-	
Low Level Output Current	I_{OL}	V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V $V_{IN}=V_{SS},V_{DD}$	5	0.52	-	0.44		-	0.36	-	
			10	1.3	-	1.1		-	0.9	-	
			15	3.6	-	3.0		-	2.4	-	
High Level Input Voltage	V_{IH}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\|<1\mu A$	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
Low Level Input Voltage	V_{IL}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\|<1\mu A$	5	-	1.5	-	2.25	1.5	-	1.5	
			10	-	3.0	-	4.5	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
Input Current "H" Level	I_{IH}	V_{IH} = 18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL} = 0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	20	-	0.005	20	-	150	μA
			10	-	40	-	0.010	40	-	300	
			15	-	80	-	0.015	80	-	600	

*All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_r		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Fall Time	t_f		5	-	100	200	
			10	-	50	100	
			15	-	40	80	

TC5027BP

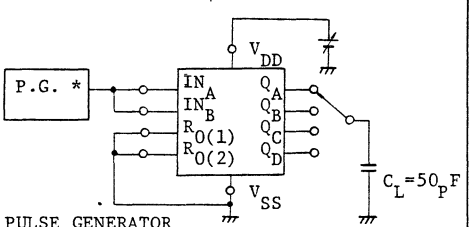
WITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=OV, C_L=50$_P$F)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}	MIN.	TYP.	MAX.	UNIT
Low-High) Propagation elay Time (IN_A, IN_B - Q)	t_{pLH}		5 10 15	- - -	340 160 130	750 350 280	ns
High-Low) Propagation elay Time (IN_A, IN_B - Q)	t_{pHL}		5 10 15	- - -	310 150 120	650 330 250	ns
High-Low) Propagation elay Time R_O - Q)	t_{pHL}		5 10 15	- - -	250 120 100	700 300 250	ns
ax. Clock Rise Time ax. Clock Fall Time	$t_{r\phi}$ $t_{f\phi}$		5 10 15	20 2.5 1.0	- - -	- - -	μs
ax. Clock Frequency (IN_A, IN_B)	$f_{MAX\phi}$		5 10 15	0.8 1.5 2.0	1.2 2.5 3.2	- - -	MHz
in. Reset Pulse Width	t_w (RESET)		5 10 15	- - -	250 110 80	500 200 150	ns
nput Capacitance	C_{IN}		-		5	-	pF

WITCHING TIME TEST CIRCUITS

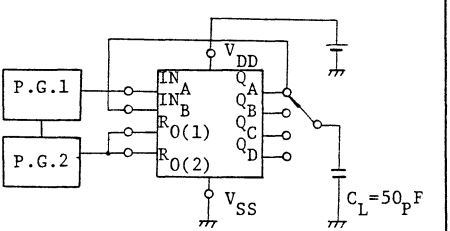
EST CIRCUIT 1. t_{pLH}, t_{pHL} (IN_A, IN_B-Q)

$f_{MAX\phi}$-1



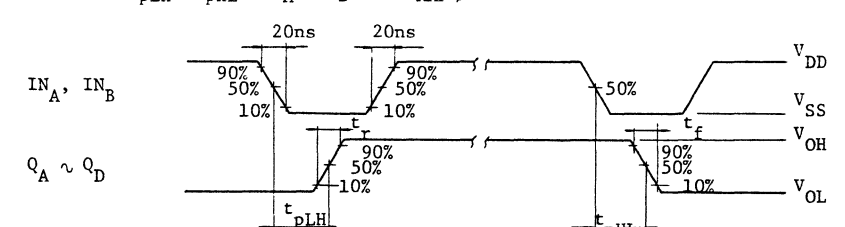
: PULSE GENERATOR

TEST CIRCUIT 2. t_{pHL} (R_O-Q), t_w



WITCHING TIME TEST WAVEFORMS

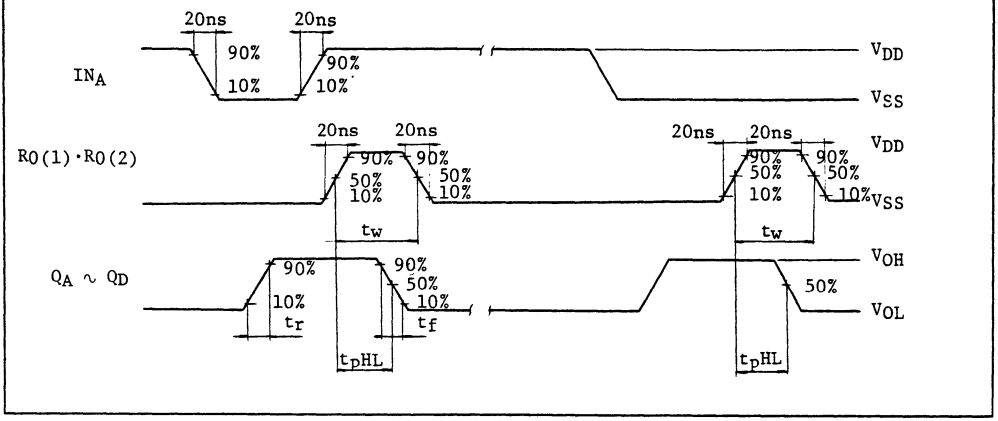
AVEFORM 1. t_{pLH}, T_{pHL} (IN_A, IN_B-Q), $f_{MAX\phi}$



TC5027BP

SWITCHING TIME TEST WAVEFORMS

WAVEFORM 2. t_{pHL} (R_0 - Q), t_w ,



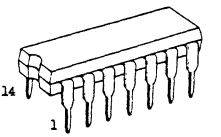
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5029BP

TC5029BP QUAD 2-INPUT NAND GATE WITH N-CHANNEL OPEN DRAIN OUTPUT

TC5029BP contains four circuits of 2 input NAND gates having its respective outputs of N-channel open drain structure.

Since the drain voltage of output transistors are guaranteed up to 26 volts, these can be used for wide range of applications such as level shifters and drivers, and the wired OR arrangement is also easily obtained. Please utilize these for level shifters for P-channel MOS, controlling analog switches of positive/negative power supplies, etc.

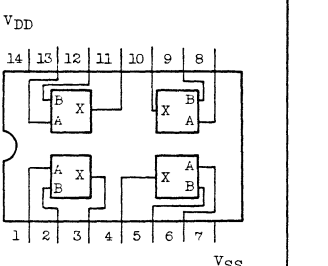


DIP 14 (3D14A-P)

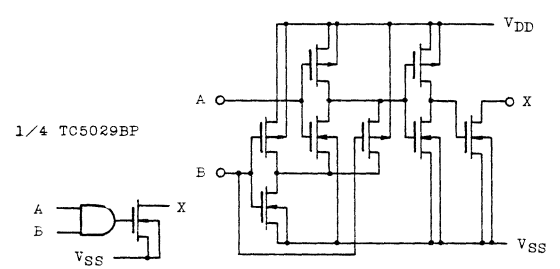
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{SS}+26	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



CIRCUIT DIAGRAM



TRUTH TABLE

INPUTS		OUTPUT
B	A	X
L	L	HZ
L	H	HZ
H	L	HZ
H	H	L

HZ ; HIGH IMPEDANCE

TC5029BP

RECOMMENDED OPERATION CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Output Voltage	V_{OUT}		0	-	24	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Low Level Output Voltage		V_{OL}	I_{OUT} <1μA $V_{IN}=V_{SS},V_{DD}$	5 10 15	- - -	0.05 0.05 0.05	- - -	0.00 0.00 0.00	0.05 0.05 0.05	- - -	0.05 0.05 0.05	V
Low Level Output Current		I_{OL}	V_{OL}=0.4V V_{OL}=0.5V V_{OL}=1.5V $V_{IN}=V_{SS},V_{DD}$	5 10 15	3.2 5.0 24.0	- - -	3.2 5.0 24.0		- - -	2.5 3.6 18.0	- - -	mA
High Level Input Voltage **		V_{IH}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V I_{OUT} <1μA	5 10 15	3.5 7.0 11.0	- - -	3.5 7.0 11.0	2.75 5.5 8.25	- - -	3.5 7.0 11.0	- - -	V
Low Level Input Voltage **		V_{IL}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V I_{OUT} <1μA	5 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.5 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	
Output off Leakage Current		I_{DH}	V_{OH}=24V	-	-	0.5	-	10^{-3}	0.5	-	50	μA
Input Current	High Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	Low Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Current Consumption		I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5 10 15	- - -	1.0 2.0 4.0	- - -	0.001 0.001 0.002	1.0 2.0 4.0	- - -	7.5 15 30	μA

* All valid input combinations. Outputs open.

** R_L=20KΩ

TC5029BP

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V)

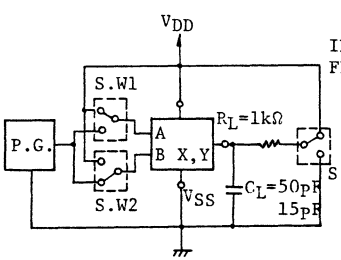
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Fall Time	t_f	C_L=50pF	5	-	85	200	ns
			10	-	30	80	
			15	-	20	60	
(Low-High) Propagation Delay Time	t_{pLH}	R_L=1KΩ, C_L=15pF	5	-	230	500	ns
			10	-	120	200	
			15	-	100	150	
(High-Low) Propagation Delay Time	t_{pHL}	R_L=1KΩ, C_L=15pF	5	-	260	500	
			10	-	90	200	
			15	-	60	150	
(Low-High) Propagation Delay Time	t_{pLH}	R_L=10KΩ, C_L=15pF	5	-	830	1200	ns
			10	-	680	1000	
			15	-	610	850	
(High-Low) Propagation Delay Time	t_{pHL}	R_L=10KΩ, C_L=50pF	5	-	270	500	
			10	-	95	200	
			15	-	63	150	
Input Capacitance	C_{IN}			-	5	7.5	pF
Output Off Capacitance	C_{OUT}			-	25	-	pF

SWITCHING TIME TEST CIRCUIT AND WAVEFORM

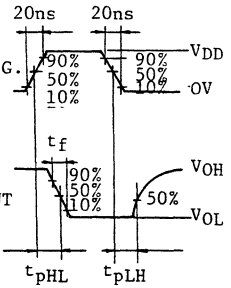
TEST CONDITION

No.	S.W1	S.W2	S.W3
1	P.G	V_{DD}	V_{DD}
2	V_{DD}	P.G	V_{DD}
3	P.G	P.G	V_{DD}

TEST CIRCUIT



WAVEFORM



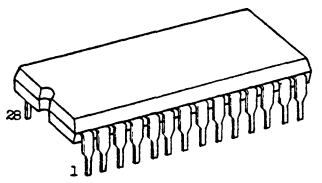
(f_{IN}=50kHz, DUTY RATIO=50%)

TC5032P

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5032P 6-DIGIT DECADE COUNTER

TC5032P is six digit decimal counter whose BCD output of each digit is dynamically output in sequence from the higher order digit on BCD OUTPUT in synchronism with SCAN input. As the carry outputs are available from all the digits, other counters and control circuits can be easily driven.
By using BC (Blanking Control) input, leading zero suppress from arbitrary digit can be achieved without external circuits.
Since the first stage counter can respond up to 10MHz (V_{DD}=5 volts), this is also suitable for counting and frequency dividing of high frequency pulses.

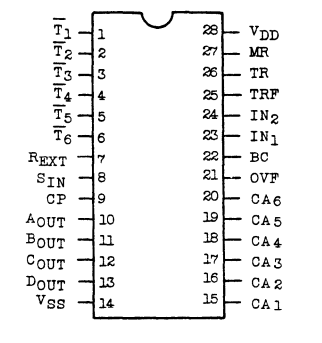


DIP 28 (6D28A-P)

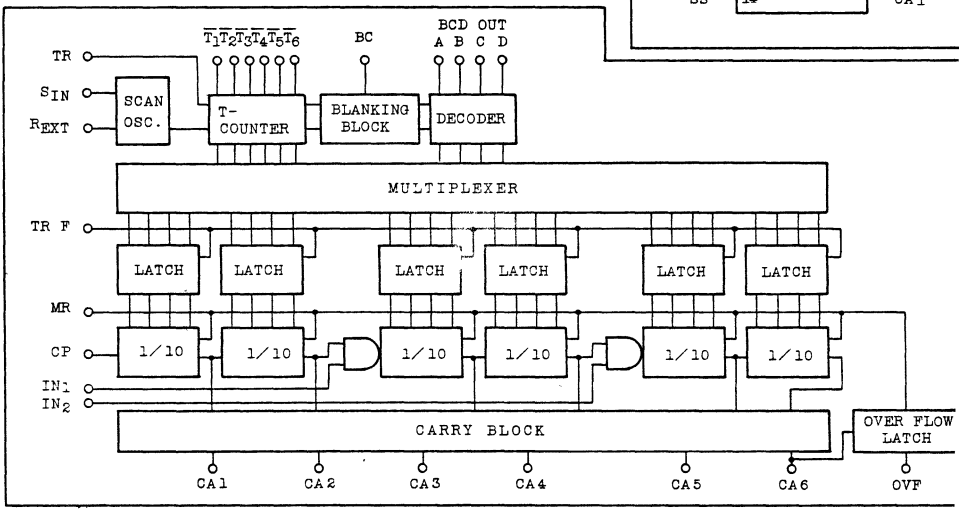
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-55 ~ 125	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



BLOCK DIAGRAM

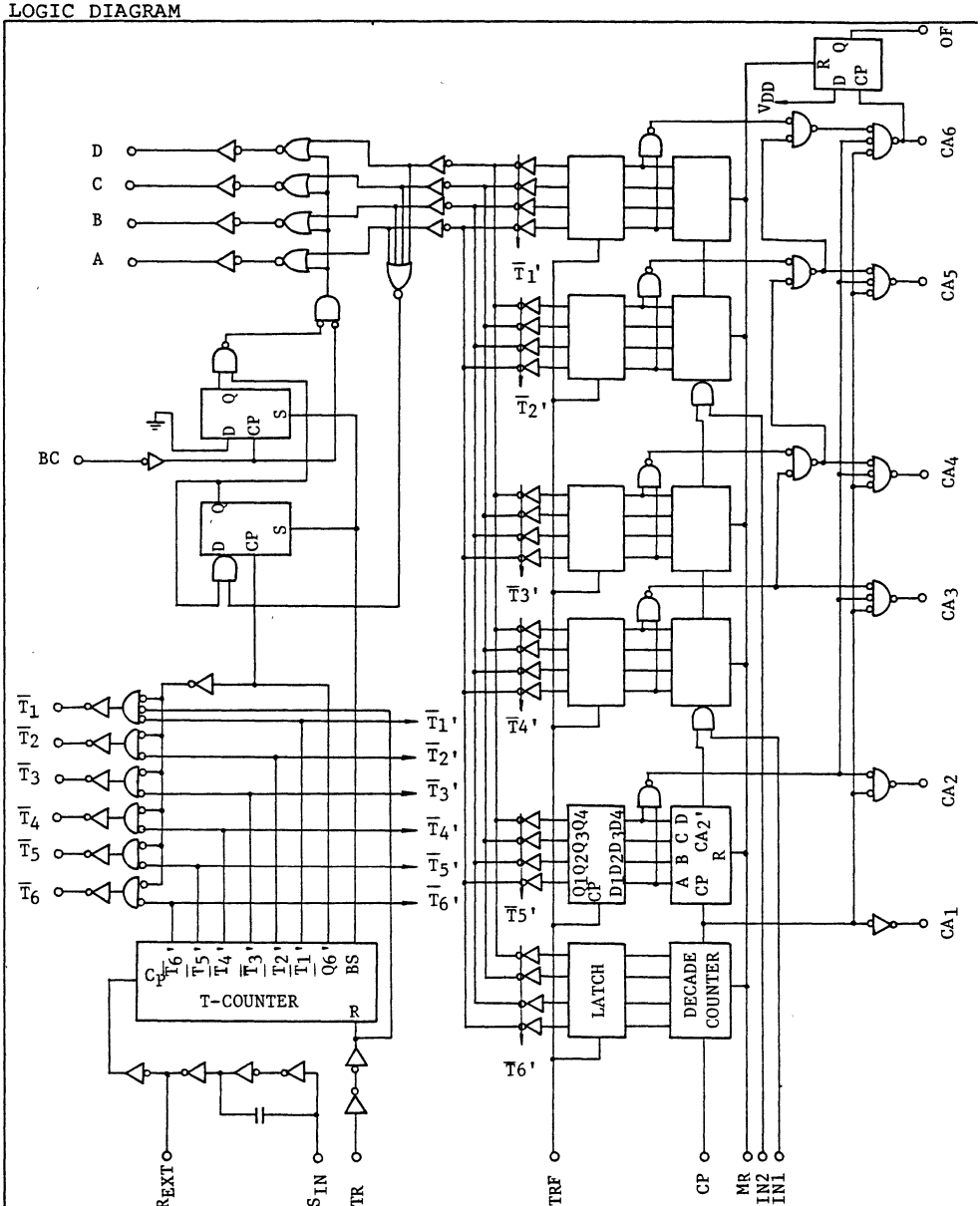


IN FUNCTION & NAME

PIN NO.	SYMBOL	NAME	FUNCTION
1	$\overline{T1}$	$\overline{T1}$	Outputs to indicate the digit of output signals A_{OUT} through D_{OUT}, the sequence is descending order from $\overline{T1}$. With TR="H", all of $\overline{T1}$ through $\overline{T6}$ become "H", and when TR falls, $\overline{T1}$ becomes "L". Then, "L" is shifted in sequence $\overline{T2}$, $\overline{T3}$ --- by each 4 clocks of S_{IN}.
2	$\overline{T2}$	$\overline{T2}$	
3	$\overline{T3}$	$\overline{T3}$	
4	$\overline{T4}$	$\overline{T4}$	
5	$\overline{T5}$	$\overline{T5}$	
6	$\overline{T6}$	$\overline{T6}$	
7	R_{EXT}	RESISTOR EXTERNAL	Leave open when an external clock is applied from S_{IN}. When no external clock is available, clock can be generated by externally connecting a resistor between S_{IN} and R_{EXT}.
8	S_{IN}	SCAN INPUT	T-COUNTER CLOCK input. T-COUNTER changes its state at the rising edge of S_{IN}.
9	CP	CLOCK INPUT	Decimal counter clock input for the lowest order digit.
10	A_{OUT}	A-OUTPUT	Decimal counter BCD output. When $\overline{T1}$="L", the highest order digit (6th digit) is output. Then, 5th digit is output with $\overline{T2}$="L", 4th digit with $\overline{T3}$="L", ---, 1st digit with $\overline{T6}$="L". During BLANKING, all the outputs become "H".
11	B_{OUT}	B-OUTPUT	
12	C_{OUT}	C-OUTPUT	
13	D_{OUT}	D-OUTPUT	
14	V_{SS}	V_{SS}	(GND)
15	CA1	CARRY 1	Carry output from n-th digit: "L" when count is "xxxxx6"~"xxxxx9", otherwise "H".
16	CA2	CARRY 2	"L" when count is "xxxx96"~"xxxx99", otherwise "H".
17	CA3	CARRY 3	"L" when count is "xxx996"~"xxx999", otherwise "H".
18	CA4	CARRY 4	"L" when count is "xx9996"~"xx9999", otherwise "H".
19	CA5	CARRY 5	"L" when count is "x99996"~"x99999", otherwise "H".
20	CA6	CARRY 6	"L" when count is "999996"~"999999", otherwise "H".
21	OVF	OVER FLOW	Detection terminal of OVER FLOW condition of counter. When the counter advances by one from "999999", it becomes "H". Once it has become "H", only MR can restore it to "L".
22	BC	BLANKING CONTROL	"H": Zero suppress for all the digits. "L": No zero suppress. If $\overline{Tn}$ is connected to BC, zero suppress is activated for the higher order digits than (n-1)th digit.
23	IN1	INPUT 1	"H": All the digits are counted. "L": Only the lower order two digits are counted.
24	IN2	INPUT 2	"H": All the digits are counted. "L": Only the lower order four digits are counted.
25	TRF	TRANSFER	"H": Decimal counter output is transferred to the multiplexer as it is. "L": Counter output at the falling edge of TRF is latched.
26	TR	T-COUNTER RESET	T-counter is initialized to T1 by "H" level input and T1 retains "H" level only for the period of TR="H".
27	MR	MASTER RESET	"H" level input resets the counter to count "000000" and OVER FLOW to "L".
28	V_{DD}	V_{DD}	V_{DD} power supply (3~8 volts)

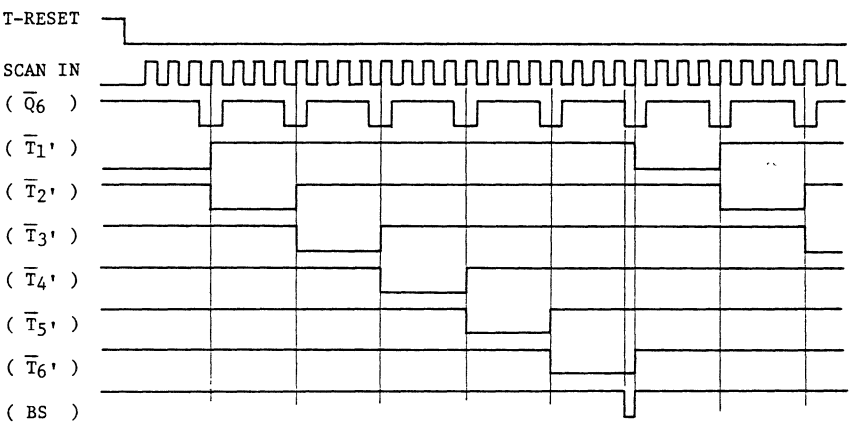
TC5032P

LOGIC DIAGRAM

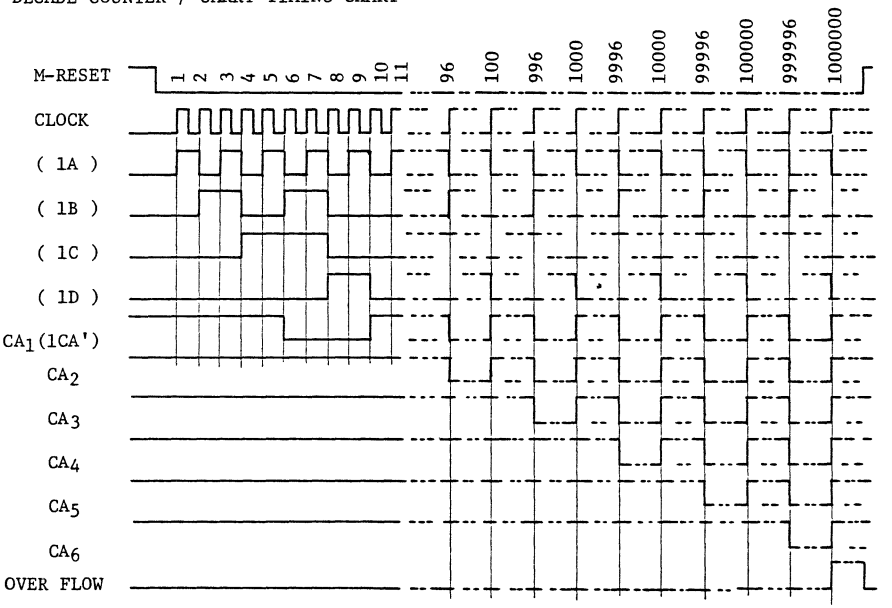


TIMING CHART

T-COUNTER TIMING CHART



DECADE COUNTER / CARRY TIMING CHART



* Waveforem marked with ( ) are timings of LSI's internals.(Refer to LOGIC DIAGRAM)

TC5032P

OPERATING CONSIDERATION

* Count Operation

Set input terminals IN1, IN2 and TRANSFER to "H" and apply "H" level to M-RESET terminal, then return it to "L" level. If pulse is fed to CLOCK terminal in this condition, the counter advances its count at the rising edge of CLOCK up to 999999.

Since CARRY outputs from all the digits are output in negative logic, the control of other CMOS logics can be easily achieved.

$\overline{CA1}$ - $\overline{CA6}$ are output with "L" level for four clock periods. (Refer to the timing chart.)

If one more clock is given in the count of 999999, OVER FLOW terminal becomes "H" indicating the overflow condition of COUNTER. Once OVER FLOW terminal has become "H", it will never return to "L" unless M-RESET is applied.

* Latch Operation

When the level of TRANSFER terminal is "H", the counter output is transferred to the multiplexer as it is with the output always indicating the counter output, but if TRANSFER terminal changes the level from "H" to "L", the count output which has been being output immediately prior to the falling edge of TRANSFER is stored in the latch and even if the counter output varies, A_{OUT} - D_{OUT} will not vary.

If TRANSFER terminal is returned to "H" again, the correct counter output appears on A_{OUT} - D_{OUT}.

* Scan Operation

BCD outputs of all digits are output to common A_{OUT} - D_{OUT} on the time sharing basis and the basic clock for this operation is fed from outside to SCAN IN (leaving R_{EXT} open in this case) or obtained by connecting a resistor between R_{EXT} and SCAN IN.

BCD output for each digit appears on A_{OUT} - D_{OUT} corresponding to each digit of 6 digit scan signals (digit signals) which are in synchronism with the rising edge of SCAN IN. The digit output for digit selection is output with "L" level on $\overline{T1}$ - $\overline{T6}$. As BCD outputs are output starting from the highest order digit ($\overline{T1}$ — 6th digit, ... $\overline{T6}$ — 1st digit), data transfer can be easily achieved.

* The relationship between external resistor between R_{EXT} and SCAN IN and oscillating frequency is given below

$$f \fallingdotseq \frac{1}{44 \times R} \times 10^{12} \text{ [Hz]}$$

* Blanking

By controlling BLANKING CONTROL terminal, leading zero suppress to an arbitrary digit can be easily achieved. When zero suppress is activated, all of A_{OUT} - D_{OUT} become "H".

BC Terminal and Zero Suppress

BRANKING CONTROL	Leading Zero Suppress
L	No zero suppress
H	Zero suppress for all digits *
Connected to $\overline{T_6}$	Zero suppress for five higher order digits and no zero suppress for the lowest order digit. *
Connected to $\overline{T_5}$	Zero suppress for four higher order digits and no zero suppress for two lower order digits. *
Connected to $\overline{T_4}$	Zero suppress for three higher order digits and no zero suppress for three lower order digits. *
Connected to $\overline{T_3}$	Zero suppress for two higher order digits and no zero suppress for four lower order digits. *
Connected to $\overline{T_2}$	Zero suppress for the highest order digit and no zero suppress for five lower order digits. *

* When carry is generated from lower order digit, the normal output may not be obtained only one cycle of T-COUNTER.

TC5032P

RECOMMENDED OPERATING CONDITIONS (V_{SS}=OV)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	8	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-30	-	85	°C
R_{EXT} External Registance	R_{EXT}		20K	-	10M	Ω

ELECTRICAL CHARACTERISTICS (V_{SS}=OV)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-30°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Voltage	High Level	V_{OH}	I_{OH}=-1μA	5	4.95	-	4.95	-	-	4.95	-	V
	Low Level	V_{OL}	I_{OL}=1μA	5	-	0.05	-	-	0.05	-	0.05	
Output Current	High Level	I_{OH}	V_{OH}=2.5V	5	-0.7	-	-0.6	-2	-	-0.5	-	mA
	Low Level	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44	1.3	-	0.36	-	
Input Voltage	High Level	V_{IH}	V_{OUT}=0.5V,4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
	Low Level	V_{IL}	V_{OUT}=0.5V,4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
Input Current	High Level	I_{IH}	V_{IH}=8V	8	-	0.15	-		0.15	-	1.0	μA
	Low Level	I_{IL}	V_{IL}=0V	8	-	-0.15	-		-0.15		-1.0	
Quiescent Current Consumption		I_{DD}	At all conditions	5	-	0.4	-	10^{-5}	0.4	-	0.8	mA
				8	-	0.5	-	10^{-5}	0.5	-	1.0	

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=OV, C_L=15pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (CP - BCD OUT)	t_{pLH}, t_{pHL}	($\overline{T6}$ = L)	5	-	800	2000	ns
		($\overline{T5}$ = L)	5	-	1000	2200	
		($\overline{T4}$ = L)	5	-	1250	2500	
		($\overline{T3}$ = L)	5	-	1500	3000	
		($\overline{T2}$ = L)	5	-	1750	3500	
		($\overline{T1}$ = L)	5	-	2000	4000	
Propagation Delay Time (CP - CARRY OUT)	t_{pLH}, t_{pHL}	CA1	5	-	(200)	500	ns
		CA2	5	-	(200)	500	
		CA3	5	-	(250)	750	
		CA4	5	-	(250)	750	
		CA5	5	-	(300)	1000	
		CA6	5	-	(300)	1000	
Max. Clock Rise Time / Max. Clock Fall Time	$t_{r\phi}$ / $t_{f\phi}$	CP, IN_1, IN_2	5	20	-	-	μs
Min. Clear Pulse Width	$t_{w(MR)}$	MASTER RESET	5	-	-	500	ns
	$t_{w(TR)}$	T-COUNTER RESET		-	-	400	

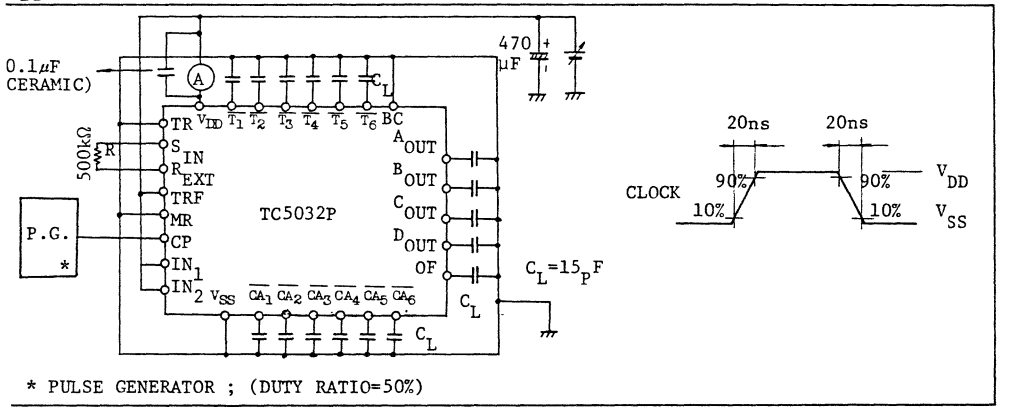
TC5032P

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=OV, C_L=15pF)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time	(High-Low)	t_{pHL}	MR-BCD OUT	5	-	-	2000	ns
	(Low-High)	t_{pLH}	TR-DIGIT OUT	5	-	-	1500	
Propagation Delay Time		t_{pLH}, t_{pHL}	SIN-BCD OUT	5	-	1000	2500	
		t_{pLH}, t_{pHL}	SIN-DIGIT OUT	5	-	500	1000	
Max. Frequency		$f_{MAX\phi-1}$	CLOCK IN *	5	10.0	14.0	-	MHz
		$f_{MAX\phi-2}$		5	1.0	2.0	-	
		f_{MAX} S_{IN}	SCAN IN	5	0.5	-	-	

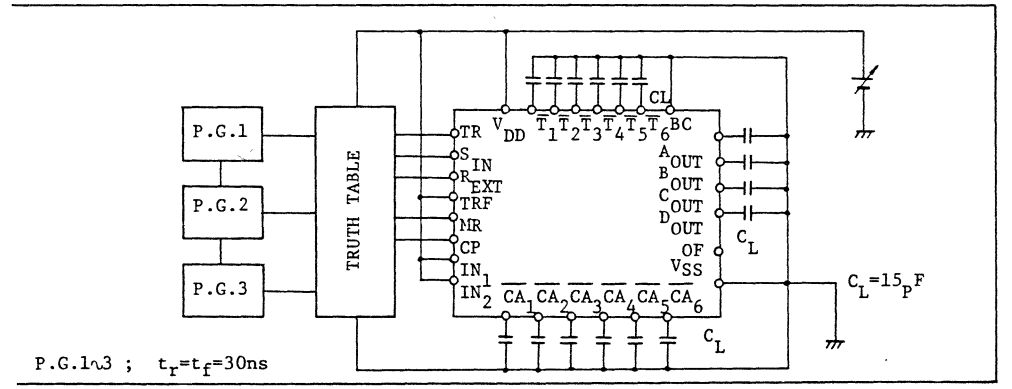
* $f_{MAX\phi-1}$; Clock burst mode. $f_{MAX\phi-2}$; BCD outputs enable.

I_{DD} TEST CIRCUIT



* PULSE GENERATOR ; (DUTY RATIO=50%)

SWITCHING TIME TEST CIRCUIT

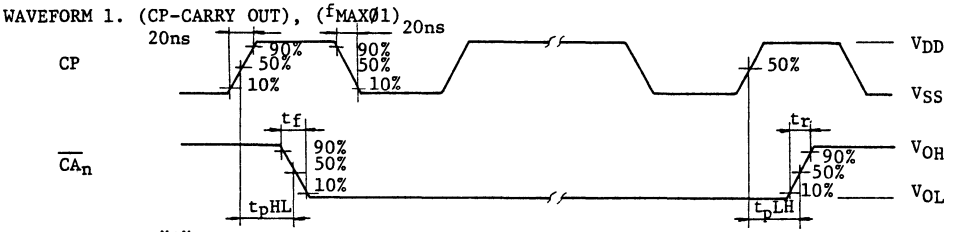


P.G.1∿3 ; t_r=t_f=30ns

TC5032P

SWITCHING TIME TEST WAVEFORMS

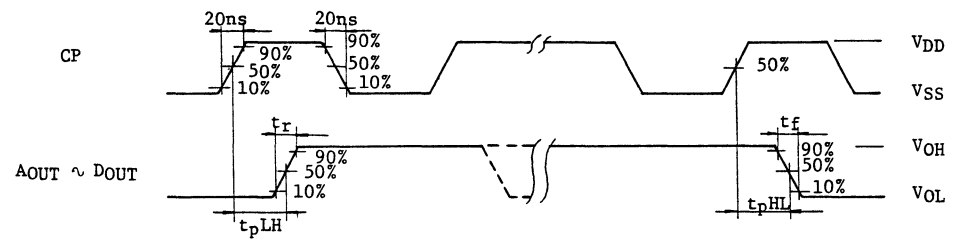
WAVEFORM 1. (CP-CARRY OUT), ($f_{MAX}/1$)



*MR, TR, S_{IN} = "L"

**CP INPUT : f=500kHz(except f_{MAX}), DUTY RATIO=50%

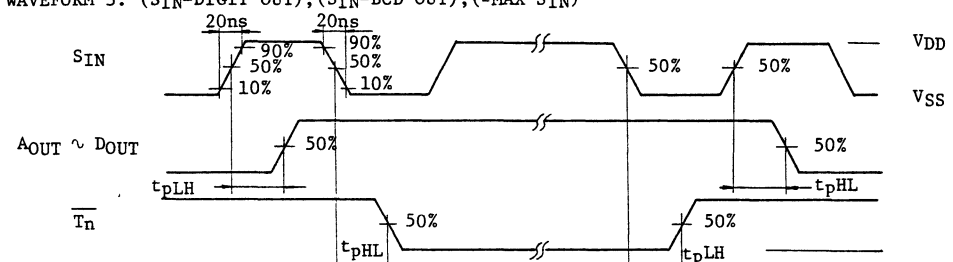
WAVEFORM 2. (CP-BCD OUT), ($f_{MAX}/2$)



* MR, TR="L" S_{IN}=MANUAL PULSE

**CP INPUT : f=250kHz (except f_{MAX}), DUTY RATIO=50%

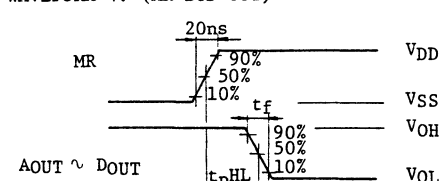
WAVEFORM 3. (S_{IN}-DIGIT OUT), (S_{IN}-BCD OUT), (f_{MAX} S_{IN})



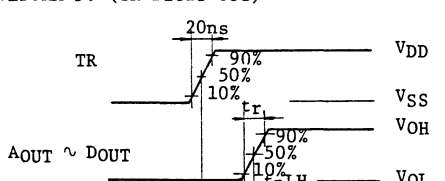
*MR, TR="L", CP : MANUAL PULSE

**S_{IN} : f=250kHz, DUTY RATIO = 50%

WAVEFORM 4. (MR-BCD OUT)



WAVEFORM 5. (TR-DIGIT OUT)



*TR="L", CP: PULSE GENERATOR, S_{IN}:MANUAL PULSE

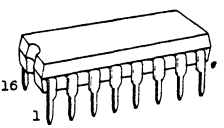
*MR="L", S_{IN}:MANUAL PULSE, CP: PULSE GENERATOR

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5036P
TC5048P

TC5036P, TC5048P 17-STAGE HIGH SPEED FREQUENCY DIVIDER

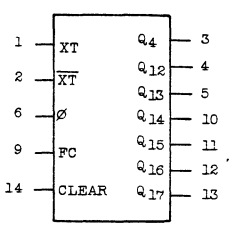
TC5036P and TC5048P are 17-stage ripple carry binary counters equipped with inverters for crystal oscillators.
As the first stage through the fourth stage are dynamic type counter, the high speed operation can be obtained but the operation starting from DC is not possible, so that these should be used in the range of $f_{MIN} \sim f_{MAX}$.
If ϕ input is opened (ϕ="L"), the inverted output of 9th stage appears on FC terminal. If ϕ input is set to "H", 9 stages from 9th stage through 17th stage can be also independently used having FC terminal as the clock input.
Outputs can be derived arbitrarily from stages 4, 12, 13, 14, 15, 16 and 17 of TC5036P and stages 4, 5, 6, 7, 14, 16 and 17 of TC5048P.



DIP16 (3D16A-P)

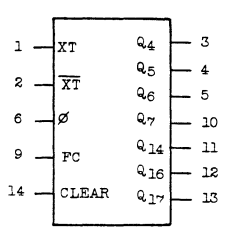
PIN ASSIGNMENT

TC5036BP



V_{DD1} ; 16 V_{SS1} ; 8
V_{DD2} ; 15 V_{SS2} ; 7

TC5048BP



V_{DD1} ; 16 V_{SS1} ; 8
V_{DD2} ; 15 V_{SS2} ; 7

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC		SYMBOL	RATING	UNIT
DC Supply Voltage		V_{DD1}	$V_{SS1}-0.5 \sim V_{SS1}+10$	V
		V_{DD2}	$V_{SS1}-0.5 \sim V_{DD1}+0.5$	
Input Voltage	XT	V_{IN}	$V_{SS1}-0.5 \sim V_{DD1}+0.5$	V
	Ø, FC	V_{IN}	$V_{SS1}-0.5 \sim V_{DD1}+0.5$	
Output Voltage		V_{OUT}	$V_{SS1}-0.5 \sim V_{DD1}+0.5$	V
DC Input Current		I_{IN}	±10	mA
Power Dissipation		P_D	300	mW
Storage Temperature Range		T_{stg}	-65 ~ 150	°C
Lead Temp./Time		T_{sol}	260°C · 10sec	

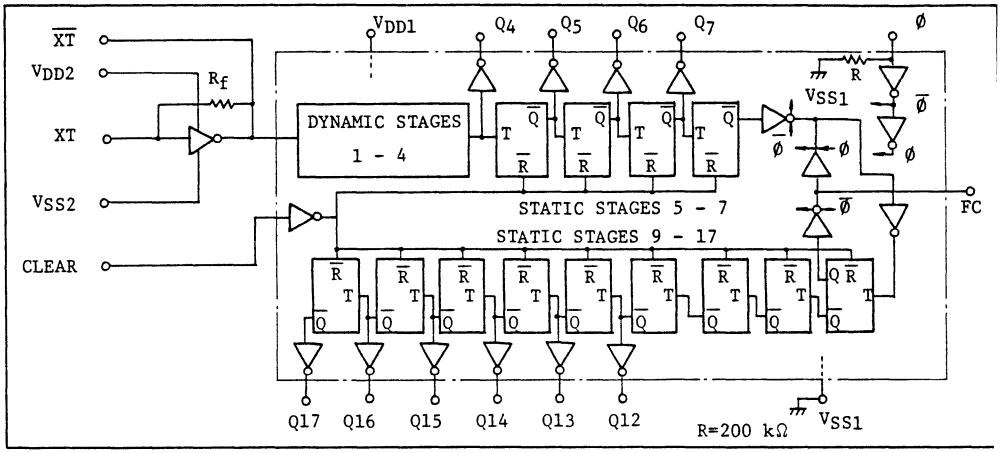
TRUTH TABLE

INPUTS				FUNCTION (See Timing Chart)
CL	XT	Ø	FC	
H		OPEN H	H *	$f_{Q4} = f_{XT} / 2^4$ $Q_5 \sim Q_{17}$ = "L" LEVEL
L		OPEN	$\overline{Q_9}$	$f_{Qn} = f_{XT} / 2^n$ n ; 5 ~ 17
L		H		$f_{Qn} = f_{XT} / 2^n$ n ; 5 ~ 7 $f_{Qm} = f_{FC} / 2^{(m-8)}$ m ; 12 ~ 17

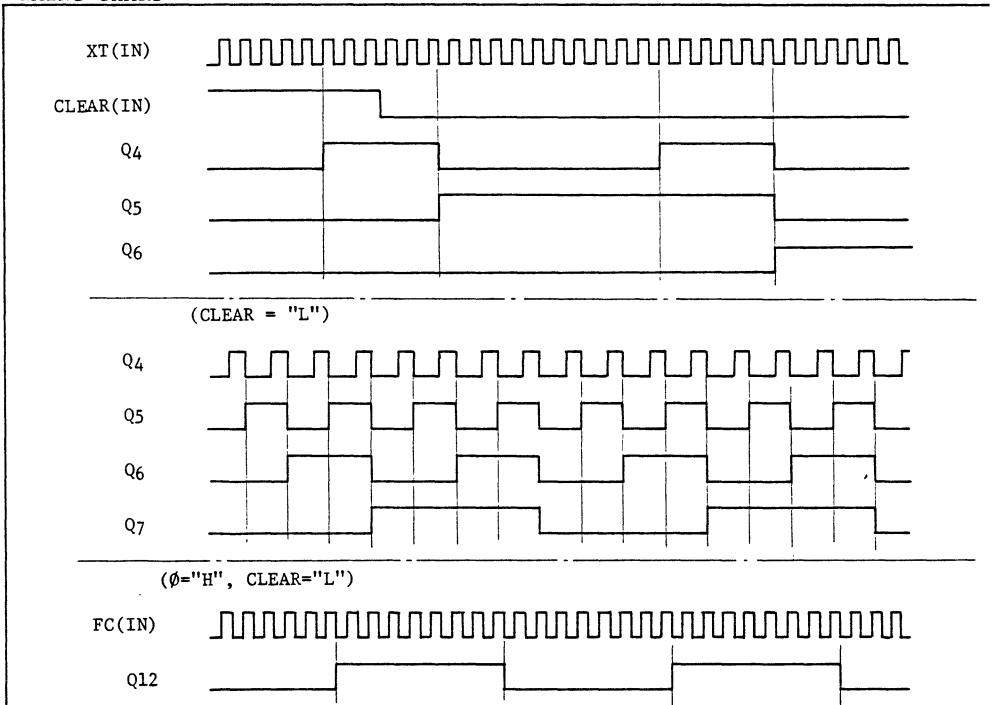
* Don't Care

TC5036P, TC5048P

BLOCK DIAGRAM



TIMING CHART



TC5036P, TC5048P

RECOMMENDED OPERATING CONDITIONS (V_{SS1}=V_{SS2}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD1}		3	-	8	V
	V_{DD2}		3	-	V_{DD1}	
Input Voltage	V_{IN}		0	-	V_{DD2}	V
Operating Temp.	Topr		-40	-	85	℃

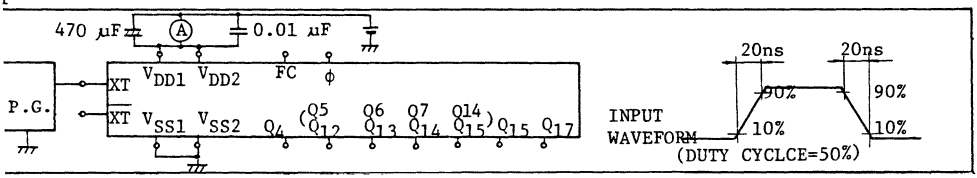
ELECTRICAL CHARACTERISTICS (V_{SS1}=V_{SS2}=0V, V_{DD1}=V_{DD2})

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage		V_{OH}	|I_{OUT}|<1μA V_{IN}=V_{DD},V_{SS}	5	4.95	-	4.95	5.00	-	4.95	-	V
Low Livel Output Voltage		V_{OL}	|I_{OUT}|<1μA V_{IN}=V_{DD},V_{SS}	5	-	0.05	-	0.00	0.05	-	0.05	V
High Level Output Current	Q Output	I_{OH}	V_{OH}=4.6V V_{IN}=V_{SS},V_{DD}	5	-0.2	-	-0.16	-0.8	-	-0.12	-	mA
	FC / XT		V_{OH}=4.6V V_{IN}=V_{SS},V_{DD}	5	-0.025	-	-0.02	-0.06	-	-0.015	-	
Low Level Output Current	Q Output	I_{OL}	V_{OL}=0.4V V_{IN}=V_{DD},V_{SS}	5	0.52	-	0.44	1.5	-	0.36	-	
	FC / XT		V_{OL}=0.4V V_{IN}=V_{DD},V_{SS}	5	0.10	-	0.08	0.25	-	0.06	-	
High Level Input Voltage		V_{IH}	V_{OUT}=0.5V,4.5V I_{OUT} <1μA	5	3.5	-	3.5	2.75	-	3.5	-	V
Low Level Input Voltage		V_{IL}	V_{OUT}=0.5V,4.5V I_{OUT} <1μA	5	-	1.5	-	2.25	1.5	-	1.5	V
gh Level Input rrent(excrpt XT,ϕ)		I_{IH}	V_{IH}= 8V	8	-	0.2	-	10^{-5}	0.2	-	1.0	μA
w Level Input Cur- nt (except, XT, ϕ)		I_{IL}	V_{IL}=0V	8	-	-0.2	-	-10^{-5}	-0.2	-	-1.0	μA
rating Current sumption(TC5048BP)		I_T	f_{XT}=1MHz	5	-	-	-	100	500	-	-	μA

SWITCHING CHARACTERISTICS (V_{DD1}=V_{DD2}, V_{SS1}=V_{SS2}=0V, Ta=25°C, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT.
tput Rise Time(Q OUTPUT)	t_r		5	-	130	250	ns
tput Fall Time(Q OUTPUT)	t_f						
put Amp Vias Resistance	R_f		8	0.6	-	3.0	MΩ
opagation Delay Time(XT-Q_4)	t_{pLH}, t_{pHL}		5	-	250	600	ns
opagation Delay Time(XT-Q_{17})	t_{pLH}, t_{pHL}		5	-	-	8.0	μs
op. Delay Time(CLEAR-Q)	t_{pHL}(CLEAR)		5	-	-	2000	ns
n. Clear Pulse Width	t_w (CLEAR)		5	-	-	1000	ns
x. Clock Frequency	f_{MAX} (XT)		5	8	14	-	MHz
n. Clock Frequency	f_{MIN} (XT)		5	-	-	20	kHz
x. Clock Frequency	f_{MAX} (FC)		5	1.0	-	-	MHz
x. Clock Rise Time	$t_{r\phi}$	(XT, FC)	5	20	-	-	μs
x. Clock Fall Time	$t_{f\phi}$						
ut Capacitance	C_{IN}	except FC		-	5	7.5	pF

TEST CIRCUIT

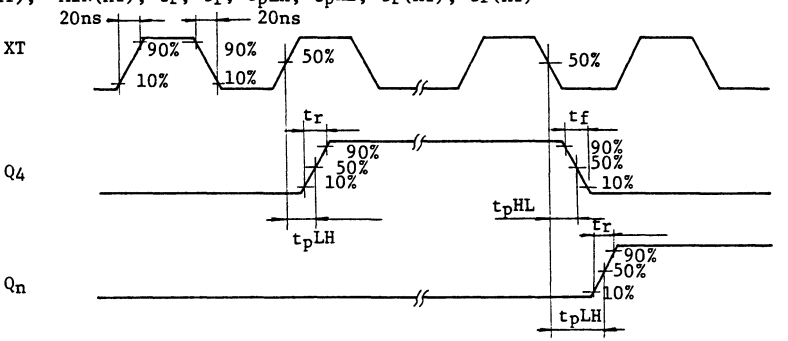


TC5036P, TC5048P

SWITCHING TIME TEST WAVEFORMS

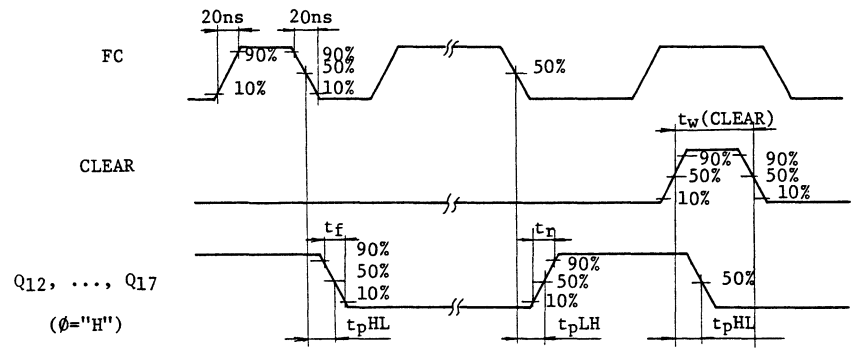
WAVEFORM 1.

1. $f_{MAX(XT)}$, $f_{MIN(XT)}$, t_r, t_f, t_{pLH}, t_{pHL}, $t_r(XT)$, $t_f(XT)$

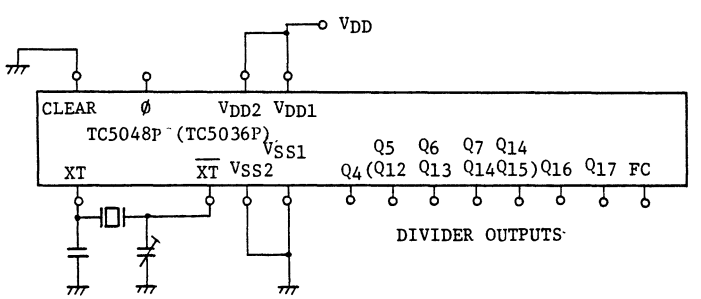


WAVEFORM 2.

2. $f_{MAX(FC)}$, $t_r(FC)$, $t_f(FC)$, $t_w(CLEAR)$, $t_{pHL}(CLEAR)$



TYPICAL APPLICATION

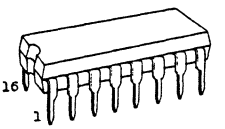


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5037P

TC5037P 4-DIGIT DECADE COUNTER

TC5037P is four digit decimal counter including the latch multipliexer circuit and has the digit signal outputs for dynamic display and the clock generator for dynamic display.
When TRANSFER input is set to "L", the latches hold the counts immediately prior to the falling edge of TRANSFER, so that even if the contents of counters vary, the outputs will not be changed.
RESET is activated by "H" level and sets the counter outputs of all digits to "L".
The outside is 16 pin plastic packages.

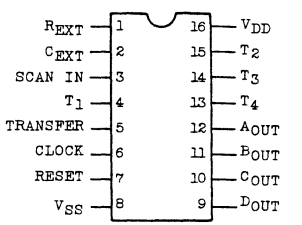


DIP16(3D16A-P)

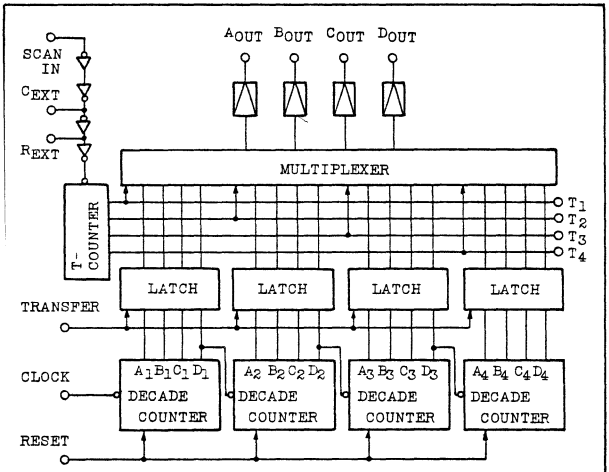
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-55~125	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



BLOCK DIAGRAM



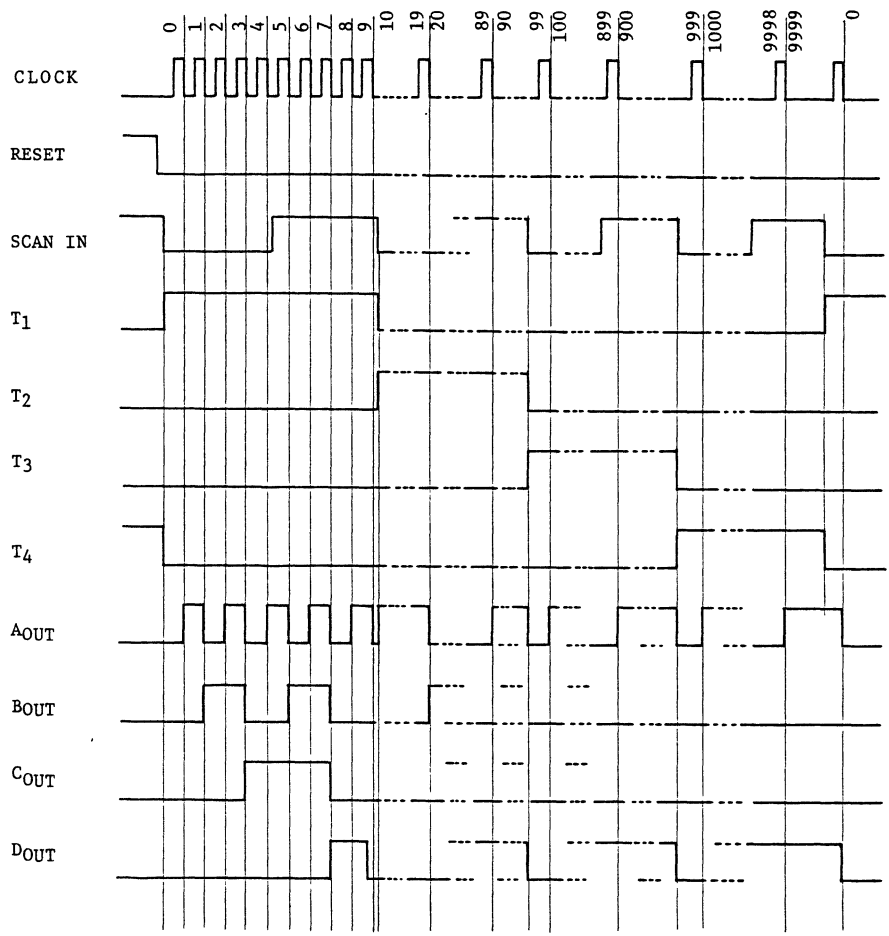
TRUTH TABLE

RESET	TRANS-FER	A_{OUT}	B_{OUT}	C_{OUT}	D_{OUT}
H	H	L	L	L	L
*	L	LA	LA	LA	LA
L	H	C	C	C	C

* ; Don't care
C ; Count operation.
(Counter outputs are dynamically output to A_{IN}-D_{IN} as they are.)
LA ; Latch operation. (Counting is performed but the outputs are not changed.)
Note 1. The outputs vary at the falling edge of CLOCK.
2. T_1~T_4 vary at the falling edge of SCAN IN.

TC5037P

TIMING CHART



Note) TRANSFER = "H"

OPERATING CONSIDERATION

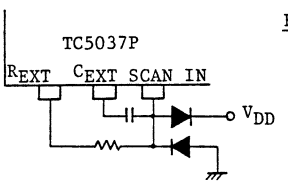
1. SCAN Operation

The scan signal for dynamic display applied to SCAN INPUT terminal is converted to four digit scan signal by T-COUNTER (4 digit ring counter) and controls the multiplexer circuit. The four digit information stored in the latches is transferred to the output in synchronism with T_1 - T_4 outputs.

By applying DC for SCAN signal, arbitrary digit can be statically output. T_1 - T_4 are used for the digit selection circuit.

There are two methods of supplying SCAN signal. One is AUTO SCAN method (Fig. 1) which consists of the multivibrator fabricated with a resistor and a capacitor externally connected to R_{EXT} and C_{EXT} terminals respectively and the internal inverter, and another is to supply external signal to SCAN IN terminal

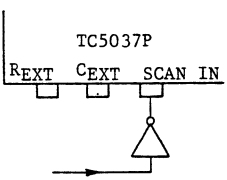
Fig. 1



R = 100 kΩ 1S1588

C = 0.02uF

Fig. 2



EXTERNAL PULSE

(Fig. 2). (Note: R_{EXT} and C_{EXT} are left open in Fig. 2.)

2. Latch Operation

Flickering of output caused by the count pulse with high frequency can be eliminated by controlling TRANSFER terminal.

TRANSFER = "H" : The counter information is transferred to the multiplexer as it is.

TRANSFER = "L" : The content of counter immediately prior to the falling edge of TRANSFER is latched and the multiplexer input is not changed.

(Note) The counter, in this case, still continues counting.

3. Count Operation

TC5037P

For normal count operation, this chip should be used with TRANSFER = "H" and RESET = "L". The output changes its state at the falling edge of CLOCK.

The content of counter can be reset to "0000" by setting RESET terminal to "H". It should be noticed that CLOCK is not active unless RESET is returned to "L".

This LSI can count up to"9999",and if five or more digits are required, TC4510P or TC4518P should be connected in the preceding stage of this LSI.

TC5037P

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	8	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	Topr		-30	-	85	°C
R_{EXT} External Resistance	R		5	100	1000	kΩ
C_{EXT} External Capacitance	C		10^{-4}	0.02	1.0	μF

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-30°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{DD},V_{SS}$	5	4.95	-	4.95	-	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{DD},V_{SS}$	5	-	0.05	-	-	0.05	-	0.05	V
High Level Output Current	A_{OUT},B_{OUT} C_{OUT},D_{OUT}	I_{OH}	V_{OH}=2.5V $V_{IN}=V_{SS},V_{DD}$	5	-1.2	-	-1.0		-	-0.75	-	mA
	T_1 , T_2 T_3 , T_4	I_{OH}		5	-1.2	-	-1.0		-	-0.75	-	
	R_{EXT},C_{EXT}	I_{OH}		5	-0.35	-	-0.3		-	-0.2	-	
Low Level Output Current	A_{OUT},B_{OUT} C_{OUT},D_{OUT}	I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	2.4	-	2.0		-	1.6	-	mA
	T_1 , T_2 T_3 , T_4	I_{OL}		5	0.52	-	0.44		-	0.36	-	
	R_{EXT},C_{EXT}	I_{OL}		5	0.28	-	0.24		-	0.2	-	
Input Voltage	H. Level	V_{IH}	V_{OUT}=0.1V,4.9V $\|I_{OUT}\|$<1μA	5	3.8	-	3.8	2.75	-	3.8	-	V
	L. Level	V_{IL}		5	-	1.2	-	2.25	1.2	-	1.2	
Input Current	H. Level	I_{IH}	V_{IH}=8V	8	-	0.2	-	10^{-5}	0.2	-	1.0	μA
	L. Level	I_{IL}	V_{IL}=0V	8	-	-0.2	-	-10^{-5}	-0.2	-	-1.0	
Quiescent Current Consumption		I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	8	-	50	-	-	50	-	500	μA

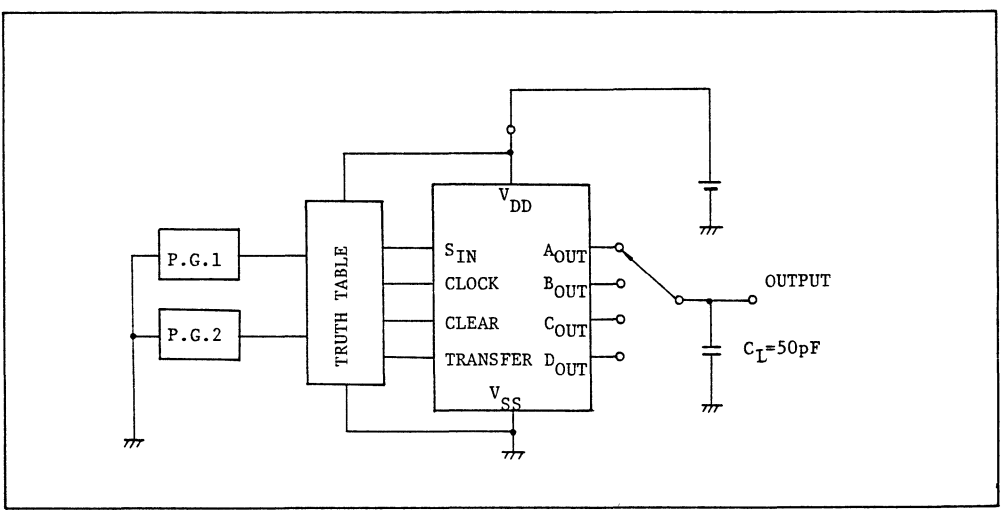
* All valid input combinations

TC5037P

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

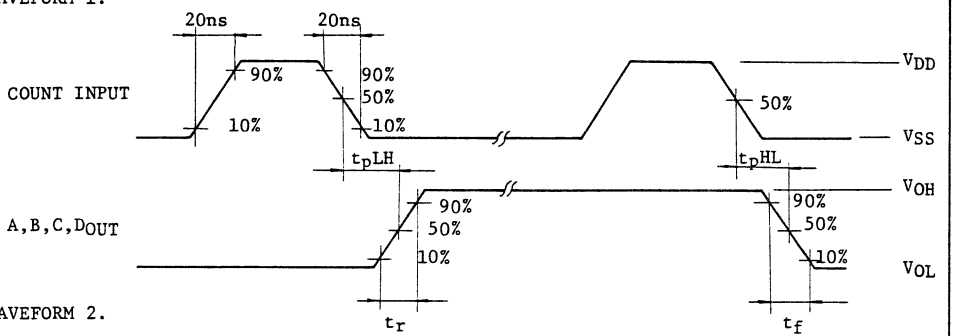
CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
(Low-High) Propagation Delay Time		t_{pLH}	COUNT INPUT → A,B,C, D_{OUT} (WAVEFORM 1)	5	-	600	1000	ns
(High-Low) Propagation Delay Time		t_{pHL}		5	-	600	1000	
(Low-High) Propagation Delay Time		t_{pLH}	TRANSFER → A,B,C, D_{OUT} (WAVEFORM 2)	5	-	400	1000	
(High-Low) Propagation Delay Time		t_{pHL}		5	-	400	1000	
Max. Clock Rise/Fall Time		$t_{r\phi}$, $t_{f\phi}$		5	20	-	-	μs
Min. Clear Pulse Width		t_w(RE)	RESET(0), (9)	5	-	-	1000	ns
Min. Transfer Pulse Width		t_w(TR)	TRANSFER	5	-	-	1000	
Input Capacitance	6, 7 PIN	C_{IN}			-	5	7.5	pF
	3 PIN	C_{IN}			-	7	10	
	5 PIN	C_{IN}			-	9	15	
Max. Frequency		f_{MAX}		5	0.5	2.0	-	MHz

SWITCHING TIME TEST CIRCUIT

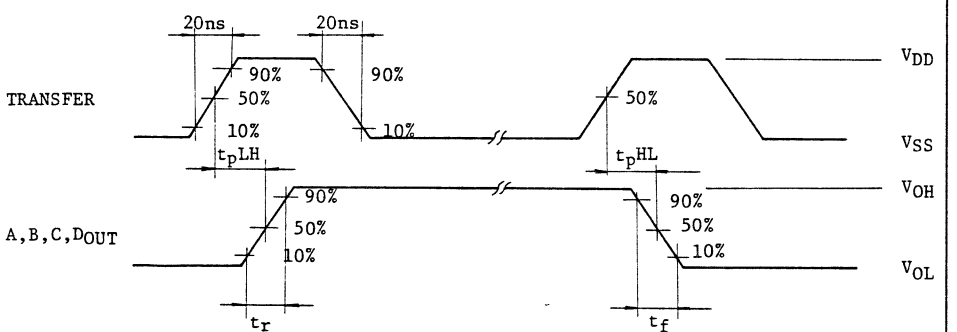


SWITCHING TIME TEST WAVEFORMS

WAVEFORM 1.



WAVEFORM 2.



TC5043P

C²MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC5043P PROGRAMMABLE CR TIMER/DIVIDER

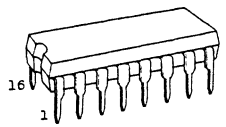
TC5043P is an timer consisting of CR oscillation circuit and frequency division circuit.
The oscillation circuit is made up by externally installing one resistor and one capacitor, being able to be set in a wide range of cycle. The frequency division circuit consists of fixed stage of 1/1000 and variable stage of 1/1 ~ 1/600, being capable of performing frequency division of 6×10^5 max.
Therefore, TC5043P can cover all the regions ranging from conventional CR timers to motor timers.
This device is so designed that the external parts required may be reduced to the minimum by means of the built-in zener diode, auto reset circuit, and pull-up/pull-down resistance.

FEATURES:

- Wide time range of timer (5ms ~ 1500Hr)
- Wide range of fine adjustment of oscillation frequency (±50% or over)
- Low power consumption (2mW ..... Typ.)
- Little supply voltage regulation of oscillation cycle (1%/V)
- Narrow temperature variations of oscillation cycle (0.02%/°C)
- Internal auto reset function
- Precision CR oscillation circuit
- Internal zener diode
- Timer/Divider switchable
- Simple display of time elapsed of oscillation
- Programmable frequency division ratio able to be set in eight ways

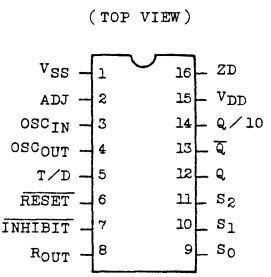
APPLICATIONS:

- Industrial timers
- Timers for various commercial equipment
- Low-frequency oscillators



DIP16(3D16A-P)

PIN ASSIGNMENT



TRUTH TABLE

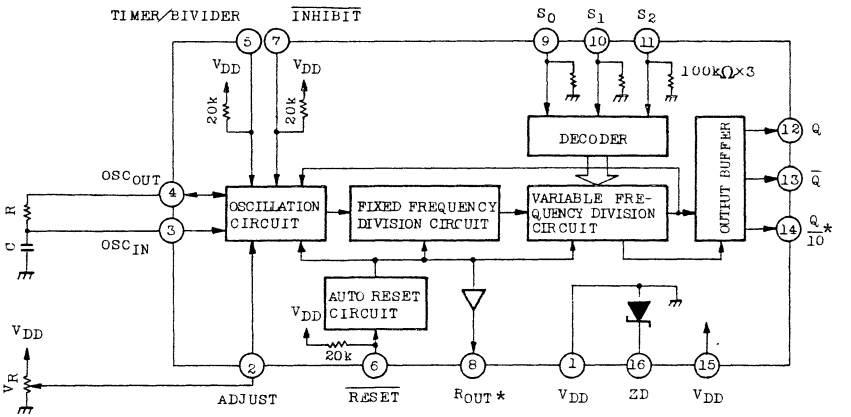
R	T/D	INH	OPERATION
L	*	*	RESET
H	H	H	TIMER OPERATION
H	L	H	DIVIDER OPERATION
H	*	L	TEMPORARY STOP OF OPERATION

* Don't Care

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC		SYMBOL	RATING	UNIT
DC Supply Voltage		V_{DD}	V_{SS}-0.5 ~ V_{SS}+12	V
Input Voltage		V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	R_{OUT}, Q/10	V_{OUT}	V_{SS}-0.5 ~ V_{SS}+12	V
	Q, $\bar{Q}$, OSC_{OUT}		V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current		I_{IN}	±10	mA
Zener Current		I_Z	10	mA
Power Dissipation		P_D	300	mW
Operating Temperature Range		T_{opr}	-40 ~ 85	°C
Storage Temperature Range		T_{stg}	-65 ~ 150	°C

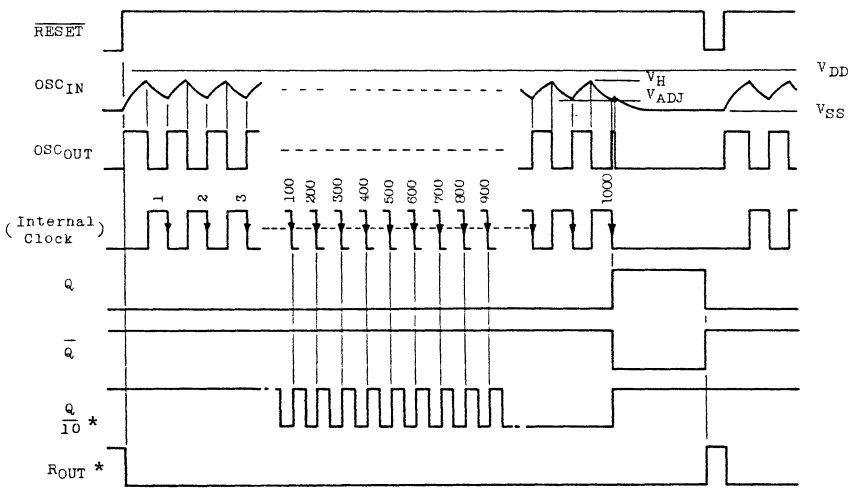
SYSTEM DIAGRAM



Outputs marked with * are N-channel open drain structure.

TIMING DIAGRAM (1)

. Timer operation, Programmable frequency division ratio 1/1
(T/D="H", $\overline{INHIBIT}$="H", $S_0=S_1=S_2$="L")

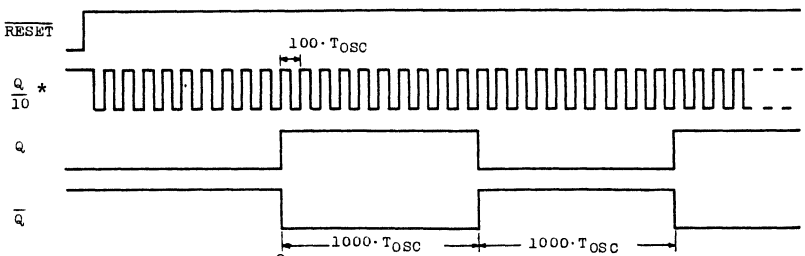


. For outputs marked with *, add pull-up resistance to V_{DD}.

TC5043P

TIMING DIAGRAM

2. Divider operation, Programmable frequency division ratio 1/1
(T/D="L", $\overline{\text{INHIBIT}}$="H", $S_0=S_1=S_2$="L")



* Connect pull-up resistance to $\frac{Q}{10}$ output.

PIN FUNCTION

PIN NO.	SYMBOL	FUNCTION
1	V_{SS}	GND (0V) Pin
2	ADJUST	Pin for fine adjustment for oscillation frequency. Externally apply the voltage ranging from $0.2V_{DD}$ to $0.55V_{DD}$.
3	OSC_{IN}	Oscillation circuit configuration pins : These pins start oscillation when resistor R is connected between OSC_{IN} and OSC_{OUT} and capacitor C between OSC_{IN} and V_{SS}, respectively. In case V_{ADJ} is $0.39V_D$ oscillation cycle becomes almost $T_{OSC}=RC$.
4	OSC_{OUT}	
5	TIMER /DIVIER	Timer/divider switching input. At time of open (or "H" level), this device operates as a timer, and at time of "L" level it operates as a divider.
6	$\overline{\text{RESET}}$	All the counters are reset at "L" level. At the rising edge of this input, the device begins to count.
7	$\overline{\text{INHIBIT}}$	When this pin is set at "L" level, the device keeps stopping oscillation during the period of "L" level state. The pin is used for temporary stop of oscillation.
8	$RESET_{OUT}$	Only at time of timer operation, reset signal is output. (At the time when $\overline{\text{RESET}}$ = "L" and during the period of auto reset at the rising time of power supply, output is off.) For the divider mode, this pin should be open.
9	S_0	$S_0 \sim S_3$ are frequency division ratio switching inputs of the counter. Eight time intervals can be predetermined by combining pins, $S_0 \sim S_2$ ($T = 1000 \times \frac{1}{f_{OSC}}$)

IN NO.	SYMBOL	FUNCTION
10	S_1	S_2: L (L: S_1 = L; H: S_1 = H) / H (L: S_1 = L; H: S_1 = H) S_0: L, H, L, H, L, H, L, H Time intervals of timer*: T, 3T, 6T, 10T, 60T, 30T, 300T, 600T * In the divider operation mode, the above time intervals of timer become half cycles of Q and $\overline{Q}$.
11	S_2	
12	Q	Q and $\overline{Q}$ are time-up outputs. After the end of time intervals, Q reaches "H" level and $\overline{Q}$ reaches "L" level. While the divider is operating, these outputs oscillate at double the cycle of time range of timer.
13	$\overline{Q}$	
14	$\frac{Q}{10}$	Q/10 is a pin which outputs the elapsed time of timer, and outputs the pulse of 1/10 cycle of timer time. This is N-channel open drain output.
15	V_{DD}	Power supply pin
16	ZD	The cathode terminal of zener diode is put out of this pin. This pin is used as a stabilized power supply by making the connection to V_{DD}.

ERATIONAL DESCRIPTION

Oscillation Circuit

The oscillation circuit can be made up by connecting resistor R between OSC_{IN} and OSC_{OUT} and capacitor C between OSC_{IN} and V_{SS}(GND) as shown in Fig. 1.

This IC has two levels of built-in reference voltage V_H(0.62 V_{DD}) and reference voltage V_L(=V_{ADJ}) externally supplied to ADJ pin, and performs oscillation in such a form as the charge and discharge wave of CR runs between these two levels.

Therefore, oscillation cycle can be adjusted by varying the voltage of ADJ pin.

When $V_{ADJ} \fallingdotseq 0.39\ V_{DD}$, the oscillation cycle is decided from the equation of T_{OSC}=RC (T : [S], R[Ω], C[F]). V_{ADJ} should be used within the range of $0.2V_{DD} \sim 0.55V_{DD}$.

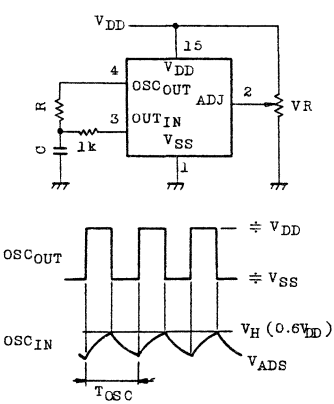


Fig. 1 Oscillation Circuit

TC5043P

2. Counting circuit (Frequency dividing circuit)

This circuit consists of the fixed frequency dividing stage of 1/1000 and the variable frequency dividing stage of 1/1 ∿ 1/600.

Time intervals of timer can be predetermined in eight ways by combining three inputs of S0 ∿ S2.

Select Input									
S_2	L				H			
S_1	L		H		L		H	
S_0	L	H	L	H	L	H	L	H
Time intervals of Timer	T	3T	6T	10T	60T	30T	300T	600T

Note 1. $T = 1000 \cdot T_{OSC}$

Note 2. "L" level may be open

3. Reset operation

The internal counter is kept reset by the built-in auto reset circuit until the power supply level reaches reset release voltage (V_{RD}) at time of application of power. However, the power rising time of more than 500μs should be taken for abrupt rising edge of power supply because there may be no possibility of the internal counter being reset. In case of the rising time of 500μs or below, differentiation circuit is made up by adding the capacitor to $\overline{RESET}$ terminal. (Refer to Fig. 2)

It is a matter of course that the internal circuit can be reset even by setting $\overline{RESET}$ input at "L" level. When the reset operation is released, oscillating and counting operations start. The reset signal is being output to this IC.

In case where this pin (R_{OUT}) is internally reset, it is off (at the rising time of power supply and during "L" level of $\overline{RESET}$); therefore, this pin can be used for making the external circuit synchronize by use of pull-up resistance or equivalent. While R_{OUT} is not in use, it should be kept set open (or at "L" level).

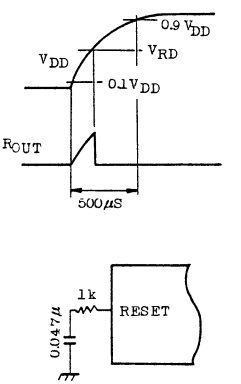


Fig. 2 Auto Reset Circuit

4. Inhibit operation

Oscillation can be stopped by setting $\overline{INHIBIT}$ input at "L" level.
Normal operation can be performed by setting $\overline{INHIBIT}$ input open (or at "H" level)

5. Divider function

When the T/D pin is set open (or at "H" level), this device operates as a timer. When this pin is set at "H" level, this divice can be used as a divider which continue operating oscillation/counting without creating time-up signal.
For the divider mode, however, R_{OUT} cannot be used. (Open or "L").

COMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL		MIN.	TYP.	MAX.	UNIT
upply Voltage	V_{DD}		6.2	-	10	V
igh Level Input Voltage	V_{IH}		0.8V_{DD}	-	V_{DD}	V
ow Level Input Voltage	V_{IL}		0	-	0.2V_{DD}	V
xternal Resistor	R		5K	-	2M	Ω
xternal Capacity	C		1000P	-	5μ	F
utput Voltage	V_{OUT}	* Applcable to R_{OUT}' Q/10	0	-	10	V

ECTRICAL CHARACTERISTICS (V_{SS}=0V)

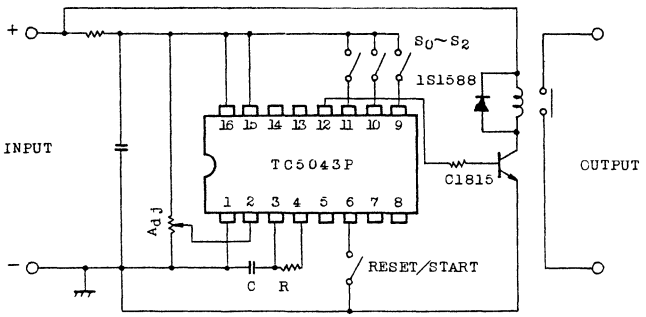
ITEM	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
ner Voltage	V_Z	I_Z=1mA	-	6.2	8.1	6.5	7.2	8.2	6.6	8.5	V
		I_Z=10mA		6.2	8.1	6.5	7.3	8.2	6.6	8.5	
gh Level tput Current	I_{OH}	V_{OH}=6V	7	-1.2	-	-1.2	-2.5	-	-1.0	-	mA
		V_{OH}=3V		-5.2	-	-5.2	-9.0	-	-4.0	-	
w Level tput Current	I_{OL}	V_{OL}=0.4V	7	1.0	-	1.0	2.0	-	0.8	-	
gh Level put Current	I_{IH}	V_{IH}=10V,(Exclusive of S_0~S_2)	10	-	5	-	10^{-3}	5	-	5	μA
w Level put Current	I_{IL}	V_{IL}=0V,(Exclusive of R·$\overline{INH}$·T/D)	10	-	-5	-	-10^{-3}	-5	-	-5	
ll-up Resistance	R_{PU}	R,$\overline{INH}$,T/D Inputs	-	7	50	10	20	50	10	75	kΩ
ll-down sistance	R_{PD}	S_0,S_1,S_2 Inputs	-	45	200	66	100	200	66	300	
tput OFF Current	I_{OFF}	V_{OH}=10V, R_{OUT}, Q/10 Outputs	10	-	1.0	-	10^{-3}	1.0	-	10.0	μA
to Reset Release ltage	V_{RD}		-	-	-	2.6	-	5.2	-	-	V
pply Current	I_{DD}	C=0.1μF, R=1MΩ*	10	-	-	-	0.3	-	-	-	mA

All inputs and outputs are open.

TC5043P

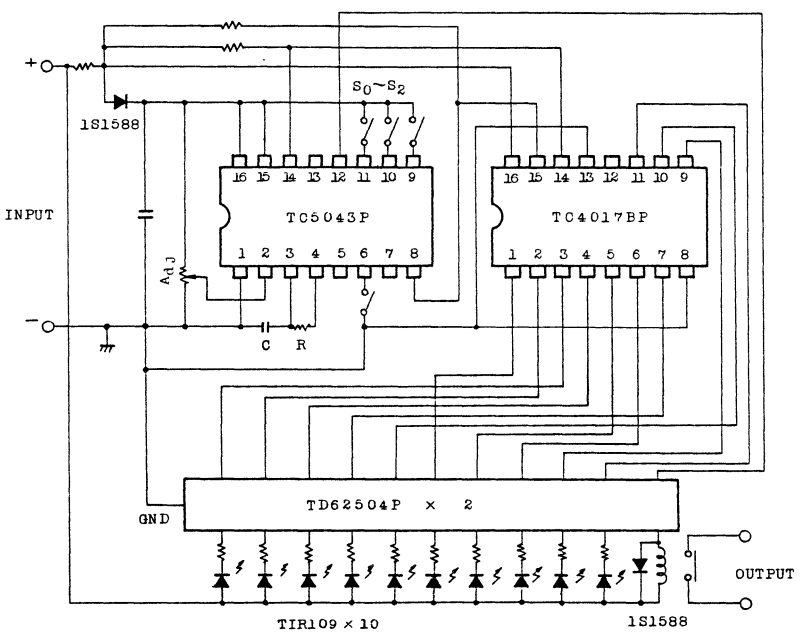
EXAMPLES OF APPLIED CIRCUIT

∘ Timer Circuit I (Basic Type)



(Time of timer can be varied to linear by using resistor R deciding time constant with variable resistance.)

∘ Timer Circuit II (Elapsed Time Displaying Type)

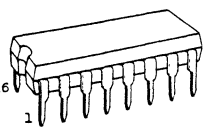


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5050P

TC5050P DUAL 50/64 STAGE STATIC SHIFT REGISTER

TC5050P is static shift register consisting of D type flip-flops, and can be used as either 50 bit shift register or 64 bit shift register depending on OUTPUT MODE input.
Since one of two input data can be selected by INPUT MODE input, the applications for scratch pad memories, etc. can be realized by connecting one of data inputs to the output. And if two circuits are connected in series, this can be expanded to 100 bit, 114 bit or 128 bit shift register.
When used with 5 volts power supply, one of TTL or DTL can be directly driven.

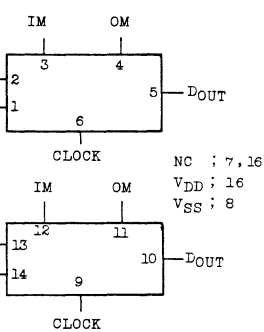


DIP 16 (3D16A-F)

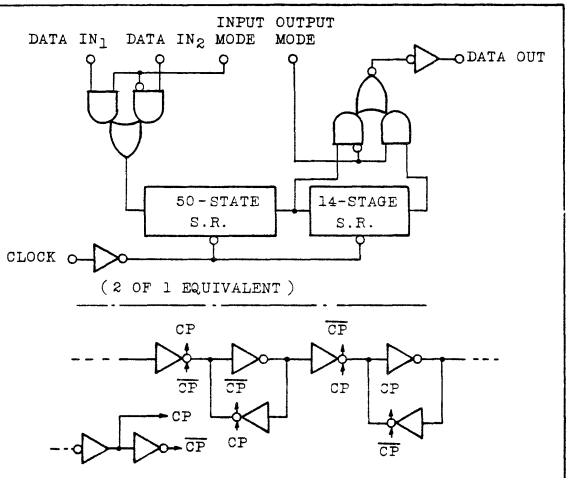
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-55 ~ 125	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



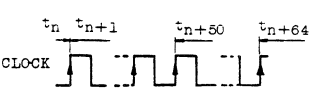
LOGIC DIAGRAM



TRUTH TABLE

t_n, t_{n+1}			t_{n+50}		t_{n+64}	
D_{IN1}	D_{IN2}	IM	OM	D_{OUT}	OM	D_{OUT}
H	*	H	L	H	H	H
L	*	H	L	L	H	L
*	H	L	L	H	H	H
*	L	L	L	L	H	L

* Don't Care



TC5050P

RECOMMENDED OPERATING CONDITIONS (V_{SS}=OV)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	8	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	Topr		-30	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=OV)

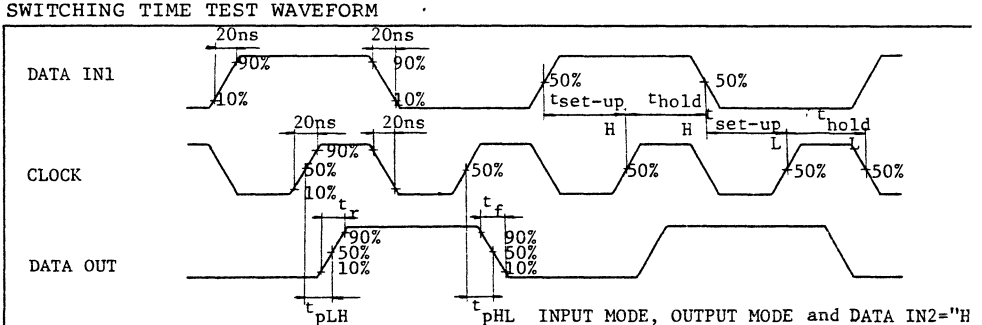
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-30°C MIN.	-30°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNI
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{DD},V_{SS}$	5	4.95	-	4.95	5.00	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{DD},V_{SS}$	5	-	0.05	-	0.00	0.05	-	0.05	
High Level Output Current	I_{OH}	$V_{OH}=2.5V$ $V_{IN}=V_{DD},V_{SS}$	5	-1.25	-	-1.25	-5.0	-	-1.0	-	mA
Low Level Output Current	I_{OL}	$V_{OL}=0.4V$ $V_{IN}=V_{DD},V_{SS}$	5	3.2	-	3.2	7.0	-	2.4	-	
High Level Input Voltage	V_{IH}	$V_{OUT}=0.5V,4.5V$ $\|I_{OUT}\|<1\mu A$	5	3.5	-	3.5	2.75	-	3.5	-	V
Low Level Input Voltage	V_{IL}	$V_{OUT}=0.5V,4.5V$ $\|I_{OUT}\|<1\mu A$	5	-	1.5	-	2.25	1.5	-	1.5	
H.Level Input Current	I_{IH}	$V_{IH}=8V$	8	-	0.2	-	10^{-5}	0.2	-	1.0	μA
L.Level Input Current	I_{IL}	$V_{IL}=0V$	8	-	-0.2	-	-10^{-5}	-0.2	-	-1.0	μA
Quiescent Current C.	I_{DD}	*V_{IN}=VSS,VDD	5	-	50	-		50	-	375	μA

* All valid input combination

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=OV, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_r		5	-	135	400	ns
Output Fall Time	t_f		5	-	100	200	ns
(Low-High)P.Delay Time	t_{pLH}		5	-	500	1000	ns
(High-Low)P.Delay Time	t_{pHL}		5	-	400	1000	
Max.Clock Rise Time	$t_{r\phi}$		5	20	-	-	μs
Max.Clock Fall Time	$t_{f\phi}$						
Max. Clock Frequency	$f_{MAX\phi}$		5	1.0	2.5	-	MHz
Data Set Up Time	t_{set-up}		5	-	100	250	ns
Data Hold Time	t_{hold}		5	-	-100	50	ns
InputCapacitance CLOCK INPUT	C_{IN}			-	10	15	pF
InputCapacitance OTHER INPUT				-	5	7.5	

SWITCHING TIME TEST WAVEFORM

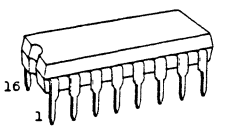


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5051P
TC5052P

TC5051P 4 DIGIT DECADE COUNTER WITH BLANKING CONTROL
TC5052P 4 DIGIT DECADE COUNTER WITH CLOCK ENABLE

TC5051P and TC5052P are four digit decimal up counters. The contents of counter are dynamically output digit by digit in sequence from the higher-order digit to BCD OUTPUT. When the content of counter reaches "9999", CARRY OUT is output with "H" level, and it holds "L" level for other counter contents.
TC5051P has BLANKING CONTROL input which facilitates the leading zero suppress operation for higher order digits than arbitrary digit position. And TC5052P is capable to inhibit CLOCK by means of CLOCK ENABLE input.

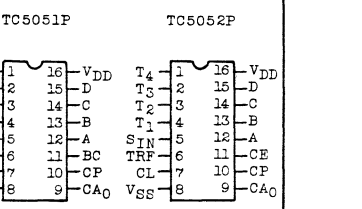


DIP 16 (3D16A-P)

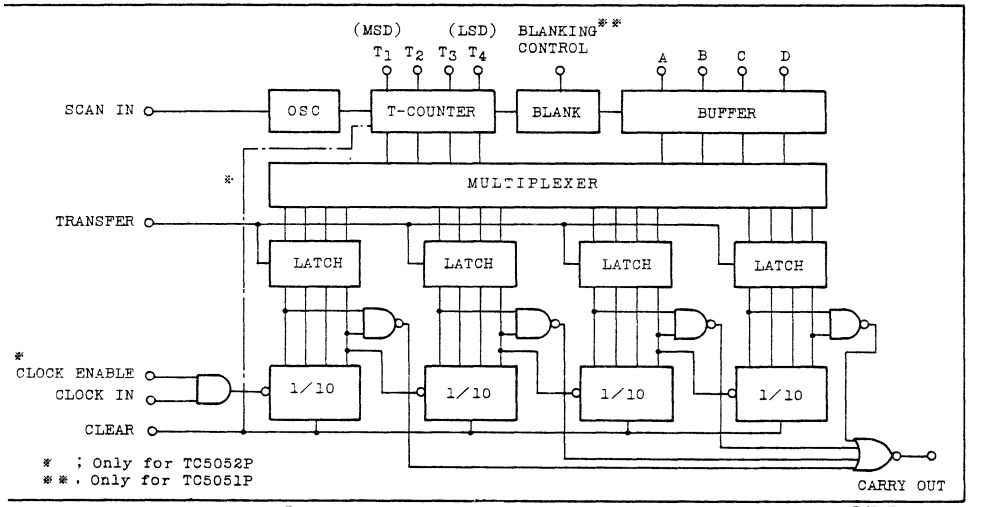
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+14	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	PD	300	mW
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



BLOCK DIAGRAM



* ; Only for TC5052P
** ; Only for TC5051P

TC5051P, TC5052P

DESCRIPTION OF PIN FUNCTION

PIN No.	SYMBOL	NAME	FUNCTION
1	T_4	DIGIT SELECT 4	Outputs to select the digit of BCD OUT (Output signal) and correspond in ascending order from T_1. "H" level is shifted from T_1, T_2, T_3 then T_4 in sequence for every eight clocks of S_{IN}. In the case of TC5052P, when CLEAR is set to "H", all of T_1~T_4 become "L" and when CLEAR falls the scan is always started from T_1. T_1~ T_4 are not affected by CLEAR for TC5051P.
2	T_3	DIGIT SELECT 3	
3	T_2	DIGIT SELECT 2	
4	T_1	DIGIT SELECT 1	
5	S_{IN}	SCAN INPUT	T-COUNTER CLOCK input. The clock can be generated by connecting a capacitor between this terminal and GND.
6	TRF	TRANSFER	H: Decimal counter outputs are transferred to the multiplexer as they are. L: The counter outputs at the falling edge of TRF are latched.
7	CL	CLEAR	The counter is reset to "0000" by "H" level input. TC5052P establishes the synchronism of T-counter by means of CLEAR input.
8	V_{SS}	V_{SS}	(GND)
9	CA_O	CARRY OUT	"H" level is output as long as the counter holds "9999". This becomes "L" level for all other counts.
10	CP	CLOCK INPUT	First stage decimal counter clock, which triggers at the falling edge.
11	CE	CLOCK ENABLE (TC5052P)	Clock input is inhibited by "L" level
	BC	BLANK CONTROL (TC5051P)	All digits are displayed by "H" level, leading zero suppress can be achieved by "L" level and zero suppress for higher order digits than a specific digit position can be achieved by connecting T output to BC.
12	A	BCD OUT A	BCD outputs of decimal counter. When T_1="H", the highest order digit (4th digit) is output. When T_2="H", 3rd digit is output, when T_3="H", 2nd digit is output and when T_4="H", 1st digit is output. If zero suppress is activated, all the outputs become "H" level.
13	B	BCD OUT B	
14	C	BCD OUT C	
15	D	BCD OUT D	
16	V_{DD}	V_{DD}	V_{DD} Power Supply (3 - 12 volts)

OPERATING CONSIDERATION

* Count and Reset Operations

When CLEAR input is set at "H" level, the counter is reset to "0000". If pulse is applied to CLOCK input after returning CLEAR input to "L", the counter advances its count up to "9999" at the falling edge of clock providing CLOCK ENABLE to be "H". If CLOCK ENABLE is "L", CLOCK is inhibited. CARRY OUT is output with "H" level only when the count is "9999".

* Latch Operation - When TRANSFER input is set to "H", the counter output is transferred to the multiplexer as it is and output dynamically to BCD OUT in synchronism with S_{IN}. When TRANSFER input is changed from "H" to "L", the counter content at the falling edge of TRANSFER is stored in the latch and BCD OUT is not varied even if the count changes.

*Scan Operation - BCD output of each digit is output on common A_{OUT}~D_{OUT} on time sharin basis and switching of digit is achieved by connecting a capacitor between SCAN IN inpu and V_{SS}(GND)(internal oscillation) or by supplying external clock from SCAN IN.

'ERATING CONSIDERATION

Capacitance of approximately 1000pF is recommended for the internal oscillation.

Switching of digit is in synchronism with the timing outputs of T_1 - T_4. When T_1 is "H" thousand's digit is output to BCD OUT, when T_2 is "H" hundred's digit is output, when T_3 is "H" ten's digit is output, and when T_4 is "H" unit's digit is output.

Blanking Operation (TC5051P)

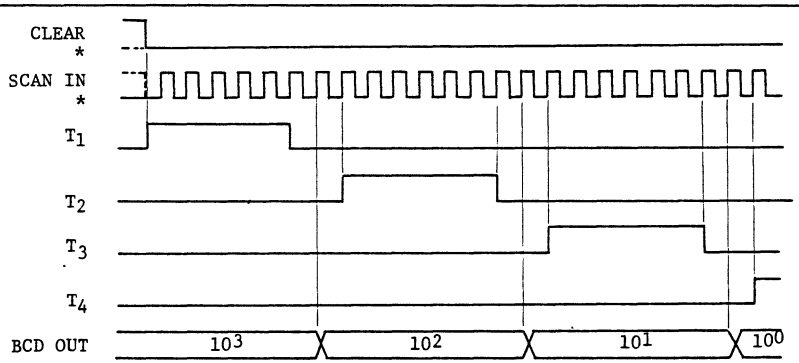
By controlling BLANKING CONTROL, leading zero suppress of higher order digit positions than a specific digit position can be achieved by the function of internal circuit.

BLANKING CONTROL = V_{SS}	Zero Suppress for all digits	*
" = V_{DD}	No Zero Suppress	
" = T_2	Zero Suppress for only thousand's digit	*
" = T_3	Zero Suppress for thousnad's and hundred's digits	*
" = T_4	Zero Suppress for all except unit's digit	*

When blanking is activated, all of A_{OUT} - D_{OUT} become "H".

* (Note) When a carry occurs from the counter and during one cycle of T counter, normal output may not be seen.

MING CHART



* ..... TC5051P, — TC5052P

TC5051P, TC5052P

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	12	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
S_{IN} Connecting Capa.	C_{EXT}		50	-	30000	pF
Operating Temp.	Topr		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UN
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA	5	4.95	-	4.95	5.00	-	4.95	-	
		V_{IN}=V_{SS},V_{DD}	10	9.95	-	9.95	10.00	-	9.95	-	
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA	5	-	0.05	-	0.00	0.05	-	0.05	
		V_{IN}=V_{SS},V_{DD}	10	-	0.05	-	0.00	0.05	-	0.05	
High Level Output Current	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{IN}=V_{SS},V_{DD}									
Low Level Output Current	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	m
		V_{OL}=0.5V									
		V_{IN}=V_{SS},V_{DD}	10	1.3	-	1.11		-	0.9	-	
High Level Input Voltage	V_{IH}	V_{OUT}=0.5V,4.5V	5	3.5	-	3.5	2.75	-	3.5	-	
		V_{OUT}=1.0V,9.0V	10	7.0	-	7.0	5.5	-	7.0		
		$\|I_{OUT}\|$<1μA									
Low Level Input Voltage	V_{IL}	V_{OUT}=0.5V,4.5V	5	-	1.5	-	2.25	1.5	-	1.5	V
		V_{OUT}=1.0V,9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		$\|I_{OUT}\|$<1μA	0								
High Level Input Current (other than S_{IN})	I_{IH}	V_{IH}=12V	12	-	0.3	-	10^{-5}	0.3	-	1.0	μ
Low Level Input Current (other than S_{IN})	I_{IL}	V_{IL}=0V	12	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μ
High Level Input Current (S_{IN})	I_{IH}	V_{IH}=12V	12	-	-	50	-	200	-	-	μ
Low Level Input Current (S_{IN})	I_{IL}	V_{IL}=0V	12	-	-	1.5	-	6	-	-	μ
Quiescent Current Consumption	I_{DD}	V_{IN}=V_{SS},V_{DD}	5	-	-	200	-	200	-	500	μ
			10	-	-	500	-	500	-	1000	

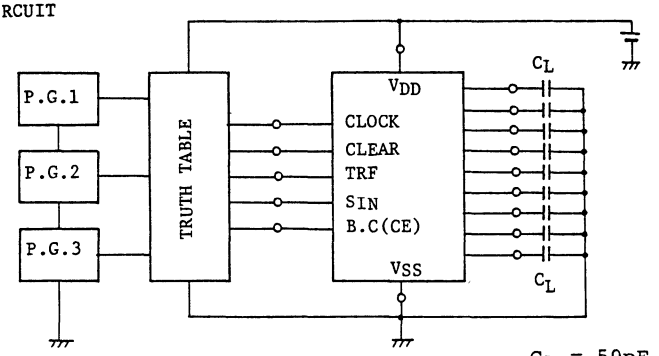
WITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
ıtput Rise Time	t_r		5 10	- -	130 65	400 200	ns
ıtput Fall Time	t_f		5 10	- -	100 50	200 100	ns
:opagation Delay ıme (CLOCK-BCD_{OUT})	t_{pLH} t_{pHL}	T_4="H"	5 10	- -	1200 450	2500 1000	ns
:opagation Delay ıme (CLOCK-CARRY)	t_{pLH} t_{pHL}		5 10	- -	900 400	2000 800	ns
:opagation Delay ıme (S_{IN} - T_n)	tpLH tpHL		5 10	- -	1200 450	2500 1000	ns
:opagation Delay ıme (S_{IN} -BCD_{OUT})	tpLH tpHL		5 10	- -	1600 700	2500 1400	ns
:opagation Delay ıme (CLEAR-BCD_{OUT})	t_{pHL}		5 10	- -	900 350	2000 800	ns
ın. Clear Pulse dth	t_w (CLEAR)		5 10	- -	700 350	1500 750	ns
ın. Transfer ılse Width	t_w (TRANSFER)		5 10	- -	140 50	500 250	ns
ıx. Clock equency	$f_{MAX\phi}$		5 10	1.0 2.0	1.5 3.5	- -	MHz
ıx. Scan equency	f_{MAX}		5 10	0.5 1.0	1.0 2.0	- -	MHz
ın. Clear Removal me	t_{rem}		5 10				ns
ın. Set Up Time RANSFER-CLOCK)	t_{set-up}		5 10				ns
ın. Set Up Time RANSFER-CLEAR)	t_{set-up}		5 10				ns
ıx. Clock Rise Time	$t_{r\phi}$		5	20	-	-	μs
ıx. Clock Fall Time	$t_{f\phi}$		10	2.5	-	-	μs
ıput Capacitance	C_{IN}						pF

TC5051P, TC5052P

SWITCHING TIME TEST CIRUIT

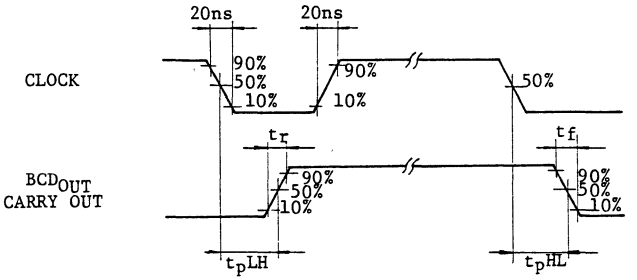
TEST CIRCUIT



C_L = 50pF

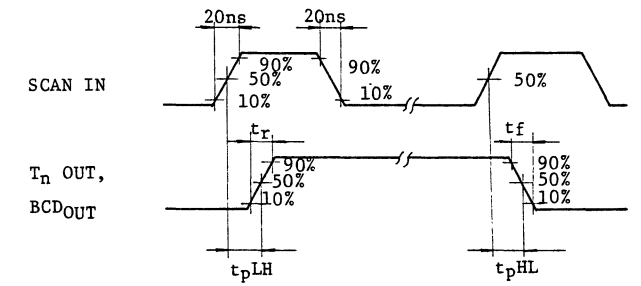
SWITCHING TIME TEST WAVEFORMS

WAVEFORM 1.



CLEAR="L"
CE(TC5052P)="H"
B.C.(TC5051P)="H"
TRF="H"
S_{IN} : Any Pulses

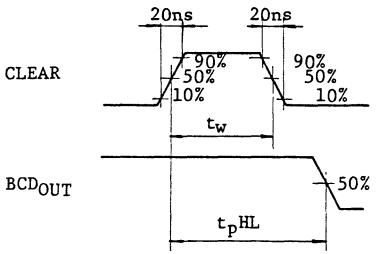
WAVEFORM 2.



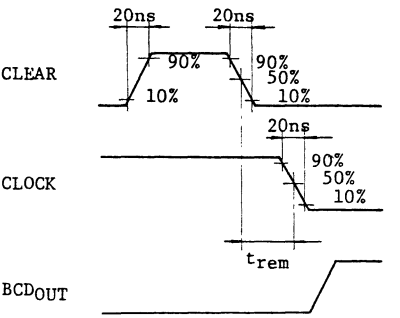
CLEAR="L"
CE,(B.C.)="H"
TRF="H"
CLOCK : Any Pulses

WITCHING TIME TEST WAVEFORMS

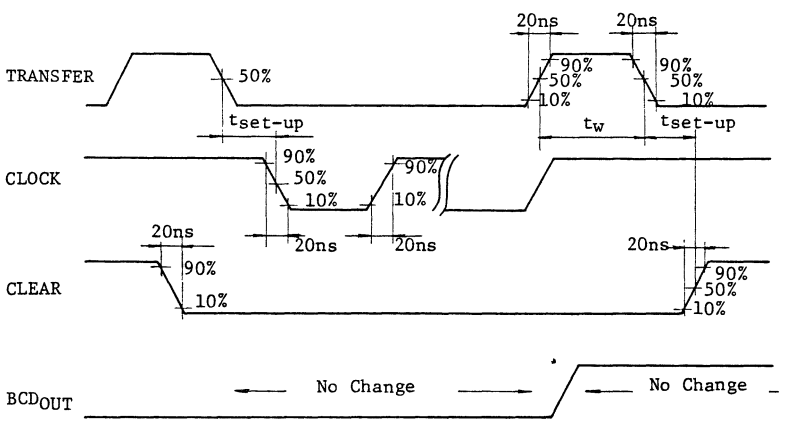
WAVEFORM 3.



CLOCK : PG
CE(BC)="H"
TRF = "H"
S_{IN} = "H"



(CE(BC)="H", TRF="H", S_{IN}="H")

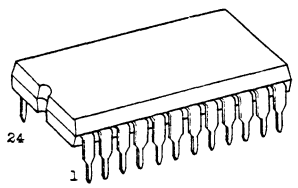


TC5053P
TC5054P

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5053P 4-DIGIT UP/DOWN DECADE COUNTER
TC5054P 4-DIGIT UP/DOWN DECADE COUNTER

TC5053P/TC5054P is a 4-digit decimal up/down counter containing 7-segment decoder/driver.
The counter consists internally of a 4-digit latch, multiplexer, scan oscillating circuit, and decoder/driver capable of directly driving LED.
The clock input is independently equipped with an up-clock and a down-clock. Each input has the function of a Schmitt trigger.
This type of up/down counter can be widely applied to counters, panelmeters, etc.

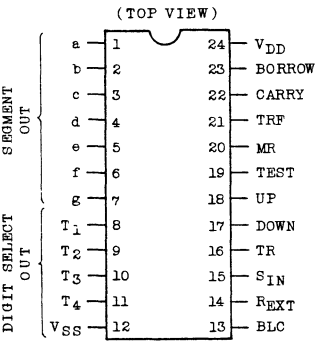


DIP 24 (6D24A-P)

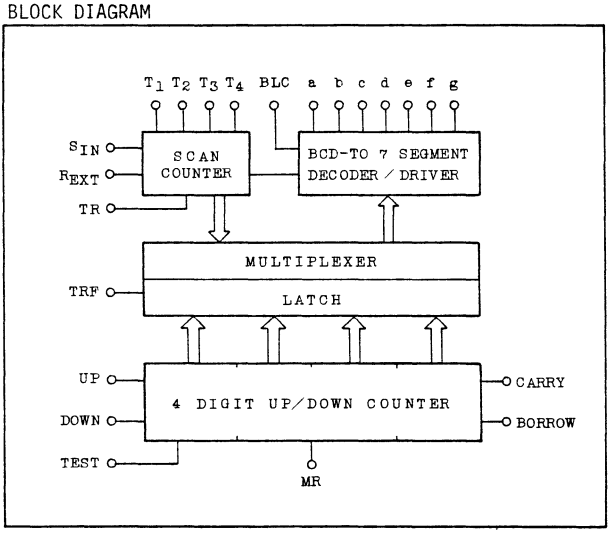
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-55 ~ 125	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

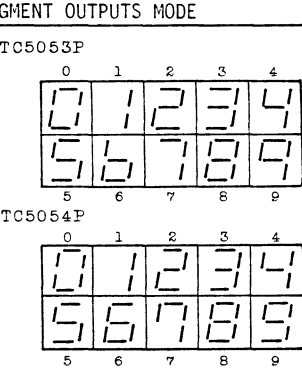
PIN ASSGNMENT



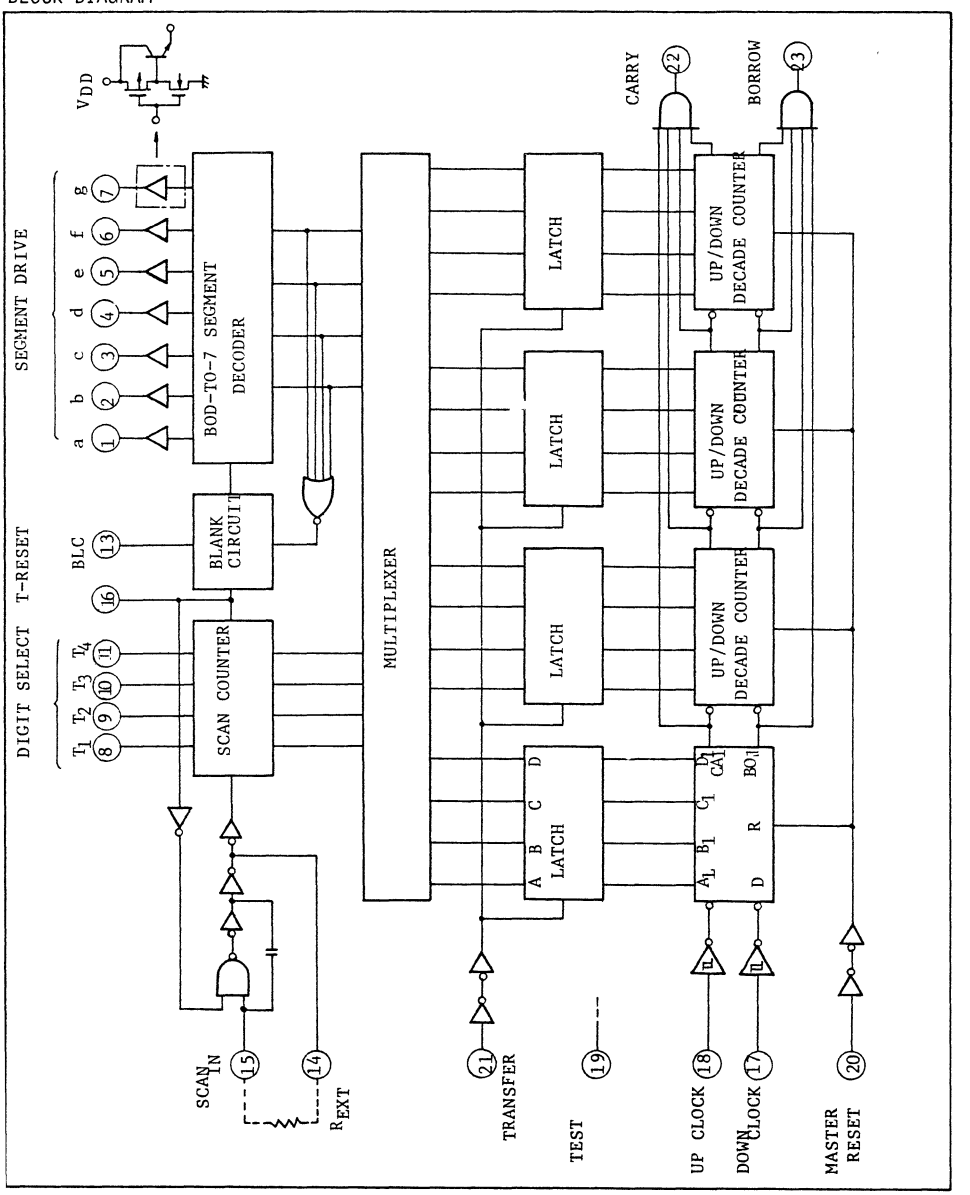
BLOCK DIAGRAM



SEGMENT OUTPUTS MODE



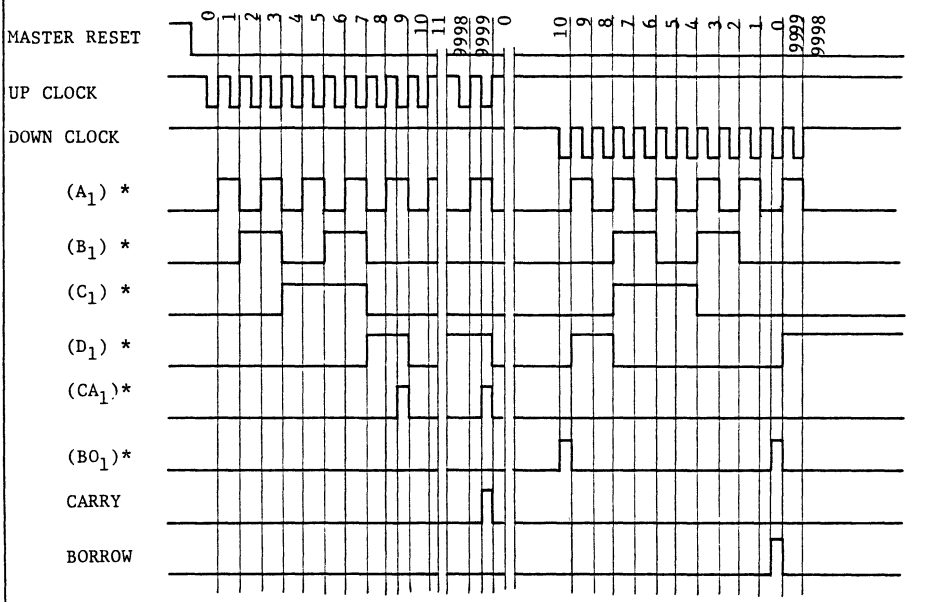
BLOCK DIAGRAM



TC5053P, TC5054P

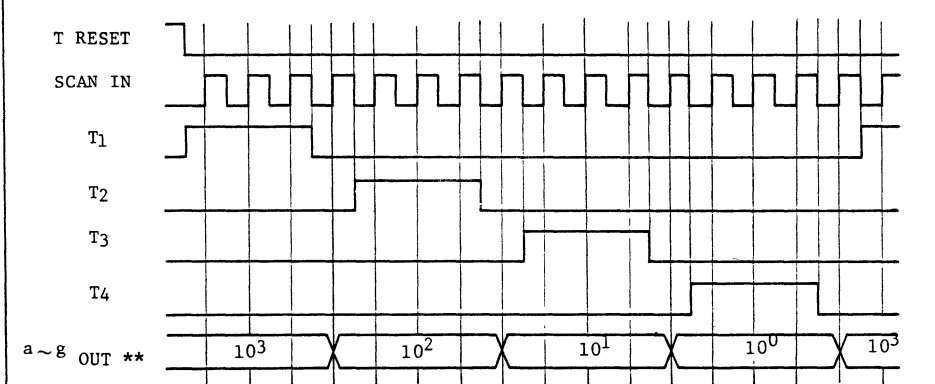
TIMING CHART

COUNT SEQUENCE



* Internal

SCAN SEQUENCE



** Required pull down Register

DESCRIPTION OF PIN FUNCTION

PIN NO.	SYMBOL	NAME	FUNCTION
1	a	SEGMENT a	The segments a ∿ g are the outputs that have convereted the decimal up/down counter BCD outputs into 7-segment display element driving codes. These segment signals are synchronous with SCAN inputs and are dynamically output from the higher order digit. Since they are designed so that I_{OH} is large, they can directly drive a cathod common type LED.
2	b	" b	
3	c	" c	
4	d	" d	
5	e	" e	
6	f	" f	
7	g	" g	
8	T_1	DIGIT SELECT 1	These are the outputs indicating the digits of the outputs a ∿ g and correspond to the higher-order positions from T_1 upward. These outputs are automatically switched in order of T_1 - T_2 - T_3 - T_4 - T_1 by giving clock to SCAN input.
9	T_2	" 2	
10	T_3	" 3	
11	T_4	" 4	
12	V_{SS}	V_{SS}	(GND)
13	BLC	BLANKING CONTROL	"H": No 0 suppression; "L": Reading zero suppression of All digits. The reading 0 suppression of the digits of more than the higher-order(N-1) can be made by connecting this terminal to Tn.
14	R_{EXT}	REGISTER EXTERNAL	SCAN clock is produced by connecting a resistor between R_{EXT} and S_{IN}. In case S_{IN} is externally provided, R_{EXT} should be opened.
15	S_{IN}	SCAN IN	This is a clock input of digit selection counter. If a resistor is connected between S_{IN} and R_{EXT} , SCAN Counter can make self-osillation. (Pulse may be externally applied)
16	TR	T-COUNTER RESET	Operation of SCAN counter can be stopped by "H" level. Whenever TR is fallen, SCAN counter starts scanning from T_1.
17	DOWN	DOWN COUNT	The internal counter makes document at the rising edge of a pulse if the pulse is provided to the in a state where UP input is kept at "H" level.
18	UP	UP COUNT	The internal counter makes up count at the rising edge of a pulse if the pulse is provided to the in a state where DOWN input is kept at "H" level.
19	TEST	TEST	This set to "L" level. (When it is set to "H" level, counting varies with the rising or falling edge.)
20	MR	MASTER RESET	A state of count is cleared to "0000" at the 'H" level.
21	TRF	TRANSFER	In case of "H" level input, the counter contents are always being output through a multiplexer. In case of "L" level input, however, the counter contents before the change to "L" level are not changed by the change in counter contents because the previous contents remain kept in the latch circuit.
22	CARRY	CARRY	In UP COUNT, when the COUNTER contents reaches "9999", "H" level is output as long as UP COUNTER input holds "L" level.
23	BORROW	BORROW	In DOWN COUNT, when the COUNTER contents reaches "0000", "H" level is output as long as DOWN COUNTER input holds "L" level.
24	V_{DD}	V_{DD}	(V_{DD})

TC5053P, TC5054P

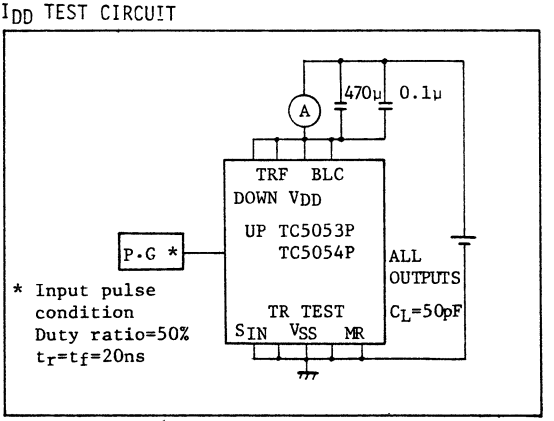
RECOMMENDED OPERATING CONDITION (V_{SS}=0V)

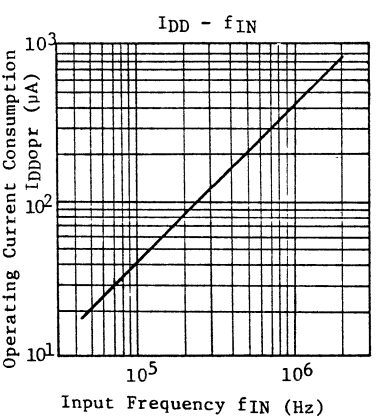
ITEM	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	8	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-30	-	85	°C
R_{EXT} EXTERNAL REGISTANCE	R		5K	-	1M	Ω

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-30°C MIN	-30°C MAX	25°C MIN	25°C TYP	25°C MAX	85°C MIN	85°C MAX	UNIT
High Level Output Voltage	T_1∿T_4,Carry,Borrow	V_{OH}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS},V_{DD}	5	4.95	-	4.95	-	-	4.95	-	V
	a ∿ g				4.0	-	4.0	4.5	-	4.0	-	
	R_{EXT}				4.95	-	4.95	-	-	4.95	-	
Low Level Output Voltage	T_1∿T_4,Carry,Borrow	V_{OL}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS},V_{DD}	5	-	0.05	-	-	0.05	-	0.05	V
	R_{EXT}				-	0.05	-	-	0.05	-	0.05	
High Level Output Current	T_1∿T_4,Carry,Borrow	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16	-	-	-0.12	-	mA
	a ∿ g		V_{OH}=3.5V		-20	-	-20	-	-	-15	-	
	R_{EXT}		V_{OH}=4.6V		-0.02	-	-0.02	-	-	-0.01	-	
Low Level Output Current	T_1∿T_4,Carry,Borrow	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44	-	-	0.36	-	mA
	R_{EXT}				0.02	-	0.02	-	-	0.01	-	
Disable Current (a∿g)		I_{DL}	V_{OL}=0V	8	-	-3.0	-	-10^{-4}	-	-	-3.0	μA
High Level Input Voltage	UP/DOWN CLOCK	V_{IH}		5	3.5	-	3.5	-	-	3.5	-	V
	OTHER				3.5	-	3.5	2.75	-	3.5	-	
Low Level Input Voltage	UP/DOWN CLOCK	V_{IL}		5	-	1.5	-	-	1.5	-	1.5	V
	OTHER				-	1.5	-	2.25	1.5	-	1.5	
High Level Input Current		I_{IH}	V_{IH}=8V	8	-	0.15	-	10^{-5}	0.15	-	1.0	μA
Low Level Input Current		I_{IL}	V_{IL}=0V	8	-	-0.15	-	-10^{-9}	-0.15	-	1.0	
Quiescent Current Consumption		I_{DD}	V_{IN}=V_{SS},V_{DD} OUTPUT OPEN	8	-		-	-		-		μA

I_{DD} TEST CIRCUIT



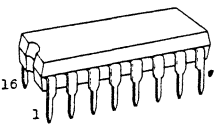


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5064BP
TC5065BP

TC5064BP HEX HIGH VOLTAGE BUFFER WITH INHIBIT/NON INVERTING TYPE
TC5065BP HEX HIGH VOLTAGE BUFFER WITH INHIBIT/INVERTING TYPE

TC5064BP and TC5065BP contain six circuits of buffers having two common INHIBIT inputs (A_{IN}, $\overline{B_{IN}}$).
As both have the output of open drain structure with high bleakdown voltage P-channel MOS FET (-50 volts.. ... Maximum Rating), these are suitable for driving fluorescent display tubes and for interfacing with high voltage MOS LSI's.
TC5064BP is non-inverting type and TC5065BP is inverting type.

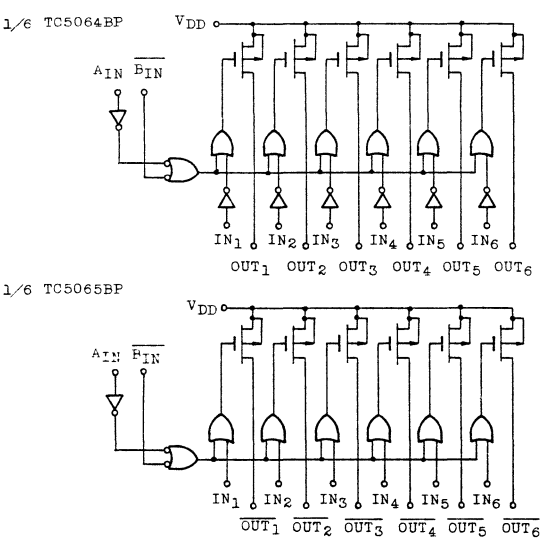


DIP 16 (3D16A-P)

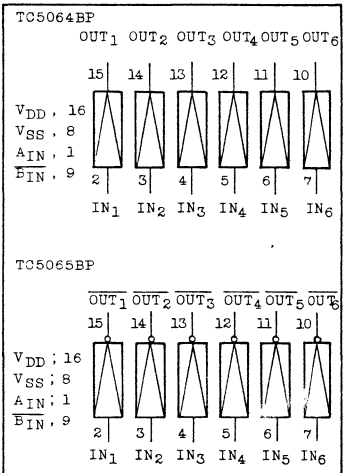
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{DD}-50 ~ V_{DD}+0.5	V
Power Dissipation	P_D	300	mW
DC Input Current	I_{IN}	±10	mA
Storage Temperature Range	T_{stg}	-65 ~150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

LOGIC DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

INPUT			OUTPUT	
A_{IN}	$\overline{B_{IN}}$	IN	TC5064BP	TC5065BP
L	H	L	HZ	H
L	H	H	H	HZ
*	L	*	HZ	HZ
H	*	*	HZ	HZ

HZ ; High Impedance
* ; Don't care

TC5064BP, TC5065BP

RECOMMENDED OPRATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3		18	V
Input Voltage	V_{IN}		0		V_{DD}	V
Operating Temp.	Topr		-40		85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

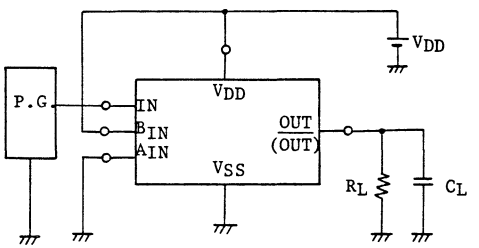
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}$ or V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
High Levle Output Current	I_{OH}	V_{OH}=3V (V_{DD}-2V)	5	- 6	-	- 5	-10	-	- 4	-	mA
		V_{OH}=2V (V_{DD}-3V)	5	- 9	-	- 8	-13	-	- 6	-	
		V_{OH}=7V (V_{DD}-3V)	10	-12	-	-10	-25	-	- 8	-	
		V_{OH}=12V(V_{DD}-3V)	15	-17	-	-15	-35	-	-12	-	
High Level Input Voltage	* V_{IH}	V_{OUT}=0.5V,4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V,9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.5	-	
Low Level Input Voltage	* V_{IL}	V_{OUT}=0.5V,4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V,9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
Output OFF Current	I_{OFF}	V_{OUT} = 0V	15	-	- 3	-	-0.01	-3	-	-10	μA
		V_{OUT} = V_{DD}-45V	15	-	- 10	-	-1	-10	-	- 20	
Input Current	I_{IH}	V_{IH} = 18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	I_{IL}	V_{IL} = 0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}, OUTPUTS OPEN	5	-	4.0	-	0.005	4.0	-	30	μA
			10	-	8.0	-	0.010	8.0	-	60	
			15	-	16.0	-	0.015	16.0	-	120	

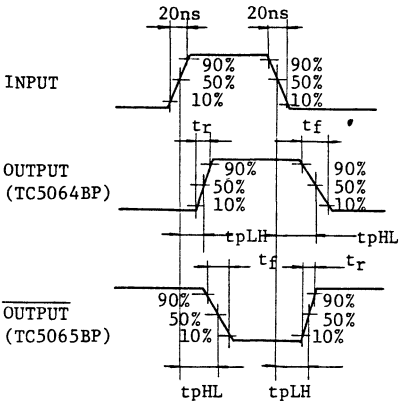
* R_L = 20 kΩ

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_r	R_L = 20 kΩ	5	-	100	200	ns
			10	-	50	100	
			15	-	40	80	
Output Fall Time	t_f	R_L = 20 kΩ	5	-	5.0	8.0	μs
			10	-	5.0	8.0	
			15	-	5.0	8.0	
(LOW-HIGH) Propagation Delay Time	t_{pLH}	R_L = 20 kΩ	5	-	200	500	ns
			10	-	100	250	
			15	-	80	200	
(HIGH-LOW) Propagation Delay Time	tpHL	R_L = 20 kΩ	5	-	2.0	4.0	μs
			10	-	2.0	4.0	
			15	-	2.0	4.0	
Input Capacity	C_{IN}				5	7.5	pF

SWITCHING TIME TEST CIRCUIT AND WAVEFORM

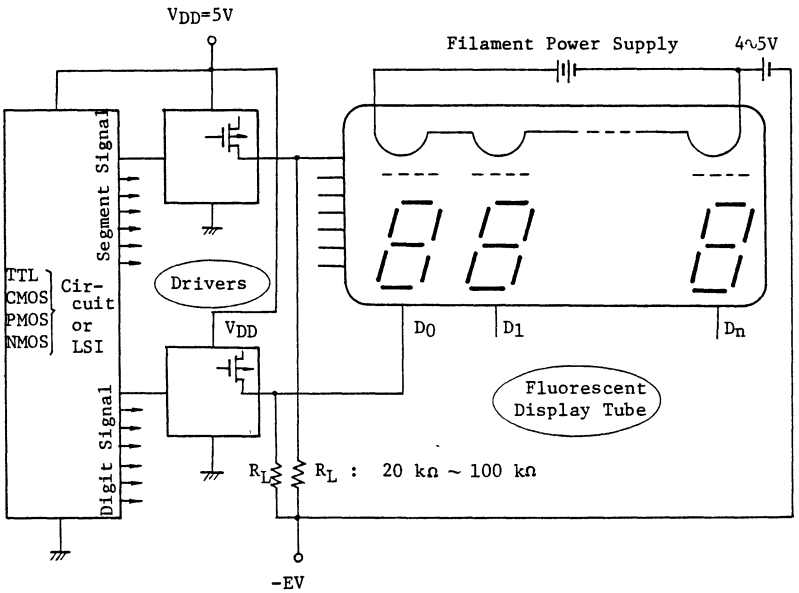




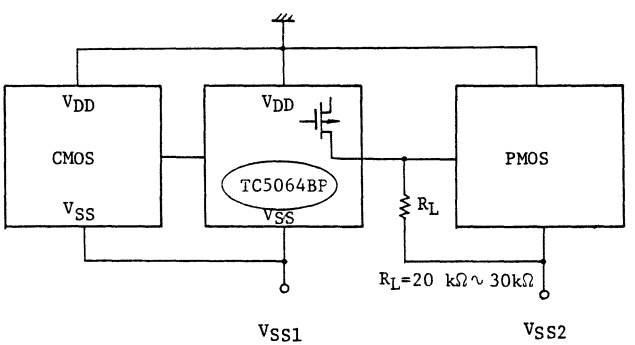
TC5064BP, TC5065BP

EXAMPLES OF APPLICABLE CIRCUITS

(1) Fluorescent Display Tube Driving Circuit



(2) Interface between CMOS and PMOS

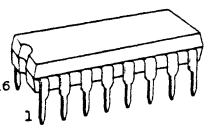


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5066BP
TC5067BP

TC5066BP 7-HIGH VOLTAGE BUFFER/NON INVERTING TYPE
TC5067BP 7-HIGH VOLTAGE BUFFER/INVERTING TYPE

TC5066BP and TC5067BP contain seven independent circuits of buffers. TC5066BP in non-inverting type and TC5067BP is inverting type.
As both have the output of open drain structure with high bleakdown voltage P-channel MOS FET (-50 volts.. .....Maximum Rating), these are suitable for driving fluorescent display tubes and for interfacing with high voltage MOS LSI's.



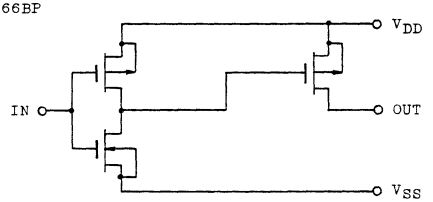
DIP 16 (3D16A-P)

ABSOLUTE MAXIMUM RATINGS

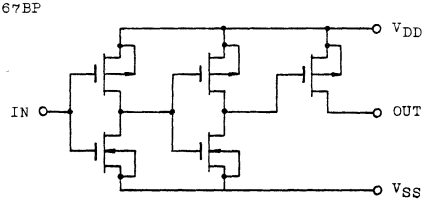
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{DD}-50 ~ V_{DD}+0.5	V
Power Dissipation	P_D	300	mW
DC Input Current	I_{IN}	±10	mA
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

LOGIC DIAGRAM

1/7 TC5066BP

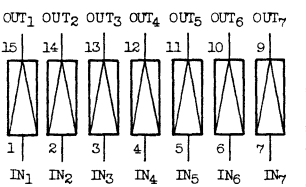


1/7 TC5067BP



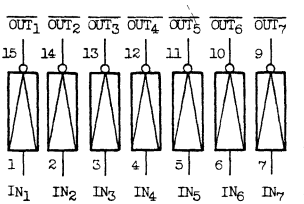
PIN ASSIGNMENT

TC5066BP



V_{DD} , 16 , V_{SS} ; 8

TC5067BP



V_{DD} ; 16 , V_{SS} , 8

TC5066BP, TC5067BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3		18	V
Input Voltage	V_{IN}		0		V_{DD}	V
Operating Temp.	Topr		-40		85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

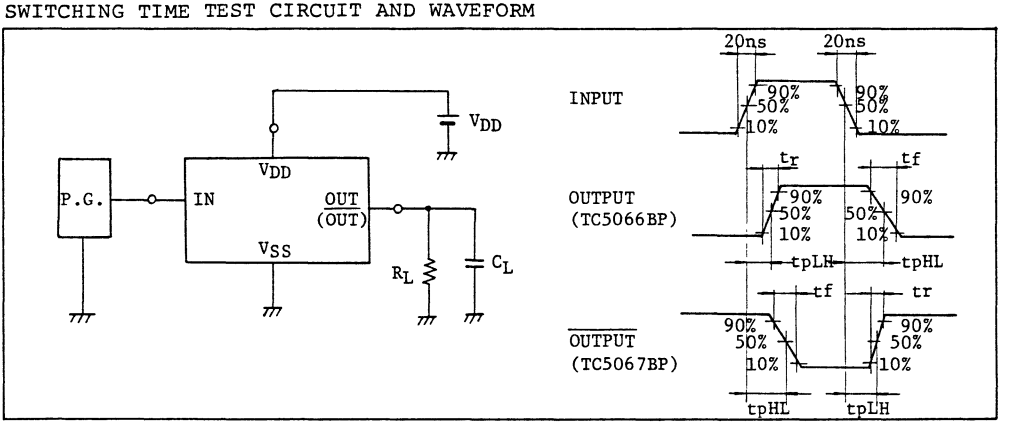
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}$ or V_{DD}	5 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.00 10.00 15.00	- - -	4.95 9.95 14.95	- - -	V
High Level Output Current	I_{OH}	V_{OH}=3V (V_{DD}-2V) V_{OH}=2V(V_{DD}-3V) V_{OH}=7V(V_{DD}-3V) V_{OH}=12V(V_{DD}-3V) $V_{IN}=V_{SS}$ or V_{DD}	5 5 10 15	- 6 - 9 -12 -17	- - - -	- 5 - 8 -10 -15	-10 -13 -25 -35	- - - -	- 4 - 6 - 8 -12	- - - -	mA
High Level Input Voltage (TC5066BP)	V_{IH}	V_{OUT}=4.5V V_{OUT}=9.0V V_{OUT}=13.5V *	5 10 15	4.0 8.0 12.5	- - -	4.0 8.0 12.5		- - -	4.0 8.0 12.5	- - -	V
Low Level Input Voltage (TC5066BP)	V_{IL}	V_{OUT}=0.5V V_{OUT}=1.0V V_{OUT}=1.5V *	5 10 15	- - -	1.0 2.0 2.5	- - -		1.0 2.0 2.5	- - -	1.0 2.0 2.5	
High Level Input Voltage (TC5067BP)	V_{IH}	V_{OUT}=0.5V V_{OUT}=1.0V V_{OUT}=1.5V *	5 10 15	3.5 7.0 11.0	- - -	3.5 7.0 11.0	2.75 5.5 8.25	- - -	3.5 7.0 11.0	- - -	V
Low Level Input Voltage (TC5067BP)	V_{IL}	V_{OUT}=4.5V V_{OUT}=9.0V V_{OUT}=13.5V *	5 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.5 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	
Output OFF Leak Current	I_{OFF}	V_{OUT} = 0V V_{OUT} = -30V	15 15	- -	3 10	- -	0.01 1	3 10	- -	10 20	μA
Input Current H Level	I_{IH}	V_{IH} = 18V	18	-	0.3	-	10^5	0.3	-	1.0	μA
Input Current L Level	I_{IL}	V_{IL} = 0V	18	-	-0.3	-	10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current	I_{DD}	V_{IN} = V_{DD}, V_{SS} Outputs Open	5 10 15	- - -	4.0 8.0 16.0	- - -	0.005 0.010 0.015	4.0 8.0 16.0	- - -	30 60 120	μA

* R_L = 20 kΩ

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_r	R_L = 20 kΩ	5	-	100	200	ns
			10	-	50	100	
			15	-	40	80	
Output Fall Time	t_f	R_L = 20 kΩ	5	-	5.0	8.0	μs
			10	-	5.0	8.0	
			15	-	5.0	8.0	
(LOW-HIGH) Propagation Delay Time	tpLH	R_L = 20 kΩ	5	-	200	500	ns
			10	-	100	250	
			15	-	80	200	
(HIGH-LOW) Propagation Delay Time	tpHL	R_L = 20 kΩ	5	-	2.0	4.0	μs
			10	-	2.0	4.0	
			15	-	2.0	4.0	
Input Capacity	C_{IN}			-	5	7.5	pF

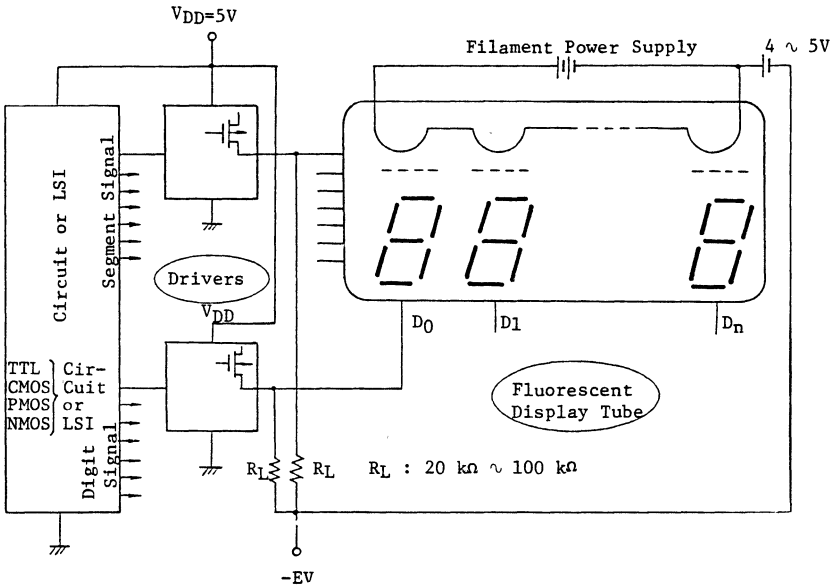
SWITCHING TIME TEST CIRCUIT AND WAVEFORM



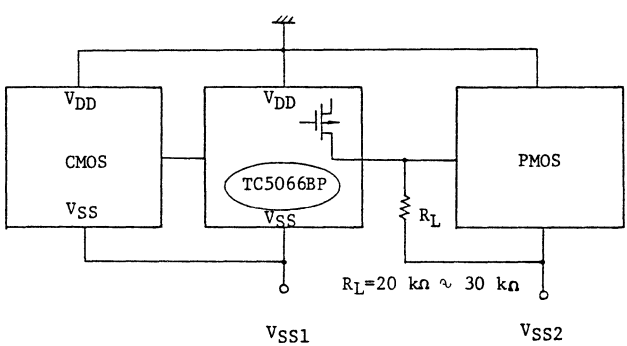
TC5066BP, TC5067BP

EXAMPLES OF APPLICABLE CIRCUITS

(1) Fluorescent Display Tube Driving Circuit



(2) Interface between CMOS and PMOS

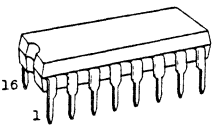


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5068BP
TC5069BP

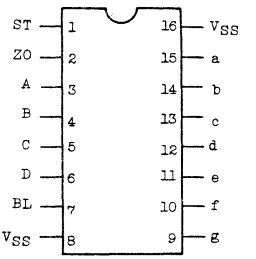
TC5068BP, TC5069BP BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

The TC5068BP and TC5069BP are decoders which convert the inputs of BCD codes into the 7-segment display element driving signals. Since the segment output is of an open drain structure with high breakdown voltage P-channel FET, these decoders can directly drive fluorescent display tubes.
Each of four input lines contains a latch controlled by common strobe input, to facilitate static drive.
Each BL input is used for forcing all the segments to the OFF state; therefore, the decoders can be applied to the leading zero suppress by combining zero output (When input code is at "0", "H" level is output).
The TC5068BP is of a hexadecimal display indicating type, and the TC5069BP is of a BCD display puls "L", "H", "A", "P", "-", and "blank" display indicating type.



DIP 16 (3D16A-P)

PIN ASSIGNMENT

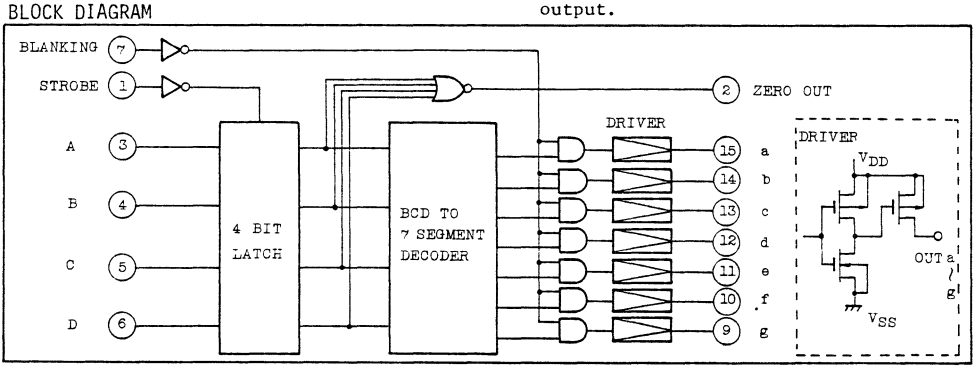


ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage *	V_{OUT1}	V_{DD}-50 ~ V_{DD}+0.5	V
	V_{OUT2}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C

* V_{OUT1} is applied to segment output, and V_{OUT2} to zero output.

BLOCK DIAGRAM



TC5068BP, TC5069BP

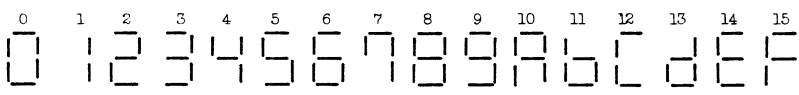
TRUTH TABLE

INPUTS						OUTPUTS													
						TC5068BP △							TC5069BP △						ZERO OUT
ST	BL	D	C	B	A	a	b	c	d	e	f	g	a	b	c	d	e	f	g	
※	H	※	※	※	※	L	L	L	L	L	L	L	L	L	L	L	L	L	L	☆
H	L	L	L	L	L	H	H	H	H	H	H	L	H	H	H	H	H	H	L	H
H	L	L	L	L	H	L	H	H	L	L	L	L	L	H	H	L	L	L	L	L
H	L	L	L	H	L	H	H	L	H	H	L	H	H	H	L	H	H	L	H	L
H	L	L	L	H	H	H	H	H	H	L	L	H	H	H	H	H	L	L	H	L
H	L	L	H	L	L	L	H	H	L	L	H	H	L	H	H	L	L	H	H	L
H	L	L	H	L	H	H	L	H	H	L	H	H	H	L	H	H	L	H	H	L
H	L	L	H	H	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	L
H	L	L	H	H	H	H	H	H	L	L	H	L	H	H	H	L	L	H	L	L
H	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H	L	H	H	L
H	L	H	L	H	L	H	H	H	L	H	H	H	L	L	L	H	H	H	L	L
H	L	H	L	H	H	L	L	H	H	H	H	H	L	H	H	L	H	H	H	L
H	L	H	H	L	L	H	L	L	H	H	H	L	H	H	H	L	H	H	H	L
H	L	H	H	L	H	L	H	H	H	H	L	H	H	H	L	L	H	H	H	L
H	L	H	H	H	L	H	L	L	H	H	H	H	L	L	L	L	L	L	H	L
H	L	H	H	H	H	H	L	L	L	H	H	H	L	L	L	L	L	L	L	L
L	L	※	※	※	※	△△														

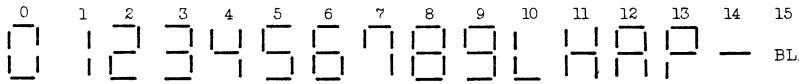
※ ; Don't care
☆ ; Undetermined
△△ ; Depends Upon the BCD code previously applied when ST = "H"
△ ; Required pull down resister "R_L"

DISPLAY INDICATING TYPE

TC5068BP



TC5069BP



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

項目	記号		MIN	TYP	MAX	単位
電源電圧	V_{DD}		3	—	18	V
入力電圧	V_{IN}		0	—	V_{DD}	V

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}$ or V_{DD}	5 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.00 10.00 15.00	- - -	4.95 9.95 14.95	- - -	V
Low Level Output Voltage (ZERO OUT)	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}$ or V_{DD}	5 10 15	- - -	0.05 0.05 0.05	- - -	0.00 0.00 0.00	0.05 0.05 0.05	- - -	0.05 0.05 0.05	V
High Level Output Current (Segment OUT)	I_{OH}	V_{OH}= 3V(V_{DD}-2V) V_{OH}= 2V(V_{DD}-3V) V_{OH}= 7V(V_{DD}-3V) V_{OH}=12V(V_{DD}-3V) $V_{IN}=V_{SS}$ or V_{DD}	5 5 10 15	-6 -9 -12 -17	- - - -	-5 -8 -10 -15		- - - -	-4 -6 -8 -12	- - - -	mA
High Level Output Current (Zero OUT)	I_{OH}	V_{OH}= 4.6V V_{OH}= 9.5V V_{OH}=13.5V $V_{IN}=V_{SS}$ or V_{DD}	5 10 15	-0.2 -0.5 -1.4	- - -	-0.16 -0.4 -1.2		- - -	-0.12 -0.3 -1.0	- - -	mA
Low Level Output Current (Zero OUT)	I_{OL}	V_{OL}=0.4V V_{OL}=0.5V V_{OL}=1.5V $V_{IN}=V_{SS}$ or V_{DD}	5 10 15	0.52 1.3 3.6	- - -	0.44 1.1 3.0		- - -	0.36 0.9 2.4	- - -	mA
High Level Input Voltage	V_{IH} *	V_{OUT}=0.5, 4.5V V_{OUT}=1.0, 9.0V V_{OUT}=1.5, 13.5V $\|I_{OUT}\| < 1\mu A$	5 10 15	3.5 7.0 11.0	- - -	3.5 7.0 11.0	2.75 5.5 8.25	- - -	3.5 7.0 11.0	- - -	V
Low Level Input Voltage	V_{IL} *	V_{OUT}=0.5, 4.5V V_{OUT}=1.0, 9.0V V_{OUT}=1.5,13.5V $\|I_{OUT}\| < 1\mu A$	5 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.5 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	V
Output Off-leak Current (Segment OUT)	I_{OFF}	V_{OUT}=0V V_{OUT}=-30V	15 15	- -	-3 -10	- -	-0.01 -1	-3 -10	- -	-10 -20	μA
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3		-1.0	μA
Quiescent Supply Current	I_{DD}	$V_{IN}=V_{SS}$ or V_{DD} Outputs Open **	5 10 15	- - -	20 40 80	- - -	0.005 0.010 0.015	20 40 80	- - -	150 300 600	μA

* R_L = 20 kΩ

** All valid input combinations.

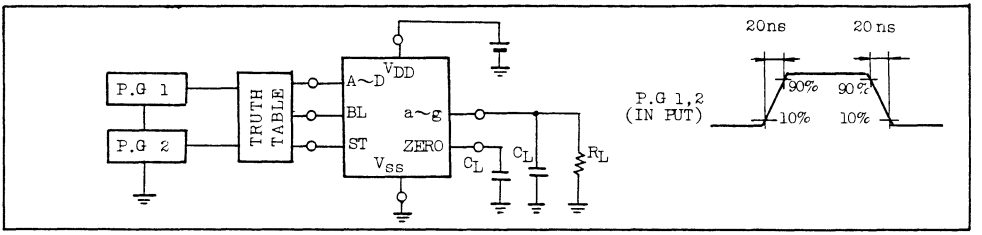
TC5068BP, TC5069BP

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

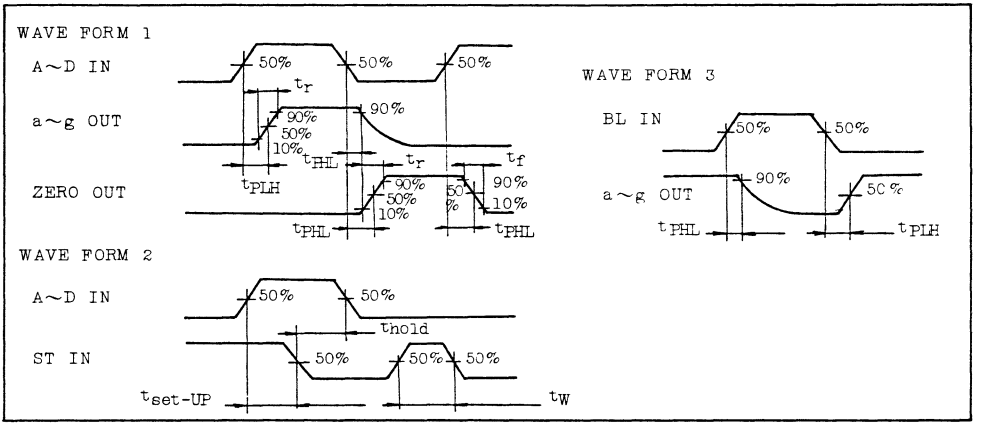
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time (SEGMENT OUT)	t_r	R_L = 1 kΩ	5	-	100	200	ns
			10	-	50	100	
			15	-	40	80	
Output Rise Time (ZERO OUT)	t_r		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Fall Time (ZERO OUT)	t_f		5	-	100	200	
			10	-	50	100	
			15	-	40	80	
(Low-High) Propagation Delay Time (A,B,C,D-SEGMENT OUT)	t_{PLH}	R_L = 1 kΩ	5	-	750	1800	ns
			10	-	300	600	
			15	-	200	400	
(High-Low) Propagation Delay Time (A,B,C,D-SEGMENT OUT)	t_{PHL}	R_L = 1 kΩ	5	-	750	1800	
			10	-	300	600	
			15	-	200	400	
(Low-High) Propagation Delay Time (A,B,C,D-ZERO OUT)	t_{PLH}		5	-	250	500	ns
			10	-	125	250	
			15	-	100	200	
(High-Low) Propagation Delay Time (A,B,C,D-ZERO OUT)	t_{PHL}		5	-	250	500	
			10	-	125	250	
			15	-	100	200	
(Low-High) Propagation Delay Time (BL-SEGMENT OUT)	t_{PLH}	R_L = 1 kΩ	5	-	200	400	ns
			10	-	100	200	
			15	-	80	160	
(High-Low) Propagation Delay Time (BL-SEGMENT OUT)	t_{PHL}	R_L = 1 kΩ	5	-	200	400	
			10	-	100	200	
			15	-	80	160	
Minimum ST Pulse Width	t_w (ST)		5	-	60	200	ns
			10	-	30	100	
			15	-	25	80	
Minimum Setup Time (ST-A,B,C,D IN)	t_{set-UP}		5	-	35	200	ns
			10	-	20	100	
			15	-	10	80	
Minimum Hold Time (ST-A,B,C,D IN)	t hold		5	-	-	100	
			10	-	-	60	
			15	-	-	40	
Input Capacitance	C_{IN}			-	5	7.5	pF

TC5068BP, TC5069BP

SWITCHING TIME TEST CIRCUIT

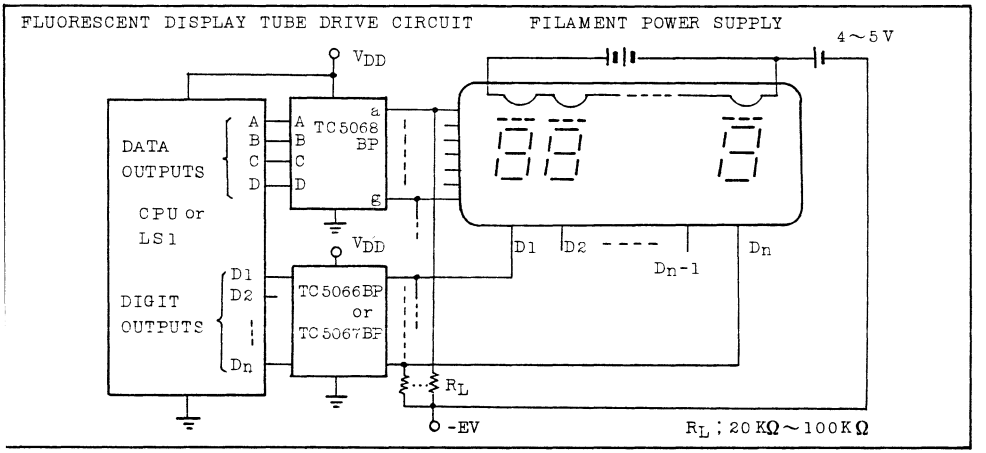


SWITCHING TIME TEST WAVEFORM



APPLICATION EXAMPLE

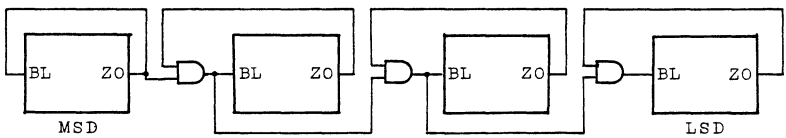
FLUORESCENT DISPLAY TUBE DRIVE CIRCUIT



TC5068BP, TC5069BP

APPLICATION EXAMPLE

LEADING ZERO SUPPRESS CIRCUIT (STATIC DRIVE)



C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

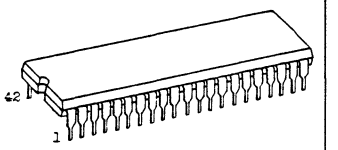
TC5070P, TC5071P
TC5972P

TENTATIVE

TC5070P/TC5071P/TC5072P 6 DIGIT UNIVERSAL COUNTER

TC5070P/TC5071P/TC5072P are 6-digit universal counter containing 6-digit memory register in addition to functions of up/down counting, data presetting, zero suppress, and latch.
The counted contents are output in BCD and seven segment dynamically stepwise from most significant digit in synchronization with input of SCAN.
The seven-segment output can directly drive the common cathode type LED.
In addition to CARRY and ZERO outputs, these counter are provided with EQUAL output, permitting a wide range of applications such as for measuring instruments, timers, etc.

Maximum counting value
TC5070P 999999 COUNTER
TC5071P 995959 TIMER
TC5072P 595999 TIMER

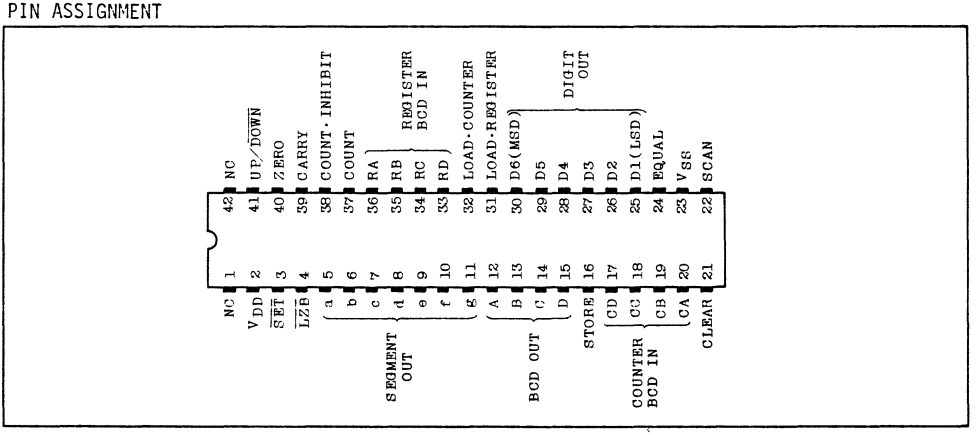


DIP 42 (6D42A-P)

ABSOLUTE MAXIMUM RATINGS

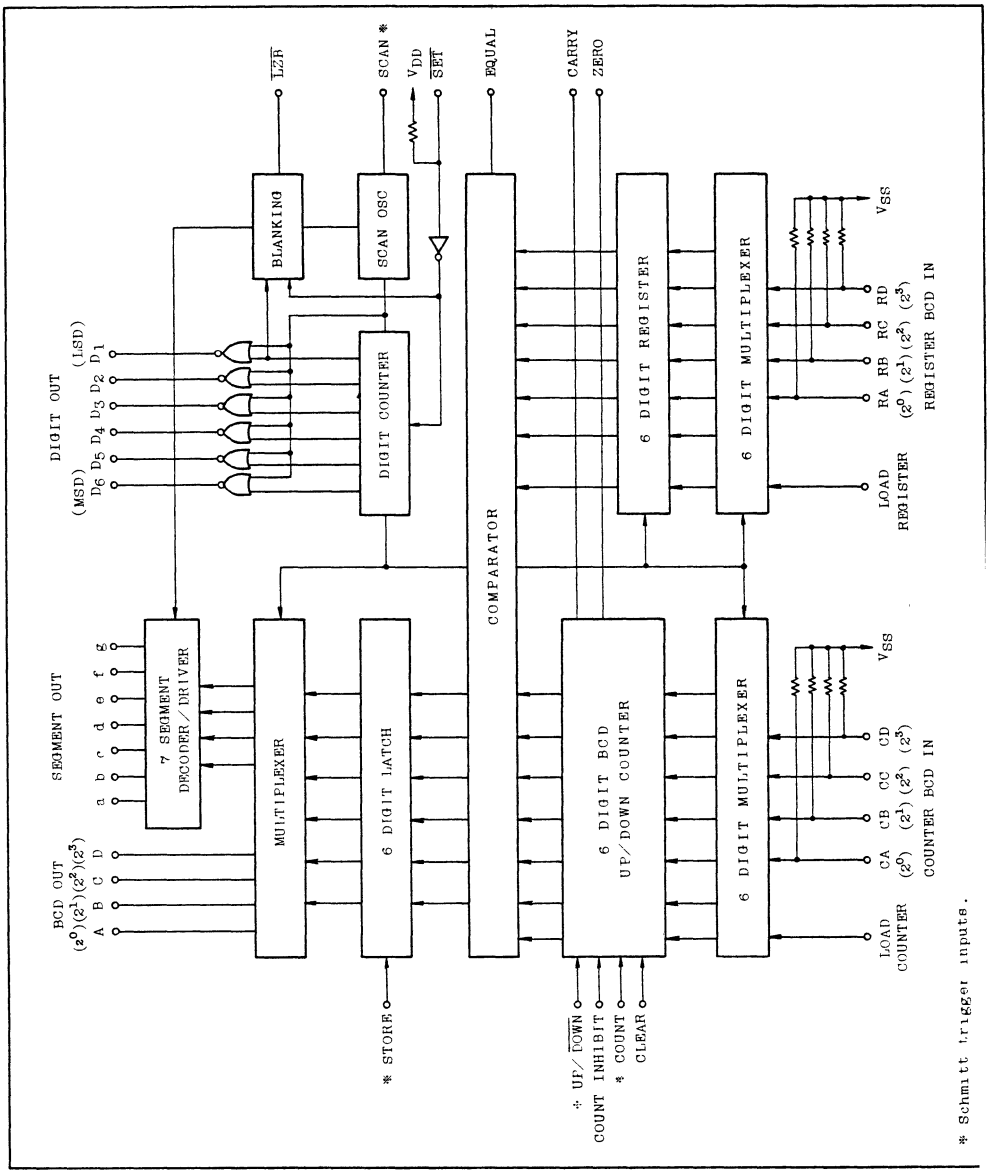
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-65~150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



TC5070P, TC5071P, TC5072P

BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTION

PIN No.	SYMBOL	FUNCTION	
1	NC	No connection	
2	V_{DD}	V_{DD} power supply (3-8V)	
3	$\overline{SET}$	At "L" level, the digit counter is reset, and D6 (MSD) only provide. The Segment-out changes to the blanking state. At "H" level, normal display operation.	
4	$\overline{LZB}$	"H"	No zero blanking
		"L"	Leading zero blanking in the higher order 5 digits.
5	a	Each pin is seven segment output of 6-digit counter. The output is synchronized with the digit-out and is provided stepwise from the most significant digit.	
6	b		
7	c		
8	d		
9	e		
10	f		
11	g		
12	A	Each pin is BCD output of 6-digit counter. The output is synchronized with the digit-out and is provided stepwise from the most significant digit. When $\overline{SET}$ input is at "L" level, the most significant digit data is provided.	
13	B		
14	C		
15	D		
16	STORE	"H"	At positive edge of the STORE input, the contents of the counter are latched.
		"L"	The contents of the counter are straight transferred to the miltiplexer.
17	CD	BCD input at the time when data are preset to the 6-digit counter. (With the LOAD COUNTER input at "H" level.)	
18	CC		
19	CB		
20	CA		
21	CLEAR	At "H" level, the 6-digit counter is reset, and the contents of the counter become ALL "0". ZERO output become at "H" level.	
22	SCAN	Auto scan oscillator is operated by connecting a capacitor (2000-20000pF) between No.22 (SCAN) and No.23 (V_{SS}) terminals. External scan oscillator may also be used to drive the scan input.	
23	V_{SS}	GND (0V)	

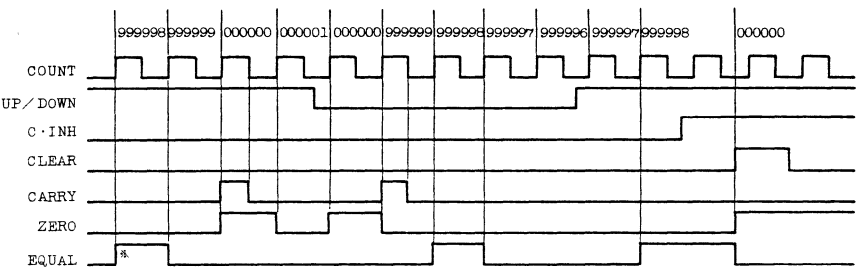
TC5070P, TC5071P, TC5072P

DESCRIPTION OF PIN FUNCTION (Cont'd)

PIN No.	SYMBOL	FUNCTION	
24	EQUAL	When the contents of the 6-digit register set by the input of RA, RB, RC, and RD coincide with the contents of 6-digit counter, EQUAL output is provided at "H" level. Even if both the contents coincide each other during setting by the inputs of LOAD REGISTER and LOAD COUNTER, the output is inhibited and "L" level remains unchanged.	
25	D1(LSD)	These are the outputs to display the digits of segment out and BCD-out. When $\overline{SET}$ input reaches "L" level, the digit counter is reset and D6 (MSD) only is provided. When $\overline{SET}$ input rises at "H" level, the output is provided in the order of D5, D4...in synchronization with the SCAN clock.	
26	D2		
27	D3		
28	D4		
29	D5		
30	D6(MSD)		
31	LOAD·REGISTER (LOAD·R)	"H"	RA ~ RD input is set to 6-digit register.
		"L"	Write operation to the register is inhibited.
32	LOAD·COUNTER (LOAD·C)	"H"	CA ~ CD input is preset to the 6-digit counter.
		"L"	Write operation to the counter is inhibited.
33	RD	BCD input at the time when the data are set to the 6-digit register. (With the LOAD REGISTER input at "H" level.)	
34	RC		
35	RB		
36	RA		
37	COUNT	Clock input of 6-digit counter (Counting at the positive edge of clock)	
38	COUNT·INHIBIT (C·INH)	"H"	No counting
		"L"	Counting
39	CARRY	When the contents of counter have become "000000" at time of up-counting, CARRY output is provided at "H" level during this time from rise to fall of COUNT input. When the contents of counter have become "999999" (for TC5070P) "995959" (for TC5071P), and "595999" (for TC5072P) at time of down-counting, CARRY output is also provided at "H" level during this time from rise and fall of COUNT input.	
40	ZERO	When the contents of counter have become "00000", ZERO is provided at "H" level. During presetting by the LOAD COUNTER input, output operation is inhibited and "L" level remains unchanged.	
41	UP/DOWN	"H"	Up count.
		"L"	Down count.
42	NC	No connection.	

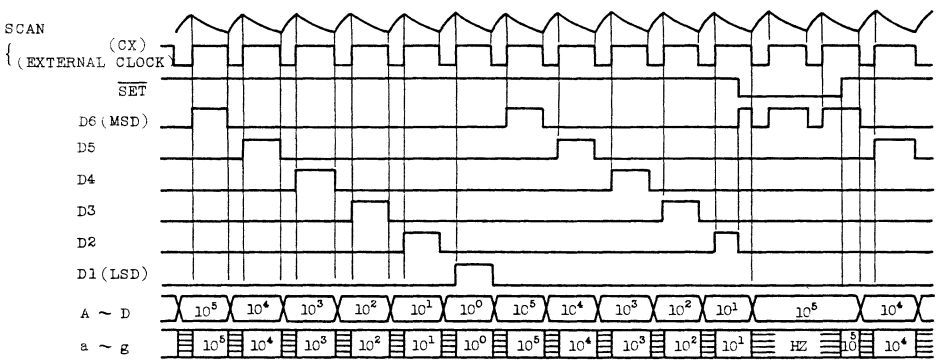
TIMING CHART

6 DIGIT COUNTER TIMING CHART (TC5070P) ; LOAD·C, LOAD·R= 'L'



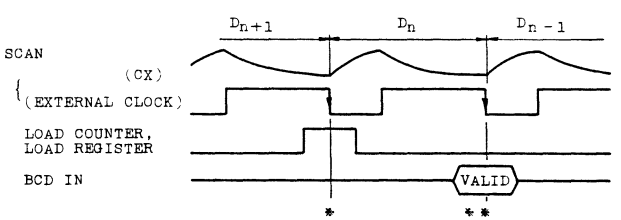
* Register value is preset to 999998.

DIGIT COUNTER TIMING CHART



HZ High impedance. (Segment driver off.)

LOAD REGISTER, LOAD COUNTER TIMING CHART



* : Timing where data is permitted to be written at the nth digit.

** : Timing where data is written at the nth digit.

TC5070P, TC5071P, TC5072P

OPERATING CONSIDERATION

1. COUNTER OPERATION

   Counting is stepped by the rise of clock when the clock is added to COUNT input at state of the inputs of LOAD·C, C·INH, and CLEAR at "L" level. At time of up-counting, CARRY and ZERO outputs are "H" level at "000000", and at time of down-counting, CARRY output is at "H" level at "999999" (for TC5070P), "995959" (for TC5071P), and "595999: (for TC5072P).

   When CARRY output is at "H" level, CARRY output remain at "H" leve until COUNT input falls, even if CLEAR and LOAD·C inputs are changed to "H" level.

   For COUNT and UP/$\overline{\text{DOWN}}$ inputs is shaped schmitt trigger, COUNT and UP/$\overline{\text{DOWN}}$ inputs rarely miscounts if waveform is not sharp.

2. COMPARATOR OPERATION

   EQUAL output is provided at "H" level, when the contents of the counter coincide with the comparator value set by LOAD·R input. However, even if they concide each other during setting by LOAD·C and LOAD·R input, output operation is inhibited and "L" level remains unchanged.

3. LOAD COUNTER AND LOAD REGISTER OPERATIONS

   When the data required to preset the counter or when the comprating value is required to set to the register, such operation is made by LOAD·C and LOAD·R input. The presetting of data to the counter is acquired by setting LOAD·C input to "H" level, synchronizing CA ~ CD input with the digit counter, and setting the digits one after another. For the purpose, the external circuits are required for timing of D6 ~ D1 output with CA ~ CD input. The comprator value can be set to the register in the same way. Load register operation is independently of counting operation; therfore, even during setting of the data to the register, counting can be performed. (See an example of input setting circuits.)

   (Note) that normal operation is not acquired when the data exceeding the maximum counting value (for each digit) shown on page 1 for the individual items are set to the counter and register.

4. LATCH OPERATION

   At STORE input is at "L" level, the contents of counter are straight transferred to the multiplexer, and the output indicates the contents of counter.

   At STORE input is at "H" level, the indicating output remains unchanged although the count varies for the contents of counter are latched at the positive edge of

OPERATING CONSIDERATION (Cont'd)

STORE input. When STORE is turned to "L" level, the contents of counter at that time are provided. STORE input shape schmitt trigger.

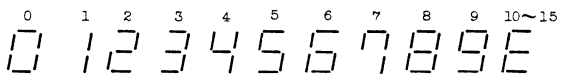
5. DISPLAY OPERATION

At $\overline{LZB}$ input is at "L" level, the higher order 5 digits of SEGMENT-OUT output are changed to the state of leading zero blanking.

At "H" level, the function of leading zero blanking is released.

At $\overline{SET}$ input is at "L" level, the SEGMENT-OUT output is changed to the state of blanking, and the digit counter is reset, and D6 (MSD) only is provided. At that time, the BCD-OUT output provided the data of the 6th digit. At "H" level, the DIGIT-OUT output provided in the order of D6, D5, D4, ... in synchronization with SCAN, and SEGMENT-OUT and CD-OUT output are also provided in synchronization.

Segment Display Format (Common Cathod type LED)



6. SCANNING OPERATION

AUTO SCAN operation can be performed by inserting a capacitor between the terminal SCAN and the terminal V_{SS}. By adding an external clock to the terminal SCAN, MANUAL SCAN operation can be performed.

SCAN OSC actuates the digit counter, and at the AUTO SCAN operation, the digit blanking is applied to each DIGIT OUT for the T/150 period of one cycle (T) of SCAN OSC, therfore, can be prevented overlap of each DIGIT OUT. One cycle of DIGIT OUT is equal to 6 cycles of SCAN OSC.

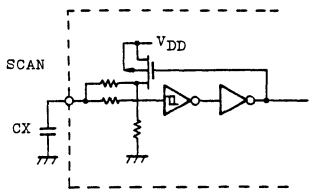
SCAN signal synchronize with data signal setting by the LOAD REGISTER and/or LOAD COUNTER inputs. An external capacitor of 2000 to 20000pF is required for SCAN (CX).

(Note) BCD-OUT output may involve some hazards at the change of COUNT input and DIGIT-OUT output; However, such hazards do not hinder operation because they occur during the blanking hours for DIGIT-OUT and SEGMENT-OUT output.

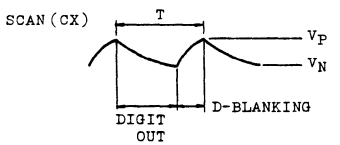
TC5070P, TC5071P, TC5072P

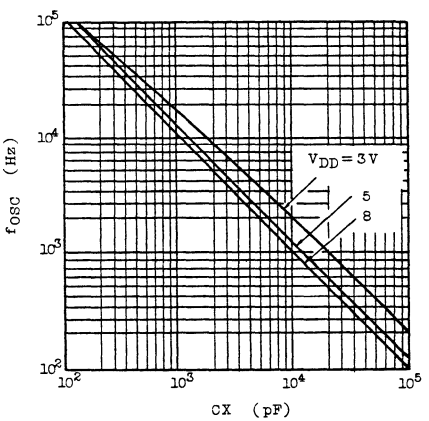
OPERATING CONSIDERATION (Cont'd)

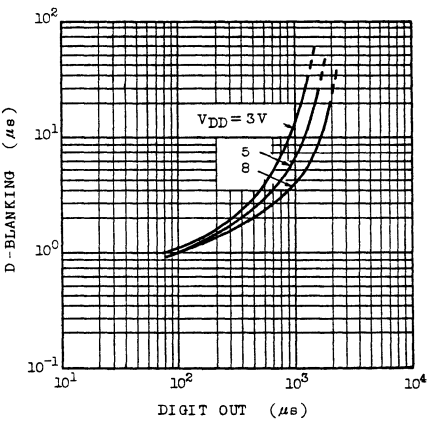
SCAN OSC



$$f_{OSC} = \frac{1}{T} \text{ (Hz)} \quad \text{(TYP.) } 25℃$$







RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	8	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature Range	T_{opr}		-40	-	85	°C

TATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
igh-Level Output oltage Except SEGMENT OUTPUT)	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
ow-Level Output oltage Except SEGMENT OUTPUT)	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
igh-Level Output oltage SEGMENT OUTPUT)	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.0	-	4.0	4.5	-	4.0	-	
utput High Current A~D, EQ, CA, ZE OUTPUT)	I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.2	-	-0.16	-0.8	-	-0.12	-	mA
utput High Current D1~D6 OUTPUT)	I_{OH}	V_{OH}=4.2V $V_{IN}=V_{SS},V_{DD}$	5	-0.75	-	-0.7	-1.5	-	-0.6	-	
utput Low Current Except SEGMENT OUTPUT)	I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	0.52	-	0.44	1.2	-	0.36	-	
utput High Current SEGMENT OUTPUT)	I_{OH}	V_{OH}=3.5V $V_{IN}=V_{SS},V_{DD}$	5	-25	-	-25	-50	-	-20	-	
nput Low Voltage Except Schmitt Trigger Input)	V_{IH}	V_{OH}=4.0V V_{OL}=0.5V $\|I_{OUT}\|<1\mu A$	5	3.5	-	3.5	2.75	-	3.5	-	V
nput High Voltage Except Schmitt Trigger Input)	V_{IL}	V_{OH}=4.0V V_{OL}=0.5V $\|I_{OUT}\|<1\mu A$	5	-	1.5	-	2.15	1.5	-	1.5	
igh-Level Input urrent Except Pull Up/ Down Resistance Input)	I_{IH}	V_{IH}=8V	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA

TC5070P, TC5071P, TC5072P

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Low-Level Input Current (Except Pull Up/ Down Resistance Input)	I_{IL}	V_{IL}=0V	8	-	-0.3	-	10^{-5}	-0.3	-	-1.0	
High-Level Input Current ($\overline{SET}$ IN)	I_{IH}	V_{IH}=8V	8	-	5.0	-	-	5.0	-	5.0	
Low-Level Input Current ($\overline{SET}$ IN)	I_{IL}	V_{IL}=0V	8	-	-180	-	-70	-160	-	-140	μA
High-Level Input Current (CA~CD, RA~RD, SCAN IN)	I_{IH}	V_{IH}=8V	8	-	180	-	80	160	-	140	
Low-Level Input Current (CA~CD, RA~RD IN)	I_{IL}	V_{IL}=0V	8	-	-5.0	-	-	-5.0	-	-5.0	
Low-Level Input Current (SCAN IN)	I_{IL}	V_{IL}=0V	5	-	-2.3	-	-1.0	-2.0	-	-1.8	mA
			8	-	-3.6	-	-1.6	-3.2	-	-2.8	
Output Leakage Current (SEGMENT OUT)	I_{DL}	V_{OL}=0V	8	-	-3.0	-	-10^{-4}	-3.0	-	-1.5	μA
Quiescent Device Current	I_{DD}	SCAN=V_{DD} $\overline{SET}$, CA~CD, RA~RD OPEN	5	-	750	-	180	500	-	1000	μA
			8	-	1500	-	250	1000	-	2000	

)YNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{DD}=5.0V, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
)utput Transition Time (Low to High)	t_r	SEGMENT OUT (R_L=1kΩ)	-	70	200	ns
	t_r	OTHER OUT	-	100	400	
)utput Transition Time (High to Low)	t_f	Except SEGMENT OUT	-	70	200	
'ropagation Delay Time	t_{pLH}, t_{pHL}	COUNT-BCD, SEGMENT OUT (R_L=1kΩ)	-	750	1500	
	t_{pLH}, t_{pHL}	COUNT-CARRY OUT	-	150	400	
	t_{pLH}, t_{pHL}	COUNT-ZERO OUT	-	200	400	
	t_{pLH}, t_{pHL}	COUNT-EQUAL OUT	-	270	500	
	t_{pLH}, t_{pHL}	SCAN-DIGIT OUT	-	250	500	
	t_{pLH}, t_{pHL}	SCAN-BCD OUT	-	750	1500	
'ropagation Delay Time	t_{pLH}	SCAN-SEGMENT OUT (R_L=1kΩ)	-	500	1000	
	t_{pHL}	SCAN-SEGMENT OUT (R_L=1kΩ)	-	300	700	
lax. Clock Frequency	f_{MAX-1}	COUNT IN *	2.0	4.0	-	MHz
	f_{MAX-2}		1.0	1.6	-	
	f_{MAX}	SCAN IN	0.5	1.0	-	
lin. Pulse Width	t_w	CLEAR IN	-	250	500	ns
	t_w	STORE IN	-	80	160	
in. Set-up Time	t_{set-up}	COUNT-STORE	-	70	150	
	t_{set-up}	COUNT-UP/$\overline{\text{DOWN}}$	-	230	500	
	t_{set-up}	STORE-CLEAR	-	130	300	
	t_{set-up}	COUNT-C·IN	-	0	100	
	t_{set-up}	SCAN IN-LOAD·C, LOAD·R	-	-40	50	
	t_{set-up}	SCAN IN-BCDIN	-	200	450	
in. Hold Time	t_{hold}	COUNT-UP/$\overline{\text{DOWN}}$	-	40	150	
	t_{hold}	SCAN IN-LOAD·C, LOAD·R	-	70	200	
	t_{hold}	SCAN IN-BCDIN	-	140	300	
in. Removal Time	t_{rem}	COUNT-CLEAR	-	60	150	
ax. Input Rise/Fall ime	$t_{r\phi}$	Except Schmitt Trigger Input	20	-	-	μs
	$t_{f\phi}$	Except Schmitt Trigger Input	20	-	-	
ositive Trigger hreshold Voltage	V_P		-	3.0	4.0	V
egative Trigger hreshold Voltage	V_N		1.0	1.8	-	
ysteresis Voltage	V_H		0.5	1.2	-	

TC5070P, TC5071P, TC5072P

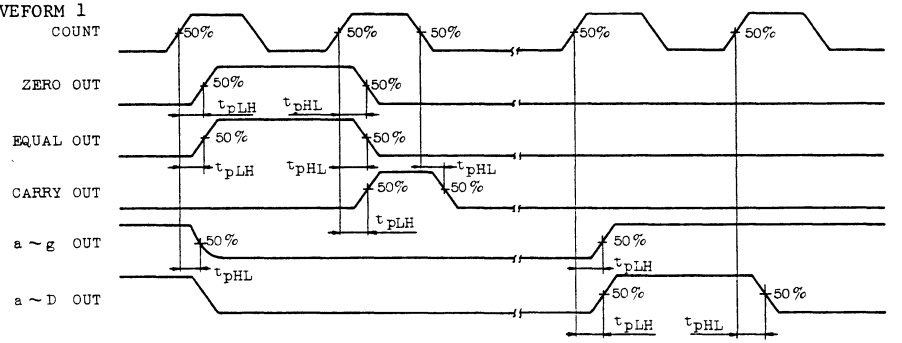
DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{DD}=5.0V, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Device Current (C_X=2000 ~ 20000pF)	I_{DD}	COUNT IN = H & L	-	250	-	μA
		COUNT IN = 1 MHz	-	650	-	
Input Capacitance	C_{IN}	Except SCAN IN	-	5.0	7.5	pF

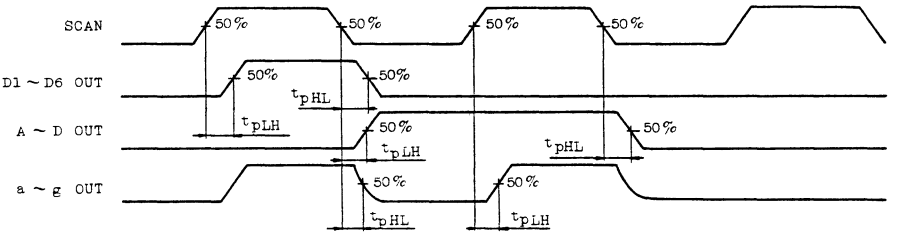
* The count operation can respond as far as f_{MAX-1}, and CARRY, EQUAL, and ZERO outputs can respond as far as f_{MAX-2}.

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

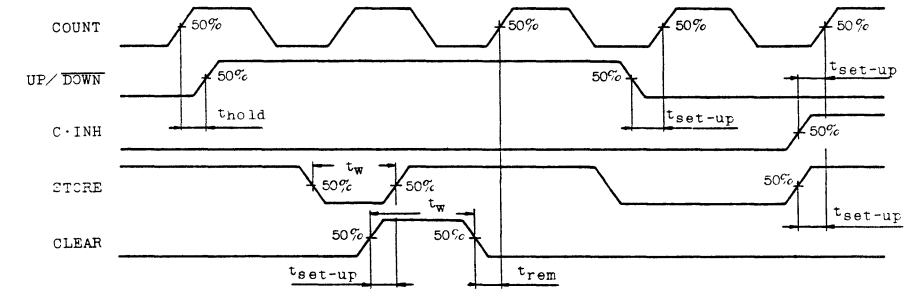
WAVEFORM 1



WAVEFORM 2

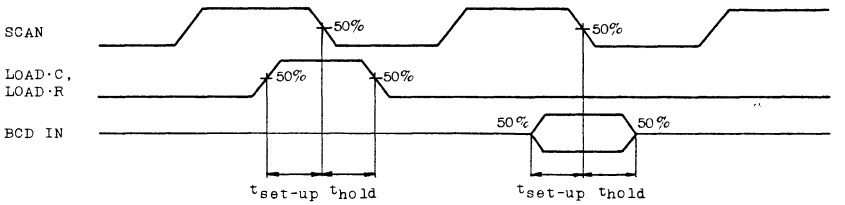


WAVEFORM 3



WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

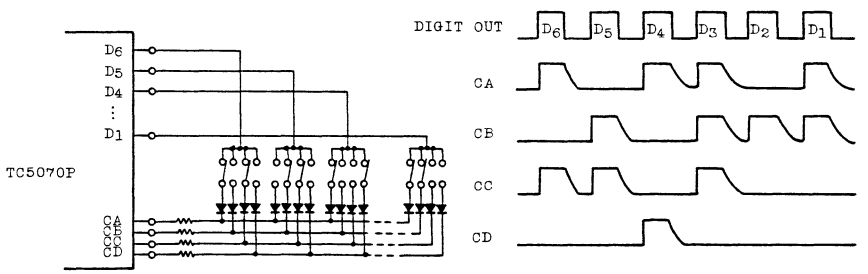
WAVEFORM 4



* Output t_r and t_f : note the output change time during 10~90% of Vout.

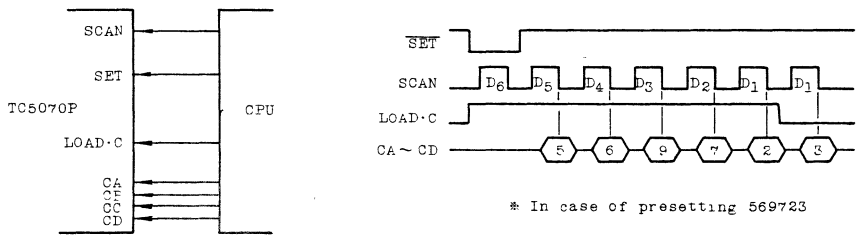
TYPICAL INPUT SELECT CIRCUIT

(1) IN CASE OF DATA PRESETTING WITH DIGITAL SWITCH, ETC.



* In case of presetting 569723

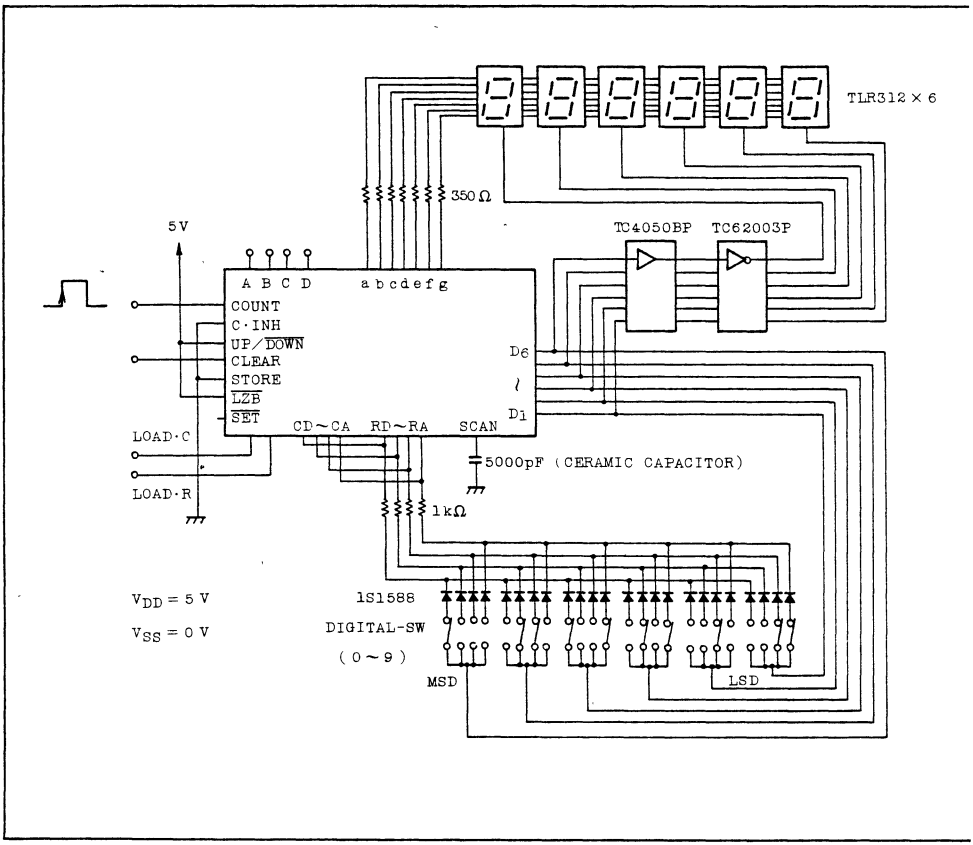
(2) IN CASE OF DATA PRESETTING WITH MICRO-COMPUTER, ETC.



* In case of presetting 569723

TC5070P, TC5071P, TC5072P

APPLICATION CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5090AP

TC5090AP PENTAPHASIC INTEGRATION 8-BIT A/D CONVERTER

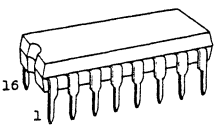
The TC5090AP is a pentaphase integration 8-bit A/D converter of high precision and low power consumption, which is mounted in a compact 16-pin standard package. The 8-bit output data can be taken out in the form of time-shared higher order 4 bits and lower order 4 bits on four 3-state data outputs.
This output system is designed specifically considering interface to 4-bit CPU.
The features of low power consumption and compact outline are applicable to battery-driven small-sized instruments.

FEATURES:

- High precision : ±1 LSB MAX.
- Low power consumption: 10mW(Typ.) @(V_{DD}=5V, f_{OSC}=1MHz)
- Single power supply : V_{DD}=5±1.5V
- High-speed conversion: 2mS(Max.) @f_{OSC}=1.5MHz
- Reference clock oscillation circuit contained (CR oscillation)
- 3-state output with output latch
- TTL/CMOS compatible digital Input/Output
- Offset automatic correction

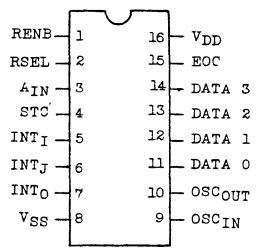
APPLICATIONS:

- Various control instruments (for temperature, humidity, pressure, etc.)
- Home electric appliances
- Electric wiring apparatuses
- Battery-driven instruments



DIP 16 (3D16A-P)

PIN ASSIGNMENT



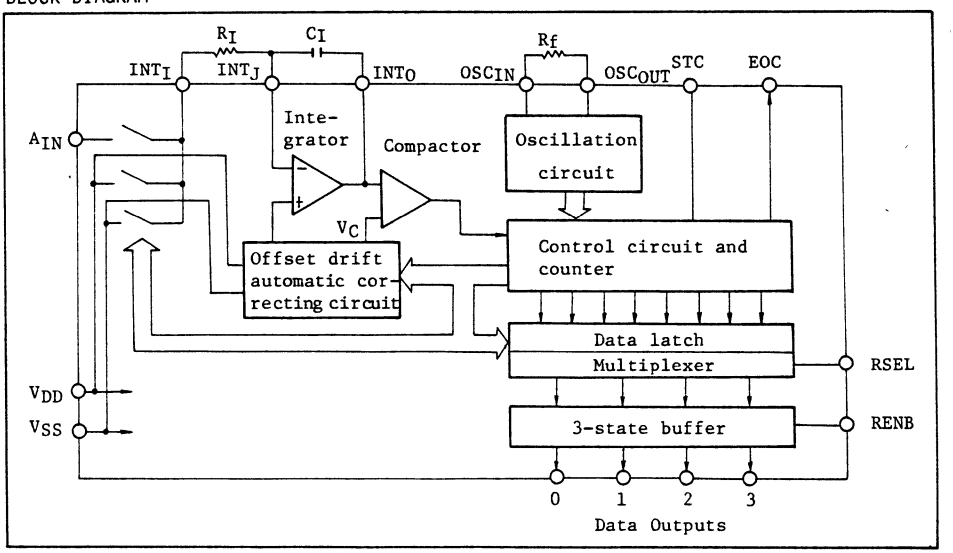
(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

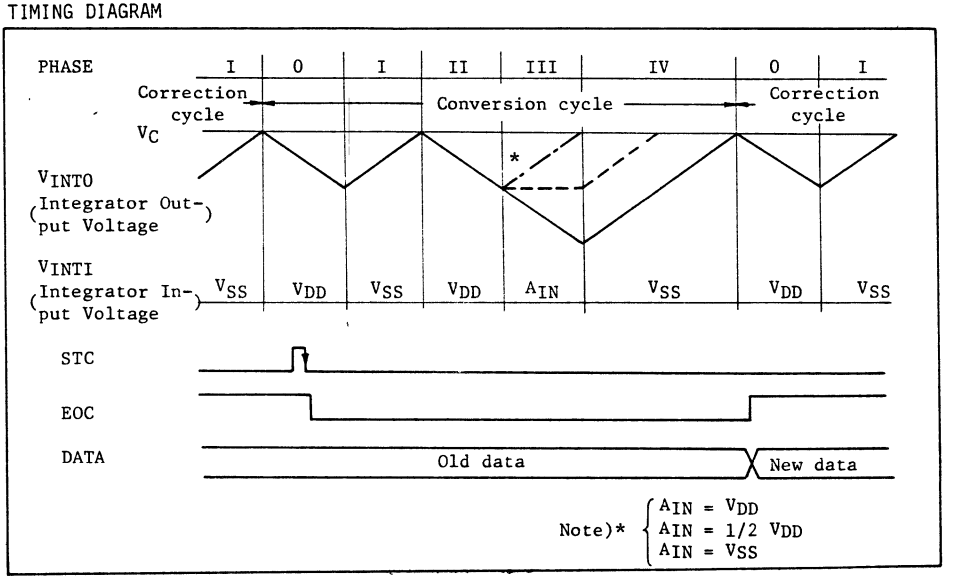
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+8	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C

TC5090AP

BLOCK DIAGRAM



TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

(1) System Description (Pentaphasic Integration)

The operation of the TC5090AP is composed of the correction cycle and the conversion cycle as shown in the timing chart. While the power is switched on, the repetition of correction cycle and conversion cycle enables the TC5090AP at make A/D conversion under the optimum conditions at all times. The operation flowchart is shown in Fig. 1.

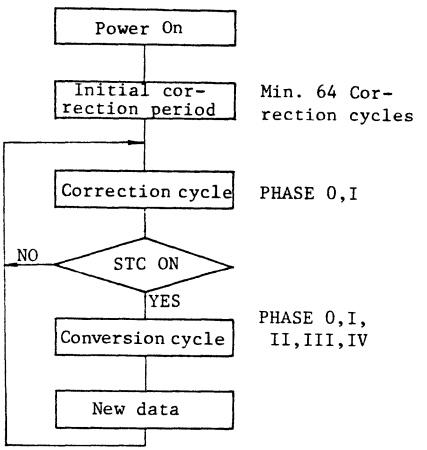


Fig. 1 Operation Flowchart

(a) Initial correction period

The internal state of this LSI is reasonably unsettled at the time when the power is switched on; therefore, the initial correction cycle is requires before stable converting operation becomes possible.

The correction cycle automatically corrects conversion error caused by offset voltage of the integrator or the like, and is composed of the period (PHASE 0) for which V_{DD} is integrated and the period (PHASE I) for which V_{SS} is integrated.

Since system correction is performed in steps at the end of this PHASE I, 64 correction cycles ($64 \times 1024 \cdot T_{OSC}$) are required as the initial correction period. (T_{OSC} denotes one clock cycle.)

(b) Conversion cycle

If the initial corection cycle period is completed, normal conversion becomes possible.
When STC input is given, (although the correction cycle in PHASE 0 or PHASE I is in operation at this time), the correction operation stops, and the conversion cycle starts.

In other words, even if STC input is given, this LSI performs the same operation as the correction cycle until PHASE I is completed; but it does not perform the correction at the time of completion of PHASE I, and shifts to PHASE II. Therefore, attention should be given to the fact that PHASE I prior to PHASE II does not act as correction cycle.
When STC input is given, the LSI integrates analog input in PHASE III through PHASE I and PHASE II, performing digital conversion in PHASE IV. When the LSI completes digital conversion in PHASE IV, the output is turned to the new data and the LSI returns to the correction cycle.

(c) Correction cycle

When the next STC input is given between completion of arbitrary conversion cycle (at the time of completion of PHASE IV) and completion of one correction cycle ($1024 \cdot T_{OSC}$), no correction is substantially made. Therefore, in case the STC input is consecutively given, another STC should be given after the lapse of one correction cycle at the earliest from completion of PHASE IV. When the STC input is given during conversion (while EOC is at "L" level), the STC cannot be accepted.

(d) Constant of integration

The R_I and C_I composing the integrator should be selected to satisfy the following equation.

$$R_I C_I = (0.9 \sim 2.5) \cdot \frac{10^3}{f_{OSC}} \quad [S]$$

Attention should be paid to the fact that, when the external R oscillation is used, f_{OSC} has ±30% variations in regard to the typ. value in Fig. 5 due to variations in sample and temperature characteristic.

In other words, if the typ. value in Fig. 5 is denoted by $f_{R \cdot TYP}$, the R_I and C_I should be selected according to the following equation.

$$R_I C_I = (1.2 \sim 1.75) \cdot \frac{10^3}{f_{R \cdot TYP}} \quad [S]$$

(2) Output Data Mode

TRUTH TABLE

RENB	ANALOG INPUT	DIGITAL OUTPUTS							
		RSEL = "L"				RSEL = "H"			
		DATA 0	DATA 1	DATA 2	DATA 3	DATA 0	DATA 1	DATA 2	DATA 3
L	Don't care	High Impedance							
H	$< \frac{1}{2}$ LSB	L	L	L	L	L	L	L	L
H	$-\frac{1}{2}$ LSB $\sim \frac{1}{2}$ LSB	L	L	L	L	L	L	L	L
H	$\frac{1}{2}$ LSB $\sim \frac{3}{2}$ LSB	H	L	L	L	L	L	L	L
H	.....		Straight Binary						
H	"FS"$-\frac{5}{2}$ LSB $\sim$ "FS"$-\frac{3}{2}$ LSB	L	H	H	H	H	H	H	H
H	"FS"$-\frac{3}{2}$ LSB $\sim$ "FS"$-\frac{1}{2}$ LSB	H	H	H	H	H	H	H	H
H	"FS"$-\frac{1}{2}$ LSB <	H	H	H	H	H	H	H	H

Note : V_{SS} = 0V 1 LSB = $V_{DD}/256$

"FS" ..... Full Scale (V_{DD})

8-bit digital data is output on four data lines after having been divided into the higher order 4 bits and the lower order 4 bits. Either the higher order bits or the lower order bits can be selected by RSEL.

(3) System Clock Oscillation Circuit

For oscillating reference clock the oscillation circuit is composed of external resistors as shown in Fig. 2.

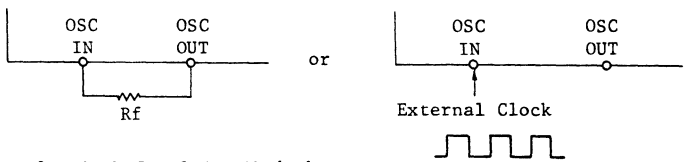


Fig.2 Clock Supplying Methods

(4) Timings for STC-EOC and EOC-DATA

o Time (t_{SE}) from the fall of STC to the fall of EOC.

$$t_{SE}=\frac{1}{2}T_{OSC} \sim \frac{3}{2}T_{OSC}$$

o Time (t_{DE}) from the out of DATA output to the rise of EOC

$$t_{DE} = \frac{1}{2}T_{OSC}$$

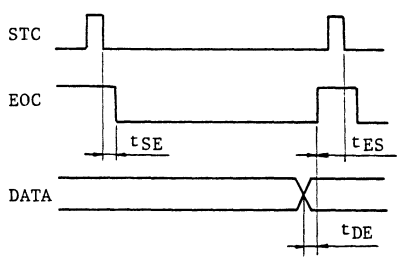


Fig.3 Timing chart of STC/EOC

o Min. time (t_{ES}) from the rise of EOC to the accpetance of another STC.

$$t_{ES} = \frac{1}{2}T_{OSC} \sim \frac{3}{2}T_{OSC}$$

(5) Timings for STC Input and RSEL/RENB Input

STC signal is taken in synchronously with the internal clock; therefore, if T_{OSC} denotes one clock cycle of OSC terminal, the pulse width of more than $(2 \cdot T_{OSC})$ is required.

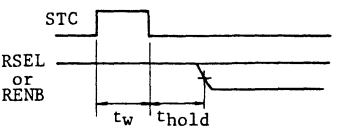


Fig.4 Timing chart of Control Input

Either RSEL input or RENB input is required to be set to "H" level at the falling time of STC by reason of internal structure.

Further, the hold time of $(T_{OSC} + 50ns)$ or more after the falling time of STC at least for "H" level time of RSEL or REMB is required.

NOTE : $t_w > 2 \cdot T_{OSC}$, $t_{hold} > T_{OSC} + 50ns$

TC5090AP

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

ITEM	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3.5	5	6.5	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Integral Resistor	R_I		0.4	-	2	MΩ
Integral Capacitor	C_I		Note			
Oscillatory Resistance	R_f	V_{DD} = 5V	10	-	-	kΩ

Note: Refer to Fuction Description (1) for determing the values of R_I and C_I, respectively.

ELECTRICAL CHARACTERISTICS (V_{SS} = 0V)

ITEM	SYMBOL	TEST CONDITIONS	V_{DD} [V]	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Input High Voltage	V_{OH}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS},V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
Output Low Voltage	V_{OL}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS},V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	V
Output High Current	I_{OH}	V_{OH}=4.0V * V_{IN}=V_{SS},V_{DD}	5	-1.2	-	-1.0	-2.0	-	-0.7	-	mA
Output Low Current	I_{OL}	V_{OL}=0.4V * V_{IN}=V_{SS},V_{DD}	5	2.4	-	2.0	4.0	-	1.6	-	mA
Input High Voltage	V_{IH}	*	5	2.4	-	2.4	-	-	2.4	-	V
Input Low Voltage	V_{IL}	*	5	-	0.8	-	-	0.8	-	0.8	V
Output Disable Current	I_{DH} I_{DL}	V_{OH}=6.5V * V_{OL}=0V	6.5	-	±0.5	-	$\pm 10^{-4}$	±0.5	-	±5	μA
Input Current	I_{IH} I_{IL}	V_{IH}=6.5V * V_{IL}=0V	6.5	-	±0.3	-	$\pm 10^{-5}$	±0.3	-	±1	μA
Analog Switch Off-Leak Current	I_{OFF}	I_{IH}=6.5V V_{IL}=0V	6.5	-	±0.3	-	$\pm 10^{-5}$	±0.3	-	±1	μA
Operating Consumption Current	I_{DD} (opr)	f_{OSC} = 1 MHz	5	-	-	-	2.0	3	-	-	mA

* Applicable to digital input/output. Not applicable to analog input/output and OSC_{IN}/OSC_{OUT}.

SWITCHING CHARACTERISTICS (V_{DD} = 5V, V_{SS} = 0V, Ta = 25°C, C_L = 50 pF)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time	tr		-	50	100	ns
Output Fall Time	tr		-	40	100	
(Low-High) Propagation Delay Time	t_{pLH}	RSEL("L"→"H")-DATA OUT	-	180	400	
(High-Low) Propagation Delay Time	t_{pHL}		-	150	400	
(Low-High) Propagation Delay Time	t_{pLH}	RSEL("H"→"L")-DATA OUT	-	380	700	
(High-Low) Propagation Delay Time	t_{pHL}		-	300	700	
Output Enable Time	t_{ZL} t_{ZH}	RENB-DATA OUT	-	80	250	
Output Disable Time	t_{LZ} t_{HZ}		-	280	500	
Max. Clock Frequency	$f_{MAX\phi}$	OSC Input	1.5	3.0	-	MHz
Min. Clock Frequency	$f_{MIN\phi}$	OSC Input	-	-	100	kHz
Input Capacity	C_{IN}	Digital Inputs	-	4	-	pF
Analog Input Capacity	C_{IN}		-	7	-	pF
3-State Output Capacity	C_{OUT}		-	8	-	pF

SYSTEM CHARACTERISTICS (Ta = -40 ∿ 85°C)

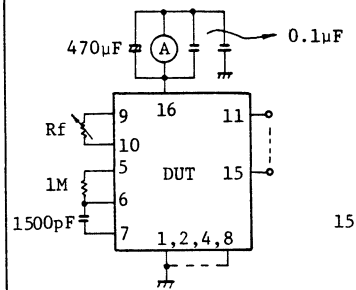
ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Zero Point Error	E_{ZP}	V_{DD}=5V, V_{SS}=0V	-	$\pm\frac{1}{4}$	$\pm\frac{1}{2}$	LSB
Full Scale Error	E_{FS}		-	$\pm\frac{1}{4}$	±1	
Nonlinearity			-	$\pm\frac{1}{4}$	±1	
STC Min. Pulse Width	t_w	*	-	-	$\frac{2}{f_{OSC}}$	s
Conversion Time	$t_{conv.}$	A_{IN} = 0 ∿ FS *	$\frac{10^3}{f_{OSC}}$	-	$\frac{3.1\times10^3}{f_{OSC}}$	s

* f_{OSC} : OSC terminal clock frequency [Hz], FS : Full Scale voltage, V_{DD} level

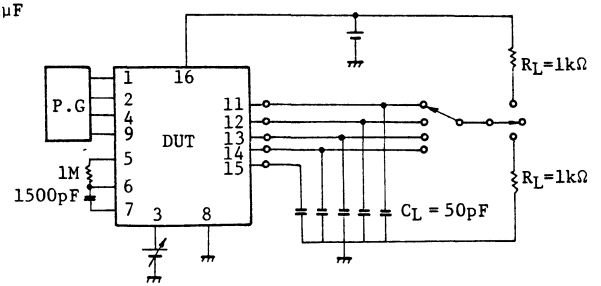
TC5090AP

TEST CIRCUIT

$I_{DD(opr.)}$ Test Circuit



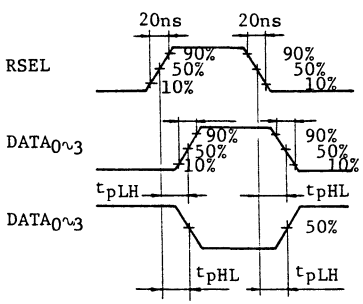
Switching Time Test Circuit



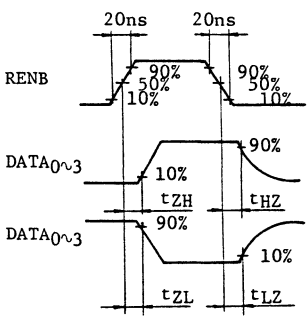
Rf is adjusted as f_{OSC} = 1MHz.

SWITCHING CHARACTERISTICS TEST WAVEFORMS

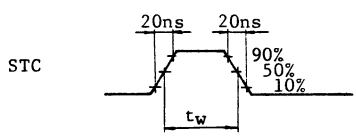
1. tpLH, tpHL (RSEL-DATA)



2. t_{ZL}, t_{ZH}, t_{LZ}, t_{ZL}



3. t_w (STC)



STANDARD CHARACTERISTICS CHARTS

Fig. 1 V_{DD} - $I_{DD(opr)}$

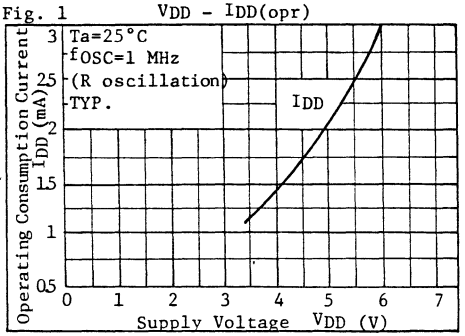


Fig. 2 $I_{DD(opr)}$ - f_{OSC}

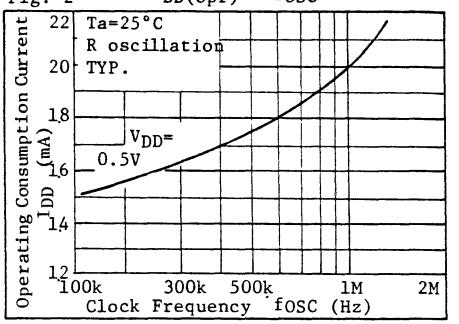


Fig. 3 P-channel Output Buffer Drain Current Characteristics

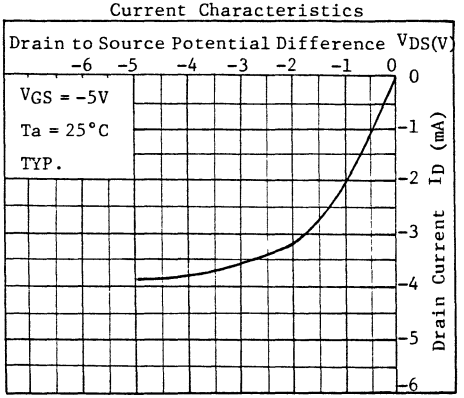


Fig. 4 N-channel Output Buffer Drain Current Characteristics

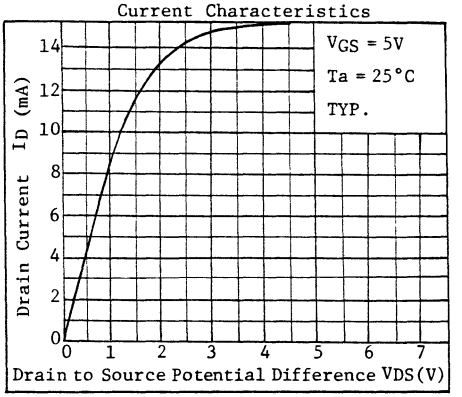


Fig.5 R_f - f_{OSC}

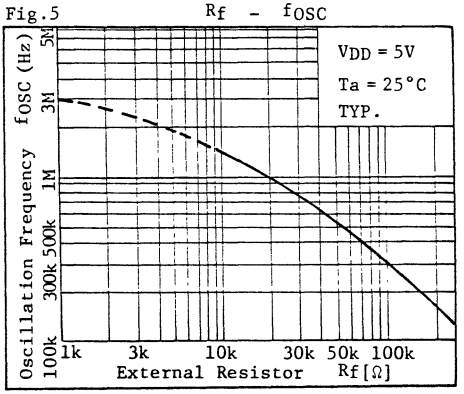
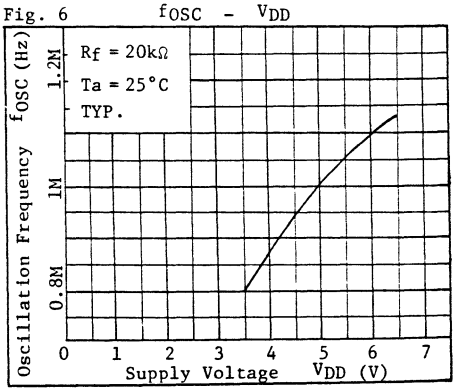


Fig. 6 f_{OSC} - V_{DD}



TC5090AP

Fig. 7 t_{pd} - V_{DD} (PENB-DATA)

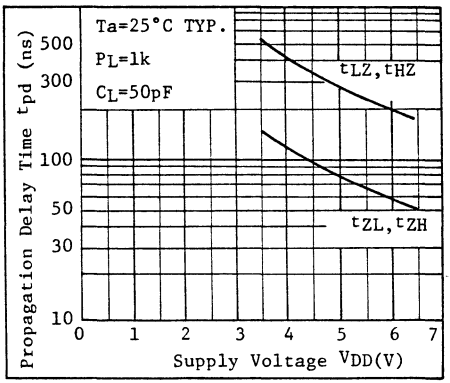


Fig. 8 t_{pd} - V_{DD} (RSEL (L→H)-DATA)

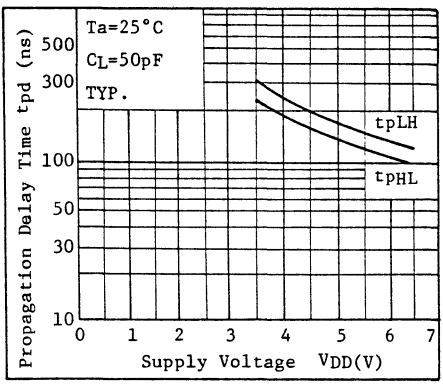


Fig. 9 t_{pd} - V_{DD}(RSEL(H → L)-DATA)

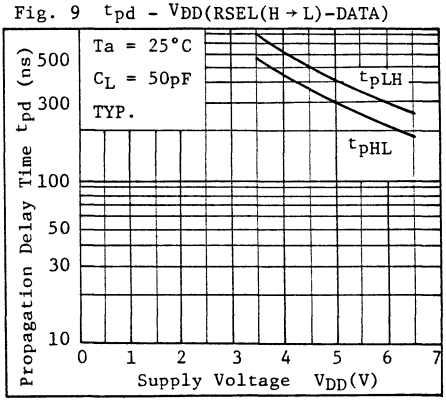
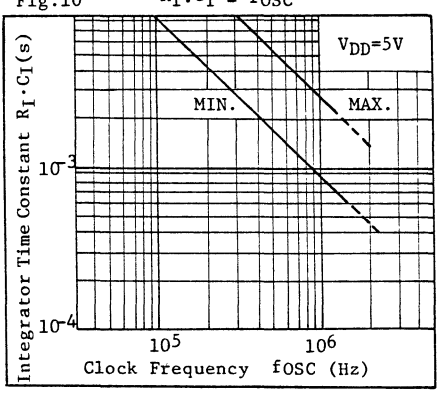


Fig.10 $R_I \cdot C_I$ - f_{OSC}



(Note) The characteristics at Fig. 10 have been prepared for reference at the time of determination of an integrator time constant, according to the equation of

$$(R_I \cdot C_I = (0.9 \sim 2.5) \frac{10^3}{f_{osc}} [\text{Sec}])$$

for determing $R_I \cdot C_I$.

In case of the determination of R_I and C_I, the product, or the value, of R_I and C_I is required to be within the range of MIN. to MAX. as shown in Fig. 10 after due consideration of dispersion.

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5091AP

TC5091AP PENTAPHASIC INTEGRATION 8-BIT A/D CONVERTER

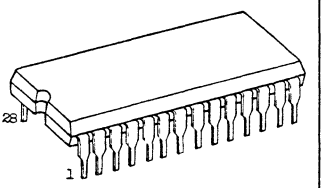
The TC5091AP is a pentaphasic integration 8-bit A/D converter of high precision and low power consumption. The 8-bit output data can be taken out in the form of time-shared higher order 4 bits and lower order 4 bits on four 3-state data output. Either the higher order bits or the lower order bits can be selected by RSEL input. This output system is designed specifically considering interface to 4-bit CPU.
Further, since this converter has an analog multiplexer capable of selecting the input data up to six channels, an over-range flag, and a serial clock output function, it is used for a variety of applications.

FEATURES:

- High precision : ±LSB(Max.)
- Low power consumption: 10mW(Typ.) @(V_{DD}=5V, f_{OSC}=1MHz)
- Single power supply : V_{DD}=5±1.5V
- High-speed conversion: 2ms(Max.) @f_{OSC}=1.5MHz
- 6-channel analog multiplexer contained
- Reference clock oscillation cirucit contained (CR oscillation)
- 3-state output with output latch
- TTL/CMOS compatible digital Input/Output
- Offset automatic correction

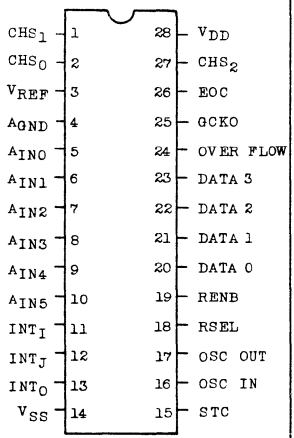
APPLICATIONS:

- Various control instruments (for temperature, humidity, pressure, etc.)
- Home electric appliances
- Electrical wiring apparatuses
- Battery-driven instruments



DIP 28 (6D28A-P)

PIN ASSIGNMENT



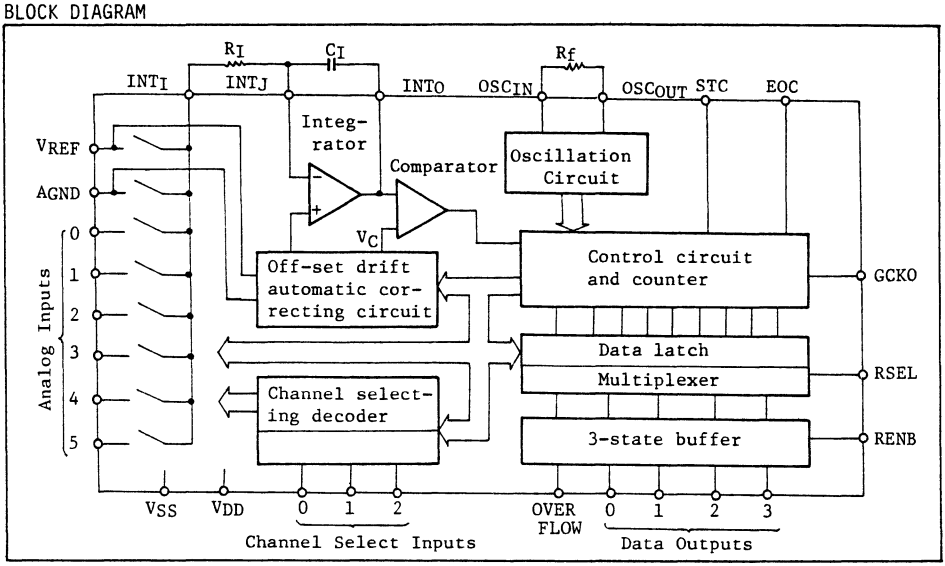
(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

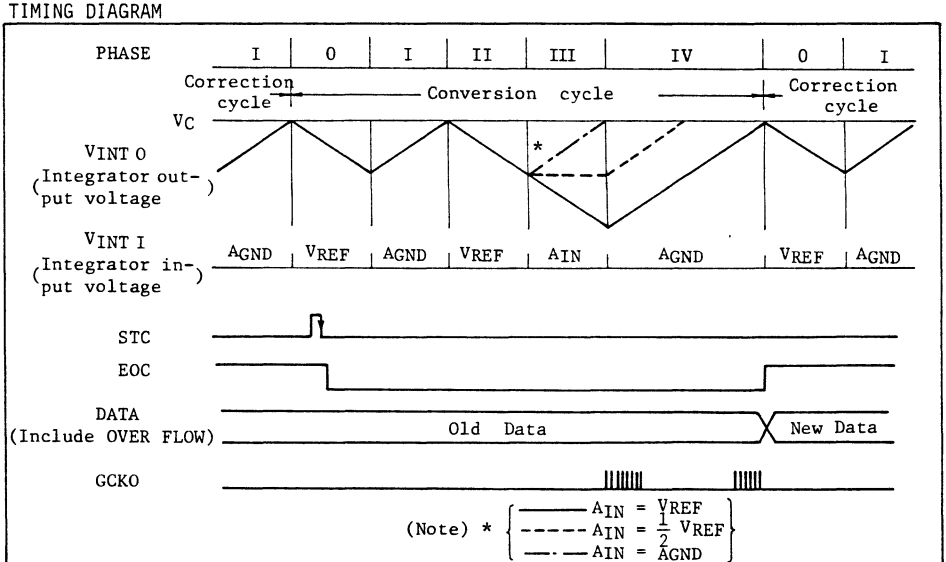
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+8	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Reference Supply Voltage	V_{REF}	V_{AGND} ~ V_{DD}+0.5	V
Analog Ground Voltage	V_{AGND}	V_{SS}-0.5 ~ V_{REF}	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C

TC5091AP

BLOCK DIAGRAM



TIMING DIAGRAM



FUNCTION OF EACH PIN

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>NAME & FUNCTION</th><th>PIN No.</th><th>SYMBOL</th><th>NAME & FUNCTION</th></tr>
<tr><td>1</td><td>CHS 1</td><td rowspan="2">(Channel Select Inputs)
Address inputs to select analog inputs, which consist of three terminals of CHS0∿2.
These select inputs are taken into the internal latch by the falling edge of STC inputs.
Test mode should not be used.
TRUTH TABLE OF MULTIPLEXER
<table><tr><th>CHS2</th><th>CHS1</th><th>CHS0</th><th>ON channel</th></tr><tr><td>L</td><td>L</td><td>L</td><td>VREF*</td></tr><tr><td>L</td><td>L</td><td>H</td><td>AGND*</td></tr><tr><td>L</td><td>H</td><td>L</td><td>AIN0</td></tr><tr><td>L</td><td>H</td><td>H</td><td>AIN1</td></tr><tr><td>H</td><td>L</td><td>L</td><td>AIN2</td></tr><tr><td>H</td><td>L</td><td>H</td><td>AIN3</td></tr><tr><td>H</td><td>H</td><td>L</td><td>AIN4</td></tr><tr><td>H</td><td>H</td><td>H</td><td>AIN5</td></tr></table>* Test Conditions</td><td>16</td><td>OSC IN</td><td rowspan="2">I/O for reference clocl oscillation. Clock oscillation can be made by means of external registance. Clock can be supplied from outside through input of OSC IN.</td></tr>
<tr><td>2</td><td>CHS 0</td><td>17</td><td>OSC OUT</td></tr>
<tr><td>3</td><td>VREF</td><td>(Reference Voltage)
Reference voltage supplying terminal, which performs as full-scale voltage of AIN.</td><td>18</td><td>RSEL</td><td>(Read Select)
Input to select the higher order 4 bits or the lower order 4 bits to 4-bit data output.
"H": Output of the higher order 4 bits.
"L": Output of the lower order 4 bits.</td></tr>
<tr><td>4</td><td>AGND</td><td>(Analog Ground)
Electrical potential to determine "zero point" of AIN.</td><td>19</td><td>RENB</td><td>(Read Enable)
Data read signal.
"H": The data 0∿3 and overflow can be output.
"L": The output above is at high impedance.</td></tr>
<tr><td>5</td><td>AIN 0</td><td rowspan="6">(Analog Ground)
Analog input terminals, by which AIN selected by CHS inputs are integrated. Input voltage range is AGND∿VREF.</td><td>20</td><td>DATA 0</td><td rowspan="4">(3-state Parallel Data Outputs)
Conversion data output.
The data 0 is LSB, and the data 3 is MSB.</td></tr>
<tr><td>6</td><td>AIN 1</td><td>21</td><td>DATA 1</td></tr>
<tr><td>7</td><td>AIN 2</td><td>22</td><td>DATA 2</td></tr>
<tr><td>8</td><td>AIN 3</td><td>23</td><td>DATA 3</td></tr>
<tr><td>9</td><td>AIN 4</td><td rowspan="2">24</td><td rowspan="2">OVER-FLOW</td><td rowspan="2">In case of overrange or underranbe, "H" level is output and the output is 3-state output.</td></tr>
<tr><td>10</td><td>AIN 5</td></tr>
<tr><td>11</td><td>INT I</td><td rowspan="3">(Integrator Input, Integrator Junction, Integrator Output)
Integrator consists of external resistor RI and external capacitor CI.</td><td rowspan="2">25</td><td rowspan="2">GCKO</td><td rowspan="2">(Gated Clock Output)
Pulses of number equivalent to the conversion data are output during conversion
(356 pulses at full scale)</td></tr>
<tr><td>12</td><td>INT J</td></tr>
<tr><td>13</td><td>INT O</td><td rowspan="2">26</td><td rowspan="2">EOC</td><td rowspan="2">(End of Conversion)
Conversion endig signal. EOC goes to "L" level at the fall of STC, and returns to "H" level at the end of conversion.</td></tr>
<tr><td>14</td><td>VSS</td><td>(Digital Ground)
Normally 0V</td><td>27</td><td>CHS 2</td><td>(Channel Select Input)
Refer to Pins 1 and 2.</td></tr>
<tr><td>15</td><td>STC</td><td>(Start Conversion)
Conversion starting signal. Conversion starts at the falling edge.</td><td>28</td><td>VDD</td><td>(Power Supply)
5V ± 1.5V</td></tr>
</table>

TC5091AP

FUNCTIONAL DESCRIPTION

(1) System Description (Pentaphasic Integration)

The operation of the TC5091AP is composed of the correction cycle and the conversion cycle as shown in the timing chart. While the power is switched on, the repetition of correction cycle and conversion cycle enables the TC5091AP at make A/D conversion under the optimum conditions at all times. The operation flowcahrt is shown in Fig. 1.

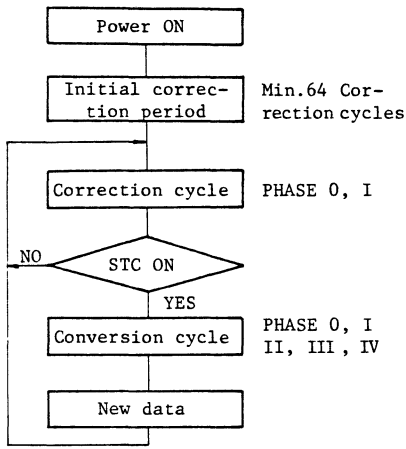


Fig. 1 Operation Flowchart

(a) Initial correction period

The internal state of this LSI is reasonably unsettled at the time when the power is switched on; therefore, the initial correction cycle is requires before stable coverting operation becomes possible.

The correction cycle automatically corrects conversion error caused by offset voltage of the integrator or the like, and is composed of the period (PHASE 0) for which V_{REF} is integrated and the period (PHASE I) for which AGND is integrated.

Since system correction is performed in steps at the end of this PHASE I, 64 correction cycles ($64 \times 1024 \cdot T_{OSC}$) are required as the initial correction period. (T_{OSC} denotes one clock cycle.)

(b) Conversion cycle

If the initial correction cycle period is completed, normal conversion becomes possible.

When STC input is given, (although the correction cycle in PHASE 0 or PHASE I is in operation at this time), the correction operation stops, and the conversion cycle starts.

In other words, even if STC input is given, this LSI performs the same operation as the correction cycle until PHASE I is completed; but it does not perform the correction at the time of completion of PHASE I, and shifts to PHASE II. Therefore, attention should be given to the fact that PHASE I prior to PHASE II does not act as correction cycle.

When STC input is given, the LSI integrates analog input in PHASE III through PHASE I and PHASE II, performing digital conversion in PHASE IV. When the LSI completes digital conversion in PHASE IV, the output is turned to the new data and the LSI returns to the correction cycle.

(c) Correction cycle

When the next STC input is given between completion of arbitrary conversion cycle (at the time of completion of PHASE IV) and completion of one correction cycle ($1024 \cdot T_{OSC}$), no correction is substantially made. Therefore, in case the STC input is consecutively given, another STC should be given after the lapse of one correction cycle at the earliest from completion of PHASE IV. When the STC input is given during conversion (While EOC is at "L" level), the STC cannot be accepted.

(d) Constant of integration

The R_I and C_I composing the integrator should be selected to satisfy the following equation.

$$R_I C_I = (0.9 \sim 2.5) \cdot \frac{V_{REF}}{V_{DD}} \cdot \frac{10^3}{f_{OSC}} \text{ [S]}$$

Attention should be paid to the fact that, when the external R oscillation is used, f_{OSC} has ±30% variations in regard to the typ. value in Fig. 5 due to variations in sample and temperature characteristic.

In other words, if the typ. value in Fig. 5 is denoted by $f_{R \cdot TYP}$, the R_I and C_I should be selected according to the following equation.

$$R_I C_I = (1.2 \sim 1.75) \cdot \frac{V_{REF}}{V_{DD}} \cdot \frac{10^3}{f_{R \cdot TYP}} \text{ [S]}$$

(2) Output Data Mode

TRUTH TABLE

RENB	ANALOG INPUT	DIGITAL OUTPUTS								OVER FLOW
		RSEL = "L"				RSEL = "H"				
		DATA 0	DATA 1	DATA 2	DATA 3	DATA 0	DATA 1	DATA 2	DATA 3	
L	Don't Care	High Impedance								
H	$\sim\frac{1}{2}$LSB	L	L	L	L	L	L	L	H	H
H	$\frac{1}{2}$LSB $\sim\frac{1}{2}$LSB	L	L	L	L	L	L	L	L	L
H	$\frac{1}{2}$LSB $\sim\frac{3}{2}$LSB	H	L	L	L	L	L	L	L	L
H	.....	Straight Binary								
H	"FS"$-\frac{5}{2}$LSB $\sim$ "FS"$-\frac{3}{2}$LSB	L	H	H	H	H	H	H	H	L
H	"FS"$-\frac{3}{2}$LSB $\sim$ "FS"$-\frac{1}{2}$LSB	H	H	H	H	H	H	H	H	L
H	"FS"$-\frac{1}{2}$LSB $\sim$	H	H	H	H	H	H	H	H	H

Note : • AGND = 0V • 1LSB = "FS"/256

• "FS" ..... Full Scale (=V_{REF})

8-bit digital data is output on four data lines after having been divided into the higher order 4 bits and the lower order 4 bits. Either the higher order bits or the lower order bits can be selected by RSEL.

(3) System Clock Oscillation Circuit

For oscillating reference clock the oscillation circuit is composed of external resistors as shown in Fig. 2.

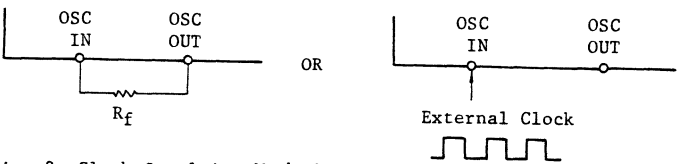


Fig. 2 Clock Supplying Methods

(4) Timings for STC-EOC and EOC-DATA

o Time (t_{SE}) from the fall of STC to the fall of EOC.

$$t_{SE} = \frac{1}{2} T_{OSC} \sim \frac{3}{2} T_{OSC}$$

o Time (t_{DE}) from the out of DATA output to the rise of EOC

$$t_{DE} = \frac{1}{2} T_{OSC}$$

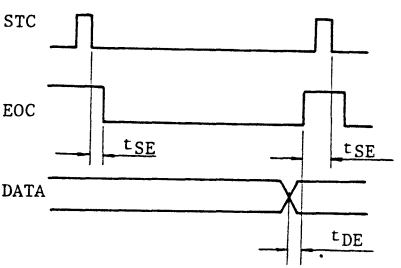


Fig. 3 Timing Chart of STC, EOC

O Min. time (t_{ES}) from the rise of EOC to the acceptance of another STC.

$$t_{ES} = \frac{1}{2} T_{OSC} \sim \frac{3}{2} T_{OSC}$$

(5) GCKO Output (Gated Clock Output)

During the conversion (PHASE IV), the pulses of number equivalent to the values of digital data can be obtained on GCKO output.
The output pluse has the frequency corresponding to four times of refernece clock as shown in Fig. 4, and is synchronized with the rising edge of OSC OUT.

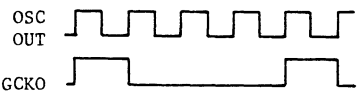


Fig. 4 Timing Chart of GCKO Output

(6) Timing for STC Input and CHS Input

STC signal is taken in synchronously with the internal clock.
Therefore, if T_{OSC} denotes one clock cycle of OSC terminal, the pulse width of more than ($2 \cdot T_{OSC}$) is required.

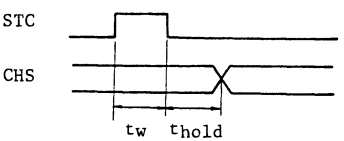


Fig.5 Timing Chart of Control Inpu

Since the data of $CHS_{0 \sim 2}$ are also latched in synchronously with the internal clock, the CHS signal at least requires the hold time of (T_{OSC} + 50ns) or more after the fall of STC.

NOTE : $t_w > 2 \cdot T_{OSC}$, $t_{hold} > T_{OSC} + 50ns$

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

ITEM	SYMBOL		MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD}		3.5	5	6.5	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Reference Voltage	V_{REF}		3	-	V_{DD}	V
Analog Ground Voltage	V_{AGND}		0	0	1	V
Integral Resistor	R_I		0.4	-	2	MΩ
Integral Capacitor	C_I	(Note)	-	-	-	-
Oscillatory Resistance	Rf	V_{DD} = 5V	10	-	-	MΩ

Note: Refer to the operating consideration (1) for determing the values of R_I and C_I respectively.
The ripples of V_{DD} and V_{REF} should be held down to less than 1/256 of the respective absolute values in view of precision.

ELECTRICAL CHARACTERISTICS (V_{SS} = 0V)

ITEM	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Output High Voltage	V_{OH}	$\|I_{OUT}\|$<1 μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
Output Low Voltage	V_{OL}	$\|I_{OUT}\|$<1 μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.0V * $V_{IN}=V_{SS},V_{DD}$	5	-1.2	-	-1.0	-2.0	-	-0.7	-	mA
Output Low Current	I_{OL}	V_{OL}=0.4V * $V_{IN}=V_{SS},V_{DD}$	5	2.4	-	2.0	4.0	-	1.6	-	
Input High Voltage	V_{IH}	*	5	2.4	-	2.4	-	-	2.4	-	V
Input Low Voltage	V_{IL}	*	5	-	0.8	-	-	0.8	-	0.8	
Output Disable Current	I_{DH} I_{DL}	V_{OH}=6.5V * V_{OL}=0V	6.5	-	±0.5	-	$\pm10^{-4}$	±0.5	-	±5	μA
Input Current	I_{IH} I_{IL}	V_{IH}=6.5V * V_{IL}=0V	6.5	-	±0.3	-	$\pm10^{-5}$	±0.3	-	±1	
Analog Switch Input Leak Current	I_{OFF}	V_{IH}=6.5V V_{IL}=0V	6.5	-	±0.3	-	$\pm10^{-5}$	±0.3	-	±1	
Operating Consumption Current	I_{DD} (opr.)	f_{OSC}=1 MHz	5	-	-	-	1.8	3	-	-	mA
Reference Supply Consumption Current	I_{REF}	V_{REF} = 5V AGND = 0V	5	-	-	-	0.3	0.6	-	-	

* Applicable to digital input/output. Not applicable to analog input/output and OSC_{IN}/OSC_{OUT}.

TC5091AP

SWITCHING CHARACTERISTICS (V_{DD} = 5V, V_{SS} = 0V, Ta = 25°C, C_L = 50pF)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time	tr		-	50	100	ns
Output Fall Time	tf		-	40	100	
(Low-High) Propagation Delay Time	tPLH	OSC_{OUT}-GCKO	-	200	400	
(High-Low) Propagation Delay Time	tPHL		-	150	400	
(Low-High) Propagation Delay Time	tPLH	RSEL("L"→"H")-DATA OUT	-	180	400	
(High-Low) Propagation Delay Time	tPHL			150	400	
(Low-High) Propagation Delay Time	tPLH	RSEL("H"→"L")-DATA OUT	-	380	700	
(High-Low) Propagation Delay Time	tPHL		-	300	700	
Output Enable Time	tZL tZH		-	80	250	
Output Disable Time	tLZ tHZ		-	280	500	
Max. Clock Frequency	fMAZØ	OSC Input	1.5	3.0	-	MHz
Min. Clock Frequency	fMINØ	OSC Input	-	-	100	kHz
Input Capacity	C_{IN}	Digital Input	-	4	-	pF
Analog Input Capacity	C_{IN}	$A_0 \sim A_5$	-	7	-	pF
3-State Output Capacity	COUT		-	8	-	pF

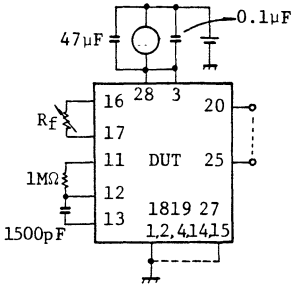
SYSTEM CHARACTERISITCS (Ta = -40 ∿ 85°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Zero Point Error	E_{ZP}	$V_{REF} = V_{DD} = 5V$, $V_{AGND} = 0V$	-	$\pm\frac{1}{4}$	$\pm\frac{1}{2}$	LSB
Full Scale Error	E_{FS}		-	$\pm\frac{1}{4}$	± 1	
Nonlinearity			-	$\pm\frac{1}{4}$	± 1	
STC Min. Pulse Width	t_w		-	-	$\frac{2}{f_{OSC}}$	s
CHS Min. Hold Time	thold	STC = $CHS_{0\sim2}$	-	-	$\frac{10}{f_{OSC}}+50$	ns
Conversion Time	tconv.	A_{IN} = 0 ∿ FS	$\frac{10^3}{f_{OSC}}$	-	$\frac{3.1\times10^3}{f_{OSC}}$	s

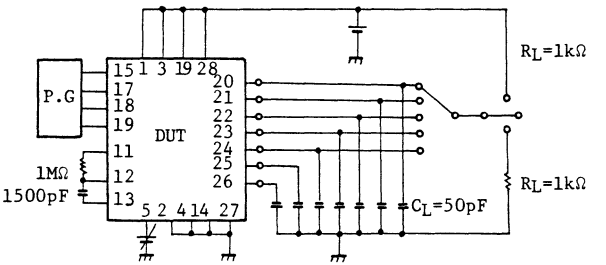
* f_{OSC} : OSC terminal clock frequency [Hz], FS : Full Scale voltage, V_{DD} level

• TEST CIRCUIT

IDD(opr.) Test Circuit



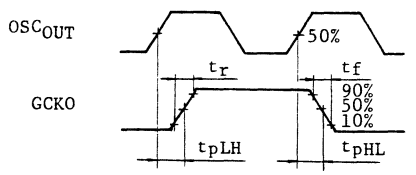
Switching Time Test Circuit



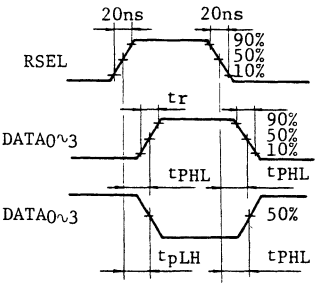
R_f is adjusted as f_{OSC} = 1 MHz.

SWITCHING CHARACTERISTICS TEST WAVEFORMS

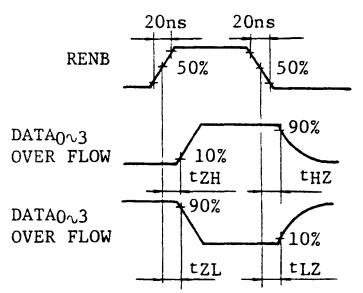
1. tpLH, tpHL (OSC OUT - GCKO)



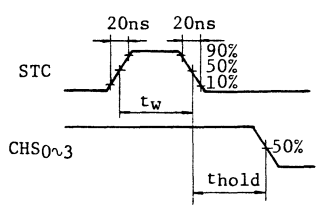
2. tpLH, tpHL (RSEL - DATA)



3. tZL, tZH, tLZ, tZL



4. tw (STC), thold (CHS)



TC5091AP

STANDARD CHARACTERISTICS CHARTS

Fig. 1 V_{DD} - I_{DD}(opr)

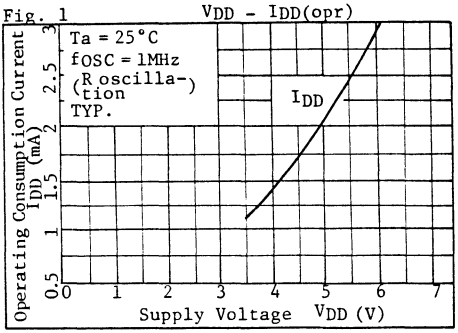


Fig. 2 I_{DD}(opr) - f_{OSC}

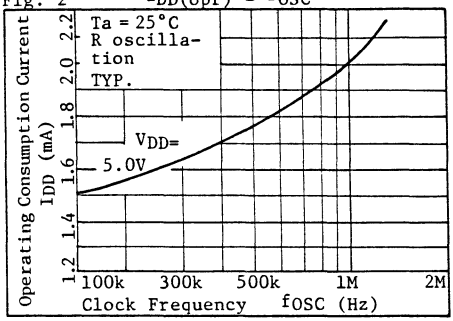


Fig. 3 P-channel Output Buffer Drain Current Characteristics

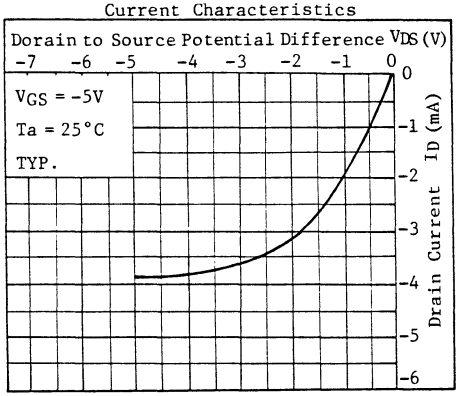


Fig. 4 N-channel Output Buffer Drain Current Characteristics

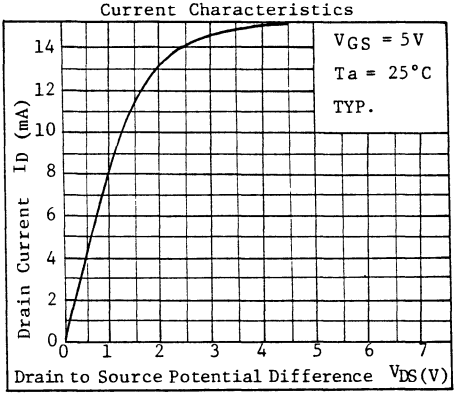


Fig. 5 R_f - f_{OSC}

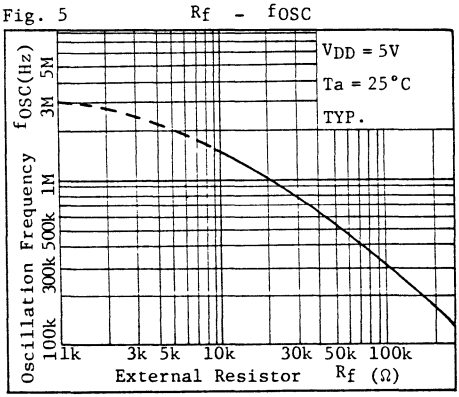


Fig. 6 f_{OSC} - V_{DD}

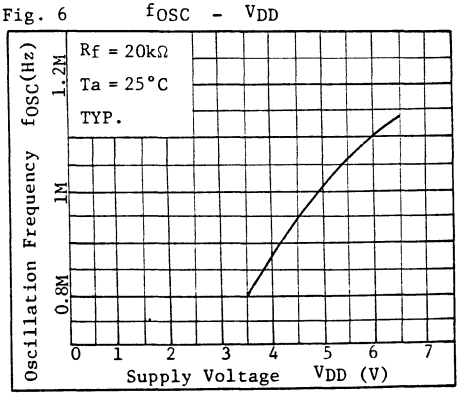


Fig. 7 t_{pd} - V_{DD} (RENB-DATA)

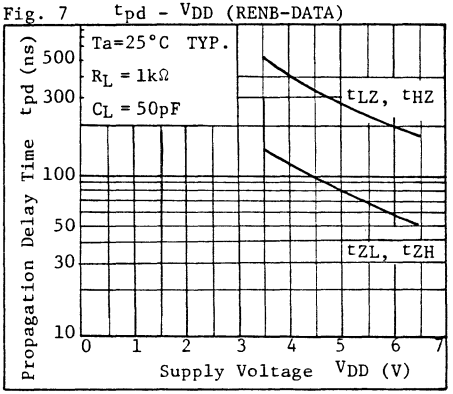


Fig.8 t_{pd} - V_{DD} (RSEL (L→H)-DATA)

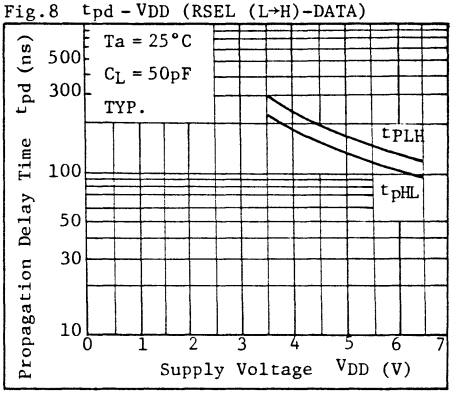


Fig. 9 t_{pd} - V_{DD} (RSEL (H→L)-DATA)

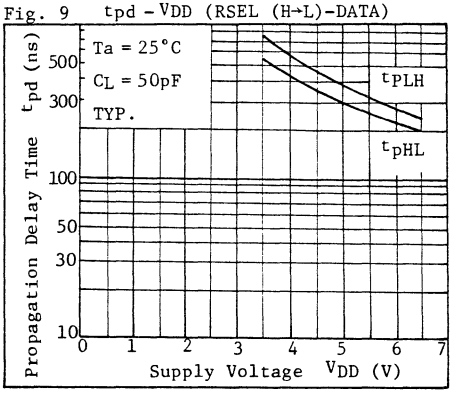


Fig.10 t_{pd} - V_{DD} (OSC_{OUT} - GCKO)

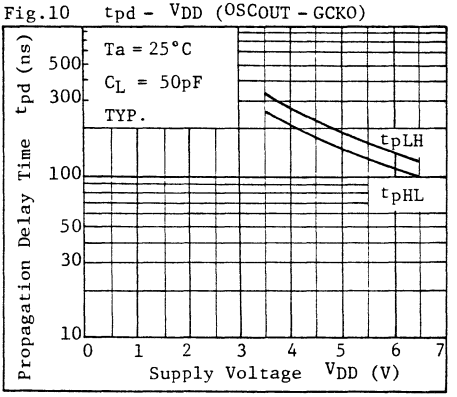
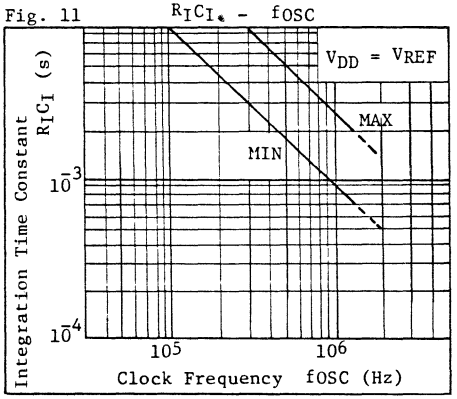


Fig. 11 $R_I C_I$ - f_{OSC}



(Note)
The characterisitcs at left have been prepared for reference at the time of determination of an integrator time constant according to the equation of

$$(R_I C_I = (0.9 \sim 2.5) \cdot \frac{V_{REF}}{V_{DD}} \cdot \frac{10^3}{f_{OSC}} (s))$$

for determing $R_I \cdot C_I$.

In case of the determination of R_I and C_I, the product, or the value, of R_I and C_I is required to be within the range of MIN. to MAX. as shown in left figure after due consideration of dispersion.

TC5092AP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5092AP C²MOS 13-BIT A/D CONVERTER

GENERAL DESCRIPTION

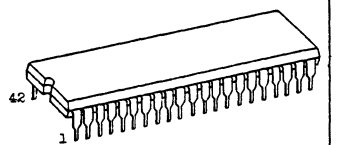
The TC5092AP is an integration 13-bit A/D converter of high precision and low power consumption.
The 13-bit, 3-state data output is capable of independent enable in 4 bits so as to be connected directly to 4-bit/8-bit/12-bit data bus. (LSB is common to lower order 4 bits.)
Further, since this converter has an 8-channel analog multiplexer, and a serial clock output function, it is most suitable as data collection unit of various industrial control instruments.

FEATURES:

- High precision.....±1 LSB(Typ.)
- Low power consumption.....10mW(Typ.)
- Single power supply.....V_{DD}=5V±0.5V
- High-speed conversion.....f_{CP} Max.=5MHz
- 8-channel analog multiplexer contained
- TLL/CMOS compatible digital Input/Output
- Capable of direct connection to 4-/8-/12-bit bus

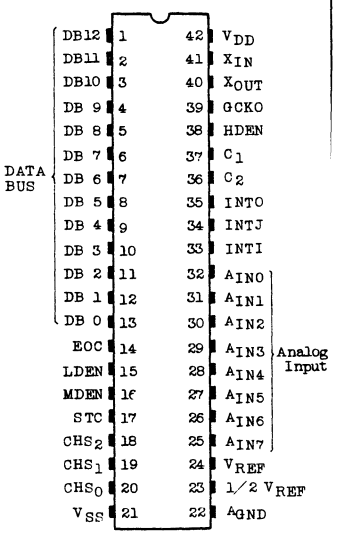
APPLICATIONS:

- Various industrial control instruments
- Data collection modules



DIP 42 (6D42A-P)

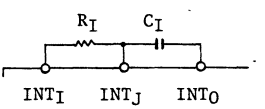
PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+7	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{DD}+0.5	V
Reference Supply Voltage	V_{REF}	V_{AGND}~V_{DD}+0.5	V
Analog Ground Voltage	V_{AGND}	V_{SS}-0.5~V_{REF}	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	-40~85	°C
Storage Temperature Range	T_{stg}	-65~150	°C

FUNCTION OF EACH PIN

PIN NO.	Symbol	NAME & FUNCTION
1	DB12	3-State Parallel Data Outputs DB12 : MSB DB 0 : LSB
2	DB11	
3	DB10	
4	DB 9	
5	DB 8	
6	DB 7	
7	DB 6	
8	DB 5	
9	DB 4	
10	DB 3	
11	DB 2	
12	DB 1	
13	DB 0	
14	EOC	End of Conversion EOC goes to "L" level at the fall of STC signal, and returns to "H" level at the end of conversion.
15	LDEN	Low Data Enable $DB_0 \sim DB_4$ are read by "H" level input.
16	MDEN	Medium Data Enable $DB_5 \sim DB_8$ are read by "H" level input.
17	STC	Start Conversion Conversion starts at the fall time, if pulse input at "H" level is provided. "L" level should be kept during conversion.
18	CHS_2	Channel Select Inputs These pins are address inputs for selecting eight analog inputs of AIN0 ∿ AIN7, and are taken into the internal latch
19	CHS_1	
20	CHS_0	
21	V_{SS}	Digital Ground
22	AGND	Analog Ground
23	$V_{REF/2}$	Reference voltage supply terminal, which supplies the voltage of $\frac{V_{REF} - A_{GND}}{2}$
24	V_{REF}	Reference voltage supply terminal
25	A_{IN7}	Analog input terminal Input voltage range: AGND ∿ V_{REF} Arbitrary input can be selected by CHS input.
26	A_{IN6}	
27	A_{IN5}	
28	A_{IN4}	
29	A_{IN3}	
30	A_{IN2}	
31	A_{IN1}	
32	AIN0	
33	INT_I	Integrator Input Integrator Junction Integrator Output The integrator consists of these three terminals.  R_I and C_I should satisfy the following formula and be set as small a value as possible $R_I \cdot C_I > \frac{13000}{fOSC}$ [S] However, R of 1 ∿ 2MΩ should be used.
34	INT_J	
35	INT_O	
36	C_2	Capacitors connection terminals for offset calibration.

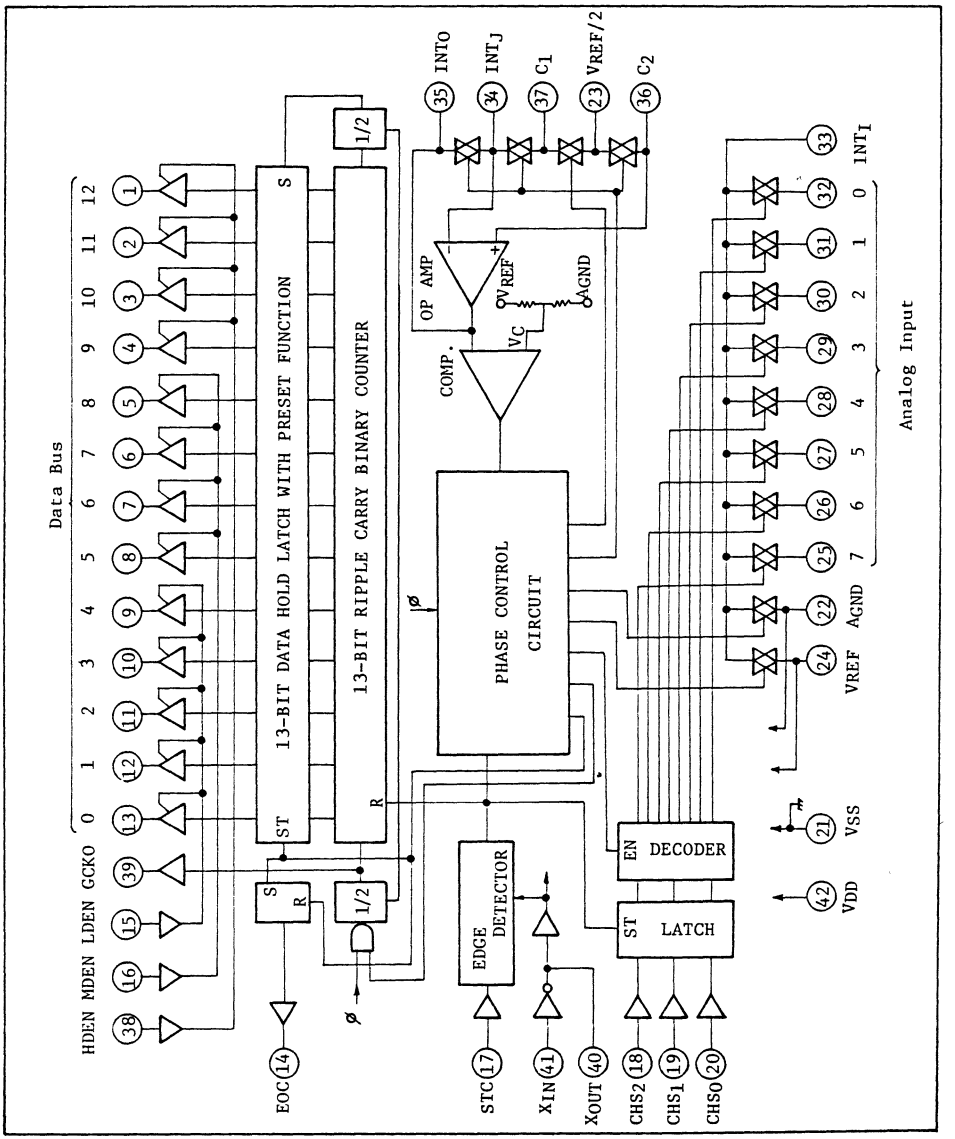
CHS_0	CHS_1	CHS_2	A_{IN}
L	L	L	AIN0
H	L	L	AIN1
L	H	L	AIN2
H	H	L	AIN3
L	L	H	AIN4
H	L	H	AIN5
L	H	H	AIN6
H	H	H	AIN7

TC5092AP

FUNCTION OF EACH PIN

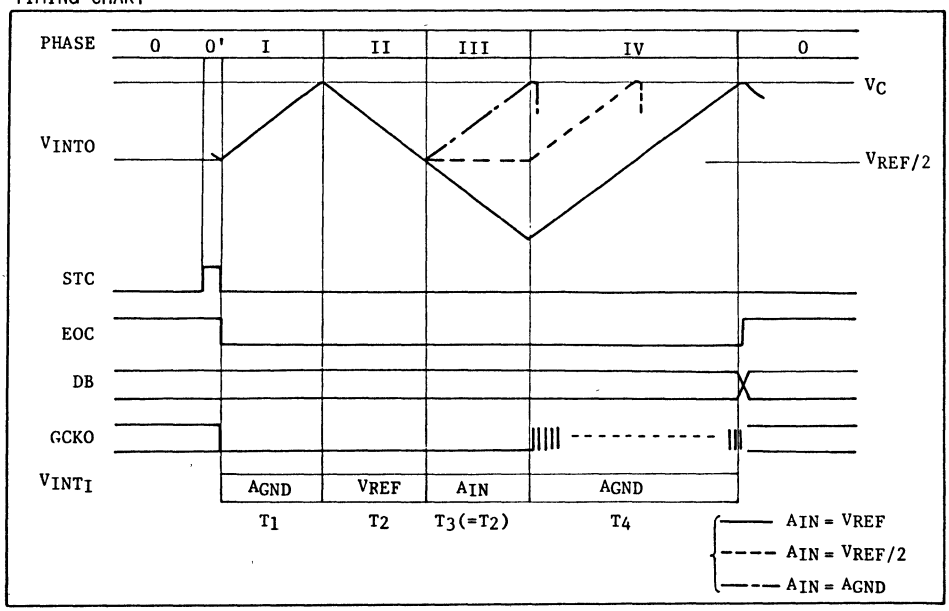
PIN NO.	Symbol	NAME & FUNCTION
37	C_1	0.1μF is connected between C_2 and C_1, and 0.01μF C_1 and V_{SS}, respectively.
38	HDEN	High Data Enable $DB_9 \sim DB_{12}$ are read by "H" level input.
39	GCKO	Gated Clock Output Pulses of number equivalent to conversion data are output during conversion.
40	X_{OUT}	Terminals for system clock oscillation. Crystal oscillators are connected to both the ends of terminals.
41	X_{IN}	
42	V_{DD}	Supply Voltage 5V±0.5V

SYSTEM DIAGRAM



TC5092AP

TIMING CHART



FUNCTIONAL DESCRIPTION

(1) Conversion cycle

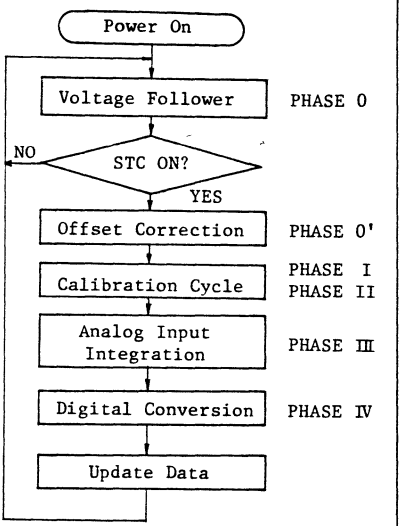
In the state of PHASE 0', the operation of LSI is at a stop and the integrating amplifier performs as voltage follower. Under this condition the external capactor (0.1μF across C_1 and C_2)

When STC is given, the offset voltage charged into external capacitors is applied to non-inversion of the integrator, thus cancelling the offset volage equivalently. In PHASE I, the integrator continues to integrate A_{GND} until its output reaches V_C.

In PHASE III the integrator integrates the analog input for the same period of time as T_2 after it has integrated V_{REF} for a fixed period of time (T_2) in PHASE II.

Finally, in PHASE IV the integrator continues to integrate A_{GND} until its output reaches V_C.

FUNCTIONAL DESCRIPTION



Let the time in PHASE IV be T_4. Then the following equation is made (formed) by omitting error factors such as offset drift.

$$V_{AIN} = \frac{T_4}{2T_2} V_{REF} \quad (AGND=0V) \quad \cdots (1)$$

In case of this LSI, T_2 is designed by 4096 x $2 \cdot T_{OSC}$ (T_{OSC} denotes reference clock synchronization). Therefore, the above formula letting $2 \cdot T_{OSC}$ be T is changed as follows:

$$\frac{V_{AIN}}{V_{REF}} = \frac{T_4}{8192T} \quad \cdots\cdots\cdots\cdots\cdots (2)$$

That is, 13-bit resolution A/D conversion of FS (full scale) = 8192 can be made by counting the period of T_4 by use of a clock having T frequency.

However, it is recommended that R_I and C_I composing the integrator be set to the values close to $13000/f_{OSC}$ as possible after having satisfied the following formula.

$$R_I C_I > 13000 / f_{OSC}, \; R_I = 1 \sim 2M\Omega \text{ is used.} \quad \cdots\cdots\cdots (3)$$

(2) Output data format

13-bit output data are output to 13 independent 3-state data buses $DB_0 \sim DB_{12}$. Since 13-bit outputs can be independently placed on 3-state every group of High, Medium and Low of 4 bits/4 bits/5 bits from the higher order, it is easy to connect the microcomputer to buses of 4, 8, 12 bits.

TC5092AP

FUNCTIONAL DESCRIPTION

TRUTH TABLE

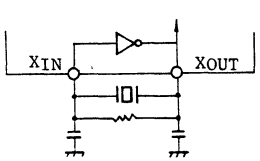
LDEN	MDEN	HDEN	Analog Input	DATA OUTPUTS (DB)												
				0	1	2	3	4	5	6	7	8	9	10	11	12
L	L	L	Don't Care	Z					Z				Z			
H	L	L		D	D	D	D	D								
L	H	L		Z					D	D	D	D				
H	H	L		D	D	D	D	D	D	D	D	D				
L	L	H		Z					Z				D	D	D	D
H	L	H		D	D	D	D	D					D	D	D	D
L	H	H		Z					D	D	D	D	D	D	D	D
H	H	H	<1/2LSB	L	L	L	L	L	L	L	L	L	L	L	L	L
			1/2LSB ∿ 3/2LSB	H	L	L	L	L	L	L	L	L	L	L	L	L
			.....	Straight Binary												
			"FS"-5/2LSB ∿ "FS"-3/2LSB	L	H	H	H	H	H	H	H	H	H	H	H	H
			"FS"-3/2 LSB <	H	H	H	H	H	H	H	H	H	H	H	H	H

Note : FS ····· Full Scale, 1 LSB = (VREF-AGND)/8192, Z ··· High Impedance
D ··· "H" or "L" Level

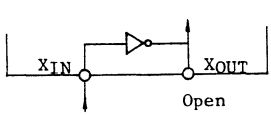
(3) Basic clock

Since this LSI operates on the basis of the frequency given to X_{IN} input, a stable clock ($\Delta f < 0.005\%$) must be used for the clock to be given to X_{IN}.

Therefore, it is proper that the oscillation circuit is configured as shown in the following figure (a) by the use of externally mounted crystal becuase the LSI has a built-in inverter for crystal oscillation.



(a)



External Clock

(b)

FUNCTIONAL DESCRIPTION

(4) How to give STC input, Conversion time, and Sampling cycle

STC input is taken in with the reference clock of LSI, but the positive pulse having the pulse width for at least two cycles is required for internal starting.

The conversion time of from the fall of STC input to the rise of EOC output. Letting this time be Tc MAX(Maximum conversion time), then the following equation is obtained.

$$TcMAX = 41000 \times T_{OSC}\ [S] \quad \cdots\cdots\cdots\cdots\cdots\cdots\ (4)$$

(where T_{OSC} is oscillation cycle of basic clock.)

For example, when f_{CP}=5MHz, TcMAX=8.2ms. For one-time sampling, an accurate output can be obtained from the falling edge of STC input after the lapse of TcMAX.

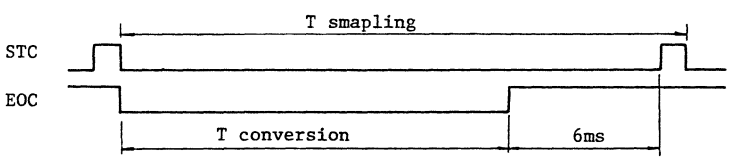
For consecutive sampling, however, STC input must be given after the lapse of a given period of time (6ms) from the rise of EOC. This period (6ms) is the time required for the recovery of LSI to normal state.

Therefore, the minimum sampling cycle TsMIN is as follows:

$$TsMIN = 41000 \times T_{OSC} + 0.006 + t_w(STC)\ [S] \quad \cdots\cdots\ (5)$$

Note: When power is set ON, following start-up procedure is required due to indefinite state of internal circuitry.

1. Applying clock, STC is to be set high over 10ms.
2. Complete at least one cycle as a dummy conversion cycle.



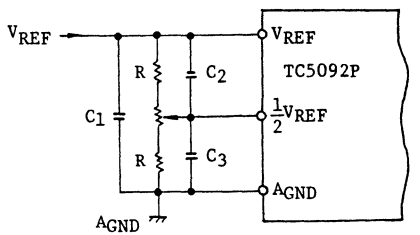
5) Reference voltage

This LSI has three reference input voltage terminals of A_{GND}, $\frac{1}{2}V_{REF}$, and V_{REF}. Since analog input signal is quantized to 1/8192 in the range of $A_{GND} \sim A_{REF}$ for digitization, stable voltages must be supplied to $\frac{1}{2}V_{REF}$ and V_{REF}.

TC5092AP

FUNCTIONAL DESCRIPTION

Espacially the value of $\frac{1}{2}$ VREF voltage has direct effects upon conversion accuracy; therefore, it is recommonded that adjustment be made so as to agree output data with analog input by actually making A/D convert by use of input voltage at FS (full scale) or 1/2FS level.

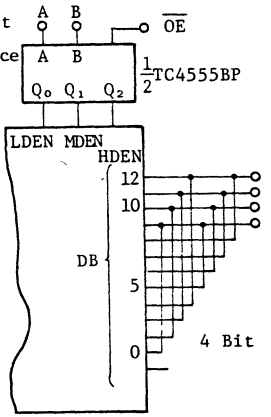


The left figure shows an example of reference voltage supplying circuit.
$C_1 \sim C_3$ are filter capacitors for preventing reference voltage variations to be caused by ripple or induction noise. Generally the value of capacitor is about $0.01 \sim 0.1\mu F$, though it varies with the system.

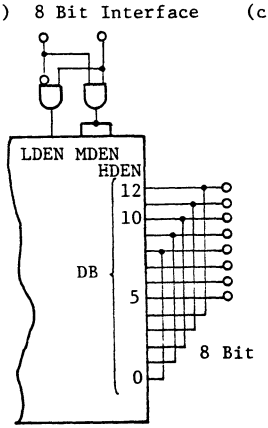
(6) BUS Interface

For connecting a microcomputer to BUS line, three independent enable terminals are used. These three enable terminals permit the processing in the unit of 4 bits (5 bits for the low order digit only). The microcomputer can be directly connected to the BUS of $4 \sim 12$ bits easily by allocating proper address of microcomputer to the TC5092AP.

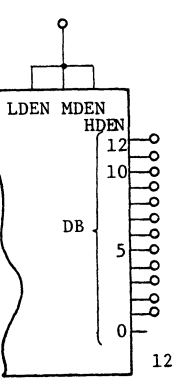
(a) 4 Bit Interface



(b) 8 Bit Interface



(c) 12 Bit Interface



RECOMMENDED OPERATING CONDITION

ITEM	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Digital Input Voltage	V_{IN}		0	-	V_{DD}	V
Analog Input Voltage	V_{AIN}		AGND	-	V_{REF}	-
Reference Supply Voltage	V_{REF}		4.0	-	V_{DD}	V
Analog Ground Voltage	V_{AGND}		0	0	0.5	V

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = -40 ~ 85°C)

ITEM	SYMBOL	TEST CONDITION		V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output High Voltage	V_{OH}	I_{OH}=-1μA, Digital output		5	4.9	5.0	-	V
Output Low Voltage	V_{OL}	I_{OL}=1μA, Digital output		5	-	0.0	0.1	
Input High Voltage	V_{IH}	Digital Input except X_{IN}		5	2.4	-	-	V
		X_{IN}		5	4.5	-	-	
Input Low Voltage	V_{IL}	Digital Input except X_{IN}		5	-	-	0.8	
		X_{IN}		5	-	-	0.5	
Output High Current	I_{OH}	V_{OH} = 2.4V Digital output except X_{OUT}		4.75	-1.0	-	-	mA
Output Low Current	I_{OL}	V_{OL} = 0.4V Digital output except X_{OUT}		4.75	1.6	-	-	mA
Output Disable Current	I_{DH}	V_{OH} = 5.5V, DB_0 ~ DB_{12}		5.5	-	10^{-3}	5	μA
	I_{DL}	V_{OL} = 0.0V, DB_0 ~ DB_{12}		5.5	-	-10^{-3}	-5	
Input Current	I_{IH}	V_{IN}=5.5V, Digital input		5.5	-	10^{-5}	1.0	
	I_{IL}	V_{IL}=0.0V, Digital input		5.5	-	-10^{-5}	-1.0	
Analog Switch Off-Leak	I_{OFF}	Analog input/output		5.5	-	$\pm 10^{-4}$	-	μA
Analog Switch On Resistor	R_{ON}	R_L = 10kΩ		5	-		-	Ω
Operating Consumption Current	I_{DD}	V_{REF} = V_{DD} Digital output open Digital input GND	f_{CP}=5MHz	5	-	2	-	mA
			f_{CP}=1MHz	5	-	1	-	

TC5092AP

SWITCHING CHARACTERISTICS (V_{DD} = 5V±10%, V_{SS} = 0V, Ta = 25°C, C_L = 50pF)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_r	Digital output	-	50	150	ns
Output Fall Time	t_f	Digital output	-	40	150	
Output Enable Time	t_{ZL} t_{ZH}	LDEN, MDEN, HDEN -DB Output	-	-	-	ns
Output Disable Time	t_{LZ} t_{HZ}	LDEN, MDEN, HDEN -DB Output	-	-	-	
Max. Clock Frequency	$f_{MAX\phi}$	X_{IN}	5.0	-	-	
Min. Clock Frequency	$f_{MIN\phi}$	X_{IN}	-	-	-	MHz
Input Capacity	C_{IN}	Digital input	-	-	-	pF
	C_{IN}	Analog input	-	-	-	
3-State Output Capacity	C_{OUT}	DB Output	-	-	-	

SYSTEM CHARACTERISTICS (V_{DD} = 5V±10%, V_{SS} = 0V, Ta = 25°C)

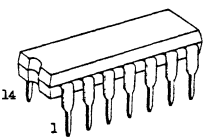
ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Resolution	n		-	13	-	Bit
Conversion Time	Tc	f_{CP} = 5 MHz	-	-	8.2	ms
		f_{CP} = 1 MHz	-	-	41	
Sampling Cycle	T_{SPL}	f_{CP} = 5 MHz	14.2	-	-	ms
		f_{CP} = 1 MHz	47	-	-	
Nonlinearity		V_{DD} = V_{REF}	-	±1		LSB
Zero Scale Error	E_{ZP}		-	±2		
Full Scale Error	E_{FS}		-	±1		
STC Min. Pulse Width	t_w		-	-	$2/f_{OSC}$	s

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC7400BP

TC7400BP QUAD 2-INPUT POSITIVE NAND GATE

TC7400BP is two input positive logic NAND gate. Since all the outputs of this gate are equiped with buffers which consist of inverters, the input/output transmission characteristic has been improved and the variation of transmission time caused by increase of load capacity has been kept minimum.



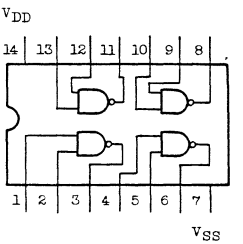
DIP 14 (3D14A-P)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	Tstg	-65 ~150	°C
Lead Temp./Time	Tsol	260°C · 10sec	

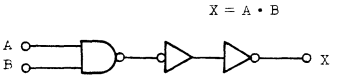
PIN ASSIGNMENT

TC7400BP



LOGIC DIAGRAM

1/4 TC7400BP



TC7400BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temp.	Topr		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
"H" Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ V_{IN} = V_{SS},V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
"L" Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ V_{IN} = V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
"H" Level Output Current	I_{OH}	V_{OH} = 4.6V V_{OH} = 9.5V V_{OH} = 13.5V V_{IN} = V_{SS},V_{DD}	5	-0.2	-	-0.16	-0.5	-	-0.12	-	mA
			10	-0.5	-	-0.4	-1.2	-	-0.3	-	
			15	-1.4	-	-1.2	-6.0	-	-1.0	-	
"L" Level Output Current	I_{OL}	V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V V_{IN} = V_{DD}	5	0.52	-	0.44	1.5	-	0.36	-	
			10	1.3	-	1.0	3.5	-	0.9	-	
			15	3.6	-	3.0	15	-	2.4	-	
"H" Level Input Voltage	V_{IH}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\| < 1\mu A$	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
"L" Level Input Voltage	V_{IL}	V_{OUT}= 4.5V V_{OUT}= 9.0V V_{OUT}= 13.5V $\|I_{OUT}\| < 1\mu A$	5	-	1.5	-	2.25	1.5	-	1.5	
			10	-	3.0	-	4.5	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
Input Current "H" Level	I_{IH}	V_{IH} = 18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL} = 0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current	I_{DD}	V_{IN} = V_{SS},V_{DD} *	5	-	1.0	-	0.001	1.0	-	7.5	μA
			10	-	2.0	-	0.001	2.0	-	15	
			15	-	4.0	-	0.002	4.0	-	30	

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

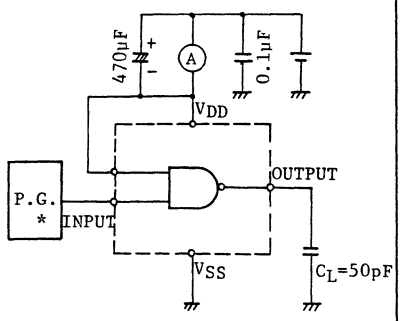
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_r		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Fall Time	t_f		5	-	100	200	
			10	-	50	100	
			15	-	40	80	

TC7400BP

ITCHING CHARACTERISTICS (Ta=25°C, V_{SS}-0V, C_L=50pF)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
C7400BP	(Low-High) Propagation Delay Time	t_{pLH}		5	-	140	300	ns
				10	-	60	150	
				15	-	50	125	
	(High=Low) Propagation Delay Time	t_{pHL}		5	-	180	300	
				10	-	80	150	
				15	-	60	125	
Input Capacitance		C_{IN}			-	5	7.5	pF

TEST CIRCUIT



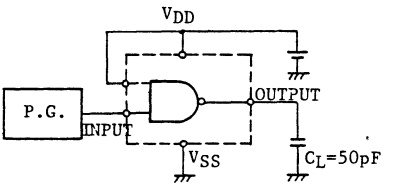
* INPUT PULSE CONDITION

DUTY RATIO = 50%

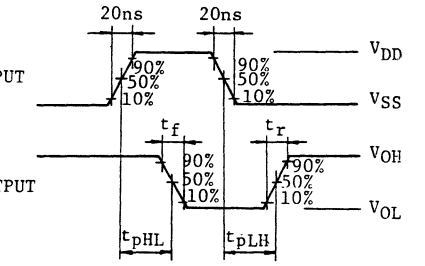
t_r=t_f=20ns

SWITCHING TIME TEST CIRCUIT AND WAVEFORM

TEST CIRUCIT



WAVEFORM

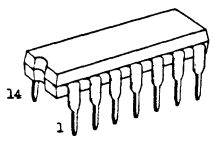


TC7404UBP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC7404UBP HEX INVERTING BUFFER

TC7404UBP contains six circuits of inverter type buffers. This has pin to pin compatibility with TC4069UBP and its large output current enables to directly drive one TTL with 5 volt power supply.
In addition to its original application as inverters, this can be used as clock drivers and for TTL interface circuits.

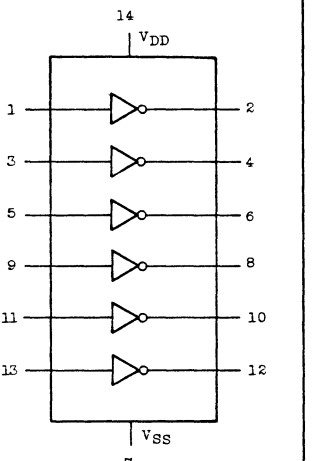


DIP 14 (3D14A-P)

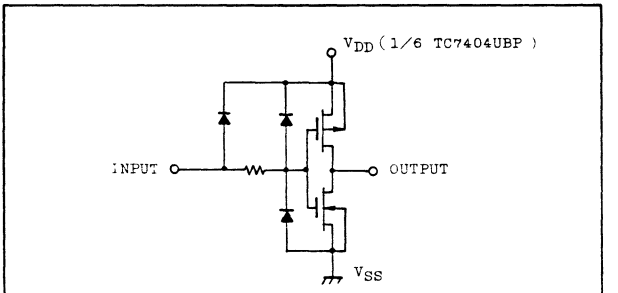
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



CIRCUIT DIAGRAM



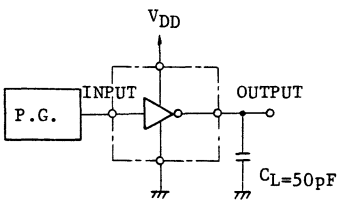
RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

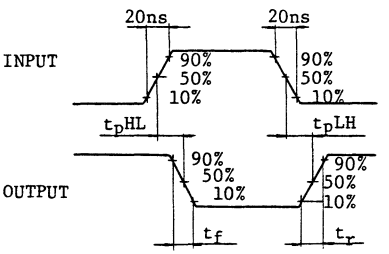
CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature Range	T_{opr}		-40	-	85	°C

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
(Low-High) Propagation Delay Time	t_pLH	5	-	80	150	ns
		10	-	40	100	
		15	-	35	80	
(High-Low) Propagation Delay Time	t_pHL	5	-	50	150	ns
		10	-	30	100	
		15	-	25	80	
Input Capacity	C_{IN}		-	15	-	pF

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





P.G.: PULSE GENERATOR

TC7404UBP

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|$ <1μA, $V_{IN}=V_{SS}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|$ <1μA, $V_{IN}=V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
High Level Output Current	I_{OH}	V_{OH}=2.5V, $V_{IN}=V_{SS}$	5	-1.40	-	-1.25		-	-1.0	-	mA
		V_{OH}=9.5V, $V_{IN}=V_{SS}$	10	-1.40	-	-1.25		-	-1.0	-	
		V_{OH}=13.5V, $V_{IN}=V_{SS}$	15	-4.00	-	-3.75		-	-3.0	-	
Low Level Output Current	I_{OL}	V_{OL}=0.4V, $V_{IN}=V_{DD}$	5	3.5	-	3.2		-	2.5		
		V_{OL}=0.5V, $V_{IN}=V_{DD}$	10	6.0	-	5.0		-	3.6		
		V_{OL}=1.5V, $V_{IN}=V_{DD}$	15	26.0	-	24.0		-	18.0		
High Level Input Voltage	V_{IH}	V_{OUT}=0.5V, $\|I_{OUT}\|$ <1μA	5	4.0	-	4.0	3.0	-	4.0	-	V
		V_{OUT}=1.0V, $\|I_{OUT}\|$ <1μA	10	8.0	-	8.0	6.5	-	8.0	-	
		V_{OUT}=1.5V, $\|I_{OUT}\|$ <1μA	15	12.0	-	12.0	9.5	-	12.0	-	
Low Level Input Voltage	V_{IL}	V_{OUT}=4.5V, $\|I_{OUT}\|$ <1μA	5	-	1.0	-	2.0	1.0	-	1.0	
		V_{OUT}=9.0V, $\|I_{OUT}\|$ <1μA	10	-	2.0	-	2.5	2.0	-	2.0	
		V_{OUT}=13.5V, $\|I_{OUT}\|$ <1μA	15	-	2.5	-	3.0	2.5	-	2.5	
H.Level Input Current	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
L.Level Input Current	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Current Consumption	I_{DD}	$V_{IN}=V_{SS}, V_{DD}$ *	5	-	4.0	-	0.002	4.0	-	30	μA
			10	-	8.0	-	0.004	8.0	-	60	
			15	-	16.0	-	0.008	16.0	-	120	

* All valid input combination

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_r		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Fall Time	t_f		5	-	100	200	
			10	-	50	100	
			15	-	40	80	

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

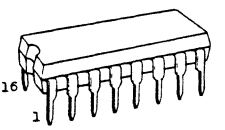
TC7476BP

TC7476BP DUAL J-K MASTER-SLAVE FLIP-FLOP

TC7476BP is J-K master-slave flip-flop having $\overline{\text{Clear}}$ and $\overline{\text{Preset}}$ functions.

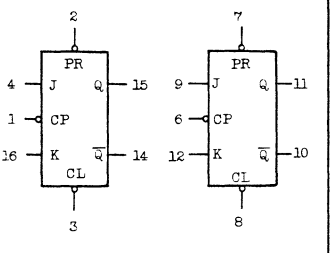
J-K Mode ; When clock input is applied with $\overline{\text{CLEAR}}$ and $\overline{\text{PRESET}}$ kept at "H", the output varies depending on the conditions of J and L at the falling edge of $\overline{\text{CLOCK}}$ input.

R-S Mode ; When CLEAR is set to "L", output Q becomes "L" regardless of other inputs, and when $\overline{\text{PRESET}}$ is set "L" and $\overline{\text{CLEAR}}$ is set "H", Q becomes "H" regardless of other inputs.



DIP 16 (3D16A-P)

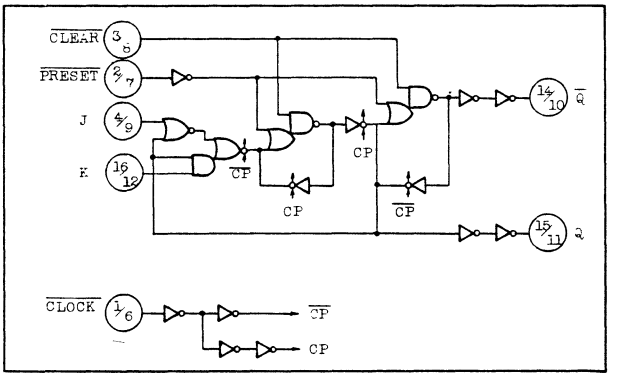
PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	Tstg	-65 ~ 150	°C
Lead Temp./Time	Tsol	260°C · 10sec	

LOGIC DIAGRAM



TRUTH TABLE

INPUTS					OUTPUT	
$\overline{CL}$	$\overline{PR}$	J	K	$\overline{CP}\wedge$	Q_{n+1}	$\overline{Q}_{n+1}$
H	L	*	*	*	H	L
L	H	*	*	*	L	H
L	L	*	*	*	L	H
H	H	L	L	↓	Q_n	$\overline{Q}_n$ •
H	H	L	H	↓	L	H
H	H	H	L	↓	H	L
H	H	H	H	↓	$\overline{Q}_n$	Q_n ••
H	H	*	*	↑	Q_n	$\overline{Q}_n$ •

* Don't care
∧ Level change
• No change
•• Change

TC7476BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temp.	Topr		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
"H" Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
"L" Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
"H" Level Output Current	I_{OH}	V_{OH} = 4.6V V_{OH} = 9.5V V_{OH} = 13.5V $V_{IN} = V_{SS}, V_{DD}$	5	-0.2	-	-0.16		-	-0.12	-	mA
			10	-0.5	-	-0.4		-	-0.3	-	
			15	-1.4	-	-1.2		-	-1.0	-	
"L" Level Output Current	I_{OL}	V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V $V_{IN} = V_{SS}, V_{DD}$	5	0.52	-	0.44		-	0.36	-	
			10	1.3	-	1.1		-	0.9	-	
			15	3.6	-	3.0		-	2.4	-	
"H" Level Input Voltage	V_{IH}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\| < 1\mu A$	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
"L" Level Input Voltage	V_{IL}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\| < 1\mu A$	5	-	1.5	-	2.25	1.5	-	1.5	
			10	-	3.0	-	4.5	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
Input Current "H" Level	I_{IH}	V_{IH} = 18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL} = 0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ *	5	-	4.0	-	0.002	4.0	-	30	μA
			10	-	8.0	-	0.004	8.0	-	60	
			15	-	16.0	-	0.008	16.0	-	120	

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_r		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Fall Time	t_f		5	-	100	200	
			10	-	50	100	
			15	-	40	80	

TC7476BP

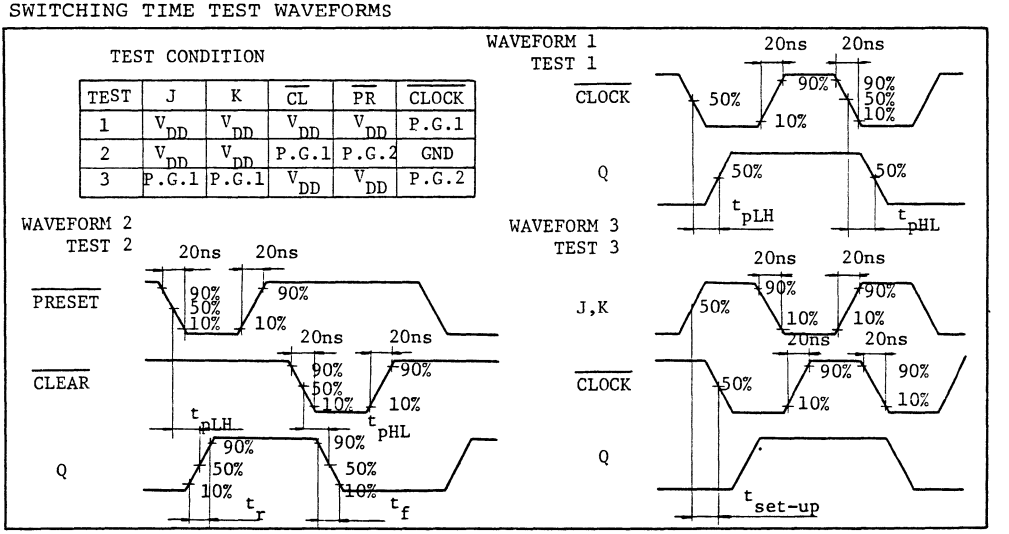
SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=OV, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
(Low-High) Propagation Delay Time ($\overline{CLOCK}$ - Q, $\overline{Q}$)	t_{pLH}	Waveform 1	5	-		550	ns
			10	-		350	
			15	-		300	
(High-Low) Propagation Delay Time ($\overline{CLOCK}$ - Q, $\overline{Q}$)	t_{pHL}	Waveform 1	5	-		500	
			10	-		300	
			15	-		260	
(Low-High) Propagation Delay Time ($\overline{CL}$, $\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH}	Waveform 2	5	-		600	ns
			10	-		300	
			15	-		260	
(High-Low) Propagation Delay Time ($\overline{CL}$, $\overline{PR}$ - Q, $\overline{Q}$)	t_{pHL}	Waveform 2	5	-		600	
			10	-		300	
			15	-		260	
Max. Clock Frequency	$f_{MAX\phi}$	Waveform 1	5	1.0		-	MHz
			10	3.0		-	
			15	3.5		-	
Max. Clock Rise Time	$t_{r\phi}$	Waveform 1	5	20	-	-	μs
Max. Clock Fall Time	$t_{f\phi}$		10	2.5	-	-	
			15	1.0	-	-	
Min. Clear, Preset Pulse Width	t_w ($\overline{CLEAR}$)	Waveform 2	5	-		500	ns
	t_w ($\overline{PRESET}$)		10	-		250	
			15	-		200	
Min. Set-up Time	t_{set-up}	Waveform 3	5	-		250	ns
			10	-		125	
			15	-		100	
Input Capacitance	C_{IN}				5	7.5	pF

SWITCHING TIME TEST WAVEFORMS

TEST CONDITION

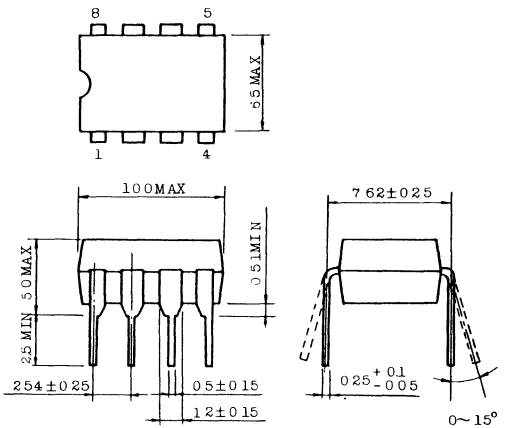
TEST	J	K	$\overline{CL}$	$\overline{PR}$	$\overline{CLOCK}$
1	V_{DD}	V_{DD}	V_{DD}	V_{DD}	P.G.1
2	V_{DD}	V_{DD}	P.G.1	P.G.2	GND
3	P.G.1	P.G.1	V_{DD}	V_{DD}	P.G.2



DIMENSIONAL OUTLINES

DIP 8 PIN OUTLINE DRAWING (3D8A-P)

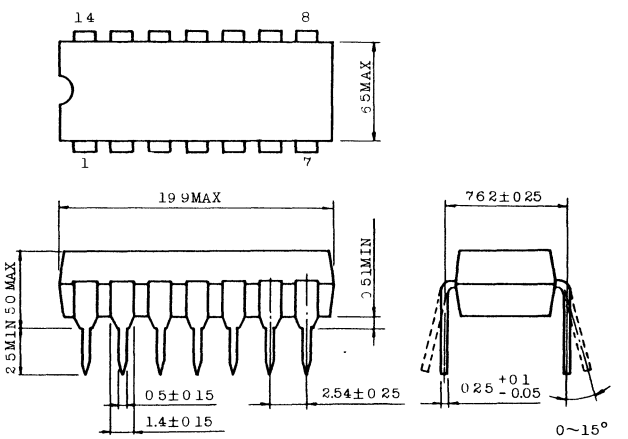
Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.8 leads.

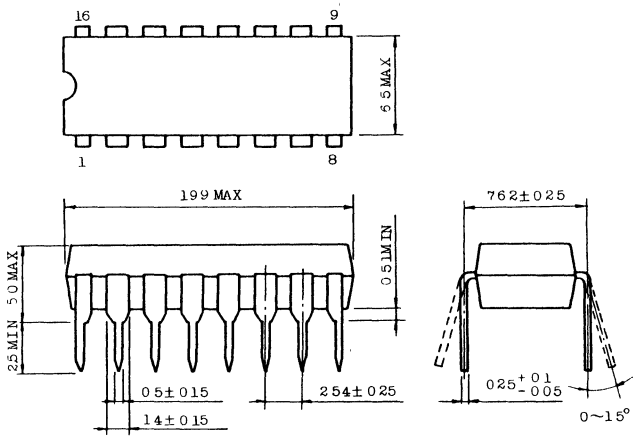
DIP 14 PIN OUTLINE DRAWING (3D14A-P)

Unit in mm



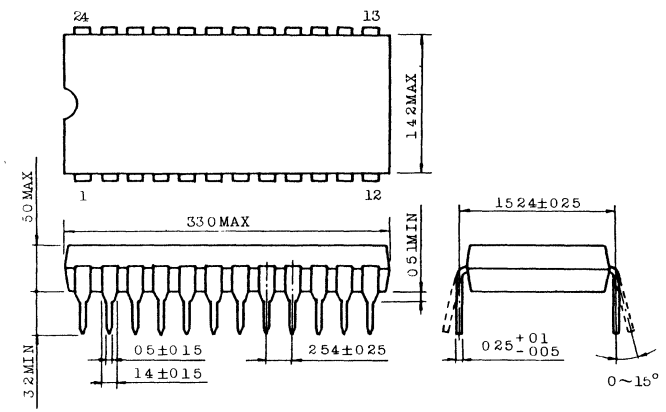
Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.14 leads.

DIP 16 PIN OUTLINE DRAWING (3D16A-P) Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.16 leads.

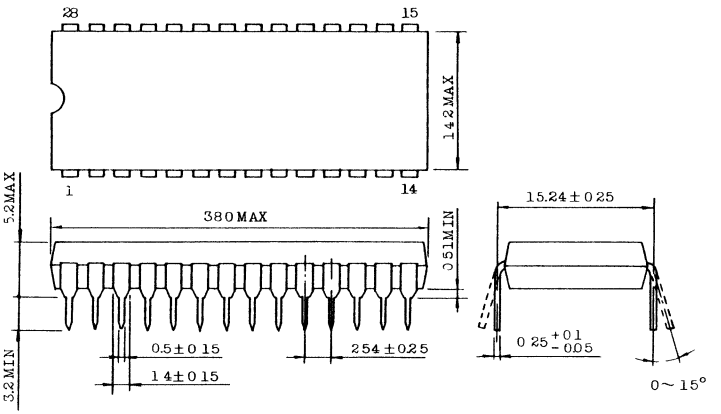
DIP 24 PIN OUTLINE DRAWING (6D24A-P) Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.24 leads.

DIP 28 PIN OUTLINE DRAWING (6D28A-P)

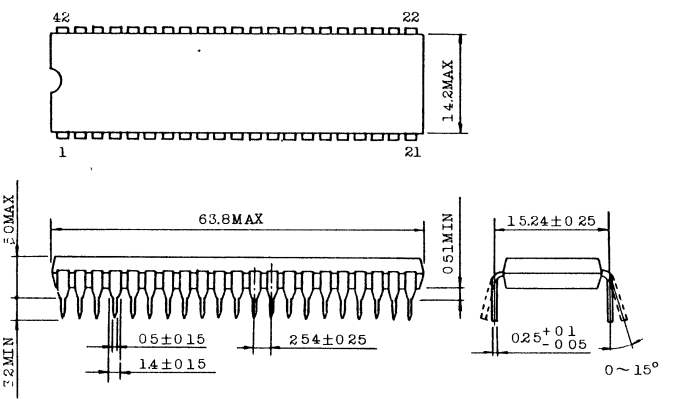
Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

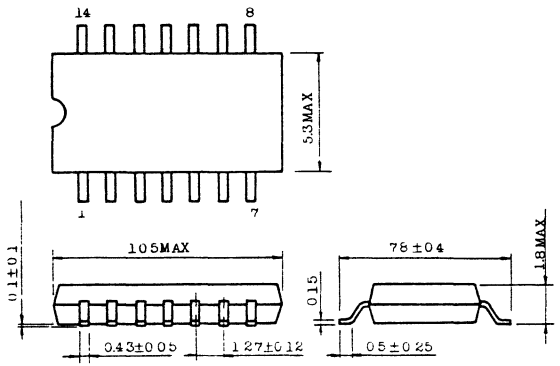
DIP 42 PIN OUTLINE DRAWING (6D42A-P)

Unit in mm



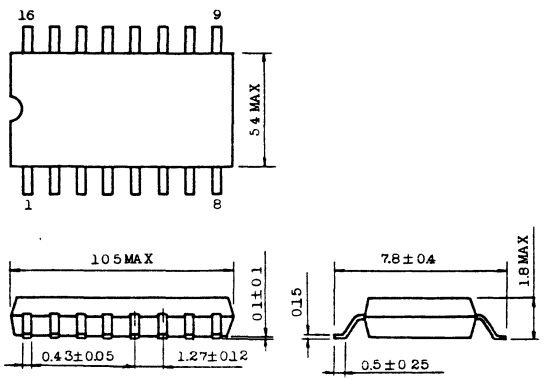
Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.42 leads.

MFP 14 PIN OUTLINE DRAWING (F14GB-P) Unit in mm



Note) Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.14 laeds.

MFP 16 PIN OUTLINE DRAWING (F16GC-P) Unit in mm



Note) Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.16 leads.

MAINTENANCE-DISCONTINUED TYPE NUMBERS

MAINTENANCE-DISCONTINUED TYPE NUMBERS

TYPE NO.	FUNCTION	REPLACEMENT
TC4508C	DUAL 4-BIT LATCH	TC4508BP
TC5000C/P	DUAL 50/64 STAGE STATIC SHIFT REGISTER	TC5050P
TC5001C	4-DIGIT DECADE COUNTER	TC5001P
TC5004P	DUAL 500/512-BIT DYNAMIC SHIFT REGISTER	-
TC5010P	4-DIGIT UP/DOWN COUNTER WITH TIMER	(TC5053P), (TC5054P)
TC5030BP	QUAD 2-INPUT NAND GATE WITH P-CHANNEL OPEN DRAIN OUTPUT	-
TC5034P	4-BIT PRESETTABLE "N" COUNTER/DECODER/DRIVER	-
TC5042BP	BCD TO 7-SEGMENT DECODER/DRIVER	TC5002BP, TC5022BP
TC5055P	3 1/2 DIGIT DVM CIRCUIT	-
TC7410BP	TRIPLE 3-INPUT POSITIVE NAND GATE	TC4023BP
TC7420BP	DUAL 4-INPUT POSITIVE NAND GATE	TC4012BP

Note: The replacement types are approximately similar to the maintenance types in terms of the characteristics and functions, but not exact equivalent. In case of doubt the original data sheets should be consulted before use.