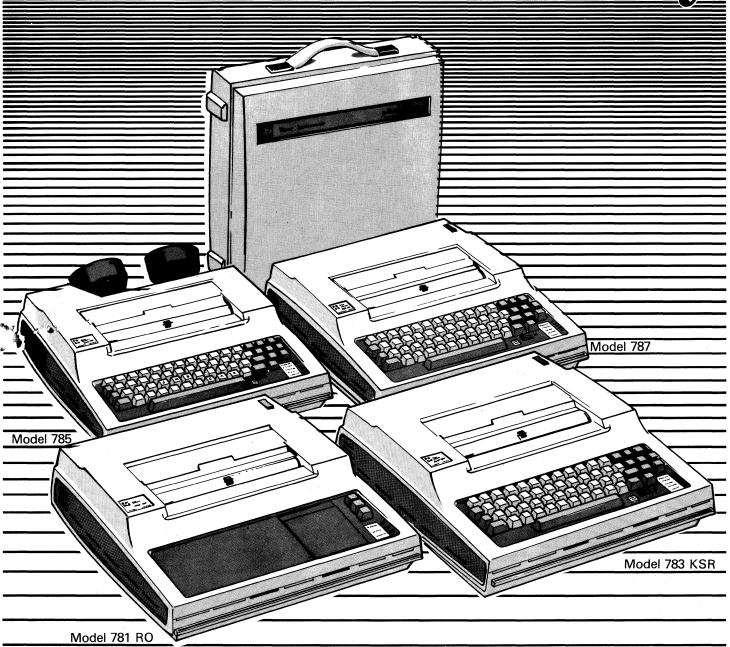




780 Series Electronic Data Terminal Family



Maintenance Manual

Manual No. 2265862-9701

TEXAS INSTRUMENTS

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780 Series Electronic Data Terminal Family

Part No. 2265862-9701

Original Issue: 15 March 1981

Total number of pages in this publication is 314 consisting of the following:

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Revision		ECN			
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Preface

SCOPE OF MANUAL

This manual contains descriptions, installation and operating instructions, communications protocol, theory of operation and maintenance procedures for the 780 Series, *Silent 700** Electronic Data Terminals. The information in this manual is intended to help in maintaining and servicing these terminals. The troubleshooting information is designed to help isolate problems in a major replaceable assembly.

Section 1 contains a general description of each model in the 780 Series. It also includes specifications and a brief description of the options offered with each terminal.

Section 2 provides installation and interfacing information.

Section 3 contains terminal operating information.

Section 4 describes terminal communications features.

Section 5 describes in detail the theory of operation.

Section 6 covers preventive maintenance procedures and tests that can be used to isolate problems.

Section 7 contains assembly drawings and associated lists of material.

Section 8 provides the schematic diagrams.

The appendixes provide additional information on the microprocessor and I/O controller, the character sets and foreign keyboards, recommended data set options and cabling information, a glossary of signals, and quick reference cards.

REFERENCES

Other TI manuals concerning the 780 Series terminals include:

- Model 781 Operating Instructions, TI Part No. 2265935-9701,
- Model 783 Operating Instructions, TI Part No. 2265936-9701,
- Model 785 Operating Instructions, TI Part No. 2265937-9701,
- Model 787 Operating Instructions, TI Part No. 2265938-9701.

The operating instructions are furnished with the respective terminal when shipped from the factory.

Operator Reference Cards which provide terminal operating information in a condensed format are attached to the inside of the paper door. Additional Quick Reference Cards can be ordered by the following TI Part Numbers:

 Model 781 Operator Reference Cards, TI Part No. 2265927,

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- Model 783 Operator Reference Cards, TI Part No. 2265941,
- Model 785 Operator Reference Cards, TI Part No. 2265942,
- Model 787 Operator Reference Cards, TI Part No. 2265943.

USER'S RESPONSE

If you have corrections or suggestions to improve this manual, please fill out the User's Response sheet found in the back of this manual. Simply remove the sheet, add your comments, fold and mail (no postage is necessary when mailed in the United States). We appreciate your comments and may contact you, if appropriate, to answer any questions you may pose.

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Section 1

Equipment Description

1.1 INTRODUCTION

This section contains general descriptions, available options, physical dimensions, and specifications of the terminals in the 780 Series.

1.2 GENERAL DESCRIPTION

The 780 Series terminals are self-contained, compact, lightweight, programmable machines for use in a wide variety of telecommunications systems. The terminals can operate in both fixed location and portable applications. Communications data is input and output via a communications port, acoustic coupler or "direct-connect" jack, depending on the particular model. Each terminal is capable of communicating via an EIA RS-232-C interface or TTY current loop.

The terminal electronics consist primarily of an 8080A microprocessor, its associated memory, and interface circuitry to drive the printer mechanism and communications port.

The terminals utilize thermal printing and are capable of bidirectional printing at speeds up to 140 characters per second (cps) while handling communications data rates from 110 bits per second (bps) to 9600 bps.

Operating parameters such as communications mode, data transmission rate, parity selection, line

control, transmission control and terminal control are configurable directly from the operator interface by entering the proper code.

1.3 780 SERIES DATA TERMINALS

The 780 Series is comprised of the following terminals:

- Model 781 Receive-Only Printer,
- Model 783 Keyboard Send/Receive Data Terminal,
- Model 785 Portable Data Terminal, and
- Model 787 Portable Communications Data Terminal.

These terminals are described in more detail in the following paragraphs.

1.3.1 Model 781

The Model 781 Receive-Only (RO) Printer (Figure 1-1) is intended for applications requiring a hard-copy, high-speed output device. Using a dual-matrix thermal printhead, the 781 RO provides virtually silent printing at up to 140 cps. Operating parameters are entered from a calculator-type keypad.

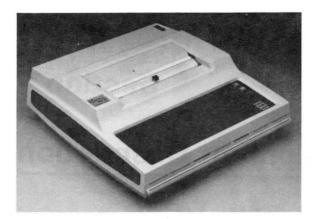


Figure 1-1. Model 781 RO Printer

1.3.2 Model 783

The Model 783 Keyboard Send/Receive (KSR) Data Terminal shown in Figure 1-2 is highly suited for conversational, data/text entry, inquiry-response, and computer console applications. Operating parameters are configured by entering the desired code via the typewriter-like keyboard.



Figure 1-2. Model 783 KSR Data Terminal

1.3.3 Model 785

The Model 785 Portable Data Terminal (Figure 1-3) is similar to the Model 783 but includes an internal modem. The modem is a dual-speed, originate-only, full-duplex modem, with an acoustic coupler interface which permits communication over standard commercial telephone lines at communications rates of 110, 300, and 1200 bps. The modem provides communications compatibility with answering Racal-Vadic VA3400 Series and Bell 103/113-type data sets. This feature provides great flexibility, permitting use of

the terminal wherever a telephone and electrical outlet are available.



Figure 1-3. Model 785 Portable Data Terminal

1.3.4 Model 787

The Model 787 Portable Communications Data Terminal (Figure 1-4) is similar to the Model 785 except that the internal modem is a dual-speed, answer/originate, full-duplex modem. The modem has a direct-connect interface which allows it to be plugged directly into a voice or data jack for communication over standard commercial telephone lines. The modem provides communications compatibility with all Racal-Vadic VA3400 series and Bell 103/113/212-type data sets. As an option, the 787 has an acoustic-coupler interface that provides greater flexibility.



Figure 1-4. Model 787 Portable Communications Data Terminal

1.4 OPTIONS

A variety of options provide versatility and flexibility for the 780 Series data terminals. These options are listed in Table 1-1 and identify the applicable terminal.

Table 1-1. Terminal Options

Option	781	783	785	787
International Character Sets	х	х	Х	х
Additional 1000-Character Buffer	x	X.	N/A	N/A
300-Foot Paper Adapter	x	х		*
Paper-Out Indicator	x	x	N/A	×
APL/Full ASCII Keyboard/Character Set		x	x	×
Katakana Keyboard/Character Set	×	x		
Protected ABM	×	x	x	x
Acoustic-Coupler Interface			**	X
EIA or Current Loop Interface Cable	**	**	**	**
Tone Dial Assist				×

N/A Not applicable

** Standard

^{*} Not compatible with acoustic-coupler interface

1.5 PHYSICAL DIMENSIONS

1.5.1 Size

Height: 139 mm (5.5 in)

Width: 391 mm (15.4 in)

Depth: 406 mm (16.0 in)

1.5.2 Weight

Model 781: 5.4 kg (12 lbs)

Model 783: 5.9 kg (13 lbs)
Model 785: 7.7 kg (17 lbs)
Model 787: 7.2 kg (16 lbs)

All weights include 110-foot paper roll.

1.6 ENVIRONMENTAL LIMITS

1.6.1 Non-Operating Environment

During shipping and storage the data terminals can withstand being subjected to the following:

In a shipping container:

Temperature: -30° C to $+70^{\circ}$ C (-22° F to $+158^{\circ}$ F).

Relative Humidity: 10% to 95% without condensation.

Shock: Drop from 1.22 meters (48") on each surface.

Vibration: Sinusoidal vibration of:

2 Gs-5 to 50 Hz 4 Gs-50 to 500 Hz.

Altitude: 15,000 meters (49,200 ft).

Cargo Bounce: Per MIL-STD-810B. One-inch double-orbital motion. 225 RPM, 30

minutes per side.

Without a shipping container:

Temperature: -30° C to $+70^{\circ}$ C (-22° F to 158° F).

Relative Humidity: 10% to 95% without condensation.

Shock: a. Portable mode

40 Gs, ½ sinewave

11 ms maximum through each axis.

b. Bench handling per MIL-STD-810B, method 516.1, procedure V.

1.6.2 Operating Environment

The data terminals are capable of operating in the following conditions:

Ambient Temperature:

10°C to 40°C (50°F to 104°F).

Relative Humidity:

10% to 95% without condensation.

Altitude:

3,500 meters (11,500 ft).

Vibration:

Sinusoidal vibration of 0.5 Gs peak in the range of 10 Hz to 60 Hz.

Temperature Shock:

Operate in a 23°C (73°F), 50% relative humidity environment within 30

minutes after being stored for two hours at -30°C (-22°F), 50%

relative humidity.

1.7 SPECIFICATIONS

The following specifications apply to all terminals.

1.7.1 Printer

Method:

Nonimpact, electrically heated, 5×7 dual-character matrix thermal

printhead, prints on thermographic paper.

Character Set:

95 printable characters in normal mode with 33 ASCII or CCITT control

characters when configured.

Character Size:

2.66 mm \times 2.0 mm (0.105 in \times 0.080 in).

Line Length:

203.2 mm (8.0 in); 25.4 mm spacing; 10 characters per inch; 80

characters per line.

Vertical Line Spacing (center-to-

center):

4.24 mm (.1669 in); 6.0 lines per inch.

Printing Rate:

Up to 140 cps.

Paper:

Thermal (TI specification 972603).

Platen:

Friction feed.

1.7.2 Keyboard

Code:

ASCII or CCITT; 128 codes generated.

1.7.3 **Modem**

Compatibility: Racal-Vadic 3400 or Bell 103-type or 212*-type data sets

Mode: Originate only (785)

Answer/Originate (787)

Modulation: Racal-Vadic 3400 and Bell 212-type

Differential Phase Shift Keying (DPSK)
Bell 103-type: Frequency Shift Keying (FSK)

Originate Mode

Transmit Carrier Frequencies: Racal-Vadic 3400: 2250 Hz

Bell 103-type: Mark = 1270 Hz

Space = 1070 Hz

Bell 212-type: 1200 Hz

Receive Carrier Frequencies: Racal-Vadic 3400: 1150 Hz

Bell 103-type: Mark = 2225 Hz

Space = 2025 Hz

Bell 212-type: 2400 Hz

Answer Mode

Transmit Carrier Frequencies: Racal-Vadic 3400: 1150 Hz

Bell 103-type: Mark = 2225 Hz

Space = 2025 Hz

Bell 212-Type: 2400 Hz

Receive Carrier Frequencies: Racal-Vadic 3400: 2250 Hz

Bell 103-type: Mark = 1270 Hz

Space = 1070 Hz

Bell 212-type: 1200 Hz

Transmit Level

Permissive Connection: -10 dBm, fixed for all methods

Programmable Connection: 0 to -12 dBm, per data jack

Optional Acoustic Coupler: Bell 103-type = -14 dBm

Bell 212-type = operation not recommended

Racal-Vadic 3400 = -17 dBm

Receiver Sensitivity

Direct Connect: All types = -45 dBm

Acoustic Coupler: Bell 103-type = +0 to -40 dBm depending upon quality of telephone

handset and communications line(s)

Bell 212-type = operation not recommended

Racal-Vadic 3400 = +0 to -32 dBm depending upon quality of

telephone handset and communications line(s)

^{*}Bell 212-type not available on 785.

Section 2

Equipment Installation

2.1 PRELIMINARY CHECKOUT

The 780 terminals are self-contained, requiring no auxiliary equipment for normal operation.

After unpacking, visually inspect the data terminal before applying power. Check for obvious shipping damage. Check that all keyboard keys operate freely. Before attempting to use the terminal, read the following cautions.

CAUTIONS

DO NOT operate printer without paper for extended periods or damage may result to the printhead.

DO NOT operate the terminal outside the specified operating range of 10°C to 40°C (50°F to 104°F) or malfunctions may occur. If the terminal has been stored outside this range, allow it to sit for a minimum of 30 minutes before applying power.

2.2 POWER CONNECTION

The terminals are designed to operate from either domestic or foreign power distribution systems. The power supply is configured at the factory and is adjusted by means of jumper(s) on the main PWB. The terminal operates properly when the input voltage is within the following limits:

Nominal Voltage:

120 Vac

90 to 134 Vac

230 Vac

187 to 264 Vac

Input Frequency: 47 Hz to 450 Hz.

CAUTIONS

Check the label on the rear of the terminal to determine the correct voltage required for your terminal. Ensure that the voltage at the wall outlet matches the terminal voltage rating listed on the label.

It is preferred that the terminal be plugged into a three-wire earth-grounded ac outlet. If an extension cord is required, it is preferred that it be of the three-wire type containing an earth-ground conductor.

2.3 COMMUNICATIONS INTERFACE

The terminals interface with numerous devices via at least one of three methods. All terminals have a communications interface connector (25-pin connector) located on the rear of the terminal that includes circuits for EIA and TTY (DC) current loop operation.

NOTE

The communications interface connector is not a standard EIA port since the TTY current loop circuits are included in the connector.

The 785 includes an acoustic-coupler interface located on the rear deck of the case. The 787 utilizes a direct-connect interface located below the 25-pin connector and, as an option, the 787 may also have an acoustic-coupler interface. The various communications interfaces are shown in Figure 2-1.

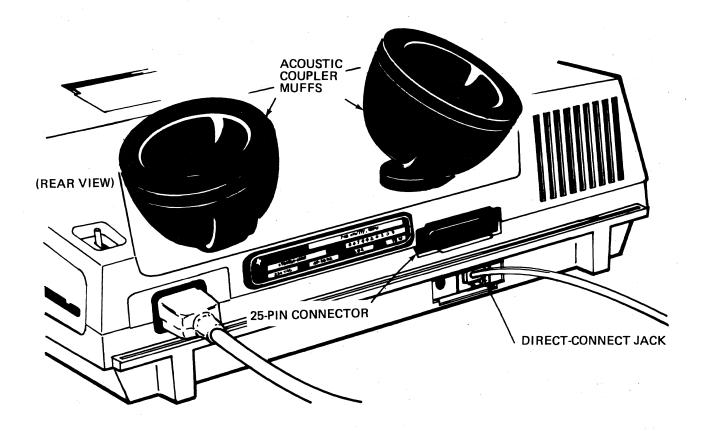


Figure 2-1. Communications Interfaces

A functional description of the interface signals present in the communications interface connector is presented in Table 2-1, and pin assignments are listed in Table 2-2.

Table 2-1. Interface Signals

Protective Ground (AA)—This lead is connected to the terminal frame and the earth-ground conductor of the power cord.

Signal Ground (AB)—This lead is tied to the dc ground of the terminal for all interface signals.

Transmitted Data (BA)—This lead conveys signals from the terminal data transmitted output to the data set transmitted circuitry. It is held to a MARKING condition unless data or BREAK signals are being transmitted.

Received Data (BB)—This lead conveys signals from the external data set receiver to the terminal data receiver input.

Request To Send (CA)—This line is used by the terminal to control the transmitter carrier of the data set. For full-duplex operation, this lead is held ON at all times that circuits CC (data set ready) and CD (data terminal ready) are ON. For half-duplex operation, this lead is held ON when the terminal is ONLINE and in the transmit mode.

Clear To Send (CB)—This line is switched on by the data set to indicate to the terminal that the data set is ready to transmit. The terminal will not attempt to transfer data across the interface when this line is off.

Data Set Ready (CC)—This signal line is controlled by the data set. The terminal will not attempt to receive or transmit data across the interface when this line is off.

Data Terminal Ready (CD)—This signal line is turned on by the terminal to indicate that it is ONLINE and ready to initiate or answer a data call. It is switched OFF momentarily during a terminal automatic disconnect sequence and is held OFF when the terminal is OFFLINE.

Ring Indicator (CE)—An ON condition on this circuit indicates that the data set is receiving a ringing signal from the communications line. The terminal monitors this circuit and uses the information presented to make a determination of whether it is in answer or originate mode for purposes of ABM autotrigger.

Received Line Signal Detector (CF)—This line is switched ON by the data set to indicate that it is receiving a valid carrier signal from the remote data set. The terminal will not accept data from the interface if this signal is OFF. This line will be regarded as ON when it is open (floating) to permit successful operation with data sets which do not provide circuit CF.

Data Signal Rate Selector (CH)—This signal is used by the terminal to select the transmit and receive data rate when used with Bell-type-212 data sets equipped with the originate speed select option. The terminal will hold circuit CH ON when configured for operation at speeds greater than or equal to 1200 bits per second (bps) or for 300/1200 auto-select, and will hold it OFF for all other data rates.

Secondary Request To Send (SCA)—This line is held ON by the terminal when it is ready to receive data and configured for half duplex with reverse channel operation (receive or idle mode). This signal will be switched OFF when the terminal enters the transmit mode. For this duplex mode, circuit SCA is the complement of circuit CA. This signal line will be controlled for other sequences of operation as described later in this manual.

Secondary Received Line Signal Detector (SCF)-This signal has a dual function, depending on the external data set. (1) It is held ON by 202 series data sets to indicate receipt of a valid reverse channel carrier from a remote data set. When the terminal is configured for half duplex with reverse channel operation, it will not transmit data until circuit SCF is ON and will treat any loss of SCF for 100-125 msec. or longer as a BREAK signal. (2) Bell 212 compatible data sets use this signal as a baud rate indicator, holding the signal ON for 1200 bps and OFF for 103 series operation. The terminal, when configured for 300/1200 auto-select, will adjust its data transmission rate in accordance to the status of circuit SCF. An open circuit SCF will be detected as an OFF condition. Detection of an ON condition will result in automatic selection of 1200 bps, and detection of an OFF condition will result in the automatic selection of 300 bps.

For more information concerning communications interconnections, refer to Appendix E.

Table 2-2. Pin Assignments

Pin	RS-232-C Circuit	Current Loop	Function
1	AA		Protective Ground (PG)
2	ВА		Transmitted Data (XMT)
3	BB		Received Data (RCV)
. 4	CA		Request to Send (RTS)
5	СВ		Clear to Send (CTS)
6	CC		Data Set Ready (DSR)
. 7	AB		Signal Ground (SG)
8	CF		Received Line Signal Detector (DCD)
11	SCA		Secondary Request to Send
12	SCF		Secondary Received Line Signal Detector
13		`X1	TTY Transmitted Data (TTYXMTD)
14		X2	TTY Transmitted Data Return (TTYXMTD/R)
15	DB		Transmission Signal Element Timing
16		RL-1	TTY Receive Data (TTYRCVD)
17	DD		Receiver Signal Element Timing
18		RL-2	TTY Receive Data Return (TTYRCVD/R)
20	CD	İ	Data Terminal Ready (DTR)
22	CE		Ring Indicator (RI)
23	СН		Data Signal Rate Selector

2.3.1 EIA Operation

All terminals interface with external devices through the 25-pin connector located at the rear of the terminal. The Asynch/Sync Cable (TI Part No. 2207634) consists of a 25-pin mating connector at the terminal end and 25-pin male connector on the modem end. The following steps provide a general guideline for setup when using Bell-type 103, 113, 202, 212, and Racal-Vadic 3400 series data sets:

- Connect the interface cable (TI Part No. 2207634-0001 supplied with the terminal) between the interface connector on the back of the terminal and the data set.
- 2. Ensure that the communications method and speed are compatible with the data set being used.

- 3. Ensure that the parity is set to conform to the requirements of the system.
- 4. Set the terminal to the ONLINE Mode.

The terminal is now ready for operation with the data set.

2.3.2 TTY (DC) Current Loop Operation

All terminals interface with external devices through the communications connector located at the rear of the terminal. The TTY Cable (TI Part No. 2265871-0001) consists of a 25-pin mating connector at the terminal end and four spade lugs at the other end. Figure 2-2 illustrates the four-wire (full-duplex) and two-wire (half-duplex) current loop configuration.

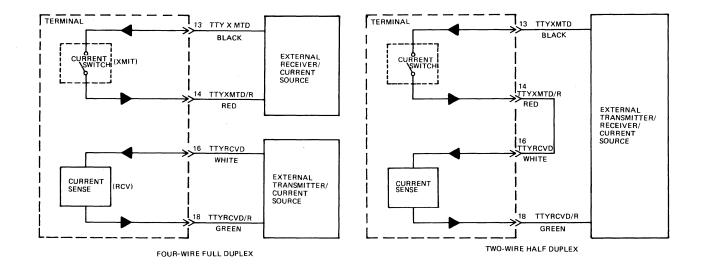


Figure 2-2. Current Loop Configuration

The following steps provide a general guideline for setup when using the current loop interface:

- Connect the current loop cable (TI Part No. 2265871-0001) between the interface connector on the back of the terminal and the external equipment.
- 2. Ensure that configuration *code* 16 (current loop) has been selected.
- Set the remaining configuration codes to comply with the requirements of the external equipment or system.
- 4. Set the terminal to the ONLINE Mode.

The terminal is now ready to communicate.

2.3.3 Internal Modem Operation

Models 785 and 787 are equipped with internal modems to provide communication over telephone lines. The modem in the 785 is a full-duplex, dual-speed, originate-only modem having an acoustic-coupler interface. The 787 has a full-duplex, dual-speed, answer/originate modem using a direct-connect interface.

2.3.3.1 Acoustic Coupler Interface Operation. The following steps provide a general guideline for

setup when using the acoustic coupler.

- Switch the terminal power ON.
- Ensure that the proper configuration codes are enabled. In the majority of applications, the standard default parameters may be all that are required.
- 3. Set the terminal to ONLINE.
- Pick up the telephone handset and dial the appropriate number; a high-frequency signal (answer tone) is heard when the call is answered.
- 5. As soon as the answer tone is heard, firmly insert the telephone handset into the acoustic-coupler muffs so that the cord is to the left of the terminal. The terminal will in turn transmit a data tone to the remote modem or acoustic coupler.
- When the connection is completed, the XMIT RDY, RCV RDY, and LINE RDY indicators light and the terminal prints CONNECTED.
- Begin communications according to your system's procedures.

NOTES

After prolonged operation the carbon particles in the telephone mouthpiece may settle, causing data errors. If this occurs, rap the handset several times against the palm of your hand.

Proper insertion of the handset in the muffs can make a significant difference in terminal operation. Ensure that the muffs fully encircle the earpiece and mouthpiece.

If the XMIT RDY and RCV RDY indicators begin flashing, communications have been lost and you must return to *Step* 4. This is indicative of the host modem not hearing us properly. If the message "connected" was printed, the terminal heard and responded to incoming carrier.

- When you are finished, terminate communications according to your system's procedures and set the terminal to LOCAL (the terminal prints DISCONNECTED).
- To hang up the telephone, remove the handset from the muffs by rolling it toward the front of the terminal and replace it in the handset cradle of the telephone.
- **2.3.3.2 Direct-Connect Interface Operation.** The following steps provide a general guideline for setup when using the direct-connect interface:
 - 1. Switch the terminal ON.

- Ensure that the proper configuration codes are enabled. In the majority of applications, the standard default parameters may be all that are required.
- Insert the cable provided with the terminal into the receptacle on the rear of the terminal and into the data jack on the wall.
- 4. Start the call initiation procedure using the *Dial Function*.
- When the connection is completed, the XMIT RDY, RCV RDY and LINE RDY indicators light and the terminal prints CONNECTED.
- Begin communications according to your system's procedures.

NOTE

If the XMIT RDY and RCV RDY indicators begin flashing, communications have been lost and you must return to *Step* 4.

- When you are finished, terminate communications according to your system's procedures.
- 8. Perform the call termination procedure (Command H). The terminal returns to LOCAL, prints DISCONNECTED, and after three seconds returns to the ONLINE Mode. A call can also be terminated by switching the terminal to LOCAL.

Section 3

Operation

3.1 OPERATING MODES

The 783, 785 and 787 terminals have three operating modes that are identifiable to the operator: LOCAL, ONLINE and COMMAND. The 781 terminal has two operating modes: LOCAL and ONLINE.

3.1.1 LOCAL

The ONLINE/LOCAL switch on the keyboard is a momentary contact switch that switches the terminal between the ONLINE and LOCAL Modes of operation. The LOCAL Mode is indicated when the LED adjacent to the switch is extinguished. In the LOCAL Mode, the terminal cannot communicate with external devices. While in the LOCAL Mode, the terminal receives command data and print data from the keyboard, and the printer can print keyboard data or report data. The 781 must be in the LOCAL Mode to change special configuration parameters.

3.1.2 ONLINE

In the ONLINE Mode, the terminal communicates with external devices through the communications interface. The keyboard and printer data is channeled through the communications interface. Command data or transmit data can be entered from the keyboard. The printer prints received line data or report data. Communications characteristics are determined by special configuration parameters entered from the keyboard when in the COMMAND Mode (783, 785 and 787). The ONLINE Mode is controlled by the ONLINE/LOCAL switch on the keyboard.

3.1.3 COMMAND

The COMMAND Mode allows the operator to change operating parameters, request reports, conduct special tests and initiate certain automatic functions. The terminal can be in either ONLINE or LOCAL Mode when the terminal is placed in the COMMAND Mode. In the 783, 785 and 787 the COMMAND Mode is entered by depressing the CMD key, while in the 781, the COMMAND Mode is entered when the CNFG or TEST key is depressed.

3.2 OPERATOR INTERFACE

The operator interface provides a way to communicate with the terminal and to other devices via the terminal. The 783, 785 and 787 are keyboard send-receive (KSR) terminals which use an operator's panel which is similar to a typewriter keyboard. The 781 is a receive-only (RO) terminal and uses a calculator-type keypad to input information.

3.2.1 KSR Operator's Panel

The KSR operator's panel is illustrated in Figure 3-1. The panel has 50 code-generating keys for generating all 128 ASCII codes. There are four keyboard mode control keys, six special function keys and one dual-position key for terminal control. The operator's panel also includes six light-emitting diode (LED) indicators for status reporting.

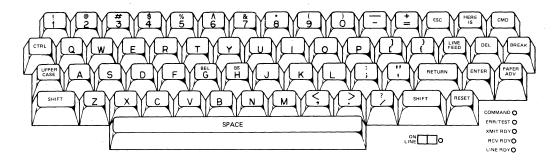


Figure 3-1. Operator's Panel

3.2.1.1 Keyboard Character Encoding. The code-generating keys include the alphabet, numerals, symbols, space, ESC, LINE FEED (except on Germany, Denmark/Norway and Sweden/Finland keyboards), DEL and RETURN. The characters generated in response to the depression of these keys are governed by the positions of the four mode control keys. These keys are SHIFT(2), UPPER CASE and CTRL which control the operating mode of the keyboard as described below:

- Unshifted—No mode control keys depressed; lowercase letters, symbols and numerals are encoded. Figure 3-2 illustrates the characters generated by each key in the unshifted mode.
- Upper Case Only—UPPER CASE (alternate action) key depressed; all alphabetic characters a through z are encoded as ASCII upper case A through Z. The characters generated by each key when the UPPER CASE key is depressed are shown in Figure 3-3.
- Shifted—Either or both SHIFT keys depressed; uppercase letters and symbols are encoded. The characters generated by each key when depressing the SHIFT key are illustrated in Figure 3-4.
- Control—CTRL key depressed; ASCII control characters and the symbols \ \ \ \ \ \ are encoded. Figure 3-5 illustrates the control characters generated by each key.

When more than one mode control key is depressed, the following priority is maintained:

CTRL—Precedence over SHIFT and UPPER CASE,

SHIFT—Subordinate to CTRL; precedence over UPPER CASE.

UPPER CASE—Subordinate to CTRL and SHIFT.

Certain functions requiring the simultaneous depression of CTRL and SHIFT are described below:

CTRL/SHIFT/RESET—Clears the receive buffer.

CTRL/SHIFT/H—Generates a backspace.

The keys ESC, DEL, LINE FEED, RETURN and SPACE generate the same codes in all keyboard modes. All code-generating keys with the exception of ESC, DEL, and RETURN initiate automatic character repeat at 10 characters per second when switch depression exceeds 600 msec. Figures 3-2 through 3-5 illustrate the characters generated by the different keyboard modes. The Character Set Dot Matrix is located in Appendix C. The ASCII control characters are described further in paragraphs 3.5 and 4.1.3.

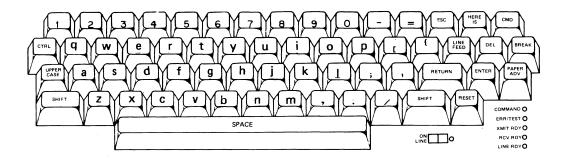


Figure 3-2. Keyboard (Unshifted)

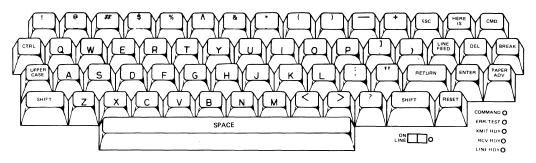


Figure 3-3. Keyboard (Shifted)

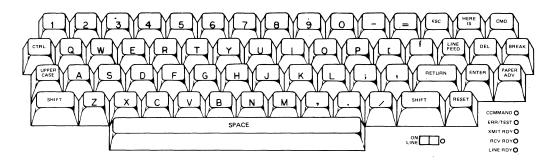


Figure 3-4. Keyboard (Upper Case)

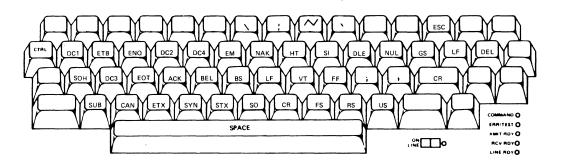


Figure 3-5. Keyboard (Control)

The terminal firmware recognizes foreign keyboards and their corresponding character sets. Each foreign character set is contained in an optional PROM. The foreign keyboards are illustrated in Appendix C.

3.2.1.2 Controls. Terminal control is facilitated by the use of one dual-position switch (ONLINE) and six unencoded special function keys (HERE IS, CMD, BREAK, ENTER, PAPER ADV, and RESET). The control keys function as described below:

ONLINE—Switches the terminal between ONLINE and LOCAL Modes of operation. A change from LOCAL to ONLINE results in Data Terminal Ready, DTR (EIA circuit CD) being switched ON, and line communications being enabled unless a nonoperational status exists. A change from ONLINE to LOCAL causes DTR to switch OFF, and line communications are disabled

HERE IS—Causes the following to happen:

ONLINE—Transmits the characters programmed in the ABM.

LOCAL—Prints the ABM message when the terminal is configured to local print ABM.

CONFIGure—Terminates the ABM or LTA programming sequence.

CMD—Causes the terminal to enter the COM-MAND Mode.

BREAK—Causes the following action depending on the communications mode:

Full Duplex—Depression of the BREAK key causes XMIT DATA (EIA circuit BA) to hold to a SPACING (ON)

condition for a minimum of 256 msec. If the depression exceeds 256 msec., the SPACING condition is maintained for the duration of the depression.

Half Duplex—In the transmit mode, the operation of the BREAK key is similar to full duplex. In the receive mode, the BREAK key has no function. However, if LTA recognition is configured, and DCD (EIA circuit CF) switches OFF before LTA is received, then the depression of the BREAK key initiates the transition to the transmit mode.

Half Duplex with Reverse Channel-When in the receive mode, depression of the BREAK key causes EIA circuit SCA (Secondary Request to Send) to be switched OFF for 256 msec. or the duration of the depression, whichever is longer. RCVD DATA (EIA circuit BB) is monitored for received data until an LTA is received or DCD switches OFF. The following transition is to either transmit or idle mode depending upon whether or not LTA recognition is configured and DCD switches OFF before an LTA is received. Depression of the BREAK key initiates transition to the transmit mode.

DC Current Loop—Depression of the BREAK key causes the transmit circuit to issue the BREAK condition for 256 msec. or for the duration of the key depression, whichever is longer.

3.2.1.3 Indicators. Six LED indicators are adjacent to the keyboard on the KSR operator's panel as shown in Figure 3-6. These indicators provide terminal status.

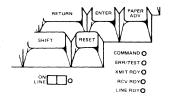


Figure 3-6. LED Indicators (783, 785, 787)

- ONLINE-This unlabeled indicator, adjacent to the ONLINE switch, is illuminated when DTR (EIA circuit CD) is ON and extinguished when DTR is OFF.
- COMMAND-This indicator, illuminated after the depression of the CMD key, indicates the terminal is in the COMMAND Mode. It remains illuminated until the COMMAND Mode is terminated.

Flashing of the COMMAND Mode indicator indicates that a request to enter the COMMAND Mode is pending. Flashing continues until the COMMAND Mode is entered.

ERR/TEST-This indicator has two functions. When flashing, the terminal has identified a reportable error or, when illuminated continuously, the terminal is in the TEST Mode. Depressing RESET extinguishes the indicator and prints the ERROR report. When both conditions exist

simultaneously, TEST has precedence over ERRor. Once TEST has been terminated with RESET, however, the ERRor condition is displayed until RESET is pressed.

- XMIT RDY-This indicator indicates the status of the terminal transmit capability as follows:
 - ON—DTR, DSR, RTS, and CTS (EIA circuits CD, CC, CA and CB) and SCF (if required) are ON.
 - FLASHING—DTR, DSR, and RTS (EIA circuits CD, CC, and CA) are ON but CTS (EIA circuit CB) or SCF (if required) is OFF.
 - OFF-circuit DSR, DTR or RTS is OFF.
- RCV RDY-This indicator indicates the status of the terminal receive capability in conjunction with DCD (EIA circuit CF) as follows:
 - ON—DTR, DSR, and DCD are ON in the receive mode.
 - FLASHING—in the receive mode and DCD is OFF.
 - OFF-not in the receive mode.

LINE RDY-This indicator indicates the status of DSR (EIA circuit CC) as follows:

ON-DTR and DSR are ON.

FLASHING—in the COMMAND Mode and DSR is ON.

OFF-DSR is OFF.

3.2.2 RO Operator's Panel

The RO operator's panel is shown in Figure 3-7. The panel includes the calculator-type keypad which has 16 code-generating keys (numerals 0

through 9 and letters A through F), six terminal control keys, and three operator control keys. The operator's panel also includes four LED indicators for reporting terminal status.

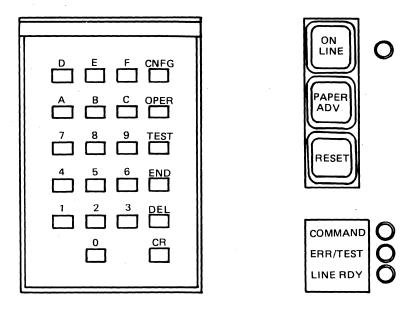


Figure 3-7. Operator's Keypad (781)

3.2.2.1 Keypad Character Encoding. The terminal uses the hexadecimal equivalent to generate all 128 ASCII characters. The ASCII characters are

encoded using a two-keystroke entry which represents the hexadecimal equivalent. Table 3-1 lists the ASCII/hexadecimal conversion codes.

Table 3-1. ASCII/Hexadecimal Conversion Codes

ASCII	CODE	ASCII	CODE	ASCII	HEX CODE	ASCII	HEX CODE	ASCII	HEX CODE	ASCII	CODE	ASCII	HEX CODE	AS	COD!	
NUL	00	BS	08	DLE	10	CAN	18	SPACE	20	(28	0	30	8	38	
SOH	01	HT	09	DC1	11	EM	19	!	21)	29	1	31	- 9	39	-[
STX	02	LF	0A	DC2	12	SUB	1A	"	22	*	2A	2	32		3A	١
ETX	03	VT	OB	DC3	13	ESC	1B	#	23	+	2B	3	33	;	3B	ł
EOT	04	FF	oc	DC4	14	FS	1C	\$	24	,	2C	4	34	<	3C	1
ENQ	05	CR	OD	NAK	15	GS	1D	%	25	-	2D	5	35	=	3D	١
ACK	06	so	0E	SYN	16	RS	1E	&	26		2E	6	36	>	3E	- 1
BEL	07	SI	0F	ETB	17	US	1F	L .	27	1	2F	7	37	?	3F	
ASCII	HEX CODE	ASCII	HEX	ASCII	HEX	ASCII	HEX CODE	ASCII	HEX CODE	ASCII	HEX CODE	ASCII	HEX CODE	AS	CII HEX	
ASCII @		ASCII H		ASCII		ASCII X		ASCII		ASCII		ASCII		AS	COD	E
	CODE		CODE		CODE		CODE	<u> </u>	CODE	-	CODE		CODE	╟	78	E
@	CODE 40	н	CODE 48	P	CODE 50	x	CODE 58	-	CODE 60	h	CODE 68	р	CODE 70	×	78 79	Ε
@ A	40 41	H	48 49	P Q	50 51	X	58 59	a	60 61	h	68 69	р	70 71	×	78 79	Ε
@ A B	40 41 42	H	48 49 4A 4B 4C	P Q R	50 51 52	X	58 59 5A	a b	60 61 62	h i j	68 69 6A	p q r	70 71 72	×	78 79 7A	Ε
@ A B C	40 41 42 43	H I K	48 49 4A 4B 4C 4D	P Q R S	50 51 52 53	X	58 59 5A 5B	, a b c	60 61 62 63	h i j	68 69 6A 6B 6C 6D	p q r	70 71 72 73	×	78 79 7A 7B 7C 7D	Ε
@ A B C D	40 41 42 43 44 45 46	H J K L	48 49 4A 4B 4C 4D 4E	P Q R S	50 51 52 53 54	X	58 59 5A 5B 5C	, a b c	60 61 62 63 64	h i j k	68 69 6A 6B 6C 6D 6E	p q r s	70 71 72 73 74 75 76	x 3 2 2 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	78 79 7A 7B 7C 7D 7E	Ε
@ A B C D	40 41 42 43 44 45	H I J K L	48 49 4A 4B 4C 4D	P Q R S T	50 51 52 53 54 55	X Y Z [\	58 59 5A 5B 5C 5D	, a b c	60 61 62 63 64 65	h i j k l	68 69 6A 6B 6C 6D	p q r s t	70 71 72 73 74 75	X 2	78 79 7A 7B 7C 7D 7E	Ε

3.2.2.2 Controls. Terminal control is facilitated by the use of three unencoded special function keys: ONLINE, PAPER ADVance, and RESET.

ONLINE-Switches the terminal between ONLINE and LOCAL Modes of operation. A change from LOCAL to ONLINE results in DTR (EIA circuit CD) being switched ON and line communications being enabled. A change from ONLINE to LOCAL causes DTR to switch OFF and line communications are disabled.

PAPER ADV-Causes paper to feed continuously at a rate of 33 msec. per linefeed. On the 781 only, when the terminal is in the LOCAL Mode, the printhead will also slew to column 1.

RESET-Causes the following action in order of priority:

- 1. Terminate a TEST in progress.
- 2. Cancel COMMAND Mode.
- 3. Clear ERRor condition indicator.

3.2.2.3 Indicators. Four red LED indicators are adjacent to the keypad as shown in Figure 3-8. These indicators are described below:





Figure 3-8. LED Indicators (781)

ONLINE-This unlabeled indicator, adjacent to the ONLINE switch, is illuminated when DTR (EIA circuit CD) is ON and extinguished when DTR is OFF.

COMMAND-This indicator, illuminated after the depression of the CNFG or TEST key, indicates the terminal is in the COM-MAND Mode. It remains illuminated until the COMMAND Mode is terminated.

> Flashing of the COMMAND Mode indicator indicates that a request to enter the COMMAND Mode is pending. Flashing continues until the COMMAND Mode is entered.

ERR/TEST-This indicator has two functions. When flashing, the terminal has identified a reportable error or when illuminated continuously, the terminal is in the TEST Mode. Depressing RESET extinguishes the indicator and prints the ERROR report. When both conditions exist simultaneously, TEST has precedence over ERRor. Once TEST has been terminated with RESET, however, the ER-Ror condition is displayed until RESET is pressed.

LINE RDY-This indicator indicates the status of the DSR (EIA circuit CC) as follows:

ON-circuit DSR is ON.

FLASHING-in the COMMAND Mode and circuit DSR is ON or DCD is OFF.

OFF-circuit DSR is OFF.

3.3 TERMINAL CONFIGURATION

Configuration parameters such as data transmission rate, character parity, and communications mode are configurable selected character sequences entered from the keyboard (Models 783, 785, and 787) or the operator keypad (Model 781) when the terminal is in the CONFIGure Mode.

3.3.1 Configuration Entry

The terminal can be configured in either the ONLINE Mode or LOCAL Mode. The CONFIGURE Mode is entered in the following manner:

Model 781

Depress CNFG

Models 783, 785, 787

Depress CMD (the terminal responds with a CR, LF and the CMD prompt is printed) followed by either C or c.

The terminal enters the CONFIGure Mode and the following occurs:

- 1. A report of the current terminal configuration is printed.
- 2. Parameter change(s) are solicited by the prompt "CR LF?".
- Valid parameter entry results in an immediate update to the operating parameter set, and a new CRC number is generated. The CRC is used to check for a battery or CMOS RAM failure.
- Parameter changes are accepted until the CONFIGure Mode is terminated by pressing ENTER (783, 785, 787), OPER (781), or RESET (all terminals).
 - ENTER and OPER cause the terminal to print the updated configuration report and terminate the COMMAND Mode.

 RESET terminates the COMMAND Mode without printing the configuration report.

The three types of configuration parameters are: on-off, mutually-exclusive multiple-choice (one per set), and special program commands. Parameters are entered, changed or deleted by the following methods:

On-Off. These parameters are selected by keying in the selected two- or three-digit code and pressing RETURN or CR (781). A previously selected parameter is disabled by typing its two- or three-digit code and pressing the DELete key. As a digit is typed, it is printed by the printer. If more than two digits are entered before pressing RETURN (CR), the last three are validated. A valid two- or three-digit entry is signified by a short tone and the printing of the printable representation of the terminating control character immediately after the last digit entered. The operating parameters are also updated. An invalid entry results in a long tone and the printing of a question mark immediately after the last digit and no update to the operating parameters. Table 3-2 lists the ON-OFF configuration codes.

Table 3-2. On-Off Configuration Codes

Code	Me	aning						
61 62 63 64 65 66	Line Control—Any Number Enable Failsafe Disconnect Disconnect on Receipt of EOT Disconnect on Receipt of DLE EOT Disconnect on Paper Out or Print Inhibi Enable No Activity Disconnect Ignore LTA Characters (202)	t Cond	lition					
72 73 74	Transmission Control—Any Number Enable Print of ABM Contents (Local H Enable ABM Autotrigger on Answer Enable ABM Autotrigger on Originate	ere Is	or 82)					
82 83 84 85 86 87 94 95	Terminal Control—Any Number Enable Local Copy of Transmitted Data Enable Communication Line Ready/Bus Do "New Line" on Receipt of LF Do "New Line" on Receipt of CR Transmit CR LF when "Return" is depr Print All Control Characters Enable Column 72 Bell Tone—Keyboard Enable Form Feed (6 LF and a CR)	sy Repo						
		DEF	785 STD	ОРТ	DEF	7 STD	87 OPT	NOTE
131	Enable Tone Dial E		3.3			3.3	х	1
132	Enable Equalizers Enable RDLB	X	x		X	х		
134 135	Enable RDLB Data Enable loss of short carrier disconnect		x x			X X		

Note:

1. Parameter 131 is valid only if parameter 101 is set.

DEF = Default parameter

 $\mathsf{STD} \ = \ \mathsf{Parameter} \ \mathsf{can} \ \mathsf{be} \ \mathsf{enabled} \ \mathsf{if} \ \mathsf{modem} \ \mathsf{is} \ \mathsf{installed}$

OPT = Parameter can be enabled if option is installed

Multiple Choice. These parameters are divided into subsets that require exactly one parameter per subset to be selected at any given time. The parameters are changed by typing the corresponding two- or three-digit code and pressing RETURN or CR (781). Entry of the

new parameter automatically replaces the old parameter in the subset. Validation and reporting of validation are the same as previously described for the on-off parameters. Table 3-3 lists the multiple-choice configuration codes.

Table 3-3. Multiple-Choice Configuration Codes

Code	м	eaning				-		
	Configuration Set Selection							
09	Install Default Configuration Set							1
	Communications Mode—One Only							
11	External Data Set 202 (Half Duplex)							
12	External Data Set 202 with Reverse Ch	annel (I	Half Du	iplex)				
13	External Data Set 103, 113, 212, 3400 (•	•			
14	External Direct Wire - Reverse Channel			(781 o	nly)			
15	External Direct Wire - Reverse Channel				•			
16	DC Current Loop		•					
17	Internal Option (3400, 212, 103)							
18	DTR On = Ready (781 only)							
	Transmission Rate							
21	110 bps (10 Char/Gec)							
22	200 bps							
23	300 bps (30 Char/Sec)							
24	600 bps							
25	1200 bps (120 Char/Sec)							
26	2400 bps—Console							
28	9600 bps—Console							
29	300/1200 bps—(Use with Dataset; Aut	ospeed	or Int	ernal N	/lodem	on 78	5. 787	
31 32 35 36 37 38	Parity Odd Parity Transmit, No Check Receiv Even Parity Transmit, No Check Receiv Odd Parity Transmit, Check Receive ar Even Parity Transmit, Check Receive a Mark Parity Transmit, No Check Receive Space Parity Transmit, No Check Receive	ve nd Repo nd Rep ve			P arana nama			
		1	785		}		787	
		DEF	STD	ОРТ	DEF	STD	ОРТ	NOTE
101	Direct Connect Interface				х			2
102	Acoustic Coupler Interface	X					X	
111	Auto	x			×			1
112	103	1	Х		}	Х		
113	212	1				Х		
114	3400		×			х	{	
121	Answer/Orig				×			1
122	Answer Only]	1		Х		1
123	Originate Only	X		1		Х		1
		1		l	l	L	L	

Notes:

1. If parameter 111 is set, parameters 121 through 123 are irrelevant.

DEF = Default parameter

STD = Parameter can be enabled if modem is installed

OPT = Parameter can be enabled if option is installed

2. Parameter 131 is valid only if parameter 101 is set.

Program Commands. These commands program the line turnaround (LTA) character(s) (783, 785, and 787) for half-duplex operation, and the answerback memory (ABM) contents (all terminals). Table 3-4 lists the program commands.

Table 3-4. Program Commands

Code	Meaning
60	Program Line Turnaround
70	Character(s) — 202 Only
/0	Program Answerback Memory

LTA characters are programmed by typing the enable sequence 60 followed by RETURN followed by up to three ASCII characters. All program characters are bracketed by quotation marks with the first being generated automatically before the first program entry and the second upon termination of the program sequence. The terminal prints the command characters and the program characters while the control characters are replaced by their printable representation. The programming sequence is terminated automatically with the entry of the third character or by pressing the HERE IS key. A previously programmed LTA can be deleted by typing the following: 60 RETURN HERE IS.

The ABM is programmed by typing the enable seguence of 70 followed by RETURN (CR) followed by up to 32 ASCII characters (64 keystrokes using the hexadecimal equivalents in the 781). Configuration parameter 70 is not valid if an optional ABM PROM is installed. All command and program characters are printed as they are entered, whereas control characters are replaced by their printable representation. The program character sequence is automatically bracketed by quotation marks and is terminated automatically after 32 ASCII characters are entered or the HERE IS or END (781) key is pressed. The command characters are validated in the same manner as previously described for the on-off parameters. The previous contents of the ABM are erased by the key sequence: 70 RETURN HERE IS (70 CR END).

In the 783, 785 and 787, errors can be corrected prior to the termination of either of the program sequences by typing CTRL/SHIFT/H (unassigned). Each CTRL/SHIFT/H typed deletes the last program character entered. The first CTRL/SHIFT/H typed causes the terminal to line-feed and backspace. Any subsequent CTRL/SHIFT/H typed causes only a backspace. The characters deleted by typing CTRL/SHIFT/H are replaced by typing from the keyboard.

3.3.2 Configuration Report

The printed configuration report displays the current configuration parameters of the terminal. The report includes the contents of the LTA (not applicable on 781) and ABM unless prohibited by configuration parameters. The configuration report is in the following format:

CONFIG: C1;C2;C3;...CN M1;M2;M3;...MN ABM:'''' LTA:''''

where C1 through CN are the enabled two-digit parameters listed in ascending sequence, and M1 through MN are the enabled three-digit internal modem configuration parameters listed in ascending sequence. The modem configuration parameters are applicable to the 785 and 787 terminals.

The absence of either ABM or LTA characters between the quotation marks indicates the absence of any ABM or LTA message. A protected ABM message is indicated by the following report:

ABM: (PROTECTED).

If LOCAL printing of the ABM (CONFIG parameter 72) is not enabled, the following message is printed if an ABM is being stored:

ABM: (MASKED).

Control characters in the ABM or LTA sequences are indicated by their printable representation.

3.4 OPERATING STATUS

The operating status of the terminal is maintained and conveyed to the user via the visual and audible indicators and the printed report.

3.4.1 Operating Error Codes

The terminal error codes tell the operator or service personnel of errors or problems that arise during the operation of the terminal. The error codes are listed in Table 3-5.

Table 3-5. Error Codes

· 1
·
n modem)
data)

3.4.2 Audible Status

The terminal produces an audible tone to provide information concerning completion of terminal activities. Two different types of tones are used:

- A short tone of 80-100 msec. signifies completion of a normal operation.
- A long tone of one second signifies that an error or abnormal operating condition exists.

Table 3-6 explains the conditions that cause the audible tone to be sounded.

Table 3-6. Audible Tone Signals

Signal	Explanation		
SHORT or or or or	 A keyboard entry has caused the carriage to pass through column 72 (i.e., exit column 72, when configured in code 94) ASCII BEL character has been received A keyboard command has been accepted Command execution has been completed A test has been completed successfully 		
LONG or	A new error status code has been activated An invalid keyboard entry has been detected		

3.4.3 Automatically Printed Status Reports Reports are printed automatically when certain

functions occur. Table 3-7 displays the format of the printed status reports.

Table 3-7. Printed Status Reports

Printout	When Generated	
78X	Completion of power-up routine or Test 1	
ERRORS: S1;;SN	When depression of reset extinguishes the error indicator	
CONNECTED	When online and a communication link is established (CC+(CB or CF))	
DISCONNECTED	When the terminal completes a disconnect sequence	

Notes:

- 1. All printouts are bracketed by CR LF.
- 2. S1-SN are enabled error status codes (paragraph 3.4.1).
- 3. For additional automatic reports, see Section 6.
- 4. X in 78X is 1, 3, 5 or 7.

3.4.4 Online Reporting

The terminals are capable of transmitting configuration and error status to remote systems. The report and request sequence is shown in Table 3-8.

3.5 CONTROL FUNCTIONS

The terminal is capable of transmitting all 33 control characters defined by the USASCII code; however, only a limited number of these

Table 3-8. Transmitted Reports

Report	Request Sequence	Response
CONFIG	ESC[c	ESC[XXX;C1;C2;;CNcLTA
ERROR	ESC[n	ESC[XXX;S1;S2;SNnLTA or ESC[XXX;nLTA (NO ERRORS)

Notes:

- 1. Requests will be honored from the line only.
- 2. XXX is the formal terminal identifier (e.g., Model 783 is XXX = 783).
- 3. LTA is the first programmed line turnaround character if required. (LTA only if in half duplex with LTAs.)
- C1—CN are the enabled configuration parameters. The report does not include ABM data or second and third LTA characters if programmed.
- 5. S1-SN are the existing error codes.

3.4.5 Operator Reference Cards

Information concerning the operation of the terminal is provided in the form of operator reference cards located below the terminal paper door. The information provided on the cards includes the following:

- Configuration programming instructions.
- Configuration parameter codes.
- List of error codes.
- Call initiation/termination procedures for internal modem/DAA (787 only).
- Control characters keyboard location.
- Report format instructions.
- Test mode instructions.
- Paper loading instructions.
- ASCII/hexadecimal conversion table (781 only).

characters are recognized. (The 781 can only transmit characters from the ABM.) The characters which are recognized or transmitted automatically are described below. All other control characters are transmitted only when entered from the keyboard or ABM and are ignored when received.

- BS—Backspace. Moves the printhead one character space in the reverse direction. Does not modify any character previously stored in the receive buffer. Generates no action if the printhead is at the left margin.
- CR—Carriage Return. Moves the printhead to the left margin when printing incrementally or initiates printing of the next line in the bidirectional mode. CR advances the paper one line space if received when the terminal is configured to perform "new line" on receipt of CR (i.e., code 85). RETURN causes a CR LF to be transmitted if the terminal is so configured (i.e., code 86).

- LF—Line Feed. Advances the paper one line for each key depression. Receipt of LF causes a carriage return function as well if the terminal is configured for "new line" on receipt of LF (i.e., code 84).
- BEL—Bell. Sounds audible tone.
- DC1—Device Control 1. DC1 is transmitted by the terminal to indicate "buffer ready" if the associated READY/BUSY function is configured (i.e., code 83).
- DC3—Device Control 3. DC3 is transmitted by the terminal to indicate "buffer full" if the associated READY/BUSY function is configured (i.e., code 83).
- ENQ—Enquiry. Receipt triggers the ABM if programmed.
- EOT—End of Transmission. Receipt causes a disconnect sequence to be completed if configured to do so; otherwise it is ignored (i.e., code 62).
- DLE—Data Link Escape. Reception of DLE followed by EOT initiates a disconnect sequence if configured to do so; otherwise it is ignored (i.e., code 63).
- ESC—Escape. Reception initiates escape sequence recognition from the communications line.

3.6 SELF-TESTS

The terminals provide automatic self-test functions to verify correct terminal operation. Two types of self-tests are built into the terminals: one is initiated during power-up and the other is initiated by the operator for maintenance purposes.

3.6.1 Power-Up Diagnostics

The terminal executes an internal memory check and a visual indicator check when switched on. Successful completion of the power-up diagnostic is indicated by the printing of the terminal model number. Errors are indicated by a long tone and the ERROR indicator, when possible. Failure of the self-test does not prohibit terminal operation.

A failure detected in the option buffer RAM automatically configures the terminal to operate with the largest available receive buffer.

If an error is indicated, the results of the diagnostic are obtained via the REPORT function when in the COMMAND Mode or by depressing the RESET key. Refer to subsection 3.7 for further discussion of the REPORT Mode.

3.6.2 Maintenance Diagnostics

The terminal provides many diagnostics for use by maintenance personnel when troubleshooting the terminal. In the 783, 785 and 787, the TEST Mode is entered from the COMMAND Mode by typing the valid syntax (T or t). In the 781, the terminal TEST Mode is entered by depressing the TEST key. The terminal TEST Mode indicator illuminates and the printer issues the prompt:

CR LF T#.

The terminal remains in the COMMAND Mode until a specific test is selected. An invalid response is indicated by a long tone and printing of the test prompt (T#). Depressing RESET causes the terminal to cancel the TEST and COMMAND Modes. Once a test is initiated, it is terminated automatically at the completion or by depressing RESET. RESET terminates the test and cancels the COMMAND Mode.

The maintenance diagnostics available for troubleshooting the terminal are described in detail in paragraph 6.2.2

3.7 REPORTS

In the 781, three reports are available: the configuration report, the error report, and the CR report. The configuration report is printed when the CNFG key is depressed, the error report is printed when an error exists and the RESET key is depressed, and the CR report is printed when Test 9 is entered.

In the 783, 785 and 787, three types of reports can be requested by the operator. The report feature of the terminal allows the operator to request the configuration report, error report and a CR report for use by service personnel. The reports are requested by entering the COMMAND Mode and typing the valid syntax (R or r) followed by ENTER. The printer issues the prompt:

CR LF R#

The terminal remains in the COMMAND Mode until a specific report is selected. An invalid response is indicated by a long tone and printing of the report prompt (R#). Once a REPORT is initiated, it

is terminated automatically at the completion.

The reports are described in greater detail in subsection 6.3.

Section 4

Communications

4.1 INTRODUCTION

The standard implementation of communication between the line and the data terminal is an ASCII, asynchronous, serial interface conforming to the electrical standard set by EIA RS-232-C and CCITT V24 standards. Communication to the line is possible only when the terminal is switched to the ONLINE Mode. The terminal also includes a DC current loop interface capable of full-duplex operation at speeds up to 1200 bits per second (bps).

4.1.1 EIA Transmission Rates and Distortion

The terminal is capable of transmitting and receiving data at transmission rates of 110, 200, 300, 600, 1200, 2400 and 9600 bps. The selection of the transmission rate is via the COMMAND Mode. The digital transmitter and receiver conform to the distortion limits listed in Table 4-1.

4.1.2 EIA Interface Signal Levels

The exchange of digital data between the terminal and an external device consists of a series of logic ONEs and ZEROs. A logic ONE, called a MARK, is indicated by a negative voltage between -3 and -25 volts. A logic ZERO, called a SPACE, is indicated by a positive voltage between +3 and +25 volts. In summary, a positive voltage on a control line indicates the ON condition, but a positive voltage on a data line represents a SPACE or logic ZERO. A negative voltage on a control line indicates the OFF condition, but on a data line a negative voltage represents a MARK or logic ONE. Table 4-2 shows the relationship between the control line and data line. The interchange voltage represents the data line, while the binary state represents the control line.

Table 4-1. Distortion Limits

Baud Rate	Maximum Allowable Received Distortion	Maximum Transmitted Distortion
110	49.0%	1.0%
200	49.0%	1.3%
300	47.7%	1.31%
600	47.7%	2.5%
1200	47.0%	2.54%
2400	46.0%	4.1%
9600	43.8%	10.1%

Table 4-2. EIA Signal Levels

	Interchange Voltage			
Notation	Negative	Positive		
Binary State	1	0		
Signal Condition	MARK	SPACE		
Function	OFF	ON		

4.1.3 Transmission Codes

The terminal generates all 128 codes of the USASCII code set as defined in ANSI Standard X3.4-1977. Table 4-3 lists the code structure for the ASCII code as interpreted by the terminal.

Table 4-3. ASCII Code System and Character Sets

8 7 6 4 3 2 1	0	0 0 0	0 0 1 0	0 0 1	0 1 0	0 1 0 1	0 1 1 0	0 1 1
0 0 0 0	NUL	DLE	SP	0	@	Р	. `	р
0 0 0 1	SOH	DC1	!	1	Α	Q	a	q
0 0 1 0	STX	DC2	"	2	В	R	b	r .
0 0 1 1	ETX	DC3	#	3	С	S	С	S
0 1 0 0	EOT	DC4	\$	4	D	Т	d	t
0 1 0 1	ENQ	NAK	%	5	E	U	е	u
0 1 1 0	ACK	SYN	&	6	F	٧	f	V
0 1 1 1	BEL	ETB	,	7	G	W	g	w
1 0 0 0	BS	CAN	(8	Н	X	h	×
1 0 0 1	HT	EM)	9	1	Υ	i	У
1 0 1 0	LF	SUB	*	:	J	Z	j	z
1 0 1 1	VT	//ÉŞÇ///	+	;	Κ	[k	
1 1 0 0	FF	FS	,	_ <	L	\	١	
1 1 0 1	CR	GS		=	M]	m	}
1 1 1 0	SO	RS	٠	>	N	^	n	~
1 1 1 1	SI	US	/	?	0	_	0	DEL

Printable Characters		Online Report Control
Printer Control Characters		
Codes Generated and Transmitted I	by the termin	nal

ASCII CONTROL CHARACTERS (From USA Standards Institute Publication X3.4-1977)

ACK	acknowledge	EM	end of medium	NAK	negative acknowledge
BEL	bell	ENQ	enquiry	NUL	null
BS	backspace	EOT	end of transmission	RS	record separator
CAN	cancel	ESC	escape	SI	shift in
CR	carriage return	ETB	end of transmission block	SO	shift out
DC1	device control 1	ETX	end of text	SOH	start of heading
DC2	device control 2	FF	form feed	STX	start of text
DC3	device control 3	FS	file separator	SUB	substitute
DC4	device control 4 (stop)	GS	group separator	SYN	synchronous idle
DEL	delete (also called RUBOUT)	HT	horizontal tabulation	US	unit separator
DLE	data link escape	LF	line feed	VT	vertical tabulation

^{*} not strictly a control character

4.1.4 Character Structure

Codes for transmitted and received data are in accordance with ANSI Standard for Character Structure and Parity Sense, X3.16-1976 and ANSI Standard for Bit Sequency of the USASCII code, X3.15-1976.

A transmitted or received character consists of a start bit (always a "0" or SPACING), seven data bits, a parity bit, and one or two stop bits (always "1" or MARKING). Two stop bits are transmitted at 110 bps and one stop bit at all higher data rates. Figure 4-1 illustrates the character serial data timing for 110 bps and 200 bps and above.

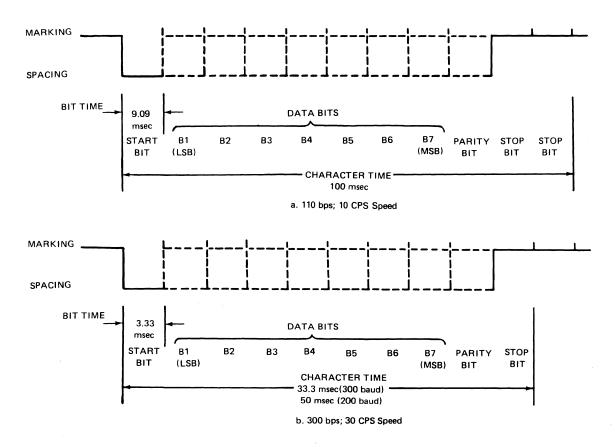


Figure 4-1. Serial Data Timing Diagram

The transmitted parity is programmable for ODD or EVEN parity, or no parity with the parity bit either always MARK or always SPACE. If ODD or EVEN parity is selected, the received data parity is specified to be checked for the same parity as transmitted data or not to be checked. If MARK or SPACE parity is specified for transmit, then receive parity is ignored. The selection is via the COMMAND Mode. If parity check is enabled, a receive character detected as having an invalid parity is replaced in the print data with a special parity error symbol (♠).

4.1.5 EIA Communications Interface

The standard interface between the terminal and the communications line conforms to the electrical requirements of EIA Standard RS-232-C and CCITT Standard V24. Table 4-4 lists the EIA/CCITT/TTY interface signals provided by the terminal.

The terminal also includes an operator-selectable DC current loop interface capable of operation in a full-duplex 20mA DC current loop (neutral only). In a neutral current loop, the flow of current indicates a MARK and a SPACE is indicated by no current flow. Some systems use bipolar current, where current flowing in one direction is a MARK and current flowing in the opposite direction is a SPACE. The neutral current loop is not compatible with the bipolar current loop, and damage to the terminal may result if it is connected to a bipolar system.

The current loop interface consists of separate transmit and receive circuits, electrically isolated from each other and from signal and chassis ground, such that they may be used separately in a four-wire half-duplex or full-duplex system or externally connected in series to form a two-wire half-duplex system. The current loop electrical characteristics are listed in Table 4-5.

Table 4-4. EIA/CCITT/TTY Interface Signals

Data Set		Circuit		News	
Connector Pin	TTY	EIA	ссітт	Name	
1 2 3 4 5 6 7 8 11 12 13 14	X1 X2 RL1	AA BA BB CA CB CC AB CF SCA/CH	101 103 104 105 106 107 102 109 120/111	Protective Ground Transmitted Data Received Data Request to Send Clear to Send Data Set Ready Signal Ground Received Line Signal Detector Secondary Request to Send/ Data Signal Rate Selector Secondary Received Line Signal Detector TTY Transmit Loop Input TTY Transmit Loop Return TTY Receive Loop Input	
18 20 22 23	RL2	CD CE SCA/CH	108.2 125 120/111	TTY Receive Loop Return Data Terminal Ready Ring Indicate Secondary Request to Send/ Data Signal Rate Selector	

Table 4-5. Current Loop Electrical Characteristics

Receive Circuit:

Nominal Current Threshold Current

Maximum Voltage Drop @ 20mA

Maximum Current*

Maximum Common Mode Voltage

20mA dc

 10 ± 5.5 mA dc

3Vdc

100mA dc

20mA dc

100mA dc

1V @ 20mA 0.5mA @ 50Vdc

50Vdc Either Continuous or Switched

Transmit Circuit:

Nominal Current Maximum Current*

Maximum Voltage Drop (MARK)

Maximum Leakage Current (SPACE) Maximum Voltage Rating (SPACE)

Maximum Common Mode Voltage

50Vdc Either Continuous or Switched

* The recommended maximum continuous current for safe operation is 80mA dc.

50Vdc

4.1.6 External Data Set Compatibility

The terminal is capable of interfacing to the communications line via the following data sets or their equivalents:

VADIC 3400 Series

Bell Series

103

113

202 C, D, S, and T

212 A, asynchronous mode only, high or low speed

The terminal provides both manual and automatic answer control of the external data set any time the terminal is ONLINE and no connection is currently in effect.

Refer to Appendix D for additional information on recommended data set options.

4.2 COMMUNICATIONS MODES

The following communications modes are selectable from the keyboard for use with external data sets (modems):

- Full duplex (i.e., code 13),
- Half duplex (i.e., code 11) and
- Half duplex with reverse channel (i.e., code 12).

One of two non-data set communications modes are also selectable from the keyboard for direct wire EIA applications:

- Full duplex with reverse channel transmit (SCA) ON for READY (i.e., code 14).
- Full duplex with reverse channel transmit (SCA) OFF for READY (i.e., code 15).

Also selectable from the keyboard is a current loop mode (i.e., code 16) for use with the current loop interface.

An additional configuration parameter is provided that enables half-duplex operation which does not require LTA characters for turnaround purposes (i.e., code 66).

It is possible to enable or disable local copy of the transmit data for any communications mode by selecting the proper configuration code from the keyboard when in the CONFIGure Mode (i.e., code 82).

4.2.1 Full-Duplex Data Set Operation

In the full-duplex mode, both the transmit and receive circuits are independent, permitting simultaneous bidirectional communications. If the local copy of the transmitted data is enabled, simultaneous communications will cause interleaving of the transmitted and received data on the printed page. Full duplex with local copy is not the same as half duplex.

For full-duplex communications, the terminal sets DTR (EIA circuit CD) ON when switched ONLINE and no disconnect is detected. Interface signal DSR must be switched ON by the data set before any data communications can take place. DTR must be ON in order for DSR to switch ON. The terminal switches ON RTS (EIA circuit CA) once DSR is ON. Once a valid carrier is established, the data set switches on DCD (EIA circuit CF) and CTS (EIA circuit CB). DSR and DCD enable the terminal to accept received data (RCVD DATA) when they are ON. DSR and CTS enable the terminal to transmit data to the line when they are ON. If circuit CTS switches OFF, any character being transmitted is completed, but no new characters are transmitted until circuit CTS switches ON.

Any characters entered from the keyboard while CTS is OFF are buffered in a FIFO memory (up to 16 characters) and are transmitted when CTS switches ON. If local copy is enabled, the buffered characters are printed when they are transmitted, not as they are entered. If more than 16 characters are entered while CTS is OFF, a one-second error tone sounds, the ERR/TEST indicator flashes, and the character is discarded. When the RESET key is depressed, the terminal will report error 25. This is repeated for every character entered that causes the FIFO buffer to exceed 16 characters, and only the first 16 characters are retained in the buffer for transmission. If DSR switches OFF, indicating a data set disconnect, any characters remaining in the transmit buffer are discarded.

If no special disconnect is enabled, the line is monitored for received data until either DCD or DSR switches OFF. With no disconnects enabled, DTR remains ON as long as the terminal is ONLINE. If DCD switches OFF in the middle of a received character, the terminal may misinterpret the character.

4.2.2 Half-Duplex Data Set Operation

The half-duplex mode of operation permits data communication to occur in only one direction at a time on the communications channel. Half-duplex operation includes a protocol that uses a line turn-around (LTA) character for line control. Up to three LTA characters are operator-selectable during the terminal configuration.

Initiation of communication in the half-duplex mode is on a contingency basis. When DSR switches ON, indicating the establishment of a connection, the terminal enters a special idle mode monitoring DCD. When DCD switches ON, the terminal enters the receive mode. If the ABM autotrigger is enabled (i.e., code 74), the terminal responds as described in paragraph 4.3.2.1 before automatically entering the transmit mode to transmit the contents of the ABM. If the autotrigger feature is OFF and DCD remains OFF, the terminal remains in the idle mode until the HERE IS key or a code-generating key is pressed on the keyboard. The terminal then enters the transmit mode to begin transmission of the keyed characters.

When entering the transmit mode, the terminal switches ON RTS and waits for CTS to switch ON before placing data on the transmitted data line (EIA circuit BA). The terminal remains in the transmit mode until one of the specified LTA characters is transmitted. If CTS switches OFF before transmission of the LTA, the terminal buffers keyboard characters in the FIFO memory as described in paragraph 4.2.1. Once the LTA character is transmitted, the terminal begins the transition to the receive mode. This transition includes switching OFF RTS. RTS can not change, however, until four milliseconds after the stop bit of the last transmitted character has cleared the terminal transmitter.

Once RTS is switched OFF, the terminal goes into the receive mode and waits for DCD to switch ON before monitoring the received data line (EIA circuit BB) for data. As long as DCD remains ON, the terminal monitors circuit BB for print and control data and/or a line turnaround character. On receipt of an LTA character, the terminal discontinues monitoring circuit BB and waits for DCD to switch OFF. When DCD goes OFF, the terminal enters the transmit mode and RTS is switched ON.

The previously described operation continues until a disconnect is initiated. A manual disconnect of the terminal from the data set is available to the operator at any time by setting the ONLINE/LOCAL switch to LOCAL. This action causes the terminal to switch OFF all control

signals that are provided to the data set and reset any communications timers that are active. All line communication remains disabled until the terminal is manually switched ONLINE. Other disconnect sequences are executed only if they are enabled as described in paragraph 4.3.2.

When a disconnect has been initiated by the terminal, all characters remaining in the transmit buffer are discarded, and all characters remaining in the received buffer are processed if possible (i.e., printable and printer control characters are executed and communication control characters are ignored).

4.2.3 Half Duplex with Reverse Channel Data Set Operation

Half duplex with reverse channel is the same as half duplex with the addition of circuits SCA and SCF (the reverse channel) for supervisory control information control. Operation of half duplex with reverse channel is the same as half duplex without reverse channel with the following exceptions.

Upon call establishment (i.e., recognition of DSR ON), the terminal enters the idle mode, where the EIA circuit SCA is switched ON to indicate the receiver is ready, and waits for DCD to switch ON or for a transmit request to be generated. The terminal is able to enter either the transmit or the receive mode from the idle mode. If DCD is ON prior to a requirement for transmitting, circuit SCA remains ON, and the terminal enters the receive mode from the idle mode and remains there until conditions for turning the line to the transmit mode are satisfied. If conditions for initiating the transmit mode are satisfied before DCD switches ON (i.e., keyboard or ABM interrupt), circuit SCA switches OFF and RTS switches ON and the terminal enters the transmit mode from the idle mode. If DCD does not switch ON and no transmit request exists during the initial idle mode, the terminal remains in the idle mode until disconnect timeout occurs (if enabled) or a requirement to enter the receive or transmit mode is generated.

Upon entering the transmit mode, initially or after LTA, the terminal monitors circuit SCF (secondary received line signal detector) for an ON condition before sending the first character.

If circuit SCF does not switch ON within eight seconds after circuit CA is switched ON, the terminal switches OFF RTS and switches ON circuit SCA, thus returning the terminal to the receive mode.

In the transmit mode, the terminal checks circuit SCF for an ON condition before sending each character. If circuit SCF switches OFF while the terminal is in the transmit mode, the terminal holds circuit BA to a MARK condition and initiates a 110-125 millisecond timeout. During the timeout and while circuit SCF remains OFF, keyboard data is buffered. If circuit SCF switches ON before the timeout completes, the terminal resumes transmission, sending first any characters that are stored in the transmit FIFO. If circuit SCF remains OFF for the duration of the timeout, the terminal reverts to the receive mode by switching OFF RTS and switching ON circuit SCA. Any characters remaining in the transmit FIFO at this time are discarded. Normal transitions from the transmit to the receive mode (i.e., after transmission of a line turnaround) are handled as previously described. After the transition to the receive mode is complete, circuit SCA is held ON as long as the terminal is in the receive mode unless a BREAK or BUSY operation occurs (see paragraph 4.3.3 or 4.3.4).

4.2.4 Half-Duplex Data Set Operation with No LTA (i.e., *code* 66)

This mode is specified with a separate configuration parameter in conjunction with the half duplex or half duplex with reverse channel parameter. The operation of this mode is similar to the mode it is used in conjunction with except that the LTA feature is not used in the data to initiate line turnaround and that any turnaround is followed by a transition to the idle mode. Initial transition from the idle mode is the same as for half duplex or half duplex with reverse channel (depending on which configuration parameter is enabled).

A transition from the receive to the idle mode is initiated by the terminal when in the receive mode and DCD goes to an OFF condition. The transition from the idle mode may be to either the receive or transmit mode. Transition from transmit to idle is initiated by depressing the ENTER key on the keyboard.

When operation is set to ignore line turnaround characters (i.e., *code* 66) and fail-safe disconnect operation is enabled (i.e., *code* 61), the loss of carrier timeout is automatically disabled by the terminal.

4.2.5 Non-Data Set Operation

Two special full-duplex modes are incorporated to simplify the use of the terminal in computer console and similar hardwired interfaces where no data set is used in the connection. Circuit SCA (secondary request to send) is used as a terminal READY/BUSY indicator. The difference between the two modes is that in one mode circuit SCA is held ON when the terminal is in a READY condition and held OFF when the terminal is BUSY. In the other mode, circuit SCA is held OFF when the terminal is in a READY condition and ON when the terminal is BUSY.

The operation of the terminal is basically the same as that described for full-duplex data set operation, except no timing constraints are placed on the communications interface. DTR and RTS are ON when the terminal is ONLINE and DSR and DCD must be ON in order for the terminal to receive data while DSR and CTS must be ON to transmit data. BUSY status is reported by circuit SCA when the terminal is in the LOCAL Mode, or cannot print, or to prevent the receive buffer to overflow.

4.2.6 DC Current Loop Operation

The terminal can be configured to operate in a DC current loop mode, via the DC loop transmitter and receiver circuitry. When ONLINE, the terminal is capable of full-duplex operation. READY/BUSY status reporting is possible via DC3/DC1 transmission (see paragraph 4.3.4). Keyboard BREAK is active when the terminal is ONLINE.

4.3 COMMUNICATIONS FEATURES

The terminal has many features which are useful when communicating with other devices. These features are enabled or disabled from the keyboard when in the CONFIGure Mode.

4.3.1 Answerback Memory (ABM)

A standard feature of the terminal is an Answerback Memory which can be programmed with a

message of up to 32 ASCII characters. If a message is programmed, it will be transmitted when the HERE IS key is depressed or when the ASCII character ENQ (enquiry) is received. The terminal is also capable of being configured to automatically transmit the contents of the answerback memory when a call is answered (i.e., code 73) or originated (i.e., code 74).

The standard ABM uses nonvolatile memory for storage and is operator-programmable. A non-alterable PROM for ABM storage is available as a hardware option.

4.3.2 Automatic Operation Control

The terminal has four configuration parameters which can be enabled or disabled from the keyboard that facilitate automatic operation of the terminal. These features are for data set communications modes and are as follows:

- ABM autotrigger on connection (code 73 or 74),
- Automatic disconnect character or character sequence (code 62 or 63),
- Fail-safe disconnect (code 61) and
- No activity disconnect (code 65).

Whenever an automatic disconnect is required in conjunction with one of the above features it is accomplished as follows:

- Recognition of additional data from the communications line and transmission to the line are inhibited.
- DTR is switched OFF by the terminal. After DSR is switched OFF for at least three seconds, DTR is switched ON by the terminal to re-enable communications.

NOTE

If DSR does not switch OFF, then DTR remains OFF until the terminal is switched manually to LOCAL and back ONLINE.

Data transmission and recognition are re-enabled when the next call is answered or originated and all appropriate control signals are present in the interface.

If no disconnect sequence is enabled, the terminal will monitor the line for data as long as the terminal is ONLINE and both DCD and DSR are ON. The terminal continues to transmit to the line as long as it is ONLINE and both DSR and CTS are ON. No automatic disconnect function is performed if none is enabled.

4.3.2.1 ABM Autotrigger. ABM autotrigger causes the contents of the answerback memory to be transmitted automatically as the first data whenever DTR is ON in accordance with the specific autotrigger parameter set (trigger on answer or trigger on originate) and the communications mode, as follows:

- Full duplex: The ABM is transmitted when DSR and CTS are turned ON by the data set and after a delay of 1.28 seconds.
- Half duplex: The ABM is transmitted as described for full duplex except that circuit DCD is checked when DSR switches ON. If DCD is OFF for 1.28 seconds, indicating the absence of a carrier, RTS is switched ON and the ABM is transmitted when CTS switches ON. If CF switches ON within 1.28 seconds after DSR switches ON, the terminal remains in the receive mode until the first line turnaround and the answerback autotrigger is cancelled for the current call.
- Half duplex with reverse channel: This mode is similar to half duplex with the exception that reverse channel (SCF) is switched on by the data set before the ABM is transmitted.

In both half duplex and half duplex with reverse channel, no automatic line turnaround on completion of the ABM is attempted unless the LTA character is part of the ABM message or unless operation with no turnaround is specified. If the terminal is configured to ignore LTA (*code* 66), the terminal returns to the idle mode upon completion of the ABM transmission.

4.3.2.2 Automatic Disconnect Character(s).

The terminal recognizes the ASCII control character EOT or the two-character sequence, DLE followed immediately by EOT, as disconnect commands when received from the communications line. Recognition of EOT (code 62) and/or DLE EOT (code 63) is enabled or disabled from the keyboard as part of the terminal configuration procedure.

4.3.2.3 Fail-Safe Disconnect. The fail-safe disconnect feature (*code* 61), when enabled via the configuration parameter, causes the terminal to disconnect from the transmission line when certain abnormal conditions occur. Disconnect is accomplished as previously explained in paragraph 4.3.2. The tone also sounds for one second and an "abnormal disconnect" error report is printed.

Fail-safe disconnect occurs under the following conditions according to the communications mode:

Full Duplex

- No carrier received (DCD) within 22 seconds after DSR switches ON (wrong number timeout).
- DCD is OFF for greater than or equal to eight seconds after having been ON (loss of carrier timeout).

Half Duplex

- No DCD within 22 seconds after DSR switches ON unless ABM autotrigger feature is enabled (wrong number timeout).
- DCD is OFF for greater than or equal to eight seconds after a line turnaround character is transmitted (loss of carrier timeout).
- DCD is OFF for greater than or equal to eight seconds after having been ON, unless DCD turn-off was preceded by receipt of a line turnaround character (loss of carrier timeout).

 CTS fails to turn ON within eight seconds after circuit RTS is switched ON (clear to send timeout).

Half Duplex with Reverse Channel

- 1. Same as number 1 for half duplex.
- 2. Same as number 2 for half duplex.
- DCD is OFF for eight seconds after having been ON, unless the turn-off of DCD was preceded by the turn-off of circuit SCA (BREAK transmitted by the terminal) or receipt of a line turnaround character (loss of carrier timeout).
- 4. Same as number 4 for half duplex.

NOTE

If the terminal is configured to ignore LTA, the loss of carrier timeout is automatically disabled for all half-duplex data set modes even if fail-safe disconnect is enabled.

- **4.3.2.4 No Activity Disconnect.** The no activity disconnect feature (*code* 65), enabled via the configuration parameter, causes the terminal to initiate an automatic disconnect from the communications line upon completion of three consecutive minutes during which no transmit or receive data activity is present on the communications line. Disconnect is accomplished as described in paragraph 4.3.2; the tone sounds for one second and an error is indicated.
- **4.3.2.5 Paper-Out Detection.** The terminal is provided with an optional paper-out detector which operates as follows:
 - 1. Error status code 12 is enabled.
 - Printing is inhibited at the end of the current print line.
 - 3. Error indication is reported to the operator.

- 4. If code 64 is enabled and 11, 12, 13, or 17 is selected, the terminal executes an automatic disconnect from the communications line. If code 64 is disabled, the terminal issues a "paper-out" signal to the line and remains connected. The signal format is as follows:
 - Full duplex: If code 83 is enabled, DC3 followed by a timed BREAK signal (256 msec. spacing condition) is transmitted on circuit BA. If code 83 is disabled, only BREAK is transmitted. If console operation (14, 15) is enabled, circuit SCA switches OFF until the condition is cleared.
 - Half duplex: No response is possible and the terminal goes to the idle mode following the receipt of the next line turnaround.
 - Half duplex with reverse channel: Circuit SCA is switched OFF and remains OFF until the condition is cleared.
- For all modes of communication, no ready signal is generated until the paperout condition is cleared.
- The error condition is not resettable as long as the detection circuitry senses the absence of paper.

Once the paper-out condition is physically cleared by loading paper, and the sensor detects the presence of paper, the RESET key initiates the following function:

Resumption of normal print and communications functions. The configured ready status is issued to the line (if the link is maintained) as soon as the receive buffer is ready to receive data based on the normal buffer ready limits following a busy condition.

4.3.3 Communication Line BREAKIn full-duplex or half-duplex transmit mode, circuit

BA is held to a SPACE condition for a minimum of 256 msec. when the keyboard BREAK key is depressed. If the key depression exceeds 256 msec., the SPACE condition is maintained for the duration of the key depression.

For half duplex with reverse channel, when in the receive mode, depression of the keyboard BREAK key causes circuit SCA to be switched OFF for 256 msec. or for the duration of the key depression. Circuit BB is monitored for receive data until an LTA is received or DCD switches OFF; then the transition to the transmit or idle mode, depending upon whether or not LTA recognition is enabled, is initiated. If LTA recognition is configured and DCD switches OFF before an LTA is recognized in the received data, the depression of the BREAK key initiates the transition to the transmit mode.

For half-duplex receive mode, no BREAK feature is possible. If LTA recognition is configured and DCD switches OFF before an LTA is recognized in the receive data, then the depression of the BREAK key initiates the transition to the transmit mode.

In the current loop mode, depression of the BREAK key causes the transmit circuit to issue BREAK or SPACE condition for 256 msec. or for the duration of the key depression.

4.3.4 Communication Line READY/BUSY Status Reporting

The terminal can be configured to indicate BUSY and READY conditions to the communications line (*code* 83) to prevent the receive data buffer to overflow at data rates higher than sustainable print rates. BUSY status is indicated when the buffer has fewer than 128 character positions available, and READY status is indicated when the buffer has 160 characters remaining.

READY/BUSY status is reported in the following manner, depending on the communications mode:

- Full-duplex data set: The terminal transmits DC3 when BUSY and DC1 when READY (only when configuration code 83 is enabled).
- Full-duplex non-data set: The terminal transmits DC3 when BUSY and DC1 when READY (only when configuration code 83 is enabled). Circuit SCA is OFF when BUSY and ON when READY when configuration code 14 is selected, or ON when BUSY and OFF when READY when configuration code 15 is selected.
- Half duplex: The terminal cannot report READY/BUSY status in this mode.
- Half duplex with reverse channel: Circuit SCA is OFF when BUSY and ON when READY (configuration code 83 enabled).

NOTE

The terminal enters the idle mode when DCD switches OFF if LTA is disabled. If DCD switches OFF while BREAK is active (SCA is OFF), the terminal enters the transmit mode. If DCD switches OFF while the terminal is BUSY (SCA is OFF), the terminal will remain in the receive mode with the receiver disabled. When the terminal goes READY (NOT BUSY), the terminal enters the transmit mode, transmits the first programmed LTA character and returns to the receive mode. If DCD switches ON while waiting for the terminal to go READY, the terminal will enable the receiver and the receive mode is resumed.

 DC current loop: READY/BUSY status is reported the same as in full-duplex data set mode.

Section 5

Theory of Operation

5.1 FUNCTIONAL DESCRIPTION

The 780 series of data terminals are light-weight interactive terminals which utilize the thermal printing technique. The terminals operate in three modes, selectable by the operator: ONLINE, LOCAL and COMMAND.

- ONLINE Operation: With the terminal in the ONLINE mode, the keyboard and printer operate in conjunction with the external interfaces as dictated by the communications discipline and modified by the specific interface options.
- LOCAL Operation: With the terminal in the LOCAL mode, the terminal operates in a "typewriter" mode; i.e., the keyboard is connected to the printer and no data is transmitted or received. All communications-related functions of the keyboard are inoperable (i.e., BREAK, etc.) in this

mode except HERE IS (ABM will be printed if the PRINT ABM copy is enabled, *code* 72).

COMMAND Operation: With the terminal in the COMMAND mode, operating parameters can be changed, reports can be requested, special tests can be conducted, and certain automatic functions can be initiated from the keyboard.

5.2 TERMINAL CONTROLLER

The terminal controller is an 8080A, which together with a TMS5504 multifunction I/O controller, associated memory and control logic, controls the mechanism stepping, keyboard scanning, printing, and data communications. A functional block diagram of the terminal is shown in Figure 5-1.

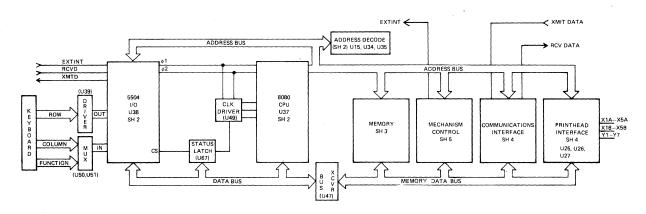


Figure 5-1. 8080A Microprocessor Functional Block Diagram

5.2.1 8080A Microprocessor

The 8080A is an eight-bit microprocessor which operates at 2 MHz, and can address up to 64K bytes of memory. The two-phase clock is provided by a 74LS424 clock generator/driver which contains a crystal-controlled oscillator, a "divide-by-nine" clock phase generator, two high-level drivers and several auxiliary logic functions. Included are power-up synchronization of ready and reset, and an advance status strobe. The external crystal operates at 18 MHz which, when divided down, provides the 2 MHz two-phase clock. For a more detailed description of the 8080A microprocessor, refer to Appendix A.

A bus transceiver (74LS245) provides buffering of the microprocessor data bus. It also provides the capability of isolating the data bus from the rest of the circuit so it may be grounded to force the microprocessor to execute NOP instructions for the purpose of signature analysis.

5.2.2 TMS5504 Multifunction I/O Controller

The TMS5504 contains five programmable interval timers which provide time intervals from 64 microseconds to 16,320 microseconds. The timers are "countdown" timers only, which means they are loaded with an initial value, counted down to zero, and then generate an interrupt to the microprocessor. These timers are used to regulate mechanism speed and to time various delays and timing loops used in the software.

The communications section of the TMS5504 is an asynchronous transmitter and receiver for serial communications and provides the following functions:

 Programmable data communications rate of 110, 200, 300, 600, 1200, 2400 or 9600 bits per second (bps),

- Incoming character detection by the receiver section,
- Character transmission, and
- Status signals including framing and overrun error flags, start and data-bit detectors and end-of-transmission (break) signals from external equipment.

The TMS5504 provides a parallel input and parallel output port used for keyboard scanning and decoding. The TMS5504 is also used as an interrupt controller prioritizing the interrupts of the internal timers, UART and an external interrupt. This external interrupt provides feedback of printhead position and velocity to the microprocessor (see paragraph 5.3.2). By using the Interrupt Mask Register, the microprocessor can enable or disable any combination of interrupts. For a more detailed description of the 5504 I/O controller, refer to Appendix B.

5.2.3 Terminal Controller Memory

The terminal utilizes the following types of memories:

- Read-Only Memory (ROM),
- Random-Access Memory (RAM),
- Complementary Metal-Oxide Semiconductor RAM (CMOS RAM),
- Programmable ROM (PROM).

Figure 5-2 shows a typical memory organization used in the terminal.

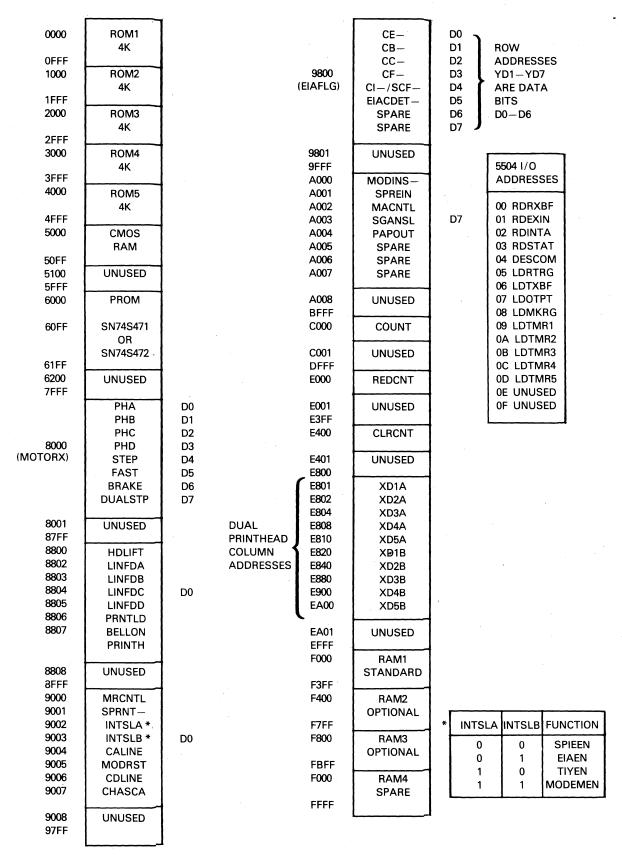


Figure 5-2. Memory Organization

5.2.3.1 Read-Only Memory. The operating program (firmware) and self-test programs are contained in 16K bytes of ROM. Four $4K \times 8$ -bit TMS4732 devices are installed in sockets U59, U60, U61, and U62. U63 is an option ROM. Data is transferred via the microprocessor bidirectional data bus, when enabled by the memory control logic and addressed by the address lines A0 through A15 (2265832, sheet 2).

5.2.3.2 Random-Access Memory. The terminal microprocessor uses up to 4K bytes of RAM for temporary storage of data and intermediate program information. The RAM consists of up to eight $1K \times 4$ -bit TMS4045 devices, installed in pairs to make $1K \times 8$ -bit memories. The self-test can be used to isolate a particular failed RAM pair. The RAM is enabled by the memory control logic (2265832, sheet 2).

5.2.3.3 Nonvolatile Memory. The nonvolatile memory consists of a Complementary Metal Oxide Semiconductor (CMOS) RAM and a +2.7 volt battery to provide nonvolatile storage of configuration parameters and communications information when the terminal is turned OFF. The CMOS RAM is a 256 \times 4-bit device installed in socket U30.

5.2.3.4 Programmable ROM. As an option, the answerback message can be stored in a nonalterable ROM. The PROM is installed in socket U64. This PROM can also contain other information.

5.2.3.5 Memory Control Logic. Memory and control latch address decoding is accomplished with three 74LS138 3-to-8 line decoders and half of a 74LS139. These devices decode address lines A10 through A15 and provide the appropriate chip enable strobes for the memory and control latches. The strobes are generated by gating the enable inputs of the decoders with DBIN or WR—. This ensures that chip enable to the various memories and latches is true when data is valid on the data bus during a WRITE or when the microprocessor is executing a READ.

A 74LS175 status latch is used to decode 8080 status. The status bits decoded are WO-, INTA, IN, and OUT. WO- is used to control data flow through the bus transceiver. INTA disables the bus transceiver and address decoders during the

time in which the TMS5504 strobes a RST (restart) instruction on the data bus resulting from an interrupt. The TMS5504 enable line is also generated from the status latch. In addition to enabling the TMS5504, this line also disables the bus transceiver and address decode chips. This prevents any possible conflict on the data bus between the TMS5504 and memory or control latches.

5.3 MECHANISM DRIVE ELECTRONICS

The printer mechanism drive electronics convert the processor control signals into the appropriate closed-loop, controlled dc signals to drive a fourphase printhead stepping motor, a headlift solenoid, and a four-phase paper advance stepping motor.

5.3.1 Printhead Drive Motor Electronics

The printhead drive motor electronics comprises five sections: phase select inputs, current-decay time-constant control, current adjust inputs, 20 KHz switching regulator, and PNP power drivers. A block diagram of the printhead drive electronics is shown in Figure 5-3.

5.3.1.1 Phase Select Circuit. Four open-collector output comparators in U201 select and control the current applied to each of the respective phases of the printhead drive motor (refer to schematic 2265832, sheet 6). The phase select input enables the particular phase, and the feedback generated by comparator (U201, pin 4) allows pulsewidth modulation control.

The operation of a single phase is discussed, using Phase A as an example. The TTL logic level from U24-19 (PHA) controls current flowing in Phase A. When the signal PHA is a logic ONE, the output of the comparator switches to a logic ZERO and power transistor Q204 is driven into saturation, applying approximately 29 volts to the Phase A (ϕ A) winding of the stepper motor. When the open-collector output of the comparator switches high (PHA at logic ZERO), Q204 is cut off and no current flows in the winding.

5.3.1.2 Switching Regulator Circuit. Current to drive the stepper motor is supplied by a switching regulator which is synchronized to a 20KHz square-wave signal (PWRCLK) from U70-13. This

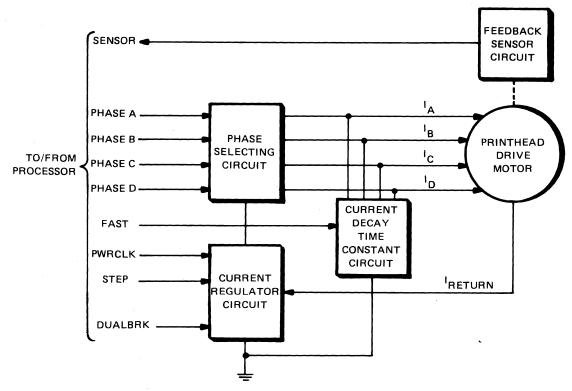


Figure 5-3. Printhead Drive Electronics Block Diagram

signal is integrated by C203, R218 and C202. Pulsewidth modulation at 20 KHz is accomplished by summing the resulting triangular waveform with the motor phase current sample voltage from R205 at the noninverting input (pin 6) of U201. When the voltage at pin 5 of U201 is more positive than at pin 6, the output of the comparator at pin 4 switches to a logic ZERO thus enabling the comparators in the phase select circuit. The voltage present at the noninverting inputs is determined by a voltage divider consisting of R215 and R217. With the comparators enabled, current flows in the selected motor winding when the respective signal (PHA-PHD) is active. When the voltage at pin 6 is more positive than pin 5, the phase select comparators are disabled and no current flows in the motor windings.

5.3.1.3 Current Adjust Circuitry. The processor generates control signals which select two sets of three current levels used for stepping, braking, and holding the motor. One set of signals is for high-speed operation which requires higher current levels than low-speed operation. The control signals are STEP and DUAL BRK. These signals change the reference voltage level at pin 5 of U201, thus changing current levels in the motor winding. Table 5-1 illustrates the current select signal relationships.

Table 5-1. Current Select Signal Relationships

STEP	DUAL BRK	MOTOR CURRENT
0	0	0.7 A (Holding)
1	0	1.85 A (Dual Step)
1	1	2.15 A (Dual Brake)
1	0	1.85 A (Single Step)

5.3.1.4 Current-Decay Time-Constant Control. This circuit controls the current discharge of the motor windings to increase the efficiency of the regulator or to provide a rapid discharge of the motor current when stepping at high velocities.

When the current regulator senses sufficient current in the printhead stepping motor winding, it switches OFF the current through the respective driver transistor. The collector of the transistor is suddenly switched from approximately ± 30 volts to a negative voltage by the inductive flyback of the motor winding. The value of this negative voltage determines the time necessary to discharge the current in that winding.

During periods when motor current needs to remain constant (FAST at a TTL low), zener diode CR205 is reverse biased and cut off. The base of transistor Ω 205 is connected through diode CR207 and resistor R211 to -12 volts and remains saturated when conducting motor current during the power switch off-time (flyback period). With Ω 205 saturated, the motor coil voltage is clamped at approximately -1.3 volts, which provides a very slow motor current-decay and results in increased regulator efficiency.

When the processor requires quick discharge of the phase current, it sets FAST to a logic ONE which forces CR205 and CR206 into conduction and reverse biases CR207. With CR207 OFF, Q205 has no base drive and is initially cut off. Q205 remains cut off until a path for base drive is established through CR208 and CR209. Since CR208 is a 20-volt zener diode, the motor coil voltage is clamped at approximately -22.5 volts. This provides a very rapid discharge of the motor current and discharges the OFF phases when stepping at high velocities.

5.3.1.5 Power Drivers. The 30-volt power supply is switched to the motor windings by four PNP darlington transistors, Q204, Q203, Q202 and Q201. When the output of any of the four drive comparators in U201 goes to logic ZERO, the corresponding transistor is driven into saturation, applying approximately 29 volts to the selected motor winding. When the comparator output switches to logic ONE, the respective transistor is cut off.

5.3.1.6 Feedback Sensor Circuit. The processor requires data on the position of the printhead stepping motor to determine when to apply braking, change phases, or make other decisions concerning motion of the printhead carriage. This data is provided by the feedback sensor consisting of a 24-position slotted wheel that interrupts a light path between an IR-emitting diode and a photosensitive transistor. This assembly is mounted on the stepping motor which drives the printhead carriage. The circuit is shown in Figure 5-4. The signal from the phototransistor is input to a Schmitt trigger circuit in U203 (2265832, sheet 8) as illustrated by the block diagram in Figure 5-5.

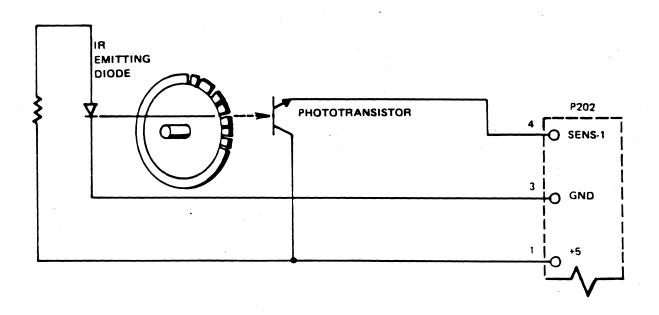


Figure 5-4. Printhead Stepping Motor Feedback Sensor Light Path Schematic

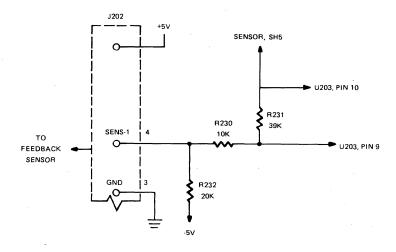


Figure 5-5. Printhead Stepping Motor Feedback Sensor Motor Schematic

As the slotted wheel opens the light path, current flows through the phototransistor and causes U203, pin 10 to high (SENSOR).

5.3.2 Motion Control Electronics

The terminal utilizes two algorithms for single-step

and dual-step printing. The algorithms are implemented with the motion control electronics (2265832, sheet 5). A timing diagram for the single- and dual-step algorithm is shown in Figure 5-6.

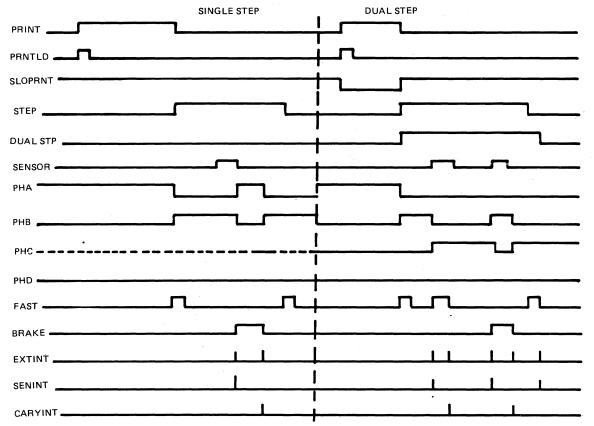


Figure 5-6. Single-Step/Dual-Step Algorithm Timing Diagram

5.3.2.1 Single-Step Algorithm. During a single step, (e.g., from phase A to phase B) the I/O controller generates signals which cause ϕ A to go low and STEP, FAST and ϕ B to go high to initiate motion. After 512 microseconds, FAST goes lows. After 5° of rotation of the stepping motor rotor, the signal from the tach wheel (SENSOR) goes high and at 10° returns low. On the falling edge of SENSOR, a short pulse is generated by single-shot U42. This pulse generates an interrupt signal (EXTINT) which is used by the TMS5504 to interrupt the processor.

At this time, ϕ B goes low and ϕ A goes high which produces the retarding torque to decelerate the printhead-carriage assembly. At the same time, BRAKE also goes high which enables counters U32 and U33. The carry output of the counters is also gated with SENINT. A number corresponding to the brake time is loaded into the counters and, when the carry output goes high, EXTINT goes high and generates another processor interrupt. When this occurs, BRAKE and ϕ A return low and ϕ B goes high. After a short delay, STEP returns low and FAST goes high for 512 microseconds, thereby terminating the single-step; the printhead-carriage assembly comes to a stop.

5.3.2.2 Dual-Step Algorithm. During a dual step (e.g., from phase A to phase C), the I/O controller generates signals which cause ϕ A to go low and FAST, STEP, DUALSTP and Φ B to go high to initiate motion. After 512 microseconds, FAST goes low. After rotating 5°, the stepping motor rotor causes the signal from the tach wheel (SENSOR) go to high and at that time a processor interrupt (EXTINT) is generated.

 $\phi\,B$ returns low, $\phi\,C$ goes high, and FAST goes high enabling the counters U32 and U33. The carry output of the counters is also gated with SENINT. A number corresponding to the desired FAST pulsewidth is loaded into the counter and, when carry goes high, EXTINT goes high interrupting the processor. At this time, FAST returns low. After 20° of rotation, SENSOR goes high again generating another processor interrupt causing $\phi\,C$ to return low and $\phi\,B$ to go high, thus

providing the retarding torque. BRAKE goes high enabling the counters and the carry interrupt. The desired brake time is loaded into the counters and, when the carry goes high, EXTINT goes high, interrupting the processor. At this time, BRAKE and ϕ B return low and ϕ C goes high. After a short delay to allow the printhead-carriage assembly to settle, STEP and DUALSTP return low and FAST goes high for 512 microseconds, terminating the dual step.

5.3.3 Headlift Solenoid

The headlift function is performed when the signal HDLFT, generated by the processor, is logic ONE. HDLFT is gated with PWRCLK generating HDLIFT which is switched at 20 KHz, thus regulating the solenoid current to 0.8 amperes. HDLIFT provides base drive for transistor Q206 which completes the path to ground for current flowing through the headlift solenoid winding.

This function prevents excessive wear of the printhead during carriage returns or when the printhead slews across the platen.

5.3.4 Paper Advance

The paper advance function utilizes a four-phase stepping motor driven by signals generated by the processor. The signals LINFDA through LINFDD create a path to ground, allowing current to flow through the respective motor winding.

5.4 PRINTHEAD SYSTEM

The printhead system consists of the following parts:

- Printhead
- Printhead drivers
- Temperature-compensation circuit
- Print voltage circuit.

A block diagram of the printhead system is shown in Figure 5-7.

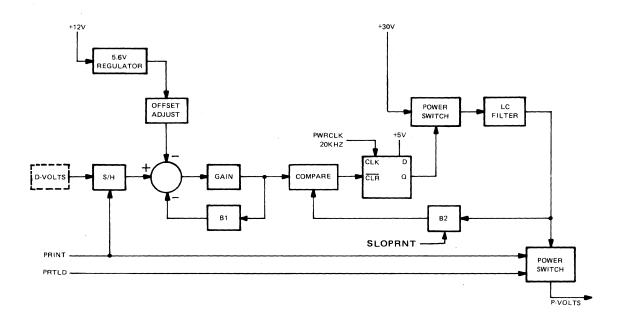
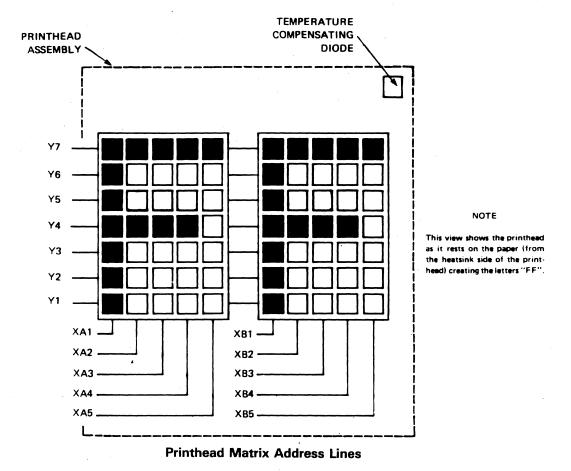


Figure 5-7. Printhead System Block Diagram

5.4.1 Printhead

The printhead consists of two five-by-seven matrices of 35 heating elements and a temperature-sensing diode mounted on a single monolithic chip. Mounted on a heatsink, the chip is connected to the printhead interface PC card by a flexible cable. Mounted on the printhead interface PC card is a selected resistor (RTRIM) which controls the characteristics of the temperature-compensating circuit so that its operation is optimum for each individual printhead.

Each of the 70 heating elements on the printhead includes an SCR. The 70 elements are controlled by the printhead driver address lines as shown in Figure 5-8. When both X and Y inputs are positive to a given element, the SCR fires and remains on (approximately four milliseconds) until PVOLTS is switched OFF.



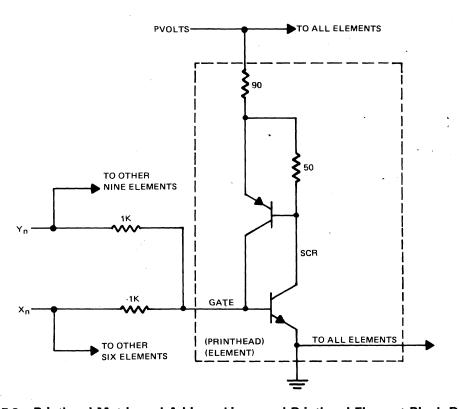


Figure 5-8. Printhead Matrix and Address Lines, and Printhead Element Block Diagram

5.4.2 Printhead Drivers

The printhead drivers are implemented using three SN98614 linear integrated circuits, consisting of six driver circuits each. Each driver has a low-power TTL AND input stage and a totem pole, power transistor output stage. All drivers are enabled by the signal PRNTHDSTBE, and each is controlled by an individual (address or data) line from the processor.

Each driver translates TTL logic levels into the levels necessary to control the printhead heating elements. The nominal output levels of the drivers are -4.7 volts low and +3.5 volts high.

5.4.3 Temperature-Compensation Circuit

This circuit provides a regulated, temperature-compensated voltage to the printhead. The proper print voltage (PVOLTS) is derived from the voltage drop (DVOLTS) across RTRIM and the PN junction of the temperature-compensating diode (DT) on the monolithic printhead chip. The total amount of energy per dot transferred from the printhead to paper (during each character print) is a function of the initial printhead temperature as well as the print time and the applied voltage. Initial temperature is determined by sampling DVOLTS prior to a character print. PVOLTS is then varied as a function of DVOLTS to achieve uniform contrast.

5.4.4 Print Voltage Circuit

Referring to schematic 2265832, sheet 7, R115 provides approximately 750 microamperes of current to RTRIM and DT, which are connected in series with R110 to ground on the printhead assembly. RTRIM is selected during manufacture so that its resistance compensates for variations in the voltage/current characteristics of DT. Thus, the resulting voltage across RTRIM and DT is nominally 0.964 volts.

When the signal PRINT from the processor is logic ZERO, Q103 saturates, applying +5 volts to the cathode of CR102 which holds it OFF and turns ON Q109, since the gate and drain are tied together through R133. With Q109 ON, a path of low impedance is provided which allows the sampling capacitor C103 to track the variation of DVOLTS. In the ON state, Q109 has a maximum resistance of 60 ohms. At a one-volt level, RTRIM and DT have a characteristic impedance of 1.0V/0.75mA = 1.3Kohms. The resultant RC

time constant is $(1.3K + 60)(10^{-6})$ or 1.36 milliseconds, $\pm 20\%$ for variation in C108, and the voltage changes and resulting impedance changes in RTRIM and DT. The maximum 95% charge time is therefore $((1.63)(10^{-6})) = 4.9$ milliseconds. The holding time (discharging time constant) for C108 is greater than 100 milliseconds with less than 1% drop.

When PRINT switches high, Q103 is cut off which places the collector of Q103 and cathode of CR102 at -12 volts. This switches Q109 OFF and prevents the voltage on C108 from changing during a PRINT period.

When printing at 30 cps or less, or from the keyboard, the print time is 8 msec. Under these conditions, the SLOPRNT signal is in the open collector state and R144 is effectively removed from the circuit. The gain and offset biasing for U103 and U102 thus provide the following relationship between DVOLTS and PVOLTS REG.

PVOLTS REG = 49.8 (DVOLTS - OFFSET)

When printing at higher speeds, the print time is 4 msec. Under these conditions, the SLOPRNT signal is low which places R144 in parallel with R105. This increases the circuit gain and the following relationship holds.

PVOLTS REG = 72.0 (DVOLTS - OFFSET)

The OFFSET voltage is varied by the contrast potentiometer (R137). The range of adjustment is from 0.569 to 0.675 volts. R139 is selected during manufacturing test of the PWB in order to calibrate the function of the temperature-compensation circuit. This calibration enables use of any printhead with any PWB without any adjustment or circuit change.

A pulsewidth-modulated switching regulator provides the increased current demands of the dual printhead while maintaining high operating efficiency. Pulsewidth modulation is implemented using comparator U102 and a type-D flip-flop U101. The D input is tied high and PWRCLK (a 20KHz square wave) is applied to the CLK input. When the Q output of U101 goes high, transistor Q106 saturates thus turning on transistor Q104 which applies approximately 30 volts to L101 and C102. Q104 remains saturated until the clear input to

U101 is pulled low, which occurs when PVOLTS REG is at the desired voltage. The inverting input (pin 10) of U102 exceeds the level at the noninverting input, thus clearing U101 and turning off Q106 and Q104. Q104 is turned on at the next leading edge of PWRCLK and subsequently turned OFF when the voltage reaches the desired level.

The switching circuit that supplies the print voltage to the printhead consists of transistors Q101, Q102 and Q108. Figures 5-9 and 5-10 show timing diagrams of the voltage waveforms for

single and dual character print, respectively. When PRINT and PRNTLD go high, Q102 and Q108 saturate, applying approximately 10 volts to the base of Q101. During the time the PRNTLD is high, print data is strobed into the printhead from the printhead drivers U25, U26 and U27 and PVOLTS is approximately 9 volts. Once the print data is strobed into the printhead, PRNTLD goes low turning OFF Q102 which allows Q101 to saturate, applying PVOLTS REG to the printhead. After four or eight milliseconds, depending on SLOPRNT, PRINT goes low turning OFF Q101 and Q108 and thus terminating the print cycle.

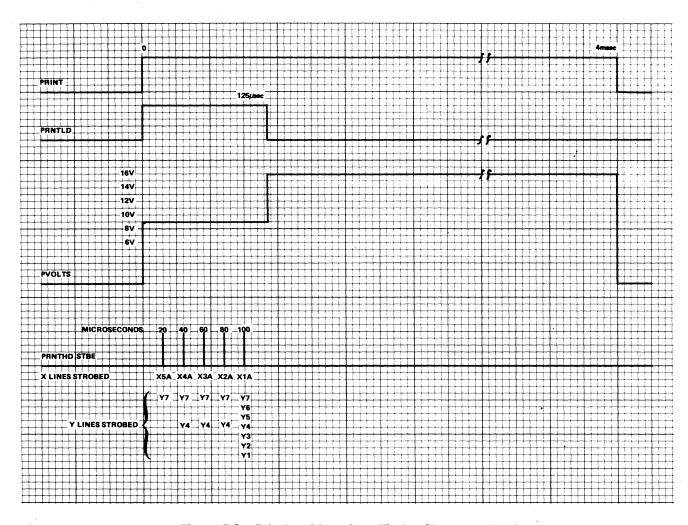


Figure 5-9. Printhead Interface Timing (For Letter "F")

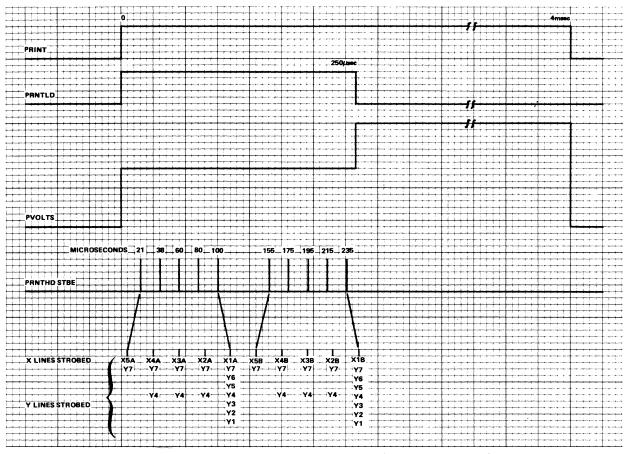


Figure 5-10. Printhead Interface Timing (For Letters "FF")

A current-limiting soft-start circuit consisting of R126, R127, CR105 and Q107 limits the power-up surge current into C102. The voltage developed across R126 and R127 is proportional to inductor (L101) current. When the voltage drop across the resistors becomes large enough to turn ON CR105 and Q107, the collector of Q107 is pulled down to PVOLTS REG and the level at U102, pin 9 is below the reference level at pin 8. This causes the output at pin 14 to go low, clearing U101 and thus turning OFF the power switch Q104. U101 is set on the next leading edge of PWRCLK and Q104 is again turned ON. The overcurrent circuit turns Q104 OFF when the current limit is exceeded, until C102 becomes sufficiently charged. During normal operation, the current in L101 should never exceed the trip point (approximately 16 amperes).

Protective circuits to prevent damage to the printhead are provided by two comparators in U102 should PRINT remain high for more than the normal four milliseconds.

PRINT is ac-coupled to the inverting input (pin 6) of U102 through C103. The noninverting input

(pin 7) is a reference level provided by CR106. When PRINT goes high, C103 goes to a TTL logic ONE causing the level at the inverting input of U102 to exceed the reference level at the noninverting input. The output at pin 1 goes low, turning on Q108 which turns on Q101. To prevent thermal damage to the printhead, R107 and C103 form a decay circuit having an RC time constant of approximately 12 milliseconds. After 12 milliseconds, the voltage on C103 and at the inverting input of U102 falls below the reference level at the noninverting input, pin 7 and the output at pin 1 goes high which turns off Q108 and Q101.

A portion of the output voltage (PVOLTS REG) is fed back (via R140 and R141) to the inverting input (pin 4) of U102 which is compared to the reference voltage generated by CR106 at the non-inverting input (pin 5). Any circuit failure which causes PVOLTS REG to exceed 24 volts will result in the voltage at pin 4 exceeding the reference voltage at pin 5. Under this condition, the output (pin 2) of U102 goes low which causes the level at pin 1 of U102 to remain high, thus keeping Q108 cut off which holds Q101 OFF.

5.5 KEYBOARD

5.5.1 Keyboard Scan

The control electronics generate control signals to scan the keyboard once every eight milliseconds. When a key depression is detected during a scan, the character is encoded and the proper action is taken by the terminal. After a depression is detected, an eight-millisecond delay is generated by the software to take care of debounce. No other key depressions are processed by the terminal until the first depression is released. Release of the key starts an eight-millisecond contactbreak debounce period. After the debounce period, keyboard scans resume at eightmillisecond intervals. Each scan is a complete scan of all rows and columns which detects multiple key depressions. The control electronics ignore simultaneous depressions, in which case neither key is acted upon.

5.5.2 Keyboard Interface

Keyboard scanning uses the parallel I/O ports of the TMS5504 along with two 74LS157 multiplexers and a 7417 open-collector driver. The keyboard rows are scanned by placing logic ZERO on each row of the keyboard with parallel output port and then reading the columns through the multiplexers and parallel input ports thus detecting a switch (key) closure. Keyboard debounce is accomplished by the software.

5.6 POWER SUPPLY

The 780 series data terminals use one of two power supplies to convert the ac input to the regulated dc output power required to drive all circuits within the terminal. The domestic version is shown in schematic 2265837 and the international version is shown in schematic 2265972. The power supplies operate over an input voltage range of 90 to 280 Vac and a frequency range of 47 to 450 Hz. A jumper or jumpers on the terminal electronics PWB change the terminal from 120 Vac to 230 Vac operation.

5.6.1 Domestic Power Supply

The power supply consists of the following major parts:

- Input voltage selection, rectification and soft start.
- Blocking oscillator and regulator.
- Failure protection.
- Snubber and clipper circuits.
- Output rectifiers and filters.

A block diagram of the power supply is shown in Figure 5-11.

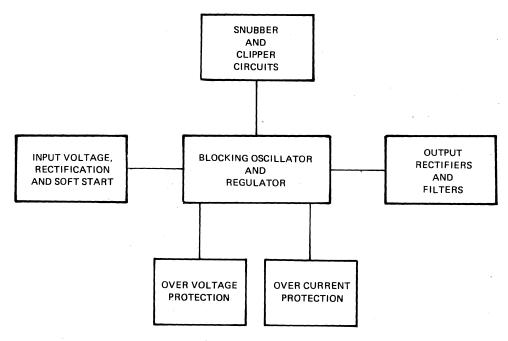
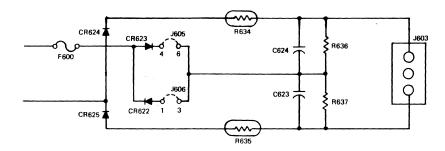


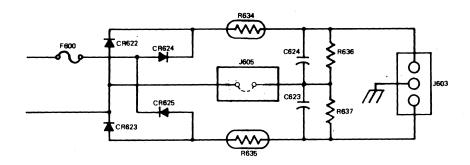
Figure 5-11. Domestic Power Supply Block Diagram

5.6.1.1 Input Voltage Selection, Rectification and Soft Start. Power is supplied through the power-on switch, transient suppressor, voltage selection and input rectification (schematic 2265832, sheet 8) to J603. If the terminal is configured for 120 Vac operation, on terminal electronic PWBs up to revision D, jumpers are installed between pin 4 and pin 6 and pin 1 and pin 3 to form a voltage doubler as shown in Figure 5-12a. Terminal electronic PWBs after revision D

use a single jumper to form a voltage doubler as shown in Figure 5-12b. For 230Vac operation, on revision D and below, jumpers are installed between pin 4 and pin 5 and pin 1 and pin 2 to form a full-wave bridge as shown in Figure 5-13a. Revision E and later terminal electronic PWBs use a single jumper as shown in Figure 5-13b. The absence of the jumper in the later version forms a full-wave bridge.

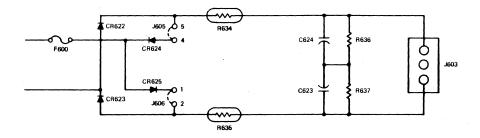


a. Voltage Doubler (Up through Rev. D)

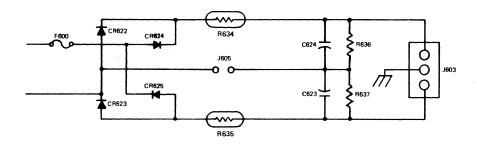


b. Voltage Doubler (Rev. E and Above)

Figure 5-12. Voltage Doublers



a. Full-Wave Bridge (Up through Rev. D)



b. Full-Wave Bridge (Rev. E and Above)

Figure 5-13. Full-Wave Bridge

During power-up, thermistors R634 and R635 limit the initial surge of current to provide the soft-start for the power supply. The thermistor has a negative temperature coefficient so that as the temperature increases, the resistance of the thermistor decreases, allowing the current to increase.

5.6.1.2 Blocking Oscillator and Regulator. The blocking oscillator and regulator circuit (2265837, sheet 1) is a self-starting circuit which uses the primary winding of transformer T600 as a collector load for the main switching transistor Q600. When the switching transistor is ON,

energy is stored in the primary winding of the transformer. When the switching transistor turns off, the magnetic field in the primary winding collapses and the energy is coupled into the secondary windings of the transformer.

In operation, the positive feedback path passes from the power transformer primary to the base-drive winding. The base-drive signal is coupled through C613 and diode CR606, then through current-setting resistor R611 to the base of power transistor Q600. Oscillation begins when the primary-side dc appears. A current set by R608

and R610 flows through R61 into the base of Q600, biasing it on. Random noise components of the Q600 collector current ensure that its collector current will increase because of the positive feedback from the primary to base windings. The base current established through Q600 will increase linearly as determined by the primary inductance of transformer T600 and the input dc supply voltage impressed across it.

When the voltage drop across the current sense resistor, R624, produced by the Q600 emitter current, raises to approximately 0.6. volts, Q601 begins to conduct, shunting base drive from the switching transistor base which starts to turn off. As soon as its collector voltage begins to rise, Q600 is rapidly switched off by regenerative feedback generated in the tertiary winding. Falling collector current causes the collector voltage to increase (because of the transformer primary inductance), resulting in falling base drive voltage and falling base current. The collector voltage of Q600 "flys back" above the input dc supply voltage (resulting in reverse base drive current coupled through C613) until the rectifiers in the transformer secondary circuits become forward biased and current flows into the output filter capacitors (and output load resistances). The energy stored in the magnetic field of the transformer during the "ON" time of Q600 is transferred to the output during the "OFF" time of Q600.

Secondary currents continue to flow, decreasing linearly (approximately) with time, until the transformer flux has fallen essentially to zero. The transformer terminal voltages remain at their flyback values during the entire period of secondary current flow. During a single flyback period the output voltages rise only a few percent of their full values, as determined by the output capacitors. As the flyback currents fall to zero, the voltages across the transformer windings decay toward zero. During the flyback interval C613 acquires a charge of about one volt (left-hand side positive) from the current drawn from R611 which is clamped by Q601; this transistor acts as an emitter follower in the inverted mode (collector acting as an emitter and vice versa) when its collector goes over a diode drop below the primary side dc ground; the current coming from start-up resistors R608 and R610 is much smaller than the current in

R611 and has negligible effect once oscillation is initiated. As the voltage across the base drive winding falls toward zero, the positive voltage across C613 raises the base of Q600 to the threshold of conduction through R611, initiating another regenerative power transistor turn-on cycle.

Transistors Q602, Q603 and Q604, along with operational amplifier U601 and associated resistors, diodes, and the sense winding of the transformer, make up the regulator portion of the power supply. Until the output voltages reach their correct values, the power transistor collector current ramps up to its current limit (as set by Q601) each cycle, transferring the maximum safe amount of energy (determined principally by transformer heating and core saturation limitations) each cycle to the filter capacitors and output loads. During each flyback cycle, C621 is charged through CR613 and series resistors R624 and R629 the same way as the output load capacitors.

R624 and C619 and R629, along with the main regulator filter capacitor C621, serve as highfrequency noise and spike filters so that C621 is charged to the average value (less a diode drop) of the flyback voltage appearing across the sense winding during each cycle. As soon as voltage is developed across C612, the negative input of U601 (because of the voltage divider formed by R630, R631 and R621) becomes negative with respect to its positive input which, since zener diode CR610 passes essentially zero current until its breakdown voltage is approached, is held at the full output voltage of C621 through R632, R633 and R619. This assures that the operational amplifier will remain in positive saturation and, therefore, Q604 will be off. As the regulator outputs rise toward their correct values and the voltage across C621 increases proportionally, the voltage at the positive input of U601 is clamped as CR610 begins conducting. Voltage then appears across R633 and R632 because of current in R619 which, as the voltage on the negative input of U601 approaches that of its positive input (because of current through R620), initiates output voltage regulation. As its base voltage falls below the output of C621 by two diode drops, Q604 begins to conduct, acting essentially as a controlled constant current source whose output current flows into timing capacitor C614.

During flyback the base drive winding, which also drives R614, is negative, energizing CR614 and thereby clamping the timing capacitor to ground through the base-collector diode of Q603, sinking the output of current source Q604. When the power transistor Q600 switches on after flyback ends. R614 is taken positive by the base drive winding, causing Q603 to operate as an emitter follower, buffering the timing capacitor C614. The voltage across C614 then begins to ramp up to a rate proportional to the current from Q604. When the increasing voltage across C614 reaches approximately two diode drops, the output of buffer Q603 begins to rapidly energize Q607, which shunts drive current from Q600 and causes its regenerative turn-off just as does current limiter Q601. The action of the regulator loop controls the power transistor "ON" time and the peak current flowing in the transformer primary.

The voltage across C621 is held constant (to within one millivolt) by U601 operating at its full dc open-loop gain to maintain zero differential input voltage. Constant voltage across C621 implies that the flyback voltage feeding CR613 remains constant, and since all windings are very tightly coupled (required for satisfactory power supply operation) the flyback or output voltage from all windings remains constant (ignoring IR drops). Therefore, almost no cross-coupling to the output voltage from one winding results from changing loads on any other winding, and nearly no effect results from changing primary side dc input voltage. The only significant output voltage deviations, well within tolerances, are the changes in output voltage from its own load change which result from rectifier diode drop and winding IR drops.

5.6.1.3 Failure Protection. The power supply has built-in overvoltage and overcurrent protection to prevent damage to the blocking oscillator switching transistor and terminal electronics.

The overvoltage protection circuit consists of Q606 and its associated circuitry. The sense winding of the transformer supplies the biasing voltage for Q606 through diode CR620. Normally, Q606 is biased off, due to zener diode CR621 in the base circuit. CR621 will not conduct until the sense voltage is sufficient to overcome the breakdown voltage of the diode. Once the voltage is greater than the breakdown voltage, Q606 conducts; this

forces the base of transistor Q605 to go to onehalf the sense voltage, which in turn forward biases the base-emitter junction of Q605 since the emitter is held at 10 volts by zener diode CR619. With Q605 conducting, the voltage present at the collector causes Q601 to conduct, which steals base current from the main switching transistor Q600, thus shutting down the power supply. The power supply remains shut down because Q605 remains in conduction because the emitter is held at 10 volts.

Overcurrent protection is provided by Q605. Any increase in current flow in the secondary windings is reflected in the sense winding by a drop in voltage. This drop in voltage is detected at the base of Q605, forward biasing the base-emitter junction, thus forcing Q605 into conduction and causing Q601 to conduct stealing base drive current from Q600, shutting down the power supply.

Instantaneous overcurrent protection is provided by Q601 when the voltage drop across the current sense resistor R624 exceeds two diode drops (CR615 and the base-emitter junction of Q601), thus turning on Q601 which steals base current from Q600.

5.6.1.4 Snubber and Clipper Circuits. The snubber circuit prevents damage to the main switching transistor Q600 during flyback by providing a low-impedance path for the energy created by the collapsing field plus the reflected voltage from the secondary winding. The energy is absorbed in C603 and is dissipated in R601 and R602. Without the snubber, the power appearing in Q600 could exceed the safe operating area of the transistor.

The clipper circuit consists of capacitors C601 and C602, diode CR601 and resistor R600. The clipper circuit clips the flyback voltage overshoot due to imperfect transformers, which prevents any fluctuations being reflected in the sense winding.

5.6.1.5 Output Rectifiers and Filters. Transformer T600 has four secondary windings which generate the voltages used in the terminal. The windings produce +30Vdc, +5Vdc, +12Vdc and -12Vdc. The -12Vdc is also used to generate a -5Vdc, by using a three-terminal regulator U600. The +30V winding is rectified by CR605 and filtered by a pi filter consisting of C604,

L600 and R605. The +5V winding is rectified by CR604 and filtered by a pi filter consisting of C605, L601 and C606. CR602 rectifies the +12V winding and a pi filter, consisting of C607, L602 and C608, filters the output. The -12V winding is rectified by CR603, and the output is filtered by a pi filter consisting of C609, L603 and C610. The filtered outputs are supplied to the terminal electronics PWB via P604.

5.6.2 International Power Supply

The international power supply consists of the following major parts:

- Input voltage selection, rectification and soft start.
- Blocking oscillator and regulator.
- Failure protection.
- Snubber and clipper circuits.
- Output rectifiers, filters and regulators.

A block diagram of the international power supply is shown in Figure 5-14.

5.6.2.1 Input Voltage Selection, Rectification and Soft Start. As previously described in paragraph 5.6.1.1, power is supplied through the power-on switch, transient suppressor, voltage selection and input rectification (schematic 2265832, sheet 8) to J603. If the terminal is configured for 120Vac operation, on terminal electronic PWBs up to revision D, jumpers are installed between pin 4 and pin 6 and pin 1 and pin 3 to form a voltage doubler as shown in Figure 5-12a. Terminal electronic PWBs after revision D use a single jumper to form a voltage doubler as shown in Figure 5-12b. For 230Vac operation, on revision D and below, jumpers are installed between pin 4 and pin 5 and pin 1 and pin 2 to form a full-wave bridge as shown in Figure 5-13a. Revision E and later terminal electronic PWBs use a single jumper as shown in Figure 5-13b. The absence of the jumper in the later version forms a full-wave bridge.

During power-up, thermistors R634 and R635 limit the initial surge of current to provide the soft-start for the power supply. The thermistor has a negative temperature coefficient so that as the temperature increases, the resistance of the thermistor decreases, allowing the current to increase.

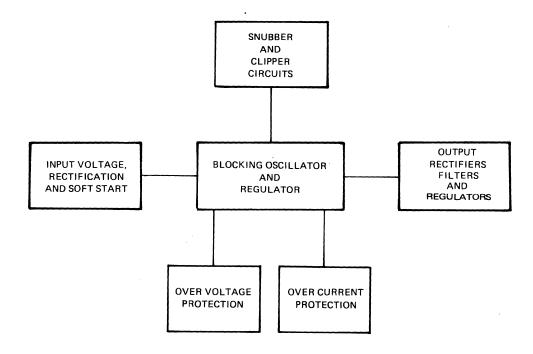


Figure 5-14. International Power Supply Block Diagram

5.6.2.2 Blocking Oscillator and Regulator. The blocking oscillator and regulator circuit (2265837, sheet 1) is a self-starting circuit which uses the primary winding of transformer T500 as a collector load for the main switching transistor Q504. When the switching transistor is ON, energy is stored in the primary winding of the transformer. When the switching transistor turns off, the magnetic field in the primary winding collapses and the energy is coupled into the secondary windings of the transformer.

In operation, the positive feedback path passes from the power transformer primary to the basedrive winding. The base-drive signal is coupled through C500 and diode CR500, then through current-sensing resistor R500 to the base of power transistor Q504. Oscillation begins when the primary-side dc appears. A current set by R512 flows through R500 into the base of Q500, biasing it on. Random noise components of the Q504 collector current ensure that its collector current will increase because of the positive feedback from the primary to base windings. The base current established through Q504 will increase linearly as determined by the primary inductance of transformer T500 and the input dc supply voltage impressed across it.

When the voltage drop across the current sense resistor R511 (produced by the Q504 emitter current) rises to approximately 1.2 volts, Q502 begins to conduct, shunting base drive from the switching transistor base which starts to turn off. As soon as its collector voltage begins to rise, Q504 is rapidly switched off by regenerative feedback generated in the tertiary winding. Falling collector current causes the collector voltage to increase (because of the transformer primary inductance), resulting in falling base drive voltage and falling base current. The collector voltage of Q504 "flys back" above the input dc supply voltage (resulting in reverse base drive current coupled through C500) until the rectifiers in the transformer secondary circuits become forward biased and current flows into the output filter capacitors (and output load resistances). The energy stored in the magnetic field of the transformer during the "ON" time of Q504 is transferred to the output during the "OFF" time of Q504.

Secondary currents continue to flow, decreasing linearly (approximately) with time, until the transformer flux has fallen essentially to zero. The transformer terminal voltages remain at their flyback values during the entire period of secondary current flow. During a single flyback period the output voltages rise only a few percent of their full values, as determined by the output capacitors. As the flyback currents fall to zero, the voltages across the transformer windings decay toward zero. During the flyback interval C500 acquires a charge of about one volt (left-hand side positive) from the current drawn from R500 which is clamped by Q502; this transistor acts as an emitter follower in the inverted mode (collector acting as an emitter and vice versa) when its collector goes over a diode drop below the primary side dc ground; the current coming from start-up resistor R512 is much smaller than the currents in R500 and have negligible effect once oscillation is initiated. As the voltage across the base drive winding falls toward zero, the positive voltage across C500 raises the base of Q504 to the threshold of conduction through R6500 initiating another regenerative power transistor turn-on cycle.

Transistors Q500 and Q501, along with the sense winding of the transformer make up the regulator portion of the power supply. Until the output voltages reach their correct values, the power transistor collector current ramps up to its current limit (as set by Q502) each cycle, transferring the maximum safe amount of energy (determined principally by transformer heating and core saturation limitations) each cycle to the filter capacitors and output loads. During each flyback cycle, C501 is charged through CR501 the same way as the output load capacitors.

The voltage appearing across the base-emitter junction of Q500 is a function of the average sense voltage on C501, the zener diode, and the voltage divider resistors (the 56-ohm and 200-ohm potentiometers). Q500 is used as voltage-controlled current source and charges timing capacitor C504. During the "charge" period for T500 (Q504 is in saturation and the current in the primary of T500 ramps positively), transistor Q501 acts as an emitter follower, buffering the voltage across timing capacitor C504. Transistor Q502 acts as a threshold switch which terminates the T500

"charge" period. The "charge" period or "ON" time for Q504 is then a function of how long it takes C504 to reach the threshold of Q502. The rate of voltage rise across C504 is proportional to the charging current from the collector of Q500, which ultimately is proportional to the voltage across C501 and all the other secondary capacitors. In this manner, the secondary voltages (it is important to remember that the sense winding and associated capacitor also are one of the secondaries) are maintained constant.

5.6.2.3 Failure Protection. The supply has an overvoltage latch, instantaneous overcurrent limiting, and secondary overcurrent limiting. Zener CR505 and R508 form an overvoltage sense divider which provides a signal to the gate of SCR Q503. When Q503 is turned ON it latches (because of the dc voltage present at its anode), and a voltage is produced across R509 which is used to disable the supply until power is removed. The +12, -12 and -5 volt secondaries have overcurrent limiting provided by linear regulators. With these regulators, the output "folds back" if the current exceeds the device limit. Overcurrent limiting is provided on the +5 and +30 volt outputs by a fuse.

Instantaneous overcurrent protection is provided by Q502 when the voltage drop across the current sense resistor R511 exceeds two diode drops (CR508 and the base-emitter junction of Q502), thus turning on Q502 which steals base current from Q504.

5.6.2.4 Snubber and Clipper Circuits. The snubber circuit prevents damage to the main switching transistor Q504 during flyback by providing a low-impedance path for the energy created by the collapsing field plus the reflected voltage from the secondary winding. The energy is absorbed in C509 and is dissipated in R515 and R516. Without the snubber, the power appearing

in Q504 could exceed the safe operating area of the transistor.

The clipper circuit consists of capacitors C516 and C517, diode CR511, and resistor R514. The clipper circuit clips the flyback voltage overshoot due to imperfect transformers, which prevents any fluctuations being reflected in the sense winding.

5.6.2.5 Output Rectifiers, Filters and Regulators. Transformer T500 has four secondary windings which generate the voltages used in the terminal. The secondaries produce +30Vdc. +5Vdc, +12Vdc, and -12Vdc. The -12Vdc is also used to generate a -5Vdc, by using a threeterminal regulator U502. The +30V winding is rectified by CR514 and filtered by a C511 and C512. The +5V winding is rectified by CR513 and filtered by C507 and C519. CR516 rectifies the +12V winding and a filter consisting of C514, C524 and C525 filters the output. The -12V winding is rectified by CR515 and the output is filtered by a filter consisting of C513, C522 and C523. The filtered outputs are supplied to the terminal electronics PWB via P604. Three-terminal linear regulators are used on the +12V, -12V and -5Vsecondaries. A linear regulator and external pass transistor are used on the +5V secondary.

5.7 COMMUNICATIONS INTERFACE

All data, incoming and outgoing, is routed through the communications interface. The communications interface is under software control and is selectable between EIA, current loop (TTY) or one of several modem options. Control signals (TTYEN-, EIASEL, and MODEMEN-) generated by the processor select which type of communication is used by the terminal. Figure 5-15 is a block diagram illustrating the receive, transmit and control circuitry of the communications interface. Further detail of the circuitry is shown in schematic 2265832, sheet 4.

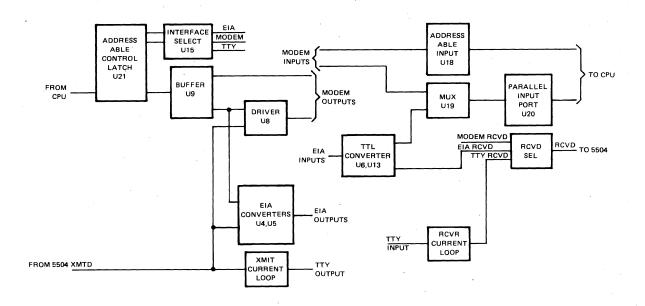


Figure 5-15. Communications Interface

5.7.1 Current Loop Interface

The current loop interface is compatible with a 20-milliampere neutral current loop. In a neutral current loop arrangement, current can flow in only one direction. The interface consists of separate transmit and receive circuits, electrically isolated from each other and from signal and chassis ground. The receiver and transmitter can be used separately in a four-wire full-duplex system or externally connected in series to form a two-wire half-duplex system.

5.7.1.1 Receiver Section. The current loop (TTY) receiver (schematic 2265832, sheet 4) consists of the necessary circuitry to sense current from an external source and to convert the current levels to the appropriate TTL logic levels. The maximum voltage drop across the receiver inputs RL1/RL2 is 3.0 volts at 20-milliamperes loop current into RL1. The MARK/SPACE threshold decision current is nominally 10 \pm 5.5 milliamperes. The receiver circuit utilizes an optically coupled isolator to isolate the current loop from the terminal electronics.

A current level at the receiver circuit input above the MARK/SPACE threshold will forward bias the photodiode of U1. When the U1 photodiode is forward-biased, the phototransistor is energized, supplying approximately +12 volts to the noninverting input of differential comparator U3. The comparator generates a TTL logic level which is applied to a three-state bus buffer U14 which is enabled by the signal TTYEN/ generated by the processor.

With the current level at the receiver circuit input below the MARK/SPACE threshold, the photodiode and phototransistor of U1 are off and the output of the comparator U3 is a logic ZERO.

5.7.1.2 Transmitter Section. The current loop (TTY) transmitter consists of the circuitry necessary to switch the current in the transmit loop (supplied from an external source). The input to the transmitter is an EIA-level logic value. The voltage drop across the transmitter output terminals is less than 1.0 volt at 20 milliamperes loop current when marking. The maximum spacing leakage current is 0.5 milliamperes at 50 volts.

A TTL low level at the transmitter input (U14, pin 9) when enabled by TTYEN/ will switch comparator U3 OFF (high-impedance state), turning the photodiode and phototransistor of U2 off. With no base current drive, output transistor Ω 1 is off and the transmitter is "open" (i.e., no current).

A TTL high at U14, pin 9 will energize comparator U3. With the output pulled low, the photodiode and phototransistor in U2 are energized. With base drive supplied to Q1, the output transistor remains ON, allowing current to flow in the transmit loop.

5.7.2 EIA Interface

The terminal interfaces to any device meeting the EIA Standard RS-232-C or the CCITT Standard V24, through connector J1 on the rear of the terminal.

5.7.2.1 Receive Section. All inputs from J1 are converted from EIA/CCITT levels to TTL logic levels by line receiver circuits U6 and U13. The TTL signals are then multiplexed onto the data bus by U19.

5.7.2.2 Transmit Section. Line drivers U4 and U5 convert the TTL logic levels to EIA/CCITT levels and output the signals through J1.

5.7.3 Acoustic Coupler/Modem

The 785 terminal uses an optional internal modem allowing communication over standard commercial telephone lines via the acoustic coupler interface. The internal modem interfaces with the communications interface through J3 on the main PWB and uses the EIA interface circuitry.

The 785 modem is an originate-only modem which can configure itself to either a RACAL-VADIC 3400 or Bell 103-type format. Selection of the modem type is controlled by an autoselection algorithm or manually through forcing the 3400 or 103 mode. Interface of the modem to the telephone network is through the acoustic coupler muffs located on the rear deck of the terminal. A simplified block diagram of the modem used in the 785 terminal is shown in Figure 5-16. Detailed schematics are in Section 7 (2265842).

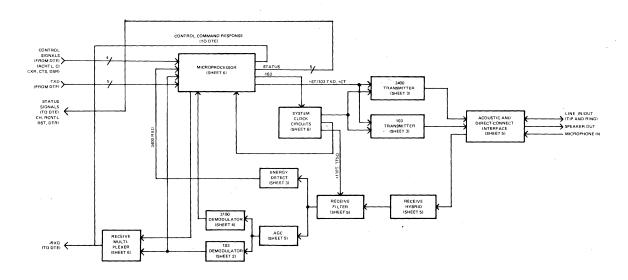


Figure 5-16. 785 Modern Simplified Block Diagram

There are two operating modes of the modem: the control mode and data transfer mode. When the control mode is requested by the terminal electronics via the RCNTL control input signal, the modem unconditionally enters the control mode and responds with a status signal ACNTL to the terminal electronics PWB. During the control mode, the terminal electronics PWB and modem communicate via the -TXD and -RXD lines. The terminal electronics send a series of configuration and operating commands to the modem via the -TXD input and the modem responds with a series of status response codes to the terminal electronics via the -RXD output. All control mode communication by the modem is handled by the internal microprocessor. Upon receipt of the various commands from the terminal electronics, the microprocessor generates the appropriate hardware control signals to configure the modem circuits to the commanded state(s). When control mode communications have been completed, control mode is dropped by the terminal electronics deactivating RCNTL and the modem responds by deactivating ACNTL. When the control mode is dropped, the data transfer mode is entered.

Upon entry into the data transfer mode, the modem must determine which type of modem is answering the call. If the autoselect mode has been commanded by the terminal electronics, the modem microprocessor begins switching the configuration between 3400 and 103 (with the – 103 control signal) at a 50-millisecond rate. If one of the forced modes is commanded by the terminal electronics, the microprocessor configures the modem for the commanded mode with the – 103 control signal. In either case, the modem searches for receive input energy from the answering modem.

The -103 control signal from the microprocessor controls the generation of the +HET FREQ (heterodyne frequency) which controls the carrier frequency that the receive filter network will accept. When receive energy from the answering modem arrives, it is coupled through the line interface circuit to the receive hybrid. From the hybrid, the receive signal is applied to the receive filter. If the receive filter is configured to accept the receive carrier frequency, the resulting filter output drives both the energy detect and AGC circuits. The AGC circuit provides a standardized

signal level to the 3400 and 103 demodulator circuits.

The energy-detect circuit provides the microprocessor with an indication that receive energy of the required level has been detected. When the microprocessor receives active energy detect plus detected MARK from the applicable demodulator circuit, the handshake routine is complete and an active CXR status signal is sent to the terminal electronics to indicate that a valid answering modem has answered the call. At the same time that the active CSR signal is generated, the microprocessor internally generates a MARK signal of the selected modem type and routes it to the appropriate transmitter circuit for application to the remote (answering) modem. At this point, data transmission can begin at either end.

When the answering modem is a 3400, the 3400 transmit circuits are used. Data from the terminal is routed to the modem via the -TXD input line at 1200 bps. The -TXD data in 3400 mode is asynchronous; the microprocessor contains an asynchronous-to-synchronous buffer which synchronizes the input data to the internallygenerated transmit clock from the system clock circuit. The resultant synchronized data from the microprocessor is encoded as dibits (two bits at a time) forming two baseband signals (+ST/103 TXD and + CT). The baseband signals are the modulating signals for the 3400 transmitter circuit. Carrier frequency for the 3400 transmitter is supplied by the system clock circuit. The resultant modulated carrier output of the 3400 transmitter is a quadrature-amplitude modulated (QAM) signal; QAM signals are carriers with phase shift of 0°. 90°, 180°, or 270°, depending upon the value of the dibit information contained in the baseband signals. The modulated 3400 carrier is coupled to the acoustic-interface circuit where it is routed to the speaker output.

When the answering modem is a 103, the 103 transmit circuits are used. Data from the terminal electronics is routed to the modem via the $-\mathsf{TXD}$ input line at 300 bps. The 103 data is asynchronous; the microprocessor performs an internal timing check on the data and synchronizes it to the transmit clock by adding an extra stop bit where necessary. The resultant synchronized data from the microprocessor is applied to the 103 transmitter circuit as the $+\mathsf{ST}/103\ \mathsf{TXD}$ signal.

The + 103 TXD signal along with the system clock frequency (from the system clock circuit) generates the frequency-shift-keyed (FSK) modulation for the 103 transmitter circuit. The FSK output of the 103 transmitter circuit is coupled to the acoustic interface circuit where it is routed to the speaker output.

The receive circuits of the modem operate in the same manner during data transfer as that previously described for the handshake routine. When the modem is in the 103 mode, the + HET FREQ signal from the system clock circuit configures the receive filter circuits to accept the 2125 Hz 103 carrier frequency; when the modem is in the 3400 mode, the + HET FREQ signal is inhibited and the receive filter circuits are configured to accept the 1150 Hz 3400 carrier frequency. The standardized output level of the AGC circuit is applied to both the 3400 and 103 demodulator circuits in parallel. If the receive signal is 103 data, the 103 demodulator circuit recovers the 103 baseband modulation signal and applies it to the receive multiplexer. If the receive signal is 3400 data, the 3400 demodulator circuit performs both carrier and clock recovery operations from which the dibit data is recovered. The resultant dibit data is then decoded into the 1200 bps, 3400 receive data internally in the microprocessor. The resultant 3400 RXD data signal is applied to the receive multiplexer. The applicable data signal from the receive multiplexer is then gated to the -RXD output which is routed to the terminal electronics.

Provisions are made for local test (analog loopback), initiated remote test (remote digital loopback), and response to remote test (although not shown in the block diagram). Analog loopback (ALB) couples the local transmitter output to the local receive input so that data sent from the local data terminal can be received by the local terminal and compared as required. Initiating remote digital loopback (RDLB) consists of transmitting data to the remote modem, which connects its receive output to its transmitter input. The remote modem then transmits the same data back to the originating modem, which processes it through its receive circuits to the local data terminal for comparison with the transmitted data. Response to remote test consists of connecting the receive output to the transmit input in response to initiation of remote test from the remote modem. Both remote test modes apply in 3400 mode only.

5.7.4 Direct Connect/Modem

The 787 terminal uses a dual-speed, answer/originate, full-duplex modem which can configure itself to Racal Vadic 3400, Bell 212 or 103-type formats. Selection of modem type is controlled by the terminal electronics PWB; selection can be made automatically via the autoselection algorithms or manually through forcing 3400, 212, or 103 mode. Interface of the modem to the telephone network can be either of two methods, direct-connect or acoustic. Acoustic interface can only be used in 3400 or 103 modes in originate mode. A simplified block diagram of the 787 modem is shown in Figure 5-17. Detailed schematics are located in Section 7 (2265842).

There are two operating modes of the modem: the control mode and data transfer mode. When the control mode is requested by the terminal electronics via the RCNTL control input signal, the modem unconditionally enters the control mode and responds with a status signal ACNTL to the terminal electronics PWB. During the control mode, the terminal electronics PWB and modem communicate via the -TXD and -RXD lines. The terminal electronics send a series of configuration and operating commands (including dialing) to the modem via the - TXD input and the modem responds with a series of status response codes to the terminal electronics via the -RXD output. All control mode communication by the modem is handled by the internal microprocessor. Upon receipt of the various commands from the terminal electronics, the microprocessor generates the appropriate hardware control signals to configure the modem circuits to the commanded state(s). When control mode communications have been completed, control mode is dropped by the terminal electronics deactivating RCNTL and the modem responds by deactivating ACNTL. When the control mode is dropped, the data transfer mode is entered.

Upon entry into the data transfer mode, the modem must determine which type of modem is answering or originating the call. If the modem is in the originate mode and the autoselect mode has been commanded by the terminal electronics, the modem microprocessor begins switching the configuration between 3400 and 103 (with the LOSPD and BELL control signals) at a 50-millisecond rate. If one of the forced modes is commanded by the terminal electronics, the microprocessor configures the modem for the commanded mode with the LOSPD or BELL control signals. In either case,

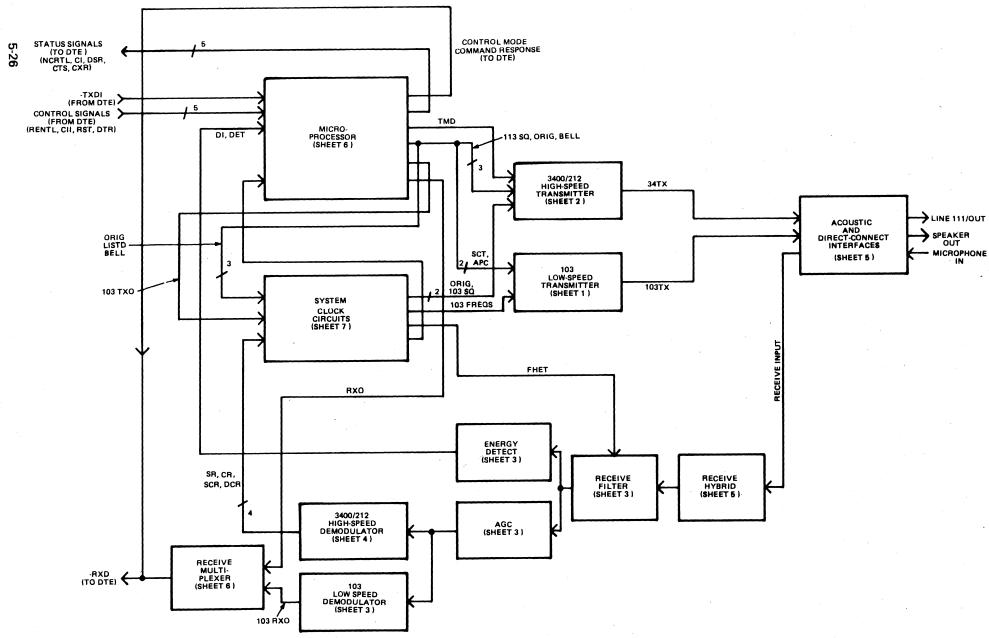


Figure 5-17. 787 Modem Simplified Block Diagram

the modem searches for receive input energy from the answering modem. The LOSPD, BELL, and ORIG control signals from the microprocessor controls the generation of the FHET heterodyne frequency (from the system clock circuits) which controls the carrier frequency that the receive filter network accepts. When receive energy from the answering modem arrives, it is coupled through the line interface circuit to the receive hybrid. From the hybrid, the receive signal is applied to the receive filter. If the receive filter is configured to accept the receive carrier frequency, the resulting filter output drives both the energy detect and AGC circuits.

The AGC circuit provides a standardized signal level to the 3400/212 high-speed and 103 lowspeed demodulator circuits. The energy-detect circuit provides the microprocessor with an indication that receive energy of the required level has been detected. When the microprocessor receives active energy detect plus the required period of detected MARK from the applicable demodulator circuit, the handshake routine is complete and an active CXR status signal is sent to the terminal electronics to indicate that a valid answering modem has answered the call. At the same time that the active CXR signal is generated, the microprocessor internally generates a MARK signal of the selected modem type (TMD for 3400/212 mode, 103 FREQS for 103 mode) and routes it to the appropriate transmitter circuit for application to the remote (answering) modem. After CTS delay, data transmission can begin at either end.

If the modem is in the answer mode, ringing voltage is detected on the telephone line and the call is answered either manually by the operator or automatically by the modem. With the modem configured for the autoselect mode, the microprocessor internally generates an answer tone sequence consisting of four seconds of 2225 Hz 103 MARK (answer tone), four seconds of 1150 Hz 3400 low-band MARK, 10 seconds of 2225 Hz 103 MARK, and four seconds of 1150 Hz 3400 low-band MARK. This sequence is accomplished by alternately generating 103 MARK in the 103 low-speed transmitter and 3400 MARK in the 3400/212 high-speed transmitter. If no receive energy is detected during the 4-4-10-4 answer mode sequence, the sequence repeats itself indefinitely. During the 4-4-10-4 sequence,

the receiver circuits are configured to detect 212 low-band scrambled MARK for the first four seconds, 3400 high-band MARK for the second four seconds, 103 low-band MARK for the third 10 seconds, and 3400 high-band MARK for the final four seconds. With the modem configured in one of the three forced-answer modes, the microprocessor internally generates four seconds of 2225 Hz 103 MARK (answer tone) for transmission to the remote (originating) modem via the 103 low-speed transmitter. If the forced modem type is 3400, the modem configures itself to 3400 mode (LOSPD and BELL low) after the four-second answer tone burst and transmits 3400 low-band MARK to the remote modem via the 3400/212 high-speed transmitter. If the forced modem type is a 212, the receive circuits of the modem are configured to search for low-band 212 scrambled MARK after the four-second answer tone burst. While searching for the scrambled MARK, the modem continues to transmit the 2225 Hz 103 high-band MARK to the remote modem. If the forced modem mode is a 103, the receive circuits of the modem are configured to search for lowband 103 MARK after the four-second answer tone burst. While searching for the low-band 103 MARK, the modem continues to transmit the 2225 Hz 103 high-band MARK to the remote modem. In either autoselect or forced-answer mode, however, the modem searches for receive input energy from the originating (remote) modem while transmitting its answer tone sequence.

The LOSPD, BELL, and ORIG signals from the microprocessor control the generation of the FHET heterodyne frequency (from the system clock circuits) which controls the carrier frequency that the receive filter network accepts. When receive energy from the originating modem arrives, it is coupled through the line interface circuit to the receive hybrid. From the hybrid, the receive signal is applied to the receive filter. If the receive filter is configured to accept the receive carrier frequency, the resulting filter output drives both the energy detect and AGC circuits. The AGC circuit provides a standardized signal level to the 3400/212 high-speed and 103 low-speed demodulator circuits. The energy-detect circuit provides the microprocessor with an indication that receive energy of the required level has been detected. When the microprocessor receives active energy detect plus detected MARK from the applicable demodulator circuit, the handshake routine is complete. Then, an active CXR status signal is sent to the terminal electronics to indicate that a valid originating modem has originated the call. At the same time that the active CXR signal is generated, the microprocessor internally generates a MARK signal of the selected modem type (TMD for 3400/212 mode, 103 FREQS for 103 mode) and routes it to the appropriate transmitter circuit for application to the remote (answering) modem. At this point, data transmission can begin at either end.

When the remote modem is a 3400, the 3400 portion of the 3400/212 high-speed transmitter circuits of the modem is used. Data from the terminal is routed to the modem via the -TXD input line at 1200 bps. The -TXD data in 3400 mode is asynchronous; the microprocessor contains an asynchronous-to-synchronous buffer which synchronizes the input data to the internallygenerated transmit clock (SCT) from the system clock circuits. The resultant synchronized data (TMD) from the microprocessor is encoded as dibits (two bits at a time) in the 3400 transmitter. Carrier frequency for the modulating (baseband) signals generated in the 3400 transmitter is supplied by the 4 F_c output of the system clock circuit. The resultant modulated carrier output of the 3400 transmitter is a DPSK (dibit-phase-shiftkeyed) signal; DPSK signals change the phase of the carrier by 0°, 90°, 180°, or 270°, depending upon the value of both the current and previous dibit information contained in the baseband signals. The modulated 3400 carrier is coupled to the acoustic and direct-connect interface circuit from which it is routed to the line output or speaker output, depending on the interface mode selected.

When the remote modem is a 212, the 212 portion of the 3400/212 high-speed transmitter circuits is used. Operation of the 212 transmitter circuit is similar to that of the 3400 circuit described previously. Differences are in carrier frequencies (1200 Hz or 2400 Hz for 212 mode), phase shift for given dibit values, and the insertion of a scrambler circuit which scrambles the TMD transmit data before application to the encoder of the 212 transmitter. Also, the 212 mode is not used when the modem is in acoustic-interface mode.

When the remote modem is a 103, the 103 lowspeed transmitter circuits of the modem are used. Data from the terminal electronics is routed to the modem via the —TXD input line at 300 bps. The 103 data is asynchronous; the microprocessor sends the data to the system clock circuits which generate the 103 MARK-SPACE frequencies (103 FREQS) to drive the 103 low-speed transmitter. The 103 low-speed transmitter generates the frequency-shift-keyed (FSK) 103 TX output signal. The FSK output of the 103 transmitter circuit is coupled to the acoustic and direct-connect interface circuit where it is routed to the line output or speaker output, depending upon the interface mode selected.

The receive circuits of the modem operate in the same manner during normal data transfer as that previously described for the handshake routines. The FHET heterodyne frequency output of the system clock circuits configures the receive circuits to accept the input carrier frequency transmitted from the remote modem. The standardized AGC output levels are applied to both the 3400/212 high-speed demodulator and 103 lowspeed demodulator circuit in parallel. When the receive signal is 103 data, the 103 low-speed demodulator circuit recovers the 103 baseband modulation signal and applies it to the receive multiplexer. If the receive signal is 3400 or 212 data, the 3400/212 high-speed demodulator circuit performs demodulation and carrier and clock recovery operations from which the dibit data is recovered. The resultant dibit data and associated clock signals are coupled to the system clock circuits where decoding into 1200 bps RXD is accomplished. From the system clock circuits, the high-speed RXD signal is routed to the microprocessor where it is synchronized to the applicable clock signal (and descrambled in 212 mode). The resultant 1200 bps RXD data stream is applied to the receive multiplexer. The applicable data signal from the multiplexer is then gated to the -RXD output which is routed to the terminal electronics.

Although not shown in the block diagram, provision is made for local test (analog loopback), initiated remote test (remote digital loopback), and response to remote test. Analog loopback (ALB) couples the local transmitter output to the local receive input so that data sent from the local data terminal can be received by the local terminal and compared as required. Initiating remote digital loopback (RDLB) consists of transmitting data to

the remote modem which connects its receive output to its transmitter input. The remote modem then transmits the same data back to the originating modem which processes it through its receive circuits to the local data terminal for comparison with the transmitted data. Response to remote test consists of connecting the receive output to the transmit input in response to initiation of remote test from the remote modem. Analog loopback can be entered in 3400, 212 and 103 modes, while both initiation of and response to remote test is restricted to 3400 and 212 modes.

5.8 FIRMWARE

The terminal operating system (firmware) is a multi-task, natural wait system consisting of interrupt processors, a scheduler, a clock routine and various system tasks. The operating system is stored in the terminal's ROM.

The terminal operates in a real-time environment, and the elements that are time-critical (i.e., which process events requiring action within a certain small period of time) are separated from the elements that process events on a time-available basis. The receiver, printer mechanism control, keyboard and system clock are events that are time-critical and are handled by interrupt processors. The remaining tasks run on a time-available basis and include print line analysis, the transmitter, various timeout protocols, ABM, and COMMAND Mode processing.

Section 6

Maintenance

6.1 INTRODUCTION

The 780 Series terminals are designed with several built-in test features to aid in quick isolation of failures. This section discusses the following procedures:

- Self-tests
- Reports
- Troubleshooting flowcharts
- Removal and replacement of terminal subassemblies
- Terminal adjustments
- Printhead cleaning

6.2 SELF-TESTS

The Model 780 terminals provide automatic selftest functions to verify correct terminal operation. Two types of self-tests are built into the terminals:

- Power-up diagnostics tests
- Maintenance tests

6.2.1 Power-Up Diagnostics Tests

The following sequence of tests is performed automatically by the terminal in the order indicated each time power is applied to the terminal.

6.2.1.1 Indicator Test. The indicator test is initiated at the beginning of the power-up sequence. The LED indicators are illuminated and

remain on until the power-up sequence is completed (approximately two seconds).

6.2.1.2 RAM Test. The terminal processor exercises the random-access memory to verify that data can be written to and read from each memory location. If an error is detected, a RAM failure error code is activated and is reported via the long bell tone and the flashing ERR/TEST indicator. If a RAM failure is detected, the operating system attempts to run with the remaining, good, lower order RAM devices as indicated by the CR report (paragraph 6.3.3). If the detected failure is in RAM 0, the terminal should not be operated before being repaired. The processor proceeds to the next test, but there is no assurance that subsequent test results are valid if this test fails.

6.2.1.3 ROM Test. The terminal processor performs a cyclic redundancy character (CRC) check of the read-only memory. If the results of the CRC check are unsatisfactory, a ROM failure error is activated. The processor proceeds to the next test, but subsequent test results may not be valid if this test fails. (Operation of the terminal is not recommended if this test fails.)

6.2.1.4 Nonvolatile Memory Test. The terminal processor computes the CRC of the contents of the nonvolatile memory (configuration parameters). If an error is found, the processor reloads the configuration memory with default parameters, proceeds to operate with the default parameters, and activates a nonvolatile memory error code.

6.2.1.5 Mechanism Test. On completion of the memory tests, the terminal controller causes the printhead to step to the left margin and print

the model number of the terminal. If any powerup test failures occurred, the audible tone sounds for one second, and the ERR/TEST indicator flashes until reset. the operator interface. A maximum of nine maintenance tests are available, depending on the model. Table 6-1 lists the tests that are available on each terminal.

6.2.2 Maintenance Tests

The maintenance tests are manually initiated from

Table 6-1. Maintenance Tests

Test	Test		M	Terminal			
Number	,	781			787	Status	
0	Transmit level			×	x	Online	
1	Power-up	x	×	x	x	Local	
2	Local barberpole	х	×	, x	x	Local	
3	Transmit check		x	х	x	Online	
4	Remote digital loopback			x	x	Online, Connected	
5	Analog loopback			х	x	Online, Not Connected	
6	Transmit barberpole	×	×	×	x	Online	
7	Transmit with error checking		x	х	х	Online	
8	Mechanism alignment	х				Local	
9	CR Report (for 781 only)	х				Local	
Α	Mechanism alignment		х	х	×	Local	

6.2.2.1 Transmit Level Test. This test is used both to verify operation of the speaker in the acoustic muff, and its electronic driver, as well as to calibrate the transmit level of the selected internal modem in the Model 785 or 787. This test may also be used with tests 3 or 6 or with data entered from the keyboard. During this test, the modem receiver is inhibited. Proper calibration is 94 dBSPL \pm 3 dB for 3400 originate mode operation.

6.2.2.2 Power-Up. This test executes the Power-Up Tests described in paragraph 6.2.1. The test terminates automatically and prints the model number of the terminal. Failures are indicated by the sounding of the long bell tone and flashing of the ERR/TEST indicator. The results of the memory test are contained in the ERROR and CR reports.

6.2.2.3 Barberpole Test. This test prints a barberpole pattern at a speed depending on the communications rate selected. At 1200 bps or greater, the printer prints at the maximum print rate. Below 1200 bps, the printer prints at 30 cps. When *code* 29 is enabled, the printer prints at the maximum print rate when the terminal is OFFLINE or according to the selected communications rate when ONLINE. A typical barberpole test pattern is illustrated in Figure 6-1.

6.2.2.4 Transmit Check. This test executes repeated transmission of the last keyboard character to the selected interface at the configured rate. The modem to be checked (103 vs 212/3400) is selected by speed as described in paragraph 6.2.2.6. A new entry from the keyboard changes the transmit character. Any data received during this test is printed. The transmit check is helpful in providing an on-board data source for use in conjunction with remote digital loopback

and analog loopback tests available on the 785 and 787 models.

NOTE

Due to the modulation technique of the 3400 modem, a repeated stream of ASCII "U" characters, with even parity, may cause false failure of the loopback test(s), due to synchronization drift.

6.2.2.5 Initiate Remote Digital Loopback (RDLB) Test. This test is used with test 3, 6 or 7 or with data entered from the keyboard for testing the Models 785 and 787 with the 212/3400 modem after communications are established. If the remote loop cannot be established, error 32 is set and the long bell tone is sounded. Figure 6-2 depicts the test setup for the RDLB test.

 $\label{eq:abcdef} ABCDEFGHIJKLMNDPQPSTUVWXYZ[\]^_\abcdefahijklmnoparstuvwxyz(\)^* !"o$%&<O ++,-...012 BCDEFGHIJKLMNDPQRSTUVWXYZ[\]^_\abcdefahijklmnoparstuvwxyz(\)^* !"o$%&<O ++,-...0123 CDEFGHIJKLMNDPQRSTUVWXYZ[\]^_\abcdefahijklmnoparstuvwxyz(\)^* !"o$%&<O ++,-...0123 BEFGHIJKLMNDPQRSTUVWXYZ[\]^_\abcdefahijklmnoparstuvwxyz(\)^* !"o$%&<O ++,-...012345 EFGHIJKLMNDPQRSTUVWXYZ[\]^_\abcdefahijklmnoparstuvwxyz(\)^* !"o$%&<O ++,-...0123456 FGHIJKLMNDPQRSTUVWXYZ[\]^_\abcdefahijklmnoparstuvwxyz(\)^* !"o$%&<O ++,-...01234567 GHIJKLMNDPQRSTUVWXYZ[\]^_\abcdefahijklmnoparstuvwxyz(\)^* !"o$%&<O ++,-...01234567 HIJKLMNDPQRSTUVWXYZ[\]^_\abcdefahijklmnoparstuvwxyz(\)^* !"o$%&<O ++,-...012345678 IJKLMNDPQRSTUVWXYZ[\]^_\abcdefahijklmnoparstuvwxyz(\)^* !"o$%&<O ++,-...0123456789 IKLMNDPQRSTUVWXYZ[\]^_\abcdefahijklmnoparstuvwxyz(\)^* !"o$%&<O ++,-...0123456789 IKLMNDPQRSTUVWXYZ[\]^_\abcdefahijklmnoparstuvwxyz(\)^* !"o$%&<O ++,-...0123456789 IKLMNDPQRSTUVWXYZ[\]^_\abcdefahijklmnoparstuvwxyz(\)^* !"o$%&<O ++,-...0123456789 IKLMNDPQRSTUVWXYZ[\]^-\abcdefahijklmnoparstuvwxyz(\)^* !"o$%&<O ++,-...0123456789 IKLMNDPQRSTUVWXYZ[\]^-\abcdefahijklmnoparstuvwxyz(\)^* !"o$%&<O ++,-...0123456789 IKLMDPQRSTUVWXYZ[\]^-\abcdefahijklmnoparstuvwxyz(\)^*

Figure 6-1. Barberpole Example

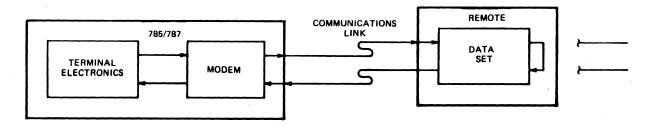


Figure 6-2. RDLB Test Setup

6.2.2.6 Initiate Analog Loopback (ALB) Test. This test is used with test 3, 6 or 7 or with data entered from the keyboard when the terminal is ONLINE but not connected. If the terminal is configured for 300 bps, the 103 (FSK) portion of the modern is tested. If the terminal is configured

for a higher rate, the 212/3400 (PSK) portion of the modem is tested. After the test is initiated, the rate can be changed to any rate that is compatible with the selected modem type. Figure 6-3 depicts the test setup for the ALB test.

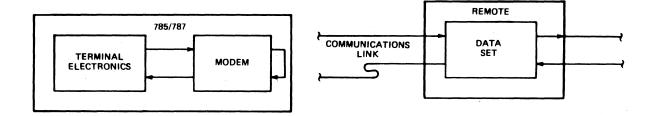


Figure 6-3. ALB Test Setup

6.2.2.7 Barberpole Transmit Test. This test transmits the barberpole pattern to the selected interface at the configured rate. Data received during this test is printed.

6.2.2.8 Barberpole with Error Check. This test transmits the barberpole pattern to the selected interface and compares the received data with the transmitted data. Data received during this test is not printed. When errors are detected, the short bell tone sounds. The error count is printed as part of the Customer Representative (CR) report (refer to subsection 6.3).

6.2.2.9 Mechanism Performance Test. This test verifies the performance of the printer mechanism and should be used whenever the printhead is changed. While running the test, check the column alignment of the ones and zeros being printed. If the headlift on the mechanism is correct (0.889 \pm 0.127 mm or 0.035 \pm 0.005 in.) and the misalignment from row to row is greater than 0.381 mm (.015 in.), the alignment should be adjusted using the pot on the sensor PWB, attached to the rear of the printhead stepping motor. Also verify that the tops and bottoms of the zeros are being printed; if they are not, clean

the printhead and repeat the test. If the tops or bottoms of the zeros are still not being printed, adjust the carriage rod up or down, as required, and repeat the test.

If carriage jam errors occur during this test (indicated by the flashing of the "ERR/TEST" indicator, long bell tone, and error code 11), verify column alignment and headlift. If column alignment and headlift are correct and carriage jam errors still occur, replace the mechanism.

6.2.3 Test Procedure Instructions

The following procedure is used to execute the previously described tests:

Model 781:

Set the terminal ONLINE or LOCAL according to the test requirements.

Depress TEST. The terminal responds with the prompt #.

Enter the desired test number or letter.

Terminate the test by depressing RESET.

Models 783, 785, 787:

Set the terminal ONLINE or LOCAL according to the test requirements.

Depress CMD. The terminal responds with the prompt .

Enter T or t for TEST. The terminal responds with the prompt #.

Enter the desired test number or letter. When test 3, 6 or 7 is used to generate data for tests 4 and 5, it is necessary to depress CMD, T or t and the desired number (3, 6 or 7) to start the test.

Terminate the test by depressing RESET.

6.3 REPORTS

Printed reports are available which provide information on the current configuration parameters, hardware status and terminal errors. The available reports are:

- CONFIG report
- ERROR report
- Customer Representative (CR) report

In the 783/785/787, a consolidated report is printed in numeric sequence beginning with report

number 1 when the report function is terminated by using ENTER or CR (carriage return).

Printing of the report resets the error status flags.

Completion of the requested report terminates the COMMAND Mode.

6.3.1 CONFIG Report

This report prints the configuration report as described in paragraph 3.3.2. In the 781, the report is printed when the CNFG key is pressed. For the 783/785/787, the configuration report can be requested by using the report function (Report 1) or the configure function.

6.3.2 ERROR Report

This report prints the error report in one of the following formats:

- CR LF ERRORS: S1, S2, ...; SN CR LF where S1 through SN are any enabled error status codes as described in paragraph 3.4.1.
- CR LF ERRORS: NONE CR LF

The 781 prints an error report only if an error is indicated, when the RESET key is pressed.

For the 783/785/787, an error report can be requested by using the report function (Report 2).

6.3.3 CR Report

This report provides pertinent information for maintenance personnel to isolate failures to the board level. The report prints the terminal hardware configuration in the following format:

NN AA BB CC DD OO PP HH II FG (X1 X2 Y1 Y2 Y3 Z1 Z2)*

w	n	Δ	rΔ	۰

NN = A two-digit hexadecimal identification number for the ROM set installed in the terminal.

AA = A two-digit hexadecimal number representing the revision level of ROM 1.

BB = A two-digit hexadecimal number representing the revision level of ROM 2.

CC = A two-digit hexadecimal number representing the revision level of ROM 3.

DD = A two-digit hexadecimal number representing the revision level of ROM 4.

OO = A two-digit hexadecimal identification number for ROM 5. This ROM is used for patches or options.

PP = A two-digit hexadecimal number representing the revision level of ROM 5.

HH = A two-digit hexadecimal number representing the identification number of the PROM installed in the terminal.

II = A two-digit hexadecimal number representing the revision level of the PROM installed in the

F = A one-digit hexadecimal number with a bit assigned to each possible RAM in the system. A one in the assigned bit indicates that the corresponding RAM is installed. Bit assignments are as shown:

RAM 3 RAM 2 RAM 1 RAM 0

G = A one-digit hexadecimal number with a bit assigned to each possible RAM in the system. A one in the assigned bit indicates that the corresponding RAM has been checked good by either the power-up test or TEST 1. Bit assignments are the same as in "F".

NOTE

If DD, OO, PP, HH, or II is greater than 7F hex, then the ROM or PROM represented by that identifier is not installed. Therefore, the highest PROM or ROM ID or revision is 7F hex.

^{*}The information in parentheses is valid only for 785/787 terminals.

This information pertains to 785/787 terminals:

X1, X2 = Two-digit hexadecimal number representing the internal modem functions that are installed in the terminal. Bit assignments are shown below.



where:

M = X, Y or Z and N = 1, 2, or 3.

X1(0) = 3400 Originate-only

X1(1) = 3400 Answer/originate

X1(2) = 212 Answer/originate

X1(3) = 103 Originate-only

X1(4) - X1(7) = Not used

X2(0) = 103 Answer/originate

X2(1) = Tone dial installed

X2(2) = Acoustic interface

X2(3) = Direct connect interface

X2(4) - X2(7) = Not used

Y1, Y2, Y3 = Two-digit hexadecimal numbers representing the current status of the internal modem. Bit assignments are shown below.

Y1(0) = On hook

Y1(1) = Off hook

Y1(2) = In RDLB

Y1(3) = 3400 Originate

Y1(4) = Y1(7) Not used

Y2(0) = 3400 Answer

Y2(1) = 212 Originate

Y2(2) = 212 Answer

Y2(3) = 103 Originate

Y2(4) - Y2(7) = Not used

Y3(0) = 103 Answer

Y3(1) = Forced idle

Y3(2) - Y3(7) = Not used

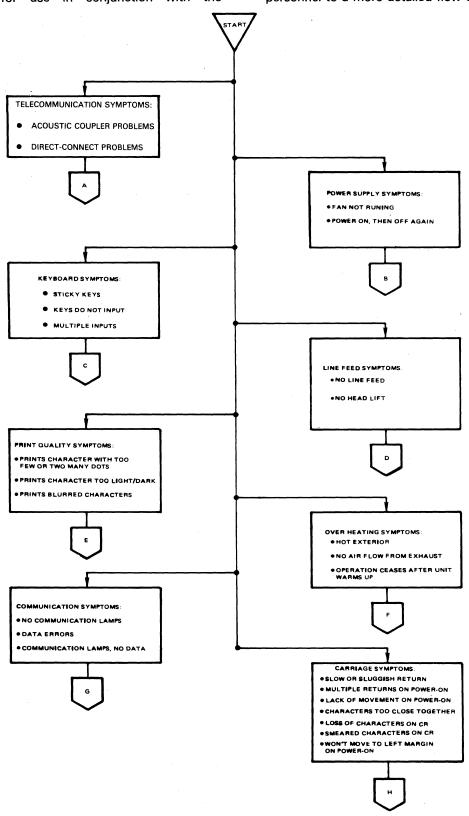
Z1, Z2 = The number of errors that have occurred since the start of TEST 7, expressed as a four-digit hexadecimal number.

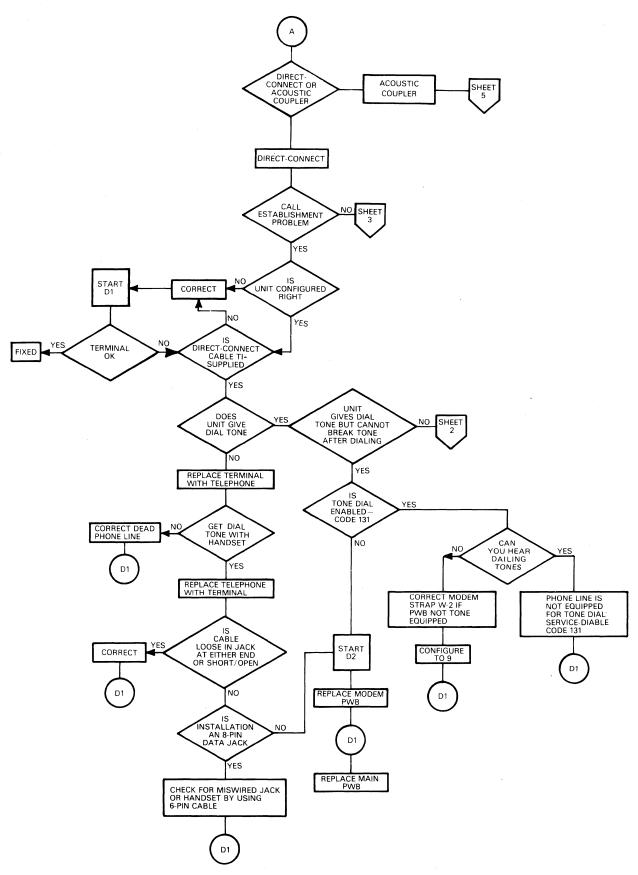
The CR report is requested using TEST 9 on the 781 and Report 0 on the 783/785/787.

6.4 TROUBLESHOOTING FLOW DIAGRAMS

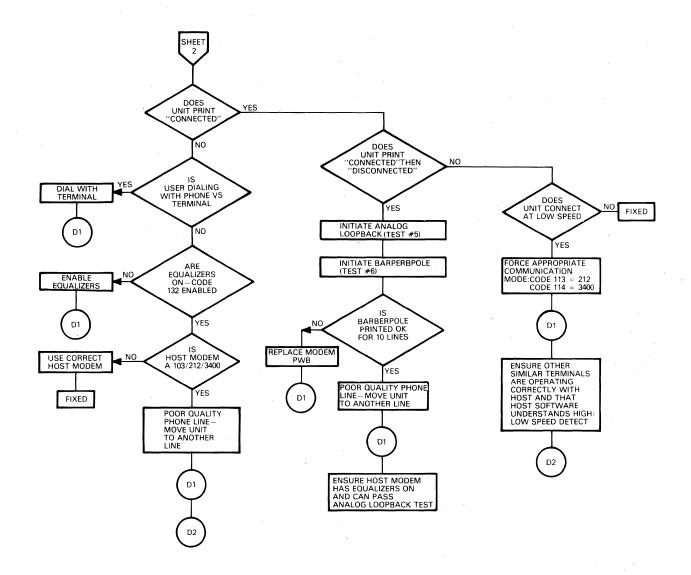
This section contains troubleshooting flow diagrams for use in conjunction with the

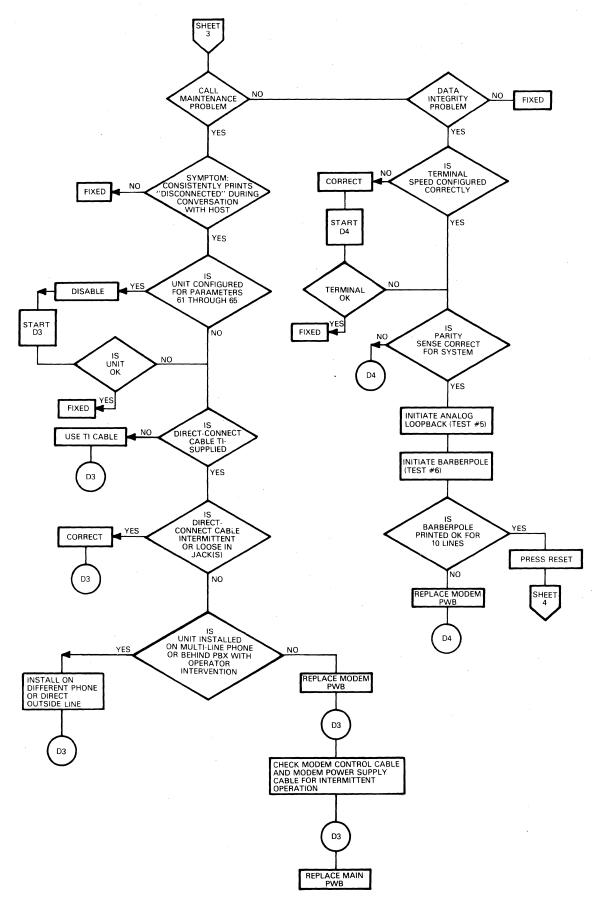
maintenance tests and the CR report to isolate failures to a specific board. The first diagram defines major symptoms and refers maintenance personnel to a more detailed flow diagram.



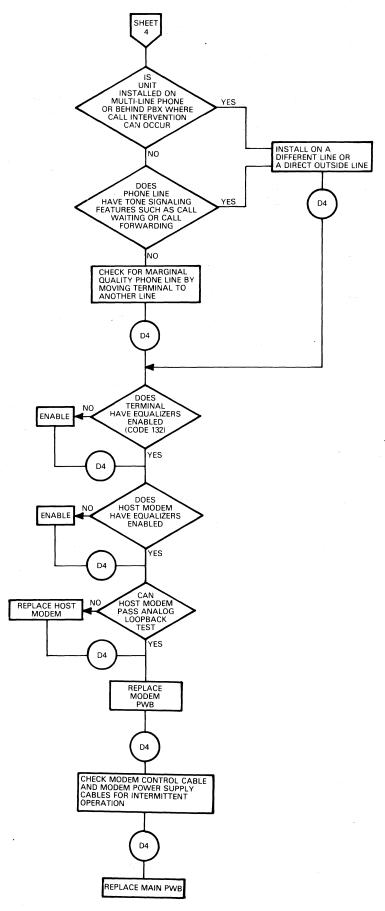


Troubleshooting Flow Diagrams

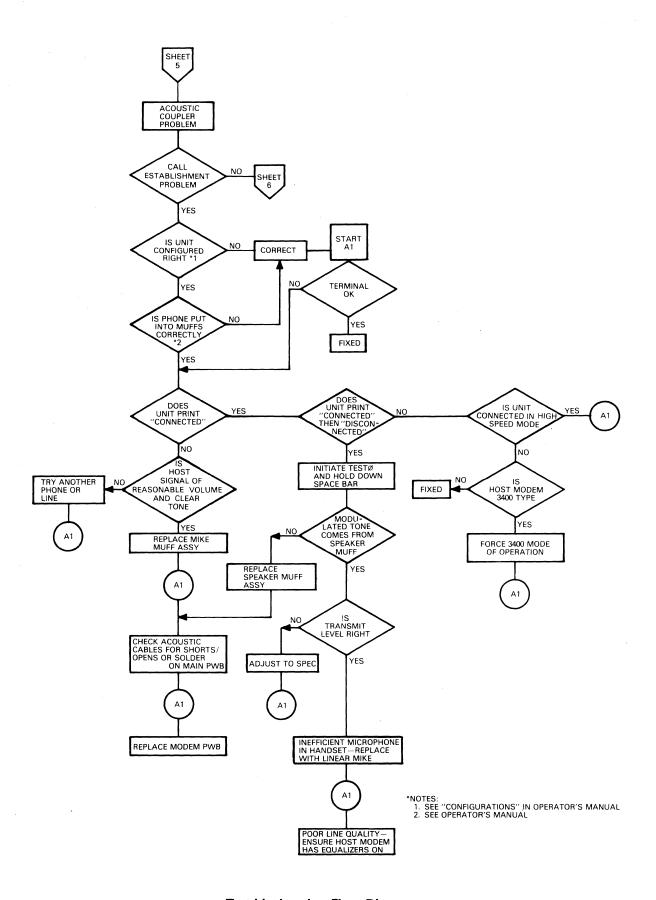




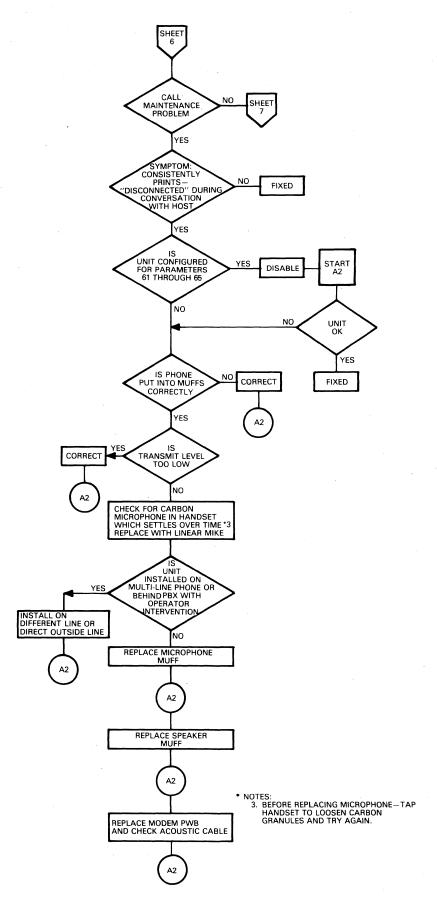
Troubleshooting Flow Diagrams



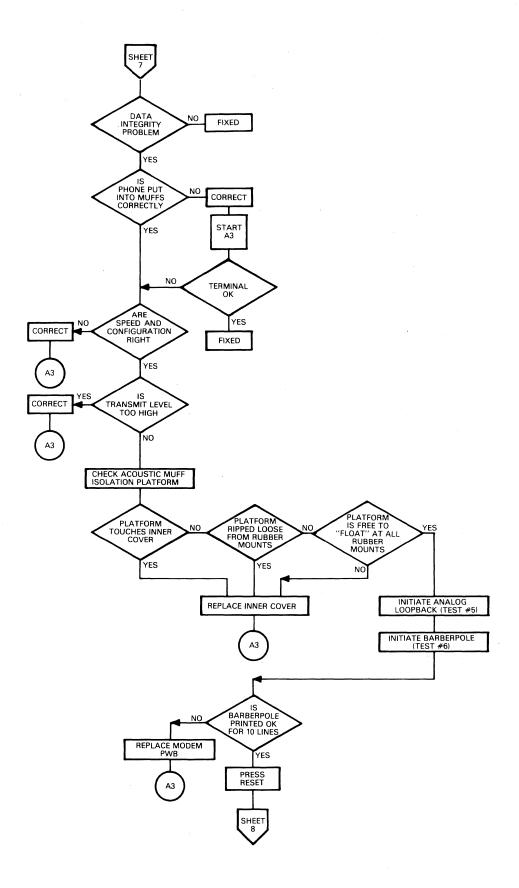
Troubleshooting Flow Diagrams



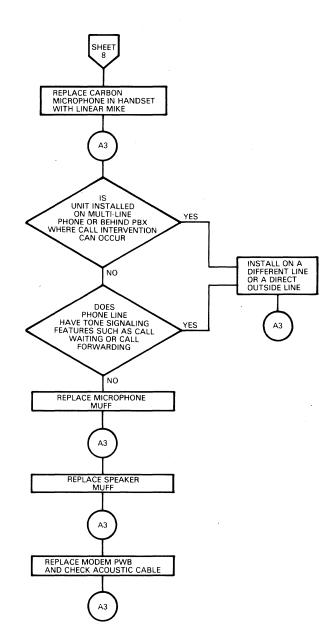
Troubleshooting Flow Diagrams

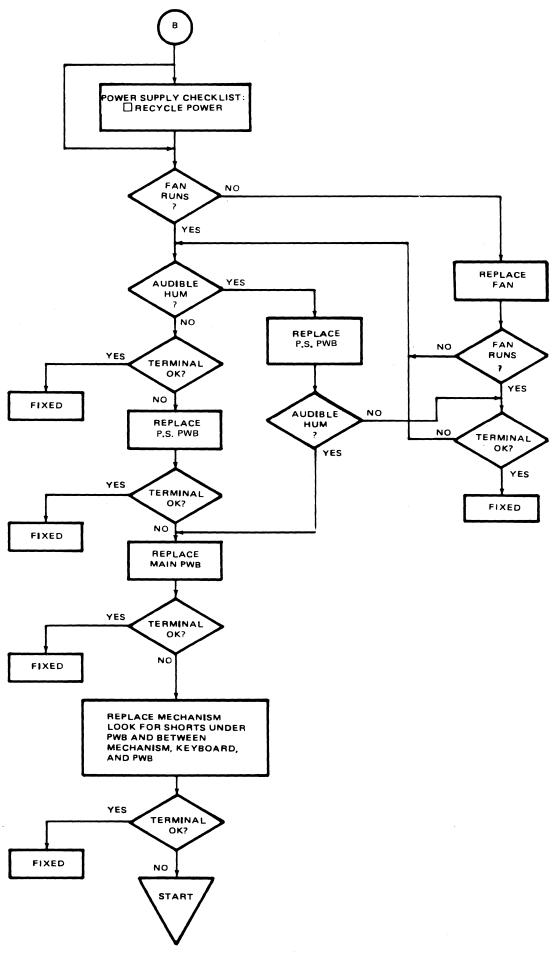


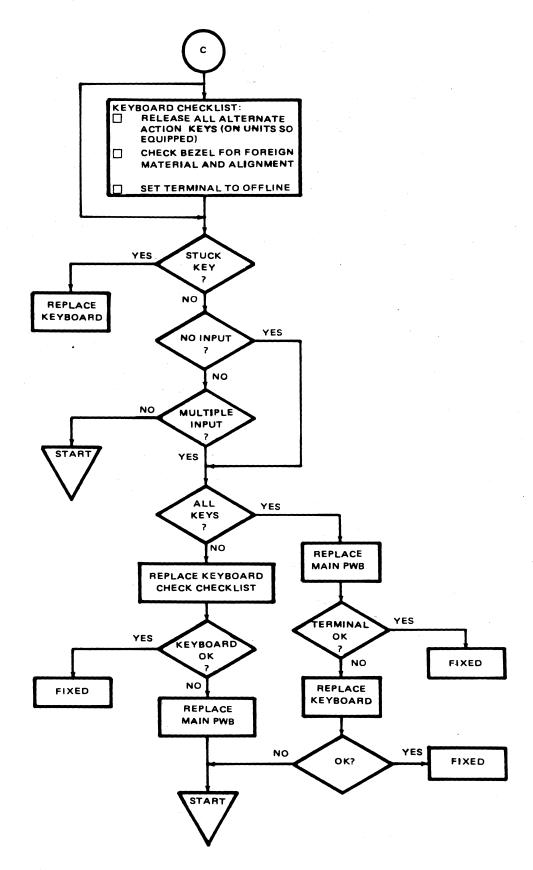
Troubleshooting Flow Diagrams



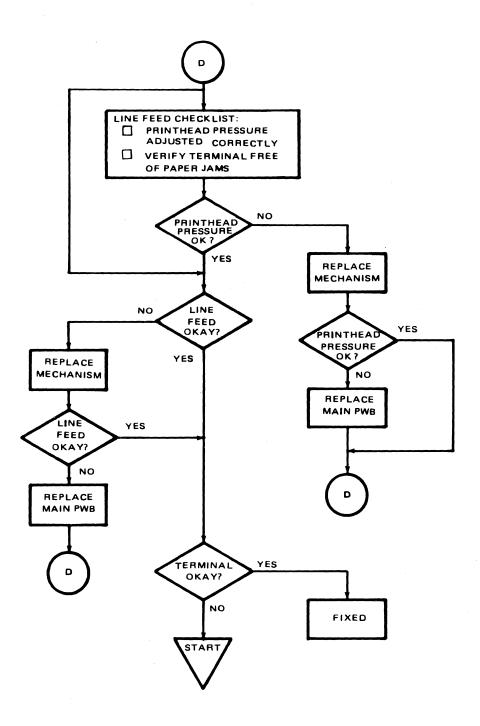
Troubleshooting Flow Diagrams



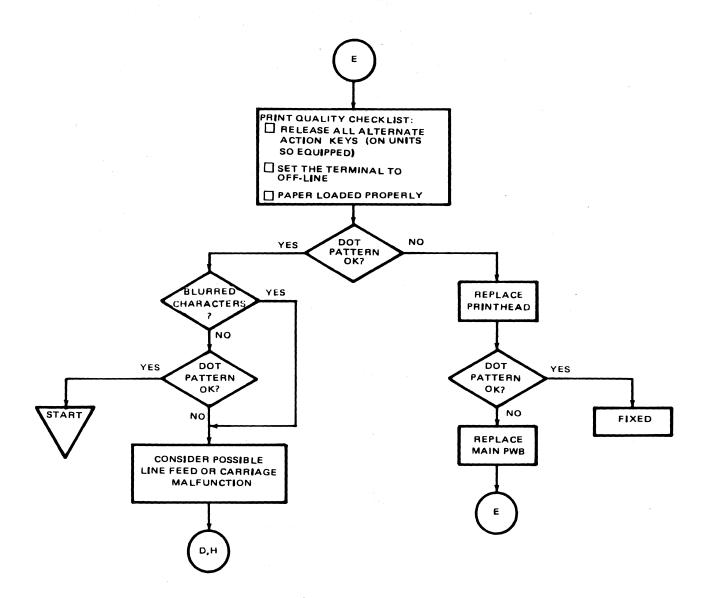


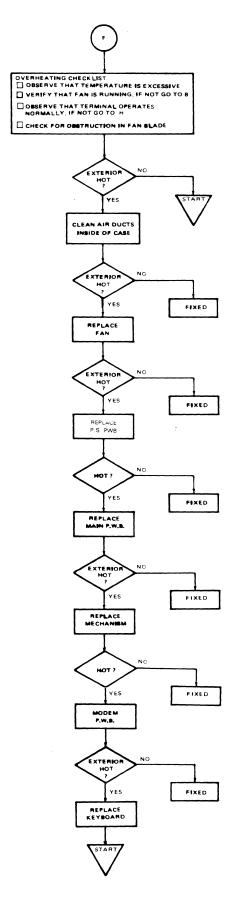


Troubleshooting Flow Diagrams

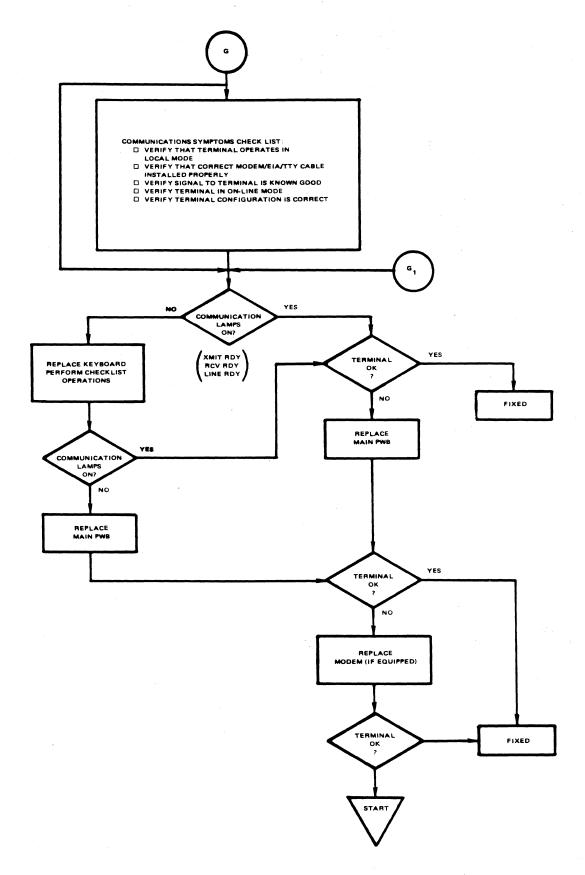


Troubleshooting Flow Diagrams

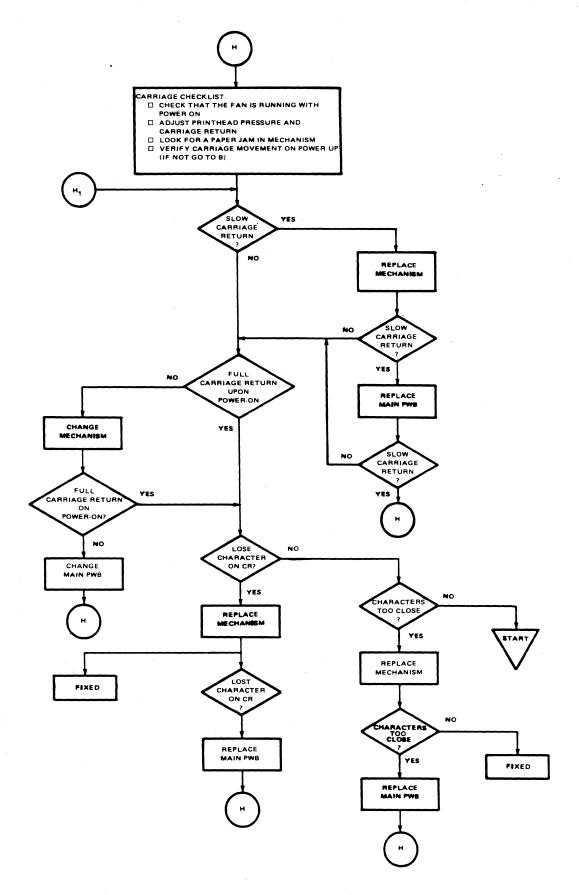




Troubleshooting Flow Diagrams



Troubleshooting Flow Diagrams



Troubleshooting Flow Diagrams

6.5 SUBASSEMBLY REPLACEMENT

The modular-designed subassemblies may be easily removed to facilitate repair or replacement. Figures 6-4, 6-5, and 6-6 show the important modules and their attachment and plug-in points. Detailed procedures are contained in the following subsections.

WARNING

Disconnect the data terminal ac power cord from the wall receptacle before attempting any internal disassembly procedures. The top board and power supply board contain high voltage.

6.5.1 Terminal Cover

Remove the terminal cover as follows:

- Disconnect the power cord and communications cable (if attached) from the rear of the terminal.
- 2. Open the paper supply door and remove any paper from the terminal.
- 3. Place the terminal upside-down on a padded working surface.
- 4. Remove the four recessed screws which secure the base to the cover.
- Firmly grasp the cover and base together and turn the terminal right-side up.
- Carefully lift the cover up and off the terminal.

NOTE

Terminals equipped with an acoustic coupler have two cable assemblies located inside the case at the rear of the terminal which must be disconnected. To disconnect, simply remove the two connecting plugs (P401, P402) attached to the modem PWB. **DO NOT** disconnect by pulling on the wires; grasp the connectors manually or use small needle-nose pliers.

Replace the terminal cover as follows:

- Set the terminal cover on its back, to the rear of the terminal base.
- On terminals equipped with acoustic couplers, connect the two acoustic coupler connectors (J401, J402) to the modem PWB.
- Verify that the fan, printer mechanism, printhead, keyboard, power supply PWB and modem PWB (if so equipped) cables are connected to their upper PWB connector pins.
- 4. Verify that the power cord receptacle is inserted in its groove in the terminal base.
- 5. Lower the front of the cover, keeping cables and wires off the heatsink and away from the fan blades.
- Guide the paper compartment rear wall (on the terminal cover) into the slot at the bottom rear of the mechanism paper supply compartment.
- 7. Verify that the sides, front, and rear of the cover are engaged in their respective grooves in the base.
- 8. Grasp the cover and base together and turn the terminal upside down.
- 9. Install the four screws through the base and tighten.

6.5.2 Printer Mechanism

Remove the printer mechanism as follows:

- 1. Remove the terminal cover as described in paragraph 6.5.1.
- Disconnect the printer mechanism sensor and motor connector, paper advance motor connector, headlift solenoid, paper-out detector (if installed) and the mechanism ground connector (see Figure 6-4).

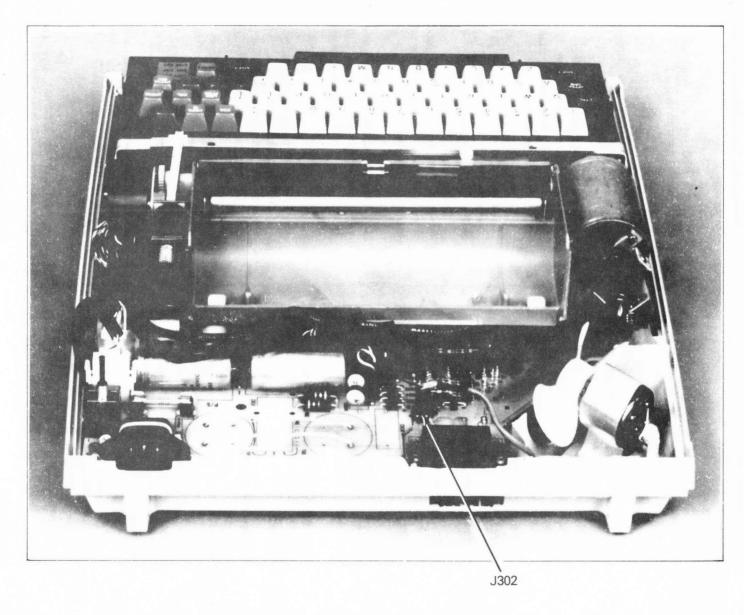


Figure 6-4. Internal Connector Locations

NOTES

Grasp only the plastic bodies of the connectors when disconnecting. DO NOT pull on the wires. Needle-nose pliers may be used if more convenient.

The printer mechanism is shockmounted and will lift up without any difficulty.

- Lift the entire mechanism approximately 100 mm (4 inches) and unplug the printhead connector (P5) from the main PWB. The connector is located below the mechanism.
- Lift the printer mechanism from the terminal.

Replace the mechanism as follows:

- Verify that the four spaces are seated atop each of the four mechanism mounting posts.
- 2. Hold the printer mechanism above the main PWB and connect the printhead connector to J5 on the PWB.
- Route the motor and sensor cables (P201, P1) under the mechanism and behind the left rear mounting post.
- 4. Connect the sensor cable to J1 and the motor cable to J201. Refer to Figure 6-4 and connect the printhead solenoid connector (P251) to J251 and the line feed stepper motor connector (P204) to J204. Connect the mechanism ground cable to the tab located beneath the line feed stepper motor.
- Lower the mechanism over the mounting posts and press down firmly on the mechanism to ensure proper seating of the mechanism on the shock-mounts.
- 6. Replace the terminal cover as described in paragraph 6.5.1.

6.5.3 Printhead

Remove the printhead as follows:

- 1. Remove the terminal cover as described in paragraph 6.5.1.
- 2. Remove the printer mechanism as described in paragraph 6.5.2.
- 3. Remove the plastic clip that holds the flat flexible ribbon cable to the printer mechanism (Figure 6-5).
- Release the pressure bar assembly (Figure 6-8) by disconnecting the plastic solenoid linkage at the point where it attaches to the pressure bar assembly.
- Carefully remove the E-clip that holds the carriage wheel. Be sure that it does not fall into the mechanism or electronics.
- Loosen the two printhead mounting screws that secure the printhead to the carriage assembly.
- Lift the clear plastic window grasp the printhead assembly pulling up and back until it is clear of the two plastic aligning tabs.
- Gently remove the printhead assembly (if the printhead does not come off, repeat steps 6 and 7) and let the clear plastic window return to its resting position against the platen.

Replace the printhead as follows:

- Lift the clear plastic window.
- Slide the printhead into position onto the printhead carriage. Ensure that the two plastic pins fit into the holes on the printhead assembly.
- 3. Tighten the two screws that retain the printhead assembly.
- 4. Replace the carriage wheel and E-clip that retains the wheel.

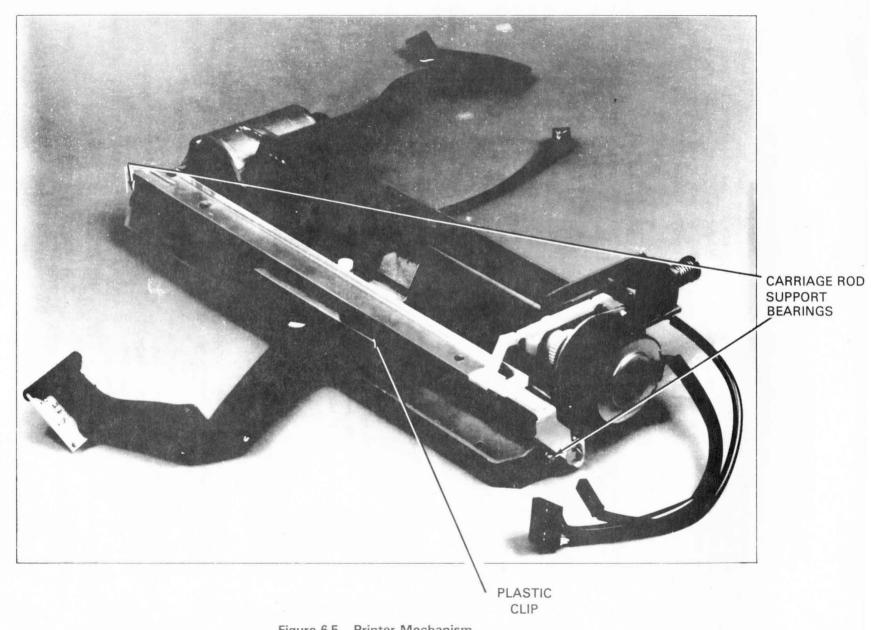


Figure 6-5. Printer Mechanism

- 5. Adjust the printhead pressure as instructed in paragraph 6.6.1.
- Lay the flexible cable under the printhead with a rolling loop to the left and ensure the cable is parallel with the front lip of the mechanism frame, as close to the mechanism frame lip as possible.
- 7. Secure the flexible cable to the mechanism with the plastic clip.
- 8. Install the mechanism in the terminal as instructed above in paragraph 6.5.2.
- 9. Adjust the printhead alignment as instructed in paragraphs 6.6.1 and 6.6.2.
 - 10. Replace the terminal cover as described in paragraph 6.5.1.

6.5.4 Keyboard

Remove the keyboard as follows:

- 1. Remove the terminal cover as described in paragraph 6.5.1.
- 2. Remove the keyboard bezel releasing the snap-on posts on the left and right ends of the keyboard and the bezel (Figure 6-6).
- Press the keyboard assembly toward the rear of the terminal until the three front retainer clips are free of the keyboard.
- Lift the front of the keyboard assembly up and slide the keyboard forward off the terminal.
- Holding the keyboard in one hand, place the index finger of the other hand under the flat keyboard ribbon connector. Gently pull up on the keyboard cable connector until it is free of the keyboard.

Replace the keyboard as follows:

 Lay the keyboard in front of the terminal and connect the keyboard ribbon cable connector to the keyboard.

NOTE

Take special care when installing the keyboard flex cable connector. The connector pins are made of a thin metal and are easily bent or broken. Verify that all pins are in their respective sockets of the connector before applying pressure.

- Lift the keyboard and inset the rear edge into the three rear keyboard clips of the base while gently folding the cable beneath the keyboard.
- Push the keyboard toward the rear of the terminal until the front clips of the base are clear. Lower the front edge of the keyboard and insert the front edge into the three front clips.
- Install the keyboard bezel by pushing down on the bezel until the two end posts snap into place.
- 5. Replace the terminal cover as described in paragraph 6.5.1.

6.5.5 Fan Assembly

Remove the fan assembly as follows:

- 1. Remove the terminal cover as described in paragraph 6.5.1.
- 2. Unplug the fan connector (P302) from the main PWB at J302 (Figure 6-4).
- 3. Loosen both fan bracket screws.
- 4. Slide the fan motor and blades forward and out of the bracket.

Replace the fan assembly by reversing the order of removal.

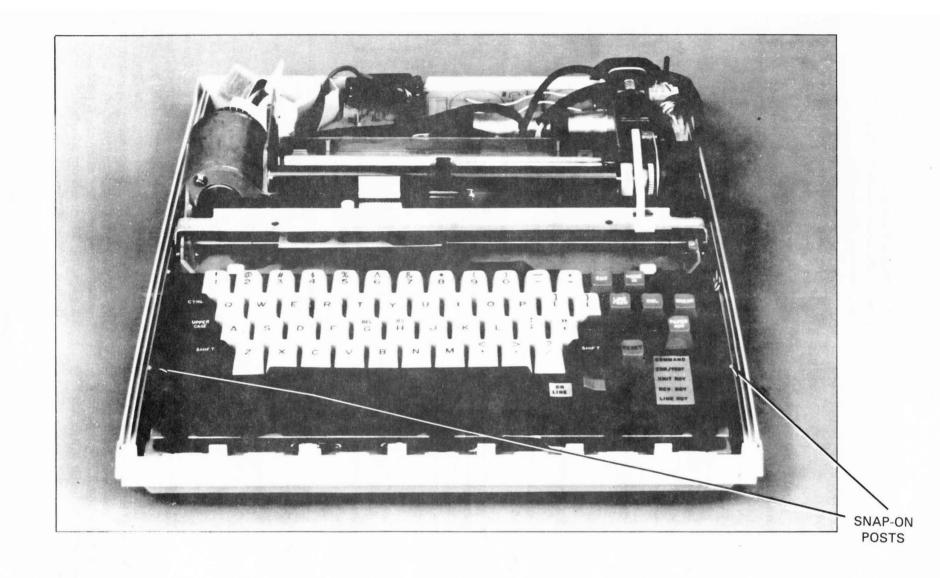


Figure 6-6. Keyboard Removal

6.5.6 Battery

Replace the battery as follows:

- 1. Remove the terminal cover as described in paragraph 6.5.1.
- 2. Remove the printer mechanism as described in paragraph 6.5.2.
- Disconnect the battery connector (P4) from the main PWB.
- 4. Remove the battery from the battery PWB and remove any remnants of double-sided tape.

Replace the battery by reversing the order of removal.

6.5.7 Main PWB

Remove the main PWB as follows:

- 1. Remove the terminal cover as described in paragraph 6.5.1.
- 2. Remove the printer mechanism as described in paragraph 6.5.2.
- 3. Disconnect the two interboard connectors P603 and P604 (Figure 6-7).
- 4. Remove four spacers (Figure 6-7).
- Slide the ac power receptacle out of its mounting slots.
- 6. Remove the main PWB by lifting it straight up.

Replace the main PWB by reversing the order of removal.

CAUTION

When replacing the main PWB, verify that the black conductive foam has been removed from the underside of the board. Damage to the terminal could result if it is not removed.

6.5.8 Power Supply PWB

Remove the power supply PWB using the following procedures (Figure 6-8):

- 1. Remove the terminal cover as described in paragraph 6.5.1.
- 2. Remove the printer mechanism as described in paragraph 6.5.2.
- 3. Remove the main PWB as described in paragraph 6.5.7.
- 4. Remove the power supply PWB by lifting it straight up.

Replace the power supply PWB reversing the order of removal.

6.5.9 Modem PWB

Remove the modem PWB as follows:

- 1. Remove the terminal cover as described in paragraph 6.5.1.
- 2. Remove the printer mechanism as described in paragraph 6.5.2.
- 3. Remove the main PWB as described in paragraph 6.5.7.
- 4. Remove the modem PWB by lifting it straight up.

Replace the modem PWB by reversing the order of removal.

6.6 TERMINAL ADJUSTMENTS

Under normal operating conditions, the closed-loop control circuitry of the printer mechanism compensates for friction changes caused by wear, temperature variations, and component aging. No field adjustments are required except alignment of the thermal printhead after replacement of the mechanism or printhead assembly. If print quality deteriorates, do not attempt adjustments until the cause is fully understood.

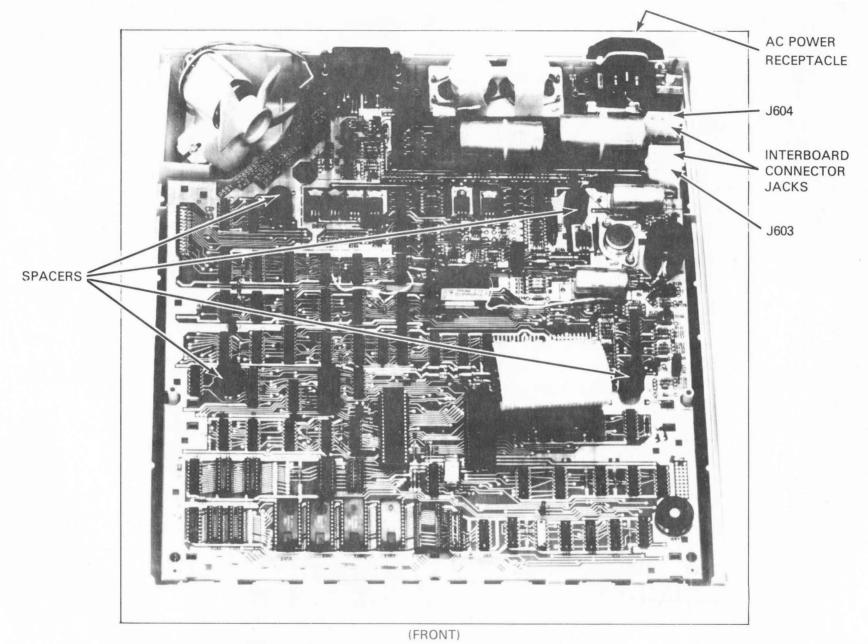
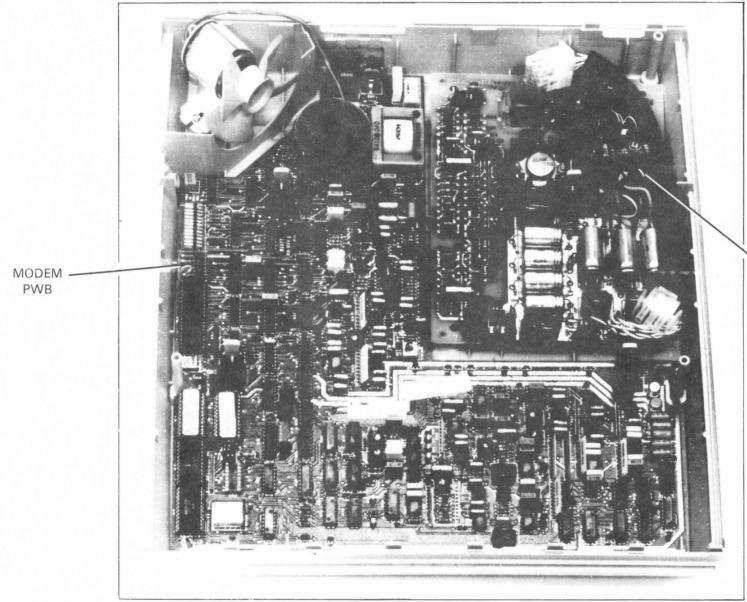


Figure 6-7. Interboard Connector and Spacer Locations



POWER SUPPLY PWB

(FRONT)

Figure 6-8. Power Supply and Modem PWB'S

6.6.1 Printhead Pressure Adjustment

Adjust the printhead pressure as follows:

- 1. Remove the terminal cover as described in paragraph 6.5.1.
- 2. Manually slide the printhead approximately 100mm (4 inches) from the left margin.
- Press the printhead lift solenoid (Figure 6-8) so that the solenoid is in the fully energized position.
- Place a measuring device along the solenoid linkage and measure the travel distance.
- 5. Adjust the solenoid travel to at least 0.5mm (0.02 inches) but no greater than 1.1mm (0.045 inches) by rotating the knurled solenoid adjustment wheel (Figure 6-8). Rotate the wheel clockwise to increase printhead travel, counterclockwise to decrease travel.
- Repeat steps 3 through 5 several times to make certain that the adjustment is correct.

6.6.2 Printhead Alignment

After installing a new printhead, check a printed line of zeros. If the tops or bottoms are missing anywhere along the printed line, correct by repositioning the printhead carriage rod support bearings (Figure 6-5) as follows:

- 1. Remove the terminal cover as described in paragraph 6.5.1.
- Loosen the screw that clamps the bearing to the frame. Move the bearing up if the bottoms of the characters are missing, or down if the tops of the characters are missing. Independently adjust each end of the carriage rod support for the condition observed.
- After adjusting, verify that the printhead carriage does not rub against the frame and that the top of the printhead does not interfere with the clear plastic window and its associated roller.

 Retighten the clamping screws and type several more lines of zeros to recheck printing quality. Readjust as necessary.

6.6.3 Print Image Contrast

The print image contrast is preset at the factory for optimum clarity and should not require adjustment. If the contrast has been changed and a darker or lighter image is desired, use the following procedures:

 For darker print insert a small standard screwdriver into the hole marked CON-TRAST located on the right side of the terminal (Figure 6-10); rotate the screwdriver clockwise (toward D), while printing characters from the keyboard, until the desired print image is obtained.

NOTE

If the print blurs, the screwdriver has been rotated too far. If so, adjust to a lighter print.

 For lighter print, rotate the screwdriver counterclockwise (toward L) while printing characters from the keyboard, until the printed image is light enough.

6.6.4 Transmit Level Adjustment (Models 785, 787)

The internal modem transmit level is factory-calibrated for optimum performance with most U.S. telephone systems. The transmit level is **not** field adjustable. *Tampering with the internal modem will violate the warranty and is subject to criminal prosecution under FCC regulations.*

6.7 PRINTHEAD CLEANING

The printhead should be cleaned each time a new roll of thermal paper is loaded into the terminal. Clean more often if the printed image begins to fade because of residue accumulated on the printhead by using the following procedures:

 Remove all thermal paper from the paper chute.

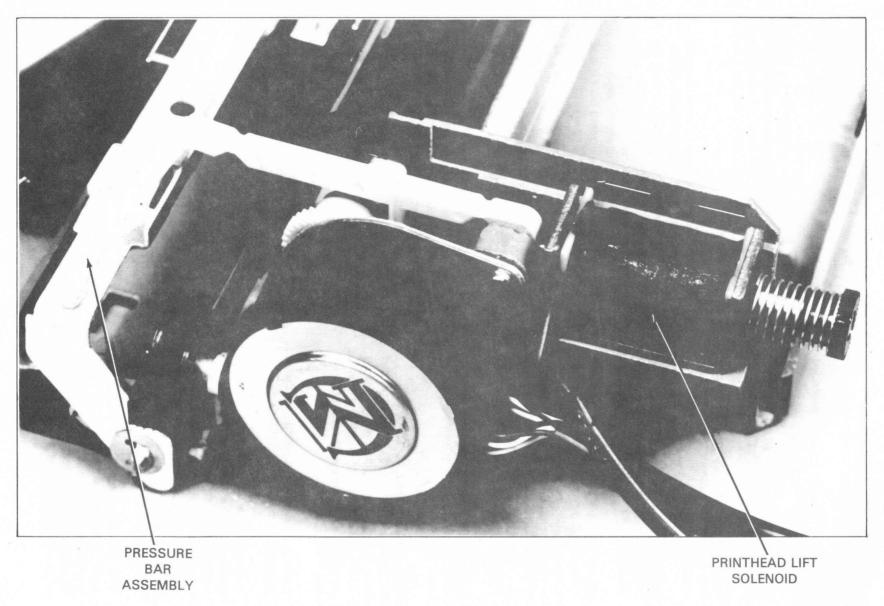


Figure 6-9. Printhead Solenoid

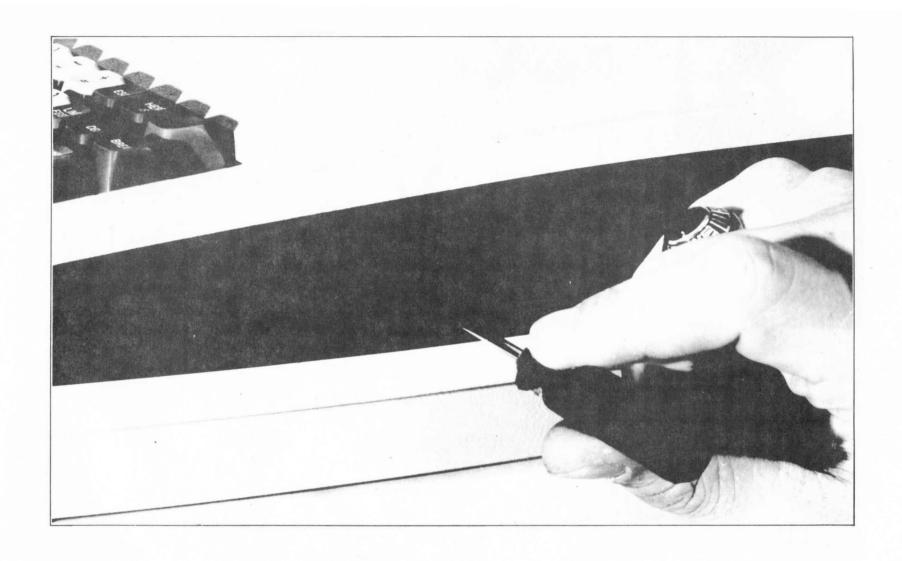


Figure 6-10. Print Contrast Adjustment

- Using 95-percent denatured alcohol, wet a 50mm (2 inch) wide strip across a sheet of good quality bond paper (Figure 6-11). Insert the sheet in the paper chute so that the wetted area appears under the printhead. If denatured alcohol is not available, rubbing alcohol can be used.
- Print five lines on the bond paper across the alcohol-wetted strip. Then advance the paper to a dry area and print two more lines.

NOTE

The printhead will not print a visible image on the bond paper.



Figure 6-11. Printhead Cleaning

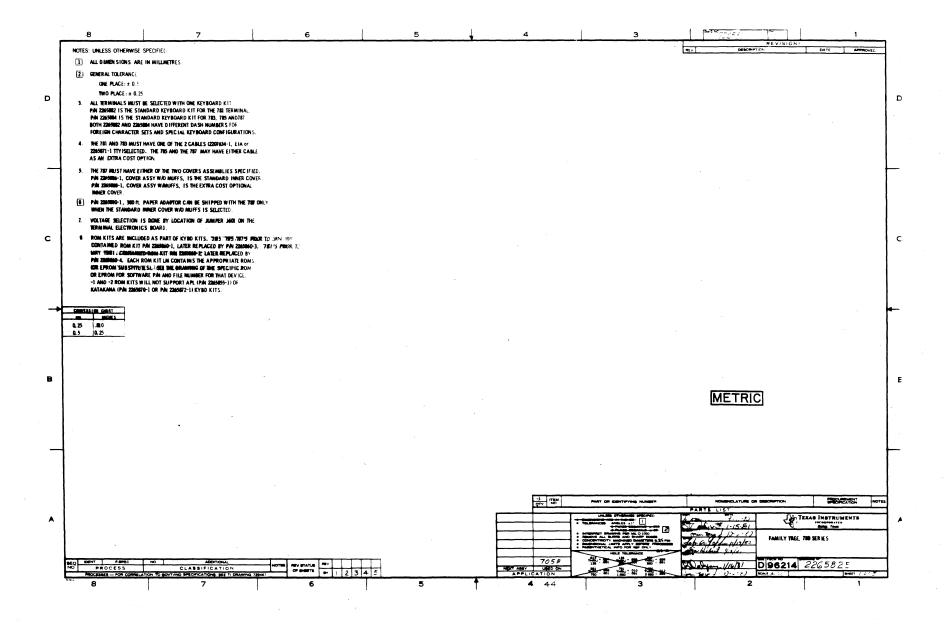
Section 7

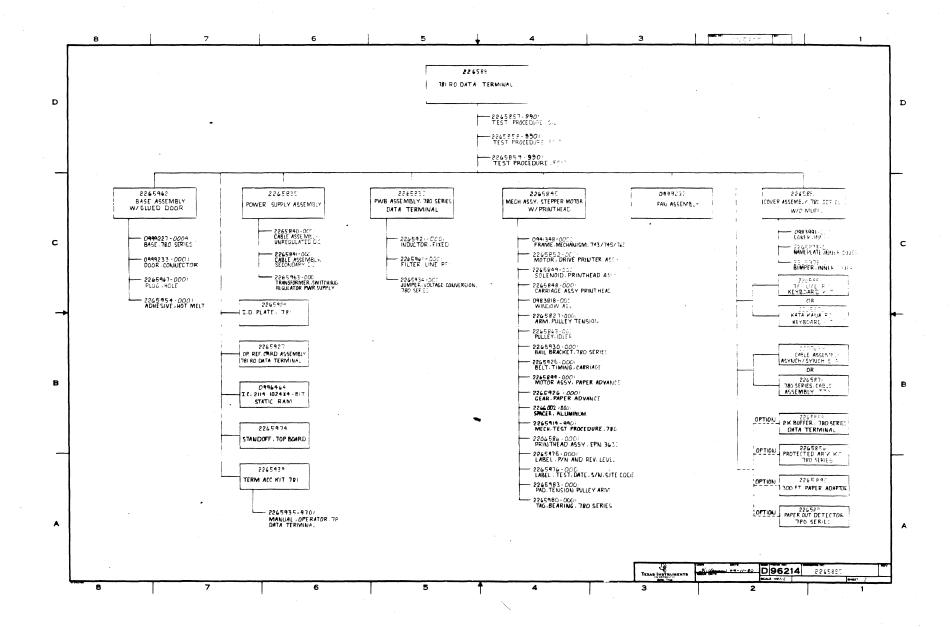
Assembly Drawings

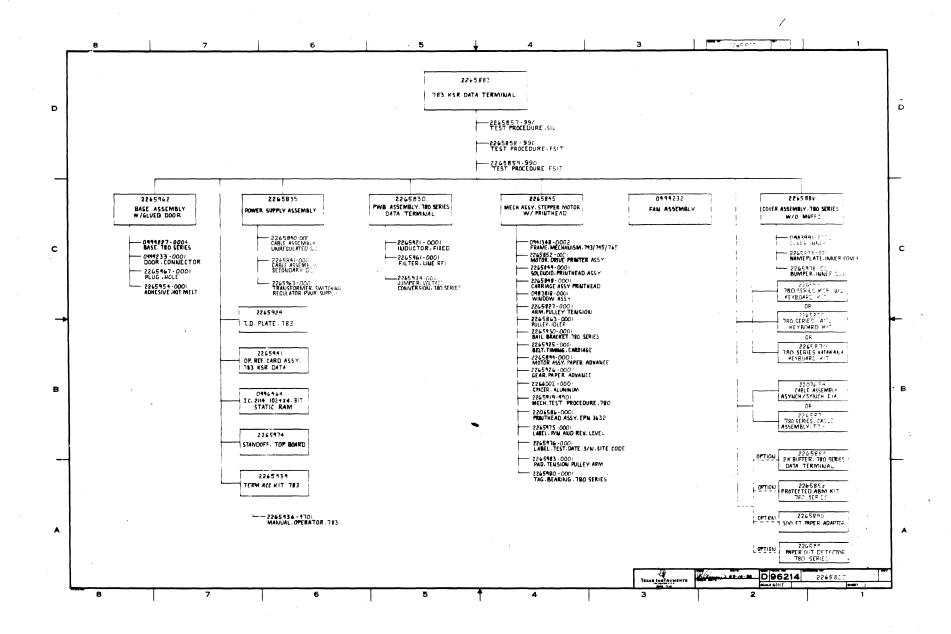
Assembly Drawings	Drawing Number	Page Number
Family Tree	2265825	7-3
PWB Assy, Terminal Electronics	2265830*	7-8
PWB Assy, Power Supply	2265835	7-22
Mechanism Assy, Stepper Motor w/Printhead	2265845	7-26
Carriage Assy, Printhead	2265848	7-31
Solenoid, Printhead Assy	2265849	7-33
Sensor Assy, Feedback Wheel Motor	2265850	7-35
Motor, Drive-Printer Assy	2265852	7-37
Muff Assy, Mike, 780 Series	2265875	7-39
Muff Assy, Speaker, 780 Series	2265878	7-41
781 RO Data Terminal	2265881	7-43
781 U/L Keyboard Kit	2265882	7-47
783 KSR Data Terminal	2265883	7-49
785 KSR Data Terminal	2265885	7-53
Cover Assy, 780 Series w/o Muffs	2265886	7-57
787 KSR Data Terminal	2265887	7-60
Cover Assy, 780 Series w/Muffs	2265888	7-64
Keytop Assy, 781 Data Terminal	2265895	7-67
Keytop Overlay, 781 Data Terminal	2265897	7-69
Motor Assy, Paper Advance	2265899	7-70
Keyboard Assy, 781 RO	2265915	7-72
Sensor Assy, 780 Series	2265951	7-74
PWB Assy, Paper Out Detector	2265952	7-76
PWB Assy, VDE Power Supply	2265970	7-79
Assy, International Power Supply	2265971	7-86
Cover Assy, Outer	0983809	7-88
Fan Assy	0999232	7-91

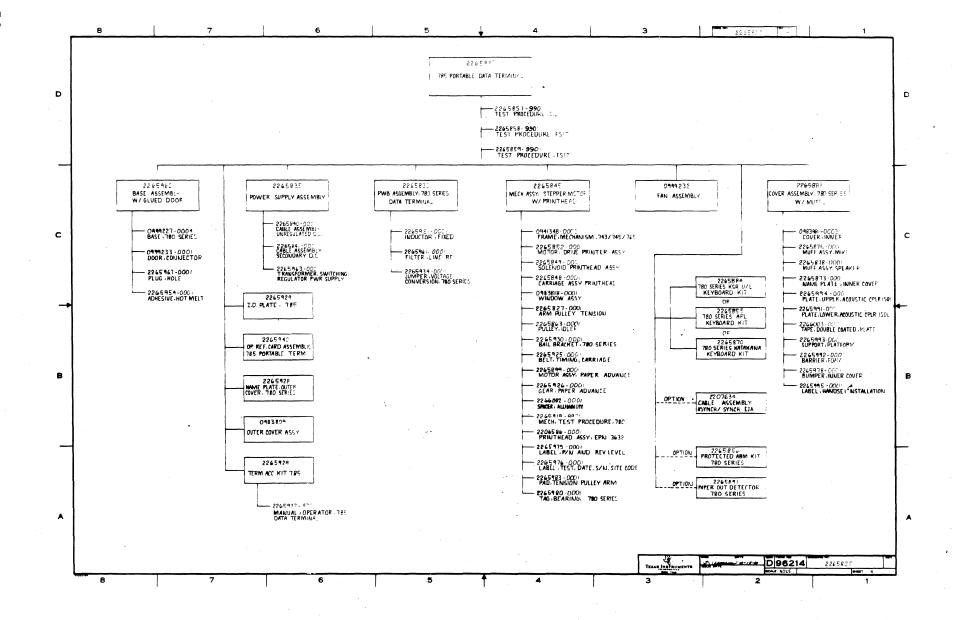
^{*}Two versions of this board are in use; they can be distinguished by their lists of materials, 2265830-0001 or 2265830-0002.

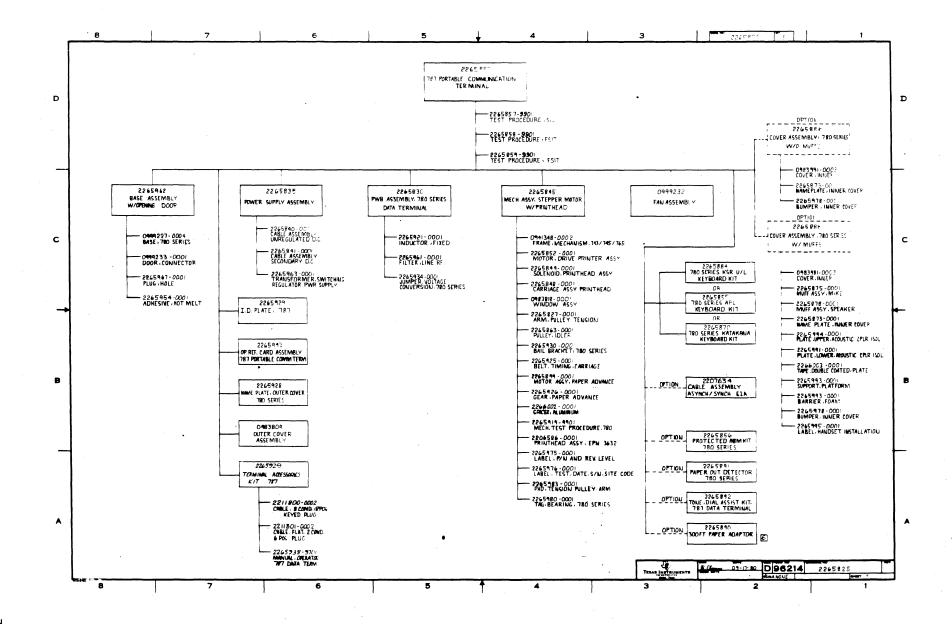
Cables	Drawing Number	Page Number
		7.00
Cable Assy, Internal Modem	2265826	7-93
Cable Assy, Unregulated dc	2265840	7-95
Cable Assy, Secondary dc	2265841	7-97
Cable Assy, Modem Power Supply	2265844	7-99
Cable Assy, TTY	2265871	7-101
Wiring Harness, Low Paper Alarm	2265898	7-103
Wiring Harness, Sensor	2265923	7-105
Cable Assy, Acoustic Coupler, 780 Series	2265932	7-107
Jumper, Voltage Conversion, 780 Series	2265934	7-109
Cable Assy, Unregulated dc	2266000	7-111
Cable Assy, Secondary dc	2266001	7-113

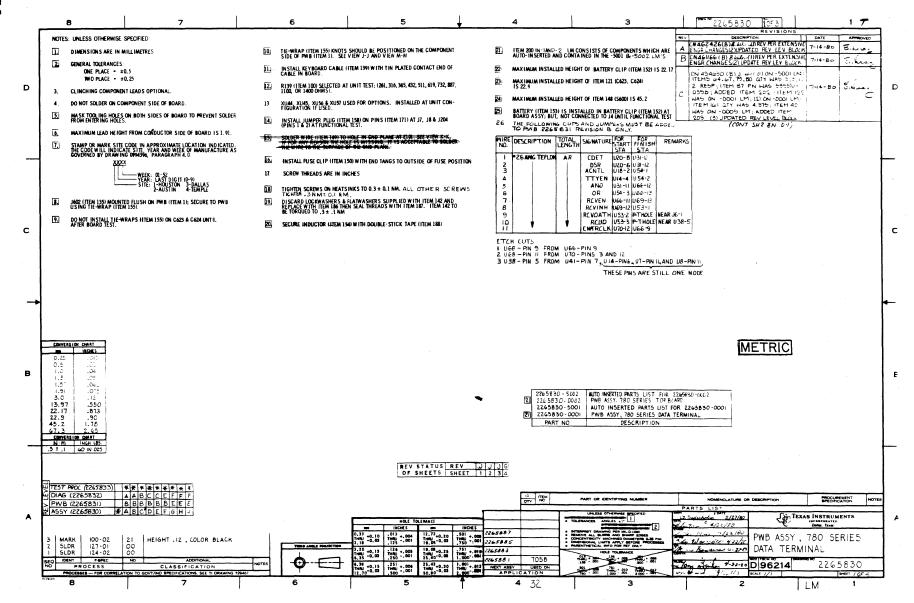


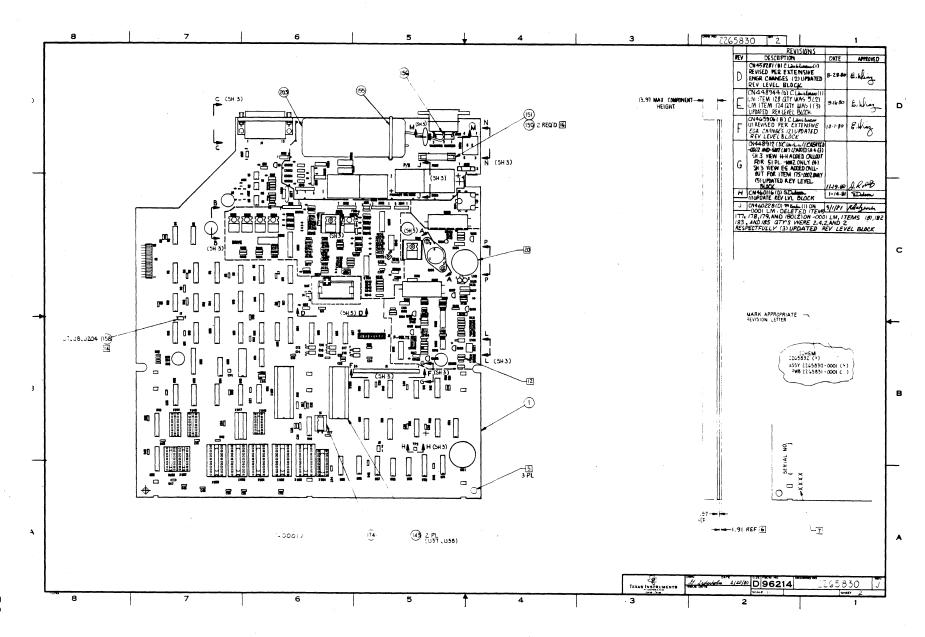




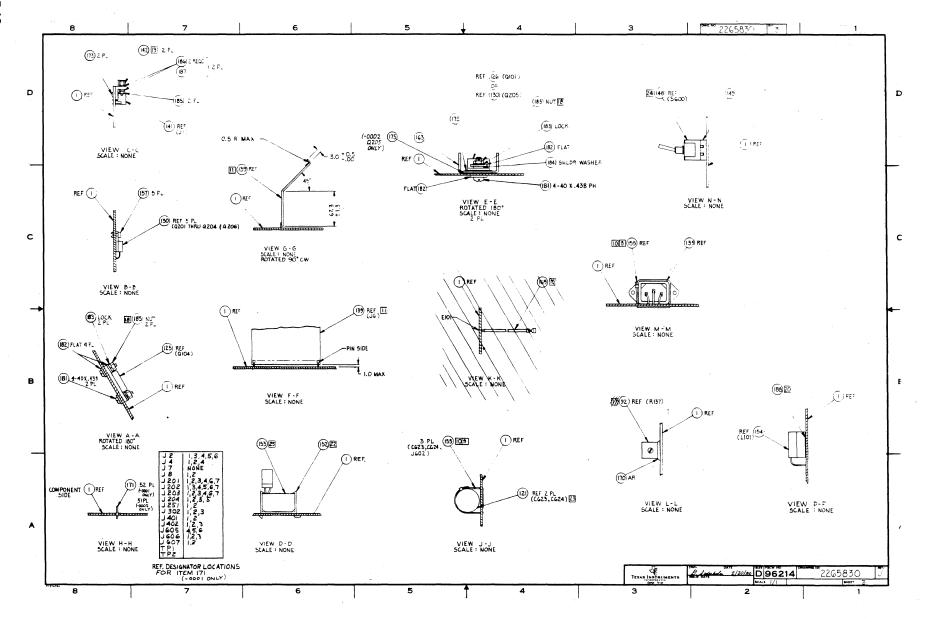


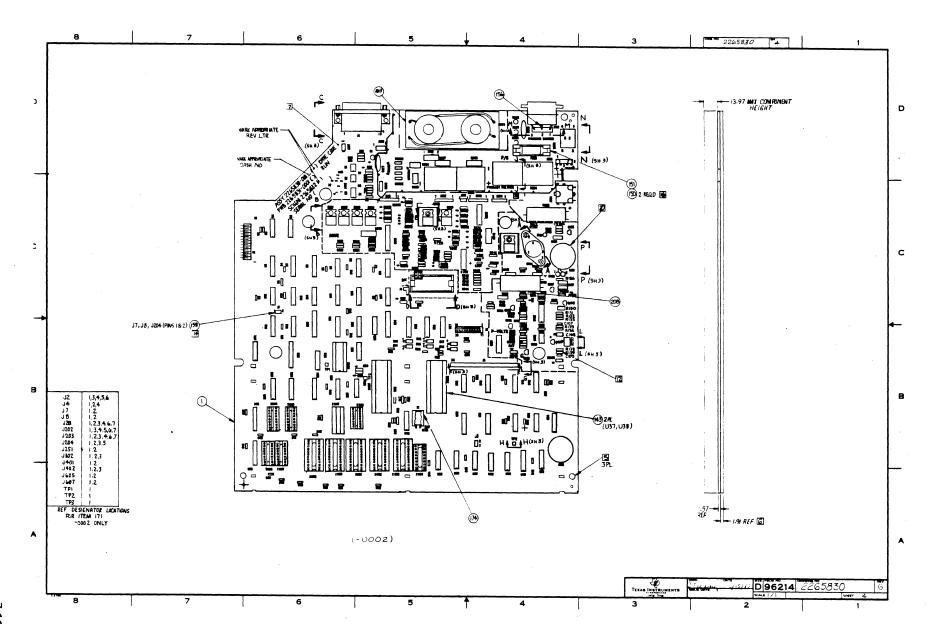






7-9





OCTOBER	24, 1980			
PART NU 2265830			ON	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
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0032A			TI -TIL111 U1	
0033	00001.000	0972625-0001	TI -TILL11 NETWORK OC1449 OPTICALLY COUPLED	
0033A			TI -0C1449 U2	•
0034	00002.000	0996089-0004	TI -OC1449 IC.SN74LS244N LINE DRIVER	
0034A	000025000	0 7 7 0 0 0 7 - 0 0 0 4	-SN74LS244N	
			U20 U28 -SN74LS244N	
0035	00001.000	0996755-0001	IC,SN74LS245N BUS XCVR TRANSITION 001295-SN74LS245N	1
0035A			U47 001295-SN74LS245N	
0036	00001-000	0996029-0001	IC.SN74LS273N OCTAL D-TYPE FLIP/FLOP TI -SN74LS273N	
0036A			U24	
0037	00001-000	0944472-0001	NETWORK, TMS-8080 MICRO PROCESSOR	
0037A			TI -TMS8080 U37	
0038	00001.000	0972469-0002	TI -TMS8080 NETWORK TMS5504,1/0 AND TIMER	
0038A			TI -TMS5504 U38	
0039	00001 000	0996203-0002	TI -TMS5504	_
	000011000	0996203-0002	IC, S 5101L-1 1024BIT(256 X 4)ST CMOS RAM 034649-S5101L-1	1
0039A			U30 034649-S5101L-1	
0040	00001.000	2210988-0001	IC, HEX DIFFERENTIAL COMPARATOR SEE TI- DRAWING	1
0040A			U201 SEE TI- DRAWING	
0092	00001.000	0972619-0004	RESISTOR VAR 500 OHM 5% .5W	1
0092A			R137	
0093	00001.000	0972554-0006	RESISTOR, FIXED, WIREWOUND .5 OHM 3W 1%	Ε
0093A			SEE - TI DRAWING R205	
0094	00001 - 000	0972946-0074	SEE - TI DRAWING RES FIX 2.4K OHM 5 % .25 W CARBON FILM	E
0094A			ROH - R-25 R233	•
0096	00001 000	0972978-0098	ROH - R-25	_
	00301*000	U712710-UUY8	RES. FIXED, 750 OHMS, 1W, 5% TOL. SEE TI- DRAWING	E
0096A			R245 SEE TI- DRAWING	
0098	00002.000	2211264-0001	THERMISTOR, DISC SEE TI- DRAWING	E
0098A			R634 R635 SEE TI- DRAWING	
0099	00002.000	0972978-0142	RES FIX COMP 51K 1 WATT 5%	E
0099A			QPL - RCR32G473JS R636 R637	
0100	00001-000	0983937-0001	QPL - RCR32G473JS RESISTOR,SELECTED,743/745 PWB,PVOLTS	Ε

OCTOBER	24, 1980			
PART NUM 2265830-			ON 780 SERIES DATA TERMINAL	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	M
0100A			R139	
0103	00001-000	0972757-0037	1224000 CAP FIX CER 0.1MF 10% 50V	E
0103A			C209	
0119	00002.000	0996326-0009	CAPACITOR, ELECT., ALUM., 390 CAP MFD	E
0119A			SEE TI- DRAWING C102 C625	
0120	00001.000	2210420-0005	SEE TI- DRAWING CAP,PLASTIC,METALLIZED,20%,4700 PF,20MHZ	E/
0120A			012624-SEE TI DWG	٠.
0121	00002.000	0972601-0001	Olicez4-SEE TI DWG CAPACITOR 200UF 200WVDC 10%	E/
0121A	***************************************	V/12001 0001	056289-076443 C623 C624	C *
0124	00004.000	0772637-0006	056289-076443	_
0124 0124A	UUU UT 4 UUU	0112031-0000	TRANSISTOR, TIS99 TITIS99	E
			Q1 Q105 Q106 Q107 TITIS99	
0125	00001-000	2210989-0001	IC, SWITCHING REGULATOR SEE TI- DRAWING	E
0125A		·	Q104 SEE TI- DRAWING	
0126	00001.000	0996801-0001	TRANSISTOR,T1P100 N-P-N,DARLINGTON 001295-T1P100	E
0126A			Q101 001295-T1P100	
0127	00001-000	0772116-0001	TRANSISTOR TIS75 TITIS75	E
0127A			Q109 TITIS75	
0128	00002.000	0972057-0001	TRANSISTOR-A5T2222 NPN SILICON	E
0128A			1640-2132-000 0102 0108	
0129	00001.000	0800523-0001	1640-2132-000 TRANSISTOR AST2907 PNP SILICON	E
0129A			TIA5T2907 Q103	
0130	00005.000	0996712-0001	TIA5T2907 Transistor,tiplo5 p-n-p power	E
0130A			001295-TIP105 Q201 Thru Q205	
0131	00001-000	0972572-0002	OOL295-TIPLO5 TRANSISTOR,TIPL21 SILICON N-P-N DARLNGTN	ΕÆ
0131A			TITIP121 9206	
0133	00001.000	0538031-0020	TITIP121 Crystal unit. Quartz	E
0133A			SEE T -I DWG	•
0134	00001 -000	2210858-0001	SE T -I DWG BUZZER, PIEZDELECTRIC	E
0134A	000014000	££10070 0001	SEE TI- DRAWING	Ε,
	00001 000	2004240-0001	DS1 SEE TI- DRAWING	-
0135 0135A	00001 *000	0996260-0001	RECEPTACLE,3-PIN AC PWR SCT -EAC-301 J602	E

-LIST OF MATERIALS-OCTOBER 24, 1980 DESCRIPTION ... PART NUMBER REV 2265830-0001 PWB ASSY, 780 SERIES DATA TERMINAL QUANTITY. COMPONENT.. DESCRIPTION...... UM ITEM. CONNECTOR PWB MOUNTED 3 CONTACTS NATURAL EA 0136 00001.000 0972423-0005 017105-350429-1 0136A 1603 017105-350429-1 00001.000 CONN, PCB HEADER 9CKT 0137 0972423-0003 FΔ 0137A 1604 0138 00001.000 0996099-0013 HEADER, RIGHT ANGLE 26 POSITIONS EΑ ee1 - 65624-126 01384 .13 BEI - 65624-126 0139 00001-000 CABLE ASSEMBLY, FLAT-FLEXIBLE 0972493-0001 FΑ AMP - 88178-1 0139A J6 AMP - 88178-1 0140 00001.000 0972498-0001 CONN, DBL ROW, EDGE MTG-20 POSITIONS EA -SEE DWG 0140A J5 -SEE DWG 0141 00001.000 0972854-0001 CONNECTOR, P.C. BOARD 25 POSITION FA AMP - 206584-2 0141A Jl AMP - 206584-2 0142 00002.000 0406769-0001 SCREW. SPECIAL, CONNECTOR LOCKING EΑ - D20418-2 CIE SCCKET, LOW PROFILE, DIP, 40 PINS 0143 00002.000 2210188-0009 FΛ 003612-DILB40P-108 0143A XU37 XU38 003612-DILB40P-108 0144 00005.000 2210188-0016 SOCKET, DIP, 24-PIN, LOW PROFILE EA SEE T -I DRAWING 0144A XU59 THRU XU63 003612-DILB24P-108 SOCKET, DIP, 20-PIN, LOW PROFILE 0145 00002-000 2210188-0014 FA SEE T -I DRAWING 0145A XU47 XU64 003612-DILB 20P-108 0146 00004.000 2210188-0013 SOCKET, DIP, 18-PINS, LOW PROFILE EΑ SEE T -I DRAWING 0146A XU44 XU45 XU56 XU57 003612-DILB18P-108 0147 00001.000 2210188-0003 SOCKET, LOW PROFILE, DIP, 16 CONT FA 003612-DIL816P-108 01474 XIIAR 003612-DILB16P-108 0148 00001.000 0996592-0001 SWITCH, TOGGLE DPDT 3A/250 VAC 6A/120 VAC FΑ 009353-9201L4H3W3QE 0148A \$600 009353-9201L4H3W3QE 0149 00001.000 0999430-0001 SPACER, SWITCH EA 1224-9430-019 0150 00002-000 0772635-0001 CLIP.FUSE EΑ LIT -1020680151 00001.000 2.0 A 250V 3AG 0416434-0203 **FUSE** FΑ LIT - 312002 0151A F600 - 312002 LIT 0152 00001-000 2265851-0001 CLIP, BATTERY PACKAGE EΑ 1238-5851-003 0153 00001.000 2210498-0001 BATTERY PACK, MERCURIC OXIDE EΑ

SEE TI- DRAWING

—LIST OF MATERIALS— OCTOBER 24, 1980 DESCRIPTION PART NUMBER RFV PWB ASSY, 780 SERIES DATA TERMINAL 2265830-0001 F QUANTITY. ITEM. 0153A BAT SEE TI- DRAWING 0154 2265921-0001 INDUCTOR, FIXED 00001-000 EA 0154A 1101 0155 00004.000 0972632-0001 STRAP, TIE DOWN, CABLE-NON-STD, 0-1-1/4 D. EΑ 0156 00000.300 0411400-0018 WIRE, BARE TINNED, 18AWG, COPPER BUS FT IWP -18-630 0157 00005-000 2265828-0001 CLIP, TRANSISTOR FΑ 1238-5828-004 0159 00004.000 0972487-0001 JUMPER PLUG, CONNECTOR BLACK EΑ 5935-0900-000 0158A J7 J8 J204 J607 5935-0900-000 00005.283 2210083-0003 WIRE, ELEC, COND U/L STYLE 1213, 24 AWG FT 0161 090484-WTE24A 0163 00002.000 0996285-0004 HEATSINK, TRANSISTOR .750 X .750 EA 013103-6073B 0165 REF 2265832-9901 DIAG LOGIC. 780 SERIES DATA TERMINAL EΑ 0166 REF 2265833-9901 TEST PROC, 780 SERIES DATA TERMINAL EΑ 0168 00002.000 JUMPER, VOLTAGE CONVERSION, 780 SERIES 2265934-0001 EΑ 1238-5934-010 0168A J605 J606 1238-5934-010 0170 AR 0996527-0001 ADHESIVE, LOCTITE 416 ΕA 059724-16SUPERBONDER 0171 00052.000 0972456-0002 PIN. 025 SQUARE EA 5935-0800-000 EYELET -121 BARREL OD X-219 LG FLANGE 00002.000 0085936-0018 0173 EA USH - #SE-47 0174 00000-170 0972437-0005 INSULATION SLEEVING 1/4" HEAT SHRINKABLE FT - HT-105C-UL-1/ LFS 0175 00002.000 0996521-0010 INSULATOR, .147DIA .750LG .500W EA 055285-7403-09FR-54 00001-000 0772696-0009 HEADER, 2 PIN . 200LG SGL ROW, STRIP OF 2 0176 FA -0002363 0176A -0002363 0177 00002.000 0972988-0029 SCREW 6-32 X .438 PAN HEAD CRES EΑ 0178 00002.000 0411027-0805 WASHER, FLAT, . 156ID X .312 OD X .035THK FΑ 0179 00002.000 0411104-0136 WASHER, LOCK-SPRING, HELICAL, #6 E٨ OPL - MS35338-136 0180 00002-000 0416453-0022 NUT, PLAIN 6-32 UNC-28 HEX CRES, SMALL EΑ QPL - NAS671C6 0181 00002-000 0972988-0016 SCREW 4-40 X .438 PAN HEAD CRES FΑ 0182 00004-000 0416622-0011 WASHER #4 FLAT EΑ QPL - AN960C4L WASHER, LOCK-SPRING, HELICAL, #4 QPL - MS35338-135 0183 00002-000 0411104-0135 FA WASHER,#4 .115ID .2000D-SHLDR NON-MET 0184 00002.000 0972628-0001 EΑ -5607-45 SFA 0185 00002.000 0416453-0021 NUT, PLAIN, 4-40 UNC-2B HEX, CRES, SMALL FΑ OPL - NAS671-C4 0410898-0004 WASHER #4 LOCK-INT TOOTH -115ID 0186 00004.000 FΑ

-LIST OF MATERIALS-

OCTOBER	24, 1980			
PART NUI 2265830			ON	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0187	AR	0996552-0002	ADHESIVE,50CC BOTTLE, WELD AND POROSITY	вт
0188	00001-000	2265966-0002	TAPE, FOAM, DOVBLE STICK, 3/4 INCH SQUARE	EA
0190	00001.000	2210188-0006	SOCKET, LOW PROFILE, DIP, 22 PINS, 10 CONT	EA
0190A			XU30 003612-DILB22P-108	
0200	00001.000	2265830-5001	AUTO INSERTED PARTS LIST FOR 2265830-1 1238-3051-019	EA
0203	00001.000	2265961-0001	FILTER, LINE	EA
0207	00001.000	0539370-0506	RES FIX FILM 18-2K OHM 1% .25 WATT	EA
0207A			R144	
0208	00000.063	0972437-0001	COR - NA55 SLEEVE,PVC .125 ID .025 WALL SEE - TI DRAWING	FĪ
9999	00002.500	0239999-9999	SEE – TI DRAWING COST, SHRINKAGE	EA

			LIST OF MATERIALS	
FEBRUAR	Y 03, 1991		·	
PART 180 2265830	MBER REV -0002 H	DESCRIPTI PWB ASSY	ION	
ITEM.	OUANTITY.	COMPONENT	DESCRIPTION	JM
0032	00001.000	0971000-0001	IC TIL-111 OPTICALLY COUPLED ISOLATOR	EA
00324			U1	
0033	00001.000	0972625-0001	METHORK OCI449 OPTICALLY COUPLED	EA
00334			11 -001449 U2 11 -001449	
0034	00002.000	0996089-0004	IC, SM74LS244N LINE DRIVER	ΕA
0034A			-SN74L S244N U20 U28	
0035	00001.000	0996755-0001	-SN74LS244N IC,SN74LS245N BUS XCVR TRANSITION	EΑ
0035A			001 295 - SN74L S 245N U47	
0036	00001.000	0996029-0001	001295-SN74LS245N IC,SN74LS273N OCTAL D-TYPF FLIP/FLOP	ΕA
0036A			TI -SN74LS273N U24	
0037	00001.000	0944472-0001	TI -SN74LS273N NETWORK,TMS-8080 MICRO PROCESSOR	FΑ
0337A			TI -TMS9080 U37	
0038	00001.000	0972469-0002	TI -TMS8080 NETWORK TMS5504,170 AND TIMER	EA
10038A			TI -TMS5504 U38	
0039	00001.000	0996203-0002	TI -TMS5504 10.5 5101L-1 1024B1T(256 X 4)ST CMOS RAM 034649-S5101L-1	EΑ
0039A			U30 034649-\$5101L-1	
0040	00001.000	2210983-0001	IC, HEX DIFFERENTIAL COMPARATOR SEE TI- DRAWING	EA
00404			U201 SEE TI- DRAWING	
0061	00001.000	3972946-0062	RES FIX 750 DHM 5 % .25 W CARBON FILM	EA
0061A			R143 ROH - R-25	
0092	00001.000	0972619-0004	RESISTOR VAR 500 OHM 5% .5W	EA
0092A			R137	
0093	00001.000	0972554-0006	RESISTOR,FIXED,WIREWOUND .5 OHM 3W 1% SEE - TI DRAWING	EA
0093A			R205 SEE - TI DRAWING	
0094	00001.000	0972946-0074	RES FIX 2.4K OHM 5 % .25 W CARBON FILM ROH - R-25	ΕA
00944			R233 ROH - R-25	
0096	0000.10000	0072978-0098	RES. FIXED, 750 OHMS, 1W, 5% TOL. SEE TI- DRAWING	FA
00964			P245 SEE TI- DRAWING	
0028	00002.000	2211264-0001	THERMISTOR, DISC SEE TI- DRAWING	EA
00984			R634 R635 SEF TI- DRAWING	
0099	00002.000	0972978-0142	RFS FIX COMP 51K 1 WATT 5% QPL - RCR32G473JS	EA

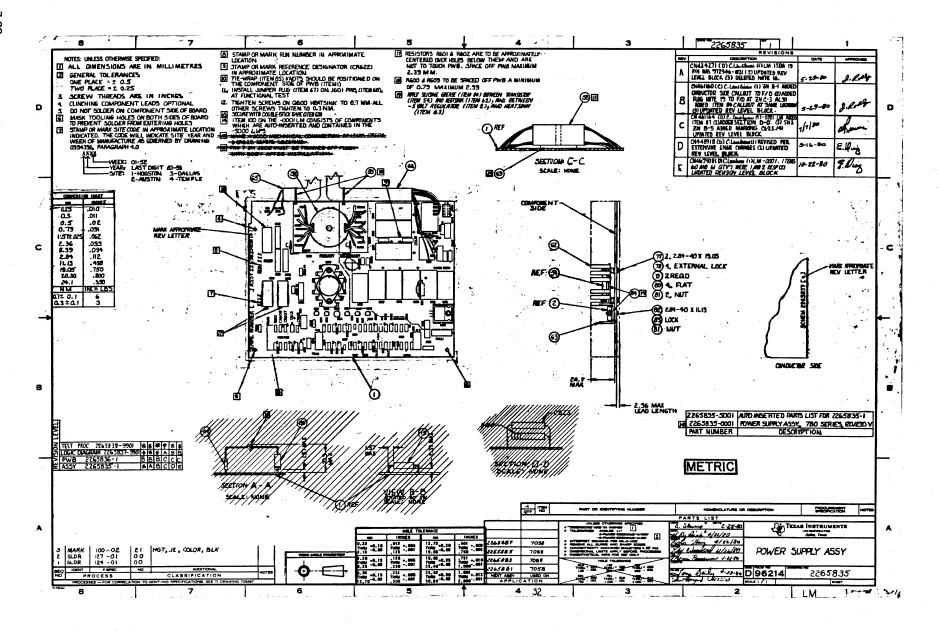
FEBRUAS	RY 03, 1981		IST OF MATERIALS	
PART N	MBER REV		CN	
2265830			786 SERIES, TOP BOARD	
ITEM. 0099A	QUANTITY.	COMPONENT	R636 R637	JM
0 100	000.01.000	0983937-0001	QPL: - PCR32G473JS RESISTOR,SELECTED,743/745 PWB,PVOLTS	E
0100A			1224000 R139	
0119	00002.000	0996326-0009	1224000 CAPACITOR, ELECT., ALUM., 390 CAP MED	Ε
0119A			SEE TI- DRAWING C102 C625	
0120	00001.000	2210420-0005	SEE TI- DRAWING CAP, PLASTIC, METALLIZED, 20%, 4700 PF, 20MHZ	Ε
0120A			012624-SEE TI DWG C626	
0121	00002.000	0972601-0001	012624-SEC TI DWG CAPACITUR 230UF 200WVDC 10%	Ε
01214			056289-D76443 C623 C624	
0124	00004.000	0772637-0006	056289-076443 TRANSESTOR.TIS99	E
0124A			TITIS99 01 0105 0106 0107	_
0125	00001.000	2210989-0001	TITIS99 IC, SWITCHING REGULATOR	E
0125A			SEE TI- DRAWING Q104	
0126	00001.000	0996801-0001	SEE TI-, DRAWING TRANSISTOR, TIP100 N-P-N, DARLINGTON	E
01264			001295-T1P100 0101	-
0127	00001.000	0772116-0001	001295-T1P100 TRANSISTOR T1S75	Ε
01274			TITIS75 0109	L
0128	00002.000	0972057-0001	TITIS75 TRANSISTOR-A512222 NPN SILICON	Ε
0128A		0 11 02 1 0001	1640-2132-000 0102 0108	L
0129	00001.000	0800523-0001	1643-2132-000 TRANSISTOR A512907 PNP SILICON	E
0129A	() / 51 • 5 • ()),,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	TIA5T2907 Q103	۲.
0130	00005.000	0996712-00G1	TIA5T2907 TRANSISTOR,TIP105 P-N-P POWER	_
0130A	00000000	3770712 6001	001295-11P105 0201 THRU 0205	E
0131	00001 000	0972572-0002	001295-TIP105	
01314	(10.7(11.4(10)	1912512-0032	TRANSISTOR, TIP121 SILICON N-P-N DARLNGTN IITIP121	E
0131A	03331 330		0206 TI	
	00001.000	0538031-0020	CRYSTAL UNIT, QUARTZ SEE T -1 DWG	Ε
0133A	00001 000	2010050 0000	Y1 SEE T -I DWG	
0134	00001.000	2210858-0001	BUZZER, PIEZOELECTRIC SEE TI- DRAWING	E
0134A	00001 000		DS1 SEE TI- DRAWING	
0135	00001.000	0996260-0001	RECEPTACLE,3-PIN AC PWR SCT -EAC-301	F.
0135A			J602 SCT -EAC-301	

f -			IST OF MATERIALS	
FEBRUARY	03, 1981		•	
	MBER REV -0002 H		ON	
ITEM. 0136		COMPONENT 0972423-0005	CONNECTOR PWB MOUNTED 3 CONTACTS NATURAL 017105-350429-1	
0136A 0137	00001.000	0972423-0003	J603 017105-350429-1 CONN, PCB HEADER 9CKT	EA
0137A			J604	
0138 01384	00001.000	0996099-0013	HEADER, PIGHT ANGLE 26 POSITIONS BEI - 65624-126 J3	EA
0137 0139A	00001.000	0972493-0001	BEI - 65624-126 CABLE ASSEMBLY,FLAT-FLEXIBLE AMP - 88178-1 J6	EA
0140 0140A	00001.000	0972493-0001	AMP - 88178-1 COMN,OBL ROW,EDGE MTG-20 POSITIONS -SEE DWG J5	EA
0141	00001.000	0972854-0001	-SEE DWG CONNECTOR,P.C. BOARD 25 POSITION AMP - 206584-2 J1	EΑ
0142	00002.000	0405769-0001	AMP - 206584-2 SCREW,SPECIAL,CONNECTOR LOCKING	EA
0143		2210188-0018	CIE - D20418-2 SOCKET,DIP,40-PINS,LOW PROFILE	EA
0143A 0144 0144A	00005.000	2210188-0016	SEE T -I DRAWING XU37 XU38 SEE T -I DRAWING SOCKET,DIP,24-PIN,LOW PROFILE SEE I -I DRAWING XU59 THPU XU63	EA
0145 0145A	00002.000	2210188-0014	SEE T -1 DRAWING SOCKET,DIP,20-PIN,LOW PROFILE SEE T -1 DRAWING XU47 XU64	EA
01 46 01 46A	00004.000	2210198-0013	SEE T -I DRAWING SOCKET,DIP,18-PINS,LOW PROFILE SEE T -I DPAWING XU44 XU45 XU56 XU57	EA
0147 0147A	00001.000	2210188-0012	SEE T -I DPAWING SOCKET,DIP,16-PINS,LOW PROFILE SEE T -I DRAWING XU48	EA
0148 0148A	00001.000	0996592-0001	SEE T -I DRAWING SWITCH, TOGGLE DPDT 3A/250 VAC 6A/120 VAC 009353-9201L4H3W3QE S600	EA
0149	00001.000	0999430-0001	009353-9201L4H3W3QE SPACER, SWITCH	EA
0150	00002.000	0772635-0001	1224-9430-020 CLIP, FUSE	EA
0151	00001.000	0416434-0203	LIT -102068 FUSE 2.0 A 250V 3AG LIT - 312002	EA
0151A			F600 LIT - 312002	
0152	00001.000	2265851-0001	CLIP, BATTERY PACKAGE 1238-5851-003	EA
0153 0153A	00001.000	2210498-0001	BATTERY PACK, MERCURIC DIXIDE SEE TI- DRAWING BAT SEE TI- DRAWING	EA

			IST OF MATERIALS	in ver
FEBRUAR	Y 03, 1981			
PART Nº 2265830			ON	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	JM
0154	00001.000	2265921-0001	INDUCTOR, FIXED	EA
0154A			ι 101	
0155	00004.000	0972632-0001	STRAP, TIE DOWN, CABLE-NON-STD, 0-1-1/4 D.	ΕA
0156	00000.300	0411400-0018	WIRE, BARE TINNED, 18AWG, COPPER BUS	FT
0157	00005.000	2265828-0001	IMP -18-630 CLIP, TRANSISTOR	EA
0158	00004.000	0972487-0001	1238-5828-005 JUMPER PLUG, CONNECTOR BLACK	EA
0158A			5935-0900-000 J7 J8 J204 J607	
0161	00000.688	2210083-0003	5935-0900-000 WIRE,ELEC,COND U/L STYLE 1213,24 AWG	FT
0163	00002.000	0996285-0004	090484-WTE24A HEATSINK,TRANSISTOR .750 X .750	EΑ
0165	REF	2265832-9901	013103-6073B DIAG LOGIC, 780 SERIES DATA TERMINAL	ΕA
0166	REF	2265833-9901	TEST PROC, 780 SERIES DATA TERMINAL	EA
0168	00001.000	2265934-1001	JUMPER, VOLTAGE CONVERSION, 780 SEPIES	EA
01 68A			1238-5934-012 J605	
0170	AI	0996527-0001	1238-5934-012 ADHESIVE,LOCTITE 416	ΕA
0171	00051.000	0972456-0002	059724-16SUPERBONDER PIN025 SQUARE	EA
01 73	00002.000	0085936-0018	5935-0300-000 EYELET .121 BARREL OD X.219 LG FLANGE	EΑ
01.74	00000.170	0972437-0005	USH - #SE-47. INSULATION SLEEVING 1/4" HEAT SHRINKABLE	FT
0175	00003.000	0996521-0010	LFS - HT-105C-UL-1/ INSULATOR, 147DIA .750LG .500W	EA
01 77	00002.000	0972988-0029	055285-7403-09FR-54 SCREW 6-32 X .438 PAN HEAD CRES	EA
0178	00002.000	0411027-0805	WASHER, FLAT, . 156ID X .312 OD X .035THK	EA
0179	00002.000	0411104-0136	WASHER, LOCK-SPRING, HELICAL, #6	EA
0180	00002.000	0416453-0022	QPL - MS35338-136 NUT,PLAIN 6-32 UNC-2B HEX CRES.SMALL	EA
0181	00002.000	0972988-0016	QPL - NAS671C6 SCREW 4-40 X .438 PAN HEAD CRES	EA
0182	00004.000	0416622-0011	WASHER #4 FLAT	EA
0183	00002.000	0411104-0135	CPL - AN960C4L WASHER, LOCK-SPRING, HELICAL, #4	EA
0184	60002.600	0972628-0001	OPt - MS35338-135 WASHER,#4 .115ID .2000D-SHLDR NON-MET	EA
01 85	00002.000	0416453-0021	SEA -5607-45 NUT-PLAIN,4-40 UNC-2B HEX,CRES,SMALL	EA
01 86	00004.000	0410898-0004	QPL - NAS671-C4 WASHER #4 LOCK-INT TOOTH .115ID	
0187	AR	0996552-0002		EA
01 88	00001.000		ADHESIVE, SOCC BOTTLE, WELD AND POROSITY 005972-290-31	ВТ
		2265966-0002	TAPE, FOAM, DOVBLE STICK, 3/4 INCH SQUARE	EA
0190	00001-000	2210188-0015	SOCKET, DIP, 22-PINS, LOW PROFILE SEE T -I DRAWING	ΈA
01904			XU30 SEE T -I DRAWING	

LIST OF MATERIALS-

FEBRUAR	Y 03, 1981	·	•	
PART NU 2265830			ON	
ITEM.	QUANTITY.	COMPONENT	DE SCRIPTION	UM
0200	00001.000	2265830-5002	AUTO INSERTED PARTS LIST FOR 2265830-2	EA
0203	00001.000	2266005-0001	ANDUCTOR, TRANSIENT SUPPRESSOR	ΕA
02.05	00001.000	0972946-0057	RES FIX 470 DHM 5 % .25 W CARBON FILM	ΕA
0205A			R142 PDH - 8-25	
0207	00001.000	0539370-0506	CES FIX FILM 18.2K OHM 1% .25 WATT	ΕA
0207A			R144 COR - NA55	
0208	00000.063	0972437-0001	SLEEVE, PVC .125 IO .025 WALL SEE - TI DRAWING	FT
9999	00002.500	0239999-9999	COST, SHRINKAGE	EΑ

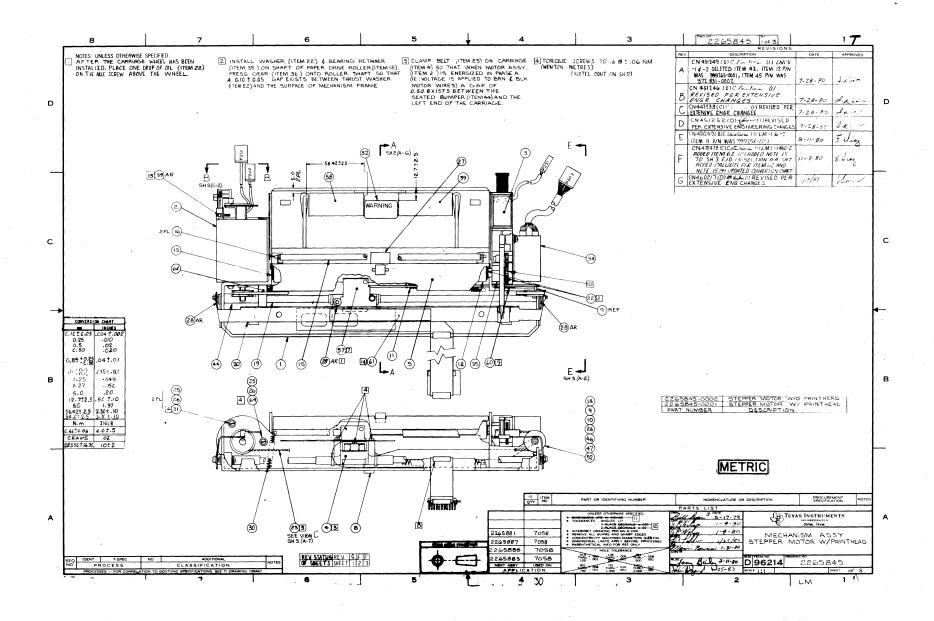


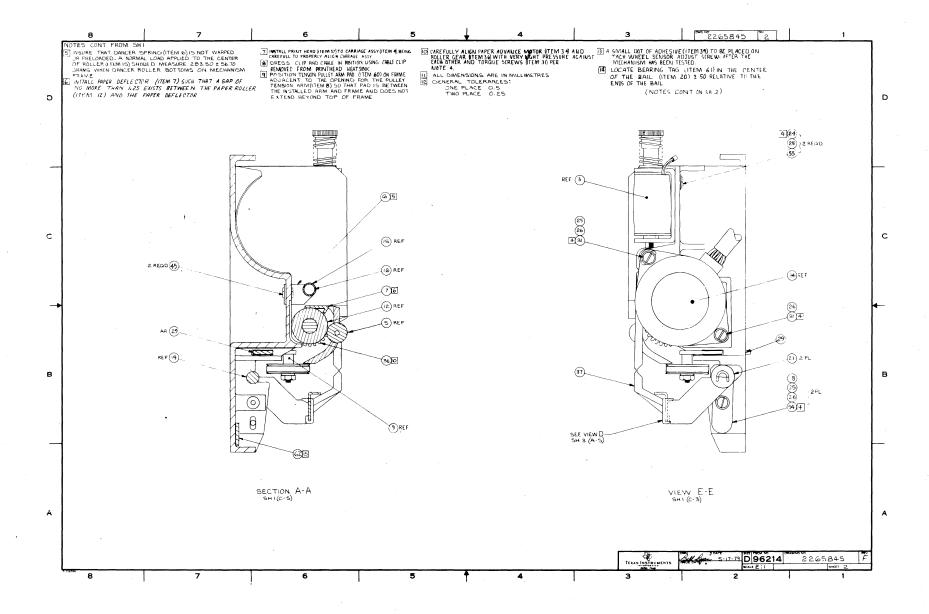
OC TOBER	24, 1980		
	MBER REV -0001 E	DESCRIPTI POWER SUP	ON
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION
0002	00001-000	0972499-0001	NETWORK,LM320T-5.0/MC7905CP,-5 VOLT SEE - TI DRAWING
0002A			U600
0003	00001.000	0222224-2741	
0003A			-SN72741P U601
0004	00002.000	0972942-0022	
0004A			SEE TI- DRAWING R601 R602
0005	00001-000	0972942-0047	
0005A			DAE - CW OR RS SERI R600
0006	00001.000	0972978-0107	· · · · · · · · · · · · · · · · · · ·
0006A			039008-SEE TI DWG R605
0007	00001.000	0972978-0069	
0007A			SEE - TI DRAWING R604
8000	00001.000	0972978-0065	
0008A		,	SEE TI- DRAWING R611
0009	00001.000		SEE TI- DRAWING RESISTOR,VARIABLE LOK OHM CERMET FILM
0009A			BOU - 3006P-1-103 R621
0011	00001-000	0538425-0131	BOU - 3006P-1-103 RESISTOR, FIX., 68K OHMS, 2W, 5% TOL.
0011A			SEE TI- DRAWING R609
0015	00001.000	0972978-0083	SEE TI- DRAWING RES FIX COMP 1.0 W 180 OHMS 5 %
0015A			QPL -RC32G181JS R607
0030	00003.000	0412645-0015	QPLRC32G181J\$ CAPACITOR1 UF +8020% 500VDC CER DIEL
0030A			1222-3866-000 C600 C601 C602
0031	00001-000	0972928-0001	056289-41C92 2/ CAP FIX MICA 1000 PF 500V 5%
0031A			C603
0032	00001.000	0972924-0019	CAP FIX TANT SOLID 22 MFD 10 % 35 VOLT
0032A			QPL -M39003/1-2306 C616
0033	00001.000	0972924-0015	QPL -M39003/1-2306 _. Cap fix tant solid 47 MFD 10 % 20 Volt
0033A			QPL -M39003/1-2295 C621
0035	00001.000	0996326-0009	QPL -M39003/1-2295 CAPACITOR,ELECT.,ALUM., 390 CAP MFD
0035A			SEE TI- DRAWING C604
0036	00004.000	0996326-0010	SEE TI- DRAWING CAPACITOR, ELECT., ALUM., 680 CAP MFD

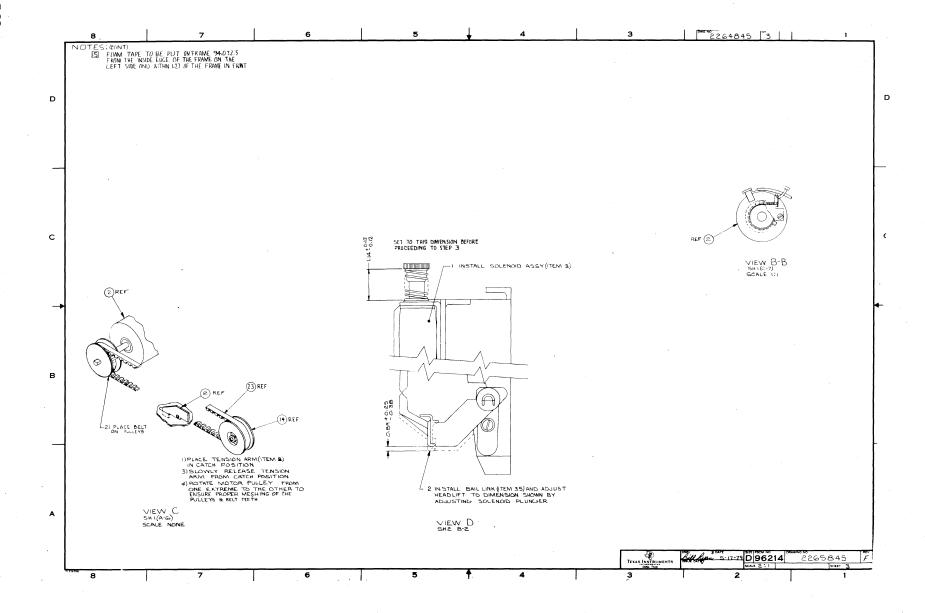
OCTUBER	24, 1980			
PART NU 2265835			IONPPLY ASSY, 780 SERIES, 120/230V	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	U
0036A			C607 THRU C610	
0037	00002.000	0996326-0011	SEE TI- DRAWING CAPACITOR, ELECT., ALUM., 1000 CAP MFD	
0037A			SEE TI- DRAWING C605 C606	
0038	00001.000	0412735-0047	SEE.TI- DRAWING Capacitor,.0047uf 3000vdc 20% ex cer	
0038A			071590-0030-472 C622	
0044	00001.000	0996281-0005	071590-0030-472 RECTIFIER,SILICON,FAST RECOVERY	
0044A			014099-553891 CR604	
0045	00001 000	0004381 0004	014099-553891	
	00001.000	0996281-0006	RECTIFIER, SS3892/UES1302, V(R)100V I(0)6A 014099-SS3892	
0045A			CR605 014099-SS3892	
0054	00001.000	0996703-0002	TRANSISTOR,NPN,125WATT,SJ9094-2 See ti- drawing	
0054A			Q600 SEE DRAWING	
0055	00001.000	0972957-0001	TRANSISTOR, 2N930A NPN LOW CUR AMP, TO-18	
0055A			MOT - 2N930A Q603	
0056	00003.000	0972057-0001	MOT - 2N930A TRANSISTOR-A5T2222 NPN SILICON	
0056A			1640-2132-000 9601 9602 9606	
0057	00002.000	0800523-0001	1640-2132-000 Transistor A5T2907 PNP SILICON	
0057A	00002000	,	TIA5T2907	
			Q604 Q605 TIA5T2907	
0058	00001.000	2265963-0001	XFORMER, SW RGLTR, PWR SPLY	
0058A			T600	,
0059	00001.000	0945247-0002	INDUCTOR,10 UH,5 AMP, FERRITE CORE	
0059A			L600	
0060	00002.000	0945247-0005	INDUCTOR, 10UH, 3AMP, FERRITE CORE	
0060A			L602 L603	
0061	00001.000	0945247-0004	INDUCTOR, 5UH, 3AMP, FERRITE CORE	
0061A			L601	
0062	00001.000	0533599-0014	HEAT SINK 75HT 1-29W 1-63LG ELEC CMPNT	
0063	00001-000	0996285-0004	098978-LAT03B3C8 HEATSINK,TRANSISTOR .750 X .750	
0064	00001.000	0996151-0009	013103-60738 HEADER,PIN,4 PINS, STR. DOUBLE ROW	
0064A			022526-65611-108 J600	
0065	00001.000	2265840-0001	022526-65611-108 CABLE ASSY, UNREGULATED D.C.	
0066	000014000	2207040-0001	1238-5840-014	

-LIST OF MATERIALS-

PART NUMBER REV 2265835-0001 E		DESCRIPTIONPOWER SUPPLY ASSY, 780 SERIES, 120/230V			
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM	
0067	00001.000	0972487-0001	JUMPER PLUG, CONNECTOR BLACK 5935-0900-000	E	
8 800	00001.000	0772696-0009	HEADER, 2 PIN .200LG SGL ROW, STRIP OF 2	E	
0068A			J601		
0069	00001.000	2265966-0001	-0002363 Tape,foam,dovble stick,1 inch square	E	
0075	REF	2265837-9901	DIAG, LOGIC, 780 SERIES POWER SUPPLY	E	
0076	REF	2265838-9901	TEST PROC, 780 SERIES POWER SUPPLY	E	
0077	00002-000	0972988-0019	SCREW 4-40 X .750 PAN HEAD CRES	E	
0078	00004.000	0411101-0057	LOCKWASHER # 4 EXTERNAL TOOTH CRES	E	
0079	00002.000	0416925-0400	SPACER,#4 1/8"LG ALUM ANODIZED -NAS43DDO-8	E	
0080	00004.000	0416622-0011	WASHER #4 FLAT OPL - AN960C4L	E	
1800	00003.000	0416453-0021	NUT,PLAIN,4-40 UNC-28 HEX,CRES,SMALL QPL - NAS671-C4	E	
0082	00001.000	0972988-0016	SCREW 4-40 X -438 PAN HEAD CRES	E	
0083	00001.000	0411104-0135	WASHER, LOCK-SPRING, HELICAL, #4 QPL - MS35338-135	E	
0084	AR	0415886-0001	SILICONE COMPOUND(8 OZ TUBE)METAL OXIDE WAK - 120	E	
0085	00002.000	0972632-0001	STRAP, TIE DOWN, CABLE-NON-STD, 0-1-1/4 D.	E	
0086	00001.000	0972608-0001	DIODE,1N5820 3AMP SCHOTTKY RECTIFIER MOT -1N5820	· E	
A 8800			CR622		
0100	00001.000	2265835-5001	MOT -1N5820 AUTO INSERTED PARTS LIST FOR 2265835-1 1238-3551-013	E	
9999	00000.750	0239999-9999	COST, SHRINKAGE	E	



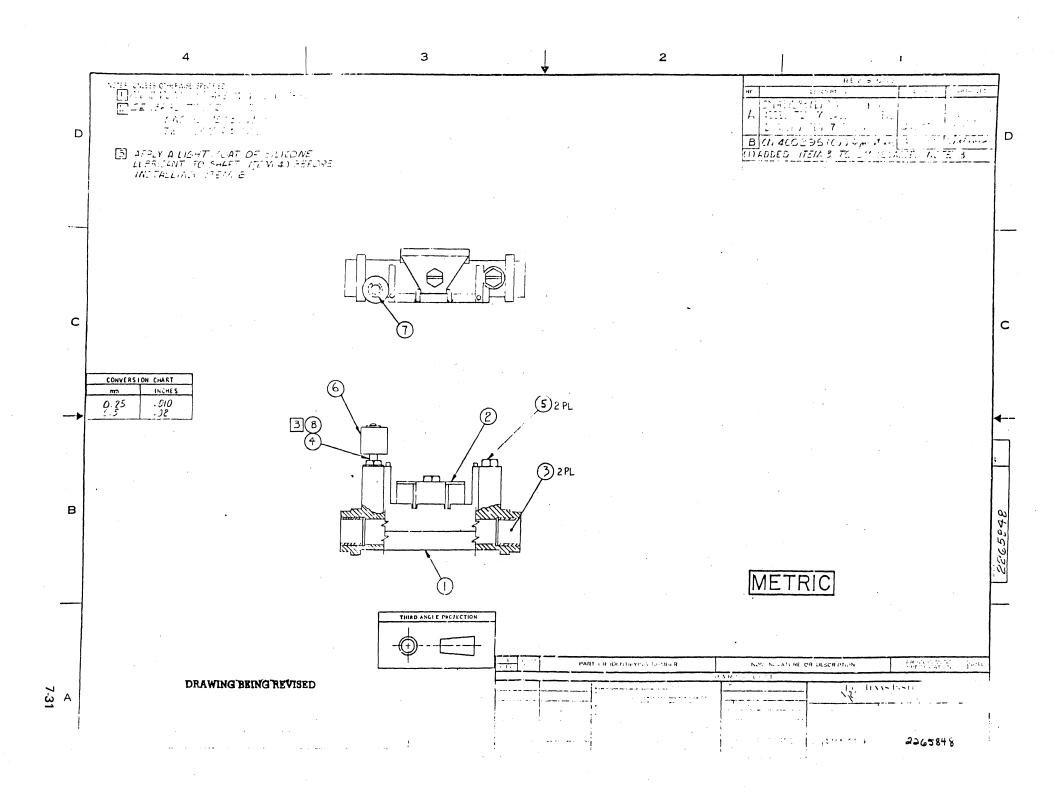




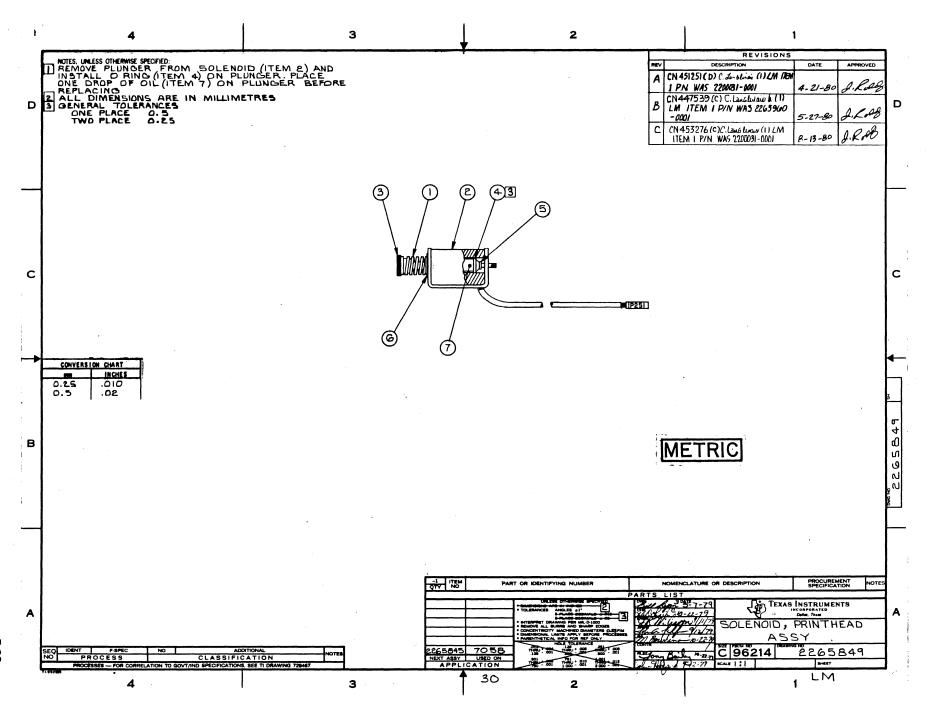
-LIST OF MATERIALS-**DCTOBER 24, 1980** PART NUMBER DESCRIPTION. REV 2265845-0001 MECH ASSY, STEPPER MOTOR W/PRINTHEAD ITFM. QUANTITY. 0001 00001.000 0941348-0001 FRAME, MECHANISM, 743/745/765 FΑ 0002 00001.000 2265852-0001 MOTOR. DRIVE PRINTER ASSY EΑ 1238-5852-000 0003 00001.000 2265849-0001 SOLENOID, PRINTHEAD ASSY EΑ 1238-5849-000 0004 00001.000 2265848-0001 CARRIAGE ASSY, PRINTHEAD EA 1238-5848-000 00001.000 0983818-0001 0005 WINDOW ASSY FΛ 1222-3818-000 0006 00001.000 0983873-0001 SPRING, DANCER EΑ 1224-3873-021 0007 00001.000 2200030-0001 DEFLECTOR, PAPER EΑ 1224-0030-013 00001.000 2265827-0001 0008 ARM, PULLEY TENTION EA 1238-5827-016 0009 00001.000 0983883-0002 SPACER, PULLEY- PMT EΑ 1224-2883-016 00001.000 0010 0199488-0001 BALL BEARING EΑ 0011 00001.000 0999258-0002 SPRING, CABLE TENSION (MK12) EA 0000-0000-000 0012 00001-000 ROLLER, PAPER DRIVE 0999263-0003 FA BEARINGS, SLEEVE-FLANGED NYLON .2510 1D 0013 00001.000 0772684-0005 EA THM -4L1 00001-000 PULLEY, IDLER 0014 2265863-0001 EΑ 1238-0000-000 0015 00001-000 0983872-0001 ROLLER, DANCER EΑ 1224-3872-021 PIVOT 0016 00002.000 0983874-0001 EΑ 1224-3874-000 BEARING, ROD SUPPORT 0018 00002-000 0983889-0001 FA 1224-3889-020 0019 00001.000 ROD, CARRIAGE 0983884-0001 EΑ 1224-3884-035 0020 00001.000 2265930-0001 BAIL BRACKET, 780 SERIES EA 1238-5930-017 00002.000 0021 0983938-0001 BAIL RETAINER FΑ 1224-3938-029 0022 00002.000 0972485-0001 WASHER, STEEL-THRUST EΑ 0023 00001.000 2265925-0001 BELT, TIMING, CARRIAGE EΑ 0024 00002-000 0972988-0013 SCREW 4-40 X .250 PAN HEAD CRES FΑ 0025 00008.000 0416622-0011 WASHER #4 FLAT FA OPI - AN960C4L 0026 00008.000 0411104-0135 WASHER, LOCK-SPRING, HELICAL, #4 QPL - MS35338-135 00001-000 0999246-0001 PAD, FRICTION 0027 EΑ 002 R AR 0232573-0001 OII #43 TERRESTIC EA HUM LUBRICANT SILICONE GRS LT GR 2 OZ TUBE 0029 AR 0232334-6050 TU SEE TI- DRAWING 0030 00001-000 0983916-0001 SPRING, EXTENSION EΑ 0031 00005.000 0972988-0015 SCREW 4-40 X .375 PAN HEAD CRES EΑ 0032 00001-000 0989712-0002 LABEL, WARNING, 743/745/763/765 FΛ

-LIST OF MATERIALS-

PART NUMBER REV 2265845-0001 F				
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0034	00001.000	2265899-0001	MOTOR ASSY, PAPER ADVANCE	E
0035	00001-000	0941347-0001	RETAINER, BEARING 1224-1347-000	· E
0036	00001-000	2265926-0001	GEAR+ PAPER ADVANCE	. E
0037	00001-000	0941346-0001	BAIL,LINK 1224-1346-006	E
0039	AR	0802749-0222	ADHESIVE, THREAD SEALING AND LOCKING LOC - TL-222	Ε
0044	00001.000	2265867-0002	BUMPER, LEFT	E
0045	00002.000	0085936-0018	EYELET -121 BARREL OD X-219 LG FLANGE USH - #SE-47	Ε
0046	00001-000	0972990-0017	SCREW 4-40 X -625 FLT HEAD CRES	· E
0047	00001-000	0416453-0021	NUT,PLAIN,4-40 UNC-2B HEX,CRES,SMALL QPL - NAS671-C4	E
0052	00001-000	0411027-0803	WASHER -125 X -250 X -022 FLAT CRES QPL - MS15795-803	E
0054	00002.000	0972988-0017	SCREW 4-40 X .500 PAN HEAD CRES	E
0055	00002.000	0411101-0057	LOCKWASHER # 4 EXTERNAL TOOTH CRES QPL - MS35335-57	E
0056	REF	2265919-9901	MECH. TEST PROCEEDURE, 780 SERIES	E
0057	00001-000	2206586-0001	PRINTHEAD ASSY, EPN 3632 1228-1586-000	E
0058	00001-000	2265975-0001	LABEL.P/N AND REV. LEVEL 1238-0000-000	E
0059	00001-000	2265976-0001	LABEL, TEST, DATE, S/N, SITE CODE 1238-0000-000	E
0060	00001.000	2265983-0001	PAD, TENSION PULLEY ARM	E
0061	00001.000	2265980-0001	TAG, BEARING, 780 SERIES	E
0062	00001-000	2265933-0002	STRIP.FOAM.SHELF	E
9999	00002.000	0239999-9999	COST, SHRINKAGE	E

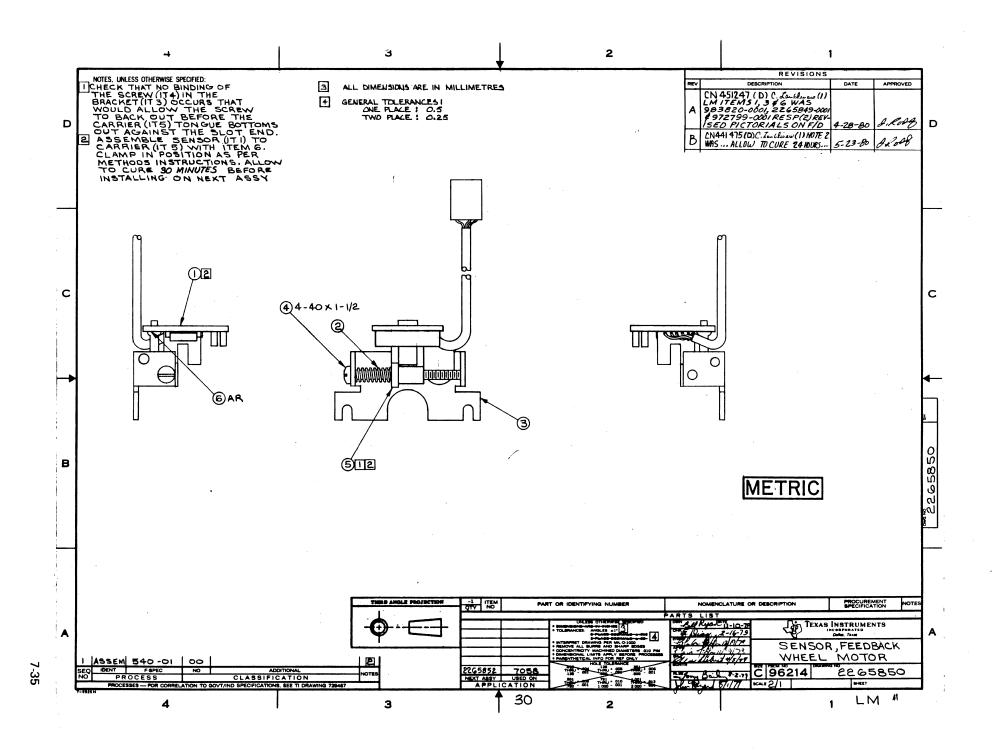


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OCTOBER	24, 1980			
PART NU 2265846			ON ASSY, PRINTHEAD	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0001	00001.000	2265846-0001	CARRIAGE, PRINT HEAD 1238-5846-003	EA
0002	00001.000	2265918-0001	CLAMP, BELT, TIMING 1238-5918-000	EA
0003	00002.000	2210152-0003	BEARING, SLEEVE, PLASTIC, .2525 A DIA.	EA
0004	00001.000	2265853-0001	AXLE SCREW, THREAD FORMING	EA
0005	00002.000	0972679-0009	SCREW #4-20 X 3/8*LG THD FORM.HEX	EA
0006	00001-000	2265865-0001	WHEEL, CARRIAGE 1238-5865-002	EA
0007	00001 -000	0056987-0009	RING.RETAINING.TYPE "E"	EA

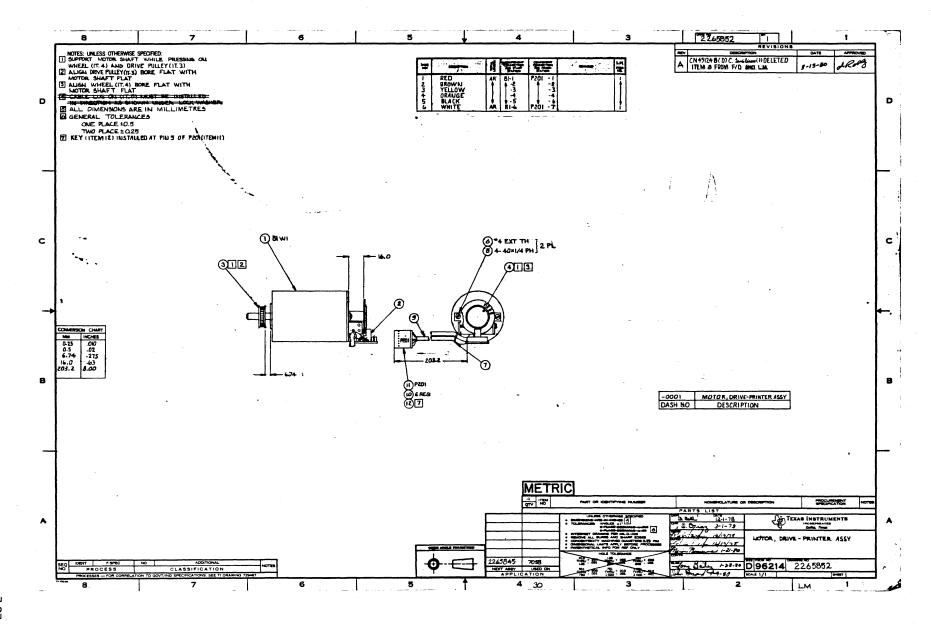


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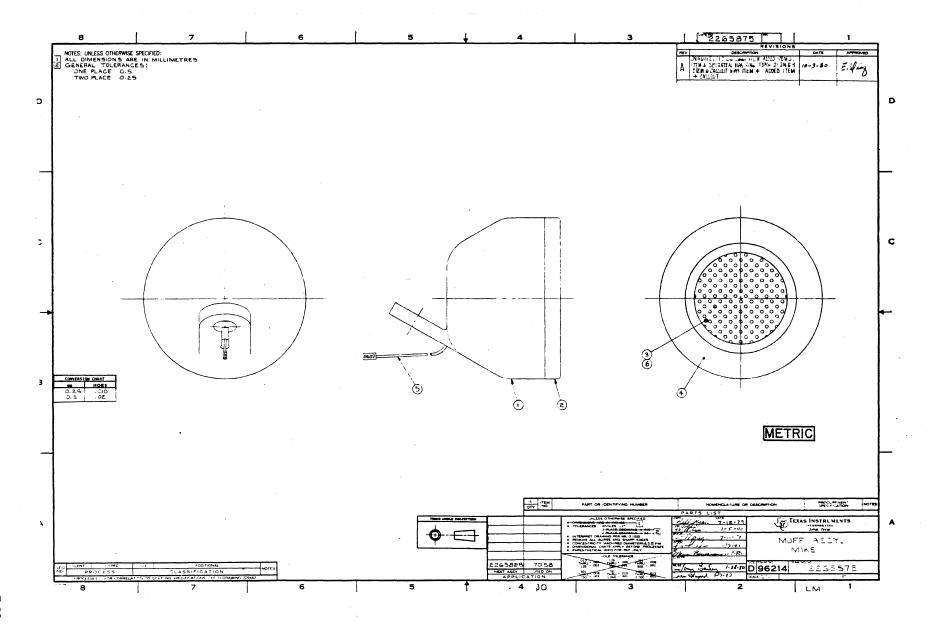
PART NU	MBER REV	DESCRIPTI	ON	
2265849			PRINTHEAD ASSY	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0001	00001.000	2200031-0003	SPRING. HEAD LIFT (STEPPER)	E
0002	00001-000	0983816-0002	SOLENOID, PRINTHEAD 1224-3316-000	ε
0003	00001-000	0983900-0001	KNOB, PLUNGER 1224-3900-014	E
0004	00001-000	0983969-0001	O-R I NG	E
0005	00001.000	0983968-0001	WASHER RUBBER 1/32 THK GRAY	E
0006	00001.000	0983915-0001	WASHER, SHOULDER SPRING	E
0007	AR	0232573-0001	OIL #43 TERRESTIC	E



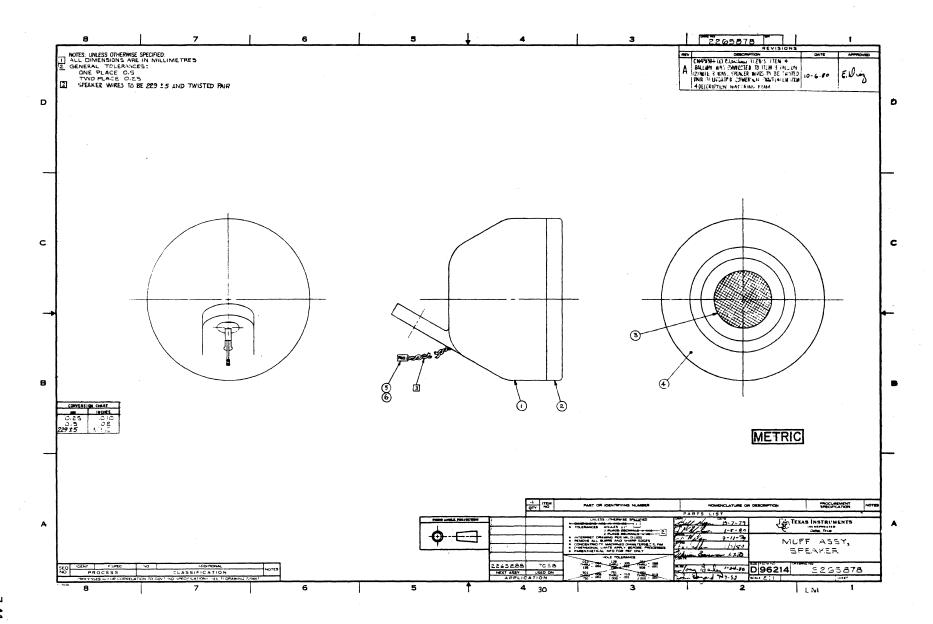
OCTOBER	24, 1980			
PART NU 2265850	MBER REV 0001 B		ONEDBACK,WHEEL MOTOR	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	. UM
0001	00001.000	2265951-0001	SENSOR ASSY, 780 SERIES 1238-5101-021	E
0002	00001.000	0960177-0001	SPRING, FEEDBACK SENSOR	E
0003	00001.000	2265861-0001	BRACKET, MOUNTING, FEEDBACK SENSOR 1238-5861-017	Ε
0004	00001-000	0972988-0023	SCREW 4-40 X 1.50 PAN HEAD CRES	E
0005	00001.000	0983919-0001	CARRIER 1224-3919-012	Ε
0006	AR	0996527-0001	ADHESIVE,LOCTITE 416 059724-16SUPERBONDER	Ε



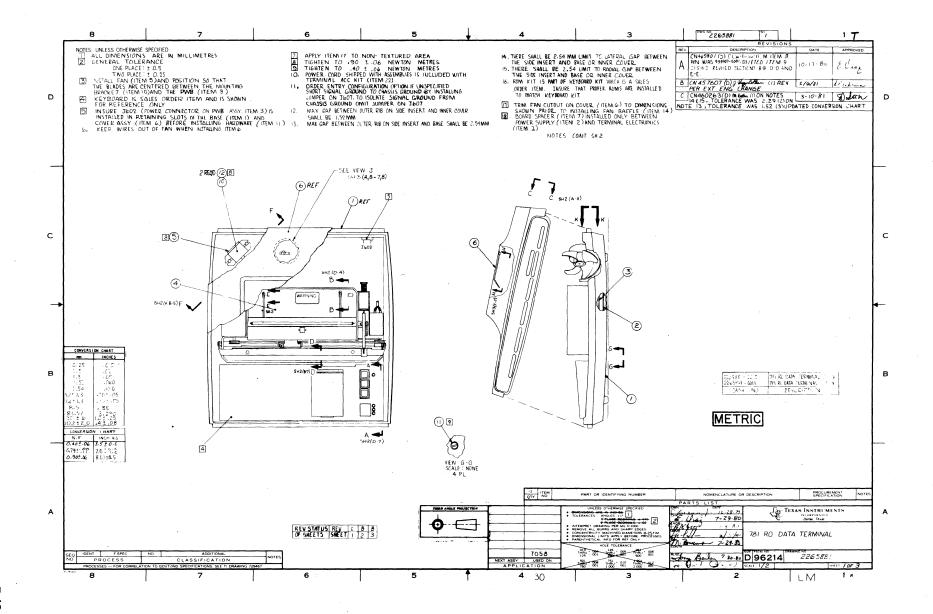
PART NU 2265852	MBER REV -0001 A		ON	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	M
0001	00001-000	2265922-0001	MOTOR, STEPPER	E
0001A			81	
0002	00001.000	2265850-0001	SENSOR, FEEDBACK, WHEEL MOTOR	E
0003	00001.000	2265864-0001	PULLEY, DRIVE 1238-0000-000	E
0004	00001.000	2265847-0001	WHEEL, FEEDBACK SENSOR, PRTHD STEPPING MTR	E
0005	00002.000	0972988-0013	SCREW 4-40 X -250 PAN HEAD CRES	E
0006	00002.000	0411101-0057	LOCKWASHER # 4 EXTERNAL TOOTH CRES	E
0007	00001.000	0418212-0040	STRAP, TIEDOWN, ADJUSTABLE, PLASTIC OPL - MS3367-4-9	E
0009	00000.500	0972436-0012	INSULATION, FLEXIBLE	F
0010	00006.000	0972104-0001	CONTACT ELEC-LOCKING.WIRE-TO.025 SQ POST AMP - 87124-1	E
0011	00001.000	0972484-0007	CONNECTOR HOUSING TPINS	E
0011A			P201 000779-1-87175-5	
0012	00001-000	0800335-0001	KEY, POLARIZATION, CONNECTOR	Ε

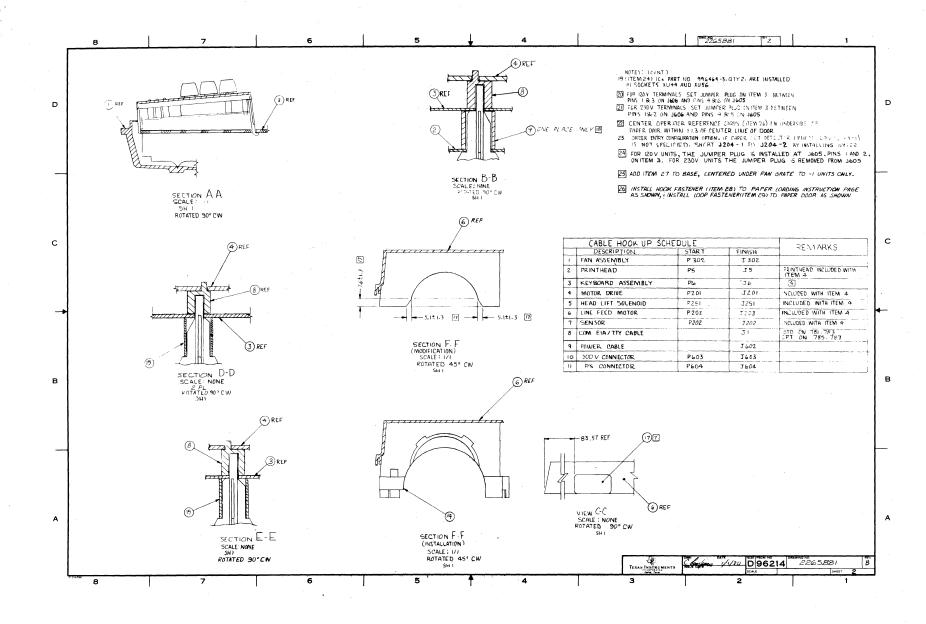


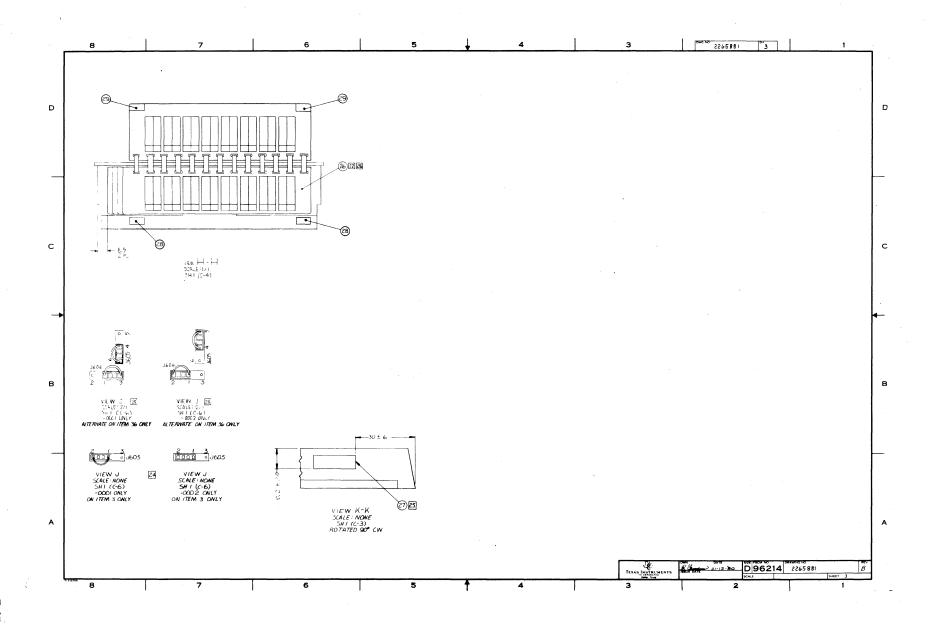
PART NU 2265875		REV A	DESCRIPTION MUFF ASSY	ON , MIKE	
ITEM.	QUANTI	TY.	COMPONENT	DESCRIPTION	UM
0001	00001.	000	2265879-0001	MUFF , OUTER 1238-5879-003	EV
0002	00001.	000	2265874-0001	MUFF , INNER , MIKE 1238-5874-002	EA
0003	00001 -	.000	2211333-0001	MICROPHONE,1200 BPS SEE T -I DRAWING	EA
0004	00001.	000	2265933-0001	STRIP, FOAM, MUFF	ΕA
0005	00001.	000	0983834-0001	WIRING HARNESS, MICROPHONE ACOUSTIC CPLR 1224-3834-060	EA
0006	00001-	000	2265904-0001	RING. FOAM. MICROPHONE	E/



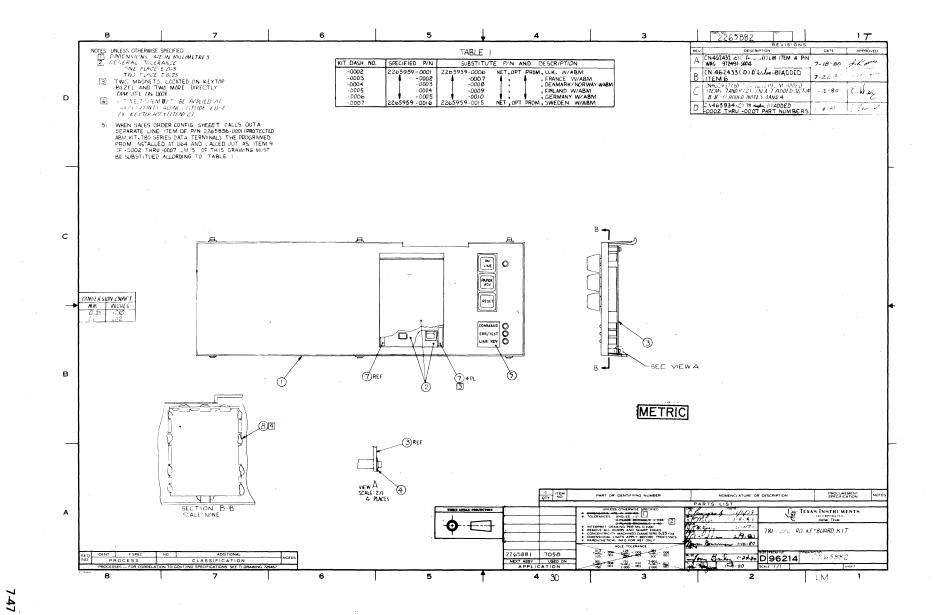
FEBRUAR	Y 03, 1981			
	MBER REV -0001 B	DESCRIPTI	ON	
ITEM.	OUANTITY.	COMPONENT	DESCRIPTION	UM
0001	00001.000	2265879-0001	MUFF , OUTER 1238-5879-005	ΕA
0002	00001.000	2265880-0001	MUFF , INNER , SPEAKER 1238-5880-003	EA
0003	00001.000	2211305-0001	SPEAKER, 1200 BDS ACQUISTIC COUPLER SEE TI- DRAWING	EA
0004	00001.000	2265933-0001		ΕA
0005	00001.000	0972484-0002	CONNECTOR HOUSING 2 CONTACT	ΕA
0005A			P401 T18 -7175-6	
0006	00002.000	0972104-0001	CONTACT ELEC-LUCKING, WIRE-TO.025 SQ POST AMP - 87124-1	EA
0007	00001.000	2266004-0001	RING, SPEAKER, NEOPRENE 1238-6004-000	ΕA
8000	AR	0996527-0001	ADHESTVE,LOCTITE 416 059724-16SUPERBONDER	EA
0009	AR	0415232-0001	COMPOUND, SILICONE GREASE	TU



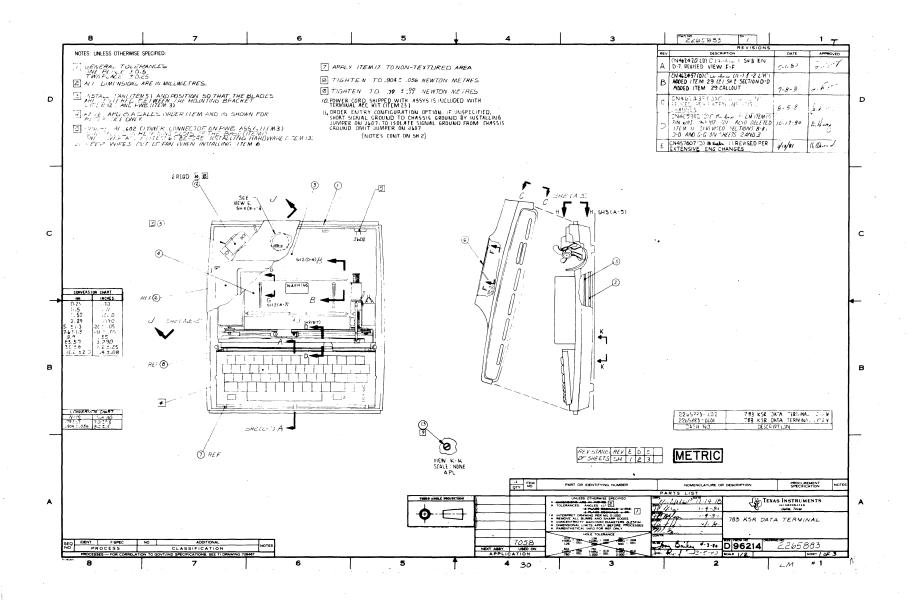


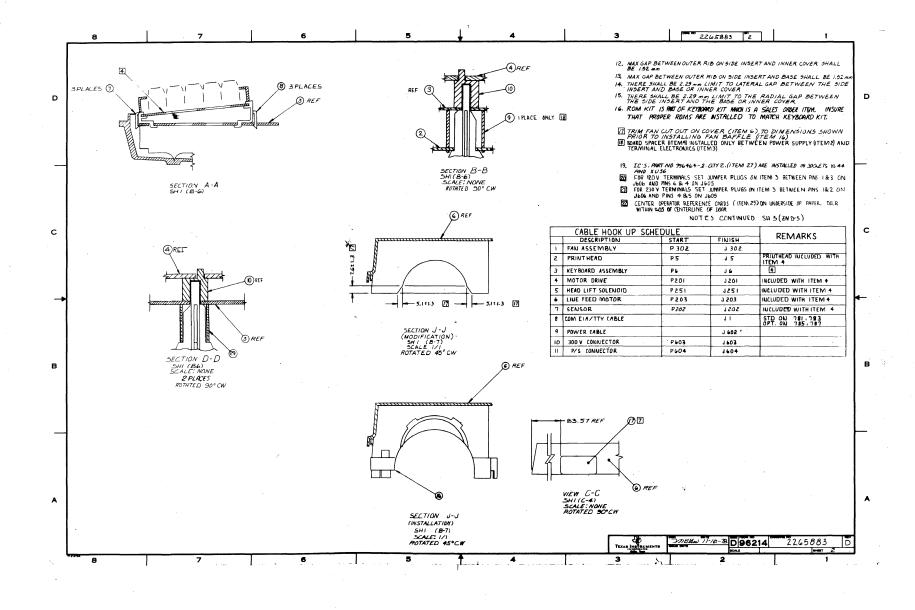


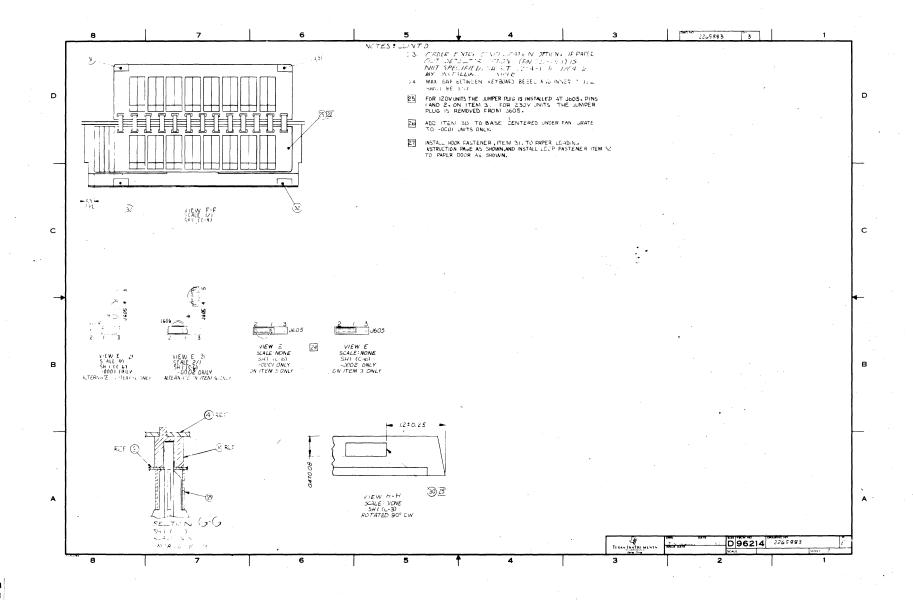
PART NU 2265881	JMBER REV L-0001 A	DESCRIPTI 781 RO DA	ONION	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0001	00001-000	2265962-0001	BASE ASSEMBLY W/ GLUED DOOR 1238-5962-000	· E
0002	00001.000	2265835-0001	POWER SUPPLY ASSY, 780 SERIES, 120/230V 1238-3501-013	E
0003	00001-000	2265830-0001	PMB ASSY, 780 SERIES DATA TERMINAL	E
0004	00001-000	2265845-0001	MECH ASSY, STEPPER MOTOR W/PRINTHEAD 1238-5845-011	•
0005	00001.000	0999232-0001	FAN ASSEMBLY,763/765 1222000	1
0006	00001.000	2265886-0001	COVER ASSY,780 SERIES W/O MUFFS 1238-5886-000	E
0007	00001.000	0999228-0001	SPACER, BOARD, 763/765 1222-9228-020	
8000	00004.000	2265982-0001	MOUNT, MECHANISM, ISOLATION	E
0010	00001.000	0983863-0001	BRACKET,FAN MOTOR,743/745/763/765/820 1224-3863-023	1
0011	00004.000	0972988-0073	SCREW.4-40 X 2.000 PAN HEAD CRES	. 6
0012	00002.000	2211412-0001	SCREW, PLASTITE, W. WASHER, 4-20 X 3/8 SEE TI-DRAWING	
0014	00001.000	0999240-0001	BAFFLE ADAPTOR, FAN 1222-9240-011	
0015	00003-000	2265974-0001	STANDOFF, TOP BOARD	. (
0017	00001.000	2265929-0001	1.D. PLATE, 781, 120V 1238-2901-000	E
0017A			983908-1 CAN BE USED AS ALT 1238-2901-000	
0019	REF	2265857-9901	TEST PROCEDURE, SIL	. €
0020	REF	2265858-9901	TEST PROCEDURE, RUN-IN	E
0021	REF	2265859-9901	TEST PROCEDURE, MANUAL, PDT	E
0022	00001.000	2265939-0001	TERM ACC KIT, 781 DOMESTIC 1238-0000-000	ŧ
0023	REF	2265862-9701	MANUAL, MAINTENANCE, 780 SERIES DATA TER	E
0024	00002.000	0996464-0003	IC,2114 1024X4-BIT STATIC RAM 001295-TMS4045-45NL	Ε
0025	00022-000	0996943-0001	LABEL, SELF-DESTRUCT, .656 X .25 085480-377	E
0026	00001.000	2265927-0001	OP. REF. CARD ASSY, 781 RO DATA TERM	Ε
9999	00002.550	0239999-9999	COST, SHRINKAGE	Ε



OCTOBER	24, 1980			
PART NU 2265882	MBER REV 2-0001 C		ONO KYBD KIT	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0001	00001.000	2265866-0001	BEZEL,781 DATA TERMINAL 1238-5866-002	E
0002	00001.000	2265895-0001	KEYTOP ASSY , 781 DATA TERMINAL 1238-0000-000	E
0003	00001.000	2265915-0001	781 RECEIVE ONLY KEYBOARD 1238-5915-009	E
0004	00004-000	0972491-0002	RING,RETAINING Wal -5115-12S	E
0005	00001-000	2265893-0001	LABEL, STATUS 781 DATA TERMINAL	E
0006	00001-000	2265860-0002	ROM KIT, 781 1238-5862-000	E
0007	00004.000	2265997-0001	MAGNET, FLEXIBLE, ADHESIVE BACKED	EA
8000	00000-150	2265954-0001	ADHESIVE, HOT-MELT 1238-5954-000	E

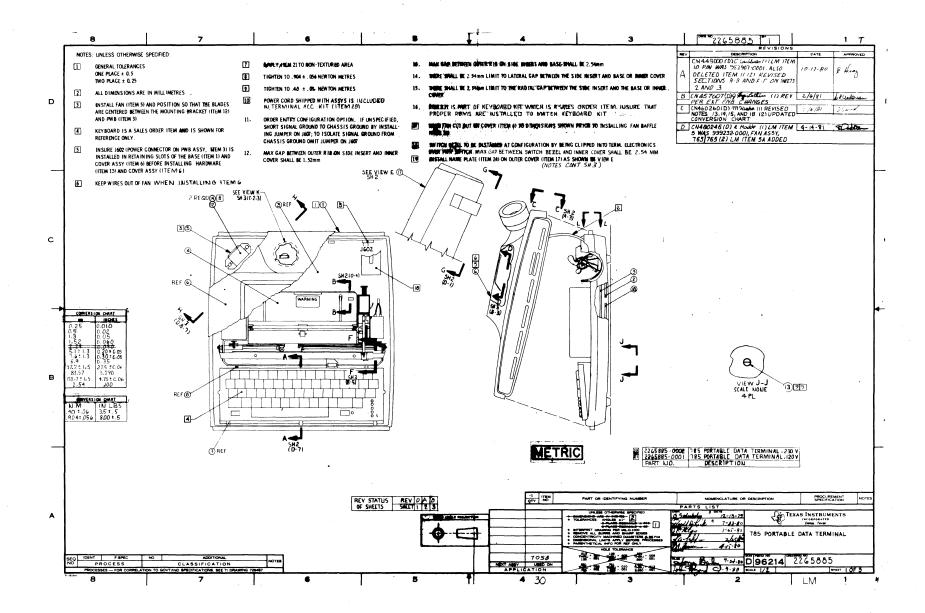


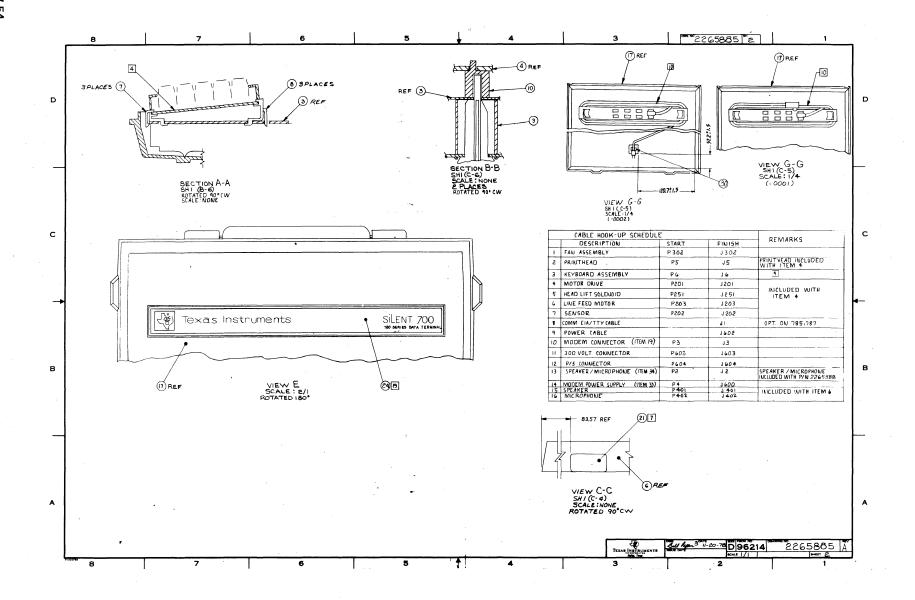


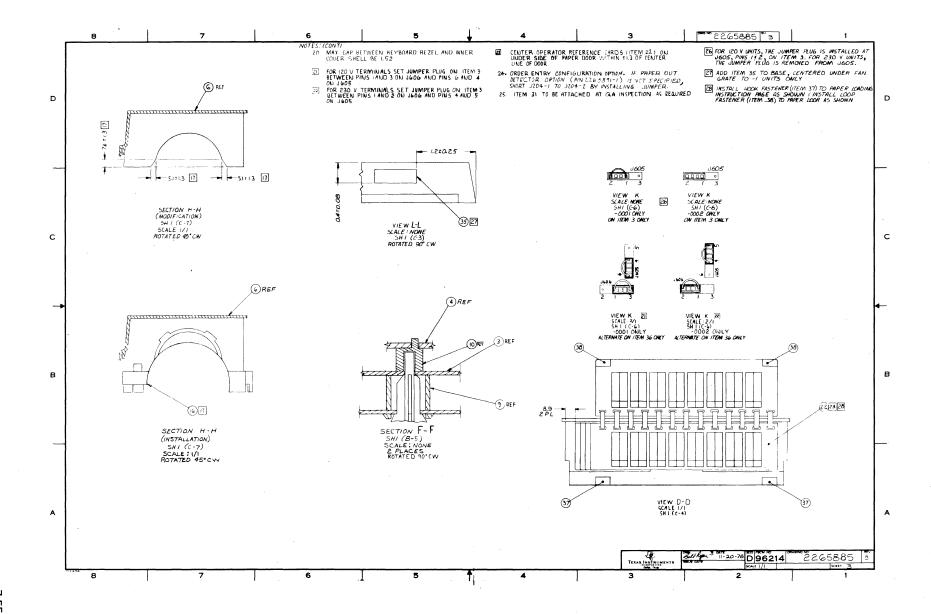


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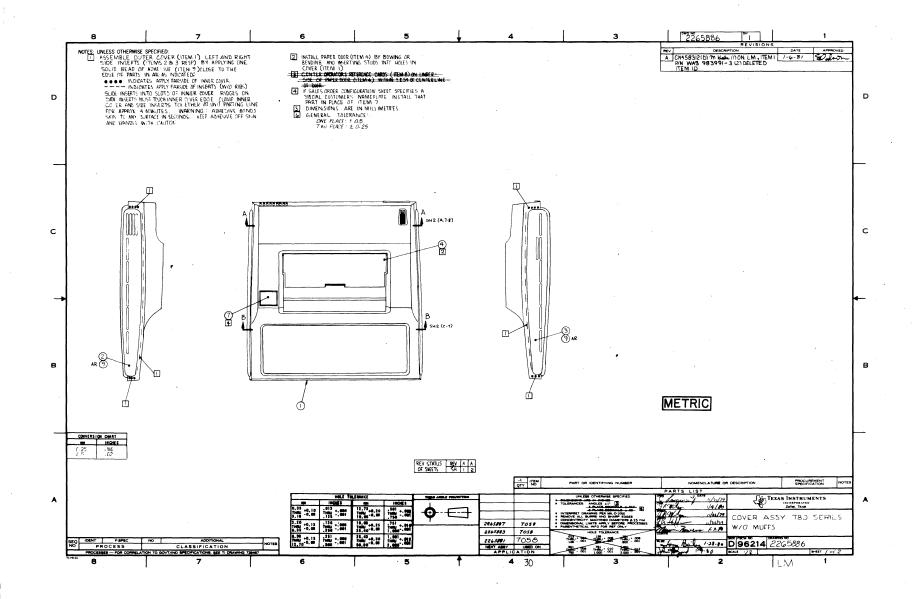
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OCTOBER	24, 1980		•	
PART NUM 2265883-			ION Data terminal, 120V	
ITEM.	QUANTITY.	COMPONENT	DE SCRIPTION	UM
0001	00001.000	2265962-0001	BASE ASSEMBLY W/ GLUED DOOR 1238-5962-000	Ε
0002	00001-000	2265835-0001	POWER SUPPLY ASSY, 780 SERIES, 120/230V 1238-3501-013	E
0003	00001.000	2265830-0001	PHB ASSY, 780 SERIES DATA TERMINAL 1238-3001-017	E
0004	00001-000	2265845-0001	MECH ASSY, STEPPER MOTOR W/PRINTHEAD 1238-5845-011	E
0005	00001.000	0999232-0001	FAN ASSEMBLY,763/765 1222000	E
0006	00001.000	2265886-0001	COVER ASSY,780 SERIES W/O MUFFS 1238-5886-000	E
0007	00003-000	0983905-0001	CLIP,KEYBOARD,FRONT 1224-3905-016	E
8000	00003.000	0983904-0001	CLIP,KEYBOARD,REAR 1224-3904-019	E
0009	00001-000	0999228-0001	SPACER, BOARD, 763/765 1222-9228-020	E
0010	00004.000	2265982-0001	MOUNT, MECHANISM, ISOLATION	`E/
0012	00001.000	0983863-0001	BRACKET,FAN MOTOR,743/745/763/765/820 1224-3863-023	E
0013	00004.000	0972988-0073	SCREW+4-40 X 2.000 PAN HEAD CRES	E
0014	00002.000	2211412-0001	SCREW,PLASTITE,W. WASHER, 4-20 X 3/8 SEE TI-DRAWING	E
0016		0999240-0001	BAFFLE ADAPTOR, FAN 1222-9240-011	E
0017	00001.000	2265929-0002	I.D. PLATE, 783, 120V 1238-2902-000	E
0017A			983908-1 CAN BE USED AS ALT 1238-2902-000	
0020	REF	2265857-9901	TEST PROCEDURE, SIL	.E/
0021	REF	2265858-9901	TEST PROCEDURE, RUN-IN	E
0022	REF	2265859-9901	TEST PROCEDURE, MANUAL, PDT	E
0023		2265939-0002	TERM ACC KIT, 783 DOMESTIC 1238-0000-000	E
0024	REF	2265862-9701	MANUAL, MAINTENANCE, 780 SERIES DATA TER	E
0025	00001.000	2265941-0001	OP. REF. CARD ASSY, 783 KSR DATA TERM	E/
0027	00002.000	0996464-0003	IC,2114 1024X4-BIT STATIC RAM 001295-TMS4045-45NL	E/
0028	00022.000	0996943-0001	LABEL, SELF-DESTRUCT, .656 X .25 085480-377	E#
0029	00003.000	2265974-0001	STANDOFF, TOP BOARD	EA
9999	00002.900	0239999-9999	COST, SHRINKAGE	E

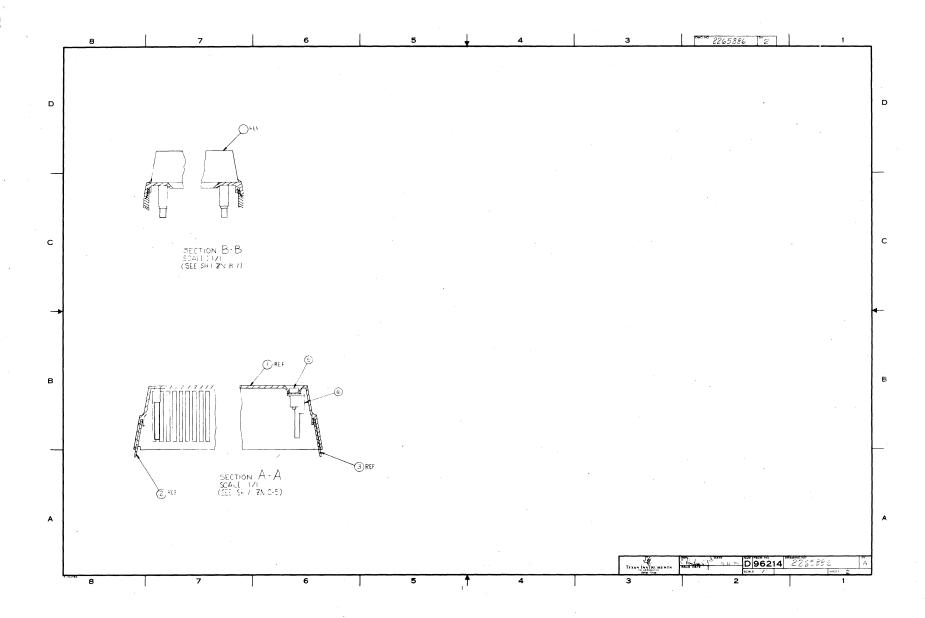




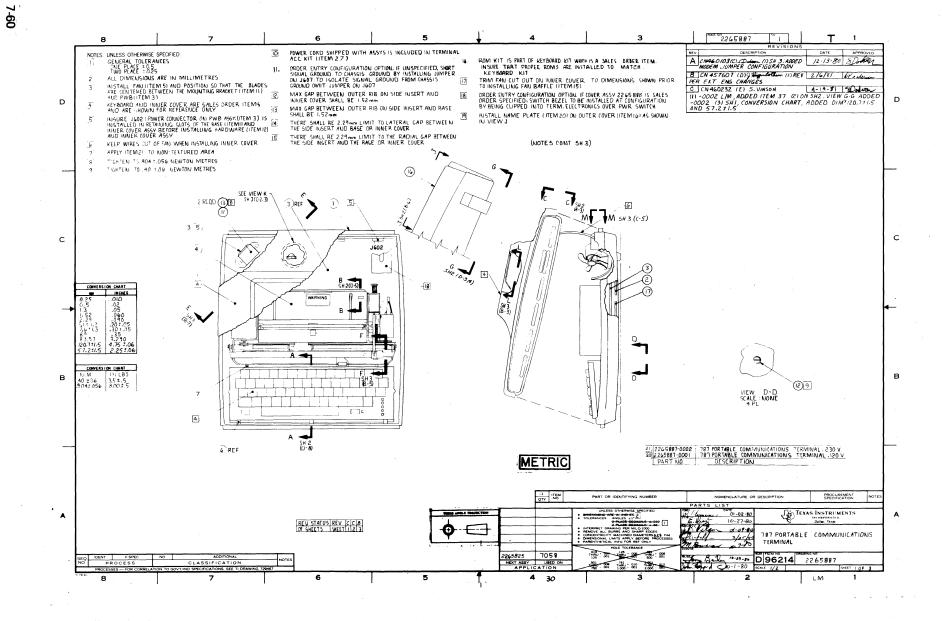


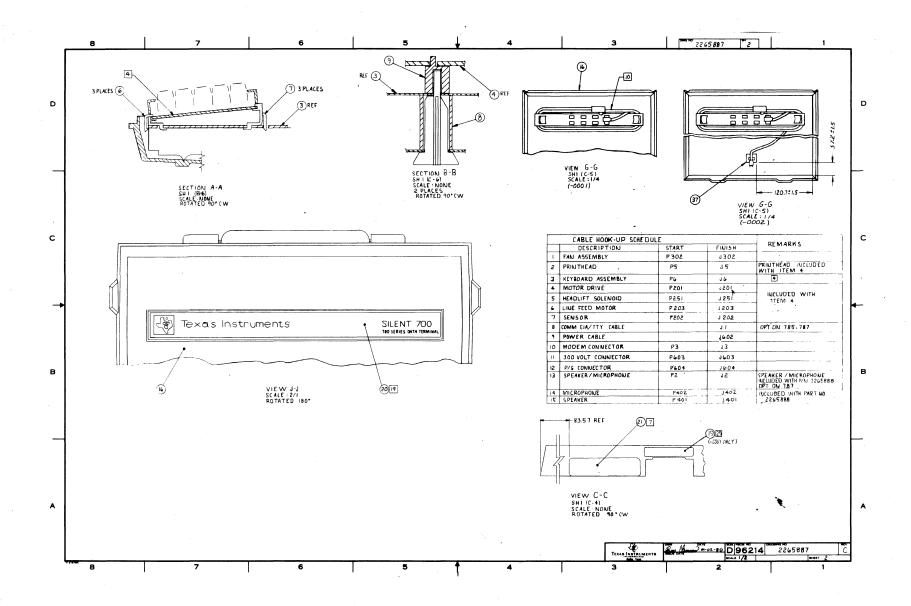
OCTOBER	24, 1980		OF MATERIALS	
PART NUI 2265885-	MBER REV		ON	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	M
0001	00001.000	2265962-0001	BASE ASSEMBLY W/ GLUED DOOR	EA
0002	00001.000	2265835-0001	1238-5962-000 POWER SUPPLY ASSY, 780 SERIES, 120/230V	EA
0003	00001.000	2265830-0001	1238-3501-013 PWB ASSY: 780 SERIES DATA TERMINAL	EA
0004	00001-000	2265845-0001	1238-3001-017 MECH ASSY, STEPPER MOTOR W/PRINTHEAD	EA
0005	00001.000	0999232-0001	1238-5845-011 FAN ASSEMBLY,763/765	EA
0006	00001-000	2265888-0001	1222000 COVER ASSY,780 SERIES W/MUFFS	EA
0007	00003.000	0983905-0001	1238-5888-000 CLIP,KEYBOARD,FRONT	EA
0008	00003.000	0983904-0001	1224-3905-016 CLIP,KEYBOARD,REAR	EA
0009	00004.000	0999228-0001	1224-3904-019 SPACER, BOARD, 763/765	EÁ
0010	00004.000	2265982-0001	1222-9228-020 Mount, Mechanism, isolation	EA
0012	00001.000	0983863-0001	BRACKET,FAN MOTOR,743/745/763/765/820	EA
0013	00004.000	0972988-0073	1224-3863-023 SCREW.4-40 X 2.000 PAN HEAD CRES	EA
0014	00002.000	2211412-0001	SCREW, PLASTITE, W. WASHER, 4-20 X 3/8	ΕA
0016	00001.000	0999240-0001	SEE TI-DRAWING BAFFLE ADAPTOR, FAN	EA
0017	00001-000	0983809-0001	1222-9240-011 Outer Cover Assy	ΕΛ
0018	00001.000	2265876-0003	1224-8090-028 300/1200 BPS ORIG ONLY MODEM	EA
0019	00001.000	2265826-0001		EA
0021	00001.000		CABLE ASSY ; INTERNAL MODEM 1238-5826-009 I.D. PLATE, 785, 120V	
	00001-000	2265929-0003	1238-2903-000	EA
0021A			983908-1 CAN BE USED AS ALT 1238-2903-000	
0022	00001.000	2265942-0001	OP. REF. CARD ASSY, 785 PORT DATA TERM	EA
0024		2265928-0001	NAMEPLATE, OUTER COVER, 780 SERIES	EA
0025	REF	2265857-9901	TEST PROCEDURE, SIL	EA
0026	REF	2265858-9901	TEST PROCEDURE, RUN-IN	EA
0027	REF	2265859-9901	TEST PROCEDURE, MANUAL, PDT	EA
0028	00001.000	2265939-0003	TERM ACC KIT, 785 DOMESTIC 1238-0000-000	EA
0029	REF	2265862-9701	MANUAL, MAINTENANCE, 780 SERIES DATA TER	EA
0031	00022.000	0996943-0001	LABEL, SELF-DESTRUCT, .656 X .25 085480-377	EA
0033	00001-000	2265844-0001	CABLE ASSY, MODEM POWER SUPPLY 1238-5844-008	EA
0034	00001.000	2265932-0001	CABLE ASSY, ACQUSTIC CPLR, 780 SERIES 1238-5932-008	EA
9999	00003-450	0239999-9999	COST, SHRINKAGE	EA

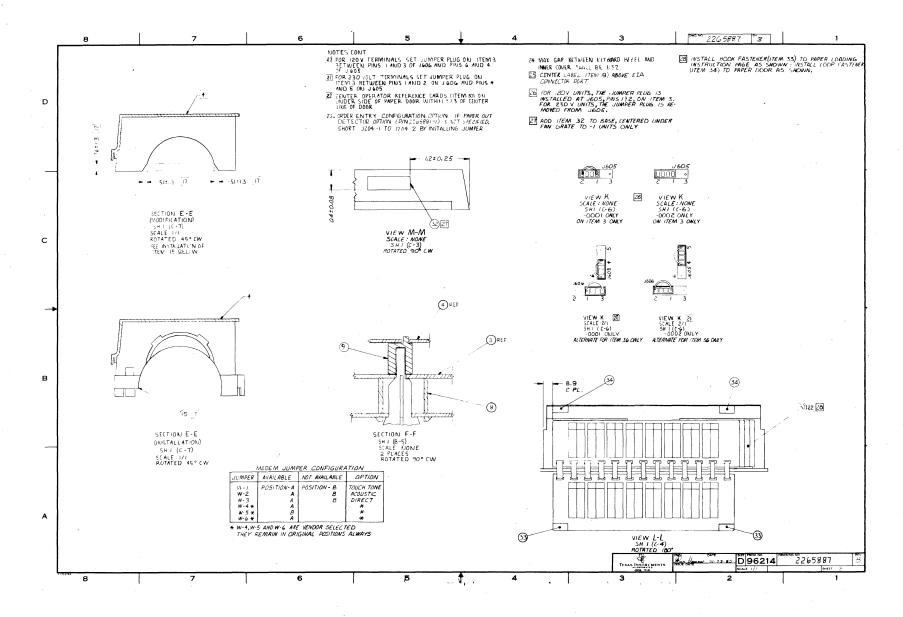




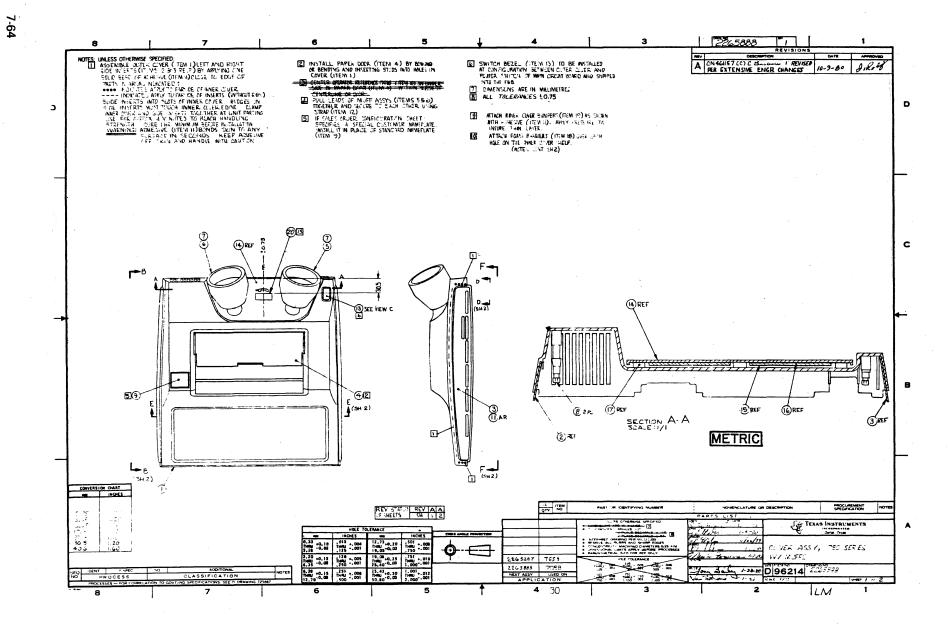
	24, 1980			
	MBER REV 5-0001 *		ON Y,780 SERIES W/O MUFFS	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0001	00001-000	0983991-0003	COVER, INNER, 780 SERIES DATA TERMINAL 1238-9913-003	
0002	00001-000	0999248-0003	INSERT, LEFT SIDE W/O XMT LEV ADJ, VENTED 1224-0248-010	E
0003	00001-000	0999249-0001	INSERT,RIGHT SIDE,VENTED 1224-9249-020	E
0004	00001.000	0983865-0001	DOOR,PAPER 1224-3865-014	Ę
0005	00001.000	0983931-0001	ADAPTER SWITCH 1224-3931-011	E
0006	00001-000	2200040-0001	COLLAR, SWITCH 1224-0040-011	Ε
0007	00001-000	2265873-0001	NAMEPLATE , INNER COVER	E
0009	AR	0996527-0001	ADHESIVE, LOCTITE 416 059724-16SUPERBONDER	E
0010	00004-000	0772334-0001	FASTNER 4-40 ON-SERT	E

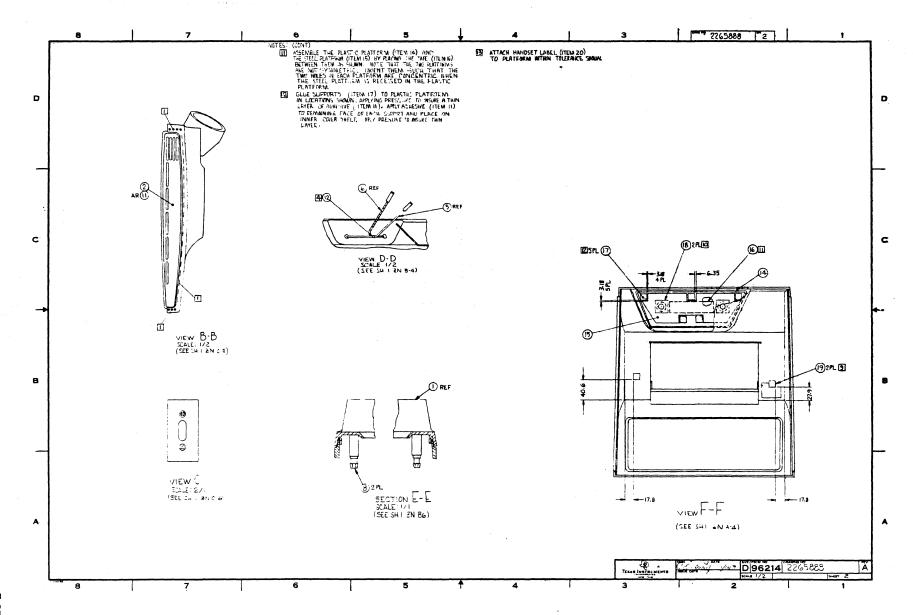




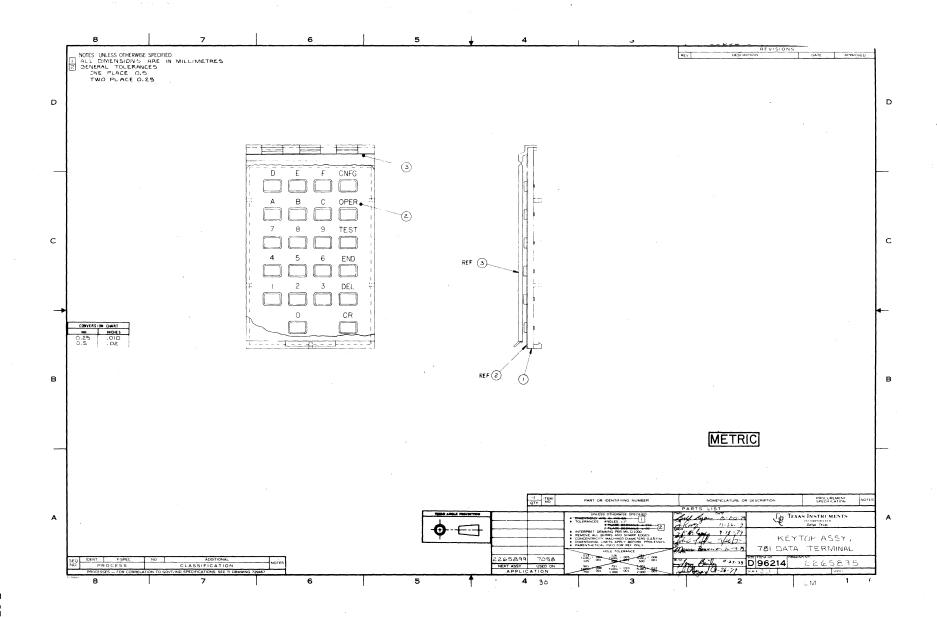


	MBER REV		ONABLE COMM TERMINAL; 120V	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	IM
0001	00001-000	2265962-0002	BASE ASSEMBLY W/ OPENING DOOR 1238-0000-000	Ε
0002	00001.000	2265835-0001	POWER SUPPLY ASSY, 780 SERIES, 120/230V 1238-3501-013	Ε
0003	00001.000	2265830-0001	PWB ASSY, 780 SERIES DATA TERMINAL	E
0004	00001-000	2265845-0001	1238-3001-017 MECH ASSY, STEPPER MOTOR W/PRINTHEAD	Ε
0005	00001.000	0999232-0001	1238-5845-011 FAN ASSEMBLY,763/765	Ε
0006	00003.000	0983905-0001	1222000 CLIP,KEYBOARD,FRONT	Ε
0007	00003.000	0983904-0001	1224-3905-016 CLIP,KEYBOARD,REAR	Ε
			1224-3904-019	
8000	00004.000	0999228-0001	SPACER,BOARD,763/765 1222-9228-020	Ε
0009	00004-000	2265982-0001	MOUNT, MECHANISM, ISOLATION	E
0011	00001.000	0983863-0001	BRACKET,FAN MOTOR,743/745/763/765/820 1224-3863-023	E
0012	00004-000	0972988-0073	SCREW,4-40 X 2.000 PAN HEAD CRES	E
0013	00002.000	2211412-0001	SCREW, PLASTITE, W. WASHER, 4-20 X 3/8 SEE TI-DRAWING	Ε
0015	00001.000	0999240-0001	BAFFLE ADAPTOR, FAN	E
0016	00001-000	0983809-0001	1222-9240-011 Duter Cover Assy	E
0017	00001.000	2265877-0001	1224-8090-028 300/1200 BPS ANSW/ORIG MODEM	E
0018	00001-000	2265826-0001	81177011 Cable assy : Internal modem	Ε
0019	00001.000	2265958-0001	1238-5826-009 Label, 787 FCC registration	E
0020	00001.000	2265928-0001	NAMEPLATE, OUTER COVER, 780 SERIES	Ε
0021	00001.000	2265929-0004	I.D. PLATE, 787, 120V	E
0021A			1238-2904-000 983908-1 CAN BE USED AS ALT	
	00001 000	22/5020 0001	1238-2904-000	
0022	00001.000	2265920-0001	BEZEL, DIRECT CONNECT	6
0024	REF	2265857-9901	TEST PROCEDURE, SIL	6
0025	REF	2265858-9901		E
0026	REF	2265859-9901	TEST PROCEDURE, MANUAL, PDT	E
0027	00001-000	2265939-0004	TERM ACC KIT, 787 DOMESTIC 1238-0000-000	Ε
0028	REF	2265862-9701	MANUAL, MAINTENANCE, 780 SERIES DATA TER	E
0029	00022.000	0996943-0001	LABEL, SELF-DESTRUCT, .656 X .25 085480-377	E
0030	00001.000	2265943-0001	OP. REF. CARD ASSY, 787 PORT COMM TERM	E
0031	00001.000	2265844-0001	CABLE ASSY, MODEM POWER SUPPLY	E
9999	00003.200	0239999-9999	1238-5844-008 COST, SHRINKAGE	E

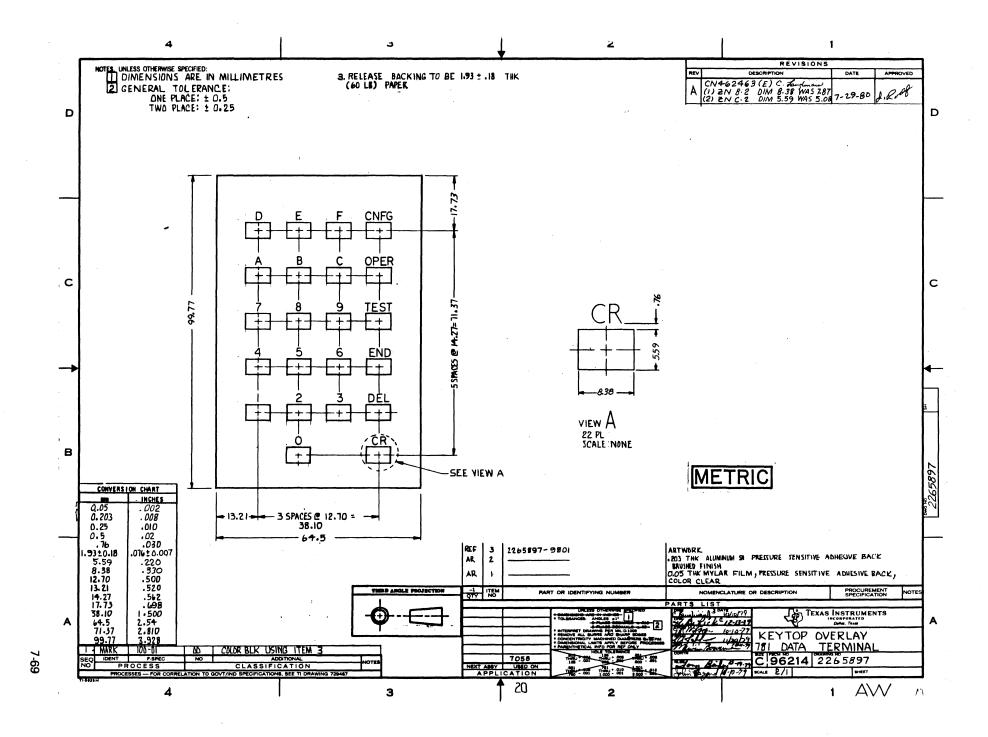


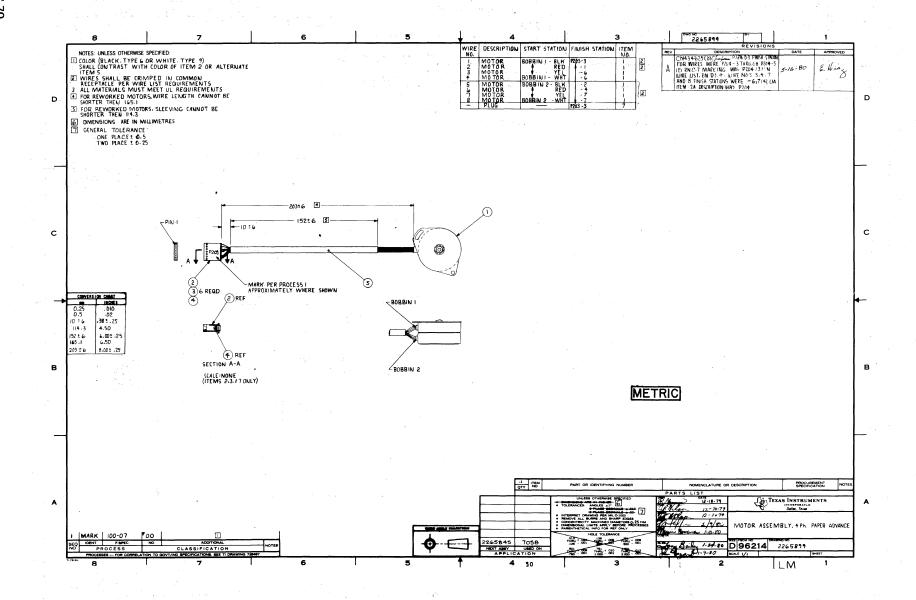


PART NUMBER REV 2265888-0001 A		DESCRIPTIONCOVER ASSY,780 SERIES W/MUFFS		
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0001	00001.000	0983981-0003	COVER, INNER, 780 SERIES DATA TERMINAL	E
0002	00001.000	0999248-0003	INSERT, LEFT SIDE W/O XMT LEV ADJ, VENTED 1224-0248-010	E
0003	00001-000	0999249-0001	INSERT,RIGHT SIDE,VENTED 1224-9249-020	E
0004	00001.000	0983865-0001	DOOR,PAPER 1224-3865-014	E
0005	00001-000	2265875-0001	MUFF ASSY , MIKE 1238-5875-000	E
0006	00001.000	2265878-0001	MUFF ASSY , SPEAKER 1238-5878-000	E
0007	00002-000	0983875-0001	RETAINER,MUFF 1224-3875-018	E
8000	00004.000	0772334-0001	FASTNER 4-40 ON-SERT Pal —nr440004	E
0009	00001-000	2265873-0001	NAMEPLATE , INNER COVER	E
0011	AR	0996527-0001	ADHESIVE, LOCTITE 416 059724-16SUPERBONDER	E
0012	00001.000	0418212-0040	STRAP,TIEDOWN,ADJUSTABLE,PLASTIC QPL - MS3367-4-9	E
0013	00001-000	0937304-0001	BEZEL,SWITCH 1224-7304-015	E
0014	00001.000	2265994-0001	PLATE, UPPER, ACOUSTIC CPLR ISOLATION 1238-5994-000	E
0015	00001.000	2265991-0001	PLATE, LOWER, ACOUSTIC CPLR ISOLATION 1238-5991-000	E
0016	00001.000	2266003-0001	TAPE, DOUBLE COATED, PLATE	E
0017	00005.000	2265993-0001	SUPPORT, PLATFORM, 12.75MM SQ 1238-5993-000	E
0018	00002.000	2265992-0001	BARRIER. FOAM	E
0019	00002.000	2265978-0001	BUMPER, INNER COVER 1238-5978-000	E
0020	00001.000	2265995-0001	LABEL+ HANDSET INSTALLATION	E



OCTOBER	24, 1980			
PART NU 2265895			ONSY , 781 DATA TERMINAL	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	- UM
0001	00001.000	2265894-0001	KEYTOP - BEZEL 781 DATA TERMINAL 1238-5894-003	EA
0002	00001.000	2265897-0001	KEYTOP OVERLAY, 781 DATA TERMINAL	EA
0003	00001.000	2265896-0001	DOOR , KEYTOP 781 DATA TERMINAL 1238-5896-002	EA





OCTOBER 24, 1980

PART NUM 2265899-			ON Y, PAPER ADVANCE	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	JM
0001	00001.000	0999256-0003	MOTOR, STEPPING PAPER DRIVE, MK-12	EA
0002	00001.000	0972484-0007	CONNECTOR HOUSING 7PINS 000779-1-87175-5	EA
0002A			P203 000779-1-87175-5	
0003	00006.000	0972104-0001	CONTACT ELEC-LOCKING, WIRE-TO.025 SQ POST AMP - 87124-1	EA
0004	00001.000	0800335-0001	KEY, POLARIZATION, CONNECTOR BEI65307-001	EA
0005	00000.500	0972436-0012	INSULATION, FLEXIBLE	FT

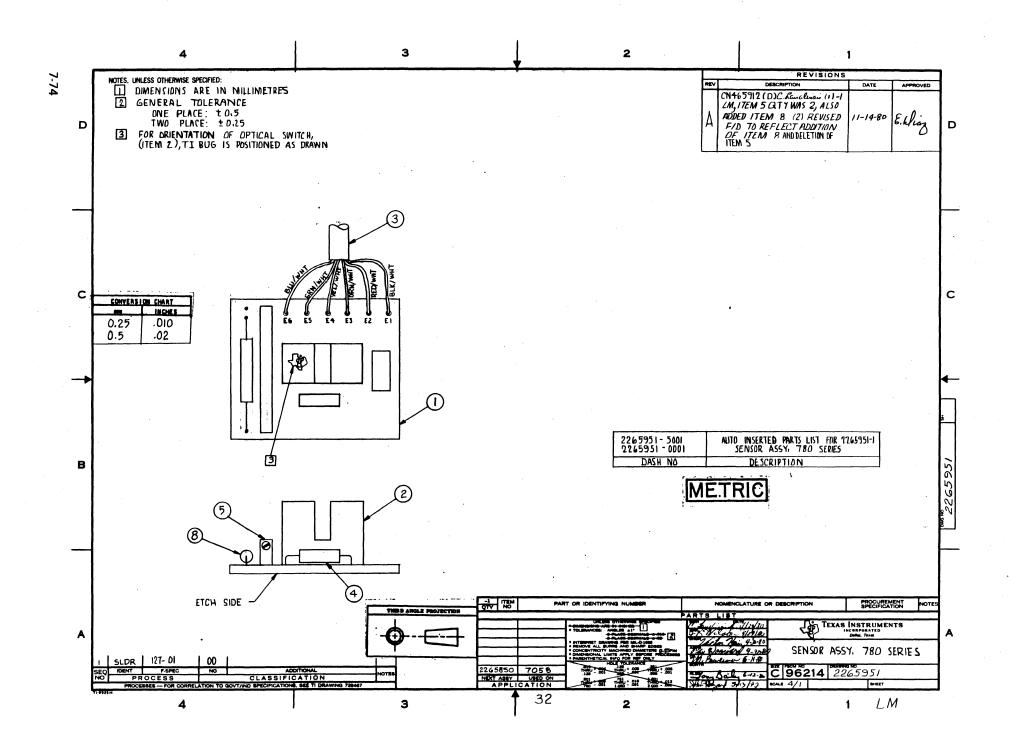
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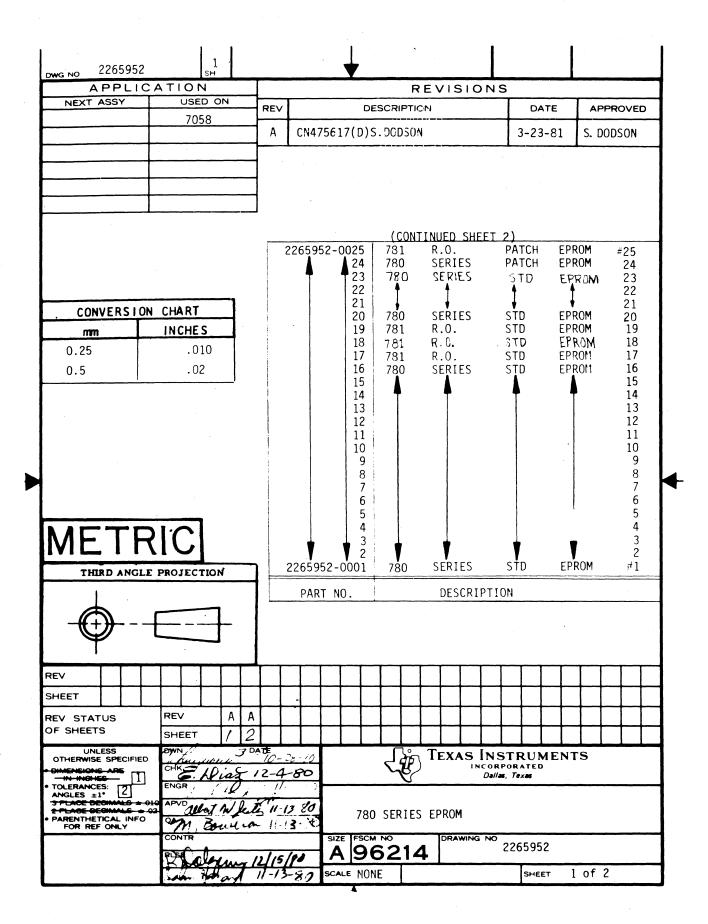
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4 LM

R 24, 1980			
QUANTITY.	COMPONENT	DESCRIPTION	JM
00001.000	2265916-0001	PWB, 781 RECEIVE ONLY KEYBOARD	EA
00002.000	0972519-0023		EA
		J6A, J6B	
00004-000	0539480-0003		EA
		CR1 THRU CR4	
00004.000	0972350-0067		EA
00004-000	0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	EA
		R1 THRU R4	
00001-000	2211263-0001	KEYPAD, PUSHBUTTON, 24-POSITION, X-Y	EA
00001.000	2265839-0001		EA
REF	2265917-9901	DIAG, LOGIC, 781 RECEIVE ONLY KEYBOARD	EA
Į	QUANTITY. JMBER REV DESCRIPTI 781 RECE1 QUANTITY. COMPONENT 00001.000 2265916-0001 00002.000 0972519-0023 00004.000 0539480-0003 00004.000 0972350-0067 00004.000 0972946-0049 00001.000 2211263-0001 00001.000 2265839-0001	DESCRIPTION	



PART NU 2265951	JMBER REV		ON	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0002	00001-000	0986355-0002	SWITCH, OPTICAL	E
	v.		SEE TI- DRAWING	
0002A			\$1	
			SEE TI- DRAWING	
0002B			PN 986355-1 IS ALT PART	
			SEE TI- DRAWING	
0003	00001.000	2265923-0001		E
	20000 000		1238-5923-012	
0005	00002.000	2211404-0004	The second secon	E
00054			SEE TI- DRAWING	
0005A			R3 R4	
0006	REF	2245024 0001	SEE TI- DRAWING	_
0000	KEF	2265924-9901	SCHEMATIC, SENSOR	E
0007	00001.000	2265951-5001	AUTO INSERTED PARTS LIST FOR 2265951-1	F
	333311000	2207731 7001	1238-5151-015	-



NOTES: UNLESS OTHERWISE SPECIFIED:

1 DIMENSIONS ARE IN MILLIMETRES

2 GENERAL TOLERANCE:

ONE PLACE \pm 0.5 TWO PLACE \pm 0.25

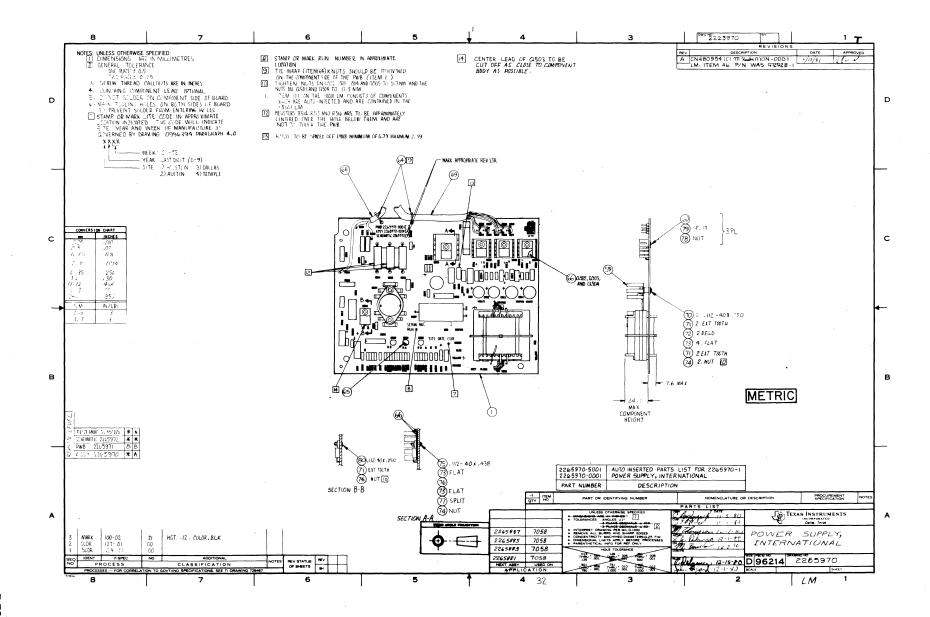
3. PROGRAM ITEM 1 USING ITEM 2.

4. MARK DEVICE WITH AT LEAST THE LAST 4 DIGITS OF BASE P/N AND THE FULL DASH #. INDELIBLE INK SHOULD BE USED, COLOR OPTIONAL.

PART NUMBER	DESCRIPTION
2265952-0026	781 R.O. STD EPROM #26
2265952-0027	781 R.O. STD EPROM #27
2265952-0028	781 R.O. STD EPROM #28
2265952-0029	780 SERIES KSR KATAKANA EPROM #29

TEXAS INSTRUMENTS INCORPORATED DIGITAL SYSTEMS DIVISION	Α	2265952	RE'
HOUSTON, TEXAS		SHEET 2	

-LIST OF MATERIALS-FEBRUARY 03, 1981 PART NUMBER 2265952-0001 REVITEM. QUANTITY. IC,TMS2532JL,BLANK EPROM G01295-TMS2532JL DDDO,78X DATA TRM F/W DISKETTE 1000 00001.000 2210020-0002 EΑ 0002 REF 2275200-1601 ΕA ASCCO UNRELEASED SOFTWARE 1261- REF-000



1/28/9	11	LIS	T OF MATERIALS	
PART NO 2265970	IMBER REV		ONPPLY, INTERNATIONAL	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0002	00002.000	0972667~0001	NETWORK +SN72723N	. د
00024			U500 U501	
דרפה	000.1000	0972499-0001	NETWORK, LM320T %.0/MC7905CP5 VOLT SEE - TI ORAWING	£t.
0003A			U502	
0004	00001.000	0972499-0002	SEE - TI DRAWING NETWORK, VOLG REG, NEG, 3 TERM-(-12V)	FA
. 0004A			U503	i
0005	00001.000	0972872-0012	NETWORK: LM 340-12T VOLTAGE REGULATOR NSC - LM340-12T	EA;
- 0005A			U504 NSC - LM340-12T	
0006 0006A	00001.000	0800523-0001	TRANSISTOR A5T2907 PNP SILICON TIA5T2907	EA
			Q500 TIA5T2907	
0007 0007A	00001*000	0972957-0001	TRANSISTOR, 2N930A NPN LOW CUR AMP, TO-18 MOT - 2N930A Q501	EA
0008	00001 000	0972057-0001	MOT - 2N937A	•
0008A	**************************************	0472057-0001	TRANSISTOR-A5T2222 NPN SILICON 1640-2132-000 Q502	:
0009	00001.000	0972455-0003	1640-2132-000 THYRISTORS,TRIODE-P-N-P-N SIL	
0009A			TE -TIC106D Q503	
0010	00001.000	0996703-0002	TI -TIC106D TRANSISTOR,NPN,125WATT.SJ9094-2 SEE TI- DRAWING	- A
0010A			Q504 SEE TI- DRAWING	
9031 9011A	00001.000	0996711-0002	TPANSISTOR, TIP734 N-P-N POWER 001295-TIP734	EA
			Q505 Q01295-TIP73A	
9021 9021A	00001.000	0972978-0065	RESISTOR, FIX., 33 OHMS, 1W, 5% TOL. SEE TI- DRAWING R500	EA
ຸດຄວນ	00001.000	0972942-0193	SEE TI- DRAWING RES.FXD.40K OHMS, 5%, 5W, WIREWOUGO	" 4 ->
00 2A	- 		SEE TI- DRAWING R513	M 1
10023	00001.000	0972942-0047	SEE TI- DRAWING PES FIX 22K OHMS 5 WATT 10% DAE - CW OR RS SERI	E,
1073A			R514 DAE - CW OR PS SERI	
702-5	00002.000	0972942-0022	RESISTOR, FIX., 1.20K, 5W, 5% TOL. SEE TI- DRAWING	Ej
30246			R515 R516 SEE TI- DRAWING	
25	<u> </u>	1972978-0169	PES FIX COMP 47 OHMS 1.0W 5° SEE - TI DRAWING R519	E ·
10.26	9001.030	0972978-0107	SEE — TI DRAWING RES,FXD,CMPSN,1W, 5%, 1.8 K OHMS	e V
اگو آنو از ا		-	039008-SEE TI DWG R521 039008-SEE TI DWG	

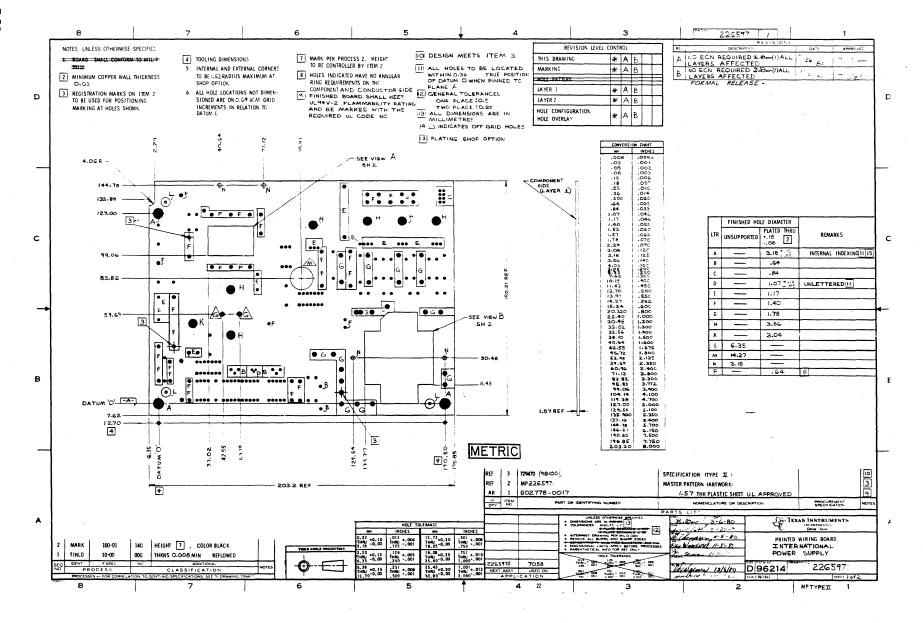
		LIST	OF MATERIALS-	
`& :/ 2× /81	l		•	
PART NUM 2265970-			ONPLY, INTERNATIONAL	
ETEM.	QUANTITY.	COMPONENT	DESCRIPTION	м
41	02001.020	0972630-0034	RES FIXED 0.221 OHMS 1WATT 17 001686-T-1A-70	ĒΑ
97414			R520 001686-T-1A-70	
3043	00001.000	0972924-0020	CAP FIX TANT SOLID 47 MFD 10 % 35 VOLT QPL	ΕA
1043A			C501 OPL -M39003/1-2312	
)] 4 4 A	90001.000	0996326-0006	CAPACITOR 1700UF 10 OCWV FLECTROLYTIC 001939-6730233 C507	FA
			001939-6730233	
945 9454	00003.000	0412645-0015	CAPACITOR, 1 UF +80, -20% 500VDC CEP DIFL 1222-3866-000 C508;516 C517	EA
			1222-3866-000	
2046 3046 A	00001.000	0972928-0011	CAP FIX MICA 500V 3000 PF 5 %	EA
·			039001-CMR06F302JOD	
)047 0047A	00002.000	2211319-0015	CAP 100 UF 35 V ALUM, ELECT, HIGH FREQUE SEE TI- DRAWING C511 C512	EA
7048	00002.000	2211319-0016	SEE TI- DRAWING CAP. 220UF, 25V, ALUM ELECT, HIGH EREQUEN.	EA
3 648A			SEE TI- DRAWING C513 C514	
ρ 49	00001.000	2210420-0005	SEE TI- DRAWING CAP, PLASTIC, METALLIZED, 20%, 4700 PF, 20MMZ 012624-SEE TI DWG	EA
0049A			C515	
958	00001.000	0996151-0009	012624-SEE TI DWG HEADER,PIN,4 PINS, STR. DOUBLE ROW 022526-65611-108	FA
9058A			J600	
0059	00001.000	0533599-0014	022526-65611-108 HEAT SINK,.75HT 1.29W 1.63LG FLEC CMPNT 098978-LAT03B3CB	EA
3060	00003.000	0996285-0005	HEATS INK, TRANSISTOR	FA
7061	00001.000	0996285-0002	SEE T -I DRAWING HEATSINK, TRANSISTOR	FA
7062	00001.000	2265998-0101	013103-6106B-14 Transformer,Switching,Intn•L Power Sup	EA .
″∂332 A			Т500	
, ,6 3	00001.000	0972217-3000	FUSE, 3AG SB 250V RADIAL LEAD	EV
7634			F500	
≥964	00004.000	0972632-0001	STRAP, TIE DOWN, CABLE-NON-STD, 0-1-1/4 D.	FA
0065	00001.000	0185113-0001	X SPACER XST TO-18 CASE	EA
9066	00005.000	0996521-0010	INSULATOR, .147DIA .750LG .500W	FA
- 0067	00001.000	0996521-0002	055285-7403-09FR-54 INSULATOR,.009# THK THERMALLY CONDUCTIVE 055285-7403-09FR-03	EA
9068	00001.000	2266000-0001	CABLE ASSY, UNREGULATED D.C. 1238-6000-016	EA
9.9	20001.000	2266001-0001	CABLE ASSY, SECONDARY D.C.	EA
370	00002-000	0972988-0019	1238-6001-016 SCREW 4-40 X .750 PAN HEAD CRES	EA

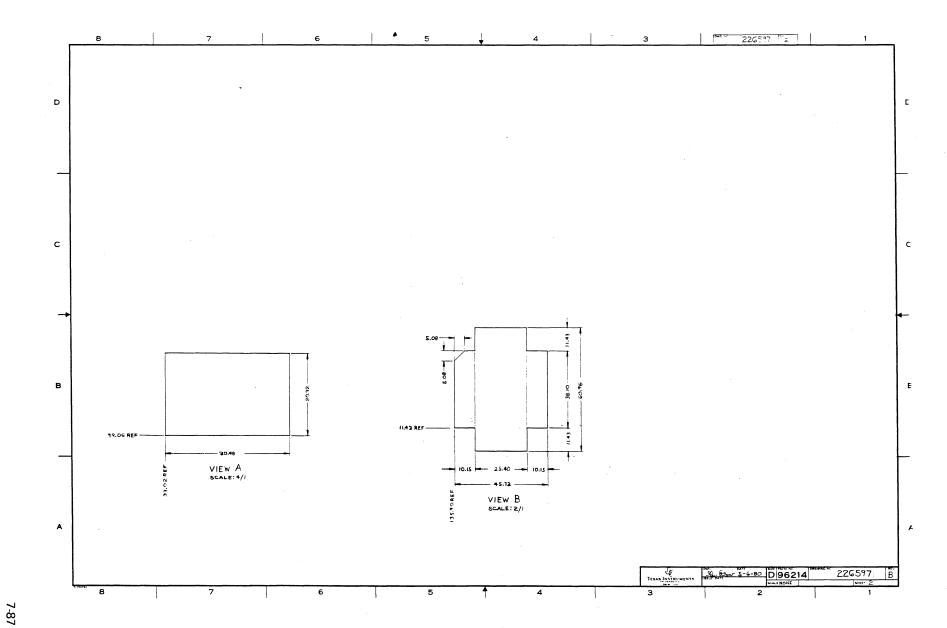
13/28/8	31			
PART NU 2265970	JMBER REV D-0001 A		ONPLY, INTERNATIONAL	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0071	00005.000	0411101-0057	LOCKWASHER # 4 EXTERNAL TOOTH CRES	EA
1772	00012-010	0416925-0400	SPACER,#4 1/8"LG ALUM ANDDIZED -NAS43DDO-8	EA
0073	00006.000	0416622-0011	WASHER #4 FLAT QPL — AN960C4L	EA
7074	00004.000	0416453-0021	NUT,PLAIN,4-40 UNC-2B HEX,CRES,SMALL QPL - NAS671-C4	E۵
0075	00001.000	0972988-0016	SCREW 4-40 X .438 PAN HEAD CRES	EA
0076	00001.000	0972628-0001	WASHER,#4 .115ID .200ND-SHLDR NON-MET SEA -5607-45	FA
2077	00001.000	0411104-0135	WASHER, LOCK-SPRING, HELICAL, #4 OPL - MS35338-135	FA
0078	00003.000	0416453-0022	NUT, PLAIN 6-32 UNC-2B HEX CRES, SMALL QPL - NAS671C6	EA
0079	00003.000	0411104-0136	WASHER, LOCK-SPRING, HELICAL, #6 QPL - MS35338-136	EΑ
1080	00001.000	0972355-0001	STUD SELF-CLINCHING-PWR 046384-KFH-440-4	EA,
0100	REF	2265973-9901	TEST PROCEDURE, POWER SUPPLY, INTN'L	
0101	00001.000	2265970-5001	AUTO INSERTED PARTS LIST FOR 2265970-1 1238-7051-016	EA
9999	00000.450	0239999-9999	COST, SHRINKAGE	EA

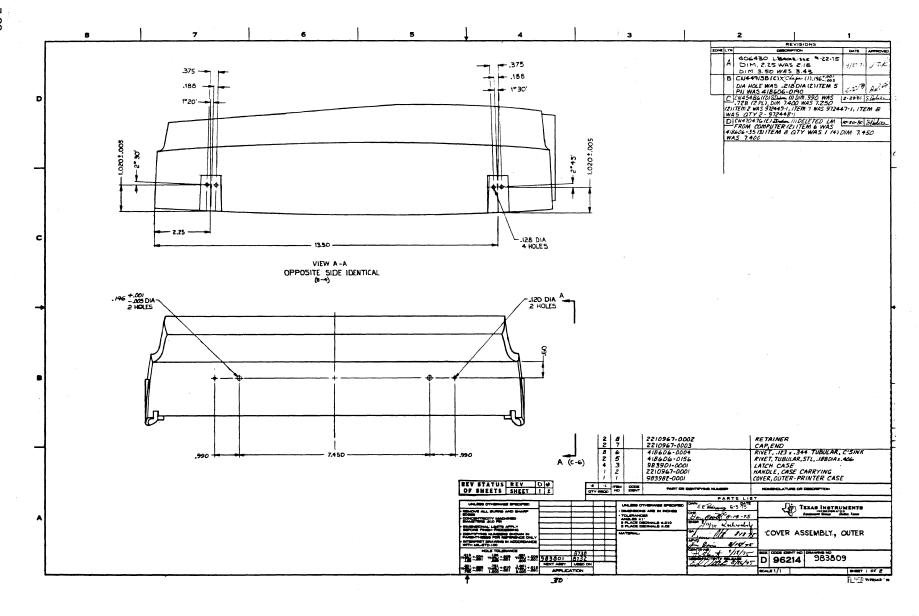
03/28/8	· · · · · · · · · · · · · · · · · · ·	LIST	TOF MATERIALS	
1		055501011		
PART NI 226 5 970			RTED PARTS LIST FOR 2265970-1	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0001	000.10000	2265971-0001	PWB, INTN°L POWER SUPPLY, 780 SERIES	EA
0012	00002.000	0539468-0007	DIODE, 194007 JAMP 1000PIV RECTIFIER	EA
0012A			TI -1N4007 CR500 CR512	
0013	00003.000	0539468-0003	TI -1N4007 DIODE,1N4003 LAMP 200PIV RECTIFIER	EA
0013A		•	TI - IN4003 CR501 CR509 CR510	
2014	00001.000	0972934-0001	TI - IN4003 DIODE,1N746A 3.3 V 5% SIL VOLT REG	EA
0014A		·	QPL - 1N746A CR502 IN746A	
0015	00005.000	0972932-0001	QPL - 1N746A DIODE 1N914B	EA
0015A			SEE TI- DRAWING CR503 CR504 CR506 CR507	
00158			SEE TI- DRAWING CR508	
0016	00001.000	. 0972454-0010	SEE TI- DRAWING DIODE, VOLTAGE-REGULATOR-SILICON, IN726A	EA
0016A			001295-IN726A CR505	
0017	00001.000	0972268-0006	001295-IN726A DIODE IN4937 1 AMP	EA
0017A			SEE - TI DRAWING CR511	Ln
0018	00001.000	0996281-0005	SEE - TI DRAWING RECTIFIER,SILICON,FAST RECOVERY	EA
00184		0770201 0005	014099-SS3891 CR513	CA
0019	00001.000	0996281-0006	014099-553891	
0019A	00001.000	0990281-0008	RECTIFIER, \$53892/UE\$1302, V(R)100V I(0)6A 014099-\$53892	EA.
	00000 000		CR514 014099-SS3892	
0020	00002.000	0996281-0001	DIODE UES 1101 014099-UES 1101	EA
00204			CR515 CR516 014099-UES 1101	
9027	00001.000	0972946-0085	RES FIX 6.8K OHM 5 % .25 W CARBON FILM ROH - R-25	EA
0027A			R501 ROH - R-25	
0028	00001.000	0972946-0041	RES FIX 100 OHM 5 % .25 W CARBON FILM ROH - R-25	EA
0028A			R502 ROH - R-25	
0029	00001.000	0539370-0529	RES FIX FILM 31.6K OHM 1% .25 WATT COR - NA55	EA
00294			R503 COR - NA55	
0030	00001.000	0539370-0481	RES FIX FILM 10.0K OHM 1% .25 WATT COR -NA55D-100PPM/C	EA
0030A			R504 COR -NA55D-100PPM/C	
0031	00001.000	0972946-0096	RES FIX 20 K OHM 5 % .25 W CARBON FILM	EA
0031A			ROH - R-25 R505	
0032	00001.000	0972946-0077	ROH - R-25 RES FIX 3.3K OHM 5 % .25 W CARBON FILM	EA
0032A			ROH - R-25 R506	
			ROH - R-25	

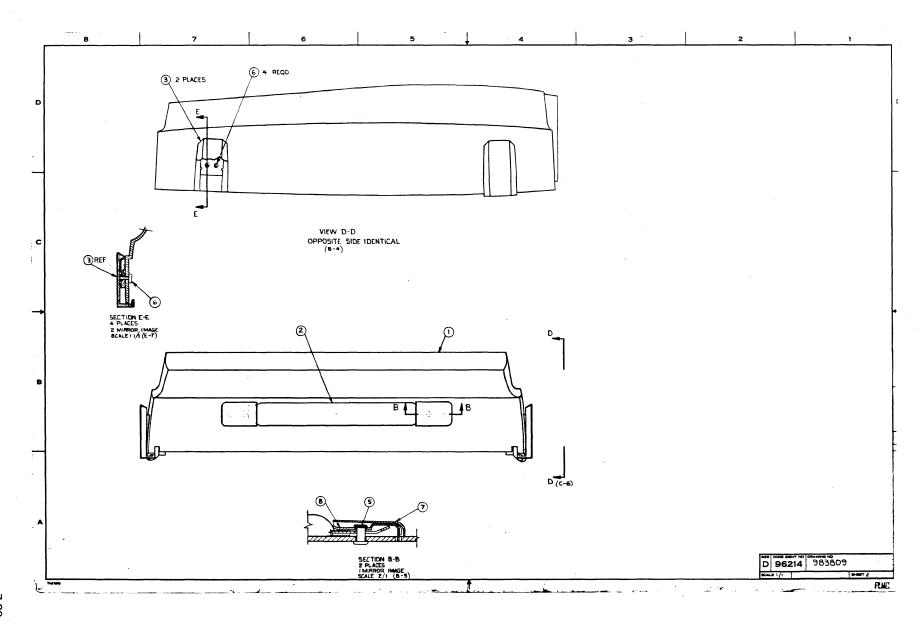
03/28/8				
	JMBER REV 3-5001 A		RTED PARTS LIST FOR 2265970-1	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	JM
0033	00001.000	0972946-0053	RES FIX 330 OHM 5 % .25 W CARBON FILM ROH - R-25	ΕA
0033A			R 50 7	
0034	00001.000	0972946-0074		EA
0034A			ROH - R-25 R508	
0035	00001.000	0972946-0080	ROH - R-25 RES FIX 4.3K OHM 5 % .25 W CARBON FILM	EΑ
0035A			ROH - R-25 R509	
0036	00001.000	0972946-0003	ROH - R-25 RES FIX 2.7 OHM 5 % .25 W.CARBON FILM	EA
0036A			ROH - R-25 R510	
0037	00001.000	0972630-0077	ROH - R-25 RESISTOR,0.619 OHMS 1W,5% FX WW	EΑ
0037A			001686-T-1A-70 R511	
0038	00001.000	0972947-0123	001686-T-1A-70 RES FIX 270K DHM 5% .5 W CARBON FILM	EA
0038A			ROH - R-50 R512	
0039	00001.000	0539812-0032	ROH - R-50 RES FIX FILM 10.5K OHM .1% .125 WATT	EA
0039A			COR - NC4-50PPM/C R517	LH
0040	00001.000	0539812-0001	COR - NC4-50PPM/C RES FIX FILM 4-12K OHM .1% .125 WATT	EA
0040A			COR - NC4-50PPM/C R518	t. M
0042	00.002 - 000	0972947-0057	COR - NC4-50PPM/C RES FIX 470 OHM 5% .5 W CARBON FILM	EA
0042A	The street of the state	Water the Mark	ROH — R-50 R522 R523	EA
0050	00001.000	0418356-2350	ROH - R-50 CAP-FXD 0.47UF.50V.10% TANTALUM SOLI	
0050A	VIVIE # 01/0	0410330-2330	QPL -M39003/1-2350	EA
0050A 0051	00002 000	0672024-0017	C500 QPL -M39003/1-2350 CAD ELY TANK 504.5 10 MED 10 M 25 MOLT	- .
0051A	00002.000	0972924-0017	CAP FIX TANT SOLID 1.0 MFD 10 % 35 VOLT SPR -150D105X9035A	EΑ
	00001 000	0072757 000	C505 C518 SPR -150D105X9035A	
0052	00001.000	0972757-0001	CAP, FIXED CERAMIC 100 PF 10% 50V UC — C51C101K	EA
0052A	00007 725		C502 UC -C51C101K	
0053	00007.000	0972757-0037	CAP FIX CER 0.1MF 10% 50V	EA
0053A			C503 C510 C520 THRU C522	
00538			C524 C525	
0054	00001.000	0972757-0021	CAPACITOR FXD 330PF 50 VOLTS 10% CERAMIC	EA
0054A			C504	
0055	00001.000	0972757-0025	CAP FIX CER .OIMF 10% 50V	EA
0055A			C 50 6	
0056	00001.000	0418356-2344	CAP FIX 0.22 MF 50V 10% TANTALUM SOLID SEE TI- DRAWING	EA

03/28/8	1	L131	OF MATERIALS————————————————————————————————————
PART NIJ 2265970			ON RTED PARTS LIST FOR 2265970-1
ITEM.	QUANT ITY.	COMPONENT	DESCRIPTIONUM
0056A			C 523 SEF TI - DRAWING
0 05 7	00001.000	0972924-0014	CAP FIX TANT SOLID 15 MFD 10 % 20 VOLT EA
0057A			OPL -M39003/1-2289 C519

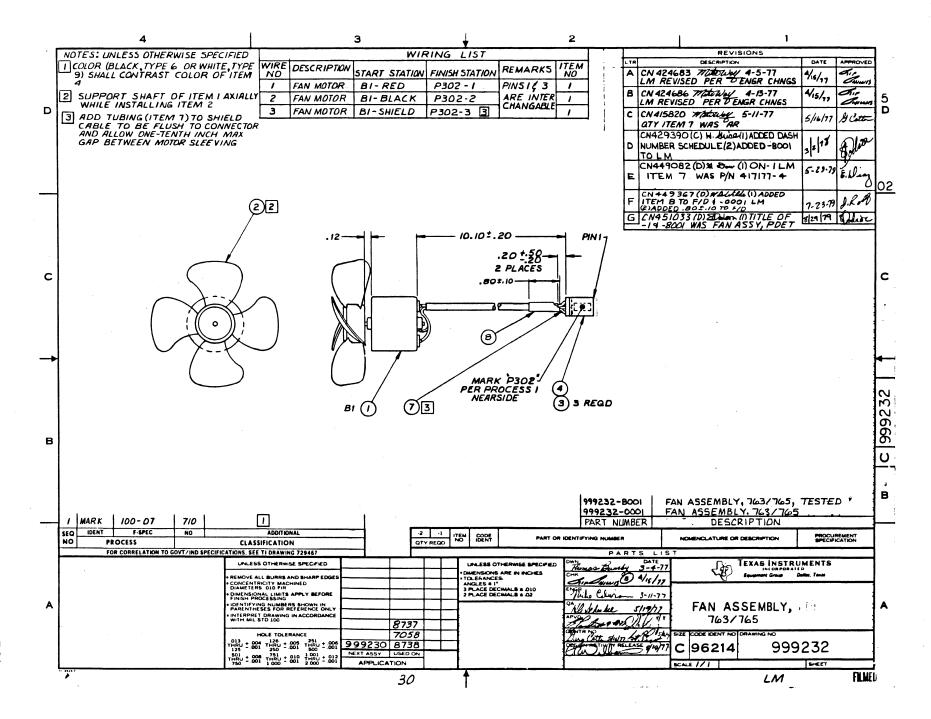




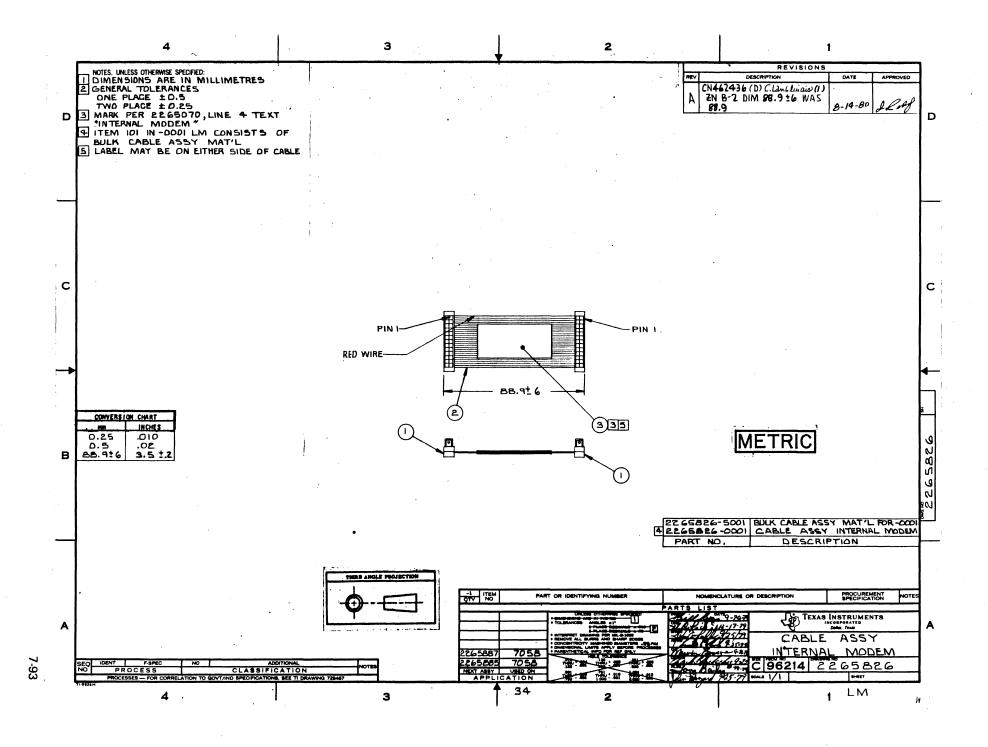




DART MI	MDCD DEV	PART NUMBER REV DESCRIPTION					
0983809		OUTER COV					
		557211 551					
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	M			
0001	00002.370	0996659-0002	MOLDING, RESIN, THERMOPLSTC NORYL LT GRA	LB			
0003	00004.000	0983901-0001	LATCH CASE	EA			
0004	00008.000	0418606-0004	RIVET123 X .344 TUBULAR.C-SINK -MS16536-4	EA			
0005	00002.000	0418606-0156	RIVET,TUBULAR,STL.188DIAX.406,MS16536-46 -SEE DRAWING	EA			
0006	00001.000	2210967-0002	HANDLE, CASE CARRYING	EA			
0007	00002.000	2210967-0003	HANDLE, CASE CARRYING	EA			
0009	00000-200	0936800-0425	CORRUGATED BOX,20718 X 163/8 X 16 SEE TI- DRAWING	EA			
0010	00000-800	0936806-0002	PAD-FLAT CORRUGATED	EA			

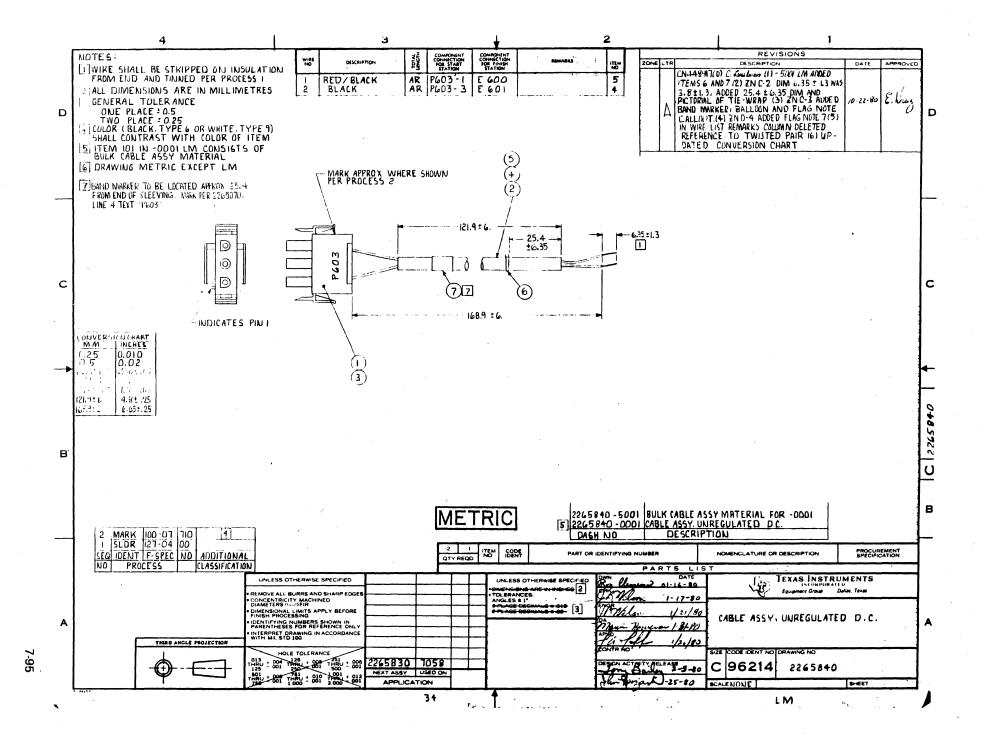


PART NU 0999232			ON	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	JM
0001	00001.000	0972486-0003	MOTOR, FAN 12V DC	1
0001A			022227-CK35-T6C B1	
OUUIA			022227-CK35-T6C	
0002	00001.000	0996515-0001	FAN BLADE,3-IN X.078 DIA HUB BORE	1
0003	00003.000	0972104-0001	CONTACT ELEC-LOCKING, WIRE-TO.025 SQ POST AMP - 87124-1	1
0004	00001.000	0972484-0003	CONNECTOR HOUSING 3 CONTACT	1
0004A			T18 -7175-8 P302	
0004B			TIB -7175-8 ITEMS 3 AND 4 CAN ONLY BE	
			TI8 -7175-8	
0004C		*	USED TOGETHER	
			T18 -7175-8	
0005	00000.000	0972482-0006	CONTACT, ELECTRICAL, CRIMP	1
0001			BEI - 75691-006	
0006	00000.000	0772707-0034	RECEPTACLE, TERMINAL - 3 CAVITIES	1
0006A			BEI -65039-034	
UUUUA			ITEMS 5 AND 6 MAY BE USED BEI -65039-034	
00068			AS ALTERNATES TO ITEMS 3	
			BEI -65039-034	
0006C			AND 4 ITEMS 5 AND 6 MAY	
			BEI -65039-034	
0006D			ONLY BE USED TOGETHER	
			BEI -65039-034	
0007	00000.030	0972436-0009	INSUL SLEEVING,#14 .016THK .066ID	F
0000	00000 070	0070144 0051	003890-HT-105C-14	
8000	00000.070	0972146-0004	TUBING020THK X 1/8 HT SHRNKABLE .1251D 003890-P0135125C1/16*	ŧ



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PART NU 2265826			ONY; INTERNAL MODEM	•••••	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	•••••••	UM
0001	00002.000	0996261-0005	CONNECTOR, RECEPTACLE	26, POSITIONS	EA
0101	00001.000	2265826-5001	BULK CABLE ASSY MAT'L 1629-5826-000	FOR -0001	EA



OCTOBER 24, 1980

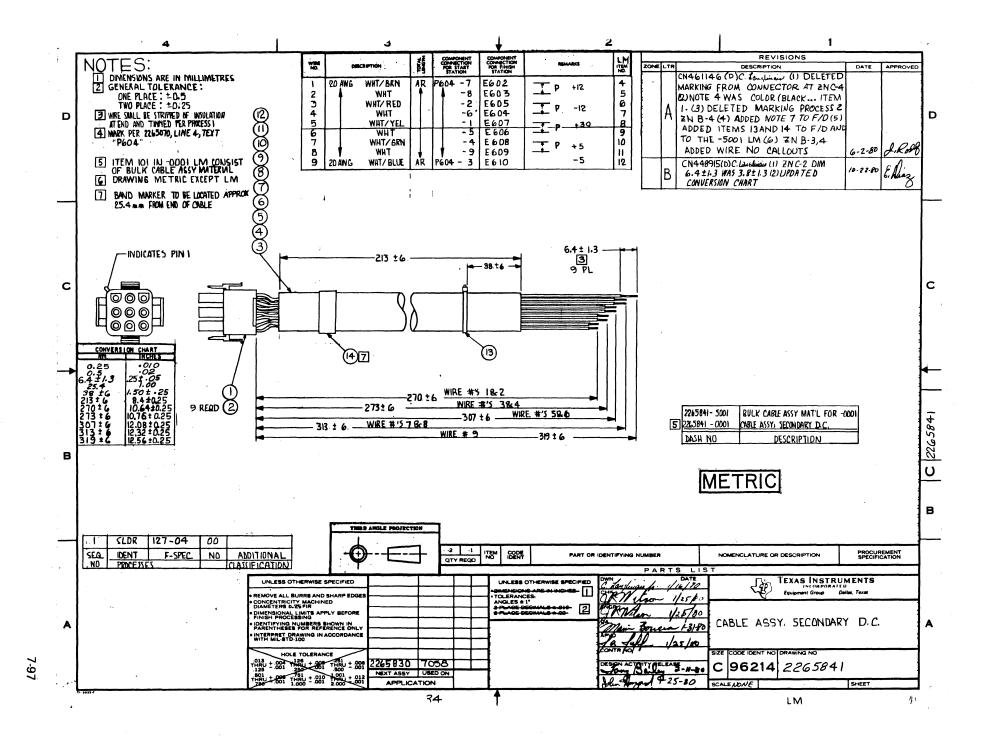
PART NUMBER 2265840-0001 DESCRIPTION.....CABLE ASSY, UNREGULATED D.C. REV A

ITEM. QUANTITY.

0001 00001.000 0972574-0006 HOUSING, CONN PLUG, LOCKING 3 CONTACTS EA

0001A P603

0101 BULK CABLE MATERIAL FOR 2265840-1 1629-5840-000 00001.000 2265840-5001 EΑ



OCTOBER 24, 1980

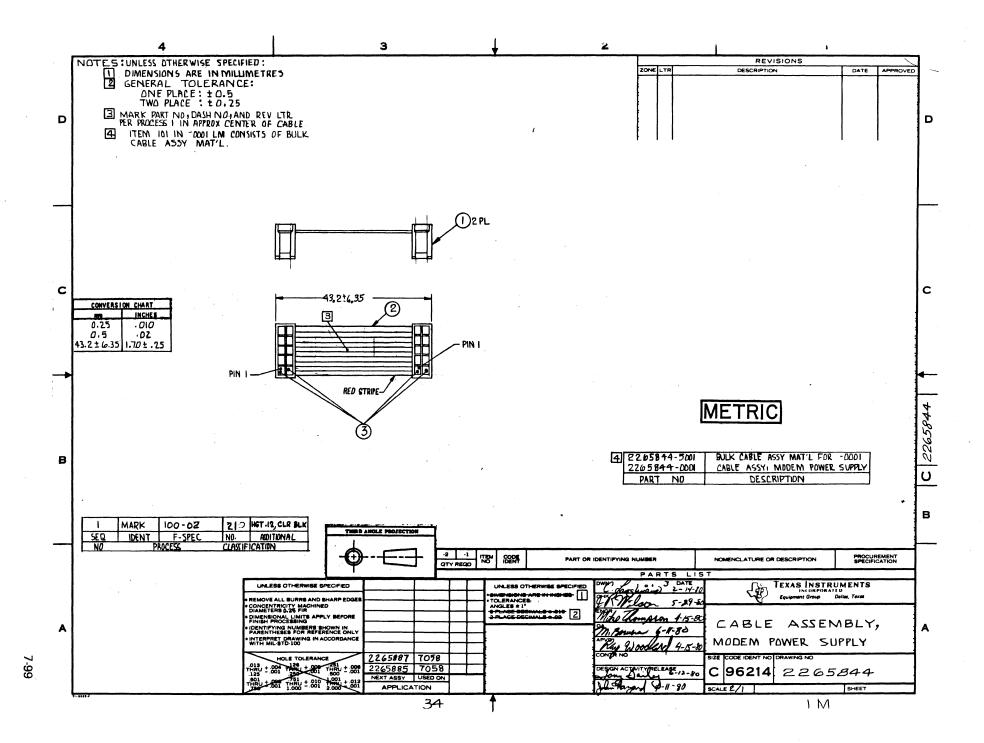
PART NUMBER R 2265841-0001 REV B DESCRIPTION.....CABLE ASSY, SECONDARY D.C.

ITEM. QUANTITY.

0001 00001.000 0972574-0002 HOUSING, CONNECTOR, PLUG, LOCKING EA

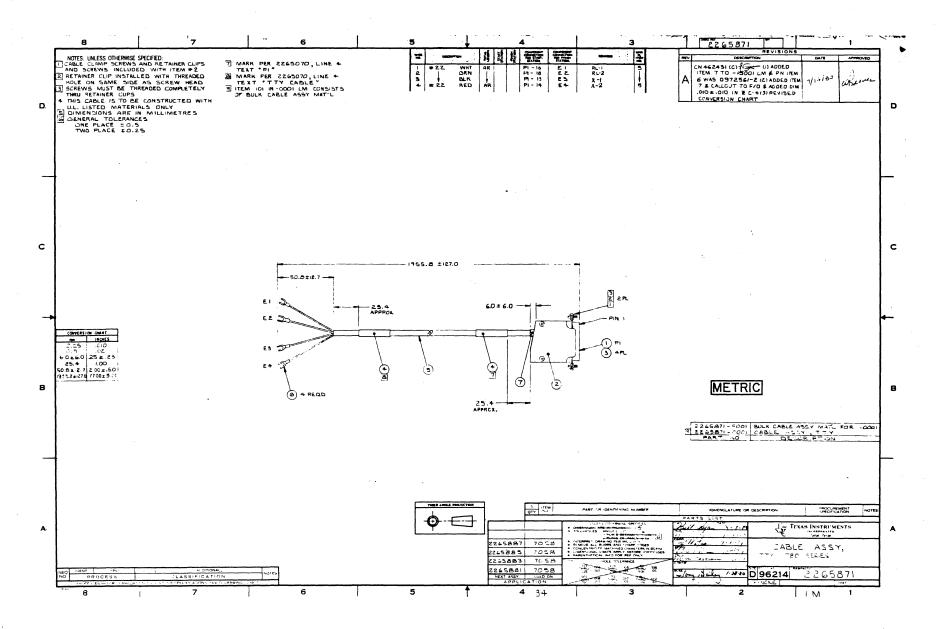
0001A P604

0101 00001.000 2265841-5001 BULK CABLE MATERIAL FOR 2265841-1 1629-5841-000 EA

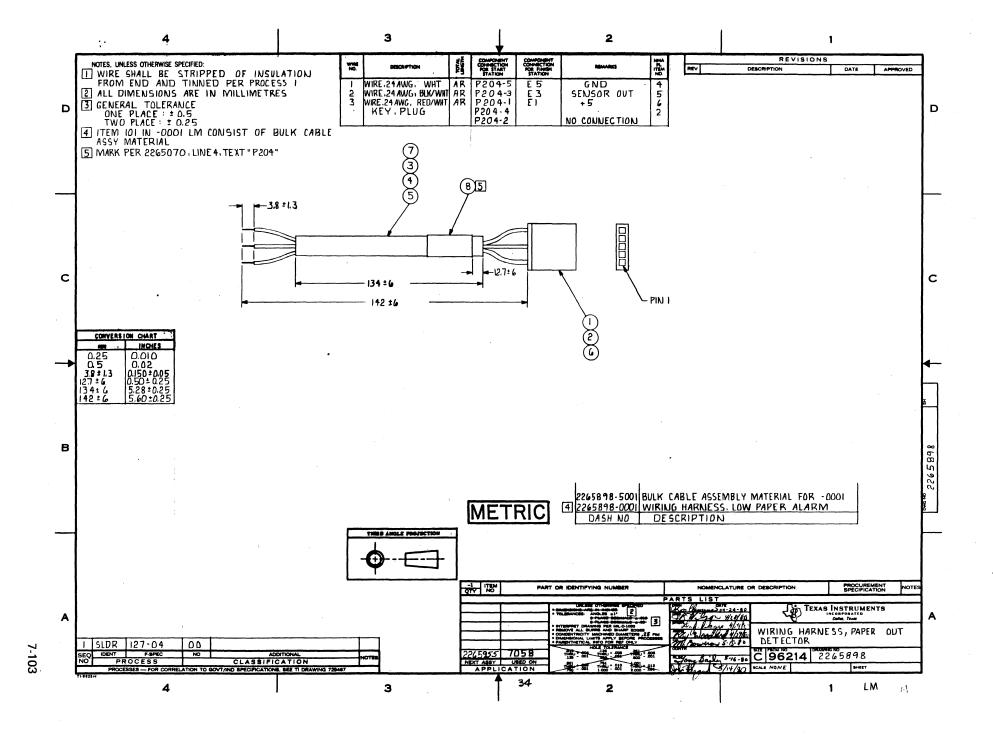


OCTOBER	24, 1980			
PART NU 2265844			ON Y, MODEM POWER SUPPLY	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	. UM
0001	00002.000	0996261-0001	CONNECTOR RECEPTACLE 10 POSITION 000779-88377-1	EA
0003	00004.000	0800335-0001	KEY,POLARIZATION,CONNECTOR BEI65307-001	EA
0101	00001.000	2265844-5001	BULK CABLE MATERIAL FOR 2265844-1 1238-0844-000	EA

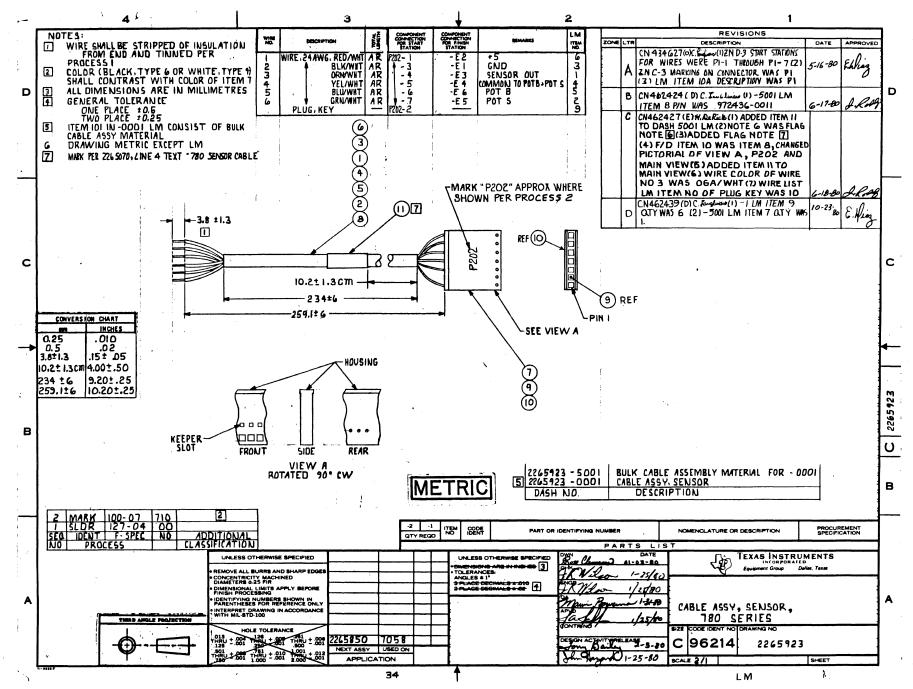




PART NU 2265871			ONY, 780 SERIES	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0001	00001.000	0539409-0006	CONNECTOR RCPT 25 PINS AMP -205207-1	E
0001A			P1 AMP -205207-1	
0002	00001-000	2210305-0003	HOOD STRN RLF 45/180DEG, BULK PK 25 POS 000779-2-206478-2	E
0101	00001-000	2265871-5001	BULK CABLE ASSY MATERIAL FOR -0001 1629-5871-000	E

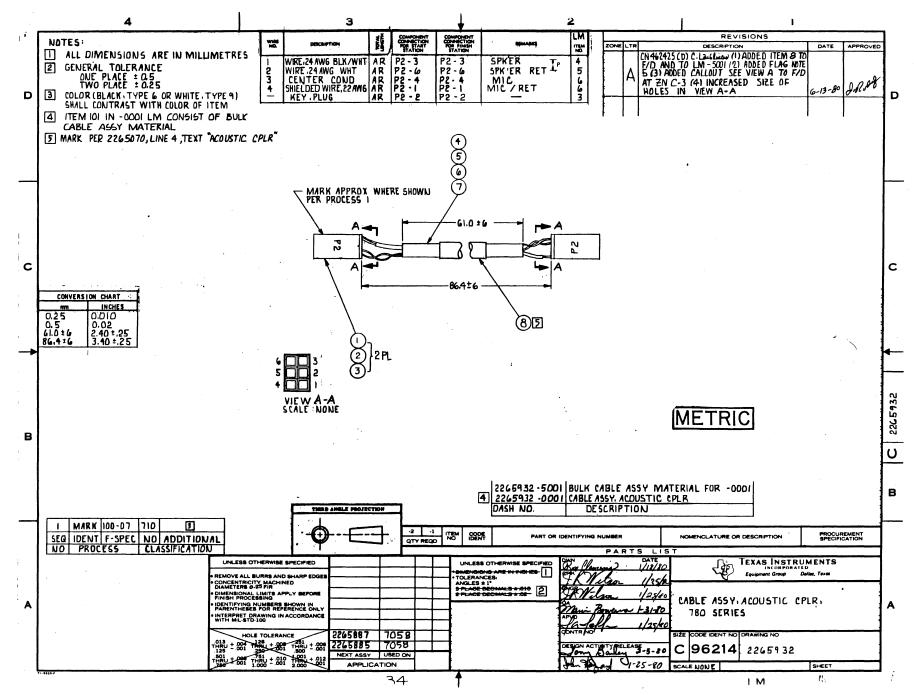


OCTOBER	24, 1980			
PART NUMBER REV 2265898-0001 *		DESCRIPTION		
ITEM.	QUANTITY.	COMPONENT	DESCRIPT ION	UM
0001	00001-000	0972484-0005	CONNECTOR HOUSING 5 CONTACT	EA
0001A			P204 TII87175-2	
0002	00001-000	0800335-0001	KEY,POLARIZATION,CONNECTOR BEI65307-001	EA
0101	00001.000	2265898-5001	BULK CABLE MATERIAL FOR 2265898-1 1650-0000-000	EA



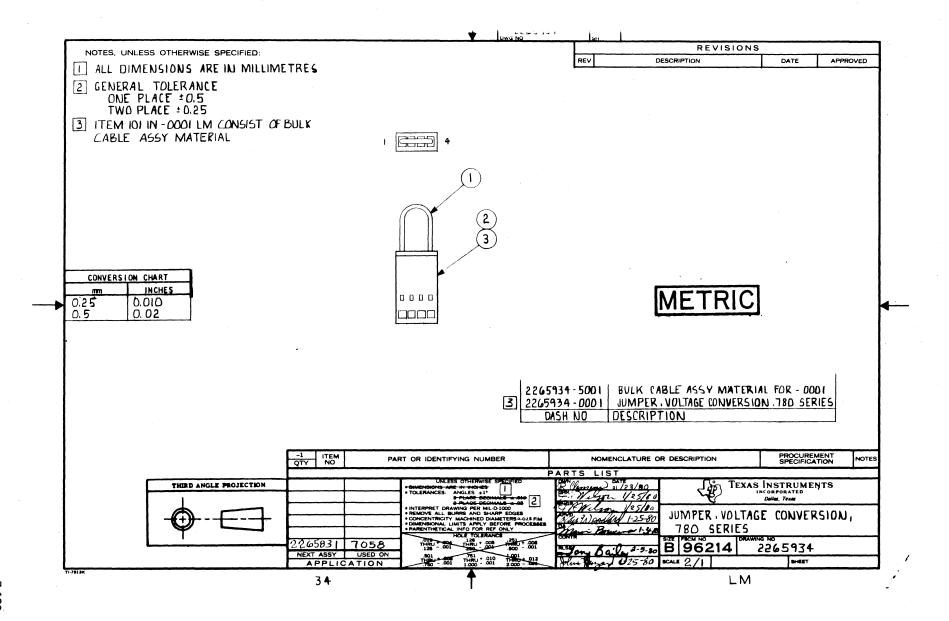
7-105

PART NU 2265923			ON Y, SENSOR 780 SERIES	
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0009	00001.000	0800335-0001	KEY, POLARIZATION, CONNECTOR BEI65307-001	E
0010	00001.000	0972484-0007	CONNECTOR HOUSING 7PINS 000779-1-87175-5	E
0010A		•	P202 000779-1-87175-5	
0101	00001-000	2265923-5001	BULK CABLE ASSY MATERIAL FOR 2265923-1 1238-0923-000	E



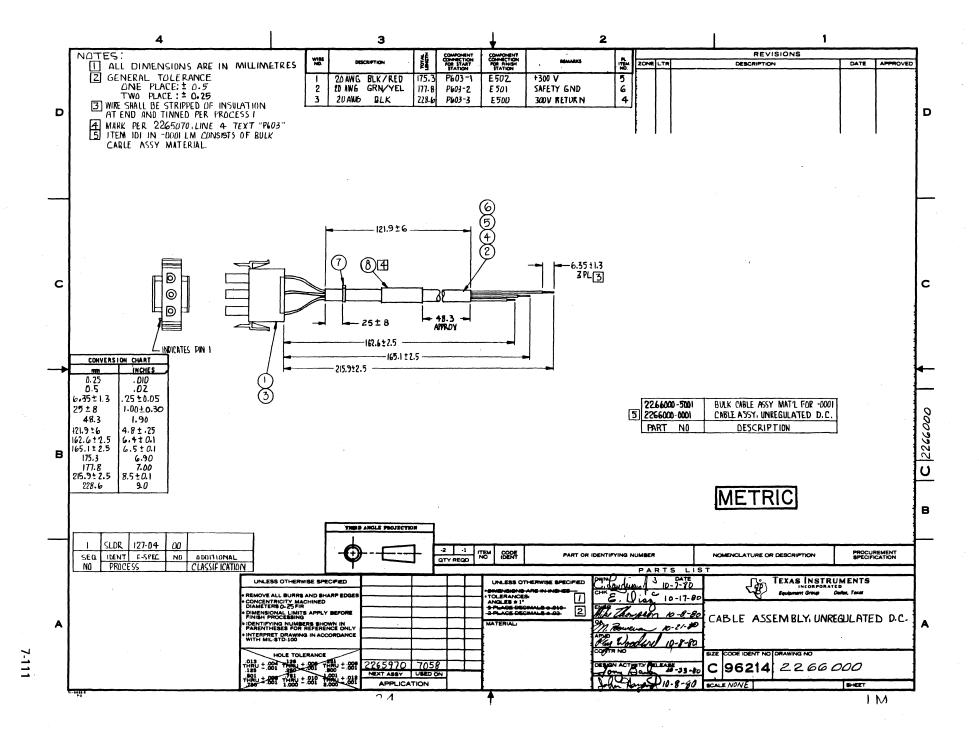
7-107

PART NUMBER REV 2265932-0001 A		DESCRIPTIONCABLE ASSY, ACOUSTIC CPLR, 780 SERIES				
2207752	. 0001	CHULL HJJ	THE MODUSTIC CPERT TOU SERIES			
ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM		
0001	00002.000	0996566-0003	HOUSING, CONNSELF-RET. CON., 6 POS. 871337	EA		
0001A			P2 P2 871337			
0003	00002.000	0800335-0001	KEY,POLARIZATION,CONNECTOR BEI65307-001	EA		
0101	00001-000	2265932-5001	BULK CABLE MATERIAL FOR 2265932-1 1629-5932-000	EA		

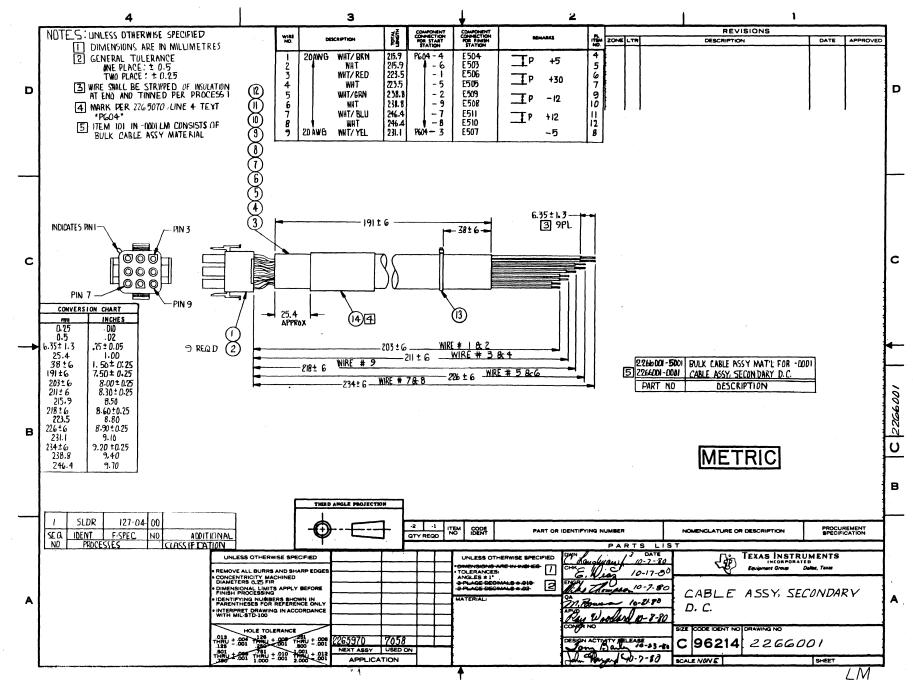


OCTOBER 24	. 1	9	80
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	JMBER REV 1-0001 +		ONOLTAGE CONVERSION, 780 SERIES	
ITEM.	QUANT ITY.	COMPONENT	DESCRIPTION	. UM
0003	00001.000	0972484-0004	CONNECTOR HOUSING 4 CONTACT	EA
0101	00001 - 000	2265934-5001	BULK CABLE MATERIAL FOR 2265934-1	EA



			IST OF MATERIALS	
FEBRUAR	Y 03, 1981			
PART NU 22 66 000			ON	
.ITEM.	QUANTITY.	COMPONENT	DESCRIPTION	UM
0061	00001.000	0972574-0006	HOUSING, CONN PLUG, LOCKING 3 CONTACTS	EA
0001A			P603	
0101	00001.300	2266000-5001	BULK CABLE MATERIAL FOR 2266000-1 1238-0000-009	EΑ



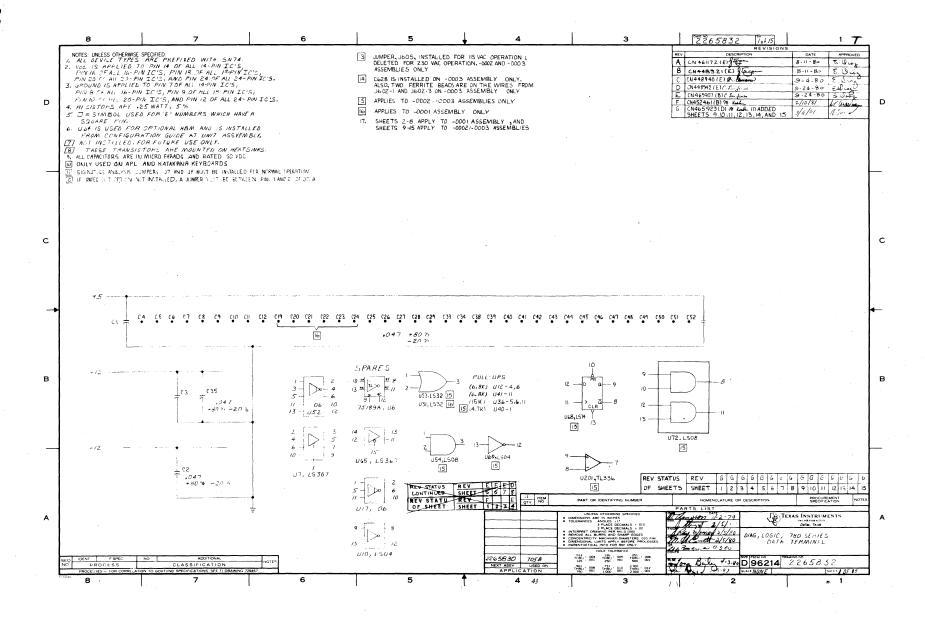
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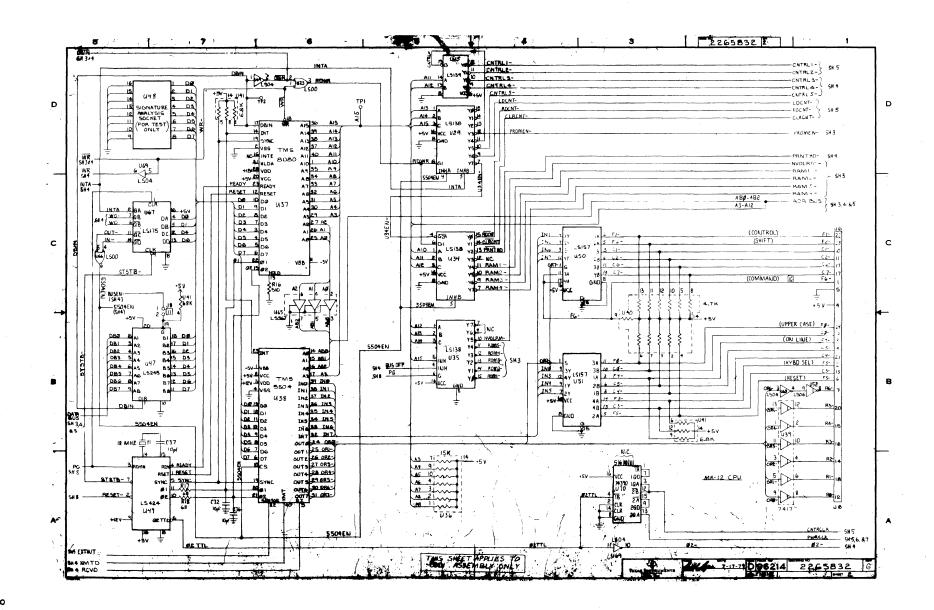
. FEBRUAI	RY 03, 1981			
PART NU 2266001			IGN SY, SECONDARY D.C.	
ITEM.	OUANTITY.	COMPONENT	DESCRIPTION	UM
0001	00001.000	0972574-0002	HOUSING, CONNECTOR, PLUG, LOCKING	EA
0001A			P604	
\$101	00001.000	2266001-5001	BULK CABLE MATERIAL FOR 2266001-1 1238-0001-009	EA

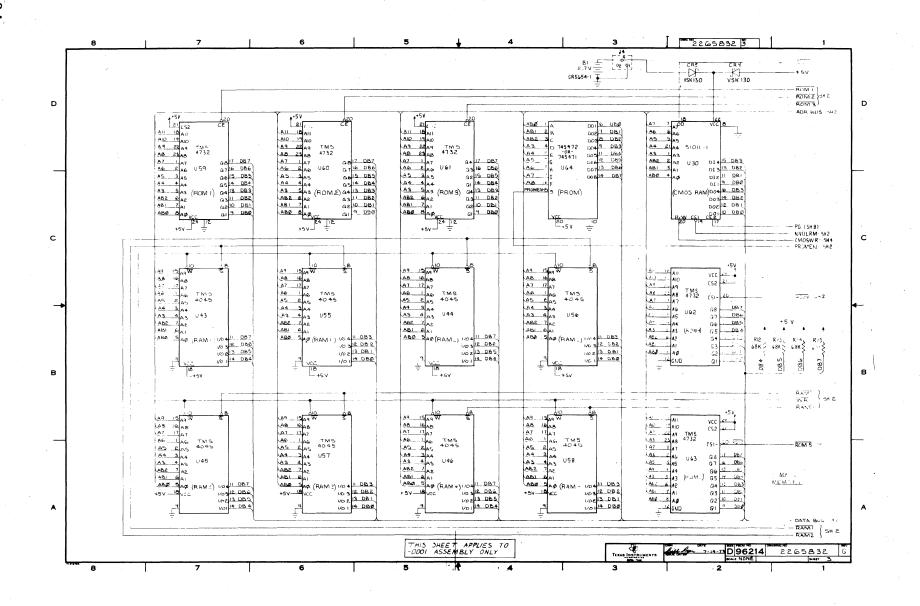
Section 8

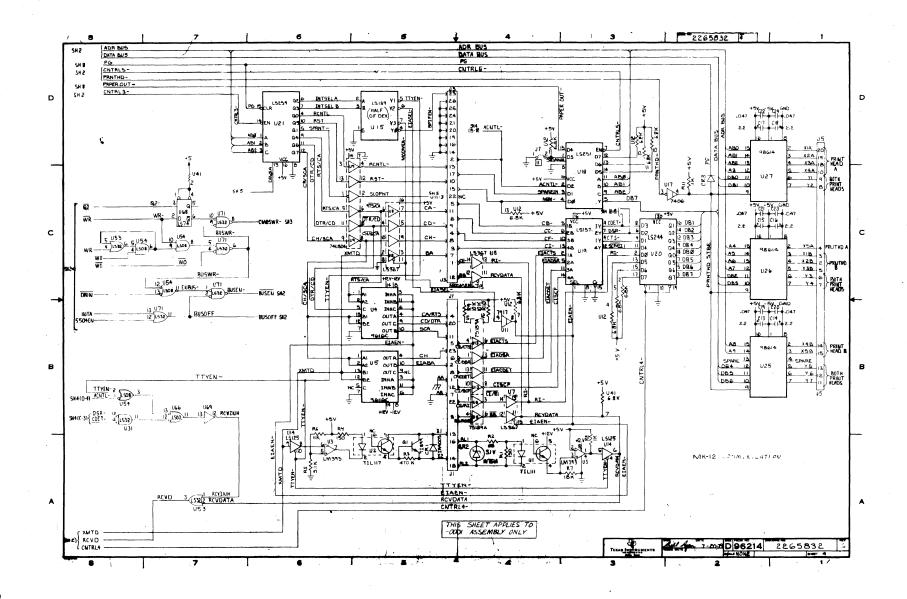
Schematics

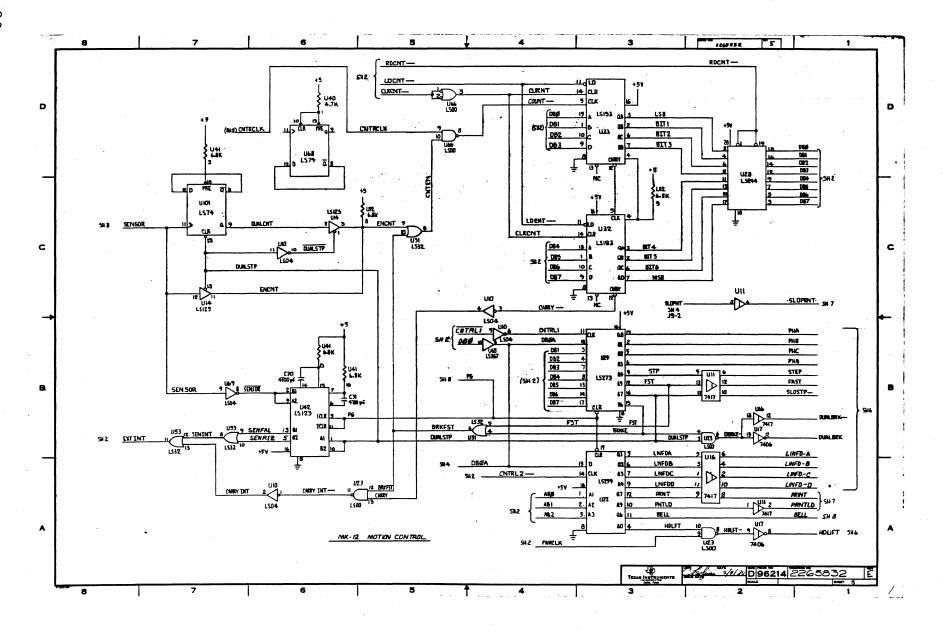
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Diagram, Logic, Power Supply	2265837	8-17
Diagram, Logic, Modem, 785	2265842	8-18
Diagram, Logic, 781 RO Keyboard	2265917	8-25
Diagram, Logic, Sensor	2265924	8-26
Diagram, Logic, Paper Out Detector	2265957	8-27
Diagram, International Power Supply	2265972	8-28

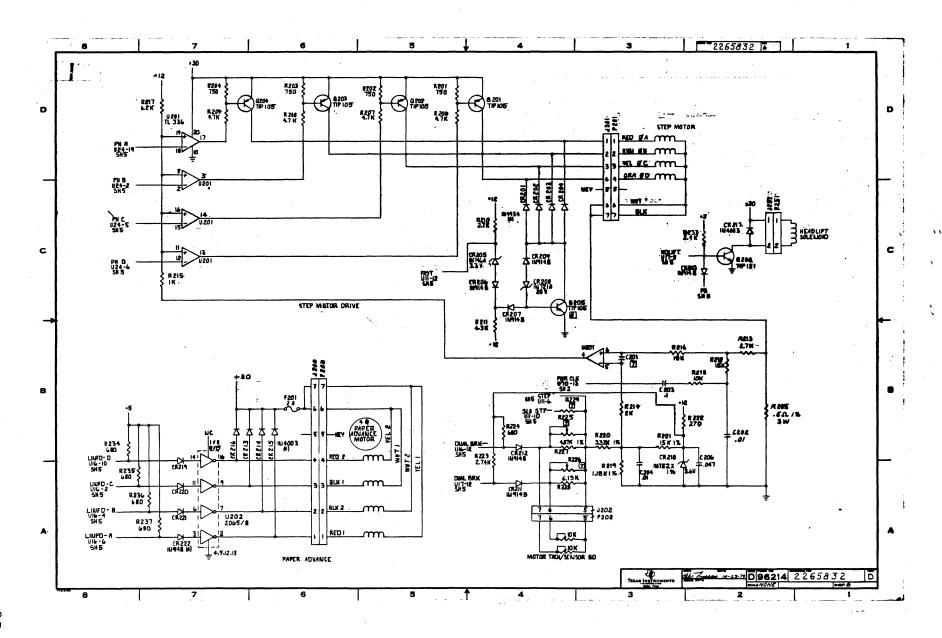


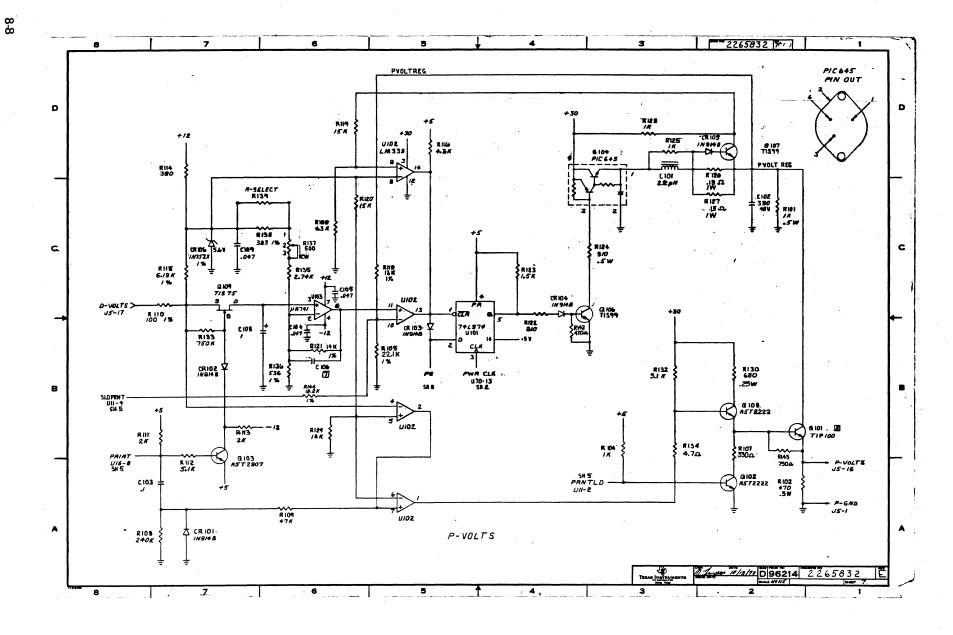


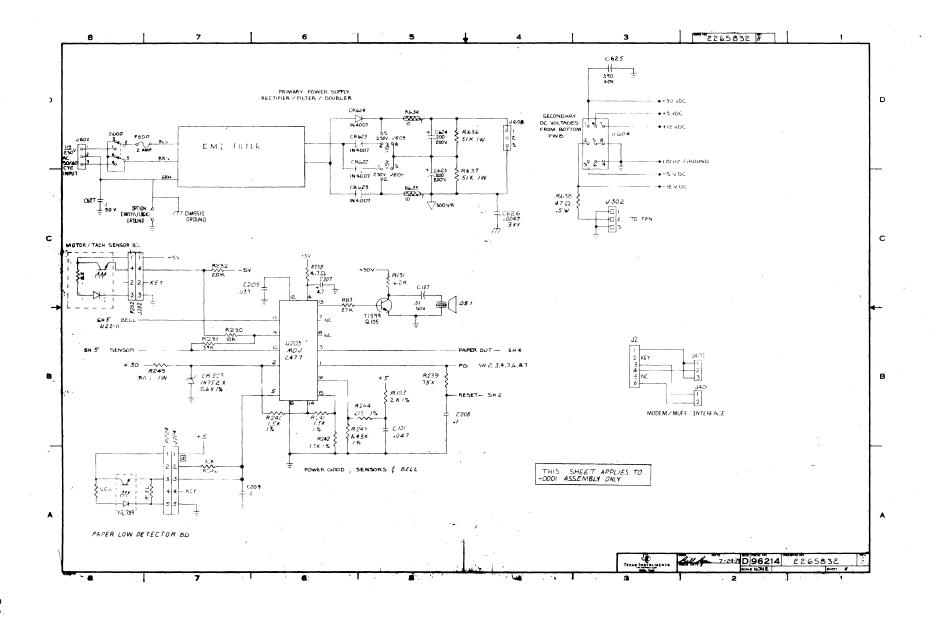


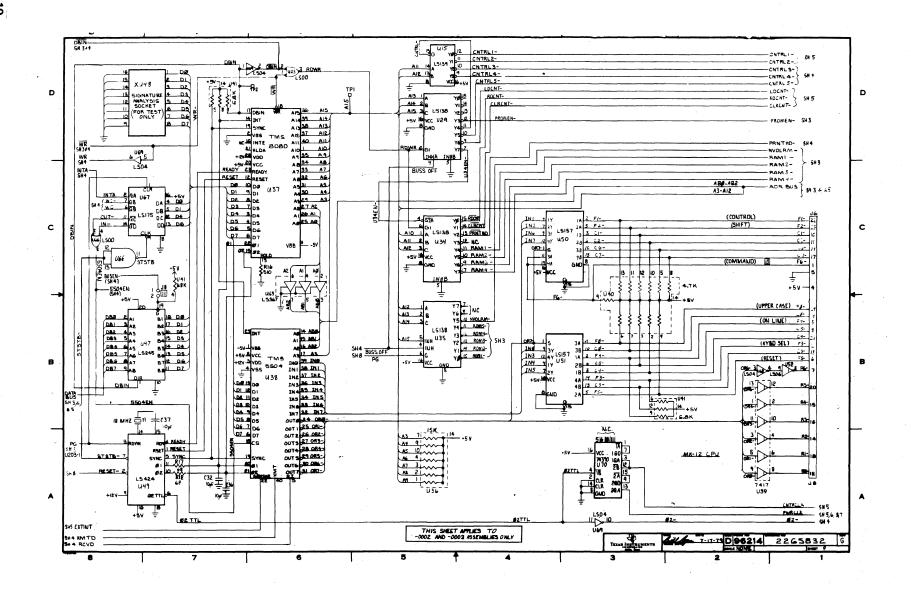


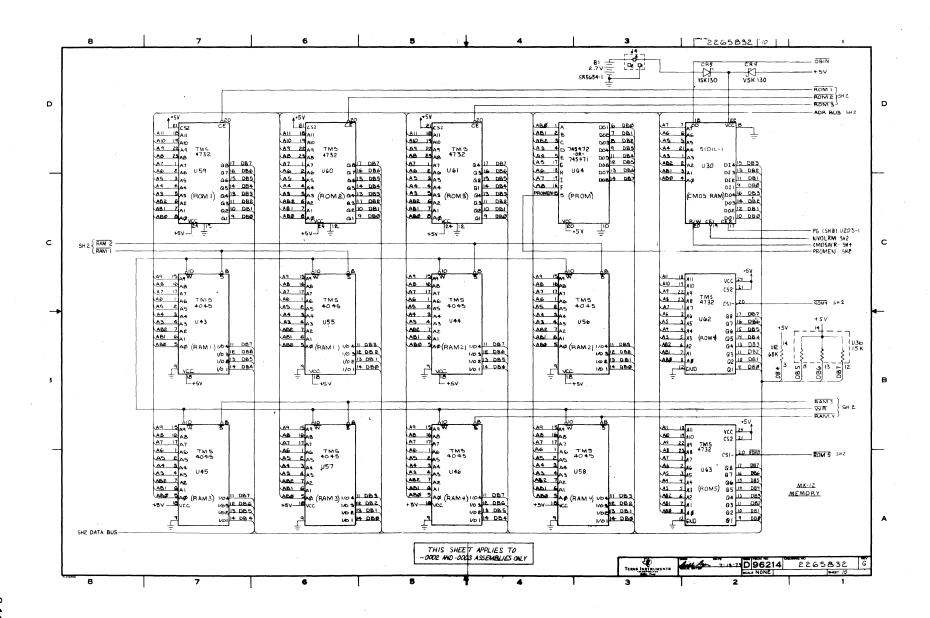


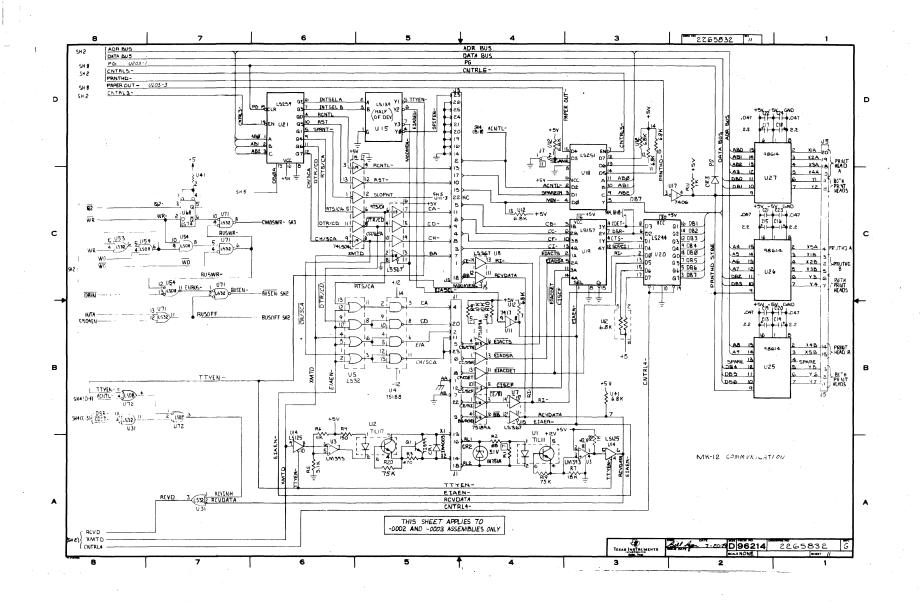


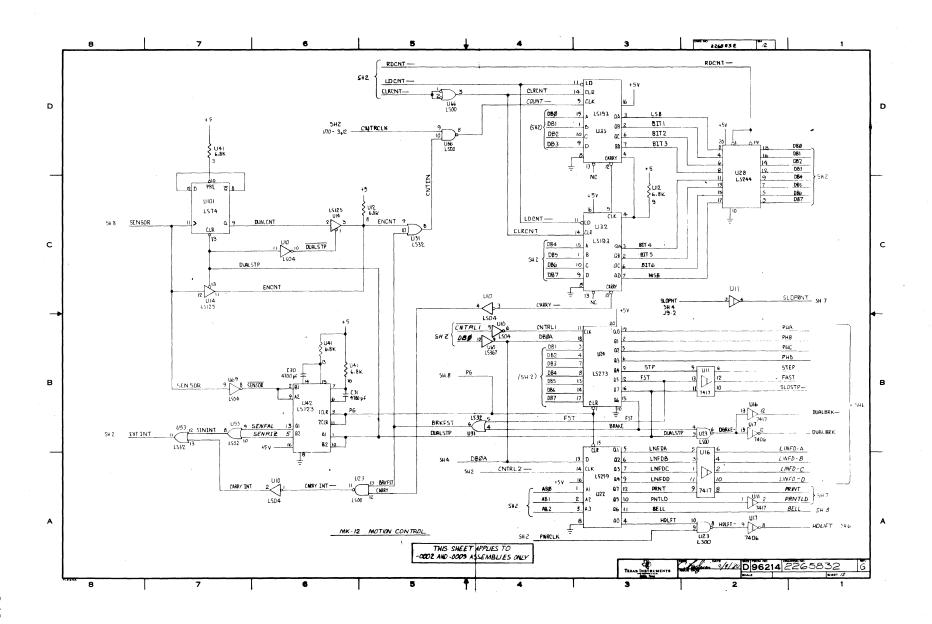


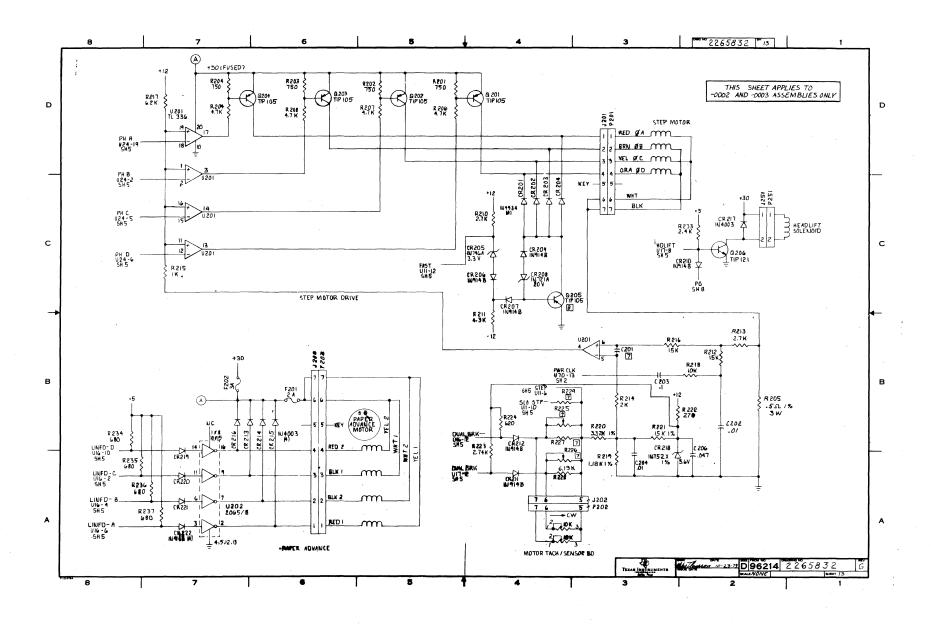


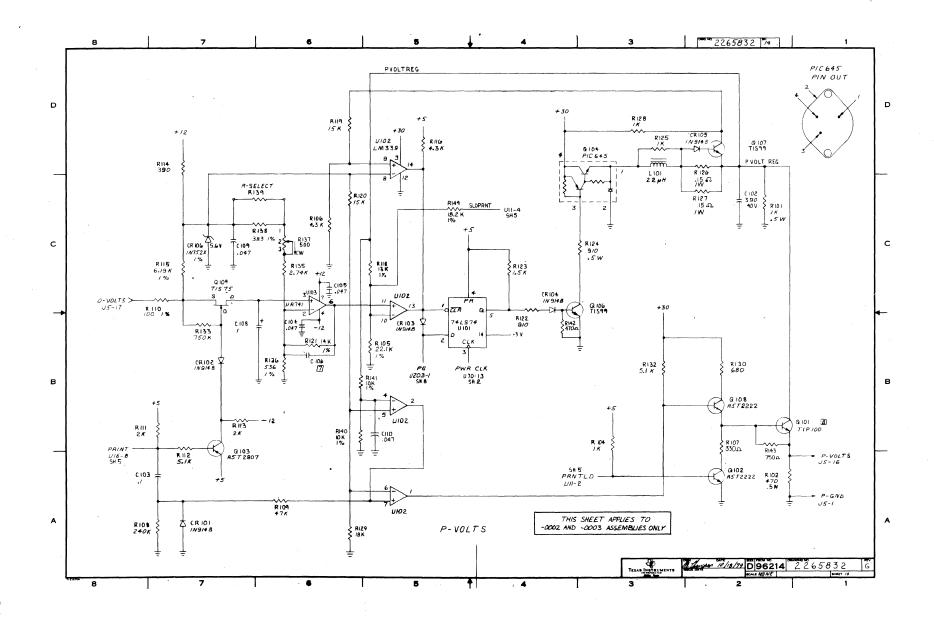


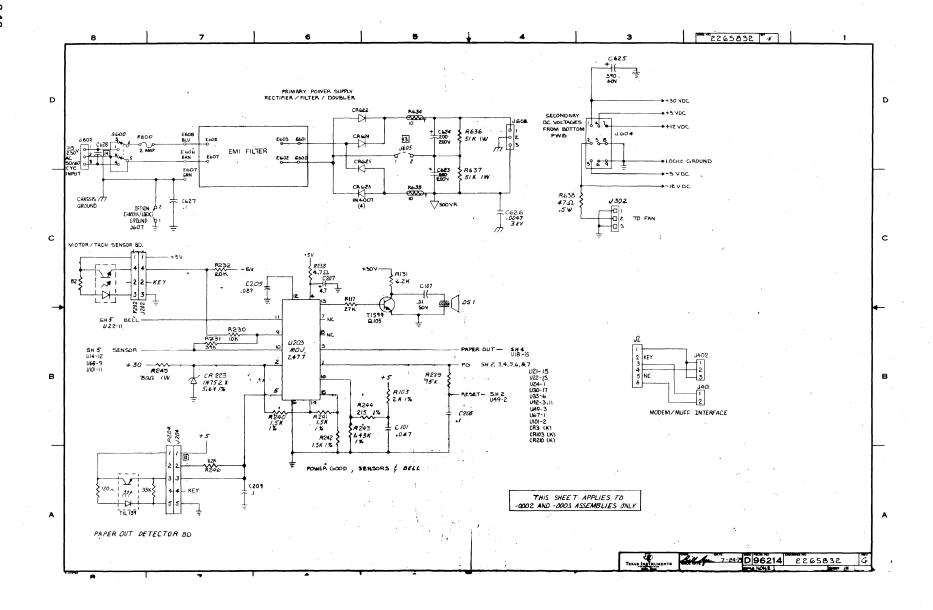


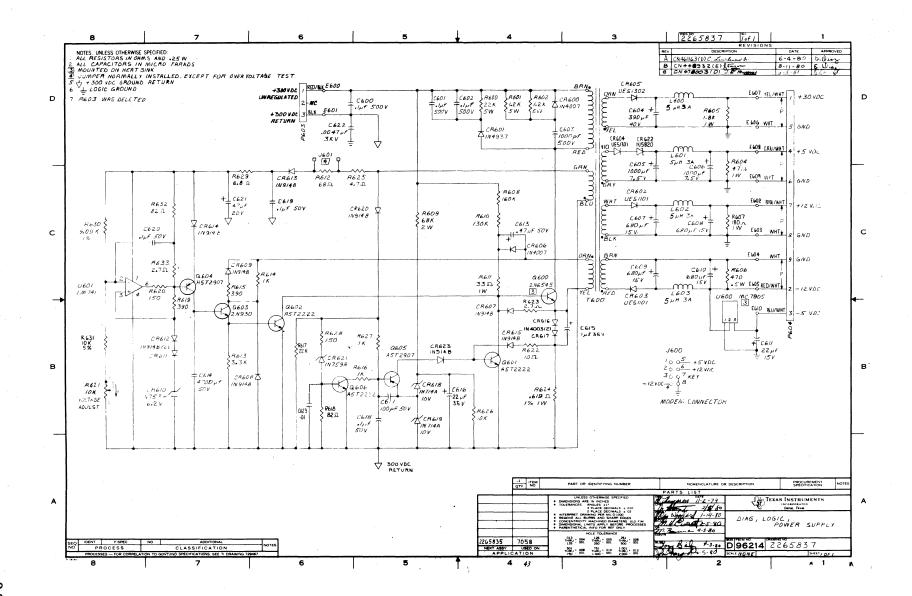


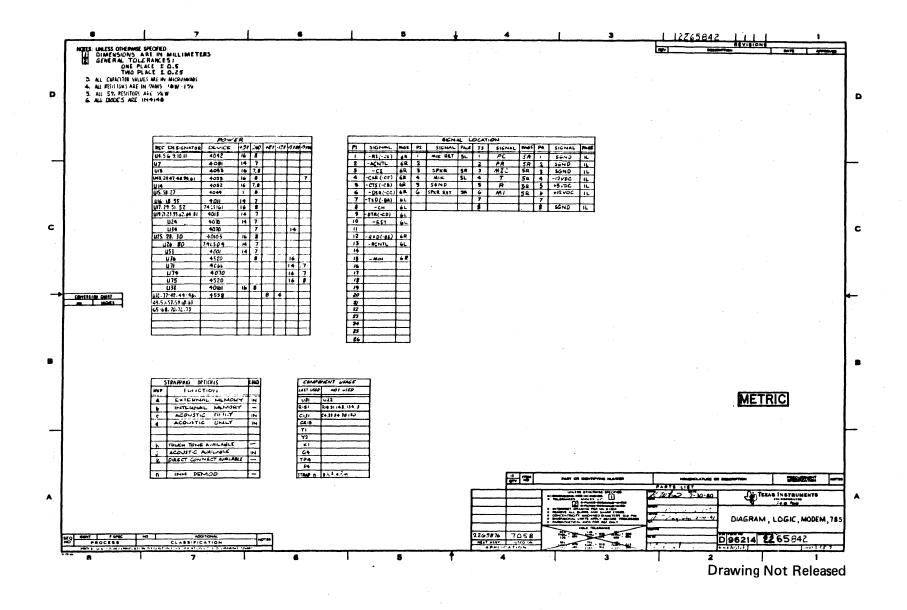


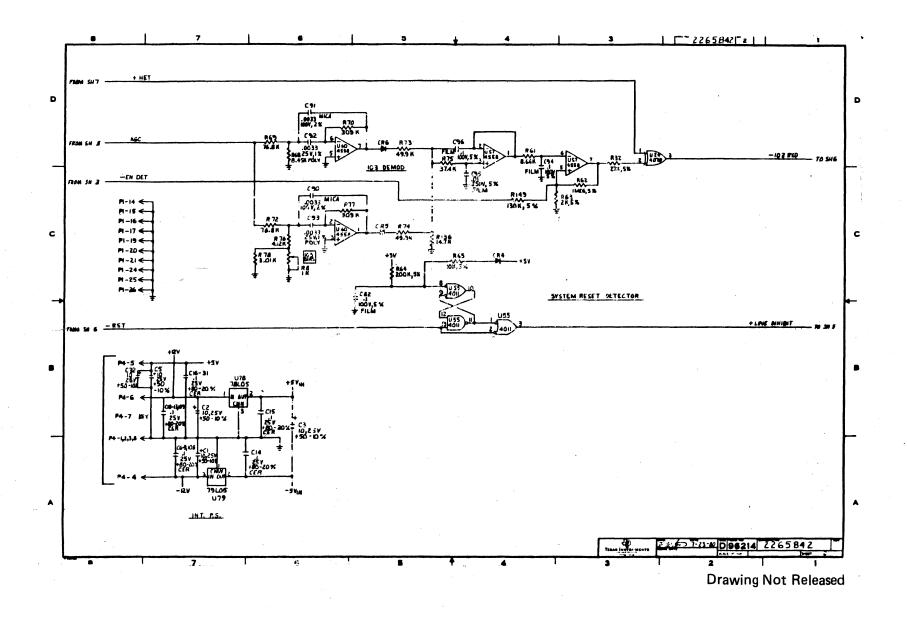


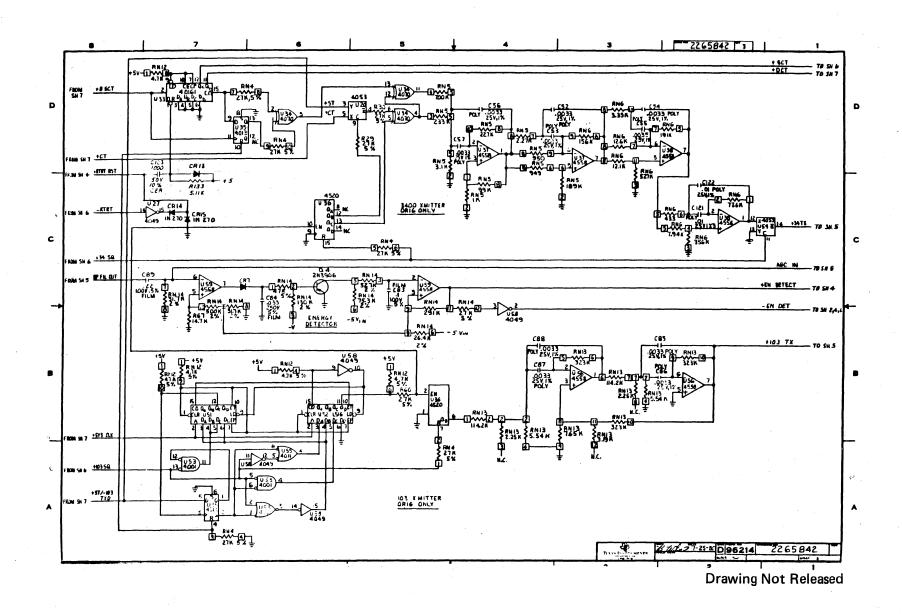


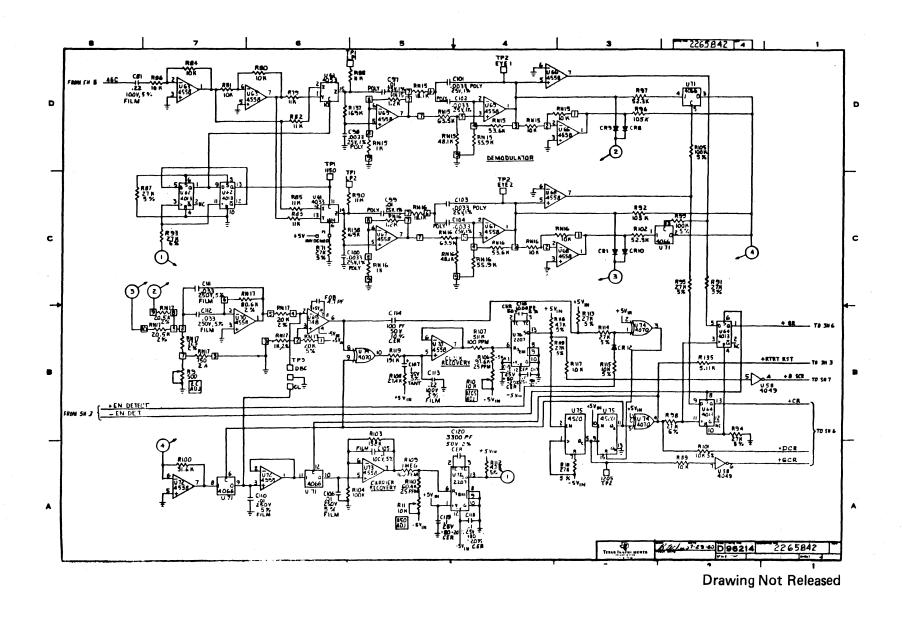


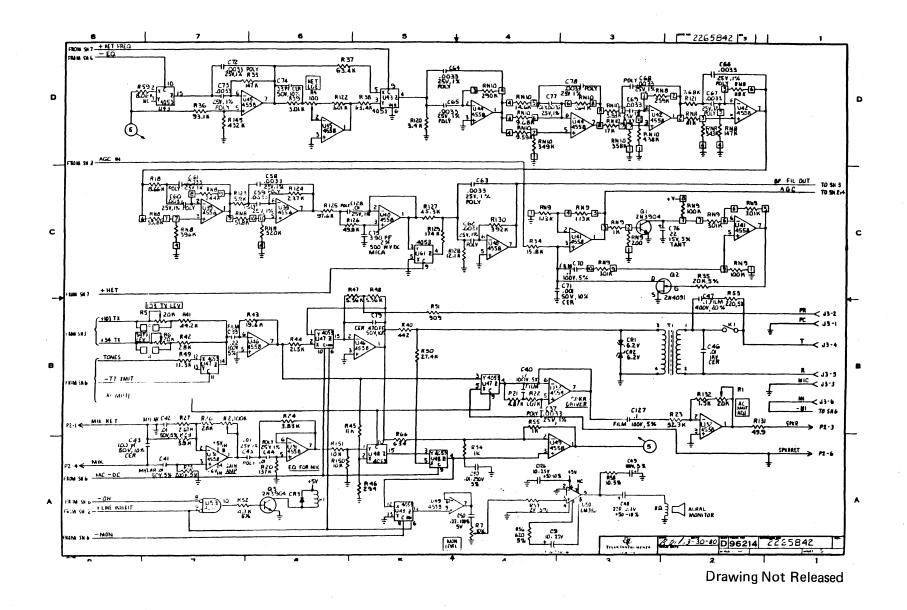


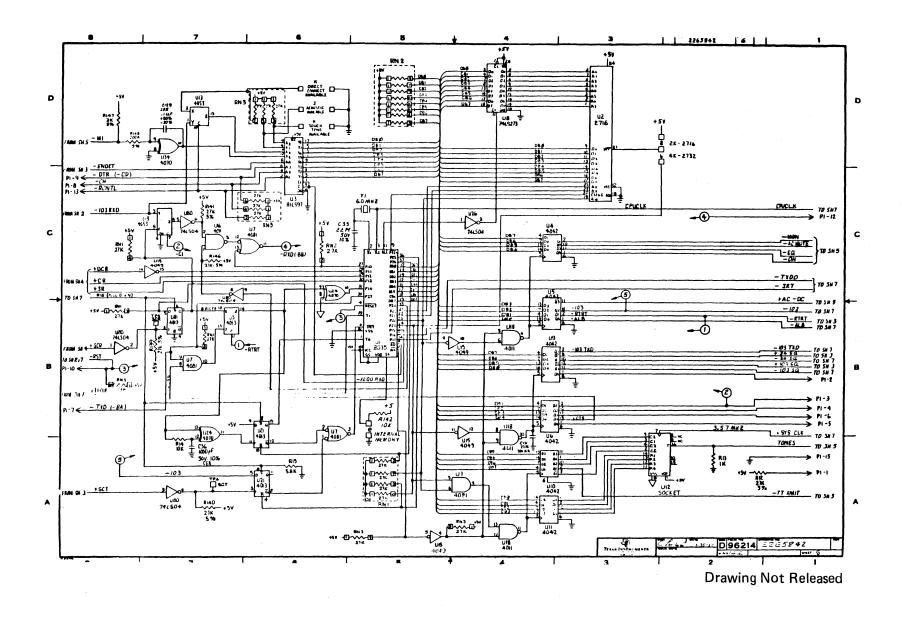


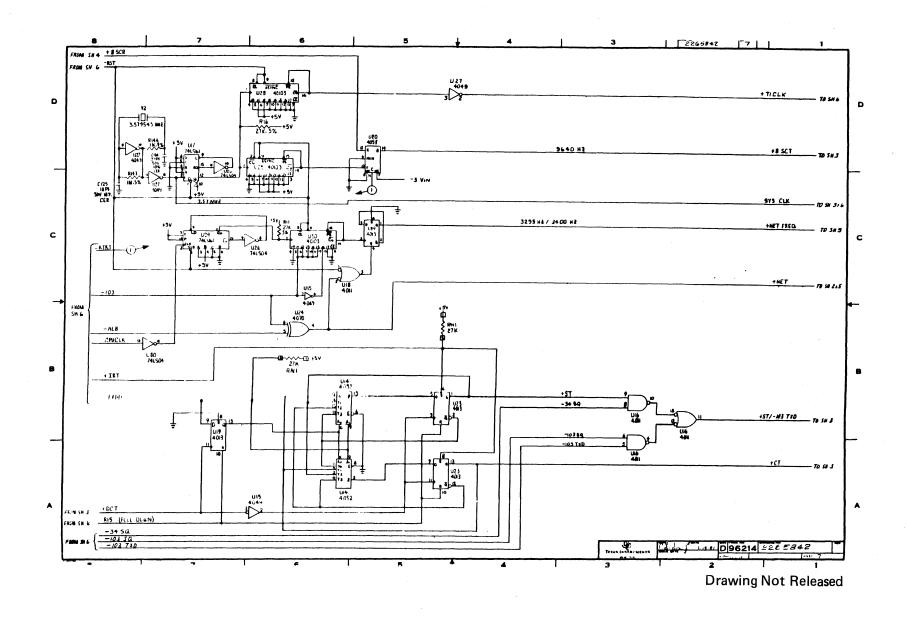


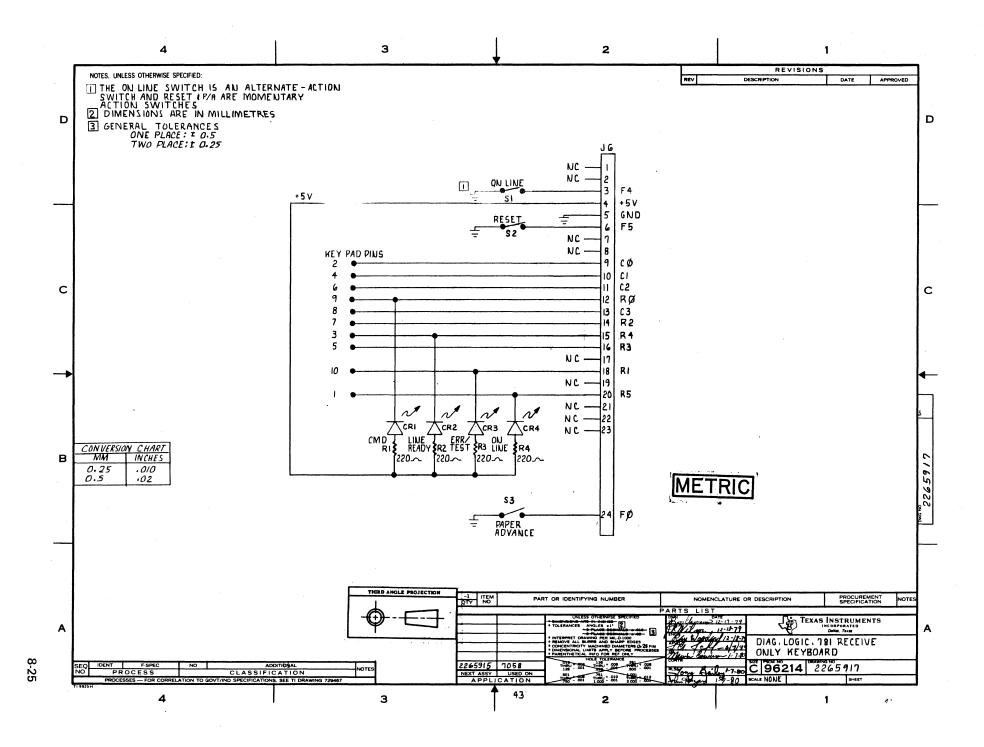


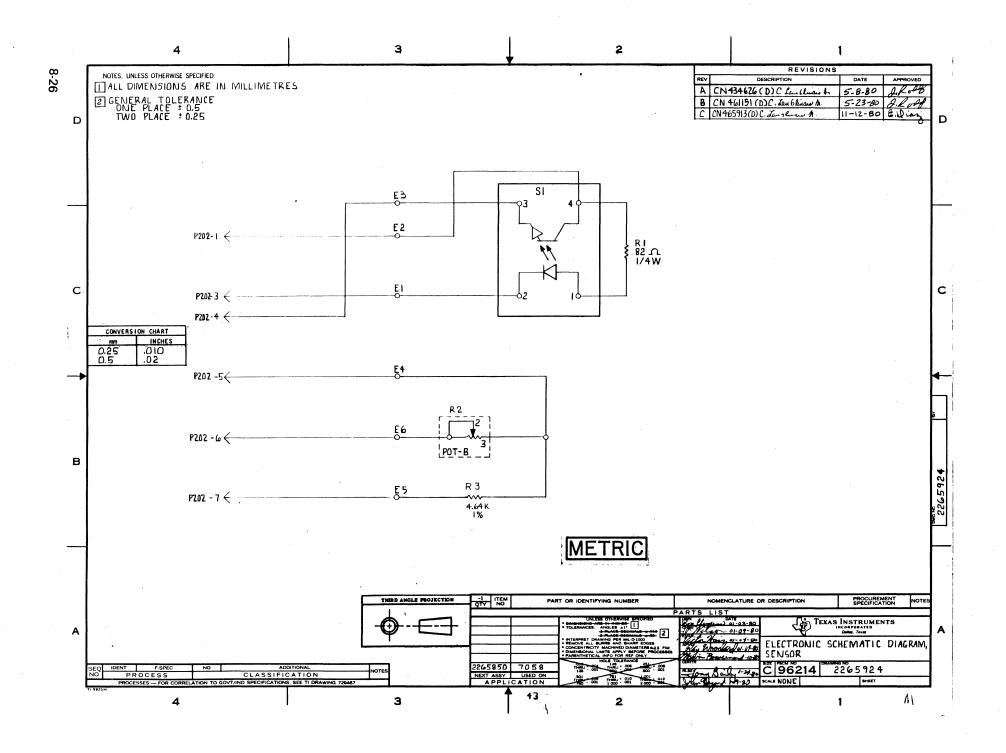


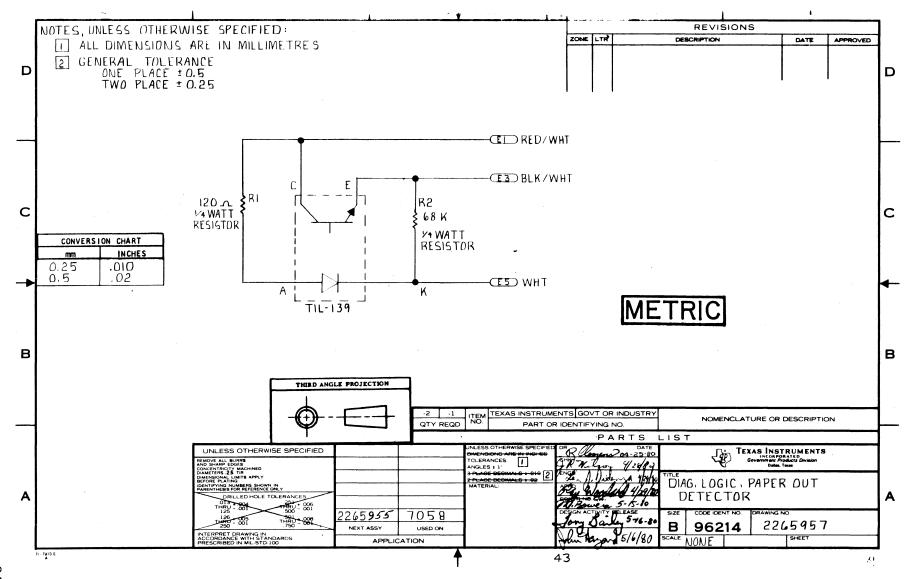




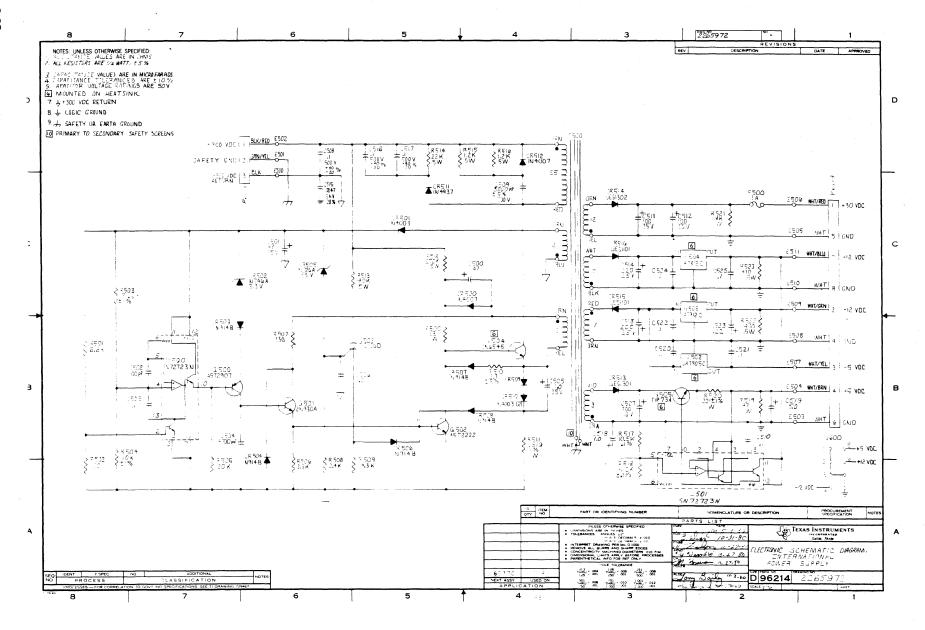








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Appendix A

8080A Microprocessor Data Manual

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TABLE 1 TMS 8080A REGISTERS

NAME	DESIGNATOR	LENGTH	PURPOSE
Accumulator	Α	8	Used for arithmetic, logical, and I/O operations
B Register	В	8	General or most significant 8 bits of double register BC
C Register	С	8	General or least significant 8 bits of double register BC
D Register	D	8	General or most significant 8 bits of double register DE
E Register	E	8	General or least significant 8 bits of double register DE
H Register	н	8	General or most significant 8 bits of double register HL
L Register	· L	8	Gèneral or least significant 8 bits of double register HL
Program Counter	PC	16	Contains address of next byte to be fetched
Stack Pointer	SP	16	Contains address of the last byte of data saved in
			the memory stack
Flag Register	F	5	Five flags (C, Z, S, P, C1)

NOTE: Registers B and C may be used together as a single 16-bit register, likewise, D and E, and H and L.

TABLE 2

FLAG DESCRIPTIONS

SYMBOL	TESTABLE	DESCRIPTION
С	YES	C is the carry/borrow out of the MSB (most significant bit) of the ALU (Arithment Logic Unit). A TRUE condition (C = 1) indicates overflow for addition or underflow for subtraction.
z	YES	A TRUE condition ($Z = 1$) indicates that the output of the ALU is equal to zero.
s	YES	A TRUE condition (S = 1) indicates that the MSB of the ALU output is equal to a one (1).
P	YES	A TRUE condition (P = 1) indicates that the output of the ALU has even parity (the number of bits equal to one is even).
C1	NO	C1 is the carry out of the fourth bit of the ALU (TRUE condition). C1 is used only for BCD correction with the DAA instruction.

TABLE 3
FUNCTION OF THE DAA INSTRUCTION
Assume the accumulator (A) contains two BCD digits, X and Y

	7	4	3		0
ACC	>	(Y	

	ACCUM	ULAT	OR	ACCUMULATOR			
	BEFOR	RE DA	Α	AFTER DAA			
С	A ₇ A ₄	C1	A ₃ A ₀	С	A7 A4	C1	A ₃ A ₀
0	X < 10	0	Y < 10	0	×	0	Υ
0	X < 10	1	Y < 10	0	Х	0	Y + 6
0	X < 9	. 0	Y ≥ 10	0	X + 1	1	Y + 6
1	X < 10	0	Y < 10	1	X + 6	0	Y
1	X < 10	1	Y < 10	1	X + 6	0	Y + 6
1	X < 10	0	Y ≥ 10	1	X + 7	1	Y + 6
0	X ≥ 10	0	Y < 10	1	X + 6	0	Υ '
0	X ≥ 10	1	Y < 10	1	X + 6	0	Y + 6
0	X ≥ 9	O.	Y ≥ 10	1	X + 7	1	Y + 6

NOTE: The corrections shown in Table 3 are sufficient for addition. For subtraction, the programmer must account for the borrow condition that can occur and give erroneous results. The most straight forward method is to set A = 99₁₆ and carry = 1. Then add the minuend to A after subtracting the subtrahend from A.

1.4 THE ARITHMETIC UNIT

Arithmetic operations are performed in an 8-bit parallel arithmetic unit that has both binary and decimal capabilities. Four testable internal flag bits are provided to facilitate program control, and a fifth flag is used for decimal corrections. Table 2 defines these flags and their operation. Decimal corrections are performed with the DAA instruction. The DAA corrects the result of binary arithmetic operation on BCD data as shown in Table 3.

1.5 STATUS AND CONTROL

Two types of status are provided by the TMS 8080A. Certain status is indicated by dedicated control lines. Additional status is transmitted on the data bus during the beginning of each instruction cycle (machine cycle). Table 4 indicates the pin functions of the TMS 8080A. Table 5 defines the status information that is presented during the beginning of each machine cycle (SYNC time) on the data bus.

1.6 I/O OPERATIONS

Input/output operations (I/O) are performed using the IN and OUT instructions. The second byte of these instructions indicates the device address (256 device addresses). When an IN instruction is executed, the input device address appears in duplicate on A7 through A0 and A15 through A8, along with $\overline{\text{WO}}$ and INP status on the data bus. The addressed input device then puts its input data on the data bus for entry into the accumulator. When an OUT instruction is executed, the same operation occurs except that the data bus has OUT status and then has output data.

Direct memory access channels (DMA) can be OR-tied directly with the data and address buses through the use of the HOLD and HLDA (hold acknowledge) controls. When a HOLD request is accepted by the CPU, HLDA goes high, the address and data lines are forced to a high-impedance or "floating" condition, and the CPU stops until the HOLD request is removed.

Interfacing with different speed memories is easily accomplished by use of the WAIT and READY pins. During each machine cycle, the CPU polls the READY input and enters a wait condition until the READY line becomes true. When the WAIT output pin is high, it indicates that the CPU has entered the wait state.

Designing interrupt driven systems is simplified through the use of vectored interrupts. At the end of each instruction, the CPU polls the INT input to determine if an interrupt request is being made. This action does not occur if the CPU is in the HOLD state or if interrupts are disabled. The INTE output indicates if the interrupt logic is enabled (INTE is high). When a request is honored, the INTA status bit becomes high, and an RST instruction may be inserted to force the CPU to jump to one of eight possible locations. Enabling or disabling interrupts is controlled by special instructions (El or DI). The interrupt input is automatically disabled when an interrupt request is accepted or when a RESET signal is received.

1.7 INSTRUCTION TIMING

The execution time of the instructions varies depending on the operation required and the number of memory references needed. A machine cycle is defined to be a memory referencing operation and is either 3, 4, or 5 state times long. A state time (designated S) is a full cycle of clocks $\phi 1$ and $\phi 2$. (NOTE: The exception to this rule is the DAD instruction, which consists of 1 memory reference in 10 state times). The first machine cycle (designated M1) is either 4 or 5 state times long and is the "instruction fetch" cycle with the program counter appearing on the address bus. The CPU then continues with as many M cycles as necessary to complete the execution of the instruction (up to a maximum of 5). Thus the instruction execution time varies from 4 state times (several including ADDr) to 18 (XTHL). The WAIT or HOLD conditions may affect the execution time since they can be used to control the machine (for example to "single step") and the HALT instruction forces the CPU to stop until an interrupt is received. As the instruction execution is completed (or in the HALT state) the INT pin is polled for an interrupt. In the event of an interrupt, the PC will not be incremented during the next M1 and an RST instruction can be inserted.

TMS 8080A MICROPROCESSOR

1. ARCHITECTURE

1.1 INTRODUCTION

The TMS 8080A is an 8-bit parallel central processing unit (CPU) fabricated on a single chip using a high-speed N-channel silicon-gate process. (See Figure 1). A complete microcomputer system with a 2-µs instruction cycle can be formed by interfacing this circuit with any appropriate memory. Separate 8-bit data and 16-bit address buses simplify the interface and allow direct addressing of 65,536 bytes of memory. Up to 256 input and 256 output ports are also provided with direct addressing. Control signals are brought directly out of the processor and all signals, excluding clocks, are TTL compatible.

1.2 THE STACK

The TMS 8080A incorporates a stack architecture in which a portion of external memory is used as a pushdown stack for storing data from working registers and internal machine status. A 16-bit stack pointer (SP) is provided to facilitate stack location in the memory and to allow almost unlimited interrupt handling capability. The CALL and RST (restart) instructions use the SP to store the program counter (PC) into the stack. The RET (return) instruction uses the SP to acquire the previous PC value. Additional instructions allow data from registers and flags to be saved in the stack.

1.3 REGISTERS

The TMS 8080 A has three categories of registers: general registers, program control registers, and internal registers. The general registers and program control registers are listed in Table 1. The internal registers are not accessible by the programmer. They include the instruction register, which holds the present instruction, and several temporary storage registers to hold internal data or latch input and output addresses and data.

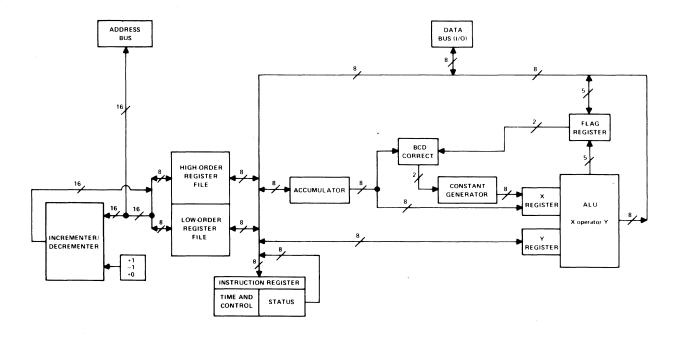


FIGURE 1-TMS 8080A FUNCTIONAL BLOCK DIAGRAM

TABLE 4
TMS 8080A PIN DEFINITIONS

SIGNATURE	PIN	1/0		DESCRIPTION
A15 (MSB)	36	OUT		A15 through A0 comprise the address bus. True memory or I/O device addresses appear on
A14	39	OUT		this 3-state bus during the first state time of each instruction cycle.
A13	38	OUT		
A12	37	ОПТ		
A11	40	оит		
A10	1	OUT		
Α9	35	OUT		
A8	34	OUT		
A7	33	оит		
A6	32	OUT		
A5	31	OUT		
A4	30	OUT		
А3	29	OUT		
A2	27	OUT		
A1	26	OUT	. •	
A0 (LSB)	25	оит	•	
D7 (MSB)	6	IN/OUT		
D6	5	IN/OUT		D7 through D0 comprise the bidirectional 3-state data bus. Memory, status, or I/O data is
D5	4	IN/OUT		transferred on this bus.
D4	3	IN/OUT		•
D3	7	IN/OUT		
D2	8	IN/OUT	,	
D1	9	IN/OUT		
D0 (LSB)	10	IN/OUT	-	
DO (LSB)	10	IN/OUT		
V _{SS}	2			Ground reference
V _{BB}	11			Supply voltage (-5 V nominal)
V _{CC}	20			Supply voltage (5 V nominal)
V _{DD}	28			Supply voltage (12 V nominal)
φ1	22	IN		Phase 1 clock.
φ2	15	IN		Phase 2 clock. See page 19 for ϕ 1 and ϕ 2 timing
RESET	12	IN		Reset. When active (high) for a minimum of 3 clock cycles, the RESET input causes the TMS 8080A to be reset. PC is cleared, interrupts are disabled, and after RESET, instruction execution starts at memory location 0. To prevent a lockup condition, a HALT instruction must not be used in location 0.
HOLD	13	IN		Hold signal. When active (high) HOLD causes the TMS 8080A to enter a hold state and float (put the 3-state address and data bus in a high-impedance state). The chip acknowledges entering the hold state with the HLDA signal and will not accept interrupts until it leaves the hold state.
INT	14	IN		Interrupt request, When active (high) INT indicates to the TMS 8080A that an interrupt is being requested. The TMS 8080A polls INT during a HALT or at the end of an instruction. The request will be accepted except when INTE is low or the CPU is in the HOLD condition.
INTE	16	OUT		Interrupts enabled, INTE indicates that an interrupt will be accepted by the TMS 8080A unless it is in the hold state, INTE is set to a high logic level by the EI (Enable Interrupt) instruction and reset to a low logic level by the DI (Disable Interrupt) instruction. INTE is also reset when an interrupt is accepted and by a high on RESET.
DBIN	17	оит		Data bus in. DBIN indicates whether the data bus is in an input or an output mode. (high = input, low = output).

TABLE 4 (CONTINUED)

SIGNATURE	PIN	1/0	DESCRIPTION
WR	18	оит	Write, When active (low) WR indicates a write operation on the data bus to memory or to an I/O port.
SYNC	19	OUT	Synchronizing control line. When active (high) SYNC indicates the beginning of each machine cycle of the TMS 8080A. Status information is also present on the data bus during SYNC for external latches.
HLDA	21	оит	Hold acknowledge. When active (high) HLDA indicates that the TMS 8080A is in a hold state.
READY	23	IN	Ready control line. An active (high) level indicates to the TMS 8080A that an external device has completed the transfer of data to or from the data bus. READY is used in conjunction with WAIT for different memory speeds.
WAIT	24	OUT	Wait status. When active (high) WAIT indicates that the TMS 8080A has entered a wait state pending a READY signal from memory.

TABLE 5 TMS 8080A STATUS

SIGNATURE	DATA BUS BIT	DESCRIPTION
INTA	D0	Interrupt acknowledge.
wo	D1	Indicates that current machine cycle will be a read (input) (high = read) or a write (output) (low = write) operation.
STACK	D2	Indicates that address is stack address from the SP.
HLTA	D3	HALT instruction acknowledge.
OUT	D4	Indicates that the address bus has an output device address and the data bus has output data.
M1	D5	Indicates instruction acquisition for first byte.
INP	D6	Indicates address bus has address of input device.
MEMR	D7	Indicates that data bus will be used for memory read data.

2. TMS 8080A INSTRUCTION SET

2.1 INSTRUCTION FORMATS

TMS 8080A instructions are either one, two, or three bytes long and are stored as binary integers in successive memory locations in the format shown below.

One-Byte Instructions	
D7 D6 D5 D4 D3 D2 D1 D0	OP CODE
Two-Byte Instructions	
D7 D6 D5 D4 D3 D2 D1 D0	OP CODE
D7 D8 D5 D4 D3 D2 D1 D0	OPERAND
Three-Byte Instructions	
D7 D6 D5 D4 D3 D2 D1 D0	OP CODE
	•
D7 D6 D5 D4 D3 D2 D1 D0	LOW ADDRESS OR OPERAND 1
D7 D6 D5 D4 D3 D2 D1 D0	HIGH ADDRESS OR OPERAND 2

2.2 INSTRUCTION SET DESCRIPTION

Operations resulting from the execution of TMS 8080A instructions are described in this section. The flags that are affected by each instruction are given after the description.

2.2.1 INSTRUCTION SYMBOLS

SYMBOL		DESCRIPTION	
<u><b2></b2></u>	Second byte of in	struction	
 b3>	Third byte of inst	ruction	
ra	Registe	r #	Register Name
	000		В
	001		С
	010		D
	011		Е
	100		Н
	101		L
	111		· A
r _b	Registe	r #	Register Name
	00		BC
	01		DE
	10		HL
	11		SP
r _c	Registe	<u>r #</u>	Register Name
	0		ВС
	1		DE
^r d	Registe	<u>r #</u>	Register Name
	00		BC
	01		DE
	10		HL
^r dL	Least significant 8		
rdH	Most significant 8	bits of rd	
f	Flags	True condition	
	Zero (Z)	Result is zero	
	Carry (C)	Carry/borrow out of MSB i	s one
	Parity (P)	Parity of result is even	
	Sign (S)	MSB of result is one	
	Carry 1(C1)	Carry out of fourth bit is o	ne
M		lefined by registers H and L	
()		ied address or register	
[]		ss contained in specified registe	er
←	Is transferred to		
↔	Exchange		
Am	Bit m of A registe	r (accumulator)	
{}	Flags affected	disas susuand	
b2	Single byte immed	•	
b3b2	Double byte imme	•	
(nnn)8	(nnn) is an octal (base 8) number	

2.2.2 ACCUMULATOR GROUP INSTRUCTIONS

			M CYCLES/	
MNEMONIC	OPERANDS	BYTES	STATES	DESCRIPTION
ACI	b ₂	2	2/7	(A) \leftarrow (A) + $<$ b ₂ $>$ +(carry), add the second byte of the
				instruction and the contents of the carry flag to register A and
				place in A. (C,Z,S,P,C1)
ADC	М	1	2/7	$(A) \leftarrow (A) + (M) + (carry) \cdot \{C,Z,S,P,C1\}$
ADC	ra	1	1/4	$(A) \leftarrow (A) + (r_a) + (carry) \cdot \{C,Z,S,P,C1\}$
ADD	M	1	2/7	(A) \leftarrow (A) + (M), add the contents of M to register A and place in
				A. \C,Z,S,P,C1\
ADD	ra	1	1/4	$(A) \leftarrow (A) + (r_a). \{C,Z,S,P,C1\}$
ADI	b2	2	2/7	$(A) \leftarrow (A) + \langle b_2 \rangle . \{C,Z,S,P,C1\}$
ANA	M	1	2/7	(A) \leftarrow (A) AND (M), take the logical AND of M and register A
				and place in A. The carry flag will be reset low. { C,Z,S,P,C1}
ANA	ra	1	1/4	$(A) \leftarrow (A) \text{ AND } (r_a). \{C,Z,S,P,C1\}$
ANI	b2	2	2/7	$(A) \leftarrow (A) \text{ AND } < b_2 > . \{C,Z,S,P,C1\}$
CMA		1	1/4	$(A) \leftarrow (\overline{A})$, complement A.
CMC		1	1/4	$(carry) \leftarrow (\overline{carry})$, complement the carry flag. $\{C\}$
CMP	M	1	2/7	(A) $-$ (M), compare the contents of M to register A and set the
				flags accordingly. { C,Z,S,P,C1}
				(A) = (M) $Z = 1$
				$(A) \neq (M) \qquad Z = 0$
				$(A) < (M) \qquad C = 1$
				$(A) > (M) \qquad C = 0$
CMP	ra	1	1/4	$(A) - (r_a). \{C,Z,S,P,C1\}$
CPI	b2	2	2/7	$(A) - \langle b_2 \rangle. \{C,Z,S,P,C1\}$
DAA		1	1/4	(A)←BCD correction of (A). The 8 bit A contents is corrected to
				form two 4 bit BCD digits after a binary arithmetic operation. A
				fifth flag C1 indicates the overflow from A_3 . The carry flag C
				indicates the overflow from A ₇ (See Table 3). $\{C,Z,S,P,C1\}$
DAD	^r b	1	1/10	(HL) \leftarrow (HL) + (r _b), add the contents of double register r _b to
				double register HL and place in HL. $\{C\}$
LDA	b3b2	3	4/13	$(A) \leftarrow [\langle b_3 \rangle \langle b_2 \rangle]$
LDAX	r _c	1	2/7	$(A)\leftarrow[(r_c)]$
ORA	Μ	1	2/7	(A) \leftarrow (A) OR (M), take the logical OR of the contents of M and
				register A and place in A. The carry flag will be reset.
				{ c,z,s,p,c1 }
ORA	r _a	1	1/4	$(A) \leftarrow (A) OR (r_a).\{C,Z,S,P,C1\}$
ORI	b ₂	2	2/7	$(A) \leftarrow (A) OR < b_2 >. \{C,Z,S,P,C1\}$
RAL		1	1/4	$A_{m+1}\leftarrow A_m$, $A_0\leftarrow$ (carry), (carry) \leftarrow (A_7). Shift the contents of
				register A to the left one bit through the carry flag. $\{C\}$
RAR		1	1/4	$A_m \leftarrow A_m + 1$, $A_7 \leftarrow (carry)$, $(carry) \leftarrow A_0 \cdot \{C\}$
RLC		1	1/4	$A_{m+1} \leftarrow A_m$, $A_0 \leftarrow A_7$ (carry) \leftarrow (A_7). Shift the contents of register
				A to the left one bit. Shift A7 into A and into the carry
				flag. { C }
RRC		1	1/4	$A_{m} \leftarrow A_{m+1}$, $A_{7} \leftarrow A_{0}$, $(carry) \leftarrow (A_{0})$. $\{C\}$
				• • • • • • • • • • • • • • • • • • • •

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES
SBB	M	1	2/7
SBB	r _a	1	1/4
SBI	b ₂	2	2/7
STA	b3b2	3	4/13
STAX	r _C	1	2/7
STC		1	1/4
SUB	Μ	1	2/7
SUB	ra	1	1/4
SUI	b ₂	2	2/7
XRA	M	1	2/7
XRA	r _a	1	1/4
XRI	b ₂	2	2/7

2.2.3 INPUT/OUTPUT INSTRUCTIONS

			M CYCLES/
MNEMONIC	OPERANDS	BYTES	STATES
IN	b ₂	2	3/10
OUT	b ₂	2	3/10

2.2.4 MACHINE INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES
HLT		1	2/7
NOP		1	1/4

DESCRIPTION

 $(A)\leftarrow (A)-(M)-(carry)$, subtract the contents of M and the contents of the carry flag from register A and place in A. Two's complement subtraction is used and a true borrow causes the carry flag to be set (underflow condition). $\{C,Z,S,P,C1\}$

$$(A)\leftarrow (A)-(r_a)-(carry). \{C,Z,S,P,C1\}$$

$$(A) \leftarrow (A) - -(carry). \{C, Z, S, P, C1\}$$

 $[<b_3><b_2>]\leftarrow(A)$, store contents of A in memory address given in bytes 2 and 3.

 $[\{r_c\}] \leftarrow (A)$, store contents of A in memory address given in BC or DE,

(carry)←1, set carry flag to a 1 (true condition).

(A) \leftarrow (A)-(M), subtract the contents of M from register A and place in A. Two's complement subtraction is used and a true borrow causes the carry flag to be set (underflow condition). $\{C,Z,S,P,C1\}$

$$(A)\leftarrow (A)-(r_a), \{C,Z,S,P,C1\}$$

$$(A) \leftarrow (A) - < b_2 > \{C, Z, S, P, C1\}$$

(A) \leftarrow (A) XOR (M), take the exclusive OR of the contents of M and register A and place in A. The carry flag will be reset.

{C,Z,S,P,C1}

(A)←(A) XOR (r_a). {C,Z,S,P,C1}

(A)←(A) XOR <b2>. {C,Z,S,P,C1}

DESCRIPTION

(A)←(input data from data bus), byte 2 is sent on bits A7-A0 and A15-A8 as the input device address. INP status is given on the data bus.

(Output data)—(A), byte 2 is sent on bits A7-A0 and A15-A8 as the output device address. OUT status is given on the data bus.

DESCRIPTION

Halt, all machine operations stop. All registers are maintained. Only an interrupt can return the TMS 8080A to the run mode. Note that a HLT should not be placed in location zero, otherwise after the reset pin is active, the TMS 8080A will enter a nonrecoverable state (until power is removed), i.e., in halt with interrupts disabled. This condition also occurs if a HLT is executed while interrupts are disabled. HLTA status is given on the data bus.

 $(PC)\leftarrow (PC)+1$, no operation.

2.2.5 PROGRAM COUNTER AND STACK CONTROL INSTRUCTIONS

M CYCLES/

MNEMONIC	OPERANDS	BYTES	STATES	DESCRIPTION
CALL	b3b2	3	5/17	[(SP)-1] [(SP)-2] \leftarrow (PC), (SP) \leftarrow (SP)-2, (PC) \leftarrow b_3 > b_2 >,
	3 2			transfer PC to the stack address given by SP, decrement SP
				twice, and jump unconditionally to address given in bytes 2 and
				3.
Conditional cal	l instructions for	r true flags:		
(f)	1 10,50, 400, 611, 101	truo mugu.	5/17 (Pass)	If (f) = 1, [(SP)-1] [(SP)-2] \leftarrow (PC), (SP) \leftarrow (SP)-2, (PS) \leftarrow $<$ b ₃ >
CC (carry)	b3b2	3	3/11 (Fail)	$\langle b_2 \rangle$, otherwise (PC) \leftarrow (PC)+3. If the flag specified, f, is 1, then
CPE (parity)	b3b2	3	3/11 (1 all/	execute a call. Otherwise, execute the next instruction.
CM (sign)	• -	3		execute a can. Otherwise, execute the next histraction.
CZ (zero)	b3b2	3		
	b3b2			
	instructions for	raise mags.	5/17 (Pass)	14 14) = 0 (199) 11 (199) 21 (190) 199) 199) 2 (190) 2 (190)
(f)	L L	2		If (f) = 0, [(SP)-1] [(SP)-2] \leftarrow (PC), (SP) \leftarrow (SP)-2, (PC) \leftarrow Shell extracted (PC) (PC) 2
CNC (carry)	b3b2	3	3/11 (Fail)	<b2>, otherwise (PC)←(PC)+3.</b2>
CPO (parity)	b3b2	3		
CP (sign)	b3b2	3		
CNZ (zero)	b3b2	3		
DI		1	1/4 .	Disable interrupts. INTE is driven false to indicate that no interrupts will be accepted.
EI		1	1/4	Enable interrupts. INTE is driven true to indicate that an interrupt will be accepted. Execution of this instruction is delayed to allow the next instruction to be executed before the
				INT input is polled.
JMP	b3b2	3	3/10	(PC)← <b3> <b2>, jump unconditionally to address given in</b2></b3>
	0.2			bytes 2 and 3.
Conditional jun	np instructions fo	or true flags:		
(f)		_	3/10	If (f) = 1, (PC) \leftarrow 53><52>, otherwise (PC) \leftarrow (PC)+3. If the flag
JC (carry)	b3b2	3		specified, f, is 1, execute a JMP. Otherwise, execute the next
JPE (parity)	b3b2	3		instruction.
JM (sign)	b3b2	3		
JZ (zero)	b3b2	3		
	np instructions for			
(f)	ip matractions in	or raise mags.	3/10	If (f) = 0, (PC) \leftarrow b ₃ > b ₂ >, othewise (PC) \leftarrow (PC)+3.
JNC (carry)	bobo	3	3/10	11 (1) 0, (1 c) \ \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
JPO (parity)	b3b2	3		
JM (sign)	b3b2			
JNZ (zero)	b3b2	3		
PCHL	b3b2	3	4.15	(00) (11)
	0014	1	1/5	(PC)←(HL)
POP	PSW	1	3/10	$(F)\leftarrow [(SP)]$, $(A)\leftarrow [(SP)+1]$, $(SP)\leftarrow (SP)+2$, restore the last stack values addressed by SP into A and F. Increment SP twice.
POP	^r d	1	3/10	$(r_{dL}) \leftarrow [(SP)], (r_{dH}) \leftarrow [(SP)+1], (SP) \leftarrow (SP)+2.$
PUSH	PSW	1	3/11	[(SP)-1]-(A), [(SP)-2]-(F), (SP)-(SP)-2, save the contents of A and F into the stack addressed by SP. Decrement SP twice.
PUSH	^r d	1	3/11	$\lfloor (SP)-1 \rfloor \leftarrow (r_{dL}), \lceil (SP)-2 \rceil \leftarrow (r_{dH}), (SP) \leftarrow (SP)-2.$
RET	.	1	3/10	(PC)←[(SP)] [(SP)+1], (SP)←(SP)+2, return to program at memory address given by last values in the stack. The SP is
				incremented by two.

			M CYCLES/	
MNEMONIC	OPERANDS E	SYTES	STATES	DESCRIPTION
Conditional reti	urn instructions for	true flag	s:	
(f)			3/11 (Pass)	If $(f) = 1$, $(PC) \leftarrow [(SP)]$ $[(SP+1]$, $(SP) \leftarrow (SP) + 2$. If the flag
RC (carry)	С	1	1/5 (Fail)	specified, f, is 1, execute a RET. Otherwise, execute the next
RPE (parity)	Р	1		instruction.
RM (sign)	S	1		
RZ (zero)	Z	1		
Conditional reti	urn instructions for	false flag	js:	
(f)			3/11 (Pass)	If (f) = 0, $(PC)\leftarrow[(SP)]$ [$(SP)+1$], $(SP)\leftarrow(SP)+2$.
RNC (carry)	С	1	1/5 (Fail)	
RPO (parity)	Р	1		•
RP (sign)	S	1		
RNZ (zero)	Z	1		
RST		1	3/11	[(SP)-1] [(SP)-2] \leftarrow (PC) (SP) \leftarrow (SP)-2, (PC) \leftarrow 0000R0 ₈ where
				R is a 3 bit field in RST (RST=3R7g). Transfer PC to the stack
			•	address given by SP, decrement SP twice, and jump to the
				address specified by R.
SPHL		1	1/5	(SP)←(HL).
RP (sign) RNZ (zero) RST	S	1 1 1 1		R is a 3 bit field in RST (RST=3R7g). Transfer PC t address given by SP, decrement SP twice, and ju address specified by R.

2.2.6 REGISTER GROUP INSTRUCTIONS

			M CYCLES/	
MNEMONIC	OPERANDS	BYTES	STATES	DESCRIPTION
DCR	M	1	3/10	(M)←(M)-1, decrement the contents of memory location
				specified by H and L. {Z,S,P,C1}
DCR	ra	1	1/5	$(r_a)\leftarrow (r_a)-1$, decrement the contents of register r_a . $\{Z,S,P,C1\}$
DCX	^r b	1	1/5	$(r_b)\leftarrow (r_b)-1$, decrement double registers BC, DE, HL, or SP.
INR	M	1	3/10	$(M)\leftarrow (M)+1$, increment the contents of memory location specified by H and L. $\{Z,S,P,C1\}$
INR	r _a	1	1/5	$(r_a)\leftarrow (r_a)+1$, increment the contents of register r_a . $\{Z,S,P,C1\}$
INX	r _b	1	1/5	$(r_b)\leftarrow (r_b)+1$, increment double registers BC, DE, HL, or SP.
LHLD	b3b2	3	5/16	(L) \leftarrow [$<$ b3 $>$ $<$ b2 $>$]; (H) \leftarrow [$<$ b3 $>$ $<$ b2 $>$ +1], load registers H and L with contents of the two memory locations specified by bytes 3 and 2.
LXI	r _b b3b2	3	3/10	$(r_{bH})\leftarrow $; $(r_{bL})\leftarrow $, load double registers BC, DE, HL, or SP immediate with bytes 3, 2, respectively.
MVI	M,b ₂	2	3/10	(M) \leftarrow < b_2 >, store immediate byte 2 in the address specified by HL
MVI	r _a b2	2	2/7	$(r_a)\leftarrow $, load register r_a immediate with byte 2 of the instruction.
MOV	Mr _a	1	2/7	$(M)\leftarrow (r_a)$, store register r_a in the memory location addressed by H and L.
MOV	r _a M	1	2/7	$(r_a)\leftarrow (M)$, load register r_a with contents of memory addressed by HL.
MOV	ra1ra2	1	1/5	$(r_{a1})\leftarrow (r_{a2})$, load register r_{a1} with contents of r_{a2} , r_{a2} contents remain unchanged.
SHLD	b3b2	3	5/16	$[]\leftarrow(L); [+1)]\leftarrow(H)$, store the contents of H and L into two successive memory locations specified by bytes 3 and 2.
XCHG		1	1/4	(H) \leftrightarrow (D); (L) \leftrightarrow (E), exchange double registers HL and DE
XTHL		1	5/18	(L) \leftrightarrow [(SP)], (H) \leftrightarrow [(SP)+1], (SP)=(SP), exchange the top of the stack with register HL.

2.3 INSTRUCTION SET OPCODES ALPHABETICALLY LISTED

			DECICTED		E-LOGIC PCODE	CLOCK
MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	\D7-D4/	\ D3-D0/	CLOCK
ACI	2	Add to A, immediate value plus carry †	ATTECTED	(<u>D</u> / D -D4)	E	7
ADC M	1	Add to A, specified memory value plus carry		8	E	, 7
ADC r	1	Add to A, specified register value plus carry †	В	8	8	4
	·		C	8	9	·
			D	8	A	
		•	E	8	В	
			н	8	С	
			L	8	D	
			Α	8	F	
ADD M	1	Add to A, specified memory value [†]		8	6	7
ADD r	1	Add to A, specified register value [†]	В	8	0	4
			С	8	1	
			D	8	2	
			E	8	3	
			н	8	4	
			L	8	5	
			Α	8	7	
ADI	2	Add to A, immediate value [†]		С	6	7
M ANA	1	Logical AND with A, specified memory value [†]		Α	6	7
ANAr	1	Logical AND with A, specified register value [†]	В	Α	0	4
			С	Α	1	
			D .	А	2	
			E	Α	3	
			Н	Α	4	
			L	Α	5	
			Α	Α	7	
ANI	2	Logical AND with A, immediate value [†]		E	6	7
CALL	3	Unconditional call		С	D	17
cc	3	Call if C flag true		D	С	11/17
CM	3	Call if S flag true		F	С	11/17
CMA	1	Logically invert A		2	F	4
CMC	1	Logically invert C flag‡		3	F	4
CMP M	1	Compare with A, specified memory value [†]		В	. Е	7
CMP r	. 1	Compare with A, specified register value				
			В	В	8 .	4
		•	С	В	9	
			D	В	Α	
			E	В	В	
			Н	В	С	
			L	В	D	
			Α	В	F	
CNC	3	Call if C flag false		D	4	11/17
CNZ	3	Call if Z flag false		С	4	11/17
CP .	3	Call if S flag false		F	4	11/17
CPE	3	Call if P flag true (even parity)		E	С	11/17
CPI	2	Compare with A, immediate value [†]		F	E	7
CPO	3	Call if P flag false (odd parity)		E	4	11/17
CZ	3	Call if Z flag true		С	С	11/17
DAA	1	Decimal convert A value [†]		2	7	4

 $^{^{\}bullet}$ Two possible cycle times (11/17) indicate instruction cycles dependent on condition flags. $^{\uparrow}$ All flags (C, Z, S, P, C1) affected. ‡ Only carry flag affected.

				POSITIV	E-LOGIC	
			REGISTER	HEX O	PCODE	CLOCK
MNEMONIC	BYTES	DESCRIPTION	A FECTED	D7-D4	_D3-D0	CYCLES
DAD B	1	16-bit add, BC to HL‡		0	9	10
DAD D	1	16-bit add, DE to HL‡		1	9	10
DAD H	1,	16-bit add, HL to HL‡		2	9	10
DAD SP	1	16-bit add, SP to HL [‡]		3	9	10
DCR M	1	Subtract 1 from specified memory value §		3	5	10
DCR r	1	Subtract 1 from specified register value §	. в	0	5	5
			C	0	D	
			. D	1	5	
			E	1	D	
			. н	2	5	
			L	· 2	D	
			A	3	D	
DCX B	1	Subtract 1 from double register BC		0	В	5
DCX D	1	Subtract 1 from double register DE		1	В	5
DCX H	1	Subtract 1 from double register HL		2	В	5
DCX SP	1	Subtract 1 from stack pointer		3	В	5
DI	1	Disable interrupt input		F	3	4
EI	1	Enable interrupt input		F ·	В	4
HLT	1	Halt until interrupted		7	6	7
IN .	2	Input data to A		, D	В	10
INRM	1	Add 1 to specified memory value §		3	4	10
INR r	1	Add 1 to specified register value §	В	0	4	5
	•	Add 1 to specified register values	C	0	c	3
			D	1	4	
			E	1	C	
			Н	2	4	
			L	2	C	
			A	3	c	
INX B	1	Add 1 to double register BC	^	0	3	5
INX D	1	Add 1 to double register DE		. 1	3	5
INX H	1	Add 1 to double register HL		2	3	5
INX SP	1	Add 1 to SP		3	3	5
JC	3	Jump if C flag true		D	. A	10
JM	3	Jump if S flag true		F	· A	10
		Unconditional jump		c	3	10
JMP	3	Jump if C flag false			ა 2	
JNC	3	Jump if Z flag false		D		10
JNZ	3	Jump if S flag false		C F	2 2	10
JP	3	Jump if P flag true				10
JPE	3	Jump if P falg false		E	A	10
JPO	3	· •		E	2	10
JZ	3	Jump if Z flag true		С	A	10
LDA	1	Load A using direct address		3	A	13
LDAX B	1	Load A using indirect address (BC)		0	A	7
LDAX D	1	Load Al using indirect address (DE)		1	A	7
LHLD	3	Load HL using direct address		2	A	16
LXIB	3	Load BC with immediate value		0	1	10
LXID	3	Load DE with immediate value		1	1	10
LXIH	3	Load HL with immediate value		2	1	10
LXI SP	3	Load SP with immediate value		3	1	10

 $[\]overset{\ddagger}{\$}$ Only carry flag affected. $\overset{\$}{\$}$ All flags except carry affected.

				POSITIVE LOGIC				
			REGISTER	HEX O	PCODE	CLOCK		
MNEMONIC	BYTES	DESCRIPTION	AFFECTED	\D7-D4	\D3-D0	CYCLES		
MOV M,r	1	Move register value to memory	В	•	•	7		
			C	7	1			
			D	7	2			
			E	7	3			
			н	7	4			
			L	7	5			
			Α	7	7			
MOV r,M	1	Move memory value to register	В	4	6	7		
			C	4	E			
			D	5	6			
			E	5	E			
			н	6	6			
			REGISTER HEX OPCODE CLOCK ON AFFECTED D7—D4 D3—D0 CYCL Emory B 7 0 7 C 7 1 D 7 2 E 7 3 H 7 4 L 7 5 A 7 7 C 4 E D 5 6 E 5 E H 6 6 L 6 E A 7 E					
•			DESCRIPTION AFFECTED D7—D4 D3—D0 egister value to memory B 7 0 C 7 1 D 7 2 E 7 3 H 7 4 4 1 4 1 4 1 4 6 8 7 7 7 7 7 8 8 4	E				
$MOV r_1, r_2$	1	Move memory value to register Move register value to register	В,В	4	0	5		
	Myr 1 Move register value to memory Myr 1 Move memory value to register Move register value to register	В,С	4	1				
				4	2			
		•	B,E	4	3			
			в,н	4	4			
			B,L	4	5			
				4				
				4	8			
				4				
				4				
				4	С			
			L,D	U	O			

			REGISTER		E-LOGIC PCODE	CLOCK
MNEMONIC	BYTES	DESCRIPTION	AFFECTED	\D7-D4/	\ <u>D3</u> - <u>D0</u> /	CYCLES*
MOV r ₁ , r ₂	1	Move register value to register (continued)	L,C	—	9	
			L,D	6	A	
			L,E	6	В	
			L,H	6	C	
			L,L	6	D	
			L,A	6	F	
			A,B	7	8	
			A,C	7	9	
			A,D	7	Α	
			A,E	7	В	
			A,H	7	С	
			A,L	7	D	
			A,A	7	F	
MVIM	2	Move immediate value to memory	·	3	6	10
MVIr	2	Move immediate value to register	В	0	6	7
		-	С	0	E	
			D	1	6	
			E	1	E	
			H	2	6	
			L	2	E	
			A	3	E	
NOP [*]	1	4-clock-cycle delay	4	0	0	4
ORA M	1	Inclusive OR with A, specified memory value †	•	В	6	7
ORA r	1	Inclusive OR with A, specified register value [†]	В	В	0	4
011717	•	The second of th	c	В	1	•
			D	В	2	
			E	В	3	
			Н	В	4	
			L.	В	5	
			A	В	7	
ORI	2	Inclusive OR with A, immediate value [†]		F	6	7
OUT	2	Output data from accumulator		D	3	10
PCHL	1	Move HL to PC		E	9	5
POP B	1	Load BC from stack		C	1	10
POP D	1	Load DE from stack		D	1	10
POP H	1	Load HL from stack		E	1	10
POP PSW	1	Load AF from stack [†]		F	1	10
PUSH B	1	Move BC to stack		C	5	11
PUSH D	1	Move DE to stack		D	5	11
PUSH H	2	Move HL to stack		E	5	11
PUSH PSW	1	Move AF to stack		F	5	11
RAL	1	Left rotate A value through C flag‡		1	7	4
RAR	1	Right rotate A value through C flag‡		1	, F	4
RC	1	Return if C flag true		D	8	5/11
RET	1	Unconditional return		С	9	10
RLC	1	Left rotate A value [‡]		0	7	4
RM	1	Return if S flag true		F	8	5/11
RNC	1	Return if C flag false		D	0	5/11
RNZ	1	Return if Z flag false		С	0	5/11
RP	1	Return if S flag false		F	0	5/11
*	•			•	•	3/ 1 1

^{*}Two possible cycles times (11/17) indicate instruction cycles dependent on condition flags. † All flags (C, Z, S, P, C1) affected. ‡ Only carry flag affected.

			REGISTER		E-LOGIC PCODE	СГОСК
MNEMONIC	BYTE	S <u>DESCRIPTION</u>	AFFECTED	\D7-D4/	\D3-D0	CYCLES*
RPE	1	Return if P flag true		Ē	8	5/11
RPO	1	Return if P flag false		E	0	5/11
RRC	1	Right rotate A value ‡		0	F	4
RST	, 1	1-byte call (restart)				11
			PC←0000 ₁₆	С	7	
			PC←0008 ₁₆	С	F	
			PC←0010 ₁₆	D	7	
		•	PC←0018 ₁₆	D	F	
			PC←0020 ₁₆	Ε	7	
			PC←0028 ₁₆	Ε	F	
			PC←0030 ₁₆	F	7	
			PC←0038 ₁₆	F	F	
RZ	1	Return if Z flag true		С	8	5/11
SBB M	1	Subtract from A, specified memory value plus borrow †		9	E	7
SBB r	1	Subtract from A, specified register value plus borrow [†]	В	9	8	4
			С	9	9	
			D	9	Α	
			Ε	9	В	
			н	9	С	
			L	9	D	
			Α	9	F	
SBI	2	Subtract from A, immediate value plus borrow [†]		D	E	7
SHLD	3	Store HL value at direct address		2	2	16
SPHL	1	Move HL value to SP		F	9 .	5
STA	3	Store A value at direct address		3	2	13
STAX B	1	Store A value at indirect address (BC)		0	2	7
STAX D	1	Store A value at indirect address (DE)		1	2	7
STC	1	Set C flag true‡		3	7	4
SUB M	1	Subtract from A, specified memory value [†]		9	6	7
SUB r	1	Subtract from A, specified register value [†]	В	9	0	4
1			С	9	1	
			D	9	2	
			E	9	3	
			н	9 .	4	
			L	9	5	
			Α	9	7	
SUI	2	Subtract from A, immediate value [†]		D	6	7
XCHG	1	Exchange contents of HL with DE		Ε	В	4
XRAM	1	Exclusive OR with A, specified memory value [†]		Α	E	7
XRA r	1	Exclusive OR with A, specified register value [†]	В	Α	8	4
			С	Α	9	
			D	Α	Α	
			Ε	Α	В	
			н	Α	С	
	•		L	Α	D	
			Α	A	F	
XRI	2	Exclusive OR with A, immediate value [†]		Ε	E	7
XTHL	1	Exchange contents of HL with top of stack		E	3	18

^{*}Two possible cycles times (11/17) indicate instruction cycles dependent on condition flags. † All flags (C, Z, S, P, C1) affected. ‡ Only carry flag affected.

3. TMS 8080A ELECTRICAL AND MECHANICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIL TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V _{CC} (see Note 1)	
Supply voltage, VDD (see Note 1	$-0.3~V$ to 20 V
Supply voltage, VSS (see Note 1)	$-0.3~V$ to 20 V
All input and output voltages (see Note 1)	$-0.3~V$ to $20~V$
Continuous power dissipation	
Operating free-air temperature range	
Storage temperature range	-65° C to 150° C

^{*}Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V _{BB}	-4.75	-5	-5.25	V
Supply voltage, V _{CC}	4.75	5	5.25	V
Supply voltage, V _{DD}	11.4	12	12.6	V
Supply voltage, VSS		0		V
High-level input voltage, V _{IH} (all inputs except clocks) (see Note 2)	3.3		V _{CC} +1	V
High-level clock input voltage, V _{IH} (φ)	9		$V_{DD}+1$	V
Low-level input voltage, V _{IL} (all inputs except clocks) (see Note 3)	-1		8.0	V
Low-level clock input voltage, V _{IL(φ)} (see Note 3)	-1		0.8	V
Operating free-air temperature, TA	0		70	C

3.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

	PARAMETER	TEST CONDITIONS	MIN TYP	† MAX	UNIT
11	Input current (any input except clocks and data bus)	V ₁ = 0 V to V _{CC}		± 10	μА
$^{1}I(\phi)$	Clock input current	$V_{I(\phi)} = 0 V \text{ to } V_{DD}$		± 10	μА
II(DB)	Input current, data bus	VI(DB) = 0 V to VCC		-100	μА
1.0 0	Address or data bus input	VI(ad) or VI(DB) = VCC		10	μА
¹ I(hold)	current during hold	$V_{I(ad)}$ or $V_{I(DB)} = 0$ V		-100	1 "
VoH	High-level output voltage	ΙΟΗ = 150 μΑ	3.7		V
VOL	Low-level output voltage	I _{OL} = 1.9 mA		0.45 V	
IBB(av)	Average supply current from VBB	100	-0.01	-1	
ICC(av)	Average supply current from VCC	Operating at $t_{c(\phi)} = 480 \text{ ns}$,	60	80	mA
IDD(av)	Average supply current from V _{DD}	T _A = 25°C	50	75	1
Ci	Capacitance, any input except clock	$V_{CC} = V_{DD} = V_{SS} = 0 V$	10) 20	
$C_{i(\phi)}$	Clock input capacitance	$V_{BB} = -4.75$ to -5.25 V, f = 1 MHz,	19	5 25	pF
Со	Output capacitance	All other pins at 0 V	10	20	1

 $^{^{\}dagger}$ All typical values are at T $_{\Delta}$ = 25 $^{\prime}$ C and nominal voltages.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the normally most negative supply voltage, V_{BB} (substrate).

Throughout the remainder of this data sheet, voltage values are with respect to V_{SS} unless otherwise noted.

NOTES: 2. Active pull-up resistors of nominally 2 $k\Omega$ will be switched onto the data bus when DBIN is high and the data input voltage is more positive than V_{1H} min.

^{3.} The algebraic convention where the most negative limit is designated as minimum is used in this specification for logic voltage levels only.

3.4 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURE 2)

	·	MIN	MAX	UNIT
t _C (φ)	Clock cycle time (see Note 5)	480	2000	ns
^t r(φ)	Clock rise time	5	50	ns
t _f (φ)	Clock fall time	5	50	ns
^t w(φ1)	Pulse width, clock 1 high	60		ns
^t w(φ2)	Pulse width, clock 2 high	220		ns
^t d(φ1L-φ2)	Delay time, clock 1 low to clock 2	0		ns
^t d(φ2-φ1)	Delay time, clock 2 to clock 1	70		ns
^t d(φ1H-φ2)	Delay time, clock 1 high to clock 2 (time between leading edges)	80		ns
t _{su} (da-φ1)	Data setup time with respect to clock 1	30		ns
^t su(da-φ2)	Data setup time with respect to clock 2	150		ns
t _{su} (hold)	Hold input setup time	140		ns
t _{su(int)}	Interrupt input setup time	120		ns
t _{su(rdy)}	Ready input setup time	120		ns
^t h(da)	Data hold time (see Note 6)	tPD(I	DBI)	ns
th(hold)	Hold input hold time	0		ns
th(int)	Interrupt input hold time	0		ns
th(rdy)	Ready input hold time	0		ns

NOTES: 5. $t_{C(\phi)} = t_{d(\phi_1 L, \phi_2)} + t_{r(\phi_2)} + t_{r(\phi_2)} + t_{d(\phi_2 - \phi_1)} + t_{r(\phi_1)}$. 480 ns $\leq t_{C(\phi)} \leq$ 2000 ns.

6. The data input should be enabled using the DBIN status signal. No bus conflict can then occur and the data hold time requirement is thus assured.

3.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURE 2)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
^t PD(ad)	Propagation delay time, clock 2 to address outputs			200	ns
^t PD(da)	Propagation delay time, clock 2 to data bus	C ₁ = 100 pF,		220	ns
tPD(cont)	Propagation delay time, clocks to control outputs	$R_1 = 1.3 k\Omega$		120	ns
tPD(DBI)	Propagation delay time, clock 2 to DBIN output		25	140	ns
^t PD(int)	Propagation delay time, clock 2 to INTE output			200	ns
^t DI	Time for data bus to enter input mode		tpi	D(DBI)	ns
^t PXZ	Disable time to high-impedance state			120	ns
	during hold (address outputs and data bus)			120	115

The time that the address outputs and output data will remain stable after \overline{WR} goes high, t_{WA} and $t_{WD} \ge t_{d}(\phi 1H.\phi 2)$

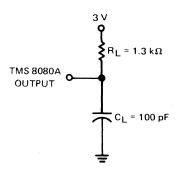
The time between address outputs becoming stable and WR going low, $t_{AW} \le 2 t_{c(\phi)} - t_{d(\phi)} + t_{f(\phi)} - 120 \text{ ns.}$

The time between output data becoming stable and \overline{WR} going low, $t_{DW} \ge t_{c(\phi)} - t_{d(\phi)H - \phi2)} - t_{r(\phi)} - 150$ ns.

The following are relevant when interfacing to devices requiring $V_{\mbox{\scriptsize IH}}$ min of 3.3 V:

a) Maximum output rise time (t_{TLH}) from 0.8 V to 3.3 V is 140 ns with C_L as specified for the propagation delay times above.

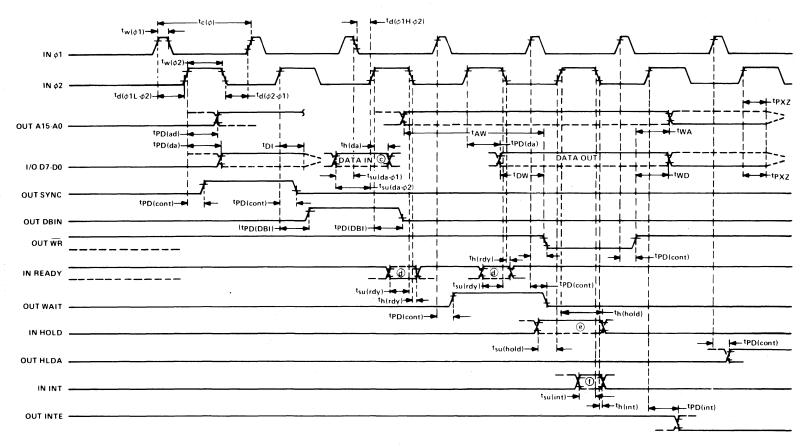
Maximum propagation delay times when measured to $V_{ref(H)} = 3 V$ (instead of 2 V) will be 60 ns more than as specified above with C_L as specified.



 C_{\perp} includes probe and jig capacitance.

LOAD CIRCUIT

voltage waveforms (see notes a and b)



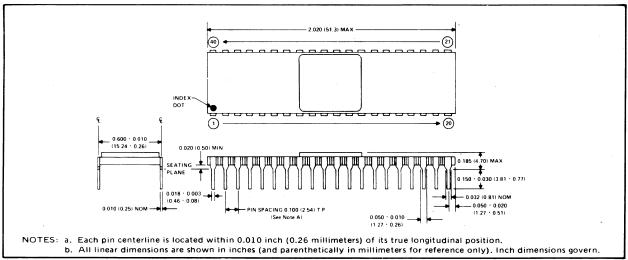
- NOTES: a. This timing diagram shows timing relationships only, it does not represent any specific machine cycle.
 - b. Time measurements are made at the following reference voltages: Clock, $V_{ref(H)} = 9.5 \text{ V}$, $V_{ref(L)} = 1 \text{ V}$. Other inputs, $V_{ref(H)} = 2 \text{ V}$, $V_{ref(L)} = 0.8 \text{ V}$.
 - c. Data in must be stable for this period when DBIN is high during S3. Requirements for both $t_{su(da-\phi1)}$ and $t_{su(da-\phi2)}$ must be satisfied.
 - d. The ready signal must be stable for this period during \$2 or \$W. This requires external synchronization.
 - e. The hold signal must be stable for this period during S2 or SW when entering the hold mode and during S3, S4, S5 and SWH when in the hold mode. This requires external synchronization.
 - f. The interrupt signal must be stable during this period on the last clock cycle of any instruction to be recognized on the following instruction. External synchronization is not required.

3.6 TERMINAL ASSIGNMENTS

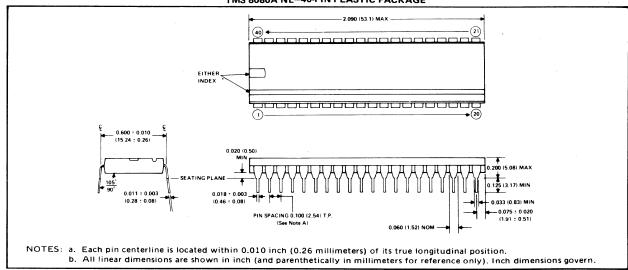
TMS 8080A								
A 10	1	40	A11					
VSS	2	39	A14					
D4	3	38	A13					
D5	4	37	A12					
D6	5	36	A15					
D7	6	35	A9					
D3	7	34	A8					
D2	8	33	A7					
D1	9	32	A6					
D0	10	31	A5					
VBB	11	30	A4					
RESET	12	29	A3					
HOLD	13	28	V_{DD}					
INT	14	27	A2 '					
φ 2	15	26	A1					
INTE	16	25	Α0					
DBIN	17	24	WAIT					
WR	18	23	READY					
SYNC	19	22	01					
vcc	20	21	HLDA					

3.7 MECHANICAL DATA

TMS 8080A JL-40-PIN CERAMIC PACKAGE







Appendix B

5504 Multifunction I/O Controller Data Manuals

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TMS 5504 MULTIFUNCTION INPUT/OUTPUT CONTROLLER

1. INTRODUCTION

1.1 DESCRIPTION

The TMS 5504 is a multifunction input/output circuit for use with TI's TMS 8080A CPU. It is fabricated with the same N-channel silicon-gate process as the TMS 8080A and has compatible timing, signal levels, and power supply requirements. The TMS 5504 provides a TMS 8080A microprocessor system with an asynchronous communications interface, data I/O buffers, interrupt control logic, and interval timers.

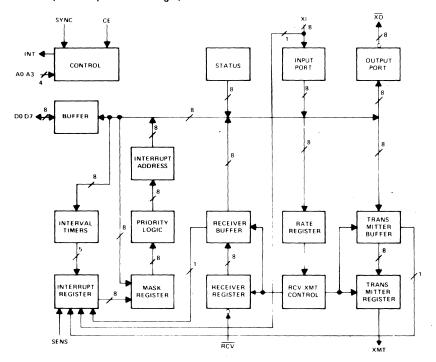


FIGURE 1-TMS 5504 BLOCK DIAGRAM

The I/O section of the TMS 5504 contains an eight-bit parallel input port and a separate eight-bit parallel output port with storage register. Five programmable interval timers provide time intervals from 64 μ s to 16.32 ms.

The interrupt system allows the processor to effectively communicate with the interval timers, external signals, and the communications interface by providing TMS 8080A-compatible interrupt logic with masking capability.

Data transfers between the TMS 5504 and the CPU are carried by the data bus and controlled by the interrupt, chip enable, sync, and address lines. The TMS 8080A uses four of its memory-address lines to select one of 14 commands to which the TMS 5504 will respond. These commands allow the CPU to:

- --- read the receiver buffer
- --- read the input port
- --- read the interrupt address
- --- read TMS 5504 status
- --- issue discrete commands
- --- load baud rate register
- --- load the transmitter buffer
- --- load the output port
- --- load the mask register
- --- load an interval timer

The commands are generated by executing memory referencing instructions such as MOV (register to memory) with the memory address being the **TMS 5504** command. This provides a high degree of flexibility for I/O operations by letting the systems programmer use a variety of instructions.

1.2 SUMMARY OF OPERATION

Addressing the TMS 5504

A convenient method for addressing the TMS 5504 is to tie the chip enable input to the highest order address line of the CPU's 16-bit address bus and the four TMS 5504 address inputs to the four lowest order bits of the bus. This, of course, limits the system to 32,768 words of memory but in many applications the full 65,536 word memory addressing capability of the TMS 8080A is not required.

Communications Functions

The communications section of the TMS 5504 is an asynchronous transmitter and receiver for serial communications and provides the following functions:

Programmable baud rate - A CPU command selects a baud rate of 200, 600, 300, 1200, 2400, or 9600 baud.

Incoming character detection — The receiver detects the start and stop bits of an incoming character and places the character in the receive buffer.

Character transmission — The transmitter generates start and stop bits for a character received from the CPU and shifts it out.

Status and command signals — Via the data bus, the **TMS 5504** signals the status of: framing error and overrun error flags; data in the receiver and transmitter buffers; start and data bit detectors; and end-of-transmission (break) signals from external equipment. It also issues break signals to external equipment.

Data Interface

The TMS 5504 moves data between the CPU and external devices through its internal data bus, input port, and output port. When data is present on the bus that is to be sent to an external device, a Load Output Port (LOP) command from the CPU puts the data on the $\overline{\text{XO}}$ pins of the TMS 5504 by latching it in the output port. The data remains in the port until another LOP command is received. When the CPU requires data that is present on the External Input (XI) lines, it issues a command that gates the data onto the internal data bus of the TMS 5504 and consequently onto the CPU's data bus at the correct time during the CPU cycles.

Interval Timers

To start a countdown by any of the five interval timers, the program selects the particular timer by an address to the TMS 5504 and loads the required interval into the timer via the data bus. Loading the timer activates it and it counts down in increments of 64 microseconds. The 8-bit counters provide intervals that vary in duration from 64 to 16,320 microseconds. Much longer intervals can be generated by cascading the timers through software. When a timer reaches zero, it generates an interrupt that typically will be used to point to a subroutine that performs a servicing function such as polling a peripheral or scanning a keyboard. Loading an interval value of zero causes an immediate interrupt. A new value loaded while the interval timer is counting overrides the previous value and the interval timer starts counting down the new interval. When an interval timer reaches zero it remains inactive until a new interval is loaded.

Servicing Interrupts

The TMS 5504 provides a TMS 8080A system with several interrupt control functions by receiving external interrupt signals, generating interrupt signals, masking out undesired interrupts, establishing the priority of interrupts, and generating RST instructions for the TMS 8080A. An external interrupt is received on pin 22, SENS. An additional external interrupt can be received on pin 32, X17, if selected by a discrete command from the TMS 8080* (See Figure 4). The TMS 5504 generates an interrupt when any of the five interval timers count to zero. Interrupts are also generated when the receiver buffer is loaded and when the transmitter buffer is empty.

When an interrupt signal is received by the interrupt register from a particular source, a corresponding bit is set and gated to the mask register. A pattern will have previously been set in the mask register by a load-mask-register command from the TMS 8080A. This pattern determines which interrupts will pass through to the priority logic. The priority logic allows an interrupt to generate an RST instruction to the TMS 8080A only if there is no higher priority interrupt that has not been accepted by the TMS 8080A. The TMS 5504 prioritizes interrupts in the order shown below:

1st — Interval Timer #1

2nd — Interval Timer #2

3rd — External Sensor

4th — Interval Timer #3

5th - Receiver Buffer Loaded

6th - Transmitter Buffer Emptied

7th - Interval Timer #4

8th - Interval Timer #5 or an External Input (XI 7)

The highest priority interrupt passes through to the interrupt address logic, which generates the RST instruction to be read by the TMS 8080A. See Table 3 for relationship of interrupt sources to RST instructions and Figures 6 and 8 for timing relationships.

The TMS 5504 provides two methods of servicing interrupts; and interrupt-driven system or a polled-interrupt system. In an interrupt-driven system, the INT signal of the TMS 5504 is tied to the INT input of the TMS 8080A. The sequence of events will be: (1) The TMS 5504 receives (or generates) an interrupt signal and readies the appropriate RST instruction. (2) the TMS 5504 INT output, tied to the TMS 8080 INT input, goes high signaling the TMS 8080A that an interrupt has occurred. (3) If the TMS 8080A is enabled to accept interrupts, it sets the INTA (interrupt acknowledge) status bit high at SYNC time of the next machine cycle. (4) If the TMS 5504 has previously received an interrupt-acknowledge-enable command from the CPU (see Bit 3, Paragraph 2.2.5), the RST instruction is transferred to the data bus.

In a polled-interrupt system, INT is not used and the sequence of events will be: (1) The TMS 5504 receives (or generates) an interrupt and readies the RST instruction. (2) The TMS 5504 interrupt-pending status bit (see Bit 5, Paragraph 2.2.4) is set high (the interrupt-pending status bit and the INT output go high simultaneously). (3) At the prescribed time, the TMS 8080A polls the TMS 5504 to see if an interrupt has occurred by issuing a read-TMS 5504 status command and reading the interrupt-pending bit. (4) If the bit is high, the TMS 8080A will then issue a read-interrupt-address command, which causes the TMS 5504 to transfer the RST instruction to the data bus as data for the instruction being executed by the TMS 8080A.

1.3 APPLICATIONS

Communications Terminals

The functions of the TMS 5504 make it particularly useful in TMS 8080A-based communications terminals and generally applicable in systems requiring periodic or random servicing of interrupts, generation of control signals to external devices, buffering of data, and transmission and reception of asynchronous serial data. As an example, a system configuration such as shown in Figure 2 can function as the controller for a terminal that governs employee entrance into a plant or security areas within a plant. Each terminal is identified by a central computer through ID switches. The central system supplies each terminal's RAM with up to 16 employee access categories applicable to that terminal. These categories are compared with an employee's badge character when he inserts his badge into the badge sensor. If a

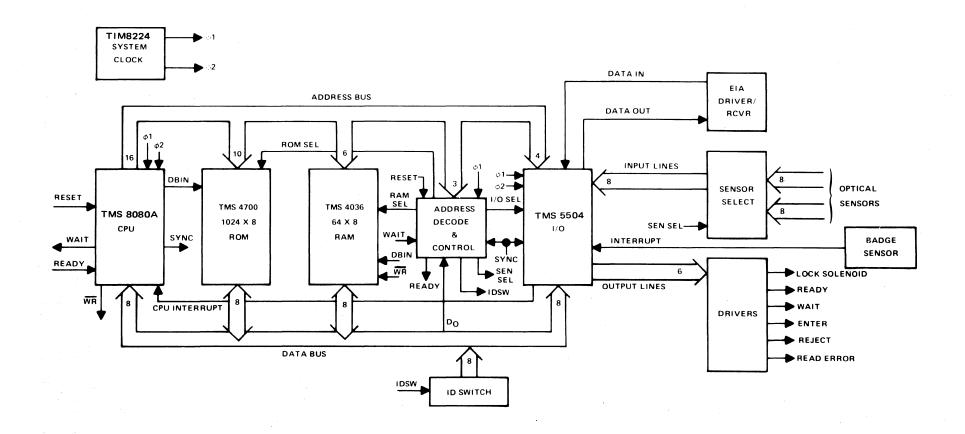


FIGURE 2-ACCESS CONTROL SYSTEM BLOCK DIAGRAM

match is not found, a reject light will be activated. If a match is found, the terminal will transmit the employee's badge number and access category to the central system, and a door unlock solenoid will be activated for 4 seconds. The central computer then may take the transmitted information and record it along with time and date of access.

The TMS 4700 is a 1024×8 ROM that contains the system program, and the TMS 4036 is a 64×8 RAM that serves as the stack for the TMS 8080A and storage for the access category information. TTL circuits control chip-enable information carried by the address bus. Signals from the CPU gate the address bits from the ROM, the RAM, or the TMS 5504 onto the data bus at the correct time in the CPU cycle. The clock generator needed to maintain accurate serial data assembly and disassembly with the central computer.

The TMS 5504 handles the asynchronous serial communication between the TMS 8080A may consist of four TTL circuits or one TIM 8224 along with a crystal and the central system and gates data from the badge reader onto the data bus. It also gates control and status data from the TMS 8080A to the door lock and badge reader and controls the time that the door lock remains open. The TMS 5504 signals the TMS 8080A when the badge reader or the communication lines need service. The functions that the TMS 5504 is to perform are selected by an address from the TMS 8080A with the highest order address line tied to the TMS 5504 chip enable input and the four lowest order lines tied to the address inputs.

2. OPERATIONAL AND FUNCTIONAL DESCRIPTION

This detailed description of the TMS 5504 consists of:

INTERFACE SIGNALS - a definition of each of the circuit's external connections

COMMANDS — the address required to select each of the TMS 5504 commands and a description of the response to the command.

2.1 INTERFACE SIGNALS

The TMS 5504 communicates with the TMS 8080A via four address lines: a chip enable line, an eight-bit bidirectional data bus, an interrupt line, and a sync line. It communicates with system components other than the CPU via eight external inputs, eight external outputs, a serial receiver input, a serial transmitter output, and an external sensor input. Table 1 defines the TMS 5504 pin assignments and describes the function of each pin.

TABLE 1
TMS 5501 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	DESCRIPTION INPUTS
CE	18	Chip enable—When CE is low, the TMS 5504 address decoding is inhibited, which prevents execution of any of the TMS 5504 commands.
A3	17	Address bus-A3 through A0 are the lines that are addressed by the TMS 8080A to select a
A2	16	particular TMS 5504 function.
A1	15	
A0	14	
SYNC	19	Synchronizing signal— The SYNC signal is issued by the TMS 8080A and indicates the beginning of a machine cycle and availability of machine status. When the SYNC signal is active (high), the TMS 5504 will monitor the data bus bits DO (interrupt acknowledge) and D1 (WO, data output function).
RCV	5	Receiver serial data input line—RCV must be held in the inactive (high) state when not receiving data. A transition from high to low will activate the receive circuitry.

TABLE 1 (continued) TMS 5504 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	DESCRIPTION INPUTS
XI O	39	External inputs—These eight external inputs are gated to the data bus when the read-external-inputs
XI 1	38	function is addressed. External input n is gated to data bus bit n without conversion.
XI 2	37	
XI 3	36	
XI 4	35	
XI 5	34	
XI 6	33	
XI 7	32	
SENS	22	External interrupt sensing $-$ A transition from low to high at SENS sets a bit in the interrupt register, which, if enabled, generates an interrupt to the TMS 8080A.
		OUTPUTS
XO 0	24	External outputs—These eight external outputs are driven by the complement of the output
XO 1	25	register; i.e., if output register bit n is loaded with a high (low) from data bus bit n by a load-
XO 2	26	output register command, the external output n will be a low (high). The external outputs change
XO 3	27	only when a load-output-register function is addressed.
XO 4	28	
XO 5	29	
XO 6	30	
XO 7	31	
XMT	40	Transmitter serial data output line—This line remains high when the TMS 5504 is not transmitting.
		DATA BUS INPUT/OUTPUT
D0	13	Data bus - Data transfers between the TMS 5504 and the TMS 8080A are made via the 8-bit
D1	12	bidirectional data bus. D0 is the LSB. D7 is the MSB.
D2	11	
D3	10	
D4	9	
D5	8	
D6	. 7	
D7	6	
INT	23	Interrupt—When active (high), the INT output indicates that at least one of the interrupt conditions has occurred and that its corresponding mask-register bit is set.
		POWER AND CLOCKS
V_{SS}	4	Ground reference
V _{BB}	1	Supply voltage (-5 V nominal)
VCC	2	Supply voltage (5 V nominal)
V _{DD}	3	Supply voltage (12 V nominal)
φ1	20	Phase 1 clock
φ2	21	Phase 2 clock

2.2 TMS 5504 COMMANDS

The TMS 5504 operates as memory device for the TMS 8080A. Functions are initiated via the TMS 8080A address bus and the TMS 5504 address inputs. Address decoding to determine the command function being issued is defined in Table 2.

TABLE 2
COMMAND ADDRESS DECODING
When Chip Enable Is High

	timen emp emane to mg.								
А3	A2	Α1	Α0	COMMAND	FUNCTION	PARAGRAPH			
L	L	L	L	Read receiver buffer	RBn → Dn	2.2.1			
L	L	L	Н	Read external inputs	XIn → Dn	2.2.2			
L	L	Н	L	Read interrupt address	$RST \rightarrow Dn$	2.2.3			
L	L	Н	Н	Read TMS 5504 status	$(Status) \rightarrow Dn$	2.2.4			
L	Н	L	L	Issue discrete commands	See Figure 4	2.2.5			
L	Н	L	Н	Load rate register	See Figure 4	2.2.6			
L	Н	Н	L	Load transmitter buffer	Dn → TBn	2.2.7			
L	Н	Н	Н	Load output port	$Dn \rightarrow \overline{XO}n$	2.2.8			
Н	L	L	L	Load mask register	$Dn \rightarrow MRn$	2.2.9			
Н	L	L	Н	Load interval timer 1	$Dn \rightarrow Timer 1$	2.2.10			
Н	L	Н	L	Load interval timer 2	Dn → Timer 2	2.2.10			
Н	L	Н	Н	Load interval timer 3	$Dn \rightarrow Timer 3$	2.2.10			
Н	Н	L	L	Load interval timer 4	Dn → Timer 4	2.2.10			
Н	Н	L.	Н	Load interval timer 5	Dn → Timer 5	2.2.10			
Н	Н	Н	L	No function					
Н	Н	Н	Н	No function					

RBn Receiver buffer bit n

Dn Data bus I/O terminal n

XIn External input terminal n

RST $11 (IA_2) (IA_1) (IA_0) 1 1 1 (see Table 3)$

TBn Transmit buffer bit n XOn Output register bit n MRn Mask register bit n

TABLE 3
RST INSTRUCTIONS

DATA BUS BIT								INTERRUPT CAUSED BY	
0	1	2	3	4	5	6	7	INTERROFT CAUSED BY	
Н	Н	Н	L	L	L	Н	Н	Interval Timer 1	
Н	Н	Н	Н	L	L	Н	Н	Interval Timer 2	
Н	Н	Н	L	Н	L	Н	Н	External Sensor	
Н	Н	Н	Н	Н	L	Н	Н	Interval Timer 3	
Н	Н	Н	L	L	Н	Н	Н	Receiver Buffer	
Н	Н	$\mathbf{H}_{\mathbf{r}}$	Н	L	Н	Н	Н	Transmitter Buffer	
Н	Н	Н	L	Н	Н	Н	Н	Interval Timer 4	
Н	Н	Н	Н	Н	Н	Н	Н	Interval Timer 5 or X17	

The following paragraphs define the functions of the TMS 5504 commands.

2.2.1 Read receiver buffer

Addressing the read-receiver-buffer function causes the receiver buffer contents to be transferred to the TMS 8080A and clears the receiver-buffer-loaded flag.

2.2.2 Read external input lines

Addressing the read-external inputs function transfers the states of the eight external input lines to the TMS 8080A.

2.2.3 Read interrupt address

Addressing the read interrupt address function transfers the current highest priority interrupt address onto the data bus as read data. After the read operation is completed, the corresponding bit in the interrupt register is reset.

If the read-interrupt-address function is addressed when there is no interrupt pending, a false interrupt address will be read. TMS 5504 status function should be addressed in order to determine whether or not an interrupt condition is pending.

2.2.4 Read TMS 5504 status

Addressing the read-TMS 5504-status function gates the various status conditions of the TMS 5504 onto the data bus. The status conditions, available as indicated in Figure 3, are described in the following paragraphs.

BIT:	7	6	5	4	3	2	1	0
	START	FULL	INTRPT	XMIT	RCV	SERIAL	OVERRUN	FRAME
	BIT	BIT	PENDING	BUFFER	BUFFER	RCVD	ERROR	ERROR
	DETECT	DETECT		EMPTY	LOADED			

FIGURE 3-DATA BUS ASSIGNMENTS FOR TMS 5504 STATUS

Bit 0, framing error

A high in bit 0 indicates that a framing error was detected on the last character received (either one or both stop bits were in error). The framing error flag is updated at the end of each character. Bit 0 of the TMS 5504 status will remain high until the next valid character is received.

Bit 1, overrun error

A high in bit 1 indicates that a new character was loaded into the receiver buffer before a previous character was read out. The overrun error flag is cleared each time the read-I/O-status function is addressed or a reset command is issued.

Bit 2, serial received data

Bit 2 monitors the receiver serial data input line. This line is provided as a status input for use in detecting a break and for test purposes. Bit 2 is normally high when no data is being received.

Bit 3, receiver buffer loaded

A high in bit 3 indicates that the receiver buffer is loaded with a new character. The receiver-buffer-loaded flag remains high until the read-receiver-buffer function is addressed (at which time the flag is cleared). The reset function also clears this flag.

Bit 4, transmitter buffer empty

A high in bit 4 indicates that the transmitter buffer register is empty and ready to accept a character. Note, however, that the serial transmitter register may be in the process of shifting out a character. The reset function sets the transmitter-buffer-empty flag high.

Bit 5, interrupt pending

A high in bit 5 indicates that one or more of the interrupt conditions has occured and the corresponding interrupt is enabled. This bit is the status of the interrupt signal INT.

Bit 6, full bit detected

A high in bit 6 indicates that the first data bit of a receive-data character has been detected. This bit remains high until the entire character has been received or until a reset is issued and is provided for test purposes.

Bit 7, start bit detected

A high in bit 7 indicates that the start bit of an incoming data character has been detected. This bit remains high until the entire character has been received or until a reset is issued and is provided for test purposes.

2.2.5 Issue discrete commands

Addressing the discrete command function causes the **TMS 5504** to interpret the data bus information according to the following descriptions. See Figure 4 for the discrete command format. Bits 1 through 5 are latched until a different discrete command is received.

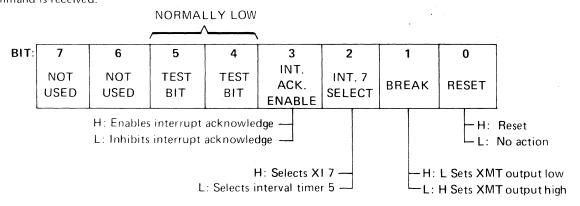


FIGURE 4-DISCRETE COMMAND FORMAT

Bit 0, reset

A high in bit 0 will cause the following:

- 1) The receiver buffer and register are cleared to the search mode including the receiver-buffer-loaded flag, the start-bit-detected flag, the full-bit-detected flag, and the overrun-error flag. The receiver buffer is not cleared and will contain the last character received.
- 2) The transmitter data output is set high (marking). The transmitter-buffer-empty flag is set high indicating that the transmitter buffer is ready to accept a character from the TMS 8080A.
- 3) The interrupt register is cleared except for the bit corresponding to the transmitter buffer interrupt, which is set high.
- 4) The interval timers are inhibited.

A low in bit 0 causes no action. The reset function has no affect on the output port, the external inputs, interrupt acknowledge enable, the mask register, the rate register, the transmitter register, or the transmitter buffer.

Bit 1, break

A low in bit 1 causes the transmitter data output to be reset low (spacing).

If bit 0 and bit 1 are both high, the reset function will override.

Bit 2, interrupt 7 select

Interrupt 7 may be generated either by a low to high transition of external input 7 or by interval timer 5.

A high in bit 2 selects the interrupt 7 source to be the transition of external input 7. A low in bit 2 selects the interrupt 7 source to be interval timer 5.

Bit 3, interrupt acknowledge enable

The TMS 5504 decodes data bus (CPU status) bit 0 at SYNC of each machine cycle to determine if an interrupt acknowledge is being issued.

A high in bit 3 enables the TMS 5504 to accept the interrupt acknowledge decode. A low in bit 3 causes the TMS 5504 to ignore the interrupt acknowledge decode.

Bit 4 and bit 5 are used only during testing of the TMS 5504. For correct system operation both bits must be kept low.

Bit 6 and bit 7 are not used and can assume any value.

2.2.6 Load rate register

Addressing the load-rate-register function causes the TMS 5504 to load the rate register from the data bus and interpret the data bits (See Figure 5) as follows.

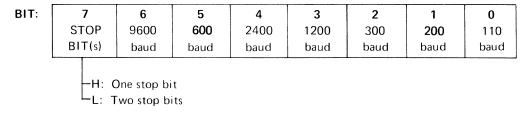


FIGURE 5-DATA BUS ASSIGNMENTS FOR RATE COMMANDS

Bits 0 through 6, rate select

The rate select bits (bits 0 through 6) are mutually exclusive, i.e., only one bit may be high. A high in bits 0 through 6 will select the baud rate for both the transmitter and receiver circuitry as defined below and in Figure 5:

Bit 0	110 baud
Bit 1	200 buad
Bit 2	300 baud
Bit 3	1200 baud
Bit 4	2400 baud
Bit 5	600 baud
Bit 6	9600 baud

If more than one bit is high, the highest rate indicated will result. If bits 0 through 6 are all low, both the receiver and the transmitter circuitry will be inhibited.

Bit 7, stop bits

Bit 7 determines whether one or two stop bits are to be used by both the transmitter and receiver circuitry. A high in bit 7 selects one stop bit. A low in bit 7 selects two stop bits.

2.2.7 Load transmitter buffer

Addressing the load-transmitter-buffer function transfers the state of the data bus into the transmitter buffer.

2.2.8 Load output port

Addressing the <u>load-output-port function</u> transfers the state of the data bus into the output port. The data is latched and remains on \overline{XO} 0 through \overline{XO} 7 as the complement of the data bus until new data is loaded.

2.2.9 Load mask register

Addressing the load-mask-register function loads the contents of the data bus into the mask register. A high in data bus bit n enables interrupt n. A low inhibits the corresponding interrupt.

2.2.10 Load timer n

Addressing the load-timer-n function loads the contents of the data bus into the appropriate interval timer. Time intervals of from 64 μ s (data bus = LLLLLLH) to 16,320 μ s (data bus HHHHHHHH) are counted in 64- μ s, steps. When the count of interval timer n reaches 0, the bit in the interrupt register that corresponds to timer n is set and an interrupt is generated. Loading all lows causes an interrupt immediately.

3. TMS 5504 ELECTRICAL AND MECHANICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, VCC (see Note 1)											$-0.3~\mathrm{V}$ to $20~\mathrm{V}$
Supply voltage, VDD (see Note 1											$-0.3~\mathrm{V}$ to 20 V
Supply voltage, VSS (see Note 1)											 $-0.3~\mathrm{V}$ to $20~\mathrm{V}$
All input and output voltages (see Note 1)											-0.3 V to 20 V
Continuous power dissipation											1.1 W
Operating free-air temperature range											
Storage temperature range											–65°C to 150°C

^{*}Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V _{BB}	Ţ-	-4 .75	5	-5.25	V
Supply voltage, V _{CC}		4.75	5	5.25	V
Supply voltage, V _{DD}		11.4	12	12.6	V
Supply voltage, V _{SS}			0		V
High-level input voltage, VIH (all inputs except clocks)		3.3		V _{CC} +1	V
High-level clock input voltage, $V_{IH(\phi)}$	\	√ _{DD} -1		V _{DD} +1	V
Low-level input voltage, VIL (all inputs except clocks) (see Note 2)		-1		8.0	V
Low-level clock input voltage, $V_{IL(\phi)}$ (see Note 2)		-1		0.6	V
Operating free-air temperature, TA		0		70	°C

NOTE 1: Under absolute maximum ratings voltage values are with respect to the normally most negative supply voltage, V_{BB} (substrate).

Throughout the remainder of this data sheet, voltage values are with respect to V_{SS} unless otherwise noted.

3.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

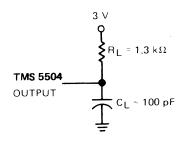
	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
l ₁	Input current (any input except clocks and data bus)	$V_1 = 0 V \text{ to } V_{CC}$		· 10	μА
1 _{1(\phi)}	Clock input current	$V_{I(\phi)} = 0 \text{ V to } V_{DD}$		· 10	μА
II(DB)	Input current, data bus	$V_{I(DB)} = 0 \text{ V to V}_{CC}$, CE at 0 V	-50	100	μА
Vон	High-level output voltage	ΙΟΗ = 400 μΑ	3.7		V
VOL	Low-level output voltage	I _{OL} = 1.7 mA,		0.45	V
IBB(av)	Average supply current from V _{BB}	0.5554		- 1	
CC(av)	Average supply current from VCC	Operating at $t_{c(\varphi)} = 480 \text{ ns}$,		100	mA
IDD(av)	Average supply current from VDD	T _A = 25 C		40	
Ci	Capacitance, any input except clock	$V_{CC} = V_{DD} = V_{SS} = 0 V$		10	
C _{I (\phi)}	Clock input capacitance	$V_{BB} = -4.75 \text{ to } -5.25 \text{ V}, \qquad f = 1 \text{ MHz},$		75	pΕ
Co	Output capacitance	All other pins at 0 V		20	

3.4 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURES 5 AND 6)

		MIN	MAX	UNIT
t _{c(φ)}	Clock cycle time	480	2000	ns
t _r (φ)	Clock rise time	5	50	ns
tf(ø)	Clock fall time	5	50	ns
^t w(φ1)	Pulse width, clock 1 high	60		ns
^t w(⇔2)	Pulse width, clock 2 high	200	300	ns
^t d(φ1L-φ2)	Delay time, clock 1 low to clock 2	0		ns
^t d(φ2-φ1)	Delay time, clock 2 to clock 1	70		ns
^t d(φ1H-φ2)	Delay time, clock 1 high to clock 2 (time between leading edges)	80		ns
t _{su(ad)}	Address setup time	50		ns
t _{su} (CE)	Chip-enable setup time	50		ns
t _{su(da)}	Data setup time	50		ns
t _{su(sync)}	Sync setup time	50		ns
t _{su(XI)}	External input setup time	50		ns
^t h(ad)	Address hold time	0		ns
^t h(CE)	Chip-enable hold time	10		ns
^t h(da)	Data hold time	10		ns
th(sync)	Sync hold time	10		ns
^t h(XI)	External input hold time	40		ns
tw(sens H)	Pulse width, sensor input high	500		ns
^t w(sens L)	Pulse width, sensor input low	500		ns
^t d(sens-int)	Delay time, sensor to interrupt (time between leading edges)		2000	ns
^t d(rst-int)	Delay time, RST instruction to interrupt (time between trailing edges)		500	ns

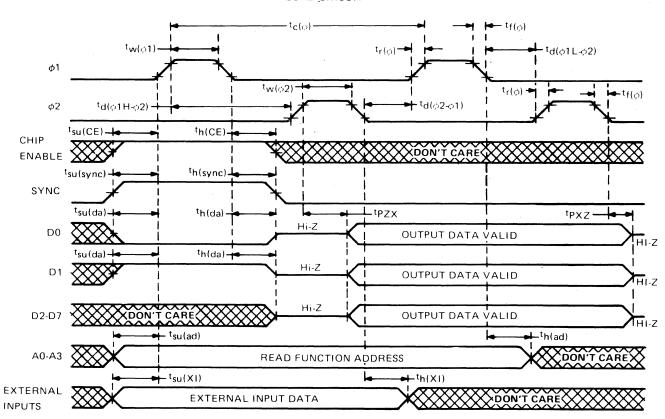
3.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURES 6 AND 7)

	PARAMETER	TEST CONDITIONS	MIN M	X	UNIT
tPZX	Data bus output enable time	C ₁ = 100 pF,	300		ns
tPXZ	Data bus output disable time to high-impedance state	$R_1 = 1.3 \text{ k}\Omega$	1	80	ns
tPD	External data output propagation delay time from $\phi 2$	NE = 1.3 K12	2	00	ns



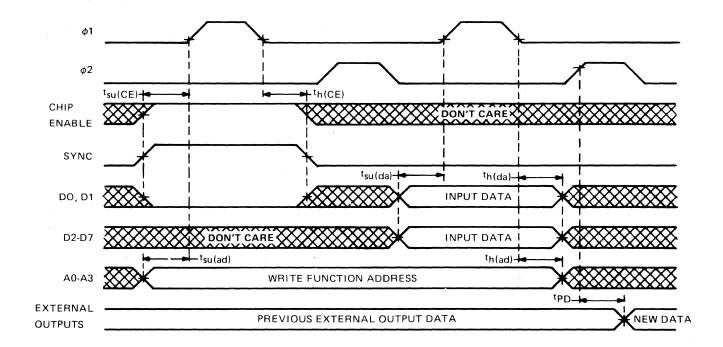
 C_L includes probe and jig capacitance

LOAD CIRCUIT



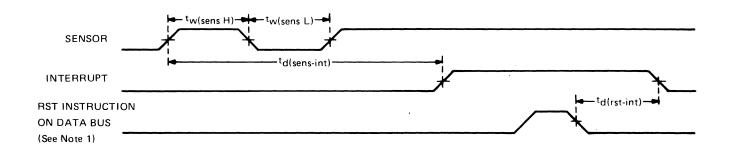
NOTE: For ϕ 1 or ϕ 2 inputs TPZX high and low timing points are 90% and 10% of $V_{1H(\phi)}$. All other timing points are the 50% level.

FIGURE 6-READ CYCLE TIMING



NOTE: For $\phi 1$ and $\phi 2$ inputs, high and low timing points are 90% and 10% of $V_{1H(\phi)}$. All other timing points are the 50% level.

FIGURE 7-WRITE CYCLE TIMING

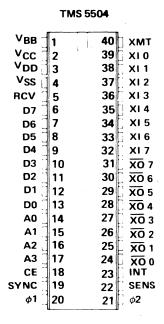


NOTES: 1. The RST instruction occurs during the output data valid time of the read cycle.

2. All timing points are 50% of $V_{\mbox{\scriptsize IH}}$.

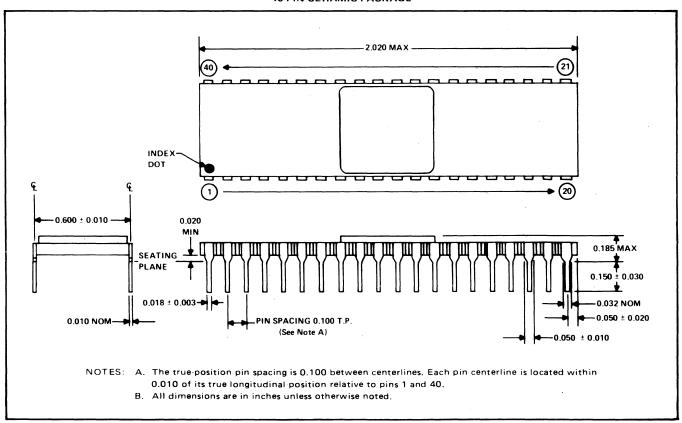
FIGURE 8-SENSOR/INTERRUPT TIMING

3.6 TERMINAL ASSIGNMENTS



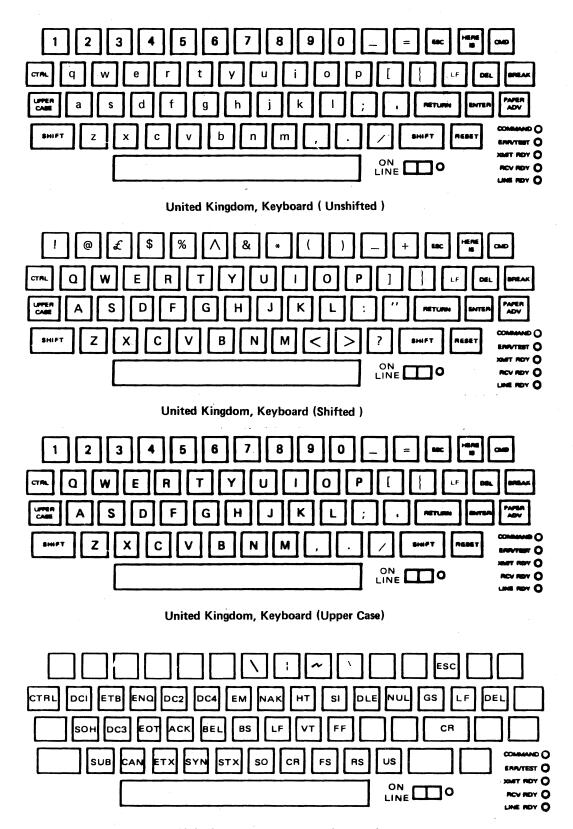
3.7 MECHANICAL DATA

40-PIN CERAMIC PACKAGE

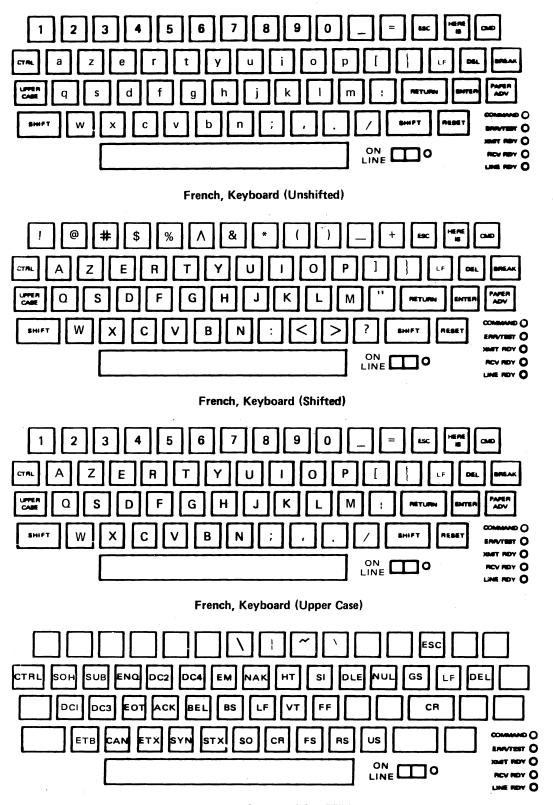


Appendix C

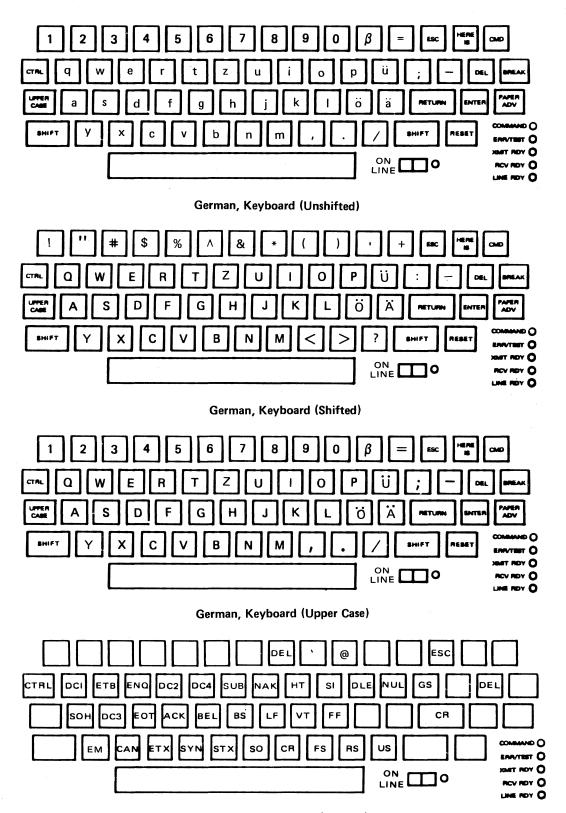
Foreign Keyboard Layouts and Symbols



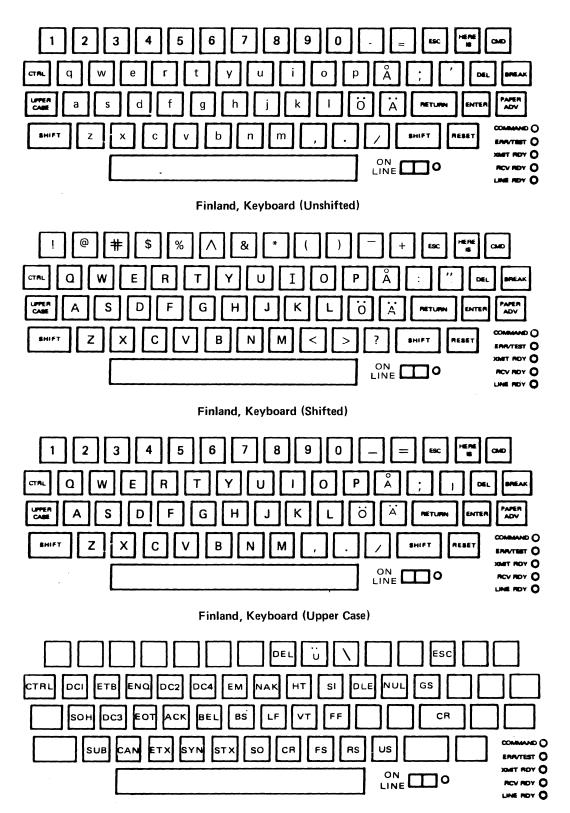
United Kingdom, Keyboard (Control)



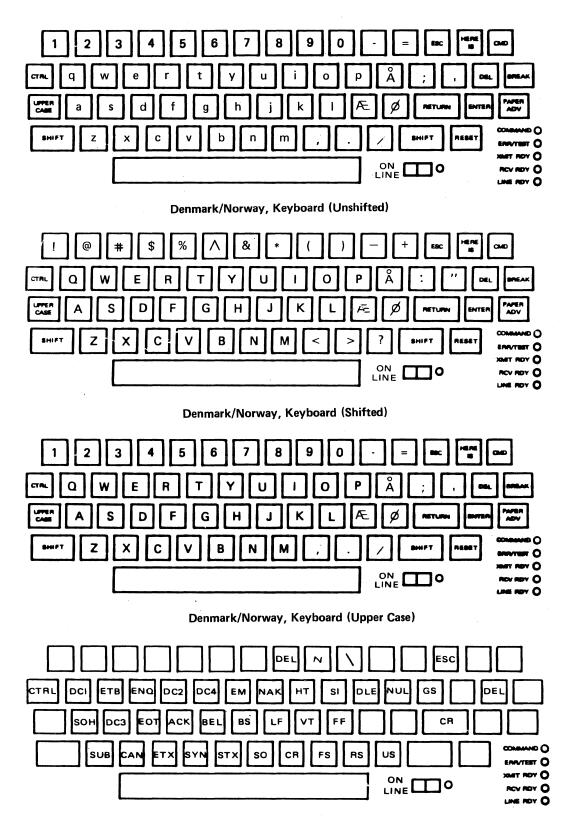
French, Keyboard (Control)



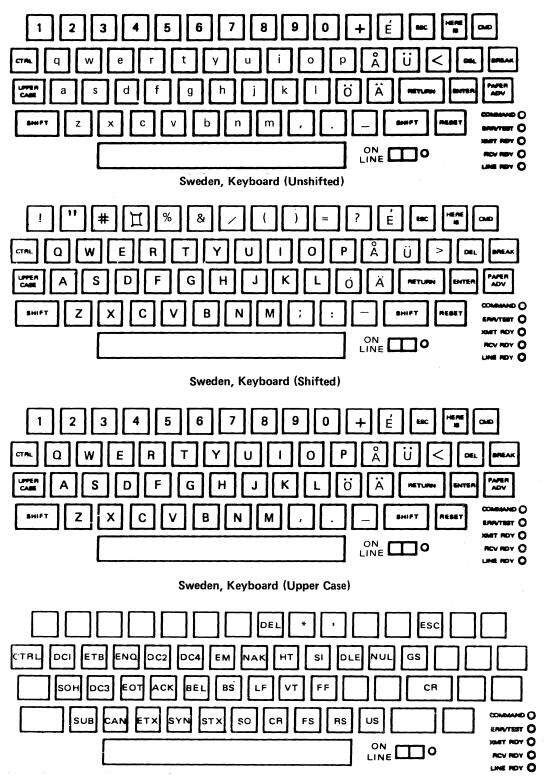
German, Keyboard (Control)



Finland, Keyboard (Control)



Denmark/Norway, Keyboard (Control)



Sweden, Keyboard (Control)

	CONTROL	3	UPPERCA	SE	LOWER	CASE		
BITS b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁	0 0 0 0 0 1	0 0 1 1 0 1 2 3	1 0 0	1 0 1 5	1 1 0	1 1 1		
0 0 0 0	NUL DLE	Space		6		11		
0 0 0 1	SOH DC1							
0 0 1 0	STX DC2							
0 0 1 1	ETX DC3						·	
0 1 0 0	EOT DC4	12					INTERNATIONAL CHARACTERS	
0 1 0 1	ENO. NAK						United Kingdom Character	1
0 1 1 0	ACK SYN						Sweden/Norway Characters	7
0 1 1 1	BEL ETB						Sweden/Finland German Characters	8
1 0 0 0	BS CAN						Sweden/Finland German Characters	9
1 0 0 1	HT EM						German/Sweden Finland Character	10
1 0 1 0	LF SUB						Sweden Characters	11
1 0 1 1	VT ESC		5		10		Sweden Character	12
1 1 0 0	FF FS		4		9		Finland Character	8
1 1 0 1	CR GS	13	2		7		German Character	13
1 1 1 0	SO RS		3		8		Norway/Denmark Characters	9
1 1 1 1	SI US					DEL *	Norway/Denmark Characters CONTROL CHARACTER	10

The following characters are generated/printed by the terminal.

8 7 6 4 3 2 1	0 0	0 0 0	0 0 1 0	0 0 1	0 1 0	0 1 0	0 1 1 0	0 1 1 1
0 0 0 0	NUL	DLE	SP	0	@	Р	•	Р
0 0 0 1	SOH		1	1	Α	Q	а	q
0 0 1 0	STX	DC2	"	2	В	R	b	r
0 0 1 1	ETX	DC3	#	3	С	S	C	s
0 1 0 0	EOT	DCA	\$	4	D	T	d	t
0 1 0 1	ENQ	NAK	%	5	E	U	e	u
0 1 1 0	ACK	SYN	&	6	F	٧	· f	٧
0 1 1 1	BEL		,	7	G	W	g ·	w
1 0 0 0	BS	CAN	(8	Н	X	h	x
1 0 0 1		EM)	9	ı	Y	i	У
1 0 1 0	LF	SUB	*	:	J	Z	j	Z
1 0 1 1	VT		+	;	K	[k	
1 1 0 0	FF	FS	,	<	L	\	1	
1 1 0 1	CR	GS		=	М]	m	
1 1 1 0	SO	RŞ	•	>	N	٨	n	~
1 1 1 1	SI	UŞ	/	?	0		0	DEL

Printable Characters		ONLINE Report Control
Printer Control Characters		
Codes Generated and Transmitt	ted by the termin	nal

NUL SOH STX ETX EOT ENQ ACK BEL BS HT LF VT FF CR SO SI

LE DC1 DC2 DC3 DC4 NAK SYN ETB CAN EM SUB ESC FS GS RS US DEL

Appendix D

Recommended Data Set Options and Cabling Information

ACCESSORY CABLES

Table D-1 specifies part numbers and description of the accessory cables available for specific equipment interface. Table D-2 through D-13 provide additional data on these cables.

Table D-14 contains the recommended settings of the 103J, 202, 212, and VADIC 3400 Series modems for use with the Model 780 Terminals.

Table D-1. Accessory Cables

ltem	Part Number	Description	780 Connector Type	Device Connector Type	Leng Meters		
1	2262093-0001	990 TTY/EIA To 820 Cable	25 Pin Male	25 Pin Male	9.1	30	
2	2262094-0001	990 Extension - 820 Cable	25 Pin Male	25 Pin Female	1.8	6	
3	993205-0001	113A/103/202/212 Data Set	25 Pin Male	25 Pin Male	1.8	6	
4	993210-0001	Data Terminal Cable	25 Pin Male	25 Pin Female	1.8	6	
5	993239-0001	770 Data Terminal Cable	25 Pin Male	25 Pin Male	1.8	6	
6	2263351-0001	Terminal Adapter Cable	25 Pin Female	25 Pin Female	1.8	6	
7	993211-0001	EIA Extension Cable (25 wires)	25 Pin Male	25 Pin Female	1.8	6	
8	959372-0002	733 EIA Cable	25 Pin Male	25 Pin Edge	1.8	6	
9	969626-0001	742 EIA Cable	25 Pin Male	10 Pin Dual	1.8	6	
				Edge Connector			N/A
10	973265-0001	742 Auxiliary Cable	25 Pin Female	15 Pin Dual	3.7	12	
		·		Edge Connector			
11	983848-0001	743 EIA Cable	25 Pin Male	15 Pin Female	1.8	6	
12	2263350-0001	763/765 Data Terminal Cable	25 Pin Male	15 Pin Female	1.8	6	
13	2200051-0001	763/765 Data Set Cable	25 Pin Male	15 Pin Female	1.8	6	
14	2265871-0001	TTY Current Loop Cable	25 Pin Male	4 Spade Lugs	1.8	6	
15	2207634-0001	Asynch/Synch EIA Cable	25 Pin Male	25 Pin Male	1.8	6	

^{*}This cable is recommended for use with the Bell 212 Modem that is configured for both 300 and 1200 baud operations.

Table D-2. Typical Connections

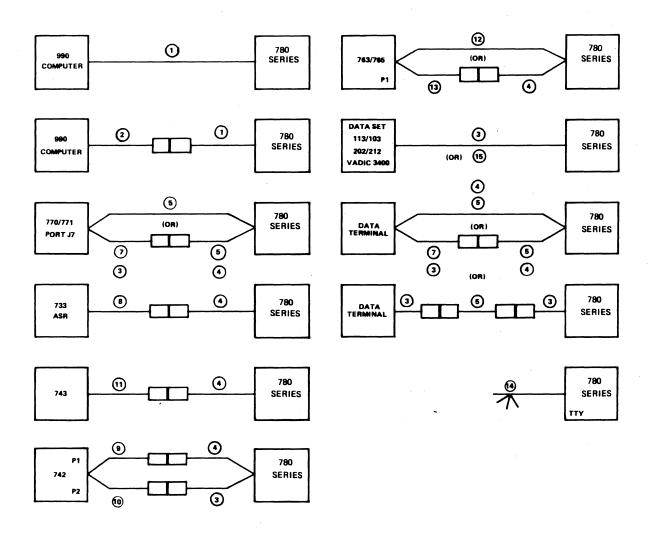


Table D-3. 113A/103, 202/212 Data Set Cable (TI Part No. 993205-0001)

780 (Male)	Data Set	RS-232-C Circuit	Function	
1	1	AA	Protective Ground	
1	1 .	BA		
2	2		Transmitted Data	
3	3	BB	Received Data	
4	4	CA	Request to Send	
5	5	СВ	Clear to Send	
6	6	cc	Data Set Ready	
7 8	7	AB	Signal Ground	
8	8	CF	Received Line Signal	
ļ			Detector	
11	11	SCA	Secondary Request	
			to Send (Reverse	
	i		Channel Transmit)	
12	12	SCF	Secondary Received	
'-	' ²	001	Line Signal Detector	
ł			, ,	
			(Reverse Channel	
			Receive)	
20	20	CD	Data Terminal Ready	
22	22	CE	Ring Indicator	

Table D-4. Data Terminal Cable (TI Part No. 993210-0001)

Reference:	Pin	RS-232-C Circuit	Function
	1	AA	Protective Ground
	2	BA	Transmitted Data
	3	BB	Received Data
ŀ	4	CA	Request to Send
	5	СВ	Clear to Send
	6	CC	Data Set Ready
	7	AB	Signal Ground
(Either	8	CF	Data Carrier Detect
End)	11	SCA	Reverse Channel
	40	205	Transmit
	12	SCF	Reverse Channel
l	4=		Receive
	15	DB	Transmission Signal
	47		Element Timing
	17	DD	Receive Signal Element
	20	CD	Timing Data Terminal Ready
	24	AUXLIO	Auxiliary Input/Output
	24	AUXLIU	Control

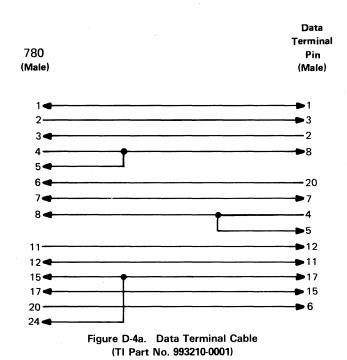
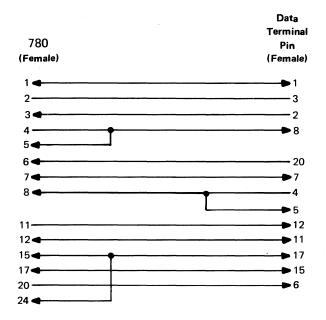


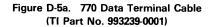
Table D-5. 770 Data Terminal Cable (TI Part No. 993239-0001)

Reference:	Pin	RS-232-C Circuit	Function
	1	AA	Protective Ground
	2	BA	Transmitted Data
	3	BB	Received Data
	4	CA	
	5	CB	Request to Send Clear to Send
	6	CC	Data Set Ready
{	7	AB	Signal Ground
(Either	8	CF	Data Carrier Detect
End)	11	SCA	Reverse Channel
2.7.0,	• • •	00,1	Transmit
	12	SCF	Reverse Channel
	-		Receive
	15	DB	Transmission Signal
			Element Timing
	17	DD	Receive Signal Element
			Timing
	20	CD	Data Terminal Ready
	24	AUXLIO	Auxiliary Input/Output
			Control
L	l	l	

Table D-6. Terminal Adapter Cable Pin Assignments (TI Part No. 2263351-0001)

Reference:	Pin	RS-232-C Circuit	Function
	_		
	1	AA	Protective Ground
	2	BA	Transmitted Data
	3	BB	Received Data
	4	CA	Request to Send
	5	СВ	Clear to Send
	6	cc	Data Set Ready
	7	AB	Signal Ground
(Either	8	CF	Data Carrier Detect
End)	11	SCA	Reverse Channel
			Transmit
	12	SCF	Reverse Channel
			Receive
	15	DB	Transmission Signal
			Element Timing
	17	DD	Receive Signal Element
			Timina
	20	CD	Data Terminal Ready
1	24	AUXLIO	Auxiliary Input/Output
	·		Control





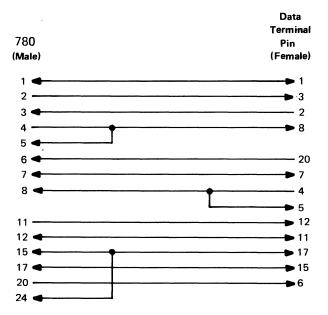


Figure D-6a. Terminal Adapter Cable (TI Part No. 2263351-0001)

Table D-7. 733 ASR Terminal Cable, 1200 Baud (TI Part No. 959372-0002)

ASR Pin 780 P1 RS-232-C Circuit **Function** 1 Α AΑ Protective Ground 2 Н ВА Transmitted Data 3 10 вв Received Data 4 С CA Request to Send 5 8 СВ Clear to Send 6 9 CC Data Set Ready

ΑB

CF

CD

Signal Ground

Detector

Received Line Signal

Data Terminal Ready

7

8

20

7

Κ

6

Table D-9. 742 Auxiliary Cable (TI Part No. 973265-0001)

780	742 Pin P2	RS-232-C Circuit	Function
3	11	ВВ	Received Data
4		CA	Request to Send
5		СВ	Clear to Send
6		CC	Data Set Ready
7	1	AB	Signal Ground
8		CF	Received Line Signal Detector
11	12	SCA	Secondary Request to Send
12	13	SCF	Secondary Received Line Signal Detector
20		CD	Data Terminal Ready

Table D-8. 742 Terminal Cable (TI Part No. 969626-0001)

780	742 P1	RS-232-C Circuit	Function
1	Α	AA	Protective Ground
2 3	Н	BA	Transmitted Data
3	10	BB	Received Data
4	F	CA	Request to Send
5	8	СВ	Clear to Send
6	9	CC	Data Set Ready
7	7	AB	Signal Ground
8	Κ	CF	Received Line Signal
			Detector
11	5	SCA	Secondary Request to Send
12	4	SCF	Secondary Received
			Line Signal Detector
20	6	CD	Data Terminal Ready
22	J	CE	Ring Indicator

Table D-9a. 742 Auxiliary Cable (TI Part No. 973265-0001)

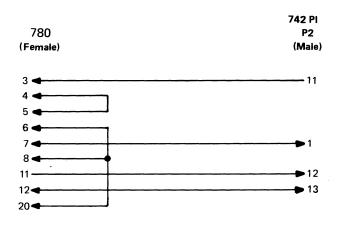


Table D-10. 743 Terminal Cable (TI Part No. 983848-0001)

780	743 Pin P1	RS-232-C Circuit	Function
1	9	AA	Protective Ground Transmitted Data Received Data Request to Send Signal Ground Received Line Signal Detector Data Terminal Ready
2	13	BA	
3	12	BB	
4	10	CA	
7	1	AB	
8	11	CF	

Table D-11. 763/765 Data Terminal Cable Pin Assignments (TI Part No. 2263350-0001)

763/765 Terminal Connector	780 Terminal	Function	763/765 Circuit	
(P1)	Plug	Tunction	EIA	C.C.I.T.T
-1	-1	PG	AA	101
-2	-11	CTS	СВ	106
-3	-2	RCV	ВВ	104
-4	-4 and -5	DCD	CF	109
-8	-6	DTR	CD	108.2
-9	-20 and -8	DSR/CCT	CC	107
-14	-3	XMT	ВА	103
-15	-7	SG	AB	102
1	l	1		

Table D-12. TTY Current Loop Interface Cable (TI Part No. 2265871-0001)

780 Series	Retainer Clip	Function	
13	E3	TTY Transmitted Data	X-1
14	E4	TTY Transmitted Data Return	X-2
16	E1	TTY Received Data Return	RL-1
18	E2	TTY Received Data	RL-2

Table D-13. Asynch/Synch EIA Cable (TI Part No. 2207634-0001)

780 Pin (Male)	Data Set Pin (Male)	RS-232-C Circuit	Function
1 2	1	AA BA	Protective Ground Transmitted Data
3	3	BB	Received Data
4	4	CA	Request to Send
5	5	CB	Clear to Send
6	6	CC	Data Set Ready
7	7	AB	Signal Ground
8	8	CF	Received Line Signal
"	·	. 01	Detector
11	11	SCA	Secondary Request to Send
12	12	SCF	Secondary Received
		,	Line Signal Detector
15	15	DB	Transmission Signal
			Element Timing
17	17	DD	Receiver Signal
			Element Timing
20	20	CD	Data Terminal Ready
22	22	CE	Ring Indicator
23	23	СН	Data Signal Rate Selector

NOTE: Recommended for use with the Bell 212 Data Sets equipped with Speed Control Option.

RECOMMENDED DATA SET OPTIONS

Table D-14 contains the recommended settings of the 103J, 202, 212, and VADIC 3400 Series modems for use with the Model 780 Terminals.

Table D-14. Recommended Data Set Options

103J	• .	212A	
Modem Option	Recommended Setting	Modem Option	Recommended Setting
Receive Space Disconnect Send Space Disconnect	Either — T or U Either — V or Y	Tip Ring Make BUSY CC Indication for Analog Loop	Out — E On — ZF
Loss of Carrier Disconnect	Either — V or T	CN Circuit	Out — YF
CC Indication		Transmitter Timing	Internal — YC
CB and CF Indications	Early — ZD Common — A	1200 Baud Operation	Async/start-stop — YG
	On – ZF	Character Length	10-bit — YJ
CC Indication for Analog Loop Automatic Answer	Ves – ZH	Receiver Respond to Digital Loop	Off — YL
Failsafe State of CN Circuit	res – zn Off – J	Loss of Carrier Disconnect	In — S
Common Ringer	Either — ZB or ZA	Receive Space Disconnect	In — V
Common Grounds	Yes — Q	CB and CF Indications	Common — A
Tip Ring Make Busy	res — u No — E	Send Space Disconnect	In — T
TIP NITIG IVIAKE BUSY	NO — E	Automatic Answer	In ZH
		Answer Mode Indication, CE	Off — W
		Speed Mode	Dual — YP
		Interface Speed Indication, CI	In — YQ
		Signal Ground to Frame	
		Connection	ln — Ω
		Speed Control	Interface — XJ
202S			
Modem Option	Recommended Setting	Vadic 3400 Series	
			Recommended
Soft Turnoff and Squelch Intervals	(R)	Modem Option	Setting
	Squelch = 156 ms (R)	Data Set Line Control	Auto Disconnect -
ast Carrier Detect	Out — N		ANS.
Clear To Send Interval	180 ms — G		Manual Disconnect —
Auto Answer	In — B		ORIG.
ocal Copy Primary Channel	Out — ZB	Abort Timer Disconnect	Enabled
Condition of CC (DSR) in	On — YI	Loss of Carrier Disconnect	Enabled
Analog Loop		Input Data Rate	1200 bps
Fransmit Only	Out — YH	Transmission Rate Control	1205 bps
Echo Suppression Enable	Out — YR	Transmit Clock	Internal
Carrier Control Turnaround	ln - YS	Asynch Character Length	10 Bit
Early CC (DSR) Indication	Out — YV	DTR Control	Terminal
Reverse Channel	Either — ZC or ZD	RTS Control	Forced
_ocal Copy on Reverse Channel	Out — ZF	Carrier Detect Control	Line
Grounding Option	Signal ground to	DSR Control	Off Hook
	frame — ZG	Injected Tone	Disabled

Appendix E

Operator Reference Cards

REPORTS/TESTS

Report Request:

Depress [CMD]

Depress [R]

Depress []

[Enter]

[1]

[2]

3

-Wait for Prompt -Wait for Prompt -Initiate Report **Combined Report** Config Report **Error Report**

Test Request:

Depress [CMD] Depress [TEST] 4 Depress [T] Depress []

-Initiate Test [1] Memory Check [2] Barberpole Test

[4] RDLB Test ② [5] ALB Test ②

-Wait for Prompt

-Wait for Prompt

-Wait for Prompt

[3] Transmit Test (3) [6] Transmit Barberpole

ERROR CODES

00 Test Failure

01 Test Failure

Recall Default

10 No LTA Char

11 Carriage Jam

12 Paper Out

20 CTS Timeout

21 Carrier Loss

Wrong Number

23 Receiver Overflow

24 Parity Error

Transmit Overflow 25

26 No Activity

RCV Char Lost

32 Modern Task (2)

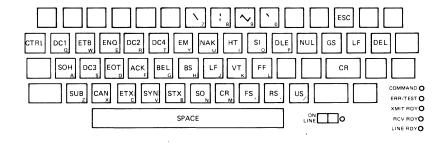
Modem Timeout ② 33

Dialing Error (5) 34

Modem Inventory (2) 35

Modem Status (2)

CONTROL KEYS ③



ASCII/HEX CODES (4)

ASCII	CODE		ASCI
NUL	00		BS
SOH	01		нт
STX	02		LF
ETX	03	l	VΤ
EOT	04		FF
ENQ	05		CR
ACK	06		so
RFI	07		SI

CII	HEX CODE		ASCII	HEX CODI
s	08		DLE	10
T	09		DC1	11
F	0A	ŀ	DC2	12
T	0B	l	DC3	13
F	0C		DC4	14
R	0D	ļ	NAK	15
0	0E	1	SYN	16
1	0F		ETB	17
		•		

E		ASCII	HEX CODE
		CAN	18
ı	ı	EM	19
		SUB	1A
		ESC	1B
		FS	1C
		GS	1D
		RS	1E
		US	1F

ASCII	HEX CODE
SPACE	20
!!	21
"	22
#	23
\$	24
%	25
&	26
'	27

ASCII	HEX CODE
(28
) -	29
*	2A
+	2B
,	2C
-	2D
	2E
1	2F

ASCII	HEX CODE	ASCII	HEX CODE
0	30	8	38
1	31	9	39
2	32	:	3A
3	33	;	3B
4	34	<	3C
5	35	=	3D
6	36	>	3E
7	37	?	3F

ASCII/HEX CODES 4

ASCII	CODE	
@	40	l
Α	41	l
В	42	ı
С	43	ı
D	44	l
E	45	ı
F	46	l
G	47	

ASCII	CODE
Н	48
1	49
J	4A
K	4B
L	4C
M-	4D
N	4E
0	4F

ASCII	HEX CODE
Р	50
a	51
R	52
S	53
Т	54
υ	- 55
V	56
w	57

	ASCII	HEX CODE
	х	58
	Υ	59
	Z	5A
	[5B
	١.	5C
į]	5D
	^	5E
	_	5F

	ASCII	HEX CODE
	•	60
	а	61
	b	62
	С	63
į	d	64
	е	65
	f.	66
	g	67

ASCII	HEX CODE
h	68
i	69
j	6A
k	6B
ı	6C
m	6D
n	6E
0	6F

ASCII	HEX CODE
р	70
q	71
r	72
s	73
l t	74
u	75
V	76
w	77

ASCII	HEX CODE
х	78
y	79
z	7A
1 1	7B
}	7C
	- 7D
\ ^	7E
DEL	7F

NOTES:

(1) 781/783 only.

(5) 787 only.

(2) 785/787 only. (3) Not available on 781. (6) 785 only.

(4) 781 only.

(7) 787 option.

CONFIGURATION

NOTE: Brackets represent keys. Empty brackets indicate selectable configuration codes.

 Enter Configuration 	re Function:		2) Enter Selection Chang	es: 3) Te	rminate Con	figure Function
Depress [CNFG] Depress [CMD]	-Wait for Prompt -Wait for Prompt	To Enable: To Enable:	Depress [] [] [CR] Depress [] [] [RETURN	Depres	ss [OPER] ss [ENTER]	-Report -Report
Depress [C]	-Wait for Report	To Disable:	Depress [] [] [DEL]	or Depres	ss [RESET]	-No Report
Special Commands	S					
Program ABM: De	press [7] [0] [CR] 4		3			
	press [7] [0] [RETURN	 Program LT. 	A: Depress [6] [0] [RETURN]	Default Configur	ration	
Ty	pe 1 to 32 Characters		Type 1 to 3 Characters	Set Selection:	Depress [0]	[9] [RETURN]
De	press [END]	j	Depress [HERE IS]		Depress [0]	[9] [CR] ④

PARAMETERS

Method (Required) Select One	Speed (Required) Select One	Parity (Required) Select One
[1] [1] = 202/Half Duplex (3)	[2] [1] = 110 bps	[3] [1] = Odd, No Check
[1] [2] = 202/Reverse Channel/(H D)	[2] [2] = 200 bps	[3] [2] = Even, No Check
[1] [3] = 103/113/212/3400/Full Duplex	[2] [3] = 300 bps	[3] [5] = Odd with Check
[1] [4] = Reverse Channel on Ready	[2] [4] = 600 bps	[3] [6] = Even with Check
[1] [5] = Reverse Channel off Ready 3	[2] [5] = 1200 bps	[3] [7] = Mark, No Check
[1] [6] = DC Current Loop (1)	[2] [6] = 2400 bps	[3] [8] = Space, No Check
[1] [7] = Internal Modem (2)	[2] [8] = 9600 bps	
[1] [8] = DTR on for Ready 4	[2] [9] = 300/1200 bps	

PARAMETERS

Additional Selections (Not R	equired - Any Number Are Allov	wed)	
[6] [1] = Fail-safe Disc	[7] [2] = Print ABM	[8] [2] = Local Copy	[9] [4] = Col 72 Bell 3
[6] [2] = EOT Disconnect	[7] [3] = Autotrigger ANS	[8] [3] = DC1/DC3 Ready/Busy	[9][5] = 6 LF/CR on FF
[6] [3] = DLE EOT Disc	[7] [4] = Autotrigger Orig	[8] [4] = New Line on LF	
[6] [4] = Paper Out Disc		[8] [5] = New Line on CR	
[6] [5] = No Activity Disc		[8] [6] = CR LF on Return ③	
[6] [6] = No LTA Required 3	-	[8] [7] = Print Control	

PARAMETERS (MODEM) 2

Modem Selections			
Interface (Required)	Modem Type (Required)	Mode (Required)	Additional (Not Required)
Select One	Select One	Select One	Any Number
[1] [0] [1] = Direct Connect 5	[1] [1] [1] = Autoselect	[1] [2] [1] = Ans/Orig	[1] [3] [1] = Tone Dial (5)
[1] [0] [2] = Acoustic 6 7	[1] [1] [2] = 103 Fixed	[1] [2] [2] = Ans Only	[1] [3] [2] = Equalizer On
	[1] [1] [3] = 212 Fixed (5)	[1] [2] [3] = Orig Only 6	[1] [3] [3] = RDLB Test
	[1] [1] [4] = 3400 Fixed		[1] [3] [4] = RDLB Data
·		·	[1] [3] [5] = Disable Disconnect

MODEM COMMANDS (5)

Store Phone Number:		Dial Phone Number:	
Depress [CMD]	-Wait for Prompt	Depress [CMD]	-Wait for Prompt
Depress [D]	-Prints Current Phone Number	Depress [D]	-Prints Current Phone Number
Enter []	-Phone Number (Up to 32 Characters)*	Depress [ENTER]	-Requests a Dial Tone
Depress [RETURN]	-Stores Phone Number and Terminates Command	Depress [ENTER]	-Dials Phone Number
*(+ or - Dial Control)			
Erase Phone Number:		Hang Up:	
Depress [CMD]	-Wait for Prompt	Depress [CMD]	-Wait for Prompt
Depress [D]	-Prints Current Phone Number	Depress [CMD]	-Wait for Prompt
Depress [DEL]	-Erases Current Phone Number		
	and Terminates Command		

Notes:

(1) 781/	783 on	ly.
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(5) 787 only.

(6) 785 only.

(7) 787 option.

^{(2) 785/787} only.

⁽³⁾ Not available on 781. (4) 781 only.

TONE DIAL OPTION INSTALATION PROCEDURE

- 1. INSTAL CHIP
- 2. CHANGE STRAPS
- 3. CHANGE CONFIGURATION
- 1a. INSTALATION OF CHIP: (GENERIC CHIP PT#2211781-0002)
 INSTAL CHIP ON MODEM BOARD IN CHIP LOCATION M-7
- 2a. CHANGING STRAPS: FIRST STRAP LOCATED DIRECTLY ABOVE CHIP LOCATION M-7..... STRAP WAS ON PIN 2-3.... STRAP SHOULD NOW BE ON PINS 1-2.....
- 3a.CONFIGURATION CHANGE: AFTER CHIP HAS BEEN INSTALLED AND STRAP HAS BEEN CHANGED, YOU THEN NEED TO CHANGE CONFIGURATION...
- 3b.GO INTO CONFIGURATION MODE TYPE C WHICH WILL PRINT OUT CURRENT CONFIGURATION...AFTER CONFIG. PRINTS OUT TYPE IN 09 cr. enter. CHANGENG CONFIG. TO 09 WILL RECOGNIZE THE STRAP SETTINGS THAT WERE CHANGED....NOW GO BACK INTO CONFIGURATION AND ENTER 131. WHICH IS THE OPTION FOR THE TONE DIAL IN THE CONFIGURATION.

T ALONG 1

USER'S RESPONSE SHEET

Manual Title:	780 Series N	Naintenance Manual				
	Part Numbe	Part Number 2265862-9701				
Manual Date:	15 March 19	981	Date of This Letter:			
User's Name:			Telephone:			
Company:			Office/Department:			
Street Address	s:					
City/State/Zip	Code:					
			y page, paragraph, figure, or table number in the four wish to make, feel free to include them. Thank			
Location in	Manual		Comment / Suggestion			
						
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