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## High-Speed Memory Interface Logic Data Book

## Address Drivers, Data Transceivers, Clock Drivers, and Synchronous DRAMs







#### INTRODUCTION

Texas Instruments (TI) Advanced System Logic group has a broad portfolio of devices designed for high-speed memory interfacing. Sections 2, 3, and 4–Data Transceivers/Multiplexers, Address Buffers/Latches/Flip-Flops, and Clock-Distribution Circuits–contain devices that have set the industry standards for fast propagation-delay speeds, bus hold, and low simultaneous-switching noise. Device families within this text include:

ALVC – One of the highest-performance 3.3-V bus-interface device families is ALVC. These specially designed 3.3-V products are processed in 0.6- $\mu$  CMOS technology, giving propagation of delays less than 3 ns, along with current drive of 24 mA and static power consumption of 40  $\mu$ A for bus-interface functions. The ALVC devices have bus-hold cells on inputs to eliminate the need for external pullup/pulldown resistors for floating inputs. The family also includes innovative functions with integrated series-damping resistors for memory interleaving, multiplexing, and interfacing to synchronous DRAMS.

SSTL – TI is the first to offer interface logic based on the new SSTL\_3 (stub series terminated logic) standard. With both an address driver and a clock driver that conform to this standard, TI continues to innovate logic for future generations of SDRAM.

LVT – The specially designed 3.3-V LVT family uses the latest 0.8- $\mu$  BiCMOS-process technology for bus-interface functions. LVT can provide up to 24 mA of drive, 4-ns propagation delays, and, in addition, consumes less than 100  $\mu$ A of standby current. The inputs have the bus-hold feature to eliminate the need for external pullup/pulldown resistors and I/Os that can tolerate up to 7 volts, which can allow them to act as 5-V/3.3-V translators.

ALB – The specially designed 3.3-V ALB family uses the latest in  $0.6-\mu$  technology for bus-interface functions. ALB provides 25 mA of drive at 3.3 V and boasts a maximum propagation delay of 2.2 ns, making it the fastest TI logic family to date. The inputs have clamping diodes to eliminate signal overshoot and undershoot.

CDC – TI's CDCs provide accurate clock-generation circuitry fundamental to every digital system, producing timing signals that are used to synchronize system activity. To meet the stringent clock-signal timing requirements of today's systems, TI offers a series of low-propagation delay and skew, high-fan-out clock drivers designed to effectively drive high-performance clocking systems.

CBT – The CBT (crossbar technology) family is the industry's bus switch of choice. CBT enables a bus-interface device to function in one of two valuable roles. When the switch is closed, it is a very fast bus switch, effectively isolating buses. When the switch is open, it offers very little propagation delay. These devices can function as high-speed bus interfaces for computer-system components such as the central processing unit (CPU) and memory.

For more information on these or other TI products, please contact your local TI representative, authorized distributor, the TI technical support hotline at 972-644-5580, or visit the TI home page at http://www.ti.com.

For a complete listing of all TI logic products, please order the Logic Selection Guide (literature number SDYU001) by calling our literature response center at 1-800-477-8924.

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## INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

## operating conditions and characteristics (in sequence by letter symbols)

C<sub>i</sub> Input capacitance

The internal capacitance at an input of the device

Cio Input/output capacitance

Input-to-output internal capacitance; transcapacitance

### Co Output capacitance

The internal capacitance at an output of the device

## C<sub>pd</sub> Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages):  $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$ 

## fmax Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification

### I<sub>CC</sub> Supply current

The current into\* the V<sub>CC</sub> supply terminal of an integrated circuit

## △I<sub>CC</sub> Supply current change

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ 

### ICEX Output high leakage current

The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition  $V_{O}$  = 5.5 V

## II(hold) Input hold current

Input current that holds the input at the previous state when the driving device goes to a high-impedance state

## IIH High-level input current

The current into\* an input when a high-level voltage is applied to that input

### IIL Low-level input current

The current into\* an input when a low-level voltage is applied to that input

## Input/output power-off leakage current

The current into a circuit mode when the device or a portion of the device affecting that circuit node is in the off state

#### IOH High-level output current

The current into\* an output with input conditions applied that, according to the product specification, establish a high level at the output

\*Current out of a terminal is given as a negative value.



#### t<sub>PHL</sub> Propagation delay time, high-to-low level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

## t<sub>PHZ</sub> Disable time (of a 3-state output) from high level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

#### tPLH Propagation delay time, low-to-high level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

#### tpLZ Disable time (of a 3-state output) from low level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

#### t<sub>PZH</sub> Enable time (of a 3-state output) to high level

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high leve

#### tpzL Enable time (of a 3-state output) to low level

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

## t<sub>sk(I)</sub> Input skew

The difference between any two propagation delay times that originate at different inputs and terminate at a single output. Input skew describes the ability of a device to manipulate (stretch, shrink, or chop) a clock signal. This is typically accomplished with a multiple-input gate wherein one of the inputs acts as a controlling signal to pass the clock through.  $t_{sk(l)}$  describes the ability of the gate to shape the pulse to the same duration regardless of the input used as the controlling input.

## t<sub>sk(I)</sub> Limit skew

The difference between 1) the greater of the maximum specified values of  $t_{PLH}$  and  $t_{PHL}$  and 2) the lesser of the minimum specified values of  $t_{PLH}$  and  $t_{PHL}$ . Limit skew is not directly observed on a device but rather is calculated from the data sheet limits for  $t_{PLH}$  and  $t_{PHL}$ .  $t_{sk(i)}$  quantifies for the designer how much variation in propagation delay time will be induced by operation over the entire ranges of supply voltage, temperature, output load, and other specified operating conditions. Specified as such,  $t_{sk(i)}$  also accounts for process variation. In fact, all other skew specifications [ $t_{sk(o)}$ ,  $t_{sk(i)}$ ,  $t_{sk(p)}$ , and  $t_{sk(pr)}$ ] are subsets of  $t_{sk(i)}$ ; they are never greater than  $t_{sk(i)}$ .

## t<sub>sk(o)</sub> Output Skew

The difference between any two propagation delay times when a single switching input or multiple inputs switching simultaneously cause multiple outputs to switch, as observed across all switching outputs. This parameter is used to describe the fanout capability of a clock driver and is of concern when making decisions on clock buffering and distribution networks.

## t<sub>sk(p)</sub> Puise Skew

The difference between propagation delay times  $t_{PHL}$  and  $t_{PLH}$  when a single switching input causes one or more outputs to switch.  $t_{sk(p)}$  quantifies the duty cycle characteristic of a clock driver. Certain applications require a fixed duty cycle for proper operation. As an example, the CLK2 input of an MC68020 processor operating at 40 MHz requires a duty cycle of 50  $\pm$  5%.  $t_{sk(p)}$  is a measure of a clock driver's ability to supply such a precisely controlled pulse.



## **EXPLANATION OF FUNCTION TABLES**

The following symbols are used in function tables on TI data sheets:

- H = high level (steady state)
- L = low level (steady state)
- ↑ = transition from low to high level
- = transition from high to low level
- ---- = value/level or resulting value/level is routed to indicated destination
- = value/level is re-entered
- X = irrelevant (any input, including transitions)
- Z = off (high-impedance) state of a 3-state output
- a...h = the level of steady-state inputs A through H respectively
- Q0 = level of Q before the indicated steady-state input conditions were established
- $\overline{Q}_0$  = complement of  $Q_0$  or level of  $\overline{Q}$  before the indicated steady-state input conditions were established
- $Q_n$  = level of Q before the most recent active transition indicated by  $\downarrow$  or  $\uparrow$
- \_\_\_\_ = one high-level pulse
- = one low-level pulse
- Toggle = each output changes to the complement of its previous level on each active transition indicated by  $\downarrow$  or  $\uparrow$

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with  $\uparrow$  and/or  $\downarrow$ , this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q<sub>0</sub>, or  $\overline{Q}_0$ ), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse,  $\neg \neg$  or  $\neg \neg$ , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

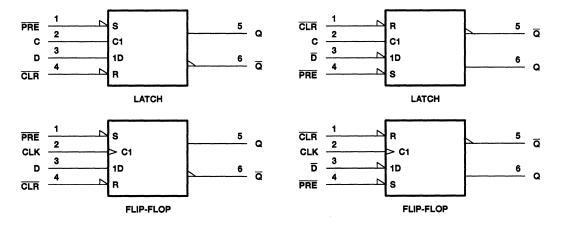


## D FLIP-FLOP AND LATCH SIGNAL CONVENTIONS

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called  $\overline{Q}$ . An input that causes a Q output to go high or a  $\overline{Q}$  output to go low is called preset (PRE). An input that causes a  $\overline{Q}$  output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active low.

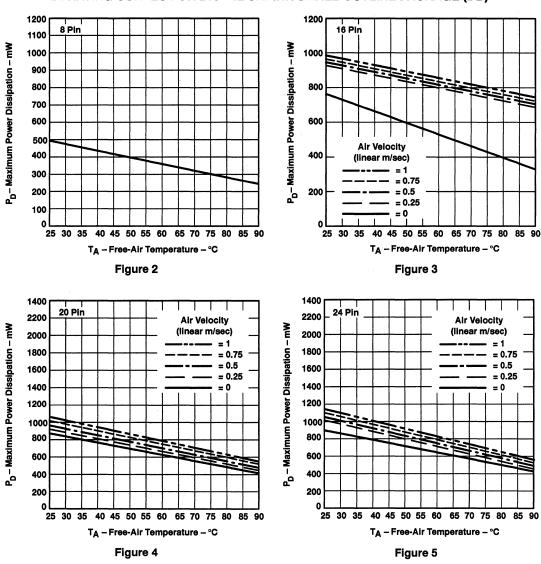
The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits  $\overline{D}$  and Q.

In some applications, it may be advantageous to redesignate the data input from D to  $\overline{D}$  or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and  $\overline{Q}$  exchange names, the preset and clear pins also exchange names. The polarity indicators ( $\square$ ) on PRE and CLR remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or  $\overline{D}$ ), Q, and  $\overline{Q}$ . Pin 5 (Q or  $\overline{Q}$ ) is still in phase with the data input (D or  $\overline{D}$ ); their active levels change together.









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## SN74ALVCH16500 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES023C - JULY 1995 - REVISED NOVEMBER 1996

	nber of the Texas Instruments <i>Jebus</i> ™ Family	DGG OR DL (TOP )	
	/C™ (Enhanced-Performance Implanted OS) Submicron Process		56 GND
	7™ (Universal Bus Transceiver)		54 B1
	nbines D-Type Latches and D-Type	GND 14	53 GND
	-Flops for Operation in Transparent,	A2 1 5	52 B2
Late	ched, or Clocked Mode	A2 U3 A3 [] 6	51 B3
• ESI	D Protection Exceeds 2000 V Per		50 V <sub>CC</sub>
MIL	-STD-883, Method 3015; Exceeds		49 B4
	V Using Machine Model	A5 0 9	49 B5
(C =	= 200 pF, R = 0)		47 B6
Late	ch-Up Performance Exceeds 250 mA Per		
JED	DEC Standard JESD-17	A7 0 12	45 B7
Bus	s Hold on Data Inputs Eliminates the	A8 1 13	44 B8
	ed for External Pullup/Pulldown	A9 11 14	43 B9
	sistors	A10 15	42 B10
Pac	kage Options Include Plastic 300-mil	A11 1 16	41 B11
	ink Small-Outline (DL) and Thin Shrink	A12 17	40 B12
	all-Outline (DGG) Packages	GND 18	39 🛛 GND
		A13 🚺 19	38 🛛 B13
descripti	ion	A14 🚺 20	37 🚺 B14
		A15 🛛 21	36 🛛 B15
	18-bit universal bus transceiver is designed	V <sub>CC</sub> 🛛 22	35 🛛 V <sub>CC</sub>
tor 2.	.3-V to 3.6-V V <sub>CC</sub> operation.	A16 23	34 B16
Data	flow in each direction is controlled by	A17 🚺 24	33 🛛 B17
	ut-enable (OEAB and OEBA), latch-enable	GND 🚺 25	32 🛛 GND
	B and LEBA), and clock (CLKAB and	A18 🚺 26	31 B18
	BA) inputs. For A-to-B data flow, the device	OEBA 🚺 27	30 CLKBA
opera	ates in the transparent mode when LEAB is	LEBA 🚺 28	29 GND

is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and OEBA is active low).

To ensure the high-impedance state during power up or power down,  $\overline{\text{OEBA}}$  should be tied to  $V_{CC}$  through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16500 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16500 is characterized for operation from -40°C to 85°C.

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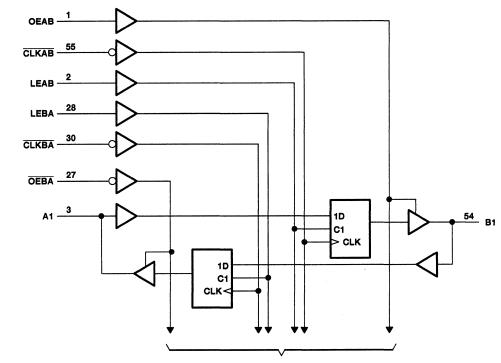
high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB

PRODUCTION DATA information is current as of publication date. Products conform to specifications par the terms of Texas instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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## SN74ALVCH16500 **18-BIT UNIVERSAL BUS TRANSCEIVER** WITH 3-STATE OUTPUTS SCES023C - JULY 1995 - REVISED NOVEMBER 1996



To 17 Other Channels

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	-0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	–0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, IIK (VI < 0)	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	
Continuous current through each V <sub>CC</sub> or GND	
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG package	
	1.4 W
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamo-current ratings are observed.
  - This value is limited to 4.6 V maximum. 2.

logic diagram (positive logic)

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. 3. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book.



## SN74ALVCH16500 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES023C - JULY 1995 - REVISED NOVEMBER 1996

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				$\begin{array}{c c} 2.5 \ V \\ 0.2 \ V \\ \end{array}  \begin{array}{c c} V \\ V_{CC} = 2.7 \ V \\ \pm \ 0.3 \ V \\ \end{array}  \begin{array}{c c} V_{CC} = 3.3 \ V \\ \pm \ 0.3 \ V \\ \end{array}$		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V	
			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	150	0	150	MHz
	D. has also that	LE high	3.3		3.3		3.3		
tw	Pulse duration	CLK high or low	3.3		3.3		3.3		ns
		Data before $\overline{CLK}\downarrow$	1.7		1.4		1.3		
t <sub>su</sub>	Setup time	Data before LE↓, CLK high	1.1		1		1		ns
		Data before LE↓, CLK low	1.9		1.6		1.4		,
th		Data after CLK↓	1.7		1.6		1.3		
	Hold time	Data after LE↓, CLK high	· 2		1.8		1.5		ns
		Data after LE↓, CLK low	1.6		1.5		1.2		

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
	(INPUT)	(001901)	MIN	MAX	MIN	MAX	MIN	MAX	
fmax			150		150		150		MHz
	A or B	B or A	1	5.7		4.7	1	3.9	
<sup>t</sup> pd	LEAB or LEBA	A or B	1	6.5		5.5	1	4.7	ns
	CLKAB or CLKBA	A or B	1	7.2		6.6	1.1	5.5	
t <sub>en</sub>	OEAB	B	1	6.2		5.4	1	4.6	ns
tdis	OEAB	В	1.7	6.3		5.7	1.5	5	ns
ten	OEBA	А	1	6.7		6.2	1	5.2	ns
<sup>t</sup> dis	OEBA	A	1	5.6		4.6	1	4.3	ns

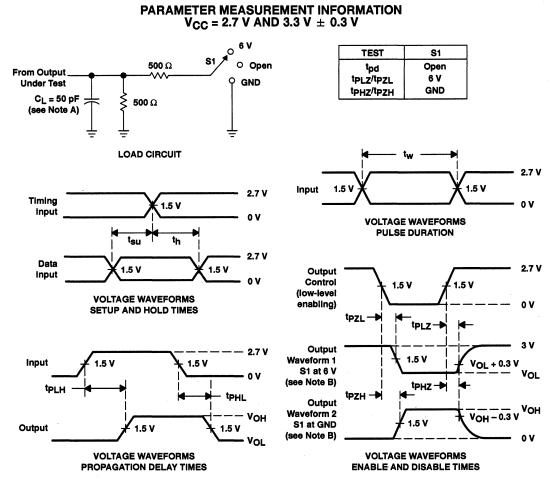
## operating characteristics, T<sub>A</sub> = 25°C

	PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
	Power dissipation capacitance	Outputs enabled	C <sub>L</sub> = 50 pF, f = 10 MHz	40	51	
Cpd	Power dissipation capacitance	Outputs disabled		6	6	pF



## SN74ALVCH16500 **18-BIT UNIVERSAL BUS TRANSCEI** WITH 3-STATE OUTPUTS

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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms



## SN74ALVCH16501 **18-BIT UNIVERSAL BUS TRANS** WITH 3-STATE OUTPUTS

SCES024A - JULY 1995 - REVISED NOVEMBER 1996

<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	DGG OR DL PACKAGE (TOP VIEW)	
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>		
<ul> <li>UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type</li> </ul>	A1 🛛 3 54 🗍 B1	
Flip-Flops for Operation in Transparent, Latched, or Clocked Mode	GND 4 53 GND A2 5 52 B2	
<ul> <li>ESD Protection Exceeds 2000 V Per</li> </ul>	A3 [] 6 51 ] B3 V <sub>CC</sub> [] 7 50 ] V <sub>CC</sub> ,	
MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model	A4 🛛 8 49 🗍 B4	
(C = 200 pF, R = 0)	A5 9 48 B5 A6 10 47 B6	
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	GND 11 46 GND A7 12 45 B7	
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown</li> </ul>	A8 🛛 13 44 🖸 B8	
Resistors	A9 114 43 B9 A10 15 42 B10	
<ul> <li>Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink</li> </ul>	A11 0 16 41 0 B11 A12 0 17 40 0 B12	
Small-Outline (DGG) Packages	GND 🛛 18 39 🗍 GND	
description	A13 [] 19 38 [] B13 A14 [] 20 37 [] B14	
This 18-bit universal bus transceiver is designed	A15 21 36 B15 V <sub>CC</sub> 22 35 V <sub>CC</sub>	
for 2.3-V to 3.6-V V <sub>CC</sub> operation.	A16 23 34 B16	
Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable	A17 224 33 B17 GND 25 32 GND	
(LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device	A18 [ 26 31 ] B18 OEBA [ 27 30 ] CLKBA	

is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

LEBA 28

29 GND

To ensure the high-impedance state during power up or power down,  $\overline{OEBA}$  should be tied to V<sub>CC</sub> through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

The SN74ALVCH16501 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16501 is characterized for operation from -40°C to 85°C.

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operates in the transparent mode when LEAB is

high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB

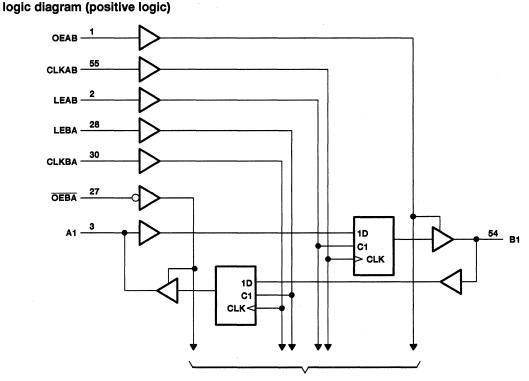
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## SN74ALVCH16501 **18-BIT UNIVERSAL BUS TRANSCEIV** WITH 3-STATE OUTPUTS

SCES024A - JULY 1995 - REVISED NOVEMBER 1996



To 17 Other Channels

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	–0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	–0.5 V to V <sub>CC</sub> + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	–0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, IIK (VI < 0)	
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3)	DGG package 1 W
	DL package 1.4 W
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - 2. This value is limited to 4.6 V maximum.
  - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book.



## SN74ALVCH16501 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES024A – JULY 1995 – REVISED NOVEMBER 1996

## timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V <sub>CC</sub> = 2.5 V ± 0.2 V								UNIT
			MIN	MAX	MIN	MAX	MIN	MAX			
fclock	Clock frequency		0	150	0	150	0	150	MHz		
tw	Pulse duration	LE high	3.3		3.3		3.3				
	Pulse duration	CLK high or low	3.3		3.3		3.3		ns		
	Setup time	Data before CLK↑	2.2		2.1		1.7				
t <sub>su</sub>		Data before LE↓, CLK high	1.9		1.6		1.5		ns		
		Data before LE↓, CLK low	1.3		1.1		1				
	Hold time	Data after CLK↑	0.6		0.6		0.7		ns		
th		Data after LE↓, CLK high or low	1.4		1.7		1.4				

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

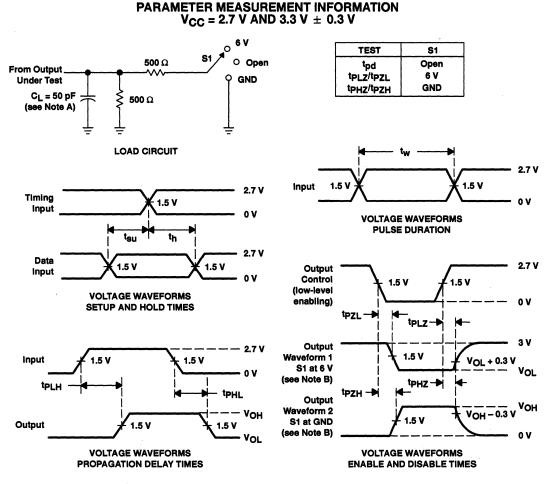
PARAMETER		TO (OUTPUT)		$V_{CC} = 2.5 V$ ± 0.2 V		2.7 V	V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
	(INFOT)	(001F01)	MIN	MAX	MIN	MAX	MIN	MAX	
fmax			150		150		150		MHz
	A or B	B or A	1.2	5.4		4.5	1	3.9	
<sup>t</sup> pd	LE	A or B	1.6	6.3		5.3	1.3	4.6	ns
	CLK	A or B	1.7	6.7		5.6	1.4	4.9	
ten	OEAB	В	1.1	6.3		5.3	1	4.6	ns
<sup>t</sup> dis	OEAB	В	2.2	6.4		5.7	1.4	5	ns
<sup>t</sup> en	OEBA	A	1.4	6.8		6	1.1	5	ns
<sup>t</sup> dis	OEBA	A	2	5.5		4.6	1.3	4.2	ns

## operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT	
			TYP	TYP		
	Power dissipation conseitance	Outputs enabled		44	54	- 5
C <sub>pd</sub> Power dissipation capacitance		Outputs disabled	CL = 50 pF, f = 10 MHz	6	6	pF



## SN74ALVCH16501 **18-BIT UNIVERSAL BUS TRANSCEIVER** WITH 3-STATE OUTPUTS SCES024A - JULY 1995 - REVISED NOVEMBER 1996



NOTES: A. CI includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



## SN74ALVCH16600 **18-BIT UNIVERSAL BUS TRANSCEIVER** WITH 3-STATE OUTPUTS SCES030A - JULY 1995 - REVISED NOVEMBER 1996

<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	DGG OR DL PACKAGE (TOP VIEW)	
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>		
<ul> <li>UBT™ (Universal Bus Transceiver)</li> <li>Combines D-Type Latches and D-Type</li> <li>Flip-Flops for Operation in Transparent,</li> </ul>	A1 3 54 B1 GND 4 53 GND A2 5 52 B2	
<ul> <li>Latched, Clocked, or Clock-Enabled Mode</li> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds</li> </ul>	A3 6 51 B3 V <sub>CC</sub> 7 50 V <sub>CC</sub> A4 8 49 B4	
200 V Using Machine Model (C = 200 pF, R = 0)	A5 9 48 B5 A6 10 47 B6	
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	GND [] 11 46 [] GND A7 [] 12 45 [] B7	
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	A8 0 13 44 B8 A9 0 14 43 B9 A10 0 15 42 0 B10	
<ul> <li>Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages</li> </ul>	A11 16 41 B11 A12 17 40 B12 GND 18 39 GND	
description	A13 19 38 B13 A14 20 37 B14 A15 21 36 B15	
This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V $V_{CC}$ operation.	V <sub>CC</sub> [ 22 35] V <sub>CC</sub> A16 [ 23 34] B16	
The SN74ALVCH16600 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.	A17 24 33 B17 GND 25 32 GND A18 26 31 B18	
Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable	OEBA [] 27 30 ] CLKBA LEBA [] 28 29 ] CLKENBA	

BA (<u>1</u>28 output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B

data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output enable OEAB is active low. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16600 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16600 is characterized for operation from -40°C to 85°C.

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## SN74ALVCH16600 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES030A – JULY 1995 – REVISED NOVEMBER 1996

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	-0.5.V to 4.6.V
Input voltage range, VI: Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	–0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, IIK (VI < 0)	–50 mA
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	
Continuous current through each V <sub>CC</sub> or GND	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 3): DGG pa	ckage 1 W
DL pack	age 1.4 W
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	v
V	High-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v
VIH		V <sub>CC</sub> = 2.7 V to 3.6 V	2		v
V.,	VIL Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
۷IL		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	v
٧I	Input voltage		0	VCC	v
Vo	Output voltage		0	VCC	v
	High-level output current	V <sub>CC</sub> = 2.3 V		-12	
ЮН		V <sub>CC</sub> = 2.7 V		-12	mA
		V <sub>CC</sub> = 3 V		24	
		V <sub>CC</sub> = 2.3 V		12	
IOL	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
		V <sub>CC</sub> = 3 V		24	
∆t/∆v	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



## SN74ALVCH16600 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES030A – JULY 1995 – REVISED NOVEMBER 1996

## switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM TO (INPUT) (OUTPUT)		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX		
fmax			150		150		150		MHz
	A or B	B or A	1	5.7		4.7	1	4	
<sup>t</sup> pd	LEAB or LEBA	A or B	1	6.5		5.5	1	4.8	ns
	CLKAB or CLKBA	A or B	1.4	7.9		6.8	1.3	5.7	
ten	OEAB or OEBA	A or B	1.1	7.1		6.3	1.1	5.2	ns
<sup>t</sup> dis	OEAB or OEBA	A or B	1.7	5.7		4.7	1.2	4.4	ns

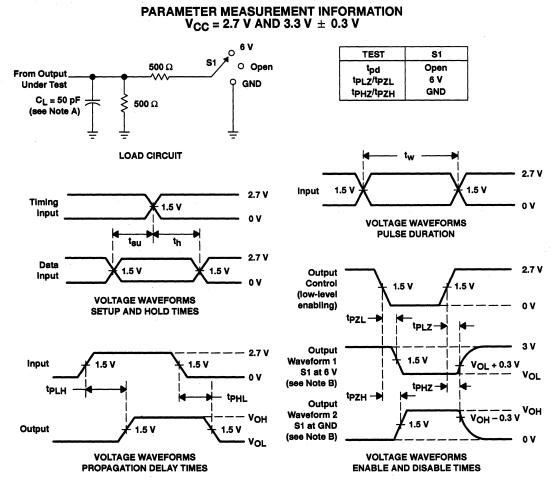
## operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT	
			TYP	TYP		
		Outputs enabled	C = = = = = = = = = = = = = = = = = = =	43	56	pF
Cpd Power dissipation capacitance		Outputs disabled	C <sub>L</sub> = 50 pF, f = 10 MHz	6	6	



## SN74ALVCH16600 **18-BIT UNIVERSAL BUS TRANSCEIV** WITH 3-STATE OUTPUTS

SCES030A - JULY 1995 - REVISED NOVEMBER 1996



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzi and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms



## SN74ALVCH16601 **18-BIT UNIVERSAL BUS TRANSCEIVER** WITH 3-STATE OUTPUTS

SCES027A - JULY 1995 - REVISED NOVEMBER 1996

● Member of the Texas Instruments Widebus™ Family	DGG OR DL PACKAGE (TOP VIEW)	
<ul> <li>UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode</li> </ul>	OEAB 1 56 CLKENAB LEAB 2 55 CLKAB A1 3 54 B1	
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	GND 4 53 GND A2 5 52 B2 A3 6 51 B3	
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	V <sub>CC</sub> [ 7 50 ] V <sub>CC</sub> A4 [ 8 49 ] B4 A5 [ 9 48 ] B5	
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds</li> </ul>	A6 [ 10 47 ] B6 GND [ 11 46 ] GND	
200 V Using Machine Model (C = 200 pF, R = 0) • Latch-Up Performance Exceeds 250 mA	A7 [] 12 45 [] B7 A8 [] 13 44 [] B8 A9 [] 14 43 [] B9	
Per JEDEC Standard JESD-17     Package Options Include Plastic 300-mil	A10 15 42 B10 A11 16 41 B11	
Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages	A12 17 40 B12 GND 18 39 GND A13 19 38 B13	
description	A14 0 20 37 0 B14 A15 0 21 36 0 B15	
This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V $V_{CC}$ operation.	V <sub>CC</sub> [] 22 35 [] V <sub>CC</sub> A16 [] 23 34 [] B16	
The SN74ALVCH16601 combines D-type latches and D-type flip-flops to allow data flow in	A17 [ 24 33 ] B17 GND [ 25 32 ] GND A18 [ 26 31 ] B18	
transparent, latched, and clocked modes. Data flow in each direction is controlled by	OEBA [] 27 30 ]] CLKBA LEBA [] 28 29 ]] CLKENBA	

output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and

CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable OEAB is active low. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16601 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16601 is characterized for operation from -40°C to 85°C.

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## SN74ALVCH16601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES027A – JULY 1995 – REVISED NOVEMBER 1996

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	
Input voltage range, VI: Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	–0.5 V to V <sub>CC</sub> + 0.5 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	$\dots \dots \dots -0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, IIK (VI < 0)	–50 mA
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V <sub>CC</sub> or GND	
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG pack	kage 1 W
DL packa	ge 1.4 W
Storage temperature range, T <sub>sto</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	v
V		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v
VIH	High-level input voltage V <sub>CC</sub> = 2.7 V to 3.6 V	2		v	
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
VIL	Low-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	v
Vi	Input voltage		0	VCC	v
Vo	Output voltage		0	VCC	v
	High-level output current	V <sub>CC</sub> = 2.3 V		-12	
юн		V <sub>CC</sub> = 2.7 V		-12	mA
		V <sub>CC</sub> = 3 V		-24	
		V <sub>CC</sub> = 2.3 V		12	
IOL	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
		V <sub>CC</sub> = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



## SN74ALVCH16601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES027A – JULY 1995 – REVISED NOVEMBER 1996

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figures 1 and 2)

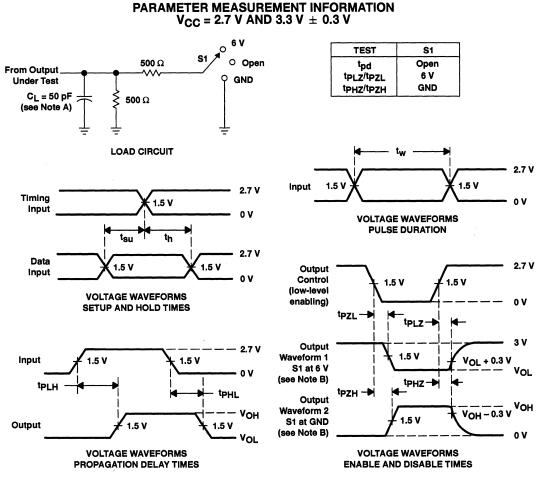
PARAMETER	FROM TO (INPUT) (OUTPUT)		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX		
fmax			150		150		150		MHz
	A or B	B or A	1.3	4.9		4.6		4.1	
<sup>t</sup> pd	LEAB or LEBA	A or B	1.2	5.6		5.3		4.7	ns
·	CLKAB or CLKBA	A or B	1.7	6.2		5.8		5	
<sup>t</sup> en	OEAB or OEBA	A or B	1.2	6.1		6.1		5.2	ns
<sup>t</sup> dis	OEAB or OEBA	A or B	2.1	5.4		4.8		4.4	ns

## operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT		
				TYP	TYP	L	
	Bower dissinction expectance	Outputs enabled	Ci = 50 pF. f = 10 MHz	41	52	٥F	
C <sub>pd</sub> Power dissipation capacitance	Outputs disabled	C <sub>L</sub> = 50 pF, f = 10 MHz	6	6	рг		



## SN74ALVCH16601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES027A – JULY 1995 – REVISED NOVEMBER 1996



- NOTES: A. CL includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpl 7 and tpH7 are the same as tdis.
  - F. tp71 and tp7H are the same as  $t_{en}$ .
  - G. tpLH and tpHL are the same as tpd.

#### Figure 2. Load Circuit and Voltage Waveforms



## SN74ALVCH162601 **18-BIT UNIVERSAL BUS TRANSCE** WITH 3-STATE OUTPUTS SCES026A - JULY 1995 - REVISED NOVEMBER 1996

● Member of the Texas Instruments <i>Widebus</i> ™ Family	DGG OR DL PACKAGE (TOP VIEW)	
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	OEAB 1 56 CLKENAB	Ī
<ul> <li>UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode</li> </ul>	A1 0 3 54 0 B1 GND 0 4 53 0 GND A2 0 5 52 0 B2	
<ul> <li>Output Ports Have Equivalent 26-Ω Series Resisters, So No External Resistors Are Required</li> </ul>	A3 [] 6 51 [] B3 V <sub>CC</sub> [] 7 50 ] V <sub>CC</sub> A4 [] 8 49 ] B4 A5 [] 9 48 [] B5	
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)</li> </ul>	A6 L 10 47 L B6 GND L 11 46 L GND A7 L 12 45 L B7 A8 L 13 44 L B8	
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	A9 1 13 44 1 B8 A9 1 14 43 1 B9 A10 15 42 1 B10	
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	A11 1 16 41 B11 A12 17 40 B12 GND 18 39 GND	
<ul> <li>Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages</li> </ul>	A13 [ 19 38 ] B13 A14 [ 20 37 ] B14 A15 [ 21 36 ] B15 V <sub>CC</sub> [ 22 35 ] V <sub>CC</sub>	
description	A16 23 34 B16	
This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V <sub>CC</sub> operation.	A17 [ 24 33 ] B17 GND [ 25 32 ] GND A18 [ 26 31 ] B18	
The SN74ALVCH162601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.	OEBA [] 27 30 [] CLKBA LEBA [] 28 29 [] CLKENBA	2

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

The B-port outputs include  $26 \Omega$  series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

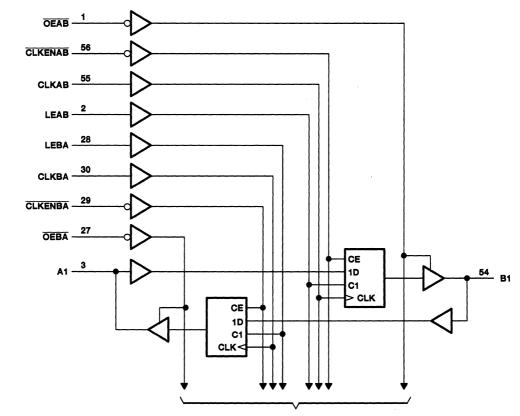
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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logic diagram (positive logic)

To 17 Other Channels



## SN74ALVCH162601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES026A – JULY 1995 – REVISED NOVEMBER 1996

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	Vcc	MIN TYPT	MAX	UNIT
	IOH = −100 µA		2.3 V to 3.6 V	V <sub>CC</sub> -0.2		
	I <sub>OH</sub> =4 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	1.9		
( <b>D</b> )		V <sub>IH</sub> = 1.7 V	2.3 V	1.7		.,
VOH (B port)	l <sub>OH</sub> = -6 mA	V <sub>IH</sub> = 2 V	3 V	2.4		v
	IOH =8 mA,	V <sub>IH</sub> = 2 V	2.7 V	2		
	lOH = −12 mA,	V <sub>IH</sub> = 2 V	3 V	2		
	lOH = -100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -0.2		
	1 <sub>OH</sub> =6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2		
\/ /A == ===\		V <sub>IH</sub> = 1.7 V	2.3 V	1.7		
V <sub>OH</sub> (A port)	port) I <sub>OH</sub> = -12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2		v
		V <sub>IH</sub> = 2 V	3 V	2.4		
	I <sub>ОН</sub> = -24 mA,	V <sub>IH</sub> = 2 V	3 V	2		
	l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V		0.2	
	$I_{OL} = 4 \text{ mA},$	V <sub>IL</sub> = 0.7 V	2.3 V		0.4	
· · · ·		V <sub>IL</sub> = 0.7 V	2.3 V		0.55	
V <sub>OL</sub> (B port)	$I_{OL} = 6 \text{ mA}$	V <sub>IL</sub> = 0.8 V	3 V		0.55	v
	I <sub>OL</sub> = 8 mA,	V <sub>IL</sub> = 0.8 V	2.7 V		0.6	
	I <sub>OL</sub> = 12 mA,	, V <sub>IL</sub> = 0.8 V	3 V		0.8	
	l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V		0.2	
	$I_{OL} = 6 \text{ mA},$	V <sub>IL</sub> = 0.7 V	2.3 V		0.4	
VOL (A port)		V <sub>IL</sub> = 0.7 V	2.3 V		0.7	v
	l <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.8 V	2.7 V		0.4	0.4
	I <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V		0.55	
11	$V_{I} = V_{CC}$ or GND		3.6 V		±5	μA
- <u></u>	V <sub>I</sub> = 0.7 V			45		
	V <sub>I</sub> = 1.7 V		2.3 V	-45		
li(hold)	VI = 0.8 V			75		μA
((1010)	VI = 2 V		3 V	-75		,
	$V_1 = 0$ to 3.6 V <sup>‡</sup>				±500	
loz§	V <sub>O</sub> = V <sub>CC</sub> or GND		3.6 V	[	±10	μA
	$V_{I} = V_{CC}$ or GND,	lO = 0	3.6 V		40	μA
	One input at V <sub>CC</sub> – 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V	1	750	μA
Ci Control inputs	$V_{I} = V_{CC}$ or GND		3.3 V	4		pF
Cio A or B ports	$V_{O} = V_{CC} \text{ or } GND$		3.3 V	8		pF

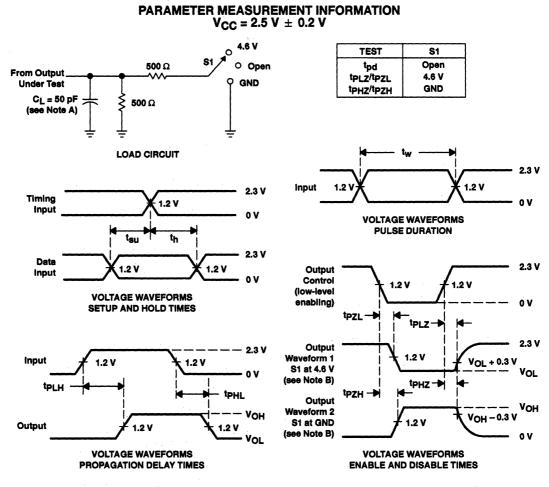
<sup>†</sup> All typical values are measured at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

<sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

§ For I/O ports, the parameter IOZ includes the input leakage current.



## SN74ALVCH162601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES026A – JULY 1995 – REVISED NOVEMBER 1996



- NOTES: A. CL includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



## SN74ALVCH16901 18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS SCES010B – JULY 1995 – REVISED NOVEMBER 1996

<ul> <li>Member of the Texas Instruments Widebus+™ Family</li> </ul>	DGG PACKAGE (TOP VIEW)	
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>		LKENBA
<ul> <li>UBT™ (Universal Bus Transceiver)</li> <li>Combines D-Type Latches and D-Type</li> <li>Flip-Flops for Operation in Transparent,</li> </ul>	CLKAB [] 3 62 [] CL 1 ERRA [] 4 61 [] 1 E	KBA RRB
Latched, or Clocked Mode	1APAR 5 60 1B GND 6 59 GN	
<ul> <li>Simultaneously Generates and Checks Parity</li> </ul>	1A1 0 7 58 1B 1A2 0 8 57 1B	1
Option to Select Generate Parity and Check	1A3 🚺 9 56 🗋 1B3	3
or Feed-Through Data/Parity in A-to-B or B-to-A Directions	V <sub>CC</sub> [] 10 55 [] V <sub>C</sub> 1A4 [] 11 54 [] 1B	
ESD Protection Exceeds 2000 V Per	1A5 🚺 12 53 🚺 1B	5
MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF,	1A6 [] 13 52 [] 1B0 GND [] 14 51 [] GN	
R = 0)		
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	1A8 0 16 490 1B 2A1 0 17 480 2B	
Bus Hold on Data Inputs Eliminates the	2A2 1 18 47 2B GND 19 46 GN	
Need for External Pullup/Pulldown Resistors	2A3 20 45 2B	
Packaged in Thin Shrink Small-Outline	2A4 [ 21 44 ] 2B 2A5 [ 22 43 ] 2B	
Package	V <sub>CC</sub> [] 23 42 [] V <sub>C</sub>	
description	2A6 24 41 2B 2A7 25 40 2B	
This 18-bit (dual-octal) noninverting registered	2A8 🛛 26 39 🗍 2B	8
transceiver is designed for 2.3-V to 3.6-V V <sub>CC</sub> operation.	GND 27 38 GN 2APAR 28 37 28	PAR
The SN74ALVCH16901 is a dual 9-bit to dual 9-bit parity transceiver with registers. The device can	2ERRA [] 29 36 ]] 2E OEAB [] 30 35 ]] OE	BA
operate as a feed-through transceiver or it can generate/check parity from the two 8-bit data		D/EVEN

The SN74ALVCH16901 features independent clock (CLKAB or CLKBA), latch-enable (LEAB or LEBA), and dual 9-bit clock-enable (CLKENAB or CLKENBA) inputs. It also provides parity-enable (SEL) and parity-select (ODD/EVEN) inputs and separate error-signal (ERRA or ERRB) outputs for checking parity. The direction of data flow is controlled by OEAB and OEBA. When SEL is low, the parity functions are enabled. When SEL is high, the parity functions are disabled and the device acts as an 18-bit registered transceiver.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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buses in either direction.



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## SN74ALVCH16901 18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS 996

SCES01	0B - JULY	1995 – RE	VISED	NOVEME	JER 1	9

FUNCTION TABLET								
	INPUTS							
CLKENAB	OEAB	LEAB	CLKAB	A	В			
Х	н	х	х	Х	Z			
x	L	н	х	L	L			
X	L	н	х	н	н			
н	L	L	х	х	в <sub>0</sub> ‡			
L	L	L	↑	L	L			
L	L	L	↑	н	н			
L	L	L	L	х	в <sub>0</sub> ‡			
L	L	L	н	х	в <sub>0</sub> ‡ в <sub>0</sub> §			

#### FUNCTION TABLET

<sup>†</sup>A-to-B data flow is shown: B-to-A flow is similar, but uses OEBA, LEBA, and CLKENBA.

<sup>‡</sup> Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low



## SN74ALVCH16901 **18-BIT UNIVERSAL BUS TRANSCEIVER** WITH PARITY GENERATORS/CHECKERS SCES010B - JULY 1995 - REVISED NOVEMBER 1996

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	
Input voltage range, VI: Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2	–0.5 V to V <sub>CC</sub> + 0.5 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	–0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (VI < 0)	
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	
Continuous current through each V <sub>CC</sub> or GND	
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3)	
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book.

### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
V	High-level input voltage		1.7		v
VIH	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2		v
VIL	Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
۲IL		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	v
Vj -	Input voltage		0	Vcc	V
Vo	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 2.3 V		-12	2 mA
ЮН	High-level output current	V <sub>CC</sub> = 2.7 V		-12	
		V <sub>CC</sub> = 3 V		-24	
	Low-level output current	V <sub>CC</sub> = 2.3 V		12	
IOL		V <sub>CC</sub> = 2.7 V		12	mA
		V <sub>CC</sub> = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



## SN74ALVCH16901 **18-BIT UNIVERSAL BUS TRANSCEIVER** WITH PARITY GENERATORS/CHECKERS SCES010B - JULY 1995 - REVISED NOVEMBER 1996

# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figures 1 and 2)

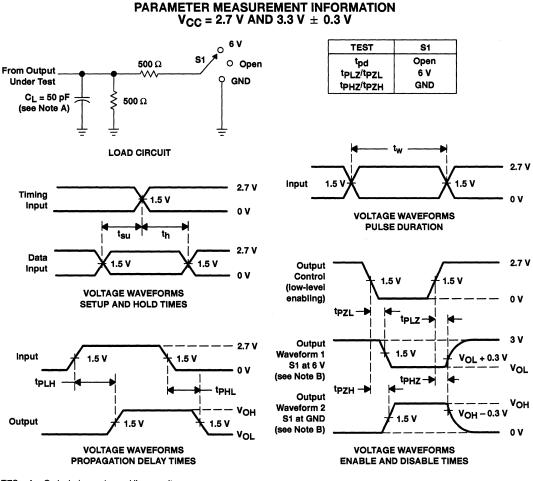
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = ± 0.3		UNIT
	(INPUT)	(001901)	MIN	MAX	MIN	MAX	MIN	MAX	
fmax			125		125		125		MHz
	A or B	B or A	1.5	5.8		4.8	1	4.4	
	A or B	BPAR or APAR	2.5	9.5		7.6	2	6.7	
	APAR or BPAR	BPAR or APAR	1.5	6.3		5.2	1	4.7	
	APAR or BPAR	ERRA or ERRB	2.5	10.3		8.7	2	7.5	
	ODD/EVEN	ERRA or ERRB	2	9.3		7.9	1.5	6.8	
	ODD/EVEN	BPAR or APAR	2	8.9		7.6	1.5	6.5	
	SEL	BPAR or APAR	1.5	6.7		5.9	1	5.1	
	CLKAB or CLKBA	A or B	1.5	7		5.8	1	5.1	
<sup>t</sup> pd	CLKAB or CLKBA	BPAR or APAR parity feedthrough	2	7.7		6.3	1.5	5.6	ns
	CLKAB or CLKBA	BPAR or APAR parity generated	3	10.8		8.7	2	7.7	
	CLKAB or CLKBA	ERRA or ERRB	3	11.1		8.9	2	7.9	
	LEAB or LEBA	A or B	1.5	6.6		5.5	1	4.8	
	LEAB or LEBA	BPAR or APAR parity feedthrough	2	7.3		6	1.5	5.3	
	LEAB or LEBA	BPAR or APAR parity generated	3	10.4		8.3	2	7.4	
	LEAB or LEBA	ERRA or ERRB	3	10.5		8.5	2	7.5	
ten	OEAB or OEBA	B, BPAR or A, APAR	1.5	6.8		6.1	1	5.3	ns
tdis	OEAB or OEBA	B, BPAR or A, APAR	2	6.3		5.2	1.5	4.9	ns
ten	OEAB or OEBA	ERRA or ERRB	1.5	6.7		5.5	1	4.9	ns
tdis	OEAB or OEBA	ERRA or ERRB	2	7.5		6.5	1	5.7	ns
ten	SEL	ERRA or ERRB	1.5	7.2		6.5	1	5.5	ns
tdis	SEL	ERRA or ERRB	2	6.6		5.4	1.5	4.9	ns

### operating characteristics, $T_A = 25^{\circ}C$

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V TYP	V <sub>CC</sub> = 3.3 V ± 0.3 V TYP	UNIT
	Power dissipation capacitance	Outputs enabled	0 50-5	22	27	
Cpd	-ower dissipation capacitance	Outputs disabled	C <sub>L</sub> = 50 pF, f = 10 MHz	5	8	pF



#### SN74ALVCH16901 18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS SCES010B – JULY 1995 – REVISED NOVEMBER 1996



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

#### Figure 2. Load Circuit and Voltage Waveforms



#### SN54LVT16500, SN74LVT16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS146D - MAY 1992 - REVISED NOVEMBER 1996

<ul> <li>State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power</li> </ul>	SN54LVT16500 WD PACKAGE SN74LVT16500 DGG OR DL PACKA (TOP VIEW)	GE
Dissipation		
<ul> <li>Members of the Texas Instruments</li> </ul>		
<i>Widebus</i> ™ Family	$\begin{array}{c} \text{LEAB} U^2 \qquad 55 \text{ IJ} \text{ CLRAB} \\ \text{A1} \text{ IJ} 3 \qquad 54 \text{ IJ} \text{ B1} \end{array}$	
<ul> <li>Support Mixed-Mode Signal Operation (5-V</li> </ul>	GND 4 53 GND	
Input and Output Voltages With 3.3-V $V_{CC}$ )	A2 1 5 52 B2	
<ul> <li>Support Unregulated Battery Operation</li> </ul>	A3 6 51 B3	
Down to 2.7 V		
● UBT™ (Universal Bus Transceiver)		
Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent,	A6 1 10 47 B6	
Latched, or Clocked Mode		
	A7 1 12 45 B7	
• Typical V <sub>OLP</sub> (Output Ground Bounce)	A8 1 13 44 B8	
< 0.8 V at V <sub>CC</sub> = 3.3 V, T <sub>A</sub> = 25°C	A9 🛛 14 43 🗍 B9	
ESD Protection Exceeds 2000 V Per	A10 15 42 B10	
MIL-STD-883, Method 3015; Exceeds 200 V	A11 16 41 B11	
Using Machine Model	A12 17 40 B12	
(C = 200 pF, R = 0)	GND 🚺 18 39 🗍 GND	
<ul> <li>Latch-Up Performance Exceeds 500 mA</li> </ul>	A13 🛛 19 🛛 38 🗍 B13	
Per JEDEC Standard JESD-17	A14 🖸 20 🛛 37 🖥 B14	
<ul> <li>Bus Hold on Data Inputs Eliminates the</li> </ul>	A15 🛛 21 36 🗋 B15	
Need for External Pullup/Pulldown	V <sub>CC</sub> <b>[</b> 22 35 <b>]</b> V <sub>CC</sub>	
Resistors	A16 🛛 23 🛛 34 🗋 B16	
<ul> <li>Support Live Insertion</li> </ul>	A17 🛛 24 🛛 33 🗍 B17	
<ul> <li>Distributed V<sub>CC</sub> and GND Pin Configuration</li> </ul>	GND 🛛 25 32 🗍 GND	
Minimizes High-Speed Switching Noise	A18 🛛 26 🛛 31 🗋 B18	
<ul> <li>Flow-Through Architecture Optimizes</li> </ul>		
PCB Layout	LEBA [28 29] GND	

Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

#### description

The 'LVT16500 are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

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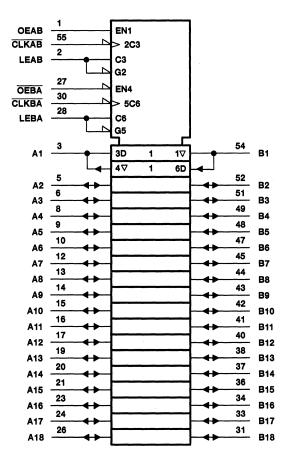
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#### SN54LVT16500, SN74LVT16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS146D - MAY 1992 - REVISED NOVEMBER 1996

logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



## SN54LVT16500, SN74LVT16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS146D - MAY 1992 - REVISED NOVEMBER 1996

#### recommended operating conditions (see Note 4)

· · ·			SN54LV	T16500	SN74LV	T16500	UNIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	Ŷ	2		V
VIL	Low-level input voltage			<b>Ø</b> .8		0.8	V
VI	Input voltage			§ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$		5.5	V
ЮН	High-level output current		Q.			-32	mA
IOL	Low-level output current		- <u>S</u>	48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled	S.	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Fasts instruments reserves the right to change or discontinue these products without notice.



#### SN54LVT16500, SN74LVT16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS146D - MAY 1992 - REVISED NOVEMBER 1996

# timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				SN54LV	T16500			SN74LV	T16500		
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
<sup>f</sup> clock	Clock frequency		0	150	0	125	0	150	0	125	MHz
	Pulse duration	LE high	3.3		3.3		3.3		3.3		ns
tw	Puise duration	CLK high or low	3.3		33		3.3		3.3		115
		A before CLKAB↓	1.8		A.1		1.8		1.1		
	O a trans there a	B before CLKBA↓	1.9	5	1.2		1.9		1.2		
t <sub>su</sub>	Setup time	A or B before LE↓ , CLK high	2.2	Č,	1.3		2.2		1.3		ns
		A or B before LE $\downarrow$ , CLK low	2.7	Ĵ,	1.9		2.7		1.9		
٠.	Hold time	A or B after CLK↓	1.2	\$	1.2		1.2		1.2		
th		A or B after LE↓	0.9		1.1		0.9		1.1		ns

#### switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

				SN54LV	T16500			SN7	4LVT16	500		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.		V <sub>CC</sub> =	2.7 V		C = 3.3 ± 0.3 V	v	V <sub>CC</sub> =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
fmax			150		125		150			125		MHz
<sup>t</sup> PLH	B or A	A or B	1.7	5.8		7	1.7	3	5.4		6.8	ns
<sup>t</sup> PHL	BORA	AOLB	1.6	6	Â	7.8	1.6	3.2	5.9		7.7	115
<sup>t</sup> PLH	LEBA or LEAB	A or B	2.3	7.3	Ð	8.9	2.3	4	7		8.5	ns
<sup>t</sup> PHL	LEBA OF LEAB	AUB	2.7	8.2		9.8	2.7	4.3	7.9		9.7	115
<sup>t</sup> PLH	CLKBA or	A or B	2	7.40	•	8.8	2	4.1	7		8.3	ns
<sup>t</sup> PHL	CLKAB	AOLP	2.4	<b>8</b> )		10	2.4	4.4	7.9		9.9	115
<sup>t</sup> PZH	OEBA or	A or B	1.2	\$5.2		6.1	1.2	3	5		5.9	
<sup>t</sup> PZL	OEAB	AOLB	1.5	ົ 5.9		7	1.5	3	5.8		6.9	ns
<sup>t</sup> PHZ	OEBA or	A or B	2.7	7.7		8.6	2.7	4.6	7.4		8.3	
<sup>t</sup> PLZ	OEAB	AOLP	2.8	7.3		7.7	2.8	4.7	6.7		7.2	ns

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notice.



#### SN54LVT16501, SN74LVT16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS147G - MAY 1992 - REVISED NOVEMBER 1996

<ul> <li>State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power</li> </ul>	SN54LVT16501 SN74LVT16501 DGG (TOP VIE	OR DL PACKAGE
Dissipation		56 GND
<ul> <li>Members of the Texas Instruments</li> </ul>		55 CLKAB
<i>Widebus</i> ™ Family		54 B1
<ul> <li>Support Mixed-Mode Signal Operation (5-V</li> </ul>		53 GND
Input and Output Voltages With 3.3-V V <sub>CC</sub> )		52 B2
<ul> <li>Support Unregulated Battery Operation</li> </ul>		51 B3
Down to 2.7 V		50 V <sub>CC</sub>
		49 B4
● UBT™ (Universal Bus Transceiver)		48 B5
Combines D-Type Latches and D-Type		47 B6
Flip-Flops for Operation in Transparent,		46 GND
Latched, or Clocked Mode		45 B7
<ul> <li>Typical V<sub>OLP</sub> (Output Ground Bounce)</li> </ul>		44 B8
< 0.8 V at V <sub>CC</sub> = 3.3 V, T <sub>A</sub> = 25°C		43 B9
<ul> <li>ESD Protection Exceeds 2000 V Per</li> </ul>		42 B10
MIL-STD-883, Method 3015; Exceeds 200 V		41 B11
Using Machine Model		40 <b>1</b> B12
(C = 200 pF, R = 0)		39 GND
<ul> <li>Latch-Up Performance Exceeds 500 mA</li> </ul>		38 B13
Per JEDEC Standard JESD-17		37 B14
<ul> <li>Bus Hold on Data Inputs Eliminates the</li> </ul>		36 B15
Need for External Pullup/Pulldown		35 V <sub>CC</sub>
Resistors	A16 23	34 B16
<ul> <li>Support Live Insertion</li> </ul>		33 B17
••		32 GND
<ul> <li>Distributed V<sub>CC</sub> and GND Pin Configuration</li> <li>Minimizes High Speed Switching Noise</li> </ul>		31 B18
Minimizes High-Speed Switching Noise		30 CLKBA
<ul> <li>Flow-Through Architecture Optimizes PCB Layout</li> </ul>		29 GND

 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

#### description

The 'LVT16501 are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

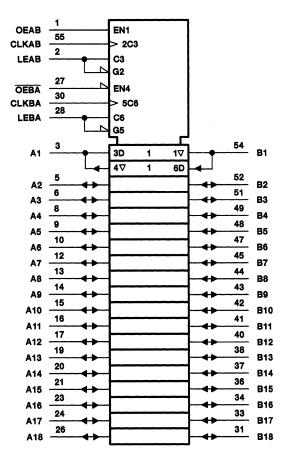
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## SN54LVT16501, SN74LVT16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS147G - MAY 1992 - REVISED NOVEMBER 1996

logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



## SN54LVT16501, SN74LVT16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS147G - MAY 1992 - REVISED NOVEMBER 1996

#### recommended operating conditions (see Note 4)

			SN54L	/T16501	SN74LV	T16501	UNIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
٧I	Input voltage			5.5		5.5	. <b>V</b>
ЮН	High-level output current			-24		-32	mA
IOL	Low-level output current		T	48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



#### SN54LVT16501, SN74LVT16501 **3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS** WITH 3-STATE OUTPUTS SCBS147G - MAY 1992 - REVISED NOVEMBER 1996

				SN54LV	T16501			SN74LV	T16501		
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	125	0	150	0	125	MHz
	Pulse duration	LE high	3.3		3.3		3.3		3.3		ns
tw Pulse du	Puise duration	CLK high or low	3.3		3.3		3.3		3.3		ns
		A before CLKAB1	1.6		2.1		1.6		2.1		
	<b>.</b>	B before CLKBA↑	1.6		2.1		1.6		2.1		
t <sub>su</sub>	Setup time	A or B before LE↓, CLK high	3.1		2.7		2.6		1.9		ns
		A or B before LE↓, CLK low	2.6		2.0		2		1.3		
٠.	Hold time	A or B after CLK1	2		2.1		2		2.1		
th	Hold time	A or B after LE↓	1.3		1.2		0.9		1.2		ns

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

## switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

			T	SN54LV	T16501			SN7	4LVT16	501		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.		V <sub>CC</sub> =	2.7 V	V	CC = 3.3 ± 0.3 V	V	V <sub>CC</sub> =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
fmax			150		125		150			125		MHz
<sup>t</sup> PLH	D	A or B	1.7	5.4		6.8	1.7	3	5.4		6.8	ns
<sup>t</sup> PHL	B or A	AOrb	1.6	6		7.8	1.6	3.2	5.9		7.7	ns
<sup>t</sup> PLH		A or B	2.3	7.3		9	2.3	4	7		8.5	ns
<sup>t</sup> PHL	LEBA or LEAB	A or B	2.7	8.2		9.8	2.7	4.3	7.9		9.7	13
<sup>t</sup> PLH	CLKBA or	A or B	2.5	8.3		9.7	2.5	4.1	7.9		9.2	ns
<sup>t</sup> PHL	CLKAB	AOD	3.5	9.4		10.7	3.5	5.4	8.9		10.4	ns
<sup>t</sup> PZH	0501	A or B	1.2	5.1		6.1	1.2	3	5		5.9	
<sup>t</sup> PZL	OEBA or OEAB	A OF B	1.5	5.9		7	1.5	3	5.8		6.9	ns
<sup>t</sup> PHZ	OEBA or OEAB	A or B	2.7	7.5		8.5	2.7	4.6	7.4		8.3	
<sup>t</sup> PLZ	UEBA OF UEAB	A of B	2.8	6.8		7.5	2.8	4.7	6.7		7.2	ns

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.



#### SN74ALVCH16524 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES080 - JULY 1996

	501
● Member of the Texas Instruments Widebus™ Family	DGG OR DL PACKAGE (TOP VIEW)
<ul> <li>EPIC ™ (Enhanced-Performance Implante CMOS) Submicron Process</li> </ul>	d GND 1 56 GND OEAB 2 55 SEL
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 Using Machine Model (C = 200 pF, R = 0)</li> </ul>	A1 [] 3 54 [] B1 GND [] 4 53 [] GND
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	A2 [] 5 52 [] B2 A3 [] 6 51 [] B3 V <sub>CC</sub> [] 7 50 [] V <sub>CC</sub>
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	A4 [] 8 49 [] B4 A5 [] 9 48 [] B5 A6 [] 10 47 [] B6
<ul> <li>Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrini Small-Outline (DGG) Packages</li> </ul>	GND 11 46 GND
description	A9 [] 14 43 [] B9 A10 [] 15 42 [] B10 A11 [] 16 41 [] B11
This 18-bit universal bus transceiver is design for 2.3-V to 3.6-V V <sub>CC</sub> operation.	AT 1 16 41 BT AT 2 17 40 B12 GND 18 39 GND
Data flow in each direction is controlled output-enable (OEAB and OEBA) and cl enable (CLKENBA) inputs. For the A-to-B d	DCK A14 🛛 20 37 🗋 B14
flow, the data flows through a single register. B-to-A data can flow through a four-stage pipe	The V <sub>CC</sub> [ 22 35 ] V <sub>CC</sub> ine A16 [ 23 34 ] B16
register path, or through a single register pa depending on the state of SEL. Data is stored in the internal registers on	

Data is stored in the internal registers on the low-to-high transition of the CLK input, provided that the appropriate CLKENBA input is low. The B-to-A data transfer is synchronized with the CLK input.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16524 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16524 is characterized for operation from -40°C to 85°C.

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30 CLK

29 GND

OEBA 27

CLKENBA 28

#### FUNCTION TABLE B-TO-A STORAGE (OEBA = L)

	INPUTS									
CLKENBA	CLK	SEL	В	A						
н	х	х	х	A0 <sup>†</sup>						
L	ſ	н	L	Ł						
L	î	н	н	н						
L	î	L	L	L‡						
L	ſ	L	н	н‡						

<sup>†</sup>Output level before the indicated steady-state input conditions were established

<sup>‡</sup>Four positive CLK edges are needed to propagate data

from B to A when SEL is low.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V <sub>CC</sub>	–0.5 V to 4.6 V
Input voltage range, V <sub>1</sub> (see Note 1)	–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 3):	DGG package 1 W
	DL package 1.4 W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. This value is limited to 4.6 V maximum.

 The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book.



#### SN74ALVCH16524 **18-BIT REGISTERED BUS TRANSCEIVER** WITH 3-STATE OUTPUTS SCES080 - JULY 1996

PARAMETER	TEST C	ONDITIONS	Vcc	MIN TYP	MAX	UNIT	
	l <sub>OH</sub> = – 100 µA		2.3 V to 3.6 V	V <sub>CC</sub> -0.2			
	I <sub>ОН</sub> = -6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2			
Maria		V <sub>IH</sub> = 1.7 V	2.3 V	1.7		v	
VOH	IOH = -12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2		v	
		V <sub>IH</sub> = 2 V	3 V	2.4			
	I <sub>ОН</sub> = -24 mA,	V <sub>IH</sub> = 2 V	3 V	2			
	l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V		0.2		
	I <sub>OL</sub> = 6 mA,	V <sub>IL</sub> = 0.7 V	2.3 V	1	0.4		
VOL	10 1	V <sub>IL</sub> = 0.7 V	2.3 V		0.7	v	
	l <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.8 V	2.7 V		0.4		
	I <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V		0.55		
1	V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V		±5	μA	
	V <sub>I</sub> = 0.7 V		0.01/	45			
	V <sub>I</sub> = 1.7 V		2.3 V	-45			
Ihold	V <sub>I</sub> = 0.8 V		0.1	75		μA	
	V <sub>1</sub> = 2 V		- 3V	-75			
	V <sub>I</sub> = 0 to 3.6 V <sup>‡</sup>				±500		
loz\$	VO = VCC or GND		3.6 V	· ·	±10	μA	
lcc	$V_{I} = V_{CC}$ or GND,	IO = 0	3.6 V		40	μA	
AICC	One input at V <sub>CC</sub> - 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V		750	μA	
Ci Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V	:	3	pF	
Co A or B ports	Vo = Vcc or GND		3.3 V	-	7	pF	

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3, T<sub>Å</sub> = 25°C.
 <sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

 $\$  For I/O ports, the parameter I\_OZ includes the input leakage current.

#### timing requirements over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

			VCC = ±0.2		V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = ± 0.3		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
<sup>f</sup> clock	Clock frequency		0	120	0	125	0	150	MHz
tw	Pulse duration, CLK high or low		3.2		3.2		3		ns
		B data before CLK1	1.5		1.2		1.1		
t <sub>su</sub>	Setup time	SEL before CLK1	2.7		2.4		2.1		ns
		CLKENBA before CLK1	2.7		2.6		2		
		B data after CLK↑	1		0.6		1.2		
th	Hold time	SEL after CLK↑	0.5		0.2		0.8		ns
		CLKENBA after CLK1	0.1		0.1		0.3		



#### SN74ALVCH16524 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCE5080 - JULY 1996

PARAMETER MEASUREMENT INFORMATION  $V_{CC} = 2.5 V \pm 0.2 V$ 4.6 V 0 TEST **S1 S1** O Open Open **500** Ω tpd From Output 4.6 V tPLZ/tPZL Under Test 0 GND GND tPHZ/tPZH CL = 50 pF Ş **500** Ω (see Note A) LOAD CIRCUIT tw 2.3 V 1.2 V Input 121 2.3 V Timing 0 V 1.2 V Input 0 V **VOLTAGE WAVEFORMS** PULSE DURATION t<sub>su</sub> th 2.3 V Data 1.2 V 2.3 V 1.2 V Output input 0 V Control .2 V 1.2 V (low-level **VOLTAGE WAVEFORMS** enabling) 0 V SETUP AND HOLD TIMES tPZL · tei 7 2.3 V Output 2.3 V Waveform 1 1.2 V Input 1.2 V VOL + 0.3 V 1.2 V S1 at 4.6 V VOL 0 V (see Note B) tPHZt<sub>PLH</sub> tPZH -> <sup>t</sup>PHL Output ۷он Waveform 2 VOH - 0.3 V VOH S1 at GND Output 1.2 V 1.2 V (see Note B) 0 V VOL **VOLTAGE WAVEFORMS** VOLTAGE WAVEFORMS **PROPAGATION DELAY TIMES** ENABLE AND DISABLE TIMES

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.
- a. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN74ALVCH16525 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES059A - NOVEMBER 1995 - REVISED NOVEMBER 1996

● Member of the Texas Instruments Widebus™ Family	DGG OR DL PACKAGE (TOP VIEW)		
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>		SEL	
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015;Exceeds 200V Using Machine Model (C = 200 pF, R = 0)</li> </ul>	A1 [] 3 54 GND [] 4 53	CLKAB B1 GND	
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	A3 🛛 6 51	B2 B3 V <sub>CC</sub>	
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	A4 🛛 8 49 A5 🖸 9 48	B4 B5 B6	
<ul> <li>Package Option Includes Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink</li> </ul>	GND 11 46 A7 12 45	GND B7	
Small-Outline (DGG) Packages description	A9 14 43 A10 15 42	B8 B9 B10	
This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V $V_{CC}$ operation.	A12 🛛 17 40	B11 B12 GND	
Data flow in each direction is controlled by output-enable (OEAB and OEBA) and clock- enable (CLKENAB and CLKENBA) inputs. For the	A14 🛛 20 37	B13 B14 B15	
A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a	V <sub>CC</sub> [22 35 A16 [23 34	V <sub>CC</sub> B16	
four-stage pipeline register path, or through a single register path, depending on the state of		B17 GND	

Data is stored in the internal registers on the low-to-high transition of the CLK input, provided that the appropriate CLKEN inputs are low. The A-to-B data transfer is synchronized to the CLKAB input, and B-to-A data transfer is synchronized with the CLK1BA and CLK2BA inputs.

SEL.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

A18 26

OEBA 27

CLKENBA 28

31 B18

30 CLK1BA

29 CLK2BA

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16525 is characterized for operation from -40°C to 85°C.

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#### **Function Tables**

#### A-TO-B STORAGE (OEAB = L)

I	OUTPUT		
CLKENAB	CLKAB	A	В
н	х	Х	B0 <sup>†</sup>
L	Ŷ	L	L
L	î	н	н

<sup>†</sup>Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE (OEBA = L)
---------------------------

	INPUTS					
CLKENBA	CLK2BA	CLK1BA	SEL	В	A	
н	х	х	х	х	A0 <sup>†</sup>	
L	↑	х	н	L	L	
L	ſ	х	н	н	н	
L	ſ	Ŷ	L	L	L‡	
L	î	Ŷ	L	н	н‡	

<sup>†</sup>Output level before the indicated steady-state input conditions were established

<sup>‡</sup> Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when SEL is low.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V <sub>CC</sub>	–0.5 V to 4.6 V
Input voltage range, V <sub>1</sub> (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V <sub>CC</sub> + 0.5 V
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3):	DGG package 1 W
	DL package 1.4 W
Storage temperature range, T <sub>stg</sub>	

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

 The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book.



#### SN74ALVCH16525 **18-BIT REGISTERED BUS TRANSCEIVER** WITH 3-STATE OUTPUTS SCES059A - NOVEMBER 1995 - REVISED NOVEMBER 1996

## timing requirements over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

				VCC = 2.5 V ±0.2 V		$CC = 2.7 V \qquad \begin{array}{c} V_{CC} = 3.3 V \\ \pm 0.3 V \end{array}$		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	
<sup>f</sup> clock	Clock frequency		0	120	0	125	0	150	MHz
tw	Pulse duration, CLK high or low		3.2		3.2		3		ns
		A data before CLKAB1	1.3		1.3		1.3		
	,	B data before CLK2BA↑	2.1		1.8		1.7		
		B data before CLK1BA1	1.3		1.2		1.1		
t <sub>su</sub>	Setup time	SEL before CLK2BA↑	3.3		3.3		3.3		ns
		CLKENAB before CLKAB1	2.1		1.9		1.6		
		CLKENBA before CLK1BA1	2.7		2.5		2.1		
		CLKENBA before CLK2BA1	2.7		2.5		2.2		
		A data after CLKAB1	0.7		0.4		0.9		
		B data after CLK2BA↑	0.4		0		0.6		
		B data after CLK1BA↑	0.8		0.4		1		
th	Hold time	SEL after CLK2BA↑	0		0		.0.1		ns
		CLKENAB after CLKAB <sup>↑</sup>	0.1		0.3		0.3		
		CLKENBA after CLK1BA1	0		0		0.1		
1		CLKENBA after CLK2BA1	0		0		0		

## switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = ± 0.3	3.3 V 3 V	UNIT
	(INFOT)	(001201)	MIN	MAX	MIN	MAX	MIN	MAX	
fmax			120		125		150		MHz
<sup>t</sup> pd	CLKAB or CLK2BA	A or B	1	5.1		4.4	1	4.2	ns
<sup>t</sup> en	OEAB or OEBA	A or B	1	6.6		6.1	1	5.1	ns
<sup>t</sup> dis	OEAB or OEBA	A or B	1	6.5		5.4	1	4.9	ns

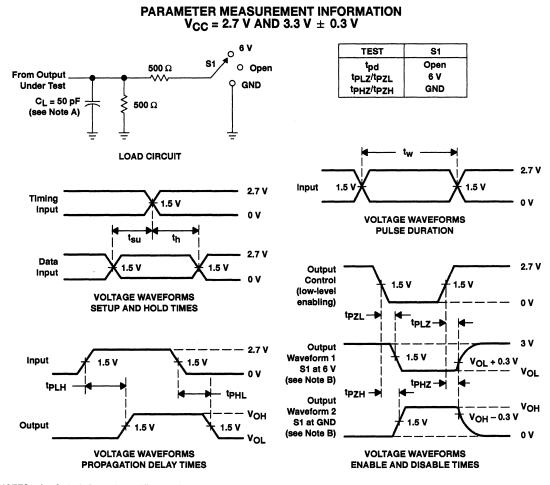
#### operating characteristics, T<sub>A</sub> = 25°C

	PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V TYP	V <sub>CC</sub> = 3.3 V ± 0.3 V TYP	UNIT
C .	Power dissipation capacitance	Outputs enabled	C <sub>1</sub> = 50 pF, f = 10 MHz	160	160	- 5
Cpd		Outputs disabled	C <sub>L</sub> = 50 pF, f = 10 MHz	160	160	pF



## SN74ALVCH16525 **18-BIT REGISTERED BUS TRANSCEIVER** WITH 3-STATE OUTPUTS

SCES059A - NOVEMBER 1995 - REVISED NOVEMBER 1996



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , tr  $\leq$  2.5 ns, tr  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpi H and tpHi are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



### SN74ALVCH162525 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES058A - NOVEMBER 1995 - REVISED NOVEMBER 1996

<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	DGG OR DL PACKAGE (TOP VIEW)
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	
<ul> <li>B-Port Outputs Have Equivalen 26-Ω Series Resistors, So No External Resistors Are Required</li> </ul>	A1 3 54 B1 GND 4 53 GND
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015;Exceeds 200V Using Machine Model (C = 200 pF, R = 0)</li> </ul>	A2 [] 5 52 [] B2 A3 [] 6 51 [] B3 V <sub>CC</sub> [] 7 50 [] V <sub>CC</sub> A4 [] 8 49 [] B4
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	A5 0 9 48 B5 A6 0 10 47 B6
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	GND [] 11 46 ]] GND A7 [] 12 45 ]] B7 A8 [] 13 44 ]] B8
<ul> <li>Package Option Includes Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages</li> </ul>	A9 [] 14 43 ] B9 A10 [] 15 42 ] B10 A11 [] 16 41 ] B11 A12 [] 17 40 [] B12
description	GND 18 39 GND A13 19 38 B13
This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V $V_{CC}$ operation.	A13 [ 19 38 ] B13 A14 [ 20 37 ] B14 A15 [ 21 36 ] B15
Data flow in each direction is controlled by output-enable (OEAB and OEBA) and clock- enable (CLKENAB and CLKENBA) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of SEL.	V <sub>CC</sub> [ 22 35] V <sub>CC</sub> A16 [ 23 34 ] B16 A17 [ 24 33 ] B17 GND [ 25 32 ] GND A18 [ 26 31 ] B18 OEBA [ 27 30 ] CLK1BA CLKENBA [ 28 29 ] CLK2BA

Data is stored in the internal registers on the low-to-high transition of the CLK input, provided that the appropriate CLKEN inputs are low. The A-to-B data transfer is synchronized to the CLKAB input, and B-to-A data transfer is synchronized with the CLK1BA and CLK2BA inputs.

The B outputs, which are designed to sink up to 12 mA, include 26- $\Omega$  resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162525 is characterized for operation from -40°C to 85°C.

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#### **Function Tables**

	A-TO-B	STORAGE (	$\overline{OEAB} = L$
--	--------	-----------	-----------------------

l	OUTPUT		
CLKENAB	CLKAB	A	В
н	х	х	B0 <sup>†</sup>
L	Ŷ	L	L
L	Ŷ	н	н

<sup>†</sup>Output level before the indicated steady-state

input conditions were established B-TO-A STORAGE (OEBA = L)

	INPUTS								
CLKENBA	CLK2BA	CLK1BA	SEL	В	A				
н	X	х	х	х	A0 <sup>†</sup>				
L	Ŷ	х	н	L	L				
L	Ŷ	х	н	н	н				
L	Ŷ	<b>↑</b>	L	L	L‡				
L	Ŷ	Ŷ	L	н	н‡				

<sup>†</sup>Output level before the indicated steady-state input conditions were established

<sup>‡</sup> Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when SEL is low.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V <sub>CC</sub>	–0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3	3): DGG package 1 W
	DL package 1.4 W
Storage temperature range, T <sub>stg</sub>	

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book.



## SN74ALVCH162525 **18-BIT REGISTERED BUS TRANSCEIVER** WITH 3-STATE OUTPUTS SCES058A - NOVEMBER 1996 - REVISED NOVEMBER 1996

PARAMETER	TEST C	ONDITIONS	Vcc	MIN TYPT	MAX	UNIT
	l <sub>OH</sub> =100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -0.2		
	I <sub>OH</sub> =6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2		
14 (A 1)		V <sub>IH</sub> = 1.7 V	2.3 V	1.7		
VOH (A port)	I <sub>OH</sub> = -12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2		V
		V <sub>IH</sub> = 2 V	3 V/	2.4		
	lон = -24 mA,	V <sub>IH</sub> = 2 V	3 V	2		
	IOH = -100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -0.2		
	I <sub>OH</sub> = -4 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	1.9		
		V <sub>IH</sub> = 1.7 V	2.3 V	1.7		
VOH (B port)	I <sub>OH</sub> = -6 mA	V <sub>IH</sub> = 2 V	3 V	2.4		v
	I <sub>OH</sub> =8 mA,	V <sub>IH</sub> = 2 V	2.7 V	2		
	$I_{OH} = -12 \text{ mA},$	V <sub>IH</sub> = 2 V	3 V	2		
	l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V		0.2	
	l <sub>OL</sub> = 6 mA,	V <sub>IL</sub> = 0.7 V	2.3 V		0.4	
V <sub>OL</sub> (A port)		V <sub>IL</sub> = 0.7 V	2.3 V		0.7	v
	I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.8 V	2.7 V		0.4	
	I <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V		0.55	
	l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V		0.2	;
	$I_{OL} = 4 \text{ mA},$	V <sub>IL</sub> = 0.7 V	2.3 V		0.4	
V <sub>OL</sub> (B port)	0	V <sub>IL</sub> = 0.7 V	2.3 V		0.55	
	I <sub>OL</sub> = 6 mA	V <sub>IL</sub> = 0.8 V	3 V		0.55	v
	l <sub>OL</sub> = 8 mA,	V <sub>IL</sub> = 0.8 V	2.7 V		0.6	
	I <sub>OL</sub> = 12 mA,	V <sub>IL</sub> = 0.8 V	3 V		0.8	
1	V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V		±5	μA
	V <sub>I</sub> = 0.7 V		0.014	45		
	V <sub>I</sub> = 1.7 V		− 2.3 V	-45		
<sup>I</sup> hold	V <sub>I</sub> = 0.8 V		0.14	75		μA
	V <sub>1</sub> = 2 V .	- 3V	-75			
	V <sub>I</sub> = 0 to 3.6 V <sup>‡</sup>	3.6 V				
loz§	V <sub>O</sub> = V <sub>CC</sub> or GND		3.6 V		±10	μA
ICC	$V_{I} = V_{CC}$ or GND,	lO = 0	3.6 V		40	μA
AICC	One input at V <sub>CC</sub> – 0.6 V,	Other inputs at VCC or GND	3 V to 3.6 V		750	μA
Ci Control inputs			3.3 V	3		pF
Co A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V	7		pF

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

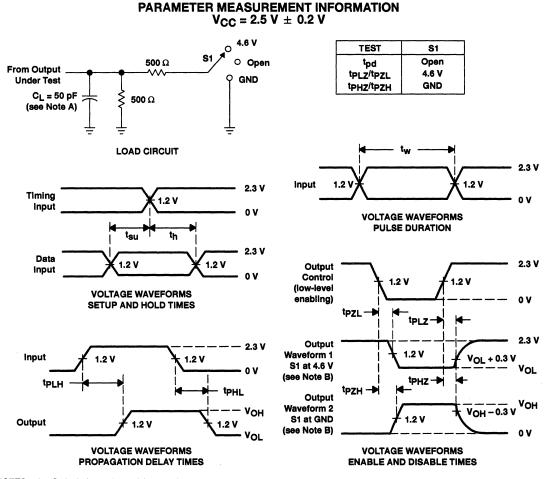
<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

<sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another. § For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.



## SN74ALVCH162525 **18-BIT REGISTERED BUS TRANSCEIV** WITH 3-STATE OUTPUTS

SCES058A - NOVEMBER 1995 - REVISED NOVEMBER 1996



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , tr  $\leq$  2.5 ns, tr  $\leq$  2.5 ns,
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

#### Figure 1. Load Circuit and Voltage Waveforms



SN74ALVCH16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS s

CES046A -	- J	υ	LY	1	99	95	- F	ΙE	٧	IS	E	DI	10	/EI	M	BEF	R	19	96

● Member of the Texas Instruments	DGG OR DL PACKAGE
Widebus™ Family	(TOP VIEW)
<ul> <li>EPIC ™ (Enhanced-Performance Implanted</li></ul>	OEA 1 56 OE2B
CMOS) Submicron Process	LE1B 2 55 LEA2B
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)</li> </ul>	2B3 3 54 2B4 GND 4 53 GND 2B2 5 52 2B5
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	2B1 0 6 51 2B6 V <sub>CC</sub> 7 50 V <sub>CC</sub> A1 8 49 2B7
<ul> <li>Bus Hold on Data Inputs Eliminates</li></ul>	A2 9 48 288
the Need for External Pullup/Pulldown	A3 10 47 289
Resistors	GND 11 46 GND
<ul> <li>Package Options Include Plastic Shrink</li></ul>	A4 [] 12 45 ] 2B10
Small-Outline (DL) and Thin Shrink	A5 [] 13 44 ] 2B11
Small-Outline (DGG) Packages	A6 [] 14 43 ] 2B12
description	A7 0 15 42 1812 A8 0 16 41 1811
This 12-bit to 24-bit multiplexed D-type latch is designed for 2.3-V to 3.6-V <sub>CC</sub> operation.	A9   17 40   1B10 GND   18 39   GND A10   19 38   1B9
The SN74ALVCH16260 is used in applications where two separate datapaths must be multiplexed ante or domultiplexed from a	A11 [ 20 37 ] 1B8 A12 [ 21 36 ] 1B7
multiplexed onto, or demultiplexed from, a	V <sub>CC</sub> 22 35 V <sub>CC</sub>
single datapath. Typical applications include	1B1 23 34 1B6
multiplexing and/or demultiplexing address and	1B2 24 33 1B5
data information in microprocessor or	GND 25 32 GND
bus-interface applications. This device is also	1B3 26 31 1B4
useful in memory-interleaving applications.	LE2B 27 30 LEA1B
Three 12-bit I/O ports (A1-A12, 1B1-1B12, and	SEL 28 29 OE1B

Three 12-bit I/O ports (A1-A12, 1B1-1B12, and 2B1-2B12) are available for address and/or data

transfer. The output-enable (OE1B, OE2B, and OEA) inputs control the bus transceiver functions. The OE1B and OE2B control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16260 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

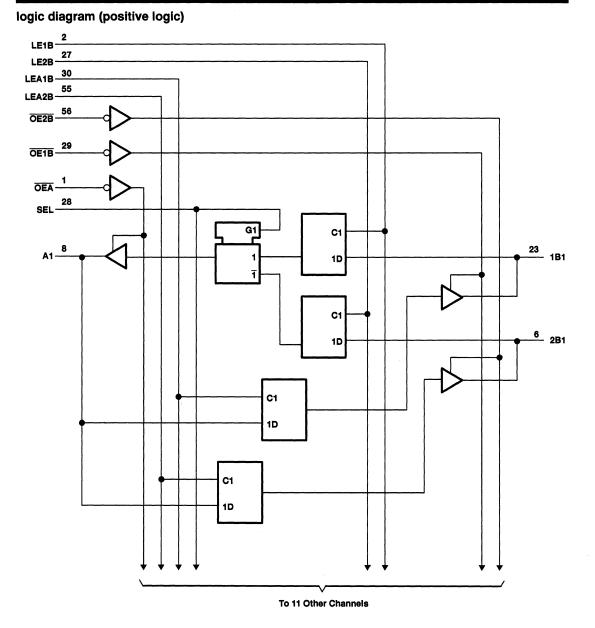
The SN74ALVCH16260 is characterized for operation from -40°C to 85°C.

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## SN74ALVCH16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS SCES046A - JULY 1995 - REVISED NOVEMBER 1996





#### SN74ALVCH16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES046A - JULY 1995 - REVISED NOVEMBER 1996

PARAM	ETER	TEST C	ONDITIONS	Vcc	MIN	түрт	MAX	UNIT	
		I <sub>OH</sub> = -100 μA		2.3 V to 3.6 V	Vcc-	0.2			
		I <sub>OH</sub> = -6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2				
			V <sub>IH</sub> = 1.7 V	2.3 V	1.7			v	
VOH		I <sub>OH</sub> = -12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2			v	
			V <sub>IH</sub> = 2 V	3 V	2.4				
		l <sub>OH</sub> = -24 mA,	V <sub>IH</sub> = 2 V	3 V	2				
		l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V			0.2		
		I <sub>OL</sub> = 6 mA,	V <sub>IL</sub> = 0.7 V	2.3 V			0.4		
VOL		l <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 V	2.3 V		0.7		v	
			V <sub>IL</sub> = 0.8 V	2.7 V			0.4		
		l <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V			0.55		
կ		VI = V <sub>CC</sub> or GND		3.6 V			±5	μA	
		V <sub>1</sub> = 0.7 V		2.3 V	45				
		Vi = 1.7 V		2.5 V	-45				
li(hold)		VI = 0.8 V		- 3V	75			μA	
		V <sub>I</sub> = 2 V		31	-75				
		V <sub>1</sub> = 0 to 3.6 V‡		3.6 V			±500		
loz§		V <sub>O</sub> = V <sub>CC</sub> or GND		3.6 V			±10	μA	
ICC		$V_{I} = V_{CC} \text{ or GND},$	IO = 0	3.6 V			40	μA	
∆lCC		One input at V <sub>CC</sub> – 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA	
C <sub>i</sub> Cor	ntrol inputs	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V		3.5		pF	
C <sub>io</sub> Ao	r B ports	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V		9		pF	

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

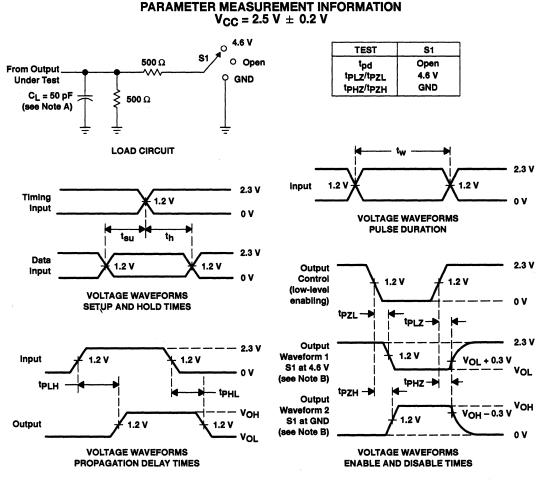
For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V <sub>CC</sub> = ± 0.2		V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = ± 0.3		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
tw	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B	1.4		1.1		1.1		ns
th	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B	1.6		1.9		1.5		ns



#### SN74ALVCH16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS SCES046A - JULY 1995 - REVISED NOVEMBER 1990



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns,
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

#### Figure 1. Load Circuit and Voltage Waveforms



SN74ALVCH162260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS SCAS570B – MARCH 1996 – REVISED NOVEMBER 1996

<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	DGG OR DL (TOP V	
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>		56 0E2B
<ul> <li>B-Port Outputs Have Equivalent 26-Ω</li> </ul>	2B3 3	54 2B4
Series Resistors, So No External Resistors	GND 4	53 GND
Are Required	2B2 🚺 5	52 2B5
ESD Protection Exceeds 2000 V Per	2B1 🚺 6	51 <b>]</b> 2B6
MIL-STD-883, Method 3015; Exceeds	V <sub>CC</sub> [] 7	50 🛛 V <sub>CC</sub>
200 V Using Machine Model (C = 200 pF, R = 0)	A1 🛛 8	49 2B7
	A2 [] 9	48 2B8
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>		47 2B9
	GND 11 A4 112	46 GND 45 2B10
<ul> <li>Bus Hold on Data Inputs Eliminates</li> <li>the Need for External Bullum/Bulldown</li> </ul>	A4 U 12 A5 1 13	45112B10 44112B11
the Need for External Pullup/Pulldown Resistors	A6    14	43 2B12
	A7 115	42 1B12
<ul> <li>Package Options Include Thin-Shrink Small-Outline (DGG) and Plastic Shrink</li> </ul>	A8 1 16	41 1 1B11
Small-Outline (DCG) and Plastic Shrink Small-Outline (DL) Packages	A9 🛛 17	40 <b>0</b> 1B10
Onian-Outline (DE) I dokageo	GND 🚺 18	39 🛛 GND
description	A10 🚺 19	38 🛛 1B9
This 40 bit to 04 bit souldisland D toss latch is	A11 🛛 20	37 🛛 1B8
This 12-bit to 24-bit multiplexed D-type latch is	A12 21	36 <b>0</b> 1B7
designed for 2.3-V to 3.6-V <sub>CC</sub> operation.	V <sub>CC</sub> 22	35 V <sub>CC</sub>
The SN74ALVCH162260 is used in applications	1B1 23	34 1B6
where two separate datapaths must be	1B2 24	33 1B5
multiplexed onto, or demultiplexed from, a	GND 25 1B3 126	32 GND
single datapath. Typical applications include	1B3 [] 26 LE2B [] 27	31 ] 1B4 30 ] LEA1B
multiplexing and/or demultiplexing address and data information in microprocessor or	SEL 28	29 0E1B
data information in microprocessor or		

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable (OE1B, OE2B, and OEA) inputs control the bus transceiver functions. The OE1B and OE2B control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

The B outputs, which are designed to sink up to 12 mA, include 26- $\Omega$  resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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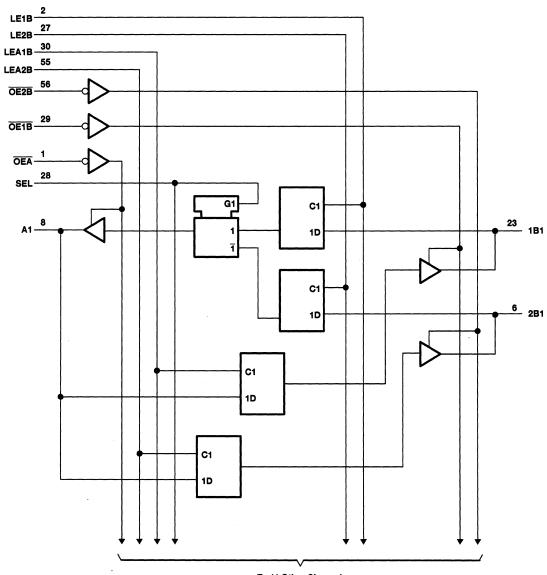
bus-interface applications. This device is also useful in memory-interleaving applications.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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## SN74ALVCH162260 **12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH** WITH 3-STATE OUTPUTS SCAS570B - MARCH 1996 - REVISED NOVEMBER 1996



logic diagram (positive logic)

To 11 Other Channels



### SN74ALVCH162260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS570B - MARCH 1996 - REVISED NOVEMBER 1996

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

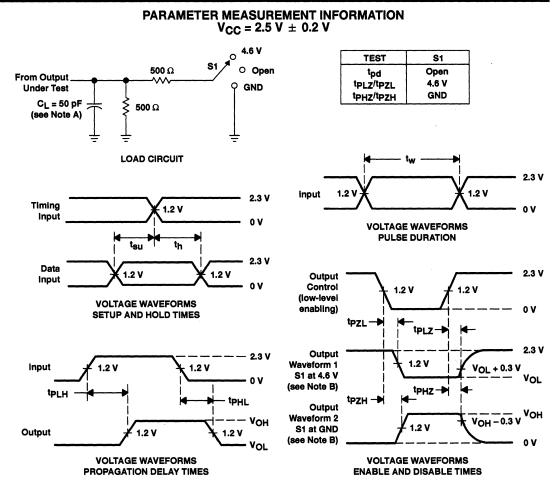
PARAN	AETER	TEST C	ONDITIONS	Vcc	MIN TY	PT MAX	UNIT
		l <sub>OH</sub> = -100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -0.2		
		<sup>1</sup> OH = −6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2		
			V <sub>IH</sub> = 1.7 V	2.3 V	1.7		v
VOH (A port)	)	1 <sub>OH</sub> = -12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2		v
			V <sub>IH</sub> = 2 V	3 V	2.4		
		I <sub>OH</sub> = -24 mA,	V <sub>IH</sub> = 2 V	3 V	2		
		I <sub>OH</sub> = – 100 µA		2.3 V to 3.6 V	Vcc-0	).2	
		$I_{OH} = -4 \text{ mA},$	V <sub>IH</sub> = 1.7 V	2.3 V	1.9		
			V <sub>IH</sub> = 1.7 V	2.3 V	1.7		.,
VOH (B port)	)	I <sub>OH</sub> = -6 mA	V <sub>IH</sub> = 2 V	3 V	2.4		v
		I <sub>OH</sub> = -8 mA,	V <sub>IH</sub> = 2 V	2.7 V	2		
		I <sub>OH</sub> = -12 mA,	V <sub>IH</sub> = 2 V	3 V	2		
		I <sub>OL</sub> = 100 μA		2.3 V to 3.6 V		0.2	
		I <sub>OL</sub> = 6 mA,	V <sub>IL</sub> = 0.7 V	2.3 V		0.4	
V <sub>OL</sub> (A port)		V <sub>IL</sub> = 0.7 V	2.3 V		0.7	0.7 V	
	I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.8 V	2.7 V		0.4		
		i <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V		0.55	
		l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V		0.2	
		I <sub>OL</sub> = 4 mA,	V <sub>IL</sub> = 0.7 V	2.3 V		0.4	
			V <sub>IL</sub> = 0.7 V	2.3 V		0.55	
VOL (B port)		I <sub>OL</sub> = 6 mA	V <sub>IL</sub> = 0.8 V	3 V		0.55	v
		i <sub>OL</sub> = 8 mA,	V <sub>IL</sub> = 0.8 V	2.7 V		0.6	
		I <sub>OL</sub> = 12 mA,	V <sub>IL</sub> = 0.8 V	3 V		0.8	
l		VI = VCC or GND		3.6 V		±5	μA
		VI = 0.7 V		0.014	45		
		VI = 1.7 V	2.3 V	-45			
<sup>I</sup> I(hold)		VI = 0.8 V		75		μA	
		V <sub>1</sub> = 2 V	- 3V	-75			
		V <sub>1</sub> = 0 to 3.6 V <sup>‡</sup>	3.6 V		±500		
loz§		V <sub>O</sub> = V <sub>CC</sub> or GND		3.6 V		±10	μA
lcc		$V_{I} = V_{CC}$ or GND,	lO = 0	3.6 V		40	μA
		One input at V <sub>CC</sub> - 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V		750	μA
	ontrol inputs	VI = VCC or GND		3.3 V		3.5	pF
······	or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V		4.5	pF

<sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C. <sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

 $For I/O ports, the parameter I_{OZ} includes the input leakage current.$ 



#### SN74ALVCH162260 **12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH** WITH 3-STATE OUTPUTS SCAS570B - MARCH 1996 - REVISED NOVEMBER 1996



- NOTES: A. CL includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN74ALVCH162268 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES018B - AUGUST 1995 - REVISED JANUARY 1997

● Member of the Texas Instruments	DGG OR DL PACKAGE
<i>Widebus</i> ™ Family	(TOP VIEW)
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	
<ul> <li>B-Port Outputs Have Equivalent 26-Ω</li></ul>	2B3 3 54 2B4
Serles Resistors, So No External Resistors	GND 4 53 GND
Are Required	2B2 5 52 2B5
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)</li> </ul>	2B2 3 52 2B3 2B1 6 51 2B6 V <sub>CC</sub> 7 50 V <sub>CC</sub> A1 8 49 2B7 A2 9 48 2B8
<ul> <li>Latch-Up Performance Exceeds 250 mA</li></ul>	A3 1 10 47 2B9
Per JEDEC Standard JESD-17	GND 11 46 GND
<ul> <li>Bus Hold on Data Inputs Eliminates</li></ul>	A4 0 12 45 2B10
the Need for External Pullup/Pulldown	A5 0 13 44 2B11
Resistors	A6 0 14 43 2B12
<ul> <li>Package Options Include Plastic Shrink</li></ul>	A7 [ 15 42 ] 1B12
Small-Outline (DL) and Thin Shrink	A8 [ 16 41 ] 1B11
Small-Outline (DGG) Packages	A9 [ 17 40 ] 1B10
description	GND 118 39 GND A10 19 38 1B9
This 12-bit to 24-bit registered bus exchanger is designed for 2.3-V to 3.6-V $V_{CC}$ operation.	A11 20 37 188 A12 21 36 1B7 V <sub>CC</sub> 22 35 V <sub>CC</sub>
The SN74ALVCH162268 is used for applications where data must be transferred from a narrow high-speed bus to a wide, lower-frequency bus.	1B1 [ 23 34 ] 1B6 1B2 [ 24 33 ] 1B5 GND [ 25 32 ] GND
The device provides synchronous data exchange	1B3 26 31 184
between the two ports. Data is stored in the	CLKEN2B 27 30 CLKENA1
internal registers on the low-to-high transition of	SEL 28 29 CLK

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path with a single storage register in the A-to-2B path. Proper control of these inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables (OEA, OEB). These control terminals are registered so bus direction changes are synchronous with CLK.

The B outputs, which are designed to sink up to 12 mA, include 26- $\Omega$  resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162268 is characterized for operation from -40°C to 85°C.

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the clock (CLK) input when the appropriate clock-enable (CLKEN) inputs are low. The select (SEL) line is synchronous with CLK and selects

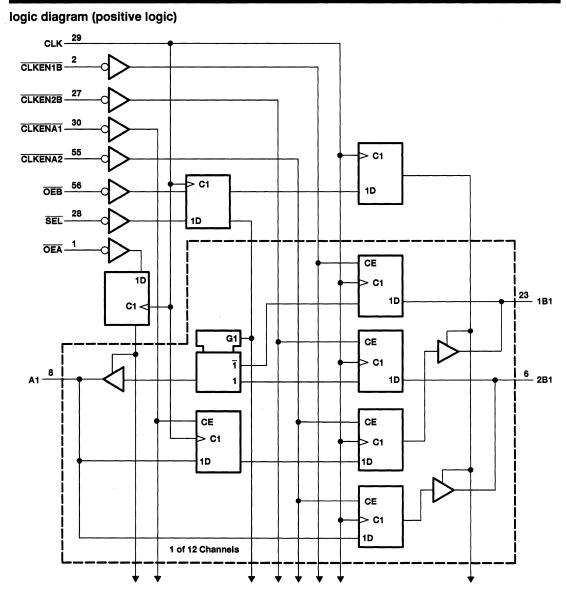
1B or 2B input data for the A outputs.

PRODUCTION DATA information is current as of publication date. Products conform to specifications par the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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## SN74ALVCH162268 **12-BIT TO 24-BIT REGISTERED BUS EXCHANGER** WITH 3-STATE OUTPUTS SCES018B - AUGUST 1995 - REVISED JANUARY 1997





## SN74ALVCH162268 **12-BIT TO 24-BIT REGISTERED BUS EXCHANGER** WITH 3-STATE OUTPUTS

SCES018B - AUGUST 1995 - REVISED JANUARY 1997

PARAMETER	TEST CO	ONDITIONS	Vcc	MIN	түрт мах	UNIT	
VOH (B port)	I <sub>OH =</sub> −100 µA		2.3 V to 3.6 V	V <sub>CC</sub> -0	.2	1	
	I <sub>OH</sub> = -4 mA,			1.9			
		V <sub>IH</sub> = 1.7 V	2.3 V	1.7		v	
	I <sub>OH</sub> = -6 mA	V <sub>IH</sub> = 2 V	3 V	2.4			
	I <sub>OH</sub> = -8 mA,	V <sub>IH</sub> = 2 V	2.7 V	2			
	I <sub>OH</sub> = -12 mA,	V <sub>IH</sub> = 2 V	3 V	2			
	l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V		0.2		
V <sub>OL</sub> (B port)	$I_{OL} = 4 \text{ mA},$				0.4	1	
		V <sub>IL</sub> = 0.7 V	2.3 V		0.55	v	
	I <sub>OL</sub> = 6 mA	V <sub>IL</sub> = 0.8 V	3 V		0.55		
	I <sub>OL</sub> = 8 mA,	V <sub>IL</sub> = 0.8 V	2.7 V		0.6		
	I <sub>OL</sub> = 12 mA,	V <sub>IL</sub> = 0.8 V	3 V		0.8		
V <sub>OH</sub> (A port)	I <sub>OH</sub> = -100 μA		2.3 V to 3.6 V		V <sub>CC</sub> -0.2	-0.2	
	l <sub>OH</sub> = −6 mA,	VIH = 1.7 V	2.3 V	2			
	I <sub>OH</sub> = -12 mA	V <sub>IH</sub> = 1.7 V	2.3 V	1.7	الالتصحير ويرالية الأخط ويتحجبوا الخط	1	
		V <sub>IH</sub> = 2 V	2.7 V	2.2		1 ~	
		V <sub>IH</sub> = 2 V	3 V	2.4			
	I <sub>OH</sub> = -24 mA,	V <sub>IH</sub> = 2 V	3 V	2			
V <sub>OL</sub> (A port)	l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V		0.2		
	$I_{OL} = 6 \text{ mA},$	VIL = 0.7 V	2.3 V		0.4	1	
	I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 V	2.3 V		0.7	v	
		V <sub>IL</sub> = 0.8 V	2.7 V		0.4		
	I <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V		0.55		
.	$V_{I} = V_{CC} \text{ or GND}$		3.6 V		±5	μA	
lı(hold)	V <sub>1</sub> = 0.7 V V <sub>1</sub> = 1.7 V		2.3 V	45	, ,	μA	
				-45			
	V <sub>1</sub> = 0.8 V V <sub>1</sub> = 2 V		- 3 V	75			
				-75			
	$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V				
loz§	$V_{O} = V_{CC}$ or GND		3.6 V		±10	μA	
	$V_{I} = V_{CC}$ or GND,	I <sub>O</sub> = 0	3.6 V		40	μΑ	
∆lcc	One input at V <sub>CC</sub> – 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V		750	μA	
Ci Control inputs			3.3 V		3.5	pF	
Cio A or B ports	$V_{O} = V_{CC} \text{ or } GND$		3.3 V		9	pF	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

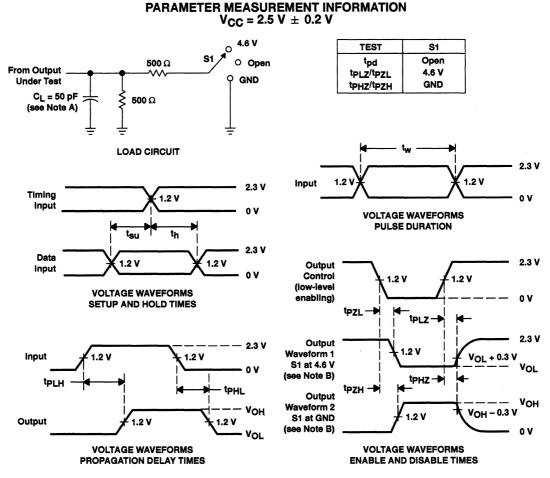
<sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C. <sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

§ For I/O ports, the parameter IOZ includes the input-leakage current.

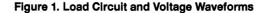


## SN74ALVCH162268 **12-BIT TO 24-BIT REGISTERED BUS EXCHANGER** WITH 3-STATE OUTPUTS

SCES018B - AUGUST 1995 - REVISED JANUARY 1997



- NOTES: A. CL includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzi and tpzH are the same as ten.
  - G. tPLH and tPHL are the same as tod.





SN74ALVCH16269 12-BIT TO 24-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES019B - JULY 1995 - REVISED JANUARY 1997

	00200		LY 1995 - REVISED		
<ul> <li>Member of the Texas Instruments</li> <li>Widebus™ Family</li> </ul>	DGG OR DL PACKAGE (TOP VIEW)				
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	OEA OEB1		56 OEB2		
ESD Protection Exceeds 2000 V Per	2B3		55 CLKENA2 54 284		
MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)	GND	4	53 GND		
<ul> <li>Latch-Up Performance Exceeds 250 mA</li> </ul>	2B2		52 2B5		
Per JEDEC Standard JESD-17	2B1 [ V <sub>CC</sub> [		51 2B6 50 V <sub>CC</sub>		
<ul> <li>Bus Hold on Data Inputs Eliminates</li> </ul>	A1		49 2B7		
the Need for External Pullup/Pulldown	A2 [		48 <b>0</b> 2B8		
Resistors	A3 [ GND [		47 2B9 46 GND		
<ul> <li>Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink</li> </ul>	A4 [		45 2B10		
Small-Outline (DGG) Packages	A5 🛛	13	44 2B11		
	A6 [		43 2B12		
description	A7 [ A8 [		42 1B12 41 1B11		
This 12-bit to 24-bit registered bus transceiver is	A9		40 <b>0</b> 1B10		
designed for 2.3-V to 3.6-V V <sub>CC</sub> operation.	GND [				
The SN74ALVCH16269 is used in applications	A10 A11		38 1B9 37 1B8		
where two separate ports must be multiplexed onto, or demultiplexed from, a single port. The	A12		36 1 1B7		
device is particularly suitable as an interface	v <sub>cc</sub> [	22	35 V <sub>CC</sub>		
between synchronous DRAMs and high-speed	1B1		34 1B6		
microprocessors.	1B2 GND		33 31 1B5 32 31 GND		
Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input	1B3 [		31 1B4		

the low-to-high transition of the clock (CLK) input when the appropriate clock-enable (CLKENA) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data

NC - No internal connection

30 CLKENA1

29 CLK

NC 127

SEL 28

transfer in the B-to-A direction, a single storage register is provided. The select (SEL) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period that the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables (OEA, OEB1, OEB2).

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16269 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16269 is characterized for operation from -40°C to 85°C.

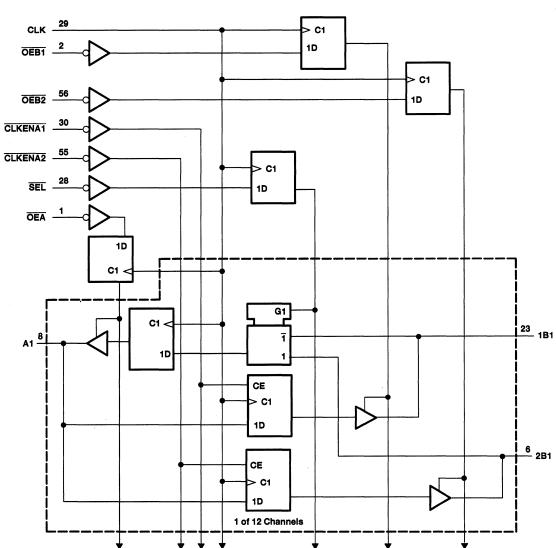
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## SN74ALVCH16269 **12-BIT TO 24-BIT REGISTERED BUS TRANSCEIVER** WITH 3-STATE OUTPUTS SCES019B – JULY 1995 – REVISED JANUARY 1997



logic diagram (positive logic)



# SN74ALVCH16269 12-BIT TO 24-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES019B – JULY 1995 – REVISED JANUARY 1997

PARAMETER	TEST CO	ONDITIONS	Vcc	MIN T	YPT MAX	UNIT	
	l <sub>OH</sub> = -100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -0.2			
	I <sub>OH</sub> = −6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2			
Veu		V <sub>IH</sub>	2.3 V	1.7			
Vон	I <sub>OH</sub> = -12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2		] `	
		V <sub>IH</sub> = 2 V	3 V	2.4			
	I <sub>OH</sub> = -24 mA,	V <sub>IH</sub> = 2 V	3 V	2			
	l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V		0.2		
	l <sub>OL</sub> ≖ 6 mA,	V <sub>IL</sub> = 0.7 V	2.3 V		0.4		
VOL	I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 V	2.3 V		0.7	V (	
		V <sub>IL</sub> = 0.8 V	2.7 V		0.4		
	I <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V		0.55		
l	V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V		±5	μA	
	VI = 0.7 V		2.3 V	45			
	V <sub>I</sub> = 1.7 V		2.5 V	-45			
l(hold)	V <sub>1</sub> = 0.8 V		3 V	75		μA	
	V <sub>I</sub> = 2 V		57	-75			
	V <sub>1</sub> = 0 to 3.6 V <sup>‡</sup>		3.6 V		±500		
loz§	V <sub>O</sub> = V <sub>CC</sub> or GND		3.6 V		±10	μA	
lcc	$V_{I} = V_{CC}$ or GND,	lO = 0	3.6 V		40	μA	
∆ICC	One input at V <sub>CC</sub> – 0.6 V,	Other inputs at $V_{CC}$ or GND	3 V to 3.6 V		750	μA	
Ci Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V		3.5	pF	
Cio A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V		9	pF	

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C. <sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

§ For I/O ports, the parameter IOZ includes the input-leakage current.



### SN74ALVCH16269 12-BIT TO 24-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES0198 - JULY 1995 - REVISED JANUARY 1997

PARAMETER MEASUREMENT INFORMATION  $V_{CC} = 2.5 V \pm 0.2 V$ 4.6 V TEST **S1** 0 **S1** Open O Open tpd **500** Ω From Output tPLZ/tPZL 4.6 V GND Under Test GND tPHZ/tPZH CL = 50 pF **500** Ω (see Note A) LOAD CIRCUIT 2.3 V 1.2 V 1.2 \ Input 2.3 V Timing 1.2 V ΛV Input 0 V **VOLTAGE WAVEFORMS** PULSE DURATION tsu th 2.3 V Data 2.3 V 1.2 V 1.2 V Output Input 0 V Control .2 V .2 V (low-level **VOLTAGE WAVEFORMS** enabling) 0 V SETUP AND HOLD TIMES tPZLtoi 7 2.3 V Output 2.3 V v Waveform 1 Input 1.2 V 1.2 V VOL + 0.3 V S1 at 4.6 V VOL 0 V (see Note B) tPHZ**t**PLH tPZH -<sup>t</sup>PHL Output VOH Waveform 2 VOH - 0.3 V VOH .2 V S1 at GND Output 1.2 V 1.2 V (see Note B) 0 V VOL **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES** ENABLE AND DISABLE TIMES

- NOTES: A. CL includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tp71 and tp7H are the same as  $t_{en}$ .
  - G. tpLH and tpHL are the same as tod.

### Figure 1. Load Circuit and Voltage Waveforms



SN74ALVCHR162269 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES050B - AUGUST 1995 - REVISED JANUARY 1997

<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	DGG OR DL PACKAGE (TOP VIEW)
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	OEA 1 56 OEB2 OEB1 2 55 CLKENA2
<ul> <li>ESD Protection Exceeds 2000 V Per</li> </ul>	2B3 3 54 2B4
MIL-STD-883, Method 3015; Exceeds 200 V	
Using Machine Model (C = 200 pF, R = 0)	2B2 5 52 2B5
<ul> <li>Latch-Up Performance Exceeds 250 mA</li> </ul>	2B1 6 51 2B6
Per JEDEC Standard JESD-17	V <sub>CC</sub> [] 7 50 ] V <sub>CC</sub>
<ul> <li>All Outputs Have Equivalent 26-Ω Series</li> </ul>	A1 🛛 8 49 🖸 2B7
Resistors, So No External Resistors Are	A2 🛛 9 48 🖸 2B8
Required	A3 10 47 2B9
<ul> <li>Bus Hold on Data Inputs Eliminates</li> </ul>	GND 11 46 GND
the Need for External Pullup/Pulldown	A4 12 45 2B10
Resistors	A5 113 44 2811
<ul> <li>Package Options Include Plastic Shrink</li> </ul>	A6 14 43 2B12
Small-Outline (DL) and Thin Shrink	A7 15 42 1B12 A8 16 41 1B11
Small-Outline (DGG) Packages	
decerintian	A9 17 40 1B10 GND 18 39 GND
description	A10 19 38 1B9
This 12-bit to 24-bit registered bus exchanger is	A11 20 37 1B8
designed for 2.3-V to 3.6-V V <sub>CC</sub> operation.	A12 21 36 1B7
	V <sub>CC</sub> 22 35 V <sub>CC</sub>
The SN74ALVCHR162269 is used in applications where two separate ports must be multiplexed	1B1 23 34 1B6
onto, or demultiplexed from, a single port. It is	1B2 24 33 1B5
particularly suitable as an interface between	GND 25 32 GND
synchronous DRAMs and high-speed micro-	1B3 26 31 1B4
processors.	NC 27 30 CLKENA1
Data is stored in the internal R-port registers on	SEL 28 29 CLK

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock enable ( $\overline{CLKENA}$ )

NC-N	٩v	internal	connection

inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select (SEL) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period that the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables (OEA, OEB1, and OEB2).

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

All outputs are designed to sink up to 12 mA and include  $26-\Omega$  resistors to reduce overshoot and undershoot.

The SN74ALVCHR162269 is characterized for operation from -40°C to 85°C.

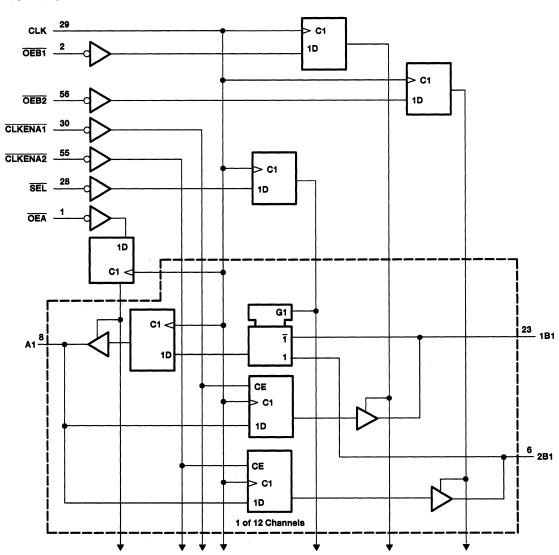
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# SN74ALVCHR162269 **12-BIT TO 24-BIT REGISTERED BUS EXCHANGER** WITH 3-STATE OUTPUTS SCES050B - AUGUST 1995 - REVISED JANUARY 1997



logic diagram (positive logic)



# SN74ALVCHR162269 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES050B - AUGUST 1995 - REVISED JANUARY 1997

PARAMETER	TEST C	CONDITIONS	Vcc	MIN	түрт	MAX	UNIT	
	I <sub>OH</sub> = −100 µA		2.3 V to 3.6 V	V <sub>CC</sub> -0.	2			
	1	V <sub>IH</sub> = 1.7 V	2.3 V	1.9	· .			
	I <sub>OH</sub> = -4 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2				
VOH	1au 6 mA	V <sub>IH</sub> = 1.7 V	2.3 V	1.7			v	
	I <sub>OH</sub> = -6 mA	V <sub>IH</sub> = 2 V	3 V	2.4				
	IOH = −8 mA,	V <sub>IH</sub> = 2 V	2.7 V	2				
	IOH = -12 mA,	V <sub>IH</sub> = 2 V	3 V	2				
,	l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V			0.2		
	lle: 4 m 4	VIL = 0.7 V	2.3 V			0.4		
	I <sub>OL</sub> = 4 mA	V <sub>IL</sub> = 0.8 V	2.7 V			0.4		
V <sub>OL</sub>	la. 6ml	VIL = 0.7 V	2.3 V			0.55 V	v	
	I <sub>OL</sub> = 6 mA	VIL = 0.8 V	3 V			0.55	0.55	
	loL = 8 mA,	V <sub>IL</sub> = 0.8 V	2.7 V			0.6		
	l <sub>OL</sub> = 12 mA,	V <sub>IL</sub> = 0.8 V	3 V			0.8		
1	VI = V <sub>CC</sub> or GND		3.6 V			±5	μA	
	VI = 0.7 V		2.3 V	45				
	V <sub>I</sub> = 1.7 V		2.3 y	-45				
li(hold)	V <sub>I</sub> = 0.8 V		3 V	75			μA	
	Vi = 2 V		7 30	-75				
	VI = 0 to 3.6 V		3.6 V			±500		
loz§	V <sub>O</sub> = V <sub>CC</sub> or GND <sup>‡</sup>		3.6 V			±10	μA	
lcc	V <sub>I</sub> = V <sub>CC</sub> or GND,	IO = 0	3.6 V			40	μA	
∆ICC	One input at V <sub>CC</sub> – 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA	
Ci Control inputs			3.3 V		3.5		pF	
Cio A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V		9		pF	

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

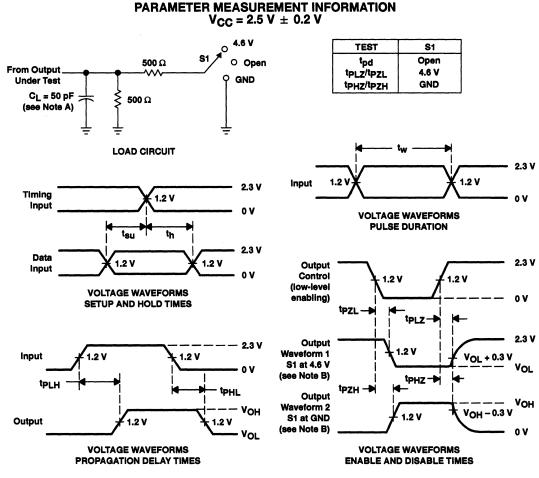
<sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.



# SN74ALVCHR162269 **12-BIT TO 24-BIT REGISTERED BUS EXCHANGER** WITH 3-STATE OUTPUTS

SCES050B - AUGUST 1995 - REVISED JANUARY 1997



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- tpLZ and tpHZ are the same as tdis. E.
- F. tpzi and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

#### Figure 1. Load Circuit and Voltage Waveforms



SN74ALVCH16270 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES028B - JULY 1995 - REVISED JANUARY 1997

<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>		DL PACKAGE DP VIEW)
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	OEA 1 CLKEN1B 2	
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model</li> </ul>	2B3 [] 3 GND [] 4 2B2 [] 5	54 2B4 53 GND
<ul> <li>(C = 200 pF, R = 0)</li> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	2B1 []6 V <sub>CC</sub> []7	51 2B6 50 V <sub>CC</sub>
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	A1 []8 A2 []9 A3 [] 10 GND [] 11	48 2B8 0 47 2B9
<ul> <li>Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages</li> </ul>	A4 [] 12 A5 [] 13 A6 [] 14	2 45 2B10 3 44 2B11
description	A7 [] 15 A8 [] 16	5 42 1B12 5 41 1B11
This 12-bit to 24-bit registered bus exchanger is designed for 2.3-V to 3.6-V $V_{CC}$ operation.	A9 [] 17 GND [] 18 A10 [] 19	3 39 GND
The SN74ALVCH16270 is used in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.	A11 20 A12 21 V <sub>CC</sub> 22	0 37 188 1 36 187
The device provides synchronous data exchange between the two ports. Data is stored in the	1B1 23 1B2 24 GND 25	3 34 1B6 4 33 1B5
internal registers on the low-to-high transition of the clock (CLK) input when the appropriate CLKEN inputs are low. The select (SEL) line	1B3 26 CLKEN2B 27	6 31 <b>]</b> 1B4

) IOW. I NE SEIECT (S selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path,

V CC L	22	35 U V CC
1B1 [		34 <b>]</b> 1B6
1B2 [		33 <b>]</b> 1B5
GND [	25	32 GND
1B3 🛛	26	31 🛛 1B4
CLKEN2B		30 CLKENA1
SEL [	28	29 CLK

with a single storage register in the A to 2B path. Proper control of the CLKENA inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables (OEA, OEB). The control terminals are registered to synchronize the bus direction changes with CLK.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16270 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16270 is characterized for operation from -40°C to 85°C.

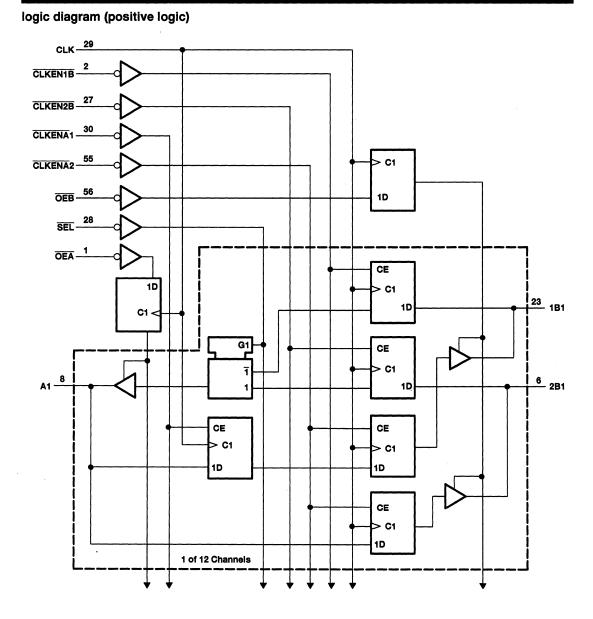
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# SN74ALVCH16270 **12-BIT TO 24-BIT REGISTERED BUS EXCHANGER** WITH 3-STATE OUTPUTS SCES028B – JULY 1995 – REVISED JANUARY 1997





# SN74ALVCH16270 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS SCES028B – JULY 1995 – REVISED JANUARY 1997

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST C	ONDITIONS	Vcc	MIN	TYPT	MAX	UNIT	
		l <sub>OH</sub> = -100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -C	).2			
		l <sub>OH</sub> = -6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2				
			V <sub>IH</sub> = 1.7 V	2.3 V	1.7				
VOH		IOH = -12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2			v	
			V <sub>IH</sub> = 2 V	3 V	2.4				
		I <sub>OH</sub> = -24 mA,	V <sub>IH</sub> = 2 V	3 V	2				
l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V			0.2				
		I <sub>OL</sub> = 6 mA,	V <sub>IL</sub> = 0.7 V	2.3 V			0.4		
VOL		1	V <sub>IL</sub> = 0.7 V	2.3 V			0.7	v	
		I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.8 V	2.7 V			0.4	0.4	
		I <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V			0.55		
h l		VI = V <sub>CC</sub> or GND		3.6 V			±5	μA	
VI = 0.7 V			2.3 V	45					
V <sub>I</sub> = 1.7 V			2.3 V	-45					
II(hold)		V <sub>1</sub> = 0.8 V		21	75			μΑ	
		V <sub>1</sub> = 2 V		3 V	-75				
		V <sub>I</sub> = 0 to 3.6 V <sup>‡</sup>		3.6 V			±500		
loz§		V <sub>O</sub> = V <sub>CC</sub> or GND		3.6 V			±10	μA	
ICC ·		VI = VCC or GND,	IO = 0	3.6 V			40	μA	
∆ICC		One input at V <sub>CC</sub> - 0.6 V,	Other inputs at VCC or GND	3 V to 3.6 V			750	μA	
Ci	Control inputs	VI = V <sub>CC</sub> or GND		3.3 V		3.5		pF	
Cio	A or B ports	Vo = Vcc or GND		3.3 V		9		pF	

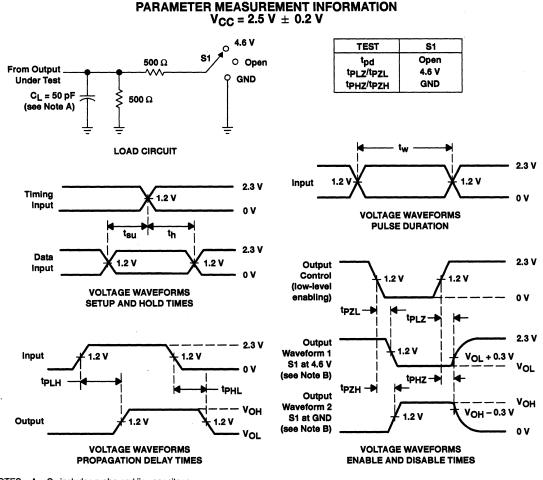
<sup>†</sup> All typical values are at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}$ C.

<sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.



### SN74ALVCH16270 **12-BIT TO 24-BIT REGISTERED BUS EXCHANGER** WITH 3-STATE OUTPUTS SCES028B - JULY 1995 - REVISED JANUARY 1997



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpHL and tpLH are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN74ALVCH16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES017B - JULY 1995 - REVISED JANUARY 1997

<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>		R DL PACK OP VIEW)	AGE
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	OEA		OEB
<ul> <li>Bus Hold on Data Inputs Eliminates</li> </ul>	LE1B C		CLKENA2
the Need for External Pullup/Pulldown	2B3 []: GND []4		2B4 GND
Resistors	2B2		2B5
<ul> <li>Packaged in Plastic Shrink Small-Outline</li> </ul>	2B2 US 2B1 [[6		2B5 2B6
(DL) and Thin Shrink Small-Outline (DGG)	V <sub>CC</sub>		V <sub>CC</sub>
Packages			2B7
	A2 0		2B7
description	A3 []		2B0 2B9
The double of bits and share while dealers of features			GND
This 12-bit to 24-bit bus exchanger is designed for	A4 1	· · · · · · · · · · · · · · · · · · ·	2B10
2.3-V to 3.6-V V <sub>CC</sub> operation.			2B10 2B11
The SN74ALVCH16271 is intended for applica-	A6 []	···	2B12
tions where two separate datapaths must be	A7 0		1B12
multiplexed onto, or demultiplexed from, a single	A8 []		1B11
datapath. This device is particularly suitable as an	A9 🛛		1B10
interface between conventional DRAMs and			GND
high-speed microprocessors.	A10		] 1B9
A data is stored in the internal A-to-B registers on	A11 0		] 1B8
the low-to-high transition of the clock (CLK) input,	A12		187
provided that the CLKENA inputs are low. Proper	Vcc		l v <sub>cc</sub>
control of these inputs allows two sequential	1B1 []:		1B6
12-bit words to be presented as a 24-bit word on	1B2 🛛		] 1B5
the B port.			GND
Transparent latches in the B-to-A path allow	1B3 [		1B4

Transparent latches in the B-to-A path allow asynchronous operation in order to maximize memory access throughput. These latches transfer data when the latch-enable ( $\overline{LE}$ ) inputs are low. The select ( $\overline{SEL}$ ) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables ( $\overline{OEA}$ ,  $\overline{OEB}$ ).

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To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

LE2B 27

SEL 28

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16271 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16271 is characterized for operation from -40°C to 85°C.

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notics.



30 CLKENA1

29 🛛 CLK

### SN74ALVCH16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS SCES017B - JULY 1995 - REVISED JANUARY 1997

### **Function Tables**

#### OUTPUT ENABLE

OUTPUT ENABLE					
INP	INPUTS		PUTS		
OEA	OEB	A 1B, 2B			
Н	н	Z	Z		
н	L	z	Active		
L	н	Active	z		
L	L	Active	Active		

### A-TO-B STORAGE (OEB = L)

	INPUTS			OUTI	PUTS
<b>CLKENA1</b>	CLKENA2	CLK	Α	1B	2B
н	Н	x	Х	1B0 <sup>†</sup>	2B0†
L	х	Ť	L	Lι	Х
L	х	<b>↑</b>	н	н	Х
х	L	Ť	L	×	L
x	L	Ŷ	н	Ao	н

### B-TO-A STORAGE (OEA = L)

B-TO-A OTOTIAGE (OEA = E)						
INPL	OUTPUT					
SEL	1B	2B	A			
x	Х	Х	A <sub>0</sub> †			
х	х	х	A0 <sup>†</sup> A0 <sup>†</sup>			
н	L	x	L			
н	н	х	н			
L	х	L	L L			
L	х	н	н			
	INPL SEL X X H H	INPUTS       SEL     1B       X     X       X     X       H     L       H     H       L     X	INPUTS           SEL         1B         2B           X         X         X           X         X         X           H         L         X           H         H         X           L         X         L			

<sup>†</sup> Output level before the indicated steady-state input conditions were established

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage range, V <sub>CC</sub>	-0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)	
	-0.5 V to V <sub>CC</sub> + 0.5 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	
Input clamp current, IIK (VI < 0)	
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3	3): DGG package 1 W
	DL package 1.4 W
Storage temperature range, Tstg	–65°C to 150°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.*



SN74ALVCH16272 **12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER** WITH 3-STATE OUTPUTS

SCES057B - OCTOBER 1995 - REVISED JANUARY 1997

			990 - REVISED JAN
<ul> <li>Member of the Texas Instruments</li> <li>Widebus™ Family</li> </ul>		R DL PACI TOP VIEW)	
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>		1 56 2 55	OEB CLKENA2
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown</li> </ul>	2B3 🛛	3 54	2B4
Resistors	GND 2B2		GND 2B5
Packaged in Plastic Shrink Small-Outline	2B1	6 51	2B6
(DL) and Thin Shrink Small-Outline (DGG) Packages		7 50 8 40	V <sub>CC</sub>   2B7
•	A2 [	9 48	2B8
description	A3 [		2B9
This 12-bit to 24-bit bus exchanger is designed for	GND 🛛 A4 🕇		GND 2B10
2.3-V to 3.3-V V <sub>CC</sub> operation.	A5 [	13 44	2B11
The SN74ALVCH16272 is intended for applica- tions where two separate datapaths must be	A6 [ A7 [		2B12
multiplexed onto, or demultiplexed from, a single	A7 U A8 []		1B12 1B11
datapath. This device is particularly suitable as an interface between conventional DRAMs and	A9 🚺	17 40	<b>]</b> 1B10
high-speed microprocessors.	GND [ A10 [		] GND ] 1B9
Data from the A inputs is stored in the internal	A10 L		1B9 1B8
registers on the low-to-high transition of the clock	A12	21 36	1B7
(CLK) input, when the CLKENA inputs are low. A two-stage pipeline is provided in each of the	V <sub>CC</sub> 1 1B1	22 35 23 34	] V <sub>CC</sub> ] 1B6
A-to-1B and A-to-2B paths to serve as a shallow	1B2 [	24 33	] 1B5
write buffer.	GND [		GND

Transparent latches are provided in the B-to-A path to allow asynchronous operation to maximize memory access throughput. These latches transfer data when the latch-enable (LE) inputs are low. The select (SEL) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables (OEA, OEB).

, . i V L		Ψ	103
A11	20	37	1B8
A12 [		36	1B7
V <sub>CC</sub>	22	35	V <sub>CC</sub>
1B1 [	23	34	1B6
1B2 🛛		33	1B5
GND [		32	GND
1B3 [	26	31	1B4
E2B	27	30	<b>CLKENA1</b>
SEL [	28	29	CLK

LE2

**PRODUCT PREVIEW** 

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16272 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16272 is characterized for operation from -40°C to 85°C.

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# SN74ALVCH16272 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS SCES057B - OCTOBER 1995 - REVISED JANUARY 1997

# **Function Tables**

#### OUTPUT ENABLE

	INP	UTS	OUTPUTS							
	OEA	OEB	A	1B, 2B						
-	н	н	Z	Z						
	н	L	z	Active						
	L	н	Active	z						
	L	L	Active	Active						

### A-TO-B STORAGE (OEB = L)

	OUT	PUTS			
CLKENA1	CLKENA2	CLK	A	1B	2B
н	н	x	Х	1B0†	2B0†
L	х	Ť	L	<u> </u> _t	x
L	х	Ť	н	нt	x
х	L	Ť	L	X	L
х	L	↑	н	Ao	н

Two CLK edges are needed to propagate data.

#### B-TO-A STORAGE (OEA = L)

	INPUTS							
LE	SEL	2B	A					
н	х	х	Х	A0‡				
н	х	х	х	A0‡ A0‡				
L	н	L	х	L				
L	н	н	Х	н				
L	L	х	L	L				
L	L	х	н	н				

<sup>‡</sup> Output level before the indicated steady-state input conditions were established



# SN74ALVCH16272 **12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER** WITH 3-STATE OUTPUTS

SCES057B - OCTOBER 1995 - REVISED JANUARY 1997

PAR	AMETER	TEST CO	ONDITIONS	Vcc	MIN	TYPT	MAX	UNIT
		l <sub>OH</sub> = –100 μA		2.3 V to 3.6 V	Vcc-0	.2		
		l <sub>OH</sub> =6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2			
Vou			V <sub>IH</sub> = 1.7 V	2.3 V	1.7			v
VOH		l <sub>OH</sub> = – 12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2			v
			V <sub>IH</sub> = 2 V	3 V	2.4			
		lOH = −24 mA,	V <sub>IH</sub> = 2 V	3 V	2			
		l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V			0.2	
		l <sub>OL</sub> = 6 mA,	V <sub>IL</sub> = 0.7 V	2.3 V			0.4	
VOL		I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 V	2.3 V			0.7	v
			V <sub>IL</sub> = 0.8 V	2.7 V			0.4	
		l <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V			0.55	
lj		V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V			±5	μA
		V <sub>I</sub> = 0.7 V		2.3 V	45			
		V <sub>I</sub> = 1.7 V		2.5 V	-45			
l(hold)		Vj = 0.8 V		3 V	75			μA
		V <sub>I</sub> = 2 V		37	-75			
		V <sub>I</sub> = 0 to 3.6 V‡		3.6 V			±500	
loz§		V <sub>O</sub> = V <sub>CC</sub> or GND		3.6 V			±10	μA
lcc		$V_{I} = V_{CC}$ or GND,	IO = 0	3.6 V			40	μA
∆lcc		One input at V <sub>CC</sub> – 0.6 V,	Other inputs at $V_{CC}$ or GND	3 V to 3.6 V			750	μA
Ci	Control inputs	VI = V <sub>CC</sub> or GND		3.3 V				pF
Cio	A or B ports	VO = VCC or GND		3.3 V				pF

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<sup>†</sup> Typical values are measured at V<sub>CC</sub> = 3.3 V,  $T_A$  = 25°C. <sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

 $\$  For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.



SN74ALVCH16282 18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS SCE5036A – JULY 1995 – REVISED AUGUST 1996

- Member of the Texas Instruments Widebus™ Family
- EPIC<sup>™</sup> (Enhanced-Performance Implanted CMOS) Sub-Micron Process
- ESD Protection Exceeds 2000 V Per MIL-STD883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Thin Shrink Small-Outline Package

#### description

The SN74ALVCH16282 is an 18-bit to 36-bit registered bus exchanger designed for 2.3-V to 3.6-V  $V_{CC}$  operation. This part is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. It is designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the CLK input. For data transfer in the B-to-A direction, SEL selects 1B or 2B data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output enable ( $\overline{OE}$ ) and the DIR input. The DIR control pin is registered to synchronize the bus direction changes with the clock.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16282 is characterized for operation from -40°C to 85°C.

V <sub>CC</sub> 1         80         V <sub>CC</sub> GND         2         79         GND           2B9         3         78         1B10           1B9         4         77         2B10           2B8         5         76         1B11           GND         6         75         GND           1B8         7         74         2B11           2B7         8         73         1B12           1B7         9         72         2B12           V <sub>CC</sub> 10         71         V <sub>CC</sub> 2B6         11         70         1B13           1B6         12         69         2B13           2B5         13         68         1B14           15         14         67         2B14           GND         15         66         GND           2B4         16         65         1B15           1B4         17         64         2B15           2B3         18         63         1B16           1B2         23         58         2B17           2B1         24         57         1B18	DBB PACKAGE (TOP VIEW)										
GND       2       79       GND         2B9       3       78       1B10         1B9       4       77       2B10         2B8       5       76       1B11         GND       6       75       GND         1B8       7       74       2B11         2B7       8       73       1B12         1B7       9       72       2B12         V <sub>CC</sub> 10       71       V <sub>CC</sub> 2B6       11       70       1B13         1B6       12       69       2B13         2B5       13       68       1B14         1B5       14       67       2B14         GND       15       66       GND         2B4       16       65       1B15         1B4       17       64       2B16         V <sub>CC</sub> 20       61       V <sub>CC</sub> GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56											
2B9       3       78       1B10         1B9       4       77       2B10         2B8       5       76       1B11         GND       6       75       GND         1B8       7       74       2B11         2B7       8       73       1B12         1B7       9       72       2B12         V <sub>CC</sub> 10       71       V <sub>CC</sub> 2B6       11       70       1B13         1B6       12       69       2B13         2B5       13       68       1B14         1B5       14       67       2B14         GND       15       66       GND         2B4       16       65       1B15         1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         V <sub>CC</sub> 20       61       V <sub>CC</sub> GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57			70								
1B9       4       77       2B10         2B8       5       76       1B11         GND       6       75       GND         1B8       7       74       2B11         2B7       8       73       1B12         1B7       9       72       2B12         V <sub>CC</sub> 10       71       V <sub>CC</sub> 2B6       11       70       1B13         1B6       12       69       2E13         2B5       13       68       1B14         1B5       14       67       2B14         GND       15       66       GND         2B4       16       65       1B15         1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         V <sub>CC</sub> 20       61       V <sub>CC</sub> GND       21       60       GND         281       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56	2B9 [		78	11B10							
2B8       5       76       1B11         GND       6       75       GND         1B8       7       74       2B11         2B7       8       73       1B12         1B7       9       72       2B12         V <sub>CC</sub> 10       71       V <sub>CC</sub> 2B6       11       70       1B13         1B6       12       69       2B13         2B5       13       68       1B14         1B5       14       67       2B14         GND       15       66       GND         2B4       16       65       1B15         1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         V <sub>CC</sub> 20       61       V <sub>CC</sub> GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       V <sub>CC</sub> A1       27       54 <td></td> <td></td> <td>77</td> <td></td>			77								
GND       6       75       GND         1B8       7       74       2B11         2B7       8       73       1B12         1B7       9       72       2B12         V <sub>CC</sub> 10       71       V <sub>CC</sub> 2B6       11       70       1B13         1B6       12       69       2B13         2B5       13       68       1B14         1B5       14       67       2B14         GND       15       66       GND         2B4       16       65       1B15         1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         V <sub>CC</sub> 20       61       V <sub>CC</sub> GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       V <sub>CC</sub> A1       27       54       A18         A2       28       53		5									
1B8       7       74       2B11         2B7       8       73       1B12         1B7       9       72       2B12         V <sub>CC</sub> 10       71       V <sub>CC</sub> 2B6       11       70       1B13         1B6       12       69       2B13         2B5       13       68       1B14         1B5       14       67       2B14         GND       15       66       GND         2B4       16       65       1B15         1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         V <sub>CC</sub> 20       61       V <sub>CC</sub> GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       V <sub>CC</sub> A1       27       54       A18         A2       28       53       A17         A3       29       52											
2B7       8       73       1B12         1B7       9       72       2B12         V <sub>CC</sub> 10       71       V <sub>CC</sub> 2B6       11       70       1B13         1B6       12       69       2B13         2B5       13       68       1B14         1B5       14       67       2B14         GND       15       66       GND         2B4       16       65       1B15         1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         V <sub>CC</sub> 20       61       V <sub>CC</sub> GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       2CC         A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51	1B8										
1B7       9       72       2B12         V <sub>CC</sub> 10       71       V <sub>CC</sub> 2B6       11       70       1B13         1B6       12       69       2B13         2B5       13       68       1B14         1B5       14       67       2B14         GND       15       66       GND         2B4       16       65       1B15         1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         V <sub>CC</sub> 20       61       V <sub>CC</sub> GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       V <sub>CC</sub> A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50	2B7 [	8									
2B6       11       70       1B13         1B6       12       69       2B13         2B5       13       68       1B14         1B5       14       67       2B14         GND       15       66       GND         2B4       16       65       1B15         1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         V <sub>CC</sub> 20       61       V <sub>CC</sub> GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       2CC         A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50       A15         A5       32       47       V <sub>CC</sub> A7       35       46	1B7 🛛	9		]2B12							
2B6       11       70       1B13         1B6       12       69       2B13         2B5       13       68       1B14         1B5       14       67       2B14         GND       15       66       GND         2B4       16       65       1B15         1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         V <sub>CC</sub> 20       61       V <sub>CC</sub> GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       2CC         A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50       A15         A5       32       47       V <sub>CC</sub> A7       35       46	Vcc										
1B6       12       69       2B13         2B5       13       68       1B14         1B5       14       67       2B14         GND       15       66       GND         2B4       16       65       1B15         1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         V <sub>CC</sub> 20       61       V <sub>CC</sub> GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       2B18         V <sub>CC</sub> 26       55       V <sub>CC</sub> A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50       A14         A6       33       48       A13         V <sub>CC</sub> 34       47	- 0D6 []	44	70	]1B13							
1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         VCC       20       61       VCC         GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       2CC         A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50       A15.         A5       32       49       A14         A6       33       48       A13         VCC       34       47       VCC         A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE	1B6 🛛	12	69	]2B13							
1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         VCC       20       61       VCC         GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       2CC         A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50       A15.         A5       32       49       A14         A6       33       48       A13         VCC       34       47       VCC         A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE	2B5 🛛	13	68	]1B14							
1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         VCC       20       61       VCC         GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       2CC         A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50       A15.         A5       32       49       A14         A6       33       48       A13         VCC       34       47       VCC         A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE	1B5 🛛	14	- · · ·								
1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         VCC       20       61       VCC         GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       2CC         A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50       A15.         A5       32       49       A14         A6       33       48       A13         VCC       34       47       VCC         A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE	GND	15									
1B4       17       64       2B15         2B3       18       63       1B16         1B3       19       62       2B16         VCC       20       61       VCC         GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       2CC         A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50       A15.         A5       32       49       A14         A6       33       48       A13         VCC       34       47       VCC         A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE	2B4 [	16									
1B3       19       62       2B16         V <sub>CC</sub> 20       61       V <sub>CC</sub> GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       2B18         V <sub>CC</sub> 26       55       V <sub>CC</sub> A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50       A15         A5       32       49       A14         A6       33       48       A13         V <sub>CC</sub> 34       47       V <sub>CC</sub> A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE	184 Ц	17									
V <sub>CC</sub> 20         61         V <sub>CC</sub> GND         21         60         GND           2B2         22         59         1B17           1B2         23         58         2B17           2B1         24         57         1B18           1B1         25         56         2B18           V <sub>CC</sub> 26         55         V <sub>CC</sub> A1         27         54         A18           A2         28         53         A17           A3         29         52         A16           GND         30         51         GND           A4         31         50         A15           A5         32         49         A14           A6         33         48         A13           V <sub>CC</sub> 34         47         V <sub>CC</sub> A7         35         46         A12           A8         36         45         A11           A9         37         44         A10           GND         38         43         GND           CLK         39         42         OE				=							
GND       21       60       GND         2B2       22       59       1B17         1B2       23       58       2B17         2B1       24       57       1B18         1B1       25       56       2B18         VCC       26       55       VCC         A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50       A15         A5       32       49       A14         A6       33       48       A13         VCC       34       47       VCC         A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE	1B3 [										
2B1       24       57       1B18         1B1       25       56       2B18         V <sub>CC</sub> 26       55       V <sub>CC</sub> A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50       A15         A5       32       49       A14         A6       33       48       A13         V <sub>CC</sub> 34       47       V <sub>CC</sub> A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE	Vcc	20	61								
2B1       24       57       1B18         1B1       25       56       2B18         V <sub>CC</sub> 26       55       V <sub>CC</sub> A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50       A15         A5       32       49       A14         A6       33       48       A13         V <sub>CC</sub> 34       47       V <sub>CC</sub> A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE	GND	21									
2B1       24       57       1B18         1B1       25       56       2B18         V <sub>CC</sub> 26       55       V <sub>CC</sub> A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50       A15         A5       32       49       A14         A6       33       48       A13         V <sub>CC</sub> 34       47       V <sub>CC</sub> A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE	2B2 [										
V <sub>CC</sub> 26         55         V <sub>CC</sub> A1         27         54         A18           A2         28         53         A17           A3         29         52         A16           GND         30         51         GND           A4         31         50         A15           A5         32         49         A14           A6         33         48         A13           V <sub>CC</sub> 34         47         V <sub>CC</sub> A7         35         46         A12           A8         36         45         A11           A9         37         44         A10           GND         38         43         GND           CLK         39         42         OE	1B2 [										
V <sub>CC</sub> 26         55         V <sub>CC</sub> A1         27         54         A18           A2         28         53         A17           A3         29         52         A16           GND         30         51         GND           A4         31         50         A15           A5         32         49         A14           A6         33         48         A13           V <sub>CC</sub> 34         47         V <sub>CC</sub> A7         35         46         A12           A8         36         45         A11           A9         37         44         A10           GND         38         43         GND           CLK         39         42         OE	281										
A1       27       54       A18         A2       28       53       A17         A3       29       52       A16         GND       30       51       GND         A4       31       50       A15         A5       32       49       A14         A6       33       48       A13         V <sub>CC</sub> 34       47       V <sub>CC</sub> A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE											
A2 28 53 A17 A3 29 52 A16 GND 30 51 GND A4 31 50 A15 A5 32 49 A14 A6 33 48 A13 V <sub>CC</sub> 34 47 V <sub>CC</sub> A7 35 46 A12 A8 36 45 A11 A9 37 44 A10 GND 38 43 GND CLK 39 42 OE											
A3       29       52       A16         GND       30       51       GND         A4       31       50       A15         A5       32       49       A14         A6       33       48       A13         V <sub>CC</sub> 34       47       V <sub>CC</sub> A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE		21									
A4       31       50       A15         A5       32       49       A14         A6       33       48       A13         V <sub>CC</sub> 34       47       V <sub>CC</sub> A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE	 ∆3 [	20									
A4       31       50       A15         A5       32       49       A14         A6       33       48       A13         V <sub>CC</sub> 34       47       V <sub>CC</sub> A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE	GND	29									
A5 32 49 A14 A6 33 48 A13 V <sub>CC</sub> 34 47 V <sub>CC</sub> A7 35 46 A12 A8 36 45 A11 A9 37 44 A10 GND 38 43 GND CLK 39 42 OE		31		-							
A6       33       48       A13         V <sub>CC</sub> 34       47       V <sub>CC</sub> A7       35       46       A12         A8       36       45       A11         A9       37       44       A10         GND       38       43       GND         CLK       39       42       OE											
V <sub>CC</sub> 34         47         V <sub>CC</sub> A7         35         46         A12           A8         36         45         A11           A9         37         44         A10           GND         38         43         GND           CLK         39         42         OE											
A8 [ 36 45 ] A11 A9 [ 37 44 ] A10 GND [ 38 43 ] GND CLK [ 39 42 ] OE	Vcc	34		-							
A8 36 45 A11 A9 37 44 A10 GND 38 43 GND CLK 39 42 OE	A7	35	46	1A12							
A9 37 44 A10 GND 38 43 GND CLK 39 42 OE	A8 🛙		45	<b>A</b> 11							
GND 38 43 GND CLK 39 42 OE	A9 🛙		44	<b>Ā</b> A10							
CLK <b>[]</b> 39 42 <b>]</b> OE	GND		43	GND							
	CLK		42	OE							
	SEL [	40		DIR							

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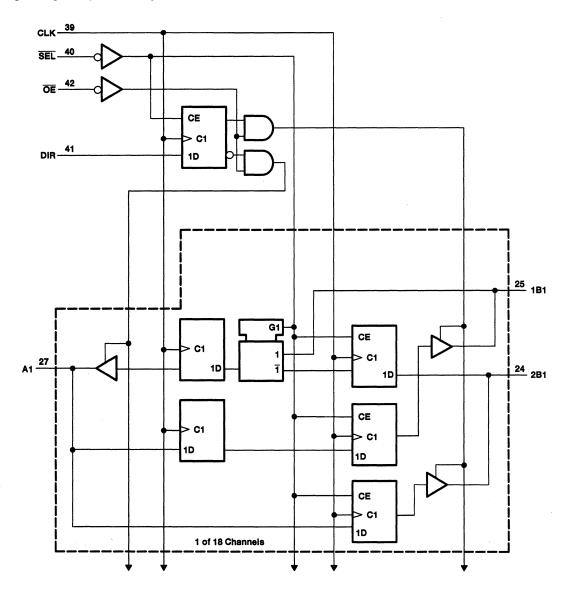
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# SN74ALVCH16282 18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS SCE5036A - JULY 1995 - REVISED AUGUST 1996

logic diagram (positive logic)





# SN74ALVCH16282 **18-BIT TO 36-BIT REGISTERED BUS EXCHANGER** WITH 3-STATE OUTPUTS SCES036A – JULY 1995 – REVISED AUGUST 1996

PARAMETER		TEST CONDITIONS			TYPT	MAX	UNIT
	I <sub>OH</sub> = -100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -0.	2		
	I <sub>OH</sub> =6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2			
Vari		V <sub>IH</sub> = 1.7 V	2.3 V	1.7			v
Vон	I <sub>OH</sub> = -12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2			v
		V <sub>IH</sub> = 2 V	3 V	2.4			
	I <sub>OH</sub> = -24 mA,	V <sub>IH</sub> = 2 V	3 V	2			
	lOL = 100 μA		2.3 V to 3.6 V			0.2	
	l <sub>OL</sub> = 6 mA,	V <sub>IL</sub> = 0.7 V	2.3 V			0.4	
VOL	I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 V	2.3 V			0.7	v
		V <sub>IL</sub> = 0.8 V	2.7 V			0.4	
	l <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V			0.55	
lı	V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V			±5	μA
	VI = 0.7 V	VI = 0.7 V VI = 1.7 V		45			
	VI = 1.7 V			-45			
l(hold)	Vi = 0.8 V		3V	75			μA
	Vi = 2 V			-75			
	VI = 0 to 3.6 V‡		3.6 V			±500	
loz\$	VO = VCC or GNI	D	3.6 V			±10	μA
lcc	V <sub>I</sub> = V <sub>CC</sub> or GND	, I <sub>O</sub> = 0	3.6 V			40	μA
∆ICC	One input at V <sub>CC</sub>	- 0.6 V, Other inputs at V <sub>CC</sub> or GNI	3 V to 3.6 V			750	μA
Ci Control i	nputs VI = V <sub>CC</sub> or GND		3.3 V		4		pF
Cio A or B po	orts VO = VCC or GNI	D	3.3 V		8.5		pF

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<sup>†</sup> Typical values are measured at  $V_{CC}$  = 3.3 V, T<sub>A</sub> = 25°C.

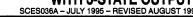
<sup>4</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another. § For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

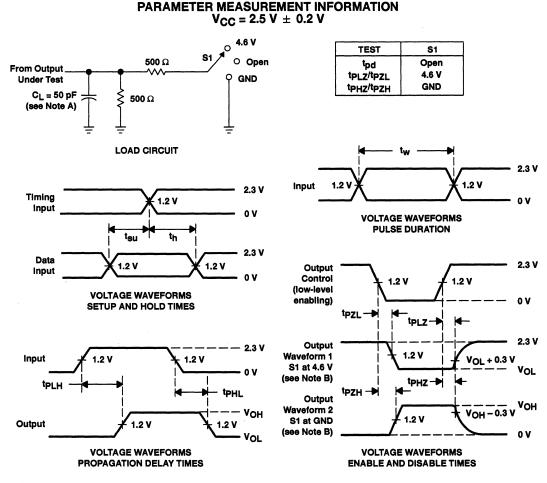
# timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

	·			CC = 2.5 V ± 0.2 V V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	
<sup>f</sup> clock	Clock frequency			150		150		150	MHz
tw	Pulse duration, CLK high or low		3.3		3.3		3.3		ns
		A data before CLK1	2.4		2.3		2		
+	Setup time	B data before CLK↑	2.2		2.2		1.8		ns
<sup>t</sup> su	Setup time	DIR before CLK1	2.2		2.1		1.7		
		SEL before CLK1	2		2		1.8		
		A data after CLK↑	0.5		0.5		0.7		
<b>.</b>	Hold time	B data after CLK↑	0.5		0.5		0.6		ns
th		DIR after CLK1	0.5		0.5		0.5		
		SEL after CLK1	0.7		0.7		0.8		



### SN74ALVCH16282 **18-BIT TO 36-BIT REGISTERED BUS EXCHANGER** WITH 3-STATE OUTPUTS SCES036A - JULY 1995 - REVISED AUGUST 1996





NOTES: A. CL includes probe and jig capacitance.

- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. B Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns,
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



SN74ALVCH16409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS SCES022A - JULY 1995 - REVISED NOVEMBER 1996

				REVISEDI
<ul> <li>Member of the Texas Instruments Widebus+™ Family</li> </ul>		OR DL P (TOP VII		AGE
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	PRE [ SEL0 [			CLK SELEN
<ul> <li>UBE ™ (Universal Bus Exchanger) Allows Synchronous Data Exchange</li> </ul>	1A1	3	54	1B1 GND
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V</li> </ul>	1A2 [ 1A3 [	5 6	52 51	1B2 1B3
Using Machine Model (C = 200 pF, R = 0)	V <sub>CC</sub> [ 1A4 [	8	49	V <sub>CC</sub> 1B4
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	1A5 [ 1A6 [	10	47	1B5 1B6
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	GND [ 1A7 [ 1A8 [	12	45	GND 1B7 1B8
Package Options Include Plastic 300-mil	1A9 [ 2A1 [	14	43	1B9 2B1
Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages	2A2 [ 2A3 [	16	41	2B2 2B3
description	GND [ 2A4 [		38	GND 2B4
This 9-bit, 4-port universal bus exchanger is designed for 2.3-V to 3.6-V V <sub>CC</sub> operation.	2A5 [ 2A6 [	21	36	2B5 2B6
The SN74ALVCH16409 allows synchronous data exchange between four different buses.	V <sub>CC</sub> [ 2A7 [	23	34	V <sub>CC</sub> 2B7
Data flow is controlled by the select (SEL0–SEL4) inputs. A data-flow state is stored on the rising	2A8 [ GND [	25	32	2B8 GND
edge of the clock (CLK) input if the select-enable (SELEN) input is low. Once a data-flow state has been established, data is <u>stored</u> in the flip-flop on	2A9 [ SEL1 [ SEL2 [	27	30	2B9 SEL4 SEL3
the rising edge of CLK if SELEN is high.				

The data-flow control logic is designed to allow glitch-free data transmission.

To ensure the high-impedance state during power up or power down, SELEN should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16409 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16409 is characterized for operation from -40°C to 85°C.

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# SN74ALVCH16409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS SCES022A - JULY 1995 - REVISED NOVEMBER 1996

DATA-FLOW CONTROL FUNCTION TABLE										
		DATA FLOW								
SELEN	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	DATA FLOW			
н	Ŷ	Х	Х	Х	X	х	No change			
L	î	0	0	0	0	0	None, all I/Os off			
L	Î	0	0	0	0	1	Not used			
L	Ŷ	0	0	0	1	0	Not used			
L	ſ	0	0	0	1	1	Not used			
L	ſ	0	0	1	0	0	Not used			
L	Ŷ	0	0	1	0	1	Not used			
L	ſ	0	0	1	1	0	Not used			
L	Ŷ	0	0	1	1	1	Not used			
L	î	0	1	0	0	0	2A to 1A and 1B to 2B			
L	ſ	0	1	0	0	1	2A to 1A			
L	î	0	1	0	1	0	2B to 1B			
L	ſ	0	1	0	1	1	2A to 1A and 2B to 1B			
L	ſ	0	1	· 1	0	0	1A to 2A and 1B to 2B			
L	î	0	1	1	0	1	1A to 2A			
L	î	0	1	1	1	0	1B to 2B			
L	î	0	1	1	1	1	1A to 2A and 2B to 1B			
L	ſ	1	0	0	0	0	1A to 1B and 2B to 2A			
L	î	1	0	0	0	1	1A to 1B			
L	î	1	0	0	1	0	2A to 2B			
L	î	1	0	0	1	1	1A to 1B and 2A to 2B			
L	Ŷ	1	0	1	0	0	1B to 1A and 2A to 2B			
L	î <sup>∙</sup>	1	0	1	0	1	1B to 1A			
L	Ŷ	1	0	1	1	0	2B to 2A			
L	î	1	0	1	1	1	1B to 1A and 2B to 2A			
L	ſ	1	1	0	0	0	2B to 1A and 2A to 1B			
L	î	1	1	0	0	1	1B to 2A			
L	Ŷ	1	1	0	1	0	2B to 1A			
L	Ŷ	1	1	0	1	1	2B to 1A and 1B to 2A			
LB	Ŷ	1	1	1	0	0	1A to 2B and 1B to 2A			
L	↑	1	1	1	0	1	1A to 2B			
L	Ŷ	1	1	1	1	0	2A to 1B			
L	Ŷ	1	1	1	1	1	1A to 2B and 2A to 1B			



# SN74ALVCH16409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES022A - JULY 1995 - REVISED NOVEMBER 1996

PARAMETER	TEST	CONDITIONS	Vcc	MIN TY	'PT MAX	UNIT	
	i <sub>OH</sub> = -100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -0.2			
	I <sub>OH</sub> = -6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2			
VOH		V <sub>IH</sub> = 1.7 V	2.3 V	1.7		v	
	I <sub>OH</sub> = -12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2		v	
		V <sub>IH</sub> = 2 V	3 V	2.4			
	I <sub>OH</sub> = -24 mA,	V <sub>IH</sub> = 2 V	3 V	2			
	l <sub>OL</sub> = 100 μA,		2.3 V to 3.6 V		0.2		
	I <sub>OL</sub> = 6 mA,	V <sub>IL</sub> = 0.7 V	2.3 V		0.4		
VOL	I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 V	2.3 V		0.7	v	
		VIL = 0.8 V	2.7 V		0.4		
	I <sub>OL</sub> = 24 mA,	VIL = 0.8 V	3 V		0.55		
lj –	V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V		±5	μA	
	V <sub>1</sub> = 0.7 V		2.3 V	45			
	V <sub>I</sub> = 1.7 V		2.5 V	-45			
l(hold)	V <sub>1</sub> = 0.8 V		3V	75		μA	
	V <sub>1</sub> = 2 V			-75			
	V <sub>I</sub> = 0 to 3.6 V <sup>‡</sup>		3.6 V		±500		
loz§	$V_{O} = V_{CC}$ or GND		3.6 V		±10	μA	
lcc	$V_1 = V_{CC}$ or GND,	IO = 0	3.6 V		40	μA	
∆ICC	One input at V <sub>CC</sub> – 0.6 V,	Other inputs at $V_{CC}$ or GND	3 V to 3.6 V		750	μA	
Ci Control input	s V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V		4	pF	
Cio A or B ports	VO = VCC or GND		3.3 V		8	pF	

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<sup>†</sup> All typical values are measured at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

<sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

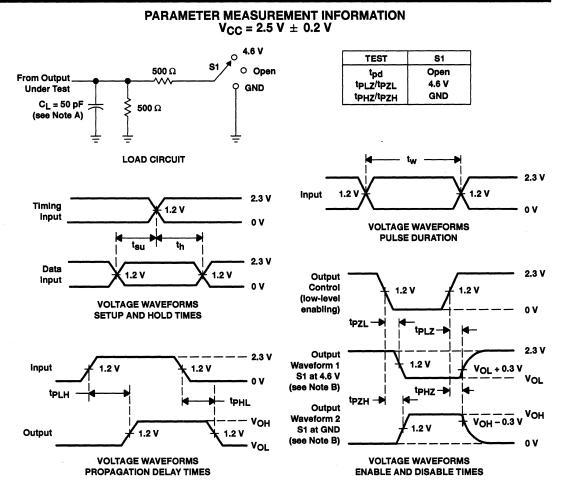
 $\$  For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V <sub>CC</sub> = 2.5 V ± 0.2 V		2.7 V	V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	120	0	120	0	120	MHz
tw	Pulse duration, CLK high or low		4.2		4.2		3		ns
		A or B before CLK1	1.9		1.9		1.4		ns
	Setup time	SEL before CLK1	5.1		4.2		3.5		
<sup>t</sup> su	Setup time	SELEN before CLK1	2.5		2.5		1.8		
		PRE before CLK1	1		1		0.7		
		A or B after CLK1	0.8		0.8		1		
th	t <sub>h</sub> Hold time	SEL after CLK1	0		0		0		ns
		SELEN after CLK1	0.5		0.5		0.8		



### SN74ALVCH16409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS SCES022A - JULY 1995 - REVISED NOVEMBER 1996



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpi 7 and tpH7 are the same as this.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



#### SN74ALVCHR162409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS sc

ES056A -	SEPTEN	ABER 1995 -	- REVISED	NOVEMBE

<ul> <li>Member of the Texas Instruments Widebus+<sup>™</sup> Family</li> </ul>	DGG OR DL PA (TOP VIEV	
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>		
<ul> <li>B-Port Outputs Have Equivalent 26-Ω</li> </ul>		40 1B1
Series Resistors, So No External Resistors are Required	GND 4 5	3 GND
•		2 1B2
● UBE™ (Universal Bus Exchanger) Allows		1 🛛 1B3
Synchronous Data Exchange	V <sub>CC</sub> [] 7 5	o]v <sub>cc</sub>
<ul> <li>ESD Protection Exceeds 2000 V Per</li> </ul>	1A4 🛛 8 4	9 <b>]</b> 1B4
MIL-STD-883, Method 3015; Exceeds 200 V	1A5 🛛 9 4	8 <b>]</b> 1B5
Using Machine Model	1A6 🚺 10 4	7 🛛 1B6
(C = 200 pF, R = 0)	GND 🚺 11 4	6 GND
<ul> <li>Latch-Up Performance Exceeds 250 mA</li> </ul>	1A7 🚺 12 4	5 🛛 1B7
Per JEDEC Standard JESD-17	1A8 🚺 13 4	4 🛛 1B8
<ul> <li>Bus Hold on Data Inputs Eliminates the</li> </ul>	1A9 🚺 14 4	3 <b>]</b> 1B9
Need for External Pullup/Pulldown	2A1 🚺 15 4	2 2B1
Resistors	2A2 🚺 16 4	1 2B2
	2A3 🚺 17 4	0 2B3
<ul> <li>Package Options Include Plastic Shrink</li> <li>Small Outline (DL) and This Shrink</li> </ul>	GND 🚺 18 3	9 🛛 GND
Small-Outline (DL) and Thin Shrink	2A4 🚺 19 3	8 2B4
Small-Outline (DGG) Packages	2A5 🛛 20 3	7 2B5
description	2A6 21 3	6 2B6
description	V <sub>CC</sub> [] 22 3	5] V <sub>CC</sub>
This 9-bit 4-port universal bus exchanger is		4 <b>[</b> ] 2B7
designed for 2.3-V to 3.6-V V <sub>CC</sub> operation.		3 🛛 2B8
		2 GND
The SN74ALVCHR162409 allows synchronous data exchange between four different buses. Data		1 <b>[</b> ] 2B9
		0 SEL4
flow is controlled by the select (SEL0–SEL4)		9 SEL3
inputs. A data-flow state is stored on the rising	· · · · · · · · · · · · · · · · · · ·	

select-enable (SELEN) input is low. Once a data-flow state is established, data is stored in the flip-flop on the rising edge of the CLK, provided SELEN is high.

The data-flow control logic is designed to allow glitch-free data transmission.

The B outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{\text{SELEN}}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCHR162409 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCHR162409 is characterized for operation from --40°C to 85°C.

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edge of the clock (CLK) input, provided the

PRODUCTION DATA information is current as of publication Products conform to specifications per the terms of Texas instru-standard warranty. Production processing does not necessarily in terms of all parameters sting of all pa



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# SN74ALVCHR162409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS SCES056A - SEPTEMBER 1995 - REVISED NOVEMBER 1996

		DATA	-FLOW	CONTRO	DL FUNG	CTION T	ABLE
			NPUTS				DATA FLOW
SELEN	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	DATA FLOW
н	Ť	х	x	Х	Х	х	No change
L	î	0	0	0	0	0	None, all I/Os off
L	î	0	0	0	0	1	Not used
L	î	0	0	0	1	0	Not used
L	ſ	0	0	0	1	1	Not used
L	Ť	0	0	1	0	0	Not used
L	î	0	0	1	0	1	Not used
L	ſ	0	0	1	1	0	Not used
L	î	0	0	1	1	1	Not used
L	Ŷ	0 -	1	0	0	0	2A to 1A and 1B to 2E
L	î	0	1	0	0	1	2A to 1A
L	î	0	1	0	1	0	2B to 1B
Ĺ	Ŷ	0	1	0	1	1	2A to 1A and 2B to 1E
L	î	0	1	1	0	0	1A to 2A and 1B to 2E
L	î	0	1	1	0	1	1A to 2A
L	î	0	1	1	1	0	1B to 2B
L	Ť	0	1	1	1	1	1A to 2A and 2B to 1E
L	ſ	1	0	0	0	0	1A to 1B and 2B to 2A
L	î	1	0	0	O	1	1A to 1B
L	î	1	0	0	1	0	2A to 2B
L	ſ	1	0	0	1	1	1A to 1B and 2A to 28
L	ſ	1	0	1	0	0	1B to 1A and 2A to 2B
L	ſ	1	0	1	0	1	1B to 1A
L	î	1	0	1	1	0	2B to 2A
L	Ť	1	0	1	1	1	1B to 1A and 2B to 2A
L	Ť	1	1	0	0	0	2B to 1A and 2A to 1E
L	Ŷ	1	1	0	0	1	1B to 2A
L	Ť	1	1	0	1	0	2B to 1A
L	î	1	1	Ο.	1	1	2B to 1A and 1B to 2A
L	Ť	1	1	1	0	0	1A to 2B and 1B to 2A
L	Ť	1	1	1	0	1	1A to 2B
L	Ť	1	1	1	1	0	2A to 1B
L	Ť	1	1	1	1	1	1A to 2B and 2A to 1E

DATA FLOW CONTROL SUNCTION TABLE



### SN74ALVCHR162409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS SCES056A - SEPTEMBER 1995 - REVISED NOVEMBER 1996

SOLSOSOR - SEP TEIMBER 1985 - REVISED NOVEMBER 1980

PARAMETER	TEST CONDITIONS	Vcc	MIN TYPT	MAX	UNIT	
	l <sub>OH</sub> = -100 μA	2.3 V to 3.6 V	V <sub>CC</sub> -0.2			
	l <sub>OH</sub> = -4 mA, V <sub>IH</sub> = 1.7 V	2.3 V	1.9			
	V <sub>IH</sub> = 1.7 V	2.3 V	1.7		v	
VOH	$I_{OH} = -6 \text{ mA}$ $V_{IH} = 2 \text{ V}$	3 V	2.4		v	
	$I_{OH} = -8 \text{ mA}, \qquad V_{IH} = 2 \text{ V}$	2.7 V	2			
	I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2 V	3 V	2			
	l <sub>OL</sub> = 100 μA	2.3 V to 3.6 V		0.2		
N	I <sub>OL</sub> = 4 mA, V <sub>IL</sub> = 0.7 V	2.3 V		0.4	v	
	$V_{IL} = 0.7 V$	2.3 V		0.55		
VOL	$I_{OL} = 6 \text{ mA}$ $V_{IL} = 0.8 \text{ V}$	3 V		0.55	v	
	I <sub>OL</sub> = 8 mA, V <sub>IL</sub> = 0.8 V	2.7 V		0.6		
	I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.8 V	3 V		0.8		
1	VI = V <sub>CC</sub> or GND	3.6 V		±5	μA	
	VI = 0.7 V	0.0.1/	45			
	V <sub>l</sub> = 1.7 V	2.3 V	-45		ł	
l(hold)	V <sub>1</sub> = 0.8 V	0.14	75		μA	
	V <sub>1</sub> = 2 V	3 V	-75			
	$V_1 = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V		±500		
loz§	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V		±10	μA	
lcc	$V_{I} = V_{CC} \text{ or GND}, \qquad I_{O} = 0$	3.6 V		40	μA	
AICC	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub>	or GND 3 V to 3.6 V		750	μA	
Ci Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	4		pF	
Cio A or B ports	$V_{O} = V_{CC}$ or GND	3.3 V	8		pF	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

<sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

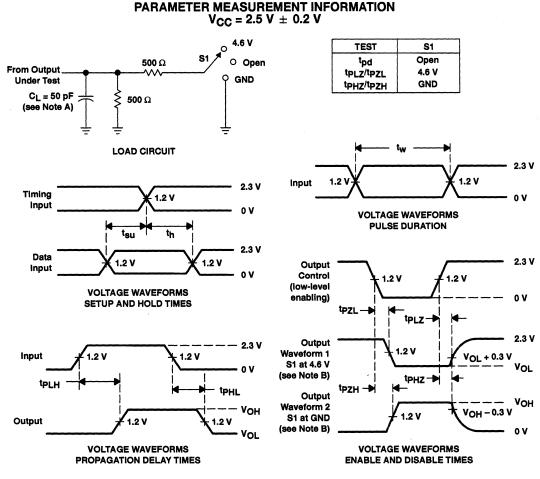
§ For I/O ports, the parameter IOZ includes the input leakage current.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	,			V <sub>CC</sub> = 2.5 V ± 0.2 V		2.7 V	V <sub>CC</sub> = 3.3V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	120	0	120	0	120	MHz
tw	Pulse duration	CLK high or low	4.2		4.2		3		ns
		A or B before CLK1	1.9		1.9		1.4		ns
	Setup time	SEL before CLK1	5.1		4.2		3.5		
<sup>t</sup> su	Setup time	SELEN before CLK1	2.5		2.5		1.8		
		PRE before CLK1	1		1		0.7		
		A or B after CLK1	0.8		0.8		1		
t <sub>h</sub>	t <sub>h</sub> Hold time	S after CLK1	0		0		0		ns
		SELEN after CLK1	0.5		0.5		0.8		

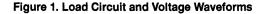


### SN74ALVCHR162409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS SCES056A - SEPTEMBER 1995 - REVISED NOVEMBER 1996



NOTES: A. C<sub>1</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \le 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \le 2.5 \text{ ns}$ ,  $t_f \le 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tod.





# SN74CBT16232 SYNCHRONOUS 16-BIT TO 32-BIT FET MULTIPLEXER/DEMULTIPLEXER

SCDS009F - MAY 1995 - REVISED AUGUST 1996

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages

### description

The SN74CBT16232 is a 16-bit to 32-bit synchronous switch used in applications in which two separate datapaths must be multiplexed onto, or demultiplexed from, a single path.

Two select inputs (S0 and S1) control the data flow. A clock (CLK) and a clock enable ( $\overline{\text{CLKEN}}$ ) synchronize the device operation. When  $\overline{\text{CLKEN}}$  is high, the bus switch remains in the last clocked function.

The SN74CBT16232 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

S1	S0	CLK	CLKEN	FUNCTION
X	х	X	н	Last state
L	L	Î ↑	L	Disconnect
L	н	Î ↑	L	A = B1 and A = B2
н	L	↑	L	A = B1
н	н	<b>↑</b>	L	A = B2

	or dl f (top vi		
1A 2B1 2B2 3A 4B1 4B2 5A 6B1 6B2 7A 6B2 7A 6B2 7A 0B1 10B2 11A 12B1 12B2 13A 14B2 14B2 14B1 16B2 14B1 16B2 15A 16B1 16B2 15A 16B1 16B2 15A 16B1 16B2 15A 16B1 16B2 15A 16B1 15A 16B2 15A 16B1 15A 16B1 15A 16B2 15A 16B1 15A 16B2 15A 16B2 15A 16B1 15A 16B2 15A 16B2 15A 16B1 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 15A 16B2 17 15A 16B2 17 15A 16B2 17 15A 16B2 17 15A 16B2 17 15A 16B2 17 15A 16B2 17 15A 16B2 17 15A 16B2 17 17 17 17 17 17 17 17 17 17	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27	56 55 53 52 51 50 49 48 47 46 45 44 43 42 41 40 38 37 36 33 32 31	] 1B1 ] 1B2 ] 2A ] 3B1 ] 3B2 ] 4A ] 5B1 ] 5B2 ] 6A ] 7B2 ] 8A D Vcc ] 9B1 ] 10A ] 11B1 ] 12A ] 13B1 ] 13B2 ] 14A ] 15B1 ] 15B2 ] 16A ] S0 ] S1

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



# SN74CBT16232 SYNCHRONOUS 16-BIT TO 32-BIT FET MULTIPLEXER/DEMULTIPLEXER

SCDS009F - MAY 1995 - REVISED AUGUST 1996

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	AMETER		TEST CON	DITIONS		MIN	TYPT	MAX	UNIT
VIK		V <sub>CC</sub> = 4.5 V,	lj = −18 mA					-1.2	v
lj lj		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V or GND					±1	μA
lcc		V <sub>CC</sub> = 5.5 V,	I <sub>O</sub> = 0,	VI = VCC or GI	ND			3	μA
∆lcc <sup>‡</sup>	Control pins	V <sub>CC</sub> = 5.5 V,	One input at 3.4 V,	Other inputs at	V <sub>CC</sub> or GND			2.5	mA
CI	Control pins	V <sub>1</sub> = 3 V or 0					4.5		pF
0	A port	N		S0 = 0, S1 = 0		6.5			
Cio(OFF)	B port	$-V_0 = 3 V \text{ or } 0,$	CLKEN = 0,		S1 = 0		4		pF
		V <sub>CC</sub> = 4 V,	V <sub>I</sub> = 2.4 V,	lj = 15 mA			14	20	
r <sub>on</sub> §			V <sub>1</sub> = 0,	lı = 64 mA			5	7	
		V <sub>CC</sub> = 4.5 V	V <sub>1</sub> = 0,	lj = 30 mA			5	7	Ω
			$V_1 = 2.4 V_2$	lı = 15 mA			10	15	

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>‡</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

S Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER				V <sub>CC</sub> = 4 V		UNIT	
	·			MAX	MIN	MAX		
fclock	Clock frequency		.0	150	0	150	MHz	
<sup>t</sup> w	Pulse duration	CLK high or low	3.3		3.3		ns	
	······································	S0, S1 before CLK↑	1.9		2.2			
tsu	Setup time	CLKEN before CLK1	1.9		2.4		ns	
		S0, S1 after CLK1	1	1	0.5			
<sup>t</sup> h	Hold time	CLKEN after CLK1	1.8		1.9		ns	

# switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V ± 0.5 V		V <sub>CC</sub> = 4 V	
			MIN	MAX	MIN	MAX	
fmax			150		150		MHz
<sup>t</sup> pd <sup>¶</sup>	A or B	B or A		0.25		0.25	ns
<sup>t</sup> pd	CLK	A or B	2	5.8		6.1	ns
<sup>t</sup> en	CLK	A, B1, B2	1.8	6.2		6.8	ns
t <sub>en</sub>	CLK	B1 or B2	3.1	7.9		8.5	ns
<sup>t</sup> dis	CLK	A or B	1.9	6.2		5.8	ns

This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).



# SN74CBT16233 16-BIT TO 32-BIT FET MULTIPLEXER/DEMULTIPLEXER

SCDS010D - MAY 1995 - REVISED AUGUST 1996

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages

#### description

The SN74CBT16233 is a 16-bit to 32-bit switch used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, where two different banks of memory need to be addressed simultaneously. The SN74CBT16233 can be used as two 8-bit to 16-bit multiplexers or as one 16-bit to 32-bit multiplexer.

Two select inputs (SEL1 and SEL2) control the data flow. When the TEST inputs are asserted, the A port is connected to both the B1 and the B2 ports. SEL1, SEL2, and the TEST inputs can be driven with a 5-V CMOS, a 5-V TTL, or a low-voltage TTL driver.

The SN74CBT16233 is specified by design not to have through current when switching directions.

The SN74CBT16233 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		FUNCTION
SEL		
L	L	A = B1
н	L	A = B2
x	н	A = B1 and A = B2

DGG OR DL PACKAGE (TOP VIEW)           1A         1         56         1B1           2B1         2         55         1B2           2B2         3         54         2A           3A         4         53         3B1           4B1         5         52         3B2           4B2         6         51         4A           5A         7         50         5B1           6B1         8         49         5B2           6B2         9         48         6A           7A         10         47         7B1           8B1         11         46         7B2           8B2         12         45         8A           GND         13         44         GND           VCC         14         43         VCC           9A         15         42         9B1           10B1         16         41         9B2           10B2         17         40         10A           11A         18         39         11B1           12B1         19         38         11B2           12B2         20         37			
1A [ 2B1 ] 2B2 ] 3A ] 4B1 ] 4B2 ] 5A ] 6B1 ] 6B2 ] 7A ] 8B2 ] 6B2 ] 7A ] 8B2 ] 7A ] 8B2 ] 7A ] 10B1 ] 12B1 ] 12B2 ] 11A ] 12B1 ] 12B2 ] 13A ] 14B1 ] 14B1 ] 14B1 ] 14B1 ] 14B1 ]	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23	56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34	] 1B1 ] 1B2 ] 2A ] 3B1 ] 3B2 ] 4A ] 5B1 ] 5B2 ] 6A ] 7B2 ] 8A ] GND ] V <sub>CC</sub> ] 9B1 ] 9B1 ] 9B2 ] 10A ] 11B1 ] 11B2 ] 12A ] 13B1 ] 13B2 ] 14A ] 15B1
	27 28	30 29	SEL1 SEL2



# SN74CBT16233 16-BIT TO 32-BIT FET MULTIPLEXER/DEMULTIPLEXER

SCDS010D - MAY 1995 - REVISED AUGUST 1996

#### recommended operating conditions

		MIN	MAX	UNIT
Vcc	Supply voltage	4.75	5.25	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	0	70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER		TEST CONDITIONS		MIN	TYPT	MAX	UNIT
VIK		V <sub>CC</sub> = 4.75 V,	lı = –18 mA				-1.2	V
1.		$V_{CC} = 0$	VI = 5.25 V				10	μA
կ		V <sub>CC</sub> = 5.25 V,	VI = 5.25 V or GND				±1	μA
ICC		V <sub>CC</sub> = 5.25 V,	I <sub>O</sub> = 0,	VI = V <sub>CC</sub> or GND			3	μA
∆lcc‡	Control pins	V <sub>CC</sub> = 5.5 V,	One input at 3.4 V,	Other inputs at $V_{CC}$ or GND			2.5	mA
CI	Control pins	V <sub>I</sub> = 3 V or 0				4.5		pF
Cio(OFF	)	V <sub>O</sub> = 3 V or 0				4		pF
			V <sub>1</sub> = 0,	lj = 64 mA		5	7	
r <sub>on</sub> §		V <sub>CC</sub> = 4.75 V	V <sub>1</sub> = 2.4 V,	lj = 30 mA		5	7	Ω
			VI = 2.4 V,	lj = 15 mA		7	12	

<sup>†</sup> All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^{\circ}C$ .

<sup>‡</sup>This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

§ Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A, B) terminals.

# switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 0°C TO 70°C		UNIT
	(INFOT)	(001201)	MIN	MAX	
tpd <sup>¶</sup>	A or B	B or A		0.25	ns
<sup>t</sup> pd	SEL	A	1.6	5.3	ns
t <sub>en</sub>	TEST or SEL	В	1.3	5.2	ns
tdis	TEST OF SEL	В	1	5.3	115

This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).



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DGG	ORD	DL PA	CKA	GE

•	Member of the Texas Instruments
	<i>Widebus</i> ™ Family

- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

### description

The SN74ALVCH16344 is a 1-bit to 4-bit address driver used in applications where four separate memory locations must be addressed by a single address.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16344 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16344 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INP	JTS	OUTPUT
ŌĒ	A	BN
L	н	Н
L	L	L
н	н	z

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# SN74ALVCH16344 1-TO-4 ADDRESS DRIVER WITH 3-STATE OUTPUTS SCES054B – SEPTEMBER 1995 – REVISED NOVEMBER 1996

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	0.5 V to V <sub>CC</sub> + 0.5 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±50 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>CC</sub> )	±50 mA
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG package	1 W
DL package .	1.4 W
Storage temperature range, T <sub>sto</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.*

# recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
V	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.7		v
ViH	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2		v
	Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
VIL		$V_{CC} = 2.7 V$ to 3.6 V		0.8	v
Vi	Input voltage		0	VCC	V
Vo	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 2.3 V		-12	
юн	High-level output current	V <sub>CC</sub> = 2.7 V		-12	mA
		V <sub>CC</sub> = 3 V		-24	
		V <sub>CC</sub> = 2.3 V		12	
IOL	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
		V <sub>CC</sub> = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



# switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> pd	A	В	1.3	5.2		4.6	1.4	4	ns
t <sub>en</sub>	ŌĒ	В	1.1	6.7		6.2	1.2	5.1	ns
<sup>t</sup> dis	ŌĒ	В	1.5	5.3		4.4	1.2	4	ns
<sup>t</sup> sk(o) <sup>†</sup>								0.35	ns
<sup>t</sup> sk(o) <sup>‡</sup>								0.5	ns

<sup>†</sup> Skew between outputs of same bank and same package (same transition). This parameter is warranted but not production tested.

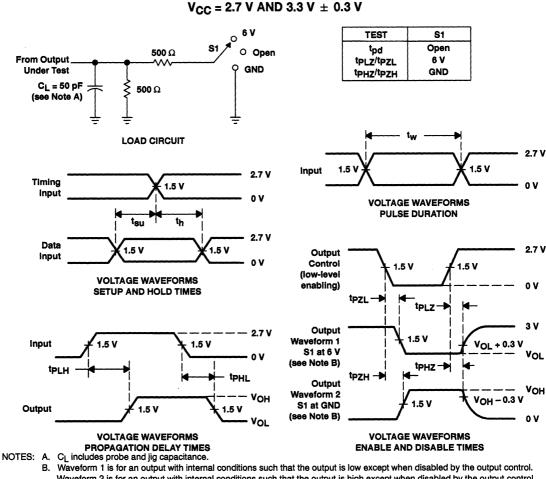
\$ Skew between outputs of all banks and same package (A1 through A8 tied together). This parameter is warranted but not production tested.

# operating characteristics, T<sub>A</sub> = 25°C

PARAMETER			TEST CON	DITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT	
						ТҮР		
	Power dissipation capacitance	Outputs enabled	С <sub>L</sub> = 50 рF,	f = 10 MHz	68	84	рF	
Cpd	C <sub>pd</sub> Power dissipation capacitance	Outputs disabled			11	14	ρr	



### SN74ALVCH16344 1-TO-4 ADDRESS DRIVER WITH 3-STATE OUTPUTS SCES054B - SEPTEMBER 1995 - REVISED NOVEMBER 1996



# PARAMETER MEASUREMENT INFORMATION

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. tpLz and tpHz are the same as tdis.

F.  $t_{PZL}$  and  $t_{PZL}$  are the same as  $t_{en}$ .

G.  $t_{PLL}$  and  $t_{PLH}$  are the same as  $t_{Dd}$ .

Figure 2. Load Circuit and Voltage Waveforms



<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	DGG OR DL PACKAGE (TOP VIEW)
<ul> <li>EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	OE1 1 56 OE4
<ul> <li>Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required</li> </ul>	1B2 3 54 8B2 GND 4 53 GND
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown</li> </ul>	1B3 [] 5 52 [] 8B3 1B4 [] 6 51 [] 8B4 V <sub>CC</sub> [] 7 50 [] V <sub>CC</sub>
Resistors     Package Options Include Plastic 300-mil	1A [] 8 49 ] 8A 2B1 [] 9 48 ] 7B1
Shrink Small-Outline (DGG) and Thin Shrink Small-Outline (DL) Packages	2B2 0 10 47 0 7B2 GND 0 11 46 0 GND 2B3 0 12 45 0 7B3
description	2B4 13 44 7B4
The SN74ALVCH162344 is a 1-bit-to-4-bit address driver used in applications where four separate memory locations must be addressed by a single address.	2A 14 43 7A 3A 15 42 6A 3B1 16 41 6B1 3B2 17 40 6B2
The outputs, which are designed to sink up to 12 mA, include 26- $\Omega$ resistors to reduce overshoot and undershoot.	GND   18 39   GND 3B3   19 38   6B3 3B4   20 37   6B4 4A   21 36   5A
To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V <sub>CC</sub> through a pullup resistor; the minimum value of	V <sub>CC</sub> 22 35 V <sub>CC</sub> 4B1 23 34 5B1 4B2 24 33 5B2
the resistor is determined by the current-sinking capability of the driver.	GND 25 32 GND 4B3 26 31 5B3 4B4 27 30 5B4

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH162344 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

OE2 28

29 0E3

The SN74ALVCH162344 is characterized for operation from -40°C to 85°C.

	A-TO-B FUNCTION TABLE				
I	INP	UTS	OUTPUT		
I	ŌĒ	Α	Bn		
ſ	L	н	н		
	L	L	L		
	н	х	z		

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 4.6 V
Input voltage range, V <sub>1</sub> (see Note 1)	–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, IIK (VI < 0)	
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 3): DGG	package 1 W
DL pa	ackage 1.4 W
Storage temperature range, T <sub>stg</sub>	65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

### recommended operating conditions (see Note 4)

		· · · ·	MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	ν
V		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v
VIH	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2		v
		input voltage V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
VIL	Low-level input voltage V <sub>CC</sub> = 2.7 V to 3.6 V		1	0.8	v
VI	Input voltage			Vcc	V
Vo	Output voltage		0	Vcc	v
		V <sub>CC</sub> = 2.3 V		-6	
ЮН		V <sub>CC</sub> = 2.7 V		-8	mA
		V <sub>CC</sub> = 3 V		-12	
		V <sub>CC</sub> = 2.3 V	1	6	
IOL	Low-level output current	V <sub>CC</sub> = 2.7 V		8	mA
	V <sub>CC</sub> = 3 V			12	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

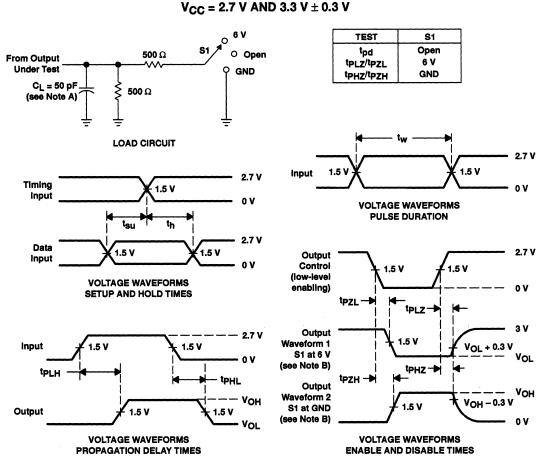


# SN74ALVCH162344 1-TO-4 ADDRESS DRIVER WITH 3-STATE OUTPUTS SCES085A - AUGUST 1996 - REVISED OCTOBER 1996

operating characteristics, T<sub>A</sub> = 25°C

	PARAMETER			TEST CONDITIONS		V <sub>CC</sub> = 3.3 V ± 0.3 V TYP	UNIT
<b>C</b> .	Power dissipation capacitance	Outputs enabled	0.0	f = 10 MHz			рF
Cpd	Power dissipation capacitance	Outputs disabled	C <sub>L</sub> = 0,				pr



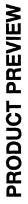


PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub>  $\leq 2.5$  ns, t<sub>f</sub>  $\leq 2.5$  ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as  $t_{en}$ .
- G. tpHL and tpLH are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms





- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- High-Impedance State During Power Up
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Plastic 300-mil Thin Shrink Small-Outline Package

### description

This 1-bit-to-4-bit address register/driver is designed for 2.3-V to 3.6-V  $V_{CC}$  operation. The device is ideal for use in applications where a single address bus is driving four separate memory locations. The SN74ALVCH16831 can be used as a buffer or a register, depending on the logic level of the select (SEL) input.

When  $\overline{\text{SEL}}$  is logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable ( $\overline{\text{OE}}$ ) controls. Each  $\overline{\text{OE}}$  controls two groups of nine outputs.

When  $\overline{\text{SEL}}$  is logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, data set up at the A inputs is stored in the internal registers.  $\overline{\text{OE}}$  controls operate the same as in buffer mode.

When  $\overline{OE}$  is logic low, the outputs are in a normal logic state (high or low logic level). When  $\overline{OE}$  is logic high, the outputs are in the high-impedance state.

SEL or  $\overline{OE}$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When  $V_{CC}$  is between 0 and 1.2 V, the device is in the high-impedance state during power up. However, to ensure the high-impedance state above 1.2 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DBB PACKAGE (TOP VIEW)					
4Y1 [		80 1Y2			
3Y1 [	• •				
GND [		79 2Y2 78 GND			
2Y1 [	-	77 3Y2			
1Y1		76 4Y2			
Vcc [	4 ~	75 V <sub>CC</sub>			
NC [		74 1 1Y3			
A1 [		73 2Y3			
GND [		72 GND			
NC		71 3Y3			
A2 [		70 4Y3			
GND [	12	69 GND			
NC [		68 🚺 1Y4			
A3 [		67 2Y4			
Vcc [		66 VCC			
NC [	16	65 3Y4			
A4 [		64 🛛 4Y4			
GND [	18	63 GND			
CLK [		62 🛛 1Y5			
OE1 [		61 2Y5			
OE2		60 3Y5			
SEL [		59 4Y5			
GND [		58 GND			
A5 [		57 ] 1Y6			
A6 [		56 2Y6			
V <sub>CC</sub> [		55 V <sub>CC</sub>			
A7 [		54 3Y6			
NC [		53 4Y6			
GND		52 GND			
A8		51 1Y7			
NC [		50 2Y7			
GND		49 GND			
A9 [		48 3Y7			
NC [		47 4Y7			
		46 V <sub>CC</sub>			
4Y9 [		45 1Y8			
3Y9 [ GND [		44 2Y8 43 GND			
		- E			
		E			
1Y9 [	40	41 4Y8			

NC - No internal connection

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ Input voltage range, $V_{I}$ (see Note 1) Output voltage range, $V_{O}$ (see Notes 1 and 2) Input clamp current, $I_{IK}$ ( $V_{I} < 0$ ) Output clamp current, $I_{OK}$ ( $V_{O} < 0$ or $V_{O} > V_{CC}$ ) Continuous output current, $I_{O}$ ( $V_{O} = 0$ to $V_{CC}$ ) Continuous current through each $V_{CC}$ or GND Maximum power dissipation at $T_{A} = 55^{\circ}$ C (in still air) (see Note 3) Storage temperature range, $T_{stg}$	-0.5 V to 4.6 V -0.5 V to V <sub>CC</sub> + 0.5 V -50 mA ±50 mA ±50 mA ±100 mA 0.84 W
---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	---------------------------------------------------------------------------------------------------------

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - 2. This value is limited to 4.6 V maximum.
  - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.*

### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage			3.6	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v
VIH	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2		v
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
VIL	Low-level input voltage V <sub>CC</sub> = 2.7 V to 3.6 V				v
VI	Input voltage				V
Vo	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 2.3 V	Τ	-12	
юн	High-level output current	V <sub>CC</sub> = 2.7 V	1	-12	mA
		V <sub>CC</sub> = 3 V		-24	
		V <sub>CC</sub> = 2.3 V	Τ	12	
IOL	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
		V <sub>CC</sub> = 3 V		24	
∆t/∆v	Input transition rise or fall rate		0	10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		μs/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



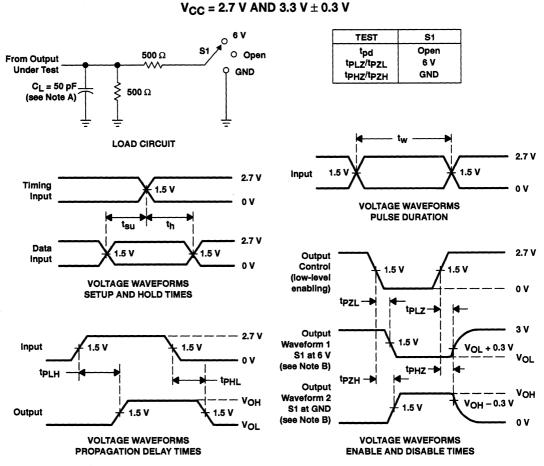
# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = ± 0.3	3.3 V 3 V	UNIT
	(INFOT)		MIN	MAX	MIN	MAX	MIN	MAX	1
fmax			150		150		150		MHz
	A								
<sup>t</sup> pd	CLK	Y							ns
	SEL								
ten	ŌĒ	Y							ns
<sup>t</sup> dis	ŌĒ	Y							ns

### operating characteristics, T<sub>A</sub> = 25°C

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V TYP	V <sub>CC</sub> = 3.3 V ± 0.3 V TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled Outputs disabled	C <sub>L</sub> = 0 pF, f = 10 MHz			рF



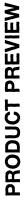


PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpi 7 and tpHZ are the same as tdis.
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G. tpHL and tpLH are the same as tpd.

### Figure 2. Load Circuit and Voltage Waveforms





- Member of the Texas Instruments *Widebus*™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- High-Impedance State During Power Up
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Plastic 300-mil Thin Shrink Small-Outline Package

### description

This 1-bit-to-4-bit address register/driver is designed for 2.3-V to 3.6-V V<sub>CC</sub> operation. The device is ideal for use in applications where a single address bus is driving four separate memory locations. The SN74ALVCH162831 can be used as a buffer or a register, depending on the logic level of the select (SEL) input.

When  $\overline{\text{SEL}}$  is logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable ( $\overline{\text{OE}}$ ) controls. Each  $\overline{\text{OE}}$  controls two groups of nine outputs.

When  $\overline{\text{SEL}}$  is logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, data set up at the A inputs is stored in the internal registers.  $\overline{\text{OE}}$  controls operate the same as in buffer mode.

When  $\overline{OE}$  is logic low, the outputs are in a normal logic state (high or low logic level). When  $\overline{OE}$  is logic high, the outputs are in high-impedance state.

SEL or  $\overline{OE}$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include  $26-\Omega$  resistors to reduce overshoot and undershoot.

DBB PACKAGE (TOP VIEW)					
4Y1	ΓŪ	80 1Y2			
3Y1		80 1Y2 79 2Y2			
GND		78 GND			
2Y1		77 3Y2			
1Y1		76 4Y2			
Vcc		75 V <sub>CC</sub>			
NC		74 1 1Y3			
A1		73 2Y3			
GND		72 GND			
NC	10	71 🚺 3Y3			
A2	11	70 4Y3			
GND	12	69 🛛 GND			
NC		68 🕽 1Y4			
A3 [		67 2Y4			
V <sub>CC</sub>		66 🛛 V <sub>CC</sub>			
NC		65 🛛 3Y4			
A4		64 <b>]</b> 4Y4			
GND		63 GND			
CLK		62 1Y5			
OE1		61 2Y5			
OE2		60 3Y5			
SEL		59 4Y5			
GND		58 GND			
A5 (		57 1Y6			
A6		56 2Y6			
V <sub>CC</sub>		55 V <sub>CC</sub> 54 3Y6			
A7 NC		<b>H</b>			
GND		53 4Y6 52 GND			
A8		51 1Y7			
NC		50 2Y7			
GND		49 GND			
A9		48 3Y7			
NC		47 4Y7			
Vcc					
4Y9		45 1Y8			
3Y9		44 2Y8			
GND		43 🖥 GND			
2Y9	39	42 <b>[</b> 3Y8			
1Y9	40	41 <b>4</b> Y8			

NC - No internal connection

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notice.



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3)	0.84 W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - 2. This value is limited to 4.6 V maximum.
  - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.3	3.6	٧
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v
ViH	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2	2.3 3.6 1.7	v
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
VIL	Low-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2.3 3.6 1.7 2 0.7 0.8 0 V <sub>CC</sub> 0 V <sub>CC</sub> -6 -8 -12 6 8 12 0 10 200	v	
VI	Input voltage		0	VCC	V
Vo	Output voltage		0	VCC	٧
		V <sub>CC</sub> = 2.3 V		-6	
ЮН	High-level output current	V <sub>CC</sub> = 2.7 V	1	-8	mA
		V <sub>CC</sub> = 3 V		$\begin{array}{cccc} 2.3 & 3.6 \\ 1.7 & & \\ 2 & & \\ & & 0.7 \\ & & 0.8 \\ 0 & V_{CC} \\ 0 & V_{CC} \\ & & -6 \\ & & -6 \\ & & -6 \\ & & -6 \\ & & -12 \\ & & 6 \\ & & & \\ & & 12 \\ & & 0 & 10 \\ 00 \\ \end{array}$	
		V <sub>CC</sub> = 2.3 V		6	
IOL	Low-level output current	V <sub>CC</sub> = 2.7 V		8	mA
		V <sub>CC</sub> = 3 V		12	
∆t/∆v	Input transition rise or fall rate		0	10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		μs/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



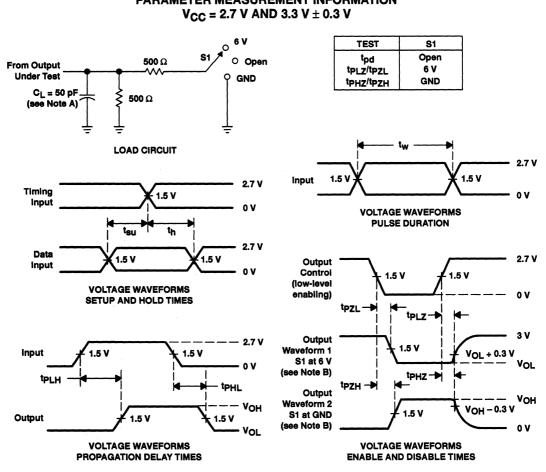
# switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.:	2.5 V 2 V	V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = ± 0.3	3.3 V 3 V	UNIT
	(111-01)	(001-01)	MIN	MAX	MIN	MAX	MIN	MAX	
fmax			150		150		150		MHz
	A								
<sup>t</sup> pd	CLK	Y							ns
	SEL								
<sup>t</sup> en	ŌĒ	Y							ns
<sup>t</sup> dis	ŌĒ	Y							ns

### operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER		TEST CO	NDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V TYP	V <sub>CC</sub> = 3.3 V ± 0.3 V TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled Outputs disabled	C <sub>L</sub> = 0 pF,	f = 10 MHz			pF





# PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq 2.5$  ns, t<sub>f</sub>  $\leq 2.5$  ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpHL and tpLH are the same as tod.

### Figure 2. Load Circuit and Voltage Waveforms



•	Member of the Texas Instruments <i>Widebus</i> ™ Family		or dl (top v		
•	EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process				]CLK
•	ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)	1Q1 1Q2 GND 2Q1	3 4	54 53 52	D1 NC GND D2
•	Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17	2Q2 [ V <sub>CC</sub> [ 3Q1 [	7	50	] NC ] V <sub>CC</sub> ] D3
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors	3Q2 4Q1 GND	9 10	48 47	] NC ] D4 ] GND
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages	4Q2 [ 5Q1 [ 5Q2 ]	12 13 14	45 44 43	] NC ] D5 ] NC
esc	cription	6Q1 [ 6Q2 [	16	41	D6 NC
	This 10-bit flip-flop is designed for 2.3-V to 3.6-V $V_{CC}$ operation.	7Q1 GND 7Q2	18 19	39 38	] D7 ] GND ] NC
	The flip-flops of the SN74ALVCH16820 are	8Q1 [	20	37	] D8

edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

de

A buffered output-enable (OE) input can be used to place the ten outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

3Q2 [	9	48	] NC
4Q1 [	10	47	] D4
GND [		46	GND
4Q2 [	12	45	] NC
5Q1 [	13	44	D5
5Q2 [	14	43	] NC
6Q1 [	15	42	] D6
6Q2 [			] NC
7Q1 [	17	40	D7
GND [	18	39	GND
7Q2	19	38	] NC
8Q1 [	20	37	] D8
8Q2 [			] NC
V <sub>CC</sub> [	22	35	Vcc
9Q1 [	23	34	] D9
9Q2 [		33	] NC
GND [			] GND
10Q1 [	26	31	D10
10Q2 [		30	NC
20E	28	29	NC

NC - No internal connection

1

OE input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16820 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16820 is characterized for operation from -40°C to 85°C.

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### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	v
		$V_{CC} = 2.3 V \text{ to } 2.7 V$	1.7		v
VIH	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2	2.3 3.6 1.7	v
M.,		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
VIL	Low-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	v
VI	Input voltage		0	VCC	v
Vo	Output voltage		0	Vcc	v
		V <sub>CC</sub> = 2.3 V		-12	
юн	High-level output current	V <sub>CC</sub> = 2.7 V		-12	mA
		V <sub>CC</sub> = 3 V		-24	
		V <sub>CC</sub> = 2.3 V		12	
IOL	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
		V <sub>CC</sub> = 3 V		2.3 3.6 .7 2 0.7 0.8 0 V <sub>CC</sub> -12 -12 -24 12 12 24 0 10	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

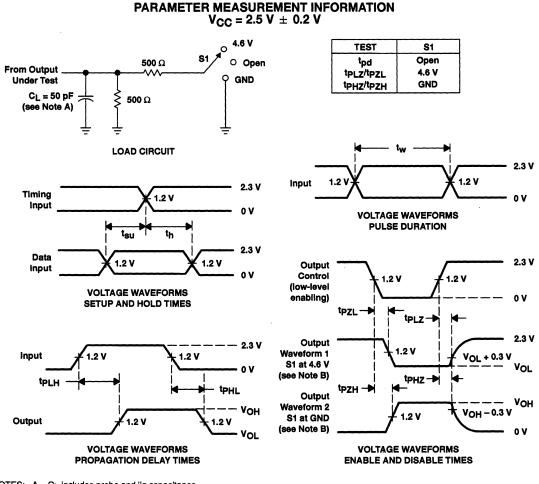
PA	RAMETER	TEST C	ONDITIONS	Vcc	MIN	түрт	MAX	UNIT
		I <sub>OH</sub> = -100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -0.2	2		
		I <sub>OH</sub> = -6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2			
			V <sub>IH</sub> = 1.7 V	2.3 V	1.7			v
VOH		IOH = -12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2			v
			V <sub>IH</sub> = 2 V	3 V	2.4			
		lон = -24 mA,	V <sub>IH</sub> = 2 V	3 V	2			
		l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V			0.2	
$\sim$		i <sub>OL</sub> = 6 mA,	VIL = 0.7 V	2.3 V			0.4	
VOL		10 = 10	VIL = 0.7 V	2.3 V			0.7	v
		I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.8 V	2.7 V			0.4	
		i <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V			0.55	
h		VI = VCC or GND		3.6 V			±5	μA
		VI = 0.7 V		0.9.1/	45			
		VI = 1.7 V		− 2.3 V	-45			
l(hold)		VI = 0.8 V		3V	75			μA
		V <sub>1</sub> = 2 V		<b>]</b> <sup>3</sup>	-75			
		V <sub>1</sub> = 0 to 3.6 V <sup>‡</sup>		3.6 V			±500	
loz		V <sub>O</sub> = V <sub>CC</sub> or GND		3.6 V			±10	μА
ICC		$V_{I} = V_{CC}$ or GND,	lO = 0	3.6 V			40	μA
∆lcc		One input at V <sub>CC</sub> - 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA
	Control inputs			0.014		3.5		- 5
Ci	Data inputs	$V_{I} = V_{CC}$ or GND		3.3 V		6		pF
Co	Outputs	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V		7		pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C. <sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.



### SN74ALVCH16820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS

SCES035A - JULY 1995 - REVISED NOVEMBER 1996



- NOTES: A. CL includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.

### Figure 1. Load Circuit and Voltage Waveforms



### SN74ALVCH162820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS BEB 1996

SCES012A – JULY	1995 – REVISED NOVEM

● Member of the Texas Instruments <i>Widebus</i> ™ Family	DGG OR DL PACKAGE (TOP VIEW)
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	
<ul> <li>Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required.</li> </ul>	1Q2 [] 3 54 ] NC GND [] 4 53 ] GND 2Q1 [] 5 52 ] D2
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model</li> </ul>	2Q2 [] 6 51 ] NC V <sub>CC</sub> [] 7 50 ] V <sub>CC</sub> 3Q1 [] 8 49 ] D3
<ul> <li>(C = 200 pF, R = 0)</li> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	3Q2 [] 9 48 ] NC 4Q1 [] 10 47 ] D4 GND [] 11 46 ] GND
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	4Q2 [] 12 45 [] NC 5Q1 [] 13 44 [] D5 5Q2 [] 14 43 [] NC
<ul> <li>Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages</li> </ul>	6Q1 0 15 42 0 D6 6Q2 0 16 41 0 NC 7Q1 0 17 40 0 D7 GND 0 18 39 0 GND
description	7Q2 19 38 NC
This 10-bit flip-flop is designed for 2.3-V to 3.6-V $V_{CC}$ operation.	8Q1 [] 20 37 [] D8 8Q2 [] 21 36 [] NC V <sub>CC</sub> [] 22 35 [] V <sub>CC</sub>
The SN74ALVCH162820 flip-flops are edge- triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device	9Q1 [] 23 34 ]] D9 9Q2 [] 24 33 ]] NC GND [] 25 32 ]] GND
provides true data at the Q outputs. A buffered output-enable ( $\overline{OE}$ ) input can be used	10Q1 []26 31 ]]D10 10Q2 []27 30 ]]NC 2OE []28 29 ]]NC

to place the eight outputs in either a normal logic state (high or low logic levels) or a highimpedance state. In the high-impedance state,

NC - No internal connection

the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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# SN74ALVCH162820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS SCES012A – JULY 1995 – REVISED NOVEMBER 1996

### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
		$V_{CC} = 2.3 V \text{ to } 2.7 V$	1.7		v
VIH	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2		v
v		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
VIL	Low-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		2.3 3.6 .7 2 0.7 0.8 0 V <sub>CC</sub> 0 V <sub>CC</sub> -6 -6 -8 -12 6 8 12 0 10	v
VI	Input voltage		0	VCC	V
Vo	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 2.3 V		-6	
ЮН	High-level output current	V <sub>CC</sub> = 2.7 V		8	mA
		V <sub>CC</sub> = 3 V		-12	
		V <sub>CC</sub> = 2.3 V		6	
IOL	Low-level output current	V <sub>CC</sub> = 2.7 V		8	mA
		V <sub>CC</sub> = 3 V		$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



### SN74ALVCH162820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS SCES012A – JULY 1995 – REVISED NOVEMBER 1996

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V <sub>CC</sub> = ± 0.	2.5 V 2 V	V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	0	150	0	150	0	150	MHz
tw	Pulse duration, CLK high or low	3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before CLK1	1.7		1.8		1.4		ns
t <sub>h</sub>	Hold time, data after CLK <sup>↑</sup>	1.1		1.1		1		ns

# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figures 1 and 2)

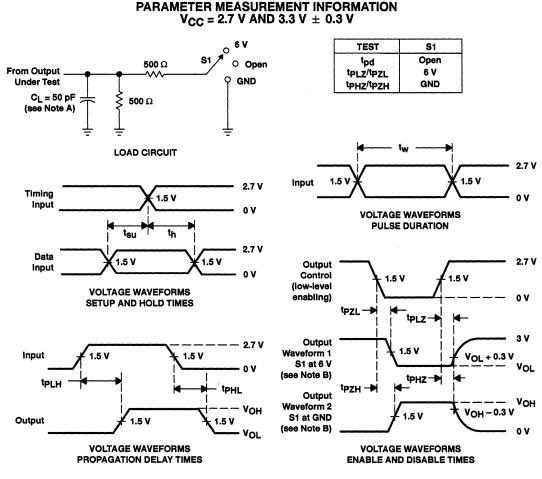
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.	2.5 V 2 V	V <sub>CC</sub> = 2.7 V		7 V V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
	((((-01)	(001401)	MIN	MAX	MIN	MAX	MIN	MAX	
fmax			150		150		150		MHz
<sup>t</sup> pd	CLK	Q	1	7		6.2	1	5.4	ns
<sup>t</sup> en	ŌĒ	Q	1	7.4		6.8	1	5.6	ns
<sup>t</sup> dis	ŌĒ	Q	1.3	6.4		5.5	1	5	ns

### operating characteristics, T<sub>A</sub> = 25°C

	PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V TYP	V <sub>CC</sub> = 3.3 V ± 0.3 V TYP	UNIT	
<u> </u>	Dewer dissignation consultance	Outputs enabled		68	66	pF	
C <sub>pd</sub> Power dissipation capacitance		Outputs disabled	C <sub>L</sub> = 50 pF, f = 10 MHz	39	47	рг	



### SN74ALVCH162820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS SCES012A – JULY 1995 – REVISED NOVEMBER 1996



- NOTES: A. CL includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzi and tpzH are the same as ten.
  - G. tpHL and tpLH are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Member of the Texas Instruments *Widebus*™ Family
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

### description

This 16-bit universal bus driver is designed for 2.3-V to 3.6-V  $V_{CC}$  operation.

Data flow from A to Y is controlled by the output-enable ( $\overline{OE}$ ) input. The device operates in the transparent mode when the latch-enable ( $\overline{LE}$ ) input is low. The A data is latched if the clock (CLK) input is held at a high or low logic level. If  $\overline{LE}$  is high, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLK. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16334 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16334 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)				
OE Y1 Y2 GND Y3 Y4 Vcc GND Y7 GND Y10 GND Y10 GND Y10 GND Y10 Y10 Y10 Y10 Y10 Y10 Y10 Y10	TOP VII 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19	48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30	CLK A1 A2 GND A3 A4 V <sub>CC</sub> A5 A6 GND A7 A8 A9 A10 GND A11 A12 V <sub>CC</sub> A13	
Y13	19	30	A13	
Y14 GND Y15	21	28	] A14 ] GND ] A15	
Y16		26	A16	

NC - No internal connection

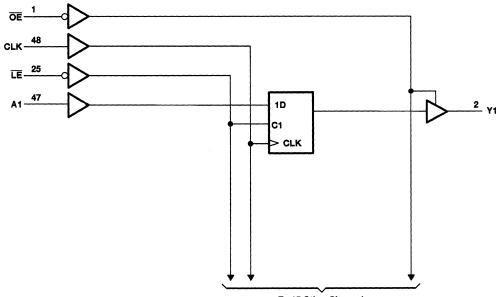
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logic diagram (positive logic)



To 15 Other Channels

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ Input voltage range, $V_I$ (see Note 1) Output voltage range, $V_O$ (see Notes 1 and 2) Input clamp current, $I_{IK}$ ( $V_I < 0$ ) Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) Continuous current through each $V_{CC}$ or GND Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG package	-0.5 V to 4.6 V 0.5 V to V <sub>CC</sub> + 0.5 V 50 mA ±50 mA ±50 mA ±100 mA e
	1.2 W

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.* 



### SN74ALVCH16334 **16-BIT UNIVERSAL BUS DRIVER** WITH 3-STATE OUTPUTS SCES090 - OCTOBER 1996

PAR	AMETER	TEST CONDITIONS		Vcc	MIN	TYPT	MAX	UNIT
		I <sub>OH</sub> = -100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -0.	2		
		I <sub>OH</sub> =6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2			
Val			V <sub>IH</sub> = 1.7 V	2.3 V	1.7			v
VOH		I <sub>OH</sub> = -12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2			
			V <sub>IH</sub>	3 V	2.4			
		IOH =24 mA,	V <sub>IH</sub> = 2 V	3 V	2			
		l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V			0.2	
		l <sub>OL</sub> = 6 mA,	V <sub>IL</sub> = 0.7 V	2.3 V			0.4	v
VOL		I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 V	2.3 V			0.7	
			V <sub>IL</sub> = 0.8 V	2.7 V			0.4	
		l <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V			0.55	
4		V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V			±5	μA
		Vj = 0.7 V		2.3 V	45			
		VI = 1.7 V 2.		2.5 V	-45			
l <sub>hold</sub>		Vj = 0.8 V		3 V	75			μA
		V <sub>I</sub> = 2 V		37	-75			
		VI = 0 to 3.6 V‡		3.6 V			±500	
loz§		VO = VCC or GND		3.6 V			±10	μA
lcc		VI = V <sub>CC</sub> or GND,	IO = 0	3.6 V			40	μA
∆lcc		One input at V <sub>CC</sub> - 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA
<u> </u>	Control inputs			3.3 V				<b></b>
Ci	Data inputs	VI = V <sub>CC</sub> or GND		3.3 V				pF
Co	Outputs	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V				pF

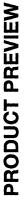
### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V.
 <sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

§ For I/O ports, the parameter IOZ includes the input leakage current.

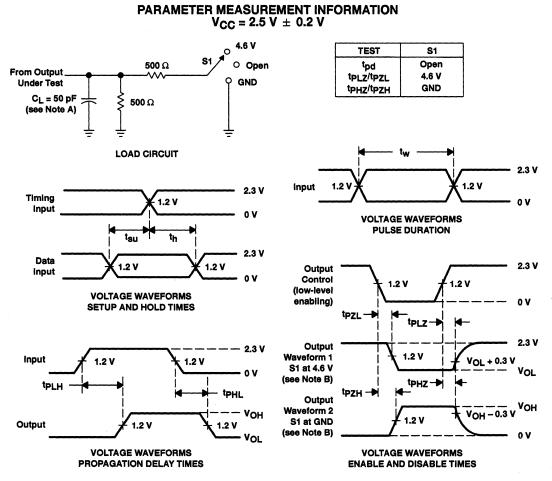
# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V <sub>CC</sub> = 2.5 V ± 0.2 V				V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MIN MAX		
fclock	Clock frequency								MHz	
tw	Pulse duration	LE low	1						ns	
		CLK high or low								
	Setup time	Data before CLK1							ns	
tsu		Data before LE1, CLK high								
		Data before LET, CLK low								
th	Hald time	Data after CLK↑							ns	
	Hold time	Data after LE↑, CLK high or low								





### SN74ALVCH16334 16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS SCES090 - OCTOBER 1996



- NOTES: A. CL includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns,
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpi H and tpHi are the same as tpd.

### Figure 1. Load Circuit and Voltage Waveforms





SCBS647A -	AUGUST	1995 - REV	ISED OCTO

DGG OR DL PACKAGE (TOP VIEW) 

4Y4 23

40E 1 24

•	State-of-the-Art Advanced Low-Voltage BICMOS Technology (ALB) Design for 3.3-V
	Operation

- **Member of the Texas Instruments** Widebus™ Family
- Schottky Diodes on All Inputs to Eliminate **Overshoot and Undershoot**
- Industry Standard '16244 Pinout
- Distributed V<sub>CC</sub> and GND Pin Configuration **Minimizes High-Speed Switching Noise**
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

### description

The SN74ALB16244 16-bit buffer and line driver is designed for high-speed, low-voltage (3.3-V) V<sub>CC</sub> operation. This device is intended to replace the conventional driver in any speed-critical path. The small propagation delay is achieved using a unity gain amplifier on the input and feedback resistors from input to output, which allows the output to track the input with a small offset voltage.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical active-low output-enable (OE) inputs.

The SN74ALB16244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)					
INPUTS OUTPUT					
ŌĒ	A	Y			
L	н	н			
Lι	L	L L			

х

z

н

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	LIQUOINAIN UL	10/43 111311 411101113	nicorporateu.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas instruments standard warranty. Production processing does not necessarily include testing of all parameters.



1 OE		48	20E
1Y1 [	2	47	] 1A1
1Y2 [	3	46	] 1A2
GND [	4	45	GND
1Y3 🕻	5		] 1A3
1Y4 [		43	] 1A4
V <sub>CC</sub> [		42	v <sub>cc</sub>
2Y1 [	8	41	] 2A1 ] 2A2
2Y2 [			
GND [			] GND
2Y3 [	11		] 2A3
2Y4 [		37	<b>2</b> A4
3Y1 [	13		] 3A1
3Y2 [	14		3A2
GND [		34	] GND
3Y3 🕻	16	33	] 3A3
3Y4 🕻			<b>]</b> 3A4
V <sub>CC</sub> [	18	31	] v <sub>cc</sub>
4Y1		30	4A1
4Y2		29	4A2
GND		28	GND
4Y3	22	27	4A3

26 🛛 4A4

25 1 3OE

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### SN74ALB16244 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS SCB5647A – AUGUST 1995 – REVISED OCTOBER 1996

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	-0.5 V to 4.6 V
Input voltage range, V <sub>1</sub> : Except I/O ports (see Note 1)	
	–0.5 V to V <sub>CC</sub> + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	–0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, IIK (VI < 0)	–50 mA
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see No	te 3): DGG package 1 W
	DL package 1.4 W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.*

### recommended operating conditions

÷	· · · · · · · · · · · · · · · · · · ·		MIN	MAX	UNIT
Vcc	Supply voltage		3	3.6	V
юн‡	High-level output current			-18	mA
lol‡	Low-level output current	· · · · · · · · · · · · · · · · · · ·		18	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		5	ns/V
TA	Operating free-air temperature		-40	85	°C

<sup>‡</sup> Refer to Figures 1 and 2 for typical I/O ranges.



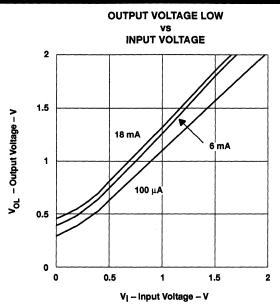


Figure 2. VOL Over Recommended Free-Air Temperature Range

switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 3)

PARAMETER	FROM	то	Vcc=	= 3.3 V ±	0.3 V	UNIT
FARAMETER	(INPUT)	(OUTPUT)	MIN	TYPT	MAX	UNIT
<sup>t</sup> pd	Α	Y	0.8	1.6	2.2	ns
<sup>t</sup> en	ŌE	Y	2.5	3.4	4.4	ns
<sup>t</sup> dis	ŌĒ	Y	2	2.9	4	ns

<sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.



### SN74ALVCH16244 **16-BIT BUFFER/DRIVER** WITH 3-STATE OUTPUTS SCES014A - JULY 1995 - REVISED NOVEMBER 1996

•	Member of the Texas Instruments <i>Widebus</i> ™ Family		OR DL (TOP \		
•	<i>EPIC</i> ™ (Enhanced-Performance Implanted CMOS) Submicron Process				20E
•	ESD Protection Exceeds 2000 V Per	1Y1 [ 1Y2 [			] 1A1 ] 1A2
	MIL-STD-883, Method 3015; Exceeds	GND			GND
	200 V Using Machine Model (C = 200 pF,	1Y3			] 1A3
	R = 0)	1Y4 🛛		43	] 1A4
•	Latch-Up Performance Exceeds 250 mA	V <sub>CC</sub> [	7	42	] v <sub>cc</sub>
	Per JEDEC Standard JESD-17	2Y1 [	8		2A1
•	Bus Hold on Data Inputs Eliminates the	2Y2	-		2A2
	Need for External Pullup/Pulldown				GND
	Resistors	2Y3 [			2A3
•	Package Options Include Plastic 300-mil	2Y4 [			] 2A4
	Shrink Small-Outline (DL) and Thin Shrink	3Y1 [			] 3A1
	Small-Outline (DGG) Packages	3Y2 [			] 3A2
des	cription	GND [ 3Y3 [	1		] GND ] 3A3
400		3Y3 [			] 3A3 ] 3A4
	This 16-bit buffer/driver is designed for 2.3-V to	V <sub>CC</sub>			
	3.6-V V <sub>CC</sub> operation.	4Y1			] 4A1
	The SN74ALVCH16244 is designed specifically	4Y2 [	1		4A2
	to improve both the performance and density of	GND			GND
	3-state memory address drivers, clock drivers,	4Y3 [			4A3
	and bus-oriented receivers and transmitters.	4Y4 [			] 4A4
	The device can be used as four 4-bit buffers, two	40E [			3 OE

8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low outputenable (OE) inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16244 is characterized for operation from -40°C to 85°C.

### FUNCTION TABLE (each 4-bit buffer)

INPL	JTS	OUTPUT
OE	Α	Y
L	Н	н
L	L	L
н	х	z

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PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	
Input voltage range, VI (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, IIK (VI < 0)	
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	
Continuous current through each V <sub>CC</sub> or GND	
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG package	0.85 W
	1.2 W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

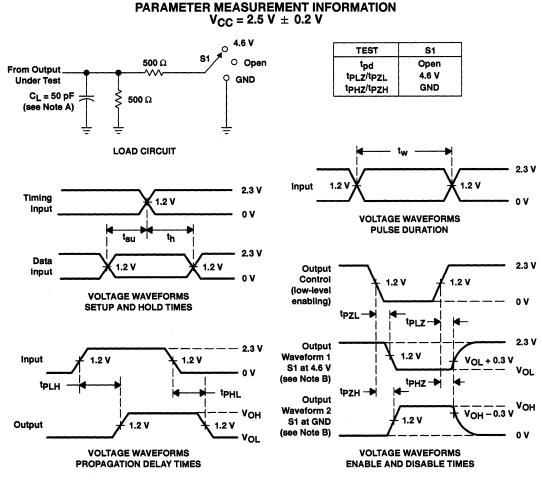
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.* 

### recommended operating conditions (see Note 4)

		- · · · · · · · · · · · · · · · · · · ·	MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
V	High-level input voltage	$V_{CC} = 2.3 V \text{ to } 2.7 V$	1.7		v
VIH		$V_{CC} = 2.7 V \text{ to } 3.6 V$	2		v
V.,	Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
VIL	Low-level liput voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	v
۷	Input voltage	· · · · · · · · · · · · · · · · · · ·	0	VCC	v
Vo	Output voltage		0	VCC	V
		V <sub>CC</sub> = 2.3 V		-12	
юн	High-level output current	V <sub>CC</sub> = 2.7 V		-12	mA
		V <sub>CC</sub> = 3 V		-24	
		V <sub>CC</sub> = 2.3 V		12	
OL	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
		V <sub>CC</sub> = 3 V		24	
∆t/∆v	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.





NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCES065A	- JANUARY	1996 - R	EVISED	NOVEMBER

<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	DGG OR DL (TOP V	
<ul> <li>EPIC<sup>™</sup> (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>		48 20E
<ul> <li>Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required.</li> </ul>	1Y2 3 GND 4 1Y3 5	47 1 1A1 46 1 1A2 45 1 GND 44 1 1A3
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model</li> </ul>	1Y4 6 V <sub>CC</sub> 7 2Y1 8	440 1A3 430 1A4 420 V <sub>CC</sub> 410 2A1
<ul> <li>(C = 200 pF, R = 0)</li> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	2Y2 9 GND 10 2Y3 11	40 2A2 39 GND 38 2A3
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	2Y4   12 3Y1   13 3Y2   14	37 2A4 36 3A1 35 3A2
<ul> <li>Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages</li> </ul>	GND    15 3Y3    16 3Y4    17	34 GND 33 3A3 32 3A4
description	V <sub>CC</sub> 18 4Y1 19	31 V <sub>CC</sub> 30 4A1
This 16-bit buffer/driver is designed for 2.3-V to 3.6-V V <sub>CC</sub> operation.	4Y2 20 GND 21	29 4A2 28 GND
The SN74ALVCH162244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.	4Y3 [ 22 4Y4 [ 23 4OE [ 24	27 4A3 26 4A4 25 30E

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable (OE) inputs.

The outputs, which are designed to sink up to 12 mA, include 26- $\Omega$  resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH162244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)				
INPL	JTS	OUTPUT		
ŌĒ	Α	Y		
L	н	н		
L	L	L		
н	х	z		

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RODUCTION DATA information is current as of publication date. roducts conform to specifications per the terms of Texas instruments andard warranty. Production processing does not necessarily include standard wa

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ Input voltage range, $V_I$ (see Note 1) Output voltage range, $V_O$ (see Notes 1 and 2) Input clamp current, $I_{IK}$ ( $V_I < 0$ ) Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) Continuous current through each $V_{CC}$ or GND Maximum power dissipation at $T_{V_O} = 5^{\circ}C$ (in still air) (see Note	-0.5 V to 4.6 V -0.5 V to V <sub>CC</sub> + 0.5 V -50 mA ±50 mA ±50 mA ±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note	
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.*

### recommended operating conditions (see Note 4)

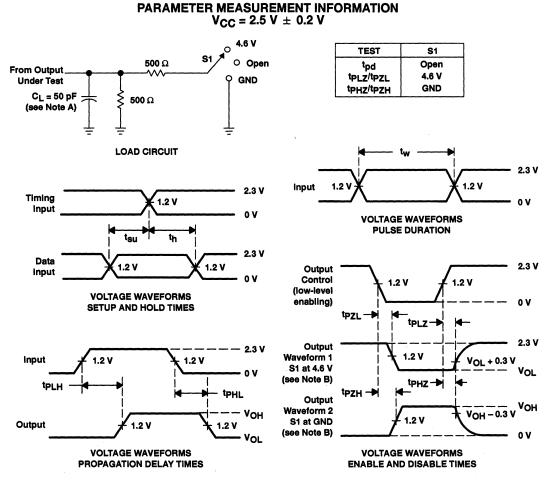
			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
V	High-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v
VIH		$V_{CC} = 2.7 V \text{ to } 3.6 V$	2		v
VIL	Low-level input voltage			0.7	v
۷IL	Low-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	Ň
VI	Input voltage	,	0	VCC	V
Vo	Output voltage	· · · · · · · · · · · · · · · · · · ·	0	VCC	V
		V <sub>CC</sub> = 2.3 V		-6	
ЮН	High-level output current	V <sub>CC</sub> = 2.7 V		<del>ا</del>	mA
		V <sub>CC</sub> = 3 V		-12	
		V <sub>CC</sub> = 2.3 V		6	
<b>I</b> OL	Low-level output current	V <sub>CC</sub> = 2.7 V		8	mA
		V <sub>CC</sub> = 3 V		12	
∆t/∆v	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



### SN74ALVCH162244 **16-BIT BUFFER/DRIVER** WITH 3-STATE OUTPUTS SCES065A - JANUARY 1996 - REVISED NOVEMBER 1996





NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , tr  $\leq$  2.5 ns, tr  $\leq$  2.5 ns,
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tPZL and tPZH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



### SN54ALVTH16244, SN74ALVTH16244 2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCES070A - JUNE 1996 - REVISED JULY 1996

	00200	, .				 
SN54AL	VT Н 16	244	wn	DACK	AGE	
0110776		6.TT .		<b>FAVIN</b>	~~~	

	bers of the Texas Instruments ebus™ Family	SN54ALVTH16244 WD PACKAGE SN74ALVTH16244 DGG, DGV, OR DL PACKAG			
	-Impedance State During Power Up Power Down		8] 2 <u>0</u> E		
• 5-V I	/O Compatible		70 1A1		
• High	-Drive Capability (-32 mA/64 mA)	1Y2 🛛 3 🛛 4	6 1A2		
•	cal V <sub>OLP</sub> (Output Ground Bounce)	GND 🚺 4 4	5 GND		
	$3 V \text{ at } V_{CC} = 3.3 V, T_A = 25^{\circ}C$	1Y3 🚺 5 4	4 🛛 1A3		
	o 3-State Eliminates Bus Current		3 <b>[</b> 1A4		
	ding When Voltage at the Output		2 V <sub>CC</sub>		
	eds V <sub>CC</sub>		1 2A1		
	Hold on Data Inputs Eliminates the		0 2A2		
	d for External Pullup/Pulldown				
	stors		8 2A3		
			37 2A4		
	er Off Disables Inputs/Outputs,		6 <b>3</b> 3 A 1		
	nitting Live Insertion		5 <b>3</b> A2		
	cage Options Include Plastic 300-mil		4 GND		
	nk Small-Outline (DL), Thin Shrink		3 <b>[</b> ] 3A3		
	II-Outline (DGG), Thin Very		2 3A4		
	II-Outline (DGV) Packages, and 380-mil		I V <sub>CC</sub>		
Fine	-Pitch Ceramic Flat (WD) Package		60 <b>2</b> 4A1		
		3	9 <b>]</b> 4A2		
descriptio	on		8 GND		
The '/	ALVTH16244 are 16-bit buffers/line drivers		27 <b>4</b> A3		
	ned for 2.5-V or 3.3-V Voc operation, but	4Y4 🛛 23 🛛 2	26 🛛 4A4		

the ALVTH16244 are 16-bit bullershine drivers designed for 2.5-V or 3.3-V  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When  $V_{CC}$  is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVTH16244 is available in TI's thin very small-outline package (DGV), which provides the same I/O pin count and functionality of standard Widebus packages in less than half the printed circuit board area.

The SN54ALVTH16244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALVTH16244 is characterized for operation from -40°C to 85°C.

	FUNCTION TABLE (each buffer)							
	INP	JTS	OUTPUT					
Ō	)E	Α	Ŷ					
	L	н	н					
	L	L	L					
	Н	X	Z					

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## SN54ALVTH16244, SN74ALVTH16244 2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCES070A - JUNE 1996 - REVISED JULY 1996

### recommended operating conditions, V<sub>CC</sub> = 2.5 V $\pm$ 0.2 V (see Note 3)

			SN54ALV	SN54ALVTH16244		SN74ALVTH16244		
			MIN	MAX	MIN	MAX	UNIT	
Vcc	Supply voltage			2.7	2.3	2.7	V	
VIH	High-level input voltage				1.7		V	
VIL	Low-level input voltage			0.7		0.7	V	
VI	Input voltage			5.5	0	5.5	V	
ЮН	High-level output current			-6		8	mA	
1	Low-level output current		6		8			
IOL	Low-level output current; current duty cycle $\leq$ 50%; f $\geq$ 1 KHz			18		24	mA	
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		10	ns/V	
TA	Operating free-air temperature			125	-40	85	°C	

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

### recommended operating conditions, V<sub>CC</sub> = 3.3 V $\pm$ 0.3 V (see Note 3)

			SN54ALV	SN54ALVTH16244		SN74ALVTH16244		
			MIN	MAX	MIN	MAX		
Vcc	V <sub>CC</sub> Supply voltage			3.6	3	3.6	V	
VIH	High-level input voltage				2		V	
VIL	Low-level input voltage			0.8		0.8	v	
VI	Input voltage			5.5	0	5.5	V	
ЮН	High-level output current			-24		-32	mA	
1	Low-level output current			24		32		
IOL	Low-level output current; current duty cycle $\leq$ 50%; f $\geq$ 1 KHz			48		64	mA	
∆t/∆v	Input transition rise or fall rate	Outputs enabled		10		10	ns/V	
TA	Operating free-air temperature		-55	125	-40	85	°C	

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

### SN54ALVTH16244, SN74ALVTH16244 2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS S

CES070A	– JUNE	1996 -	REVISED	JULY 199

PARAMETER	TEST CONDITIONS			SN54ALVTH16244			SN74A			
				MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	V <sub>CC</sub> = 3 V,	lj =18 mA		1		-1.2			-1.2	V
	V <sub>CC</sub> = 3 V to 3.6 V,	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2			
VOH	N 0 N	$I_{OH} = -24 \text{ mA}$ $I_{OH} = -32 \text{ mA}$		2						v
	V <sub>CC</sub> = 3 V						2			
	V <sub>CC</sub> = 3 V to 3.6 V,	l <sub>OL</sub> = 100 μA		1		0.2			0.2	
		I <sub>OL</sub> = 16 mA		1					0.4	
Max		1 <sub>OL</sub> = 24 mA				0.5				
VOL	V <sub>CC</sub> = 3 V	l <sub>OL</sub> = 32 mA	$l_{OL} = 32 \text{ mA}$						0.5	v
		I <sub>OL</sub> = 48 mA I <sub>OL</sub> = 64 mA		1	- 1	0.55				
								0.55		
	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V	$c_{\rm C} = 3.6$ V, $V_{\rm I} = V_{\rm CC}$ or GND		Ι		±1			±1	
	$V_{CC} = 0 \text{ or } 3.6 \text{ V},  V_{I} = 5.5 \text{ V}$		Control inputs			10			10	
կ	V <sub>CC</sub> = 3.6 V	V <sub>I</sub> = 5.5 V	Data inputs	1		20			20	μA
		VI = VCC				10			10	
		V <sub>1</sub> = 0				-5			-5	
loff	V <sub>CC</sub> = 0,	$V_{\rm I}$ or $V_{\rm O} = 0$ to	4.5 V	1		±100			±100	μA
	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0.8 V	Data inputs	75			75			μΑ
li (hold)		V <sub>1</sub> = 2 V		-75			-75			
	V <sub>CC</sub> = 3.6 V <sup>‡</sup> ,	V <sub>1</sub> = 0 to 3.6 V	]			±500		±500		
<sup>I</sup> EX <sup>§</sup>	V <sub>CC</sub> = 3 V,	V <sub>O</sub> = 5.5 V				125			125	μA
IOZ(PU/PD) <sup>¶</sup>	$V_{CC} \le 1.2 \text{ V}, \qquad V_{O} = 0.5 \text{ V to } V_{CC}, \\ V_{I} = \text{GND or } V_{CC}, \qquad \overline{\text{OE}} = \text{don't care}$					±100			±100	μA
lozh	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 3	V, VI = 0.8 V or 2	V			5			5	μA
<sup>I</sup> OZL	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0.5 V, V <sub>I</sub> = 0.8 V or 2 V				-5			-5	μA	
lcc			Outputs high		0.07	0.09		0.07	0.09	
	$V_{CC} = 3.6 V$ , $I_O = 0$ , $V_I = V_{CC}$ or GND		Outputs low		3.2	5		3.2	5	mA
			Outputs disabled		0.07	0.09		0.07	0.09	
∆I <sub>CC</sub> #	$V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ –0.6 V, Other inputs at $V_{CC}$ or GND					0.2			0.2	mA
Ci	V <sub>CC</sub> = 3.3 V, V <sub>1</sub> = 3.3 V or 0				3			3		pF
Co	V <sub>CC</sub> = 3.3 V,	$V_{0} = 3.3 V \text{ or } 0$	)		9		[	9		pF

# electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 2)

<sup>†</sup> All typical values are at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}$ C.

<sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

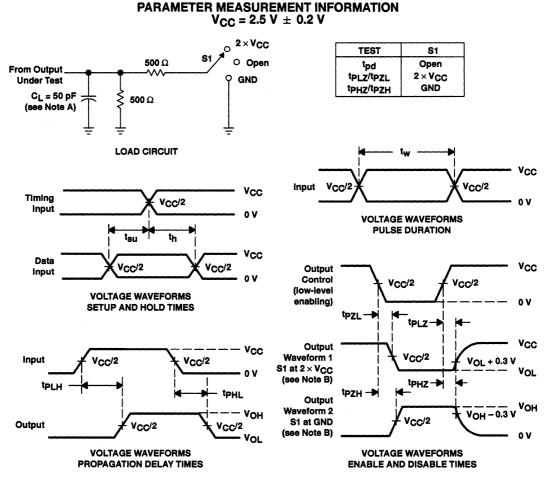
Current into an output in the high state when VO > VCC

<sup>¶</sup> High-impedance state during power up/high-impedance state during power down

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.



### SN54ALVTH: 5244, SN74ALVTH16244 2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCESO70A - JUNE 1996 - REVISED JULY 1996



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as  $t_{en}$ .
- G. tpi H and tpH are the same as tod.

### Figure 1. Load Circuit and Voltage Waveforms

# **PRODUCT PREVIEW**



### SN54ALVTH162244, SN74ALVTH162244 2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCES074A - JUNE 1996 - REVISED JULY 1996

● Members of the Texas Instruments Widebus™ Family	SN54ALVTH162244 WD PACKAGE SN74ALVTH162244 DGG, DGV, OR DL PACKAGE (TOP VIEW)
<ul> <li>Output Ports Have Equivalent 30-Ω Series Resistors, So No External Resistors Are Required</li> </ul>	
<ul> <li>High-Impedance State During Power Up and Power Down</li> </ul>	1Y2 [ 3 46 ] 1A2 GND [ 4 45 ] GND
• 5-V I/O Compatible	1Y3 5 44 1A3
<ul> <li>High-Drive Capability (-12 mA/12 mA)</li> </ul>	1Y4 🚺 6 43 🗍 1A4
<ul> <li>Typical V<sub>OLP</sub> (Output Ground Bounce)</li> </ul>	V <sub>CC</sub> []7 42 [] V <sub>CC</sub>
< 0.8 V at V <sub>CC</sub> = 3.3 V, T <sub>A</sub> = 25°C	2Y1 🛛 8 41 🖸 2A1
<ul> <li>Auto 3-State Eliminates Bus Current</li> </ul>	2Y2 9 40 2A2
Loading When Voltage at the Output	
Exceeds V <sub>CC</sub>	2Y3 <b>[</b> 11 38 <b>[</b> 2A3
	2Y4 12 37 2A4
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Bullup (Bulldown)</li> </ul>	3Y1 13 36 3A1
Need for External Pullup/Pulldown Resistors	3Y2 14 35 3A2
	GND [] 15 34 [] GND
<ul> <li>Power Off Disables Inputs/Outputs,</li> </ul>	3Y3 🛛 16 🛛 33 🖸 3A3
Permitting Live Insertion	3Y4 🛛 17 32 🖸 3A4
<ul> <li>Package Options Include Plastic 300-mil</li> </ul>	
Shrink Small-Outline (DL), Thin Shrink	4Y1 <b>[]</b> 19 30 <b>[]</b> 4A1
Small-Outline (DGG), Thin Very	4Y2 <b>[</b> ]20 29 <b>[</b> ] 4A2
Small-Outline (DGV) Packages, and 380-mil	GND 21 28 GND
Fine-Pitch Ceramic Flat (WD) Package	4Y3 🛛 22 27 🖸 4A3
· · · · ·	4Y4 <b>[</b> ]23 26 <b>[</b> ] 4A4
description	40E <b>[</b> 24 25 <b>]</b> 30E

#### description

The 'ALVTH162244 are 16-bit buffers/line drivers designed for low-voltage 2.5-V or 3.3-V V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable (OE) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V<sub>CC</sub> is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, OE should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

All outputs are designed to sink up to 12 mA and include 30-Ω resistors to reduce overshoot and undershoot.

The SN74ALVTH162244 is available in TI's thin very small-outline package (DGV), which provides the same I/O pin count and functionality of standard Widebus packages in less than half the printed circuit board area.

The SN54ALVTH162244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALVTH162244 is characterized for operation from -40°C to 85°C.

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PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notice.



### SN54ALVTH162244, SN74ALVTH162244 2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCES074A - JUNE 1996 - REVISED JULY 1996

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1)0.5	
Output current in the low state, I <sub>O</sub>	. 30 mA
Output current in the high state, $I_{O}$	. –30 mA
Input clamp current, I <sub>IK</sub> (VI < 0)	
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0)	
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2): DGG package	
DGV package	
Storage temperature range, T <sub>stg</sub> 65°C	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

 The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book.

### recommended operating conditions, $V_{CC}$ = 2.5 V ± 0.2 V (see Note 3)

			SN54ALVTH162244 SN74ALVTH162244 MIN MAX MIN MAX		SN74ALVT		
					MAX		
Vcc	Supply voltage		2.3	2.7	2.3	2.7	V
VIH	High-level input voltage		1.7		1.7		v
VIL	Low-level input voltage			0.7		0.7	V
VI	Input voltage		0	5.5	0	5.5	V
ЮН	High-level output current						mA
IOL	Low-level output current						mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled	1	. 10		10	ns/V
TA	Operating free-air temperature		55	125	-40	85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

### recommended operating conditions, V<sub>CC</sub> = 3.3 V $\pm$ 0.3 V (see Note 3)

	· · · · · ·		SN54ALVT	H162244	SN74ALVT		
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		3	3.6	3	3.6	V
٧ <sub>IH</sub>	High-level input voltage		2		2		V
٧ <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
٧I	Input voltage		0	5.5	0	5.5	V
ЮН	High-level output current			8		-12	mA
lol	Low-level output current			8		12	mA
∆t/∆v	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Τ <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.



### SN54ALVTH162244, SN74ALVTH162244 2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCES074A - JUNE 1996 - REVISED JULY 1996

		SN54A	LVTH162	244	SN74A	LVTH162	244	UNIT			
PARAMETER	TE	MIN	TYPT	MAX	MIN	TYPT	MAX				
VIK	V <sub>CC</sub> = 3 V,	lj =18 mA	lj =18 mA			-1.2			-1.2	v	
	V <sub>CC</sub> = 3 V to 3.6 V	/, I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2				
Voн	N 0.V	I <sub>OH</sub> = - 8 mA								v	
	V <sub>CC</sub> = 3 V	1 <sub>OH</sub> = - 12 mA					T				
	V <sub>CC</sub> = 3 V to 3.6 V	, I <sub>OL</sub> = 100 μA				0.2			0.2		
VOL	No. 2V	I <sub>OL</sub> = 8 mA								v	
	V <sub>CC</sub> = 3 V	I <sub>OL</sub> = 12 mA	I <sub>OL</sub> = 12 mA								
	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V	V <sub>CC</sub> or GND	Control inputs			±1			±1		
	V <sub>CC</sub> = 0 or 3.6 V	V <sub>I</sub> = 5.5 V	Control inputs			10			10		
կ		Vj = 5.5 V				20			20	μA	
	V <sub>CC</sub> = 3.6 V	$V_I = V_{CC}$	Data inputs			10			10		
		VI = 0				-5			-5		
loff	V <sub>CC</sub> = 0,	$V_1 \text{ or } V_0 = 0 \text{ to}$	4.5 V			±100			±100	μA	
	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0.8 V		75			75				
l(hold)	VCC = 3 V	V <sub>1</sub> = 2 V	Data inputs	-75			-75			μA	
	$V_{CC} = 3.6 V^{\ddagger},$	V <sub>I</sub> = 0 to 3.6 V			±50				±500		
I <sub>EX</sub> §	V <sub>CC</sub> = 3 V,	V <sub>O</sub> = 5.5 V				125			125	μA	
<sup>I</sup> OZ(PU/PD) <sup>¶</sup>	$V_{CC} \le 1.2 \text{ V},$ V <sub>I</sub> = GND or V <sub>CC</sub> ,	$V_O = 0.5 V$ to V $\overline{OE} = don't care$				±100			±100	μA	
			Outputs high		0.07	0.09		0.07	0.09		
Icc		IO = 0,	Outputs low		3.2	5		3.2	5	mA	
	$V_{I} = V_{CC} \text{ or } GND$		Outputs disabled		0.07	0.09		0.07	0.09		
∆I <sub>CC</sub> #	$V_{CC} = 3 V \text{ to } 3.6 V$ Other inputs at $V_{C}$		/ <sub>CC</sub> – 0.6 V,			0.2			0.2	mA	
Ci	V <sub>CC</sub> = 3.3 V,	V <sub>1</sub> = 3.3 V or 0			3			3		pF	
Co	V <sub>CC</sub> = 3.3 V,	V <sub>O</sub> = 3.3 V or 0	)		9			9		pF	

#### electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

<sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C. <sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

Current into an output in the high state when VO > VCC

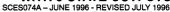
<sup>¶</sup> High-impedance state during power up/high-impedance state during power down

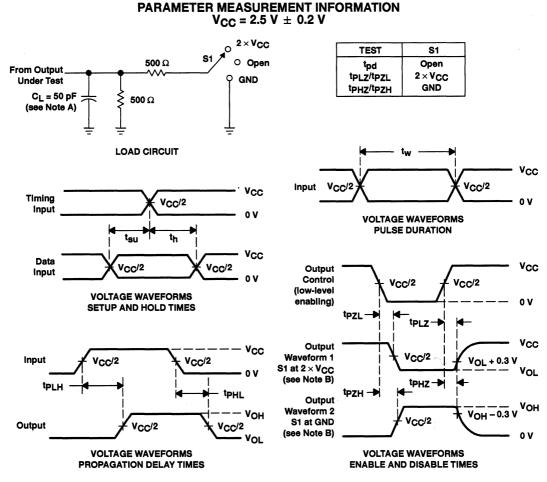
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.





### SN54ALVTH162244, SN74ALVTH162244 2.5-V/3.3-V 16-BIT BUFFERS/DRIV WITH 3-STATE OUTPUTS

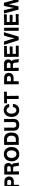




NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpH7 are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms





### SN54LVTH16244A, SN74LVTH16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCB5142G - MAY 1992 - REVISED NOVEMBER 1996

<ul> <li>State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power</li> </ul>	SN54LVTH16244A WD PACKAGE SN74LVTH16244A DGG OR DL PACKAGE (TOP VIEW)
Dissipation <ul> <li>Members of the Texas Instruments</li> <li>Widebus™ Family</li> </ul>	10E [1 48] 20E 1Y1 [2 47] 1A1
<ul> <li>High-Impedance State During Power Up and Power Down</li> </ul>	1Y2 [] 3 46 [] 1A2 GND [] 4 45 [] GND 1Y3 [] 5 44 [] 1A3
<ul> <li>Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)</li> </ul>	1Y4 []6 43 ]] 1A4 V <sub>CC</sub> []7 42 ]] V <sub>CC</sub>
<ul> <li>Support Unregulated Battery Operation Down to 2.7 V</li> </ul>	2Y1 8 41 2A1 2Y2 9 40 2A2
<ul> <li>Typical V<sub>OLP</sub> (Output Ground Bounce)</li> <li>&lt; 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C</li> </ul>	GND [] 10 39 [] GND 2Y3 [] 11 38 [] 2A3 2Y4 [] 12 37 [] 2A4
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)</li> </ul>	3Y1 0 13 360 3A1 3Y2 0 14 350 3A2
<ul> <li>Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17</li> </ul>	GND [] 15 34 [] GND 3Y3 [] 16 33 [] 3A3 3Y4 [] 17 32 [] 3A4
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	$V_{CC}$ [ 18 31 ] $V_{CC}$ 4Y1 [ 19 30 ] 4A1 4Y2 [ 20 29 ] 4A2
<ul> <li>Power Off Disables Inputs/Outputs, Permitting Live Insertion</li> </ul>	GND [21 28] GND 4Y3 [22 27] 4A3
<ul> <li>Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages, and 380-mil</li> </ul>	4Y4 []23 26 [] 4A4 4OE []24 25 ] 3OE

#### description

The 'LVTH16244A are 16-bit buffers and line drivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When  $V_{CC}$  is between 0 and 1.5-V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5-V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVTH16244A is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

Widebus is a trademark of Texas Instruments Incorporated.

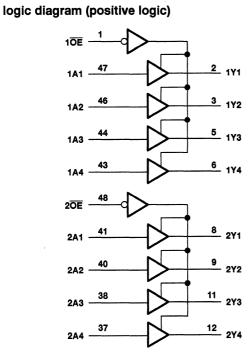
Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

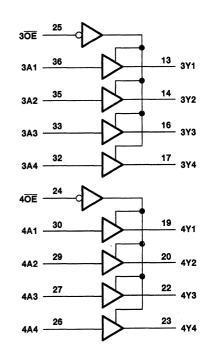
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### SN54LVTH16244A, SN74LVTH16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS142G - MAY 1992 - REVISED NOVEMBER 1996





### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 4.6 V
Input voltage range, VI (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1) .	–0.5 V to 7 V
Current into any output in the low state, IO: SN54LVTH16244A	96 mA
SN74LVTH16244A	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVTH16244A	48 mA
SN74LVTH16244A	64 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range, T <sub>stg</sub>	65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ . 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book.



### SN54LVTH16244A, SN74LVTH16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCBS142G - MAY 1992 - REVISED NOVEMBER 1996

DADAMETED	TE	SN54L	VTH162	44A	SN74L	LINUT					
PARAMETER		ST CONDITIONS		MIN	TYPT	MAX	MIN	түрт	MAX	UNIT	
VIK	V <sub>CC</sub> = 2.7 V,	lj = -18 mA				-1.2			-1.2	v	
	V <sub>CC</sub> = 2.7 V to 3.6 V,	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2				
Maria	V <sub>CC</sub> = 2.7 V,	IOH = -8 mA		2.4			2.4			v	
VOH		I <sub>OH</sub> = -24 mA		2						v	
	$V_{CC} = 3 V$	I <sub>OH</sub> = -32 mA					2				
	Vec 27V	l <sub>OL</sub> = 100 μA				0.2			0.2		
	V <sub>CC</sub> = 2.7 V	I <sub>OL</sub> = 24 mA				0.5			0.5		
Ma.		I <sub>OL</sub> = 16 mA				0.4			0.4		
V <sub>OL</sub>		IOL = 32 mA				0.5			0.5 V		
	$V_{CC} = 3 V$	I <sub>OL</sub> = 48 mA			0.55						
		IOL = 64 mA			Å	4			0.55		
$V_{CC} = 0 \text{ or } 3.6$	V <sub>CC</sub> = 0 or 3.6 V,	V <sub>I</sub> = 5.5 V				10			10		
	V <sub>CC</sub> = 3.6 V	VI = V <sub>CC</sub> or GND	Control inputs		A A A A A A A A A A A A A A A A A A A	±1			±1	μA	
		VI = VCC	Data		Ş –	1			1		
		V <sub>I</sub> = 0	inputs	Š		-5			-5		
loff	V <sub>CC</sub> = 0,	$V_{I} \text{ or } V_{O} = 0 \text{ to } 4.5 \text{ V}$		L. S.		±100			±100	μA	
I	N 0.1	V <sub>I</sub> = 0.8 V	Data	75			75				
l(hold)	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 2 V	inputs	-75			-75			μA	
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V,				5			5	μA	
lozl	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V,				-5			-5	μA	
lozpu‡	V <sub>CC</sub> = 0 to 1.5 V,	$V_{O} = 0.5 V \text{ to } 3 V,$	<u>OE</u> = 0			±100			±100	μA	
IOZPD <sup>‡</sup>	V <sub>CC</sub> = 1.5 V to 0,	V <sub>O</sub> = 0.5 V to 3 V,	$\overline{OE} = 0$			±100			±100	μA	
	V <sub>CC</sub> = 3.6 V,	Outputs high				0.19			0.19		
ICC	I <sub>O</sub> = 0,	Outputs low				5			5	mA	
	$V_{I} = V_{CC} \text{ or } GND$			0.19			0.19				
∆I <sub>CC</sub> §	$V_{CC} = 3 V \text{ to } 3.6 V, O$ Other inputs at $V_{CC}$ o	ne input at V <sub>CC</sub> – 0.6 V or GND	Ι,			0.2			0.2	mA	
Ci	V <sub>I</sub> = 3 V or 0				4			4		pF	
Co	V <sub>O</sub> = 3 V or 0				9			9		pF	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

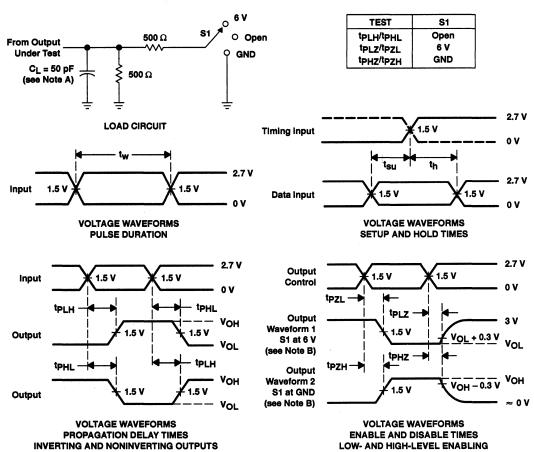
<sup>‡</sup> This parameter is warranted by characterization but not production tested.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



### SN54LVTH16244A, SN74LVTH16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS142G - MAY 1992 - REVISED NOVEMBER 1996



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns,
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



### SN54LVTH162244, SN74LVTH162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCB5258E - JUNE 1993 - REVISED NOVEMBER 1996

SN54LVTH162244... WD PACKAGE SN74LVTH162244... DGG OR DL PACKAGE

 Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Inputs/Outputs, Permitting Live Insertion
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

### description

The 'LVTH162244 are 16-bit buffers and line drivers designed for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

The outputs, which are designed to source or sink up to 12 mA, include  $22-\Omega$  series resistors to reduce overshoot and undershoot.

Widebus is a trademark of Texas Instruments Incorporated.

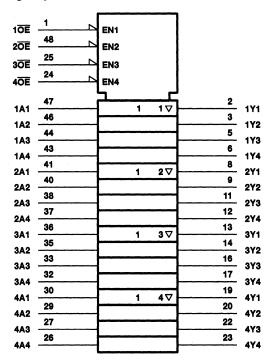
UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of reass instruments standard warranty. Production processing does not necessarily include testing of all parameters.



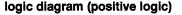
	(TOP VI	EW)	
			L
10E	3		20E
1Y1 [			1A1
1Y2 [	3		] 1A2
GND [	4		GND
1Y3 [	5	44	] 1A3
1Y4 [	6		<b>]</b> 1A4
V <sub>CC</sub> [	7	42	]v <sub>cc</sub>
2Y1 [		41	2A1
2Y2 [	9		2A2
GND [	10	39	GND
2Y3 [	11	38	2A3
2Y4 [	12	37	2A4
3Y1 [	13	36	3A1
3Y2 [	14	35	3A2
GND [	15	34	] GND
3Y3 [	16	33	3A3
3Y4 [	17	32	3A4
V <sub>CC</sub> [	18	31	Vcc
4Y1 [	19		4A1
4Y2 [		29	4A2
GND [		28	GND
4Y3		27	4A3
4Y4 [			<b>4</b> A4
40E	24		3 OE

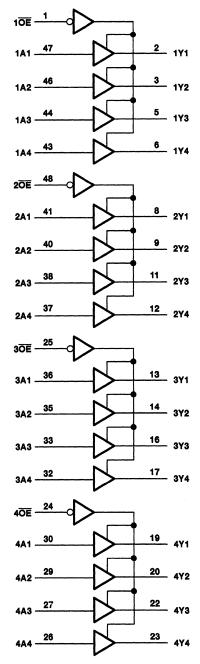
### SN54LVTH162244, SN74LVTH162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCB3258E - JUNE 1993 - REVISED NOVEMBER 1996





<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.







### SN54LVTH162244, SN74LVTH162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCBS258E - JUNE 1993 - REVISED NOVEMBER 1996

electrical otherwise		over	recommended	operating	free-air	temperature	range	(unless
otherwise	noteuj							

	TEST CONDITIONS				LVTH16	2244	SN74	LINUT			
PARAMETER				MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT	
VIK	V <sub>CC</sub> = 2.7 V,	lj = –18 mA				-1.2			-1.2	V	
VOH	V <sub>CC</sub> = 3 V,	<sup>I</sup> OH = -12 mA		2			2			v	
VOL	V <sub>CC</sub> = 3 V,	l <sub>OL</sub> = 12 mA				0.8			0.8	V	
	V <sub>CC</sub> = 0 or 3.6 V					10			10		
		V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins			±1			±1		
ų	V <sub>CC</sub> = 3.6 V	$V_{I} = V_{CC}$	Data pins			1			1	μA	
		V <sub>1</sub> = 0	Data pins			🖇 -5			5	1	
loff	$V_{CC} = 0,$	$V_{\rm I}$ or $V_{\rm O}$ = 0 to 4.5 V	V		di la	, ,			±100	μA	
	V 2V	VI = 0.8 V	A impute	75	Å.		75			μA	
l(hold)	V <sub>CC</sub> = 3 V	V  = 2 V	A inputs	-75	S.		-75				
IOZH	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V		2	ř	5			5	μA	
IOZL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V		Q.		-5			5	μA	
<sup>I</sup> OZPU <sup>‡</sup>	$V_{CC} = 0$ to 1.5 V,	$V_{O} = 0.5 \text{ V to 3 V}, \overline{OE}$	= X			±100			±100	μA	
<sup>I</sup> OZPD <sup>‡</sup>	V <sub>CC</sub> = 1.5 V to 0,	$V_{O} = 0.5 \text{ V to 3 V}, \overline{OE}$	= X			±100			±100	μA	
			Outputs high			0.19			0.19		
ICC	$V_{CC} = 3.6 V,$ $V_{I} = V_{CC} \text{ or GND}$	l <sub>O</sub> = 0,	Outputs low			5			5	mA	
			Outputs disabled			0.19			0.19		
∆I <sub>CC</sub> §		$_{CC}$ = 3 V to 3.6 V, One input at V <sub>CC</sub> – 0.6 V, ther inputs at V <sub>CC</sub> or GND				0.2			0.2	mA	
Ci	V <sub>I</sub> = 3 V or 0				4			4		pF	
Co	V <sub>O</sub> = 3 V or 0				9			9		pF	

<sup>†</sup> All typical values are at  $V_{CC} = 3.3$  V,  $T_A = 25$ °C.

<sup>‡</sup> This parameter is characterized but not tested.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

## switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

			S	SN54LVTH162244			SN74LVTH162244									
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		UNIT				
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX					
<sup>t</sup> PLH	٨	v	1.3	4.5	L <sup>N</sup>	5.1	1.4	3.4	4		4.8	ns				
<sup>t</sup> PHL	Α	1	1.1	3.9	. Ch	4.5	1.2	2.9	3.6		4.1	lis				
<sup>t</sup> PZH	ŌĒ	v	1.1	5.3	\$ <sup>7</sup> ~	6.7	1.2	3.9	5.1		6.5	ns				
<sup>t</sup> PZL	OE	1	1.3	A.S		6.1	1.4	3.8	4.5		5.8	115				
<sup>t</sup> PHZ	ŌĒ	v	2.1	_O <sup>™</sup> 5.3		5.6	2.2	4.4	5		5.4	ns				
<sup>t</sup> PLZ	UL UL	I	T	T	T	T	1.9	<b>5.5</b>		5.8	2	4.2	5		5.4	115

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .



#### SN74ALVCH16373 **16-BIT TRANSPARENT D-TYPE LATCH** WITH 3-STATE OUTPUTS s

CES020A	- JULY 1995	- REVISED	NOVEMB

<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	DGG OR DL PACKAGE (TOP VIEW)		
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	1 OE		48 1LE
ESD Protection Exceeds 2000 V Per	1Q1 1Q2		47 1D1 46 1D2
MIL-STD-833, Method 3015; Exceeds 200 V Using Machine Model	GND 🛛	4	45 GND 44 103
(C = 200  pF, R = 0)	1Q3   1Q4		43 1D4
<ul> <li>Latch-Up Performance Exceeds 250 mA</li> <li>Per JEDEC Standard JESD-17</li> </ul>	V <sub>CC</sub> 1Q5		42 V <sub>CC</sub> 41 105
Bus Hold on Data Inputs Eliminates the	1Q6 🛛	9	40 <b>0</b> 1D6
Need for External Pullup/Pulldown Resistors	GND 1Q7		39 GND 38 1D7
<ul> <li>Package Options Include Plastic 300-mil</li> <li>Shrink Small Outline (DL) and Thin Shrink</li> </ul>	1Q8 🛛	12	37 <b>0</b> 1D8
Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages	2Q1 2Q2		36 2D1 35 2D2
description	GND 2Q3		34 GND 33 2D3
This 16-bit transparent D-type latch is designed	2Q4 [	17	32 <b>]</b> 2D4
for 2.3-V to 3.6-V $V_{CC}$ operation.	V <sub>CC</sub> 2Q5	18 19	31 V <sub>CC</sub> 30 2D5
The SN74ALVCH16373 is particularly suitable	2Q6 🛛	20	29 2D6
for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.	GND 2Q7		28 GND 27 2D7

This device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

2Q8 23

20E

26 🛛 2D8

2LE

25

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16373 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16373 is characterized for operation from -40°C to 85°C.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas instruments standard warranty. Production processing does not necessarily include testing of all parameters.



### SN74ALVCH16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS SCES020A – JULY 1995 – REVISED NOVEMBER 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

	0514-4614
Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	. –0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)0.5 V	/ to V <sub>CC</sub> + 0.5 V
Input clamp current, IIK (VI < 0)	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range, T <sub>stg</sub>	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.*

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v
VIH	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2		v
<b>M</b>		$V_{CC} = 2.3 V \text{ to } 2.7 V$		0.7	v
VIL	Low-level input voltage		0.8	v	
٧I	Input voltage		0	VCC	v
Vo	Output voltage		0	VCC	v
		V <sub>CC</sub> = 2.3 V		-12	
ЮН	High-level output current	V <sub>CC</sub> = 2.7 V		-12	mA
		V <sub>CC</sub> = 3 V		-24	
		V <sub>CC</sub> = 2.3 V		12	
IOL	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
		V <sub>CC</sub> = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



# timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

		V <sub>CC</sub> = ± 0.	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.5 V         V <sub>CC</sub> = 2.7 V         V <sub>CC</sub> = 3.3 V           ± 0.2 V         V <sub>CC</sub> = 2.7 V         ± 0.3 V		3.3 V 3 V	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
tw	Pulse duration, LE high or low	3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before LE↓	1		1		1.1		ns
th	Hold time, data after LE↓	1.5		1.7		1.4		ns

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

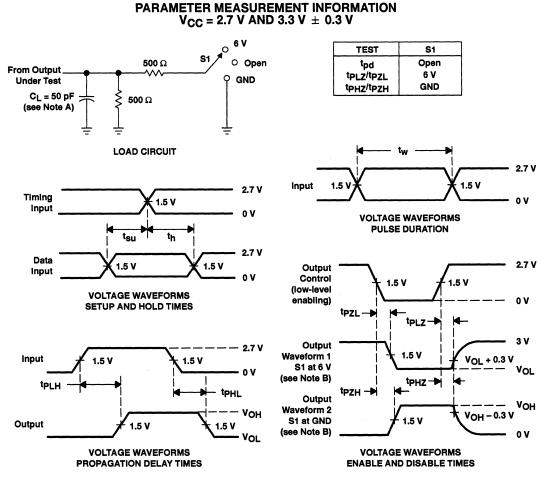
PARAMETER	FROM TO		V <sub>CC</sub> = ± 0.3	2.5 V 2 V	V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = ± 0.3	3.3 V 3 V	UNIT
	(111601)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	
	D	Q	1	5.1		4.3	1.1	3.6	ns
<sup>t</sup> pd	LE	Q	1	5.5		4.6	1	3.9	115
ten	ŌĒ	Q	1	6.5		5.7	1	4.7	'ns
<sup>t</sup> dis	ŌĒ	Q	1.9	5.3		4.5	1.4	4.1	ns

### operating characteristics, T<sub>A</sub> = 25°C

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT
			TYP	TYP		
	Rever dissignation experitonee	Outputs enabled		19	22	рF
Cpd	Power dissipation capacitance	Outputs disabled	C <sub>L</sub> = 50 pF, f = 10 MHz	4	5	ρr



### SN74ALVCH16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS SCES020A - JULY 1995 - REVISED NOVEMBER 1996



- NOTES: A. CL includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>r</sub>  $\leq$  2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLZ and tpHZ are the same as tdis.
  - F. tp<sub>ZL</sub> and tp<sub>ZH</sub> are the same as  $t_{en}$ .
  - G. tpLH and tpHL are the same as tpd.
  - . PLH and PHL are the same as the

### Figure 2. Load Circuit and Voltage Waveforms



### SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS SCBS144F - MAY 1992 - REVISED NOVEMBER 1996

1 C	tate-of-the-Art Advanced BiCMOS echnology (ABT) Design for 3.3-V Operation and Low-Static Power	SN54LVTH16373 WD PACKAGE SN74LVTH16373 DGG OR DL PACKA (TOP VIEW)				
• •	Dissipation Members of the Texas Instruments <i>Widebus</i> ™ Family	1Q1 <b>[</b> 2 47	1LE 1D1			
	Support Mixed-Mode Signal Operation (5-V nput and Output Voltages With 3.3-V V <sub>CC</sub> )		1D2 GND 1D3			
	Support Unregulated Battery Operation Down to 2.7 V	1Q4 <b>[</b> ]6 4:	1D4 V <sub>CC</sub>			
	ligh-Impedance State During Power Up Ind Power Down	1Q5 <b>[]</b> 8 4 <sup>.</sup>	1D5 1D6			
	<sup>•</sup> ypical V <sub>OLP</sub> (Output Ground Bounce) : 0.8 V at V <sub>CC</sub> = 3.3 V, T <sub>A</sub> = 25°C	1Q7 🚺 11 38	GND 1D7			
• E N	SD Protection Exceeds 2000 V Per ML-STD-883, Method 3015; Exceeds 200 V Jsing Machine Model C = 200 pF, R = 0)	2Q1 [ 13 30 2Q2 [ 14 33 GND [ 15 34	1D8 2D1 2D2 GND			
	atch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17	2Q4 🛽 17 3:	2 2D3 2 2D4			
1	Bus Hold on Data Inputs Eliminates the leed for External Pullup/Pulldown Resistors	2Q5 [] 19 30 2Q6 [] 20 29	V <sub>CC</sub>   2D5   2D6   GND			
	Power Off Disables Inputs/Outputs, Permitting Live Insertion	2Q7 <b>2</b> 22 2	2D7 2D8			
• [	Distributed V <sub>CC</sub> and GND Pin Configuration		2LE			

- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes
   PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

### description

The 'LVTH16373 are 16-bit transparent D-type latches with 3-state outputs designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

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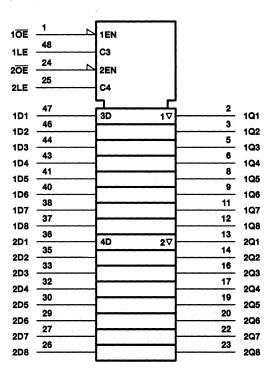
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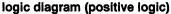
3–113

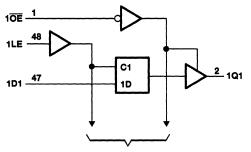
### SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS SCB5144F - MAY 1992 - REVISED NOVEMBER 1996

SCBS144F - MAY 1992 - REVISED NOVEMBER

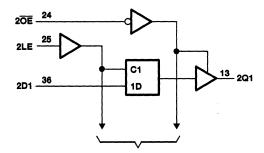








**To Seven Other Channels** 



**To Seven Other Channels** 

<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



### SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS SCBS144F - MAY 1992 - REVISED NOVEMBER 1996

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN5	4LVTH1	3373	SN74	LVTH16	6373	UNIT
	ANAMEIEN	TEST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK		V <sub>CC</sub> = 2.7 V,	lj =18 mA			-1.2			-1.2	٧
		V <sub>CC</sub> = 2.7 V to 3.6 V	IOH =100 μA	Vcc-0	).2		V <sub>CC</sub> -0	.2		
V		V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> =8 mA	2.4			2.4			v
VOH		V <sub>CC</sub> = 3 V	I <sub>ОН</sub> = -24 mA	2						v
		VCC = 3 V	IOH = -32 mA				2			
		V <sub>CC</sub> = 2.7 V	l <sub>OL</sub> = 100 μA			0.2			0.2	
		VCC = 2.7 V	I <sub>OL</sub> = 24 mA			0.5			0.5	
VOL			l <sub>OL</sub> = 16 mA			0.4			0.4	v
VOL		V <sub>CC</sub> = 3 V	l <sub>OL</sub> = 32 mA			0.5			0.5	v
		VCC = 3 V	l <sub>OL</sub> = 48 mA			0.55				
			I <sub>OL</sub> = 64 mA			á.			0.55	
		V <sub>CC</sub> = 0 or 3.6 V	VI = 5.5 V			S 10			10	
lj -	Control inputs	V <sub>CC</sub> = 3.6 V,	VI = V <sub>CC</sub> or GND		<u> </u>	/ ±1			±1	μA
4	Data inputs	V <sub>CC</sub> = 3.6 V	VI = V <sub>CC</sub>		A	1			1	μΛ
	Data inputs	VCC = 3.0 V	V <sub>I</sub> = 0		S.	-5			5	
loff		$V_{\rm CC} = 0,$	$V_{I}$ or $V_{O}$ = 0 to 4.5 V		õ	±100			±100	μA
h/h a hab	Data inputs	V <sub>CC</sub> = 3 V	VI = 0.8 V	75.	•		75			μA
li(hold)	Data inputs	VCC = 0 V	V <sub>I</sub> = 2 V	-75			-75			μ
lozн		V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V			5			5	μA
IOZL		V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V			-5			5	μA
IOZPU <sup>‡</sup>		$V_{CC} = 0$ to 1.5 V, $V_{C}$	$= 0.5 \text{ V to 3 V}, \overline{\text{OE}} = X$			±100			±100	μA
IOZPD <sup>‡</sup>		$V_{CC} = 1.5 V \text{ to } 0, V_{CC}$	$= 0.5 \text{ V to 3 V}, \overline{\text{OE}} = X$			±100			±100	μA
	Outputs high	N 00V	1- 0			0.19			0.19	
ICC	Outputs low	$V_{CC} = 3.6 V,$ $V_1 = V_{CC} \text{ or GND}$	l <sub>O</sub> = 0,			5			5	mA
	Outputs disabled					0.19			0.19	
∆I <sub>CC</sub> §		$V_{CC} = 3 V \text{ to } 3.6 V, C$ Other inputs at $V_{CC}$ of	one input at V <sub>CC</sub> – 0.6 V, r GND			0.2			0.2	mA
Ci		V <sub>I</sub> = 3 V or 0			3			3		pF
Co		$V_{O} = 3 V \text{ or } 0$			9			9		pF

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>‡</sup> This parameter is characterized but not tested.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

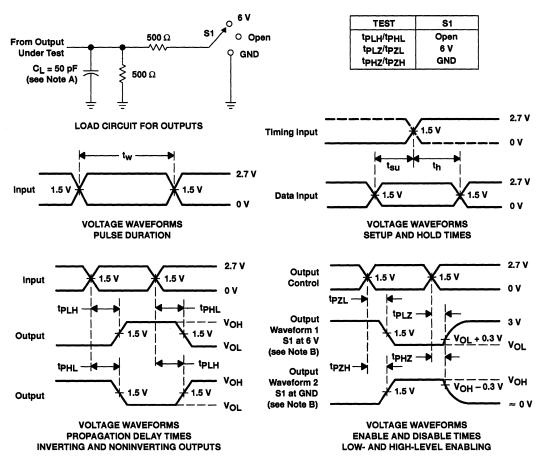
			SN54LVTH16373			SN74LVTH16373				
		V <sub>CC</sub> = ± 0.		V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = ± 0.	: 3.3 V 3 V	V <sub>CC</sub> =	2.7 V	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tw	Pulse duration, LE high	3	"I for	<u>с</u> з		3		3		ns
t <sub>su</sub>	Setup time, data before LE↓	1 «	,ROXI	0.6		1		0.6		ns
th	Hold time, data after LE↓	1	bur	1.1		1	x	1.1		ns

AODUCT PREVIEW information concerns products in the formative or usign phase of development. Characteristic data and other sectifications are design goals. Texas instruments reserves the right to section of informative these products without notice.



### SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS144F - MAY 1992 - REVISED NOVEMBER 1996



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns,
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



SN74ALVCH16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES021A - JULY 1995 - REVISED NOVEMBER 1996

25 2CLK

20E 24

<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	DGG OR DL PACKAG (TOP VIEW)			
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>		48 1CLK		
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-833, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, B = 0)</li> </ul>	1Q1 []2 1Q2 []3 GND []4 1Q3 []5	47 1D1 46 1D2 45 GND 44 1D3		
<ul> <li>R = 0)</li> <li>Latch-Up Performance Exceeds 250 mA</li> <li>Per JEDEC Standard JESD-17</li> </ul>	1Q4 <b>[</b> 6 V <sub>CC</sub> <b>[</b> 7 1Q5 <b>[</b> 8	43 ] 1D4 42 ] V <sub>CC</sub> 41 ] 1D5		
<ul> <li>Bus Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	1Q6 [] 9 GND [] 10 1Q7 [] 11	40 106 39 GND 38 107		
<ul> <li>Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages</li> </ul>	1Q8 [ 12 2Q1 [ 13 2Q2 [ 14	37 ] 1D8 36 ] 2D1 35 ] 2D2		
description	GND 15 2Q3 16	34 GND 33 2D3		
This 16-bit edge-triggered D-type flip-flop is designed for 2.3-V to 3.6-V V <sub>CC</sub> operation.	2Q4 [] 17 V <sub>CC</sub> [] 18 2Q5 [] 19	32 2D4 31 V <sub>CC</sub> 30 2D5		
The SN74ALVCH16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It	2Q6 [ 20 2Q6 [ 20 GND [ 21 2Q7 [ 22	29 2D5 29 2D6 28 GND 27 2D7		
can be used as two 8-bit flip-flops or one 16-bit	2Q8 23	26 2D8		

can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.  $\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16374 is characterized for operation from -40°C to 85°C.

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flip-flop. On the positive transition of the clock

(CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.  $\overline{OE}$ )

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



### SN74ALVCH16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS SCES021A – JULY 1995 – REVISED NOVEMBER 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 4.6 V
Input voltage range, VI (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±50 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>CC</sub> )	±50 mA
Continuous current through each V <sub>CC</sub> or GND	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 3): DGG package	0.85 W
	1.2 W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

### recommended operating conditions (see Note 4)

	s		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.3	3.6	V
VIH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		v
ЧН		V <sub>CC</sub> = 2.7 V to 3.6 V	2		v
VIL	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	v
۲IL		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	v
٧I	Input voltage		0	VCC	V
Vo	Output voltage		0	VCC	V
		V <sub>CC</sub> = 2.3 V		-12	
ЮН	High-level output current	V <sub>CC</sub> = 2.7 V		-12	mA
		V <sub>CC</sub> = 3 V		-24	
		V <sub>CC</sub> = 2.3 V		12	
lol	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
		V <sub>CC</sub> = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



### SN74ALVCH16374 **16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP** WITH 3-STATE OUTPUTS SCES021A – JULY 1995 – REVISED NOVEMBER 1996

noted	) (see Figures 1 and 2)	-		-					
		\ \	/CC = ± 0.2		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = ± 0.3	3.3 V 3 V	UNIT
		· · · ·	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	150	0	150	MHz
tw	Pulse duration, CLK high or low		3.3		3.3		3.3		ns
tsu	Setup time, data before CLK1		2.1		2.2		1.9		ns
th	Hold time, data after CLK↑		0.6		0.5		0.5		ns

## timing requirements over recommended operating free-air temperature range (unless otherwise

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.	2.5 V 2 V	V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = ± 0.:	3.3 V 3 V	UNIT
	(INPUT)	(001201)	MIN	MAX	MIN	MAX	MIN	MAX	
fmax			150		150		150		MHz
<sup>t</sup> pd	CLK	Q	1	5.9		4.9	1	4.2	ns
ten	CLK	Q	1	6.7		5.9	1	4.8	ns
<sup>t</sup> dis	CLK	Q	1.7	5.5		4.7	1.2	4.3	ns

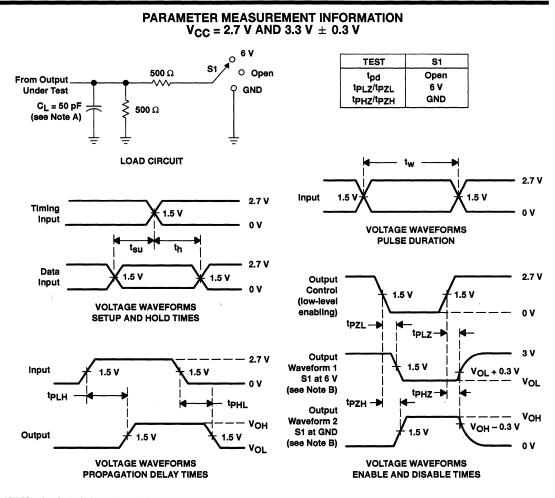
### operating characteristics, T<sub>A</sub> = 25°C

	PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
		Outputs enabled		31	30	pF
C <sub>pd</sub> Power dissipation capacitance		Outputs disabled	C <sub>L</sub> = 50 pF, f = 10 MHz	16	18	рг



### SN74ALVCH16374 **16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP** WITH 3-STATE OUTPUTS

SCES021A - JULY 1995 - REVISED NOVEMBER 1996



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns. C. D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tp71 and tp7H are the same as ten.
- G. tpLH and tpHL are the same as tpd.

### Figure 2. Load Circuit and Voltage Waveforms



#### SN54LVTH16374, SN74LVTH16374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS SCB5145F - MAY 1992 - REVISED NOVEMBER 1996

20E ||24

25 2CLK

SCBS	1451 -	- MAY	1992	– HEV	ISED	NOV	EMBEH	

<ul> <li>State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power</li> </ul>	SN54LVTH16374 WD PACKAGE SN74LVTH16374 DGG OR DL PACKAGE (TOP VIEW)
Dissipation	
<ul> <li>Members of the Texas Instruments Widebus™ Family</li> </ul>	1Q1 🛛 2 47 🖉 1D1
<ul> <li>Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)</li> </ul>	1Q2 0 3 46 1D2 GND 0 4 45 GND
· · · · · · · · · · · · · · · · · · ·	1Q3 5 44 1D3
<ul> <li>Support Unregulated Battery Operation</li> </ul>	
Down to 2.7 V	$V_{CC}$ 7 42 $V_{CC}$
<ul> <li>High-Impedance State During Power Up</li> </ul>	1Q5 8 41 1D5
and Power Down	1Q6 <b>]</b> 9 40 <b>]</b> 1D6
<ul> <li>Typical V<sub>OLP</sub> (Output Ground Bounce)</li> </ul>	
< 0.8 V at V <sub>CC</sub> = 3.3 V, T <sub>A</sub> = 25°C	1Q7 11 38 1D7
ESD Protection Exceeds 2000 V Per	1Q8 12 37 1D8
MIL-STD-883, Method 3015; Exceeds 200 V	2Q1 13 36 2D1
Using Machine Model	2Q2 <b>1</b> 4 35 2D2
(C = 200  pF, R = 0)	
<ul> <li>Latch-Up Performance Exceeds 500 mA</li> </ul>	2Q3 🛛 16 33 🗍 2D3
Per JEDEC Standard JESD-17	2Q4 <b>[</b> 17 32 <b>]</b> 2D4
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown</li> </ul>	2Q5 19 30 2D5
Resistors	2Q6 20 29 2D6
<ul> <li>Power Off Disables Inputs/Outputs,</li> </ul>	2Q7 22 27 2D7
Permitting Live Insertion	2Q8 [23 26] 2D8

- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

#### description

The 'LVTH16374 are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

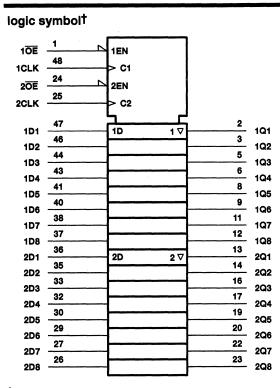
These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

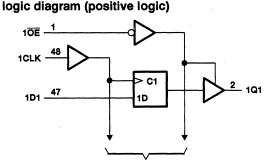
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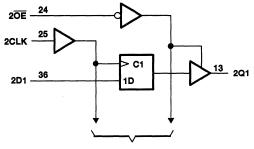


### SN54LVTH16374, SN74LVTH16374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS SCBS145F - MAY 1992 - REVISED NOVEMBER 1996





**To Seven Other Channels** 



**To Seven Other Channels** 

<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>1</sub> (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, VO (see Note	1)0.5 V to 7 V
Current into any output in the low state, Io: SN54LVTH16374	96 mA
SN74LVTH16374	
Current into any output in the high state, IO (see Note 2): SN54LVTH16374	48 mA
SN74LVTH16374	64 mA
Input clamp current, IIK (VI < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG package	
	1.2 W
Storage temperature range, T <sub>stg</sub>	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book.



## SN54LVTH16374, SN74LVTH16374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS145F - MAY 1992 - REVISED NOVEMBER 1996

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ADAMETED	TESTO	CONDITIONS		4LVTH10	6374	SN74	UNIT		
	ARAMETER	TEST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK		V <sub>CC</sub> = 2.7 V,	lj = −18 mA			-1.2			-1.2	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	l <sub>OH</sub> = -100 μA	Vcc-0	).2		Vcc-0	.2		
VOH		V <sub>CC</sub> = 2.7 V,	IOH =8 mA	2.4			2.4			v
		V <sub>CC</sub> = 3 V	IOH = -24 mA	2						v
		VCC = 3 V	IOH = -32 mA				2			
		V <sub>CC</sub> = 2.7 V	l <sub>OL</sub> = 100 μA			0.2			0.2	
		VCC = 2.7 V	I <sub>OL</sub> = 24 mA			0.5			0.5	
Va			I <sub>OL</sub> = 16 mA			0.4			0.4	v
VOL		V <sub>CC</sub> = 3 V	I <sub>OL</sub> = 32 mA			0.5			0.5	V
		VCC = 3 V	I <sub>OL</sub> = 48 mA			0.55				
			IOL = 64 mA			í.			0.55	
		V <sub>CC</sub> = 0 or 3.6 V	VI = 5.5 V			🕺 10			10	
կ	Control inputs	V <sub>CC</sub> = 3.6 V,	VI = V <sub>CC</sub> or GND		Ž	/ ±1			±1	
	Data inputs	V <sub>CC</sub> = 3.6 V	VI = V <sub>CC</sub>		A	· 1			1	μA
	Data inputs	VCC = 3.0 V	VI = 0		de la compañía de la	-5			-5	
loff		V <sub>CC</sub> = 0,	$V_{I} \text{ or } V_{O} = 0 \text{ to } 4.5 \text{ V}$		õ	±100			±100	μA
1	Data inputs	Vac. 2.V	VI = 0.8 V	75.	»		75			
li(hold)	Data inputs	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 2 V	-75			-75			μA
IOZH		V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V			5			5	μA
IOZL		V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V			-5			-5	μA
lozpu‡		V <sub>CC</sub> = 0 to 1.5 V, V <sub>C</sub>	= 0.5 V to 3 V, OE = X			±100			±100	μA
IOZPD <sup>‡</sup>		V <sub>CC</sub> = 1.5 V to 0, V <sub>C</sub>	) = 0.5 V to 3 V, OE = X			±100			±100	μA
	Outputs high					0.19			0.19	
ICC	Outputs low	$V_{CC} = 3.6 V,$ $V_{I} = V_{CC} \text{ or GND}$	lO = 0,			5			5	mA
	Outputs disabled					0.19		0.19		
∆I <sub>CC</sub> §		$V_{CC} = 3 V \text{ to } 3.6 V, C$ Other inputs at $V_{CC}$ o	Dne input at V <sub>CC</sub> – 0.6 V, r GND			0.2			0.2	mA
Ci		V <sub>I</sub> = 3 V or 0			3			3		pF
Co		V <sub>O</sub> = 3 V or 0			9			9		pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

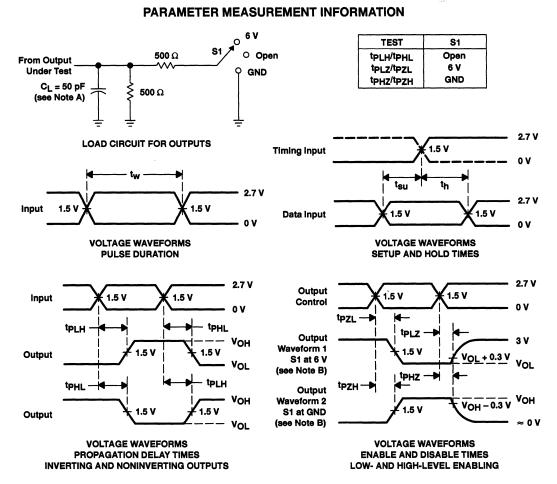
<sup>‡</sup> This parameter is characterized but not tested.

\$ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



### SN54LVTH16374, SN74LVTH16374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS145F - MAY 1992 - REVISED NOVEMBER 1996



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



### SN74ALVCH16835 **18-BIT UNIVERSAL BUS TRANSCEIVER** WITH 3-STATE OUTPUTS

SCES053A - SEPTEMBER 1995 - REVISED NOVEMBER 1996

● Member of the Texas Instruments	DGG OR DL PACKAGE
<i>Widebus</i> ™ Family	(TOP VIEW)
<ul> <li>EPIC<sup>™</sup> (Enhanced-Performance implanted CMOS) Submicron Process</li> </ul>	
<ul> <li>Bus Hold on Data Inputs Eliminates the</li></ul>	NC 2 55 NC
Need for External Pullup/Pulldown	Y1 3 54 A1
Resistors	GND 4 53 GND
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)</li> </ul>	Y2 5 52 A2 Y3 6 51 A3 V <sub>CC</sub> 7 50 V <sub>CC</sub> Y4 8 49 A4
<ul> <li>Latch-Up Performance Exceeds 250 mA Per</li></ul>	Y5 🛛 9 48 🗍 A5
JEDEC Standard JESD-17	Y6 🖸 10 47 🗍 A6
<ul> <li>Package Options Include Plastic Shrink</li></ul>	GND 11 46 GND
Small-Outline (DL) and Thin Shrink	Y7 12 45 A7
Small-Outline (DGG) Packages	Y8 13 44 A8
description	Y9 14 43 A9 Y10 15 42 A10 Y11 16 41 A11
This 18-bit universal bus driver is designed for 2.3-V to 3.6-V V $_{CC}$ operation.	Y12 [ 17 40 ] A12 GND [ 18 39 ] GND
Data flow from A to Y is controlled by the output-enable $(\overline{OE})$ . The device operates in the	Y13 [] 19   38 [] A13 Y14 [] 20   37 [] A14
transparent mode when the latch-enable (LE)	Y15 21 36 A15
input is high. The A data is latched if the clock	V <sub>CC</sub> 22 35 V <sub>CC</sub>
(CLK) input is held at a high or low logic level. If LE	Y16 23 34 A16
is low, the A-bus data is stored in the latch/flip-flop	Y17 24 33 A17
on the low-to-high transition of CLK. When OE is	GND 25 32 GND

#### d

on the low-to-high transition of CLK. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, OE should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

· UU 4			1.00
Y16			]A16
Y17 [	24		A17
GND [		32	] GND
Y18[	26		A18
OE [	27	30	]CLK
LE [	28	29	] GND
		السبي	-
NC – N	o interna	al coi	nnection

NC

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16835 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16835 is characterized for operation from -40°C to 85°C.

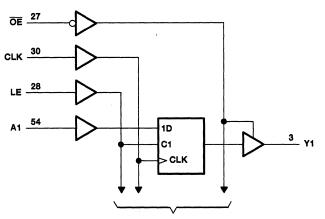
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DOUCTION DATA information is current as of publication Texas instrum tion date Products conform to specifications standard warranty. Production proc ng does not necessarily include of all na



### SN74ALVCH16835 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES053A – SEPTEMBER 1995 – REVISED NOVEMBER 1996

logic diagram (positive logic)



To Seventeen Other Channels

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 4.6 V
Input voltage range, VI (see Note 1)	
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	–0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, IIK (VI < 0)	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 3): DO	GG package 1 W
DI	_ package 1.4 W
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.*



### SN74ALVCH16835 **18-BIT UNIVERSAL BUS TRANSCEIVER** WITH 3-STATE OUTPUTS SCES053A - SEPTEMBER 1995 - REVISED NOVEMBER 1996

	PARAMETER	TEST	CONDITIONS	Vcc	MIN	TYP†	MAX	UNIT	
		l <sub>OH</sub> = -100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -0.2				
		I <sub>OH</sub> = -6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2				
v <sub>OH</sub>			V <sub>IH</sub> = 1.7 V	2.3 V	1.7			v	
	I <sub>OH</sub> = -12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2			v		
			V <sub>IH</sub> = 2 V	3 V	2.4				
		I <sub>ОН</sub> = -24 mA,	V <sub>IH</sub> = 2 V	3 V	2				
		l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V			0.2		
		1 <sub>OL</sub> = 6 mA,	V <sub>IL</sub> = 0.7 V	2.3 V			0.4		
VOL		10	V <sub>IL</sub> = 0.7 V	2.3 V			0.7	.7 V	
	l <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.8 V	2.7 V			0.4			
		I <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V			0.55		
ų		VI = VCC or GND		3.6 V			±5	μA	
<u> </u>		VI = 0.7 V		2.3 V	45				
		V <sub>I</sub> = 1.7 V		2.3 V	-45				
ll(hold	(t	V <sub>I</sub> = 0.8 V	V <sub>1</sub> = 0.8 V V <sub>1</sub> = 2 V		75			μΑ	
•		V <sub>1</sub> = 2 V			-75				
		$V_{ } = 0$ to 3.6 V <sup>‡</sup>		3.6 V			±500		
loz		VO = VCC or GND		3.6 V			±10	μA	
ICC		$V_1 = V_{CC}$ or GND,	IO = 0	3.6 V			40	μA	
∆ICC		One input at $V_{CC} - 0.6$ Other inputs at $V_{CC}$ or	V, GND	3 V to 3.6 V			750	μA	
~	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V		3.5		~5	
Ci	Data inputs	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V		6		pF	
Cio	Outputs	VO = VCC or GND		3.3 V		7		pF	

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<sup>†</sup> All typical values are at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}$ C.

<sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

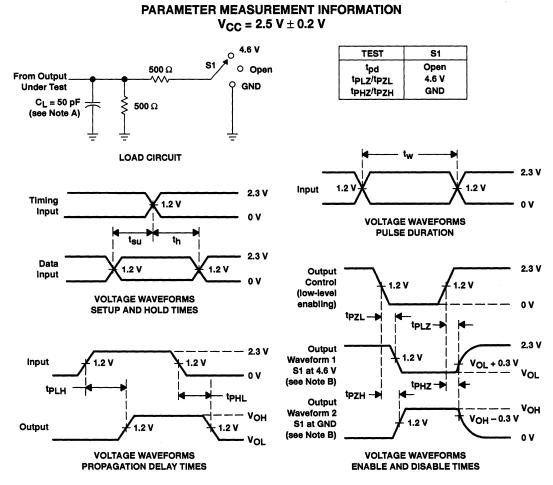
# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				= 2.5 V 0.2 V V <sub>CC</sub> =		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V	
			MIN	MAX	MIN	MAX	MIN	MAX	
fciock	Clock frequency		0	150	0	150	0	150	MHz
	Pulse duration	LE high	3.3		3.3		3.3		
<sup>t</sup> w	Pulse duration	CLK high or low	3.3		3.3		3.3		ns
		Data before CLK1	2.2		2.1		1.7		ns
t <sub>su</sub>	Setup time	Data before LE↓, CLK high	1.9		1.6		1.5		
		Data before LE↓, CLK low	1.3		1.1		1		
•.	Hold time	Data after CLK1	0.6		0.6		0.7		
<sup>t</sup> h		Data after LE↓, CLK high or low	1.4		1.7		1.4		ns



### SN74ALVCH16835 **18-BIT UNIVERSAL BUS TRANSCEIVER** WITH 3-STATE OUTPUTS

SCES053A - SEPTEMBER 1995 - REVISED NOVEMBER 1996



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>Q</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpi 7 and tpH7 are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

### Figure 1. Load Circuit and Voltage Waveforms



### SN74LVT16835 3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

I F**N** 28

29 1 GND

NC - No internal connection

SCBS309D - MARCH 1994 - REVISED NOVEMBER 1996

<ul> <li>State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V</li> </ul>	DGG OR DL PACKAGE (TOP VIEW)				
Operation and Low-Static Power Dissipation		56 GND			
<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	NC 2 Y1 3				
<ul> <li>Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)</li> </ul>	GND 4 Y2 5 Y3 6	51 🛛 A3			
<ul> <li>Supports Unregulated Battery Operation Down to 2.7 V</li> </ul>	V <sub>CC</sub> 7 Y4 8 Y5 9	50 ] V <sub>CC</sub> 49 ] A4 48 ] A5			
<ul> <li>Typical V<sub>OLP</sub> (Output Ground Bounce)</li> <li>&lt; 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C</li> </ul>	Y6 10 GND 11				
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	Y7 [] 12 Y8 [] 13 Y9 [] 14	44 🛛 A8 43 🖉 A9			
Supports Live Insertion	Y10 15				
<ul> <li>Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise</li> </ul>	Y11 16 Y12 17 GND 18	40 🛛 A12			
<ul> <li>Flow-Through Architecture Optimizes PCB Layout</li> </ul>	Y13 19 Y14 20	38 🛛 A13			
<ul> <li>Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink</li> </ul>	Y15 21 V <sub>CC</sub> 22				
Small-Outline (DGG) Packages Using 25-mil Center-to-Center Spacings	Y16 23	34 A16 33 A17			
description	GND 25 Y18 26	31 🛛 A18			
The SN74LVT16835 is an 18-bit universal bus	OE 27	30 🛛 CLK			

The SN74LVT16835 is an 18-bit universal bus driver designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow from A to Y is controlled by the output-enable  $(\overline{OE})$  input. This device operates in the transparent mode when the latch-enable (LE)

input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of the clock. When OE is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16835 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the input/output (I/O) pins and functionality of standard small-outline packages in the same printed circuit board area.

The SN74LVT16835 is characterized for operation from -40°C to 85°C.

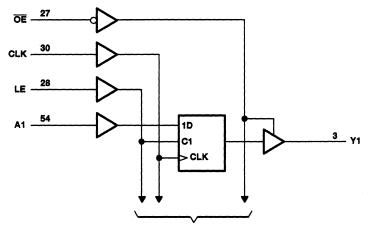
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### SN74LVT16835 **3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER** WITH 3-STATE OUTPUTS SCBS309D - MARCH 1994 - REVISED NOVEMBER 1996

logic diagram (positive logic)



To 17 Other Channels

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub> Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high state or power-off state,	
Current into any output in the low state, Io	
Current into any output in the high state, IO (see Note 2)	64 mÅ
Input clamp current, IIK (VI < 0)	
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0)	
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG	i package 1 W
	ackage 1.4 W
Operating free-air temperature range, TA	
Storage temperature range, Tstg	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book.



# timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V	
			MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	125	MHz
	Pulse duration	LE high	3.3	3.3 3.3			
tw		CLK high or low	3.3		3.3		ns
		Data before CLK↑	1.6		2.1		
tsu	Setup time	Data before LE↓, CLK high	2.6	1.9		ns	
		Data before LE↓, CLK low	2		1.3		
th	Hold time Data after CLK↑ Data after LE↓	Data after CLK↑	2		2.1	****	
		0.9		1.2		ns	

# switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	$V_{CC}=3.3~V\pm0.3~V$			V <sub>CC</sub> = 2.7 V		UNIT
FANAMEIEN	(INPUT)		MIN	TYPT	MAX	MIN	MAX	UNIT
fmax			150			150		MHz
<sup>t</sup> PLH	А	v	1.7	3	5.4		6.8	
<sup>t</sup> PHL	^	T	1.6	3.2	5.9		7.7	ns
<sup>t</sup> PLH	tpLH LE LE	Y	2.3	4	7		8.5	ns
<sup>t</sup> PHL		1	2.7	4.3	7.9		9.7	115
<sup>t</sup> PLH	CLK	Y	2.5	4.1	7.9		9.2	ns
<sup>t</sup> PHL	ULK	1	3.5	5.4	8.9		10.4	115
<sup>t</sup> PZH	ŌĒ	Y	1.2	3	5		5.9	ns
<sup>t</sup> PZL	ÛE	T	1.5	3	5.8		6.9	115
<sup>t</sup> PHZ	ŌĒ	Y	2.7	4.6	7.4		8.3	ns
<sup>t</sup> PLZ		r	2.8	4.7	6.7		7.2	115

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.



### SN74ALVCH16825 **18-BIT BUFFER/DRIVER** WITH 3-STATE OUTPUTS

SCES039A - JULY 1995 - REVISED NOVEMBER 1996

<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	DGG OR DL PACKAGE (TOP VIEW)				
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	10E1 1Y1			10E2 1A1	
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	1Y2 GND	3	54	1A2 GND	
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method3015; Exceeds</li> </ul>	1Y3 [ 1Y4 [	5	52	1A3 1A4	
200 V Using Machine Model (C = 200 pF, R = 0)	V <sub>CC</sub> [ 1Y5 [	8	49	V <sub>CC</sub> 1A5	
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown</li> </ul>	1Y6 [ 1Y7 [	10	47	1A6 1A7	
<ul> <li>Resistors</li> <li>Package Options Include Plastic 300-mil</li> </ul>	GND [ 1Y8 [			GND 1A8	
Shrink Small-Outline (DL) and Thin Shrink	1Y9 [	13	44	1A9	
Small-Outline (DGG) Packages	GND [ GND [			GND GND	
description	2Y1 [ 2Y2 [			2A1 2A2	
This 18-bit buffer and line driver is designed for 2.3-V to 3.6-V V <sub>CC</sub> operation.	GND [ 2Y3 [	18	39	GND 2A3	
This SN74ALVCH16825 improves the perform- ance and density of 3-state memory address	2Y4 [ 2Y5 ]	20	37	2A4 2A5	
drivers, clock drivers, and bus-oriented receivers and transmitters.	V <sub>CC</sub> [ 2Y6 [	23	34	V <sub>CC</sub>   2A6	
The device can be used as two 9-bit buffers or one 18-bit buffer. It provides true data.	2Y7 [ GND [	25	32	2A7 GND	
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable	2Y8 [ 2Y9 [ 2 <del>0E1</del> [	27	30	2A8 2A9 2OE2	
(OE1 or OE2) input is high, all nine affected	2021	Ľ.		J 2062	

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16825 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16825 is characterized for operation from -40°C to 85°C.

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outputs are in the high-impedance state.

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### SN74ALVCH16825 18-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS SCES039A – JULY 1995 – REVISED NOVEMBER 1996

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG package .	
DL package	1.4 W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book.

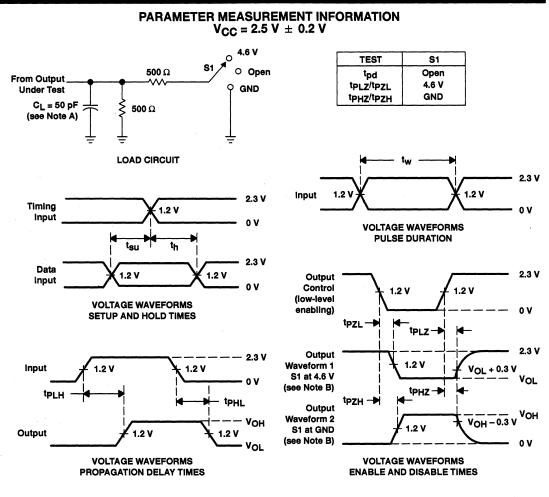
### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
V	High-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v
⊻н	High-level liput voltage	$V_{CC} = 2.7 V \text{ to } 3.6 V$	2		v
V	Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
VIL		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	
٧I	Input voltage		0	VCC	V
Vo	Output voltage			VCC	V
		V <sub>CC</sub> = 2.3 V		-12	
ЮН	High-level output current	V <sub>CC</sub> = 2.7 V		-12	mA
		V <sub>CC</sub> = 3 V		-24	
		V <sub>CC</sub> = 2.3 V		12	[
lol	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
		V <sub>CC</sub> = 3 V		24	l
∆t/∆v	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature	-40	85	°C	

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



#### SN74ALVCH16825 **18-BIT BUFFER/DRIVER** WITH 3-STATE OUTPUTS SCES039A - JULY 1995 - REVISED NOVEMBER 1996



NOTES: A. Cl includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.

F. tpzL and tpzH are the same as ten.

G. tpLH and tpHL are the same as tod.

#### Figure 1. Load Circuit and Voltage Waveforms



# SN74ALVCH16843 18-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

DGG OR DL PACKAGE

SCES044A - JULY 1995 - REVISED NOVEMBER 1996

- Member of the Texas Instruments Widebus™ Family
- **EPIC**™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown** Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

#### description

This 18-bit bus-interface D-type latch is designed for 2.3-V to 3.6-V V<sub>CC</sub> operation.

The SN74ALVCH16843 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working reaisters.

The SN74ALVCH16843 can be used as two 9-bit latches or one 18-bit latch. The 18 latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable (OE) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs also are in the high-impedance state during power-up and power-down

(TOP VIEW)										
1	<u> </u>									
1CLR		56 🛛 1LE								
10E		55 1 1PRE								
1Q1 🛛	3	54 🛛 1D1								
GND 🛛	4	53 🛛 GND								
1Q2 🛛	5	52 1D2								
1Q3 🛛	6	51 🛛 1D3								
V <sub>CC</sub>	7	50 V <sub>CC</sub>								
1Q4 [	8	49 1D4								
1Q5 🛛	9	48 🛛 1D5								
1Q6 🛛	10	47 🛛 1D6								
	11	46 GND								
1Q7 🛛		45 <b>0</b> 1D7								
1Q8 🛛		44 🛛 1D8								
1Q9 🛛	14	43 🛛 1D9								
2Q1 [		42 2D1								
2Q2 🛛	16	41 <b>2</b> 2D2								
2Q3 🏾	17	40 <b>2</b> 2D3								
GND 🛛	18	39 🛛 GND								
2Q4 🛛		38 <b>]</b> 2D4								
2Q5 🛛		37 <b>2</b> 2D5								
2Q6 [		36 2D6								
v <sub>cc</sub> [		35 V <sub>CC</sub>								
2Q7 🏾		34 <b>[</b> 2D7								
2Q8 🛛		33 🛛 2D8								
GND 🛛	25	32 🛛 GND								
2Q9 🛛		31 2D9								
2OE		30 2 2 PRE								
2CLR	28	29 2LE								

PRODUCT PREVIEW

conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16843 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16843 is characterized for operation from -40°C to 85°C.

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### SN74ALVCH16843 18-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES044A - JULY 1995 - REVISED NOVEMBER 1996

#### FUNCTION TABLE

	(each 9-bit latch)											
	INPUTS											
 PRE	CLR	ŌĒ	LE	D	a							
L	х	L	х	х	н							
н	L	L	х	x	L							
н	н	L	н	L	L							
н	н	L	н	н	н							
н	н	L	L	Х	Q <sub>0</sub>							
 х	Х	н	Х	Х	Z							

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub> Input voltage range, V <sub>1</sub> (see Note 1) Output voltage range, V <sub>O</sub> (see Notes 1 and 2) Input clamp current, $I_{IK}$ (V <sub>1</sub> < 0) Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> ) Continuous output current, $I_O$ (V <sub>O</sub> = 0 to V <sub>CC</sub> )	-0.5 V to 4.6 V -0.5 V to V <sub>CC</sub> + 0.5 V -50 mA ±50 mA ±50 mA
Continuous current through each V <sub>CC</sub> or GND	
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG package	
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v
VIН	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2		v
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
VIL	Low-level input voltage		0.8	v	
VI	Input voltage		0	Vcc	V
Vo	Output voltage		0	VCC	V
		V <sub>CC</sub> = 2.3 V		-12	
ЮН	High-level output current	V <sub>CC</sub> = 2.7 V		-12	mA
		V <sub>CC</sub> = 3 V		24	1
		V <sub>CC</sub> = 2.3 V		12	
IOL	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
			24		
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



# SN74ALVCH16823 **18-BIT BUS-INTERFACE FLIP-FLOP** WITH 3-STATE OUTPUTS

SCES038A - JULY 1995 - REVISED NOVEMBER 1996

34 2D7

3312D8

32 GND

31 2D9

30 2CLKEN

29 20LK

2Q7 23

2Q8 🛛 24

GND 25

2Q9 26

20E 27

2CLR 28

● Member of the Texas Instruments <i>Widebus</i> ™ Family	DGG OR DL PACKAGE (TOP VIEW)
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	1CLR 1 56 1CLK 1OE 2 55 1CLK
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)</li> </ul>	1Q1 [] 3 54 [] 1D1 GND [] 4 53 [] GND 1Q2 [] 5 52 [] 1D2
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	1Q3 [] 6 51 [] 1D3 V <sub>CC</sub> [] 7 50 [] V <sub>CC</sub> 1Q4 [] 8 49 [] 1D4
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	1Q5 []9 48 [1D5 1Q6 []10 47 ]1D6 GND []11 46 ]GND
<ul> <li>Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages</li> </ul>	1Q7 [] 12 45 ]] 1D7 1Q8 [] 13 44 ]] 1D8 1Q9 [] 14 43 ]] 1D9
description	2Q1 0 15 42 2D1 2Q2 0 16 41 2D2
This 18-bit bus-interface flip-flop is designed for 2.3-V to 3.6-V $V_{CC}$ operation.	2Q3 [ 17 40 ] 2D3 GND [ 18 39 ] GND 2Q4 [ 19 38 ] 2D4
The SN74ALVCH16823 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is	2Q5

particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The SN74ALVCH16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable (CLKEN) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high disables the clock buffer, thus latching the outputs. Taking the clear (CLR) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable (OE) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

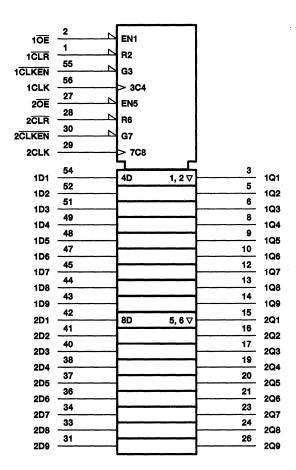
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#### SN74ALVCH16823 **18-BIT BUS-INTERFACE FLIP-FLOP** WITH 3-STATE OUTPUTS SCES038A - JULY 1995 - REVISED NOVEMBER 1996

logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



#### SN74ALVCH16823 18-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCES038A – JULY 1995 – REVISED NOVEMBER 1996

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	05V to 46V
Input voltage range, V <sub>1</sub> (see Note 1)	
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	–0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, IIK (VI < 0)	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V <sub>CC</sub> or GND	
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.*

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	v
V	High lovel input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v
VIH	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2		Ň
<b>V</b>	Low-level input voltage	$V_{CC} = 2.3 V \text{ to } 2.7 V$		0.7	v
VIL		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	v
٧I	Input voltage		0	VCC	v
Vo	Output voltage		0	VCC	v
		V <sub>CC</sub> = 2.3 V		-12	
ЮН	High-level output current	V <sub>CC</sub> = 2.7 V		-12	mA
		V <sub>CC</sub> = 3 V		-24	
		V <sub>CC</sub> = 2.3 V		12	
IOL	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
			24	1	
∆t/∆v	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



#### SN74ALVCH16823 18-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCES038A – JULY 1995 – REVISED NOVEMBER 1996

				$\begin{array}{c c} V_{CC} = 2.5 V \\ \pm 0.2 V \end{array}  V_{CC} = 2.7 \end{array}$		2.7 V	V <sub>CC</sub> = ± 0.3	UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	150	0	150	MHz
t <sub>w</sub>	Pulse duration	CLR low	3.3		3.3		3.3		
	Pulse duration	CLK high or low	3.3		3.3		3.3		ns
		CLR low	0.7		0.7		0.8		
	O store that a	Data low	1.4		1.6		1.3		ns
tsu	Setup time	Data high	1.1		1.1		1		
		CLKEN low	1.8		1.9		1.5		
		Data low	0.4		0.5		0.5		
<sup>t</sup> h	Hold time	Data high	0.7		0.1		0.8		ns
		CLKEN low	0.2		0.3		0.4		

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

# switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figures 1 and 2)

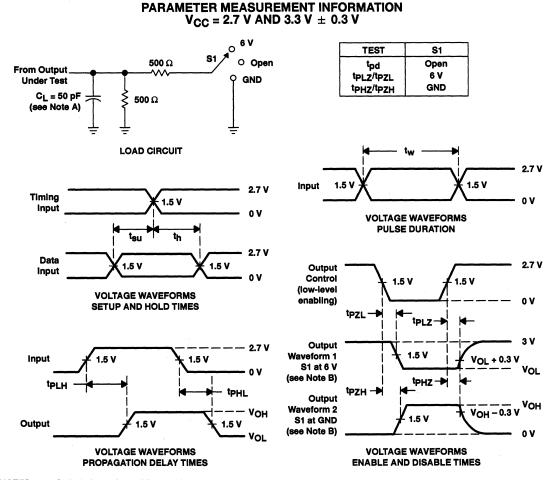
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.3	2.5 V 2 V	V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = ± 0.3	3.3 V 3 V	UNIT
		(001401)	MIN	MAX	MIN	MAX	MIN	MAX	
fmax			150		150		150		MHz
• .	CLK	Q	1	6.4		5.2	1	4.5	
<sup>t</sup> pd	CLR	Q	1.4	6		5.2	1.2	4.6	ns
ten	ŌĒ	Q	1	6.5		5.7	1	4.8	ns
<sup>t</sup> dis	ŌĒ	Q	1.8	5.6		4.7	1.3	4.5	ns

# operating characteristics, T<sub>A</sub> = 25°C

	PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V TYP	V <sub>CC</sub> = 3.3 V ± 0.3 V TYP	UNIT
	Outputs enabled	C) E0 = E ( 10 MU	27	30	- 5	
Cpd	Power dissipation capacitance	Outputs disabled	C <sub>L</sub> = 50 pF, f = 10 MHz	16	18	рF



#### SN74ALVCH16823 18-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCES038A – JULY 1995 – REVISED NOVEMBER 1996



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzi and tpzH are the same as ten.
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- a. PLH and PHL are the same as tpg.

Figure 2. Load Circuit and Voltage Waveforms



#### SN74ALVCH16830 **1-TO-2 ADDRESS DRIVER** WITH 3-STATE OUTPUTS SCES081 - AUGUST 1996

•			f the Te ' Family		strum	ents		_	BB PAC (TOP V		E
•		•	nhance bmicro			nce Imp	blanted	2Y2 [ 1Y2 [			] 1Y3 ] 2Y3
•	Bus	Hold (	on Data	Input	s Elim	ninates	the	GND [			GND
			xternal	Pullu	p/Pull	down		2Y1 [			1Y4
	Res	istors							5		2Y4
•	Plas	tic 300	)-mil Th	nin Sh	rink S	mall-O	utline	Vcc [	6	75	Vcc
	Pac	kage						A1 [	7		] 1Y5
								A2 [			2Y5
des	cripti	on						GND [			GND
	This	1-bit-to	-2-bit a	ddress	drive	r is des	igned for	A3 [	1		] 1Y6
			-V Vcc			10 000	ignou ioi		11		2Y6
			00	•			4. 1 1.1	GND [			GND
							to hold	A5 [			1Y7
	unuse	ed or th	oating ir	iputs a	at a va	na iogic	ievei.		14		2Y7
							ng power		15		V <sub>CC</sub>
							d to V <sub>CC</sub>	-	16		] 1Y8
							value of	A8 [ GND [	17 18		2Y8
					by the	e currer	nt-sinking				
	capal	cility of	the driv	ver.							] 1Y9 ] 2Y9
	The S	SN74A	LVCH16	5830 is	s pack	aged in	TI's thin	OE2	20		1Y10
							e, which	A10			2Y10
	provie	des twi	ce the l	/O pin	count	and fun	octionality	GND			GND
	of sta	Indard	small-o	utline	packa	ges in t	the same		24		1Y11
	printe	d-circu	lit-board	l area.				-	25		2Y11
	The	SN74	ALVCH1	6830	is ch	naracter	rized for		26		V <sub>CC</sub>
			om –40°					A13			1Y12
								A14			2Y12
			FUNC	TION T	ABLE			GND			GND
			INPUTS		OUT	PUTS		A15			j 1Y13
		OE1	OE2	A	1Yn	2Yn		A16	31	50	j 2Y13

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49 GND

48 🗍 1Y14

47 2Y14

46 VCC

45 1Y15

44 2Y15

43 GND

42 1Y16 41 1 2Y16

GND

A17

A18 34

Vcc [ 35

1Y18 🛛 37

GND

1Y17 40

2Y18 36

2Y17 [ 39

32

33

38

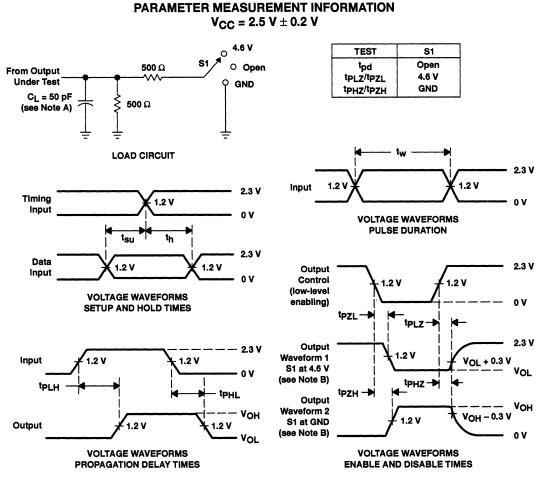
### SN74ALVCH16830 1-TO-2 ADDRESS DRIVER WITH 3-STATE OUTPUTS SCES081 - AUGUST 1996

### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
V		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v
VIH	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2		v
<b>M</b>		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
VIL	Low-level input voltage V <sub>CC</sub> = 2.7 V to 3.6 V				v
VI	Input voltage		0	VCC	v
Vo	Output voltage		0	Vcc	v
		V <sub>CC</sub> = 2.3 V		-12	
ЮН	High-level output current	V <sub>CC</sub> = 2.7 V		-12	mA
	r	V <sub>CC</sub> = 3 V		-24	
		V <sub>CC</sub> = 2.3 V		12	
<b>IOL</b>	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
		1	24		
∆t/∆v	Input transition rise or fall rate	······································	0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



#### SN74ALVCH16830 1-TO-2 ADDRESS DRIVER WITH 3-STATE OUTPUTS SCES081 - AUGUST 1996



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpHL and tpLH are the same as tpd.

#### Figure 1. Load Circuit and Voltage Waveforms





#### SN74ALVCH162830 1-TO-2 ADDRESS DRIVER WITH 3-STATE OUTPUTS SCE5082 - AUGUST 1996

- Member of the Texas instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Plastic 300-mil Thin Shrink Small-Outline
   Package

#### description

This 1-bit-to-2-bit address driver is designed for 2.3-V to 3.6-V  $V_{CC}$  operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The outputs, which are designed to sink up to 12 mA, include  $26 \cdot \Omega$  resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVCH162830 is packaged in TI's thin shrink small-outline (DBB) package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH162830 is characterized for operation from -40°C to 85°C.

	FOROTION TABLE					
	INPUTS			PUTS		
OE1	OE2	A	1Yn	2Yn		
L	н	н	н	Z		
L	н	L	L	z		
н	L	н	z	н		
н	L	L	z	L		
L	· L	н	н	н		
L	L	L	L	L		
н	н	X	z	z		

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FUNCTION TABLE

			SCES			
DBB PACKAGE (TOP VIEW)						
_						
2Y2 [	$1 \sim$	80	1Y3			
1Y2 [	2	79	2Y3			
GND [	3	78	GND			
2Y1 [	4	770	1Y4			
1Y1 [	5	76	2Y4			
V <sub>CC</sub> [	6	75	Vcc			
A1 [	7	74	1Y5			
A2 [	8	73	2Y5			
GND [	9	72	GND			
A3 [	10	71	1Y6			
A4 [	11	70	2Y6			
GND [	12	69	GND			
A5 [		68	1Y7			
A6 [		67	2Y7			
V <sub>CC</sub> [	15	66	V <sub>CC</sub>			
A7 [		65	1Y8			
A8 [		64	2Y8			
GND [		63	GND			
A9 [	19	62 <b>[</b> ]	1Y9			
OE1		61 <b>[</b> ]	2Y9			
OE2		60 <b>[</b>	1Y10			
A10 [	22	59	2Y10			
GND [	23	58	GND			
A11 [	24	57	1Y11			
A12 [	25	56	2Y11			
Vcc [	26	55	V <sub>CC</sub>			
A13 [	27	54	1Y12			
A14 [	28	53	2Y12			
GND [	29	52 <b>]</b>	GND			
A15 [	30	51	1Y13			
A16 [	31	50	2Y13			
GND [		49	GND			
A17 [		48 🛛	1Y14			
A18 [	34	47 <b>[</b>	2Y14			
V <sub>CC</sub> [		46 🛛	V <sub>CC</sub>			
2Y18 [		45 🛛	1Y15			
1Y18 [		44 []	2Y15			
GND [	38	43 []	GND			
2Y17 [		420	1Y16			
1Y17 [	40	<b>1</b> ]	2Y16			

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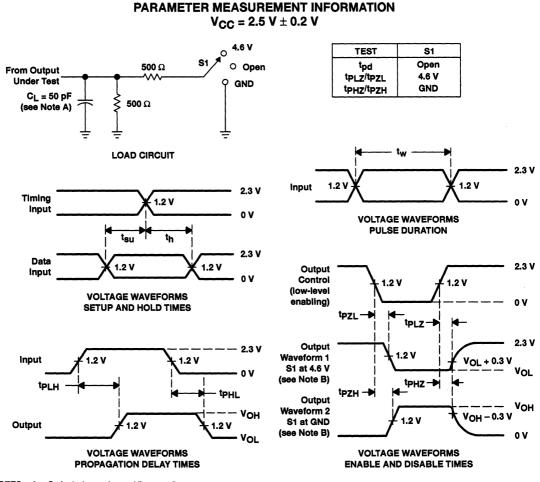


### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	v
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v
۷н	High-level input voltage	$V_{CC} = 2.7 V \text{ to } 3.6 V$	2		v
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
VIL Low-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	v	
VI	Input voltage		0	Vcc	V
Vo	Output voltage		0	Vcc	v
		V <sub>CC</sub> = 2.3 V		-6	
юн	High-level output current	V <sub>CC</sub> = 2.7 V		-8	mA
-		V <sub>CC</sub> = 3 V		-12	1
		V <sub>CC</sub> = 2.3 V	1	6	[
<b>IOL</b>	Low-level output current	V <sub>CC</sub> = 2.7 V		8	mA
	V <sub>CC</sub> = 3 V			12	1
∆t/∆v	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature	e de la contra la contra la contra de la contra contra contra contra contra contra contra contra contra contra ,	-40	85	°C



#### SN74ALVCH162830 1-TO-2 ADDRESS DRIVER WITH 3-STATE OUTPUTS SCES082 - AUGUST 1996



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G. tpHL and tpLH are the same as tpd.

#### Figure 1. Load Circuit and Voltage Waveforms





#### SN74ALVCH16836 20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS SCES089 - OCTOBER 1996

- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Member of the Texas Instruments Widebus™ Family
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

#### description

This 20-bit universal bus driver is designed for 2.3-V to 3.6-V  $V_{CC}$  operation.

Data flow from A to Y is controlled by the output-enable  $(\overline{OE})$  input. The device operates in the transparent mode when the latch-enable  $(\overline{LE})$  input is low. The A data is latched if the clock (CLK) input is held at a high or low logic level. If  $\overline{LE}$  is high, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLK. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16836 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16836 is characterized for operation from  $-40^{\circ}$ C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)					
ŌĒ		56 CLK			
Y1		55 🛛 A1			
Y2		54 🛛 A2			
GND		53 GND			
Y3		52 🛛 A3			
Y4		51 🛛 A4			
Vcc	7	50 V <sub>CC</sub>			
Y5	8	49 🛛 A5			
Y6	9	48 🛛 A6			
Y7		47 🛛 A7			
GND		46 GND			
Y8		45 🛛 A8			
Y9		44 🛛 A9			
Y10	14	43 🛛 A10			
Y11	15	42 A11			
Y12		41 🛛 A12			
Y13		40 🛛 A13			
GND	18	39 🛛 GND			
Y14	19	38 🛛 A14			
Y15	20	37 🛛 A15			
Y16	21	36 🛛 A16			
Vccl	22	35 🛛 V <sub>CC</sub>			
Y17	23	34 🛛 A17			
Y18	24	33 🛛 A18			
GND		32 GND			
Y19		31 🛛 A19			
Y20	27	30 🛛 A20			
NC		29] LE			

NC - No internal connection

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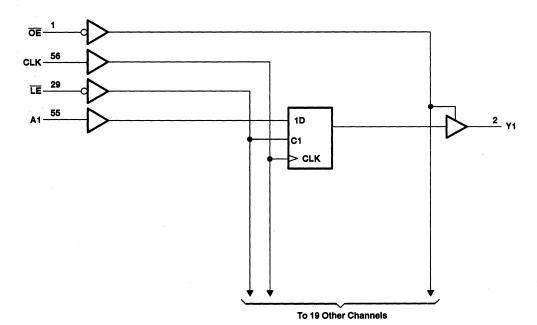
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#### SN74ALVCH16836 20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS SCESO89 - OCTOBER 1996

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	-0.5.V to 4.6.V
Input voltage range, VI (see Note 1)	–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, IIK (VI < 0)	–50 mA
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 3): DG	
DL	package 1.4 W
Storage temperature range, T <sub>stg</sub>	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABTAdvanced BiCMOS Technology Data Book*.



#### SN74ALVCH16836 20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS SCES089 - OCTOBER 1996

PARA	METER	TEST CONDITIONS		Vcc	MIN	түр†	MAX	UNIT
		I <sub>OH</sub> = -100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -0.2			
		l <sub>OH</sub> =6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2			v
V			V <sub>IH</sub> = 1.7 V	2.3 V	1.7			
VOH		IOH = -12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2			v
			VIH = 2 V	3 V	2.4			
		I <sub>OH</sub> = -24 mA,	V <sub>IH</sub>	3 V	2			
	••	lOL = 100 μA	·	2.3 V to 3.6 V			0.2	
		I <sub>OL</sub> = 6 mA,	V <sub>IL</sub> = 0.7 V	2.3 V			0.4	
VOL		l <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 V	2.3 V			0.7	v
			V <sub>IL</sub> = 0.8 V	2.7 V			0.4	
		l <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V			0.55	
lı		VI = V <sub>CC</sub> or GND		3.6 V			±5	μA
		V <sub>I</sub> = 0.7 V		2.3 V	45			
		VI = 1.7 V		2.3 V	-45			
Ihold		VI = 0.8 V VI = 2 V		3 V	75			μA
				1 *	75			
		V <sub>1</sub> = 0 to 3.6 V <sup>‡</sup>		3.6 V			±500	
loz§		$V_{O} = V_{CC}$ or GND		3.6 V			±10	μA
lcc		VI = V <sub>CC</sub> or GND,	IO = 0	3.6 V			40	μA
AICC		One input at V <sub>CC</sub> - 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA
0	Control inputs			2.2.1				~ <b>C</b>
Ci	Data inputs	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V				pF
Co	Outputs	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V		-		pF

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

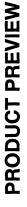
<sup>†</sup> All typical values are at  $V_{CC} = 3.3$  V.

<sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

§ For I/O ports, the parameter IOZ includes the input leakage current.

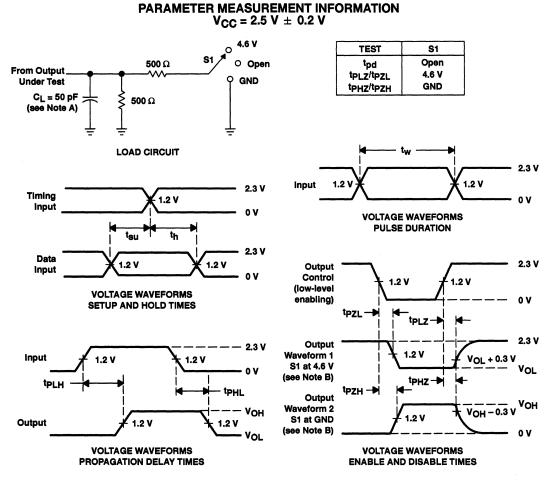
# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> = ± 0.		V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = ± 0.3		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency								MHz	
. Distanting		LE low	1							
t <sub>w</sub> Pulse du	Pulse duration	CLK high or low							ns	
		Data before CLK1	Т							
<sup>t</sup> su	Setup time	Data before LE↑, CLK high							ns	
		Data before LE↑, CLK low								
t <sub>h</sub> Hold time	Hald time	Data after CLK1								
		Data after $\overline{LE}$ , CLK high or low							ns	





#### SN74ALVCH16836 20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS SCES089 - OCTOBER 1996



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzi and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.
- a. IPLH and IPHL are the same as Ipd.

#### Figure 1. Load Circuit and Voltage Waveforms





SN74SSTL16837 20-BIT SSTL\_3 INTERFACE UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS SCB8075 - SEPTEMBER 1996

- Member of the Texas Instruments Widebus™ Family
- Supports SSTL\_3 Signal Inputs and Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Meets SSTL\_3 Class I and Class II Specifications
- Packaged in Plastic Thin Shrink Small-Outline Package

#### description

This 20-bit universal bus driver is designed for 3-V to 3.6-V  $V_{CC}$  operation and SSTL\_3 or LVTTL I/O levels.

Data flow from A to Y is controlled by the output-enable ( $\overline{OE}$ ). The device operates in the transparent mode when LE is high. The A data is latched if LE is low and CLK is held at a high or low logic level. If LE is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLK. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74SSTL16837 is available in TI's thin shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74SSTL16837 is characterized for operation from –40°C to 85°C.

DGG PACKAGE (TOP VIEW)						
GND [ Y3 [	1 2 3 4 5	63 62 61	] A1 ] A2 ] GND ] A3 ] A4			
V <sub>DDQ</sub> Y5 Y6 GND Y7	5 6 7 8 9 10	57 56 55	V <sub>CC</sub> A5 A6 GND A7			
	13 14 15	54 53 52 51 50	A8 V <sub>CC</sub> A9 A10 GND			
OE V <sub>REF</sub> GND Y11 Y12 V <sub>DDQ</sub>	16 17 18 19 20	48	CLK LE GND A11 A12 V <sub>CC</sub>			
Y13 [ Y14 [ GND [ Y15 ]	21 22 23 24 25 26	43 42 41 40	A13 A14 GND A15 A16			
V <sub>DDQ</sub> Y17 Y18 GND Y19	27 28 29	38 37 36 35	V <sub>CC</sub> A17 A18 GND A19			

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# 20-BIT SSTL\_3 INTERFACE UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS SCBS675 - SEPTEMBER 1996

#### recommended operating conditions (see Note 4)

				MIN	NOM	MAX	UNIT
VCC	Supply voltage			3		3.6	v
VDDQ	I/O supply voltage			3		3.6	V
VREF	Supply voltage			1.3	1.5	1.7	V
V <sub>I</sub> <sup>in</sup> i	Input voltage			0		Vcc	V
VIH	High-level input voltage	All pins		VREF+200m	v		V
VIL	Low-level input voltage	All pins			v	REF-200mV	V
ЮН	High-level output current				-20	mA	
IOL	Low-level output current					20	
TA	Operating free-air temperature			-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

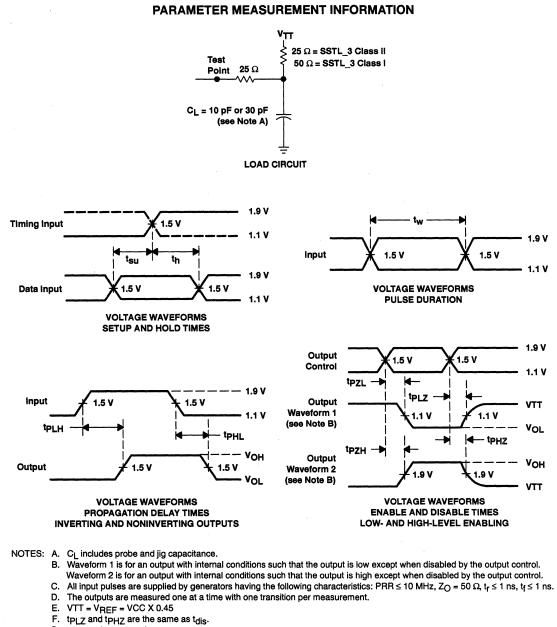
# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP <sup>†</sup>	MAX	UNIT		
٧ <sub>IK</sub>	IK V <sub>CC</sub> = 3 V   I <sub>I</sub> = -18 mA		lj = – 18 mA			-1.2	V	
		V <sub>CC</sub> = 3 V to 3.6 V	lOH = -100 μA					
VOH		V 2V	I <sub>OH</sub> = -16 mA	2.2			V	
		V <sub>CC</sub> = 3 V	I <sub>OH</sub> = -20 mA	2.1				
		V <sub>CC</sub> = 3 V to 3.6 V	l <sub>OL</sub> = 100 μA					
VOL		V 2V	IOH = 16 mA			0.5	V	
		V <sub>CC</sub> = 3 V	I <sub>OH</sub> = 20 mA			0.55	1	
	LE		V <sub>i</sub> = 2.1 V or 0.9V, V <sub>REF</sub> = 1.3 V or 1.7 V			±40		
	LE		V <sub>I</sub> = 3.6 V or 0, V <sub>REF</sub> = 1.3 V or 1.7 V			±500		
	Data inputs, OE		V <sub>I</sub> = 2.1 V or 0.9V, V <sub>REF</sub> = 1.3 V or 1.7 V			±5	μΑ	
lμ –	Data inputs, OE	V <sub>CC</sub> = 3.6 V	V <sub>I</sub> = 3.6 V or 0, V <sub>REF</sub> = 1.3 V or 1.7 V			±5	]	
	CLK		VI = 2.1 V or 0.9V, VREF = 1.3 V or 1.7 V			±150	]	
	CLK		VI = 3.6 V or 0, VREF = 1.3 V or 1.7 V			±2	mA	
	VREF		VREF = 1.3 V or 1.7 V			±150	μA	
la-		Vee - 26 V	V <sub>O</sub> = 0.9 V or 2.1 V			±10		
loz		V <sub>CC</sub> = 3.6 V	V <sub>O</sub> = 0 or 3.6 V			±10	- μΑ	
		No. 0.6.V	$V_{I} = 2.1 V \text{ or } 0.9 V, I_{O} = 0$		$V_{\rm I} = 2.1  \text{V} \text{ or } 0.9  \text{V},  I_{\rm O} = 0$		90	
ICC		V <sub>CC</sub> = 3.6 V	$V_{I} = 3.6 V \text{ or } 0, \qquad I_{O} = 0$	90		90	- mA	
<u>.</u>	Control pin	Vac. 22V	VI = 2.1 V or 0.9 V				-5	
Ci	A port	V <sub>CC</sub> = 3.3 V	v] = 2.1 v or 0.9 v				pF	
CO	Y port	V <sub>CC</sub> = 3.3 V	V <sub>O</sub> = 2.1 V or 0.9 V				pF	

<sup>†</sup> All typical values are at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}$ C.



#### SN74SSTL16837 20-BIT SSTL\_3 INTERFACE UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS SCB5675 - SEPTEMBER 1996



- G. tpzL and tpzH are the same as ten.
- H. tpHI and tpI H are the same as  $t_{pd}$ .
  - PHL and PLH are the same as tpg.





#### SN74ALVCH16827 20-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS SCES041A - JULY 1995 - REVISED NOVEMBER 1996

<ul> <li>Member of the Texas Instruments Widebus ™ Family</li> </ul>	DGG OR DL PACKAGE (TOP VIEW)		
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>	10E1		10E2
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds</li> </ul>	1Y1 1Y2	3 54	1A1 1A2
200 V Using Machine Model (C = 200 pF, R = 0)	GND 1Y3		GND 1A3
Latch-Up Performance Exceeds 250 mA	1Y4 [ V <sub>CC</sub> [	6 51	] 1A4 ] V <sub>CC</sub>
<ul> <li>Per JEDEC Standard JESD-17</li> <li>Bus Hold on Data Inputs Eliminates the</li> </ul>	1Y5 ( 1Y6 (	8 49	1A5 1A6
Need for External Pullup/Pulldown Resistors	1Y7 GND	10 47	I 1A7 GND
<ul> <li>Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink</li> </ul>	1Y8 1Y9	12 45	1A8 1A9
Small-Outline (DGG) Packages	1Y10 🛛	14 43	1A10
description	2Y1 2Y2	16 41	2A1 2A2
This 20-bit non-inverting buffer/driver is designed for 2.3-V to 3.6-V $V_{CC}$ operation.	2Y3 GND	18 39	2A3 GND
The SN74ALVCH16827 is composed of two 10-bit	2Y4 2Y5	20 37	2A4 2A5
sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable	2Y6 [ V <sub>CC</sub> [		2A6 V <sub>CC</sub>
$(1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$ ) inputs must both be low for the corresponding Y outputs to be	2Y7 [ 2Y8 [	23 34	2A7 2A8
active. If either output-enable input is high, the	GND		GND

high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

outputs of that 10-bit buffer section are in the

2Y6		36 🛛 2A6
V <sub>CC</sub>	22	35 🛛 V <sub>CC</sub>
2Y7	23	34 🛛 2A7
2Y8	24	33 🛛 2A8
GND	25	32 🛿 GND
2Y9	26	31 🛛 2A9
2Y10	27	30 🛛 2A10
20E1	28	29 20E2

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16827 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16827 is characterized for operation from -40°C to 85°C.

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#### SN74ALVCH16827 20-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS SCES041A - JULY 1995 - REVISED NOVEMBER 1996

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 4.6 V
Input voltage range, V <sub>1</sub> (see Note 1)	–0.5 V to 4.6 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	–0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, IIK (VI < 0)	
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3)	: DGG package 1 W
	DL package 1.4 W
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.*

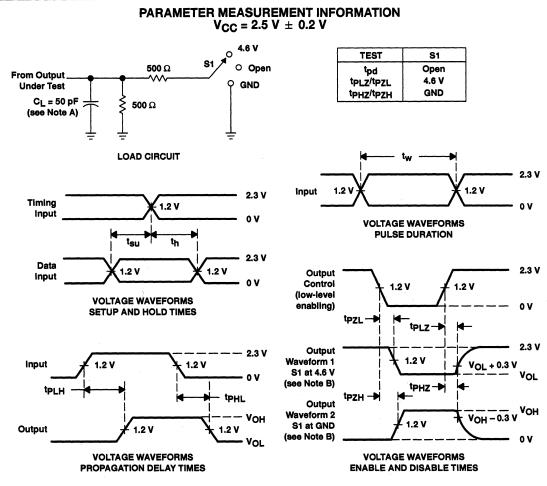
#### recommended operating conditions (see Note 4)

	· · · · · · · · · · · · · · · · · · ·		MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	v
V		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v
VIH	High-level input voltage V <sub>CC</sub> = 2.7 V to 3.6 V	2		v	
N.,	$V_{\rm CC} = 2.3$ V to 2	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	v
VIL	Low-level input voltage V <sub>CC</sub> = 2.7 V to 3.6 V			0.8	v
٧I	Input voltage		0	Vcc	v
Vo	Output voltage		0	Vcc	v
	High-level output current	V <sub>CC</sub> = 2.3 V		-12	mA
ЮН		V <sub>CC</sub> = 2.7 V		-12	
		$V_{CC} = 3 V$		24	
		V <sub>CC</sub> = 2.3 V		12	
IOL	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
		V <sub>CC</sub> = 3 V		24	
∆t/∆v	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



# SN74ALVCH16827 20-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS





NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , tr  $\leq$  2.5 ns, tr  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpi H and tpHi are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



### SN74ALVCH162827 20-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES013B - JULY 1995 - REVISED DECEMBER 1996

<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	DGG OR DL (TOP )	
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>		56 10E2
<ul> <li>Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required</li> </ul>	1Y2 3 GND 4	54 1A2 53 GND
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)</li> </ul>	1Y3 5 1Y4 6 V <sub>CC</sub> 7 1Y5 8	52 1A3 51 1A4 50 V <sub>CC</sub> 49 1A5
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	1Y6 9 1Y7 10 GND 11	48 1A6 47 1A7 46 GND
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	1Y8 [] 12 1Y9 [] 13 1Y10 [] 14	45 1A8 44 1A9 43 1A10
<ul> <li>Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages</li> </ul>	2Y1 15 2Y2 16 2Y3 17	42 2A1 41 2A2 40 2A3
description	GND 18 2Y4 19 2Y5 20	39 GND 38 2A4 37 2A5
This 20-bit noninverting buffer/driver is designed for 2.3-V to 3.6-V $V_{CC}$ operation.	2Y6 21 V <sub>CC</sub> 22	36 2A6 35 V <sub>CC</sub>
The SN74ALVCH162827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (10E1 and 10E2 or 20E1 and	2Y7 23 2Y8 24 GND 25 2Y9 26	34 2A7 33 2A8 32 GND 31 2A9
20E2) inputs must both be low for the corresponding Y outputs to be active. If either	2Y10 27 2V10 27 2OE1 28	30 2A10 29 2OE2

The outputs, which are designed to sink up to 12 mA, include 26- $\Omega$  resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162827 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH162827 is characterized for operation from -40°C to 85°C.

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output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance

state.

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#### SN74ALVCH162827 **20-BIT BUFFER/DRIVER** WITH 3-STATE OUTPUTS SCES013B - JULY 1995 - REVISED DECEMBER 1996

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, IIK (VI < 0)	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air): DGG package	1 W
DL package	
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

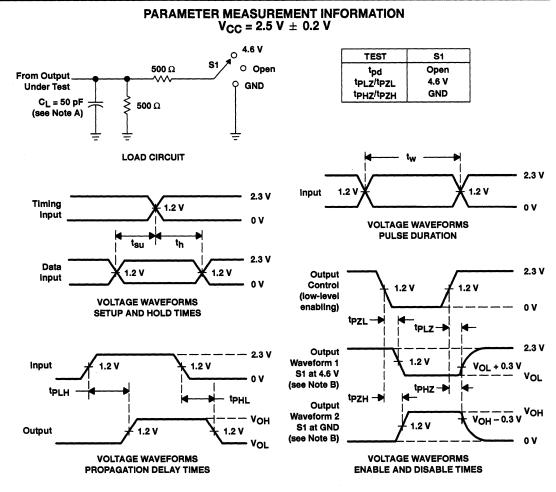
- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
V	High lovel input veltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v
VIH	High-level input voltage V <sub>CC</sub> = 2.7 V to 3.6 V	2		v	
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	v	
VIL	Low-level input voltage V <sub>CC</sub> = 2.7 V to 3.6 V			0.8	v
٧I	Input voltage	· · ·	0	VCC	V
Vo	Output voltage		0	VCC	v
	High-level output current	V <sub>CC</sub> = 2.3 V		-þ	mA
ЮН		V <sub>CC</sub> = 2.7 V		<del>ا</del>	
		$V_{CC} = 3 V$		-12	
		V <sub>CC</sub> = 2.3 V		6	mA
IOL	Low-level output current	V <sub>CC</sub> = 2.7 V		8	
		V <sub>CC</sub> = 3 V		12	
∆t/∆v	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		40	85	°C



#### SN74ALVCH162827 **20-BIT BUFFER/DRIVER** WITH 3-STATE OUTPUTS SCES013B - JULY 1995 - REVISED DECEMBER 1996



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \le 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \le 2.5 \text{ ns}$ ,  $t_f \le 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



### SN74ALVCH16841 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES043A - JULY 1995 - REVISED NOVEMBER 1996

31 **2**209

29 🛛 2LE

30 **D** 2D10

2Q9 1 26

2Q10 27

20E 28

● Member of the Texas Instruments Widebus™ Family		OR DL PACI (TOP VIEW)	
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>			L 1LE
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	1Q1 1Q2 GND	3 54	1D1 1D2 GND
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method3015; Exceeds</li> </ul>	1Q3 1Q4	5 52	1D3 1D4
200 V Using Machine Model (C = 200 pF, R = 0)	V <sub>CC</sub>	7 50	V <sub>CC</sub>
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown</li> </ul>	1Q6 1Q7	9 48 10 47	1D6 1D7
<ul> <li>Resistors</li> <li>Package Options Include Plastic 300-mil</li> </ul>	GND 1Q8	12 45	GND 1D8
Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages	1Q9 [ 1Q10 ]	14 43	1D9 1D10
description	2Q1 2Q2	16 41	2D1 2D2
This 20-bit bus-interface D-type latch is designed for 2.3-V to 3.6-V $V_{CC}$ operation.	2Q3 GND	18 39	2D3 GND 2D4
The SN74ALVCH16841 features 3-state outputs designed specifically for driving highly capacitive	2Q4 2Q5 2Q6	20 37	2D4 2D5 2D6
or relatively low-impedance loads. This device is particularly suitable for implementing buffer	200 V <sub>CC</sub> 207	22 35	V <sub>CC</sub> 2D7
registers, unidirectional bus drivers, and working registers.	2Q8 2Q8 GND	24 33	2D7 2D8 GND
		•	<b>n</b>

The SN74ALVCH16841 can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true

data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (10E or 20E) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output-enable (OE) input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16841 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16841 is characterized for operation from -40°C to 85°C.

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

	ev
Supply voltage range, V <sub>CC</sub> 0.5 V to 4	
Input voltage range, V <sub>1</sub> (see Note 1)	.6 V
Output voltage range, $V_O$ (see Notes 1 and 2)0.5 V to $V_{CC}$ + 0	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	mΑ
Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> ) ±50	
Continuous output current, $I_O$ (V <sub>O</sub> = 0 to V <sub>CC</sub> ) ±50	mΑ
Continuous current through each V <sub>CC</sub> or GND	mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG package	1 W
DL package	
Storage temperature range, T <sub>stg</sub> 65°C to 15	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		2.3	3.6	V	
<b>V</b>	High-level input voltage         V <sub>CC</sub> = 2.3 V to 2.7 V           V <sub>CC</sub> = 2.7 V to 3.6 V	1.7		v		
ViH		2		v		
VIL	V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v	
VIL .	Low-level input voltage V <sub>CC</sub> = 2.7 V to 3.6 V			0.8	v	
٧I	Input voltage		0	VCC	V	
Vo	Output voltage		0	VCC	V	
,	High-level output current	V <sub>CC</sub> = 2.3 V		-12		
юн		V <sub>CC</sub> = 2.7 V		-12	mA	
		V <sub>CC</sub> = 3 V		-24		
		V <sub>CC</sub> = 2.3 V		12	12	
IOL	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA	
	·	V <sub>CC</sub> = 3 V		24		
∆t/∆v	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	



#### SN74ALVCH16841 **20-BIT BUS-INTERFACE D-TYPE LATCH** WITH 3-STATE OUTPUTS SCES043A - JULY 1995 - REVISED NOVEMBER 1996

# timing requirements over recommended ranges of supply voltage and operating free-air temperature, (unless otherwise noted) (see Figures 1 and 2)

	PARAMETER		2.5 V 2 V	V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
tw	Pulse duration, LE high or low	3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before LE↑	0.9		0.7		1.1		ns
th	Hold time, data after LE↑	1.2		1.5		1.1		ns

# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figures 1 and 2)

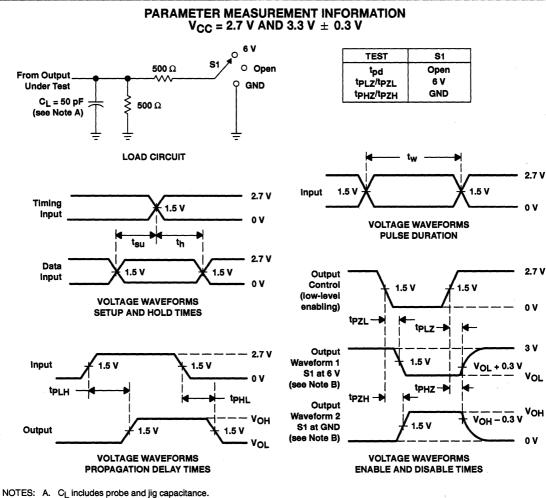
PARAMETER	FROM TO (INPUT) (OUTPUT)		V <sub>CC</sub> = ± 0.	2.5 V 2 V	V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = ± 0.3	3.3 V 3 V	UNIT
	(INFOT)	(001F01)	MIN	MAX	MIN	MAX	MIN	MAX	
· .	D	Q	1.1	5.6		4.7	1.2	3.9	
<sup>t</sup> pd	LE	Q	1	6.2		5.1	1	4.3	ns
ten	ŌĒ	Q	1	6.7		6	1	4.9	ns
<sup>t</sup> dis	ŌĒ	Q	1.8	5.5		4.3	1.3	4.1	ns

### operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT	
				TYP	TYP	
C .	Power dissipation capacitance $\begin{array}{c} \text{Outputs enabled} \\ \text{Outputs disabled} \end{array}$ C <sub>L</sub> = 50 pF, f = 10 M	Outputs enabled		12	20	рF
Cpd		Outputs disabled	OL = 50 pr, T = 10 MHZ	1	3	рг



#### SN74ALVCH16841 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS SCES043A - JULY 1995 - REVISED NOVEMBER 1996



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , tr  $\leq$  2.5 ns, tr  $\leq$  2.5 ns,
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHI are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms



#### SN74ALVCH16721 3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS SCES052A - JULY 1995 - REVISED NOVEMBER 1996

<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	DGG OR DL PACKAGE (TOP VIEW)
<ul> <li>EPIC ™ (Enhanced-Performance Implant CMOS) Submicron Process</li> </ul>	ed OE 1 56 CLK Q1 2 55 D1
• ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds	Q2 [] 3 54 ] D2 Q2 [] 3 54 ] D2 GND [] 4 53 ] GND
200 V Using Machine Model (C = 200 pF, R = 0)	Q3 [ 5 52 ] D3 Q4 [ 6 51 ] D4
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	
Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown	Q6 [] 9 48 [] D6 Q7 [] 10 47 [] D7
<ul> <li>Resistors</li> <li>Package Options Include Plastic 300-mil</li> </ul>	GND 0 11 46 0 GND Q8 0 12 45 0 D8
Shrink Small-Outline (DL) and Thin Shrin Small-Outline (DGG) Packages	nk Q9 [] 13 44 ]] D9 Q10 [] 14 43 ]] D10
description	Q11 [] 15 42 ] D11 Q12 [] 16 41 [] D12
This 20-bit flip-flop is designed specifically $2.3-V$ to $3.6-V$ V <sub>CC</sub> operation.	
The SN74ALVCH16721 20 flip-flops are e triggered D-type flip-flops with qualified of	·
storage. On the positive transition of the c (CLK) input, the device provides true data a	clock V <sub>CC</sub> [22 35] V <sub>CC</sub>

Q outputs if the clock-enable (CLKEN) input is low. If CLKEN is high, no data is stored.

A buffered output-enable (OE) input places the 20 outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive

GND 25	32	GND				
Q19 🛛 26		D19				
Q20 27		D20				
NC 28	29	CLKEN				
NC - No internal connection						

33 🛛 D18

Q18 24

provide the capability to drive bus lines without need for interface or pullup components. OE does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16721 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16721 is characterized for operation from -40°C to 85°C.

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# SN74ALVCH16721 3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS SCES052A - JULY 1995 - REVISED NOVEMBER 1996

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
	High-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	1	v
VIH		$V_{CC} = 2.7 V \text{ to } 3.6 V$	2		
	Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	v
VIL		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	
VI	Input voltage		0	Vcc	v
Vo	Output voltage		0	VCC	V
	High-level output current	V <sub>CC</sub> = 2.3 V		-12	mA
юн		V <sub>CC</sub> = 2.7 V	-	-12	
		V <sub>CC</sub> = 3 V		-24	
	Low-level output current	V <sub>CC</sub> = 2.3 V		12	mA
IOL		V <sub>CC</sub> = 2.7 V		12	
		V <sub>CC</sub> = 3 V		24	
∆t/∆v	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

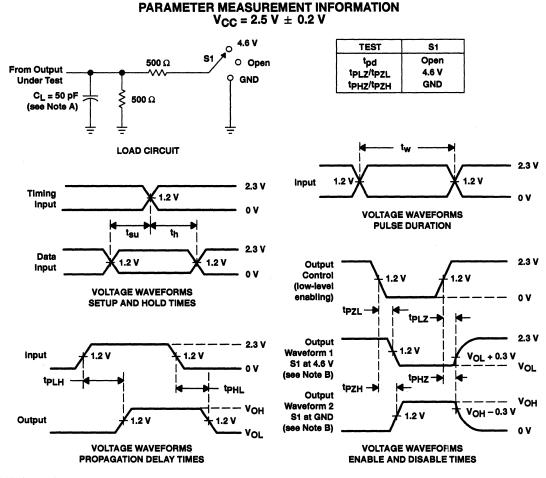
#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	RAMETER	TEST CO	ONDITIONS	Vcc	MIN	TYPT	MAX	UNIT
		I <sub>OH</sub> = -100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -0.	2		
		I <sub>OH</sub> = -6 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	2			
		I <sub>OH</sub> = -12 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	1.7			v
VOH		I <sub>OH</sub> = -12 mA,	V <sub>IH</sub> = 2 V	2.7 V	2.2			v
		I <sub>OH</sub> = -12 mA,	V <sub>IH</sub> = 2 V	3 V	2.4			
		I <sub>OH</sub> = -24 mA,	V <sub>IH</sub> = 2 V	3 V	2			
		l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V			0.2	
		I <sub>OL</sub> = 6 mA,	VIL = 0.7 V	2.3 V			0.4	v
VOL		I <sub>OL</sub> = 12 mA,	V <sub>IL</sub> = 0.7 V	2.3 V			0.7	
		I <sub>OL</sub> = 12 mA,	V <sub>IL</sub> = 0.8 V	2.7 V			0.4	
		I <sub>OL</sub> = 24 mA,	V <sub>IL</sub> = 0.8 V	3 V			0.55	
ų		VI = VCC or GND		3.6 V			±5	μA
lı(hold)		V <sub>1</sub> = 0.7 V		2.3 V	45			
		V <sub>I</sub> = 1.7 V			-45			
		V <sub>1</sub> = 0.8 V			75		μA	
		V <sub>I</sub> = 2 V		3V	-75			
		V <sub>I</sub> = 0 to 3.6 V <sup>‡</sup>		3.6 V			±500	
loz		V <sub>O</sub> = V <sub>CC</sub> or GND		3.6 V			±10	μA
Icc		V <sub>I</sub> = V <sub>CC</sub> or GND,	IO = 0	3.6 V			40	μA
∆ICC		One input at V <sub>CC</sub> - 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA
	Control inputs	V V 0ND	Maria Manana Manana ang kanang ka	3.3 V		3.5		_
Ci	Data inputs	VI = V <sub>CC</sub> or GND				6		pF
Cio	Data inputs	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V	1	7		pF

<sup>†</sup> Typical values are measured at V<sub>CC</sub> = 3.3 V,  $T_A$  = 25°C. <sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.



#### SN74ALVCH16721 3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS SCES052A - JULY 1995 - REVISED NOVEMBER 1996



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl z and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- PLH and PHL are the same as the.

#### Figure 1. Load Circuit and Voltage Waveforms



# SN74ALVCH162721 3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

SCES055A - DECEMBER 1995 - REVISED NOVEMBER 1996

<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	DGG OR DL PACKAGE (TOP VIEW)				
<ul> <li>EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>					
<ul> <li>Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required</li> </ul>	Q1 2 55 D1 Q2 3 54 D2 GND 4 53 GND Q3 5 52 D3				
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)</li> </ul>	$\begin{array}{cccccccccccccccccccccccccccccccccccc$				
<ul> <li>Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17</li> </ul>	Q7 0 10 47 0 D7 GND 0 11 46 0 GND				
<ul> <li>Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors</li> </ul>	Q8 12 45 D8 Q9 13 44 D9 Q10 14 43 D10				
<ul> <li>Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages</li> </ul>	Q11 [ 15 42 ] D11 Q12 [ 16 41 ] D12 Q13 [ 17 40 ] D13 Q13 [ 17 40 ] D13				
description	GND   18 39   GND Q14   19 38   D14				
This 20-bit flip-flop is designed for low-voltage 2.3-V to 3.6-V V <sub>CC</sub> operation.	Q15 20 37 D15 Q16 21 36 D16 V <sub>CC</sub> 22 35 V <sub>CC</sub>				
The 20 flip-flops are edge-triggered D-type flip-flops with qualified clock storage. On the	V <sub>CC</sub> 22 35 V <sub>CC</sub> Q17 23 34 D17 Q18 24 33 D18				

lops with qualified clock s positive transition of the clock (CLK) input, the device provides true data at the Q outputs if the clock-enable (CLKEN) input is low. If CLKEN is high, no data is stored.

A buffered output-enable (OE) input places the 20 outputs in either a normal logic state (high or low level) or the high-impedance state. In the

high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components. OE does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

The outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

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NC - No internal connection

32 GND

31 D19

30 D20

29 CLKEN

Q19 26 Q20 27 NC 28

GND 25

#### SN74ALVCH162721 3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS SCES055A – DECEMBER 1995 – REVISED NOVEMBER 1996

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

*	
Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>1</sub> (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	–0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, IIK (VI < 0)	
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	
Continuous output current, $I_{O}$ (V <sub>O</sub> = 0 to V <sub>CC</sub> )	
Continuous current through each V <sub>CC</sub> or GND	
Maximum power dissipation at $T_{A} = 55^{\circ}C$ (in still air) (see Note 3): DGG particularly between the transmission of transmission of the transmission of transmission	
	age 1.4 W
Storage temperature range, T <sub>sto</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage			3.6	v	
VIH	High-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		v	
		V <sub>CC</sub> = 2.7 V to 3.6 V	2			
	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	v	
VIL		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	v	
VI	Input voltage		0	Vcc	V	
Vo	Output voltage		0	Vcc	V	
	High-level output current	V <sub>CC</sub> = 2.3 V		4	mA	
ЮН		V <sub>CC</sub> = 2.7 V		-8		
		V <sub>CC</sub> = 3 V		-12		
	Low-level output current	V <sub>CC</sub> = 2.3 V		6	mA	
IOL		V <sub>CC</sub> = 2.7 V		8		
		V <sub>CC</sub> = 3 V		12		
∆t/∆v	Input transition rise or fall rate	,	0	10	ns/V	
Τ <sub>Α</sub>	Operating free-air temperature		-40	85	°C	



#### SN74ALVCH162721 3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS SCES055A – DECEMBER 1995 – REVISED NOVEMBER 1996

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 and 2)

				V <sub>CC</sub> = 2.5 V ± 0.2 V		2.7 V	V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency			150	0	150	0	150	MHz	
tw	Pulse duration, CLK high or low		3.3		3.3		3.3		ns	
	Catura Airma	Data before CLK↑	4		3.6		3.1		ns	
t <sub>su</sub>	Setup time	CLKEN before CLK1	3.4		3.1		2.7			
	Hold time	Data after CLK↑	0		0		0			
<sup>t</sup> h		CLKEN after CLK1	0		0		0		ns	

# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figures 1 and 2)

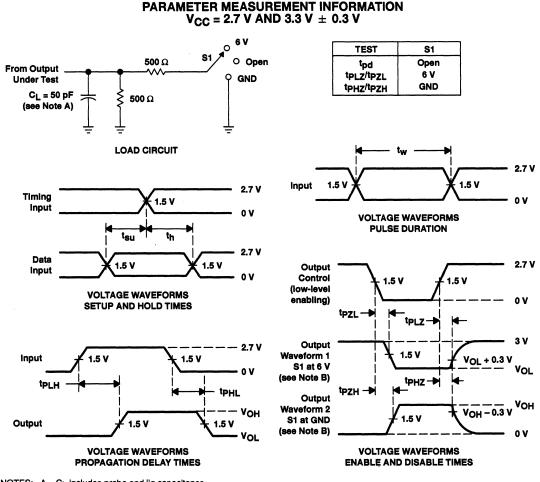
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1	2.5 V 2 V	V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = ± 0.3	3.3 V 3 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
fmax			150		150		150		MHz
<sup>t</sup> pd	CLK	Q	1	7.5		6.4	1	5.5	ns
ten	ŌĒ	Q	1	7.9		7.2	1	6	ns
<sup>t</sup> dis	ŌĒ	Q	· 1	6.7		5.6	1	5.2	ns

## operating characteristics, T<sub>A</sub> = 25°C

	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT	
			TYP	TYP		
	Power dissipation capacitance	Outputs enabled		55	59	pF
Cpd	Power dissipation capacitance	Outputs disabled	C <sub>L</sub> = 50 pF, f = 10 MHz	46	49	рг



#### SN74ALVCH162721 3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS SCES055A - DECEMBER 1995 - REVISED NOVEMBER 1996



- NOTES: A. CL includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLZ and tpHZ are the same as tdis.
  - F. tp71 and tp7H are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - . IPLH and IPHL are the same as Ipd.

Figure 2. Load Circuit and Voltage Waveforms



### SN74ALVCH16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES037A - JULY 1995 - REVISED NOVEMBER 1996

<ul> <li>Member of the Texas Instruments</li> <li>Widebus™ Family</li> </ul>	DGG OR DL (TOP V	
<ul> <li>EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process</li> </ul>		56 1CLK
ESD Protection Exceeds 2000 V Per	1Q2 <b>[</b> 3	54 1D2
MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model		53 GND
(C = 200 pF, R = 0)	1Q3 5 1Q4 6	52 1D3 51 1D4
Latch-Up Performance Exceeds 250 mA		50 V <sub>CC</sub>
Per JEDEC Standard JESD-17	1Q5 🛛 8	49 1D5
<ul> <li>Bus Hold on Data Inputs Eliminates the</li> </ul>	1Q6 🛿 9	48 🛛 1D6
Need for External Pullup/Pulldown	1Q7 🚺 10	47 <b>]</b> 1D7
Resistors	GND 🚺 11	46 🛛 GND
<ul> <li>Package Options Include Plastic 300-mil</li> </ul>	1Q8 🛛 12	45 <b>]</b> 1D8
Shrink Small-Outline (DL) and Thin Shrink	1Q9 🛛 13	44 1D9
Small-Outline (DGG) Packages	1Q10 14	43 1D10
• • • •	2Q1 15	42 2D1
description	2Q2 16	41 2D2
This 20-bit bus-interface flip-flop is designed for	2Q3 17	40 2D3
2.3-V to 3.6-V $V_{CC}$ operation.	GND [] 18 2Q4 [] 19	39 GND 38 2D4
	2Q4 [ 19 2Q5 [ 20	37 2D4
The SN74ALVCH16821 can be used as two 10-bit	2Q6 21	36 2D6
flip-flops or one 20-bit flip-flop. The 20 flip-flops are edge-triggered D-type flip-flops. On the	V <sub>CC</sub> [ 22	35 V <sub>CC</sub>
positive transition of the clock (CLK) input, the	207 23	34 2D7
device provides true data at the Q outputs.	2Q8 24	33 2D8
· · · ·	GND 25	32 GND
A buffered output-enable (OE) input can be	2Q9 🛛 26	31 2D9

used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

2Q10 🛛 27

20E 28

30 12D10

2CLK

29

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16821 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16821 is characterized for operation from -40°C to 85°C.

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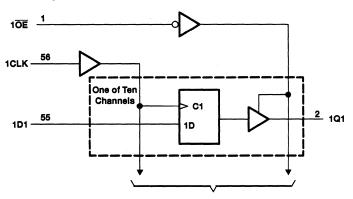
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



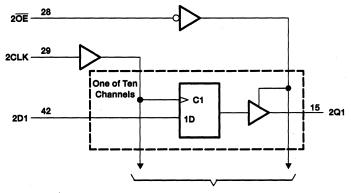
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# SN74ALVCH16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCES037A - JULY 1995 - REVISED NOVEMBER 1996

## logic diagram (positive logic)



**To Nine Other Channels** 



**To Nine Other Channels** 



# SN74ALVCH16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCES037A - JULY 1995 - REVISED NOVEMBER 1996

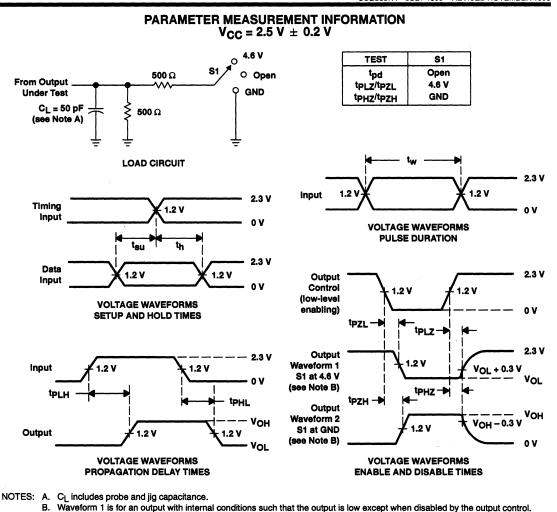
P	ARAMETER	TEST	CONDITIONS	Vcc	MIN	түрт	MAX	UNIT	
		I <sub>OH</sub> = -100 μA		2.3 V to 3.6 V	V <sub>CC</sub> -0.2	2			
		I <sub>OH</sub> = -6 mA,	VIH = 1.7 V	2.3 V	2				
VOH			V <sub>IH</sub> = 1.7 V	2.3 V	1.7			v	
⊻ОН		I <sub>OH</sub> = -12 mA	V <sub>IH</sub> = 2 V	2.7 V	2.2			v	
			V <sub>IH</sub> = 2 V	3 V	2.4				
		I <sub>OH</sub> = -24 mA,	V <sub>IH</sub> = 2 V	3 V	2				
		l <sub>OL</sub> = 100 μA		2.3 V to 3.6 V			0.2		
		l <sub>OL</sub> = 6 mA,	V <sub>IL</sub> = 0.7 V	2.3 V			0.4	1	
VOL		I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 V	2.3 V	2.3 V		0.7	v	
			V <sub>IL</sub> = 0.8 V	2.7 V			0.4		
		l <sub>OL</sub> = 24 mA,	VIL = 0.8 V	3 V			0.55		
lj –		VI = V <sub>CC</sub> or GND		3.6 V			±5	μA	
		V <sub>I</sub> = 0.7 V		0.01/	45				
		V <sub>I</sub> = 1.7 V		- 2.3 V	45				
li(hold	)	V <sub>I</sub> = 0.8 V		0.1/	75			μA	
		VI = 2 V		- 3V	-75				
		$V_1 = 0$ to 3.6 V <sup>‡</sup>		3.6 V			±500		
loz		V <sub>O</sub> = V <sub>CC</sub> or GND	······································	3.6 V			±10	μA	
ICC		VI = V <sub>CC</sub> or GND,	IO = 0	3.6 V			40	μA	
∆ICC		One input at V <sub>CC</sub> – 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA	
0	Control inputs			0.014		3.5		-5	
Ci	Data inputs	VI = V <sub>CC</sub> or GND		3.3 V		6		pF	
Co	Outputs	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V		7		pF	

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<sup>†</sup> All typical values are measured at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C. <sup>‡</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.



#### SN74ALVCH16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCES037A - JULY 1995 - REVISED NOVEMBER 1996



- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl z and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

#### Figure 1. Load Circuit and Voltage Waveforms



General Information	1
Data Transceivers/Multiplexers	2
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CDC509 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS576A – JULY 1996 – REVISED OCTOBER 1996

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- Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications
- Distributes One Clock Input to One Bank of Five and One Bank of Four Outputs
- Separate Output Enable for Each Output Bank
- External Feedback (FBIN) Pin Is Used to Synchronize the Outputs to the Clock Input
- No External RC Network Required
- Operates at 3.3-V V<sub>CC</sub>
- Packaged in Plastic 24-Pin Thin Shrink Small-Outline Package

•	PW PACKAGE (TOP VIEW)									
•	1 2 3 4 5 6 7 8	24 23 22 21 20 19 18 17	E CLK AV <sub>CC</sub> 2Y0 2Y1 GND GND 2Y2 2Y3							
V <sub>CC</sub> 1G FBOUT	10 11	15	V <sub>CC</sub> 2G FBIN							
10001	12	13								

#### description

The CDC509 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDC509 operates at 3.3-V  $V_{CC}$  and is designed to drive up to five clock loads per output.

One bank of five outputs and one bank of four outputs provide nine low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. Each bank of outputs can be enabled or disabled separately via the control (1G and 2G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CDC509 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC509 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping  $AV_{CC}$  to ground.

The CDC509 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE									
	INPUTS	5		OUTPU	rs				
1G	1G 2G CLK			2Y (0:3)	FBOUT				
X	х	L	L	L	L				
L	L	н	L	L	н				
L	н	н	L	н	Ъ				
н	L	н	н	L	н				
н	н	н	н	н	н				

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#### CDC509 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS576A – JULY 1996 – REVISED OCTOBER 1996

#### **Terminal Functions**

TERMINAL NAME NO.		TYPE	
		ITPE	DESCRIPTION
CLK	24	1	Clock input. CLK provides the clock signal to be distributed by the CDC509 clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
1G	11	I	Output bank enable. 1G is the output enable for outputs 1Y(0:4). When 1G is low, outputs 1Y(0:4) are disabled to a logic-low state. When 1G is high, all outputs 1Y(0:4) are enabled and switch at the same frequency as CLK.
2G	14	1	Output bank enable. 2G is the output enable for outputs 2Y(0:3). When 2G is low, outputs 2Y(0:3) are disabled to a logic low state. When 2G is high, all outputs 2Y(0:3) are enabled and switch at the same frequency as CLK.
FBOUT	12	0	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL.
1Y(0:4)	3, 4, 5, 8, 9	0	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:4) is enabled via the 1G input. These outputs can be disabled to a logic-low state by deasserting the 1G control input.
2Y(0:3)	16, 17, 20 21	0	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 2Y(0:3) is enabled via the 2G input. These outputs can be disabled to a logic-low state by deasserting the 2G control input.
AV <sub>CC</sub>	23	Power	Analog power supply. AV <sub>CC</sub> provides the power reference for the analog circuitry. In addition, AV <sub>CC</sub> can be used to bypass the PLL for test purposes. When AV <sub>CC</sub> is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
VCC	2, 10, 15, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

	-
Supply voltage range, V <sub>CC</sub>	
Input voltage range, VI (see Note 1)	
Voltage range applied to any output in the high-impedance state	
or power-off state, VO (see Note 1)	
Voltage range applied to any output in the high	
or low state, V <sub>O</sub> (see Notes 1 and 2)	–0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3)	0.7 W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

 The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book, literature number SCBD002.



#### CDC509 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS576A – JULY 1996 – REVISED OCTOBER 1996

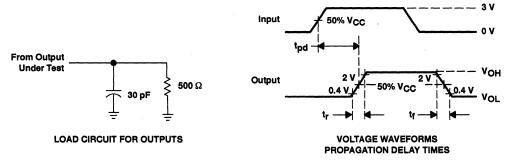
# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 30 \text{ pF}$ (see Note 5 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 3.3 V ± 0.165 V		V <sub>CC</sub> = 3.3 V ± 0.3 V	
	(INPOT)	(001901)	MIN	MAX	MIN	MAX	
<sup>t</sup> phase error <sup>†</sup>	CLKIN↑	FBIN↑			-150	150	ps
<sup>t</sup> sk(o) <sup>†</sup>	Any Y or FBOUT	Any Y or FBOUT				250	ps
Jitter(pk-pk)		Any Y or FBOUT			-100	100	ps
Duty cycle		Any Y or FBOUT			45%	55%	
tr		Any Y or FBOUT	0.4	1.6	0.5	2	ns
tf		Any Y or FBOUT	0.4	1.6	0.5	2	ns

<sup>†</sup> The t<sub>sk(0)</sub> specification is only valid for equal loading of all outputs.

NOTE 5: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. CL includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z<sub>O</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns,
  - C. The outputs are measured one at a time with one transition per measurement.

#### Figure 1. Load Circuit and Voltage Waveforms

**PRODUCT PREVIEW** 

#### CDC2509 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS560 - OCTOBER 1996

PW PACKAGE (TOP VIEW)

V<sub>CC</sub> [] 2

1Y0 3

1Y1 4

1Y2 🛛 5

GND 6

GND 17

1Y3 🛛 8

1Y4 🛛 9

V<sub>CC</sub> [] 10

1G 🛛 11

FBOUT 12

24 CLK

23 AV<sub>CC</sub>

22 🛛 V<sub>CC</sub>

21 2Y0

20 **1** 2Y1

19 GND

18 GND

17 2Y2

16 🛛 2Y3

15 VCC

13 **FBIN** 

14 2G

- Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications
- Distributes One Clock Input to One Bank of Five and One Bank of Four Outputs
- Separate Output Enable for Each Output Bank
- External Feedback (FBIN) Pin Is Used to Synchronize the Outputs to the Clock Input
- On-Chip Series Damping Resistors
- No External RC Network Required
- Operates at 3.3-V V<sub>CC</sub>
- Packaged in Plastic 24-Pin Thin Shrink Small-Outline Package

### description

The CDC2509 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDC2509 operates at 3.3-V  $V_{CC}$  and provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of five outputs and one bank of four outputs provide nine low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. Each bank of outputs can be enabled or disabled separately via the control (1G and 2G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CDC2509 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC2509 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping  $AV_{CC}$  to ground.

The CDC2509 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE									
	INPUTS	•	OUTPUTS						
1G	2G	CLK	1Y (0:4)	2Y (0:3)	FBOUT				
Х	х	L	L	L	L				
L	L	н	L	L	н				
L	н	н	L	н	н				
н	L	н	н	L	н				
н	н	н	н	н	н				

₹ U



### CDC2509 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS560 - OCTOBER 1996

### **Terminal Functions**

TERMINAL		TYPE	DESORIDITION			
NAME	NAME NO.		DESCRIPTION			
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CDC2509 clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.			
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.			
1G	11	1	Output bank enable. 1G is the output enable for outputs 1Y(0:4). When 1G is low, outputs 1Y(0:4) are disabled to a logic-low state. When 1G is high, all outputs 1Y(0:4) are enabled and switch at the same frequency as CLK.			
2G	14	l	Output bank enable. 2G is the output enable for outputs 2Y(0:3). When 2G is low, outputs 2Y(0:3) are disabled to a logic low state. When 2G is high, all outputs 2Y(0:3) are enabled and switch at the same frequency as CLK.			
FBOUT	12	ο	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has and integrated 25- $\Omega$ series-damping resistor.			
1Y (0:4)	3, 4, 5, 8, 9	ο	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:4) is enabled via the 1G input. These outputs can be disabled to a logic-low state by deasserting the 1G control input. Each output has an integrated $25$ - $\Omega$ series-damping resistor.			
2Y (0:3)	16, 17, 20, 21	ο	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 2Y(0:3) is enabled via the 2G input. These outputs can be disabled to a logic-low state by deasserting the 2G control input. Each output has an integrated $25$ - $\Omega$ series-damping resistor.			
AVCC	23	Power	Analog power supply. AV <sub>CC</sub> provides the power reference for the analog circuitry. In addition, AV <sub>CC</sub> can be used to bypass the PLL for test purposes. When AV <sub>CC</sub> is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.			
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.			
Vcc	2, 10, 15, 22	Power	Power supply			
GND	6, 7, 18, 19	Ground	Ground			



#### CDC2509 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCA5580 - OCTOBER 1996

# timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
fclock	fclock Clock frequency			125	MHz
	Input clock duty cycle		40%	60%	
	Stabilization time <sup>†</sup>	After power up		1	ms

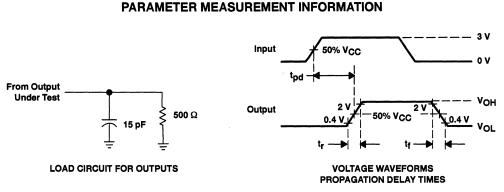
<sup>†</sup> Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 15 \text{ pF}$ (see Note 5 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 3.3 V ± 0.165 V		V <sub>CC</sub> = 3.3 V ± 0.3 V	
	((((-01))	(001F01)	MIN	MAX	MIN	MAX	
<sup>t</sup> phase error <sup>‡</sup>	CLKINÎ	FBIN↑			-150	150	ps
<sup>t</sup> sk(o) <sup>‡</sup>	Any Y or FBOUT	Any Y or FBOUT				250	ps
Jitter(pk-pk)		Any Y or FBOUT			-100	100	ps
Duty cycle		Any Y or FBOUT			45%	55%	
tr		Any Y or FBOUT	0.4	1.6	0.5	2	ns
t <sub>f</sub>		Any Y or FBOUT	0.4	1.6	0.5	2	ns

<sup>‡</sup> The t<sub>sk(0)</sub> specification is only valid for equal loading of all outputs.

NOTE 5: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.



NOTES: A. CL includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z<sub>O</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.

C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



CDC516 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS575 – JULY 1996

- Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications
- Distributes One Clock Input to Four Banks of Four Outputs
- Separate Output Enable for Each Output Bank
- External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input
- No External RC Network Required
- Operates at 3.3-V V<sub>CC</sub>
- Packaged in Plastic 48-Pin Thin Shrink Small-Outline Package

### description

The CDC516 is a high-performance, low-skew, low-jitter, phase-lock loop clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the feedback output (FBOUT) to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDC516 operates at 3.3-V V<sub>CC</sub> and is designed to drive up to five clock loads per output.

Four banks of four outputs provide 16 low-skew, low-jitter copies of the input clock. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at the input clock. Each bank of outputs can be enabled or disabled separately via the 1G, 2G, 3G, and 4G control inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

DGG PACKAGE (TOP VIEW)							
	TOP VI 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21	<b>EW</b> ) 48 47 46 45 44 43 42 41 40 38 37 36 35 34 33 21 30 29 28					
2Y3 [ V <sub>CC</sub> [	23	26	3Y3 V <sub>CC</sub>				

**PRODUCT PREVIEW** 

Unlike many products containing PLLs, the CDC516 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

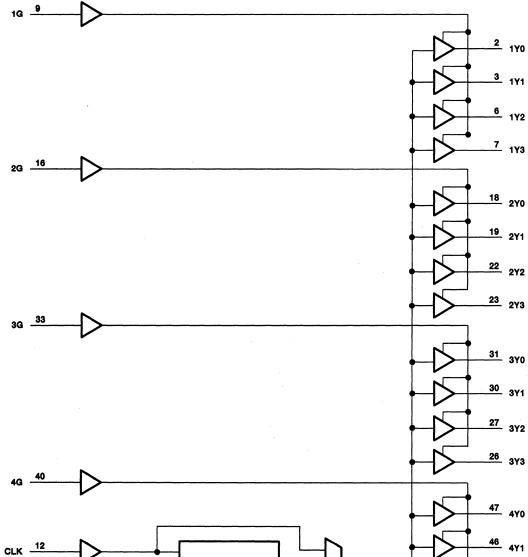
Because it is based on PLL circuitry, the CDC516 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL may be bypassed for test purposes by strapping AV<sub>CC</sub> to ground.

The CDC516 is characterized for operation from 0°C to 70°C.

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## **CDC516** 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS575 - JULY 1996



functional block diagram

FBIN 37

AVCC 11

**PRODUCT PREVIEW** 

2 1Y0

<u>3</u> 1Y1

<u>6</u> 1Y2

7 1Y3



PLL

43 4Y2

42 4Y3

35 FBOUT

#### CDC516 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCA5575 - JULY 1996

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	
Input voltage range, VI (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance state	
or power-off state, V <sub>O</sub> (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, V <sub>O</sub> (see Notes 1 and 2)	–0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, IIK (VI < 0)	
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V <sub>CC</sub> or GND	
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3)	0.85 W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

#### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
Vcc	Supply voltage	3	3.6	v
VIH	High-level input voltage	2		v
VIL	Low-level input voltage		0.8	V
Vj	Input voltage	- 0	Vcc	v
ЮН	High-level output current		-20	mA
lol	Low-level output current		20	mA
TA	Operating free-air temperature	0	70	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	Vcc	MIN	TYP‡	MAX	UNIT
VIK	lj = -18 mA		3 V			-1.2	v
Neu	lOH = -100 μA	MIN to MAX	V <sub>CC</sub> -0.2			v	
VOH	I <sub>ОН</sub> =20 mA		_ 3 V	2.4			v
Ve	l <sub>OL</sub> = 100 μA		MIN to MAX			0.2	v
VOL	I <sub>OL</sub> = 20 mA		3 V			0.55	v
li li	VI = VCC or GND		3.6 V			±5	μA
ICC	VI = V <sub>CC</sub> or GND	IO = 0	3.6 V				mA
AICC	One input at V <sub>CC</sub> – 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3.3 V to 3.6 V			500	μA
Ci	VI = V <sub>CC</sub> or GND		3.3 V		4		pF
Co	VO = VCC or GND		3.3 V		6		pF

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



# **CDC516** 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS575 - JULY 1996

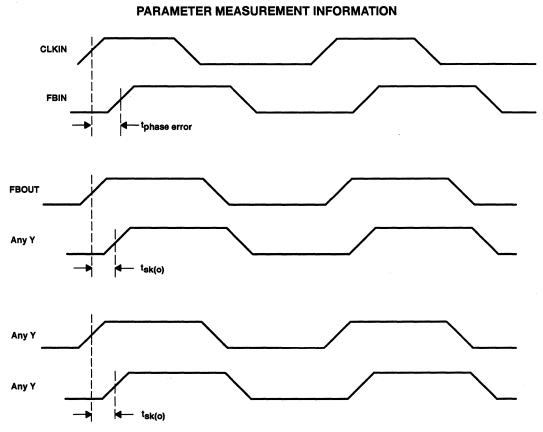


Figure 2. Phase Error and Skew Calculations



**PRODUCT PREVIEW** 

#### CDC2516 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS579 - OCTOBER 1996

DGG PACKAGE

(TOP VIEW)

Vcc.L

1Y0 2

1Y1 🛛 3

GND 4

GND 5

1Y2 16

1Y3 17

V<sub>CC</sub> 8 1G 9

GND 10

AV<sub>CC</sub> 11

AGND 113

AGND 114

GND 115

2G II 16

V<sub>CC</sub> 17

2Y0 118

2Y1 19

GND 120

GND 21

2Y2 222

2Y3 23

V<sub>CC</sub> [24

CLK 112

48 VCC

47 **4**Y0

46 4Y1

45 GND

44 🛛 GND

43 🛛 4Y2

42 4Y3

40 🛛 4G

39 GND

38 AV<sub>CC</sub>

37 FBIN

36 AGND

35 FBOUT

34 GND

33 3G 32 V<sub>CC</sub>

31 3Y0

30 3Y1

29 GND

28 GND

27 3Y2

26 3Y3

25 V<sub>CC</sub>

- Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications
- Distributes One Clock Input to Four Banks of Four Outputs
- Separate Output Enable for Each Output Bank
- External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input
- On-Chip Series-Damping Resistors
- No External RC Network Required
- Operates at 3.3-V V<sub>CC</sub>
- Packaged in Plastic 48-Pin Thin Shrink
   Small-Outline Package

### description

The CDC2516 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback output (FBOUT) to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDC2516 operates at 3.3-V V<sub>CC</sub> and provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

Four banks of four outputs provide 16 low-skew, low-jitter copies of the input clock. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at the input clock. Each bank of outputs can be enabled or disabled separately via the 1G, 2G, 3G, and 4G control inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

an be enabled or disabled	i nës	a <sup>2</sup> e		
2G, 3G, and 4G control	1			a
outs are high, the outputs				
quency with CLK; when the utputs are disabled to the	÷		x - 1	
				1.5.5

Unlike many products containing PLLs, the CDC2516 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC2516 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL may be bypassed for test purposes by strapping AV<sub>CC</sub> to ground.

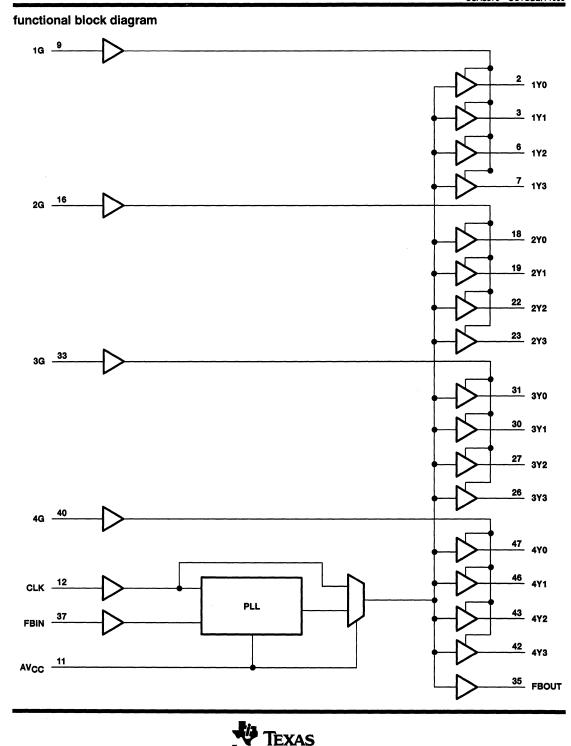
The CDC2516 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinus these products without position.



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### CDC2516 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS579 - OCTOBER 1996



INSTRUMENTS POST OFFICE BOX 655303 • DALLAS, TEXAS 75265 **PRODUCT PREVIEW** 

#### CDC2516 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCA5579 - OCTOBER 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>1</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance state	
or power-off state, V <sub>O</sub> (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, V <sub>O</sub> (see Notes 1 and 2)	–0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ (V <sub>1</sub> < 0)	
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3)	0.85 W
Storage temperature range, T <sub>sto</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
Vcc	Supply voltage	3	3.6	V
VIH	High-level input voltage	2		v
VIL	Low-level input voltage		0.8	v
VI	Input voltage	0	Vcc	v
юн	High-level output current		-12	mA
IOL	Low-level output current		12	mA
TA	Operating free-air temperature	0	70	ç

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	Vcc	MIN	TYP‡	MAX	UNIT
VIK	lj = −18 mA	•	3 V			-1.2	V
	l <sub>OH</sub> = -100 μA	MIN to MAX	V <sub>CC</sub> -0.2			v	
VOH	I <sub>OH</sub> = -12 mA		3 V	2.4			v
V-	l <sub>OL</sub> = 100 μA		MIN to MAX			0.2	
VOL	I <sub>OL</sub> = 12 mA		3 V			0.55	v
ų	V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V			±5	μA
lcc	VI = V <sub>CC</sub> or GND	IO = 0	3.6 V				mA
AICC	One input at V <sub>CC</sub> – 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3.3 V to 3.6 V			500	μA
Ci	VI = V <sub>CC</sub> or GND		3.3 V		4		pF
Co	Vo = V <sub>CC</sub> or GND		3.3 V		6		pF

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



## CDC2516 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS579 - OCTOBER 1996

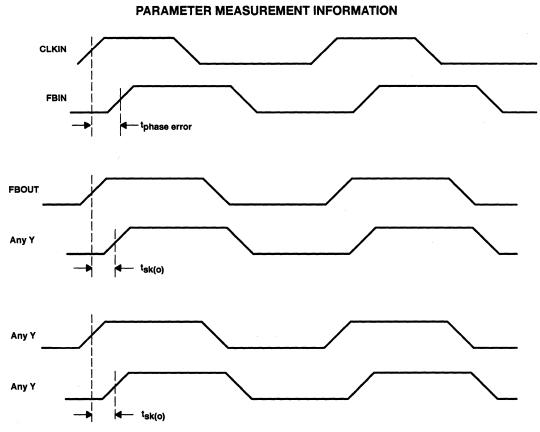


Figure 2. Phase Error and Skew Calculations



**PRODUCT PREVIEW** 

#### CDC536 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS378D – APRIL 1994 – REVISED APRIL 1996

DL PACKAGE

(TOP VIEW)

- Low-Output Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V V<sub>CC</sub>
- Distributes One Clock Input to Six Outputs
- One Select Input Configures Three Outputs to Operate at One-Half or Double the Input Frequency
- No External RC Network Required
- External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input
- Application for Synchronous DRAM, High-Speed Microprocessor
- Negative-Edge-Triggered Clear for Half-Frequency Outputs
- TTL-Compatible Inputs and Outputs
- Outputs Drive 50-Ω Parallel-Terminated Transmission Lines
- State-of-the-Art *EPIC-*II*B*<sup>™</sup> BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V<sub>CC</sub> and Ground Pins Reduce Switching Noise
- Packaged in Plastic 28-Pin Shrink Small Outline Package

#### description

The CDC536 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with synchronous DRAMs and popular microprocessors operating at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. The CDC536 operates at 3.3-V  $V_{CC}$  and is designed to drive a properly terminated 50- $\Omega$  transmission line.

The feedback input (FBIN) is used to synchronize the output clocks in frequency and phase to the input clock (CLKIN). One of the six output clocks must be fed back to FBIN for the PLL to maintain synchronization between CLKIN and the outputs. The output used as the feedback pin is synchronized to the same frequency as CLKIN.

The Y outputs can be configured to switch in phase and at the same frequency as CLKIN. The select (SEL) input configures three Y outputs to operate at one-half or double the CLKIN frequency depending on which pin is fed back to FBIN (see Tables 1 and 2). All output signal duty cycles are adjusted to 50% independent of the duty cycle at the input clock.

Output-enable ( $\overline{OE}$ ) is provided for output control. When  $\overline{OE}$  is high, the outputs are in the high-impedance state. When  $\overline{OE}$  is low, the outputs are active.  $\overline{CLR}$  is negative-edge triggered and can be used to reset the outputs operating at half frequency. TEST is used for factory testing of the device and can be use to bypass the PLL. TEST should be strapped to GND for normal operation.

Unlike many products containing PLLs, the CDC536 does not require external RC networks. The loop filter for the PLL is included on chip, minimizing component count, board space, and cost.

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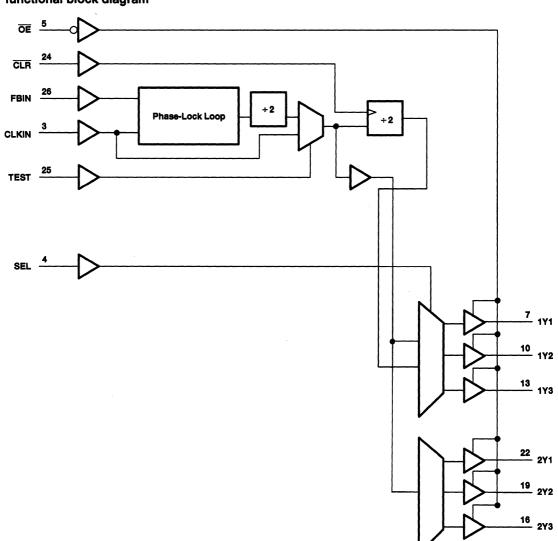


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orporate

AV <sub>CC</sub> [ 1 28 ] AV <sub>CC</sub> AGND [ 2 27 ] AGND CLKIN [ 3 26 ] FBIN SEL [ 4 25 ] TEST OE [ 5 24 ] CLR GND [ 6 23 ] V <sub>CC</sub> 1Y1 [ 7 22 ] 2Y1 V <sub>CC</sub> [ 8 21 ] GND GND [ 9 20 ] V <sub>CC</sub> 1Y2 [ 10 19 ] 2Y2 V <sub>CC</sub> [ 11 18 ] GND GND [ 12 17 ] V <sub>CC</sub> 1Y3 [ 13 16 ] 2Y3 V <sub>CC</sub> [ 14 15 ] GND			,	
	AGND [ CLKIN [ SEL ] GND [ 1Y1 ] V <sub>CC</sub> [ 1Y2 ] V <sub>CC</sub> [ GND ] 1Y2 ] GND [ 1Y3 ]	2 3 4 5 6 7 8 9 10 11 12 13	27 A 26 F 25 T 24 C 23 V 22 2 21 C 20 V 19 2 20 V 19 2 18 C 17 V 16 2	GND EST CC YCC YCC YCC YCC YCC YCC YCC YCC YCC

#### CDC536 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS378D - APRIL 1994 - REVISED APRIL 1996







#### CDC536 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS378D - APRIL 1994 - REVISED APRIL 1996

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ $-0.5$ V to 4.6 VInput voltage range, $V_I$ (see Note 1) $-0.5$ V to 7 VVoltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) $-0.5$ V to 7 VVoltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) $-0.5$ V to 5.5 VCurrent into any output in the low state, $I_O$ $64$ m/Input clamp current, $I_{IK}$ ( $V_I < 0$ ) $-20$ m/Output clamp current, $I_{OK}$ ( $V_O < 0$ ) $-50$ m/Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 2) $0.7$ VOperating free-air temperature range, $T_A$ $0^{\circ}$ C to $70^{\circ}$ CStorage temperature range, $T_{stg}$ $-65^{\circ}$ C to $150^{\circ}$ C
------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

 The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book, literature number SCBD002.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	3	3.6	v
VIH	High-level input voltage	2		v
VIL	Low-level input voltage		0.8	v
VI	Input voltage	0	5.5	V
ЮН	High-level output current		-32	mA
IOL	Low-level output current		32	mA
TA	Operating free-air temperature	0	70	°C

NOTE 3: Unused inputs must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

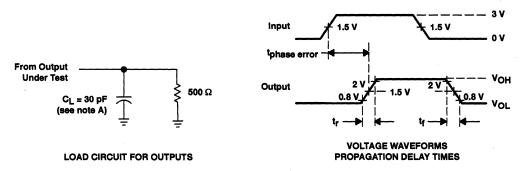
PARAMETER		TEST CONDITIONS		T <sub>A</sub> = 3	25°C	UNIT
FARAMEIER		TEST CONDITIONS			MAX	UNIT
VIK	$V_{\rm CC} = 3 V,$	lj = –18 mA			-1.2	V
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	l <sub>OH</sub> = -100 μA		Vcc-0	.2	v
VOH	$V_{CC} = 3 V,$	i <sub>OH</sub> = - 32 mA		2		v
Vei	V <sub>CC</sub> = 3 V,	l <sub>OL</sub> = 100 μA			0.2	v
VOL	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA			0.5	v
	$V_{CC} = 0$ or MAX <sup>‡</sup> ,	V <sub>I</sub> = 3.6 V V <sub>I</sub> = V <sub>CC</sub> or GND			±10	
li .	V <sub>CC</sub> = 3.6 V,				±1	μA
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V			10	μA
lozl	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0			-10	μA
			Outputs high		2	
lcc	$V_{CC} = 3.6 V,$ $V_{I} = V_{CC} \text{ or GND}$	l <sub>O</sub> = 0,	Outputs low		2	mA
			Outputs disabled		2	
Ci	$V_{I} = V_{CC}$ or GND				6	pF
Co	VO = VCC or GND				9	pF

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



#### CDC536 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS378D – APRIL 1994 – REVISED APRIL 1996

PARAMETER MEASUREMENT INFORMATION



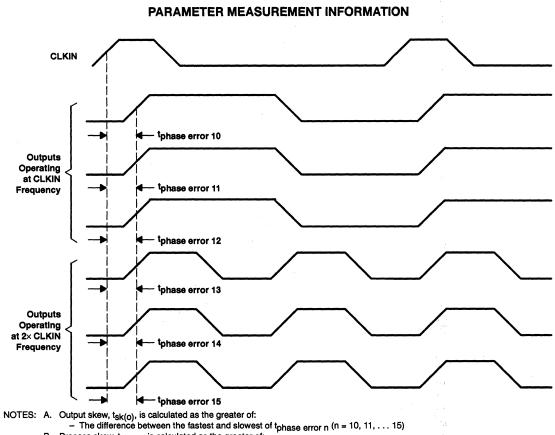
NOTES: A. CL includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  100 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns. C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



## **CDC536 3.3-V PHASE-LOCK LOOP CLOCK DRIVER** WITH 3-STATE OUTPUTS SCAS378D – APRIL 1994 – REVISED APRIL 1996



B. Process skew,  $t_{sk(pr)}$ , is calculated as the greater of:

- The difference between the maximum and minimum tphase error n (n = 10, 11, ... 15) across multiple devices under identical operating conditions.

Figure 3. Waveforms for Calculation of tsk(o) and tsk(pr)



CDC2536 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS377B – APRIL 1994 – REVISED NOVEMBER 1995

DL PACKAGE

(TOP VIEW)

AV<sub>CC</sub> [1

AGND 2

CLKIN 13

SEL 🛛 4

OE 15

GND 6

1Y1 07

V<sub>CC</sub> Is

GND 9

1Y2 10

V<sub>CC</sub> [11

GND 112

1Y3 113

VCC 114

28 AV<sub>CC</sub>

27 AGND

26 FBIN

25 TEST

24 CLR

23 Vcc

22 2Y1

21 GND

20 Vcc

19 2Y2

18 GND

17 Vcc

16 2Y3

15 GND

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V V<sub>CC</sub>
- Distributes One Clock Input to Six Outputs
- One Select Input Configures Three Outputs to Operate at One-Half or Double the Input Frequency
- No External RC Network Required
- On-Chip Series Damping Resistors
- External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input
- Application for Synchronous DRAM, High-Speed Microprocessor
- TTL-Compatible Inputs and Outputs
- Outputs Drive 50-Ω Parallel-Terminated Transmission Lines
- State-of-the-Art *EPIC-*II*B*<sup>TM</sup> BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V<sub>CC</sub> and Ground Pins Reduce Switching Noise
- Packaged in Plastic 28-Pin Shrink Small-Outline Package

#### description

The CDC2536 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with syncronous DRAMs and popular microprocessors operating at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. The CDC2536 operates at 3.3-V V<sub>CC</sub> and is designed to drive a properly terminated 50- $\Omega$  transmission line. The CDC2536 also provides on-chip series-damping resistors, eliminating the need for external termination components.

The feedback (FBIN) input is used to synchronize the output clocks in frequency and phase to the input clock (CLKIN). One of the six output clocks must be fed back to FBIN for the PLL to maintain synchronization between CLKIN and the outputs. The output used as the feedback pin is synchronized to the same frequency as CLKIN.

The Y outputs can be configured to switch in phase and at the same frequency as CLKIN. The select (SEL) input configures three Y outputs to operate at one-half or double the CLKIN frequency depending on which pin is fed back to FBIN (see Tables 1 and 2). All output signal duty cycles are adjusted to 50% independent of the duty cycle at the input clock.

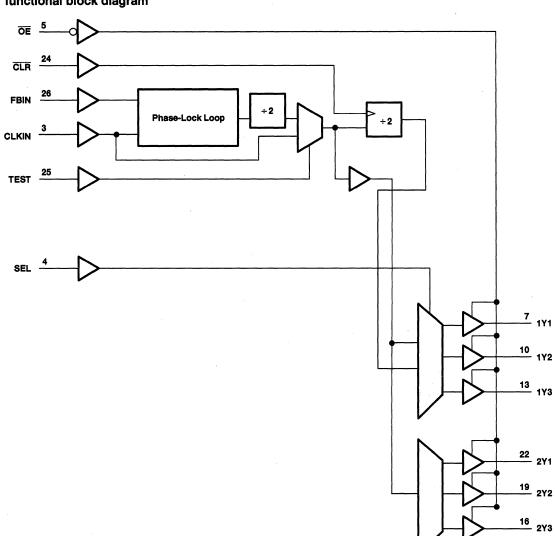
Output-enable  $\overline{(OE)}$  is provided for output control. When  $\overline{OE}$  is high, the outputs are in the high-impedance state. When  $\overline{OE}$  is low, the outputs are active.  $\overline{CLR}$  is negative-edge triggered and can be used to reset the outputs operating at half frequency. TEST is used for factory testing of the device and can be use to bypass the PLL. TEST should be strapped to GND for normal operation.

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#### CDC2536 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS377B – APRIL 1994 – REVISED NOVEMBER 1995



functional block diagram



#### CDC2536 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS377B – APRIL 1994 – REVISED NOVEMBER 1995

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	-0.5 V to 7 V 0.5 V to 5.5 V 24 mA 20 mA 50 mA 0.7 W
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

 The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book, literature number SCBD002.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	3	3.6	V
VIH	High-level input voltage	2		V
VIL	Low-level input voltage		0.8	V
VI	Input voltage	0	5.5	V
ЮН	High-level output current		-12	mA
IOL	Low-level output current		12	mA
TA	Operating free-air temperature	0	70	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

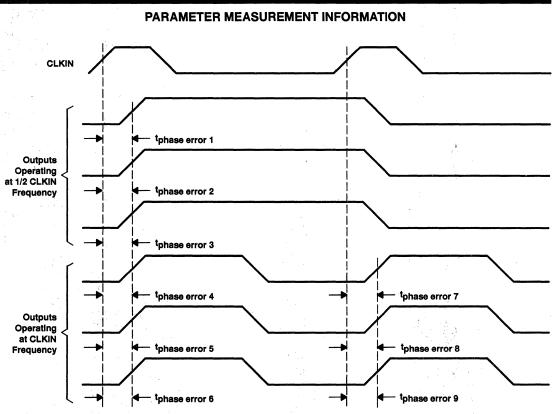
# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				TA = 2	25°C	UNIT
PARAMETER		TEST CONDITIONS				
VIK	V <sub>CC</sub> = 3 V,	lj = -18 mA	· · · · · · · · · · · · · · · · · · ·		-1.2	v
Veu	$V_{CC} = MIN \text{ to MAX}^{\ddagger},$	lOH = -100 μA		V <sub>CC</sub> -0.2	2	v
VOH	V <sub>CC</sub> = 3 V,	IOH = - 12 mA		2		v
Vei	V <sub>CC</sub> = 3 V,	l <sub>OL</sub> = 100 μA			0.2	v
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	IOL = 12 mA			0.8	v
	$V_{CC} = 0$ or MAX <sup>‡</sup> ,	V <sub>I</sub> = 3.6 V V <sub>I</sub> = V <sub>CC</sub> or GND			±10	μA
1	V <sub>CC</sub> = 3.6 V,				±1	
<sup>I</sup> OZH	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V			10	μA
IOZL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0			-10	μA
		l <sub>O</sub> = 0,	Outputs high		2	
ICC	$V_{CC} = 3.6 V,$ $V_{I} = V_{CC} \text{ or GND}$		Outputs low		2	mA
			Outputs disabled		2	
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND				6	рF
Co	Vo = VCC or GND				9	pF

<sup>+</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



# CDC2536 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS377B - APRIL 1994 - REVISED NOVEMBER 1995



NOTES: A. Output skew, tsk(o), is calculated as the greater of:

- The difference between the fastest and slowest of tphase error n (n = 1, 2, ... 6) - The difference between the fastest and slowest of tphase error n (n = 7, 8, 9)

B. Process skew, tsk(pr), is calculated as the greater of:

- The difference between the maximum and minimum tphase error n (n = 1, 2, ... 6) across multiple devices under identical operating conditions
- The difference between the maximum and minimum tphase error n (n = 7, 8, 9) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculations of tsk(o) and tsk(pr)



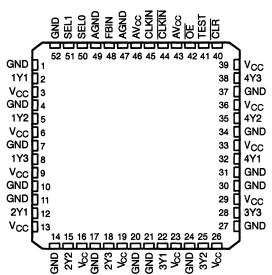
## **CDC582** 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH DIFFERENTIAL LVPECL CLOCK INPUTS

SCAS446B - JULY 1994 - REVISED FEBRUARY 1996

- . Low Output Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V V<sub>CC</sub>
- **Distributes Differential LVPECL Clock** Inputs to 12 TTL-Compatible Outputs
- **Two Select Inputs Configure Up to Nine** Outputs to Operate at One-Half or Double the Input Frequency
- **No External RC Network Required**

- . State-of-the-Art EPIC-IIB™ BICMOS Design Significantly Reduces Power Dissipation
- External Feedback Input (FBIN) is Used to Synchronize the Outputs With the Clock Inputs
- Application for Synchronous DRAMs
- Distributed V<sub>CC</sub> and Ground Pins Reduce Switching Noise
- Packaged in 52-Pin Quad Flatpack

PAH PACKAGE (TOP VIEW)



#### description

The CDC582 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align the frequency and phase of the clock output signals to the differential LVPECL clock (CLKIN, CLKIN) input signals. It is specifically designed to operate at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. The CDC582 operates at 3.3-V V<sub>CC</sub>.

The feedback input (FBIN) synchronizes the frequency of the output clocks with the input clock (CLKIN, CLKIN) signals. One of the twelve output clocks must be fed back to FBIN for the PLL to maintain synchronization between the differential CLKIN and CLKIN inputs and the outputs. The output used as feedback is synchronized to the same frequency as the clock (CLKIN and CLKIN) inputs.

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#### output configuration B

Output configuration B is valid when any output configured as a  $1 \times$  frequency output in Table 2 is fed back to FBIN. The frequency range for the differential clock inputs is 25 MHz to 50 MHz when using output configuration B. Outputs configured as  $1 \times$  outputs operate at the input clock frequency, while outputs configured as  $2 \times$  outputs operate at double the frequency of the differential clock inputs.

INP	UTS	OUTPUTS		
SEL1	SEL0	1× FREQUENCY	2× FREQUENCY	
L	L	All	None	
L	н	1Yn	2Yn, 3Yn, 4Yn	
н	L	1Yn, 2Yn	3Yn, 4Yn	
н	н	1Yn, 2Yn, 3Yn	4Yn	
NOTE:	n = 1, 2,	3		

Table	2.	Output	Confid	guration	В



#### CDC582 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH DIFFERENTIAL LVPECL CLOCK INPUTS SCA5446B – JULY 1994 – REVISED FEBRUARY 1996

#### **Terminal Functions**

TERMINAL						
NAME	NO.	1/0	DESCRIPTION			
	44, 45	I	Clock input. CLKIN and $\overline{\text{CLKIN}}$ are the differential clock signals to be distributed by the CDC582 clock-driver circuit. These inputs are used to provide the reference signal to the integrated PLL that generates the clock output signals. CLKIN and $\overline{\text{CLKIN}}$ must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and valid CLKIN and $\overline{\text{CLKIN}}$ signals are applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.			
CLR	40	I	Clear. $\overline{\text{CLR}}$ is used to reset the VCO/4 reference frequency. $\overline{\text{CLR}}$ is negative-edge triggered and should be strapped to V <sub>CC</sub> or GND for normal operation.			
FBIN	48	1	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hardwired to one of the twelve clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between the FBIN and the differential clock input (CLKIN and $\overline{\text{CLKIN}}$ ).			
ŌĒ	42	I	Output enable. $\overline{OE}$ is the output enable for all outputs. When $\overline{OE}$ is low, all outputs are enabled. When $\overline{OE}$ is high, all outputs are driven to the low state. Since the feedback signal for the PLL is taken directly from an output terminal, placing the outputs in the logic low state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{OE}$ , enabling the output buffers, a stabilization time is required before the PLL obtains phase lock.			
SEL1, SEL0	51, 50	1	Output configuration select. SEL0 and SEL1 select the output configuration for each output bank (e.g., $1 \times , 1/2 \times ,$ or $2 \times )$ (see Tables 1 and 2).			
TEST	41	1	TEST is used to bypass the PLL circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be strapped to GND for normal operation.			
1Y1-1Y3 2Y1-2Y3 3Y1-3Y3	2, 5, 8 12, 15, 18 22, 25, 28	ο	These outputs are configured by SEL1 and SEL0 to transmit one-half or one-fourth the frequency of the VCO. The relationship between the input clock frequency and the output frequency is dependent on SEL1 and SEL0 and the frequency of the output being fed back to FBIN. The duty cycle of the Y outputs is nominally 50% independent of the duty cycle of the input clock signals.			
4Y1-4Y3	32, 35, 38	0	These outputs transmit one-half the frequency of the VCO. The relationship between the input clock frequency and the output frequency is dependent on the frequency of the output being fed back to FBIN. The duty cycle of the Y outputs is nominally 50% independent of the duty cycle of CLKIN.			

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 4.6 V
Input voltage range, V <sub>1</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> (see Note 1)	–0.5 V to 5.5 V
Current into any output in the low state, Io	
Input clamp current, IIK (VI < 0)	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipationat T <sub>A</sub> = 55°C (in still air) (see Note 2)	1.2 W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

 The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book, literature number SCBD002.



#### CDC582 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH DIFFERENTIAL LVPECL CLOCK INPUTS SCA5446B – JULY 1994 – REVISED FEBRUARY 1996

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
<sup>†</sup> clock	Clock frequency	VCO is operating at four times the CLKIN/CLKIN frequency		.50	MHz
		VCO is operating at double the CLKIN/CLKIN frequency		100	MILTZ
	Input clock duty cycle		40%	60%	
	Stabilization time <sup>†</sup>	After SEL1, SEL0		/ <b>50</b>	
		Atter OE↓		50	<sup>,</sup> μs
		After power up		50	

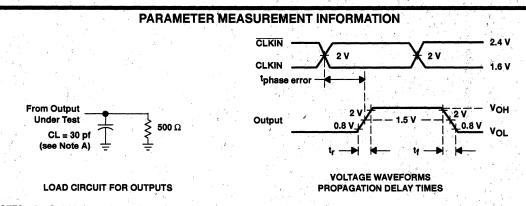
<sup>†</sup> Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 15 \text{ pF}$ (see Note 4 and Figures 1, 2, and 3)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
	Duty cycle		Y	45% 55%	
	fmax			100	MHz
	Jitter(pk-pk)		Yî:	200	ps
1.1	<sup>t</sup> phase error <sup>‡</sup>	CLKINT	n the term of ter	-500 500	ps
· · ·	<sup>t</sup> sk(o) <sup>‡</sup>		$\mathbf{Y} = \{\mathbf{y}_{i}, \dots, \mathbf{y}_{i}\}$	0.5	ns
	<sup>t</sup> sk(pr) <sup>‡</sup>		Y	1	ns
	tr 👘		*	1.4	, ns
·	tr i			1.4	ns

<sup>‡</sup> The propagation delay, tphase error, is dependent on the feedback path from any output to the FBIN. The tphase error, tsk(o), and tsk(pr) specifications are only valid for equal loading of all outputs.

NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.



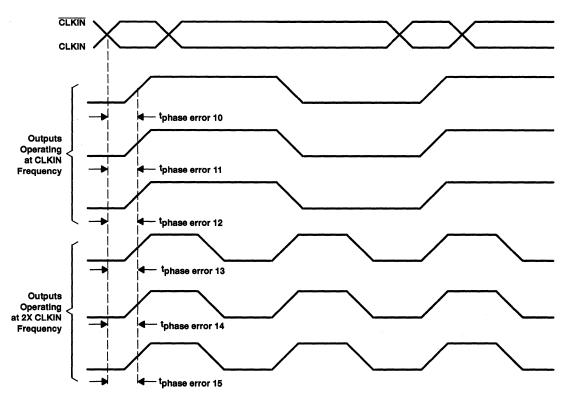
NOTES: A. CL includes probe and jig capacitance.

- B. The outputs are measured one at a time with one transition per measurement.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>Q</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns,

#### Figure 1. Load Circuit and Voltage Waveforms



## **CDC582 3.3-V PHASE-LOCK LOOP CLOCK DRIVER** WITH DIFFERENTIAL LVPECL CLOCK INPUTS SCAS446B – JULY 1994 – REVISED FEBRUARY 1996



PARAMETER MEASUREMENT INFORMATION

NOTES: A. Output skew,  $t_{sk(0)}$ , is calculated as the greater of:

- The difference between the fastest and slowest of tphase error n (n = 10, 11, ... 15)

B. Process skew, tsk(pr), is calculated as the greater of:

- The difference between the maximum and minimum tphase error n (n = 10, 11, ... 15) across multiple devices under identical operating conditions

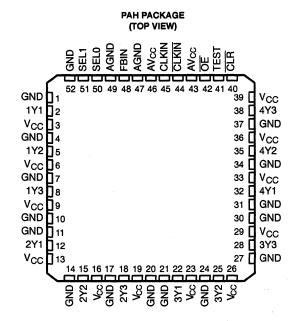
Figure 3. Waveforms for Calculation of tsk(o)



#### CDC2582 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH DIFFERENTIAL LVPECL CLOCK INPUTS SCAS3798 – FEBRUARY 1993 – REVISED FEBRUARY 1996

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V V<sub>CC</sub>
- Distributes Differential LVPECL Clock Inputs to 12 TTL-Compatible Outputs
- Two Select Inputs Configure Up to Nine Outputs to Operate at One-Half or Double the Input Frequency
- No External RC Network Required
- External Feedback Input (FBIN) Is Used to Synchronize the Outputs With the Clock Inputs

- Application for Synchronous DRAMs
- Outputs Have Internal 26-Ω Series Resistors to Dampen Transmission-Line Effects
- State-of-the-Art *EPIC*-II*B*<sup>TM</sup> BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V<sub>CC</sub> and Ground Pins Reduce Switching Noise
- Packaged in 52-Pin Quad Flatpack



#### description

The CDC2582 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align the frequency and phase of the clock output signals to the differential LVPECL clock (CLKIN, CLKIN) input signals. It is specifically designed to operate at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. Each output has an internal 26- $\Omega$  series resistor that improves the signal integrity at the load. The CDC2582 operates at 3.3-V V<sub>CC</sub>.

The feedback input (FBIN) synchronizes the frequency of the output clocks with the input clock (CLKIN, CLKIN) signals. One of the twelve output clocks must be fed back to FBIN for the PLL to maintain synchronization between the differential CLKIN and CLKIN inputs and the outputs. The output used as feedback is synchronized to the same frequency as the clock (CLKIN and CLKIN) inputs.

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## output configuration B

Output configuration B is valid when any output configured as a  $1 \times$  frequency output in Table 2 is fed back to FBIN. The frequency range for the differential clock inputs is 25 MHz to 50 MHz when using output configuration B. Outputs configured as  $1 \times$  outputs operate at the input clock frequency, while outputs configured as  $2 \times$  outputs operate at double the frequency of the differential clock inputs.

INPUTS		OUTPUTS		
SEL1	SEL0	1× FREQUENCY	2× FREQUENCY	
L	L	All	None	
L	н	1Yn	2Yn, 3Yn, 4Yn	
н	L	1Yn, 2Yn	3Yn, 4Yn	
н	н	1Yn, 2Yn, 3Yn	4Yn	

## Table 2. Output Configuration B

NOTE: n = 1, 2, 3



# 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH DIFFERENTIAL LVPECL CLOCK INPUTS SCAS379B – FEBRUARY 1993 – REVISED FEBRUARY 1996

		1	Terminal Functions
TERM NAME	INAL NO.	vo	DESCRIPTION
CLKIN CLKIN	44, 45	, L.	Clock input. CLKIN and CLKIN are the differential clock signals to be distributed by the CDC2582 clock-driver circuit. These inputs are used to provide the reference signal to the integrated PLL that generates the clock-output signals. CLKIN and CLKIN must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and valid CLKIN and CLKIN signals are applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
CLR	40	1	Clear. $\overline{\text{CLR}}$ is used to reset the VCO/4 reference frequency. $\overline{\text{CLR}}$ is negative-edge triggered and should be strapped to V <sub>CC</sub> or GND for normal operation.
FBIN	48	1 1 1	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hardwired to one of the twelve clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero-phase delay between the FBIN and the differential clock input (CLKIN and CLKIN).
<b></b>	42	7	Output enable. $\overline{OE}$ is the output enable for all outputs. When $\overline{OE}$ is low, all outputs are enabled. When $\overline{OE}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the PLL is taken directly from an output terminal, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{OE}$ , enabling the output buffers, a stabilization time is required before the PLL obtains phase lock.
SEL1, SEL0	51, 50	) 	Output configuration select. SEL0 and SEL1 select the output configuration for each output bank (e.g., $1\times$ , $1/2\times$ , or $2\times$ ) (see Tables 1 and 2).
TEST	41	: 	TEST is used to bypass the PLL circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high; the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be strapped to GND for normal operation.
1Y1-1Y3 2Y1-2Y3 3Y1-3Y3	2, 5, 8 12, 15, 18 22, 25, 28		These outputs are configured by SEL1 and SEL0 to transmit one-half or one-fourth the frequency of the VCO. The relationship between the input clock frequency and the output frequency is dependent on SEL1 and SEL0 and the frequency of the output being fed back to FBIN. The duty cycle of the Y outputs is nominally 50% independent of the duty cycle of the input clock signals. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.
4Y1-4Y3	32, 35, 38	 0	These outputs transmit one-half the frequency of the VCO. The relationship between the input clock frequency and the output frequency is dependent on the frequency of the output being fed back to FBIN. The duty cycle of the Y outputs is nominally 50% independent of the duty cycle of CLKIN. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

	Supply voltage range, V <sub>CC</sub> 0.5 V to 4.6 V
	Input voltage range, VI (see Note 1)
	Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> (see Note 1) $\dots$ -0.5 V to 5.5 V
4	Current into any output in the low state, IO
	Input clamp current, $I_{IK}$ (VI < 0)
	Output clamp current, $I_{OK}$ (V <sub>O</sub> < 0)
	Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 2) 1.2 W
	Storage temperature range, T <sub>stg</sub> 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book, literature number SCBD002.



## CDC2582 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH DIFFERENTIAL LVPECL CLOCK INPUTS SCAS379B - FEBRUARY 1993 - REVISED FEBRUARY 1996

# timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT	
	Clock frequency	VCO is operating at four times the CLKIN/CLKIN frequency	25	50	MHz	
fclock	Clock frequency	VCO is operating at double the CLKIN/CLKIN frequency	50	100	IVIFIZ	
	Input clock duty cycle		40%	60%		
		After SEL1, SEL0		50		
	Stabilization time <sup>†</sup>	After OE↓		50	μs	
		After power up		50		

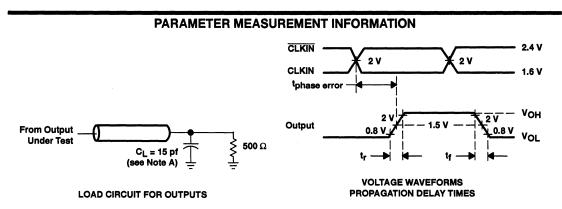
<sup>†</sup> Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 15 \text{ pF}$ (see Note 4 and Figures 1, 2, and 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
Duty cycle		Y	45%	55%	
fmax			100		MHz
Jitter(pk-pk)	CLKIN↑	Y↑		200	ps
<sup>t</sup> phase error <sup>‡</sup>	CLKINŤ	Y	500	500	ps
<sup>t</sup> sk(o) <sup>‡</sup>		Y		0.5	ns
<sup>t</sup> sk(pr) <sup>‡</sup>		Y		1	ns
tr				1.4	ns
tf				1.4	ns

<sup>‡</sup> The propagation delay, t<sub>phase error</sub>, is dependent on the feedback path from any output to FBIN. The t<sub>phase error</sub>, t<sub>sk(o)</sub>, and t<sub>sk(pr)</sub> specifications are only valid for equal loading of all outputs.

NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.



NOTES: A. CL includes probe and jig capacitance.

- B. The outputs are measured one at a time with one transition per measurement.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms



## CDC2582 **3.3-V PHASE-LOCK LOOP CLOCK DRIVER** WITH DIFFERENTIAL LVPECL CLOCK INPUTS SCAS379B - FEBRUARY 1993 - REVISED FEBRUARY 1996

## CLKIN CLKIN tphase error 10 Outputs Operating at CLKIN tphase error 11 Frequency tphase error 12 tphase error 13 Outputs Operating at 2X CLKIN tphase error 14 Frequency <sup>- t</sup>phase error 15

## PARAMETER MEASUREMENT INFORMATION

NOTES: A. Output skew,  $t_{sk(0)}$ , is calculated as the greater of:

- The difference between the fastest and slowest of tphase error n (n = 10, 11, ... 15)

B. Process skew, tsk(pr), is calculated as the greater of:

- The difference between the maximum and minimum tphase error n (n = 10, 11, ... 15) across multiple devices under identical operating conditions

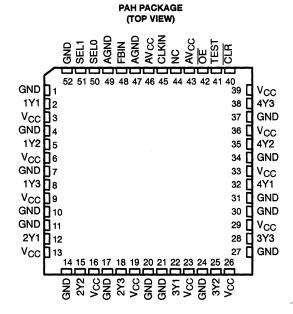
Figure 3. Waveforms for Calculation of tsk(o) and tsk(pr)



CDC586 3.3-V PHASE-LOCK-LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS336C - FEBRUARY 1993 - REVISED NOVEMBER 1995

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V V<sub>CC</sub>
- Distributes One Clock Input to Twelve Outputs
- Two Select Inputs Configure Up to Nine Outputs to Operate at One-Half or Double the Input Frequency
- No External RC Network Required
- External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input

- Application for Synchronous DRAM, High-Speed Microprocessor
- TTL-Compatible Inputs and Outputs
- Outputs Drive Parallel 50-Ω Terminated Transmission Lines
- State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V<sub>CC</sub> and Ground Pins Reduce Switching Noise
- Packaged in 52-Pin Thin Quad Flat Package



NC - No internal connection

## description

The CDC586 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with popular microprocessors operating at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. The CDC586 operates at 3.3-V V<sub>CC</sub> and is designed to drive a properly terminated 50- $\Omega$  transmission line.

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## output configuration A

Output configuration A is valid when any output configured as a 1x frequency output in Table 1 is fed back to FBIN. The input frequency range for CLKIN is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2x outputs operate at half the CLKIN frequency, while outputs configured as 1x outputs operate at the same frequency as CLKIN.

INPUTS		OUTPUTS		
SEL1	SEL0	1/2x 1x FREQUENCY FREQUEN		
L	۲ <b>L</b> .	None	All	
L	H	··· 1Yn	2Yn, 3Yn, 4Yn	
н	L	1Yn, 2Yn	3Yn, 4Yn	
н	н	1Yn, 2Yn, 3Yn	4Yn	

## Table 1. Output Configuration A

## output configuration B

Output configuration B is valid when any output configured as a 1x frequency output in Table 2 is fed back to FBIN. The input frequency range for CLKIN is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1x outputs operate at the CLKIN frequency, while outputs configured as 2x outputs operate at double the frequency of CLKIN.

INPUTS		OUTPUTS		
SEL1	SEL0	1x FREQUENCY	2x FREQUENCY	
L	L	All	None	
L	Н	. 1Yn	2Yn, 3Yn, 4Yn	
н	L	1Yn, 2Yn	3Yn, 4Yn	
н	н	1Yn, 2Yn, 3Yn	4Yn	

#### Table 2. Output Configuration B



## Terminal Functions

TERM	NAL		
NAME	NO.	1/0	DESCRIPTION
CLKIN	45	I	Clock input. CLKIN is the clock signal distributed by the CDC586 clock-driver circuit. CLKIN provides the reference signal to the integrated PLL that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
CLR	40	I	Clear. $\overline{\text{CLR}}$ resets the VCO/4 reference frequency. $\overline{\text{CLR}}$ is negative edge triggered and should be strapped to GND or V <sub>CC</sub> for normal operation.
FBIN	48	1	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hardwired to one of the twelve clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between FBIN and CLKIN.
ŌĒ	42	I	Output enable. $\overline{OE}$ is the output enable for all outputs. When $\overline{OE}$ is low, all outputs are enabled. When $\overline{OE}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the PLL is taken directly from an output terminal, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{OE}$ , enabling the output buffers, a stabilization time is required before the PLL obtains phase lock.
SEL1, SEL0	51, 50	1	Output configuration select. SEL0 and SEL1 select the output configuration for each output bank (e.g. $1 \times 1/2 \times$ or $2 \times$ ). (see Tables 1 and 2).
TEST	41	1	TEST is used to bypass the PLL circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be strapped to GND for normal operation.
1Y1-1Y3 2Y1-2Y3 3Y1-3Y3	2, 5, 8 12, 15, 18 22, 25, 28	0	Output ports. These outputs are configured by SEL1 and SEL0 to transmit one-half or one-fourth the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on SEL1 and SEL0 and the frequency of the output being fed back to FBIN. The duty cycle of the Y output signals is nominally 50% independent of the duty cycle of CLKIN.
4Y1-4Y3	32, 35, 38	ο	Output ports. 4Y1-4Y3 transmit one-half the frequency of the VCO regardless of the state of SEL1 and SEL0. The relationship between the CLKIN frequency and the output frequency is dependent on the frequency of the output being fed back to FBIN. The duty cycle of the Y output signals is nominally 50% independent of the duty cycle of CLKIN.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	
Input voltage range, VI (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state,	
V <sub>O</sub> (see Note 1)	
Current into any output in the low state, IO	64 mA
Input clamp current, IIK (VI < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2)	1.2 W
Storage temperature range, T <sub>stg</sub>	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

 The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book, literature number SCBD002.



## CDC586 3.3-V PHASE-LOCK-LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS336C - FEBRUARY 1993 - REVISED NOVEMBER 1995

# timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f	Clock frequency	VCO is operating at four times the CLKIN frequency	25	50	MHz
<sup>†</sup> clock		VCO is operating at double the CLKIN frequency	50	100	MHZ
	Input clock duty cycle		40%	60%	
		After SEL1, SEL0		50	
	Stabilization time <sup>†</sup>	After OE↓		50	
	Stabilization time	After power up		50	μs
		After CLKIN		50	

<sup>†</sup> Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 30 \text{ pF}$ (see Note 4 and Figures 1 through 3)

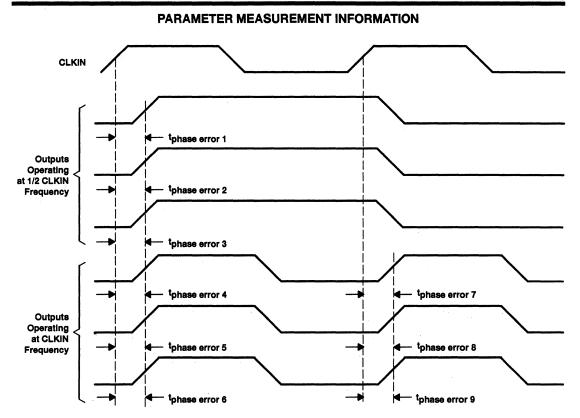
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	МАХ	UNIT
fmax			100		MHz
Duty cycle		Y	45%	55%	
<sup>t</sup> phase error <sup>‡</sup>	CLKIN↑	Y	500	+500	ps
Jitter(pk-pk)	CLKIN↑	Y		200	ps
<sup>t</sup> sk(o) <sup>‡</sup>				0.5	ns
t <sub>sk(pr)</sub> ‡				1	ns
tr				1.4	ns
tf				1.4	ns

<sup>‡</sup> The propagation delay, t<sub>phase error</sub>, is dependent on the feedback path from any output to FBIN. The t<sub>phase error</sub>, t<sub>sk(o)</sub>, and t<sub>sk(pr)</sub> specifications are valid only for equal loading of all outputs.

NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.



## **CDC586 3.3-V PHASE-LOCK-LOOP CLOCK DRIVER** WITH 3-STATE OUTPUTS SCAS336C - FEBRUARY 1993 - REVISED NOVEMBER 1995



NOTES: A. Output skew, tsk(o), is calculated as the greater of:

The difference between the fastest and slowest of tphase error n (n = 1, 2, ... 6)

- The difference between the fastest and slowest of tphase error n (n = 7, 8, 9)

B. Process skew, tsk(pr), is calculated as the greater of:

- The difference between the maximum and minimum tphase error n (n = 1, 2, ... 6) across multiple devices under identical operating conditions.
- The difference between the maximum and minimum tphase error n (n = 7, 8, 9) across multiple devices under identical operating conditions.

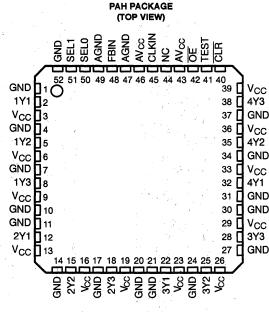
## Figure 2. Waveforms for Calculation of tsk(o)



## CDC2586 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS337B - FEBRUARY 1993 - REVISED NOVEMBER 1995

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V V<sub>CC</sub>
- Distributes One Clock Input to Twelve Outputs
- Two Select Inputs Configure Up to Nine Outputs to Operate at One-Half or Double the Input Frequency
- No External RC Network Required
- External Feedback (FBIN) Synchronizes the Outputs to the Clock Input

- Application for Synchronous DRAM, High-Speed Microprocessor
- TTL-Compatible inputs and Outputs
- Outputs Have Internal 26-Ω Series Resistors to Dampen Transmission-Line Effects
- State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V<sub>CC</sub> and Ground Pins Reduce Switching Noise
- Packaged in 52-Pin Thin Quad Flat Package



NC - No internal connection

## description

The CDC2586 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with popular microprocessors operating at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured for half-frequency operation. Each output has an internal 26- $\Omega$  series resistor that improves the signal integrity at the load. The CDC2586 operates at nominal 3.3-V V<sub>CC</sub>.

The feedback input (FBIN) synchronizes the output clocks in frequency and phase to CLKIN. One of the twelve output clocks must be fed back to FBIN for the PLL to maintain synchronization between CLKIN and the outputs. The output used as feedback is synchronized to the same frequency as CLKIN.

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## output configuration A

Output configuration A is valid when any output configured as a  $1 \times$  frequency output in Table 1 is fed back to FBIN. The input frequency range for CLKIN is 50 MHz to 100 MHz when using output configuration A. Outputs configured as  $1/2 \times$  outputs operate at half the CLKIN frequency, while outputs configured as  $1 \times$  outputs operate at the same frequency as CLKIN.

INPUTS		OUTPUTS		
SEL1	SEL0	1/2× FREQUENCY	1× FREQUENCY	
L	L	None	All	
L	н	1Yn	2Yn, 3Yn, 4Yn	
н	L	1Yn, 2Yn	3Yn, 4Yn	
н	н	1Yn, 2Yn, 3Yn	4Yn	

Table 1. Outpu	t Configuration A	4
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NOTE: n = 1, 2, 3

## output configuration B

Output configuration B is valid when any output configured as a  $1 \times$  frequency output in Table 2 is fed back to FBIN. The input frequency range for CLKIN is 25 MHz to 50 MHz when using output configuration B. Outputs configured as  $1 \times$  outputs operate at the CLKIN frequency, while outputs configured as  $2 \times$  outputs operate at double the frequency of CLKIN.

Table	2. Output	ut Config	guration I	В
-------	-----------	-----------	------------	---

INP	UTS	OUTPUTS		
SEL1	SEL0	1× FREQUENCY	2× FREQUENCY	
L	L	All	None	
L	н	1Yn	2Yn, 3Yn, 4Yn	
н	L	1Yn, 2Yn	3Yn, 4Yn	
н	н	1Yn, 2Yn, 3Yn	4Yn	

NOTE: n = 1, 2, 3



## CDC2586 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS

SCAS337B - FEBRUARY 1993 - REVISED NOVEMBER 1995

## **Terminal Functions**

TERMINAL			B TO OBIOTIONI
NAME	NO.	1/0	DESCRIPTION
CLKIN	45	I	Clock input. CLKIN is the clock signal to be distributed by the CDC2586 clock-driver circuit. CLKIN provides the reference signal to the integrated PLL that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
CLR	40	1	Clear. $\overline{\text{CLR}}$ resets the VCO/4 reference frequency. $\overline{\text{CLR}}$ is negative-edge triggered and should be strapped to GND or V <sub>CC</sub> for normal operation.
FBIN	48	1	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard wired to one of the twelve clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between FBIN and CLKIN.
ŌĒ	42	I	Output enable. $\overline{OE}$ is the output enable for all outputs. When $\overline{OE}$ is low, all outputs are enabled. When $\overline{OE}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the PLL is taken directly from an output, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{OE}$ , enabling the output buffers, a stabilization time is required before the PLL obtains phase lock.
SEL1, SEL0	51, 50	1	Output configuration select. SEL0 and SEL1 select the output configuration for each output bank (e.g., $1/2 \times 1 \times$ or 2x) (see Tables 1 and 2).
TEST	41	ļ	TEST is used to bypass the PLL circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be strapped to GND for normal operation.
1Y1-1Y3 2Y1-2Y3 3Y1-3Y3	2, 5, 8 12, 15, 18 22, 25, 28	ο	Output ports. These outputs are configured by the select inputs (SEL1, SEL0) to transmit one-half or one-fourth the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on the select inputs and the frequency of the output being fed back to FBIN (see Tables 1 and 2). The duty cycle of the Y output signals is nominally 50%, independent of the duty cycle of CLKIN. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.
4Y1-4Y3	32, 35, 38	0	Output ports. 4Y1-4Y3 transmit one-half the frequency of the VCO regardless of the state of the select inputs. The relationship between the CLKIN frequency and the output frequency is dependent on the frequency of the output being fed back to FBIN (see Tables 1 and 2). The duty cycle of the Y output signals is nominally 50%, independent of the duty cycle of CLKIN. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 4.6 V
Input voltage range, VI (see Note 1)	
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)	0.5 V to 5.5 V
Current into any output in the low state, Io	24 mA
Input clamp current, I <sub>IK</sub> (VI < 0)	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2)	1.2 W
Storage temperature range, T <sub>stg</sub>	65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book, literature number SCBD002.



## CDC2586 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS337B - FEBRUARY 1993 - REVISED NOVEMBER 1995

## timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
	Clock frequency	VCO operating at four times the CLKIN frequency	25	50	MHz
fclock	Clock frequency	VCO operating at double the CLKIN frequency	50	100	WINZ
	Input clock duty cycle			60%	
		After SEL1, SEL0		50	
	o	After OE↓		50	
	Stabilization time <sup>†</sup>	After power up		50	μs
		After CLKIN		50	

<sup>†</sup> Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

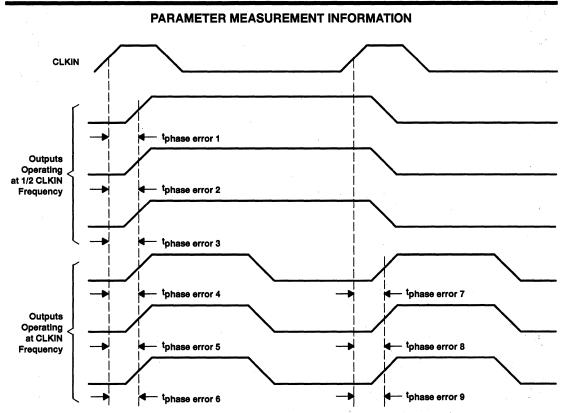
## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 15 \text{ pF}$ (see Note 4 and Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	МАХ	UNIT
fmax			100		MHz
Duty cycle		Y	45%	55%	
<sup>t</sup> phase error <sup>‡</sup>	CLKIN↑	Y↑	-500	+500	ps
jitter	CLKINÎ	Y↑		200	ps
<sup>t</sup> sk(o) <sup>‡</sup>				0.5	ns
<sup>t</sup> sk(pr) <sup>‡</sup>				1	ns
tr				1.4	ns
t <sub>f</sub>				1.4	ns

<sup>‡</sup>The propagation delay, t<sub>phase error</sub>, is dependent on the feedback path from any output to FBIN. The t<sub>phase error</sub>, t<sub>sk(0)</sub>, and t<sub>sk(pr)</sub> specifications are valid only for equal loading of all outputs. NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.



## CDC2586 **3.3-V PHASE-LOCK LOOP CLOCK DRIVER** WITH 3-STATE OUTPUTS SCAS337B - FEBRUARY 1993 - REVISED NOVEMBER 1995



NOTES: A. Output skew, t<sub>sk(0)</sub>, is calculated as the greater of:
The difference between the fastest and slowest of tphase error n (n = 1, 2, ... 6)
The difference between the fastest and slowest of tphase error n (n = 7, 8, 9)
B. Process skew, t<sub>sk(pr)</sub>, is calculated as the greater of:

- The difference between the maximum and minimum tphase error n (n = 1, 2, ... 6) across multiple devices under identical operating conditions
- The difference between the maximum and minimum tphase error n (n = 7, 8, 9) across multiple devices under identical operating conditions

C. For configuration A, see Table 1

## Figure 2. Waveforms for Calculation of tsk(o) for Configuration A



CDC587 3.3-V PHASE-LOCK LOOP CLOCK DRIN WITH 3-STATE OUTPUTS

> DGG PACKAGE (TOP VIEW)

CLKIN [

V<sub>CC</sub> 🛾 15 2Y0 🛛 16

2Y1 117

GND 🚺 18

V<sub>CC</sub> [] 19

2Y2 🛛 20

2Y3 121

GND 🛛 22

V<sub>CC</sub> [] 23

GND 24

SEL0 25

SEL1 26

SEL2 27

SEL3 28

SCAS562B - DECEMBER 1995 - REVISED JULY 1996

CC

•	Low-Output Skew and Jitter for Clock
	Distribution and Synchronization

- Operates at 3.3-V V<sub>CC</sub>
- **Distributes One Clock Input to 16 Outputs**
- Four Select Inputs Configure Output Frequency
- Internal Loop Filter Eliminates the Need for External RC Network
- **Dedicated External Feedback Output and** Input for Phase Synchronization With the Clock Input
- Applications for Synchronous DRAM, High-Speed Microprocessors, and SSTL 3 Applications
- LVTTL- or SSTL\_3-Compatible Inputs and Outputs
- Distributed V<sub>CC</sub> and Ground Pins Reduce **Switching Noise**
- Meets SSTL\_3 Class 1 and 2 Specifications
- Packaged in Plastic Small-Outline Package

## description

The CDC587 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. The CDC587 operates at 3.3-V LVTTL-Vcc and provides or SSTL 3-compatible inputs and outputs. The CDC587 operates at frequencies from 16.67 MHz up to 150 MHz, and is ideally suited for high-speed microprocessor and synchronous DRAM applications.

A dedicated feedback output (FBOUT) is used to synchronize the output clocks in frequency and phase to the
CLKIN reference. Four banks of four outputs (1Yn, 2Yn, 3Yn, 4Yn) are configured to operate at specified ratios
of the input frequency by four select (SELn) inputs. Selectable ratios of the input frequency are 1X, 2X, 3X, 1/2X,
and 1/3X.

The output-enable  $\overline{(OE)}$  input provides control for the Y output banks. When  $\overline{OE}$  is high, the outputs are in a high-impedance state. When  $\overline{OE}$  is low, the outputs switch in accordance with the select inputs. In addition, RESET provides a master reset for the CDC587 counter circuitry. This allows the outputs to be reset to a known state. TEST provides a bypass of the integrated PLL and divider circuitry. When TEST is high, the input clock bypasses the PLL and is buffered directly to the outputs.

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V <sub>REF</sub> [	2	55 GND
FBIN	3	54 AV <sub>CC</sub>
V <sub>CC</sub>	4	53 AGND
FBOUT	5	52 AV <sub>CC</sub>
GND [	6	51 AGND
V <sub>CC</sub> [	7	50 V <sub>CC</sub>
1Y0	8	49 4Y0
1Y1 [	9	48 4Y1
GND [	10	47 🛛 GND
V <sub>CC</sub>	11	46 V <sub>CC</sub>
1Y2	12	45 4Y2
1Y3 [	13	44 🛛 4Y3
GND [	14	43 🛛 GND

42**1)** V<sub>CC</sub>

41 🛛 3Y0

40 1 3Y1

39 🛛 GND

38 🛛 V<sub>CC</sub>

37 3Y2

36 🛛 3Y3

35 GND

34 🛛 V<sub>CC</sub>

33 🛛 GND

32 RESET

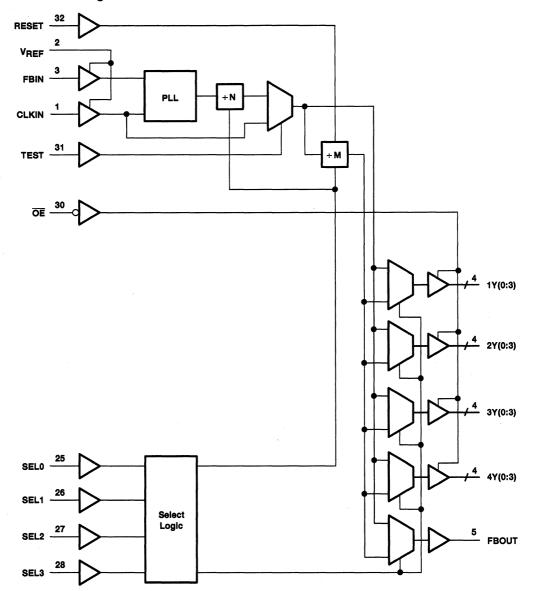
31 TEST

30 1 OE

29 GND

## CDC587 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS562B - DECEMBER 1995 - REVISED JULY 1996







**PRODUCT PREVIEW** 

## CDC587 **3.3-V PHASE-LOCK LOOP CLOCK DRIVER** WITH 3-STATE OUTPUTS SCAS562B – DECEMBER 1995 – REVISED JULY 1996

## recommended operating conditions (see Note 4)

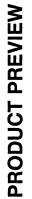
			MIN	NOM	MAX	UNIT
Vcc	Supply voltage	Supply voltage			3.6	V
VREF	SSTL reference voltage		1.3	1.5	1.7	V
VI	Input voltage		0		5.5	V
VIH F		CLK, FBIN	VREF+100 mV			
	High-level input voltage	CLK, FBIN (V <sub>REF</sub> = GND)	2		· · · · · · · · · · · · · · · · · · ·	v
		Other inputs	2			
	Low-level input voltage	CLK, FBIN			VREF-100 mV	
VIL		CLK, FBIN (V <sub>REF</sub> = GND)			0.8	v
		Other inputs			0.8	
ЮН	High-level output current				-20	mA
lol	Low-level output current				20	mA
Τ <sub>A</sub>	Operating free-air temperature		0		70	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYPT	MAX	UNIT
VIK	V <sub>CC</sub> = 3 V,	lj =18 mA				-1.2	v
	$V_{CC} = MIN \text{ to MAX}^{\ddagger},$	IOH =100 μA		V <sub>CC</sub> -0.2			
Voн	Vac. 2V	IOH = -16 mA		2.2			v
	V <sub>CC</sub> = 3 V	I <sub>OH</sub> = -20 mA		2.1			
		l <sub>OL</sub> = 100 μA				0.2	
VOL	V <sub>CC</sub> = 3 V	I <sub>OL</sub> = 16 mA				0.5	v
		I <sub>OL</sub> = 20 mA				0.5	l
	$V_{CC} = 0$ or MAX <sup>‡</sup> ,	V <sub>1</sub> = 3.6 V,	VREF = GND			±10	
lμ <sup>1</sup>	V <sub>CC</sub> = 3.6 V	$V_1 = V_{CC}$ or GND,	V <sub>REF</sub> = GND			±1	μA
	VCC = 3.6 V	V <sub>I</sub> = 2.1 V or 0.9 V,	V <sub>REF</sub> = 1.5			±1	
IOZH	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				10	μA
IOZL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0				-10	μA
	V <sub>CC</sub> = 3.6 V,	$V_1 = V_{CC}$ or GND,	V <sub>REF</sub> = GND			1	
lcc	IO = 0	V <sub>I</sub> = 2.1 V or 0.9 V,	VREF = 1.5 V			6	mA
<u> </u>	$V_{I} = V_{CC}$ or GND,	VREF = GND			3		~5
Ci	V <sub>I</sub> = 2.1 V or 0.9 V,	V <sub>REF</sub> = 1.5 V			3		pF
Co	V <sub>O</sub> = 3 V or 0,	VREF = GND			6		~~
0	V <sub>O</sub> = 2.1 V or 0.9 V,	V <sub>REF</sub> = 1.5 V			6		pF

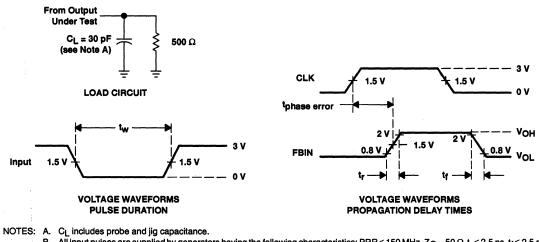
<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.
 <sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.





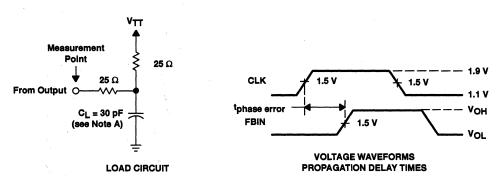
## CDC587 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS562B - DECEMBER 1995 - REVISED JULY 1996

#### PARAMETER MEASUREMENT INFORMATION



- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  150 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- C. The outputs are measured one at a time with one transition per measurement.





NOTES: A. CL includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  150 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- C. The outputs are measured one at a time with one transition per measurement.
- D.  $V_{TT} = V_{REF} = V_{CC} \times 0.45$

Figure 2. Load Circuit and Voltage Waveforms for SSTL\_3



**PRODUCT PREVIEW** 

## 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS560B - DECEMBER 1995 - REVISED JULY 1996

DGG PACKAGE (TOP VIEW)

•	Low-Output Skew and Jitter for Clock
	Distribution and Synchronization

- Operates at 3.3-V V<sub>CC</sub>
- **Distributes One Clock Input to 16 Outputs**
- Four Select Inputs Configure Output Frequency
- Internal Loop Filter Eliminates the Need for External RC Network
- **Dedicated External Feedback Output and** Input for Phase Synchronization With the Clock Input
- Applications for Synchronous DRAM, High-Speed Microprocessors, and SSTL\_3 Applications
- LVTTL- or SSTL 3-Compatible Inputs and Outputs
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimize High-Speed Switching Noise
- Meets SSTL 3 Class 1 and 2 Specifications
- Packaged in 56-Pin Plastic Small-Outline Package

## description

The CDC2587 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. The CDC2587 operates at 3.3-V Vcc and provides LVTTLor SSTL\_3-compatible inputs and outputs. The CDC2587 operates at frequencies from 16.67 MHz to 150 MHz, and is ideally suited for high-speed microprocessor and synchronous DRAM applications. The CDC2587 provides integrated 25- $\Omega$  series damping resistors to improve signal integrity.

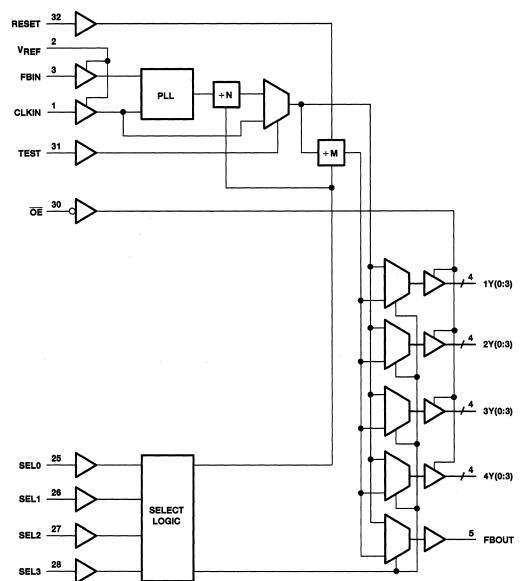
A dedicated feedback output (FBOUT) is used to synchronize the output clocks in frequency and phase to the CLKIN reference. Four banks of four outputs (1Yn, 2Yn, 3Yn, 4Yn) are configured to operate at specified ratios of the input frequency by four select (SELn) inputs. Selectable ratios of the input frequency are 1X, 2X, 3X, 1/2X, and 1/3X.

PRODUCT PREVIEW information concerns products in the formative or	
design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to	
change or discontinue these products without notice.	



CLKIN VREF FBIN GNC FBO VCC 1Y0 1Y1 GNC 1Y2 1Y3 GND VCC 1Y2 1Y3 GND VCC 2Y0 2Y1 GND VCC 2Y2 GND VCC 2Y2 GND VCC 2Y2 GND VCC C C C C C C C C C C C C C C C C C	2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25	55         54           53         52           51         50           52         51           50         49           48         44           43         44           44         43           44         44           39         38           37         36           33         32           31         32	V <sub>CC</sub> GND AV <sub>CC</sub> AGND V <sub>CC</sub> 4Y0 4Y1 GND V <sub>CC</sub> 4Y2 4Y3 GND V <sub>CC</sub> 3Y0 3Y1 GND V <sub>CC</sub> 3Y0 3Y1 GND V <sub>CC</sub> 3Y2 3Y3 GND V <sub>CC</sub>
SELO	25	32	RESET
		31	TEST
SEL2	27		ŌĒ
SEL3	28	29	GND

## CDC2587 3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS SCAS560B – DECEMBER 1995 – REVISED JULY 1996



functional block diagram



**PRODUCT PREVIEW** 

## CDC2587 **3.3-V PHASE-LOCK LOOP CLOCK DRIVER** WITH 3-STATE OUTPUTS SCAS560B - DECEMBER 1995 - REVISED JULY 1996

## recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		3		3.6	V
VREF	SSTL reference voltage		1.3	1.5	1.7	V
VI	Input voltage		0		5.5	V
		CLKIN, FBIN	VREF+100 mV			
VIH	High-level input voltage	CLKIN, FBIN (V <sub>REF</sub> = GND)	2			V
		Other inputs	2			
		CLKIN, FBIN			VREF-100 mV	
VIL	Low-level input voltage	CLKIN, FBIN (V <sub>REF</sub> = GND)			0.8	v
		Other inputs			0.8	
ЮН	High-level output current				-12	mA
IOL	Low-level output current				12	mA
TA	Operating free-air temperature		0		70	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYPT	MAX	UNIT
VIK	V <sub>CC</sub> = 3 V,	lı =18 mA				-1.2	٧
Varia	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	l <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			v
VOH	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 12 mA		2.4			v
Ve	V <sub>CC</sub> = 3 V	l <sub>OL</sub> = 100 μA				0.2	v
VOL	vCC = 3 v	I <sub>OL</sub> = 12 mA				0.4	v
	$V_{CC} = 0$ or MAX <sup>‡</sup> ,	V <sub>I</sub> = 3.6 V,	V <sub>REF</sub> = GND			±10	
li i	V <sub>CC</sub> = 3.6 V	$V_{I} = V_{CC}$ or GND,	V <sub>REF</sub> = GND			±1	μA
	vCC = 3.0 v	V <sub>I</sub> = 2.1 V or 0.9 V,	VREF = 1.5 V			±1	
lozн	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				10	μA
IOZL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0				-10	μA
1	V <sub>CC</sub> = 3.6 V,	$V_{I} = V_{CC}$ or GND,	V <sub>REF</sub> = GND			1	mA
lcc	I <sub>O</sub> = 0,	V <sub>I</sub> = 2.1 V or 0.9 V,	V <sub>REF</sub> = 1.5 V			1	mA
· •	$V_{I} = V_{CC}$ or GND,	V <sub>REF</sub> = GND			3		•E
Ci	V <sub>I</sub> = 2.1 V or 0.9 V,	V <sub>REF</sub> = 1.5 V			3		pF
C	V <sub>O</sub> = 3 V or 0,	V <sub>REF</sub> = GND			6		- F
Co	V <sub>O</sub> = 2.1 V or 0.9 V,	V <sub>REF</sub> = 1.5 V			6		pF

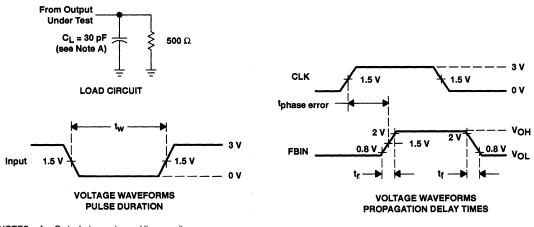
<sup>†</sup> All typical values are at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}C$ .

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



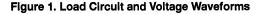
## CDC2587 **3.3-V PHASE-LOCK LOOP CLOCK DRIVER** WITH 3-STATE OUTPUTS SCAS560B - DECEMBER 1995 - REVISED JULY

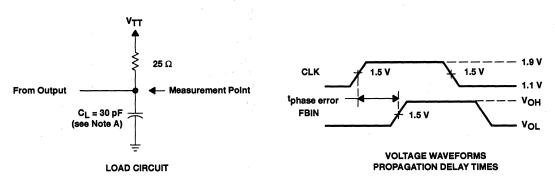
## PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  150 MHz, Z<sub>O</sub> = 50 Ω, t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns,
- C. The outputs are measured one at a time with one transition per measurement.





NOTES: A. CL includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  150 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.

C. The outputs are measured one at a time with one transition per measurement.

D.  $V_{TT} = V_{REF} = V_{CC} \times 0.4$ 

Figure 2. Load Circuit and Voltage Waveforms for SSTL 3 Class 1



General Information	1
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Address Buffers/Latches/Flip-Flops	3
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TMS626162 524288-WORD BY 16-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY VISED JULY 1996

<ul> <li>Organization 512K × 16 × 2 Banks</li> <li>3.3-V Power Supply (±10% Tolerance)</li> </ul>	-	GE PACKAG ( TOP VIEW )	
<ul> <li>Two Banks for On-Chip Interleaving (Gapless Accesses)</li> </ul>			] V <sub>SS</sub> ] DQ15
<ul> <li>High Bandwidth – Up to 83-MHz Data Rates</li> </ul>	DQU [ DQ1 [		
<ul> <li>Read Latency Programmable to 1, 2, or 3 Cycles From Column-Address Entry</li> </ul>	V <sub>SSQ</sub> [ DQ2 [	4 47	V <sub>SSQ</sub> DQ13
<ul> <li>Burst Sequence Programmable to Serial or</li> </ul>	DQ3		DQ12
Interleave	V <sub>CCQ</sub> [	7 44	D V <sub>CCQ</sub>
<ul> <li>Burst Length Programmable to 1, 2, 4, 8, or</li> </ul>	DQ4 [		DQ11
Full Page	DQ5 [		DQ10
Chip Select and Clock Enable for	V <sub>SSQ</sub> [		l v <sub>ssa</sub>
Enhanced-System Interfacing	DQ6		
Cycle-by-Cycle DQ-Bus Mask Capability	DQ7 [		
With Upper and Lower Byte Control			I V <sub>CCQ</sub>
<ul> <li>Auto-Refresh and Self-Refresh Capability</li> </ul>			
<ul> <li>4K Refresh (Total for Both Banks)</li> </ul>			DQMU CLK
<ul> <li>High-Speed, Low-Noise, Low-Voltage TTL</li> </ul>	RAS		
(LVTTL) Interface			
Power-Down Mode			
<ul> <li>Compatible With JEDEC Standards</li> </ul>	A10		
Pipeline Architecture	AO [	1	D A7
<ul> <li>Employs Enhanced Performance Implanted</li> </ul>	A1 [	22 29	A6
CMOS (EPIC™) Technology Fabricated by	A2 [	23 28	D A5
Texas Instruments (TI™)	A3 [	24 27	] A4
Temperature Ranges:     Operating 000 to 7000	V <sub>CC</sub> [	25 26	]v <sub>ss</sub>

- Operating, 0°C to 70°C Storage, - 55°C to 150°C
- **Performance Ranges:**

		ACTV	
	SYNCHRONOUS	COMMAND TO	REFRESH
	CLOCK CYCLE	READ OR WRT	TIME
	TIME	COMMAND	INTERVAL
	<sup>t</sup> CK	<sup>t</sup> RCD	<sup>t</sup> REF
	(MIN)	(MIN)	(MAX)
'626162-124	12 ns	30 ns	64 ms
'626162-12	12 ns	30 ns	64 ms
'626162-15	15 ns	30 ns	64 ms

## description

The TMS626162 series of devices are high-speed 16777216-bit synchronous dynamic randomaccess memories (SDRAMs) organized as two banks of 524288 words with sixteen bits per word.

	PIN NOMENCLATURE					
A0-A10	Address Inputs					
	A0-A10 Row Addresses					
	A0-A7 Column Addresses					
	A10 Automatic-Precharge Select					
A11	Bank Select					
CAS	Column-Address Strobe					
CKE	Clock Enable					
CLK	System Clock					
CS	Chip Select					
DQ0-DQ15	SDRAM Data Input/Data Output					
DQML, DQMU	Data/Output Mask Enables					
NC	No Connect					
RAS	Row-Address Strobe					
VCC	Power Supply (3.3 V Typ)					
VCCQ	Power Supply for Output Drivers (3.3 V Typ)					
VSS	Ground					
VSSQ	Ground for Output Drivers					
W	Write Enable					

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## TMS626162 524288-WORD BY 16-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY

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## operation (continued)

COMMAND	STATE OF BANK(S)	<del>cs</del>	RAS	CAS	W	A11	A10	A9-A0	MNEMONIC
Mode register set	T = deac B = deac	L	L	L	L	x	x	A9=V A8-A7=0 A6-A0=V	MRS
Bank deactivate (precharge)	X	L	L	н	L	BS	L	X	DEAC
Deactivate all banks	X	L	L	н	L	X	н	X	DCAB
Bank activate/row-address entry	SB = deac	L	L	н	н	BS	V	V	ACTV
Column-address entry/write operation	SB = actv	L	н	L	L	BS	L	V	WRT
Column-address entry/write operation with auto-deactivate	SB = actv	L	н	L	L	BS	н	v	WRT-P
Column-address entry/read operation	SB = actv	L	н	L	н	BS	L	V	READ
Column-address entry/read operation with auto-deactivate	SB = actv	L	н	L	н	BS	н	v	READ-P
Burst stop	SB = actv	L	н	н	L	X	Х	X	STOP
No operation	Х	L	н	н	н	X	Х	X	NOOP
Control-input inhibit/no operation	x	н	х	х	х	X	X	X	DESL
Auto refresh‡	T = deac B = deac	L	L	L	н	x	х	x	REFR

#### Table 1. Basic Command Truth Table<sup>†</sup>

<sup>†</sup> For execution of these commands on cycle n:

- CKE (n-1) must be high, or

- tCESP must be satisfied for power-down exit, or

- tCESP and tRC must be satisfied for self-refresh exit, or

- t<sub>CES</sub> and nCLE must be satisfied for clock-suspend exit.

DQMx(n) is a don't care.

<sup>‡</sup> Auto-refresh or self-refresh entry requires that all banks be deactivated or in an idle state prior to the command entry.

Legend: n

- = CLK cycle number
- = Logic low L
- Logic high н =
- = Don't care, either logic low or logic high х
- v Valid = т
  - Bank T =
- в = Bank B
- actv = Activated

deac = Deactivated

- BS = Logic high to select bank T; logic low to select bank B
- SB = Bank selected by A11 at cycle n



## TMS626162 524288-WORD BY 16-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY SMOS683D - FEBRUARY 1995 - REVISED JULY 1996

## operation (continued)

COMMAND	STATE OF BANK(S)	DQML DQMU‡ (n)	DATA IN (n)	DATA OUT (n + 2)	MNEMONIC
· _	T = deac and B = deac	x	N/A	Hi-Z	-
_	T = actv and B = actv (no access operation)\$	x	N/A	Hi-Z	· _
Data-in enable	T = write or B = write	L	v	N/A	ENBL
Data-in mask	T = write or B = write	н	м	N/A	MASK
Data-out enable	T = read or B = read	L	N/A	v	ENBL
Data-out mask	T = read or B = read	н	N/A	Hi-Z	MASK

## Table 3. DQM-Use Command Truth Table<sup>†</sup>

<sup>†</sup> For execution of these commands on cycle n:

- CKE (n) must be high, or

- tCESP must be satisfied for power-down exit, or

- tCESP and tRC must be satisfied for self-refresh exit, or

-  $t_{CES}$  and  $n_{CLE}$  must be satisfied for clock suspend exit.  $\overline{CS}(n)$ ,  $\overline{RAS}(n)$ ,  $\overline{CAS}(n)$ ,  $\overline{W}(n)$ , and A0-A11 are don't cares.

<sup>‡</sup> DQML controls D0-D7 and Q0-Q7

DQMU controls D8-D15 and Q8-Q15

§ A bank is no longer in an access operation one cycle after the last data-out cycle of a read operation, and two cycles after the last data-in cycle of a write operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a write operation.

Legend: n

- CLK cycle number
- Logic low L -
- Logic high н х

Don't care, either logic low or logic high

v Valid

М Masked input data

- N/A Not applicable
- т Bank T
- в Bank B

actv Activated

- Deactivated deac ...
- Activated and accepting data in on cycle n write =
- read Activated and delivering data out on cycle (n + 2) =



## TMS626162 524288-WORD BY 16-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY SMOS883D - FEBRUARY 1995 - REVISED JULY 1996

## burst sequence (continued)

	1	INTERNAL COLUM							IN ADDRESS A2-A0								
		DECIMAL					BINARY										
	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH	
	0 -	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111	
	1	2	3	4	5	6	7	0	001	010	011	100	101	110	111	000	
	2	3	4	5	6	7	0	1	010	011	100	101	110	111	000	001	
Serial	3	4	5	6	7	0	1	2	011	100	101	110	111	000	001	010	
Sella	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011	
	5	6	7	0	1	2	3	4	· 101	110	111	000	001	010	011	100	
	6	7	0	1	2	3	4	5	110	111	000	001	010	011	100	101	
	7	0	1	2	3	4	5	6	111	000	001	010	011	100	101	110	
	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111	
	1	0	3	2	5	4	7	6	001	000	011	010	101	100	111	110	
	2	3	0	1	6	7	4	5	010	011	000	001	110	111	100	101	
Interleave	3	2	1	0	7	6	5	4	011	010	001	000	111	110	101	100	
IIIGIIGAVE	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011	
	5	4	7	6	1	0	3	2	101	100	111	110	001	000	011	010	
	6	7	4	5	2	3	0	1	110	111	100	101	010	011	000	001	
	7	6	5	4	3	2	1	0	111	110	101	100	011	010	001	000	

#### Table 6. 8-Bit Burst Sequences

#### latency

The beginning data-out cycle of a read burst can be programmed to occur 1, 2, or 3 CLK cycles after the read command (see the section on setting the mode register, page 5–11). This feature allows the user to adjust the '626162 to operate in accordance with the system's capability to latch the data output from the '626162. The delay between the READ command and the beginning of the output burst is known as *read latency* (also known as **CAS** latency). After the initial output cycle begins, the data burst occurs at the CLK frequency without any intervening gaps. Use of minimum read latencies is restricted based on the particular maximum frequency rating of the '626162.

There is no latency for data-in cycles (write latency). The first data-in cycle of a write burst is entered at the same rising edge of CLK on which the WRT command is entered. The write latency is fixed and is not determined by the mode-register contents.

## two-bank operation

The '626162 contains two independent banks that can be accessed individually or in an interleaved fashion. Each bank must be activated with a row address before it can be accessed. Each bank then must be deactivated before it can be activated again with a new row address. The bank-activate/row-address-entry command (ACTV) is entered by holding RAS low, CAS high, W high, and A11 valid on the rising edge of CLK. A bank can be deactivated either automatically during a READ-P or a WRT-P command or by use of the deactivate-bank (DEAC) command. Both banks can be deactivated at once by use of the DCAB command (see Table 1 and the section on bank deactivation, page 5–10).



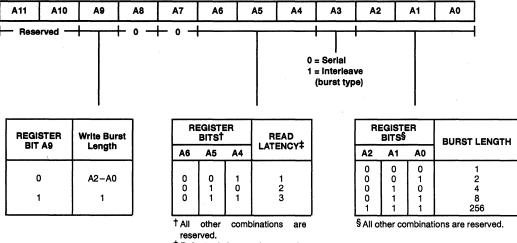
## CLK-suspend/power-down mode

For normal device operation, CKE should be held high to enable CLK. If CKE goes low during the execution of a READ (READ-P) or WRT (WRT-P) operation, the state of the DQ bus occurring at the immediate next rising edge of CLK is frozen at its current state, and no further inputs are accepted until CKE returns high. This is known as a CLK-suspend operation, and its execution is denoted as a HOLD command. The device resumes operation from the point at which it was placed in suspension, beginning with the second rising edge of CLK after CKE returns high.

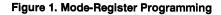
If CKE is brought low when no read or write command is in progress, the device enters power-down mode. If both banks are deactivated when power-down mode is entered, power consumption is reduced to the minimum. Power-down mode can be used during row-active or auto-refresh periods to reduce input-buffer power. After power-down mode is entered, no further inputs are accepted until CKE returns high. To ensure that data in the device remains valid during the power-down mode, the self-refresh command (SLFR) must be executed concurrently with the power-down entry (PDE) command. When exiting power-down mode, new commands can be entered on the first CLK edge after CKE returns high, provided that the setup time (t<sub>CESP</sub>) is satisfied. Table 2 shows the command configuration for a CLK-suspend/power-down operation; Figure 19, Figure 20, and Figure 38 show examples of the procedure.

## setting the mode register

The '626162 contains a mode register that must be programmed with the read latency, the burst type, and the burst length. This is accomplished by executing a mode-register set (MRS) command with the information entered on the address lines A0-A9. A logic 0 must be entered on A7 and A8, but A10 and A11 are don't-care entries for the '626162. When A9 = 1, the write-burst length is always 1. When A9 = 0, the write-burst length is defined by A0-A2. Figure 1 shows the valid combinations for a successful MRS command. Only valid addresses allow the mode register to be changed. If the addresses are not valid, the previous contents of the mode register remain unaffected. The MRS command is executed by holding RAS, CAS, and W low and the input mode word valid on A0-A9 on the rising edge of CLK (see Table 1). The MRS command can be executed only when both banks are deactivated.



‡ Refer to timing requirements for minimum valid read latencies based on maximum frequency rating.





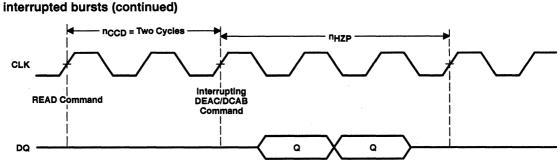
# TMS626162 524288-WORD BY 16-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY SMOS663D - FEBRUARY 1995 - REVISED JULY 1996

## Table 7. Read-Burst Interruption

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING READ BURST
READ, READ-P	Current output cycles continue until the programmed latency from the superseding-READ (READ-P) command is met and new output cycles begin (see Figure 2).
WRT, WRT-P	The WRT (WRT-P) command immediately supersedes the read burst in progress. To avoid data contention, DQMx must be held high before the WRT (WRT-P) command to mask output of the read burst on cycles ( $n_{CCD}$ -1), $n_{CCD}$ , and ( $n_{CCD}$ +1), assuming that there is any output on these cycles. For read latency = 1, read burst interruption by a WRT (WRT-P) command is not allowed at $n_{CCD}$ = 1, 2 (see Figure 3).
DEAC, DCAB	The DQ bus is in the high-impedance state when n <sub>HZP</sub> cycles are satisfied or when the read burst completes, whichever occurs first (see Figure 4).
STOP	The DQ bus is in the high-impedance state when n <sub>BSD</sub> cycles are satisfied or when the read burst completes, whichever occurs first. The bank remains active. A new read or write command cannot be entered for at least two cycles after the STOP command (see Figure 5).

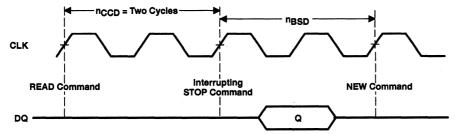


## TMS626162 524288-WORD BY 16-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY SMOS683D - FEBRUARY 1995 - REVISED JULY 1996



NOTE A: For this example, assume read latency = 3 and burst length = 4.

Figure 4. Read Burst Interrupted by DEAC Command



NOTE A: For this example, assume read latency = 3 and burst length = 4.

## Figure 5. Read Burst Interrupt by STOP Command

#### **Table 8. Write-Burst Interruption**

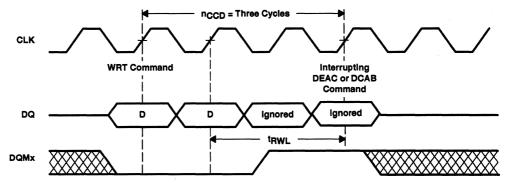
INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING WRITE BURST						
READ, READ-P Data in on previous cycle is written. No further data in is accepted (see Figure 6).							
WRT, WRT-P	The new WRT (WRT-P) command and data in immediately supersede the write burst in progress (see Figure 7).						
DEAC, DCAB	The DEAC/DCAB command immediately supersedes the write burst in progress. DQMx must be used to mask the DQ bus such that the write recovery specification (t <sub>RWL</sub> ) is not violated by the interrupt (see Figure 8).						
STOP	The data on the input pins at the time of the burst-STOP command is not written; no further data is accepted. The bank remains active. A new read or write command cannot be entered for at least nBSD cycles after the STOP command (see Figure 9).						



## TMS626162 524288-WORD BY 16-BIT BY 2-BA SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY

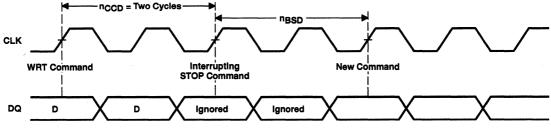
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## interrupted bursts (continued)



NOTE A: For this example, assume burst length = 4.

#### Figure 8. Write Burst Interrupted by DEAC/DCAB Command



NOTE A: For this example, assume burst length = 4.

## Figure 9. Write Burst Interrupted by STOP Command

#### power up

Device initialization should be performed after a power up to the full V<sub>CC</sub> level. After power is established, a 200-µs interval is required (with no inputs other than CLK). After this interval, both banks of the device must be deactivated. Eight REFR commands must be performed, and the mode register must be set to complete the device initialization.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	– 0.5 V to 4.6 V
Supply voltage range for output drivers, V <sub>CCO</sub>	– 0.5 V to 4.6 V
Voltage range on any pin (see Note 1)	– 0.5 V to 4.6 V
Short-circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range, TA	
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: All voltage values are with respect to VSS.



	DAMETED		TEOT CONDITI			'62616	'626162-12A		'626162-12		'626162-15	
PA	RAMETER		TEST CONDIT	IONS		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
VOH	High-level output voltage	I <sub>OH</sub> = −2 mA				2.4		2.4		2.4		v
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 2 mA	I <sub>OL</sub> = 2 mA						0.4		0.4	v
ų	Input current (leakage)	$0 V \le V_{I} \le V_{CC} + 0.3 V,$	All other pins = 0 V t	o V <sub>CC</sub>			±10		±10		±10	μA
ю	Output current (leakage)	$0 V \le V_O \le V_{CC} + 0.3 V$ , Output disabled					±10		±10		±10	μA
		T T		1 bank active	Burst length = 1 or 2		90		90		80	
1	Average read or write	t <sub>RC</sub> = MIN, t <sub>CK</sub> = M	1IN,	I Dank active	Burst length = 4 or 8		115		115		100	<u>ה</u> ע
ICC1	current	Read latency = 3		2 banks active, interleaving	Burst length = 1 or 2		150		150		120	
			Burst length = 4 or 8		190		190		150			
			CKE=VIH	KE=VIH			25		25		20	mA
	Standby	Both banks deactivated	CKE=V <sub>IL</sub>				2		2		2	
ICC2	current		CKE = 0 V (CMOS) CKE=VIH				1		1		1	
		1 or 2 banks active			30		30			- mA		
			CKE=VIL				8		8		100 mA 120 150 20 2 mA 1 25	
ICC3	Consecutive CBR commands	t <sub>RC</sub> = MIN	C = MIN						90		80	mA
	Burst		Read latency =				80		80		70	
ICC4 burst ICC4 gapless burst		ACTV not allowed, t <sub>CK</sub> = MIN, 2-bank interleaved			Read latency = 2		140		120		110	mA
		Read latency = 3					160		160		140	
1000	Self-refresh	CKE = VIL		,			2		2		2	m
ICC6	C6 current CKE = 0 V (CMOS)					1		1		1	1 11	

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Note 2)

NOTES: 2. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.

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## TMS626162 524288-WORD BY 16-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY SMO56830 - FEBRUARY 1995 - REVISED JULY 1996

# ac timing requirements over recommended ranges of supply voltage and operating free-air temperature<sup>†‡</sup>

			'62616	52-12A	'6261	62-12	'6261		
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		Read latency = 1	36		36		40		
tCK	Cycle time, CLK (system clock)	Read latency = 2	15		18		20		ns
		Read latency = 3	12		12		15		
<sup>t</sup> CKH	Pulse duration, CLK (system clock) high		4		4		4		ns
<sup>t</sup> CKL	Pulse duration, CLK (system clock) low		4		4		4		ns
		Read latency = 1		31		31		35	
<sup>t</sup> AC	Access time, CLK T to data out (see Note 4)	Read latency = 2		9		13		35 15 9 20 14 11	ns
	·,	Read latency = 3		9		9		9	
tLZ	Delay time, CLK to DQ in the low-impedanc	e state (see Note 5)	0		0		0		ns
	Delay time, CLK to DQ in the	Read latency = 1		20		20		20	
tHZ	high-impedance state	Read latency = 2		13		13		14	ns
	(see Note 6)	Read latency = 3		10		10		11	
tDS	Setup time, data input		3		3		3		ns
tAS	Setup time, address				3		3		ns
tcs	Setup time, control input (CS, RAS, CAS, W, DQMx)				3		3		ns
tCES	Setup time, CKE (suspend entry/exit, powe	r-down entry)	3		3		3		ns
<sup>t</sup> CESP	Setup time, CKE (power-down/self-refresh	exit) (see Note 7)	10		10		10		ns
tон	Hold time, CLK ↑ to data out		3		3		3		ns
<sup>t</sup> DH	Hold time, data input		1		1.5		1.5		ns
<sup>t</sup> AH	Hold time, address		1		1.5		1.5		ns
<sup>t</sup> CH	Hold time, control input (CS, RAS, CAS, W,	DQMx)	1		1.5		1.5		ns
<sup>t</sup> CEH	Hold time, CKE		1		1.5		1.5		ns
<sup>t</sup> RC	REFR command to ACTV, MRS, REFR, or ACTV command to ACTV, MRS, REFR, or Self-refresh exit to ACTV, MRS, REFR, or S	SLFR command;	96		108		120		ns
tRAS	ACTV command to DEAC or DCAB comma	Ind	60	100 000	72	100 000	75	100 000	ns
tRCD	ACTV command to READ or WRT command (see Note 8)		30		30		30		ns
t <sub>RP</sub>	DEAC or DCAB command to ACTV, MRS command	S, SLFR, or REFR	36		36		45		ns

<sup>†</sup> See Parameter Measurement Information, page 5-24, for load circuits.

<sup>‡</sup> All references are made to the rising transition of CLK, unless otherwise noted.

NOTES: 4. t<sub>AC</sub> is referenced from the rising transition of CLK that is previous to the data-out cycle. For example, the first data out t<sub>AC</sub> is referenced from the rising transition of CLK that is read latency – one cycle after the READ command. An access time is measured at output reference level 1.4 V.

5. tl 7 is measured from the rising transition of CLK that is read latency - one cycle after the READ command.

6. tHZ (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.

7. See Figure 20 and Figure 21

8. For read or write operations with automatic deactivate, tBCD must be set to satisfy minimum tBAS.



## TMS626162 524288-WORD BY 16-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY SMOS683D - FEBRUARY 1995 - REVISED JULY 1996

## Table 9. Number of Cycles Required to Meet Minimum Specification for Key Timing Parameters<sup>†</sup>

	• •			•				-	-			•	
			TMS	626802	-12A	TMS	TMS626802-12			62680	2-15	UNITS	
	Operating frequency			66	50	83	66	50	66	50	33	MHz	
<sup>t</sup> CK	Cycle time, CLK (syst	em clock)	12	15	20	12	15	20	15	20	30	ns	
	KEY PARAMETER				NL	JMBER	OFC	CLES	REQL	JIRED			
	Read latency, minimum programmed value			2	2	3	3	2	3	2	2	cycles	
<sup>t</sup> RCD	ACTV command to R	EAD or WRT command	3	2	2	3	2	2	2	2	1	cycles	
<sup>t</sup> RAS	ACTV command to D	EAC or DCAB command	5	4	3	6	5	4	5	4	3	cycles	
tRP	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR command			3	2	3	3	2	3	3	2	cycles	
<sup>t</sup> RC	REFR command to ACTV, MRS, or REFR command; self-refresh exit to ACTV, MRS, SLFR, or REFR command			7	5	9	8	6	8	6	4	cycles	
tRWL	Final data in to DEAC	or DCAB command	2	2	1	3	2	1	2	2	1	cycles	
tRRD	ACTV command for o other bank	ne bank to ACTV command for the	2	2	2	2	2	2	2	2	1	cycles	
	Final data out of READ-P operation	Read latency = 1	—	-	-	-	_	—	—		—	cycles	
<sup>t</sup> APR	to ACTV, MRS, SLFR. or REFR	Read latency = 2	-	2	1	_	-	1	-	2	2	cycles	
	command Read latency = 3		1	1	0	1	1	0	1	1	0	cycles	
tAPW	Final data in of WRT- REFR command	P operation to ACTV, MRS, SLFR, or	5	4	3	5	4	3	5	4	3	cycles	

<sup>†</sup> All references are made to the rising transition of CLK, unless otherwise noted.



## TMS626162 524288-WORD BY 16-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY SMOS663D – FEBRUARY 1995 – REVISED JULY 1996

## PARAMETER MEASUREMENT INFORMATION

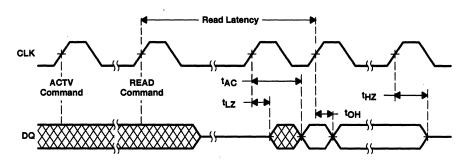


Figure 12. Output Parameters

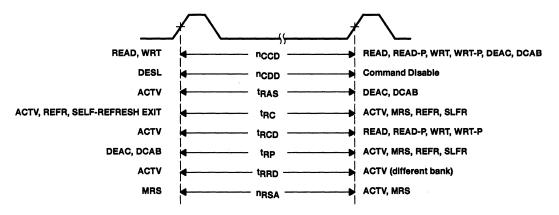


Figure 13. Command-to-Command Parameters



## TMS626162 524288-WORD BY 16-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY SMO56830 – FEBRUARY 1995 – REVISED JULY 1996

PARAMETER MEASUREMENT INFORMATION

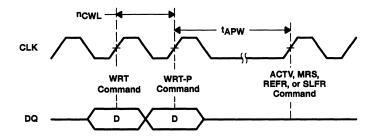
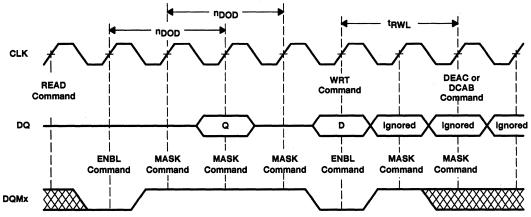


Figure 17. Write With Auto-Deactivate



NOTE A: For this example, assume read latency = 3, and burst length = 4.

Figure 18. DQ Masking



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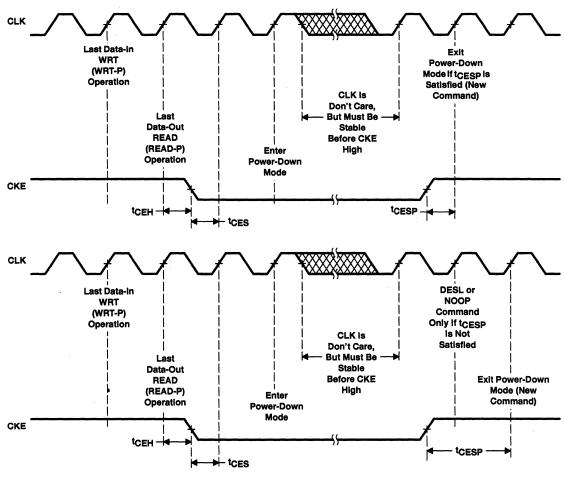
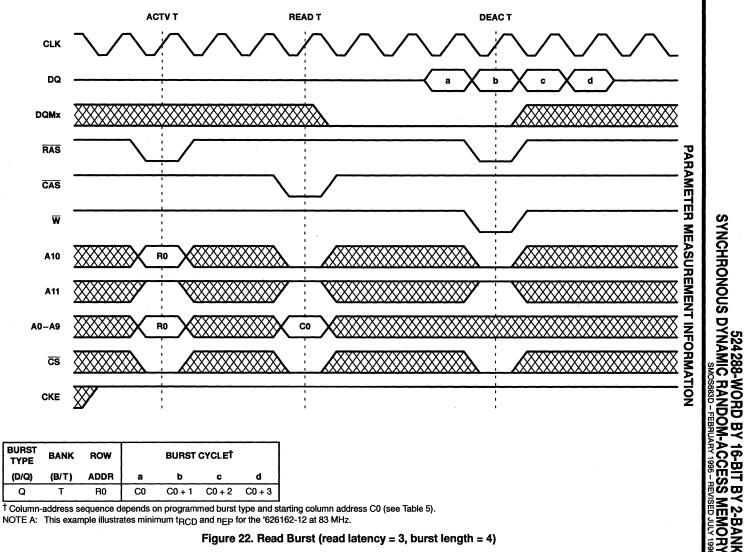


Figure 20. Power-Down Operation





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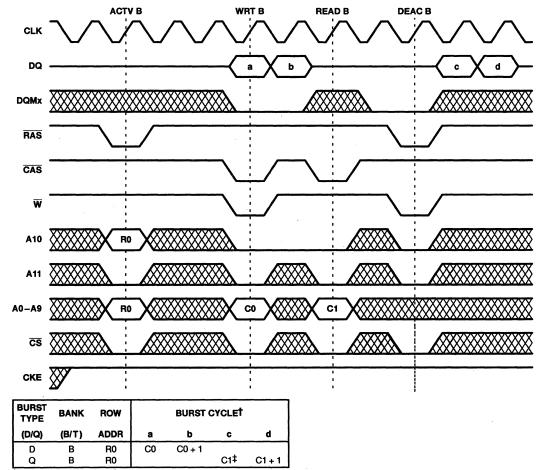
TMS626162

2-BANK

Figure 22. Read Burst (read latency = 3, burst length = 4)

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<sup>†</sup> Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 4). NOTE A: This example illustrates minimum t<sub>RCD</sub> and n<sub>EP</sub> for the '626162-12 at 83 MHz.

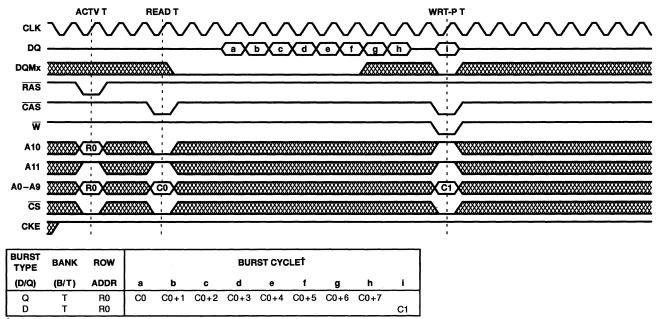
Figure 24. Write-Read Burst (read latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION

TMS626162 524 288-WORD BY 16-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY SMOSBBD - FEBRUARY 1995 - NEWSEND - FEBRUARY 1995

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<sup>†</sup> Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 6). NOTE A: This example illustrates minimum t<sub>RCD</sub> for the '626162-12 at 83 MHz.

Figure 26. Read Burst - Single Write With Automatic Deactivate (read latency = 3, burst length = 8)

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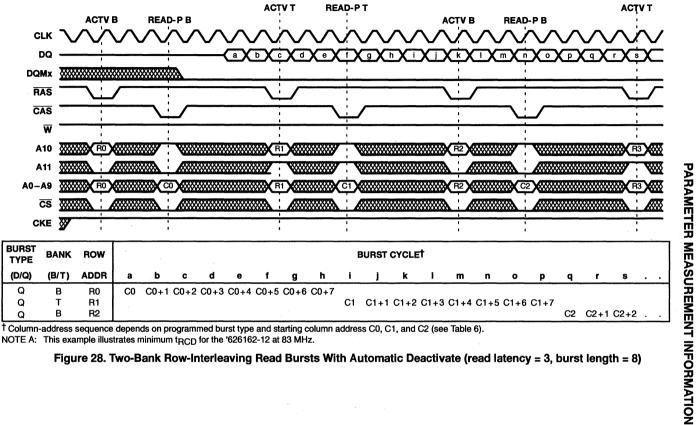
TMS626162

PARAMETER MEASUREMENT INFORMATION

5-35

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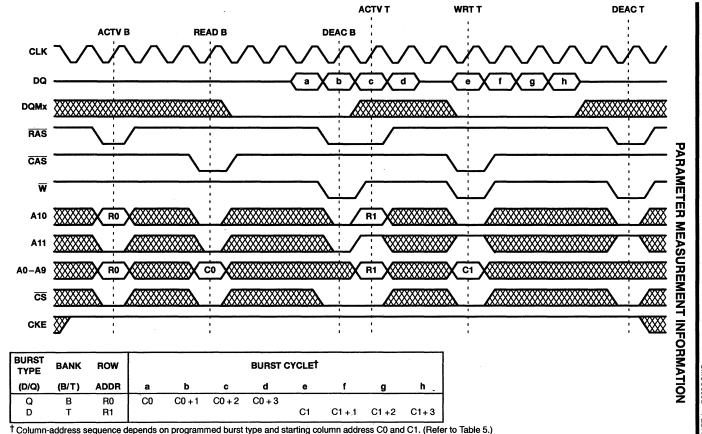
IEXAS



<sup>†</sup> Column-address sequence depends on programmed burst type and starting column address C0, C1, and C2 (see Table 6). NOTE A: This example illustrates minimum t<sub>BCD</sub> for the '626162-12 at 83 MHz.

Figure 28. Two-Bank Row-Interleaving Read Bursts With Automatic Deactivate (read latency = 3, burst length = 8)

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524 288-WORD E SYNCHRONOUS DYNAMIC RANDO

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BIT B

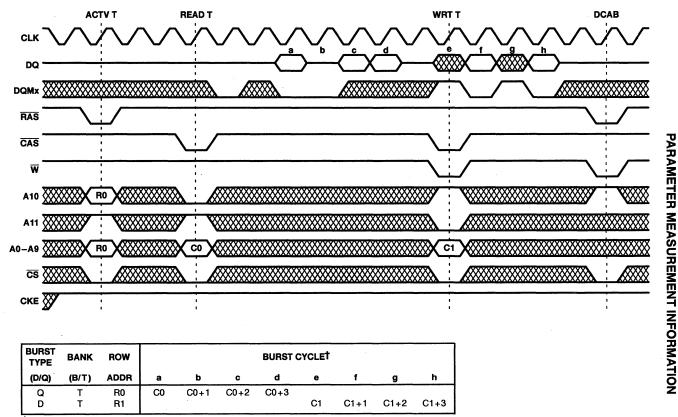
Y 2-BANK

NOTE A: This example illustrates minimum tRCD, nEP, and tRWL for the '626162-12 at 83 MHz.

Figure 30. Read-Burst Bank B, Write-Burst Bank T (read latency = 3, burst length = 4)

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5-39



<sup>†</sup> Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 5). NOTE A: This example illustrates minimum t<sub>RCD</sub> for the '626162-12 at 83 MHz.

Figure 32. Data Mask (read latency = 3, burst length = 4)

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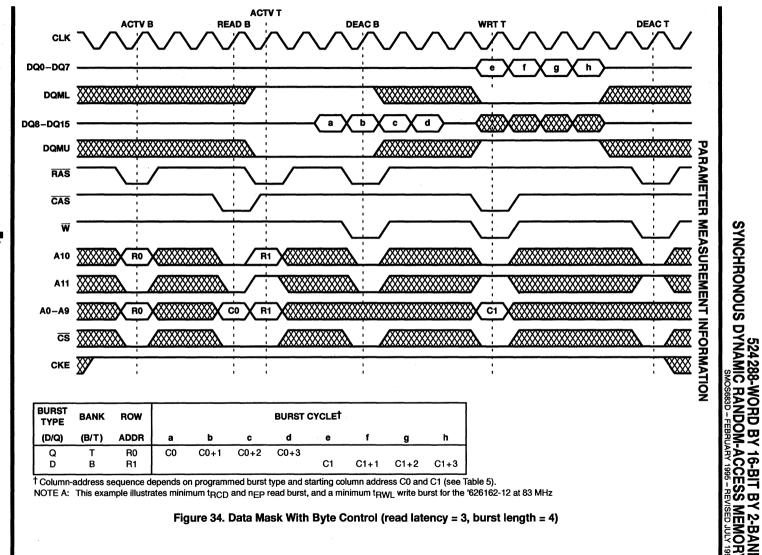


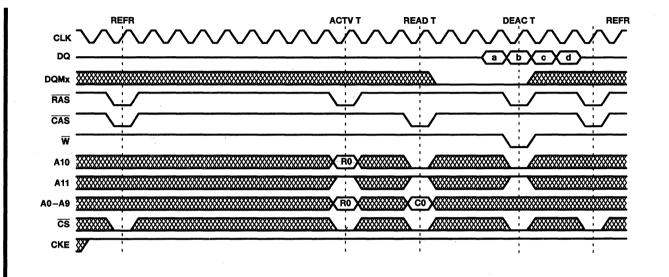
Figure 34. Data Mask With Byte Control (read latency = 3, burst length = 4)

16-BIT

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TMS626162

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BURST TYPE	BANK	ROW	BURST CYCLE†				
(D/Q)	(B/T)	ADDR	а	b	c	d	
Q	Т	R0	C0	C0+1	C0+2	C0+3	

<sup>†</sup> Column-address sequence depends on programmed burst type and starting column address C0 (see 5). NOTE A: This example illustrates minimum  $t_{RC}$ ,  $t_{RCD}$ , and  $n_{EP}$  for the '626162-12 at 83 MHz.

Figure 36. Refresh Cycles (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

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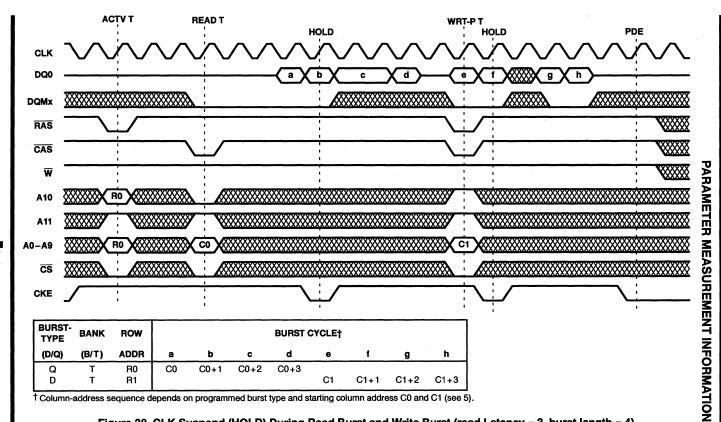


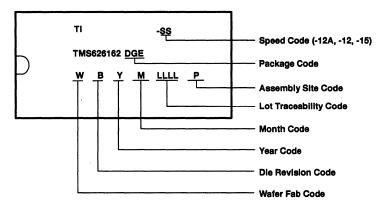
Figure 38. CLK Suspend (HOLD) During Read Burst and Write Burst (read Latency = 3, burst length = 4)

SYNCHRONOUS DYNAMIC 524 288-WORD RANDO ACCESS TMS626162 MEMOR' 2-B ANK

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## TMS626162 524288-WORD BY 16-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY SMOS663D - FEBRUARY 1995 - REVISED JULY 1996

## device symbolization





DGE PACKAGE (TOP VIEW)

44 🛛 V<sub>SS</sub>

43 DQ7

42 VSSQ

41 DQ6

40 VCCQ

39 🛛 DQ5

38 VSSQ

37 DQ4 36 🛛 V<sub>CCQ</sub>

35 🛛 NC

34 🛛 NC

33 DQM

32 CLK

31 CKE

30 🛛 NC 29 A9

28 A8

27 🛛 A7 26 🗋 A6

25 🛛 A5

|--|

٠	<b>Organization 1M</b> $\times$ 8 $\times$ 2 Banks	DG	iE F
•	3.3-V Power Supply (±10% Tolerance)	(*	тоі
•	Two Banks for On-Chip Interleaving (Gapless Accesses)	v <sub>cc</sub> [	1
۲	High Bandwidth – Up to 83-MHz Data Rates		
•	Read Latency Programmable to 1, 2, or 3 Cycles From Column-Address Entry	V <sub>SSQ</sub> [ 3 DQ1 [ 4	4
٠	Burst Sequence Programmable to Serial or Interleave		6
٠	Burst Length Programmable to 1, 2, 4, or 8		
٠	Chip Select and Clock Enable for Enhanced-System Interfacing	DQ3 [] 8 V <sub>CCQ</sub> [] 9	9
•	Cycle-by-Cycle DQ-Bus Mask Capability		
٠	Auto-Refresh and Self-Refresh Capability		12
٠	4K Refresh (Total for Both Banks)		
٠	High-Speed, Low-Noise Low-Voltage TTL	RAS	
	(LVTTL) Interface	CS.[	15
٠	Power-Down Mode	A11 🖸 '	16
•	Compatible With JEDEC Standards	A10 [	17
٠	Pipeline Architecture	A0 []	
•	Employs Enhanced Performance Implanted CMOS (EPIC™) Technology Fabricated by	A1 [] A2 [] 2	19 20

- Texas Instruments (TI™)
- **Temperature Ranges** Operating, 0°C to 70°C Storage, - 55°C to 150°C
- **Performance Ranges:**

		ACTV	
	SYNCHRONOUS	COMMAND TO	REFRESH
	CLOCK CYCLE	READ OR WRITE	TIME
	TIME	COMMAND	INTERVAL
	<sup>t</sup> CK	<sup>t</sup> RCD	<sup>t</sup> REF
	(MIN)	(MIN)	(MAX)
'626812-12/	A 12 ns	30 ns	64 ms
'626812-12	12 ns	30 ns	64 ms
'626812-15	15 ns	30 ns	64 ms

## description

The TMS626812 series of devices are high-speed 16777216-bit synchronous dynamic randomaccess memories (SDRAMs) organized as two banks of 1048576 words with eight bits per word.

All inputs and outputs of the TMS626812 series are compatible with the LVTTL interface.

	A3 [ 21 24 ] A4 V <sub>CC</sub> [ 22 23 ] V <sub>SS</sub>
	PIN NOMENCLATURE
A0-A10	Address Inputs A0-A10 Row Addresses A0-A8 Column Addresses
A11 CAS CKE CLK CS DQ0-DQ7 DQM NC RAS VCC VCCQ VSS VCCQ VSS VSSQ W	A10 Automatic-Precharge Select Bank Select Column-Address Strobe Clock Enable System Clock Chip Select SDRAM Data Input/Data Output Data/Output Mask Enable No External Connect Row-Address Strobe Power Supply (3.3 V Typ) Power Supply for Output Drivers (3.3 V Typ) Ground Ground for Output Drivers Write Enable

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# operation (continued)

COMMAND	STATE OF BANK(S)	<del>cs</del>	RAS	CAS	w	A11	A10	A9-A0	MNEMONIC
Mode register set	T ≖ deac B = deac	L	L	L	L	x	x	A9 = V A8-A7 = 0 A6-A0 = V	MRS
Bank deactivate (precharge)	X	L	L	н	L	BS	L	X	DEAC
Deactivate all banks	X	L	L	н	L	X	н	X	DCAB
Bank activate / row-address entry	SB = deac	L	L	н	н	BS	V	V	ACTV
Column-address entry/write operation	SB = actv	L	н	L	L	BS	L	V	WRT
Column-address entry/write operation with automatic deactivate	SB = actv	L	н	L	L	BS	н	v	WRT-P
Column-address entry/read operation	SB = actv	L	н	L	н	BS	L	V	READ
Column-address entry/read operation with automatic deactivate	SB = actv	L	н	L	н	BS	н	V .	READ-P
Burst stop	SB = actv	L	н	н	L	X	X	X	STOP
No operation	х	L	н	н	н	x	x	X	NOOP
Control-input inhibit / no operation	X	н	X	X	X	X	x	X	DESL
Auto-refresh‡	T = deac B = deac	L	L	L	н	x	x	x	REFR

#### Table 1. Basic-Command Truth Table<sup>†</sup>

<sup>†</sup> For exception of these commands on cycle n:

- CKE(n-1) must be high, or

- tCESP must be satisfied for power-down exit, or

- tCESP and tRC must be satisfied for self-refresh exit, or

 $-t_{CES}$  and  $n_{CLE}$  must be satisfied for clock-suspend exit. DQM(n) is a don't care.

+ Auto-refresh or self-refresh entry requires that all banks be deactivated or in an idle state prior to the command entry.

Legend: n

- CLK cycle number =
- Logic low L =

н Logic high -

- Don't care, either logic low or logic high х v
- Valid т
  - Bank T =
- Bank B в =
- actv = Activated

deac = Deactivated

- BS = Logic high to select bank T; logic low to select bank B
- SB = Bank selected by A11 at cycle n



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## operation (continued)

COMMAND	STATE OF BANK(S)	DQM (n)	DATA IN (n)	DATA OUT (n+2)	MNEMONIC
_	T = deac and B = deac	x	N/A	Hi-Z	
-	T = actv and B = actv (no access operation)‡	X	N/A	Hi-Z	_
Data-in enable	T = write or B = write	L	v	N/A	ENBL
Data-in mask	T = write or B = write	н	м	N/A	MASK
Data-out enable	T = read or B = read	L	N/A	v	ENBL
Data-out mask	T = read or B = read	н	N/A	Hi-Z	MASK

#### Table 3. DQM-Use Command Truth Table<sup>†</sup>

<sup>†</sup> For exception of these commands on cycle n:

- CKE(n-1) must be high, or

- tCESP must be satisfied for power-down exit, or

- tCESP and tRC must be satisfied for self-refresh exit, or

 $-t_{CES}$  and  $n_{CLE}$  must be satisfied for clock-suspend exit. CS(n), RAS(n), CAS(n), W(n), and A0-A11(n) are don't cares

+ A bank is no longer in an access operation one cycle after the last data-out cycle of a read operation, and two cycles after the last data-in cycle of a write operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a write operation.

#### Legend:

- CLK cycle number n
- = Logic low L
- н Logic high =
- х Don't care, either logic low or logic high
- v Valid
- м Masked input data
- Not applicable N/A =
- Bank T т -
- в = Bank B
- actv = Activated
- deac = Deactivated
- write = Activated and accepting data in on cycle n
- read = Activated and delivering data out on cycle (n + 2)



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## burst sequence (continued)

	[					NTER	NAL CO	OLUMI	ADDRE	SS A2-	-A0					
			l	DECIM	AL				BINARY							
	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH
	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	2	3	4	5	6	7	0	001	010	011	100	101	110	111	000
	2	3	4	5	6	7	0	1	010	011	100	101	110	111	000	001
Serial	3	4	5	6	7	0	1	2	011	100	101	110	111	000	001	010
Sella	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	6	7	0	1	2	3	4	101	110	111	000	001	010	011	100
×	6	7	0	1	2	3	4	5	110	111	000	001	010	011	100	101
	7	0	1	2	3	4	5	6	111	000	001	010	011	100	101	110
	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	0	3	2	5	4	7	6	001	000	011	010	101	100	111	110
	2	3	0	1	6	- 7	4	5	010	011	000	001	110	111	100	101
Interleave	3	2	1	0	7	6	5	4	011	010	001	000	111	110	101	100
Interioave	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	4	7	6	1	0	3	2	101	100	111	110	001	000	011	010
	6	7	4	5	2	3	0	1	110	111	100	101	010	011	000	001
	7	6	5	4	3	2	1	0	111	110	101	100	011	010	001	000

#### **Table 6. 8-Bit Burst Sequences**

#### latency

The beginning data-out cycle of a read burst can be programmed to occur 1, 2, or 3 CLK cycles after the read command (see the section on setting the mode register, page 5–59). This feature allows the user to adjust the '626812 to operate in accordance with the system's capability to latch the data output from the '626812. The delay between the READ command and the beginning of the output burst is known as read latency (also known as CAS latency). After the initial output cycle begins, the data burst occurs at the CLK frequency without any intervening gaps. Use of minimum read latencies is restricted based on the particular maximum frequency rating of the '626812.

There is no latency for data-in cycles (write latency). The first data-in cycle of a write burst is entered at the same rising edge of CLK on which the WRT command is entered. The write latency is fixed and is not determined by the mode-register contents.

#### two-bank operation

The '626812 contains two independent banks that can be accessed individually or in an interleaved fashion. Each bank must be activated with a row address before it can be accessed. Each bank must then be deactivated before it can be activated again with a new row address. The bank-activate/row-address-entry command (ACTV) is entered by holding RAS low, CAS high, W high, and A11 valid on the rising edge of CLK. A bank can be deactivated either automatically during a READ-P or a WRT-P command or by use of the deactivate-bank (DEAC) command. Both banks can be deactivated at once by use of the DCAB command (see Table 1 and the section on bank deactivation description, page 5–58).



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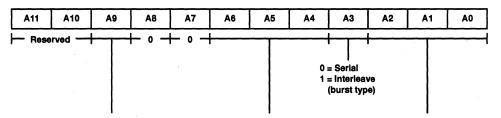
#### CLK suspend/power-down mode (continued)

as a CLK-suspend operation, and its execution is denoted as a HOLD command. The device resumes operation from the point at which it was placed in suspension, beginning with the second rising edge of CLK after CKE returns high.

If CKE is brought low when no read or write command is in progress, the device enters power-down mode. If both banks are deactivated when power-down mode is entered, power consumption is reduced to the minimum. Power-down mode can be used during row-active or auto-refresh periods to reduce input buffer power. After power-down mode is entered, no further inputs are accepted until CKE returns high. To ensure that data in the device remains valid during the power-down mode, the self-refresh command (SLFR) must be executed concurrently with the power-down entry (PDE) command. When exiting power-down mode, new commands can be entered on the first CLK edge after CKE returns high, provided that the setup time (t<sub>CESP</sub>) is satisfied. Table 2 shows the command configuration for a CLK suspend/power-down operation, and Figure 19, Figure 20, and Figure 38 show an example of the procedure.

#### setting the mode register

The '626812 contains a mode register that must be programmed with the read latency, the burst type, and the burst length. This is accomplished by executing a mode-register set (MRS) command with the information entered on address lines AO-A9. A logic 0 must be entered on A7 and A8, but A10 and A11 are don't-care entries for the '626812. When A9=1, the write-burst length is always 1. When A9=0, the write-burst length is defined by AO-A2. Figure 1 shows the valid combinations for a successful MRS command. Only valid addresses allow the mode register to be changed. If the addresses are not valid, the previous contents of the mode register remain unaffected. The MRS command is executed by holding RAS, CAS, and W low, and the input-mode word valid on AO-A9 on the rising edge of CLK (see Table 1). The MRS command can be executed only when both banks are deactivated.



REGISTER	WRITE-BURST
BIT A9	LENGTH
0	A2-A0
1	1

STER B	READ	
A5	A4	LATENCY <sup>‡</sup>
0 1 1	1 0 1	1 2 3
		A5         A4           0         1           1         0           1         1

REG	ISTER B	BURST	
A2	A1	A0	LENGTH
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8

 <sup>†</sup> All other combinations are reserved.
 <sup>‡</sup> Refer to timing requirements for minimum valid-read latencies based § All other combinations are reserved.

Figure 1. Mode-Register Programming

on maximum frequency rating.

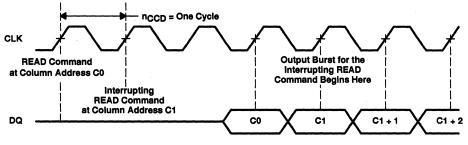


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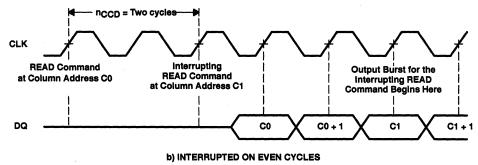
## interrupted bursts (continued)

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING READ BURST
READ, READ-P	Current output cycles continue until the programmed latency from the superseding READ (READ-P) command is met and new output cycles begin (see Figure 2).
WRT, WRT-P	The WRT (WRT-P) command immediately supersedes the read burst in progress. To avoid data contention, DQM must be high before the WRT (WRT-P) command to mask output of the read burst on cycles ( $n_{CCD}$ -1), $n_{CCD}$ , and ( $n_{CCD}$ +1) assuming that there is any output on these cycles. For read latency = 1, read burst interruption by WRT (WRT-P) command is not allowed at $n_{CCD}$ = 1, 2 (see Figure 3).
DEAC, DCAB	The DQ bus is in the high-impedance state when n <sub>HZP</sub> cycles are satisfied or when the read burst completes, whichever occurs first (see Figure 4).
STOP	The DQ bus is in the high-impedance state when nBSD cycles are satisfied or when the read burst completes, whichever occurs first. The bank remains active. A new read or write command cannot be entered for at least two cycles after the STOP command (see Figure 5).

#### **Table 7. Read-Burst Interruption**



a) INTERRUPTED ON ODD CYCLES



NOTE A: For these examples assume read latency = 3, and burst length = 4.

Figure 2. Read Burst Interrupted by Read Command

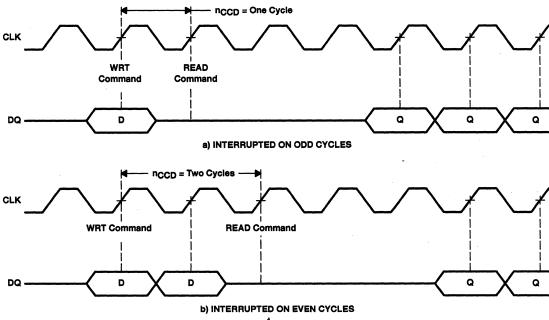


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# interrupted bursts (continued)

Table	8.	Write-Burst Interruption
IUNIO	ς.	

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING WRITE BURST
READ, READ-P	Data in on previous cycle is written. No further data in is accepted (see Figure 6).
WRT, WRT-P	The new WRT (WRT-P) command and data in immediately supersede the write burst in progress (see Figure 7).
DEAC, DCAB	The DEAC/DCAB command immediately supersedes the write burst in progress. DQM must be used to mask the DQ bus such that the write recovery specification ( $t_{RWL}$ ) is not violated by the interrupt (see Figure 8).
STOP	The data on the input pins at the time of the burst STOP command is not written, and no further data is accepted. The bank remains active. A new read or write command cannot be entered for at least nBSD cycles after the STOP command (see Figure 9).



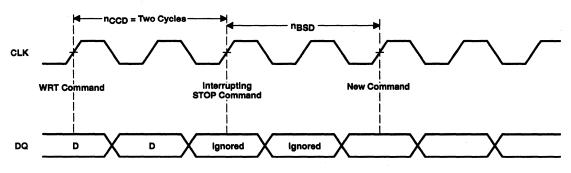
NOTE A: For these examples assume read latency = 3, burst length = 4.

## Figure 6. Write Burst Interrupted by Read Command



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#### interrupted bursts (continued)



NOTE A: For this example assume burst length = 4.

#### Figure 9. Write Burst Interrupted by STOP Command

#### power up

Device initialization should be performed after a power up to the full  $V_{CC}$  level. After power is established, a 200-µs interval is required (with no inputs other than CLK). After this interval, both banks of the device must be deactivated. Eight REFR commands must be performed, and the mode register must be set to complete the device initialization.



electrical characteristics over recommended ranges of supply vo	Itage and free-air temperature (unless otherwise noted)
(see Note 2)	

	PARAMETER	TEST CONDITIONS					2-12A	· '626812-12		'626812-15		UNIT	
			. 201			MIN	MAX	MIN	MAX	MIN	MAX	0111	
VOH	High-level output voltage	$I_{OH} = -2 \text{ mA}$				2.4		2.4		2.4		v	
VOL	Low-level output voltage	I <sub>OL</sub> = 2 mA	OL = 2 mA				0.4		0.4		0.4	v	
կ	input current (leakage)	$0 \; V \leq V_I \leq V_{CC}$	$V \le V_I \le V_{CC} + 0.3 V$ , All other pins = 0 V to $V_{CC}$				±10		±10		±10	μA	
lo	Output current (leakage)	$0 \text{ V} \leq \text{V}_O \leq \text{V}_C($	; + 0.3 V, O	utput disabled			±10		±10		±10	μA	
I <sub>CC1</sub> Average read or write current			One bank active	Burst length = 1 or 2		85		85		75			
	t <sub>RC</sub> = MIN,	t <sub>CK</sub> = MIN,	One bank active	Burst length = 4 or 8		105		105		90	mA		
	Read latency = 3	3	Two banks active interleaving	Burst length = 1 or 2		140		140		120			
				Burst length = 4 or 8		165		165		135	<u>ن</u> ا		
		CKE=VIH			25		25		20	mA			
		Both banks deactivated	CKE=VIL				2		2			2	
ICC2	Standby current	doublivalou	CKE = 0 V (CM	OS)	S)				1			1	
		1 or 2 banks	CKE=VIH	ЖЕ=V <sub>IH</sub>			30		30			25	
		active CKE=VIL					8		8		8	1117	
ICC3	Consecutive CBR commands	t <sub>RC</sub> = MIN		,			80		80		70	m/	
		107/1010			Read latency = 1		60		60		50		
ICC4	Burst current, gapless burst	ACTV not allow Two bank interle		cκ = MIN,	Read latency = 2		120		100		90	mA	
		Read latency = 3			Read latency = 3		140		140		120		
	Colf refresh current	CKE = VIL					2		2		2		
CC6	Self-refresh current	CKE = 0 V (CMOS)					1		1		1	m,	

NOTE 2: All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.

·

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## ac timing requirements over recommended ranges of supply voltage and operating free-air temperature<sup>†‡</sup>

		'62681	2-12A	'6268 <sup>.</sup>	12-12	'6268'	2-15	
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
tRAS	ACTV command to DEAC or DCAB command	60	100 000	72	100 000	75	100 000	ns
tRCD	ACTV command to READ or WRT command (see Note 8)	30		30		30		ns
t <sub>RP</sub>	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR command	36		36		45		ns
<sup>t</sup> APR	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command			t <sub>RP</sub> + (n <sub>E</sub>	P + tCK)	1		ns
tAPW	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command	60		60		75	i	ns
tRWL	Final data in to DEAC or DCAB command	18		20		30		ns
tRRD	ACTV command for one bank to ACTV command for the other bank	24		24		30		ns
tŢ	Transition time, all inputs (see Note 9)	1	5	1	5	1	5	ns
tREF	Refresh interval		64		64		64	ms

† See Parameter Measurement Information for load circuits.

<sup>‡</sup> All references are made to the rising transition of CLK, unless otherwise noted.

NOTES: 8. For read or write operations with automatic deactivate, tRCD must be set to satisfy minimum tRAS.

9. Transition time,  $t_T$ , is measured between V<sub>IH</sub> and V<sub>IL</sub>.



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# Table 9. Number of Cycles Required to Meet Minimum Specification for Key Timing Parameters

			TMS	626812	-12A	TMS626812-12			TMS626812-15			UNITS			
	Operating frequency		83	66	50	83	66	50	66	50	33	MHz			
tCK	Cycle time, CLK (system clock)		12	15	20	12	15	20	15	20	30	ns			
	KEY PARAMETER				NUMBER OF CYCLES REQUIRED										
	Read latency, minimum programmed value			2	2	3	3	2	3	2	2	cycles			
tRCD	ACTV command to READ or WRT command			2	2	3	2	2	2	2	1	cycles			
tRAS	ACTV command to DEAC or DCAB command			4	3	6	5	4	5	4	3	cycles			
tRP	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR command			3	2	3	3	2	3	3	2	cycles			
<sup>t</sup> RC	REFR command to ACTV, MRS, or REFR command; self-refresh exit to ACTV, MRS, SLFR, or REFR command		8	7	5	9	8	6	8	6	4	cycles			
tRWL	Final data in to DEAC or DCAB comman	ld	2	2	1	3	2	1	2	2	1	cycles			
tRRD	ACTV command for one bank to ACTV command for the		2	2	2	2	2	2	2	2	1	cycles			
		Read latency = 1	-	—	-	-	-	—	-	-		cycles			
tAPR	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command	Read latency = 2	_	2	1	—	-	1	_	2	1	cycles			
~		Read latency = 3	1	1	0	1	1	0	1	1	0	cycles			
tAPW	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command		5	4	3	5	4	3	5	4	3	cycles			

<sup>†</sup> All references are made to the rising transition of CLK, unless otherwise noted.



## PARAMETER MEASUREMENT INFORMATION

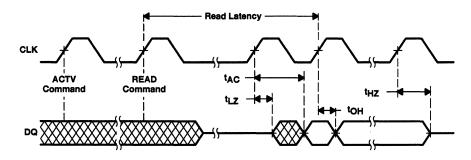
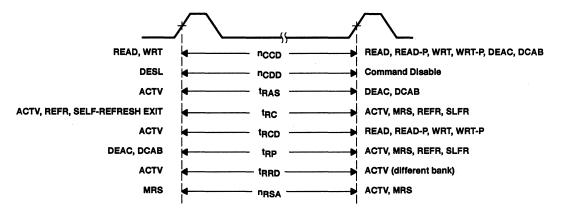


Figure 12. Output Parameters



#### Figure 13. Command-to-Command Parameters



#### PARAMETER MEASUREMENT INFORMATION

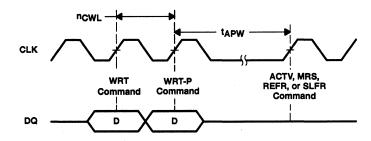
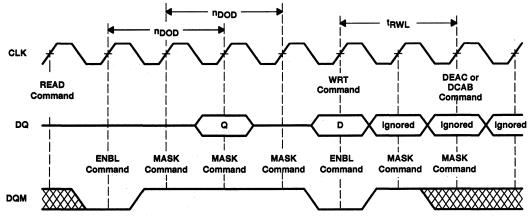


Figure 17. Write With Auto-Deactivate

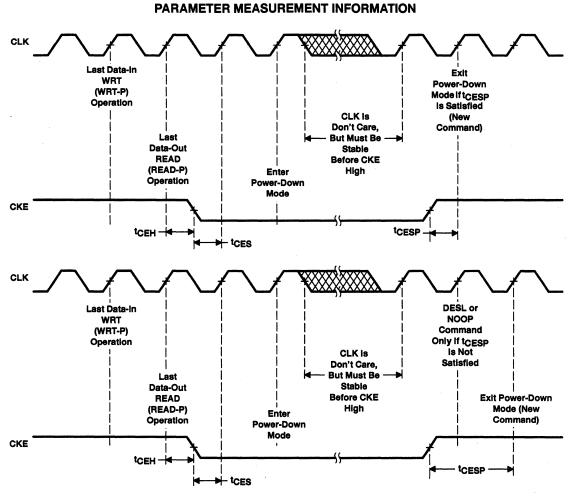


NOTE A: For this example assume read latency = 3, and burst length = 4.

Figure 18. DQ Masking

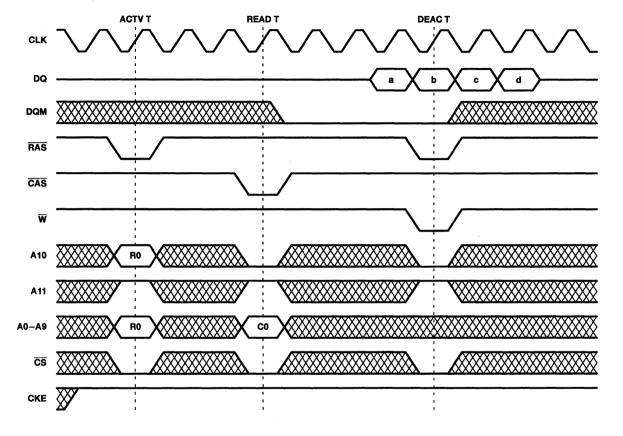


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## Figure 20. Power-Down Operation





BURST TYPE	BANK	ROW	BURST CYCLET						
(D/Q)	(B/T)	ADDR	а	b	c	d			
Q	Т	R0	C0	C0 + 1	C0 + 2	C0 + 3			

<sup>†</sup> Column-address sequence depends on programmed burst type and starting column address C0 (see Table 5). NOTE A: This example illustrates minimum  $t_{RCD}$  and  $n_{EP}$  for the '626812-12 at 83 MHz.

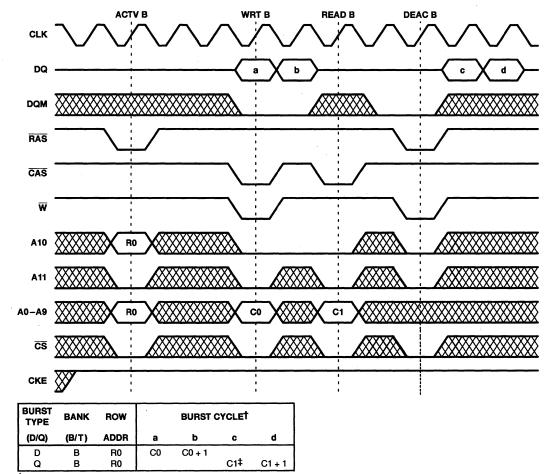
Figure 22. Read Burst (read latency = 3, burst length = 4)

TMS626812 1048576-WORD BY 8-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY SMOSBB7 - JULY 1996

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<sup>†</sup> Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 4). NOTE A: This example illustrates minimum t<sub>RCD</sub>, n<sub>CWL</sub>, and n<sub>EP</sub> for the '626812-12 at 83 MHz.

Figure 24. Write-Read Burst (read latency = 3, burst length = 2)

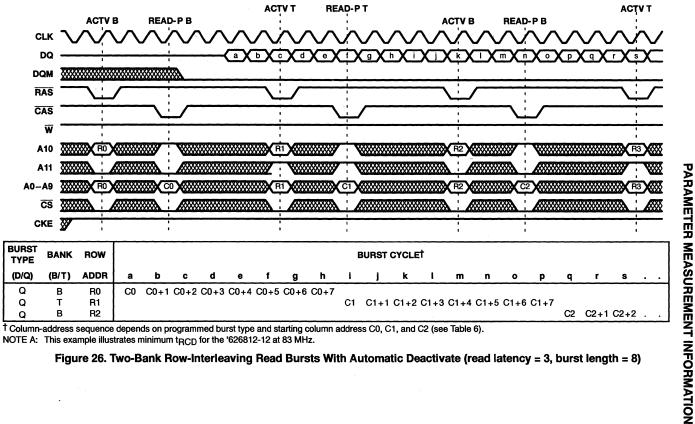
PARAMETER MEASUREMENT INFORMATION 1048576-WORD BY 8-BIT BY SYNCHRONOUS DYNAMIC RANDOM-ACCESS N SMOSE

TMS626812

2-BAN

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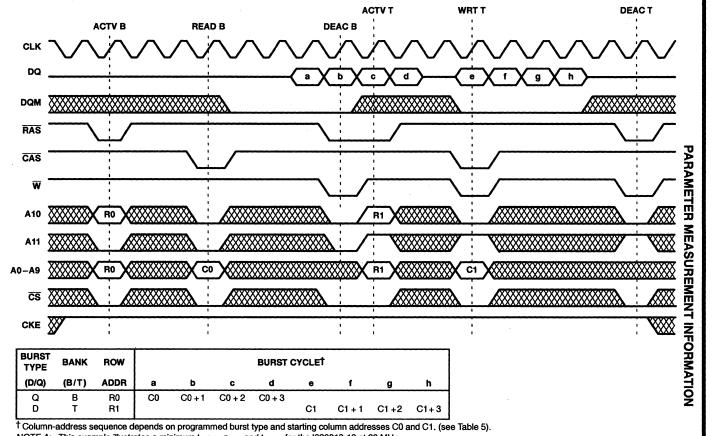
<sup>†</sup> Column-address sequence depends on programmed burst type and starting column address C0, C1, and C2 (see Table 6).

NOTE A: This example illustrates minimum t<sub>RCD</sub> for the '626812-12 at 83 MHz.

Figure 26. Two-Bank Row-Interleaving Read Bursts With Automatic Deactivate (read latency = 3, burst length = 8)

5-83

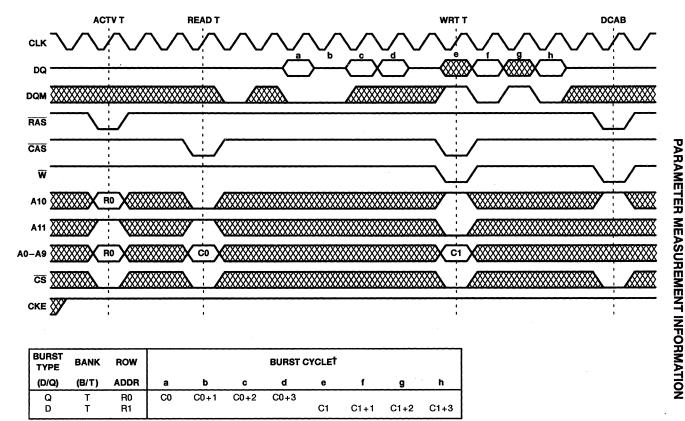
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NOTE A: This example illustrates a minimum tRCD, nEP, and tRWL for the '626812-12 at 83 MHz.

Figure 28. Read-Burst Bank B, Write-Burst Bank T (read latency = 3, burst length = 4)

5-85



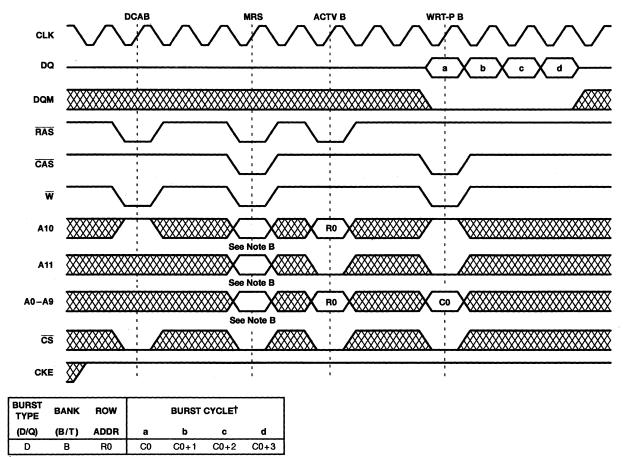
<sup>+</sup>Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 5). NOTE A: This example illustrates minimum t<sub>RCD</sub> for the '626812-12 at 83 MHz.

Figure 30. Data Mask (read latency = 3, burst length = 4)

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<sup>†</sup>Column-address sequence depends on programmed burst type and starting column address C0 (see Table 5).

NOTES: A. This example illustrates minimum tRP, nRSA, and tRCD for the '626812-12 at 83 MHz.

B. Refer to Figure 1

Figure 32. Set Mode Register (deactivate all, set mode register, write burst with automatic deactivate) (burst length = 4)

TMS626812 1048576-WORD BY 8-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY SMOSGEF - JULY 199

PARAMETER MEASUREMENT INFORMATION

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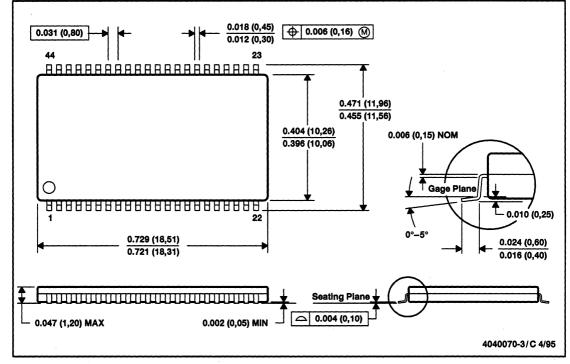
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#### **MECHANICAL DATA**

## PLASTIC SMALL-OUTLINE PACKAGE



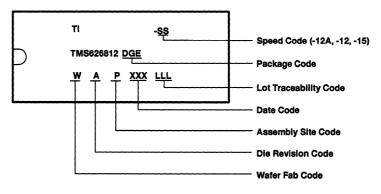
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion.

#### device symbolization

DGE (R-PDSO-G44)





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 Organization . . . 1M x 16 x 4 Banks 2M x 8 x 4 Banks 4M x 4 x 4 Banks

- 3.3-V Power Supply (±10% Tolerance)
- Four Banks for On-Chip Interleaving for x4/x8/x16 (Gapless Access) Depending on Organizations
- High Bandwidth Up to 100-MHz Data Rates
- Burst Length Programmable to 1, 2, 4, 8, or Full Page
- Programmable Output Sequence Serial or Interleave
- Chip Select and Clock Enable for Enhanced-System Interfacing
- Cycle-by-Cycle DQ Bus Mask Capability
- Only x16 SDRAM Configuration Supports
   Upper-/Lower-Byte Masking Control
- Programmable Read Latency From Column Address
- Pipeline Architecture (Single-Cycle Architecture)
- Single Write/Read Burst
- Self-Refresh Capability (every 16 μs)

#### description

The TMS664xx4 series are high-speed, 67108864-bit synchronous dynamic random-access memories (SDRAMs), which are organized as follows:

- Four banks of 1 048 576 words with 16 bits per word
- Four banks of 2097152 words with 8 bits per word
- Four banks of 4194304 words with 4 bits per word

All inputs and outputs of the TMS664xx4 series are compatible with the LVTTL interface.

The SDRAM employs state-of-the-art enhanced performance implanted CMOS (EPIC™) technology for high-performance, reliability, and low power. All inputs and outputs are synchonized with the CLK input to simplify system design and to enhance use with high-speed microprocessors and caches.

The TMS664xx4 SDRAM is available in a 400-mil, 54-pin surface-mount thin small-outline package (TSOP) (II) (DGE suffix).

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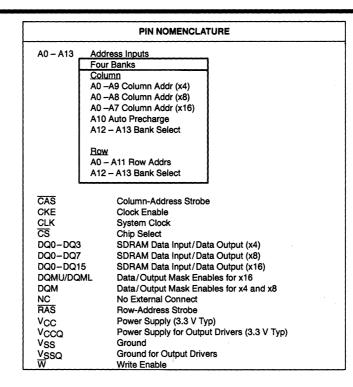


- High-Speed, Low-Noise Low-Voltage Transistor-Transistor Logic (LVTTL) Interface
- Power-Down Mode
- Compatible With JEDEC Standards
- 16K RAS-Only Refresh (Total for All Banks)
- 4K Auto Refresh (Total for All Banks)/64 ms
- Automatic Precharge and Controlled Precharge
- Burst Interruptions Supported
  - Read Interruption
  - Write Interruption
  - Stop Interruption
  - Precharge Interruption
- Support Clock-Suspend Operation (Hold Command)
- Performance Ranges:

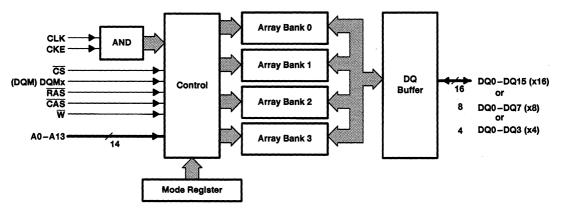
		ACTV	
	SYNCHRONOUS	COMMAND TO	REFRESH
	CLOCK CYCLE	READ OR WRT	TIME
	TIME	COMMAND	INTERVAL
	<sup>t</sup> CK	<sup>t</sup> RCD	<sup>t</sup> REF
•	(MIN)	(MIN)	(MAX)
'664xx4-10	10 ns	30 ns	64 ms
'664xx4-12	12 ns	35 ns	64 ms

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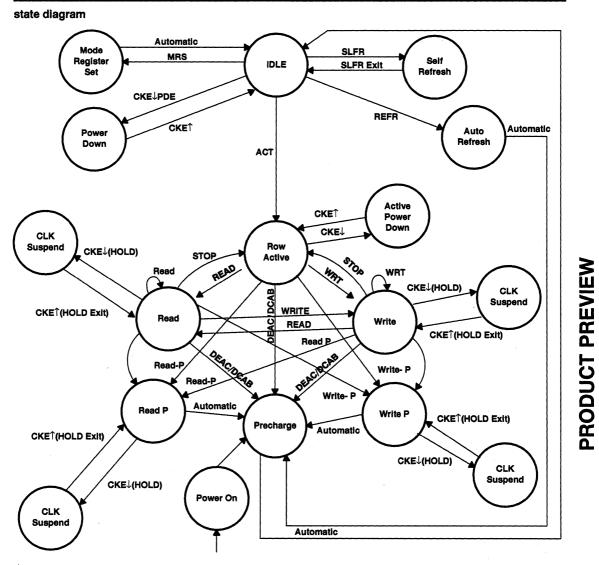
## functional block diagram (four banks)





**PRODUCT PREVIEW** 

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## operation (continued)

# Table 2. CKE-Use Command Truth Table<sup>†</sup>

COMMAND	STATE OF BANK(S)	CKE (n-1)	CKE (n)	CS (n)	RAS (n)	CAS (n)	W (n)	MNEMONIC
Self-refresh entry	All Banks = deac	H,	L	L	L	L	н	SLFR
Power-down entry at n + 1 <sup>‡</sup>	All Banks = no access operation§	н	L	×	x	x	х	PDE
Self-refresh exit	All Banks =	L	н	L	н	н	н	—
	self-refresh	L	н	н	X	X	X	-
Power-down exit <sup>¶</sup>	All Banks = power down	L	н	x	×	x	x	-
CLK suspend at n + 1	All Banks = access operation§	н	L	x	x	x	x	HOLD
CLK suspend exit at n + 1	All Banks = access operation\$	L	н	x	x	x	x	-

<sup>†</sup> For execution of these commands, A0-A13 (n) and DQMx (n) are don't cares.

<sup>‡</sup>On cycle n, the device executes the respective command (listed in Table 1). On cycle (n+1), the device enters the power-down mode.

\$ A bank is no longer in an access operation one cycle after the last data-out cycle of a READ (READ-P) operation, and two cycles after the last data-in cycle of a WRT (WRT-P) operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a WRT (WRT-P) operation.

If setup time from CKE high to the next CLK high satisfies t<sub>CESP</sub>, the device executes the respective command (listed in Table 1). Otherwise, either DESL or NOOP command must be applied before any other command.

Legend: n

CLK cycle number

L = Logic low

H = Logic high

X = Don't care (either logic high or logic low)

deac = Deactivated



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#### burst sequence

All data for the '664xx4 is written or read in a *burst* fashion. That is, a single starting address is entered into the device and then the '664xx4 internally accesses a sequence of locations based on that starting address. Some of the subsequent accesses after the first one can be at preceding, as well as succeeding, column addresses, depending on the starting address entered. This sequence can be programmed to follow either a serial burst or an interleave burst (see Table 4 through Table 6). The length of the burst sequence can be user-programmed to be 1, 2, 4, 8, or full page [256 (x16), 512 (x8), 1024 (x4)] accesses. After a read burst is completed (as determined by the programmed burst length), the outputs are in the high-impedance state until the next read access is initiated.

	INTERNAL COLUMN ADDRESS A0					
	DECI	MAL	BINARY			
	START	2ND	START	2ND		
Serial	0	1	0	1		
Senai	1	0	1	0		
Interleave	0	1	0	1		
Interleave	1	0	1	0		

#### Table 5. 4-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A1-A0							
	DECIMAL			BINARY				
1	START	2ND	3RD	4TH	START	2ND	3RD	4TH
	0	1	2	3	00	01	10	11
Serial	1	2	3	0	01	10	11	00
Serial	2	3	0	1	10	11	00	.01
	3	0	1	2	11	00	01	10
	0	1	2	3	00	01	10	11
Interleave	1	0	3	2	01	00	11	10
meneave	2	3	0	1	10	11	00	01
	3	2	1	0	11	10	01	00



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#### four-bank row-access operation

One of the features of the four-bank operation is access to information on random rows at a higher rate of operation than is possible with a standard DRAM. This can be accomplished by activating one of the banks with a row address and, while the data stream is being accessed to/from that bank, activating one of the other banks with other row addresses. When the data stream to/from the first activated bank is complete, the data stream to/from the second activated bank can begin without interruption. After the second bank is activated, the first bank can be deactivated to allow the entry of a new row address for the next round of accesses or the entry of new row addresses for other banks which currently are deactivated. In this manner, operation can continue in an interleaved fashion. Figure 30 is an example of four-bank row-interleaving read bursts with automatic deactivate with a read latency of 3 and a burst length of 8.

#### four-bank column-access operation

The availability of four banks allows the access of data from random starting columns between banks at a higher rate of operation. After activating each bank with a row address (ACTV command), A12–A13 for the four-bank column-access operation can be used to alternate READ or WRT commands between the banks to provide gapless accesses at the CLK frequency, provided all specified timing requirements are met. Figure 31 is an example of four-bank column-interleaving read bursts with a read latency of 3 and a burst length of 2.

#### bank deactivation (precharge)

All banks can be deactivated simultaneously (placed in precharge) by using the DCAB command. A single bank can be deactivated by using the DEAC command. The DEAC command is entered identically to the DCAB command except that A10 must be low and A12–A13 selects the bank to be precharged as shown in Table 1. Figure 26 and Figure 34 provide examples. A bank also can be deactivated automatically by using A10 during a READ or WRT command. If A10 is held high during the entry of a READ or WRT command, the accessed bank, selected by A12–A13 for the 4-bank option, is automatically deactivated upon completion of the access burst. If A10 is held low during READ- or WRT-command entry, that bank remains active following the burst. The READ and WRT commands with automatic deactivation are denoted as READ-P and WRT-P. See Figure 29 for an example.

#### chip select

CS (chip select) can be used to select or deselect the '664xx4 for command entry which might be required for multiple-memory-device decoding. If CS is held high on the rising edge of CLK (DESL command), the device does not respond to RAS, CAS, or W until the device is selected again. Device select is accomplished by holding CS low on the rising edge of CLK. Any other valid command can be entered simultaneously on the same rising CLK edge of the select operation. The device can be selected/deselected on a cycle-by-cycle basis (see Table 1 and Table 2). Using CS does not affect an access burst that is in progress; the DESL command can restrict only RAS, CAS, and W input to the '664xx4.



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#### setting the mode register

The '664xx4 contains a mode register that should be user-programmed with the read latency, the burst type, and the burst length. This is accomplished by executing an MRS command with the information entered on address lines A0–A9. A logic 0 must be entered on A7 and A8, but A10–A13 are don't care entries for the '664xx4. When A9 = 1, the write burst length is always 1. When A9 = 0, the write burst length is defined by A2–A0. Figure 1 shows the valid combinations for a successful MRS command. Only valid addresses allow the mode register to be changed. If the addresses are not valid, the previous contents of the mode register remain unaffected. The MRS command is executed by holding RAS, CAS, and W low and the input-mode word valid on A0–A9 on the rising edge of CLK (see Table 1). The MRS command can be executed only when all banks are deactivated. See Figure 22 and Figure 36 for examples.

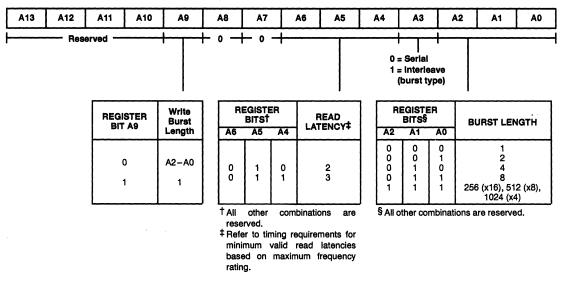


Figure 1. Mode-Register Programming

#### refresh

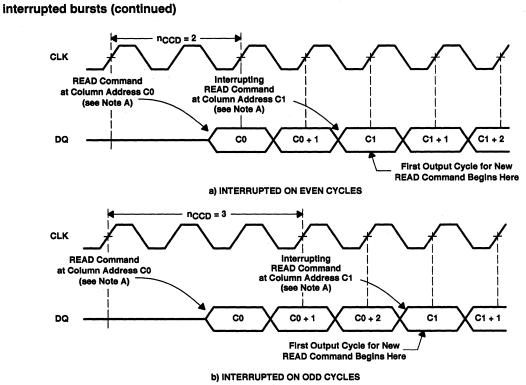
The '664xx4 must be refreshed at intervals not exceeding  $t_{REF}$  (see timing requirements) or data cannot be retained. Refresh can be accomplished by performing an ACTV command (RAS-only refresh) to every row in all banks, by performing 4096 auto-refresh (REFR) commands, or by placing the device in self refresh. Regardless of the method used, refresh must be accomplished before  $t_{REF}$  has expired. See Figure 35 for an example.

#### auto refresh

Before performing an auto refresh, all banks must be deactivated (placed in precharge). To enter a REFR command, RAS and CAS must be low and  $\overline{W}$  must be high upon the rising edge of CLK (see Table 1). The refresh address is generated internally such that after 4096 REFR commands, all banks of the '664xx4 are refreshed. The external address and bank select A12–A13 are ignored. The execution of a REFR command automatically deactivates all banks upon completion of the internal auto-refresh cycle. This allows consecutive REFR-only commands to be executed, if desired, without any intervening DEAC commands. The REFR commands do not necessarily have to be consecutive, but all 4096 must be completed before t<sub>REFF</sub> expires.

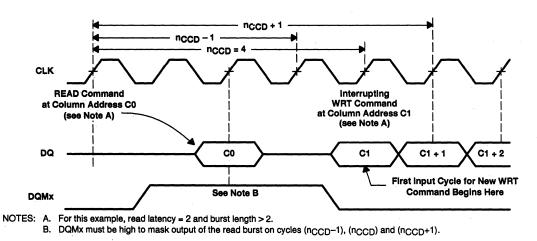


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NOTE A: For this example, assume read latency = 2 and burst length > 2.

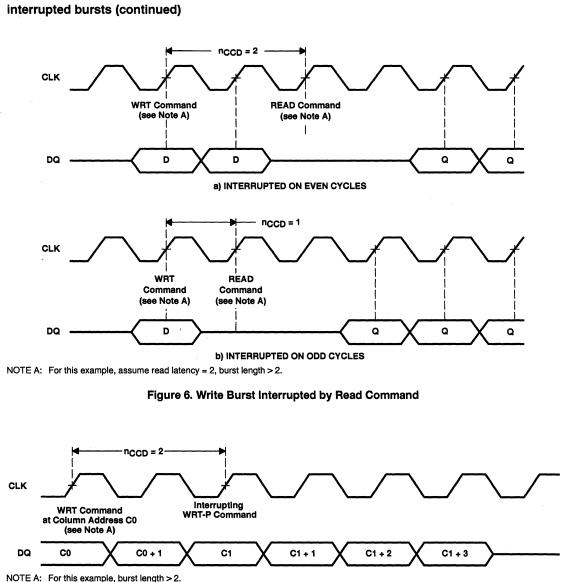








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#### Figure 7. Write Burst Interrupted by Write Command



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absolute maximum rating	as over operatin	a free-air tem	perature range	(unless otherwise noted) <sup>†</sup>
		9		

	•		•	<b>U</b> (	
Supply voltage rang	e, V <sub>CC</sub>			 	– 0.5 V to 4.6 V
Supply voltage rang	e for output	drivers	, V <sub>CCO</sub>	 	– 0.5 V to 4.6 V
Voltage range on ar	y input pin	(see No	te 1)	 	– 0.5 V to 4.6 V
Voltage range on an	y output pir	i (see N	ote 1)	 	0.5 V to V <sub>CC</sub> + 0.5 V
					50 mA
Power dissipation				 	1 W
Operating free-air te	mperature	range, 1	Δ	 	0°C to 70°C
					– 55°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to VSS.

#### recommended operating conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3	3.3	3.6	٧
VCCQ	Supply voltage for output drivers‡	3	3.3	3.6	٧
VSS	Supply voltage		0		V
VSSQ	Supply voltage for output drivers		0		٧
VIH	High-level input voltage	2		V <sub>CC</sub> + 0.3	V
VIL	Low-level input voltage	- 0.3		0.8	٧
TA	Operating free-air temperature	0		70	°C
		L			4

 $V_{CCQ} \leq V_{CC} + 0.3 V$ 



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# capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

		MIN	MAX	UNIT
C <sub>i(S)</sub>	Input capacitance, CLK input		5	рF
Ci(AC)	Input capacitance, address and control inputs: A0-A13, CS, DQMx, RAS, CAS, W		5	pF
C <sub>i(E)</sub>	Input capacitance, CKE input		5	pF
Co	Output capacitance		7	pF

NOTE 4: V<sub>CC</sub> =  $3.3 \pm 0.3$  V and bias on pins under test is 0 V.

# ac timing requirements over recommended ranges of supply voltage and operating free-air temperature<sup>†‡</sup>

			'664 <u>)</u>	x4-10	'664	xx4-12	UNIT
			MIN	MAX	MIN	MAX	UNIT
+	Cycle time, CLK (system clock)	Read latency = 2	15		18		
<sup>t</sup> CK	Cycle time, CLK (System Clock)	Read latency = 3	10		12		ns
<sup>t</sup> CKH	Pulse duration, CLK (system clock) high		3		4		ns
<sup>t</sup> CKL	Pulse duration, CLK (system clock) low		3		4		ns
110	Access time, CLK ↑ to data out	Read latency = 2		12		15	ns
tAC	(see Note 4)	Read latency = 3		8		10	ns
<sup>t</sup> LZ	Delay time, CLK to DQ in the low-impedance state (see Note s	5)	0		0		ns
**	Delay time, CLK to DQ in the high-impedance state	Read latency = 2		7		9	
tHZ	(see Note 6)	Read latency = 3		7		9	ns
tDS	Setup time, data input		2		3		ns
tAS	Setup time, address		2		3		ns
tcs	Setup time, control input (CS, RAS, CAS, W, DQMx)		2		3		ns
tCES	Setup time, CKE (suspend entry/exit, power-down entry)		2		3		ns
tCESP	Setup time, CKE (power-down/self-refresh exit) (see Note 7)		8		10		ns
tон	Hold time, CLK ↑ to data out		3		3		ns
<sup>t</sup> DH	Hold time, data input		1		1		ns
tAH	Hold time, address		1		1		ns
<sup>t</sup> CH	Hold time, control input (CS, RAS, CAS, W, DQMx)		1		1		ns
<sup>t</sup> CEH	Hold time, CKE		1		1		ns
<sup>t</sup> RC	REFR command to ACTV, MRS, REFR, or SLFR command; ACTV, MRS, REFR, or SLFR command; Self-refresh exit to AC SLFR command		90		110		ns
tRAS	ACTV command to DEAC or DCAB command (see Note 9)	· · ·	60	120 000	70	120 000	ns
tRCD	ACTV command to READ or WRT command (see Note 9)		30		35		ns
tRP	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR con	nmand	30		40		ns

<sup>†</sup> See Figure 10 for load circuits.

<sup>‡</sup> All references are made to the rising transition of CLK, unless otherwise noted.

NOTES: 5. t<sub>AC</sub> is referenced from the rising transition of CLK that is previous to the data-out cycle. For example, the first data out t<sub>AC</sub> is referenced from the rising transition of CLK that is read latency – one cycle after the READ command. An access time is measured at output reference level 1.4 V.

6. tLZ is measured from the rising transition of CLK that is read latency - one cycle after the READ command.

7. tHZ (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.

8. See Figures 19 and 20.

 In case of WRITE with auto precharge (WRT\_P), the t<sub>RCD</sub> parameter must be relaxed to satisfy t<sub>RAS</sub> parameter. For example, - t<sub>RCD</sub> = 40 ns, for BL = 1 in order to satisfy t<sub>RAS</sub> = 60 ns in - 10 spec.



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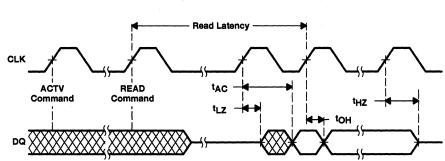
#### Table 9. Number of Cycles Required to Meet Minimum Specification for Key Timing Parameters<sup>†</sup>

			'664x	x4-10	'664x	x4-12	UNITS
	Operating frequency		100	66.6	83.3	55.5	MHz
<sup>t</sup> CK	Cycle time, CLK (system clock)		10	15	12	18	ns
	KEY PARAMETER			NUMBER OF CYCLES			QUIRED
	Read latency, minimum programmed value		3	2	3	2	cycles
tRCD	D ACTV command to READ or WRT command		3	2	3	2	cycles
<sup>t</sup> RAS	S ACTV command to DEAC or DCAB command		6	4	6	4	cycles
tRP	DEAC or DCAB command to ACTV, MRS, SLFR, or RI	EFR command	3	2	3	2	cycles
<sup>t</sup> RC	REFR command to ACTV, MRS, or REFR command; s or REFR command	self-refresh exit to ACTV, MRS, SLFR,	9	6	10	7	cycles
tRWL	Final data in to DEAC or DCAB command		2	1	2	1	cycles
tRRD	ACTV command for one bank to ACTV command for th	ne other bank	2	2	2	2	cycles
*****	Final data out of READ-P operation to ACTV, MRS,	Read latency = 2 ( $n_{EP} = -1$ )	-	2	_	2	cycles
tAPR	SLFR, or REFR command	Read latency = 3 ( $n_{EP} = -2$ )	2	1	2	1	cycles
<sup>t</sup> APW	Final data in of WRT-P operation to ACTV, MRS, SLFR	, or REFR command	4	3	5	3	cycles

 $^{\dagger}$  All references are made to the rising transition of CLK, unless otherwise noted.

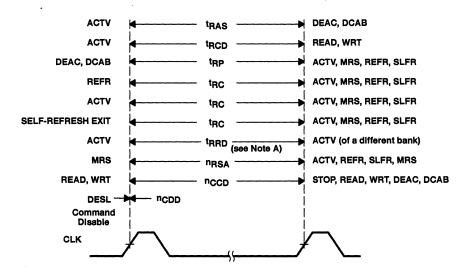


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### PARAMETER MEASUREMENT INFORMATION

Figure 12. Output Parameters



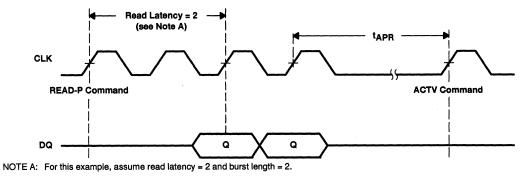
NOTE A: tRRD is specified for command execution in one bank to command execution in the other bank.

Figure 13. Command-to-Command Parameters

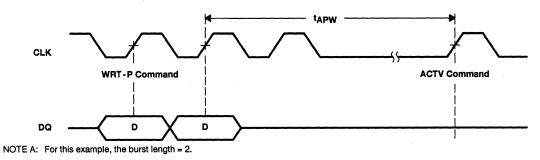


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### PARAMETER MEASUREMENT INFORMATION



#### Figure 16. Read-Automatic Deactivate (Autoprecharge)



#### Figure 17. Write-Automatic Deactivate (Autoprecharge)

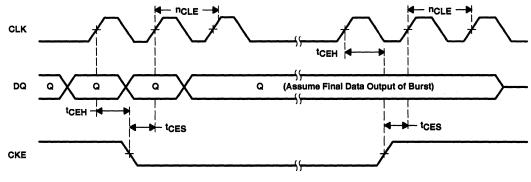
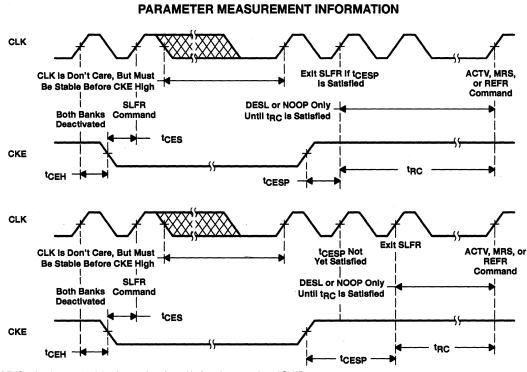


Figure 18. CLK-Suspend Operation (Assume BL = 4)



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NOTES: A. Assume both banks are deactivated before the execution of SLFR. B. Before/after self-refresh mode, 4K burst auto refresh cycles are recommended to ensure the SDRAM is fully refreshed.

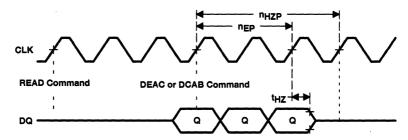
Figure 20. Self-Refresh Entry/Exit



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### PARAMETER MEASUREMENT INFORMATION



NOTE A: For this example, assume read latency = 3, and burst length = 4.



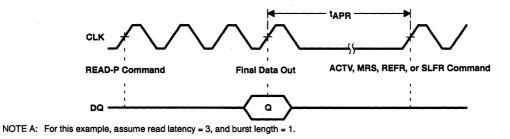
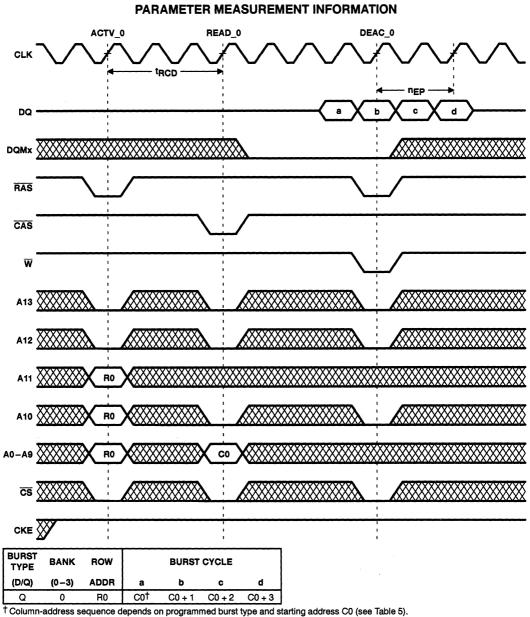


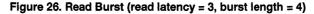
Figure 24. Read With Auto-Deactivate



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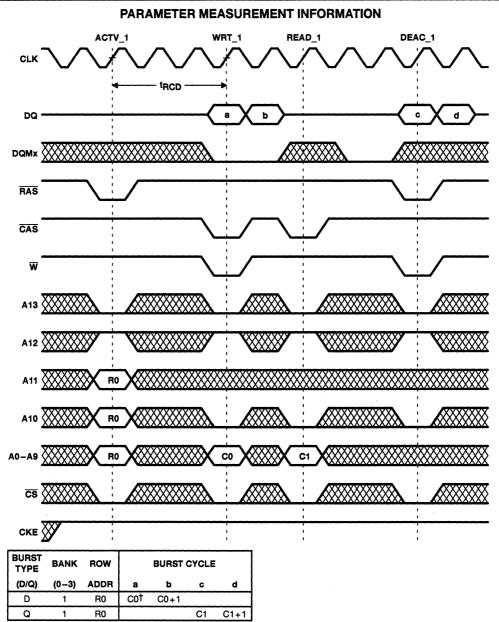
NOTE A: This example illustrates minimum t<sub>RCD</sub> and n<sub>EP</sub> for the '664xx4 at 100 MHz.





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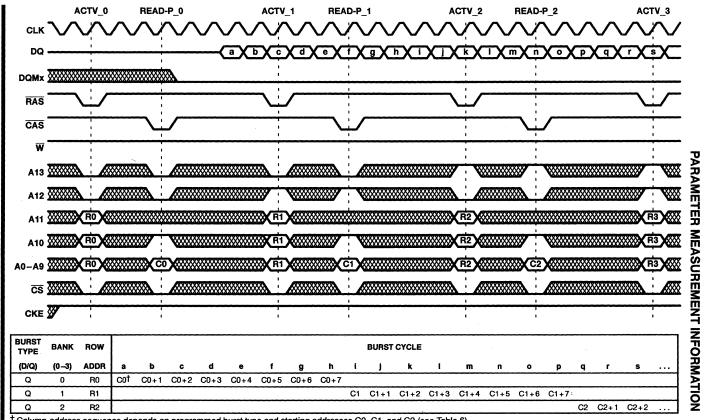


<sup>†</sup> Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 4). NOTE A: This example illustrates minimum t<sub>RCD</sub> for the '664xx4 at 100 MHz.

Figure 28. Write-Read Burst (read latency = 3, burst length = 2)



**PRODUCT PREVIEW** 



<sup>†</sup> Column-address sequence depends on programmed burst type and starting addresses C0, C1, and C2 (see Table 6). NOTE A: This example illustrates minimum t<sub>RCD</sub> for the '664xx4 at 100 MHz.

(a)

Figure 30. Four-Bank Row-Interleaving Read Bursts With Automatic Deactivate (read latency = 3, burst length = 8)

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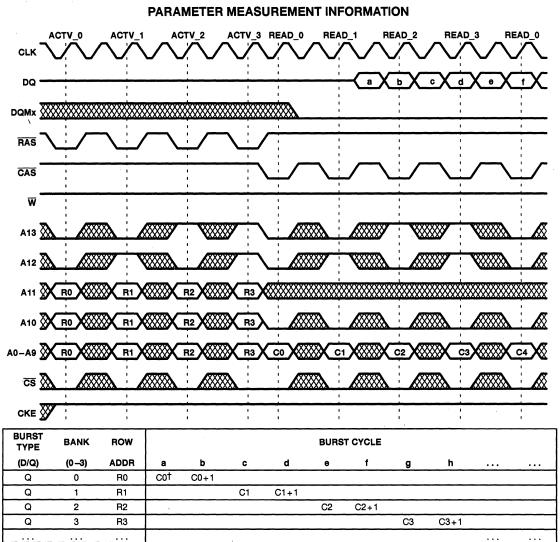
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<sup>†</sup> Column-address sequence depends on programmed burst type and starting addresses C0, C1, and C2 (see Table 4).

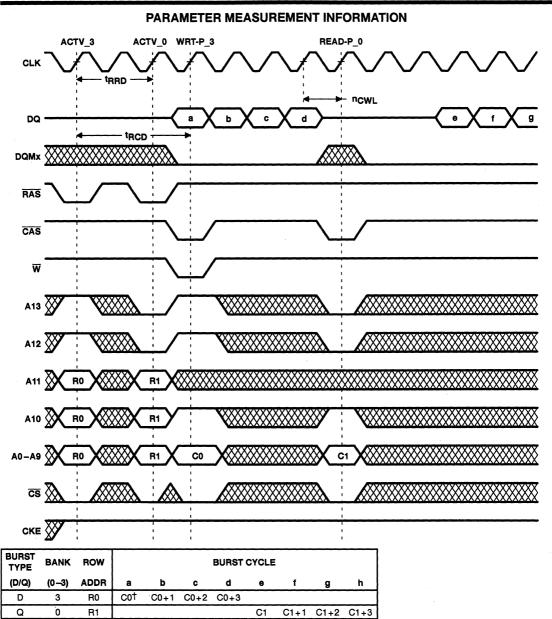
Figure 31. Four-Bank Column-Interleaving Read Bursts (read latency = 3, burst length = 2)



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<sup>†</sup> Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5). NOTE A: This example illustrates minimum  $n_{CWL}$  and  $t_{RRD}$  for the '664xx4 at 100 MHz.

Figure 33. Write-Burst Bank 3, Read-Burst Bank 0 With Automatic Deactivate (read latency = 3, burst length = 4)



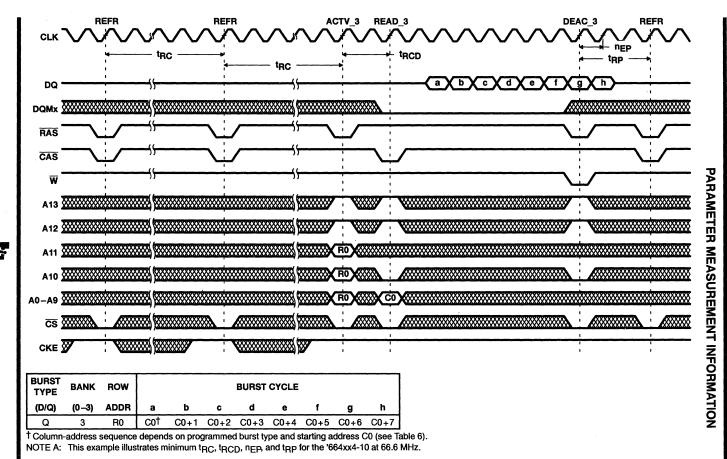


Figure 35. Refresh Cycles (Refreshes Followed by Read Burst, Followed by Refresh) (read latency = 2, burst length = 8)

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64M-BIT SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORIES

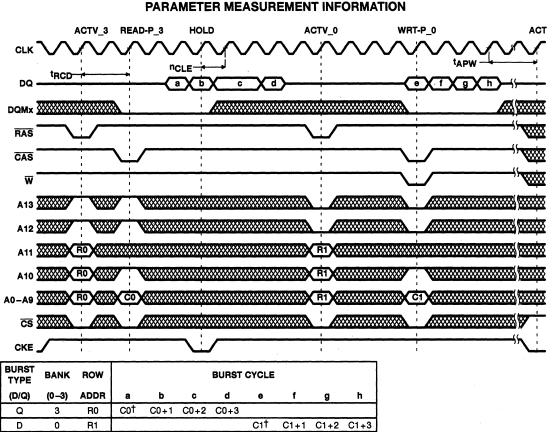
TMS664414, TMS664814,

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<sup>†</sup> Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5).

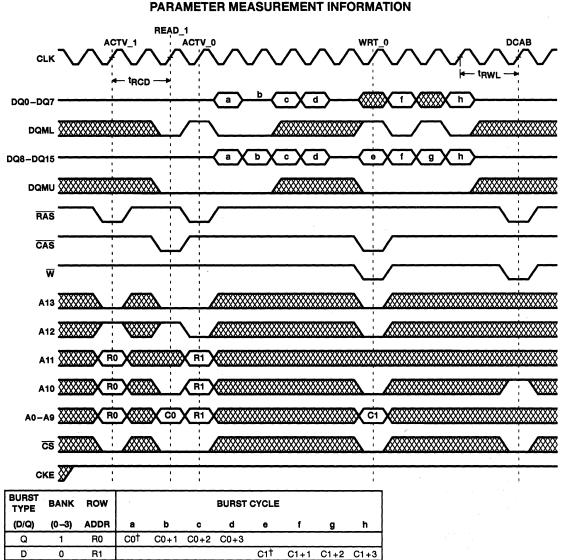
NOTES: A. This example illustrates minimum tRCD and tAPW for the '664xx4-10 at 66.6 MHz.

B. If entering the PDE command with violation of short t<sub>APW</sub>, the device still is entering the power-down mode and then both banks are deactivated (still in power-down mode).

Figure 37. Use of CKE for Clock Gating (Hold) and Standby Mode (Read-Burst Bank 3 With Hold, Write-Burst Bank 0, Standby Mode) (read latency = 2, burst length = 4)



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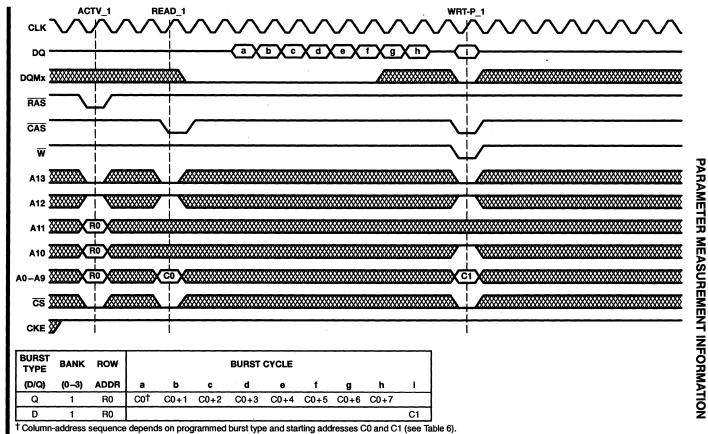


<sup>†</sup> Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5). NOTE A: This example illustrates minimum t<sub>BCD</sub> and a minimum t<sub>BWL</sub> write burst for the '664xx4-10 at 66.6 MHz.



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Figure 39. Use of DQM for Output and Data-In Cycle Masking (Read-Burst Bank 1, Write-Burst Bank 0, Deactivate All Banks) [Only Masked Out the Lower Bytes (Random Bits)] for x16 (read latency = 2, burst length = 4)



NOTE A: This example illustrates minimum t<sub>RCD</sub> for the '664xx4-10 at 100 MHz.

Figure 41. Read Burst — Single Write With Automatic Deactivate (read latency = 3, burst length = 8)

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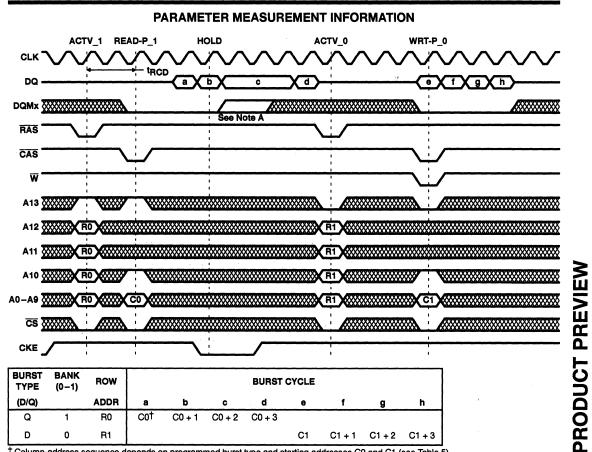
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<sup>†</sup> Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5).

NOTES: A. These rising clocks during output "c" with DQMx = Hi would not mask out the output "d" due to CKE insert low to suspend those rising clocks at cycle DQMx = Hi.

B. This example illustrates minimum tRCD for the '664xx4-10 at 66.6 MHz.

Figure 43. Use of CKE for Clock Gating (Hold/Suspend) and DQM = Hi Showed No Effect (read latency = 2, burst length = 4, two banks)

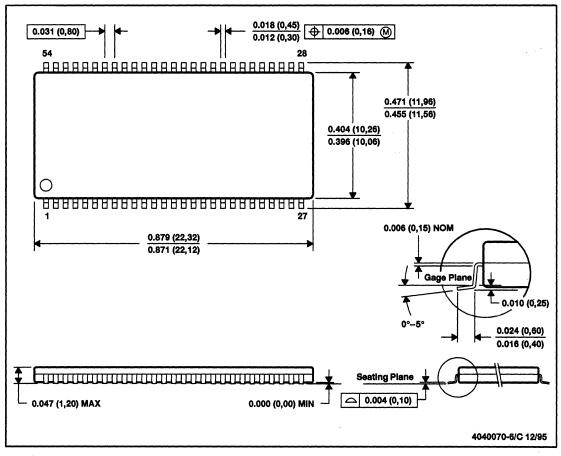


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#### DGE (R-PDSO-G54)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion.



Address Buffers/Latches/Flip-Flops3Clock-Distribution Circuits4	Clock-Distribution Circuits	4
Address Buffers/Latches/Flip-Flops 3		
	Address Buffers/Latches/Flip-Flops	3

# *Timing Differences of 10-pF Versus 50-pF Loading*

SCEA004 November 1996



#### Introduction

This application report provides a data analysis of Texas Instruments (TI) 'ALVCH16244, which is an advanced low-voltage CMOS (ALVC) 16-bit unidirectional driver. The 'ALVCH16244, 'ALVCH16721, 'ALVCH162827, and 'ALVCH16835 are unidirectional drivers that are commonly used in personal computers and workstations for memory addressing in dual in-line memory modules (DIMMs). Typical DIMM applications, however, require loads of approximately 10 pF and a temperature range from 0°C to 70°C. Since the data sheet values for  $t_{pd}$ ,  $t_{en}$ , and  $t_{dis}$  are characterized under a 50-pF load and a temperature range of -40°C to 85°C, designers may find the difference in typical values to be beneficial. The purpose of this application report is to provide design engineers with the difference in typical values for  $t_{pd}$ ,  $t_{en}$ , and  $t_{dis}$  using a load of 10 pF, as opposed to 50 pF, and a temperature range of 0°C to 70°C, as opposed to -40°C to 85°C.

#### Laboratory Testing Technique

Due to its widespread use, the 'ALVCH16244 was selected as the device for actual laboratory data. The data measures propagation delay time, enable time, and disable time. The values presented are the averages of three different outputs. The data presented is indicative of the 'ALVCH16721, the 'ALVCH162827, and the 'ALVCH16835, since the size of their output transistors are the same as those on the 'ALVCH16244. All values provided are typical values. Unique testing specifications are shown in the top, left portion of each graph.

Figure 1 shows the difference in propagation delay time, enable time, and disable time for  $V_{CC} = 2.7$  V and temperature values of 0°C and 70°C. The impact of a 10-pF versus a 50-pF loading results in decreases of approximately 20% in propagation delay time, approximately 25% in enable time, and approximately 10% in disable time.

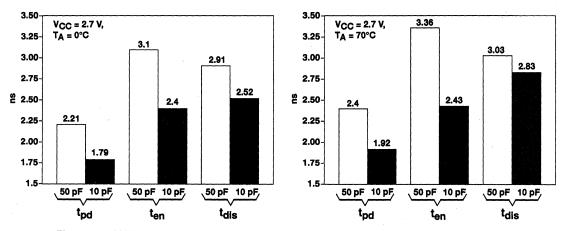
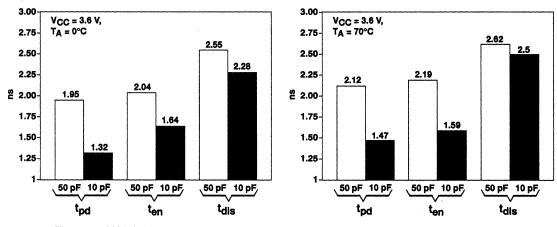


Figure 1. 'ALVCH16244 10-pF Versus 50-pF Switching-Time Differences for  $V_{CC} = 2.7 V$ 

Figure 2 shows the difference in propagation delay time, enable time, and disable time for  $V_{CC} = 3$  V and temperature values of 0°C and 70°C. The impact of a 10-pF versus a 50-pF loading results in decreases of approximately 25% in propagation delay time and enable time, and approximately 8% in disable time.





#### Conclusion

There is a noticeable difference in propagation delay time, enable time, and disable time when a 10-pF load versus a 50-pF load is used, and when an operating temperature range of 0°C to 70°C, as opposed to -40°C to 85°C, is used. The propagation delay time decreased an average of 26%, the enable time decreased an average of 24%, and the disable time decreased an average of 8%.

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Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a three-part type number as explained in the following example.

	EXAMPLE:	SN	74ALVCH16721 DGG	R
Prefix	·			/
MUST CONTAIN TWO TO FOUR LETTERS				
SN = Standard prefix SNJ = MIL-STD-883 processed and screened per JEDEC Standard 101		/		
Unique Circuit Description		_		
MUST CONTAIN SIX TO TWELVE CHARACTERS				
Examples: 74ALVCH16244 74SSTL16837 CDC587		/		
Package	/	/		
MUST CONTAIN ONE TO THREE LETTERS		/	/	
DBB, DGV=plastic thin very small-outlineDGE, DGG, PW=plastic thin shrink small-outlineDL=plastic shrink small-outline pastic shrink small-outline pastic thin quad flat packagePAH=plastic thin quad flat package	e package (TSSOP ckage (SSOP)	x/		
Tape and Reel Packaging	/			
Valid for surface-mount packages only. All orders for	or tape and reel mus	st be fo	r whole reels.	

#### MUST CONTAIN ONE OR TWO LETTERS

- LE = Left embossed tape and reel (required for PW package)
- R = Standard tape and reel (required for DBB, DGG, DGV; optional for DGE and DL packages)

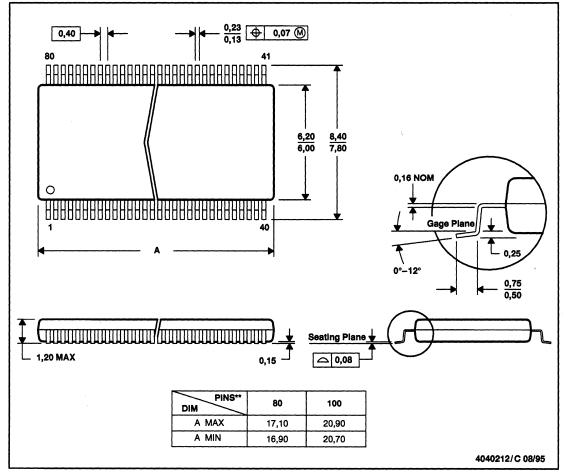


## **MECHANICAL DATA**

## DBB (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE PACKAGE

**80 PIN SHOWN** 



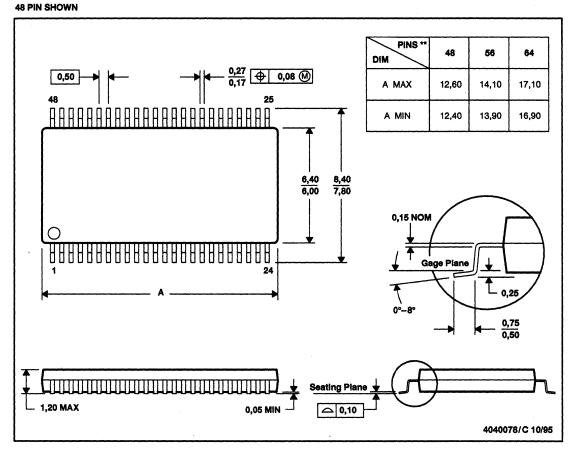
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.



PLASTIC SMALL-OUTLINE PACKAGE

DGG (R-PDSO-G\*\*)



NOTES: A. All linear dimensions are in millimeters.

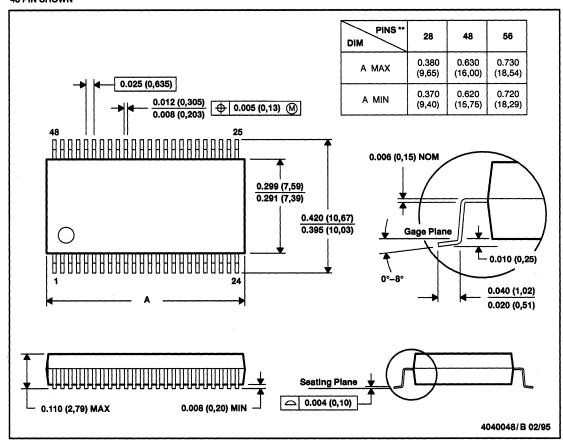
B. This drawing is subject to change without notice.

C. Falls within JEDEC MO-153



PLASTIC SMALL-OUTLINE PACKAGE

DL (R-PDSO-G\*\*) 48 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

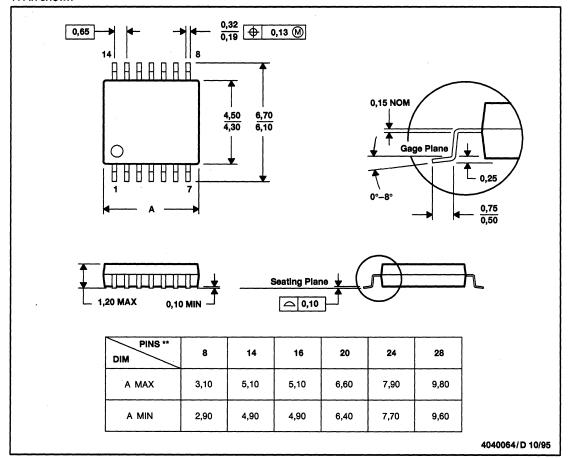
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).



#### PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN

PW (R-PDSO-G\*\*)



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153



