TEXAS INSTRUMENTS

MOS Memory

Commercial and Military Specifications

Data Book

MOS Memory
Commercial and Military Specifications
Data Book

1995

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MOS Memory Data Book

Commercial and Military Specifications

Printed on Recycled Paper

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INTRODUCTION

The 1995 *MOS Memory Data Book* from Texas Instruments includes complete detailed specifications on the expanding MOS Memory product line including Dynamic Random Access Memories (DRAMs), Single-In-Line Memory Modules (SIMMs), Erasable Programmable Read-Only Memories (EPROMs), One-Time Programmable Read-Only Memories (OTP PROMs), Electrically Erasable Programmable Read-Only Memories (Flash Memories), and Video RAMs (VRAMs). Also included are military specifications for DRAMs, EPROMs, and VRAMs.

The data book is divided into 12 chapters. Below you will find a brief description of each chapter.

Chapter 1. General Information — Includes an alphanumeric index for quickly finding device numbers and a part number guide with ordering information.

Chapter 2. Selection Guide — An easy-to-use reference guide that includes specific device information. Page numbers are also shown for easy access to the detailed specifications.

Chapter 3. Glossary/Timing Conventions/Data Sheet Structure — Defines terms and standards used throughout the data book.

Chapter 4–8. Product specifications for more than 100 devices can be found in these sections.

Chapter 9. Mechanical Data — Detailed package drawings and specifications are shown in this section.

Chapter 10. Logic Symbols — Includes an explanation and examples of the IEEE standard.

Chapter 11. Quality and Reliability — Details selected processes and the philosophies of Texas Instruments that are used to ensure high quality standards.

Chapter 12. Electrostatic Discharge Guidelines — Because all MOS Memory devices are ESD-sensitive, handling guidelines are included.

For ordering information or further assistance, please contact your nearest Texas Instruments Sales Office or Distributor as listed in the back of this book.

PRODUCT STAGE STATEMENTS

Product stage statements are used on Texas Instruments data sheets to indicate the development stage(s) of the product(s) specified in the data sheets.

If all products specified in a data sheet are at the same development stage, the appropriate statement from the following list is placed in the lower left corner of the first page of the data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

If not all products specified in a data sheet are at the PRODUCTION DATA stage, then the first statement below is placed in the lower left corner of the first page of the data sheet. Subsequent pages of the data sheet containing PRODUCT PREVIEW information or ADVANCE INFORMATION are then marked in the lower left-hand corner with the appropriate statement given below:

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

Contents

CHAPTER 6. SINGLE-IN-LINE MEMORY MODULES (SIMMS)

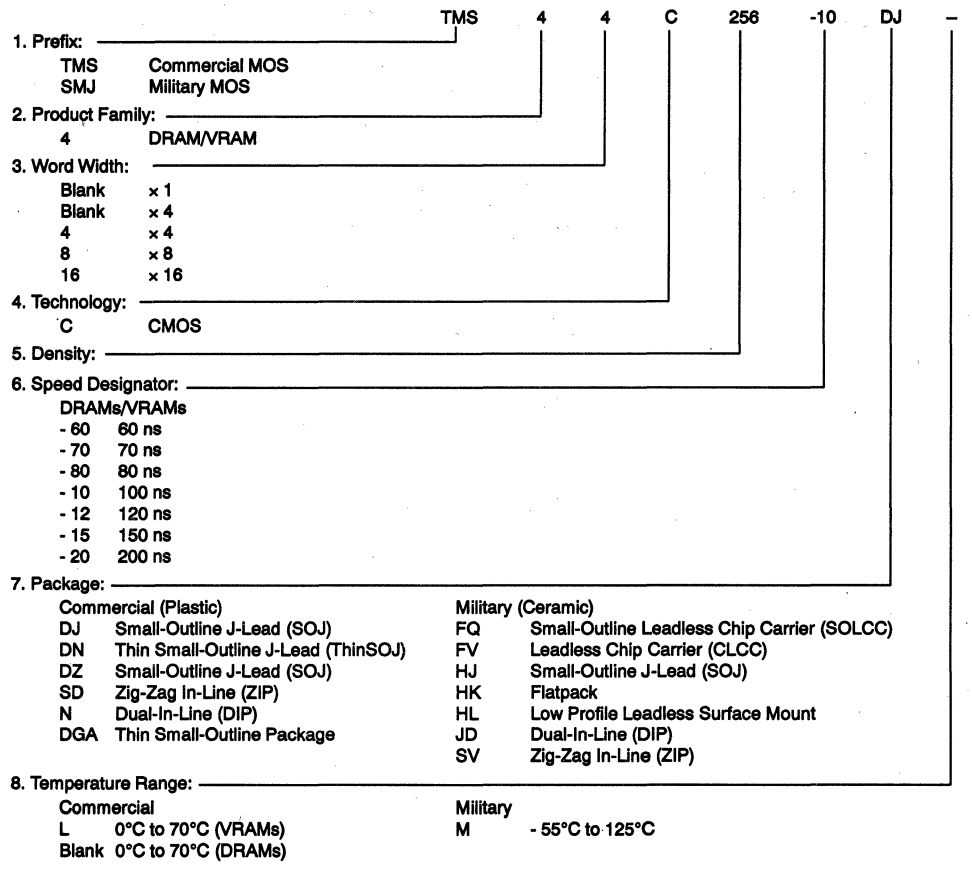
CHAPTER 7. FLASH MEMORY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EPROM) ONE-TIME PROGRAMMABLE MEMORY (OTP)

CHAPTER 8. MILITARY PRODUCTS

Alphanumeric Index

DRAM/VRAM/FMEM Ordering Information

Orders for DRAMs and VRAMs described in this book should include an eight-part number as explained in the following example:



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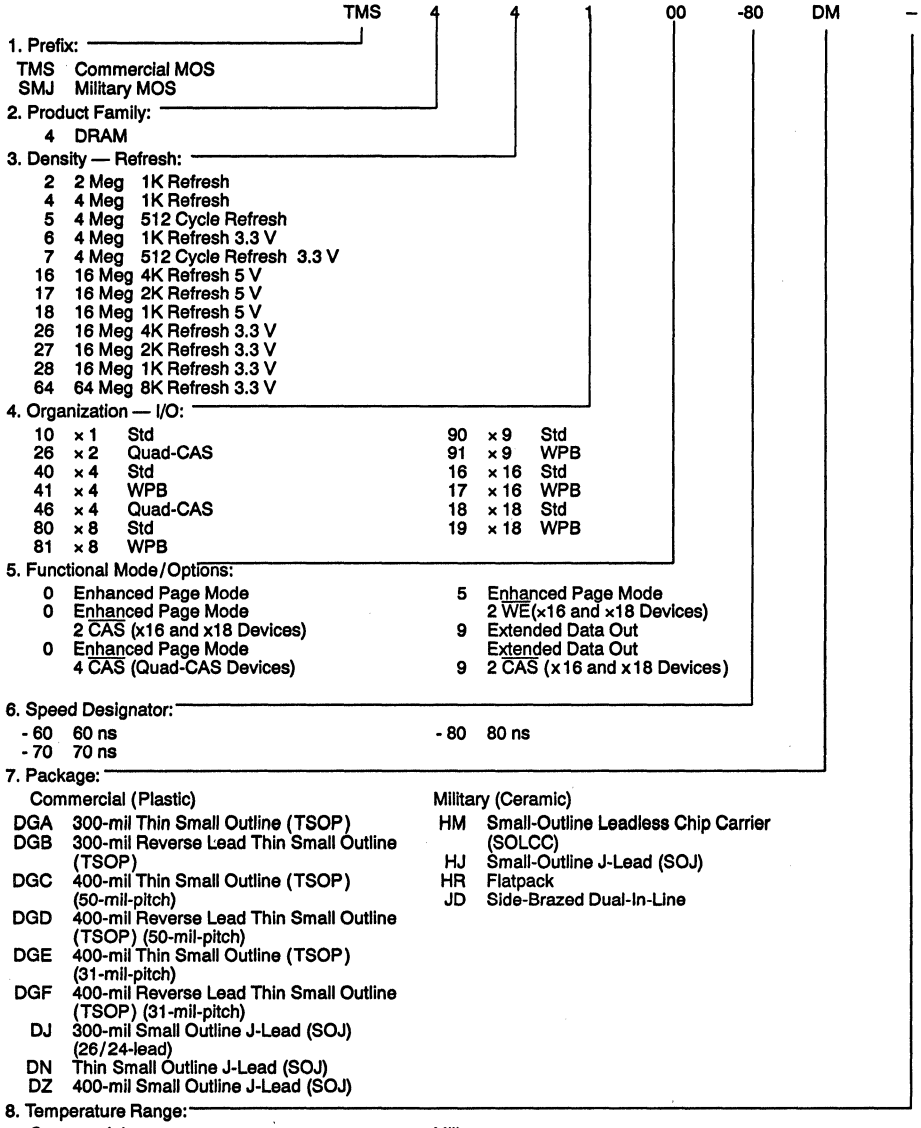
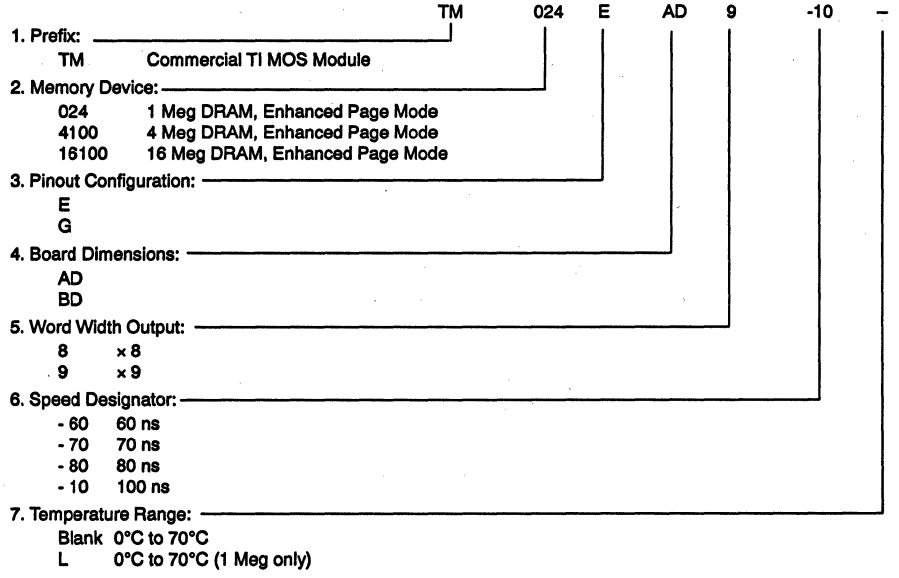
DRAM Ordering Information

Orders for the 4 Meg and 16 Meg and 64 Meg DRAMs described in this book should include an eight-part number as explained in the following example:



Standard DRAM Module Ordering Information

Orders for the standard DRAM Modules described in this book should include a seven-part number as explained in the following example:



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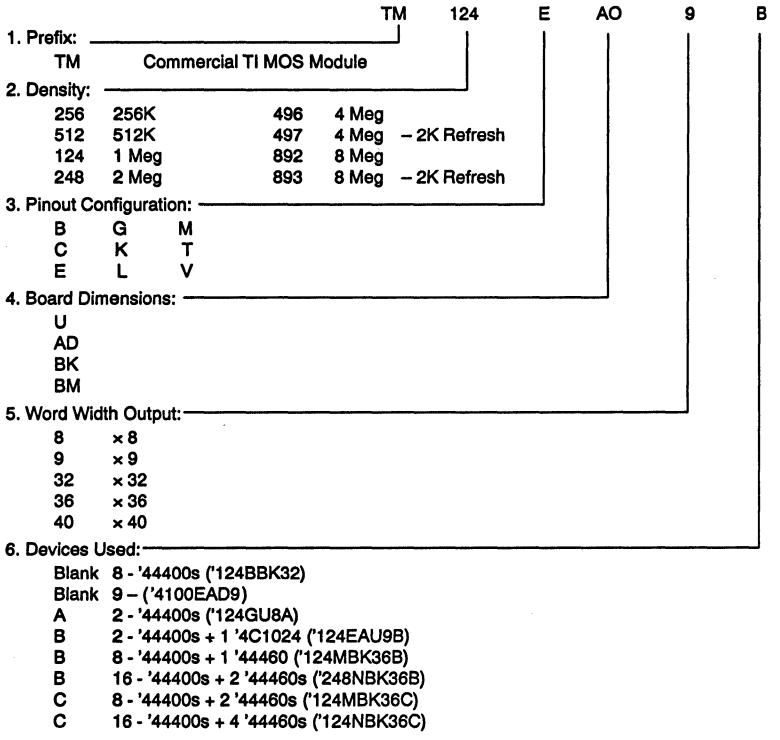
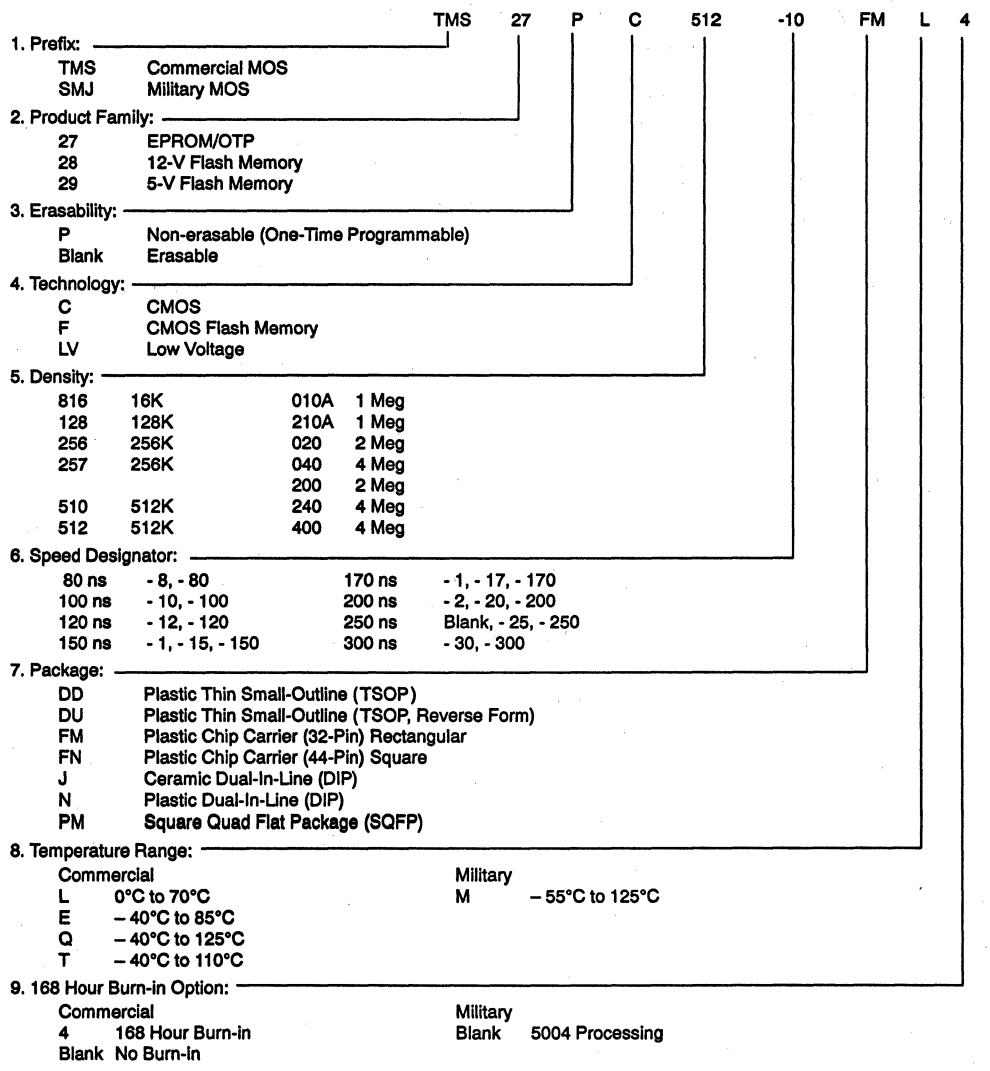
Differentiated DRAM Module Ordering Information

Orders for the mixed DRAM Modules described in this book should include an eight-part number as explained in the following example:



EPROM, FLASH, OTP Ordering Information

Orders for EPROMs, OTPs, and Flash Memories described in this book should include a nine-part number as explained in the following example:



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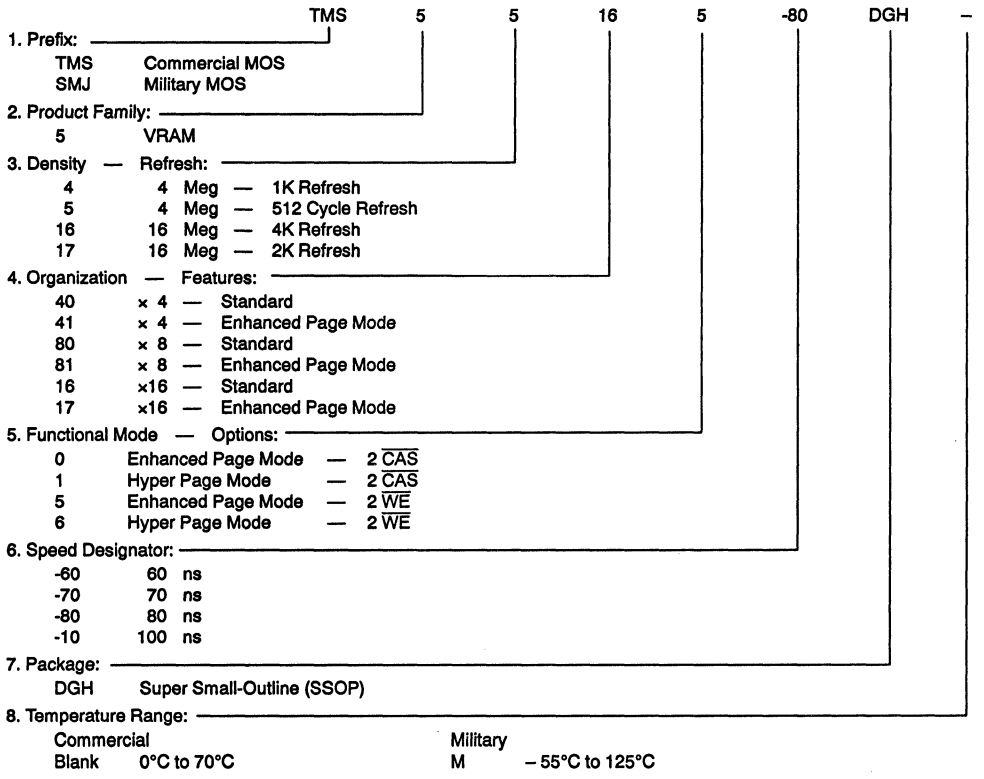
VRAM Ordering Information

Orders for 4 Meg VRAMs described in this book should include an eight-part number as explained in the following example:



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DRAM

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STAND-BY (mW)				
1024K	1024K × 1	SMJ4C1024-80 SMJ4C1024-100 SMJ4C1024-120 SMJ4C1024-150	80 100 120 150	5 ± 10%		22	18, 20, 20/26	HJ, FQ, HL,JD, HK, SV	Military	8-25
	256K × 4	SMJ44C256-80 SMJ44C256-100 SMJ44C256-120 SMJ4C1024-150	80 100 120 150	5 ± 10%			20/26	HJ, FQ, HL,JD, HK, SV	Military	8-5
4096K	1024K × 4	TMS44460-60‡ TMS44460-70‡ TMS44460-80‡	60 70 80	5 ± 10%	578 495 440	11	24/26	DJ, DGA	CMOS Enhanced Page Mode Quad CAS	4-5
		TMS44460P-60‡ TMS44460P-70‡ TMS44460P-80‡	60 70 80	5 ± 10%	578 495 440	11	24/26	DJ, DGA	CMOS Enhanced Page Mode Quad CAS	4-5
		TMS46460-60‡ TMS46460-70‡ TMS46460-80‡	60 70 80	5 ± 10%	385 330 275	3.6	24/26	DJ, DGA	CMOS Enhanced Page Mode Low Voltage Quad CAS	4-5
		TMS46460P-60‡ TMS46460P-70‡ TMS46460P-80‡	60 70 80	5 ± 10%	385 330 275	3.6	24/26	DJ, DGA	CMOS Enhanced Page Mode Low Voltage Quad CAS	4-5
	4096K × 1	TMS44100-60‡ TMS44100-70‡ TMS44100-80‡	60 70 80	5 ± 10%	523 468 413	11	20/26	DGA DJ	CMOS Enhanced Page Mode	4-27
		TMS44100P-60‡ TMS44100P-70‡ TMS44100P-80‡	60 70 80	5 ± 10%	523 468 413	11	20/26	DGA, DJ	CMOS Enhanced Page Mode Low Power	4-27
		SMJ44100-80 SMJ44100-10 SMJ44100-12	80 100 120	5 ± 10%	468 440 385	22	18, 20, 28	HR, JD, JDB,HL	Military CMOS Enhanced Page Mode	8-45
16384K	1024 × 16	SMJ416160‡ SMJ418160‡	60 70 80	5 ± 10%	495 440 385	11	50	HKD	Military CMOS Enhanced Page Mode	8-123

† DGA Plastic Thin Small-Outline-Package (TSOP)
DJ Plastic Small-Outline J-Lead (SOJ)
FQ Leadless Ceramic Chip Carrier (Military) (CDCC)
HJ Ceramic Small-Outline J-Lead (Military) (SOJ)
HK Flatpack (Military)
HKD Flatpack (Military)
HL Small-Outline Leadless Ceramic Chip Carrier (Military) (SOLCC)
HR Flatpack (Military)
JD 400-Mil Ceramic Sidebrazed Dual In-Line Package (Military) (DIP)
JDB 300-mil Ceramic Side-Brazed Dual In-Line Package (Military) (DIP)
SV Ceramic Zig-Zag Package (ZIP) (Military)

‡ Advance Information for product under development by TI

DRAM (Continued)

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
4096K	4096K × 1	TMS46100-70‡ TMS46100-80‡ TMS46100-10‡	70 80 100	3.3 ± 10%	216 180 144	3.6	20/26	DGA, DJ	CMOS Enhanced Page Mode Low Voltage	4-27
		TMS46100P-70‡ TMS46100P-80‡ TMS46100P-10‡	70 80 100	3.3 ± 10%	216 180 144	3.6	20/26	DGA, DJ	CMOS Enhanced Page Mode Low Voltage Extended Refresh	4-27
	1024K × 4	TMS44400-60‡ TMS44400-70‡ TMS44400-80‡	60 70 80	5 ± 10%	550 495 440	11	20/26	DJ, DGA	CMOS Enhanced Page Mode	4-51
		TMS44400P-60‡ TMS44400P-70‡ TMS44400P-80‡	60 70 80	5 ± 10%	550 495 440	11	20/26	DJ, DGA	CMOS Enhanced Page Mode Low Power	4-51
		SMJ44400-80 SMJ44400-10 SMJ44400-12	80 100 120	5 ± 10%	468 440 358	22	20	HR, JDB, HL, SV	Military CMOS Enhanced Page Mode	8-65
		TMS46400-70‡ TMS46400-80‡ TMS46400-10‡	70 80 100	3.3 ± 10%	252 216 180	7.2	20/26	DGA, DJ	CMOS Enhanced Page Mode Low Voltage	4-51
		TMS46400P-70‡ TMS46400P-80‡ TMS46400P-10‡	70 80 100	3.3 ± 10%	252 216 180	7.2	20/26	DGA, DJ	CMOS Enhanced Page Mode Low Voltage Extended Refresh	4-51
	256K × 16	TMS44165-70 TMS44165-80 TMS44165-10	70 80 100	5 ± 10%	660 578 523	11	40, 40/44	DGE, DZ	CMOS Enhanced Page Mode	4-73
		TMS44165P-70 TMS44165P-80 TMS44165P-10	70 80 100	5 ± 10%	660 578 523	11	40, 40/44	DGE, DZ	CMOS Enhanced Page Mode Low Power	4-73
		TMS45160-70 TMS45160-80 TMS45160-10	70 80 100	5 ± 10%	880 770 660	11	40, 40/44	DGE, DZ	CMOS Enhanced Page Mode	4-93
		TMS45160P-70 TMS45160P-80 TMS45160P-10	70 80 100	5 ± 10%	880 770 660	11	40, 40/44	DGE, DZ	CMOS Enhanced Page Mode Low Power	4-93

† DGA Plastic Thin Small-Outline-Package (TSOP)
DGE Plastic Surface Mount Thin Small-Outline Package (TSOP)
DJ Plastic Small-Outline J-Lead (SOJ)
DZ Plastic Small-Outline J-Lead (SOJ)
HL Small-Outline Leadless Ceramic Chip Carrier (Military) (SOLCC)
HR Flatpack (Military)
JDB 300-mil Ceramic Side-Brazed Dual In-Line Package (Military) (DIP)
SV Ceramic Zig-Zag Package (ZIP) (Military)
‡ Advance Information for product under development by TI

DRAM (Continued)

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
4096K	256K × 16	TMS45165-70‡ TMS45165-80‡ TMS45165-10‡	70 80 100	5 ± 10%	880 770 660	11	40, 40/44	DGE, DZ	CMOS Enhanced Page Mode	4-115
		TMS45165P-70‡ TMS45165P-80‡ TMS45165P-10‡	70 80 100	5 ± 10%	880 770 660	11	40, 40/44	DGE, DZ	CMOS Enhanced Page Mode Low Power	4-115
16 384K	16 384K × 1	SMJ416100-70 SMJ416100-80	70 80	5 ± 10%	440 385	11	24/28	FNC, HKB	Military Enhanced Page Mode	8-85
	4096K × 4	TMS416400-60 TMS416400-70 TMS416400-80	60 70 80	5 ± 10%	440 385 330	11	24/26	DGA, DJ	CMOS Enhanced Page Mode	4-135
		TMS416400P-60 TMS416400P-70 TMS416400P-80	60 70 80	5 ± 10%	440 385 330	11	24/26	DGA, DJ	CMOS Enhanced Page Mode	4-135
		SMJ416400-60 SMJ416400-70 SMJ416400-80 SMJ416400-10	60 70 80 100	5 ± 10%	495 440 385 330	11	24/28	FNC, HKB, SV	Military Enhanced Page Mode	8-105
		TMS417400-60 TMS417400-70 TMS417400-80	60 70 80	5 ± 10%	605 550 495	11	24/26	DGA, DJ	CMOS Enhanced Page Mode	4-135
		TMS417400P-60 TMS417400P-70 TMS417400P-80	60 70 80	5 ± 10%	605 550 495	11	24/26	DGA, DJ	CMOS Enhanced Page Mode	4-135
		TMS426400-60§ TMS426400-70§ TMS426400-80§	60 70 80	3.3 ± 10%	252 216 180	3.6	24/26	DGA, DJ	CMOS Enhanced Page Mode Low Voltage	4-135
		TMS426400P-60§ TMS426400P-70§ TMS426400P-80§	60 70 80	3.3 ± 10%	252 216 180	3.6	24/26	DGA, DJ	CMOS Enhanced Page Mode Low Voltage Low Power	4-135

† DGA Plastic Thin Small-Outline-Package (TSOP)
DGE Plastic Surface Mount Thin Small-Outline Package (TSOP)
DJ Plastic Small-Outline J-Lead (SOJ)
DZ Plastic Small-Outline J-Lead (SOJ)
FNC Small-Outline Leadless Chip Carrier (Military) (SOLCC)
HKB Flatpack (Military)
SV Ceramic Zig-Zag Package (ZIP) (Military)

‡ Advance Information for product under development by TI

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DRAM (Continued)

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
16 384K	4096K × 4	TMS427400-60‡ TMS427400-70‡ TMS427400-80‡	60 70 80	3.3 ± 10%	360 324 288	3.6	24/26	DGA, DJ	CMOS Enhanced Page Mode Low Voltage	4-135
		TMS427400P-60‡ TMS427400P-70‡ TMS427400P-80‡	60 70 80	3.3 ± 10%	360 324 288	3.6	24/26	DGA, DJ	CMOS Enhanced Page Mode Low Voltage Low Power	4-135
	1024K × 16	TMS416160-60‡ TMS416160-70‡ TMS416160-80‡	60 70 80	5 ± 10%	495 440 385	11	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode	4-163
		TMS416160P-60‡ TMS416160P-70‡ TMS416160P-80‡	60 70 80	5 ± 10%	495 440 385	11	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode Low Power	4-163
		TMS418160-60‡ TMS418160-70‡ TMS418160-80‡	60 70 80	5 ± 10%	1045 990 935	11	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode	4-163
		TMS418160P-60‡ TMS418160P-70‡ TMS418160P-80‡	60 70 80	5 ± 10%	1045 990 935	11	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode Low Power	4-163
		TMS426160-60‡ TMS426160-70‡ TMS426160-80‡	60 70 80	3.3 ± 10%	324 288 252	3.6	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode Low Voltage	4-163
		TMS426160P-60‡ TMS426160P-70‡ TMS426160P-80‡	60 70 80	3.3 ± 10%	324 288 252	3.6	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode Low Voltage Low Power	4-163
		TMS428160-60‡ TMS428160-70‡ TMS428160-80‡	60 70 80	3.3 ± 10%	684 648 612	3.6	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode Low Voltage	4-163
		TMS428160P-60‡ TMS428160P-70‡ TMS428160P-80‡	60 70 80	3.3 ± 10%	684 648 612	3.6	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode Low Voltage Low Power	4-163

† DGA Plastic Thin Small-Outline-Package (TSOP)
DGE Plastic Surface Mount Thin Small-Outline Package (TSOP)
DJ Plastic Small-Outline J-Lead (SOJ)
DZ Plastic Small-Outline J-Lead (SOJ)

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DRAM (Continued)

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
16 384K	1024K × 16	TMS416169-60‡ TMS416169-70‡ TMS416169-80‡	60 70 80	5 ± 10%	495 440 385	11	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode	4-191
		TMS416169P-60‡ TMS416169P-70‡ TMS416169P-80‡	60 70 80	5 ± 10%	495 440 385	11	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode Low Power	4-191
		TMS418169-60‡ TMS418169-70‡ TMS418169-80‡	60 70 80	5 ± 10%	1045 990 935	11	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode	4-191
		TMS418169P-60‡ TMS418169P-70‡ TMS418169P-80‡	60 70 80	5 ± 10%	1045 990 935	11	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode Low Power	4-191
		TMS426169-60‡ TMS426169-70‡ TMS426169-80‡	60 70 80	3.3 ± 10%	324 288 252	3.6	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode Low Voltage	4-191
		TMS426169P-60‡ TMS426169P-70‡ TMS426169P-80‡	60 70 80	3.3 ± 10%	324 288 252	3.6	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode Low Voltage Low Power	4-191
		TMS428169-60‡ TMS428169-70‡ TMS428169-80‡	60 70 80	3.3 ± 10%	684 648 612	3.6	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode Low Voltage	4-191
		TMS428169P-60‡ TMS428169P-70‡ TMS428169P-80‡	60 70 80	3.3 ± 10%	684 648 612	3.6	42, 44/50	DGE, DZ	CMOS Enhanced Page Mode Low Voltage Low Power	4-191
65 536K	8192K × 8	TMS464800-50‡ TMS464800-60‡ TMS464800-70‡ TMS464800-80‡	50 60 70 80	3.3 ± 10%	504 432 396 360	7.2	32	DZ, DGC	CMOS Enhanced Page Mode Low Voltage	4-187
		TMS464800P-50‡ TMS464800P-60‡ TMS464800P-70‡ TMS464800P-80‡	50 60 70 80	3.3 ± 10%	504 432 396 360	7.2	32	DGC, DZ	CMOS Enhanced Page Mode Low Voltage Low Power	4-187

† DGC Plastic Thin Small-Outline Package (TSOP) 400-mil (50-mil pitch)
DGE Plastic Surface Mount Thin Small-Outline Package (TSOP)
DZ Plastic Small-Outline J-Lead (SOJ)

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DRAM (Continued)

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	ACTIVE (mW)	STANDBY (mW)	PINS	PACKAGE†	NOTES	PAGE
65536K	4096K × 16	TMS464160-50‡	50	3.3 ± 10%	504	7.2	50, TBD	DGE, DZ	CMOS Enhanced Page Mode Low Voltage	4-187
		TMS464160-60‡	60		432					
		TMS464160-70‡	70		396					
		TMS464160-80‡	80		360					
		TMS464160P-50‡	50	3.3 ± 10%	504	7.2	50, TBD	DGE, DZ	CMOS Enhanced Page Mode Low Voltage Low Power	4-187
		TMS464160P-60‡	60		432					
		TMS464160P-70‡	70		396					
		TMS464160P-80‡	80		360					
	16384K × 4	TMS464400-50‡	50	3.3 ± 10%	504	7.2	32	DGC, DZ	CMOS Enhanced Page Mode Low Voltage	4-187
		TMS464400-60‡	60		432					
		TMS464400-70‡	70		396					
		TMS464400-80‡	80		360					
		TMS464400P-50‡	50	3.3 ± 10%	504	7.2	32	DGC, DZ	CMOS Enhanced Page Mode Low Voltage Low Power	4-187
		TMS464400P-60‡	60		432					
		TMS464400P-70‡	70		396					
		TMS464400P-80‡	80		360					

† DGC Plastic Thin Small-Outline Package (TSOP) 400-mil (50-mil pitch)
DGE Plastic Surface Mount Thin Small-Outline Package (TSOP)
DZ Plastic Small-Outline J-Lead (SOJ)

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SDRAMs

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
16M	4M × 4	TMS626402-10	9	3.3 ± 10%	612	3.6	44	DGE		5-3
		TMS626402-12	10		504					
		TMS626402-15	12		468					
	2M × 8	TMS626802-10	9	3.3 ± 10%	612	3.6	44	DGE		5-41
		TMS626802-12	10		504					
		TMS626802-15	12		468					

† DGE Plastic Surface Mount Thin Small-Outline Package (TSOP)

Video RAMs

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
1024K	256K × 4	SMJ44C251B-10 SMJ44C251B-12	100 120	5 ± 10%	550 495	83	28	HJ, HM, JD, SV	Military CMOS Multiport Video RAM	8-145
4096K	256K × 16	SMJ55161-70 SMJ55161-80	70 80	5 ± 10%	1050 975	825 800	64, 68	GB, HKC	Military CMOS Multiport Video RAM	8-197
		SMJ55166-70 SMJ55166-80	70 80	5 ± 10%	1050 975	825 800	64, 68	GB, HKC	Military CMOS Multiport Video RAM	8-259
		TMS55160-60 TMS55160-70 TMS55160-80	60 70 80	5 ± 10%	908 880	28	64	DGH	CMOS Multiport Video RAM	5-79
		TMS55161-60 TMS55161-70 TMS55161-80	60 70 80	5 ± 10%	908 880	28	64	DGH	CMOS Multiport Video RAM	5-191
		TMS55165-60 TMS55165-70 TMS55165-80	60 70 80	5 ± 10%	908 880	28	64	DGH	CMOS Multiport Video RAM	5-135
		TMS55166-60 TMS55166-70 TMS55166-80	60 70 80	5 ± 10%	908 880	28	64	DGH	CMOS Multiport Video RAM	5-251

† DGH Plastic Super Small-Outline Package (SSOP)
GB Ceramic Pin Grid Array
HJ Ceramic Small-Outline J-Lead (Military) (SOJ)
HKC 0.5 mm Pitch Ceramic Flatpack (Non-conductive tie bar) (Military)
HM Small-Outline Leadless Ceramic Chip Carrier (Military) (SOLCC)
JD Ceramic Sidebrazed Dual In-Line Package (Military) (DIP)
SV Ceramic Zig-Zag Package (ZIP) (Military)

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DRAM Module

DENSITY	ORGANIZATION (WORDS x BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	DIMENSION LENGHT x HEIGHT INCHES (MILLIMETERS)	PINS	PACKAGE	PAGE
4 MByte	4M x 8	TM4100GAD8-60 TM4100GAD8-70 TM4100GAD8-80	60 70 80	5 ± 10%	3.5" x 0.8" (88,90 x 20,32)	30	Single-Sided Socketable Solder-Tabbed	6-3
		TM497GU8-60 TM497GU8-70 TM497GU8-80	60 70 80	5 ± 10%	3.5" x 0.65" (88,90 x 16,65)	30	Single-Sided Socketable Solder-Tabbed	6-9
	4M x 9	TM4100EAD9-60 TM4100EAD9-70 TM4100EAD9-80	60 70 80	5 ± 10%	3.5" x 0.8" (88,90 x 20,32)	30	Single-Sided Socketable Solder-Tabbed	6-15
		TM497EU9-60 TM497EU9-70 TM497EU9-80	60 70 80	5 ± 10%	3.5" x 0.8" (88,90 x 20,32)	30	Single-Sided Socketable Solder-Tabbed	6-23
	1M x 32	TM124BBK32-60 TM124BBK32-70 TM124BBK32-80	60 70 80	5 ± 10%	3.5" x 0.65" (88,90 x 16,65)	72	Single-Sided, Socketable Gold-Tabbed	6-29
		TM124BBK32S-60 TM124BBK32S-70 TM124BBK32S-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Single-Sided Socketable Solder-Tabbed	6-29
		TM124BBK32F-60 TM124BBK32F-70 TM124BBK32F-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Single-Sided Socketable Gold-Tabbed	6-39
		TM124BBK32U-60 TM124BBK32U-70 TM124BBK32U-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Single-Sided Socketable Solder-Tabbed	6-39
	1M x 36	TM124MBK36B-60 TM124MBK36B-70 TM124MBK36B-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Single-Sided Socketable Gold-Tabbed	6-63
		TM124MBK36R-60 TM124MBK36R-70 TM124MBK36R-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Single-Sided Socketable Solder-Tabbed	6-63
		TM124MBK36C-60 TM124MBK36C-70 TM124MBK36C-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Single-Sided Socketable Gold-Tabbed	6-81
		TM124MBK36S-60 TM124MBK36S-70 TM124MBK36S-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Single-Sided Socketable Solder-Tabbed	6-81
		TM124MBK36F-60 TM124MBK36F-70 TM124MBK36F-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Single-Sided Socketable Gold-Tabbed	6-73
		TM124MBK36U-60 TM124MBK36U-70 TM124MBK36U-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Single-Sided Socketable Solder-Tabbed	6-73
		TM124MBK36G-60 TM124MBK36G-70 TM124MBK36G-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Single-Sided Socketable Gold-Tabbed	6-91
		TM124MBK36V-60 TM124MBK36V-70 TM124MBK36V-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Single-Sided Socketable Solder-Tabbed	6-91

DRAM Module (continued)

DENSITY	ORGANIZATION (WORDS x BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	DIMENSION LENGHT x HEIGHT INCHES (MILLIMETERS)	PINS	PACKAGE	PAGE
8 MByte	2M x 32	TM248CBK32-60 TM248CBK32-70 TM248CBK32-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Double-Sided Socketable Gold-Tabbed	6-29
		TM248CBK32S-60 TM248CBK32S-70 TM248CBK32S-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Double-Sided Socketable Solder-Tabbed	6-29
		TM248CBK32F-60 TM248CBK32F-70 TM248CBK32F-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Double-Sided Socketable Gold-Tabbed	6-39
		TM248CBK32U-60 TM248CBK32U-70 TM248CBK32U-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Double-Sided Socketable Solder-Tabbed	6-39
	2M x 36	TM248NBK36B-60 TM248NBK36B-70 TM248NBK36B-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Double-Sided Socketable Gold-Tabbed	6-63
		TM248NBK36R-60 TM248NBK36R-70 TM248NBK36R-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Double-Sided Socketable Solder-Tabbed	6-63
		TM248NBK36C-60 TM248NBK36C-70 TM248NBK36C-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Double-Sided Socketable Gold-Tabbed	6-81
		TM248NBK36S-60 TM248NBK36S-70 TM248NBK36S-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Double-Sided Socketable Solder-Tabbed	6-81
		TM248NBK36F-60 TM248NBK36F-70 TM248NBK36F-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Double-Sided Socketable Solder-Tabbed	6-73
		TM248NBK36U-60 TM248NBK36U-70 TM248NBK36U-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Double-Sided Socketable Solder-Tabbed	6-73
		TM248NBK36G-60 TM248NBK36G-70 TM248NBK36G-0	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Double-Sided Socketable Solder-Tabbed	6-91
		TM248NBK36V-60 TM248NBK36V-70 TM248NBK36V-80	60 70 80	5 ± 10%	4.25" x 1.00" (107,95 x 25,40)	72	Double-Sided Socketable Solder-Tabbed	6-91

DRAM Module (Concluded)

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	DIMENSION LENGHT × HEIGHT INCHES (MILLIMETERS)	PINS	PACKAGE	PAGE
16 MByte	4M × 32	TM497BBK32-60 TM497BBK32-70 TM497BBK32-80	60 70 80	5 ± 10%	4.25" × 1.00" (107,95 × 25,40)	72	Single-Sided Socketable Gold-Tabbed	6-47
		TM497BBK32S-60 TM497BBK32S-70 TM497BBK32S-80	60 70 80	5 ± 10%	4.25" × 1.00" (107,95 × 25,40)	72	Single-Sided Socketable Solder-Tabbed	6-47
	4M × 36	TM497MBK36A-60 TM497MBK36A-70 TM497MBK36A-80	60 70 80	5 ± 10%	4.25" × 1.00" (107,95 × 25,40)	72	Double-Sided Socketable Gold-Tabbed	6-99
		TM497MBK36Q-60 TM497MBK36Q-70 TM497MBK36Q-80	60 70 80	5 ± 10%	4.25" × 1.00" (107,95 × 25,40)	72	Double-Sided Socketable Solder-Tabbed	6-99
		TM497MBM36A-60 TM497MBM36A-70 TM497MBM36A-80	60 70 80	5 ± 10%	4.25" × 1.25" (107,95 × 31,75)	72	Single-Sided Socketable Gold-Tabbed	6-107
		TM497MBM36Q-60 TM497MBM36Q-70 TM497MBM36Q-80	60 70 80	5 ± 10%	4.25" × 1.25" (107,95 × 31,75)	72	Single-Sided Socketable Solder-Tabbed	6-107
	8M × 32	TM893CBK32-60 TM893CBK32-70 TM893CBK32-80	60 70 80	5 ± 10%	4.25" × 1.25" (107,95 × 31,75)	72	Double-Sided Socketable Gold-Tabbed	6-55
		TM893CBK32S-60 TM893CBK32S-70 TM893CBK32S-80	60 70 80	5 ± 10%	4.25" × 1.25" (107,95 × 31,75)	72	Double-Sided Socketable Solder-Tabbed	6-55
32 MByte	8M × 36	TM893NBM36A-60 TM893NBM36A-70 TM893NBM36A-80	60 70 80	5 ± 10%	4.25" × 1.25" (107,95 × 31,75)	72	Double-Sided Socketable Gold-Tabbed	6-107
		TM893NBM36Q-60 TM893NBM36Q-70 TM893NBM36Q-80	60 70 80	5 ± 10%	4.25" × 1.25" (107,95 × 31,75)	72	Double-Sided Socketable Solder-Tabbed	6-107

EPROM

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
	16K × 8	SMJ27C128-12 SMJ27C128-15 SMJ27C128-17 SMJ27C128-20 SMJ27C128-25	120 150 170 200 250	5 ± 10%	138	1.7	28	J	Military	8-319
256K	32K × 8	TMS27C256-10 TMS27C256-12 TMS27C256-15 TMS27C256-17 TMS27C256-20 TMS27C256-25	100 120 150 170 200 250	5 ± 10%	165	1.4	28	J	CMOS	7-143
512K	64K × 8	TMS27C510-12 TMS27C510-15 TMS27C510-17 TMS27C510-20 TMS27C510-25	120 150 170 200 250	5 ± 10%	165	1.4	32	J	CMOS	7-155
		TMS27C512-10 TMS27C512-12 TMS27C512-15 TMS27C512-20 TMS27C512-25	100 120 150 200 250	5 ± 10%	165	1.4	28	J	CMOS	7-167
1024K	128K × 8	TMS27C010A-10 TMS27C010A-12 TMS27C010A-15 TMS27C010A-20	100 120 150 200	5 ± 10%	165	0.55	32	J	CMOS	7-179
	64K × 16	TMS27C210A-10 TMS27C210A-12 TMS27C210A-15 TMS27C210A-20 TMS27C210A-25	100 120 150 200 250	5 ± 10%	165	0.55	40	J	CMOS	7-191
2048K	256K × 8	TMS27C020-12 TMS27C020-15 TMS27C020-20 TMS27C020-25	120 150 200 250	5 ± 10%	165	0.55	32	J	CMOS	7-201

† J Ceramic Dual In-Line Package (DIP)

Flash

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
512K	64K × 8	TMS28F512A-10 TMS28F512A-12 TMS28F512A-15 TMS28F512A-17	100 120 150 170	5 ± 10%	165	.55	32	FM, N, DD, DU	CMOS Flash Memory	7-3
1024K	128K × 8	TMS28F010B-90 TMS28F010B-10 TMS28F010B-12 TMS28F010B-15	100 120 150 170	5 ± 10%	165	.55	32	DD, DU, FM	CMOS Flash Memory	7-25
	64K × 16	TMS28F210-10 TMS28F210-12 TMS28F210-15 TMS28F210-17	100 120 150 170	5 ± 10%	275	.55	40, 44	FN, J	CMOS Flash Memory	7-47
2048K	256K × 8	TMS28F020-10 TMS28F020-12 TMS28F020-15 TMS28F020-17	100 120 150 170	5 ± 10%	275	.55	32	FM, DD	CMOS Flash Memory	7-67
	256K × 8 or 128K × 16	TMS28F200x-60‡ TMS28F200x-70‡ TMS28F200x-80‡ TMS28F200x-90‡	60 70 80 90	5 ± 5% 5 ± 10% 5 ± 10% 5 ± 10%	358	.55	44, 56	DBJ, DBR	CMOS Boot-Block Flash Memory	7-87
4096K	517K × 8 or 256K × 16	TMS28F400x-60‡ TMS28F400x-70‡ TMS28F400x-80‡ TMS28F400x-90‡	60 70 80 90	5 ± 5% 5 ± 10% 5 ± 10% 5 ± 10%	358	.55	44, 56	DBJ, DBR	CMOS-Boot-Block Flash Memory	7-115

† DBJ Plastic Small-Outline Package
DBR Plastic Small-Outline Package
DD Plastic Thin Small-Outline Package
DU Plastic Thin Small-Outline Reverse Form Package
FM Plastic Leaded Chip Carrier
FN Plastic Leaded Chip Carrier
J Ceramic Dual In-Line Package (DIP)
N Plastic Dual In-Line Package (DIP)

‡ Advance Information for product under development by TI

EPROM

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
4096K	512K × 8	TMS27C040-10 TMS27C040-12 TMS27C040-15	100 120 150	5 ± 10%	275	0.55	32	J	CMOS	7-211
		SMJ27C040-10 SMJ27C040-12 SMJ27C040-15	100 120 150	5 ± 10%	275	0.55	32	J	Military	8-331
	256K × 16	TMS27C240-10 TMS27C240-12 TMS27C240-15	100 120 150	5 ± 10%	275	0.55	40	J	CMOS	7-221

† J Ceramic Dual In-Line Package (DIP)

One-Time Programmable (OTP) PROM

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
256K	32K × 8	TMS27PC256-10 TMS27PC256-15 TMS27PC256-17 TMS27PC256-20 TMS27PC256-25	100 150 170 200 250	5 ± 10%	165	1.4	28, 32	FM, N	CMOS	7-143
512K	64K × 8	TMS27PC510-15 TMS27PC510-17 TMS27PC510-20 TMS27PC510-25	150 170 200 250	5 ± 10%	165	1.4	32	FM, N	CMOS	7-155
		TMS27PC512-10 TMS27PC512-12 TMS27PC512-15 TMS27PC512-20 TMS27PC512-25	100 120 150 200 250	5 ± 10%	165	1.4	28, 32	DD, DU, FM, N	CMOS	7-167
1024K	128K × 8	TMS27PC010A-12 TMS27PC010A-15 TMS27PC010A-20	120 150 200	5 ± 10%	165	0.55	32	DD, DU, FM, N	CMOS	7-179
	64K × 16	TMS27PC210A-12 TMS27PC210A-15 TMS27PC210A-20 TMS27PC210A-25	120 150 200 250	5 ± 10%	165	0.55	44	FN	CMOS	7-191
2048K	256K × 8	TMS27PC020-12 TMS27PC020-15 TMS27PC020-20 TMS27PC020-25	120 150 200 250	5 ± 10%	165	0.55	32	FM	CMOS	7-201
4096K	512K × 8	TMS27PC040-10 TMS27PC040-12 TMS27PC040-15	100 120 150	5 ± 10%	275	0.55	32	FM	CMOS	7-211
	256K × 16	TMS27PC240-10 TMS27PC240-12 TMS27PC240-15	100 120 150	5 ± 10%	275	0.55	44	FN	CMOS	7-221

† DD Plastic Thin Small-Outline Package
DU Plastic Thin Small-Outline Reverse Form Package
FM Plastic Leaded Chip Carrier
FN Plastic Leaded Chip Carrier
N Plastic Dual In-Line Package (DIP)

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GENERAL CONCEPTS AND TYPES OF MEMORIES

Address – Any given memory location in which data can be stored or from which it can be retrieved.

Automatic Chip-Select/Power Down – see Chip Enable Input.

Bit – Contraction of *binary digit* i.e., a 1 or a 0. In electrical terms, the value of a bit can be represented by the presence or absence of charge, voltage, or current.

Byte – A word of eight bits (see Word).

C of C – Certification of Conformance.

CDIP – Ceramic Dual In-Line Package.

CERPAC – CERamic flat PACk (hermetic).

CMOS – A complementary MOS technology that uses transistors with electron (N-channel) and hole (P-channel) conduction.

Chip Enable Input – A control input to an integrated circuit that, when active, permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and, when inactive, causes the integrated circuit to be in a reduced-power standby mode.

Chip Select Input – Chip select inputs are gating inputs that control the input to, and output from, the memory. They may be of two kinds:

1. Synchronous – Clocked/latched with the memory clock. Affects the inputs and outputs for the duration of that memory cycle.
2. Asynchronous – Has direct asynchronous control of inputs and outputs. In the read mode, an asynchronous chip select functions like an output enable.

Column Address Strobe (CAS) – A clock used in dynamic RAMs to control the input of column addresses. It can be active high (CAS) or active low ($\overline{\text{CAS}}$).

Data – Any information stored or retrieved from a memory device.

Die – Unpackaged semiconductor.

DIP – Dual In-line Package.

DESC – Defense Electronics Supply Center.

Dynamic (Read/Write) Memory (DRAM) – A read/write memory in which the cells require the repetitive application of control signals in order to retain the stored data.

NOTES:

1. The words "read/write" can be omitted from the term when no misunderstanding will result.
2. Such repetitive application of the control signals is normally called a refresh operation.
3. A dynamic memory might use static addressing or sensing circuits.
4. This definition applies whether the control signals are generated inside or outside the integrated circuit.

EPIC™ – Enhanced Performance Implanted CMOS.

Erasable and Programmable Read-Only Memory (EPROM) – A field-programmable read-only memory that can have the data content of each memory cell altered more than once.

Erase – Typically associated with EPROMs and Flash Memories. The procedure whereby programmed data is removed and the device returns to its unprogrammed state.

ESD – Electrostatic Discharge.

Extended Data Output – Extended data out allows for data output rates of up to 40 MHz for 60 ns devices. When keeping the same row address while selecting random column addresses, the time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP}, the maximum $\overline{RAS}$ low time.

Extended data out does not enter the DQs into the high-impedance state with the rising edge of $\overline{CAS}$. The output remains valid for the system to latch the data. After $\overline{CAS}$ goes high, the DRAM is decoding the next address. $\overline{OE}$ and $\overline{WE}$ can be used to control the output impedance. Descriptions of $\overline{OE}$ and $\overline{WE}$ further explains EDO operation benefit.

Field Memory (FMEM) – A serial-access memory that performs high-speed, asynchronous read/write operations. (Used mainly for fields of digital TV/VTR that require higher speed operation, lower power consumption, and larger capacity.)

Field-Programmable Read-Only Memory – See One-Time Programmable Read-Only Memory.

FIFO – First-In, First-Out.

Fit – A failure rate of one failure in one billion hours.

Fixed Memory – A common term for ROMs, EPROMs, EEPROMs, etc., containing data that is not normally changed. A more precise term for EPROMs and EEPROMs is nonvolatile since their data can be easily changed.

Flash Memory – A nonvolatile memory that can be field-programmed like an OTP PROM or EPROM but that can be electrically erased by a combination of electrical signals at its inputs.

FRAM – First-in first-out pseudo-static RAM or Field RAM.

Fully Static RAM – In a fully static RAM, the periphery as well as the memory array is fully static. The periphery is thus always active and ready to respond to input changes without the need of clocks. There is no precharge required for static periphery.

GENERIC DATA – Group A, B, C, & D Quality Conformance Data.

JAN – Joint Army Navy. Specifically, a JM38510 qualified device.

JANB – Class B screened JAN device.

JANS – Class S screened JAN device.

JEDEC – Joint Electronic Device Engineering Council.

JTAG – Joint Test Action Group.

K – When used in the context of specifying a given number of bits of information, 1K = 2^{10} = 1024 bits. Thus, 64K = 64 x 1024 = 65 536 bits.

Mask-Programmed Read-Only Memory – A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Memory – A medium capable of storing information that can be retrieved.

Memory Card – A pocket-size memory storage system.

Memory Cell – The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

Metal-Oxide Semiconductor (MOS) – The technology involving photolithographic layering of metal and oxide to produce a semiconductor device.

MIL-M-38510 – A military controlling specification pertaining mainly to JAN-qualified devices (microcircuits).

MIL-STD-883 – A military controlling specification containing detailed descriptions of the screening processes pertaining to Class B and Class S devices (microcircuits).

NMOS – A type of MOS technology in which the basic conduction mechanism is governed by electrons. (Short for N-channel MOS.)

Nonvolatile Memory – A memory in which the data content is maintained whether the power supply is connected or not.

OTP – One-Time Programmable.

One-Time Programmable (OTP) Read-Only Memory – A read-only memory that, after being manufactured, can have the data content of each memory cell altered once. Also referred to as OTP.

Output Enable – A control input that, when true, permits data to appear at the memory output, and when false, causes the output to assume a high-impedance state. (See also chip select.)

PCMCIA – Personal Computer Memory Card International Association.

PDIP – Plastic Dual-Inline Package.

PLCC – Plastic Leaded Chip Carrier.

PMOS – A type of MOS technology in which the basic conduction mechanism is governed by holes. (Short for P-channel MOS.)

Parallel Access – A feature of a memory by which all the bits of a byte or word are entered simultaneously at several inputs or retrieved simultaneously from several outputs.

Power Down – A mode of a memory during which the device is operating in a low-power or standby mode. Normally read or write operations of the memory are not possible under this condition.

Program – Typically associated with EPROM and OTP memories, the procedure whereby logical 0s (or 1s) are stored into various desired locations in a previously erased device.

Program Enable – An input signal that, when true, puts a programmable memory device into the program mode.

Programmable Read-Only Memory (PROM) – See One-Time Programmable (OTP) Read-Only Memory.

Printed Wiring Board (PWB) – A substrate of epoxy glass, clad material, or other material upon which a pattern of conductive traces is formed to interconnect the components that are mounted upon it.

Read – A memory operation whereby data is output from a desired address location.

Read-Only Memory (ROM) – A memory in which the contents are not intended to be altered during normal operation. NOTE: Unless otherwise qualified, the term "read-only memory" implies that the contents are determined by its structure and are unalterable.

Read/Write Memory – A memory in which each cell may be selected by applying appropriate electrical input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electrical input signals.

Row Address Strobe (RAS) – A clock used in dynamic RAMs to control the input of the row addresses. It can be active high (RAS) or active low ($\overline{\text{RAS}}$).

SCD – Source Control Drawings.

Scaled-MOS (SMOS) – MOS technology under which the device is scaled down in size in three dimensions and in operating voltages allowing for improved performance.

SDRAM – Synchronous Dynamic Random Access Memory. SDRAM synchronizes all address, data and control signals with the system clock. This makes the data transfer rates much higher than can be attained with asynchronous data. System design will be made easier with timing relationships now similar to other system operations.

Semi-Static (Quasi-Static, Pseudo-Static) RAM – In a semi-static RAM, the periphery is clock-activated (i.e., dynamic). Thus the periphery is inactive until clocked, and only one memory cycle is permitted per clock. The peripheral circuitry must be allowed to reset after each active memory cycle for a minimum precharge time. No refresh is required.

Serial Access – A feature of a memory by which all the bits are entered sequentially at a single input or retrieved sequentially from a single output.

SIMM – Single In-Line Memory Module.

Small Outline Integrated Circuit (SOIC) – A package in which an integrated circuit chip can be mounted to form a surface-mounted component. It is made of a plastic material that can withstand high temperatures and has leads formed in a gull-wing shape along its two longer sides for connection to a PWB footprint.

SMD – Standard Military Drawing.

SOLCC – Small Outline Leadless Ceramic Chip Carrier.

SOJ – Small Outline J-lead package.

SOP – Small Outline Package.

SQFP – Small Quad Flat Pack.

Static RAM (SRAM) – A read/write random-access device within which information is stored as latched voltage levels. The memory cell is a static latch that retains data as long as power is applied to the memory array. No refresh is required. The type of periphery circuitry sub-categorizes static RAMs.

ThinSOJ – (TSOJ) Thin Small-Outline J-Lead package.

ThinSOP – (TSOP) Thin Small-Outline package.

Very-Large-Scale Integration (VLSI) – The description of an IC technology that is much more complex than large-scale integration (LSI) and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

Video RAM (VRAM) – A dual-port dynamic random-access memory with an on-chip serial data register.

Volatile Memory – A memory in which the data content is lost when the power supply is disconnected.

Word – A series of one or more bits that occupy a given address location and then can be stored and retrieved in parallel.

Write – A memory operation whereby data is written into a desired address location.

Write Enable – A control signal that when true causes the memory to assume the write mode, and when false causes it to assume the read mode.

ZIP – Zig-zag In-line Package.

OPERATING CONDITIONS AND CHARACTERISTICS (INCLUDING LETTER SYMBOLS)

Capacitance

The inherent capacitance on every pin, which can vary with various inputs and outputs.

Example symbology:

C_i	Input capacitance
C_o	Output capacitance
$C_{i(D)}$	Input capacitance, data input

Current

High-level input current, I_{IH}

The current into an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}

The current into* an output with input conditions applied that, according to the product specification, establishes a high level at the output.

Low-level input current, I_{IL}

The current into an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}

The current into* an output with input conditions applied that, according to the product specification, establishes a low level at the output.

Off-state (high-impedance state) output current (of a three-state output,) I_{OZ}

The current into* an output having three-state capability with input conditions applied that according to the product specification establishes the high-impedance state at the output.

Short-circuit output current, I_{OS}

The current into* an output when the output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{BB}, I_{CC}, I_{DD}, I_{PP}

The current into, respectively, the V_{BB}, V_{CC}, V_{DD}, V_{PP} supply terminals.

*Current out of a terminal is given as a negative value.

Operating Free-Air Temperature

The temperature (T_A) range over which the device operates and the range which meets the specified electrical characteristics.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that, according to the product specification, establishes a high level at the output.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values is used to represent the binary variables.

NOTE: The most positive value of low-level input voltage is specified for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that, according to the product specification, establishes a low level at the output.

Supply voltages, V_{BB}, V_{CC}, V_{DD}, V_{PP}

The voltages supplied to the corresponding voltage pins that are required for the device to function. From one to four of these supplies may be necessary, along with ground (V_{SS}).

Time Intervals

New or revised data sheets in this book use letter symbols in accordance with standards recently adopted by JEDEC, the IEEE, and the IEC. Two basic forms are used. The first form is usually used when intervals can be easily classified as access, cycle, disable, enable, hold, refresh, setup, transition, or valid times and for pulse durations. The second form can be used generally, but in this book primarily, for time intervals not easily classifiable. The second (unclassified) form is described first. Since some manufacturers use this form for all time intervals, symbols in the unclassified form are given with the examples for most of the classified time intervals.

Unclassified time intervals

Generalized letter symbols can be used to identify almost any time interval without classifying it using traditional or contrived definitions. Symbols for unclassified time intervals identify two signal events listed in from-to sequence using the format:

$t_{AB\text{-}CD}$

Subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval. Every effort is made to keep the A and C subscript length down to one letter, if possible (e.g., R for $\overline{RAS}$ and C for $\overline{CAS}$).

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high

L = low or transition to low

V = a valid steady-state level

X = unknown, changing, or "don't care" level

Z = high-impedance (off) state

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur.

Classified time intervals (general comments, specific times follow)

Because of the information contained in the definitions, frequently the identification of one or both of the two signal events that begin and end the intervals can be significantly shortened compared to the unclassified forms. For example, it is not necessary to indicate in the symbol that an access time ends with valid data at the output. However, if both signals are named (e.g., in a hold time), the from-to sequence is maintained.

Access time

The time interval between the application of a specific input pulse and the availability of valid signals at an output.

Example symbology:

Classified	Unclassified	Description
$t_{a(A)}$	t_{AVQV}	Access time from address
$t_{a(S)}$, $t_{a(CS)}$	t_{SLQV}	Access time from chip select (low)

Cycle time

The time interval between the start and end of a cycle.

NOTE: The cycle time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval that must be allowed for the digital circuit to perform a specified function (e.g., read, write, etc.) correctly.

Example symbology:

Classified	Unclassified	Description
$t_{c(R)}$, $t_{c(rd)}$	$t_{AVAV(R)}$	Read cycle time
$t_{c(W)}$	$t_{AVAV(W)}$	Write cycle time

NOTE: R is usually used as the abbreviation for "read"; however, in the case of dynamic memories, "rd" is used to permit R to stand for $\overline{RAS}$.

Disable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Example symbology:

Classified	Unclassified	Description
$t_{dis(S)}$	t_{SHQZ}	Output disable time after chip select (high)
$t_{dis(W)}$	t_{WLQZ}	Output disable time after write enable (low)

These symbols supersede the older forms t_{PVZ} or t_{PXZ}.

Enable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: For memories these intervals are often classified as access times.

Example symbology:

Classified	Unclassified	Description
$t_{en(SL)}$	t_{SLQV}	Output enable time after chip select low

These symbols supersede the older from t_{PZV}.

Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time can have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{h(D)}$	t_{WHDX}	Data hold time (after write high)
$t_{h(RHrd)}$	t_{RHWH}	Read (write enable high) hold time after $\overline{RAS}$ high
$t_{h(CHrd)}$	t_{CHWH}	Read (write enable high) hold time after $\overline{CAS}$ high
$t_{h(CLCA)}$	$t_{CL\text{-}CAX}$	Column address hold time after $\overline{CAS}$ low
$t_{h(RLCA)}$	$t_{RL\text{-}CAX}$	Column address hold time after $\overline{RAS}$ low
$t_{h(RA)}$	$t_{RL\text{-}RAX}$	Row address hold time (after $\overline{RAS}$ low)

These last three symbols supersede the older forms:

NEW FORM	OLD FORM
$t_{h(CLCA)}$	$t_{h(AC)}$
$t_{h(RLCA)}$	$t_{h(ARL)}$
$t_{h(RA)}$	$t_{h(AR)}$

NOTE: The from-to sequence in the order of subscripts in the unclassified form is maintained in the classified form. In the case of hold times, this causes the order to seem reversed from what would be suggested by the terms.

Pulse duration (width)

The time interval between the specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

Classified	Unclassified	Description
$t_{w(W)}$	t_{WLWH}	Write pulse duration
$t_{w(RL)}$	t_{RLRH}	Pulse duration, $\overline{RAS}$ low

Refresh time interval

The time interval between the beginnings of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

NOTE: The refresh time interval is the actual time interval between two refresh operations and is determined by the system in which the digital circuit operates. A maximum value is specified that is the longest interval for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
t_{rf}		Refresh time interval

Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time can have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{su(D)}$	t_{DVWH}	Data setup time (before write high)
$t_{su(CA)}$	t_{CAV-CL}	Column address setup time (before $\overline{CAS}$ low)
$t_{su(RA)}$	t_{RAV-RL}	Row address setup time (before $\overline{RAS}$ low)

Transition times (also called rise and fall times)

The time interval between two reference points (10% and 90% unless otherwise specified) on the same waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

Example symbology:

Classified	Unclassified	Description
t_t		Transition time (general)
$t_{t(CH)}$	t_{CHCH}	Low-to-high transition time of $\overline{CAS}$
$t_{r(C)}$	t_{CHCH}	$\overline{CAS}$ rise time
$t_{f(C)}$	t_{CLCL}	$\overline{CAS}$ fall time

Valid time

(a) General

The time interval during which a signal is (or should be) valid.

(b) Output data-valid time

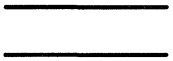
The time interval in which output data continues to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

Example symbology:

Classified	Unclassified	Description
$t_{v(A)}$	t_{AXQX}	Output data valid time after change of address

This supersedes the older form t_{PVX}.

TIMING DIAGRAMS CONVENTIONS

Timing Diagram Symbol	Meaning	
	Input Forcing Functions	Output Response Functions
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated intervals
	Low-to-high changes permitted	Will be changing from low to high sometime during designated intervals
	Don't care	State unknown or changing
	(Does not apply)	Centerline represents high-impedance (off) state.

Contents

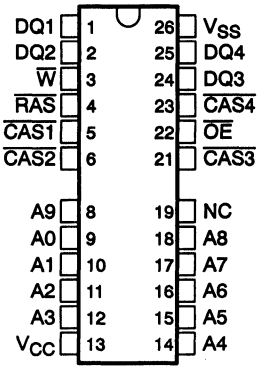
CHAPTER 4. DYNAMIC RANDOM-ACCESS MEMORY (DRAM)

- **Organization . . . 1048576 × 4**
- **Single 5-V Power Supply for TMS44460/P (±10% Tolerance)**
- **Single 3.3-V Power Supply for TMS46460/P (±10% Tolerance)**
- **Low Power Dissipation (for TMS46460P)**
  - **200-µA CMOS Standby**
  - **200-µA Self Refresh**
  - **300-µA Extended-Refresh Battery Backup**
- **Performance Ranges:**

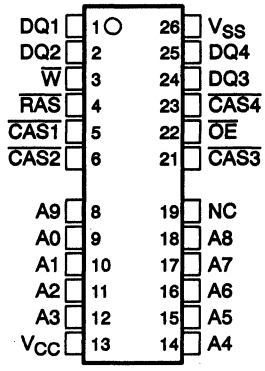
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
'4x460/P-60	60 ns	15 ns	30 ns	110 ns
'4x460/P-70	70 ns	18 ns	35 ns	130 ns
'4x460/P-80	80 ns	20 ns	40 ns	150 ns

- **Four Separate $\overline{CAS}$x Pins Provide for Separate I/O Operation**
- **Parity-Mode Operation**
- **Enhanced Page-Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  - **1024-Cycle Refresh in 16 ms**
  - **128 ms (Max) Low-Power, Self-Refresh Version (TMS4x460P)**
- **3-State Unlatched Output**
- **Texas Instruments EPIC™ CMOS Process**
- **Operating Free-Air Temperature Range 0°C to 70°C**

DJ PACKAGE
(TOP VIEW)



DGA PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS1}$–$\overline{CAS4}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V or 3.3-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

ADVANCE INFORMATION

description

The TMS4x460 series are high-speed, 4194304-bit dynamic random-access memories, organized as 1048576 words of four bits each. The TMS4x400P series are high-speed, low-power, self-refresh with extended-refresh, 4194304-bit dynamic random-access memories, organized as 1048576 words of four bits each. Both series employ state-of-the-art enhanced performance implanted CMOS EPIC™ technology for high performance, reliability, and low power.

AVAILABLE OPTIONS

DEVICE	POWER SUPPLY	SELF-REFRESH BATTERY BACKUP	REFRESH CYCLES
TMS44460	5 V	—	1024 in 16 ms
TMS44460P	5 V	YES	1024 in 128 ms
TMS46460	3.3 V	—	1024 in 16 ms
TMS46460P	3.3 V	YES	1024 in 128 ms

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

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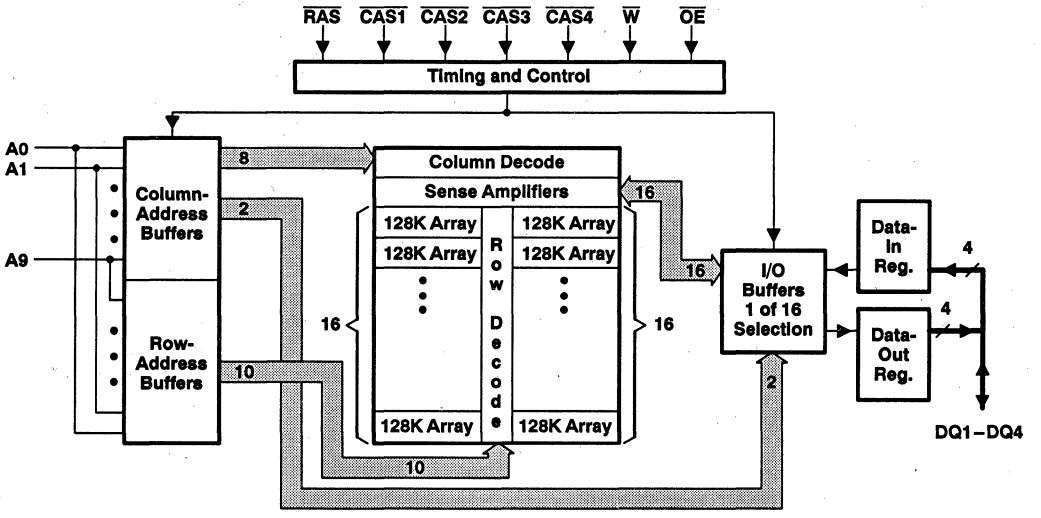
description (continued)

Four separate $\overline{CAS}$ pins ($\overline{CAS1}$–$\overline{CAS4}$) provide for separate I/O operations, allowing this device to operate in parity mode. The TMS44460 also functions in enhanced page mode, similar to the TMS44400.

The TMS4x400 and TMS4x400P are offered in a 24/26-lead plastic small outline (TSOP) package (DGA suffix) and a 300-mil 24/26-lead plastic surface mount SOJ package (DJ suffix). Both packages are characterized for operation from 0°C to 70°C.

functional block diagram



operation

parity mode

Four $\overline{CASx}$ pins ($\overline{CAS1}$–$\overline{CAS4}$) are provided to give independent control of the four data I/O pins (DQ1–DQ4). For read or write cycles, the column addressed is latched on the first $\overline{CASx}$ falling edge. Each $\overline{CASx}$ pin going low enables its corresponding DQ pin with data coming from the column address latched on the first $\overline{CASx}$ falling edge. All address setup and hold parameters are referenced to the first $\overline{CASx}$ falling edge. The delay time from $\overline{CASx}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{CASx}$ to its corresponding DQx pin.

To latch in a new column address, all four $\overline{CASx}$ pins must be brought high. The column precharge time (see parameter t_{CP}) is measured from the last $\overline{CASx}$ rising edge to the first $\overline{CASx}$ falling edge of the new cycle. In order for a column address to remain valid while toggling $\overline{CASx}$, there exists a minimum setup time (t_{CLCH}) where at least one $\overline{CASx}$ must be brought low before all other $\overline{CASx}$ pins are taken high.

For early-write cycles, the data is latched on the first $\overline{CASx}$ falling edge. Only the DQs that have the corresponding $\overline{CASx}$ low are written into. Each $\overline{CASx}$ has to meet t_{CAS} minimum in order to ensure writing into the storage cell. To latch a new address and new data, all $\overline{CASx}$ pins must come high and meet t_{CP}.

This DQ independence allows the TMS4x460/P to provide four parity bits in memory designs that normally require the use of four 1-megabit × 1 DRAMs.

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CASx}$ page-cycle time used. With minimum $\overline{CASx}$ page-cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CASx}$ is high. The falling edge of $\overline{CASx}$ latches the column addresses. This feature allows the TMS4x400 to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when $\overline{CASx}$ transitions low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CASx}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CASx}$ low) if t_{AA} max (access time from column address) has been satisfied. If column addresses for the next cycle are valid at the time $\overline{CASx}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CASx}$).

address (A0–A9)

Twenty address bits are required to decode 1 of 1 048 576 storage-cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CASx}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CASx}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CASx}$ is used as a chip select, activating the output buffer as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. $\overline{W}$ can be driven from standard TTL circuits (TMS44460/P) or low-voltage TTL circuits (TMS46460/P) without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CASx}$ (early write), data out remain in the high-impedance state for the entire cycle, permitting a write operation independent of the state of $\overline{OE}$. This permits early-write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ1–DQ4)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CASx}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CASx}$ and $\overline{OE}$ are low. $\overline{CASx}$ or $\overline{OE}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CASx}$ to be brought low for the output buffers to go into the low-impedance state. They remain in the low-impedance state until either $\overline{OE}$ or $\overline{CASx}$ is brought high.

refresh

A refresh operation must be performed at least once every 16 ms (128 ms for TMS4x400P) to retain data. This can be achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CASx}$ at the high (inactive) level,

refresh (continued)

conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh. Hidden refresh can be performed while maintaining valid data at the output. This is accomplished by holding $\overline{\text{CASx}}$ at V_{IL} after a read operation and cycling $\overline{\text{RAS}}$ after a specified precharge period, similar to a $\overline{\text{RAS}}$-only refresh cycle. The external address is ignored during the hidden-refresh cycle.

$\overline{\text{CASx}}$-before-$\overline{\text{RAS}}$ refresh (CBR)

CBR refresh is utilized by bringing $\overline{\text{CASx}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CSR}) and holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{\text{CASx}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 300-µA (TMS46460P) or 500-µA (TMS44460P) refresh current is available on the low-power devices. Data integrity is maintained using CBR refresh with a period of 125 µs while holding $\overline{\text{RAS}}$ low for less than 1 µs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self refresh

The self-refresh mode is entered by dropping $\overline{\text{CASx}}$ low prior to $\overline{\text{RAS}}$ going low. $\overline{\text{CASx}}$ and $\overline{\text{RAS}}$ are both held low for a minimum of 100 µs. The chip is then refreshed by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{\text{RAS}}$ and $\overline{\text{CASx}}$ are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This ensures the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles must include at least one refresh ($\overline{\text{RAS}}$-only or CBR) cycle.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: TMS44460, TMS44460P ..... – 1 V to 7 V
TMS46460, TMS46460P ..... – 0.5 V to 4.6 V
Voltage range on any pin (see Note 1): TMS44460, TMS44460P ..... – 1 V to 7 V
TMS46460, TMS46460P ..... – 0.5 V to 4.6 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{sttg} ..... – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		'44460/P			'46460/P			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	2.4		6.5	2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TMS44460/P

PARAMETER		TEST CONDITIONS		'44460-60 '44460P-60		'44460-70 '44460P-70		'44460-80 '44460P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CASx}$ high			± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note)	V_{CC} = 5.5 V, Minimum cycle			105		90		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CASx}$ high, V_{IH} = 2.4 V (TTL)			2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CASx}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)	'44460		1		1		1	mA
			'44460P		500		500		500	µA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 4)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CASx}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CASx}$ low (CBR)			105		90		80	mA
I_{CC4}	Average page current (see Notes 4 and 5)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CASx}$ cycling			90		80		70	mA
I_{CC6}†	Self-refresh current (see Note 4)	$\overline{CASx}$< 0.2 V, $\overline{RAS}$< 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			500		500		500	µA
I_{CC7}	Standby current, outputs enabled (see Note 4)	$\overline{RAS}$ = V_{IH}, $\overline{CASx}$ = V_{IL} Data out enabled			5		5		5	mA
I_{CC10}†	Battery-backup current (with CBR)	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			500		500		500	µA

† For TMS44460P only

NOTES: 3. I_{CC} max is specified with no load connected.
4. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
5. Measured with a maximum of one address change while $\overline{CASx}$ = V_{IH}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TMS46460/P

PARAMETER		TEST CONDITIONS		'46460-60 '46460P-60		'46460-70 '46460P-70		'46460-80 '46460P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA (LVTTL)		2.4		2.4		2.4		V
		I_{OH} = – 100 µA (LVCMOS)		V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA (LVTTL)			0.4		0.4		0.4	V
		I_{OL} = 100 µA (LVCMOS)			0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{CAS}$x high			± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note)	V_{CC} = 3.6 V, Minimum cycle			70		60		50	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$x high, V_{IH} = 2 V (LVTTL)			2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$x high, V_{IH} = V_{CC} – 0.2 V (LVCMOS)	'46460		300		300		300	µA
			'46460P		200		200		200	µA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 4)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$x high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$x low (CBR)			70		60		50	mA
I_{CC4}	Average page current (see Notes 4 and 5)	V_{CC} = 3.6 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$x cycling			60		50		40	mA
I_{CC6}†	Self-refresh current (see Note 4)	$\overline{CAS}$x< 0.2 V, $\overline{RAS}$< 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			200		200		200	µA
I_{CC7}	Standby current, outputs enabled (see Note 4)	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$x = V_{II} Data out enabled			5		5		5	mA
I_{CC10}†	Battery-backup current (with CBR)	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			300		300		300	µA

† For TMS46460P only

NOTES: 4. I_{CC} max is specified with no load connected.
4. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
5. Measured with a maximum of one address change while $\overline{CAS}$x = V_{IH}

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A9		5	pF
$C_{i(RC)}$	Input capacitance, $\overline{CASx}$ and $\overline{RAS}$		7	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance		7	pF

NOTE 6: V_{CC} = 5 V ± .5 V for the TMS44460/P devices, V_{CC} = 3.3 V ± 0.3 V for the TMS46460/P devices, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'4x400-60 '4x400P-60		'4x400-70 '4x400P-70		'4x400-80 '4x400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CASx}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20	ns
t_{CLZ}	$\overline{CASx}$ to output in low-impedance state	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CASx}$ high (see Note 7)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 7)	0	15	0	18	0	20	ns

NOTE 7: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4x400-60 '4x400P-60		'4x400-70 '4x400P-70		'4x400-80 '4x400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 8)	110		130		150		ns
t_{RWC}	Cycle time, read-write (see Note 8)	155		181		205		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 8 and 9)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-write (see Note 8)	85		96		105		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 10)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 10)	60	10 000	70	10 000	80	10 000	ns
t_{RASS}	Pulse duration, $\overline{RAS}$ low, self refresh		100		100		100	µs
t_{CAS}	Pulse duration, $\overline{CASx}$ low (see Note 11)	10	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CASx}$ precharge time	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{RPS}	Precharge time after self refresh using $\overline{RAS}$	110		130		150		ns
t_{WP}	Pulse duration, write	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CASx}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 12)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CASx}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CASx}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CASx}$ low (early-write operation only)	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CASx}$ low	10		15		15		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{DH}	Hold time, data (see Note 12)	10		15		15		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{CLCH}	Hold time, $\overline{CASx}$ low to $\overline{CASx}$ high	5		5		5		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CASx}$ high (see Note 14)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 14)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CASx}$ low (early-write operation only)	10		15		15		ns
t_{WCR}	Hold time, $\overline{W}$ low after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{WHR}	Hold time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{CHS}	Hold time, $\overline{CASx}$ low after $\overline{RAS}$ high (self refresh)	–50		–50		–50		ns
t_{OEH}	Hold time, $\overline{OE}$ command	15		18		20		ns

NOTES: 8. All cycle times assume t_T = 5 ns.
9. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Referenced to the later of $\overline{CASx}$ or $\overline{W}$ in write operations
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

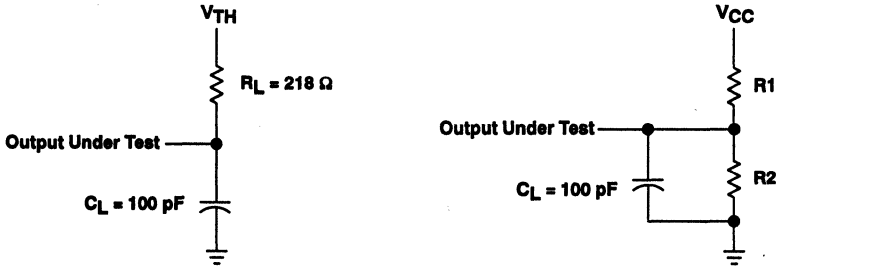
ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			'4x460-60 '4x460P-60		'4x460-70 '4x460P-70		'4x460-80 '4x460P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{OED}	Hold time, $\overline{OE}$ to data delay		15		18		20		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$		10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)		55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ high (CBR refresh only)		10		10		10		ns
t_{CRP}	Delay time, $\overline{CASx}$ high to $\overline{RAS}$ low		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ high		60		70		80		ns
t_{CSR}	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ low (CBR refresh only)		5		5		5		ns
t_{CWD}	Delay time, $\overline{CASx}$ low to $\overline{W}$ low (read-write operation only)		40		46		50		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CASx}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ low (see Note 15)		20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CASx}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ high		15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)		85		98		110		ns
t_{REF}	Refresh time interval	'4x460		16		16		16	ms
		'4x460P		128		128		128	ms
t_T	Transition time		2	30	2	30	2	30	ns

NOTE 15: The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT

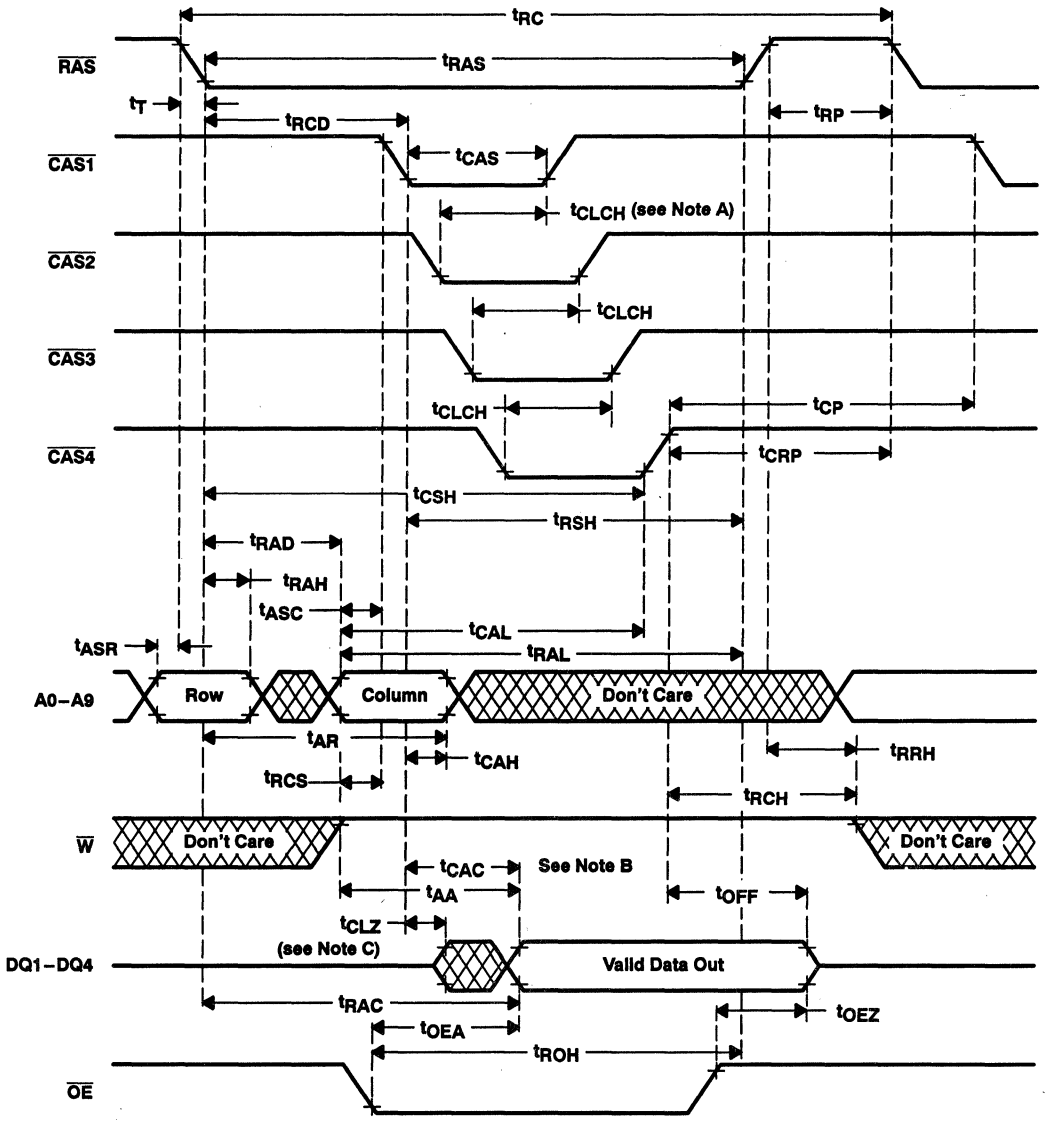
(b) ALTERNATE LOAD CIRCUIT

DEVICE	V_{CC} (V)	R1 (Ω)	R2 (Ω)	V_{TH} (V)	R_L (Ω)
46460/P	3.3	1178	868	1.4	500
44460/P	5	828	295	1.31	218

Figure 1. Load Circuits for Timing Parameters

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
C. Output can go from high-impedance to an invalid-data state prior to the specified access time.
D. $\overline{CASx}$ order is arbitrary.

Figure 2. Read-Cycle Timing (see Note D)

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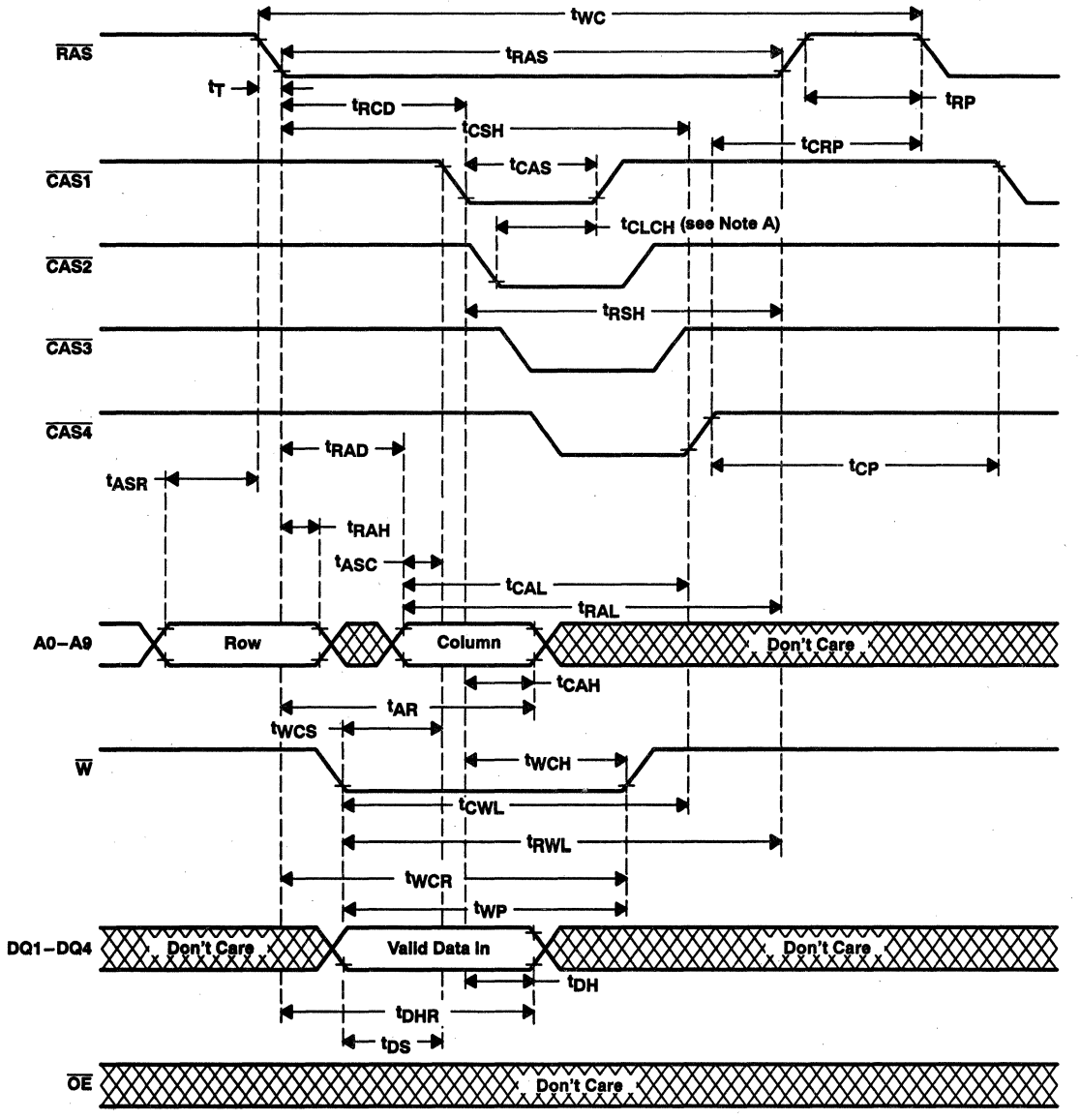
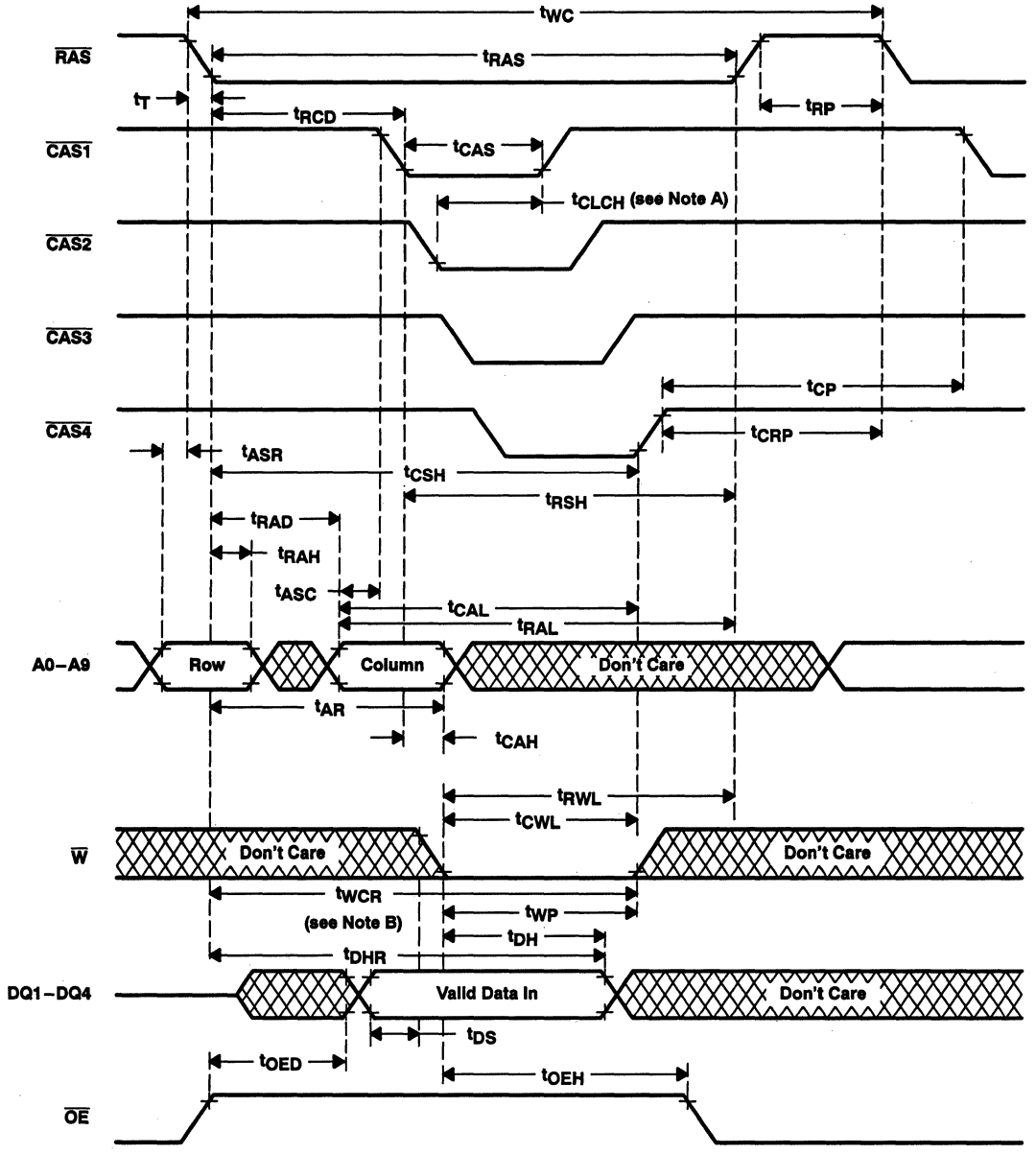
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{CASx}$ order is arbitrary.

Figure 3. Early-Write-Cycle Timing (see Note B)

PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{CAS}x$ going low, the parameter t_{CLCH} must be met.
B. Referenced to the later of either the first $\overline{CAS}x$ or $\overline{W}$ in write operations.
C. $\overline{CAS}x$ order is arbitrary.

Figure 4. Write-Cycle Timing (see Note C)

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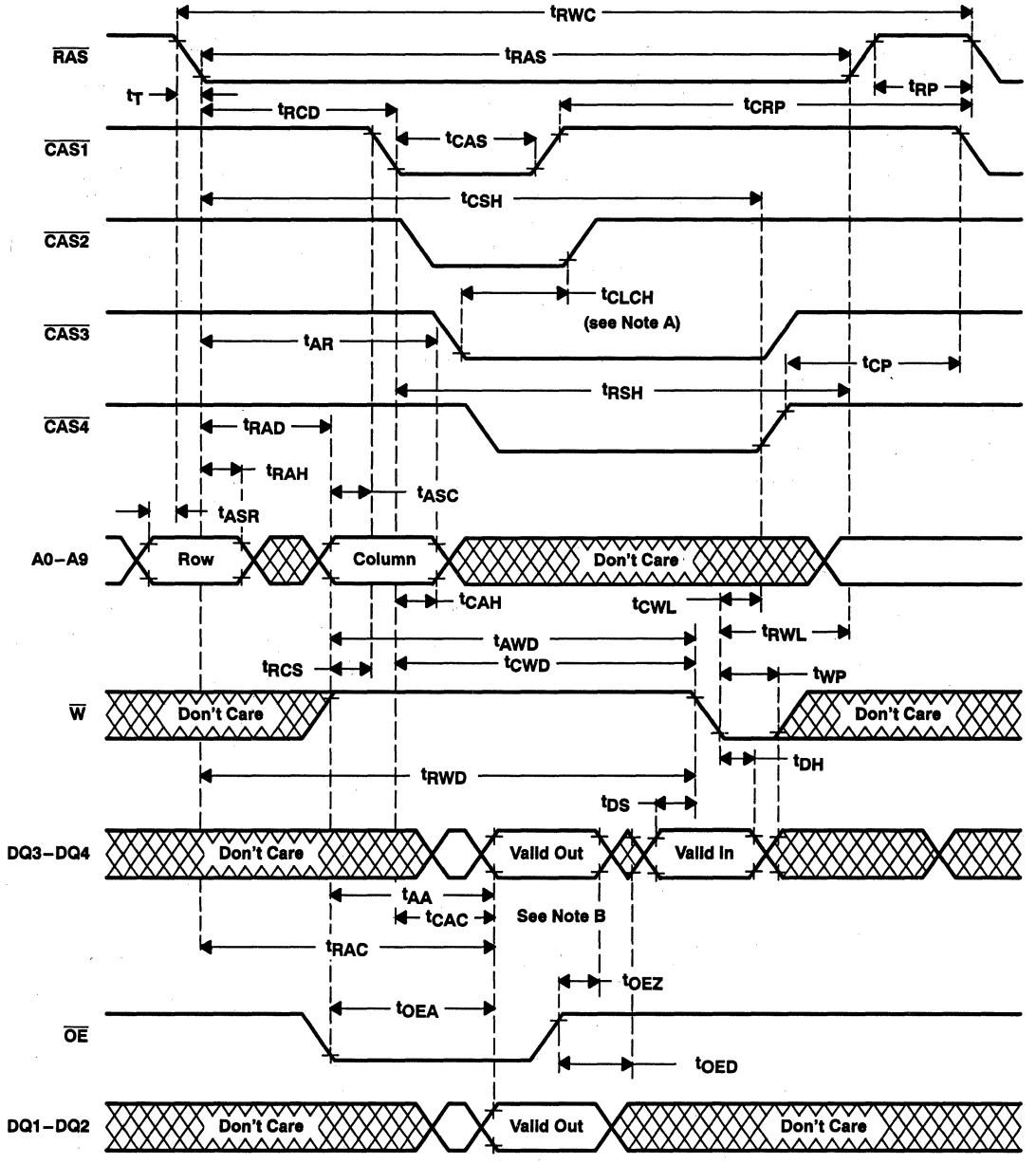
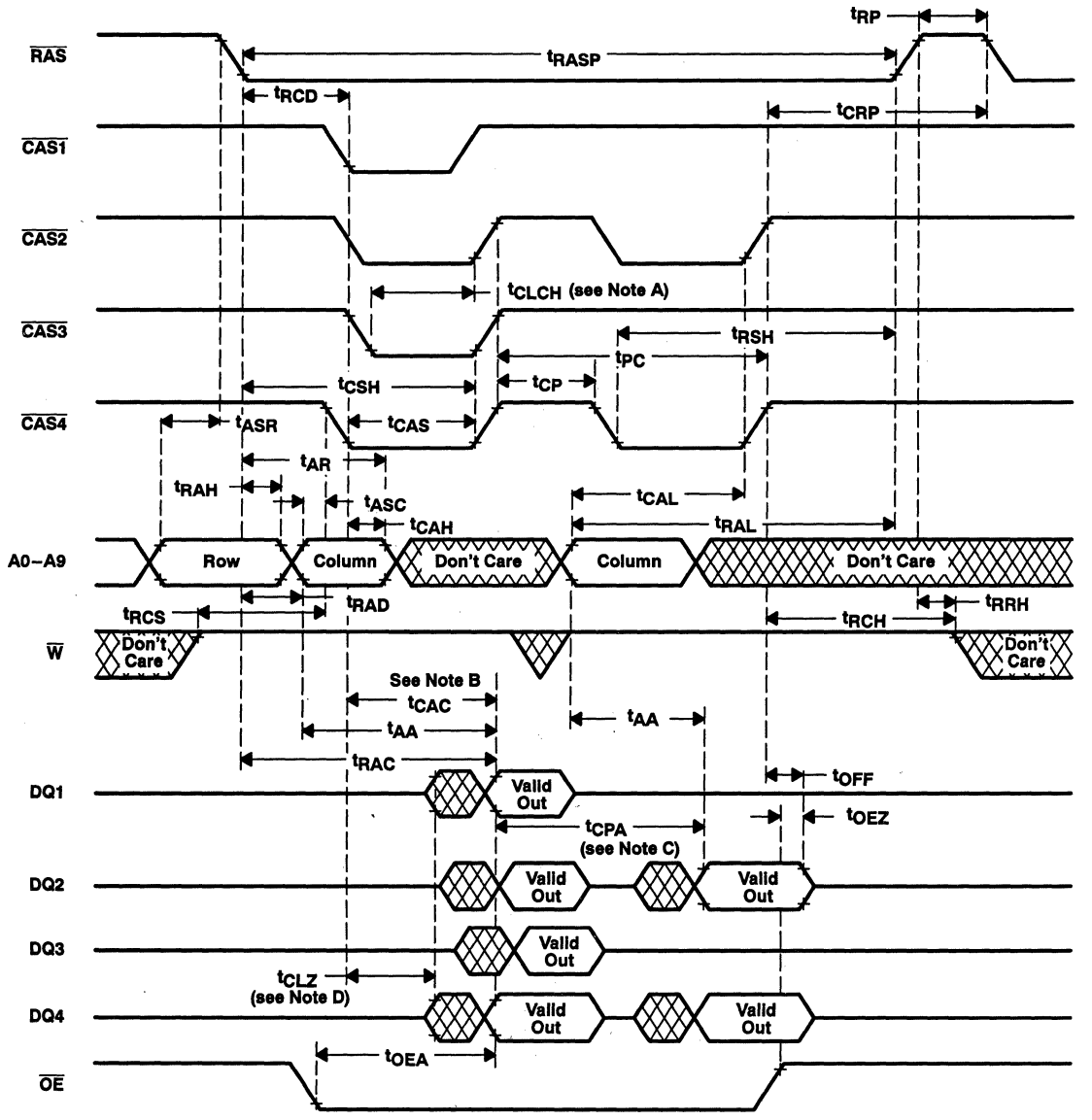
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
C. $\overline{CASx}$ order is arbitrary.

Figure 5. Read-Write/Read-Modify-Write-Cycle Timing (see Note C)

PARAMETER MEASUREMENT INFORMATION

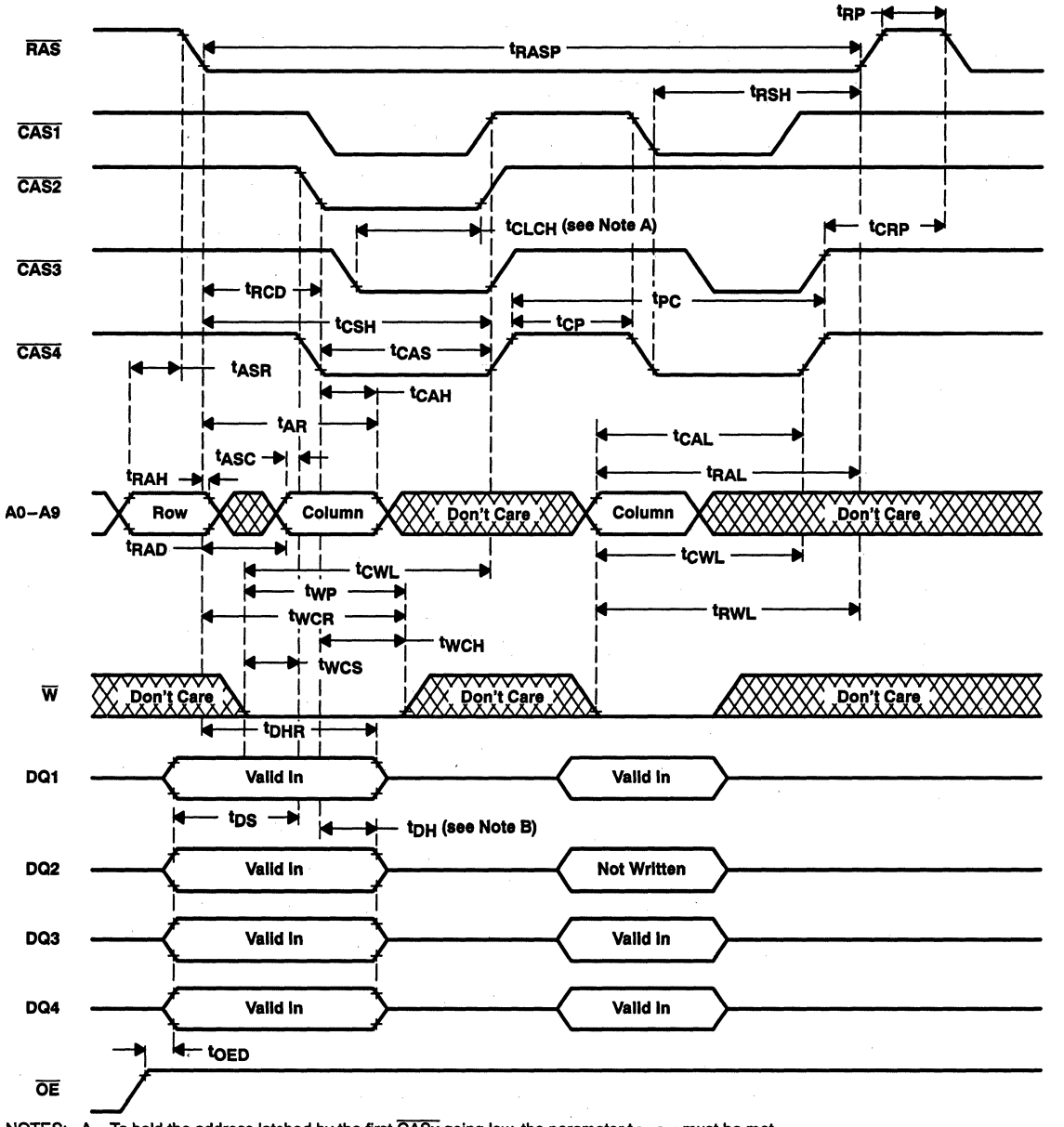


NOTES: A. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
C. Access time is t_{CPA} or t_{AA} dependent.
D. Output can go from high-impedance to an invalid-data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
F. $\overline{CASx}$ order is arbitrary.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing (see Notes E and F)

ADVANCE INFORMATION

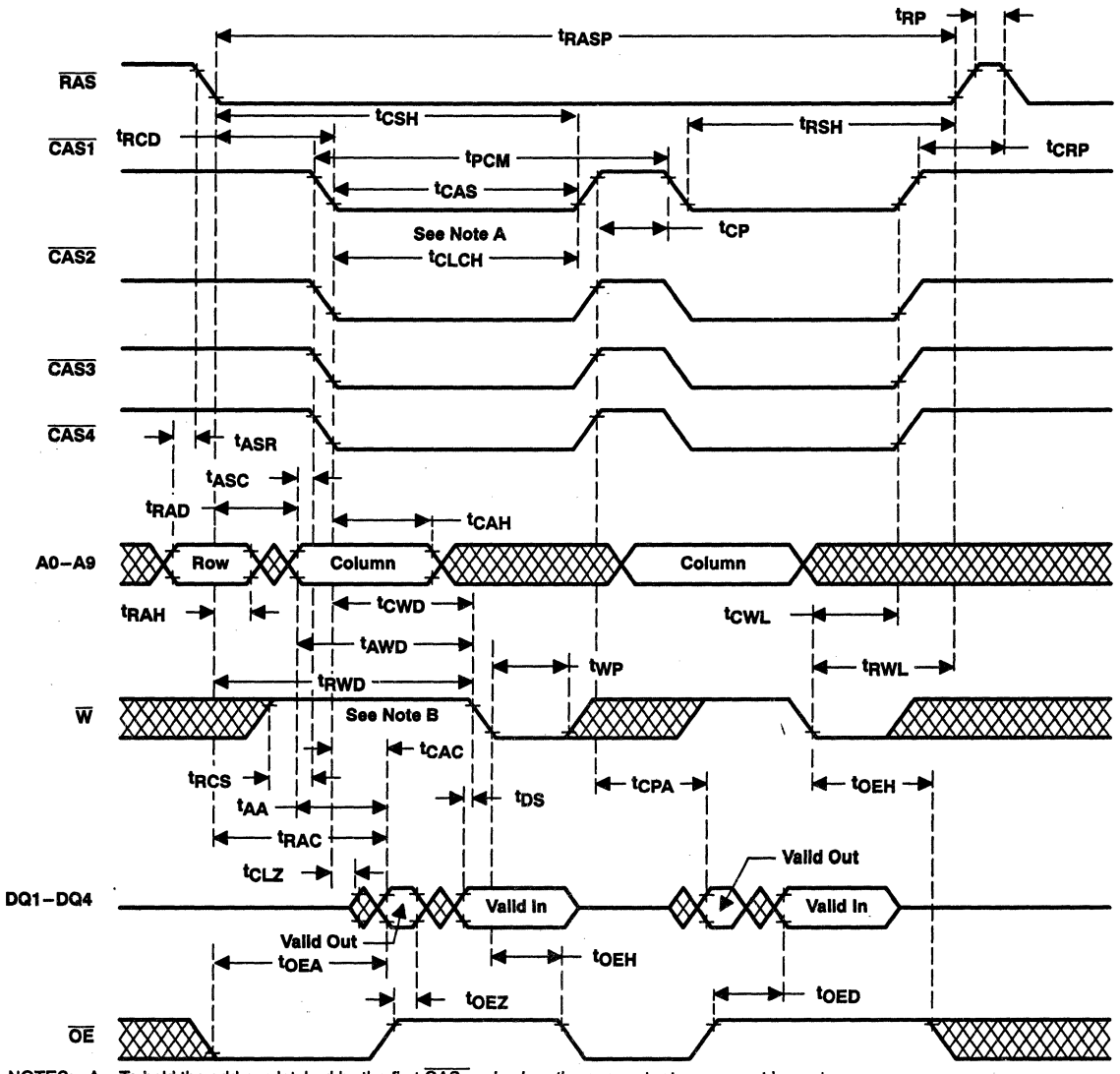
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to the later of either the first $\overline{CASx}$ or $\overline{W}$ in write operations.
C. $\overline{CASx}$ order is arbitrary.
D. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
C. $\overline{CASx}$ order is arbitrary.
D. A read or write cycle can be intermixed with read-modify-write cycles as long as the read- and write-cycle timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Read-Modify-Write Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

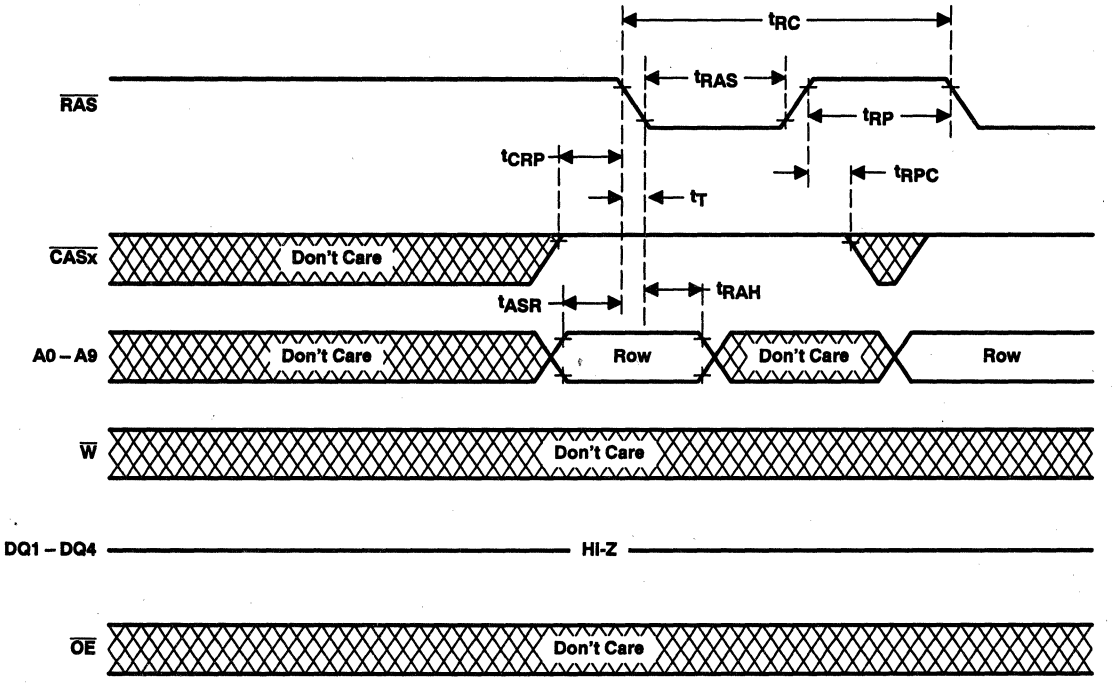
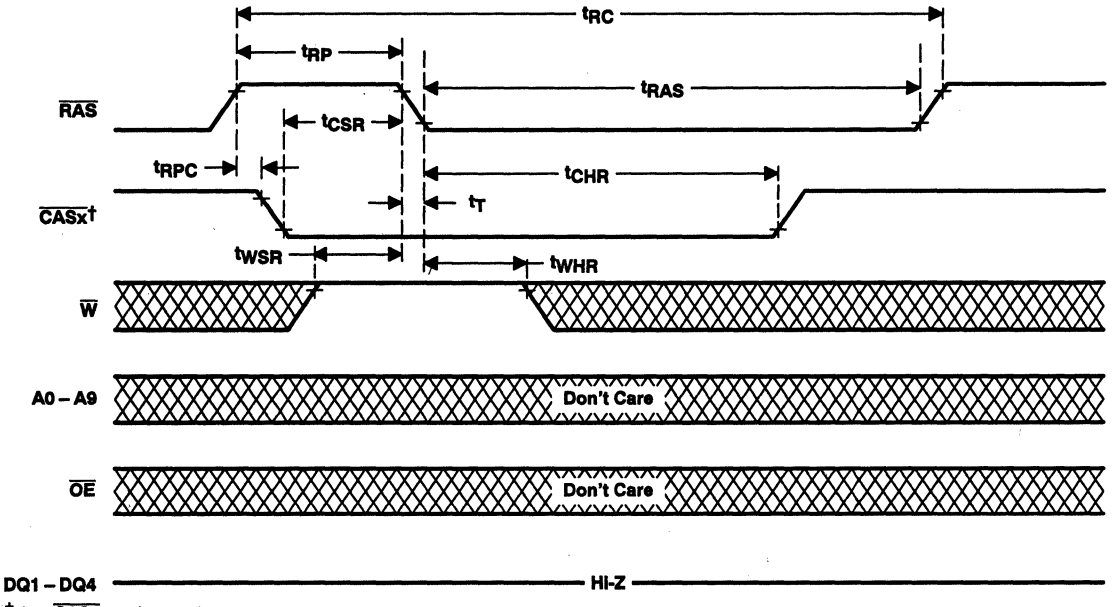


Figure 9. $\overline{RAS}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Any $\overline{CASx}$ can be used.

Figure 10. Automatic CBR Refresh-Cycle Timing

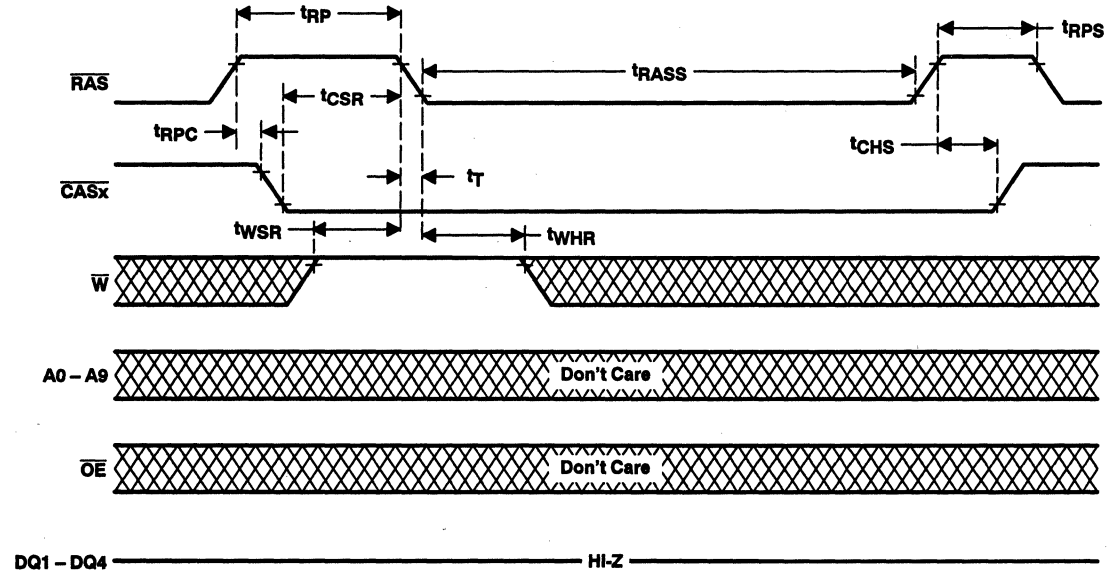


Figure 11. Self-Refresh-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

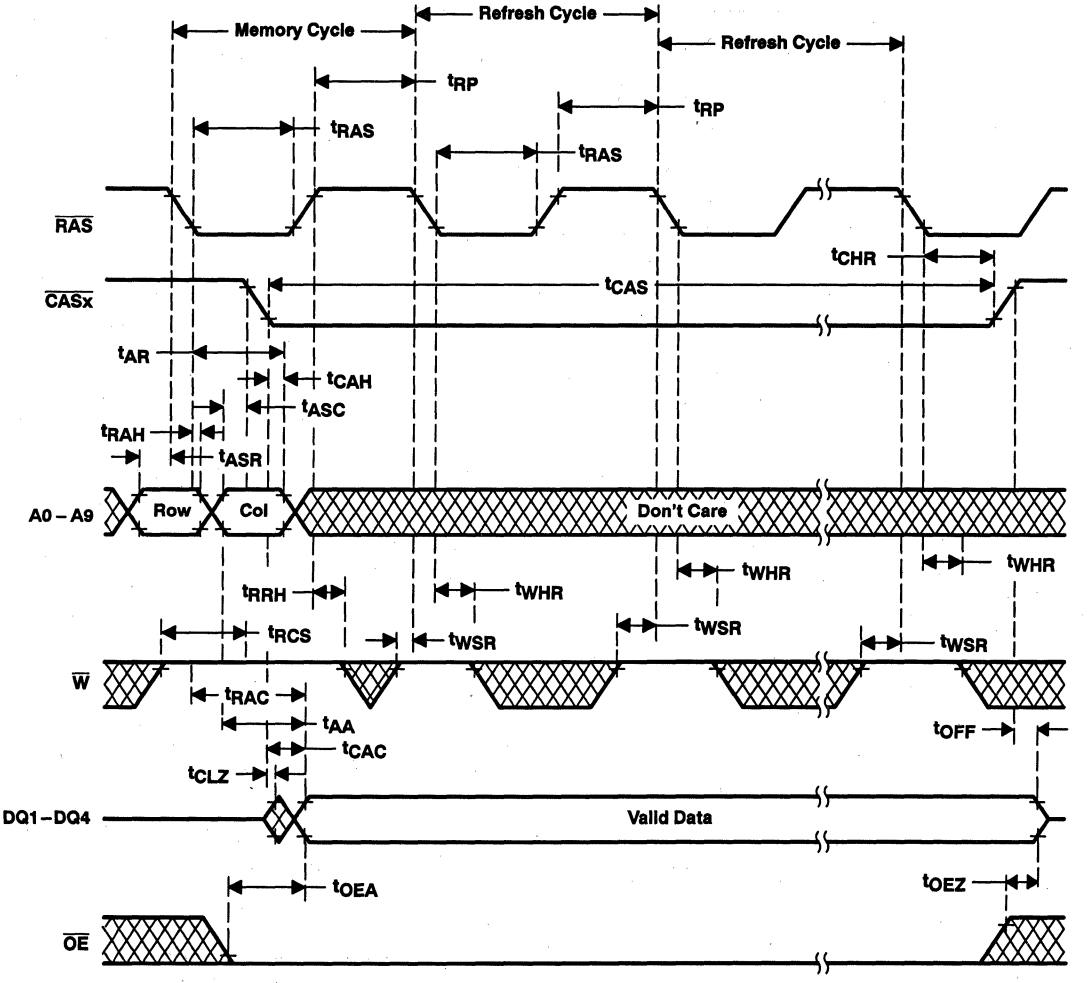


Figure 12. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

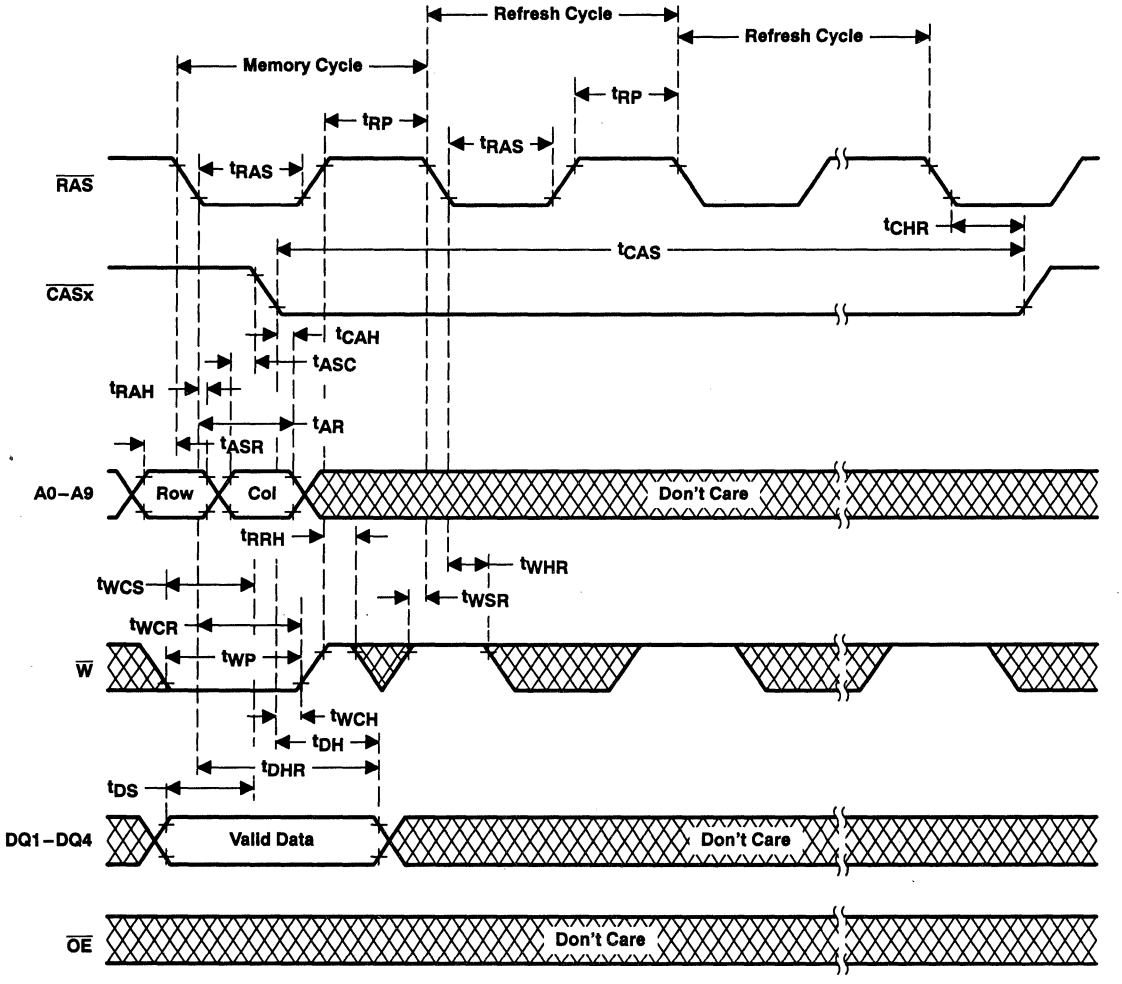
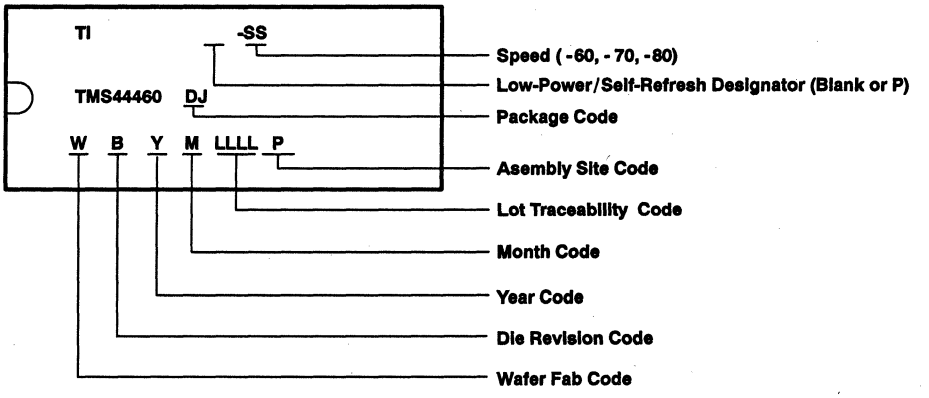


Figure 13. Hidden-Refresh-Cycle (Write) Timing

ADVANCE INFORMATION

device symbolization (TMS44460 illustrated)

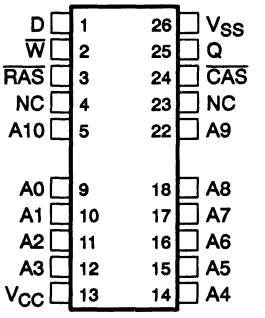


- **Organization . . . 4194304 × 1**
- **Single 5 V Power Supply, for TMS44100/P (±10% Tolerance)**
- **Single 3.3 V Power Supply, for TMS46100/P (±10% Tolerance)**
- **Low Power Dissipation (TMS46100P only)**
  - **200-µA CMOS Standby**
  - **200-µA Self Refresh**
  - **300-µA Extended-Refresh Battery Backup**
- **Performance Ranges:**

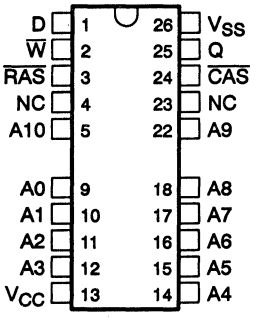
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
'4x100/P-60	60 ns	15 ns	30 ns	110 ns
'4x100/P-70	70 ns	18 ns	35 ns	130 ns
'4x100/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page-Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  - **1024-Cycle Refresh In 16 ms**
  - **128 ms (Max) for Low-Power, Self-Refresh Version (TMS4x100P)**
- **3-State Unlatched Output**
- **Texas Instruments EPIC™ Process**
- **Operating Free-Air Temperature Range 0°C to 70°C**

DGA PACKAGE
(TOP VIEW)



DJ PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V or 3.3-V Supply
V_{SS}	Ground

ADVANCE INFORMATION

description

The TMS4x100 series are high-speed, 4194304-bit dynamic random-access memories, organized as 4194304 words of one bit each. The TMS4x100P series are high-speed, low-power, self-refresh with extended-refresh, 4194304-bit dynamic random-access memories, organized as 4194304 words of one bit each. Both series employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low voltage.

DEVICE	POWER SUPPLY	SELF-REFRESH BATTERY BACKUP	REFRESH CYCLES
TMS44100	5 V	—	1024 in 16 ms
TMS44100P	5 V	YES	1024 in 128 ms
TMS46100	3.3 V	—	1024 in 16 ms
TMS46100P	3.3 V	YES	1024 in 128 ms

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4x100 and TMS4x100P are offered in a 20-/26-lead plastic surface-mount small-outline (TSOP) package (DGA suffix) and a 300-mil 20-/26-lead plastic surface-mount SOJ package (DJ suffix). Both packages are characterized for operation from 0°C to 70°C.

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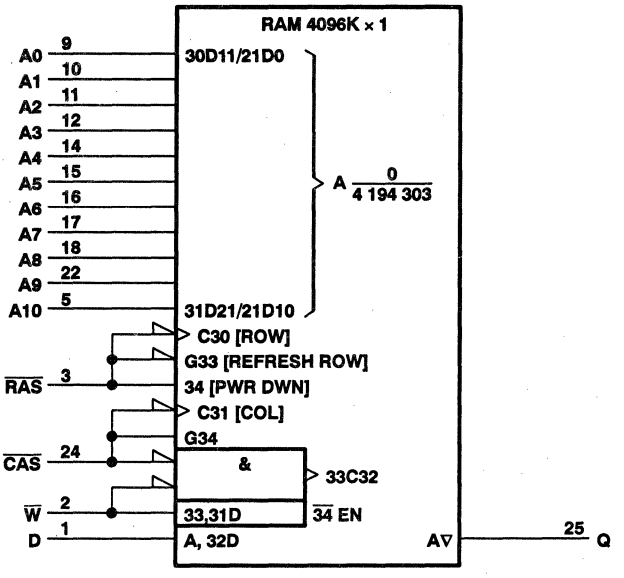
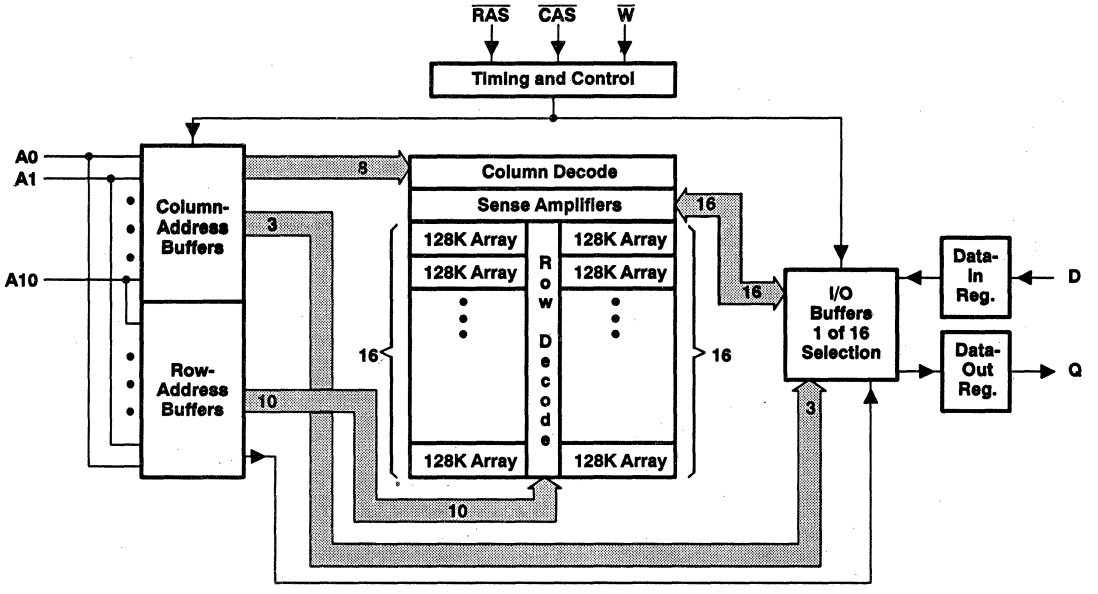
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



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operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS4x100 to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. If column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0–A10)

Twenty-two address bits are required to decode 1 of 4194304 storage cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The eleven column-address bits are set up on A0 through A10 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. $\overline{W}$ can be driven from standard TTL circuits (TMS44100/P) or low-voltage TTL circuits (TMS46100/P) without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-write cycle, $\overline{CAS}$ is already low and the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{CAS}$) as long as t_{RAC} and t_{AA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to the high-impedance state. In a delayed-write or read-write cycle, the output follows the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every 16 ms (128 ms for TMS4x100P) to retain data. This can be achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed while maintaining valid data at the output. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden-refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 300-µA (TMS46100P) or 500-µA (TMS44100P) refresh current is available on the low-power devices. Data integrity is maintained using CBR refresh with a period of 125 µs while holding $\overline{RAS}$ low for less than 1 µs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self refresh

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 µs. The chip is then refreshed by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This ensures the DRAM is fully refreshed.

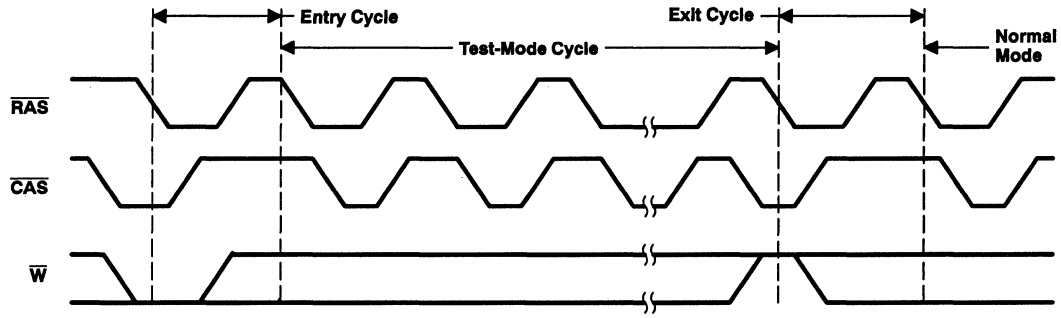
power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

test mode

An industry-standard design-for-test (DFT) mode is incorporated in the TMS4x100 and TMS4x100P. A CBR cycle with $\overline{W}$ low (WCBR) cycle is used to enter the test mode. In the test mode, data is written into and read from eight sections of the array in parallel. Data is compared upon reading and if all bits are equal, the data-out terminal goes high. If any one bit is different, the data-out terminal goes low. Any combination of read, write, read-write, or page-mode cycles can be used in the test mode. The test-mode function reduces test times by enabling the 4-Mbit DRAM to be tested as if it were a 512K DRAM, where row address 10, column address 10, and column address 0 are not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

test mode (continued)



† The states of $\overline{W}$, data in, and address are defined by the type of cycle used during test mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}: TMS44100, TMS44100P ..... –1 V to 7 V
TMS46100, TMS46100P ..... –0.5 V to 4.6 V
Voltage range on any pin (see Note 1): TMS44100, TMS44100P ..... –1 V to 7 V
TMS46100, TMS46100P ..... –0.5 V to 4.6 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –55°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		TMS44100/P			TMS46100/P			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	3	3.3	3.6	V
V_{IH}	High-level input voltage	2.4		6.5	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	–0.3		0.8	V
T_A	Operating free-air temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'44100-60 '44100P-60		'44100-70 '44100P-70		'44100-80 '44100P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle			105		90		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)			2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)	'44100		1		1		1	mA
			'44100P		500		500		500	µA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 4)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			105		90		80	mA
I_{CC4}	Average page current (see Notes 3 and 5)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling			90		80		70	mA
I_{CC6}†	Self-refresh current (see Note 3)	$\overline{CAS}$ ≤ 0.2 V, $\overline{RAS}$ < 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			500		500		500	µA
I_{CC7}	Standby current, outputs enabled (see Note 3)	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled			5		5		5	mA
I_{CC10}†	Battery-backup current (with CBR)	t_{RC} = 125 µs, t_{RAS} ≤ 1 ms, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			500		500		500	µA

† For TMS44100P only

NOTES: 3. I_{CC} max is specified with no load connected.
4. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
5. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'46100-60 '46100P-60		'46100-70 '46100P-70		'46100-80 '46100P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA (LVTTL)		2.4		2.4		2.4		V
		I_{OH} = – 100 µA (LVCMOS)		V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA (LVTTL)			0.4		0.4		0.4	V
		I_{OL} = 100 µA (LVCMOS)			0.2		0.2		0.2	
I_I	Input current (leakage)	V_I = 0 V to 3.9 V, V_{CC} = 3.6 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 3.6 V, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	Minimum cycle, V_{CC} = 3.6 V			70		60		50	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.0 V (LVTTL)			2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (LVCMOS)	'46100		300		300		300	µA
			'46100P		200		200		200	µA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 4)	Minimum cycle, V_{CC} = 3.6 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			70		60		50	mA
I_{CC4}	Average page current (see Notes 3 and 5)	t_{PC} = minimum, V_{CC} = 3.6 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling			60		50		40	mA
I_{CC6}†	Self-refresh current (see Note 3)	$\overline{CAS}$ ≤ 0.2 V, $\overline{RAS}$ < 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			200		200		200	µA
I_{CC7}	Standby current, outputs enabled (see Note 3)	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled			5		5		5	mA
I_{CC10}†	Battery-backup current (with CBR)	t_{RC} = 125 µs, t_{RAS} ≤ 1 ms, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			300		300		300	µA

† For TMS46100P only

NOTES: 3. I_{CC} max is specified with no load connected.
4. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
5. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

	PARAMETER	MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A10		5	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance		7	pF

NOTE 6: V_{CC} = 5 V ± .5 V for the TMS44100 devices, V_{CC} = 3.3 V ± 0.3 V for the TMS46100 devices, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	'4x100-60 '4x100P-60		'4x100-70 '4x100P-70		'4x100-80 '4x100P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low impedance	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 7)	0	15	0	18	0	20	ns

NOTE 7: t_{OFF} is specified when the output is no longer driven.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4x100-60 '4x100P-60		'4x100-70 '4x100P-70		'4x100-80 '4x100P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 8)	110		130		150		ns
t_{RWC}	Cycle time, read-write (see Note 8)	130		153		175		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 8 and 9)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-write (see Note 8)	60		68		75		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 10)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 10)	60	10 000	70	10 000	80	10 000	ns
t_{RASS}	Pulse duration, $\overline{RAS}$ low, self refresh	100		100		100		µs
t_{CAS}	Pulse duration, $\overline{CAS}$ low, (see Note 11)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{RPS}	Precharge time after self refresh using $\overline{RAS}$	140		130		150		ns
t_{WP}	Pulse duration, write	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 12)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{WTS}	Setup time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{DH}	Hold time, data (see Note 12)	10		15		15		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 14)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 14)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low (early-write operation only)	10		15		15		ns
t_{WCR}	Hold time, $\overline{W}$ low after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{WHR}	Hold time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{WTH}	Hold time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)	30		35		40		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns

NOTES: 8. All cycle times assume t_T = 5 ns.
9. To assure t_{PC} min, t_{ASC} should be ≥ 5 ns.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

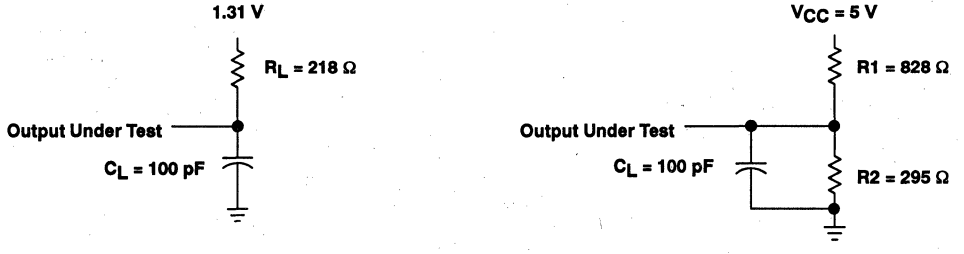
ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			'4x100-60 '4x100P-60		'4x100-70 '4x100P-70		'4x100-80 '4x100P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)		5		5		5		ns
t_{CHS}	Hold time, $\overline{CAS}$ low after $\overline{RAS}$ high, self refresh		−50		−50		−50		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-write operation only)		15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)		20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)		60		70		80		ns
t_{TAA}	Access time from address (test mode)		35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)		40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)		65		75		85		ns
t_{REF}	Refresh time interval	'4x100		16		16		16	ms
		'4x100P		128		128		128	ms
t_T	Transition time		2	50	2	50	2	50	ns

NOTE 15: The maximum value is specified only to assure access time.

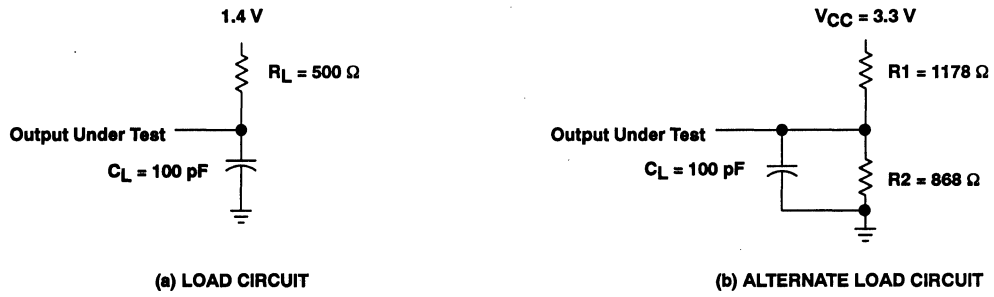
PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT (b) ALTERNATE LOAD CIRCUIT

Figure 1. Load Circuits for Timing Parameters

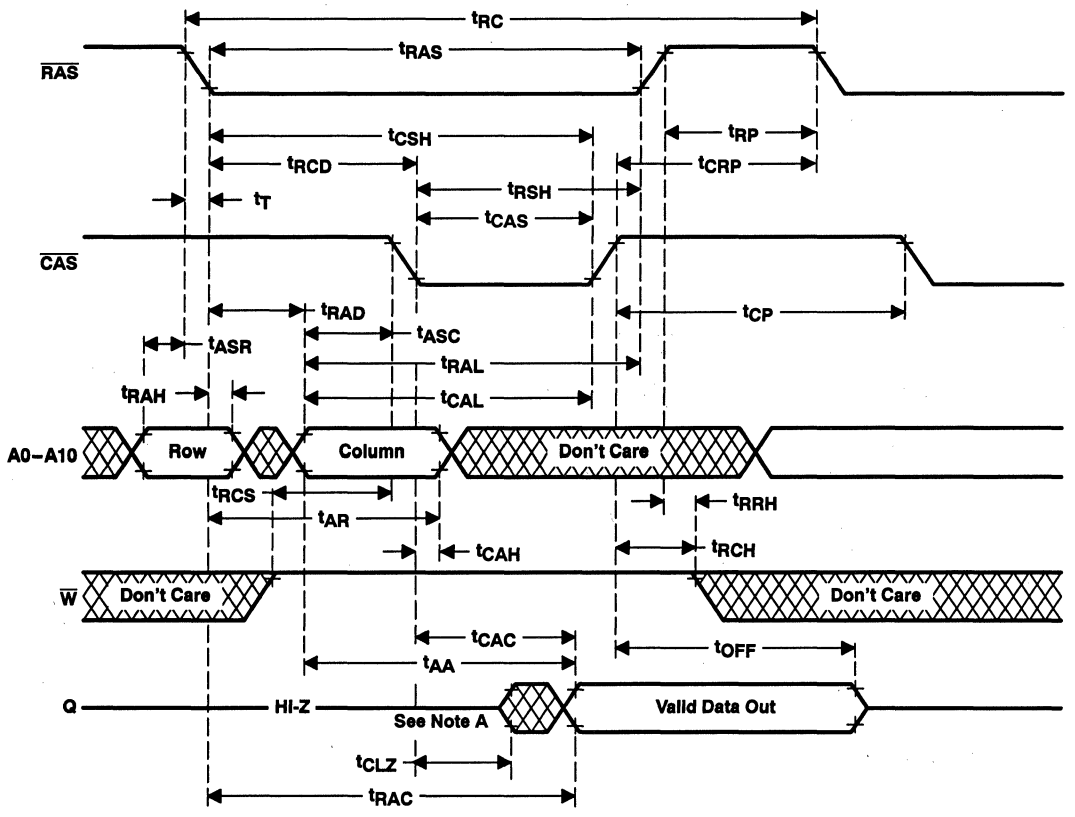
PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

Figure 2. Low-Voltage Load Circuits for Timing Parameters



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 3. Read-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

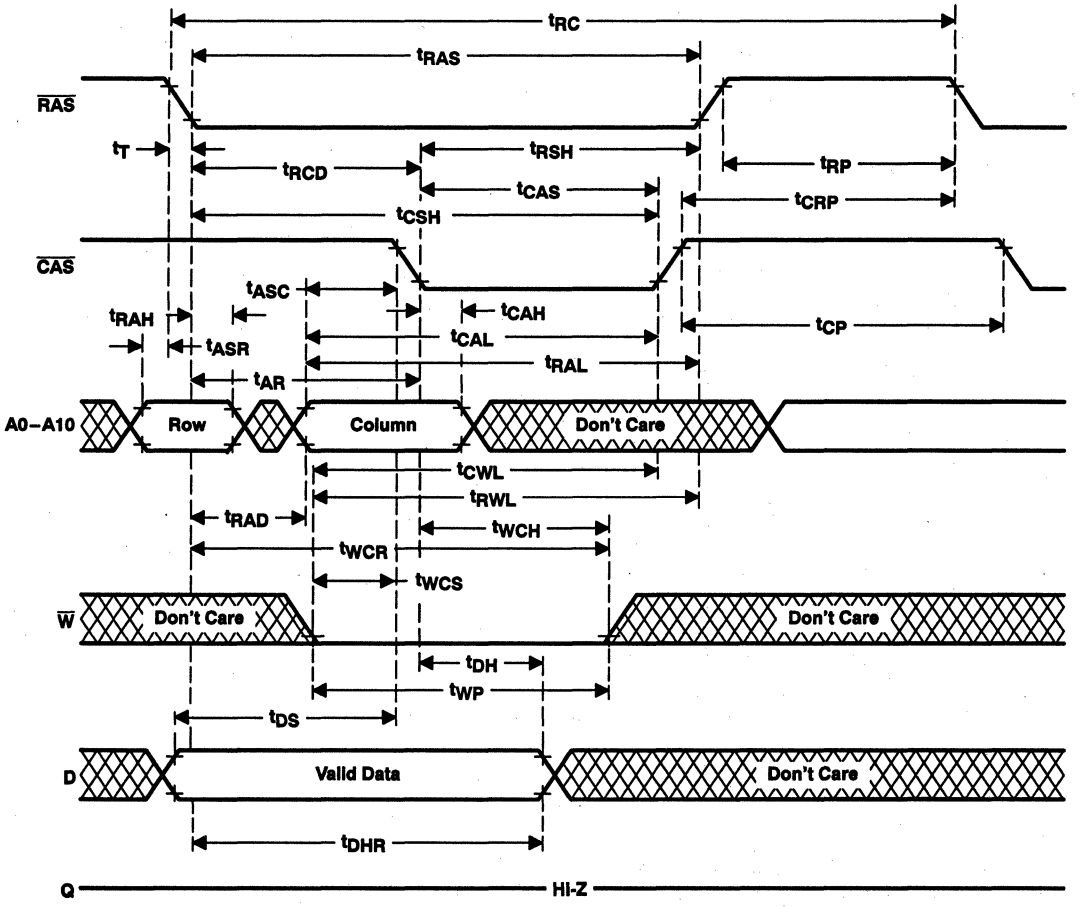


Figure 4. Early-Write-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

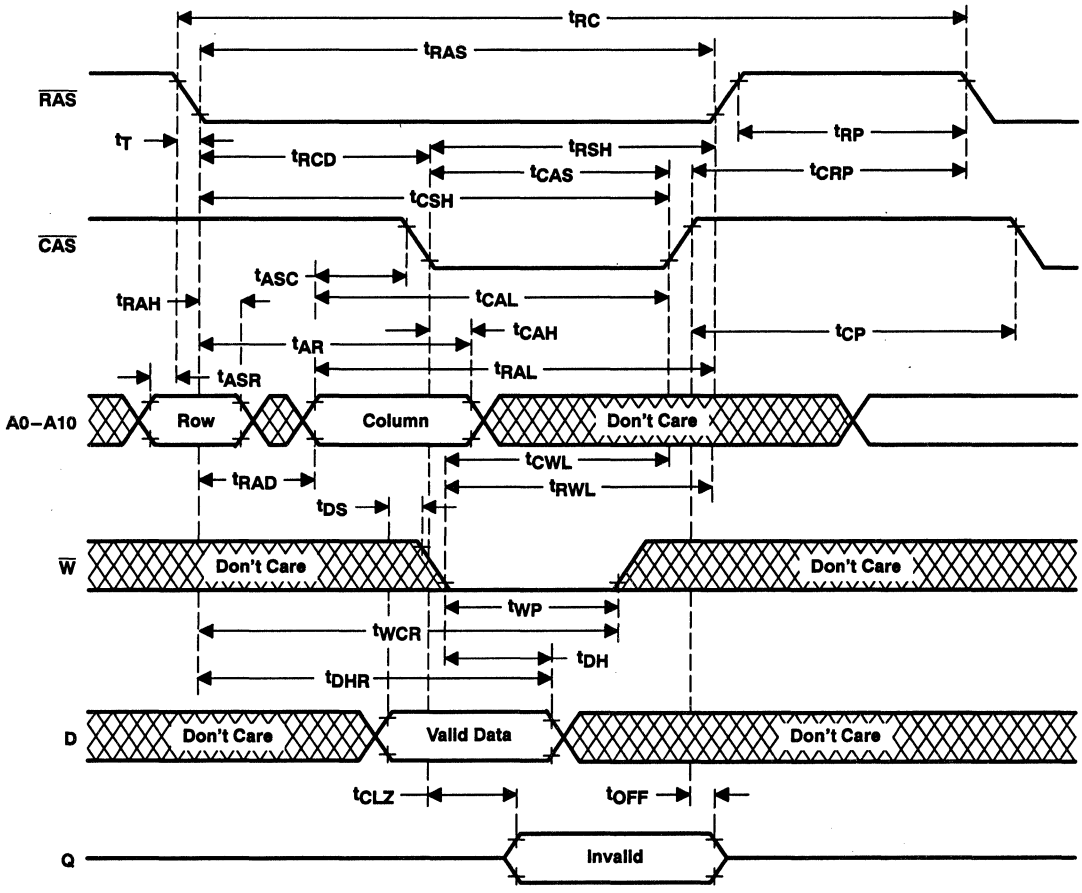
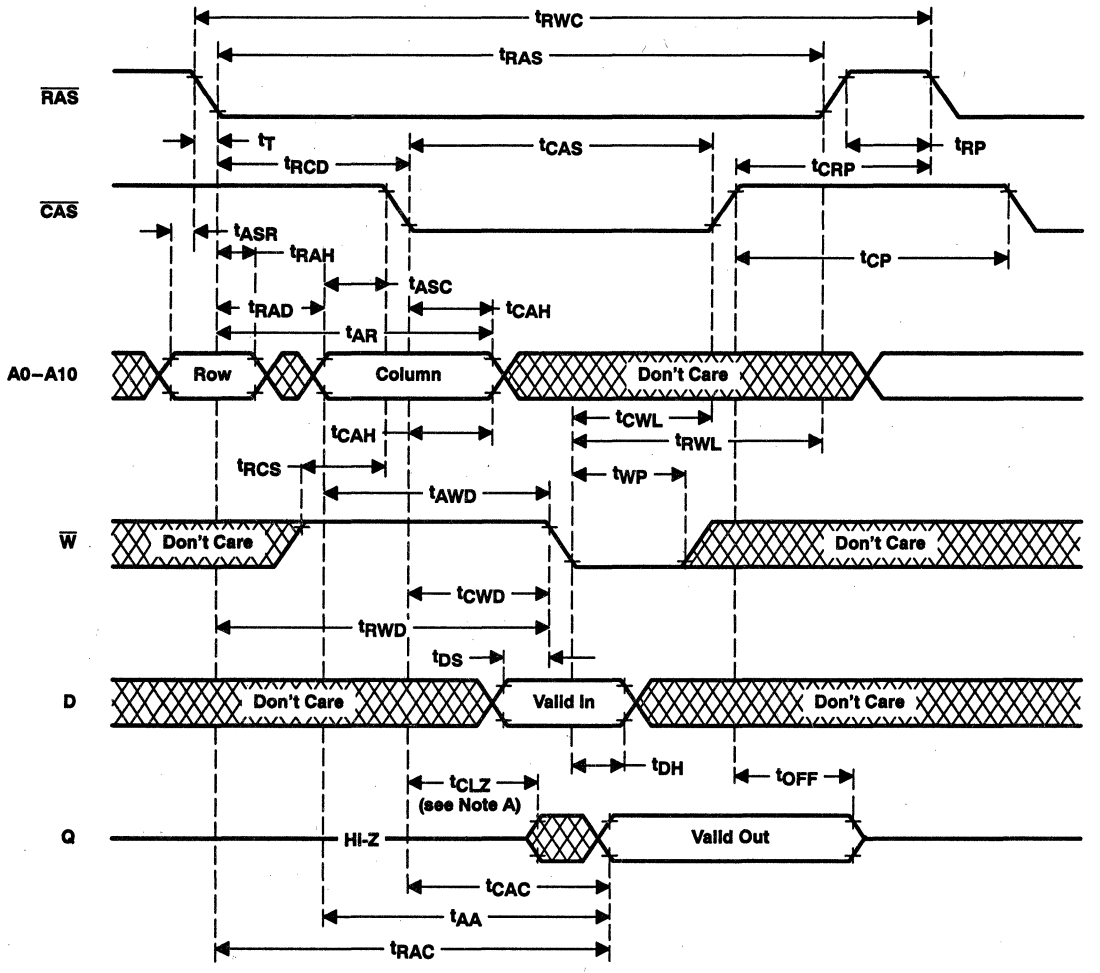


Figure 5. Write-Cycle Timing

ADVANCE INFORMATION

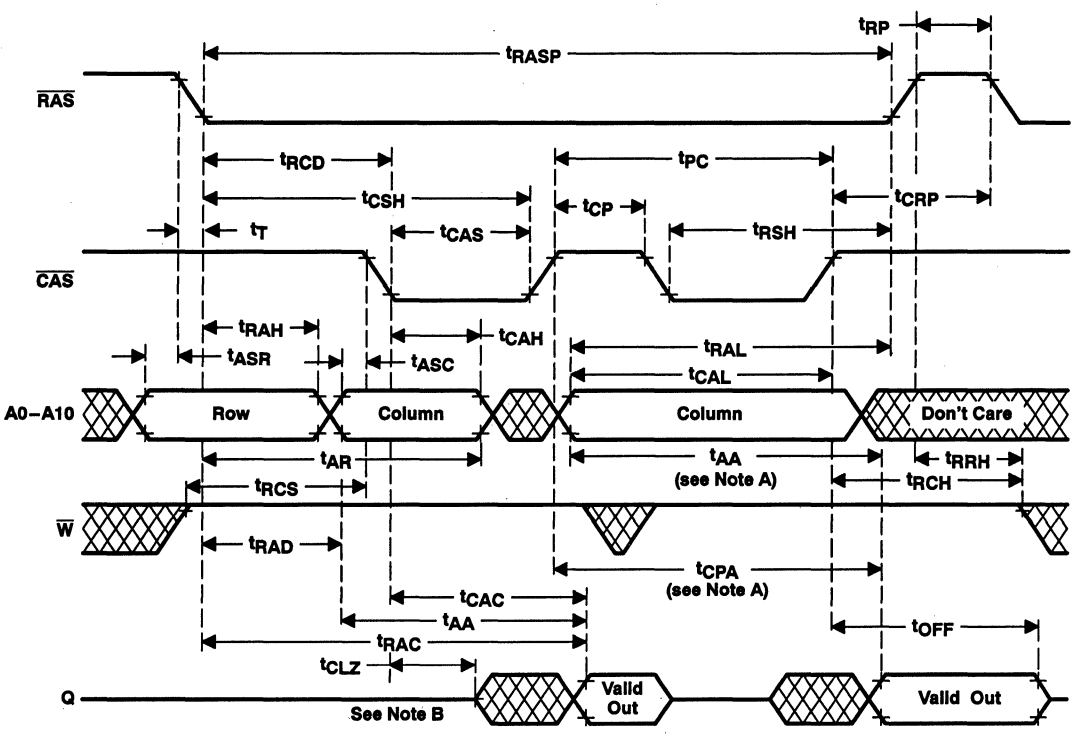
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

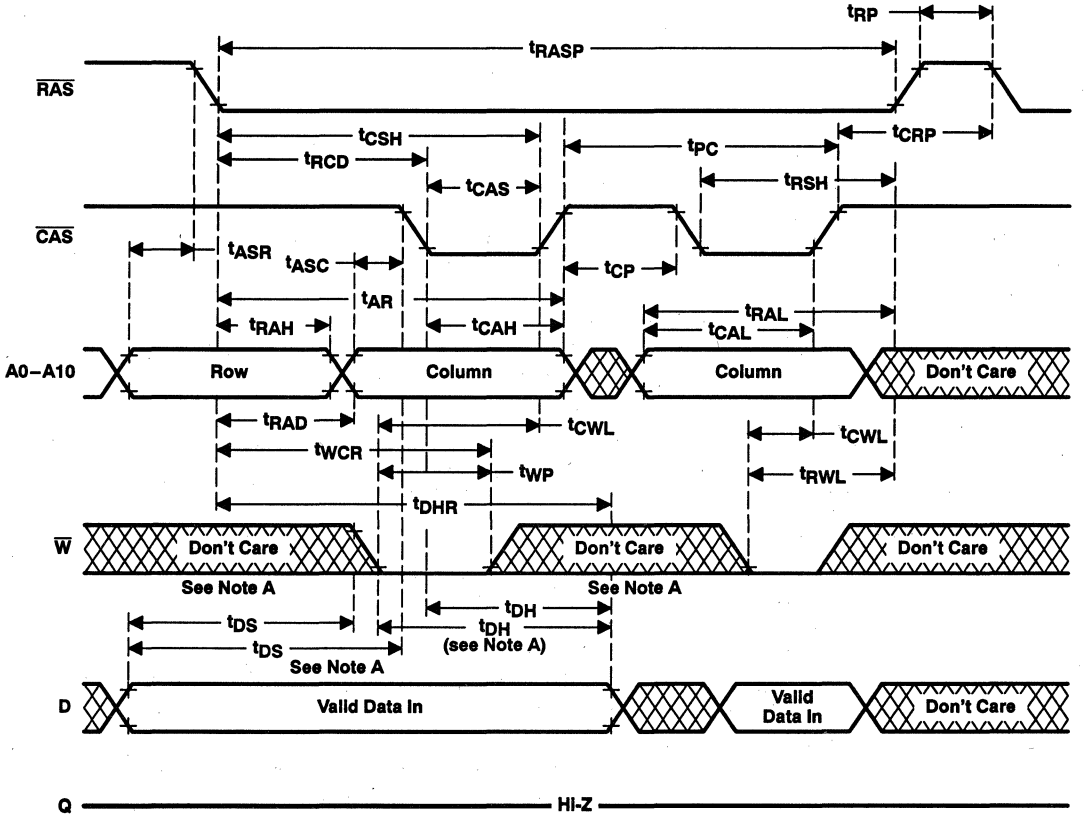


NOTES: A. Access time is t_{CPA} or t_{AA} dependent.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 7. Enhanced-Page-Mode Read-Cycle Timing

ADVANCE INFORMATION

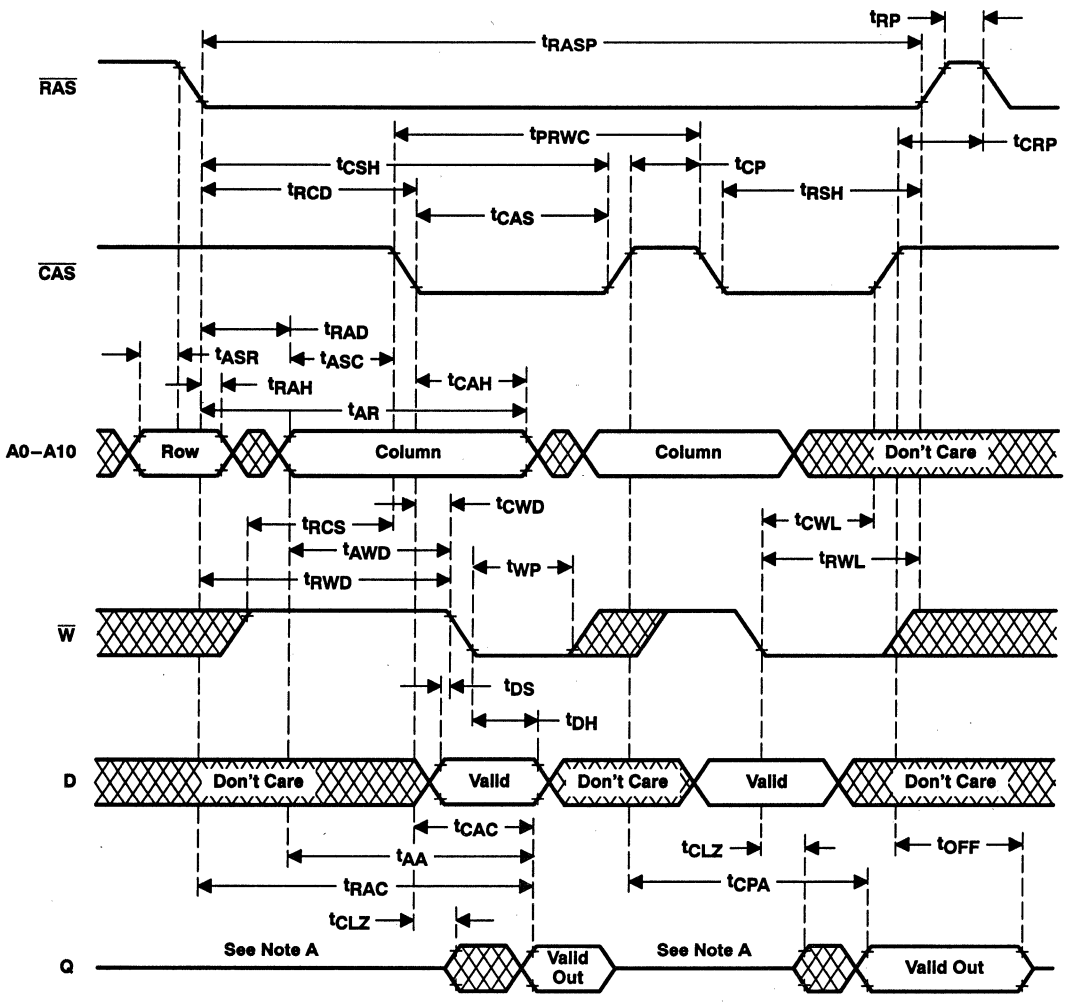
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

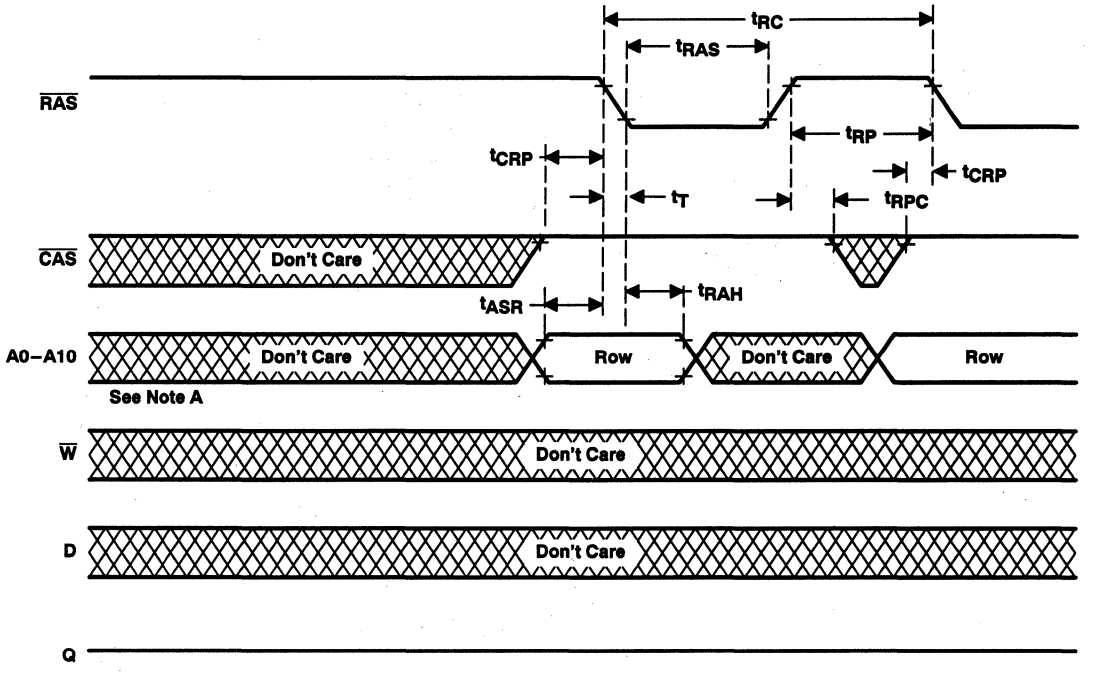


NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced-Page-Mode Read-Write-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTE A: A10 is a don't care.

Figure 10. $\overline{RAS}$-Only Refresh-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

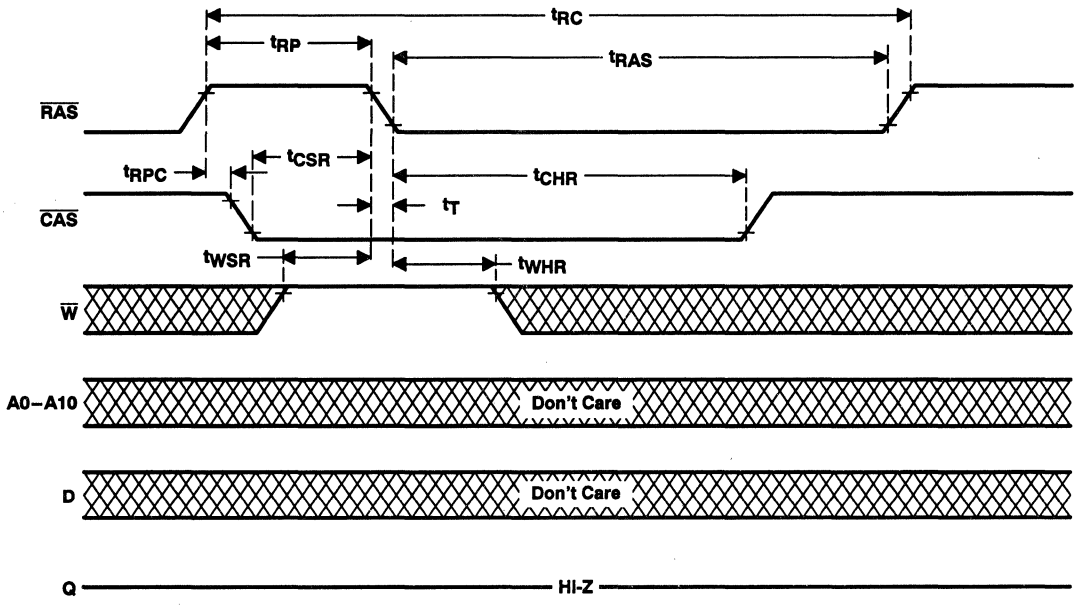


Figure 11. Automatic CBR-Refresh-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

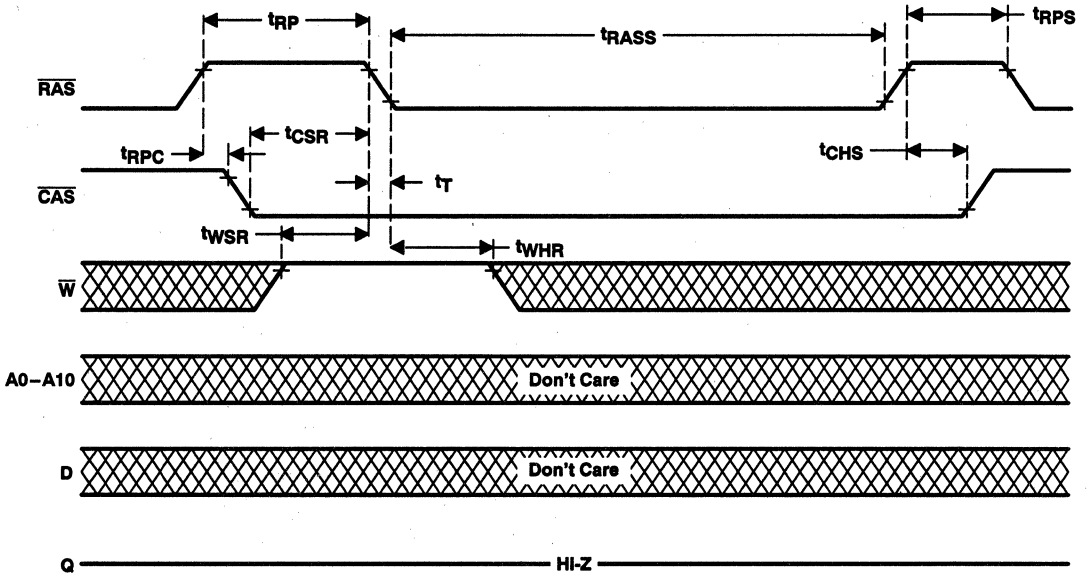


Figure 12. Self-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

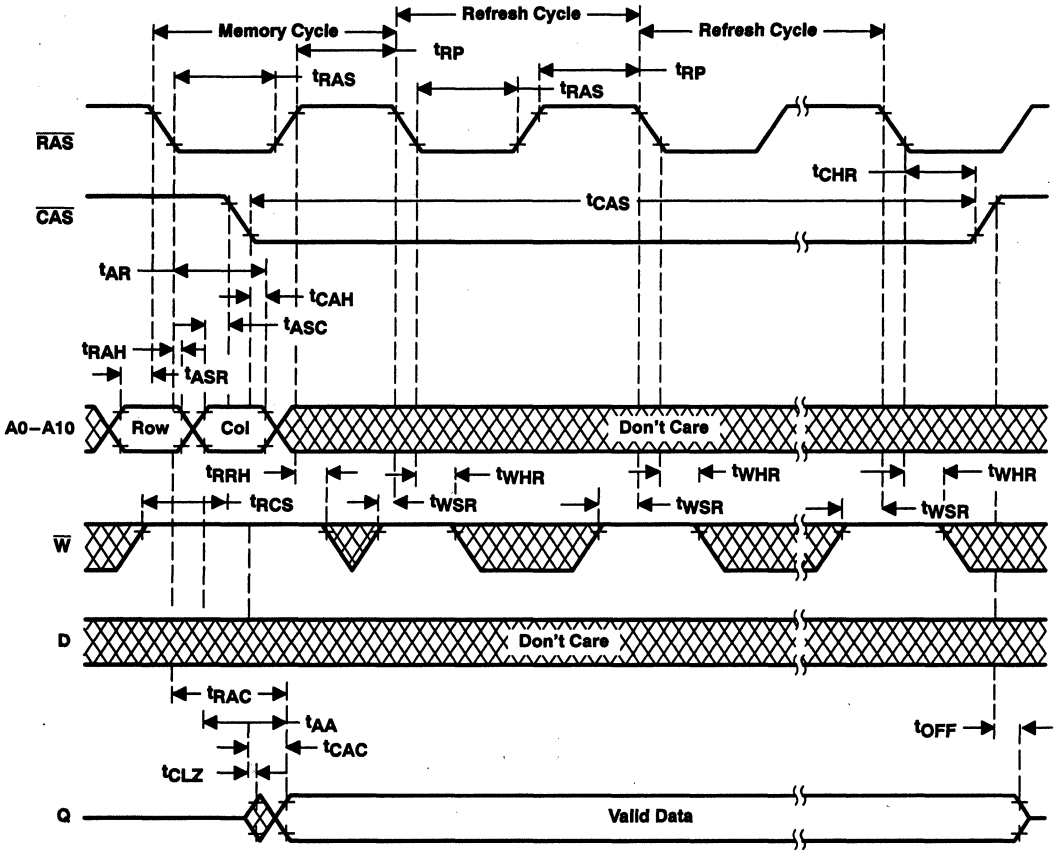


Figure 13. Hidden-Refresh-Cycle (Read) Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

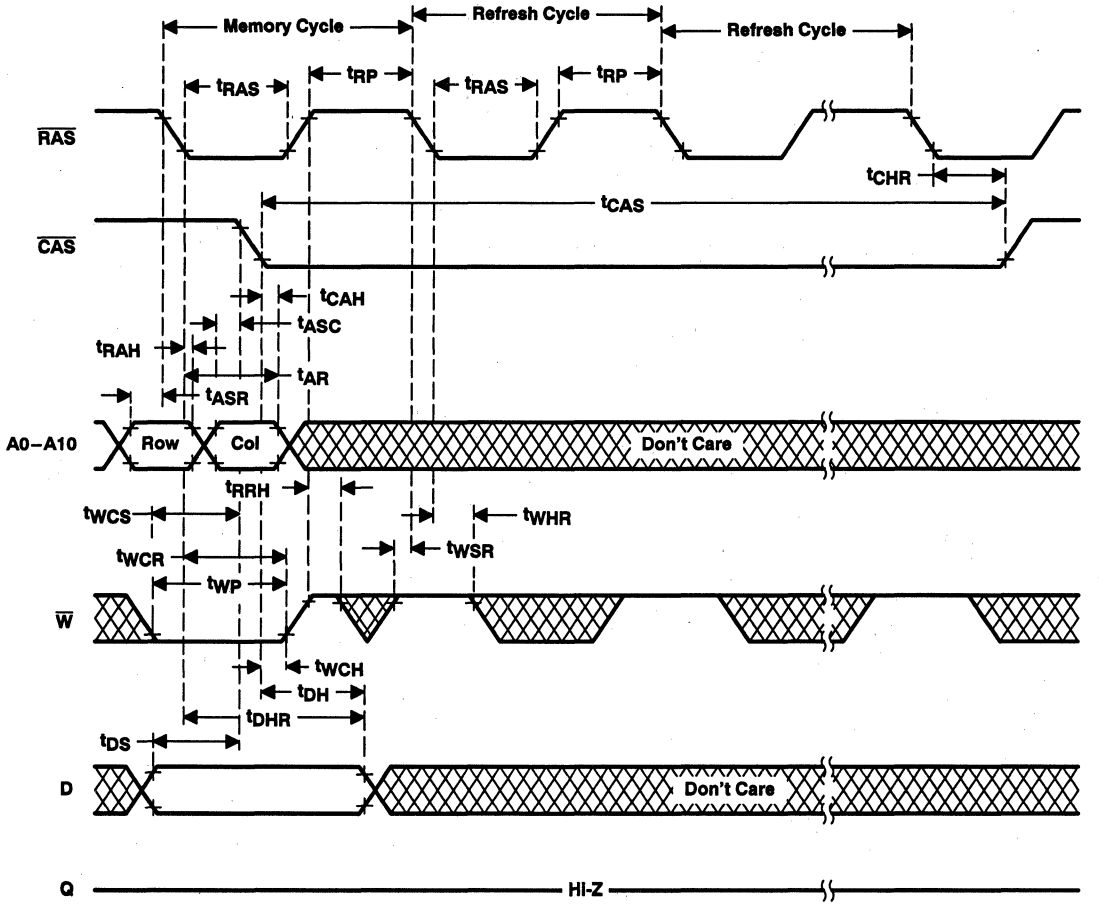


Figure 14. Hidden-Refresh-Cycle (Write) Timing

PARAMETER MEASUREMENT INFORMATION

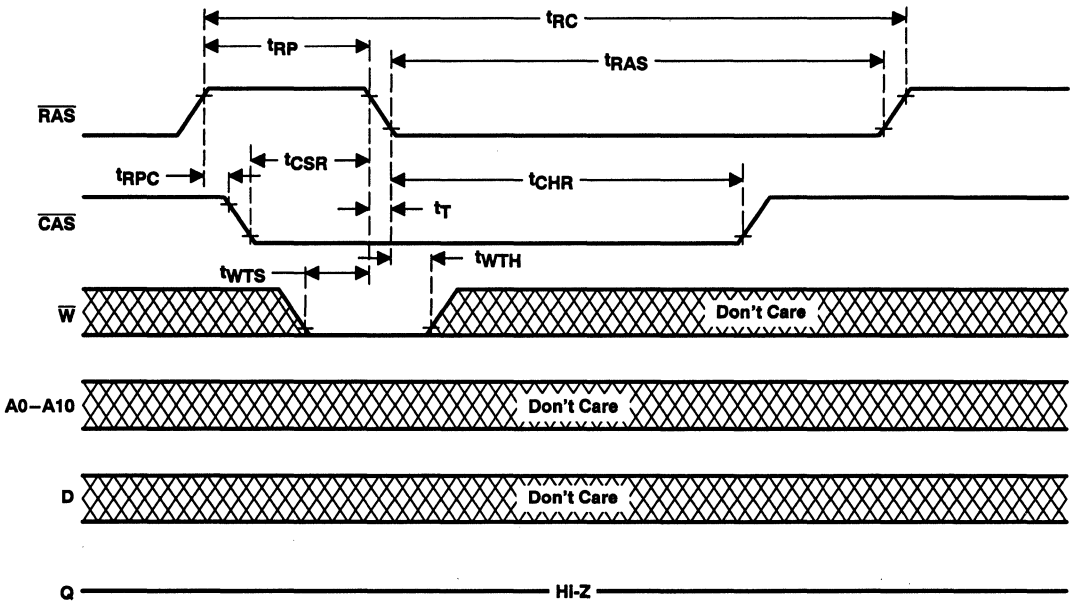
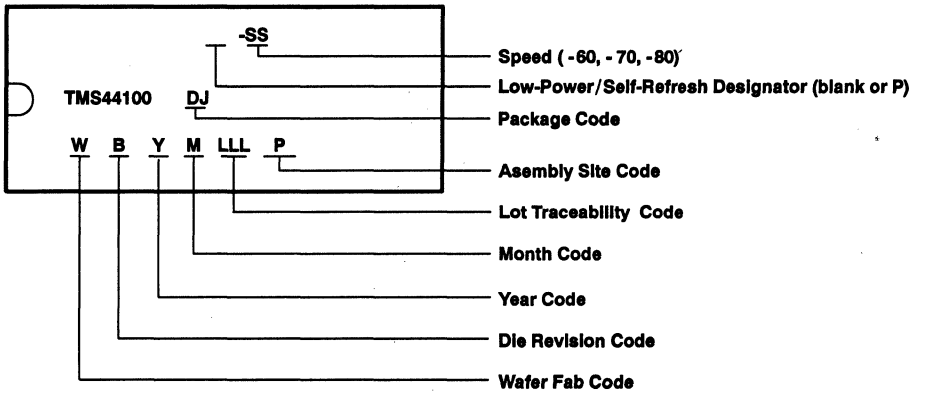


Figure 15. Test-Mode Entry Cycle

device symbolization (TMS44100 illustrated)



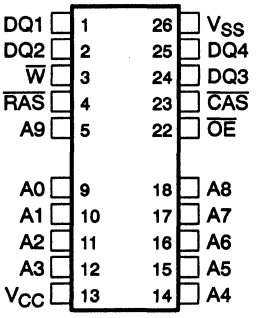
ADVANCE INFORMATION

- **Organization . . . 1048576 × 4**
- **Single 5-V Power Supply for TMS44400/P (±10% Tolerance)**
- **Single 3.3-V Power Supply for TMS46400/P (±10% Tolerance)**
- **Low Power Dissipation (TMS46400P only)**
  - **200-μA CMOS Standby**
  - **200-μA Self Refresh**
  - **300-μA Extended-Refresh Battery Backup**
- **Performance Ranges:**

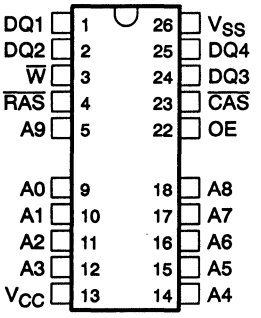
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
'4x400/P-60	60 ns	15 ns	30 ns	110 ns
'4x400/P-70	70 ns	18 ns	35 ns	130 ns
'4x400/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page-Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  1024-Cycle Refresh In 16 ms
  128 ms (Max) for Low-Power, Self-Refresh Version (TMS4x400P)
- **3-State Unlatched Output**
- **Texas Instruments EPIC™ CMOS Process**
- **Operating Free-Air Temperature Range**
  0°C to 70°C

DGA PACKAGE
(TOP VIEW)



DJ PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V or 3.3-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4x400 series is a set of high-speed, 4194304-bit dynamic random-access memories (DRAMs), organized as 1048576 words of four bits each. The TMS4x400P series is a set of high-speed, low-power, self-refresh with extended-refresh, 4194304-bit DRAMs, organized as 1048576 words of four bits each. Both series employ state-of-the-art enhanced performance implanted CMOS (EPIC™) technology for high performance, reliability, and low power.

AVAILABLE OPTIONS

DEVICE	POWER SUPPLY	SELF-REFRESH BATTERY BACKUP	REFRESH CYCLES
TMS44400	5 V	—	1024 in 16 ms
TMS44400P	5 V	Yes	1024 in 128 ms
TMS46400	3.3 V	—	1024 in 16 ms
TMS46400P	3.3 V	Yes	1024 in 128 ms

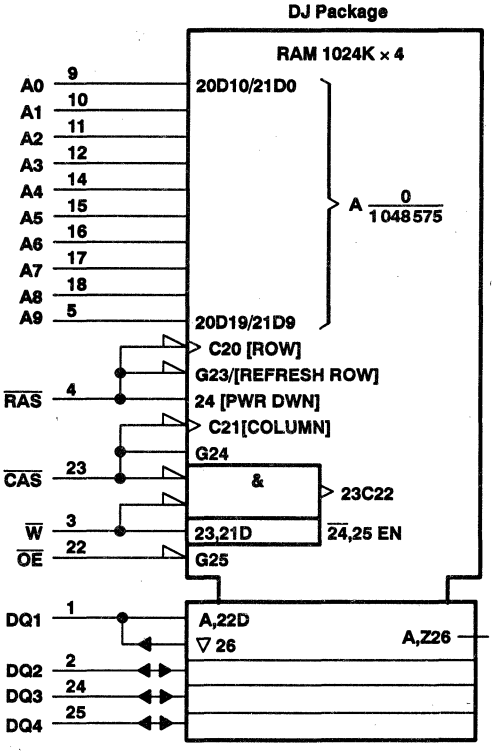
These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4x400 and TMS4x400P are offered in a 20/26-lead plastic small-outline (TSOP) package (DGA suffix) and a 300-mil 20/26-lead plastic surface-mount SOJ package (DJ suffix). Both packages are characterized for operation from 0°C to 70°C.

ADVANCE INFORMATION

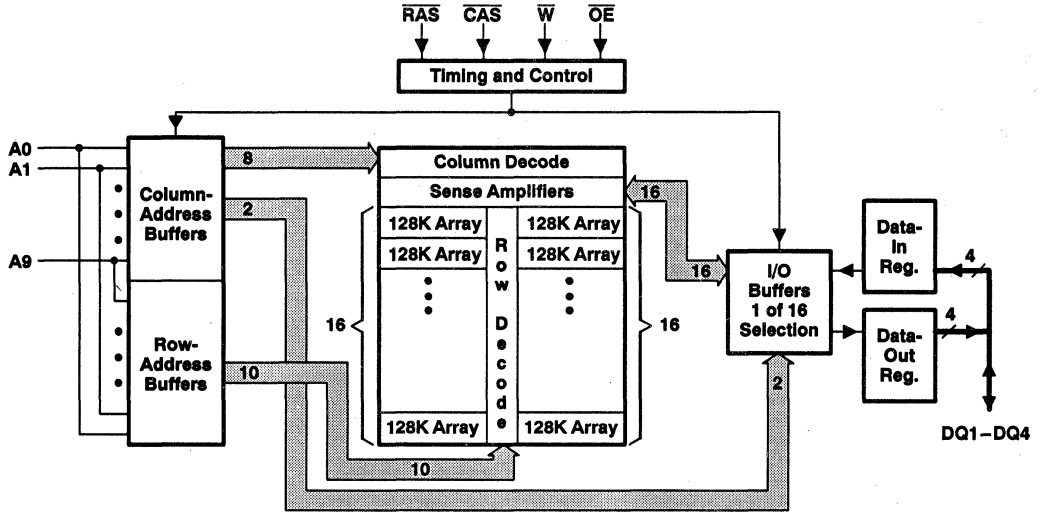
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device activate on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS4x400 to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} maximum (access time from $\overline{CAS}$ low) if t_{AA} maximum (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0–A9)

Twenty address bits are required to decode any one of the 1 048 576 storage-cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by $\overline{RAS}$. The ten column-address bits are set up on A0 through A9 and latched onto the chip by $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable because it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$ input. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. $\overline{W}$ can be driven from standard TTL circuits (TMS44400/P) or low voltage TTL circuits (TMS46400/P) without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation independent of the state of $\overline{OE}$. This permits early-write operation to complete with $\overline{OE}$ grounded.

data in/out (DQ1–DQ4)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns the output to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. They remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every 16 ms (128 ms for TMS4x400P) to retain data. This can be achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed while maintaining valid data at the output. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden-refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 300-µA (TMS46400P) or 500-µA (TMS44400P) refresh current is available on the low-power devices. Data integrity is maintained using CBR refresh with a period of 125 µs while holding $\overline{RAS}$ low for less than 1 µs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self refresh

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 µs. The chip is then refreshed by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must execute before continuing with normal operation. This ensures the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

test mode

The test mode is initiated with a CBR refresh cycle while simultaneously holding $\overline{W}$ low (WCBR). The entry cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in test mode, any desired data sequence can be performed on the device. The device exits test mode if a CBR refresh cycle with $\overline{W}$ held high or a $\overline{RAS}$-only refresh (ROR) cycle is performed.

The TMS4x400/P is configured as a 512K × 8 bit device in test mode, where each DQ pin has a separate 2-bit parallel read- and write-data bus. During a read cycle, the two internal bits are compared for each DQ pin separately. If the two bits agree, the DQ pin goes high; if not, the DQ pin goes low. The two bits are written to reflect the state of their respective DQ pins during a parallel write operation. Each DQ pin is independent of the others, and any data pattern desired can be written on each DQ pin. Test time is reduced by a factor of 4 for this series.

test mode (continued)

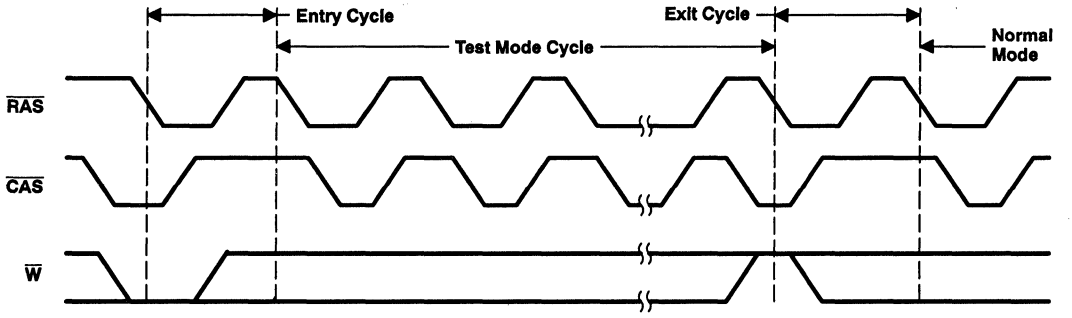


Figure 1. Test-Mode Cycle Timing†

† The states of $\overline{W}$, data in, and address are defined by the type of cycle used during test mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}: TMS44400, TMS44400P ..... –1.0 V to 7.0 V
TMS46400, TMS46400P ..... –0.5 V to 4.6 V
Voltage range on any pin (see Note 1) TMS44400, TMS44400P ..... –1.0 V to 7.0 V
TMS46400, TMS46400P ..... –0.5 V to 4.6 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –55°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		TMS44400/P			TMS46400/P			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	3	3.3	3.6	V
V_{IH}	High-level input voltage	2.4		6.5	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	–0.3		0.8	V
T_A	Operating free-air temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'44400-60 '44400P-60		'44400-70 '44400P-70		'44400-80 '44400P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle			105		90		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)			2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)	'44400		1		1		1	mA
			'44400P		500		500		500	µA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 4)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			105		90		80	mA
I_{CC4}	Average page current (see Notes 3 and 5)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling			90		80		70	mA
I_{CC6}†	Self-refresh current (see Note 3)	$\overline{CAS}$ ≤ 0.2 V, $\overline{RAS}$ < 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			500		500		500	µA
I_{CC7}	Standby current, outputs enabled (see Note 3)	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled			5		5		5	mA
I_{CC10}†	Battery-backup current (with CBR)	t_{RC} = 125 µs, t_{RAS} ≤ 1 ms, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			500		500		500	µA

† For TMS44400P only

NOTES: 3. I_{CC} max is specified with no load connected.
4. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
5. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'46400-60 '46400P-60		'46400-70 '46400P-70		'46400-80 '46400P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –2 mA (LVTTL)		2.4		2.4		2.4		V
		I_{OH} = –100 µA (LVCMOS)		V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA (LVTTL)			0.4		0.4		0.4	V
		I_{OL} = 100 µA (LVCMOS)			0.2		0.2		0.2	
I_I	Input current (leakage)	V_I = 0 V to 3.9 V, V_{CC} = 3.6 V, All others = 0 V to V_{CC}			±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 3.6 V, $\overline{CAS}$ high			±10		±10		±10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	Minimum cycle, V_{CC} = 3.6 V			70		60		50	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2 V (LVTTL)			2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (LVCMOS)	'46400		300		300		300	µA
			'46400P		200		200		200	µA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 4)	Minimum cycle, V_{CC} = 3.6 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			70		60		50	mA
I_{CC4}	Average page current (see Notes 3 and 5)	t_{PC} = minimum, V_{CC} = 3.6 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling			60		50		40	mA
I_{CC6}†	Self-refresh current (see Note 3)	$\overline{CAS}$ ≤ 0.2 V, $\overline{RAS}$ < 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			200		200		200	µA
I_{CC7}	Standby current, outputs enabled (see Note 3)	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled			5		5		5	mA
I_{CC10}†	Battery-backup current (with CBR)	t_{RC} = 125 µs, t_{RAS} ≤ 1 ms, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			300		300		300	µA

† For TMS46400P only

NOTES: 3. I_{CC} max is specified with no load connected.
4. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
5. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

	PARAMETER	MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A10		5	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance		7	pF

NOTE 6: V_{CC} = 5 V ± .5 V for the TMS44400 devices, V_{CC} = 3.3 V ± 0.3 V for the TMS46400 devices, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	'4x400-60 '4x400P-60		'4x400-70 '4x400P-70		'4x400-80 '4x400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20	ns
t_{CLZ}	$\overline{CAS}$ to output in low impedance	0		0		0		ns
t_{OFF}	Output-disable time after $\overline{CAS}$ high (see Note 7)	0	15	0	18	0	20	ns
t_{OEZ}	Output-disable time after $\overline{OE}$ high (see Note 7)	0	15	0	18	0	20	ns

NOTE 7: t_{OFF} is specified when the output is no longer driven.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4x400-60 '4x400P-60		'4x400-70 '4x400P-70		'4x6400-80 '4x400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 8)	110		130		150		ns
t_{RWC}	Cycle time, read-write	155		181		205		ns
t_{PC}	Cycle time, page-mode read or write (see Note 9)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-write	85		96		105		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 10)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 10)	60	10 000	70	10 000	80	10 000	ns
t_{RASS}	Pulse duration, $\overline{RAS}$ low, self refresh	100		100		100		µs
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 11)	10	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{RPS}	Precharge time after self refresh using $\overline{RAS}$	110		130		150		ns
t_{WP}	Pulse duration, write	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 12)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high ($\overline{CBR}$ refresh only)	10		10		10		ns
t_{WTS}	Setup time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{DH}	Hold time, data (see Note 12)	10		15		15		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 14)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 14)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low (early-write operation only)	10		15		15		ns
t_{WCR}	Hold time, $\overline{W}$ low after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{WHR}	Hold time, $\overline{W}$ high ($\overline{CBR}$ refresh only)	10		10		10		ns
t_{WTH}	Hold time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{CHS}	Hold time, $\overline{CAS}$ low after $\overline{RAS}$ high (self refresh)	–50		–50		–50		ns
t_{OEH}	Hold time, $\overline{OE}$ command	15		18		20		ns
t_{OED}	Hold time, $\overline{OE}$ to data delay	15		18		20		ns

NOTES: 8. All cycle times assume t_T = 5 ns.
9. To ensure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

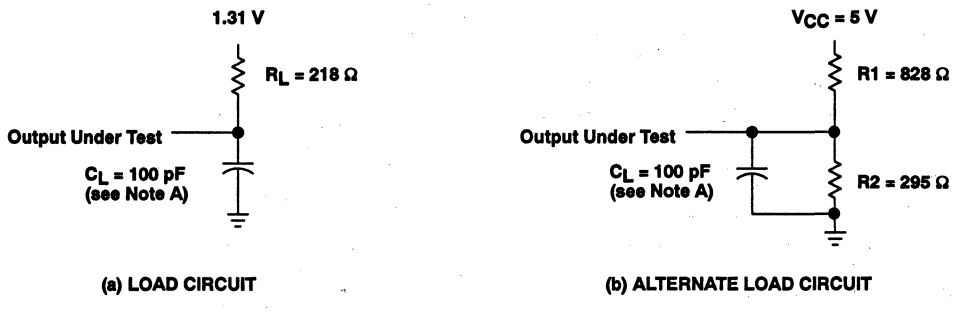
ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			'4x400-60 '4x400P-60		'4x400-70 '4x400P-70		'4x400-80 '4x400P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$		10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)		55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CBR}$ refresh only)		10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CBR}$ refresh only)		5		5		5		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-write operation only)		40		46		50		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)		20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)		85		98		110		ns
t_{TAA}	Access time from address (test mode)		35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)		40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)		65		75		85		ns
t_{REF}	Refresh time interval	'4x400		16		16		16	ms
		'4x400P		128		128		128	ms
t_T	Transition time		2	30	2	30	2	30	ns

NOTE 15: The maximum value is specified only to ensure access time.

PARAMETER MEASUREMENT INFORMATION



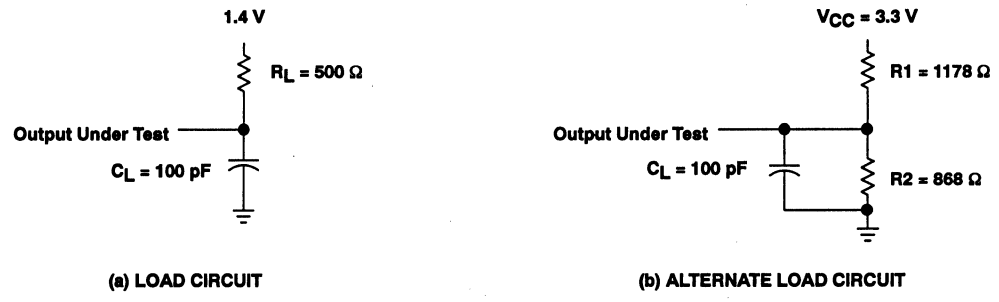
(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.

Figure 2. Load Circuits for Timing Parameters

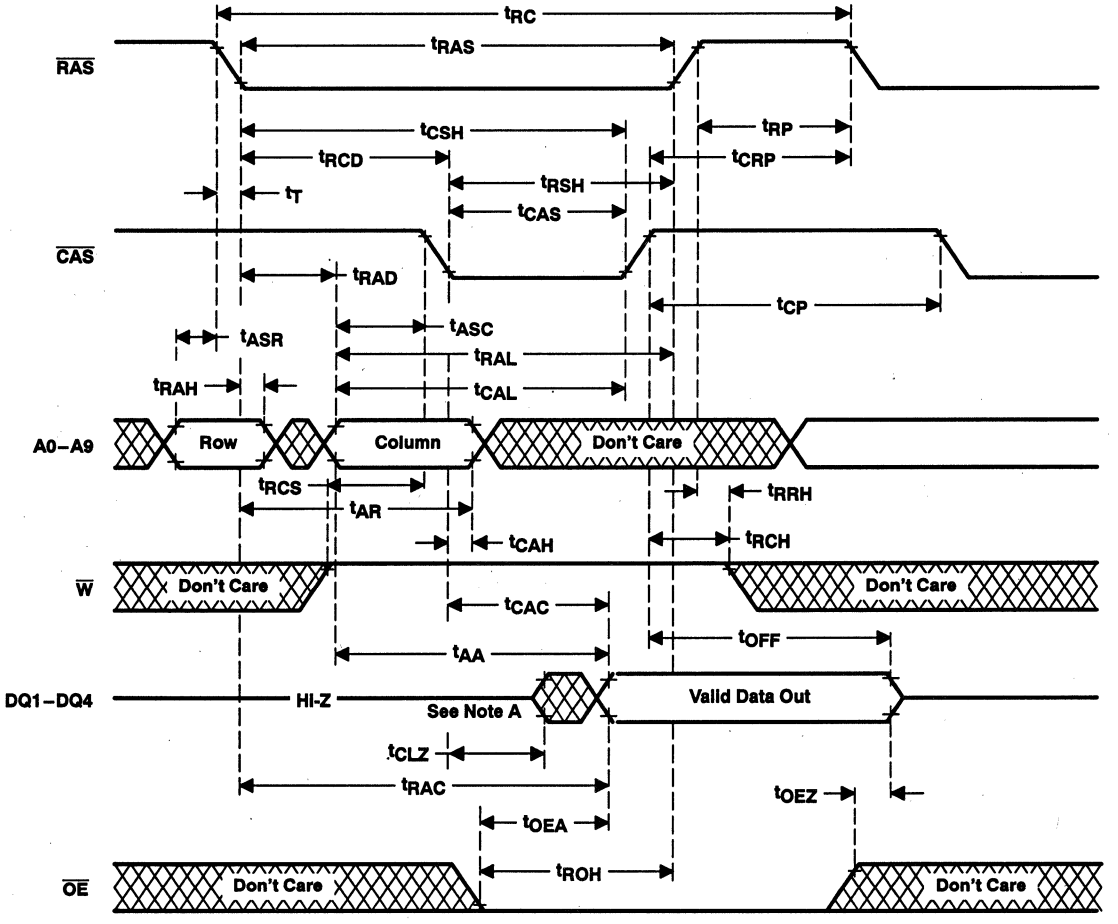
PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

Figure 3. Low-Voltage Load Circuits for Timing Parameters



NOTE B: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 4. Read-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

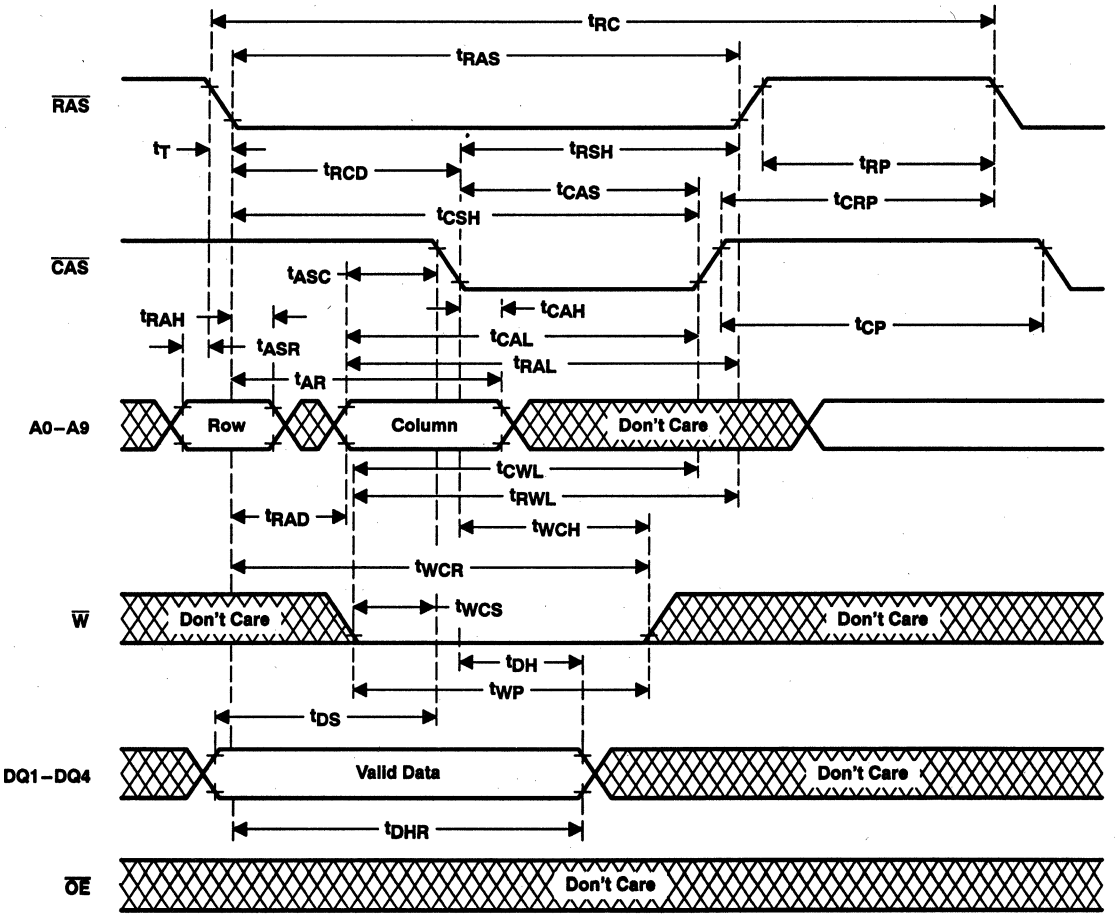


Figure 5. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

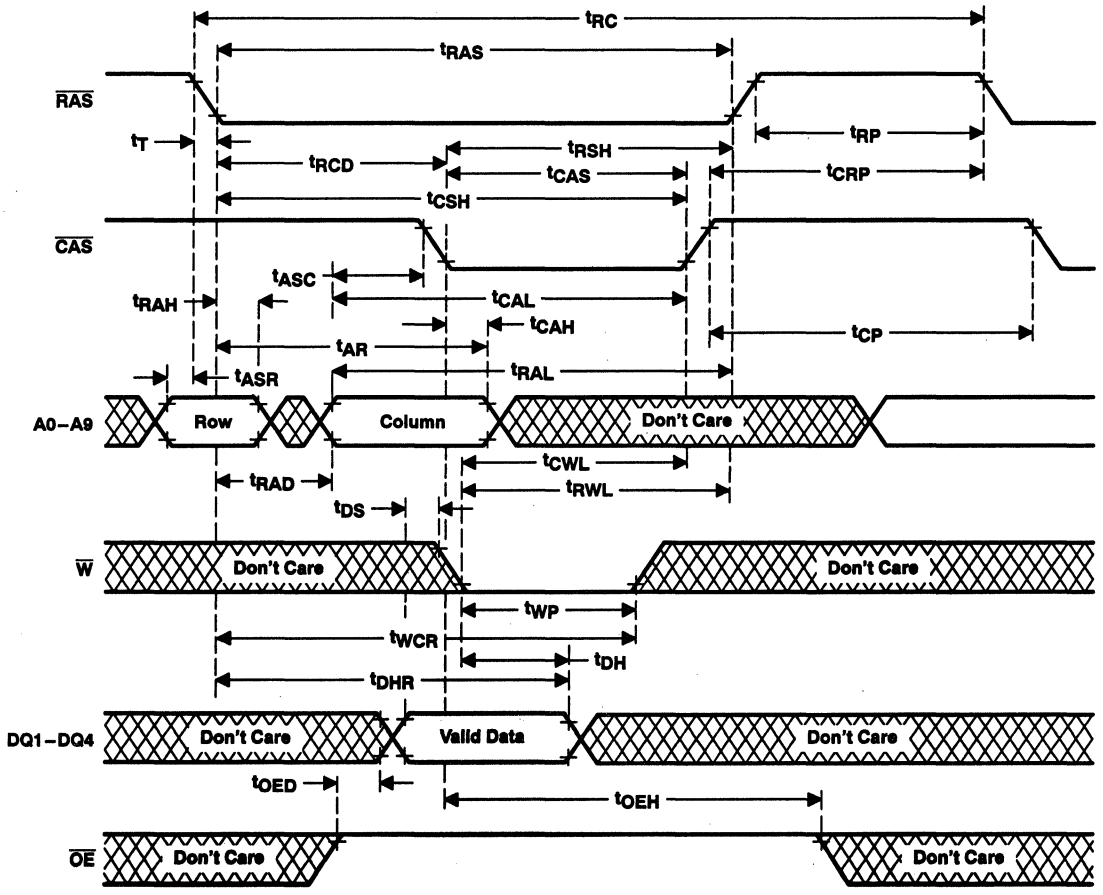
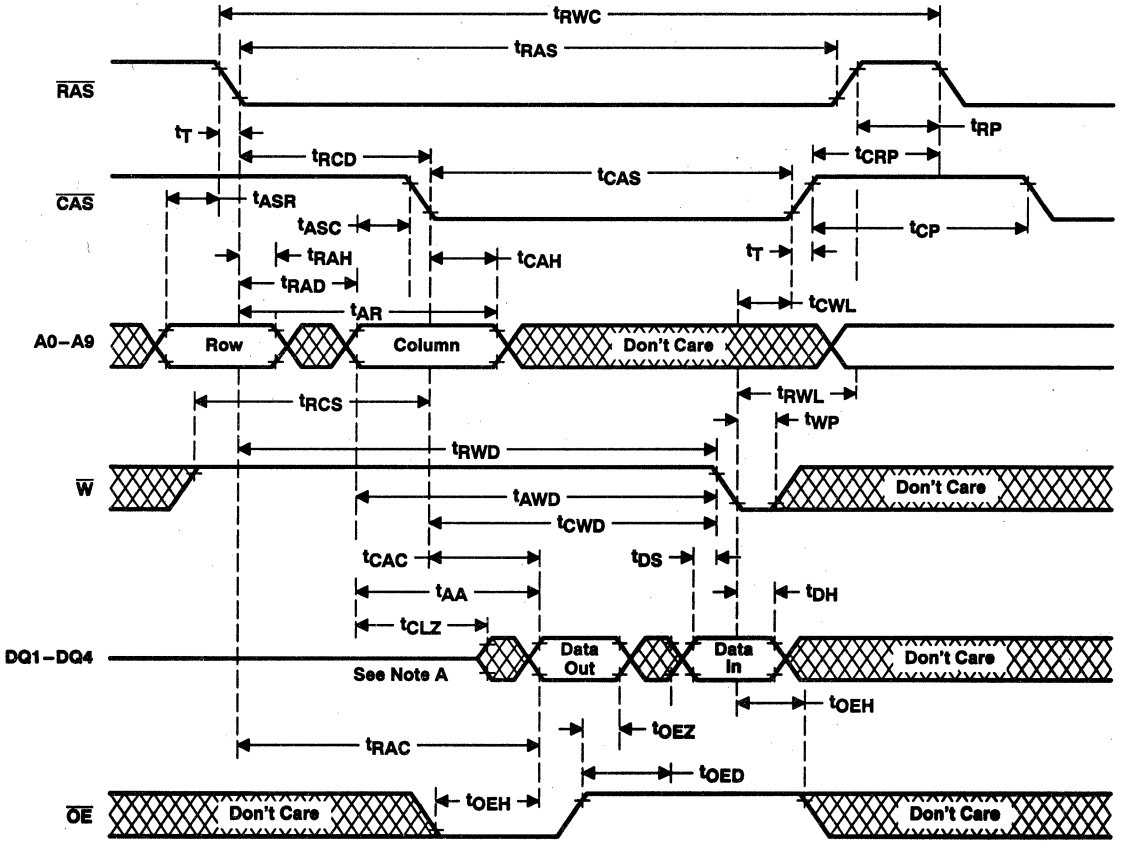


Figure 6. Write-Cycle Timing

ADVANCE INFORMATION

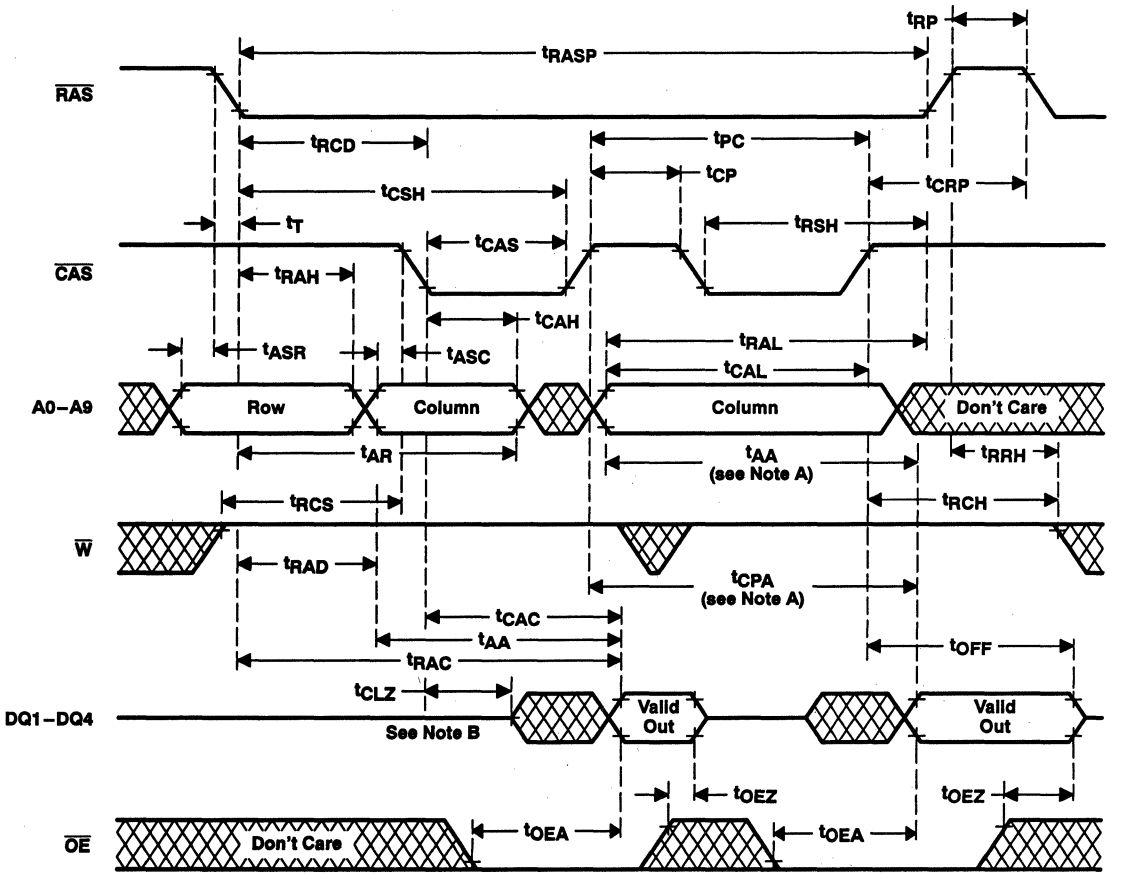
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 7. Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

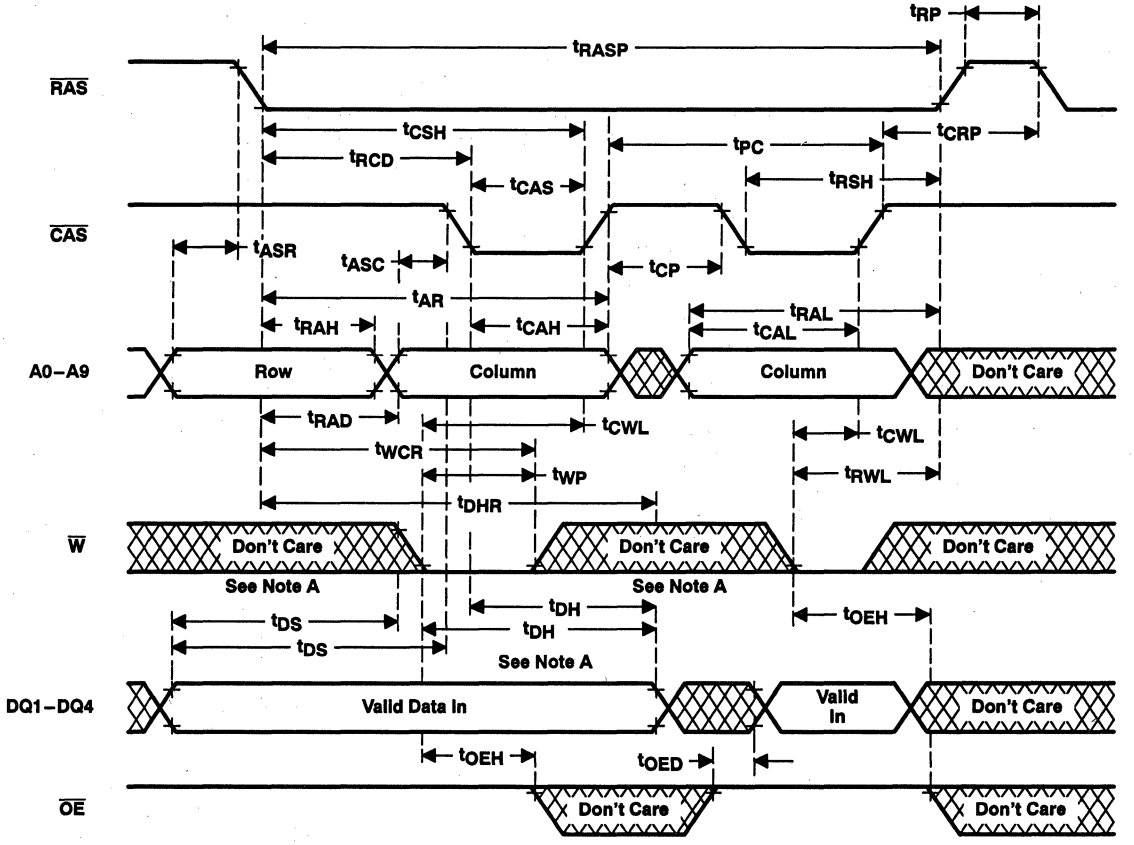


NOTES: A. Access time is t_{CPA} or t_{AA} dependent.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 8. Enhanced-Page-Mode Read-Cycle Timing

ADVANCE INFORMATION

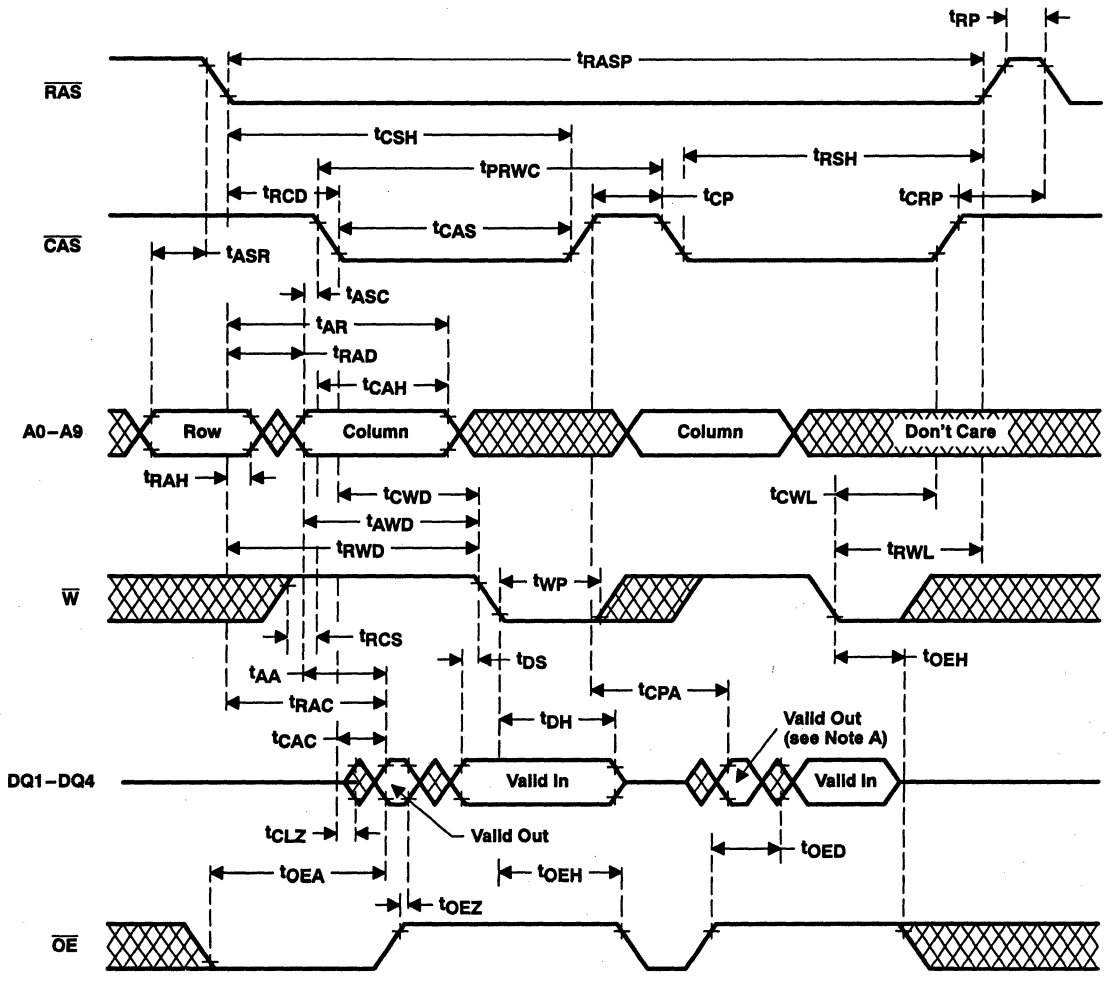
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 9. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 10. Enhanced-Page-Mode Read-Write-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

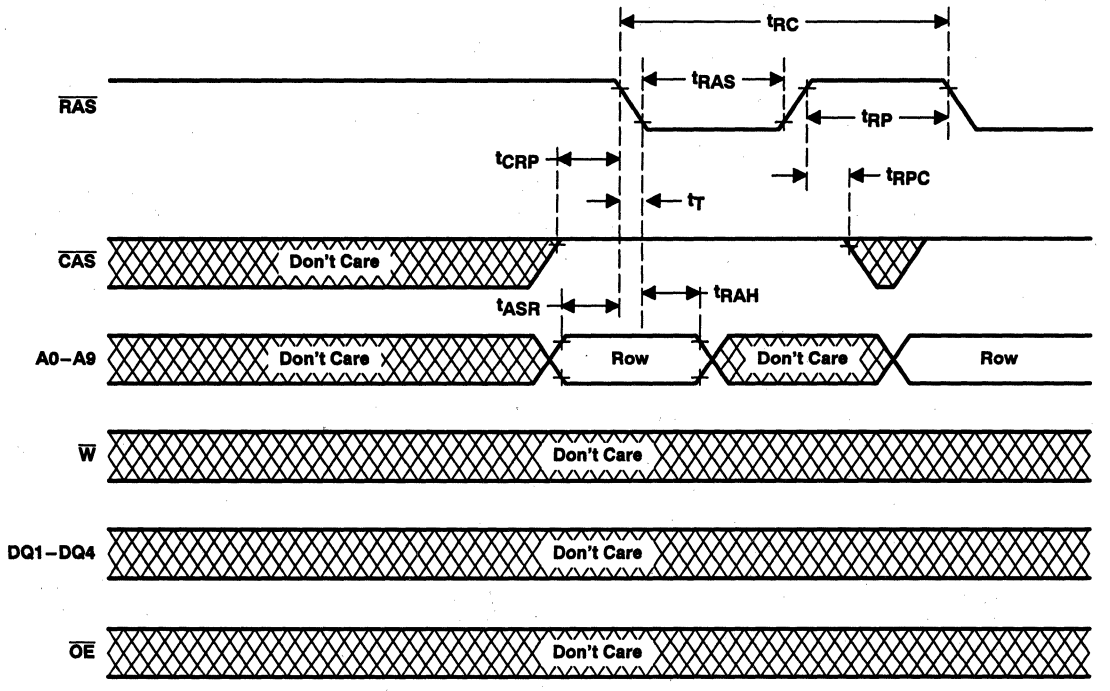


Figure 11. $\overline{RAS}$-Only Refresh-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

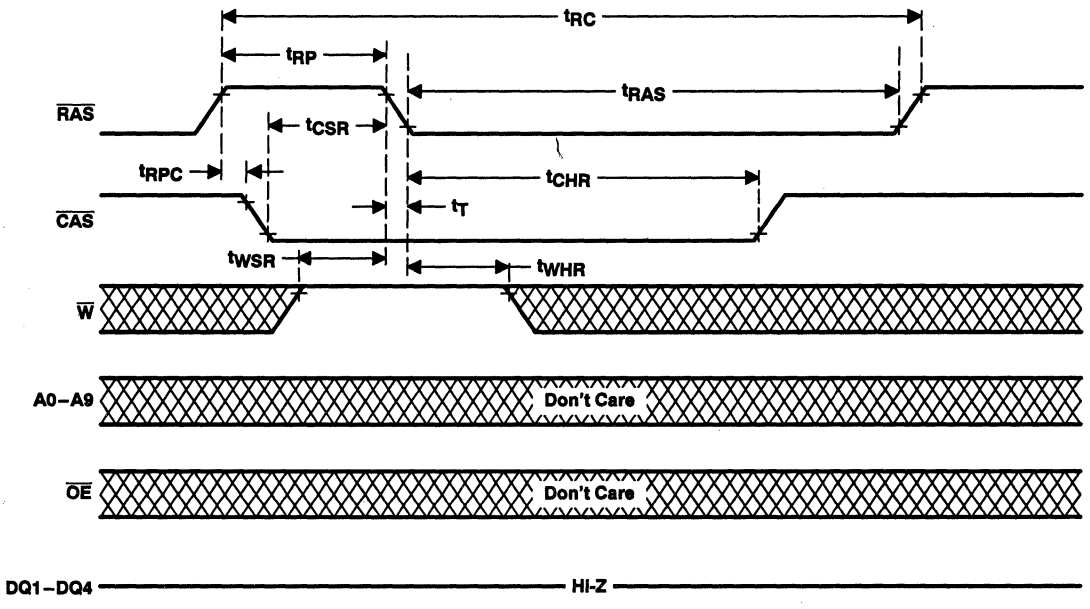


Figure 12. Automatic-CBR-Refresh-Cycle Timing

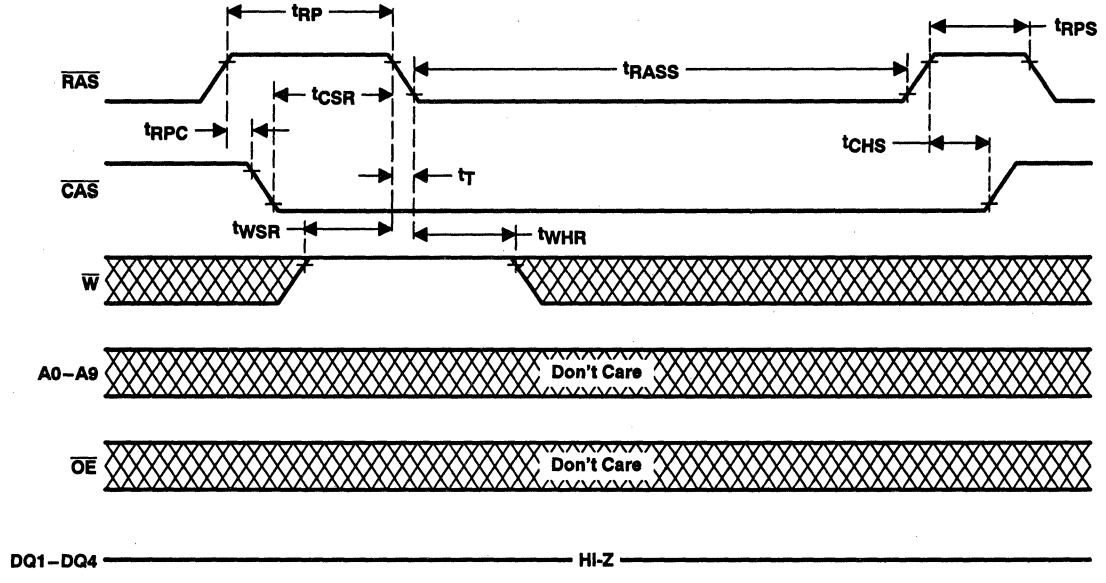


Figure 13. Self-Refresh-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

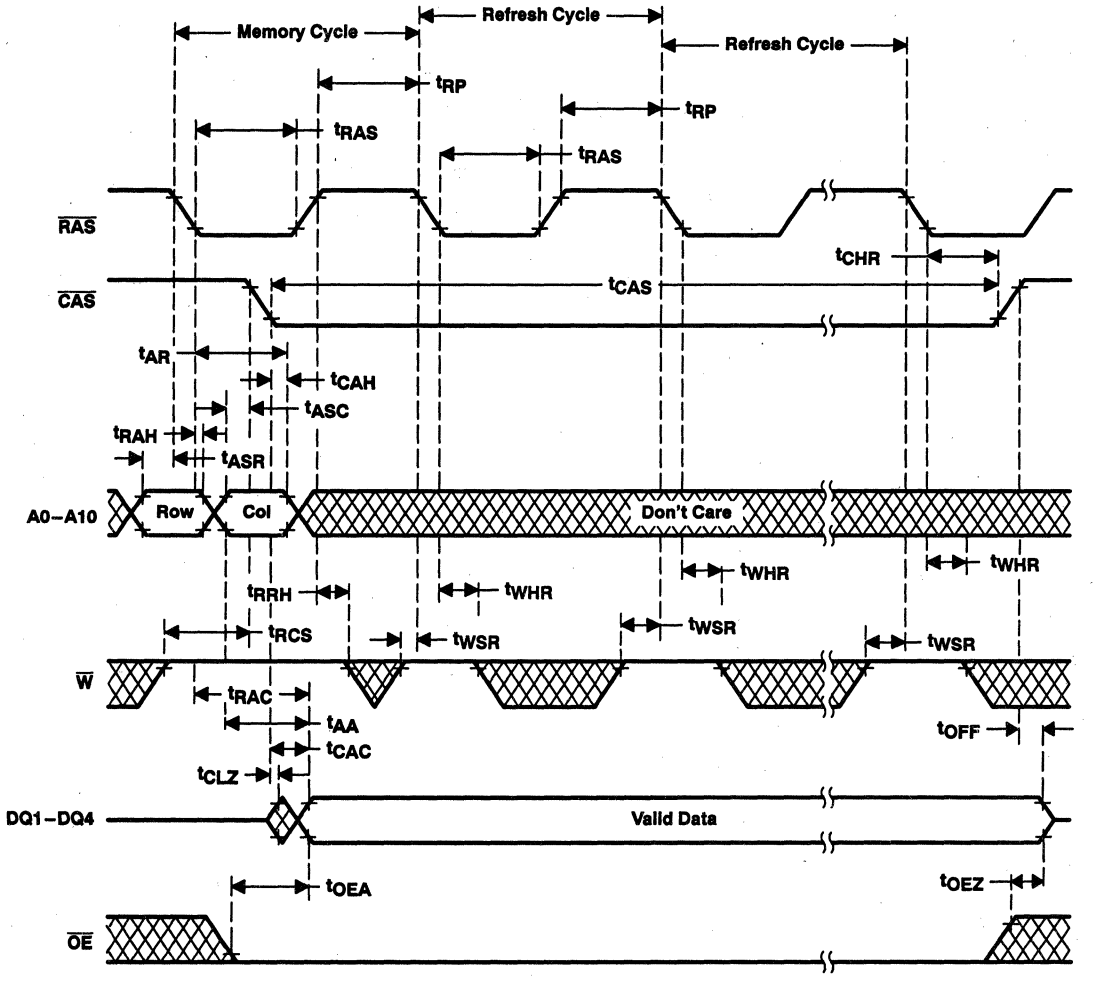


Figure 14. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

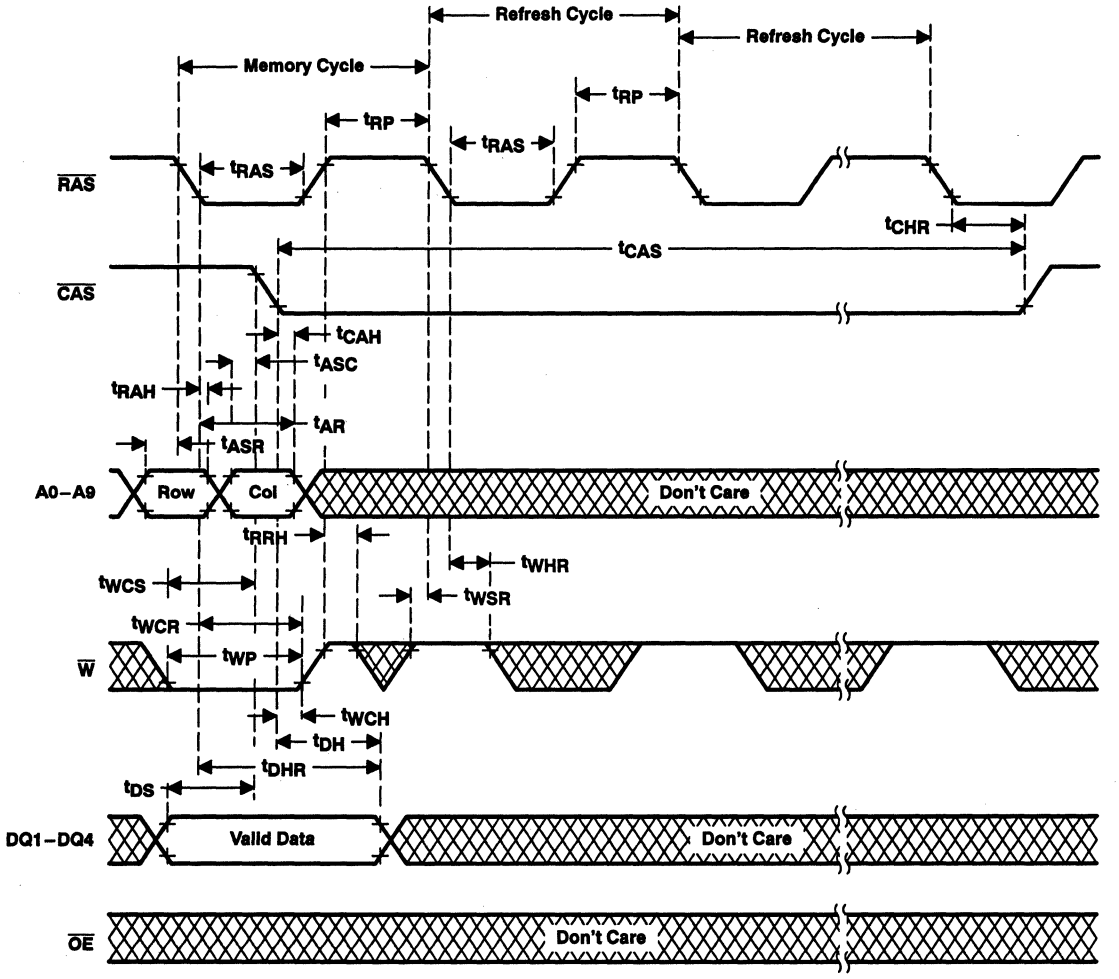


Figure 15. Hidden-Refresh-Cycle (Write) Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

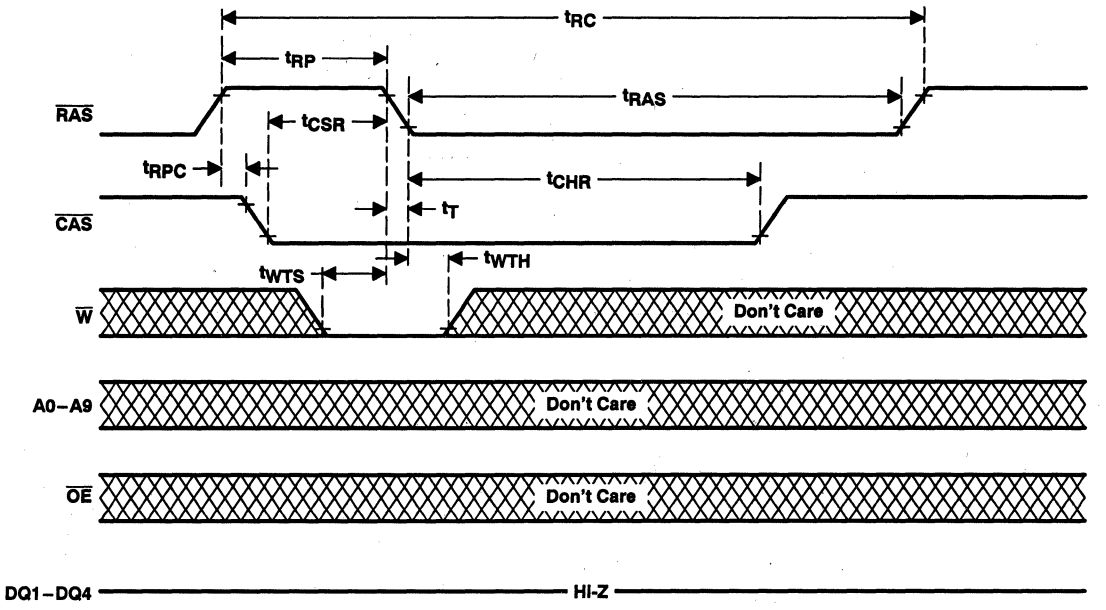
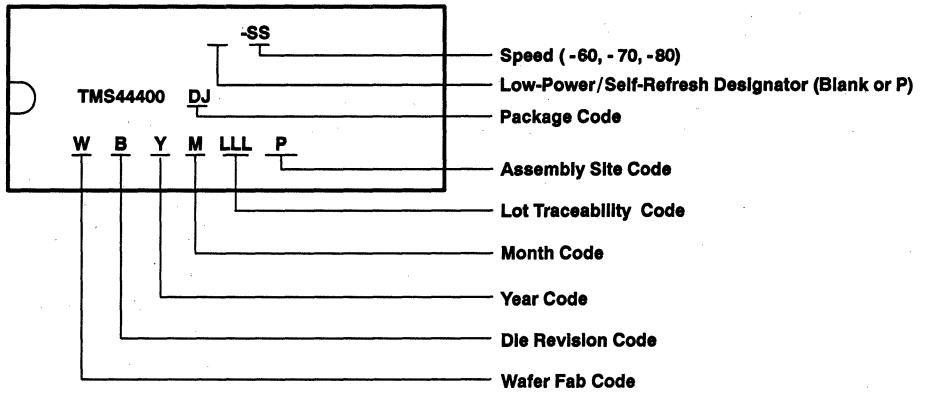


Figure 16. Test-Mode Entry-Cycle Timing

device symbolization (TMS44400 illustrated)



ADVANCE INFORMATION

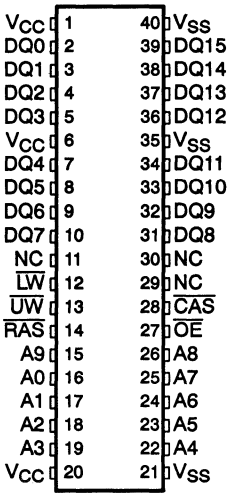
This data sheet is applicable to all TMS44165/Ps symbolized with Revision "D" and subsequent revisions as described on page 4-92.

- **Organization . . . 262 144 × 16**
- **5-V Supply (±10% Tolerance)**
- **Performance Ranges:**

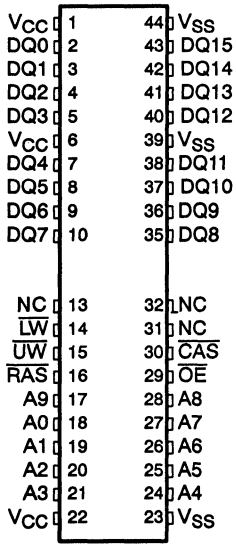
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'44165/P-60	60 ns	15 ns	30 ns	110 ns
'44165/P-70	70 ns	20 ns	35 ns	130 ns
'44165/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced-Page-Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  1024-Cycle Refresh In 16 ms (Max)
  128 ms Max for Low-Power With Self-Refresh Version (TMS44165P)
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs, Outputs, and Clocks Are TTL Compatible**
- **High-Reliability, 40-Lead, 400-Mil-Wide Plastic Surface-Mount (SOJ) Package and 40/44-Lead Thin Small-Outline Package (TSOP)**
- **Operating Free-Air Temperature Range**
  0°C to 70°C
- **Low-Power With Self-Refresh Version**
- **Upper and Lower Byte Control During Write Operations**

DZ PACKAGE
(TOP VIEW)



DGE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE

A0–A9	Address Inputs
DQ0–DQ15	Data In/Data Out
$\overline{CAS}$	Column-Address Strobe
$\overline{LW}$	Lower Write Enable
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{UW}$	Upper Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS44165 series are high-speed, 4 194 304-bit dynamic random-access memories organized as 262 144 words of 16 bits each. The TMS44165P series are high-speed, low-power, self-refresh 4 194 304-bit dynamic random-access memories organized as 262 144 words of 16 bits each. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. Maximum power dissipation is as low as 580 mW operating and 11 mW standby on 80-ns devices. All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS44165 and TMS44165P are each offered in a 40-lead plastic surface-mount SOJ package (DZ suffix) and a 40/44-lead plastic surface-mount TSOP package (DGE suffix). These packages are characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page-mode cycle time used. With minimum $\overline{CAS}$ page cycle time, all 256 columns specified by column addresses A0–A7 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The first falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after t_{RAH} (row-address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low) if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, minimum access time for the next cycle is determined by t_{CPA} (access time from rising edge of the last $\overline{CAS}$).

address (A0–A9)

Eighteen address bits are required to decode 1 of 262144 storage cell locations. Ten row-address bits are set up on A0–A9 and latched onto the chip by $\overline{RAS}$. Then, eight column-address bits are set up on A0 through A7 and latched onto the chip by $\overline{CAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffers and latching the address bits into the column-address buffers.

write enable ($\overline{UW}$, $\overline{LW}$)

The read or write mode is selected through the upper or lower write-enable ($\overline{UW}$, $\overline{LW}$) input. $\overline{LW}$ controls DQ0–DQ7, and $\overline{UW}$ controls DQ8–DQ15. A logic high on the $\overline{UW}$ and $\overline{LW}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{UW}$ or $\overline{LW}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle permitting a write operation with $\overline{OE}$ grounded.

Either $\overline{UW}$ or $\overline{LW}$ can be brought low, and the user can write into eight DQ locations; $\overline{UW}$ and $\overline{LW}$ can be brought low at the same time and all 16 DQ are written into.

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$, $\overline{UW}$, or $\overline{LW}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{UW}$ or $\overline{LW}$ is brought low prior to $\overline{CAS}$, and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ is already low, and data is strobed in by $\overline{UW}$ or $\overline{LW}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines. The $\overline{LW}$ terminal controls DQ0–DQ7. The $\overline{UW}$ pin controls DQ8–DQ15.

data out (DQ0–DQ15)

The 3-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{CAS}$) as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

$\overline{RAS}$-only refresh

A refresh operation must be performed at least once every 16 ms (128 ms for TMS44165P) to retain data. This can be achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored, and the refresh address is generated internally.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{CAS}$ remains low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 500 μA refresh current is available on the TMS44165P. Data integrity is maintained using CBR refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

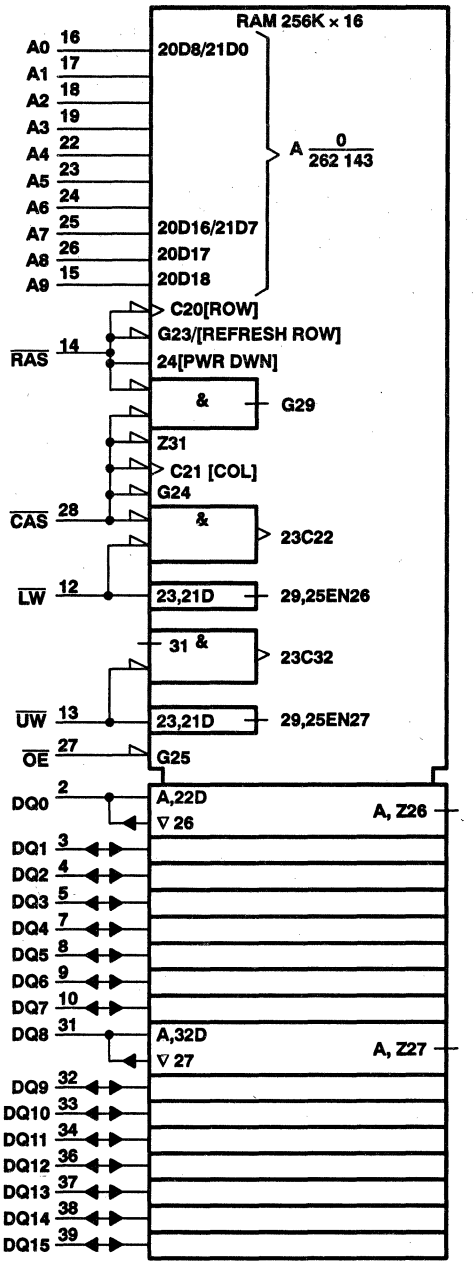
self refresh (TMS44165P)

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This ensures the DRAM is fully refreshed.

power up

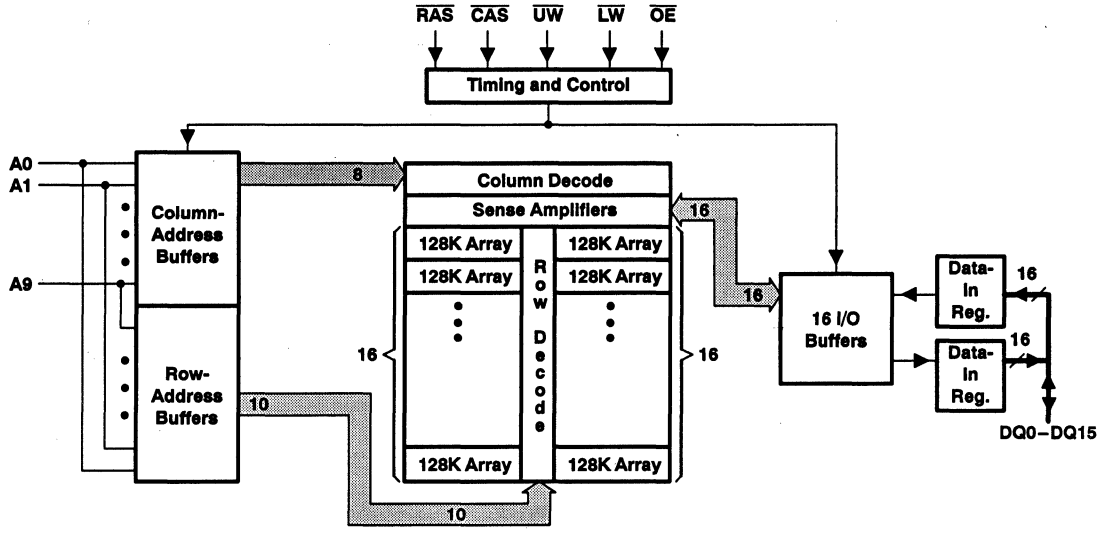
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{RAS}$ cycles is required after power up to the full V_{CC} level.These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the DZ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –1 V to 7 V
Input voltage range (see Note 1) ..... –1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'44165-60 '44165P-60 MIN	'44165-60 '44165P-60 MAX	'44165-70 '44165P-70 MIN	'44165-70 '44165P-70 MAX	'44165-80 '44165P-80 MIN	'44165-80 '44165P-80 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle			140		120		105	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'44165		1		1		1	mA
			'44165P		350		350		350	µA
I_{CC3}‡	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 5.5 V, ($\overline{RAS}$ only), $\overline{CAS}$ high (CBR only), $\overline{RAS}$ low after $\overline{CAS}$ low	Minimum cycle, $\overline{RAS}$ cycling,		140		120		105	mA
I_{CC4}†§	Average page current	V_{CC} = 5.5 V, $\overline{RAS}$ low,	t_{PC} = MIN, $\overline{CAS}$ cycling		120		100		85	mA
I_{CC5}¶	Battery back-up operating current (equivalent refresh time is 64 ms); CBR only	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{UW}$, $\overline{LW}$ and $\overline{OE}$ = V_{IH}, Address and data stable			500		500		500	µA
I_{CC6}†¶	Self-refresh current	$\overline{CAS}$ < 0.2 V, t_{RAS} and t_{CAS} > 1 s	$\overline{RAS}$ < 0.2 V,		400		400		400	µA

† Measured with outputs open
‡ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
§ Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}
¶ For TMS44165P only

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz# (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A8		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{xW}$		7	pF
C_o	Output capacitance		7	pF

Capacitance measurements are made on a sample basis only.
NOTE 3: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'44165-60 '44165P-60		'44165-70 '44165P-70		'44165-80 '44165P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		15		20		20	ns
t_{AA}	Access time from column address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		20		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	Delay time, $\overline{CAS}$ low to output in the low-impedance state	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 4)	0	15	0	20	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 4)	0	15	0	20	0	20	ns

NOTE 4: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		'44165-60 '44165P-60		'44165-70 '44165P-70		'44165-80 '44165P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read (see Note 6)	110		130		150		ns
t_{WC}	Cycle time, write	110		130		150		ns
t_{RWC}	Cycle time, read-write/read-modify-write	155		185		205		ns
t_{PC}	Cycle time, page-mode read or write (see Note 7)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-modify-write	85		90		105		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 8)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 8)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 9)	15	10 000	20	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, write	15		15		15		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{xW}$ low (see Note 10)	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{xW}$ low before $\overline{CAS}$ high	15		20		20		ns
t_{RWL}	Setup time, $\overline{xW}$ low before $\overline{RAS}$ high	15		20		20		ns
t_{WCS}	Setup time, $\overline{xW}$ low before $\overline{CAS}$ low (see Note 11)	0		0		0		ns

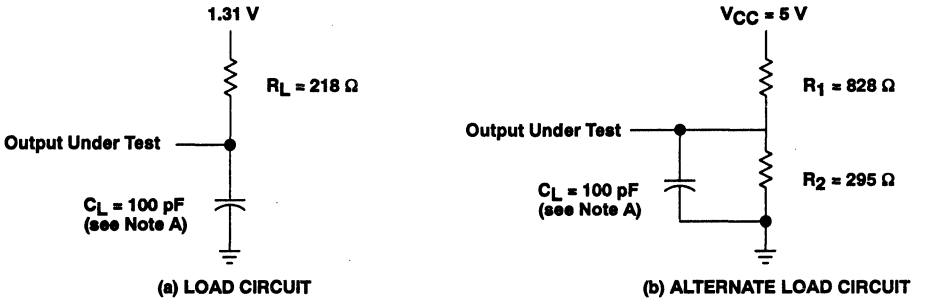
NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_T = 5 ns.
7. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
8. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed.
9. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
11. Early-write operation only

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued) (see Note 5)

			'44165-60 '44165P-60		'44165-70 '44165P-70		'44165-80 '44165P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Hold time, column address after $\overline{CAS}$ low (see Note 10)		10		15		15		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 13)		30		35		35		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low (see Note 10)		10		15		15		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 13)		30		35		35		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low		10		10		10		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 14)		0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 14)		0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low (see Note 14)		10		15		15		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low (see Note 12)		30		35		35		ns
t_{CLCH}	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high		5		5		5		ns
t_{AWD}	Delay time, column address to $\overline{xW}$ low (see Note 15)		55		65		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 11)		15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 11)		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{xW}$ low (see Note 15)		40		50		50		ns
t_{OEH}	Hold time, $\overline{OE}$ command		15		20		20		ns
t_{OED}	Delay time, $\overline{OE}$ high before data at DQ		15		20		20		ns
t_{ROH}	Delay time, $\overline{OE}$ low to $\overline{RAS}$ high		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 16)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 16)		20	45	20	50	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 11)		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		15		20		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{xW}$ low (see Note 15)		85		100		110		ns
t_{CPR}	Pulse duration, $\overline{CAS}$ precharge before self refresh		0		0		0		ns
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self refresh		110		130		150		ns
t_{RASS}	Pulse duration, self refresh entry from $\overline{RAS}$ low		100		100		100		µs
t_{CHS}	Hold time, $\overline{CAS}$ low after $\overline{RAS}$ high (for self refresh)		−50		−50		−50		ns
t_{REF}	Refresh time interval	'44165		16		16		16	ms
		'44165P		128		128		128	
t_T	Transition time		2	50	2	50	2	50	ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
10. Referenced in the later of $\overline{CAS}$ or $\overline{xW}$ in write operations
11. Early-write operation only
12. CBR refresh only
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. Read-modify-write operation only
16. Maximum value specified only to assure access time

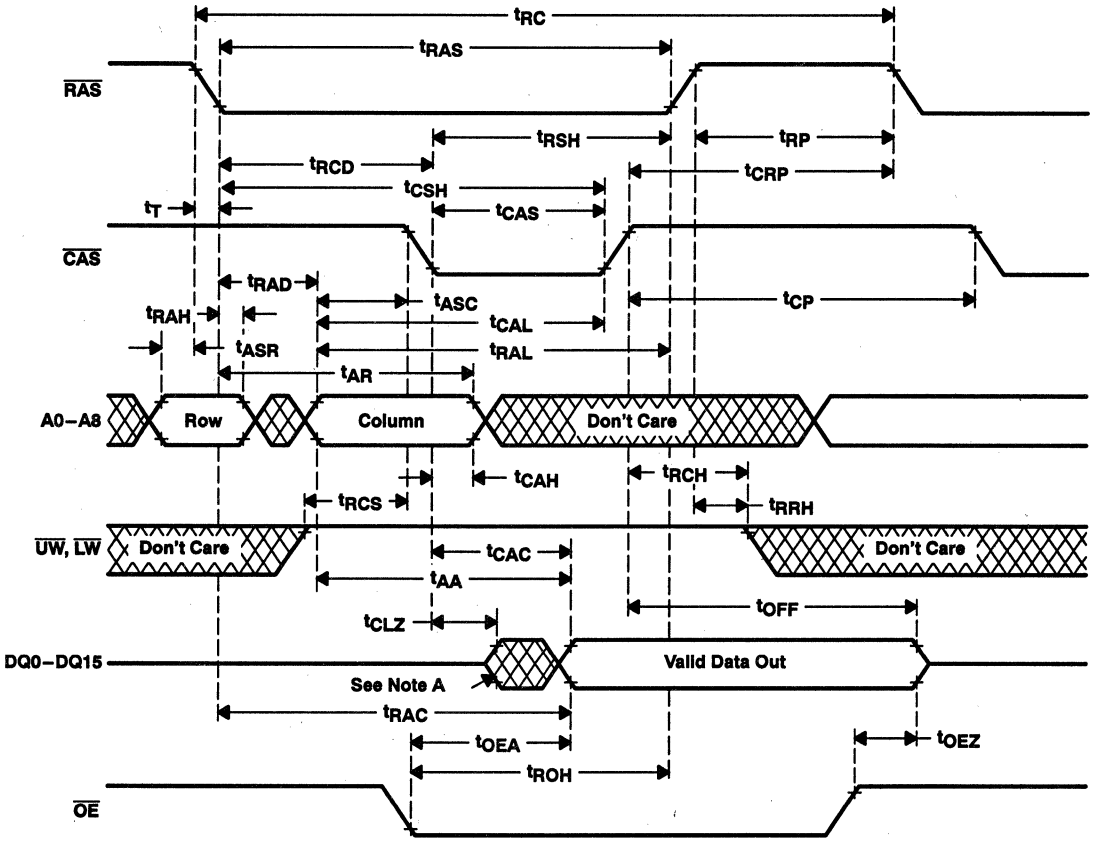
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

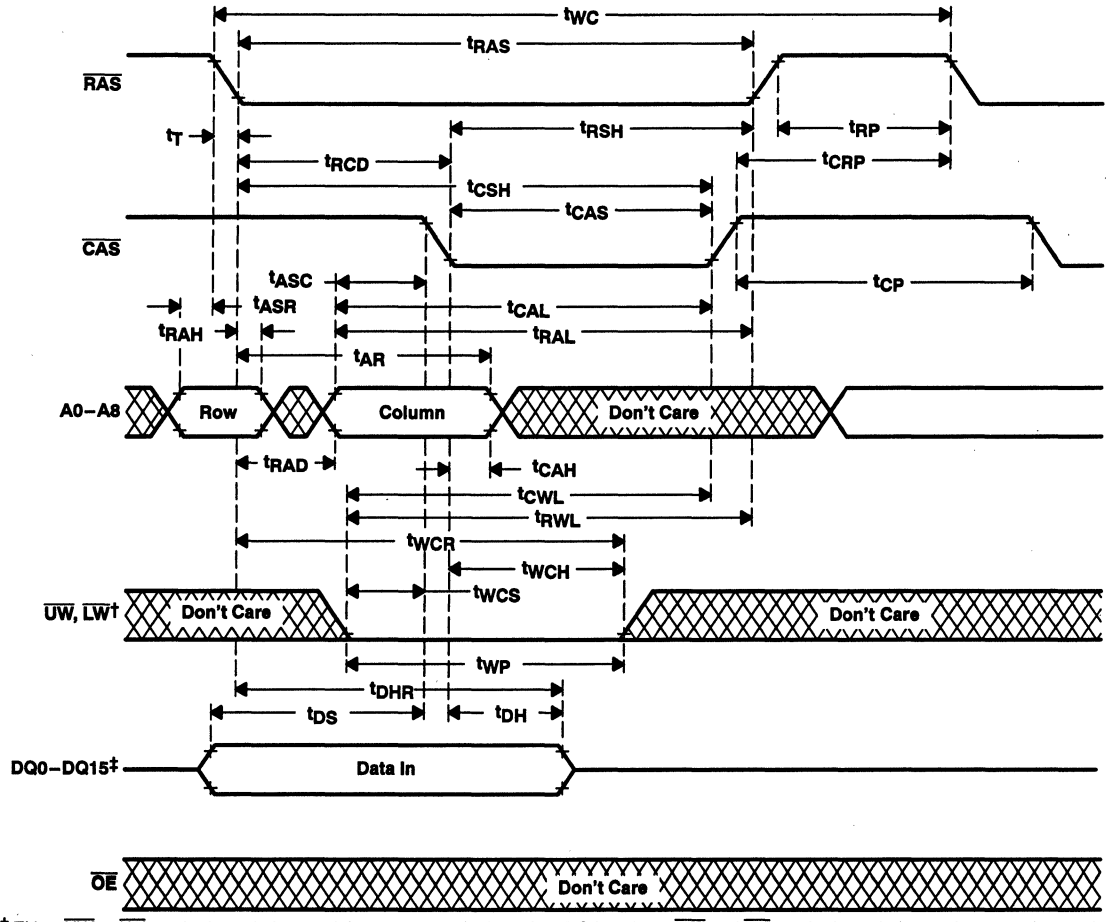
PARAMETER MEASUREMENT INFORMATION



NOTE B: Output can go from the high-impedance state to an invalid data state prior to the specified access time.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

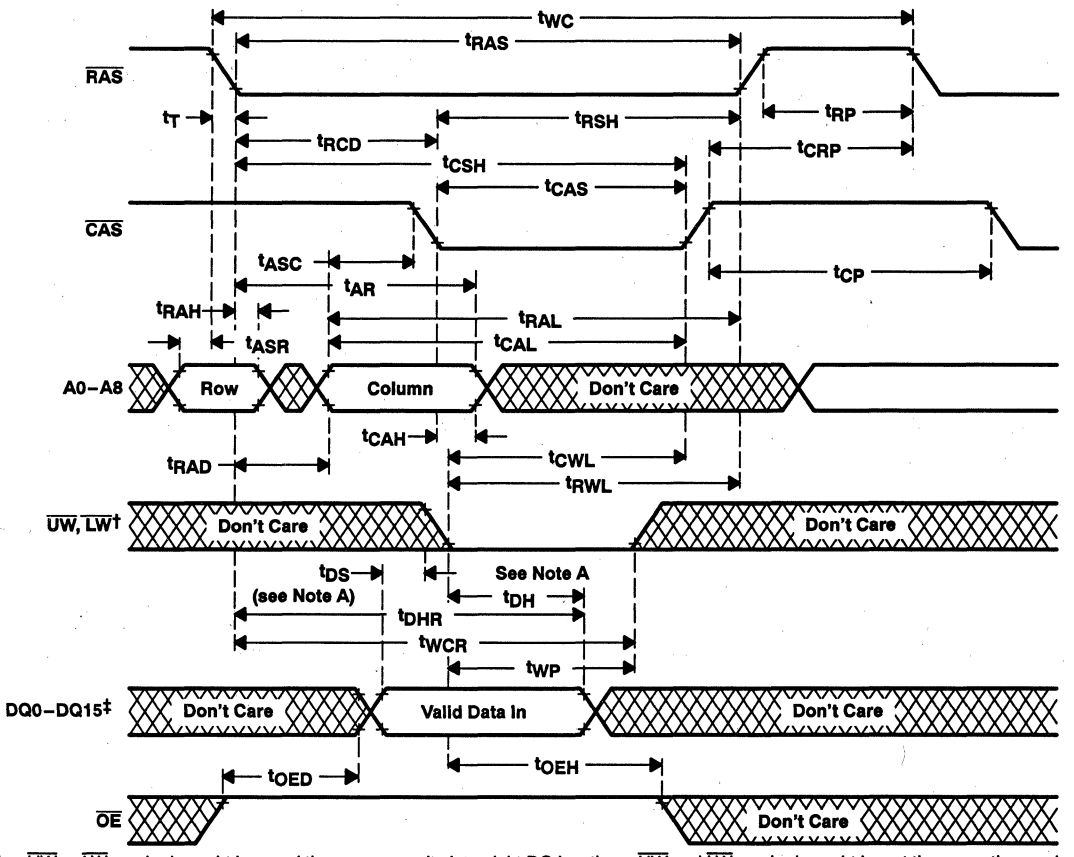


† Either $\overline{UW}$ or $\overline{LW}$ can be brought low, and the user can write into eight DQ locations; $\overline{UW}$ and $\overline{LW}$ can be brought low at the same time and all 16 DQ locations are written into.

‡ All DQ pins remain in the high-impedance state for an early write cycle.

Figure 3. Early-Write-Cycle Timing

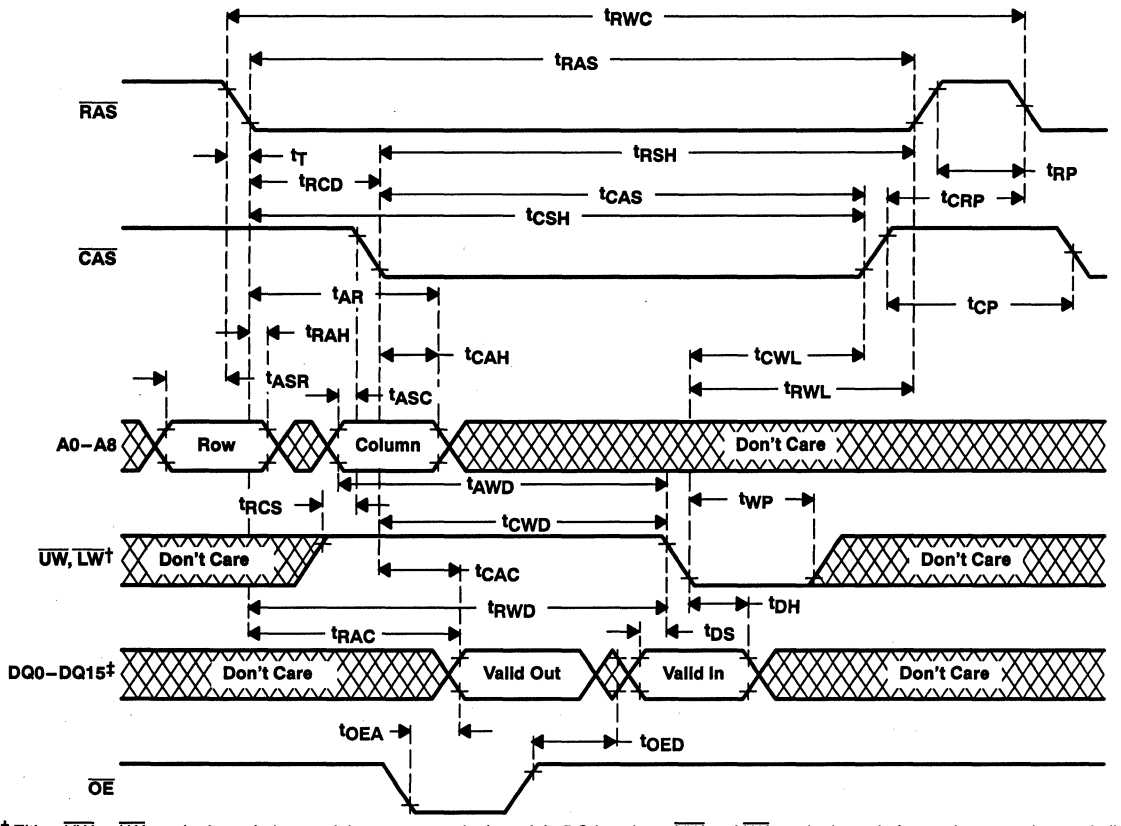
PARAMETER MEASUREMENT INFORMATION



† Either $\overline{UW}$ or $\overline{LW}$ can be brought low, and the user can write into eight DQ locations; $\overline{UW}$ and $\overline{LW}$ can be brought low at the same time and all 16 DQ locations are written into.
‡ All DQ pins remain in the high-impedance state for an early write cycle.
NOTE A: Later of $\overline{CAS}$ or $\overline{xW}$ in write operations.

Figure 4. Write-Cycle Timing

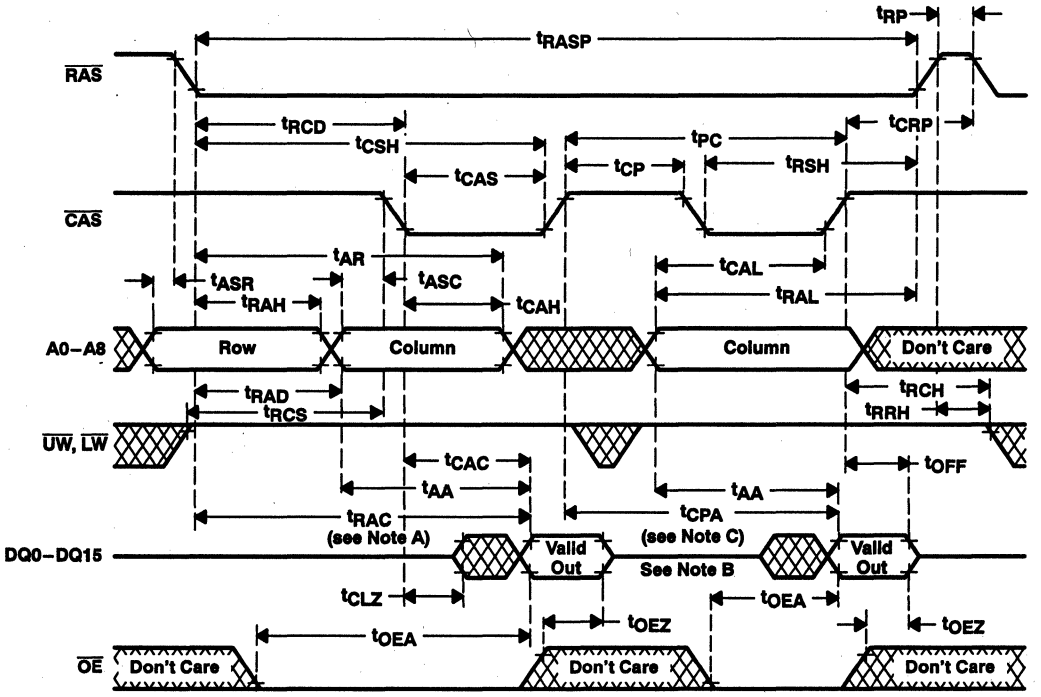
PARAMETER MEASUREMENT INFORMATION



† Either $\overline{UW}$ or $\overline{LW}$ can be brought low, and the user can write into eight DQ locations; $\overline{UW}$ and $\overline{LW}$ can be brought low at the same time and all 16 DQ locations are written into.
‡ All DQ pins remain in the high-impedance state for an early write cycle.

Figure 5. Read-Modify-Write-Cycle Timing

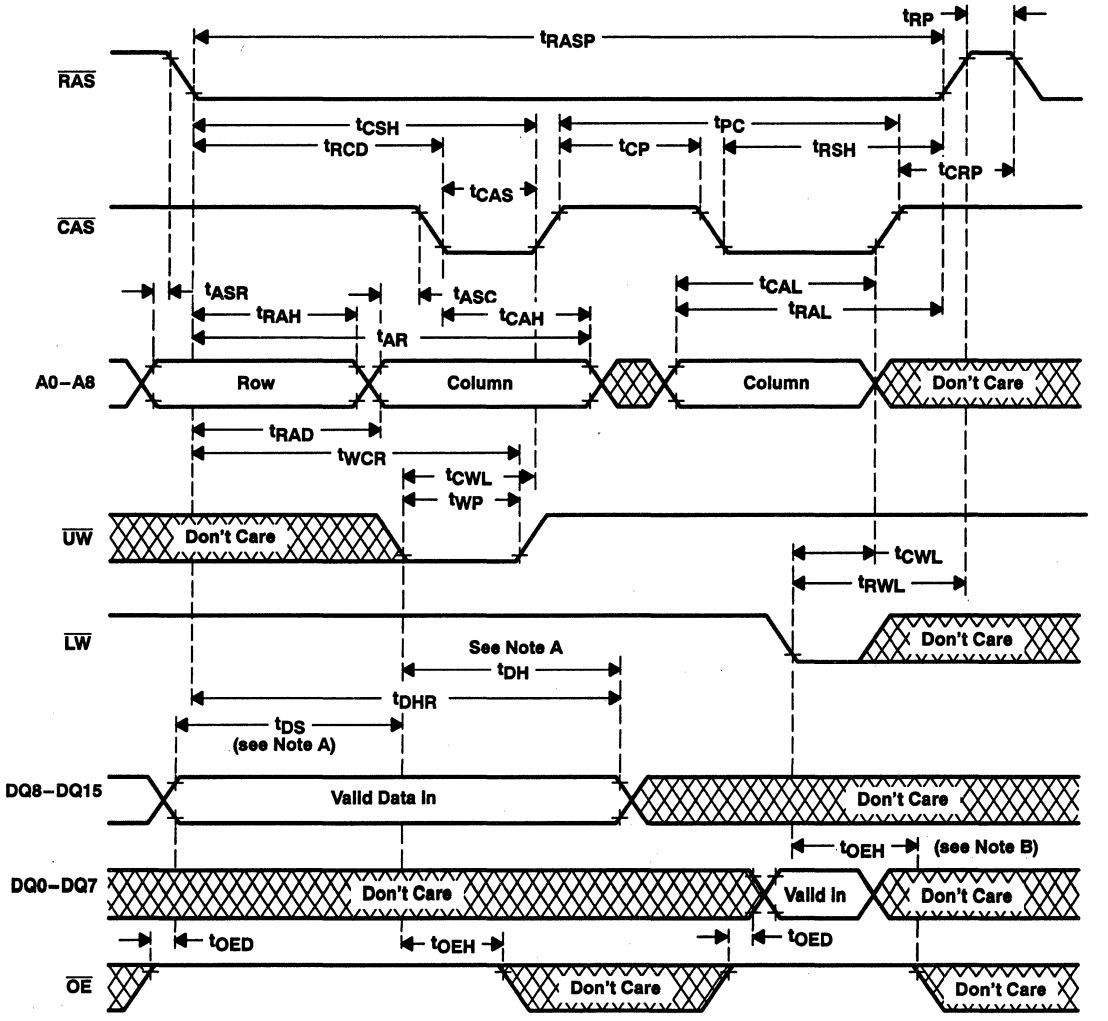
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid data state prior to the specified access time.
B. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
C. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

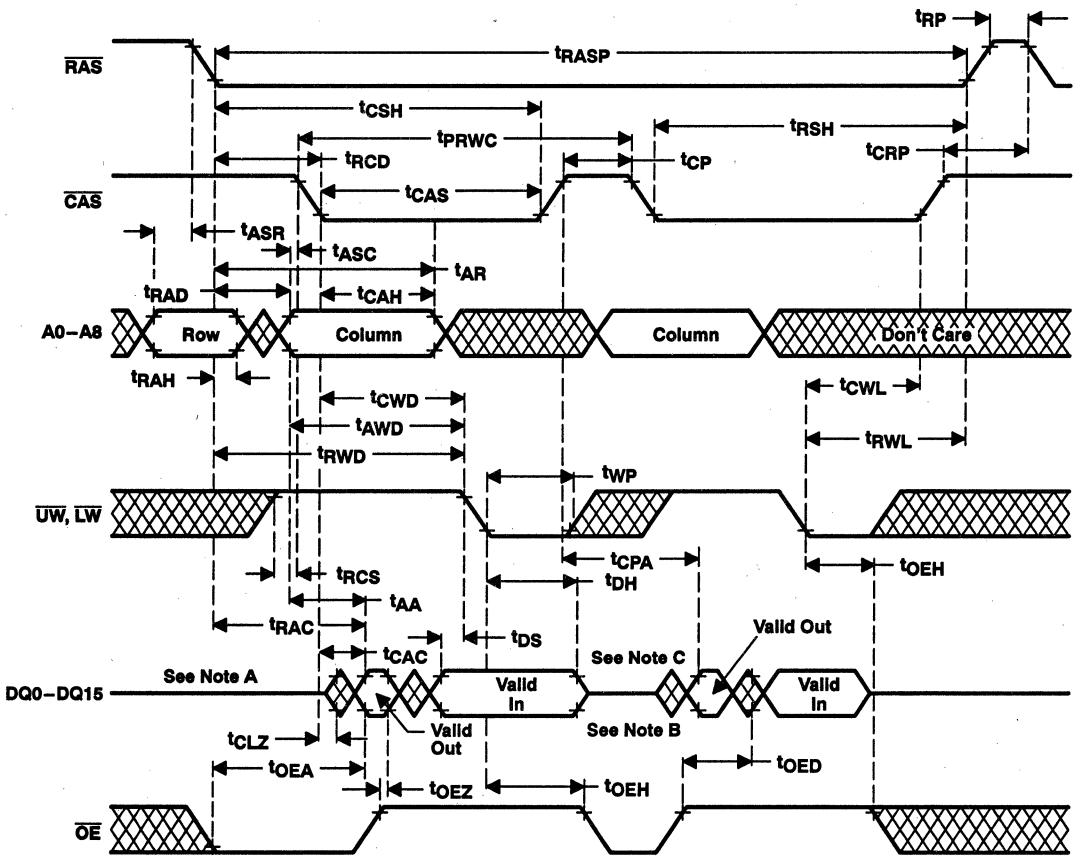
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Later of $\overline{CAS}$ or $\overline{xW}$ in write operations.
B. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.
C. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

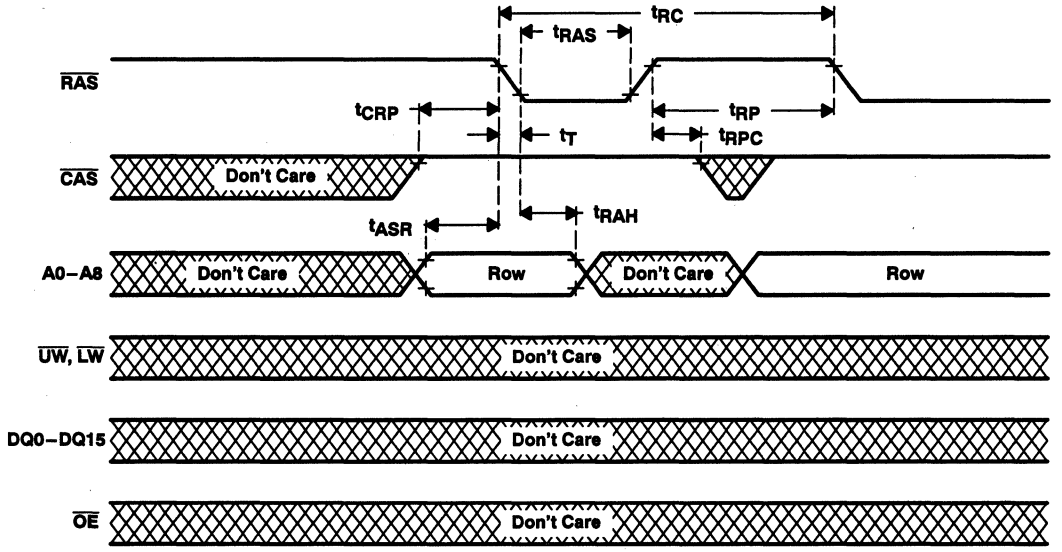


Figure 9. RAS-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

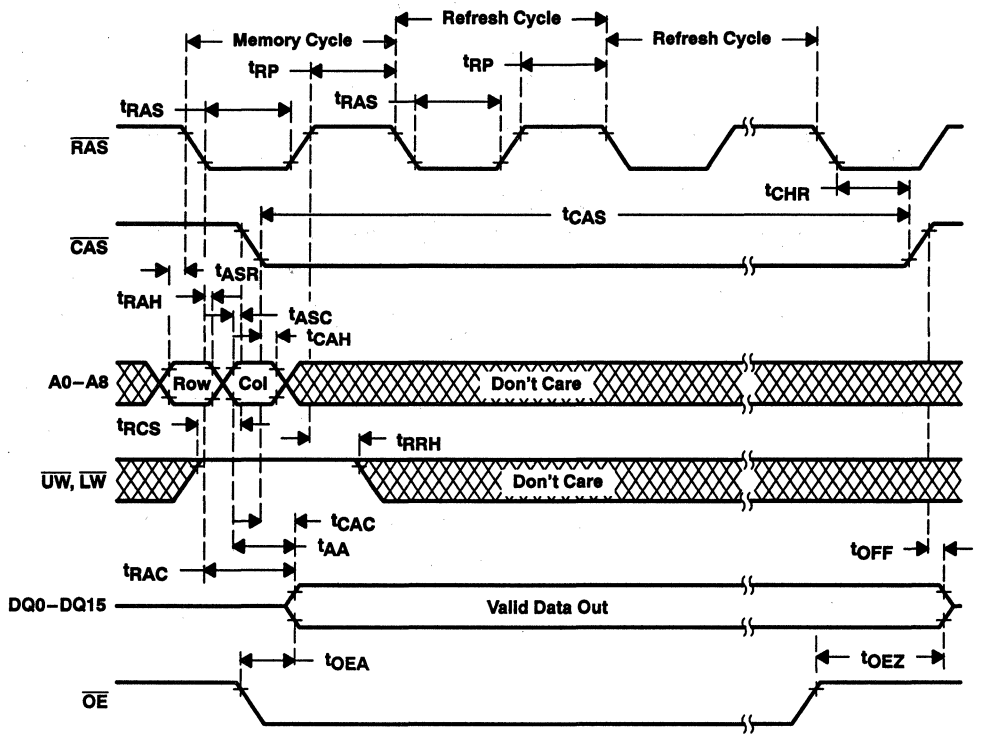


Figure 10. Hidden-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

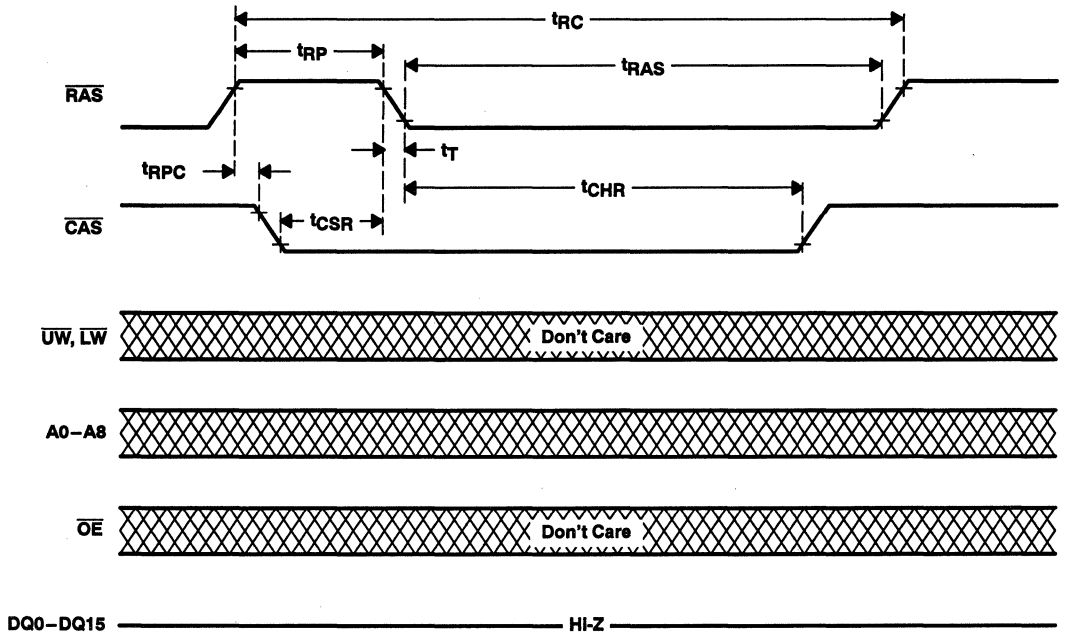


Figure 11. Automatic CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

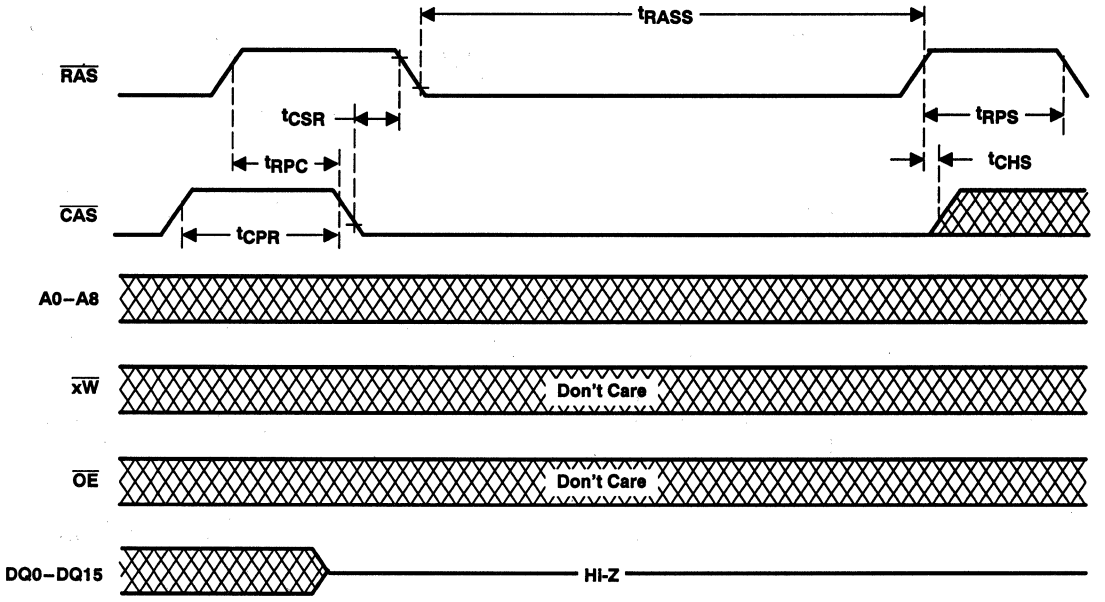
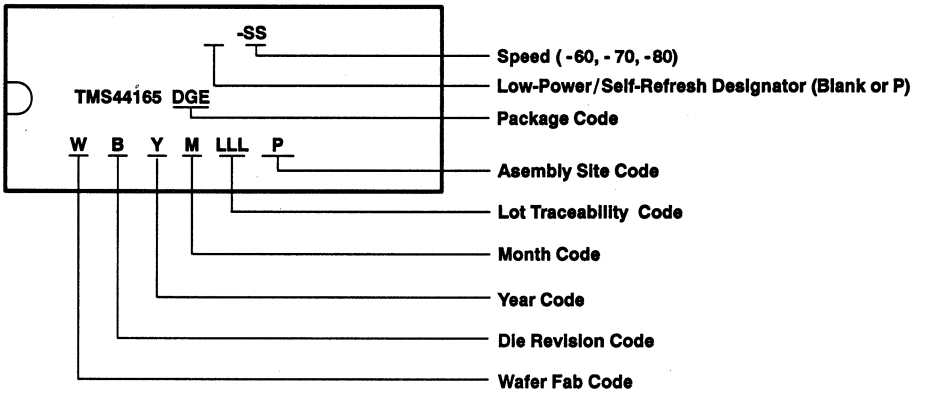


Figure 12. Self-Refresh-Cycle Timing

device symbolization (TMS44165 illustrated)



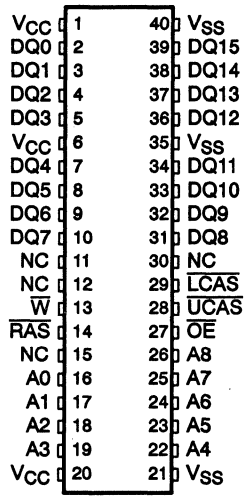
This data sheet is applicable to all TMS45160/Ps symbolized with Revision "D" and subsequent revisions as described on page 4-113.

- **Organization . . . 262144 × 16**
- **5-V Supply (±10% Tolerance)**
- **Performance Ranges:**

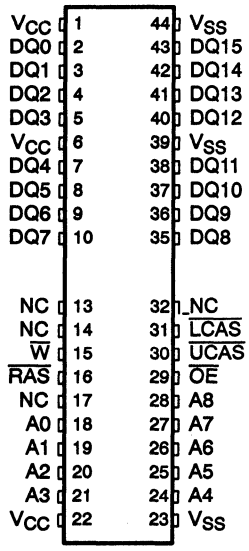
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'45160/P-60	60 ns	15 ns	30 ns	110 ns
'45160/P-70	70 ns	20 ns	35 ns	130 ns
'45160/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced-Page-Mode Operation With $\overline{\text{xCAS}}$-Before-$\overline{\text{RAS}}$ (xCBR) Refresh**
- **Long Refresh Period**
  - **512-Cycle Refresh In 8 ms (Max)**
  - **64 ms Max for Low Power With Self-Refresh Version (TMS45160P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs, Outputs, and Clocks Are TTL Compatible**
- **High-Reliability, 40-Lead, 400-Mil-Wide Plastic Surface-Mount (SOJ) Package and 40/44-Lead Thin Small-Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Low Power With Self-Refresh Version**
- **Upper and Lower Byte Control During Read and Write Operations**

DZ PACKAGE
(TOP VIEW)



DGE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE

A0–A8	Address Inputs
DQ0–DQ15	Data In/Data Out
$\overline{\text{LCAS}}$	Lower Column-Address Strobe
NC	No Internal Connection
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row-Address Strobe
$\overline{\text{UCAS}}$	Upper Column-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

description

The TMS45160 series are high-speed, 4194304-bit dynamic random-access memories organized as 262144 words of 16 bits each. The TMS45160P series are high-speed, low-power, self-refresh 4194304-bit dynamic random-access memories organized as 262144 words of 16 bits each. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

These devices feature maximum $\overline{\text{RAS}}$ access times of 60 ns, 70 ns, and 80 ns. Maximum power dissipation is as low as 770 mW operating and 11 mW standby on 80-ns devices. All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS45160 and TMS45160P are each offered in a 40-lead plastic surface-mount SOJ package (DZ suffix) and a 40/44-lead plastic surface-mount small-outline (TSOP) package (DGE suffix). These packages are characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

operation

dual $\overline{CAS}$

Two $\overline{CAS}$ pins ($\overline{LCAS}$–$\overline{UCAS}$) are provided to give independent control of the 16 data I/O pins (DQ0–DQ15) with $\overline{LCAS}$ corresponding to DQ0–DQ7 and $\overline{UCAS}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{xCAS}$ falling edge. Each $\overline{xCAS}$ going low enables its corresponding DQx pins with data associated with the column address latched on the first falling $\overline{xCAS}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{xCAS}$ edge.The delay time from $\overline{xCAS}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{xCAS}$ to its corresponding DQx pins.

In order to latch in a new column address, both $\overline{xCAS}$ pins must be brought high. The column precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first falling $\overline{xCAS}$ edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

For early-write cycles, the data is latched on the first falling edge of $\overline{xCAS}$. Only the DQs that have the corresponding $\overline{xCAS}$ low are written into. Each $\overline{xCAS}$ must meet t_{CAS} minimum in order to ensure writing into the storage cell. In order to latch a new address and new data, both $\overline{xCAS}$ pins must go high and meet t_{CP}.

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{xCAS}$ page-mode cycle time used. With minimum $\overline{xCAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{xCAS}$ is high. The first falling edge of $\overline{xCAS}$ latches the column addresses. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as column address is valid rather than when $\overline{xCAS}$ transitions low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after t_{RAH} (row-address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{xCAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{xCAS}$ low) if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{xCAS}$ goes high, minimum access time for the next cycle is determined by t_{CPA} (access time from rising edge of the last $\overline{xCAS}$).

address (A0–A8)

Eighteen address bits are required to decode 1 of 262144 storage cell locations. Nine row-address bits are set up on A0 through A8 and latched onto the chip by $\overline{RAS}$. Then, nine column-address bits are set up on A0 through A8 and latched onto the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. $\overline{W}$ can be driven from the standard TTL circuits without a pullup resistor. The data input lines are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{OE}$ grounded.

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{xCAS}$ and the data is strobed in by the first occurring $\overline{xCAS}$ with setup and hold times referenced to data in. In a delayed-write or read-modify-write cycle, $\overline{xCAS}$ is already low and the data is strobed in by $\overline{W}$ with setup and hold times referenced to data in. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

data out (DQ0–DQ15)

The 3-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access-time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{xCAS}$ to be brought low for the output buffers to go into the low-impedance state. They remain in the low-impedance state until either $\overline{OE}$ or $\overline{xCAS}$ is brought high.

$\overline{RAS}$-only refresh

A refresh operation must be performed at least once every 8 ms (64 ms for TMS45160P) to retain data. This can be achieved by strobing each of the 512 rows (A0–A8). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding all $\overline{xCAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored and the refresh address is generated internally.

$\overline{xCAS}$-before-$\overline{RAS}$ (xCBR) refresh

xCBR refresh is utilized by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive xCBR refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 500-μA refresh current is available on the TMS45160P. Data integrity is maintained using xCBR refresh with a period of 125 μs holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

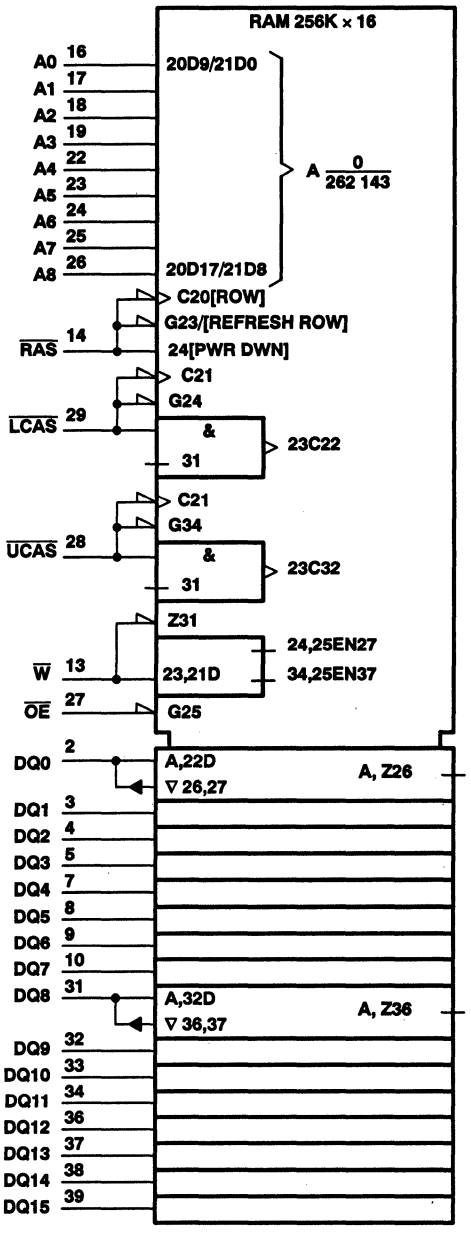
self refresh (TMS45160P)

The self-refresh mode is entered by dropping $\overline{xCAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{xCAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{xCAS}$ are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This ensures that the DRAM is fully refreshed.

power up

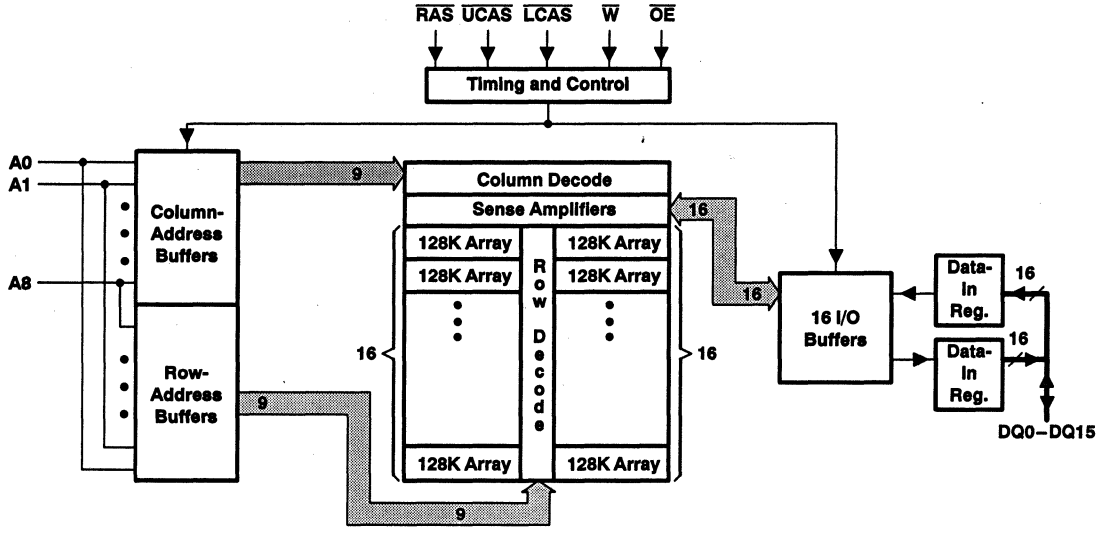
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{RAS}$ cycles is required after power up to the full V_{CC} level.These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or $\overline{xCBR}$) cycle.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the DZ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 1 V to 7 V
Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'45160-60 '45160P-60 MIN	'45160-60 '45160P-60 MAX	'45160-70 '45160P-70 MIN	'45160-70 '45160P-70 MAX	'45160-80 '45160P-80 MIN	'45160-80 '45160P-80 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle			180		160		140	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'45160		1		1		1	mA
			'45160P		350		350		350	µA
I_{CC3}‡	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 5.5 V, ($\overline{RAS}$ only), Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high (CBR only), $\overline{RAS}$ low after $\overline{xCAS}$ low			180		160		140	mA
I_{CC4}†§	Average page current	V_{CC} = 5.5 V, $\overline{RAS}$ low, t_{PC} = MIN, $\overline{xCAS}$ cycling			160		140		120	mA
I_{CC5}¶	Battery-backup operating current (equivalent refresh time is 64 ms); CBR only	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			500		500		500	µA
I_{CC6}†¶	Self-refresh current	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			400		400		400	µA

† Measured with outputs open
‡ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
§ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}
¶ For TMS45160P only

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz# (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A8		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{xCAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance		7	pF

Capacitance measurements are made on a sample basis only.
NOTE 3: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'45160-60 '45160P-60		'45160-70 '45160P-70		'45160-80 '45160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{xCAS}$ low		15		20		20	ns
t_{AA}	Access time from column address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		20		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	Delay time, $\overline{xCAS}$ low to output in low impedance	0		0		0		ns
t_{OFF}	Output disable time after $\overline{xCAS}$ high (see Note 4)	0	15	0	20	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 4)	0	15	0	20	0	20	ns

NOTE 4: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		'45160-60 '45160P-60		'45160-70 '45160P-70		'45160-80 '45160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read (see Note 6)	110		130		150		ns
t_{WC}	Cycle time, write	110		130		150		ns
t_{RWC}	Cycle time, read-write/read-modify-write	155		185		205		ns
t_{PC}	Cycle time, page-mode read or write (see Note 7)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-modify-write	85		90		105		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 8)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 8)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{xCAS}$ low (see Note 9)	15	10 000	20	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{xCAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, write	15		15		15		ns
t_{ASC}	Setup time, column address before $\overline{xCAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{W}$ low (see Note 10)	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{xCAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ high	15		20		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		20		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ low (see Note 11)	0		0		0		ns

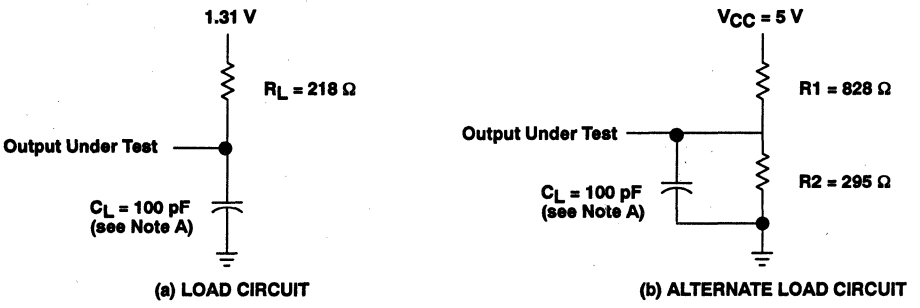
NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_T = 5 ns.
7. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
8. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed.
9. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed.
10. Referenced to the later of $\overline{xCAS}$ or $\overline{W}$ in write operations
11. Early-write operation only

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued) (see Note 5)

			'45160-60 '45160P-60		'45160-70 '45160P-70		'45160-80 '45160P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Hold time, column address after $\overline{xCAS}$ low (see Note 10)		10		15		15		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 12)		30		35		35		ns
t_{DH}	Hold time, data after $\overline{xCAS}$ low (see Note 10)		10		15		15		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 12)		30		35		35		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low		10		10		10		ns
t_{RCH}	Hold time, read after $\overline{xCAS}$ high (see Note 13)		0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 13)		0		0		0		ns
t_{WCH}	Hold time, write after $\overline{xCAS}$ low (see Note 13)		10		15		15		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low (see Note 14)		30		35		35		ns
t_{CLCH}	Hold time, $\overline{xCAS}$ low to $\overline{xCAS}$ high		5		5		5		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (see Note 15)		55		65		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high (see Note 11)		15		15		20		ns
t_{CRP}	Delay time, $\overline{xCAS}$ high to $\overline{RAS}$ low		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high		60		70		80		ns
t_{CSR}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ low (see Note 11)		10		10		10		ns
t_{CWD}	Delay time, $\overline{xCAS}$ low to $\overline{W}$ low (see Note 15)		40		50		50		ns
t_{OEH}	Hold time, $\overline{OE}$ command		15		20		20		ns
t_{OED}	Delay time, $\overline{OE}$ high before data at DQ		15		20		20		ns
t_{ROH}	Delay time, $\overline{OE}$ low to $\overline{RAS}$ high		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 16)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{xCAS}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ low (see Note 16)		20	45	20	50	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{xCAS}$ low (see Note 11)		0		0		0		ns
t_{RSH}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ high		15		20		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 15)		85		100		110		ns
t_{CPR}	Pulse duration, $\overline{xCAS}$ precharge before self refresh		0		0		0		ns
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self refresh		110		130		150		ns
t_{RASS}	Pulse duration, self refresh entry from $\overline{RAS}$ low		100		100		100		µs
t_{CHS}	Hold time, $\overline{xCAS}$ low after $\overline{RAS}$ high (for self refresh)		−50		−50		−50		ns
t_{REF}	Refresh time interval	'45160		8		8		8	ms
		'45160P		64		64		64	
t_T	Transition time		2	50	2	50	2	50	ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
10. Referenced in the later of $\overline{xCAS}$ or $\overline{W}$ in write operations.
11. Early-write operation only
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. xCBR refresh only
15. Read-modify-write operation only
16. Maximum value specified only to assure access time

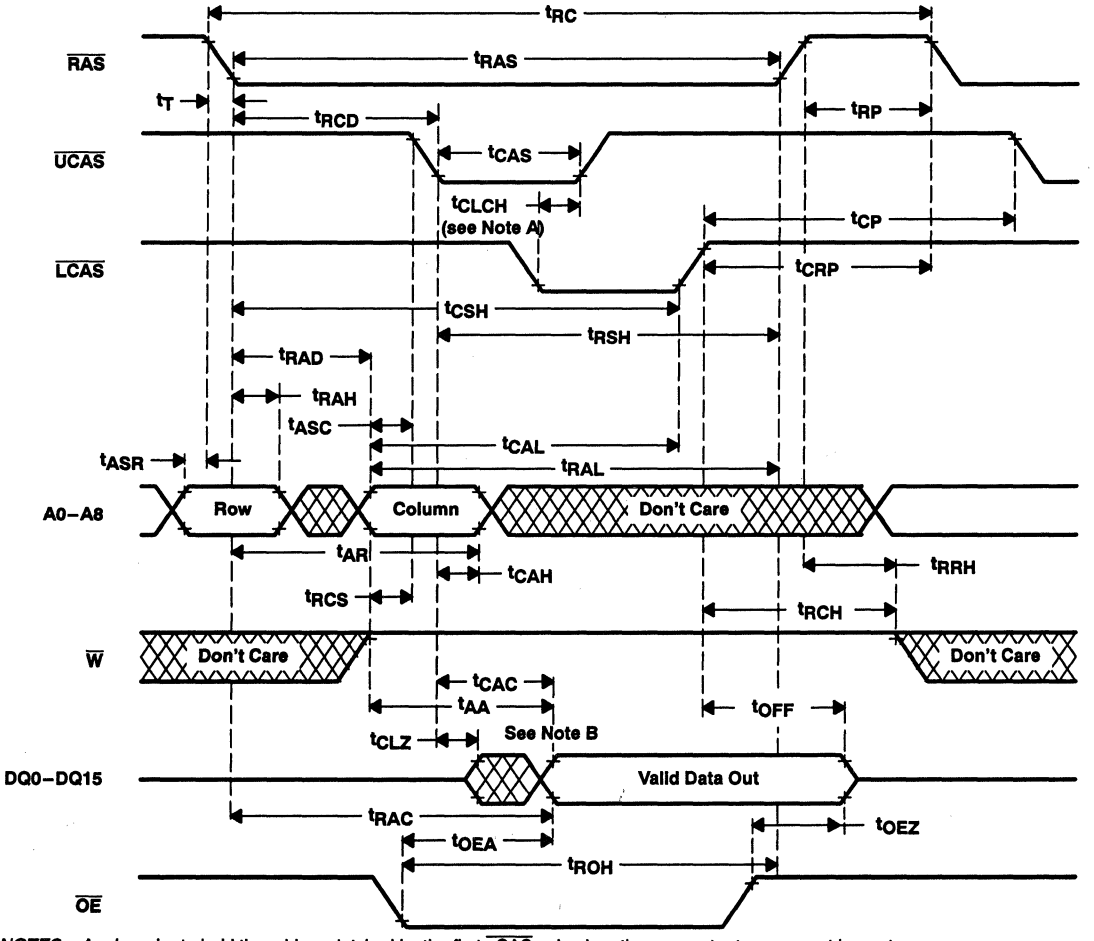
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

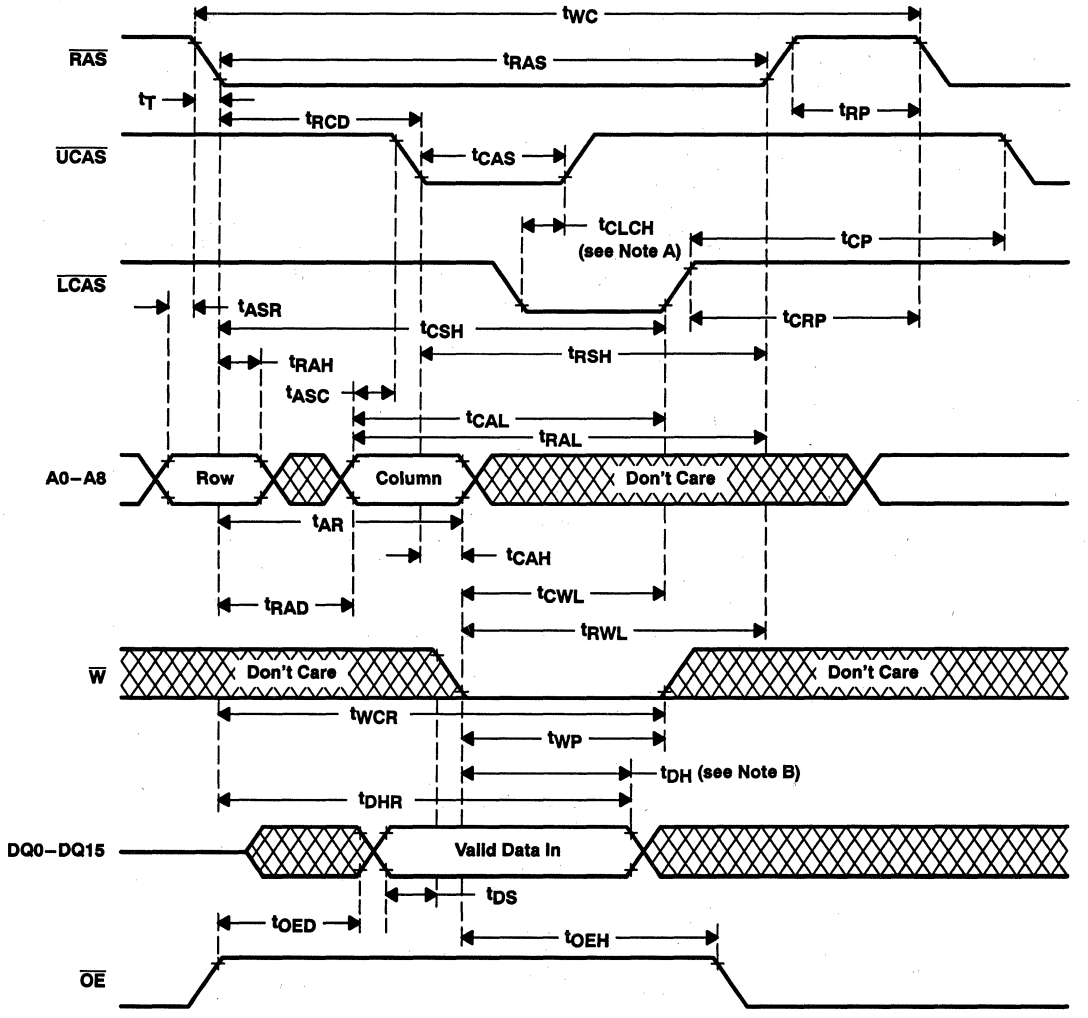
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
C. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
D. $\overline{xCAS}$ order is arbitrary.

Figure 2. Read-Cycle Timing

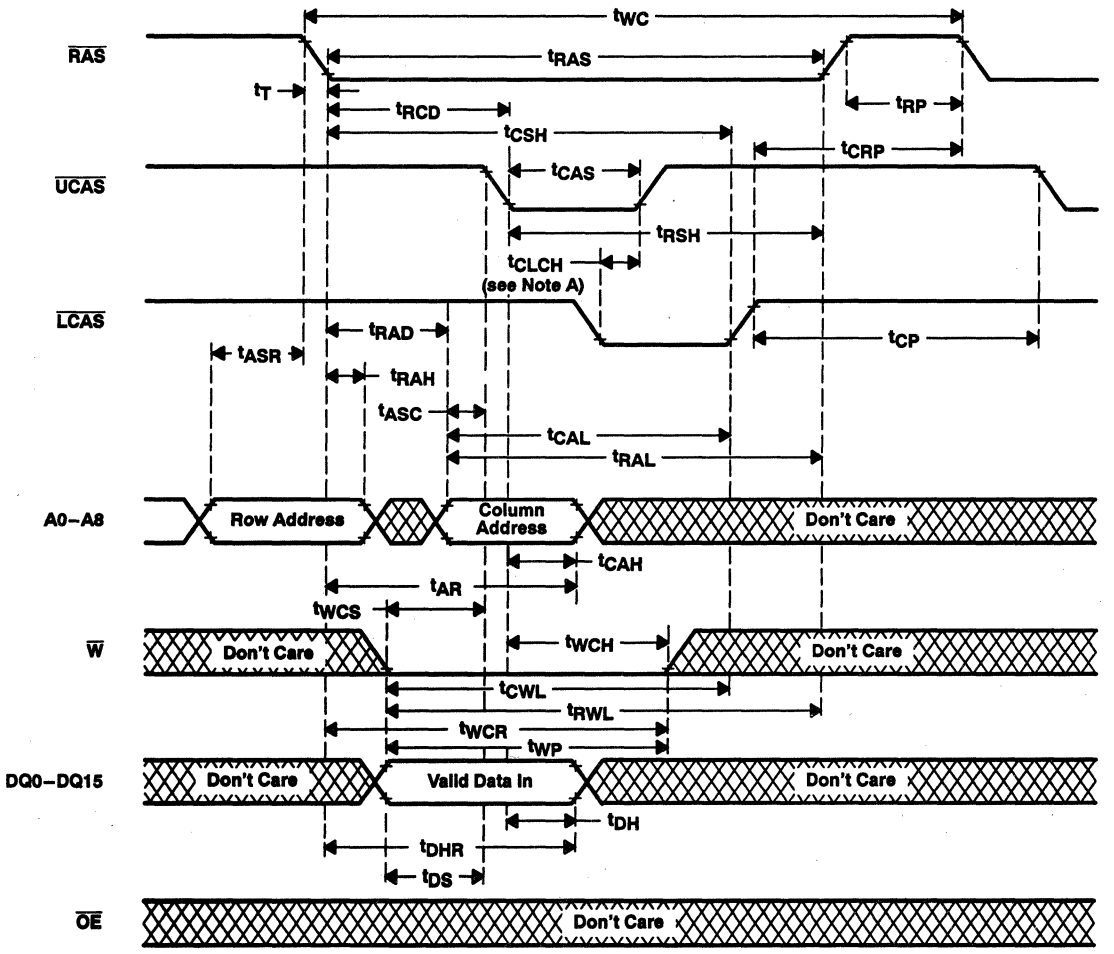
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Later of $\overline{xCAS}$ or $\overline{W}$ in write operations
C. $\overline{xCAS}$ order is arbitrary.

Figure 3. Write-Cycle Timing

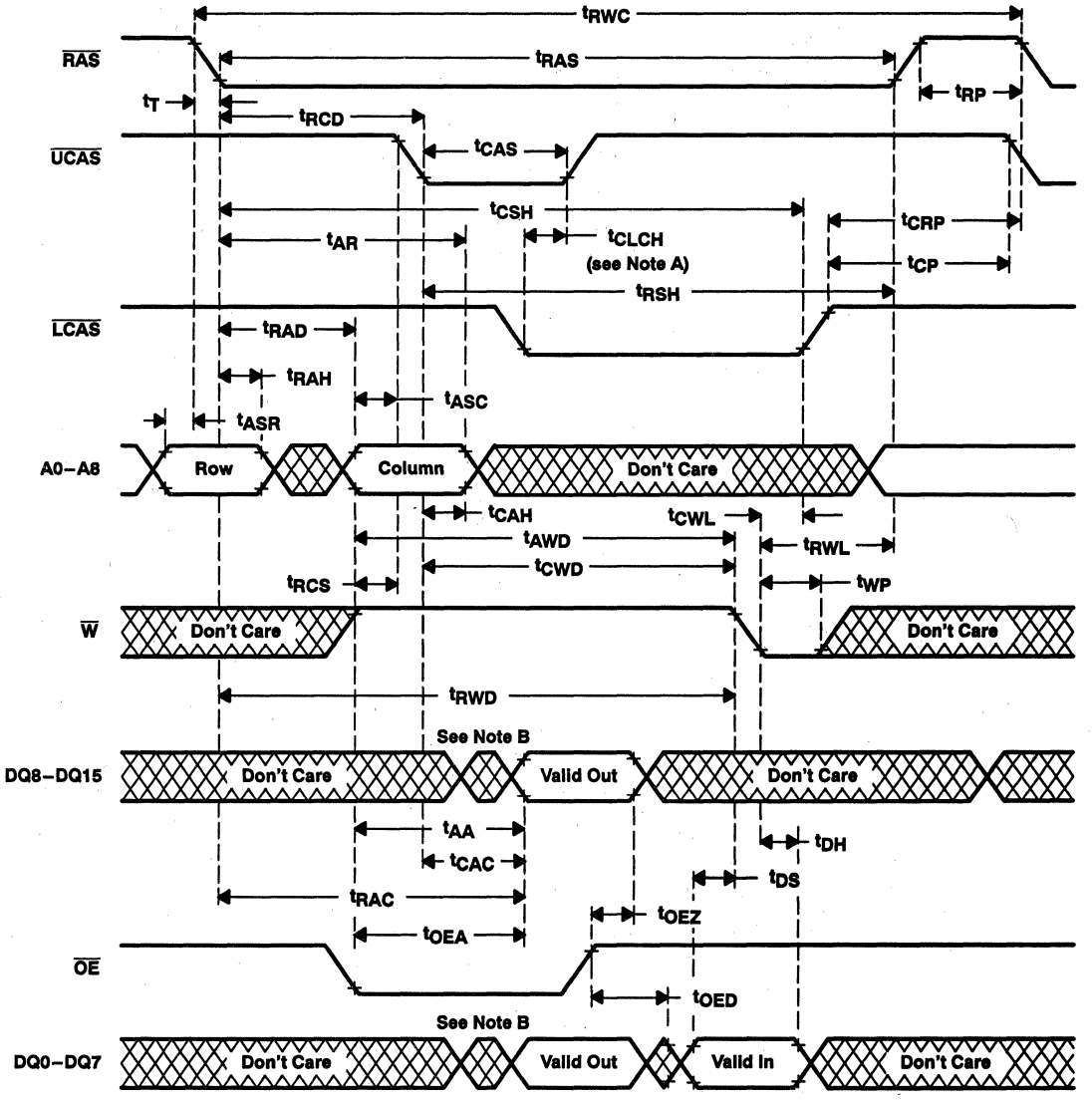
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.

Figure 4. Early-Write-Cycle Timing

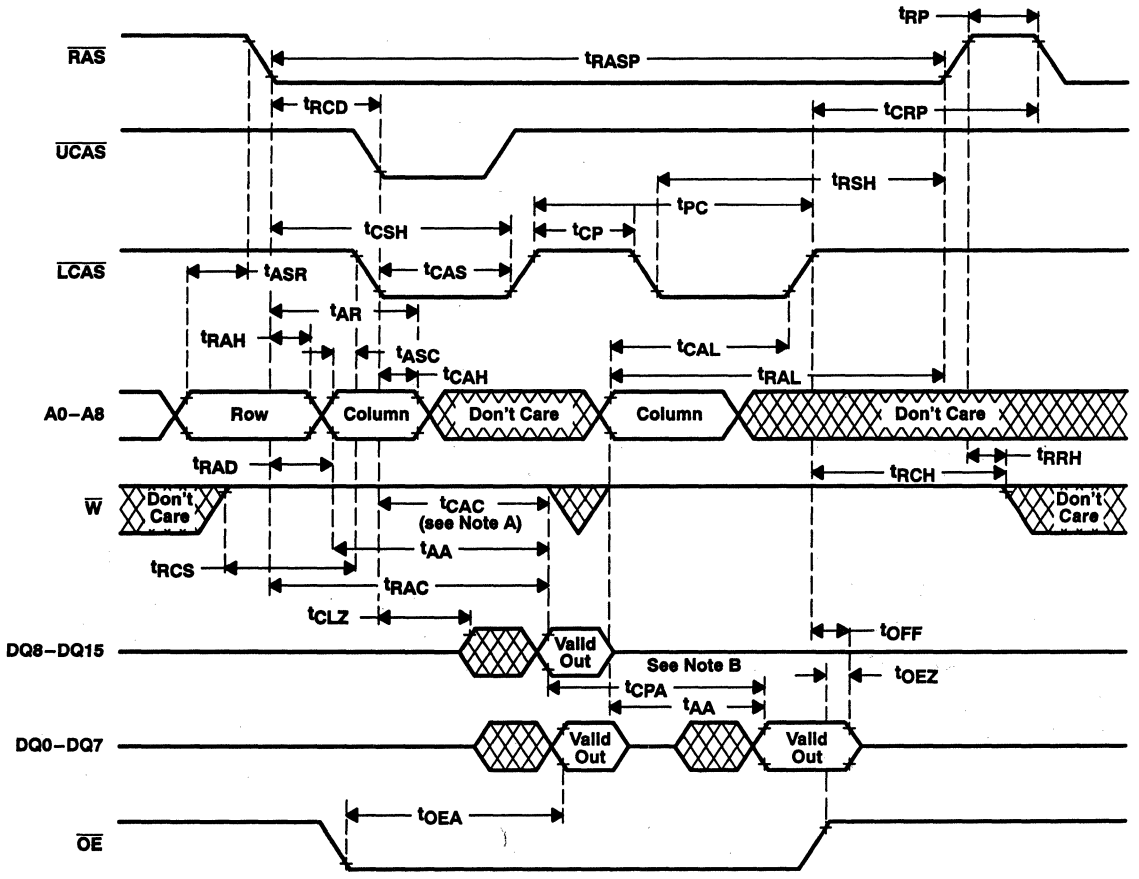
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
C. $\overline{xCAS}$ order is arbitrary.

Figure 5. Read-Modify-Write-Cycle Timing

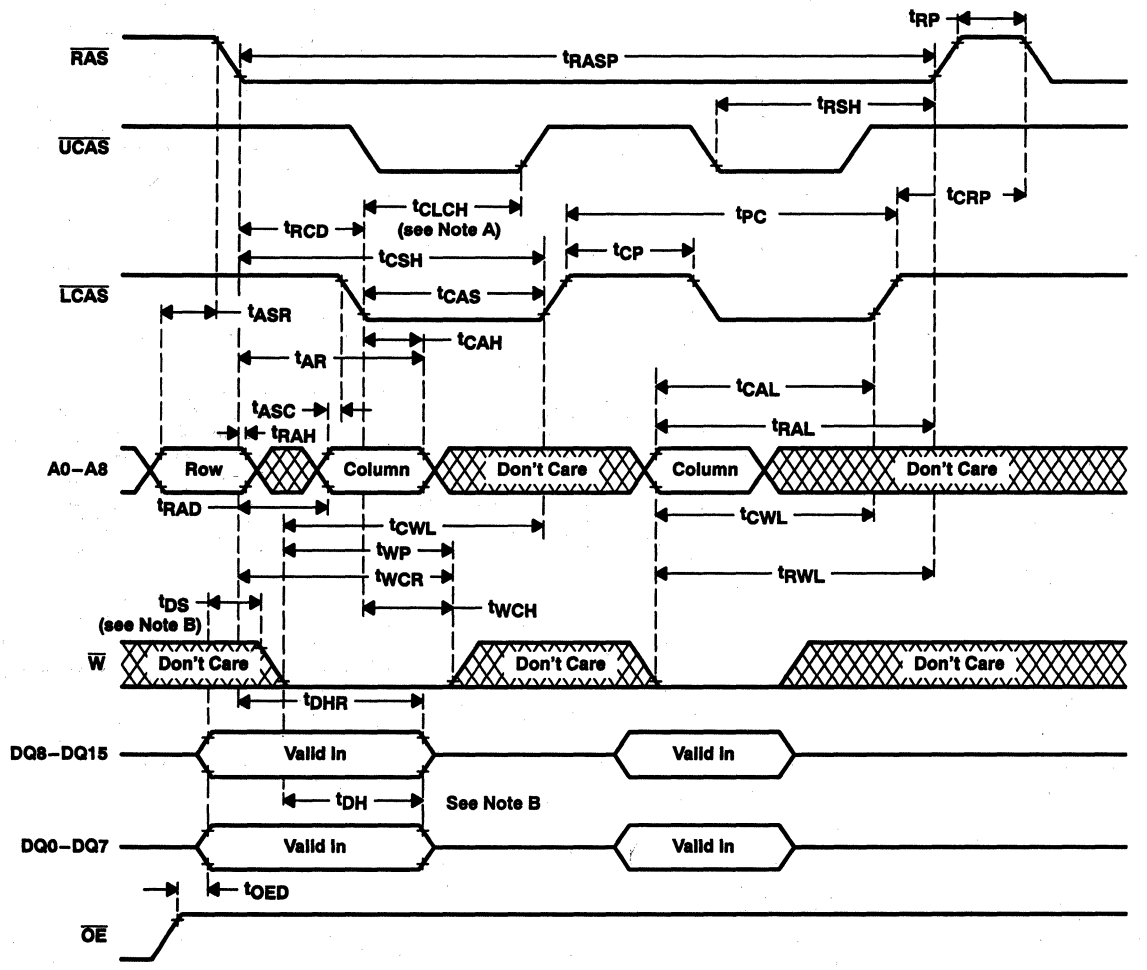
PARAMETER MEASUREMENT INFORMATION



NOTES: A. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
B. Access time is t_{CPA} or t_{AA} dependent.
C. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
D. $\overline{xCAS}$ order is arbitrary.
E. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

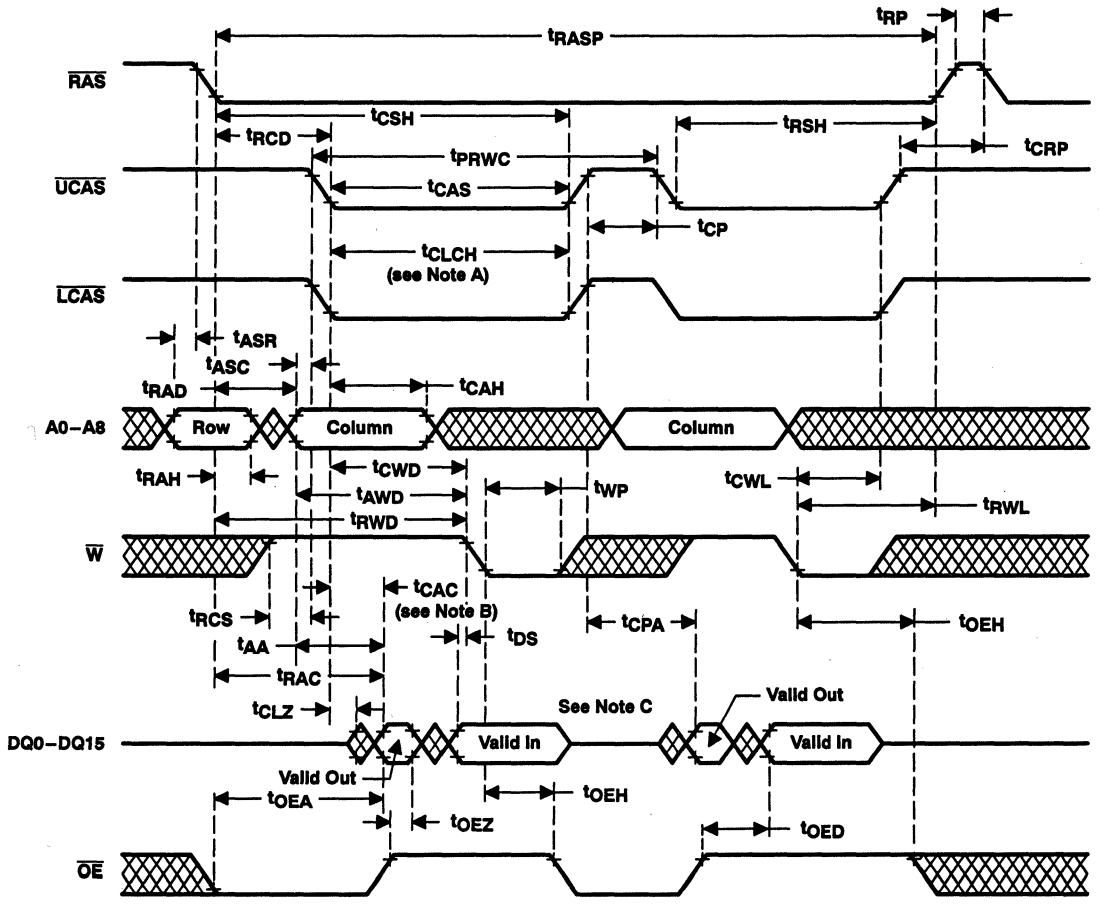
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to $\overline{xCAS}$ or $\overline{W}$, whichever occurs last
C. $\overline{xCAS}$ order is arbitrary.
D. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

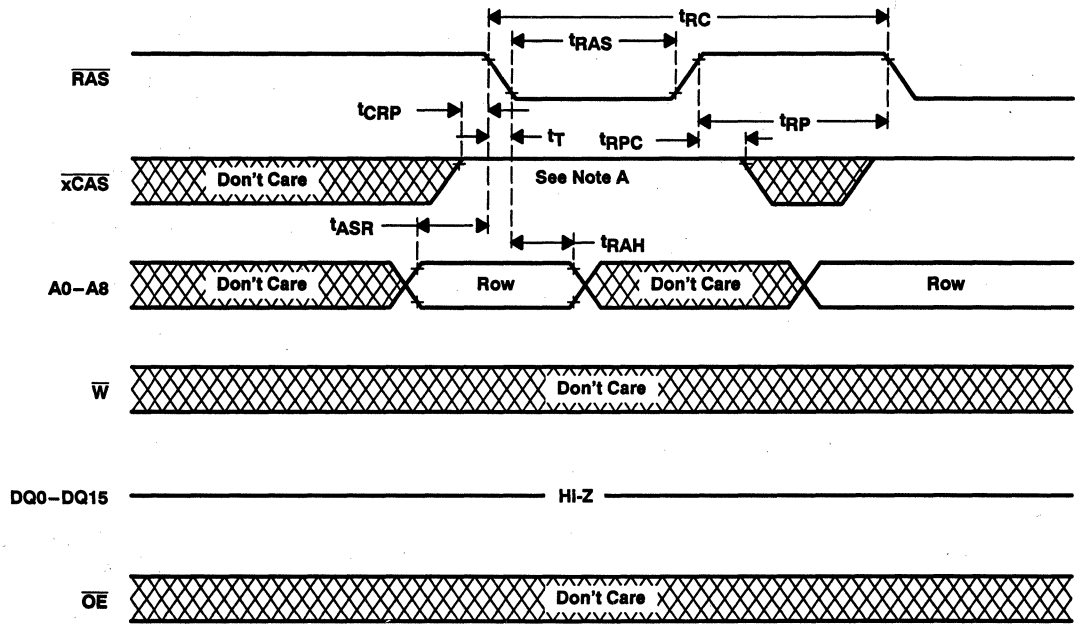
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. Output can go from the high-impedance state to an invalid data state prior to the specified access time.
D. $\overline{xCAS}$ order is arbitrary.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: All $\overline{xCAS}$ must be high.

Figure 9. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

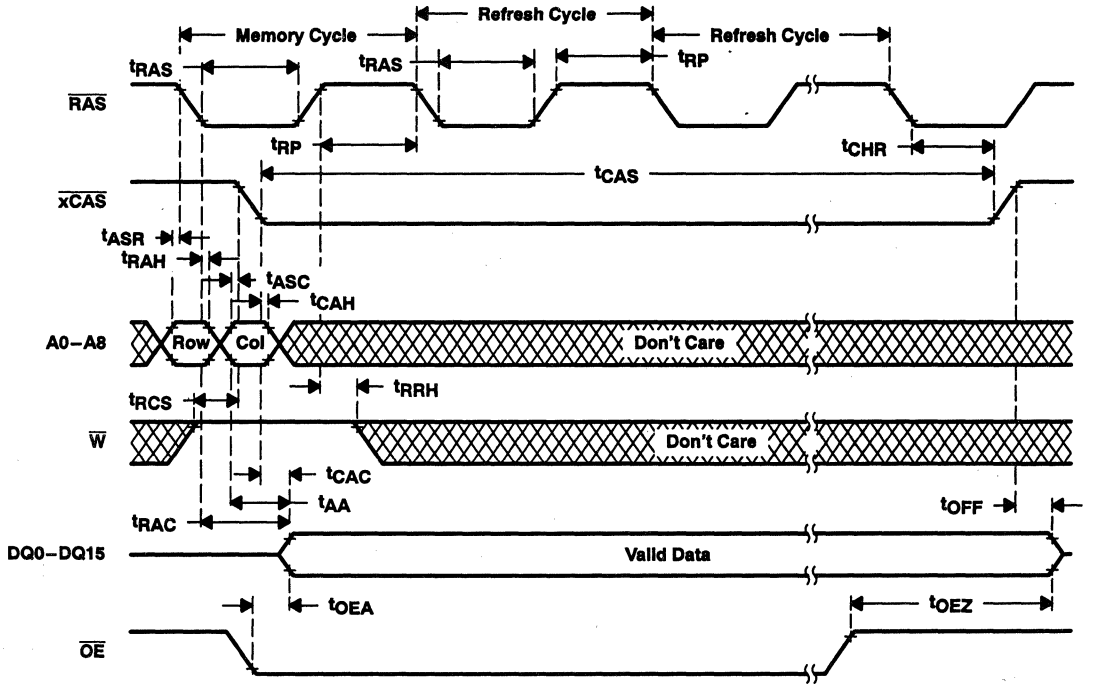
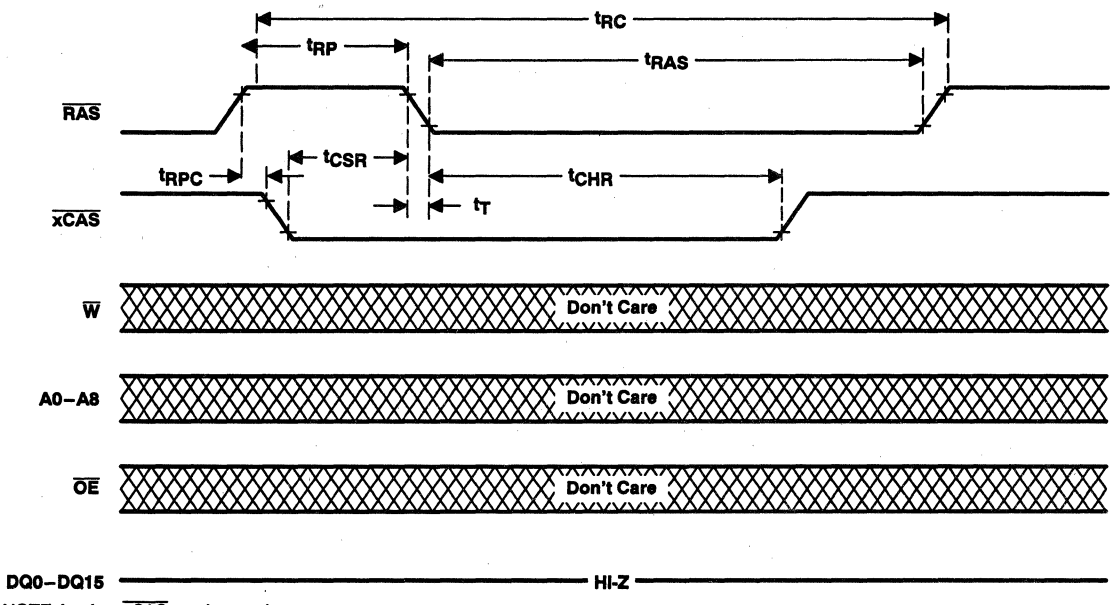


Figure 10. Hidden-Refresh-Cycle Timing

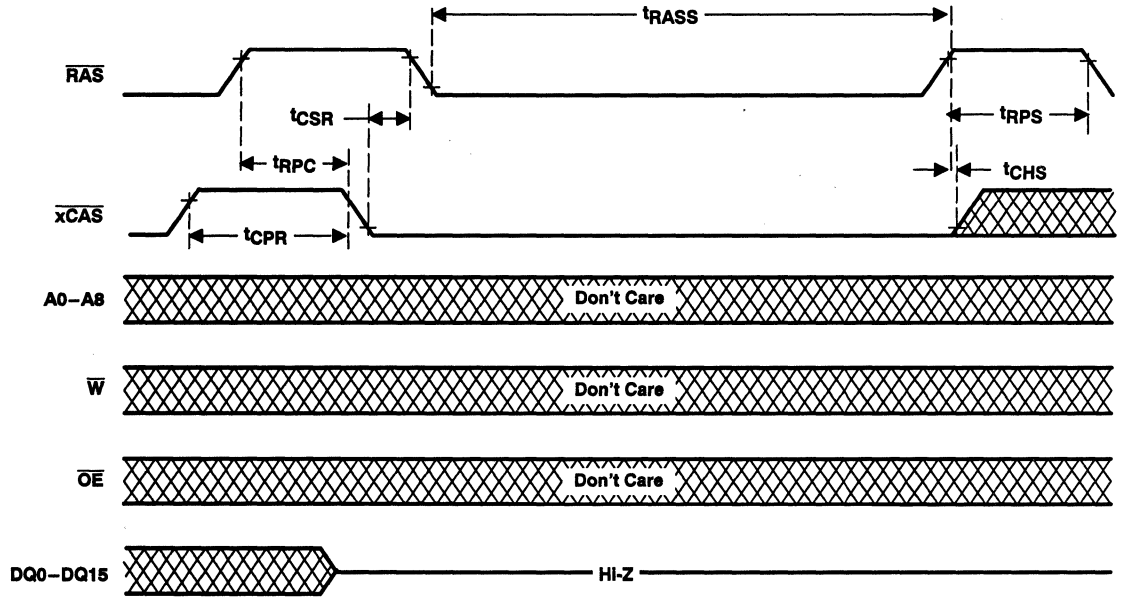
PARAMETER MEASUREMENT INFORMATION



NOTE A: Any $\overline{xCAS}$ can be used.

Figure 11. Automatic-CBR- Refresh-Cycle Timing

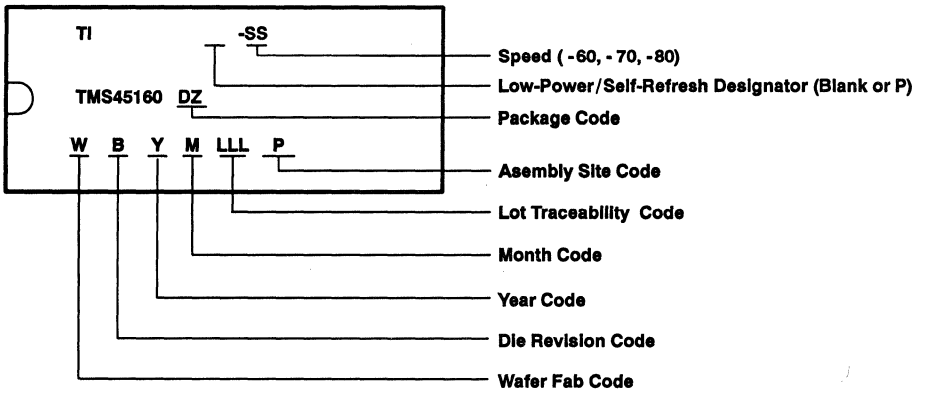
PARAMETER MEASUREMENT INFORMATION



NOTE A: Any xCAS can be used.

Figure 12. Self-Refresh-Cycle Timing

device symbolization (TMS45160 illustrated)



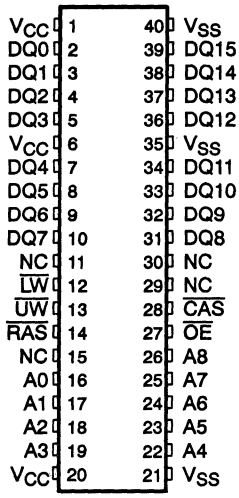
This data sheet is applicable to all TMS45165/Ps symbolized with Revision "B" and subsequent revisions as described on page 4-134.

- **Organization . . . 262144 × 16**
- **Single 5-V Supply (±10% Tolerance)**
- **Performance Ranges:**

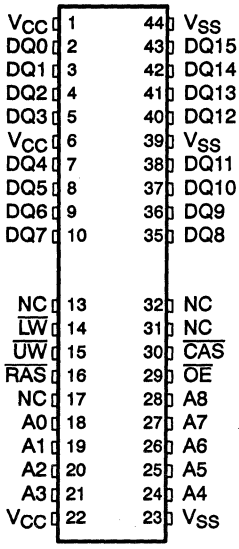
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'45165/P-70	70 ns	20 ns	35 ns	130 ns
'45165/P-80	80 ns	20 ns	40 ns	150 ns
'45165/P-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  512-Cycle Refresh in 8 ms (Max)
  64 ms for Low Power With Self-Refresh Version (TMS45165P)
- **3-State Unlatched Output**
- **Lower Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs, Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 40-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 40/44-Lead Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Low-Power With Self-Refresh**
- **Upper and Lower Byte Control During Write Operations**

DZ PACKAGE
(TOP VIEW)



DGE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ0–DQ15	Data In/Data Out
$\overline{LW}$	Lower Write Enable
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{UW}$	Upper Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

ADVANCE INFORMATION

description

The TMS45165 series are high-speed, 4194304-bit dynamic random access memories organized as 262144 words of sixteen bits each.

The TMS45165P series are high-speed, low-power with self-refresh, 4194304-bit dynamic random-access memories organized as 262144 words by sixteen bits each.

They employ state-of-the-art enhanced performance implanted CMOS (EPIC™) technology for high performance, reliability, and low power at low cost. These devices feature maximum $\overline{RAS}$ access times of 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 660 mW operating and 11 mW standby on 100 ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

EPIC is a trademark of Texas Instruments Incorporated.

description (continued)

The TMS45165 and TMS45165P are each offered in a 40-lead plastic surface mount SOJ (DZ suffix) package, and a 40/44-lead plastic surface mount TSOP (DGE suffix). These packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page-mode cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in these devices are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS45165 and TMS45165P to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as enhanced page mode. Valid column address can be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low) if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of the last $\overline{CAS}$).

address (A0–A8)

Eighteen address bits are required to decode 1 of 262144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. In the TMS45165 and TMS45165P $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffers.

write enable ($\overline{UW}$, $\overline{LW}$)

The read or write mode is selected through the upper or lower write-enable ($\overline{UW}$, $\overline{LW}$) input. $\overline{LW}$ controls DQ0–DQ7, and $\overline{UW}$ controls DQ8–DQ15. A logic high on the $\overline{UW}$ and $\overline{LW}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{UW}$ or $\overline{LW}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle permitting a write operation with $\overline{OE}$ grounded.

NOTE: Either $\overline{UW}$ or $\overline{LW}$ can be brought low in a given write cycle and only eight data bits are written into. The user can bring both $\overline{UW}$ and $\overline{LW}$ low at the same time and all 16 data bits are written into.

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$, $\overline{UW}$, or $\overline{LW}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{UW}$ or $\overline{LW}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ is already low, the data is strobed in by $\overline{UW}$ or $\overline{LW}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to high-impedance prior to impressing data on the I/O lines. The $\overline{LW}$ pin controls DQ0–DQ7. The $\overline{UW}$ pin controls DQ8–DQ15.

data out (DQ0–DQ15)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state, they remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

$\overline{RAS}$-only refresh

A refresh operation must be performed at least once every eight milliseconds (64 ms for TMS45165P) to retain data. This can be achieved by strobing each of the 512 rows (A0–A8). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh (CBR)

CBR refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 300 μA refresh current is available on the TMS45165P. Data integrity is maintained using CBR refresh with a period of 125 μs holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self-refresh (TMS45165P)

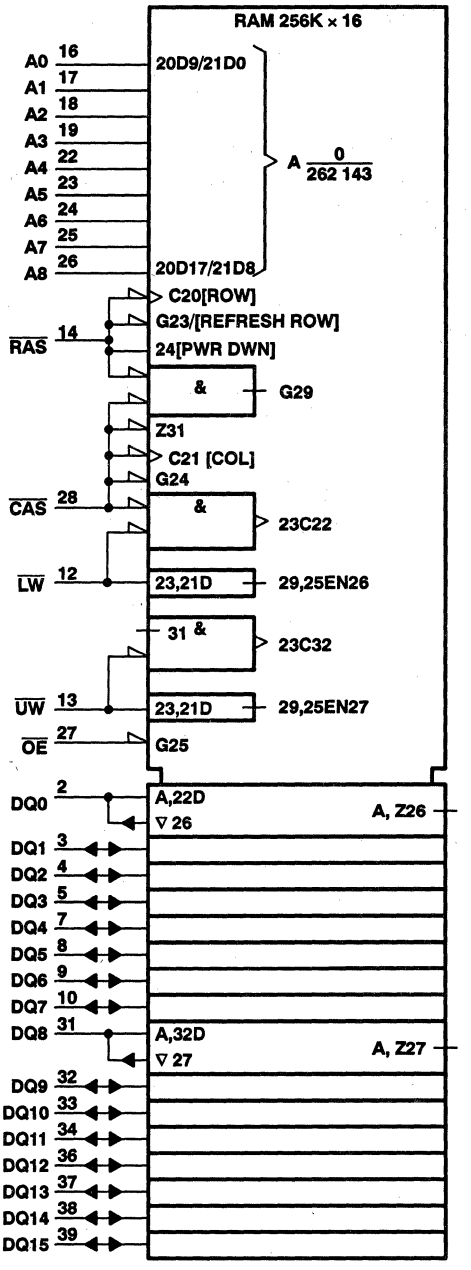
The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{RAS}$ cycles is required after power-up to the full V_{CC} level.

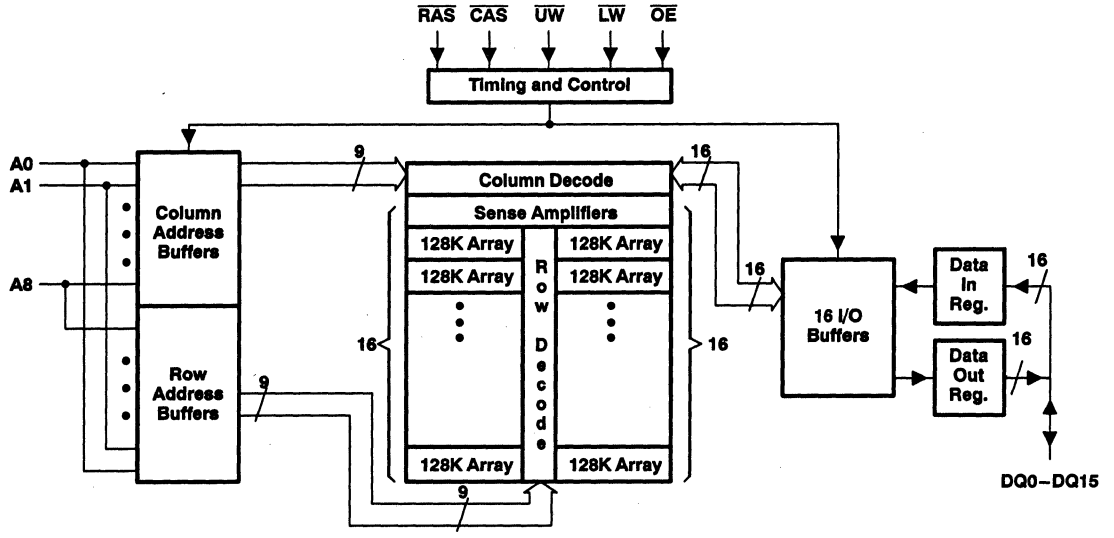
ADVANCE INFORMATION

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown correspond to the DZ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... –1 V to 7 V
Supply voltage range on V_{CC} ..... –1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'45165-70 '45165P-70 MIN	'45165-70 '45165P-70 MAX	'45165-80 '45165P-80 MIN	'45165-80 '45165P-80 MAX	'45165-10 '45165P-10 MIN	'45165-10 '45165P-10 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle			160		140		120	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL) After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS) After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'45165		1		1		1	mA
			'45165P		200		200		200	µA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, ($\overline{RAS}$ only), $\overline{RAS}$ cycling, $\overline{CAS}$ high (CBR only) $\overline{RAS}$ low after $\overline{CAS}$ low			160		140		120	mA
I_{CC4}†	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling			160		140		120	mA
I_{CC5}‡	Battery backup operating current (equivalent refresh time is 64 ms) (CBR only)	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{UW}$, $\overline{LW}$ and $\overline{OE}$=V_{IH}, Address and data stable			300		300		300	µA
I_{CC6}†‡	Self refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			200		200		200	µA

† Measured with outputs open
‡ For TMS45165P only
NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A8		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_O	Output capacitance		7	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'45165-70 '46165P-70		'45165-80 '46165P-80		'45165-10 '46165P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		20		20		25	ns
t_{AA}	Access time from column address		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		20		20		25	ns
t_{CPA}	Access time from column precharge		40		45		50	ns
t_{CLZ}	$\overline{CAS}$ low to output in the low-impedance state	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	20	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	20	0	20	0	25	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		'45165-70 '45165P-70		'45165-80 '45165P-80		'45165-10 '45165P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read (see Note 8)	130		150		180		ns
t_{WC}	Cycle time, write	130		150		180		ns
t_{RWC}	Cycle time, read-modify-write	185		205		245		ns
t_{PC}	Cycle time, page-mode read or write (see Note 9)	45		50		55		ns
t_{PRWC}	Cycle time, page-mode read-modify-write	90		105		120		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low (see Note 11)	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low (see Note 11)	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	20	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		70		ns
t_{WP}	Pulse duration, write	15		15		20		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{xW}$ low (see Note12)	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{xW}$ low before $\overline{CAS}$ high	20		20		25		ns
t_{RWL}	Setup time, $\overline{xW}$ low before $\overline{RAS}$ high	20		20		25		ns
t_{WCS}	Setup time, $\overline{xW}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns

NOTES: 7. Timing measurements are referenced to V_{IL} max and V_{IH} min.
8. All cycle times assume t_T = 5 ns.
9. $t_{PC} > t_{CP}$ min + t_{CAS} min + $2t_T$.
10. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this can require additional $\overline{CAS}$ low time (t_{CAS}).
11. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this can require additional $\overline{RAS}$ low time (t_{RAS}).
12. Later of $\overline{CAS}$ or $\overline{xW}$ in write operations

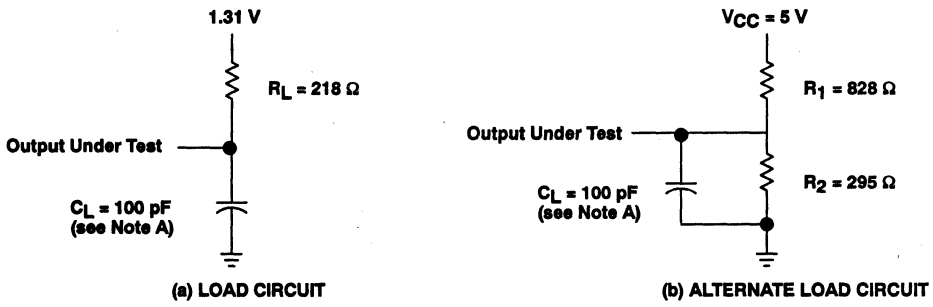
timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 7) (concluded)

PARAMETER		'45165-70 '45165P-70		'45165-80 '45165P-80		'45165-10 '45165P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Hold time, column address after $\overline{CAS}$ low (see Note 12)	15		15		20		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 13)	35		35		45		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low (see Note 12)	15		15		20		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 13)	35		35		45		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		15		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 14)	0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 14)	0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low (early-write operation only)	15		15		20		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low (see Note 13)	35		35		45		ns
t_{OEH}	Hold time, $\overline{OE}$ command	20		20		25		ns
t_{AWD}	Delay time, column address to $\overline{xW}$ low (see Note 15)	65		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{xW}$ low (see Note 16)	50		50		60		ns
t_{OED}	Delay time, $\overline{OE}$ high before data at DQ	20		20		25		ns
t_{ROH}	Delay time, $\overline{OE}$ low to $\overline{RAS}$ high	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 16)	15	35	15	40	20	55	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 16)	20	50	20	60	25	75	ns
t_{RPC}	Delay time, RAS high to CAS low (CBR refresh only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	20		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{xW}$ low (see Note 15)	100		110		135		ns
t_{CPR}	$\overline{CAS}$ precharge before self refresh	0		0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	130		150		180		ns
t_{RASS}	Self-refresh entry from $\overline{RAS}$ low	100		100		100		µs
t_{REF}	Refresh time interval (TMS45165 only)		8		8		8	ms
t_{REF}	Refresh time interval, low power (TMS45165P only)		64		64		64	ms
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high	–50		–50		–50		ns
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 7. Timing measurements are referenced to V_{IL} max and V_{IH} min.
12. Later of $\overline{CAS}$ or $\overline{xW}$ in write operations
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. Read-modify-write operation only
16. Maximum value specified only to assure access time.

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

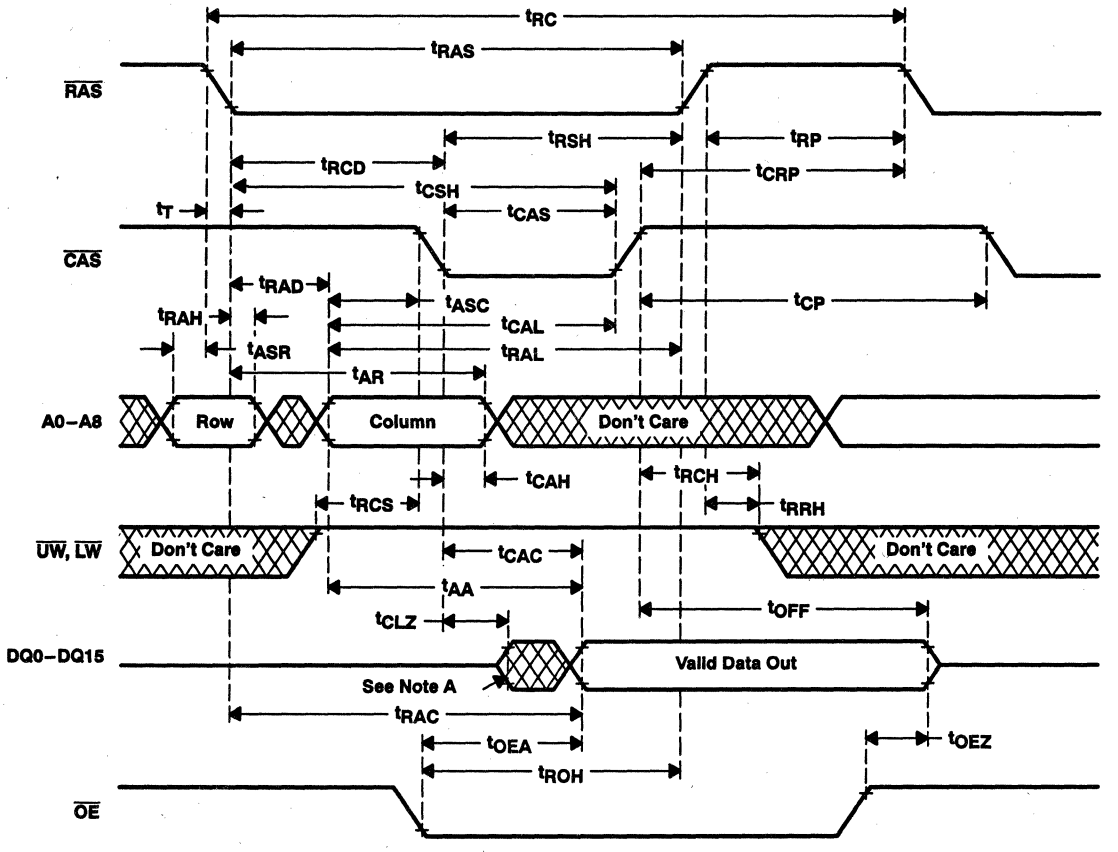


NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

ADVANCE INFORMATION

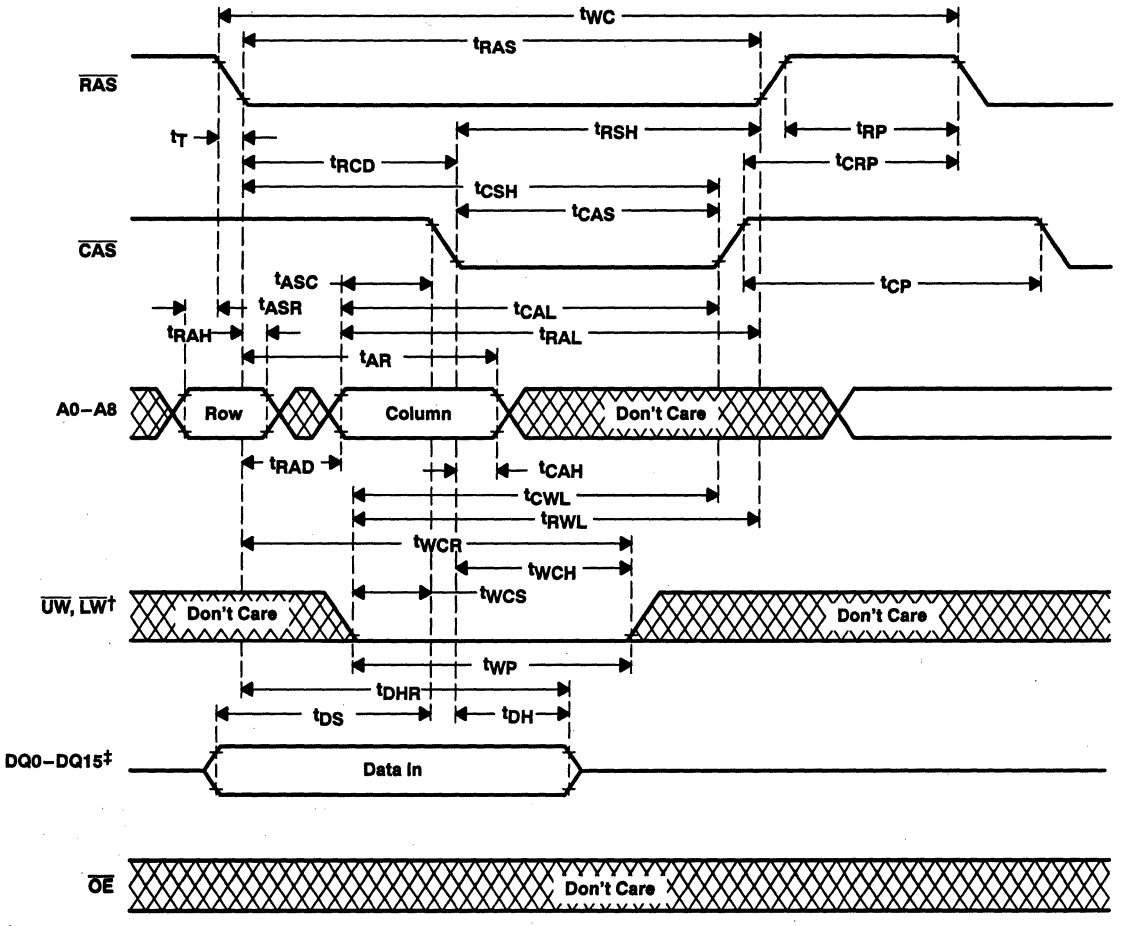
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

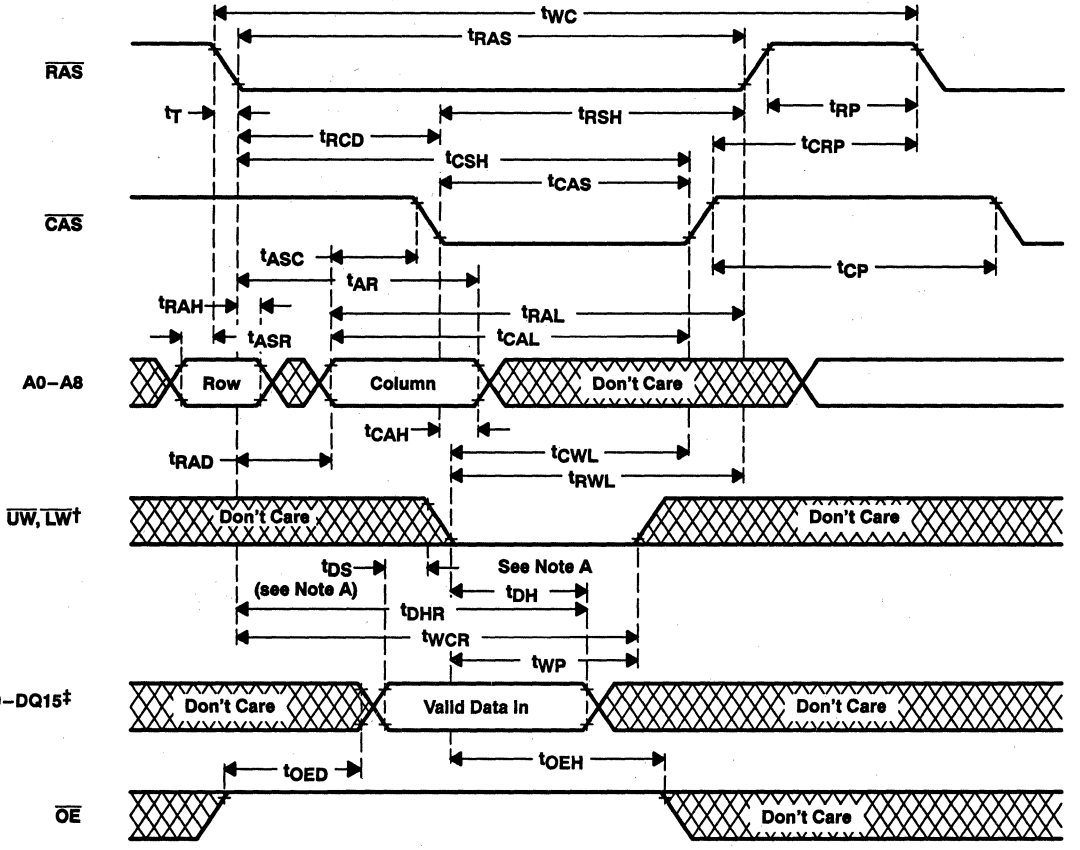


† Either $\overline{UW}$ or $\overline{LW}$ can be brought low and the user can write into eight DQ locations, or $\overline{UW}$ and $\overline{LW}$ can be brought low at the same time and all 16 DQ locations are written into.
‡ All DQ pins remain in the high-impedance state for an early-write cycle.

Figure 3. Early-Write-Cycle Timing

ADVANCE INFORMATION

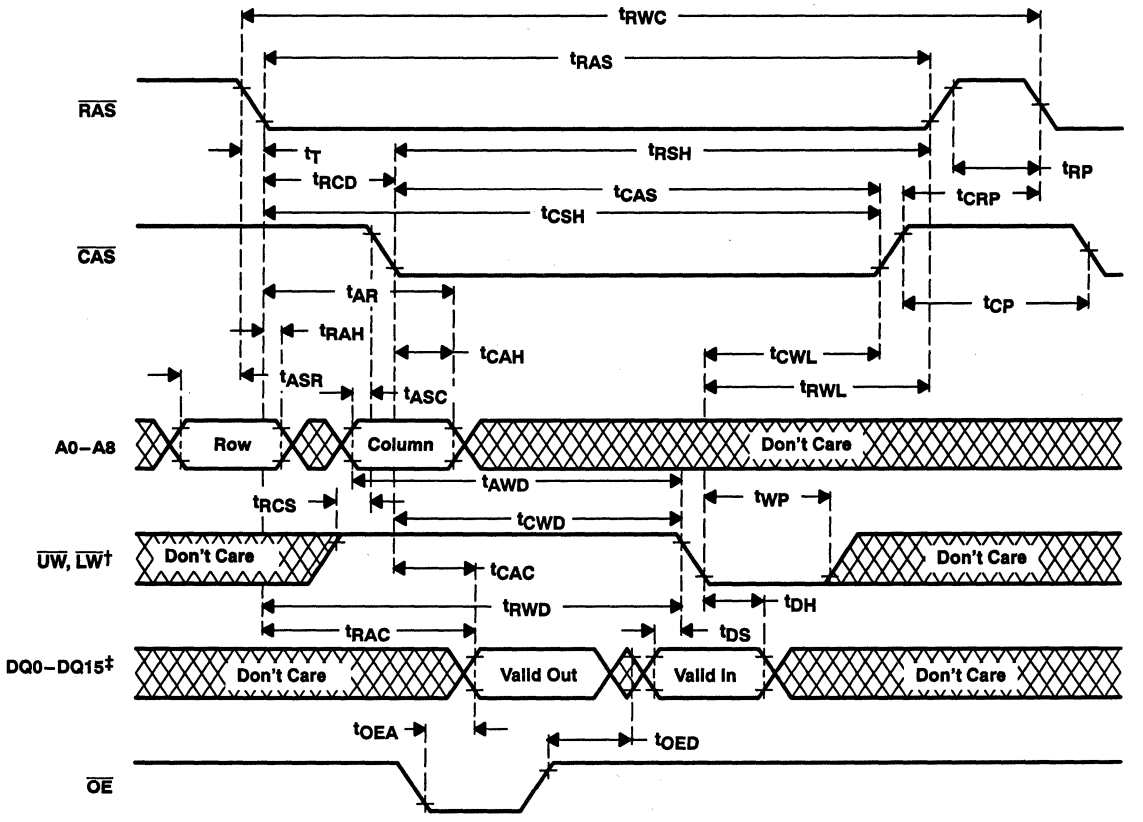
PARAMETER MEASUREMENT INFORMATION



† Either $\overline{UW}$ or $\overline{LW}$ can be brought low and the user can write into eight DQ locations, or $\overline{UW}$ and $\overline{LW}$ can be brought low at the same time and all 16 DQ locations are written into.
‡ All DQ pins remain in the high-impedance state while $\overline{OE}$ is high.
NOTE A: Later of $\overline{CAS}$ or $\overline{xW}$ in write operations.

Figure 4. Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

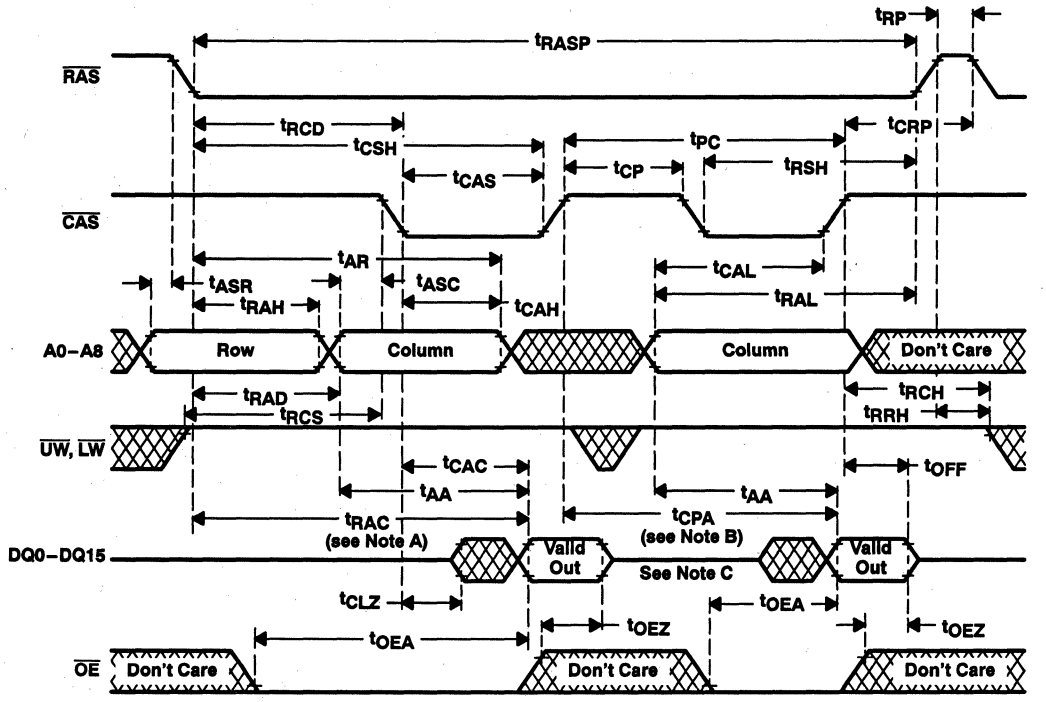


† Either $\overline{UW}$ or $\overline{LW}$ can be brought low and the user can write into eight DQ locations, or $\overline{UW}$ and $\overline{LW}$ can be brought low at the same time and all 16 DQ locations are written into.
‡ All DQ pins remain in the high-impedance state for an early-write cycle.

Figure 5. Read-Modify-Write-Cycle Timing

ADVANCE INFORMATION

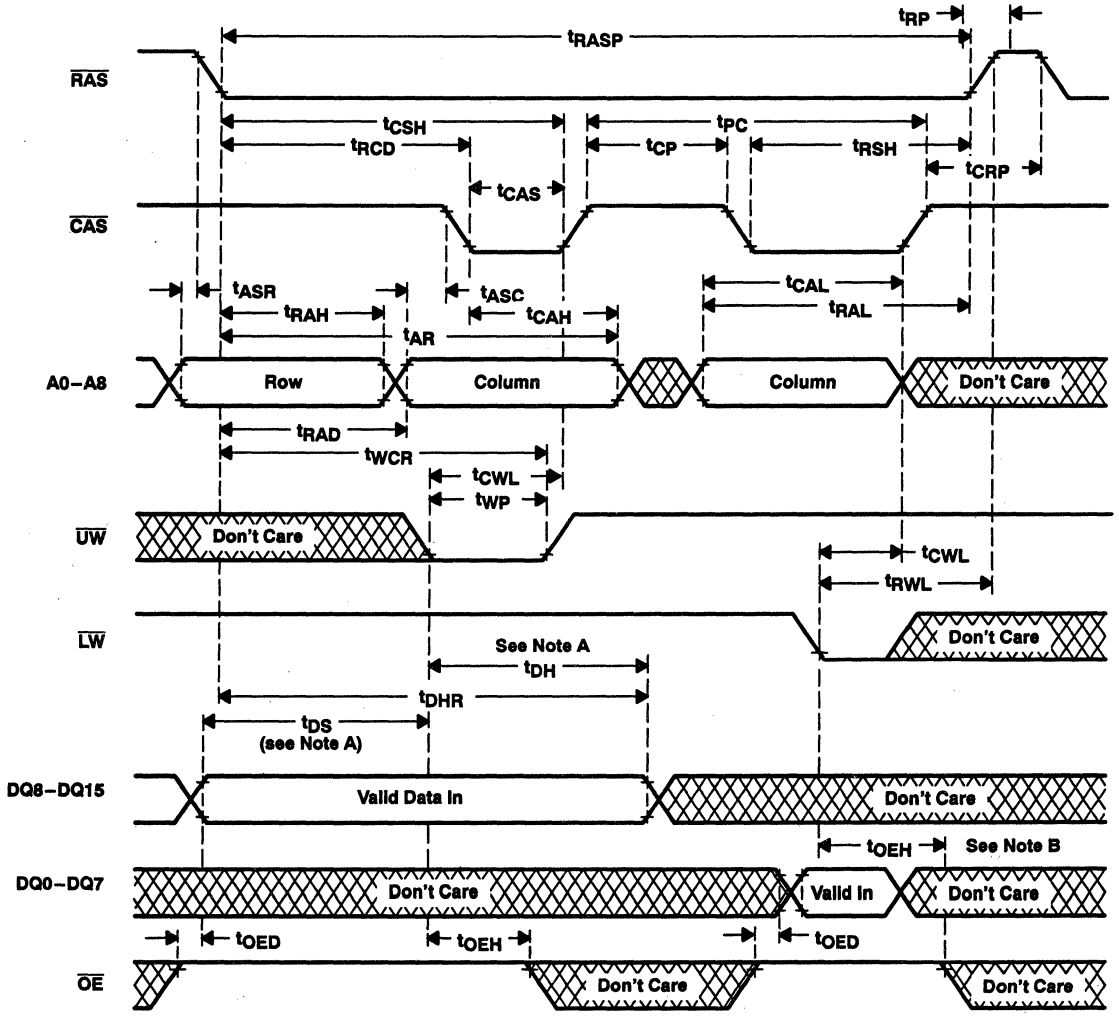
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.
C. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

Figure 6. Enhanced Page-Mode Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

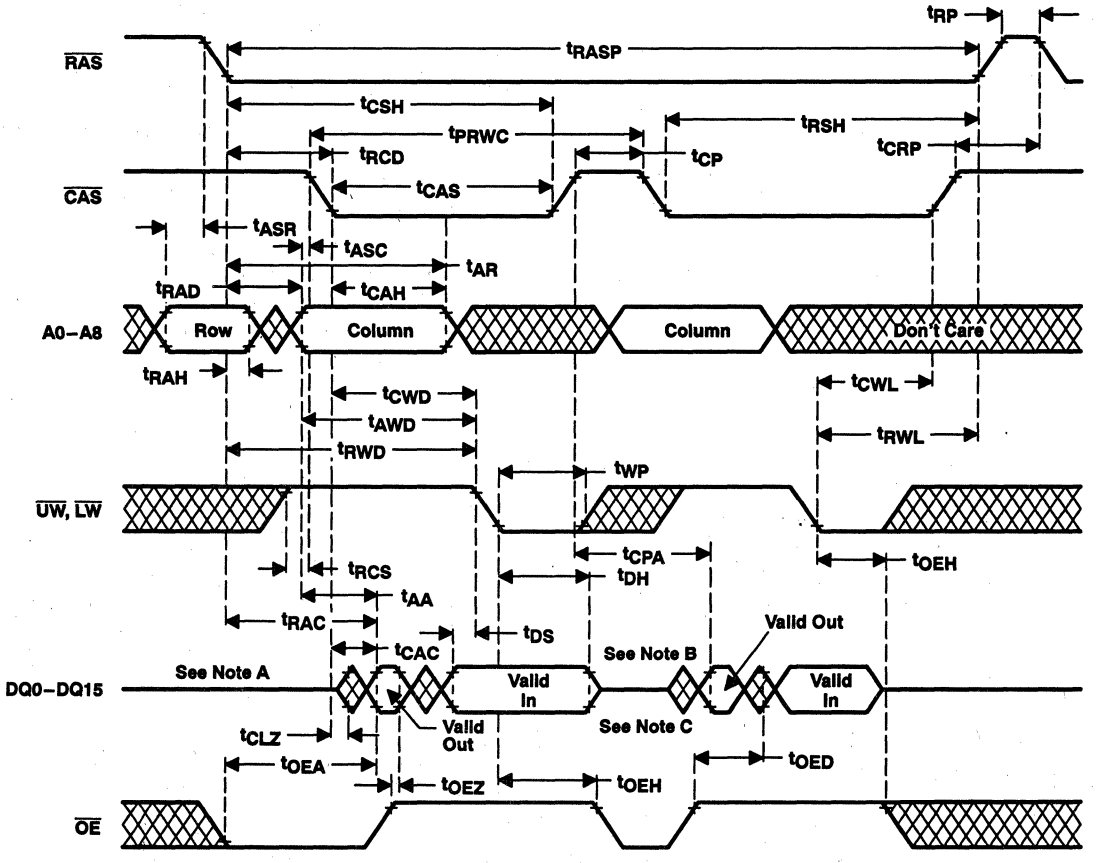


NOTES: A. Later of $\overline{CAS}$ or $\overline{xW}$ in write operations.
B. A read-cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read- or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.
C. Access time is t_{CPA} or t_{AA} dependent.

Figure 8. Enhanced Page-Mode Read-Modify-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

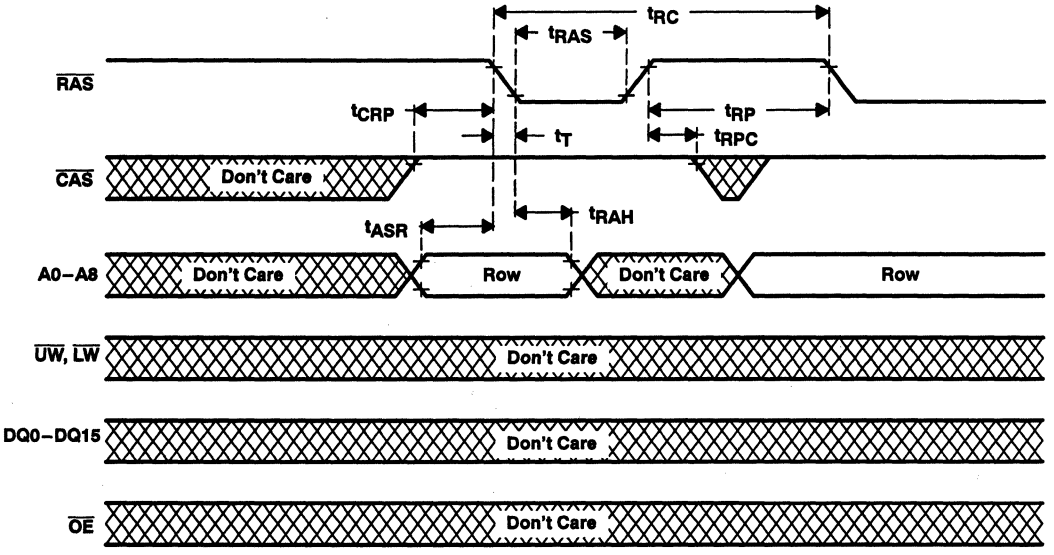


Figure 9. RAS-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

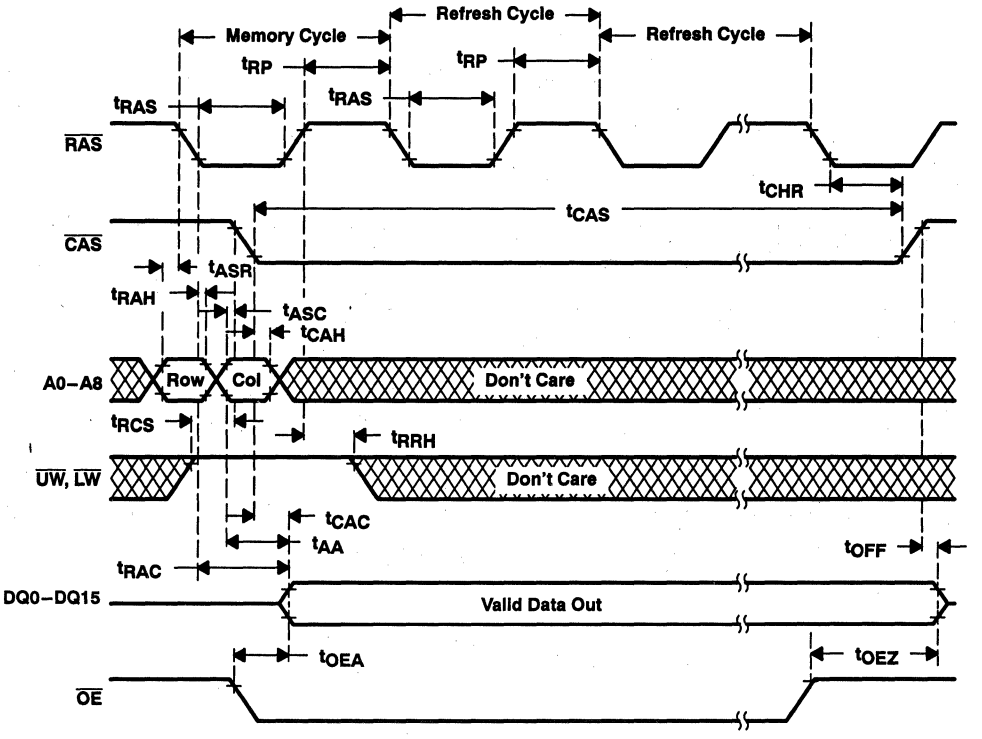
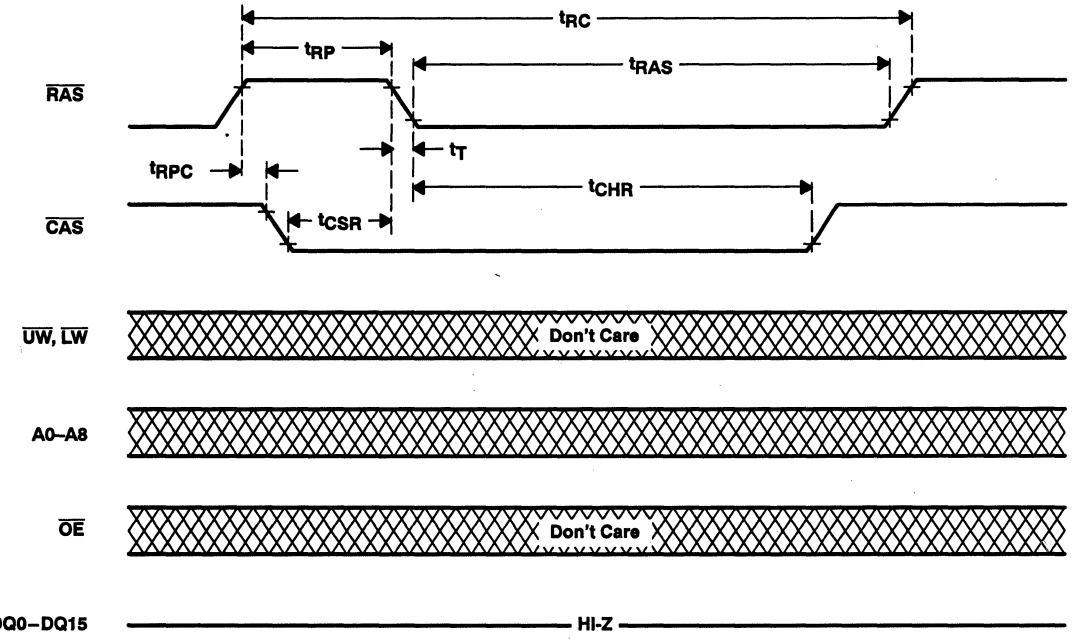


Figure 10. Hidden-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: 512 CBR cycles must be used for CBR counter test.

Figure 11. Automatic-CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

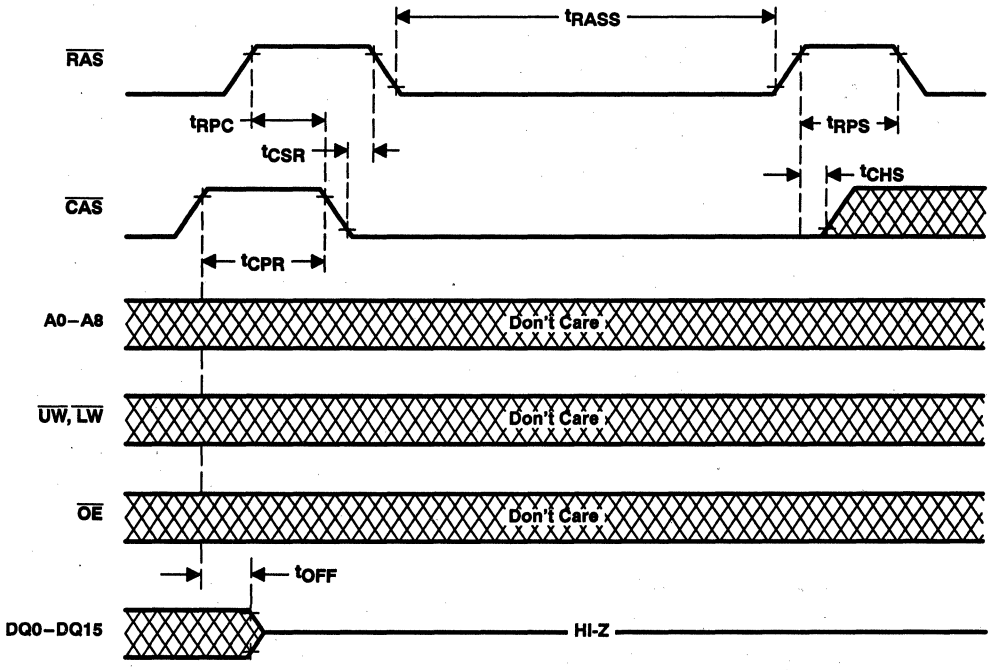
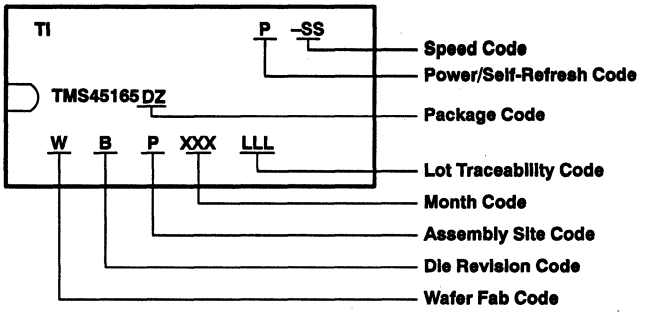


Figure 12. Self-Refresh-Cycle Timing

device symbolization



ADVANCE INFORMATION

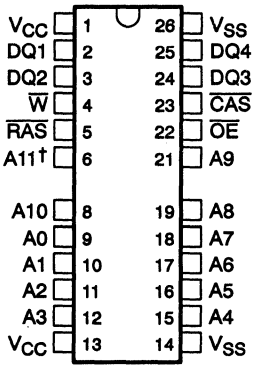
Electrical characteristics for TMS416400/P and TMS417400/P is Production Data. Electrical characteristics for TMS426400/P and TMS427400/P is Product Preview only.

- **Organization . . . 4194304 × 4**
- **Single 5 V Power Supply for TMS41x400/P (±10% Tolerance)**
- **Single 3.3 V Power Supply for TMS42x400/P (±0.3 V Tolerance)**
- **Performance Ranges:**

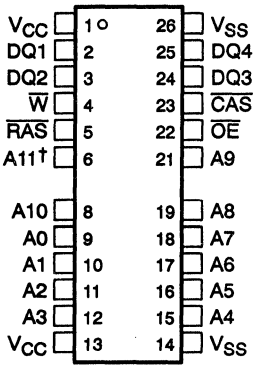
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'4xx400/P-60	60 ns	15 ns	30 ns	110 ns
'4xx400/P-70	70 ns	18 ns	35 ns	130 ns
'4xx400/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page-Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ ($\overline{CBR}$) Refresh**
- **Long Refresh Period and Self-Refresh Option (TMS4xx400P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **High-Reliability Plastic 24/26-Lead 300-Mil-Wide Surface-Mount Small-Outline J-Lead (SOJ) Package and 24/26-Lead Surface-Mount Thin Small-Outline Package (TSOP)**
- **Operating Free-Air Temperature Range: 0°C to 70°C**
- **EPIC™ (Enhanced Performance Implanted CMOS) Technology**

DJ PACKAGE (TOP VIEW)



DGA PACKAGE (TOP VIEW)



PIN NOMENCLATURE	
A0–A11†	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
NC	No Internal Connection
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V or 3.3-V Supply‡
V_{SS}	Ground
$\overline{W}$	Write Enable

† A11 is NC for TMS4x7400/P.
‡ See Table 1.

description

The TMS4xx400 is a set of high-speed, 16777216-bit dynamic random-access memories organized as 4194304 words of 4 bits each. The TMS4xx400P series are high-speed, low-power, self-refresh, 16777216-bit dynamic random-access memories organized as 4194304 words of 4 bits each. The TMS4xx400 and TMS4xx400P employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power.

AVAILABLE OPTIONS

DEVICE	POWER SUPPLY	SELF REFRESH BATTERY BACKUP	REFRESH CYCLES
TMS416400	5 V	—	4096 in 64 ms
TMS416400P	5 V	Yes	4096 in 128 ms
TMS417400	5 V	—	2048 in 32 ms
TMS417400P	5 V	Yes	2048 in 128 ms
TMS426400	3.3 V	—	4096 in 64 ms
TMS426400P	3.3 V	Yes	4096 in 128 ms
TMS427400	3.3 V	—	2048 in 32 ms
TMS427400P	3.3 V	Yes	2048 in 128 ms

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

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description (continued)

The TMS4xx400 and TMS4xx400P are each offered in a 24/26-lead plastic surface-mount TSOP (DGA suffix) package and a 24/26-lead plastic surface-mount SOJ (DJ suffix) package. These packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP}, the maximum $\overline{RAS}$ low time.

Unlike conventional page-mode DRAMs, the column-address buffers in these devices are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses and enables the output. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low) if t_{AA} max (access time from column address) and t_{RAC} have been satisfied. In the event that column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CPA} or t_{CAC}.

address: A0–A11 (TMS4x6400/P) and A0–A10 (TMS4x7400/P)

Twenty-two address bits are required to decode 1 of 4194304 storage cell locations. For the TMS4x6400 and TMS4x6400P, 12 row-address bits are set up on A0 through A11 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Ten column-address bits are set up on A0 through A9. For TMS4x7400 and TMS4x7400P, 11 row-address bits are set up on inputs A0 through A10 and latched onto the chip by $\overline{RAS}$. Eleven column-address bits are set up on A0 through A10. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable because it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffers and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode, and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{OE}$ grounded.

data in (DQ0–DQ3)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$, and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ is already low, and the data is strobed in by $\overline{W}$ with setup and hold time referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

data out (DQ0–DQ3)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{CAS}$) as long as t_{RAC} and t_{AA} are satisfied.

$\overline{\text{RAS}}$-only refresh

TMS4x6400, TMS4x6400P

A refresh operation must be performed at least once every 64 ms (128 ms for TMS4x6400P) to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding $\overline{\text{CAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh.

TMS4x7400, TMS4x7400P

A refresh operation must be performed at least once every 32 ms (128 ms for TMS4x7400P) to retain data. This can be achieved by strobing each of the 2048 rows (A0–A10). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding $\overline{\text{CAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{\text{CAS}}$ at V_{IL} after a read operation and cycling $\overline{\text{RAS}}$ after a specified precharge period, similar to a $\overline{\text{RAS}}$-only refresh cycle. The external address is ignored, and the refresh address is generated internally.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ (CBR) refresh

CBR refresh is utilized by bringing $\overline{\text{CAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CSR}) and holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored, and the refresh address is generated internally.

battery-backup refresh

TMS4x6400P

A low-power battery-backup refresh mode that requires less than 500 µA (5 V) or 350 µA (3.3 V) refresh current is available on the TMS4x6400P. Data integrity is maintained using CBR refresh with a period of 31.25 µs while holding $\overline{\text{RAS}}$ low for less than 1 µs. To minimize current consumption, all input levels must be at CMOS levels (V_{IL} < 0.2 V, V_{IH} > V_{CC} – 0.2 V).

TMS4x7400P

A low-power battery-backup refresh mode that requires less than 500 µA (5 V) or 350 µA (3.3 V) refresh current is available on the TMS4x7400P. Data integrity is maintained using CBR refresh with a period of 62.5 µs while holding $\overline{\text{RAS}}$ low for less than 1 µs. To minimize current consumption, all input levels must be at CMOS levels (V_{IL} < 0.2 V, V_{IH} > V_{CC} – 0.2 V).

self refresh (TMS4xx400P)

The self-refresh mode is entered by dropping $\overline{\text{CAS}}$ low prior to $\overline{\text{RAS}}$ going low. Then $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ are both held low for a minimum of 100 µs. The chip is then refreshed internally by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

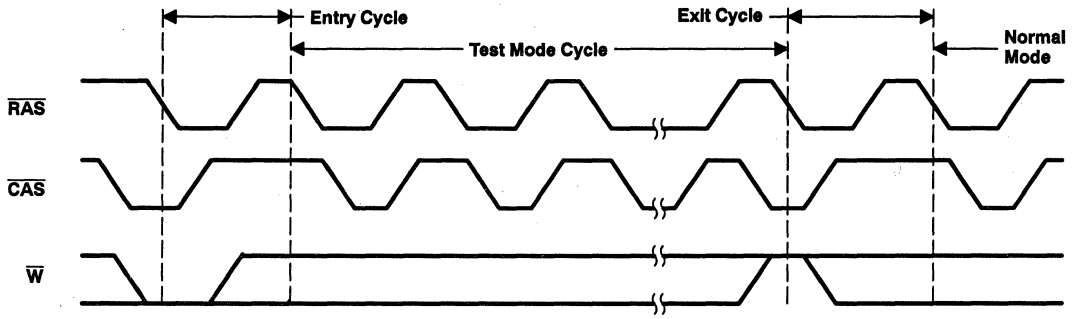
power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level. These eight initialization cycles must include at least one refresh ($\overline{\text{RAS}}$-only or CBR) cycle.

test mode

The test mode is initiated with a CBR-refresh cycle while simultaneously holding the $\overline{W}$ input low. The entry cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in the test mode, any data sequence can be performed. The device exits test mode if a CBR refresh cycle with $\overline{W}$ held high or a $\overline{RAS}$-only refresh cycle is performed.

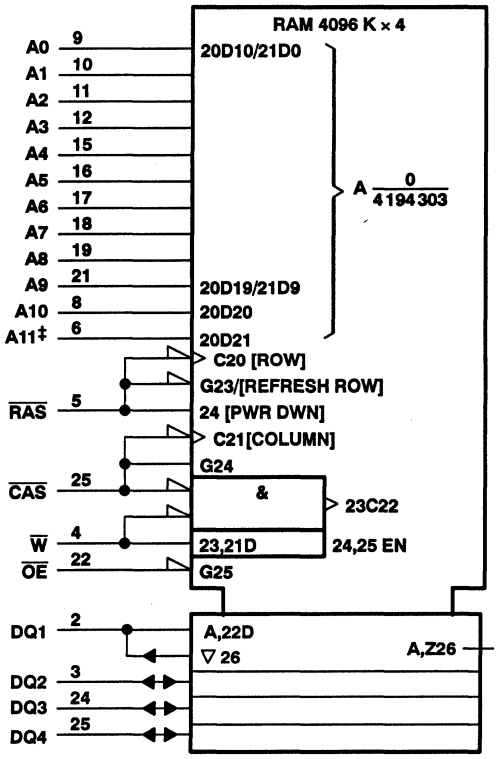
In the test mode, the device is configured as 1024K bits × 4 bits for each DQ. Each DQ pin has a separate 4-bit parallel read and write data bus that ignores column addresses A0 and A1. During a read cycle, the four internal bits are compared for each DQ pin separately. If the four bits agree, DQ goes high; if not, DQ goes low. During a write cycle, the data states of all four DQs must be the same to ensure proper function of the test mode. Test time is reduced by a factor of four for this series.



NOTE A: The states of $\overline{W}$, data in, and address are defined by the type of cycle used during test mode.

Figure 1. Test-Mode Cycle

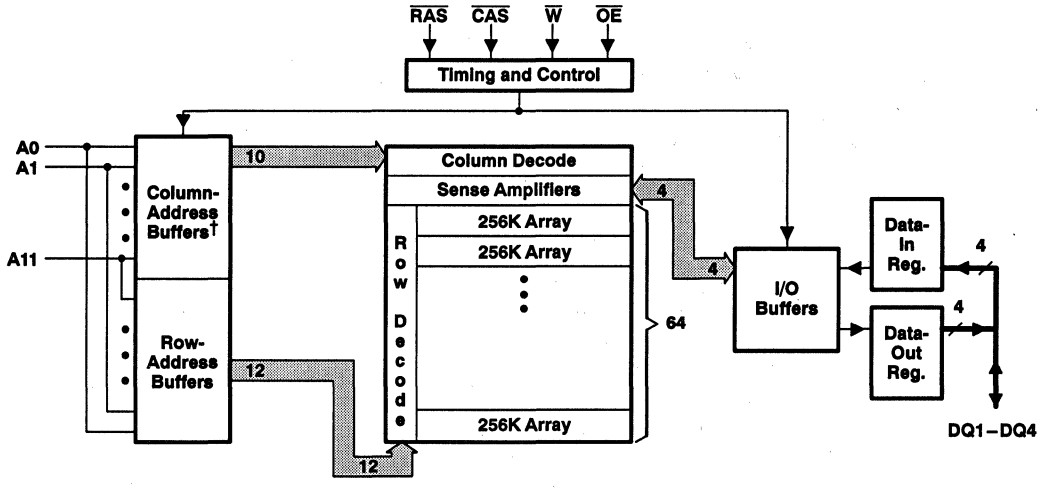
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 647-12.
‡ A11 is NC for TMS4x7400 and TMS4x7400P.

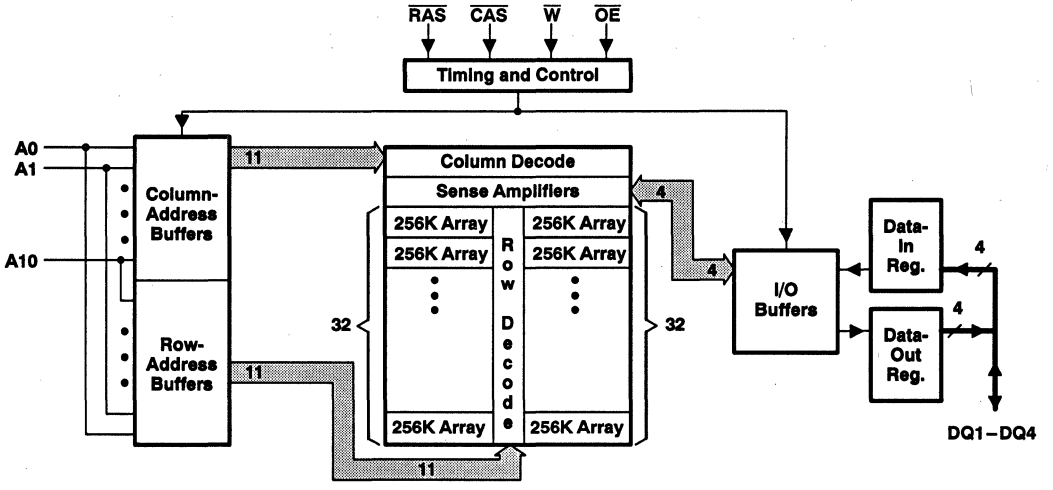
functional block diagram

TMS4x6400/P



† Column addresses A10 and A11 are not used.

TMS4x7400/P



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: TMS41x400, TMS41x400P ..... –1 V to 7 V
TMS42x400, TMS42x400P ..... –0.5 V to 4.6 V
Voltage range on any pin (see Note 1): TMS41x400, TMS41x400P ..... –1 V to 7 V
TMS42x400, TMS42x400P ..... –0.5 V to 4.6 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		TMS41x400			TMS42x400			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	3	3.3	3.6	V
V_{SS}	Supply voltage		0			0		V
V_{IH}	High-level input voltage	2.4		6.5	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	–0.3		0.8	V
T_A	Operating free-air temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TMS416400/P

PARAMETER		TEST CONDITIONS†		'416400-60 '416400P-60		'416400-70 '416400P-70		'416400-80 '416400P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle			80		70		60	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'416400		1		1		1	mA
			'416400P		500		500		500	µA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			80		70		60	mA
I_{CC4}‡¶	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling			70		60		50	mA
I_{CC6}#	Self-refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			500		500		500	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms); CBR only	t_{RC} = 31.25 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			500		500		500	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}
# For TMS416400P only

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

TMS417400/P

PARAMETER		TEST CONDITIONS†		'417400-60 '417400P-60		'417400-70 '417400P-70		'417400-80 '417400P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle			110		100		90	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'417400		1		1		1	mA
			'417400P		500		500		500	µA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			110		100		90	mA
I_{CC4}‡¶	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling			70		60		50	mA
I_{CC6}#	Self-refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			500		500		500	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms); CBR only	t_{RC} = 62.5 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			500		500		500	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}
# For TMS417400P only

electrical characteristics over recommended ranges of supply voltage and operating free-air conditions (unless otherwise noted) (continued)

TMS426400/P

PARAMETER		TEST CONDITIONS†		'426400-60 '426400P-60 MIN	'426400-60 '426400P-60 MAX	'426400-70 '426400P-70 MIN	'426400-70 '426400P-70 MAX	'426400-80 '426400P-80 MIN	'426400-80 '426400P-80 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 3.6 V, Minimum cycle			70		60		50	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			1		1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'426400		500		500		500	µA
			'426400P		200		200		200	µA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only refresh), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			70		60		50	mA
I_{CC4}‡¶	Average page current	V_{CC} = 3.6 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling			60		50		40	mA
I_{CC6}#	Self-refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			250		250		250	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms), CBR only	t_{RC} = 31.25 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}
# For TMS426400P only

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and operating free-air conditions (unless otherwise noted) (continued)

TMS427400/P

PARAMETER		TEST CONDITIONS†		'427400-60 '427400P-60 MIN	'427400-60 '427400P-60 MAX	'427400-70 '427400P-70 MIN	'427400-70 '427400P-70 MAX	'427400-80 '427400P-80 MIN	'427400-80 '427400P-80 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 3.6 V, Minimum cycle			100		90		80	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			1		1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'427400		500		500		500	µA
			'427400P		200		200		200	µA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only refresh), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			100		90		80	mA
I_{CC4}‡¶	Average page current	V_{CC} = 3.6 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling			60		50		40	mA
I_{CC6}#	Self-refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			250		250		250	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms), CBR only	t_{RC} = 62.5 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}
# For TMS427400P only

PRODUCT PREVIEW

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

	PARAMETER	MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A11		5	pF
$C_{i(\overline{OE})}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(\overline{W})}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance		7	pF

NOTE 3: V_{CC} = NOM supply voltage ±10%, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	'4xx400-60 '4xx400P-60		'4xx400-70 '4xx400P-70		'4xx400-80 '4xx400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 4)		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low (see Note 4)		15		18		20	ns
t_{CPA}	Access time from column precharge (see Note 4)		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low (see Note 4)		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low (see Note 4)		15		18		20	ns
t_{CLZ}	Delay time, $\overline{CAS}$ low to output in low-impedance state	0		0		0		ns
t_{OH}	Output data hold time (from $\overline{CAS}$)	3		3		3		ns
t_{OHO}	Output data hold time (from $\overline{OE}$)	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 5)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 5)	0	15	0	18	0	20	ns

NOTES: 4. Access times for TMS42x400 measured with output reference levels of V_{OH} = 2 V and V_{OL} = 0.8 V.
5. t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4xx400-60 '4xx400P-60		'4xx400-70 '4xx400P-70		'4xx400-80 '4xx400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read (see Note 6)	110		130		150		ns
t_{WC}	Cycle time, write (see Note 6)	110		130		150		ns
t_{RWC}	Cycle time, read-write (see Note 6)	155		181		205		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 6 and 7)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-write (see Note 6)	85		96		105		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 8)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 8)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 9)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 10)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{WTS}	Setup time, $\overline{W}$ low before $\overline{RAS}$ low (test mode only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Hold time, data (see Note 10)	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 11)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 11)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low (early-write operation only)	10		15		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{OEH}	Hold time, $\overline{OE}$ command	15		18		20		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	10		10		10		ns
t_{CHS}	Hold time, $\overline{CAS}$ low after $\overline{RAS}$ high (self refresh)	–50		–50		–50		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{WTH}	Hold time, $\overline{W}$ low after $\overline{RAS}$ low (test mode only)	10		10		10		ns

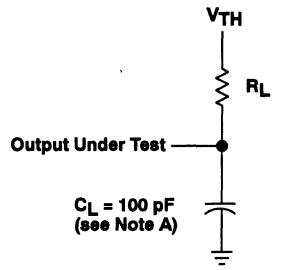
NOTES: 6. All cycle times assume t_T = 5 ns.
7. To assure t_{PC} min, t_{ASC} should be ≥ to t_{CP}.
8. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
9. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

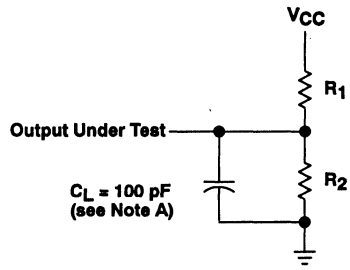
			'4xx400-60 '4xx400P-60		'4xx400-70 '4xx400P-70		'4xx400-80 '4xx400P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)		55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)		10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)		5		5		5		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-write operation only)		40		46		50		ns
t_{OED}	Delay time, $\overline{OE}$ to data		15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 12)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 12)		20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)		85		98		110		ns
t_{CPW}	Delay time, $\overline{W}$ low after $\overline{CAS}$ precharge (read-write operation only)		60		68		75		ns
t_{RASS}	Pulse duration, self-refresh entry from $\overline{RAS}$ low		100		100		100		µs
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self refresh		110		130		150		ns
t_{TAA}	Access time from address (test mode)		35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)		40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)		65		75		85		ns
t_{REF}	Refresh time interval	'4x6400		64		64		64	ms
		'4x6400P		128		128		128	
		'4x7400		32		32		32	
		'4x7400P		128		128		128	
t_T	Transition time		3	30	3	30	3	30	ns

NOTE 12: The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT

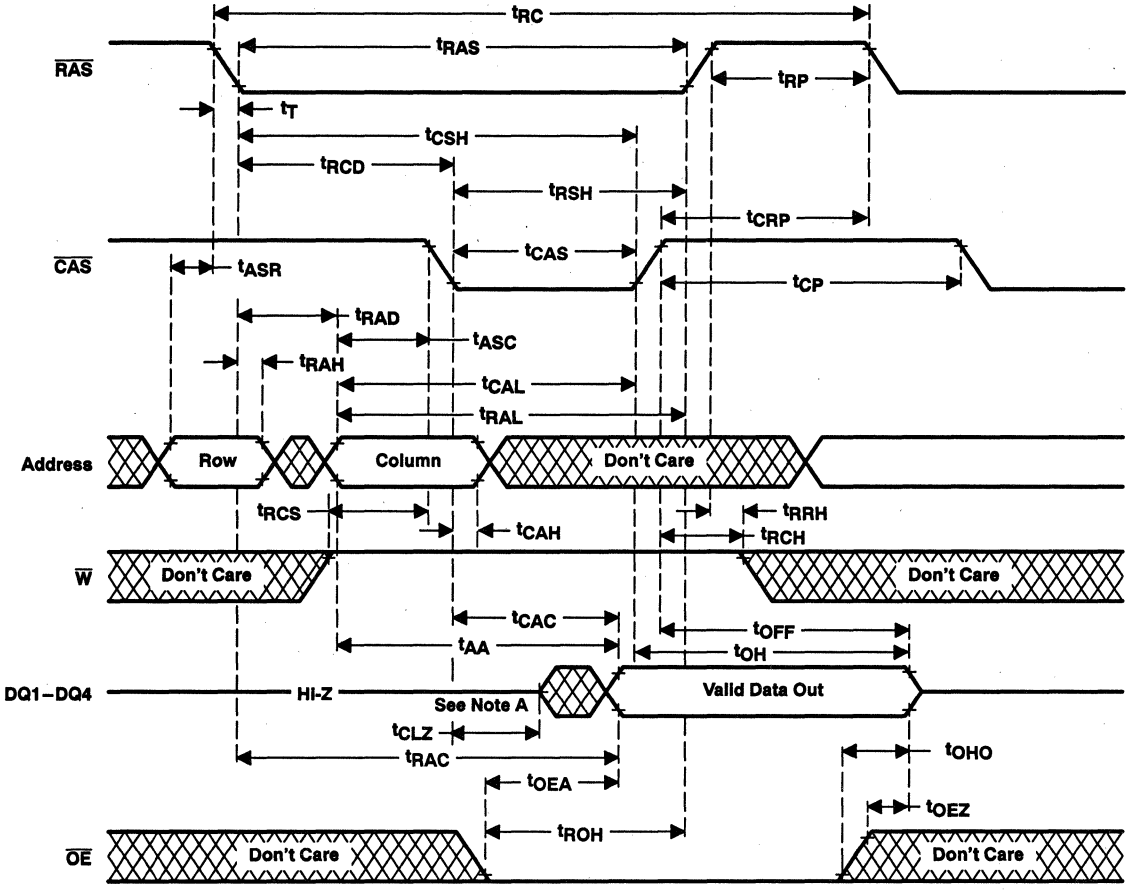


(b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capactiance.

DEVICE	V_{CC} (V)	R_1 (Ω)	R_2 (Ω)	V_{TH} (V)	R_L (Ω)
'41x400/P	5	828	295	1.31	218
'42x400/P	3.3	1178	868	1.4	500

Figure 2. Load Circuits for Timing Parameters



NOTE A: Output can go from 3-state to an invalid-data state prior to the specified access time.

Figure 3. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

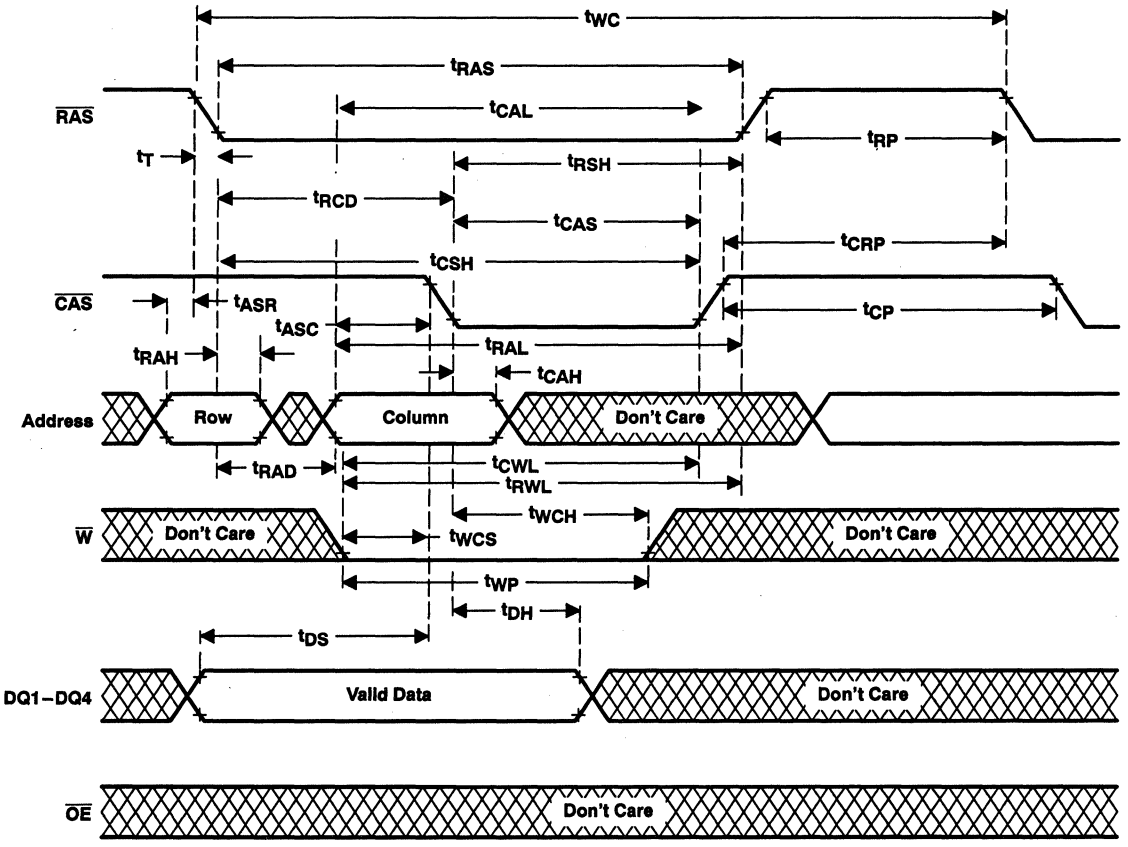


Figure 4. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

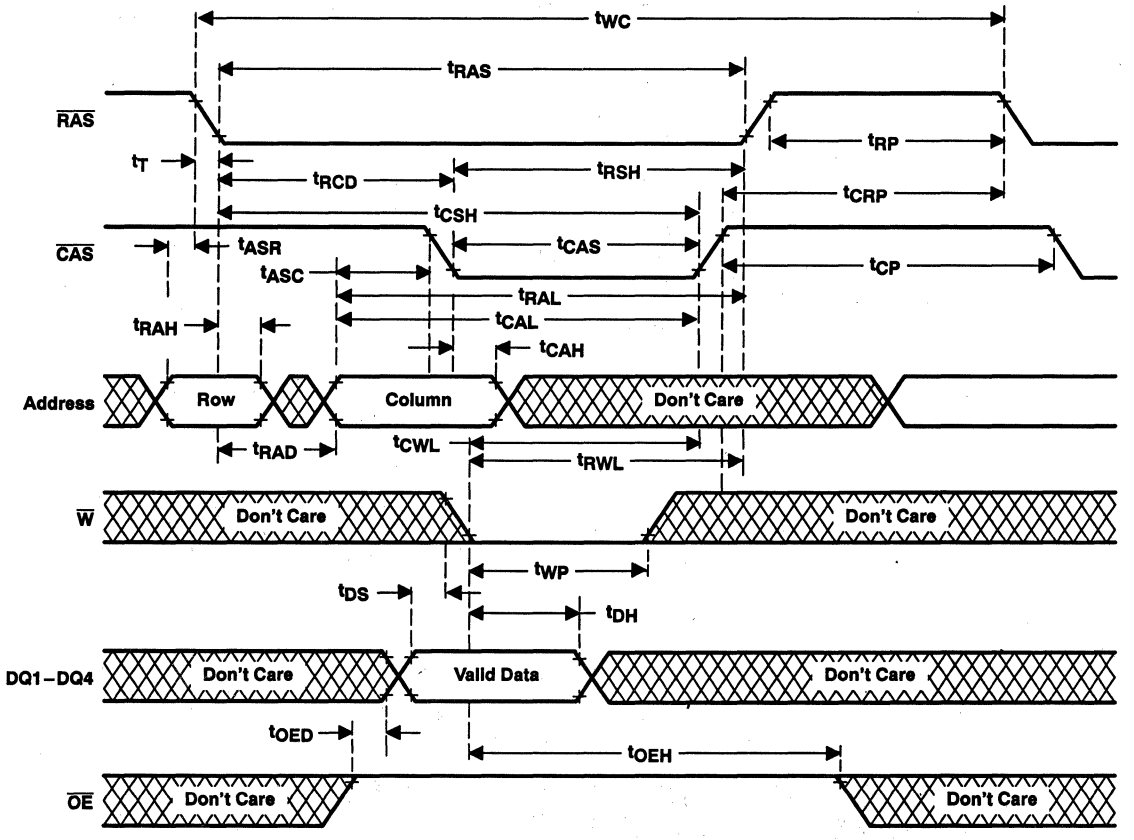
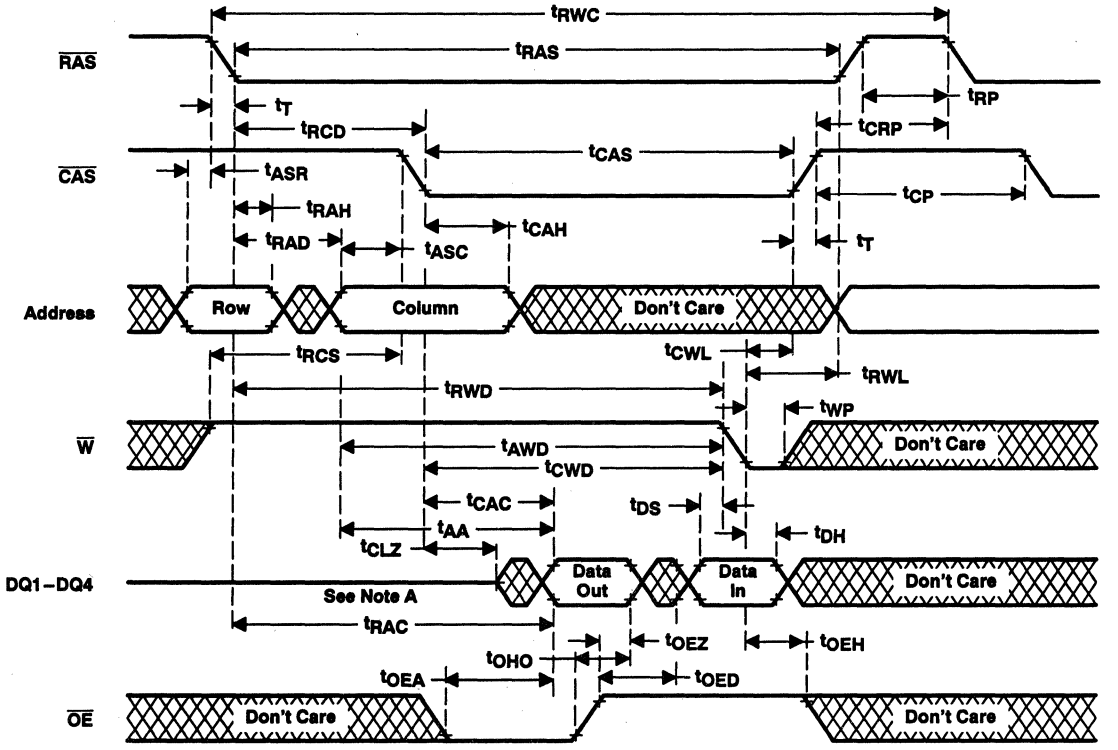


Figure 5. Write-Cycle Timing

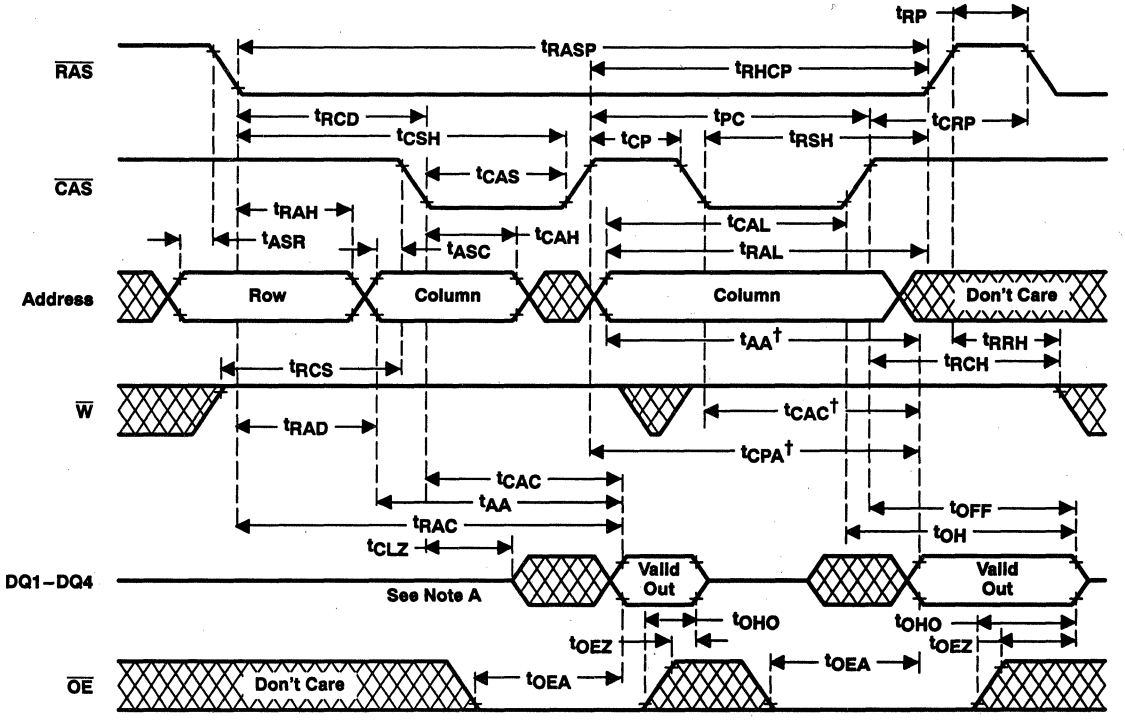
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from 3-state to an invalid-data state prior to the specified access time.

Figure 6. Read-Write-Cycle Timing

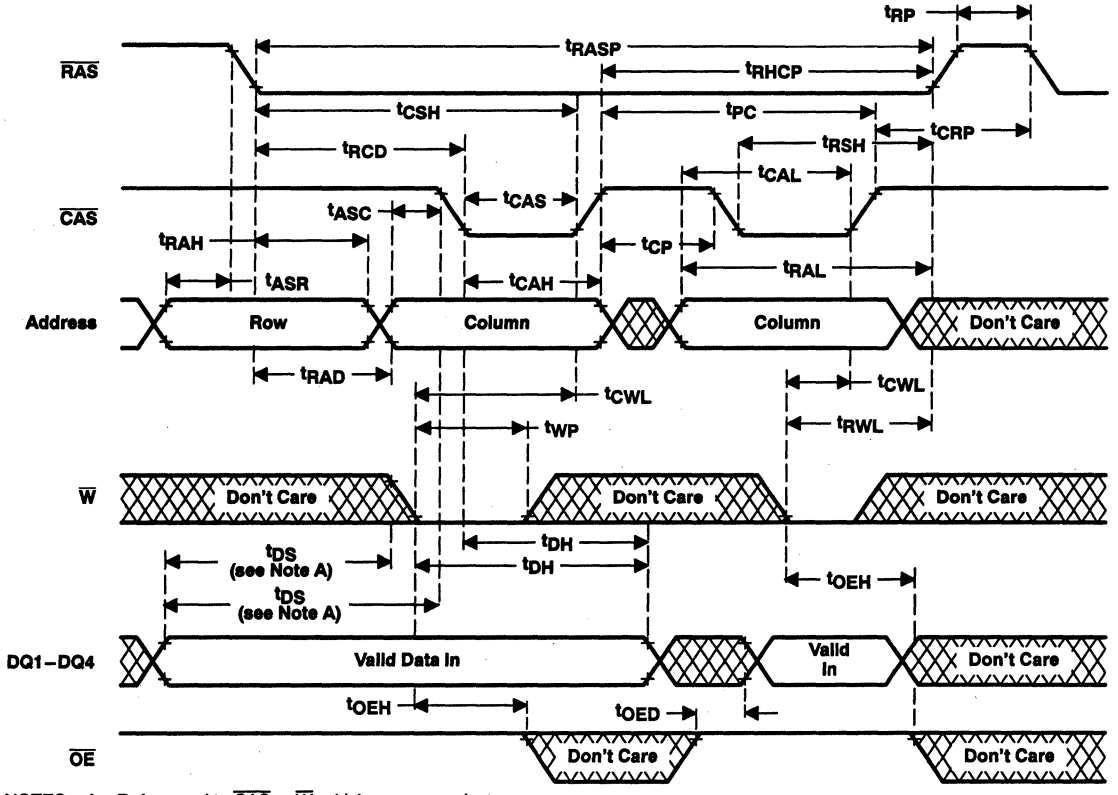
PARAMETER MEASUREMENT INFORMATION



† Access time is t_{CPA}, t_{CAC}, or t_{AA} dependent.
NOTE A: Output can go from 3-state to an invalid-data state prior to the specified access time.

Figure 7. Enhanced-Page-Mode Read-Cycle Timing

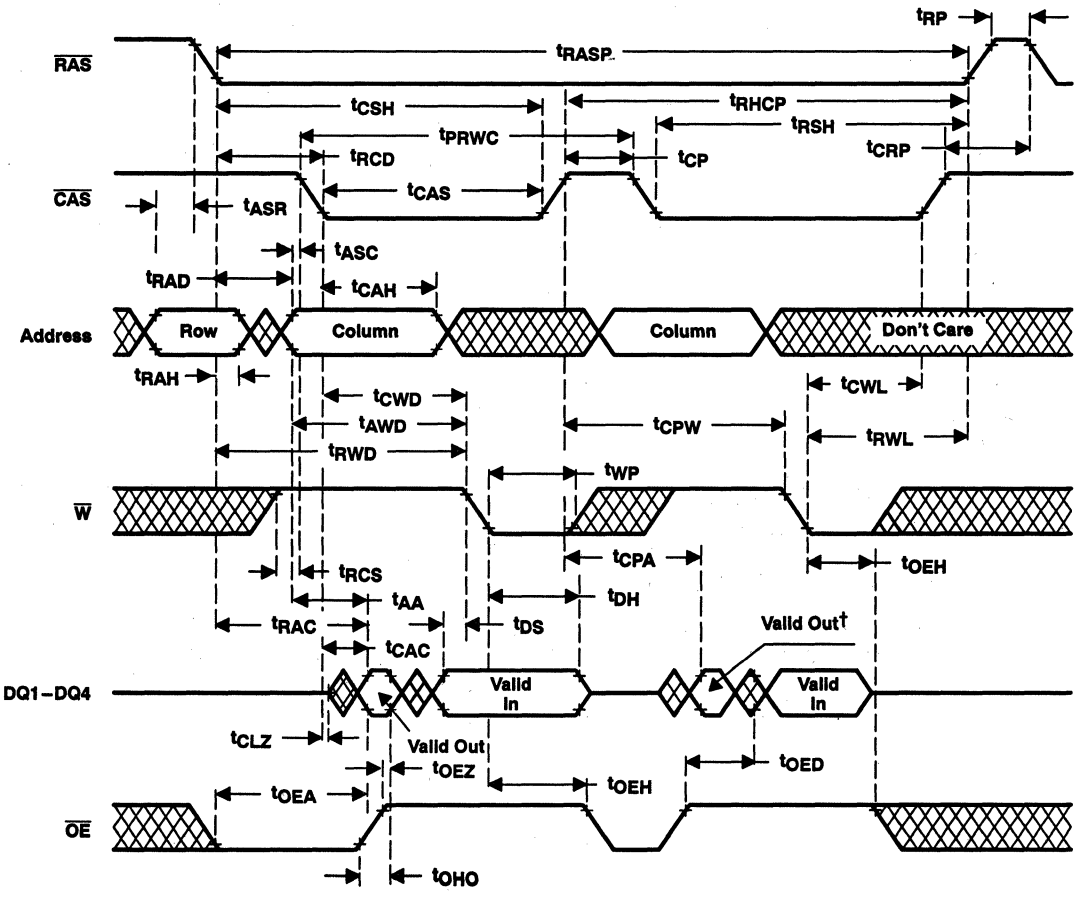
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Output can go from 3-state to an invalid-data state prior to the specified access time.
NOTE A: A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced-Page-Mode Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

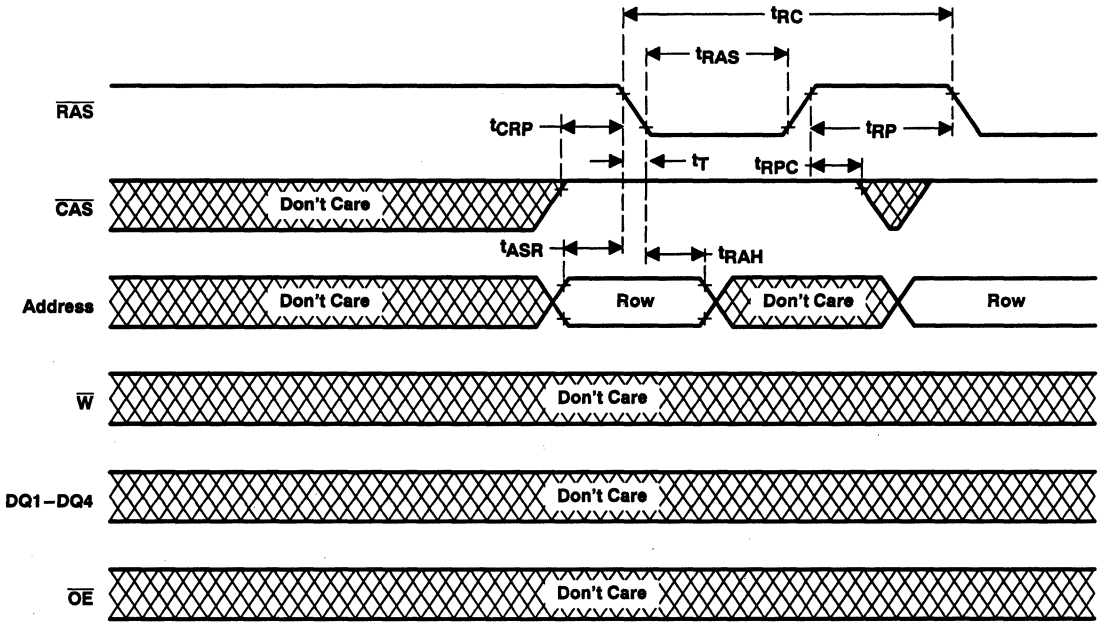


Figure 10. RAS-Only Refresh Timing

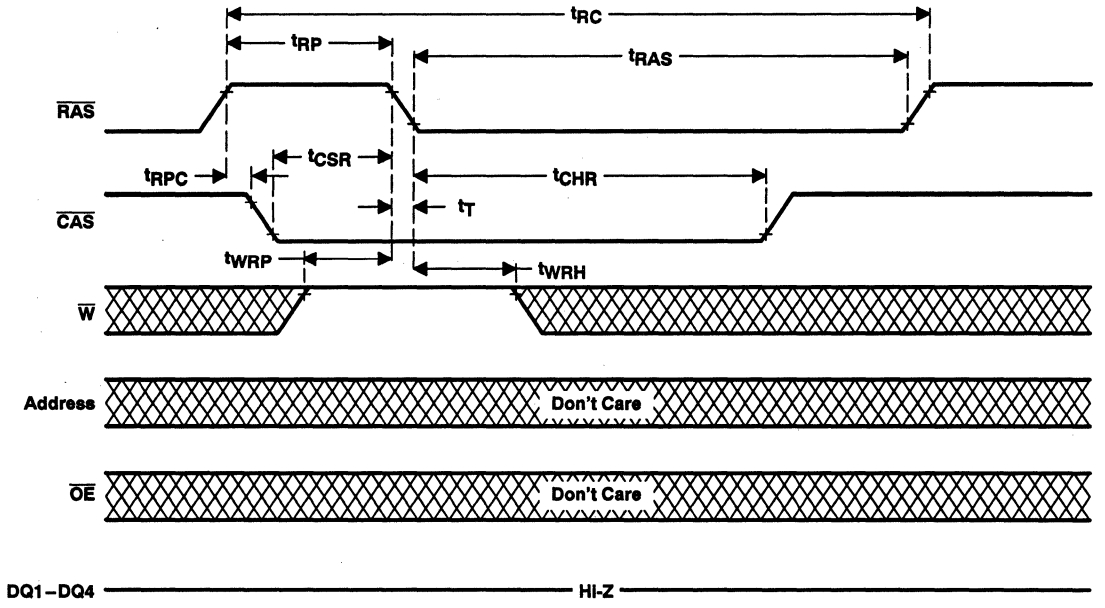


Figure 11. Automatic-CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

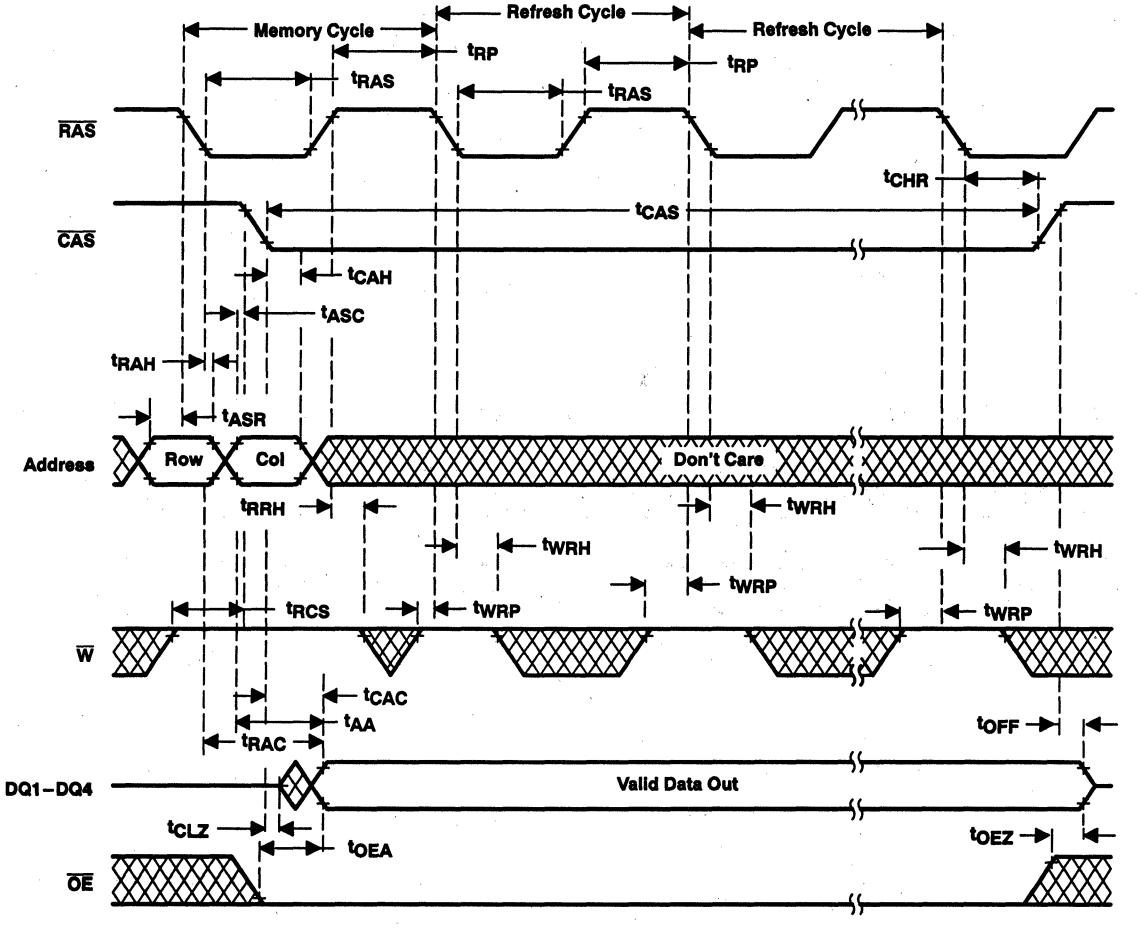


Figure 12. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

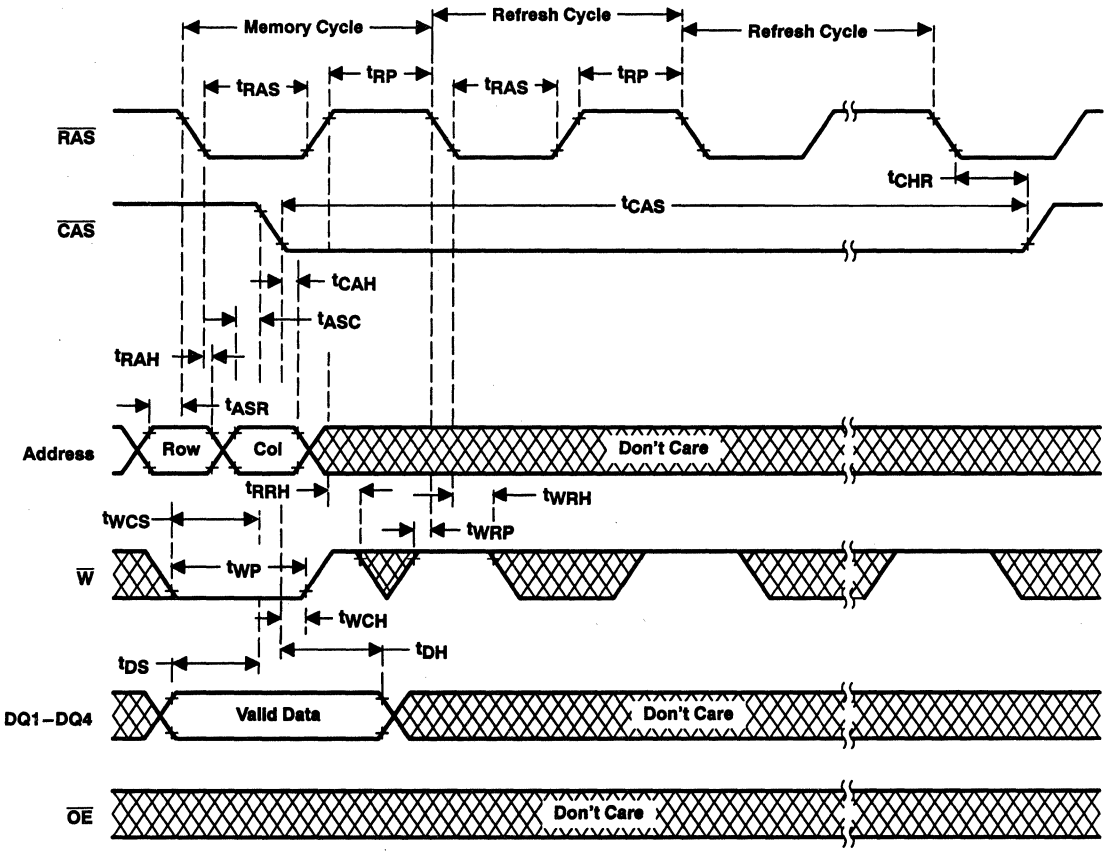


Figure 13. Hidden-Refresh-Cycle (Write) Timing

PARAMETER MEASUREMENT INFORMATION

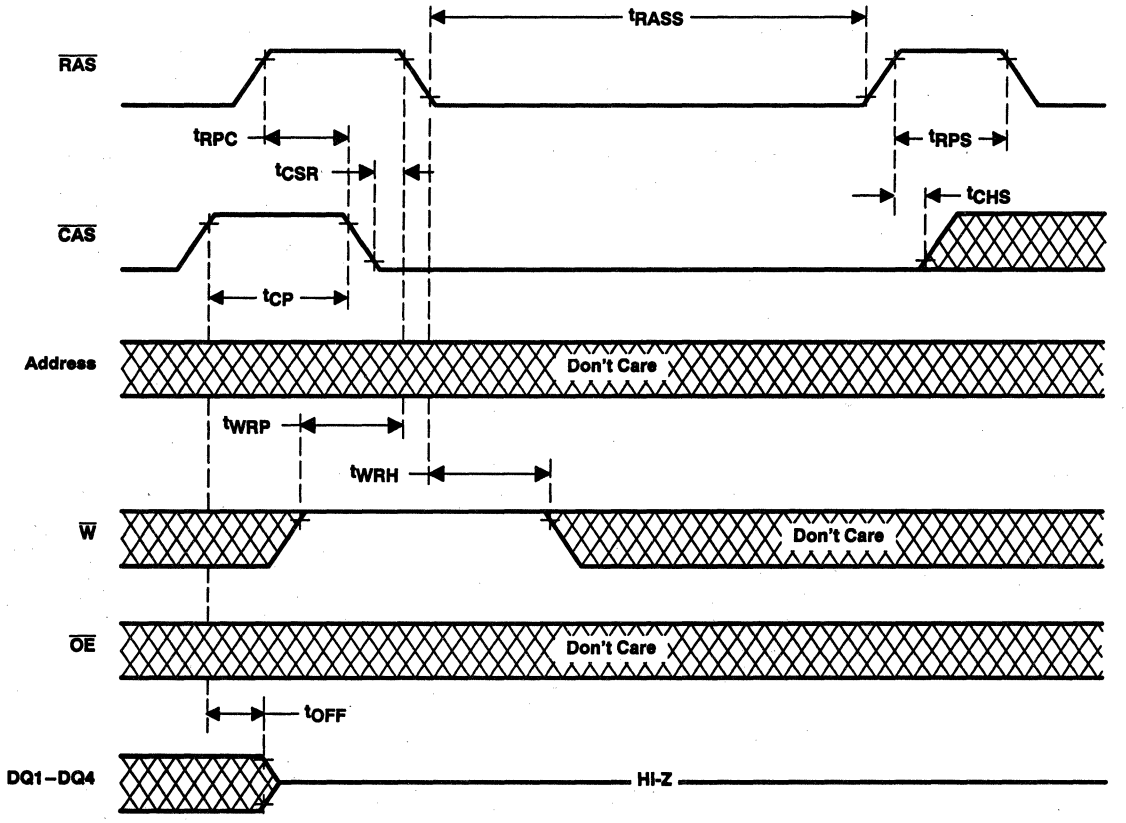


Figure 14. Self-Refresh-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

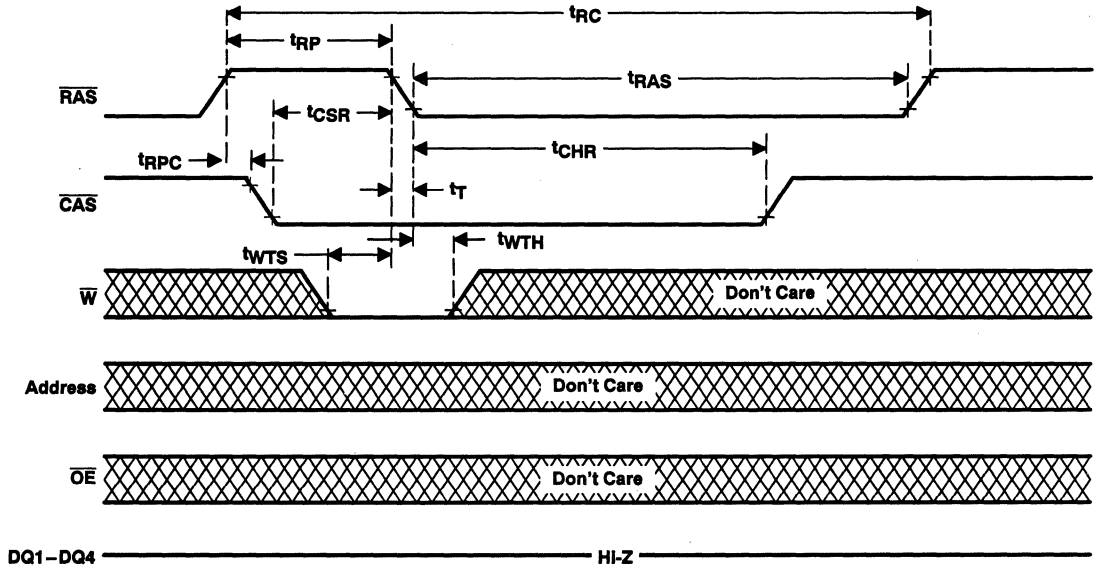


Figure 15. Test-Mode-Entry-Cycle Timing

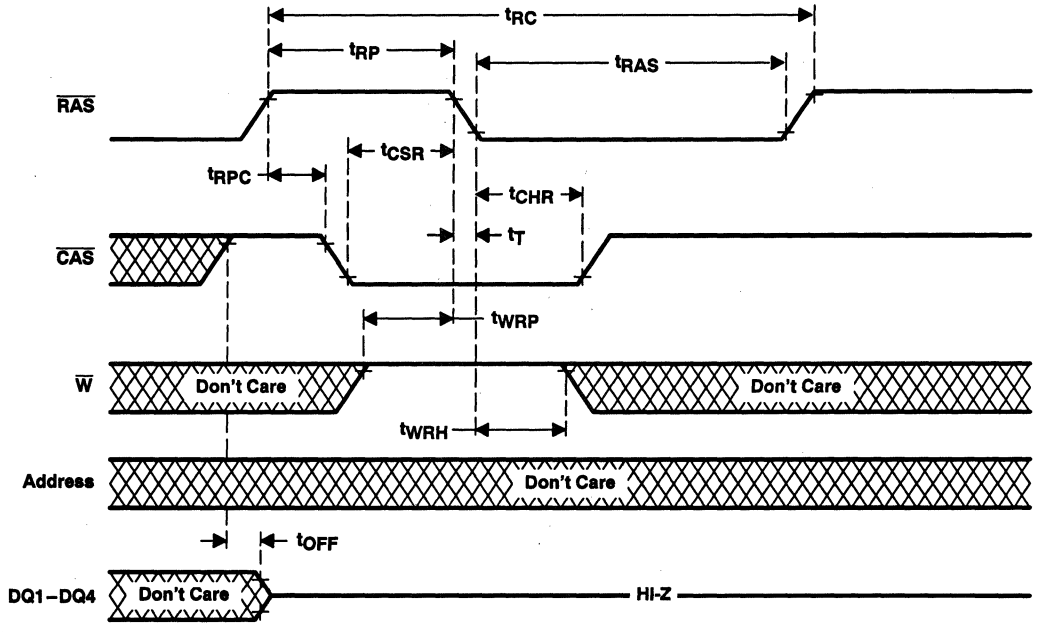
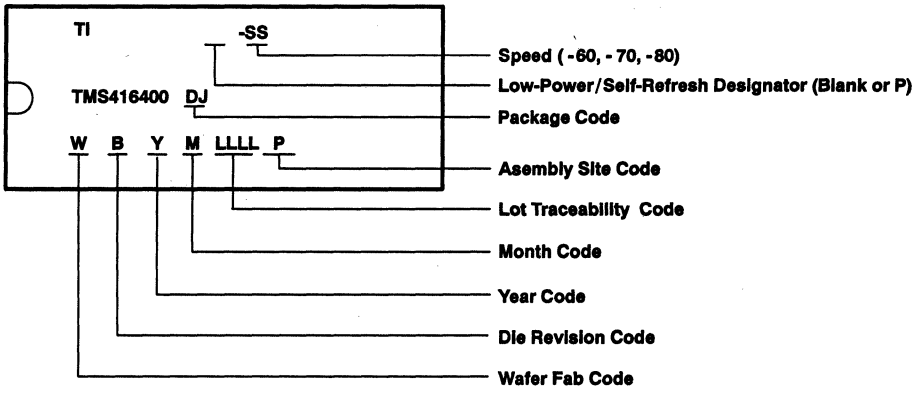


Figure 16. Test-Mode-Exit-Cycle CBR-Refresh-Cycle Timing

device symbolization (TMS416400 illustrated)



- **Organization . . . 1048576 × 16**
- **Single Power Supply (5 V or 3.3 V)**
- **Performance Ranges:**

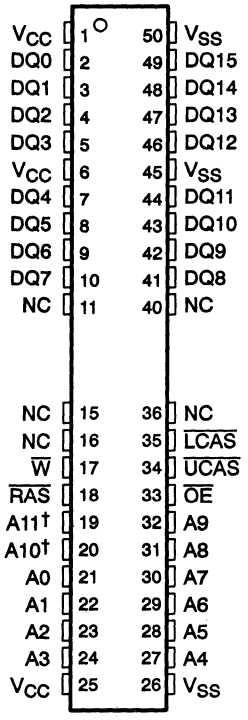
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'4xx160/P-60	60 ns	15 ns	30 ns	110 ns
'4xx160/P-70	70 ns	18 ns	35 ns	130 ns
'4xx160/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page-Mode Operation With CAS-Before-RAS (CBR) Refresh**
- **Long Refresh Period and Self-Refresh Option (TMS4xx160P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **High-Reliability Plastic 42-Lead (DZ Suffix) 400-Mil-Wide Surface-Mount (SOJ) Package and 44/50-Lead (DGE Suffix) Surface-Mount Thin Small-Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instruments EPIC™ CMOS Process**

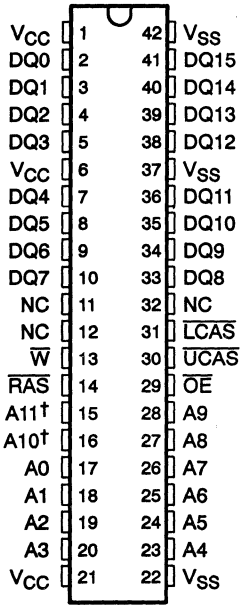
AVAILABLE OPTIONS

DEVICE	POWER SUPPLY	SELF REFRESH, BATTERY BACKUP	REFRESH CYCLES
TMS416160	5 V	—	4096 in 64 ms
TMS416160P	5 V	Yes	4096 in 256 ms
TMS418160	5 V	—	1024 in 16 ms
TMS418160P	5 V	Yes	1024 in 128 ms
TMS426160	3.3 V	—	4096 in 64 ms
TMS426160P	3.3 V	Yes	4096 in 256 ms
TMS428160	3.3 V	—	1024 in 16 ms
TMS428160P	3.3 V	Yes	1024 in 128 ms

DGE PACKAGE
(TOP VIEW)



DZ PACKAGE
(TOP VIEW)



† A10 and A11 are NC for TMS4x8160 and TMS4x8160P.

PIN NOMENCLATURE	
A0–A11	Address Inputs
DQ0–DQ15	Data In/Data Out
LCAS	Lower Column-Address Strobe
NC	No Internal Connection
OE	Output Enable
RAS	Row-Address Strobe
UCAS	Upper Column-Address Strobe
VCC	5-V or 3.3-V Supply‡
VSS	Ground
W	Write Enable

‡ See Available Options Table.

description

The TMS4xx160 series is a set of high-speed, 16777216-bit dynamic random-access memories (DRAMs) organized as 1048576 words of 16 bits each. The TMS4xx160P series is a similar set of high-speed, low-power, self-refresh, 16777216-bit DRAMs organized as 1048576 words of 16 bits each.

Both sets employ state-of-the-art enhanced performance implanted CMOS (EPIC™) technology for high performance, reliability, and low power at low cost.

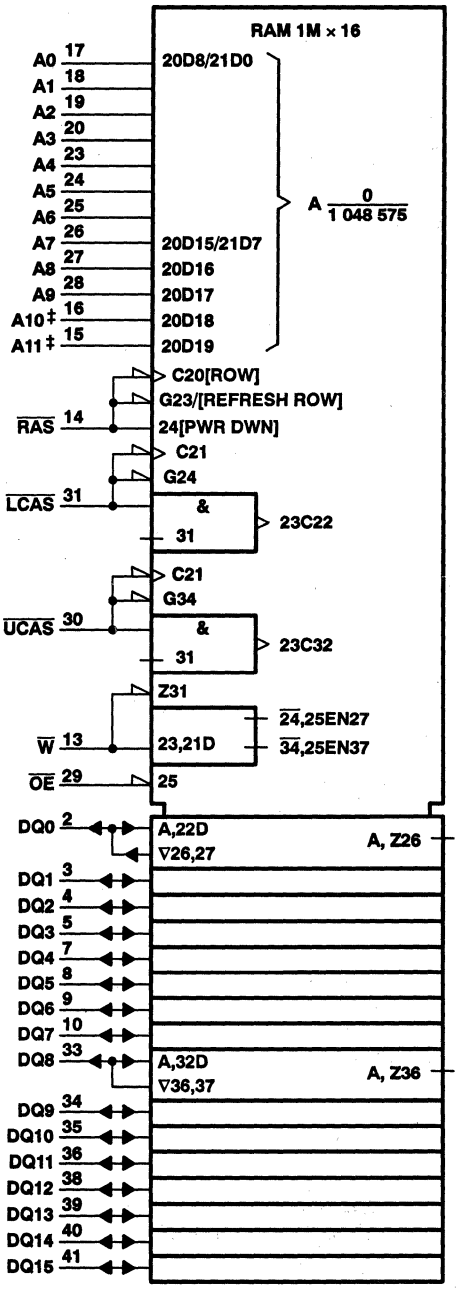
These devices feature maximum RAS access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4xx160 and TMS4xx160P are offered in a 44/50-lead plastic surface-mount TSOP (DGE suffix) and a 42-lead plastic surface-mount SOJ (DZ suffix) package. These packages are characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

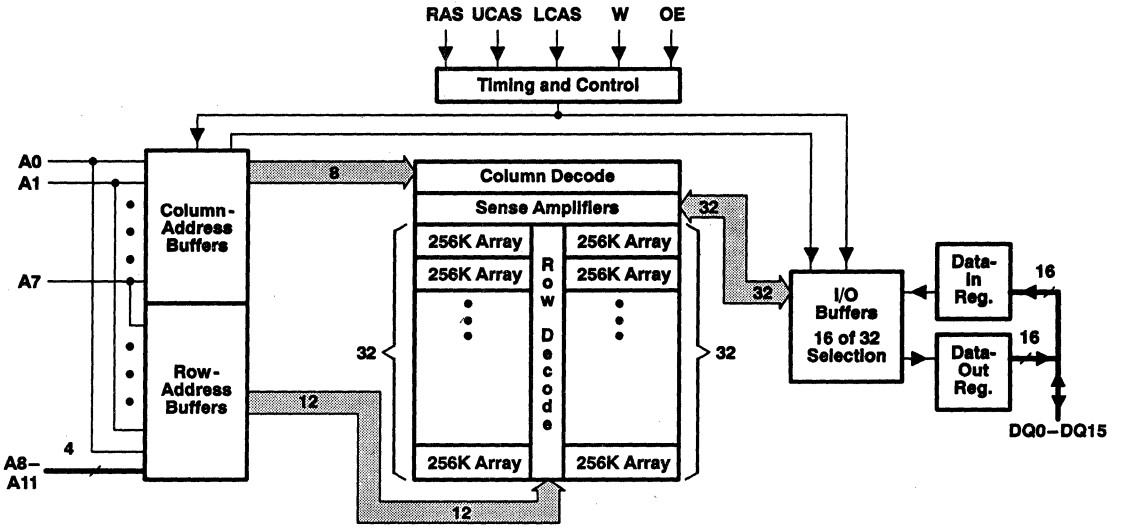
PRODUCT PREVIEW

logic symbol†



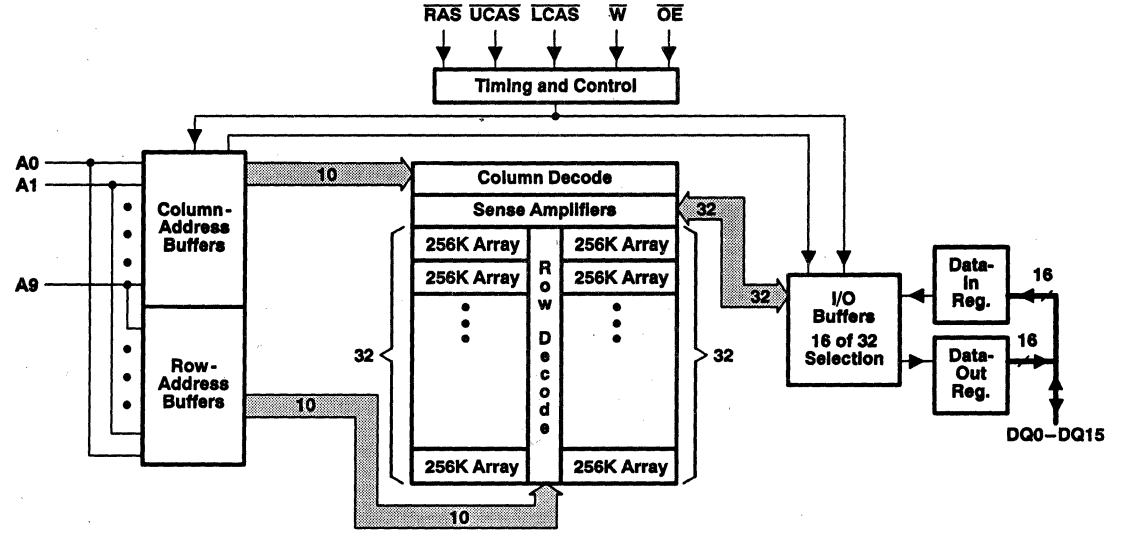
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the DZ package.
‡ A10 and A11 are NC for TMS4x8160 and TMS4x8160P.

functional block diagrams (TMS4x6160/P)



(a) TMS4x6160, TMS4x6160P

functional block diagram (TMS4x8160/P)



(b) TMS4x8160, TMS4x8160P

PRODUCT PREVIEW

operation

dual $\overline{CAS}$

Two $\overline{CAS}$ pins ($\overline{LCAS}$ and $\overline{UCAS}$) are provided to give independent control of the 16 data-I/O pins (DQ0–DQ15), with $\overline{LCAS}$ corresponding to DQ0–DQ7 and $\overline{UCAS}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{xCAS}$ falling edge. Each $\overline{xCAS}$ going low enables its corresponding DQx pin with data associated with the column address latched on the first falling $\overline{xCAS}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{xCAS}$ edge. The delay time from $\overline{xCAS}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{xCAS}$ to its corresponding DQx pin.

In order to latch in a new column address, both $\overline{xCAS}$ pins must be brought high. The column-precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first $\overline{xCAS}$ falling edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

For early-write cycles, the data is latched on the first $\overline{xCAS}$ falling edge. Only the DQs that have the corresponding $\overline{xCAS}$ low are written into. Each $\overline{xCAS}$ must meet t_{CAS} minimum in order to ensure writing into the storage cell. To latch a new address and new data, all $\overline{xCAS}$ pins must be high and meet t_{CP}.

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{xCAS}$ page-mode cycle time used. With minimum $\overline{xCAS}$ page-cycle time, all columns can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{xCAS}$ is high. The falling edge of the first $\overline{xCAS}$ latches the column addresses. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when $\overline{xCAS}$ transitions low. This performance improvement is referred to as enhanced page mode. A valid column address may be presented immediately after t_{RAH} (row-address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{xCAS}$. In this case, data is obtained after t_{CAC} maximum (access time from $\overline{xCAS}$ low) if t_{AA} maximum (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{xCAS}$ goes high, minimum access time for the next cycle is determined by t_{CPA} (access time from rising edge of the last $\overline{xCAS}$).

address: A0–A11 (TMS4x6160, TMS4x6160P) and A0–A9 (TMS4x8160, TMS4x8160P)

Twenty address bits are required to decode 1 of 1048576 storage cell locations. For the TMS4x6160 and TMS4x6160P, 12 row-address bits are set up on A0 through A11 and latched onto the chip by $\overline{RAS}$. Eight column-address bits are set up on A0 through A7 and latched onto the chip by the first $\overline{xCAS}$. For the TMS4x8160 and TMS4x8160P, 10 row-address bits are set up on A0–A9 and latched onto the chip by $\overline{RAS}$. Ten column-address bits are set up on A0–A9 and latched onto the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{OE}$ grounded.

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data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{xCAS}$ and the data is strobed in by the first occurring $\overline{xCAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{xCAS}$ is already low and the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

data out (DQ0–DQ15)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{xCAS}$ to be brought low for the output buffers to go into the low-impedance state, and they remain in the low-impedance state until either $\overline{OE}$ or $\overline{xCAS}$ is brought high.

$\overline{RAS}$-only refresh

TMS4x6160, TMS4x6160P

A refresh operation must be performed at least once every 64 ms (256 ms for TMS4x6160P) to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding both $\overline{xCAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

TMS4x8160, TMS4x8160P

A refresh operation must be performed at least once every 16 ms (128 ms for TMS4x8160P) to retain data. This can be achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding both $\overline{xCAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored and the refresh address is generated internally.

$\overline{xCAS}$-before-$\overline{RAS}$ (xCBR) refresh

$\overline{xCBR}$ refresh is utilized by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{xCBR}$ refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

battery-backup refresh

TMS4x6160P

A low-power battery-backup refresh mode that requires less than 600 µA (5 V) or 350 µA (3.3 V) refresh current is available on the TMS4x6160P. Data integrity is maintained using $\overline{xCBR}$ refresh with a period of 62.5 µs while holding $\overline{RAS}$ low for less than 300 ns. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} < 0.2$ V, $V_{IH} > V_{CC} - 0.2$ V).

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TMS4x8160P

A low-power battery-backup refresh mode that requires less than 600 μA (5 V) or 350 μA (3.3 V) refresh current is available on the TMS4x8160P. Data integrity is maintained using xCBR refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 300 ns. To minimize current consumption, all input levels must be at CMOS levels (V_{IL} < 0.2 V, V_{IH} > V_{CC} – 0.2 V).

self refresh (TMS4xx160P)

The self-refresh mode is entered by dropping $\overline{xCAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{xCAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{xCAS}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or $\overline{xCBR}$) cycle.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: TMS41x160, TMS41x160P ..... – 1 V to 7 V
TMS42x160, TMS42x160P ..... – 0.5 V to 4.6 V
Voltage range on any pin (see Note 1): TMS41x160, TMS41x160P ..... – 1 V to 7 V
TMS42x160, TMS42x160P ..... – 0.5 V to 4.6 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		TMS41x160			TMS42x160			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	3	3.3	3.6	V
V_{SS}	Supply voltage		0			0		V
V_{IH}	High-level input voltage	2.4		6.5	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

TMS416160/P

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'416160-60 '416160P-60		'416160-70 '416160P-70		'416160-80 '416160P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle			90		80		70	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'416160		1		1		1	mA
			'416160P		500		500		500	µA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			90		80		70	mA
I_{CC4}‡¶	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			90		80		70	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			500		500		500	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 256 ms); CBR only	t_{RC} = 62.5 µs, t_{RAS} ≤ 300 ns, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			600		600		600	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}
# For TMS416160P only

PRODUCT PREVIEW

TMS418160/P

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†		'418160-60 '418160P-60		'418160-70 '418160P-70		'418160-80 '418160P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle			190		180		170	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'418160		1		1		1	mA
			'418160P		500		500		500	µA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			190		180		170	mA
I_{CC4}‡¶	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			100		90		80	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			500		500		500	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms); CBR only	t_{RC} = 125 µs, t_{RAS} ≤ 300 ns, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			600		600		600	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}
# For TMS418160P only

PRODUCT PREVIEW

TMS426160/P

electrical characteristics over recommended ranges of supply voltage and operating free-air conditions (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†		'426160-60 '426160P-60		'426160-70 '426160P-70		'426160-80 '426160P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 3.6 V, Minimum cycle			90		80		70	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			1		1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'426160		500		500		500	µA
			'426160P		200		200		200	µA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$-only refresh) $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			90		80		70	mA
I_{CC4}‡¶	Average page current	V_{CC} = 3.6 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			90		80		70	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			250		250		250	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 256 ms), CBR only	t_{RC} = 62.5 µs, t_{RAS} ≤ 300 ns, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}
# For TMS426160P only

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TMS428160/P

electrical characteristics over recommended ranges of supply voltage and operating free-air conditions (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†		'428160-60 '428160P-60		'428160-70 '428160P-70		'428160-80 '428160P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = –100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 3.6 V, Minimum cycle			190		180		170	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			1		1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'428160		500		500		500	µA
			'428160P		200		200		200	µA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$-only refresh) $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			190		180		170	mA
I_{CC4}‡¶	Average page current	V_{CC} = 3.6 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			100		90		80	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			250		250		250	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms), CBR only	t_{RC} = 125 µs, t_{RAS} ≤ 300 ns, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}
# For TMS428160P only

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

	PARAMETER	MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A11		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{xCAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_O	Output capacitance		7	pF

NOTE 3: V_{CC} = 5 V ± 0.5 V or 3.3 V + 0.3 V (see Table 1), and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	'4xx160-60 '4xx160P-60		'4xx160-70 '4xx160P-70		'4xx160-80 '4xx160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 4)		30		35		40	ns
t_{CAC}	Access time from $\overline{xCAS}$ low (see Note 4)		15		18		20	ns
t_{CPA}	Access time from column precharge (see Note 4)		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low (see Note 4)		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low (see Note 4)		15		18		20	ns
t_{CLZ}	Delay time, $\overline{xCAS}$ low to output in low-impedance state	0		0		0		ns
t_{OH}	Output data hold time (from $\overline{xCAS}$)	3		3		3		ns
t_{OHO}	Output data hold time (from $\overline{OE}$)	3		3		3		ns
t_{OFF}	Output disable time after $\overline{xCAS}$ high (see Note 5)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 5)	0	15	0	18	0	20	ns

NOTES: 4. Access times for TMS42x160 are measured with output reference levels of V_{OH} = 2 V and V_{OI} = 0.8 V.
5. t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4xx160-60 '4xx160P-60		'4xx160-70 '4xx160P-70		'4xx160-80 '4xx160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read (see Note 6)	110		130		150		ns
t_{WC}	Cycle time, write (see Note 6)	110		130		150		ns
t_{RWC}	Cycle time, read-write (see Note 6)	155		181		205		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 6 and 7)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-write (see Note 6)	85		96		105		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 8)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 8)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{xCAS}$ low (see Note 9)	15	10 000	18	10 000	20	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{xCAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 9)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{xCAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ low (early-write operation only)	0		0		0		ns
t_{CAH}	Hold time, column address after $\overline{xCAS}$ low	10		15		15		ns
t_{DH}	Hold time, data (see Note 10)	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{xCAS}$ high (see Note 11)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 11)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{xCAS}$ low (early-write operation only)	10		15		15		ns
t_{CLCH}	Hold time, $\overline{xCAS}$ low to $\overline{xCAS}$ high	5		5		5		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{xCAS}$ precharge	35		40		45		ns
t_{OEH}	Hold time, $\overline{OE}$ command	15		18		20		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	10		10		10		ns
t_{CHS}	Hold time, $\overline{xCAS}$ low after $\overline{RAS}$ high (self refresh)	– 50		– 50		– 50		ns

NOTES: 6. All cycle times assume t_T = 5 ns.
7. To assure t_{PC} min, t_{ASC} should be ≥ to t_{CP}.
8. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
9. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
10. Referenced to the later of $\overline{xCAS}$ or $\overline{W}$ in write operations
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

PRODUCT PREVIEW

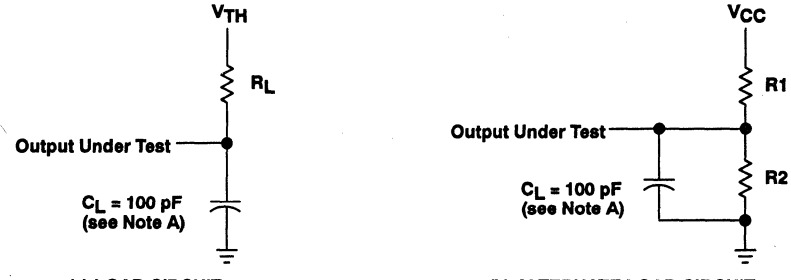
timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			'4xx160-60 '4xx160P-60		'4xx160-70 '4xx160P-70		'4xx160-80 '4xx160P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CP}	Delay time, $\overline{xCAS}$ high (precharge)		10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)		55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high ($\overline{xCBR}$ refresh only)		10		10		10		ns
t_{CRP}	Delay time, $\overline{xCAS}$ high to $\overline{RAS}$ low		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high		60		70		80		ns
t_{CSR}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ low ($\overline{xCBR}$ refresh only)		5		5		5		ns
t_{CWD}	Delay time, $\overline{xCAS}$ low to $\overline{W}$ low (read-write operation only)		40		46		50		ns
t_{OED}	Delay time, $\overline{OE}$ to data		15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 12)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{xCAS}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ low (see Note 12)		20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{xCAS}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ high		15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)		85		98		110		ns
t_{CPW}	Delay time, $\overline{W}$ low after $\overline{xCAS}$ precharge (read-write operation only)		60		68		75		ns
t_{RASS}	Pulse duration, self-refresh entry from $\overline{RAS}$ low		100		100		100		µs
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self refresh		110		130		150		ns
t_{REF}	Refresh time interval	'4x6160		64		64		64	ms
		'4x6160P		256		256		256	
		'4x8160		16		16		16	ms
		'4x8160P		128		128		128	
t_T	Transition time		3	30	3	30	3	30	ns

NOTE 12: The maximum value is specified only to assure access time.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



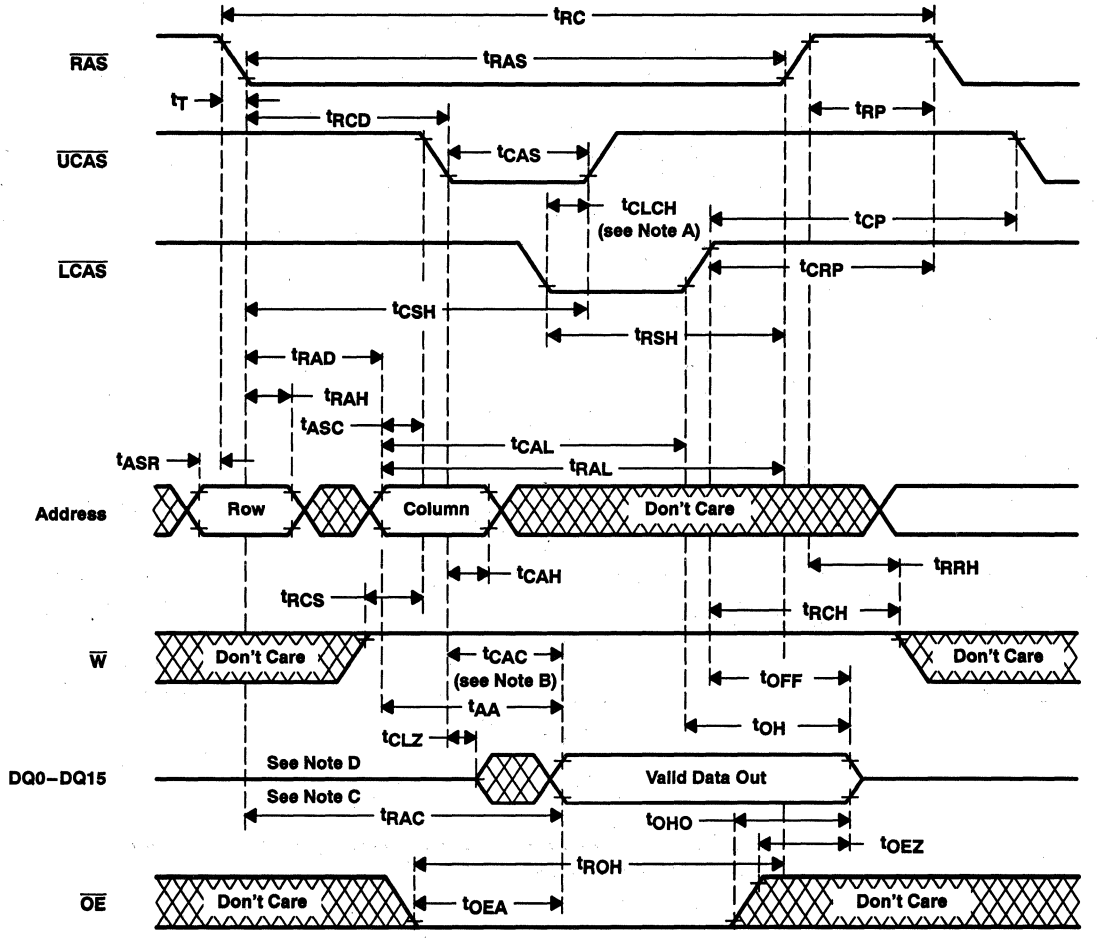
(a) LOAD CIRCUIT (b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.

DEVICE	V_{CC} (V)	R1 (Ω)	R2 (Ω)	V_{TH} (V)	R_L (Ω)
41x160/P	5	828	295	1.31	218
42x160/P	3.3	1178	868	1.4	500

Figure 1. Load Circuits for Timing Parameters

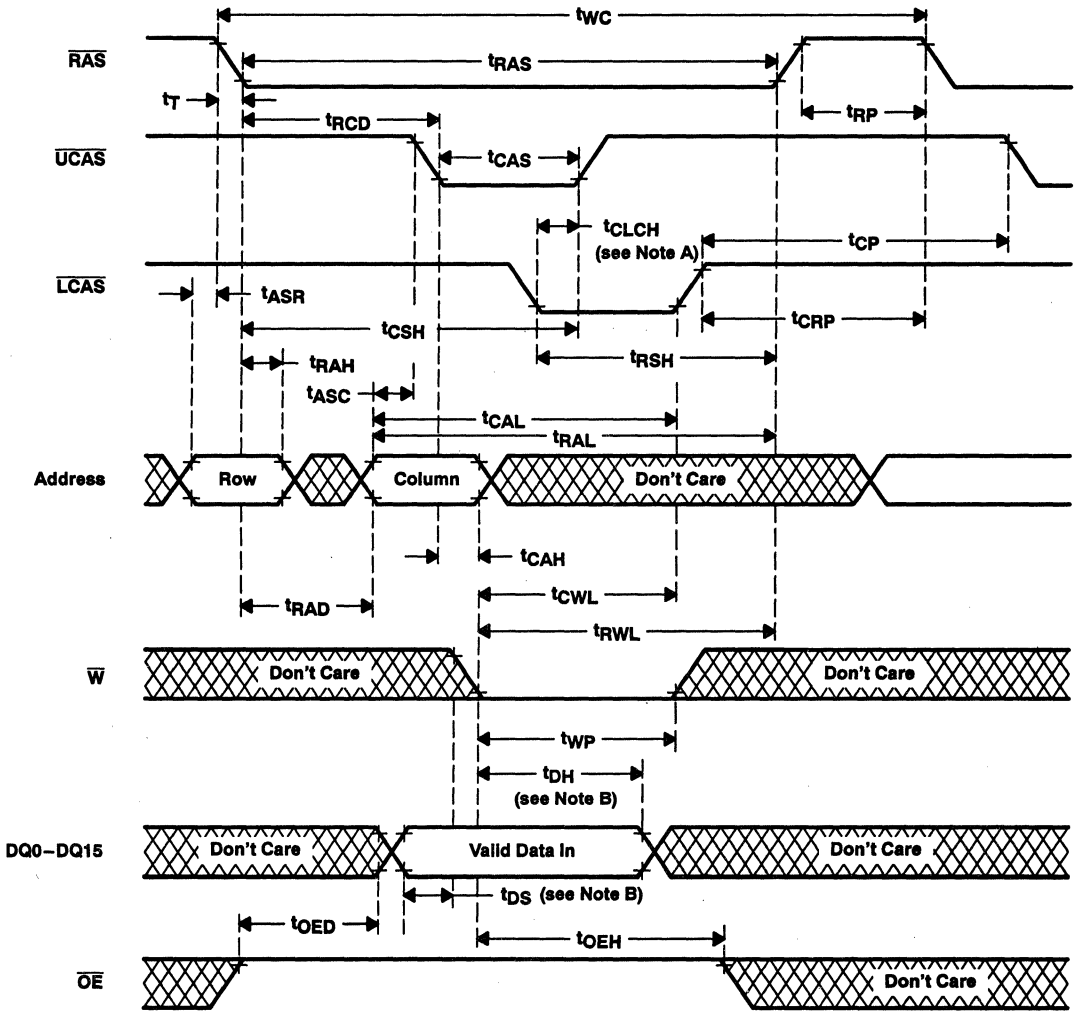
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. $\overline{xCAS}$ order is arbitrary.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

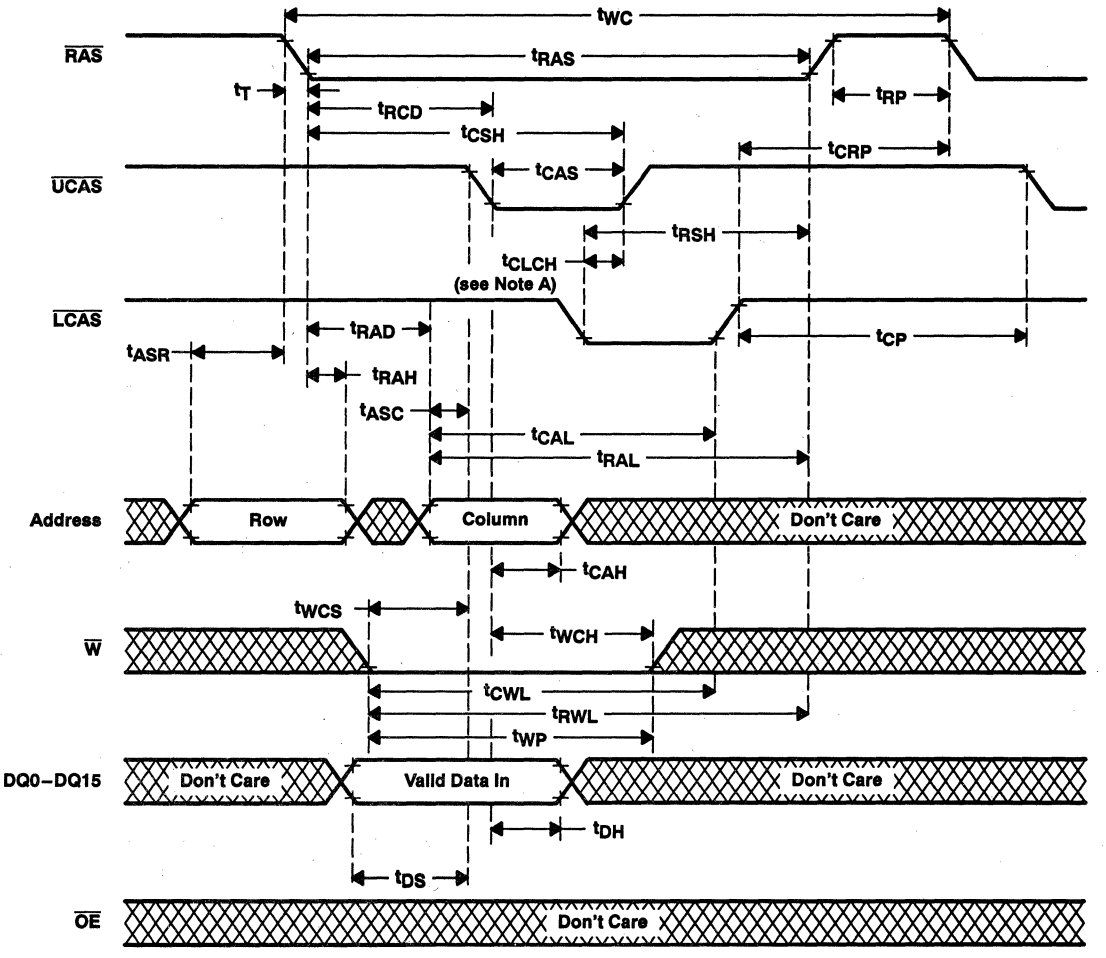


NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to the first $\overline{\text{xCAS}}$ or $\overline{\text{W}}$, whichever occurs last
C. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 3. Write-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

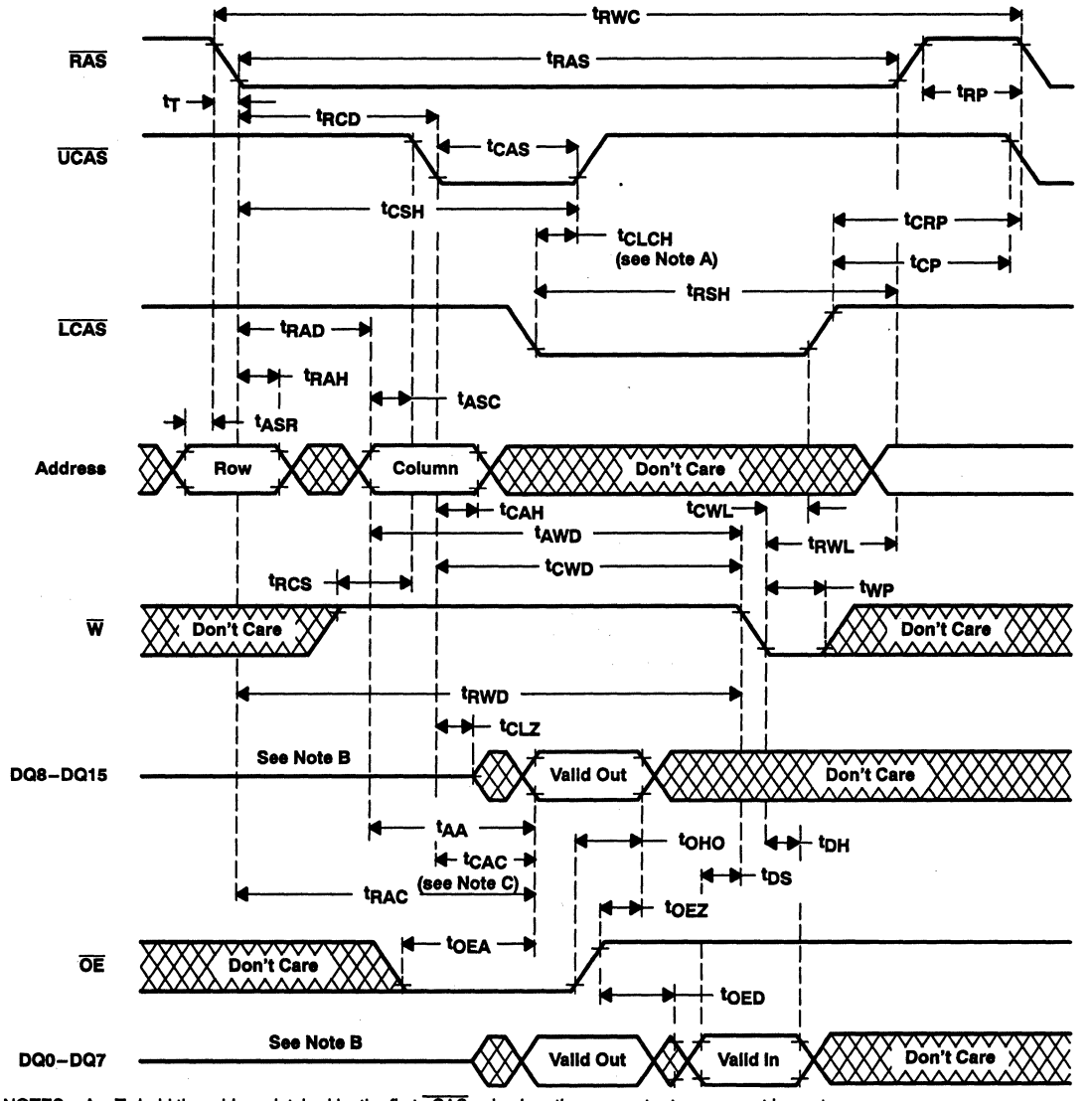


NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.

Figure 4. Early-Write-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

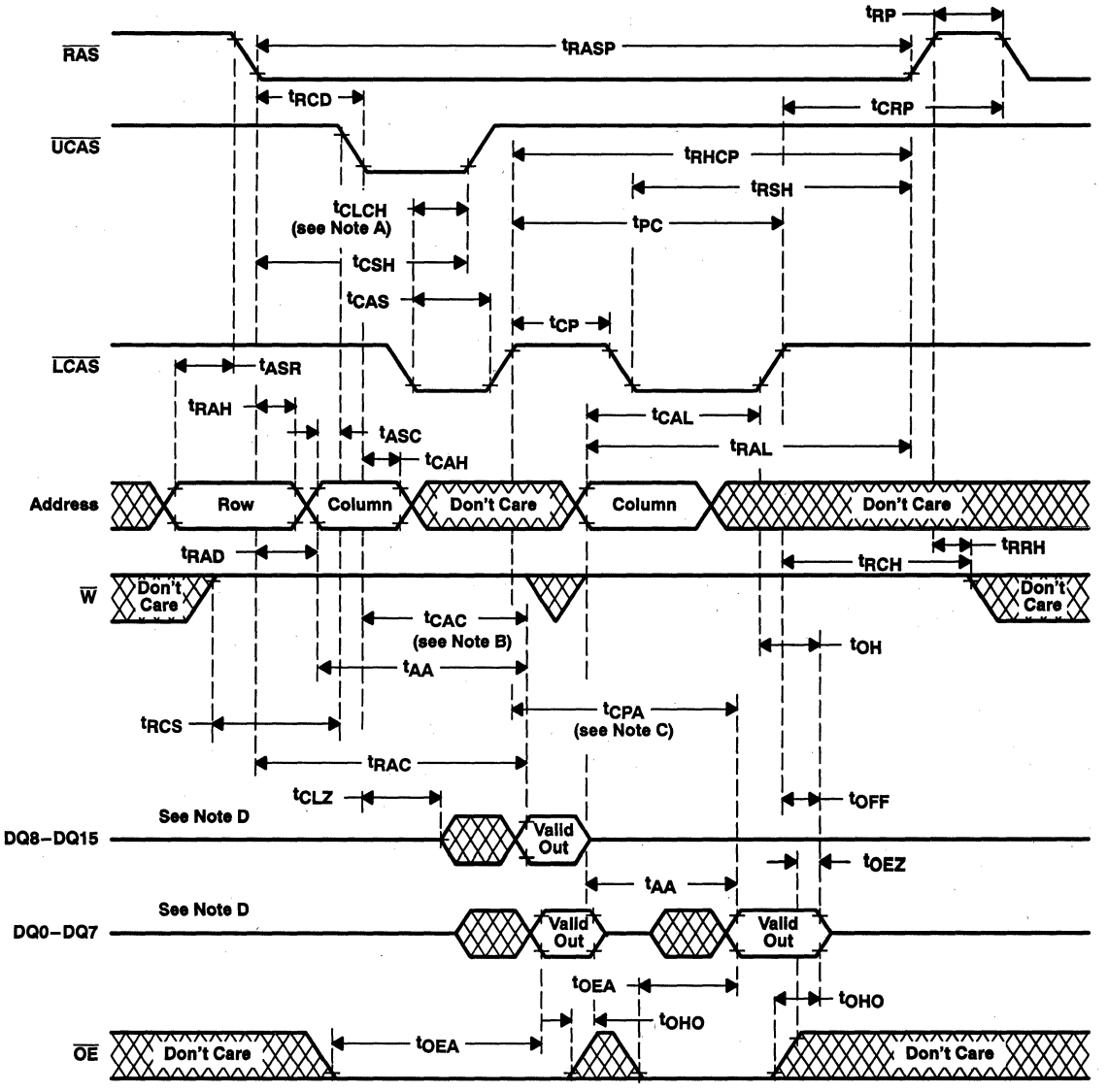


NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Output can go from a the high-impedance state to an invalid-data state prior to the specified access time.
C. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
D. $\overline{xCAS}$ order is arbitrary.

Figure 5. Read-Modify-Write-Cycle Timing

PRODUCT PREVIEW

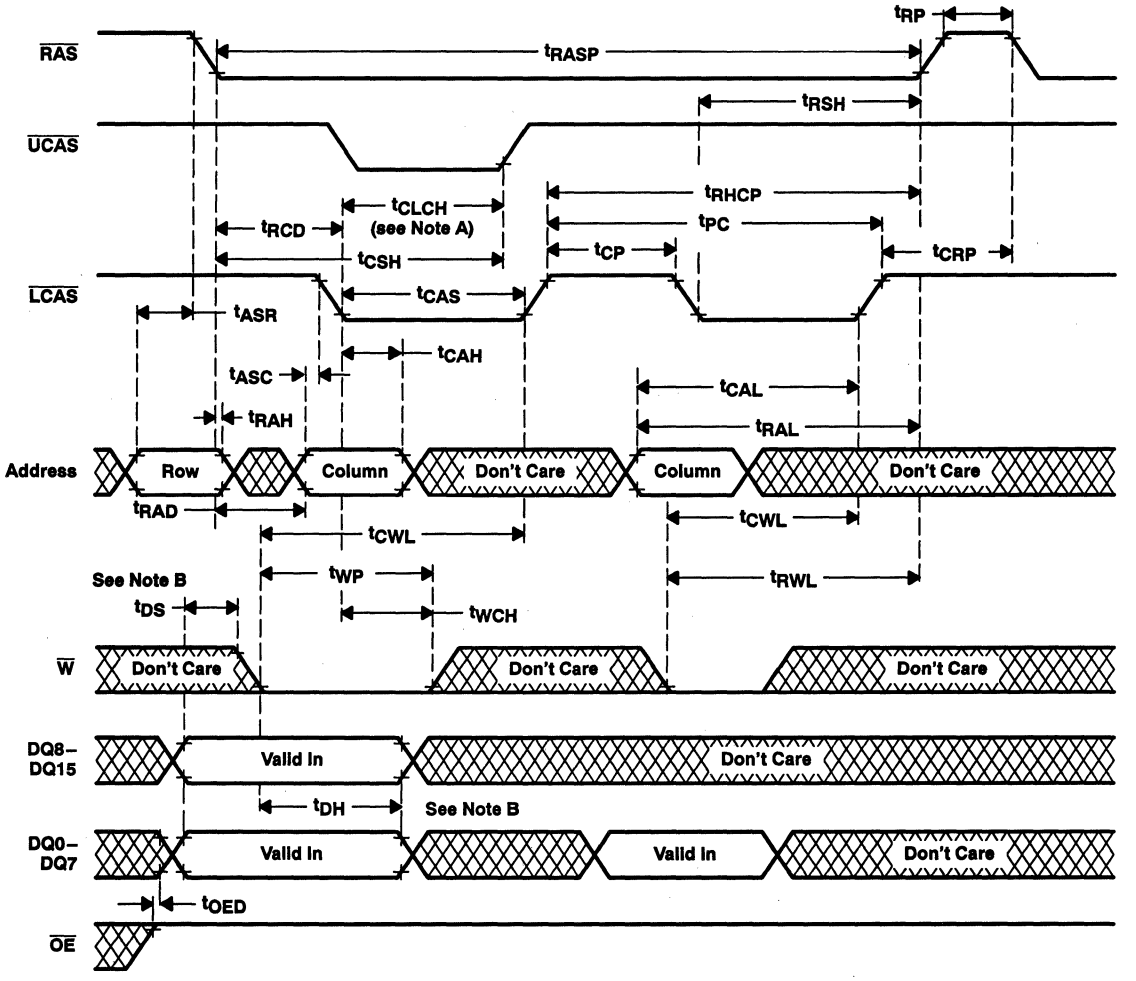
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. Access time is t_{CPA} or t_{AA} dependent.
D. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write- and read-modify-write-timing specifications are not violated.
F. $\overline{xCAS}$ order is arbitrary.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

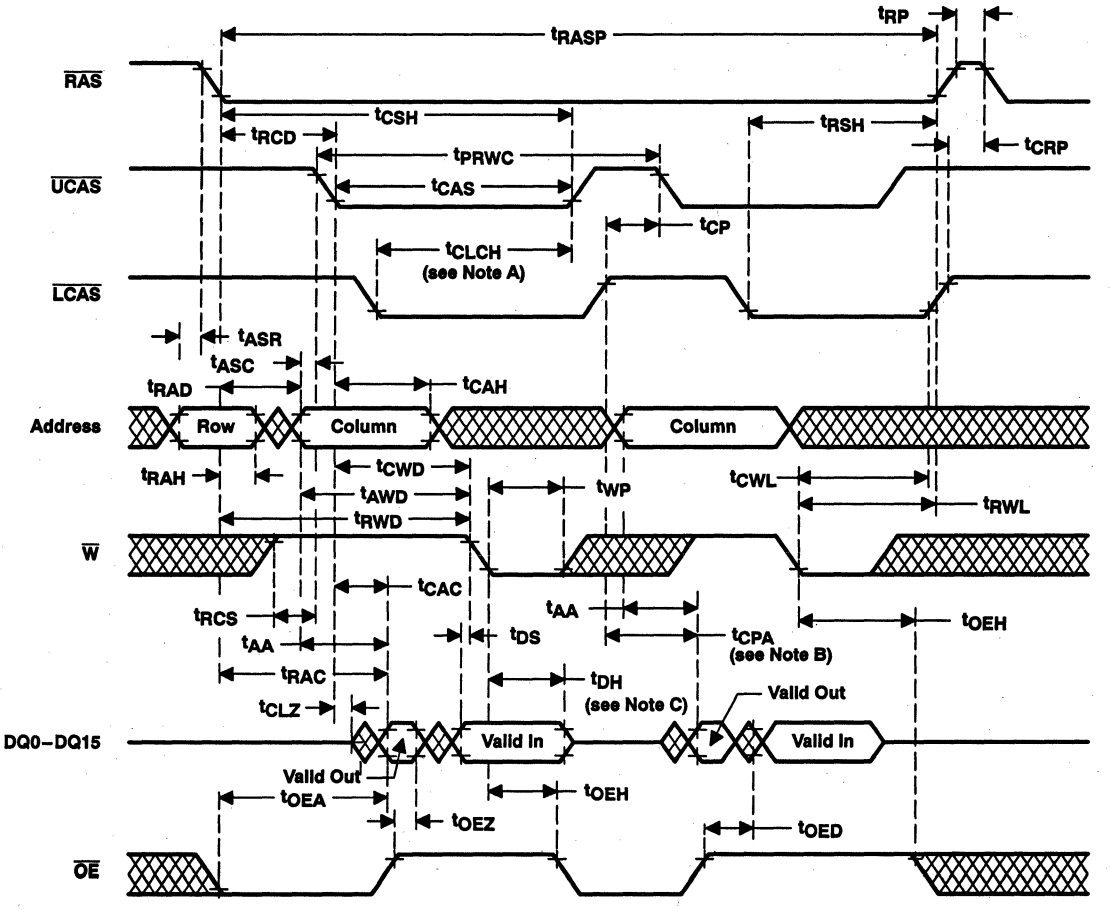


NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last
C. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read- and read-modify-write-timing specifications are not violated.
D. $\overline{xCAS}$ order is arbitrary.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

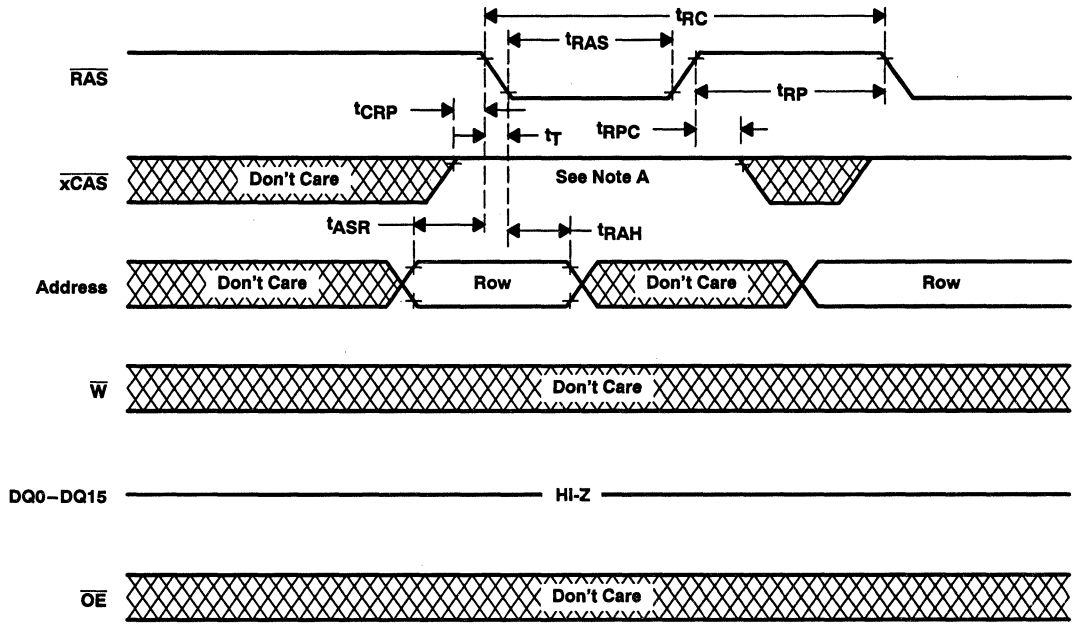


NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Access time is t_{CPA} or t_{AA} dependent.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. $\overline{xCAS}$ order is arbitrary.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read- and write-cycle timing specifications are not violated.
F. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.

Figure 8. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTE A: All xCAS must be high.

Figure 9. RAS-Only Refresh-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

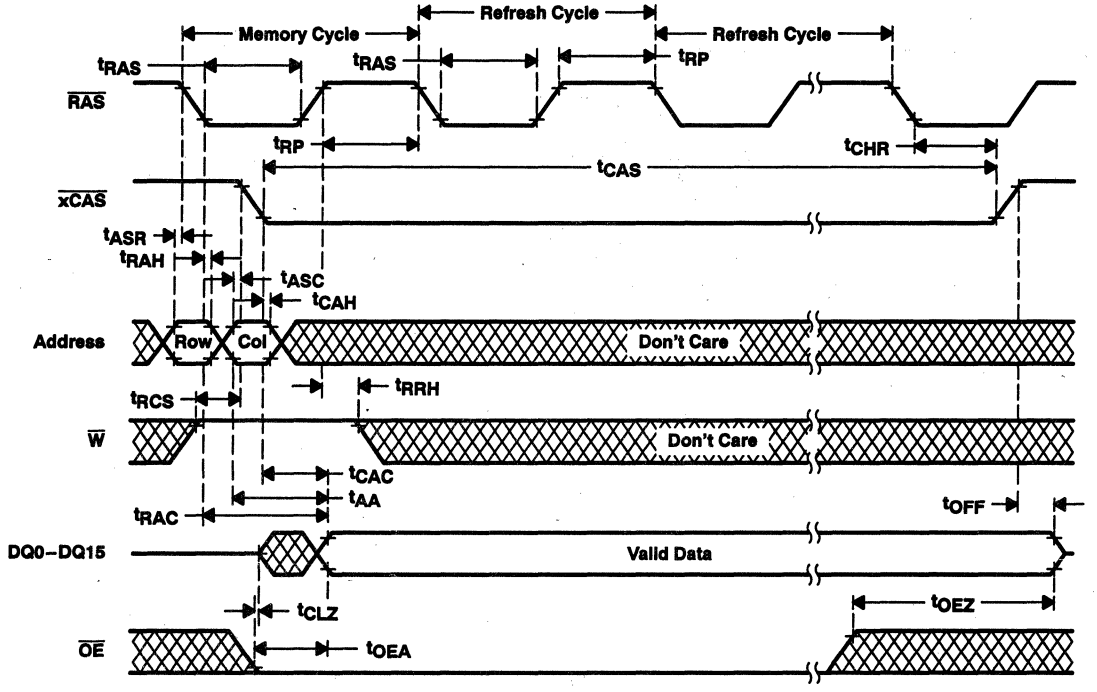
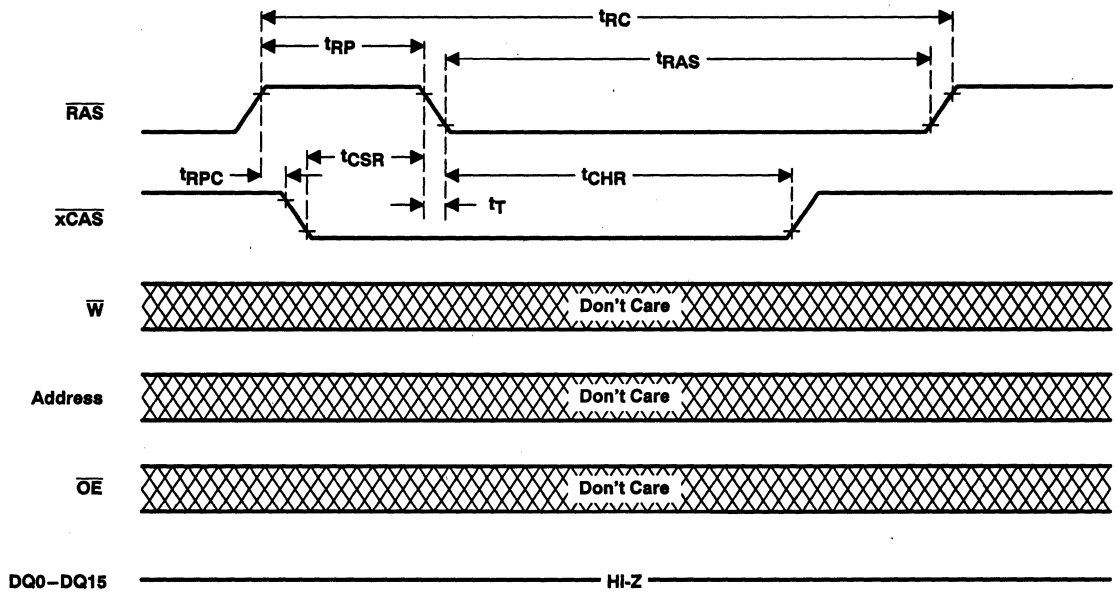


Figure 10. Hidden-Refresh-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTE A: Any $\overline{xCAS}$ can be used.

Figure 11. Automatic-CBR-Refresh-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

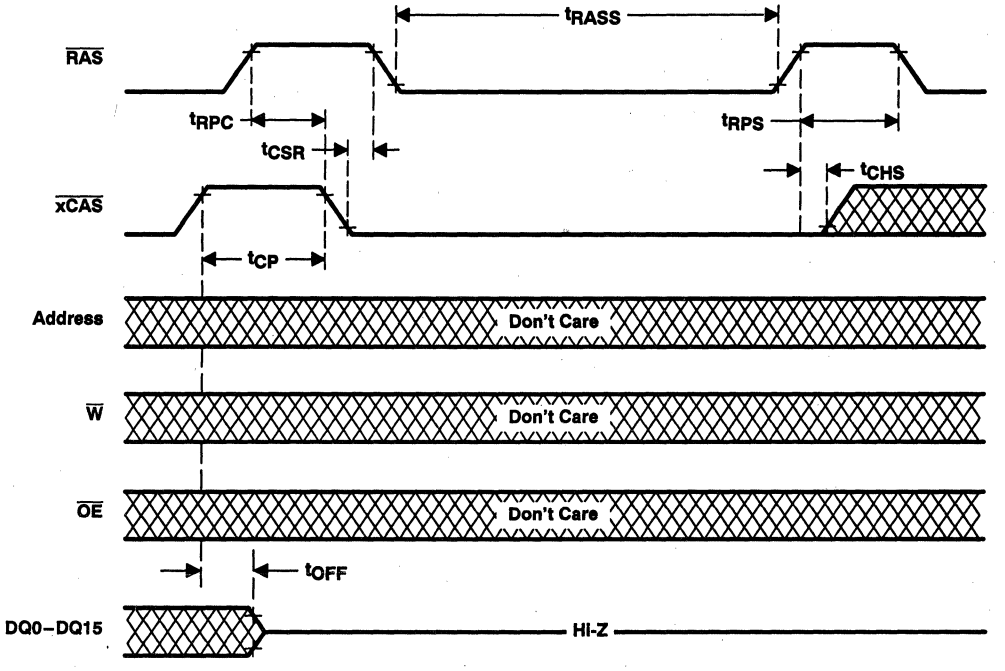
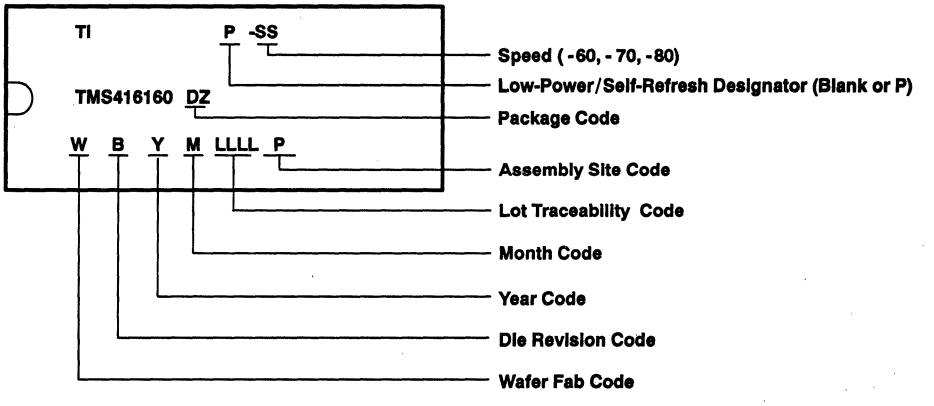


Figure 12. Self-Refresh-Cycle Timing

device symbolization (TMS416160P illustrated)



PRODUCT PREVIEW

This data sheet is applicable to all TMS464400/P, TMS464800/P, and TMS464160/P devices symbolized with Revision "A" and subsequent revisions as described on page 4-189.

- **Organization**
  16777216 × 4 TMS464400, TMS464400P
  8388608 × 8 TMS464800, TMS464800P
  4194304 × 16 TMS464160, TMS464160P
- **TMS464400/P and TMS464800/P in High-Reliability Plastic 32-Lead 400-Mil-Wide Surface-Mount (DZ) Package and 32-Lead Surface-Mount Thin Small-Outline Package (DGC)**
- **Low Power Dissipation**
  - **CMOS Standby**
  - **Extended Refresh**
  - **Battery Backup**
- **3-State Unlatched Outputs**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)	I_{CC1} OPERATING CURRENT (MIN)	I_{CC3} REFRESH CURRENT (MIN)
TMS464400/P-60	60 ns	15 ns	30 ns	110 ns	TBD mA	TBD mA
TMS464400/P-70	70 ns	18 ns	35 ns	130 ns	TBD mA	TBD mA
TMS464400/P-80	80 ns	20 ns	40 ns	150 ns	TBD mA	TBD mA
TMS464800/P-60	60 ns	15 ns	30 ns	110 ns	120 mA	120 mA
TMS464800/P-70	70 ns	18 ns	35 ns	130 ns	110 mA	110 mA
TMS464800/P-80	80 ns	20 ns	40 ns	150 ns	100 mA	100 mA
TMS464160/P-60	60 ns	15 ns	30 ns	110 ns	TBD mA	TBD mA
TMS464160/P-70	70 ns	18 ns	35 ns	130 ns	TBD mA	TBD mA
TMS464160/P-80	80 ns	20 ns	40 ns	150 ns	TBD mA	TBD mA

- **All Inputs, Outputs, and Clocks Are LVTTL Compatible**
- **Enhanced Page-Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  - **4096-Cycle CBR Refresh In 64 ms (max)**
  - **8192-Cycle $\overline{RAS}$-Only Refresh In 64 ms (max)**
- **Low-Power, Self-Refresh Version (TMS464400P, TMS464800P, TMS464160P)**
- **Single 3.3-V Power Supply (±0.3 V Tolerance)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Fully Compatible With 64-Megabit DRAM Specification From Hitachi**
- **Texas Instruments EPIC™ CMOS Process**

PRODUCT PREVIEW

description

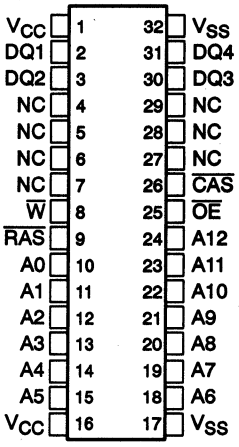
The TMS464400, TMS464800, TMS464160 series are high-speed, 67108864-bit dynamic random-access memories (DRAMS), organized as either 16 777 216 words of four bits each (TMS464400), 8388608 words of eight bits each (TMS464800), or 4194304 words of 16 bits each (TMS464160).

The TMS464400P, TMS464800P, and TMS464160P series are high-speed, low-voltage, low-power, self-refresh and extended-refresh, 67108864-bit DRAMS, organized as either 16 777 216 words of four bits each (TMS464400P), 8388608 words of eight bits each (TMS464800P), or 4194304 words of 16 bits each (TMS464160P).

The TMS464400/P and TMS464800/P are offered in a 400-mil 32-lead plastic surface-mount SOJ package (DZ suffix) and a 32-lead plastic surface-mount thin small-outline TSOP package (DGC suffix). The TMS464160/P packages are still being discussed by JEDEC. All packages are characterized for operation from 0°C to 70°C.

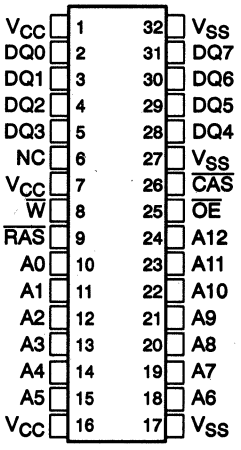
EPIC is a trademark of Texas Instruments Incorporated.

TMS464400
DZ, DGC PACKAGES
(TOP VIEW)



PIN NOMENCLATURE	
A0–A12	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	3.3-V Supply
V_{SS}	Ground

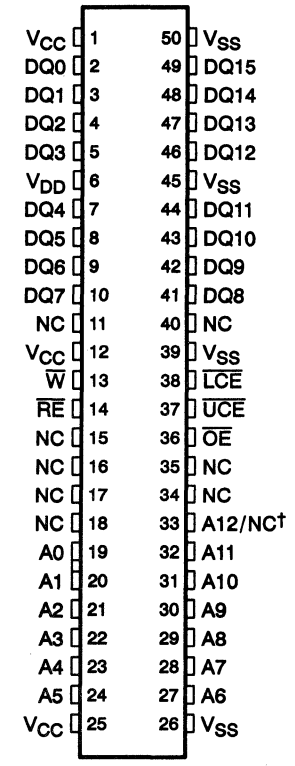
TMS464800
DZ, DGC PACKAGES
(TOP VIEW)



PIN NOMENCLATURE	
A0–A12	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ7	Data In/Data Out
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	3.3-V Supply
V_{SS}	Ground

PRODUCT PREVIEW

TMS464160DZ, DGC PACKAGE
(TOP VIEW)



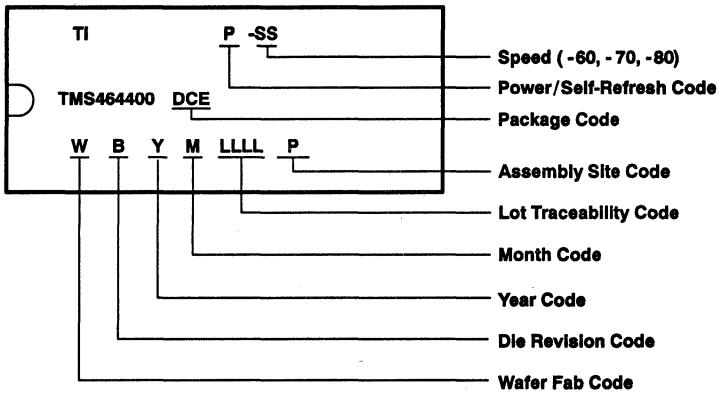
PIN NOMENCLATURE	
A0–A12†	Address Inputs
CAS or LCE, UCE	Column-Address Strobe
DQ0–DQ15	Data In/Data Out
NC	No Internal Connection
OE	Output Enable
RAS	Row-Address Strobe
RE	Read Enable
W	Write Enable
VCC	3.3-V Supply
VSS	Ground

Table 1. TMS464160 Refresh Configuration

	4K REFRESH†	8K REFRESH†
Row/refresh addresses	A0–A11	A0–A12
Column addresses	A0–A9	A0–A8

† Pin 33 is A12 for 8K refresh and NC for 4K refresh. CBR refresh is strongly recommended for this device.

device symbolization (TMS464400P illustrated)



PRODUCT PREVIEW

1048576-WORD BY 16-BIT EXTENDED DATA OUT HIGH-SPEED DRAMS

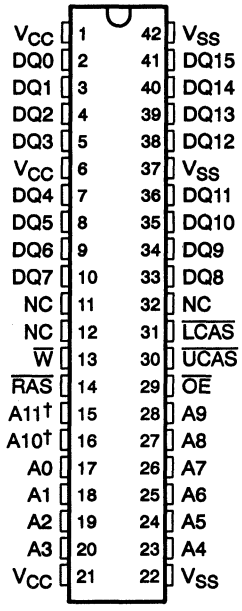
SMKS886A – APRIL 1995 – REVISED JUNE 1995

- **Organization . . . 1048576 × 16**
- **Single Power Supply (5 V or 3.3 V)**
- **Performance Ranges:**

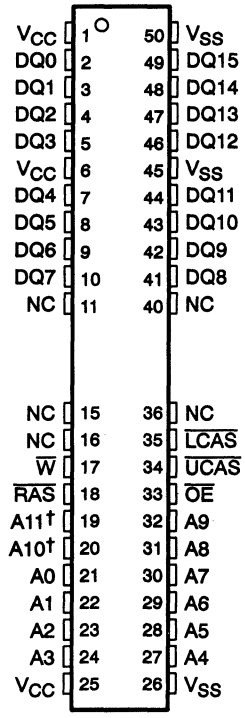
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR EDO CYCLE MIN
'4xx169/P-60	60 ns	15 ns	30 ns	25 ns
'4xx169/P-70	70 ns	18 ns	35 ns	30 ns
'4xx169/P-80	80 ns	20 ns	40 ns	35 ns

- **Extended Data Out (EDO) Operation**
- **$\overline{\text{xCAS}}$-Before-$\overline{\text{RAS}}$ (xCBR) Refresh**
- **Long Refresh Period and Self-Refresh Option (TMS4xx169P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **High-Reliability Plastic 42-Lead (DZ Suffix) 400-Mil-Wide Surface-Mount (SOJ) Package and 44/50-Lead (DGE Suffix) Surface-Mount Thin Small-Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instrument Enhanced Performance Implanted CMOS (EPIC™) Process**

DZ PACKAGE (TOP VIEW)



DGE PACKAGE (TOP VIEW)



† A10 and A11 are NC for TMS4x8169 and TMS4x8169P.

AVAILABLE OPTIONS

DEVICE	POWER SUPPLY	SELF REFRESH, BATTERY BACKUP	REFRESH CYCLES
TMS416169	5 V	—	4096 in 64 ms
TMS416169P	5 V	Yes	4096 in 128 ms
TMS418169	5 V	—	1024 in 16 ms
TMS418169P	5 V	Yes	1024 in 128 ms
TMS426169	3.3 V	—	4096 in 64 ms
TMS426169P	3.3 V	Yes	4096 in 128 ms
TMS428169	3.3 V	—	1024 in 16 ms
TMS428169P	3.3 V	Yes	1024 in 128 ms

PIN NOMENCLATURE

A0–A11	Address Inputs
DQ0–DQ15	Data In/Data Out
$\overline{\text{LCAS}}$	Lower Column-Address Strobe
$\overline{\text{UCAS}}$	Upper Column-Address Strobe
NC	No Internal Connection
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row-Address Strobe
V_{CC}	5-V or 3.3-V Supply‡
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

‡ See Available Options Table.

description

The TMS4xx169 series is a set of high-speed, 16777216-bit dynamic random-access memories (DRAMs) organized as 1048576 words of 16 bits each. The TMS4xx169P series is a similar set of high-speed, low-power, self-refresh, 16777216-bit DRAMs organized as 1048576 words of 16 bits each. Both sets employ state-of-the-art EPIC™ technology for high performance, reliability, and low power at low cost.

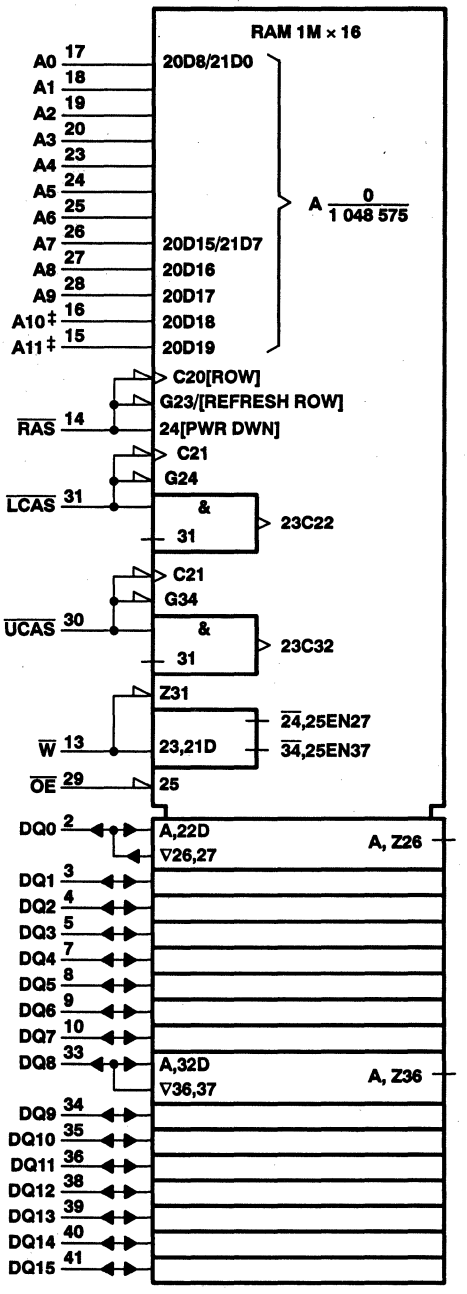
These devices feature maximum $\overline{\text{RAS}}$ access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4xx169 and TMS4xx169P are offered in a 44/50-lead plastic surface-mount TSOP (DGE suffix) and a 42-lead plastic surface-mount SOJ (DZ suffix) package. These packages are characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

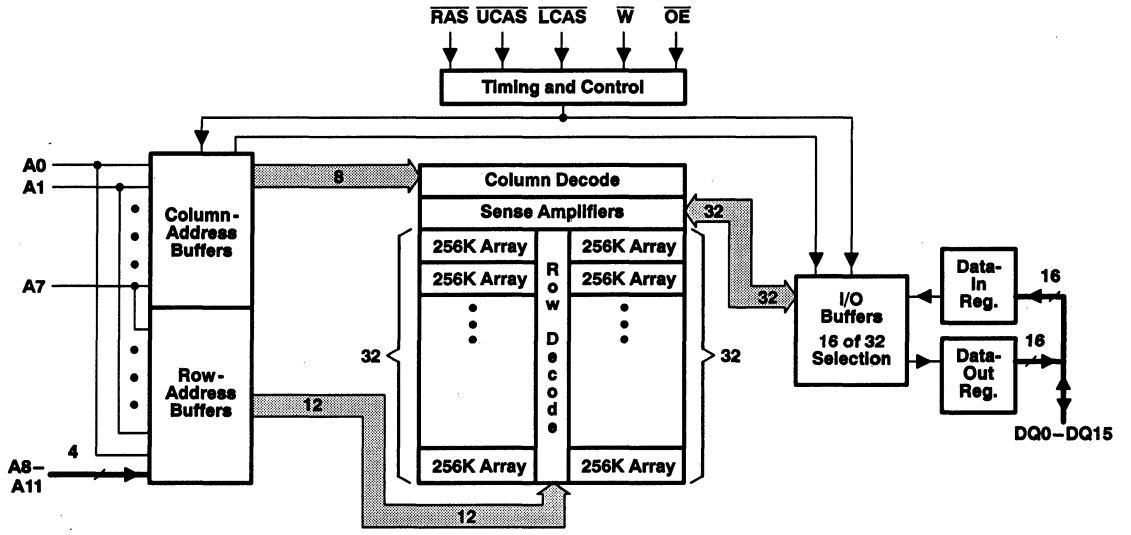
PRODUCT PREVIEW

logic symbol†



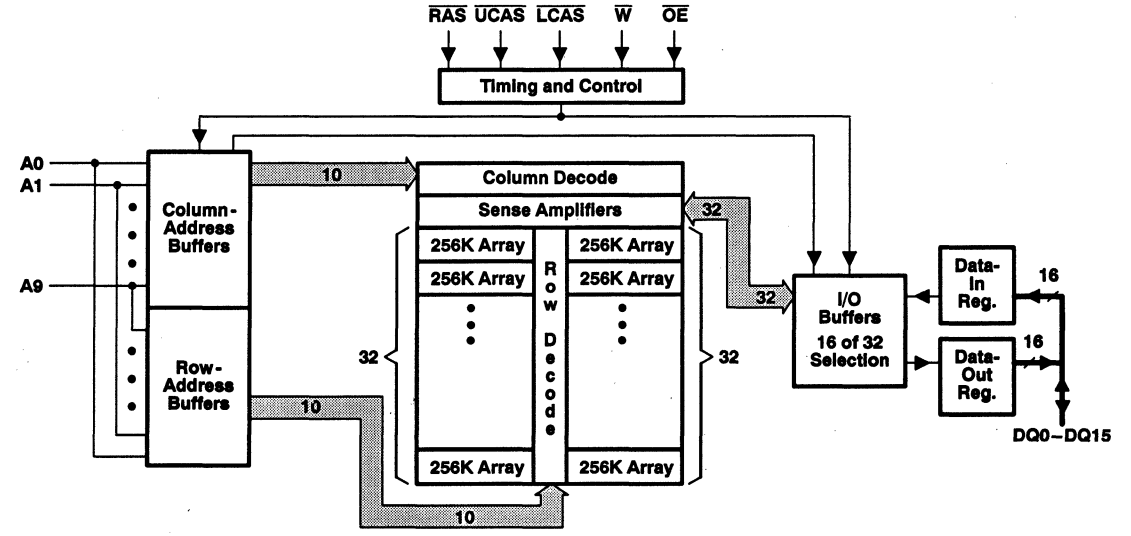
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the DZ package.
‡ A10 and A11 are NC for TMS4x8169 and TMS4x8169P.

functional block diagram (TMS4x6169/P)



(a) TMS4x6169, TMS4x6169P

functional block diagram (TMS4x8169/P)



(b) TMS4x8169, TMS4x8169P

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operation

dual $\overline{CAS}$

Two $\overline{CAS}$ pins ($\overline{LCAS}$ and $\overline{UCAS}$) are provided to give independent control of the 16 data-I/O pins (DQ0–DQ15), with $\overline{LCAS}$ corresponding to DQ0–DQ7 and $\overline{UCAS}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{xCAS}$ falling edge. Each $\overline{xCAS}$ going low enables its corresponding DQx pin with data associated with the column address latched on the first falling $\overline{xCAS}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{xCAS}$ edge. The delay time from $\overline{xCAS}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{xCAS}$ to its corresponding DQx pin.

In order to latch in a new column address, both $\overline{xCAS}$ pins must be brought high. The column-precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first $\overline{xCAS}$ falling edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

For early-write cycles, the data is latched on the first $\overline{xCAS}$ falling edge. Only the DQs that have the corresponding $\overline{xCAS}$ low are written into. Each $\overline{xCAS}$ must meet t_{CAS} minimum in order to ensure writing into the storage cell. To latch a new address and new data, all $\overline{xCAS}$ pins must be high and meet t_{CP}.

extended data out

Extended data out (EDO) allows for data output rates of up to 40 MHz for 60-ns devices. When keeping the same row address while selecting random column addresses, the time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP}, the maximum $\overline{RAS}$ low time.

EDO does not enter the DQs into the high-impedance state with the rising edge of $\overline{xCAS}$. The output remains valid for the system to latch the data. After $\overline{xCAS}$ goes high, the DRAM is decoding the next address. $\overline{OE}$ and $\overline{W}$ can be used to control the output impedance. Descriptions of $\overline{OE}$ and $\overline{W}$ further explain EDO operation benefit.

address: A0–A11 (TMS4x6169, TMS4x6169P) and A0–A9 (TMS4x8169, TMS4x8169P)

Twenty address bits are required to decode a single one of the 1048576 storage cell locations. For the TMS4x6169 and TMS4x6169P, 12 row-address bits are set up on A0 through A11 and latched onto the chip by $\overline{RAS}$. Eight column-address bits are set up on A0 through A7 and latched on the chip by the first $\overline{xCAS}$. For the TMS4x8169 and TMS4x8169P, 10 row-address bits are set up on A0–A9 and latched on the chip by $\overline{RAS}$. Ten column-address bits are set up on A0–A9 and latched on the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip-enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip-select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation independent of the state of $\overline{OE}$. This permits early-write operation to be completed with $\overline{OE}$ grounded. If $\overline{W}$ goes low in an extended-data-out read cycle, the DQs go into the high-impedance state as long as $\overline{xCAS}$ is high.

data In (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{xCAS}$ and the data is strobed in by the first occurring $\overline{xCAS}$ with setup and hold times referenced to this signal. In a

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data in (DQ0–DQ15) (continued)

delayed-write or read-modify-write cycle, $\overline{xCAS}$ is already low and the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

data out (DQ0–DQ15)

Data out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. While $\overline{xCAS}$ and $\overline{RAS}$ are low and $\overline{W}$ is high, $\overline{OE}$ can be brought low or high and the DQs transition between valid data and high impedance. There are two methods for placing the DQs into the high-impedance state and keeping them that way during $\overline{xCAS}$ high time using $\overline{OE}$. The first method is to transition $\overline{OE}$ high before $\overline{xCAS}$ transitions high and keep $\overline{OE}$ high for t_{CHO} past the $\overline{CAS}$ transition. This disables the DQs and they remain in the high-impedance state, regardless of $\overline{OE}$, until $\overline{xCAS}$ falls again. The second method is to have $\overline{OE}$ low as $\overline{xCAS}$ transitions high. Then $\overline{OE}$ can pulse high for a minimum of t_{OEP} anytime during $\overline{CAS}$ high time disabling the DQs regardless of further transitions on $\overline{OE}$ until $\overline{CAS}$ falls again.

$\overline{RAS}$-only refresh

TMS4x6169, TMS4x6169P

A refresh operation must be performed at least once every 64 ms (256 ms for TMS4x6169P) to retain data. This is achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding both $\overline{xCAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

TMS4x8169, TMS4x8169P

A refresh operation must be performed at least once every 16 ms (128 ms for TMS4x8169P) to retain data. This is achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding both $\overline{xCAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pins. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored and the refresh address is generated internally.

$\overline{xCAS}$-before-$\overline{RAS}$ (xCBR) refresh

xCBR refresh is achieved by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive xCBR refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

battery-backup refresh

TMS4x6169P

A low-power battery-backup refresh mode that requires less than 600 µA (5 V) or 350 µA (3.3 V) refresh current is available on the TMS4x6169P. Data integrity is maintained using xCBR refresh with a period of 31.25 µs while holding $\overline{RAS}$ low for less than 300 ns. To minimize current consumption, all input levels must be at CMOS levels (V_{IL} < 0.2 V, V_{IH} > V_{CC} – 0.2 V).

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TMS4x8169P

A low-power battery-backup refresh mode that requires less than 600 μA (5 V) or 350 μA (3.3 V) refresh current is available on the TMS4x8169P. Using xCBR refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 300 ns maintains data integrity. To minimize current consumption, all input levels must be at CMOS levels (V_{IL} < 0.2 V, V_{IH} > V_{CC} – 0.2 V).

self-refresh (TMS4xx169P)

The self-refresh mode is entered by dropping $\overline{xCAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{xCAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{xCAS}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power-up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power-up to the full V_{CC} level. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or xCBR) cycle.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: TMS41x169, TMS41x169P ..... – 1 V to 7 V
TMS42x169, TMS42x169P ..... – 0.5 V to 4.6 V
Voltage range on any pin (see Note 1): TMS41x169, TMS41x169P ..... – 1 V to 7 V
TMS42x169, TMS42x169P ..... – 0.5 V to 4.6 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		'41x169			'42x169			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	3	3.3	3.6	V
V_{SS}	Supply voltage		0			0		V
V_{IH}	High-level input voltage	2.4		6.5	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

TMS416169/P

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'416169-60 '416169P-60		'416169-70 '416169P-70		'416169-80 '416169P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle			90		80		70	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'416169		1		1		1	mA
			'416169P		500		500		500	µA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			90		80		70	mA
I_{CC4}‡¶	Average EDO current	V_{CC} = 5.5 V, t_{HPC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			100		90		80	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			500		500		500	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms); CBR only	t_{RC} = 31.25 µs, t_{RAS} ≤ 300 ns, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			600		600		600	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}
# For TMS416169P only

PRODUCT PREVIEW

TMS418169/P

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†		'418169-60 '418169P-60		'418169-70 '418169P-70		'418169-80 '418169P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle			190		180		170	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'418169		1		1		1	mA
			'418169P		500		500		500	µA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			190		180		170	mA
I_{CC4}‡¶	Average EDO current	V_{CC} = 5.5 V, t_{HPC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			100		90		80	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			500		500		500	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms); CBR only	t_{RC} = 125 µs, t_{RAS} ≤ 300 ns, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			600		600		600	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}
# For TMS418169P only

PRODUCT PREVIEW

TMS426169/P

electrical characteristics over recommended ranges of supply voltage and operating free-air conditions (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†		'426169-60 '426169P-60 MIN	'426169-60 '426169P-60 MAX	'426169-70 '426169P-70 MIN	'426169-70 '426169P-70 MAX	'426169-80 '426169P-80 MIN	'426169-80 '426169P-80 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 3.6 V, Minimum cycle			90		80		70	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			1		1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'426169		500		500		500	µA
			'426169P		200		200		200	µA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$-only refresh) $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			90		80		70	mA
I_{CC4}‡¶	Average EDO current	V_{CC} = 3.6 V, t_{HPC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			100		90		80	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			250		250		250	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms), CBR only	t_{RC} = 31.25 µs, t_{RAS} ≤ 300 ns, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}
# For TMS426169P only

PRODUCT PREVIEW

TMS428169/P

electrical characteristics over recommended ranges of supply voltage and operating free-air conditions (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†		'428169-60 '428169P-60 MIN	'428169-60 '428169P-60 MAX	'428169-70 '428169P-70 MIN	'428169-70 '428169P-70 MAX	'428169-80 '428169P-80 MIN	'428169-80 '428169P-80 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = –100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 3.6 V, Minimum cycle			190		180		170	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			1		1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'428169		500		500		500	µA
			'428169P		200		200		200	µA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$-only refresh) $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			190		180		170	mA
I_{CC4}‡¶	Average EDO current	V_{CC} = 3.6 V, t_{HPC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			100		90		80	mA
I_{CC6}#	Self-refresh current	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			250		250		250	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms), CBR only	t_{RC} = 125 µs, t_{RAS} ≤ 300 ns, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}
# For TMS428169P only

PRODUCT PREVIEW

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A11		5	pF
$C_{i(\overline{OE})}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{xCAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_O	Output capacitance		7	pF

NOTE 3: V_{CC} = 5 V ± 0.5 V or 3.3 V ± 0.3 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'4xx169-60 '4xx169P-60		'4xx169-70 '4xx169P-70		'4xx169-80 '4xx169P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 4)		30		35		40	ns
t_{CAC}	Access time from $\overline{xCAS}$ low (see Note 4)		15		18		20	ns
t_{CPA}	Access time from column precharge (see Note 4)		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low (see Note 4)		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low (see Note 4)		15		18		20	ns
t_{CLZ}	Delay time, $\overline{xCAS}$ low to output in low-impedance state	0		0		0		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 5)	3	15	3	18	3	20	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high (see Note 5)	3	15	3	18	3	20	ns
t_{CEZ}	Output disable time after $\overline{CAS}$ high (see Note 5)	3	15	3	18	3	20	ns
t_{WEZ}	Output disable time after $\overline{W}$ low (see Note 5)	3	15	3	18	3	20	ns

NOTES: 4. Access times for TMS42x169 are measured with output reference levels of V_{OH} = 2 V and V_{OL} = 0.8 V.
5. Maximum t_{REZ}, t_{CEZ}, t_{WEZ} and t_{OEZ} are specified when the output is no longer driven.

EDO timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4xx169-60		'4xx169-70		'4xx169-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page-mode read or write	25		30		35		ns
t_{PRWC}	Cycle time, EDO read-write	80		90		100		ns
t_{CSH}	Hold time, $\overline{xCAS}$ from $\overline{RAS}$	50		55		60		ns
t_{CHO}	Hold time, $\overline{OE}$ from $\overline{xCAS}$	10		10		10		ns
t_{DOH}	Hold time, output from $\overline{xCAS}$	3		3		3		ns
t_{CAS}	Pulse duration, $\overline{xCAS}$	10	10000	12	10000	15	10000	ns
t_{WPE}	Pulse duration, $\overline{W}$ (output disable only)	5		5		5		ns
t_{OCH}	Setup time, $\overline{OE}$ before $\overline{xCAS}$	10		10		10		ns
t_{CP}	Precharge time, $\overline{xCAS}$	5		5		5		ns
t_{OEP}	Precharge time, $\overline{OE}$	5		5		5		ns

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4xx169-60 '4xx169P-60		'4xx169-70 '4xx169P-70		'4xx169-80 '4xx169P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read (see Note 6)	110		130		150		ns
t_{WC}	Cycle time, write (see Note 6)	110		130		150		ns
t_{RWC}	Cycle time, read-write (see Note 6)	150		175		200		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 7)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 7)	60	10 000	70	10 000	80	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{xCAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 8)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{xCAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ high	10		12		15		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	10		12		15		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ low (early-write operation only)	0		0		0		ns
t_{CAH}	Hold time, column address after $\overline{xCAS}$ low	10		15		15		ns
t_{DH}	Hold time, data (see Note 8)	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{xCAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{xCAS}$ low (early-write operation only)	10		15		15		ns
t_{CLCH}	Hold time, $\overline{xCAS}$ low to $\overline{xCAS}$ high	5		5		5		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{xCAS}$ precharge	35		40		45		ns
t_{OEH}	Hold time, $\overline{OE}$ command	15		18		20		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	10		10		10		ns
t_{CHS}	Hold time, $\overline{xCAS}$ low after $\overline{RAS}$ high (self refresh)	–50		–50		–50		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)	55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high (xCBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{xCAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high	50		55		60		ns
t_{CSR}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ low (xCBR refresh only)	5		5		5		ns
t_{CWD}	Delay time, $\overline{xCAS}$ low to $\overline{W}$ low (read-write operation only)	40		46		50		ns
t_{OED}	Delay time, $\overline{OE}$ to data	15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{xCAS}$ high	20		25		30		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ low (see Note 10)	20	45	20	52	20	60	ns

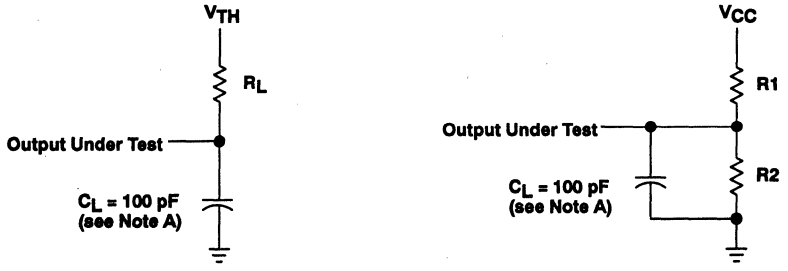
NOTES: 6. All cycle times assume t_T = 5 ns.
7. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
8. Referenced to the later of $\overline{xCAS}$ or $\overline{W}$ in write operations
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to assure access time.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			'4xx169-60 '4xx169P-60		'4xx169-70 '4xx169P-70		'4xx169-80 '4xx169P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{xCAS}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ high		10		12		15		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)		85		98		110		ns
t_{CPW}	Delay time, $\overline{W}$ low after $\overline{xCAS}$ precharge (read-write operation only)		60		68		75		ns
t_{RASS}	Pulse duration, self-refresh entry from $\overline{RAS}$ low		100		100		100		µs
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self refresh		110		130		150		ns
t_{REF}	Refresh time interval	'4x6169		64		64		64	ms
		'4x6169P		128		128		128	
		'4x8169		16		16		16	ms
		'4x8169P		128		128		128	
t_T	Transition time		2	30	2	30	2	30	ns

PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT (b) ALTERNATE LOAD CIRCUIT

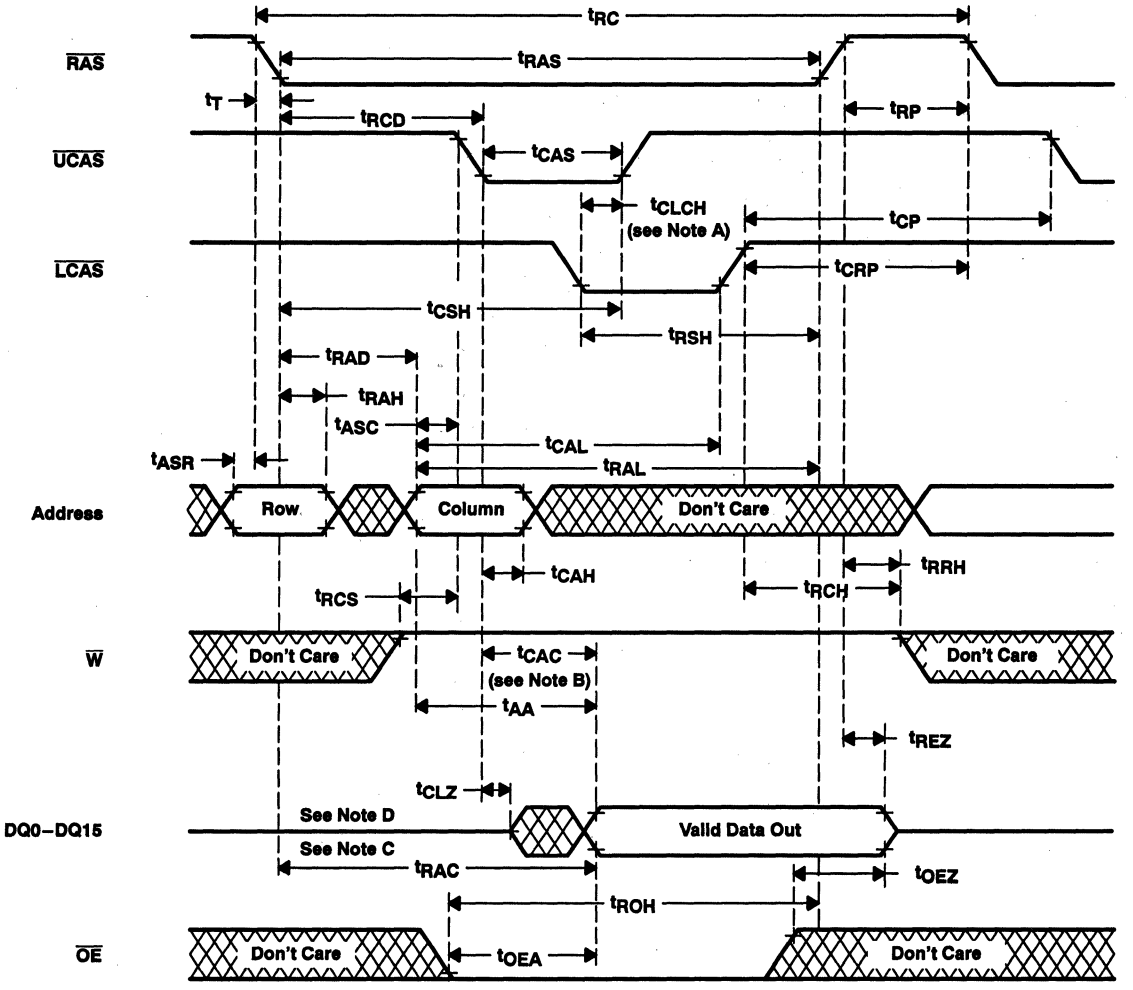
DEVICE	V_{CC} (V)	R1 (Ω)	R2 (Ω)	V_{TH} (V)	R_L (Ω)
41x169/P	5	828	295	1.31	218
42x169/P	3.3	1178	868	1.4	500

NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

PRODUCT PREVIEW

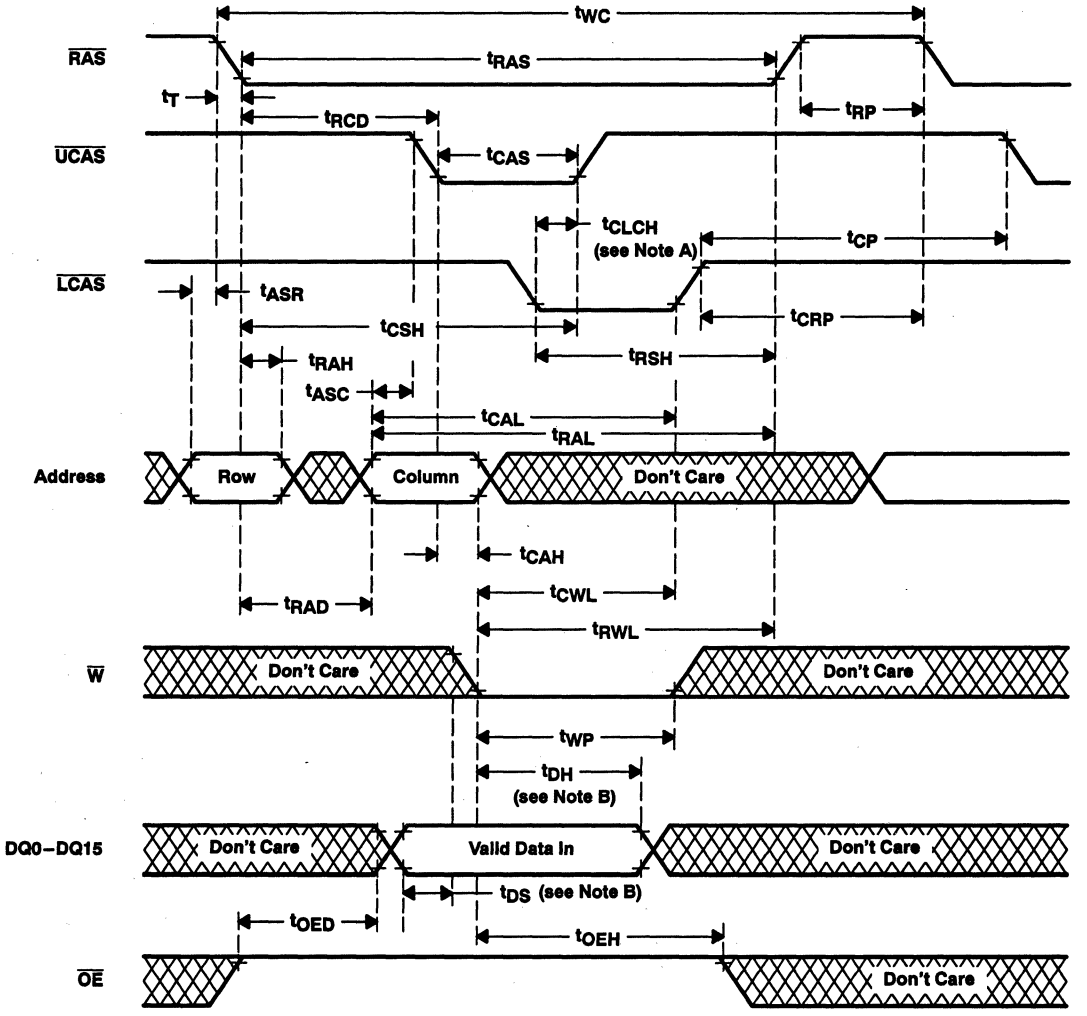
PARAMETER MEASUREMENT INFORMATION



NOTES: B. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
C. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
D. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
E. $\overline{xCAS}$ order is arbitrary.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last
C. $\overline{xCAS}$ order is arbitrary.

Figure 3. Write-Cycle Timing

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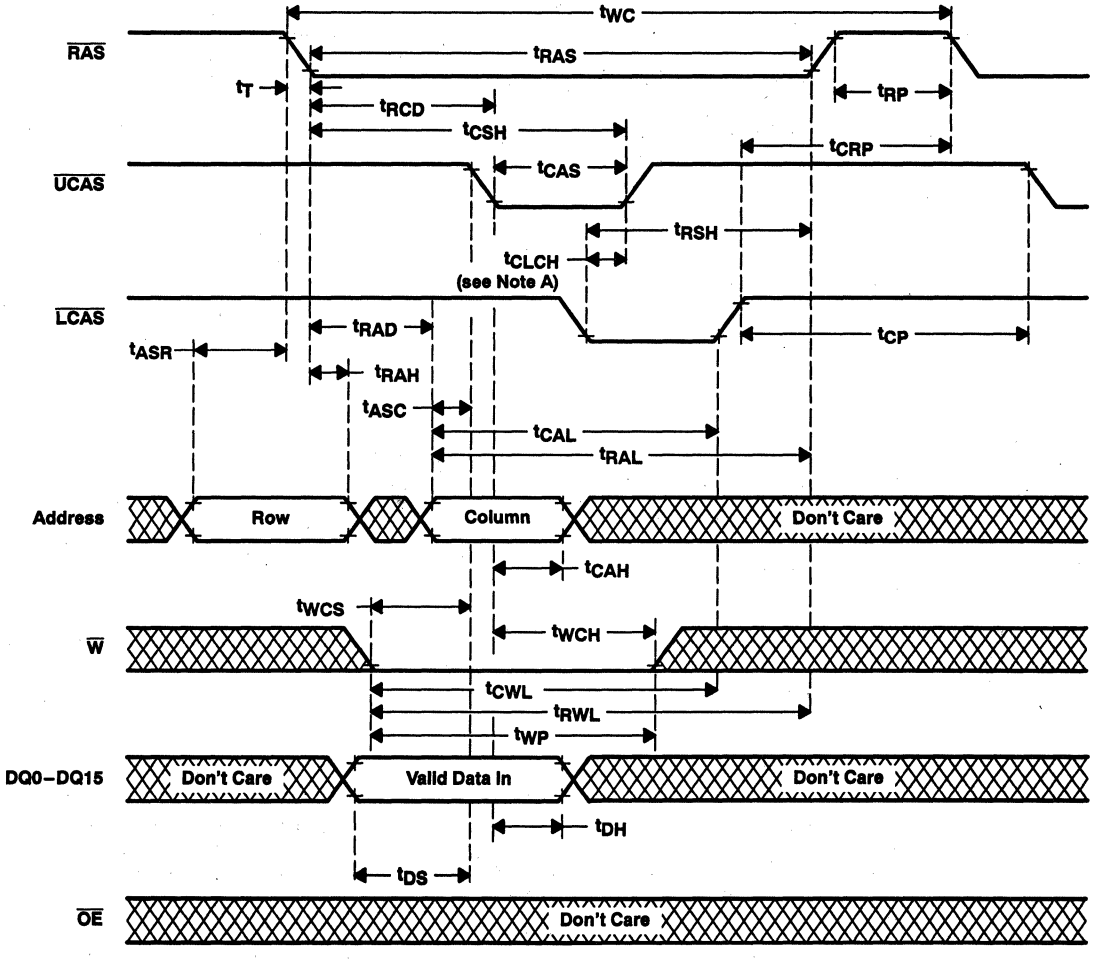
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.

Figure 4. Early-Write-Cycle Timing

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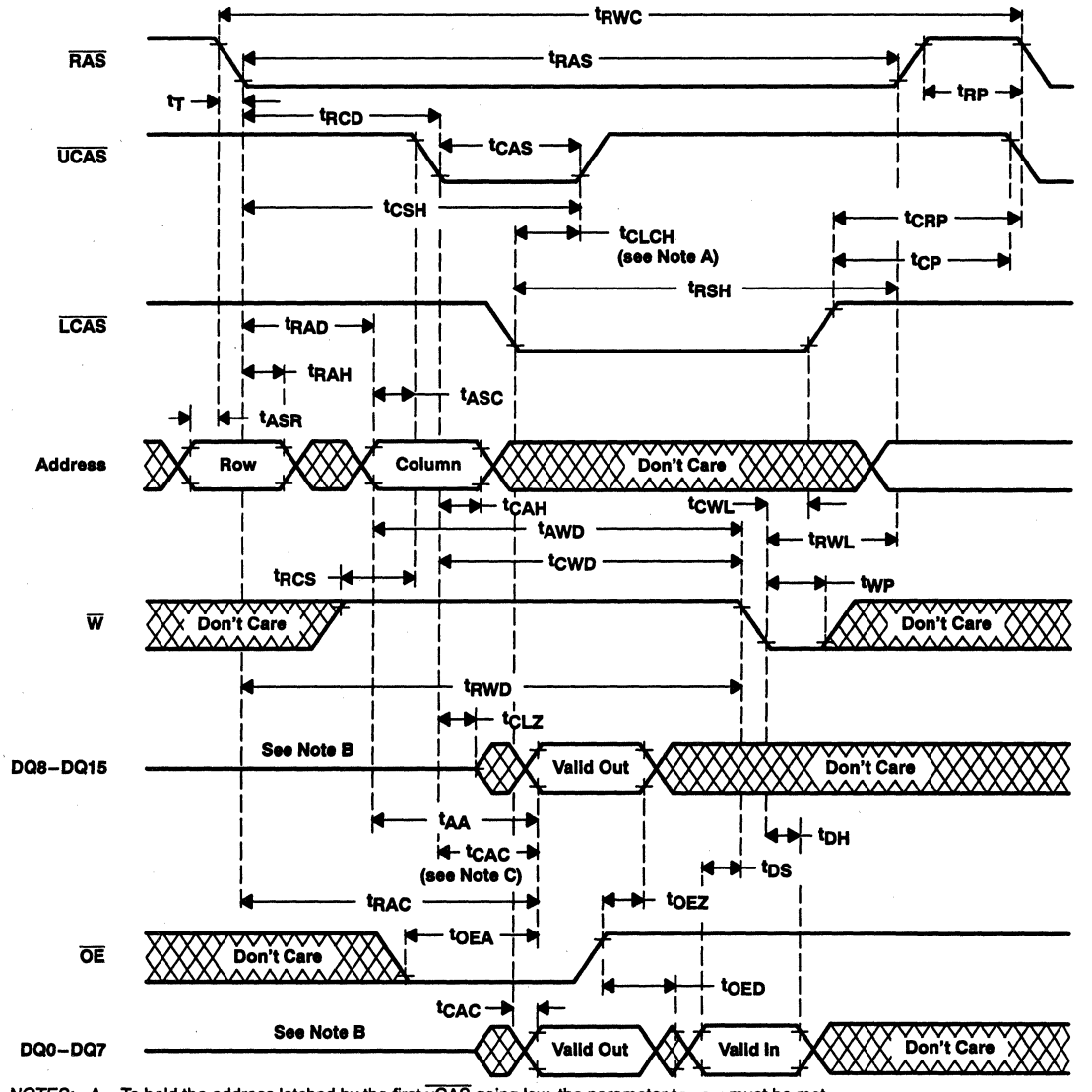
PARAMETER MEASUREMENT INFORMATION

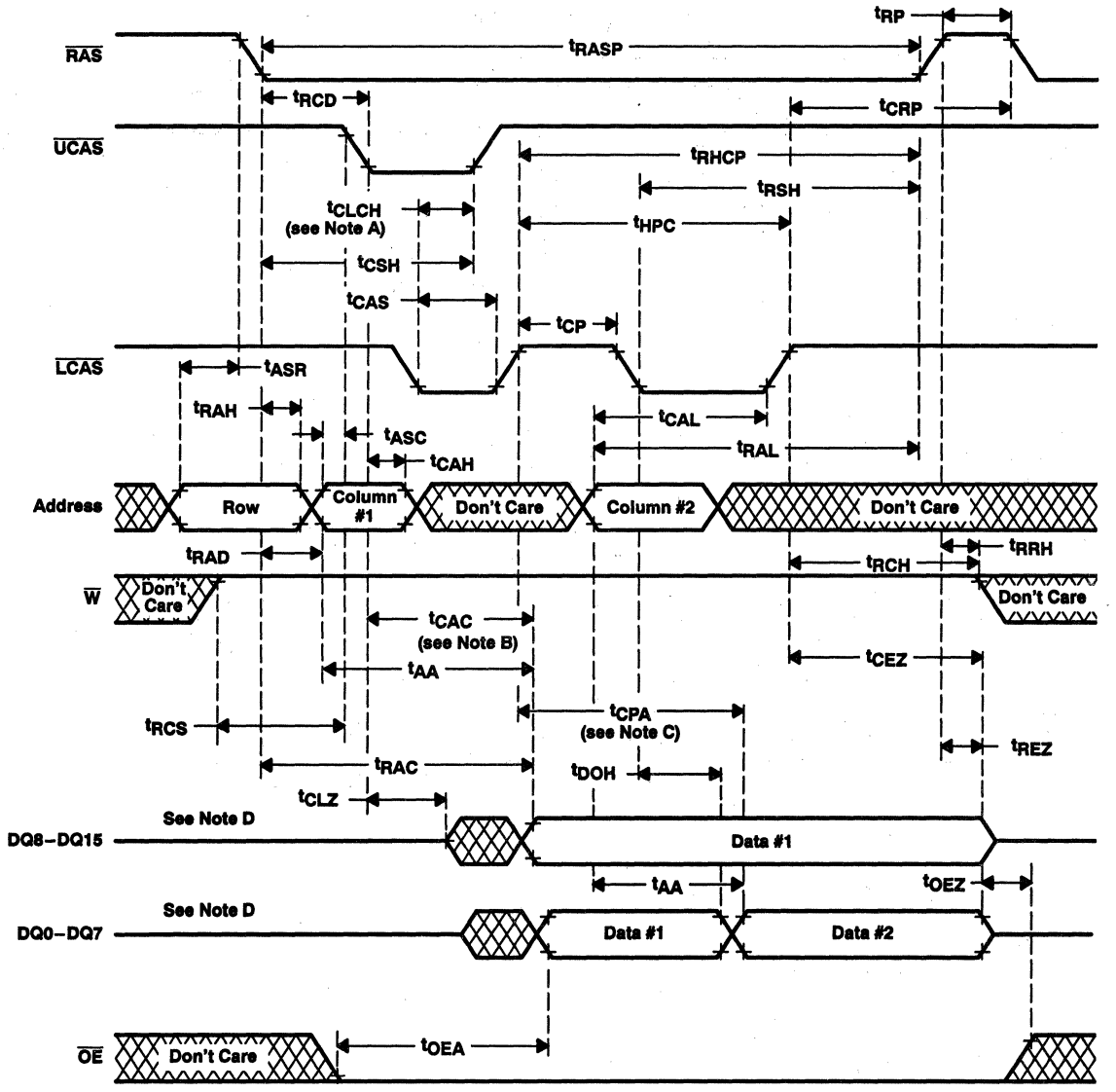


NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
C. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
D. $\overline{xCAS}$ order is arbitrary.

Figure 5. Read-Modify-Write-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. Access time is t_{CPA} or t_{AA} dependent.
D. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write- and read-modify-write-timing specifications are not violated.
F. $\overline{xCAS}$ order is arbitrary.

Figure 6. Extended-Data-Out Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

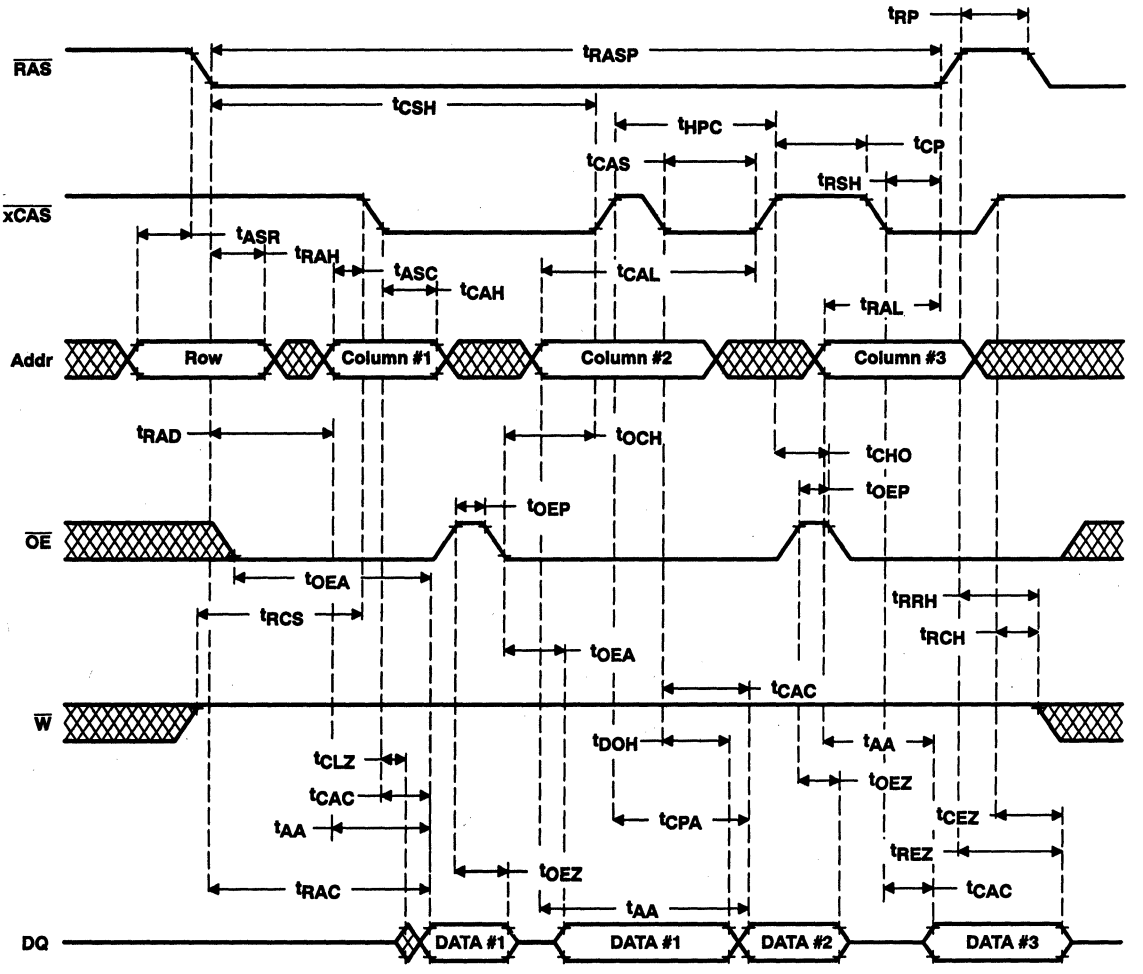


Figure 7. Extended-Data-Out Read-Cycle Timing With $\overline{OE}$ Control

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PARAMETER MEASUREMENT INFORMATION

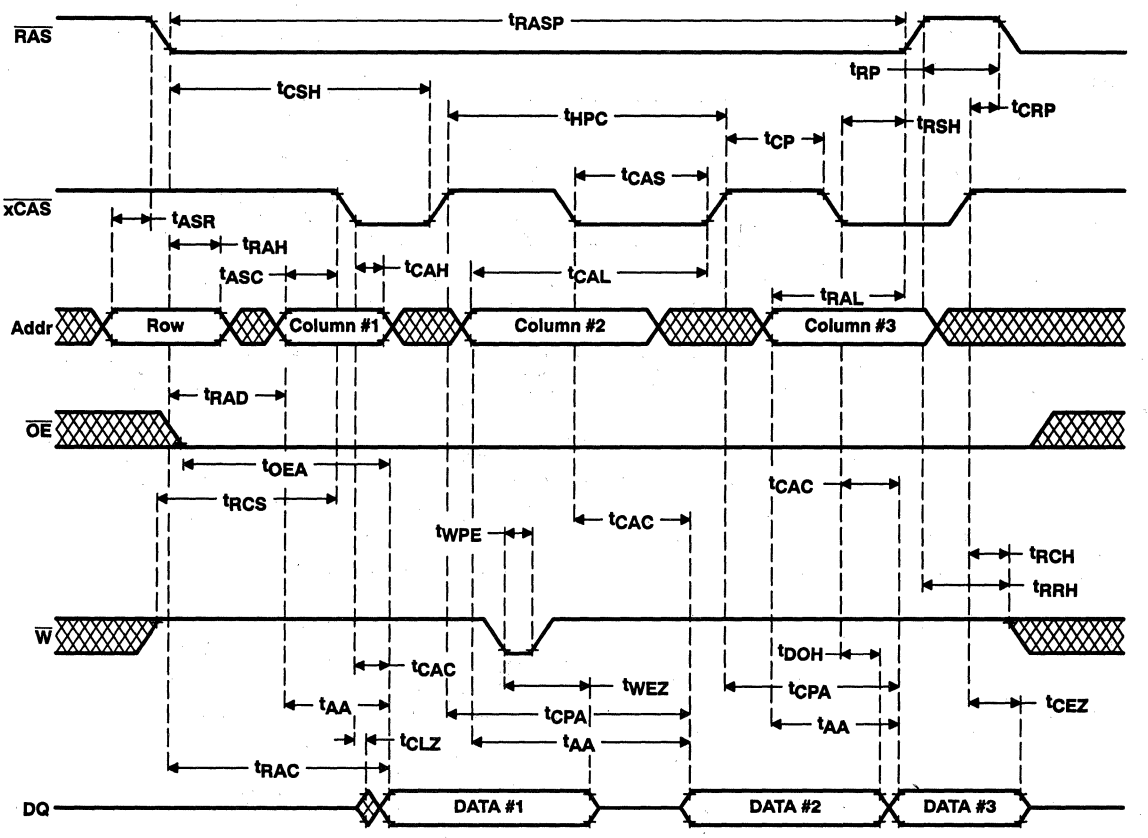
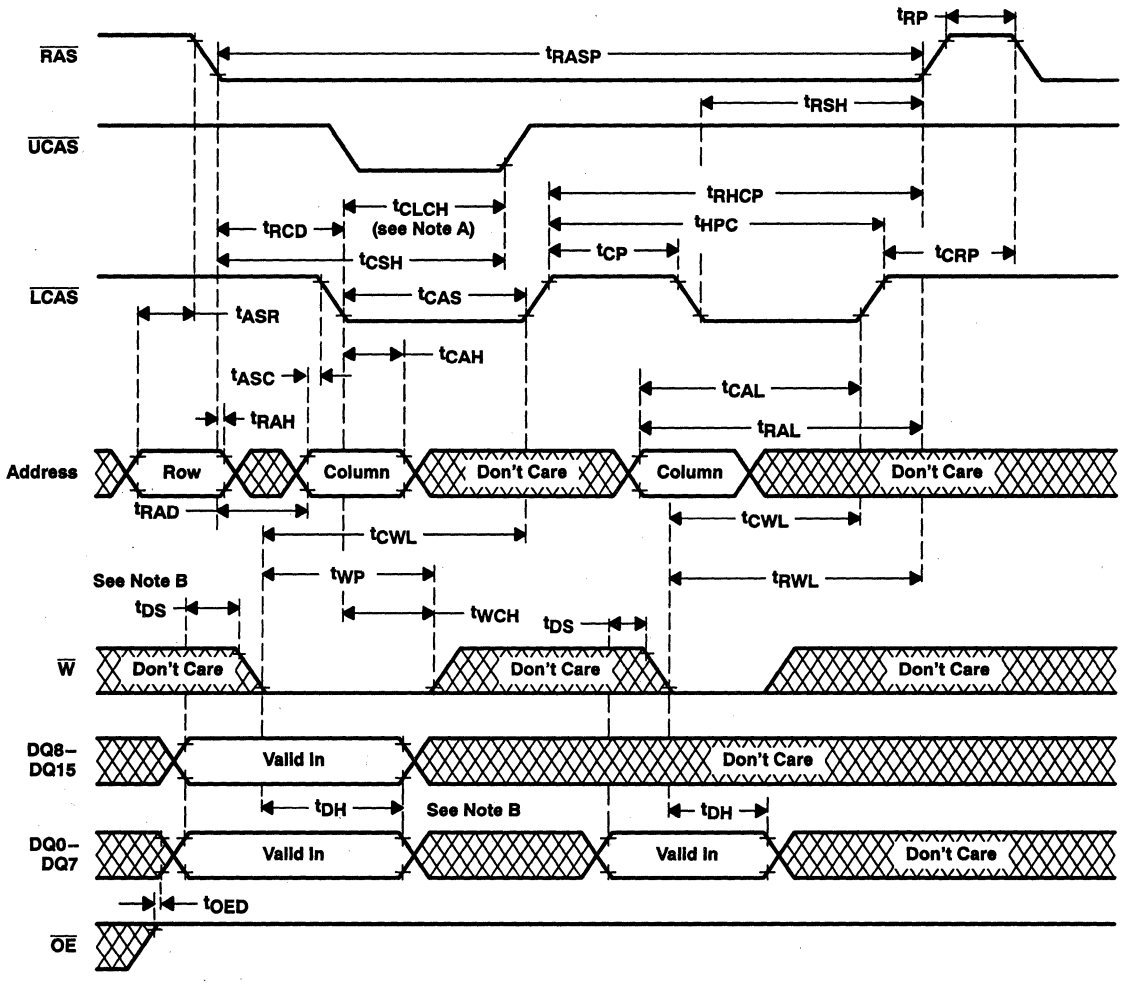


Figure 8. Extended-Data-Out Read-Cycle Timing With $\overline{W}$ Control

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last
C. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read- and read-modify-write-timing specifications are not violated.
D. $\overline{xCAS}$ order is arbitrary.

Figure 9. Extended-Data-Out Write-Cycle Timing

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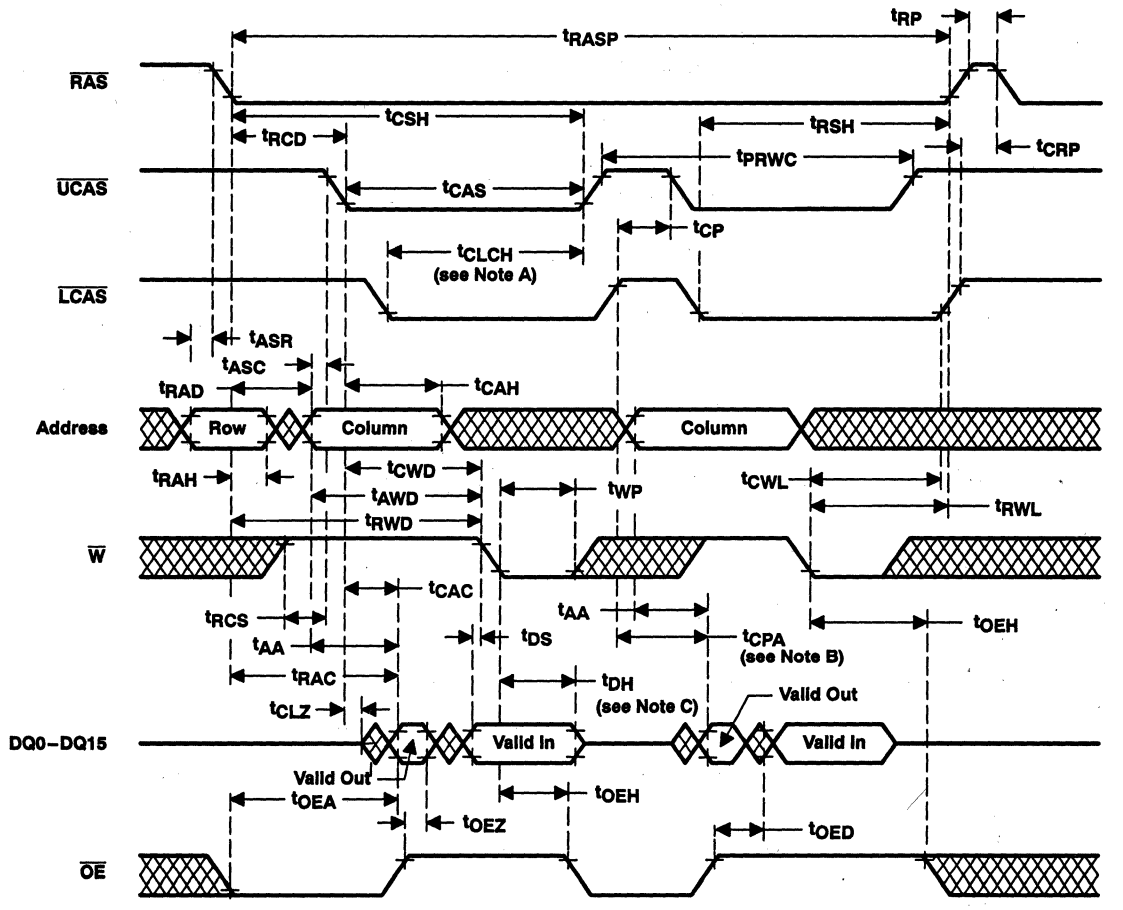
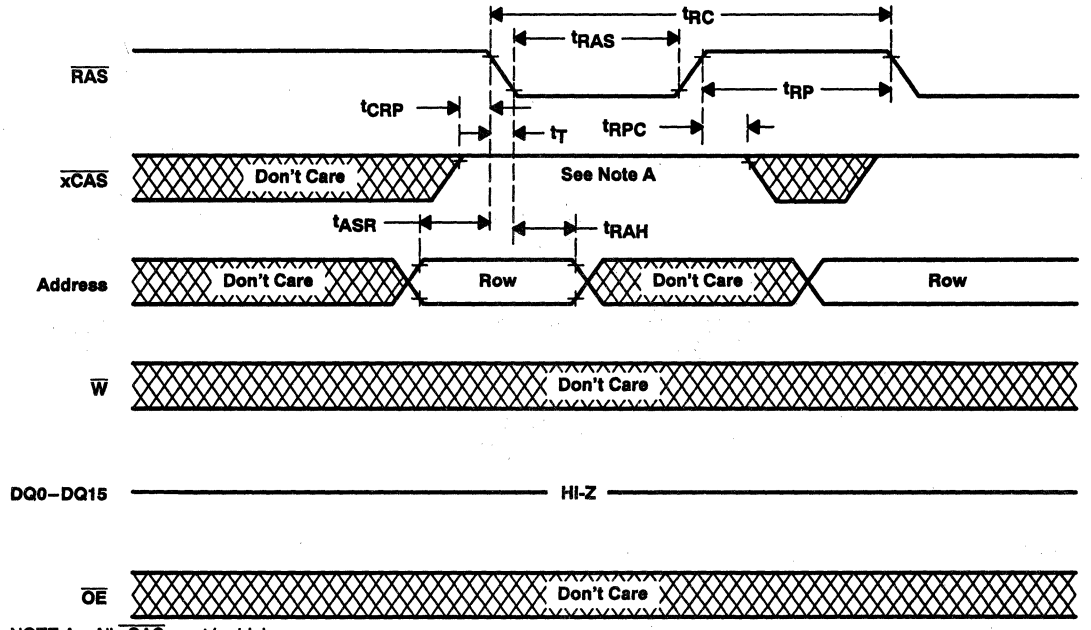
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Access time is t_{CPA}- or t_{AA}-dependent.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. $\overline{xCAS}$ order is arbitrary.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read- and write-cycle timing specifications are not violated.
F. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.

Figure 10. Extended-Data-Out Read-Modify-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: All $\overline{xCAS}$ must be high.

Figure 11. $\overline{RAS}$-Only Refresh-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

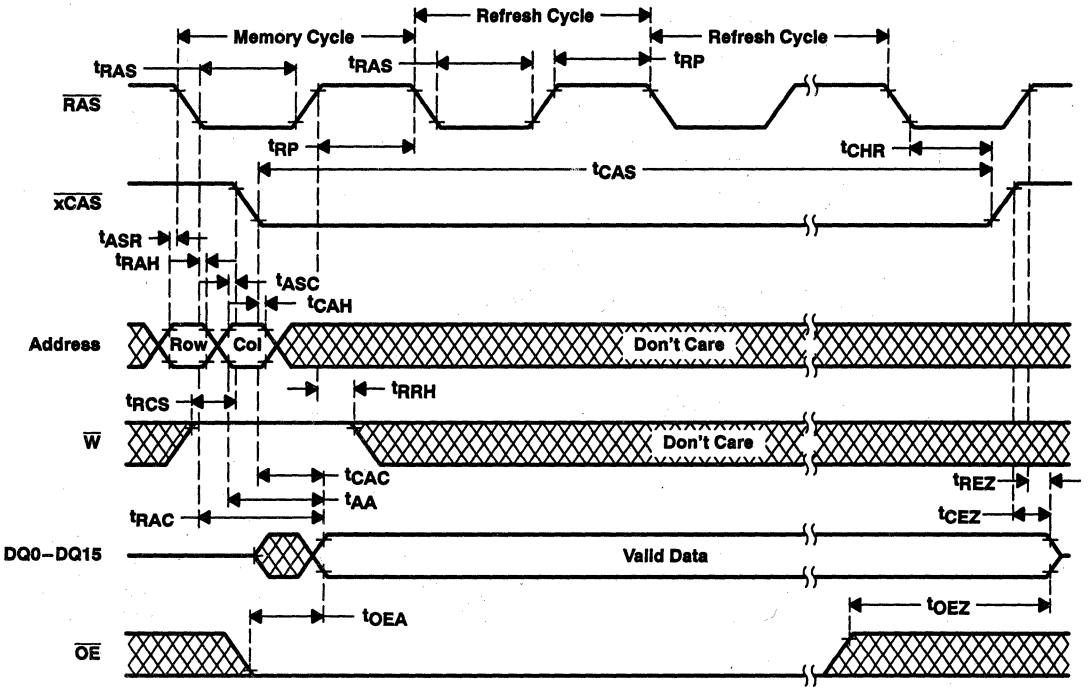

Figure 12. Hidden-Refresh-Cycle Timing

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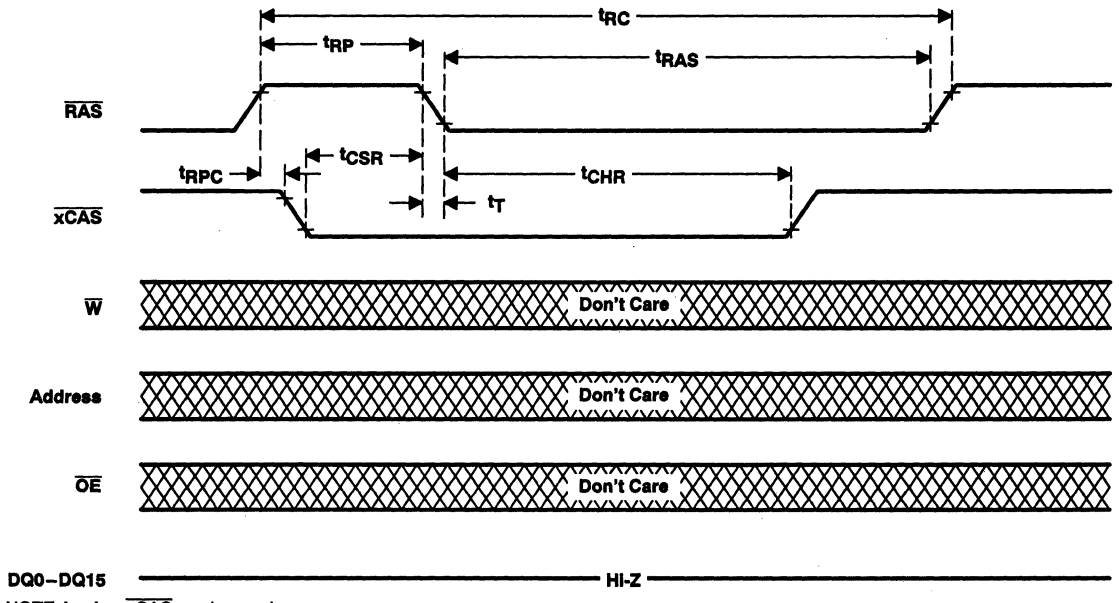
PARAMETER MEASUREMENT INFORMATION



NOTE A: Any $\overline{xCAS}$ can be used.

Figure 13. Automatic-xCBR-Refresh-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

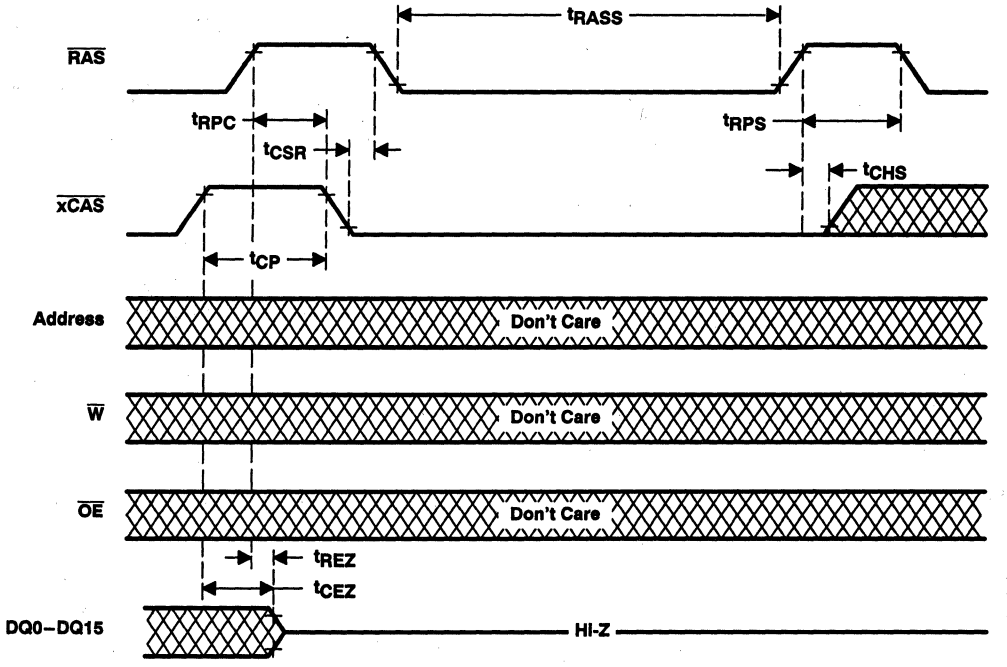
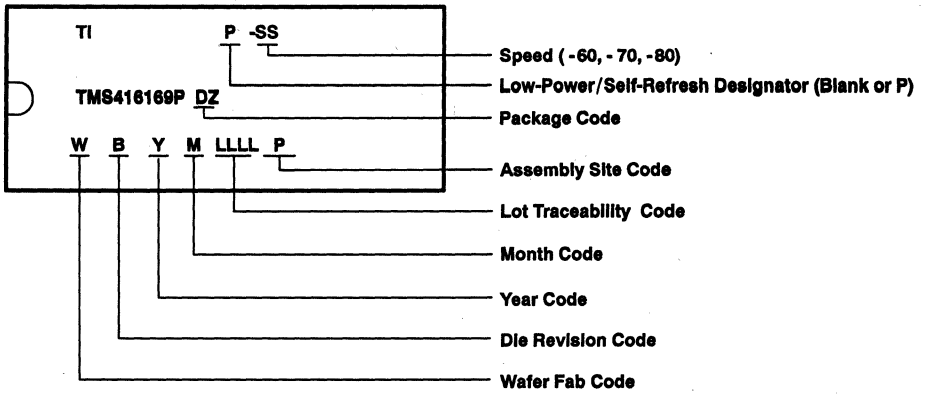


Figure 14. Self-Refresh-Cycle Timing

device symbolization (TMS416169P illustrated)



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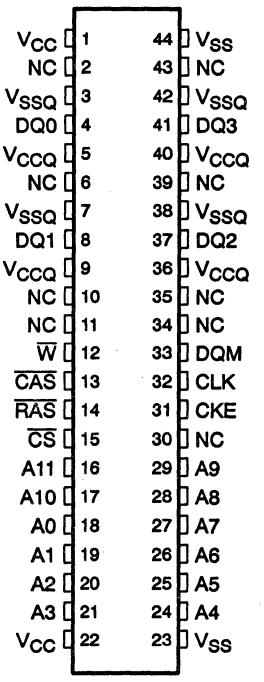
Contents

CHAPTER 5. SYNCHRONOUS DRAM (SDRAM) VIDEO RANDOM-ACCESS MEMORY (VRAM)

- **Organization . . . 2M × 4 × 2 Banks**
- **3.3-V Power Supply (±10% Tolerance)**
- **Two Banks for On-Chip Interleaving (Gapless Accesses)**
- **High Bandwidth – Up to 100-MHz Data Rates**
- **Burst Length Programmable to 1, 2, 4, or 8**
- **Programmable Output Sequence – Serial or Interleave**
- **Chip Select and Clock Enable for Enhanced-System Interfacing**
- **Cycle-by-Cycle DQ-Bus Mask Capability**
- **Programmable Read Latency From Column Address**
- **Self-Refresh Capability**
- **High-Speed, Low-Noise LVTTL**
- **Power-Down Mode**
- **Compatible With JEDEC Standards**
- **4K Refresh (Total for Both Banks)**
- **2-Bit Prefetch Architecture for High Speed Performance**
- **Performance Ranges:**

	SYNCHRONOUS CLOCK CYCLE TIME t_{CK} (MIN)	ACTV COMMAND TO READ OR WRITE COMMAND t_{RCD} (MIN)	REFRESH TIME INTERVAL t_{REF} (MAX)
TMS626402-10	10 ns	30 ns	64 ms
TMS626402-12	12.5 ns	35 ns	64 ms
TMS626402-15	15 ns	40 ns	64 ms

DGE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs A0–A10 Row Addresses A0–A9 Column Addresses A10 Automatic-Precharge Select
A11	Bank Select
$\overline{CAS}$	Column-Address Strobe
CKE	Clock Enable
CLK	System Clock
$\overline{CS}$	Chip Select
DQ0–DQ3	SDRAM Data Input/Data Output
DQM	Data/Output Mask Enable
NC	No External Connect
$\overline{RAS}$	Row-Address Strobe
V_{CC}	Power Supply (3.3 V Typ)
V_{CCQ}	Power Supply for Output Drivers (3.3 V Typ)
V_{SS}	Ground
V_{SSQ}	Ground for Output Drivers
$\overline{W}$	Write Enable

description

The TMS626402 series are high-speed 16777216-bit synchronous dynamic random-access memories organized as two banks of 2097152 words with four bits per word.

All inputs and outputs of the TMS626402 series are compatible with the low-voltage TTL (LVTTL) interface.

The synchronous DRAM employs state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power. All inputs and outputs are synchronized with the CLK input to simplify system design and enhance use with high-speed microprocessors and caches.

The TMS626402 synchronous DRAM is available in a 400-mil, 44-pin surface-mount TSOP (II) package (DGE suffix).

EPIC is a trademark of Texas Instruments Incorporated.

operation

All inputs of the '626402 synchronous DRAM are latched on the rising edge of the system (synchronous) clock. The outputs, DQ0–DQ3, are also referenced to the rising edge of CLK. The '626402 has two banks that are accessed independently. A bank must be activated before it can be accessed (read from or written to). Refresh cycles refresh both banks alternately.

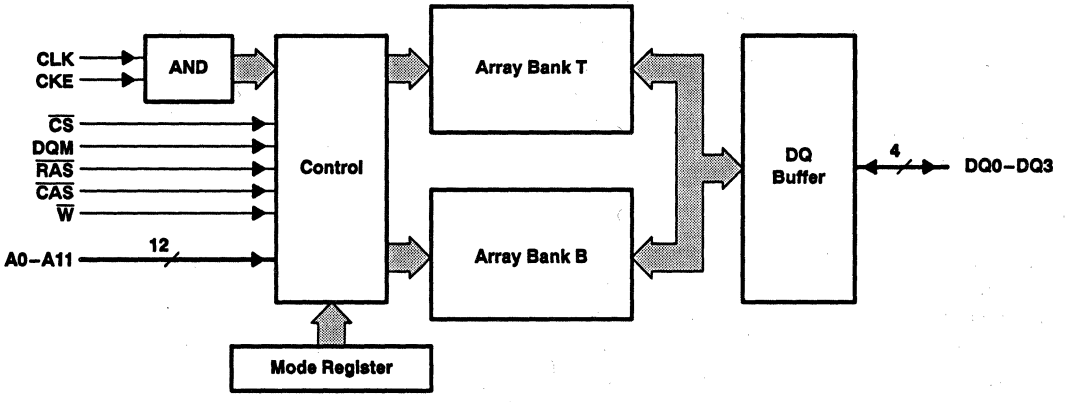
Six basic commands or functions control most operations of the '626402:

- Bank activate/row-address entry
- Column-address entry/write operation
- Column-address entry/read operation
- Bank deactivate
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ (CBR)
- Self-refresh entry

Additionally, operation can be controlled by three methods: using chip select ($\overline{\text{CS}}$) to select/deselect the devices, using DQM to enable/mask the DQ signals on a cycle-by-cycle basis, or using CKE to suspend (or gate) the CLK input. The device contains a mode register that must be programmed for proper operation.

Tables 1 through 3 show the various operations that are available on the '626402. These truth tables identify the commands and/or operations and their respective mnemonics. Each truth table is followed by a legend that explains the abbreviated symbols. An access operation refers to any READ (READ-P) or WRT (WRT-P) command in progress at cycle n. Access operations include the cycle upon which the READ (READ-P) or WRT (WRT-P) command is entered and all subsequent cycles through the completion of the access burst.

functional block diagram



operation (continued)

Table 1. Basic-Command Truth Table†

COMMAND	STATE OF BANK(S)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A11	A10	A9–A0	MNEMONIC
Mode register set	T = deac B = deac	L	L	L	L	X	X	A9=X A8=0 A7=0 A6–A0=V	MRS
Bank deactivate (precharge)	X	L	L	H	L	BS	L	X	DEAC
Deactivate all banks	X	L	L	H	L	X	H	X	DCAB
Bank activate/row-address entry	SB = deac	L	L	H	H	BS	V	V	ACTV
Column-address entry/write operation	SB = actv	L	H	L	L	BS	L	V	WRT
Column-address entry/write operation with autodeactivate	SB = actv	L	H	L	L	BS	H	V	WRT-P
Column-address entry/read operation	SB = actv	L	H	L	H	BS	L	V	READ
Column-address entry/read operation with autodeactivate	SB = actv	L	H	L	H	BS	H	V	READ-P
Burst stop	SB = actv	L	H	H	L	X	X	X	STOP
No operation	X	L	H	H	H	X	X	X	NOOP
Control input inhibit / no operation	X	H	X	X	X	X	X	X	DESL
CBR refresh‡	T = B = deac	L	L	L	H	X	X	X	REFR

† For execution of these commands on cycle n, CKE (n) must be high and satisfy t_{CESP} from power-down exit (PDE), t_{CES} and nCLE from clock-suspend (HOLD) exit, and t_{CESP} and t_{RC} from self-refresh (SLFR) exit. DQM (n) is a don't care.

‡ CBR or self-refresh entry requires that all banks be deactivated or in an idle state prior to the command entry.

Legend:

L = Logic low
H = Logic high
X = Don't care
V = Valid
T = Bank T
B = Bank B
actv = Activated
deac = Deactivated
BS = Logic high to select bank T; logic low to select bank B
SB = Bank selected by A11 at cycle n

operation (continued)

Table 2. CKE-Use Command Truth Table†

COMMAND	STATE OF BANK(S)	CKE (n−1)	CKE (n)	$\overline{CS}$ (n)	$\overline{RAS}$ (n)	$\overline{CAS}$ (n)	$\overline{W}$ (n)	MNEMONIC
Self-refresh entry	T = B = deac	H	L	L	L	L	H	SLFR
Power-down entry at n + 1	T = B = no access operation‡	H	L	L	H	H	H	PDE
		H	L	H	X	X	X	PDE
Self-refresh exit	T = B = self refresh	L	H	L	H	H	H	—
		L	H	H	X	X	X	—
Power-down exit	T = B = power down	L	H	X	X	X	X	—
CLK suspend at n + 1	T or B = access operation‡	H	L	X	X	X	X	HOLD
CLK suspend exit at n + 1	T or B = access operation‡	L	H	X	X	X	X	—

† For execution of these commands, A0–A11 (n) and DQM (n) are don't cares.
‡ An access operation refers to any READ (READ-P) or WRT (WRT-P) command in progress at cycle n. Access operations include the cycle upon which the READ (READ-P) or WRT (WRT-P) command is entered and all subsequent cycles through the completion of the access burst.

Legend:

n = CLK cycle number
L = Logic low
H = Logic high
X = Don't care
T = Bank T
B = Bank B
deac = Deactivated

operation (continued)

Table 3. DQM-Use Command Truth Table†

COMMAND	STATE OF BANK(S)	DQM (n)	DATA IN (n)	DATA OUT (n+2)	MNEMONIC
—	T = deac and B = deac	X	N/A	Hi-Z	—
—	T = actv and B = actv (no access operation)‡	X	N/A	Hi-Z	—
Data-in enable	T = write or B = write	L	V	N/A	ENBL
Data-in mask	T = write or B = write	H	M	N/A	MASK
Data-out enable	T = read or B = read	L	N/A	V	ENBL
Data-out mask	T = read or B = read	H	N/A	Hi-Z	MASK

† For execution of these commands, CKE (n) must be high and satisfy t_{CESP} from power-down exit (PDE), t_{CES} and nCLE from clock-suspend (HOLD) exit, and t_{CESP} and t_{RC} from self-refresh (SLFR) exit. $\overline{CS}$ (n), $\overline{RAS}$ (n), $\overline{CAS}$ (n), $\overline{W}$ (n), and A0–A11 (n) are don't cares.

‡ An access operation refers to any READ (READ-P) or WRT (WRT-P) command in progress at cycle n. Access operations include the cycle upon which the READ (READ-P) or WRT (WRT-P) command is entered and all subsequent cycles through the completion of the access burst.

Legend:

- n = CLK cycle number
- L = Logic low
- H = Logic high
- X = Don't care
- V = Valid
- M = Masked input data
- N/A = Not applicable
- T = Bank T
- B = Bank B
- actv = Activated
- deac = Deactivated
- write = Activated and accepting data in on cycle n
- read = Activated and delivering data out on cycle n + 2

burst sequence

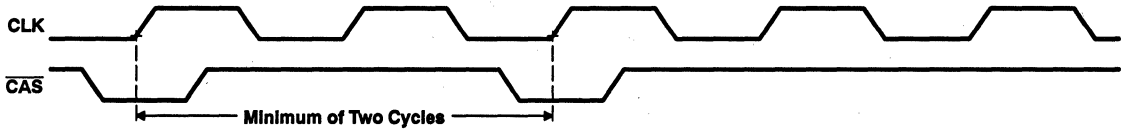
All data for the '626402 is written or read in a burst fashion; that is, a single starting address is entered into the device and the '626402 internally accesses a sequence of locations based on that starting address. Some of the subsequent accesses after the first can be at preceding as well as succeeding column addresses, depending on the starting address entered. This sequence can be programmed to follow either a serial burst or an interleave burst (see Tables 4 through 6). The length of the burst sequence can be user programmed to be either 1-, 2-, 4-, or 8-bit accesses. After a read burst is completed (as determined by the programmed burst length), the outputs are in the high-impedance state until the next read access is initiated.

Table 4. 2-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A0			
	DECIMAL		BINARY	
	START	2ND	START	2ND
Serial	0	1	0	1
	1	0	1	0
Interleave	0	1	0	1
	1	0	1	0

Table 5. 4-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A1–A0							
	DECIMAL				BINARY			
	START	2ND	3RD	4TH	START	2ND	3RD	4TH
Serial	0	1	2	3	00	01	10	11
	1	2	3	0	01	10	11	00
	2	3	0	1	10	11	00	01
	3	0	1	2	11	00	01	10
Interleave	0	1	2	3	00	01	10	11
	1	0	3	2	01	00	11	10
	2	3	0	1	10	11	00	01
	3	2	1	0	11	10	01	00



NOTE: For burst sequence of one, subsequent read or write commands must be done at least two clock cycles from initial read or write command (see timing diagram above),

Figure 1. Subsequent Read or Write CMD for BL = 1

burst sequence (continued)

Table 6. 8-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A2–A0															
	DECIMAL								BINARY							
	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH
Serial	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	2	3	4	5	6	7	0	001	010	011	100	101	110	111	000
	2	3	4	5	6	7	0	1	010	011	100	101	110	111	000	001
	3	4	5	6	7	0	1	2	011	100	101	110	111	000	001	010
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	6	7	0	1	2	3	4	101	110	111	000	001	010	011	100
	6	7	0	1	2	3	4	5	110	111	000	001	010	011	100	101
	7	0	1	2	3	4	5	6	111	000	001	010	011	100	101	110
Interleave	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	0	3	2	5	4	7	6	001	000	011	010	101	100	111	110
	2	3	0	1	6	7	4	5	010	011	000	001	110	111	100	101
	3	2	1	0	7	6	5	4	011	010	001	000	111	110	101	100
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	4	7	6	1	0	3	2	101	100	111	110	001	000	011	010
	6	7	4	5	2	3	0	1	110	111	100	101	010	011	000	001
	7	6	5	4	3	2	1	0	111	110	101	100	011	010	001	000

latency

The beginning data-output cycle of a read burst can be programmed to occur 1, 2, or 3 CLK cycles after the read command (see setting the mode register). This feature allows the user to adjust the '626402 to operate in accordance with the system's capability to latch the data output from the '626402. The delay between the READ command and the beginning of the output burst is known as read latency (also known as $\overline{CAS}$ latency). After the initial output cycle begins, the data burst occurs at the CLK frequency without any intervening gaps. Use of minimum read latencies is restricted based on the particular maximum frequency rating of the '626402.

There is no latency for data-in cycles (write latency). The first data-in cycle of a write burst is entered at the same rising edge of CLK on which the WRT command is entered. The write latency is fixed and not determined by the mode-register contents.

two-bank operation

The '626402 contains two independent banks that can be accessed individually or in an interleaved fashion. Each bank must be activated with a row address before it can be accessed. Each bank must then be deactivated before it can be activated again with a new row address. The bank-activate/row-address-entry command (ACTV) is entered by holding $\overline{RAS}$ low, $\overline{CAS}$ high, $\overline{W}$ high, and A11 valid on the rising edge of CLK. A bank can be deactivated either automatically during a READ (READ-P) or a WRT (WRT-P) command or by use of the deactivate-bank (DEAC) command. Both banks can be deactivated at once by use of the DCAB command (see Table 1 and the bank deactivation description).

two-bank row-access operation

The two-bank feature allows the user to access information on random rows at a higher rate of operation than is possible with a standard DRAM. This is accomplished by activating one bank with a row address, and while the data stream is being accessed to/from that bank, activating the second bank with another row address.

two-bank row-access operation (continued)

When the data stream to/from the first bank is complete, the data stream to/from the second bank can begin without interruption. After the second bank is activated, the first bank can be deactivated to allow the entry of a new row address for the next round of accesses. In this manner, operation can continue in an interleaved fashion. Figure 27 is an example of two-bank row interleaving with automatic deactivate for the case of a read latency of 3 and a burst length of 8.

two-bank column-access operation

The availability of two banks allows the access of data from random starting columns between banks at a higher rate of operation. After activating each bank with a row address (ACTV command), A11 can be used to alternate READ or WRT commands between the banks to provide gapless accesses at the CLK frequency, provided all specified timing requirements are met. Figure 28 is an example of two-bank column interleaving with a read latency of 3 and a burst length of 2.

bank deactivation (precharge)

Both banks can be simultaneously deactivated (placed in precharge) by using the DCAB command. A single bank can be deactivated by using the DEAC command. The DEAC command is entered identically to the DCAB command except that A10 must be low and A11 selects the bank to be precharged as shown in Table 1. A bank can also be deactivated automatically by using A10 during a READ or WRT command. If A10 is held high during the entry of a READ or WRT command, the accessed bank (selected by A11) automatically deactivates upon completion of the access burst. If A10 is held low during READ or WRT command entry, that bank remains active following the burst. The READ and WRT commands with automatic deactivation are denoted as READ-P and WRT-P.

chip select ($\overline{CS}$)

$\overline{CS}$ can be used to select or deselect the '626402 for command entry, which might be required for multiple memory-device decoding. If $\overline{CS}$ is held high on the rising edge of CLK (DESL command), the device does not respond to $\overline{RAS}$, $\overline{CAS}$, or $\overline{W}$ until the device is selected again. Device select is accomplished by holding $\overline{CS}$ low on the rising edge of CLK. Any other valid command can be entered simultaneously on the same rising CLK edge of the select operation. The device can be selected/deselected on a cycle-by-cycle basis (see Tables 1 and 2). The use of $\overline{CS}$ does not affect an access burst that is in progress; the DESL command can only restrict $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ input to the '626402.

data/output mask

Masking of individual data cycles within a burst sequence can be accomplished by use of the MASK command (see Table 3). If DQM is held high on the rising edge of CLK during a write burst, the incident data word (referenced to the same rising edge of CLK) on DQ0–DQ3 is ignored. If DQM is held high on the rising edge of CLK for a read burst, DQ0–DQ3 referenced to the second rising edge of CLK are in the high-impedance state. The application of DQM to data output cycles (READ burst) involves a latency of two CLK cycles, but the application of DQM to data-in cycles (WRITE burst) has no latency. The MASK command (or its opposite, the ENBL command) is performed on a cycle-by-cycle basis, allowing the user to gate any individual data cycle or cycles within either a read- or a write-burst sequence. Figure 31 shows an example of data/output masking.

NOTE: Data masking using DQM input is not supported when the mode register is set for read latency of one and burst length of one. If the mode register is in this mode, the DQM pin should be held low.

CLK suspend/power-down mode

For normal device operation, CKE should be held high to enable CLK. If CKE goes low during the execution of a READ (READ-P) or WRT (WRT-P) operation, the state of the DQ bus at the immediate next rising edge of CLK is frozen at its current state, and no further inputs are accepted until CKE is returned high.

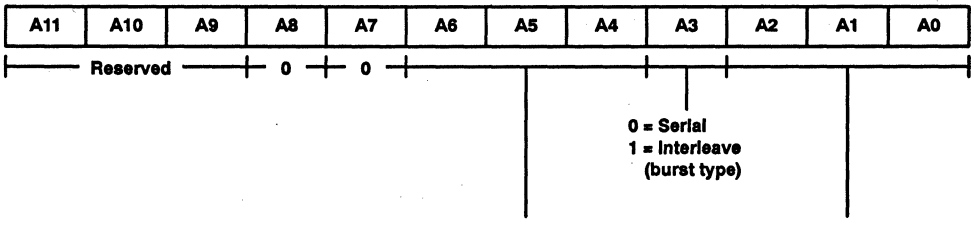
CLK suspend/power-down mode (continued)

This CLK suspend/power-down mode is known as a CLK suspend operation, and its execution is denoted as a HOLD command. The device resumes operation from the point at which it was placed in suspension, beginning with the second rising edge of CLK after CKE is returned high.

If CKE is brought low when no READ (READ-P) or WRT (WRT-P) command is in progress, the device enters power-down mode. If both banks are deactivated when power-down mode is entered, power consumption is reduced to the minimum. Power-down mode can be used during row-active or CBR-refresh periods to reduce input-buffer power. After power-down mode has been entered, no further inputs are accepted until CKE returns high. To ensure data in the device remains valid during the power-down mode, the self-refresh command (SLRF) must be executed concurrently with the power-down entry command (PDE). When exiting power-down mode, new commands can be entered on the first CLK edge after CKE returns high, provided that the setup time (t_{CESP}) is satisfied. Table 2 shows the command configuration for a CLK suspend/power-down operation, and Figures 18 and 19 show an example of the procedure.

setting the mode register

The '626402 contains a mode register that the user shoud program with the read latency, the burst type, and the burst length. This is accomplished by executing an MRS command with the information entered on address lines A0–A8. A logic 0 should always be entered on A7 and A8, but A9–A11 are don't-care entries for the '626402. Figure 2 shows the valid combinations for a successful MRS command. Only valid addresses allow the mode register to be changed. If the addresses are not valid, the previous contents of the mode register remain unaffected. The MRS command is executed by holding $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ low, and the input-mode word valid on A0–A8 on the rising edge of CLK (see Table 1). The MRS command can be executed only when both banks are deactivated.



REGISTER BITS†			READ LATENCY‡
A6	A5	A4	
0	0	1	1
0	1	0	2
0	1	1	3

† All other combinations are reserved.
‡ Refer to timing requirements for minimum valid-read latencies based on maximum frequency rating.

REGISTER BITS§			BURST LENGTH
A2	A1	A0	
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8

§ All other combinations are reserved.

Figure 2. Mode-Register Programming

refresh

The '626402 must be refreshed at intervals not exceeding t_{REF} (see timing requirements) or data cannot be retained. Refresh can be accomplished by performing a read or write access to every row in both banks, by performing 4096 $\overline{CAS}$-before-$\overline{RAS}$ (REFR) commands, or by placing the device in self refresh. Regardless of the method used, refresh must be accomplished before t_{REF} has expired.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

Before performing a $\overline{CAS}$-before-$\overline{RAS}$ refresh, both banks must be deactivated (placed in precharge). To enter a REFR command, $\overline{RAS}$ and $\overline{CAS}$ must be low and $\overline{W}$ must be high upon the rising edge of CLK (see Table 1). The refresh address is generated internally such that after 4096 REFR commands, both banks of the '626402 are refreshed. The external address and bank select (A11) are ignored. The execution of a REFR command automatically deactivates both banks upon completion of the internal CBR cycle. This allows consecutive REFR-only commands to be executed, if desired, without any intervening DEAC commands. The REFR commands do not necessarily have to be consecutive, but all 4096 must be completed before t_{REF} expires.

self refresh

To enter self refresh, both banks of the '626402 must first be deactivated and a SLFR command must be executed (see Table 2). The SLFR command is identical to the REFR command except that CKE is low. For proper entry of the SLFR command, CKE is brought low for the same rising edge of CLK that $\overline{RAS}$ and $\overline{CAS}$ are low and $\overline{W}$ is high. CKE must be held low to stay in self-refresh mode. In the self-refresh mode, all refreshing signals are generated internally for both banks with all external signals (except CKE) being ignored. Data can be retained by the device automatically for an indefinite period when power is maintained (consumption is reduced to a minimum). To exit self-refresh mode, CKE must be brought high. New commands are issued after t_{RC} has expired. If CLK is made inactive during self refresh, it must be returned to an active and stable condition before CKE is brought high to exit self refresh (see Figure 21).

Upon exiting self-refresh, the normal refresh scheme must begin immediately. If the burst-refresh scheme is used, 4096 REFR commands must be executed before continuing with normal device operations. If a distributed-refresh scheme utilizing CBR is used (e.g., two rows every 32 μs), the first set of refreshes must be performed before continuing with normal device operation. This ensures that the SDRAM is fully refreshed.

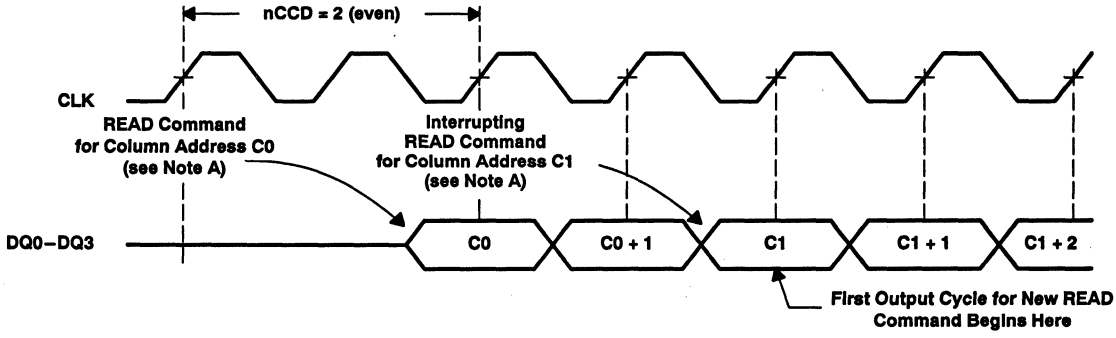
Interrupted bursts

A read or write can be interrupted before the burst sequence has been completed with no adverse effects to the operation. This is accomplished by entering certain superseding commands as listed in Tables 7 and 8, provided that all timing requirements are met. The command interrupting either a read or write burst must be entered only on an even number of cycles (2n rule) from the initial burst command (nCCD). nCCD is defined as the number of clock cycles from the initial command to the interrupting command. In the case when the number of clock cycles between a read/write command and the following command is greater than the burst length, the "2n rule" and nCCD does not apply. A DEAC command is considered an interrupt only if it is issued to the same bank as the preceding READ or WRITE command. The interruption of READ-P and WRT-P operations is not supported.

Interrupted bursts (continued)

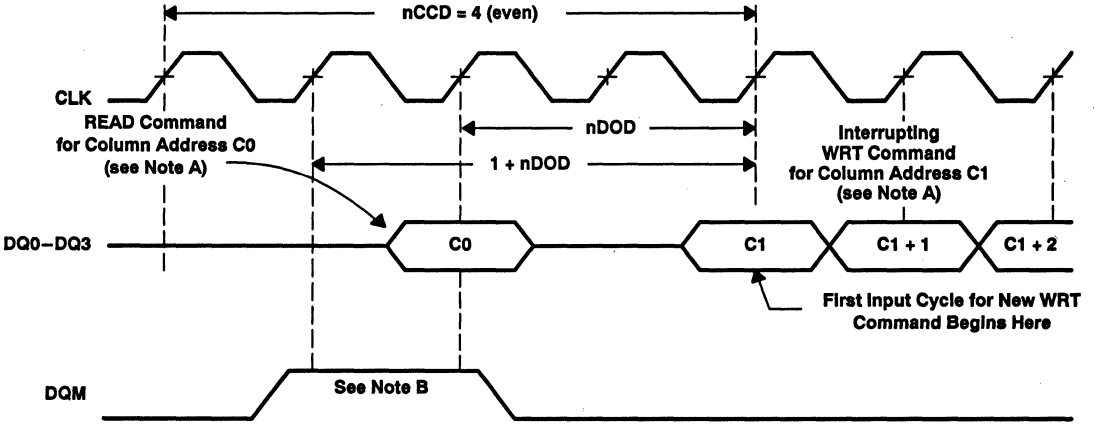
Table 7. Read-Burst Interruption

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING READ BURST
DEAC, DCAB	The DQ bus is placed in the high-impedance state when nHZP cycles are satisfied or upon completion of the read burst, whichever occurs first (see Figures 5 and 21).
WRT, WRT-P	The WRT command immediately supersedes the read burst in progress, but DQM must be high nDOD+1 and nDOD cycles previous to the WRT (WRT-P) command (see Figure 4).
READ, READ-P	Current output cycles continue until the programmed latency from the superseding READ (READ-P) command is met, and new output cycles begin (see Figure 3).
STOP	The DQ bus is placed in the high-impedance state two clock cycles after the stop command is entered or upon completion of the read burst, whichever occurs first. The bank remains active. A new read or write command cannot be entered for at least two cycles after the STOP command (see Figure 5).



NOTE A: For the purposes of this example, read latency = 2 and burst length > 2.

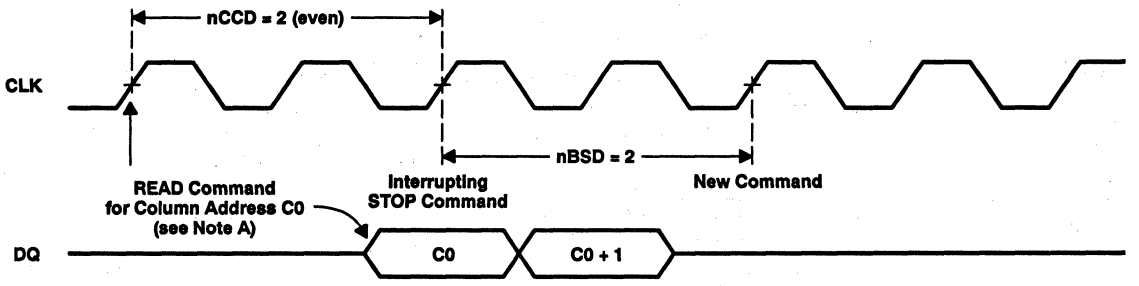
Figure 3. Read Burst Interrupted by Read Command



NOTES: A. For the purposes of this example, read latency = 2 and burst length > 2.
B. DQM is held high for 2 CLK cycles (2 rising edges). DQM is held high for nDOD+1 to mask out bit prior to interrupting WRT command. DQM is held high for nDOD as specified spec.

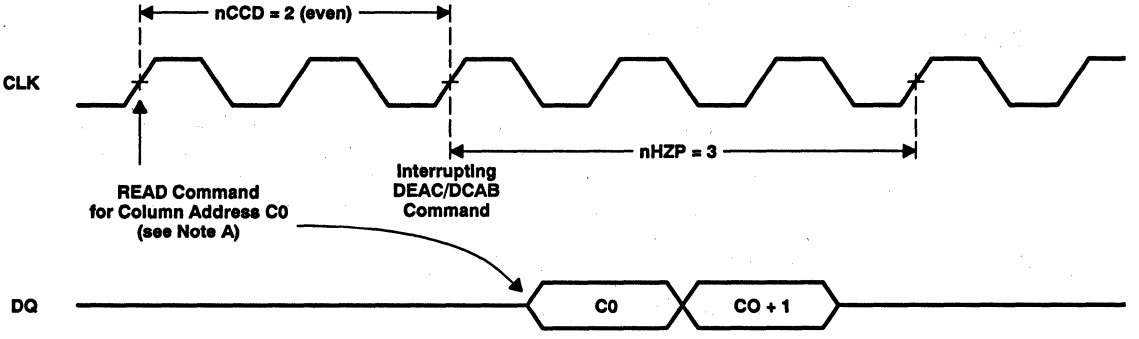
Figure 4. Read Burst Interrupted by Write Command

Interrupted bursts (continued)



NOTE A: For this example, read latency = 2 and burst length > 2.

Figure 5. Read Burst Interrupted by STOP Command



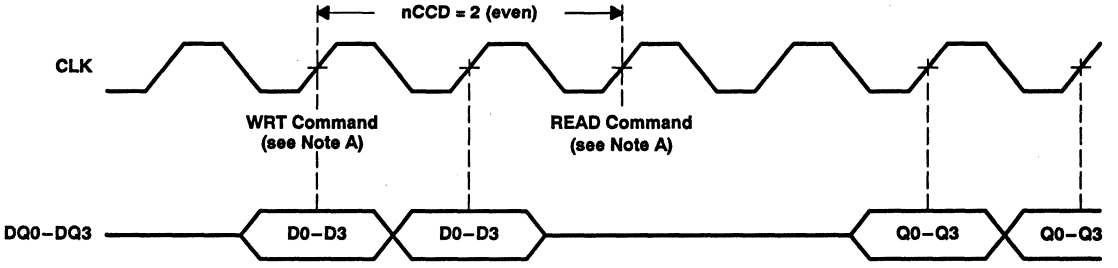
NOTE A: For this example, read latency = 3 and burst length > 2.

Figure 6. Read Burst Interrupted by DEAC Command

Interrupted bursts (continued)

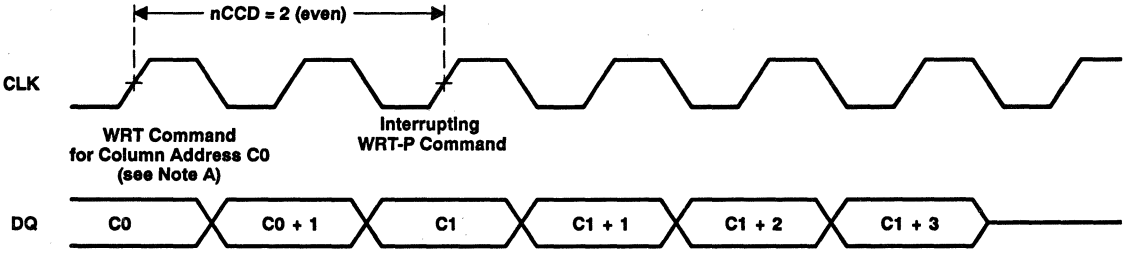
Table 8. Write-Burst Interruption

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING WRITE BURST
DEAC, DCAB	The DEAC/DCAB command immediately supersedes the write burst in progress. DQM must be used to mask the DQ bus such that the write-recovery specification (t_{RWL}) is not violated by the interrupt (see Figure 10).
WRT, WRT-P	The new WRT (WRT-P) command and data in immediately supersede the write burst in progress (see Figure 8).
READ, READ-P	Data in on previous cycle is written. No further data input is accepted (see Figure 7).
STOP	The data on the input pins at the time of the burst STOP command is not written, and no further data is accepted. The bank remains active. A new read or write command cannot be entered for at least two cycles after the STOP command (see Figure 9).



NOTE A: For this example, read latency = 2 and burst length > 2.

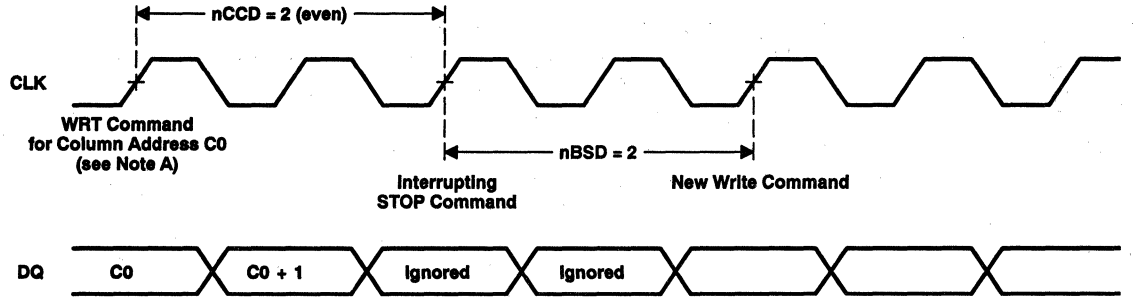
Figure 7. Write Burst Interrupted by Read Command



NOTE A: For this example, burst length > 2.

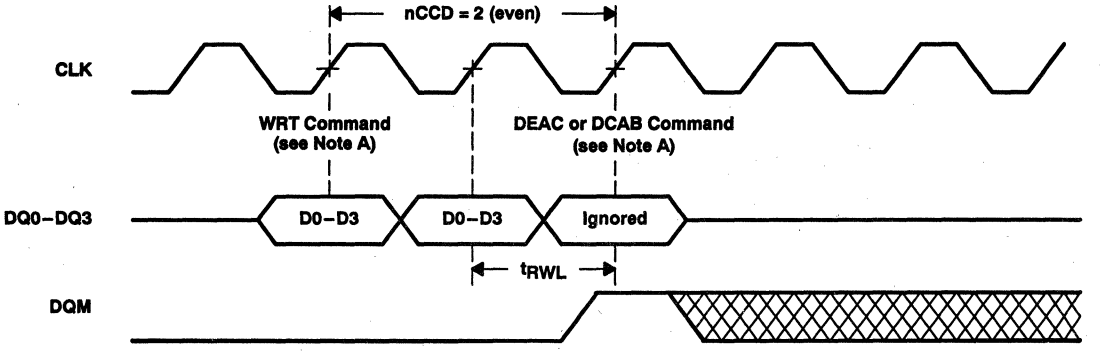
Figure 8. Write Burst Interrupted by Write Command

Interrupted bursts (continued)



NOTE A: For tthis example, burst length > 2.

Figure 9. Write Burst Interrupted by STOP Command



NOTE A: For this example, read latency = 2, burst length > 2, and $t_{CK} = t_{RWL}$.

Figure 10. Write Burst Interrupted by DEAC/DCAB Command

power up

Device initialization should be performed after a power up to the full V_{CC} level. After power is established, a 200-µs interval is required (with no inputs other than CLK). After this interval, both banks of the device must be deactivated. Eight REFR commands must be performed, and the mode register must be set to complete the device initialization.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 4.6 V
Supply voltage range for output drivers, V_{CCQ} ..... – 0.5 V to 4.6 V
Voltage range on any pin (see Note 1) ..... – 0.5 V to 4.6 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{CCQ}	Supply voltage for output drivers	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{SSQ}	Supply voltage for output drivers		0		V
V_{IH}	High-level input voltage	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS			'626402-10 MIN	'626402-10 MAX	'626402-12 MIN	'626402-12 MAX	'626402-15 MIN	'626402-15 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −2 mA			2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA				0.4		0.4		0.4	V
I_I	Input current (leakage)	0 V ≤ V_I ≤ V_{CC} + 0.3 V, All other pins = 0 V to V_{CC}				±10		±10		±10	µA
I_O	Output current (leakage)	0 V ≤ V_O ≤ V_{CC} + 0.3 V, Output disabled				±10		±10		±10	µA
I_{CC1}	Average read or write current	t_{RC} = MIN, t_{CK} = MIN, Read latency = 3	1 bank active	Burst length = 1 or 2		90		80		70	mA
				Burst length = 4 or 8		110		100		90	
			2 banks active interleaving	Burst length = 1 or 2		150		120		100	
				Burst length = 4 or 8		170		140		130	
I_{CC2}	Standby current	Both banks deactivated	CKE = V_{IH}, See Note 3			16		16		16	mA
			CKE = V_{IL}			2		2		2	
			CKE = 0 V (CMOS)			1		1		1	
		One or both banks active	CKE = V_{IL}			6		6		6	
I_{CC3}	Consecutive CBR commands	t_{RC} = MIN				90		80		70	mA
I_{CC4}	Burst current, gapless burst	ACTV not allowed, 2-bank interleaved, t_{CK} = MIN,		Read latency = 1		70		60		50	mA
				Read latency = 2		100		90		80	
				Read latency = 3		140		120		100	
I_{CC6}	Self-refresh current	CKE = V_{IL}				2		2		2	mA
		CKE = 0 V (CMOS)				1		1		1	

NOTES: 2. All specifications apply to the device after power-up initialization.
3. All control and address inputs must be stable and valid.

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 4)

		MIN	MAX	UNT
$C_{i(S)}$	Input capacitance, CLK		7	pF
$C_{i(AC)}$	Input capacitance, A0–A11, $\overline{CS}$, DQM, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		5	pF
$C_{i(E)}$	Input capacitance, CKE		5	pF
C_o	Output capacitance		8	pF

NOTE 4: V_{CC} = 3.3 ± 0.3 V and bias on pins under test is 0 V.

ac timing requirements over recommended ranges of supply voltage and operating free-air temperature †‡

			'626402-10		'626402-12		'626402-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CK}	Cycle time, CLK (system clock)	Read latency = 1	30		36		40		ns
		Read latency = 2	15		18		20		
		Read latency = 3	10		12		15		
t_{CKH}	Pulse duration, CLK (system clock) high		3		3.5		4		ns
t_{CKL}	Pulse duration, CLK (system clock) low		3		3.5		4		ns
t_{AC}	Access time, CLK ↑ to data out (see Note 5)	Read latency = 1		29		33		38	ns
		Read latency = 2		14		15		18	
		Read latency = 3		9		10		12	
t_{OH}	Hold time, CLK ↑ to data out		3		3		3		ns
t_{LZ}	Delay time, CLK to DQ in the low-impedance state (see Note 6)		0		0		0		ns
t_{HZ}	Delay time, CLK to DQ in the high-impedance state (see Note 7)	Read latency = 1		20		20		20	ns
		Read latency = 2		12		13		14	
		Read latency = 3		9		10		11	
t_{DS}	Setup time, data in		2		2		2		ns
t_{AS}	Setup time, address		2		2		2		ns
t_{CS}	Setup time, control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQM)		2		2		2		ns
t_{CES}	Setup time, CKE (suspend entry/exit, power-down entry)		2		2		2		ns
t_{CESP}	Setup time, CKE (power-down/self-refresh exit) (see Note 8)		8		10		12		ns
t_{DH}	Hold time, data in		2		3		4		ns
t_{AH}	Hold time, address		2		3		4		ns
t_{CH}	Hold time, control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQM)		2		3		4		ns
t_{CEH}	Hold time, CKE		2		3		4		ns
t_{RC}	REFR command to ACTV, MRS, REFR or SLFR command; ACTV command to ACTV, MRS, REFR or SLFR command; Self-refresh exit to ACTV, MRS, REFR or SLFR command		100		110		125		ns

† See Parameter Measurement Information for load circuits

‡ All references are made to the rising transition of CLK, unless otherwise noted.

NOTES: 5. t_{AC} is referenced from the rising transition of CLK that is previous to the data-out cycle. For example, the first data-out t_{AC} is referenced from the rising transition of CLK that is read latency – 1 cycles after the READ command. An access time is measured at output reference level 1.4 V.

6. t_{LZ} is measured from the rising transition of CLK that is read latency – 1 cycles after the READ command.

7. t_{HZ} (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.

8. If $t_{CESP} > t_{CK}$, NOOP or DESL commands must be entered until t_{CESP} is met. CLK must be active and stable (if CLK was turned off for power down) before CKE is returned high.

ac timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†‡

			'626402-10		'626402-12		'626402-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{RAS}	ACTV command to DEAC or DCAB command		60	100 000	70	100 000	80	100 000	ns
t_{RCD}	ACTV command to READ or WRT command		30		35		40		ns
t_{RP}	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR command		40		40		45		ns
t_{APR}	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command		t_{RP} + (nEP × t_{CK})						ns
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command (see Note 10)	Burst length = 1	1 clock+60		1 clock+60		1 clock+75		ns
		Burst length > 1	60		60		75		
t_{RWL}	Final data in to DEAC or DCAB command (see Note 11)	Burst length = 1	1 clock+20		1 clock+20		1 clock+30		ns
		Burst length > 1	20		20		30		
t_{RRD}	ACTV command for one bank to ACTV command for the other bank		20		25		30		ns
t_T	Transition time, all inputs (see Note 9)		1	5	1	5	1	5	ns
t_{REF}	Refresh interval			64		64		64	ms

† See Parameter Measurement Information for load circuits
‡ All references are made to the rising transition of CLK, unless otherwise noted.

NOTES: 9. Transition time, t_T, is measured between V_{IH} and V_{IL}.
10. for BL=1only
SPEED
–10, –12 = t_{APW} is 60 ns from first unsuspended clock edge after last data in
–15 = t_{APW} is 80 ns from first unsuspended clock edge after last data in
11. for BL = 1 only
SPEED
–10, –12 = t_{RWL} is 20 ns from first unsuspended clock edge after last data in
–15 = t_{RWL} is 30 ns from first unsuspended clock edge after last data in

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature†

			'626402-10		'626402-12		'626402-15		UNIT‡
			MIN	MAX	MIN	MAX	MIN	MAX	
nEP	Final data out to DEAC or DCAB command	Burst length = 1, Read latency = 1	1		1		1		cycles
		Burst length = 1, Read latency = 2	0		0		0		
		Burst length = 1, Read latency = 3	−1		−1		−1		
		Burst length > 1, Read latency = 1	0		0		0		cycles
		Burst length > 1, Read latency = 2	−1		−1		−1		
		Burst length > 1, Read latency = 3	−2		−2		−2		
nHZP	DEAC or DCAB interrupt of data out burst to DQ in the high-impedance state (see Note 12)	Read latency = 1	1		1		1		cycles
		Read latency = 2	2		2		2		
		Read latency = 3	3		3		3		
nCCD	READ or WRT command to interrupting STOP, READ, WRT, DEAC, or DCAB command (i = 1, 2, 3, . . .) (see Note 13)		2i		2i		2i		cycles
nCWL	Final data in to READ or WRT command in either bank	Burst length = 1	2		2		2		cycles
		Burst length > 1	1		1		1		cycles
nWCD	WRT command to first data in		0	0	0	0	0	0	cycles
nDID	ENBL or MASK command to data in		0	0	0	0	0	0	cycles
nDOD	ENBL or MASK command to data out		2	2	2	2	2	2	cycles
nCLE	HOLD command to suspended CLK edge; HOLD operation exit to entry of any command		1	1	1	1	1	1	cycles
nRSA	MRS command to ACTV, REFR, SLFR, or MRS command		2		2		2		cycles
nCDD	DESL command to control input inhibit		0	0	0	0	0	0	cycles
nBSD	STOP command to READ or WRT command		2		2		2		cycles

† All references are made to the rising transition of CLK, unless otherwise noted.

‡ A CLK cycle can be considered as contributing to a timing requirement for those parameters defined in cycle units only when not gated by CKE (those CLK cycles occurring during the time when CKE is asserted low).

NOTES: 12. A data-out burst can be interrupted only on an even number of clock cycles after the initial READ command is entered (refer to nCCD).

13. A read or write burst can be interrupted only at an even number of clock cycles after entry of the initial READ or WRT command. The nCCD parameter is only required in the case of a burst interruption.

Table 9. Number of Cycles Required to Meet Minimum Specification for Key Timing Parameters

			TMS626402-10					TMS626402-12				TMS626402-15			UNIT
	Operating frequency		100	80	66	50	33	80	66	50	33	66	50	33	MHz
t_{CK}	Cycle time, CLK (system clock)		10	12	15	20	30	12	15	20	30	15	20	30	ns
	KEY PARAMETER		NUMBER OF CYCLES REQUIRED												
	Read latency, minimum programmed value		3	3	2	2	1	3	3	2	2	3	2	2	cycles
t_{RCD}	ACTV command to READ or WRT command		3	3	2	2	1	3	3	2	2	3	2	2	cycles
t_{RAS}	ACTV command to DEAC or DCAB command		6	5	4	3	2	6	5	4	3	6	4	3	cycles
t_{RP}	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR command		4	4	3	2	2	4	3	2	2	4	3	2	cycles
t_{RC}	REFR command to ACTV, MRS, SLFR, or REFR command; self-refresh exit to ACTV, MRS, SLFR, or REFR command		10	9	7	5	4	10	8	6	4	9	7	5	cycles
t_{RWL}	Final data in to DEAC or DCAB command	Burst length = 1	3	3	3	2	2	3	3	2	2	3	3	2	cycles
		Burst length > 1	2	2	2	1	1	2	2	1	1	2	2	1	cycles
t_{RRD}	ACTV command for one bank to ACTV command for the other bank		2	2	2	1	1	3	2	2	1	2	2	1	cycles
t_{APR}	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command	Burst length = 1, Read latency = 1	—	—	—	—	3	—	—	—	—	—	—	—	cycles
		Burst length = 1, Read latency = 2	—	—	3	2	2	—	—	2	2	—	3	2	cycles
		Burst length = 1, Read latency = 3	3	3	2	1	1	3	2	1	1	3	2	1	cycles
		Burst length > 1, Read latency = 1	—	—	—	—	2	—	—	—	—	—	—	—	cycles
		Burst length > 1, Read latency = 2	—	—	2	1	1	—	—	1	1	—	2	1	cycles
		Burst length > 1, Read latency = 3	2	2	1	0	0	2	1	0	0	2	1	0	cycles
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command	Burst length = 1	7	6	5	4	3	6	5	4	3	6	5	4	cycles
		Burst length > 1	6	5	4	3	2	5	4	3	2	5	4	3	cycles

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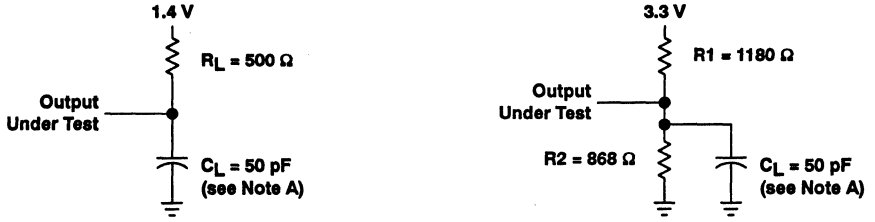
PARAMETER MEASUREMENT INFORMATION

general information for ac timing measurements

The ac timing measurements are based on signal rise and fall times equal to 1 ns (t_T = 1 ns) and a midpoint reference level of 1.4 V for LVTTL. For signal rise and fall times greater than 1 ns, the reference level should be changed to V_{IH} min and V_{IL} max instead of the midpoint level. All specifications referring to READ commands are also valid for READ-P commands unless otherwise noted. All specifications referring to WRT commands are also valid for WRT-P commands unless otherwise noted. All specifications referring to consecutive commands are specified as consecutive commands for the same bank unless otherwise noted.

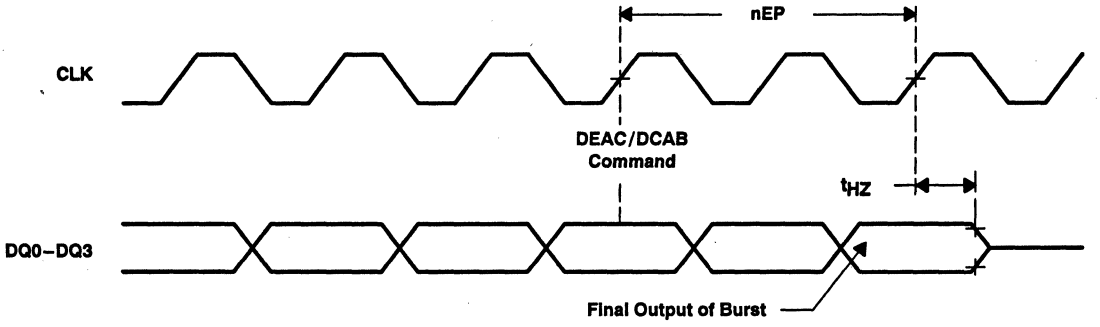


(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.

Figure 11. Load Circuits



NOTE A: For this example, assume read latency = 3 and burst length > 1.

Figure 12. nEP, Final Data Output to DEAC or DCAB Command

PARAMETER MEASUREMENT INFORMATION

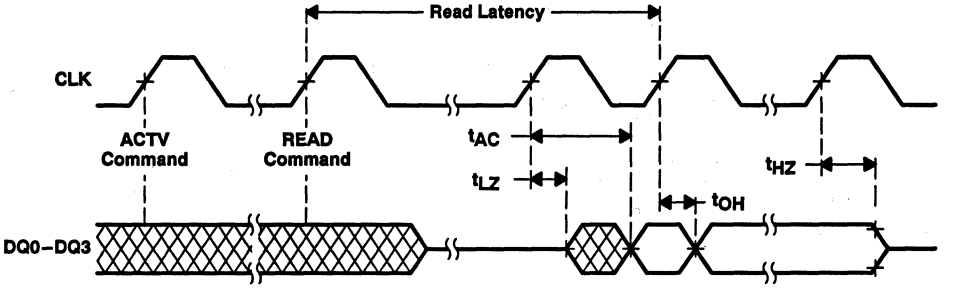
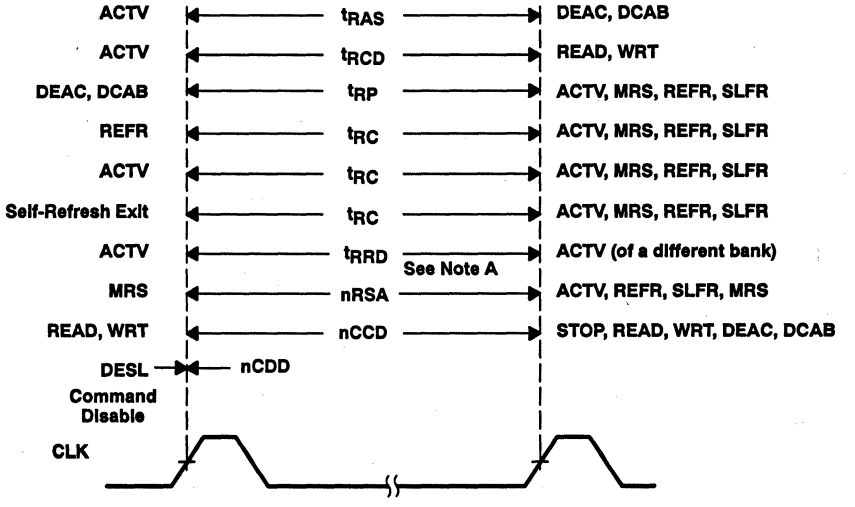


Figure 13. Output Parameters



NOTE A: t_{RRD} is specified for command execution in one bank to command execution in the other bank.

Figure 14. Command-to-Command Parameters

PARAMETER MEASUREMENT INFORMATION

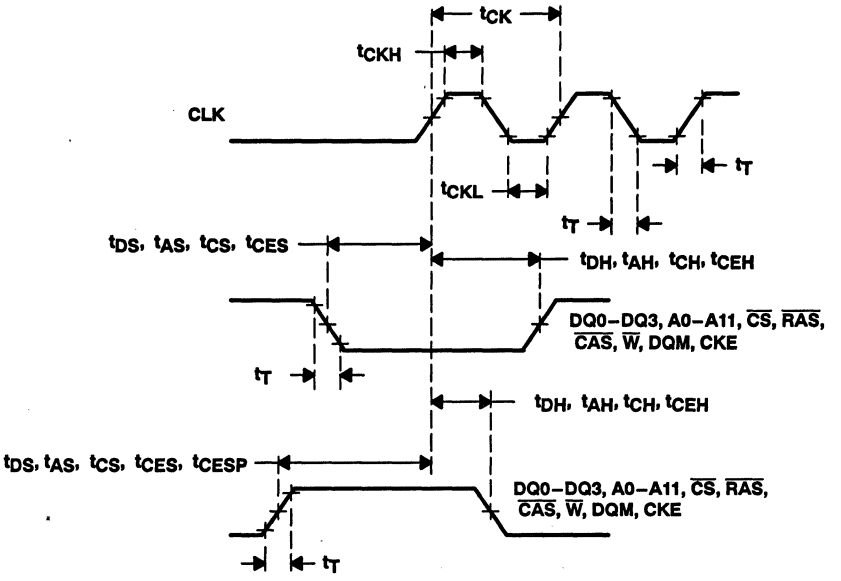
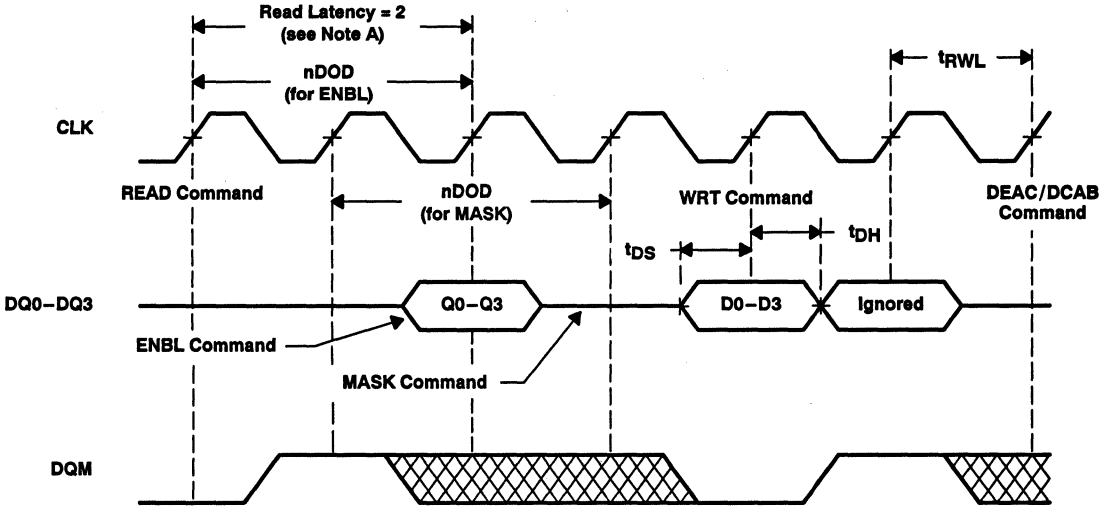


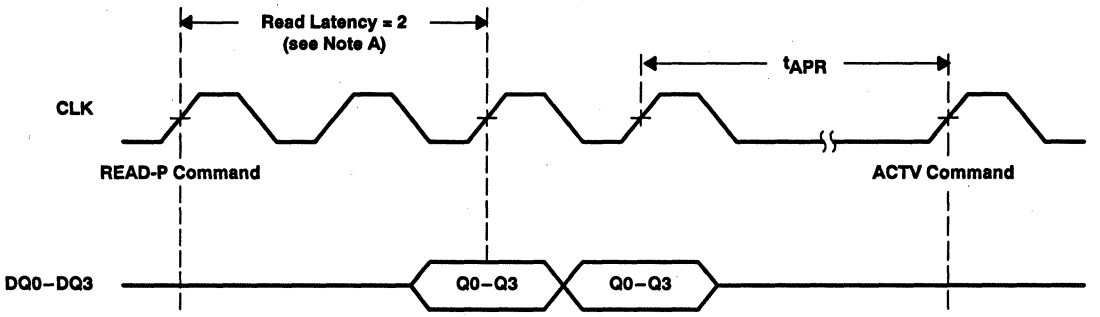
Figure 15. Input-Attribute Parameters



NOTE A: For this example, assume read latency = 2 and burst length = 2.

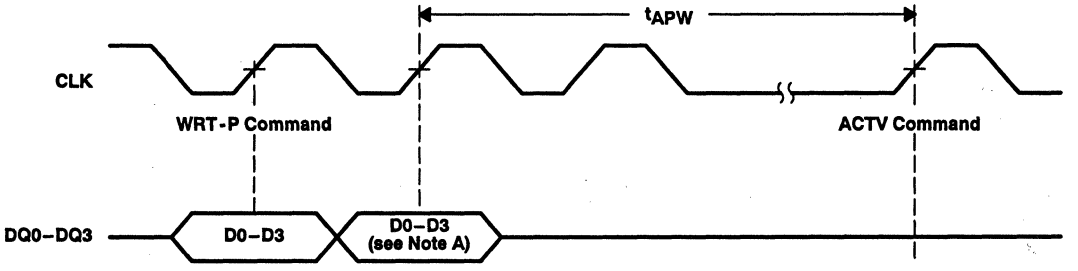
Figure 16. DQ Masking

PARAMETER MEASUREMENT INFORMATION



NOTE A: For this example, assume read latency = 2 and burst length = 2.

Figure 17. Read-Automatic Deactivate (Autoprecharge)



NOTE A: For this example, the burst length = 2.

Figure 18. Write-Automatic Deactivate (Autoprecharge)

PARAMETER MEASUREMENT INFORMATION

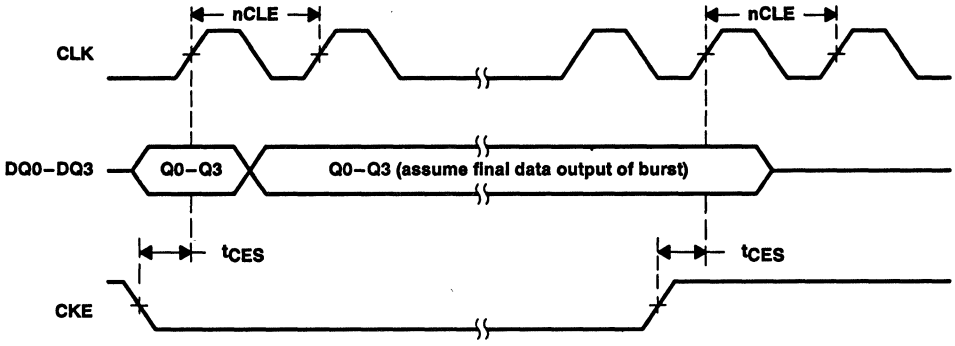


Figure 19. CLK-Suspend Operation

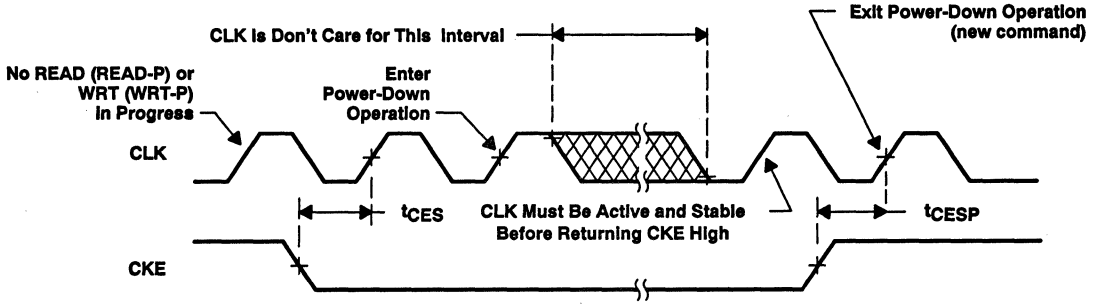
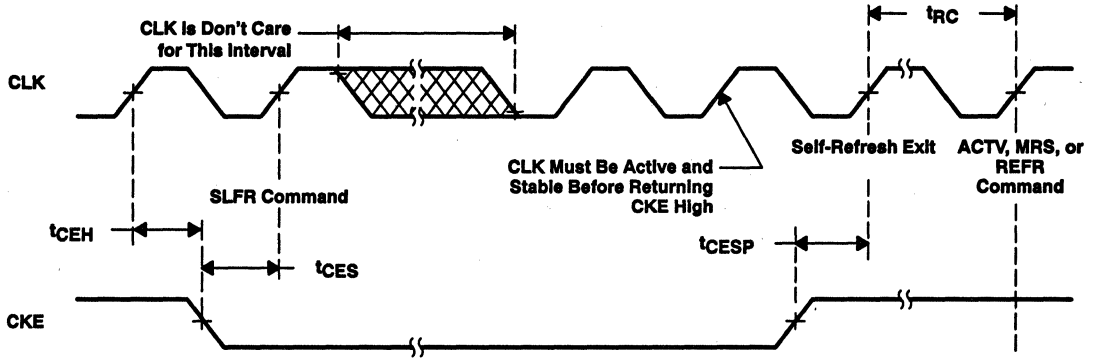


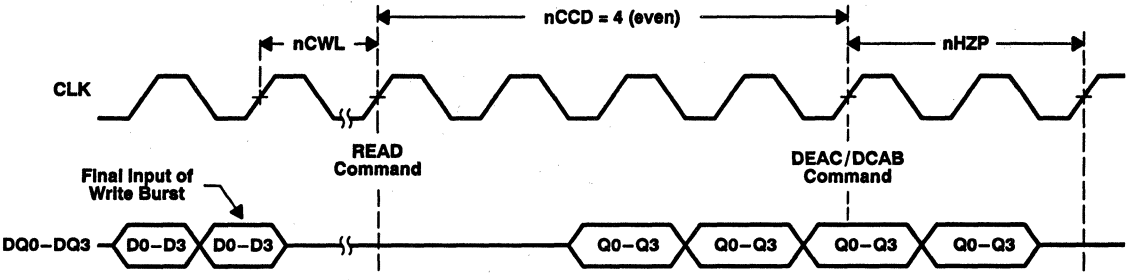
Figure 20. Power-Down Operation

PARAMETER MEASUREMENT INFORMATION



NOTE A: Assume both banks are previously deactivated.

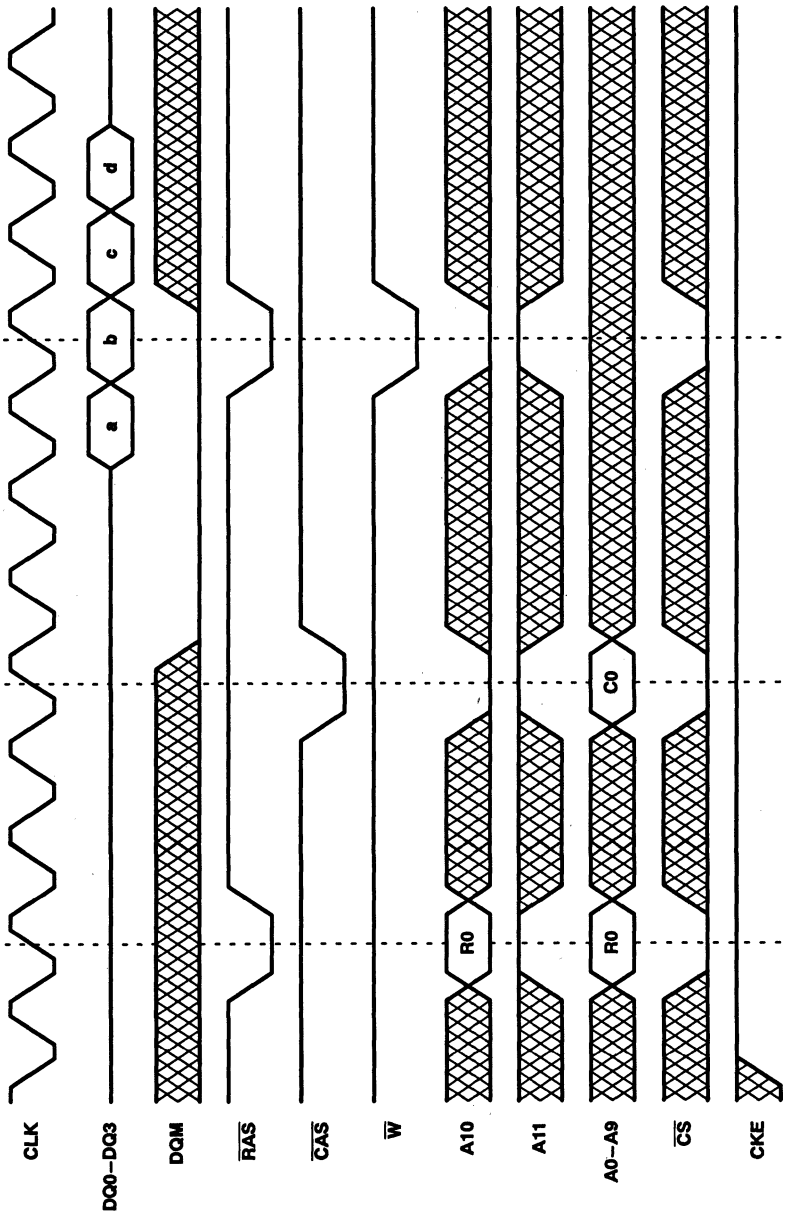
Figure 21. Self-Refresh Entry/Exit



NOTE A: Assume read latency = 2 and burst length = 8.

Figure 22. Write Burst Followed by DEAC/DCAB-Interrupted Read

PARAMETER MEASUREMENT INFORMATION

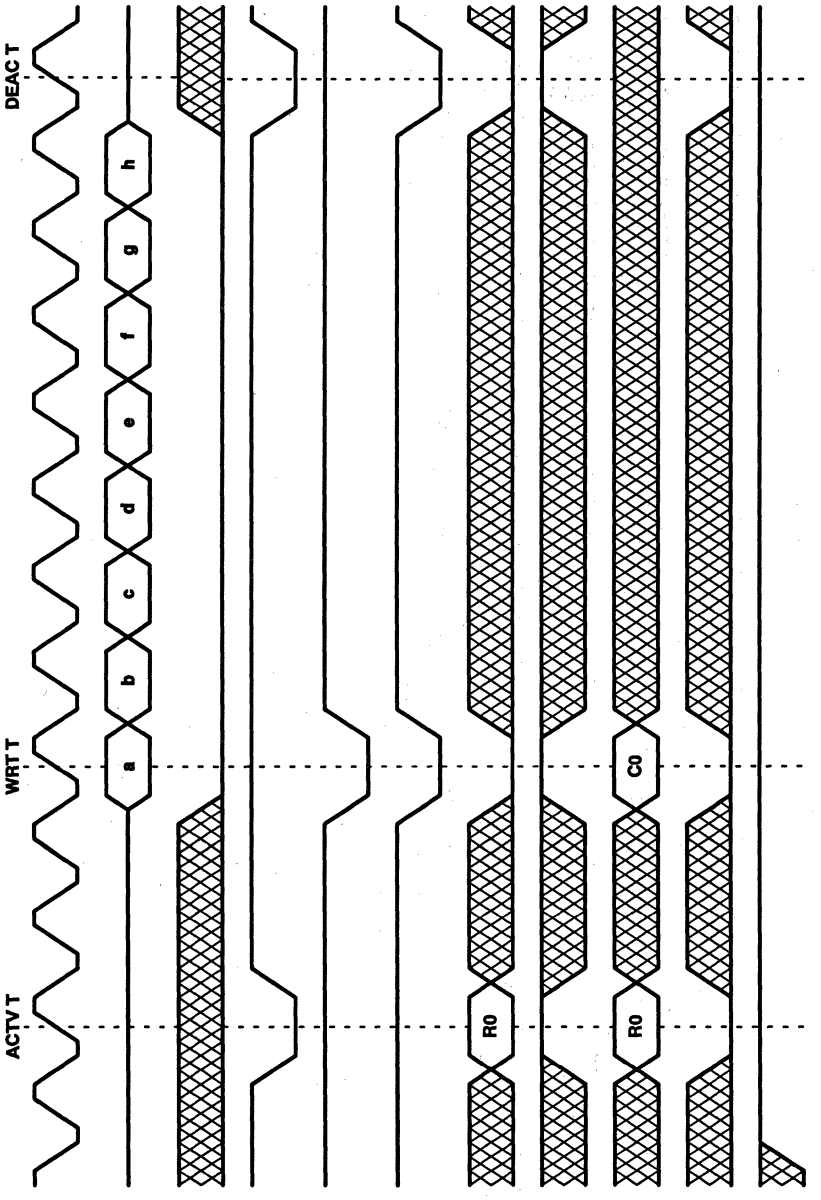


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d
Q	T	R0	C0†	C0 + 1	C0 + 2	C0 + 3

† Column-address sequence depends on programmed burst type and C0 (see Table 5).
NOTE A: This example illustrates minimum t_{RCD} and nEP for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 23. Read Burst (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

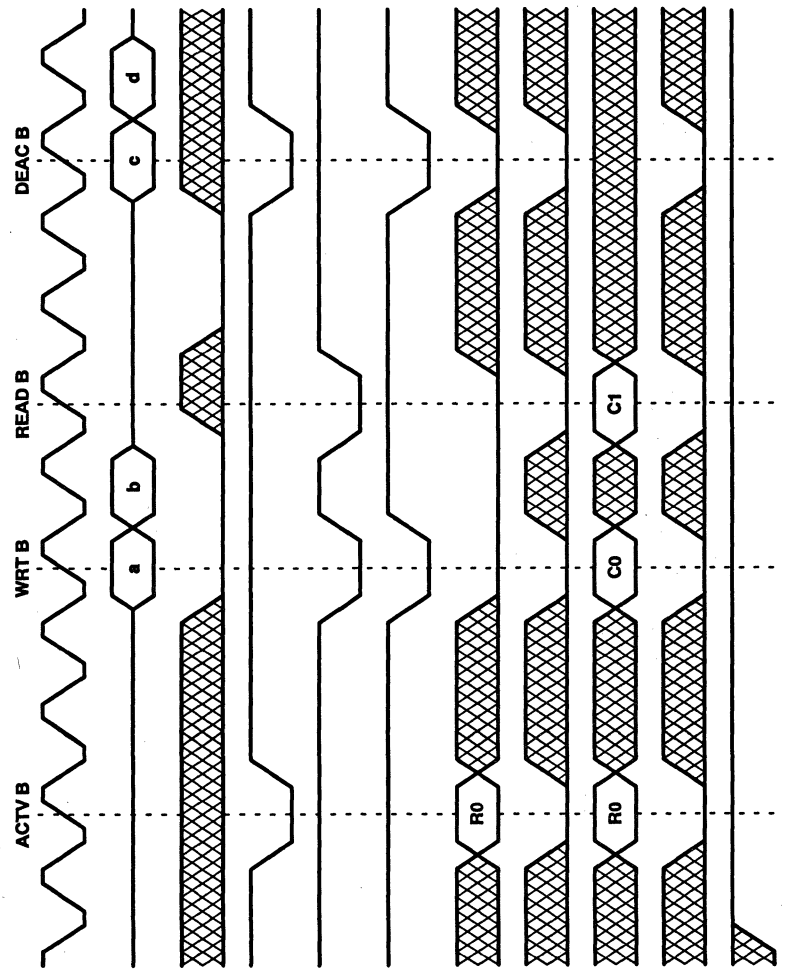


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
D	T	R0	C0†	C0 + 1	C0 + 2	C0 + 3	C0 + 4	C0 + 5	C0 + 6	C0 + 7

† Column-address sequence depends on programmed burst type and C0 (see Table 6).
NOTE A: This example illustrates minimum t_{RWL} for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 24. Write Burst (burst length = 8)

PARAMETER MEASUREMENT INFORMATION

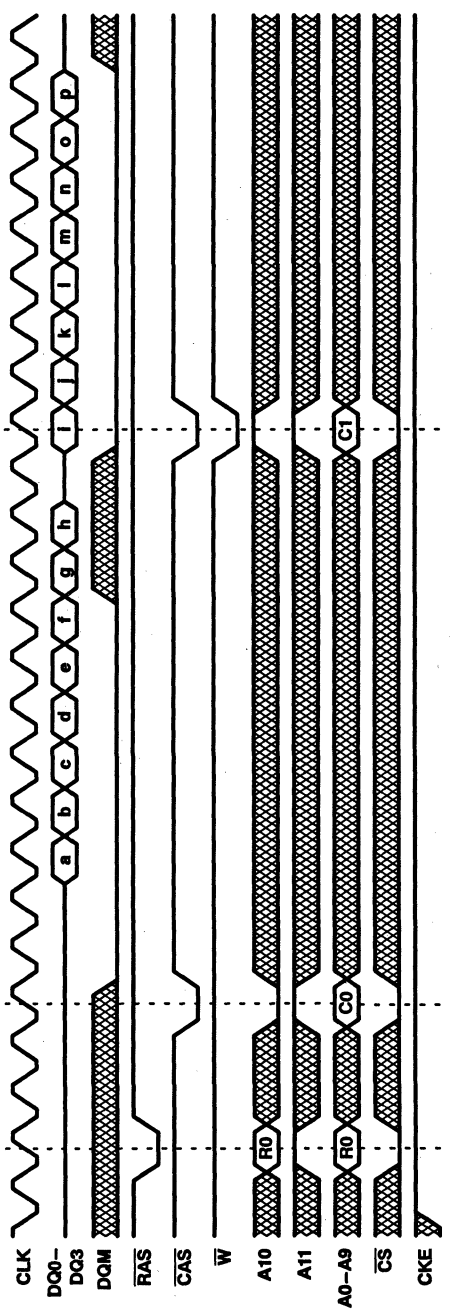


BURST TYPE	BANK	ROW	BURST CYCLE			
(D/Q)	(B/T)	ADDR	a	b	c	d
D	B	R0	C0†	C0 + 1		
Q	B	R0			C1‡	C1 + 1

† Column-address sequence depends on programmed burst type and C0 (see Table 4).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 4).
NOTE A: This example illustrates minimum t_{RCD} for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 25. Write-Read Burst (read latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION

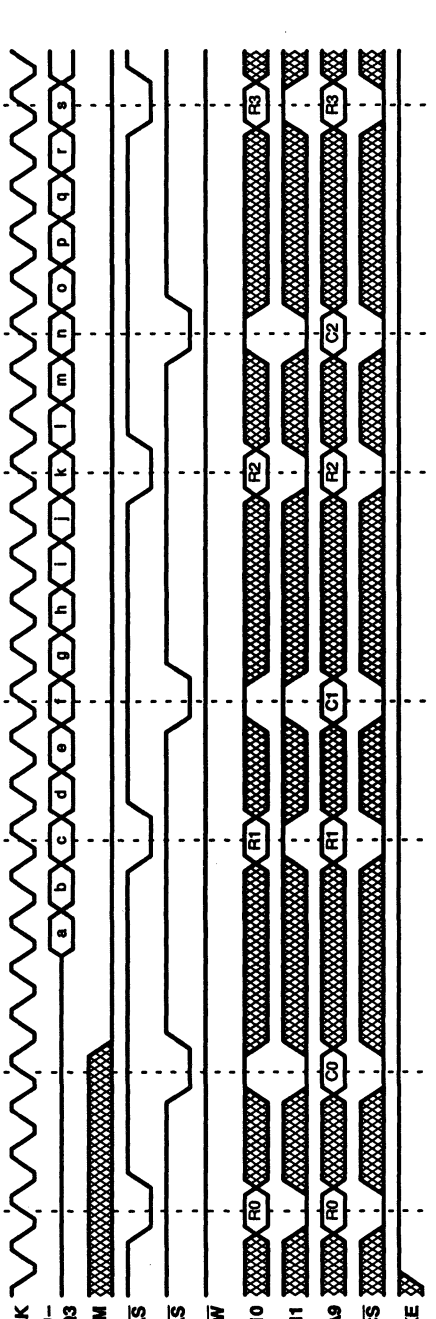


BURST TYPE	BANK	ROW	BURST CYCLE															
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p
Q	T	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7								
D	T	R0									C1‡	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7

† Column-address sequence depends on programmed burst type and C0 (see Table 6).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 6).
NOTE A: This example illustrates minimum t_{RCD} for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 26. Read-Write Burst With Automatic Deactivate (read latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION

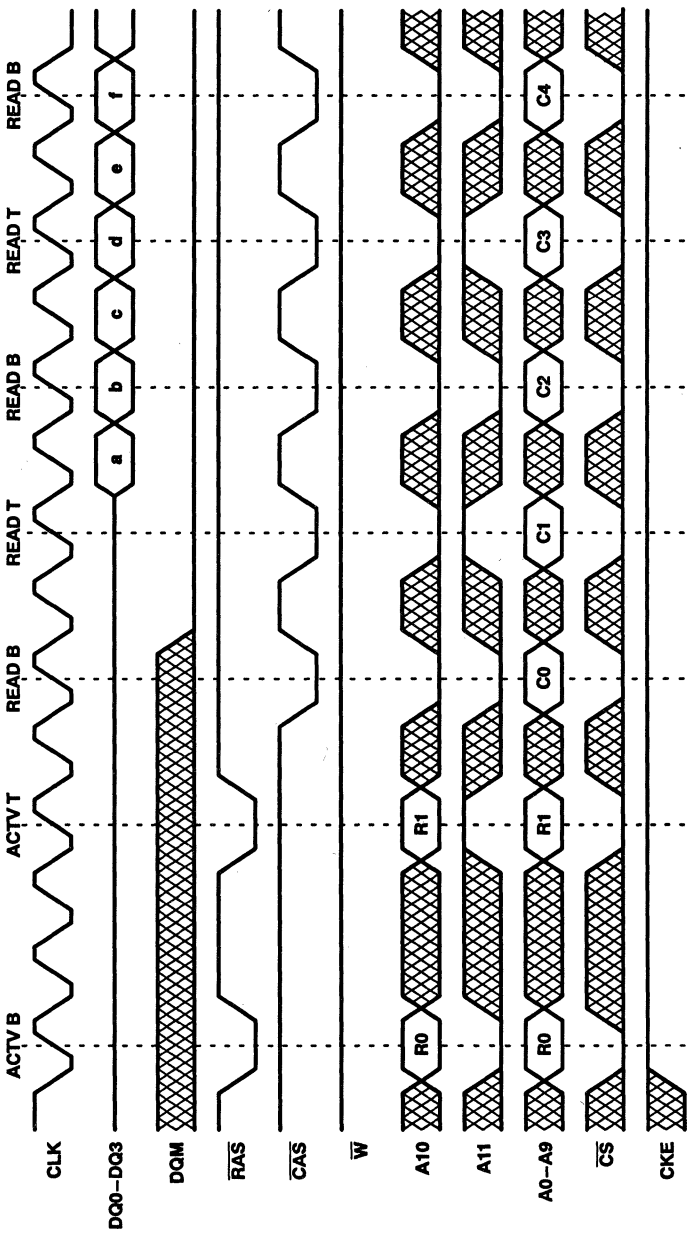


BURST TYPE	BANK	ROW	BURST CYCLE																			
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	....
Q	B	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7												
Q	T	R1									C1‡	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7				
Q	B	R2																	C2§	C2+1	C2+2	....

† Column-address sequence depends on programmed burst type and C0 (see Table 6).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 6).
§ Column-address sequence depends on programmed burst type and C2 (see Table 6).
NOTE A: This example illustrates minimum t_{RCD} for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 27. Two-Bank Row-Interleaving Read Bursts With Automatic Deactivate (read latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION

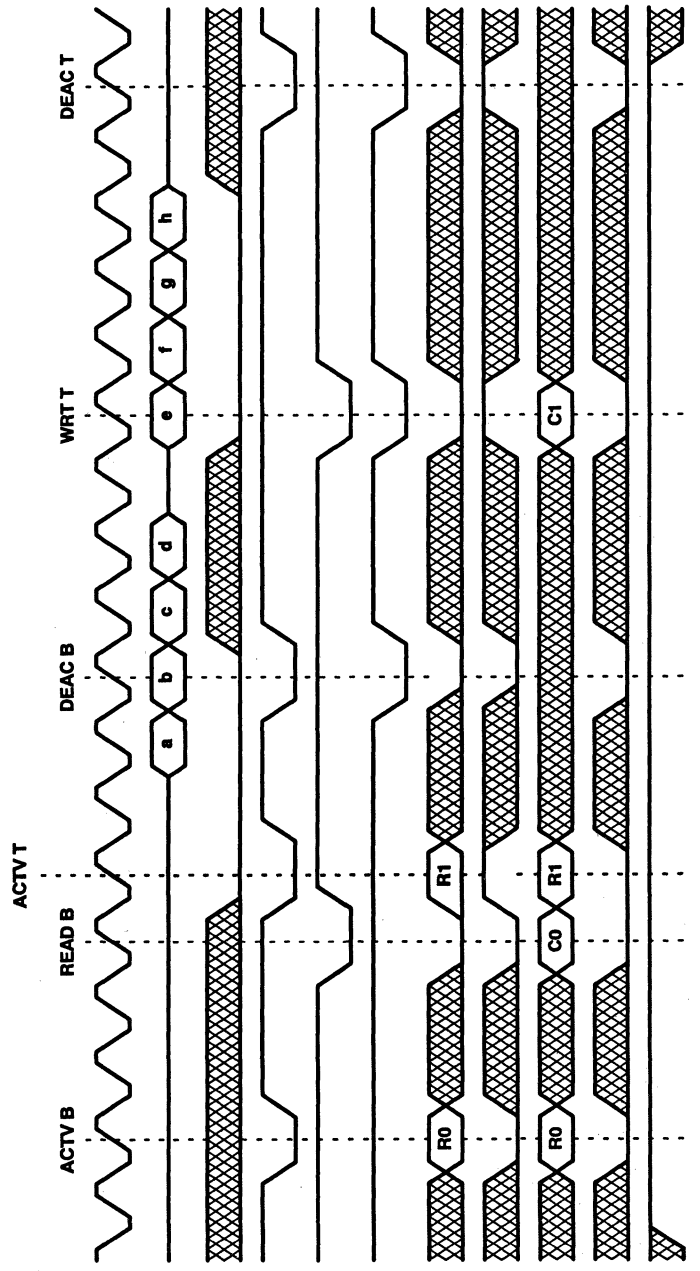


BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	...	...
Q	B	R0	C0†	C0 + 1	C1‡	C1 + 1	C2§	C2 + 1	...	...
Q	T	R1								
Q	B	R0								
...	...	...							...	...

† Column-address sequence depends on programmed burst type and C0 (see Table 4).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 4).
§ Column-address sequence depends on programmed burst type and C2 (see Table 4).

Figure 28. Two-Bank Column-Interleaving Read Bursts (read latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION

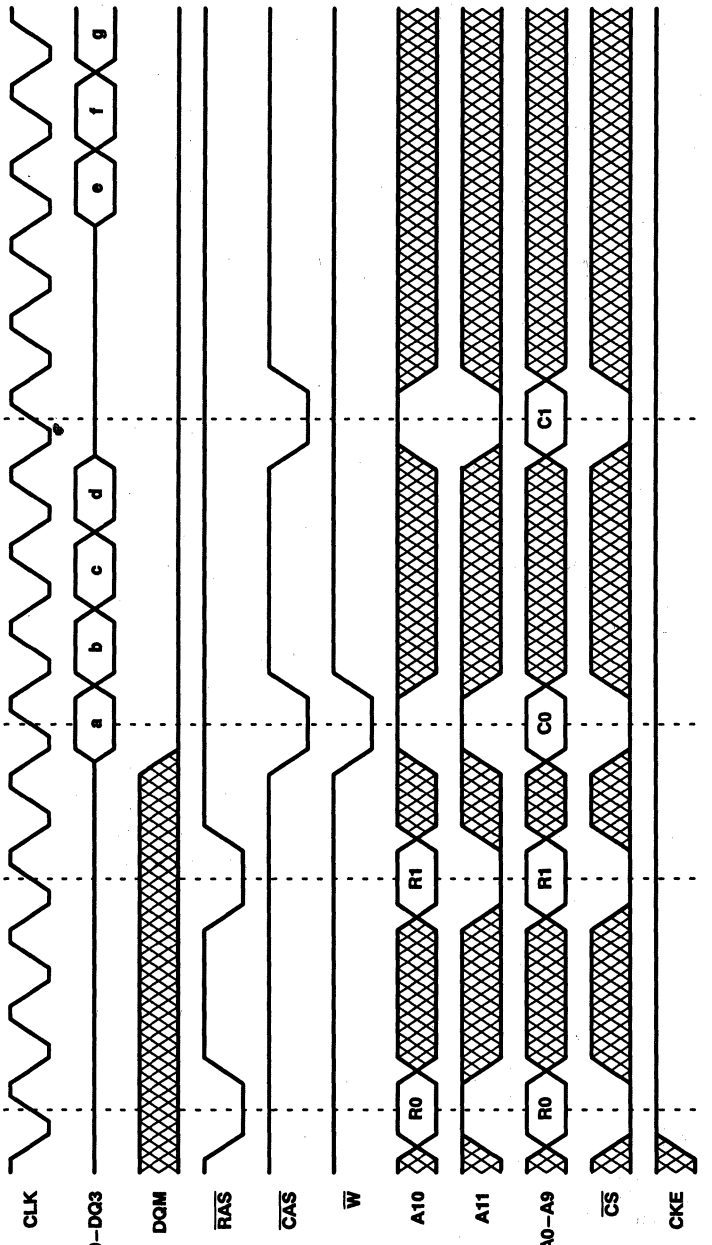


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	B	R0	C0†	C0+1	C0+2	C0+3				
D	T	R1					C1‡	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and C0 (see Table 5).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 5).
NOTE A: This example illustrates a minimum t_{RCD} and nEP read burst, and a minimum t_{RWL} write burst for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 29. Read-Burst Bank B, Write-Burst Bank T (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

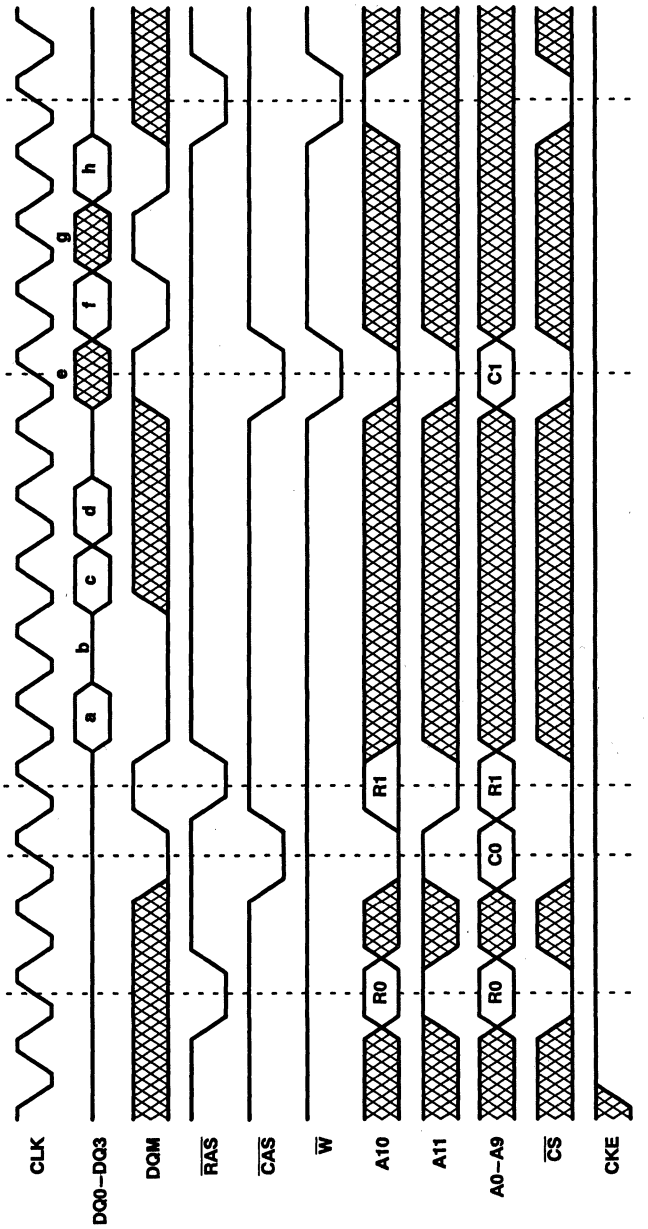


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
D	T	R0	C0†	C0+1	C0+2	C0+3				
Q	B	R1					C1‡	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and C0 (see Table 5).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 5).
NOTE A: This example illustrates minimum nCWL for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 30. Write-Burst Bank T, Read-Burst Bank B With Automatic Deactivate (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

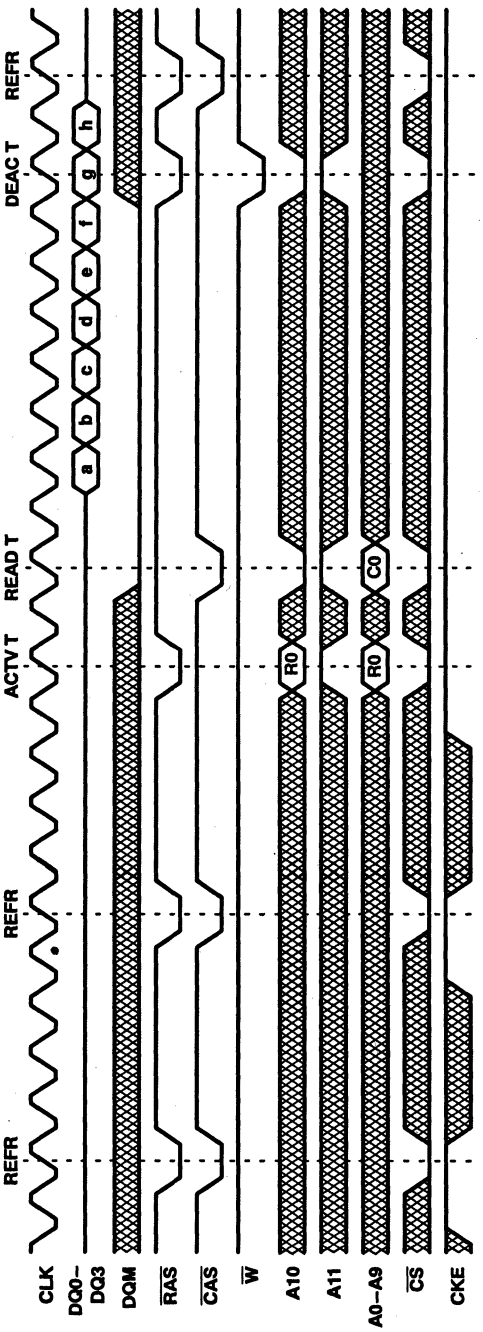


BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h
Q	T	R0	C0†	C0+1	C0+2	C0+3				
D	B	R1					C1‡	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and C0 (see Table 5).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 5).
NOTE A: This example illustrates a minimum t_{RCD} read burst and minimum t_{RWL} write burst for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 31. Use Of DQM for Output and Data-In Cycle Masking (read-burst bank T, write-burst bank B, deactivate all banks) (read latency = 2, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



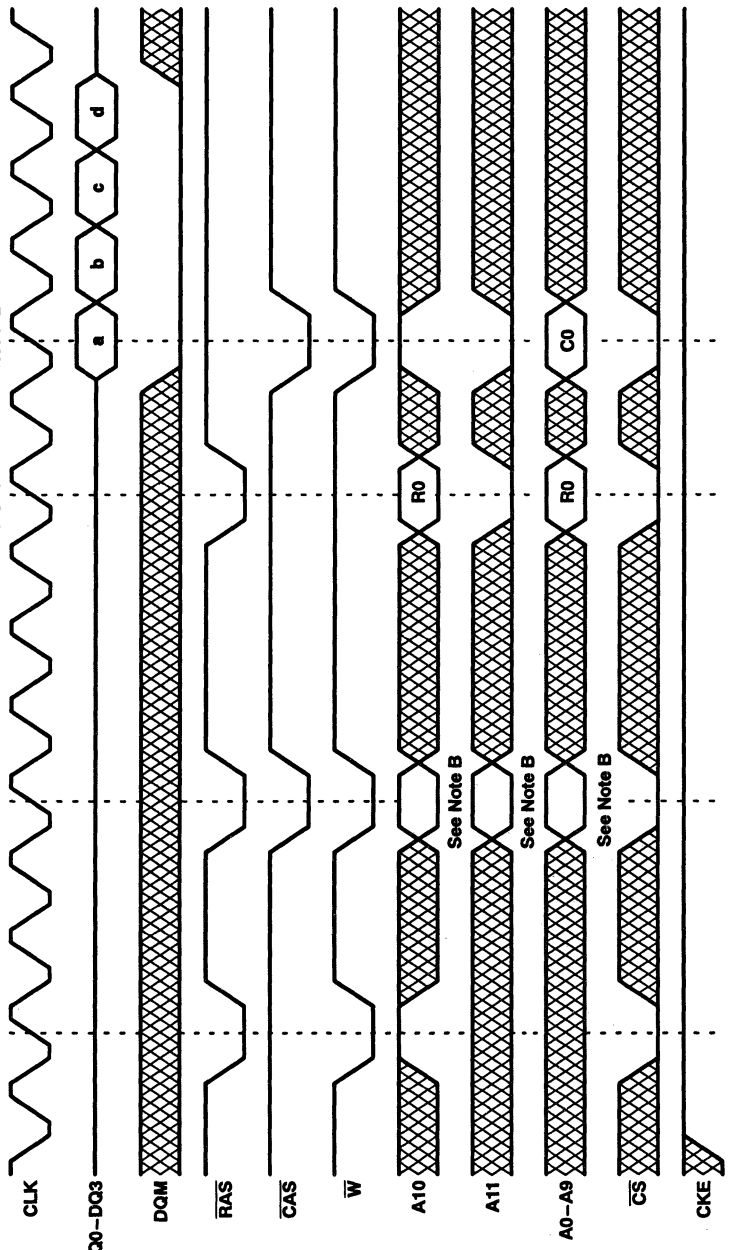
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	T	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7

† Column-address sequence depends on programmed burst type and C0 (see Table 6).

NOTE A: This example illustrates minimum t_{RC}, t_{RCD}, nEP, and t_{RP} for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 32. Refresh Cycles (refreshes followed by read burst followed by refresh) (read latency = 2, burst length = 8)

PARAMETER MEASUREMENT INFORMATION



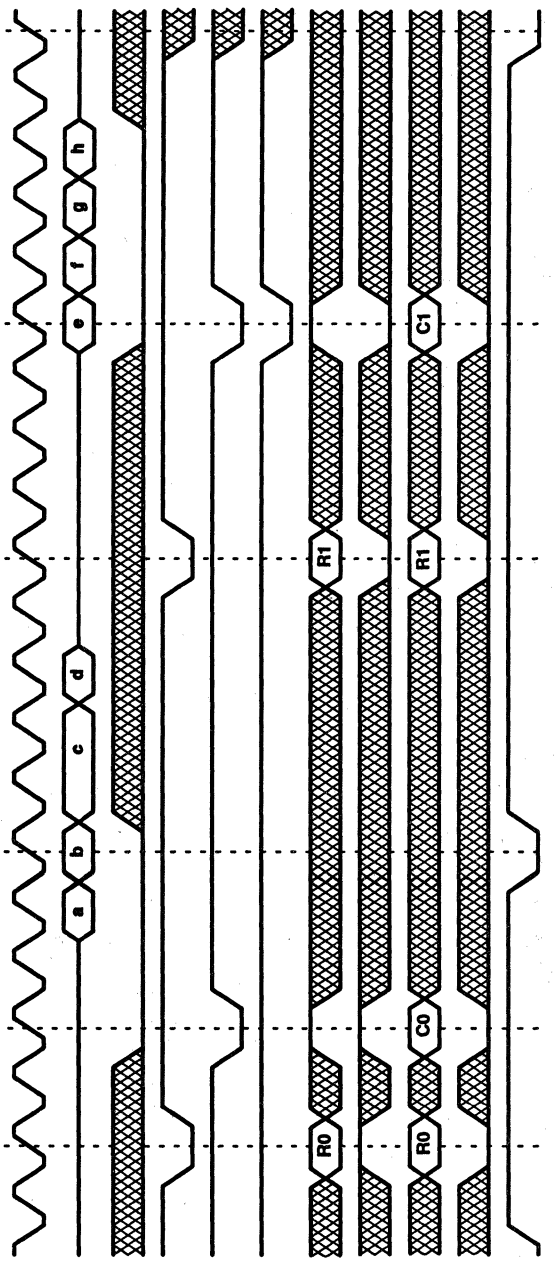
BURST TYPE	BANK	ROW	BURST CYCLE			
(D/Q)	(B/T)	ADDR	a	b	c	d
D	B	R0	C0†	C0+1	C0+2	C0+3

† Column-address sequence depends on programmed burst type and C0 (see Table 5).

NOTES: B. This example illustrates minimum t_{RCD} for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.
C. Refer to Figure 1

**Figure 33. Mode-Register Programming (deactivate all, mode program, write burst with automatic deactivate)
(read latency = 2, burst length = 4)**

PARAMETER MEASUREMENT INFORMATION



BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	T	R0	C0†	C0+1	C0+2	C0+3				
D	B	R1					C1‡	C1+1	C1+2	C1+3

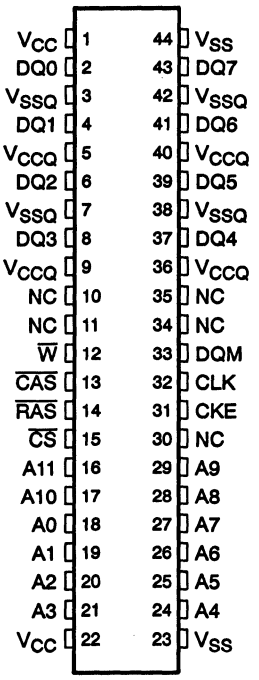
† Column-address sequence depends on programmed burst type and C0 (see Table 5).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 5).
NOTE A: This example illustrates minimum t_{RCD} for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 34. Use of CKE for Clock Gating (Hold) and Standby Mode (read-burst bank T with hold, write-burst bank B, standby mode) (read latency = 2, burst length = 4)

- **Organization . . . 1M × 8 × 2 Banks**
- **3.3-V Power Supply (±10% Tolerance)**
- **Two Banks for On-Chip Interleaving (Gapless Accesses)**
- **High Bandwidth – Up to 100-MHz Data Rates**
- **Burst Length Programmable to 1, 2, 4, or 8**
- **Programmable Output Sequence – Serial or Interleave**
- **Chip Select and Clock Enable for Enhanced-System Interfacing**
- **Cycle-by-Cycle DQ-Bus Mask Capability**
- **Programmable Read Latency From Column Address**
- **Self-Refresh Capability**
- **High-Speed, Low-Noise LVTTL Interface**
- **Power-Down Mode**
- **Compatible With JEDEC Standards**
- **4K Refresh (Total for Both Banks)**
- **2-Bit Prefetch Architecture for High Speed Performance**
- **Performance Ranges:**

	SYNCHRONOUS CLOCK CYCLE TIME	ACTV COMMAND TO READ OR WRITE COMMAND	REFRESH TIME INTERVAL
	t_{CK} (MIN)	t_{RCD} (MIN)	t_{REF} (MAX)
'626802-10	10 ns	30 ns	64 ms
'626802-12	12.5 ns	35 ns	64 ms
'626802-15	15 ns	40 ns	64 ms

DGE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs A0–A10 Row Addresses A0–A8 Column Addresses A10 Automatic-Precharge Select
A11	Bank Select
$\overline{CAS}$	Column-Address Strobe
CKE	Clock Enable
CLK	System Clock
$\overline{CS}$	Chip Select
DQ0–DQ7	SDRAM Data Input/Data Output
DQM	Data/Output Mask Enable
NC	No External Connect
$\overline{RAS}$	Row-Address Strobe
V_{CC}	Power Supply (3.3 V Typ)
V_{CCQ}	Power Supply for Output Drivers (3.3 V Typ)
V_{SS}	Ground
V_{SSQ}	Ground for Output Drivers
$\overline{W}$	Write Enable

description

The TMS626802 series are high-speed 16777216-bit synchronous dynamic random-access memories (DRAMs) organized as two banks of 1048576 words with eight bits per word.

All inputs and outputs of the TMS626802 series are compatible with the low-voltage TTL (LVTTL) interface.

The synchronous DRAM employs state-of-the-art enhanced performance implanted CMOS (EPIC™) technology for high performance, reliability, and low power. All inputs and outputs are synchronized with the CLK input to simplify system design and enhance use with high-speed microprocessors and caches.

The TMS626802 synchronous DRAM is available in a 400-mil, 44-pin surface-mount TSOP (II) package (DGE suffix).

EPIC is a trademark of Texas Instruments Incorporated.

operation

All inputs of the '626802 synchronous DRAM are latched on the rising edge of the system (synchronous) clock. The outputs, DQ0–DQ7, are also referenced to the rising edge of CLK. The '626802 has two banks that are accessed independently. A bank must be activated before it can be accessed (read from or written to). Refresh cycles refresh both banks alternately.

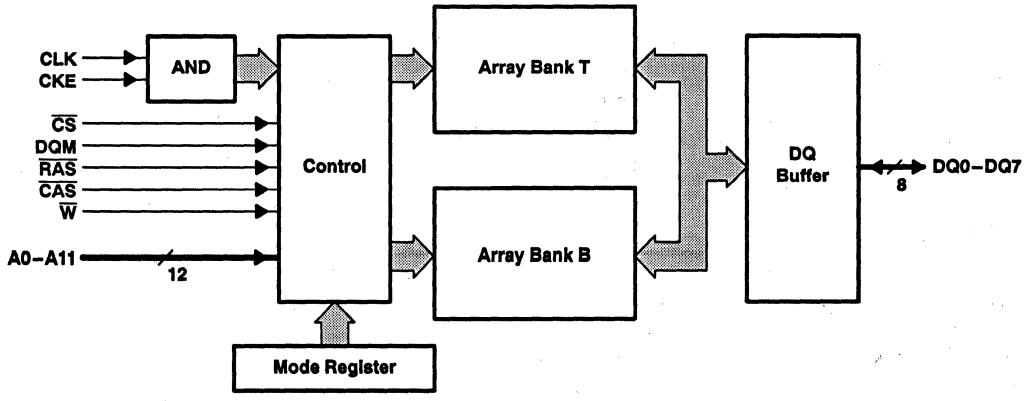
Five basic commands or functions control most operations of the '626802:

- Bank activate/row-address entry
- Column-address entry/write operation
- Column-address entry/read operation
- Bank deactivate
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ (CBR)
- Self-refresh entry

Additionally, operation can be controlled by three methods: using chip select ($\overline{\text{CS}}$) to select/deselect the devices, using DQM to enable/mask the DQ signals on a cycle-by-cycle basis, or using CKE to suspend (or gate) the CLK input. The device contains a mode register that must be programmed for proper operation.

Tables 1 through 3 show the various operations that are available on the '626802. These truth tables identify the command and/or operations and their respective mnemonics. Each truth table is followed by a legend that explains the abbreviated symbols. An access operation refers to any READ (READ-P) or WRT (WRT-P) command in progress at cycle n. Access operations include the cycle upon which the READ (READ-P) or WRT (WRT-P) command is entered and all subsequent cycles through the completion of the access burst.

functional block diagram



operation (continued)

Table 1. Basic-Command Truth Table†

COMMAND	STATE OF BANK(S)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A11	A10	A9–A0	MNEMONIC
Mode register set	T = deac B = deac	L	L	L	L	X	X	A9=X A8=0 A7=0 A6–A0=V	MRS
Bank deactivate (precharge)	X	L	L	H	L	BS	L	X	DEAC
Deactivate all banks	X	L	L	H	L	X	H	X	DCAB
Bank activate/row-address entry	SB = deac	L	L	H	H	BS	V	V	ACTV
Column-address entry/write operation	SB = actv	L	H	L	L	BS	L	V	WRT
Column-address entry/write operation with automatic deactivate	SB = actv	L	H	L	L	BS	H	V	WRT-P
Column-address entry/read operation	SB = actv	L	H	L	H	BS	L	V	READ
Column-address entry/read operation with automatic deactivate	SB = actv	L	H	L	H	BS	H	V	READ-P
Burst stop	SB = actv	L	H	H	L	X	X	X	STOP
No operation	X	L	H	H	H	X	X	X	NOOP
Control-input inhibit/no operation	X	H	X	X	X	X	X	X	DESL
CBR refresh‡	T = B = deac	L	L	L	H	X	X	X	REFR

† For execution of these commands on cycle n, CKE (n) must be high and satisfy t_{CESP} from power-down exit (PDE), t_{CES} and nCLE from clock-suspend (HOLD) exit, and t_{CESP} and t_{RC} from self-refresh (SLFR) exit. DQM (n) is a don't care.

‡ CBR or self-refresh entry requires that all banks be deactivated or in an idle state prior to the command entry.

Legend:

- L = Logic low
- H = Logic high
- X = Don't care
- V = Valid
- T = Bank T
- B = Bank B
- actv = Activated
- deac = Deactivated
- BS = Logic high to select bank T; logic low to select bank B
- SB = Bank selected by A11 at cycle n

operation (continued)

Table 2. CKE-Use Command Truth Table†

COMMAND	STATE OF BANK(S)	CKE (n−1)	CKE (n)	$\overline{CS}$ (n)	$\overline{RAS}$ (n)	$\overline{CAS}$ (n)	$\overline{W}$ (n)	MNEMONIC
Self-refresh entry	T = B = deac	H	L	L	L	L	H	SLFR
Power-down entry at n + 1	T = B = no access operation‡	H	L	L	H	H	H	PDE
		H	L	H	X	X	X	PDE
Self-refresh exit	T = B = self refresh	L	H	L	H	H	H	—
		L	H	H	X	X	X	—
Power-down exit	T = B = power down	L	H	X	X	X	X	—
CLK suspend at n+1	T or B = access operation‡	H	L	X	X	X	X	HOLD
CLK suspend exit at n+1	T or B = access operation‡	L	H	X	X	X	X	—

† For execution of these commands, A0–A11 (n) and DQM (n) are don't cares.

‡ An access operation refers to any READ (READ-P) or WRT (WRT-P) command in progress at cycle n. Access operations include the cycle upon which the READ (READ-P) or WRT (WRT-P) command is entered and all subsequent cycles through the completion of the access burst.

Legend:

n = CLK cycle number
L = Logic low
H = Logic high
X = Don't care
T = Bank T
B = Bank B
deac = Deactivated

operation (continued)

Table 3. DQM-Use Command Truth Table†

COMMAND	STATE OF BANK(S)	DQM (n)	DATA IN (n)	DATA OUT (n+2)	MNEMONIC
—	T = deac and B = deac	X	N/A	Hi-Z	—
—	T = actv and B = actv (no access operation)‡	X	N/A	Hi-Z	—
Data-in enable	T = write or B = write	L	V	N/A	ENBL
Data-in mask	T = write or B = write	H	M	N/A	MASK
Data-out enable	T = read or B = read	L	N/A	V	ENBL
Data-out mask	T = read or B = read	H	N/A	Hi-Z	MASK

† For execution of these commands, CKE (n) must be high and satisfy t_{CESP} from power-down exit (PDE), t_{CES} and nCLE from clock-suspend (HOLD) exit, and t_{CESP} and t_{RC} from self-refresh (SLFR) exit. $\overline{CS}$ (n), $\overline{RAS}$ (n), $\overline{CAS}$ (n), $\overline{W}$ (n), and A0–A11 (n) are don't cares.

‡ An access operation refers to any READ (READ-P) or WRT (WRT-P) command in progress at cycle n. Access operations include the cycle upon which the READ (READ-P) or WRT (WRT-P) command is entered and all subsequent cycles through the completion of the access burst.

Legend:

n = CLK cycle number
L = Logic low
H = Logic high
X = Don't care
V = Valid
M = Masked input data
N/A = Not applicable
T = Bank T
B = Bank B
actv = Activated
deac = Deactivated
write = Activated and accepting data in on cycle n
read = Activated and delivering data out on cycle n + 2

burst sequence

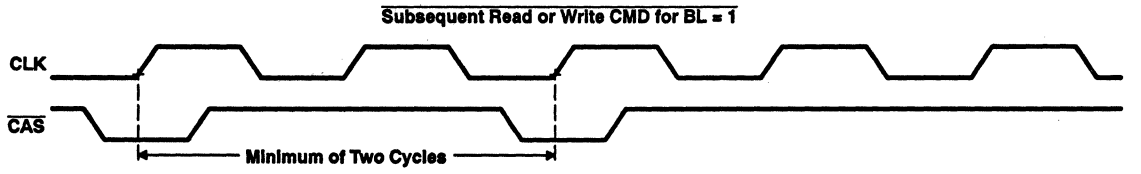
All data for the '626802 is written or read in a burst fashion; that is, a single starting address is entered into the device and the '626802 internally accesses a sequence of locations based on that starting address. Some of the subsequent accesses after the first can be at preceding as well as succeeding column addresses, depending on the starting address entered. This sequence can be programmed to follow either a serial burst or an interleave burst (see Tables 4 through 6). The length of the burst sequence can be user programmed to be either 1, 2, 4, or 8 accesses. After a read burst is completed (as determined by the programmed-burst length), the outputs are in the high-impedance state until the next read access is initiated.

Table 4. 2-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A0			
	DECIMAL		BINARY	
	START	2ND	START	2ND
Serial	0	1	0	1
	1	0	1	0
Interleave	0	1	0	1
	1	0	1	0

Table 5. 4-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A1–A0							
	DECIMAL				BINARY			
	START	2ND	3RD	4TH	START	2ND	3RD	4TH
Serial	0	1	2	3	00	01	10	11
	1	2	3	0	01	10	11	00
	2	3	0	1	10	11	00	01
	3	0	1	2	11	00	01	10
Interleave	0	1	2	3	00	01	10	11
	1	0	3	2	01	00	11	10
	2	3	0	1	10	11	00	01
	3	2	1	0	11	10	01	00



NOTE: For burst sequence of one, subsequent read or write commands must be done at least two clock cycles from initial read or write command (see timing diagram above).

burst sequence (continued)

Table 6. 8-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A2–A0															
	DECIMAL								BINARY							
	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH
Serial	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	2	3	4	5	6	7	0	001	010	011	100	101	110	111	000
	2	3	4	5	6	7	0	1	010	011	100	101	110	111	000	001
	3	4	5	6	7	0	1	2	011	100	101	110	111	000	001	010
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	6	7	0	1	2	3	4	101	110	111	000	001	010	011	100
	6	7	0	1	2	3	4	5	110	111	000	001	010	011	100	101
	7	0	1	2	3	4	5	6	111	000	001	010	011	100	101	110
Interleave	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	0	3	2	5	4	7	6	001	000	011	010	101	100	111	110
	2	3	0	1	6	7	4	5	010	011	000	001	110	111	100	101
	3	2	1	0	7	6	5	4	011	010	001	000	111	110	101	100
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	4	7	6	1	0	3	2	101	100	111	110	001	000	011	010
	6	7	4	5	2	3	0	1	110	111	100	101	010	011	000	001
	7	6	5	4	3	2	1	0	111	110	101	100	011	010	001	000

latency

The beginning data-output cycle of a read burst can be programmed to occur 1, 2, or 3 CLK cycles after the read command (see setting the mode register). This feature allows the user to adjust the '626802 to operate in accordance with the system's capability to latch the data output from the '626802. The delay between the READ command and the beginning of the output burst is known as read latency (also known as $\overline{CAS}$ latency). After the initial output cycle begins, the data burst occurs at the CLK frequency without any intervening gaps. Use of minimum read latencies is restricted based on the particular maximum frequency rating of the '626802.

There is no latency for data-in cycles (write latency). The first data-in cycle of a write burst is entered at the same rising edge of CLK on which the WRT command is entered. The write latency is fixed and not determined by the mode-register contents.

two-bank operation

The '626802 contains two independent banks that can be accessed individually or in an interleaved fashion. Each bank must be activated with a row address before it can be accessed. Each bank must then be deactivated before it can be activated again with a new row address. The bank-activate/row-address-entry command (ACTV) is entered by holding $\overline{RAS}$ low, $\overline{CAS}$ high, $\overline{W}$ high, and A11 valid on the rising edge of CLK. A bank can be deactivated either automatically during a READ (READ-P) or a WRT (WRT-P) command or by use of the deactivate-bank (DEAC) command. Both banks can be deactivated at once by use of the DCAB command (see Table 1 and the bank deactivation description).

two-bank row-access operation

The two-bank feature allows the user to access information on random rows at a higher rate of operation than is possible with a standard DRAM. This is accomplished by activating one bank with a row address and, while the data stream is being accessed to/from that bank, activating the second bank with another row address. When the data stream to/from the first bank is complete, the data stream to/from the second bank can begin without interruption. After the second bank is activated, the first bank can be deactivated to allow the entry of a new row address for the next round of accesses. In this manner, operation can continue in an interleaved fashion. Figure 26 shows an example of two-bank row interleaving with automatic deactivate for the case of read latency of 3 and a burst length of 8.

two-bank column-access operation

The availability of two banks allows the access of data from random starting columns between banks at a higher rate of operation. After activating each bank with a row address (ACTV command), A11 can be used to alternate READ or WRT commands between the banks to provide gapless accesses at the CLK frequency, provided all specified timing requirements are met. Figure 27 is an example of two-bank column interleaving with a read latency of 3 and a burst length of 2.

bank deactivation (precharge)

Both banks can be simultaneously deactivated (placed in precharge) by using the DCAB command. A single bank can be deactivated by using the DEAC command. The DEAC command is entered identically to the DCAB command except that A10 must be low and A11 selects the bank to be precharged as shown in Table 1. A bank can also be deactivated automatically by using A10 during a READ or WRT command. If A10 is held high during the entry of a READ or WRT command, the accessed bank (selected by A11) automatically deactivates upon completion of the access burst. If A10 is held low during READ or WRT command entry, that bank remains active following the burst. The READ and WRT commands with automatic deactivation are denoted as READ-P and WRT-P.

chip select ($\overline{CS}$)

$\overline{CS}$ can be used to select or deselect the '626802 for command entry, which might be required for multiple memory-device decoding. If $\overline{CS}$ is held high on the rising edge of CLK (DESL command), the device does not respond to $\overline{RAS}$, $\overline{CAS}$, or $\overline{W}$ until the device is selected again. Device select is accomplished by holding $\overline{CS}$ low on the rising edge of CLK. Any other valid command can be entered simultaneously on the same rising CLK edge of the select operation. The device can be selected/deselected on a cycle-by-cycle basis (see Tables 1 and 2). The use of $\overline{CS}$ does not affect an access burst that is in progress; the DESL command can only restrict $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ input to the '626802.

data/output mask

Masking of individual data cycles within a burst sequence can be accomplished by use of the MASK command (see Table 3). If DQM is held high on the rising edge of CLK during a write burst, the incident data word (referenced to the same rising edge of CLK) on DQ0–DQ7 is ignored. If DQM is held high on the rising edge of CLK for a read burst, DQ0–DQ7 referenced to the second rising edge of CLK are in the high-impedance state. The application of DQM to data-out cycles (READ burst) involves a latency of two CLK cycles, but the application of DQM to data-in cycles (WRITE burst) has no latency. The MASK command (or its opposite, the ENBL command) is performed on a cycle-by-cycle basis, allowing the user to gate any individual data cycle or cycles within either a read- or a write-burst sequence. Figure 15 shows an example of data/output masking.

NOTE: Data masking using DQM input is not supported when the mode register is set for read latency of one and burst length of one. If the mode register is in this mode, the DQM pin should be held low.

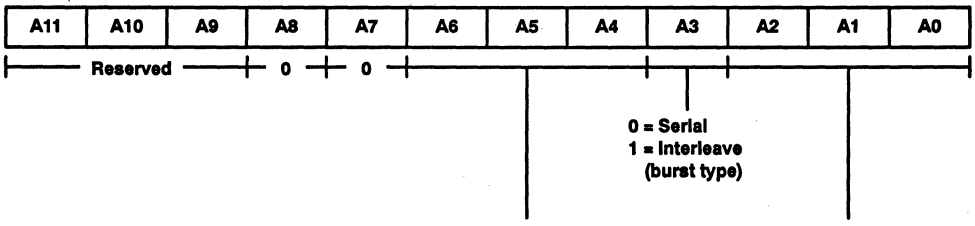
CLK suspend/power-down mode

For normal device operation, CKE should be held high to enable CLK. If CKE goes low during the execution of a READ (READ-P) or WRT (WRT-P) operation, the state of the DQ bus at the immediate next rising edge of CLK is frozen at its current state, and no further inputs are accepted until CKE is returned high. This is known as a CLK suspend operation, and its execution is denoted as a HOLD command. The device resumes operation from the point at which it was placed in suspension, beginning with the second rising edge of CLK after CKE is returned high.

If CKE is brought low when no READ (READ-P) or WRT (WRT-P) command is in progress, the device enters power-down mode. If both banks are deactivated when power-down mode is entered, power consumption is reduced to the minimum. Power-down mode can be used during row-active or CBR-refresh periods to reduce input buffer power. After power-down mode is entered, no further inputs are accepted until CKE returns high. To ensure that data in the device remains valid during the power-down mode, the self-refresh command (SLRF) must be executed concurrently with the power-down entry (PDE) command. When exiting power-down mode, new commands can be entered on the first CLK edge after CKE returns high, provided that the setup time (t_{CESP}) is satisfied. Table 2 shows the command configuration for a CLK suspend/power-down operation, and Figures 18 and 19 show an example of the procedure.

setting the mode register

The '626802 contains a mode register that the user should program with the read latency, the burst type, and the burst length. This is accomplished by executing an MRS command with the information entered on address lines A0–A8. A logic 0 should always be entered on A7 and A8, but A9–A11 are don't care entries for the '626802. Figure 2 shows the valid combinations for a successful MRS command. Only valid addresses allow the mode register to be changed. If the addresses are not valid, the previous contents of the mode register remain unaffected. The MRS command is executed by holding $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ low, and the input-mode word valid on A0–A8 on the rising edge of CLK (see Table 1). The MRS command can be executed only when both banks are deactivated.



REGISTER BITS†			READ LATENCY‡
A6	A5	A4	
0	0	1	1
0	1	0	2
0	1	1	3

† All other combinations are reserved.
‡ Refer to timing requirements for minimum valid-read latencies based on maximum frequency rating.

REGISTER BITS§			BURST LENGTH
A2	A1	A0	
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8

§ All other combinations are reserved.

Figure 1. Mode-Register Programming

refresh

The '626802 must be refreshed at intervals not exceeding t_{REF} (see timing requirements), or data cannot be retained. Refresh can be accomplished by performing a read or write access to every row in both banks, by performing 4096 $\overline{CAS}$-before-$\overline{RAS}$ (REFR) commands, or by placing the device in self refresh. Regardless of the method used, refresh must be accomplished before t_{REF} has expired.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

Before performing a $\overline{CAS}$-before-$\overline{RAS}$ refresh, both banks must be deactivated (placed in precharge). To enter a REFR command, $\overline{RAS}$ and $\overline{CAS}$ must be low and $\overline{W}$ must be high upon the rising edge of CLK (see Table 1). The refresh address is generated internally such that after 4096 REFR commands, both banks of the '626802 will have been refreshed. The external address and bank select (A11) are ignored. The execution of a REFR command automatically deactivates both banks upon completion of the internal CBR cycle. This allows consecutive REFR-only commands to be executed, if desired, without any intervening DEAC commands. The REFR commands do not necessarily have to be consecutive, but all 4096 must be completed before t_{REF} expires.

self refresh

To enter self refresh, both banks of the '626802 must first be deactivated and a SLFR command must be executed (see Table 2). The SLFR command is identical to the REFR command except that CKE is low. For proper entry of the SLFR command, CKE is brought low for the same rising edge of CLK that $\overline{RAS}$ and $\overline{CAS}$ are low and $\overline{W}$ is high. CKE must be held low to stay in self-refresh mode. In the self-refresh mode, all refreshing signals are generated internally for both banks with all external signals (except CKE) being ignored. Data can be retained by the device automatically for an indefinite period when power is maintained (consumption is reduced to a minimum). To exit self-refresh mode, CKE must be brought high. New commands are issued after t_{RC} has expired. If CLK is made inactive during self refresh, it must be returned to an active and stable condition before CKE is brought high to exit self refresh (see Figure 21).

Upon exiting self refresh, the normal refresh scheme must begin immediately. If the burst-refresh scheme is used, 4096 REFR commands must be executed before continuing with normal device operations. If a distributed-refresh scheme utilizing CBR is used (e.g., two rows every 32 μs), the first set of refreshes must be performed before continuing with normal device operation. This ensures that the SDRAM is fully refreshed.

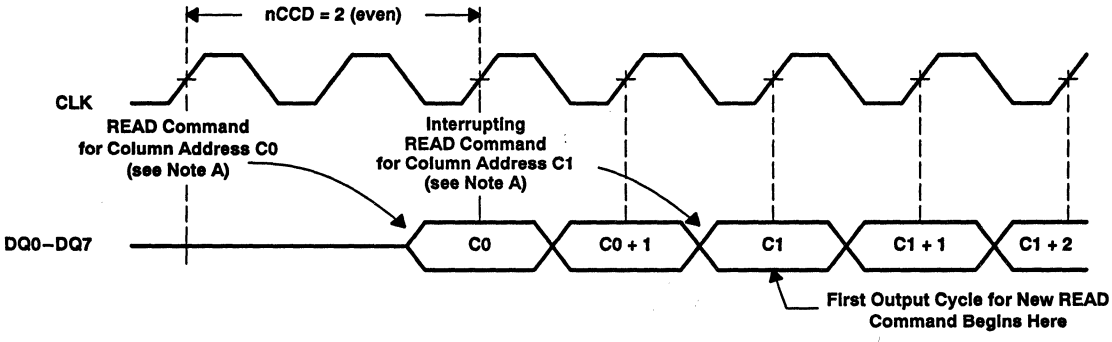
Interrupted bursts

A read or write can be interrupted before the burst sequence has been completed with no adverse effects to the operation. This is accomplished by entering certain superseding commands as listed in Tables 7 and 8, provided that all timing requirements are met. The command interrupting either a read or write burst must be entered only on an even number of cycles (2n rule) from the initial burst command (nCCD). nCCD is defined as the number of clock cycles from the initial command to the interrupting command. In the case when the number of clock cycles between a read/write command and the following command is greater than the burst length the "2n rule" and nCCD does not apply. A DEAC command is considered an interrupt only if it is issued to the same bank as the preceding READ or WRITE command. The interruption of READ-P and WRT-P operations is not supported.

interrupted bursts (continued)

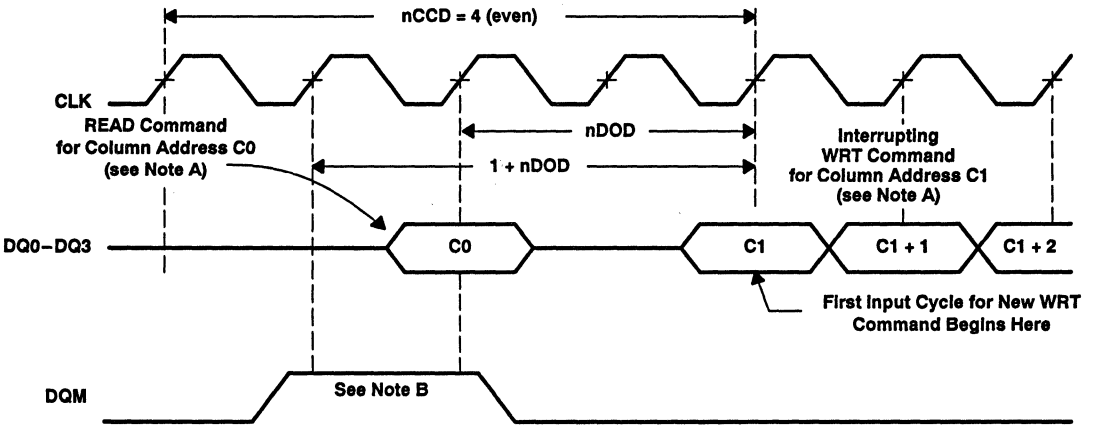
Table 7. Read-Burst Interruption

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING READ BURST
DEAC, DCAB	The DQ bus is in the high-impedance state when nHZP cycles are satisfied or upon completion of the read burst, whichever occurs first (see Figures 5 and 21).
WRT, WRT-P	The WRT command immediately supersedes the read burst in progress, but DQM must be high nDOD+1 and nDOD cycles previous to the WRT (WRT-P) command (see Figure 4).
READ, READ-P	Current output cycles continue until the programmed latency from the superseding READ (READ-P) command is met and new output cycles begin (see Figure 4).
STOP	The DQ bus is in the high-impedance state two clock cycles after the stop command is entered or upon completion of the read burst, whichever occurs first. The bank remains active. A new read or write command cannot be entered for at least two cycles after the STOP command (see Figure 5).



NOTE A: For this example, read latency = 2 and burst length > 2.

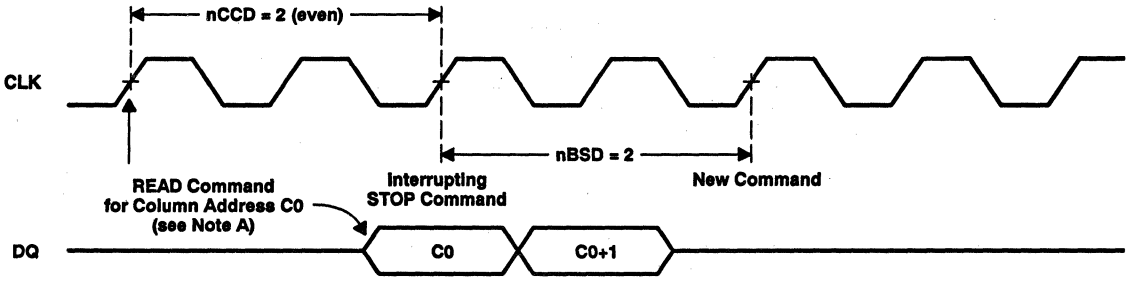
Figure 2. Read Burst Interrupted by Read Command



NOTES: A. For this example, read latency = 2 and burst length > 2.
B. DQM is held high for 2 CLK cycles (2 rising edges). DQM is held high for nDOD+1 to mask out bit prior to interrupting WRT command. DQM is held high for nDOD as specified.

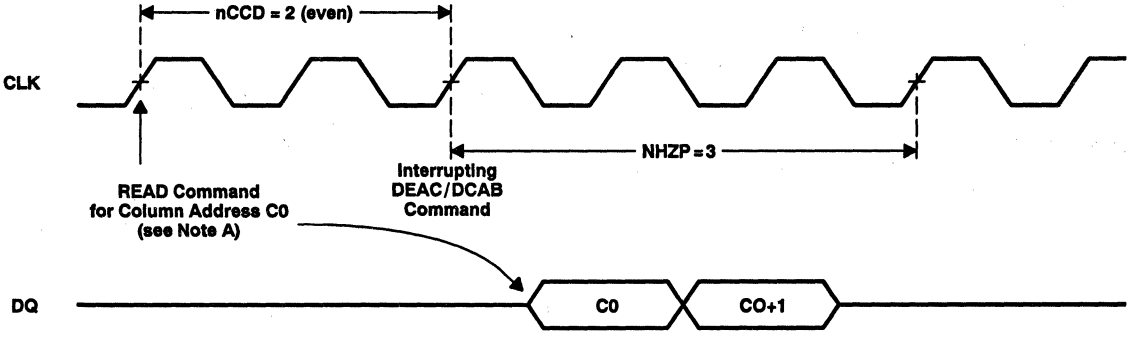
Figure 3. Read Burst Interrupted by Write Command

Interrupted bursts (continued)



NOTE A: For this example, read latency = 2 and burst length > 2.

Figure 4. Read Burst Interrupted by STOP Command



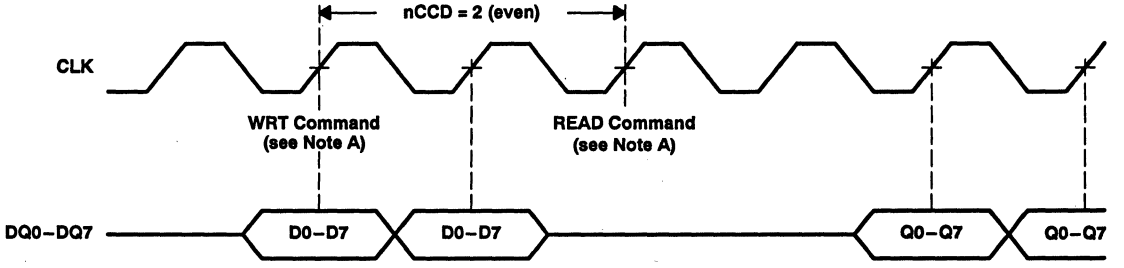
NOTE A: For this example, read latency = 3 and burst length > 2.

Figure 5. Read Burst Interrupted by DEAC Command

Interrupted bursts (continued)

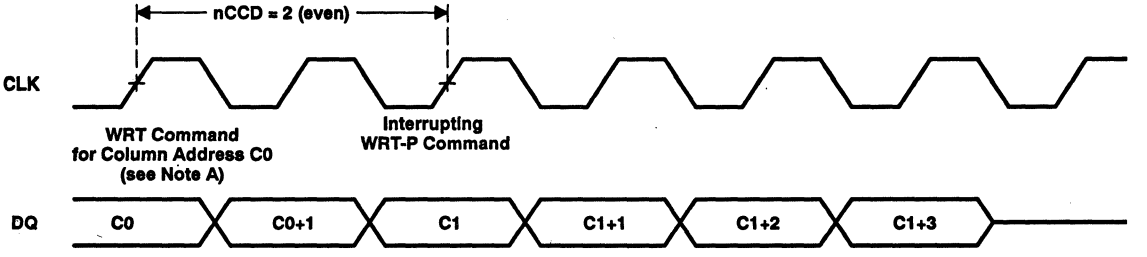
Table 8. Write-Burst Interruption

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING WRITE BURST
DEAC, DCAB	The DEAC/DCAB command immediately supersedes the write burst in progress. DQM must be used to mask the DQ bus such that the write recovery specification (t_{RWL}) is not violated by the interrupt (see Figure 10).
WRT, WRT-P	The new WRT (WRT-P) command and data in immediately supersede the write burst in progress (see Figure 8).
READ, READ-P	Data in on previous cycle is written. No further data in is accepted (see Figure 7).
STOP	The data on the input pins at the time of the burst STOP command is not written, and no further data is accepted. The bank remains active. A new read or write command cannot be entered for at least two cycles after the STOP command (see Figure 9).



NOTE A: For this example, read latency = 2 and burst length > 2.

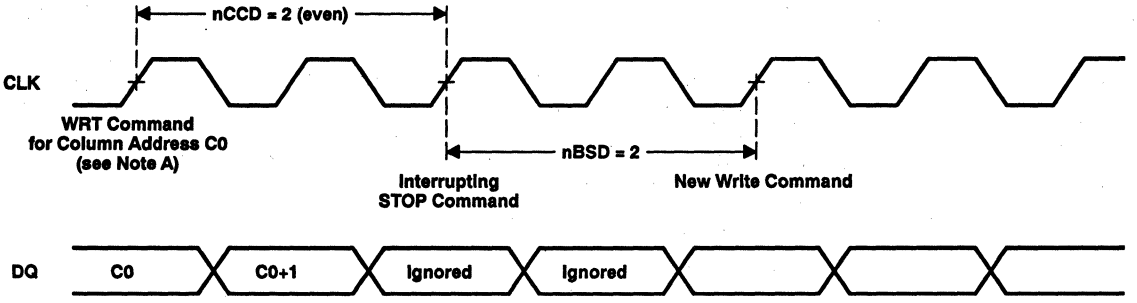
Figure 6. Write Burst Interrupted by Read Command



NOTE A: For this example, burst length > 2.

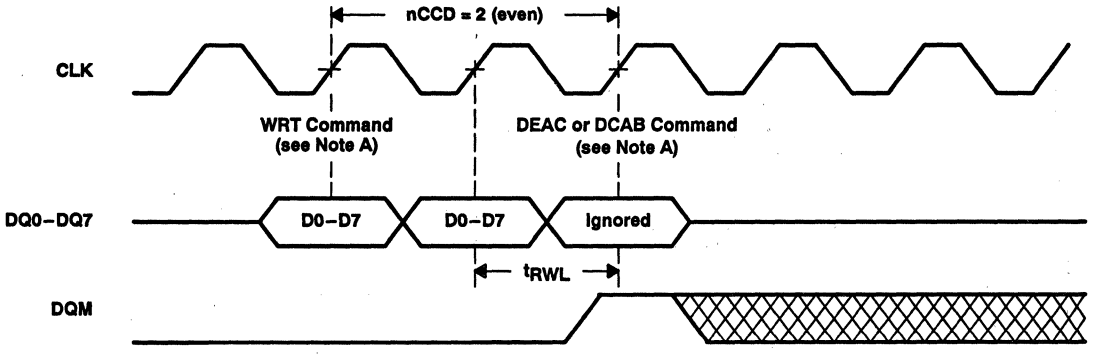
Figure 7. Write Burst Interrupted by Write Command

Interrupted bursts (continued)



NOTE A: For this example, burst length > 2.

Figure 8. Write Burst Interrupted by STOP Command



NOTE A: For this example, read latency = 2, burst length > 2, and $t_{CK} = t_{RWL}$.

Figure 9. Write Burst Interrupted by DEAC/DCAB Command

power up

Device initialization should be performed after a power up to the full V_{CC} level. After power is established, a 200-µs interval is required (with no inputs other than CLK). After this interval, both banks of the device must be deactivated. Eight REFR commands must be performed, and the mode register must be set to complete the device initialization.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 4.6 V
Supply voltage range for output drivers, V_{CCQ} ..... – 0.5 V to 4.6 V
Voltage range on any pin (see Note 1) ..... – 0.5 V to 4.6 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{CCQ}	Supply voltage for output drivers	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{SSQ}	Supply voltage for output drivers		0		V
V_{IH}	High-level input voltage	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS			'626802-10 MIN	'626802-10 MAX	'626802-12 MIN	'626802-12 MAX	'626802-15 MIN	'626802-15 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA			2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA				0.4		0.4		0.4	V
I_I	Input current (leakage)	0 V ≤ V_I ≤ V_{CC} + 0.3 V, All other pins = 0 V to V_{CC}				±10		±10		±10	µA
I_O	Output current (leakage)	0 V ≤ V_O ≤ V_{CC} + 0.3 V, Output disabled				±10		±10		±10	µA
I_{CC1}	Average read or write current	t_{RC} = MIN, t_{CK} = MIN, Read latency = 3	1 bank active	Burst length = 1 or 2		90		80		70	mA
				Burst length = 4 or 8		110		100		90	
			2 banks active interleaving	Burst length = 1 or 2		150		120		100	
				Burst length = 4 or 8		170		140		130	
I_{CC2}	Standby current	Both banks deactivated	CKE = V_{IH}, See Note 3			16		16		16	mA
			CKE = V_{IL}			2		2		2	
			CKE = 0 V (CMOS)			1		1		1	
		One or both banks active	CKE = V_{IL}			6		6		6	
I_{CC3}	Consecutive CBR commands	t_{RC} = MIN				90		80		70	mA
I_{CC4}	Burst current, gapless burst	ACTV not allowed, 2 bank interleaved, t_{CK} = MIN,		Read latency = 1		70		60		50	mA
				Read latency = 2		100		90		80	
				Read latency = 3		140		120		100	
I_{CC6}	Self-refresh current	CKE = V_{IL}				2		2		2	mA
		CKE = 0 V (CMOS)				1		1		1	

NOTES: 2. All specifications apply to the device after power-up initialization.
3. All control and address inputs must be stable and valid.

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 4)

		MIN	MAX	UNT
$C_{i(S)}$	Input capacitance, CLK		7	pF
$C_{I(AC)}$	Input capacitance, A0–A11, $\overline{CS}$, DQM, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		5	pF
$C_{i(E)}$	Input capacitance, CKE		5	pF
C_o	Output capacitance		8	pF

NOTE 4: V_{CC} = 3.3 ± 0.3 V and bias on pins under test is 0 V.

ac timing requirements over recommended ranges of supply voltage and operating free-air temperature†‡

			'626802-10		'626802-12		'626802-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CK}	Cycle time, CLK (system clock)	Read latency = 1	30		36		40		ns
		Read latency = 2	15		18		20		
		Read latency = 3	10		12		15		
t_{CKH}	Pulse duration, CLK (system clock) high		3		3.5		4		ns
t_{CKL}	Pulse duration, CLK (system clock) low		3		3.5		4		ns
t_{AC}	Access time, CLK ↑ to data out (see Note 5)	Read latency = 1		29		33		38	ns
		Read latency = 2		14		15		18	
		Read latency = 3		9		10		12	
t_{LZ}	Delay time, CLK to DQ in the low-impedance state (see Note 6)		0		0		0		ns
t_{HZ}	Delay time, CLK to DQ in the high-impedance state (see Note 7)	Read latency = 1		20		20		20	ns
		Read latency = 2		12		13		14	
		Read latency = 3		9		10		11	
t_{DS}	Setup time, data input		2		2		2		ns
t_{AS}	Setup time, address		2		2		2		ns
t_{CS}	Setup time, control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQM)		2		2		2		ns
t_{CES}	Setup time, CKE (suspend entry/exit, power-down entry)		2		2		2		ns
t_{CESP}	Setup time, CKE (power down/self-refresh exit) (see Note 8)		8		10		12		ns
t_{OH}	Hold time, CLK ↑ to data out		3		3		3		ns
t_{DH}	Hold time, data input		2		3		4		ns
t_{AH}	Hold time, A0–A10		2		3		4		ns
t_{CH}	Hold time, control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQM)		2		3		4		ns
t_{CEH}	Hold time, CKE		2		3		4		ns
t_{RC}	REFR command to ACTV, MRS, REFR or SLFR command; ACTV command to ACTV, MRS, REFR or SLFR command; Self-refresh exit to ACTV, MRS, REFR or SLFR command		100		110		125		ns

† See Parameter Measurement Information for load circuits.

‡ All references are made to the rising transition of CLK, unless otherwise noted.

NOTES: 5. t_{AC} is referenced from the rising transition of CLK that is previous to the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CLK that is read latency – 1 cycles after the READ command. An access time is measured at output reference level 1.4 V.

6. t_{LZ} is measured from the rising transition of CLK that is read latency – 1 cycles after the READ command.

7. t_{HZ} (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.

8. If $t_{CESP} > t_{CK}$, NOOP or DESL commands must be entered until t_{CESP} is met. CLK must be active and stable (if CLK was turned off for power down) before CKE is returned high.

ac timing requirements over recommended ranges of supply voltage and operating free-air temperature†‡

			'626802-10		'626802-12		'626802-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{RAS}	ACTV command to DEAC or DCAB command		60	100 000	70	100 000	80	100 000	ns
t_{RCD}	ACTV command to READ or WRT command		30		35		40		ns
t_{RP}	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR command		40		40		45		ns
t_{APR}	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command		t_{RP} + (nEP × t_{CK})						ns
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command (see Note 10)	Burst length = 1	1 clock+60		1 clock+60		1 clock+75		ns
		Burst length > 1	60		60		75		
t_{RWL}	Final data in to DEAC or DCAB command (see Note 11)	Burst length = 1	1 clock+20		1 clock+20		1 clock+30		ns
		Burst length > 1	20		20		30		
t_{RRD}	ACTV command for one bank to ACTV command for the other bank		20		25		30		ns
t_T	Transition time, all inputs (see Note 9)		1	5	1	5	1	5	ns
t_{REF}	Refresh interval			64		64		64	ms

† See Parameter Measurement Information for load circuits.
‡ All references are made to the rising transition of CLK, unless otherwise noted.

NOTES: 9. Transition time, t_T, is measured between V_{IH} and V_{IL}.
10. for BL=1only
SPEED
–10, –12 = t_{APW} is 60 ns from first unsuspended clock edge after last data in
–15 = t_{APW} is 80 ns from first unsuspended clock edge after last data in
11. for BL = 1 only
SPEED
–10, –12 = t_{RWL} is 20 ns from first unsuspended clock edge after last data in
–15 = t_{RWL} is 30 ns from first unsuspended clock edge after last data in

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature†

			'626802-10		'626802-12		'626802-15		UNIT‡
			MIN	MAX	MIN	MAX	MIN	MAX	
nEP	Final data out to DEAC or DCAB command	Burst length = 1, Read latency = 1	1		1		1		cycles
		Burst length = 1, Read latency = 2	0		0		0		
		Burst length = 1, Read latency = 3	−1		−1		−1		
		Burst length > 1, Read latency = 1	0		0		0		cycles
		Burst length > 1, Read latency = 2	−1		−1		−1		
		Burst length > 1, Read latency = 3	−2		−2		−2		
nHZP	DEAC or DCAB interrupt of data-out burst to DQ in the high-impedance state (see Note 10)	Read latency = 1	1		1		1		cycles
		Read latency = 2	2		2		2		
		Read latency = 3	3		3		3		
nCCD	READ or WRT command to interrupting STOP, READ, WRT, DEAC, or DCAB command (i = 1, 2, 3, . . .) (see Note 11)		2i		2i		2i		cycles
nCWL	Final data in to READ or WRT command in either bank	Burst length = 1	2		2		2		cycles
		Burst length > 1	1		1		1		cycles
nWCD	WRT command to first data in		0	0	0	0	0	0	cycles
nDID	ENBL or MASK command to data in		0	0	0	0	0	0	cycles
nDOD	ENBL or MASK command to data out		2	2	2	2	2	2	cycles
nCLE	HOLD command to suspended CLK edge; HOLD operation exit to entry of any command		1	1	1	1	1	1	cycles
nRSA	MRS command to ACTV, REFR, SLFR, or MRS command		2		2		2		cycles
nCDD	DESL command to control input inhibit		0	0	0	0	0	0	cycles
nBSD	STOP command to READ or WRT command		2		2		2		cycles

† All references are made to the rising transition of CLK, unless otherwise noted.

‡ A CLK cycle can be considered as contributing to a timing requirement for those parameters defined in cycle units only when not gated by CKE (those CLK cycles occurring during the time when CKE is asserted low).

NOTES: 12. A data-out burst can be interrupted only on an even number of clock cycles after the initial READ command is entered (refer to nCCD).

13. A read or write burst can be interrupted only at an even number of clock cycles after entry of the initial READ or WRT command. The nCCD parameter is only required in the case of a burst interruption.

Table 9. Number of Cycles Required to Meet Minimum Specification for Key Timing Parameters

			TMS626802-10					TMS626802-12				TMS626802-15			UNITS
	Operating frequency		100	80	66	50	33	80	66	50	33	66	50	33	MHz
t_{CK}	Cycle time, CLK (system clock)		10	12	15	20	30	12	15	20	30	15	20	30	ns
	KEY PARAMETER		NUMBER OF CYCLES REQUIRED												
	Read latency, minimum programmed value		3	3	2	2	1	3	3	2	2	3	2	2	cycles
t_{RCD}	ACTV command to READ or WRT command		3	3	2	2	1	3	3	2	2	3	2	2	cycles
t_{RAS}	ACTV command to DEAC or DCAB command		6	5	4	3	2	6	5	4	3	6	4	3	cycles
t_{RP}	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR command		4	4	3	2	2	4	3	2	2	3	3	2	cycles
t_{RC}	REFR command to ACTV, MRS, or REFR command; self-refresh exit to ACTV, MRS, SLFR, or REFR command		10	9	7	5	4	10	8	6	4	9	7	5	cycles
t_{RWL}	Final data in to DEAC or DCAB command	Burst length = 1	3	3	3	2	2	3	3	2	2	3	3	2	cycles
		Burst length > 1	2	2	2	1	1	2	2	1	1	2	2	1	cycles
t_{RRD}	ACTV command for one bank to ACTV command for the other bank		2	2	2	1	1	3	2	2	1	2	2	1	cycles
t_{APR}	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command	Burst length = 1, Read latency = 1	—	—	—	—	3	—	—	—	—	—	—	—	cycles
		Burst length = 1, Read latency = 2	—	—	3	2	2	—	—	2	2	—	3	2	cycles
		Burst length = 1, Read latency = 3	3	3	2	1	1	3	2	1	1	3	2	1	cycles
		Burst length > 1, Read latency = 1	—	—	—	—	2	—	—	—	—	—	—	—	cycles
		Burst length > 1, Read latency = 2	—	—	2	1	1	—	—	1	1	—	2	1	cycles
		Burst length > 1, Read latency = 3	2	2	1	0	0	2	1	0	0	2	1	0	cycles
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command	Burst length = 1	7	6	5	4	3	6	5	4	3	6	5	4	cycles
		Burst length > 1	6	5	4	3	2	5	4	3	2	5	4	3	cycles

TEXAS INSTRUMENTS
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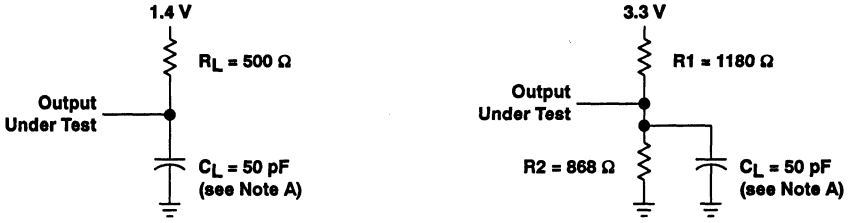
PARAMETER MEASUREMENT INFORMATION

general information for ac timing measurements

The ac timing measurements are based on signal rise and fall times equal to 1 ns (t_T = 1 ns) and a midpoint reference level of 1.4 V for LVTTL. For signal rise and fall times greater than 1 ns, the reference level should be changed to V_{IH} min and V_{IL} max instead of the midpoint level. All specifications referring to READ commands are also valid for READ-P commands unless otherwise noted. All specifications referring to WRT commands are also valid for WRT-P commands unless otherwise noted. All specifications referring to consecutive commands are specified as consecutive commands for the same bank unless otherwise noted.

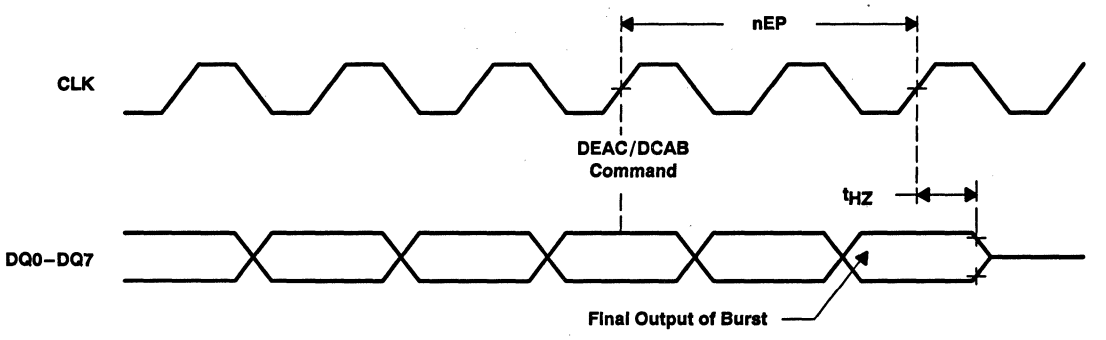


(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.

Figure 10. Load Circuits



NOTE A: For this example, assume read latency = 3 and burst length > 1.

Figure 11. nEP, Final Data Output to DEAC or DCAB Command

PARAMETER MEASUREMENT INFORMATION

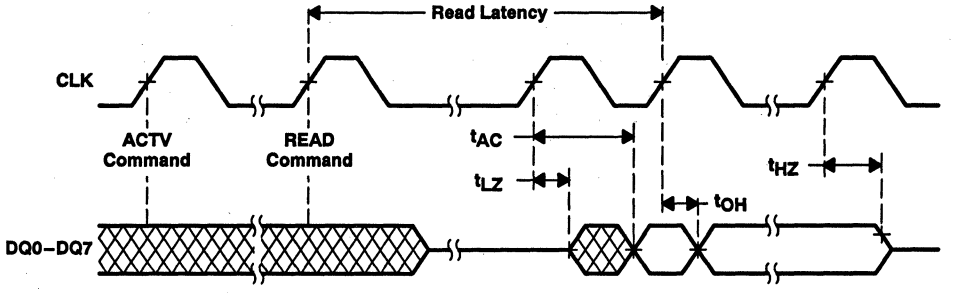
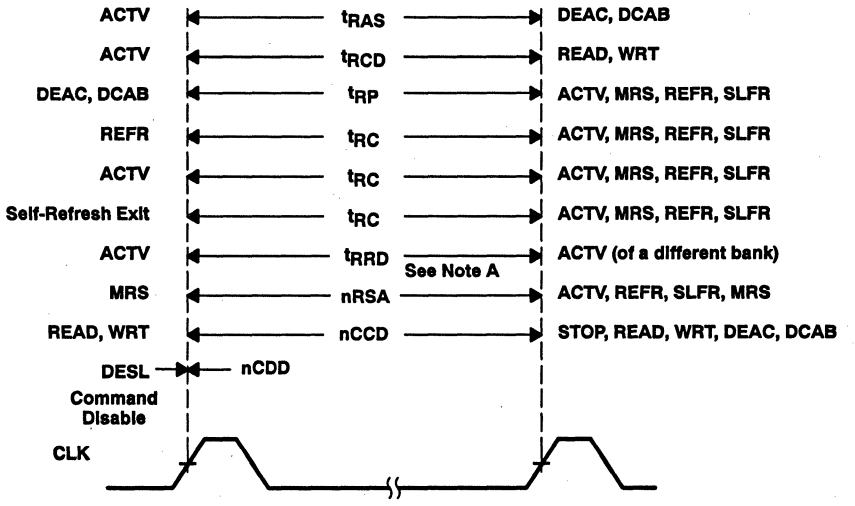


Figure 12. Output Parameters



NOTE A: t_{RRD} is specified for command execution in one bank to command execution in the other bank.

Figure 13. Command-to-Command Parameters

PARAMETER MEASUREMENT INFORMATION

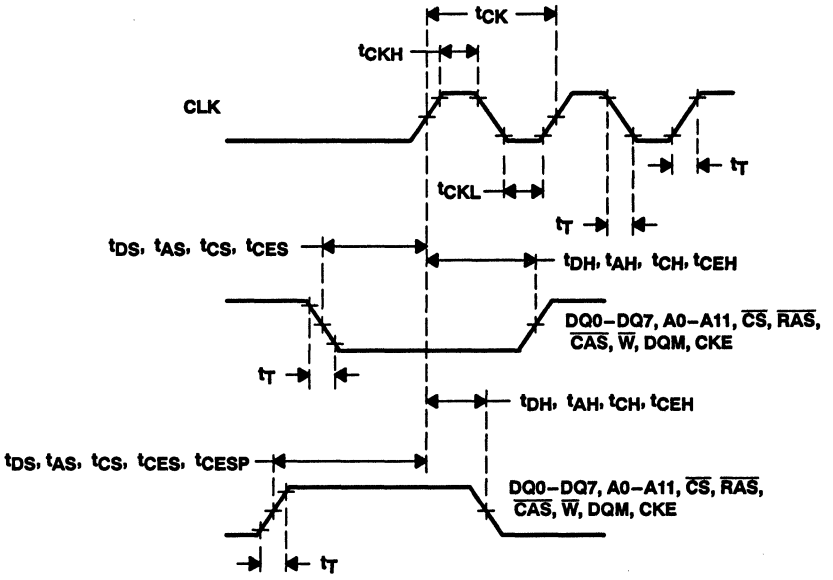
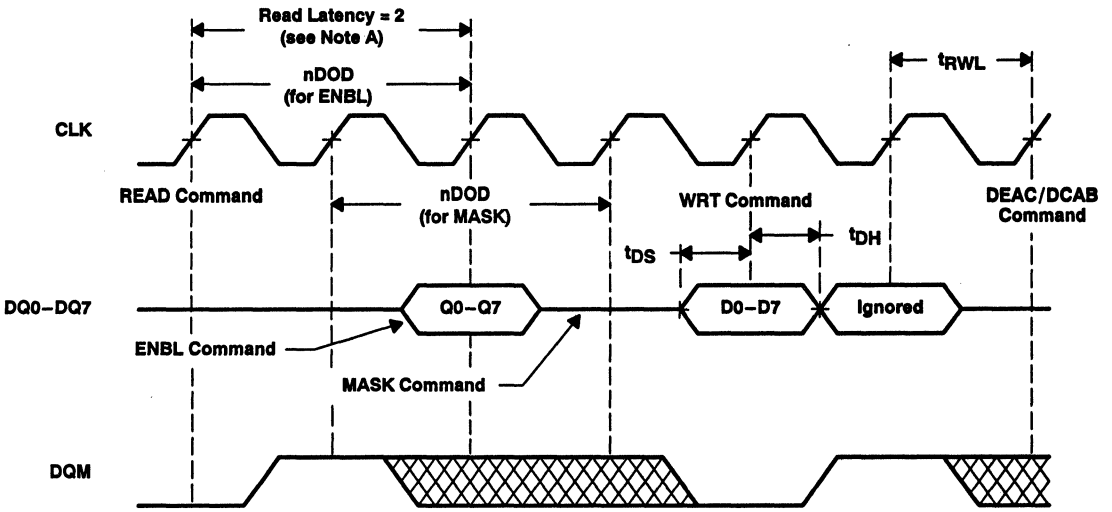


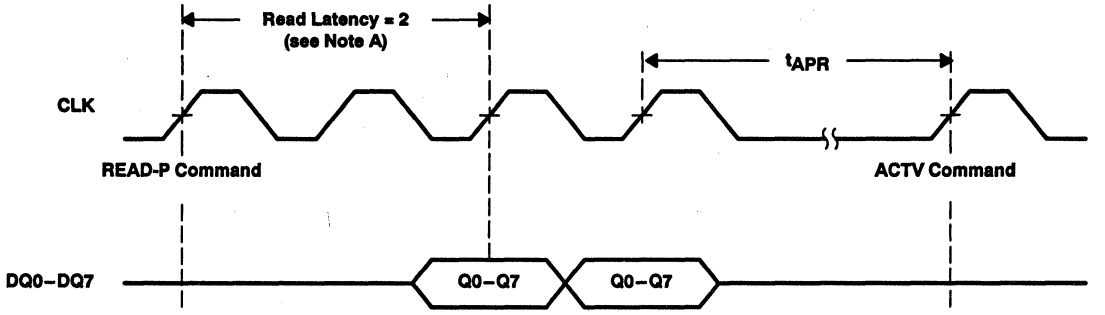
Figure 14. Input-Attribute Parameters



NOTE A: For this example, assume read latency = 2 and burst length = 2.

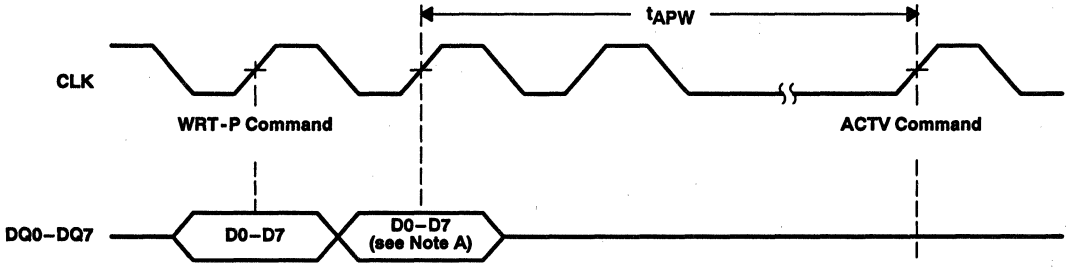
Figure 15. DQ Masking

PARAMETER MEASUREMENT INFORMATION



NOTE A: For this example, assume read latency = 2 and burst length = 2.

Figure 16. Read-Automatic Deactivate (Autoprecharge)



NOTE A: For this example, the burst length = 2.

Figure 17. Write-Automatic Deactivate (Autoprecharge)

PARAMETER MEASUREMENT INFORMATION

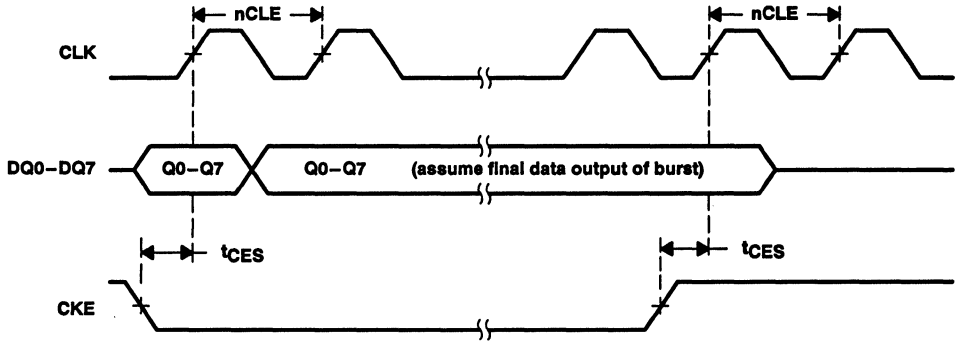


Figure 18. CLK-Suspend Operation

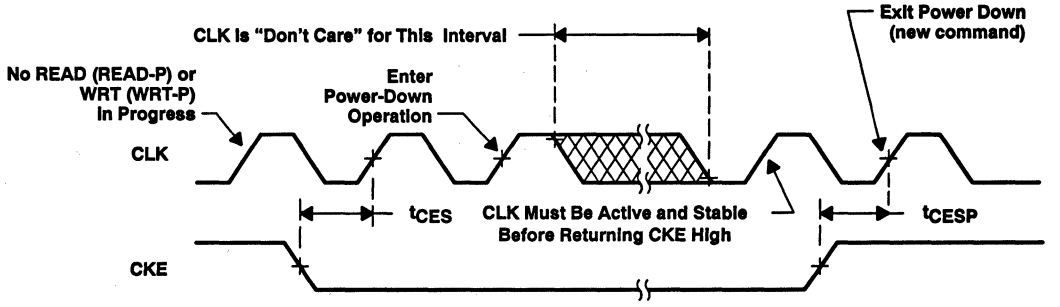
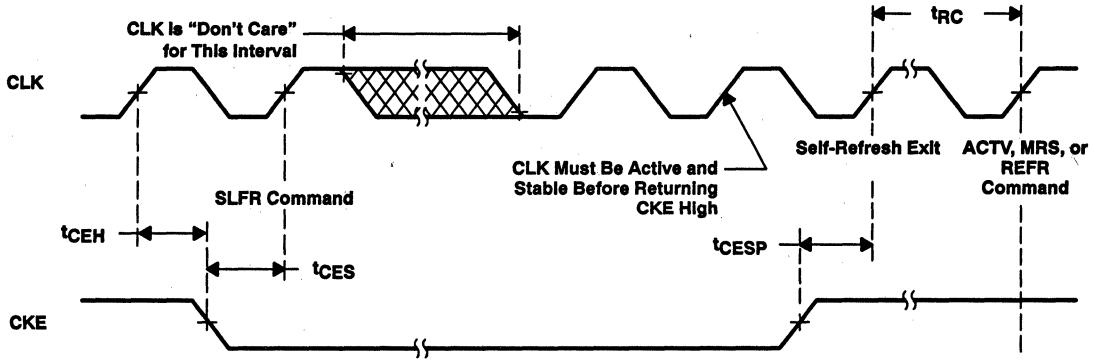


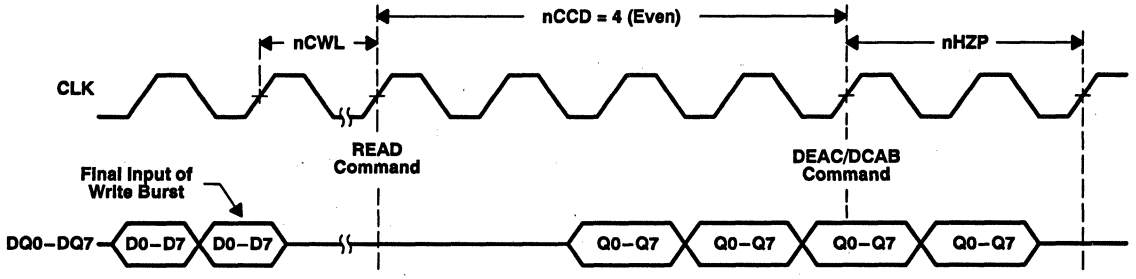
Figure 19. Power-Down Operation

PARAMETER MEASUREMENT INFORMATION



NOTE A: Assume both banks are previously deactivated.

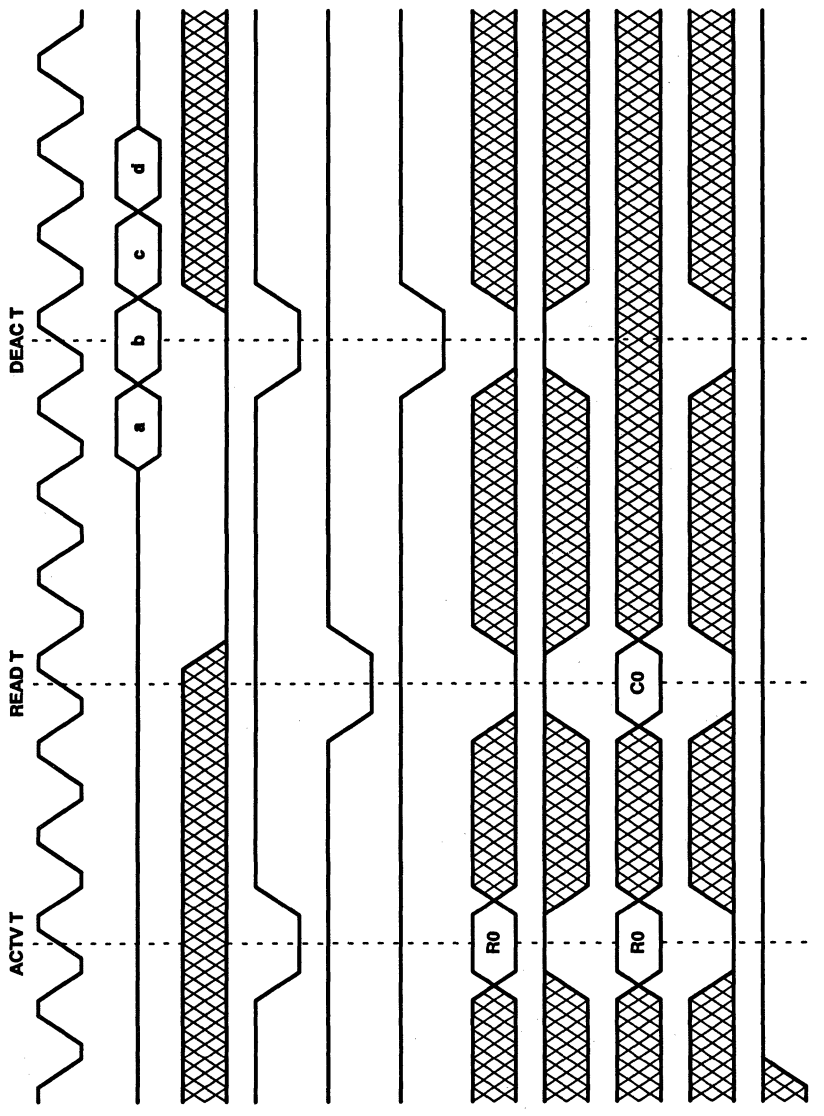
Figure 20. Self-Refresh Entry/Exit



NOTE A: Assume read latency = 2 and burst length = 8.

Figure 21. Write Burst Followed by DEAC/DCAB-Interrupted Read

PARAMETER MEASUREMENT INFORMATION



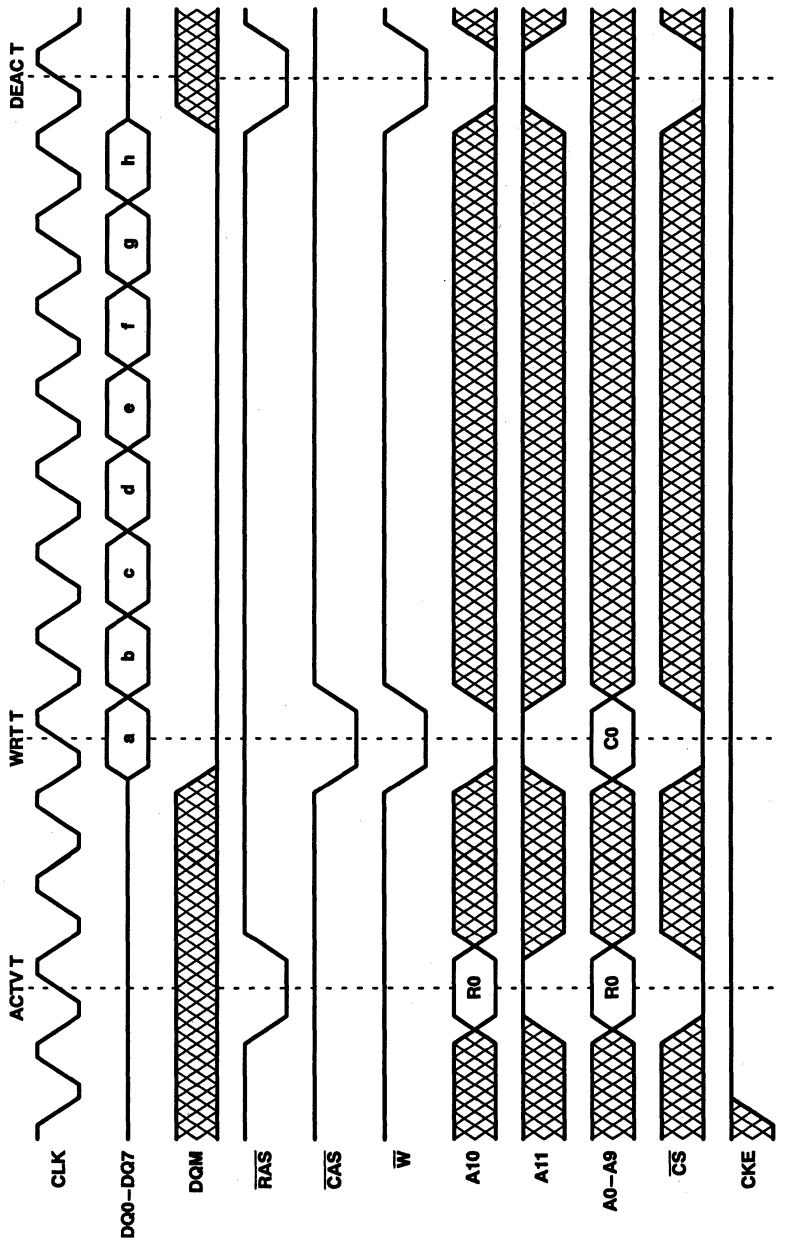
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d
Q	T	R0	C0†	C0 + 1	C0 + 2	C0 + 3

† Column-address sequence depends on programmed burst type and C0 (see Table 5).

NOTE A: This example illustrates minimum t_{RCD} and nEP for the '626802-10 at 100 MHz, the '626802-12 at 80 MHz, and the '626802-15 at 66 MHz.

Figure 22. Read Burst (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

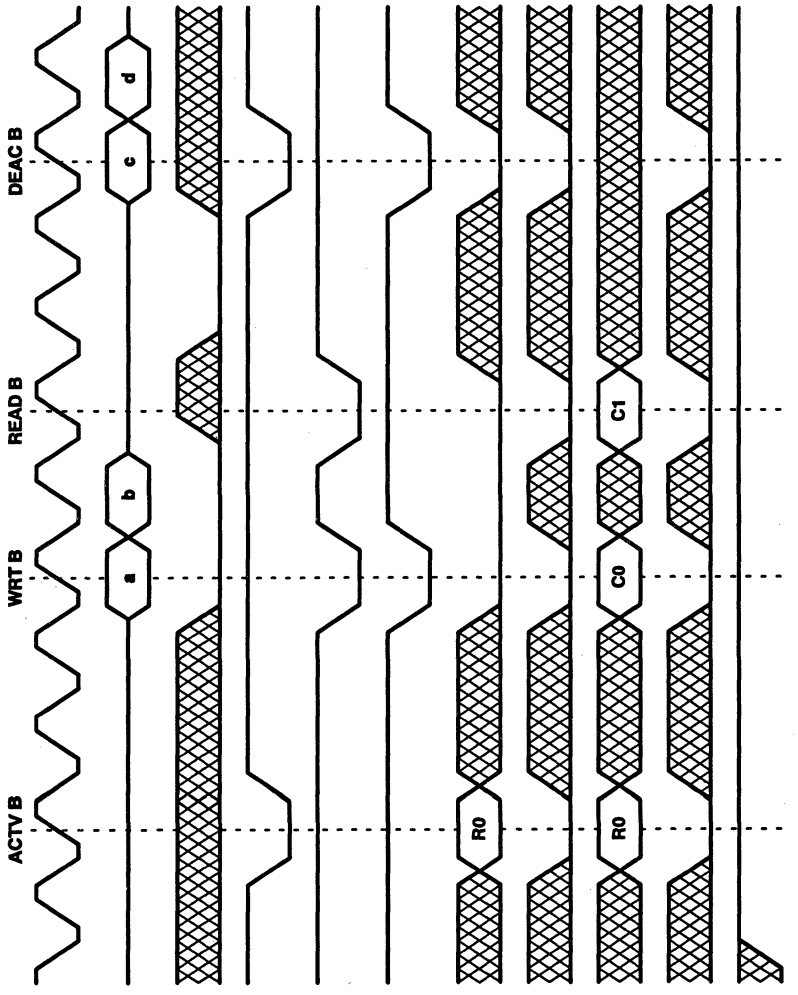


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
D	T	R0	C0†	C0 + 1	C0 + 2	C0 + 3	C0 + 4	C0 + 5	C0 + 6	C0 + 7

† Column-address sequence depends on programmed burst type and C0 (see Table 5).
NOTE A: This example illustrates minimum t_{RWL} for the '626802-10 at 100 MHz, the '626802-12 at 80 MHz, and the '626802-15 at 66 MHz.

Figure 23. Write Burst (burst length = 8)

PARAMETER MEASUREMENT INFORMATION

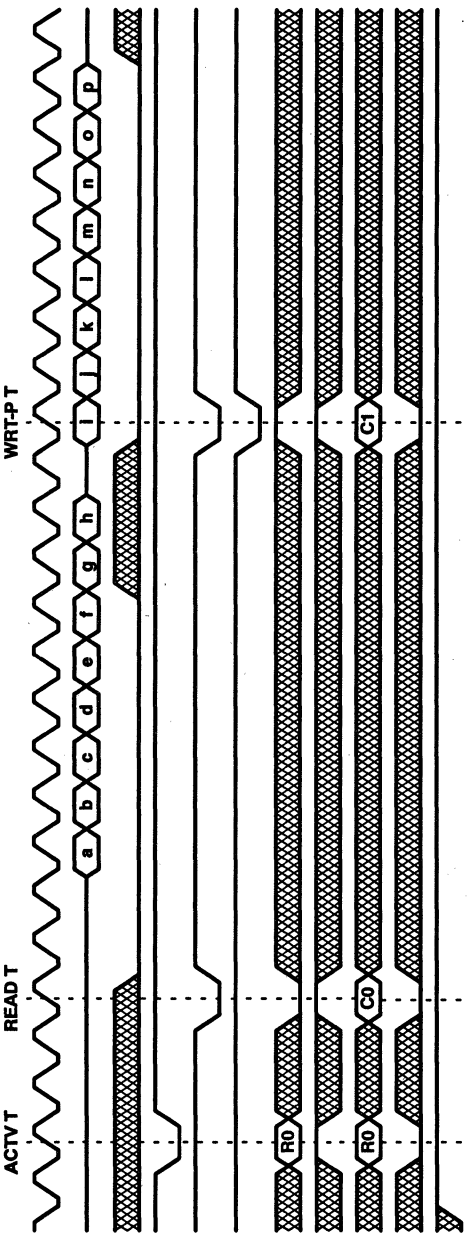


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d
D	B	R0	C0†	C0 + 1		
Q	B	R0			C1‡	C1 + 1

† Column-address sequence depends on programmed burst type and C0 (see Table 4).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 4).
NOTE A: This example illustrates minimum t_{RCD} for the '626802-10 at 100 MHz, the '626802-12 at 80 MHz, and the '626802-15 at 66 MHz.

Figure 24. Write-Read Burst (read latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION



BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p
Q	T	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7								
D	T	R0									C1‡	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7

† Column-address sequence depends on programmed burst type and C0 (see Table 6).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 6).
NOTE A: This example illustrates minimum t_{RCD} for the '626802-10 at 100 MHz, the '626802-12 at 80 MHz, and the '626802-15 at 66 MHz.

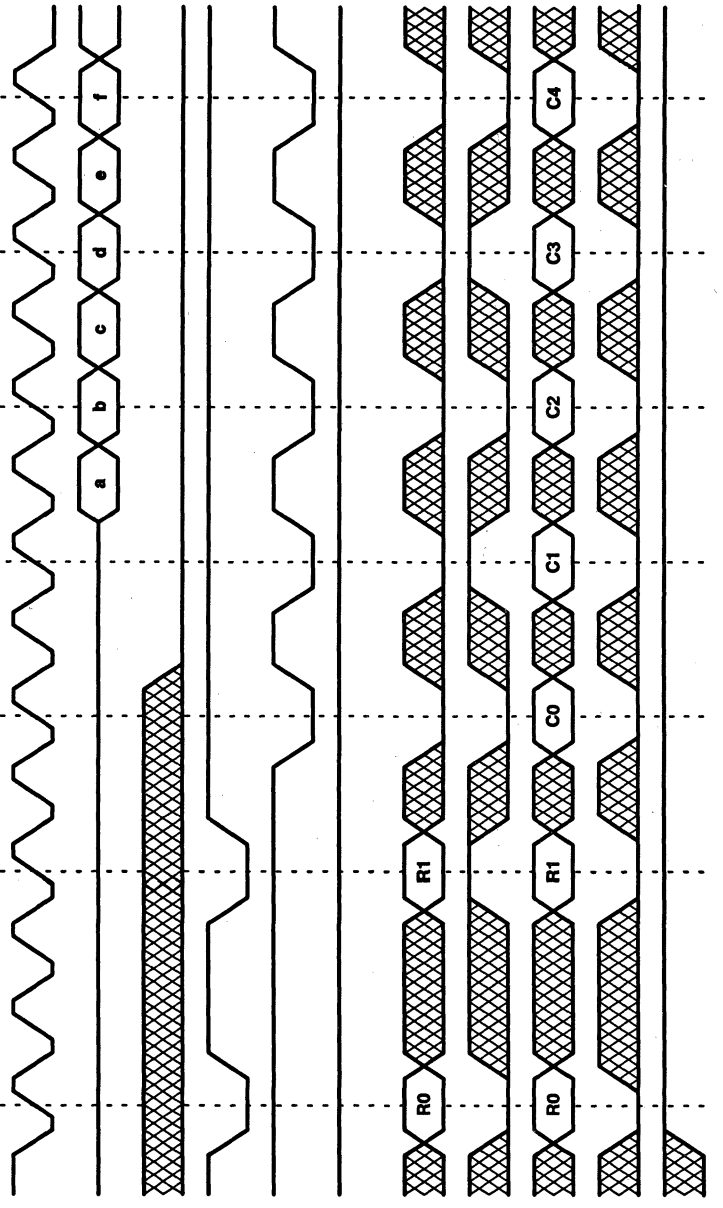
Figure 25. Read-Write Burst With Automatic Deactivate (read latency = 3, burst length = 8)

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	.	.
Q	B	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7													
Q	T	R1									C1‡	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7					
Q	B	R2																	C2§	C2+1	C2+2	.	.

† Column-address sequence depends on programmed burst type and C0 (see Table 6).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 6).
§ Column-address sequence depends on programmed burst type and C2 (see Table 6).
NOTE A: This example illustrates minimum t_{RCD} for the '626802-10 at 100 MHz, the '626802-12 at 80 MHz, and the '626802-15 at 66 MHz.

Figure 26. Two-Bank Row-Interleaving Read Bursts With Automatic Deactivate (read latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION

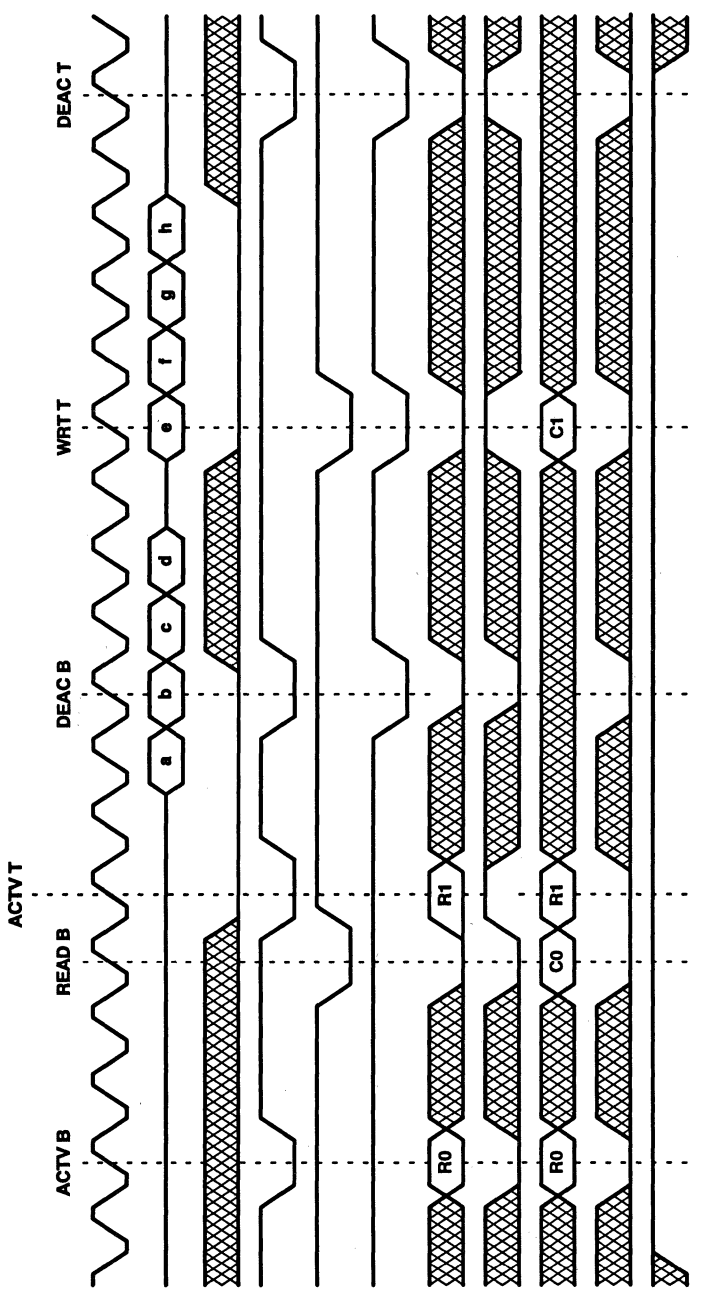


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	...
Q	B	R0	C0†	C0 + 1					...
Q	T	R1			C1‡	C1 + 1			...
Q	B	R0					C2§	C2 + 1	...
.	...	...							...

† Column-address sequence depends on programmed burst type and C0 (see Table 4).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 4).
§ Column-address sequence depends on programmed burst type and C2 (see Table 4).

Figure 27. Two-Bank Column-Interleaving Read Bursts (read latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION

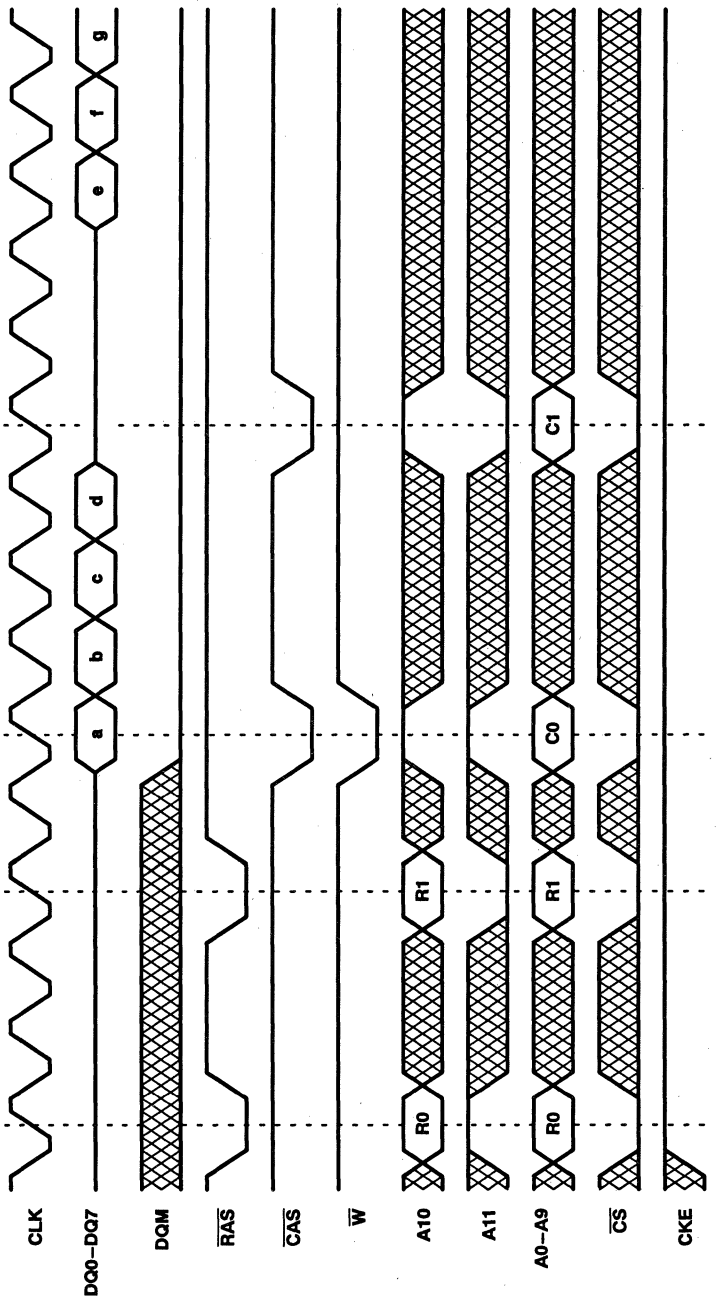


BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h
Q	B	R0	C0†	C0 + 1	C0 + 2	C0 + 3	C1‡	C1 + 1	C1 + 2	C1 + 3
D	T	R1								

† Column-address sequence depends on programmed burst type and C0. (see Table 5).
‡ Column-address sequence depends on programmed burst type and C1. (see Table 5).
NOTE A: This example illustrates a minimum t_{RCD} and nEP read burst, and a minimum t_{RWL} write burst for the '626802-10 at 100 MHz, the '626802-12 at 80 MHz, and the '626802-15 at 66 MHz.

Figure 28. Read-Burst Bank B, Write-Burst Bank T (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

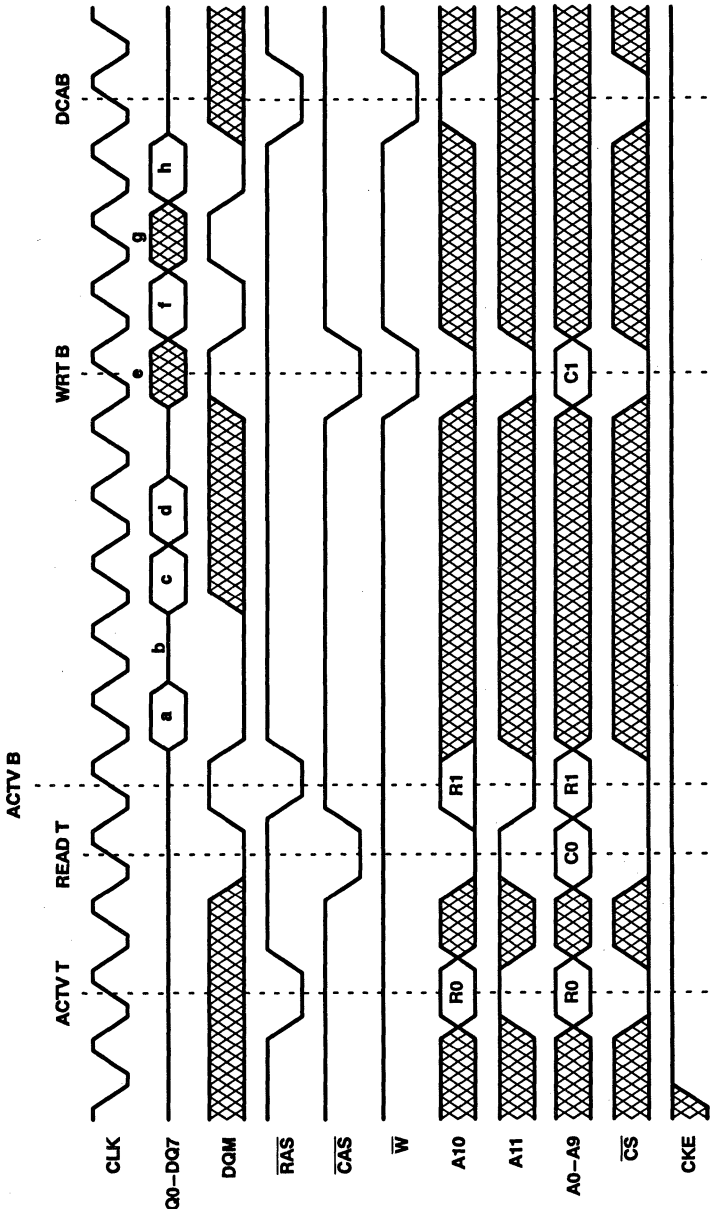


BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h
D	T	R0	C0†	C0 + 1	C0 + 2	C0 + 3				
Q	B	R1					C1‡	C1 + 1	C1 + 2	C1 + 3

† Column-address sequence depends on programmed burst type and C0 (see Table 5).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 5).
NOTE A: This example illustrates minimum nCWL for the '626802-10 at 100 MHz, the '626802-12 at 80 MHz, and the '626802-15 at 66 MHz.

Figure 29. Write-Burst Bank T, Read-Burst Bank B With Automatic Deactivate (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

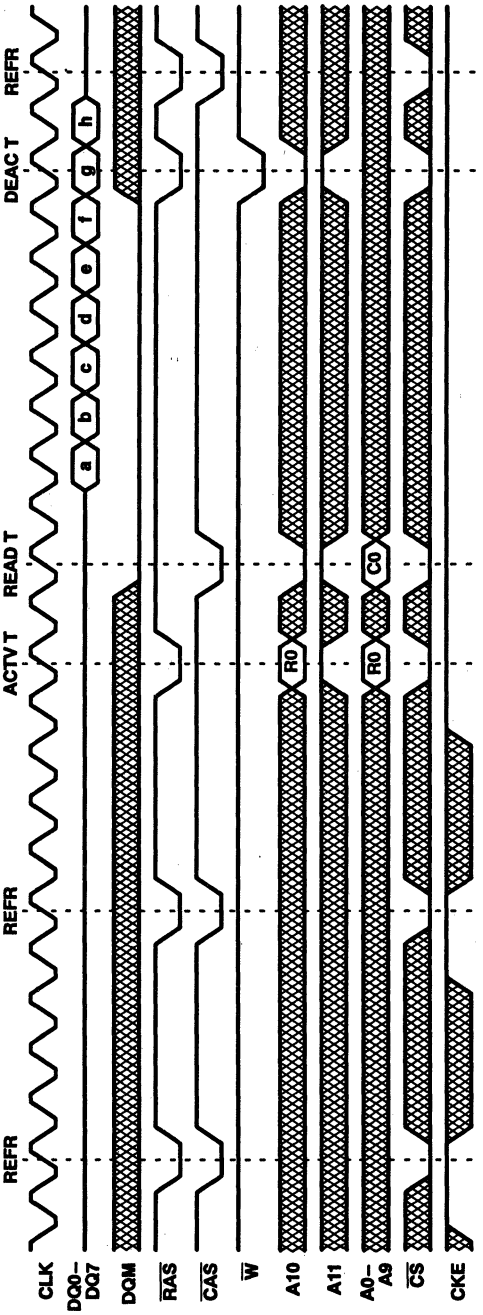


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	T	R0	C0†	C0+1	C0+2	C0+3				
D	B	R1					C1‡	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and C0 (see Table 5).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 5).
NOTE A: This example illustrates a minimum t_{RCD} read burst and minimum t_{RWL} write burst for the '626802-10 at 100 MHz, the '626802-12 at 80 MHz, and the '626802-15 at 66 MHz.

Figure 30. Use of DQM for Output and Data-In Cycle Masking (read-burst bank T, write-burst bank B, deactivate all banks) (read latency = 2, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



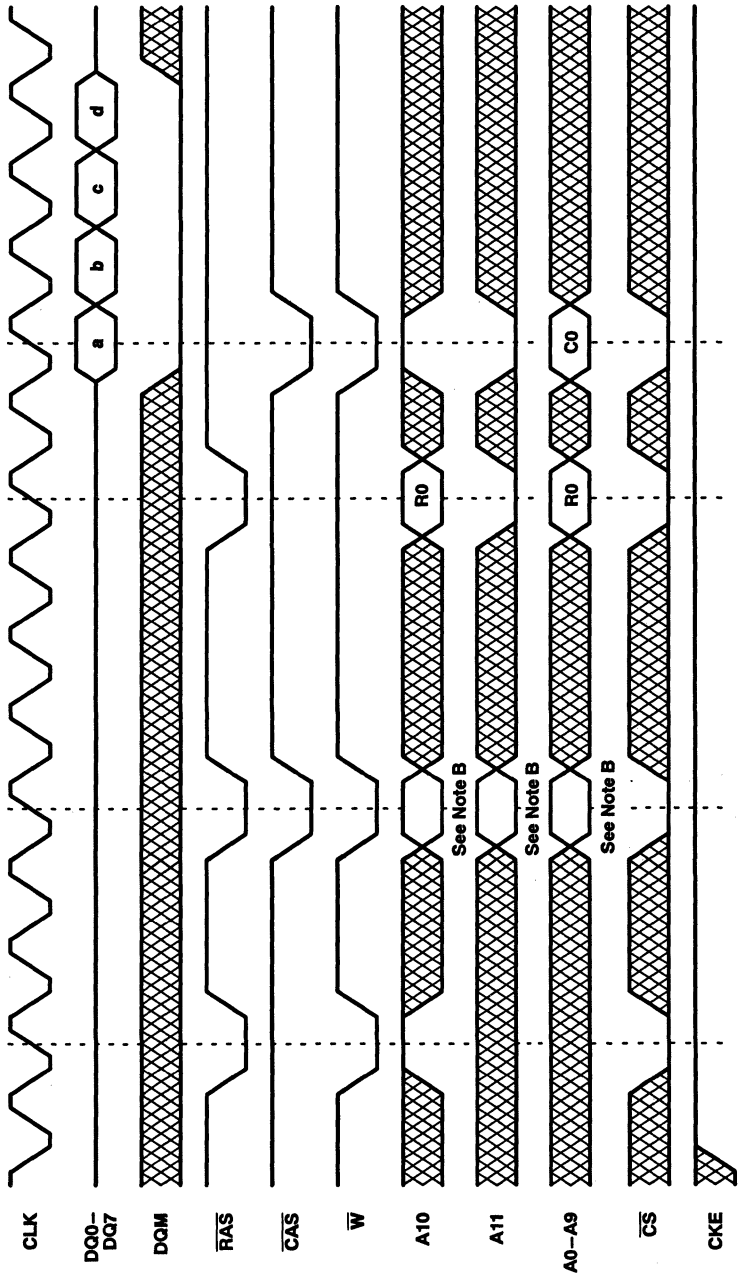
BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h
Q	T	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7

† Column-address sequence depends on programmed burst type and C0 (see Table 6).

NOTE A: This example illustrates minimum t_{RC}, t_{RCD}, nEP, and t_{RP} for the '626802-10 at 100 MHz, the '626802-12 at 80 MHz, and the '626802-15 at 66 MHz.

Figure 31. Refresh Cycles (refreshes followed by read burst followed by refresh) (read latency = 2, burst length = 8)

PARAMETER MEASUREMENT INFORMATION



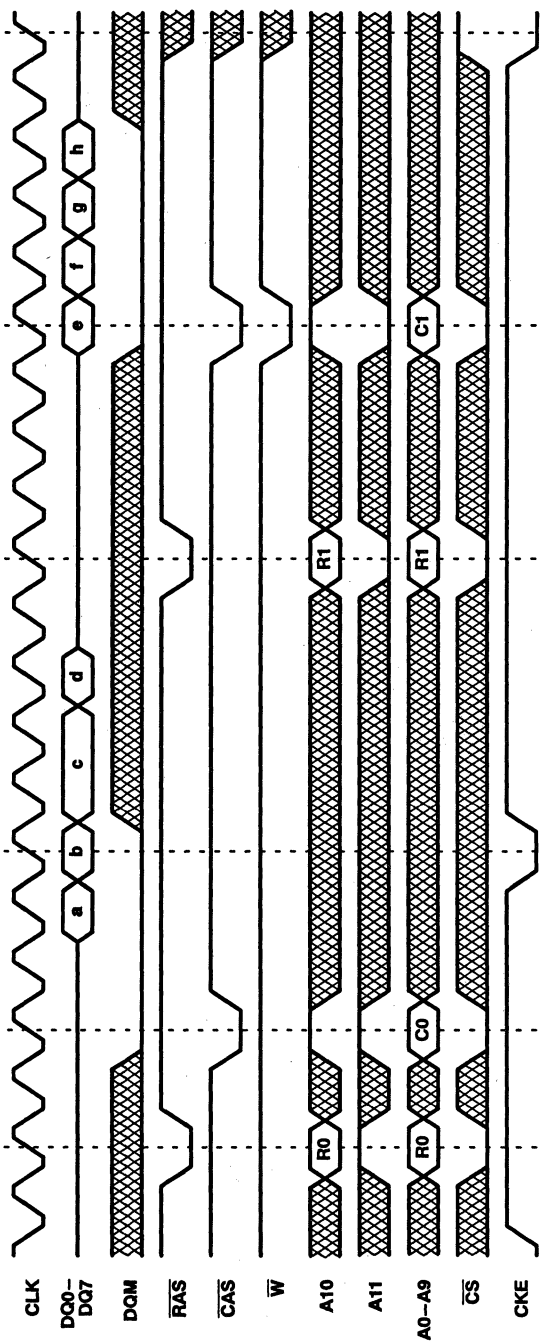
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d
D	B	R0	C0†	C0+1	C0+2	C0+3

† Column-address sequence depends on programmed burst type and C0 (see Table 5).

NOTES: A. This example illustrates minimum t_{RCD} for the '626802-10 at 100 MHz, the '626802-12 at 80 MHz, and the '626802-15 at 66 MHz.
B. Refer to Figure 1

Figure 32. Mode Register Programming (deactivate all, mode program, write burst with automatic deactivate) (read latency = 2, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	T	R0	C0†	C0+1	C0+2	C0+3				
D	B	R1					C1‡	C1+1	C1+2	C1+3

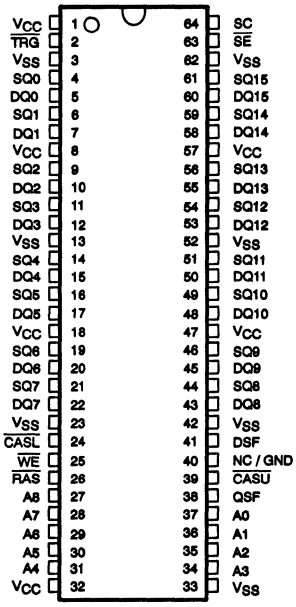
† Column-address sequence depends on programmed burst type and C0 (see Table 5).
‡ Column-address sequence depends on programmed burst type and C1 (see Table 5).
NOTE A: This example illustrates minimum t_{RCD} for the '626802-10 at 100 MHz, the '626802-12 at 80 MHz, and the '626802-15 at 66 MHz.

Figure 33. Use of CKE for Clock Gating (hold) and Standby Mode (read-burst bank T with hold, write-burst bank B, standby mode) (read latency = 2, burst length = 4)

This data sheet is applicable to all TMS55160s symbolized with Revision "C" and subsequent revisions as described on page 5-134.

- **Organization:**
  - **DRAM: 262144 Words × 16 Bits**
  - **SAM: 256 Words × 16 Bits**
- **Dual-Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Data Transfer Function From the DRAM to the Serial Data Register**
- **(4 × 4) × 4 Block-Write Feature for Fast Area Fill Operations; As Many as Four Memory Address Locations Written Per Cycle From the 16-Bit On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O; Two Write-Per-Bit Modes to Simplify System Design**
- **Byte Write Control ($\overline{CASL}$, $\overline{CASU}$) Provides Flexibility**
- **Enhanced Page-Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) and Hidden Refresh Modes**
- **Long Refresh Period**
  Every 8 ms (Max)
- **Up to 55-MHz Uninterrupted Serial Data Streams**
- **256 Selectable Serial-Register Starting Locations**
- **$\overline{SE}$-Controlled Register-Status QSF**
- **Split-Register-Transfer Read for Simplified Real-Time Register Load**
- **Programmable Split-Register Stop Point**
- **3-State Serial Outputs Allow Easy Multiplexing of Video Data Streams**
- **All Inputs/Outputs and Clocks TTL Compatible**
- **Compatible With JEDEC Standards**
- **Texas Instruments EPIC™ CMOS Process**
- **Designed to Work With the Industry-Leading Texas Instruments Graphics Family**
- **Performance Ranges:**

DGH PACKAGE
(TOP VIEW)



PIN NOMENCLATURE

A0–A8	Address Inputs
$\overline{CASL}$, $\overline{CASU}$	Column-Address Strobe/Byte Selects
DQ0–DQ15	DRAM Data I/O, Write Mask Data
DSF	Special Function Select
NC/GND	No Connect/Ground (Important: Not connected internally to V_{SS})
QSF	Special Function Output
$\overline{RAS}$	Row-Address Strobe
SC	Serial Clock
$\overline{SE}$	Serial Enable
SQ0–SQ15	Serial Data Output
$\overline{TRG}$	Output Enable, Transfer Select
V_{CC}	5-V Supply (TYP)
V_{SS}	Ground
$\overline{WE}$	DRAM Write-Enable Select

	ACCESS TIME ROW ENABLE $t_{a(R)}$ (MAX)	ACCESS TIME SERIAL DATA $t_{a(SQ)}$ (MAX)	DRAM CYCLE TIME $t_{c(W)}$ (MIN)	DRAM PAGE MODE $t_{c(P)}$ (MIN)	SERIAL CYCLE TIME $t_{c(SC)}$ (MIN)	OPERATING CURRENT SERIAL PORT STANDBY I_{CC1} (MAX)	OPERATING CURRENT SERIAL PORT ACTIVE I_{CC1A} (MAX)
TMS55160-60	60 ns	15 ns	110 ns	35 ns	18 ns	180 mA	225 mA
TMS55160-70	70 ns	20 ns	130 ns	40 ns	22 ns	165 mA	205 mA
TMS55160-80	80 ns	25 ns	150 ns	45 ns	30 ns	150 mA	185 mA

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description

The TMS55160 multiport video RAM is a high-speed dual-ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262144 words of 16 bits each interfaced to a serial data register [serial-access memory (SAM)] organized as 256 words of 16 bits each. The TMS55160 supports three basic types of operation: random access to and from the DRAM, serial access from the serial register, and transfer of data from any row in the DRAM to the serial register. Except during transfer operations, the TMS55160 can be accessed simultaneously and asynchronously from the DRAM and SAM ports.

The TMS55160 is equipped with several features designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's (4 × 4) × 4 block-write feature. The block-write mode allows 16 bits of data (present in an on-chip color data register) to be written to any combination of four adjacent column-address locations. As many as 64 bits of data can be written to memory during each $\overline{CAS}$ cycle time. Also on the DRAM port, a write mask or a write-per-bit feature allows masking of any combination of the 16 inputs/outputs on any write cycle. The persistent write-per-bit feature uses a mask register that, once loaded, can be used on subsequent write cycles without reloading. The TMS55160 also offers byte control. Byte control can be applied in read cycles, write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles.

The TMS55160 offers a split-register-transfer read (DRAM to SAM) feature for the serial register (SAM port). This feature enables real-time register load implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. For applications not requiring real-time register load (for example, loads done during CRT retrace periods), the full-register mode of operation is retained to simplify system design.

The SAM port is designed for maximum performance. Data can be accessed from the SAM at serial rates up to 55 MHz. During the split-register-transfer read operations, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, QSF, is included to indicate which half of the serial register is active.

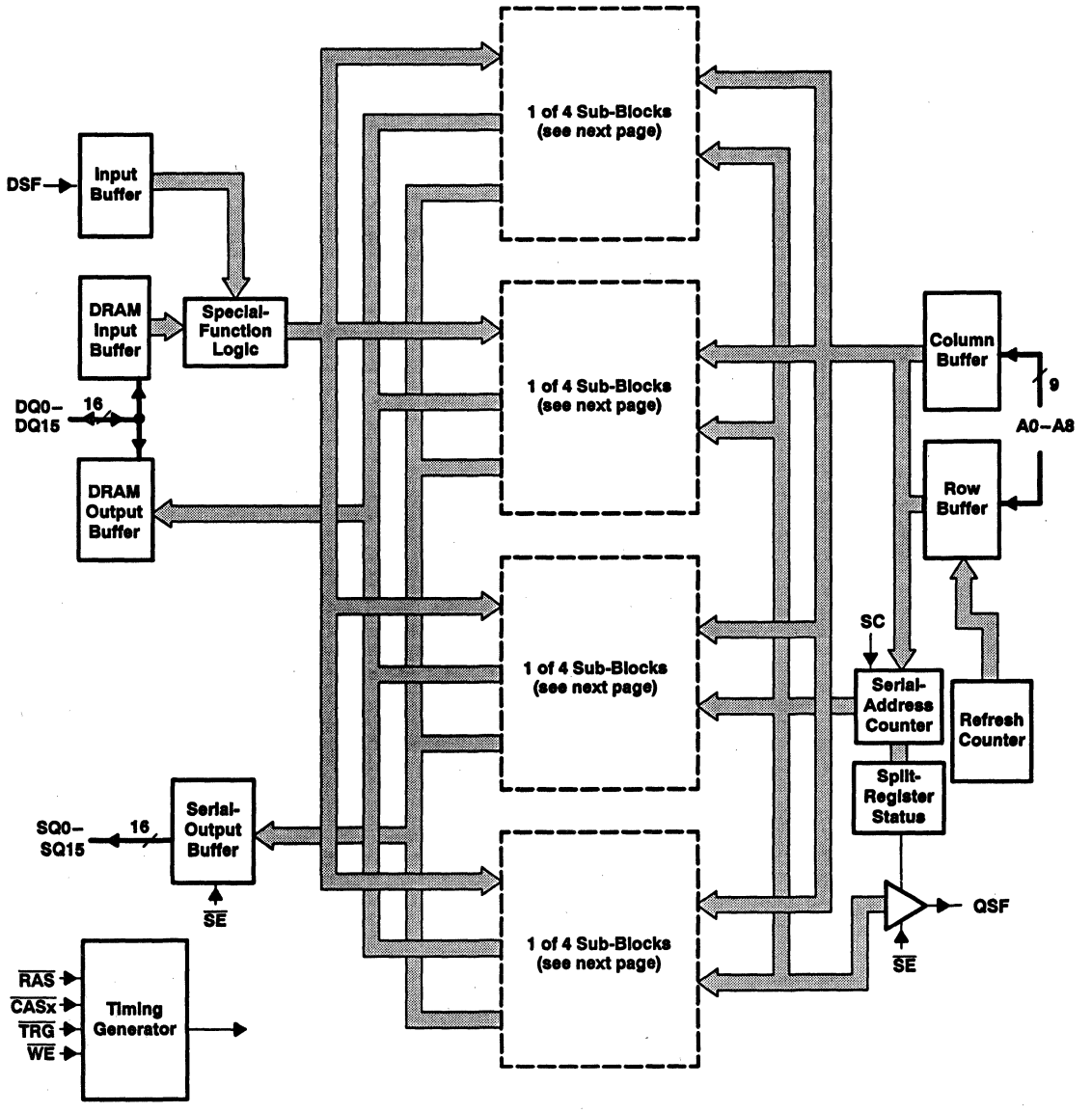
All inputs, outputs, and clock signals on the TMS55160 are compatible with Series 74 TTL. All address lines and data-in lines are latched on chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

The TMS55160 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The TMS55160 is offered in a 64-pin small-outline gull-wing-leaded package (DGH suffix) for direct surface mounting.

The TMS55160 and other TI multiport video RAMs are supported by a broad line of graphics processors and control devices from Texas Instruments.

functional block diagram



functional block diagram (continued)

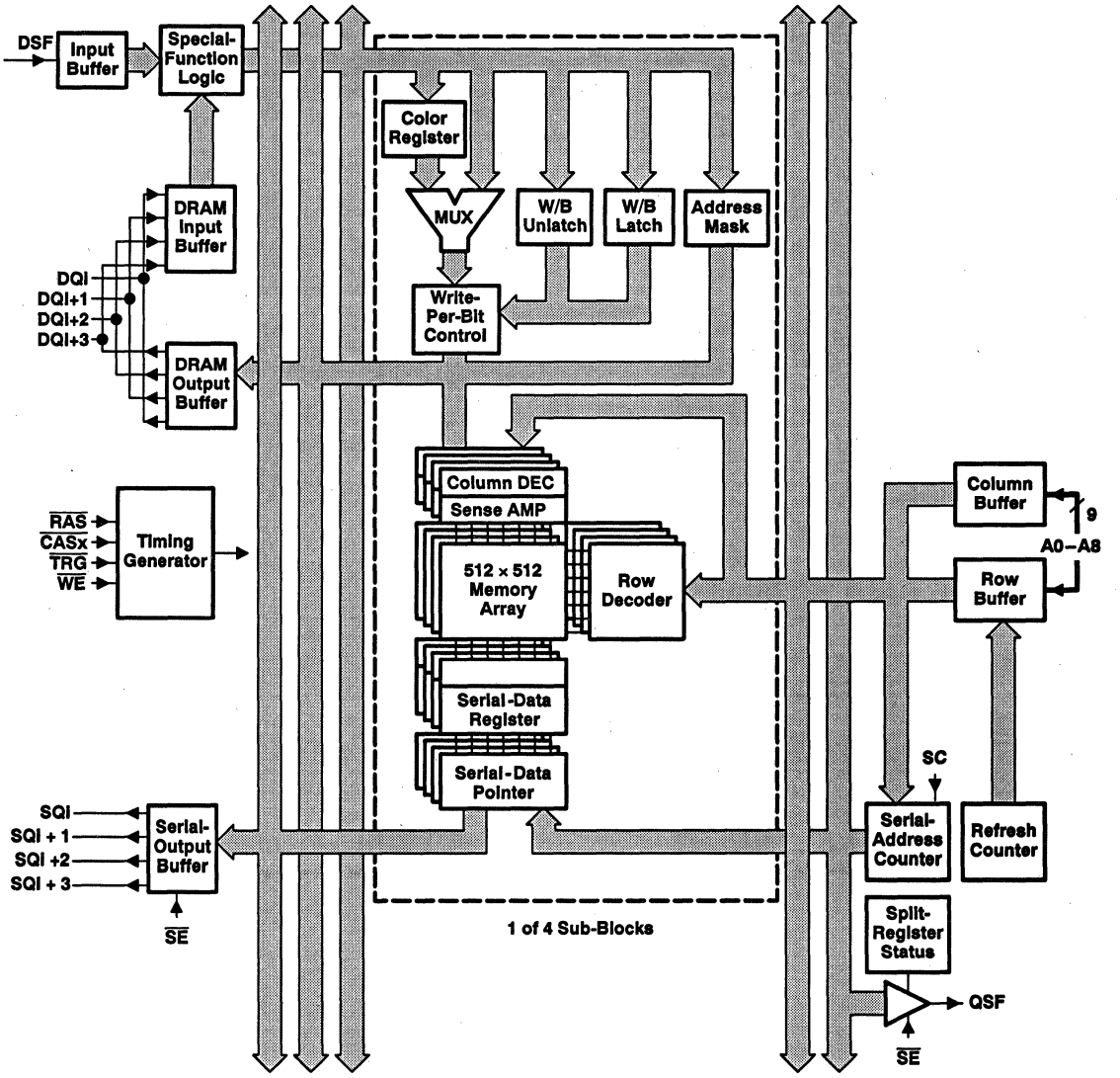


Table 1. Function Table

FUNCTION	RAS FALL				CASx FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CASx‡	TRG	WE	DSF	DSF	RAS	CASx§	RAS	CASL CASU WE	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop-point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)*	L	X	H	H	X	X	X	X	X	CBRN
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
Load write-mask register□	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
X = Don't care
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled

† DQ0–DQ15 are latched on either the first falling edge of CASx or the falling edge of WE, whichever occurs later.
‡ Logic L is selected when either or both CASL and CASU are low.
§ The column address and block address are latched on the first falling edge of CASx.
¶ CBRS cycle should be performed immediately after the power-up initialization cycle.
# A0–A3, A8: don't care; A4–A7: stop-point code
‖ CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
* CBR refresh (no reset) mode does not end persistent write-per-bit mode or stop-point mode.
□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.

Table 2. Pin Description Versus Operational Mode

PIN	DRAM	TRANSFER	SAM
A0 – A8	Row, column address	Row address, tap point	
$\overline{CASL}$ $\overline{CASU}$	Column-address strobe, DQ output enable	Tap-address strobe	
DQ	DRAM data I/O, Write mask		
DSF	Block-write enable Write-mask-register load enable Color-register load enable CBR (option reset)	Split-register-transfer enable	
$\overline{RAS}$	Row-address strobe	Row-address strobe	
$\overline{SE}$			SQ output enable, QSF output enable
SC			Serial clock
SQ			Serial-data output
$\overline{TRG}$	DQ output enable	Transfer enable	
$\overline{WE}$	Write enable		
QSF			Serial-register status
NC/GND	Make no external connection or tie to system GND		
V_{CC}†	5-V supply		
V_{SS}†	Ground		

† For proper device operation, all V_{CC} pins must be connected to a 5-V supply, and all V_{SS} pins must be tied to ground.

pin definitions

address (A0–A8)

Eighteen address bits are required to decode one of 262144 storage cell locations. Nine row-address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Nine column-address bits are set up on pins A0–A8 and latched onto the chip on the first falling edge of $\overline{CASx}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and the first falling edge of $\overline{CASx}$.

During the full-register-transfer read operation, the states of A0–A8 are latched on the falling edge of $\overline{RAS}$ to select one of the 512 rows where the transfer occurs. At the first falling edge of $\overline{CASx}$, the column-address bits A0–A8 are latched. The most significant column-address bit (A8) selects which half of the row is transferred to the SAM. The appropriate 8-bit column address (A0–A7) selects one of 256 tap points (starting positions) for the serial data output.

During the split-register-transfer read operation, address bit A7 is ignored at the falling edge of $\overline{CASx}$. An internal counter selects which half of the register is used. If the high half of the SAM is currently in use, the low half of the SAM is loaded with the low half of the DRAM half row, and vice versa. Column address (A8) selects the DRAM half row. The remaining seven address bits (A0–A6) are used to select 1 of 127 possible starting locations within the SAM. Locations 127 and 255 are not valid tap points.

row-address strobe ($\overline{RAS}$)

$\overline{RAS}$ is similar to a chip enable, so that all DRAM cycles and transfer cycles are initiated by the falling edge of $\overline{RAS}$. $\overline{RAS}$ is a control input that latches the states of the row address, $\overline{WE}$, $\overline{TRG}$, $\overline{CASL}$, $\overline{CASU}$, and DSF onto the chip to invoke DRAM and transfer read functions of the TMS55160.

column-address strobe ($\overline{CASL}$, $\overline{CASU}$)

$\overline{CASL}$ and $\overline{CASU}$ are control inputs that latch the states of the column address and DSF to control DRAM and transfer functions of the TMS55160. $\overline{CASx}$ also act as output enables for the DRAM output pins DQ0–DQ15.

In DRAM operation, $\overline{CASL}$ enables data to be written to or read from the lower byte (DQ0–DQ7) and $\overline{CASU}$ enables data to be written to or from the upper byte (DQ8–DQ15).

In transfer operations, address bits A0–A8 are latched at the first falling edge of $\overline{CASx}$ as the start position (tap) for the serial data output (SQ0–SQ15).

output enable/transfer select ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either DRAM or transfer operation as $\overline{RAS}$ falls. For DRAM operation, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. During DRAM operation, $\overline{TRG}$ functions as an output enable for the DRAM output pins DQ0–DQ15. For transfer operation, $\overline{TRG}$ must be brought low before $\overline{RAS}$ falls.

write mask select, write enable ($\overline{WE}$)

In DRAM operation, $\overline{WE}$ enables data to be written to the DRAM. $\overline{WE}$ is also used to select the DRAM write-per-bit mode of operation. Holding $\overline{WE}$ low on the falling edge of $\overline{RAS}$ invokes the write-per-bit operation. The TMS55160 supports both the nonpersistent write-per-bit mode and the persistent write-per-bit mode.

special function select (DSF)

The DSF input is latched on the falling edge of $\overline{RAS}$ or the first falling edge of $\overline{CASx}$, similar to an address. DSF determines which of the following functions are invoked on a particular cycle:

- CBR refresh with reset (CBR)
- CBR refresh with no reset (CBRN)
- CBR refresh with no reset and stop point set (CBRS)
- Block write
- Loading write-mask register for the persistent write-per-bit mode (LMR)
- Loading color register for the block-write mode
- Split-register-transfer read

DRAM data I/O, write mask data (DQ0–DQ15)

DRAM data is written or read through the common I/O DQ pins. The 3-state DQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state as long as either $\overline{TRG}$ or $\overline{CASx}$ is held high. Data does not appear at the outputs until after both $\overline{CASx}$ and $\overline{TRG}$ have been brought low. The write mask is latched into the device via the random DQ pins by the falling edge of $\overline{RAS}$ and is used on all write-per-bit cycles. In a transfer operation, the DQ outputs remain in the high-impedance state for the entire cycle.

serial data outputs (SQ0–SQ15)

Serial data is read from the SQ pins. The SQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. The serial outputs are in the high-impedance (floating) state as long as the serial enable pin, $\overline{SE}$, is high. The serial outputs are enabled when $\overline{SE}$ is brought low.

serial clock (SC)

Serial data is accessed out of the data register from the rising edge of SC. The TMS55160 is designed to work with a wide range of clock duty cycles to simplify system design. There is no refresh requirement because the data registers that comprise the SAM are static. There is also no minimum SC clock operating frequency.

serial enable ($\overline{SE}$)

During serial access operations, $\overline{SE}$ is used as an enable/disable for the SQ outputs. $\overline{SE}$ low enables the serial data output. $\overline{SE}$ high disables the serial data output. $\overline{SE}$ is also used as an enable/disable for output pin QSF.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is not disabled. External SC pulses increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low because the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

special function output (QSF)

QSF is an output pin that indicates which half of the SAM is being accessed. When QSF is low, the serial address pointer is accessing the lower (least significant) 128 bits of the serial register (SAM). When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM.

During full-register-transfer operations, QSF can change state upon completing the cycle. This state is determined by the tap point loaded during the transfer cycle. The QSF output is enabled by $\overline{SE}$. If $\overline{SE}$ is high, the QSF output is in the high-impedance state.

no connect/ground (NC/GND)

The NC/GND pin should be tied to system ground or left floating for proper device operation.

functional operation description

random access operation

Table 3. DRAM Function Table

FUNCTION	RAS FALL				CASx FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CASx‡	TRG	WE	DSF	DSF	RAS	CASx§	RAS	CASL CASU WE	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop-point set¶	L	X	L	H	X	Stop Point #	X	X	X	CBRS
CBR refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)★	L	X	H	H	X	X	X	X	X	CBRN
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
Load write-mask register □	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
X = Don't care
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled

† DQ0–DQ15 are latched on either the first falling edge of CASx or the falling edge of WE, whichever occurs later.
‡ Logic L is selected when either or both CASL and CASU are low.
§ The column address and block address are latched on the first falling edge of CASx.
¶ CBRS cycle should be performed immediately after the power-up initialization cycle.
# A0–A3, A8: don't care; A4–A7: stop-point code
‖ CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
★ CBR refresh (no reset) mode does not end persistent write-per-bit mode or stop-point mode.
□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.

enhanced page mode

Enhanced-page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. This mode eliminates the time required for row-address setup, row-address hold, and address multiplex. The maximum $\overline{RAS}$ low time and the minimum $\overline{CAS}$ page cycle time are used to determine the number of columns that can be accessed.

Unlike conventional page-mode operations, the enhanced page mode allows the TMS55160 to operate at a higher data bandwidth. Data retrieval begins as soon as the column address is valid rather than when $\overline{CASx}$ transitions low. A valid column address can be presented immediately after the row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CASx}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CASx}$ low) if $t_{a(CA)}$ max (access time from column address) has been satisfied.

refresh

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refreshes are accomplished by bringing either or both $\overline{CASL}$ and $\overline{CASU}$ low earlier than $\overline{RAS}$. The external row address is ignored, and the refresh row address is generated internally. Three types of CBR refresh cycles are available. The CBR refresh (option reset) ends the persistent write-per-bit mode and the stop-point mode. The CBRN and CBRS refreshes (no reset) do not end the persistent write-per-bit mode or the stop-point mode. The 512 rows of the DRAM do not necessarily need to be refreshed consecutively as long as the entire refresh is completed within the required time period, $t_{rf(MA)}$. The output buffers remain in the high-impedance state during the CBR refresh cycles regardless of the state of $\overline{TRG}$.

hidden refresh

A hidden refresh is accomplished by holding both $\overline{CASL}$ and $\overline{CASU}$ low in the DRAM read cycle and cycling $\overline{RAS}$. The output data of the DRAM read cycle remains valid while the refresh is being carried out. Like the CBR refresh, the refreshed row addresses are generated internally during the hidden refresh.

$\overline{RAS}$-only refresh

A $\overline{RAS}$-only refresh is accomplished by cycling $\overline{RAS}$ at every row address. Unless $\overline{CASx}$ and $\overline{TRG}$ are low, the output buffers remain in the high-impedance state to conserve power. Externally generated addresses must be supplied during $\overline{RAS}$-only refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed.

byte operation

Byte operation can be applied in DRAM read cycles, write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. In byte operation, the column address (A0–A8) is latched at the first falling edge of $\overline{CAS}$x. In read cycles, $\overline{CASL}$ enables the lower byte (DQ0–DQ7) and $\overline{CASU}$ enables the upper byte (DQ8–DQ15) (see Figure 1).

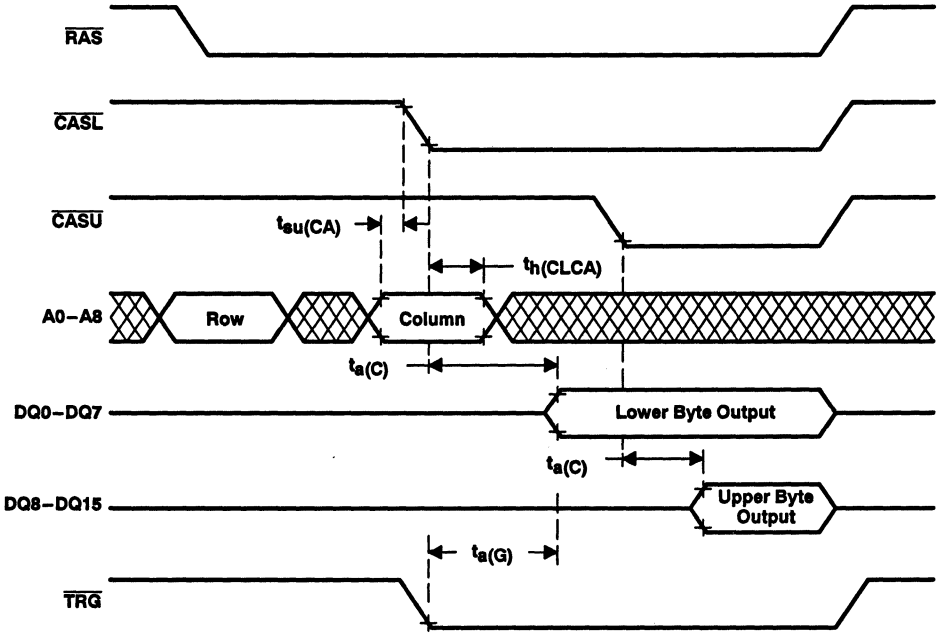


Figure 1. Example of a Byte-Read Cycle

byte operation (continued)

In byte-write operation, $\overline{CASL}$ enables data to be written to the lower byte (DQ0–DQ7) and $\overline{CASU}$ enables data to be written to the upper byte (DQ8–DQ15). In an early-write cycle, $\overline{WE}$ is brought low prior to both $\overline{CASx}$ signals. Data setup and hold times for DQ0–DQ15 are referenced to the first falling edge of $\overline{CASx}$ (see Figure 2).

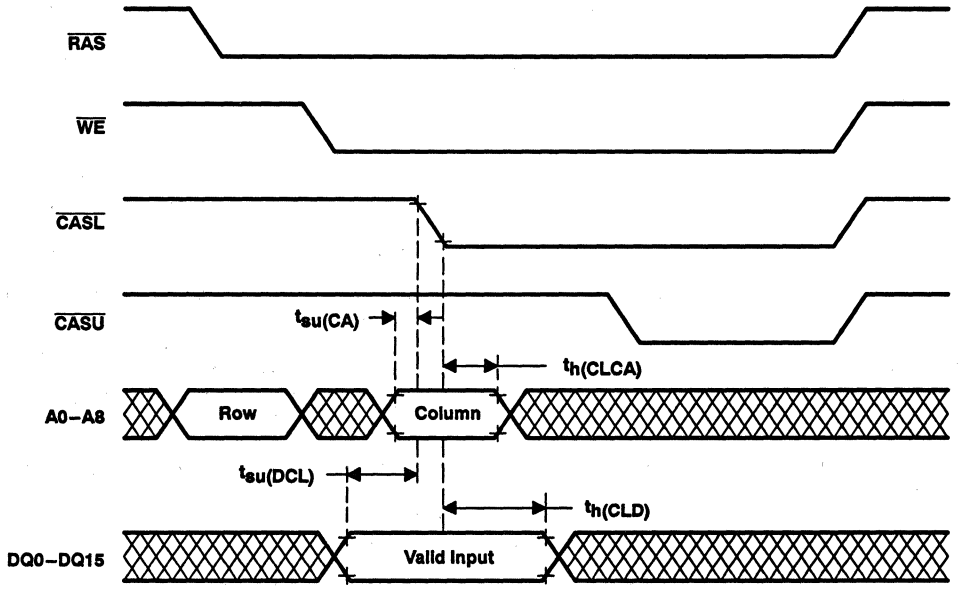


Figure 2. Example of an Early-Write Cycle

byte operation (continued)

For late-write or read-modify-write cycles, $\overline{WE}$ is brought low after either or both $\overline{CASL}$ and $\overline{CASU}$ fall. The data is strobed in with data setup and hold times for DQ0–DQ15 referenced to $\overline{WE}$ (see Figure 3).

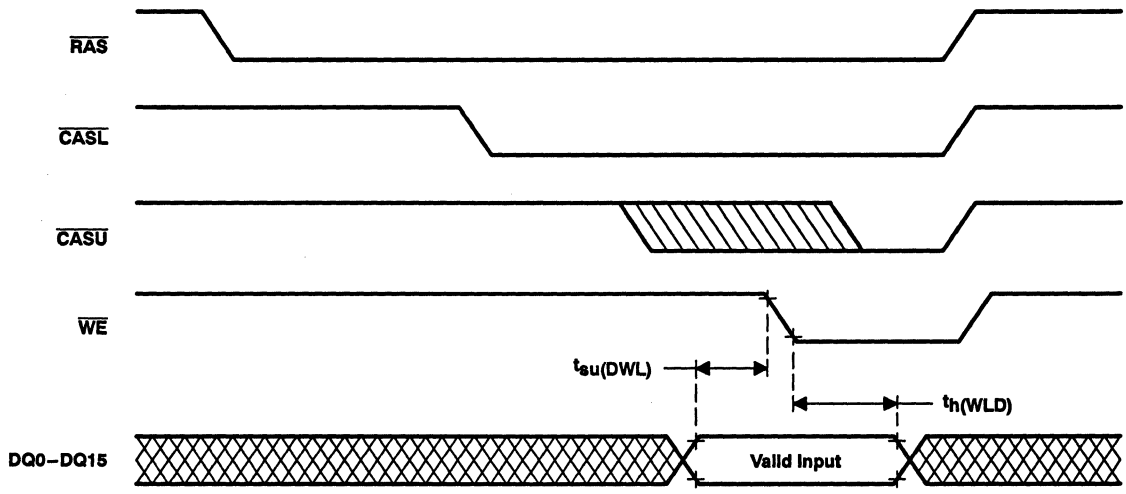


Figure 3. Example of a Late-Write Cycle

write-per-bit

The write-per-bit feature allows masking any combination of the 16 DQs on any write cycle. The write-per-bit operation is invoked when $\overline{WE}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{WE}$ is held high on the falling edge of $\overline{RAS}$, the write operation is performed without any masking. The TMS55160 offers two write-per-bit modes: the nonpersistent write-per-bit and the persistent write-per-bit.

nonpersistent write-per-bit

When $\overline{WE}$ is low on the falling edge of $\overline{RAS}$, the write mask is reloaded. A 16-bit binary code (the write-per-bit mask) is input to the device via the DQ pins and latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the 16 I/Os are to be written and which are not. After $\overline{RAS}$ has latched the on-chip write-per-bit mask, input data is driven onto the DQ pins and is latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. $\overline{CASL}$ enables the lower byte (DQ0–DQ7) to be written through the mask, and $\overline{CASU}$ enables the upper byte (DQ8–DQ15) to be written through the mask. If a data low (write mask = 0) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data is not written to that I/O. If a data high (write mask = 1) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data is written to that I/O (see Figure 4).

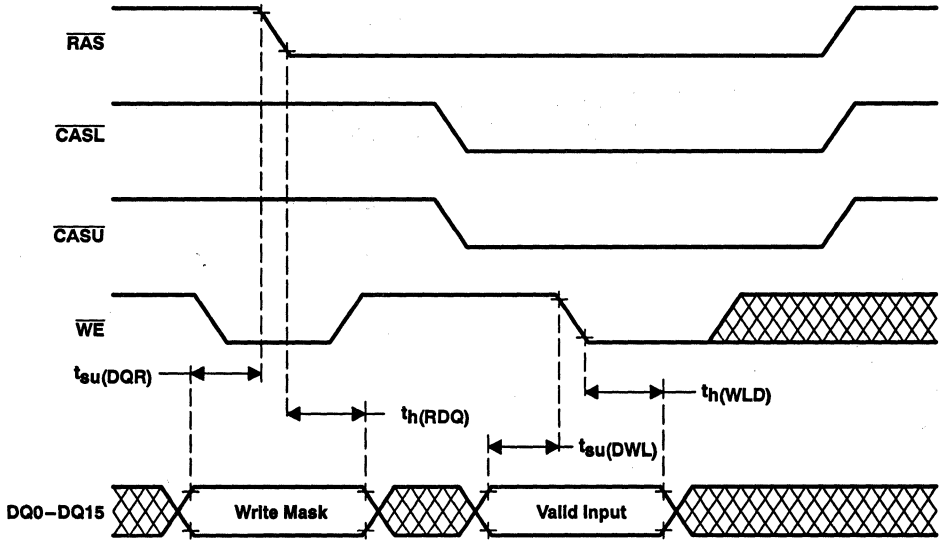


Figure 4. Example of a Nonpersistent Write-Per-Bit (Late-Write) Operation

persistent write-per-bit

The persistent write-per-bit mode is initiated only by performing a load-write-mask-register (LMR) cycle first. In the persistent write-per-bit mode, the write-per-bit mask is not overwritten but remains valid over an arbitrary number of write cycles until another LMR cycle is performed or power is removed.

The load-write-mask-register cycle is performed using DRAM write-cycle timing except DSF is held high on the falling edge of $\overline{RAS}$ and held low on the first falling edge of $\overline{CASx}$. A binary code is input to the write-mask register via the random I/O pins and latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. Byte-write control can be applied to the write mask during the load-write-mask-register cycle. The persistent write-per-bit mode can then be used in exactly the same way as the nonpersistent write-per-bit mode except that the input data on the falling edge of $\overline{RAS}$ is ignored. When the device is set to the persistent write-per-bit mode, it remains in this mode and is reset only by a $\overline{CBR}$ refresh with option reset cycle (see Figure 5).

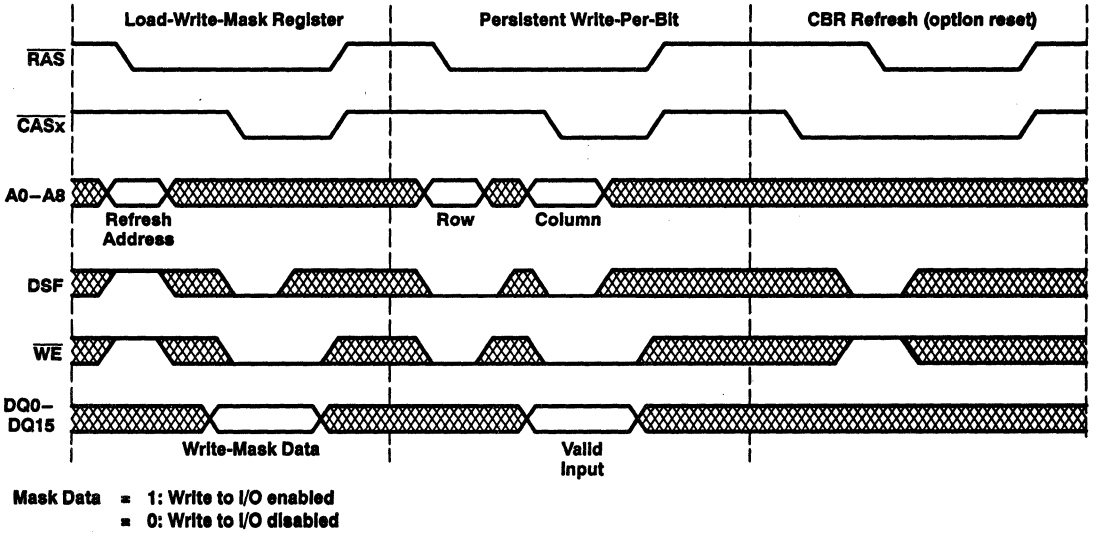


Figure 5. Example of a Persistent Write-Per-Bit Operation

block write

The block-write feature allows up to 64 bits of data to be written simultaneously to one row of the memory array. This function is implemented as (4 columns × 4 DQs) repeated in four quadrants. In this manner, each of the four one-megabit quadrants can have up to four consecutive columns written at a time with up to four DQs per column (see Figure 6).

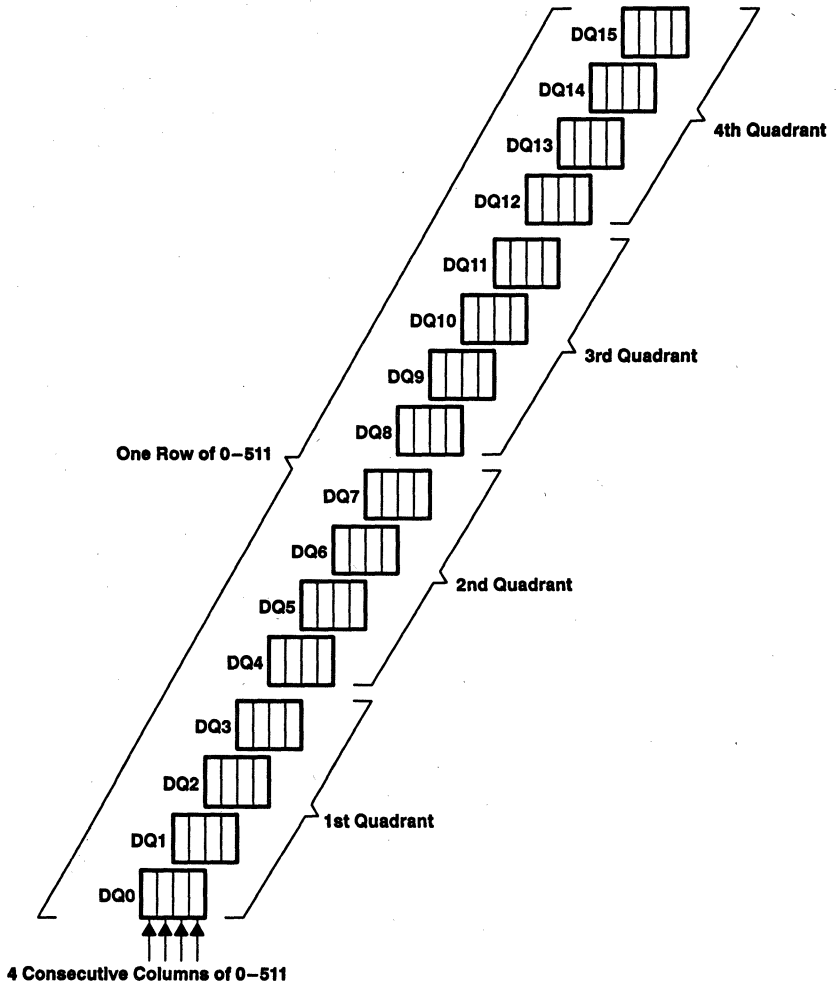


Figure 6. Block-Write Operation

Each one-megabit quadrant has a 4-bit column mask to mask off any or all of the four columns from being written with data. Nonpersistent write-per-bit or persistent write-per-bit functions can be applied to the block-write operation to provide write masking options. The DQ data is provided by four bits from the on-chip color register. Bits 0–3 from the 16-bit write-mask register, bits 0–3 from the 16-bit column-mask register, and bits 0–3 from the 16-bit color-data register configure the block write for the first quadrant, while bits 4–7, 8–11, and 12–15 of the corresponding registers control the other quadrants in a similar fashion (see Figure 7).

block write (continued)

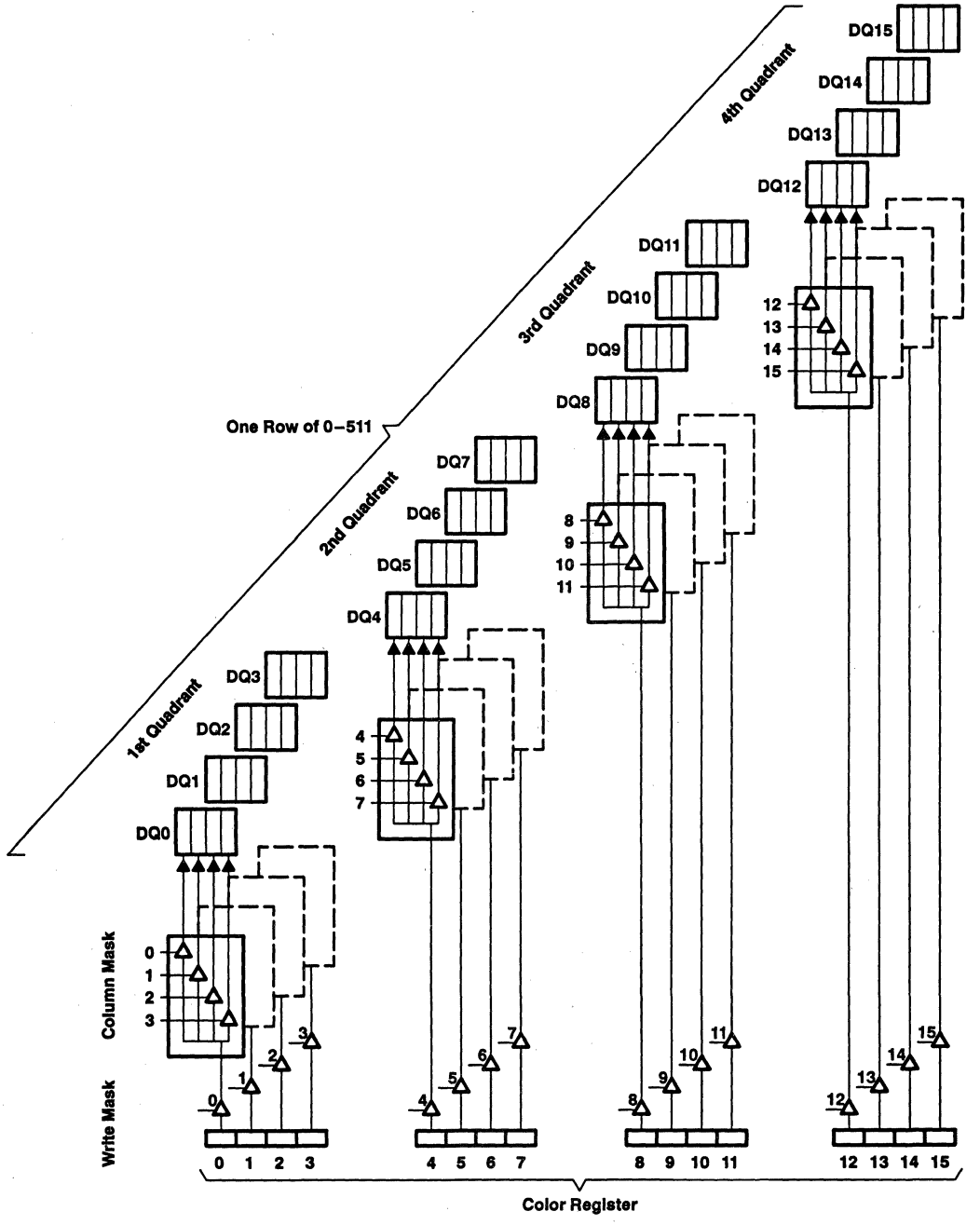


Figure 7. Block Write With Masks

block write (continued)

Every four columns make a block, which makes 128 blocks along one row. Block 0 comprises columns 0–3, block 1 comprises columns 4–7, block 2 comprises columns 8–11, etc., as shown in Figure 8.

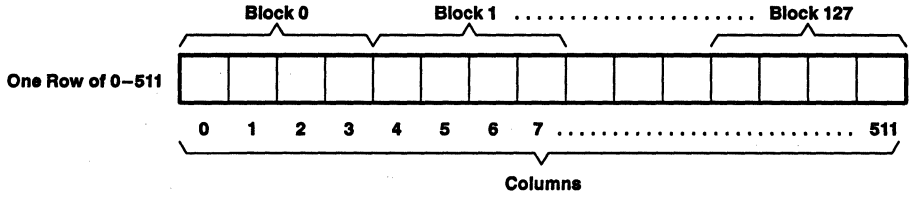


Figure 8. Block Columns Organization

During block-write cycles, only the seven most significant column addresses (A2–A8) are latched on the first falling edge of $\overline{CASx}$ to decode one of the 128 blocks. Address bits A0–A1 are ignored. Each one-megabit quadrant has the same block selected.

A block-write cycle is entered in a manner similar to a DRAM write cycle except DSF is held high on the first falling edge of $\overline{CASx}$. As in a DRAM write operation, $\overline{CASL}$ and $\overline{CASU}$ enable the corresponding lower and upper DRAM DQ bytes to be written, respectively. The column-mask data is input via the DQs and is latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. The 16-bit color-data register must be loaded prior to performing a block write as described below. Refer to the write-per-bit section for details on use of the write-mask capability, allowing additional performance options.

Example of block write:

block-write column address = 110000000 (A0–A8 from left to right)

	bit 0			bit 15
color-data register =	1011	1011	1100	0111
write-mask register =	1110	1111	1111	1011
column-mask register =	1111	0000	0111	1010
	1st Quad	2nd Quad	3rd Quad	4th Quad

Column-address bits A0 and A1 are ignored. Block 0 (columns 0–3) is selected for each one-megabit quadrant. The first quadrant has DQ0–DQ2 written with bits 0–2 from the color-data register (101) to all four columns of block 0. DQ3 is not written and retains its previous data due to the write-mask register bit 3 being a 0.

The second quadrant (DQ4–DQ7) has all four columns masked off due to the column mask bits 4–7 being 0, so that no data is written.

The third quadrant (DQ8–DQ11) has its four DQs written with bits 8–11 from the color-data register (1100) to columns 1–3 of its block 0. Column 0 is not written and retains its previous data on all four DQs due to the column mask-register bit 8 being 0.

The fourth quadrant (DQ12–DQ15) has DQ12, DQ14, and DQ15 written with bits 12, 14, and 15 from the color-data register to column 0 and column 2 of its block 0. DQ13 retains its previous data on all columns due to the write mask. Columns 1 and 3 retain their previous data on all DQs due to the column mask. If the previous data for the quadrant was all 0s, the fourth quadrant would contain the data pattern shown in Figure 9 after the block-write operation shown in the previous example.

block write (continued)

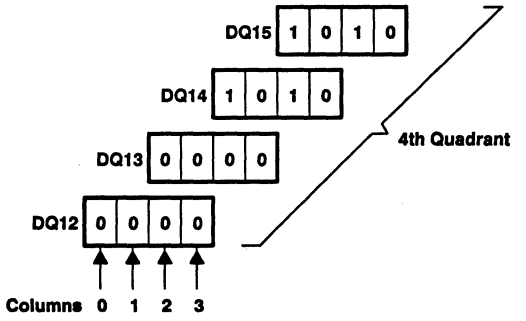
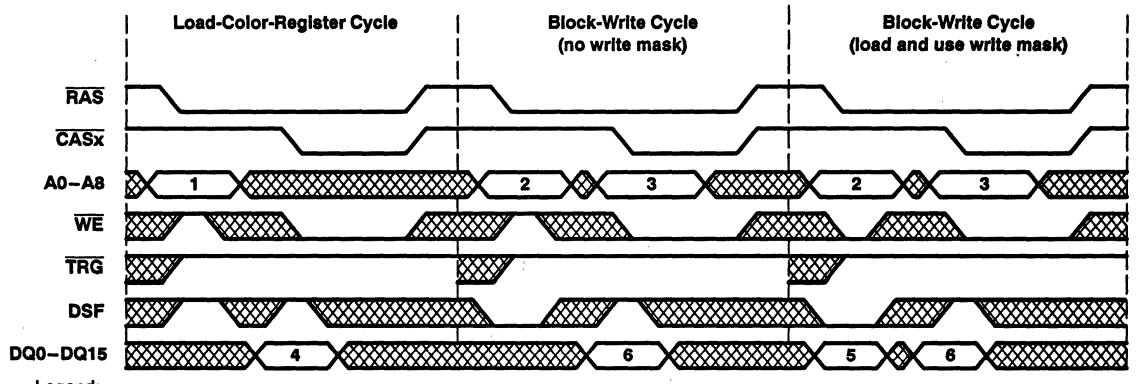


Figure 9. Example of Fourth Quadrant After a Block-Write Operation

load color register

The load-color-register cycle is performed using normal DRAM write-cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$, $\overline{CASL}$, and $\overline{CASU}$. The color register is loaded from pins DQ0–DQ15, which are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. If only one $\overline{CASx}$ is low, only the corresponding byte of the color register is loaded. When the color register is loaded, it retains data until power is lost or until another load-color-register cycle is performed (see Figure 10 and Figure 11).



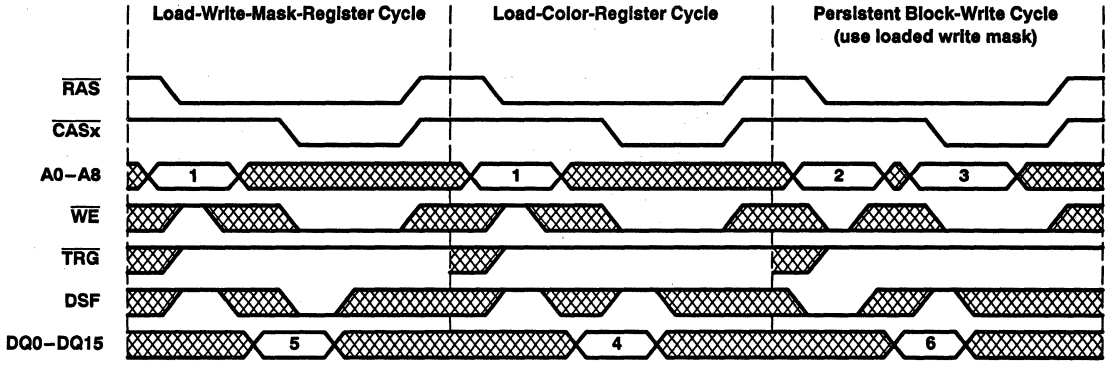
Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the first falling edge of $\overline{CASx}$.
4. Color-register data
5. Write-mask data: DQ0–DQ15 are latched on the falling edge of $\overline{RAS}$.
6. Column-mask data: DQi–DQi+3 (i = 0, 4, 8, 12) are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.

= don't care

Figure 10. Example of Block Writes

load color register (continued)



Legend:
1. Refresh address
2. Row address
3. Blockaddress (A2–A8) is latched on the first falling edge of $\overline{CASx}$.
4. Color-register data
5. Write-mask data: DQ0 – DQ15 are latched on the falling edge of $\overline{CASx}$.
6. Column-mask data: DQi – DQi+3 (i = 0, 4, 8, 12) are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.

= don't care

Figure 11. Example of a Persistent Block Write

DRAM-to-SAM transfer operation

During the DRAM-to-SAM transfer operation, one half of a row (256 columns) in the DRAM array is selected to be transferred to the 256-bit serial-data register. The transfer operation is invoked by bringing $\overline{TRG}$ low and holding $\overline{WE}$ high on the falling edge of $\overline{RAS}$. The state of DSF, which is latched on the falling edge of $\overline{RAS}$, determines whether the full-register-transfer read operation or the split-register-transfer read operation is performed.

Table 4. SAM Function Table

FUNCTION	$\overline{RAS}$ FALL				$\overline{CASx}$ FALL	ADDRESS		DQ0–DQ15		MNE CODE
	$\overline{CASx}$†	$\overline{TRG}$	$\overline{WE}$	DSF	DSF	$\overline{RAS}$	$\overline{CASx}$	$\overline{RAS}$	$\overline{CASx}$ $\overline{WE}$	
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT

† Logic L is selected when either or both $\overline{CASL}$ and $\overline{CASU}$ are low.
X = don't care

full-register-transfer read

A full-register-transfer read operation loads data from a selected half of a row in the DRAM into the SAM. $\overline{TRG}$ is brought low and latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. The nine column-address bits (A0–A8) are latched at the first falling edge of $\overline{CASx}$, where address bit A8 selects which half of the row is transferred. Address bits A0–A7 select one of the SAM's 256 available tap points from which the serial data is read out (see Figure 12).

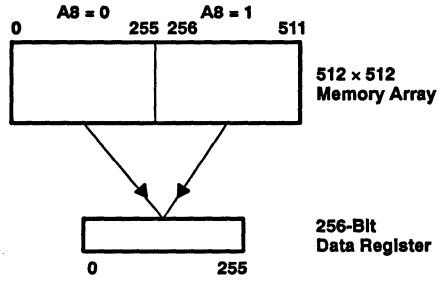


Figure 12. Full-Register-Transfer Read

A full-register-transfer read can be performed in three ways: early load, real-time load (or midline load), or late load. Each of these offers the flexibility of controlling the $\overline{TRG}$ trailing edge in the full-register-transfer read cycle (see Figure 13).

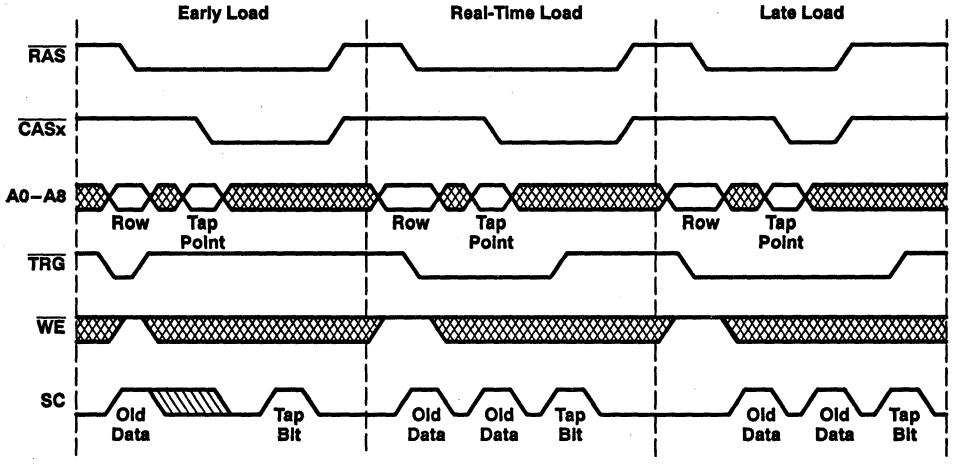


Figure 13. Example of Full-Register-Transfer Read Operations

split-register-transfer read

In the split-register-transfer read operation, the serial data register is split into halves. The low half contains bits 0–127, and the high half contains bits 128–255. While one half is being read out of the SAM port, the other half can be loaded from the memory array.

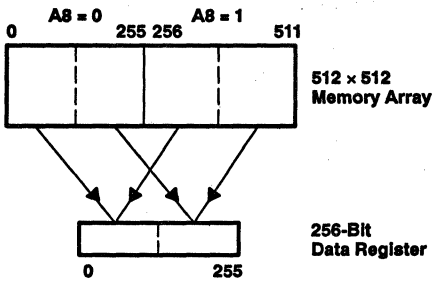
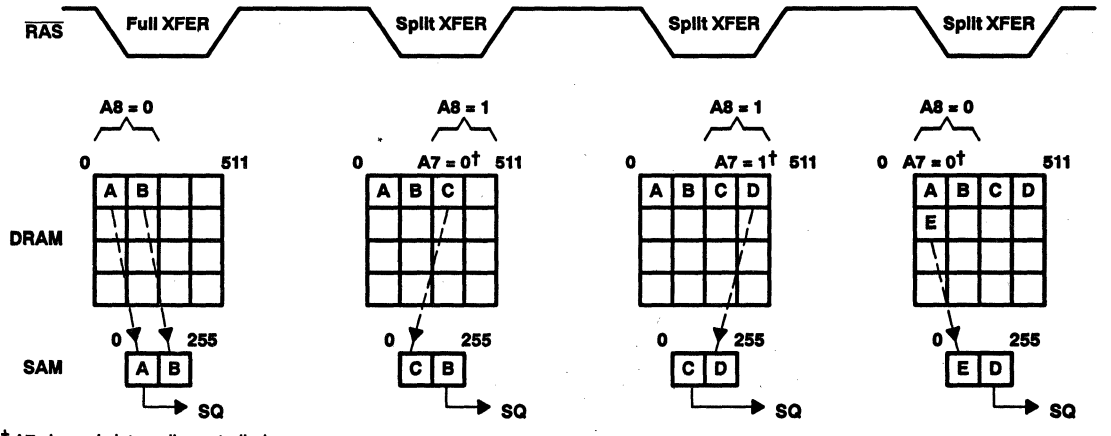


Figure 14. Split-Register-Transfer Read

To invoke a split-register-transfer read cycle, DSF is brought high, $\overline{TRG}$ is brought low, and both are latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. Eight of the nine column-address bits (A0–A6 and A8) are latched at the first falling edge of $\overline{CASx}$. Column-address bit A8 selects which half of the row is to be transferred. Column-address bits A0–A6 select one of the 127 tap points in the specified half of the SAM. Column-address bit A7 is ignored, and the split-register-transfer is internally controlled to select the inactive register half.



† A7 shown is internally controlled.

Figure 15. Example of a Split-Register-Transfer Read Operation

A full-register-transfer read must precede the first split-register-transfer read to ensure proper operation. After the full-register-transfer read cycle, the first split-register-transfer read can follow immediately without any minimum SC clock requirement.

split-register-transfer read (continued)

QSF indicates which half of the register is being accessed during serial access operation. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of the SAM. When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF changes state upon completing a full-register-transfer read cycle. The tap point loaded during the current transfer cycle determines the state of QSF. QSF also changes state when a boundary between two register halves is reached.

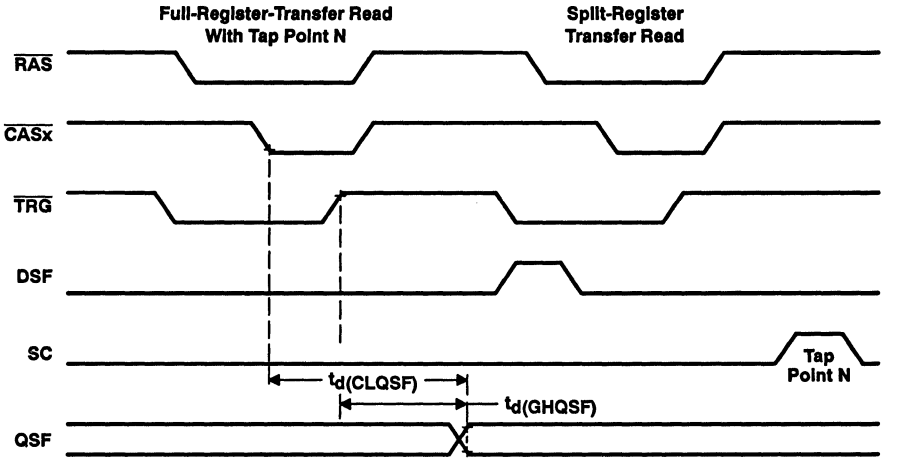


Figure 16. Example of a Split-Register-Transfer Read After a Full-Register-Transfer Read

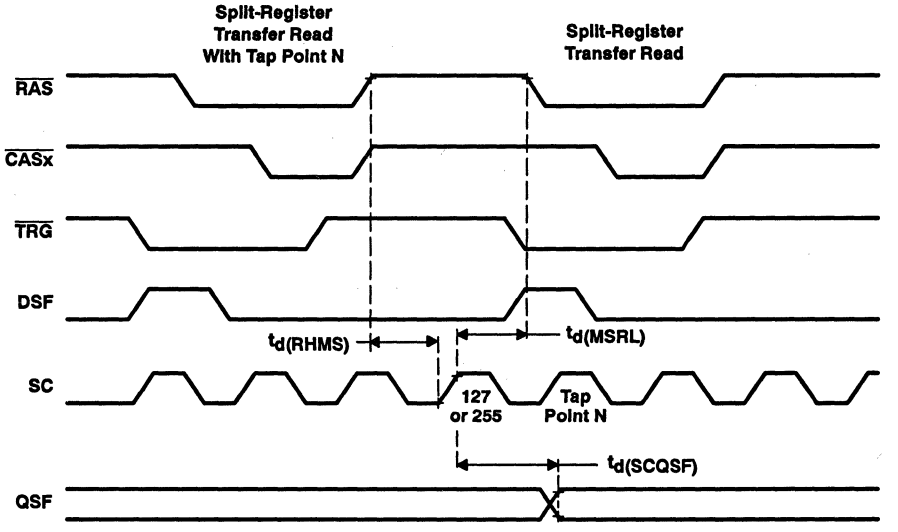


Figure 17. Example of Successive Split-Register-Transfer Read Operations

serial-read operation

The serial-read operation can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during transfer operations. Serial data can be read from the SAM by clocking SC starting at the tap point loaded by the preceding transfer cycle, proceeding sequentially to the most significant bit (bit 255), and then wrapping around to the least significant bit (bit 0), as shown in Figure 18.

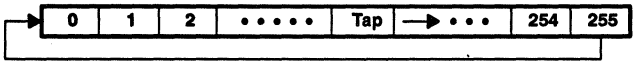


Figure 18. Serial Pointer Direction for Serial Read

For split-register-transfer read operation, serial data can be read out from the active half of the SAM by clocking SC starting at the tap point loaded by the preceding split-register-transfer cycle. The serial pointer proceeds sequentially to the most significant bit of the half, bit 127 or bit 255. If there is a split-register-transfer read to the inactive half during this period, the serial pointer points next to the tap point location loaded by that split-register-transfer (see Figure 19).

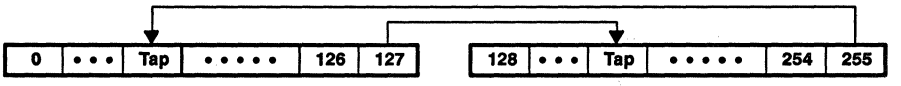


Figure 19. Serial Pointer for Split-Register Read – Case I

If there is no split-register-transfer read to the inactive half during this period, the serial pointer points next to the least significant bit of the inactive half, bit 128 or bit 0 (see Figure 20).

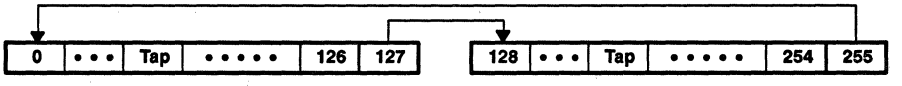


Figure 20. Serial Pointer for Split-Register Read – Case II

split-register programmable stop point

The TMS55160 offers programmable stop-point mode for split-register-transfer read operation. This mode can be used to improve 2-D drawing performance in a nonscanline data format.

In split-register-transfer read operation, the stop point is defined as a register location at which the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM. While in stop-point mode, the SAM is divided into partitions whose length is programmed via row addresses A4–A7 in a $\overline{\text{CBR}}$ set (CBRS) cycle. The last serial-address location of each partition is the stop point (see Figure 21).

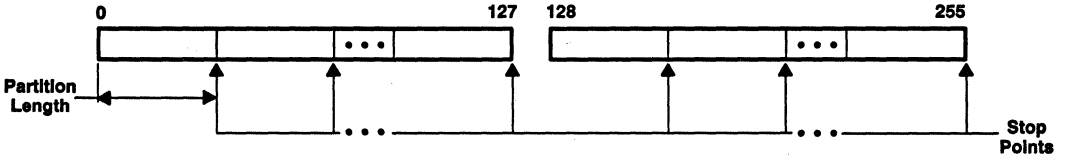


Figure 21. Example of the SAM With Partitions

split-register programmable stop point (continued)

Stop-point mode is not active until the CBRS cycle is initiated. The CBRS operation is performed by holding $\overline{CAS}$x and $\overline{WE}$ low and DSF high on the falling edge of $\overline{RAS}$. The falling edge of $\overline{RAS}$ latches row addresses A4–A7, which are used to define the SAM's partition length. The other row-address inputs are don't care. Stop-point mode should be initiated after the initialization cycles have been performed (see Table 5).

Table 5. Programming Code for Stop-Point Mode

MAXIMUM PARTITION LENGTH	ADDRESS AT $\overline{RAS}$ IN CBRS CYCLE						NUMBER OF PARTITIONS	STOP-POINT LOCATIONS
	A8	A7	A6	A5	A4	A0–A3		
16	X	L	L	L	L	X	16	15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255
32	X	L	L	L	H	X	8	31, 63, 95, 127, 159, 191, 223, 255
64	X	L	L	H	H	X	4	63, 127, 191, 255
128 (default)	X	L	H	H	H	X	2	127, 255

In stop-point mode, the tap point loaded during the split-register-transfer read cycle determines in which SAM partition the serial output begins and at which stop point the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM (see Figure 22).

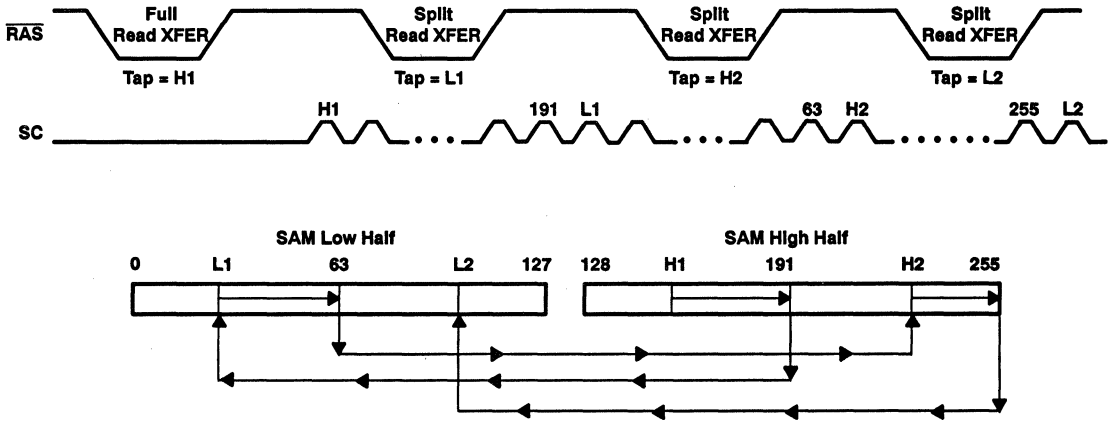


Figure 22. Example of Split-Register Operation With Programmable Stop Points

256-/512-bit compatibility of split-register programmable stop point

The stop-point mode is designed to be compatible both for 256-bit SAM and 512-bit SAM devices. After the CBRS cycle is initiated, the stop-point mode becomes active. In the stop-point mode, and only in the stop-point mode, the column-address bits AY7 and AY8 are internally swapped to assure the compatibility (see Figure 23). This address-bit swap applies to the column address, and it is effective for all DRAM and transfer cycles. For example, during the split-register-transfer cycle with stop point, column-address bit AY8 is a don't care and AY7 decodes the DRAM row half for the split-register-transfer. During stop-point mode, a $\overline{CBR}$ option reset cycle is not recommended because it ends the stop-point mode and restores address bits AY7 and AY8 to their normal function. Consistent use of CBR cycles ensures that the TMS55160 remains in normal mode.

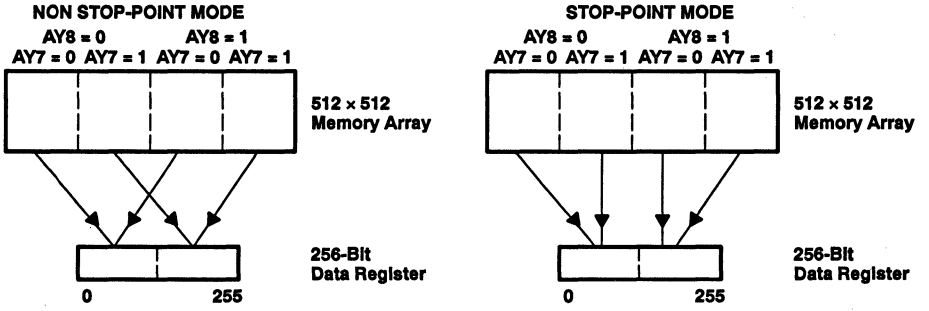


Figure 23. DRAM-to-SAM Mapping, Non Stop-Point Versus Stop Point

IMPORTANT: For proper device operation in a split-register stop-point mode, a CBRS cycle should be initiated right after the power-up initialization cycles have been performed.

power up

To achieve proper device operation, an initial pause of 200 µs is required after power up followed by a minimum of eight $\overline{RAS}$ cycles or eight $\overline{CBR}$ cycles to initialize the DRAM port. A full-register-transfer read cycle and two SC cycles are needed to initialize the SAM port.

After initialization, the internal state of the TMS55160 is as follows:

	STATE AFTER INITIALIZATION
QSF	Defined by the transfer cycle during initialization
Write mode	Nonpersistent mode
Write-mask register	Undefined
Color register	Undefined
Serial-register tap point	Defined by the transfer cycle during initialization
SAM port	Output mode

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −1 V to 7 V
Voltage range on any pin ..... −1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1.1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	SAM PORT	'55160-60		'55160-70		'55160-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –1 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 5.8 V, All other pins at 0 V to V_{CC}			±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC} See Note 3			±10		±10		±10	µA
I_{CC1}	Operating current§	See Note 4	Standby		180		165		150	mA
I_{CC1A}	Operating current§	$t_{c(SC)}$ = MIN	Active		225		205		185	mA
I_{CC2}	Standby current	All clocks = V_{CC}	Standby		5		5		5	mA
I_{CC2A}	Standby current	$t_{c(SC)}$ = MIN	Active		70		65		60	mA
I_{CC3}	$\overline{RAS}$-only refresh current	See Note 4	Standby		180		165		150	mA
I_{CC3A}	$\overline{RAS}$-only refresh current	$t_{c(SC)}$ = MIN, See Note 5	Active		225		205		185	mA
I_{CC4}	Page-mode current§	$t_{c(P)}$ = MIN, See Note 5	Standby		135		115		105	mA
I_{CC4A}	Page-mode current§	$t_{c(SC)}$ = MIN, See Note 5	Active		175		155		140	mA
I_{CC5}	CBR current	See Note 4	Standby		180		165		150	mA
I_{CC5A}	CBRcurrent	$t_{c(SC)}$ = MIN, See Note 5	Active		225		205		185	mA
I_{CC6}	Data-transfer current	See Note 4	Standby		200		180		160	mA
I_{CC6A}	Data-transfer current	$t_{c(SC)}$ = MIN	Active		250		225		200	mA

‡ For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
§ Measured with outputs open
NOTES: 3. $\overline{SE}$ is disabled for SQ output leakage tests.
4. Measured with one address change while $\overline{RAS}$ = V_{IL}, $t_{c(rd)}$, $t_{c(W)}$, $t_{c(TRD)}$, = MIN.
5. Measured with one address change while $\overline{CASx}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, address strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(DSF)}$	Input capacitance, special function		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
$C_{o(O)}$	Output capacitance, SQ and DQ		7	pF
$C_{o(QSF)}$	Output capacitance, QSF		9	pF

NOTE 6: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		TEST CONDITIONS†	ALT. SYMBOL	'55160-60		'55160-70		'55160-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CASx}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		17		20		20	ns
$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{AA}		30		35		40	ns
$t_{a(CP)}$	Access time from $\overline{CASx}$ high	$t_{d(RLCL)}$ = MAX	t_{CPA}		35		40		45	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MAX	t_{RAC}		60		70		80	ns
$t_{a(G)}$	Access time of DQ from $\overline{TRG}$ low		t_{OEA}		15		20		20	ns
$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 30 pF	t_{SCA}		15		20		25	ns
$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		12		15		20	ns
$t_{dis(CH)}$	Disable time, random output from $\overline{CASx}$ high (see Note 8)	C_L = 50 pF	t_{OFF}	0	15	0	20	0	20	ns
$t_{dis(G)}$	Disable time, random output from $\overline{TRG}$ high (see Note 8)	C_L = 50 pF	t_{OEZ}	0	15	0	20	0	20	ns
$t_{dis(SE)}$	Disable time, serial output from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	0	10	0	15	0	20	ns

† Measured with outputs open. For conditions shown as MIN/MAX, use the appropriate value specified under timing requirements.

NOTES: 7. Switching times for RAM port output are measured with a load equivalent to 1 TTL load and 50 pF. Data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V. Switching times for SAM port output are measured with a load equivalent to 1 TTL load and 30 pF. Serial data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V.

8. $t_{dis(CH)}$, $t_{dis(G)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature†

		ALT. SYMBOL	'55160-60		'55160-70		'55160-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Cycle time, read	t_{RC}	110		130		150		ns
$t_{c(W)}$	Cycle time, write	t_{WC}	110		130		150		ns
$t_{c(rdW)}$	Cycle time, read-modify-write	t_{RMW}	150		175		200		ns
$t_{c(P)}$	Cycle time, page-mode read, write	t_{PC}	35		40		45		ns
$t_{c(RDWP)}$	Cycle time, page-mode read-modify-write	t_{PRMW}	80		90		100		ns
$t_{c(TRD)}$	Cycle time, transfer read	t_{RC}	110		130		150		ns
$t_{c(SC)}$	Cycle time, serial clock (see Note 9)	t_{SCC}	18		22		30		ns
$t_{w(CH)}$	Pulse duration, $\overline{CASx}$ high	t_{CPN}	10		10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CASx}$ low (see Note 10)	t_{CAS}	17	10 000	20	10 000	20	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	40		50		60		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 11)	t_{RAS}	60	10 000	70	10 000	80	10 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{WE}$ low	t_{WP}	10		10		15		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		15		20		20		ns
$t_{w(SCH)}$	Pulse duration, SC high (see Note 9)	t_{SC}	5		8		10		ns
$t_{w(SCL)}$	Pulse duration, SC low (see Note 9)	t_{SCP}	5		8		10		ns
$t_{w(GH)}$	Pulse duration, $\overline{TRG}$ high	t_{TP}	20		20		20		ns
$t_{w(RL)P}$	Pulse duration, $\overline{RAS}$ low (page mode)	t_{RASP}	60	100 000	70	100 000	80	100 000	ns
$t_{su(CA)}$	Setup time, column address before $\overline{CASx}$ low	t_{ASC}	0		0		0		ns
$t_{su(SFC)}$	Setup time, DSF before $\overline{CASx}$ low	t_{FSC}	0		0		0		ns
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(WMR)}$	Setup time, $\overline{WE}$ before $\overline{RAS}$ low	t_{WSR}	0		0		0		ns
$t_{su(DQR)}$	Setup time, DQ before $\overline{RAS}$ low	t_{MS}	0		0		0		ns
$t_{su(TRG)}$	Setup time, $\overline{TRG}$ high before $\overline{RAS}$ low	t_{THS}	0		0		0		ns
$t_{su(SFR)}$	Setup time, DSF low before $\overline{RAS}$ low	t_{FSR}	0		0		0		ns
$t_{su(DCL)}$	Setup time, data valid before $\overline{CASx}$ low	t_{DSC}	0		0		0		ns
$t_{su(DWL)}$	Setup time, data valid before $\overline{WE}$ low	t_{DSW}	0		0		0		ns
$t_{su(rd)}$	Setup time, read command, $\overline{WE}$ high before $\overline{CASx}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	Setup time, early write command, $\overline{WE}$ low before $\overline{CASx}$ low	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	Setup time, $\overline{WE}$ low before $\overline{CASx}$ high, write	t_{CWL}	15		15		20		ns
$t_{su(WRH)}$	Setup time, $\overline{WE}$ low before $\overline{RAS}$ high, write	t_{RWL}	15		15		20		ns
$t_{h(CLCA)}$	Hold time, column address after $\overline{CASx}$ low	t_{CAH}	10		10		15		ns
$t_{h(SFC)}$	Hold time, DSF after $\overline{CASx}$ low	t_{CFH}	10		10		15		ns
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low	t_{RAH}	10		10		10		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. Cycle time assumes t_t = 3 ns.

10. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this can require additional $\overline{CASx}$ low time [$t_{w(CL)}$].

11. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this can require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

			ALT. SYMBOL	'55160-60		'55160-70		'55160-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(TRG)}$	Hold time, $\overline{TRG}$ after $\overline{RAS}$ low		t_{THH}	10		10		10		ns
$t_{h(RWM)}$	Hold time, write mask after $\overline{RAS}$ low		t_{RWH}	10		10		10		ns
$t_{h(RDQ)}$	Hold time, DQ after $\overline{RAS}$ low (write-mask operation)		t_{MH}	10		10		10		ns
$t_{h(SFR)}$	Hold time, DSF after $\overline{RAS}$ low		t_{RFH}	10		10		10		ns
$t_{h(RLCA)}$	Hold time, column address valid after $\overline{RAS}$ low (see Note 12)		t_{AR}	30		30		35		ns
$t_{h(CLD)}$	Hold time, data valid after $\overline{CASx}$ low		t_{DH}	15		15		15		ns
$t_{h(RLD)}$	Hold time, data valid after $\overline{RAS}$ low (see Note 12)		t_{DHR}	35		35		35		ns
$t_{h(WLD)}$	Hold time, data valid after $\overline{WE}$ low		t_{DH}	15		15		15		ns
$t_{h(CHrd)}$	Hold time, read, $\overline{WE}$ high after $\overline{CASx}$ high (see Note 13)		t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Hold time, read, $\overline{WE}$ high after $\overline{RAS}$ high (see Note 13)		t_{RRH}	0		0		0		ns
$t_{h(CLW)}$	Hold time, write, $\overline{WE}$ low after $\overline{CASx}$ low		t_{WCH}	10		15		15		ns
$t_{h(RLW)}$	Hold time, write, $\overline{WE}$ low after $\overline{RAS}$ low (see Note 12)		t_{WCR}	30		35		35		ns
$t_{h(WLG)}$	Hold time, $\overline{TRG}$ high after $\overline{WE}$ low (see Note 14)		t_{OEH}	10		10		10		ns
$t_{h(SHSQ)}$	Hold time, SQ valid after SC high		t_{SOH}	4		5		5		ns
$t_{h(RSF)}$	Hold time, DSF after $\overline{RAS}$ low		t_{FHR}	30		30		35		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ high		t_{CSH}	60		70		80		ns
		See Note 15	t_{CHR}	10		10		15		
$t_{d(CHRL)}$	Delay time, $\overline{CASx}$ high to $\overline{RAS}$ low		t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ high		t_{RSH}	17		20		20		ns
$t_{d(CLWL)}$	Delay time, $\overline{CASx}$ low to $\overline{WE}$ low (see Notes 16 and 17)		t_{CWD}	37		45		45		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ low (see Note)		t_{RCD}	20	43	20	50	20	60	ns
$t_{d(CARH)}$	Delay time, column address valid to $\overline{RAS}$ high		t_{RAL}	30		35		40		ns
$t_{d(CACH)}$	Delay time, column address valid to $\overline{CASx}$ high		t_{CAL}	30		35		40		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{WE}$ low (see Note 16)		t_{RWD}	80		95		105		ns
$t_{d(CAWL)}$	Delay time, column address valid to $\overline{WE}$ low (see Note 16)		t_{AWD}	50		60		65		ns
$t_{d(CLRL)}$	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ low (see Note 15)		t_{CSR}	0		0		0		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CASx}$ low (see Note 15)		t_{RPC}	0		0		0		ns
$t_{d(CLGH)}$	Delay time, $\overline{CASx}$ low to $\overline{TRG}$ high for DRAM read cycles			17		20		20		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ		t_{OED}	10		15		15		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
14. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
15. CBRrefresh operation only
16. Read-modify-write operation only
17. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
18. The maximum value is specified only to assure $\overline{RAS}$ access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	'55160-60		'55160-70		'55160-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (see Note 19)	t_{RTH}	50		55		60		ns
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 20)	t_{RSD}	65		70		80		ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address valid	t_{RAD}	15	30	15	35	15	40	ns
$t_{d(GLRH)}$	Delay time, $\overline{TRG}$ low to $\overline{RAS}$ high	t_{ROH}	10		15		15		ns
$t_{d(CLSH)}$	Delay time, $\overline{CASx}$ low to first SC high after $\overline{TRG}$ high (see Note 20)	t_{CSD}	20		20		25		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 19 and 20)	t_{TSL}	5		5		5		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 19)	t_{TRD}	−10		−10		−10		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 21)	t_{TRP}	40		50		60		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 19)	t_{TSD}	10		10		15		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split-register-transfer read cycles		15		20		20		ns
$t_{d(CLTH)}$	Delay time, $\overline{CASx}$ low to $\overline{TRG}$ high in real-time transfer read cycles	t_{CTH}	15		15		15		ns
$t_{d(CASH)}$	Delay time, column address to first SC in early-load transfer read cycles	t_{ASD}	25		25		30		ns
$t_{d(CAGH)}$	Delay time, column address to $\overline{TRG}$ high in real-time transfer read cycles	t_{ATH}	20		20		20		ns
$t_{d(DCL)}$	Delay time, data to $\overline{CASx}$ low	t_{DZC}	0		0		0		ns
$t_{d(DGL)}$	Delay time, data to $\overline{TRG}$ low	t_{DZO}	0		0		0		ns
$t_{d(MSRL)}$	Delay time, last (most significant) rising edge of SC to $\overline{RAS}$ low before boundary switch during split-register-transfer read cycles		15		20		20		ns
$t_{d(SCQSF)}$	Delay time, last (127 or 255) rising edge of SC to QSF switching at the boundary during split-register-transfer read cycles (see Note 22)	t_{SQD}		20		25		30	ns
$t_{d(CLQSF)}$	Delay time, $\overline{CASx}$ low to QSF switching in transfer read cycles (see Note 2222)	t_{CQD}		25		30		35	ns
$t_{d(GHQSF)}$	Delay time, $\overline{TRG}$ high to QSF switching in transfer read cycles (see Note 2222)	t_{TQD}		20		25		30	ns
$t_{d(RLQSF)}$	Delay time, $\overline{RAS}$ low to QSF switching in transfer read cycles (see Note 2222)	t_{RQD}		65		70		75	ns
$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 19. Real-time load transfer read or late-load transfer read cycle only
20. Early-load transfer read cycle only
21. Full-register (read) transfer cycles only
22. Switching times for QSF output are measured with a load equivalent to 1 TTL load and 30 pF, and output reference level is V_{OH} / V_{OL} = 2 V/0.8 V.

PARAMETER MEASUREMENT INFORMATION

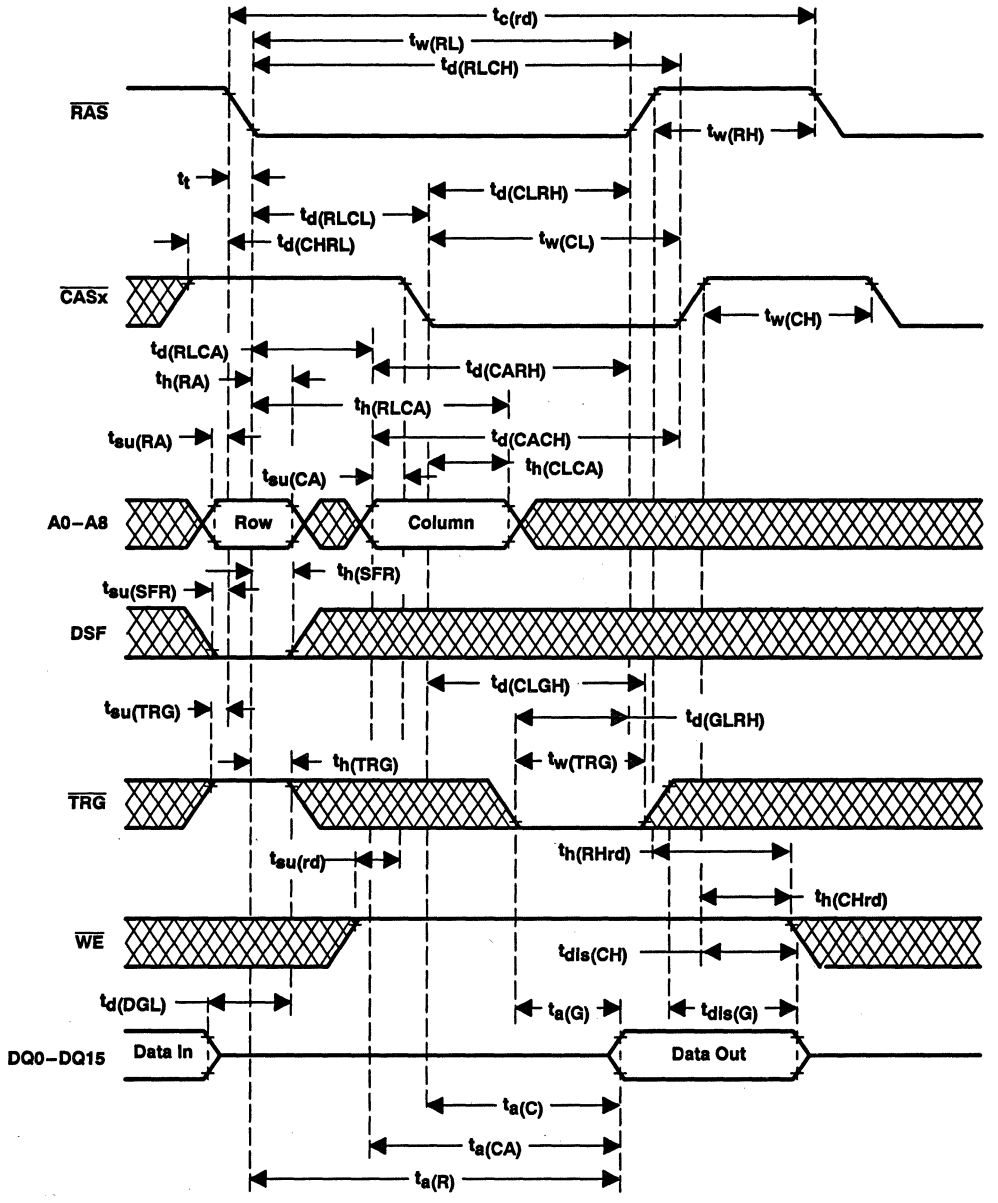


Figure 24. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

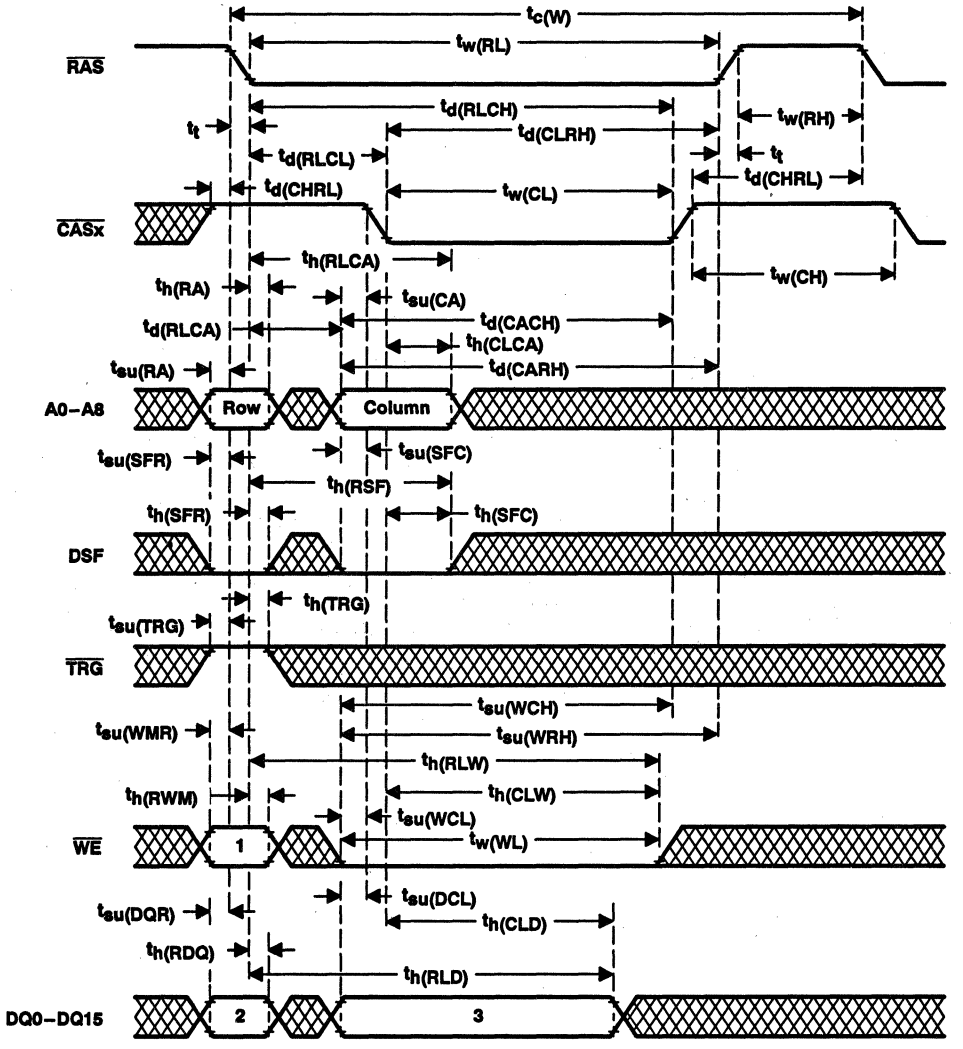


Figure 25. Early-Write-Cycle Timing

Table 6. Early-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

PARAMETER MEASUREMENT INFORMATION

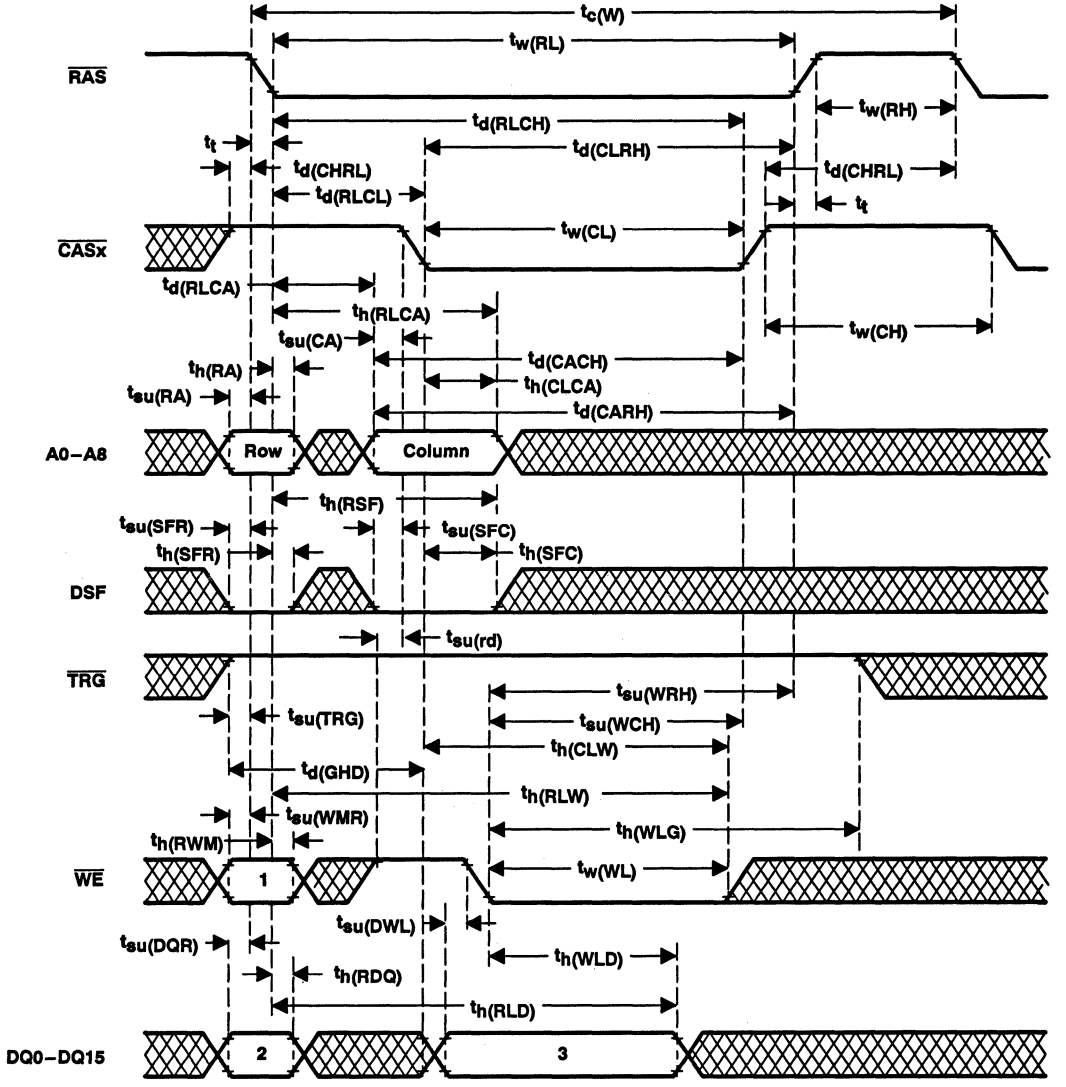
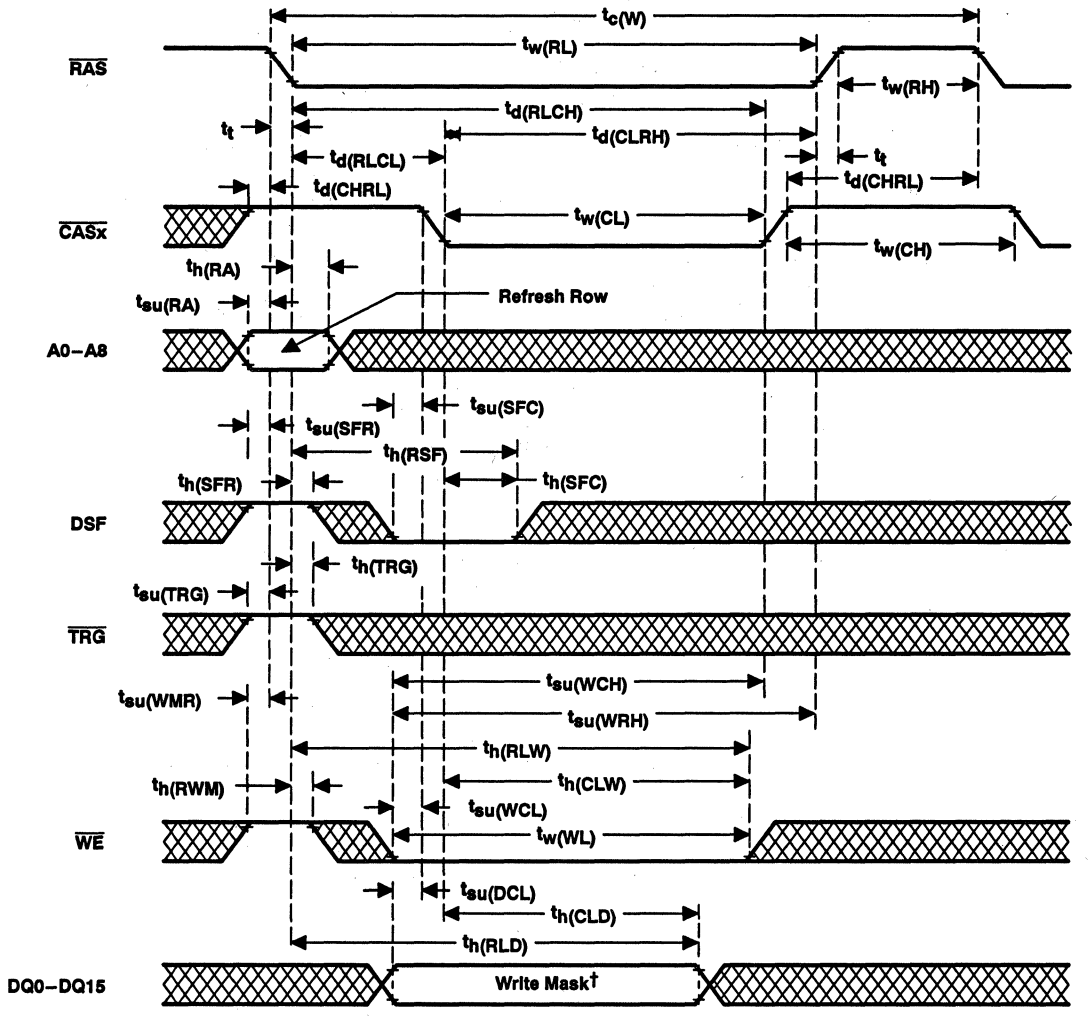


Figure 26. Late-Write-Cycle Timing (Output-Enable-Controlled Write)

Table 7. Late-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

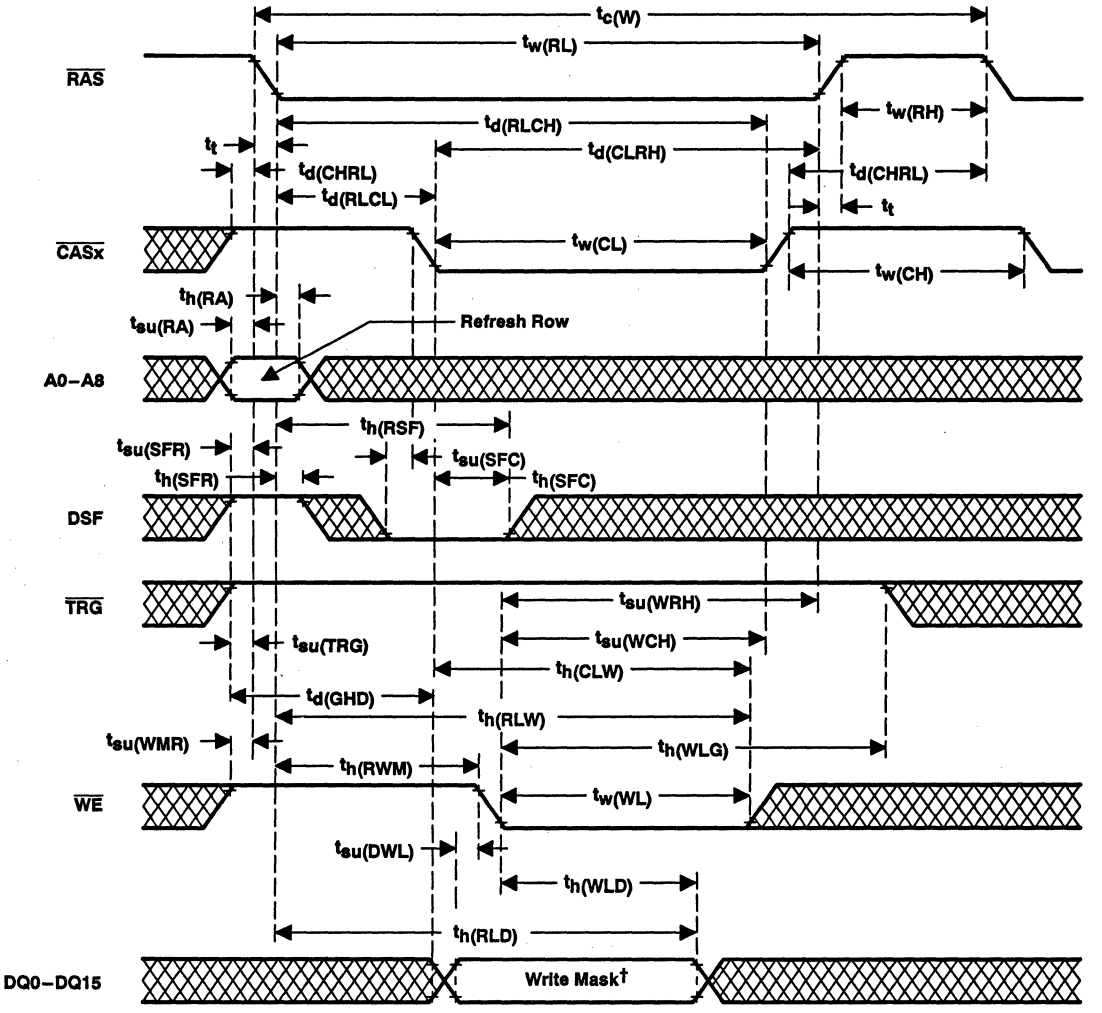
PARAMETER MEASUREMENT INFORMATION



† Load-write-mask-register cycle puts the device into the persistent write-per-bit mode.

Figure 27. Load-Write-Mask-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION



† Load-write-mask-register cycle puts the device into the persistent write-per-bit mode.

Figure 28. Load-Write-Mask-Register-Cycle Timing (Late-Write Load)

PARAMETER MEASUREMENT INFORMATION

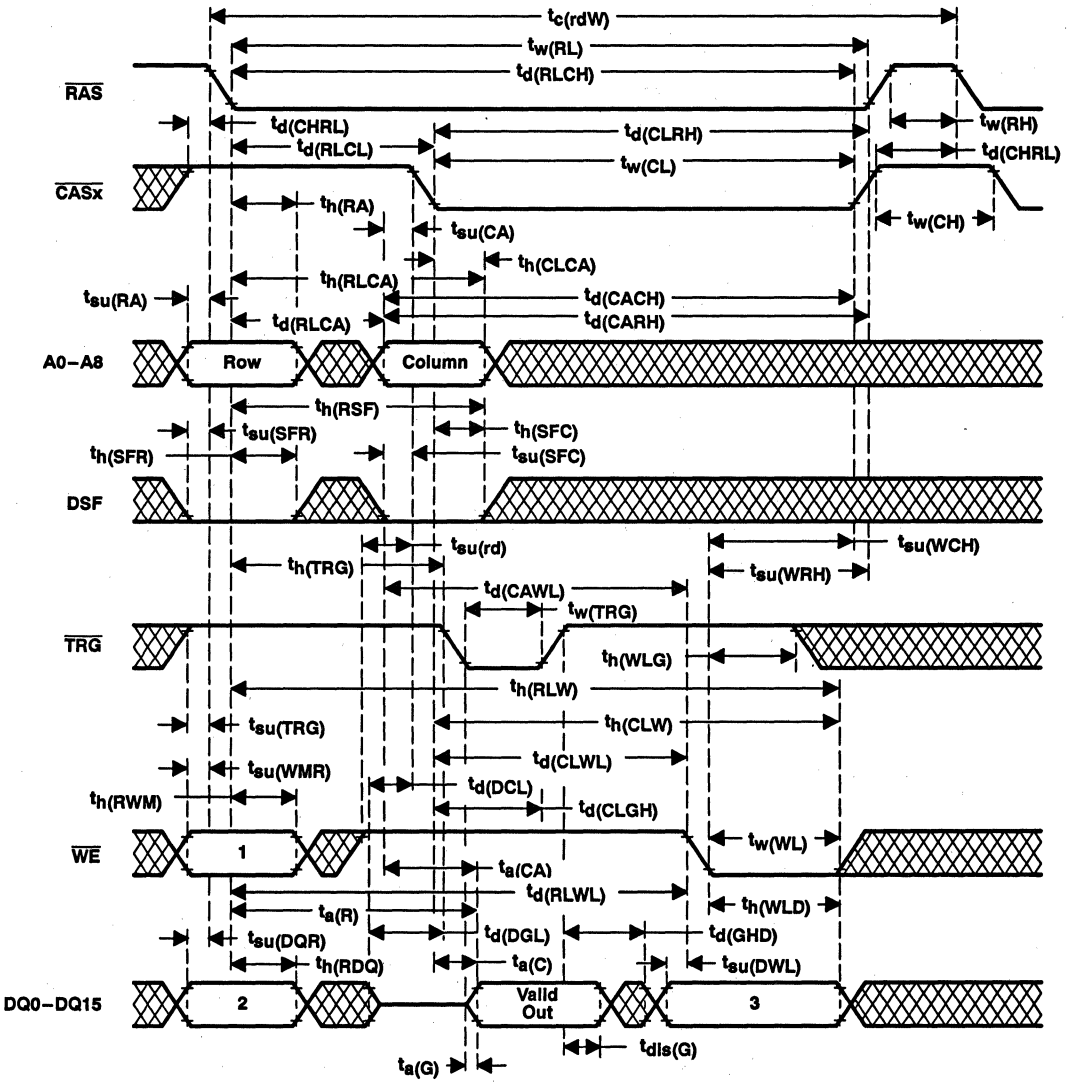
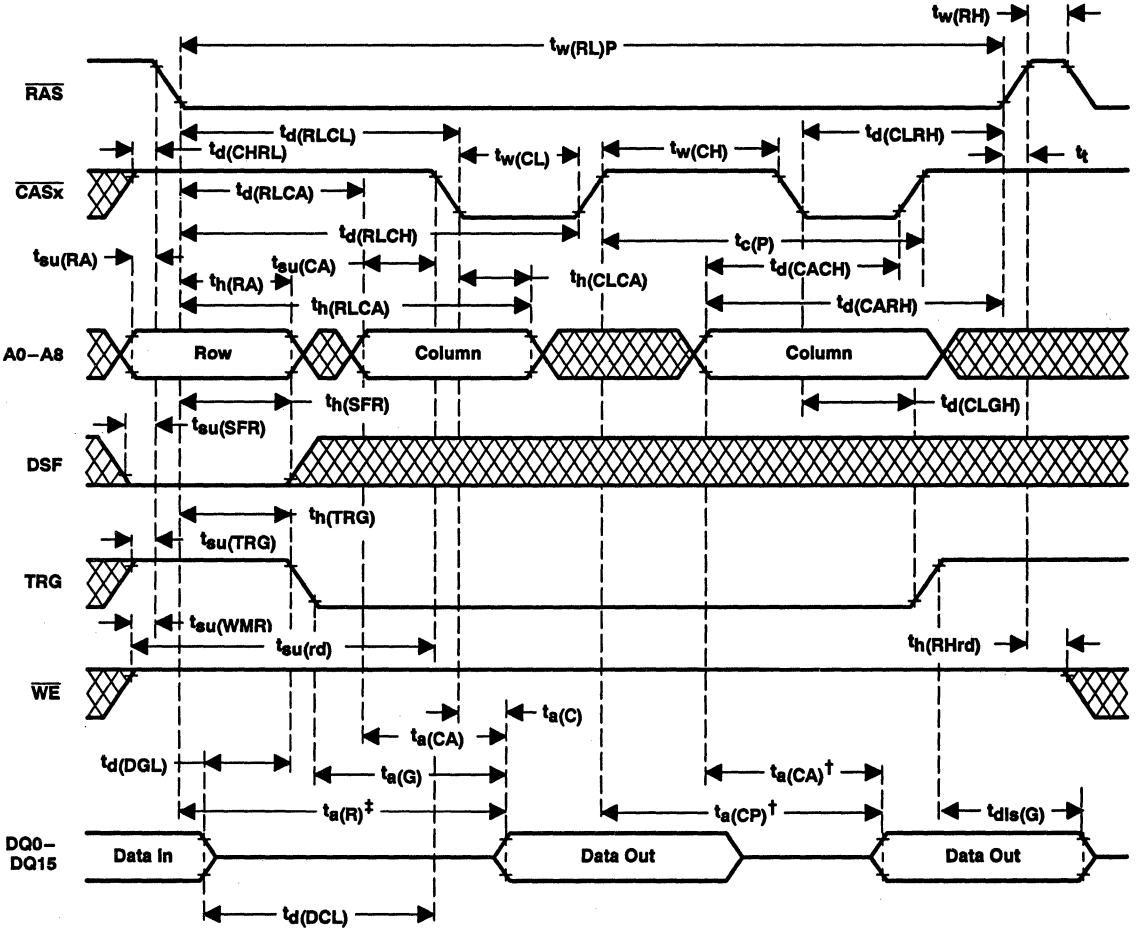


Figure 29. Read-Write-/Read-Modify-Write-Cycle Timing

Table 8. Read-Write-/Read-Modify-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

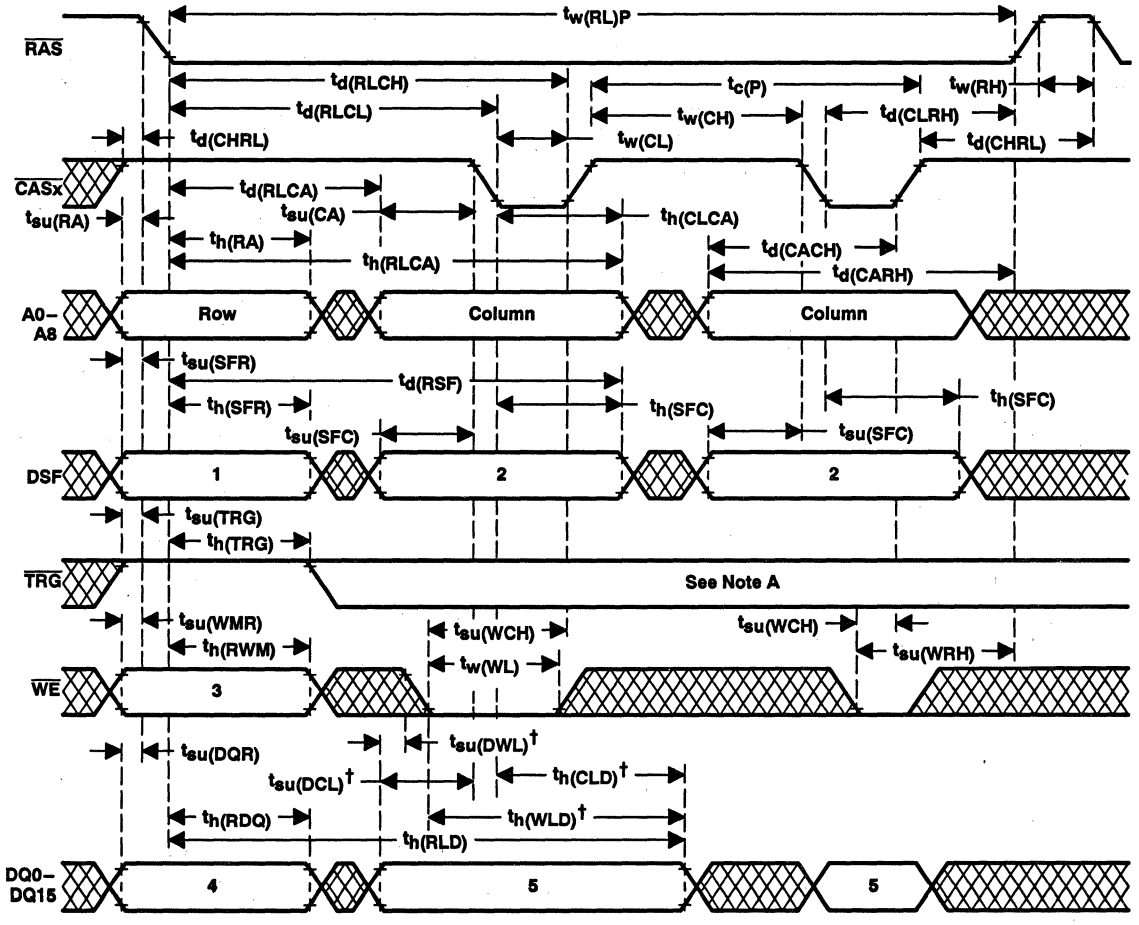
PARAMETER MEASUREMENT INFORMATION



† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output can go from the high-impedance state to an invalid data state prior to the specified access time.
NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CASx}$ to select the desired write mode (normal, block write, etc.).

Figure 30. Enhanced-Page-Mode Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later

NOTE A: A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late-write feature is used. If the early-write-cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

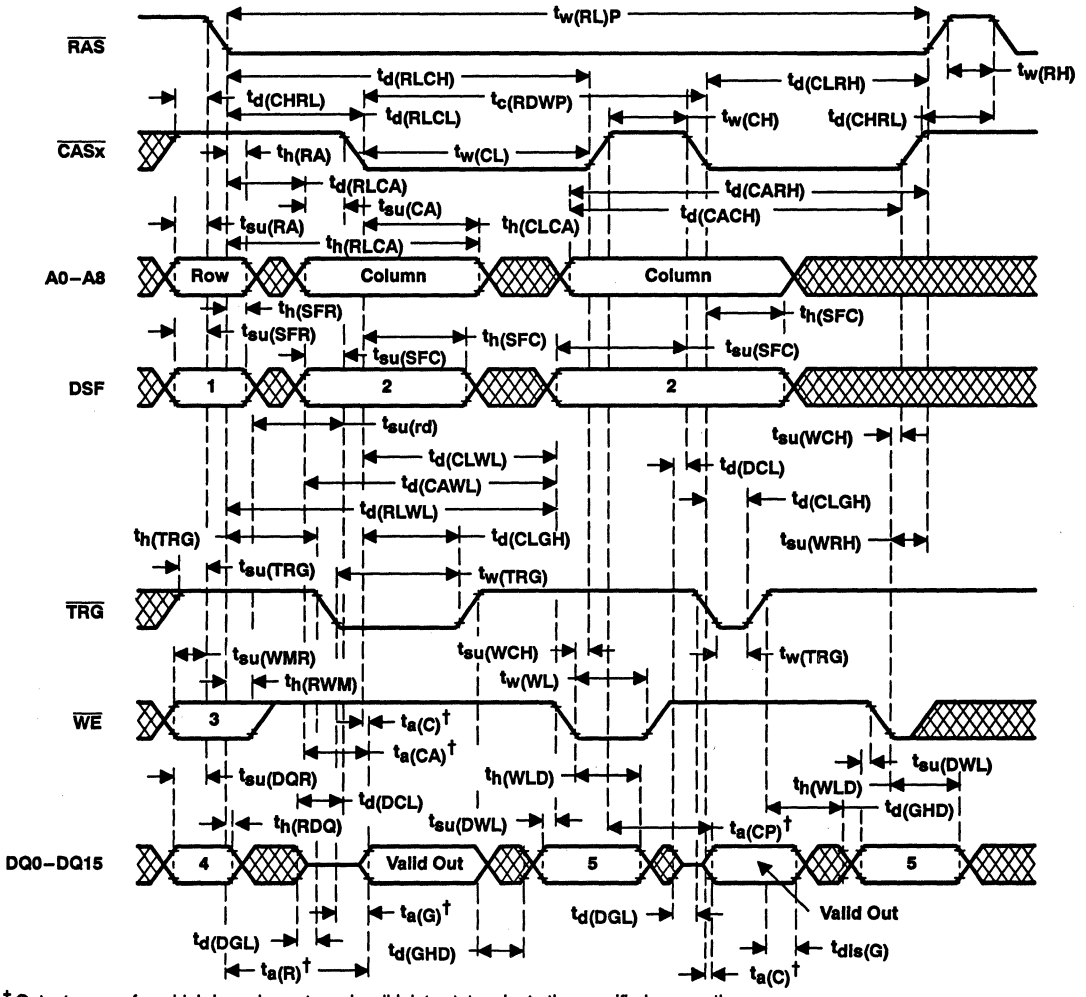
Figure 31. Enhanced-Page-Mode Write-Cycle Timing

Table 9. Enhanced Page-Mode Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load write-mask register on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load-write-mask-register cycle sets the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CASx}$ is a don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



† Output can go from high-impedance to an invalid data state prior to the specified access time.

NOTE A: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 32. Enhanced Page-Mode Read-Modify-Write-Cycle Timing

Table 10. Enhanced Page-Mode Read-Modify-Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load-write-mask register on either the first falling edge of CASx or the falling edge of WE, whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load-write-mask-register cycle sets the device to the persistent write-per-bit mode. Column address at the falling edge of CASx is a don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION

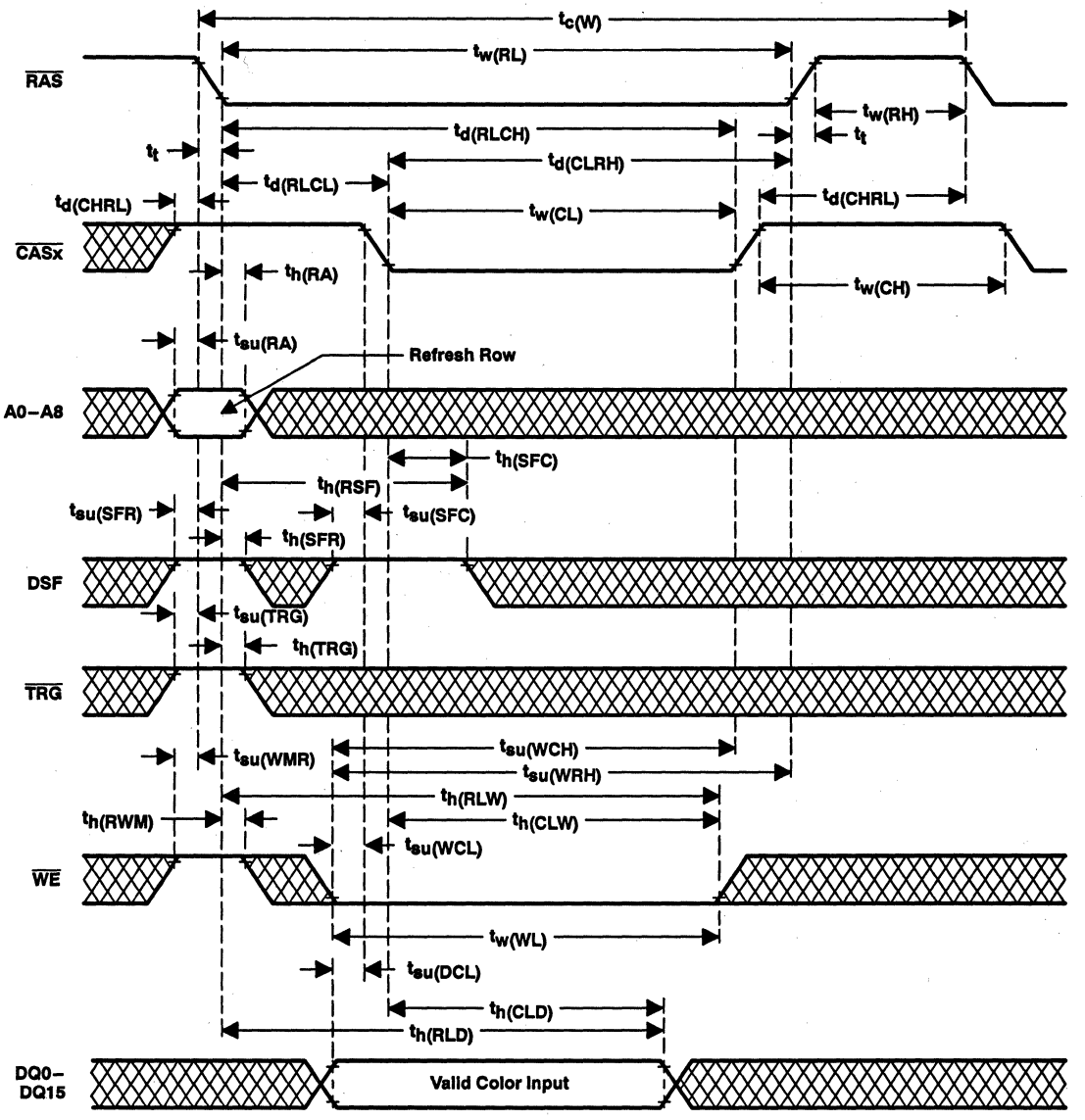


Figure 33. Load-Color-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION

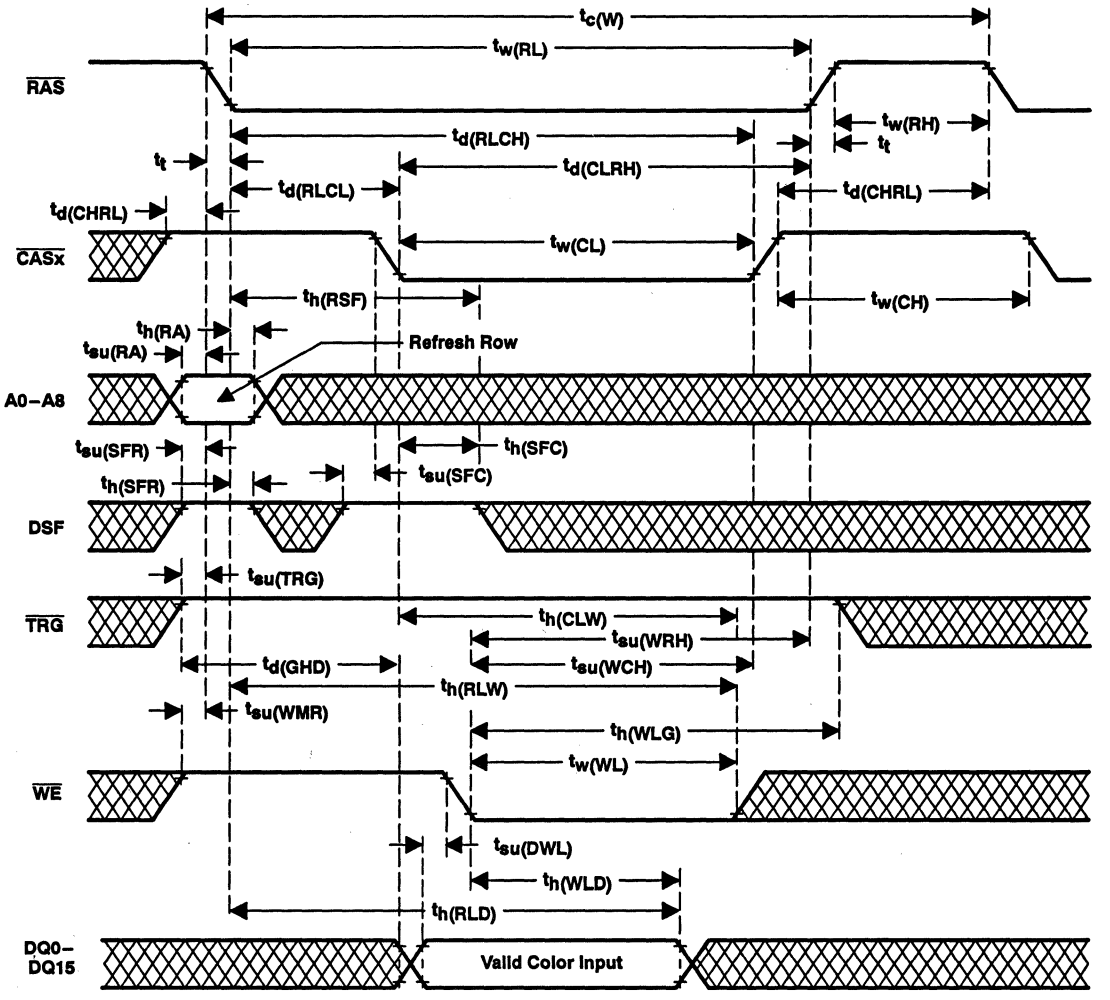


Figure 34. Load-Color-Register-Cycle Timing (Late-Write Load)

PARAMETER MEASUREMENT INFORMATION

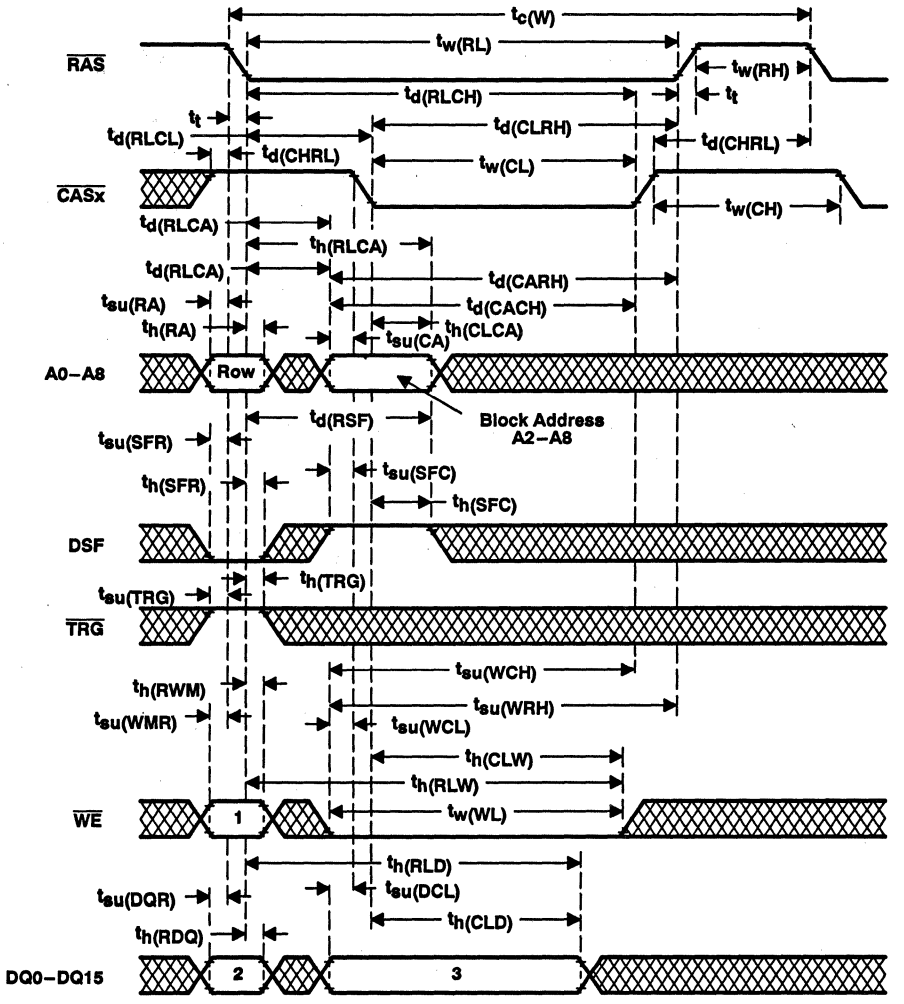


Figure 35. Block-Write-Cycle Timing (Early Write)

Table 11. Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi+3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

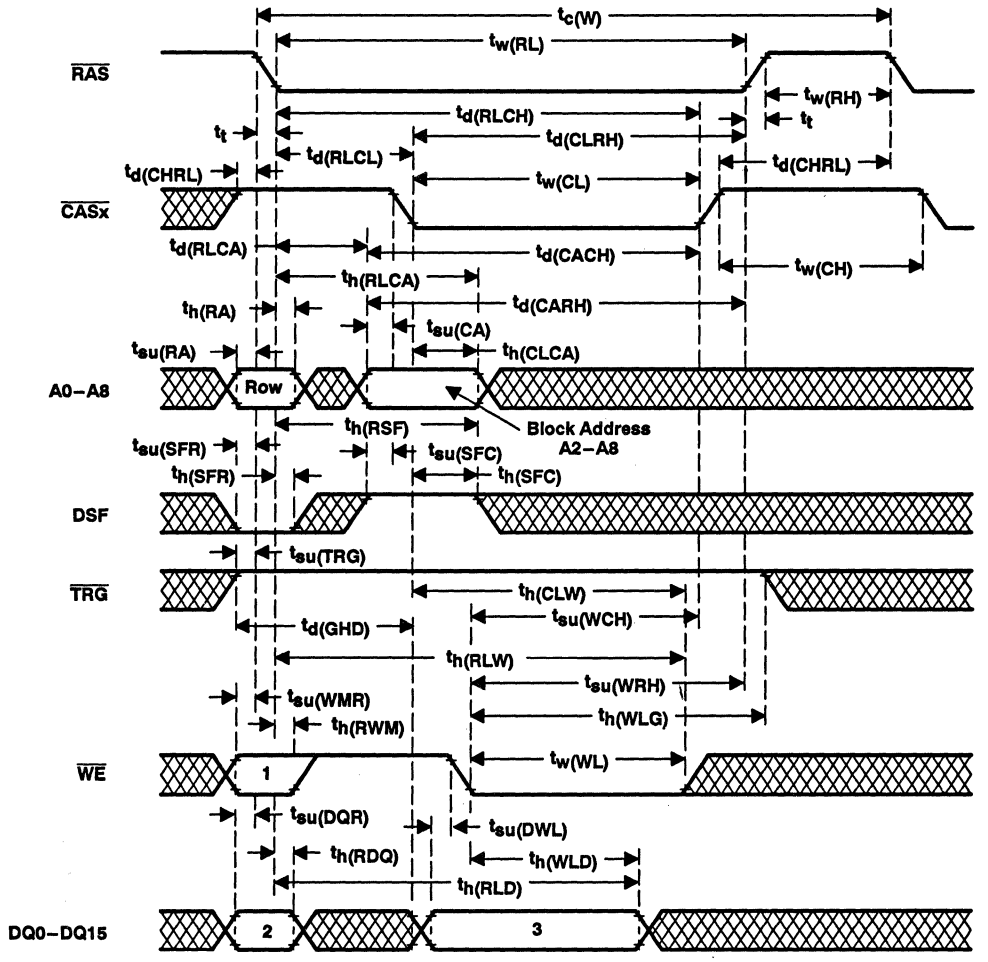


Figure 36. Block-Write-Cycle Timing (Late Write)

Table 12. Block-Write-Cycle State Table

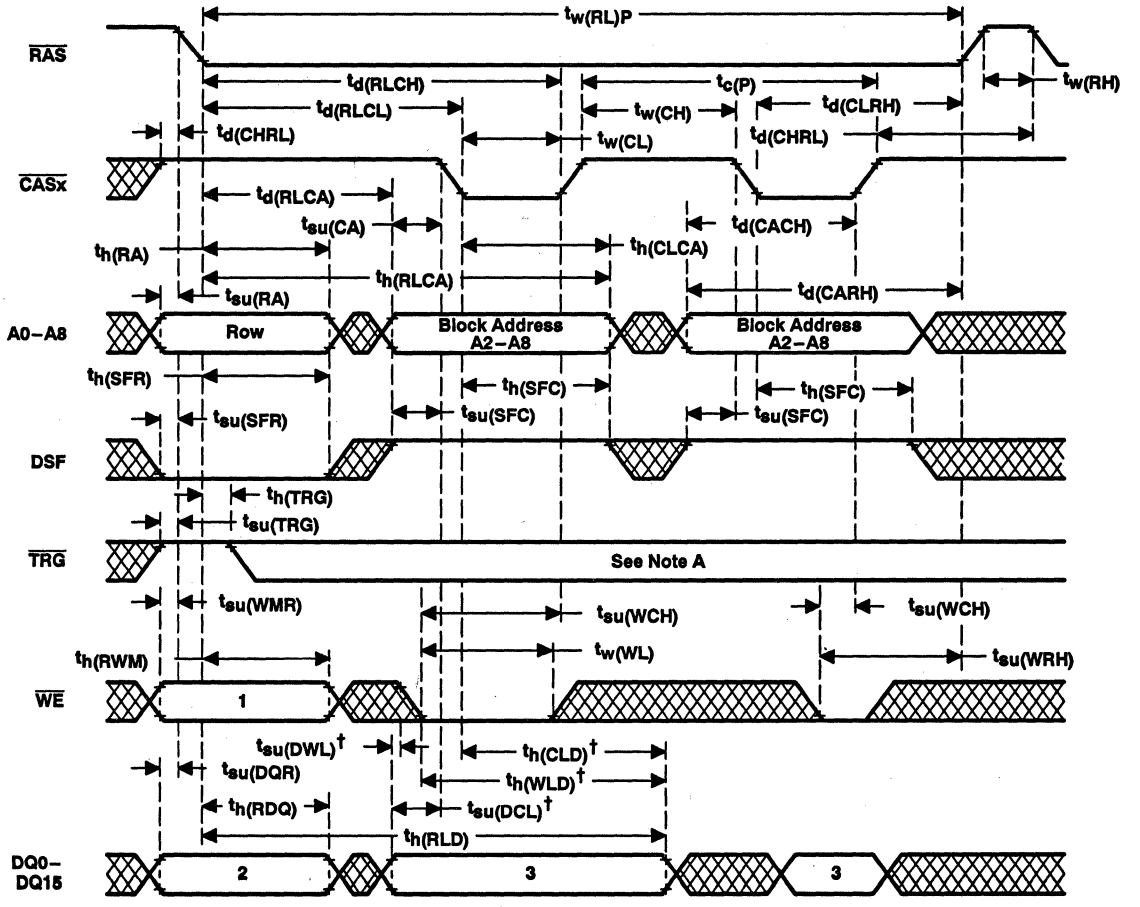
CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi+3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later

NOTE A: To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late-write feature is used. If the early-write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 37. Enhanced-Page-Mode Block-Write-Cycle Timing

Table 13. Enhanced-Page-Mode Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi+3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

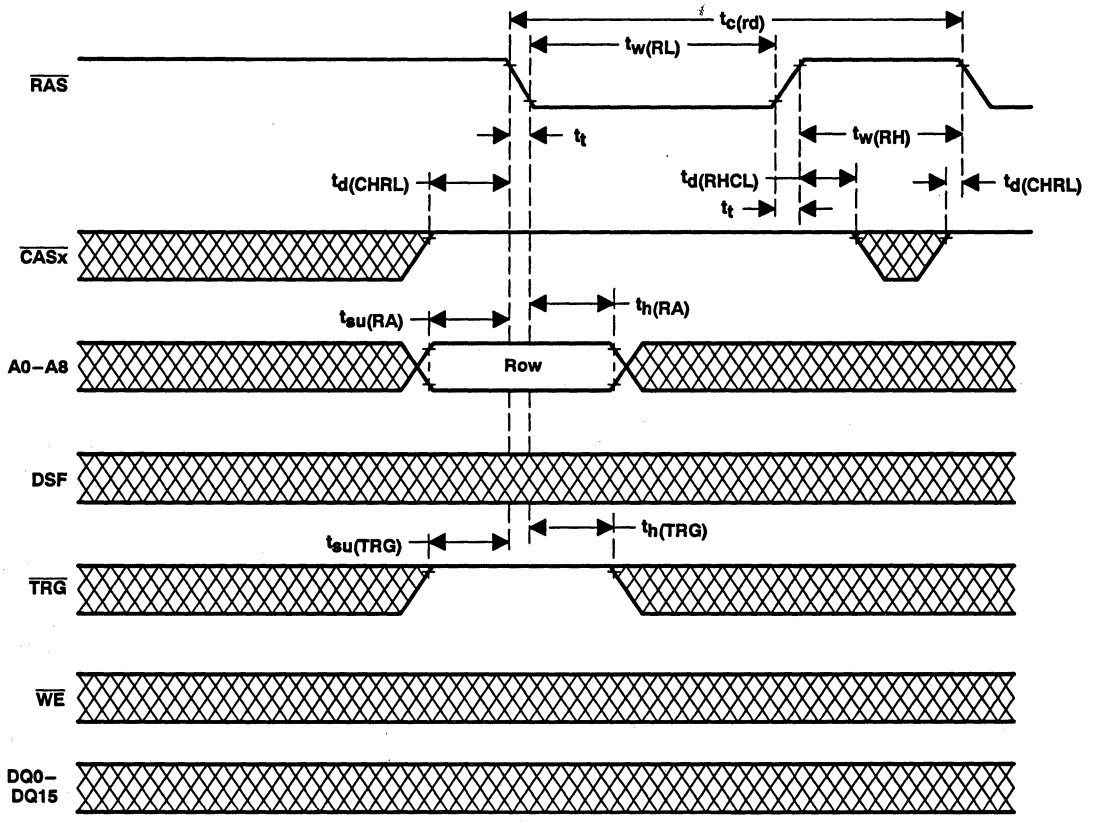


Figure 38. $\overline{RAS}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

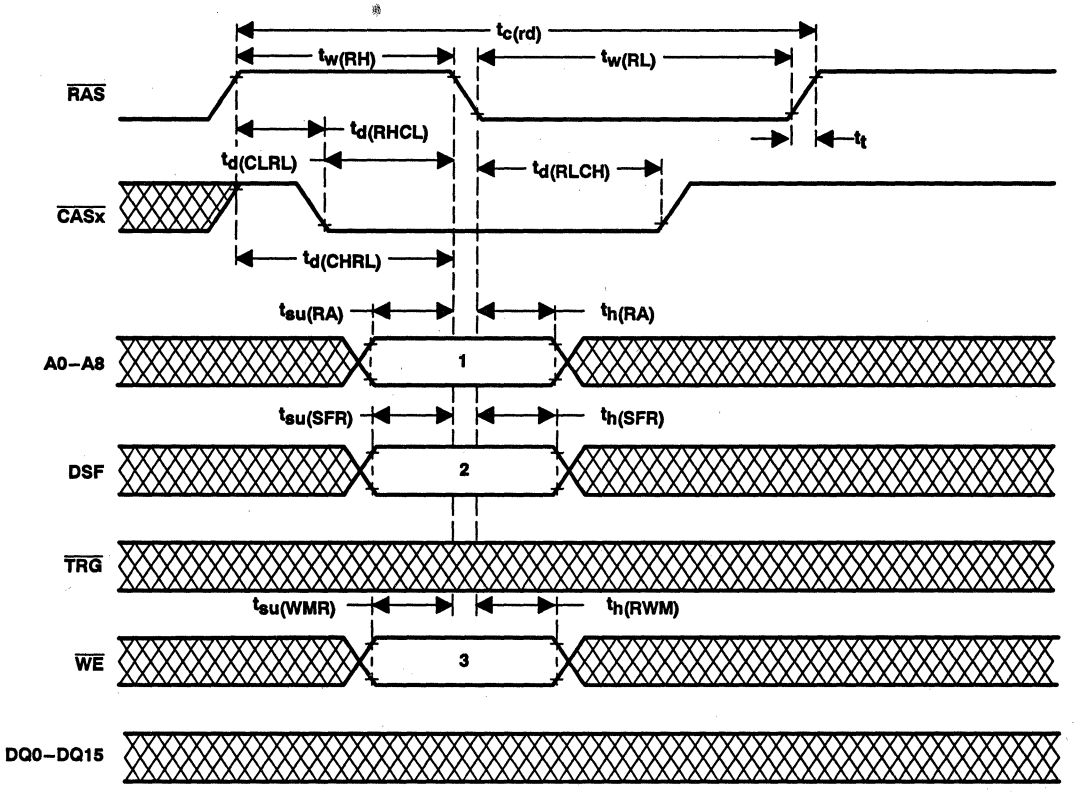


Figure 39. CBR-Refresh-Cycle Timing

Table 14. CBR-Cycle State Table

CYCLE	STATE		
	1	2	3
$\overline{\text{CBR}}$ refresh with option reset	Don't care	L	H
$\overline{\text{CBR}}$ refresh with no reset	Don't care	H	H
$\overline{\text{CBR}}$ refresh with stop point set and no reset	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION

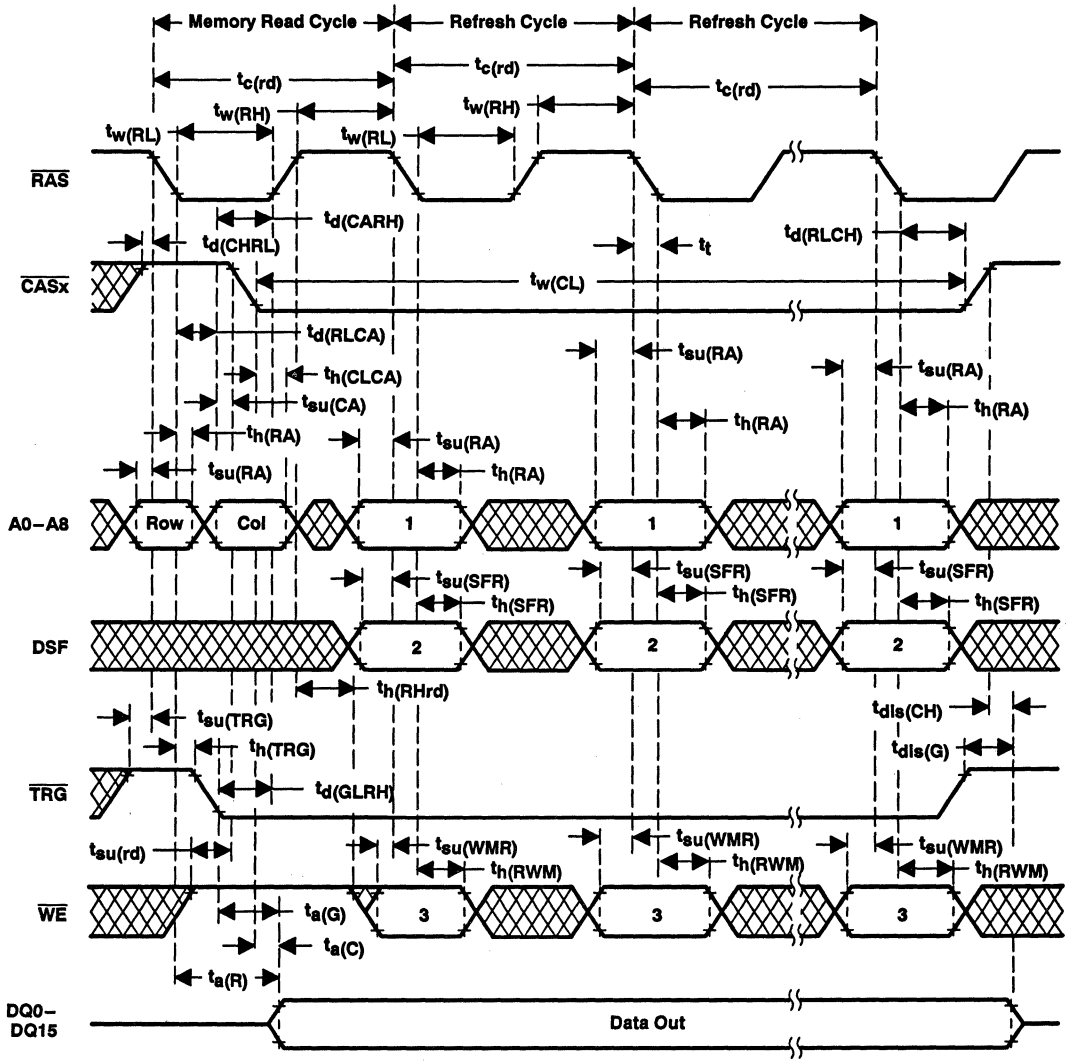
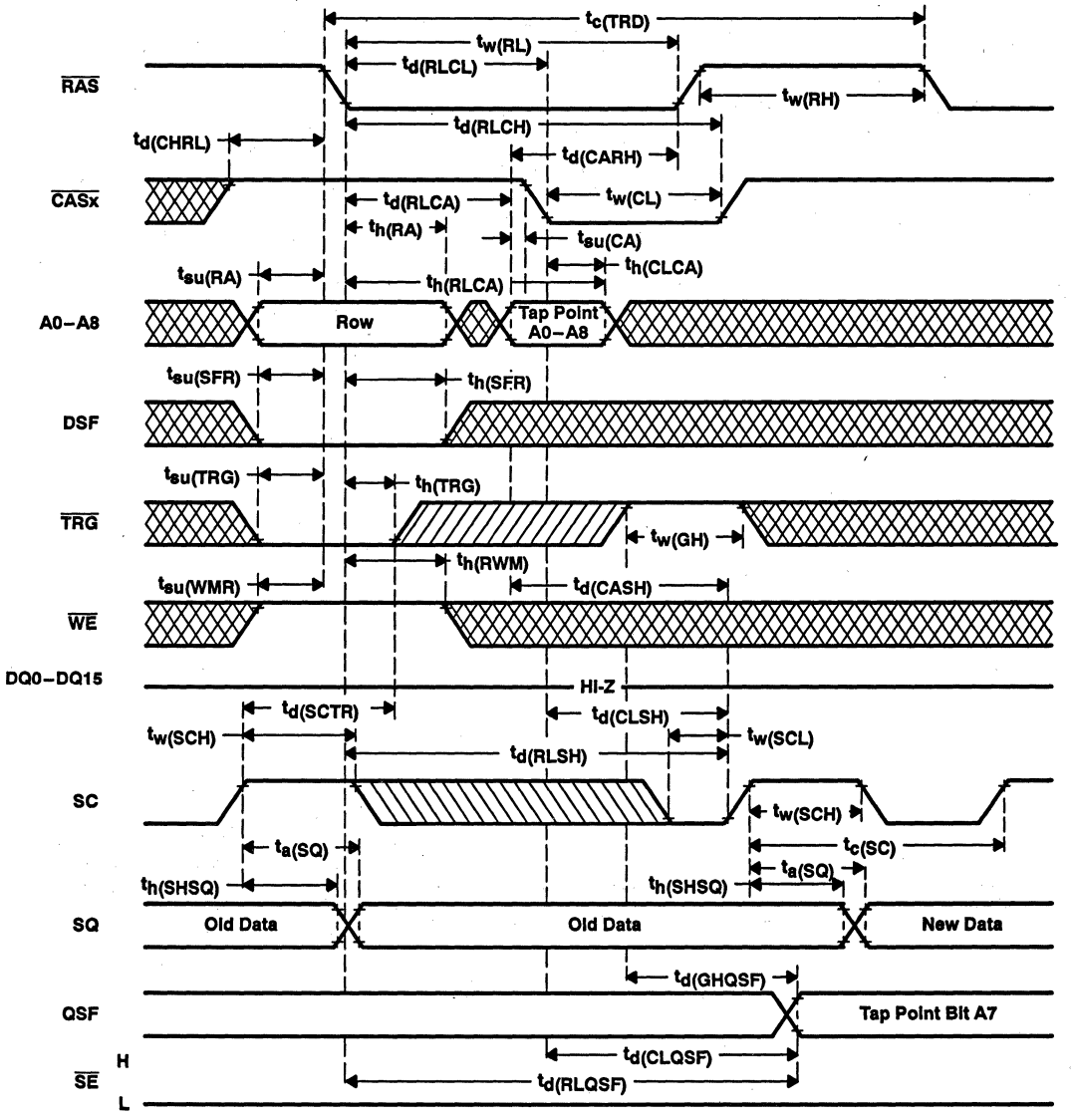


Figure 40. Hidden-Refresh-Cycle Timing

Table 15. Hidden-Refresh-Cycle State Table

CYCLE	STATE		
	1	2	3
$\overline{\text{CBR}}$ refresh with option reset	Don't care	L	H
$\overline{\text{CBR}}$ refresh with no reset	Don't care	H	H
$\overline{\text{CBR}}$ refresh with stop point set and no option reset	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register-transfer cycle. The memory-to-data-register-transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

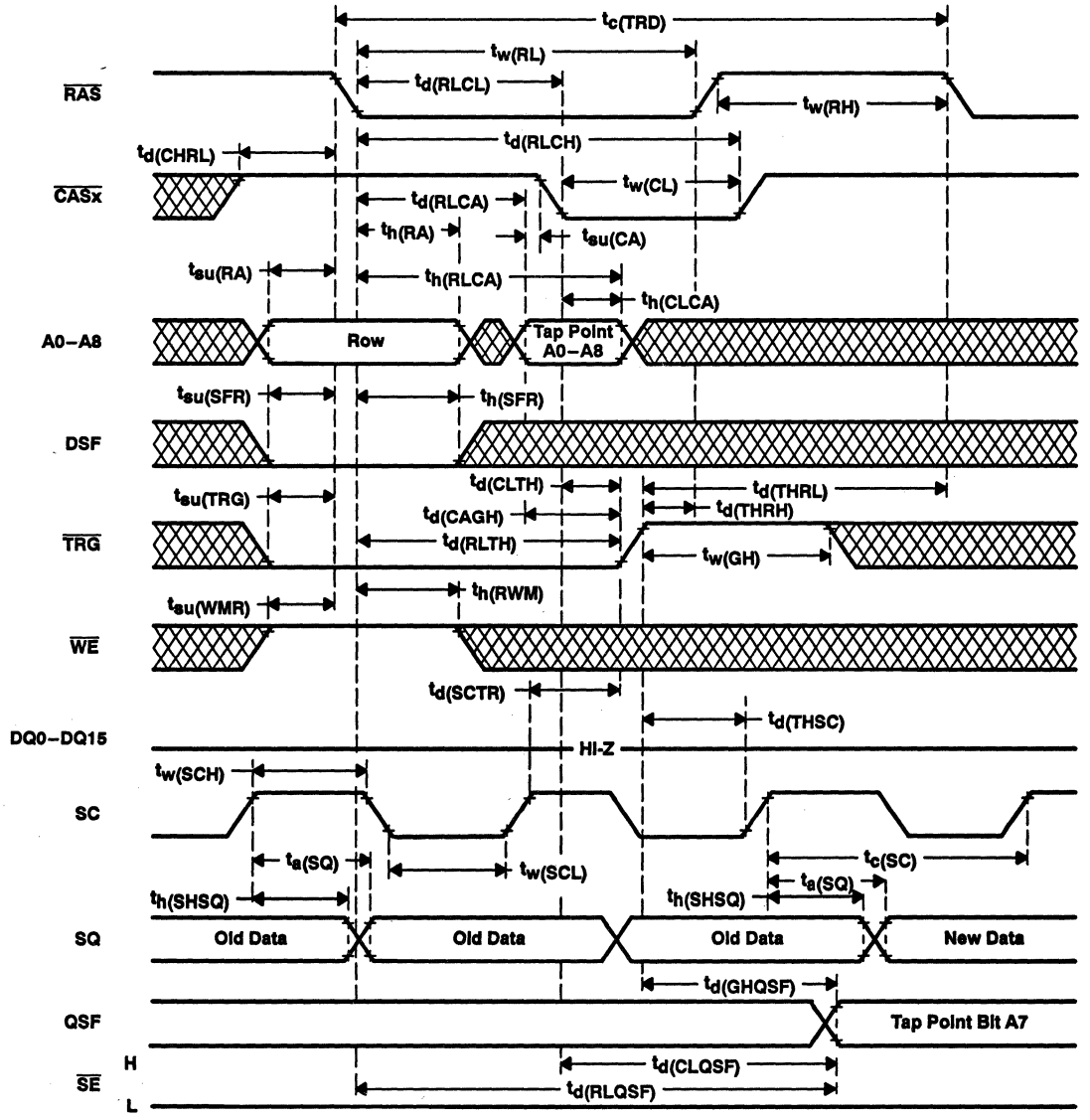
B. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0 – A7: register tap point; A8: identifies the half of the transferred row

D. Early-load operation is defined as $t_{h(TRG)}$ min < $t_{h(TRG)}$ < $t_{d(RLTH)}$ min.

Figure 41. Full-Register-Transfer Read Timing, Early-Load Operations

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Random-mode (DQ) outputs remain in the high-impedance state for the entire memory-to-data-register-transfer cycle. The memory-to-data-register-transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

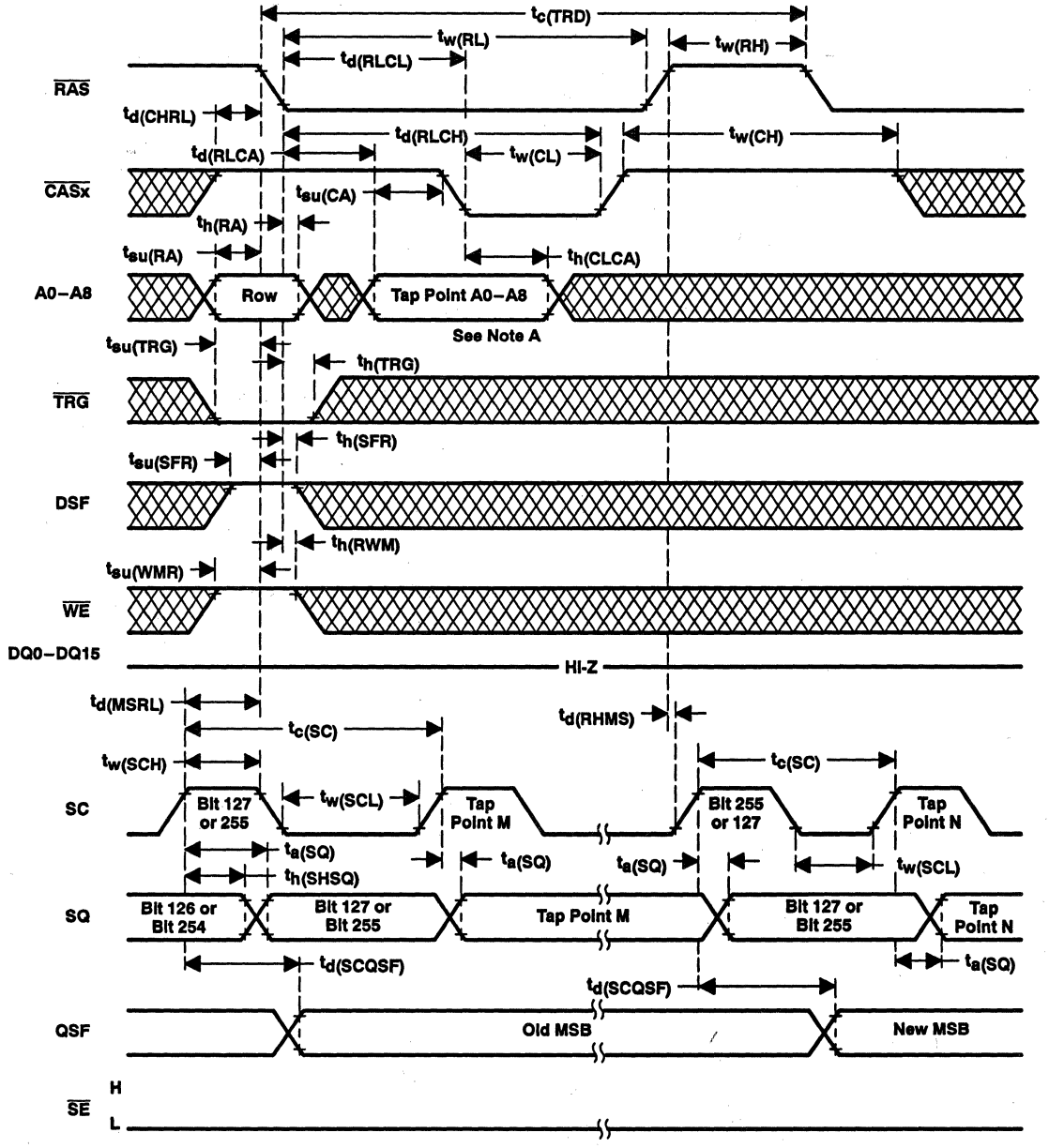
B. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0–A7: register tap point; A8: identifies the half of the transferred row

D. Late-load operation is defined as $t_{d(THRH)} < 0$ ns.

Figure 42. Full-Register-Transfer Read Timing, Real-Time Load Operation/Late-Load Operation

PARAMETER MEASUREMENT INFORMATION



NOTE A: A0–A6: tap point of the given half; A7: don't care; A8: identifies the DRAM row half

Figure 43. Split-Register-Transfer Read Timing

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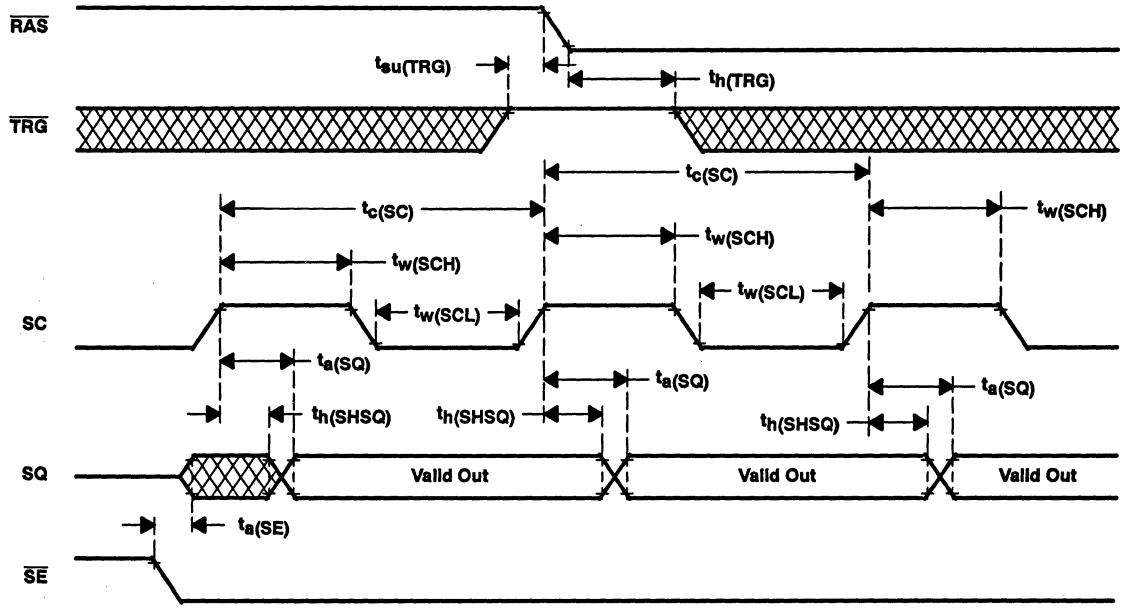
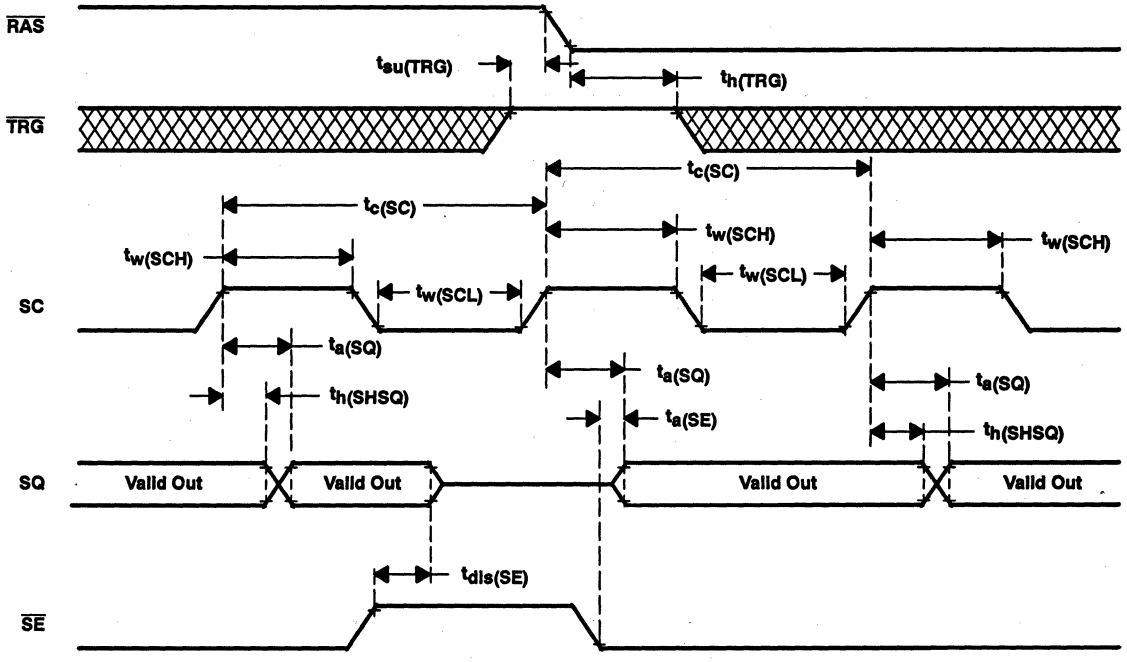
PARAMETER MEASUREMENT INFORMATION



NOTE A: While the data is being read through the serial-data register, $\overline{TRG}$ is a don't care except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

Figure 44. Serial-Read Timing ($\overline{SE}$ = V_{IL})

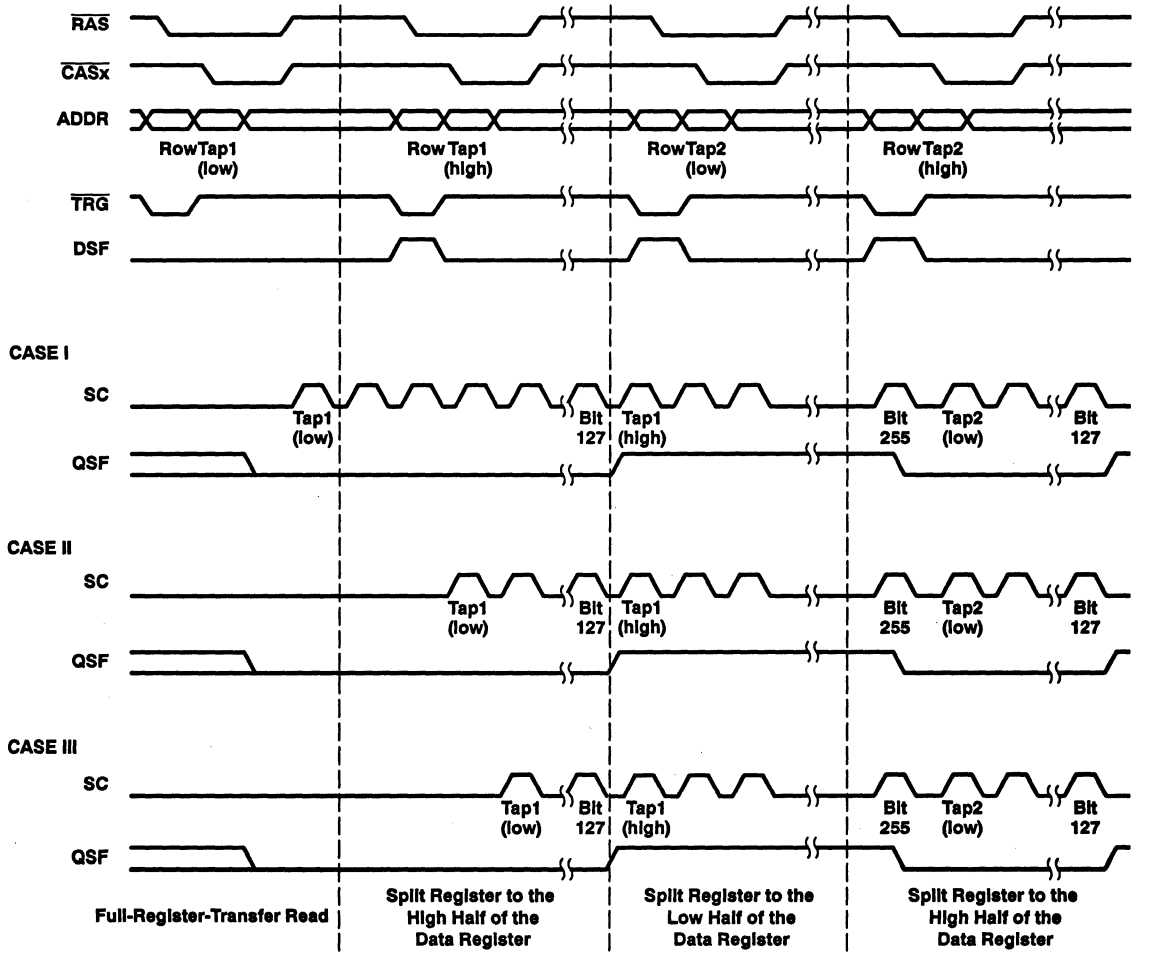
PARAMETER MEASUREMENT INFORMATION



NOTE A: While the data is being read through the serial-data register, $\overline{TRG}$ is a don't care except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

Figure 45. Serial-Read Timing ($\overline{SE}$-Controlled Read)

PARAMETER MEASUREMENT INFORMATION

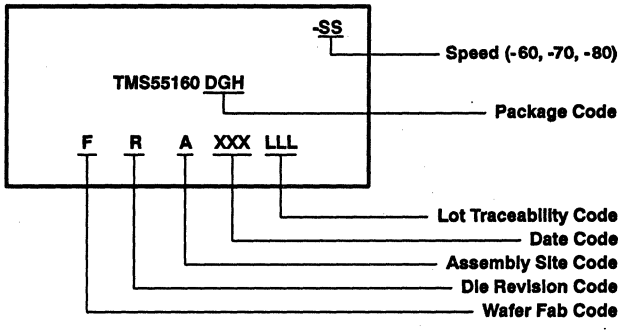


NOTES: A. In order to achieve proper split-register operation, a full-register-transfer read should be performed before the first split-register-transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can then begin either after the full-register-transfer-read cycle (CASE I), during the first split-register-transfer cycle (CASE II), or even after the first split-register-transfer cycle (CASE III). There is no minimum requirement of SC clock between the full-register-transfer-read cycle and the first split-register cycle.

B. A split-register-transfer into the inactive half is not allowed until $t_{d(MSRL)}$ is met. $t_{d(MSRL)}$ is the minimum delay time between the rising edge of the serial clock of the last bit (bit 127 or 255) and the falling edge of $\overline{RAS}$ of the split-register-transfer cycle into the inactive half. After the $t_{d(MSRL)}$ requirement is met, the split-register-transfer into the inactive half must also satisfy the minimum $t_{d(RHMS)}$ requirement. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register-transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 127 or 255).

Figure 46. Split-Register Operating Sequence

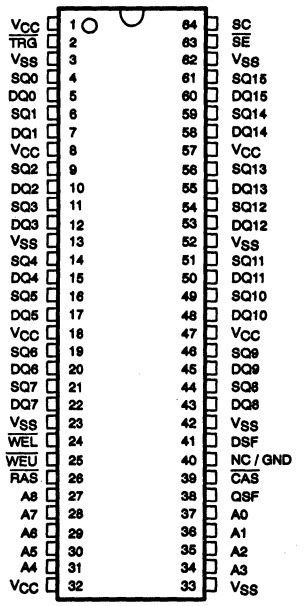
device symbolization



This data sheet is applicable to all TMS55165s symbolized with Revision "C" and subsequent revisions as described on page 5-189.

- **Organization:**
  - **DRAM : 262144 Words × 16 Bits**
  - **SAM: 256 Words × 16 Bits**
- **Dual-Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Data Transfer Function From the DRAM to the Serial Data Register**
- **(4 × 4) × 4 Block-Write Feature for Fast Area Fill Operations; As Many as Four Memory Address Locations Written Per Cycle From the 16-Bit On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O; Two Write-Per-Bit Modes to Simplify System Design**
- **Byte Write Control ($\overline{WEL}$, $\overline{WEU}$) Provides Flexibility**
- **Enhanced Page-Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) and Hidden Refresh Modes**
- **Long Refresh Period**
  Every 8 ms (Max)
- **Up to 55-MHz Uninterrupted Serial Data Streams**
- **256 Selectable Serial-Register Starting Locations**
- **$\overline{SE}$-Controlled Register-Status QSF**
- **Split-Register Transfer Read for Simplified Real-Time Register Load**
- **Programmable Split-Register Stop Point**
- **3-State Serial Outputs Allow Easy Multiplexing of Video Data Streams**
- **All Inputs/Outputs and Clocks TTL Compatible**
- **Compatible With JEDEC Standards**
- **Texas Instruments EPIC™ CMOS Process**
- **Designed to Work With the Industry-Leading Texas Instruments Graphics Family**
- **Performance Ranges:**

DGH PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ15	DRAM Data I/O, Write Mask Data
DSF	Special Function Select
NC/GND	No Connect/Ground (Important: Not connected internally to V_{SS})
QSF	Special Function Output
$\overline{RAS}$	Row-Address Strobe
SC	Serial Clock
$\overline{SE}$	Serial Enable
SQ0–SQ15	Serial Data Output
$\overline{TRG}$	Output Enable, Transfer Select
V_{CC}	5-V Supply (TYP)
V_{SS}	Ground
$\overline{WEL}$, $\overline{WEU}$	DRAM Byte-Write Enable Selects

	ACCESS TIME ROW ENABLE $t_{a(R)}$ (MAX)	ACCESS TIME SERIAL DATA $t_{a(SQ)}$ (MAX)	DRAM CYCLE TIME $t_{c(W)}$ (MIN)	DRAM PAGE MODE $t_{c(P)}$ (MIN)	SERIAL CYCLE TIME $t_{c(SC)}$ (MIN)	OPERATING CURRENT SERIAL PORT STANDBY I_{CC1} (MAX)	OPERATING CURRENT SERIAL PORT ACTIVE I_{CC1A} (MAX)
TMS55165-60	60 ns	15 ns	110 ns	35 ns	18 ns	180 mA	225 mA
TMS55165-70	70 ns	20 ns	130 ns	40 ns	22 ns	165 mA	205 mA
TMS55165-80	80 ns	25 ns	150 ns	45 ns	30 ns	150 mA	185 mA

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description

The TMS55165 multiport video RAM is a high-speed dual-ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 16 bits each interfaced to a serial data register [serial-access memory (SAM)] organized as 256 words of 16 bits each. The TMS55165 supports three basic types of operation: random access to and from the DRAM, serial access from the serial register, and transfer of data from any row in the DRAM to the serial register. Except during transfer operations, the TMS55165 can be accessed simultaneously and asynchronously from the DRAM and SAM ports.

The TMS55165 is equipped with several features designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's (4 × 4) × 4 block-write feature. The block-write mode allows 16 bits of data (present in an on-chip color data register) to be written to any combination of four adjacent column address locations. As many as 64 bits of data can be written to memory during each $\overline{CAS}$ cycle time. Also on the DRAM port, a write mask or a write-per-bit feature allows masking of any combination of the 16 inputs/outputs on any write cycle. The persistent write-per-bit feature uses a mask register that, once loaded, can be used on subsequent write cycles without reloading. The TMS55165 also offers byte control. Byte control can be applied in write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles.

The TMS55165 offers a split-register-transfer read (DRAM to SAM) feature for the serial register (SAM port). This feature enables real-time register load implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. For applications not requiring real-time register load (for example, loads done during CRT retrace periods), the full-register mode of operation is retained to simplify system design.

The SAM port is designed for maximum performance. Data can be accessed from the SAM at serial rates up to 55 MHz. During the split-register-transfer read operations, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, QSF, is included to indicate which half of the serial register is active.

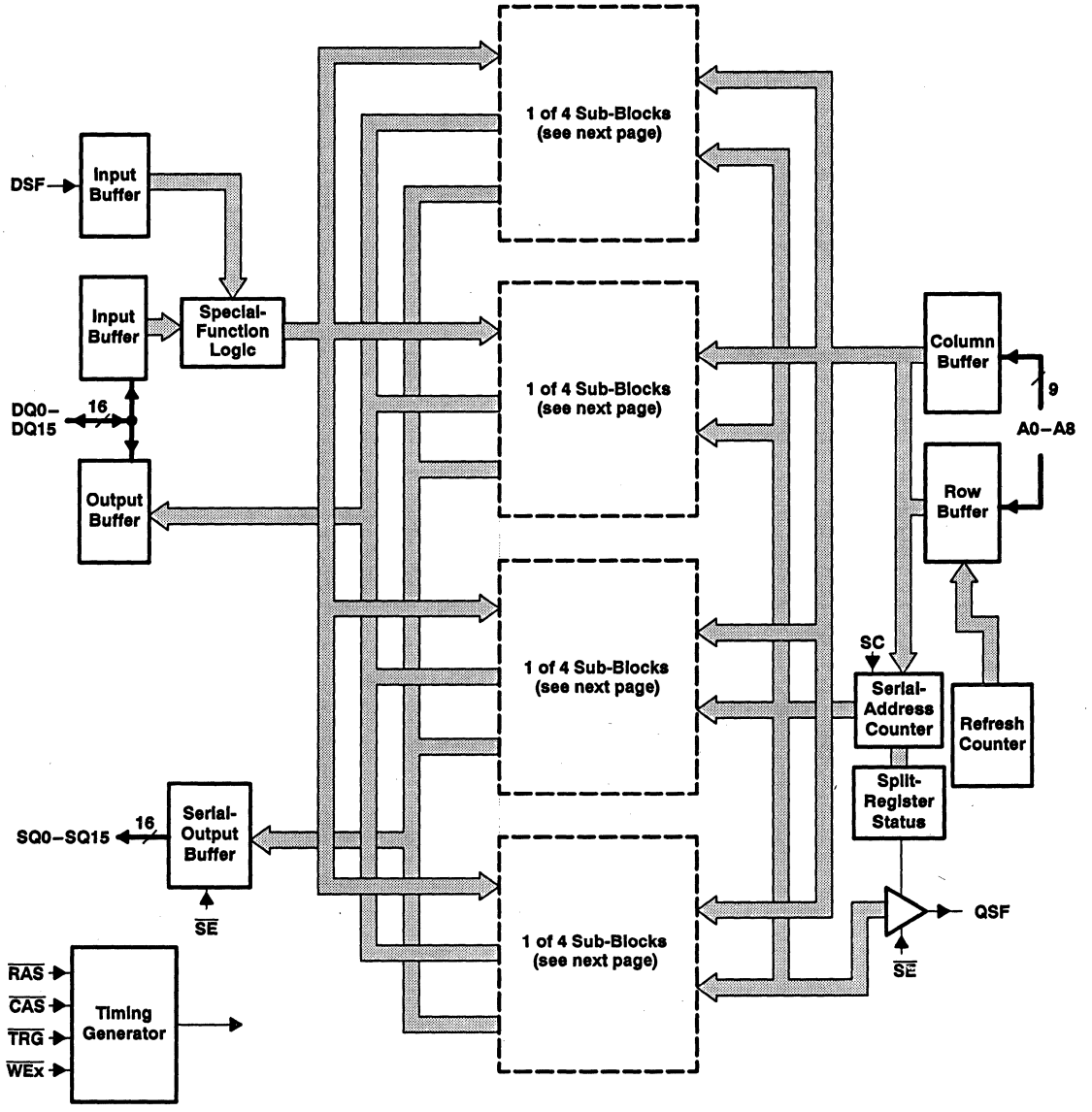
All inputs, outputs, and clock signals on the TMS55165 are compatible with Series 74 TTL. All address lines and data-in lines are latched on chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

The TMS55165 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The TMS55165 is offered in a 64-pin small-outline gull-wing-leaded package (DGH suffix) for direct surface mounting.

The TMS55165 and other TI multiport video RAMs are supported by a broad line of graphics processors and control devices from Texas Instruments.

functional block diagram



functional block diagram (continued)

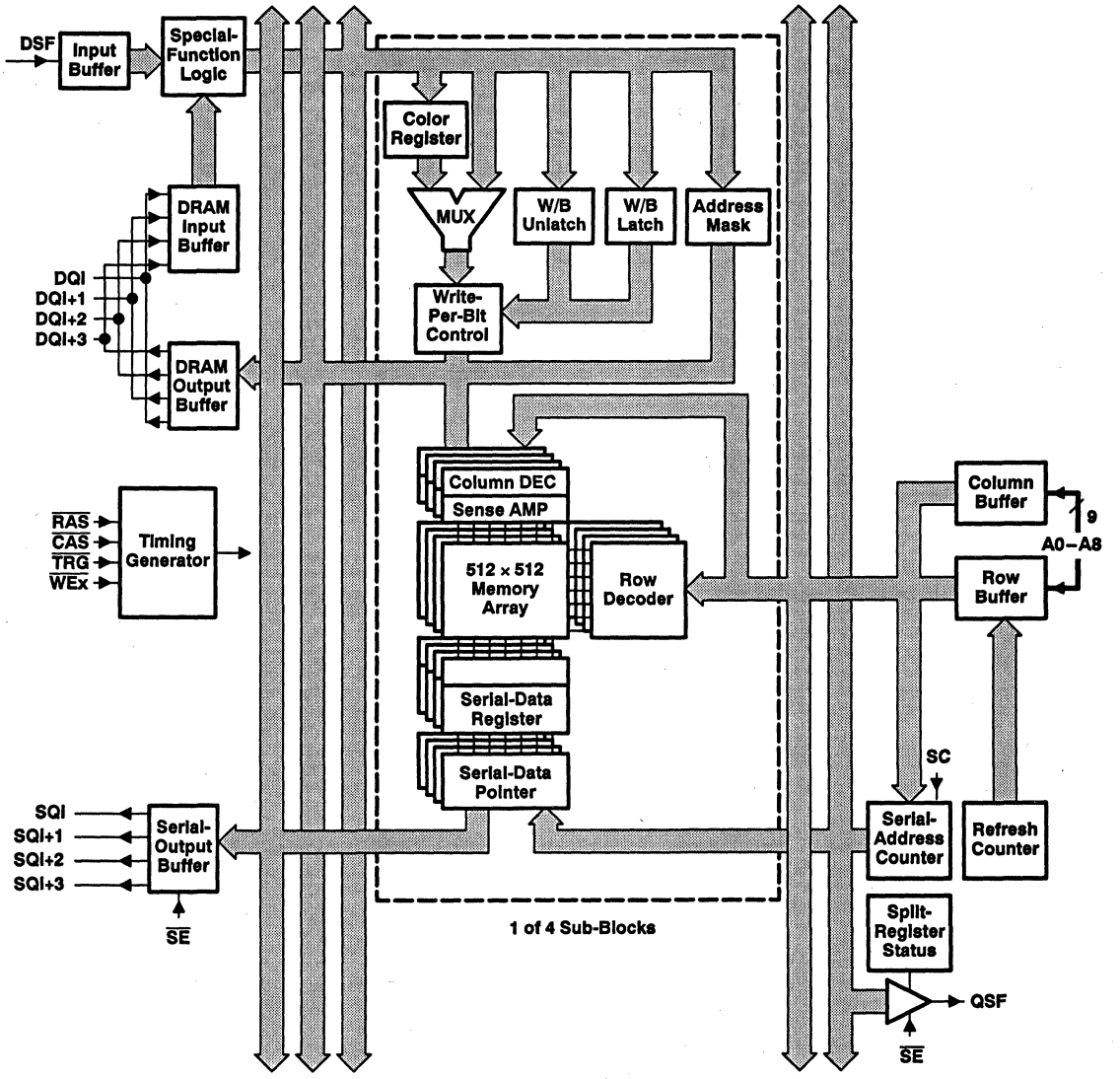


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Table 1. Function Table

FUNCTION	RAS FALL				CAS FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CAS	TRG	WEx‡	DSF	DSF	RAS	CAS§	RAS	WEL WEU CAS	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop point set ¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)★	L	X	H	H	X	X	X	X	X	CBRN
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
Load write-mask register □	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
X = Don't care
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled

† DQ0–DQ15 are latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later.
‡ Logic L is selected when either or both $\overline{WEL}$ and $\overline{WEU}$ are low.
§ The column address and block address are latched on the falling edge of $\overline{CAS}$.
¶ CBRS cycle should be performed immediately after the power-up initialization cycle.
# A0–A3, A8: don't care; A4–A7: stop-point code
‖ CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
★ CBR refresh (no reset) mode does not end persistent write-per-bit mode or stop-point mode.
□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.

Table 2. Pin Description Versus Operational Mode

PIN	DRAM	TRANSFER	SAM
A0–A8	Row, column address	Row address, tap point	
$\overline{CAS}$	Column-address strobe, DQ output enable	Tap-address strobe	
DQ	DRAM data I/O, Write mask		
DSF	Block-write enable Write-mask-register load enable Color-register load enable CBR (option reset)	Split-register-transfer enable	
$\overline{RAS}$	Row-address strobe	Row-address strobe	
$\overline{SE}$			SQ output enable, QSF output enable
SC			Serial clock
SQ			Serial-data output
$\overline{TRG}$	DQ output enable	Transfer enable	
$\overline{WEL}$ $\overline{WEU}$	Write enable, Write-per-bit enable		
QSF			Serial-register status
NC/GND	Make no external connection or tie to system GND		
V_{CC}†	5-V supply		
V_{SS}†	Ground		

† For proper device operation, all V_{CC} pins must be connected to a 5-V supply, and all V_{SS} pins must be tied to ground.

pin definitions

address (A0–A8)

Eighteen address bits are required to decode one of 262144 storage cell locations. Nine row-address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Nine column-address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and the falling edge of $\overline{CAS}$.

During the full-register-transfer read operation, the states of A0–A8 are latched on the falling edge of $\overline{RAS}$ to select one of the 512 rows where the transfer occurs. At the falling edge of $\overline{CAS}$, the column-address bits A0–A8 are latched. The most significant column-address bit (A8) selects which half of the row is transferred to the SAM. The appropriate 8-bit column address (A0–A7) selects one of 256 tap points (starting positions) for the serial data output.

During the split-register-transfer read operation, address bit A7 is ignored at the falling edge of $\overline{CAS}$. An internal counter selects which half of the register is used. If the high half of the SAM is currently in use, the low half of the SAM is loaded with the low half of the DRAM half row, and vice versa. Column address (A8) selects the DRAM half row. The remaining seven address bits (A0–A6) are used to select 1 of 127 possible starting locations within the SAM. Locations 127 and 255 are not valid tap points.

row-address strobe ($\overline{RAS}$)

$\overline{RAS}$ is similar to a chip enable, so that all DRAM cycles and transfer cycles are initiated by the falling edge of $\overline{RAS}$. $\overline{RAS}$ is a control input that latches the states of the row address, $\overline{WEL}$, $\overline{WEU}$, $\overline{TRG}$, $\overline{CAS}$, and DSF onto the chip to invoke DRAM and transfer functions of the TMS55165.

column-address strobe ($\overline{CAS}$)

$\overline{CAS}$ is a control input that latches the states of the column address and DSF to control DRAM and transfer functions of the TMS55165. $\overline{CAS}$ also acts as output enable for the DRAM output pins DQ0–DQ15.

In transfer operations, address bits A0–A8 are latched at the falling edge of $\overline{CAS}$ as the start position (tap) for the serial data output (SQ0–SQ15).

output enable/transfer select ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either DRAM or transfer operation as $\overline{RAS}$ falls. For DRAM operation, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. During DRAM operation, $\overline{TRG}$ functions as an output enable for the DRAM output pins DQ0–DQ15. For transfer operation, $\overline{TRG}$ must be brought low before $\overline{RAS}$ falls.

write mask select, write enable ($\overline{WEL}$, $\overline{WEU}$)

In DRAM operation, $\overline{WEL}$ enables data to be written to the lower byte (DQ0–DQ7) and $\overline{WEU}$ enables data to be written to the upper byte (DQ8–DQ15) of the DRAM. Both $\overline{WEL}$ and $\overline{WEU}$ have to be held high together to select the read mode. Bringing either or both $\overline{WEL}$ and $\overline{WEU}$ low selects the write mode.

$\overline{WEL}$ and $\overline{WEU}$ are also used to select the DRAM write-per-bit mode of operation. If either or both $\overline{WEL}$ and $\overline{WEU}$ are brought low on the falling edge of $\overline{RAS}$, the write-per-bit operation is invoked. The TMS55165 supports both the nonpersistent write-per-bit mode and the persistent write-per-bit mode.

special function select (DSF)

The DSF input is latched on the falling edge of $\overline{RAS}$ or $\overline{CAS}$, similar to an address. DSF determines which of the following functions are invoked on a particular cycle:

- CBR refresh with reset (CBR)
- CBR refresh with no reset (CBRN)
- CBR refresh with no reset and stop point set (CBRS)
- Block write
- Loading write-mask register for the persistent write-per-bit mode (LMR)
- Loading color register for the block-write mode
- Split-register-transfer read

DRAM data I/O, write mask data (DQ0–DQ15)

DRAM data is written or read through the common I/O DQ pins. The 3-state DQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state as long as either $\overline{TRG}$ or $\overline{CAS}$ is held high. Data is not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. The write mask is latched into the device via the random DQ pins by the falling edge of $\overline{RAS}$ and is used on all write-per-bit cycles. In a transfer operation, the DQ outputs remain in the high-impedance state for the entire cycle.

serial data outputs (SQ0–SQ15)

Serial data is read from the SQ pins. The SQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. The serial outputs are in the high-impedance (floating) state as long as the serial enable pin, $\overline{SE}$, is high. The serial outputs are enabled when $\overline{SE}$ is brought low.

serial clock (SC)

Serial data is accessed out of the data register from the rising edge of SC. The TMS55165 is designed to work with a wide range of clock duty cycles to simplify system design. There is no refresh requirement because the data registers that comprise the SAM are static. There is also no minimum SC clock operating frequency.

serial enable ($\overline{SE}$)

During serial access operations, $\overline{SE}$ is used as an enable/disable for the SQ outputs. $\overline{SE}$ low enables the serial data output. $\overline{SE}$ high disables the serial data output. $\overline{SE}$ is also used as an enable/disable for output pin QSF.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is not disabled. Thus, external SC pulses increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low because the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

special function output (QSF)

QSF is an output pin that indicates which half of the SAM is being accessed. When QSF is low, the serial address pointer is accessing the lower (least significant) 128 bits of the serial register (SAM). When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF changes state upon crossing a boundary between the two SAM halves.

During full-register-transfer operations, QSF can change state upon completing the cycle. This state is determined by the tap point loaded during the transfer cycle.

The QSF output is enabled by $\overline{SE}$. If $\overline{SE}$ is high, the QSF output is in the high-impedance state.

no connect/ground (NC/GND)

The NC/GND pin should be tied to system ground or left floating for proper device operation.

functional operation description

random access operation

Table 3. DRAM Function Table

FUNCTION	RAS FALL				CAS FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CAS	TRG	WEx‡	DSF	DSF	RAS	CAS§	RAS	WEL WEU CAS	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop-point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)★	L	X	H	H	X	X	X	X	X	CBRN
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
Load write-mask register □	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
X = Don't care
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled

† DQ0–DQ15 are latched on either the first falling edge of WEx or the falling edge of CAS, whichever occurs later.
‡ Logic L is selected when either or both WEL and WEU are low.
§ The column address and block address are latched on the falling edge of CAS.
¶ CBRS cycle should be performed immediately after the power-up initialization cycle.
# A0–A3, A8: don't care; A4–A7: stop-point code
‖ CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
★ CBR refresh (no reset) mode does not end persistent write-per-bit mode or stop-point mode.
□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.

enhanced page mode

Enhanced-page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. This mode eliminates the time required for row-address setup, row-address hold, and address multiplex. The maximum $\overline{RAS}$ low time and the minimum $\overline{CAS}$ page cycle time are used to determine the number of columns that can be accessed.

Unlike conventional page-mode operations, the enhanced page mode allows the TMS55165 to operate at a higher data bandwidth. Data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. A valid column address can be presented immediately after the row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low) if $t_{a(CA)}$ max (access time from column address) has been satisfied.

refresh

$\overline{CAS}$-before $\overline{RAS}$ (CBR) refresh

CBR refreshes are accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored, and the refresh row address is generated internally. Three types of CBR refresh cycles are available. The CBR refresh (option reset) ends the persistent write-per-bit mode and the stop-point mode. The CBRN and CBRS refreshes (no reset) do not end the persistent write-per-bit mode or the stop-point mode. The 512 rows of the DRAM do not necessarily need to be refreshed consecutively as long as the entire refresh is completed within the required time period, $t_{rf(MA)}$. The output buffers remain in the high-impedance state during the CBR refresh cycles regardless of the state of $\overline{TRG}$.

hidden refresh

A hidden refresh is accomplished by holding $\overline{CAS}$ low in the DRAM read cycle and cycling $\overline{RAS}$. The output data of the DRAM read cycle remains valid while the refresh is being carried out. Like the CBR refresh, the refreshed row addresses are generated internally during the hidden refresh.

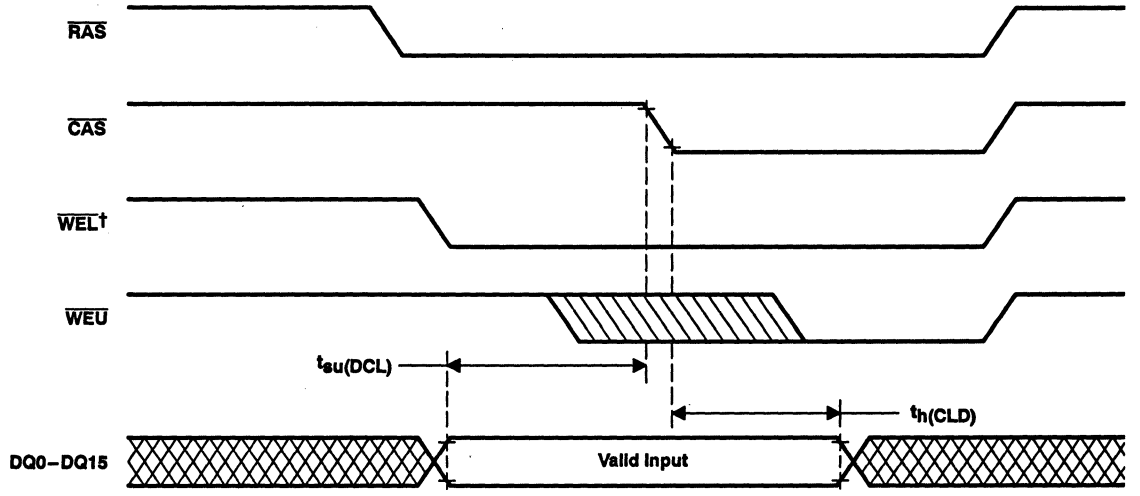
$\overline{RAS}$-only refresh

A $\overline{RAS}$ only refresh is accomplished by cycling $\overline{RAS}$ at every row address. Unless $\overline{CAS}$ and $\overline{TRG}$ are low, the output buffers remain in the high-impedance state to conserve power. Externally generated addresses must be supplied during $\overline{RAS}$ only refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed.

byte-write operation

Byte-write operations can be applied in DRAM write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles.

Holding either or both $\overline{WEL}$ and $\overline{WEU}$ low selects the write mode. In normal write cycles, $\overline{WEL}$ enables data to be written to the lower byte (DQ0–DQ7) and $\overline{WEU}$ enables data to be written to the upper byte (DQ8–DQ15). For early-write cycles, one of $\overline{WEx}$ is brought low before $\overline{CAS}$ falls. The other $\overline{WEx}$ can be brought low before $\overline{CAS}$ falls or after $\overline{CAS}$ falls. The data is strobed in with data setup and hold times for DQ0–DQ15 referenced to $\overline{CAS}$ (see Figure 1).



†Either $\overline{WEx}$ can be brought low prior to $\overline{CAS}$ assertion to initiate an early-write cycle.

Figure 1. Example of an Early-Write Cycle

byte-write operation (continued)

For late-write or read-modify-write cycles, $\overline{WEL}$ and $\overline{WEU}$ are both held high before $\overline{CAS}$ falls. After $\overline{CAS}$ falls, either or both $\overline{WEL}$ and $\overline{WEU}$ are brought low to select the corresponding byte or bytes to be written. Data is strobed in by either or both $\overline{WEL}$ and $\overline{WEU}$ with data setup and hold times for DQ0–DQ15 referenced to whichever $\overline{WEx}$ falls earlier (see Figure 2).

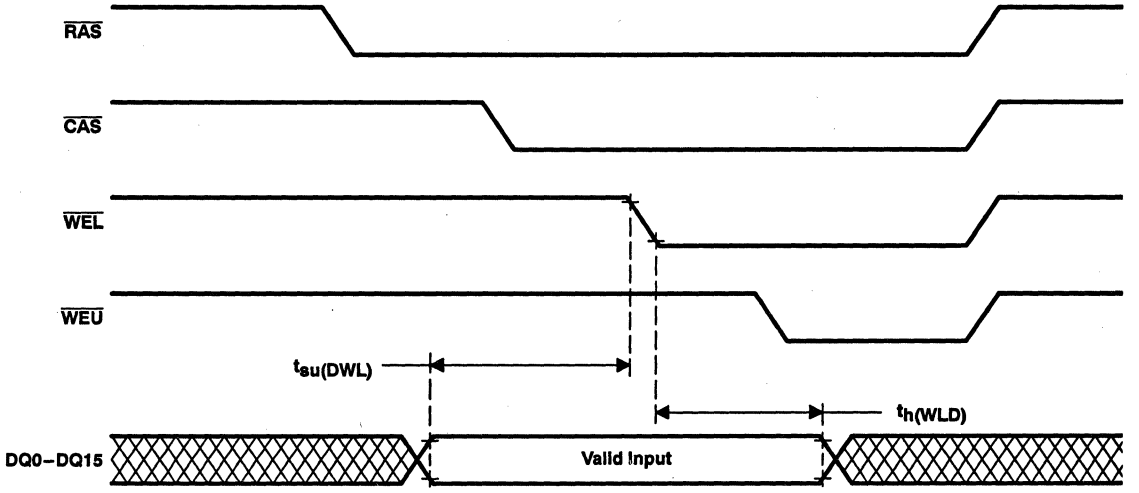


Figure 2. Example of a Late-Write Cycle

write-per-bit

The write-per-bit feature allows masking any combination of the 16 DQs on any write cycle. The write-per-bit operation is invoked when either or both $\overline{WEL}$ and $\overline{WEU}$ are held low on the falling edge of $\overline{RAS}$. Assertion of either individual $\overline{WEx}$ allows entry of the entire 16-bit mask on DQ0–DQ15. Byte control of the mask input is not allowed.

If both $\overline{WEL}$ and $\overline{WEU}$ are held high on the falling edge of $\overline{RAS}$, the write operation is performed without any masking. The TMS55165 offers two write-per-bit modes: the nonpersistent write-per-bit and the persistent write-per-bit.

nonpersistent write-per-bit

When either or both $\overline{WEL}$ and $\overline{WEU}$ are low on the falling edge of $\overline{RAS}$, the write mask is reloaded. A 16-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the 16 random I/Os are to be written and which are not. After $\overline{RAS}$ has latched the on-chip write-per-bit mask, input data is driven onto the DQ pins and is latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later. $\overline{WEL}$ enables the lower byte (DQ0–DQ7) to be written through the mask, and $\overline{WEU}$ enables the upper byte (DQ8–DQ15) to be written through the mask. If a data low (write mask = 0) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data is not written to that I/O. If a data high (write mask = 1) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data is written to that I/O (see Figure 3).

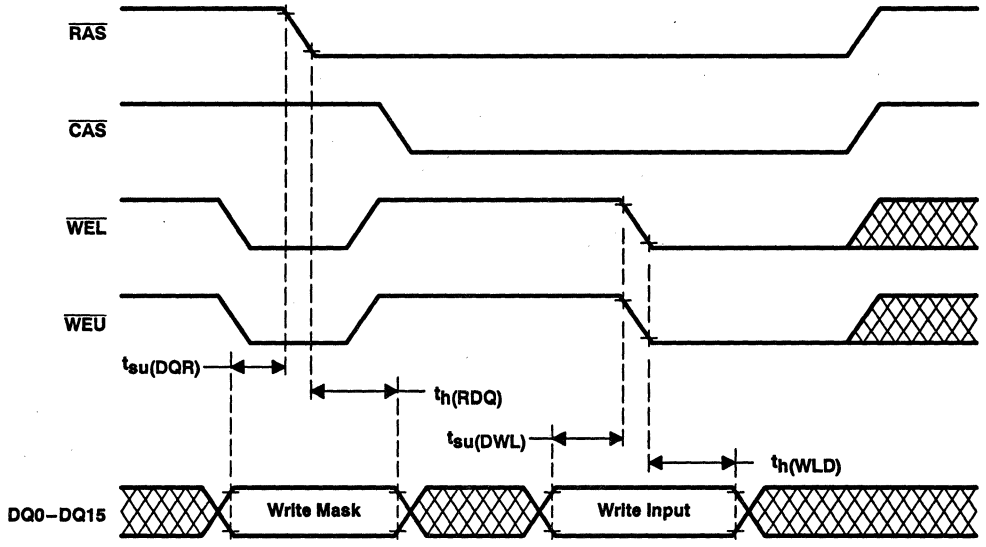


Figure 3. Example of a Nonpersistent Write-Per-Bit (Late-Write) Operation

persistent write-per-bit

The persistent write-per-bit mode is initiated only by performing a load-write-mask-register (LMR) cycle first. In the persistent write-per-bit mode, the write-per-bit mask is not overwritten but remains valid over an arbitrary number of write cycles until another LMR cycle is performed or power is removed.

The load-write-mask-register cycle is performed using DRAM write-cycle timing except DSF is held high on the falling edge of $\overline{RAS}$ and held low on the falling edge of $\overline{CAS}$. A binary code is input to the write-mask register via the random I/O pins and latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later. Byte-write control can be applied to the write mask during the load-write-mask-register cycle. The persistent write-per-bit mode can then be used in exactly the same way as the nonpersistent write-per-bit mode except that the input data on the falling edge of $\overline{RAS}$ is ignored. When the device is set to the persistent write-per-bit mode, it remains in this mode and is reset only by a CBR refresh with option reset cycle (see Figure 4).

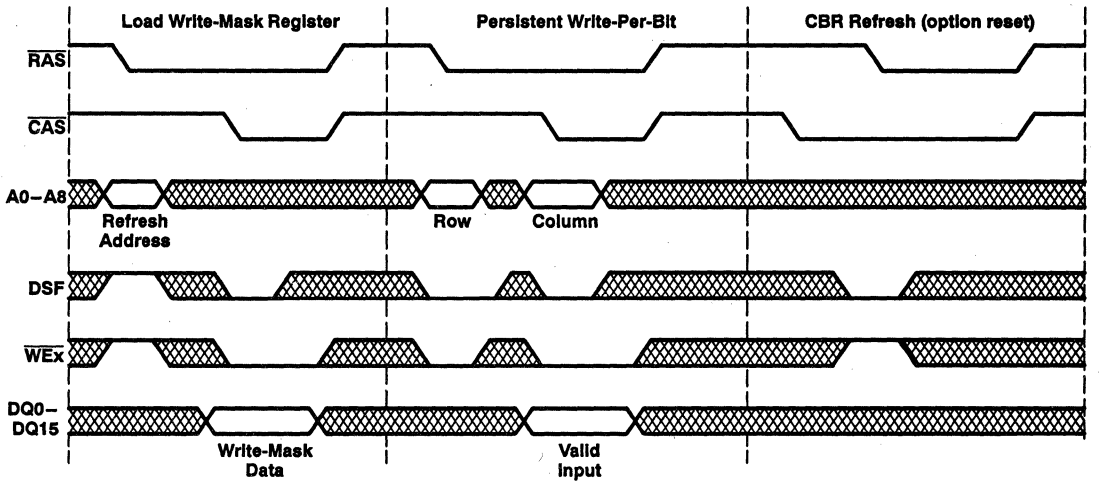


Figure 4. Example of a Persistent Write-Per-Bit Operation

block write

The block-write feature allows up to 64 bits of data to be written simultaneously to one row of the memory array. This function is implemented as (4 columns × 4 DQs) repeated in four quadrants. In this manner, each of the four one-megabit quadrants can have up to four consecutive columns written at a time with up to four DQs per column (see Figure 5).

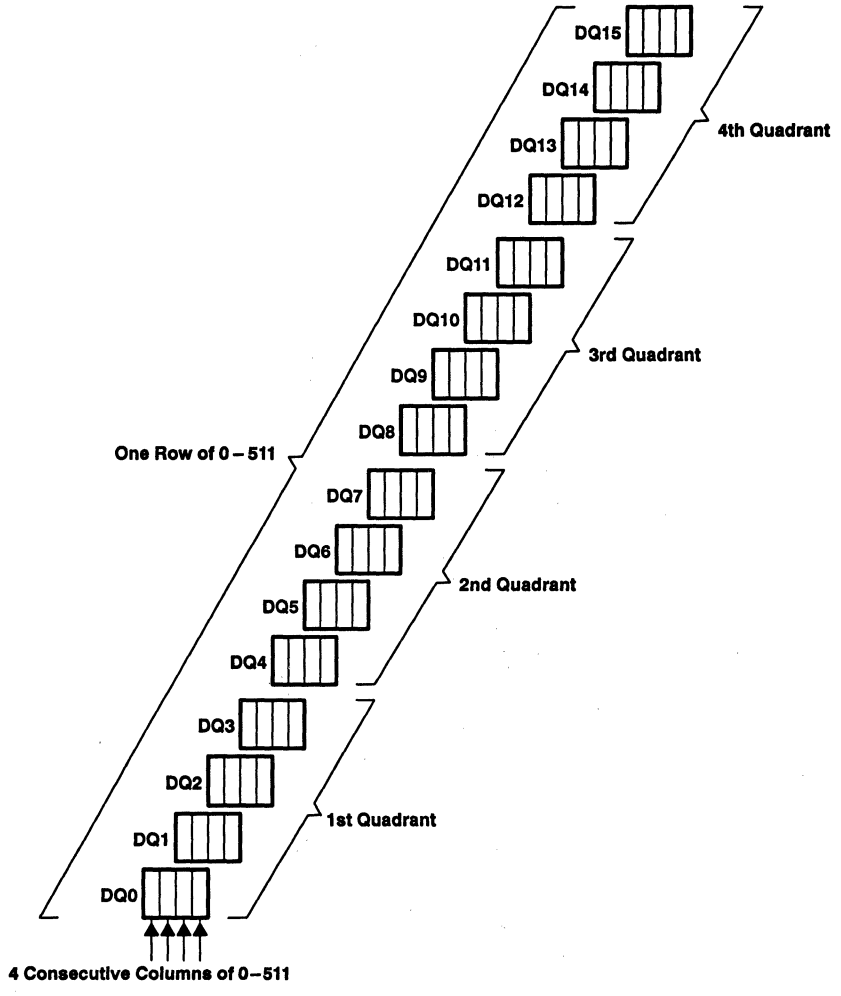


Figure 5. Block-Write Operation

Each one-megabit quadrant has a 4-bit column mask to mask off any or all of the four columns from being written with data. Nonpersistent write-per-bit or persistent write-per-bit functions can be applied to the block-write operation to provide write-masking options. The DQ data is provided by four bits from the on-chip color register. Bits 0–3 from the 16-bit write-mask register, bits 0–3 from the 16-bit column-mask register, and bits 0–3 from the 16-bit color-data register configure the block write for the first quadrant, while bits 4–7, 8–11, and 12–15 of the corresponding registers control the other quadrants in a similar fashion (see Figure 6).

block write (continued)

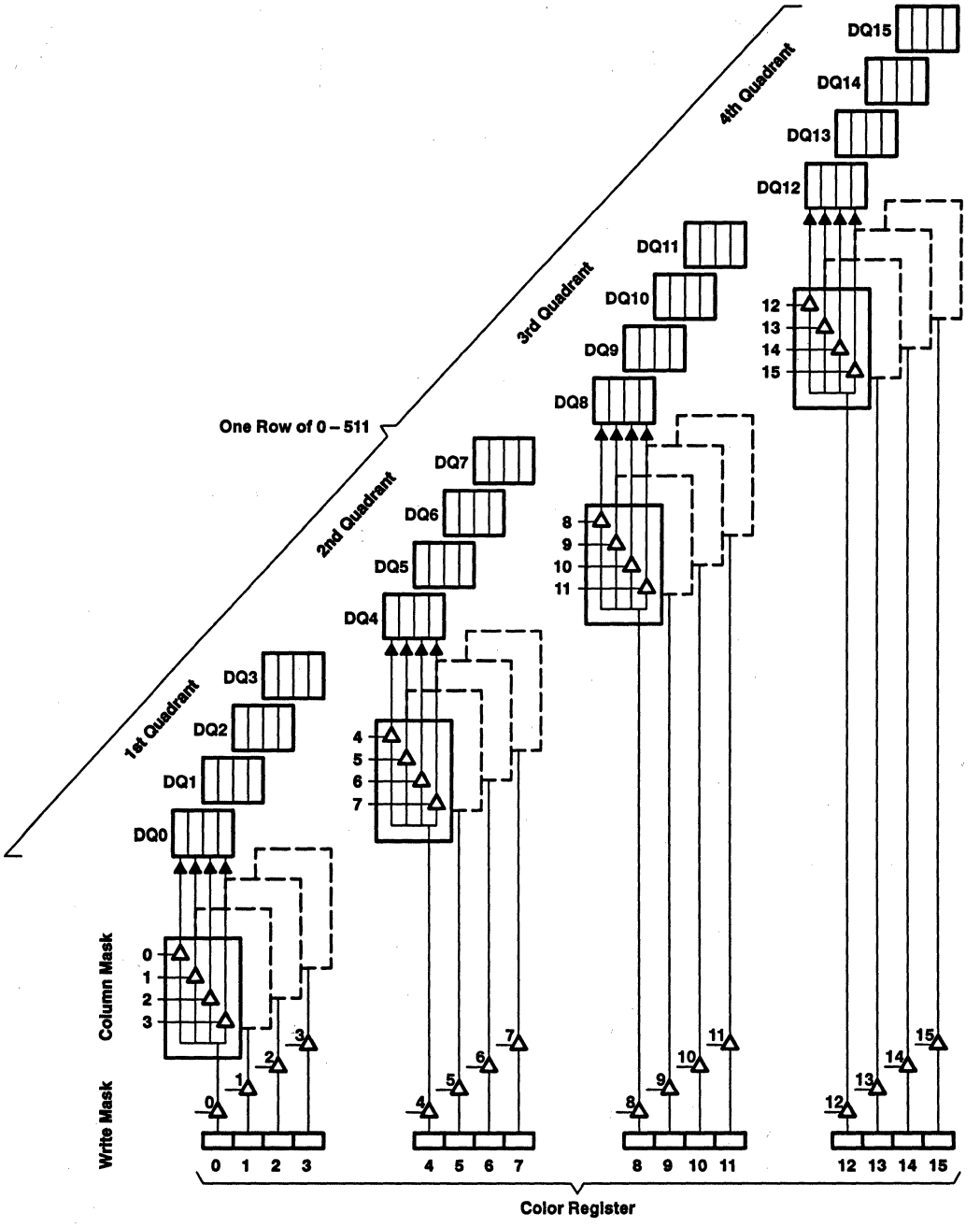


Figure 6. Block Write With Masks

block write (continued)

Every four columns make a block, which makes 128 blocks along one row. Block 0 comprises columns 0–3, block 1 comprises columns 4–7, block 2 comprises columns 8–11, etc., as shown in Figure 7.

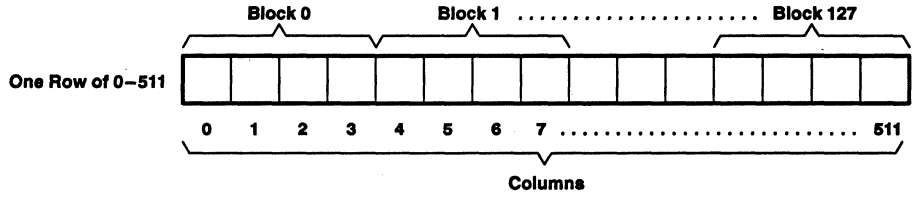


Figure 7. Block Columns Organization

During block-write cycles, only the seven most significant column addresses (A2–A8) are latched on the falling edge of $\overline{CAS}$ to decode one of the 128 blocks. Address bits A0–A1 are ignored. Each one-megabit quadrant has the same block selected.

A block-write cycle is entered in a manner similar to a DRAM write cycle except DSF is held high on the first falling edge of $\overline{CAS}$. As in a DRAM write operation, $\overline{WEL}$ and $\overline{WEU}$ enable the corresponding lower and upper DRAM DQ bytes to be written, respectively. The column-mask data is input via the DQs and is latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later. The 16-bit color-data register must be loaded prior to performing a block write as described below. Refer to the write-per-bit section for details on use of the write-mask capability, allowing additional performance options.

Example of block write:

block-write column address = 110000000 (A0–A8 from left to right)

	bit 0			bit 15
color-data register =	1011	1011	1100	0111
write-mask register =	1110	1111	1111	1011
column-mask register =	1111	0000	0111	1010
	1st Quad	2nd Quad	3rd Quad	4th Quad

Column-address bits A0 and A1 are ignored. Block 0 (columns 0–3) is selected for each one-megabit quadrant. The first quadrant has DQ0–DQ2 written with bits 0–2 from the color-data register (101) to all four columns of block 0. DQ3 is not written and retains its previous data due to the write-mask register bit 3 being a 0.

The second quadrant (DQ4–DQ7) has all four columns masked off due to the column mask bits 4–7 being 0, so that no data is written.

The third quadrant (DQ8–DQ11) has its four DQs written with bits 8–11 from the color-data register (1100) to columns 1–3 of its block 0. Column 0 is not written and retains its previous data on all four DQs due to the column-mask-register bit 8 being 0.

The fourth quadrant (DQ12–DQ15) has DQ12, DQ14, and DQ15 written with bits 12, 14, and 15 from the color-data register to column 0 and column 2 of its block 0. DQ13 retains its previous data on all columns due to the write mask. Columns 1 and 3 retain their previous data on all DQs due to the column mask. If the previous data for the quadrant was all 0s, the fourth quadrant would contain the data pattern shown in Figure 8 after the block-write operation shown in the previous example.

block write (continued)

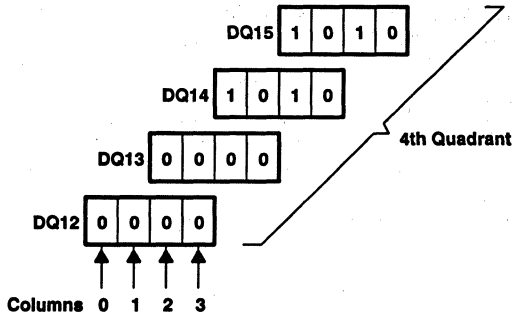
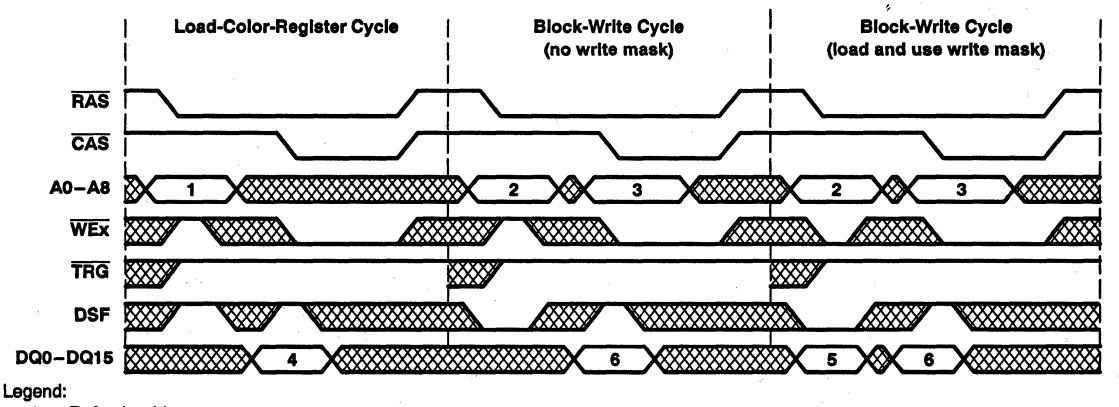


Figure 8. Example of Fourth Quadrant After a Block-Write Operation

load color register

The load-color-register cycle is performed using normal DRAM write-cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. The color register is loaded from pins DQ0–DQ15, which are latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later. If only one $\overline{WEx}$ is low, only the corresponding byte of the color register is loaded. When the color register is loaded, it retains data until power is lost or until another load-color-register cycle is performed (see Figure 9 and Figure 10).



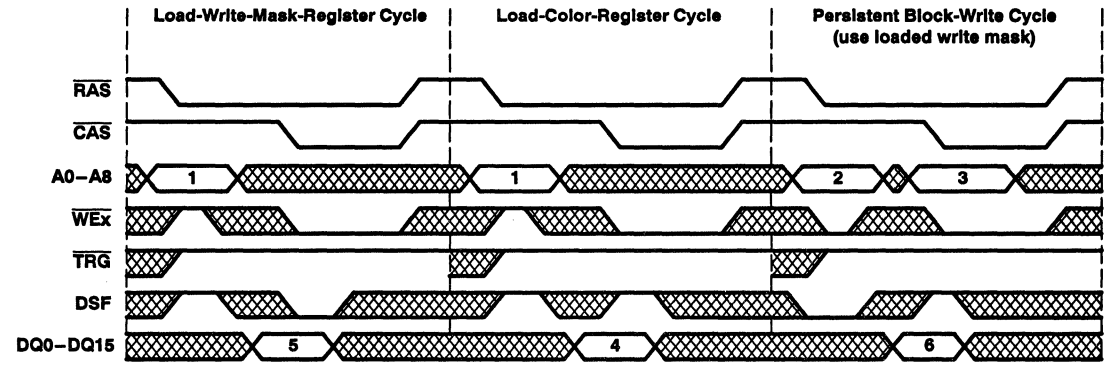
Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the falling edge of $\overline{CAS}$.
4. Color-register data
5. Write-mask data: DQ0–DQ15 are latched on the falling edge of $\overline{RAS}$.
6. Column-mask data: DQi–DQi+3 (i = 0, 4, 8, 12) are latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later.

= don't care

Figure 9. Example of Block Writes

load color register (continued)



Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the falling edge of $\overline{CAS}$.
4. Color-register data
5. Write-mask data: DQ0 – DQ15 are latched on the falling edge of $\overline{CAS}$.
6. Column-mask data: DQi–DQi+3 (i = 0, 4, 8, 12) are latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later.

= don't care

Figure 10. Example of a Persistent Block Write

DRAM-to-SAM transfer operation

During the DRAM-to-SAM transfer operation, one half of a row (256 columns) in the DRAM array is selected to be transferred to the 256-bit serial-data register. The transfer operation is invoked by bringing $\overline{TRG}$ low and holding $\overline{WEx}$ high on the falling edge of $\overline{RAS}$. The state of DSF, which is latched on the falling edge of $\overline{RAS}$, determines whether the full-register-transfer read operation or the split-register-transfer read operation is performed.

Table 4. SAM Function Table

FUNCTION	$\overline{RAS}$ FALL				$\overline{CAS}$ FALL	ADDRESS		DQ0–DQ15		MNE CODE
	$\overline{CAS}$	$\overline{TRG}$	$\overline{WEx}$†	DSF	DSF	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$ $\overline{WEx}$	
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT

† Logic L is selected when either or both $\overline{WEL}$ and $\overline{WEU}$ are low.
X = don't care

full-register-transfer read

A full-register-transfer read operation loads data from a selected half of a row in the DRAM into the SAM. $\overline{TRG}$ is brought low and latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. The nine column-address bits (A0–A8) are latched at the falling edge of $\overline{CAS}$, where address bit A8 selects which half of the row is transferred. Address bits A0–A7 select one of the SAM's 256 available tap points from which the serial data is read out (see Figure 11).

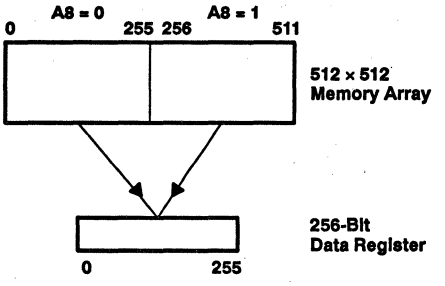


Figure 11. Full-Register-Transfer Read

A full-register-transfer read can be performed in three ways: early load, real-time load (or midline load), or late load. Each of these offers the flexibility of controlling the $\overline{TRG}$ trailing edge in the full-register-transfer read cycle (see Figure 12).

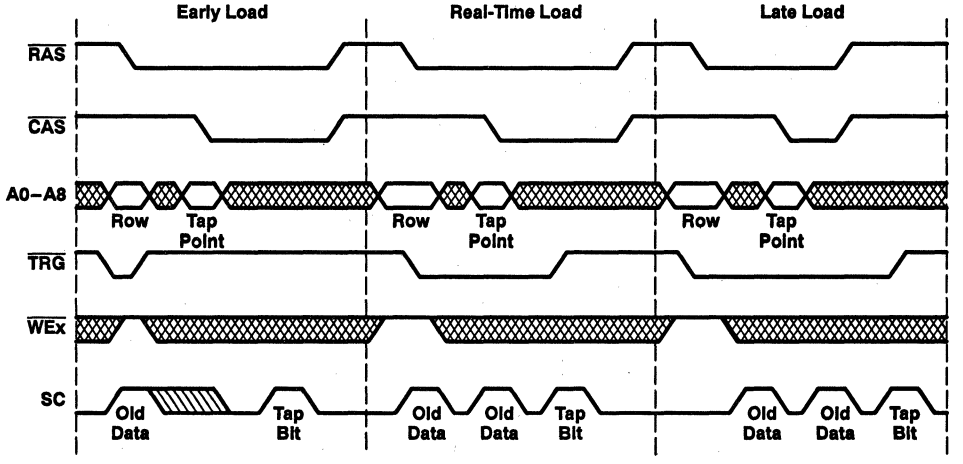


Figure 12. Example of Full-Register-Transfer Read Operations

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split-register-transfer read

In the split-register-transfer read operation, the serial data register is split into halves. The low half contains bits 0–127, and the high half contains bits 128–255. While one half is being read out of the SAM port, the other half can be loaded from the memory array.

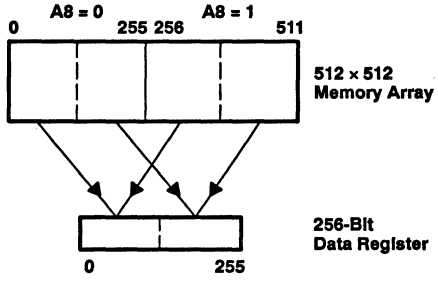
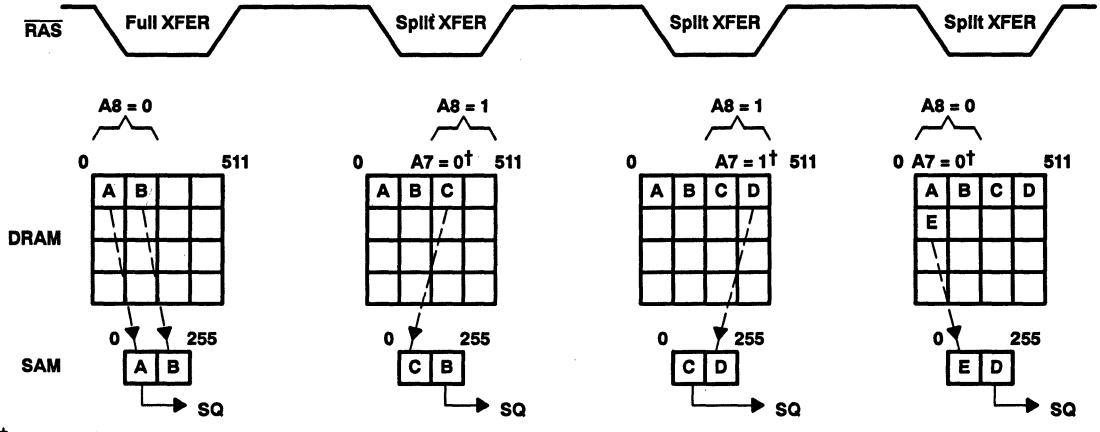


Figure 13. Split-Register-Transfer Read

To invoke a split-register-transfer read cycle, DSF is brought high, $\overline{TRG}$ is brought low, and both are latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. Eight of the nine column-address bits (A0–A6 and A8) are latched at the falling edge of $\overline{CAS}$. Column-address bit A8 selects which half of the row is to be transferred. Column-address bits A0–A6 select one of the 127 tap points in the specified half of the SAM. Column-address bit A7 is ignored, and the split-register-transfer is internally controlled to select the inactive register half.



† A7 shown is internally controlled.

Figure 14. Example of a Split-Register-Transfer Read Operation

A full-register-transfer read must precede the first split-register-transfer read to ensure proper operation. After the full-register-transfer read cycle, the first split-register-transfer read can follow immediately without any minimum SC clock requirement.

split-register-transfer read (continued)

QSF indicates which half of the register is being accessed during serial access operation. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of the SAM. When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF changes state upon completing a full-register-transfer read cycle. The tap point loaded during the current transfer cycle determines the state of QSF. QSF also changes state when a boundary between two register halves is reached.

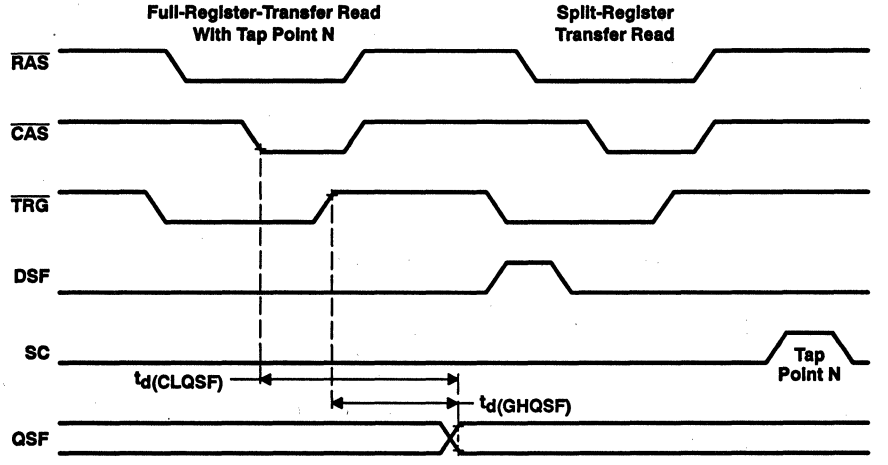


Figure 15. Example of a Split-Register-Transfer Read After a Full-Register-Transfer Read

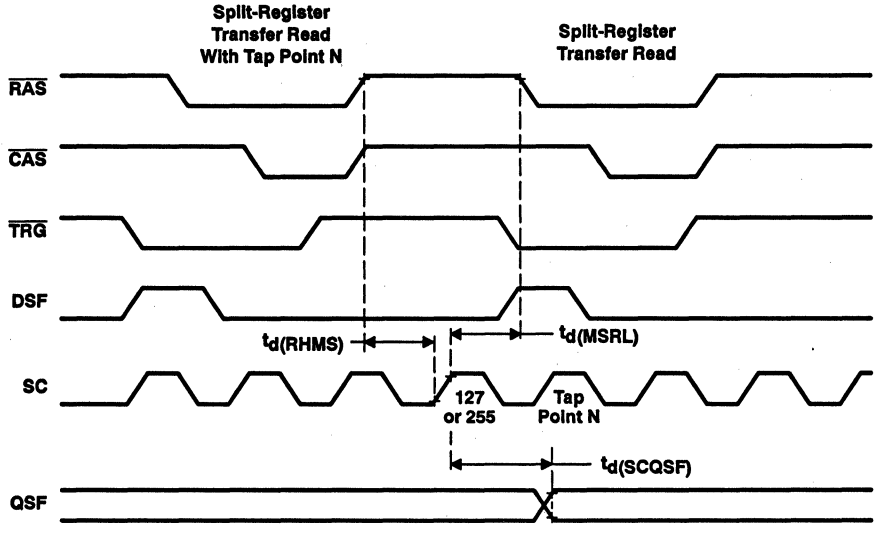


Figure 16. Example of Successive Split-Register-Transfer Read Operations

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serial-read operation

The serial-read operation can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during transfer operations. Serial data can be read from the SAM by clocking SC starting at the tap point loaded by the preceding transfer cycle, proceeding sequentially to the most significant bit (bit 255), and then wrapping around to the least significant bit (bit 0), as shown in Figure 17.

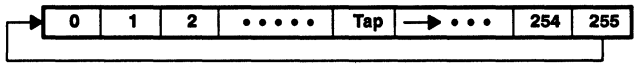


Figure 17. Serial Pointer Direction for Serial Read

For split-register operation, serial data can be read out from the active half of the SAM by clocking SC starting at the tap point loaded by the preceding split-register-transfer cycle. The serial pointer proceeds sequentially to the most significant bit of the half, bit 127 or bit 255. If there is a split-register-transfer read to the inactive half during this period, the serial pointer points next to the tap point location loaded by that split-register-transfer (see Figure 18).

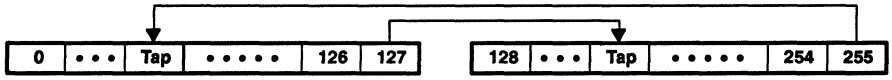


Figure 18. Serial Pointer for Split-Register Read – Case I

If there is no split-register-transfer read to the inactive half during this period, the serial pointer points next to the least significant bit of the inactive half, bit 128 or bit 0 (see Figure 19).

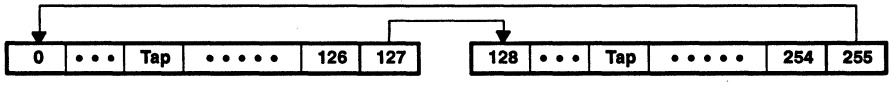


Figure 19. Serial Pointer for Split-Register Read – Case II

split-register programmable stop point

The TMS55165 offers programmable stop-point mode for split-register-transfer read operation. This mode can be used to improve 2-D drawing performance in a nonscanline data format.

In split-register-transfer read operation, the stop point is defined as a register location at which the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM. While in stop-point mode, the SAM is divided into partitions whose length is programmed via row addresses A4–A7 in a CBR set (CBRS) cycle. The last serial-address location of each partition is the stop point (see Figure 20).

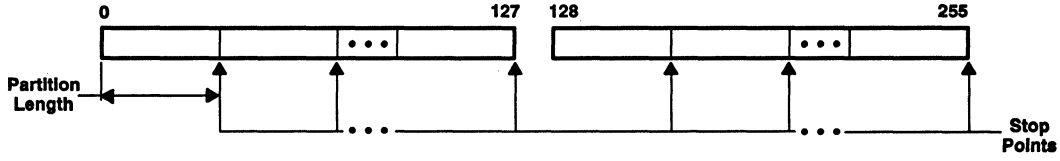


Figure 20. Example of the SAM With Partitions

split-register programmable stop point (continued)

Stop-point mode is not active until the CBRS cycle is initiated. The CBRS operation is performed by holding $\overline{CAS}$ and $\overline{WEx}$ low and DSF high on the falling edge of $\overline{RAS}$. The falling edge of $\overline{RAS}$ also latches row addresses A4–A7, which are used to define the SAM's partition length. The other row address inputs are don't care. Stop-point mode should be initiated after the initialization cycles have been performed (see Table 5).

Table 5. Programming Code for Stop-Point Mode

MAXIMUM PARTITION LENGTH	ADDRESS AT $\overline{RAS}$ IN CBRS CYCLE						NUMBER OF PARTITIONS	STOP-POINT LOCATIONS
	A8	A7	A6	A5	A4	A0–A3		
16	X	L	L	L	L	X	16	15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255
32	X	L	L	L	H	X	8	31, 63, 95, 127, 159, 191, 223, 255
64	X	L	L	H	H	X	4	63, 127, 191, 255
128 (default)	X	L	H	H	H	X	2	127, 255

In stop-point mode, the tap point loaded during the split-register-transfer read cycle determines in which SAM partition the serial output begins and at which stop point the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM (see Figure 21).

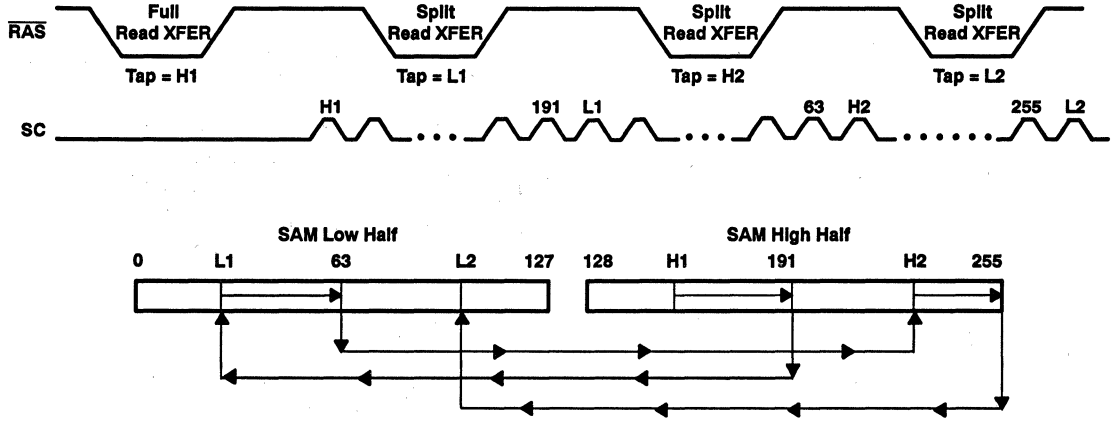


Figure 21. Example of Split-Register Operation with Programmable Stop Points

256-/512-bit compatibility of split-register programmable stop point

The stop-point mode is designed to be compatible both for 256-bit SAM and 512-bit SAM devices. After the CBRS cycle is initiated, the stop-point mode becomes active. In the stop-point mode, and only in the stop-point mode, the column-address bits AY7 and AY8 are internally swapped to assure the compatibility (see Figure 22). This address-bit swap applies to the column address, and it is effective for all DRAM and transfer cycles. For example, during the split-register-transfer cycle with stop point, column-address bit AY8 is a don't care and AY7 decodes the DRAM row half for the split-register-transfer. During stop-point mode, a CBR option reset (CBR) cycle is not recommended because this ends the stop-point mode and restores address bits AY7 and AY8 to their normal function. Consistent use of CBR cycles ensures that the TMS55165 remains in normal mode.

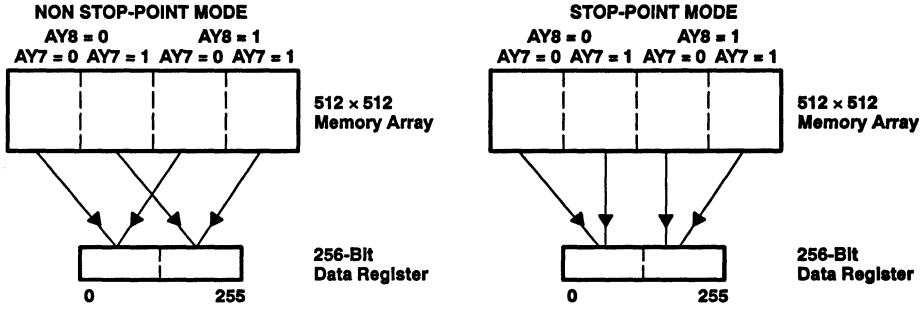


Figure 22. DRAM-to-SAM Mapping, Non Stop-Point Versus Stop Point

IMPORTANT: For proper device operation in a split-register stop-point mode, a CBRS cycle should be initiated right after the power-up initialization cycles have been performed.

power up

To achieve proper device operation, an initial pause of 200 µs is required after power up followed by a minimum of eight $\overline{RAS}$ cycles or eight CBR cycles to initialize the DRAM port. A full-register-transfer read cycle and two SC cycles are needed to initialize the SAM port.

After initialization, the internal state of the TMS55165 is as follows:

	STATE AFTER INITIALIZATION
QSF	Defined by the transfer cycle during initialization
Write mode	Nonpersistent mode
Write-mask register	Undefined
Color register	Undefined
Serial-register tap point	Defined by the transfer cycle during initialization
SAM port	Output mode

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −1 V to 7 V
Voltage range on any pin ..... −1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1.1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	SAM PORT	'55165-60		'55165-70		'55165-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −1 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 5.8 V, All other pins at 0 V to V_{CC}			±10		±10		±10	μA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC} See Note 3			±10		±10		±10	μA
I_{CC1}	Operating current§	See Note 4	Standby		180		165		150	mA
I_{CC1A}	Operating current§	$t_{c(SC)}$ = MIN	Active		225		205		185	mA
I_{CC2}	Standby current	All clocks = V_{CC}	Standby		5		5		5	mA
I_{CC2A}	Standby current	$t_{c(SC)}$ = MIN	Active		70		65		60	mA
I_{CC3}	$\overline{RAS}$-only refresh current	See Note 4	Standby		180		165		150	mA
I_{CC3A}	$\overline{RAS}$-only refresh current	$t_{c(SC)}$ = MIN, See Note 4	Active		225		205		185	mA
I_{CC4}	Page-mode current§	$t_{c(P)}$ = MIN, See Note 5	Standby		135		115		105	mA
I_{CC4A}	Page-mode current§	$t_{c(SC)}$ = MIN, See Note 5	Active		175		155		140	mA
I_{CC5}	CBR current	See Note 4	Standby		180		165		150	mA
I_{CC5A}	CBR current	$t_{c(SC)}$ = MIN, See Note 4	Active		225		205		185	mA
I_{CC6}	Data-transfer current	See Note 4	Standby		200		180		160	mA
I_{CC6A}	Data-transfer current	$t_{c(SC)}$ = MIN	Active		250		225		200	mA

‡ For conditions shown as MIN/MAX, use the appropriate value specified in timing requirements.
§ Measured with outputs open
NOTES: 3. $\overline{SE}$ is disabled for SQ output leakage tests.
4. Measured with one address change while $\overline{RAS}$ = V_{IL}, $t_{c(rd)}$, $t_{c(W)}$, $t_{c(TRD)}$ = MIN.
5. Measured with one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, address strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(DSF)}$	Input capacitance, special function		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
$C_{o(O)}$	Output capacitance, SQ and DQ		7	pF
$C_{o(QSF)}$	Output capacitance, QSF		9	pF

NOTE 6: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		TEST CONDITIONS†	ALT. SYMBOL	'55165-60		'55165-70		'55165-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		17		20		20	ns
$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{AA}		30		35		40	ns
$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = MAX	t_{CPA}		35		40		45	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MAX	t_{RAC}		60		70		80	ns
$t_{a(G)}$	Access time of DQ from $\overline{TRG}$ low		t_{OEA}		15		20		20	ns
$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 30 pF	t_{SCA}		15		20		25	ns
$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		12		15		20	ns
$t_{dis(CH)}$	Disable time, random output from $\overline{CAS}$ high (see Note 8)	C_L = 50 pF	t_{OFF}	0	15	0	20	0	20	ns
$t_{dis(G)}$	Disable time, random output from $\overline{TRG}$ high (see Note 8)	C_L = 50 pF	t_{OEZ}	0	15	0	20	0	20	ns
$t_{dis(SE)}$	Disable time, serial output from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	0	10	0	15	0	20	ns

† Measured with outputs open. For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

NOTES: 7. Switching times for RAM port output are measured with a load equivalent to 1 TTL load and 50 pF. Data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V. Switching times for SAM port output are measured with a load equivalent to 1 TTL load and 30 pF. Serial data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V.

8. $t_{dis(CH)}$, $t_{dis(G)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature†

		ALT. SYMBOL	'55165-60		'55165-70		'55165-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Cycle time, read	t_{RC}	110		130		150		ns
$t_{c(W)}$	Cycle time, write	t_{WC}	110		130		150		ns
$t_{c(rdW)}$	Cycle time, read-modify-write	t_{RMW}	150		175		200		ns
$t_{c(P)}$	Cycle time, page-mode read, write	t_{PC}	35		40		45		ns
$t_{c(RDWP)}$	Cycle time, page-mode read-modify-write	t_{PRMW}	80		90		100		ns
$t_{c(TRD)}$	Cycle time, transfer read	t_{RC}	110		130		150		ns
$t_{c(SC)}$	Cycle time, serial clock (see Note 9)	t_{SCC}	18		22		30		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CPN}	10		10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 10)	t_{CAS}	17	10 000	20	10 000	20	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	40		50		60		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 11)	t_{RAS}	60	10 000	70	10 000	80	10 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{WEx}$ low	t_{WP}	10		10		15		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		15		20		20		ns
$t_{w(SCH)}$	Pulse duration, SC high (see Note 9)	t_{SC}	5		8		10		ns
$t_{w(SCL)}$	Pulse duration, SC low (see Note 9)	t_{SCP}	5		8		10		ns
$t_{w(GH)}$	Pulse duration, $\overline{TRG}$ high	t_{TP}	20		20		20		ns
$t_{w(RL)P}$	Pulse duration, $\overline{RAS}$ low (page mode)	t_{RASP}	60	100 000	70	100 000	80	100 000	ns
$t_{su(CA)}$	Setup time, column address before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{su(SFC)}$	Setup time, DSF before $\overline{CAS}$ low	t_{FSC}	0		0		0		ns
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(WMR)}$	Setup time, $\overline{WEx}$ before $\overline{RAS}$ low	t_{WSR}	0		0		0		ns
$t_{su(DQR)}$	Setup time, DQ before $\overline{RAS}$ low	t_{MS}	0		0		0		ns
$t_{su(TRG)}$	Setup time, $\overline{TRG}$ high before $\overline{RAS}$ low	t_{THS}	0		0		0		ns
$t_{su(SFR)}$	Setup time, DSF low before $\overline{RAS}$ low	t_{FSR}	0		0		0		ns
$t_{su(DCL)}$	Setup time, data valid before $\overline{CAS}$ low	t_{DSC}	0		0		0		ns
$t_{su(DWL)}$	Setup time, data valid before $\overline{WEx}$ low	t_{DSW}	0		0		0		ns
$t_{su(rd)}$	Setup time, read command, $\overline{WEx}$ high before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	Setup time, early write command, $\overline{WEx}$ low before $\overline{CAS}$ low	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	Setup time, $\overline{WEx}$ low before $\overline{CAS}$ high, write	t_{CWL}	15		15		20		ns
$t_{su(WRH)}$	Setup time, $\overline{WEx}$ low before $\overline{RAS}$ high, write	t_{RWL}	15		15		20		ns
$t_{h(CLCA)}$	Hold time, column address after $\overline{CAS}$ low	t_{CAH}	10		10		15		ns
$t_{h(SFC)}$	Hold time, DSF after $\overline{CAS}$ low	t_{CFH}	10		10		15		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. Cycle time assumes t_t = 3 ns.

10. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].

11. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

			ALT. SYMBOL	'55165-60		'55165-70		'55165-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low		t_{RAH}	10		10		10		ns
$t_{h(TRG)}$	Hold time, $\overline{TRG}$ after $\overline{RAS}$ low		t_{THH}	10		10		10		ns
$t_{h(RWM)}$	Hold time, write mask after $\overline{RAS}$ low		t_{RWH}	10		10		10		ns
$t_{h(RDQ)}$	Hold time, DQ after $\overline{RAS}$ low (write-mask operation)		t_{MH}	10		10		10		ns
$t_{h(SFR)}$	Hold time, DSF after $\overline{RAS}$ low		t_{RFH}	10		10		10		ns
$t_{h(RLCA)}$	Hold time, column address valid after $\overline{RAS}$ low (see Note 12)		t_{AR}	30		30		35		ns
$t_{h(CLD)}$	Hold time, data valid after $\overline{CAS}$ low		t_{DH}	15		15		15		ns
$t_{h(RLD)}$	Hold time, data valid after $\overline{RAS}$ low (see Note 12)		t_{DHR}	35		35		35		ns
$t_{h(WLD)}$	Hold time, data valid after $\overline{WEx}$ low		t_{DH}	15		15		15		ns
$t_{h(CHrd)}$	Hold time, read, $\overline{WEx}$ low after $\overline{CAS}$ high (see Note 13)		t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Hold time, read, $\overline{WEx}$ high after $\overline{RAS}$ high (see Note 13)		t_{RRH}	0		0		0		ns
$t_{h(CLW)}$	Hold time, write, $\overline{WEx}$ low after $\overline{CAS}$ low		t_{WCH}	10		15		15		ns
$t_{h(RLW)}$	Hold time, write, $\overline{WEx}$ low after $\overline{RAS}$ low (see Note 12)		t_{WCR}	30		35		35		ns
$t_{h(WLG)}$	Hold time, $\overline{TRG}$ high after $\overline{WEx}$ low (see Note 14)		t_{OEH}	10		10		10		ns
$t_{h(SHSQ)}$	Hold time, SQ after SC high		t_{SOH}	4		5		5		ns
$t_{h(RSF)}$	Hold time, DSF after $\overline{RAS}$ low		t_{FHR}	30		30		35		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		t_{CSH}	60		70		80		ns
		See Note 15	t_{CHR}	10		10		15		
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		t_{RSH}	17		20		20		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{WEx}$ low (see Notes 16 and 17)		t_{CWD}	37		45		45		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note)		t_{RCD}	20	43	20	50	20	60	ns
$t_{d(CARH)}$	Delay time, column address valid to $\overline{RAS}$ high		t_{RAL}	30		35		40		ns
$t_{d(CACH)}$	Delay time, column address valid to $\overline{CAS}$ high		t_{CAL}	30		35		40		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{WEx}$ low (see Note 16)		t_{RWD}	80		95		105		ns
$t_{d(CAWL)}$	Delay time, column address valid to $\overline{WEx}$ low (see Note 16)		t_{AWD}	50		60		65		ns
$t_{d(CLRL)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 15)		t_{CSR}	0		0		0		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 15)		t_{RPC}	0		0		0		ns
$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high for DRAM read cycles			17		20		20		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ		t_{OED}	10		15		15		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
14. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
15. CBR refresh operation only
16. Read-modify-write operation only
17. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
18. The maximum value is specified only to assure $\overline{RAS}$ access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	'55165-60		'55165-70		'55165-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (see Note 19)	t_{RTH}	50		55		60		ns
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 19)	t_{RSD}	65		70		80		ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address valid	t_{RAD}	15	30	15	35	15	40	ns
$t_{d(GLRH)}$	Delay time, $\overline{TRG}$ low to $\overline{RAS}$ high	t_{ROH}	10		15		15		ns
$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 20)	t_{CSD}	20		20		25		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 19 and 20)	t_{TSL}	5		5		5		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 19)	t_{TRD}	−10		−10		−10		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 21)	t_{TRP}	40		50		60		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 19)	t_{TSD}	10		10		15		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split-register-transfer read cycles		15		20		20		ns
$t_{d(CLTH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high in real-time transfer read cycles	t_{CTH}	15		15		15		ns
$t_{d(CASH)}$	Delay time, column address to first SC in early-load transfer read cycles	t_{ASD}	25		25		30		ns
$t_{d(CAGH)}$	Delay time, column address to $\overline{TRG}$ high in real-time transfer read cycles	t_{ATH}	20		20		20		ns
$t_{d(DCL)}$	Delay time, data to $\overline{CAS}$ low	t_{DZC}	0		0		0		ns
$t_{d(DGL)}$	Delay time, data to $\overline{TRG}$ low	t_{DZO}	0		0		0		ns
$t_{d(MSRL)}$	Delay time, last (most significant) rising edge of SC to $\overline{RAS}$ low before boundary switch during split-transfer read cycles		15		20		20		ns
$t_{d(SCQSF)}$	Delay time, last (127 or 255) rising edge of SC to QSF switching at the boundary during split-register-transfer read cycles (see Note 2222)	t_{SQD}		20		25		30	ns
$t_{d(CLQSF)}$	Delay time, $\overline{CAS}$ low to QSF switching in transfer read cycles (see Note 2222)	t_{CQD}		25		30		35	ns
$t_{d(GHQSF)}$	Delay time, $\overline{TRG}$ high to QSF switching in transfer read cycles (see Note 2222)	t_{TQD}		20		25		30	ns
$t_{d(RLQSF)}$	Delay time, $\overline{RAS}$ low to QSF switching in transfer read cycles (see Note 2222)	t_{RQD}		65		70		75	ns
$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 19. Real-time load transfer read or late-load transfer read cycle only
20. Early-load transfer read cycle only
21. Full-register (read) transfer cycles only
22. Switching times for QSF output are measured with a load equivalent to 1 TTL load and 30 pF and output reference level is V_{OH} / V_{OL} = 2 V/0.8 V.

PARAMETER MEASUREMENT INFORMATION

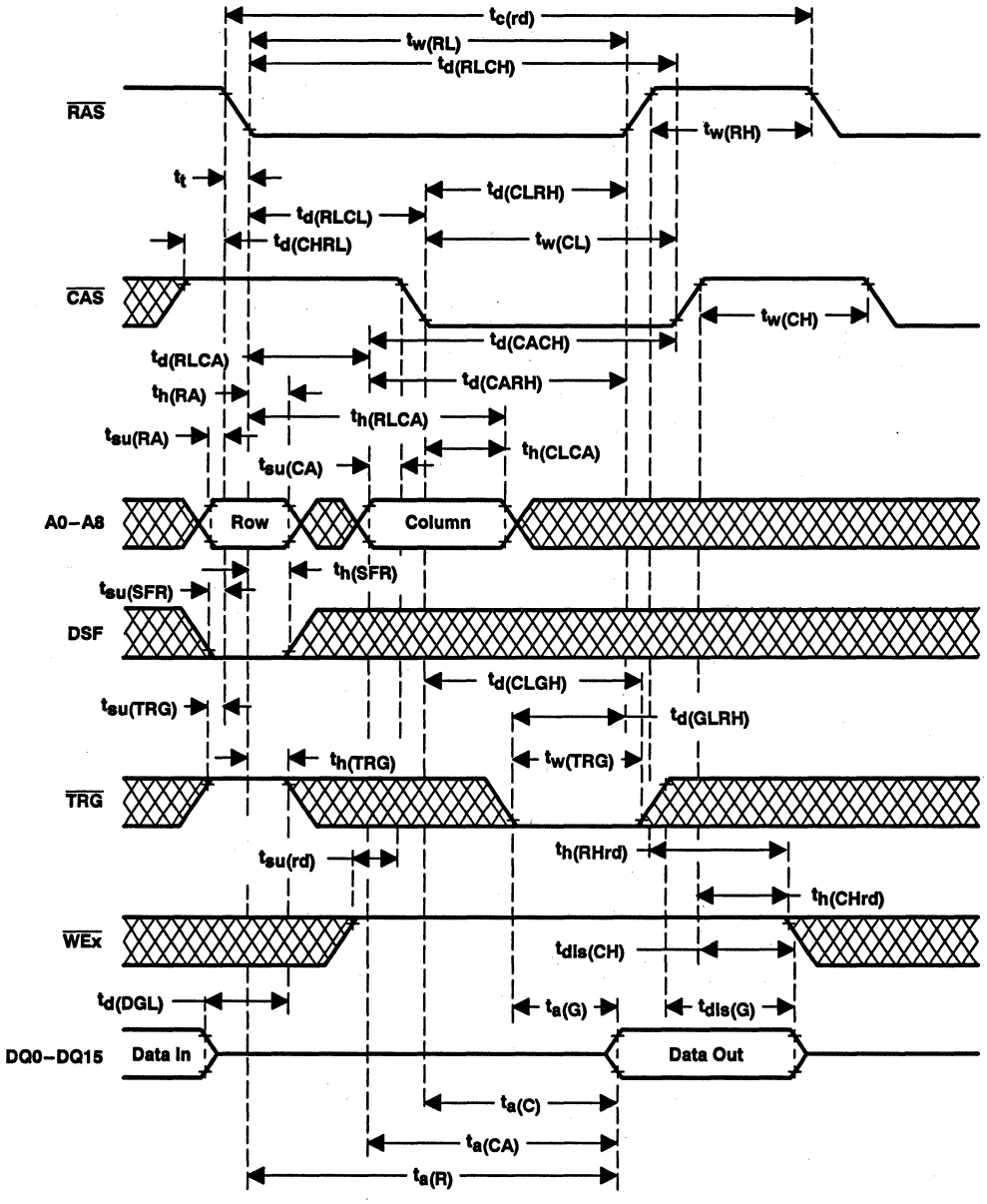


Figure 23. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

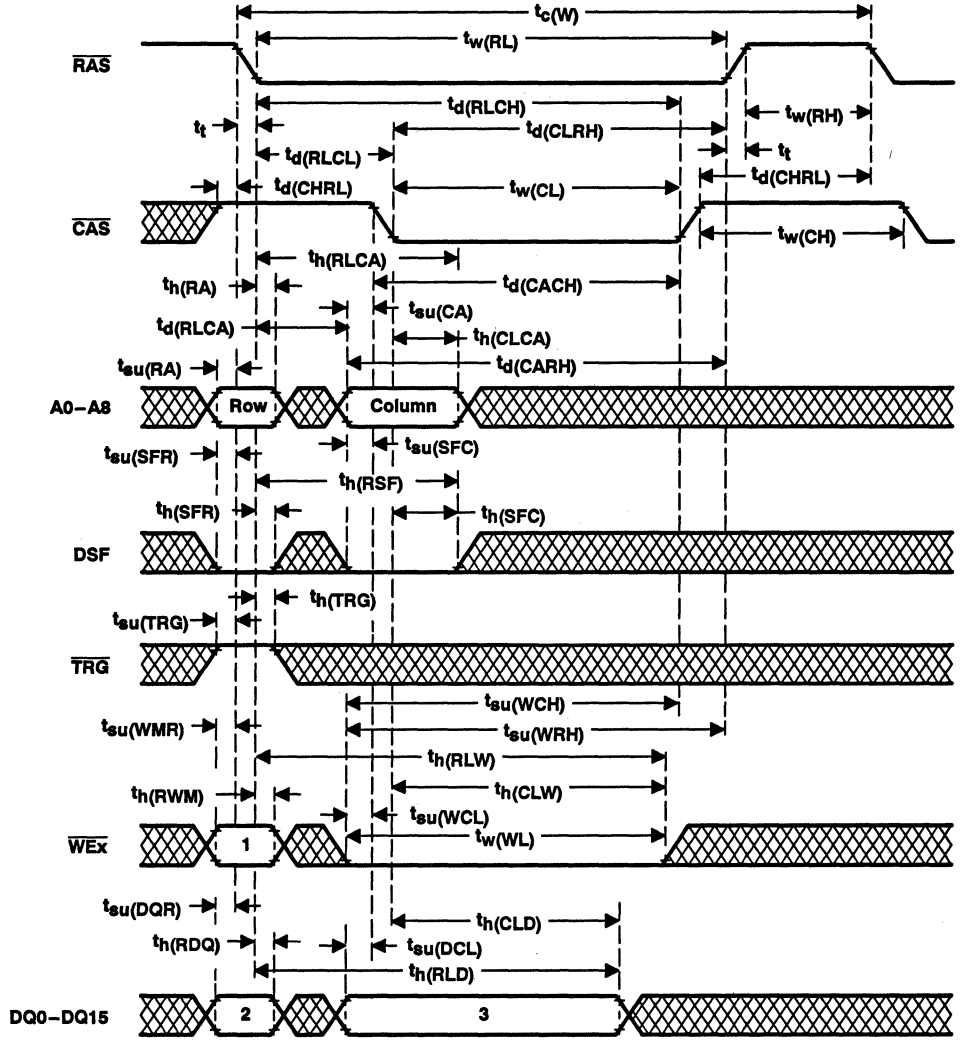


Figure 24. Early-Write-Cycle Timing

Table 6. Early-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

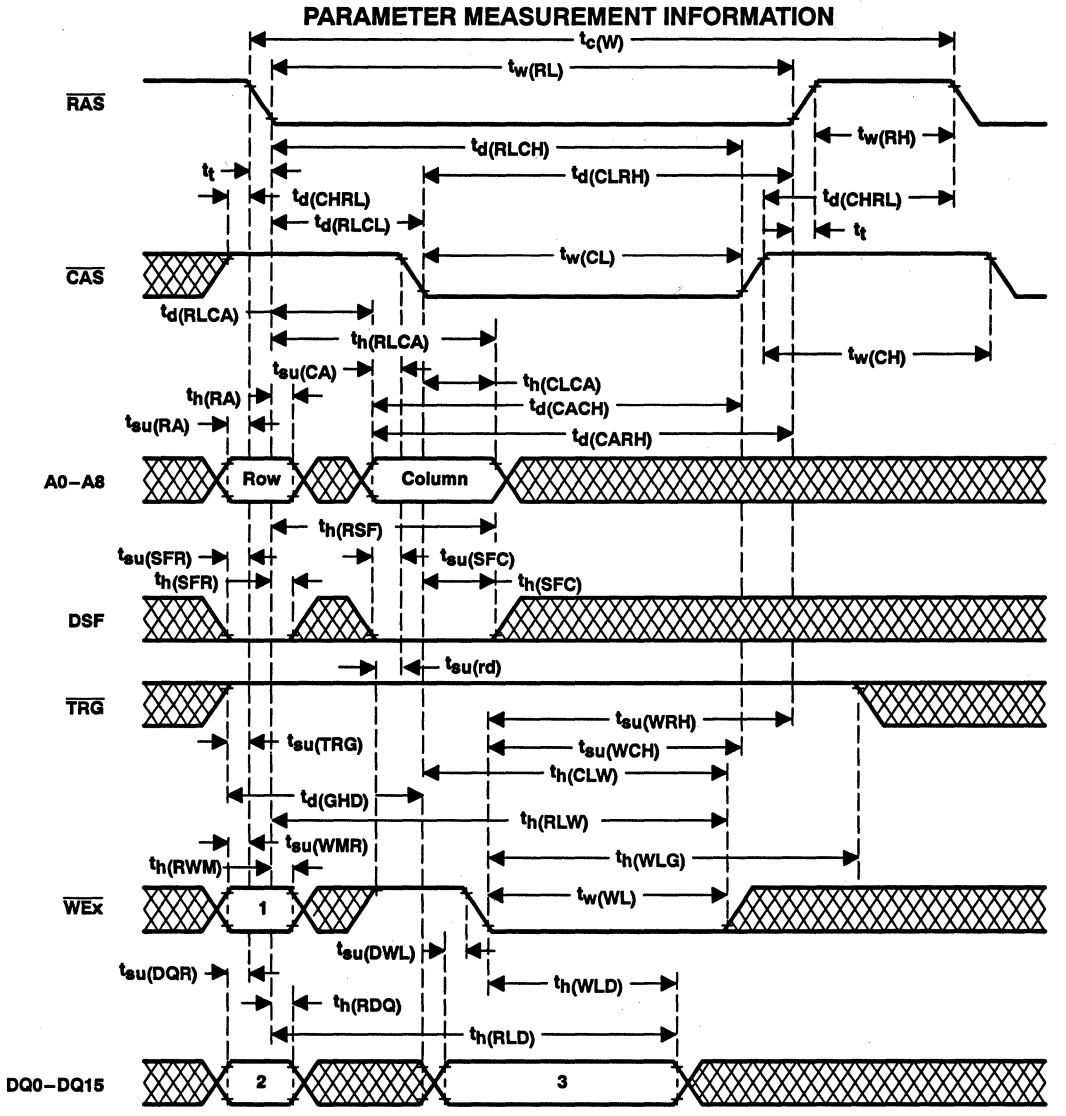
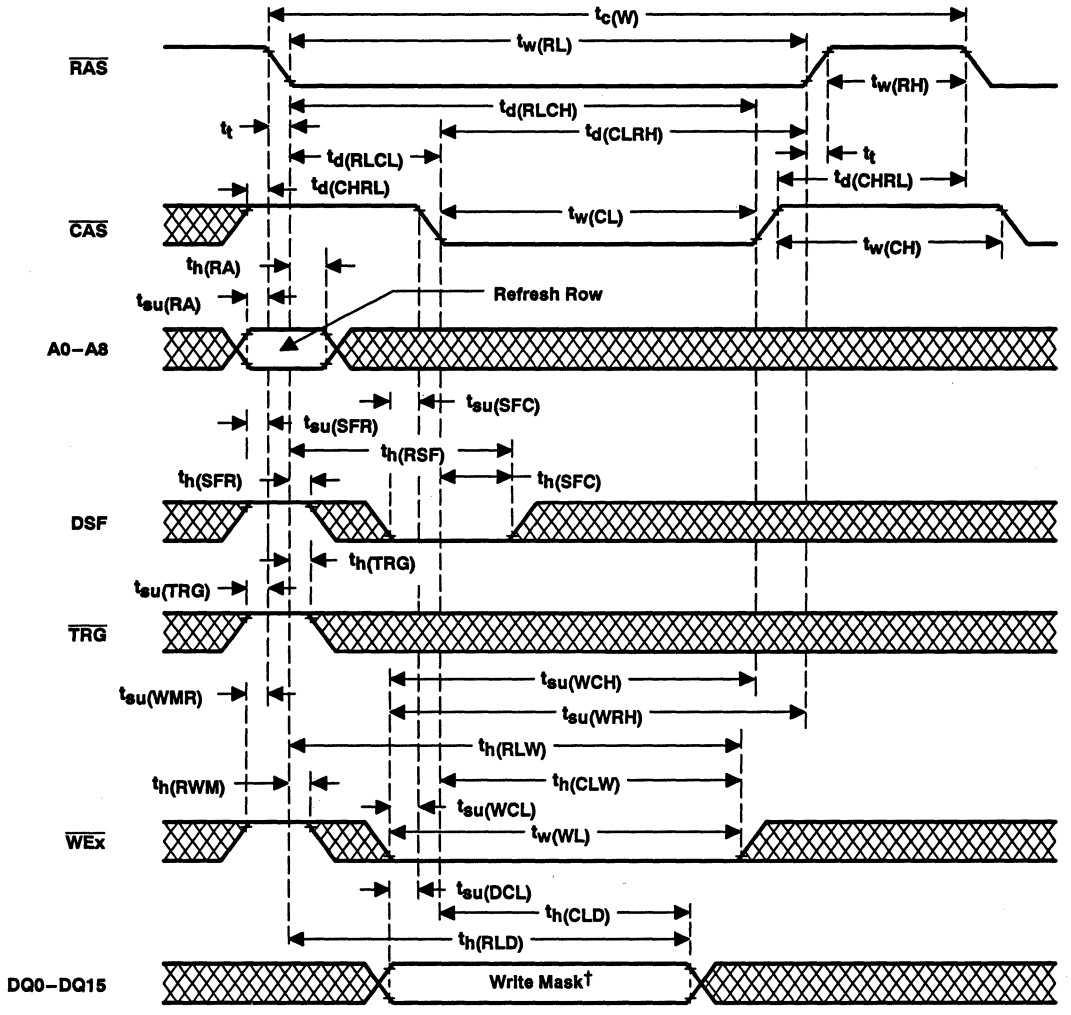


Figure 25. Late-Write-Cycle Timing (Output-Enable-Controlled Write)

Table 7. Late-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

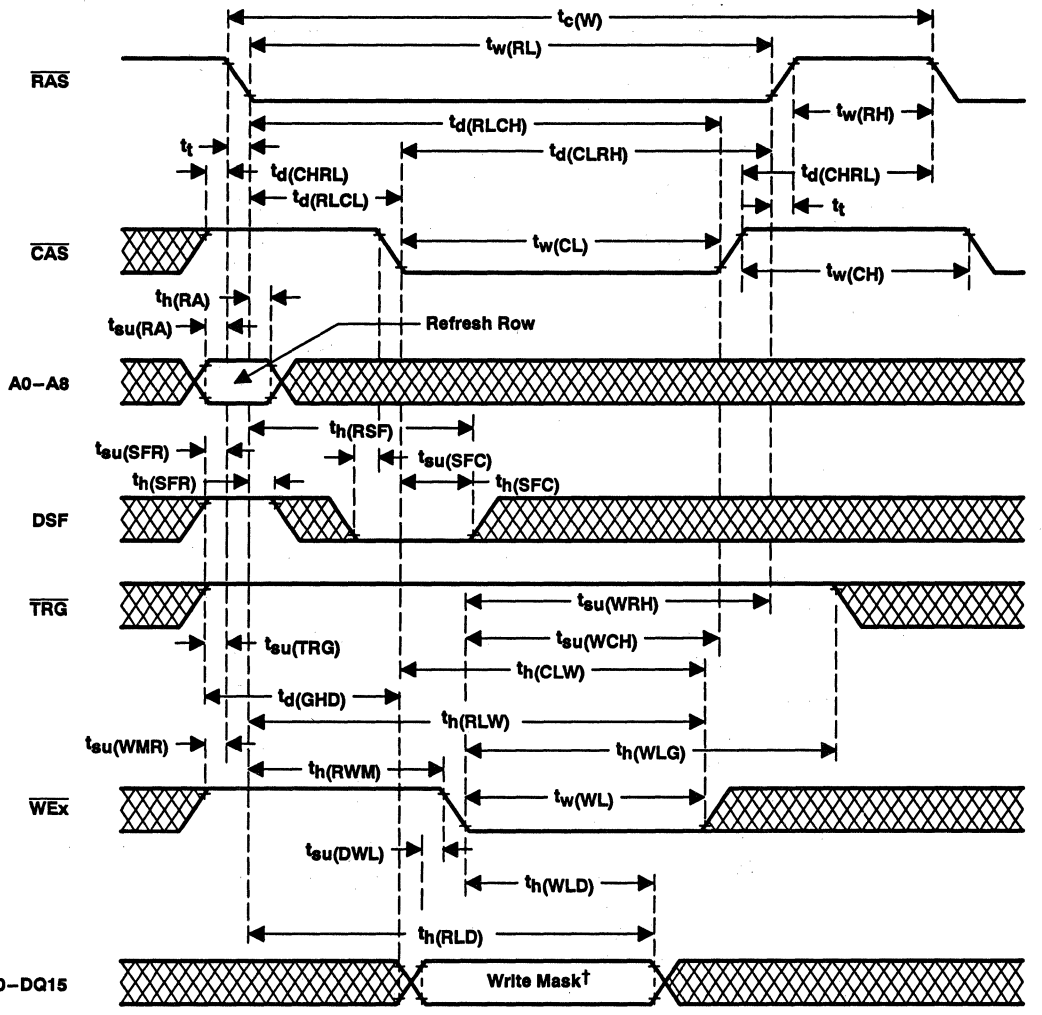
PARAMETER MEASUREMENT INFORMATION



† Load-write-mask-register cycle puts the device into the persistent write-per-bit mode.

Figure 26. Load-Write-Mask-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION



† Load-write-mask-register cycle puts the device into the persistent write-per-bit mode.

Figure 27. Load-Write-Mask-Register-Cycle Timing (Late-Write Load)

PARAMETER MEASUREMENT INFORMATION

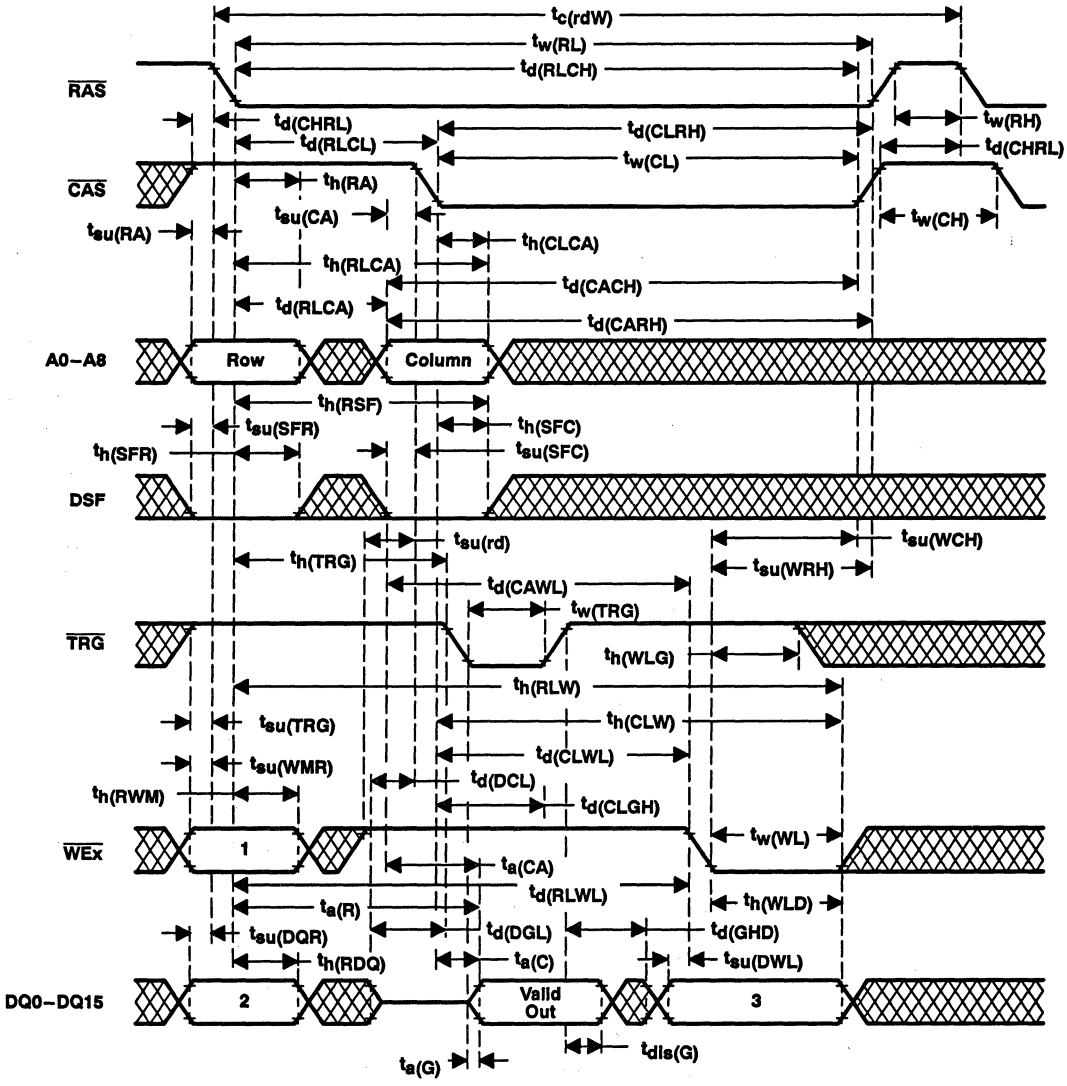
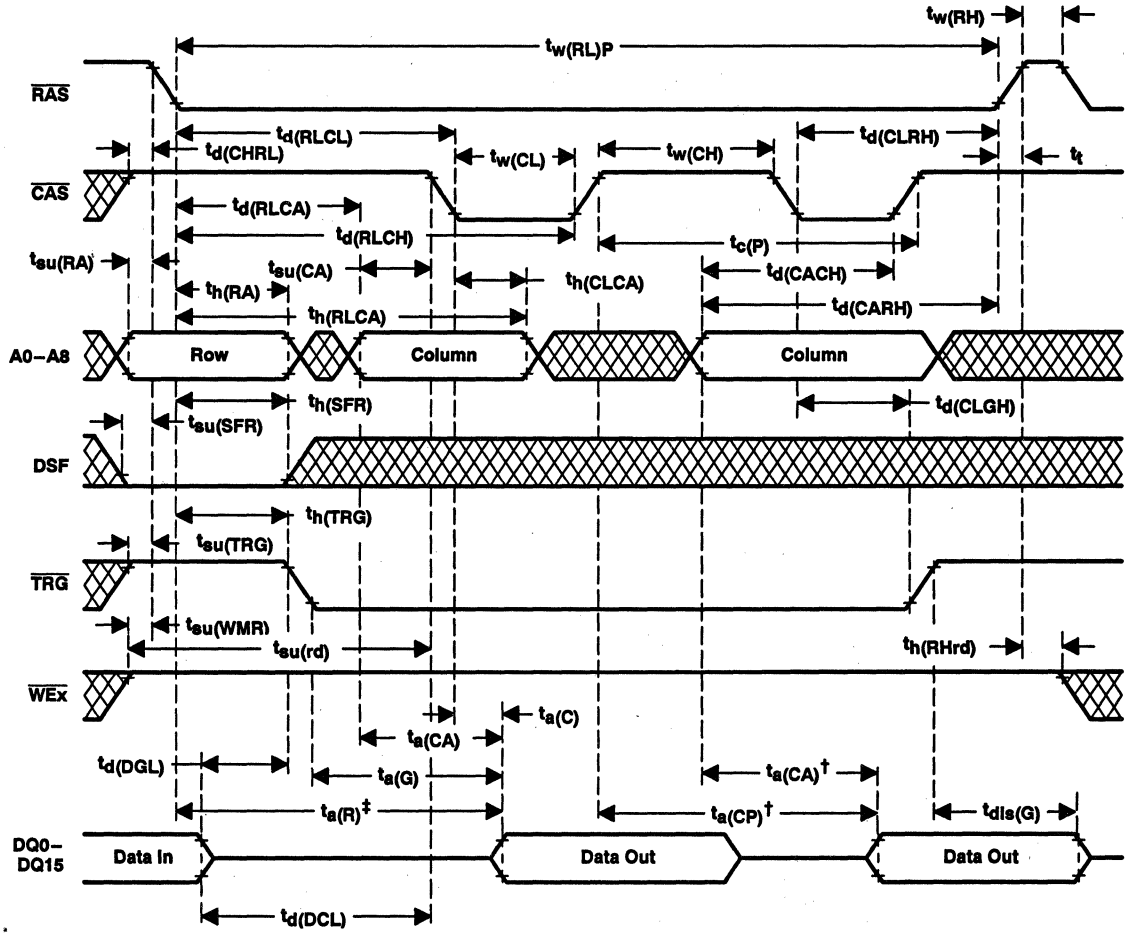


Figure 28. Read-Write-/Read-Modify-Write-Cycle Timing

Table 8. Read-Write-/Read-Modify-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

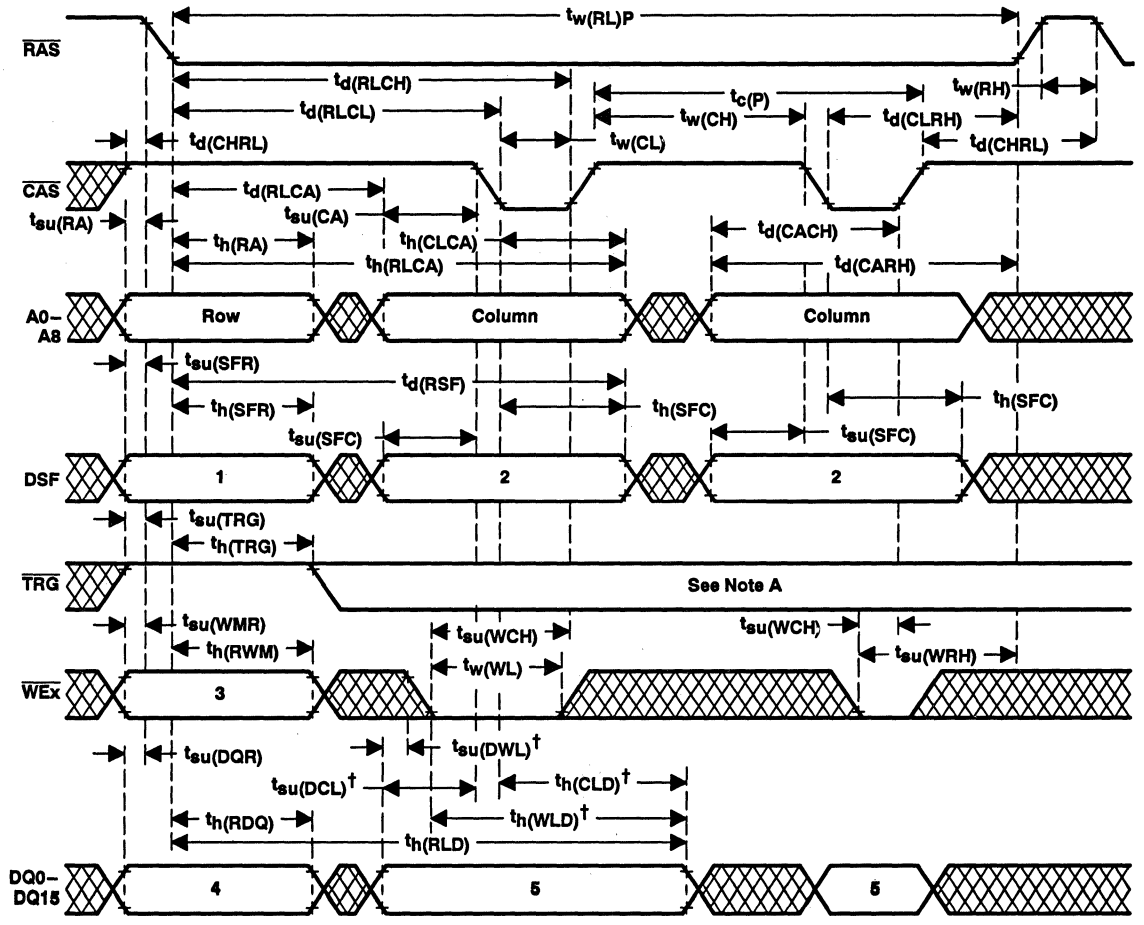
PARAMETER MEASUREMENT INFORMATION



† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.).

Figure 29. Enhanced-Page-Mode Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later

NOTE A: A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used. If the early write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

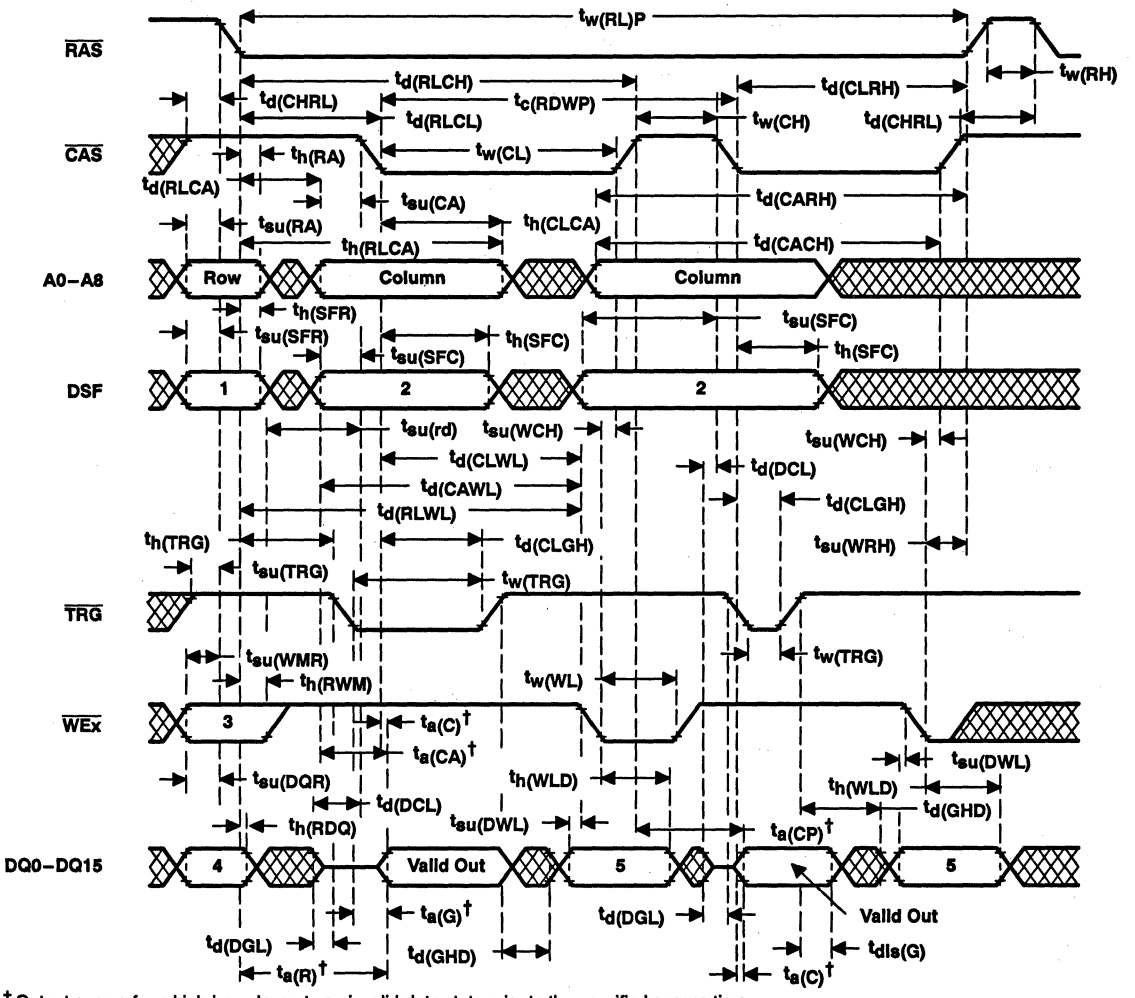
Figure 30. Enhanced-Page-Mode Write-Cycle Timing

Table 9. Enhanced-Page-Mode Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load write-mask register on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load-write-mask-register cycle sets the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CAS}$ is a don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



† Output can go from high-impedance to an invalid-data state prior to the specified access time.

NOTE A: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 31. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

Table 10. Enhanced-Page-Mode Read-Modify-Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load write-mask register on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load-write-mask register cycle sets the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CAS}$ is a don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION

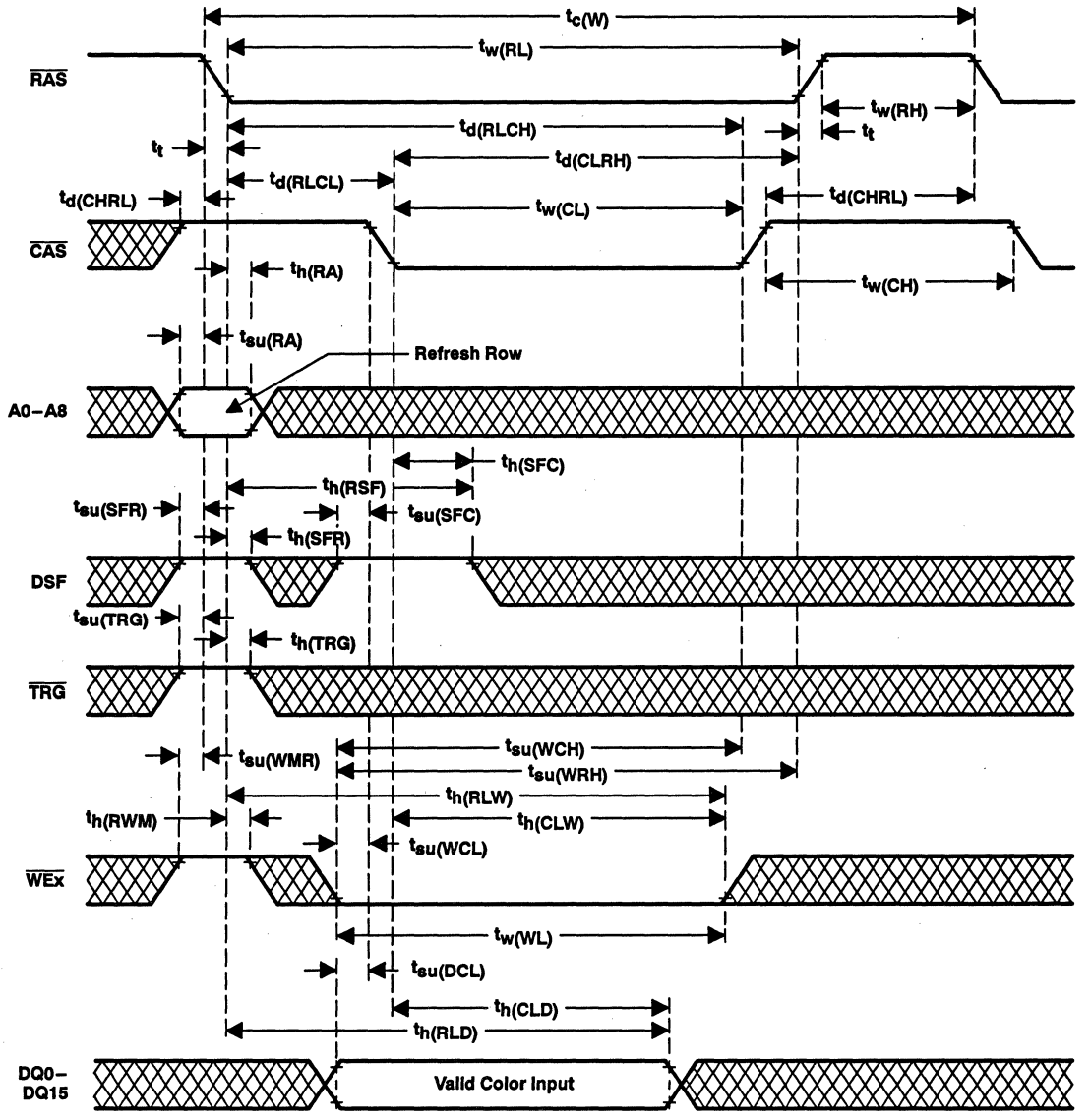


Figure 32. Load-Color-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION

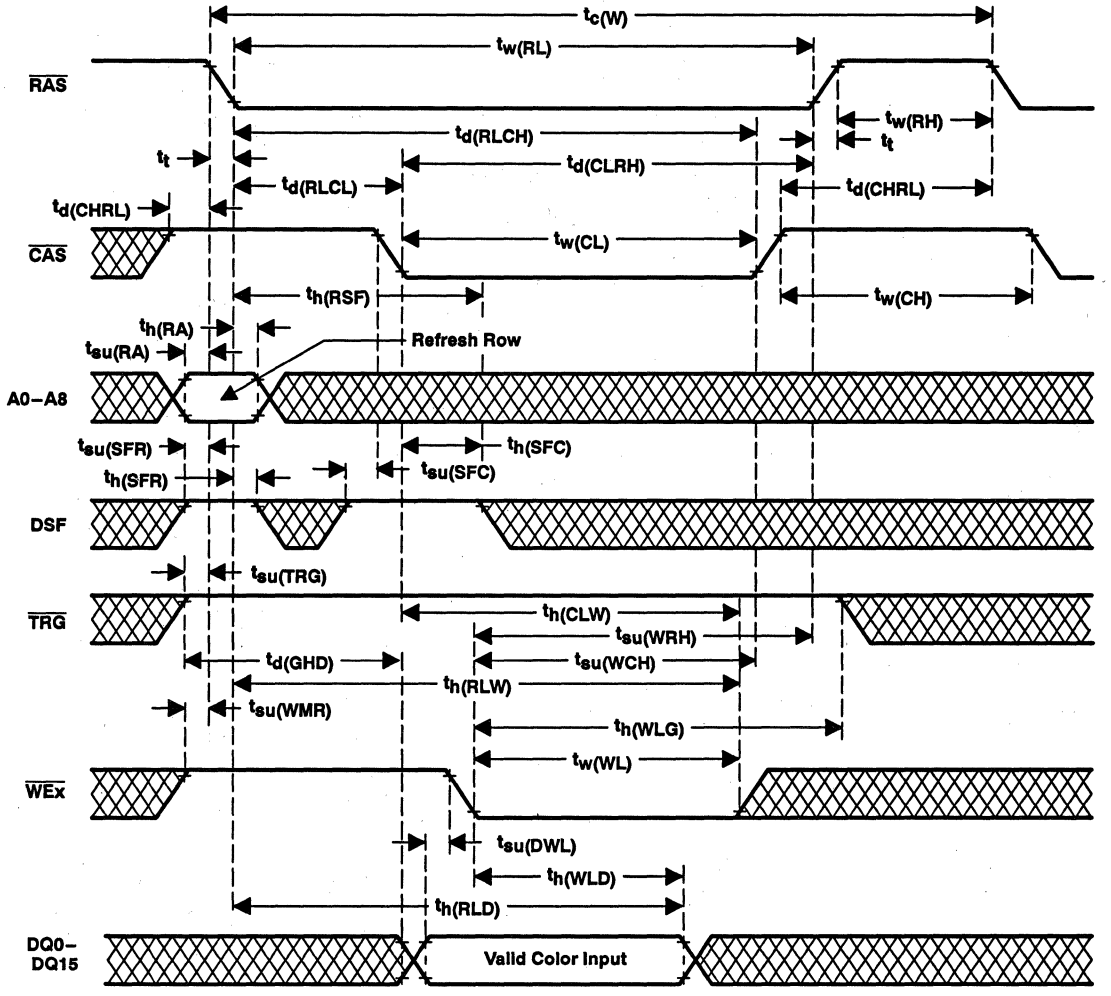


Figure 33. Load-Color-Register-Cycle Timing (Late-Write Load)

PARAMETER MEASUREMENT INFORMATION

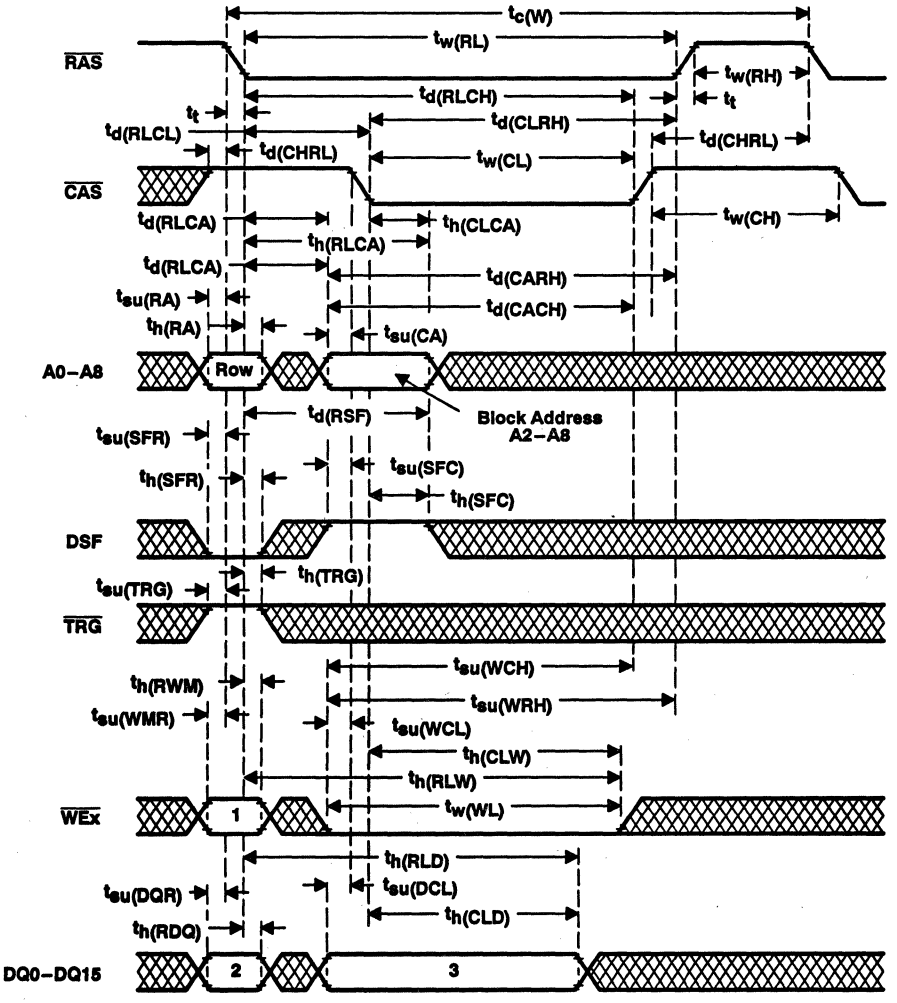


Figure 34. Block-Write-Cycle Timing (Early Write)

Table 11. Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi+3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

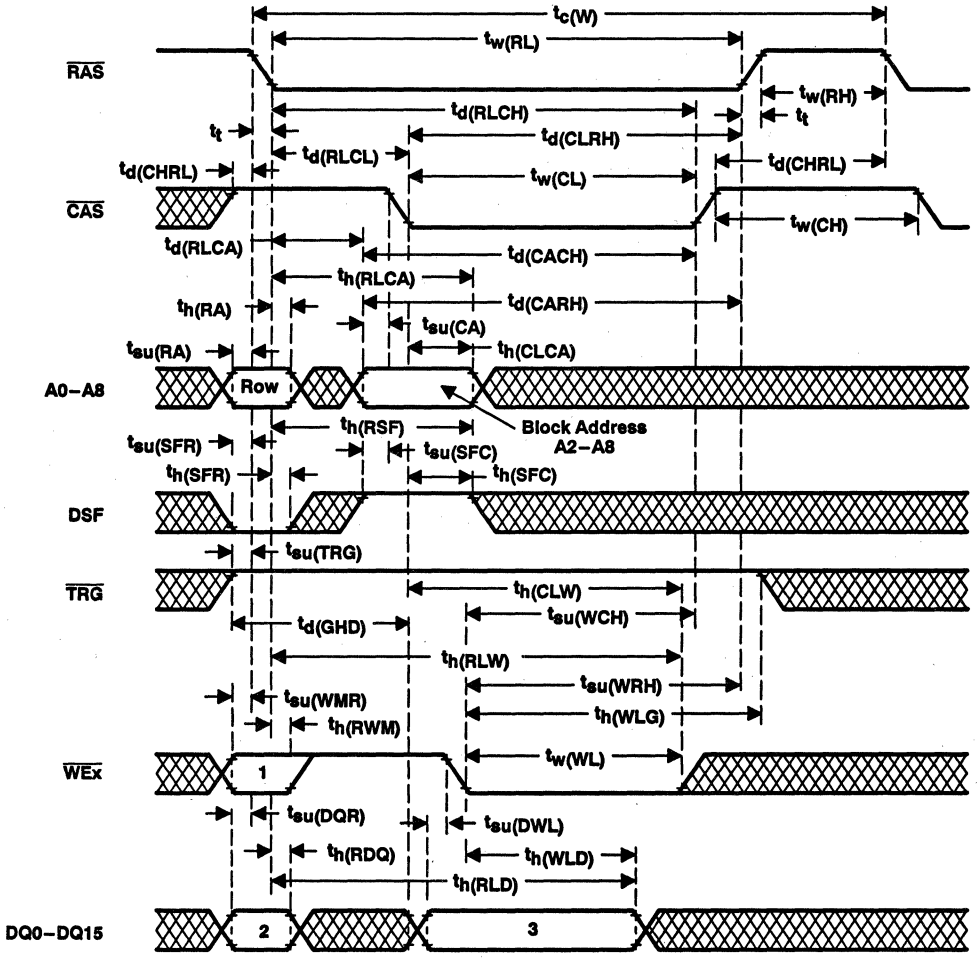


Figure 35. Block-Write-Cycle Timing (Late Write)

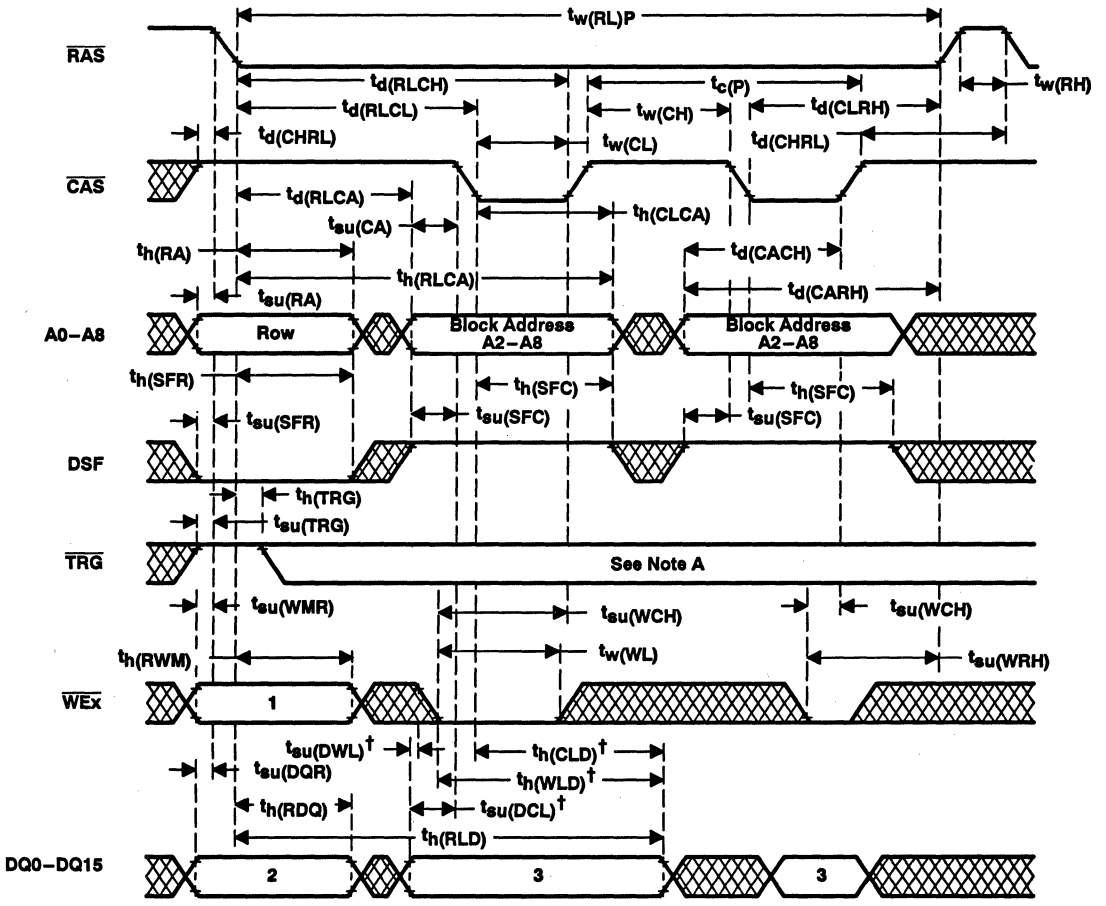
Table 12. Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable
Column-mask data DQi – DQi+3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later

NOTE A: To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used. If the early-write-cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 36. Enhanced-Page-Mode Block-Write-Cycle Timing

Table 13. Enhanced-Page-Mode Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi+3 (i = 0, 4, 8, 12) 0: column write disable 1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

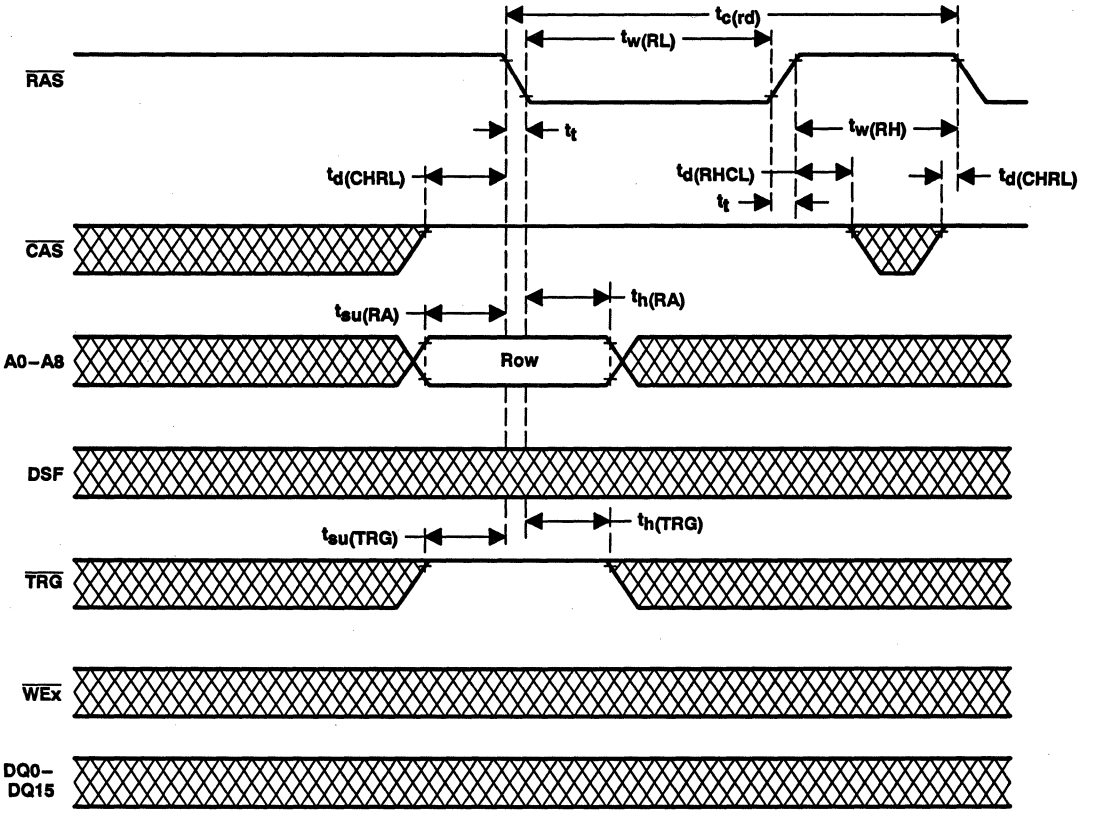


Figure 37. $\overline{\text{RAS}}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

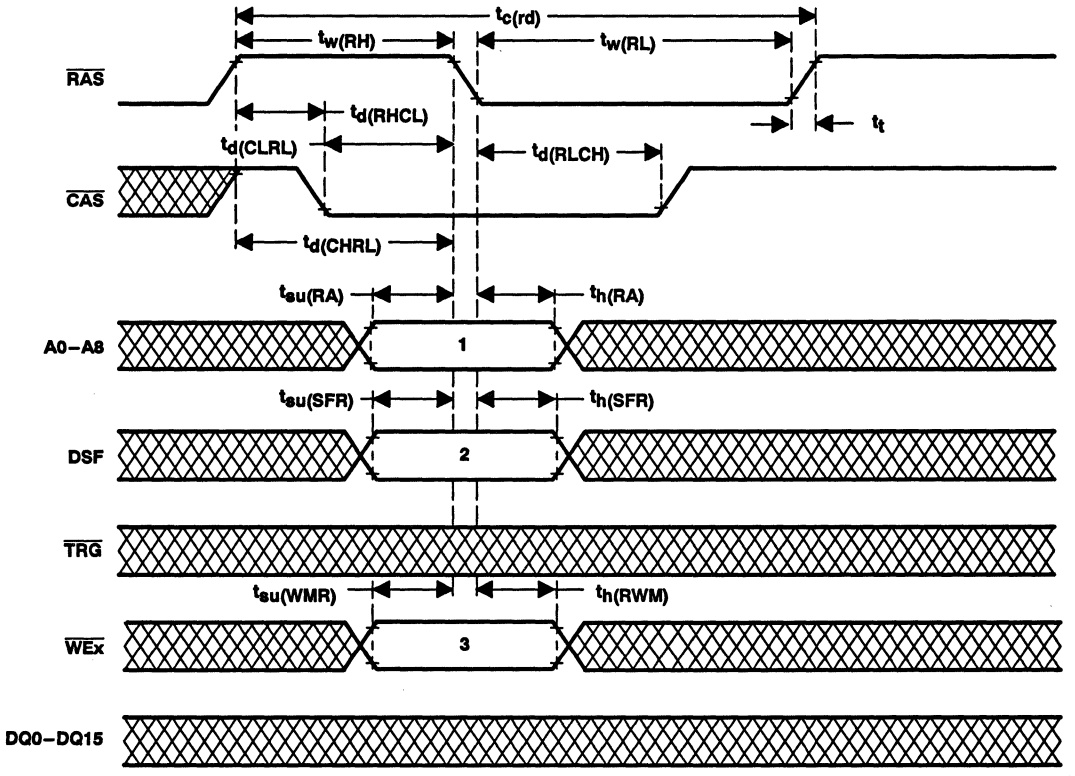


Figure 38. CBR-Refresh-Cycle Timing

Table 14. CBR-Cycle State Table

CYCLE	STATE		
	1	2	3
CBR refresh with option reset	Don't care	L	H
CBR refresh with no reset	Don't care	H	H
CBR refresh with stop point set and no reset	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION

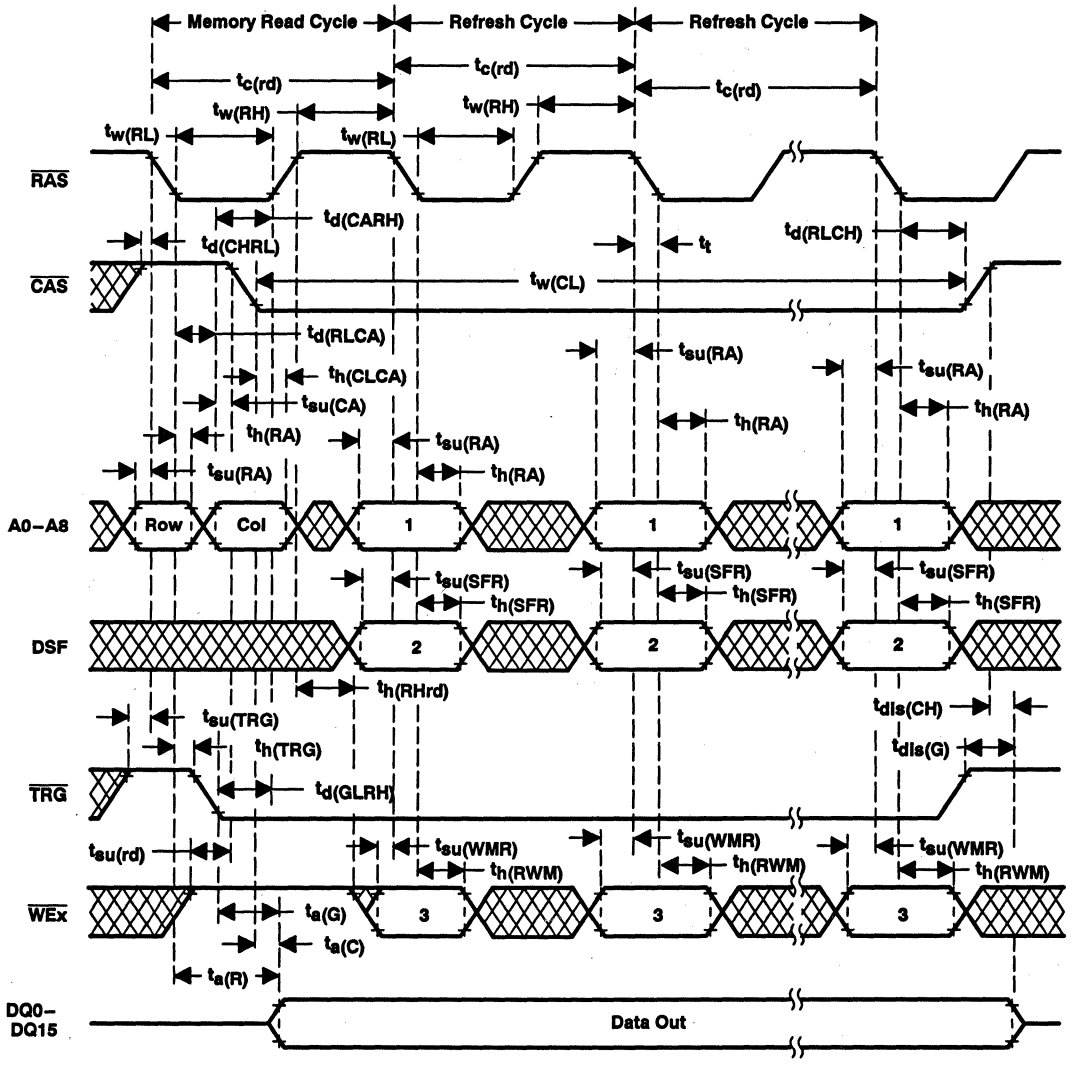
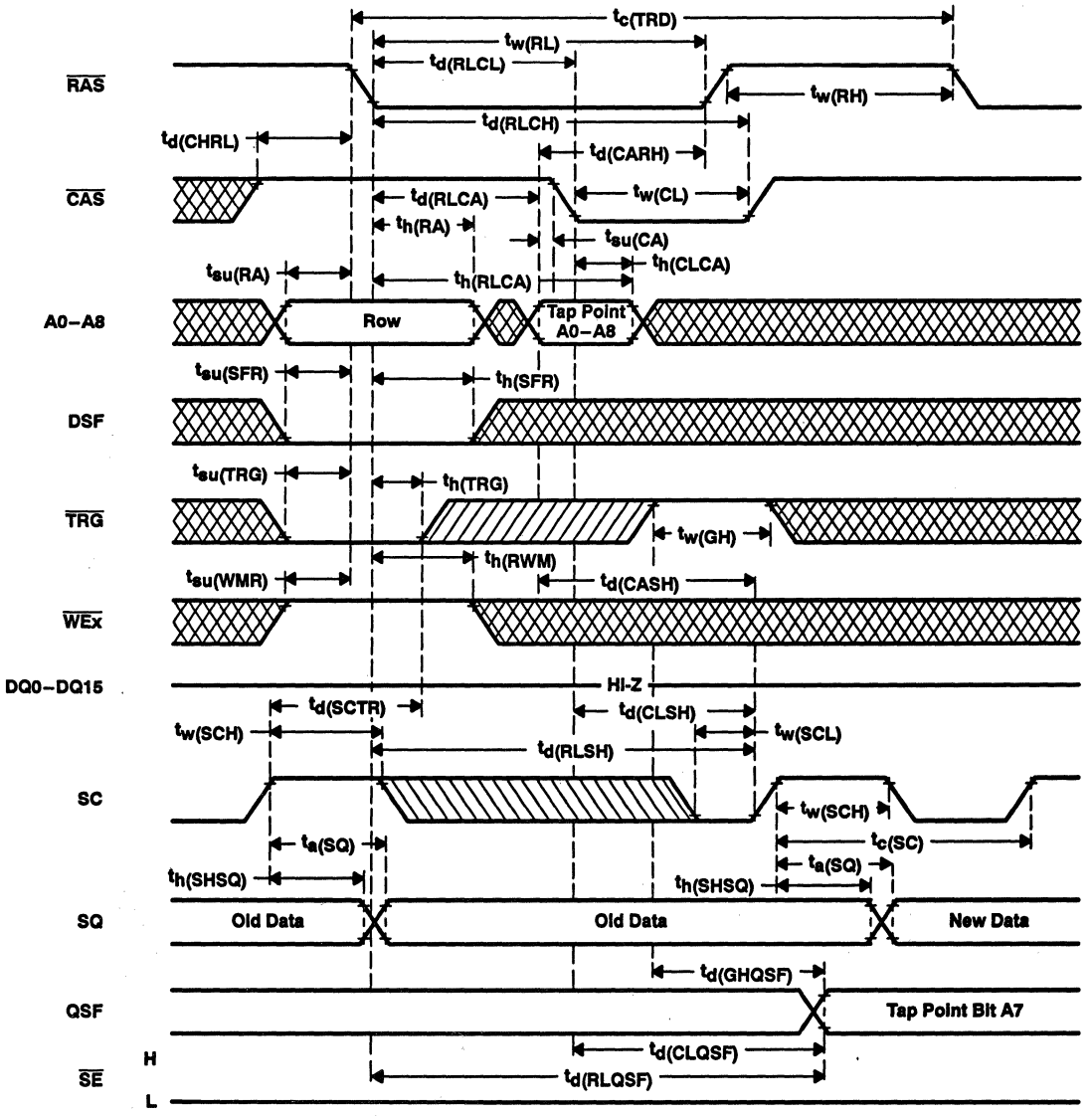


Figure 39. Hidden-Refresh-Cycle Timing

Table 15. Hidden-Refresh-Cycle State Table

CYCLE	STATE		
	1	2	3
CBR refresh with option reset	Don't care	L	H
CBR refresh with no reset	Don't care	H	H
CBR refresh with stop point set and no option reset	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register-transfer cycle. The memory-to-data-register-transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

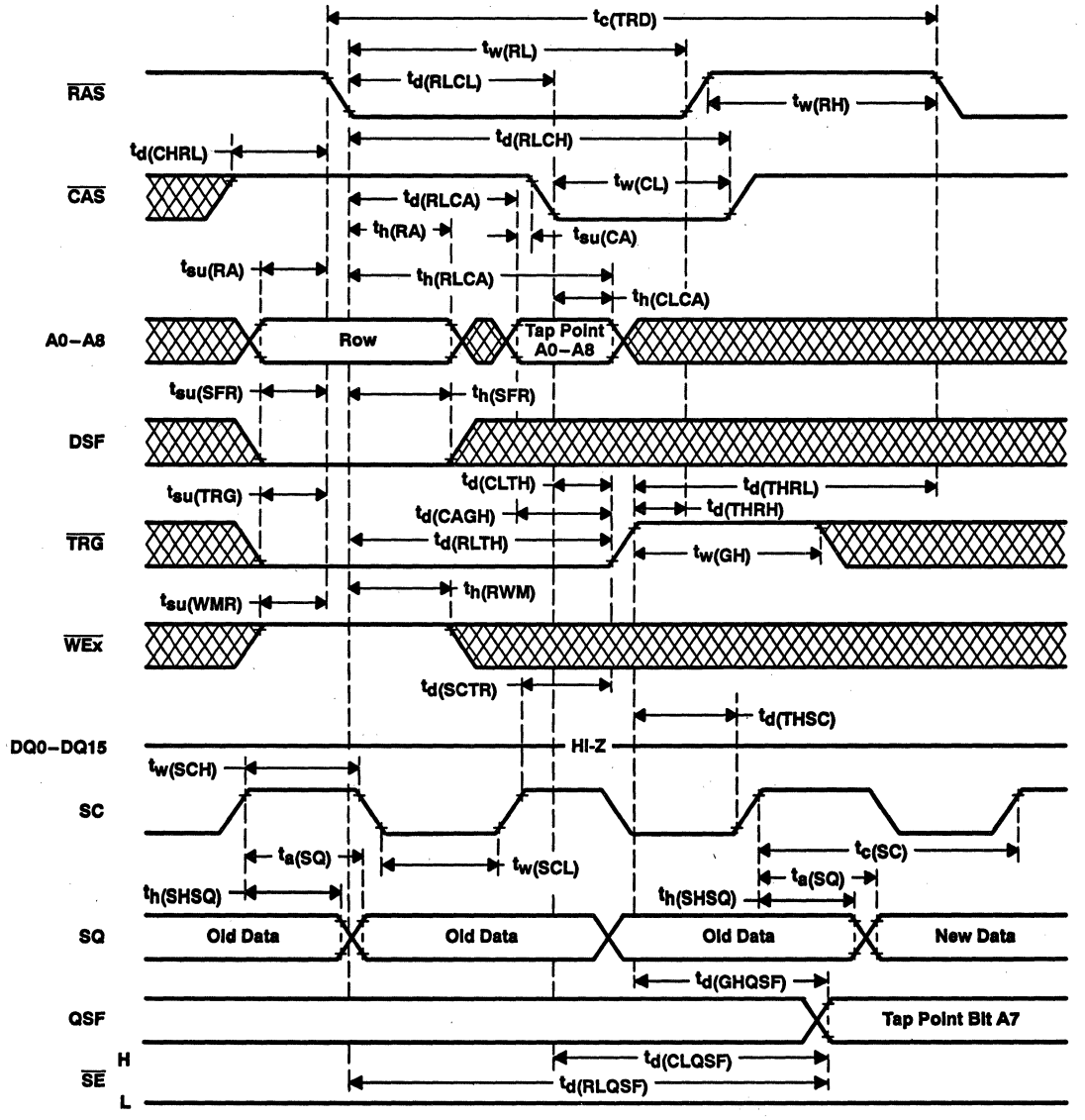
B. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0–A7: register tap point; A8: which half of the transferred row

D. Early-load operation is defined as $t_{h(TRG)}$ min < $t_{h(TRG)}$ < $t_{d(RLTH)}$ min.

Figure 40. Full-Register-Transfer Read Timing, Early-Load Operations

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Random-mode (DQ) outputs remain in the high-impedance state for the entire memory-to-data-register-transfer cycle. The memory-to-data-register-transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

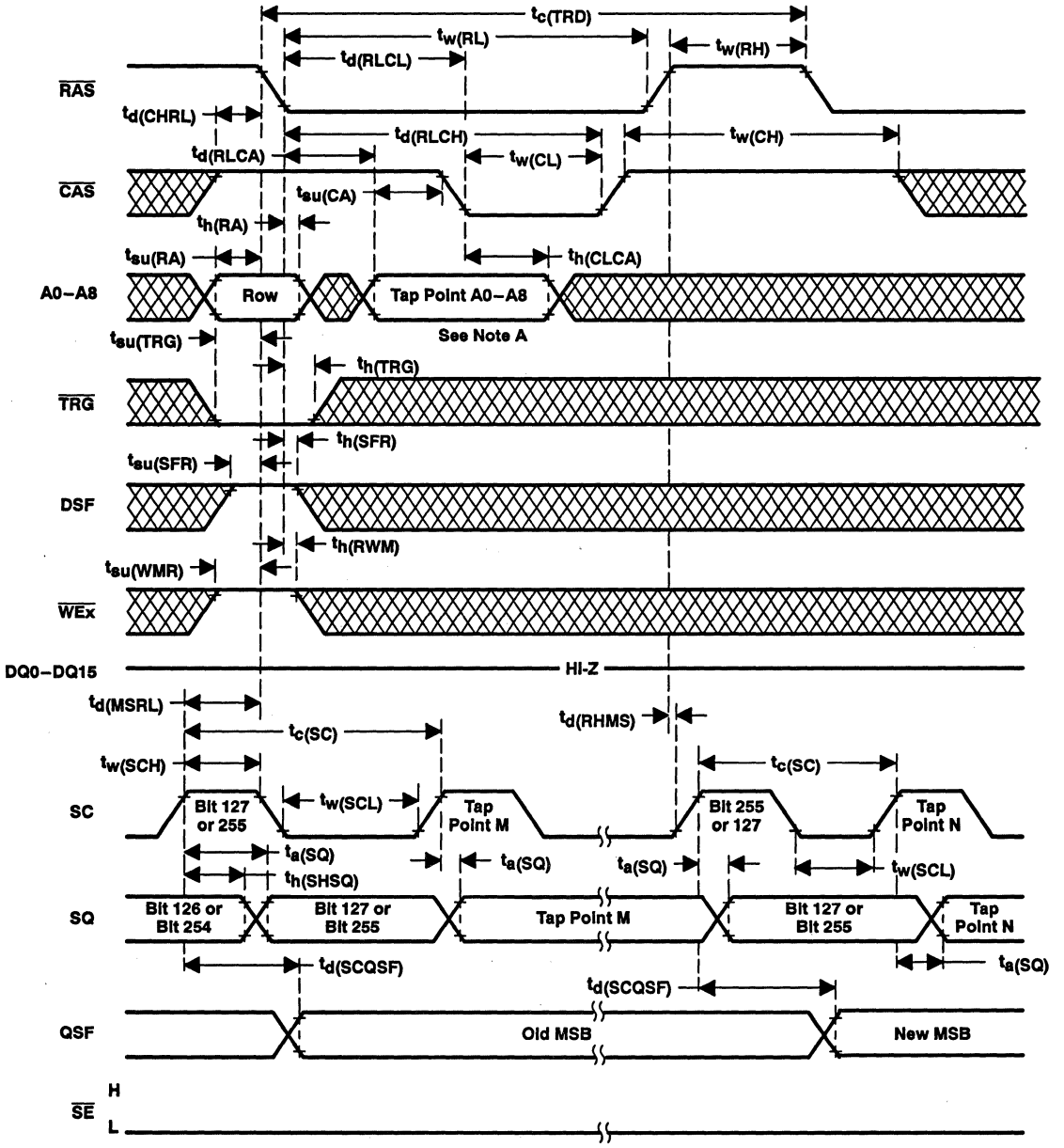
B. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0–A7: register tap point; A8: which half of the transferred row

D. Late load operation is defined as $t_{d(THRH)} < 0$ ns.

Figure 41. Full-Register-Transfer Read Timing, Real-Time Load Operation/Late-Load Operation

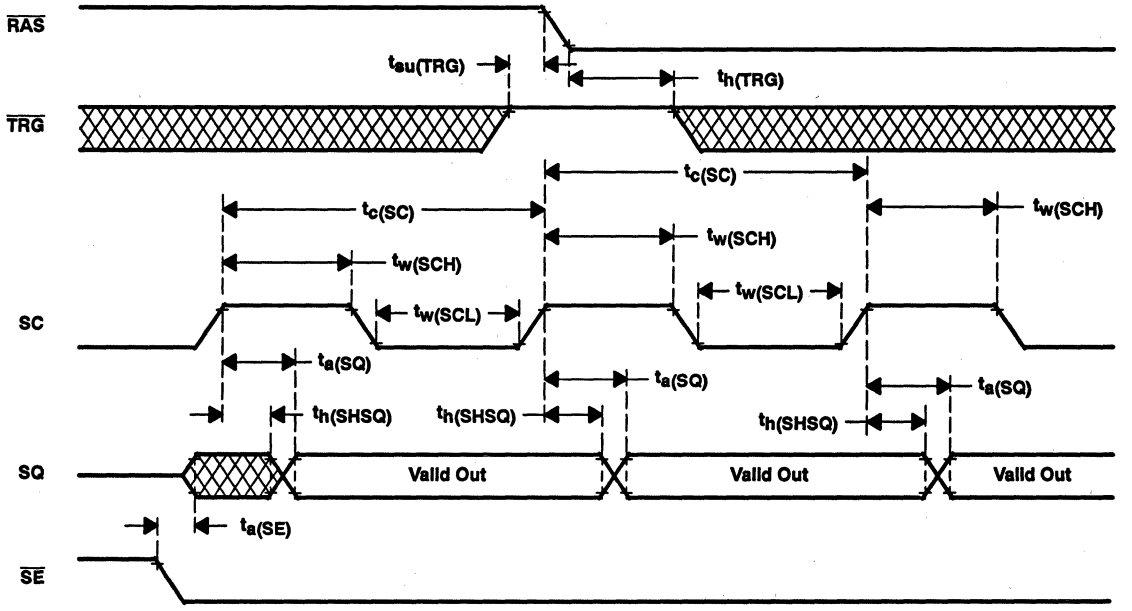
PARAMETER MEASUREMENT INFORMATION



NOTE A: A0–A6: tap point of the given half; A7: don't care; A8: identifies the DRAM row half

Figure 42. Split-Register-Transfer Read Timing

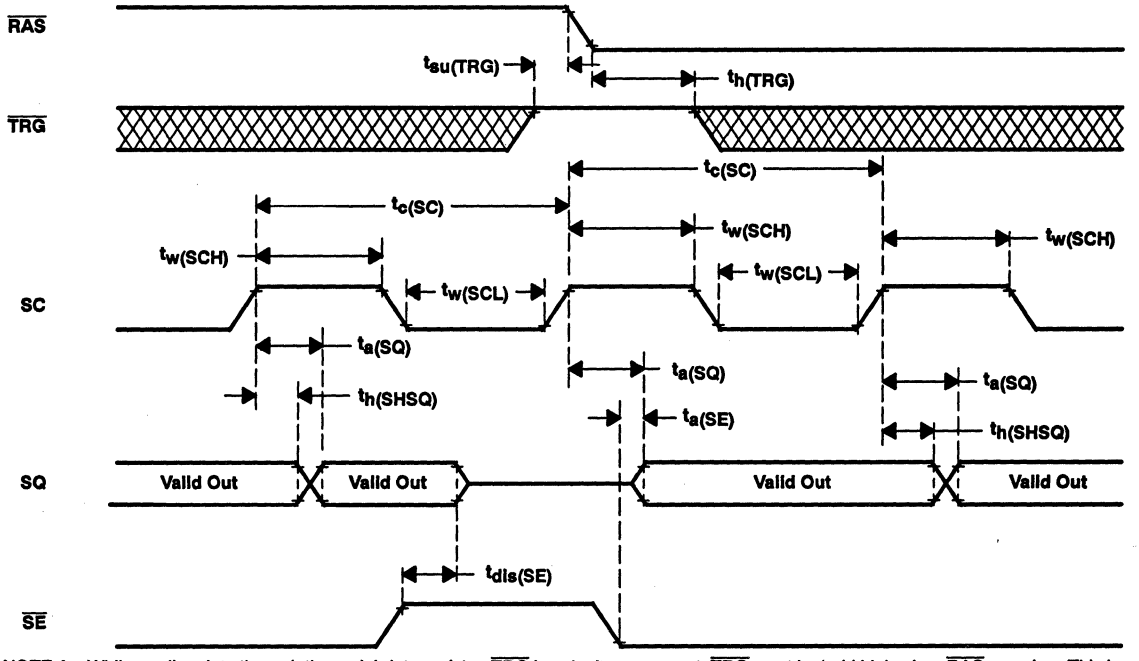
PARAMETER MEASUREMENT INFORMATION



NOTE A: While reading data through the serial-data register, $\overline{TRG}$ is a don't care except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

Figure 43. Serial-Read Timing ($\overline{SE}$ = V_{IL})

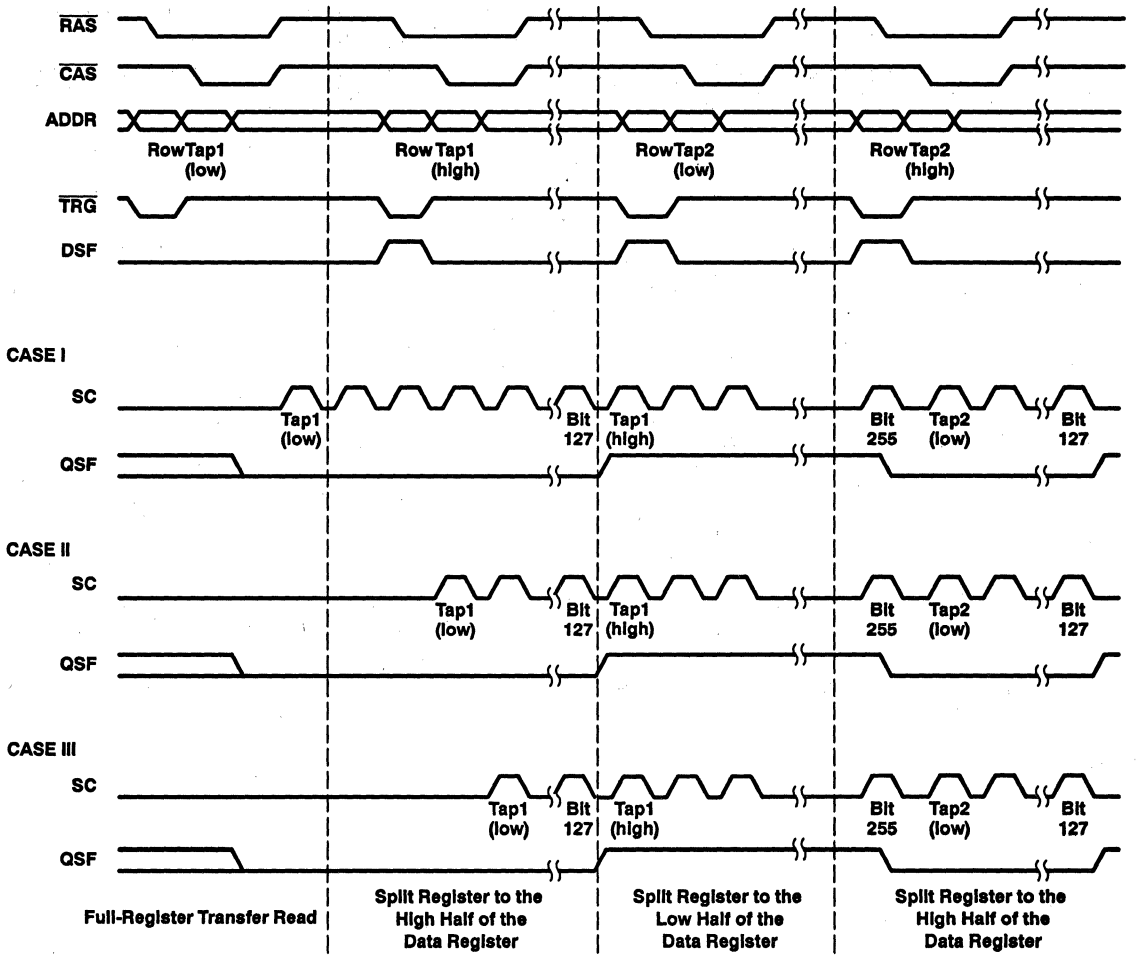
PARAMETER MEASUREMENT INFORMATION



NOTE A: While reading data through the serial-data register, $\overline{TRG}$ is a don't care except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

Figure 44. Serial-Read Timing ($\overline{SE}$-Controlled Read)

PARAMETER MEASUREMENT INFORMATION

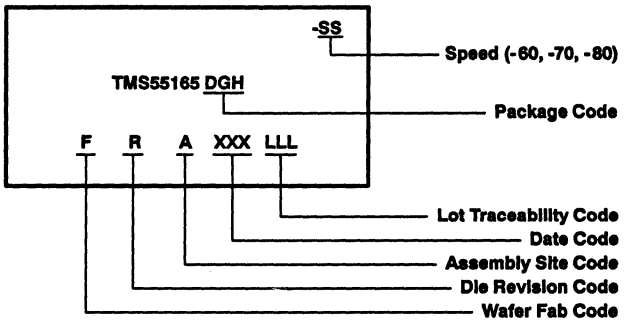


NOTES: A. In order to achieve proper split-register operation, a full-register transfer read should be performed before the first split-register transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can then begin either after the full-register transfer-read cycle (CASE I), during the first split-register transfer cycle (CASE II), or even after the first split-register transfer cycle (CASE III). There is no minimum requirement of SC clock between the full-register transfer-read cycle and the first split-register cycle.

B. A split-register transfer into the inactive half is not allowed until $t_{d(MSRL)}$ is met. $t_{d(MSRL)}$ is the minimum delay time between the rising edge of the serial clock of the last bit (bit 127 or 255) and the falling edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half. After the $t_{d(MSRL)}$ is met, the split-register transfer into the inactive half must also satisfy the minimum $t_{d(RHMS)}$ requirement. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 127 or 255).

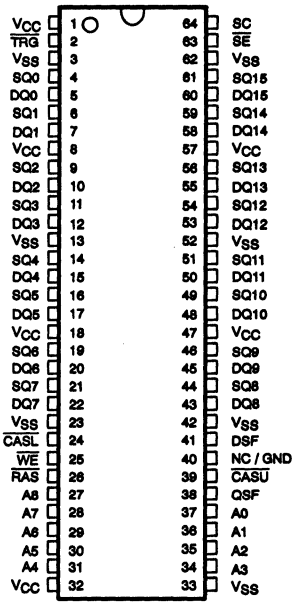
Figure 45. Split-Register Operating Sequence

device symbolization



- **Organization:**
  - **DRAM: 262144 Words × 16 Bits**
  - **SAM: 256 Words × 16 Bits**
- **Dual-Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Data Transfer Function From the DRAM to the Serial Data Register**
- **(4 × 4) × 4 Block-Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle From the 16-Bit On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O. Two Write-Per-Bit Modes to Simplify System Design**
- **Byte Write Control ($\overline{CASL}$, $\overline{CASU}$) Provides Flexibility**
- **Extended Data Output for Faster System Cycle Time**
- **Enhanced Page-Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) and Hidden Refresh Modes**
- **Long Refresh Period**
  Every 8 ms (Max)
- **Up to 55-MHz Uninterrupted Serial Data Streams**
- **256 Selectable Serial-Register Starting Locations**
- **$\overline{SE}$-Controlled Register-Status QSF**
- **Split-Register Transfer Read for Simplified Real-Time Register Load**
- **Programmable Split-Register Stop Point**
- **3-State Serial Outputs Allow Easy Multiplexing of Video Data Streams**
- **All Inputs/Outputs and Clocks TTL Compatible**
- **Compatible With JEDEC Standards**
- **Texas Instruments EPIC™ Process**
- **Designed to Work With the Industry-Leading Texas Instruments Graphics Family**
- **Performance Ranges:**

DGH PACKAGE
(TOP VIEW)



PIN NOMENCLATURE

A0–A8	Address Inputs
$\overline{CASL}$, $\overline{CASU}$	Column-Address Strobe/Byte Selects
DQ0–DQ15	DRAM Data I/O, Write Mask Data
DSF	Special Function Select
NC/GND	No Connect/Ground (Important: not connected internally to V_{SS})
QSF	Special Function Output
$\overline{RAS}$	Row-Address Strobe
SC	Serial Clock
$\overline{SE}$	Serial Enable
SQ0–SQ15	Serial Data Output
$\overline{TRG}$	Output Enable, Transfer Select
V_{CC}	5-V Supply (TYP)
V_{SS}	Ground
$\overline{WE}$	DRAM Write Enable Select

	ACCESS TIME ROW ENABLE $t_{a(R)}$ (MAX)	ACCESS TIME SERIAL DATA $t_{a(SQ)}$ (MAX)	DRAM CYCLE TIME $t_{c(W)}$ (MIN)	DRAM PAGE MODE $t_{c(P)}$ (MIN)	SERIAL CYCLE TIME $t_{c(SC)}$ (MIN)	OPERATING CURRENT SERIAL PORT STANDBY I_{CC1} (MAX)	OPERATING CURRENT SERIAL PORT ACTIVE I_{CC1A} (MAX)
TMS55161-60	60 ns	15 ns	110 ns	30 ns	18 ns	180 mA	225 mA
TMS55161-70	70 ns	20 ns	130 ns	30 ns	22 ns	165 mA	205 mA
TMS55161-80	80 ns	25 ns	150 ns	35 ns	30 ns	150 mA	185 mA

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description

The TMS55161 multiport video RAM is a high-speed dual-ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262144 words of 16 bits each interfaced to a serial data register [serial-access memory (SAM)] organized as 256 words of 16 bits each. The TMS55161 supports three basic types of operation: random access to and from the DRAM, serial access from the serial register, and transfer of data from any row in the DRAM to the serial register. Except during transfer operations, the TMS55161 can be accessed simultaneously and asynchronously from the DRAM and SAM ports.

The TMS55161 is equipped with several features designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's (4 × 4) × 4 block-write feature. The block-write mode allows 16 bits of data (present in an on-chip color data register) to be written to any combination of four adjacent column-address locations. As many as 64 bits of data can be written to memory during each $\overline{\text{CAS}}$ cycle time. Also on the DRAM port, a write mask or a write-per-bit feature allows masking of any combination of the 16 inputs/outputs on any write cycle. The persistent write-per-bit feature uses a mask register which, once loaded, can be used on subsequent write cycles without reloading. The TMS55161 also offers byte control. Byte control can be applied in read cycles, write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. The TMS55161 also offers extended output mode. The extended output mode is effective in both the page-mode cycles and standard cycles.

The TMS55161 offers a split-register-transfer read (DRAM to SAM) feature for the serial register (SAM port). This feature enables real-time register load implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. For applications not requiring real-time register load (for example, loads done during CRT retrace periods), the full-register mode of operation is retained to simplify system design.

The SAM port is designed for maximum performance. Data can be accessed from the SAM at serial rates up to 55 MHz. During the split-register-transfer read operations, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, QSF, is included to indicate which half of the serial register is active.

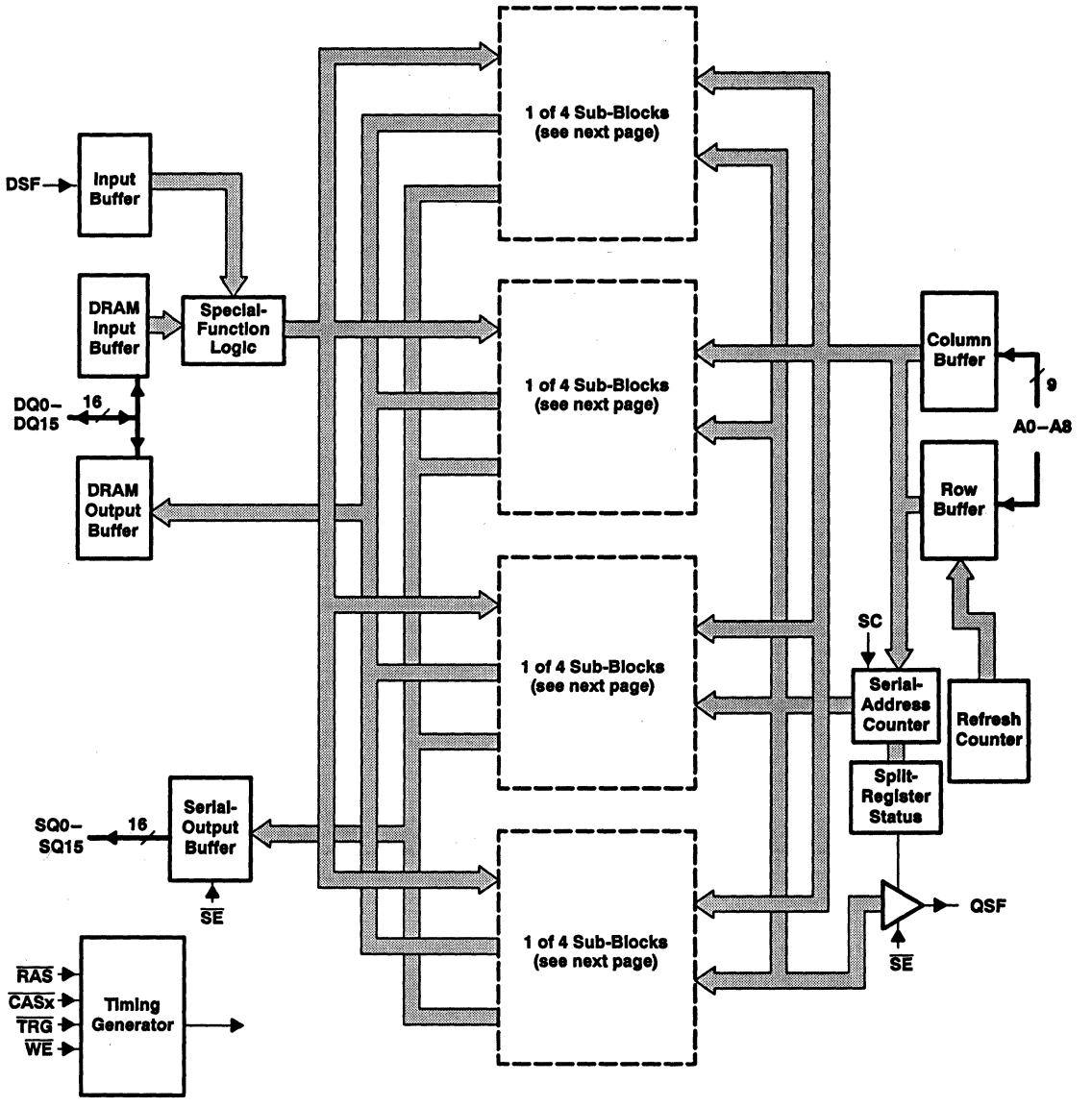
All inputs, outputs, and clock signals on the TMS55161 are compatible with Series 74 TTL. All address lines and data-in lines are latched on chip to simplify system design. All data outs are unlatched to allow greater system flexibility.

The TMS55161 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

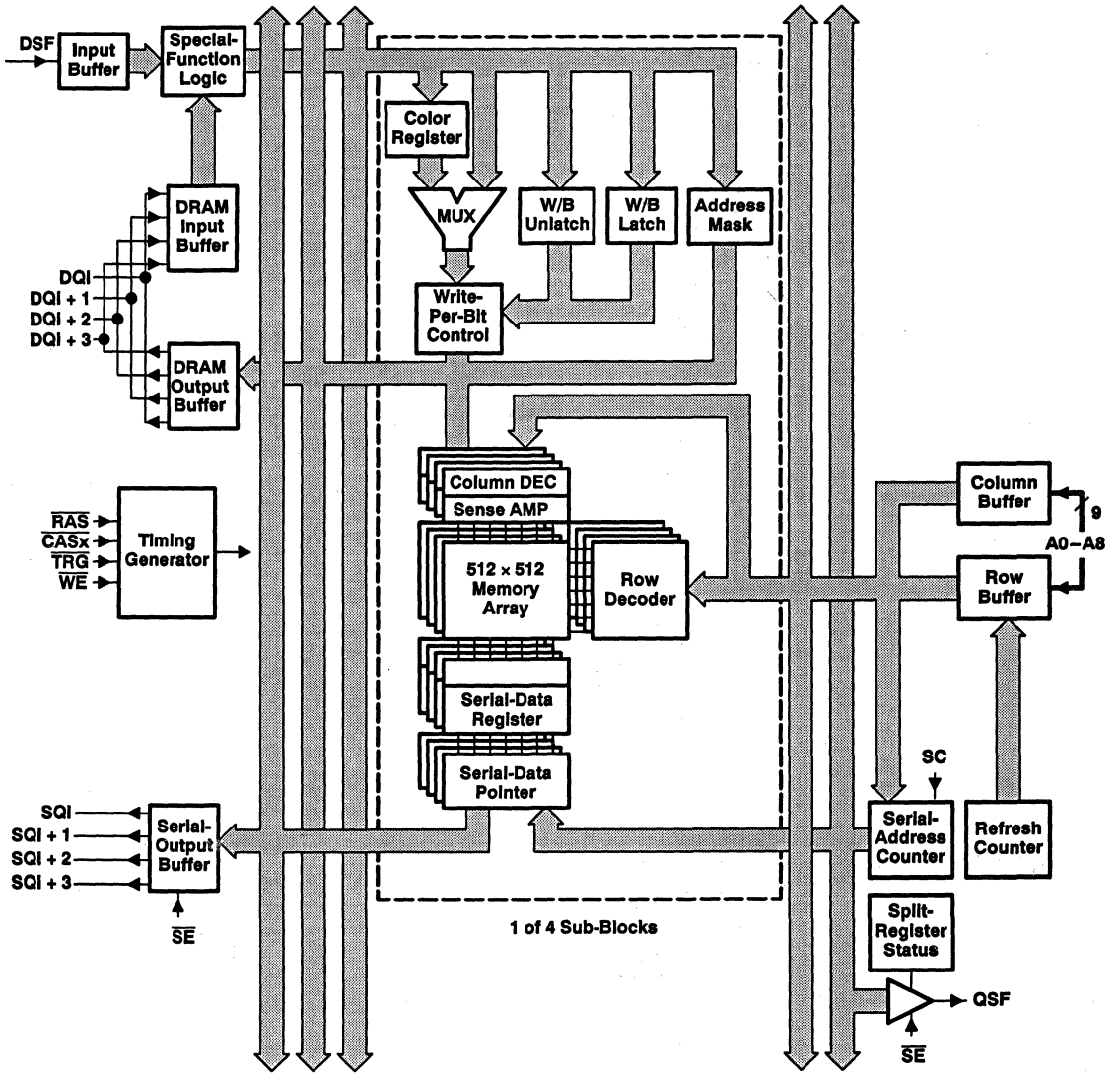
The TMS55161 is offered in a 64-pin small-outline gull-wing-leaded package (DGH suffix) for direct surface mounting.

The TMS55161 and other TI multiport video RAMs are supported by a broad line of graphics processors and control devices from Texas Instruments.

functional block diagram



functional block diagram (continued)



TEXAS INSTRUMENTS
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Table 1. Function Table

FUNCTION	RAS FALL				CASx FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CASx‡	TRG	WE	DSF	DSF	RAS	CASx§	RAS	CASL CASU WE	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)★	L	X	H	H	X	X	X	X	X	CBRN
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
Load write mask register □	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
X = Don't care
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled

† DQ0–DQ15 are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.
‡ Logic L is selected when either or both $\overline{CASL}$ and $\overline{CASU}$ are low.
§ The column address and block address are latched on the first falling edge of $\overline{CASx}$.
¶ CBRS cycle should be performed immediately after the power-up initialization cycle.
# A0–A3, A8: don't care; A4–A7 : stop-point code
‖ CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
★ CBR refresh (no reset) mode is not end persistent write-per-bit mode or stop-point mode.
□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.

Table 2. Pin Description Versus Operational Mode

PIN	DRAM	TRANSFER	SAM
A0 – A8	Row, column address	Row address, tap point	
$\overline{CASL}$ $\overline{CASU}$	Column-address strobe, DQ output enable	Tap-address strobe	
DQ	DRAM data I/O, Write mask		
DSF	Block-write enable Write-mask-register-load enable Color-register-load enable CBR (option reset)	Split-register-transfer enable	
$\overline{RAS}$	Row-address strobe	Row-address strobe	
$\overline{SE}$			SQ output enable, QSF output enable
SC			Serial clock
SQ			Serial data output
$\overline{TRG}$	DQ output enable	Transfer enable	
$\overline{WE}$	Write enable		
QSF			Serial-register status
NC/GND	Make no external connection or tie to system GND		
V_{CC}†	5-V supply		
V_{SS}†	Ground		

† For proper device operation, all V_{CC} pins must be connected to a 5-V supply and all V_{SS} pins must be tied to ground.

pin definitions

address (A0–A8)

Eighteen address bits are required to decode one of 262144 storage cell locations. Nine row-address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Nine column-address bits are set up on pins A0–A8 and latched onto the chip on the first falling edge of $\overline{CASx}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and the first falling edge of $\overline{CASx}$.

During the full-register-transfer read operation, the states of A0–A8 are latched on the falling edge of $\overline{RAS}$ to select one of the 512 rows where the transfer occurs. At the first falling edge of $\overline{CASx}$, the column-address bits A0–A8 are latched. The most significant column-address bit (A8) selects which half of the row is transferred to the SAM. The appropriate 8-bit column address (A0–A7) selects one of 256 tap points (starting positions) for the serial data output.

During the split-register-transfer read operation, address bit A7 is ignored at the falling edge of $\overline{CASx}$. An internal counter selects which half of the register is used. If the high half of the SAM is currently in use, the low half of the SAM is loaded with the low half of the DRAM half row, and vice versa. Column address (A8) selects the DRAM half row. The remaining seven address bits (A0–A6) are used to select 1 of 127 possible starting locations within the SAM. Locations 127 and 255 are not valid tap points.

row-address strobe ($\overline{RAS}$)

$\overline{RAS}$ is similar to a chip enable, so that all DRAM cycles and transfer cycles are initiated by the falling edge of $\overline{RAS}$. $\overline{RAS}$ is a control input that latches the states of the row address, $\overline{WE}$, $\overline{TRG}$, $\overline{CASL}$, $\overline{CASU}$, and DSF onto the chip to invoke DRAM and transfer read functions of the TMS55161.

column-address strobe ($\overline{CASL}$, $\overline{CASU}$)

$\overline{CASL}$ and $\overline{CASU}$ are control inputs that latch the states of the column address and DSF to control DRAM and transfer functions of the TMS55161. $\overline{CASx}$ also act as output enables for the DRAM output pins, DQ0–DQ15.

In DRAM operation, $\overline{CASL}$ enables data to be written to or read from the lower byte (DQ0–DQ7), and $\overline{CASU}$ enables data to be written to or from the upper byte (DQ8–DQ15).

In transfer operations, address bits A0–A8 are latched at the first falling edge of $\overline{CASx}$ as the start position (tap) for the serial data output (SQ0–SQ15).

output enable/transfer select ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either DRAM or transfer operation as $\overline{RAS}$ falls. For DRAM operation, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. During DRAM operation, $\overline{TRG}$ functions as an output enable for the DRAM output pins, DQ0–DQ15. For transfer operation, $\overline{TRG}$ must be brought low before $\overline{RAS}$ falls.

write mask select, write enable ($\overline{WE}$)

In DRAM operation, $\overline{WE}$ enables data to be written to the DRAM. $\overline{WE}$ is also used to select the DRAM write-per-bit mode of operation. Holding $\overline{WE}$ low on the falling edge of $\overline{RAS}$ invokes the write-per-bit operation. The TMS55161 supports both the nonpersistent write-per-bit mode and the persistent write-per-bit mode.

special function select (DSF)

The DSF input is latched on the falling edge of $\overline{RAS}$ or the first falling edge of $\overline{CASx}$ similar to an address. DSF determines which of the following functions are invoked on a particular cycle:

- CBR refresh with no reset (CBRN)
- CBR refresh with no reset and stop-point set (CBRS)
- Block write (BW, BWM)
- Loading write-mask register for the persistent write-per-bit mode (LMR)
- Loading color register for the block-write mode (LCR)
- Split-register-transfer read (SRT)

DRAM data I/O, write mask data (DQ0–DQ15)

DRAM data is written or read through the common I/O DQ pins. The 3-state DQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state as long as either $\overline{TRG}$ or $\overline{CASx}$ is held high. Data does not appear at the outputs until after both $\overline{CASx}$ and $\overline{TRG}$ have been brought low. The write mask is latched into the device via the random DQ pins by the falling edge of $\overline{RAS}$ and is used on all write-per-bit cycles. In a transfer operation, the DQ outputs remain in the high-impedance state for the entire cycle.

serial data outputs (SQ0–SQ15)

Serial data is read from the SQ pins. The SQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. The serial outputs are in the high-impedance (floating) state as long as the serial enable pin, $\overline{SE}$, is high. The serial outputs are enabled when $\overline{SE}$ is brought low.

serial clock (SC)

Serial data is accessed out of the data register from the rising edge of SC. The TMS55161 is designed to work with a wide range of clock duty cycles to simplify system design. There is no refresh requirement because the data registers that comprise the SAM are static. There is also no minimum SC operating frequency.

serial enable ($\overline{SE}$)

During serial-access operations, $\overline{SE}$ is used as an enable/disable for the SQ outputs. $\overline{SE}$ low enables the serial data output. $\overline{SE}$ high disables the serial data output. $\overline{SE}$ is also used as an enable/disable for output pin QSF.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is not disabled. External SC pulses increment the internal serial-address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low because the serial clock input buffer and the serial-address counter are not disabled by $\overline{SE}$.

special function output (QSF)

QSF is an output pin that indicates which half of the SAM is being accessed. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of the serial register (SAM). When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM.

During full-register-transfer operations, QSF can change state upon completing the cycle. This state is determined by the tap point loaded during the transfer cycle. The QSF output is enabled by $\overline{SE}$. If $\overline{SE}$ is high, the QSF output is in the high-impedance state.

no connect/ground (NC/GND)

The NC/GND pin should be tied to system ground or left floating for proper device operation.

functional operation description

random access operation

Table 3. DRAM Function Table

FUNCTION	$\overline{RAS}$ FALL				$\overline{CASx}$ FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	$\overline{CASx}$‡	$\overline{TRG}$	$\overline{WE}$	DSF	DSF	$\overline{RAS}$	$\overline{CASx}$§	$\overline{RAS}$	$\overline{CASL}$ $\overline{CASU}$ $\overline{WE}$	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop-point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)★	L	X	H	H	X	X	X	X	X	CBRN
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
Load write-mask register □	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
X = Don't care
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled

† DQ0–DQ15 are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.
‡ Logic L is selected when either or both $\overline{CASL}$ and $\overline{CASU}$ are low.
§ The column address and block address are latched on the first falling edge of $\overline{CASx}$.
¶ CBRS cycle should be performed immediately after the power-up initialization cycle.
# A0–A3, A8: don't care; A4–A7: stop-point code
‖ CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
★ CBR refresh (no reset) mode is not end persistent write-per-bit mode or stop-point mode.
□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.

enhanced page mode

Enhanced-page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. This mode eliminates the time required for row-address setup, row-address hold, and address multiplex. The maximum $\overline{RAS}$ low time and the minimum $\overline{CAS}$ page cycle time are used to determine the number of columns that can be accessed.

Unlike conventional page-mode operations, the enhanced page mode allows the TMS55161 to operate at a higher data bandwidth. Data retrieval begins as soon as the column address is valid rather than when $\overline{CASx}$ transitions low. A valid column address can be presented immediately after the row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CASx}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CASx}$ low) if $t_{a(CA)}$ max (access time from column address) has been satisfied.

refresh

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refreshes are accomplished by bringing either or both $\overline{CASL}$ and $\overline{CASU}$ low earlier than $\overline{RAS}$. The external row address is ignored, and the refresh row address is generated internally. Three types of CBR refresh cycles are available. The CBR refresh (option reset) ends the persistent write-per-bit mode and the stop-point mode. The CBRN and CBRS refreshes (no reset) do not end the persistent write-per-bit mode or the stop-point mode. The 512 rows of the DRAM do not necessarily need to be refreshed consecutively as long as the entire refresh is completed within the required time period, $t_{rf(MA)}$. The output buffers remain in the high-impedance state during the CBR refresh cycles regardless of the state of $\overline{TRG}$.

hidden refresh

A hidden refresh is accomplished by holding both $\overline{CASL}$ and $\overline{CASU}$ low in the DRAM read cycle and cycling $\overline{RAS}$. The output data of the DRAM read cycle remains valid while the refresh is being carried out. Like the CBR refresh, the refreshed row addresses are generated internally during the hidden refresh.

$\overline{RAS}$-only refresh

A $\overline{RAS}$-only refresh is accomplished by cycling $\overline{RAS}$ at every row address. Unless $\overline{CASx}$ and $\overline{TRG}$ are low, the output buffers remain in the high-impedance state to conserve power. Externally generated addresses must be supplied during $\overline{RAS}$-only refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed.

extended data output

The TMS55161 features extended data output during DRAM accesses. While $\overline{RAS}$ and $\overline{TRG}$ are low, the DRAM output remains valid even when $\overline{CASx}$ returns high. The output remains valid until $\overline{WE}$ is low, $\overline{TRG}$ is high, or both $\overline{CASx}$ and $\overline{RAS}$ are high. The extended-data-output mode functions in all read cycles including DRAM-read, page-mode-read, and read-modify-write cycles.

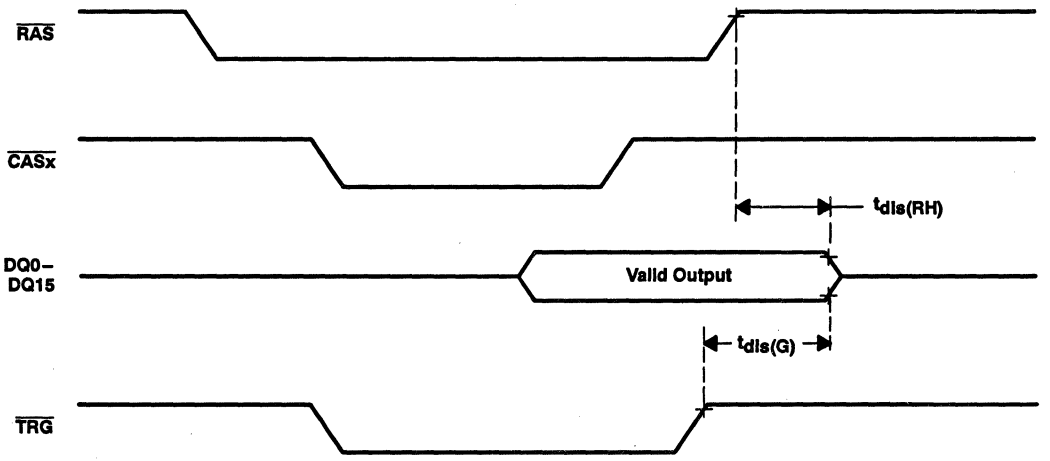

Figure 1. DRAM-Read Cycle With $\overline{RAS}$-Controlled Output

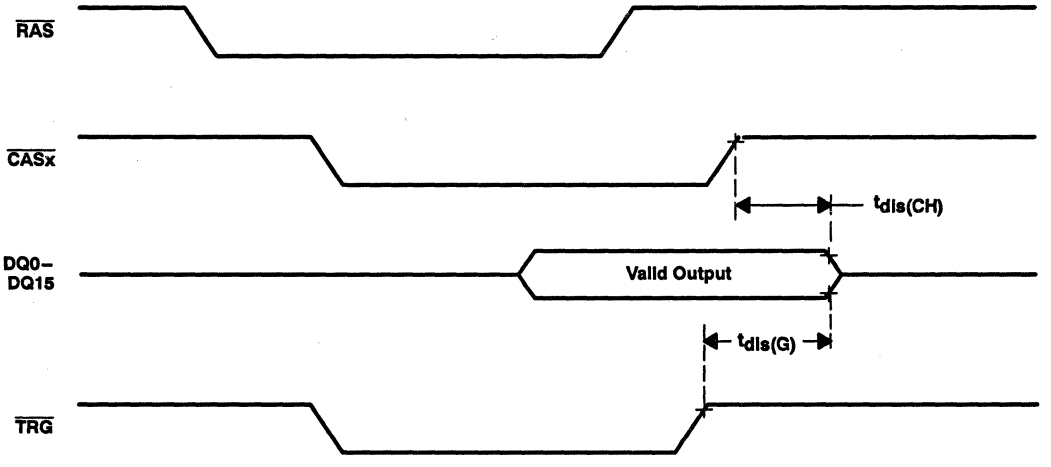

Figure 2. DRAM-Read Cycle With $\overline{CASx}$-Controlled Output

extended data output (continued)

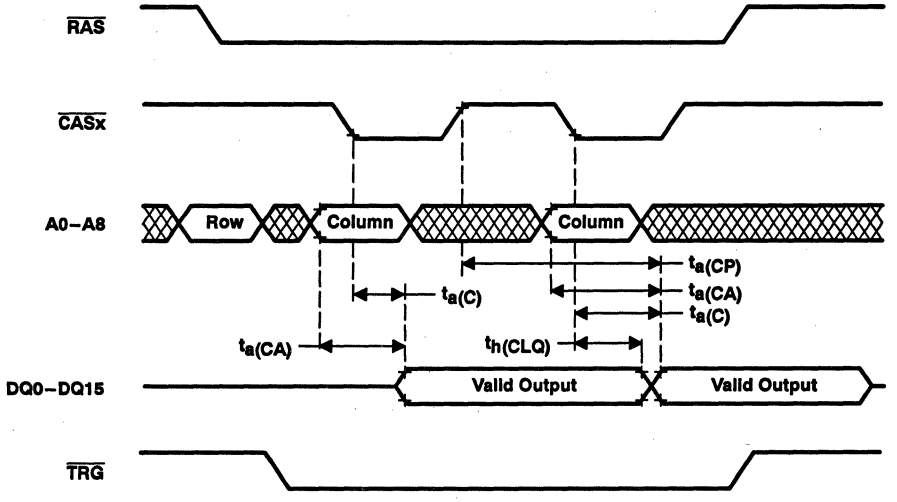

Figure 3. DRAM-Page-Read Cycle With Extended Output

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byte operation

Byte operation can be applied in DRAM read cycles, write cycles, block-write cycles, load-write-mask-register cycles and load-color-register cycles. In byte operation, the column address (A0–A8) is latched at the first falling edge of $\overline{CAS}$x. In read cycles, $\overline{CASL}$ enables the lower byte (DQ0–DQ7) and $\overline{CASU}$ enables the upper byte (DQ8–DQ15) (see Figure 4).

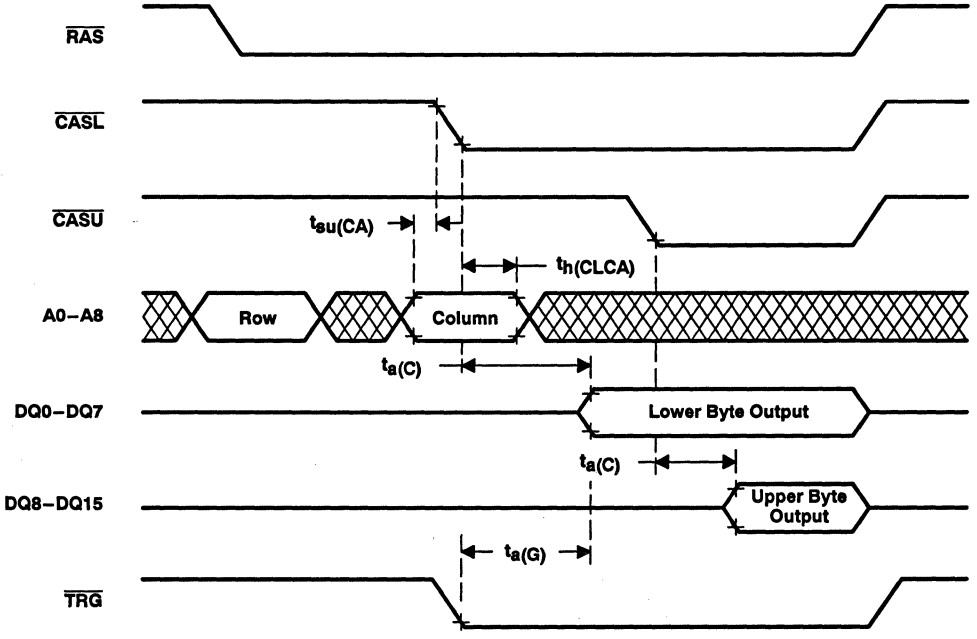


Figure 4. Example of a Byte-Read Cycle

byte operation (continued)

In byte-write operation, $\overline{CASL}$ enables data to be written to the lower byte (DQ0–DQ7) and $\overline{CASU}$ enables data to be written to the upper byte (DQ8–DQ15). In an early-write cycle, $\overline{WE}$ is brought low prior to both $\overline{CASx}$ signals. Data setup and hold times for DQ0–DQ15 are referenced to the first falling edge of $\overline{CASx}$ (see Figure 5).

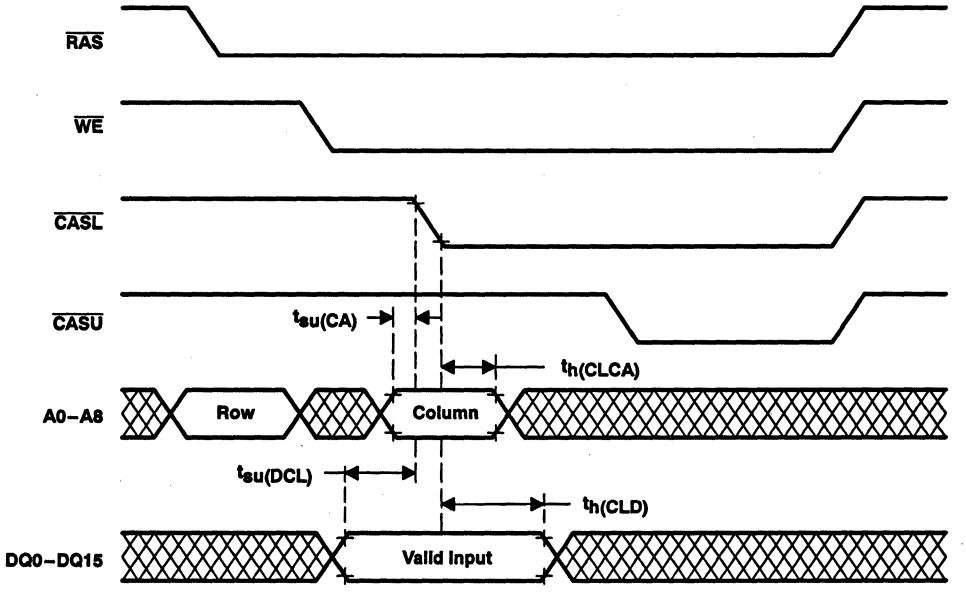


Figure 5. Example of an Early-Write Cycle

byte operation (continued)

For late-write or read-modify-write cycles, $\overline{WE}$ is brought low after either or both $\overline{CASL}$ and $\overline{CASU}$ fall. The data is strobed in with data setup and hold times for DQ0–DQ15 referenced to $\overline{WE}$ (see Figure 6).

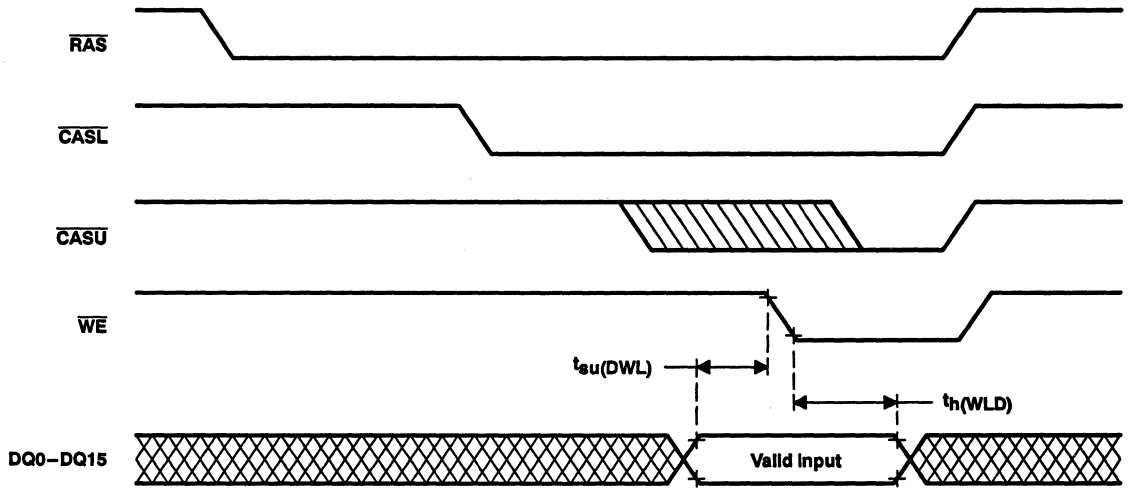


Figure 6. Example of a Late-Write Cycle

write-per-bit

The write-per-bit feature allows masking any combination of the 16 DQs on any write cycle. The write-per-bit operation is invoked when $\overline{WE}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{WE}$ is held high on the falling edge of $\overline{RAS}$, the write operation is performed without any masking. The TMS55161 offers two write-per-bit modes: the nonpersistent write-per-bit and the persistent write-per-bit.

nonpersistent write-per-bit

When $\overline{WE}$ is low on the falling edge of $\overline{RAS}$, the write mask is reloaded. A 16-bit binary code (the write-per-bit mask) is input to the device via the DQ pins and latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the 16 I/Os are to be written and which are not. After $\overline{RAS}$ has latched the on-chip write-per-bit mask, input data is driven onto the DQ pins and is latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. $\overline{CASL}$ enables the lower byte (DQ0–DQ7) to be written through the mask and $\overline{CASU}$ enables the upper byte (DQ8–DQ15) to be written through the mask. If a data low (write mask = 0) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data is not written to that I/O. If a data high (write mask = 1) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data is written to that I/O (see Figure 7).

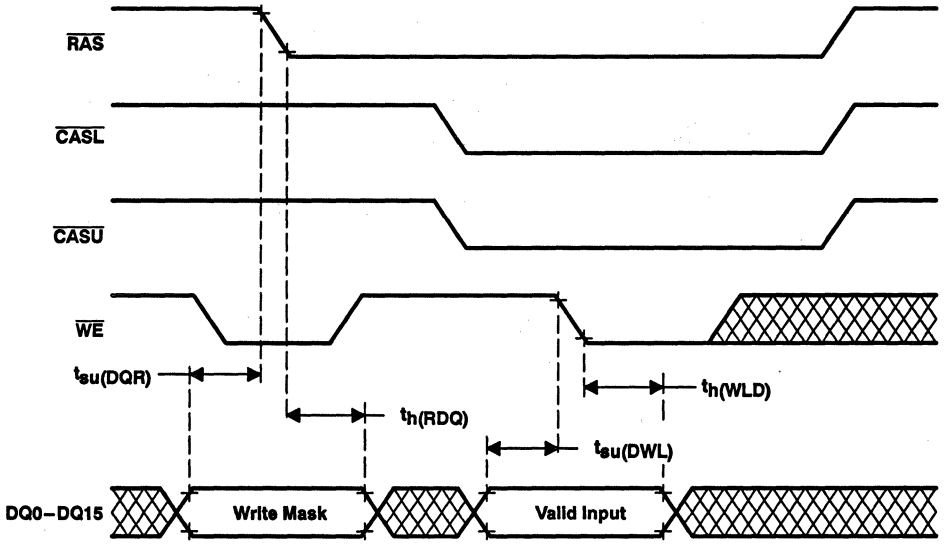


Figure 7. Example of a Nonpersistent Write-Per-Bit (Late-Write) Operation

persistent write-per-bit

The persistent write-per-bit mode is initiated only by performing a load-write-mask-register cycle first. In the persistent write-per-bit mode, the write-per-bit mask is not overwritten but remains valid over an arbitrary number of write cycles until another LMR cycle is performed or power is removed.

The load-write-mask-register cycle is performed using DRAM write-cycle timing except DSF is held high on the falling edge of $\overline{RAS}$ and held low on the first falling edge of $\overline{CASx}$. A binary code is input to the write-mask register via the random I/O pins and latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. Byte-write control can be applied to the write mask during the load-write-mask-register cycle. The persistent write-per-bit mode can then be used in exactly the same way as the nonpersistent write-per-bit mode except that the input data on the falling edge of $\overline{RAS}$ is ignored. When the device is set to the persistent write-per-bit mode, it remains in this mode and is reset only by a CBR refresh with option reset cycle (see Figure 8).

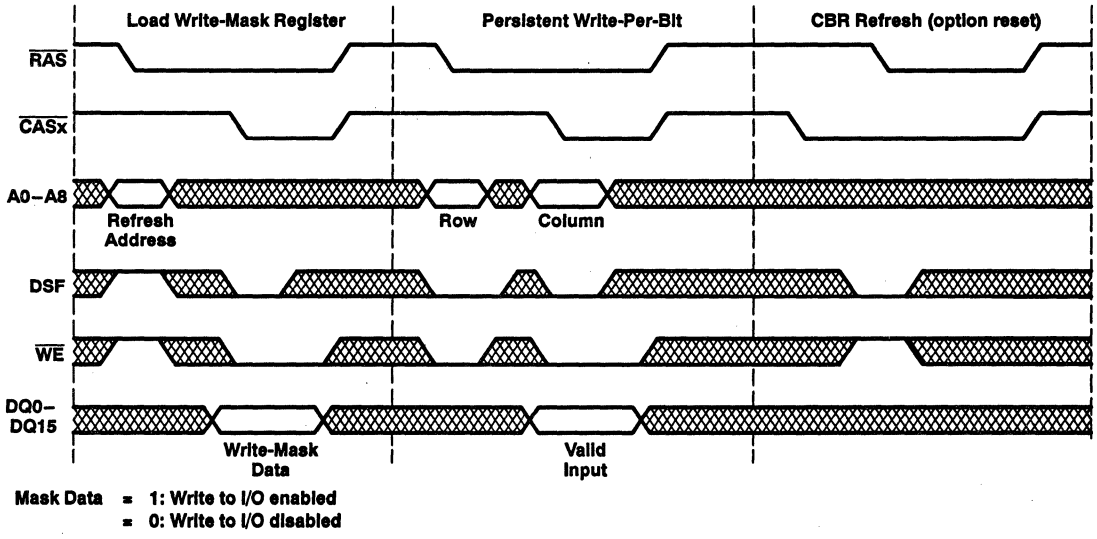


Figure 8. Example of a Persistent Write-Per-Bit Operation

block write

The block-write feature allows up to 64 bits of data to be written simultaneously to one row of the memory array. This function is implemented as (4 columns × 4 DQs) repeated in four quadrants. In this manner, each of the four one-megabit quadrants can have up to four consecutive columns written at a time with up to four DQs per column (see Figure 9).

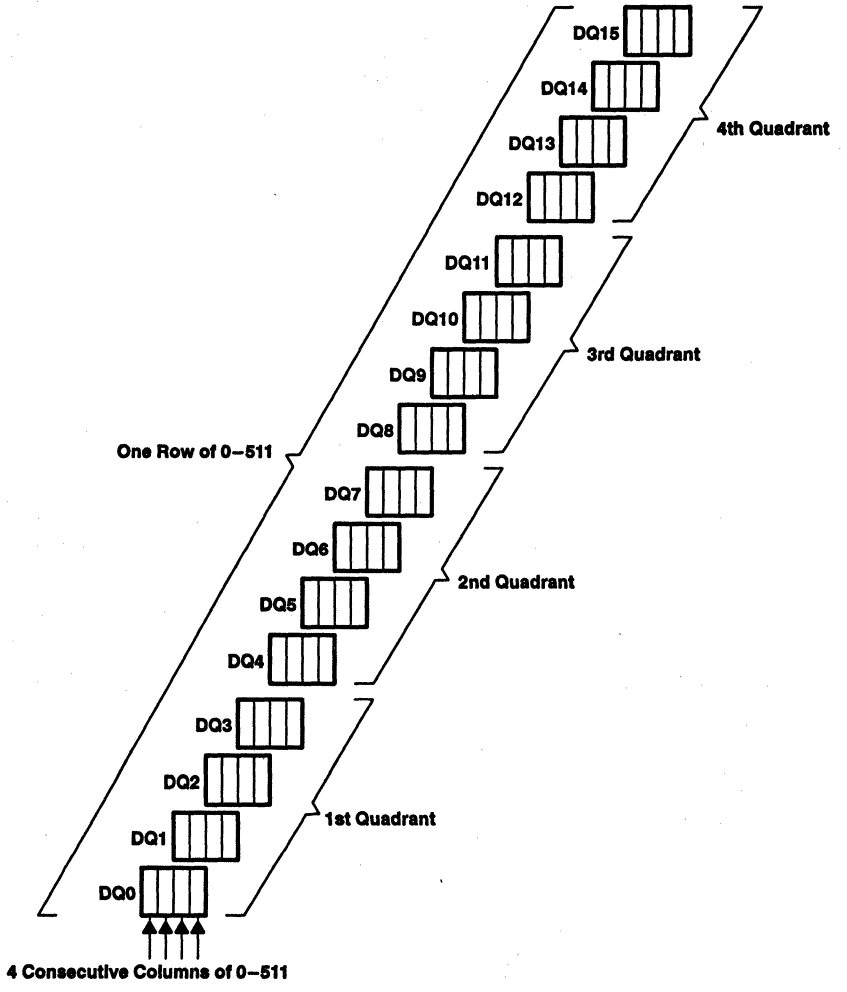


Figure 9. Block-Write Operation

Each one-megabit quadrant has a 4-bit column mask to mask off any or all of the four columns from being written with data. Nonpersistent write-per-bit or persistent write-per-bit functions can be applied to the block-write operation to provide write masking options. The DQ data is provided by four bits from the on-chip color register. Bits 0–3 from the 16-bit write-mask register, bits 0–3 from the 16-bit column-mask register, and bits 0–3 from the 16-bit color-data register configure the block write for the first quadrant, while bits 4–7, 8–11, and 12–15 of the corresponding registers control the other quadrants in a similar fashion (see Figure 10).

block write (continued)

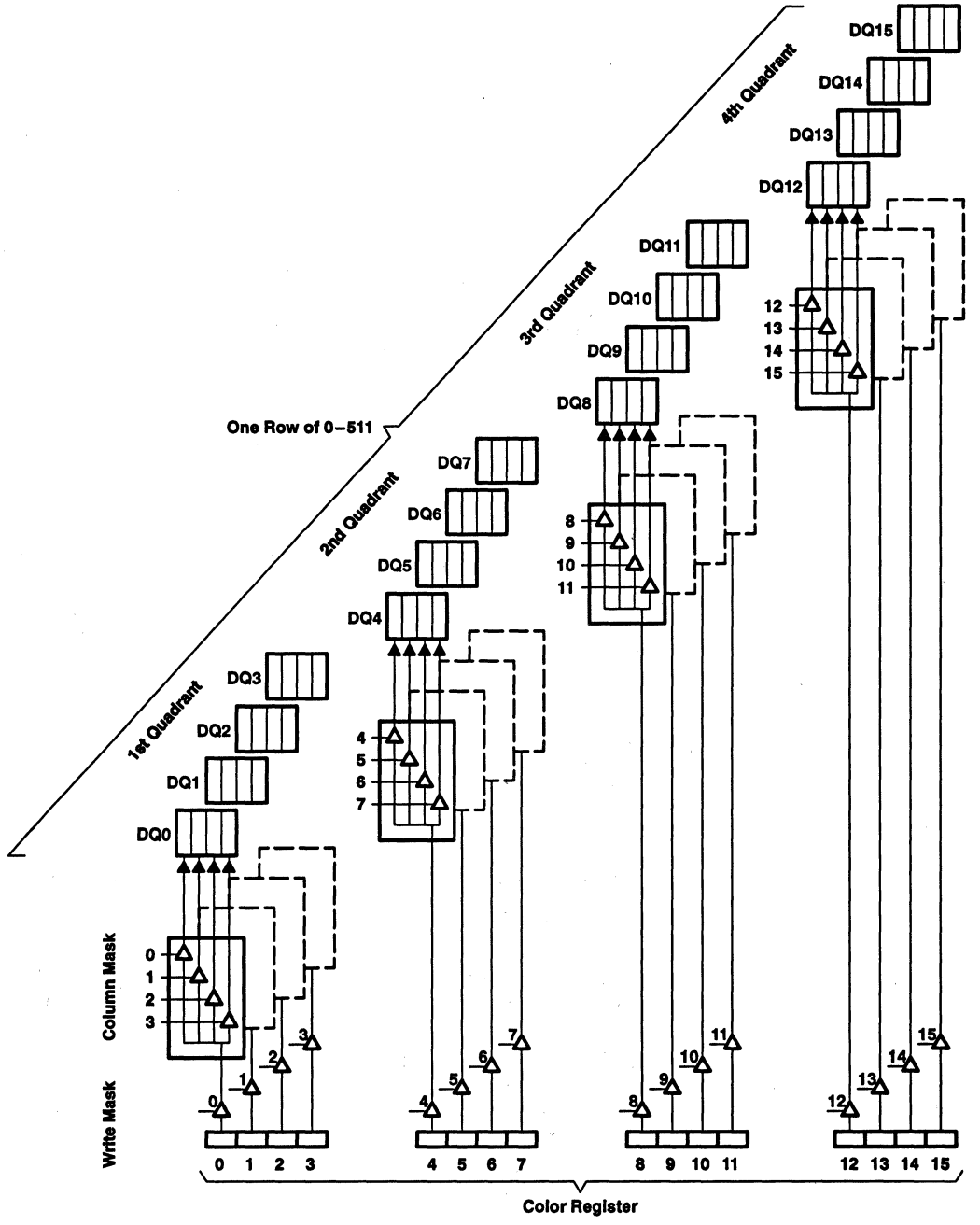


Figure 10. Block Write With Masks

block write (continued)

Every four columns make a block, which makes 128 blocks along one row. Block 0 comprises columns 0–3, block 1 comprises columns 4–7, block 2 comprises columns 8–11, etc., as shown in Figure 11.

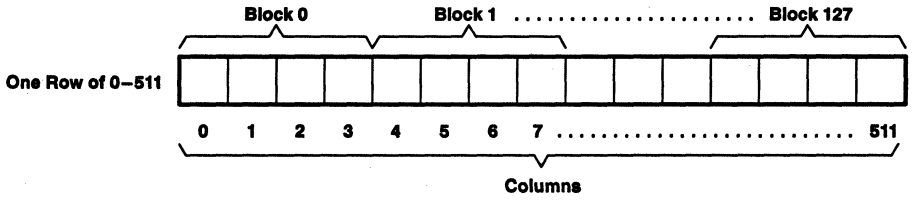


Figure 11. Block Columns Organization

During block-write cycles, only the seven most significant column addresses (A2–A8) are latched on the first falling edge of $\overline{CASx}$ to decode one of the 128 blocks. Address bits A0–A1 are ignored. Each one-megabit quadrant has the same block selected.

A block-write cycle is entered in a manner similar to a DRAM write cycle except DSF is held high on the first falling edge of $\overline{CASx}$. As in a DRAM write operation, $\overline{CASL}$ and $\overline{CASU}$ enable the corresponding lower and upper DRAM DQ bytes to be written, respectively. The column-mask data is input via the DQs and is latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. The 16-bit color-data register must be loaded prior to performing a block write as described below. Refer to the write-per-bit section for details on use of the write-mask capability allowing additional performance options.

Example of block write:

block-write column address = 110000000 (A0–A8 from left to right)

	bit 0			bit 15
color-data register =	1011	1011	1100	0111
write-mask register =	1110	1111	1111	1011
column-mask register =	1111	0000	0111	1010
	1st Quad	2nd Quad	3rd Quad	4th Quad

Column-address bits A0 and A1 are ignored. Block 0 (columns 0–3) is selected for each one-megabit quadrant. The first quadrant has DQ0–DQ2 written with bits 0–2 from the color-data register (101) to all four columns of block 0. DQ3 is not written and retains its previous data due to the write-mask-register bit 3 being a 0.

The second quadrant (DQ4–DQ7) has all four columns masked off due to the column mask bits 4–7 being 0, so that no data is written.

The third quadrant (DQ8–DQ11) has its four DQs written with bits 8–11 from the color-data register (1100) to columns 1–3 of its block 0. Column 0 is not written and retains its previous data on all four DQs due to the column mask-register bit 8 being 0.

The fourth quadrant (DQ12–DQ15) has DQ12, DQ14, and DQ15 written with bits 12, 14, and 15 from the color-data register to column 0 and column 2 of its block 0. DQ13 retains its previous data on all columns due to the write mask. Columns 1 and 3 retain their previous data on all DQs due to the column mask. If the previous data for the quadrant was all 0s, the fourth quadrant would contain the data pattern shown in Figure 12 after the block-write operation shown in the previous example.

block write (continued)

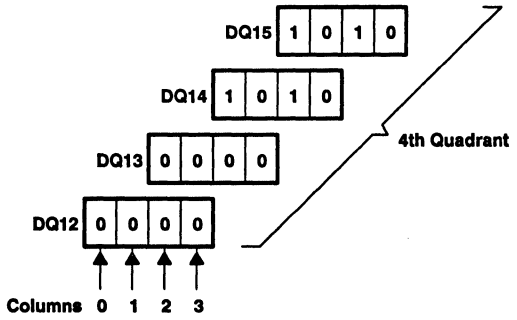
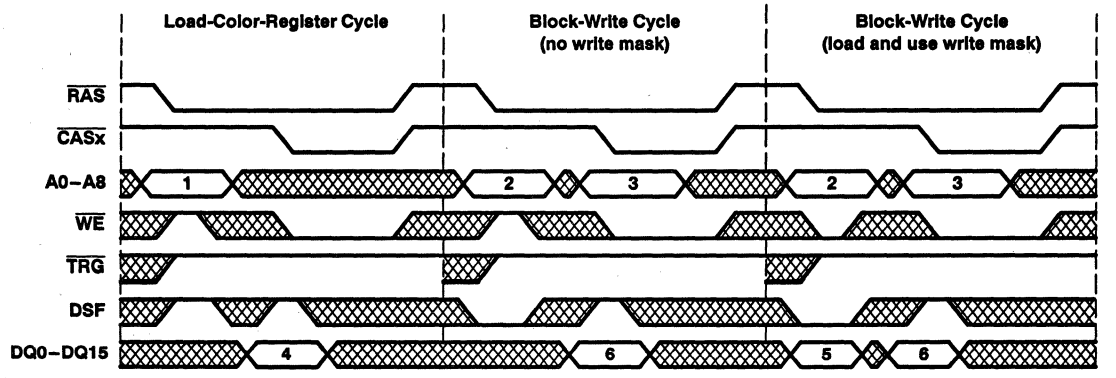


Figure 12. Example of Fourth Quadrant After a Block-Write Operation

load color register

The load-color-register cycle is performed using normal DRAM write-cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$, $\overline{CASL}$, and $\overline{CASU}$. The color register is loaded from pins DQ0–DQ15, which are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. If only one $\overline{CASx}$ is low, only the corresponding byte of the color register is loaded. When the color register is loaded, it retains data until power is lost or until another load-color-register cycle is performed (see Figure 13 and Figure 14).



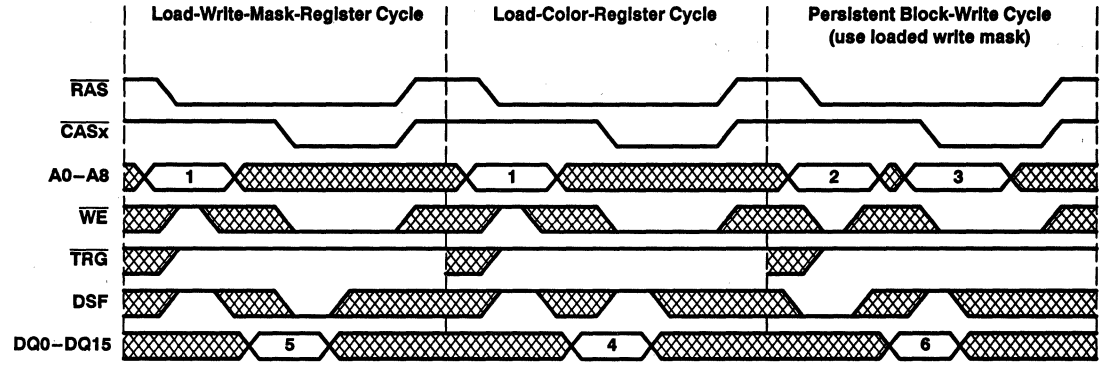
Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the first falling edge of $\overline{CASx}$.
4. Color-register data
5. Write-mask data: DQ0–DQ15 are latched on the falling edge of $\overline{RAS}$.
6. Column-mask data: DQi–DQi+3 (i = 0, 4, 8, 12) are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.

= don't care

Figure 13. Example of Block Writes

load color register (continued)



Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the first falling edge of $\overline{CAS}$x.
4. Color-register data
5. Write-mask data: DQ0 –DQ15 are latched on the falling edge of $\overline{CAS}$x.
6. Column-mask data: DQi–DQi+3 (i = 0, 4, 8, 12) are latched on either the first falling edge of $\overline{CAS}$x or the falling edge of $\overline{WE}$, whichever occurs later.

= don't care

Figure 14. Example of a Persistent Block Write

DRAM-to-SAM transfer operation

During the DRAM-to-SAM transfer operation, one half of a row (256 columns) in the DRAM array is selected to be transferred to the 256-bit serial-data register. The transfer operation is invoked by bringing $\overline{TRG}$ low and holding $\overline{WE}$ high on the falling edge of $\overline{RAS}$. The state of DSF, which is latched on the falling edge of $\overline{RAS}$, determines whether the full-register-transfer read operation or the split-register-transfer read operation is performed.

Table 4. SAM Function Table

FUNCTION	$\overline{RAS}$ FALL				$\overline{CASx}$ FALL	ADDRESS		DQ0–DQ15		MNE CODE
	$\overline{CASx}$†	$\overline{TRG}$	$\overline{WE}$	DSF	DSF	$\overline{RAS}$	$\overline{CASx}$	$\overline{RAS}$	$\overline{CASx}$ $\overline{WE}$	
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT

† Logic L is selected when either or both $\overline{CASL}$ and $\overline{CASU}$ are low.
X = don't care

full-register-transfer read

A full-register-transfer read operation loads data from a selected half of a row in the DRAM into the SAM. $\overline{TRG}$ is brought low and latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. The nine column-address bits (A0–A8) are latched at the first falling edge of $\overline{CASx}$, where address bit A8 selects which half of the row is transferred. Address bits A0–A7 select one of the SAM's 256 available tap points from which the serial data is read out (see Figure 15).

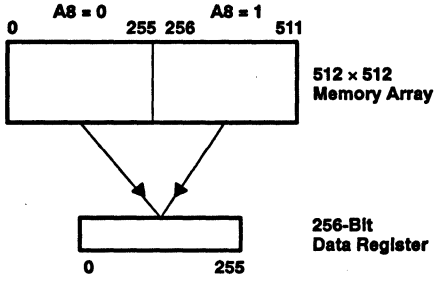


Figure 15. Full-Register-Transfer Read

A full-register-transfer read can be performed in three ways: early load, real-time load (or midline load), or late load. Each of these offers the flexibility of controlling the $\overline{TRG}$ trailing edge in the full-register-transfer read cycle (see Figure 16).

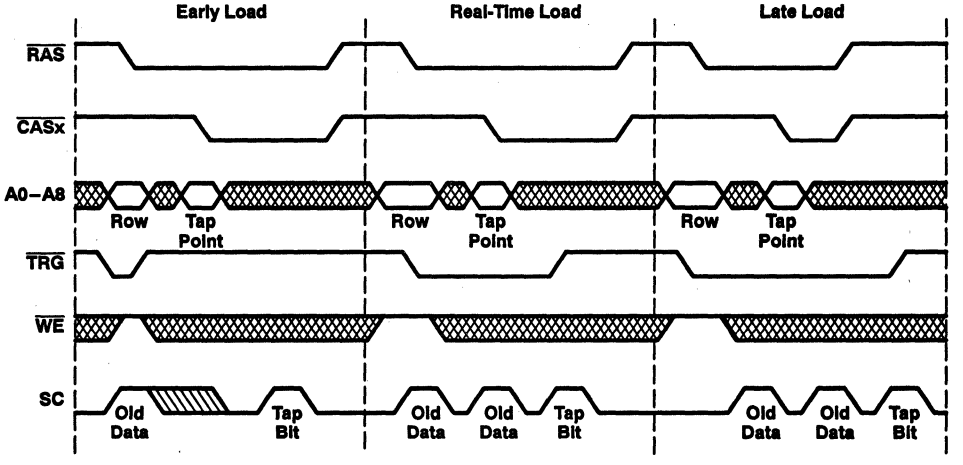


Figure 16. Example of Full-Register-Transfer Read Operations

split-register-transfer read

In the split-register-transfer read operation, the serial-data register is split into halves. The low half contains bits 0–127, and the high half contains bits 128–255. While one half is being read out of the SAM port, the other half can be loaded from the memory array.

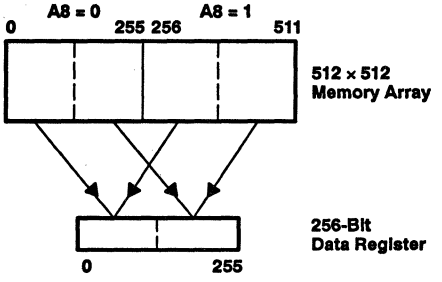
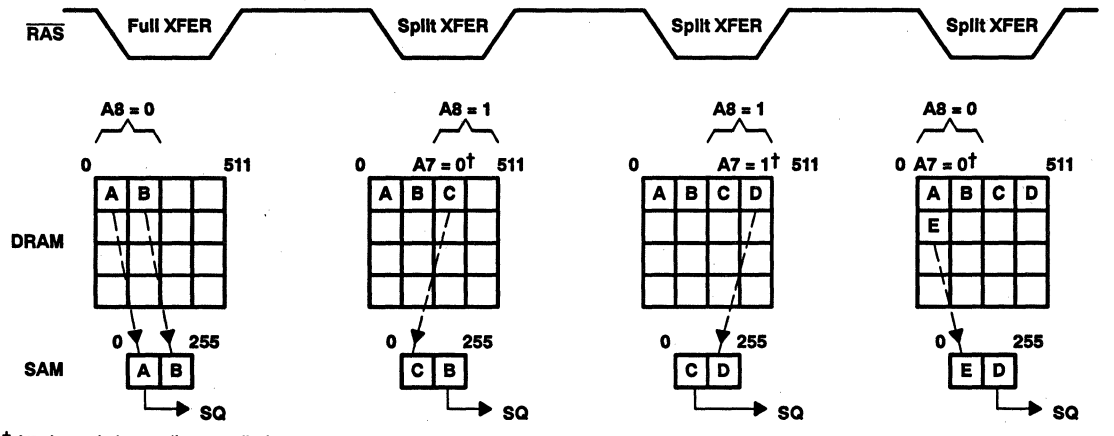


Figure 17. Split-Register-Transfer Read

To invoke a split-register-transfer read cycle, DSF is brought high, $\overline{TRG}$ is brought low, and both are latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. Eight of the nine column-address bits (A0–A6 and A8) are latched at the first falling edge of $\overline{CASx}$. Column-address bit A8 selects which half of the row is to be transferred. Column-address bits A0–A6 select one of the 127 tap points in the specified half of the SAM. Column-address bit A7 is ignored, and the split-register-transfer is internally controlled to select the inactive register half.



† A7 shown is internally controlled.

Figure 18. Example of a Split-Register-Transfer Read Operation

A full-register-transfer read must precede the first split-register-transfer read to ensure proper operation. After the full-register-transfer read cycle, the first split-register-transfer read can follow immediately without any minimum SC clock requirement.

split-register-transfer read (continued)

QSF indicates which half of the register is being accessed during serial-access operation. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of the SAM. When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF changes state upon completing a full-register-transfer read cycle. The tap point loaded during the current transfer cycle determines the state of QSF. QSF also changes state when a boundary between two register halves is reached.

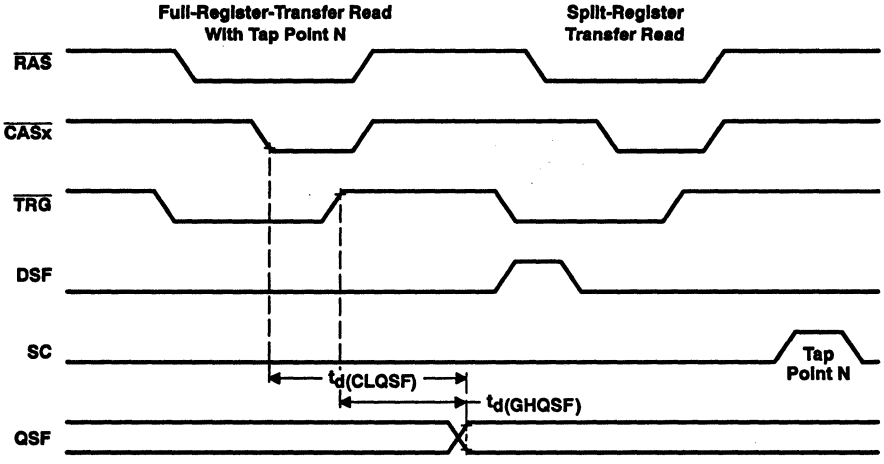


Figure 19. Example of a Split-Register-Transfer Read After a Full-Register Transfer Read

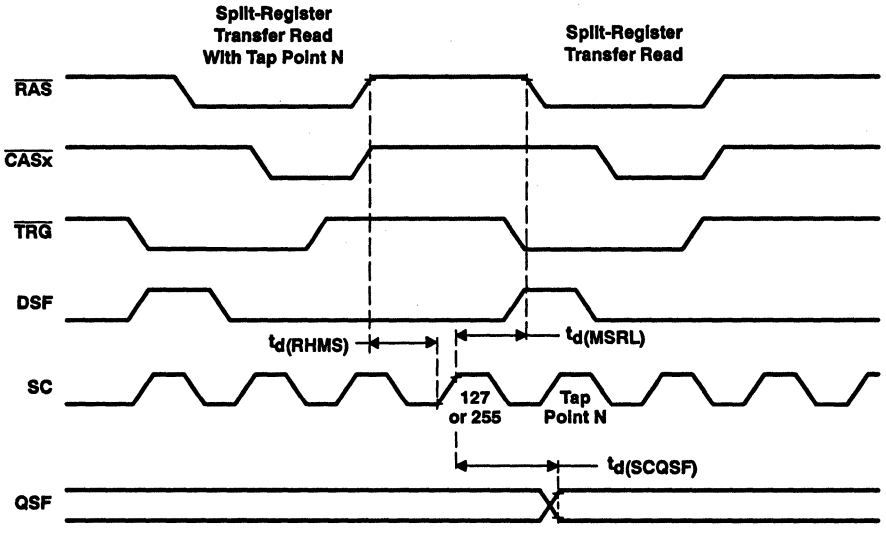


Figure 20. Example of Successive Split-Register-Transfer Read Operations

serial-read operation

The serial-read operation can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during transfer operations. Serial data can be read from the SAM by clocking SC starting at the tap point loaded by the preceding transfer cycle, proceeding sequentially to the most significant bit (bit 255), and then wrapping around to the least significant bit (bit 0), as shown in Figure 21.

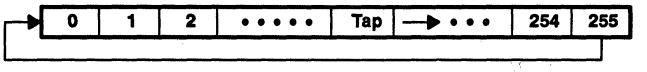


Figure 21. Serial Pointer Direction for Serial Read

For split-register-transfer read operation, serial data can be read out from the active half of the SAM by clocking SC starting at the tap point loaded by the preceding split-register-transfer cycle. The serial pointer then proceeds sequentially to the most-significant bit of the half, bit 127 or bit 255. If there is a split-register-transfer read to the inactive half during this period, the serial pointer points next to the tap point location loaded by that split-register-transfer (see Figure 22).

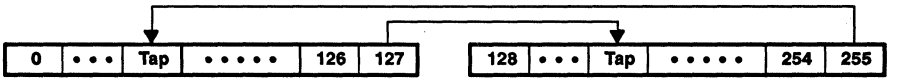


Figure 22. Serial Pointer for Split-Register Read – Case I

If there is no split-register-transfer read to the inactive half during this period, the serial pointer points next to the least significant bit of the inactive half (bit 128 or bit 0) (see Figure 23).

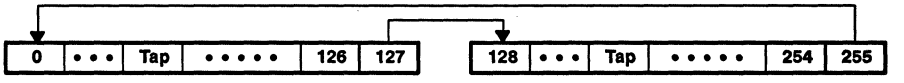


Figure 23. Serial Pointer for Split-Register Read – Case II

split-register programmable stop point

The TMS55161 offers programmable stop-point mode for split-register-transfer read operation. This mode can be used to improve 2-D drawing performance in a nonscanline data format.

In split-register-transfer read operation, the stop point is defined as a register location at which the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM. While in stop-point mode, the SAM is divided into partitions whose length is programmed via row addresses A4–A7 in a CBR set (CBRS) cycle. The last serial-address location of each partition is the stop point (see Figure 24).

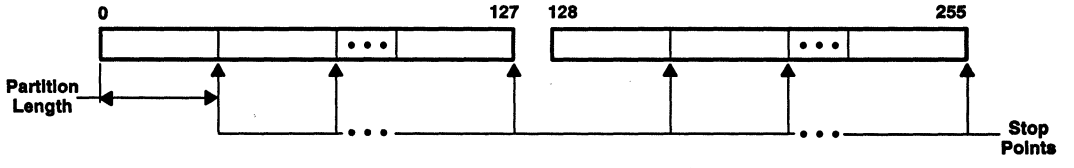


Figure 24. Example of the SAM With Partitions

split-register programmable stop point (continued)

Stop-point mode is not active until the CBRS cycle is initiated. The CBRS operation is performed by holding $\overline{CAS}$x and $\overline{WE}$ low and DSF high on the falling edge of $\overline{RAS}$. The falling edge of $\overline{RAS}$ also latches row addresses A4–A7, which are used to define the SAM's partition length. The other row-address inputs are don't care. Stop-point mode should be initiated after the initialization cycles have been performed (see Table 5).

Table 5. Programming Code for Stop-Point Mode

MAXIMUM PARTITION LENGTH	ADDRESS AT $\overline{RAS}$ IN CBRS CYCLE						NUMBER OF PARTITIONS	STOP-POINT LOCATIONS
	A8	A7	A6	A5	A4	A0–A3		
16	X	L	L	L	L	X	16	15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255
32	X	L	L	L	H	X	8	31, 63, 95, 127, 159, 191, 223, 255
64	X	L	L	H	H	X	4	63, 127, 191, 255
128 (default)	X	L	H	H	H	X	2	127, 255

In stop-point mode, the tap point loaded during the split-register-transfer read cycle determines in which SAM partition the serial output begins and at which stop point the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM (see Figure 25).

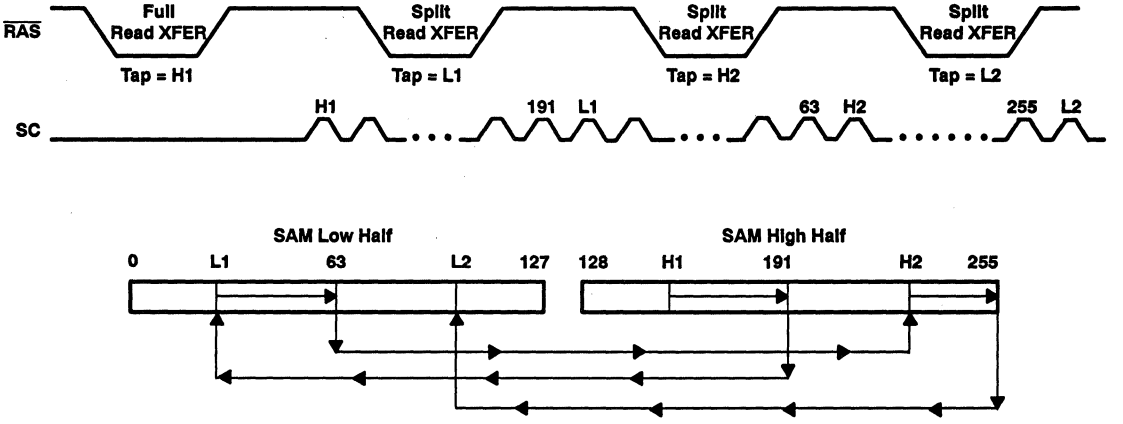


Figure 25. Example of Split-Register Operation With Programmable Stop Points

256-/512-bit compatibility of split-register programmable stop point

The stop-point mode is designed to be compatible both for 256-bit SAM and 512-bit SAM devices. After the CBRS cycle is initiated, the stop-point mode becomes active. In the stop-point mode, and only in the stop-point mode, the column-address bits AY7 and AY8 are internally swapped to assure the compatibility (see Figure 26). This address-bit swap applies to the column address, and it is effective for all DRAM and transfer cycles. For example, during the split-register-transfer cycle with stop point, column-address bit AY8 is a don't care and AY7 decodes the DRAM row half for the split-register-transfer. During stop-point mode, a CBR option reset (CBR) cycle is not recommended because it ends the stop-point mode and restores address bits AY7 and AY8 to their normal function. Consistent use of CBR cycles ensures that the TMS55161 remains in normal mode.

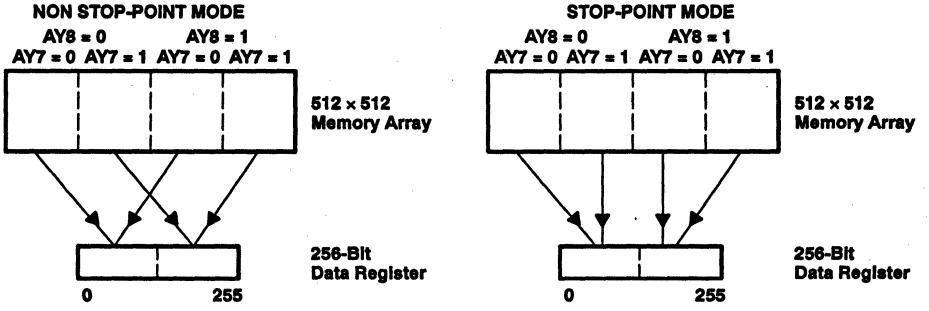


Figure 26. DRAM-to-SAM Mapping, Non Stop Point Versus Stop Point

IMPORTANT: For proper device operation in a split-register stop-point mode, a CBRS cycle should be initiated right after the power-up initialization cycles have been performed.

power up

To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight $\overline{RAS}$ cycles or eight CBR cycles to initialize the DRAM port. A full-register-transfer read cycle and two SC cycles are needed to initialize the SAM port.

After initialization, the internal state of the TMS55161 is as follows:

	STATE AFTER INITIALIZATION
QSF	Defined by the transfer cycle during initialization
Write mode	Nonpersistent mode
Write mask register	Undefined
Color register	Undefined
Serial-register tap point	Defined by the transfer cycle during initialization
SAM port	Output mode

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −1 V to 7 V
Input voltage range ..... −1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1.1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SAM PORT	'55161-60		'55161-70		'55161-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –1 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 5.8 V, All other pins at 0 V to V_{CC}			±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC} See Note 3			±10		±10		±10	µA
I_{CC1}	Operating current‡	See Note 4	Standby		180		165		150	mA
I_{CC1A}	Operating current‡	$t_{c(SC)}$ = MIN	Active		225		205		185	mA
I_{CC2}	Standby current	All clocks = V_{CC}	Standby		5		5		5	mA
I_{CC2A}	Standby current	$t_{c(SC)}$ = MIN	Active		70		65		60	mA
I_{CC3}	$\overline{RAS}$-only refresh current	See Note 4	Standby		180		165		150	mA
I_{CC3A}	$\overline{RAS}$-only refresh current	$t_{c(SC)}$ = MIN, See Note 4	Active		225		205		185	mA
I_{CC4}	Page-mode current‡	$t_{c(P)}$ = MIN, See Note 5	Standby		140		140		120	mA
I_{CC4A}	Page-mode current‡	$t_{c(SC)}$ = MIN, See Note 5	Active		185		185		165	mA
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ current	See Note 4	Standby		180		165		150	mA
I_{CC5A}	$\overline{CAS}$-before-$\overline{RAS}$ current	$t_{c(SC)}$ = MIN, See Note 4	Active		225		205		185	mA
I_{CC6}	Data-transfer current	See Note 4	Standby		200		180		160	mA
I_{CC6A}	Data-transfer current	$t_{c(SC)}$ = MIN	Active		250		225		200	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
NOTES: 3. $\overline{SE}$ is disabled for SQ output leakage tests.
4. Measured with one address change while $\overline{RAS}$ = V_{IL}. $t_{c(rd)}$, $t_{c(W)}$, $t_{c(TRD)}$ = MIN.
5. Measured with one address change while $\overline{CASx}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, address strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(DSF)}$	Input capacitance, special function		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
$C_{o(O)}$	Output capacitance, SQ and DQ		7	pF
$C_{o(QSF)}$	Output capacitance, QSF		9	pF

NOTE 6: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		TEST CONDITIONS†	ALT. SYMBOL	'55161-60		'55161-70		'55161-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CASx}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		17		20		20	ns
$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{AA}		30		35		40	ns
$t_{a(CP)}$	Access time from $\overline{CASx}$ high	$t_{d(RLCL)}$ = MAX	t_{CPA}		35		40		45	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MAX	t_{RAC}		60		70		80	ns
$t_{a(G)}$	Access time of DQ from $\overline{TRG}$ low		t_{OEA}		15		20		20	ns
$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 30 pF	t_{SCA}		15		20		25	ns
$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		12		15		20	ns
$t_{dis(CH)}$	Disable time, random output from $\overline{CASx}$ high (see Note 8)	C_L = 50 pF	t_{OFF}	0	15	0	20	0	20	ns
$t_{dis(RH)}$	Disable time, random output from $\overline{RAS}$ high (see Note 8)	C_L = 50 pF		0	15	0	20	0	20	ns
$t_{dis(G)}$	Disable time, random output from $\overline{TRG}$ high (see Note 8)	C_L = 50 pF	t_{OEZ}	0	15	0	20	0	20	ns
$t_{dis(WL)}$	Disable time, random output from $\overline{WE}$ low (see Note 8)	C_L = 30 pF	t_{WEZ}	0	15	0	20	0	20	ns
$t_{dis(SE)}$	Disable time, serial output from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	0	10	0	15	0	20	ns

† Measured with outputs open. For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

NOTES: 7. Switching times for RAM port output are measured with a load equivalent to 1 TTL load and 50 pF. Data out reference level: V_{OH}/V_{OL} = 2 V/0.8 V. Switching times for SAM port output are measured with a load equivalent to 1 TTL load and 30 pF. Serial data out reference level: V_{OH}/V_{OL} = 2 V/0.8 V.

8. $t_{dis(CH)}$, $t_{dis(RH)}$, $t_{dis(G)}$, $t_{dis(WL)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature†

		ALT. SYMBOL	'55161-60		'55161-70		'55161-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Cycle time, read	t_{RC}	110		130		150		ns
$t_{c(W)}$	Cycle time, write	t_{WC}	110		130		150		ns
$t_{c(rdW)}$	Cycle time, read-modify-write	t_{RMW}	150		175		200		ns
$t_{c(P)}$	Cycle time, page-mode read, write	t_{PC}	30		30		35		ns
$t_{c(RDWP)}$	Cycle time, page-mode read-modify-write	t_{PRMW}	80		90		100		ns
$t_{c(TRD)}$	Cycle time, transfer read	t_{RC}	110		130		150		ns
$t_{c(SC)}$	Cycle time, serial clock (see Note 9)	t_{SCC}	18		22		30		ns
$t_{w(CH)}$	Pulse duration, $\overline{CASx}$ high	t_{CPN}	10		10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CASx}$ low (see Note 10)	t_{CAS}	10	10 000	10	10 000	20	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	40		50		60		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 11)	t_{RAS}	60	10 000	70	10 000	80	10 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{WE}$ low	t_{WP}	10		10		15		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		15		20		20		ns
$t_{w(SCH)}$	Pulse duration, SC high (see Note 9)	t_{SC}	5		8		10		ns
$t_{w(SCL)}$	Pulse duration, SC low (see Note 9)	t_{SCP}	5		8		10		ns
$t_{w(GH)}$	Pulse duration, $\overline{TRG}$ high	t_{TP}	20		20		20		ns
$t_{w(RL)P}$	Pulse duration, $\overline{RAS}$ low (page mode)	t_{RASP}	60	100 000	70	100 000	80	100 000	ns
$t_{su(CA)}$	Setup time, column address before $\overline{CASx}$ low	t_{ASC}	0		0		0		ns
$t_{su(SFC)}$	Setup time, DSF before $\overline{CASx}$ low	t_{FSC}	0		0		0		ns
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(WMR)}$	Setup time, $\overline{WE}$ before $\overline{RAS}$ low	t_{WSR}	0		0		0		ns
$t_{su(DQR)}$	Setup time, DQ before $\overline{RAS}$ low	t_{MS}	0		0		0		ns
$t_{su(TRG)}$	Setup time, $\overline{TRG}$ high before $\overline{RAS}$ low	t_{THS}	0		0		0		ns
$t_{su(SFR)}$	Setup time, DSF low before $\overline{RAS}$ low	t_{FSR}	0		0		0		ns
$t_{su(DCL)}$	Setup time, data valid before $\overline{CASx}$ low	t_{DSC}	0		0		0		ns
$t_{su(DWL)}$	Setup time, data valid before $\overline{WE}$ low	t_{DSW}	0		0		0		ns
$t_{su(rd)}$	Setup time, read command, $\overline{WE}$ high before $\overline{CASx}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	Setup time, early write command, $\overline{WE}$ low before $\overline{CASx}$ low	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	Setup time, $\overline{WE}$ low before $\overline{CASx}$ high, write	t_{CWL}	15		15		20		ns
$t_{su(WRH)}$	Setup time, $\overline{WE}$ low before $\overline{RAS}$ high, write	t_{RWL}	15		15		20		ns
$t_{h(CLCA)}$	Hold time, column address after $\overline{CASx}$ low	t_{CAH}	10		10		15		ns
$t_{h(SFC)}$	Hold time, DSF after $\overline{CASx}$ low	t_{CFH}	10		10		15		ns
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low	t_{RAH}	10		10		10		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. Cycle time assumes t_t = 3 ns.

10. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CASx}$ low time [$t_{w(CL)}$].

11. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

			ALT. SYMBOL	'55161-60		'55161-70		'55161-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(TRG)}$	Hold time, $\overline{TRG}$ after $\overline{RAS}$ low		t_{THH}	10		10		10		ns
$t_{h(RWM)}$	Hold time, write mask after $\overline{RAS}$ low		t_{RWH}	10		10		10		ns
$t_{h(RDQ)}$	Hold time, DQ after $\overline{RAS}$ low (write-mask operation)		t_{MH}	10		10		10		ns
$t_{h(SFR)}$	Hold time, DSF after $\overline{RAS}$ low		t_{RFH}	10		10		10		ns
$t_{h(RLCA)}$	Hold time, column address valid after $\overline{RAS}$ low (see Note 12)		t_{AR}	30		30		35		ns
$t_{h(CLD)}$	Hold time, data valid after $\overline{CASx}$ low		t_{DH}	15		15		15		ns
$t_{h(RLD)}$	Hold time, data valid after $\overline{RAS}$ low (see Note 12)		t_{DHR}	35		35		35		ns
$t_{h(WLD)}$	Hold time, data valid after $\overline{WE}$ low		t_{DH}	15		15		15		ns
$t_{h(CHrd)}$	Hold time, read, $\overline{WE}$ high after $\overline{CASx}$ high (see Note 13)		t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Hold time, read, $\overline{WE}$ high after $\overline{RAS}$ high (see Note 13)		t_{RRH}	0		0		0		ns
$t_{h(CLW)}$	Hold time, write, $\overline{WE}$ low after $\overline{CASx}$ low		t_{WCH}	10		15		15		ns
$t_{h(RLW)}$	Hold time, write, $\overline{WE}$ low after $\overline{RAS}$ low (see Note 12)		t_{WCR}	30		35		35		ns
$t_{h(WLG)}$	Hold time, $\overline{TRG}$ high after $\overline{WE}$ low (see Note 14)		t_{OEH}	10		10		10		ns
$t_{h(SHSQ)}$	Hold time, SQ valid after SC high		t_{SOH}	4		5		5		ns
$t_{h(RSF)}$	Hold time, DSF after $\overline{RAS}$ low		t_{FHR}	30		30		35		ns
$t_{h(CLQ)}$	Hold time, output valid after $\overline{CASx}$ low		t_{DHC}	4		5		5		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ high		t_{CSH}	53		60		80		ns
		See Note 15	t_{CHR}	10		10		15		
$t_{d(CHRL)}$	Delay time, $\overline{CASx}$ high to $\overline{RAS}$ low		t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ high		t_{RSH}	17		20		20		ns
$t_{d(CLWL)}$	Delay time, $\overline{CASx}$ low to $\overline{WE}$ low (see Notes 16 and 17)		t_{CWD}	37		45		45		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ low (see Note 18)		t_{RCD}	20	43	20	50	20	60	ns
$t_{d(CARH)}$	Delay time, column address valid to $\overline{RAS}$ high		t_{RAL}	30		35		40		ns
$t_{d(CACH)}$	Delay time, column address valid to $\overline{CASx}$ high		t_{CAL}	30		35		40		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{WE}$ low (see Note 16)		t_{RWD}	80		95		105		ns
$t_{d(CAWL)}$	Delay time, column address valid to $\overline{WE}$ low (see Note 16)		t_{AWD}	50		60		65		ns
$t_{d(CLRL)}$	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ low (see Note 15)		t_{CSR}	0		0		0		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CASx}$ low (see Note 15)		t_{RPC}	0		0		0		ns
$t_{d(CLGH)}$	Delay time, $\overline{CASx}$ low to $\overline{TRG}$ high for DRAM read cycles			17		20		20		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ		t_{OED}	10		15		15		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
14. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
15. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only
16. Read-modify-write operation only
17. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
18. The maximum value is specified only to assure $\overline{RAS}$ access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)†

		ALT. SYMBOL	'55161-60		'55161-70		'55161-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (see Note 19)	t_{RTH}	50		55		60		ns
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 19)	t_{RSD}	65		70		80		ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address valid	t_{RAD}	15	30	15	35	15	40	ns
$t_{d(GLRH)}$	Delay time, $\overline{TRG}$ low to $\overline{RAS}$ high	t_{ROH}	10		15		15		ns
$t_{d(CLSH)}$	Delay time, $\overline{CASx}$ low to first SC high after $\overline{TRG}$ high (see Note 20)	t_{CSD}	20		20		25		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 19 and 20)	t_{TSL}	5		5		5		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 19)	t_{TRD}	−10		−10		−10		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 21)	t_{TRP}	40		50		60		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 19)	t_{TSD}	10		10		15		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split-register-transfer read cycles		15		20		20		ns
$t_{d(CLTH)}$	Delay time, $\overline{CASx}$ low to $\overline{TRG}$ high in real-time transfer read cycles	t_{CTH}	15		15		15		ns
$t_{d(CASH)}$	Delay time, column address to first SC in early-load transfer read cycles	t_{ASD}	25		25		30		ns
$t_{d(CAGH)}$	Delay time, column address to $\overline{TRG}$ high in real-time transfer read cycles	t_{ATH}	20		20		20		ns
$t_{d(DCL)}$	Delay time, data to $\overline{CASx}$ low	t_{DZC}	0		0		0		ns
$t_{d(DGL)}$	Delay time, data to $\overline{TRG}$ low	t_{DZO}	0		0		0		ns
$t_{d(MSRL)}$	Delay time, last (most significant) rising edge of SC to $\overline{RAS}$ low before boundary switch during split-register-transfer read cycles		15		20		20		ns
$t_{d(SCQSF)}$	Delay time, last (127 or 255) rising edge of SC to QSF switching at the boundary during split-register-transfer read cycles (see Note 22)	t_{SQD}		20		25		30	ns
$t_{d(CLQSF)}$	Delay time, $\overline{CASx}$ low to QSF switching in transfer read cycles (see Note 22)	t_{CQD}		25		30		35	ns
$t_{d(GHQSF)}$	Delay time, $\overline{TRG}$ high to QSF switching in transfer read cycles (see Note 22)	t_{TQD}		20		25		30	ns
$t_{d(RLQSF)}$	Delay time, $\overline{RAS}$ low to QSF switching in transfer read cycles (see Note 22)	t_{RQD}		65		70		75	ns
$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 19. Real-time load transfer read or late-load transfer read cycle only
20. Early-load transfer read cycle only
21. Full-register (read) transfer cycles only
22. Switching times for QSF output are measured with a load equivalent to 1 TTL load and 30 pF and output reference level is V_{OH} / V_{OL} = 2 V/0.8 V.

PARAMETER MEASUREMENT INFORMATION

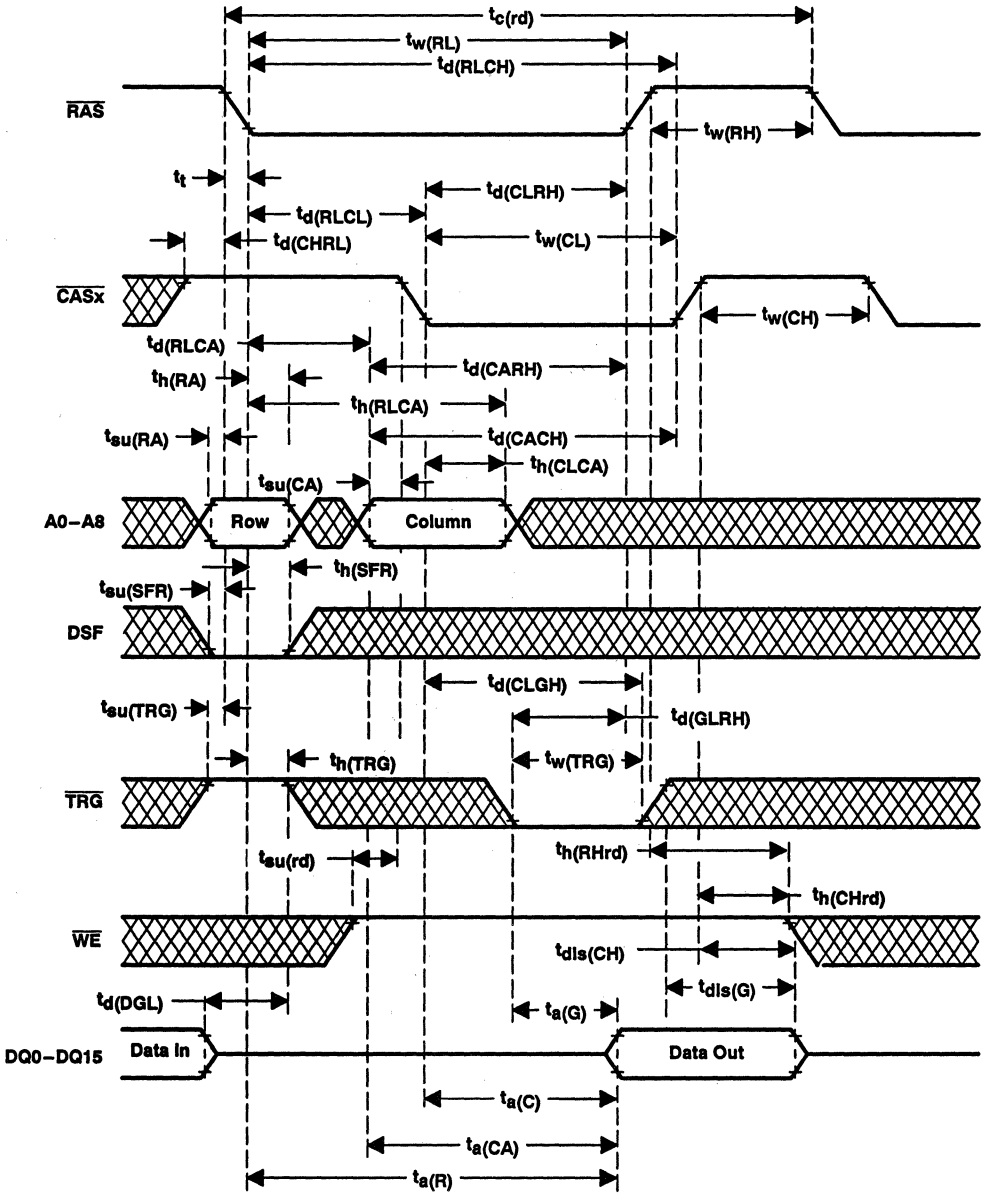


Figure 27. Read-Cycle Timing With $\overline{\text{CASx}}$-Controlled Output

PARAMETER MEASUREMENT INFORMATION

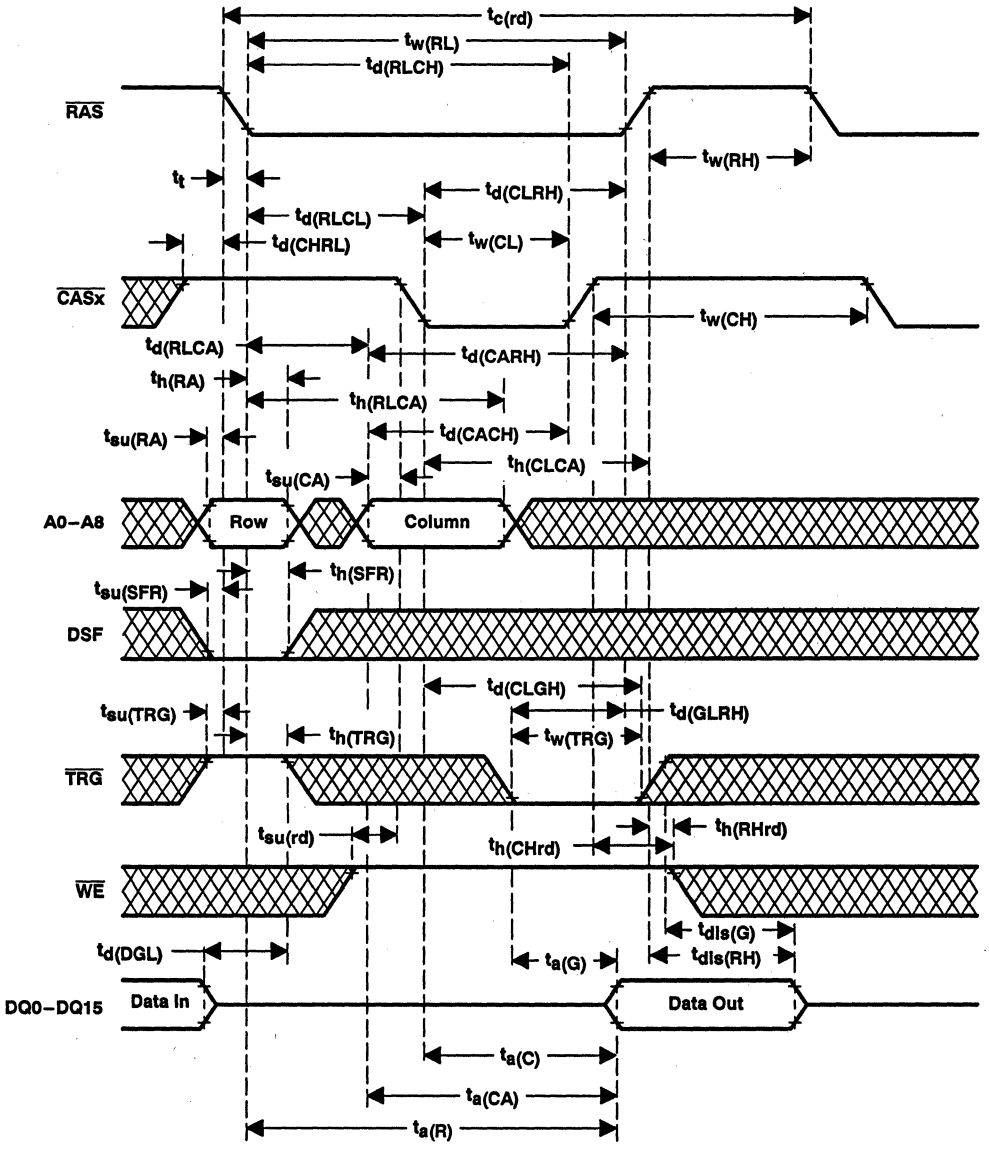


Figure 28. Read-Cycle Timing With $\overline{RAS}$-Controlled Output

PARAMETER MEASUREMENT INFORMATION

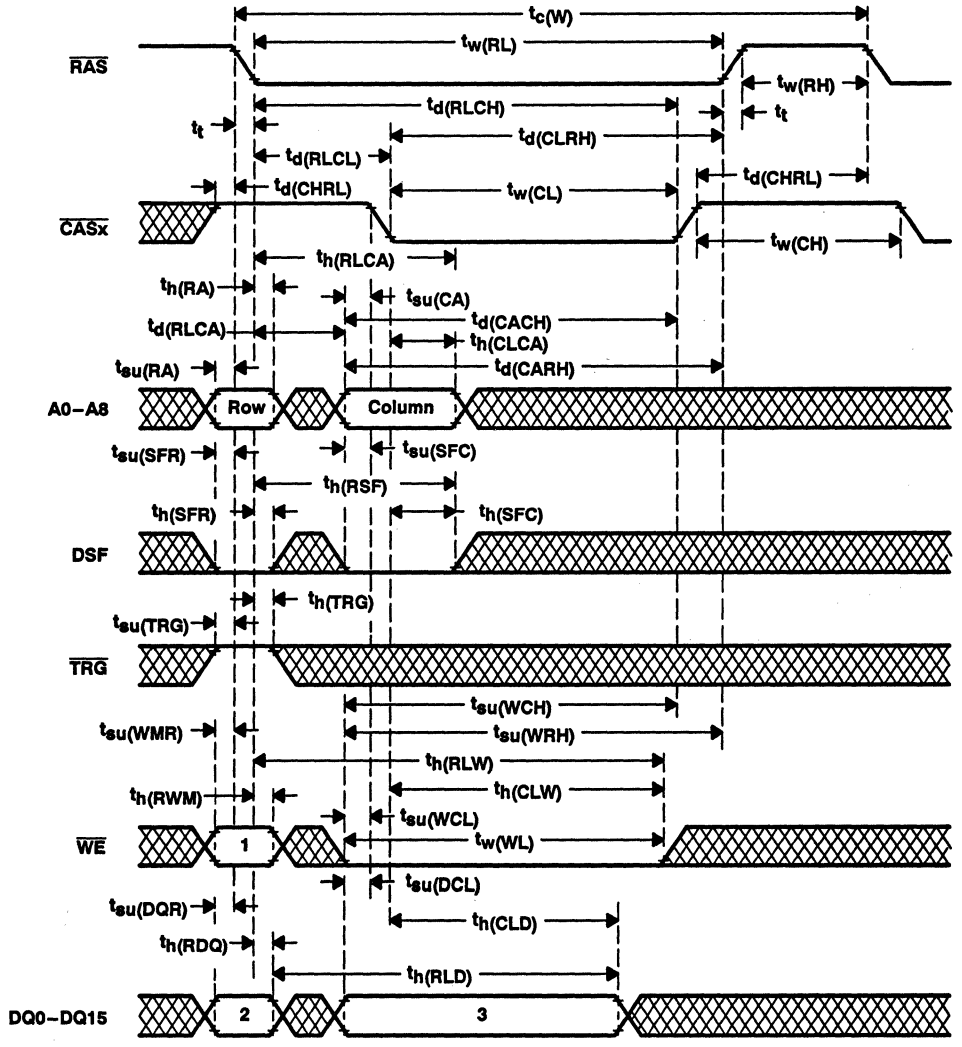


Figure 29. Early-Write-Cycle Timing

Table 6. Early-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

PARAMETER MEASUREMENT INFORMATION

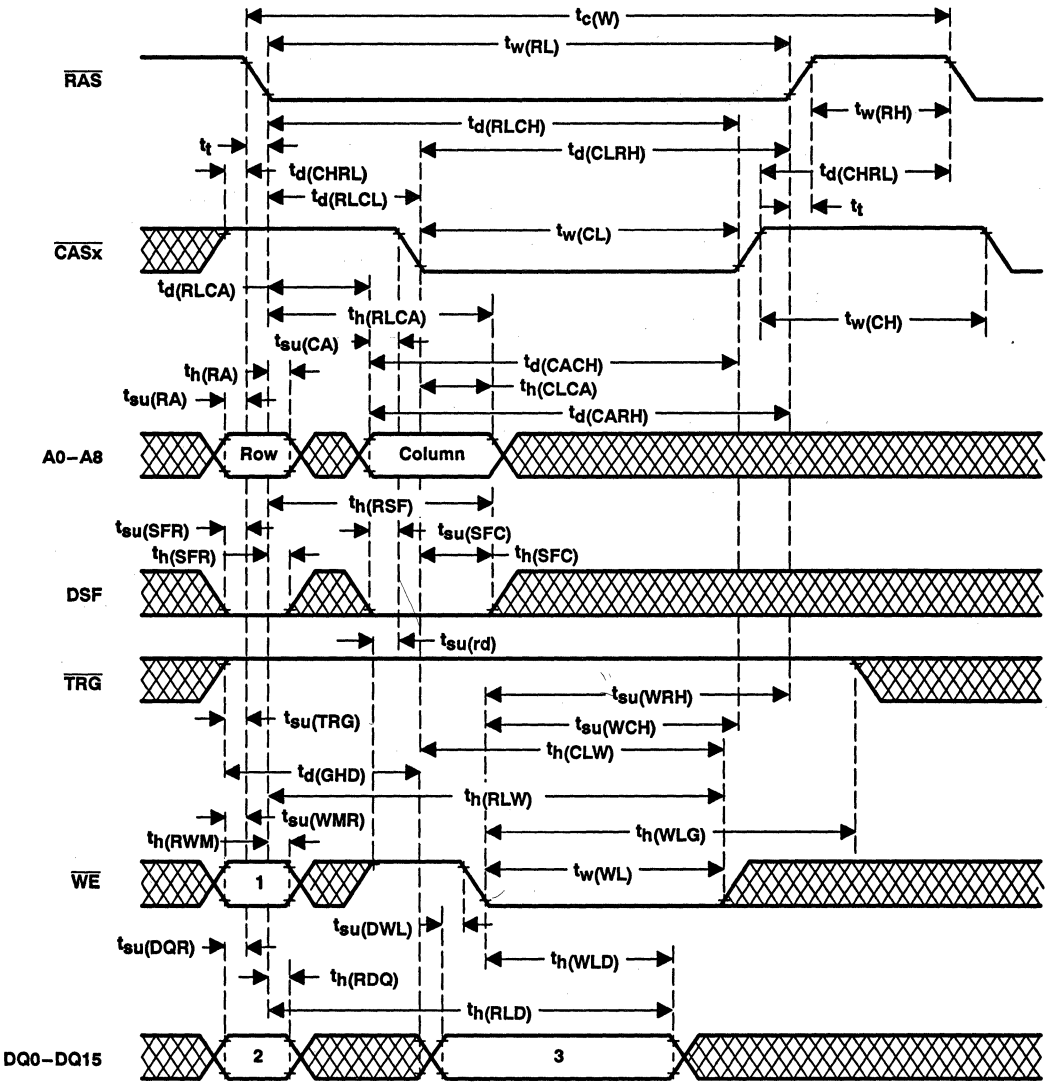
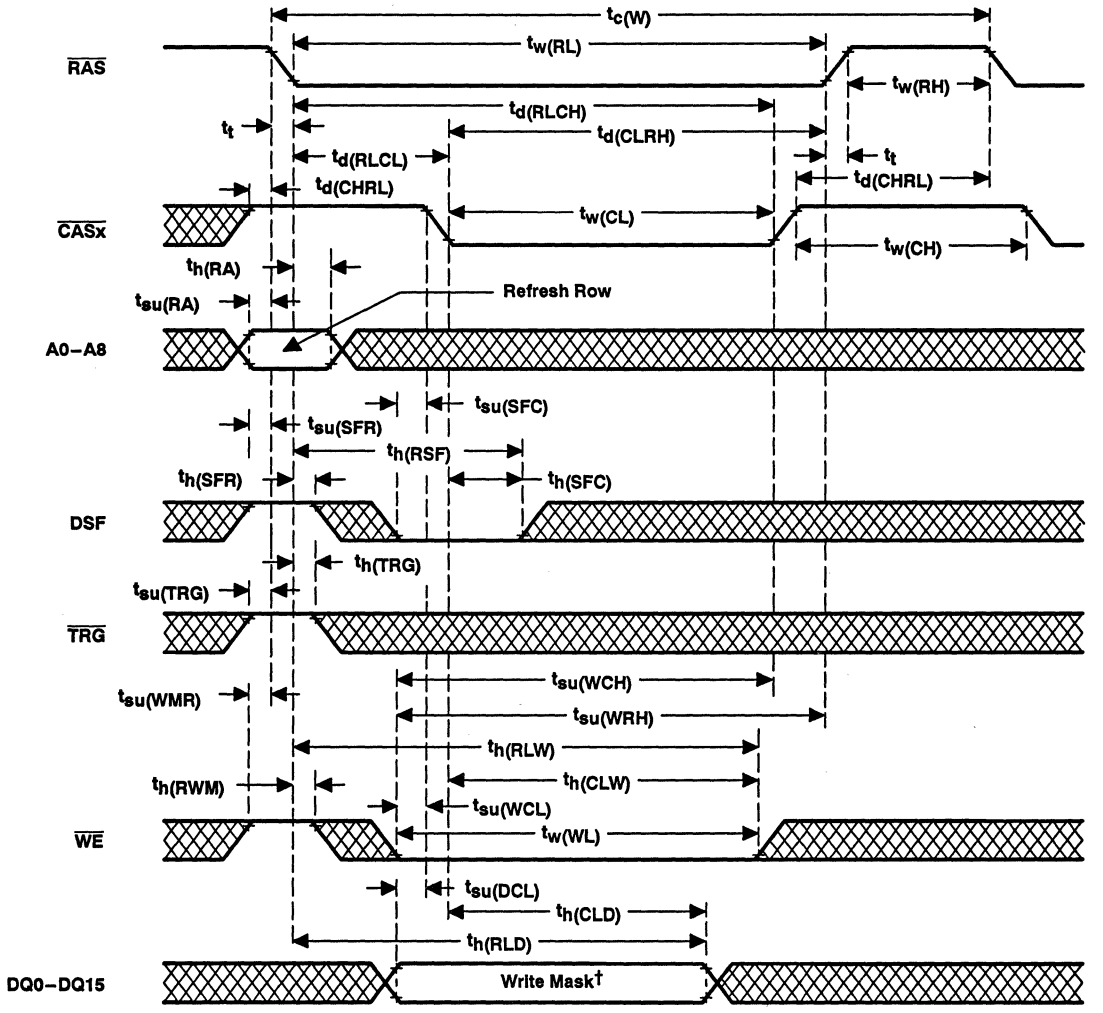


Figure 30. Late-Write-Cycle Timing (Output-Enable-Controlled Write)

Table 7. Late-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

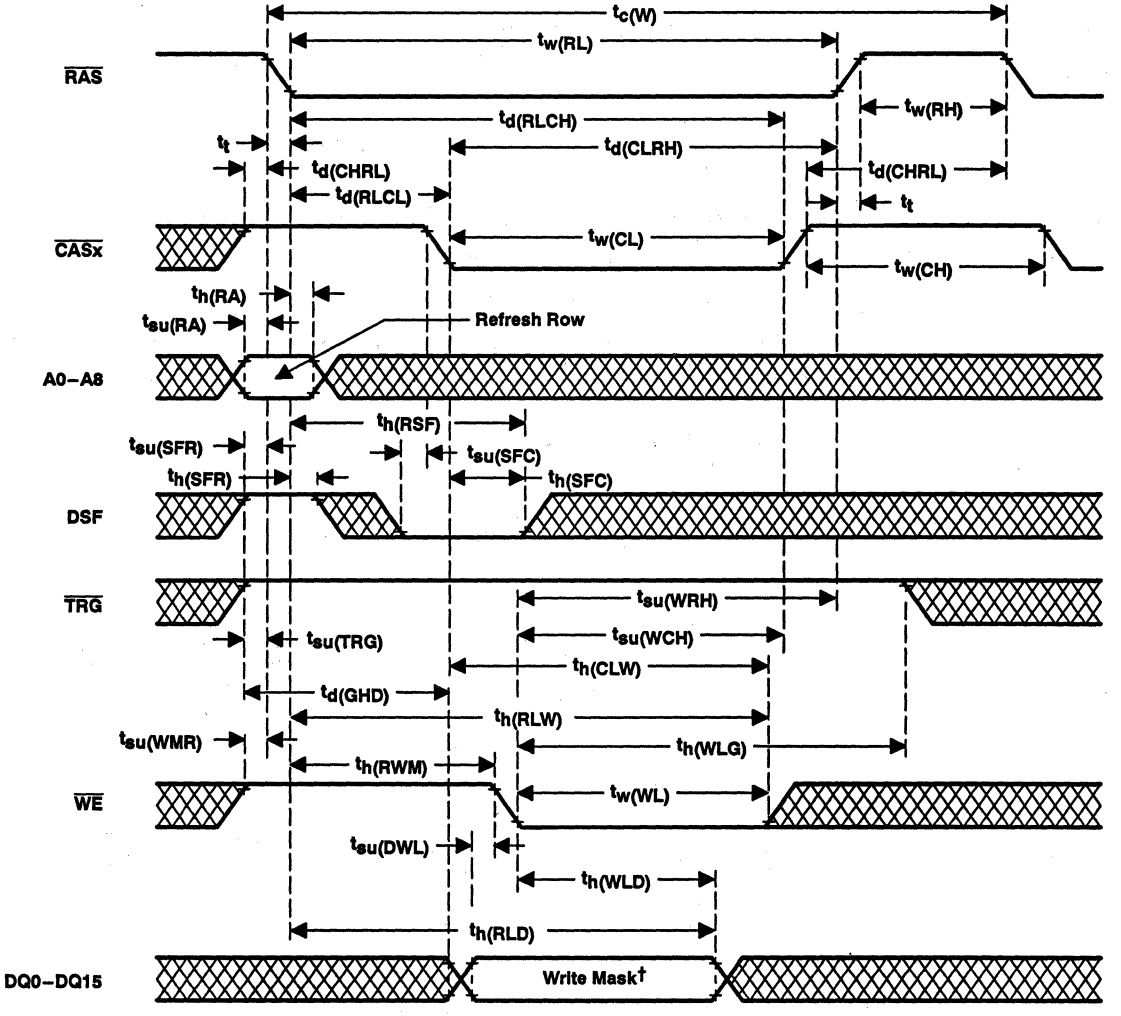
PARAMETER MEASUREMENT INFORMATION



† Load-write-mask-register cycle will put the device into the persistent write-per-bit mode.

Figure 31. Load-Write-Mask-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION



† Load-write-mask-register cycle will put the device into the persistent write-per-bit mode.

Figure 32. Load-Write-Mask-Register-Cycle Timing (Late-Write Load)

PARAMETER MEASUREMENT INFORMATION

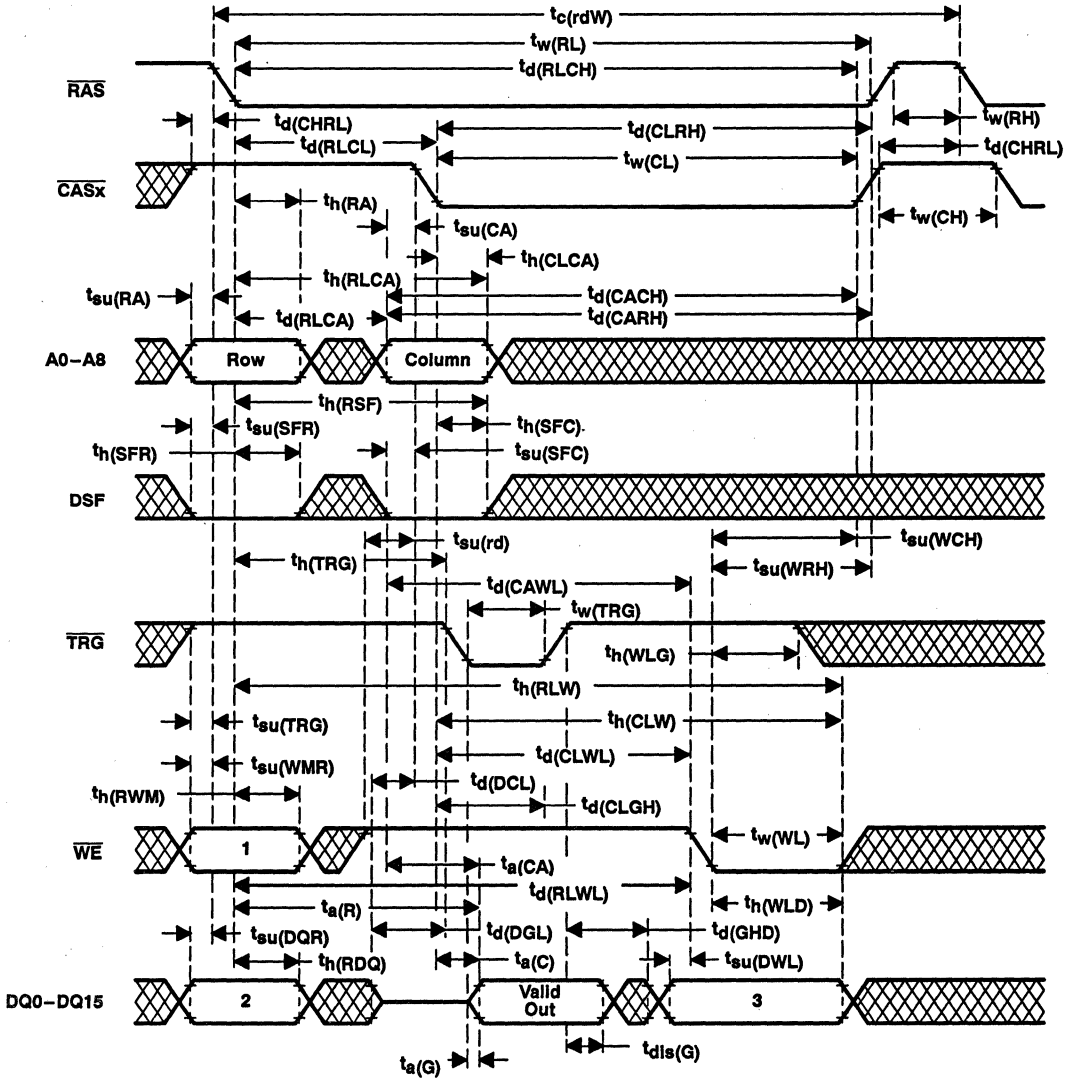
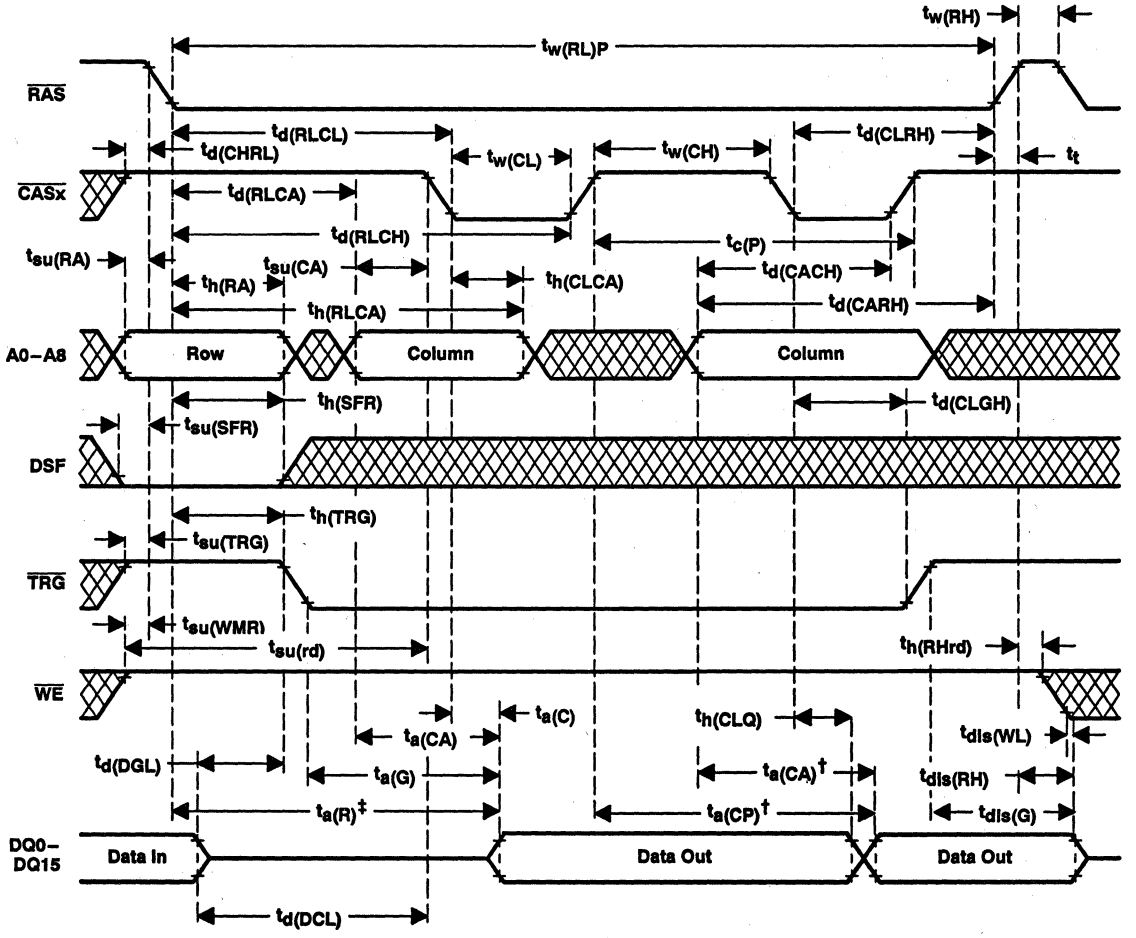


Figure 33. Read-Write/Read-Modify-Write-Cycle Timing

Table 8. Read-Write/Read-Modify-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

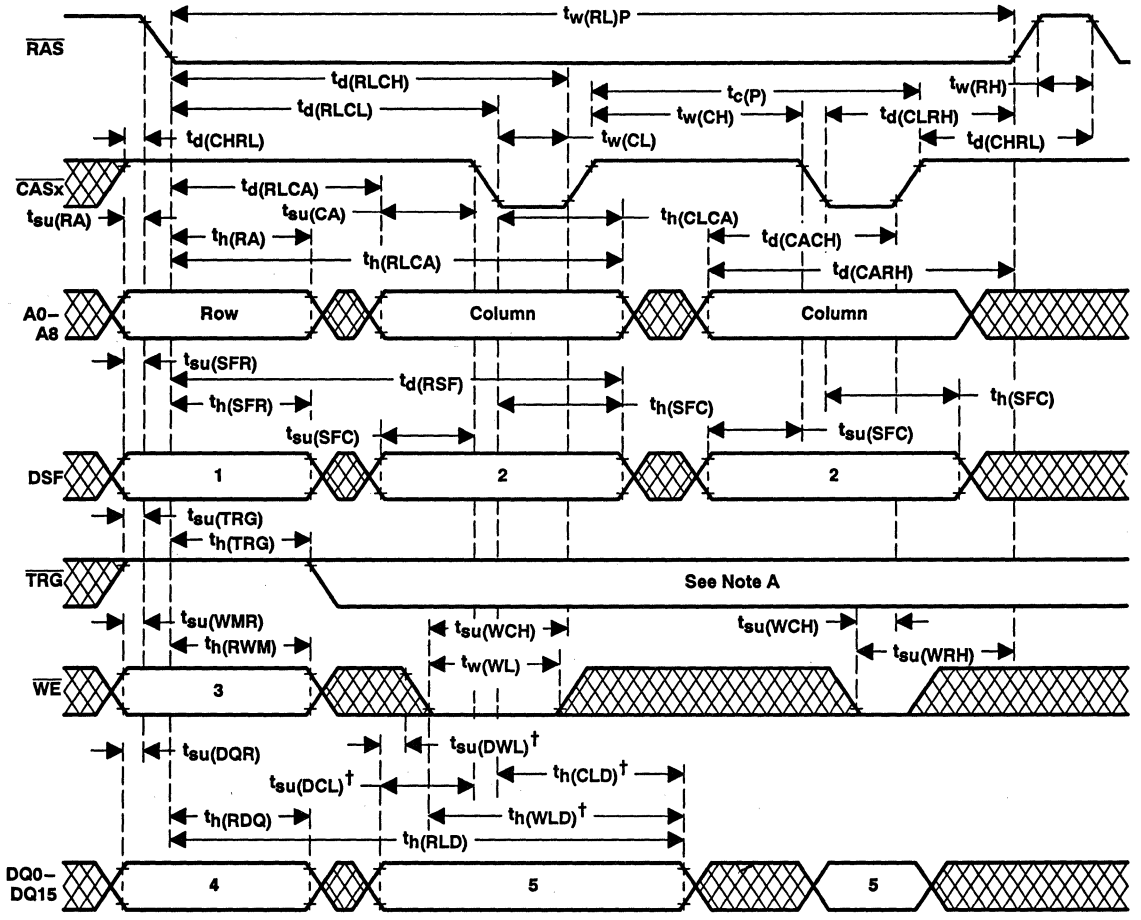
PARAMETER MEASUREMENT INFORMATION



† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CASx}$ to select the desired write mode (normal, block write, etc.).

Figure 34. Enhanced-Page-Mode Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later

NOTE A: A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used. If the early write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

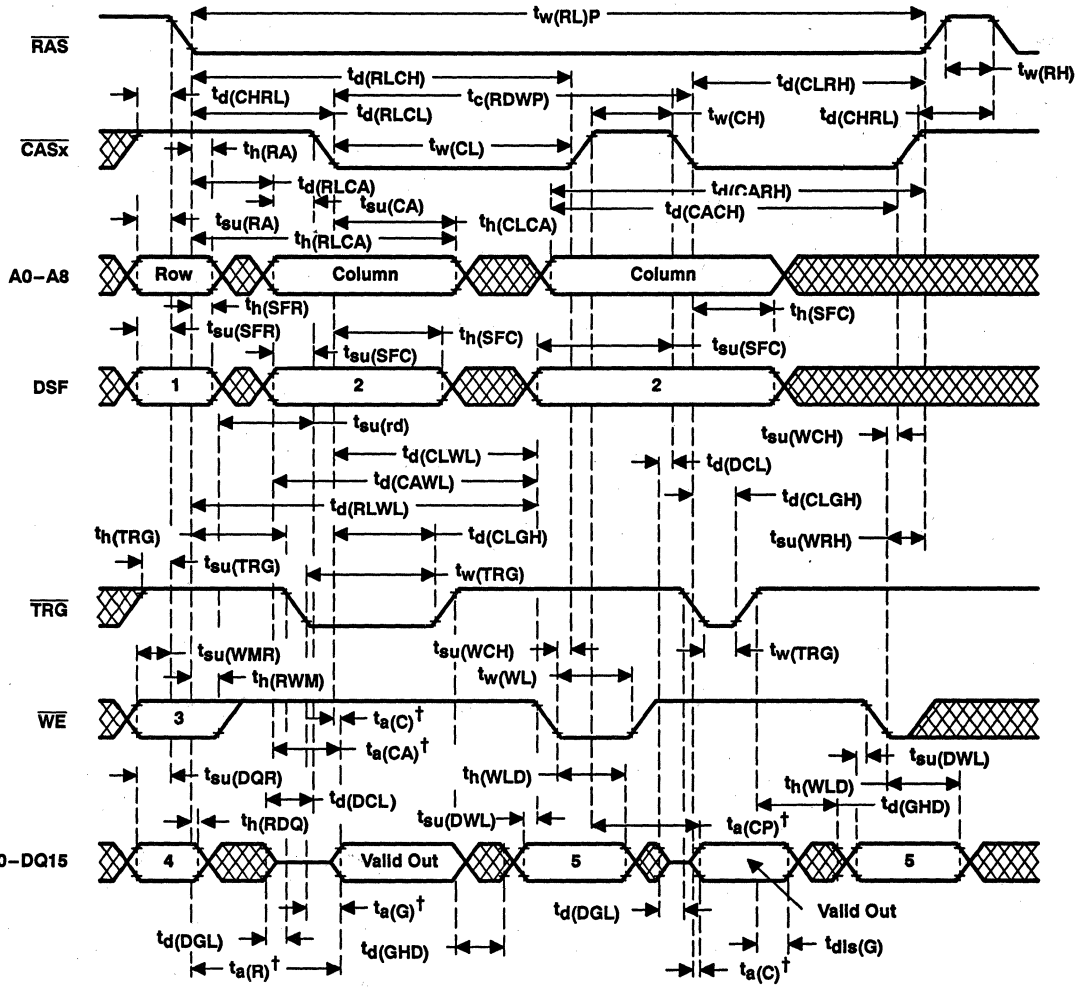
Figure 35. Enhanced-Page-Mode Write-Cycle Timing

Table 9. Enhanced-Page-Mode Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load-write mask on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurrs later.‡	H	L	H	Don't care	Write mask

‡ Load-write-mask-register cycle will set the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CASx}$ is a don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



† Output can go from the high-impedance to an invalid-data state prior to the specified access time.

NOTE A: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

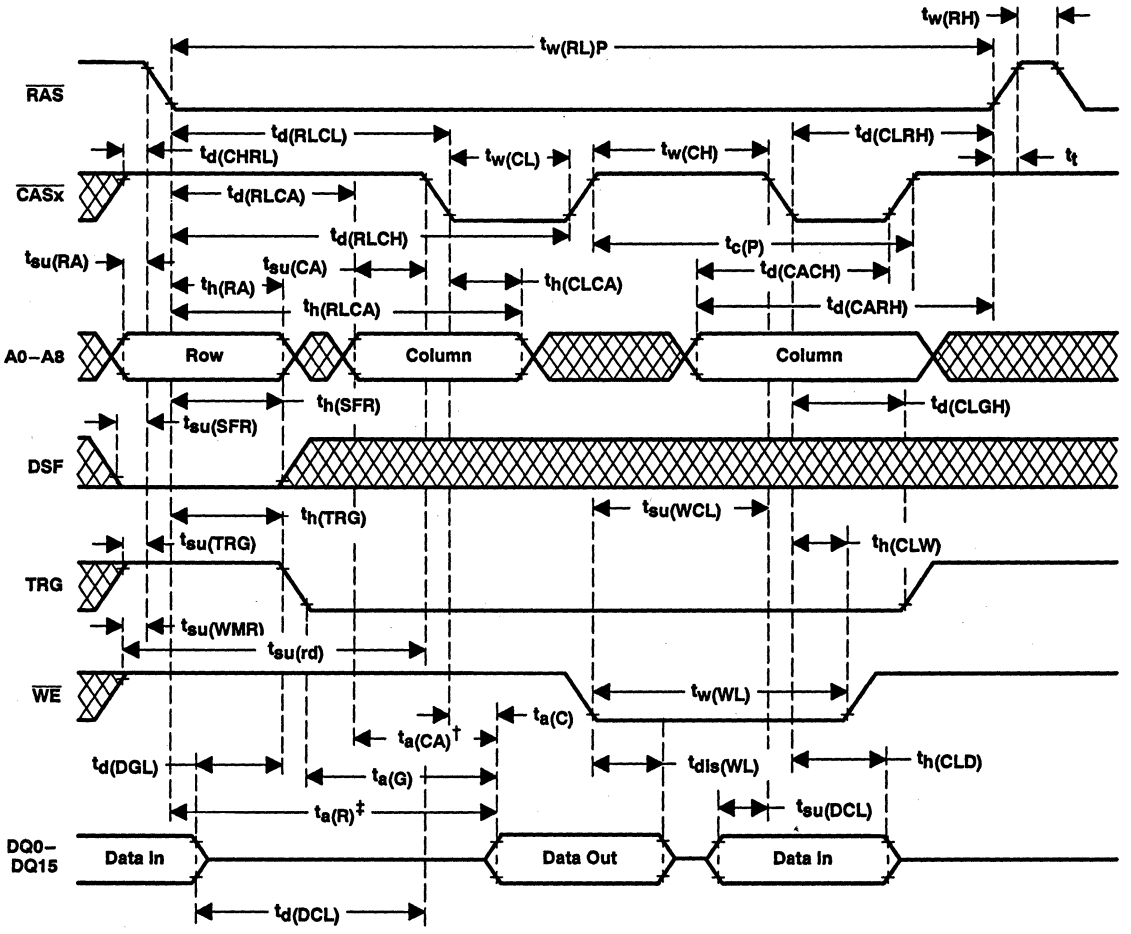
Figure 36. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

Table 10. Enhanced-Page-Mode Read-Modify-Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load write mask on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load-write-mask cycle will set the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CASx}$ is a don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



† Access time is $t_{a(CA)}$ dependent.
‡ Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 37. Enhanced-Page-Mode Read/Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

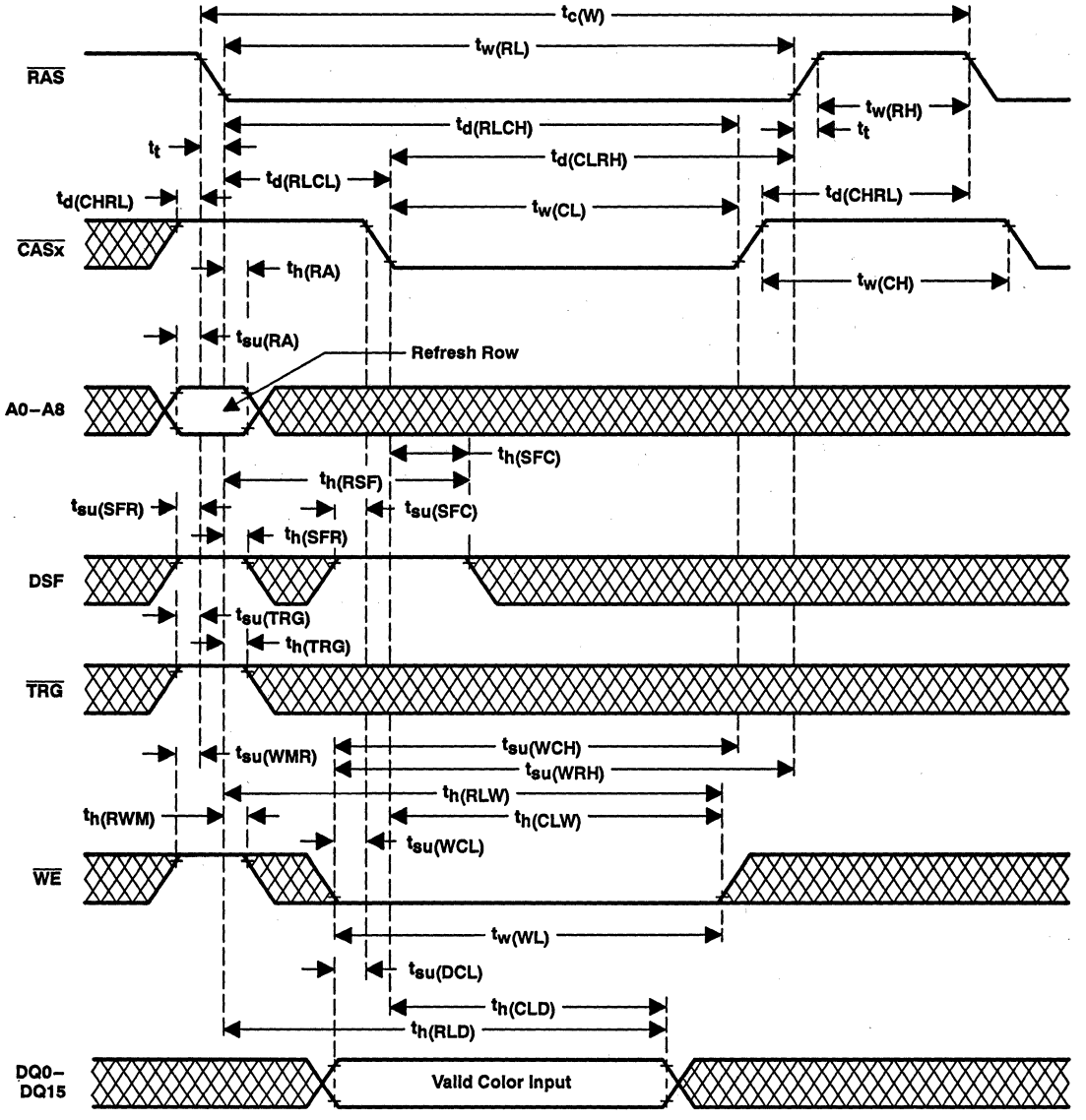


Figure 38. Load-Color-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION

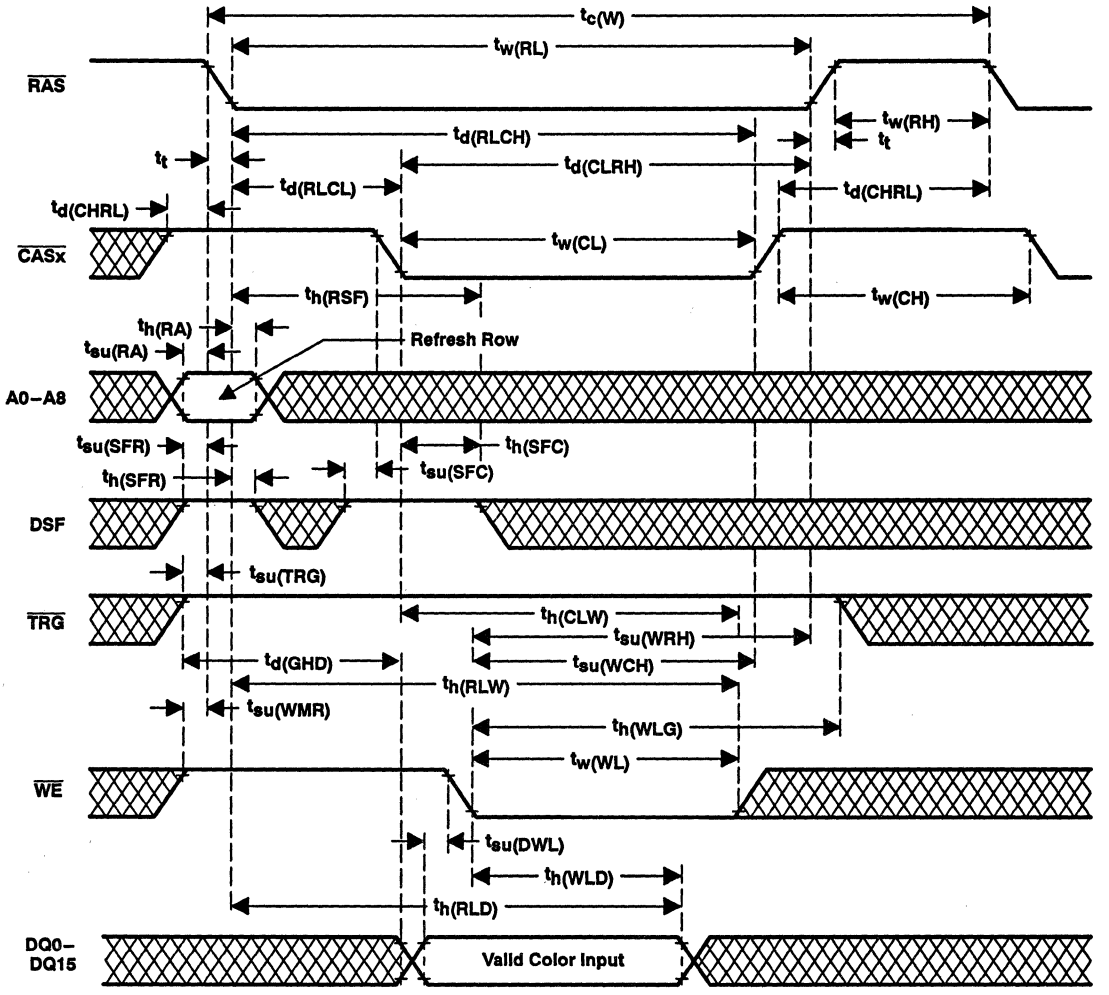


Figure 39. Load-Color-Register-Cycle Timing (Late-Write Load)

PARAMETER MEASUREMENT INFORMATION

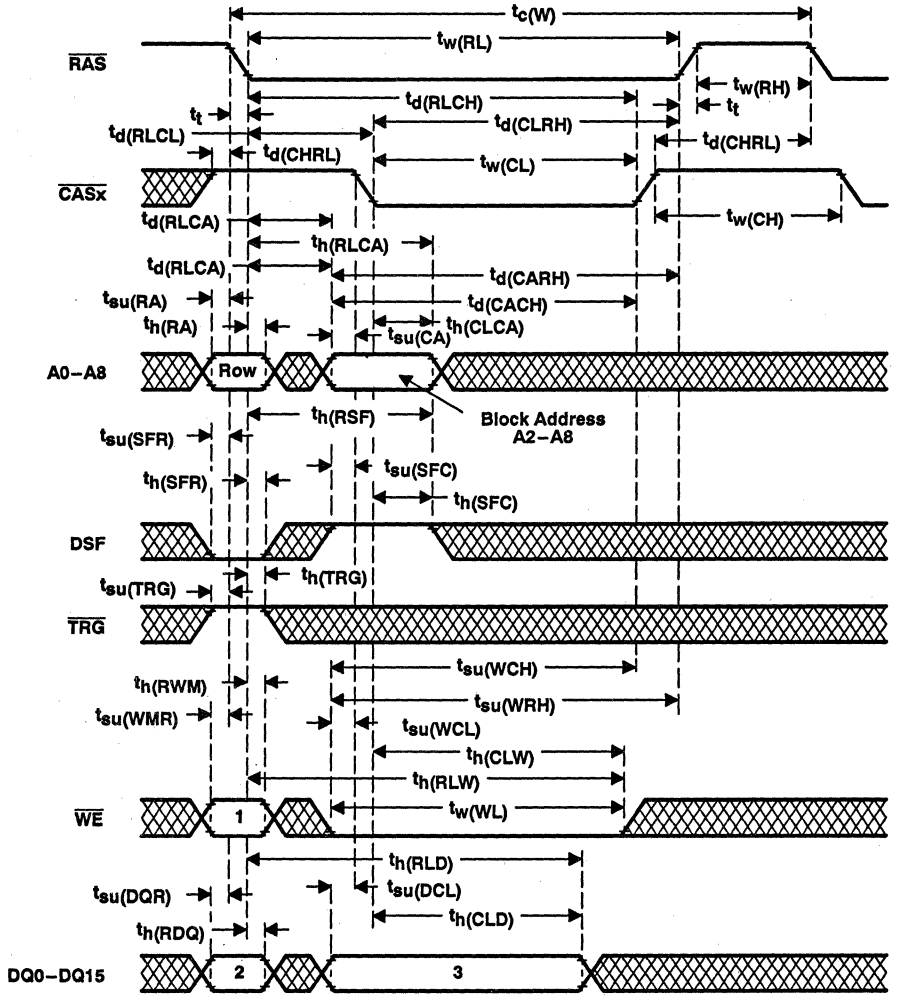


Figure 40. Block-Write-Cycle Timing (Early Write)

Table 11. Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi+3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

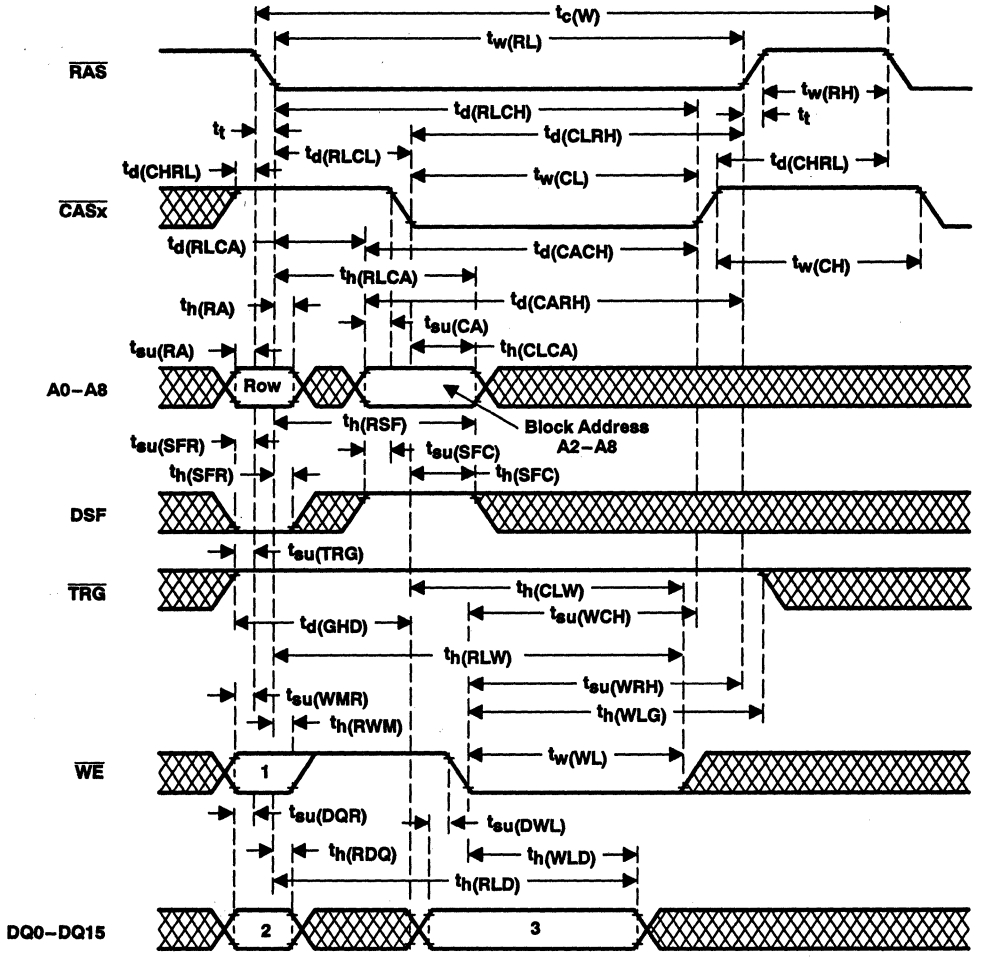


Figure 41. Block-Write-Cycle Timing (Late Write)

Table 12. Block-Write-Cycle State Table

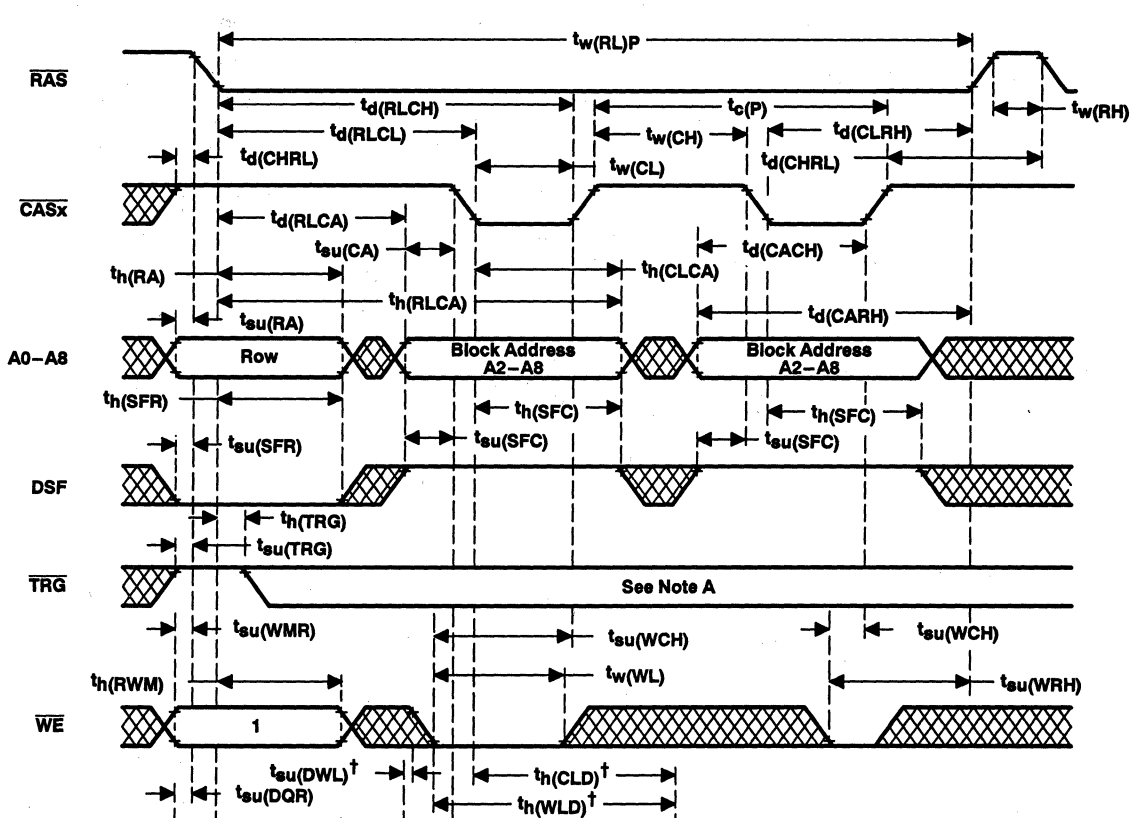
CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi+3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.

NOTE A: To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late-write feature is used. If the early-write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 42. Enhanced-Page-Mode Block-Write-Cycle Timing

Table 13. Enhanced-Page-Mode Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi+3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

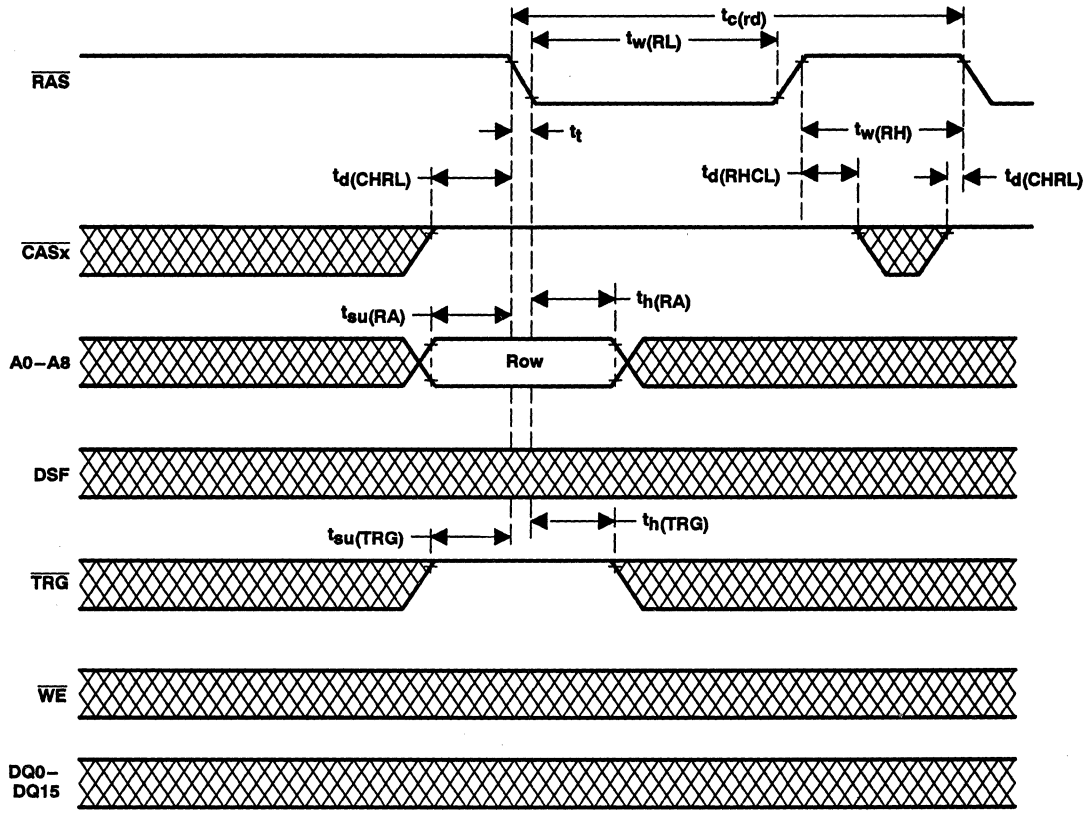


Figure 43. $\overline{RAS}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

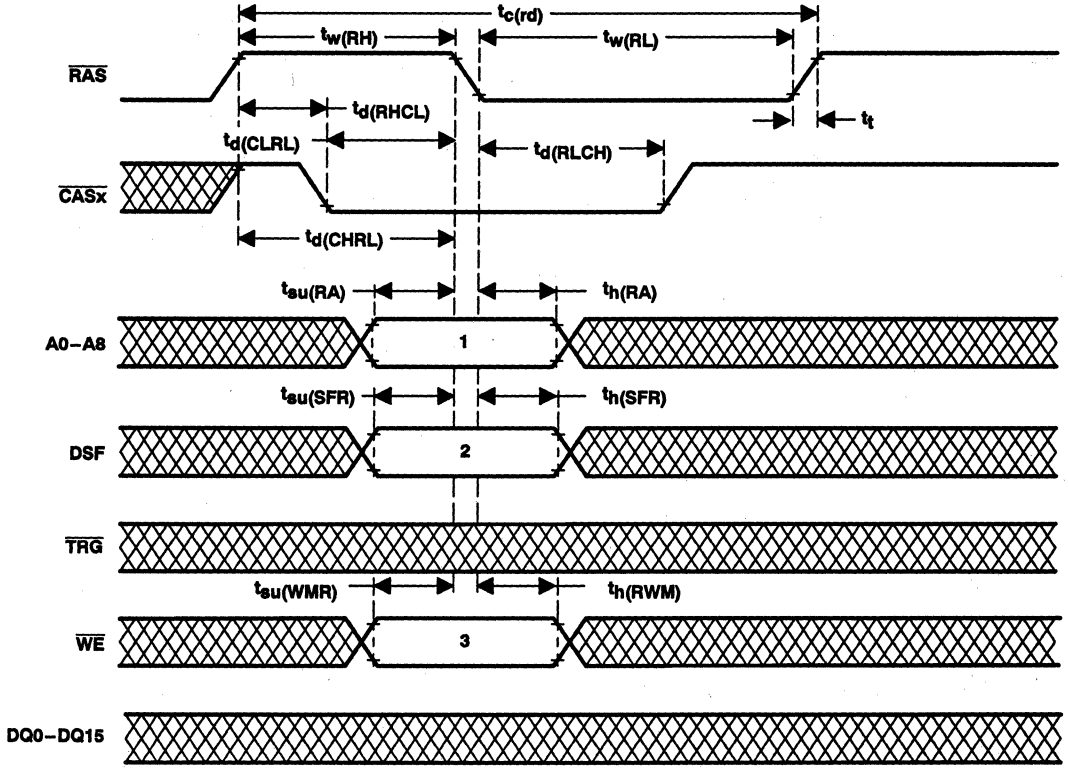


Figure 44. CBR-Refresh-Cycle Timing

Table 14. CBR-Cycle State Table

CYCLE	STATE		
	1	2	3
CBR refresh with option reset	Don't care	L	H
CBR refresh with no reset	Don't care	H	H
$\overline{\text{CBR}}$ refresh with stop point set and no reset	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION

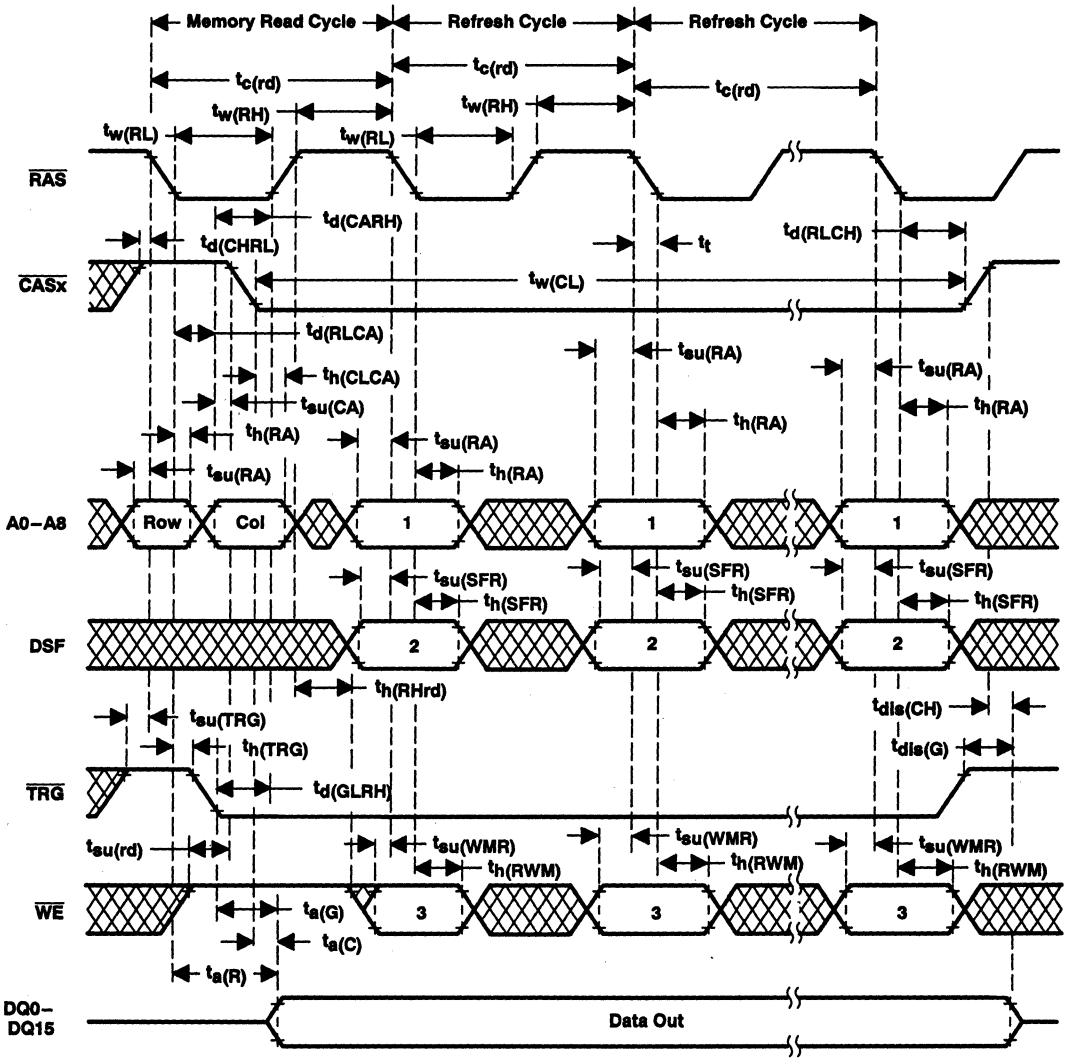
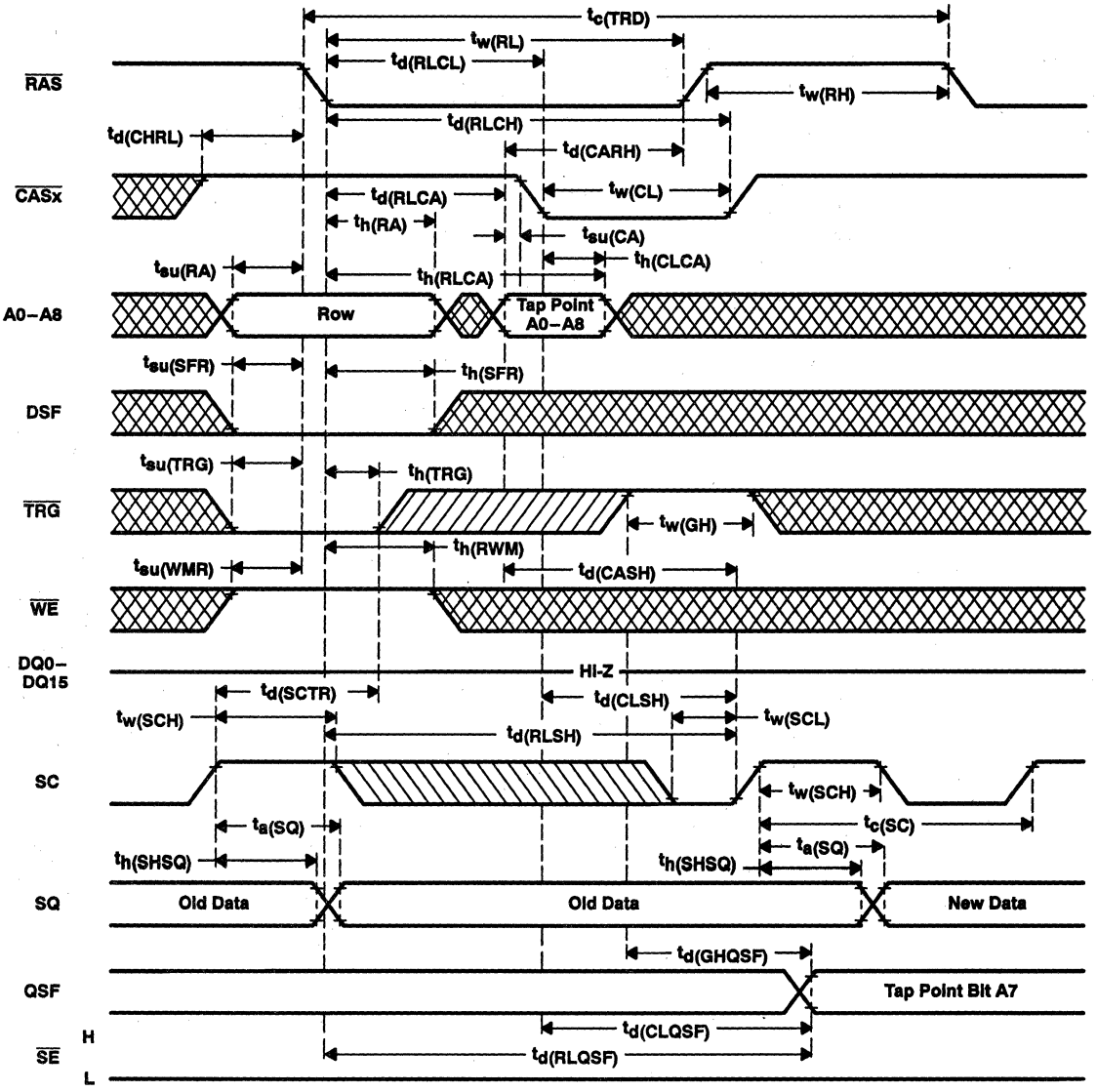


Figure 45. Hidden-Refresh-Cycle Timing

Table 15. Hidden-Refresh-Cycle State Table

CYCLE	STATE		
	1	2	3
CBR refresh with option reset	Don't care	L	H
CBR refresh with no reset	Don't care	H	H
CBR refresh with stop point set and no option reset	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register-transfer cycle. The memory-to-data-register-transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

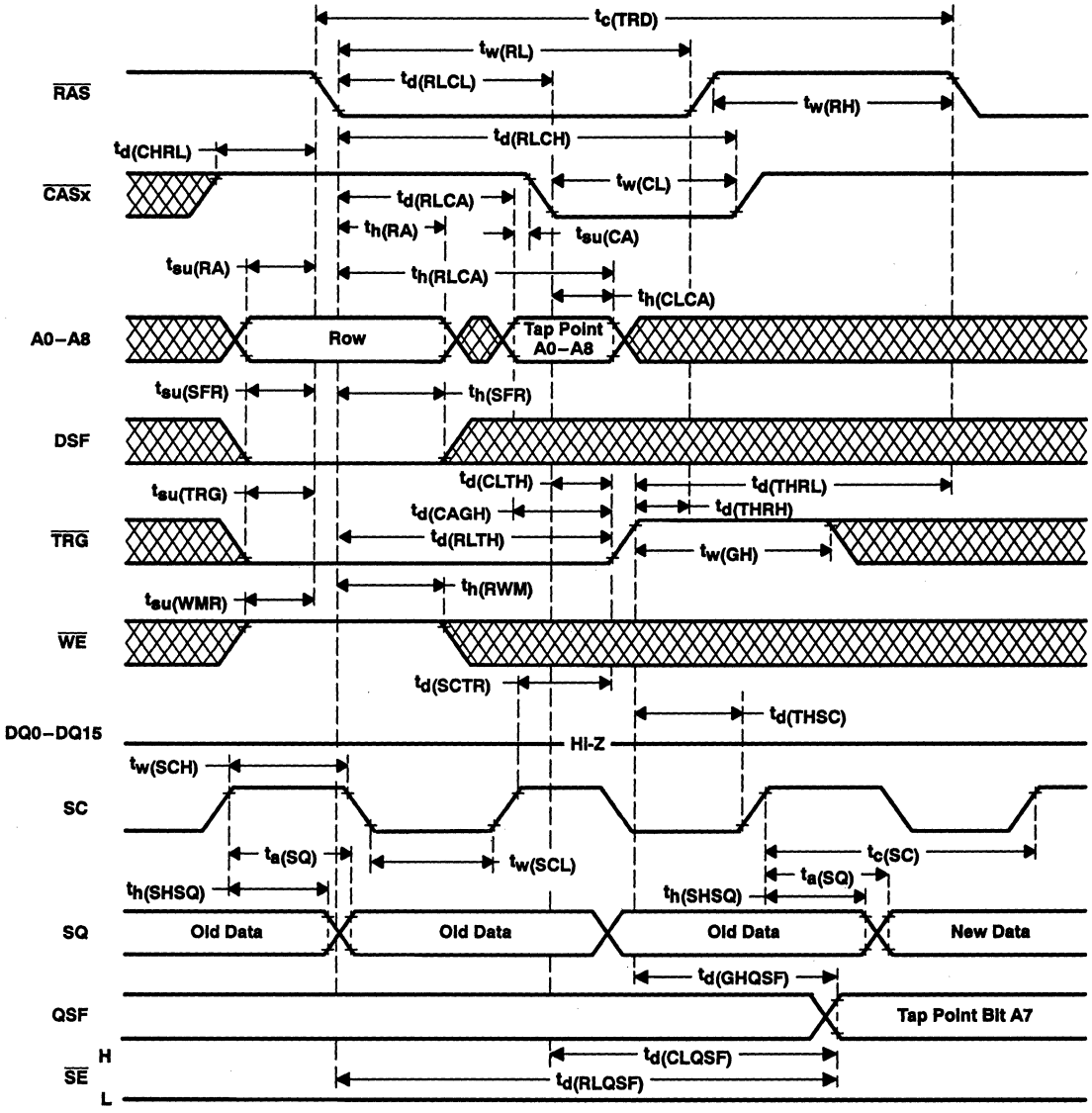
B. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0 – A7: register tap point; A8: identifies the half of the transferred row

D. Early-load operation is defined as $t_{h(TRG)}$ min < $t_{h(TRG)}$ < $t_{d(RLTH)}$ min.

Figure 46. Full-Register-Transfer Read Timing, Early-Load Operations

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register-transfer cycle. The memory-to-data-register-transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

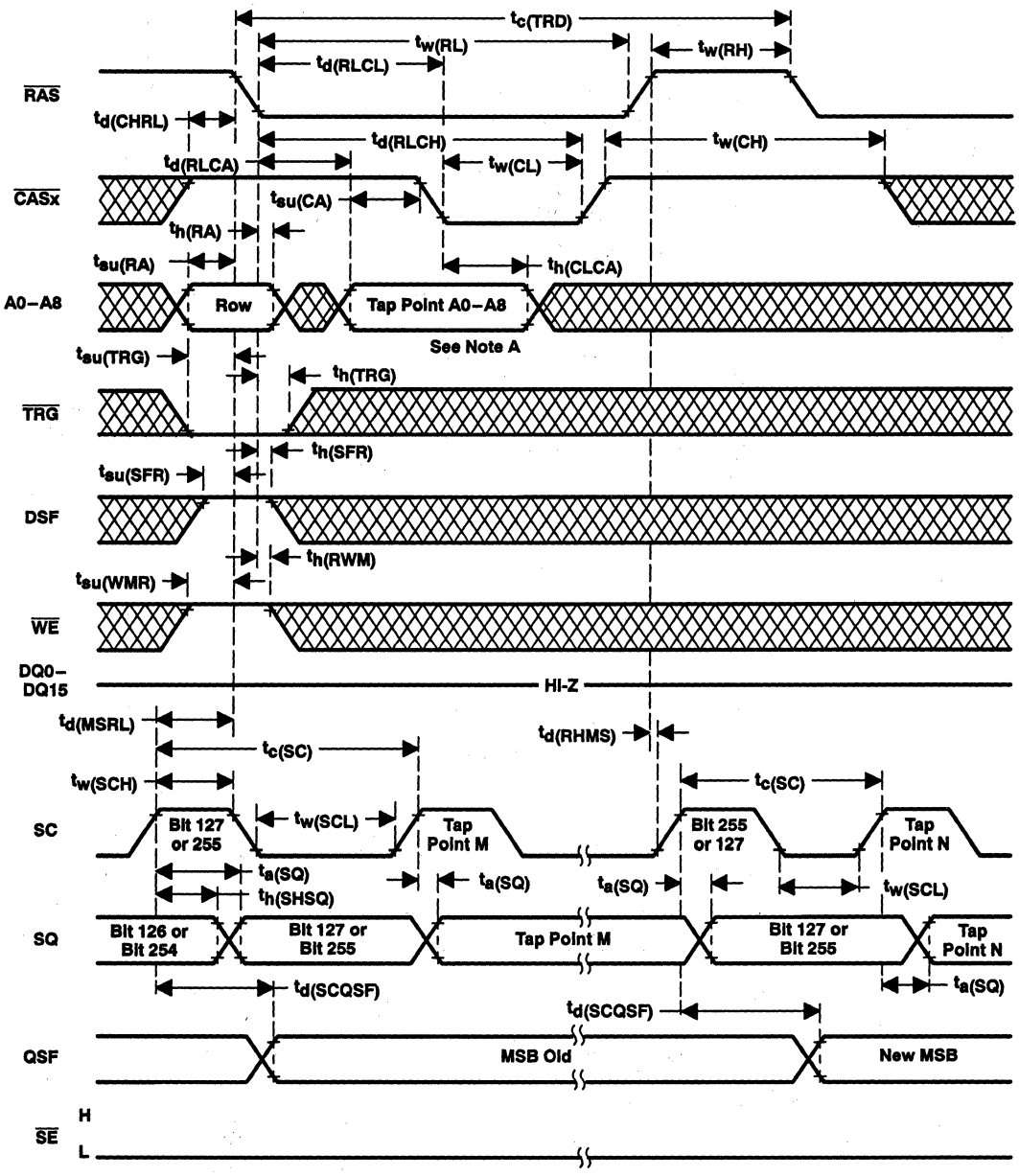
B. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0–A7: register tap point; A8: identifies the half of the transferred row

D. Late load operation is defined as $t_{d(THRH)} < 0$ ns.

Figure 47. Full-Register-Transfer Read Timing, Real-Time Load Operation/Late-Load Operation

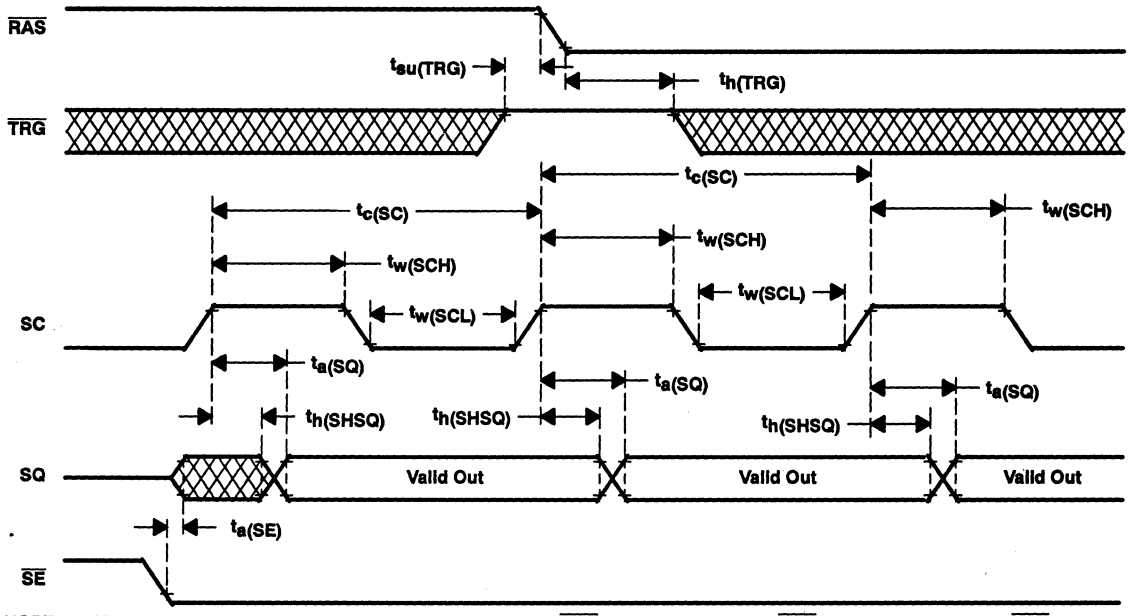
PARAMETER MEASUREMENT INFORMATION



NOTE A: A0–A6: tap point of the given half; A7: don't care; A8: identifies the DRAM row half

Figure 48. Split-Register-Transfer Read Timing

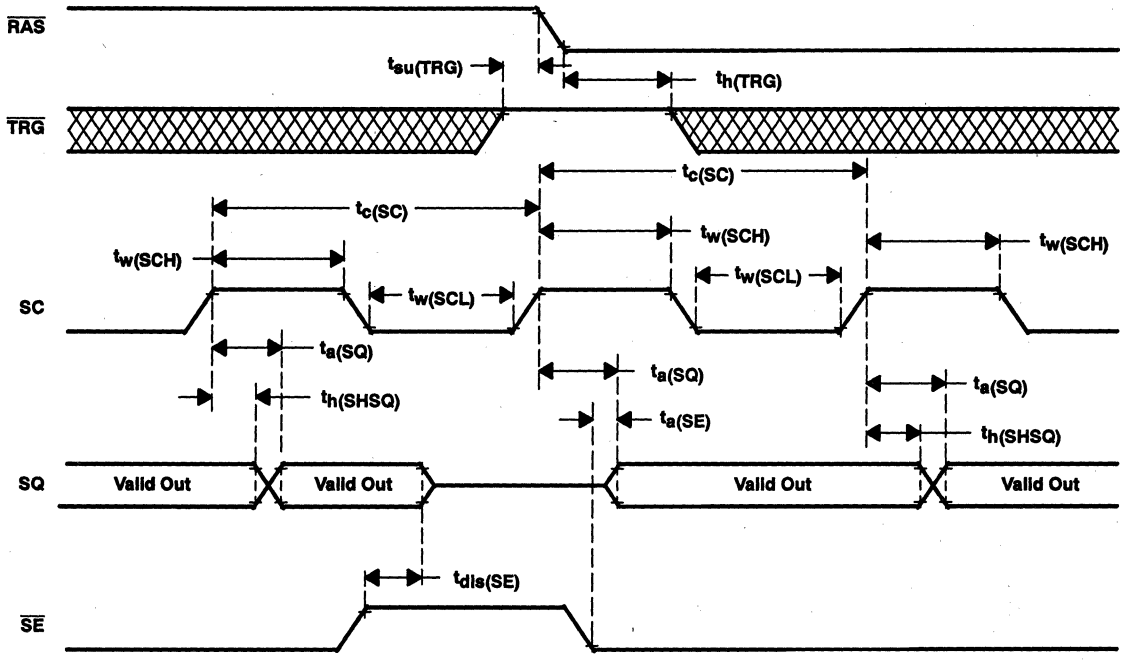
PARAMETER MEASUREMENT INFORMATION



NOTE A: While the data is being read through the serial-data register, $\overline{TRG}$ is a don't care, except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

Figure 49. Serial-Read-Cycle Timing ($\overline{SE}$ = V_{IL})

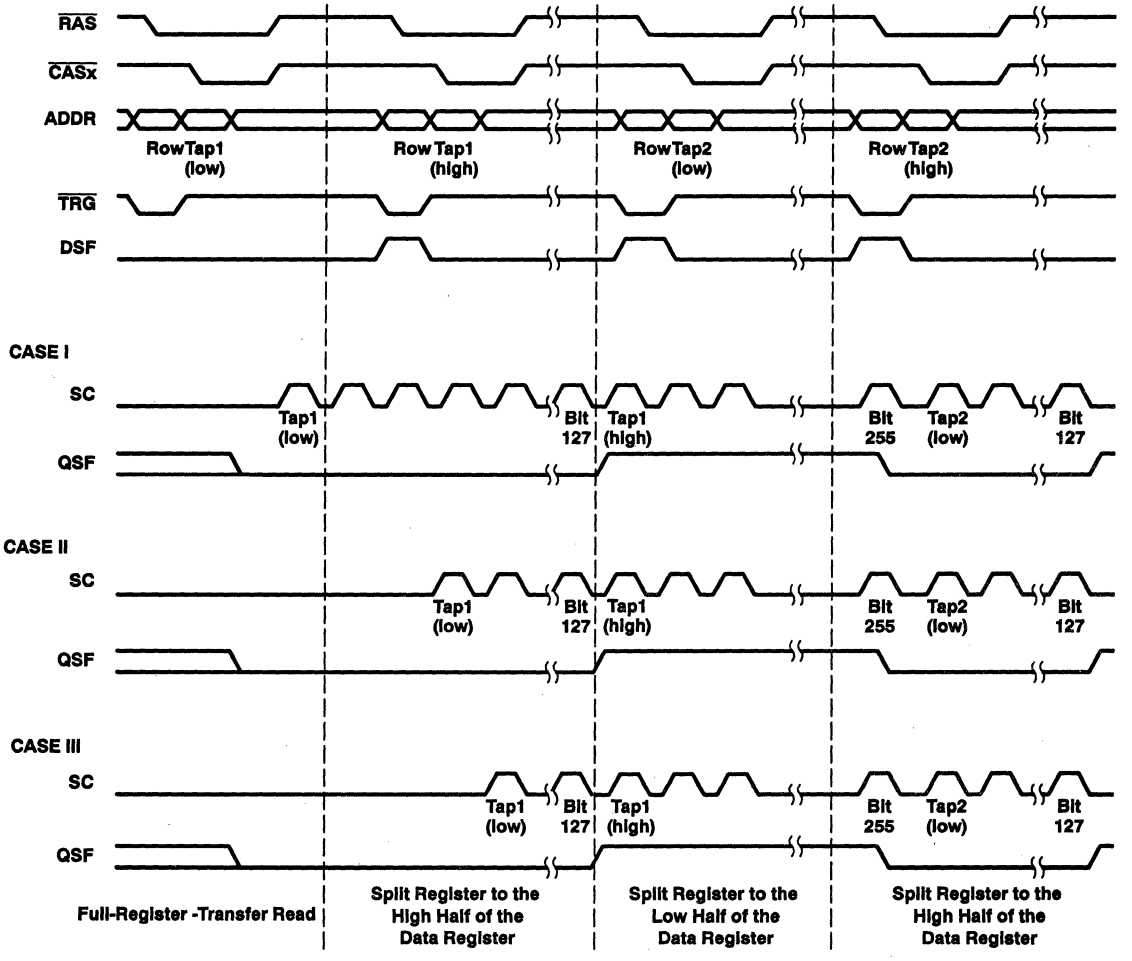
PARAMETER MEASUREMENT INFORMATION



NOTE A: While the data is being read through the serial-data register, $\overline{TRG}$ is a don't care except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

Figure 50. Serial-Read-Cycle Timing ($\overline{SE}$-Controlled Read)

PARAMETER MEASUREMENT INFORMATION

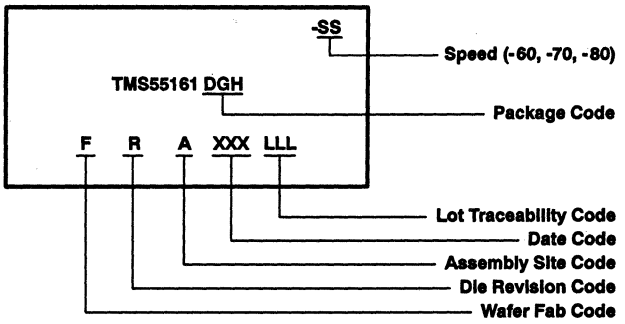


NOTES: A. In order to achieve proper split-register operation, a full-register-transfer read should be performed before the first split-register-transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can then begin either after the full-register-transfer read cycle (CASE I), during the first split-register-transfer cycle (CASE II), or even after the first split-register-transfer cycle (CASE III). There is no minimum requirement of SC clock between the full-register-transfer read cycle and the first split-register cycle.

B. A split-register-transfer into the inactive half is not allowed until $t_{d(MSRL)}$ is met. $t_{d(MSRL)}$ is the minimum delay time between the rising edge of the serial clock of the last bit (bit 127 or 255) and the falling edge of $\overline{RAS}$ of the split-register-transfer cycle into the inactive half. After the $t_{d(MSRL)}$ requirement is met, the split-register-transfer into the inactive half must also satisfy the minimum $t_{d(RHMS)}$ requirement. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register-transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 127 or 255).

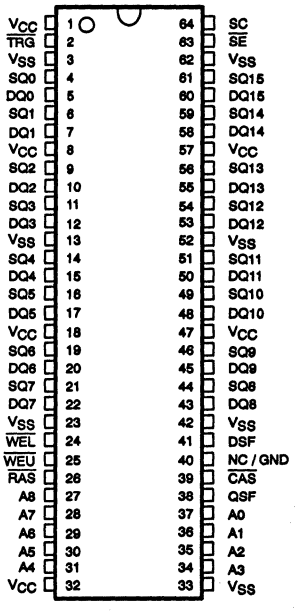
Figure 51. Split-Register Operating Sequence

device symbolization



- **Organization:**
  - **DRAM : 262 144 Words × 16 Bits**
  - **SAM: 256 Words × 16 Bits**
- **Dual-Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Data Transfer Function From the DRAM to the Serial Data Register**
- **(4 × 4) × 4 Block-Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle From the 16-Bit On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O. Two Write-Per-Bit Modes to Simplify System Design**
- **Byte Write Control ($\overline{WEL}$, $\overline{WEU}$) Provides Flexibility**
- **Extended Data Output for Faster System Cycle Time**
- **Enhanced Page-Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) and Hidden Refresh Modes**
- **Long Refresh Period**
  Every 8 ms (Max)
- **Up to 55-MHz Uninterrupted Serial Data Streams**
- **256 Selectable Serial Register Starting Locations**
- **$\overline{SE}$-Controlled Register Status QSF**
- **Split Register-Transfer Read for Simplified Real-Time Register Load**
- **Programmable Split-Register Stop Point**
- **3-State Serial Outputs Allow Easy Multiplexing of Video Data Streams**
- **All Inputs/Outputs and Clocks TTL Compatible**
- **Compatible With JEDEC Standards**
- **Texas Instruments EPIC™ CMOS Process**
- **Designed to Work With the Industry-Leading Texas Instruments Graphics Family**
- **Performance Ranges:**

DGH PACKAGE
(TOP VIEW)



PIN NOMENCLATURE

A0–A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ15	DRAM Data I/O, Write Mask Data
DSF	Special Function Select
NC/GND	No Connect/Ground (Important: not connected internally to V_{SS})
QSF	Special Function Output
$\overline{RAS}$	Row-Address Strobe
SC	Serial Clock
$\overline{SE}$	Serial Enable
SQ0–SQ15	Serial Data Output
$\overline{TRG}$	Output Enable, Transfer Select
V_{CC}	5-V Supply (TYP)
V_{SS}	Ground
$\overline{WEL}$, $\overline{WEU}$	DRAM Byte Write Enable Selects

	ACCESS TIME ROW ENABLE $t_{a(R)}$ (MAX)	ACCESS TIME SERIAL DATA $t_{a(SQ)}$ (MAX)	DRAM CYCLE TIME $t_{c(W)}$ (MIN)	DRAM PAGE MODE $t_{c(P)}$ (MIN)	SERIAL CYCLE TIME $t_{c(SC)}$ (MIN)	OPERATING CURRENT SERIAL PORT STANDBY I_{CC1} (MAX)	OPERATING CURRENT SERIAL PORT ACTIVE I_{CC1A} (MAX)
TMS55166-60	60 ns	15 ns	110 ns	30 ns	18 ns	180 mA	225 mA
TMS55166-70	70 ns	20 ns	130 ns	30 ns	22 ns	165 mA	205 mA
TMS55166-80	80 ns	25 ns	150 ns	35 ns	30 ns	150 mA	185 mA

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description

The TMS55166 multiport video RAM is a high-speed dual-ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 16 bits each interfaced to a serial data register [serial-access memory (SAM)] organized as 256 words of 16 bits each. The TMS55166 supports three basic types of operation: random access to and from the DRAM, serial access from the serial register, and transfer of data from any row in the DRAM to the serial register. Except during transfer operations, the TMS55166 can be accessed simultaneously and asynchronously from the DRAM and SAM ports.

The TMS55166 is equipped with several features designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's (4 × 4) × 4 block-write feature. The block-write mode allows 16 bits of data (present in an on-chip color data register) to be written to any combination of four adjacent column address locations. As many as 64 bits of data can be written to memory during each $\overline{CAS}$ cycle time. Also on the DRAM port, a write mask or a write-per-bit feature allows masking of any combination of the 16 inputs/outputs on any write cycle. The persistent write-per-bit feature uses a mask register which, once loaded, can be used on subsequent write cycles without reloading. The TMS55166 also offers byte control. Byte control can be applied in write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. The TMS55166 also offers extended output mode. The extended output mode is effective in both the page-mode and standard DRAM cycles.

The TMS55166 offers a split-register-transfer read (DRAM to SAM) feature for the serial register (SAM port). This feature enables real-time register load implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. For applications not requiring real-time register load (for example, loads done during CRT retrace periods), the full-register mode of operation is retained to simplify system design.

The SAM port is designed for maximum performance. Data can be accessed from the SAM at serial rates up to 55 MHz. During the split-register-transfer read operations, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, QSF, is included to indicate which half of the serial register is active.

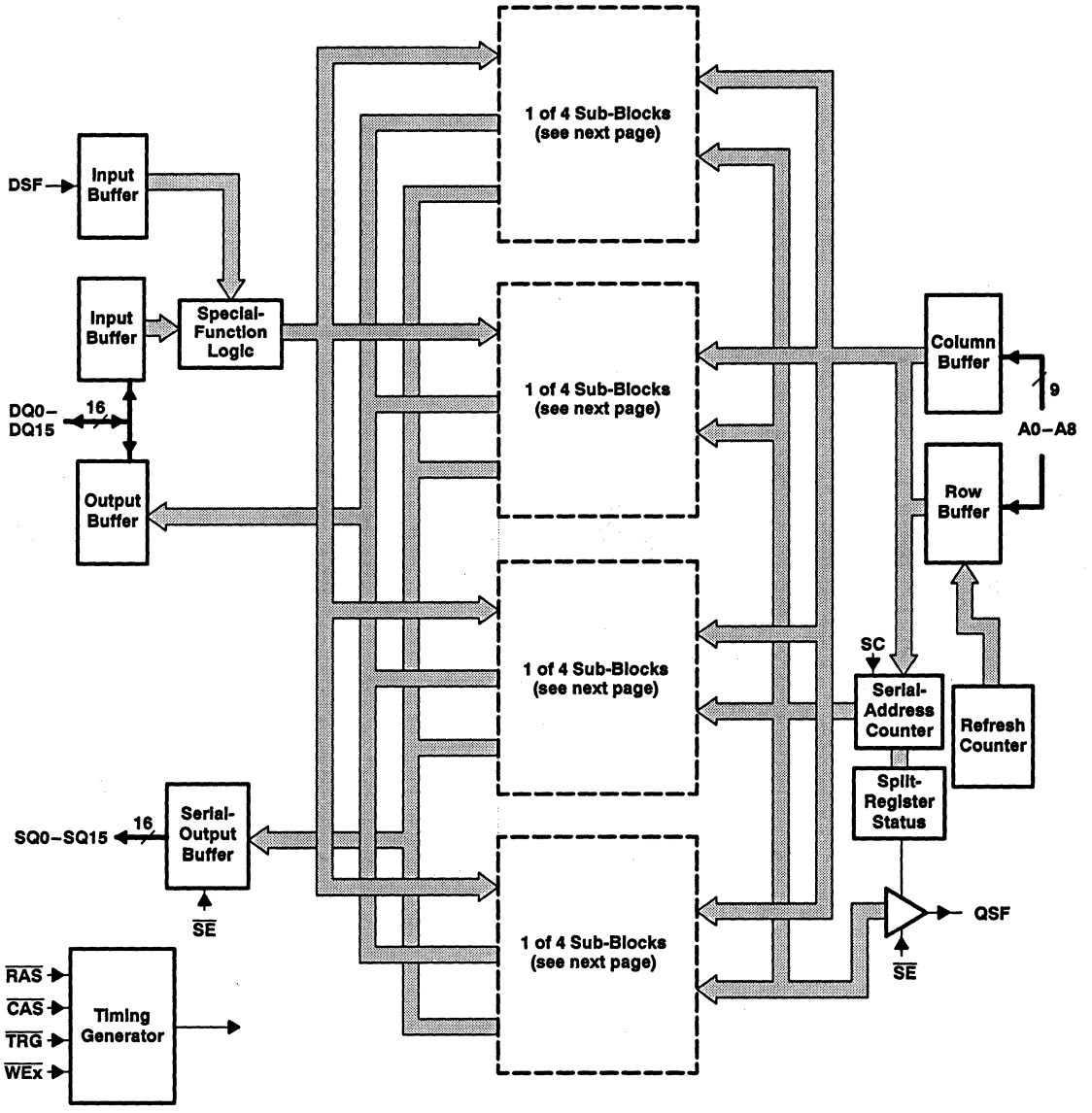
All inputs, outputs, and clock signals on the TMS55166 are compatible with Series 74 TTL. All address lines and data-in lines are latched on chip to simplify system design. All data outs are unlatched to allow greater system flexibility.

The TMS55166 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The TMS55166 is offered in a 64-pin small-outline gull-wing-leaded package (DGH suffix) for direct surface mounting.

The TMS55166 and other TI multiport video RAMs are supported by a broad line of graphics processors and control devices from Texas Instruments.

functional block diagram



functional block diagram (continued)

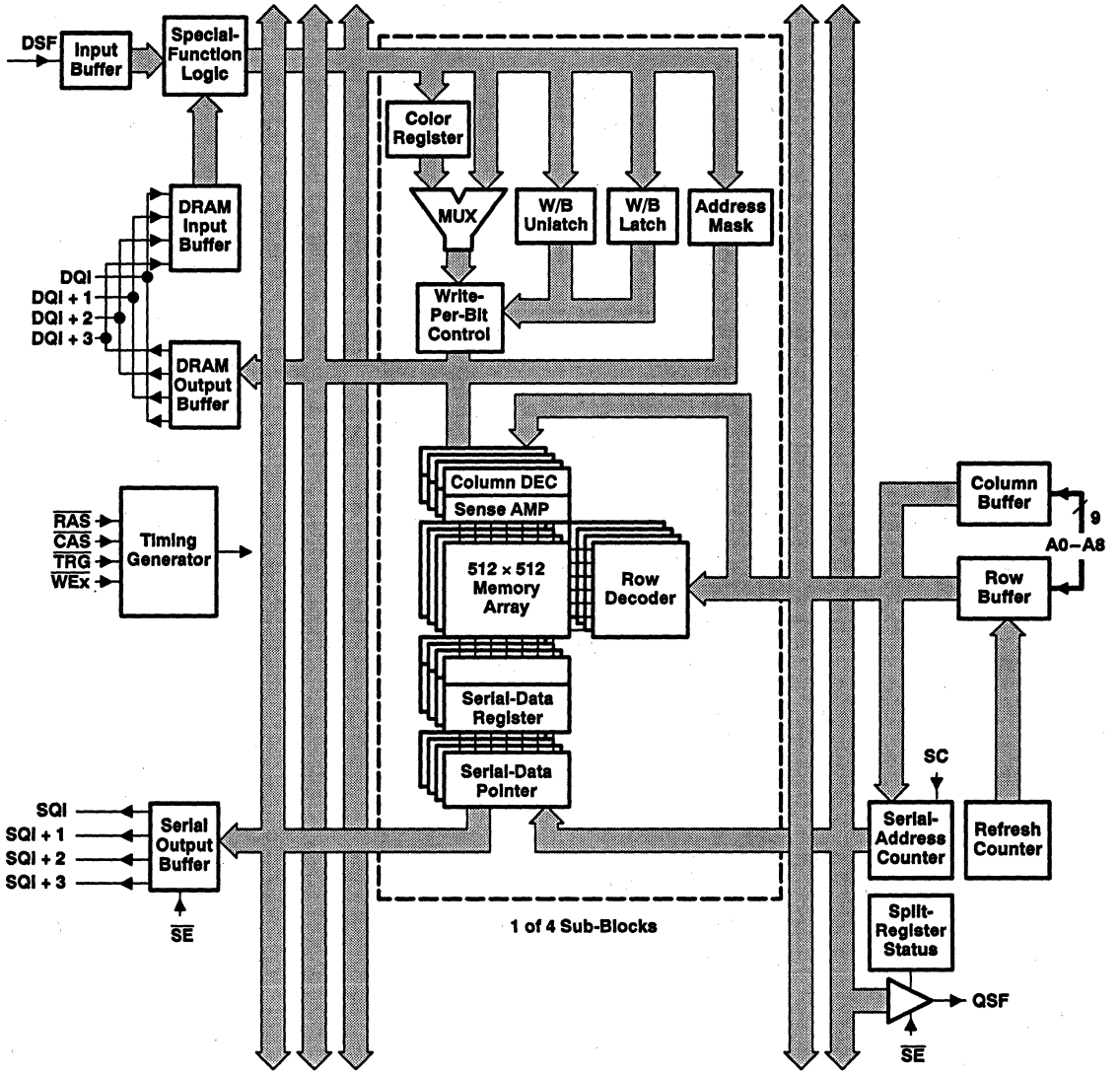


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Table 1. Function Table

FUNCTION	RAS FALL				CAS FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CAS	TRG	WEx‡	DSF	DSF	RAS	CAS§	RAS	WEL WEU CAS	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)★	L	X	H	H	X	X	X	X	X	CBRN
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
Load write mask register □	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
X = Don't care
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled

† DQ0–DQ15 are latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later.
‡ Logic L is selected when either or both $\overline{WEL}$ and $\overline{WEU}$ are low.
§ The column address and block address are latched on the falling edge of $\overline{CAS}$.
¶ CBRS cycle should be performed immediately after the power-up initialization cycle.
# A0–A3, A8: don't care; A4–A7 : stop-point code
‖ CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
★ CBR refresh (no reset) mode will not end persistent write-per-bit mode or stop-point mode.
□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.

Table 2. Pin Description Versus Operational Mode

PIN	DRAM	TRANSFER	SAM
A0–A8	Row, column address	Row address, tap point	
$\overline{CAS}$	Column-address strobe, DQ output enable	Tap-address strobe	
DQ	DRAM data I/O, Write mask		
DSF	Block-write enable Write-mask-register-load enable Color-register-load enable CBR (option reset)	Split-register-transfer enable	
$\overline{RAS}$	Row-address strobe	Row-address strobe	
$\overline{SE}$			SQ output enable, QSF output enable
SC			Serial clock
SQ			Serial data output
$\overline{TRG}$	DQ output enable	Transfer enable	
$\overline{WEL}$ $\overline{WEU}$	Write enable, Write-per-bit enable		
QSF			Serial-register status
NC/GND	Make no external connection or tie to system GND		
V_{CC}†	5-V supply		
V_{SS}†	Ground		

† For proper device operation, all V_{CC} pins must be connected to a 5-V supply and all V_{SS} pins must be tied to ground.

pin definitions

address (A0–A8)

Eighteen address bits are required to decode one of 262 144 storage cell locations. Nine row-address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Nine column-address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and the falling edge of $\overline{CAS}$.

During the full-register-transfer read operation, the states of A0–A8 are latched on the falling edge of $\overline{RAS}$ to select one of the 512 rows where the transfer occurs. At the falling edge of $\overline{CAS}$, the column-address bits A0–A8 are latched. The most significant column-address bit (A8) selects which half of the row is transferred to the SAM. The appropriate 8-bit column address (A0–A7) selects one of 256 tap points (starting positions) for the serial data output.

During the split-register-transfer read operation, address bit A7 is ignored at the falling edge of $\overline{CAS}$. An internal counter selects which half of the register is used. If the high half of the SAM is currently in use, the low half of the SAM is loaded with the low half of the DRAM half row, and vice versa. Column address (A8) selects the DRAM half row. The remaining seven address bits (A0–A6) are used to select 1 of 127 possible starting locations within the SAM. Locations 127 and 255 are not valid tap points.

row-address strobe ($\overline{RAS}$)

$\overline{RAS}$ is similar to a chip enable, so that all DRAM cycles and transfer cycles are initiated by the falling edge of $\overline{RAS}$. $\overline{RAS}$ is a control input that latches the states of the row address, $\overline{WEL}$, $\overline{WEU}$, $\overline{TRG}$, $\overline{CAS}$, and DSF onto the chip to invoke DRAM and transfer functions of the TMS55166.

column-address strobe ($\overline{CAS}$)

$\overline{CAS}$ is a control input that latches the states of the column address and DSF to control DRAM and transfer functions of the TMS55166. $\overline{CAS}$ also acts as output enable for the DRAM output pins, DQ0–DQ15.

In transfer operations, address bits A0–A8 are latched at the falling edge of $\overline{CAS}$ as the start position (tap) for the serial data output (SQ0–SQ15).

output enable/transfer select ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either DRAM or transfer operation as $\overline{RAS}$ falls. For DRAM operation, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. During DRAM operation, $\overline{TRG}$ functions as an output enable for the DRAM output pins, DQ0–DQ15. For transfer operation, $\overline{TRG}$ must be brought low before $\overline{RAS}$ falls.

write mask select, write enable ($\overline{WEL}$, $\overline{WEU}$)

In DRAM operation, $\overline{WEL}$ enables data to be written to the lower byte (DQ0–DQ7) and $\overline{WEU}$ enables data to be written to the upper byte (DQ8–DQ15) of the DRAM. Both $\overline{WEL}$ and $\overline{WEU}$ have to be held high together to select the read mode. Bringing either or both $\overline{WEL}$ and $\overline{WEU}$ low selects the write mode.

$\overline{WEL}$ and $\overline{WEU}$ are also used to select the DRAM write-per-bit mode of operation. If either or both $\overline{WEL}$ and $\overline{WEU}$ are brought low on the falling edge of $\overline{RAS}$, the write-per-bit operation is invoked. The TMS55166 supports both the nonpersistent write-per-bit mode and the persistent write-per-bit mode.

special function select (DSF)

The DSF input is latched on the falling edge of $\overline{RAS}$ or $\overline{CAS}$ similar to an address. DSF determines which of the following functions are invoked on a particular cycle:

- CBR refresh with no reset (CBRN)
- CBR refresh with no reset and stop-point set (CBRS)
- Block write (BW, BWM)
- Loading write-mask register for the persistent write-per-bit mode (LMR)
- Loading write-color register for the block-write mode (LCR)
- Split-register-transfer read (SRT)

DRAM data I/O, write mask data (DQ0–DQ15)

DRAM data is written or read through the common I/O DQ pins. The 3-state DQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state as long as either $\overline{TRG}$ or $\overline{CAS}$ is held high. Data does not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. The write mask is latched into the device via the random DQ pins by the falling edge of $\overline{RAS}$ and is used on all write-per-bit cycles. In a transfer operation, the DQ outputs remain in the high-impedance state for the entire cycle.

serial data outputs (SQ0–SQ15)

Serial data is read from the SQ pins. The SQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. The serial outputs are in the high-impedance (floating) state as long as the serial enable pin, $\overline{SE}$, is high. The serial outputs are enabled when $\overline{SE}$ is brought low.

serial clock (SC)

Serial data is accessed out of the data register from the rising edge of SC. The TMS55166 is designed to work with a wide range of clock duty cycles to simplify system design. There is no refresh requirement because the data registers that comprise the SAM are static. There is also no minimum SC operating frequency.

serial enable ($\overline{SE}$)

During serial-access operations, $\overline{SE}$ is used as an enable/disable for the SQ outputs. $\overline{SE}$ low enables the serial data output. $\overline{SE}$ high disables the serial data output. $\overline{SE}$ is also used as an enable/disable for output pin QSF.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is not disabled. External SC pulses increment the internal serial-address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low because the serial clock input buffer and the serial-address counter are not disabled by $\overline{SE}$.

special function output (QSF)

QSF is an output pin that indicates which half of the SAM is being accessed. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of the serial register (SAM). When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF changes state upon crossing a boundary between the two SAM halves.

During full-register-transfer operations, QSF can change state upon completing the cycle. This state is determined by the tap point loaded during the transfer cycle. The QSF output is enabled by $\overline{SE}$. If $\overline{SE}$ is high, the QSF output is in the high-impedance state.

no connect/ground (NC/GND)

The NC/GND pin should be tied to system ground or left floating for proper device operation.

functional operation description

random access operation

Table 3. DRAM Function Table

FUNCTION	RAS FALL				CAS FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CAS	TRG	WEx‡	DSF	DSF	RAS	CAS§	RAS	WEL WEU CAS	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)★	L	X	H	H	X	X	X	X	X	CBRN
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
Load write-mask register □	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
X = Don't care
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled

† DQ0–DQ15 are latched on either the first falling edge of WEx or the falling edge of CAS, whichever occurs later.
‡ Logic L is selected when either or both WEL and WEU are low.
§ The column address and block address are latched on the falling edge of CAS.
¶ CBRS cycle should be performed immediately after the power-up initialization cycle.
# A0–A3, A8: don't care; A4–A7 : stop-point code
‖ CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
★ CBR refresh (no reset) mode will not end persistent write-per-bit mode or stop-point mode.
□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.

enhanced page mode

Enhanced-page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. This mode eliminates the time required for row-address setup, row-address hold, and address multiplex. The maximum $\overline{RAS}$ low time and minimum $\overline{CAS}$ page cycle time are used to determine the number of columns that can be accessed.

Unlike conventional page-mode operations, the enhanced page mode allows the TMS55166 to operate at a higher data bandwidth. Data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. A valid column address can be presented immediately after the row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low) if $t_{a(CA)}$ max (access time from column address) has been satisfied.

refresh

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refreshes are accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored, and the refresh row address is generated internally. Three types of CBR refresh cycles are available. The CBR refresh (option reset) ends the persistent write-per-bit mode and the stop-point mode. The CBRN and CBRS refreshes (no reset) do not end the persistent write-per-bit mode or the stop-point mode. The 512 rows of the DRAM do not necessarily need to be refreshed consecutively as long as the entire refresh is completed within the required time period, $t_{rf(MA)}$. The output buffers remain in the high-impedance state during the CBR refresh cycles regardless of the state of $\overline{TRG}$.

hidden refresh

A hidden refresh is accomplished by holding $\overline{CAS}$ low in the DRAM read cycle and cycling $\overline{RAS}$. The output data of the DRAM read cycle remains valid while the refresh is being carried out. Like the CBR refresh, the refreshed row addresses are generated internally during the hidden refresh.

$\overline{RAS}$-only refresh

A $\overline{RAS}$-only refresh is accomplished by cycling $\overline{RAS}$ at every row address. Unless $\overline{CAS}$ and $\overline{TRG}$ are low, the output buffers remain in the high-impedance state to conserve power. Externally generated addresses must be supplied during $\overline{RAS}$-only refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed.

extended data output

The TMS55166 features extended data output during DRAM accesses. While $\overline{RAS}$ and $\overline{TRG}$ are low, the DRAM output remains valid even when $\overline{CAS}$ returns high. The output remains valid until $\overline{WEx}$ is low, $\overline{TRG}$ is high, or both $\overline{CAS}$ and $\overline{RAS}$ are high. The extended-data-output mode functions in all read cycles including DRAM-read, page-mode-read, and read-modify-write cycles.

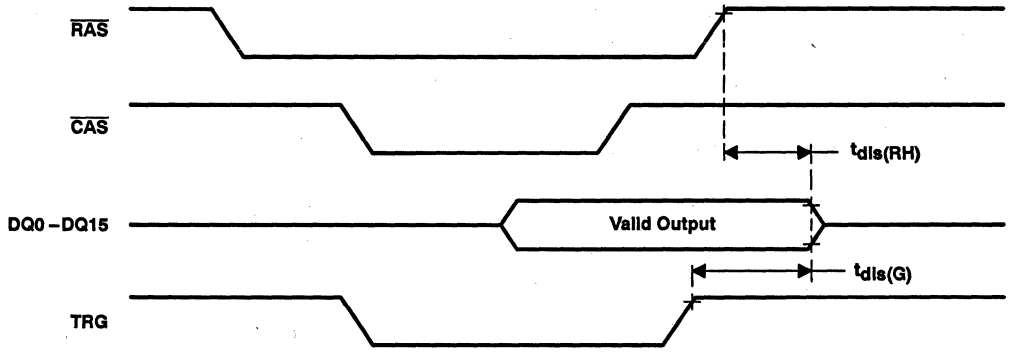


Figure 1. DRAM-Read Cycle With $\overline{RAS}$-Controlled Output

extended data output (continued)

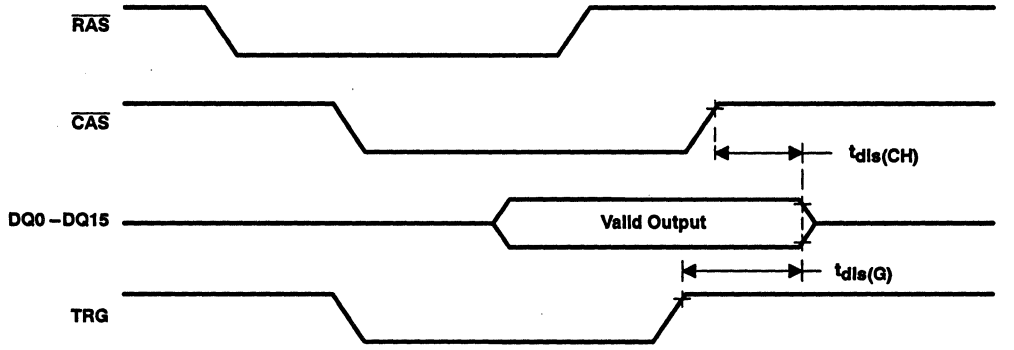


Figure 2. DRAM-Read Cycle With $\overline{CAS}$-Controlled Output

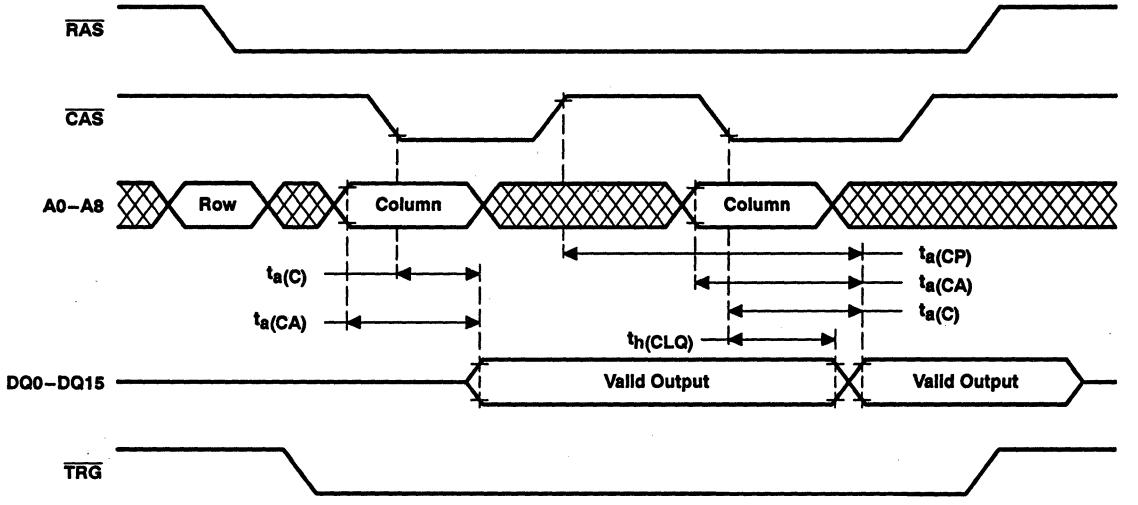
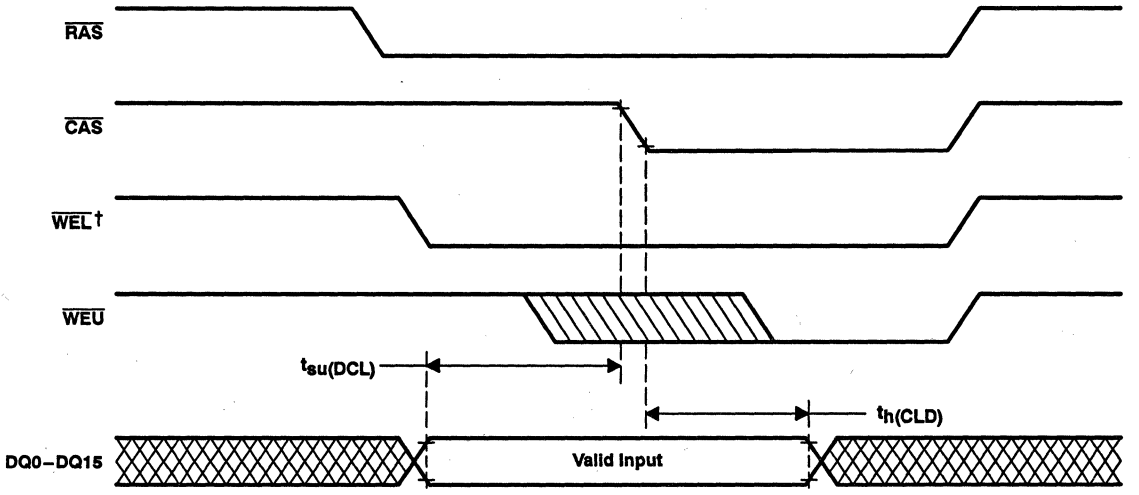


Figure 3. DRAM-Page-Read Cycle With Extended Output

byte-write operation

Byte-write operations can be applied in DRAM-write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. Holding either or both $\overline{WEL}$ and $\overline{WEU}$ low selects the write mode. In normal write cycles, $\overline{WEL}$ enables data to be written to the lower byte (DQ0–DQ7) and $\overline{WEU}$ enables data to be written to the upper byte (DQ8–DQ15). For early-write cycles, one $\overline{WEx}$ is brought low before $\overline{CAS}$ falls. The other $\overline{WEx}$ can be brought low before or after $\overline{CAS}$ falls. The data is strobed in with data setup and hold times for DQ0–DQ15 referenced to $\overline{CAS}$ (see Figure 4).



† Either $\overline{WEx}$ can be brought low prior to $\overline{CAS}$ to initiate an early-write cycle.

Figure 4. Example of an Early-Write Cycle

byte-write operation (continued)

For late-write or read-modify-write cycles, $\overline{WEL}$ and $\overline{WEU}$ are both held high before $\overline{CAS}$ falls. After $\overline{CAS}$ falls, either or both $\overline{WEL}$ and $\overline{WEU}$ are brought low to select the corresponding byte or bytes to be written. Data is strobed in by $\overline{WEL}$ and/or $\overline{WEU}$ with data setup and hold times for DQ0–DQ15 referenced to whichever $\overline{WEx}$ falls earlier (see Figure 5).

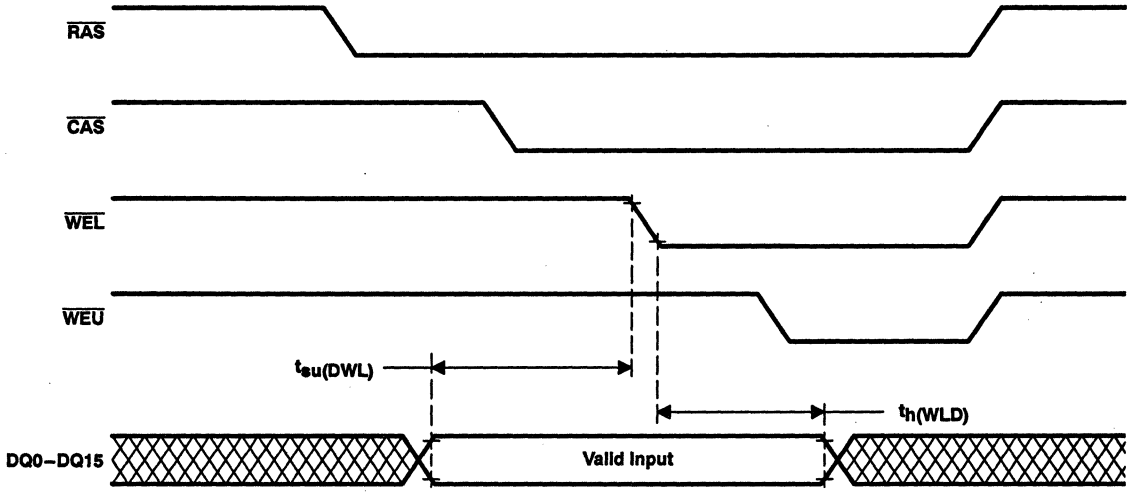


Figure 5. Example of a Late-Write Cycle

write-per-bit

The write-per-bit feature allows masking any combination of the 16 DQs on any write cycle. The write-per-bit operation is invoked when either or both $\overline{WEL}$ and $\overline{WEU}$ are held low on the falling edge of $\overline{RAS}$. Either individual $\overline{WEx}$ allows entry of the entire 16-bit mask on DQ0–DQ15. Byte control of the mask input is not allowed.

If both $\overline{WEL}$ and $\overline{WEU}$ are held high on the falling edge of $\overline{RAS}$, the write operation is performed without any masking. The TMS55166 offers two write-per-bit modes: the nonpersistent write-per-bit and the persistent write-per-bit.

nonpersistent write-per-bit

When either or both $\overline{WEL}$ and $\overline{WEU}$ are low on the falling edge of $\overline{RAS}$, the write mask is reloaded. A 16-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the 16 random I/Os are to be written and which are not. After $\overline{RAS}$ has latched the on-chip write-per-bit mask, input data is driven onto the DQ pins and is latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later. $\overline{WEL}$ enables the lower byte (DQ0–DQ7) to be written through the mask and $\overline{WEU}$ enables the upper byte (DQ8–DQ15) to be written through the mask. If a data low (write mask = 0) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data is not written to that I/O. If a data high (write mask = 1) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data is written to that I/O (see Figure 6).

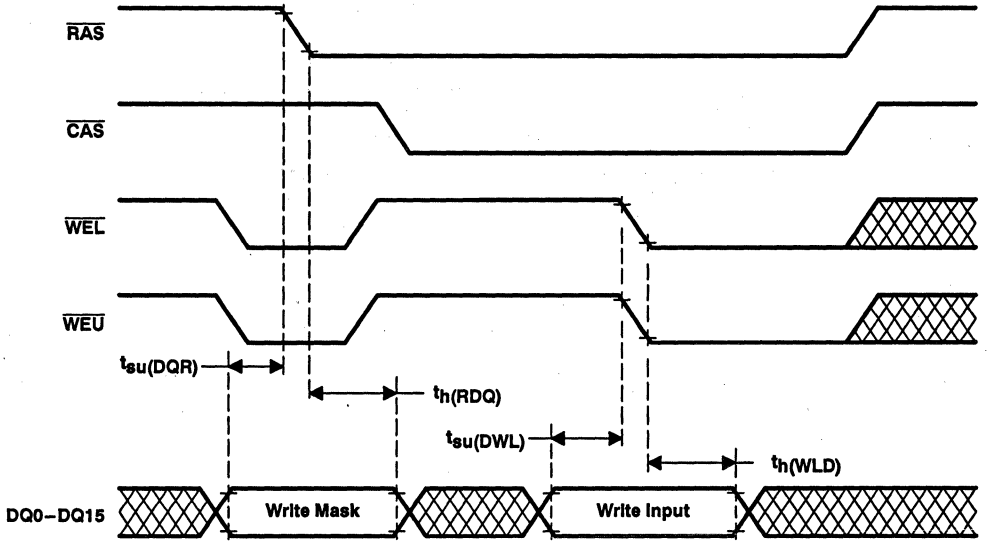


Figure 6. Example of a Nonpersistent Write-Per-Bit (Late-Write) Operation

persistent write-per-bit

The persistent write-per-bit mode is initiated only by performing a load-write-mask-register cycle first. In the persistent write-per-bit mode, the write-per-bit mask is not overwritten but remains valid over an arbitrary number of write cycles until another LMR cycle is performed or power is removed.

The load-write-mask-register cycle is performed using DRAM write-cycle timing except DSF is held high on the falling edge of $\overline{RAS}$ and held low on the falling edge of $\overline{CAS}$. A binary code is input to the write-mask register via the random I/O pins and latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later. Byte-write control can be applied to the write mask during the load-write-mask-register cycle. The persistent write-per-bit mode can then be used in exactly the same way as the nonpersistent write-per-bit mode except that the input data on the falling edge of $\overline{RAS}$ is ignored. When the device is set to the persistent write-per-bit mode, it remains in this mode and is reset only by a CBR refresh with option reset cycle (see Figure 7).

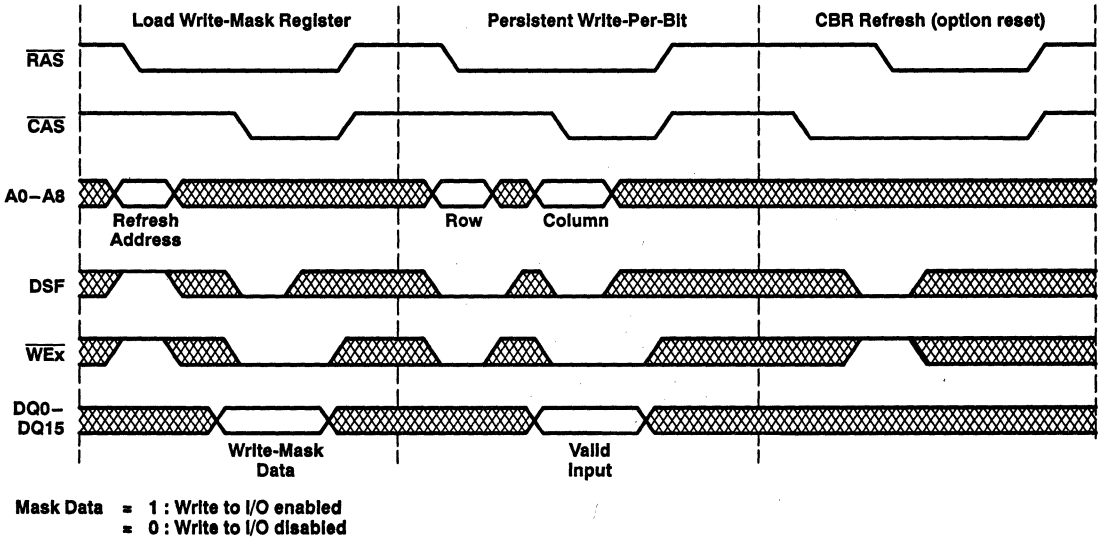


Figure 7. Example of a Persistent Write-Per-Bit Operation

block write

The block-write feature allows up to 64 bits of data to be written simultaneously to one row of the memory array. This function is implemented as (4 columns × 4 DQs) repeated in four quadrants. In this manner, each of the four one-megabit quadrants can have up to four consecutive columns written at a time with up to four DQs per column (see Figure 8).

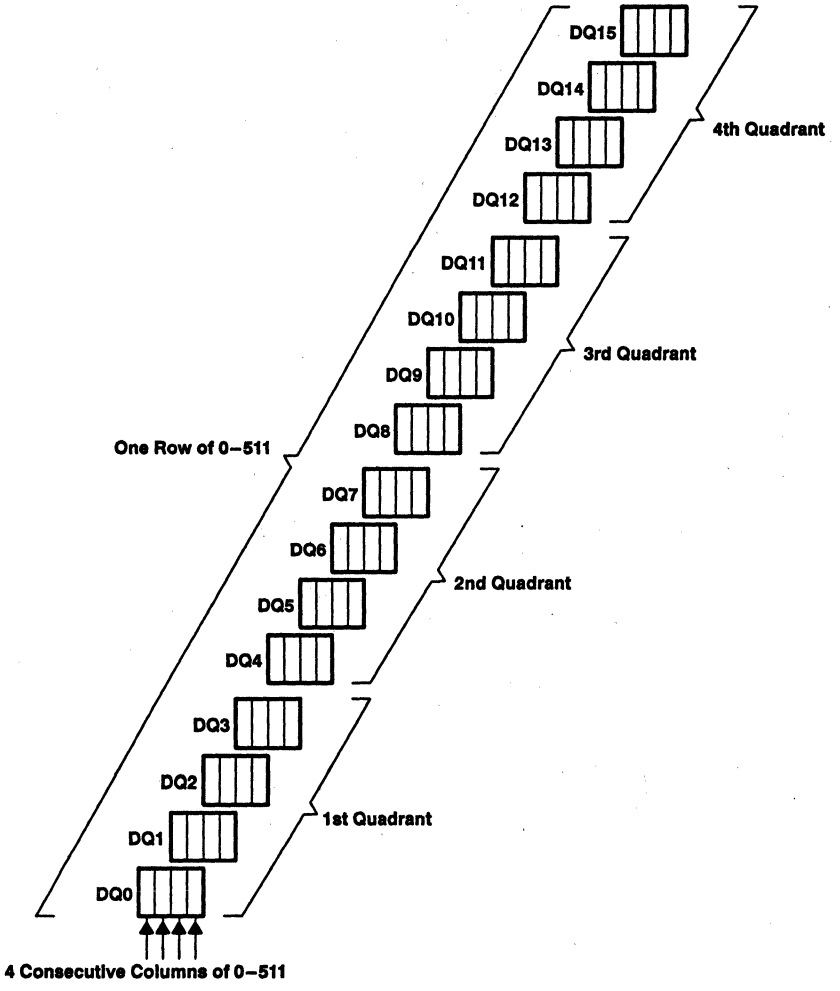


Figure 8. Block-Write Operaton

Each one-megabit quadrant has a 4-bit column mask to mask off any or all of the four columns from being written with data. Nonpersistent write-per-bit or persistent write-per-bit functions can be applied to the block-write operation to provide write-masking options. The DQ data is provided by four bits from the on-chip color register. Bits 0–3 from the 16-bit write-mask register, bits 0–3 from the 16-bit column-mask register, and bits 0–3 from the 16-bit color-data register configure the block write for the first quadrant, while bits 4–7, 8–11, and 12–15 of the corresponding registers control the other quadrants in a similar fashion (see Figure 9).

block write (continued)

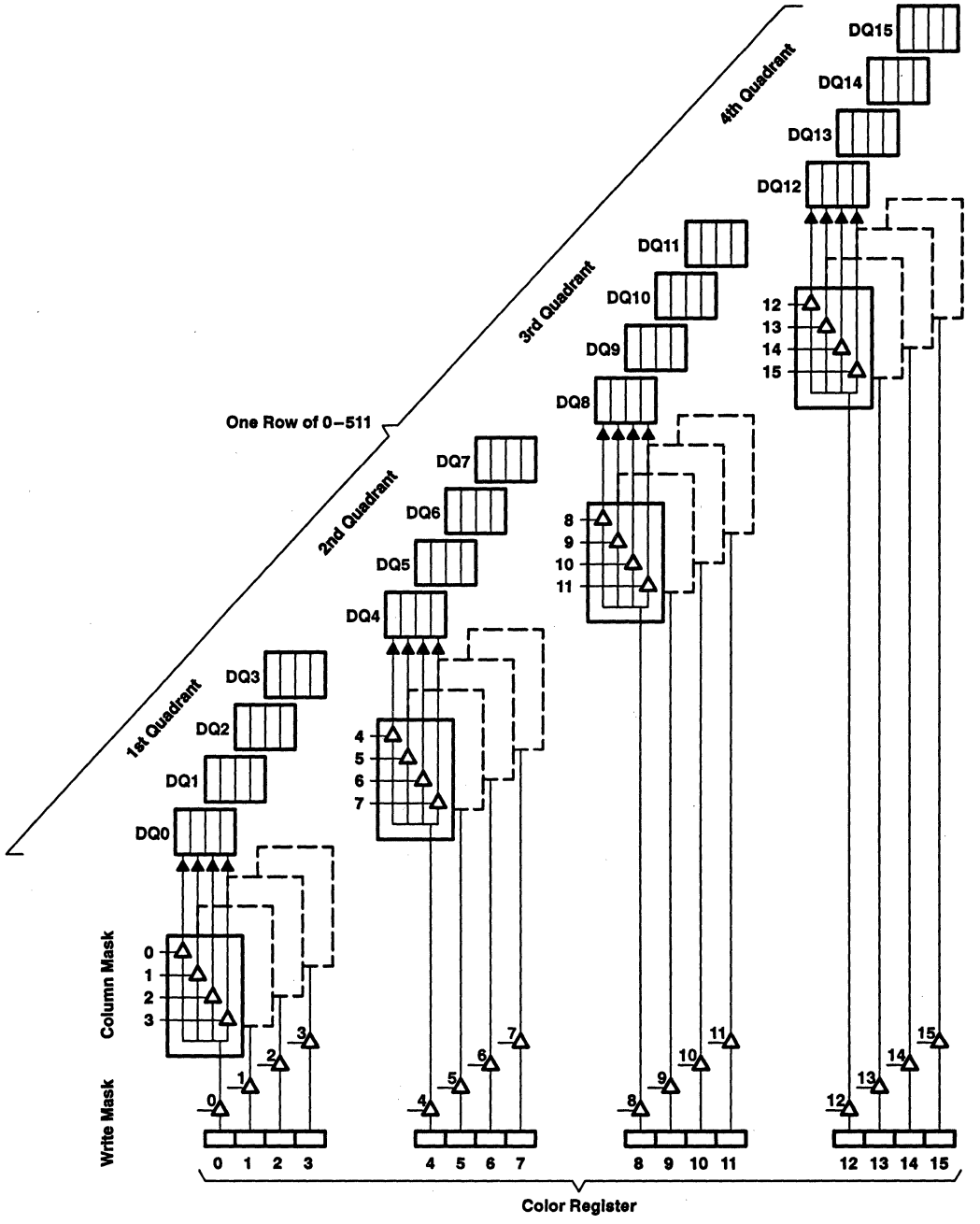


Figure 9. Block Write With Masks

block write (continued)

Every four columns make a block, which makes 128 blocks along one row. Block 0 comprises columns 0–3, block 1 comprises columns 4–7, block 2 comprises columns 8–11, etc., as shown in Figure 10.

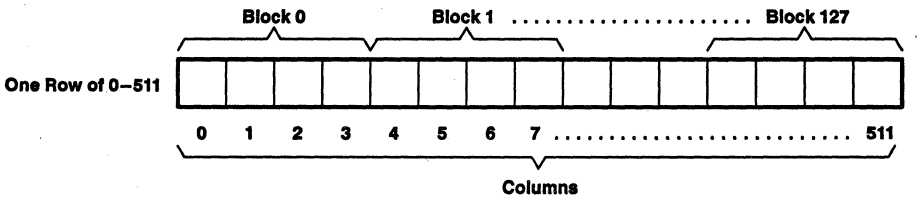


Figure 10. Block Columns Organization

During block-write cycles, only the seven most significant column addresses (A2–A8) are latched on the falling edge of $\overline{CAS}$ to decode one of the 128 blocks. Address bits A0–A1 are ignored. Each one-megabit quadrant has the same block selected.

A block-write cycle is entered in a manner similar to a DRAM write cycle except DSF is held high on the first falling edge of $\overline{CAS}$. As in a DRAM write operation, $\overline{WEL}$ and $\overline{WEU}$ enable the corresponding lower and upper DRAM DQ bytes to be written, respectively. The column-mask data is input via the DQs and is latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later. The 16-bit color-data register must be loaded prior to performing a block write as described below. Refer to the write-per-bit section for details on use of the write-mask capability allowing additional performance options.

Example of block write:

block-write column address = 110000000 (A0–A8 from left to right)

	bit 0			bit 15
color-data register =	1011	1011	1100	0111
write-mask register =	1110	1111	1111	1011
column-mask register =	1111	0000	0111	1010
	1st Quad	2nd Quad	3rd Quad	4th Quad

Column-address bits A0 and A1 are ignored. Block 0 (columns 0–3) is selected for each one-megabit quadrant. The first quadrant has DQ0–DQ2 written with bits 0–2 from the color-data register (101) to all four columns of block 0. DQ3 is not written and retains its previous data due to the write-mask register bit 3 being a 0.

The second quadrant (DQ4–DQ7) has all four columns masked off due to the column mask bits 4–7 being 0, so that no data is written.

The third quadrant (DQ8–DQ11) has its four DQs written with bits 8–11 from the color-data register (1100) to columns 1–3 of its block 0. Column 0 is not written and retains its previous data on all four DQs due to the column-mask-register bit 8 being 0.

The fourth quadrant (DQ12–DQ15) has DQ12, DQ14, and DQ15 written with bits 12, 14, and 15 from the color-data register to column 0 and column 2 of its Block 0. DQ13 retains its previous data on all columns due to the write mask. Columns 1 and 3 retain their previous data on all DQs due to the column mask. If the previous data for the quadrant was all 0s, the fourth quadrant would contain the data pattern shown in Figure 15 after the block-write operation shown in the previous example.

block write (continued)

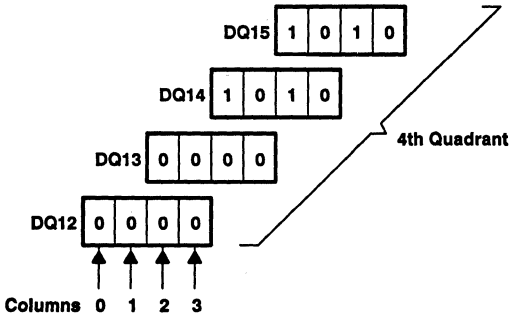
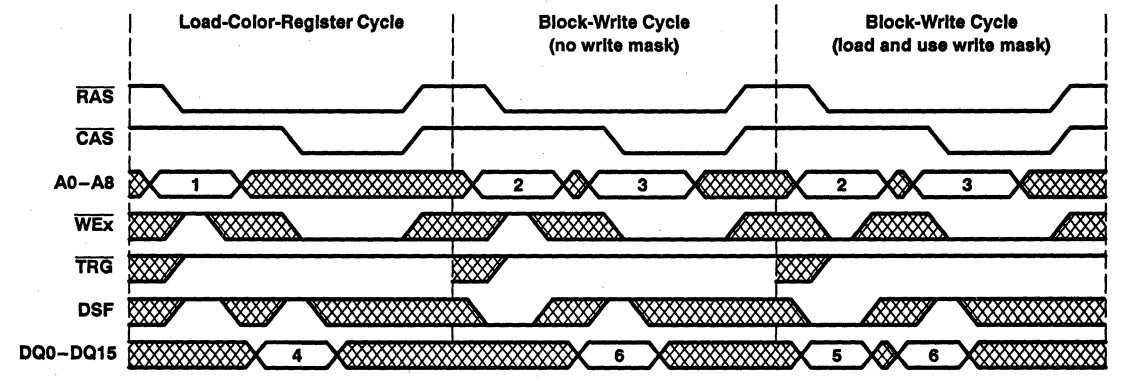


Figure 11. Example of Fourth Quadrant After Block-Write Operation

load color register

The load-color-register cycle is performed using normal DRAM write-cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. The color register is loaded from pins DQ0–DQ15, which are latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later. If only one $\overline{WEx}$ is low, only the corresponding byte of the color register is loaded. When the color register is loaded, it retains data until power is lost or until another load-color-register cycle is performed (see Figure 12 and Figure 13).



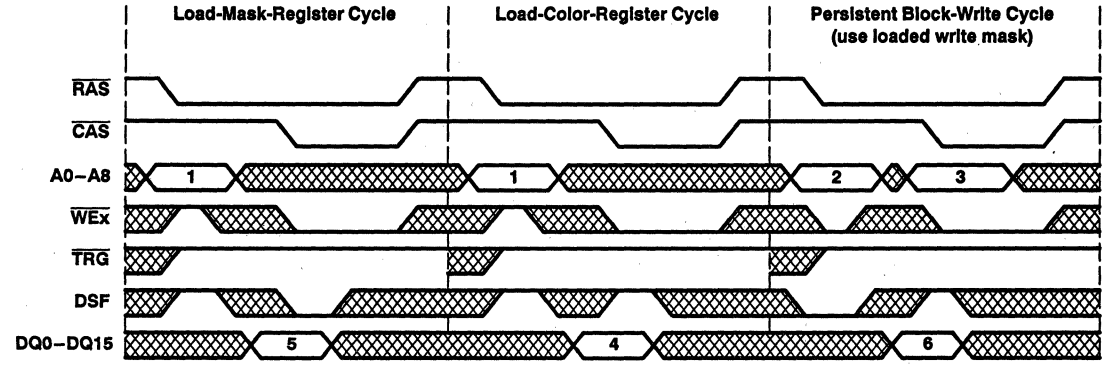
Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the falling edge of $\overline{CAS}$.
4. Color-register data
5. Write-mask data: DQ0–DQ15 are latched on the falling edge $\overline{RAS}$.
6. Column-mask data: DQi–DQi+3 (i = 0, 4, 8, 12) are latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later.

= don't care

Figure 12. Example of Block Writes

load color register (continued)



Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the falling edge of $\overline{CAS}$.
4. Color-register data
5. Write-mask data: DQ0–DQ15 are latched on the falling edge $\overline{RAS}$.
6. Column-mask data: DQi–DQi+3 (i = 0, 4, 8, 12) are latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later.

= don't care

Figure 13. Example of a Persistent Block Write

DRAM-to-SAM transfer operation

During the DRAM-to-SAM transfer operation, one half of a row (256 columns) in the DRAM array is selected to be transferred to the 256-bit serial-data register. The transfer operation is invoked by bringing $\overline{TRG}$ low and holding $\overline{WEx}$ high on the falling edge of $\overline{RAS}$. The state of DSF, which is latched on the falling edge of $\overline{RAS}$, determines whether the full-register-transfer read operation or the split-register-transfer read operation is performed.

Table 4. SAM Function Table

FUNCTION	$\overline{RAS}$ FALL				$\overline{CAS}$ FALL	ADDRESS		DQ0–DQ15		MNE CODE
	$\overline{CAS}$	$\overline{TRG}$	$\overline{WEx}$†	DSF	DSF	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$ $\overline{WEx}$	
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT

† Logic L is selected when either or both $\overline{WEL}$ and $\overline{WEU}$ are low.
X = don't care

full-register-transfer read

A full-register-transfer read operation loads data from a selected half of a row in the DRAM into the SAM. $\overline{TRG}$ is brought low and latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. The nine column-address bits (A0–A8) are latched at the falling edge of $\overline{CAS}$, where address bit A8 selects which half of the row is transferred. Address bits A0–A7 select one of the SAM's 256 available tap points from which the serial data is read out (see Figure 14).

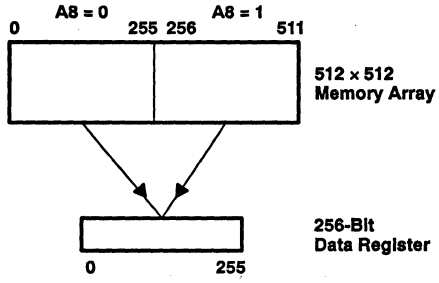


Figure 14. Full-Register-Transfer Read

A full-register-transfer read can be performed in three ways: early load, real-time load (or midline load), or late load. Each of these offers the flexibility of controlling the $\overline{TRG}$ trailing edge in the full-register-transfer read cycle (see Figure 15).

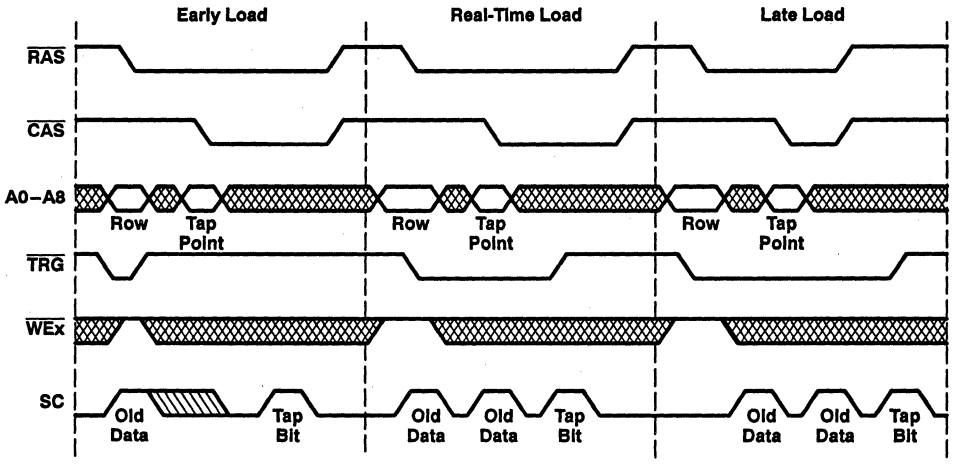


Figure 15. Example of Full-Register-Transfer Read Operations

split-register-transfer read

In the split-register-transfer read operation, the serial-data register is split into halves. The low half contains bits 0–127, and the high half contains bits 128–255. While one half is being read out of the SAM port, the other half can be loaded from the memory array.

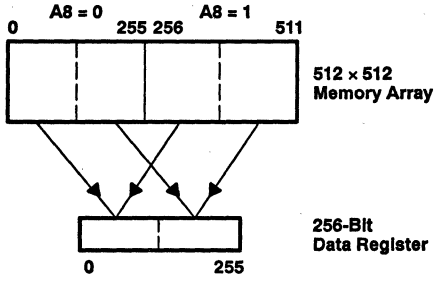
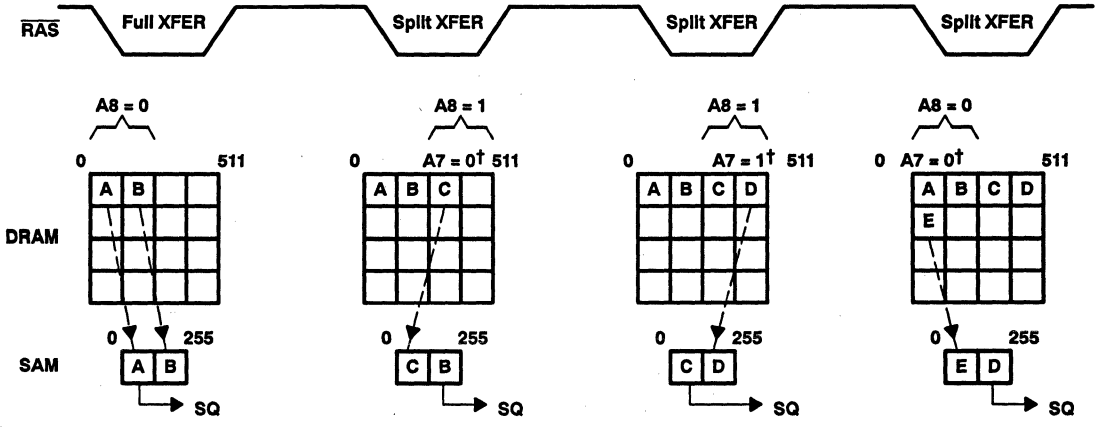


Figure 16. Split-Register-Transfer Read

To invoke a split-register-transfer read cycle, DSF is brought high, $\overline{TRG}$ is brought low, and both are latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. Eight of the nine column-address bits (A0–A6 and A8) are latched at the falling edge of $\overline{CAS}$. Column-address bit A8 selects which half of the row is to be transferred. Column-address bits A0–A6 select one of the 127 tap points in the specified half of the SAM. Column-address bit A7 is ignored, and the split-register-transfer is internally controlled to select the inactive register half.



† A7 shown is internally controlled.

Figure 17. Example of a Split-Register-Transfer Read Operation

A full-register-transfer read must precede the first split-register-transfer read to ensure proper operation. After the full-register-transfer read cycle, the first split-register-transfer read can follow immediately without any minimum SC clock requirement.

split-register-transfer read (continued)

QSF indicates which half of the register is being accessed during serial-access operation. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of the SAM. When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF changes state upon completing a full-register-transfer read cycle. The tap point loaded during the current transfer cycle determines the state of QSF. QSF also changes state when a boundary between two register halves is reached.

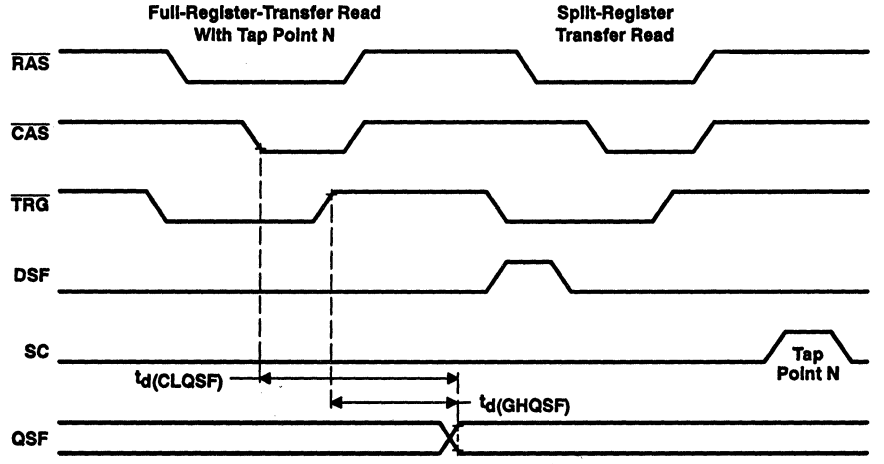


Figure 18. Example of a Split-Register-Transfer Read After a Full-Register-Transfer Read

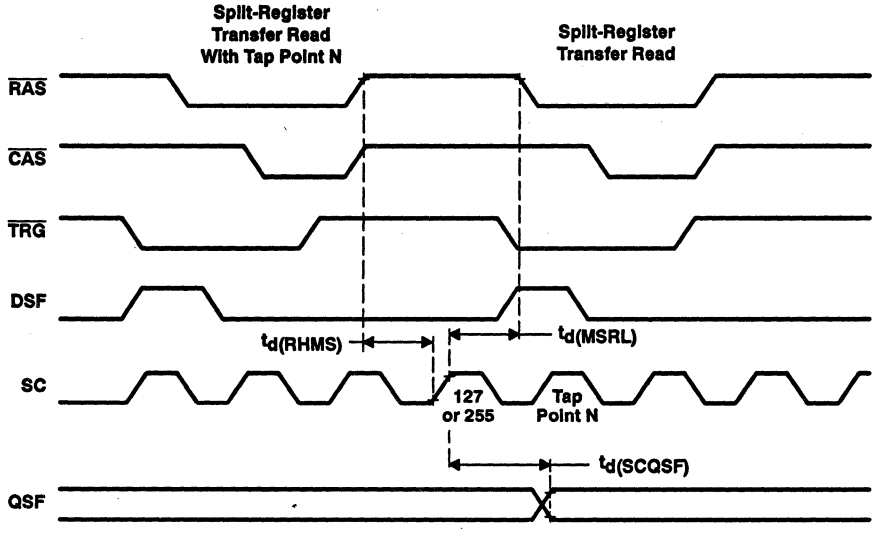


Figure 19. Example of Successive Split-Register-Transfer Read Operations

serial-read operation

The serial-read operation can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during transfer operations. Serial data can be read from the SAM by clocking SC starting at the tap point loaded by the preceding transfer cycle, proceeding sequentially to the most significant bit (bit 255), and then wrapping around to the least significant bit (bit 0), as shown in Figure 20.

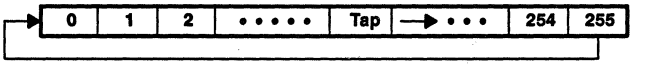


Figure 20. Serial Pointer Direction for Serial Read

For split-register operation, serial data can be read out from the active half of the SAM by clocking SC starting at the tap point loaded by the preceding split-register-transfer cycle. The serial pointer then proceeds sequentially to the most significant bit of the half, bit 127 or bit 255. If there is a split-register-transfer read to the inactive half during this period, the serial pointer points next to the tap point location loaded by that split-register-transfer (see Figure 21).

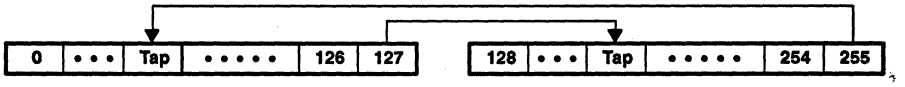


Figure 21. Serial Pointer for Split-Register Read – Case I

If there is no split-register-transfer read to the inactive half during this period, the serial pointer points next to the least significant bit of the inactive half (bit 128 or bit 0) (see Figure 22).

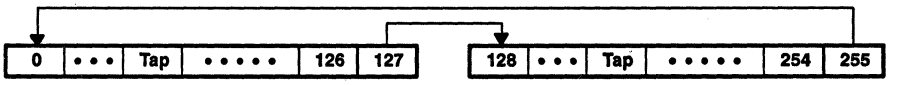


Figure 22. Serial Pointer for Split-Register Read – Case II

split-register programmable stop point

The TMS55166 offers programmable stop-point mode for split-register-transfer read operation. This mode can be used to improve 2-D drawing performance in a nonscanline data format.

In split-register-transfer read operation, the stop point is defined as a register location at which the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM. While in stop-point mode, the SAM is divided into partitions whose length is programmed via row addresses A4–A7 in a CBR set (CBRS) cycle. The last serial-address location of each partition is the stop point (see Figure 23).

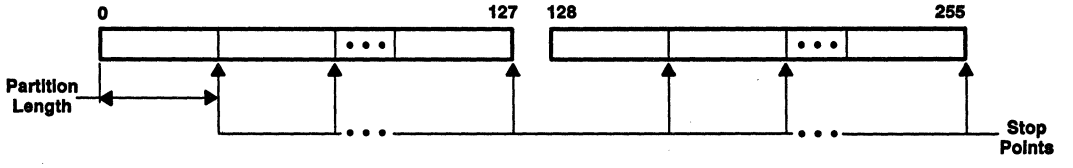


Figure 23. Example of the SAM With Partitions

split-register programmable stop point (continued)

Stop-point mode is not active until the CBRS cycle is initiated. The CBRS operation is performed by holding $\overline{CAS}$ and $\overline{WEx}$ low and DSF high on the falling edge of $\overline{RAS}$. The falling edge of $\overline{RAS}$ also latches row addresses A4–A7, which are used to define the SAM's partition length. The other row address inputs are don't care. Stop-point mode should be initiated after the initialization cycles have been performed (see Table 5).

Table 5. Programming Code for Stop-Point Mode

MAXIMUM PARTITION LENGTH	ADDRESS AT $\overline{RAS}$ IN CBRS CYCLE						NUMBER OF PARTITIONS	STOP-POINT LOCATIONS
	A8	A7	A6	A5	A4	A0–A3		
16	X	L	L	L	L	X	16	15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255
32	X	L	L	L	H	X	8	31, 63, 95, 127, 159, 191, 223, 255
64	X	L	L	H	H	X	4	63, 127, 191, 255
128 (default)	X	L	H	H	H	X	2	127, 255

In stop-point mode, the tap point loaded during the split-register-transfer read cycle determines in which SAM partition the serial output begins and at which stop point the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM (see Figure 24).

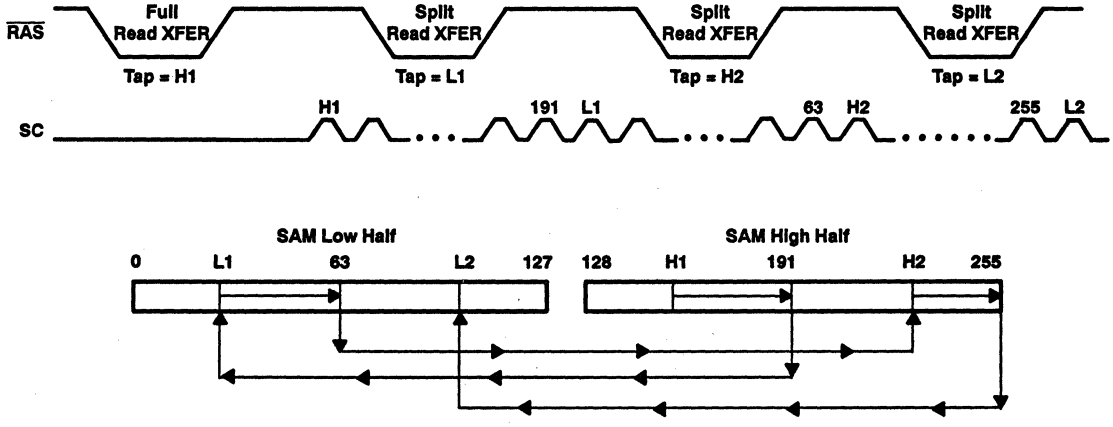


Figure 24. Example of Split-Register Operation With Programmable Stop Points

256-/512-bit compatibility of split-register programmable stop point

The stop-point mode is designed to be compatible both for 256-bit SAM and 512-bit SAM devices. After the CBRS cycle is initiated, the stop-point mode becomes active. In the stop-point mode, and only in the stop-point mode, the column-address bits AY7 and AY8 are internally swapped to assure the compatibility (see Figure 25). This address-bit swap applies to the column address, and it is effective for all DRAM and transfer cycles. For example, during the split-register-transfer cycle with stop point, column-address bit AY8 is a don't care and AY7 decodes the DRAM row half for the split-register-transfer. During stop-point mode, a CBR option reset (CBR) cycle is not recommended because this ends the stop-point mode and restores address bits AY7 and AY8 to their normal functions. Consistent use of CBR cycles ensures that the TMS55166 remains in nomal mode.

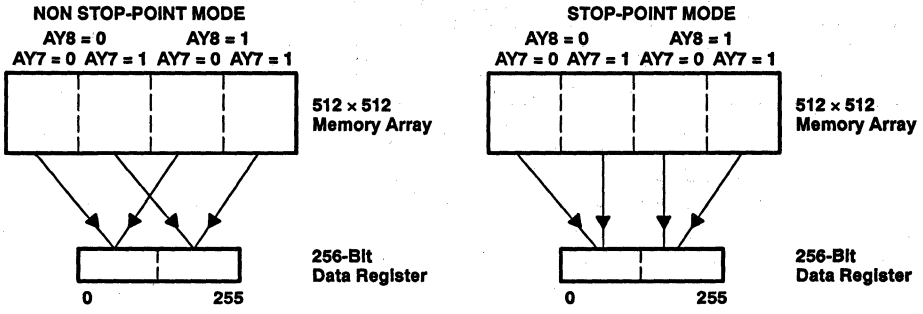


Figure 25. DRAM-to-SAM Mapping, Non Stop Point Versus Stop Point

IMPORTANT: For proper device operation in the split-register stop-point mode, a CBRS cycle should be initiated right after the power-up initialization cycles have been performed.

power up

To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight $\overline{RAS}$ cycles or eight CBR cycles to initialize the DRAM port. A full-register-transfer read cycle and two SC cycles are needed to initialize the SAM port.

After initialization, the internal state of the TMS55166 is as follows:

	STATE AFTER INITIALIZATION
QSF	Defined by the transfer cycle during initialization
Write mode	Nonpersistent mode
Write mask register	Undefined
Color register	Undefined
Serial-register tap point	Defined by the transfer cycle during initialization
SAM port	Output mode

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −1 V to 7 V
Voltage range on any pin ..... −1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1.1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SAM PORT	'55166-60		'55166-70		'55166-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −1 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 5.8 V, All other pins at 0 V to V_{CC}			±10		±10		±10	μA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC} See Note 3			±10		±10		±10	μA
I_{CC1}	Operating current‡	See Note 4	Standby		180		165		150	mA
I_{CC1A}	Operating current‡	$t_{c(SC)}$ = MIN	Active		225		205		185	mA
I_{CC2}	Standby current	All clocks = V_{CC}	Standby		5		5		5	mA
I_{CC2A}	Standby current	$t_{c(SC)}$ = MIN	Active		70		65		60	mA
I_{CC3}	$\overline{RAS}$-only refresh current	See Note 4	Standby		180		165		150	mA
I_{CC3A}	$\overline{RAS}$-only refresh current	$t_{c(SC)}$ = MIN, See Note 4	Active		225		205		185	mA
I_{CC4}	Page-mode current‡	$t_{c(P)}$ = MIN, See Note 5	Standby		140		140		120	mA
I_{CC4A}	Page-mode current‡	$t_{c(SC)}$ = MIN, See Note 5	Active		185		185		165	mA
I_{CC5}	CBR current	See Note 4	Standby		180		165		150	mA
I_{CC5A}	CBR current	$t_{c(SC)}$ = MIN, See Note 4	Active		225		205		185	mA
I_{CC6}	Data-transfer current	See Note 4	Standby		200		180		160	mA
I_{CC6A}	Data-transfer current	$t_{c(SC)}$ = MIN	Active		250		225		200	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open

NOTES: 3. $\overline{SE}$ is disabled for SQ output leakage tests.
4. Measured with one address change while $\overline{RAS}$ = V_{IL}, $t_{c(rd)}$, $t_{c(W)}$, $t_{c(TRD)}$ = MIN.
5. Measured with one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, address strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(DSF)}$	Input capacitance, special function		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
$C_{o(O)}$	Output capacitance, SQ and DQ		7	pF
$C_{o(QSF)}$	Output capacitance, QSF		9	pF

NOTE 6: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		TEST CONDITIONS†	ALT. SYMBOL	'55166-60		'55166-70		'55166-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		17		20		20	ns
$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{AA}		30		35		40	ns
$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = MAX	t_{CPA}		35		40		45	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MAX	t_{RAC}		60		70		80	ns
$t_{a(G)}$	Access time of DQ from $\overline{TRG}$ low		t_{OEA}		15		20		20	ns
$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 30 pF	t_{SCA}		15		20		25	ns
$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		12		15		20	ns
$t_{dis(CH)}$	Disable time, random output from $\overline{CAS}$ high (see Note 8)	C_L = 50 pF	t_{OFF}	0	15	0	20	0	20	ns
$t_{dis(RH)}$	Disable time, random output from $\overline{RAS}$ high (see Note 8)	C_L = 50 pF		0	15	0	20	0	20	ns
$t_{dis(G)}$	Disable time, random output from $\overline{TRG}$ high (see Note 8)	C_L = 50 pF	t_{OEZ}	0	15	0	20	0	20	ns
$t_{dis(WL)}$	Disable time, random output from $\overline{WE}$ low (see Note 8)	C_L = 30 pF	t_{WEZ}	0	15	0	20	0	20	ns
$t_{dis(SE)}$	Disable time, serial output from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	0	10	0	15	0	20	ns

† Measured with outputs open. For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

NOTES: 7. Switching times for RAM port output are measured with a load equivalent to 1 TTL load and 50 pF. Data out reference level: V_{OH}/V_{OL} = 2 V/0.8 V. Switching times for SAM port output are measured with a load equivalent to 1 TTL load and 30 pF. Serial data out reference level: V_{OH}/V_{OL} = 2 V/0.8 V.

8. $t_{dis(CH)}$, $t_{dis(RH)}$, $t_{dis(G)}$, $t_{dis(WL)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature†

		ALT. SYMBOL	'55166-60		'55166-70		'55166-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Cycle time, read	t_{RC}	110		130		150		ns
$t_{c(W)}$	Cycle time, write	t_{WC}	110		130		150		ns
$t_{c(rdW)}$	Cycle time, read-modify-write	t_{RMW}	150		175		200		ns
$t_{c(P)}$	Cycle time, page-mode read, write	t_{PC}	30		30		35		ns
$t_{c(RDWP)}$	Cycle time, page-mode read-modify-write	t_{PRMW}	80		90		100		ns
$t_{c(TRD)}$	Cycle time, transfer read	t_{RC}	110		130		150		ns
$t_{c(SC)}$	Cycle time, serial clock (see Note 9)	t_{SCC}	18		22		30		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CPN}	10		10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 10)	t_{CAS}	10	10 000	10	10 000	20	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	40		50		60		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 11)	t_{RAS}	60	10 000	70	10 000	80	10 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{WEx}$ low	t_{WP}	10		10		15		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		15		20		20		ns
$t_{w(SCH)}$	Pulse duration, SC high (see Note 9)	t_{SC}	5		8		10		ns
$t_{w(SCL)}$	Pulse duration, SC low (see Note 9)	t_{SCP}	5		8		10		ns
$t_{w(GH)}$	Pulse duration, $\overline{TRG}$ high	t_{TP}	20		20		20		ns
$t_{w(RL)P}$	Pulse duration, $\overline{RAS}$ low (page mode)	t_{RASP}	60	100 000	70	100 000	80	100 000	ns
$t_{su(CA)}$	Setup time, column address before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{su(SFC)}$	Setup time, DSF before $\overline{CAS}$ low	t_{FSC}	0		0		0		ns
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(WMR)}$	Setup time, $\overline{WEx}$ before $\overline{RAS}$ low	t_{WSR}	0		0		0		ns
$t_{su(DQR)}$	Setup time, DQ before $\overline{RAS}$ low	t_{MS}	0		0		0		ns
$t_{su(TRG)}$	Setup time, $\overline{TRG}$ high before $\overline{RAS}$ low	t_{THS}	0		0		0		ns
$t_{su(SFR)}$	Setup time, DSF low before $\overline{RAS}$ low	t_{FSR}	0		0		0		ns
$t_{su(DCL)}$	Setup time, data valid before $\overline{CAS}$ low	t_{DSC}	0		0		0		ns
$t_{su(DWL)}$	Setup time, data valid before $\overline{WEx}$ low	t_{DSW}	0		0		0		ns
$t_{su(rd)}$	Setup time, read command, $\overline{WEx}$ high before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	Setup time, early write command, $\overline{WEx}$ low before $\overline{CAS}$ low	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	Setup time, $\overline{WEx}$ low before $\overline{CAS}$ high, write	t_{CWL}	15		15		20		ns
$t_{su(WRH)}$	Setup time, $\overline{WEx}$ low before $\overline{RAS}$ high, write	t_{RWL}	15		15		20		ns
$t_{h(CLCA)}$	Hold time, column address after $\overline{CAS}$ low	t_{CAH}	10		10		15		ns
$t_{h(SFC)}$	Hold time, DSF after $\overline{CAS}$ low	t_{CFH}	10		10		15		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. Cycle time assumes t_t = 3 ns.

10. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].

11. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

			ALT. SYMBOL	'55166-60		'55166-70		'55166-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low		t_{RAH}	10		10		10		ns
$t_{h(TRG)}$	Hold time, $\overline{TRG}$ after $\overline{RAS}$ low		t_{THH}	10		10		10		ns
$t_{h(RWM)}$	Hold time, write mask after $\overline{RAS}$ low		t_{RWH}	10		10		10		ns
$t_{h(RDQ)}$	Hold time, DQ after $\overline{RAS}$ low (write-mask operation)		t_{MH}	10		10		10		ns
$t_{h(SFR)}$	Hold time, DSF after $\overline{RAS}$ low		t_{RFH}	10		10		10		ns
$t_{h(RLCA)}$	Hold time, column address valid after $\overline{RAS}$ low (see Note 12)		t_{AR}	30		30		35		ns
$t_{h(CLD)}$	Hold time, data valid after $\overline{CAS}$ low		t_{DH}	15		15		15		ns
$t_{h(RLD)}$	Hold time, data valid after $\overline{RAS}$ low (see Note 12)		t_{DHR}	35		35		35		ns
$t_{h(WLD)}$	Hold time, data valid after $\overline{WEx}$ low		t_{DH}	15		15		15		ns
$t_{h(CHrd)}$	Hold time, read, $\overline{WEx}$ high after $\overline{CAS}$ high (see Note 13)		t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Hold time, read, $\overline{WEx}$ high after $\overline{RAS}$ high (see Note 13)		t_{RRH}	0		0		0		ns
$t_{h(CLW)}$	Hold time, write, $\overline{WEx}$ low after $\overline{CAS}$ low		t_{WCH}	10		15		15		ns
$t_{h(RLW)}$	Hold time, write, $\overline{WEx}$ low after $\overline{RAS}$ low (see Note 12)		t_{WCR}	30		35		35		ns
$t_{h(WLG)}$	Hold time, $\overline{TRG}$ high after $\overline{WEx}$ low (see Note 14)		t_{OEH}	10		10		10		ns
$t_{h(SHSQ)}$	Hold time, SQ after SC high		t_{SOH}	4		5		5		ns
$t_{h(RSF)}$	Hold time, DSF after $\overline{RAS}$ low		t_{FHR}	30		30		35		ns
$t_{h(CLQ)}$	Hold time, output valid after $\overline{CAS}$ low		t_{DHC}	4		5		5		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		t_{CSH}	53		60		80		ns
		See Note 15	t_{CHR}	10		10		15		
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		t_{RSH}	17		20		20		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{WEx}$ low (see Notes 16 and 17)		t_{CWD}	37		45		45		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 18)		t_{RCD}	20	43	20	50	20	60	ns
$t_{d(CARH)}$	Delay time, column address valid to $\overline{RAS}$ high		t_{RAL}	30		35		40		ns
$t_{d(CACH)}$	Delay time, column address valid to $\overline{CAS}$ high		t_{CAL}	30		35		40		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{WEx}$ low (see Note 16)		t_{RWD}	80		95		105		ns
$t_{d(CAWL)}$	Delay time, column address valid to $\overline{WEx}$ low (see Note 16)		t_{AWD}	50		60		65		ns
$t_{d(CLRL)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 15)		t_{CSR}	0		0		0		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 15)		t_{RPC}	0		0		0		ns
$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high for DRAM read cycles			17		20		20		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ		t_{OED}	10		15		15		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
14. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
15. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only
16. Read-modify-write operation only
17. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
18. The maximum value is specified only to assure $\overline{RAS}$ access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	'55166-60		'55166-70		'55166-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (see Note 19)	t_{RTH}	50		55		60		ns
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 19)	t_{RSD}	65		70		80		ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address valid	t_{RAD}	15	30	15	35	15	40	ns
$t_{d(GLRH)}$	Delay time, $\overline{TRG}$ low to $\overline{RAS}$ high	t_{ROH}	10		15		15		ns
$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 20)	t_{CSD}	20		20		25		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 19 and 20)	t_{TSL}	5		5		5		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 19)	t_{TRD}	−10		−10		−10		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 21)	t_{TRP}	40		50		60		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 19)	t_{TSD}	10		10		15		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split-register-transfer read cycles		15		20		20		ns
$t_{d(CLTH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high in real-time transfer read cycles	t_{CTH}	15		15		15		ns
$t_{d(CASH)}$	Delay time, column address to first SC in early-load transfer read cycles	t_{ASD}	25		25		30		ns
$t_{d(CAGH)}$	Delay time, column address to $\overline{TRG}$ high in real-time transfer read cycles	t_{ATH}	20		20		20		ns
$t_{d(DCL)}$	Delay time, data to $\overline{CAS}$ low	t_{DZC}	0		0		0		ns
$t_{d(DGL)}$	Delay time, data to $\overline{TRG}$ low	t_{DZO}	0		0		0		ns
$t_{d(MSRL)}$	Delay time, last (most significant) rising edge of SC to $\overline{RAS}$ low before boundary switch during split-transfer read cycles		15		20		20		ns
$t_{d(SCQSF)}$	Delay time, last (127 or 255) rising edge of SC to QSF switching at the boundary during split-register-transfer read cycles (see Note 2222)	t_{SQD}		20		25		30	ns
$t_{d(CLQSF)}$	Delay time, $\overline{CAS}$ low to QSF switching in transfer read cycles (see Note 2222)	t_{CQD}		25		30		35	ns
$t_{d(GHQSF)}$	Delay time, $\overline{TRG}$ high to QSF switching in transfer read cycles (see Note 2222)	t_{TQD}		20		25		30	ns
$t_{d(RLQSF)}$	Delay time, $\overline{RAS}$ low to QSF switching in transfer read cycles (see Note 2222)	t_{RQD}		65		70		75	ns
$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 19. Real-time load transfer read or late-load transfer read cycle only
20. Early-load transfer read cycle only
21. Full-register (read) transfer cycles only
22. Switching times for QSF output are measured with a load equivalent to 1 TTL load and 30 pF and output reference level is V_{OH} / V_{OL} = 2 V/0.8 V.

PARAMETER MEASUREMENT INFORMATION

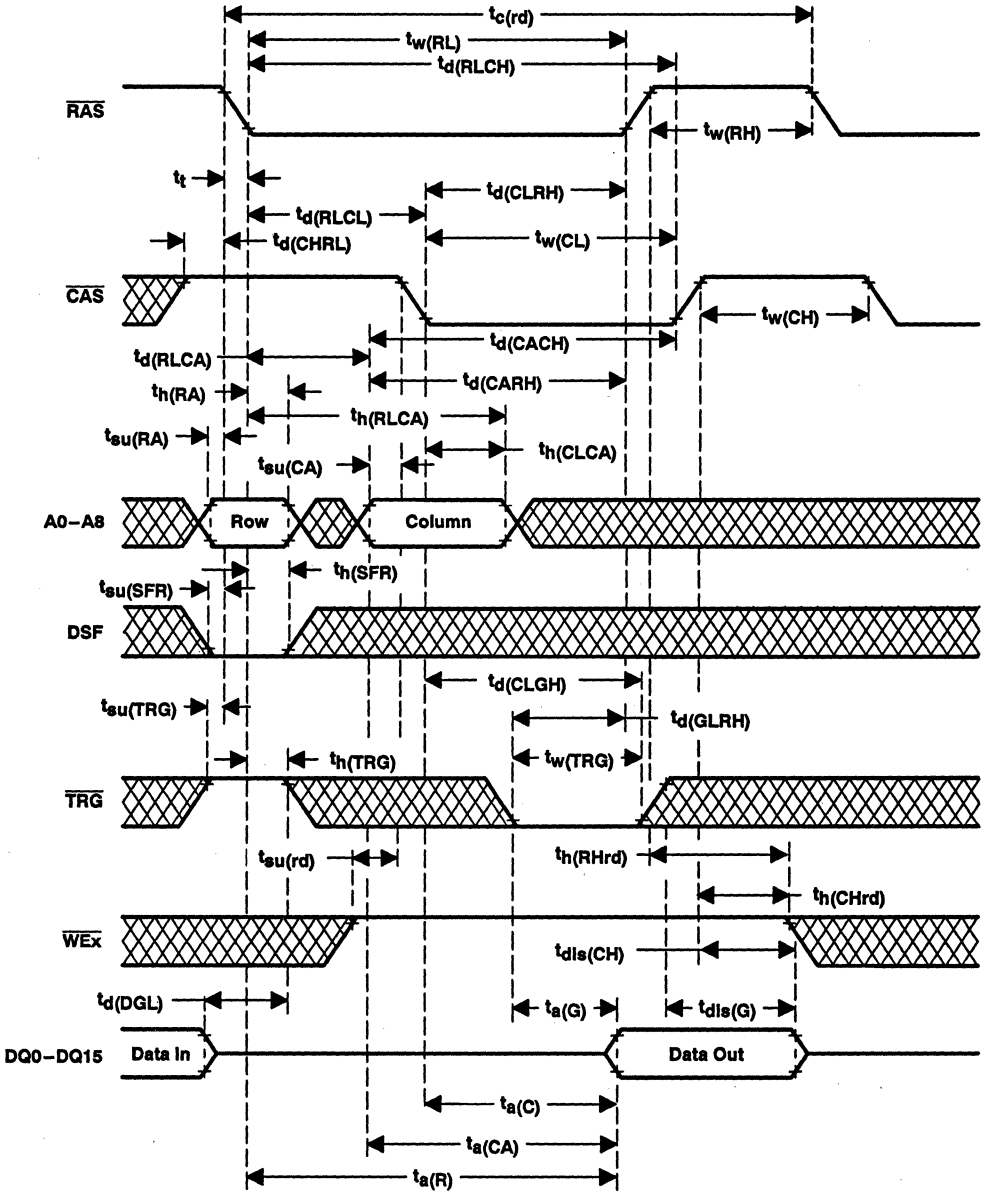


Figure 26. Read-Cycle Timing With $\overline{CAS}$-Controlled Output

PARAMETER MEASUREMENT INFORMATION

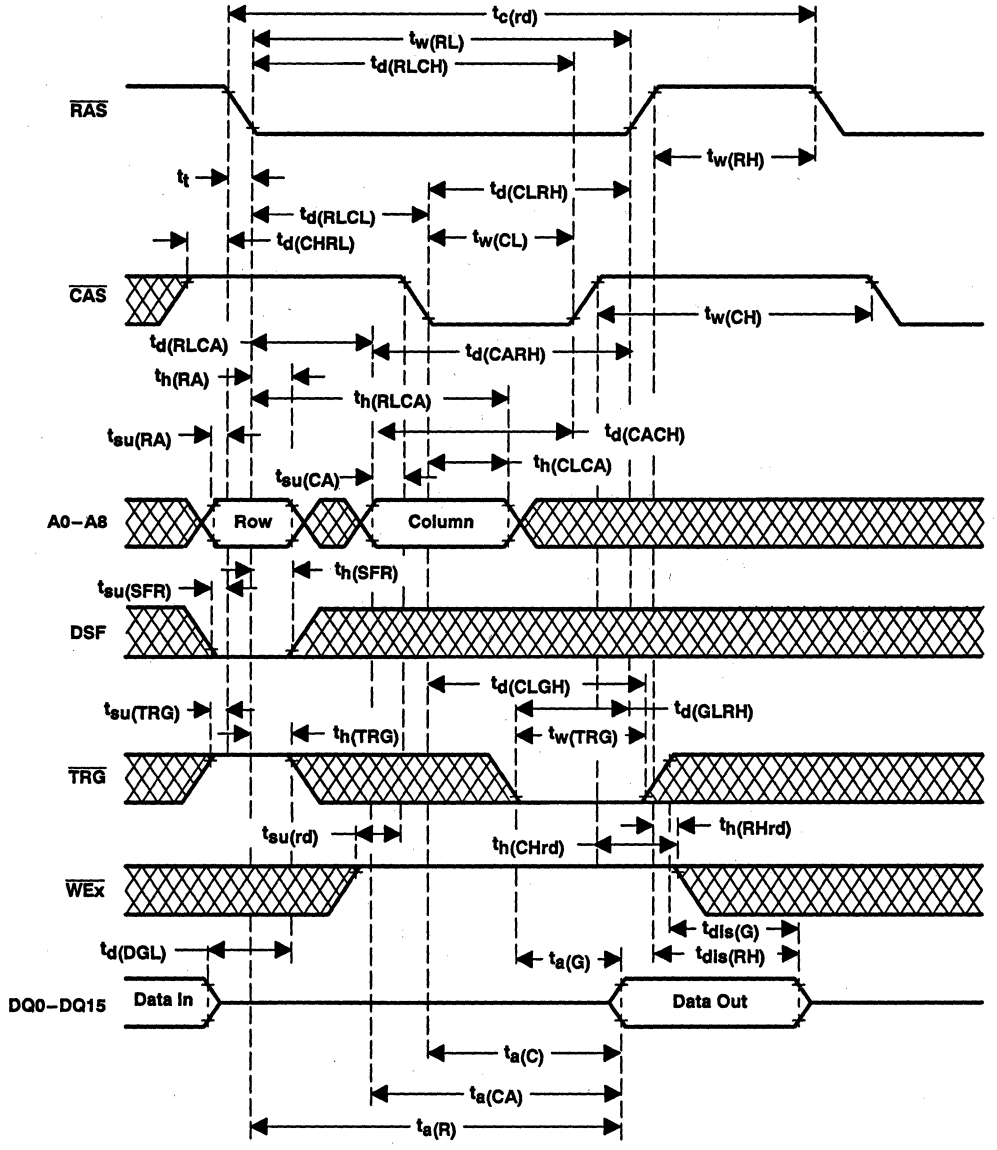


Figure 27. Read-Cycle Timing With $\overline{RAS}$-Controlled Output

PARAMETER MEASUREMENT INFORMATION

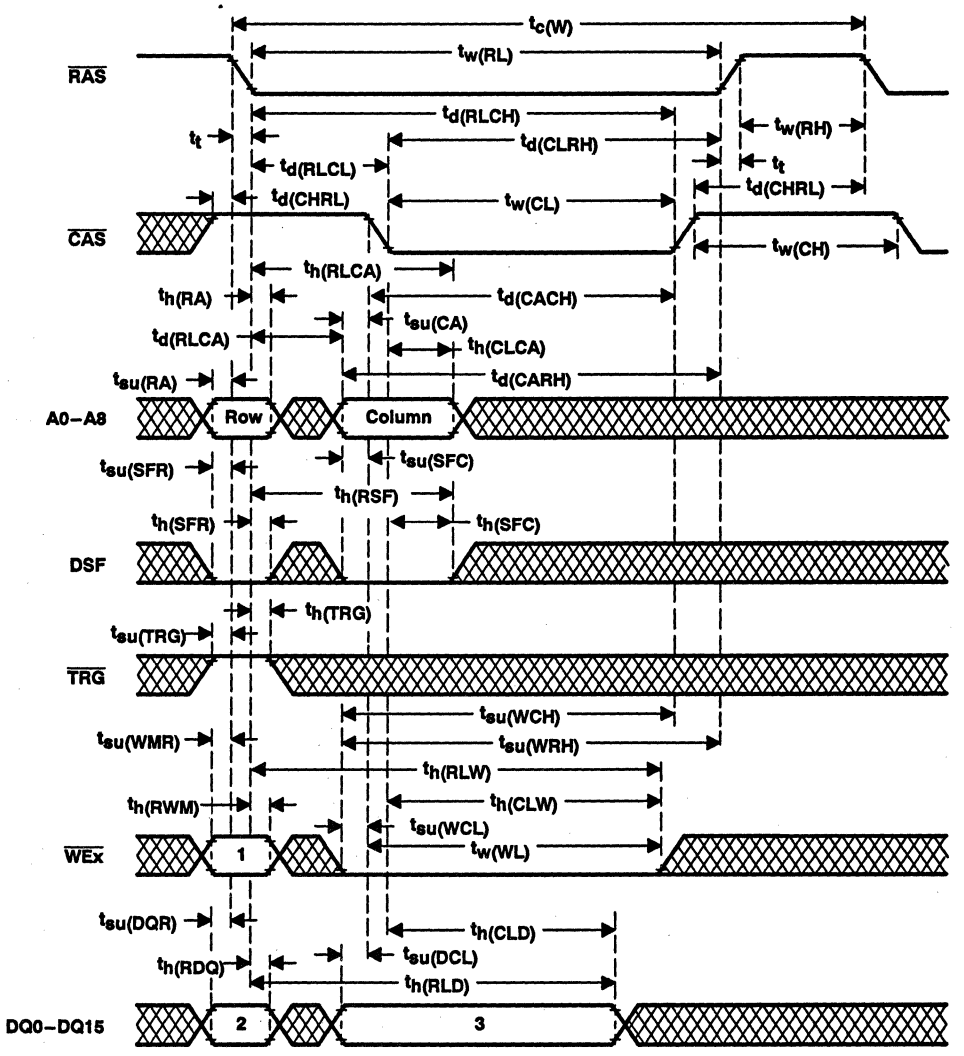


Figure 28. Early-Write-Cycle Timing

Table 6. Early-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

PARAMETER MEASUREMENT INFORMATION

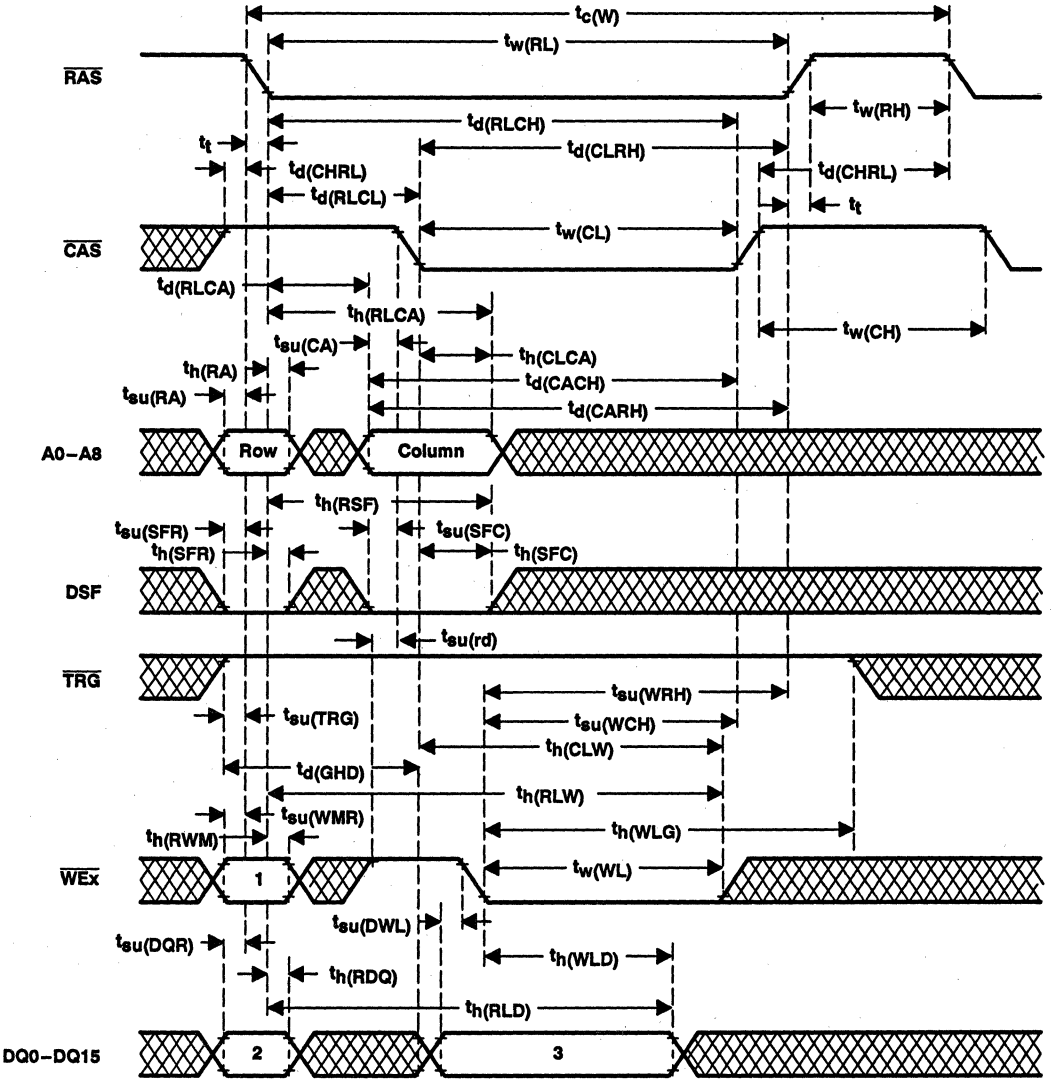
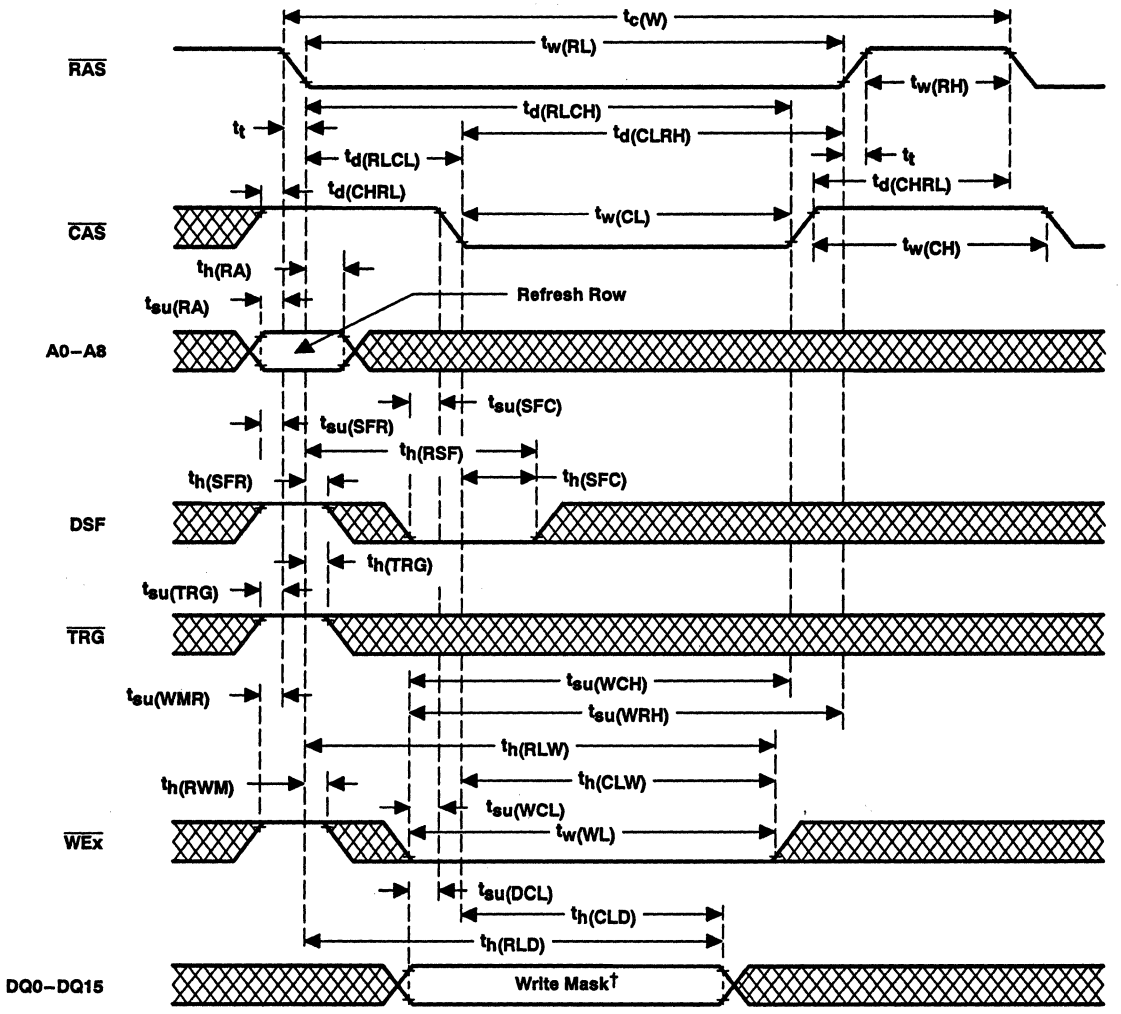


Figure 29. Late-Write-Cycle Timing (Output-Enable-Controlled Write)

Table 7. Late-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

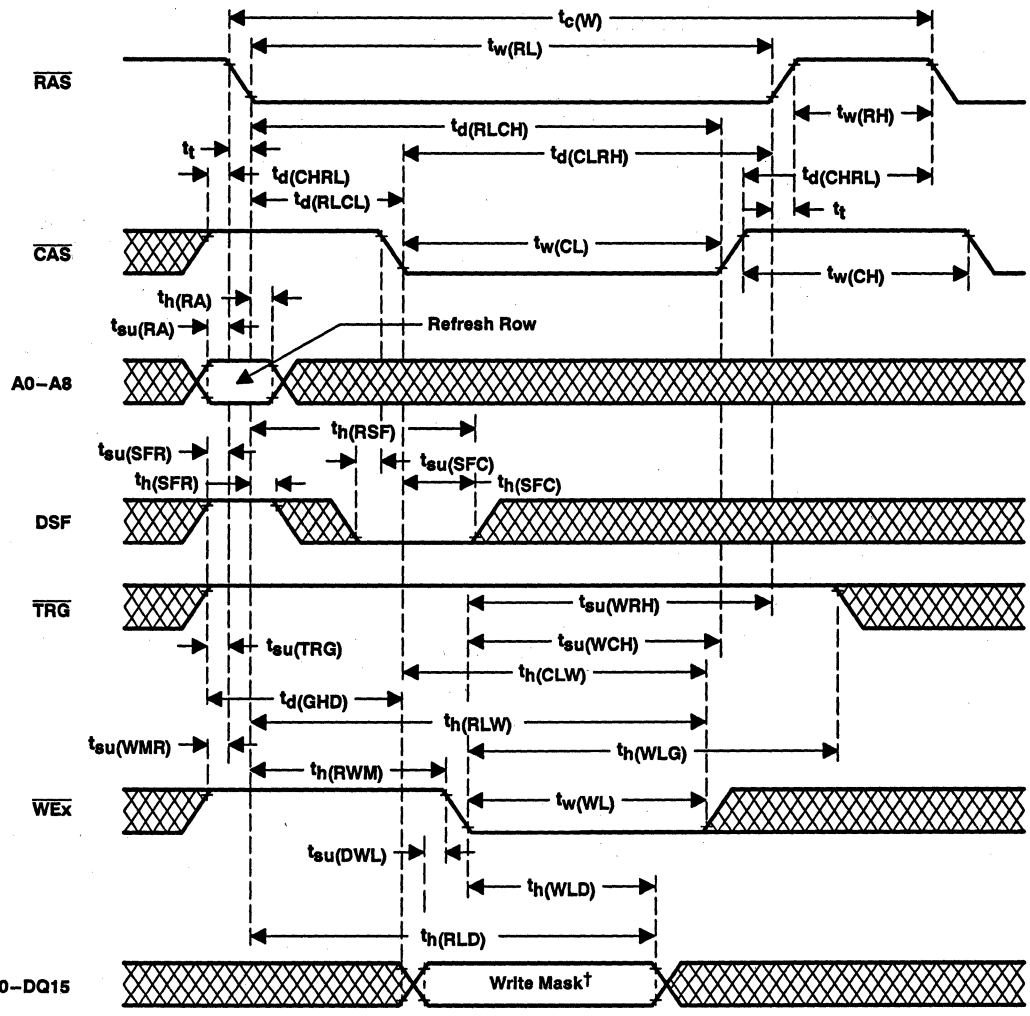
PARAMETER MEASUREMENT INFORMATION



† Load-write-mask-register cycle will put the device into the persistent write-per-bit mode.

Figure 30. Load-Write-Mask-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION



† Load-write-mask-register cycle will put the device into the persistent write-per-bit mode.

Figure 31. Load-Write-Mask-Register-Cycle Timing (Late-Write Load)

PARAMETER MEASUREMENT INFORMATION

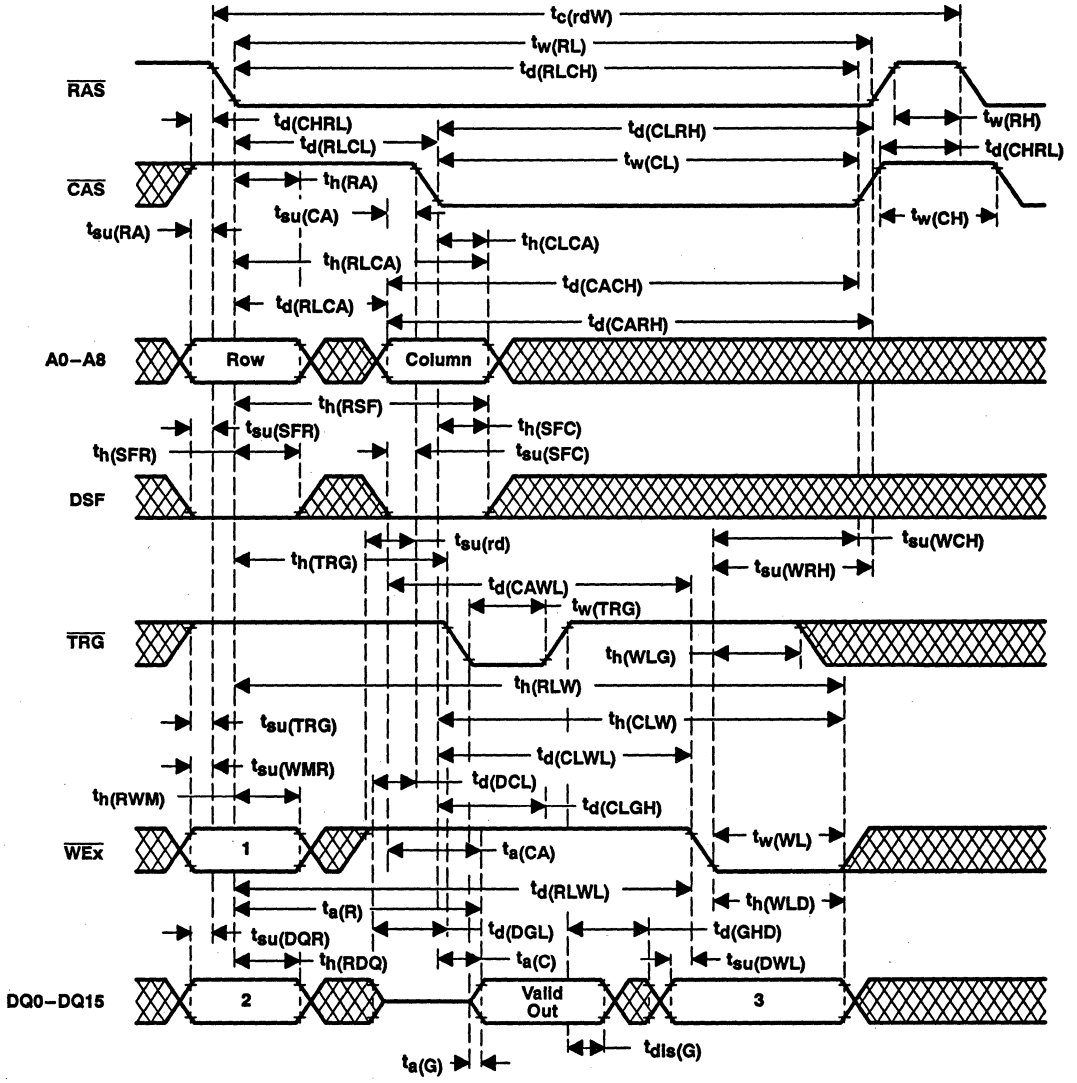
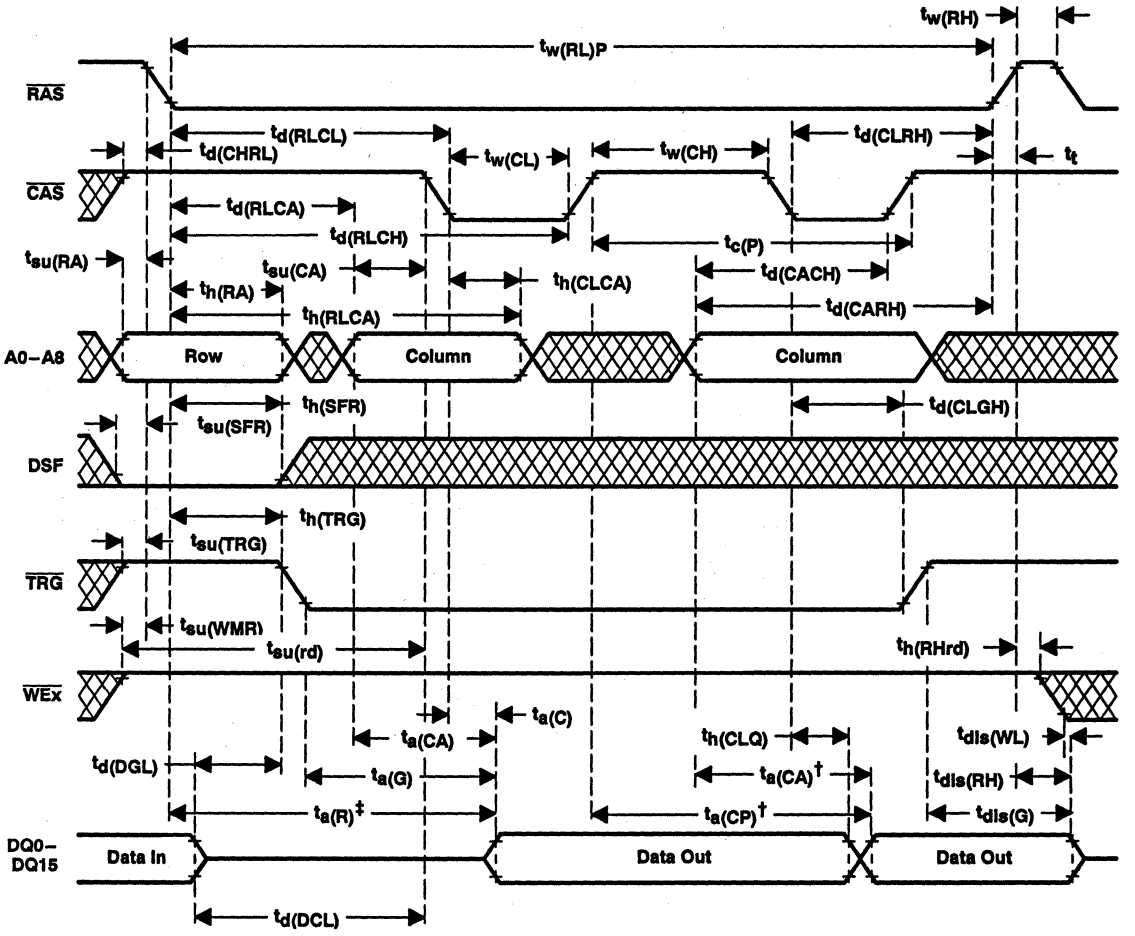


Figure 32. Read-Write/Read-Modify-Write-Cycle Timing

Table 8. Read-Write/Read-Modify-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

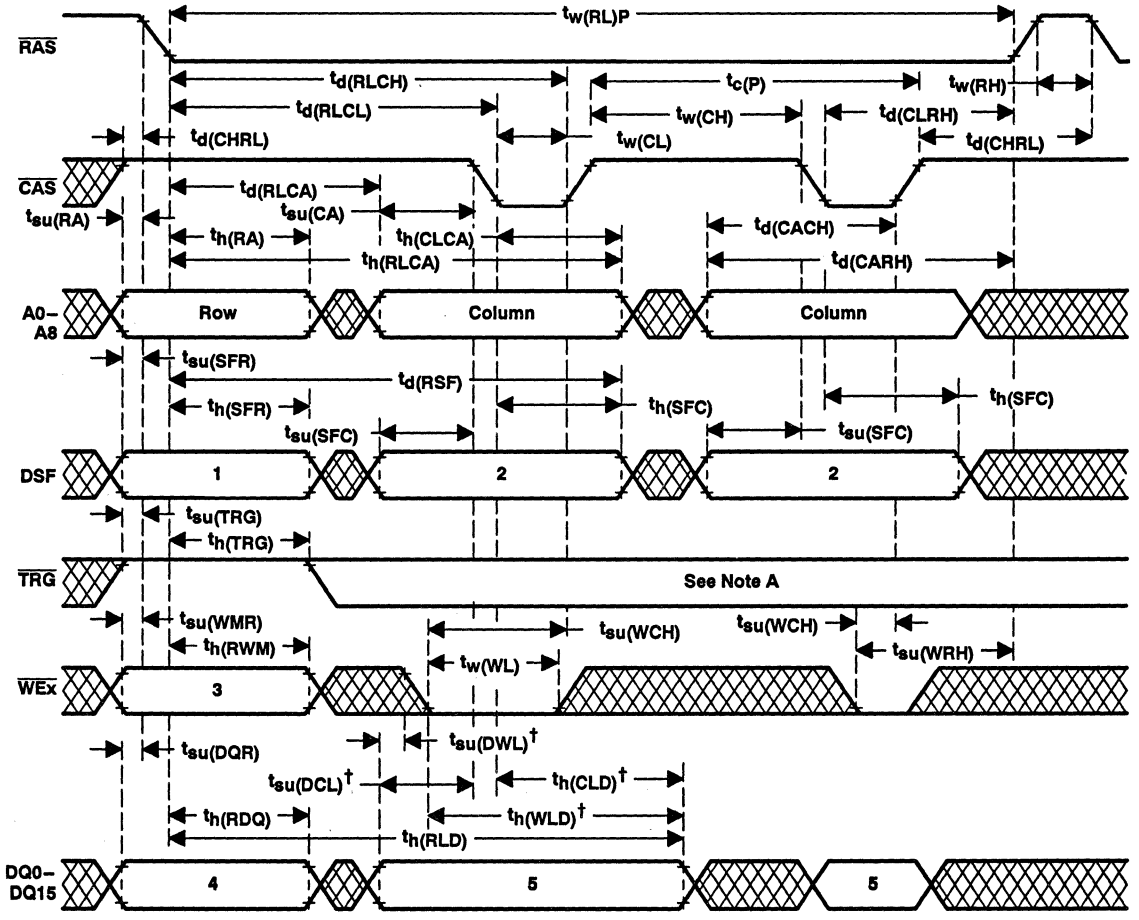
PARAMETER MEASUREMENT INFORMATION



† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output can go from the high-impedance state to an invalid data state prior to the specified access time.
NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.).

Figure 33. Enhanced-Page-Mode Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later

NOTE A: A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used. If the early-write-cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

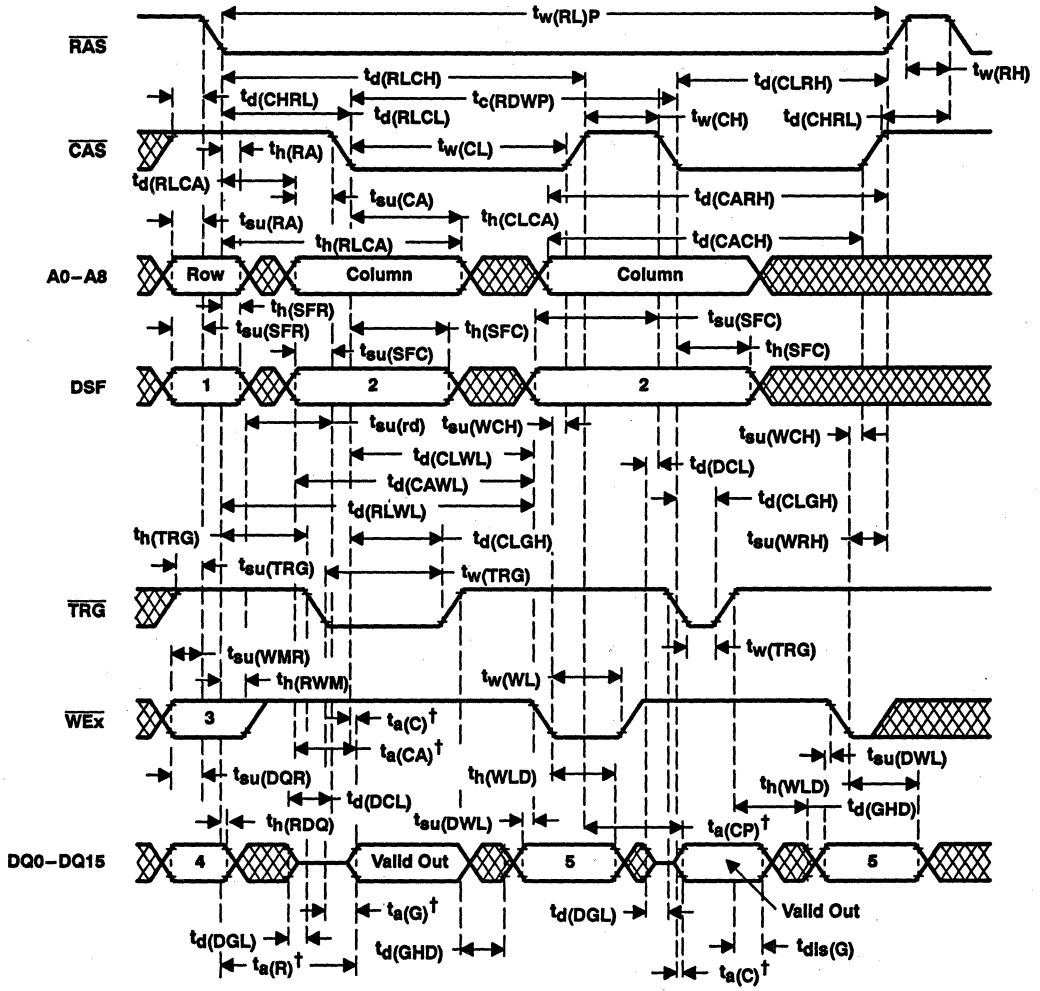
Figure 34. Enhanced-Page-Mode Write-Cycle Timing

Table 9. Enhanced-Page-Mode Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load-write-mask register on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load-write-mask-register cycle will set the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CAS}$ is a don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



† Output can go from the high-impedance state to an invalid data state prior to the specified access time.

NOTE A: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

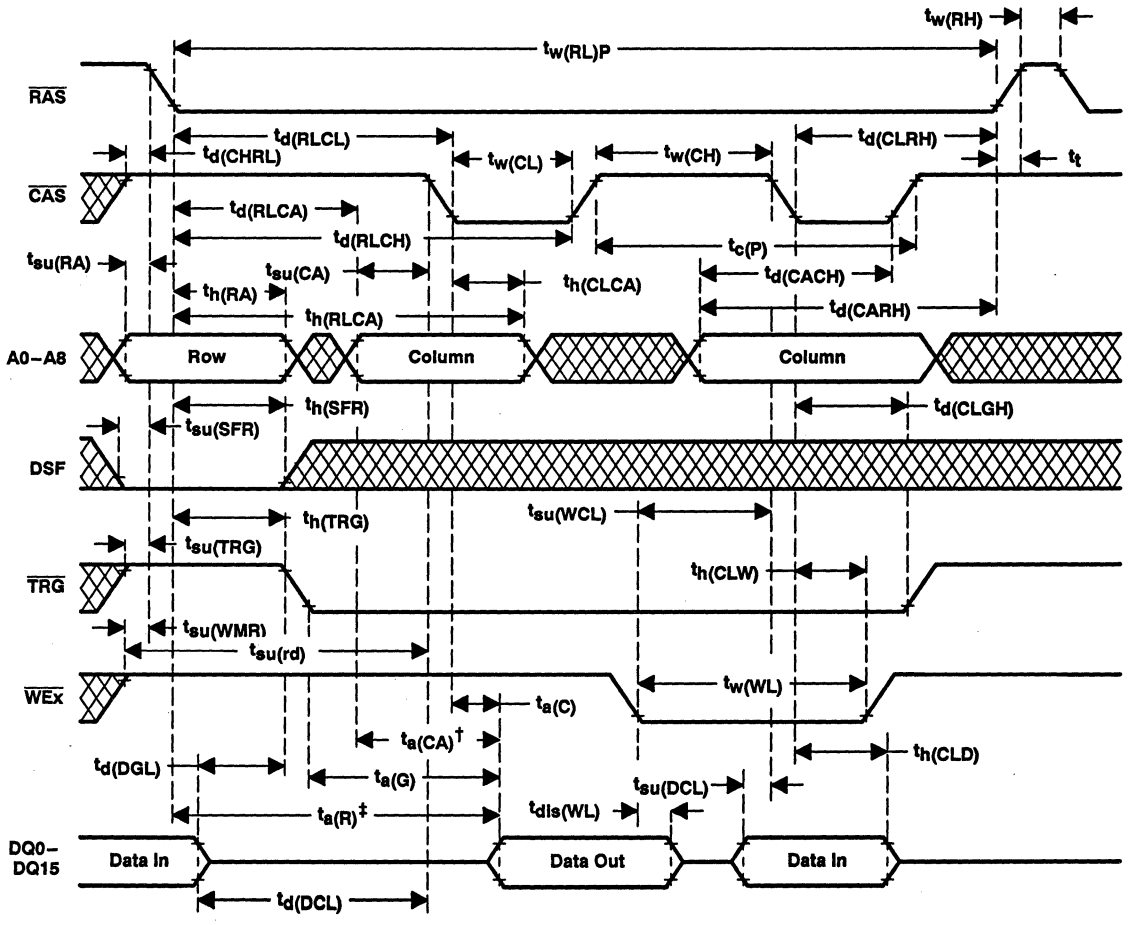
Figure 35. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

Table 10. Enhanced Page-Mode Read-Modify-Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load-write-mask register on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load-write-mask-register cycle will set the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CAS}$ is a don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



† Access time is $t_{a(CA)}$ dependent.
‡ Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 36. Enhanced-Page-Mode Read/Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

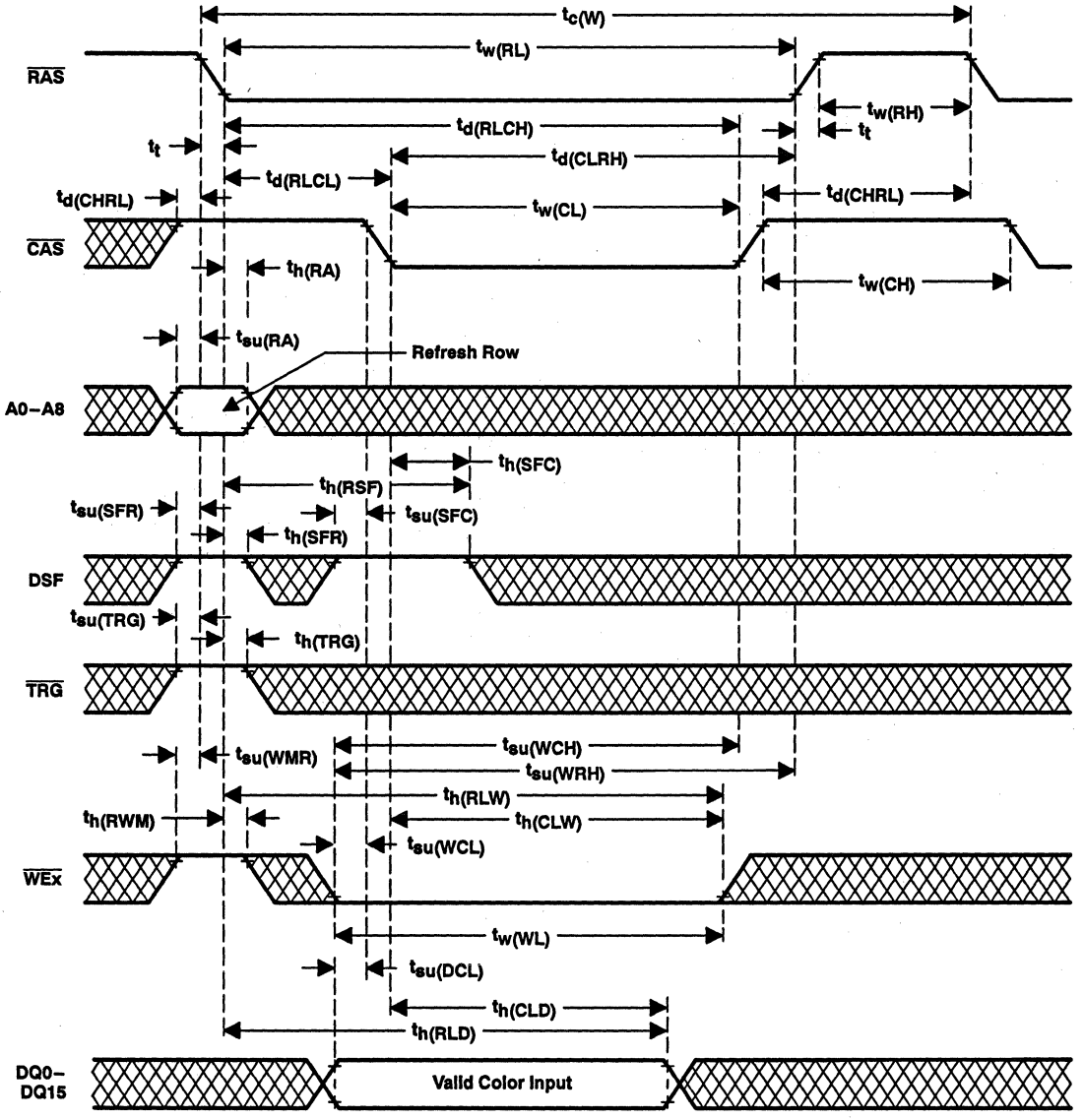


Figure 37. Load-Color-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION

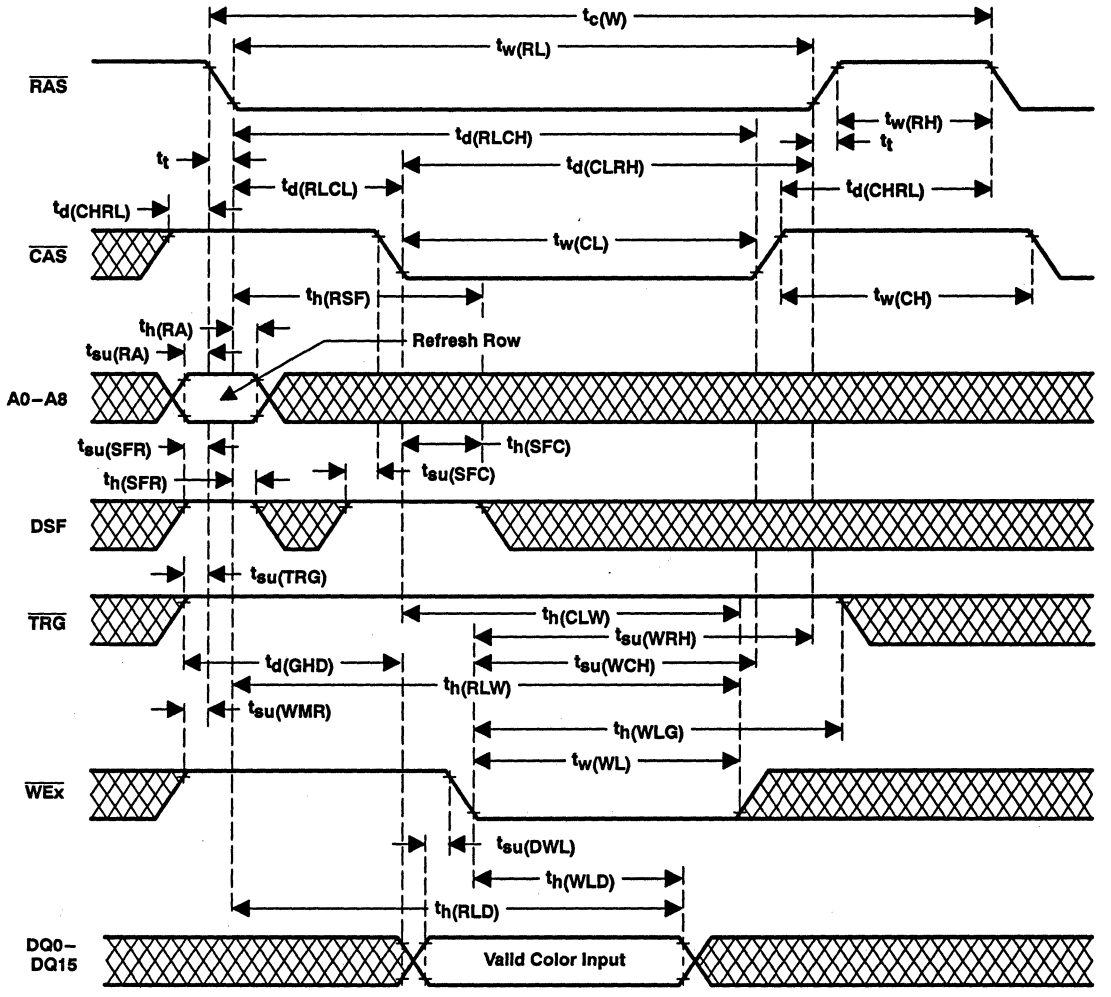


Figure 38. Load-Color-Register-Cycle Timing (Late-Write Load)

PARAMETER MEASUREMENT INFORMATION

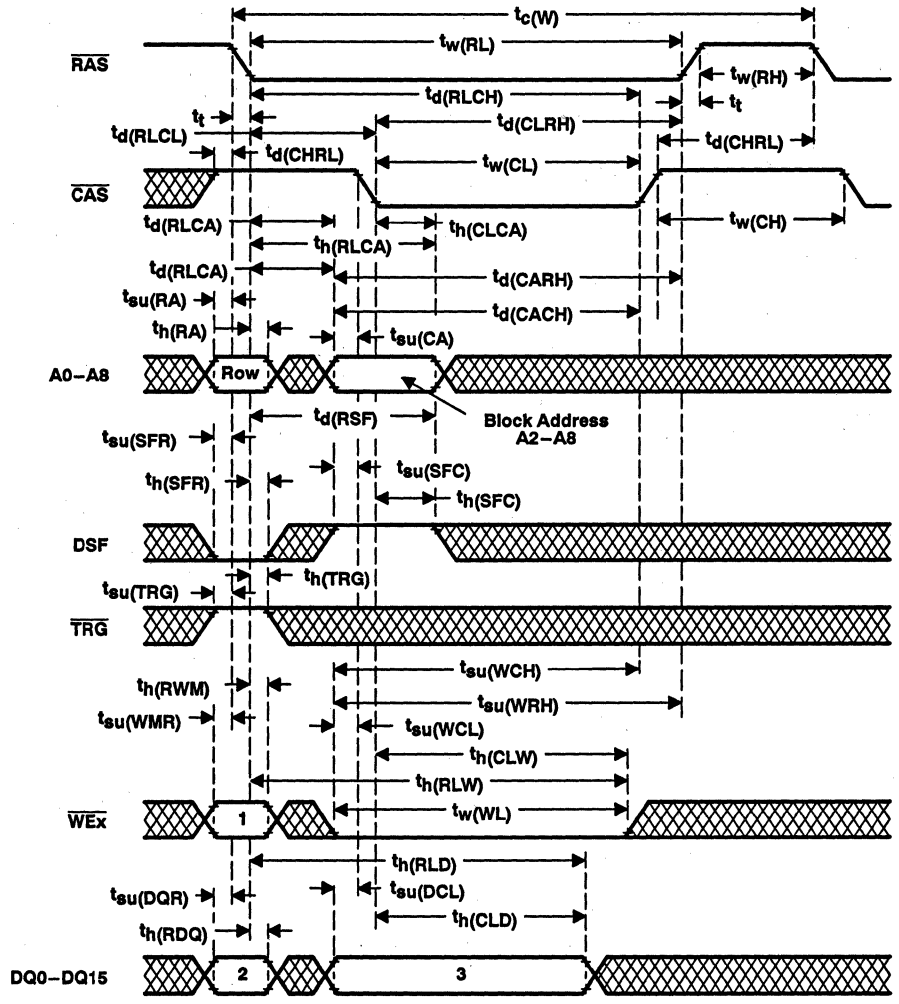


Figure 39. Block-Write-Cycle Timing (Early Write)

Table 11. Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi + 3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

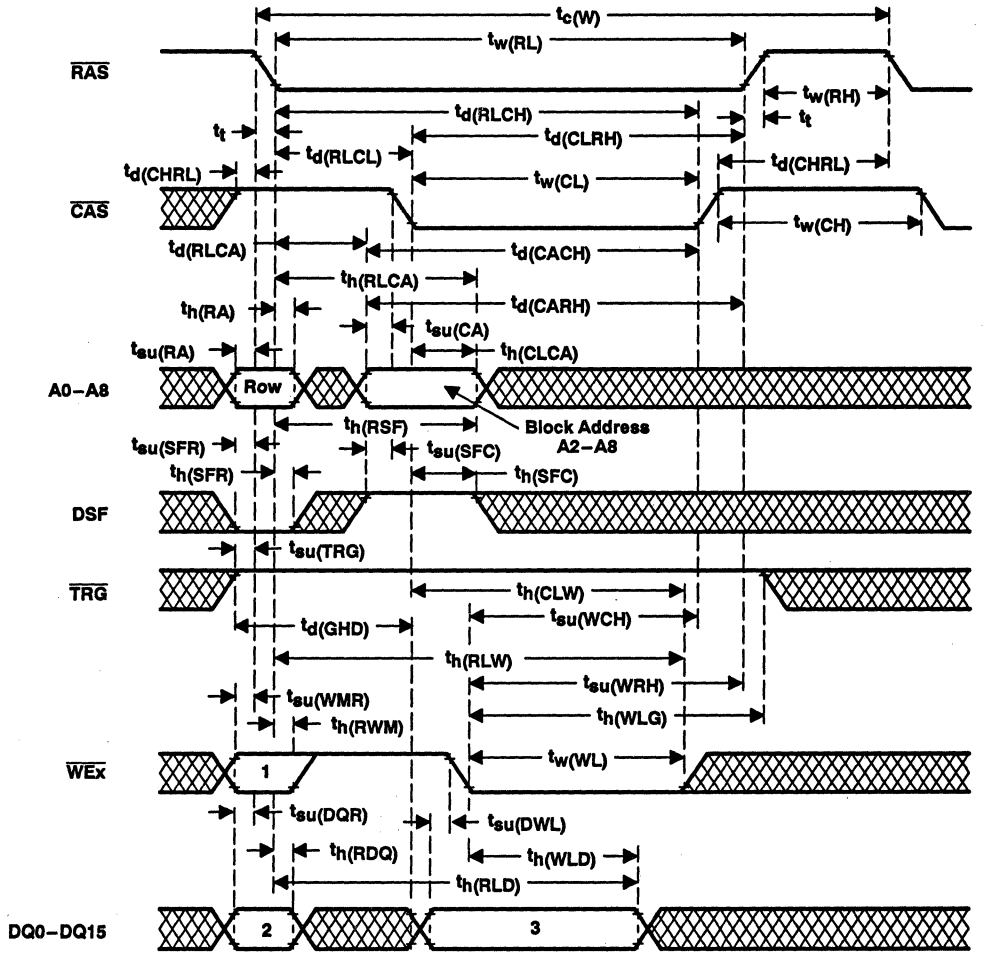


Figure 40. Block-Write-Cycle Timing (Late Write)

Table 12. Block-Write-Cycle State Table

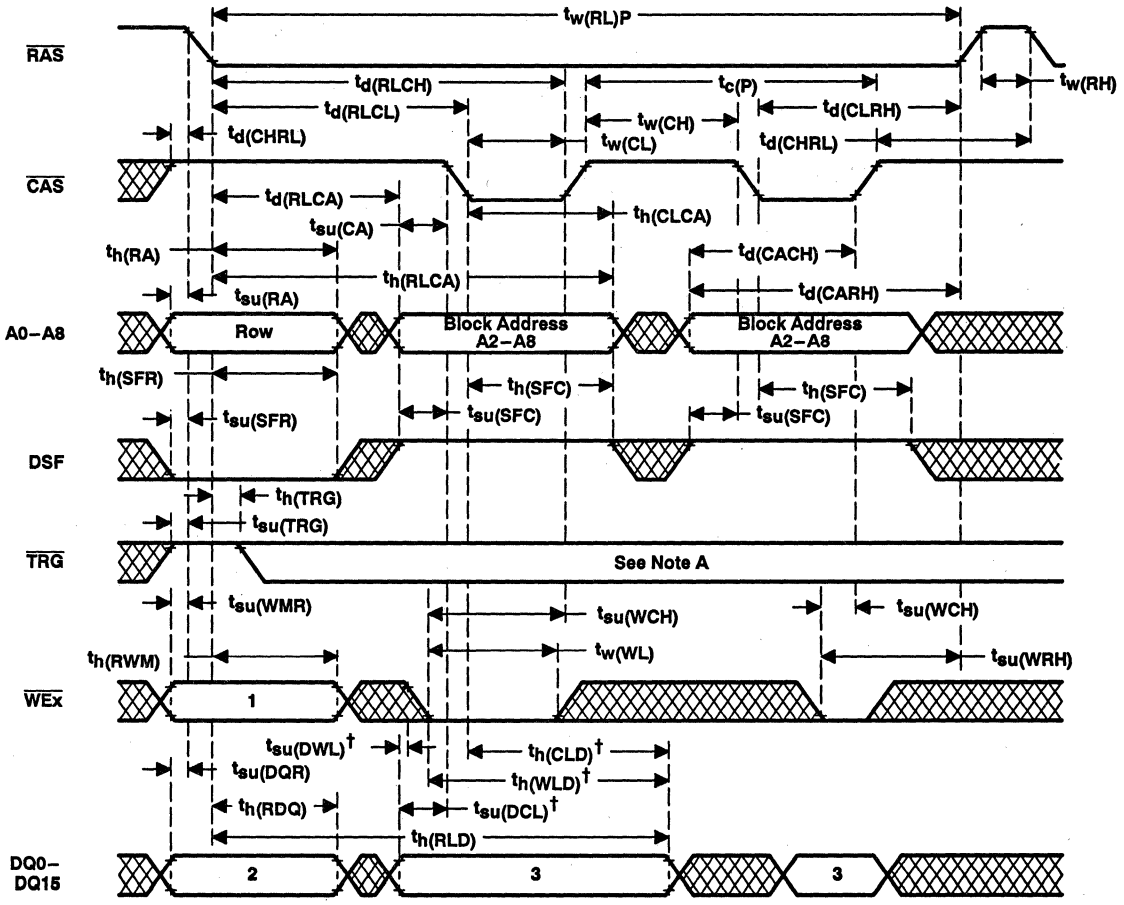
CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi + 3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later

NOTE A: To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used. If the early write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 41. Enhanced-Page-Mode Block-Write-Cycle Timing

Table 13. Enhanced-Page-Mode Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi + 3 (i = 0, 4, 8, 12)
0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

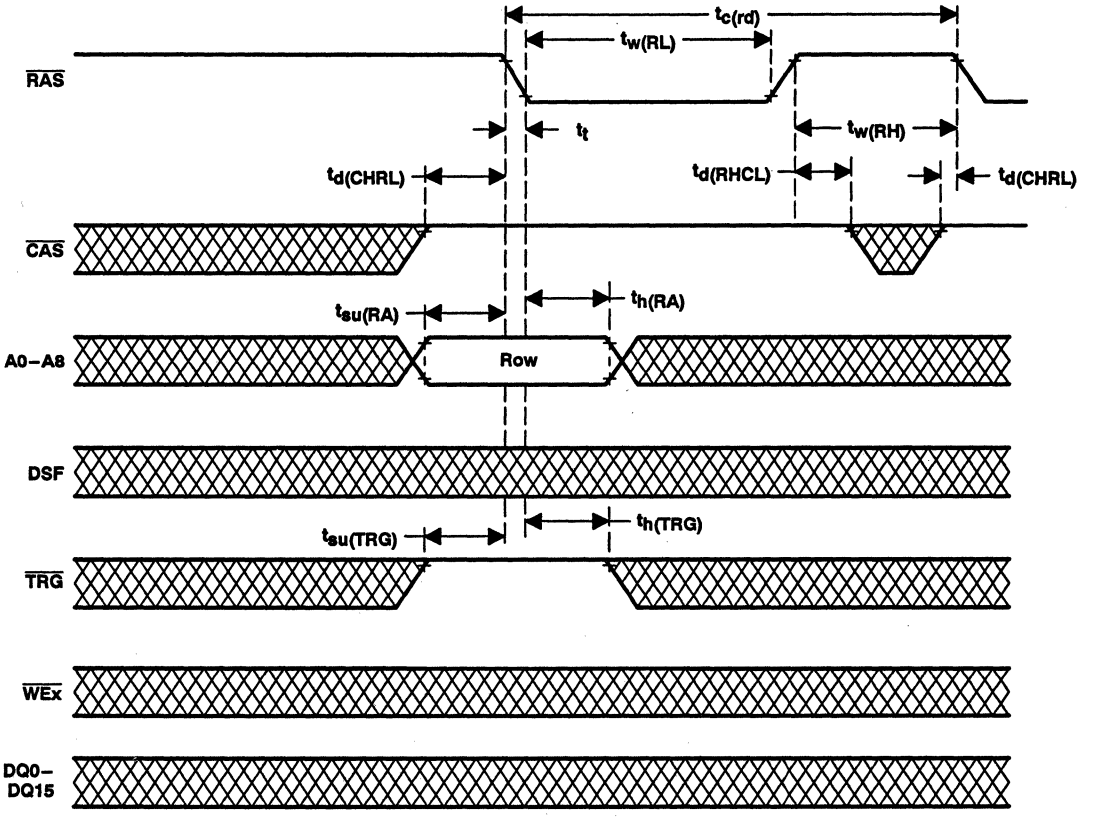


Figure 42. $\overline{RAS}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

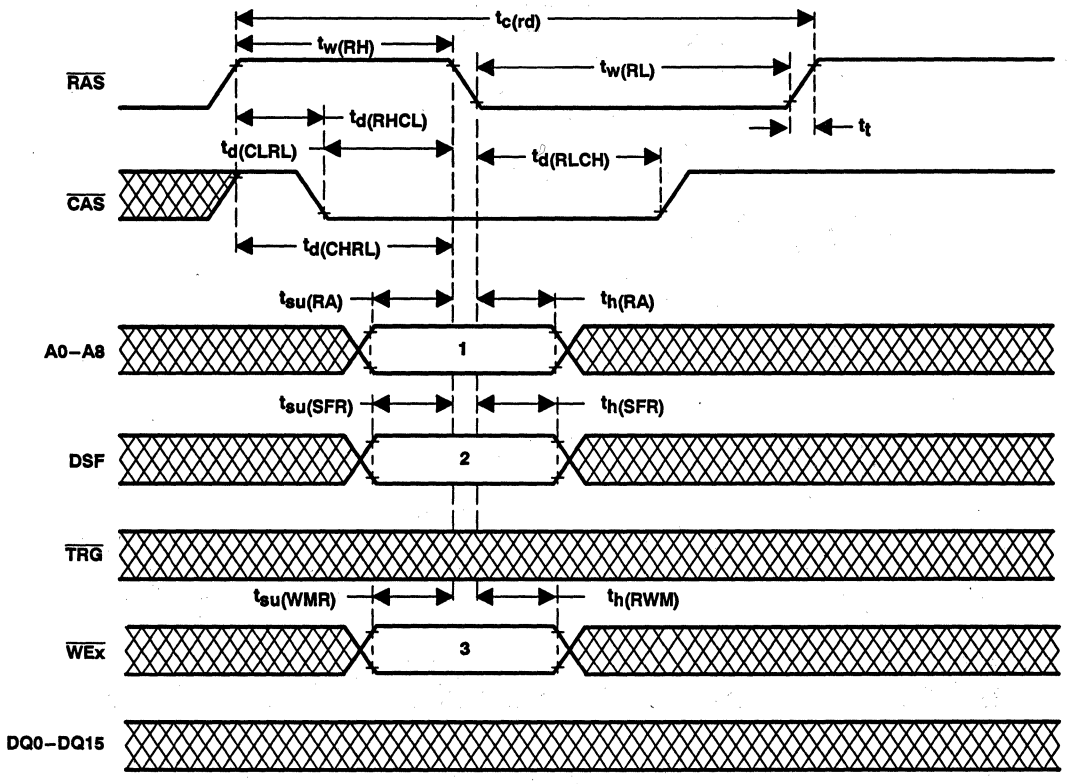


Figure 43. CBR-Refresh-Cycle Timing

Table 14. CBR-Cycle State Table

CYCLE	STATE		
	1	2	3
CBR refresh with option reset	Don't care	L	H
CBR refresh with no reset	Don't care	H	H
CBR refresh with stop point set and no reset	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION

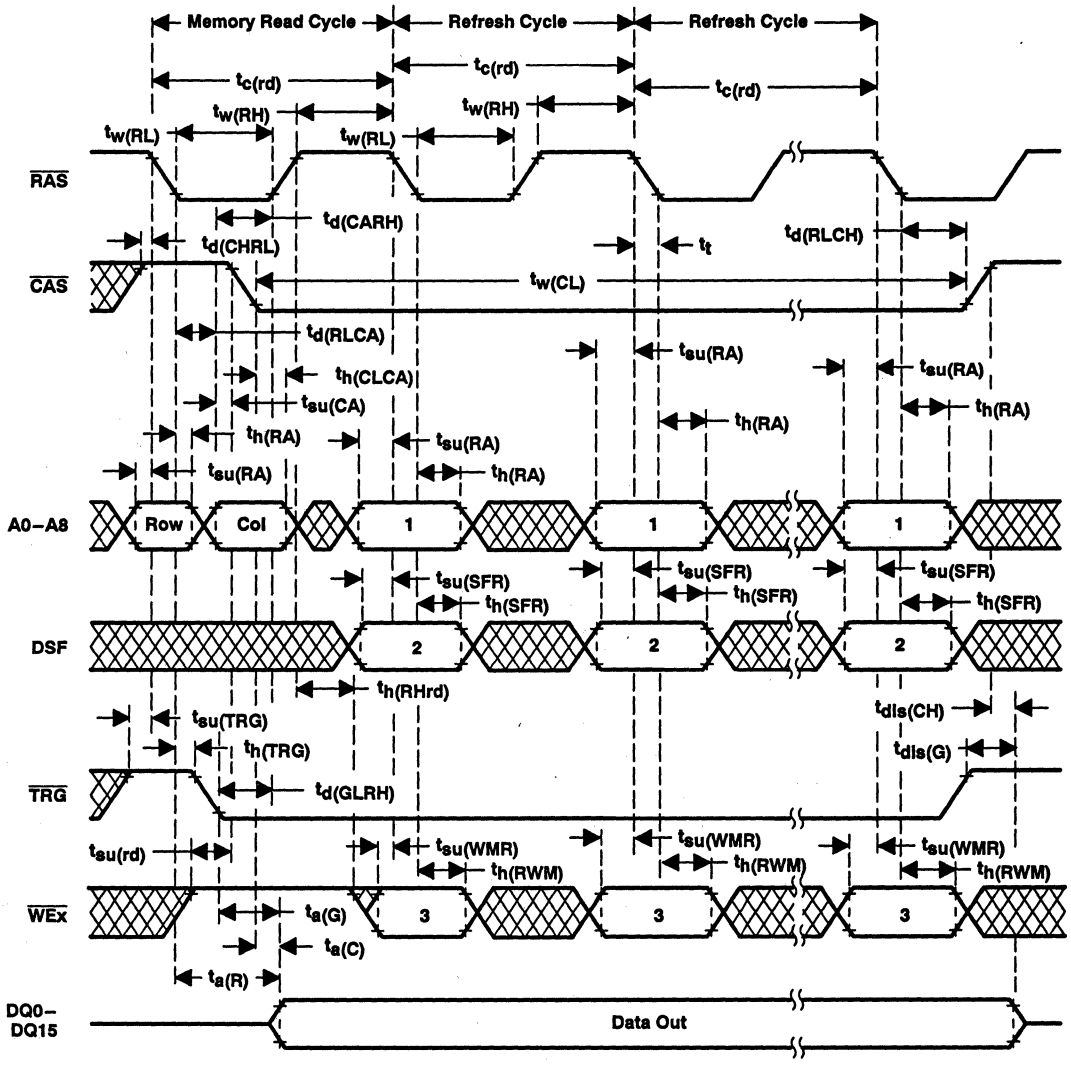
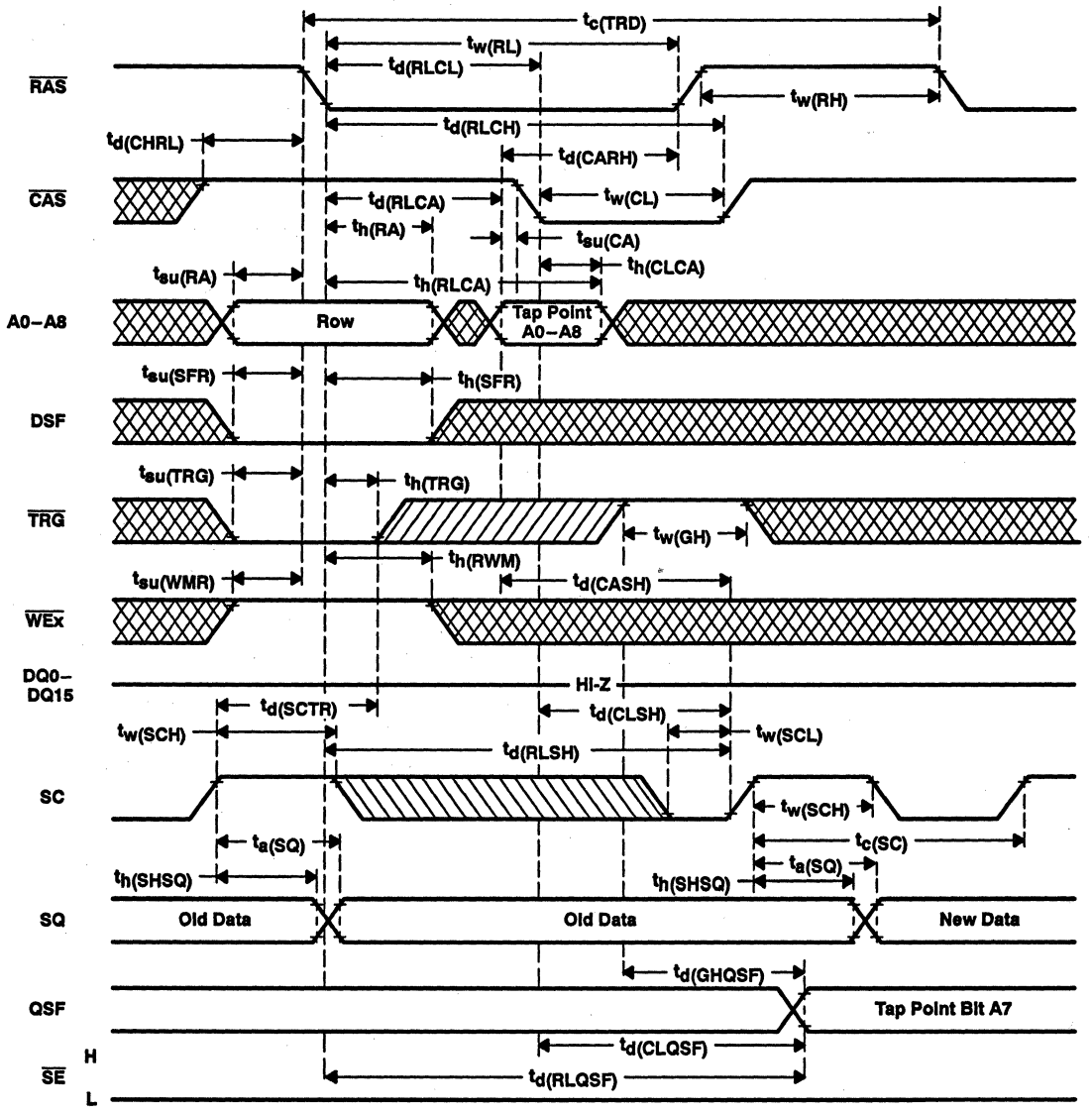


Figure 44. Hidden-Refresh-Cycle Timing

Table 15. Hidden-Refresh-Cycle State Table

CYCLE	STATE		
	1	2	3
CBR refresh with option reset	Don't care	L	H
CBR refresh with no reset	Don't care	H	H
CBR refresh with stop point set and no option reset	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register-transfer cycle. The memory-to-data-register-transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

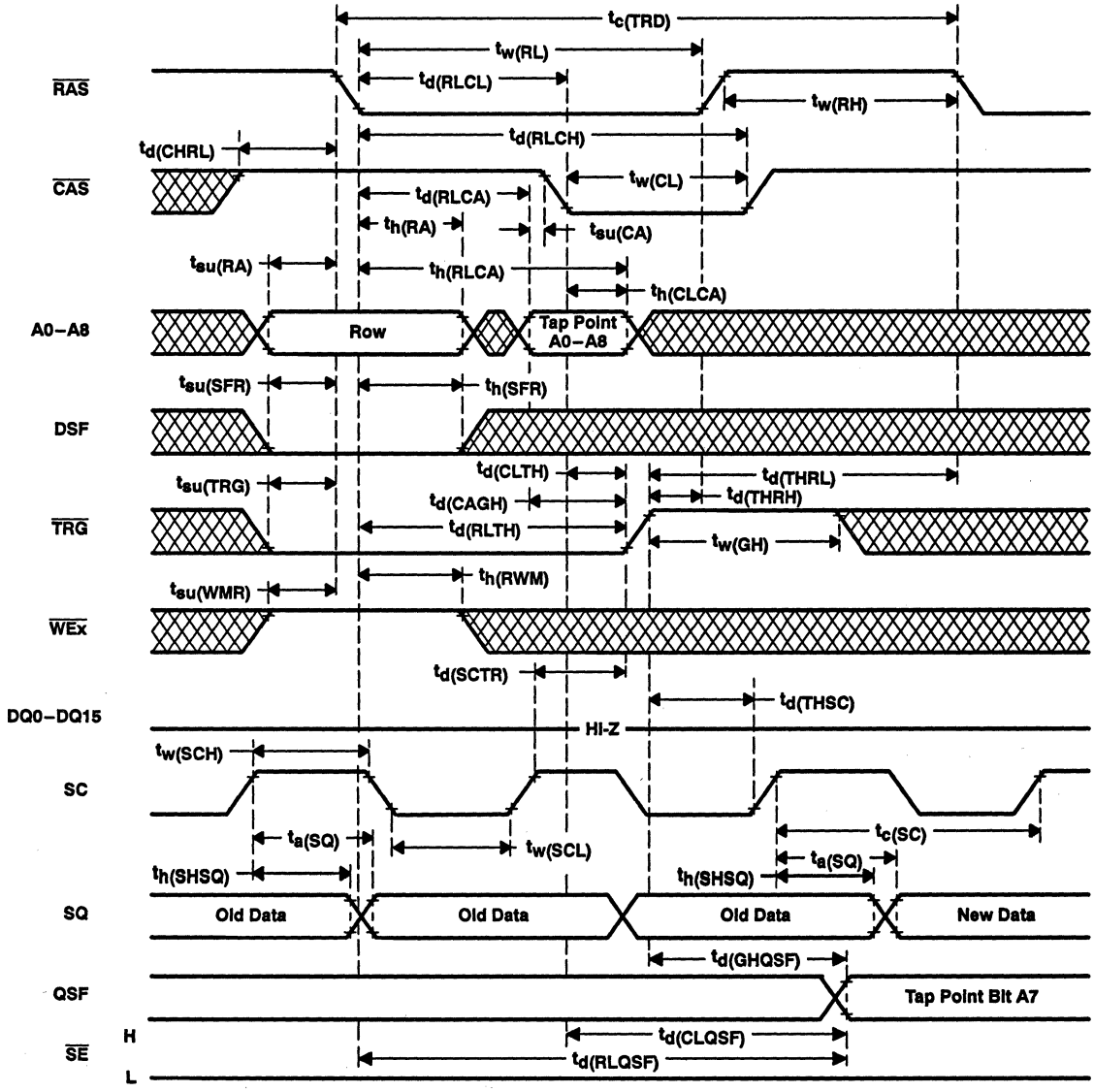
B. Once data is transferred into the data registers, the SAM is in the serial-read mode (i.e., SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0–A7: register tap point; A8: which half of the transferred row

D. Early-load operation is defined as $t_{h(TRG)}$ min < $t_{h(TRG)}$ < $t_{d(RLTH)}$ min.

Figure 45. Full-Register-Transfer Read Timing, Early-Load Operations

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register-transfer cycle. The memory to data register-transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

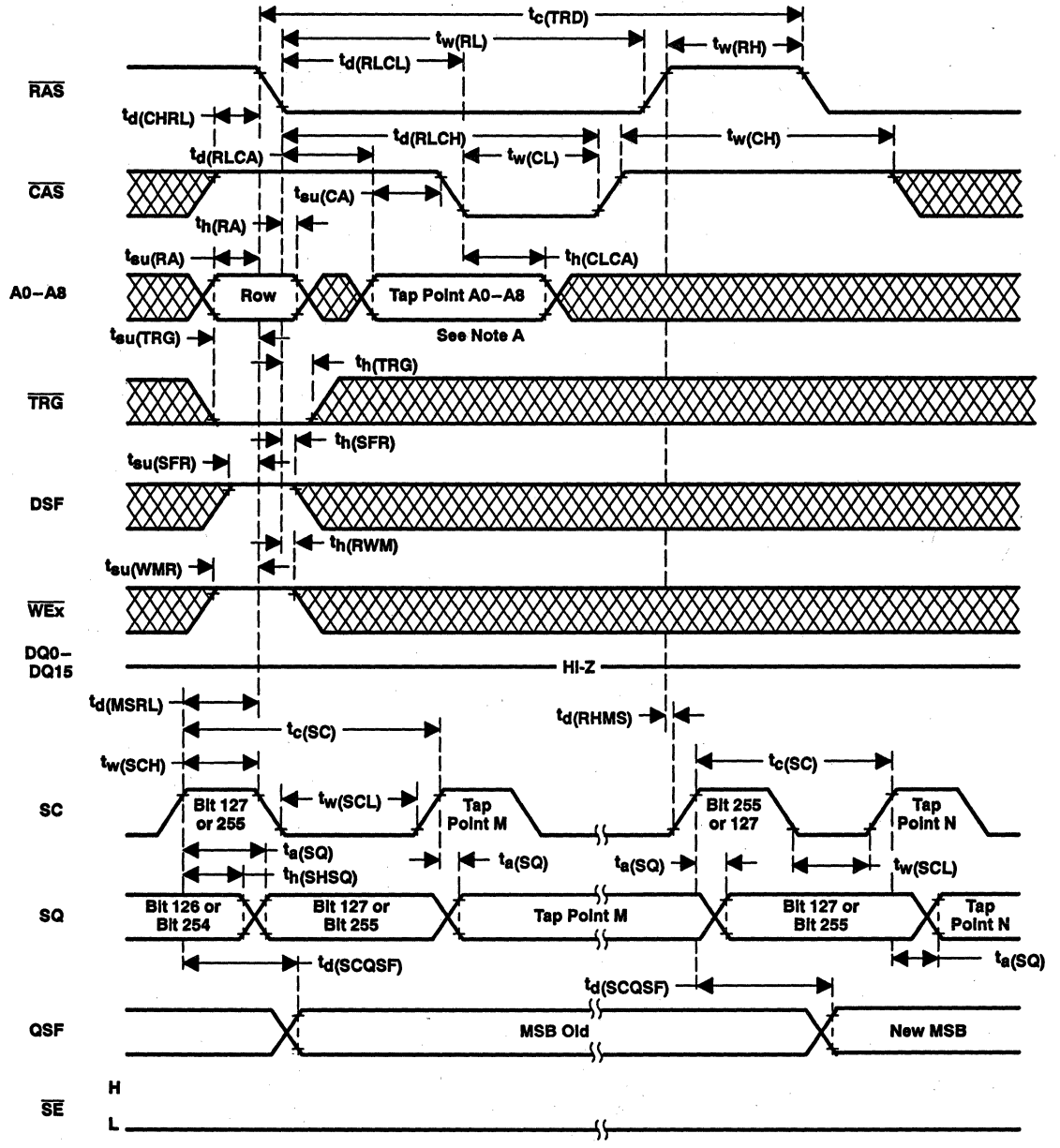
B. Once data is transferred into the data registers, the SAM is in the serial-read mode (i.e., SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0–A7: register tap point; A8: identifies the DRAM half of the row

D. Late load operation is defined as $t_{d(THRH)} < 0$ ns.

Figure 46. Full-Register-Transfer Read Timing, Real-Time Load Operation/Late-Load Operation

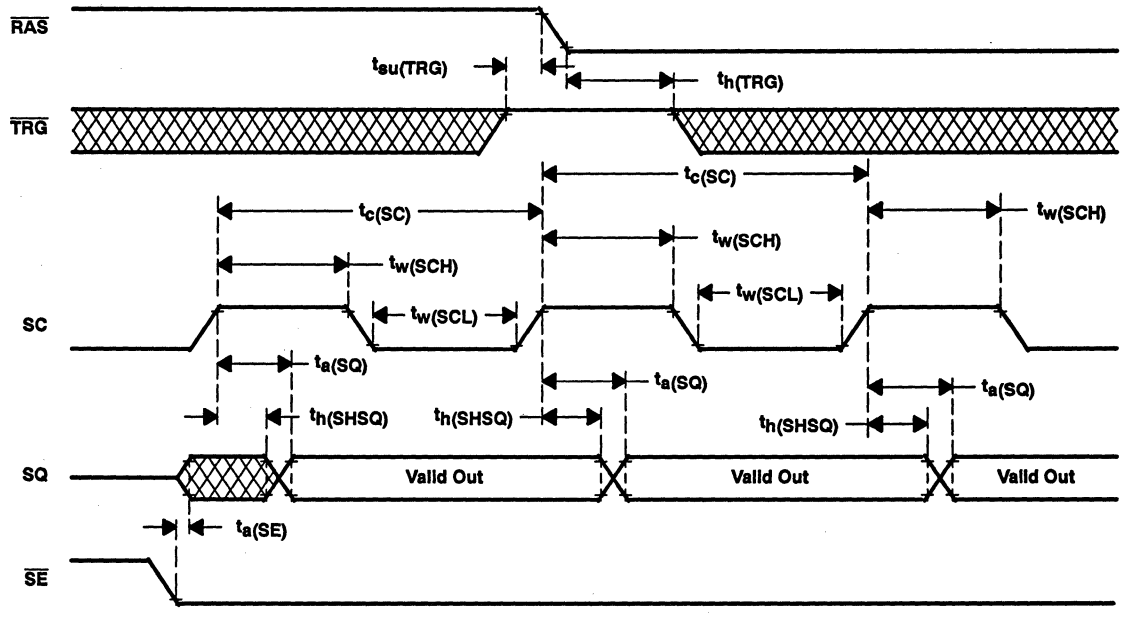
PARAMETER MEASUREMENT INFORMATION



NOTE A: A0–A6: tap point of the given half; A7: don't care; A8: identifies the DRAM half of the row

Figure 47. Split-Register-Transfer Read Timing

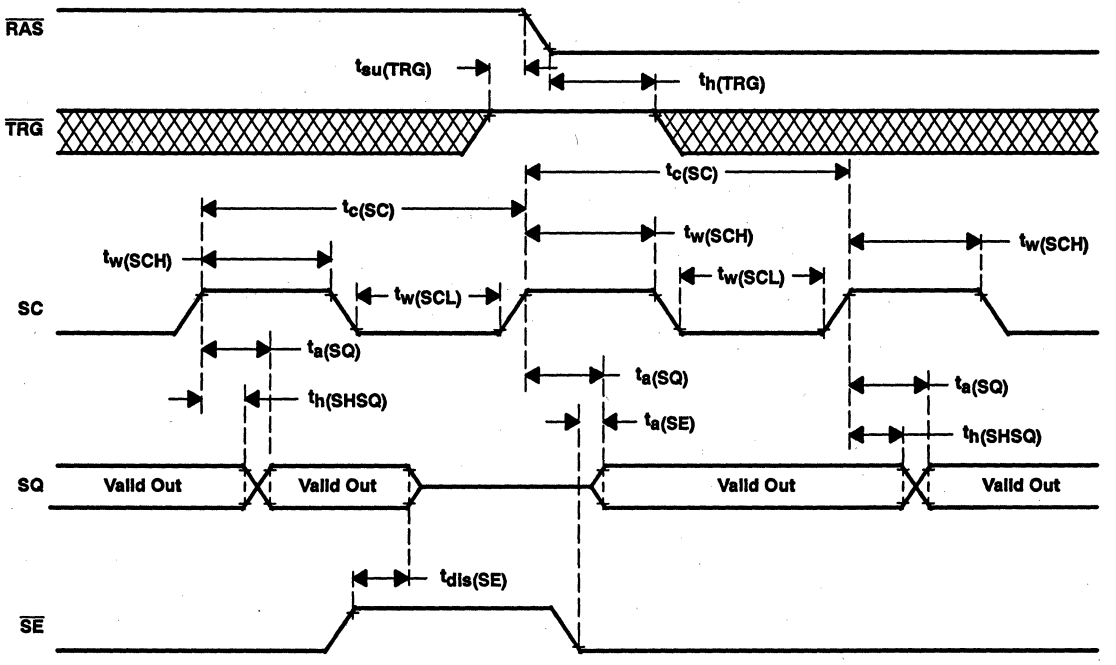
PARAMETER MEASUREMENT INFORMATION



NOTE A: While reading data through the serial-data register, $\overline{TRG}$ is a don't care, except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

Figure 48. Serial-Read Timing ($\overline{SE}$ = V_{IL})

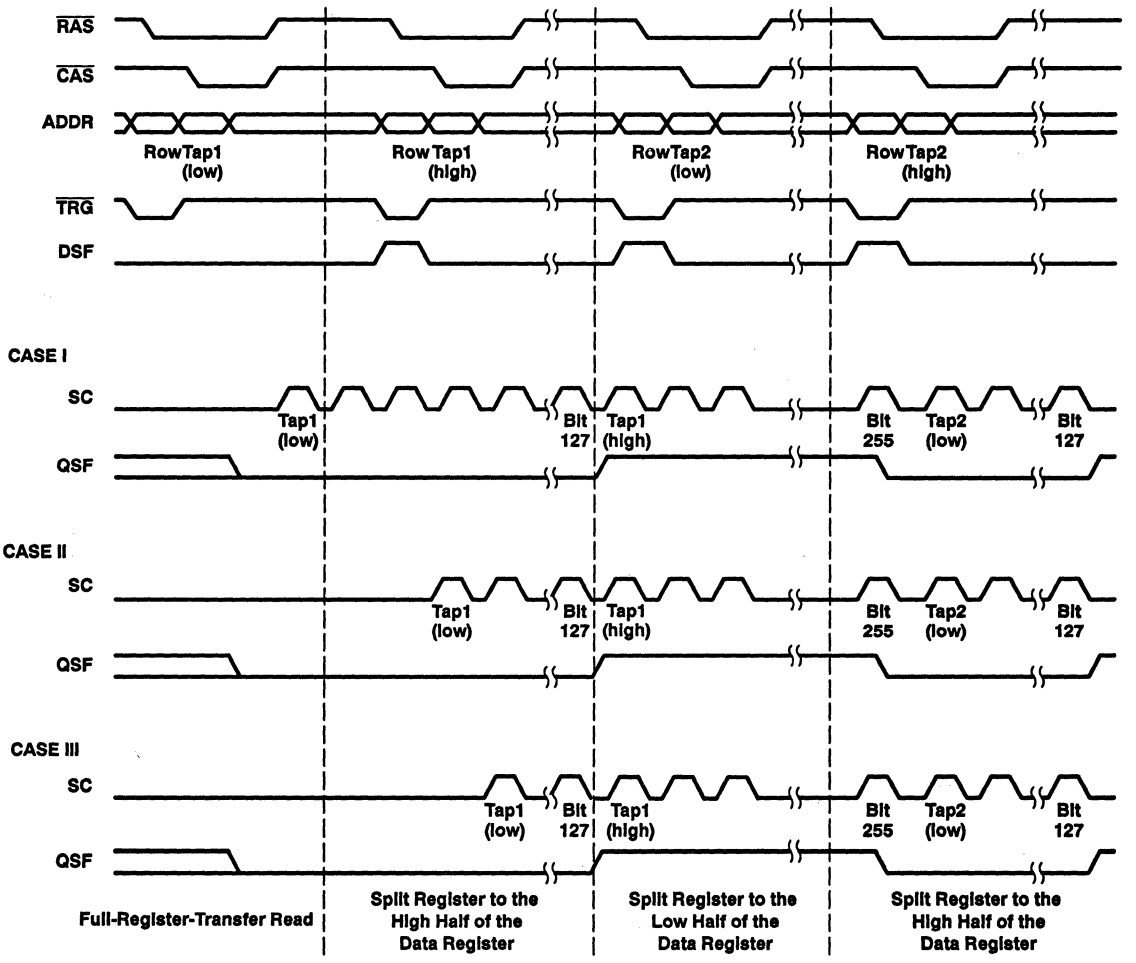
PARAMETER MEASUREMENT INFORMATION



NOTE A: While reading data through the serial-data register, $\overline{TRG}$ is a don't care except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

Figure 49. Serial-Read Timing ($\overline{SE}$-Controlled Read)

PARAMETER MEASUREMENT INFORMATION

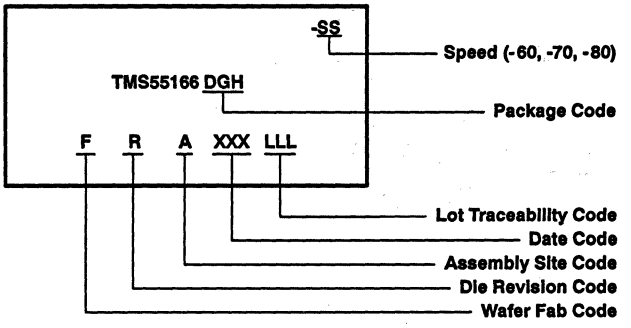


NOTES: A. In order to achieve proper split-register operation, a full-register-transfer read should be performed before the first split-register-transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can then begin either after the full-register-transfer read cycle (CASE I), during the first split-register-transfer cycle (CASE II), or even after the first split-register-transfer cycle (CASE III). There is no minimum requirement of SC clock between the full-register-transfer read cycle and the first split-register cycle.

B. A split-register-transfer into the inactive half is not allowed until $t_{d(MSRL)}$ is met. $t_{d(MSRL)}$ is the minimum delay time between the rising edge of the serial clock of the last bit (bit 127 or 255) and the falling edge of $\overline{RAS}$ of the split-register-transfer cycle into the inactive half. After the $t_{d(MSRL)}$ is met, the split-register-transfer into the inactive half must also satisfy the minimum $t_{d(RHMS)}$ requirement. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register-transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 127 or 255).

Figure 50. Split-Register Operating Sequence

device symbolization



Contents

CHAPTER 6. SINGLE-IN-LINE MEMORY MODULES (SIMMS)

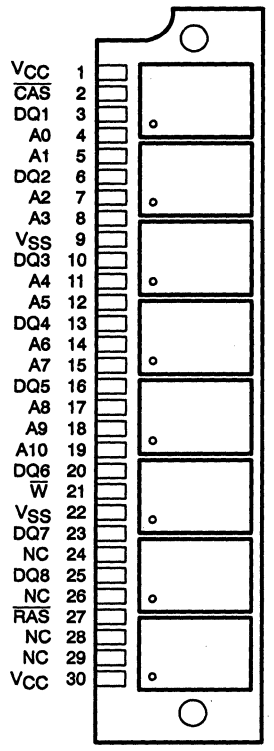
SMMS508C – MARCH 1992 – REVISED JUNE 1995

- **Organization . . . 4194304 × 8**
- **Single 5-V Power Supply (±10% Tolerance)**
- **30-Pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes Eight 4-Megabit DRAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Long Refresh Period 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'4100GAD8-60	60 ns	30 ns	15 ns	110 ns
'4100GAD8-70	70 ns	35 ns	18 ns	130 ns
'4100GAD8-80	80 ns	40 ns	20 ns	150 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**

SINGLE IN-LINE MODULE
(TOP VIEW)



description

The TM4100GAD8 is a dynamic random-access memory (DRAM) module organized as 4194304 × 8 bits in a 30-pin leadless single in-line memory module (SIMM).

The SIMM is composed of eight TMS44100DJ 4194304 × 1-bit DRAMs in 20/26-lead plastic small-outline J-lead packages (SOJ) mounted on a substrate with decoupling capacitors.

The TM4100GAD8 is available in the AD single-sided, leadless module for use with sockets.

The TM4100GAD8 is characterized for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ8	Data In/Data Out
NC	No Internal Connection
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

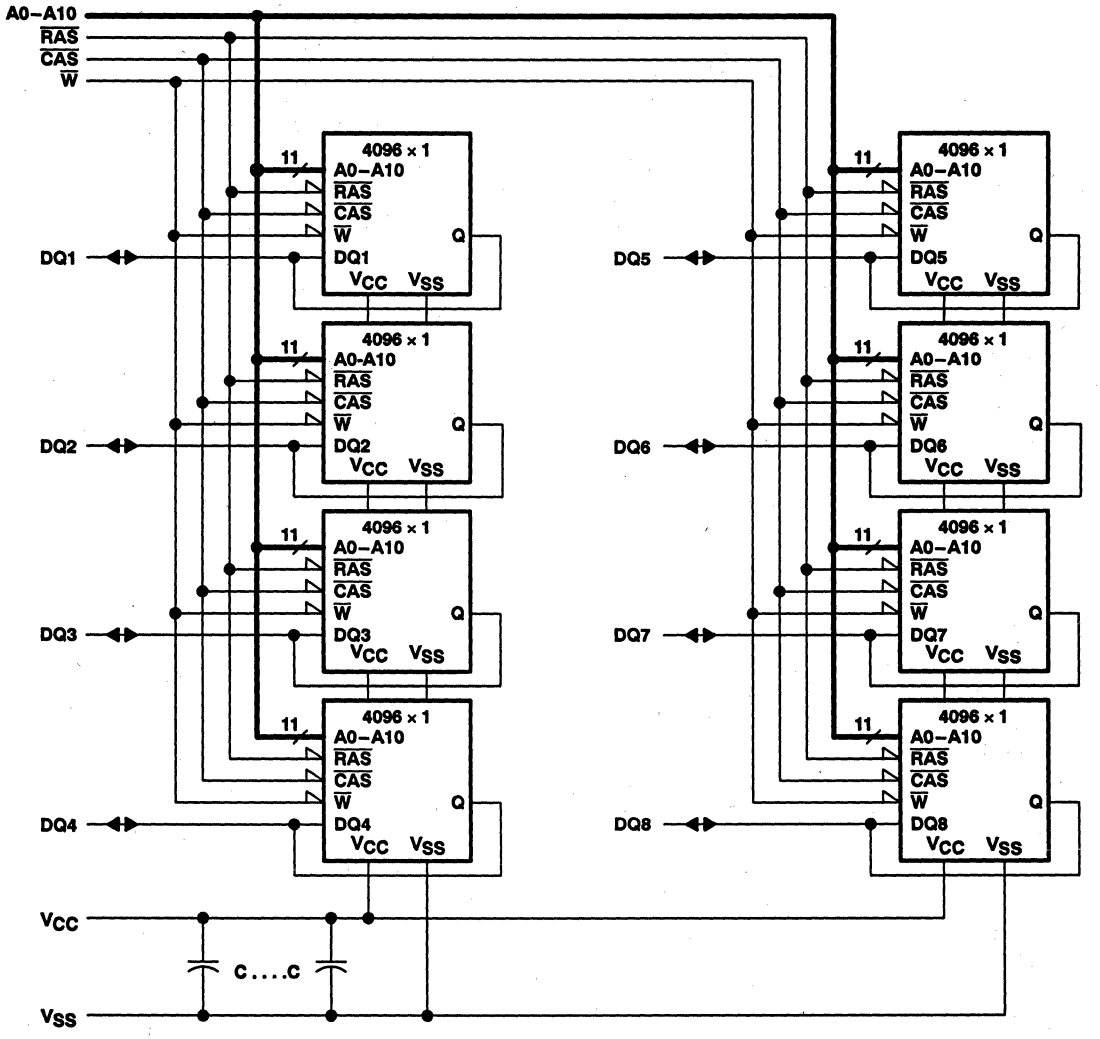
operation

The TM4100GAD8 operates as eight TMS44100DJs connected as shown in the functional block diagram. Refer to the TMS44100 data sheet for details of its operation. The common I/O feature of the TM4100GAD8 dictates the use of early-write cycles to prevent contention on D and Q.

single in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate over copper

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... –1 V to 7 V
Supply voltage range on V_{CC} ..... –1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 8 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'4100GAD8-60		'4100GAD8-70		'4100GAD8-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		840		720		640	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high,		16		16		16	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		8		8		8	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR‡) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR‡)		840		720		640	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		720		640		560	mA

‡ $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A10		40	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		56	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		56	pF
C_O	Output capacitance (pins DQ1–DQ8)		12	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V and the bias on the pin under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'4100GAD8-60		'4100GAD8-70		'4100GAD8-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low impedance	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4100GAD8-60		'4100GAD8-70		'4100GAD8-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{PC}	Cycle time, page-mode read or write (see Note 8)	40		45		50		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{DH}	Hold time, data	10		15		15		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 9)	50		55		60		ns

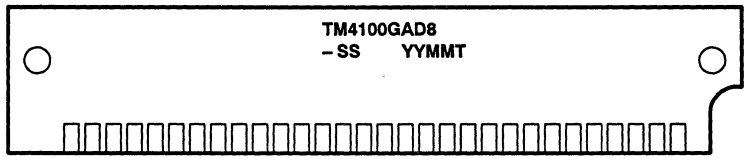
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
9. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
10. The maximum value is specified only to assure access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'4100GAD8-60		'4100GAD8-70		'4100GAD8-80		UINT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 11)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 11)	0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Hold time, $\overline{W}$ low after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{WTH}	Hold time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, write	15		15		15		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{CAS}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{WTS}	Setup time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{TAA}	Access time from address (test mode)	35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 9: The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed

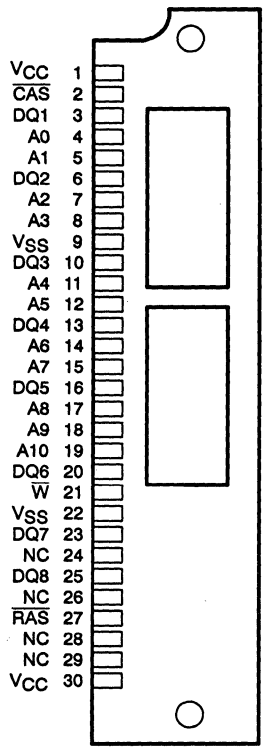
NOTE A: The location of symbolization may vary.

- **Organization . . . 4194304 × 8**
- **Single 5-V Power Supply (±10% Tolerance)**
- **30-Pin Single-In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes Two 16-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period 32 ms (2048 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'497GU8-60	60 ns	30 ns	15 ns	110 ns
'497GU8-70	70 ns	35 ns	18 ns	130 ns
'497GU8-80	80 ns	40 ns	20 ns	150 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Enhanced Page-Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ ($\overline{CBR}$), $\overline{RAS}$-Only, and Hidden Refresh**

U SINGLE-IN-LINE PACKAGE
(TOP VIEW)



description

The TM497GU8 is a 4M-byte dynamic random-access memory module organized as 4194304 × 8 bits in a 30-pin leadless single-in-line memory module (SIMM).

The SIMM is composed of two TMS417400DJ, 4194304 × 4-bit dynamic RAMs in 24/26-lead plastic small-outline J-lead (SOJ) packages mounted on a substrate with decoupling capacitors.

The TM497GU8 is available in the U single-sided, leadless module for use with sockets and is characterized for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ8	Data In/Data Out
NC	No Internal Connection
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

operation

The TM497GU8 operates as two TMS417400DJs connected as shown in the functional block diagram. Refer to the TMS417400 data sheet for details of its operation. The common I/O feature of the TM497GU8 dictates the use of early-write cycles to prevent contention on D and Q.

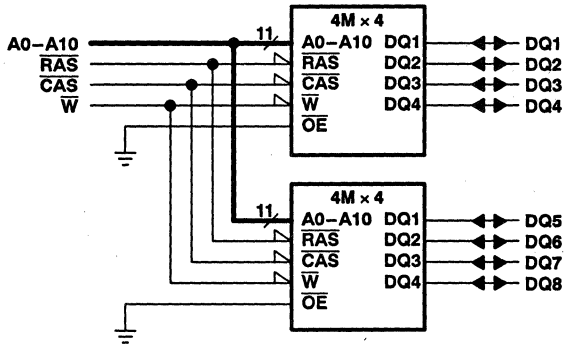
power up

To achieve proper operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only orCBR) cycle.

single-in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate over copper

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 1 V to 7 V
Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 2 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'497GU8-60		'497GU8-70		'497GU8-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		220		200		180	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		4		4		4	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2		2		2	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, $\overline{RAS}$ cycling, Minimum cycle, $\overline{CAS}$ high		220		200		180	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, $\overline{RAS}$ low, t_{PC} = MIN, $\overline{CAS}$ cycling		140		120		100	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A10		10	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		14	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		14	pF
C_o	Output capacitance, DQ1–DQ8		7	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on the pin under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'497GU8-60		'497GU8-70		'497GU8-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low-impedance state	0		0		0		ns
t_{OH}	Output disable time from start of $\overline{CAS}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

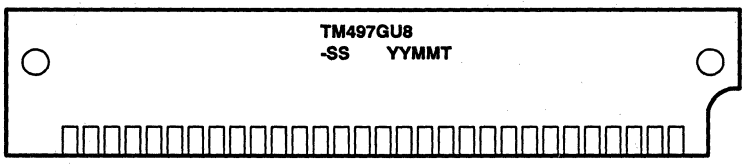
NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'497GU8-60		'497GU8-70		'497GU8-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 7 and 8)	40		45		50		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{CAS}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low	10		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to assure access time

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed

NOTE: The location of the part number may vary.

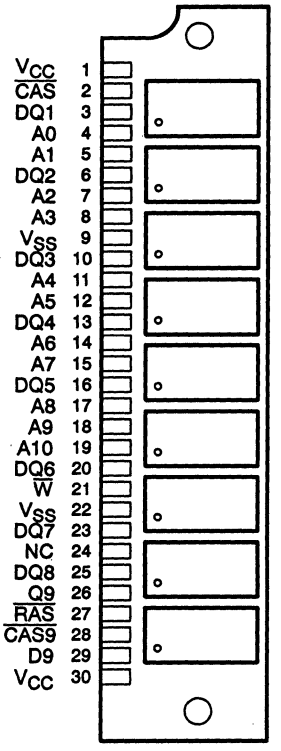
TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

- **Organization . . . 4194304 × 9**
- **Single 5-V Power Supply (±10% Tolerance)**
- **30-Pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes Nine 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Long Refresh Period 16 ms (1024 Cycles)**
- **All Inputs, Outputs, and Clocks Fully TTL Compatible**
- **3-State Outputs**
- **Performance Ranges:**

	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
'4100EAD9-60	60 ns	15 ns	30 ns	110 ns
'4100EAD9-70	70 ns	18 ns	35 ns	130 ns
'4100EAD9-80	80 ns	20 ns	40 ns	150 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**

SINGLE IN-LINE MODULE
(TOP VIEW)



description

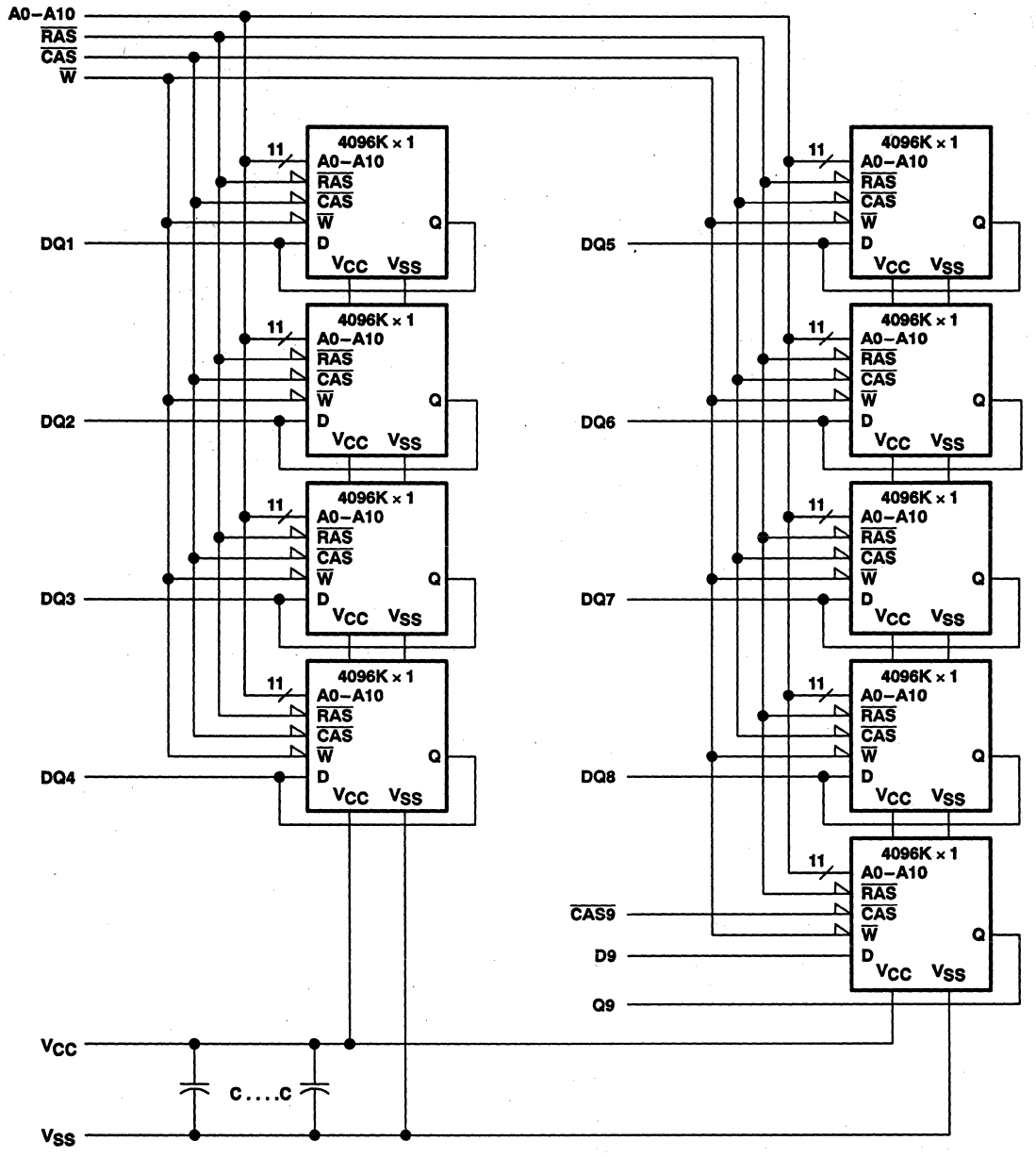
The TM4100EAD9 is a dynamic random-access memory module organized as 4194304 × 9 [bit nine (D9, Q9) is generally used for parity and is controlled by $\overline{CAS9}$] in a 30-pin leadless single in-line memory module (SIMM).

This module is composed of nine TMS44100DJ, 4194304 × 1-bit dynamic RAMs (DRAMs) each in a 20/26-lead plastic small-outline J-lead package (SOJ) mounted on a substrate with decoupling capacitors.

The TM4100EAD9 is characterized for operation from 0°C to 70°C and is available in the AD single-sided, leadless module for use with sockets.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobe
DQ1–DQ8	Data In/Data Out
D9	Data In
NC	No Internal Connection
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

operation

The TM4100EAD9 operates as nine TMS44100DJs connected as shown in the functional block diagram. Refer to the TMS44100 data sheet for details of its operation. The common I/O feature of the TM4100EAD9 dictates the use of early-write cycles to prevent contention on D and Q.

single in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate over copper

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 9 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'4100EAD9-60		'4100EAD9-70		'4100EAD9-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		945		810		720	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		18		18		18	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		9		9		9	mA
I_{CC3}	Average refresh current (RAS only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		945		810		720	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		810		720		630	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A10		45	pF
$C_{i(D)}$	Input capacitance, data input (pin D9)		5	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		63	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		63	pF
$C_{o(DQ)}$	Output capacitance, DQ1–Q8		12	pF
C_O	Output capacitance, Q9		7	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'4100EAD9-60		'4100EAD9-70		'4100EAD9-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low-impedance	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4100EAD9-60		'4100EAD9-70		'4100EAD9-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{PC}	Cycle time, page-mode read or write (see Note 8)	40		45		50		ns
t_{RASP}	Pulse duration, page mode $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, write	15		15		15		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 11)	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{WTS}	Setup time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 12)	50		55		60		ns
t_{DH}	Hold time, data (see Note 10)	10		15		15		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 12)	50		55		60		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 13)	0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low (early-write operation only)	15		15		15		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low (see Note 12)	50		55		60		ns
t_{WHR}	Hold time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{WTH}	Hold time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns

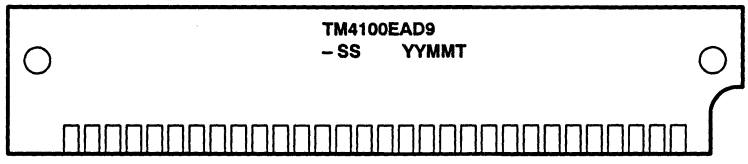
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ 5 ns.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'4100EAD9-60		'4100EAD9-70		'4100EAD9-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 14)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{TAA}	Access time from address (test mode)	35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTE 14: The maximum value is specified only to assure access time.

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed

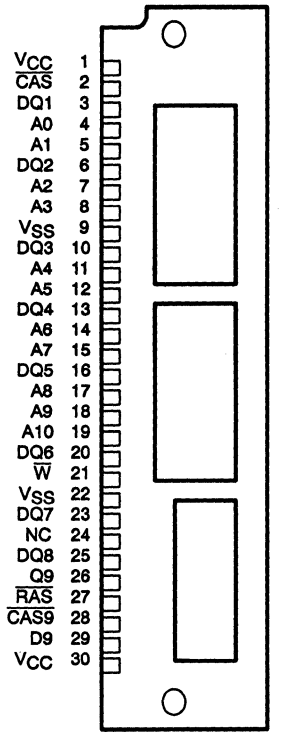
NOTE: The location of symbolization may vary.

- **Organization . . . 4194304 × 9**
- **Single 5-V Power Supply (±10% Tolerance)**
- **30-Pin Single-In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes One 4-Megabit and Two 16-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period 32 ms† (2048 Cycles)**
- **All Inputs, Outputs, and Clocks Fully TTL Compatible**
- **3-State Outputs**
- **Performance Ranges:**

	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME $t_{(AA)}$ (MAX)	ACCESS TIME (t_{CAC}) (MAX)	READ OR WRITE CYCLE (MIN)
'497EU9-60	60 ns	30 ns	15 ns	110 ns
'497EU9-70	70 ns	35 ns	18 ns	130 ns
'497EU9-80	80 ns	40 ns	20 ns	150 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ ($\overline{CBR}$), $\overline{RAS}$-Only, and Hidden Refresh**

U SINGLE-IN-LINE PACKAGE
(TOP VIEW)



description

The TM497EU9 is a 4M-byte dynamic random-access memory (RAM) organized as 4194304 × 9 bits [bit nine (D9, Q9) is generally used for parity and is controlled by $\overline{CAS9}$] in a 30-pin leadless single-in-line memory module (SIMM). The SIMM is composed of two TMS417400DJ, 4194304 × 4-bit dynamic RAMs, each in a 24/26-lead plastic small-outline J-lead (SOJ) package, and one TMS44100DJ, 4194304 × 1-bit dynamic RAM in a 20/26-lead plastic SOJ package, mounted on a substrate with decoupling capacitors.

PIN NOMENCLATURE

A0–A10	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobe
DQ1–DQ8	Data In/Data Out
D9	Data In
NC	No Connection
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

The TM497EU9 is available in the U single-sided, leadless module for use with sockets and is characterized for operation from 0°C to 70°C.

† A0–A9 address lines must be refreshed every 16 ms.

operation

The TM497EU9 operates as two TMS417400DJs and one TMS44100DJ connected as shown in the functional block diagram (refer to the TMS417400 and TMS44100 data sheets for details of their operation). The common I/O feature of the TM497EU9 dictates the use of early write cycles to prevent contention on D and Q.

refresh

The refresh period is extended to 32 ms and, during this period, each of the 2048 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. In addition, the ten least significant row addresses (A0–A9) must be refreshed every 16 ms as required by the TMS44100.

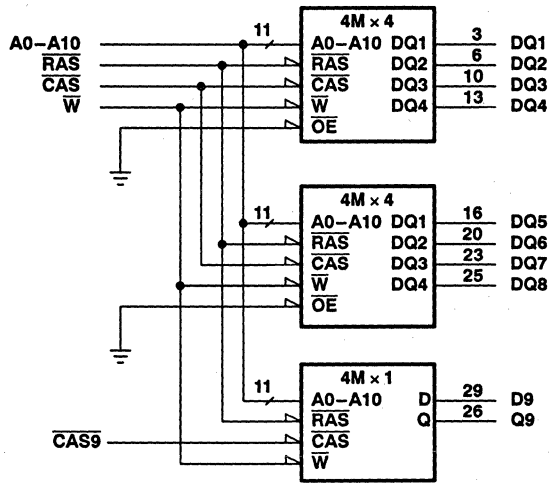
power up

To achieve proper operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

single-in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate over copper

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... – 1 V to 7 V
Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 3 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'497EU9-60		'497EU9-70		'497EU9-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		325		290		260	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		6		6		6	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3		3		3	
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		325		290		260	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		210		180		150	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER			MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A10			15	pF
$C_{i(D)}$	Input capacitance, data input (D9)			5	pF
$C_{i(R)}$	Input capacitance, strobe input ($\overline{RAS}$)			21	pF
$C_{i(C)}$	Input capacitance, strobe inputs	$\overline{CAS}$		14	pF
		$\overline{CAS9}$		7	
$C_{i(W)}$	Input capacitance, $\overline{W}$			21	pF
$C_{o(DQ)}$	Output capacitance (DQ1–DQ8)			7	pF
$C_{o(Q)}$	Output capacitance (Q9)			7	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pin under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'497EU9-60		'497EU9-70		'497EU9-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low-impedance state	0		0		0		ns
t_{OH}	Output disable time, start of $\overline{CAS}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

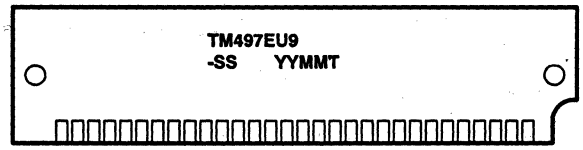
NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'497EU9-60		'497EU9-70		'497EU9-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{PC}	Cycle time, page mode read or write (see Notes 7 and 8)	40		45		50		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{CAS}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low	10		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to assure access time.

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed

NOTE: The location of the part number may vary.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

- **Organization**
  TM124BBK32 . . . 1 048 576 × 32
  TM248CBK32 . . . 2 097 152 × 32
- **Single 5-V Power Supply (±10 % Tolerance)**
- **72-pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **TM124BBK32-Utilizes Eight 4-Megabit DRAMs In Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM248CBK32-Utilizes Sixteen 4-Megabit DRAMs In Plastic Small-Outline J-Lead (SOJ) Packages**
- **Distributed Refresh Period**
  16 ms (1024 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines, In Four Blocks**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
TM124BBK32-60	60 ns	15 ns	110 ns
TM124BBK32-70	70 ns	18 ns	130 ns
TM124BBK32-80	80 ns	20 ns	150 ns
TM248CBK32-60	60 ns	15 ns	110 ns
TM248CBK32-70	70 ns	18 ns	130 ns
TM248CBK32-80	80 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air-Temperature Range**
  0°C to 70°C
- **Gold-Tabbed Versions Available:†**
  – TM124BBK32
  – TM248CBK32
- **Tin-Lead (Solder) Tabbed Versions Available:**
  – TM124BBK32S
  – TM248CBK32S

description

TM124BBK32

The TM124BBK32 is a dynamic random-access memory (DRAM) organized as four times 1048576 × 8 in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of eight TMS44400, 1048576 × 4-bit DRAMs, each in 20/26-lead plastic SOJ packages, mounted on a substrate together with decoupling capacitors. Each TMS44400 is described in the TMS44400 data sheet.

The TM124BBK32 is available in the single-sided BK leadless module for use with sockets.

The TM124BBK32 features $\overline{RAS}$ access times of 60 ns, 70 ns and 80 ns. This device is rated for operation from 0°C to 70°C

TM248CBK32

The TM248CBK32 is a dynamic random-access memory organized as four times 2097152 × 8 in a 72-pin leadless SIMM. The SIMM is composed of sixteen TMS44400, 1048576 × 4-bit dynamic RAMs, each in 20/26-lead plastic SOJ packages SOJs, mounted on a substrate together with decoupling capacitors. Each TMS44400 is described in the TMS44400 data sheet.

The TM248CBK32 is available in the double-sided BK leadless module for use with sockets.

The TM248CBK32 features $\overline{RAS}$ access times of 60 ns, 70 ns and 80 ns. This device is rated for operation from 0°C to 70°C

operation

TM124BBK32

The TM124BBK32 operates as eight TMS44400DJs connected as shown in the functional block diagram. Refer to the TMS44400 data sheet for details of operation. The common I/O feature of the TM124BBK32 dictates the use of early write cycles to prevent contention on D and Q.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

TM248CBK32

The TM248CBK32 operates as sixteen TMS44400DJs connected as shown in the functional block diagram. Refer to the TMS44400 data sheet for details of operation. The common I/O feature of the TM248CBK32 dictates the use of early write cycles to prevent contention on D and Q.

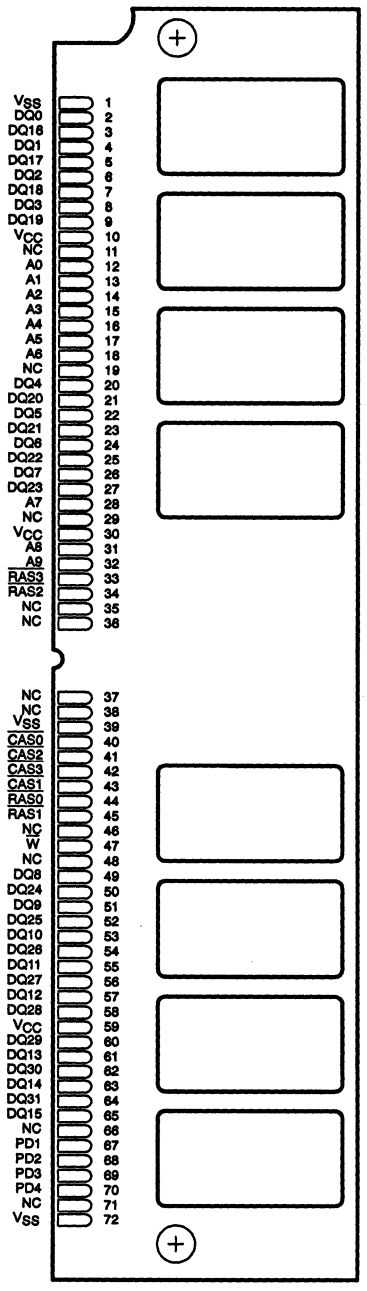
refresh

Refresh period is extended to 16 ms and, during this period, each of the 1024 rows must be strobed with $\overline{RAS}$ in order to retain data. A0-A9 address lines must be refreshed every 16 ms as required by the TMS44400 DRAM. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124BBK32 AND TM248CBK32: Nickel plate and gold plate over copper.
Contact area for TM124BBK32S AND TM248CBK32S: Nickel plate and tin-lead over copper.

BK SINGLE IN-LINE MEMORY MODULE
(TOP VIEW)



TM124BBK32T
(SIDE VIEW)

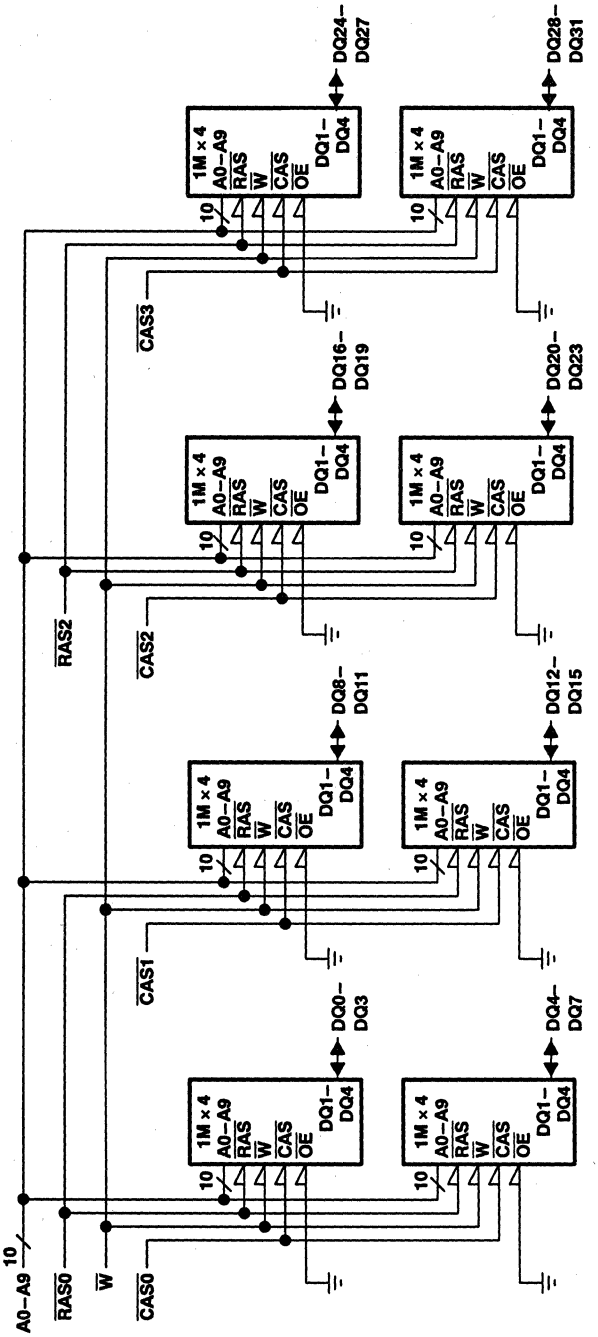
TM248CBK32T
(SIDE VIEW)

PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ31	Data In/Data Out
NC	No Connection
PD1– PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124BBK32	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248CBK32	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

† The packages shown here are not drawn to scale.

functional block diagram (for TM124BBK32 and TM248CBK32, Side 1)



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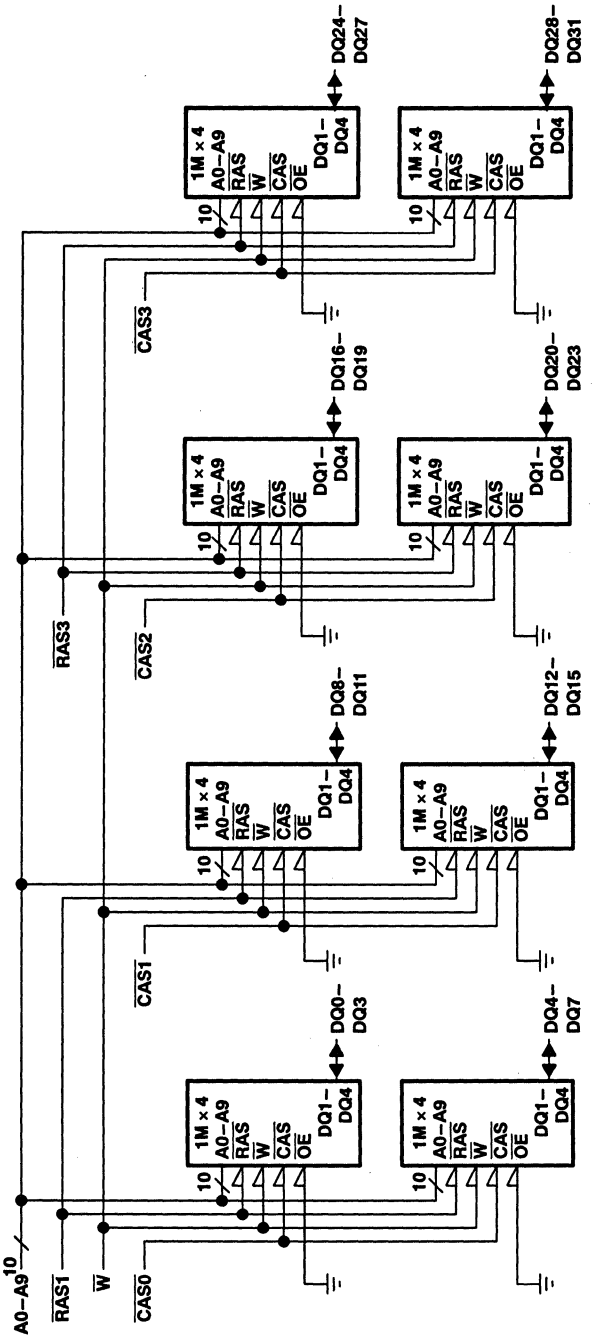
functional block diagram (for TM248CBK32, Side 2)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 8 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124BBK32-60		'124BBK32-70		'124BBK32-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		840		720		640	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		16		16		16	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		8		8		8	
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		840		720		640	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		720		640		560	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'248CBK32-60		'248CBK32-70		'248CBK32-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		±20		±20		±20	μA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		±20		±20		±20	μA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		856		736		656	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		32		32		32	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		16		16		16	
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1680		1440		1280	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		736		656		576	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature f = 1 MHz (see Note 5)

		'124BBK32		'248CBK32		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		40		80	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$		28		28	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$		14		28	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		56		112	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		7		14	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124BBK32-60 '248CBK32-60		'124BBK32-70 '248CBK32-70		'124BBK32-80 '248CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended range of supply voltage and operating free-air temperature

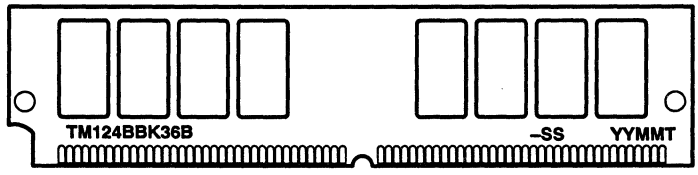
		'124BBK32-60 '248CBK32-60		'124BBK32-70 '248CBK32-70		'124BBK32-80 '248CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{PC}	Cycle time, page-mode read or write (see Note 8)	40		45		50		ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{WP}	Pulse duration, write	15		15		15		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WTS}	Setup time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{DH}	Hold time, data	10		15		15		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 10)	0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 10)	0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low	15		15		15		ns
t_{WHR}	Hold time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low	50		55		60		ns
t_{WTH}	Hold time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 11)	20	45	20	52	20	60	ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	15		15		20		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 11)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PL}min, t_{ASC} should be ≥ 5 ns.
9. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. Maximum value specified only to assure access time.

timing requirements over recommended range of supply voltage and operating free-air temperature (concluded)

		'124BBK32-60 '248CBK32-60		'124BBK32-70 '248CBK32-70		'124BBK32-80 '248CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR refresh only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{TAA}	Access time from address (test mode)	35		40		45		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

device symbolization (TM124BBK32 illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed Code

NOTE: Location of symbolization may vary.

TM124BBK32F, TM124BBK32U 1048576 BY 32-BIT DYNAMIC RAM MODULE
TM248CBK32F, TM248CBK32U 2097152 BY 32-BIT DYNAMIC RAM MODULE

SMMS649A – DECEMBER 1994 – REVISED JUNE 1995

- **Organization**
  TM124BBK32F . . . 1 048 576 × 32
  TM248CBK32F . . . 2 097 152 × 32
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Single-In-Line Memory Module (SIMM) for Use With Socket**
- **TM124BBK32F – Utilizes Two 16-Megabit DRAMs In Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM248CBK32F – Utilizes Four 16-Megabit DRAMs In Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period**
  16 ms (1024 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines In Four Blocks**
- **Enhanced Page-Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR), $\overline{RAS}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'124BBK32F-60	60 ns	30 ns	15 ns	110 ns
'124BBK32F-70	70 ns	35 ns	18 ns	130 ns
'124BBK32F-80	80 ns	40 ns	20 ns	150 ns
'248CBK32F-60	60 ns	30 ns	15 ns	110 ns
'248CBK32F-70	70 ns	35 ns	18 ns	130 ns
'248CBK32F-80	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range**
  0°C to 70°C
- **Gold-Tabbed Versions Available:†**
  – TM124BBK32F
  – TM248CBK32F
- **Tin-Lead (Solder) Tabbed Versions Available:**
  – TM124BBK32U
  – TM248CBK32U

description

TM124BBK32F

The TM124BBK32F is a 32-megabit dynamic random-access memory (DRAM) organized as four times 1 048 576 × 8 in a 72-pin SIMM. The SIMM is composed of two TMS418160DZ, 1 048 576 × 16-bit DRAMs, each in a 42-lead plastic SOJ package mounted on a substrate with decoupling capacitors. The TMS418160DZ is described in the TMS418160 data sheet. The TM124BBK32F SIMM is available in the single-sided BK-leadless module for use with sockets.

TM248CBK32F

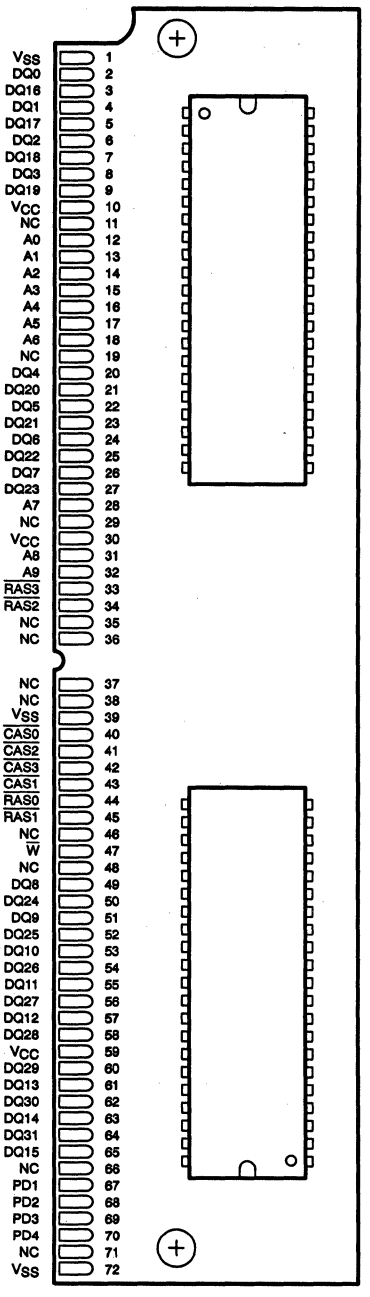
The TM248CBK32F is a 64-megabit DRAM organized as four times 2 097 152 × 8 in a 72-pin SIMM. The SIMM is composed of four TMS418160DZ, 1 048 576 × 16-bit DRAMs, each in a 42-lead plastic SOJ package mounted on a substrate with decoupling capacitors. The TMS418160DZ is described in the TMS418160 data sheet. The TM248CBK32F SIMM is available in the double-sided BK-leadless module for use with sockets.

operation

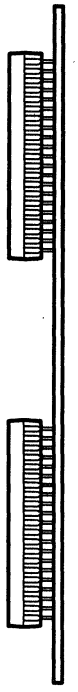
The TM124BBK32F operates as two TMS418160DZs connected as shown in the functional block diagram and Table 1. The TM248CBK32F operates as four TMS418160DZs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early-write cycles to prevent contention on D and Q.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

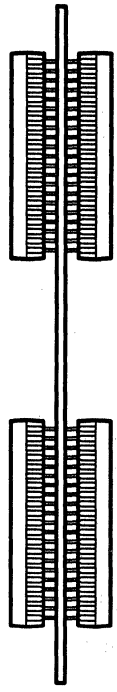
BK SINGLE-IN-LINE MEMORY MODULE
(TOP VIEW)



TM124BBK32F
(SIDE VIEW)



TM248CBK32F
(SIDE VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ31	Data In/Data Out
NC	No Connection
PD1– PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124BBK32F	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248CBK32F	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

Table 1. Connection Table

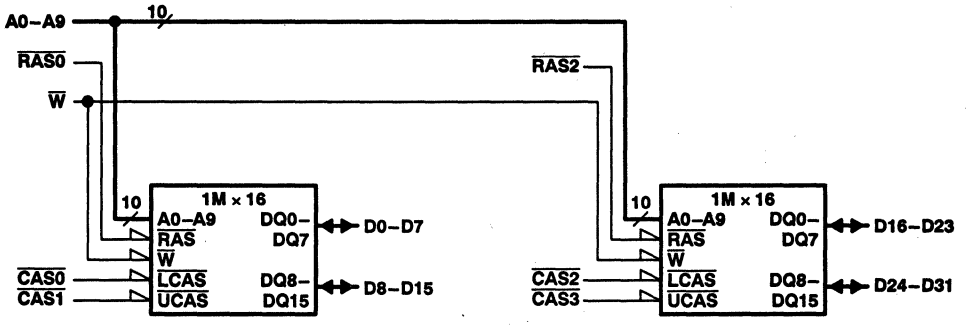
DATA BLOCK	$\overline{RAS}x$		$\overline{CAS}x$
	SIDE 1	SIDE 2†	
DQ0–DQ7	$\overline{RAS}0$	$\overline{RAS}1$	$\overline{CAS}0$
DQ8–DQ15	$\overline{RAS}0$	$\overline{RAS}1$	$\overline{CAS}1$
DQ16–DQ23	$\overline{RAS}2$	$\overline{RAS}3$	$\overline{CAS}2$
DQ24–DQ31	$\overline{RAS}2$	$\overline{RAS}3$	$\overline{CAS}3$

† Side 2 applies to the TM248CBK32F only.

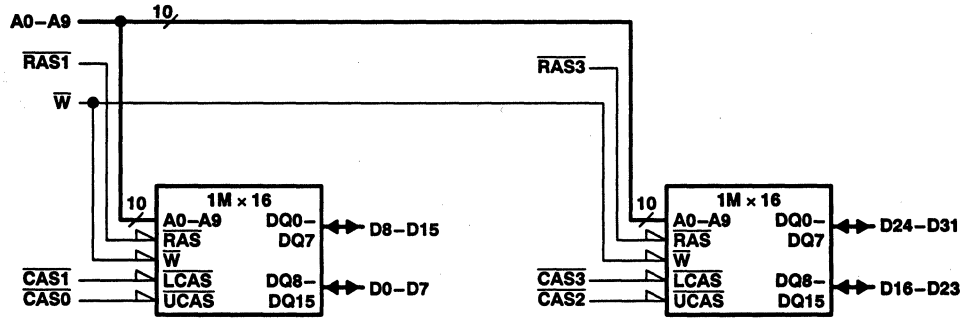
single-in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124BBK32F and TM248CBK32F: Nickel plate and gold plate over copper
Contact area for TM124BBK32U and TM248CBK32U: Nickel plate and tin/lead over copper

functional block diagram (TM124BBK32F and TM248CBK32F, side 1)



functional block diagram (TM248CBK32F, side 2)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –1 V to 7 V
Voltage range on any pin (see Note 1) ..... –1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation: TM124BBK32F, TM124BBK32U ..... 2 W
TM248CBK32F, TM248CBK32U ..... 4 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124BBK32F-60		'124BBK32F-70		'124BBK32F-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		180		160		140	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		4		4		4	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2		2		2	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		180		160		140	mA
I_{CC4}	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		180		160		140	mA

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)†

PARAMETER		TEST CONDITIONS	'248CBK32F-60		'248CBK32F-70		'248CBK32F-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		184		164		144	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		8		8		8	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		4		4		4	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		360		320		280	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		184		164		144	mA

† For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		'124BBK32F		'248CBK32F		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, A0–A9		10		20	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs		7		7	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs		7		14	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		14		28	pF
$C_{o(DQ)}$	Output capacitance on DQ0–DQ31		7		14	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124BBK32F-60 '248CBK32F-60		'124BBK32F-70 '248CBK32F-70		'124BBK32F-80 '248CBK32F-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ to output in low-impedance state	0		0		0		ns
t_{OH}	Output disable time from start of $\overline{CAS}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124BBK32F-60 '248CBK32F-60		'124BBK32F-70 '248CBK32F-70		'124BBK32F-80 '248CBK32F-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{RWC}	Cycle time, read-write	155		181		205		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 7 and 8)	40		45		50		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{CAS}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns

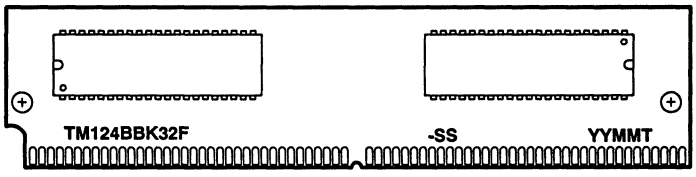
NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'124BBK32F-60 '248CBK32F-60		'124BBK32F-70 '248CBK32F-70		'124BBK32F-80 '248CBK32F-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low	10		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTE 10: The maximum value is specified only to assure access time.

device symbolization (TM124BBK32F illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE: Location of symbolization may vary.

- **Organization . . . 4194304 × 32**
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Single-In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes Eight 16-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period 32 ms (2048 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines in Four Blocks**
- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR), $\overline{RAS}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'497BBK32-60	60 ns	30 ns	15 ns	110 ns
'497BBK32-70	70 ns	35 ns	18 ns	130 ns
'497BBK32-80	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air-Temperature Range 0°C to 70°C**
- **Gold-Tabbed Version Available:† TM497BBK32**
- **Tin-Lead (Solder) Tabbed Version Available: TM497BBK32S**

description

The TM497BBK32 is a 16M-byte dynamic random-access memory (DRAM) organized as four times 4194304 × 8 in a 72-pin leadless single-in-line memory module (SIMM). The SIMM is composed of eight TMS417400DJ, 4194304 × 4-bit DRAMs, each in 24/26-lead plastic small-outline J-lead (SOJ) packages mounted on a substrate with decoupling capacitors. The TMS417400DJ is described in the TMS417400 data sheet.

The TM497BBK32 SIMM is available in the single-sided BK leadless module for use with sockets. The TM497BBK32 SIMM features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is characterized for operation from 0°C to 70°C.

operation

The TM497BBK32 operates as eight TMS417400DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

refresh

The refresh period is extended to 32 ms and, during this period, each of the 2048 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

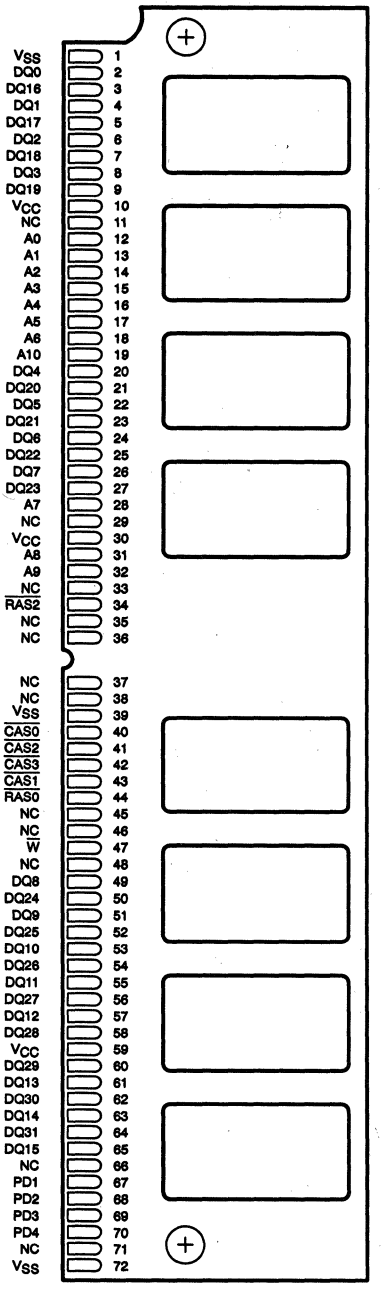
power up

To achieve proper operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

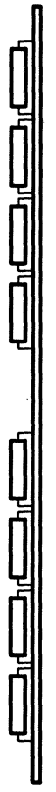
† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

BK SINGLE-IN-LINE PACKAGE

(TOP VIEW)



(SIDE VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ31	Data In/Data Out
NC	No Connection
PD1–PD4	Presence Detects
$\overline{RAS0}$, $\overline{RAS2}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM497BBK32	80 ns	V_{SS}	NC	NC	V_{SS}
	70 ns	V_{SS}	NC	V_{SS}	NC
	60 ns	V_{SS}	NC	NC	NC

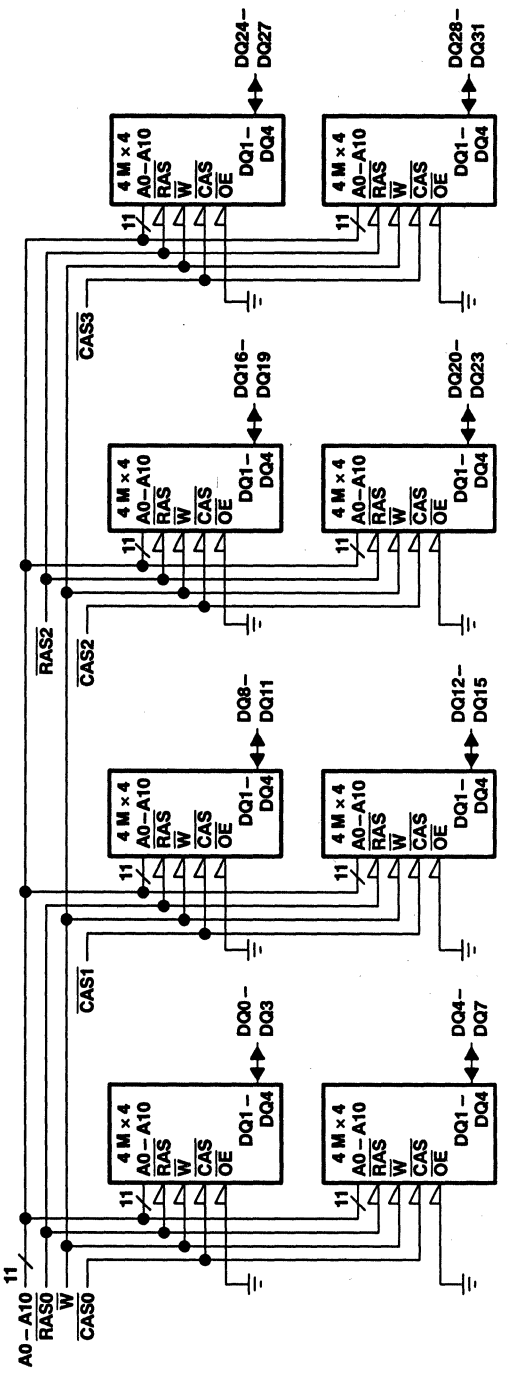
Table 1. Connection Table

DATA BLOCK	$\overline{RAS}x$	$\overline{CAS}x$
DQ0–DQ7	$\overline{RAS}0$	$\overline{CAS}0$
DQ8–DQ15	$\overline{RAS}0$	$\overline{CAS}1$
DQ16–DQ23	$\overline{RAS}2$	$\overline{CAS}2$
DQ24–DQ31	$\overline{RAS}2$	$\overline{CAS}3$

single-in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM497BBK32: Nickel plate and gold plate over copper
Contact area for TM497BBK32S: Nickel plate and tin-lead over copper

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –1 V to 7 V
Voltage range on any pin (see Note 1) ..... –1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 8 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	'497BBK32-60		'497BBK32-70		'497BBK32-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		±80		±80		±80	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		880		800		720	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		16		16		16	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		8		8		8	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, $\overline{RAS}$ cycling, ($\overline{RAS}$ only); $\overline{CAS}$ low (CBR)	Minimum cycle, $\overline{CAS}$ high $\overline{RAS}$ low after	880		800		720	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, $\overline{RAS}$ low,	t_{PC} = MIN, $\overline{CAS}$ cycling	560		480		400	mA

‡ For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

	PARAMETER	MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		40	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs		28	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs		14	pF
$C_{i(W)}$	Input capacitance, write-enable input		56	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		7	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	'497BBK32-60		'497BBK32-70		'497BBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low-impedance state	0		0		0		ns
t_{OH}	Output disable time from start of $\overline{CAS}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'497BBK32-60		'497BBK32-70		'497BBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 7 and 8)	40		45		50		ns
t_{RASP}	Pulse duration, page-mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, non-page-mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{CAS}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$-low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$-low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$-low before $\overline{CAS}$ low	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$-high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns

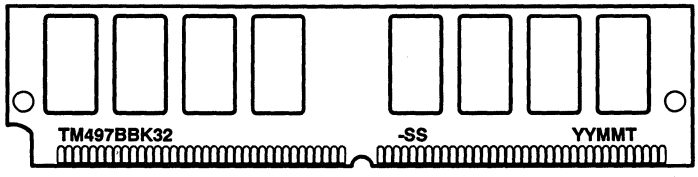
NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'497BBK32-60		'497BBK32-70		'497BBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low	10		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	3	30	3	30	3	30	ns

9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to assure access time.

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE: The location of the part number may vary.

- **Organization**
  TM893CBK32 . . . 8388608 × 32 Bit
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin, Leadless Single In-Line Memory Module (SIMM) for Use With Sockets**
- **TM893CBK32 – Utilizes Sixteen 16-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period**
  32 ms (2048 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines in Four Blocks**
- **Enhanced Page-Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR), $\overline{RAS}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'893CBK32-60	60 ns	30 ns	15 ns	110 ns
'893CBK32-70	70 ns	35 ns	18 ns	130 ns
'893CBK32-80	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air-Temperature Range**
  0°C to 70°C
- **Gold-Tabbed Versions Available:†**
  TM893CBK32
- **Tin-Lead (Solder) Tabbed Versions Available:**
  TM893CBK32S

description

The TM893CBK32 is a 32-megabyte, dynamic random-access memory organized as four times 8388608 × 8 bits in a 72-pin, leadless single in-line memory module (SIMM). The SIMM is composed of 16 TMS417400DJ, 4194304 × 4-bit dynamic RAMs, each in 24/26-lead plastic small-outline J-lead (SOJ) packages mounted on a substrate with decoupling capacitors. The TMS417400DJ is described in the TMS417400 data sheet. The TM893CBK32 SIMM is available in the double-sided BK leadless module for use with sockets.

operation

The TM893CBK32 operates as sixteen TMS417400DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early-write cycles to prevent contention on D and Q.

refresh

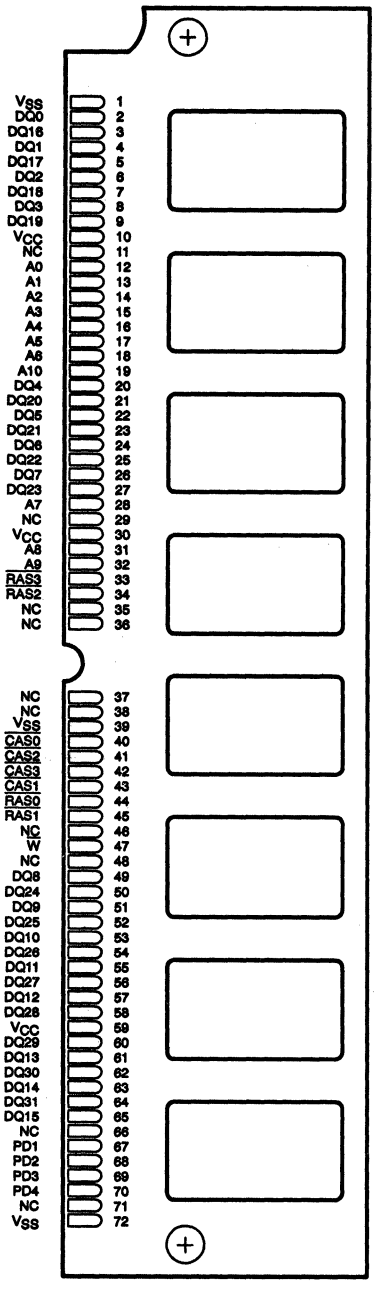
The refresh period is extended to 32 ms, and during this period each of the 2048 rows must be strobed with $\overline{RAS}$ to retain data. To conserve power, $\overline{CAS}$ can remain high during the refresh sequence.

power up

To achieve proper operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

BK SINGLE-IN-LINE PACKAGE
(TOP VIEW)



TM893CBK32
(SIDE VIEW)

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ31	Data In/Data Out
NC	No Connection
PD1–PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM893CBK32	80 ns	NC	V_{SS}	NC	V_{SS}
	70 ns	NC	V_{SS}	V_{SS}	NC
	60 ns	NC	V_{SS}	NC	NC

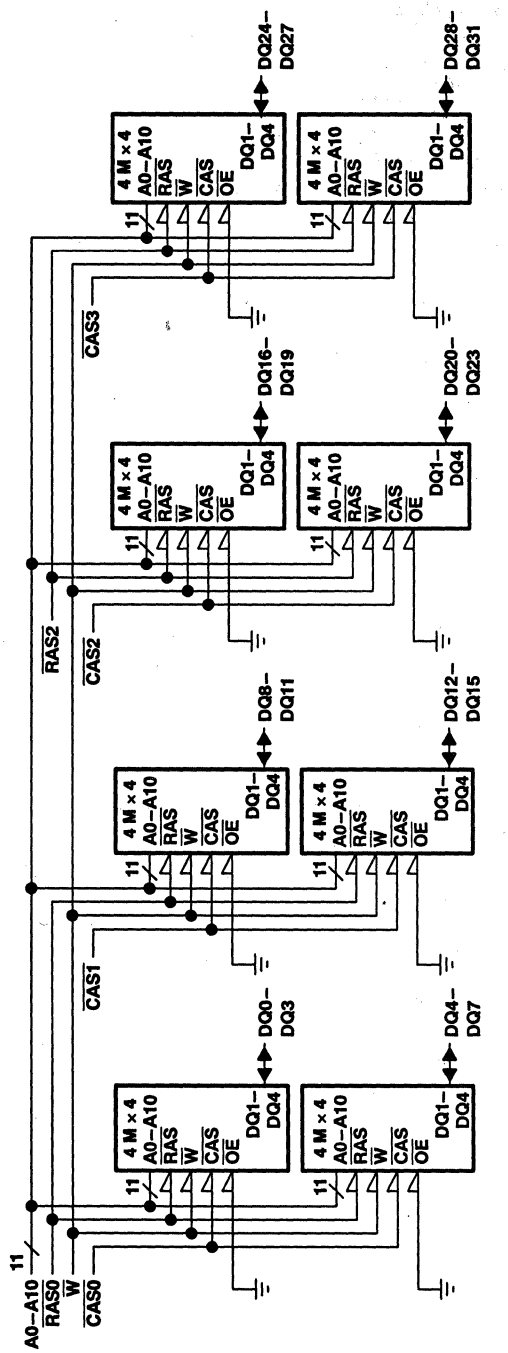
Table 1. Connection Table

DATA BLOCK	$\overline{RAS}x$		$\overline{CAS}x$
	SIDE 1	SIDE 2	
DQ0–DQ7	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ8–DQ15	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ16–DQ23	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ24–DQ31	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$

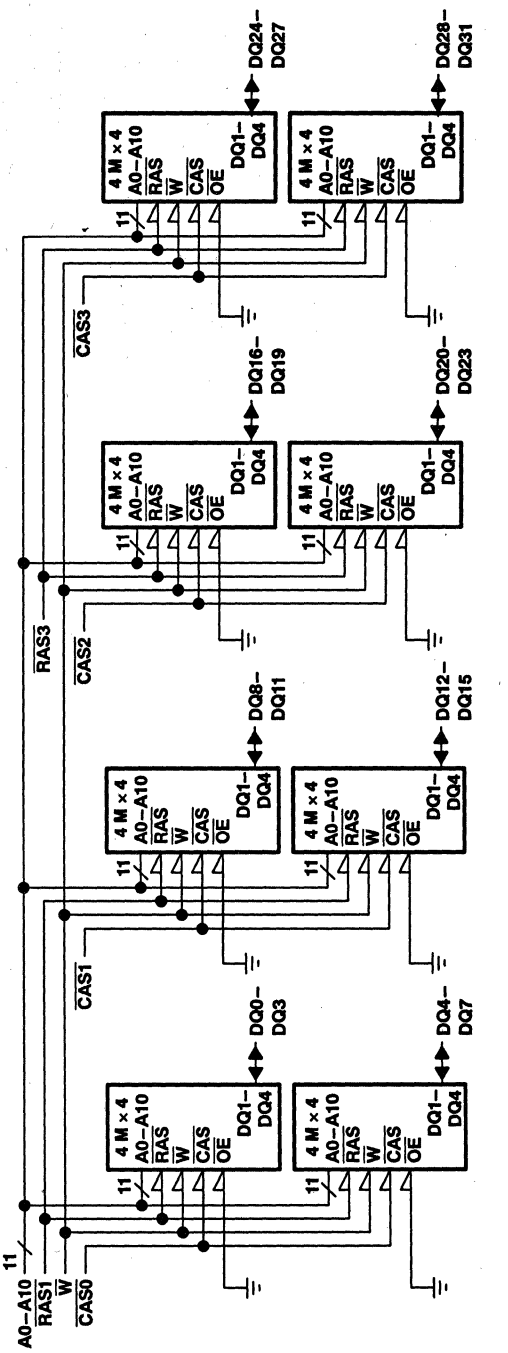
single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM893CBK32: Nickel plate and gold plate over copper
Contact area for TM893CBK32S: Nickel plate and tin-lead over copper

functional block diagram (side 1)



functional block diagram (side 2)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation (TM893CBK32) ..... 16 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'893BBK32-60		'893BBK32-70		'893BBK32-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		±20		±20		±20	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		±20		± 20		± 20	µA
I_{CC1}	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		896		816		736	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		32		32		32	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		16		16		16	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1760		1600		1440	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		576		496		416	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		'893CBK32		UNIT
		MIN	MAX	
$C_{i(A)}$	Input capacitance, A0–A10		80	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs		28	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs		28	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		112	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		14	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'893CBK32-60		'893CBK32-70		'893CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in the low-impedance state	0		0		0		ns
t_{OH}	Output disable from start of $\overline{CAS}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'893CBK32-60		'893CBK32-70		'893CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 7 and 8)	40		45		50		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high (precharge)	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{CAS}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before (precharge) $\overline{CAS}$ low	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns

NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'893CBK32-60		'893CBK32-70		'893CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Hold time, data after $\overline{CAS}$ and $\overline{W}$ low	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low	10		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR refresh only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to assure access time.

- **Organization**
  TM124MBK36B . . . 1 048 576 × 36
  TM248NBK36B . . . 2 097 152 × 36
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-pin Leadless Single In-Line Memory Module (SIMM) for Use With Sockets**
- **TM124MBK36B–Utilizes Eight 4-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages and One 4-Megabit Quad-$\overline{CAS}$ DRAM in a Plastic Small-Outline J-Lead (SOJ) Package**
- **TM248NBK36B–Utilizes Sixteen 4-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Two 4-Megabit Quad-$\overline{CAS}$ DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period**
  16 ms (1024 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines, in Four Blocks**
- **Enhanced Page Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$ ($\overline{CBR}$), $\overline{RAS}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'124MBK36B-60	60 ns	30 ns	15 ns	110 ns
'124MBK36B-70	70 ns	35 ns	18 ns	130 ns
'124MBK36B-80	80 ns	40 ns	20 ns	150 ns
'248NBK36B-60	60 ns	30 ns	15 ns	110 ns
'248NBK36B-70	70 ns	35 ns	18 ns	130 ns
'248NBK36B-80	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range**
  0°C to 70°C
- **Gold-Tabbed Versions Available:†**
  – TM124MBK36B
  – TM248NBK36B
- **Tin-Lead (Solder) Tabbed Versions Available:**
  – TM124MBK36R
  – TM248NBK36R

description

TM124MBK36B

The TM124MBK36B is a dynamic random-access memory (DRAM) organized as four times 1 048 576 × 9 (bit 9 is generally used for parity) in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of eight TMS44400DJ, 1 048 576 × 4-bit DRAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), and one TMS44460DJ, 1 048 576 × 4-bit Quad-$\overline{CAS}$ DRAM in a 24/26-lead plastic small-outline J-lead package (SOJ), mounted on a substrate with decoupling capacitors. Each TMS44400DJ and TMS44460DJ is described in the TMS44400 or TMS44460 data sheet, respectively.

The TM124MBK36B is available in the single-sided BK leadless module for use with sockets.

The TM124MBK36B features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is rated for operation from 0°C to 70°C.

TM248NBK36B

The TM248NBK36B is a DRAM organized as four times 2 097 152 × 9 (bit 9 is generally used for parity) in a 72-pin leadless SIMM. The SIMM is composed of sixteen TMS44400DJ, 1 048 576 × 4-bit DRAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), and two TMS44460DJ, 1 048 576 × 4-bit Quad-$\overline{CAS}$ DRAMs, each in a 24/26-lead plastic small-outline J-lead package (SOJ), mounted on a substrate with decoupling capacitors. Each TMS44400DJ and TMS44460DJ is described in the TMS44400 and TMS44460 data sheet, respectively.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

TM248NBK36B (continued)

The TM124NBK36B is available in the double-sided BK leadless module for use with sockets.

The TM124NBK36B features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is rated for operation from 0°C to 70°C

operation

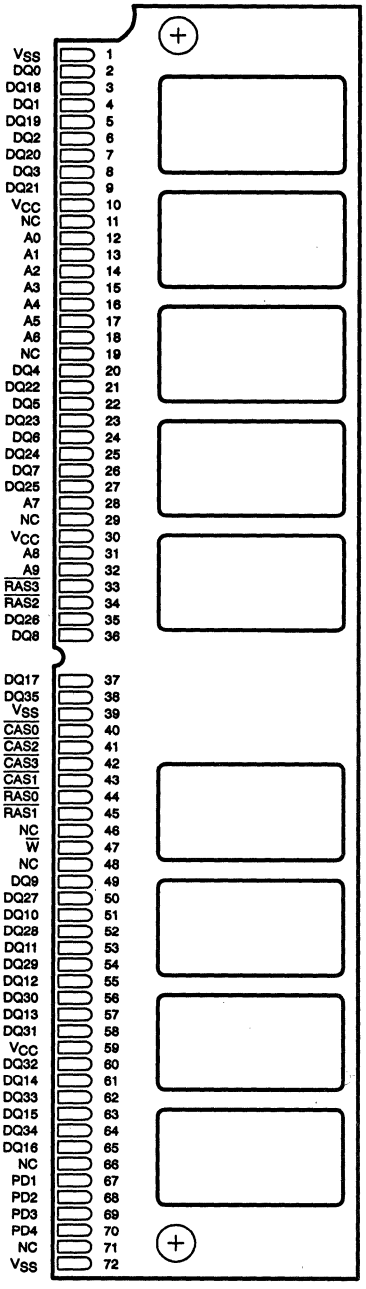
TM124MBK36B

The TM124MBK36B operates as eight TMS44400DJs and one TMS44460DJ connected as shown in the functional block diagram and Table 1. The parity bits are provided by the TMS44460DJ and are controlled by $\overline{RAS2}$. To ensure proper parity bit operation all memory accesses should include a $\overline{RAS2}$ pulse. Refer to the TMS44400 and TMS44460 data sheets for details of operation. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

TM248NBK36B

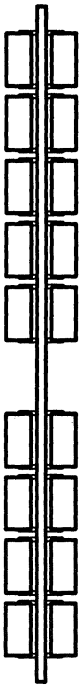
The TM248NBK36B operates as sixteen TMS44400DJs and two TMS44460DJs connected as shown in the functional block diagram and Table 1. The parity bits are provided by the TMS44460DJ and are controlled by $\overline{RAS2}$ on side 1 and $\overline{RAS3}$ on side 2. To ensure proper parity bit operation, all memory accesses should include a $\overline{RAS2}$ or $\overline{RAS3}$ pulse. Refer to the TMS44400 and TMS44460 data sheets for details of operation. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

BK SINGLE IN-LINE MEMORY MODULE
(TOP VIEW)



TM124MBK36B
(SIDE VIEW)

TM248NBK36B
(SIDE VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ35	Data In/Data Out
NC	No Connection
PD1– PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124MBK36B	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248NBK36B	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

Table 1. Connection Table

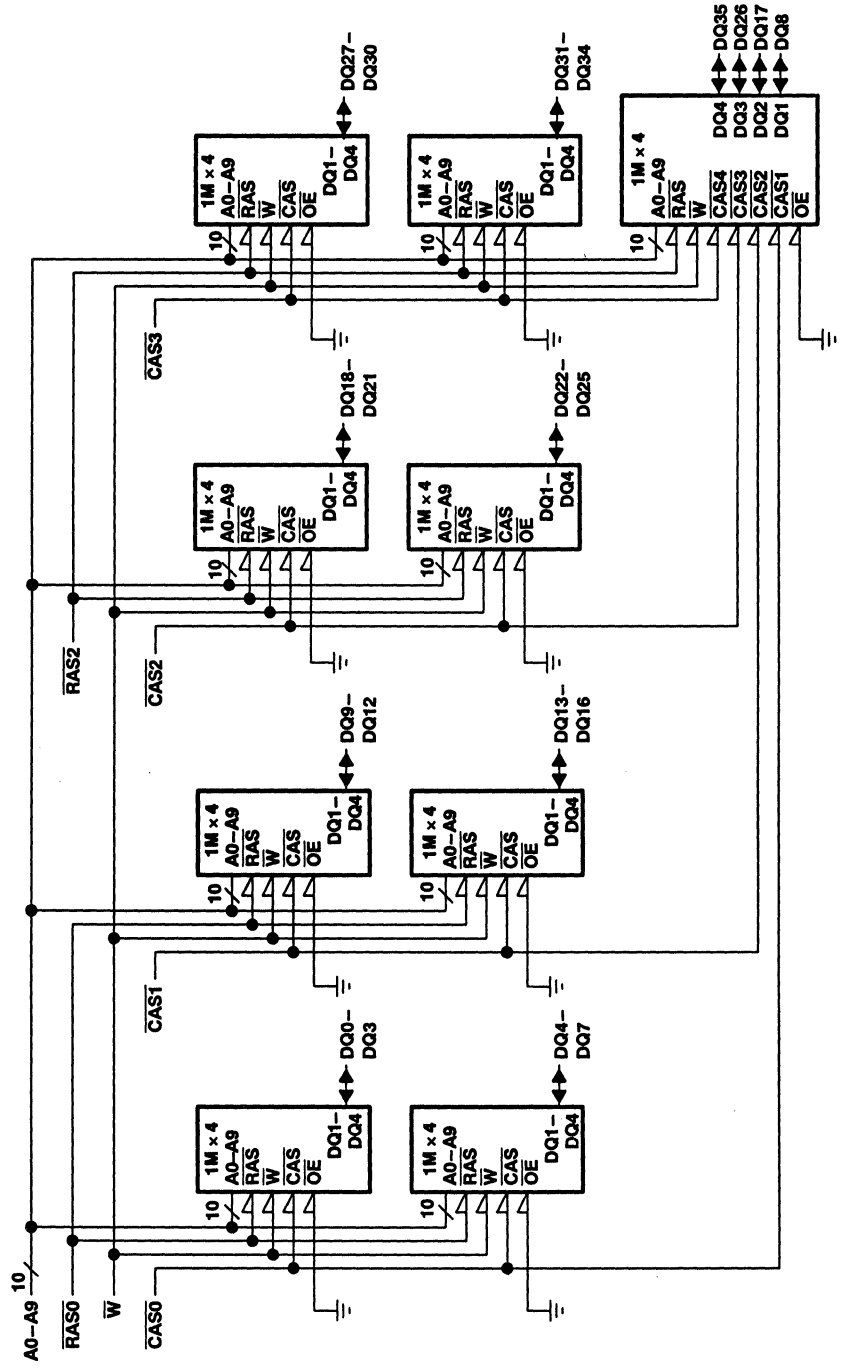
DATA BLOCK	$\overline{RAS}x$		$\overline{CAS}x$
	SIDE 1	SIDE 2†	
DQ0–DQ7	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ8	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS0}$
DQ9–DQ16	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ17	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS1}$
DQ18–DQ25	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ26	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ27–DQ34	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$
DQ35	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$

† Side 2 applies to the TM248NBK36B only.

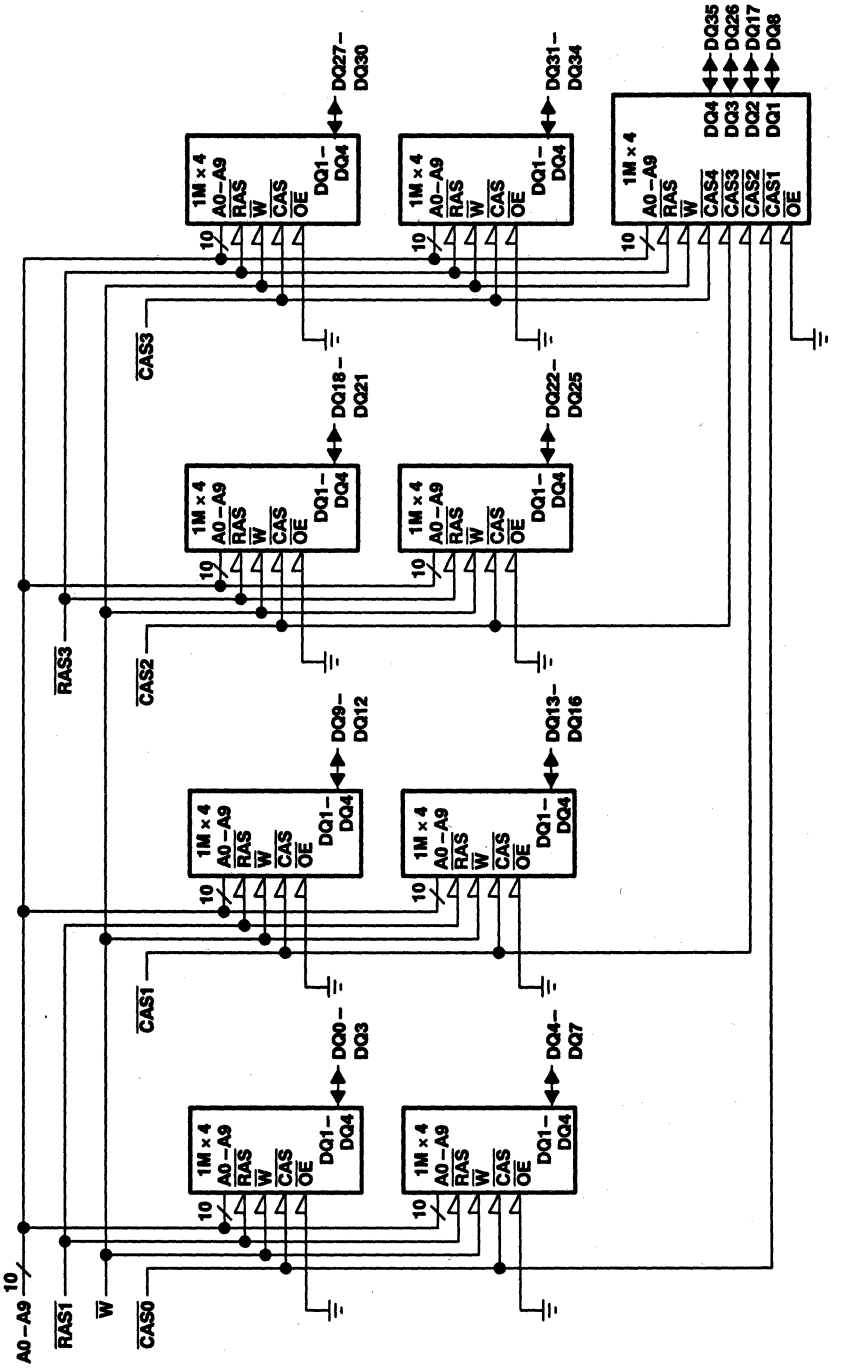
single-in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124MBK36B and TM248NBK36B: Nickel plate and gold plate over copper
Contact area for TM124MBK36R and TM248NBK36R: Nickel plate and tin-lead over copper

functional block diagram (TM124MBK36B and TM248NBK36B, side 1)



functional block diagram (TM248NBK36B, side 2)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... –1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... –1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 9 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124MBK36B-60		'124MBK36B-70		'124MBK36B-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		945		810		720	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		18		18		18	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		9		9		9	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		945		810		720	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		810		720		630	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'248NBK36B-60		'248NBK36B-70		'248NBK36B-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 20		± 20		± 20	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		963		828		738	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		36		36		36	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		18		18		18	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1890		1620		1440	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		828		738		648	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		'124MBK36B		'248NBK36B		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, A0–A9		45		90	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$		35		35	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$		21		42	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		63		126	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		7		14	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124MBK36B-60 '248NBK36B-60		'124MBK36B-70 '248NBK36B-70		'124MBK36B-80 '248NBK36B-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{AA}	Access time from column address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ to output in low impedance	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124MBK36B-60 '248NBK36B-60		'124MBK36B-70 '248NBK36B-70		'124MBK36B-80 '248NBK36B-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{RWC}	Cycle time, read write	130		153		175		ns
t_{PC}	Cycle time, page-mode read or write (see Note 8)	40		45		50		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, write	15		15		15		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (see Note 9)	10		10		10		ns

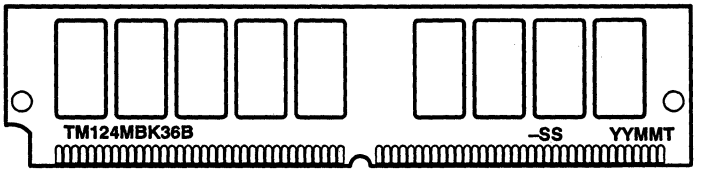
NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ 5 ns.
9. CBR refresh only

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'124MBK36B-60 '248NBK36B-60		'124MBK36B-70 '248NBK36B-70		'124MBK36B-80 '248NBK36B-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{DH}	Hold time, data	10		15		15		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{CLCH}	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high	5		5		5		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 11)	0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 11)	0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{WHR}	Hold time, $\overline{W}$ high (see Note 9)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 9)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 9)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 12)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 12)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 9)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 9. CBR refresh only
10. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. The maximum value is specified only to assure access time.

device symbolization (TM124MBK36B illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed Code

NOTE: Location of symbolization may vary.

SMMS650A – APRIL 1995 – REVISED JUNE 1995

- **Organization**
  TM124MBK36F . . . 1 048 576 × 36
  TM248NBK36F . . . 2 097 152 × 36
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Single-In-Line Memory Module (SIMM) for Use With Socket**
- **TM124MBK36F – Utilizes Two 16-Megabit and One 4-Megabit DRAMs In Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM248NBK36F – Utilizes Four 16-Megabit and Two 4-Megabit DRAMs In Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines In Four Blocks**
- **Enhanced Page-Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR), $\overline{RAS}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'124MBK36F-60	60 ns	30 ns	15 ns	110 ns
'124MBK36F-70	70 ns	35 ns	18 ns	130 ns
'124MBK36F-80	80 ns	40 ns	20 ns	150 ns
'248NBK36F-60	60 ns	30 ns	15 ns	110 ns
'248NBK36F-70	70 ns	35 ns	18 ns	130 ns
'248NBK36F-80	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range: 0°C to 70°C**
- **Gold-Tabbed Versions Available:†**
  - **TM124MBK36F**
  - **TM248NBK36F**
- **Tin-Lead (Solder) Tabbed Versions Available:**
  - **TM124MBK36U**
  - **TM248NBK36U**

description

TM124MBK36F

The TM124MBK36F is a 4-MByte dynamic random-access memory (DRAM) organized as four times 1 048 576 × 9 in a 72-pin single-in-line memory module (SIMM). The SIMM is composed of two TMS418160DZ, 1 048 576 × 16-bit dynamic RAMs, each in a 42-lead plastic small-outline J-lead (SOJ) package and one TMS44460DJ, 1 048 576 × 4-bit DRAM in a 24/26-lead plastic small-outline J-lead (SOJ) package mounted on a substrate with decoupling capacitors. The TMS418160DZ and TMS44460DJ are described in the TMS418160 and TMS44460 data sheets, respectively. The TM124MBK36F SIMM is available in the single-sided BK leadless module for use with sockets.

TM248NBK36F

The TM248NBK36F is an 8-MByte DRAM organized as four times 2 097 152 × 9 in a 72-pin single-in-line memory module (SIMM). The SIMM is composed of four TMS418160DZ, 1 048 576 × 16-bit dynamic RAMs, each in a 42-lead plastic small-outline J-lead (SOJ) package and two TMS44460DJ, 1 048 576 × 4-bit DRAMs, each in a 24/26-lead plastic small-outline (SOJ) package mounted on a substrate with decoupling capacitors. The TMS418160DZ and TMS44460DJ are described in the TMS418160 and TMS44460 data sheets, respectively. The TM248NBK36F SIMM is available in the double-sided BK leadless module for use with sockets.

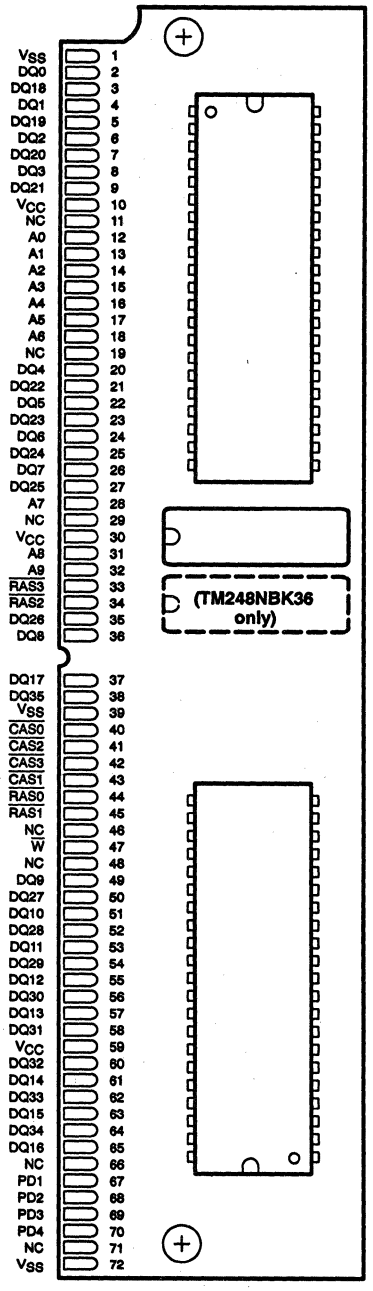
operation

The TM124MBK36F operates as two TMS418160DZs and one TMS44460DJ connected as shown in the functional block diagram and Table 1. The TM248NBK36F operates as four TMS418160DZs and two TMS44460DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

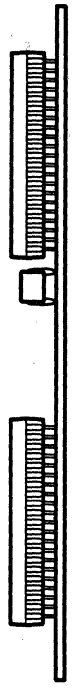
BK SINGLE-IN-LINE MEMORY MODULE

(TOP VIEW)



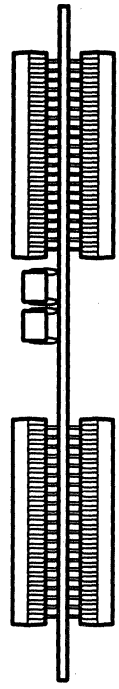
TM124MBK36F

(SIDE VIEW)



TM248NBK36F

(SIDE VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ35	Data In/Data Out
NC	No Connection
PD1– PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124MBK36F	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248NBK36F	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

Table 1. Connection Table

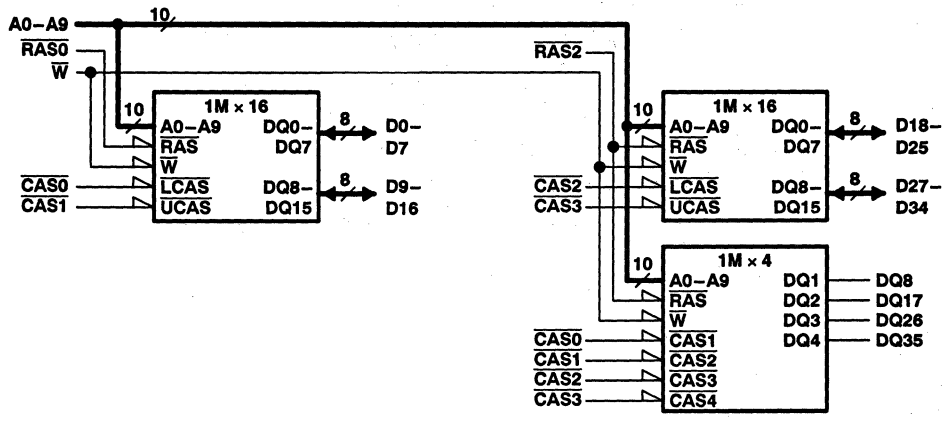
DATA BLOCK	$\overline{RAS}x$		$\overline{CAS}x$
	SIDE 1	SIDE 2†	
DQ0–DQ7	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ8	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS0}$
DQ9–DQ16	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ17	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS1}$
DQ18–DQ25	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ26	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ27–DQ34	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$
DQ35	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$

† Side 2 applies to the TM248NBK36F only.

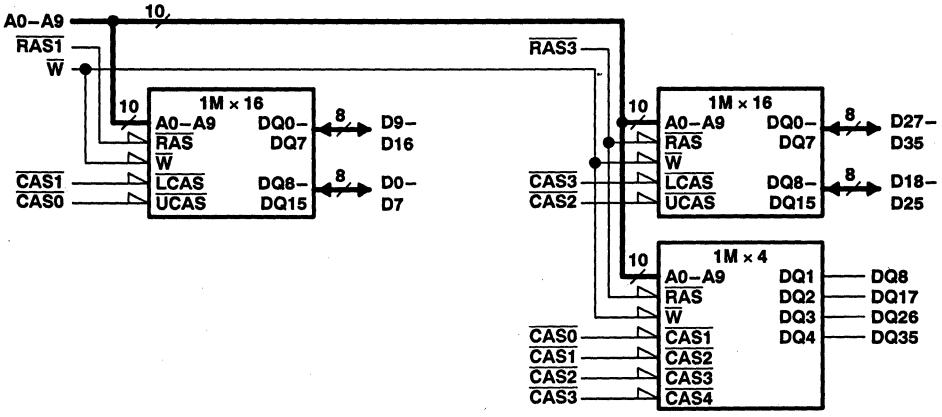
single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124MBK36F and TM248NBK36F: Nickel plate and gold plate over copper
Contact area for TM124MBK36U and TM248NBK36U: Nickel plate and tin/lead over copper

functional block diagram [TM124MBK36F and TM248NBK36F, side 1]



functional block diagram [TM248NBK36F, side 2]



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... – 1 V to 7 V
Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation TM124MBK36F, TM124MBK36U ..... 3 W
TM248NBK36F, TM248NBK36U ..... 6 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124MBK36F-60		'124MBK36F-70		'124MBK36F-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		285		250		220	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		6		6		6	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3		3		3	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		285		250		220	mA
I_{CC4}	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		250		220		190	mA

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)†

PARAMETER		TEST CONDITIONS	'248NBK36F-60		'248NBK36F-70		'248NBK36F-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		391		256		226	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		12		12		12	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		6		6		6	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		570		500		440	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		256		226		196	mA

† For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER			'124MBK36F		'248NBK36F		UNIT
			MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs			15		30	pF
$C_{i(R)}$	Input capacitance, RAS inputs	$\overline{RAS2}$, $\overline{RAS3}$		14		14	pF
		$\overline{RAS0}$, $\overline{RAS1}$		7		7	
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs			14		28	pF
$C_{i(W)}$	Input capacitance, write-enable input			21		42	pF
$C_{o(DQ)}$	Output capacitance on DQ pins			7		14	pF

NOTE 5: Bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124MBK36F-60 '248NBK36F-60		'124MBK36F-70 '248NBK36F-70		'124MBK36F-80 '248NBK36F-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ to output in low-impedance state	0		0		0		ns
t_{OH}	Output disable time from start of $\overline{CAS}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124MBK36F-60 '248NBK36F-60		'124MBK36F-70 '248NBK36F-70		'124MBK36F-80 '248NBK36F-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 7 and 8)	40		45		50		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high (precharge)	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{CAS}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low	10		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns

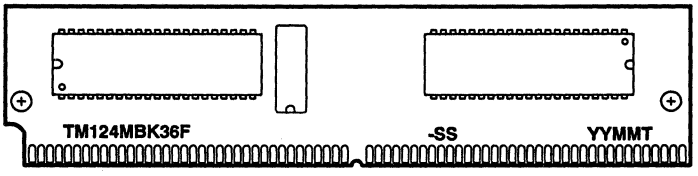
NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'124MBK36F-60 '248NBK36F-60		'124MBK36F-70 '248NBK36F-70		'124MBK36F-80 '248NBK36F-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTE 10: The maximum value is specified only to assure access time.

device symbolization (TM124MBK36F illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE: Location of symbolization may vary.

- **Organization**
  TM124MBK36C . . . 1048576 × 36
  TM248NBK36C . . . 2097152 × 36
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-pin Leadless Single In-Line Memory Module (SIMM)**
- **TM124MBK36C – Utilizes Eight 4-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Two 4-Megabit Quad-$\overline{CAS}$ DRAMs in Plastic SOJ Packages**
- **TM248NBK36C – Utilizes Sixteen 4-Megabit DRAMs in Plastic SOJ Packages and Four 4-Megabit Quad-$\overline{CAS}$ DRAMs in Plastic SOJ Packages**
- **Long Refresh Period**
  16 ms (1024 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines, In Four Blocks**
- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR), $\overline{RAS}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'124MBK36C-60	60 ns	30 ns	15 ns	110 ns
'124MBK36C-70	70 ns	35 ns	18 ns	130 ns
'124MBK36C-80	80 ns	40 ns	20 ns	150 ns
'248NBK36C-60	60 ns	30 ns	15 ns	110 ns
'248NBK36C-70	70 ns	35 ns	18 ns	130 ns
'248NBK36C-80	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air-Temperature Range**
  0°C to 70°C
- **Gold-Tabbed Versions Available:†**
  - **TM124MBK36C**
  - **TM248NBK36C**
- **Tin-Lead (Solder) Tabbed Versions**
  - **TM124MBK36S**
  - **TM248NBK36S**

description

TM124MBK36C

The TM124MBK36C is a dynamic random-access memory (DRAM) organized as four times 1048576 × 9 (bit 9 is generally used for parity) in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of eight TMS44400DJ, 1 048 576 × 4-bit DRAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), and two TMS44460DJ, 1048576 × 4-bit Quad-$\overline{CAS}$ DRAMs, in 24/26-lead plastic SOJs mounted on a substrate with decoupling capacitors. Each TMS44400DJ and TMS44460DJ is described in the TMS44400 and TMS44460 data sheets, respectively.

The TM124MBK36C is available in the single-sided BK leadless module for use with sockets.

The TM124MBK36C features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is characterized for operation from 0°C to 70°C.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

TM248NBK36C

The TM248NBK36C is a DRAM organized as four times 2 097 152 × 9 (bit 9 is generally used for parity) in a 72-pin leadless SIMM) The SIMM is composed of sixteen TMS44400DJ, 1048576 × 4-bit DRAMs, each in 20/26-lead plastic SOJs, and four TMS44460DJ, 1 048 576 × 4-bit Quad-$\overline{CAS}$ DRAMs, in 24/26-lead plastic SOJs mounted on a substrate with decoupling capacitors. Each TMS44400DJ and TMS44460DJ is described in the TMS44400 or TMS44460 data sheet, respectively.

The TM248NBK36C is available in the double-sided BK leadless module for use with sockets.

The TM248NBK36C features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is rated for operation from 0°C to 70°C.

operation

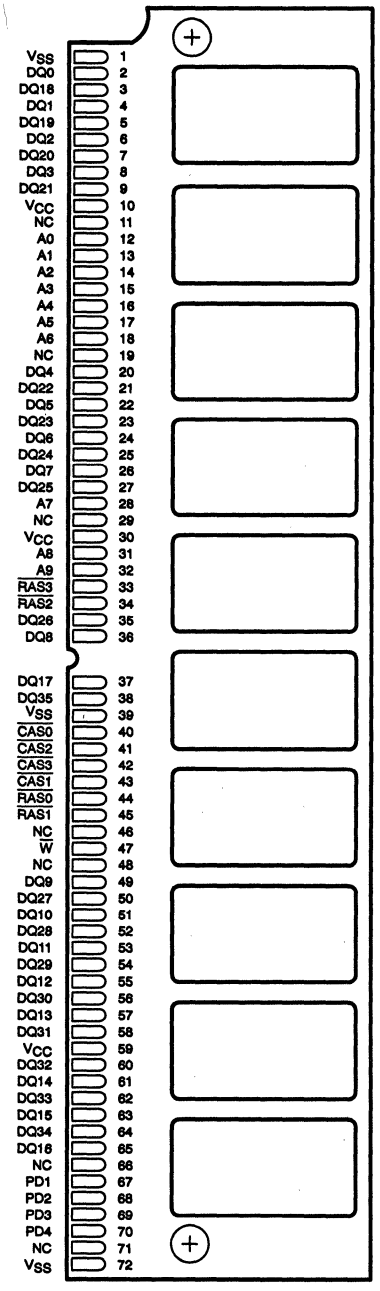
TM124MBK36C

The TM124MBK36C operates as eight TMS44400DJs and two TMS44460DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

TM248NBK36C

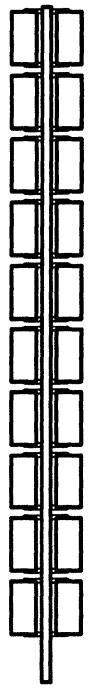
The TM248NBK36C operates as sixteen TMS44400DJs and four TMS44460DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

BK SINGLE IN-LINE MODULE
(TOP VIEW)



TM124MBK36C
(SIDE VIEW)

TM248NBK36C
(SIDE VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ35	Data In/Data Out
NC	No Connection
PD1– PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124MBK36C	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248NBK36C	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

Table 1. Connection Table

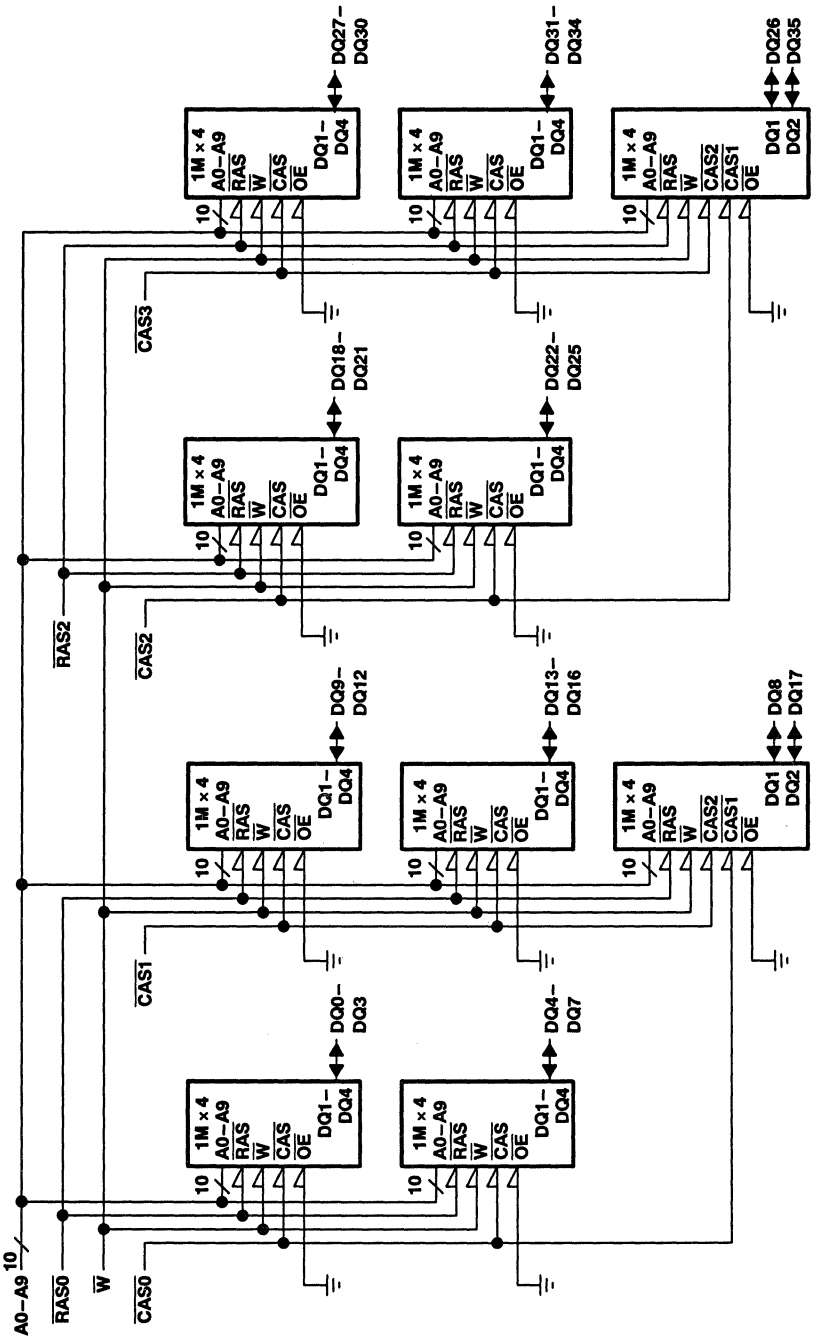
DATA BLOCK	$\overline{RAS}x$		$\overline{CAS}x$
	SIDE 1	SIDE 2†	
DQ0–DQ7	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ8	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ9–DQ16	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ17	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ18–DQ25	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ26	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ27–DQ34	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$
DQ35	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$

† Side 2 applies to the TM248NBK36C only.

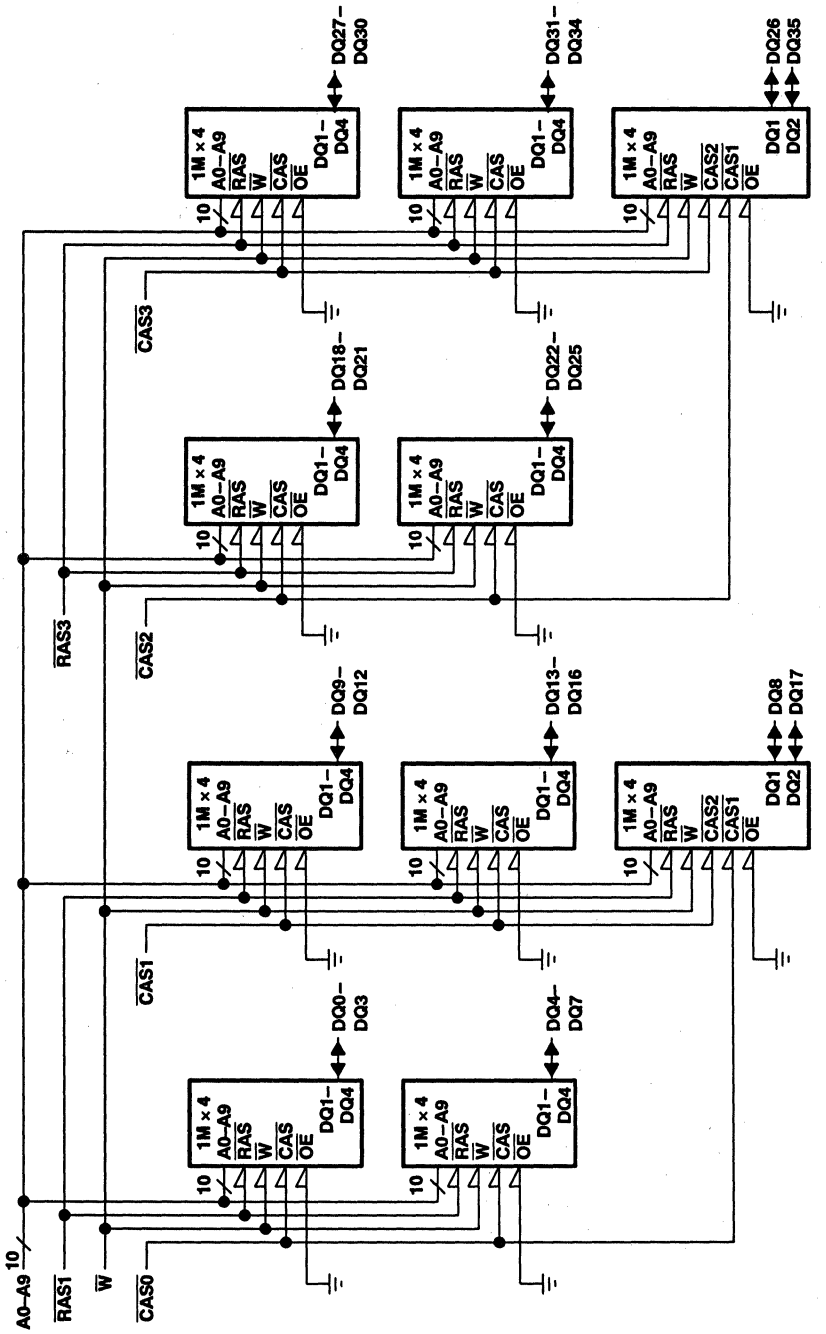
single-in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124MBK36C and TM248NBK36C: Nickel plate and gold plate over copper
Contact area for TM124MBK36S and TM248NBK36S: Nickel plate and tin-lead over copper

functional block diagram (for TM124MBK36C and TM248NBK36C, Side 1)



functional block diagram (for TM248NBK36C, Side 2)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on V_{CC} (see Note 1) ..... –1 V to 7 V
Supply voltage range on any pin (see Note 1) ..... –1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 10 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124MBK36C-60		'124MBK36C-70		'124MBK36C-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		1050		900		800	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), after 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		20		20		20	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), after 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		10		10		10	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1050		900		800	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		900		800		700	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'248NBK36C-60		'248NBK36C-70		'248NBK36C-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 20		± 20		± 20	μA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	μA
I_{CC1}	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		1070		920		820	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), after 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		40		40		40	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), after 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		20		20		20	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		2100		1800		1600	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		920		820		720	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		'124MBK36C		'248NBK36C		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, A0–A9		50		100	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs		35		35	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs		21		42	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		70		140	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		7		14	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124MBK36C-60 '248NBK36C-60		'124MBK36C-70 '248NBK36C-70		'124MBK36C-80 '248NBK36C-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{AA}	Access time from column-address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124MBK36C-60 '248NBK36C-60		'124MBK36C-70 '248NBK36C-70		'124MBK36C-80 '248NBK36C-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{RWC}	Cycle time, read-write	130		153		175		ns
t_{PC}	Cycle time, page-mode read or write (see Note 8)	40		45		50		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, write	15		15		15		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{DH}	Hold time, data	10		15		15		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 99)	50		55		60		ns
t_{CLCH}	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high	5		5		5		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 10)	0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 10)	0		0		0		ns

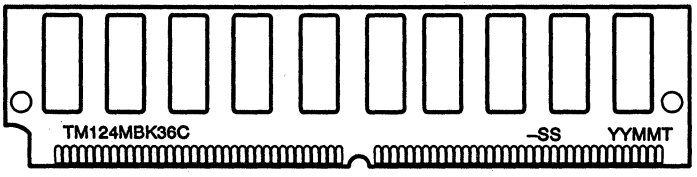
NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ 5 ns.
9. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'124MBK36C-60 '248NBK36C-60		'124MBK36C-70 '248NBK36C-70		'124MBK36C-80 '248NBK36C-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WCH}	Hold time, write after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{WHR}	Hold time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 11)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 11)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR refresh only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 9. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. The maximum value is specified only to assure access time.

device symbolization (TM124MBK36C illustrated)



YY = **Year Code**
MM = **Month Code**
T = **Assembly Site Code**
–SS = **Speed Code**

NOTE: Location of symbolization may vary.

TM124MBK36G, TM124MBK36V 1048576 BY 36-BIT DYNAMIC RAM MODULE
TM248NBK36G, TM248NBK36V 2097152 BY 36-BIT DYNAMIC RAM MODULE

SMMS651A – MAY 1995 – REVISED JUNE 1995

- **Organization**
  TM124MBK36G . . . 1 048 576 × 36
  TM248NBK36G . . . 2 097 152 × 36
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Single-In-Line Memory Module (SIMM) for Use With Socket**
- **TM124MBK36G – Utilizes Two 16-Megabit and Two 4-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM248NBK36G – Utilizes Four 16-Megabit and Four 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period**
  16 ms (1024 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines in Four Blocks**
- **Enhanced Page-Mode Operation With $\overline{CAS}$x-Before-$\overline{RAS}$ (CBR), $\overline{RAS}$x-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'124MBK36G-60	60 ns	30 ns	15 ns	110 ns
'124MBK36G-70	70 ns	35 ns	18 ns	130 ns
'124MBK36G-80	80 ns	40 ns	20 ns	150 ns
'248NBK36G-60	60 ns	30 ns	15 ns	110 ns
'248NBK36G-70	70 ns	35 ns	18 ns	130 ns
'248NBK36G-80	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range**
  0°C to 70°C
- **Gold-Tabbed Versions Available:†**
  TM124MBK36G
  TM248NBK36G
- **Tin-Lead (Solder) Tabbed Versions Available:**
  TM124MBK36V
  TM248NBK36V

description

TM124MBK36G

The TM124MBK36G is a 4M-byte dynamic random-access memory (DRAM) organized as four times 1 048 576 × 9 in a 72-pin SIMM. The SIMM is composed of two TMS418160DZ, 1 048 576 × 16-bit DRAMs, each in a 42-lead plastic SOJ package and two TMS44460DJ, 1 048 576 × 4-bit DRAMs, in a 24/26-lead plastic SOJ package mounted on a substrate with decoupling capacitors. The TMS418160DZ and TMS44460DJ are described in the TMS418160 and TMS44460 data sheets respectively. The TM124MBK36G SIMM is available in the single-sided BK leadless module for use with sockets.

TM248NBK36G

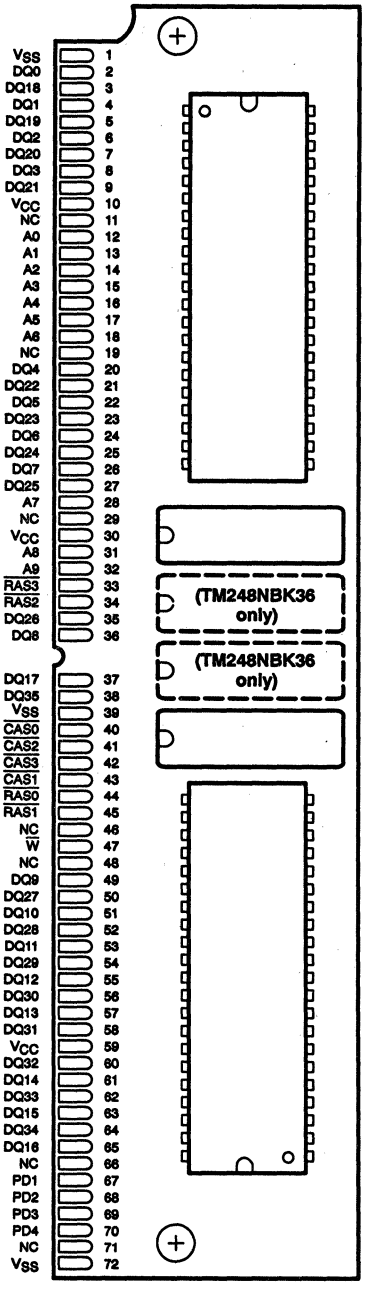
The TM248NBK36G is an 8M-byte DRAM organized as four times 2 097 152 × 9 in a 72-pin SIMM. The SIMM is composed of four TMS418160DZ, 1 048 576 × 16-bit DRAMs, each in a 42-lead plastic SOJ package and four TMS44460DJ, 1 048 576 × 4-bit DRAMs, each in a 24/26-lead plastic SOJ package mounted on a substrate with decoupling capacitors. The TMS418160DZ and TMS44460DJ are described in the TMS418160 and TMS44460 data sheets, respectively. The TM248NBK36G SIMM is available in the double-sided BK leadless module for use with sockets.

operation

The TM124MBK36G operates as two TMS418160DZs and two TMS44460DJs connected as shown in the functional block diagram and Table 1. The TM248NBK36G operates as four TMS418160DZs and four TMS44460DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early-write cycles to prevent contention on D and Q.

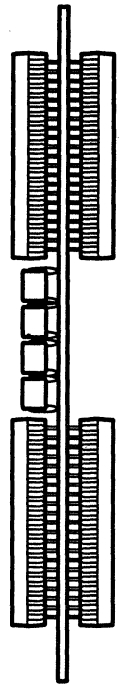
† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

BK SINGLE-IN-LINE MEMORY MODULE†
(TOP VIEW)



TM124MBK36G
(SIDE VIEW)

TM248NBK36G
(SIDE VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ35	Data In/Data Out
NC	No Connection
PD1– PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124MBK36G	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248NBK36G	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

† The packages shown here are not drawn to scale.

Table 1. Connection Table

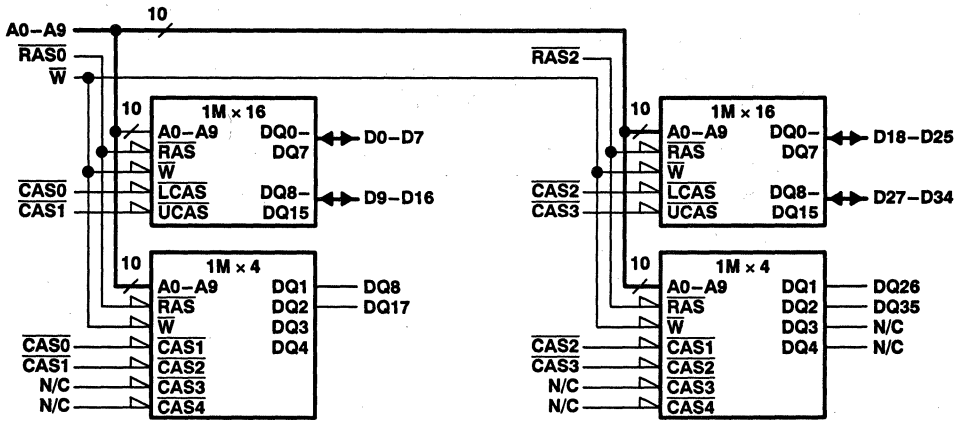
DATA BLOCK	$\overline{RAS}x$		$\overline{CAS}x$
	SIDE 1	SIDE 2†	
DQ0–DQ7	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ8	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ9–DQ16	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ17	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ18–DQ25	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ26	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ27–DQ34	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$
DQ35	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$

† Side 2 applies to the TM248NBK36G only.

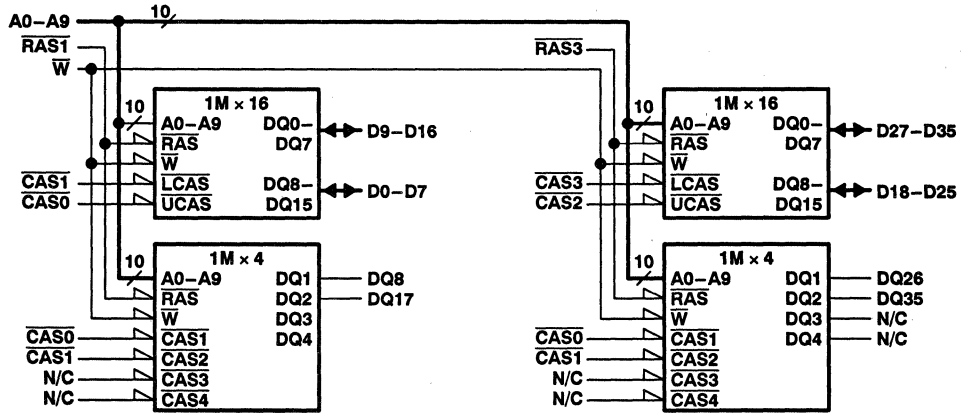
single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124MBK36G and TM248NBK36G: Nickel plate and gold plate over copper
Contact area for TM124MBK36V and TM248NBK36V: Nickel plate and tin/lead over copper

functional block diagram [TM124MBK36G and TM248NBK36G, side 1]



functional block diagram [TM248NBK36G, side 2]



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... – 1 V to 7 V
Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation TM124MBK36G, TM124MBK36V ..... 4 W
TM248NBK36G, TM248NBK36V ..... 8 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124MBK36G-60		'124MBK36G-70		'124MBK36G-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$x high		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		390		340		300	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$x and $\overline{CAS}$x high		8		8		8	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$x and $\overline{CAS}$x high		4		4		4	mA
I_{CC3}	Average refresh current ($\overline{RAS}$x only or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$x cycling, $\overline{CAS}$x high ($\overline{RAS}$x only), $\overline{RAS}$x low after $\overline{CAS}$x low (CBR)		390		340		300	mA
I_{CC4}	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$x low, $\overline{CAS}$x cycling		320		280		240	mA

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)†

PARAMETER		TEST CONDITIONS	'248NBK36G-60		'248NBK36G-70		'248NBK36G-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		398		348		308	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		16		16		16	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		8		8		8	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		780		680		600	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		328		288		248	mA

† For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		'124MBK36G		'248NBK36G		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		20		40	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs		14		14	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs		14		28	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		28		56	pF
$C_{O(DQ)}$	Output capacitance on DQ pins		7		14	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124MBK36G-60 '248NBK36G-60		'124MBK36G-70 '248NBK36G-70		'124MBK36G-80 '248NBK36G-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ to output in low-impedance state	0		0		0		ns
t_{OH}	Output disable time from start of $\overline{CAS}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124MBK36G-60 '248NBK36G-60		'124MBK36G-70 '248NBK36G-70		'124MBK36G-80 '248NBK36G-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 7 and 8)	40		45		50		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high (precharge)	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{CAS}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low	10		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns

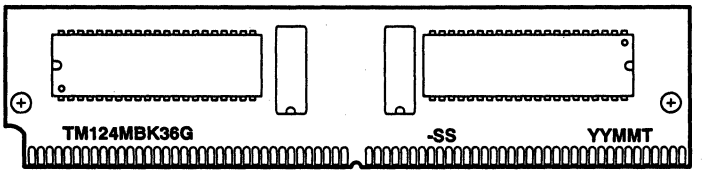
NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124MBK36G-60 '248NBK36G-60		'124MBK36G-70 '248NBK36G-70		'124MBK36G-80 '248NBK36G-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTE 10: The maximum value is specified only to assure access time.

device symbolization (TM124MBK36G illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE: Location of symbolization may vary.

- **Organization . . . 4 194 304 × 36**
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Single-In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes Eight 16-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Four 4-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period 32 ms (2048 Cycles)†**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines in Four Blocks**
- **Separate $\overline{RAS}$ Control for Eighteen Data-In and Data-Out Lines in Two Blocks**
- **3-State Output**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
'497MBK36A-60	60 ns	15 ns	30 ns	110 ns
'497MBK36A-70	70 ns	18 ns	35 ns	130 ns
'497MBK36A-80	80 ns	20 ns	40 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Presence Detect**
- **Gold-Tabbed Version Available:‡ TM497MBK36A**
- **Tin-Lead (Solder) Tabbed Version Available: TM497MBK36Q**

description

The TM497MBK36A is a 16M-byte dynamic random-access memory (DRAM) organized as four times 4194304 × 9 (bit 9 is generally used for parity) in a 72-pin leadless single-in-line memory module (SIMM). The SIMM is composed of eight TMS417400DJ, 4194304 × 4-bit DRAMs, each in 24/26-lead plastic SOJ packages, and four TMS44100DJ, 4194304 × 1-bit DRAMs, each in 20/26-lead plastic SOJ packages mounted on a substrate with decoupling capacitors. Each TMS417400DJ and TMS44100DJ is described in the TMS417400 and TMS44100 data sheets (respectively).

The TM497MBK36A is available in a double-sided BK leadless module for use with sockets. The TM497MBK36A features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is characterized for operation from 0°C to 70°C.

operation

The TM497MBK36A operates as eight TMS417400DJs and four TMS44100DJs connected as shown in the functional block diagram and Table 1. Refer to the TMS417400 and TMS44100 data sheets for details of operation. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

refresh

The refresh period is extended to 32 ms and, during this period, each of the 2048 rows must be strobed with $\overline{RAS}$ in order to retain data. Address line A10 must be used as most significant refresh address line (lowest frequency) to assure correct refresh for both TMS417400 and TMS44100. A0–A9 address lines must be refreshed every 16 ms as required by the TMS44100 DRAM. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

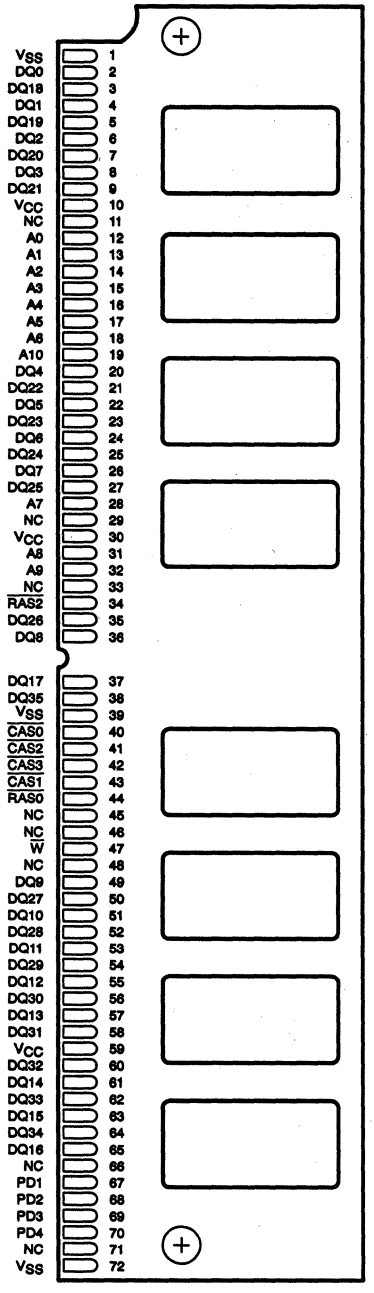
power up

To achieve proper operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh [$\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ (CBR)] cycle.

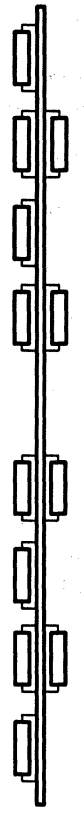
† A0–A9 address lines must be refreshed every 16 ms.
‡ Part numbers in this data sheet refer only to the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

BK SINGLE-IN-LINE PACKAGE

(TOP VIEW)



(SIDE VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ7, DQ9–DQ16, DQ18–DQ25, DQ27–DQ34	Data In/Data Out
DQ8, DQ17, DQ26, DQ35	Parity
NC	No Connection
PD1–PD4	Presence Detects
$\overline{RAS0}$, $\overline{RAS2}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM497MBK36A	80 ns	V_{SS}	NC	NC	V_{SS}
	70 ns	V_{SS}	NC	V_{SS}	NC
	60 ns	V_{SS}	NC	NC	NC

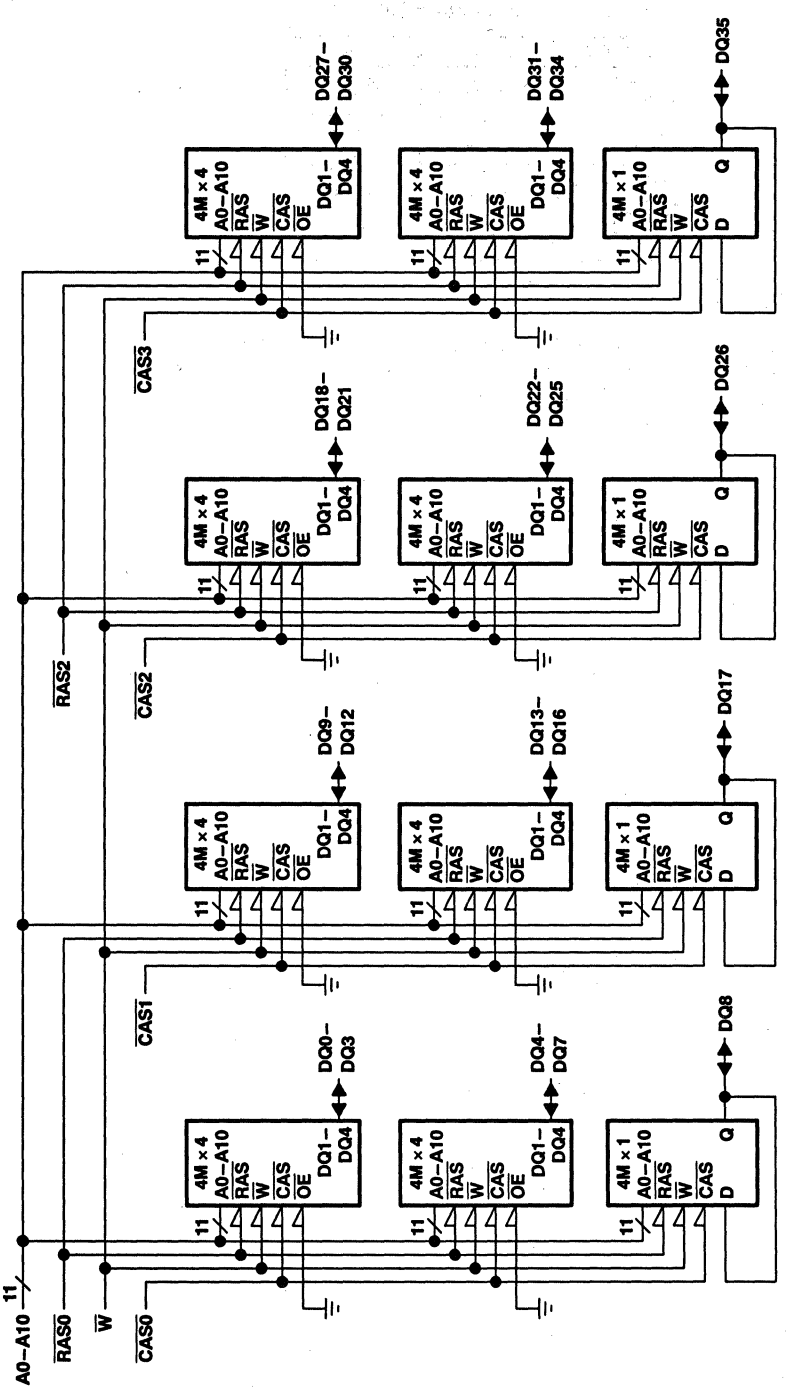
Table 1. Connection Table

DATA BLOCK	$\overline{RAS}$x	$\overline{CAS}$x
DQ0–DQ7 DQ8	$\overline{RAS0}$	$\overline{CAS0}$
DQ9–DQ16 DQ17	$\overline{RAS0}$	$\overline{CAS1}$
DQ18–DQ25 DQ26	$\overline{RAS2}$	$\overline{CAS2}$
DQ27–DQ34 DQ35	$\overline{RAS2}$	$\overline{CAS3}$

single-in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM497MBK36A: Nickel plate and gold plate over copper
Contact area for TM497MBK36Q: Nickel plate and tin-lead over copper

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –1 V to 7 V
Voltage range on any pin (see Note 1) ..... –1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 12 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'497MBK36A-60		'497MBK36A-70		'497MBK36A-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 120		± 120		± 120	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		1300		1160		1040	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		24		24		24	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		12		12		12	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1300		1160		1040	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, $\overline{RAS}$ low, t_{PC} = MIN $\overline{CAS}$ cycling		920		800		680	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

	PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			60	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs			21	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs			42	pF
$C_{i(W)}$	Input capacitance, write-enable input			84	pF
C_o	Output capacitance	DQ pins		7	pF
		Parity pins		12	

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	'497MBK36A-60		'497MBK36A-70		'497MBK36A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low-impedance state	0		0		0		ns
t_{OH}	Output disable time, start of $\overline{CAS}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'497MBK36A-60		'497MBK36A-70		'497MBK36A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 7 and 8)	40		45		50		ns
t_{RASP}	Pulse duration, page-mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage-mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{CAS}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns

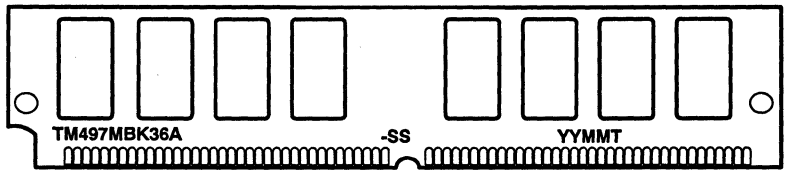
NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'497MBK36A-60		'497MBK36A-70		'497MBK36A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	15		15		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low	15		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low	10		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to assure access time.

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE: Location of symbolization may vary.

- **Organization**
  TM497MBM36A . . . 4194304 × 36
  TM893NBM36A . . . 8388608 × 36
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Leadless Single-In-Line Memory Module (SIMM) for Use With Sockets**
- **TM497MBM36A – Utilizes Eight 16-Megabit and Four 4-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM893NBM36A – Utilizes Sixteen 16-Megabit and Eight 4-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period**
  32 ms (2048 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines in Four Blocks**
- **Enhanced Page-Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ ($\overline{CBR}$), $\overline{RAS}$-Only, and Hidden Refresh**
- **Present Detect**
- **Operating Free-Air-Temperature Range**
  0°C to 70°C
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'497MBM36A-60	60 ns	30 ns	15 ns	110 ns
'497MBM36A-70	70 ns	35 ns	18 ns	130 ns
'497MBM36A-80	80 ns	40 ns	20 ns	150 ns
'893NBM36A-60	60 ns	30 ns	15 ns	110 ns
'893NBM36A-70	70 ns	35 ns	18 ns	130 ns
'893NBM36A-80	80 ns	40 ns	20 ns	150 ns

- **Gold-Tabbed Versions Available:†**
  TM497MBM36A
  TM893NBM36A
- **Tin-Lead (Solder) Tabbed Versions Available:**
  TM497MBM36Q
  TM893NBM36Q

description

TM497MBM36A

The TM497MBM36A is a 16-megabyte dynamic random-access memory (DRAM) organized as four times 4194304 × 9 (bit 9 is generally used for parity) in a 72-pin, leadless single-in-line memory module (SIMM). The SIMM is composed of eight TMS417400DJ, 4194304 × 4-bit DRAMs, each in 24/26-lead plastic small-outline J-lead (SOJ) packages and four TMS44100DJ, 4194304 × 1-bit DRAMs, each in 20/26-lead plastic small-outline J-lead (SOJ) packages mounted on a substrate with decoupling capacitors. The TMS417400DJ and TMS44100DJ are described in the TMS417400 and TMS44100 data sheets, respectively. The TM497MBM36A SIMM is available in the single-sided, BM leadless module for use with sockets.

TM893NBM36A

The TM893NBM36A is a 32-megabyte DRAM organized as four times 8388608 × 9 (bit 9 is generally used for parity) in a 72-pin, leadless single-in-line memory module (SIMM). The SIMM is composed of sixteen TMS417400DJ, 4194304 × 4-bit DRAMs, each in 24/26-lead plastic small-outline J-lead (SOJ) packages and eight TMS44100DJ, 4194304 × 1-bit DRAMs, each in 20/26-lead plastic small-outline J-lead (SOJ) packages mounted on a substrate with decoupling capacitors. The TMS417400DJ and TMS44100DJ are described in the TMS417400 and TMS44100 data sheets, respectively. The TM893NBM36A SIMM is available in the double-sided, BM leadless module for use with sockets.

operation

TM497MBM36A

The TM497MBM36A operates as eight TMS417400DJs and four TMS44100DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early-write cycles to prevent contention on D and Q.

† Part numbers in this data sheet refer only to the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

TM893NBM36A

The TM893NBM36A operates as sixteen TMS417400DJs and eight TMS44100DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early-write cycles to prevent contention on D and Q.

refresh

The refresh period is extended to 32 ms and, during this period, each of the 2048 rows must be strobed with $\overline{RAS}$ in order to retain data. Address line A10 must be used as the most significant refresh address line (lowest frequency) to ensure correct refresh for both TMS417400 and TMS44100. Address lines A0–A9 must be refreshed every 16 ms as required by the TMS44100 DRAM. To conserve power, $\overline{CAS}$ can remain high during the refresh sequence.

power up

To achieve proper operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or CBR-refresh) cycle.

Table 1. Connection Table

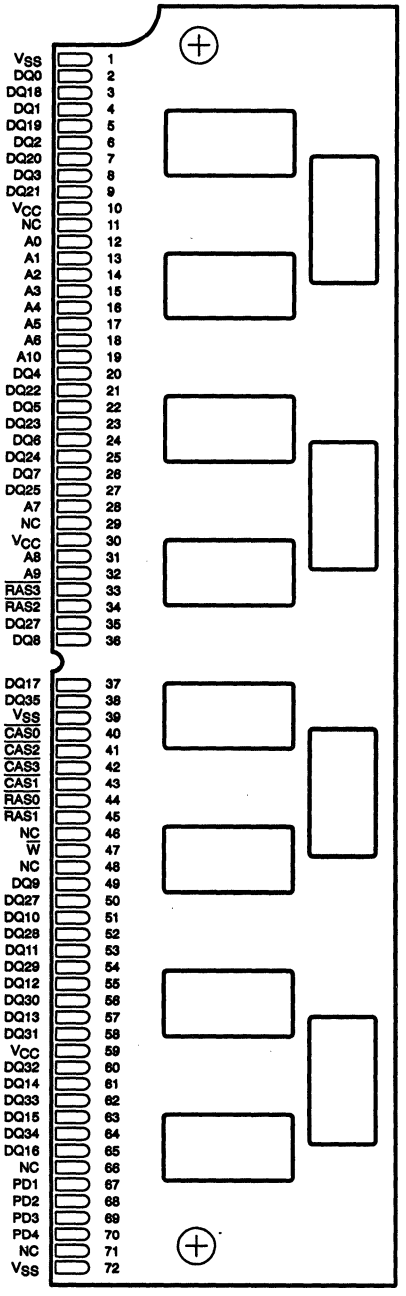
DATA BLOCK	$\overline{RASX}$		$\overline{CASX}$
	SIDE 1	SIDE 2†	
DQ0–DQ7 DQ8	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ9–DQ16 DQ17	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ18–DQ25 DQ26	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ27–DQ34 DQ35	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$

† Side 2 applies to the TM893NBM36A.

single-in-line-memory module and components

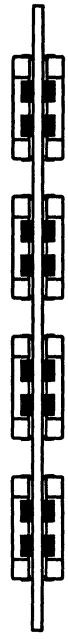
PC substrate: 1, 27 ± 0,1 mm (0.05 inch) nominal thickness; inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM497MBM36A and TM893NBM36A: Nickel plate and gold plate over copper
Contact area for TM497MBM36Q and TM893NBM36Q: Nickel plate and tin/lead over copper

BM SINGLE-IN-LINE PACKAGE
(TOP VIEW)



TM497MBM36A
(SIDE VIEW)

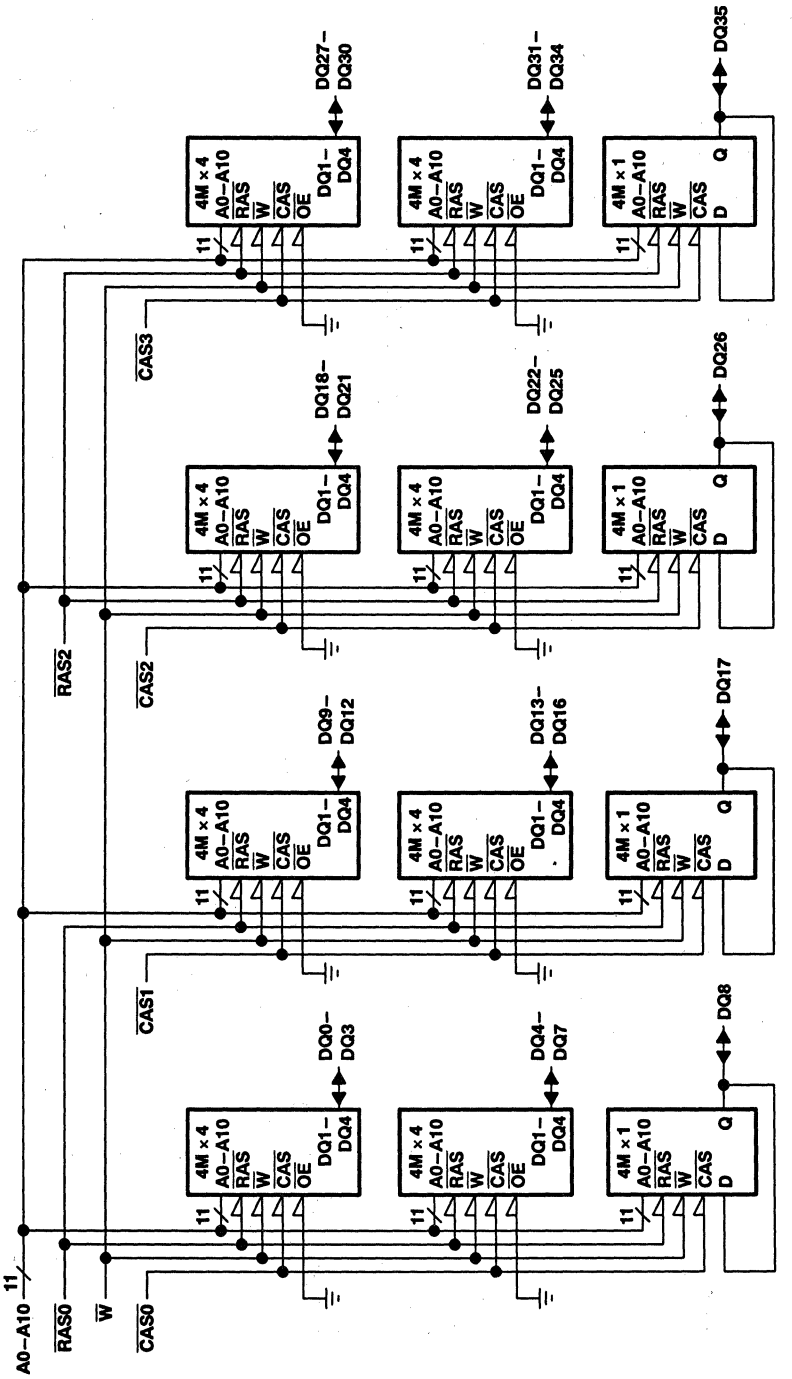
TM893NBM36A
(SIDE VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ35	Data In/Data Out
NC	No Connection
PD1–PD5	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM497MBM36A	80 ns	V_{SS}	NC	NC	V_{SS}
	70 ns	V_{SS}	NC	V_{SS}	NC
	60 ns	V_{SS}	NC	NC	NC
TM893NBM36A	80 ns	NC	V_{SS}	NC	V_{SS}
	70 ns	NC	V_{SS}	V_{SS}	NC
	60 ns	NC	V_{SS}	NC	NC

functional block diagram (TM497MBM36A and TM893NBM36A, side 1)



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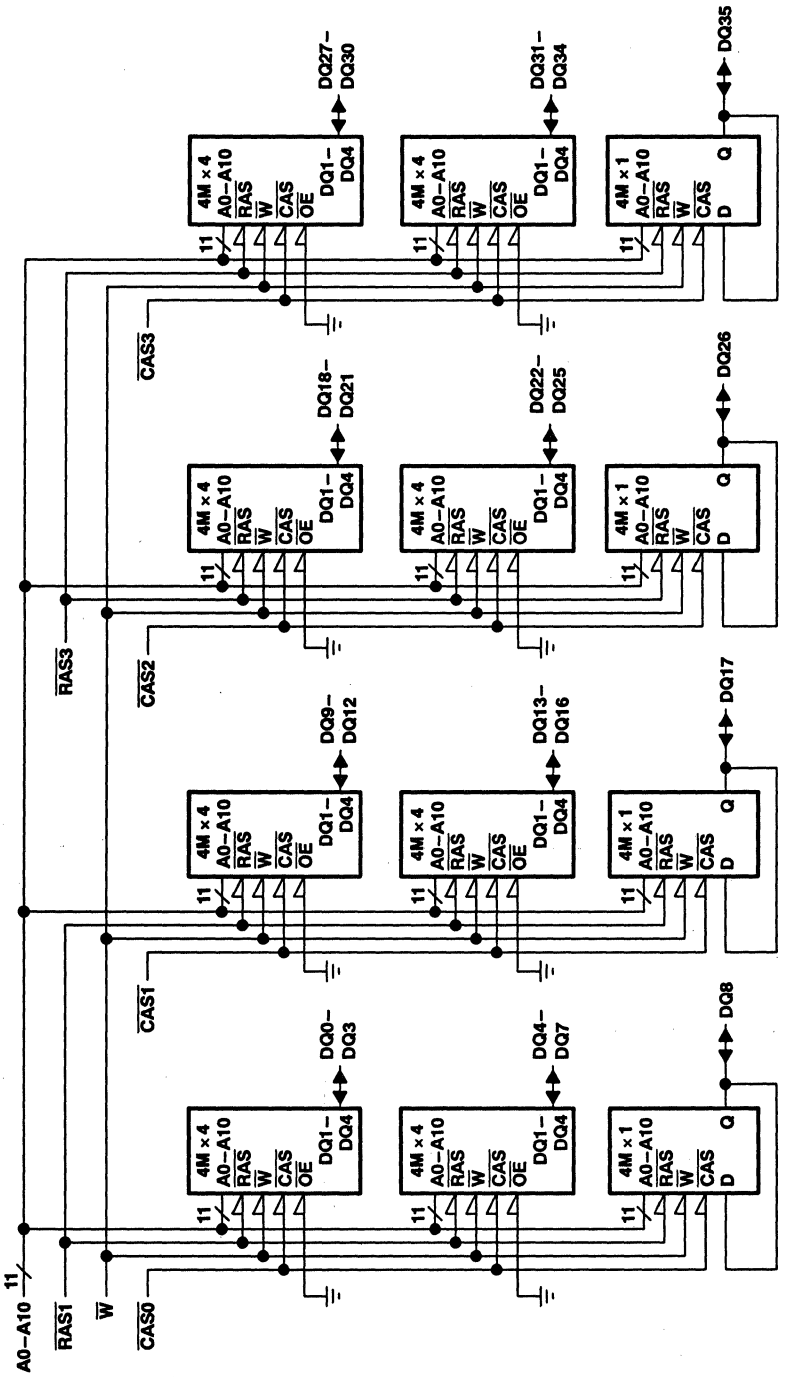
functional block diagram (TM893NBM36A, side 2)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –1 V to 7 V
Voltage range on any pin (see Note 1) ..... –1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation: TM497MBM36A, TM497MBM36Q ..... 12 W
TM893NBM36A, TM893NBM36Q ..... 24 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	'497MBM36A-60		'497MBM36A-70		'497MBM36A-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		1300		1160		1040	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		24		24		24	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		12		12		12	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only refresh); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1300		1160		1040	mA
I_{CC4}	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		920		800		680	mA

‡ For test conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†	'893NBM36A-60		'893NBM36A-70		'893NBM36A-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 20		± 20		± 20	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read- or write-cycle current (one $\overline{RAS}$ active, see Note 3)	V_{CC} = 5.5 V, Minimum cycle		1324		1184		1064	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		48		48		48	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		24		24		24	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR, see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only refresh); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1324		1184		1064	mA
I_{CC4}	Average page current (one $\overline{RAS}$ active, see Note 4)	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		944		824		704	mA

† For test conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz (see Note 5)

PARAMETER			'497MBM36A		'893NMB36A		UNIT
			MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, A0–A10			60		120	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs			42		42	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs			21		42	pF
$C_{i(W)}$	Input capacitance, write-enable input			84		168	pF
$C_{o(DQ)}$	Output capacitance	DQ pins		7		14	pF
		Parity pins		12		24	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'497MBM36A-60 '893NBM36A-60		'497MBM36A-70 '893NBM36A-70		'497MBM36A-80 '893NBM36A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ low to output in low-impedance state	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns
t_{OH}	Output disable time, start of $\overline{CAS}$ high	3		3		3		ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'497MBM36A-60 '893NBM36A-60		'497MBM36A-70 '893NBM36A-70		'497MBM36A-80 '893NBM36A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 7 and 8)	40		45		50		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low,	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{CAS}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low	10		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns

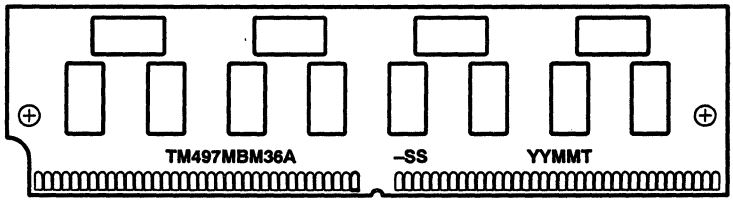
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'497MBM36A-60 '893NBM36A-60		'497MBM36A-70 '893NBM36A-70		'497MBM36A-80 '893NBM36A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR refresh only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTE 10: The maximum value is specified only to assure access time.

device symbolization (TM497MBM36A illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE: Location of symbolization may vary.

Contents

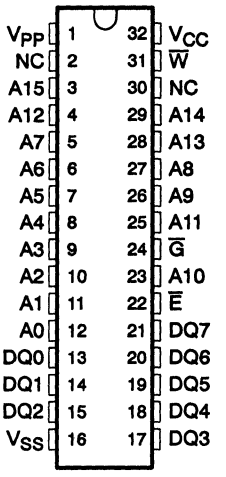
CHAPTER 7. FLASH MEMORY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EPROM) ONE-TIME PROGRAMMABLE MEMORY (OTP)

- **Organization . . . 64K × 8-Bit Flash Memory**
- **All Inputs/Outputs TTL Compatible**
- **V_{CC} Tolerance ±10%**
- **Maximum Access / Minimum Cycle Time**

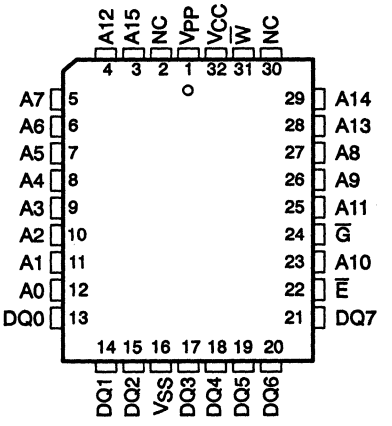
'28F512A-10	100 ns
'28F512A-12	120 ns
'28F512A-15	150 ns
'28F512A-17	170 ns

- **Industry-Standard Programming Algorithm**
- **PEP4 Version Available With 168-Hour Burn-In and Choice of Operating Temperature Ranges**
- **Chip Erase Before Reprogramming**
- **10000 and 1000 Program/Erase Cycles**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active Write . . . 55 mW**
  - **Active Read . . . 165 mW**
  - **Electrical Erase . . . 82.5 mW**
  - **Standby . . . 0.55 mW (CMOS-Input Levels)**
- **Automotive Temperature Range – 40°C to 125°C**

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

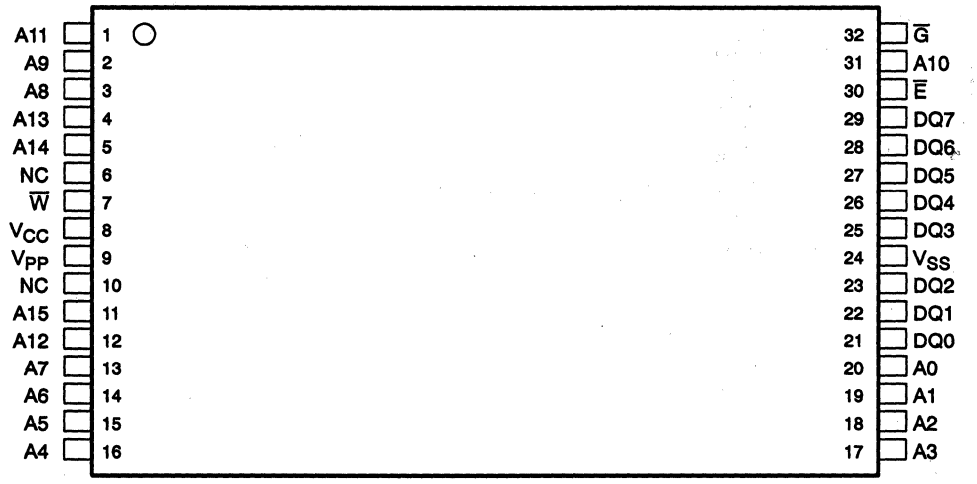
The TMS28F512A Flash memory is a 524 288-bit, programmable read-only memory that can be electrically bulk-erased and reprogrammed. It is available in 10000 and 1000 program/erase endurance cycle versions.

The TMS28F512A is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers, a 32-lead plastic leaded chip-carrier package with 1,25-mm (50-mil) lead spacing (FM suffix), a 32-lead thin small-outline package (DD suffix), and a reverse-pinout TSOP package (DU suffix).

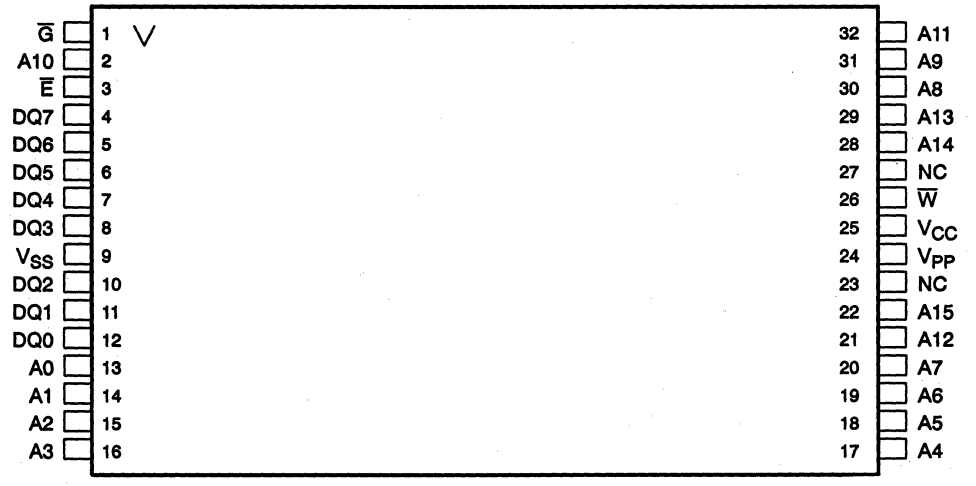
The TMS28F512A is characterized for operation in temperature ranges of 0°C to 70°C (NL, FML, DDL, and DUL suffixes), –40°C to 85°C (NE, FME, DDE, and DUE suffixes), and –40°C to 125°C (NQ, FMQ, DDQ, and DUQ suffixes). All package types are offered with 168-hour burn-in (4 suffix).

PIN NOMENCLATURE	
A0–A15	Address Inputs
DQ0–DQ7	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Internal Connection
V_{CC}	5-V Power Supply
V_{PP}	12-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

DD PACKAGE
(TOP VIEW)



DU PACKAGE
REVERSE PINOUT
(TOP VIEW)



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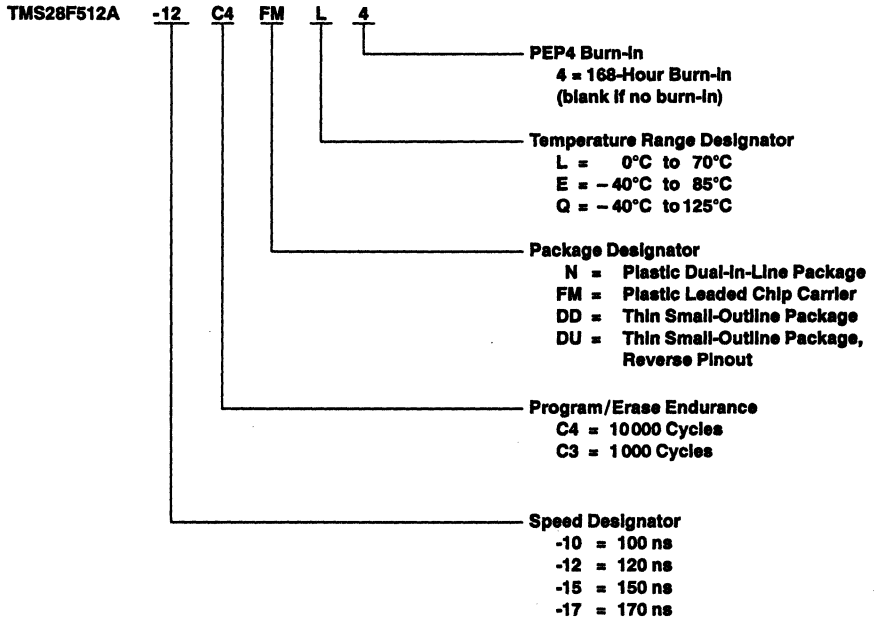
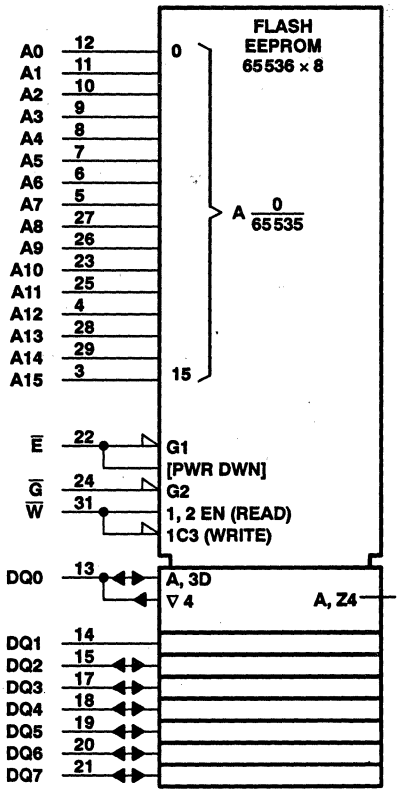
device symbol nomenclature



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

functional block diagram

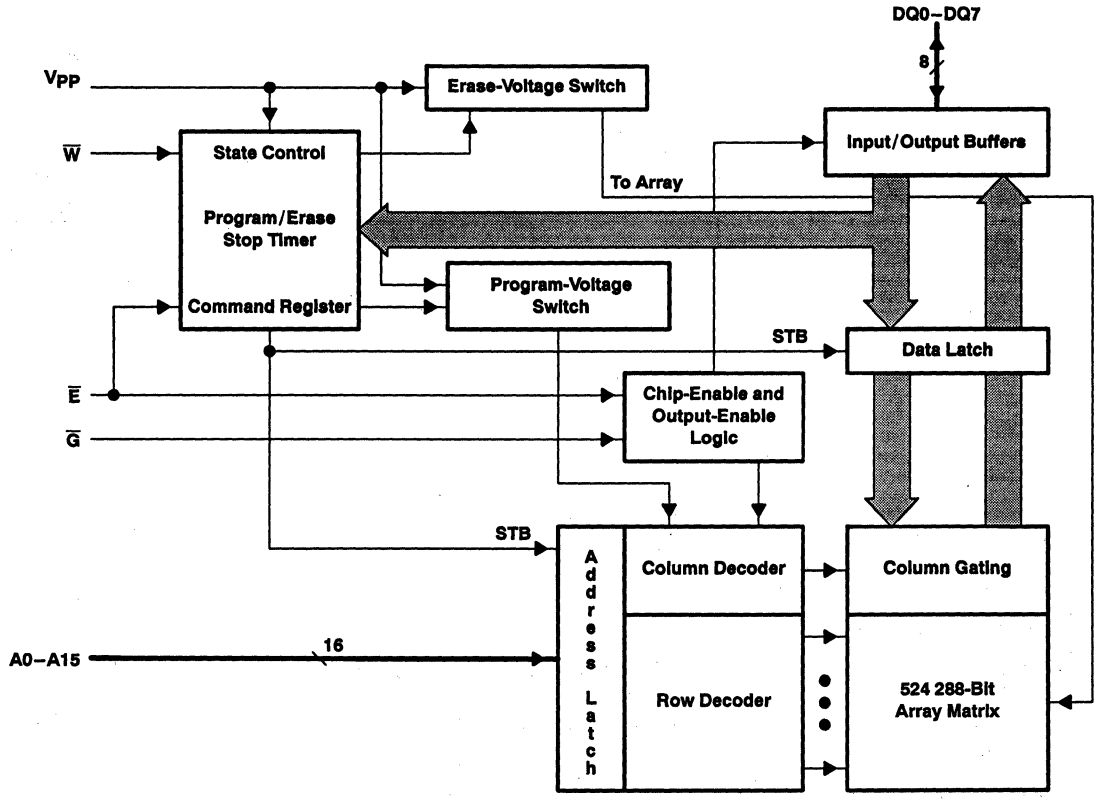


Table 1. Operation Modes

MODE		FUNCTION†						
		V_{PP}‡ (1)	$\overline{E}$ (22)	$\overline{G}$ (24)	A0 (12)	A9 (26)	$\overline{W}$ (31)	DQ0–DQ7 (13–15, 17–21)
Read	Read	V_{PPL}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable	V_{PPL}	V_{IL}	V_{IH}	X	X	V_{IH}	Hi-Z
	Standby and Write Inhibit	V_{PPL}	V_{IH}	X	X	X	X	Hi-Z
	Algorithm-Selection Mode	V_{PPL}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	V_{IH}	Mfr Equivalent Code 89h
					V_{IH}			Device Equivalent Code B8h
Read / Write	Read	V_{PPH}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IH}	Hi-Z
	Standby and Write Inhibit	V_{PPH}	V_{IH}	X	X	X	X	Hi-Z
	Write	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IL}	Data In

† X can be V_{IL} or V_{IH}.
‡ $V_{PPL} \le V_{CC} + 2$ V; V_{PPH} is the programming voltage specified for the device. For more details, see recommended operating conditions.

operation

read/output disable

When the outputs of two or more TMS28F512As are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of other devices. To read the output of the TMS28F512A, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

standby and write inhibit

Active I_{CC} current can be reduced from 30 mA to 1 mA by applying a high TTL level on $\overline{E}$ or to 100 µA with a high CMOS level on $\overline{E}$. In this mode, all outputs are in the high-impedance state. The TMS28F512A draws active current when it is deselected during programming, erasure, or program/erase verification. It continues to draw active current until the operation is terminated.

algorithm-selection mode

The algorithm-selection mode provides access to a binary code identifying the correct programming and erase algorithms. This mode is activated when A9 is forced to V_{ID}. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. A0 low selects the manufacturer equivalent code 89h, and A0 high selects the device equivalent code B8h, as shown in the algorithm-selection mode table below:

IDENTIFIER§	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Manufacturer Equivalent Code	V_{IL}	1	0	0	0	1	0	0	1	89
Device Equivalent Code	V_{IH}	1	0	1	1	1	0	0	0	B8

§ $\overline{E} = \overline{G} = V_{IL}$, A1 – A8 = V_{IL}, A9 = V_{ID}, A10–A15 = V_{IL}, $V_{PP} = V_{PPL}$.

programming and erasure

In the erased state, all bits are at a logic 1. Before erasing the device, all memory bits must be programmed to a logic 0. Afterwards, the entire chip is erased. At this point, the bits, now logic 1s, can be programmed accordingly. Refer to the Fastwrite and Fasterase algorithms for further detail.

command register

The command register controls the program and erase functions of the TMS28F512A. The algorithm-selection mode can be activated using the command register in addition to the previously described method. When V_{PP} is high, the contents of the command register and the function being performed can be changed. The command register is written to when $\overline{E}$ is low and $\overline{W}$ is pulsed low. The address is latched on the leading edge of the pulse, while the data is latched on the trailing edge. Accidental programming or erasure is minimized because two commands must be executed to invoke either operation.

power supply considerations

Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Changes in current drain on V_{PP} requires it to have a bypass capacitor as well. Printed circuit traces for both power supplies should be appropriate to handle the current demand.

Table 2. Command Definitions

COMMAND	REQUIRED BUS CYCLES	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION†	ADDRESS	DATA	OPERATION†	ADDRESS	DATA
Read	1	Write	X	00h	Read	RA	RD
Algorithm-Selection Mode	3	Write	X	90h	Read	0000 0001	89h B8h
Set-Up-Erase/Erase	2	Write	X	20h	Write	X	20h
Erase Verify	2	Write	EA	A0h	Read	X	EVD
Set-Up-Program/Program	2	Write	X	40h	Write	PA	PD
Program Verify	2	Write	X	C0h	Read	X	PVD
Reset	2	Write	X	FFh	Write	X	FFh

† Modes of operation are defined in Table 1.

Legend:

EA Address of memory location to be read during erase verify
RA Address of memory location to be read
PA Address of memory location to be programmed. Address is latched on the falling edge of $\overline{W}$.
RD Data read from location RA during the read operation
EVD Data read from location EA during erase verify
PD Data to be programmed at location PA. Data is latched on the rising edge of $\overline{W}$.
PVD Data read from location PA during program verify

command definitions

read command

Memory contents can be accessed while V_{PP} is high or low. When V_{PP} is high, writing 00h into the command register invokes the read operation. When the device is powered up, the default contents of the command register are 00h and the read operation is enabled. The read operation remains enabled until a different valid command is written to the command register.

algorithm-selection-mode command

The algorithm-selection mode is activated by writing 90h into the command register. The manufacturer equivalent code (89h) is identified by the value read from address location 0000h, and the device equivalent code (B8h) is identified by the value read from address location 0001h.

set-up-erase/erase commands

The erase algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = V_{PPH}$, and $V_{CC} = 5$ V. To enter the erase mode, write the set-up-erase command, 20h, into the command register. After the TMS28F512A is in the erase mode, writing a second erase command, 20h, into the command register invokes the erase operation. The erase operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$. The erase operation requires 10 ms to complete before the erase-verify command, A0h, can be loaded.

Maximum erase timing is controlled by the internal stop timer. When the stop timer terminates the erase operation, the device enters an inactive state and remains inactive until a valid erase-verify, read, or reset command is received.

erase-verify command

All bytes must be verified following an erase operation. After the erase operation is complete, an erased byte can be verified by writing the erase-verify command, A0h, into the command register. This command causes the device to exit the erase mode on the rising edge of $\overline{W}$. The address of the byte to be verified is latched on the falling edge of $\overline{W}$. The erase-verify operation remains enabled until a valid command is written to the command register.

To determine whether or not all the bytes have been erased, the TMS28F512A applies a margin voltage to each byte. If FFh is read from the byte, all bits in the designated byte have been erased. The erase-verify operation continues until all of the bytes have been verified. If FFh is not read from a byte, an additional erase operation needs to be executed. Figure 2 shows the combination of commands and bus operations for electrically erasing the TMS28F512A.

set-up-program/program commands

The programming algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = V_{PPH}$, and $V_{CC} = 5$ V. To enter the programming mode, write the set-up-program command, 40h, into the command register. The programming operation is invoked by the next write-enable pulse. Addresses are latched internally on the falling edge of $\overline{W}$, and data is latched internally on the rising edge of $\overline{W}$. The programming operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$ pulse. The program operation requires 10 µs for completion before the program-verify command, C0h, can be loaded.

Maximum program timing is controlled by the internal stop timer. When the stop timer terminates the program operation, the device enters an inactive state and remains inactive until a valid program-verify, read, or reset command is received.

program-verify command

The TMS28F512A can be programmed sequentially or randomly because it is programmed one byte at a time. Each byte must be verified after it is programmed. The program-verify operation prepares the device to verify the most recently programmed byte. To invoke the program-verify operation, C0h must be written into the command register. The program-verify operation ends on the rising edge of $\overline{W}$.

While verifying a byte, the TMS28F512A applies an internal margin voltage to the designated byte. If the true data and programmed data match, programming continues to the next designated byte location; otherwise, the byte must be reprogrammed. Figure 1 shows how commands and bus operations are combined for byte programming.

reset command

To reset the TMS28F512A after set-up-erase command or set-up-program command operations without changing the contents in memory, write FFh into the command register two consecutive times. After executing the reset command, a valid command must be written into the command register to change to a new state.

Fastwrite algorithm

The TMS28F512A is programmed using the Texas Instruments Fastwrite algorithm shown in Figure 1. This algorithm programs in a nominal time of two seconds.

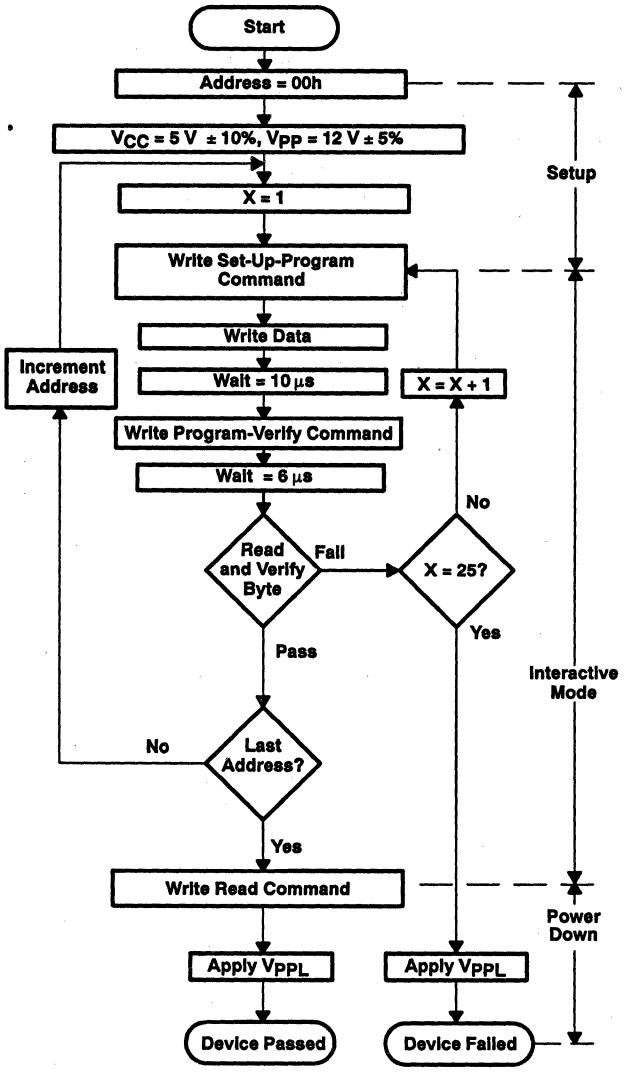
Fasterase algorithm

The TMS28F512A is erased using the Texas Instruments Fasterase algorithm shown in Figure 2. The memory array needs to be completely programmed (using the Fastwrite algorithm) before erasure begins. Erasure typically occurs in one second.

parallel erasure

To reduce total erase time, several devices can be erased in parallel. Since each Flash EEPROM can erase at a different rate, every device must be verified separately after each erase pulse. After a given device has been successfully erased, the erase command should not be issued to this device again. All devices that complete erasure should be masked until the parallel erasure process is finished (see Figure 3).

Examples of how to mask a device during parallel erase include driving the $\overline{E}$ pin high, writing the read command (00h) to the device when the others receive a set-up-erase or erase command, or disconnecting it from all electrical signals with relays or other types of switches.



Bus Operation	Command	Comments
Initialize Address		
Standby		Wait for V_{PP} to ramp to V_{PPH} (see Note A)
		Initialize pulse count
Write	Set-Up-Program	Data = 40h
Write	Write Data	Valid address/data
Standby		Wait = 10 µs
Write	Program-Verify	Data = C0h; ends program operation
Standby		Wait = 6 µs
Read		Read byte to verify programming; compare output to expected output
Write	Read	Data = 00h; resets register for read operations
Standby		Wait for V_{PP} to ramp to V_{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 1. Programming Flowchart: Fastwrite Algorithm

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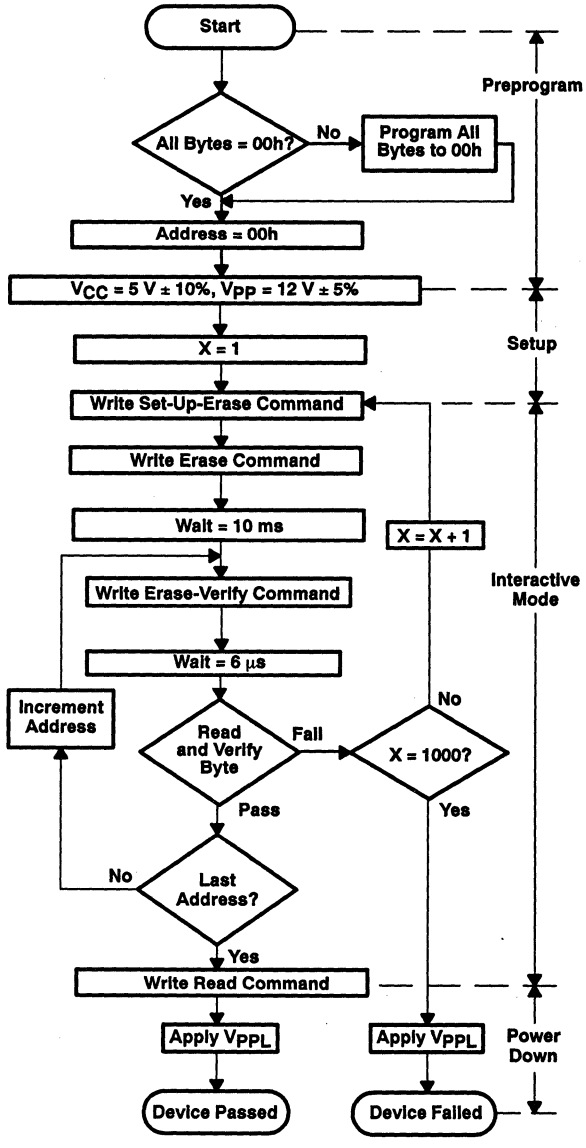
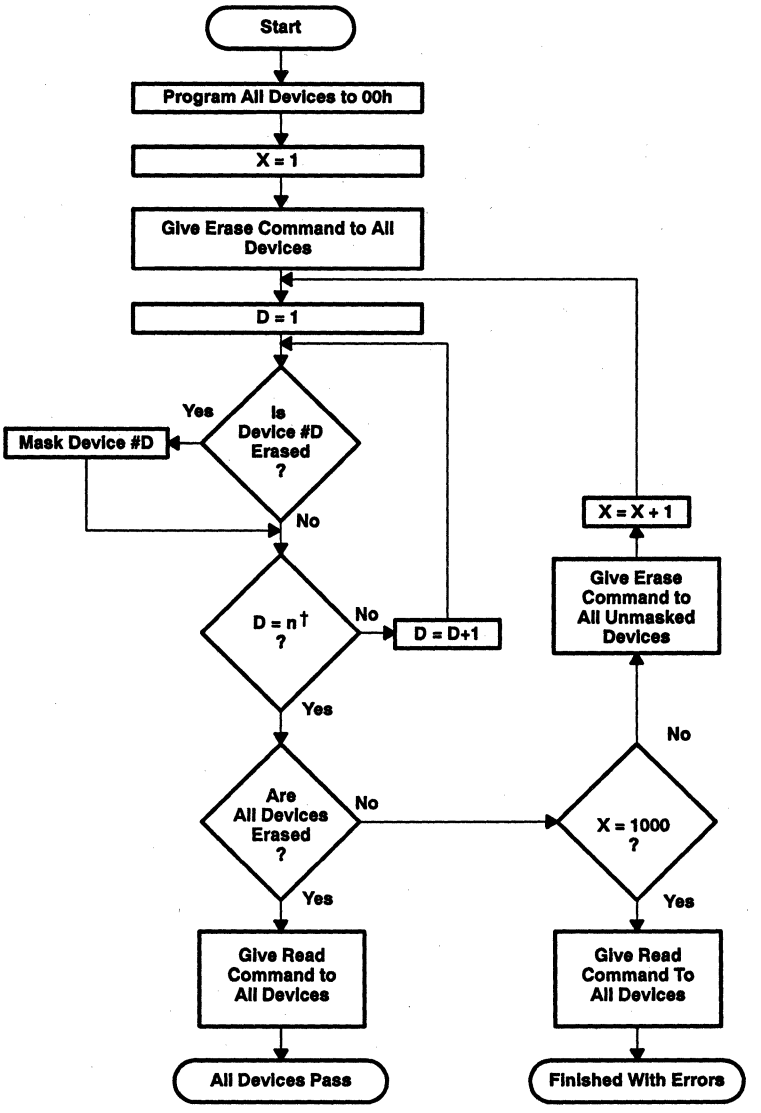


Bus Operation	Command	Comments
		Entire memory must = 00h before erasure Use Fastwrite programming algorithm
		Initialize addresses
Standby		Wait for V_{PP} to ramp to V_{PPH} (see Note A)
		Initialize pulse count
Write	Set-Up-Erase	Data = 20h
Write	Erase	Data = 20h
Standby		Wait = 10 ms
Write	Erase-Verify	Addr = Byte to verify; Data = A0h; ends the erase operation
Standby		Wait = 6 µs
Read		Read byte to verify erasure; compare output to FFh
Write	Read	Data = 00h; resets register for read operations
Standby		Wait for V_{PP} to ramp to V_{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 2. Flash-Erase Flowchart: Fasterase Algorithm



† n = number of devices being erased.

Figure 3. Parallel-Erase Flow Diagram

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} ..... – 0.6 V to 14 V
Input voltage range (see Note 2): All inputs except A9 ..... – 0.6 V to V_{CC} + 1 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range (see Note 3) ..... – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range during read/erase/program, T_A
NL, FML, DDL, DUL ..... 0°C to 70°C
NE, FME, DDE, DUE ..... – 40°C to 85°C
NQ, FMQ, DDQ, DUQ ..... – 40° C to 125°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to V_{SS}.
2. The voltage on any input pin can undershoot to – 2.0 V for periods less than 20 ns.
3. The voltage on any output pin can overshoot to 7.0 V for periods less than 20 ns.

recommended operating conditions

				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	During write/read/flash erase		4.5	5	5.5	V
V_{PP}	Supply voltage	During read only (V_{PPL})		0		$V_{CC}+2$	V
		During write/read/flash erase (V_{PPH})		11.4	12	12.6	V
V_{ID}	Voltage level on A9 for algorithm-selection mode			11.5		13	V
V_{IH}	High-level dc input voltage		TTL	2		$V_{CC}+0.5$	V
			CMOS	$V_{CC}-0.5$		$V_{CC}+0.5$	
V_{IL}	Low-level dc input voltage		TTL	–0.5		0.8	V
			CMOS	GND – 0.2		GND+0.2	
T_A	Operating free-air temperature		NL, FML, DDL, DUL suffix	0		70	°C
			NE, FME, DDE, DUE suffix	– 40		85	
			NQ, FMQ, DDQ, DUQ suffix	– 40		125	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 2.5 mA	2.4			V
			I_{OH} = – 100 µA	V_{CC} – 0.4			
V_{OL}	Low-level output voltage		I_{OL} = 5.8 mA			0.45	V
			I_{OL} = 100 µA			0.1	
I_{ID}	A9 algorithm-selection-mode current		A9 = V_{ID} max			200	µA
I_I	Input current (leakage)	All except A9	V_I = 0 V to 5.5 V			±1	µA
		A9	V_I = 0 V to 13 V			± 200	
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±10	µA
I_{PP1}	V_{PP} supply current (read/standby)		V_{PP} = V_{PPH}, Read mode			200	µA
			V_{PP} = V_{PPL}			±10	µA
I_{PP2}	V_{PP} supply current (during program pulse) (see Note 4)		V_{PP} = V_{PPH}			30	mA
I_{PP3}	V_{PP} supply current (during flash erase) (see Note 4)		V_{PP} = V_{PPH}			30	mA
I_{PP4}	V_{PP} supply current (during program/erase-verify) (see Note 4)		V_{PP} = V_{PPH}			5.0	mA
I_{CCS}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			1	mA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			100	µA
I_{CC1}	V_{CC} supply current (active read)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, f = 6 MHz, Outputs open			30	mA
I_{CC2}	V_{CC} average supply current (active write) (see Note 4)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, Programming in progress			10	mA
I_{CC3}	V_{CC} average supply current (flash erase) (see Note 4)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, Erasure in progress			15	mA
I_{CC4}	V_{CC} average supply current (program/erase-verify) (see Note 4)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, V_{PP} = V_{PPH}, Program/erase-verify in progress			15	mA

NOTE 4: Not 100% tested; characterization data available

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_I	Input capacitance	V_I = 0 V, f = 1 MHz		6	pF
C_O	Output capacitance	V_O = 0 V, f = 1 MHz		12	pF

† Capacitance measurements are made on sample basis only.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

		TEST CONDITIONS	ALTERNATE SYMBOL	'28F512A-10		'28F512A-12		'28F512A-15		'28F512A-17		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address, A	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns	t_{AVQV}		100		120		150		170	ns
$t_{a(E)}$	Access time from $\overline{E}$		t_{ELQV}		100		120		150		170	ns
$t_{en(G)}$	Access time from $\overline{G}$		t_{GLQV}		45		50		55		60	ns
$t_{c(R)}$	Cycle time, read		t_{AVAV}	100		120		150		170		ns
$t_{d(E)}$	Delay time, $\overline{E}$ low to low-Z output		t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-Z output		t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Chip disable time to Hi-Z output		t_{EHQZ}	0	55	0	55	0	55	0	55	ns
$t_{dis(G)}$	Output disable time to Hi-Z output		t_{GHQZ}	0	30	0	30	0	35	0	35	ns
$t_{h(D)}$	Hold time, data valid from address, $\overline{E}$, or $\overline{G}$‡		t_{AXQX}	0		0		0		0		ns
$t_{rec(W)}$	Write recovery time before read		t_{WHGL}	6		6		6		6		µs

‡ Whichever occurs first

timing requirements–write/erase/program operations

PARAMETER		ALTERNATE SYMBOL	'28F512A-10			'28F512A-12			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{W}$	t_{AVAV}	100			120			ns
$t_{c(W)PR}$	Cycle time, programming operation	t_{WHWH1}	10			10			µs
$t_{c(W)ER}$	Cycle time, erase operation	t_{WHWH2}	9.5	10		9.5	10		ms
$t_{h(A)}$	Hold time, address	t_{WLAX}	55			60			ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0			0			ns
$t_{h(WHD)}$	Hold time, data valid after $\overline{W}$ high	t_{WHDX}	10			10			ns
$t_{su(A)}$	Setup time, address	t_{AVWL}	0			0			ns
$t_{su(D)}$	Setup time, data	t_{DVWH}	50			50			ns
$t_{su(E)}$	Setup time, $\overline{E}$ before $\overline{W}$	t_{ELWL}	20			20			ns
$t_{su(EHVPP)}$	Setup time, $\overline{E}$ high to V_{PP} ramp	t_{EHVP}	100			100			ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ low	t_{VPEL}	1.0			1.0			µs
$t_{rec(W)}$	Recovery time, $\overline{W}$ before read	t_{WHGL}	6			6			µs
$t_{rec(R)}$	Recovery time, read before $\overline{W}$	t_{GHWL}	0			0			µs
$t_{w(W)}$	Pulse duration, $\overline{W}$ (see Note 5)	t_{WLWH}	60			60			ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20			20			ns
$t_{r(VPP)}$	Rise time, V_{PP}	t_{VPPR}	1			1			µs
$t_{f(VPP)}$	Fall time, V_{PP}	t_{VPPF}	1			1			µs

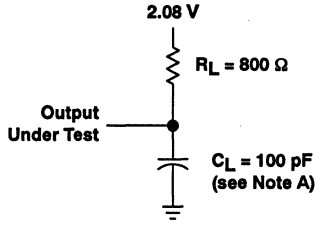
PARAMETER		ALTERNATE SYMBOL	'28F512A-15			'28F512A-17			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{W}$	t_{AVAV}	150			170			ns
$t_{c(W)PR}$	Cycle time, programming operation	t_{WHWH1}	10			10			µs
$t_{c(W)ER}$	Cycle time, erase operation	t_{WHWH2}	9.5	10		9.5	10		ms
$t_{h(A)}$	Hold time, address	t_{WLAX}	60			70			ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0			0			ns
$t_{h(WHD)}$	Hold time, data valid after $\overline{W}$ high	t_{WHDX}	10			10			ns
$t_{su(A)}$	Setup time, address	t_{AVWL}	0			0			ns
$t_{su(D)}$	Setup time, data	t_{DVWH}	50			50			ns
$t_{su(E)}$	Setup time, $\overline{E}$ before $\overline{W}$	t_{ELWL}	20			20			ns
$t_{su(EHVPP)}$	Setup time, $\overline{E}$ high to V_{PP} ramp	t_{EHVP}	100			100			ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ low	t_{VPEL}	1.0			1.0			µs
$t_{rec(W)}$	Recovery time, $\overline{W}$ before read	t_{WHGL}	6			6			µs
$t_{rec(R)}$	Recovery time, read before $\overline{W}$	t_{GHWL}	0			0			µs
$t_{w(W)}$	Pulse duration, $\overline{W}$ (see Note 5)	t_{WLWH}	60			60			ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20			20			ns
$t_{r(VPP)}$	Rise time, V_{PP}	t_{VPPR}	1			1			µs
$t_{f(VPP)}$	Fall time, V_{PP}	t_{VPPF}	1			1			µs

NOTE 5: Rise/fall time ≤ 10 ns

timing requirements — alternative $\overline{E}$-controlled writes

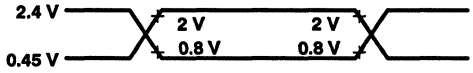
PARAMETER		ALTERNATE SYMBOL	'28F512A-10		'28F512A-12		'28F512A-15		'28F512A-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{E}$	t_{AVAV}	100		120		150		170		ns
$t_{c(E)PR}$	Cycle time, programming operation	t_{EHEH}	10		10		10		10		µs
$t_{h(EA)}$	Hold time, address	t_{ELAX}	75		80		80		90		ns
$t_{h(ED)}$	Hold time, data	t_{EHDX}	10		10		10		10		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	0		0		0		0		ns
$t_{su(A)}$	Setup time, address	t_{AVEL}	0		0		0		0		ns
$t_{su(D)}$	Setup time, data	t_{DVEH}	50		50		50		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before $\overline{E}$	t_{WLEL}	0		0		0		0		ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ low	t_{VPEL}	1.0		1.0		1.0		1.0		µs
$t_{rec(E)R}$	Recovery time, write using $\overline{E}$ before read	t_{EHGL}	6		6		6		6		µs
$t_{rec(E)W}$	Recovery time, read before write using $\overline{E}$	t_{GHEL}	0		0		0		0		µs
$t_{w(E)}$	Pulse duration, write using $\overline{E}$	t_{ELEH}	70		70		70		80		ns
$t_{w(EH)}$	Pulse duration, write, $\overline{E}$ high	t_{EHEL}	20		20		20		20		ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.



VOLTAGE WAVEFORMS

Figure 4. Load Circuit and Voltage Waveforms

AC testing inputs are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} as close as possible to the device pins.

PARAMETER MEASUREMENT INFORMATION

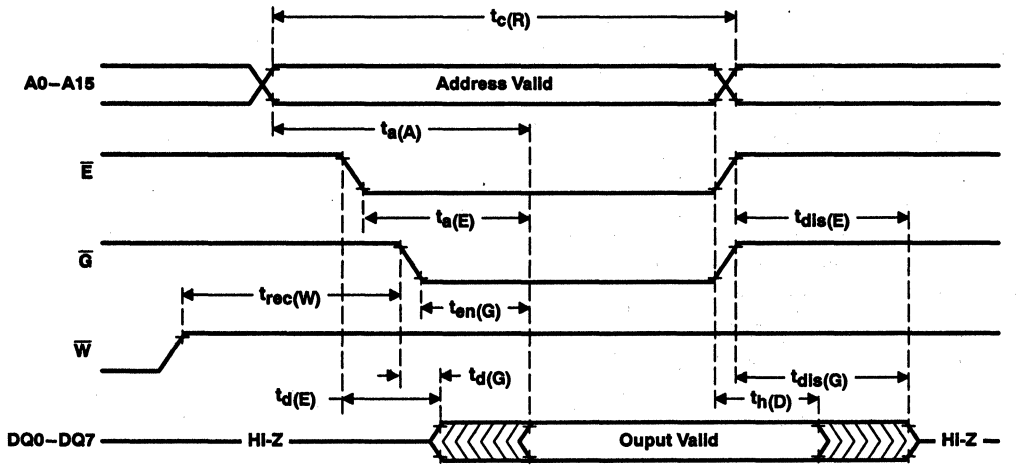


Figure 5. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

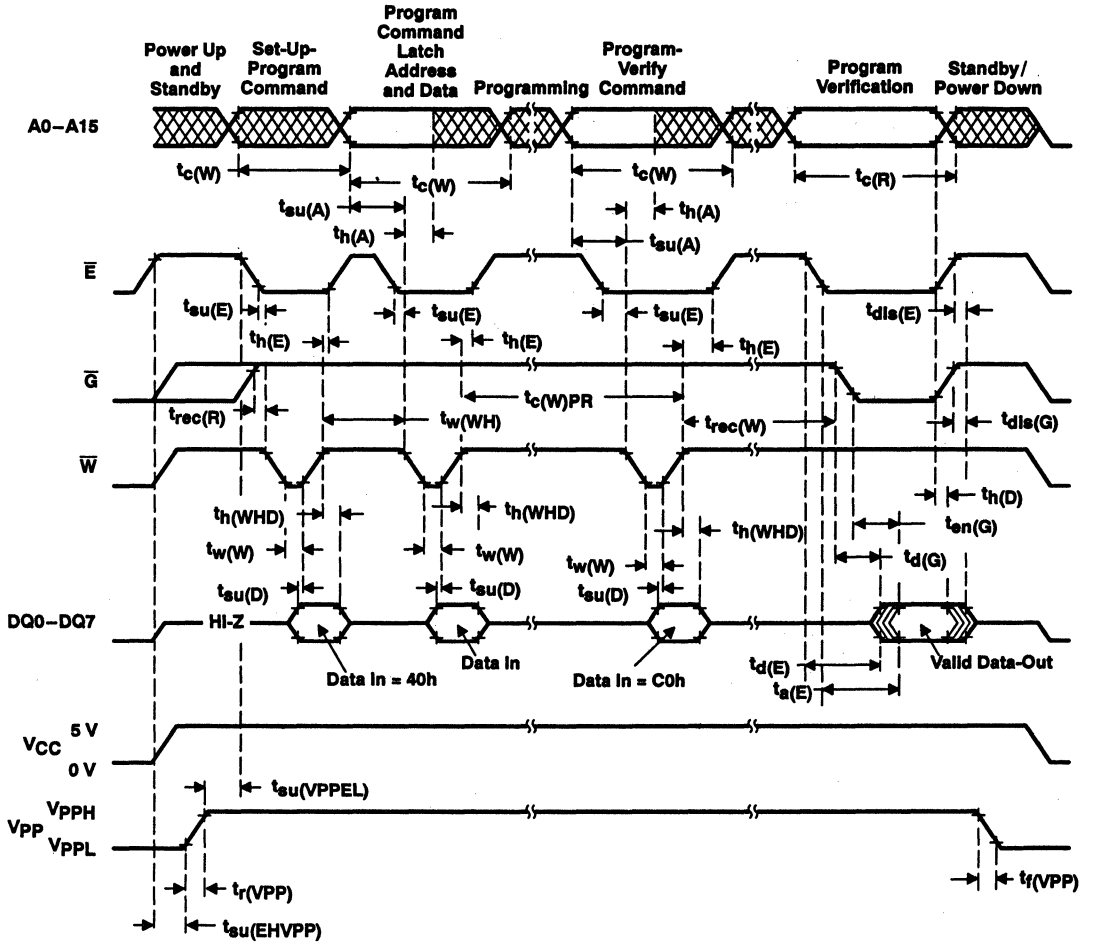


Figure 6. Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

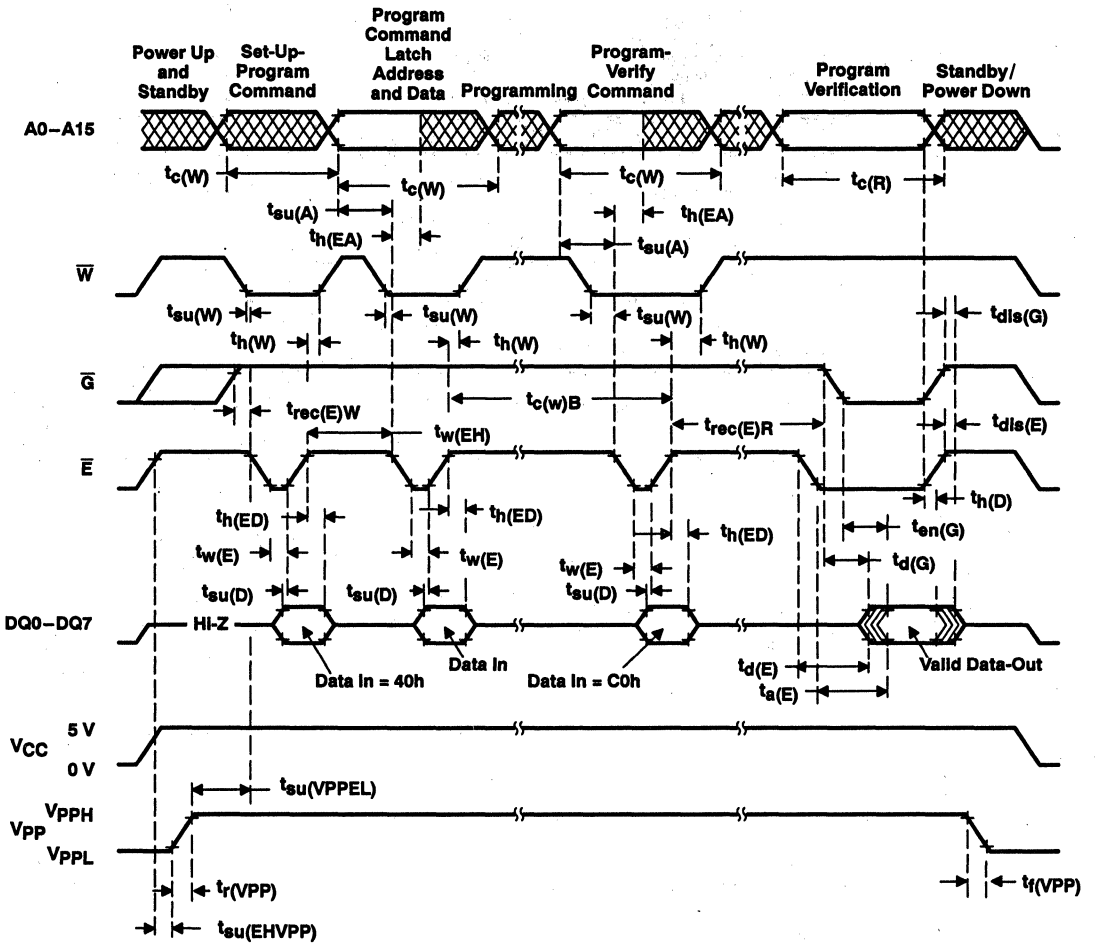


Figure 7. Write-Cycle (Alternative $\overline{E}$-Controlled Writes) Timing

PARAMETER MEASUREMENT INFORMATION

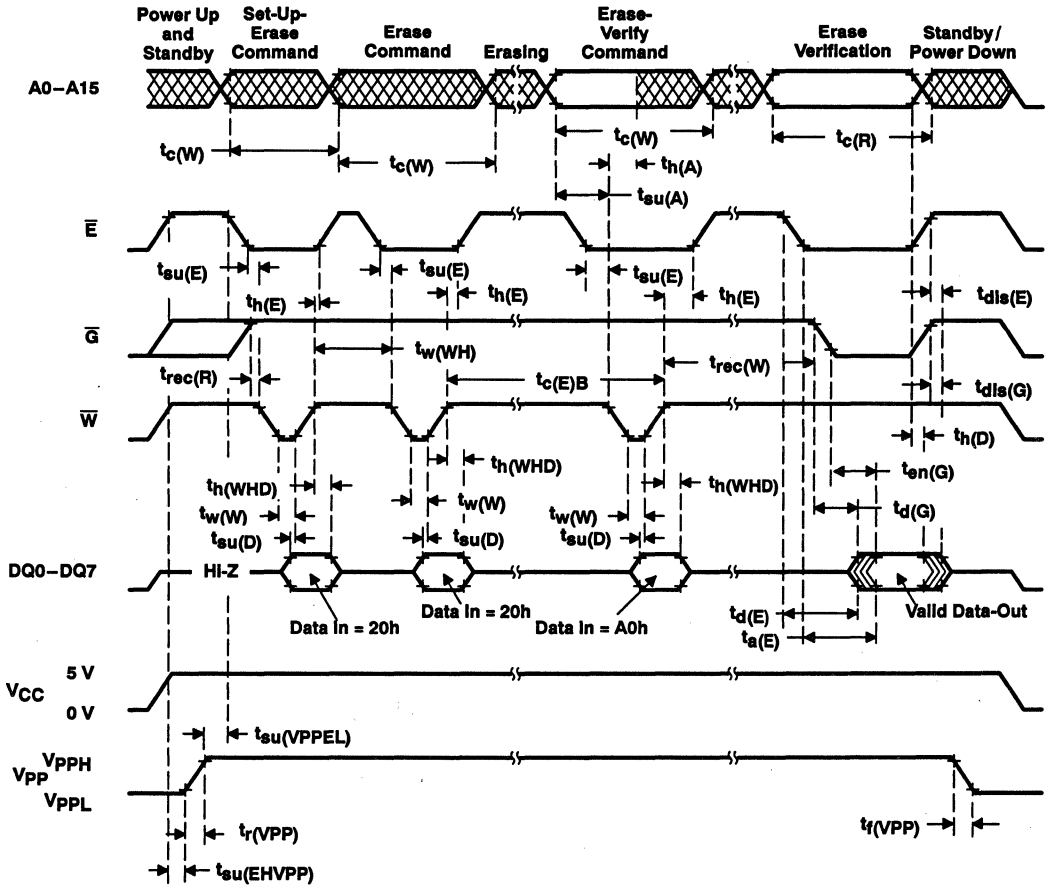
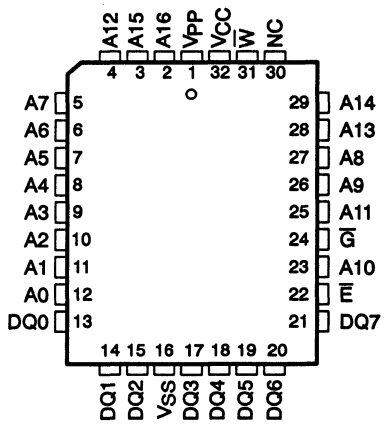


Figure 8. Flash-Erase-Cycle Timing

SMJS824A – MAY 1995 – REVISED JUNE 1995

- **Organization . . . 128K × 8-Bit Flash Memory**
- **Pin Compatible With Existing 1-Megabit EPROMs**
- **V_{CC} Tolerance ±10%**
- **All Inputs/Outputs TTL Compatible**
- **Maximum Access/Minimum Cycle Time**
  - **'28F010B-90 90 ns**
  - **'28F010B-10 100 ns**
  - **'28F010B-12 120 ns**
  - **'28F010B-15 150 ns**
- **Industry-Standard Programming Algorithm**
- **PEP4 Version Available With 168-Hour Burn-In, and Choice of Operating Temperature Ranges**
- **100000 and 10000 Program/Erase-Cycle Versions Available**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **–Active Write . . . 55 mW**
  - **–Active Read . . . 165 mW**
  - **–Electrical Erase . . . 82.5 mW**
  - **–Standby . . . 0.55 mW (CMOS-Input Levels)**
- **Automotive Temperature Range – 40°C to 125°C**

FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A16	Address Inputs
DQ0–DQ7	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Internal Connection
V_{CC}	5-V Power Supply
V_{PP}	12-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

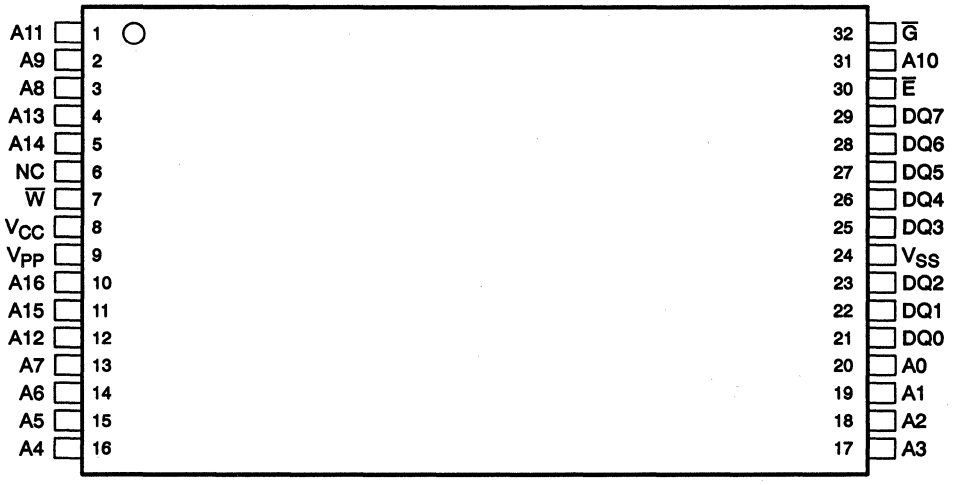
NOTE: Refer to page 2 for the DD and DU pinouts.

description

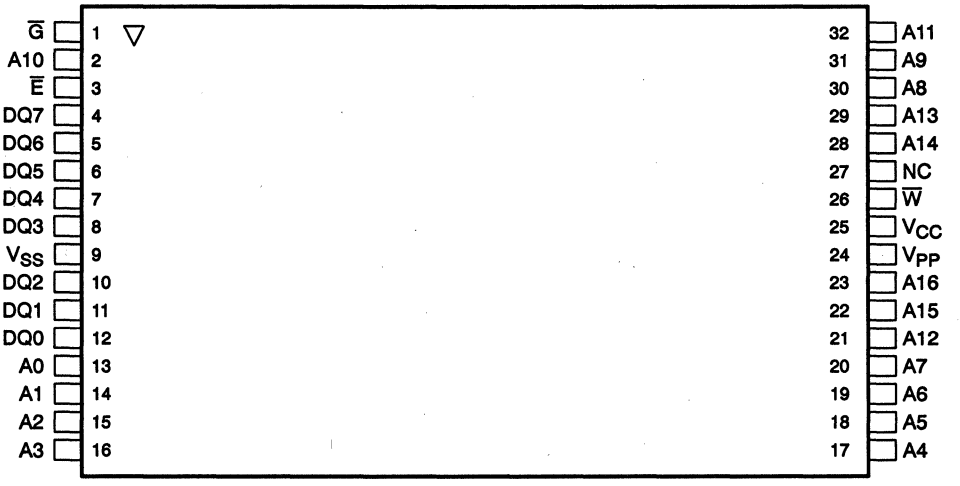
The TMS28F010B is a 1048576-bit, programmable read-only memory that can be electrically bulk-erased and reprogrammed. It is available in 100000 and 10000 program/erase-endurance-cycle versions.

The TMS28F010B Flash Memory is offered in a 32-lead plastic leaded chip-carrier package using 1,25-mm (50-mil) lead spacing (FM suffix), a 32-lead thin small-outline package (DD suffix), and a reverse pinout TSOP package (DU suffix).

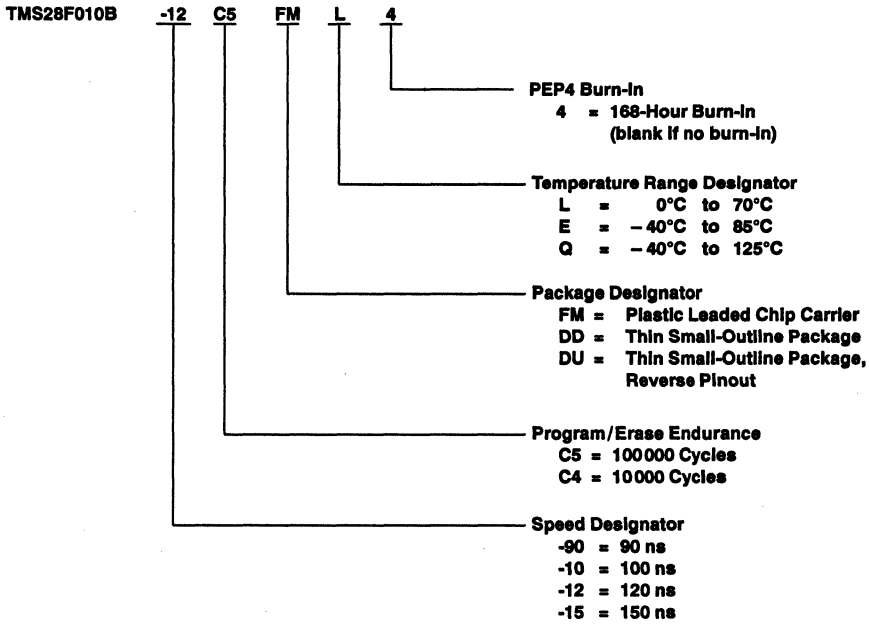
DD PACKAGE
(TOP VIEW)



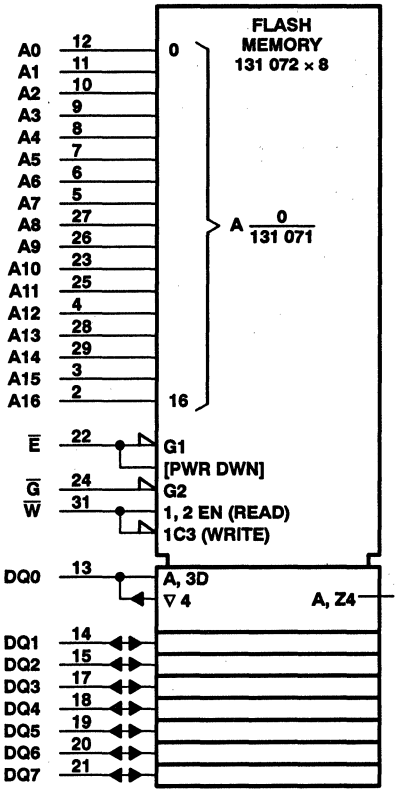
DU PACKAGE
REVERSE PINOUT
(TOP VIEW)



device symbol nomenclature



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FM package.

functional block diagram

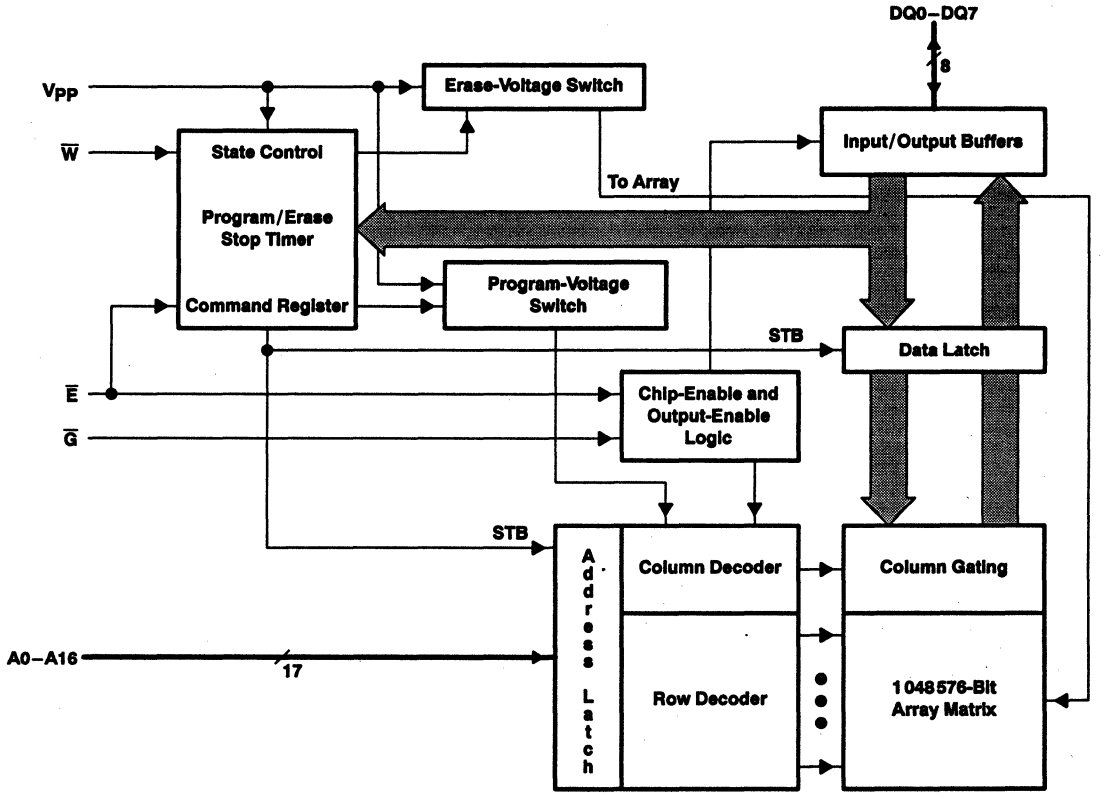


Table 1. Operation Modes

MODE		FUNCTION†						
		V_{PP}‡ (1)	$\overline{E}$ (22)	$\overline{G}$ (24)	A0 (12)	A9 (26)	$\overline{W}$ (31)	DQ0–DQ7 (13–15, 17–21)
Read	Read	V_{PPL}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable	V_{PPL}	V_{IL}	V_{IH}	X	X	V_{IH}	Hi-Z
	Standby and Write Inhibit	V_{PPL}	V_{IH}	X	X	X	X	Hi-Z
	Algorithm-Selection Mode	V_{PPL}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	V_{IH}	Mfr Equivalent Code 89h
					V_{IH}			Device Equivalent Code B4h
Read/ Write	Read	V_{PPH}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IH}	Hi-Z
	Standby and Write Inhibit	V_{PPH}	V_{IH}	X	X	X	X	Hi-Z
	Write	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IL}	Data In

† X can be V_{IL} or V_{IH}.
‡ $V_{PPL} \le V_{CC} + 2$ V; V_{PPH} is the programming voltage specified for the device. For more details, refer to the recommended operating conditions.

operation

read/output disable

When the outputs of two or more TMS28F010Bs are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of other devices. To read the output of the TMS28F010B, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

standby and write inhibit

Active I_{CC} current can be reduced from 30 mA to 1 mA by applying a high TTL level on $\overline{E}$ or to 100 µA with a high CMOS level on $\overline{E}$. In this mode, all outputs are in the high-impedance state. The TMS28F010B draws active current when it is deselected during programming, erasure, or program/erase verification. It continues to draw active current until the operation is terminated.

algorithm-selection mode

The algorithm-selection mode provides access to a binary code identifying the correct programming and erase algorithms. This mode is activated when A9 (pin 26) is forced to V_{ID}. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. A0 low selects the manufacturer equivalent code 89h, and A0 high selects the device equivalent code B4h, as shown in the algorithm-selection mode table below:

IDENTIFIER§	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Manufacturer Equivalent Code	V_{IL}	1	0	0	0	1	0	0	1	89
Device Equivalent Code	V_{IH}	1	0	1	1	0	1	0	0	B4

§ $\overline{E} = \overline{G} = V_{IL}$, A1–A8 = V_{IL}, A9 = V_{ID}, A10–A16 = V_{IL}, $V_{PP} = V_{PPL}$.

programming and erasure

In the erased state, all bits are at a logic 1. Before erasing the device, all memory bits must be programmed to a logic 0. Afterwards, the entire chip is erased. At this point, the bits, now logic 1s, can be programmed accordingly. Refer to the Fastwrite and Fasterase algorithms for further detail.

command register

The command register controls the program and erase functions of the TMS28F010B. The algorithm-selection mode can be activated using the command register in addition to the previously described method. When V_{PP} is high, the contents of the command register and the function being performed can be changed. The command register is written to when $\overline{E}$ is low and $\overline{W}$ is pulsed low. The address is latched on the leading edge of the pulse, while the data is latched on the trailing edge. Accidental programming or erasure is minimized because two commands must be executed to invoke either operation. The command register is inhibited when V_{CC} is below the erase/write lockout voltage, V_{LKO}.

power supply considerations

Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Changes in current drain on V_{PP} require it to have a bypass capacitor as well. Printed-circuit traces for both power supplies should be appropriate to handle the current demand.

Table 2. Command Definitions

COMMAND	REQUIRED BUS CYCLES	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION†	ADDRESS	DATA	OPERATION†	ADDRESS	DATA
Read	1	Write	X	00h	Read	RA	RD
Algorithm-Selection Mode	3	Write	X	90h	Read	0000 0001	89h B4h
Set-Up-Erase/Erase	2	Write	X	20h	Write	X	20h
Erase Verify	2	Write	EA	A0h	Read	X	EVD
Set-Up-Program/Program	2	Write	X	40h	Write	PA	PD
Program Verify	2	Write	X	C0h	Read	X	PVD
Reset	2	Write	X	FFh	Write	X	FFh

† Modes of operation are defined in Table 1.

Legend:

EA	Address of memory location to be read during erase verify
RA	Address of memory location to be read
PA	Address of memory location to be programmed. Address is latched on the falling edge of $\overline{W}$
RD	Data read from location RA during the read operation
EVD	Data read from location EA during erase verify
PD	Data to be programmed at location PA. Data is latched on the rising edge of $\overline{W}$
PVD	Data read from location PA during program verify

command definitions

read command

Memory contents can be accessed while V_{PP} is high or low. When V_{PP} is high, writing 00h into the command register invokes the read operation. When the device is powered up, the default contents of the command register are 00h and the read operation is enabled. The read operation remains enabled until a different valid command is written to the command register.

algorithm-selection mode command

The algorithm-selection mode is activated by writing 90h into the command register. The manufacturer-equivalent code (89h) is identified by the value read from address location 0000h, and the device-equivalent code (B4h) is identified by the value read from address location 0001h.

set-up-erase/erase commands

The erase-algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = V_{PPH}$, and $V_{CC} = 5$ V. To enter the erase mode, write the set-up-erase command, 20h, into the command register. After the TMS28F010B is in the erase mode, writing a second erase command, 20h, into the command register invokes the erase operation. The erase operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$. The erase operation requires at least 9.5 ms to complete before the erase-verify command, A0h, can be loaded.

Maximum erase timing is controlled by the internal stop timer. When the stop timer terminates the erase operation, the device enters an inactive state and remains inactive until a command is received.

program-verify command

The TMS28F010B can be programmed sequentially or randomly because it is programmed one byte at a time. Each byte must be verified after it is programmed. The program-verify operation prepares the device to verify the most recently programmed byte. To invoke the program-verify operation, C0h must be written into the command register. The program-verify operation ends on the rising edge of $\overline{W}$.

While verifying a byte, the TMS28F010B applies an internal margin voltage to the designated byte. If the true data and programmed data match, programming continues to the next designated byte location; otherwise, the byte must be reprogrammed. Figure 1 shows how commands and bus operations are combined for byte programming.

erase-verify command

All bytes must be verified following an erase operation. After the erase operation is complete, an erased byte can be verified by writing the erase-verify command, A0h, into the command register. This command causes the device to exit the erase mode on the rising edge of $\overline{W}$. The address of the byte to be verified is latched on the falling edge of $\overline{W}$. The erase-verify operation remains enabled until a command is written to the command register.

To determine whether or not all the bytes have been erased, the TMS28F010B applies a margin voltage to each byte. If FFh is read from the byte, all bits in the designated byte have been erased. The erase-verify operation continues until all of the bytes have been verified. If FFh is not read from a byte, an additional erase operation needs to be executed. Figure 2 shows the combination of commands and bus operations for electrically erasing the TMS28F010B.

set-up-program/program commands

The programming algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = V_{PPH}$, and $V_{CC} = 5$ V. To enter the programming mode, write the set-up-program command, 40h, into the command register. The programming operation is invoked by the next write-enable pulse. Addresses are latched internally on the falling edge of $\overline{W}$, and data is latched internally on the rising edge of $\overline{W}$. The programming operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$ pulse. The program operation requires 10 µs for completion before the program-verify command, C0h, can be loaded.

set-up-program/program commands (continued)

Maximum program timing is controlled by the internal stop timer. When the stop timer terminates the program operation, the device enters an inactive state and remains inactive until a command is received.

reset command

To reset the TMS28F010B after set-up-erase command or set-up-program command operations without changing the contents in memory, write FFh into the command register two consecutive times. After executing the reset command, the device defaults to the read mode.

Fastwrite algorithm

The TMS28F010B is programmed using the Texas Instruments Fastwrite algorithm shown in Figure 1. This algorithm programs in a nominal time of two seconds.

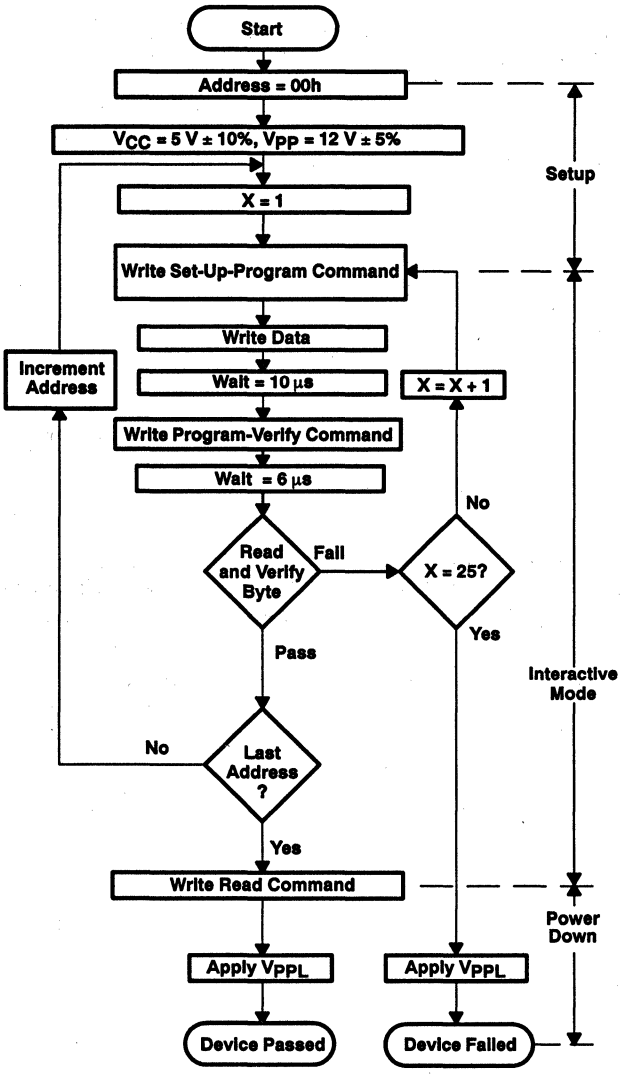
Fasterase algorithm

The TMS28F010B is erased using the Texas Instruments Fasterase algorithm shown in Figure 2. The memory array needs to be completely programmed (using the Fastwrite algorithm) before erasure begins. Erasure typically occurs in one second.

parallel erasure

To reduce total erase time, several devices can be erased in parallel. Since each Flash Memory can erase at a different rate, every device must be verified separately after each erase pulse. After a given device has been successfully erased, the erase command should not be issued to this device again. All devices that complete erasure should be masked until the parallel erasure process is finished (see Figure 3).

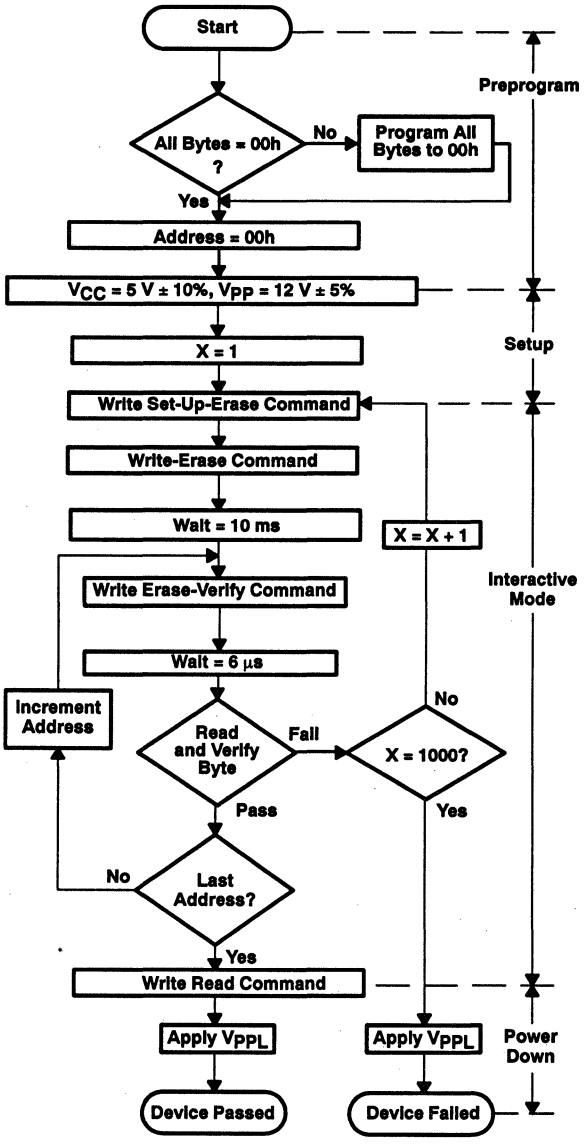
Examples of how to mask a device during parallel erase include driving the $\overline{E}$ pin high, writing the read command (00h) to the device when the others receive a set-up-erase or erase command, or disconnecting it from all electrical signals with relays or other types of switches.



Bus Operation	Command	Comments
Initialize Address *Standby*		 Wait for V_{PP} to ramp to V_{PPH} (see Note A) Initialize pulse count
Write	Set-Up-Program Write	Data = 40h
Write	Write Data	Valid address/data
Standby		Wait = 10 µs
Write	Program-Verify	Data = C0h; ends Program operation
Standby		Wait = 6 µs
Read		Read byte to verify Programming; compare output to expected output
—	—	—
Write	Read	Data = 00h; resets register for read operations
Standby		Wait for V_{PP} to ramp to V_{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

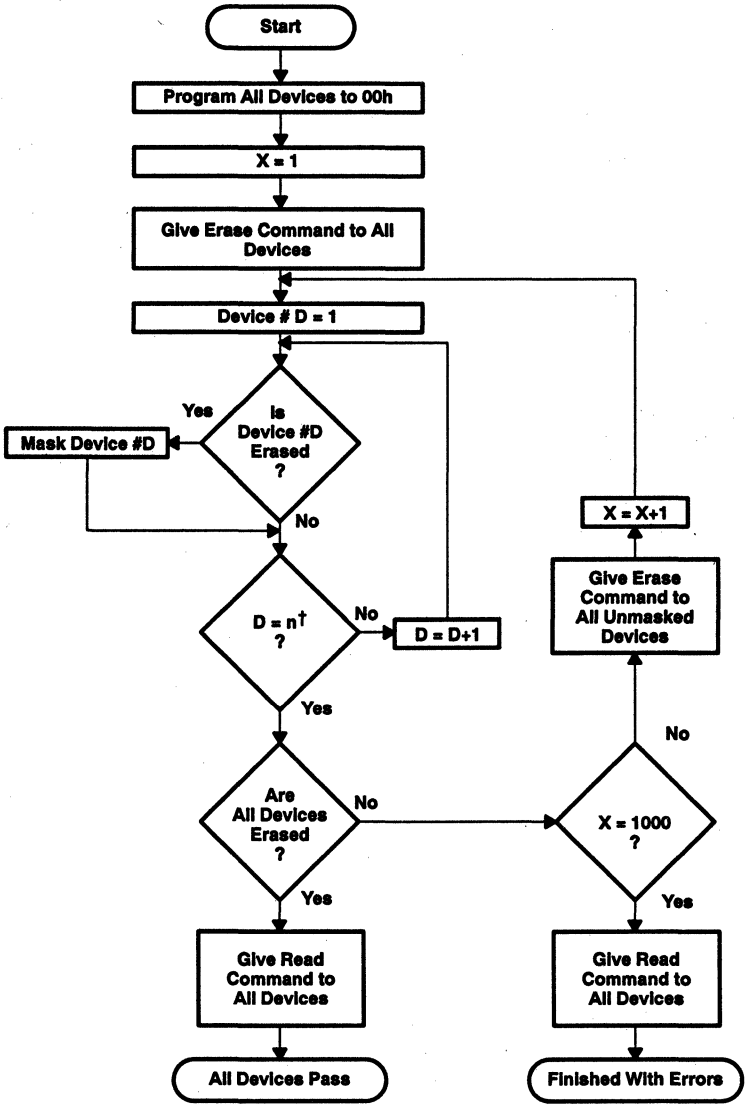
Figure 1. Programming Flowchart: Fastwrite Algorithm



Bus Operation	Command	Comments
		Entire memory must = 00h before erasure Use Fastwrite programming algorithm
		Initialize addresses
Standby		Wait for V_{PP} to ramp to V_{PPH} (see Note A)
		Initialize pulse count
Write	Set-Up-Erase	Data = 20h
Write	Erase	Data = 20h
Standby		Wait = 10 ms
Write	Erase Verify	Addr = Byte to verify; Data = A0h; ends the erase operation
Standby		Wait = 6 µs
Read		Read byte to verify erasure; compare output to FFh
Write	Read	Data = 00h; resets register for read operations
Standby		Wait for V_{PP} to ramp to V_{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 2. Flash-Erase Flowchart: Fasterase Algorithm



† n = number of devices being erased.

Figure 3. Parallel-Erase Flow Diagram

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –0.6 V to 7 V
Supply voltage range, V_{PP} ..... –0.6 V to 14 V
Input voltage range (see Note 2): All inputs except A9 ..... –0.6 V to V_{CC} + 1 V
A9 ..... –0.6 V to 13.5 V
Output voltage range (see Note 3) ..... –0.6 V to V_{CC} + 1 V
Operating free-air temperature range during read/erase/program, T_A
L ..... 0°C to 70°C
E ..... – 40°C to 85°C
Q ..... – 40° C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to V_{SS}.
2. The voltage on any input pin can undershoot to –2 V for periods less than 20 ns.
3. The voltage on any output pin can overshoot to 7 V for periods less than 20 ns.

recommended operating conditions

				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	During write/read/flash erase		4.5	5	5.5	V
V_{PP}	Supply voltage	During read only (V_{PPL})		0		V_{CC} + 2	V
		During write/read/flash erase (V_{PPH})		11.4	12	12.6	V
V_{IH}	High-level dc input voltage		TTL	2		V_{CC}+0.5	V
			CMOS	V_{CC} – 0.5		V_{CC}+0.5	
V_{IL}	Low-level dc input voltage		TTL	–0.5		0.8	V
			CMOS	GND – 0.2		GND+0.2	
V_{ID}	Voltage level on A9 for algorithm-selection mode			11.5		13	V

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 2.5 mA	2.4		V
			I_{OH} = – 100 µA	V_{CC} – 0.4		
V_{OL}	Low-level output voltage		I_{OL} = 5.8 mA		0.45	V
			I_{OL} = 100 µA		0.1	
I_{ID}	A9 algorithm-selection-mode current		A9 = V_{ID} max		200	µA
I_I	Input current (leakage)	All except A9	V_I = 0 V to 5.5 V		±1	µA
		A9	V_I = 0 V to 13 V		± 200	
I_O	Output current (leakage)		V_O = 0 V to V_{CC}		±10	µA
I_{PP1}	V_{PP} supply current (read/standby)		V_{PP} = V_{PPH}, Read mode		200	µA
			V_{PP} = V_{PPL}		±10	µA
I_{PP2}	V_{PP} supply current (during program pulse) (see Note 4)		V_{PP} = V_{PPH}		30	mA
I_{PP3}	V_{PP} supply current (during flash erase) (see Note 4)		V_{PP} = V_{PPH}		30	mA
I_{PP4}	V_{PP} supply current (during program/erase-verify) (see Note 4)		V_{PP} = V_{PPH}		5.0	mA
I_{CCS}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		1	mA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	µA
I_{CC1}	V_{CC} supply current (active read)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, f = 6 MHz, I_{OUT} = 0 mA		30	mA
I_{CC2}	V_{CC} average supply current (active write) (see Note 4)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, Programming in progress		10	mA
I_{CC3}	V_{CC} average supply current (flash erase) (see Note 4)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, Erasure in progress		15	mA
I_{CC4}	V_{CC} average supply current (program/erase-verify) (see Note 4)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, V_{PP} = V_{PPH}, Program/erase-verify in progress		15	mA
V_{LKO}	V_{CC} erase/write-lockout voltage		V_{PP} = V_{PPH}	2.5		V

NOTE 4: Not 100% tested; characterization data available.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		12	pF

† Capacitance measurements are made on sample basis only.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	ALTERNATE SYMBOL	'28F010B-90		'28F010B-10		'28F010B-12		'28F010B-15		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address, A0–A16	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns	t_{AVQV}		90		100		120		150	ns
$t_{a(E)}$	Access time from chip enable, $\overline{E}$		t_{ELQV}		90		100		120		150	ns
$t_{en(G)}$	Access time from output enable, $\overline{G}$		t_{GLQV}		35		45		50		55	ns
$t_{c(R)}$	Cycle time, read		t_{AVAV}	90		100		120		150		ns
$t_{d(E)}$	Delay time, $\overline{E}$ low to low-Z output		t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-Z output		t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Chip disable time to Hi-Z output		t_{EHQZ}	0	45	0	55	0	55	0	55	ns
$t_{dis(G)}$	Output disable time to Hi-Z output		t_{GHQZ}	0	30	0	30	0	30	0	35	ns
$t_{h(D)}$	Hold time, data valid from address, $\overline{E}$ or $\overline{G}$†		t_{AXQX}	0		0		0		0		ns
$t_{rec(W)}$	Write recovery time before read		t_{WHGL}	6		6		6		6		µs

† Whichever occurs first

timing requirements–write/erase/program operations

PARAMETER		ALTERNATE SYMBOL	'28F010B-90			'28F010B-10			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{W}$	t_{AVAV}	90			100			ns
$t_{c(W)PR}$	Cycle time, programming operation	t_{WHWH1}	10			10			µs
$t_{c(W)ER}$	Cycle time, erase operation	t_{WHWH2}	9.5			9.5	10		ms
$t_{h(A)}$	Hold time, address	t_{WLAX}	40			55			ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0			0			ns
$t_{h(WHD)}$	Hold time, data valid after $\overline{W}$ high	t_{WHDX}	10			10			ns
$t_{su(A)}$	Setup time, address	t_{AVWL}	0			0			ns
$t_{su(D)}$	Setup time, data	t_{DVWH}	40			50			ns
$t_{su(E)}$	Setup time, $\overline{E}$ before $\overline{W}$	t_{ELWL}	15			20			ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ going low	t_{VPEL}	1			1			µs
$t_{rec(W)}$	Recovery time, $\overline{W}$ before read	t_{WHGL}	6			6			µs
$t_{rec(R)}$	Recovery time, read before $\overline{W}$	t_{GHWL}	0			0			µs
$t_{w(W)}$	Pulse duration, $\overline{W}$ (see Note 5)	t_{WLWH}	40			60			ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20			20			ns
$t_{r(VPP)}$	Rise time, V_{PP}	t_{VPPR}	1			1			µs
$t_{f(VPP)}$	Fall time, V_{PP}	t_{VPPF}	1			1			µs

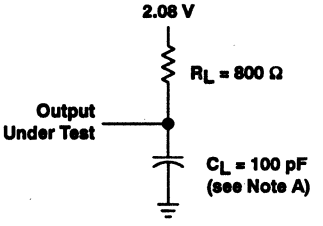
PARAMETER		ALTERNATE SYMBOL	'28F010B-12			'28F010B-15			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{W}$	t_{AVAV}	120			150			ns
$t_{c(W)PR}$	Cycle time, programming operation	t_{WHWH1}	10			10			µs
$t_{c(W)ER}$	Cycle time, erase operation	t_{WHWH2}	9.5	10		9.5	10		ms
$t_{h(A)}$	Hold time, address	t_{WLAX}	60			60			ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0			0			ns
$t_{h(WHD)}$	Hold time, data valid after $\overline{W}$ high	t_{WHDX}	10			10			ns
$t_{su(A)}$	Setup time, address	t_{AVWL}	0			0			ns
$t_{su(D)}$	Setup time, data	t_{DVWH}	50			50			ns
$t_{su(E)}$	Setup time, $\overline{E}$ before $\overline{W}$	t_{ELWL}	20			20			ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ low	t_{VPEL}	1			1			µs
$t_{rec(W)}$	Recovery time, $\overline{W}$ before read	t_{WHGL}	6			6			µs
$t_{rec(R)}$	Recovery time, read before $\overline{W}$	t_{GHWL}	0			0			µs
$t_{w(W)}$	Pulse duration, $\overline{W}$ (see Note 5)	t_{WLWH}	60			60			ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20			20			ns
$t_{r(VPP)}$	Rise time, V_{PP}	t_{VPPR}	1			1			µs
$t_{f(VPP)}$	Fall time, V_{PP}	t_{VPPF}	1			1			µs

NOTE 5: Rise/fall time ≤ 10 ns

timing requirements — alternative $\overline{E}$-controlled writes

PARAMETER		ALTERNATE SYMBOL	'28F010B-90		'28F010B-10		'28F010B-12		'28F010B-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{E}$	t_{AVAV}	90		100		120		150		ns
$t_{c(E)PR}$	Cycle time, programming operation	t_{EHEH}	10		10		10		10		µs
$t_{h(EA)}$	Hold time, address	t_{ELAX}	45		75		80		80		ns
$t_{h(ED)}$	Hold time, data	t_{EHDX}	10		10		10		10		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	0		0		0		0		ns
$t_{su(A)}$	Setup time, address	t_{AVEL}	0		0		0		0		ns
$t_{su(D)}$	Setup time, data	t_{DVEH}	35		50		50		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before $\overline{E}$	t_{WLEL}	0		0		0		0		ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ low	t_{VPEL}	1		1		1		1		µs
$t_{rec(E)R}$	Recovery time, write using $\overline{E}$ before read	t_{EHGL}	6		6		6		6		µs
$t_{rec(E)W}$	Recovery time, read before write using $\overline{E}$	t_{GHEL}	0		0		0		0		µs
$t_{w(E)}$	Pulse duration, write using $\overline{E}$	t_{ELEH}	45		70		70		70		ns
$t_{w(EH)}$	Pulse duration, write, $\overline{E}$ high	t_{EHEL}	20		20		20		20		ns

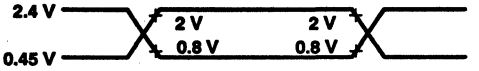
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 4. AC Test Output Load Circuit

AC testing input/output waveforms



AC testing inputs are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} as close as possible to the device pins.

PARAMETER MEASUREMENT INFORMATION

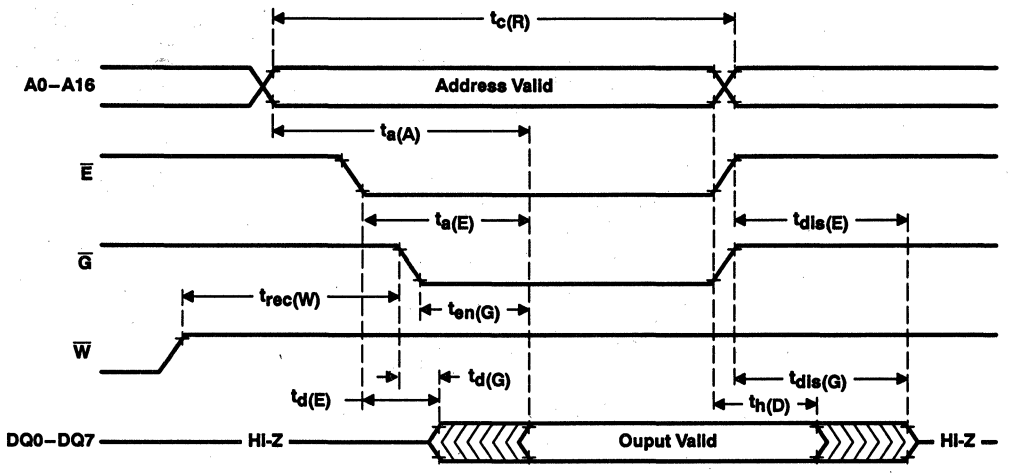


Figure 5. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

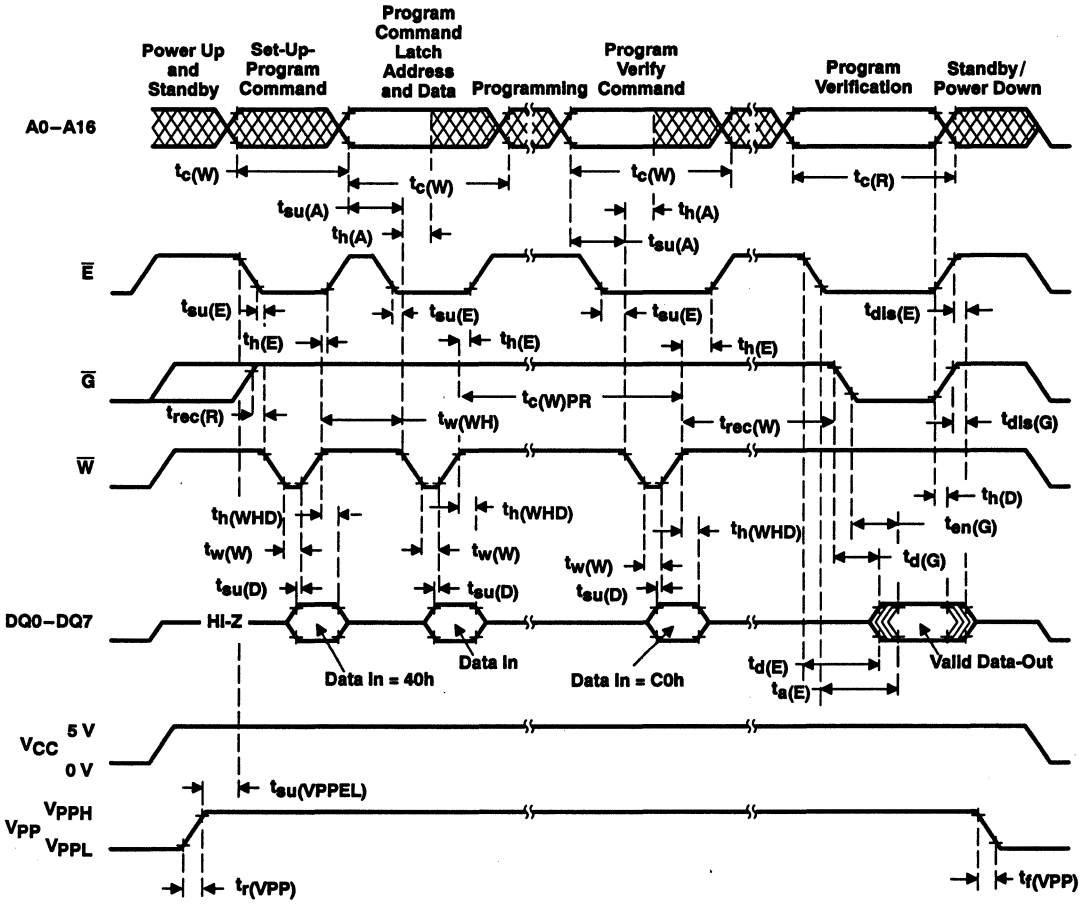


Figure 6. Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

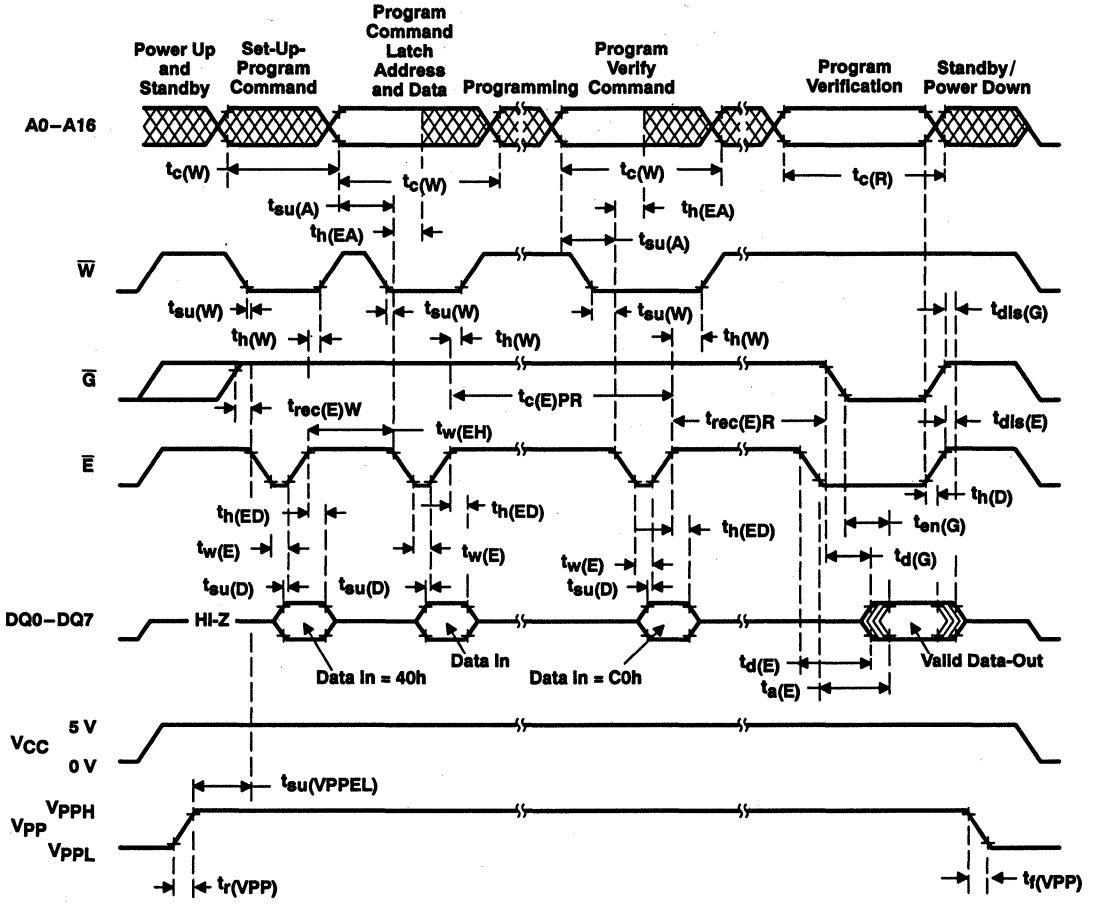


Figure 7. Write-Cycle (Alternative $\overline{E}$-Controlled Writes) Timing

PARAMETER MEASUREMENT INFORMATION

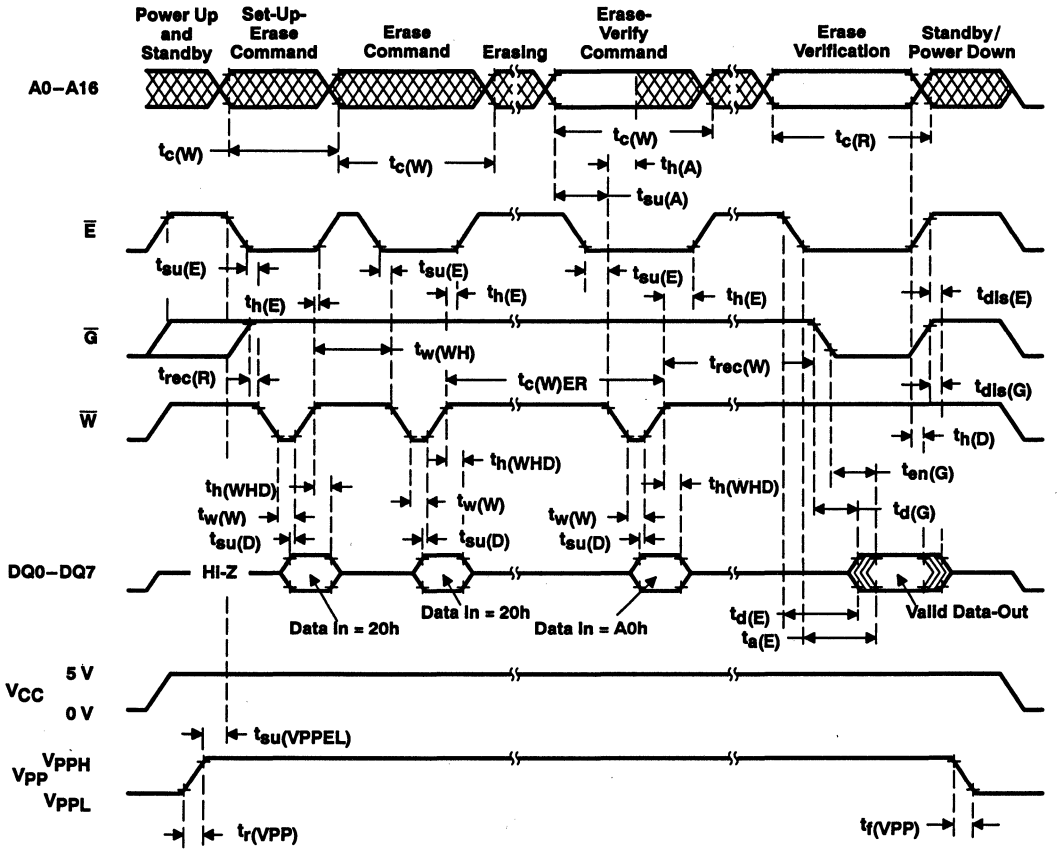


Figure 8. Flash-Erase-Cycle Timing

- **Organization . . . 64K × 16 Flash Memory**
- **Pin Compatible With Existing 1-Megabit EPROMs**
- **All Inputs/Outputs TTL Compatible**
- **V_{CC} Tolerance ±10%**
- **Maximum Access/Minimum Cycle Time**

'28F210-10	100 ns
'28F210-12	120 ns
'28F210-15	150 ns
'28F210-17	170 ns

- **Industry-Standard Programming Algorithm**
- **PEP4 Version Available With 168-Hour Burn-In and Choice of Operating Temperature Ranges**
- **Chip Erase Before Reprogramming**
- **10000 and 1000 Program/Erase Cycles**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **–Active Write . . . 55 mW**
  - **–Active Read . . . 165 mW**
  - **–Electrical Erase . . . 82.5 mW**
  - **–Standby . . . 0.55 mW (CMOS-Input Levels)**
- **Automotive Temperature Range – 40°C to 125°C**

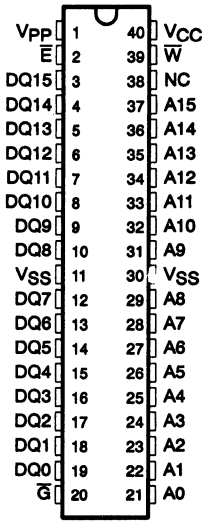
description

The TMS28F210 is a 1048576-bit, programmable read-only memory that can be electrically bulk erased and reprogrammed. It is available in 10000 and 1000 program/erase endurance cycle versions.

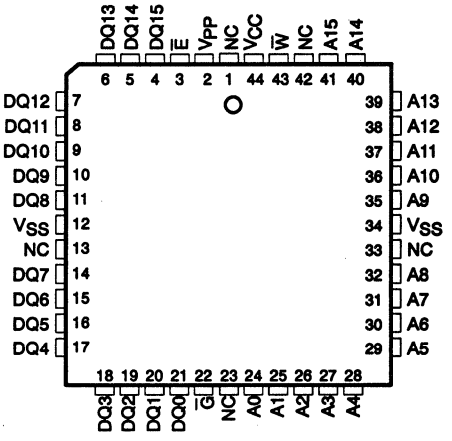
The TMS28F210 flash memory is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2 mm (600-mil) center and a 44-lead plastic leaded-chip carrier package using 1,25 mm (50-mil) lead spacing (FN suffix).

The TMS28F210 is characterized for operation in temperature ranges of 0°C to 70°C (NL and FNL suffixes), –40°C to 85°C (NE and FNE suffixes), and –40°C to 125°C (NQ and FNQ suffixes). All packages are offered with 168-hour burn-in (4 suffix).

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A15	Address Inputs
DQ0–DQ15	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Internal Connection
V_{CC}	5-V Power Supply
V_{SS}	Ground
V_{PP}	12-V Power Supply†
$\overline{W}$	Program

† Only in program mode

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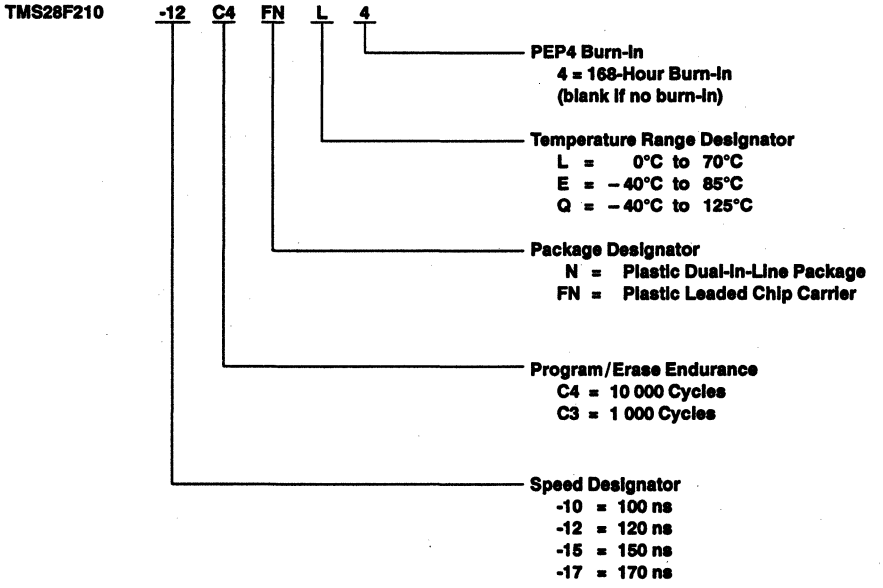
device symbol nomenclature



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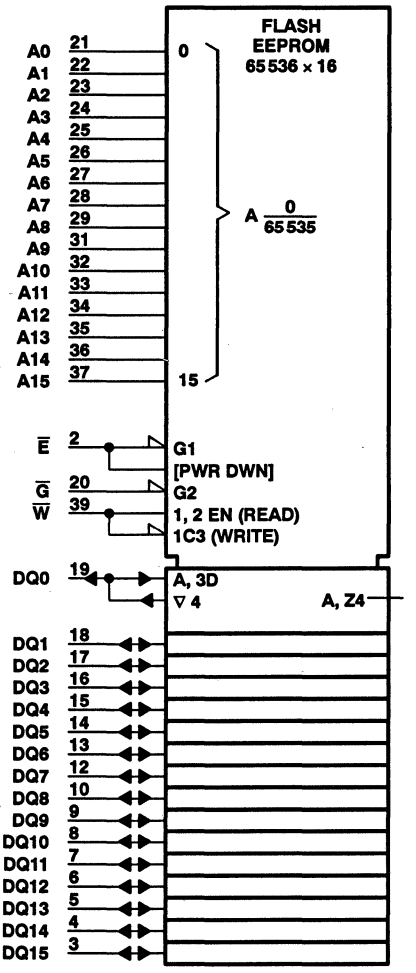
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

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functional block diagram

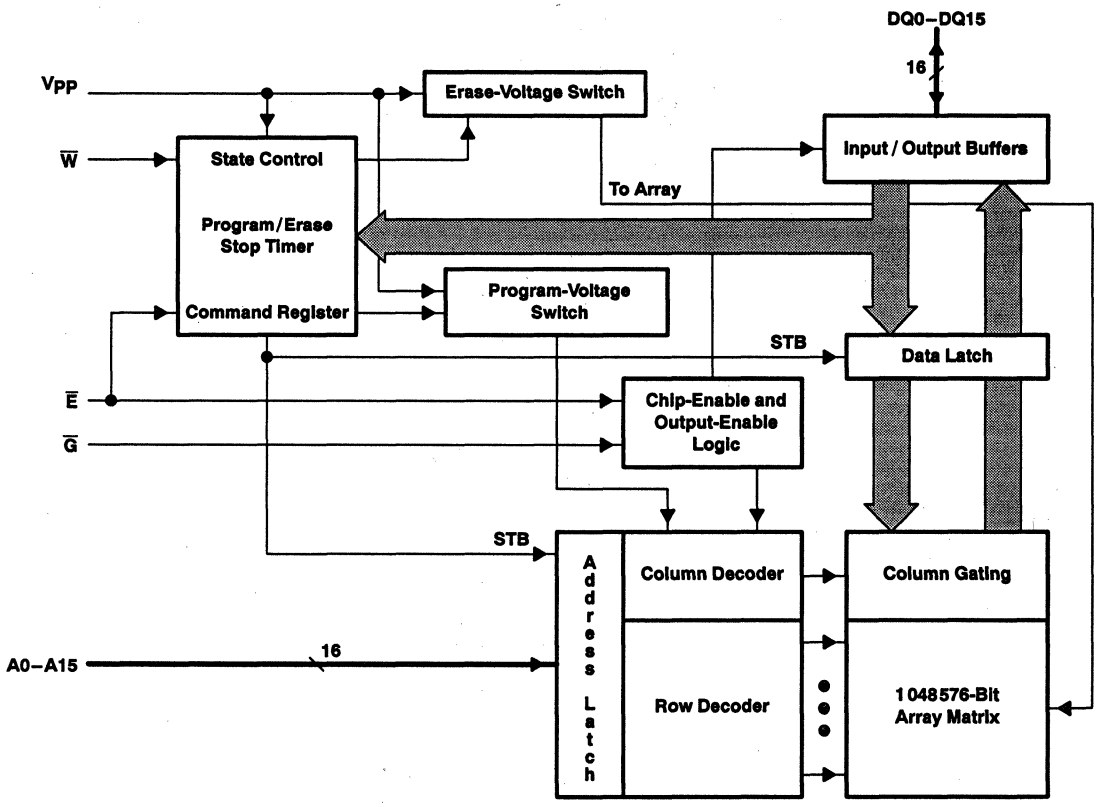

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Table 1. Operation Modes

MODE		FUNCTION†						
	N PACKAGE	V_{PP}‡	$\overline{E}$	$\overline{G}$	A0	A9	$\overline{W}$	DQ0–DQ15
		1	2	20	21	31	39	3–10, 12–19
	FN PACKAGE	2	3	22	24	35	43	21–14, 11–4
Read	Read	V_{PPL}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable	V_{PPL}	V_{IL}	V_{IH}	X	X	V_{IH}	Hi-Z
	Standby and Write Inhibit	V_{PPL}	V_{IH}	X	X	X	X	Hi-Z
	Algorithm-Selection Mode	V_{PPL}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	V_{IH}	Mfr Equivalent Code 0097h
					V_{IH}			Device Equivalent Code 00E5h
Read/ Write	Read	V_{PPH}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IH}	Hi-Z
	Standby and Write Inhibit	V_{PPH}	V_{IH}	X	X	X	X	Hi-Z
	Write	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IL}	Data In

† X can be V_{IL} or V_{IH}.
‡ $V_{PPL} \le V_{CC} + 2$ V; V_{PPH} is the programming voltage specified for the device. For more details, see the recommended operating conditions.

operation

read/output disable

When the outputs of two or more TMS28F210s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of other devices. To read the output of the TMS28F210, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

standby and write inhibit

Active I_{CC} current can be reduced from 50 mA to 1 mA by applying a high TTL level on $\overline{E}$ or to 100 µA with a high CMOS level on $\overline{E}$. In this mode, all outputs are in the high-impedance state. The TMS28F210 draws active current when it is deselected during programming, erasure, or program/erase verification. It continues to draw active current until the operation is terminated.

algorithm-selection mode

The algorithm-selection mode provides access to a binary code identifying the correct programming and erase algorithms. This mode is activated when A9 is forced to V_{ID}. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. A0 low selects the manufacturer-equivalent code 0097h, and A0 high selects the device-equivalent code 00E5h, as shown in the algorithm-selection mode table below:

IDENTIFIER¶	PINS§									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Manufacturer-Equivalent Code	V_{IL}	1	0	0	1	0	1	1	1	0097
Device-Equivalent Code	V_{IH}	1	1	1	0	0	1	0	1	00E5

§ D8–D15 are not shown in the table because the upper 8 data bits read 0.
¶ $\overline{E} = \overline{G}$ = A1–A8 = A10–A15 = V_{IL}, $A_9 = V_{ID}$, $V_{PP} = V_{PPL}$

programming and erasure

In the erased state, all bits are at a logic 1. Before erasing the device, all memory bits must be programmed to a logic 0. Afterwards, the entire chip is erased. At this point, the bits, now logic 1s, can be programmed accordingly. Refer to the Fastwrite and Fasterase algorithms for further detail.

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command register

The command register controls the program and erase functions of the TMS28F210. The algorithm-selection mode can be activated using the command register in addition to the previously described method. When V_{PP} is high, the contents of the command register and the function being performed can be changed. The command register is written to when $\overline{E}$ is low and $\overline{W}$ is pulsed low. The address is latched on the leading edge of the pulse, while the data is latched on the trailing edge. Accidental programming or erasure is minimized because two commands must be executed to invoke either operation.

power supply considerations

Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Changes in current drain on V_{PP} require it to have a bypass capacitor as well. Printed circuit traces for both power supplies should be appropriate to handle the current demand.

Table 2. Command Definitions

COMMAND	REQUIRED BUS CYCLES	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION†	ADDRESS	DATA	OPERATION†	ADDRESS	DATA
Read	1	Write	X	0000h	Read	RA	RD
Algorithm-Selection Mode	3	Write	X	0090h	Read	0000 0001	0097h 00E5h
Set-Up-Erase/Erase	2	Write	X	0020h	Write	X	20h
Erase Verify	2	Write	EA	00A0h	Read	X	EVD
Set-Up-Program/Program	2	Write	X	0040h	Write	PA	PD
Program Verify	2	Write	X	00C0h	Read	X	PVD
Reset	2	Write	X	00FFh	Write	X	00FFh

† Modes of operation are defined in Table 1.

Legend:

EA	Address of memory location to be read during erase verify
RA	Address of memory location to be read
PA	Address of memory location to be programmed. Address is latched on the falling edge of $\overline{W}$.
RD	Data read from location RA during the read operation
EVD	Data read from location EA during erase verify
PD	Data to be programmed at location PA. Data is latched on the rising edge of $\overline{W}$.
PVD	Data read from location PA during program verify

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command definitions

read command

Memory contents can be accessed while V_{PP} is high or low. When V_{PP} is high, writing 0000h into the command register invokes the read operation. When the device is powered up, the default contents of the command register are 0000h and the read operation is enabled. The read operation remains enabled until a different valid command is written to the command register.

algorithm-selection-mode command

The algorithm-selection mode is activated by writing 0090h into the command register. The manufacturer equivalent code (0097h) is identified by the value read from address location 0000h, and the device equivalent code (00E5h) is identified by the value read from address location 0001h.

set-up-program/program commands

The programming algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = V_{PPH}$, and $V_{CC} = 5$ V. To enter the programming mode, write the set-up-program command, 0040h, into the command register. The programming operation is invoked by the next write-enable pulse. Addresses are latched internally on the falling edge of $\overline{W}$, and data is latched internally on the rising edge of $\overline{W}$. The programming operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$ pulse. The program operation requires 10 µs for completion before the program-verify command, 00C0h, can be loaded.

Maximum program timing is controlled by the internal stop timer. When the stop timer terminates the program operation, the device enters an inactive state and remains inactive until a valid program-verify, read, or reset command is received.

program-verify command

The TMS28F210 can be programmed sequentially or randomly because it is programmed one word at a time. Each word must be verified after it is programmed. The program-verify operation prepares the device to verify the most recently programmed word. To invoke the program-verify operation, 00C0h must be written into the command register. The program-verify operation ends on the rising edge of $\overline{W}$.

While verifying a word, the TMS28F210 applies an internal margin voltage to the designated word. If the true data and programmed data match, programming continues to the next designated word location; otherwise, the word must be reprogrammed. Figure 1 shows how commands and bus operations are combined for word programming.

set-up-erase/erase commands

The erase algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = V_{PPH}$, and $V_{CC} = 5$ V. To enter the erase mode, write the set-up-erase command, 0020h, into the command register. After the TMS28F210 is in the erase mode, writing a second erase command, 0020h, into the command register invokes the erase operation. The erase operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$. The erase operation requires 10 ms to complete before the erase-verify command, 00A0h, can be loaded.

Maximum erase timing is controlled by the internal stop timer. When the stop timer terminates the erase operation, the device enters an inactive state and remains inactive until a valid erase-verify, read, or reset command is received.

erase-verify command

All words must be verified following an erase operation. After the erase operation is complete, an erased word can be verified by writing the erase-verify command, 00A0h, into the command register. This command causes the device to exit the erase mode on the rising edge of $\overline{W}$. The address of the word to be verified is latched on the falling edge of $\overline{W}$. The erase-verify operation remains enabled until a valid command is written to the command register.

erase-verify command (continued)

To determine whether or not all the words have been erased, the TMS28F210 applies a margin voltage to each word. If FFFFh is read from the word, all bits in the designated word have been erased. The erase-verify operation continues until all of the words have been verified. If FFFFh is not read from a word, an additional erase operation needs to be executed. Figure 2 shows the combination of commands and bus operations for electrically erasing the TMS28F210.

reset command

To reset the TMS28F210 after set-up-erase command or set-up-program command operations without changing the contents in memory, write 00FFh into the command register two consecutive times. After executing the reset command, a valid command must be written into the command register to change to a new state.

Fastwrite algorithm

The TMS28F210 is programmed using the Texas Instruments Fastwrite algorithm shown in Figure 1. This algorithm programs in a nominal time of two seconds.

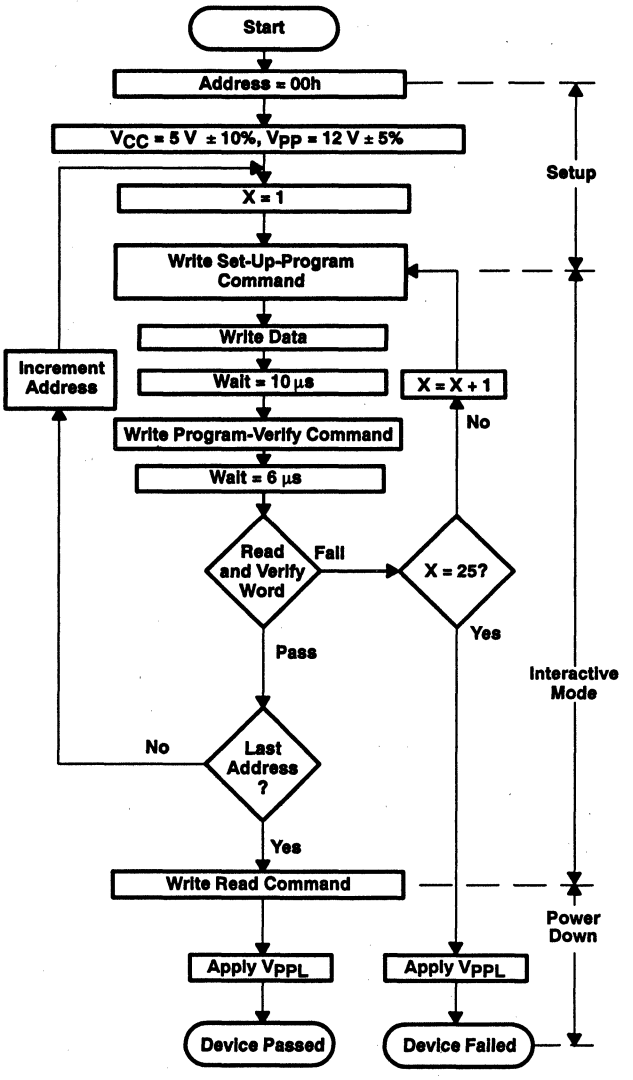
Fasterase algorithm

The TMS28F210 is erased using the Texas Instruments Fasterase algorithm shown in Figure 2. The memory array needs to be completely programmed (using the Fastwrite algorithm) before erasure begins. Erasure typically occurs in one second.

parallel erasure

To reduce total erase time, several devices can be erased in parallel. Since each Flash EEPROM can erase at a different rate, every device must be verified separately after each erase pulse. After a given device has been successfully erased, the erase command should not be issued to this device again. All devices that complete erasure should be masked until the parallel erasure process is finished (see Figure 3).

Examples of how to mask a device during parallel erase include driving the $\overline{E}$ pin high, writing the read command (0000h) to the device when the others receive a set-up-erase or erase command, or disconnecting it from all electrical signals with relays or other types of switches.



Bus Operation	Command	Comments
Initialize Address		
Standby		Wait for Vpp to ramp to V_{PPH} (see Note A)
		Initialize pulse count
Write	Set-Up-Program	Data = 0040h
Write	Write Data	Valid address / data
Standby		Wait = 10 µs
Write	Program-Verify	Data = 00C0h; ends program operation
Standby		Wait = 6 µs
Read		Read word to verify programming; compare output to expected output
Write	Read	Data = 0000h; resets register for read operations
Standby		Wait for Vpp to ramp to V_{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 1. Programming Flowchart: Fastwrite Algorithm

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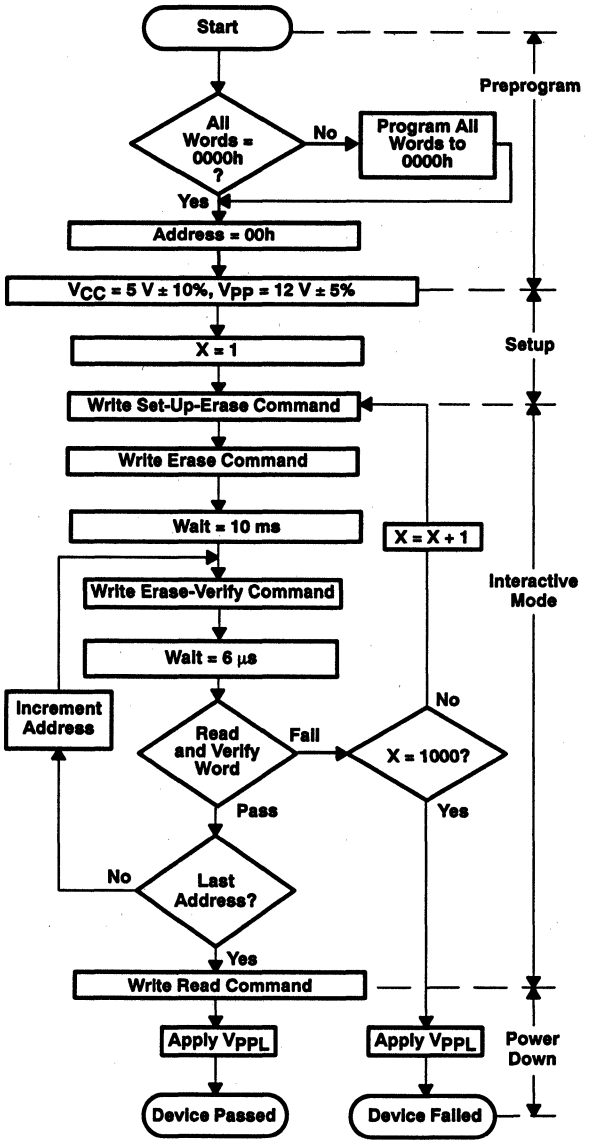
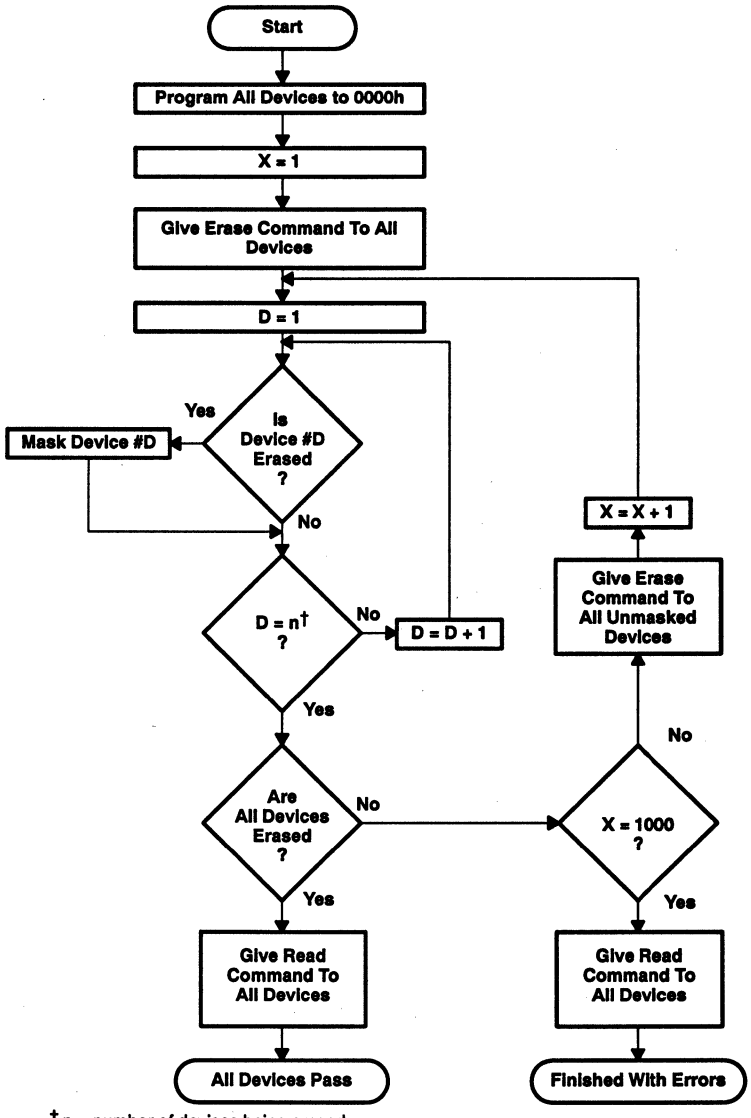


Bus Operation	Command	Comments
		Entire memory must = 0000h before erasure Use Fastwrite programming algorithm
		Initialize addresses
Standby		Wait for V_{PP} to ramp to V_{PPH} (see Note A)
		Initialize pulse count
Write	Set-Up-Erase	Data = 0020h
Write	Erase	Data = 0020h
Standby		Wait = 10 ms
Write	Erase Verify	Addr = Word to verify; data = 00A0h; ends the erase operation
Standby		Wait = 6 µs
Read		Read word to verify erasure; compare output to FFFFh
Write	Read	Data = 0000h; resets register for read operations
Standby		Wait for V_{PP} to ramp to V_{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 2. Flash-Erase Flowchart: Fasterase Algorithm



† n = number of devices being erased

Figure 3. Parallel-Erase Flow Diagram

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –0.6 V to 7 V
Programming supply voltage range, V_{PP} ..... –0.6 V to 14 V
Input voltage range (see Note 2): All inputs except A9 ..... –0.6 V to V_{CC} + 1 V
A9 ..... –0.6 V to 13.5 V
Output voltage range (see Note 3) ..... –0.6 V to V_{CC} + 1 V
Operating free-air temperature range during read/erase/program, T_A
NL, FNL ..... 0°C to 70°C
NE, FNE ..... – 40°C to 85°C
NQ, FNQ ..... – 40° C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to V_{SS}.
2. The voltage on any input can undershoot to –2 V for periods less than 20 ns.
3. The voltage on any output can overshoot to 7 V for periods less than 20 ns.

recommended operating conditions

				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	During write/read/flash erase		4.5	5	5.5	V
V_{PP}	Programming supply voltage	During read only (V_{PPL})		0		V_{CC}+2	V
		During write/read/flash erase (V_{PPH})		11.4	12	12.6	V
V_{ID}	Voltage level on A9 for algorithm-selection mode			11.5		13	V
V_{IH}	High-level dc input voltage		TTL	2		V_{CC}+0.5	V
			CMOS	V_{CC} – 0.5		V_{CC}+0.5	
V_{IL}	Low-level dc input voltage		TTL	–0.5		0.8	V
			CMOS	GND – 0.2		GND+0.2	
T_A	Operating free-air temperature		NL, FNL suffix	0		70	°C
			NE, FNE suffix	– 40		85	
			NQ, FNQ suffix	– 40		125	

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL	$I_{OH} = -2.5$ mA	2.4		V
		CMOS	$I_{OH} = -100$ µA	$V_{CC} - 0.4$		
V_{OL}	Low-level output voltage	TTL	$I_{OL} = 5.8$ mA		0.45	V
		CMOS	$I_{OL} = 100$ µA		0.1	
I_I	Input current (leakage)	All except A9	$V_I = 0$ V to 5.5 V		±1	µA
		A9	$V_I = 0$ V to 13 V		± 200	
I_O	Output current (leakage)		$V_O = 0$ V to V_{CC}		±10	µA
I_{ID}	A9 algorithm-selection-mode current		A9 = V_{ID} max		TBD	mA
I_{PP1}	V_{PP} supply current (read/standby)		$V_{PP} = V_{PPH}$, Read mode		200	µA
			$V_{PP} = V_{PPL}$		±10	µA
I_{PP2}	V_{PP} supply current (during program pulse) (see Note 4)		$V_{PP} = V_{PPH}$		50	mA
I_{PP3}	V_{PP} supply current (during flash erase) (see Note 4)		$V_{PP} = V_{PPH}$		50	mA
I_{PP4}	V_{PP} supply current (during program/erase verify) (see Note 4)		$V_{PP} = V_{PPH}$		5.0	mA
I_{CCS}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$		1	mA
		CMOS-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$		100	µA
I_{CC1}	V_{CC} supply current (active read)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, f = 6 MHz, Outputs open		50	mA
I_{CC2}	V_{CC} average supply current (active write) (see Note 4)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, Programming in progress		10	mA
I_{CC3}	V_{CC} average supply current (flash erase) (see Note 4)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, Erasure in progress		15	mA
I_{CC4}	V_{CC} average supply current (program/erase verify) (see Note 4)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, $V_{PP} = V_{PPH}$, Program/erase verify in progress		15	mA

NOTE 4: Not 100% tested; characterization data available

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_I	Input capacitance	$V_I = 0$ V, f = 1 MHz		6	pF
C_O	Output capacitance	$V_O = 0$ V, f = 1 MHz		12	pF

† Capacitance measurements are made on sample basis only.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

		TEST CONDITIONS	ALTERNATE SYMBOL	'28F210-10		'28F210-12		'28F210-15		'28F210-17		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns	t_{AVQV}		100		120		150		170	ns
$t_{a(E)}$	Access time from $\overline{E}$		t_{ELQV}		100		120		150		170	ns
$t_{a(G)}$	Access time from $\overline{G}$		t_{GLQV}		45		50		55		60	ns
$t_{c(R)}$	Cycle time, read		t_{AVAV}	100		120		150		170		ns
$t_{d(E)}$	Delay time, chip enable low to low-Z output		t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-Z output		t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Chip disable to Hi-Z output		t_{EHQZ}	0	55	0	55	0	55	0	55	ns
$t_{dis(G)}$	Hold time, output enable to Hi-Z output		t_{GHQZ}	0	30	0	30	0	35	0	35	ns
$t_{h(D)}$	Hold time, data valid from address, $\overline{E}$, or $\overline{G}$†		t_{AXQX}	0		0		0		0		ns
$t_{rec(W)}$	Write recovery time before read		t_{WHGL}	6		6		6		6		µs

† Whichever occurs first

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timing requirements—write/erase/program operations

		ALTERNATE SYMBOL	'28F210-10			'28F210-12			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{W}$	t_{AVAV}	100			120			ns
$t_{c(W)PR}$	Cycle time, programming operation	t_{WHWH1}	10			10			µs
$t_{c(W)ER}$	Cycle time, erase operation	t_{WHWH2}	9.5	10		9.5	10		ms
$t_{h(A)}$	Hold time, address	t_{WLAX}	55			60			ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0			0			ns
$t_{h(WHD)}$	Hold time, data valid after $\overline{W}$ high	t_{WHDX}	10			10			ns
$t_{su(A)}$	Setup time, address	t_{AVWL}	0			0			ns
$t_{su(D)}$	Setup time, data	t_{DVWH}	50			50			ns
$t_{su(E)}$	Setup time, $\overline{E}$ before $\overline{W}$	t_{ELWL}	20			20			ns
$t_{su(EHVPP)}$	Setup time, $\overline{E}$ high to V_{PP} ramp	t_{EHVP}	100			100			ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ low	t_{VPEL}	1			1			µs
$t_{rec(W)}$	Recovery time, $\overline{W}$ before read	t_{WHGL}	6			6			µs
$t_{rec(R)}$	Recovery time, read before $\overline{W}$	t_{GHWL}	0			0			µs
$t_{w(W)}$	Pulse duration, $\overline{W}$ (see Note 5)	t_{WLWH}	60			60			ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20			20			ns
$t_{r(VPP)}$	Rise time, V_{PP}	t_{VPPR}	1			1			µs
$t_{f(VPP)}$	Fall time, V_{PP}	t_{VPPF}	1			1			µs

		ALTERNATE SYMBOL	'28F210-15			'28F210-17			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{W}$	t_{AVAV}	150			170			ns
$t_{c(W)PR}$	Cycle time, programming operation	t_{WHWH1}	10			10			µs
$t_{c(W)ER}$	Cycle time, erase operation	t_{WHWH2}	9.5	10		9.5	10		ms
$t_{h(A)}$	Hold time, address	t_{WLAX}	60			70			ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0			0			ns
$t_{h(WHD)}$	Hold time, data valid after $\overline{W}$ high	t_{WHDX}	10			10			ns
$t_{su(A)}$	Setup time, address	t_{AVWL}	0			0			ns
$t_{su(D)}$	Setup time, data	t_{DVWH}	50			50			ns
$t_{su(E)}$	Setup time, $\overline{E}$ before $\overline{W}$	t_{ELWL}	20			20			ns
$t_{su(EHVPP)}$	Setup time, $\overline{E}$ high to V_{PP} ramp	t_{EHVP}	100			100			ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ low	t_{VPEL}	1			1			µs
$t_{rec(W)}$	Recovery time, $\overline{W}$ before read	t_{WHGL}	6			6			µs
$t_{rec(R)}$	Recovery time, read before $\overline{W}$	t_{GHWL}	0			0			µs
$t_{w(W)}$	Pulse duration, $\overline{W}$ (see Note 5)	t_{WLWH}	60			60			ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20			20			ns
$t_{r(VPP)}$	Rise time, V_{PP}	t_{VPPR}	1			1			µs
$t_{f(VPP)}$	Fall time, V_{PP}	t_{VPPF}	1			1			µs

NOTE 5: Rise/fall time ≤ 10 ns.

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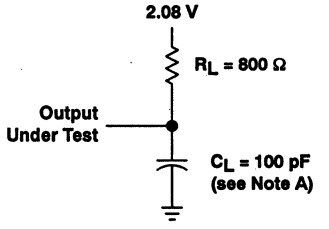
timing requirements—alternative $\overline{E}$-controlled writes

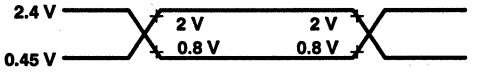
		ALTERNATE SYMBOL	'28F210-10		'28F210-12		'28F210-15		'28F210-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{E}$	t_{AVAV}	100		120		150		170		ns
$t_{c(E)PR}$	Cycle time, programming operation	t_{EHEH}	10		10		10		10		µs
$t_{h(EA)}$	Hold time, address	t_{ELAX}	75		80		80		90		ns
$t_{h(ED)}$	Hold time, data	t_{EHDX}	10		10		10		10		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	0		0		0		0		ns
$t_{su(A)}$	Setup time, address	t_{AVEL}	0		0		0		0		ns
$t_{su(D)}$	Setup time, data	t_{DVEH}	50		50		50		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before $\overline{E}$	t_{WLEL}	0		0		0		0		ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ low	t_{VPEL}	1		1		1		1		µs
$t_{rec(E)R}$	Recovery time, write using $\overline{E}$ before read	t_{EHGL}	6		6		6		6		µs
$t_{rec(E)W}$	Recovery time, read before write using $\overline{E}$	t_{GHEL}	0		0		0		0		µs
$t_{w(E)}$	Pulse duration, write using $\overline{E}$	t_{ELEH}	70		70		70		80		ns
$t_{w(EH)}$	Pulse duration, write, $\overline{E}$ high	t_{EHEL}	20		20		20		20		ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.



VOLTAGE WAVEFORMS

Figure 4. Load Circuit and Voltage Waveforms

AC testing inputs are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} as close as possible to the device pins.

PARAMETER MEASUREMENT INFORMATION

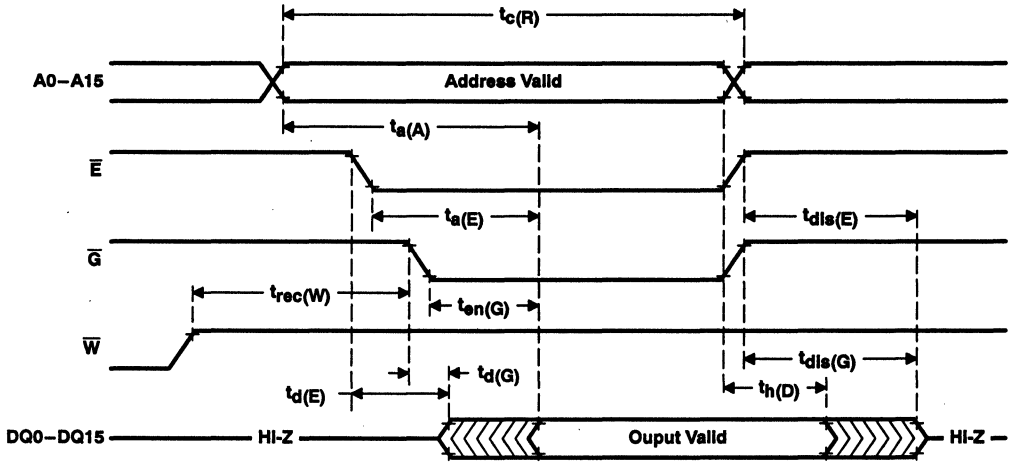


Figure 5. Read-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

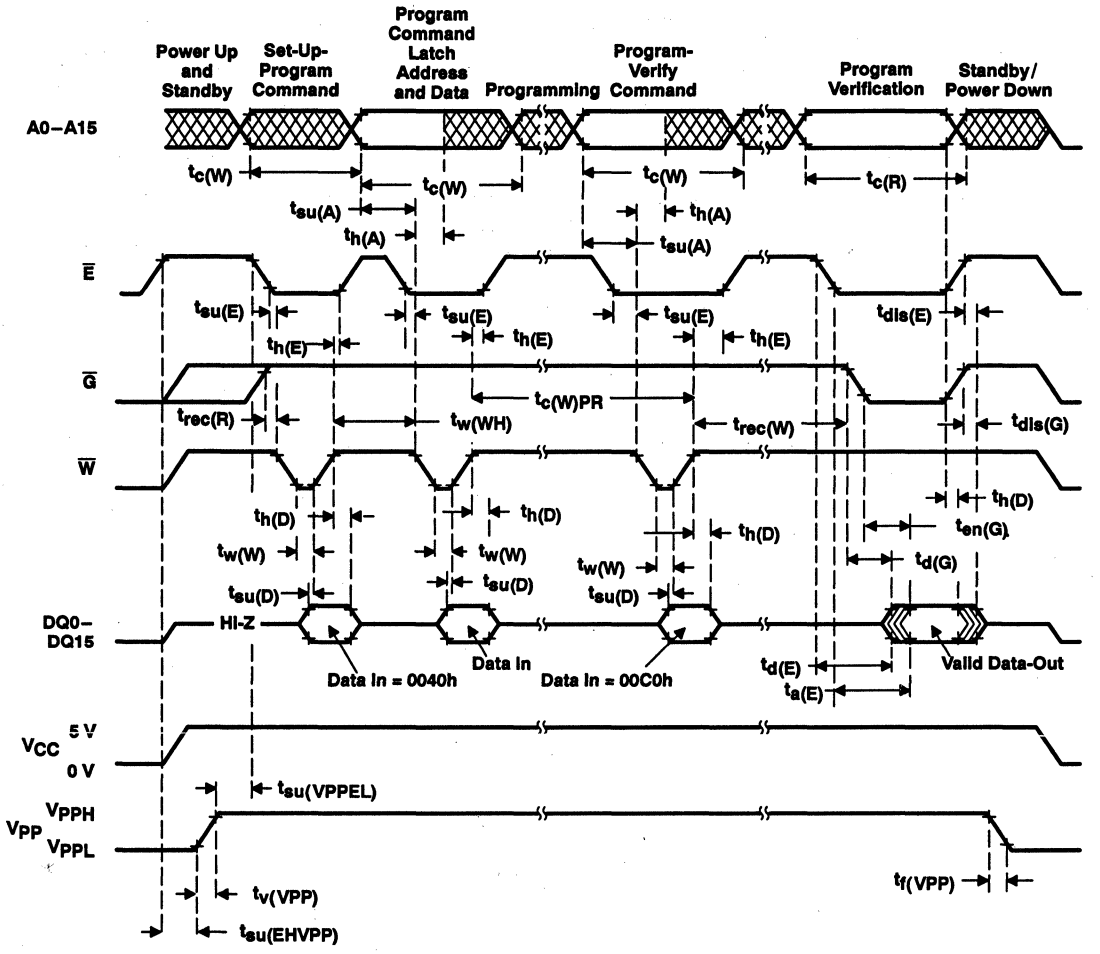


Figure 6. Write-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

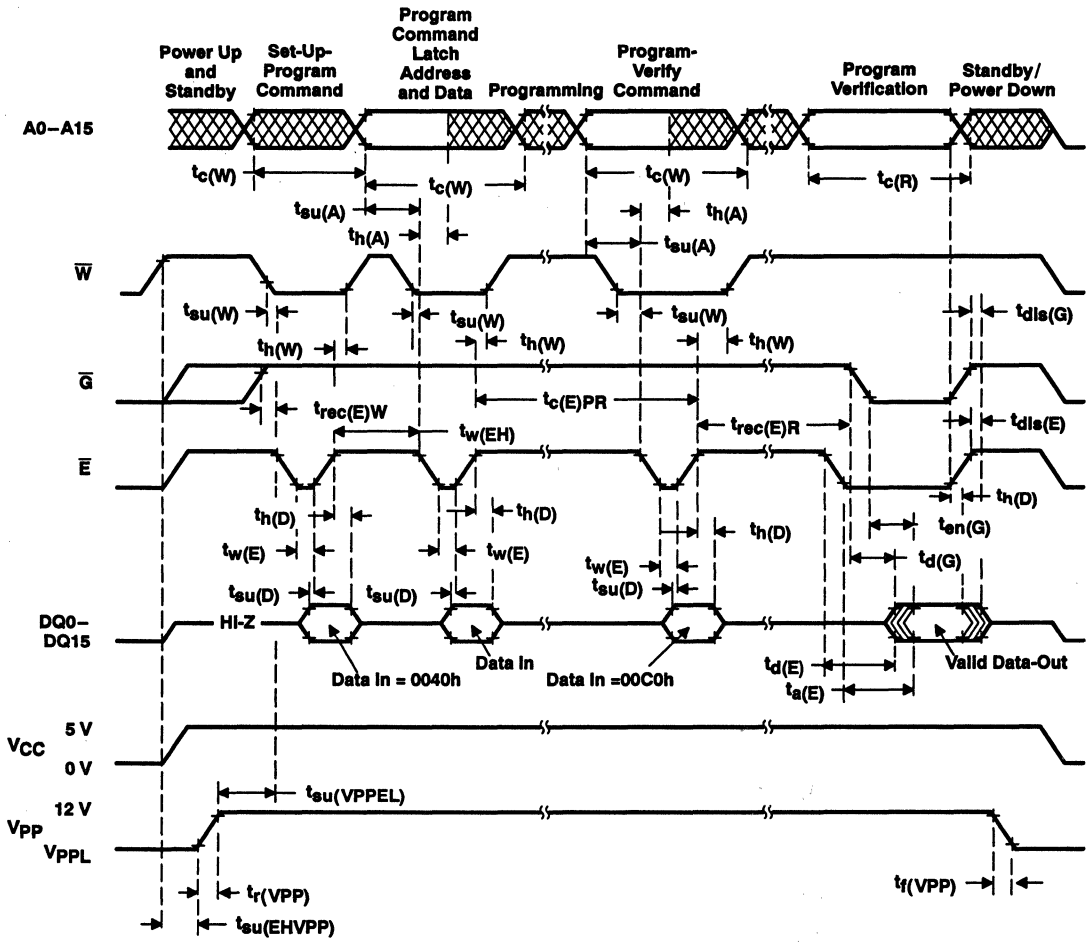


Figure 7. Write-Cycle (Alternative $\overline{E}$-Controlled Writes) Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

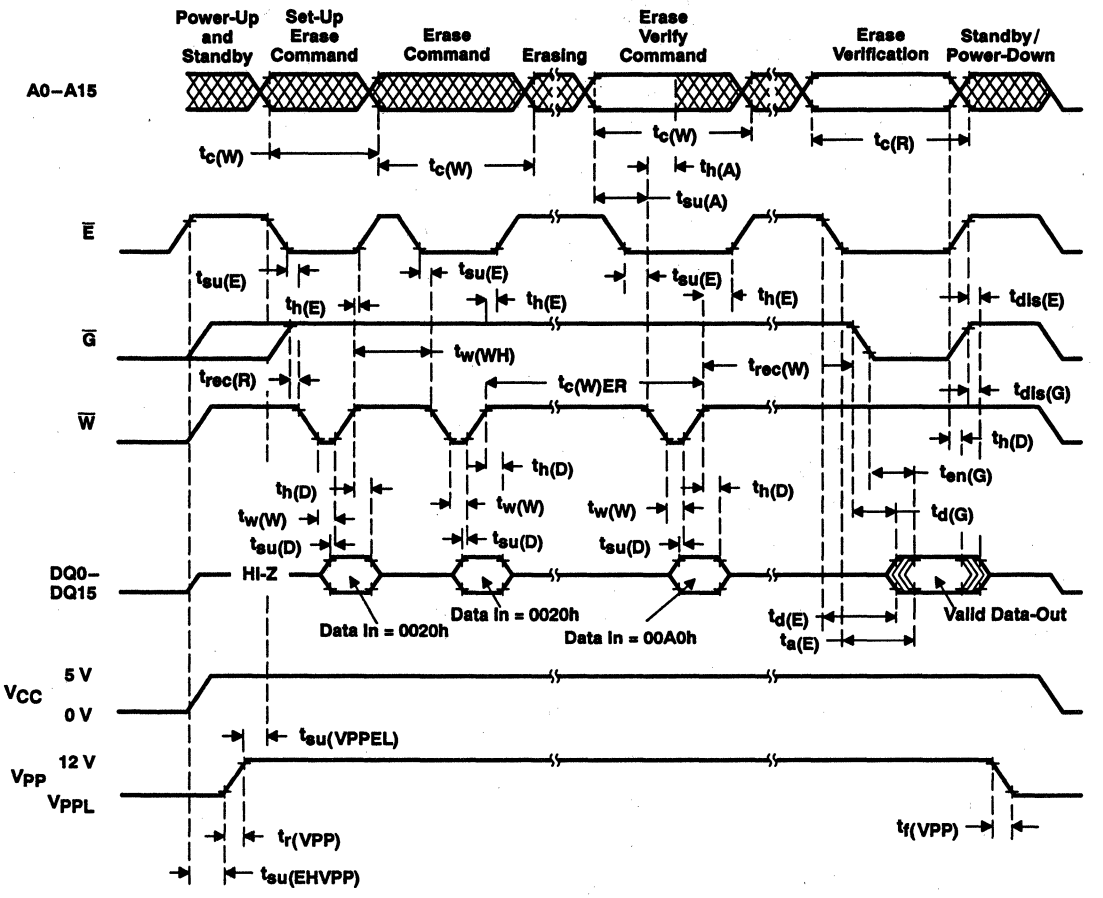


Figure 8. Flash-Erase-Cycle Timing

PRODUCT PREVIEW

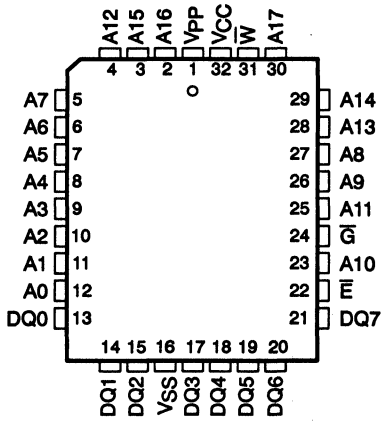
SMJS020B – OCTOBER 1994 – REVISED JUNE 1995

- Organization . . . 256K × 8-Bits
- Pin Compatible With Existing 2-Megabit EPROMs
- V_{CC} Tolerance ±10%
- All Inputs/Outputs TTL Compatible
- Maximum Access/Minimum Cycle Time

'28F020-10	100 ns
'28F020-12	120 ns
'28F020-15	150 ns
'28F020-17	170 ns

- Industry-Standard Programming Algorithm
- PEP4 Version Available With 168-Hour Burn-In and Choice of Operating Temperature Ranges
- 100000 and 10000 Program/Erase-Cycle Versions Available
- Latchup Immunity of 250 mA on All Input and Output Lines
- Low Power Dissipation (V_{CC} = 5.5 V)
  - Active Write . . . 55 mW
  - Active Read . . . 165 mW
  - Electrical Erase . . . 82.5 mW
  - Standby . . . 0.55 mW (CMOS-Input Levels)
- Automotive Temperature Range – 40°C to 125°C

FM PACKAGE
(TOP VIEW)



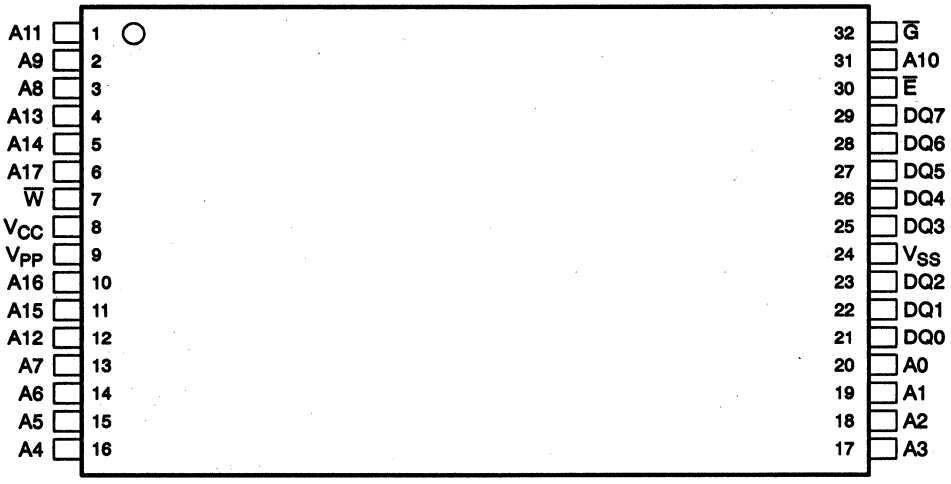
PIN NOMENCLATURE	
A0–A17	Address Inputs
DQ0–DQ7	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	5-V Power Supply
V_{PP}	12-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS28F020 flash memory is a 2097152-bit, programmable read-only memory that can be electrically bulk-erased and reprogrammed. It is available in 100000 and 10000 program/erase-endurance-cycle versions.

The TMS28F020 is offered in a 32-lead plastic leaded chip-carrier package using 1,25-mm (50-mil) lead spacing (FM suffix) and a 32-lead thin small-outline package (DD suffix).

DD PACKAGE
(TOP VIEW)



device symbol nomenclature

TMS28F020 -12 C5 FM L 4

PEP4 Burn-In
4 = 168 Hour Burn-In
(blank if no burn-in)

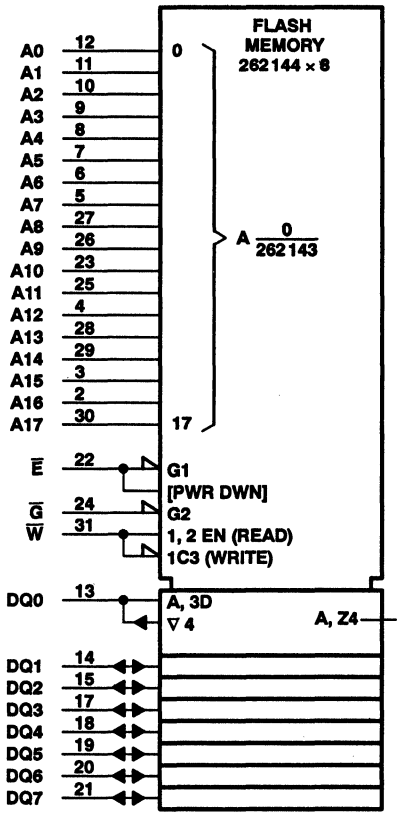
Temperature Range Designator
L = 0°C to 70°C
E = –40°C to 85°C
Q = –40°C to 125°C

Package Designator
FM = Plastic Leaded Chip-Carrier
DD = Thin Small-Outline Package

Program/Erase Endurance
C5 = 100000 Cycles
C4 = 10000 Cycles

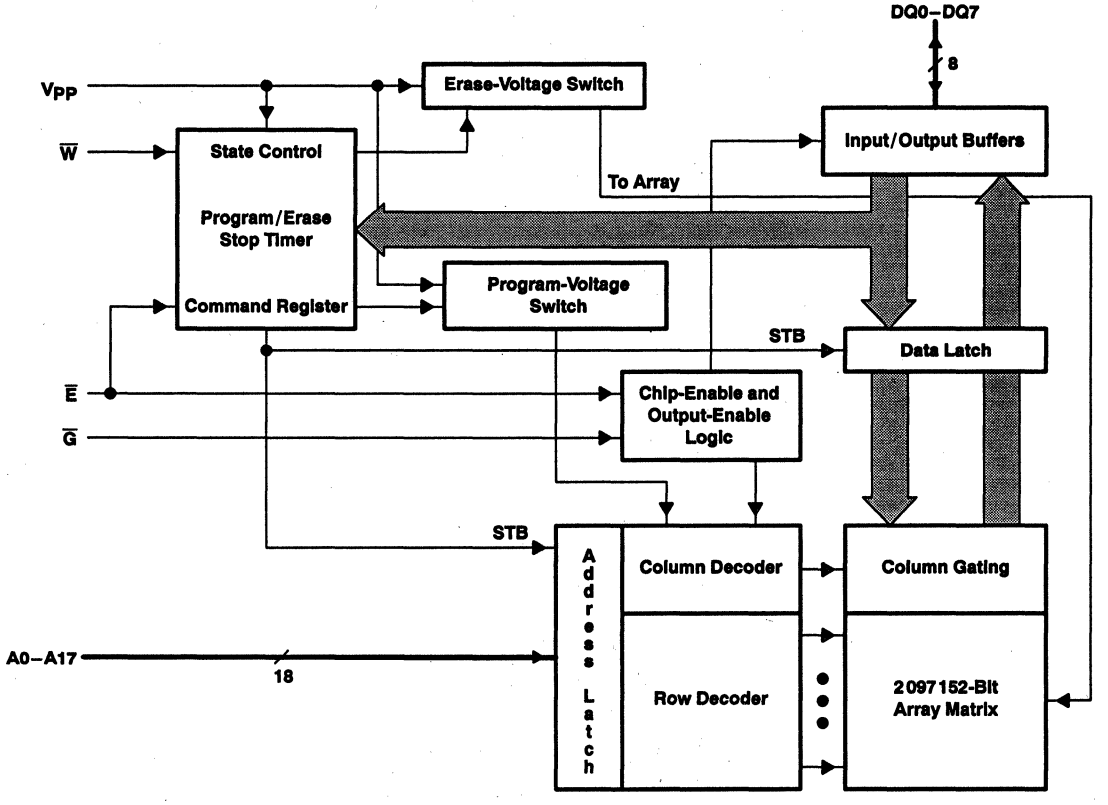
Speed Designator
-10 = 100 ns
-12 = 120 ns
-15 = 150 ns
-17 = 170 ns

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FM package.

functional block diagram



operation

The operation of the TMS28F020 is fully summarized in Table 1 with required signal levels shown for each operation. The sections following the table describe operations in detail.

Table 1. Operation Modes

MODE		FUNCTION†						
		V_{PP}‡ (1)	$\overline{E}$ (22)	$\overline{G}$ (24)	A0 (12)	A9 (26)	$\overline{W}$ (31)	DQ0–DQ7 (13–15, 17–21)
Read	Read	V_{PPL}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable	V_{PPL}	V_{IL}	V_{IH}	X	X	V_{IH}	Hi-Z
	Standby and Write Inhibit	V_{PPL}	V_{IH}	X	X	X	X	Hi-Z
	Algorithm-Selection Mode	V_{PPL}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	V_{IH}	Mfr-Equivalent Code 89h
					V_{IH}			Device-Equivalent Code BDh
Read/ Write	Read	V_{PPH}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IH}	Hi-Z
	Standby and Write Inhibit	V_{PPH}	V_{IH}	X	X	X	X	Hi-Z
	Write	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IL}	Data In

† X can be V_{IL} or V_{IH}.
‡ $V_{PPL} \le V_{CC} + 2$ V; V_{PPH} is the programming voltage specified for the device. For more details, refer to the recommended operating conditions.

read/output disable

When the outputs of two or more TMS28F020s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of other devices. To read the output of the TMS28F020, a low-level signal is applied to $\overline{E}$ and $\overline{G}$. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these terminals.

standby and write inhibit

Active I_{CC} current can be reduced from 30 mA to 1 mA by applying a high TTL level on $\overline{E}$ or to 100 µA with a high CMOS level on $\overline{E}$. In this mode, all outputs are in the high-impedance state. The TMS28F020 draws active current when it is deselected during programming, erasure, or program/erase verification. It continues to draw active current until the operation is terminated.

algorithm-selection mode

The algorithm-selection mode provides access to a binary code identifying the correct programming and erase algorithms. This mode is activated when A9 is forced to V_{ID}. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. A0 low selects the manufacturer-equivalent code 89h, and A0 high selects the device-equivalent code BDh, as shown in the algorithm-selection mode table below:

IDENTIFIER§	TERMINALS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Manufacturer-Equivalent Code	V_{IL}	1	0	0	0	1	0	0	1	89
Device-Equivalent Code	V_{IH}	1	0	1	1	1	1	0	1	BD

§ $\overline{E} = \overline{G} = V_{IL}$, A1–A8 = V_{IL}, A9 = V_{ID}, A10–A17 = V_{IL}, $V_{PP} = V_{PPL}$.

programming and erasure

In the erased state, all bits are at a logic 1. Before erasing the device, all memory bits must be programmed to a logic 0. Afterward, the entire chip is erased. At this point, the bits, now logic 1s, can be programmed accordingly (refer to the Fastwrite and Fasterase algorithms for further detail).

command register

The command register controls the program and erase functions of the TMS28F020. The algorithm-selection mode can be activated using the command register in addition to the method described in the algorithm-selection mode section. When V_{PP} is high, the contents of the command register and the function being performed can be changed. The command register is written to when $\overline{E}$ is low and $\overline{W}$ is pulsed low. The address is latched on the leading edge of the pulse and the data is latched on the trailing edge. Accidental programming or erasure is minimized because two commands must be executed to invoke either operation. The command register is inhibited when V_{CC} is below the erase/write lockout voltage, V_{LKO}.

power supply considerations

Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Changes in current drain on V_{PP} require it to have a bypass capacitor to V_{SS} as well. Printed-circuit traces for both power supplies should be appropriate to handle the current demand.

Table 2. Command Definitions

COMMAND	REQUIRED BUS CYCLES	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION†	ADDRESS	DATA	OPERATION†	ADDRESS	DATA
Read	1	Write	X	00h	Read	RA	RD
Algorithm-Selection Mode	3	Write	X	90h	Read	00000 00001	89h BDh
Set-Up-Erase/Erase	2	Write	X	20h	Write	X	20h
Erase Verify	2	Write	EA	A0h	Read	X	EVD
Set-Up-Program/Program	2	Write	X	40h	Write	PA	PD
Program Verify	2	Write	X	C0h	Read	X	PVD
Reset	2	Write	X	FFh	Write	X	FFh

† Modes of operation are defined in Table 1.

Legend:

EA Address of memory location to be read during erase verify
RA Address of memory location to be read
PA Address of memory location to be programmed. Address is latched on the falling edge of $\overline{W}$.
RD Data read from location RA during the read operation
EVD Data read from location EA during erase verify
PD Data to be programmed at location PA. Data is latched on the rising edge of $\overline{W}$.
PVD Data read from location PA during program verify

command definitions

read command

Memory contents can be accessed while V_{PP} is high or low. When V_{PP} is high, writing 00h into the command register invokes the read operation. When the device is powered up, the default contents of the command register are 00h and the read operation is enabled. The read operation remains enabled until a different valid command is written to the command register.

algorithm-selection-mode command

The algorithm-selection mode is activated by writing 90h into the command register. The manufacturer-equivalent code (89h) is identified by the value read from address location 00000h, and the device-equivalent code (BDh) is identified by the value read from address location 00001h.

set-up-erase/erase commands

The erase algorithm begins with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = V_{PPH}$, and $V_{CC} = 5$ V. To enter the erase mode, write the set-up-erase command, 20h, into the command register. Writing a second erase command, 20h, into the command register invokes the erase operation. The erase operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$. The erase operation requires 10 ms to complete before the erase-verify command, A0h, can be loaded.

Maximum erase timing is controlled by the internal stop timer. When the stop timer terminates the erase operation, the device enters an inactive state and remains inactive until a command is received.

erase-verify command

All bytes must be verified following an erase operation. After the erase operation is complete, an erased byte can be verified by writing the erase-verify command, A0h, into the command register. This command causes the device to exit the erase mode on the rising edge of $\overline{W}$. The address of the byte to be verified is latched on the falling edge of $\overline{W}$. The erase-verify operation remains enabled until a command is written to the command register.

To determine whether or not all the bytes have been erased, the TMS28F020 applies a margin voltage to each byte. If FFh is read from the byte, all bits in the designated byte have been erased. The erase-verify operation continues until all of the bytes have been verified. If FFh is not read from a byte, an additional erase operation must be executed. Figure 1 shows the combination of commands and bus operations for electrically erasing the TMS28F020.

set-up-program/program commands

The programming algorithm begins with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = V_{PPH}$, and $V_{CC} = 5$ V. To enter the programming mode, write the set-up-program command, 40h, into the command register. The programming operation is invoked by the next write-enable pulse. Addresses are latched internally on the falling edge of $\overline{W}$, and data is latched internally on the rising edge of $\overline{W}$. The programming operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$ pulse. The program operation requires 10 µs for completion before the program-verify command, C0h, can be loaded.

Maximum program timing is controlled by the internal stop timer. When the stop timer terminates the program operation, the device enters an inactive state and remains inactive until a command is received.

program-verify command

The TMS28F020 can be programmed sequentially or randomly because it is programmed one byte at a time. Each byte must be verified after it is programmed. The program-verify operation prepares the device to verify the most recently programmed byte. To invoke the program-verify operation, C0h must be written into the command register. The program-verify operation ends on the rising edge of $\overline{W}$.

While verifying a byte, the TMS28F020 applies an internal margin voltage to the designated byte. If the true data and programmed data match, programming continues to the next designated byte location; otherwise, the byte must be reprogrammed. Figure 2 shows how commands and bus operations are combined for byte programming.

reset command

To reset the TMS28F020 after set-up-erase command or set-up-program command operations without changing the contents in memory, write FFh into the command register two consecutive times. After executing the reset command, the device will default to the read mode.

Fastwrite algorithm

The TMS28F020 is programmed using the Texas Instruments Fastwrite algorithm shown in Figure 2. This algorithm programs in a nominal time of four seconds.

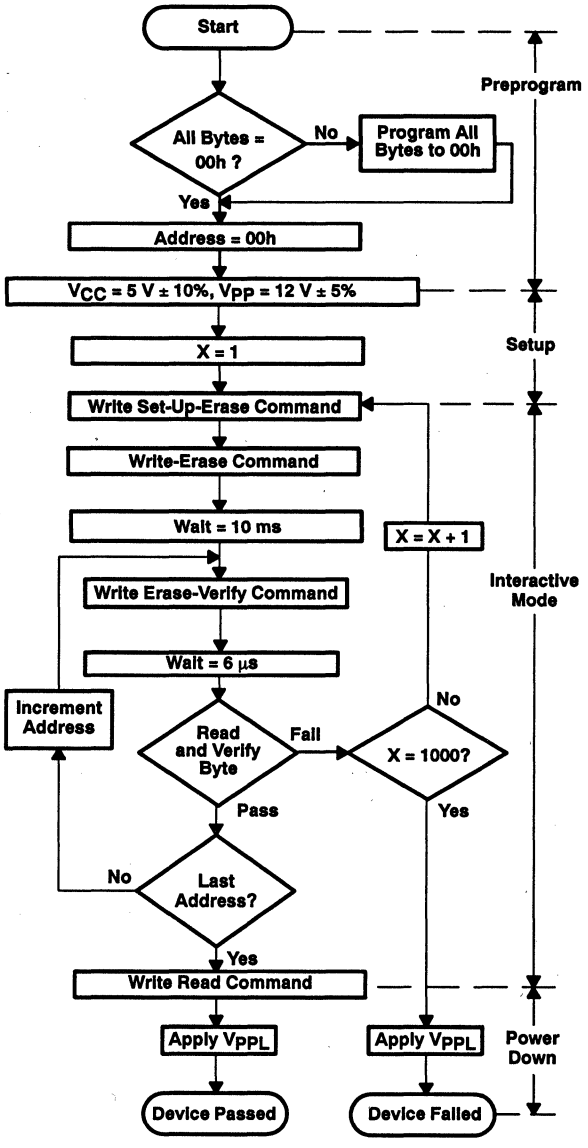
Fasterase algorithm

The TMS28F020 is erased using the Texas Instruments Fasterase algorithm shown in Figure 1. The memory array needs to be completely programmed (using the Fastwrite algorithm) before erasure begins. Erasure typically occurs in two seconds.

parallel erasure

To reduce total erase time, several devices can be erased in parallel. Since each Flash memory can erase at a different rate, every device must be verified separately after each erase pulse. After a given device has been successfully erased, the erase command should not be issued to this device again for this erase cycle. All devices that complete erasure should be masked until the parallel erasure process is finished (see Figure 3).

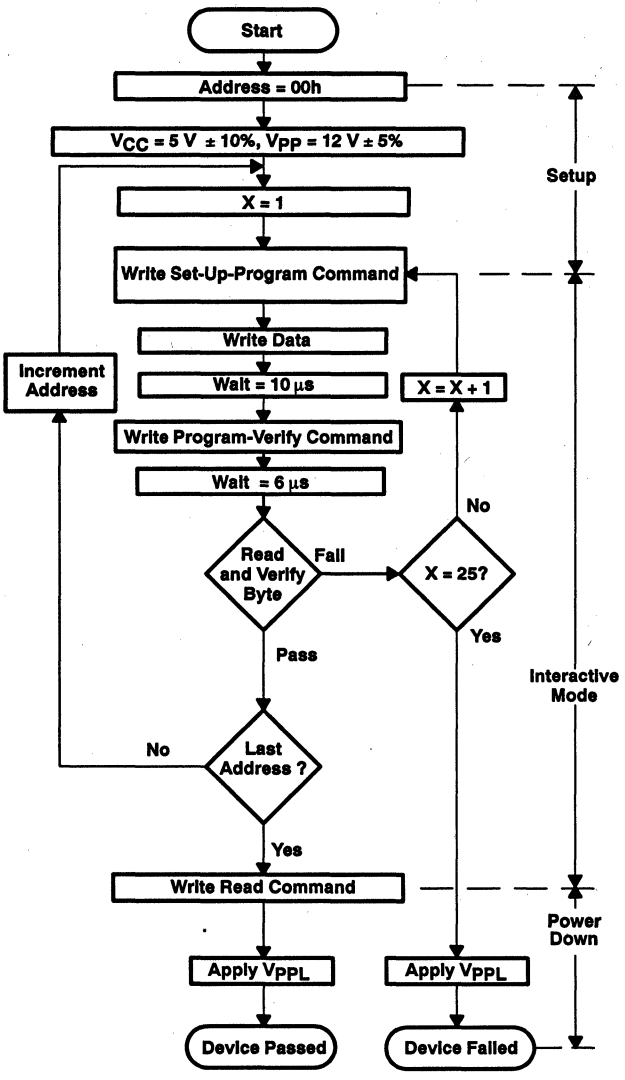
Examples of how to mask a device during parallel erase include driving $\overline{E}$ high, writing the read command (00h) to the device when the others receive a set-up-erase or erase command, or disconnecting it from all electrical signals with relays or other types of switches.



Bus Operation	Command	Comments
		Entire memory must = 00h before erasure Use Fastwrite programming algorithm
		Initialize addresses
Standby		Wait for V_{PP} to ramp to V_{PPH} (see Note A)
		Initialize pulse count
Write	Set-Up-Erase	Data = 20h
Write	Erase	Data = 20h
Standby		Wait = 10 ms
Write	Erase Verify	Addr = Byte to verify; Data = A0h; ends the erase operation
Standby		Wait = 6 µs
Read		Read byte to verify erasure; compare output to FFh
Write	Read	Data = 00h; resets register for read operations
Standby		Wait for V_{PP} to ramp to V_{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

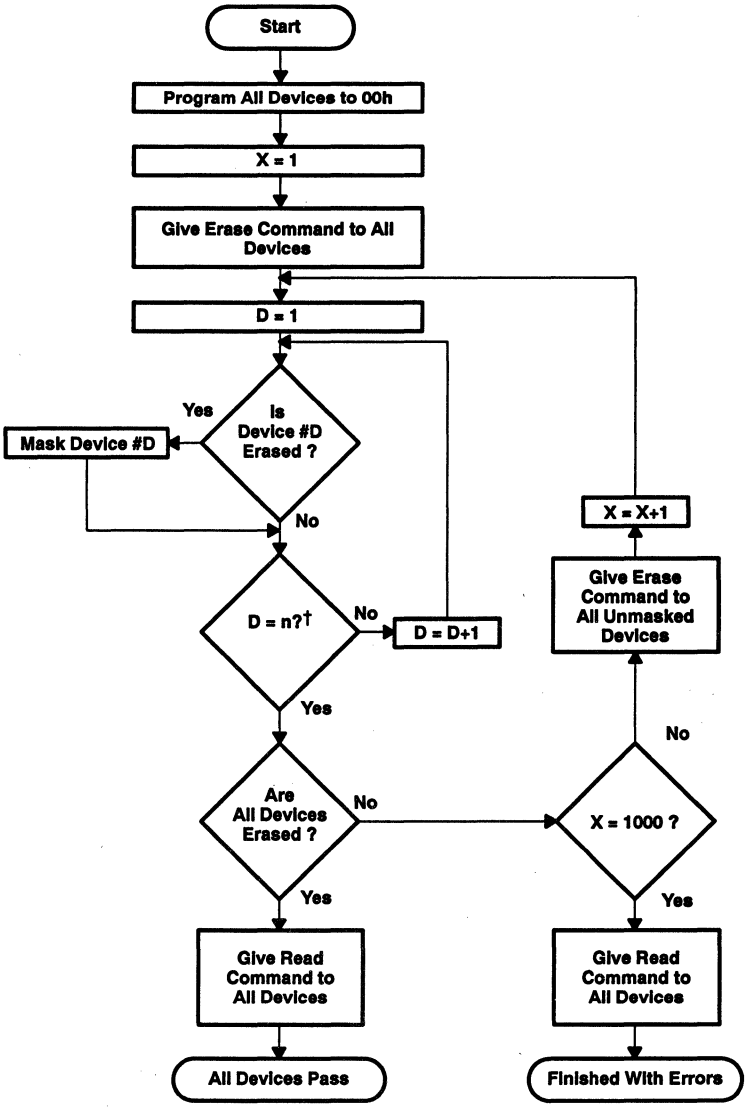
Figure 1. Flash-Erase Flowchart: Fasterase Algorithm



Bus Operation	Command	Comments
Initialize Address		
Standby		Wait for V_{PP} to ramp to V_{PPH} (see Note A)
		Initialize pulse count
Write	Set-Up-Program Write	Data = 40h
Write	Write Data	Valid address/data
Standby		Wait = 10 µs
Write	Program Verify	Data = C0h; ends Program operation
Standby		Wait = 6 µs
Read		Read byte to verify Programming; compare output to expected output
Write	Read	Data = 00h; resets register for read operations
Standby		Wait for V_{PP} to ramp to V_{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 2. Programming Flowchart: Fastwrite Algorithm



† n = number of devices being erased.

Figure 3. Parallel-Erase Flow Diagram

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 2): All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 3) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range during read/erase/program, T_A:
L ..... 0°C to 70°C
E ..... −40°C to 85°C
Q ..... −40°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to V_{SS}.
2. The voltage on any input can undershoot to −2 V for periods less than 20 ns.
3. The voltage on any output can overshoot to 7 V for periods less than 20 ns.

recommended operating conditions

				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	During write/read/flash erase		4.5	5	5.5	V
V_{PP}	Supply voltage	During read only (V_{PPL})		0		V_{CC} + 2	V
		During write/read/flash erase (V_{PPH})		11.4	12	12.6	V
V_{IH}	High-level dc input voltage		TTL inputs	2		V_{CC} + 0.5	V
			CMOS inputs	V_{CC} − 0.5		V_{CC} + 0.5	
V_{IL}	Low-level dc input voltage		TTL inputs	−0.5		0.8	V
			CMOS inputs	GND − 0.2		GND + 0.2	
V_{ID}	Voltage level on A9 for algorithm-selection mode			11.5		13	V

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 2.5 mA	2.4		V
			I_{OH} = – 100 µA	V_{CC} – 0.4		
V_{OL}	Low-level output voltage		I_{OL} = 5.8 mA		0.45	V
			I_{OL} = 100 µA		0.1	
I_{ID}	A9 algorithm-selection-mode current		A9 = V_{ID} max		200	µA
I_I	Input current (leakage)	All except A9	V_I = 0 V to 5.5 V		±1	µA
		A9	V_I = 0 V to 13 V		± 200	
I_O	Output current (leakage)		V_O = 0 V to V_{CC}		±10	µA
I_{PP1}	V_{PP} supply current (read/standby)		V_{PP} = V_{PPH}, Read mode		200	µA
			V_{PP} = V_{PPL}		±10	µA
I_{PP2}	V_{PP} supply current (during program pulse) (see Note 4)		V_{PP} = V_{PPH}		30	mA
I_{PP3}	V_{PP} supply current (during flash erase) (see Note 4)		V_{PP} = V_{PPH}		30	mA
I_{PP4}	V_{PP} supply current (during program/erase verify) (see Note 4)		V_{PP} = V_{PPH}		5	mA
I_{CCS}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		1	mA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	µA
I_{CC1}*	V_{CC} supply current (active read)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, f = 6 MHz, I_{OUT} = 0 mA		30	mA
I_{CC2}	V_{CC} average supply current (active write) (see Note 4)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, Programming in progress		10	mA
I_{CC3}	V_{CC} average supply current (flash erase) (see Note 4)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, Erasure in progress		15	mA
I_{CC4}	V_{CC} average supply current (program/erase verify) (see Note 4)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, V_{PP} = V_{PPH}, Program/erase verify in progress		15	mA
V_{LKO}	V_{CC} erase/write lockout voltage		V_{PP} = V_{PPH}	2.5		V

NOTE 4: Not 100% tested; characterization data available.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_i	Input capacitance	V_I = 0 V		6	pF
C_o	Output capacitance	V_O = 0 V		12	pF

† Capacitance measurements are made on sample basis only.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	ALTERNATE SYMBOL	'28F020-10		'28F020-12		'28F020-15		'28F020-17		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address, A0–A17	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns	t_{AVQV}		100		120		150		170	ns
$t_{a(E)}$	Access time from chip enable, $\overline{E}$		t_{ELQV}		100		120		150		170	ns
$t_{en(G)}$	Access time from output enable, $\overline{G}$		t_{GLQV}		45		50		55		60	ns
$t_{c(R)}$	Cycle time, read		t_{AVAV}	100		120		150		170		ns
$t_{d(E)}$	Delay time, $\overline{E}$ going low to low-impedance output		t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ going low to low-impedance output		t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Chip disable time to high-impedance output		t_{EHQZ}	0	55	0	55	0	55	0	55	ns
$t_{dis(G)}$	Output disable time to high-impedance output		t_{GHQZ}	0	30	0	30	0	35	0	35	ns
$t_{h(D)}$	Hold time, data valid from address, $\overline{E}$ or $\overline{G}$†		t_{AXQX}	0		0		0		0		ns
$t_{rec(W)}$	Write recovery time before read		t_{WHGL}	6		6		6		6		µs

† Whichever occurs first

timing requirements–write/erase/program operations

		ALTERNATE SYMBOL	'28F020-10			'28F020-12			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{W}$	t_{AVAV}	100			120			ns
$t_{c(W)PR}$	Cycle time, programming operation	t_{WHWH1}	10			10			µs
$t_{c(W)ER}$	Cycle time, erase operation	t_{WHWH2}	9.5	10		9.5	10		ms
$t_{h(A)}$	Hold time, address	t_{WLAX}	55			60			ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0			0			ns
$t_{h(WHD)}$	Hold time, data valid after $\overline{W}$ high	t_{WHDX}	10			10			ns
$t_{su(A)}$	Setup time, address	t_{AVWL}	0			0			ns
$t_{su(D)}$	Setup time, data	t_{DVWH}	50			50			ns
$t_{su(E)}$	Setup time, $\overline{E}$ before $\overline{W}$	t_{ELWL}	20			20			ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ going low	t_{VPEL}	1			1			µs
$t_{rec(W)}$	Recovery time, $\overline{W}$ before read	t_{WHGL}	6			6			µs
$t_{rec(R)}$	Recovery time, read before $\overline{W}$	t_{GHWL}	0			0			µs
$t_{w(W)}$	Pulse duration, $\overline{W}$ (see Note 5)	t_{WLWH}	60			60			ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20			20			ns
$t_{r(VPP)}$	Rise time, V_{PP}	t_{VPPR}	1			1			µs
$t_{f(VPP)}$	Fall time, V_{PP}	t_{VPPF}	1			1			µs

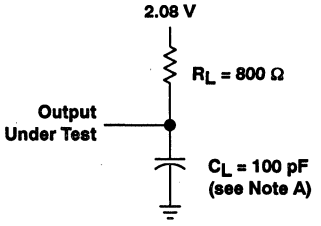
		ALTERNATE SYMBOL	'28F020-15			'28F020-17			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{W}$	t_{AVAV}	150			170			ns
$t_{c(W)PR}$	Cycle time, programming operation	t_{WHWH1}	10			10			µs
$t_{c(W)ER}$	Cycle time, erase operation	t_{WHWH2}	9.5	10		9.5	10		ms
$t_{h(A)}$	Hold time, address	t_{WLAX}	60			70			ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0			0			ns
$t_{h(WHD)}$	Hold time, data valid after $\overline{W}$ high	t_{WHDX}	10			10			ns
$t_{su(A)}$	Setup time, address	t_{AVWL}	0			0			ns
$t_{su(D)}$	Setup time, data	t_{DVWH}	50			50			ns
$t_{su(E)}$	Setup time, $\overline{E}$ before $\overline{W}$	t_{ELWL}	20			20			ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ going low	t_{VPEL}	1			1			µs
$t_{rec(W)}$	Recovery time, $\overline{W}$ before read	t_{WHGL}	6			6			µs
$t_{rec(R)}$	Recovery time, read before $\overline{W}$	t_{GHWL}	0			0			µs
$t_{w(W)}$	Pulse duration, $\overline{W}$ (see Note 5)	t_{WLWH}	60			60			ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20			20			ns
$t_{r(VPP)}$	Rise time, V_{PP}	t_{VPPR}	1			1			µs
$t_{f(VPP)}$	Fall time, V_{PP}	t_{VPPF}	1			1			µs

NOTE 5: Rise/fall time ≤ 10 ns

timing requirements — alternative $\overline{E}$-controlled writes

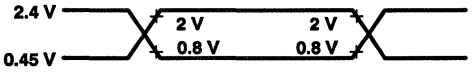
		ALTERNATE SYMBOL	'28F020-10		'28F020-12		'28F020-15		'28F020-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{E}$	t_{AVAV}	100		120		150		170		ns
$t_{c(E)PR}$	Cycle time, programming operation	t_{EHEH}	10		10		10		10		µs
$t_{h(EA)}$	Hold time, address	t_{ELAX}	75		80		80		90		ns
$t_{h(ED)}$	Hold time, data	t_{EHDX}	10		10		10		10		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	0		0		0		0		ns
$t_{su(A)}$	Setup time, address	t_{AVEL}	0		0		0		0		ns
$t_{su(D)}$	Setup time, data	t_{DVEH}	50		50		50		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before $\overline{E}$	t_{WLEL}	0		0		0		0		ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ low	t_{VPEL}	1		1		1		1		µs
$t_{rec(E)R}$	Recovery time, write using $\overline{E}$ before read	t_{EHGL}	6		6		6		6		µs
$t_{rec(E)W}$	Recovery time, read before write using $\overline{E}$	t_{GHEL}	0		0		0		0		µs
$t_{w(E)}$	Pulse duration, write using $\overline{E}$	t_{ELEH}	70		70		70		80		ns
$t_{w(EH)}$	Pulse duration, write, $\overline{E}$ high	t_{EHEL}	20		20		20		20		ns

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

LOAD CIRCUIT



VOLTAGE WAVEFORMS

The ac testing inputs are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} as close as possible to the device terminals.

Figure 4. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

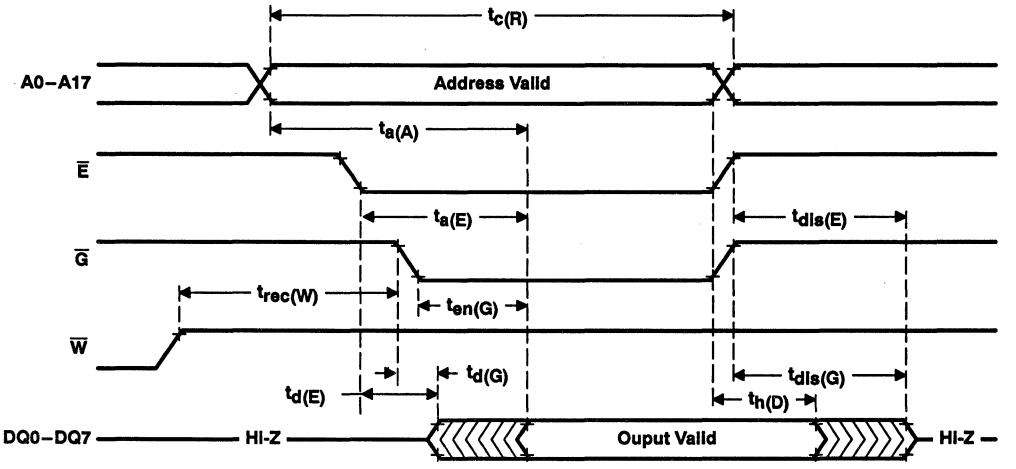


Figure 5. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

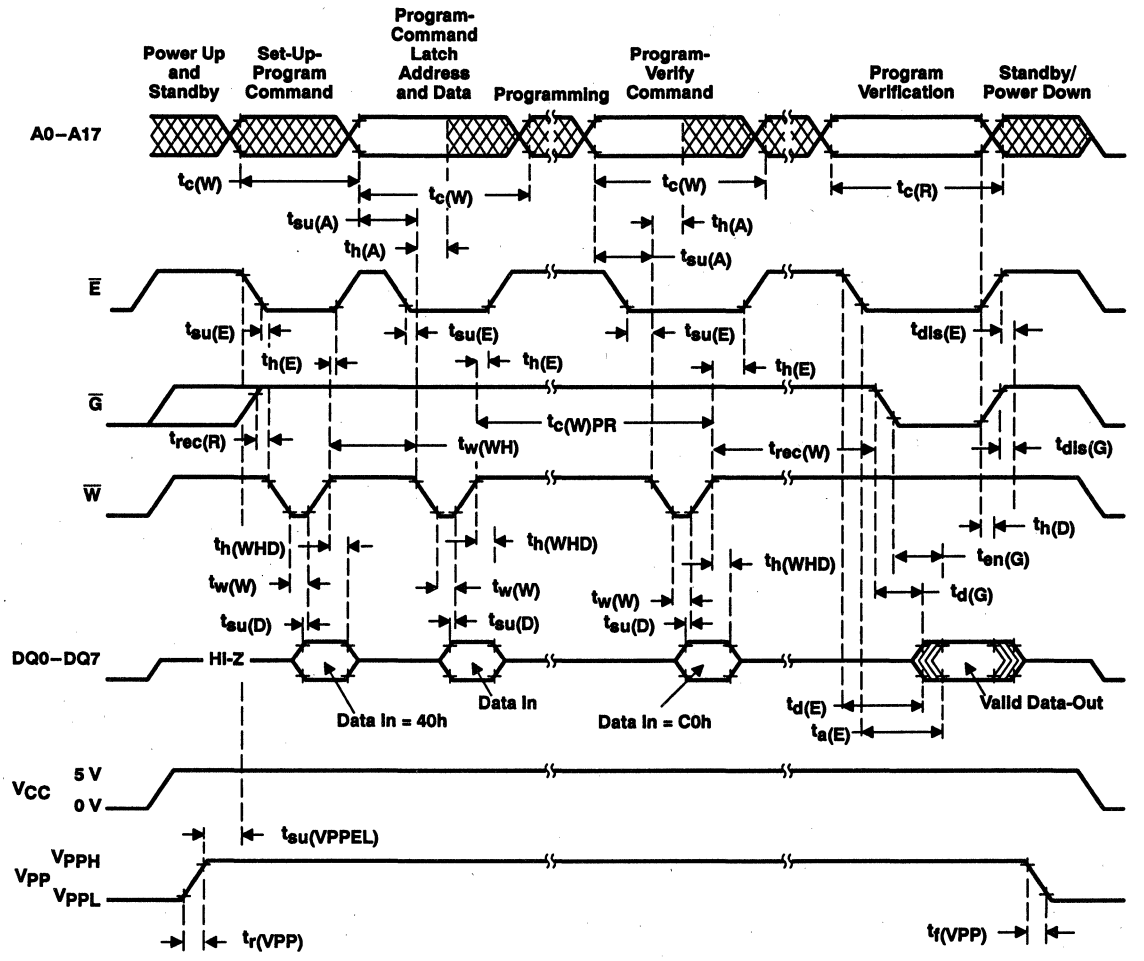


Figure 6. Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

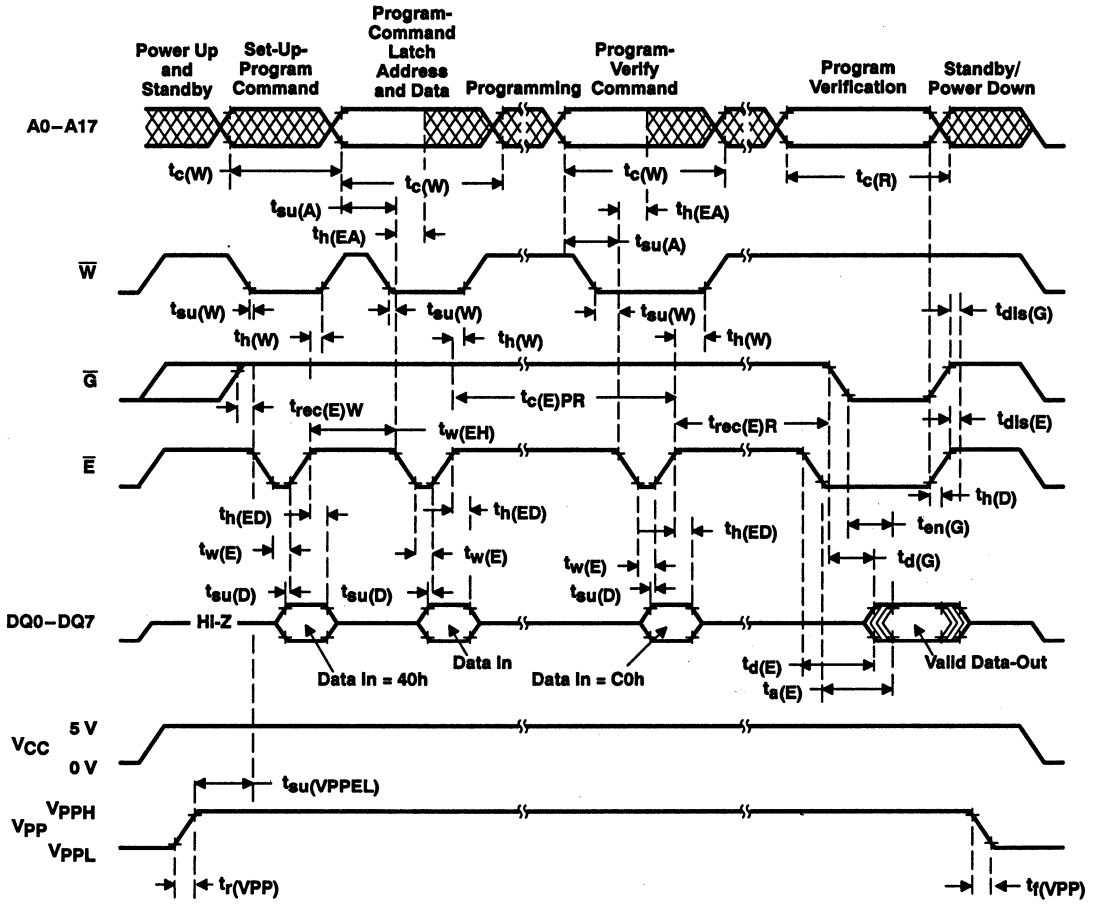


Figure 7. Write-Cycle (Alternative $\overline{E}$-Controlled Writes) Timing

PARAMETER MEASUREMENT INFORMATION

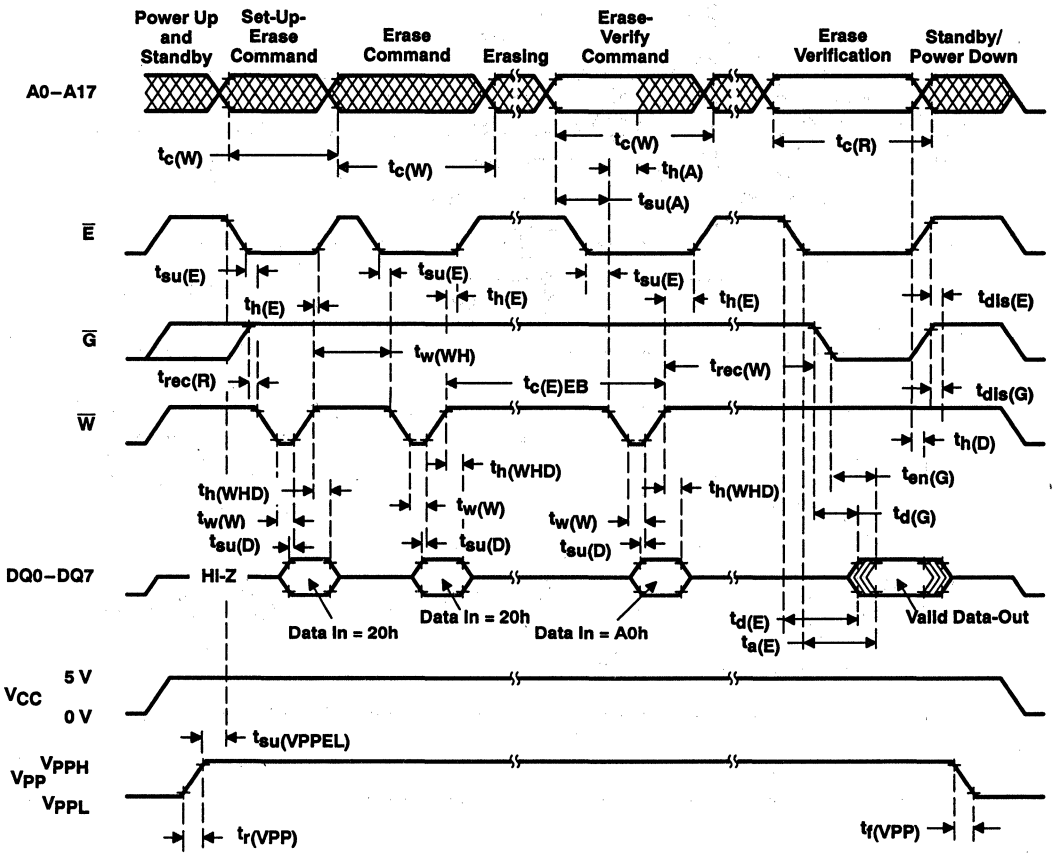


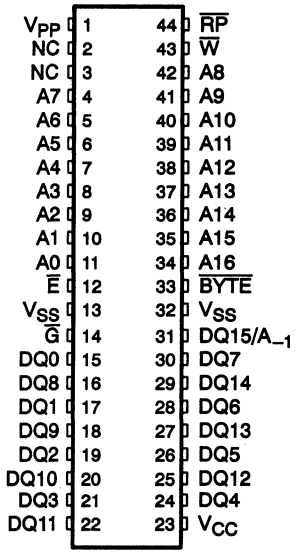
Figure 8. Flash-Erase-Cycle Timing

- **Organization**
  - **Two 8K-Byte Parameter Blocks**
  - **One 96K-Byte Main Block**
  - **One 128K-Byte Main Block**
  - **One 16K-Byte Protected Boot Block**
  - **Top or Bottom Boot Locations**
- **All Inputs/Outputs TTL Compatible**
- **Maximum Access/Minimum Cycle Time**

V_{CC} ± 5%	V_{CC} ± 10%	
'28F200BZ-6-x		60 ns
	'28F200BZ-70-x	70 ns
	'28F200BZ-80-x	80 ns
	'28F200BZ-90-x	90 ns

- **100000 and 10000 Program/Erase Cycle Versions**
- **Three Temperature Ranges**
  - **Commercial . . . 0°C to 70°C**
  - **Extended . . . – 40°C to 85°C**
  - **Automotive . . . – 40°C to 125°C**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active Write . . . 330 mW (Byte Write)**
  - **Active Read . . . 330 mW (Byte Read)**
  - **Active Write . . . 358 mW (Word Write)**
  - **Active Read . . . 330 mW (Word Read)**
  - **Block Erase . . . 165 mW**
  - **Standby . . . 0.55 mW (CMOS-Input Levels)**
  - **Deep Power-Down Mode . . . 0.0066 mW**
- **Fully Automated On-Chip Erase and Word/Byte Program Operations**
- **Write Protection for Boot Block**
- **Command State Machine (CSM)**
  - **Erase Suspend/Resume**
  - **Algorithm-Selection Identifier**

DBJ PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A16	Address Inputs
$\overline{BYTE}$	Byte Enable
DQ0–DQ14	Data In/Out
DQ15/A_{-1}	Data In/Out (word-wide mode), Low-Order Address (byte-wide mode)
DU	Do Not Use
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Internal Connection
$\overline{RP}$	Reset/Deep Power-Down
V_{CC}	5-V Power Supply
V_{PP}	12-V Power Supply for Program/Erase
V_{SS}	Ground
$\overline{W}$	Write Enable

ADVANCE INFORMATION

description

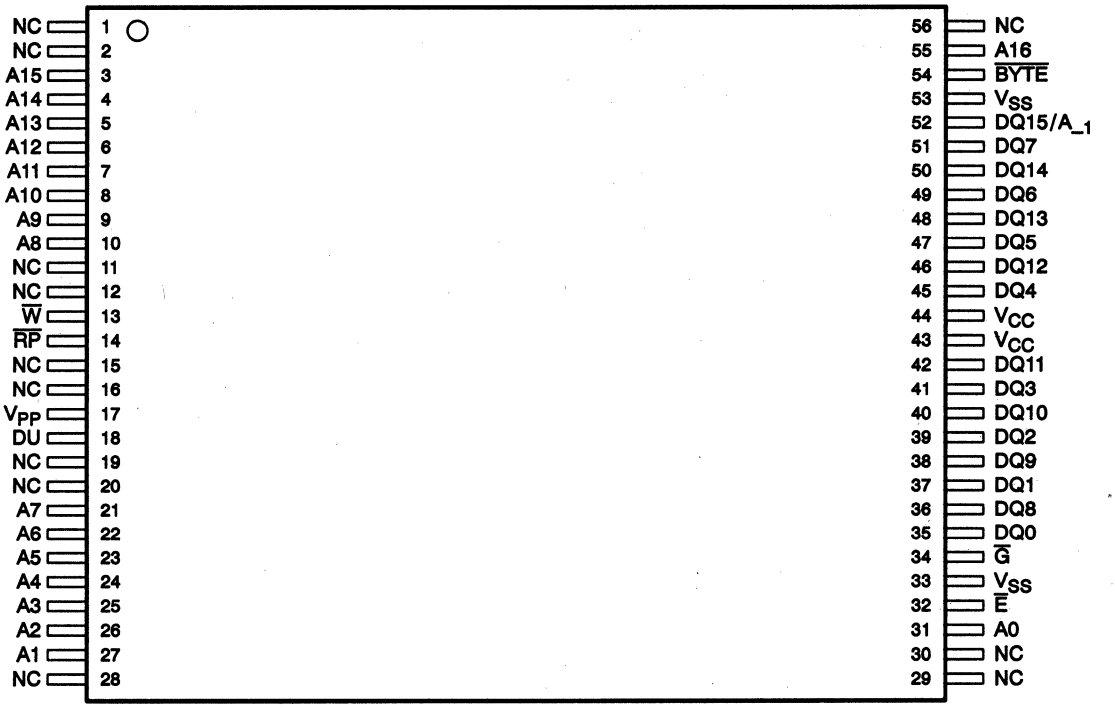
The TMS28F200BZx is a 2097152-bit, boot-block flash memory that can be electrically block erased and reprogrammed. The TMS28F200BZx is organized in a blocked architecture consisting of one 16K-byte protected boot block, two 8K-byte parameter blocks, one 96K-byte main block, and one 128K-byte main block. The device can be ordered with either a top or bottom boot-block configuration. Operation as a 256K-byte (8-bit) or a 128K-word (16-bit) organization is user-definable.

Embedded program and block-erase functions are fully automated by an on-chip write state machine (WSM), simplifying these operations and relieving the system microcontroller of these secondary tasks. WSM status can be monitored by an on-chip status register to determine progress of program/erase tasks. The device features user-selectable block erasure.

description (continued)

The TMS28F200BZx flash memory is offered in a 44-pin PSOP and a 56-pin TSOP package. It is available in three temperature ranges: 0°C to 70°C, – 40°C to 85°C, and – 40°C to 125°C.

DBR PACKAGE
(TOP VIEW)



device symbol nomenclature

TMS28F200BZT 6 C DBJ L

Temperature Range Designator
L = 0°C to 70°C
E = –40°C to 85°C
Q = –40°C to 125°C

Package Designator
DBJ = Plastic Small-Outline Package
DBR = Thin Small-Outline Package

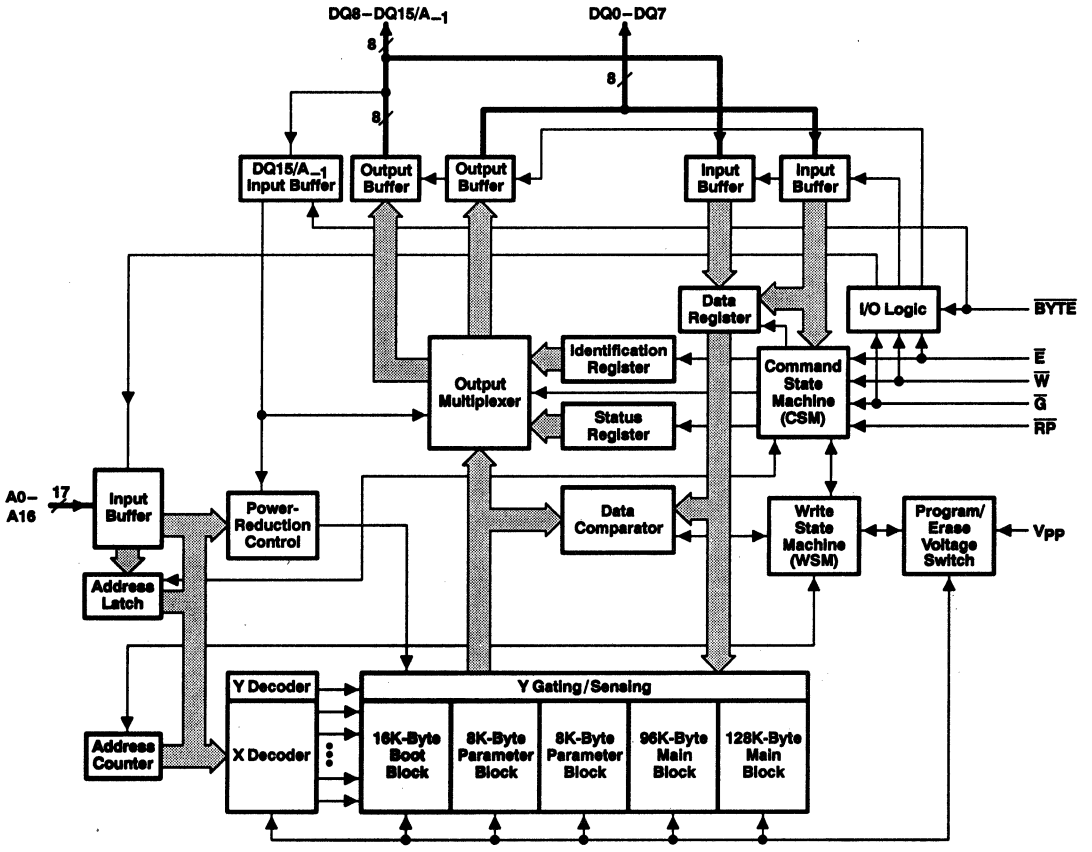
Program/Erase Endurance
C = 100000 Cycles
B = 10000 Cycles

Speed Designator
6 = 60 ns (±5% V_{CC} tolerance)
70 = 70 ns (±10% V_{CC} tolerance)
80 = 80 ns (±10% V_{CC} tolerance)
90 = 90 ns (±10% V_{CC} tolerance)

Boot Block Location Indicator
T = Top Location
B = Bottom Location

ADVANCE INFORMATION

functional block diagram



architecture

The TMS28F200BZx uses a blocked architecture to allow independent erasure of selected memory blocks. Any address within a block address range selects that block for the required read, program, or erase operation.

block memory maps

The TMS28F200BZx is available with the block architecture mapped in either of two configurations: the boot block located at the top or at the bottom of the memory array, as required by different microprocessors. The TMS28F200BZB (bottom boot block) is mapped with the 16K-byte boot block located at the low-order address range (00000h to 01FFFh). The TMS28F200BZT (top boot block) is inverted with respect to the TMS28F200BZB with the boot block located at the high-order address range (1E000h to 1FFFFh). Both of these address ranges are for word-wide mode. Figure 2 and Figure 3 show the memory maps for these configurations.

ADVANCE INFORMATION

block memory maps (continued)

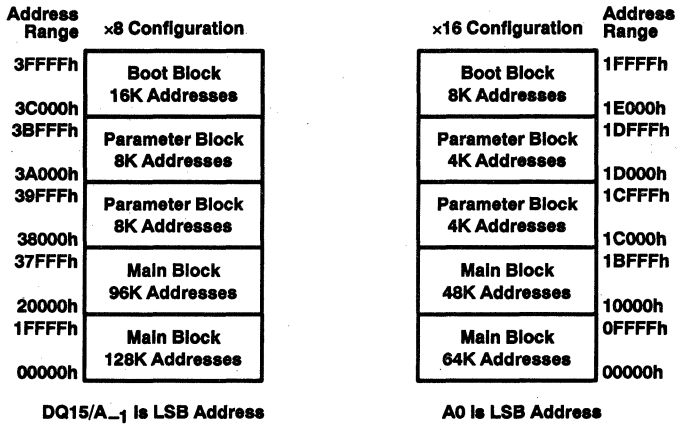


Figure 1. TMS28F200BZT (Top Boot Block) Memory Map

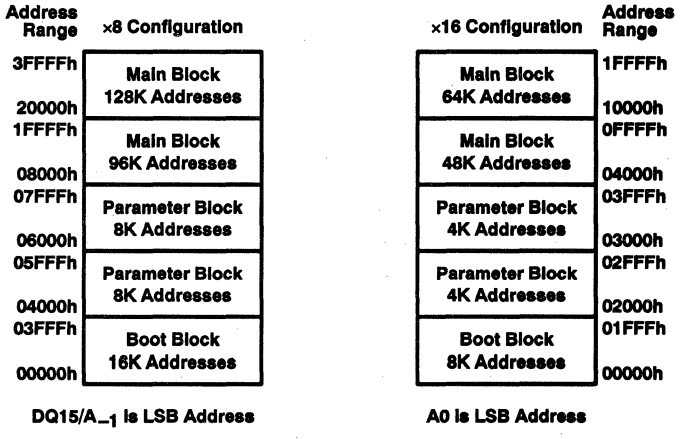


Figure 2. TMS28F200BZB (Bottom Boot Block) Memory Map

boot-block data protection

The 16K-byte boot block is used to store key system data that is seldom changed in normal operation. To protect data within this memory sector, the $\overline{RP}$ terminal can be used to provide a lockout to eliminate accidental erase or program operations. When $\overline{RP}$ is operated with normal TTL/CMOS logic levels, the contents of the boot block cannot be erased or reprogrammed. Changes to the contents of the boot block can be made only when $\overline{RP}$ is at V_{HH} (nominally 12 V) during normal write/erase operations.

parameter block

Two parameter blocks of 8K bytes each can be used like a scratch pad to store frequently updated data. Alternately, the parameter blocks can be used for additional boot- or main-block data. If a parameter block is used to store additional boot-block data, caution should be exercised because the parameter block does not have the boot-block data-protection safety feature.

main block

Primary memory on the TMS28F200BZx is located in two main blocks. One of the blocks has storage capacity of 128K bytes and the other block has storage capacity of 96K bytes.

command state machine (CSM)

The CSM is the interface between an external microprocessor and the write state machine and status register on the memory chip. When the WSM has completed a task, the WSM status (WSMS) bit (SB7) is set to a logic high (1), allowing the CSM to respond to the full command set.

status register (SR)

The status register provides a means of determining whether the state of a program/erase operation is pending or complete. The status register is read by writing a read-status command to the CSM and reading the resulting status code on I/O terminals DQ0–DQ7. This is valid for operation in either the byte- or word-wide mode. When the device is operating in the word-wide mode, the high order I/Os (DQ8–DQ15) are set to 00h when performing a read-status operation.

After a read-status command has been given, the data appearing on DQ0–DQ7 remains as the status register data until a new command is issued to the CSM. To return the device to other modes of operation, a new command must be issued to the CSM.

Register data is updated on the falling edge of $\overline{G}$ or $\overline{E}$. The latest falling edge of either of these two signals updates the latch within a given read cycle. Latching data prevents errors from occurring should the register input change during a status-register read. To assure that the status-register output contains updated status data, $\overline{E}$ or $\overline{G}$ must be toggled for each subsequent status read.

The status register provides the internal state of the WSM to the external microprocessor. During periods when the WSM is active, the status register can be polled to determine the WSMS. Table 1 defines the status register bits and their functions.

status register (SR) (continued)

Table 1. Status Register Bit Definitions and Functions

STATUS BIT	FUNCTION	DATA	COMMENTS
SB7	Write-state-machine status (WSMS)	1 = Ready 0 = Busy	If SB7 = 0, the WSM has not completed an erase or programming operation. If SB7 = 1 (ready), other polling operations can be performed. SB7 does not automatically update WSM status at the completion of a WSM task. If the WSM status bit shows busy (0), the user must periodically toggle $\overline{E}$ or $\overline{G}$ to determine when the WSM has completed an operation (SB7 = 1).
SB6	Erase-suspend status (ESS)	1 = Erase suspended 0 = Erase in progress or completed	When an erase-suspend command is issued, the WSM halts execution and sets the ESS bit high (SB6 = 1) indicating that the erase operation has been suspended. The WSMS bit is also set high (SB7 = 1) indicating that the erase-suspend operation has been successfully completed. The ESS bit remains at a high level until an erase-resume command is input to the CSM (code D0h).
SB5	Erase status (ES)	1 = Block erase error 0 = Block erase good	SB5 = 0 indicates that a successful block erasure has occurred. SB5 = 1 indicates that an erase error has occurred. In this case, the WSM has completed the maximum allowed erase pulses determined by the internal algorithm, but this was insufficient to completely erase the device.
SB4	Program status (PS)	1 = Byte/word program error 0 = Byte/word program good	SB4 = 0 indicates successful programming has occurred at the addressed block location. SB4 = 1 indicates that the WSM was unable to correctly program the addressed block location.
SB3	V_{PP} status (V_{PPS})	1 = Program abort: V_{PP} too low 0 = V_{PP} good	SB3 provides information on the status of V_{PP} during programming. If V_{PP} is too low after a program or erase command has been issued, SB3 is set to a 1 indicating that the programming operation is aborted. The V_{PP} status bit is not assured to give accurate feedback between V_{PPH} and V_{PPL}.
SB2–SB0	Reserved		These bits should be masked out when reading the status register.

operation

Device operations are selected by entering standard JEDEC 8-bit command codes with conventional microprocessor timing into an on-chip command state machine (CSM) through I/O terminals DQ0–DQ7. When the device is powered up, internal reset circuitry initializes the chip to a read-array mode of operation. Changing the mode of operation requires a command code to be entered into the CSM. Table 2 lists the CSM codes for all modes of operation.

The on-chip status register allows the progress of various operations to be monitored. The status register is interrogated by entering a read-status-register command into the CSM (cycle 1) and reading the register data on I/O terminals DQ0–DQ7 (cycle 2). Status-register bits SB0 through SB7 correspond to DQ0 through DQ7.

ADVANCE INFORMATION

operation (continued)

Table 2. Command State Machine Codes for Device Mode Selection

COMMAND CODE ON DQ0–DQ7†	DEVICE MODE
00h	Invalid/Reserved
10h	Alternate Program Setup
20h	Block-Erase Setup
40h	Program Setup
50h	Clear-Status Register
70h	Read-Status Register
90h	Algorithm Selection
B0h	Erase Suspend
D0h	Erase Resume/Block-Erase Confirm
FFh	Read Array

† DQ0 is the least significant bit. DQ8–DQ15 are any valid 2-state level.

command definition

Once a specific command code has been entered, the WSM executes an internal algorithm generating the necessary timing signals to program, erase, and verify data. See Table 3 for the CSM command definitions and data for each of the bus cycles.

Following the read-algorithm-selection-code command, two read cycles are required to access the manufacturer-equivalent code and the device-equivalent code as shown in Table 4 and Table 5.

Table 3. Command Definitions

COMMAND	BUS CYCLES REQUIRED	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION	ADDRESS	CSM INPUT	OPERATION	ADDRESS	DATA IN/OUT
Read Operations							
Read Array	1	Write	X	FFh	Read	X	Data Out
Read Algorithm-Selection Code	3	Write	X	90h	Read	A0	M/D
Read-Status Register	2	Write	X	70h	Read	X	SRB
Clear-Status Register	1	Write	X	50h			
Program Mode							
Program Setup/Program (byte/word)	2	Write	PA	40h or 10h	Write	PA	PD
Erase Operations							
Block-Erase Setup/ Block-Erase Confirm	2	Write	BEA	20h	Write	BEA	D0h
Erase Suspend/ Erase Resume	2	Write	X	B0h	Write	X	D0h

Legend:

BEA Block-erase address. Any address selected within a block selects that block for erase.
M/D Manufacturer-equivalent/device-equivalent code
PA Address to be programmed
PD Data to be programmed at PA
SRB Status-register data byte that can be found on DQ0–DQ7

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byte-wide or word-wide mode selection

The memory array is divided into two parts: an upper half byte that outputs data through I/Os DQ8–DQ15, and a lower half byte that outputs data through DQ0–DQ7. Device operation in either byte-wide or word-wide mode is user-selectable and is determined by the logic state of $\overline{BYTE}$. When $\overline{BYTE}$ is at a logic high level, the device is in the word-wide mode and data is written to or read from I/Os DQ0–DQ15. When $\overline{BYTE}$ is at a logic low, the device is in the byte-wide mode and data is written to or read from I/Os DQ0–DQ7. In the byte-wide mode, I/Os DQ8–DQ14 are placed in the high-impedance state and DQ15/A_{-1} becomes the low-order address terminal and selects either the upper or lower half of the array. Array data from the upper half (DQ8–DQ15) and the lower half (DQ0–DQ7) are multiplexed and appear on DQ0–DQ7. Table 4 and Table 5 summarize operations for word-wide mode and byte-wide mode.

Table 4. Operation Modes for Word-Wide Mode ($\overline{BYTE}$ = V_{IH})

MODE	$\overline{E}$	$\overline{G}$	$\overline{RP}$	$\overline{W}$	A9	A0	V_{PP}	DQ0–DQ15
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	Data out
Algorithm-selection mode	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IL}	X	Manufacturer-equivalent code 0089h
	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IH}	X	Device-equivalent code 2274h (top boot block)
								Device-equivalent code 2275h (bottom boot block)
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	High impedance
Standby	V_{IH}	X	V_{IH}	X	X	X	X	High impedance
Reset/deep power down	X	X	V_{IL}	X	X	X	X	High impedance
Write (see Note 1)	V_{IL}	V_{IH}	V_{IH} or V_{HH}	V_{IL}	X	X	V_{PPL} or V_{PPH}	Data in

Table 5. Operation Modes for Byte-Wide Mode ($\overline{BYTE}$ = V_{IL})

MODE	$\overline{E}$	$\overline{G}$	$\overline{RP}$	$\overline{W}$	A9	A0	V_{PP}	DQ15/A_{-1}	DQ8–DQ14	DQ0–DQ7
Read lower byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	V_{IL}	Hi-Z	Data out
Read upper byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	V_{IH}	Hi-Z	Data out
Algorithm-selection mode	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IL}	X	X	Hi-Z	Manufacturer-equivalent code 89h
	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IH}	X	X	Hi-Z	Device-equivalent code 74h (top boot block)
										Device-equivalent code 75h (bottom boot block)
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	X	Hi-Z	High impedance
Standby	V_{IH}	X	V_{IH}	X	X	X	X	X	Hi-Z	High impedance
Reset/deep power down	X	X	V_{IL}	X	X	X	X	X	Hi-Z	High impedance
Write (see Note 1)	V_{IL}	V_{IH}	V_{IH} or V_{HH}	V_{IL}	X	X	V_{PPL} or V_{PPH}	X	Hi-Z	Data in

NOTE 1: When writing commands to the '28F200BZx, V_{PP} must be V_{PPH} for block-erase or program commands to be executed and $\overline{RP}$ must be held at V_{HH} for the entire boot block program or erase operation.

command state machine (CSM) operations

The CSM decodes instructions for read, read algorithm-selection code, read status register, clear status register, program, erase, erase suspend, and erase resume. The 8-bit command code is input to the device on DQ0–DQ7 (see Table 2 for CSM codes). During a program or erase cycle, the CSM informs the WSM that a program or erase cycle has been requested. During a program cycle, the WSM controls the program sequences and the CSM responds only to status reads.

During an erase cycle, the CSM responds to status reads and erase suspend. When the WSM has completed its task, the WSM status bit (SB7) is set to a logic high and the CSM responds to the full command set. The CSM stays in the current command state until the microprocessor issues another command.

The WSM successfully initiates an erase or program operation only when V_{PP} is within its correct voltage range (V_{PPH}). For data protection, it is recommended that $\overline{RP}$ be held at a logic low during a CPU reset.

read operations

There are three read operations available: read array, read algorithm-selection code, and read status register.

read array

The array is read by entering the command code FFh on DQ0–DQ7. Control terminals $\overline{E}$ and $\overline{G}$ must be at a logic low (V_{IL}) and $\overline{W}$ and $\overline{RP}$ must be at a logic high (V_{IH}) to read data from the array. Data is available on DQ0–DQ15 (word-wide mode) or DQ0–DQ7 (byte-wide mode). Any valid address within any of the blocks selects that block and allows data to be read from the block.

read algorithm-selection code

Algorithm-selection codes are read by entering command code 90h on DQ0–DQ7. Two bus cycles are required for this operation: the first to enter the command code and a second to read the device-equivalent code. Control terminals $\overline{E}$ and $\overline{G}$ must be at a logic low (V_{IL}) and $\overline{W}$ and $\overline{RP}$ must be at a logic high (V_{IH}). Two identifier bytes are accessed by toggling A0. The manufacturer-equivalent code is obtained on DQ0–DQ7 with A0 at a logic low (V_{IL}). The device-equivalent code is obtained when A0 is set to a logic high (V_{IH}). Alternately, the manufacturer- and device-equivalent codes can be read by applying V_{ID} (nominally 12 V) to A9 and selecting the desired code by toggling A0 high or low. All other addresses are don't care (see Table 3, Table 4, and Table 5).

read status register

The status register is read by entering the command code 70h on DQ0–DQ7. Control terminals $\overline{E}$ and $\overline{G}$ must be at a logic low (V_{IL}) and $\overline{W}$ and $\overline{RP}$ must be at a logic high (V_{IH}). Two bus cycles are required for this operation: one to enter the command code and a second to read the status register. In a given read cycle, status register contents are updated on the falling edge of $\overline{E}$ or $\overline{G}$, whichever occurs last within the cycle.

clear status register

The internal circuitry can set only the V_{PP} status (SB3), the program status (SB4), and the erase status (SB5) bits of the status register. The clear-status-register command (50h) allows the external microprocessor to clear these status bits and synchronize to internal operations. When the status bits are cleared, the device returns to the read array mode.

boot-block programming/erasing

Should changes to the boot block be required, $\overline{RP}$ must be set to V_{HH} (12 V) and V_{PP} to the programming voltage level (V_{PPH}). If an attempt is made to write, erase, or erase suspend the boot block without $\overline{RP}$ at V_{HH}, an error signal is generated on SB4 (program-status bit) or SB5 (erase-status bit).

A program-setup command can be aborted by writing FFh (in byte-wide mode) or FFFFh (in word-wide mode) during the second cycle. After writing FFh or FFFFh during the second cycle, the CSM responds only to status reads. When the WSM status bit (SB7) is set to a logic high, signifying termination of the nonprogram operation is terminated, all commands to the CSM become valid again.

normal programming

There are two CSM commands for programming: program setup and alternate program setup (see Table 2 on page 7). After the desired command code is entered, the WSM takes over and correctly sequences the device to complete the program operation. During this time, the CSM responds only to status reads until the program operation has been completed, after which all commands to the CSM become valid again. Once a program command has been issued, the WSM cannot normally be interrupted until the program algorithm is completed (see Figure 4 and Figure 4). Taking $\overline{RP}$ to V_{IL} during programming aborts the program operation. During programming, V_{PP} must remain at V_{PPH}. Only 0s are written and compared during a program operation. If 1s are programmed, the memory cell contents do not change and no error occurs.

A program-setup command can be aborted by writing FFh (in byte-wide mode) or FFFFh (in word-wide mode) during the second cycle. After writing all 1s during the second cycle, the CSM responds only to status reads. When the WSM status bit (SB7) is set to a logic high, signifying the nonprogram operation is terminated, all commands to the CSM become valid again.

erase operations

There are two erase operations that can be performed by the TMS28F200BZx devices: block erase and erase suspend/erase resume. An erase operation must be used to initialize all bits in an array block to 1s. After block-erase confirm is issued, the CSM responds only to status reads or erase-suspend commands until the WSM completes its task.

block erasure

Block erasure inside the memory array sets all bits within the addressed block to logic 1s. Erasure is accomplished only by blocks; data at single address locations within the array cannot be individually erased. Any valid address within the parameter or main blocks acts as a block selector and allows that block to be erased. $\overline{RP}$ must be at V_{HH} for changing the data content of the boot block. Block erasure is initiated by a command sequence to the CSM: block-erase setup (20h) followed by block-erase confirm (D0h). A two-command erase sequence protects against accidental erasure of memory contents.

Erase setup and confirm commands are latched on the rising edge of $\overline{E}$ or $\overline{W}$, whichever occurs first. Block addresses are latched during the block-erase-confirm command on the rising edge of $\overline{E}$ or $\overline{W}$ (see Figure 5). When the block-erase-confirm command is complete, the WSM automatically executes a sequence of events to complete the block erasure. During this sequence, the block is programmed with logic 0s, data is verified, all bits in the block are erased, and finally, verification is performed to assure that all bits are correctly erased. Monitoring of the erase operation is possible through the status register (see read status register).

erase suspend/erase resume

During the execution of an erase operation, the erase-suspend command (B0h) can be entered to direct the WSM to suspend the erase operation. Once the WSM has reached the suspend state, it allows the CSM to respond only to the read-array, read-status-register, and erase-resume commands. During the erase-suspend operation, array data should be read from a block other than the one being erased. To resume the erase operation, an erase-resume command (D0h) must be issued to cause the CSM to clear the suspend state previously set (see Figure 5 and Figure 10).

automatic power-saving mode

Substantial power savings can be realized during periods when the array is not being read. During this time, the device switches to the automatic power-saving mode. When the device switches to this mode, I_{CC} is typically reduced from 40 mA to 1 mA (I_{OUT} = 0 mA). The low level of power is maintained until another read operation is initiated. In this mode, the I/O terminals retain the data from the last memory address read until a new address is read. This mode is entered automatically if no address or control pins toggle within a 200-ns time-out period. At least one transition on $\overline{E}$ must occur after power up to activate this mode.

reset/deep power-down mode

Very low levels of power consumption can be attained by using a special terminal, $\overline{RP}$, that disables internal device circuitry. When $\overline{RP}$ is at a CMOS logic low of 0.0 V ± 0.2 V, an I_{CC} value on the order of 0.2 μA (or 1 μW of power) is achievable. This is important in portable applications where extended battery life is of major concern.

A recovery time is required when exiting from deep power-down mode. For a read-array operation, a minimum of 300 ns is required before data is valid, and a minimum of 215 ns in deep power-down mode is required before data input to the CSM can be recognized. With $\overline{RP}$ at ground, the WSM is reset and the status register is cleared, effectively eliminating accidental programming to the array during system reset. After restoration of power, the device does not recognize any operation command until $\overline{RP}$ is returned to a V_{IH} or V_{HH} level.

Should $\overline{RP}$ become low during a program or erase operation, the device becomes nonfunctional (is in a power-down state) and data being written or erased is invalid or indeterminate, requiring that the operation be performed again after power restoration.

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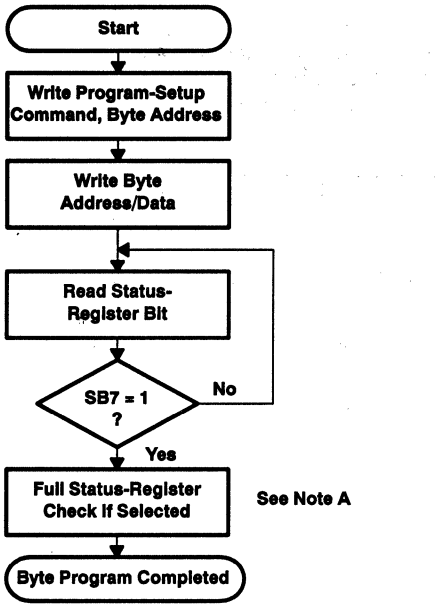
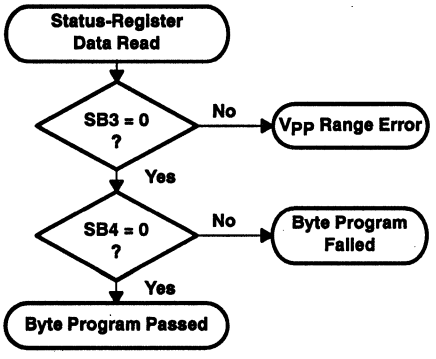


BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h or 10h Addr = Address of byte to be programmed
Write	Write data	Data = Byte to be programmed Addr = Address of byte to be programmed
Read		Status register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register.
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent bytes. Write FFh after the last byte-programming operation to reset the device to read-array mode.		

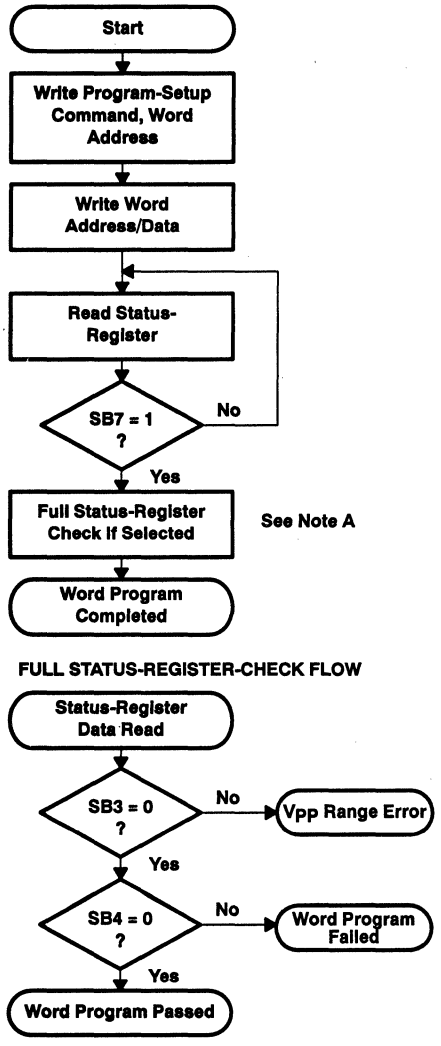
FULL STATUS-REGISTER-CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 1 = Byte program error (see Note C)

NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB4 is cleared only by the clear-status-register command, but it does not prevent additional program operation attempts.

Figure 3. Automated Byte-Programming Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h or 10h Addr = Address of word to be programmed
Write	Write data	Data = Word to be programmed Addr = Address of word to be programmed
Read		Status register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register.
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write FFh after the last word-programming operation to reset the device to read-array mode.		

BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 1 = Word program failed (see Note C)

NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB4 is cleared only by the clear-status-register command, but it does not prevent additional program operation attempts.

Figure 4. Automated Word-Programming Flowchart

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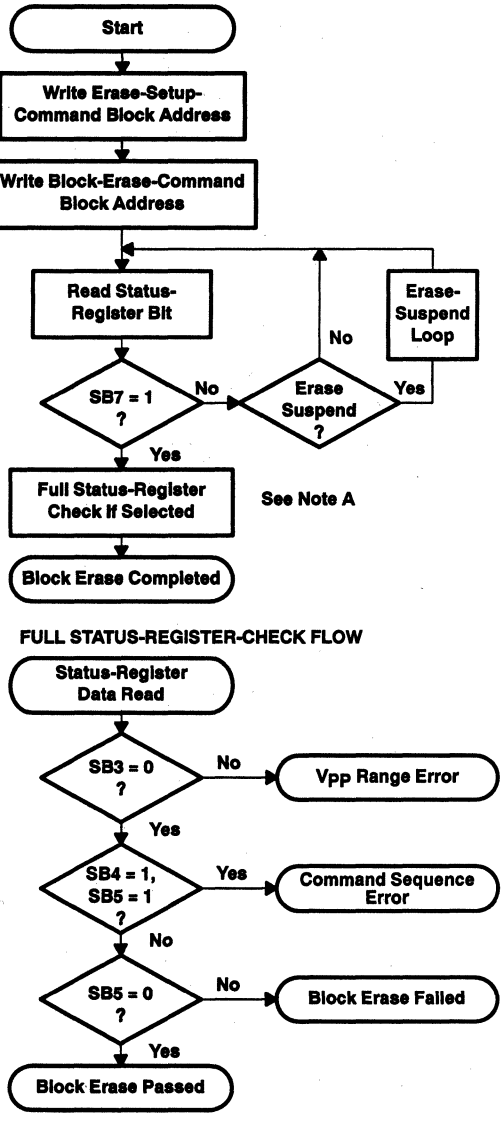
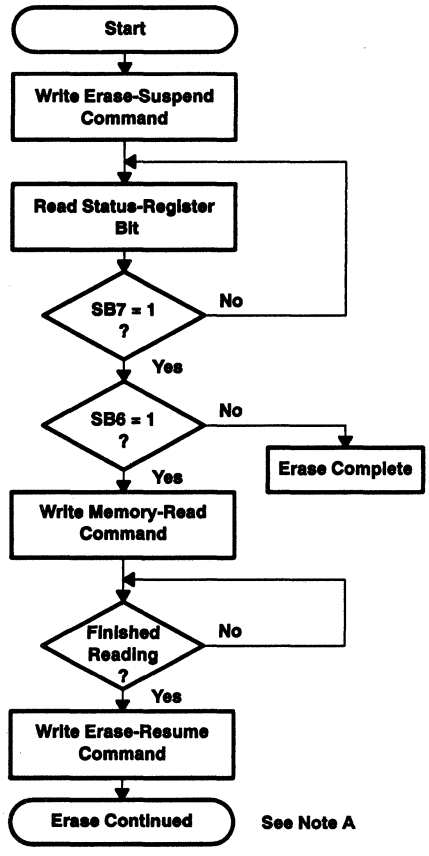


BUS OPERATION	COMMAND	COMMENTS
Write	Write erase setup	Data = 20h Block Addr = Address within block to be erased
Write	Erase	Data = D0h Block Addr = Address within block to be erased
Read		Status register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent blocks. Write FFh after the last block-erase operation to reset the device to read-array mode.		

BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 and SB5 1 = Block-erase command error
Standby		Check SB5 1 = Block-erase failed (see Note C)

NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB5 is cleared only by the clear-status-register command in cases where multiple blocks are erased before full status is checked.

Figure 5. Automated Block-Erase Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Erase suspend	Data = B0h
Read		Status register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register.
Standby		Check SB7 1 = Ready
Standby		Check SB6 1 = Suspended
Write	Read memory	Data = FFh
Read		Read data from block other than that being erased.
Write	Erase resume	Data = D0h

NOTE A: Refer to block-erase flowchart for complete erasure procedure.

Figure 6. Erase-Suspend/Resume Flowchart

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 2) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 2) ..... – 0.6 V to 14 V
Input voltage range: All inputs except A9, $\overline{RP}$ ..... – 0.6 V to V_{CC} + 1 V
$\overline{RP}$, A9 (see Note) ..... – 0.6 V to 13.5 V
Output voltage range (see Note 4) ..... – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range, T_A, during read/erase/program: L suffix ..... 0°C to 70°C
E suffix ..... – 40°C to 85°C
Q suffix ..... – 40°C to 125°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. All voltage values are with respect to V_{SS}.
3. The voltage on any input can undershoot to – 2 V for periods less than 20 ns.
4. The voltage on any output can overshoot to 7 V for periods less than 20 ns.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During write/read/erase/erase suspend	'28F200BZ-x-6	4.75	5	5.25	V
			All others	4.5	5	5.5	
V_{PP}	Supply voltage	During read only (V_{PPL})		0		6.5	V
		During write/erase/erase suspend (V_{PPH})		11.4	12	12.6	V
V_{IH}	High-level dc input voltage		TTL	2		V_{CC} + 0.5	V
			CMOS	V_{CC} – 0.5		V_{CC} + 0.5	V
V_{IL}	Low-level dc input voltage		TTL	– 0.5		0.8	V
			CMOS	V_{SS} – 0.2		V_{SS} + 0.2	V
V_{LKO}	V_{CC} lock-out voltage from write/erase			2			V
V_{HH}	$\overline{RP}$ unlock voltage			11.5	12	13	V

word/byte-write and block-erase performance, T_A = 25°C, V_{PP} = 12 V (see Note 5)

PARAMETER	'28F200BZx-6			'28F200BZx-70			'28F200BZx-80			'28F200BZx-90			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Main-block erase time		2.2			2.2			2.2			2.2		s
Main-block byte-program time		3.2			3.2			3.2			3.2		s
Main-block word-program time		1.6			1.6			1.6			1.6		s
Parameter/boot-block erase time		0.32			0.32			0.32			0.32		s

NOTE 5: Excludes system-level overhead

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature using test conditions given in Table 6 (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage			V_{CC} = 4.5 V, I_{OH} = – 2.5 mA	2.4		V
V_{OL}	Low-level output voltage			V_{CC} = 4.5 V, I_{OL} = 5.8 mA		0.45	V
V_{ID}	A9 selection code voltage				11.5	13	V
I_I	Input current (leakage), except for A9 when A9 = V_{ID}			V_{CC} = 5.5 V, V_I = 0 V to 5.5 V		±1	µA
I_{ID}	A9 selection code current			A9 = V_{ID}		500	µA
I_{RP}	$\overline{RP}$ boot-block unlock current					500	µA
I_O	Output current (leakage)			V_{CC} = 5.5 V, V_O = 0 V to V_{CC}		±10	µA
I_{PPS}	V_{PP} standby current (standby)			$V_{PP} \le V_{CC}$		10	µA
I_{PPL}	V_{PP} supply current (reset/deep power-down mode)			$\overline{RP}$ = V_{SS} ± 0.2 V		5	µA
I_{PP1}	V_{PP} supply current (read)			$V_{PP} > V_{CC}$		200	µA
I_{PP2}	V_{PP} supply current (active byte write)			V_{PP} = V_{PPH}, Programming in progress		30	mA
I_{PP3}	V_{PP} supply current (active word write)			V_{PP} = V_{PPH}, Programming in progress		40	mA
I_{PP4}	V_{PP} supply current (block erase)			V_{PP} = V_{PPH}, Block erase in progress		30	mA
I_{PP5}	V_{PP} supply current (erase suspend)			V_{PP} = V_{PPH}, Block erase suspended		200	µA
I_{CCS}	V_{CC} supply current (standby)	TTL-input level		V_{CC} = 5.5 V, $\overline{E}$ = $\overline{RP}$ = V_{IH}		1.5	mA
		CMOS-input level		V_{CC} = 5.5 V, $\overline{E}$ = $\overline{RP}$ = V_{IH}		100	µA
I_{CCL}	V_{CC} supply current (reset/deep power-down mode)		0°C to 70°C – 40°C to 85°C	RP = V_{SS} ± 0.2 V		1.2	µA
			– 40°C to 125°C			8	µA
I_{CC1}	V_{CC} supply current (active read)	TTL-input level		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA		60	mA
		CMOS-input level		V_{CC} = 5.5 V, $\overline{E}$ = V_{SS} ± 0.2 V, f = 10 MHz, I_{OUT} = 0 mA		55	mA
I_{CC2}	V_{CC} supply current (active byte write) (see Notes 10 and 11)			V_{CC} = 5.5 V, Programming in progress		60	mA
I_{CC3}	V_{CC} supply current (active word write) (see Notes 10 and 11)			V_{CC} = 5.5 V, Programming in progress		65	mA
I_{CC4}	V_{CC} supply current (block erase) (see Notes 10 and 11)			V_{CC} = 5.5 V, Block erase in progress		30	mA
I_{CC5}	V_{CC} supply current (erase suspend) (see Notes 10 and 11)			V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}, Block erase suspended		10	mA

NOTES: 6. Not 100% tested; characterization data available
7. All ac current values are RMS unless otherwise noted.

Table 6. AC Test Conditions

SPEED DESIGNATOR	I_{OL} (mA)	I_{OH} (mA)	V_Z† (V)	V_{OL} (V)	V_{OH} (V)	V_{IL} (V)	V_{IH} (V)	C_{LOAD} (pF)	t_f (ns)	t_r (ns)	TEMPERATURE
-6	5.8	– 2.5	1.5	1.5	1.5	0	3.0	30	<10	<10	0°C to 70°C
-70, -80, -90	5.8	– 2.5	1.5	0.8	2.0	0.45	2.4	100	<10	<10	– 40°C to 125°C

† V_Z is the measured value used to detect high impedance.

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz, V_I = 0 V

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_i	Input capacitance			8	pF
C_o	Output capacitance	V_O = 0 V		12	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	'28F200BZx-6		'28F200BZx-70		'28F200BZx-80		'28F200BZx-90		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from A0–A16	t_{AVQV}		60		70		80		90	ns
$t_{a(E)}$	Access time from $\overline{E}$	t_{ELQV}		60		70		80		90	ns
$t_{a(G)}$	Access time from $\overline{G}$	t_{GLQV}		30		35		40		45	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	60		70		80		90		ns
$t_{d(E)}$	Delay time, $\overline{E}$ low to low-impedance output	t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-impedance output	t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Disable time, $\overline{E}$ to high-impedance output	t_{EHQZ}		20		25		30		35	ns
$t_{dis(G)}$	Disable time, $\overline{G}$ to high-impedance output	t_{GHQZ}		20		25		30		35	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A16, $\overline{E}$, or $\overline{G}$, whichever occurs first	t_{AXQX}	0		0		0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{E}$ low	t_{ELFL} t_{ELFH}		5		5		5		5	ns
$t_{d(RP)}$	Output delay time from $\overline{RP}$ high	t_{PHQV}		300		300		300		300	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in high-impedance state	t_{FLQV}		20		25		30		35	ns
$t_{a(BH)}$	Access time from $\overline{BYTE}$ switching high	t_{FHQV}		60		70		80		90	ns

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature

write/erase operations — $\overline{W}$-controlled writes

		ALT. SYMBOL	'28F200BZx-6		'28F200BZx-70		'28F200BZx-80		'28F200BZx-90		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	60		70		80		90		ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6		6		6		7		µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3		0.3		0.3		0.4		s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3		0.3		0.3		0.4		s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6		0.6		0.6		0.7		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100		100		100	ns
$t_{h(A)}$	Hold time, A0–A16	t_{WHAX}	10		10		10		10		ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0		0		0		0		ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	10		10		10		10		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status register bit	t_{QVVL}	0		0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status register bit	t_{QVPH}	0		0		0		0		ns
$t_{su(A)}$	Setup time, A0–A16	t_{AVWH}	50		50		50		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	50		50		50		50		ns
$t_{su(E)}$	Setup time, $\overline{E}$ before write operation	t_{ELWL}	0		0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{W}$ going high	t_{PHHWH}	100		100		100		100		ns
$t_{su(VPP)}$	Setup time, V_{PP} to $\overline{W}$ going high	t_{VPWH}	100		100		100		100		ns
$t_{w(W)}$	Pulse duration, $\overline{W}$ low	t_{WLWH}	50		50		50		50		ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WLWL}	10		20		30		30		ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{W}$ going low	t_{PHWL}	215		215		215		215		ns

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

write/erase operations — $\overline{E}$-controlled writes

		ALT. SYMBOL	'28F200BZx-6		'28F200BZx-70		'28F200BZx-80		'28F200BZx-90		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{E}$	t_{AVAV}	60		70		80		90		ns
$t_{c(E)OP}$	Cycle time, duration of programming operation using $\overline{E}$	t_{EHQV1}	6		6		6		7		µs
$t_{c(E)ERB}$	Cycle time, erase operation using $\overline{E}$ (boot block)	t_{EHQV2}	0.3		0.3		0.3		0.4		s
$t_{c(E)ERP}$	Cycle time, erase operation using $\overline{E}$ (parameter block)	t_{EHQV3}	0.3		0.3		0.3		0.4		s
$t_{c(E)ERM}$	Cycle time, erase operation using $\overline{E}$ (main block)	t_{EHQV4}	0.6		0.6		0.6		0.7		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100		100		100	ns
$t_{h(A)}$	Hold time, A0–A16	t_{EHAX}	10		10		10		10		ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0		0		0		0		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	10		10		10		10		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		0		ns
$t_{su(A)}$	Setup time, A0–A16	t_{AVEH}	50		50		50		50		ns
$t_{su(D)}$	Setup time, DQ valid	t_{DVEH}	50		50		50		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before $\overline{E}$	t_{WLEL}	0		0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{E}$ going high	t_{PHHEH}	100		100		100		100		ns
$t_{su(VPP)}$	Setup time, V_{PP} to $\overline{E}$ going high	t_{VPEH}	100		100		100		100		ns
$t_{w(E)}$	Pulse duration, $\overline{E}$ low, write using $\overline{E}$	t_{ELEH}	50		50		50		50		ns
$t_{w(EH)}$	Pulse duration, $\overline{E}$ high, write using $\overline{E}$	t_{EHEL}	10		20		30		30		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{E}$ going low	t_{PHEL}	215		215		215		215		ns

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

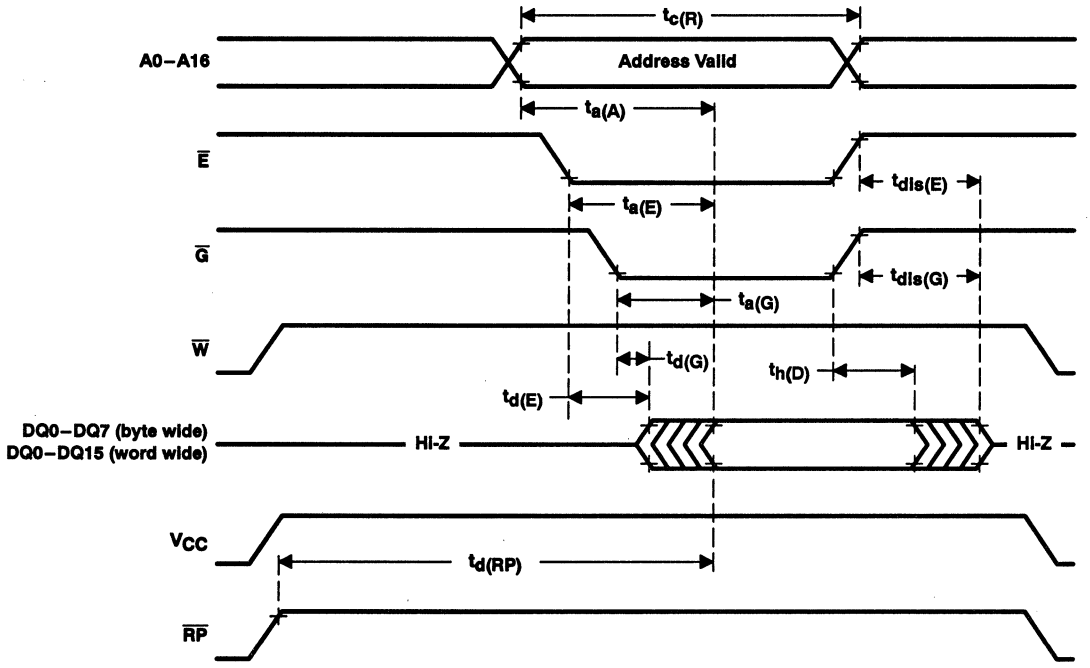


Figure 7. Read-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

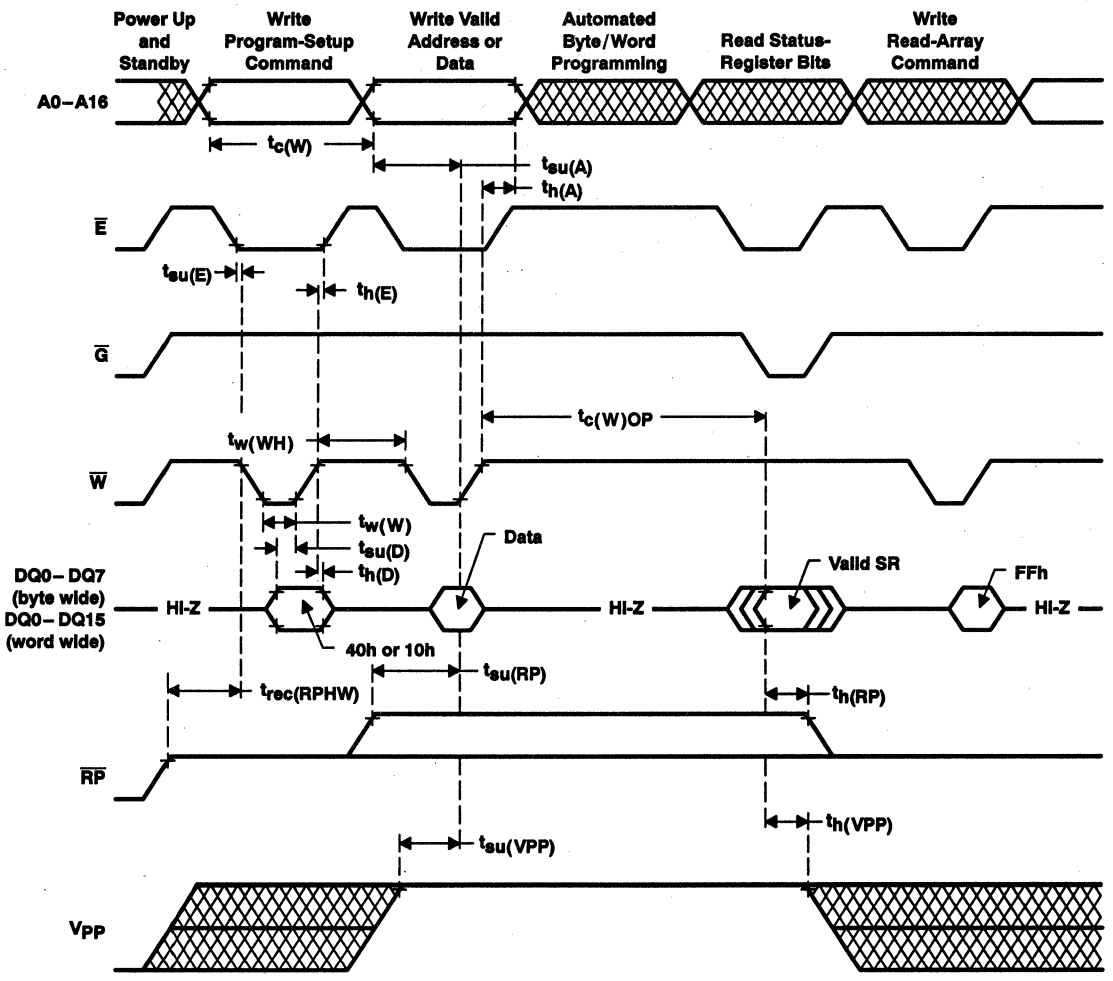


Figure 8. Write-Cycle Timing ($\overline{W}$-Controlled Write)

PARAMETER MEASUREMENT INFORMATION

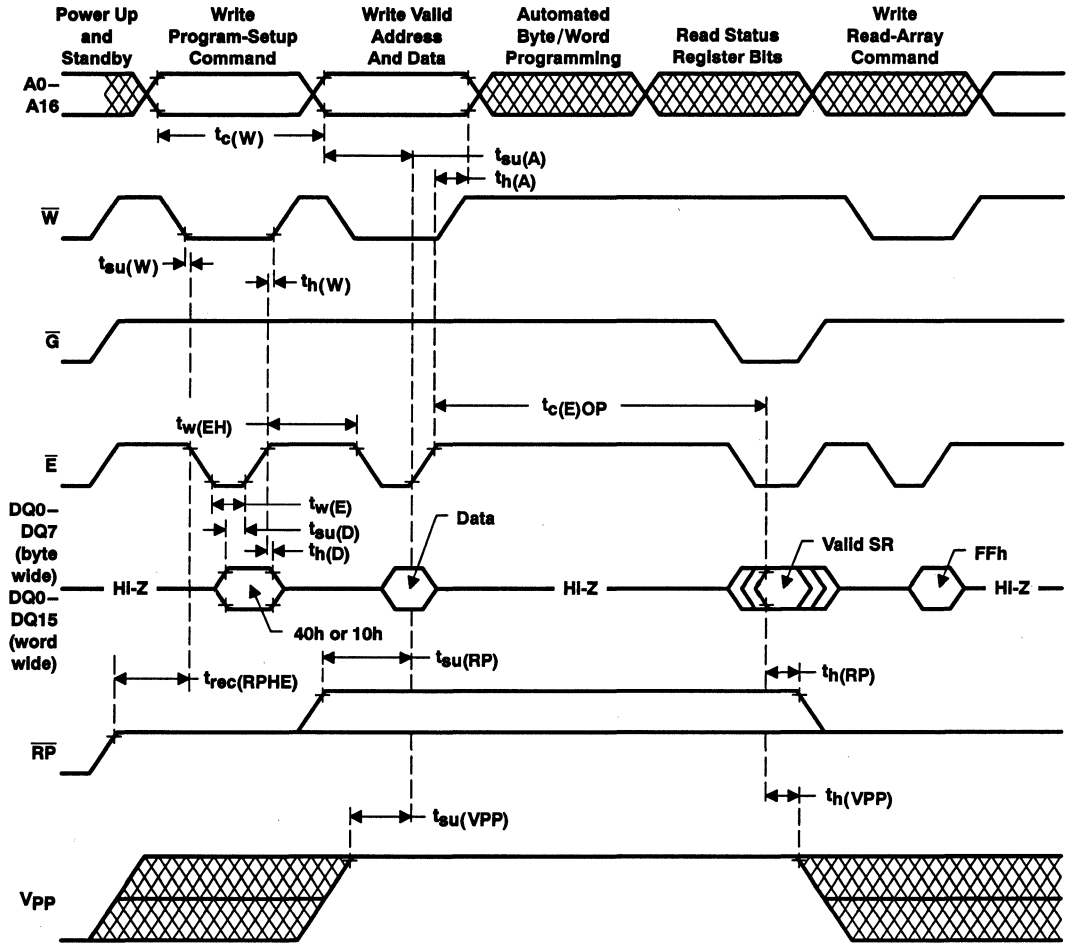


Figure 9. Write-Cycle Timing ($\overline{E}$-Controlled Write)

ADVANCE INFORMATION

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

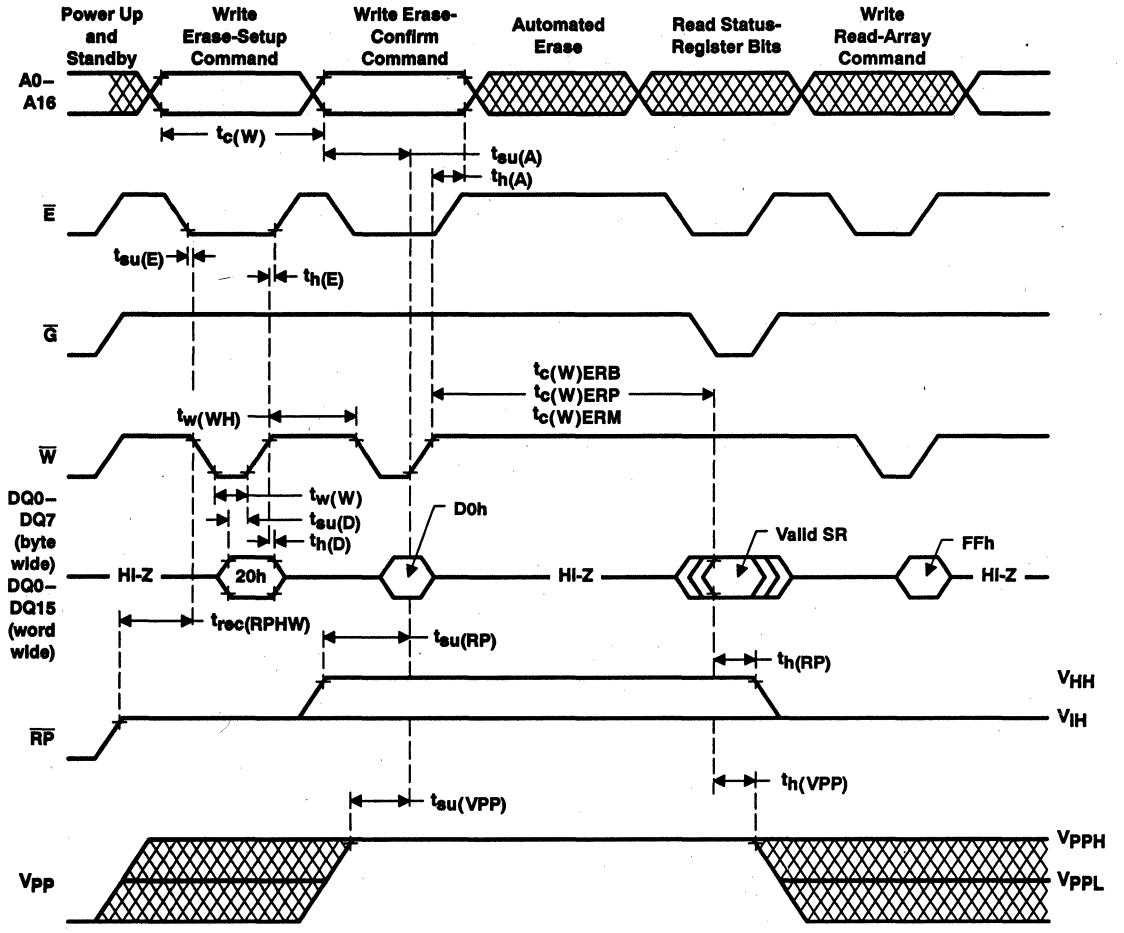


Figure 10. Erase-Cycle Timing ($\overline{W}$-Controlled Write)

PARAMETER MEASUREMENT INFORMATION

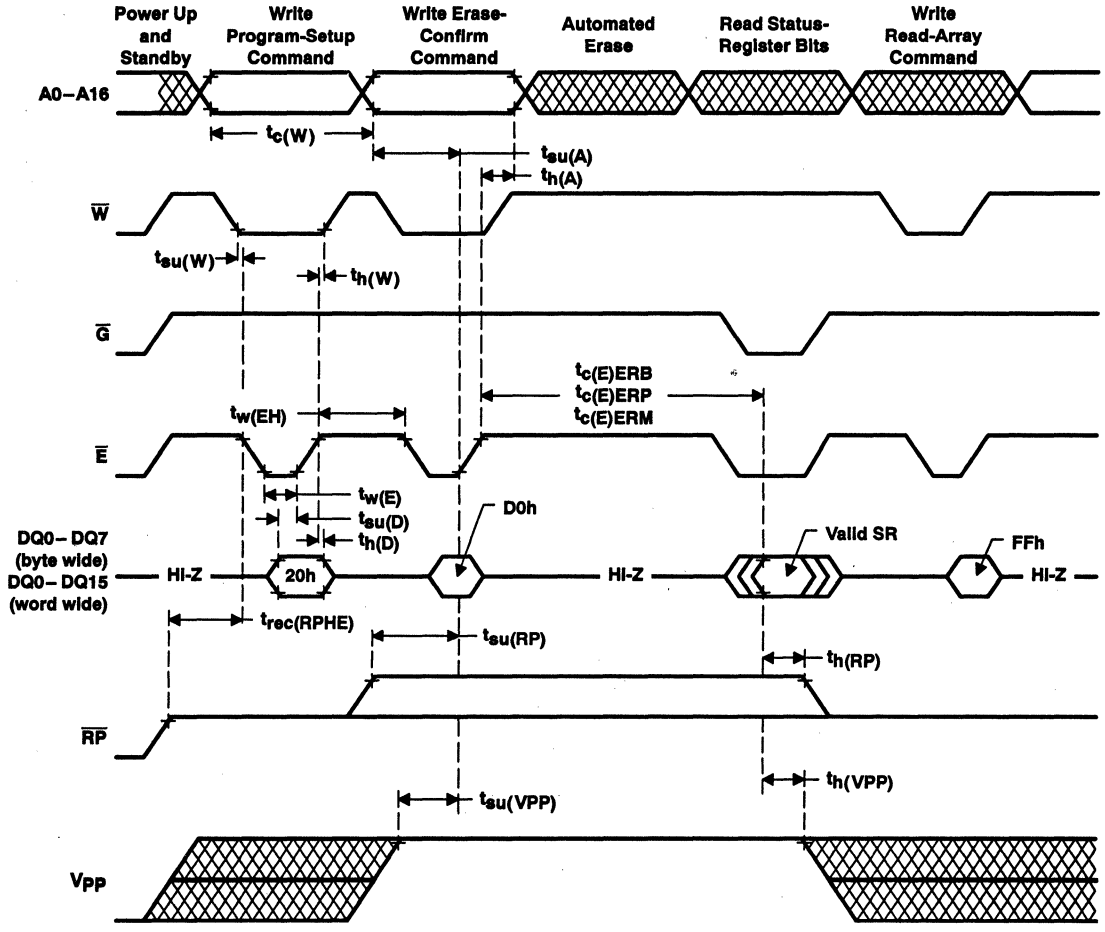


Figure 11. Erase-Cycle Timing ($\overline{E}$-Controlled Write)

ADVANCE INFORMATION

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

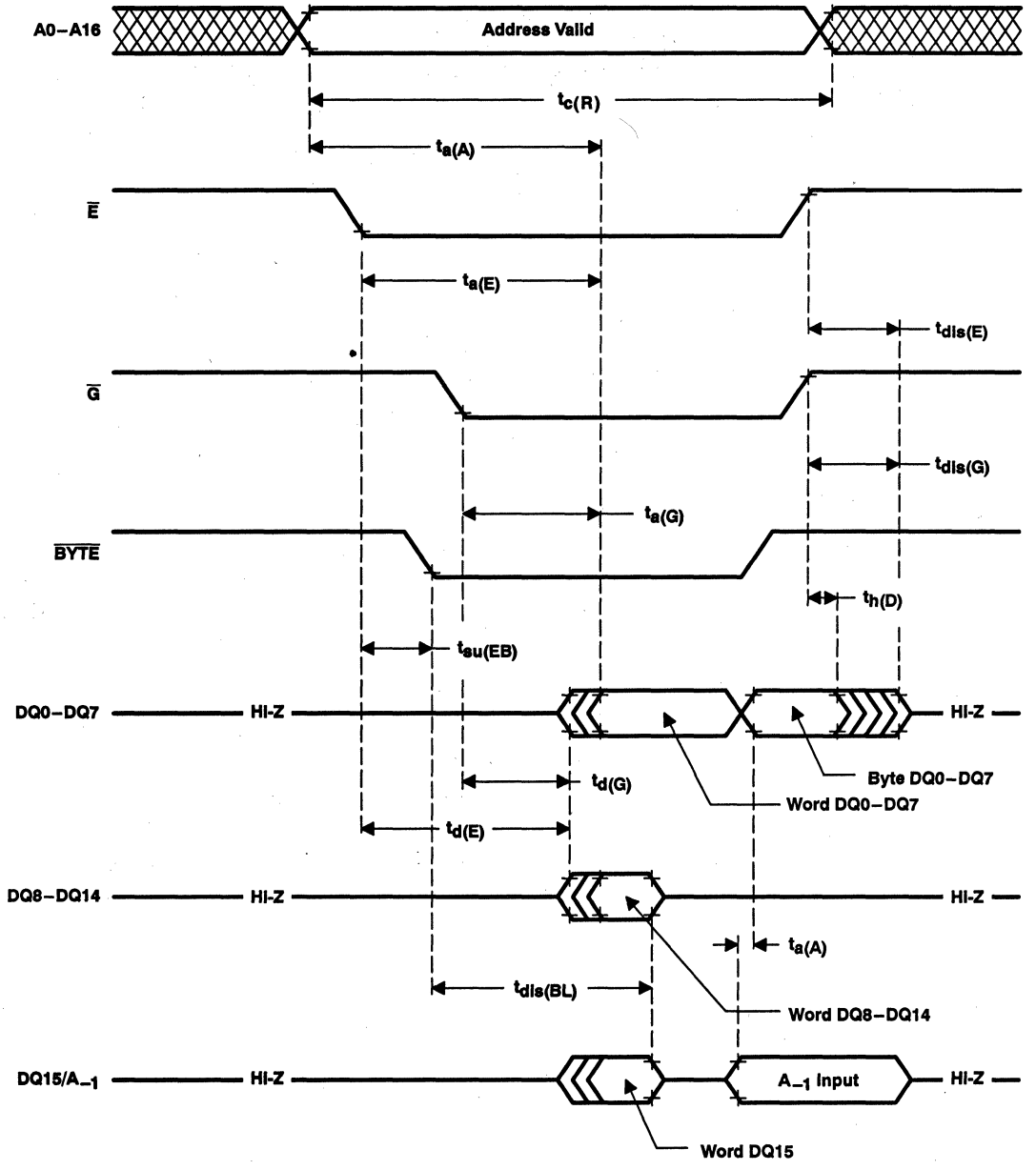


Figure 12. $\overline{BYTE}$ Timing, Changing From Word-Wide to Byte-Wide Mode

PARAMETER MEASUREMENT INFORMATION

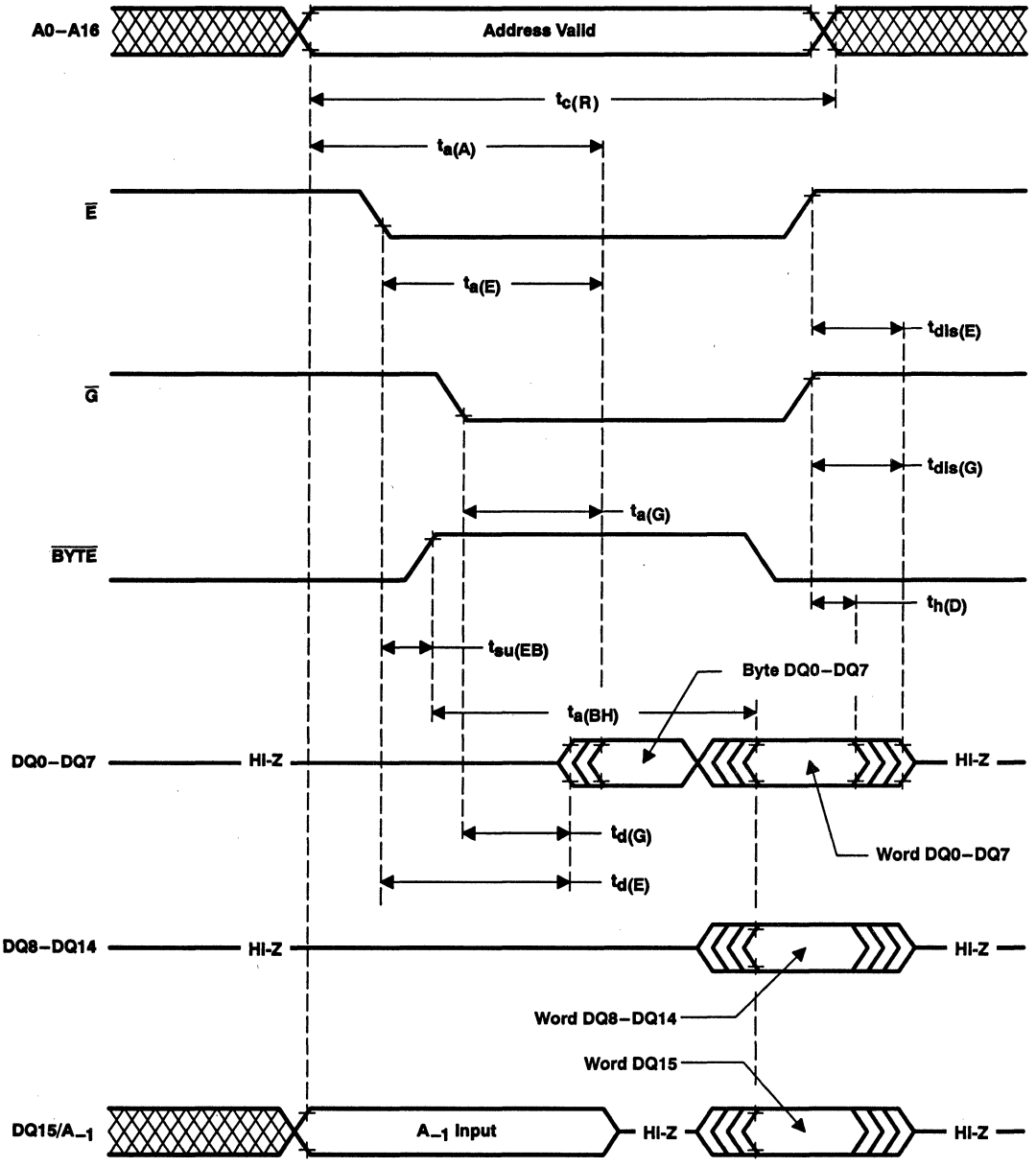


Figure 13. $\overline{BYTE}$ Timing, Changing From Byte-Wide to Word-Wide Mode

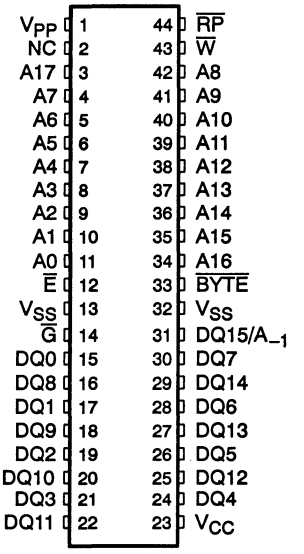
ADVANCE INFORMATION

- **Organization**
  - **Two 8K-Byte Parameter Blocks**
  - **One 96K-Byte Main Block**
  - **Three 128K-Byte Main Blocks**
  - **One 16K-Byte Protected Boot Block**
  - **Top or Bottom Boot Locations**
- **All Inputs/Outputs TTL Compatible**
- **Maximum Access/Minimum Cycle Time**

V_{CC} ± 5%	V_{CC} ± 10%	
'28F400BZ-6-x		60 ns
	'28F400BZ-70-x	70 ns
	'28F400BZ-80-x	80 ns
	'28F400BZ-90-x	90 ns

- **100000 and 10000 Program/Erase Cycle Versions**
- **Three Temperature Ranges**
  - **Commercial . . . 0°C to 70°C**
  - **Extended . . . – 40°C to 85°C**
  - **Automotive . . . – 40°C to 125°C**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active Write . . . 330 mW (Byte Write)**
  - **Active Read . . . 330 mW (Byte Read)**
  - **Active Write . . . 358 mW (Word Write)**
  - **Active Read . . . 330 mW (Word Read)**
  - **Block Erase . . . 165 mW**
  - **Standby . . . 0.55 mW (CMOS-Input Levels)**
  - **Deep Power-Down Mode . . . 0.0066 mW**
- **Fully Automated On-Chip Erase and Word/Byte Program Operations**
- **Write Protection for Boot Block**
- **Command State Machine (CSM)**
  - **Erase Suspend/Resume**
  - **Algorithm-Selection Identifier**

DBJ PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A17	Address Inputs
$\overline{BYTE}$	Byte Enable
DQ0–DQ14	Data In/Out
DQ15/A_{-1}	Data In/Out (word-wide mode), Low-Order Address (byte-wide mode)
DU	Do Not Use
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Internal Connection
$\overline{RP}$	Reset/Deep Power Down
V_{CC}	5-V Power Supply
V_{PP}	12-V Power Supply for Program/Erase
V_{SS}	Ground
$\overline{W}$	Write Enable

ADVANCE INFORMATION

description

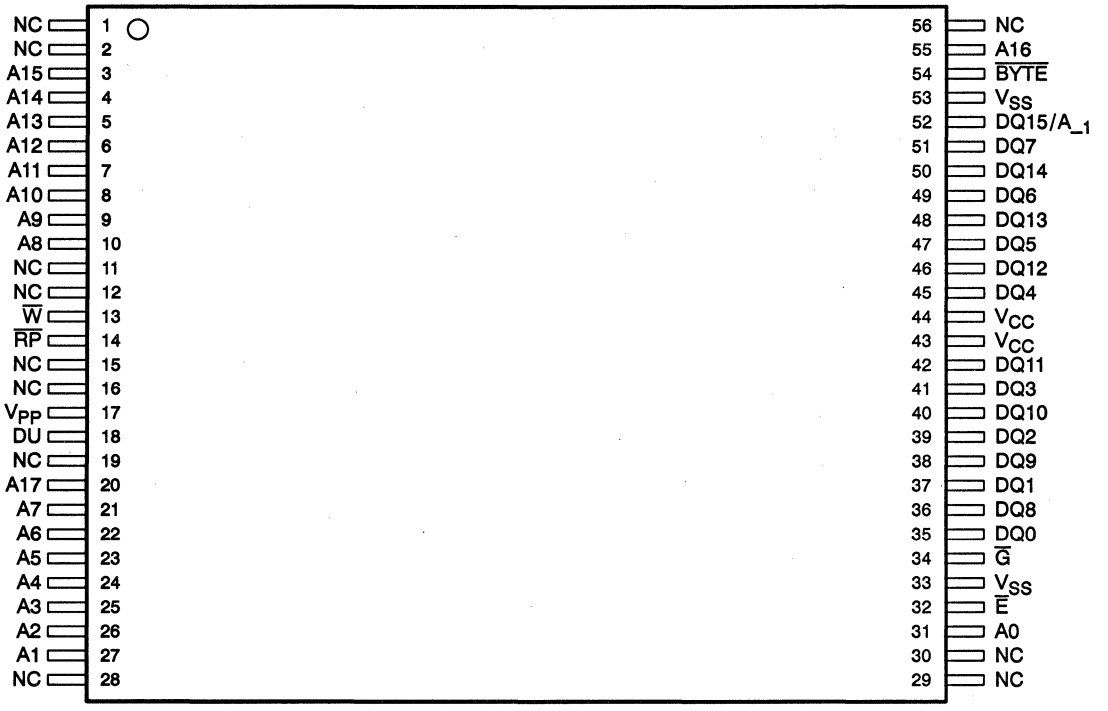
The TMS28F400BZx is a 4194304-bit, boot-block flash memory that can be electrically block-erased and reprogrammed. The TMS28F400BZx is organized in a blocked architecture consisting of one 16K-byte protected boot block, two 8K-byte parameter blocks, one 96K-byte main block, and three 128K-byte main blocks. The device can be ordered with either a top or bottom boot-block configuration. Operation as a 512K-byte (8-bit) or a 256K-word (16-bit) organization is user definable.

Embedded program and block-erase functions are fully automated by an on-chip write state machine (WSM), simplifying these operations and relieving the system microcontroller of these secondary tasks. WSM status can be monitored by an on-chip status register to determine progress of program/erase tasks. The device features user-selectable block erasure.

description (continued)

The TMS28F400BZx flash memory is offered in a 44-pin PSOP and a 56-pin TSOP package and is available in three temperature ranges: 0°C to 70°C, – 40°C to 85°C, and – 40°C to 125°C.

DBR PACKAGE
(TOP VIEW)



device symbol nomenclature

TMS28F400BZT 6 C DBJ L

Temperature Range Designator
L = 0°C to 70°C
E = – 40°C to 85°C
Q = – 40°C to 125°C

Package Designator
DBJ = Plastic Small-Outline Package
DBR = Thin Small-Outline Package

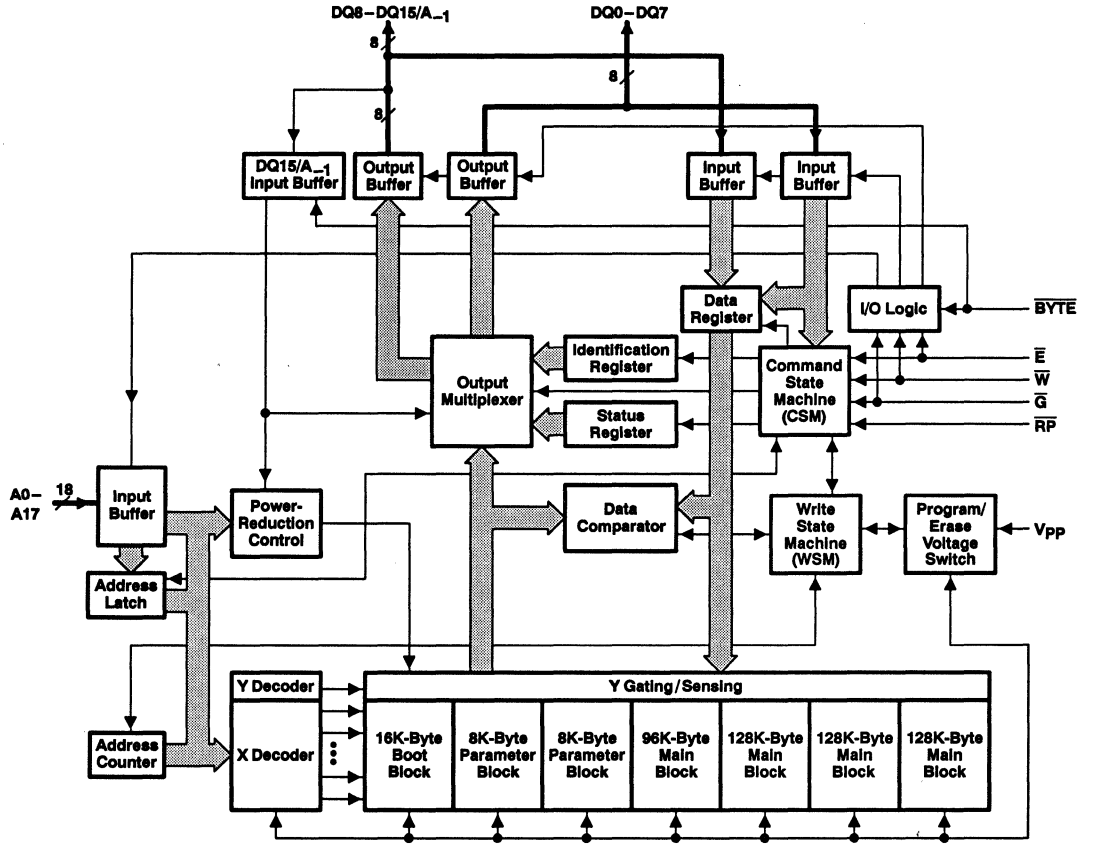
Program/Erase Endurance
C = 100000 Cycles
B = 10000 Cycles

Speed Designator
6 = 60 ns (±5% V_{CC} tolerance)
70 = 70 ns (±10% V_{CC} tolerance)
80 = 80 ns (±10% V_{CC} tolerance)
90 = 90 ns (±10% V_{CC} tolerance)

Boot Block Location Indicator
T = Top Location
B = Bottom Location

ADVANCE INFORMATION

functional block diagram



architecture

The TMS28F400BZx uses a blocked architecture to allow independent erasure of selected memory blocks. Any address within a block address range selects that block for the required read, program, or erase operation.

block memory maps

The TMS28F400BZx is available with the block architecture mapped in either of two configurations: the boot block located at the top or at the bottom of the memory array, as required by different microprocessors. The TMS28F400BZB (bottom boot block) is mapped with the 16K-byte boot block located at the low-order address range (00000h to 01FFFh). The TMS28F400BZT (top boot block) is inverted with respect to the TMS28F400BZB with the boot block located at the high-order address range (3E000h to 3FFFFh). Both of these address ranges are for word-wide mode. Figure 2 and Figure 3 show the memory maps for these configurations.

ADVANCE INFORMATION

block memory maps (continued)

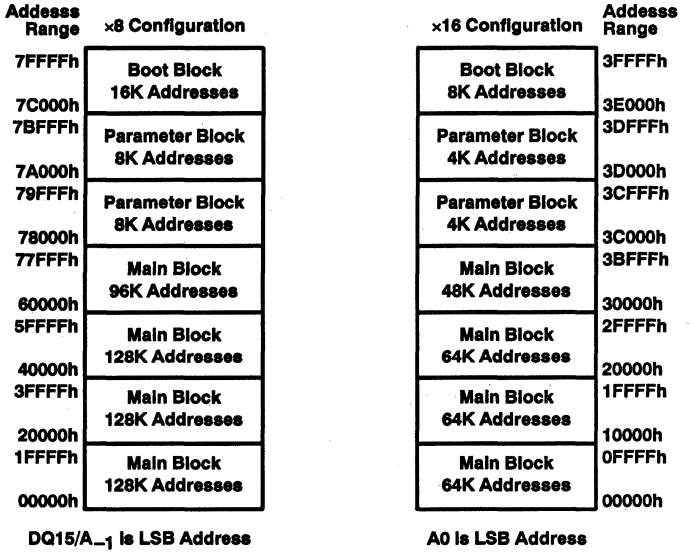


Figure 1. TMS28F400BZT (Top Boot Block) Memory Map

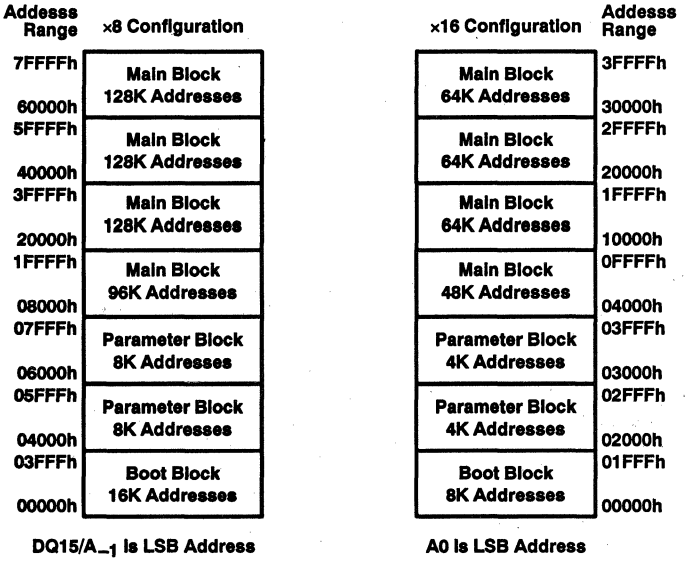


Figure 2. TMS28F400BZB (Bottom Boot Block) Memory Map

ADVANCE INFORMATION

boot-block data protection

The 16K-byte boot block is used to store key system data that is seldom changed in normal operation. To protect data within this memory sector, the $\overline{RP}$ terminal can be used to provide a lockout to eliminate accidental erase or program operations. When $\overline{RP}$ is operated with normal TTL/CMOS logic levels, the contents of the boot block cannot be erased or reprogrammed. Changes to the contents of the boot block can be made only when $\overline{RP}$ is at V_{HH} (nominally 12 V) during normal write/erase operations.

parameter block

Two parameter blocks of 8K bytes each can be used like a scratch pad to store frequently updated data. Alternately, the parameter blocks can be used for additional boot- or main-block data. If a parameter block is used to store additional boot-block data, caution should be exercised because the parameter block does not have the boot-block data-protection safety feature.

main block

Primary memory on the TMS28F400BZx is located in four main blocks. Three of the blocks have storage capacity of 128K bytes and the fourth block has storage capacity of 96K bytes.

command state machine (CSM)

The CSM is the interface between an external microprocessor and the write state machine and status register on the memory chip. When the WSM has completed a task, the WSMS bit (SB7) is set to a logic high (1), allowing the CSM to respond to the full command set.

status register (SR)

The status register provides a means of determining whether the state of a program/erase operation is pending or complete. The status register is read by writing a read-status command to the CSM and reading the resulting status code on I/O terminals DQ0–DQ7. This is valid for operation in either the byte- or word-wide mode. When the device is operating in the word-wide mode, the high order I/Os (DQ8–DQ15) are set to 00h when performing a read-status operation.

After a read-status command has been given, the data appearing on DQ0–DQ7 remains as the status register data until a new command is issued to the CSM. To return the device to other modes of operation, a new command must be issued to the CSM.

Register data is updated on the falling edge of $\overline{G}$ or $\overline{E}$. The latest falling edge of either of these two signals updates the latch within a given read cycle. Latching data prevents errors from occurring should the register input change during a status-register read. To ensure that the status-register output contains updated status data, $\overline{E}$ or $\overline{G}$ must be toggled for each subsequent status read.

The status register provides the internal state of the WSM to the external microprocessor. During periods when the WSM is active, the status register can be polled to determine the WSM status (WSMS). Table 1 defines the status register bits and their functions.

status register (SR) (continued)

Table 1. Status Register Bit Definitions and Functions

STATUS BIT	FUNCTION	DATA	COMMENTS
SB7	Write-state-machine status (WSMS)	1 = Ready 0 = Busy	If SB7 = 0, the WSM has not completed an erase or programming operation. If SB7 = 1 (ready), other polling operations can be performed. SB7 does not automatically update WSM status at the completion of a WSM task. If the WSM status bit shows busy (0), the user must periodically toggle $\overline{E}$ or $\overline{G}$ to determine when the WSM has completed an operation (SB7 = 1).
SB6	Erase-suspend status (ESS)	1 = Erase suspended 0 = Erase in progress or completed	When an erase-suspend command is issued, the WSM halts execution and sets the ESS bit high (SB6 = 1) indicating that the erase operation has been suspended. The WSMS bit is also set high (SB7 = 1) indicating that the erase-suspend operation has been successfully completed. The ESS bit remains at a high level until an erase-resume command is input to the CSM (code D0h).
SB5	Erase status (ES)	1 = Block erase error 0 = Block erase good	SB5 = 0 indicates that a successful block erasure has occurred. SB5 = 1 indicates that an erase error has occurred. In this case, the WSM has completed the maximum allowed erase pulses determined by the internal algorithm, but this was insufficient to completely erase the device.
SB4	Program status (PS)	1 = Byte/word program error 0 = Byte/word program good	SB4 = 0 indicates successful programming has occurred at the addressed block location. SB4 = 1 indicates that the WSM was unable to correctly program the addressed block location.
SB3	V_{PP} status (V_{PPS})	1 = Program abort: V_{PP} too low 0 = V_{PP} good	SB3 provides information on the status of V_{PP} during programming. If V_{PP} is too low after a program or erase command has been issued, SB3 is set to a 1 indicating that the programming operation is aborted. The V_{PP} status bit is not assured to give accurate feedback between V_{PPH} and V_{PPL}.
SB2–SB0	Reserved		These bits should be masked out when reading the status register.

operation

Device operations are selected by entering standard JEDEC 8-bit command codes with conventional microprocessor timing into an on-chip CSM through I/O terminals DQ0–DQ7. When the device is powered up, internal reset circuitry initializes the chip to a read-array mode of operation. Changing the mode of operation requires a command code to be entered into the CSM. Table 2 lists the CSM codes for all modes of operation.

The on-chip status register allows the progress of various operations to be monitored. The status register is interrogated by entering a read-status register command into the CSM (cycle 1) and reading the register data on I/O terminals DQ0–DQ7 (cycle 2). Status-register bits SB0 through SB7 correspond to DQ0 through DQ7.

operation (continued)

Table 2. Command State Machine Codes for Device Mode Selection

COMMAND CODE ON DQ0–DQ7†	DEVICE MODE
00h	Invalid/Reserved
10h	Alternate Program Setup
20h	Block-Erase Setup
40h	Program Setup
50h	Clear Status Register
70h	Read Status Register
90h	Algorithm Selection
B0h	Erase Suspend
D0h	Erase Resume/Block-Erase Confirm
FFh	Read Array

† DQ0 is the least significant bit. DQ8–DQ15 are any valid 2-state level.

command definition

Once a specific command code has been entered, the WSM executes an internal algorithm generating the necessary timing signals to program, erase, and verify data. See Table 3 for the CSM command definitions and data for each of the bus cycles.

Following the read-algorithm-selection-code command, two read cycles are required to access the manufacturer-equivalent code and the device-equivalent code as shown in Table 4 and Table 5.

Table 3. Command Definitions

COMMAND	BUS CYCLES REQUIRED	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION	ADDRESS	CSM INPUT	OPERATION	ADDRESS	DATA IN/OUT
Read Operations							
Read Array	1	Write	X	FFh	Read	X	Data Out
Read Algorithm-Selection Code	3	Write	X	90h	Read	A0	M/D
Read Status Register	2	Write	X	70h	Read	X	SRB
Clear Status Register	1	Write	X	50h			
Program Mode							
Program Setup/Program (byte/word)	2	Write	PA	40h or 10h	Write	PA	PD
Erase Operations							
Block-Erase Setup/ Block-Erase Confirm	2	Write	BEA	20h	Write	BEA	D0h
Erase Suspend/ Erase Resume	2	Write	X	B0h	Write	X	D0h

Legend:

BEA Block-erase address. Any address selected within a block selects that block for erase.
M/D Manufacturer-equivalent/device-equivalent code
PA Address to be programmed
PD Data to be programmed at PA
SRB Status-register data byte that can be found on DQ0–DQ7

ADVANCE INFORMATION

byte-wide or word-wide mode selection

The memory array is divided into two parts: an upper half byte that outputs data through I/Os DQ8–DQ15 and a lower half byte that outputs data through DQ0–DQ7. Device operation in either byte-wide or word-wide mode is user-selectable and is determined by the logic state of $\overline{BYTE}$. When $\overline{BYTE}$ is at a logic high level, the device is in the word-wide mode and data is written to or read from I/Os DQ0–DQ15. When $\overline{BYTE}$ is at a logic low, the device is in the byte-wide mode and data is written to or read from I/Os DQ0–DQ7. In the byte-wide mode, I/Os DQ8–DQ14 are placed in the high-impedance state and DQ15/A_{-1} becomes the low-order address terminal and selects either the upper or lower half of the array. Array data from the upper half (DQ8–DQ15) and the lower half (DQ0–DQ7) are multiplexed and appear on DQ0–DQ7. Table 4 and Table 5 summarize operations for word-wide mode and byte-wide mode.

Table 4. Operation Modes for Word-Wide Mode ($\overline{BYTE}$ = V_{IH})

MODE	$\overline{E}$	$\overline{G}$	$\overline{RP}$	$\overline{W}$	A9	A0	V_{PP}	DQ0–DQ15
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	Data out
Algorithm-selection mode	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IL}	X	Manufacturer-equivalent code 0089h
	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IH}	X	Device-equivalent code 4470h (top boot block)
								Device-equivalent code 4471h (bottom boot block)
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	High impedance
Standby	V_{IH}	X	V_{IH}	X	X	X	X	High impedance
Reset/deep power down	X	X	V_{IL}	X	X	X	X	High impedance
Write (see Note 1)	V_{IL}	V_{IH}	V_{IH} or V_{HH}	V_{IL}	X	X	V_{PPL} or V_{PPH}	Data in

Table 5. Operation Modes for Byte-Wide Mode ($\overline{BYTE}$ = V_{IL})

MODE	$\overline{E}$	$\overline{G}$	$\overline{RP}$	$\overline{W}$	A9	A0	V_{PP}	DQ15/A_{-1}	DQ8–DQ14	DQ0–DQ7
Read lower byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	V_{IL}	Hi-Z	Data out
Read upper byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	V_{IH}	Hi-Z	Data out
Algorithm-selection mode	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IL}	X	X	Hi-Z	Manufacturer-equivalent code 89h
	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IH}	X	X	Hi-Z	Device-equivalent code 70h (top boot block)
										Device-equivalent code 71h (bottom boot block)
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	X	Hi-Z	High impedance
Standby	V_{IH}	X	V_{IH}	X	X	X	X	X	Hi-Z	High impedance
Reset/deep power down	X	X	V_{IL}	X	X	X	X	X	Hi-Z	High impedance
Write (see Note 1)	V_{IL}	V_{IH}	V_{IH} or V_{HH}	V_{IL}	X	X	V_{PPL} or V_{PPH}	X	Hi-Z	Data in

NOTE 1: When writing commands to the '28F400BZx, V_{PP} must be V_{PPH} for block-erase or program commands to be executed and $\overline{RP}$ must be held at V_{HH} for the entire boot-block program or erase operation.

command state machine (CSM) operations

The CSM decodes instructions for read array, read algorithm-selection code, read status register, clear status register, program, erase, erase suspend, and erase resume. The 8-bit command code is input to the device on DQ0–DQ7 (see Table 2 for CSM codes). During a program or erase cycle, the CSM informs the WSM that a program or erase cycle has been requested. During a program cycle, the WSM controls the program sequences and the CSM responds only to status reads.

During an erase cycle, the CSM responds to status reads and the erase suspend command. When the WSM has completed its task, the WSM status bit (SB7) is set to a logic high and the CSM responds to the full command set. The CSM stays in the current command state until the microprocessor issues another command.

The WSM successfully initiates an erase or program operation only when V_{PP} is within its correct voltage range (V_{PPH}). For data protection, it is recommended that $\overline{RP}$ be held at a logic low during a CPU reset.

read operations

There are three read operations available: read array, read algorithm-selection code, and read status register.

read array

The array is read by entering the command code FFh on DQ0–DQ7. Control terminals $\overline{E}$ and $\overline{G}$ must be at a logic low (V_{IL}) and $\overline{W}$ and $\overline{RP}$ must be at a logic high (V_{IH}) to read data from the array. Data is available on DQ0–DQ15 (word-wide mode) or DQ0–DQ7 (byte-wide mode). Any valid address within any of the blocks selects that block and allows data to be read from the block.

read algorithm-selection code

Algorithm-selection codes are read by entering command code 90h on DQ0–DQ7. Two bus cycles are required for this operation. The first bus cycle is used to enter the command code and the second bus cycle is used to read the device-equivalent code. Control terminals $\overline{E}$ and $\overline{G}$ must be at a logic low (V_{IL}) and $\overline{W}$ and $\overline{RP}$ must be at a logic high (V_{IH}). Two identifier bytes are accessed by toggling A0. The manufacturer-equivalent code is obtained on DQ0–DQ7 with A0 at a logic low (V_{IL}). The device-equivalent code is obtained when A0 is set to a logic high (V_{IH}). Alternately, the manufacturer- and device-equivalent codes can be read by applying V_{ID} (nominally 12 V) to A9 and selecting the desired code by toggling A0 high or low. All other addresses are don't care (see Table 3, Table 4, and Table 5).

read status register

The status register is read by entering the command code 70h on DQ0–DQ7. Control terminals $\overline{E}$ and $\overline{G}$ must be at a logic low (V_{IL}) and $\overline{W}$ and $\overline{RP}$ must be at a logic high (V_{IH}). Two bus cycles are required for this operation: one to enter the command code and a second to read the status register. In a given read cycle, status register contents are updated on the falling edge of $\overline{E}$ or $\overline{G}$, whichever occurs last within the cycle.

clear status register

The internal circuitry can set only the V_{PP} status bit (SB3), the program status bit (SB4) and the erase status bit (SB5) bits of the status register. The clear status register command (50h) allows the external microprocessor to clear these status bits and synchronize to internal operations. When the status bits are cleared, the device returns to the read array mode.

boot-block programming/erasing

Should changes to the boot block be required, $\overline{RP}$ must be set to V_{HH} (12 V) and V_{PP} to the programming voltage level (V_{PPH}). If an attempt is made to write, erase or erase-suspend the boot block without $\overline{RP}$ at V_{HH}, an error signal is generated on SB4 (program-status bit) or SB5 (erase-status bit).

A program-setup command can be aborted by writing FFh (in byte-wide mode) or FFFFh (in word-wide mode) during the second cycle. After writing FFh or FFFFh during the second cycle, the CSM responds only to status reads. When the WSM status bit (SB7) is set to a logic high, signifying the nonprogram operation is terminated, all commands to the CSM become valid again.

normal programming

There are two CSM commands for programming: program setup and alternate program setup (see Table 2). After the desired command code is entered, the WSM takes over and correctly sequences the device to complete the program operation. During this time, the CSM responds only to status reads until the program operation has been completed, after which all commands to the CSM become valid again. Once a program command has been issued, the WSM cannot normally be interrupted until the program algorithm has been completed (see Figure 4 and Figure 4). Taking $\overline{RP}$ to V_{IL} during programming aborts the program operation. During programming, V_{PP} must remain at V_{PPH}. Only 0s are written and compared during a program operation. If 1s are programmed, the memory cell contents do not change and no error occurs.

A program-setup command can be aborted by writing FFh (in byte-wide mode) or FFFFh (in word-wide mode) during the second cycle. After writing all 1s during the second cycle, the CSM responds only to status reads. When the WSM status bit (SB7) is set to a logic high, signifying the nonprogram operation is terminated, all commands to the CSM become valid again.

erase operations

There are two erase operations that can be performed by the TMS28F400BZx devices: block erase and erase suspend/erase resume. An erase operation must be used to initialize all bits in an array block to 1s. After block-erase confirm is issued, the CSM responds only to status reads or erase-suspend commands until the WSM completes its task.

block erasure

Block erasure inside the memory array sets all bits within the addressed block to logic 1s. Erasure is accomplished only by blocks; data at single address locations within the array cannot be individually erased. Any valid address within the parameter or main blocks acts as a block selector and allows that block to be erased. $\overline{RP}$ must be at V_{HH} for changing the data content of the boot block. Block erasure is initiated by a command sequence to the CSM: block-erase setup (20h) followed by block-erase confirm (D0h). A two-command erase sequence protects against accidental erasure of memory contents.

Erase setup and confirm commands are latched on the rising edge of $\overline{E}$ or $\overline{W}$, whichever occurs first. Block addresses are latched during the block-erase-confirm command on the rising edge of $\overline{E}$ or $\overline{W}$ (see Figure 5). When the block-erase-confirm command is complete, the WSM automatically executes a sequence of events to complete the block erasure. During this sequence, the block is programmed with logic 0s, data is verified, all bits in the block are erased, and finally, verification is performed to ensure that all bits are correctly erased. Monitoring of the erase operation is possible through the status register (see read status register).

erase suspend/erase resume

During the execution of an erase operation, the erase-suspend command (B0h) can be entered to direct the WSM to suspend the erase operation. Once the WSM has reached the suspend state, it allows the CSM to respond only to the read-array, read-status-register, and erase-resume commands. During the erase-suspend operation, array data should be read from a block other than the one being erased. To resume the erase operation, an erase-resume command (D0h) must be issued to cause the CSM to clear the suspend state previously set (see Figure 5 and Figure 10).

automatic power-saving mode

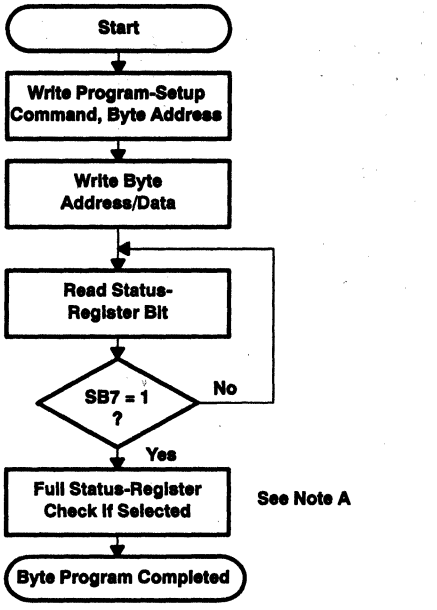
Substantial power savings can be realized during periods when the array is not being read. During this time, the device switches to the automatic power-saving mode. When the device switches to this mode, I_{CC} is typically reduced from 40 mA to 1 mA (I_{OUT} = 0 mA). The low level of power is maintained until another read operation is initiated. In this mode, the I/O terminals retain the data from the last memory address read until a new address is read. This mode is entered automatically if no address or control pins toggle within a 200-ns time-out period. At least one transition on $\overline{E}$ must occur after power up to activate this mode.

reset/deep power-down mode

Very low levels of power consumption can be attained by using a special terminal, $\overline{RP}$, disable internal device circuitry. When $\overline{RP}$ is at a CMOS logic low of 0.0 V ± 0.2 V, an I_{CC} value on the order of 0.2 μA, or 1 μW of power, is achievable. This is important in portable applications where extended battery life is of major concern.

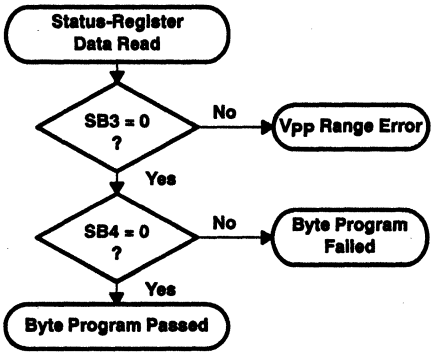
A recovery time is required when exiting from deep power-down mode. For a read-array operation, a minimum of 300 ns is required before data is valid, and a minimum of 215 ns in deep power-down mode is required before data input to the CSM can be recognized. With $\overline{RP}$ at ground, the WSM is reset and the status register is cleared, effectively eliminating accidental programming to the array during system reset. After restoration of power, the device does not recognize any operation command until $\overline{RP}$ is returned to a V_{IH} or V_{HH} level.

Should $\overline{RP}$ become low during a program or erase operation, the device becomes nonfunctional (is in a power-down state) and data being written or erased is invalid or indeterminate, requiring that the operation be performed again after power restoration.



BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h or 10h Addr = Address of byte to be programmed
Write	Write data	Data = Byte to be programmed Addr = Address of byte to be programmed
Read		Status register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register.
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent bytes. Write FFh after the last byte-programming operation to reset the device to read array mode.		

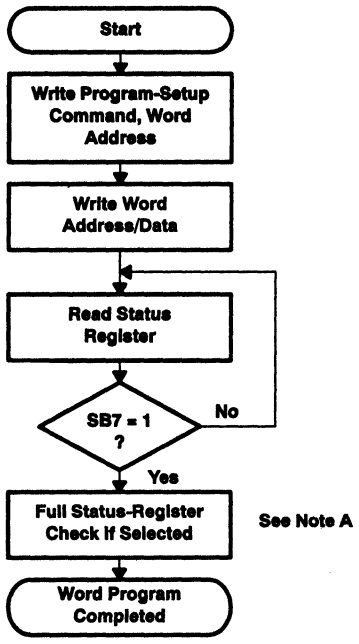
FULL STATUS-REGISTER-CHECK FLOW



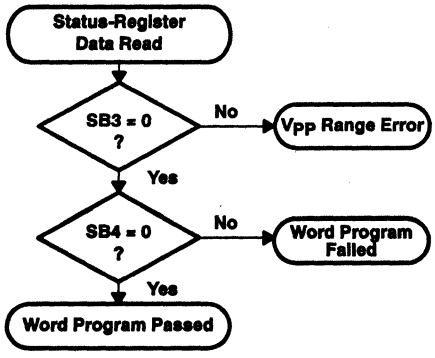
BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect VPP low (see Note B)
Standby		Check SB4 1 = Byte program error (see Note C)

NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB4 is cleared only by the clear-status-register command, but it does not prevent additional program operation attempts.

Figure 3. Automated Byte-Programming Flowchart



FULL STATUS-REGISTER-CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h or 10h Addr = Address of word to be programmed
Write	Write data	Data = Word to be programmed Addr = Address of word to be programmed
Read		Status register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register.
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write FFh after the last word-programming operation to reset the device to read array mode.		

BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 1 = Word program failed (see Note C)

NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB4 is cleared only by the clear-status-register command, but it does not prevent additional program operation attempts.

Figure 4. Automated Word-Programming Flowchart

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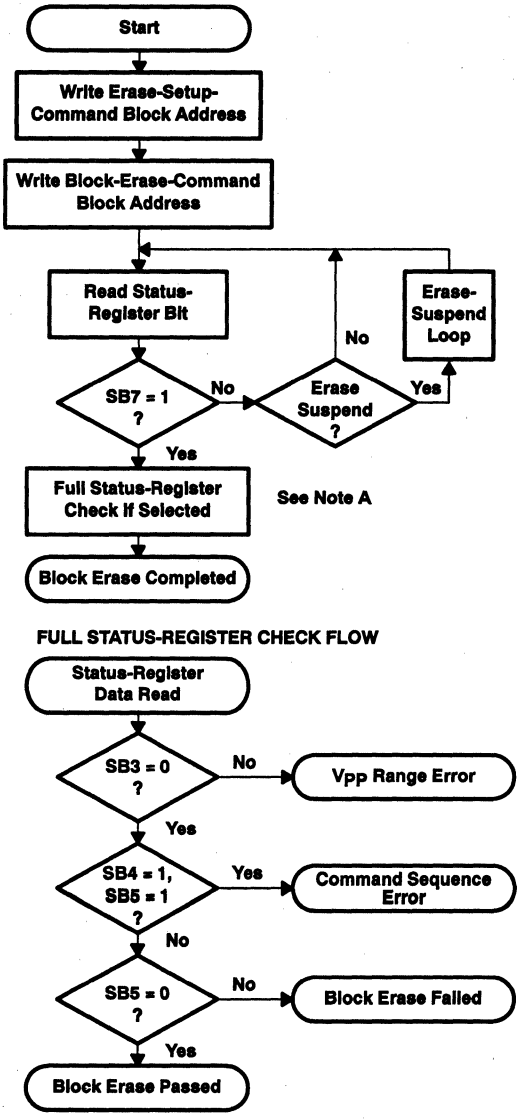


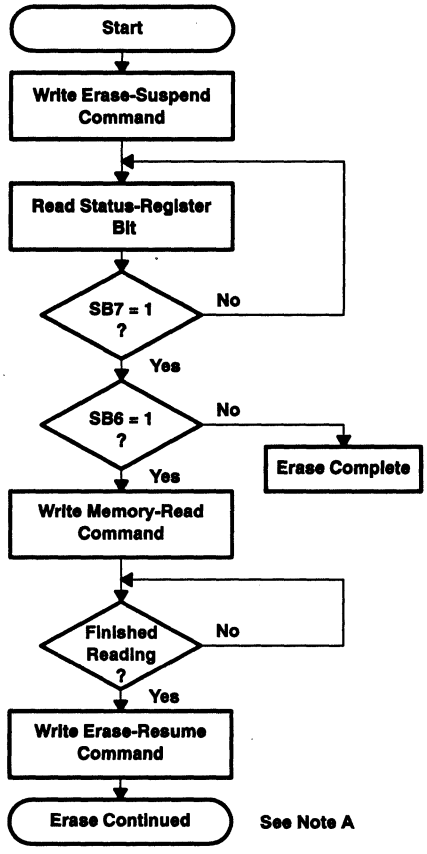
BUS OPERATION	COMMAND	COMMENTS
Write	Write erase setup	Data = 20h Block Addr = Address within block to be erased
Write	Erase	Data = D0h Block Addr = Address within block to be erased
Read		Status register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent blocks. Write FFh after the last block-erase operation to reset the device to read array mode.		

FULL STATUS-REGISTER CHECK FLOW

BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 and SB5 1 = Block-erase command error
Standby		Check SB5 1 = Block erase failed (see Note C)

NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB5 is cleared only by the clear-status-register command in cases where multiple blocks are erased before full status is checked.

Figure 5. Automated Block-Erase Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Erase suspend	Data = B0h
Read		Status register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register.
Standby		Check SB7 1 = Ready
Standby		Check SB6 1 = Suspended
Write	Read memory	Data = FFh
Read		Read data from block other than that being erased.
Write	Erase resume	Data = D0h

NOTE A: Refer to automated block-erase flowchart for complete erasure procedure.

Figure 6. Erase-Suspend/Resume Flowchart

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 2) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 2) ..... – 0.6 V to 14 V
Input voltage range: All inputs except A9, $\overline{RP}$ ..... – 0.6 V to V_{CC} + 1 V
$\overline{RP}$, A9 (see Note) ..... – 0.6 V to 13.5 V
Output voltage range (see Note 4) ..... – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range, T_A, during read/erase/program: L suffix ..... 0°C to 70°C
E suffix ..... – 40°C to 85°C
Q suffix ..... – 40°C to 125°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. All voltage values are with respect to V_{SS}.
3. The voltage on any input can undershoot to – 2 V for periods less than 20 ns.
4. The voltage on any output can overshoot to 7 V for periods less than 20 ns.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During write/read/erase/erase suspend	'28F400BZx-6	4.75	5	5.25	V
			All others	4.5	5	5.5	
V_{PP}	Supply voltage	During read only (V_{PPL})		0		6.5	V
		During write/erase/erase suspend (V_{PPH})		11.4	12	12.6	V
V_{IH}	High-level dc input voltage		TTL	2		V_{CC} + 0.5	V
			CMOS	V_{CC} – 0.5		V_{CC} + 0.5	V
V_{IL}	Low-level dc input voltage		TTL	– 0.5		0.8	V
			CMOS	V_{SS} – 0.2		V_{SS} + 0.2	V
V_{LKO}	V_{CC} lock-out voltage from write/erase			2			V
V_{HH}	$\overline{RP}$ unlock voltage			11.5	12	13	V

word/byte-write and block-erase performance, T_A = 25°C, V_{PP} = 12 V (see Note 5)

PARAMETER	'28F400BZx-6			'28F400BZx-70			'28F400BZx-80			'28F400BZx-90			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Main-block erase time		2.2			2.2			2.2			2.2		s
Main-block byte-program time		3.2			3.2			3.2			3.2		s
Main-block word-program time		1.6			1.6			1.6			1.6		s
Parameter/boot-block erase time		0.32			0.32			0.32			0.32		s

NOTE 5: Excludes system-level overhead

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature using test conditions given in Table 6 (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage			V_{CC} = 4.5 V, I_{OH} = −2.5 mA	2.4		V
V_{OL}	Low-level output voltage			V_{CC} = 4.5 V, I_{OL} = 5.8 mA		0.45	V
V_{ID}	A9 selection code voltage				11.5	13	V
I_I	Input current (leakage), except for A9 when A9 = V_{ID}			V_{CC} = 5.5 V, V_I = 0 V to 5.5 V		±1	µA
I_{ID}	A9 selection code current			A9 = V_{ID}		500	µA
I_{RP}	$\overline{RP}$ boot-block unlock current					500	µA
I_O	Output current (leakage)			V_{CC} = 5.5 V, V_O = 0 V to V_{CC}		±10	µA
I_{PPS}	V_{PP} standby current (standby)			$V_{PP} \leq V_{CC}$		10	µA
I_{PPL}	V_{PP} supply current (reset/deep power-down mode)			$\overline{RP}$ = V_{SS} ± 0.2 V		5	µA
I_{PP1}	V_{PP} supply current (read)			$V_{PP} > V_{CC}$		200	µA
I_{PP2}	V_{PP} supply current (active byte write)			V_{PP} = V_{PPH}, Programming in progress		30	mA
I_{PP3}	V_{PP} supply current (active word write)			V_{PP} = V_{PPH}, Programming in progress		40	mA
I_{PP4}	V_{PP} supply current (block erase)			V_{PP} = V_{PPH}, Block erase in progress		30	mA
I_{PP5}	V_{PP} supply current (erase suspend)			V_{PP} = V_{PPH}, Block erase suspended		200	µA
I_{CCS}	V_{CC} supply current (standby)	TTL-input level		V_{CC} = 5.5 V, $\overline{E}$ = $\overline{RP}$ = V_{IH}		1.5	mA
		CMOS-input level		V_{CC} = 5.5 V, $\overline{E}$ = $\overline{RP}$ = V_{IH}		100	µA
I_{CCL}	V_{CC} supply current (reset/deep power-down mode)		0°C to 70°C −40°C to 85°C	RP = V_{SS} ± 0.2 V		1.2	µA
			−40°C to 125°C			8	µA
I_{CC1}	V_{CC} supply current (active read)	TTL-input level		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA		60	mA
		CMOS-input level		V_{CC} = 5.5 V, $\overline{E}$ = V_{SS} ± 0.2 V, f = 10 MHz, I_{OUT} = 0 mA		55	mA
I_{CC2}	V_{CC} supply current (active byte write) (see Notes 10 and 11)			V_{CC} = 5.5 V, Programming in progress		60	mA
I_{CC3}	V_{CC} supply current (active word write) (see Notes 10 and 11)			V_{CC} = 5.5 V, Programming in progress		65	mA
I_{CC4}	V_{CC} supply current (block erase) (see Notes 10 and 11)			V_{CC} = 5.5 V, Block erase in progress		30	mA
I_{CC5}	V_{CC} supply current (erase suspend) (see Notes 10 and 11)			V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}, Block erase suspended		10	mA

NOTES: 6. Not 100% tested; characterization data available
7. All current values are RMS unless otherwise noted.

Table 6. AC Test Conditions

SPEED DESIGNATOR	I_{OL} (mA)	I_{OH} (mA)	V_Z† (V)	V_{OL} (V)	V_{OH} (V)	V_{IL} (V)	V_{IH} (V)	C_{LOAD} (pF)	t_f (ns)	t_r (ns)	TEMPERATURE
-6	5.8	−2.5	1.5	1.5	1.5	0	3.0	30	<10	<10	0°C to 70°C
-70, -80, -90	5.8	−2.5	1.5	0.8	2.0	0.45	2.4	100	<10	<10	−40°C to 125°C

† V_Z is the measured value used to detect high impedance.

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz, V_I = 0 V

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_i	Input capacitance			8	pF
C_o	Output capitance	V_O = 0 V		12	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	'28F400BZx-6		'28F400BZx-70		'28F400BZx-80		'28F400BZx-90		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from A0–A17	t_{AVQV}		60		70		80		90	ns
$t_{a(E)}$	Access time from $\overline{E}$	t_{ELQV}		60		70		80		90	ns
$t_{a(G)}$	Access time from $\overline{G}$	t_{GLQV}		30		35		40		45	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	60		70		80		90		ns
$t_{d(E)}$	Delay time, $\overline{E}$ low to low-impedance output	t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-impedance output	t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Disable time, $\overline{E}$ to high-impedance output	t_{EHQZ}		20		25		30		35	ns
$t_{dis(G)}$	Disable time, $\overline{G}$ to high-impedance output	t_{GHQZ}		20		25		30		35	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A17, $\overline{E}$, or $\overline{G}$, whichever occurs first	t_{AXQX}	0		0		0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{E}$ low	t_{ELFL} t_{ELFH}		5		5		5		5	ns
$t_{d(RP)}$	Output delay time from $\overline{RP}$ high	t_{PHQV}		300		300		300		300	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in high-impedance state	t_{FLQV}		20		25		30		35	ns
$t_{a(BH)}$	Access time from $\overline{BYTE}$ switching high	t_{FHQV}		60		70		80		90	ns

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

write/erase operations — $\overline{W}$-controlled writes

		ALT. SYMBOL	'28F400BZx-6		'28F400BZx-70		'28F400BZx-80		'28F400BZx-90		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	60		70		80		90		ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6		6		6		7		µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3		0.3		0.3		0.4		s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3		0.3		0.3		0.4		s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6		0.6		0.6		0.7		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100		100		100	ns
$t_{h(A)}$	Hold time, A0–A17	t_{WHAX}	10		10		10		10		ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0		0		0		0		ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	10		10		10		10		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status register bit	t_{QVVL}	0		0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status register bit	t_{QVPH}	0		0		0		0		ns
$t_{su(A)}$	Setup time, A0–A17	t_{AVWH}	50		50		50		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	50		50		50		50		ns
$t_{su(E)}$	Setup time, $\overline{E}$ before write operation	t_{ELWL}	0		0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{W}$ going high	t_{PHHWH}	100		100		100		100		ns
$t_{su(VPP)}$	Setup time, V_{PP} to $\overline{W}$ going high	t_{VPWH}	100		100		100		100		ns
$t_{w(W)}$	Pulse duration, $\overline{W}$ low	t_{WLWH}	50		50		50		50		ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WLWL}	10		20		30		30		ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{W}$ going low	t_{PHWL}	215		215		215		215		ns

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

write/erase operations — $\overline{E}$-controlled writes

		ALT. SYMBOL	'28F400BZx-6		'28F400BZx-70		'28F400BZx-80		'28F400BZx-90		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{E}$	t_{AVAV}	60		70		80		90		ns
$t_{c(E)OP}$	Cycle time, duration of programming operation using $\overline{E}$	t_{EHQV1}	6		6		6		7		µs
$t_{c(E)ERB}$	Cycle time, erase operation using $\overline{E}$ (boot block)	t_{EHQV2}	0.3		0.3		0.3		0.4		s
$t_{c(E)ERP}$	Cycle time, erase operation using $\overline{E}$ (parameter block)	t_{EHQV3}	0.3		0.3		0.3		0.4		s
$t_{c(E)ERM}$	Cycle time, erase operation using $\overline{E}$ (main block)	t_{EHQV4}	0.6		0.6		0.6		0.7		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100		100		100	ns
$t_{h(A)}$	Hold time, A0–A17	t_{EHAX}	10		10		10		10		ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0		0		0		0		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	10		10		10		10		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		0		ns
$t_{su(A)}$	Setup time, A0–A17	t_{AVEH}	50		50		50		50		ns
$t_{su(D)}$	Setup time, DQ valid	t_{DVEH}	50		50		50		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before $\overline{E}$	t_{WLEL}	0		0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{E}$ going high	t_{PHHEH}	100		100		100		100		ns
$t_{su(VPP)}$	Setup time, V_{PP} to $\overline{E}$ going high	t_{VPEH}	100		100		100		100		ns
$t_{w(E)}$	Pulse duration, $\overline{E}$ low, write using $\overline{E}$	t_{ELEH}	50		50		50		50		ns
$t_{w(EH)}$	Pulse duration, $\overline{E}$ high, write using $\overline{E}$	t_{EHEL}	10		20		30		30		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{E}$ going low	t_{PHEL}	215		215		215		215		ns

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

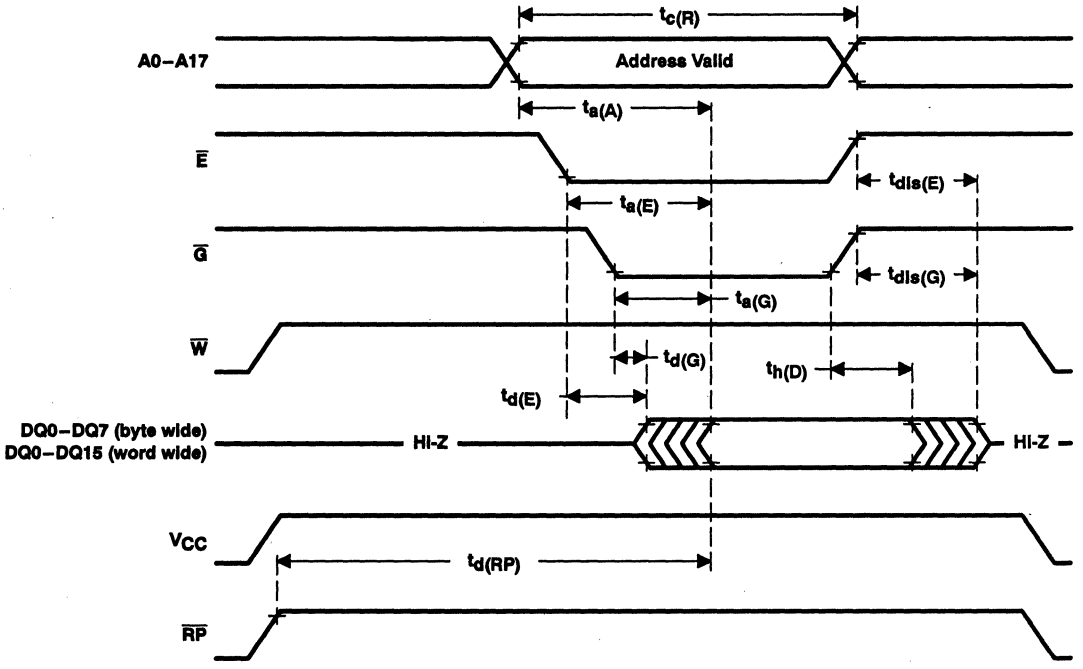


Figure 7. Read-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

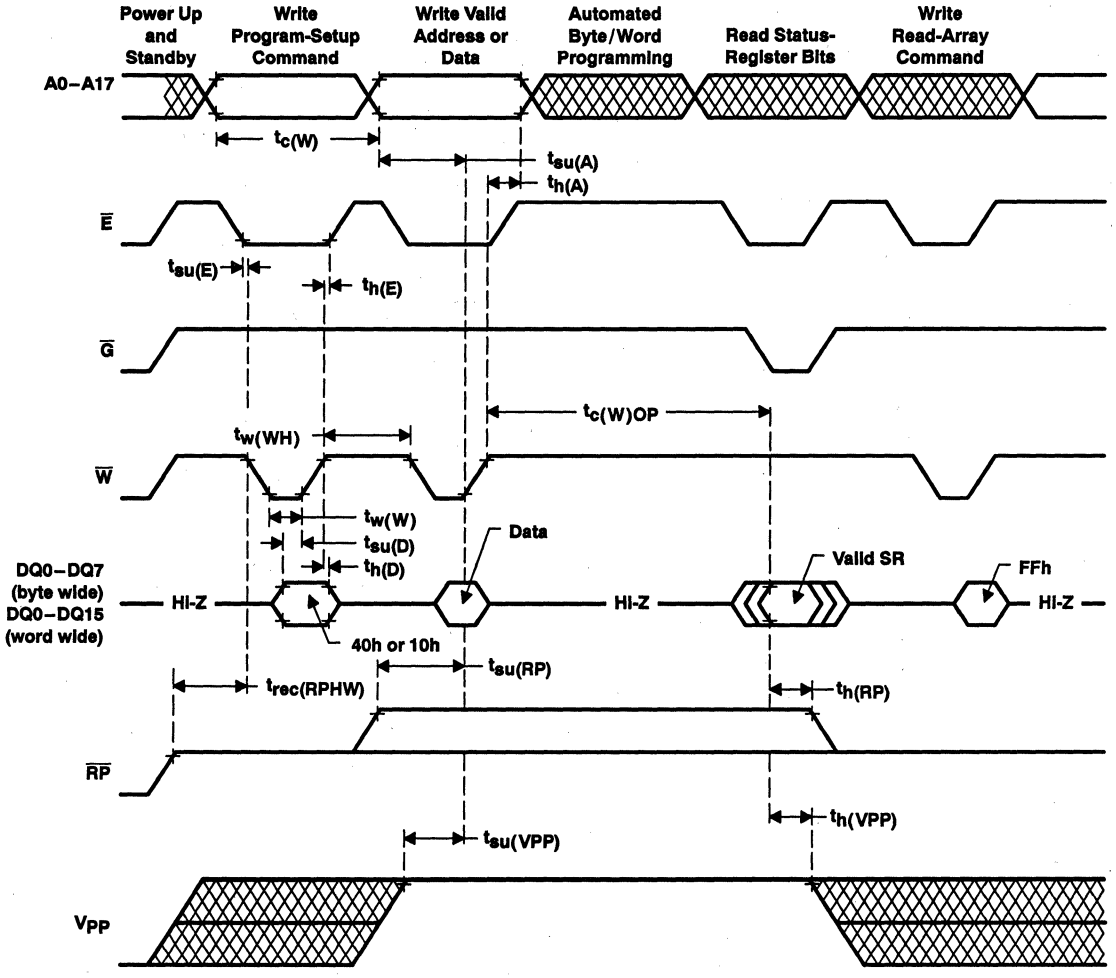


Figure 8. Write-Cycle Timing ($\overline{W}$-Controlled Write)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

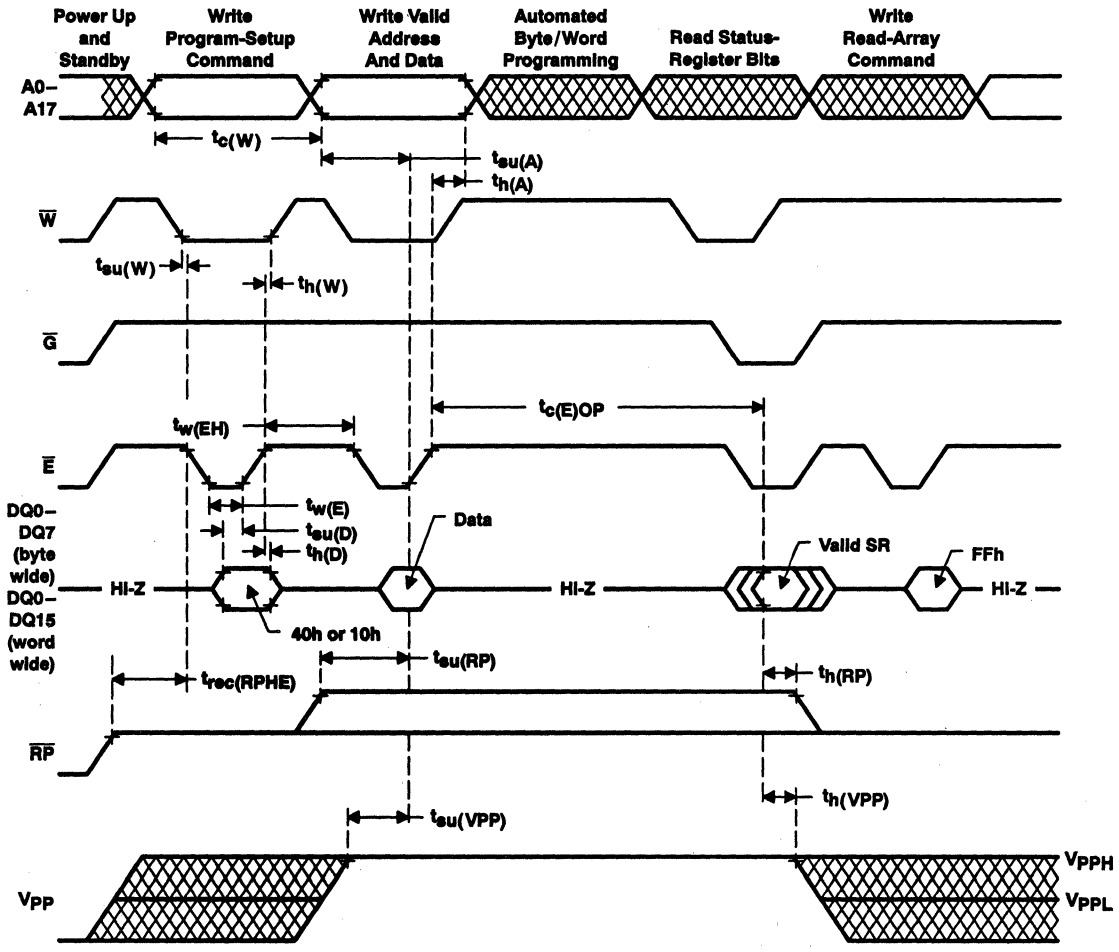


Figure 9. Write-Cycle Timing (Ē-Controlled Write)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

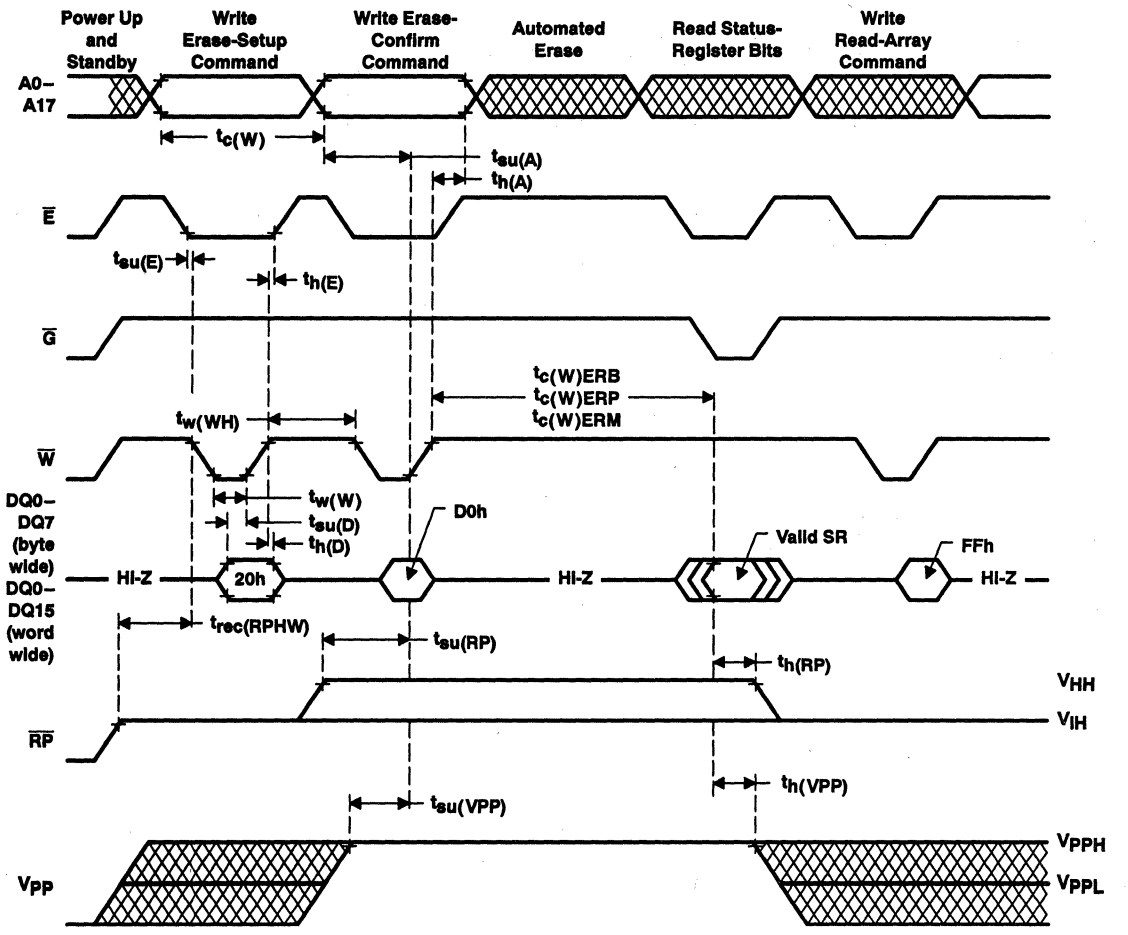


Figure 10. Erase-Cycle Timing ($\overline{W}$-Controlled Write)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

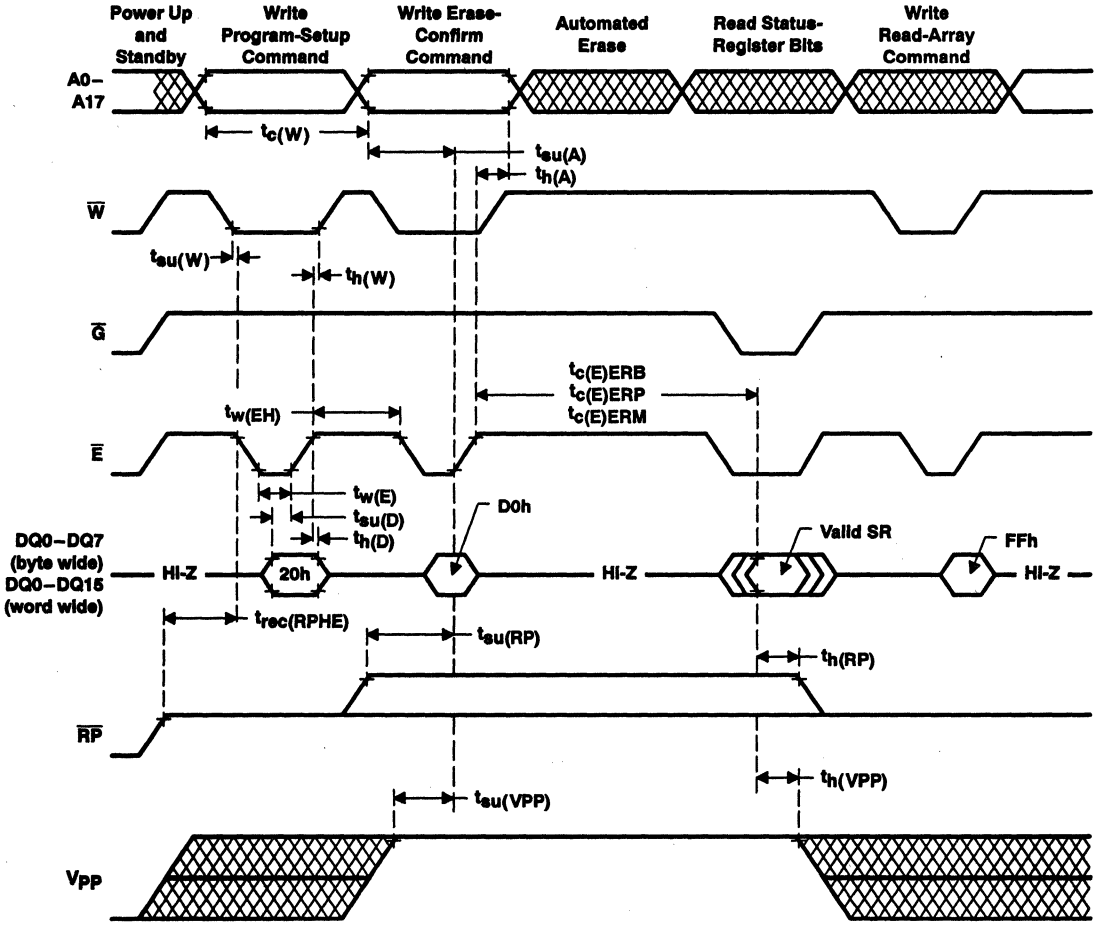


Figure 11. Erase-Cycle Timing ($\overline{E}$-Controlled Write)

ADVANCE INFORMATION

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

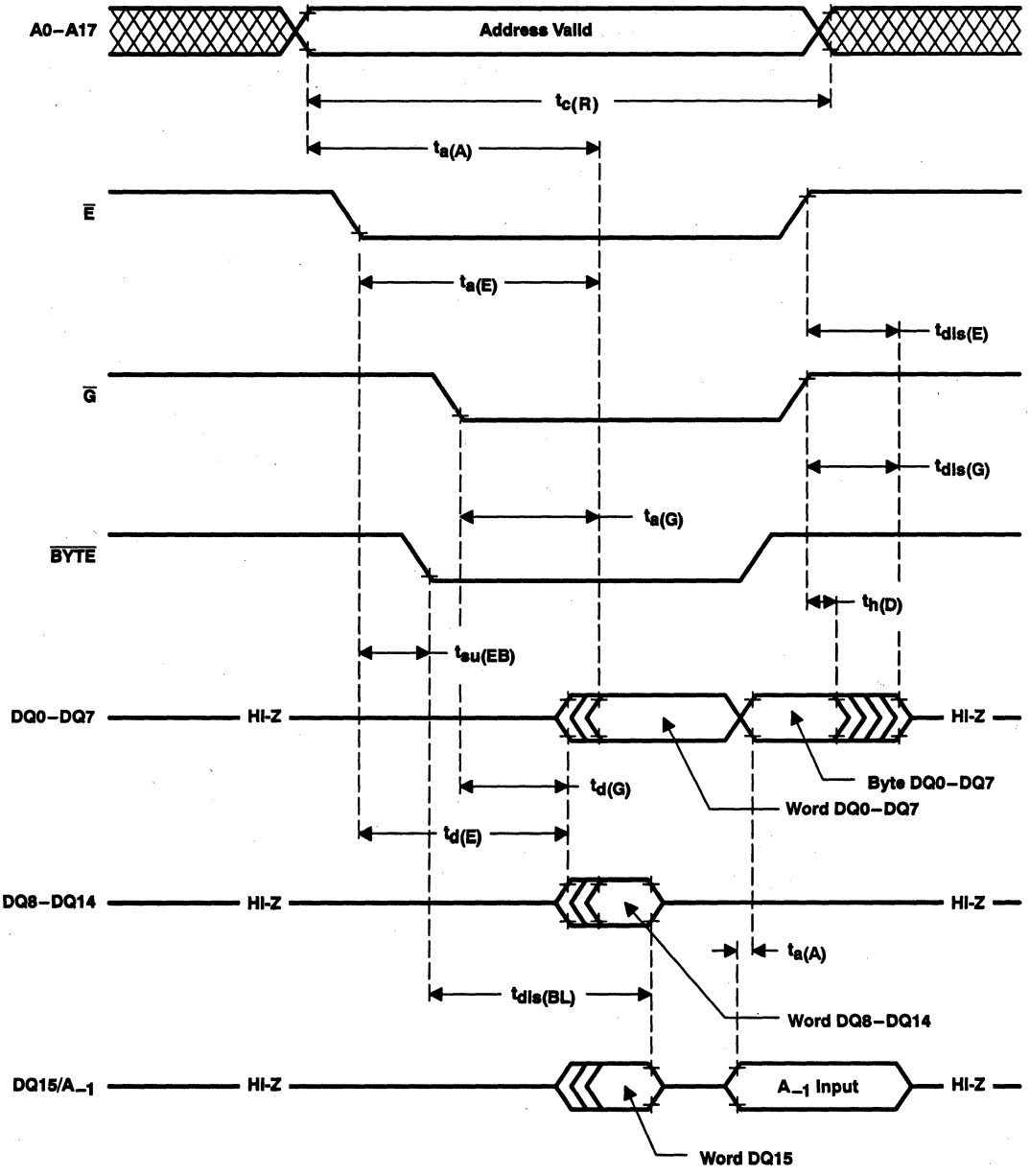


Figure 12. $\overline{BYTE}$ Timing, Changing From Word-Wide to Byte-Wide Mode

PARAMETER MEASUREMENT INFORMATION

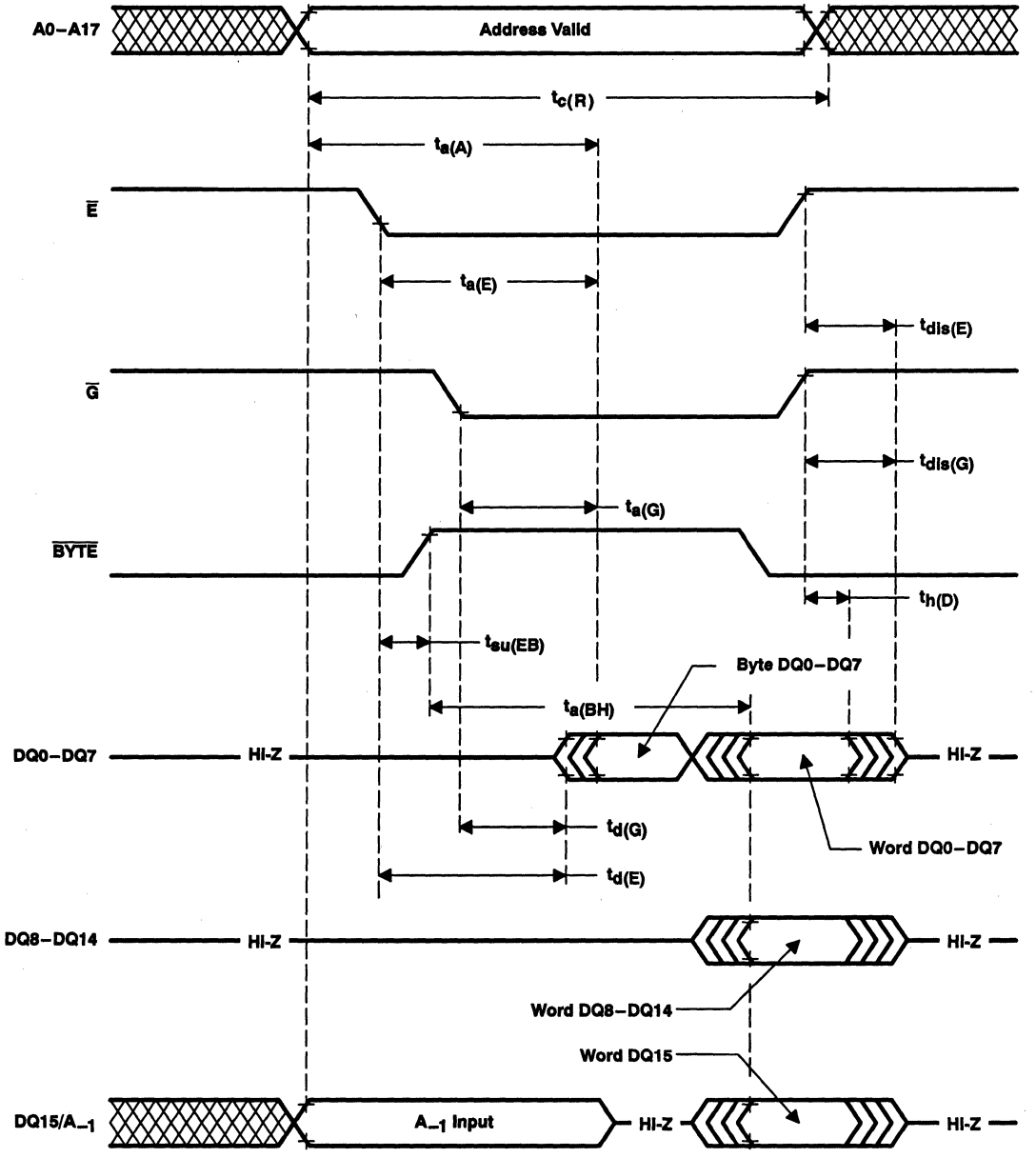


Figure 13. $\overline{BYTE}$ Timing, Changing From Byte-Wide to Word-Wide Mode

ADVANCE INFORMATION

This Data Sheet is Applicable to All TMS27C256s and TMS27PC256s Symbolized With Code "B" as Described on Page 157.

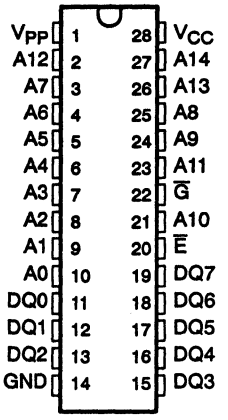
- **Organization . . . 32K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 256K MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

  V_{CC} ± 10%

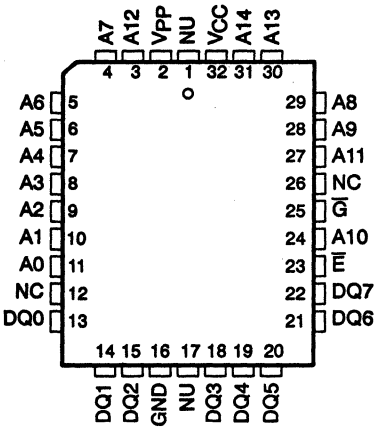
'27C/PC256-10	100 ns
'27C/PC256-12	120 ns
'27C/PC256-15	150 ns
'27C/PC256-17	170 ns
'27C/PC256-20	200 ns
'27C/PC256-25	250 ns

- **Power Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 165 mW Worst Case**
  - **Standby . . . 1.4 mW Worst Case (CMOS Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-In, and Choices of Operating Temperature Ranges**
- **256K EPROM Available With MIL-STD-883C Class B High Reliability Processing (SMJ27C256)**

J AND N PACKAGES
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

The TMS27C256 series are 262144-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC256 series are 262144-bit, one-time electrically programmable read-only memories.

PIN NOMENCLATURE	
A0–A14	Address Inputs
DQ0–DQ7	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable/Powerdown
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
NU	Make No External Connection
V_{CC}	5-V Power Supply
V_{PP}	13-V Power Supply

description (continued)

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C256 and the TMS27PC256 are pin compatible with 28-pin 256K MOS ROMs, PROMs, and EPROMs.

The TMS27C256 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers. The TMS27PC256 OTP PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers. The TMS27PC256 OTP PROM is also supplied in a 32-lead plastic leaded chip-carrier package using 1,25-mm (50-mil) lead spacing (FM suffix).

The TMS27C256 and TMS27PC256 are offered with two choices of temperature ranges of 0°C to 70°C (JL, NL, and FML suffixes) and – 40°C to 85°C (JE, NE, and FME suffixes). The TMS27C256 and the TMS27PC256 are also offered with 168-hour burn-in on both temperature ranges (JL4, FML4, JE4, and FME4 suffixes); see table below.

All package styles conform to JEDEC standards.

EPROM AND OTP PROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168-HR. BURN-IN VS TEMPERATURE RANGES	
	0°C TO 70°C	– 40°C TO 85°C	0°C TO 70°C	– 40°C TO 85°C
TMS27C256-XXX	JL	JE	JL4	JE4
TMS27PC256-XXX	NL	NE	NL4	NE4
TMS27PC256-XXX	FML	FME	FML4	FME4

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 13-V supply is needed for programming . All programming signals are TTL level. These devices are programmable by the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations can be programmed singly, in blocks, or at random.

operation

The seven modes of operation are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse), and 12 V on A9 for the signature mode.

FUNCTION	MODE†							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X	V_{IL}	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7	Data Out	Hi-Z	Hi-Z	Data In	Data Out	Hi-Z	CODE	
							MFG	DEVICE
							97	04

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C256s or TMS27PC256s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ0 through DQ7.

latchup immunity

Latchup immunity on the TMS27C256 and TMS27PC256 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL or CMOS signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C256)

Before programming, the TMS27C256 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are in the logic high state. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity × exposure time) is 15-W•s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C256, the window should be covered with an opaque label.

initializing (TMS27PC256)

The one-time programmable TMS27PC256 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The 256K EPROM and OTP PROM are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which programs in a nominal time of four seconds. Actual programming time varies as a function of the programmer used.

Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{G} = V_{IH}$, and $\overline{E} = V_{IL}$. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP}$ = 5 V.

program inhibit

Programming can be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits can be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$ and $\overline{E} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code, which is output on DQ0–DQ7; A0 = V_{IH} accesses the device code, which is output on DQ0–DQ7. All other addresses must be held at V_{IL}. The manufacturer code for these devices is 97, and the device code is 04.

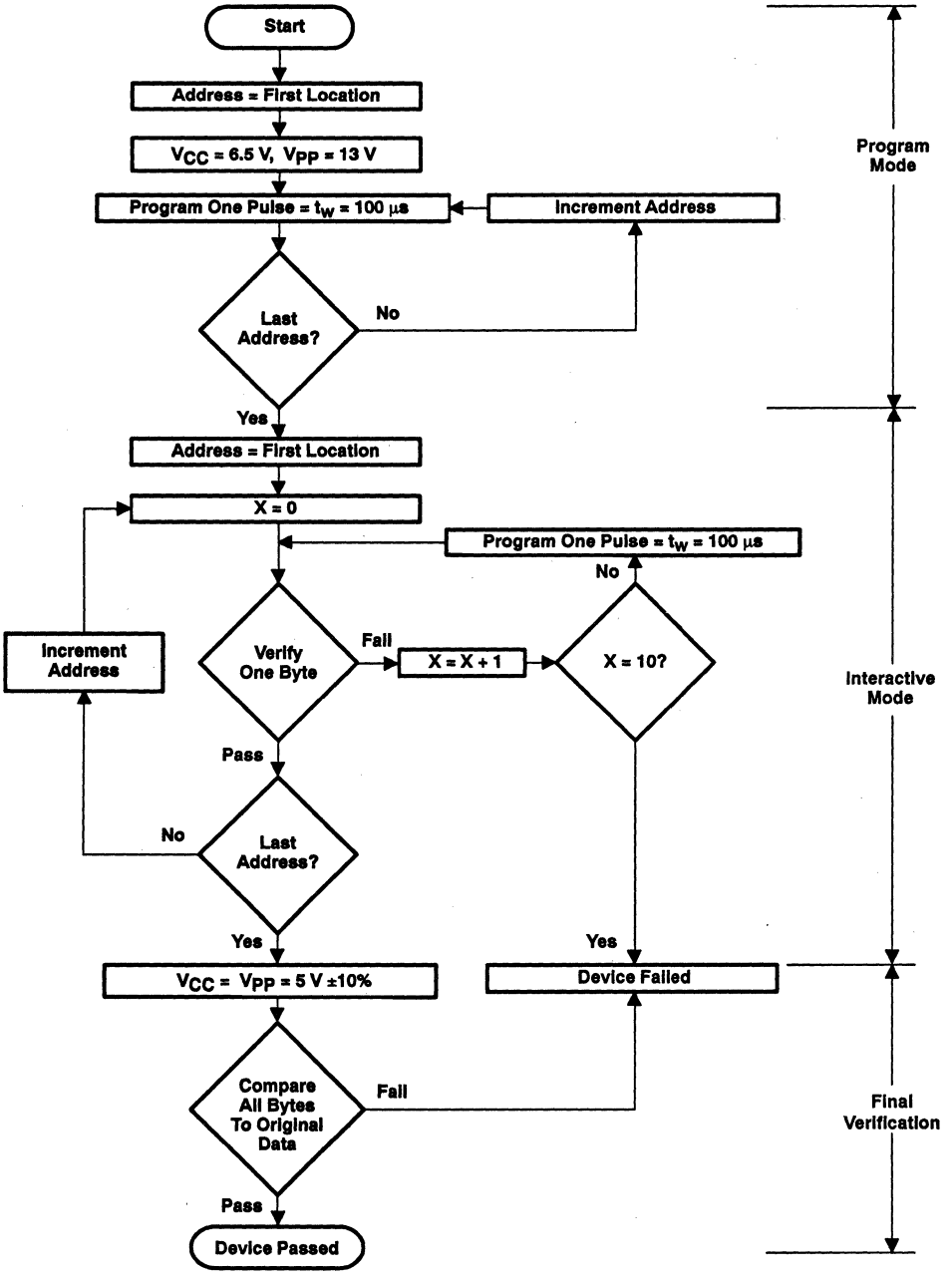
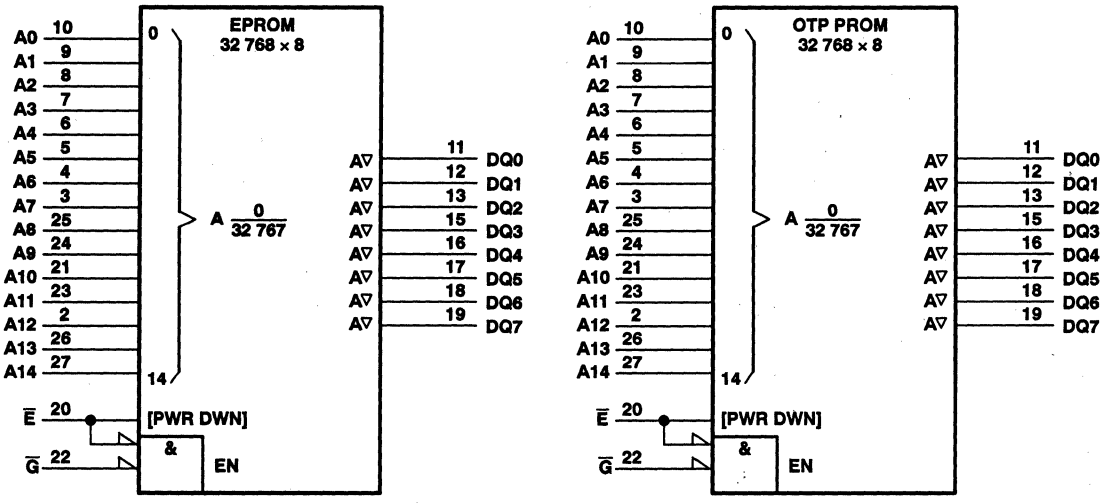


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C256-_ _JL and JL4, '27PC256-_ _NL, NL4, FML, and FML4) ..... 0° C to 70°C
Operating free-air temperature range ('27C256-_ _JE and JE4, '27PC256-_ _NE, NE4, FME, and FME4) ..... − 40° C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode	$V_{CC}-0.6$		$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	
V_{IH}	High-level dc input voltage	TTL	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	
V_{IL}	Low-level dc input voltage	TTL	−0.5		0.8	V
		CMOS	−0.5		0.2	
T_A	Operating free-air temperature	'27C256-_ _JL, JL4 '27PC256-_ _NL, NL4, FML, FML4	0		70	°C
T_A	Operating free-air temperature	'27C256-_ _JE, JE4 '27PC256-_ _NE, NE4, FME, FME4	−40		85	°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over recommended ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level dc output voltage		$I_{OH}=-2.5$ mA	3.5			V
			$I_{OH}=-20$ µA	$V_{CC}-0.1$			
V_{OL}	Low-level dc output voltage		$I_{OL}=2.1$ mA			0.4	V
			$I_{OL}=20$ µA			0.1	
I_I	Input current (leakage)		$V_I=0$ V to 5.5 V			±1	µA
I_O	Output current (leakage)		$V_O=0$ V to V_{CC}			±1	µA
I_{PP1}	V_{PP} supply current		$V_{PP}=V_{CC}=5.5$ V		1	10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP}=13$ V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC}=5.5$ V, $\overline{E}=V_{IH}$		250	500	µA
		CMOS-input level	$V_{CC}=5.5$ V, $\overline{E}=V_{CC}$		100	250	
I_{CC2}	V_{CC} supply current (active)		$V_{CC}=5.5$ V, $\overline{E}=V_{IL}$, t_{cycle} = minimum cycle time, outputs open		15	30	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	$V_I=0$, f = 1 MHz		6	10	pF
C_o	Output capacitance	$V_O=0$, f = 1 MHz		10	14	pF

† Typical values are at T_A = 25°C and nominal voltages.
‡ Capacitance measurements are made on a sample basis only.

switching characteristics over recommended range of operating conditions

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C256-10 '27PC256-10		'27C256-12 '27PC256-12		'27C256-15 '27PC256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		55		75	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	45	0	45	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C256-17 '27PC256-17		'27C256-20 '27PC256-20		'27C256-25 '27PC256-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		170		200		250	ns
$t_{a(E)}$	Access time from chip enable			170		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6.50 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0	130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		150	ns

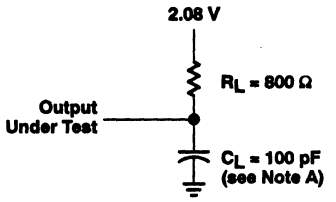
NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low). (Reference page 9.)
4. Common test conditions apply for the t_{dis} except during programming.

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V, T_A = 25°C (see Note 3)

		MIN	NOM	MAX	UNIT
$t_{h(A)}$	Hold time, address	0			µs
$t_{h(D)}$	Hold time, data	2			µs
$t_{w(IPGM)}$	Pulse duration, initial program	95	100	105	µs
$t_{su(A)}$	Setup time, address	2			µs
$t_{su(G)}$	Setup time, $\overline{G}$	2			µs
$t_{su(E)}$	Setup time, $\overline{E}$	2			µs
$t_{su(D)}$	Setup time, data	2			µs
$t_{su(VPP)}$	Setup time, V_{PP}	2			µs
$t_{su(VCC)}$	Setup time, V_{CC}	2			µs

NOTE 3: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low). (Reference page 9.)

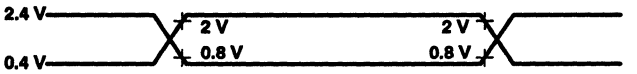
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

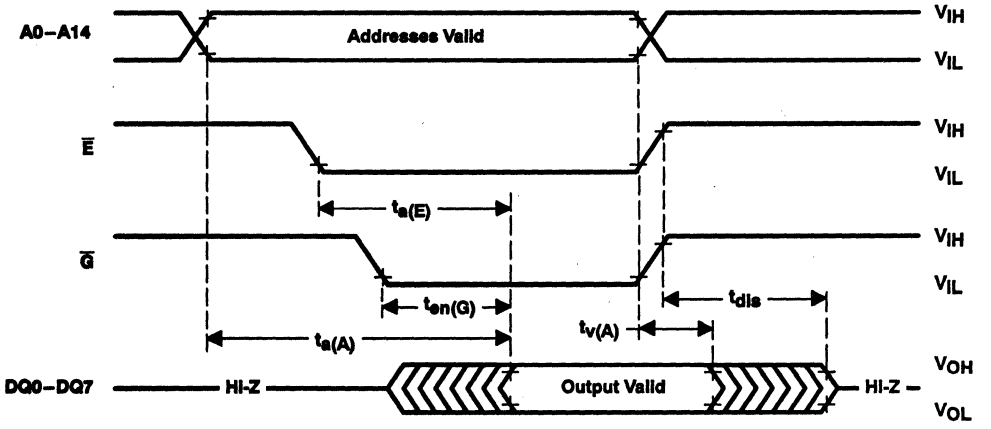
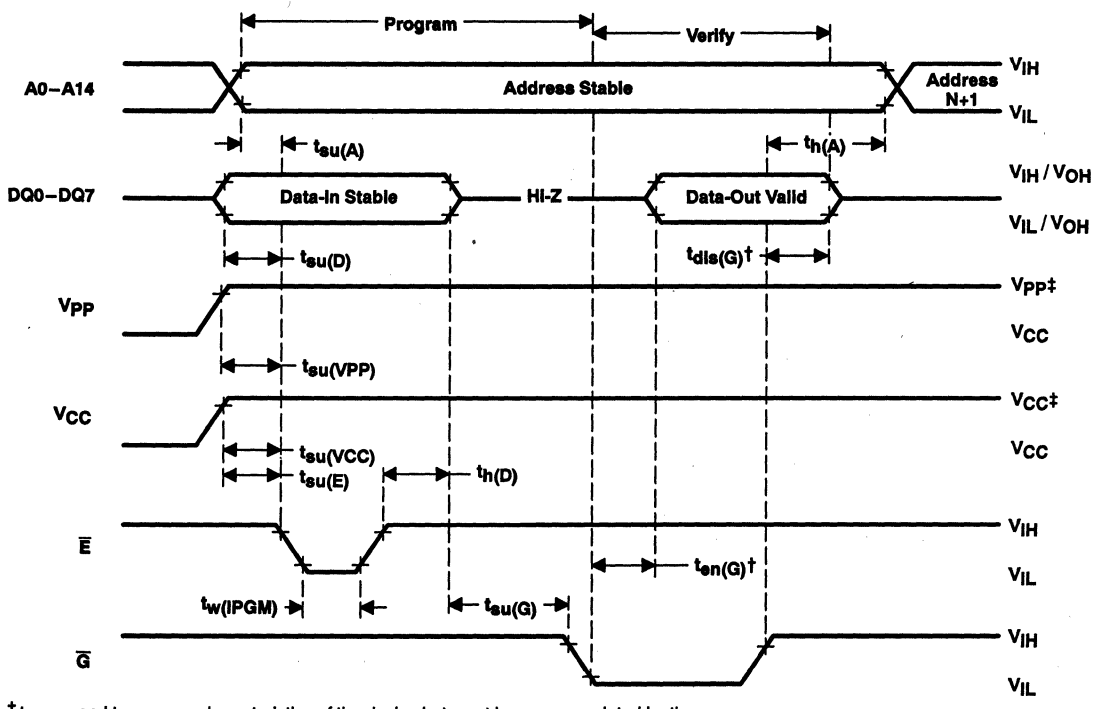


Figure 3. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

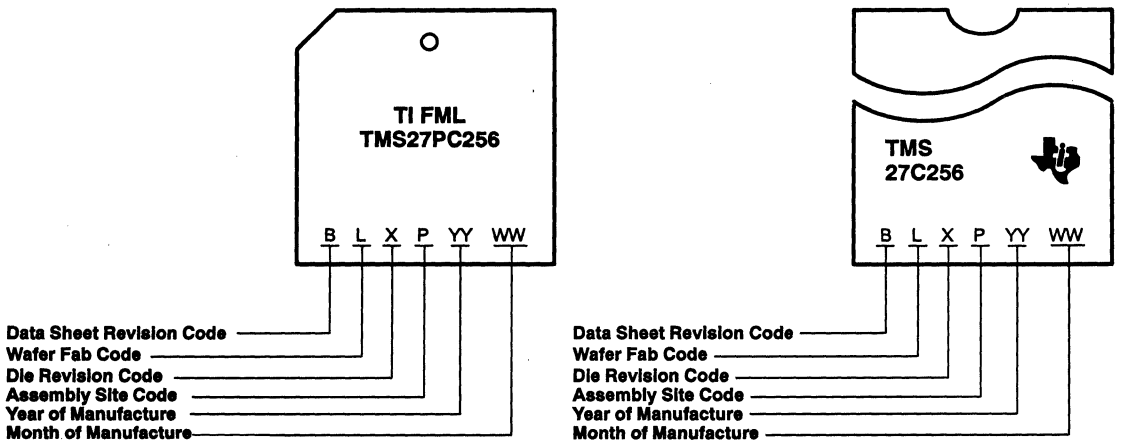


† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming

Figure 4. Program-Cycle Timing (SNAP! Pulse Programming)

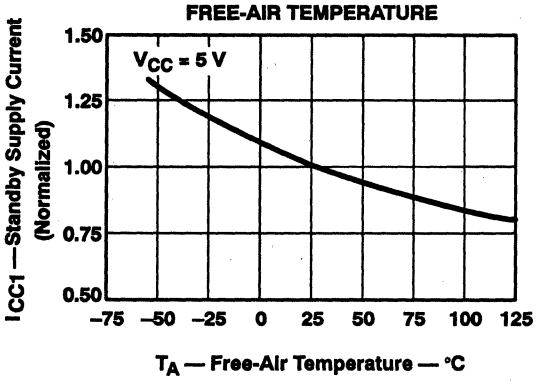
device symbolization

This data sheet is applicable to all TI TMS27C256 CMOS EPROMs and TMS27PC256 CMOS OTP PROMs with the data sheet revision code "B" as shown below.

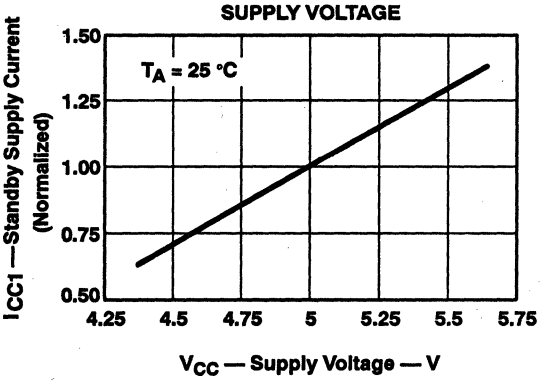


TYPICAL TMS27C/PC256 CHARACTERISTICS

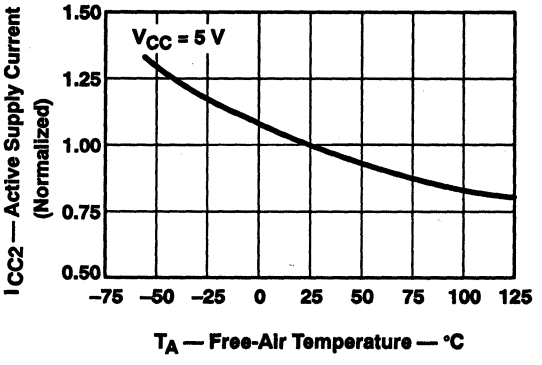
STANDBY SUPPLY CURRENT vs FREE-AIR TEMPERATURE



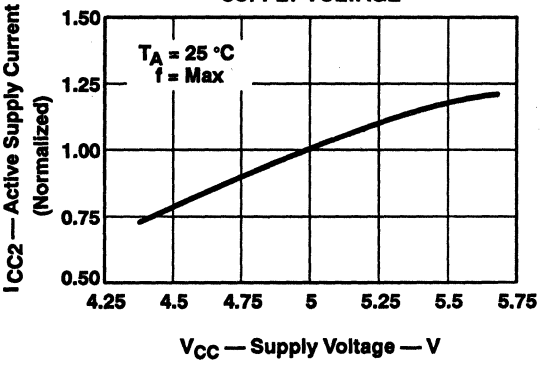
STANDBY SUPPLY CURRENT vs SUPPLY VOLTAGE



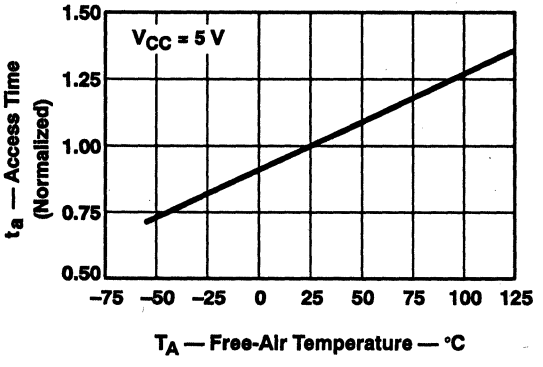
ACTIVE SUPPLY CURRENT vs FREE-AIR TEMPERATURE



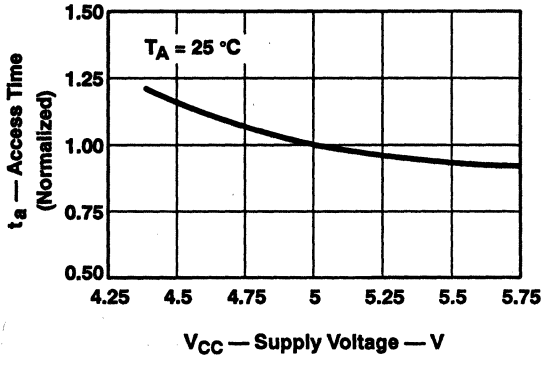
ACTIVE SUPPLY CURRENT vs SUPPLY VOLTAGE



ACCESS TIME vs FREE-AIR TEMPERATURE



ACCESS TIME vs SUPPLY VOLTAGE



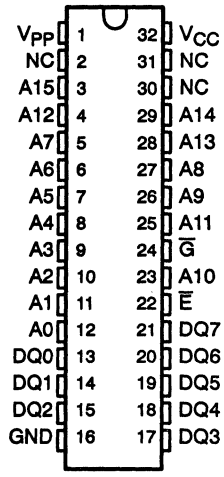
- **Organization . . . 64K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 1 Meg MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access / Min Cycle Times**

  V_{CC} ± 10%

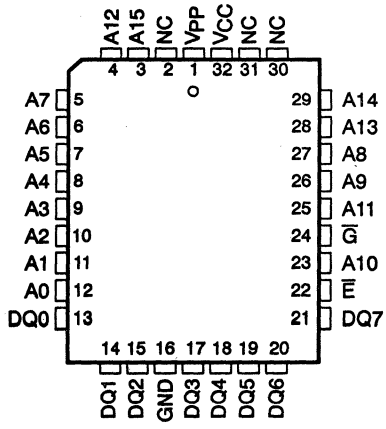
'27C510-12	120 ns
'27C/PC510-15	150 ns
'27C/PC510-17	170 ns
'27C/PC510-20	200 ns
'27C/PC510-25	250 ns

- **Power Saving CMOS Technology**
- **Very High Speed SNAP! Pulse Programming**
- **3-State Output Buffers**
- **400 mV Guaranteed DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 165 mW Worst Case**
  - **Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-In, and Choices of Operating Temperature Range**
- **512K EPROM Available With MIL-STD-883C Class B High Reliability Processing (SMJ27C510)**

J AND N PACKAGES
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A15	Address Inputs
$\overline{E}$	Chip Enable
DQ0–DQ7	Inputs (programming)/Outputs
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
V_{CC}	5-V Power Supply
V_{PP}	12-13 V Power Supply

description

The TMS27C510 series are 524288-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC510 series are 524288-bit, one-time electrically programmable read-only memories.

These devices are fabricated using power saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

description (continued)

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C510 and the TMS27PC510 are pin compatible with 32-pin 1-megabit MOS ROMs, PROMs, and EPROMs.

The TMS27C510 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers. The TMS27C510 is available with two choices of temperature ranges of 0°C to 70°C (JL suffix) and – 40°C to 85°C (JE suffix). The TMS27C510 is also offered with 168-hour burn-in on both temperature ranges (JL4 and JE4 suffixes). (See table below.)

The TMS27PC510 PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers. The TMS27PC510 is also supplied in a 32-lead plastic leaded chip-carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). The TMS27PC510 is specified for operation from 0°C to 70°C, and – 40°C to 85°C.

All package styles conform to JEDEC standards.

EPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168-HR. BURN-IN VS TEMPERATURE RANGES	
	0°C TO 70°C	– 40°C TO 85°C	0°C TO 70°C	– 40°C TO 85°C
TMS27C510-XXX	JL	JE	JL4	JE4
TMS27PC510-XXX	NL, FML	NE, FME	—	NE4, FME4

These EPROMs and PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other (13-V) supply is needed for programming. All programming signals are TTL level. These devices are programmable by a SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13.0 V and a V_{CC} of 6.5 V for a nominal programming time of seven seconds. For programming outside the system, existing EPROM programers can be used. Locations can be programmed singly, in blocks, or at random.

operation

The seven modes of operation are in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13.0 V for SNAP! Pulse), and 12 V on A9 for the signature mode.

FUNCTION	MODE†							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X	V_{IL}	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7	Data Out	Hi-Z	Hi-Z	Data In	Data Out	Hi-Z	CODE	
							MFG	DEVICE
							97	15

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C510s or TMS27PC510s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ0 to DQ7.

latchup immunity

Latchup immunity on the TMS27C510 and TMS27PC510 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

powerdown

Active I_{CC} current can be reduced from 30 mA to 500 μA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C510)

Before programming, the TMS27C510 EPROM is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C510, the window should be covered with an opaque label. After erasure (all bits in logic 1 state), logic 0s are programmed into the desired locations. A programmed zero can be erased only by ultraviolet light.

initializing (TMS27PC510)

The one-time programmable TMS27PC510 PROM is provided with all bits in logic 1 state, then logic 0s are programmed into the desired locations. Logic 0s programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 512K EPROM and PROM can be programmed using the TI SNAP! Pulse programming algorithm as illustrated by the flowchart in Figure 1, which can reduce programming time to a nominal 7 seconds. Actual programming time varies as a function of the programmer used.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13.0 V, V_{CC} = 6.5 V, $\overline{G} = V_{IH}$, and $\overline{E} = V_{IL}$. Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable, $\overline{E}$ is pulsed.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP}$ = 5 V.

program inhibit

Programming can be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits can be verified with V_{PP} = 13.0 V when $\overline{G} = V_{IL}$ and $\overline{E} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code which is output on DQ0–DQ7; A0 = V_{IH} accesses the device code which is output on DQ0–DQ7. All other addresses must be held at V_{IL}. The manufacturer code for these devices is 97, and the device code is 15.

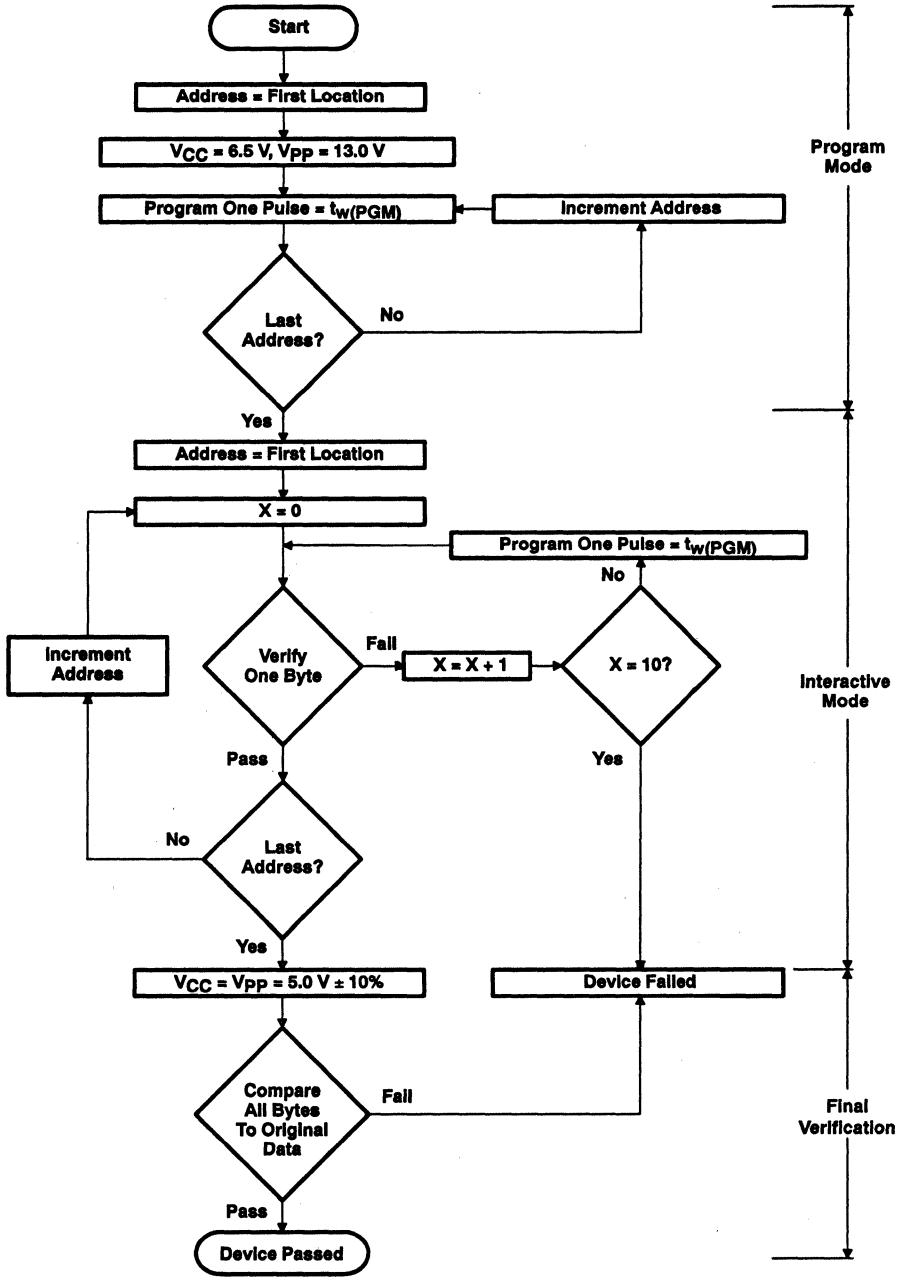
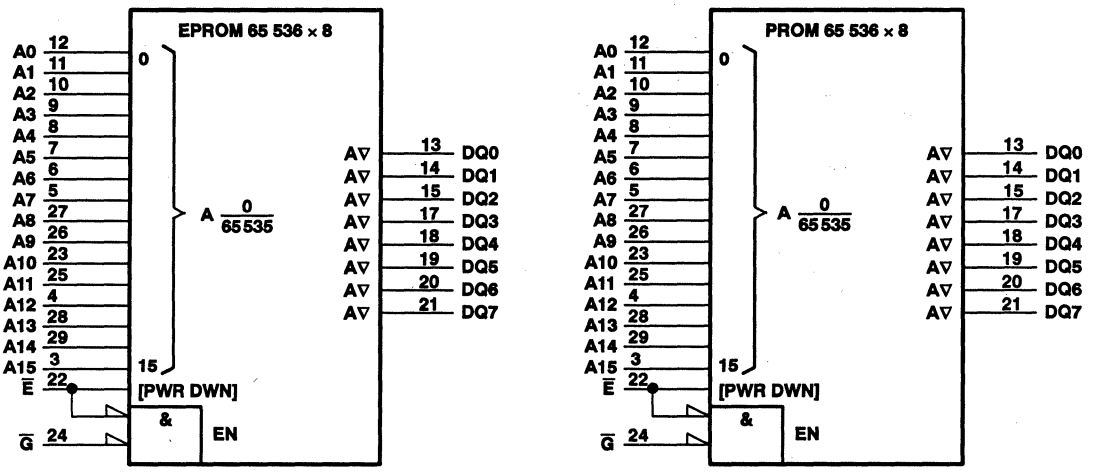


Figure 1. SNAP! Pulse Programming Flowchart

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
J and N packages illustrated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... –0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... –0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... –0.6 V to 6.5 V
A9 ..... –0.6 V to 13.5 V
Output voltage range (see Note 1) ..... –0.6 V to V_{CC} + 1 V

Operating free-air temperature range ('27C510-__JL and JL4;
'27PC510-__NL, FML, NE, and FME) ..... 0°C to 70°C
Operating free-air temperature range ('27C510-__JE, JE4, NE4, and FME4) ..... –40°C to 85°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode		$V_{CC}-0.6$		$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	
V_{IH}	High-level dc input voltage		TTL	2		$V_{CC}+1$	V
			CMOS	$V_{CC}-0.2$		$V_{CC}+1$	
V_{IL}	Low-level dc input voltage		TTL	−0.5		0.8	V
			CMOS	−0.5		0.2	
T_A	Operating free-air temperature			(see Table, page 2)			°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH}=-2.5$ mA	3.5			V
			$I_{OH}=-20$ µA	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL}=2.1$ mA			0.4	V
			$I_{OL}=20$ µA			0.1	
I_I	Input current (leakage)		$V_I=0$ V to 5.5 V			±1	µA
I_O	Output current (leakage)		$V_O=0$ V to V_{CC}			±1	µA
I_{PP1}	V_{PP} supply current		$V_{PP}=V_{CC}=5.5$ V		1	10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP}=13$ V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC}=5.5$ V, ... $\overline{E}=V_{IH}$		250	500	µA
		CMOS-input level	$V_{CC}=5.5$ V, $\overline{E}=V_{CC}$		100	250	
I_{CC2}	V_{CC} supply current (active)		$V_{CC}=5.5$ V, $\overline{E}=V_{IL}$, t_{cycle} = minimum cycle time, outputs open		15	30	mA

† Typical values are at $T_A=25°C$ and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	$V_I=0$ V, f = 1 MHz		6	10	pF
C_o	Output capacitance	$V_O=0$ V, f = 1 MHz		10	14	pF

† Typical values are at $T_A=25°C$ and nominal voltages.
‡ Capacitance measurements are made on sample basis only.

switching characteristics over recommended ranges of operating conditions

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C510-12 '27PC510-12		'27C510-15 '27PC510-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		120		150	ns
$t_{a(E)}$	Access time from chip enable			120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		75	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	45	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C510-17 '27PC510-17		'27C510-20 '27PC510-20		'27C510-25 '27PC510-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		170		200		250	ns
$t_{a(E)}$	Access time from chip enable			170		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 3)

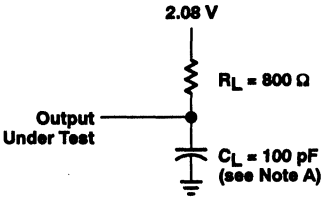
PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0	130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		150	ns

recommended timing requirements for programming, V_{CC} = 6.5 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 3)

			MIN	NOM	MAX	UNIT
$t_{w(PGM)}$	Pulse duration, program	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Setup time, address		2			µs
$t_{su(G)}$	Setup time, $\overline{G}$		2			µs
$t_{su(E)}$	Setup time, $\overline{E}$		2			µs
$t_{su(D)}$	Setup time, data		2			µs
$t_{su(VPP)}$	Setup time, V_{PP}		2			µs
$t_{su(VCC)}$	Setup time, V_{CC}		2			µs
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs

NOTES: 3. For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic 1 and 0.8 V for logic 0. (Reference page 9.)
4. Common test conditions apply for the t_{dis} except during programming.

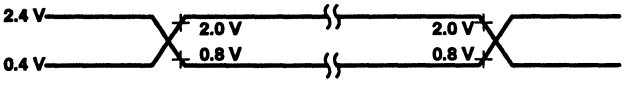
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

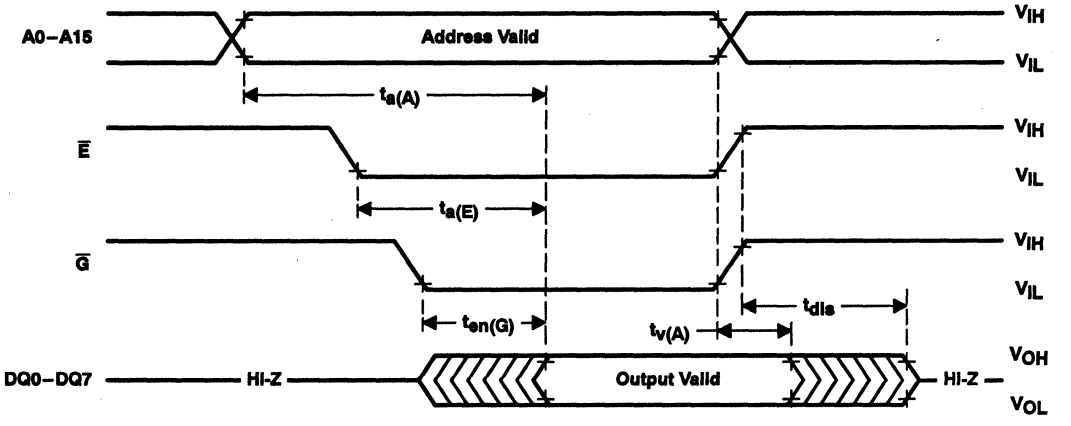
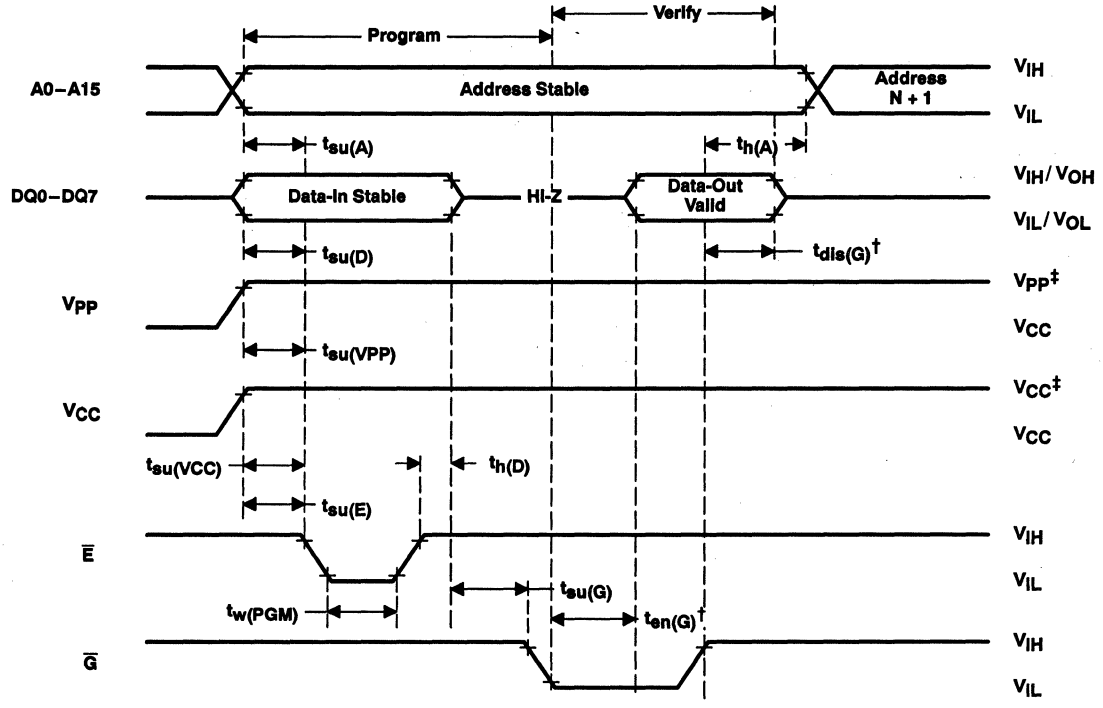


Figure 3. Read-Cycle Timing

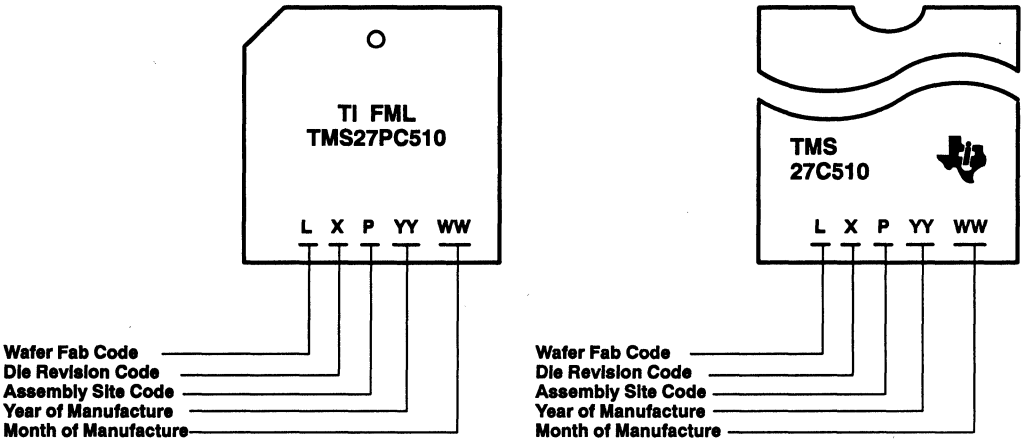
PARAMETER MEASUREMENT INFORMATION



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13.0-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming

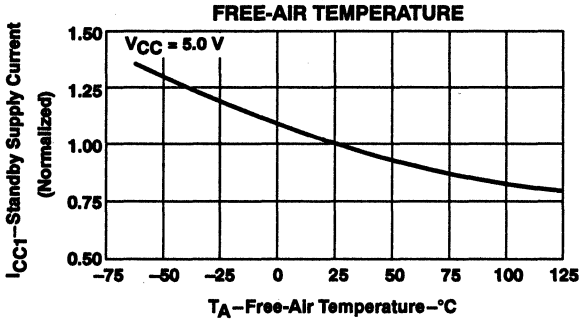
Figure 4. Program-Cycle Timing

device symbolization

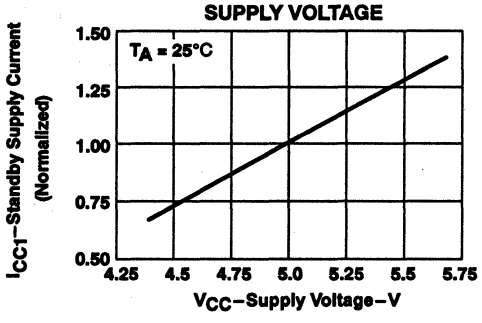


TYPICAL TMS27C/P0C510 CHARACTERISTICS

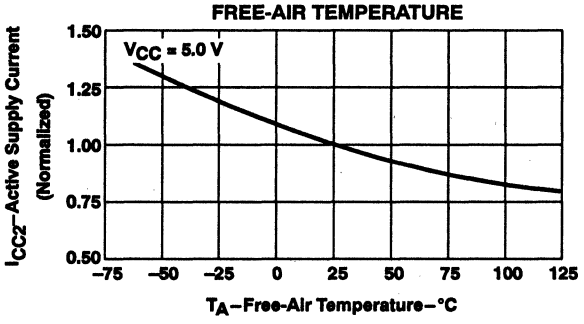
STANDBY SUPPLY CURRENT vs FREE-AIR TEMPERATURE



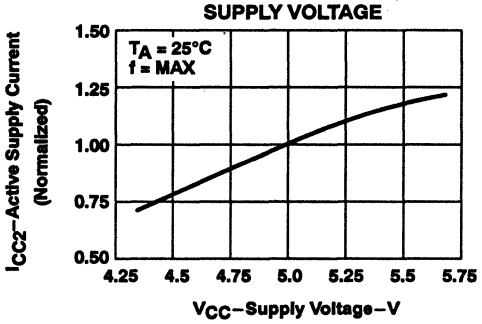
STANDBY SUPPLY CURRENT vs SUPPLY VOLTAGE



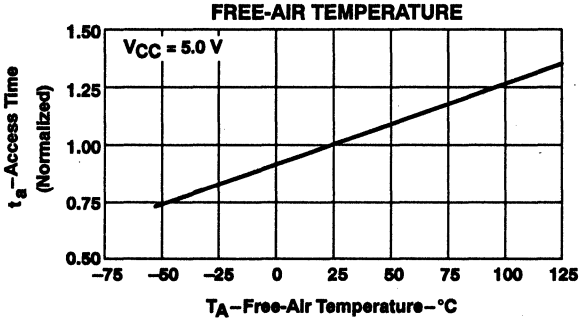
ACTIVE SUPPLY CURRENT vs FREE-AIR TEMPERATURE



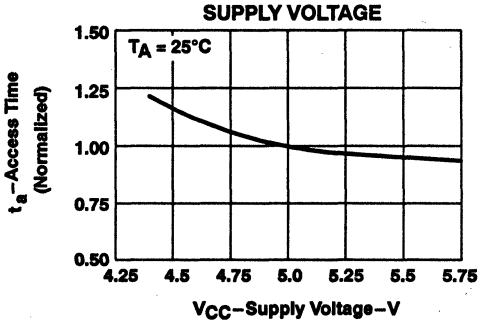
ACTIVE SUPPLY CURRENT vs SUPPLY VOLTAGE



ACCESS TIME vs FREE-AIR TEMPERATURE



ACCESS TIME vs SUPPLY VOLTAGE



This Data Sheet is Applicable to All TMS27C512s and TMS27PC512s Symbolized with Code "B" as Described on Page 182.

- **Organization . . . 64K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 512K MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

  V_{CC} ± 10%

'27C/PC512-10	100 ns
'27C/PC512-12	120 ns
'27C/PC512-15	150 ns
'27C/PC512-20	200 ns
'27C/PC512-25	250 ns

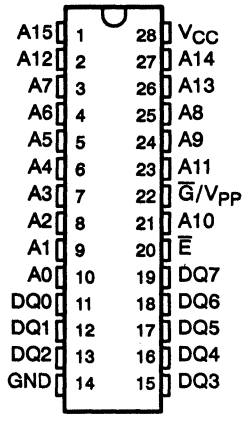
- **Power Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.25 V)**
  - **Active . . . 158 mW Worst Case**
  - **Standby . . . 1.4 mW Worst Case (CMOS Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-In, and Choices of Operating Temperature Ranges**
- **512K EPROM Available With MIL-STD-883C Class B High Reliability Processing (SMJ27C512)**

description

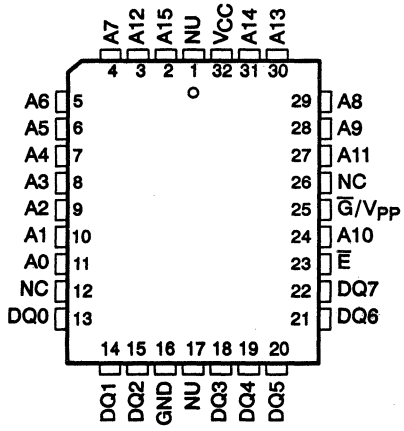
The TMS27C512 series are 524288-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC512 series are 524288-bit, one-time electrically programmable read-only memories.

J AND N PACKAGES
(TOP VIEW)

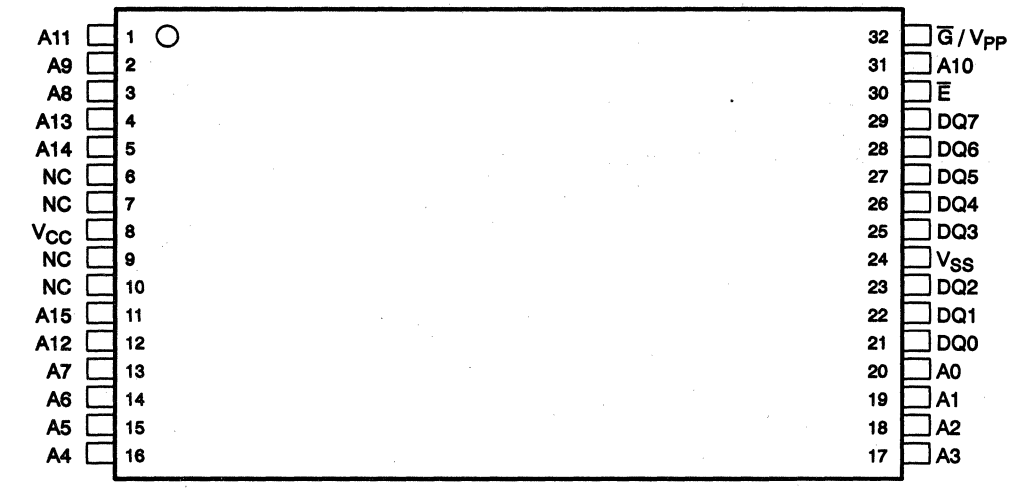


FM PACKAGE
(TOP VIEW)

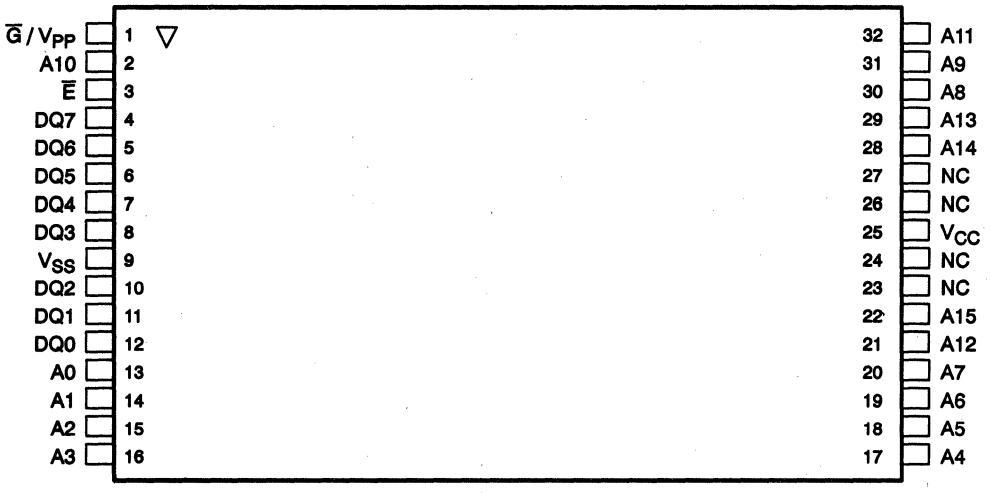


PIN NOMENCLATURE	
A0–A15	Address Inputs
$\overline{E}$	Chip Enable/Powerdown
DQ0–DQ7	Inputs (programming) / Outputs
$\overline{G}/V_{PP}$	13-V Programming Power Supply
GND	Ground
NC	No Internal Connection
NU	Make No External Connection
V_{CC}	5-V Power Supply

TMS27PC512
DD PACKAGE
(TOP VIEW)



TMS27PC512
DU PACKAGE
REVERSE PINOUT
(TOP VIEW)



description (continued)

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C512 and the TMS27PC512 are pin compatible with 28-pin 512K MOS ROMs, PROMs, and EPROMs.

The TMS27C512 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC512 OTP PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC512 OTP PROM is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix), and in a 32-lead thin small-outline package (DD and DU suffixes).

The TMS27C512 and TMS27PC512 are offered with two choices of temperature ranges of 0°C to 70°C (JL, NL, FML, and DDL suffixes) and – 40°C to 85°C (JE, NE, FME, and DDE suffixes). The TMS27C512 and TMS27PC512 are also offered with a 168-hour burn-in on both temperature ranges (JL4, NL4, FML4, DDL4, JE4, NE4, FME4, and DDE4 suffixes); see table below.

All package styles conform to JEDEC standards.

EPROM AND OTP PROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C TO 70°C	– 40°C TO 85°C	0°C TO 70°C	– 40°C TO 85°C
TMS27C512-xxx	JL	JE	JL4	JE4
TMS27PC512-xxx	NL	NE	NL4	NE4
TMS27PC512-xxx	FML	FME	FML4	FME4
TMS27PC512-xxx	DDL	DDE	DDL4	DDE4
TMS27PC512-xxx	DUL	DUE	DUL4	DUE4

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 13-V supply is needed for programming. All programming signals are TTL level. The device is programmed using the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of seven seconds. For programming outside the system, existing EPROM programmers can be used. Locations can be programmed singly, in blocks, or at random.

operation

The seven modes of operation are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION	MODE†							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}/V_{PP}$	V_{IL}	V_{IH}	X	V_{PP}	V_{IL}	V_{PP}	V_{IL}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7	Data Out	Hi-Z	Hi-Z	Data In	Data Out	Hi-Z	CODE	
							MFG	DEVICE
							97	85

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C512s or TMS27PC512s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}/V_{PP}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ0 through DQ7.

latchup immunity

Latchup immunity on the TMS27C512 and TMS27PC512 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL/CMOS signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C512)

Before programming, the TMS27C512 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 angstroms). EPROM erasure before programming is necessary to assure that all bits are in the logic high state. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C512, the window should be covered with an opaque label.

Initializing (TMS27PC512)

The one-time programmable TMS27PC512 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 512K EPROM and OTP PROM are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which programs in a nominal time of seven seconds. Actual programming time varies as a function of the programmer used.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved with $\overline{G}/V_{PP}$ = 13 V, V_{CC} = 6.5 V, and $\overline{E} = V_{IL}$. Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable, $\overline{E}$ is pulsed.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = 5 V, $\overline{G}/V_{PP} = V_{IL}$, and $\overline{E} = V_{IL}$.

program inhibit

Programming can be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits can be verified when $\overline{G}/V_{PP}$ and $\overline{E} = V_{IL}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code, which is output on DQ0–DQ7; A0 = V_{IH} accesses the device code, which is output on DQ0–DQ7. All other addresses must be held at V_{IL}. The manufacturer code for these devices is 97, and the device code is 85.

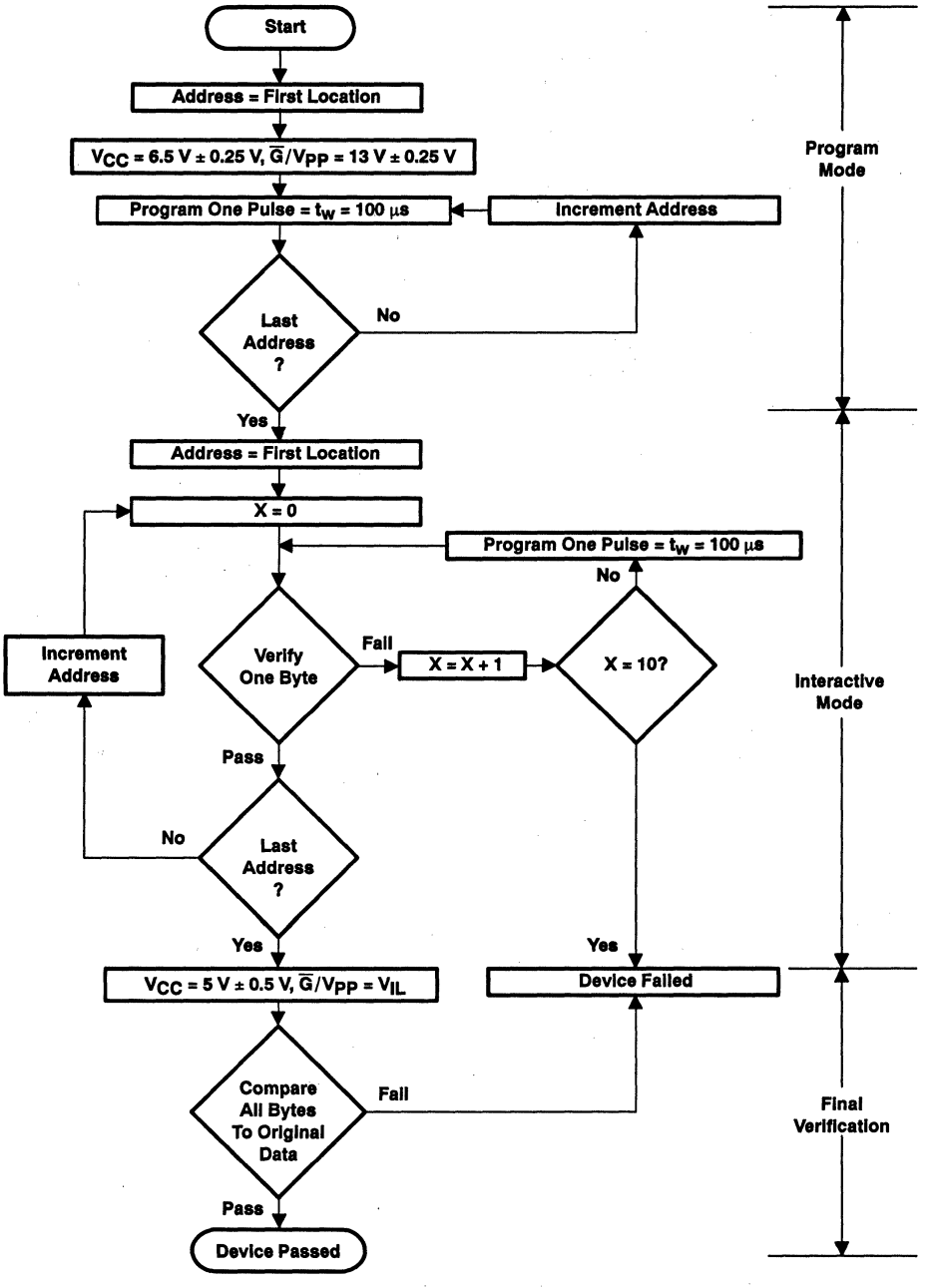
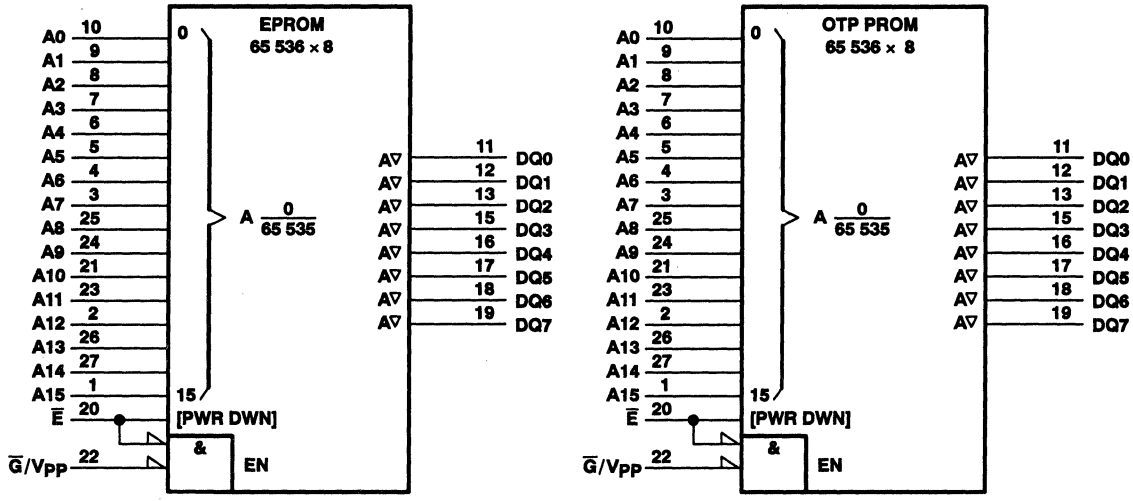


Figure 1. SNAP! Pulse Programming Flowchart

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C512-_ _JL and JL4, '27PC512-_ _NL and NL4,
FML and FML4, DDL and DDL4) ..... 0°C to 70°C
Operating free-air temperature range ('27C512-_ _JE and JE4, '27PC512-_ _NE and NE4,
FME and FME4, DDE and DDE4) ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	
$\overline{G}/V_{PP}$	Supply voltage	SNAP! Pulse programming algorithm	12.75	13	13.25	V
V_{IH}	High-level dc input voltage	TTL	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	
V_{IL}	Low-level dc input voltage	TTL	−0.5		0.8	V
		CMOS	−0.5		0.2	
T_A	Operating free-air temperature	TMS27C512-_ _JL, JL4 TMS27PC512-_ _NL, NL4, FML, FML4, DDL, DDL4	0		70	°C
T_A	Operating free-air temperature	TMS27C512-_ _JE, JE4 TMS27PC512-_ _NE, NE4, FME, FME4, DDE, DDE4	−40		85	°C

NOTE 2: V_{CC} must be applied before or at the same time as $\overline{G}/V_{PP}$ and removed after or at the same time as $\overline{G}/V_{PP}$. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level dc output voltage		I_{OH} = −2.5 mA	3.5			V
			I_{OH} = −20 µA	$V_{CC}-0.1$			
V_{OL}	Low-level dc output voltage		I_{OL} = 2.1 mA			0.4	V
			I_{OL} = 20 µA			0.1	
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±1	µA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±1	µA
I_{PP}	$\overline{G}/V_{PP}$ supply current (during program pulse)		$\overline{G}/V_{PP}$ = 13 V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, ... $\overline{E}$ = V_{IH}		250	500	µA
		CMOS-input level	V_{CC} = 5.5 V, ... $\overline{E}$ = V_{CC}		100	250	
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		15	30	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_I	Input capacitance	V_I = 0 V, f = 1 MHz		6	10	pF
C_O	Output capacitance	V_O = 0 V, f = 1 MHz		10	14	pF
$C_{G/VPP}$	$\overline{G}/V_{PP}$ input capacitance	$\overline{G}/V_{PP}$ = 0 V, f = 1 MHz		20	25	pF

† Typical values are at T_A = 25°C and nominal voltages.
‡ Capacitance measurements are made on a sample basis only.

switching characteristics over recommended ranges of operating conditions

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C512-10 '27PC512-10		'27C512-12 '27PC512-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		100		120	ns
$t_{a(E)}$	Access time from chip enable			100		120	ns
$t_{en(G)}$	Output enable time from $\overline{G}/V_{PP}$			55		55	ns
t_{dis}	Output disable time from $\overline{G}/V_{PP}$ or $\overline{E}$, whichever occurs first†		0	45	0	45	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}/V_{PP}$, whichever occurs first†		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C512-15 '27PC512-15		UNIT
			MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		150	ns
$t_{a(E)}$	Access time from chip enable			150	ns
$t_{en(G)}$	Output enable time from $\overline{G}/V_{PP}$			75	ns
t_{dis}	Output disable time from $\overline{G}/V_{PP}$ or $\overline{E}$, whichever occurs first†		0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}/V_{PP}$, whichever occurs first†		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C512-20 '27PC512-20		'27C512-25 '27PC512-25		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		200		250	ns
$t_{a(E)}$	Access time from chip enable			200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}/V_{PP}$			75		100	ns
t_{dis}	Output disable time from $\overline{G}/V_{PP}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}/V_{PP}$, whichever occurs first†		0		0		ns

† Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6.50 V and $\overline{G}/V_{PP}$ = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Disable time, output from $\overline{G}/V_{PP}$	0	130	ns

NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (Reference page 10.)
4. Common test conditions apply for t_{dis} except during programming.

recommended timing requirements for programming: V_{CC} = 6.50 V and $\overline{G}/V_{PP}$ = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

		MIN	TYP	MAX	UNIT
$t_{w(IPGM)}$	Pulse duration, initial program	95	100	105	µs
$t_{su(A)}$	Setup time, address	2			µs
$t_{su(D)}$	Setup time, data	2			µs
$t_{su(VPP}$	Setup time, $\overline{G}/V_{PP}$	2			µs
$t_{su(VCC)}$	Setup time, V_{CC}	2			µs
$t_{h(A)}$	Hold time, address	0			µs
$t_{h(D)}$	Hold time, data	2			µs
$t_{h(VPP)}$	Hold time, $\overline{G}/V_{PP}$	2			µs
$t_{rec(PG)}$	Recovery time, $\overline{G}/V_{PP}$	2			µs
t_{EHD}	Data valid from $\overline{E}$ low			1	µs
$t_{r(PG)G}$	Rise time, $\overline{G}/V_{PP}$	50			ns

NOTE 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (Reference below.)

PARAMETER MEASUREMENT INFORMATION

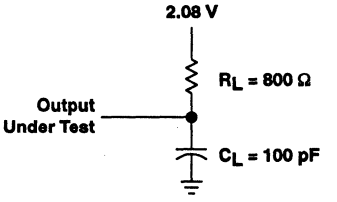
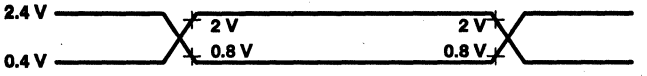


Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

PARAMETER MEASUREMENT INFORMATION

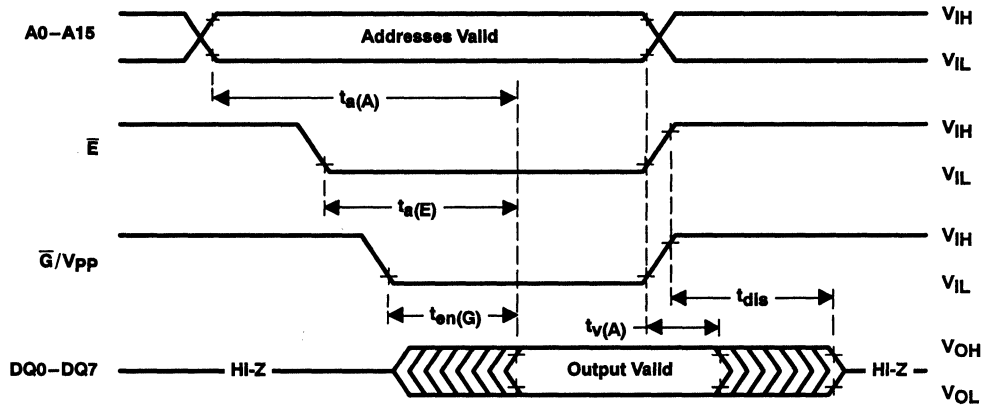
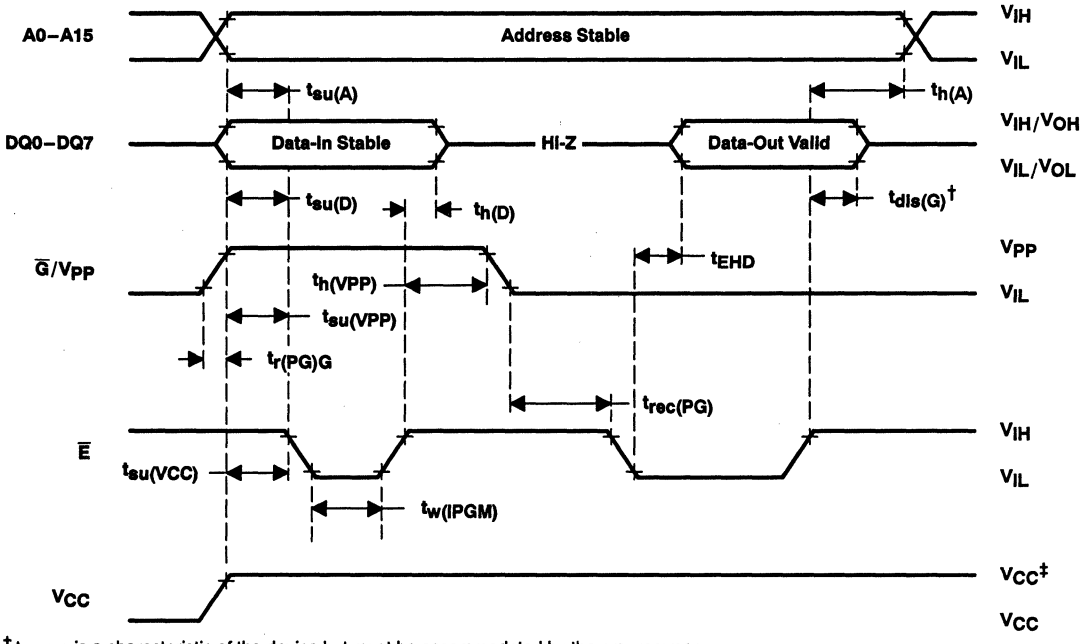


Figure 3. Read-Cycle Timing

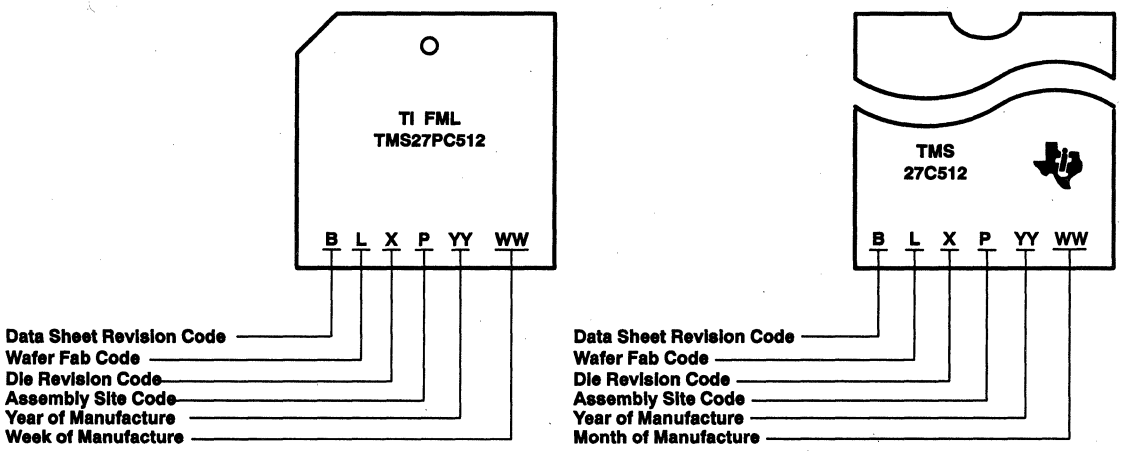


† $t_{dis(G)}$ is a characteristic of the device but must be accommodated by the programmer.
‡ 13-V $\overline{G}/V_{PP}$ and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program-Cycle Timing (SNAP! Pulse Programming)

device symbolization

This data sheet is applicable to all TI TMS27C512 CMOS EPROMs and TMS27PC512 CMOS OTP PROMs with the data sheet revision code "B" as shown below.



TMS27C010A 1048576-BIT UV ERASABLE PROGRAMMABLE
TMS27PC010A 1048576-BIT PROGRAMMABLE
READ-ONLY MEMORY

SMLS110B – NOVEMBER 1990 – REVISED JUNE 1995

- **Organization . . . 128K × 8**
- **Single 5-V Power Supply**
- **Operationally Compatible With Existing Megabit EPROMs**
- **Industry Standard 32-Pin Dual-In-line Package, 32-Lead Plastic Leaded Chip Carrier, and 32-Lead Thin Small-Outline Package**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

  V_{CC} ± 10%

'27C010A-10	100	ns
'27C/PC010A-12	120	ns
'27C/PC010A-15	150	ns
'27C/PC010A-20	200	ns

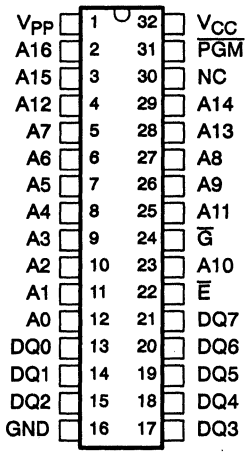
- **8-Bit Output For Use In Microprocessor-Based Systems**
- **Very High-Speed SNAP! Pulse Programming**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 165 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-In and Choices of Operating Temperature Ranges**

description

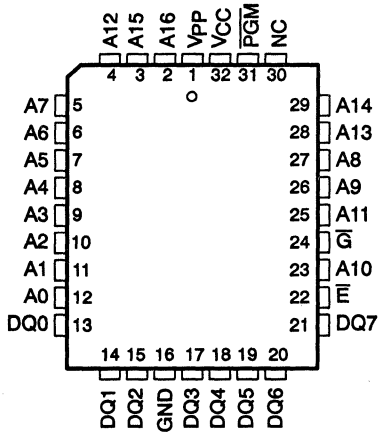
The TMS27C010A series are 1048576-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC010A series are 1048576-bit, one-time electrically programmable read-only memories.

J AND N PACKAGES
(TOP VIEW)



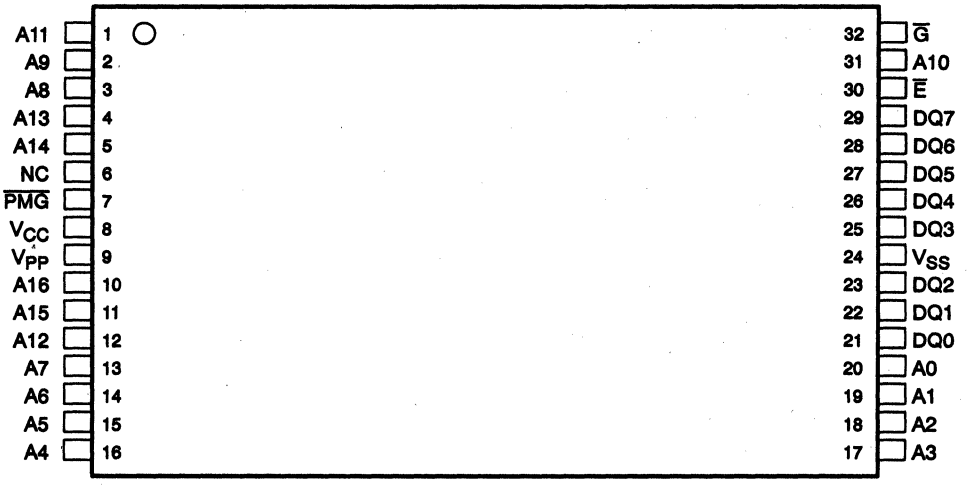
FM PACKAGE
(TOP VIEW)



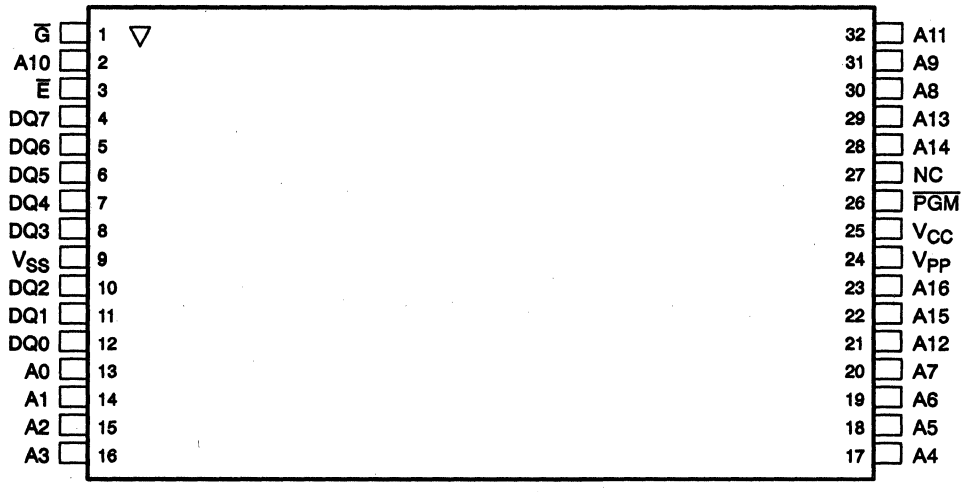
PIN NOMENCLATURE	
A0–A16	Address Inputs
DQ0–DQ7	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
$\overline{PGM}$	Program
V_{CC}	5-V Power Supply
V_{PP}	13-V Power Supply†

† Only in program mode

TMS27PC010A . . . DD PACKAGE†
(TOP VIEW)



TMS27PC010A . . . DU PACKAGE†
REVERSE PINOUT
(TOP VIEW)



† The packages shown are for pinout reference only.

description (continued)

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27C010A EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C010A is also offered with two choices of temperature ranges, 0°C to 70°C (JL suffix) and –40°C to 85°C (JE suffix). The TMS27C010A is also offered with 168-hour burn-in on both temperature ranges (JL4 and JE4 suffix). (See table below.)

The TMS27PC010A OTP PROM is offered in a dual-in-line plastic package (N suffix), a 32-pin, plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix), and a 32-lead TSOP package (DD and DU suffixes). The TMS27PC010A is offered with two choices of temperature ranges, 0°C to 70°C (NL, FML, DDL, and DUL suffixes) and – 40°C to 85°C (NE, FME, DDE, and DUE suffixes). (See table below.)

EPROM AND OTP PROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HOUR BURN-IN VS TEMPERATURE RANGES	
	0°C to 70°C	– 40°C to 85°C	0°C to 70°C	– 40°C to 85°C
TMS27C010A-xxx	JL	JE	JL4	JE4
TMS27PC010A-xxx	NL	NE	NL4	NE4
	FML	FME	FML4	FME4
	DDL	DDE		
	DUL	DUE		

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 13-V supply is needed for programming. All programming signals are TTL level. These devices are programmable using the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of thirteen seconds. For programming outside the system, existing EPROM programmers can be used. Locations can be programmed singly, in blocks, or at random.

operation

The seven modes of operation are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse), and 12 V on A9 for signature mode.

FUNCTION	MODE†							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7	Data Out	Hi-Z	Hi-Z	Data In	Data Out	Hi-Z	CODE	
							MFG	DEVICE
							97	D6

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C010As or TMS27PC010As are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C010A and TMS27PC010A is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C010A)

Before programming, the TMS27C010A EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C010A, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

initializing (TMS27PC010A)

The one-time programmable TMS27PC010A PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C010A and TMS27PC010A are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which programs in a nominal time of thirteen seconds. Actual programming time varies as a function of the programmer used.

The SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$. Data is presented in parallel (eight bits) on pins DQ0 through DQ7. Once addresses and data are stable, $\overline{PGM}$ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 5\ V \pm 10\%$.

program inhibit

Programming can be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pins.

program verify

Programmed bits can be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

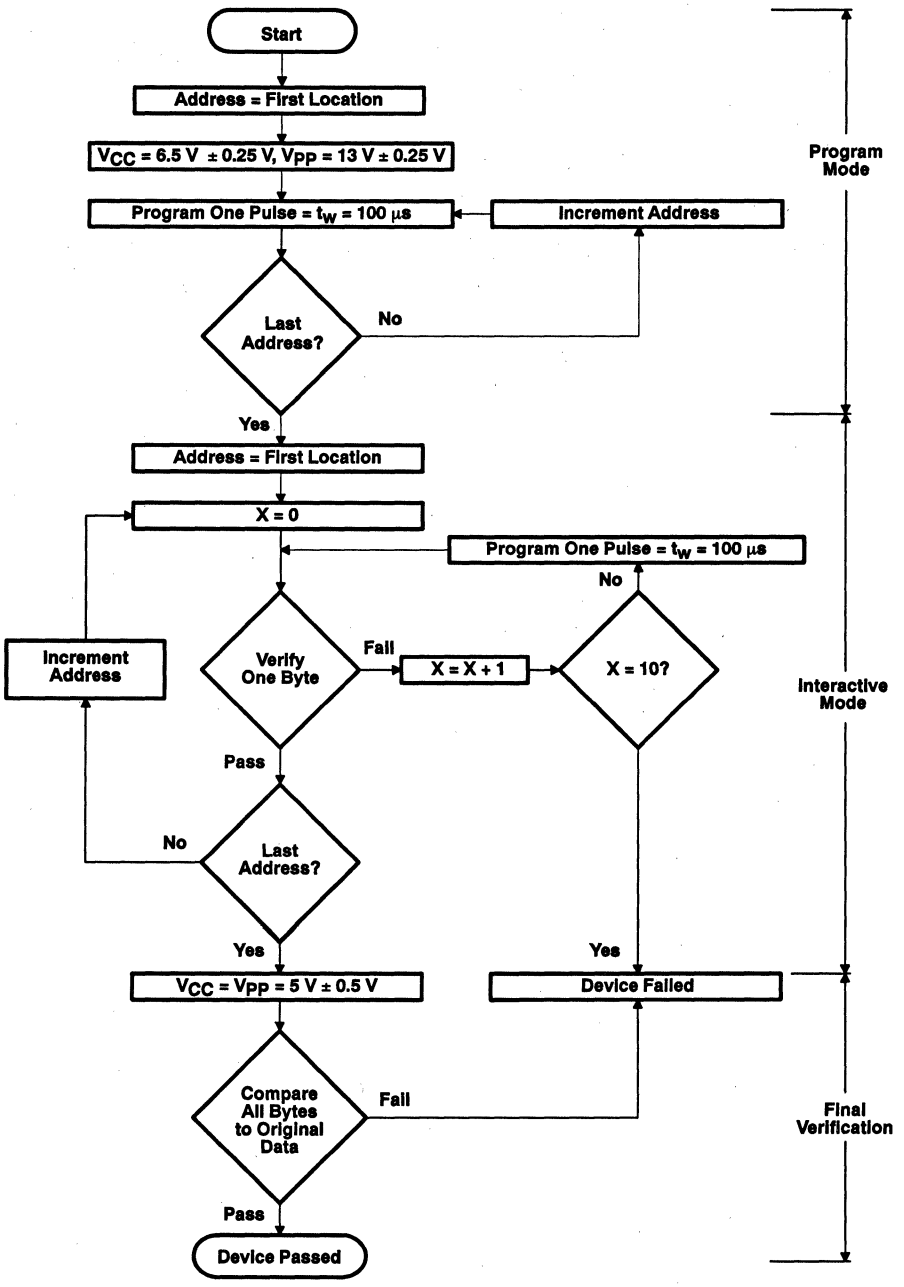


Figure 1. SNAP! Pulse Programming Flowchart

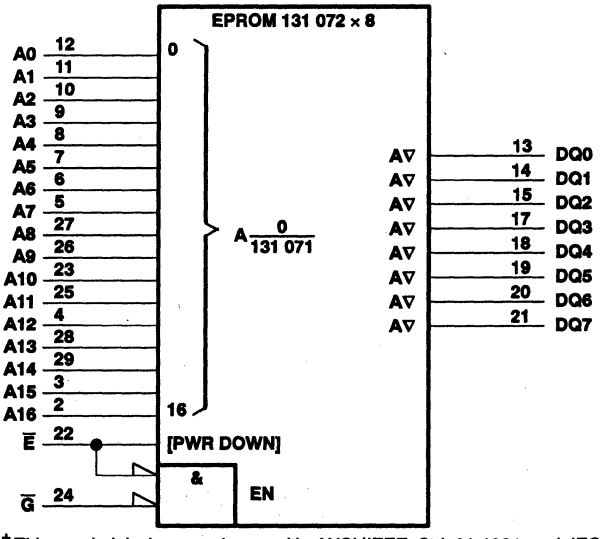
signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All addresses must be held low. The signature code for these devices is 97D6. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code D6 (Hex), as shown by the signature mode table below.

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	1	1	0	1	0	1	1	0	D6

†$\overline{E} = \overline{G} = V_{IL}$, A1–A8 = V_{IL}, A9 = V_H, A10–A16 = V_{IL}, $V_{PP} = V_{CC}$.

logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. J package illustrated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range, All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13.5 V
Output voltage range, with respect to V_{SS} (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C010A-__JL and JL4,
'27PC010A-__NL, FML, DDL, and DUL) ..... 0°C to 70°C
Operating free-air temperature range ('27C010A-__JE and JE4,
'27PC010A-__NE, FME, DDE, and DUE) ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				'27C010A-10 '27C010A/PC010A-12 '27C010A/PC010A-15 '27C010A/PC010A-20			UNIT
				MIN	TYP	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)		V_{CC}−0.6	V_{CC}	V_{CC}+0.6	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level dc input voltage		TTL	2		V_{CC}+0.5	V
			CMOS	V_{CC}−0.2		V_{CC}+0.5	
V_{IL}	Low-level dc input voltage		TTL	−0.5		0.8	V
			CMOS	−0.5		GND+0.2	
T_A	Operating free-air temperature		'27C010A-__JL,JL4 '27PC010A-__NL, FML, DDL, DUL	0		70	°C
T_A	Operating free-air temperature		'27C010A-__JE,JE4 '27PC010A-__NE, FME, DDE, DUE	−40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. During programming, V_{PP} must be maintained at 13 V ± 0.25 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level dc output voltage		I_{OH} = −20 μA	V_{CC}−0.2		V
			I_{OH} = −2.5 mA	3.5		
V_{OL}	Low-level dc output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 μA		0.1	
I_I	Input current (leakage)		V_I = 0 V to 5.5 V		±1	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}		±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC} ± 0.2 V		100	
I_{CC2}	V_{CC} supply current (active) (output open)		V_{CC} = 5.5 V, E = V_{IL}, t_{cycle} = minimum cycle time†, outputs open		30	mA

† Minimum cycle time = maximum access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
C_I	Input capacitance	V_I = 0 V, f = 1 MHz		4	8	pF
C_O	Output capacitance	V_O = 0 V, f = 1 MHz		6	10	pF

‡ Capacitance measurements are made on sample basis only.
§ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended ranges of operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS	'27C010A-10		'27C010A-12 '27PC010A-12		'27C010A-15 '27PC010A-15		'27C010A-20 '27PC010A-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	CL = 100 pF, 1 Series 74 TTL load, Input t_r ≤ 20 ns, Input t_f ≤ 20 ns		100		120		150		200	ns
$t_{a(E)}$	Access time from chip enable			100		120		150		200	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		55		75		75	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first¶		0	50	0	50	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first¶		0		0		0		0		ns

¶ Value calculated from 0.5-V delta to measured output level.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC testing waveform).
5. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

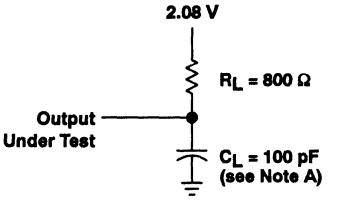
PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Disable time, output disable time from $\overline{G}$	0	130	ns
$t_{en(G)}$	Enable time, output enable time from $\overline{G}$		150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 4)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Pulse duration, program	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Setup time, address		2			µs
$t_{su(E)}$	Setup time, $\overline{E}$		2			µs
$t_{su(G)}$	Setup time, $\overline{G}$		2			µs
$t_{su(D)}$	Setup time, data		2			µs
$t_{su(VPP)}$	Setup time, V_{PP}		2			µs
$t_{su(VCC)}$	Setup time, V_{CC}		2			µs
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC testing waveform).

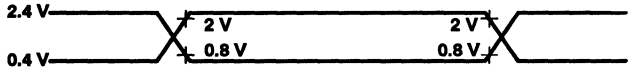
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 2. AC Test Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

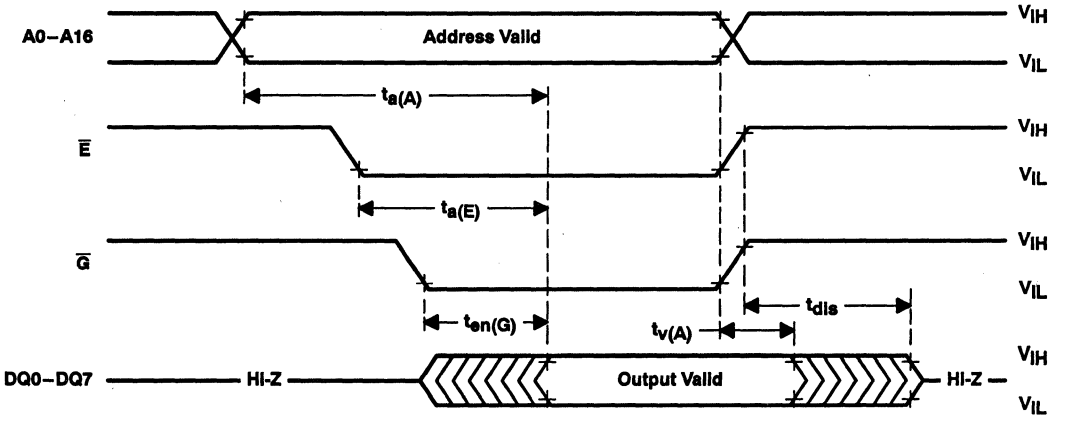
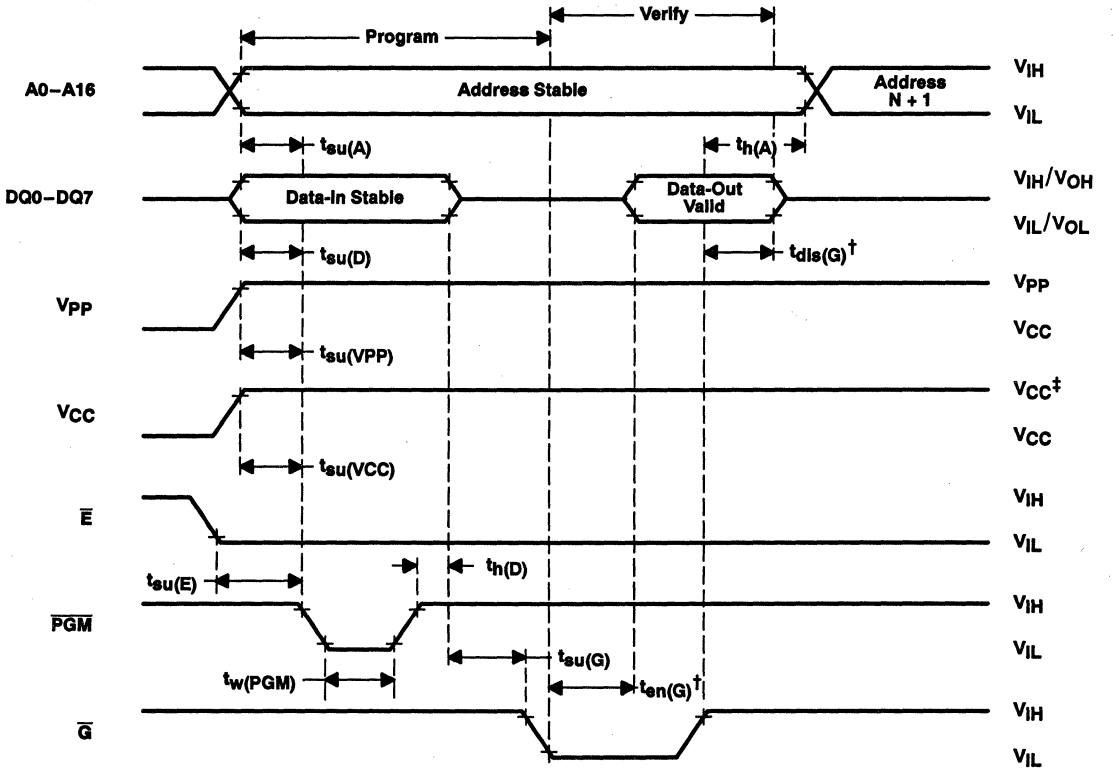


Figure 3. Read-Cycle Timing

PROGRAMMING INFORMATION



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program-Cycle Timing (SNAP! Pulse Programming)

- **Wide-Word Organization . . . 64K × 16**
- **Single 5-V Power Supply**
- **Operationally Compatible With Existing Megabit EPROMs**
- **40-Pin Dual-In-Line Package and 44-Lead Plastic Leaded Chip Carrier**
- **All Inputs/Outputs Fully TTL Compatible**
- **±10% V_{CC} Tolerance**
- **Max Access/Min Cycle Time**

'27C210A-10	100	ns
'27C/PC210A-12	120	ns
'27C/PC210A-15	150	ns
'27C/PC210A-20	200	ns
'27C/PC210A-25	250	ns

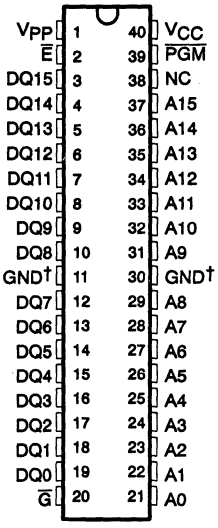
- **16-Bit Output For Use In Microprocessor-Based Systems**
- **Very High-Speed SNAP! Pulse Programming**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation**
  - **Active . . . 275 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-In and Choices of Operating Temperature Ranges**

description

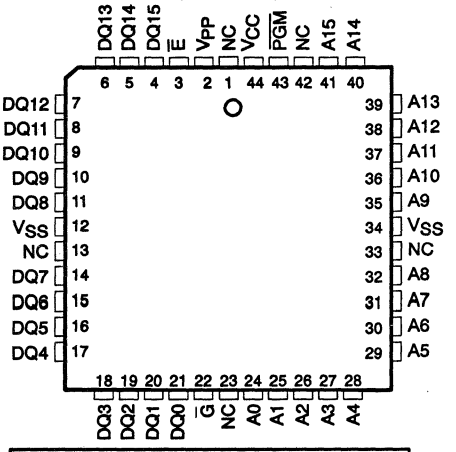
The TMS27C210A series are 1048576-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC210A series are 1048576-bit, one-time electrically programmable read-only memories.

J PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A15	Address Inputs
DQ0–DQ15	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
$\overline{PGM}$	Program
V_{CC}	5-V Power Supply
V_{PP}	13-V Power Supply‡

† Pins 11 and 30 must be connected externally to ground.
‡ Only in program mode.

description (continued)

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27C210A EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C210A is also offered with two choices of temperature ranges, 0°C to 70°C (JL suffix) and – 40°C to 85°C (JE suffix). The TMS27C210A is also offered with 168-hour burn-in on both temperature ranges (JL4 and JE4 suffixes).

The TMS27PC210A OTP PROM is offered in a 44-pin plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FN suffix). The TMS27PC210A is offered with two choices of temperature ranges, 0°C to 70°C (FNL suffix) and –40°C to 85°C (FNE suffix). The TMS27PC210A is also offered with 168 hour burn-in on both temperature ranges (FNL4 and FNE4 suffixes). (See table below.)

EPROM AND OTP PROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HOUR BURN-IN VS TEMPERATURE RANGES	
	0°C to 70°C	– 40°C to 85°C	0°C to 70°C	– 40°C to 85°C
TMS27C210A-xx	JL	JE	JL4	JE4
TMS27PC210A-xx	FNL	FNE	FNL4	FNE4

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor based systems. One other (13 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

The seven modes of operation for the TMS27C210A and TMS27PC210A are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V), and 12 V on A9 for signature mode.

FUNCTION	MODE†							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ15	Data Out	Hi-Z	Hi-Z	Data In	Data Out	Hi-Z	CODE	
							MFG	DEVICE
							97	AB

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C210As or TMS27PC210As are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C210A and TMS27PC210A is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, "*Design Considerations; Latchup Immunity of the HVCMOS EPROM Family*", available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 50 mA to 500 μA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C210A)

Before programming, the TMS27C210A is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W•s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C210A the window should be covered with an opaque label.

initializing (TMS27PC210A)

The one-time programmable TMS27PC210A PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C210A and TMS27PC210A are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which can program in a nominal time of seven seconds. Actual programming time varies as a function of the programmer used.

The SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$. Data is presented in parallel (16 bits) on pins DQ0 through DQ15. Once addresses and data are stable, $\overline{PGM}$ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 5\ V \pm 10\%$.

program inhibit

Programming can be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pins.

program verify

Programmed bits can be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V. Two identifier bytes are accessed by toggling A0. DQ0–DQ7 contain the valid codes. All other addresses must be held low. The signature code for these devices is 97AB. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code AB (Hex), as shown by the signature mode table below.

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	1	0	1	0	1	0	1	1	AB

† $\overline{E} = \overline{G} = V_{IL}$, A9 = V_H, A1–A8 = V_{IL}, A10–A15 = V_{IL}, $V_{PP} = V_{CC}$, $\overline{PGM} = V_{IH}$ or V_{IL}.

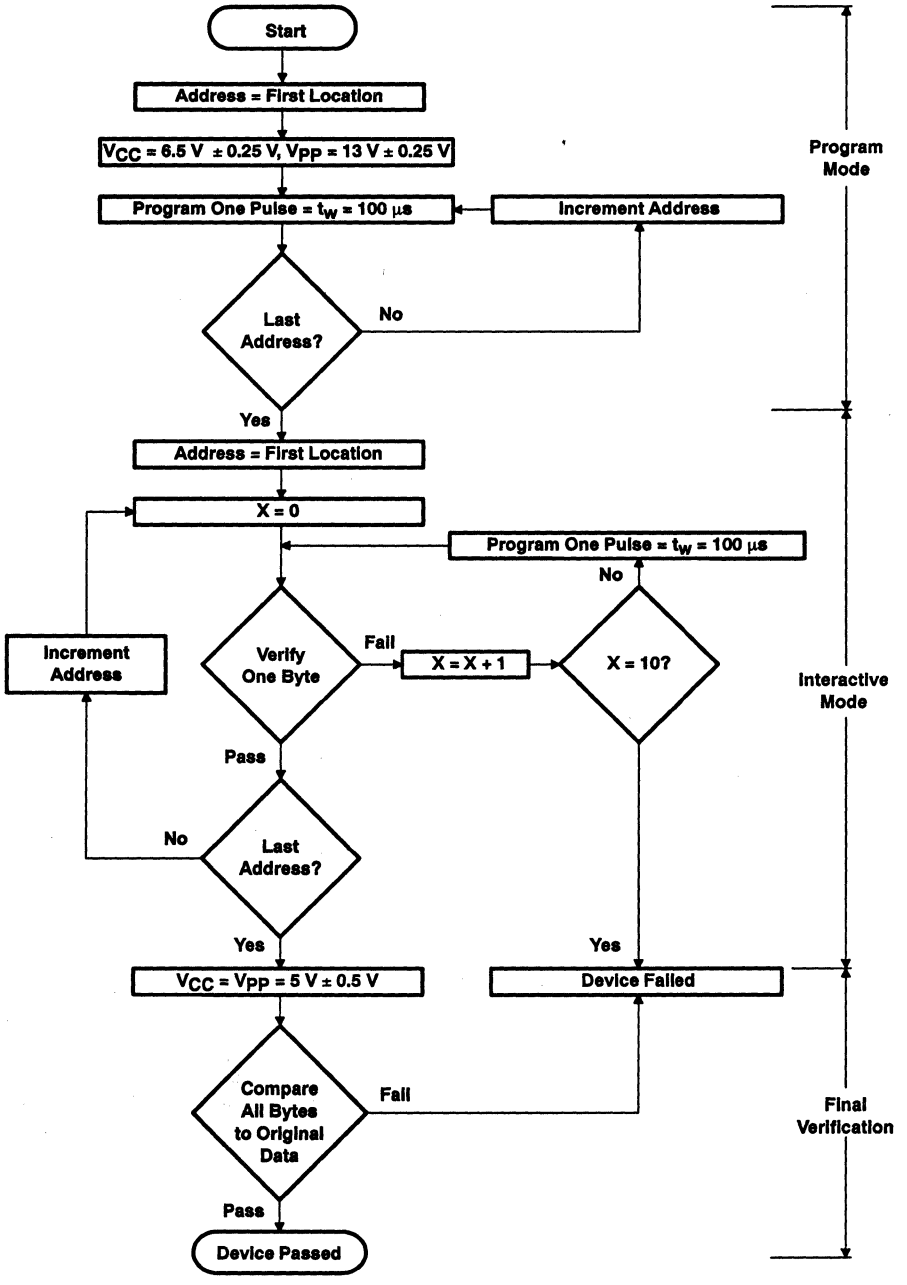
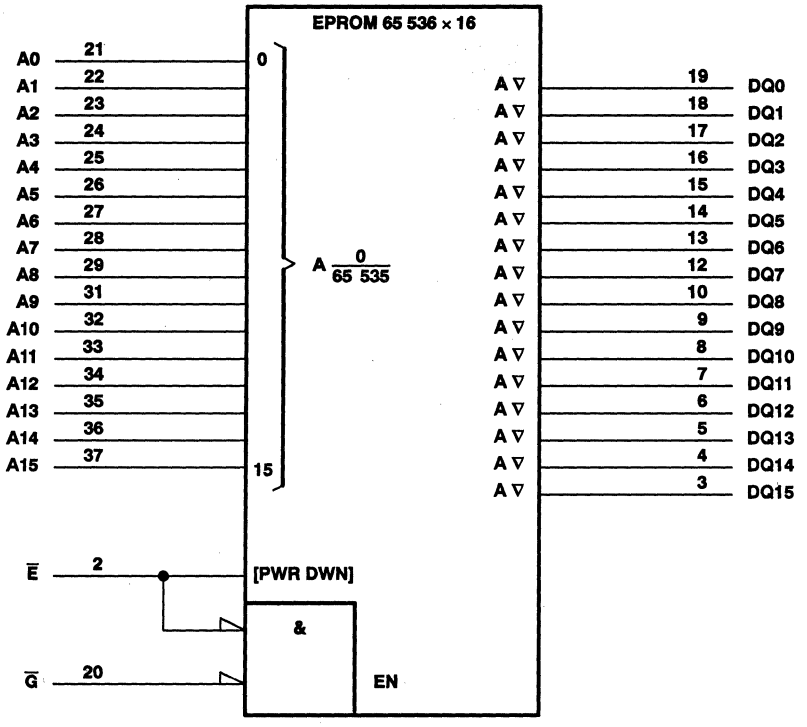


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91–1984 and IEC Publication 617–12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C210A-_ _JL and JL4, '27PC210A-_ _FNL) ..... 0° C to 70°C
Operating free-air temperature range ('27C210A-_ _JE and JE4) ..... − 40° C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			TMS27C210A-10 TMS27C/PC210A-12 TMS27C/PC210A-15 TMS27C/PC210A-20 TMS27C/PC210A-25			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode	$V_{CC}-0.6$	V_{CC}	$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	
V_{IH}	High-level dc input voltage	TTL	2		$V_{CC}+0.5$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+0.5$	
V_{IL}	Low-level dc input voltage	TTL	−0.5		0.8	V
		CMOS	−0.5		GND+0.2	
T_A	Operating free-air temperature	'27C210A-_ _JL, JL4 '27PC210A-_ _FNL	0		70	°C
T_A	Operating free-air temperature	'27C210A-_ _JE, JE4	−40		85	°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over recommended ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level dc output voltage		$I_{OH}=-20\ \mu A$	$V_{CC}-0.2$		V
			$I_{OH}=-2$ mA	2.4		
V_{OL}	Low-level dc output voltage		$I_{OL}=2.1$ mA		0.4	V
			$I_{OL}=20\ \mu A$		0.1	
I_I	Input current (leakage)		$V_I=0$ V to 5.5 V		±1	µA
I_O	Output current (leakage)		$V_O=0$ V to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current		$V_{PP}=V_{CC}=5.5$ V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP}=13$ V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC}=5.5$ V, $\overline{E}=V_{IH}$		500	µA
		CMOS-input level	$V_{CC}=5.5$ V, $\overline{E}=V_{CC}$		100	
I_{CC2}	V_{CC} supply current (active)		$V_{CC}=5.5$ V, $\overline{E}=V_{IL}$, t_{cycle} = minimum cycle time, outputs open†		50	mA

† Minimum cycle time = maximum address access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
C_I	Input capacitance	$V_I=0$ V, f = 1 MHz		8	12	pF
C_O	Output capacitance	$V_O=0$ V, f = 1 MHz		12	15	pF

‡ Capacitance measurements are made on a sample basis only.
§ Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS	'27C210A-10		'27C210A-12 '27PC210A-12		'27C210A-15 '27PC210A-15		'27C210A-20 '27PC210A-20		'27C210A-25 '27PC210A-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	CL = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		100		120		150		200		250	ns
$t_{a(E)}$	Access time from chip enable			100		120		150		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		55		75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	50	0	50	0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		0		0		ns

† Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC testing waveform)

4. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

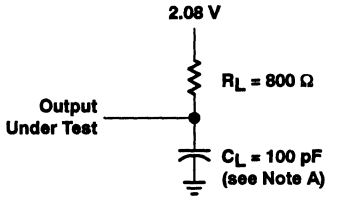
PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0	100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 3)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Pulse duration, program	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Setup time, address		2			µs
$t_{su(E)}$	Setup time, $\overline{E}$		2			µs
$t_{su(G)}$	Setup time, $\overline{G}$		2			µs
$t_{su(D)}$	Setup time, data		2			µs
$t_{su(VPP)}$	Setup time, V_{PP}		2			µs
$t_{su(VCC)}$	Setup time, V_{CC}		2			µs
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs

NOTE 3: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC testing waveform)

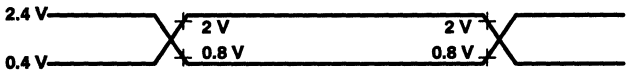
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

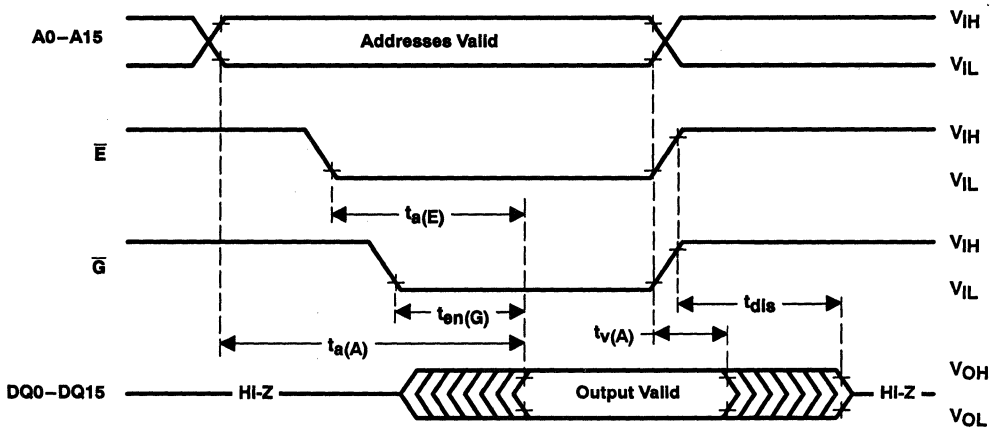
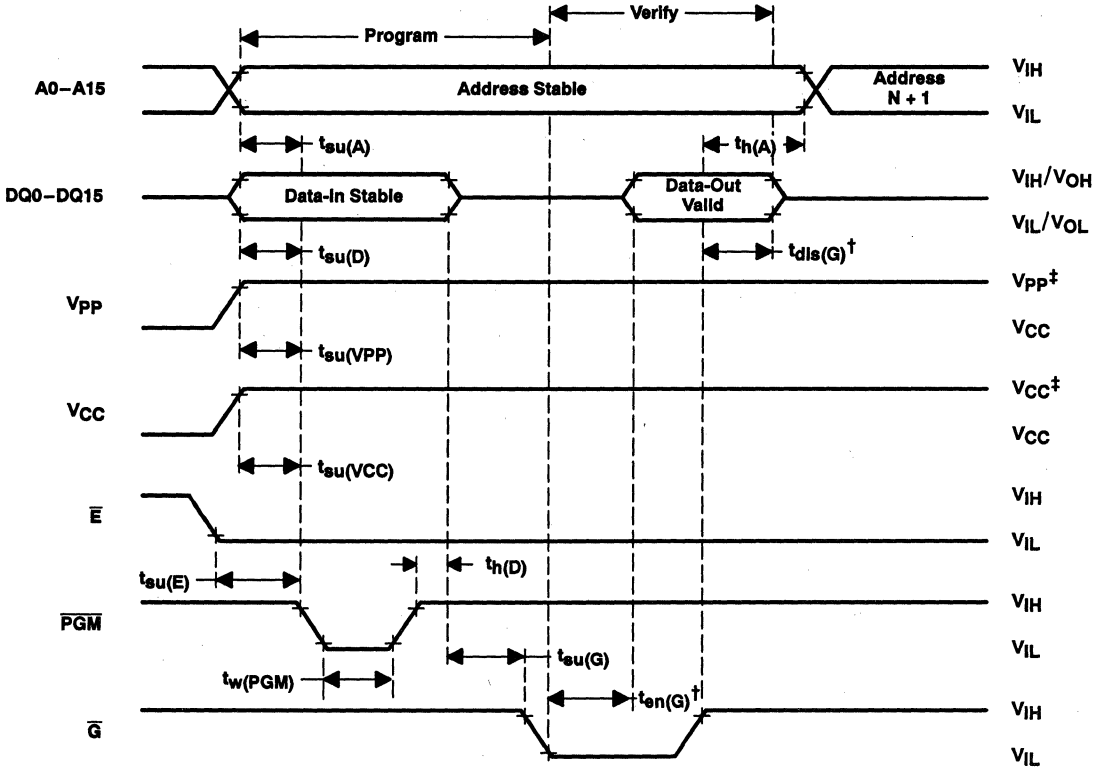


Figure 3. Read-Cycle Timing

PROGRAMMING INFORMATION



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program-Cycle Timing (SNAP! Pulse Programming)

TMS27C020 2097152-BIT UV ERASABLE PROGRAMMABLE
TMS27PC020 2097152-BIT PROGRAMMABLE
READ-ONLY MEMORY

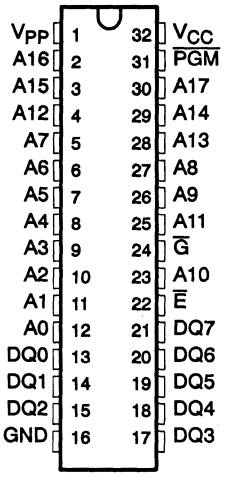
SMLS020B – NOVEMBER 1990 – REVISED JUNE 1995

- **Organization . . . 256K × 8**
- **Single 5-V Power Supply**
- **Operationally Compatible With Existing Megabit EPROMs**
- **Industry Standard 32-Pin Dual-In-line Package and 32-Lead Plastic Leaded Chip Carrier**
- **All Inputs/Outputs Fully TTL Compatible**
- **±10% V_{CC} Tolerance**
- **Max Access/Min Cycle Time V_{CC} ± 10%**

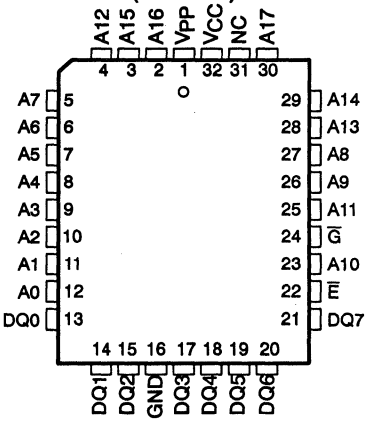
'27C/PC020-12	120 ns
'27C/PC020-15	150 ns
'27C/PC020-20	200 ns
'27C/PC020-25	250 ns

- **8-Bit Output For Use In Microprocessor-Based Systems**
- **Very High-Speed SNAP! Pulse Programming**
- **Power Saving CMOS Technology**
- **3-State Output Buffers**
- **400 mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 165 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-In, and Choices of Operating Temperature Ranges**

J PACKAGE
(TOP VIEW)



TMS27PC020†
FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A17	Address Inputs
DQ0–DQ7	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
$\overline{PGM}$	Program
V_{CC}	5-V Power Supply
V_{PP}	13-V Power Supply‡

† The ADVANCE INFORMATION notice applies to this package.
‡ Only in program mode.

description

The TMS27C020 series are 2097152-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC020 series are one-time electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

description (continued)

The TMS27C020 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C020 is also offered with two choices of temperature ranges of 0° to 70°C (JL suffix) and – 40°C to 85°C (JE suffix). The TMS27C020 is also offered with 168-hour burn-in on both temperature ranges (JL4 and JE4 suffixes). (See table below.)

The TMS27PC020 is offered in a 32-lead plastic leaded chip carrier using 1,25 mm (50 mil) lead spacing (FM suffix). The TMS27PC020 is offered with a temperature range of 0°C to 70°C.

EPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS. TEMPERATURE RANGES	
	0°C to 70°C	– 40°C to 85°C	0°C to 70°C	– 40°C to 85°C
TMS27C020-XXX	JL	JE	JL4	JE4
TMS27PC020-XXX	FML			

These EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (13 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

The seven modes of operation for the TMS27C020 and TMS27PC020 are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V), and V_H (12 V) on A9 for the signature mode.

FUNCTION	MODE†							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7	Data Out	Hi-Z	Hi-Z	Data In	Data Out	Hi-Z	CODE	
							MFG	DEVICE
							97	32

† X can be V_{IL} or V_{IH}
‡ $V_H = 12\ V \pm 0.5\ V$

read/output disable

When the outputs of two or more TMS27C020s or TMS27PC020s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C020 and TMS72PC020 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the TMS27C020 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C020, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

SNAP! Pulse programming

The TMS27C020 and TMS27PC020 are programmed using the TI SNAP! Pulse programming algorithm, illustrated by the flowchart in Figure 1, which programs in a nominal time of twenty-six seconds. Actual programming time varies as a function of the programmer used.

The SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$. Data is presented in parallel (eight bits) on pins DQ0 through DQ7. Once addresses and data are stable, $\overline{PGM}$ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 5\ V \pm 10\%$.

program inhibit

Programming can be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pins.

program verify

Programmed bits can be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All addresses must be held low. The signature code for the TMS27C020 is 9732. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code 32 (Hex), as shown by the signature mode table below.

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	0	0	1	1	0	0	1	0	32

† $\overline{E} = \overline{G} = V_{IL}$, A1–A8 = V_{IL}, A9 = V_H, A10–A17 = V_{IL}, $V_{PP} = V_{CC}$.

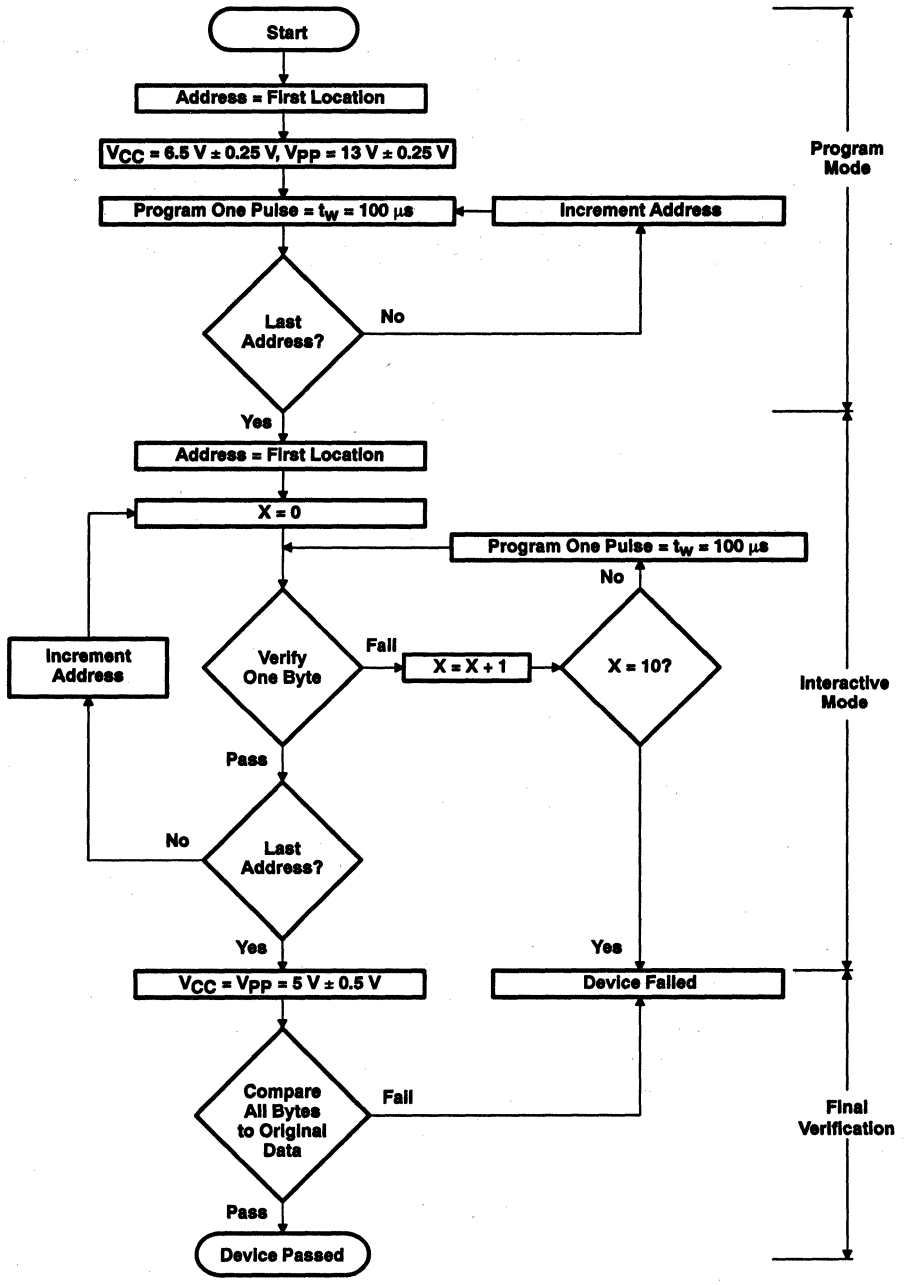
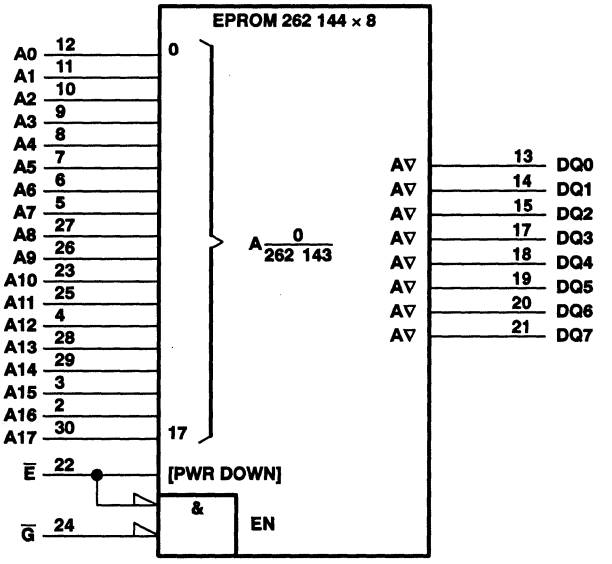


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for the J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13.5 V
Output voltage range, with respect to V_{SS} (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C020-_ _ JL and JL4) ..... 0°C to 70°C
Operating free-air temperature range ('27C020-_ _JE and JE4) ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode		$V_{CC}-0.6$	V_{CC}	$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level dc input voltage		TTL	2		$V_{CC}+0.5$	V
			CMOS	$V_{CC}-0.2$		$V_{CC}+0.5$	
V_{IL}	Low-level dc input voltage		TTL	−0.5		0.8	V
			CMOS	−0.5		GND+0.2	
T_A	Operating free-air temperature		'27C020-_ _JL, JL4	0		70	°C
T_A	Operating free-air temperature		'27C020-_ _JE, JE4	− 40		85	°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level dc output voltage		I_{OH} = −20 μA	$V_{CC}-0.2$		V
			I_{OH} = − 2 mA	2.4		
V_{OL}	Low-level dc output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 μA		0.1	
I_I	Input current (leakage)		V_I = 0 V to 5.5 V		±1	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}		±1	μA
I_{PP1}	V_{PP} supply current		$V_{PP}=V_{CC}$ = 5.5 V		10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, ... $\overline{E}=V_{IH}$		500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}=V_{CC}\pm0.2$ V		100	
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}=V_{IL}$, t_{cycle} = minimum cycle time, outputs open†		30	mA

† Minimum cycle time = maximum access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
C_I	Input capacitance	V_I = 0 V, f = 1 MHz		4	8	pF
C_O	Output capacitance	V_O = 0 V, f = 1 MHz		6	10	pF

‡ Capacitance measurements are made on sample basis only.
§ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS	'27C020-12 '27PC020-12		'27C020-15 '27PC020-15		27C020-20 27PC020-20		'27C020-25 '27PC020-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	CL = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		120		150		200		250	ns
$t_{a(E)}$	Access time from chip enable			120		150		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	50	0	60	0	60	0	80	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		0		ns

† Value calculated from 0.5-V delta to measured output level. This parameter is sampled and not 100% tested.

NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)

4. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

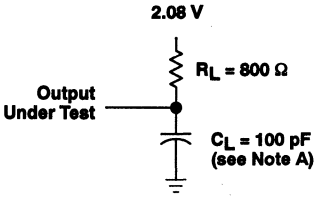
PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0	100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 3)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Pulse duration, program	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Setup time, address		2			µs
$t_{su(E)}$	Setup time, $\overline{E}$		2			µs
$t_{su(G)}$	Setup time, $\overline{G}$		2			µs
$t_{su(D)}$	Setup time, data		2			µs
$t_{su(VPP)}$	Setup time, V_{PP}		2			µs
$t_{su(VCC)}$	Setup time, V_{CC}		2			µs
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs

NOTE 3: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)

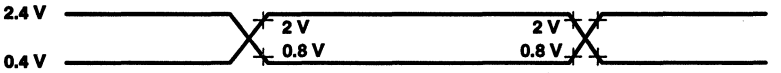
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

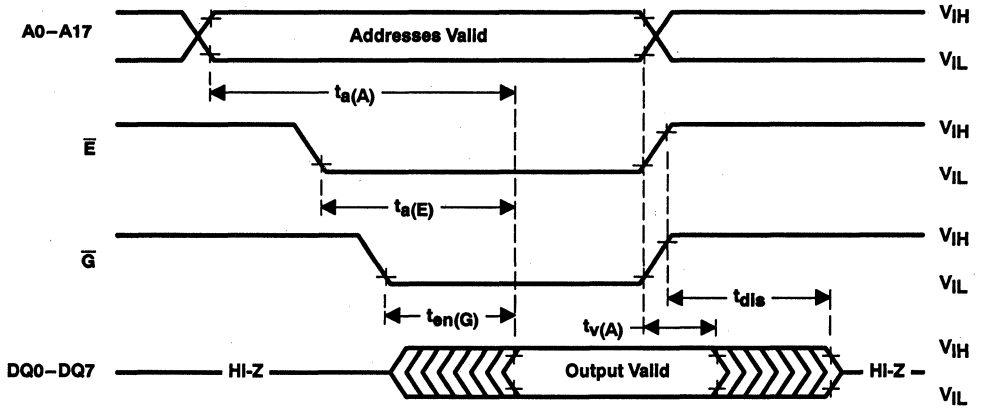
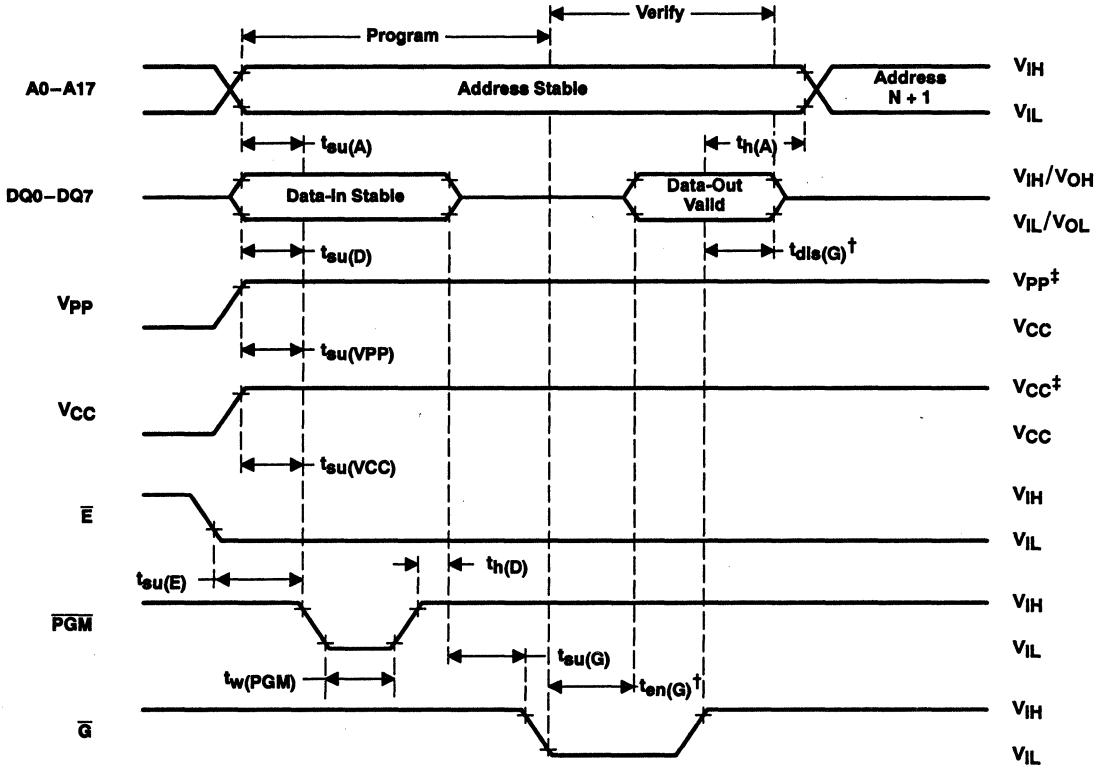


Figure 3. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program-Cycle Timing (SNAP! Pulse Programming)

- **Organization . . . 512K × 8**
- **Single 5-V Power Supply**
- **Industry Standard 32-Pin Dual In-Line Package and 32-Lead Plastic Leaded Chip Carrier**
- **All Inputs/Outputs Fully TTL Compatible**
- **Static Operation (No Clocks, No Refresh)**
- **Max Access/Min Cycle Time**

  V_{CC} ± 10%

  '27C/PC040-10 100 ns
  '27C/PC040-12 120 ns
  '27C/PC040-15 150 ns
- **8-Bit Output For Use in Microprocessor-Based Systems**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Assured DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 275 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Cas E (CMOS-Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-In, and Choice of Two Operating Temperature Ranges**

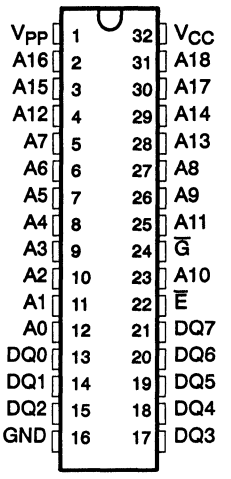
description

The TMS27C040 series are 4194304-bit, ultra-violet-light erasable, electrically programmable read-only memories.

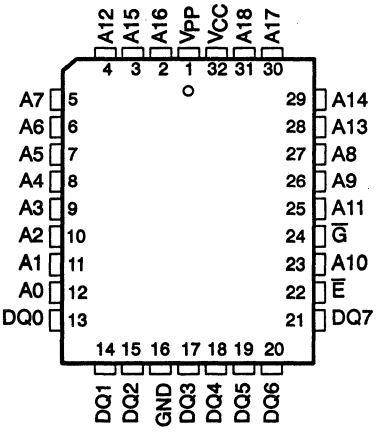
The TMS27PC040 series are 4194304-bit, one-time electrically programmable read-only memories.

These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits. Each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus.

TMS27C040
J PACKAGE
(TOP VIEW)



TMS27PC040
FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A18	Address Inputs
DQ0–DQ7	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply†

† Only in program mode.

description (continued)

The TMS27C040 is offered in a 600-mil ceramic dual-in-line package (J suffix). The TMS27C040 is offered with two choices of temperature ranges of 0°C to 70°C (JL suffix) and – 40°C to 85°C (JE suffix). The TMS27C040 is also offered with 168-hour burn-in on both temperature ranges (JL4 and JE4 suffixes). (See table below.)

The TMS27PC040 is offered in a 32-lead plastic leaded chip carrier package (FM suffix). The TMS27PC040 is characterized for operation from 0°C to 70°C (FML suffix).

FUNCTION	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR OPERATING TEMPERATURE RANGES WITH PEP4 168 HR. BURN-IN	
	0°C TO 70°C	–40 °C TO 85°C	0°C TO 70°C	–40 °C TO 85°C
TMS27C040-XXX	JL	JE	JL4	JE4
TMS27PC040-XXX	FML			

These EPROMs and PROMS operate from a single 5-V supply (in the read mode), and they are ideal for use in microprocessor-based systems. One other (13 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

The seven modes of operation are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V), and V_H (12 V) on A9 for the signature mode.

MODE	FUNCTION†						
	$\overline{E}$	$\overline{G}$	V_{PP}	V_{CC}	A9	A0	DQ0–DQ7
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	X	X	Data Out
Output Disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	X	Hi-Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	X	X	Hi-Z
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	Data In
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	X	X	Hi-Z
Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	Data Out
Signature Mode	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H‡	V_{IL}	MFG Code 97
						V_{IH}	Device Code 50

† X can be V_{IL} or V_{IH}
‡ V_H = 12 V ± 0.5 V

read/output disable

When the outputs of two or more TMS27C040s or TMS27PC040s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C040 and TMS27PC040 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 50 mA to 1 mA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C040)

Before programming, the TMS27C040 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet-light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C040, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

Initializing (TMS27PC040)

The one-time programmable TMS27PC040 PROM is provided with all bits in logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C040 and TMS27PC040 are programmed by using the SNAP! Pulse programming algorithm. The programming sequence is shown in the SNAP! Pulse programming flow chart (Figure 1).

The initial setup is V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IH}$. Once the initial location is selected, the data is presented in parallel (eight bits) on pins DQ0 through DQ7. Once addresses and data are stable, the programming mode is achieved when $\overline{E}$ is pulsed low (V_{IL}) with a pulse duration of $t_{w(PGM)}$. Every location is programmed only once before going to interactive mode.

In the interactive mode, the word is verified at V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IL}$. If the correct data is not read, the programming is performed by pulling $\overline{E}$ low with a pulse duration of $t_{w(PGM)}$. This sequence of verification and programming is performed up to a maximum of 10 times. When the device is fully programmed, all bytes are verified with $V_{CC} = V_{PP} = 5\ V \pm 10\%$.

program inhibit

Programming can be inhibited by maintaining high level inputs on the $\overline{E}$ and $\overline{G}$ pins.

program verify

Programmed bits can be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, and $\overline{E} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. The signature code for the TMS27C040 is 9750. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code 50 (Hex), as shown by the signature mode table below.

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	0	1	0	1	0	0	0	0	50

† $\overline{E} = \overline{G} = V_{IL}$, A1-A8 = V_{IL}, A9 = V_H, A10-A18 = V_{IL}, $V_{PP} = V_{CC}$.

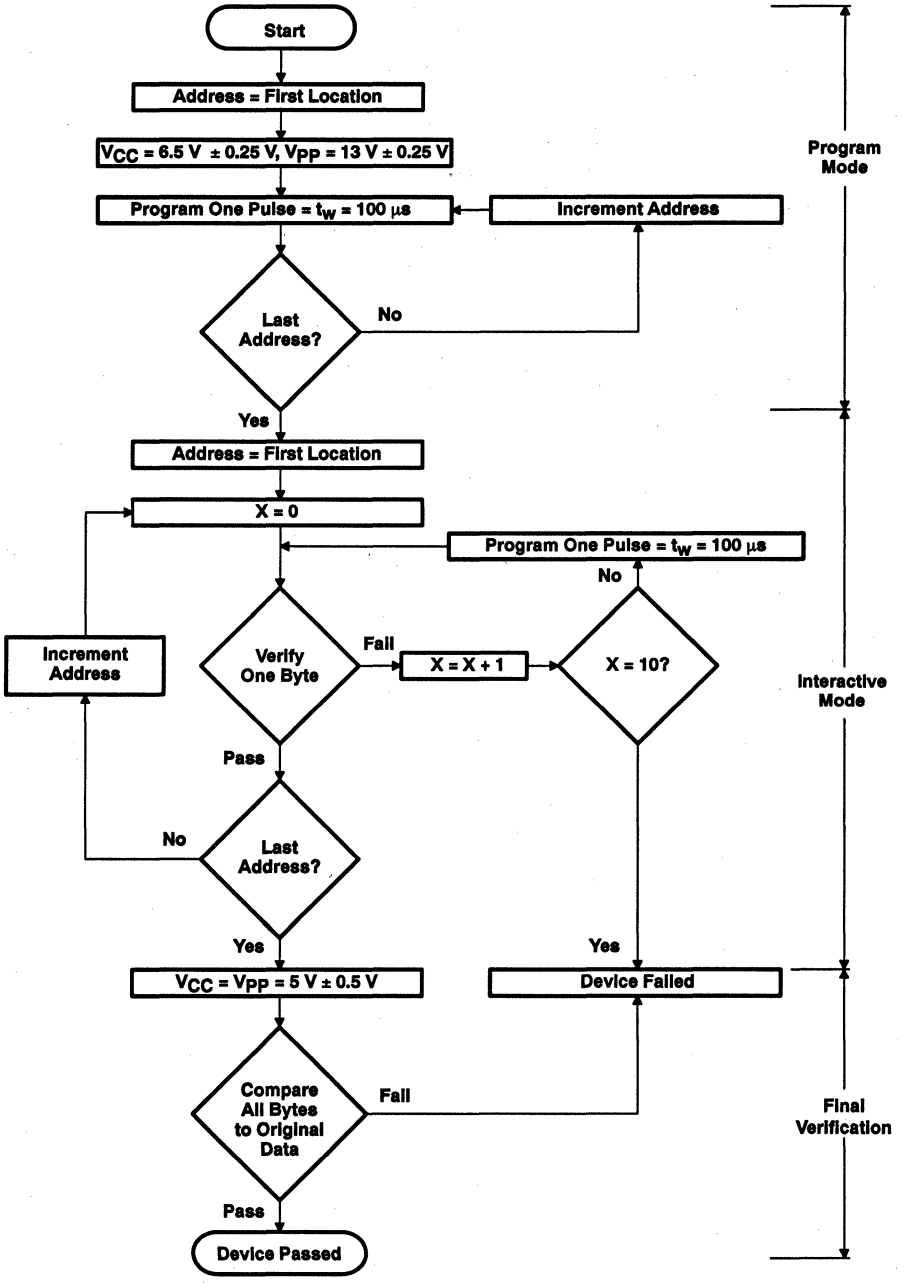
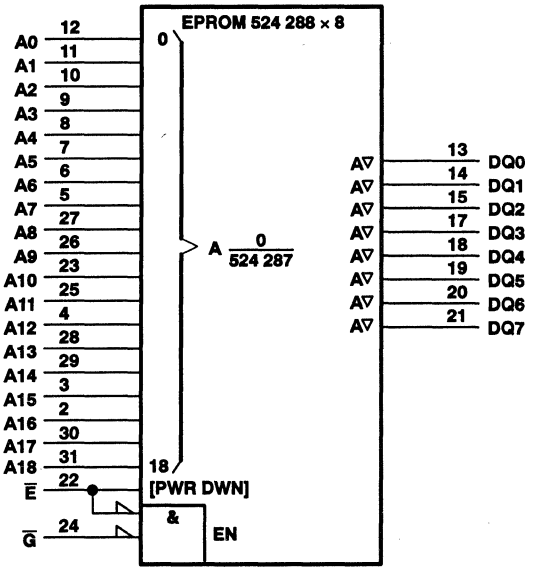


Figure 1. SNAP! Pulse Programming Flow Chart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for the J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... −0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13 V
Output voltage range, with respect to V_{SS} (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C040-_ _JL and JL4;'27PC040-_ _FML) ..... 0°C to 70°C
Operating free-air temperature range ('27C040-_ _JE and JE4) ..... − 40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 125°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode		$V_{CC}-0.6$		$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level dc input voltage		TTL	2		$V_{CC}+0.5$	V
			CMOS	$V_{CC}-0.2$		$V_{CC}+0.5$	V
V_{IL}	Low-level dc input voltage		TTL	−0.5		0.8	V
			CMOS	−0.5		0.2	V
T_A	Operating free-air temperature	'27C040-_ _JL and JL4 '27PC040-_ _FML		0		70	°C
T_A	Operating free-air temperature	'27C040-_ _JE and JE4		−40		85	°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level dc output voltage		$I_{OH}=-400\ \mu A$	2.4		V
			$I_{OH}=-20\ \mu A$	$V_{CC}-0.1$		
V_{OL}	Low-level dc output voltage		$I_{OL}=2.1$ mA		0.4	V
			$I_{OL}=20\ \mu A$		0.1	
I_I	Input current (leakage)		$V_I=0$ V to 5.5 V		±1	µA
I_O	Output current (leakage)		$V_O=0$ V to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current		$V_{PP}=V_{CC}=5.5$ V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP}=12.75$ V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-Input level	$V_{CC}=5.5$ V, $\overline{E}=V_{IH}$		1	mA
		CMOS-Input level	$V_{CC}=5.5$ V, $\overline{E}=V_{CC}$		100	µA
I_{CC2}	V_{CC} supply current (active)		$\overline{E}=V_{IL}$, $V_{CC}=5.5$ V t_{cycle} = minimum cycle time, outputs open†		50	mA

† Minimum cycle time = maximum access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz§

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	$V_I=0$ V		4	8	pF
C_o	Output capacitance	$V_O=0$ V		8	12	pF

‡ Capacitance measurements are made on sample basis only.
§ All typical values are at $T_A=25°C$ and nominal voltages.

switching characteristics over recommended ranges of operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS	'27C040-10 '27PC040-10		'27C040-12 '27PC040-12		'27C040-15 '27PC040-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		50		50	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first		0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5-V delta to measured output level.

NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)
4. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

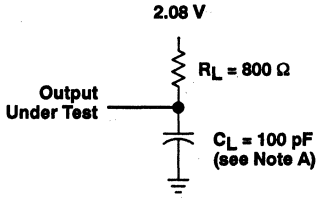
PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0	100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 3)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Pulse duration, program	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Setup time, address		2			µs
$t_{su(E)}$	Setup time, $\overline{E}$		2			µs
$t_{su(G)}$	Setup time, $\overline{G}$		2			µs
$t_{su(D)}$	Setup time, data		2			µs
$t_{su(VPP)}$	Setup time, V_{PP}		2			µs
$t_{su(VCC)}$	Setup time, V_{CC}		2			µs
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs

NOTE 3: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)

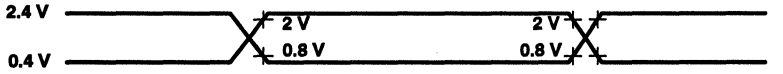
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

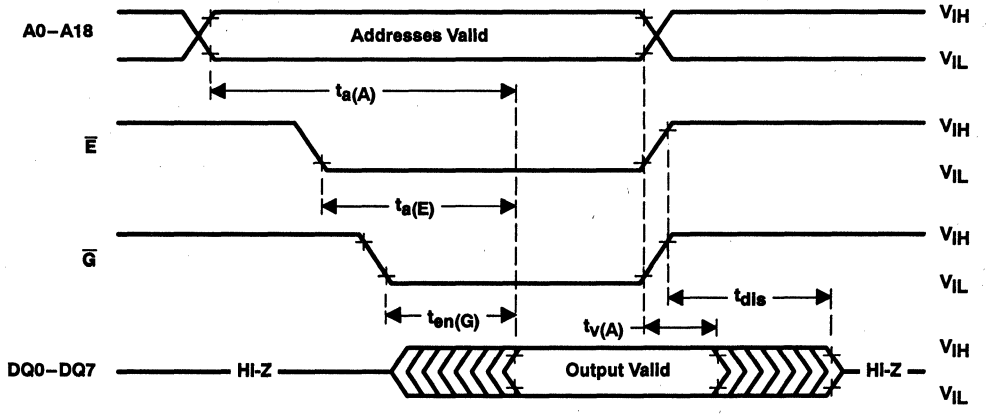
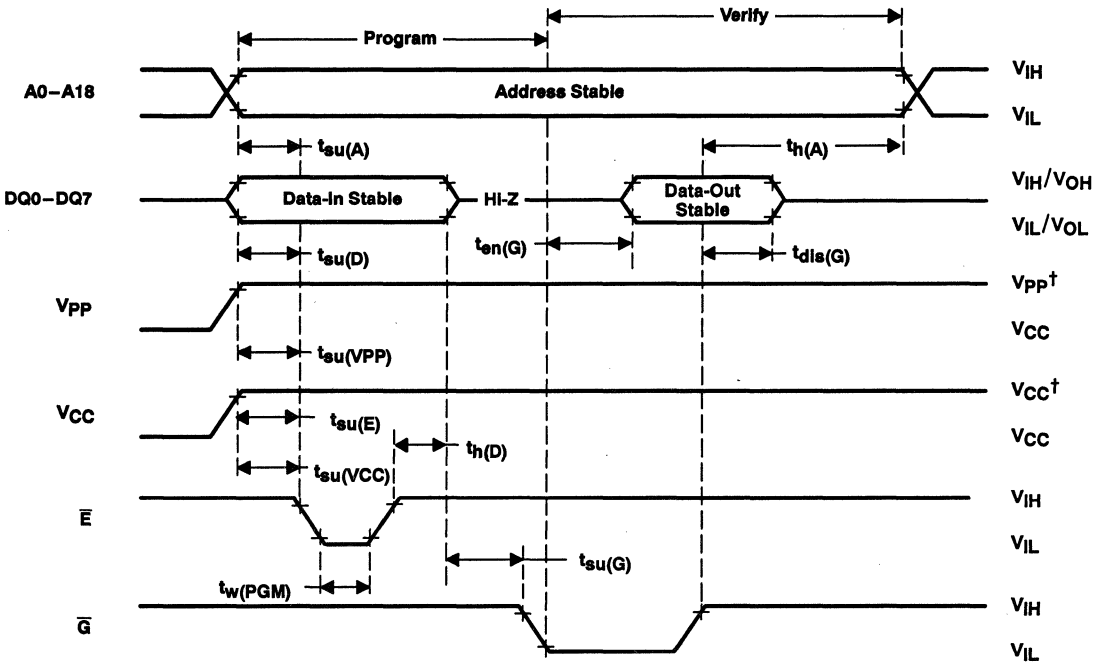


Figure 3. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming

Figure 4. Program-Cycle Timing (SNAP! Pulse Programming)

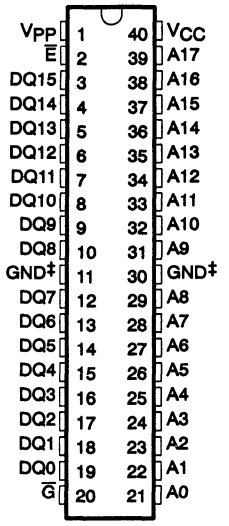
- **Wide-Word Organization . . . 256K × 16**
- **Single 5-V Power Supply**
- **All Inputs/Outputs Fully TTL Compatible**
- **Static Operations (No Clocks, No Refresh)**
- **Max Access/Min Cycle Time**

  V_{CC} ± 10%

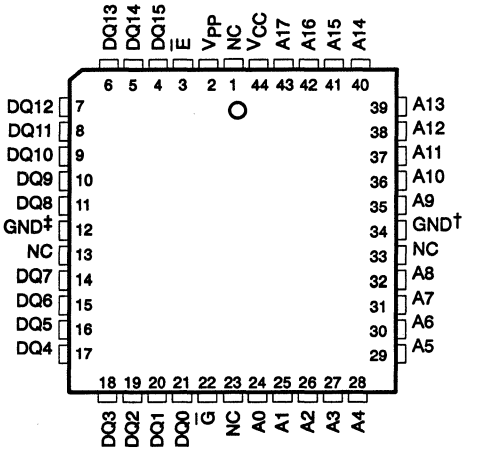
'27C/PC240-10	**100 ns**
'27C/PC240-12	**120 ns**
'27C/PC240-15	**150 ns**

- **16-Bit Output For Use in Microprocessor-Based Systems**
- **Very High Speed SNAP! Pulse Programming**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 275 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-In, and Choices of Operating Temperature Ranges**

TMS27C240 J PACKAGE
(TOP VIEW)



TMS27PC240 FN PACKAGE
(TOP VIEW)



description

The TMS27C240 series are 4194304-bit, ultra-violet-light erasable, electrically programmable read-only memories.

The TMS27PC240 series are 4194304-bit, one-time electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

PIN NOMENCLATURE	
A0–A17	Address Inputs
DQ0–DQ15	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply‡

† Pins 11 and 30 (J package) and pins 12 and 34 (FN package) must be connected externally to ground.
‡ Only in program mode

description (continued)

The TMS27C240 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C240 is also offered with two choices of temperature ranges of 0°C to 70°C (JL suffix) and – 40°C to 85°C (JE suffix). The TMS27C240 is also offered with 168-hour burn-in on both temperature ranges (JL4 and JE4 suffixes). (See table below.)

The TMS27PC240 OTP PROM is offered in a 44-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FN suffix). The TMS27PC240 is characterized for a temperature range of 0°C to 70°C.

	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C TO 70°C	– 40°C TO 85°C	0°C TO 70°C	– 40°C TO 85°C
TMS27C240-XXX	JL	JE	JL4	JE4
TMS27PC240-XXX	FNL	FNE	N/A	N/A

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), and they are ideal for use in microprocessor-based systems. One other (13 V) supply is needed for programming . All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

The eight modes of operation for the TMS27C240 and TMS27PC240 are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse), and 12 V on A9 for the signature mode.

	FUNCTION†						
	$\overline{E}$	$\overline{G}$	V_{PP}	V_{CC}	A9	A0	I/O
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	X	X	DQ0–DQ7 DQ8–DQ15
Output Disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	X	Hi-Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	X	X	Hi-Z
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	Data In
Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	Data Out
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	X	X	Hi-Z
Signature Mode (Mfg)	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H‡	V_{IL}	Mfg Code 0097
Signature Mode (Device)	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H‡	V_{IH}	Device Code 0030

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C240s or TMS27PC240s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C240 and TMS27PC240 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 50 mA to 1 mA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C240)

Before programming, the TMS27C240 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C240, the window should be covered with an opaque label.

initializing (TMS27PC240)

The one-time programmable TMS27PC240 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C240 and TMS27PC240 are programmed by using the SNAP! Pulse programming algorithm. The programming sequence is shown in the SNAP! Pulse programming flow chart, see Figure 1.

The initial setup is V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IH}$. Once the initial location is selected, the data is presented in parallel (eight bits) on pins DQ0 through DQ15. Once addresses and data are stable, the programming mode is achieved when $\overline{E}$ is pulsed low (V_{IL}) with a pulse duration of $t_{w(PGM)}$. Every location is programmed only once before going to interactive mode.

In the interactive mode, the word is verified at V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IL}$. If the correct data is not read, the programming is performed by pulling $\overline{E}$ low with a pulse duration of $t_{w(PGM)}$. This sequence of verification and programming is performed up to a maximum of 10 times. When the device is fully programmed, all bytes are verified with $V_{CC} = V_{PP} = 5\ V \pm 10\%$.

program inhibit

Programming can be inhibited by maintaining a high level input on the $\overline{E}$ and $\overline{G}$ pins.

program verify

Programmed bits can be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$ and $\overline{E} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 31 for the J package) is forced to 12 V. Two identifier bytes are accessed by toggling A0. DQ0–DQ7 contain the valid codes. All other addresses must be held low. The signature code for these devices is 9730. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code 30 (Hex), as shown by the signature mode table below.

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	0	0	1	1	0	0	0	0	30

† $\overline{E} = \overline{G} = V_{IL}$, A9 = V_H, A1–A8 = V_{IL}, A10–A17 = V_{IL}, $V_{PP} = V_{CC}$, $\overline{PGM} = V_{IH}$ or V_{IL}.

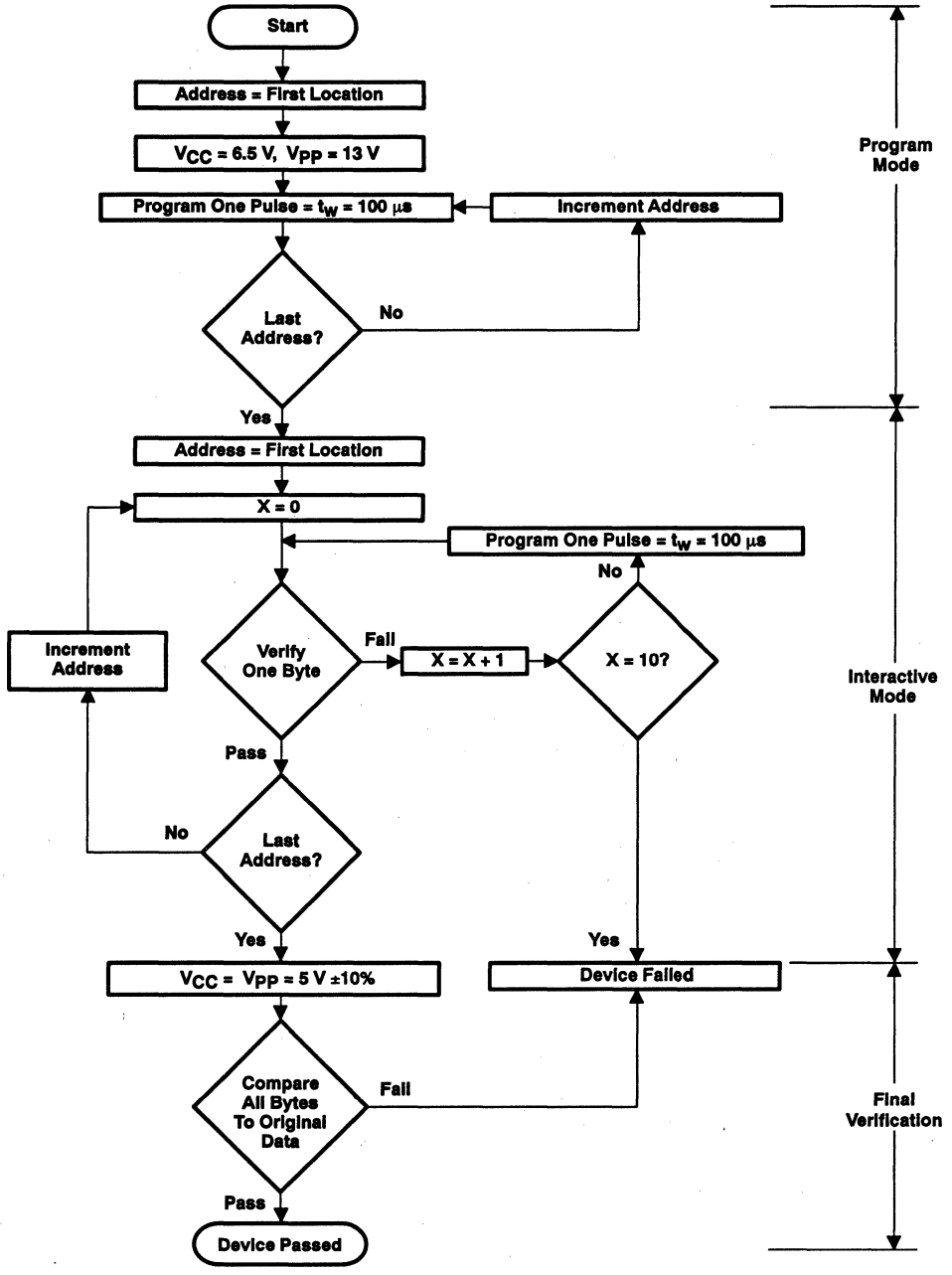
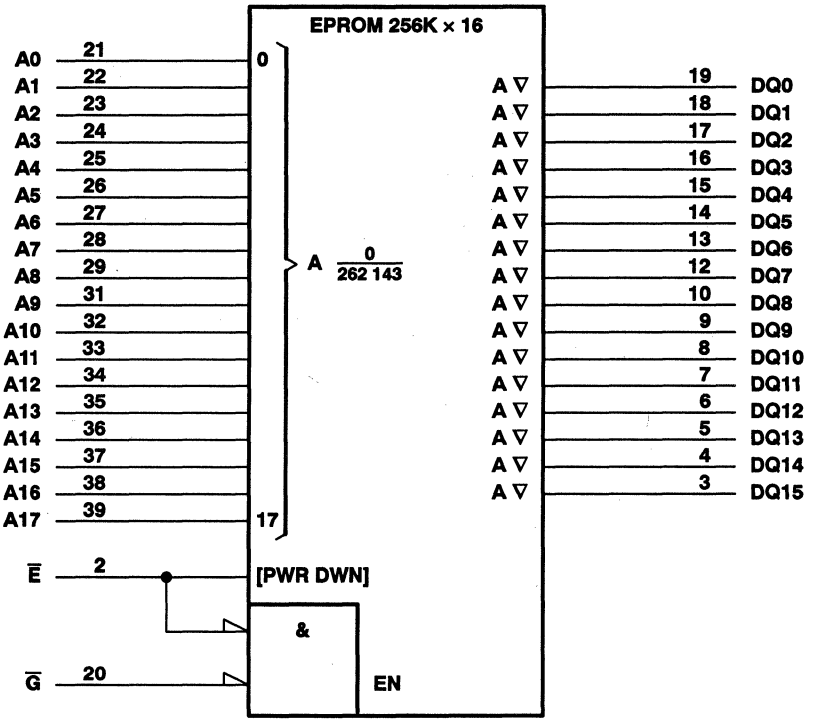


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for the J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 13 V
Input voltage range (see Note 1): All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C240-_ _JL and JL4,
'27PC240-_ _FNL) ..... 0° C to 70° C
Operating free-air temperature range ('27C240-_ _JE and JE4) ..... − 40° C to 85° C
Storage temperature range, T_{stg} ..... −65°C to 150° C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode		$V_{CC}-0.6$		$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	
V_{IH}	High-level dc input voltage		TTL	2		$V_{CC}+0.5$	V
			CMOS	$V_{CC}-0.2$		$V_{CC}+0.5$	
V_{IL}	Low-level dc input voltage		TTL	−0.5		0.8	V
			CMOS	−0.5		0.2	
T_A	Operating free-air temperature		'27C240-__JL, JL4 '27PC240-__FNL	0		70	°C
T_A	Operating free-air temperature		'27C240-__JE, JE4	−40		85	°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level dc output voltage	I_{OH} = −400 μA	2.4		V
		I_{OH} = −20 μA	$V_{CC}-0.1$		
V_{OL}	Low-level dc output voltage	I_{OL} = 2.1 mA		0.4	V
		I_{OL} = 20 μA		0.1	
I_I	Input current (leakage)	V_I = 0 V to 5.5 V		±1	μA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}		±1	μA
I_{PP1}	V_{PP} supply current	$V_{PP} = V_{CC}$ = 5.5 V		10	μA
I_{PP2}	V_{PP} supply current (during program pulse)	V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	V_{CC} = 5.5 V, $\overline{E} = V_{IH}$		1	mA
		V_{CC} = 5.5 V, $\overline{E} = V_{CC}$		100	μA
I_{CC2}	V_{CC} supply current (active)	V_{CC} = 5.5 V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		50	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V		4	8	pF
C_o	Output capacitance	V_O = 0 V		8	12	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended ranges of operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS	'27C240-10 '27PC240-10		'27C240-12 '27PC240-12		'27C240-15 '27PC240-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		50		50	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)
4. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

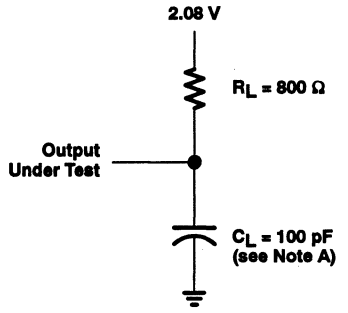
PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0	100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 3)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Pulse duration, program	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Setup time, address		2			µs
$t_{su(E)}$	Setup time, $\overline{E}$		2			µs
$t_{su(G)}$	Setup time, $\overline{G}$		2			µs
$t_{su(D)}$	Setup time, data		2			µs
$t_{su(VPP)}$	Setup time, V_{PP}		2			µs
$t_{su(VCC)}$	Setup time, V_{CC}		2			µs
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs

NOTE 3: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)

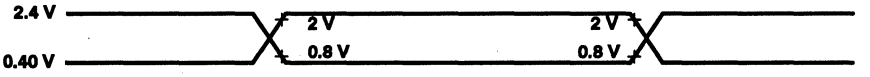
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

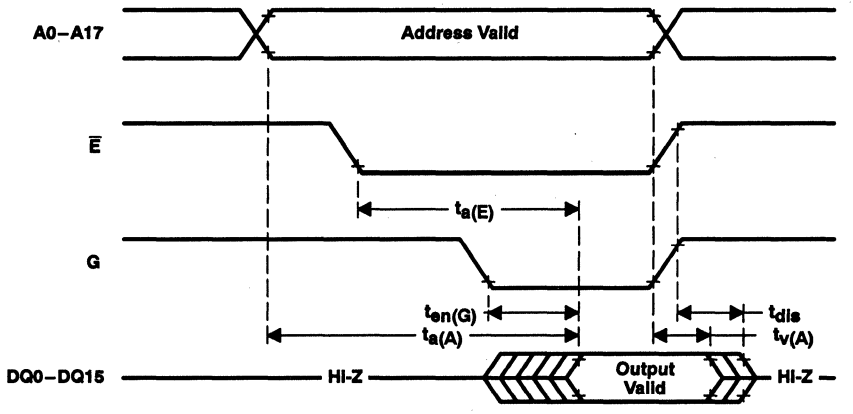
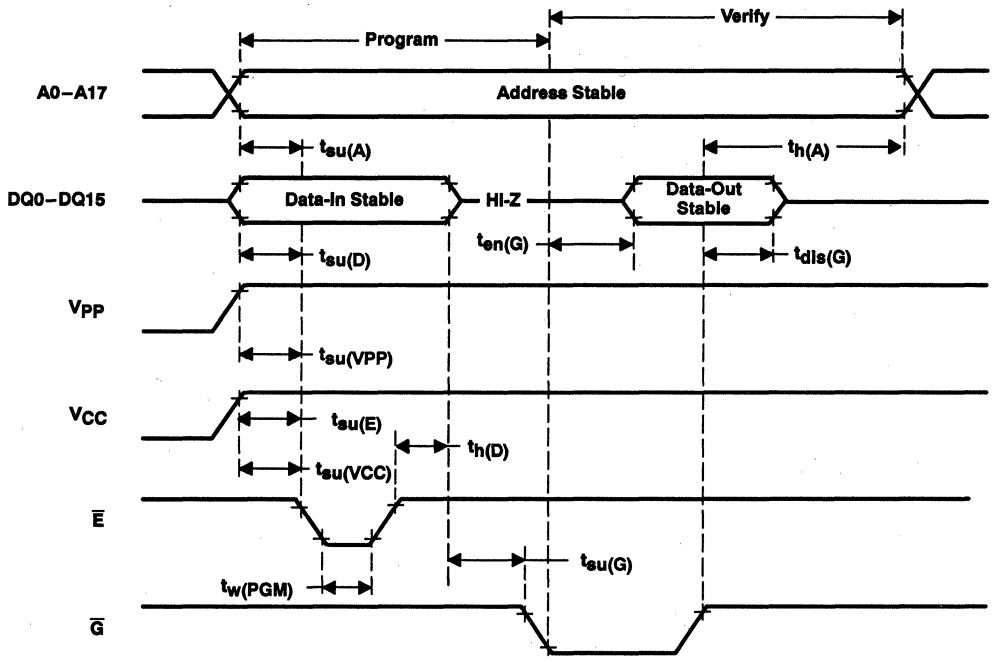


Figure 3. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming

Figure 4. Programming-Cycle Timing (SNAP! Pulse Programming)

Contents

CHAPTER 8. MILITARY PRODUCTS

This section contains Military MOS Memory data sheets.

For additional information on Military devices and availability, please refer to the *Military Selection Guide* (literature number SCYC002), or contact your local TI Field Sales Office.

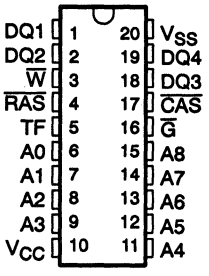
SGMS034C – MAY 1989 – REVISED JUNE 1995

- **Organization . . . 262144 Words × 4 Bits**
- **Single 5-V Supply (10% Tolerance)**
- **Processed to MIL-STD-833, Class B**
- **Performance Ranges:**

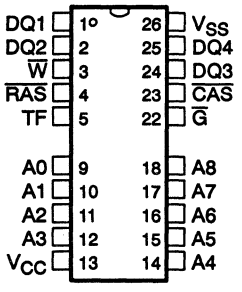
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ44C256-80	80 ns	20 ns	40 ns	150 ns
SMJ44C256-10	100 ns	25 ns	45 ns	190 ns
SMJ44C256-12	120 ns	30 ns	55 ns	220 ns
SMJ44C256-15	150 ns	40 ns	70 ns	260 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  512-Cycle Refresh in 8 ms (Max)
- **All Inputs and Clocks are TTL Compatible**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Packaging Offered:**
  - **20-Pin 300-Mil Ceramic DIP (JD Suffix)**
  - **20-Lead Ceramic Surface-Mount Package (HJ Suffix)**
  - **20-Pin Ceramic Flat Pack (HK Suffix)**
  - **20-Terminal Leadless Ceramic Surface-Mount Package (FQ Suffix)**
  - **20-Terminal Low-Profile Leadless Ceramic Surface-Mount Package (HL Suffix)**
  - **20-Pin Ceramic Zig Zag In-Line Package (SV Suffix)**
- **Operating Free-Air Temperature Range**
  – 55°C to 125°C

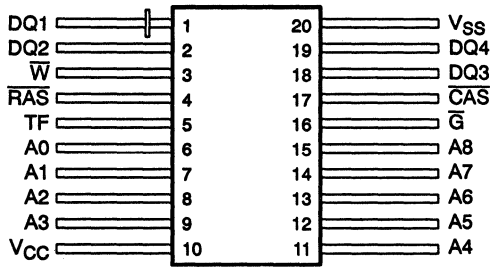
JD PACKAGE
(TOP VIEW)



HJ PACKAGE
(TOP VIEW)

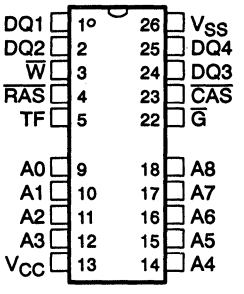


HK PACKAGE
(TOP VIEW)

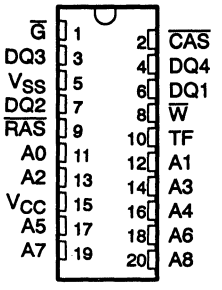


PIN NOMENCLATURE	
A0–A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{G}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
TF	Test Function
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

FQ/HL PACKAGES
(TOP VIEW)



SV PACKAGE
(TOP VIEW)



EPIC is a trademark of Texas Instruments Incorporated.

description

The SMJ44C256 series is a set of high-speed, 1048576-bit dynamic random access memories (DRAMs), organized as 262 144 words of four bits each. These devices employ EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power.

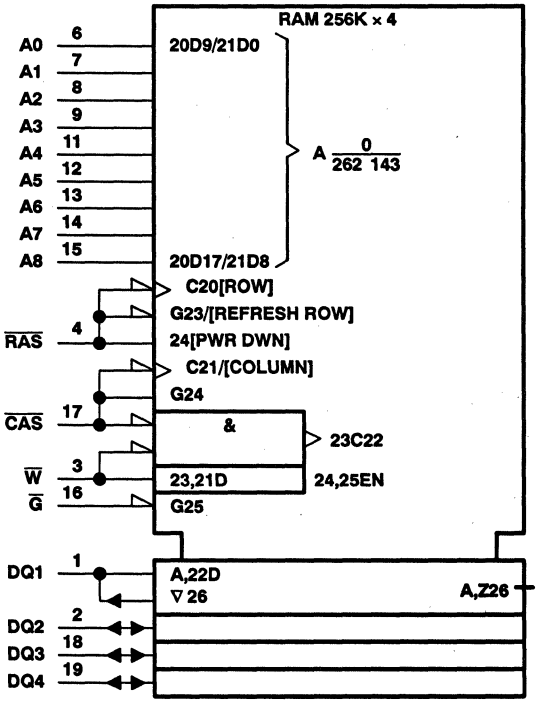
These devices feature maximum $\overline{RAS}$ access times of 80 ns, 100 ns,120 ns, and 150 ns. Maximum power dissipation is as low as 305 mW operating and 16.5 mW standby on 150-ns devices.

The EPIC technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{CC} peaks are 140 mA typical, and an input voltage undershoot of –1 V can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 54/174 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ44C256 is offered in 20-pin ceramic dual-in-line packages (JD suffix) and 20/26-terminal ceramic leadless carriers (FQ/HL suffixes), 20/26-pin leaded carrier (HJ suffix), a 20-pin flatpack (HK suffix), and a 20-pin ceramic zig-zag in-line package (SV suffix). They are specified for operation from –55°C to125°C.

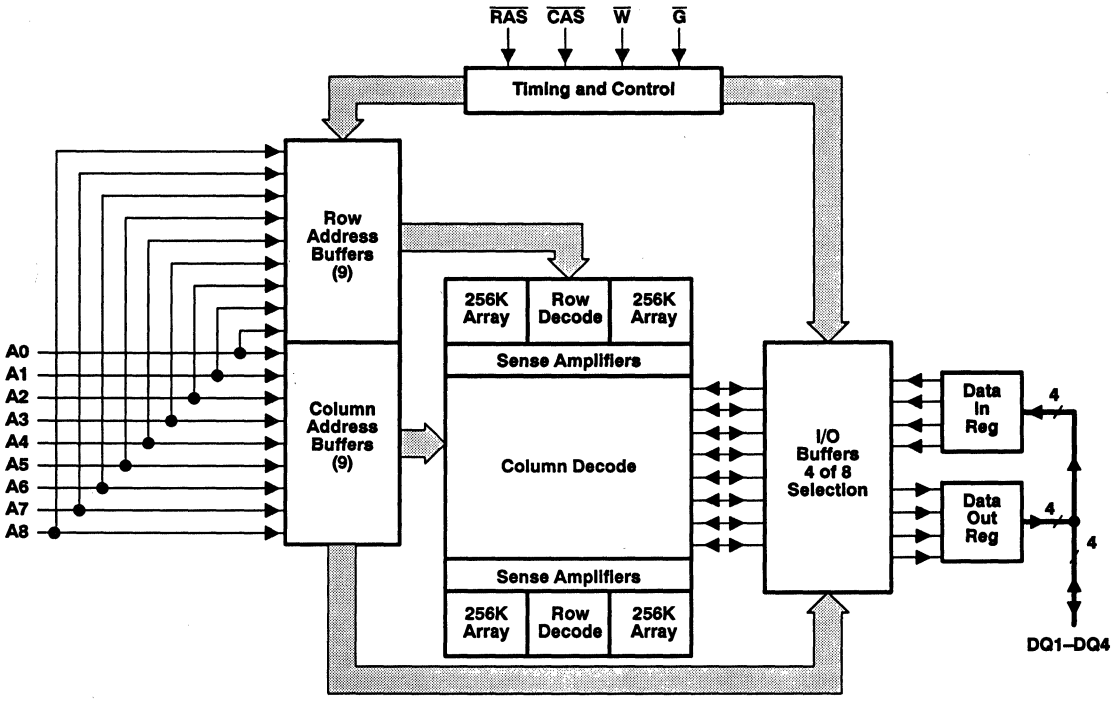
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the JD package.

EPIC is a trademark of Texas Instruments Incorporated.

functional block diagram



operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The column address latches to the first $\overline{CAS}$ falling edge. This feature allows the SMJ44C256 to operate at a wider data bandwidth than conventional page mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ goes low. This performance improvement is referred to as enhanced page mode. Valid column address can be presented immediately after $t_{h(RA)}$ (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ maximum (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ maximum (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by $\overline{RAS}$. Nine column-address bits are set up on pins A0 through A8 and latched onto the chip by $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. In the SMJ44C256, $\overline{CAS}$ is used as a chip select, activating the output buffer as well as latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early-write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{G}$ grounded.

data in (DQ1–DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ is already low, the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to the high-impedance state prior to applying data to the I/O lines.

data out (DQ1–DQ4)

The 3-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{G}$ are brought low. In a read cycle the output becomes valid after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying $t_{d(GHD)}$.

output enable ($\overline{G}$)

$\overline{G}$ controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{G}$ and $\overline{CAS}$ to be brought low for the output buffers, to go into the low-impedance state. Once in the low-impedance state, they remain in the low-impedance state until either $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every 8 ms to retain data. This can be achieved by strobing each of the 512 rows (A0–A8). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

CBR refresh

CBR refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter $t_{d(CLRL)R}$] and holding it low after $\overline{RAS}$ falls [see parameter $t_{d(RLCH)R}$]. For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization (refresh) cycles is required after power-up to the full V_{CC} level.

test function pin

During normal device operation the TF pin must either be disconnected or biased at a voltage less than or equal to V_{CC}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... 0 V to 7 V
Voltage range on any pin (see Note 1) ..... –1 V to 7 V
Short-circuit output current ..... 50 mA
Continuous total power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... –55°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	–55			°C
T_C	Case temperature			125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current	V_{CC} = 5.5 V, $t_{c(rdW)}$ = minimum		80		70		60		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		3		3		3		3	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only, or CBR)	V_{CC} = 5.5 V, $t_{c(rdW)}$ = minimum, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		75		65		55		50	mA
I_{CC4}	Average page current	V_{CC} = 5.5 V, $\overline{RAS}$ low, $t_{c(P)}$ = minimum, $\overline{CAS}$ cycling		50		45		35		30	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		HL/JD/FQ		HJ		HK		SV		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		6		7		8		9	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7		7		8		8	pF
$C_{i(W)}$	Input capacitance, write-enable input		7		7		7		7	pF
C_O	Output capacitance		7		9		10		8	pF

NOTE 3: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25°C with a 1-MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER		ALT. SYMBOL	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		20		25		30		40	ns
$t_{a(CA)}$	Access time from column-address	t_{AA}		40		45		55		70	ns
$t_{a(RL)}$	Access time from $\overline{RAS}$ low	t_{RAC}		80		100		120		150	ns
$t_{a(G)}$	Access time from $\overline{G}$ low	t_{GAC}		20		25		30		40	ns
$t_{a(CP)}$	Access time from $\overline{CAS}$ high column precharge	t_{CPA}		40		50		60		75	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}		20		25		30		35	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high (see Note 4)	t_{GOFF}		20		25		30		35	ns

NOTE 4: $t_{dis(CH)}$ and $t_{dis(G)}$ are specified when the output is no longer driven. The outputs are disabled by bringing either $\overline{G}$ or $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

PARAMETER		ALT. SYMBOL	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Cycle time, read (see Note 6)	t_{RC}	150		190		220		260		ns
$t_{c(W)}$	Cycle time, write	t_{WC}	150		190		220		260		ns
$t_{c(rdW)}$	Cycle time,read-write/read-modify-write	t_{RWC}	225		270		305		355		ns
$t_{c(P)}$	Cycle time, page-mode read or write (see Note 7)	t_{PC}	50		55		65		80		ns
$t_{c(PM)}$	Cycle time, page-mode read-modify-write	t_{PRWC}	115		135		150		175		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	10 000	25	10 000	30	10 000	40	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	60		80		90		100		ns
$t_{w(RL)}$	Pulse duration, nonpage mode $\overline{RAS}$ low (see Note 9)	t_{RAS}	80	10 000	100	10 000	120	10 000	150	10 000	ns
$t_{w(RL)P}$	Pulse duration, page mode $\overline{RAS}$ low (see Note 9)	t_{RASP}	80	100 000	100	100 000	120	100 000	150	100 000	ns
$t_{w(WL)}$	Pulse duration, write low	t_{WP}	15		15		20		25		ns
$t_{su(CA)}$	Setup time, column address before $\overline{CAS}$ low	t_{ASC}	5		5		5		5		ns

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To assure $t_{c(P)}$ min, $t_{su(CA)}$ should be ≥ $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this can require additional $\overline{CAS}$ low time [$t_{w(CL)}$].
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this can require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating temperature (continued) (see Note 5)

PARAMETER		ALT. SYMBOL	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low	t_{ASR}	0		0		0		0		ns
$t_{su(D)}$	Setup time, data before $\overline{W}$ low (see Note 10)	t_{DS}	0		0		0		0		ns
$t_{su(rd)}$	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	t_{RCS}	0		0		0		0		ns
$t_{su(WCL)}$	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		0		ns
$t_{su(WCH)}$	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	t_{CWL}	20		25		30		40		ns
$t_{su(WRH)}$	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	t_{RWL}	20		25		30		40		ns
$t_{h(CA)}$	Hold time, column address after $\overline{CAS}$ low (see Note 10)	t_{CAH}	15		20		20		25		ns
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low	t_{RAH}	15		15		15		15		ns
$t_{h(RLCA)}$	Hold time, column address after $\overline{RAS}$ low (see Note 12)	t_{AR}	60		70		80		100		ns
$t_{h(D)}$	Hold time, data after $\overline{CAS}$ low (see Note 10)	t_{DH}	15		20		25		30		ns
$t_{h(RLD)}$	Hold time, data after $\overline{RAS}$ low (see Note 12)	t_{DHR}	60		70		85		110		ns
$t_{h(WLGL)}$	Hold time, $\overline{G}$ high after $\overline{W}$ low	t_{GH}	20		25		30		40		ns
$t_{h(CHrd)}$	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 14)	t_{RCH}	0		0		0		0		ns
$t_{h(RHrd)}$	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 14)	t_{RRH}	10		10		10		10		ns
$t_{h(CLW)}$	Hold time, $\overline{W}$ low after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		20		25		30		ns
$t_{h(RLW)}$	Hold time, $\overline{W}$ low after $\overline{RAS}$ low (see Note 12)	t_{WCR}	65		75		90		105		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	80		100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 15)	t_{CWD}	60		70		80		90		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)	t_{RCD}	30	60	30	75	30	90	30	110	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 13)	t_{RAD}	20	40	20	55	20	65	25	80	ns

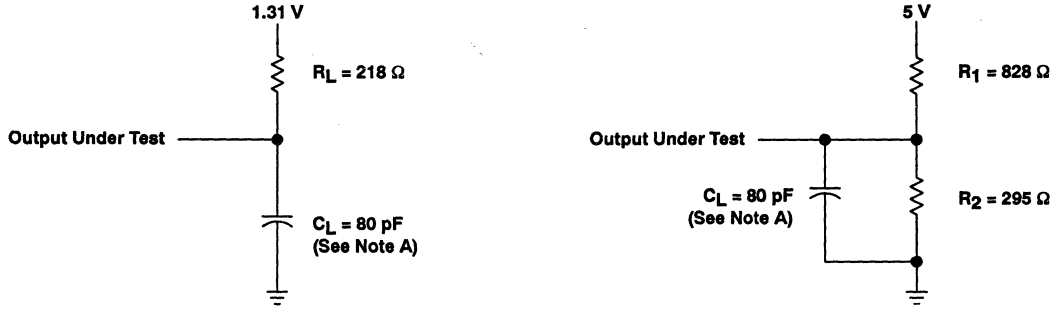
NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early-write operation only
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Maximum value specified only to assure access time.
14. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
15. Read-modify-write operation only

timing requirements over recommended ranges of supply voltage and operating temperature (continued) (see Note 5)

PARAMETER		ALT. SYMBOL	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	40		45		55		70		ns
$t_{d(CACH)}$	Delay time, column address to $\overline{CAS}$ high	t_{CAL}	40		45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 15)	t_{RWD}	130		150		170		200		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 15)	t_{AWD}	80		95		105		120		ns
$t_{d(GHD)}$	Delay time, $\overline{G}$ high before data at DQ	t_{GDD}	20		25		30		40		ns
$t_{d(GLRH)}$	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	t_{GSR}	20		25		30		40		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	20		25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		10		15		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8		8	ms
t_t	Transition time (see Note 17)	t_T									ns

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
15. Read-modify-write operation only
16. CBR refresh only
17. System transition times (rise and fall) are to be a minimum of 3 ns and a maximum of 50 ns.

PARAMETER MEASUREMENT INFORMATION



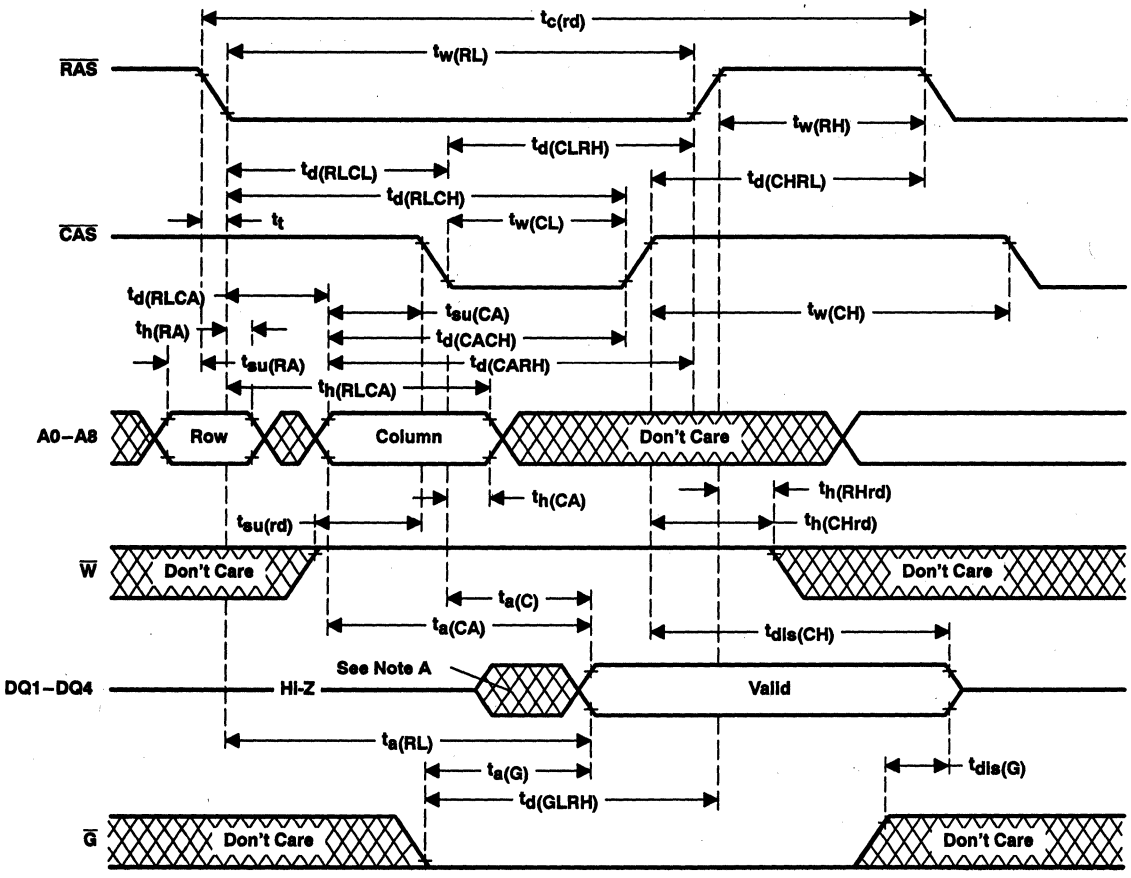
(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

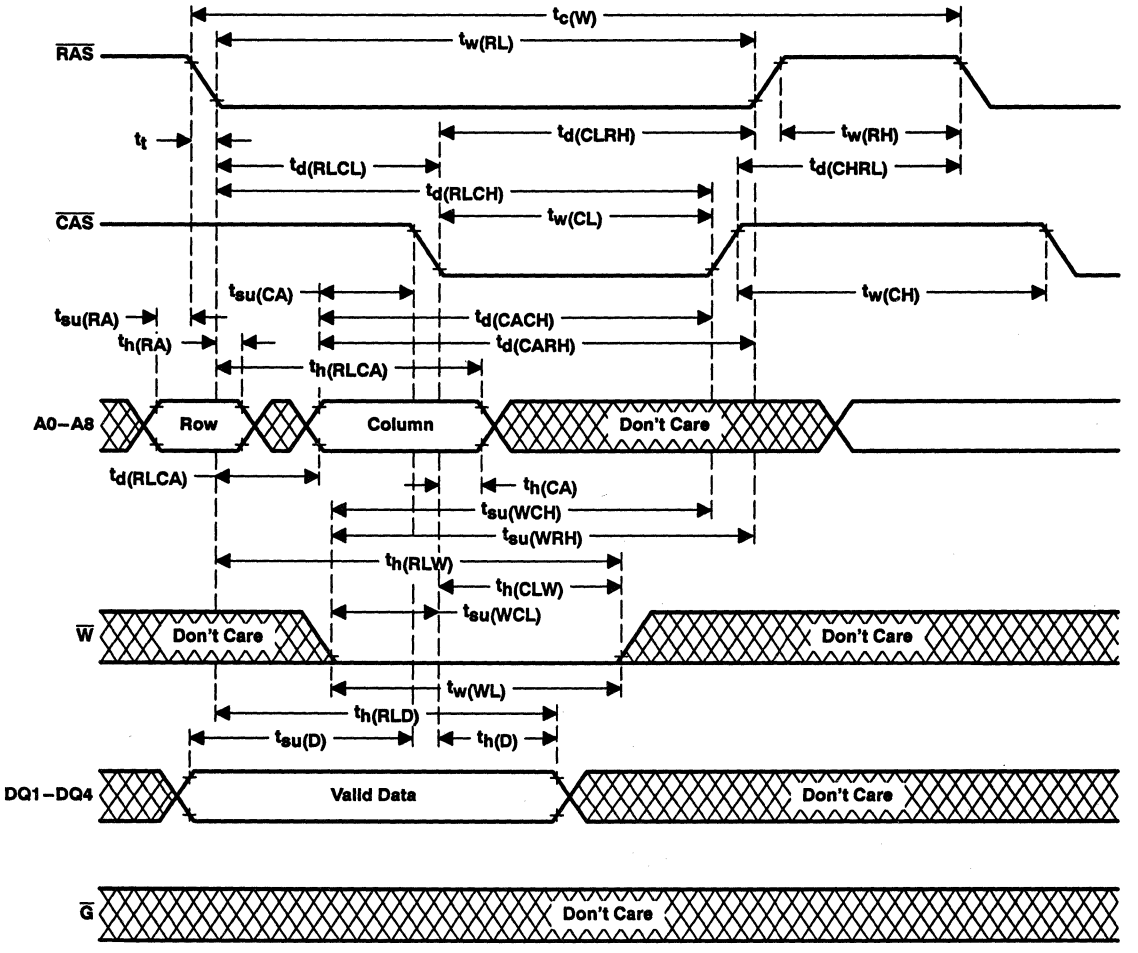


Figure 3. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

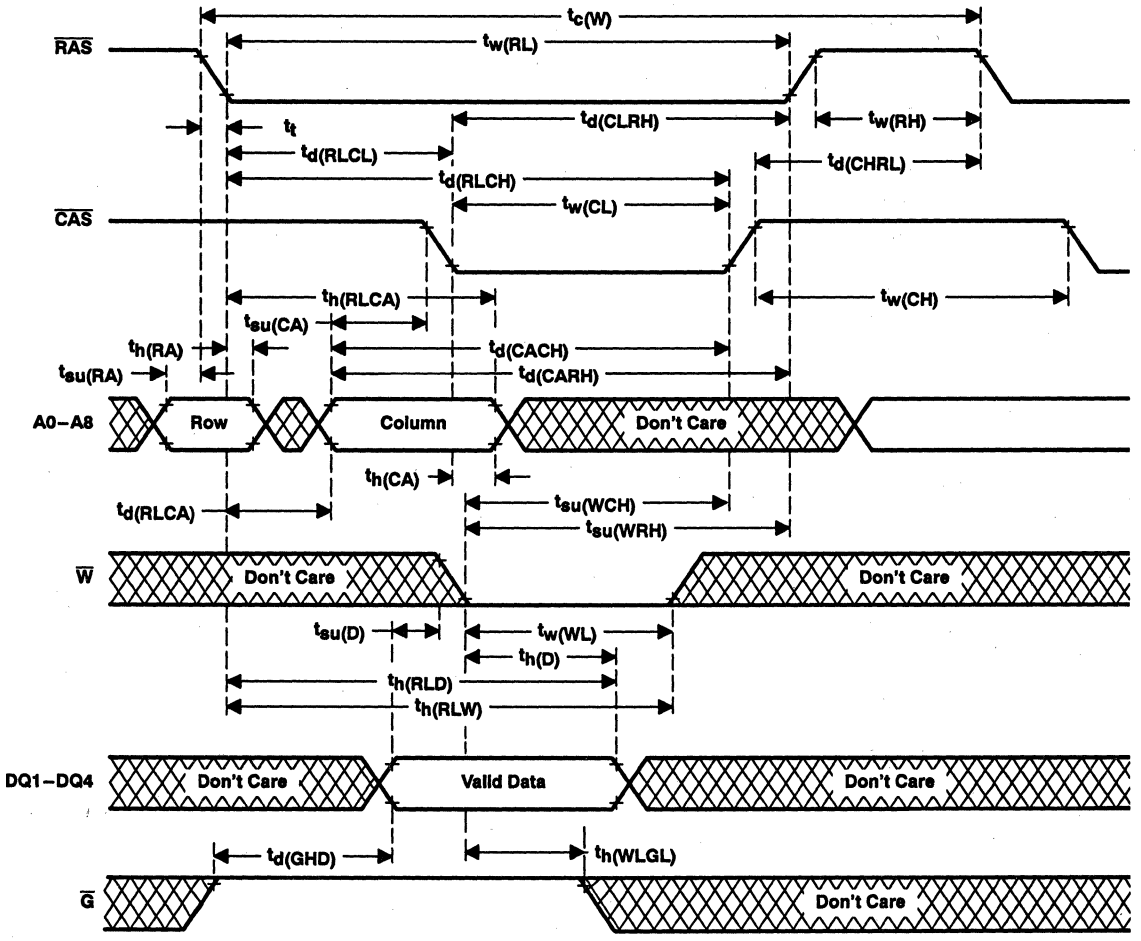
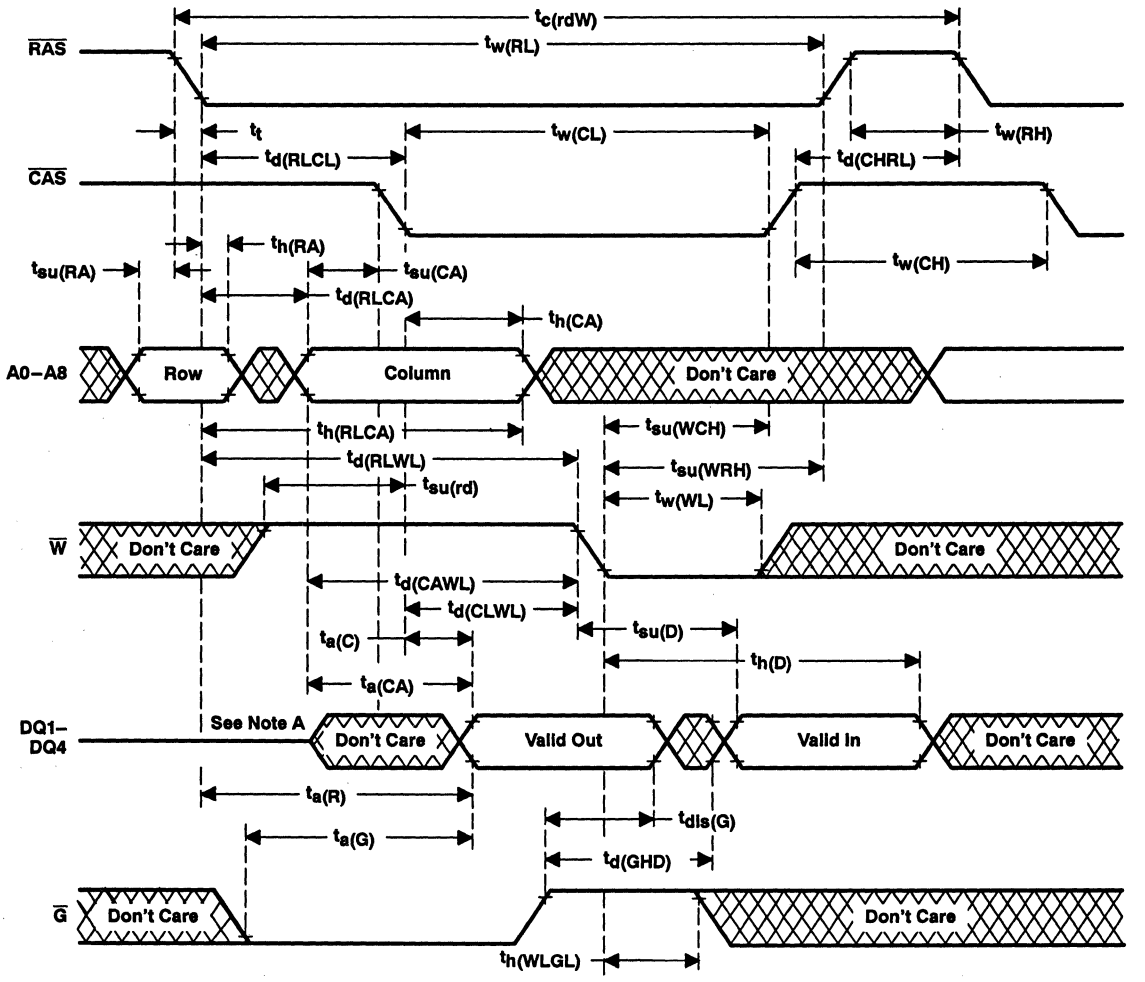


Figure 4. Write-Cycle Timing

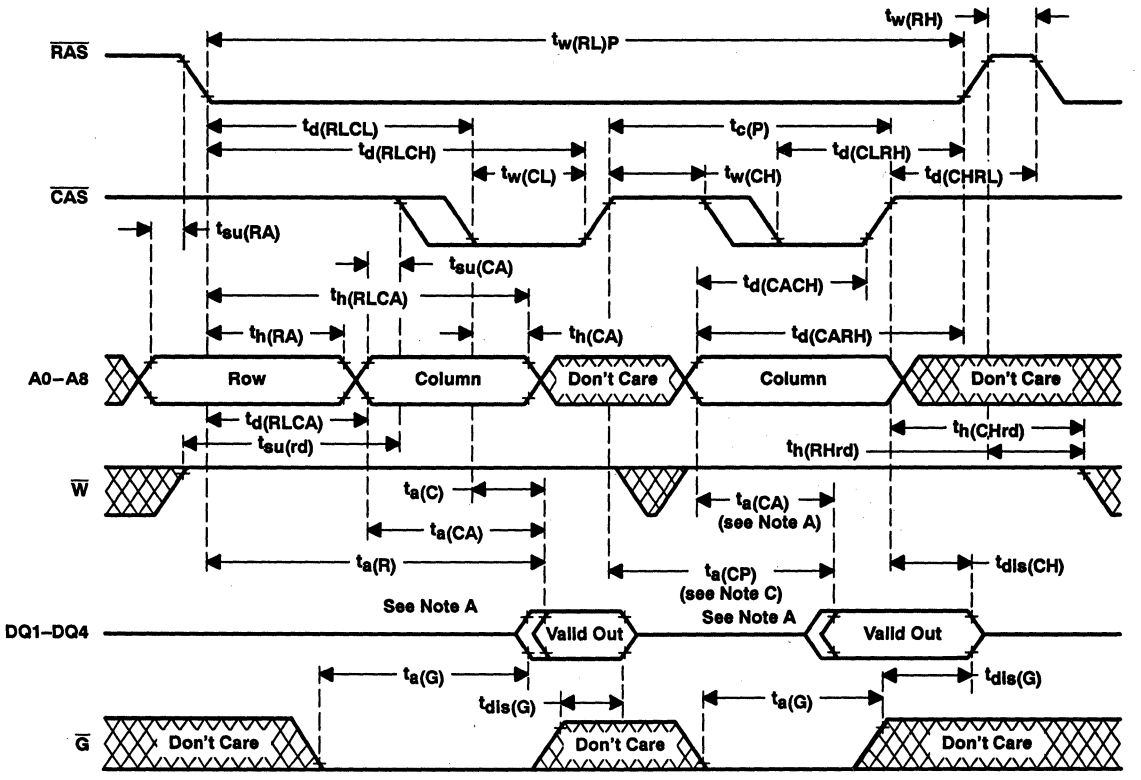
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 5. Read-Write-/Read-Modify-Write-Cycle Timing

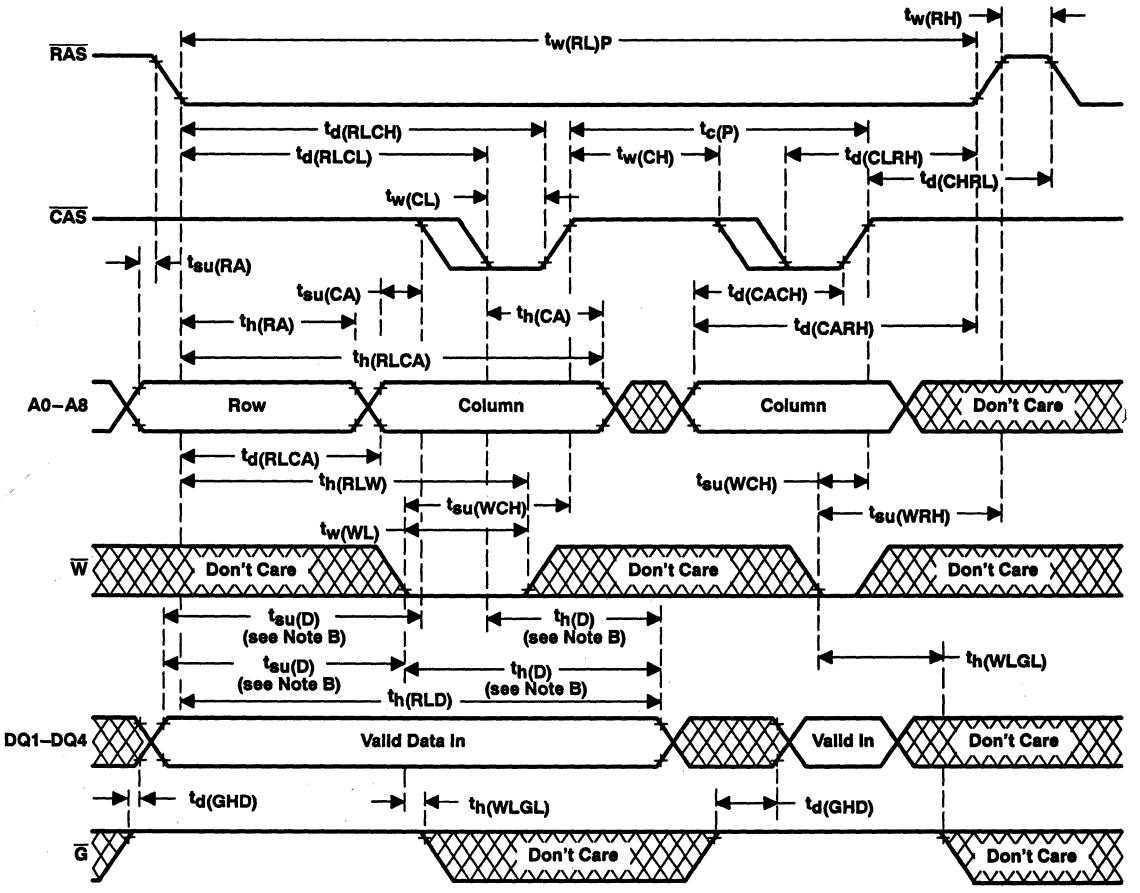
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A write-cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
C. Access time is $t_{a(CP)}$- or $t_{a(CA)}$-dependent.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

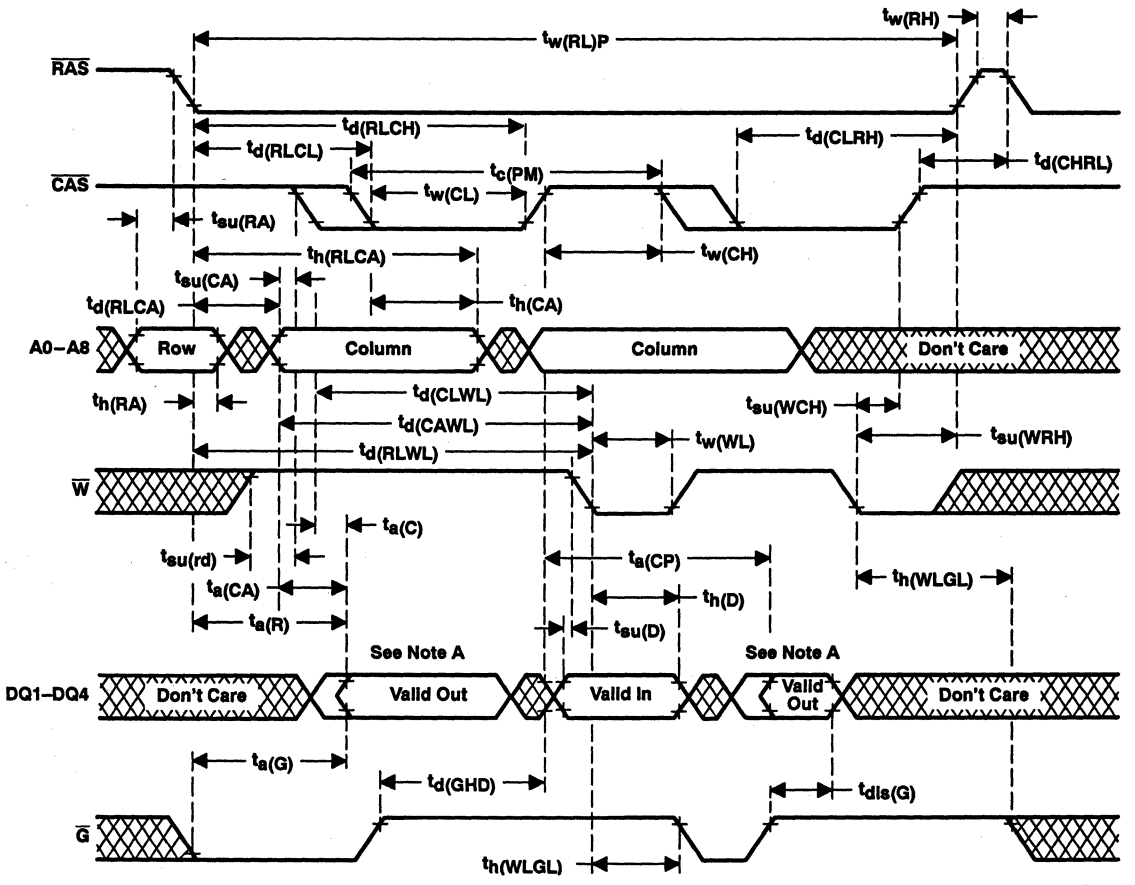
PARAMETER MEASUREMENT INFORMATION



NOTES: A. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.
B. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing (see Note A)

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing (see Note B)

PARAMETER MEASUREMENT INFORMATION

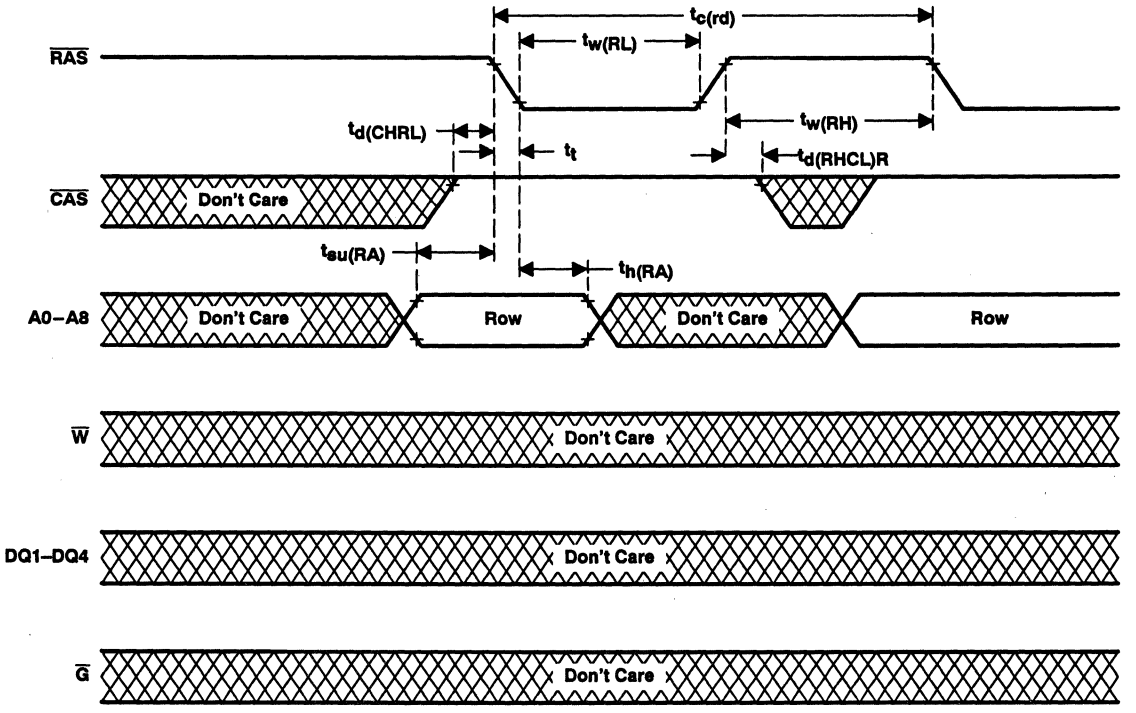


Figure 9. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

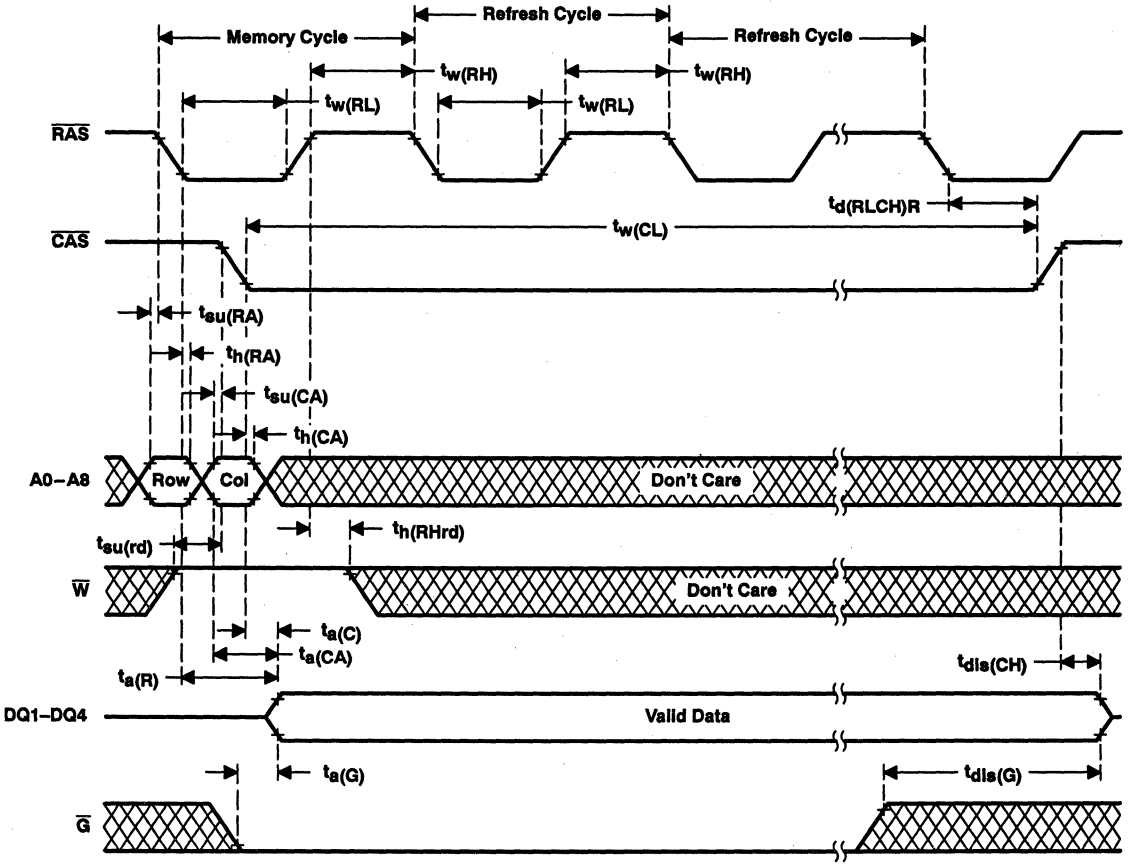


Figure 10. Hidden-Refresh-Cycle (Enhanced Page Mode) Timing

PARAMETER MEASUREMENT INFORMATION

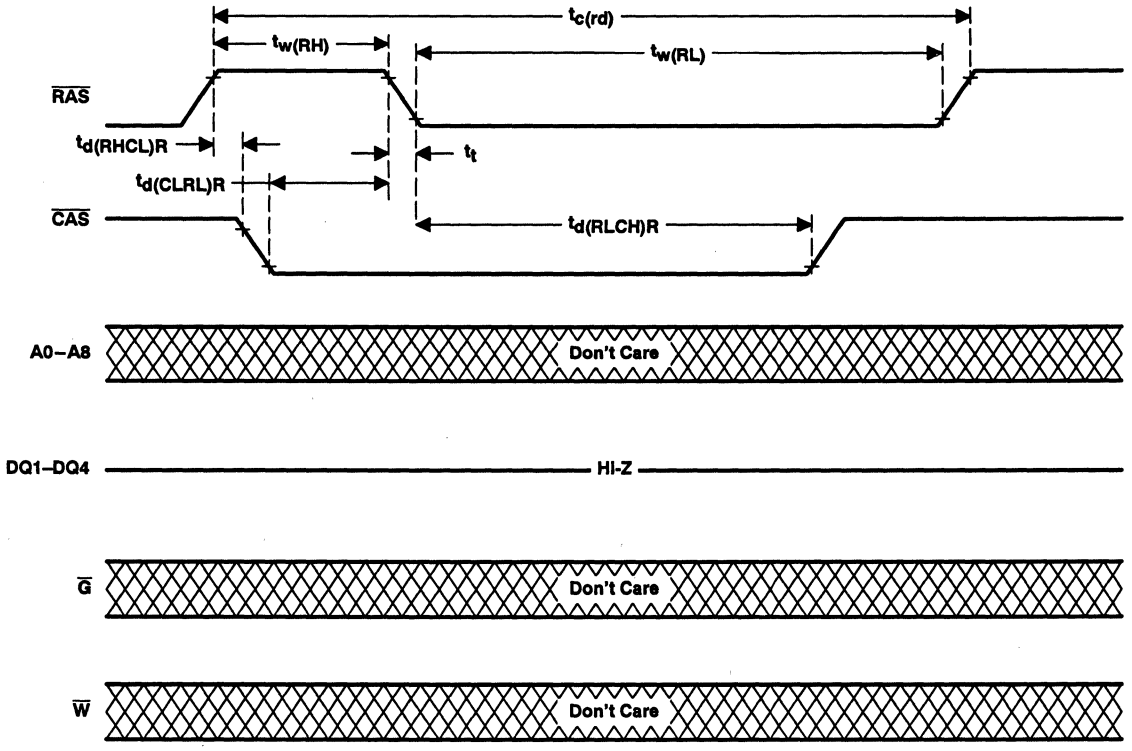


Figure 11. Automatic CBR Refresh-Cycle Timing

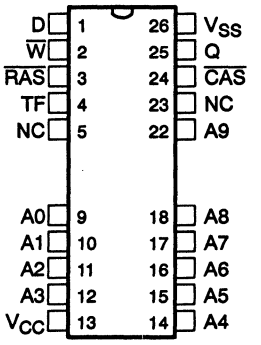
SGMS023D – DECEMBER 1988 – REVISED JUNE 1995

- **Organization . . . 1 048 576 × 1**
- **Processed to MIL-STD-883, Class B**
- **Single 5-V Supply (10% Tolerance)**
- **Performance Ranges:**

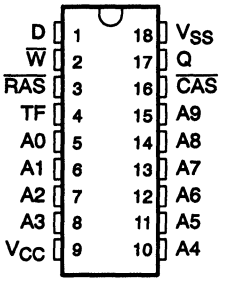
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
'4C1024-80	80 ns	20 ns	40 ns	150 ns
'4C1024-10	100 ns	25 ns	45 ns	190 ns
'4C1024-12	120 ns	30 ns	55 ns	220 ns
'4C1024-15	150 ns	40 ns	70 ns	260 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
  - **Higher Data Bandwidth Than Conventional Page Mode Parts**
  - **Random Single-Bit Access Within a Row With a Column Address**
- **One of TI's CMOS Megabit DRAM Family Including SMJ44C256 — 256K × 4 Enhanced Page Mode**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  512-Cycle Refresh in 8 ms (Max)
- **3-State Unlatched Output**
- **Low-Power Dissipation**
- **Texas Instruments EPIC™ Process**
- **All Inputs/Outputs and Clocks Are TTL-Compatible**
- **Packaging Offered:**
  - **20/26-Lead Ceramic Surface Mount Package (HJ Suffix)**
  - **18-Pin 300-Mil Ceramic DIP (JD Suffix)**
  - **20-Pin Ceramic Flat Pack (HK Suffix)**
  - **20/26-Terminal Leadless Ceramic Surface Mount Package (FQ/HL Suffixes)**
  - **20-Pin Ceramic Zig-Zag In-Line Package (SV Suffix)**
- **Operating Temperature Range**
  – 55°C to 125°C

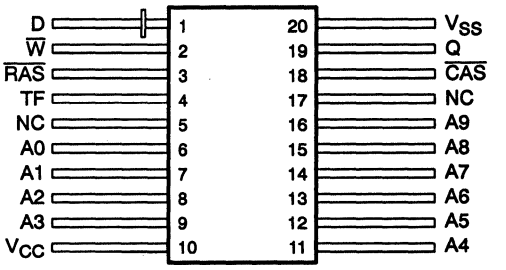
HJ PACKAGE
(TOP VIEW)



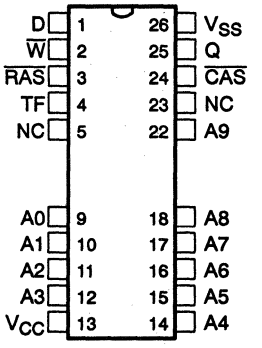
JD PACKAGE
(TOP VIEW)



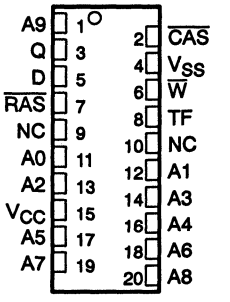
HK PACKAGE
(TOP VIEW)



FQ/HL PACKAGES
(TOP VIEW)



SV PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS}$	Column Address Strobe
D	Data In
NC	No Internal Connection
Q	Data Out
$\overline{RAS}$	Row Address Strobe
TF	Test Function
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

EPIC is a trademark of Texas Instruments Incorporated.

description

The SMJ4C1024 is a high-speed, 1 048 576-bit dynamic random-access memory (RAM) organized as 1 048 576 words of one bit each. It employs enhanced performance implanted CMOS (EPIC™) technology for high performance, reliability, and low power at a low cost.

This device features maximum $\overline{RAS}$ access times of 80 ns, 100 ns, 120 ns, and 150 ns. Maximum power dissipation is as low as 305 mW operating and 16.5 mW standby on 150 ns devices.

The EPIC™ technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 140 mA typical, and a –1 V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ4C1024 is offered in an 18-pin ceramic dual-in-line package (JD suffix), a 20/26-terminal ceramic leadless carrier package (FQ/HL suffixes), a 20/26-pin leaded carrier package (HJ suffix), a 20-pin flatpack (HK suffix), and a 20-pin ceramic zig-zag in-line package (SV suffix). They are characterized for operation from – 55°C to 125°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row address setup and hold and address multiplexing is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature lets the SMJ4C1024 operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ goes low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after the row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ maximum (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ maximum (access time from column address) has been satisfied. If the column addresses for the next page cycle are valid at the same time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

address (A0–A9)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by $\overline{RAS}$. The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select to activate the output buffer as well as latch the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on the $\overline{W}$ input selects the read mode, and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data-in is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$, and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ is already low, and the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The 3-state output buffers provide direct TTL compatibility (no pullup resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time $t_{a(C)}$. $t_{a(C)}$ begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; when $\overline{CAS}$ goes high, the output returns to a high-impedance state. In a delayed-write or read-modify-write cycle, the output follows the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every 8 ms to retain data. This can be achieved by strobing each of the 512 rows (A0–A8). A normal read or write cycle refreshes all bits in each selected row. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refresh is used by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter $t_{d(CLRL)R}$) and holding it low after $\overline{RAS}$ falls (parameter $t_{d(RLCH)R}$). For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh cycles.

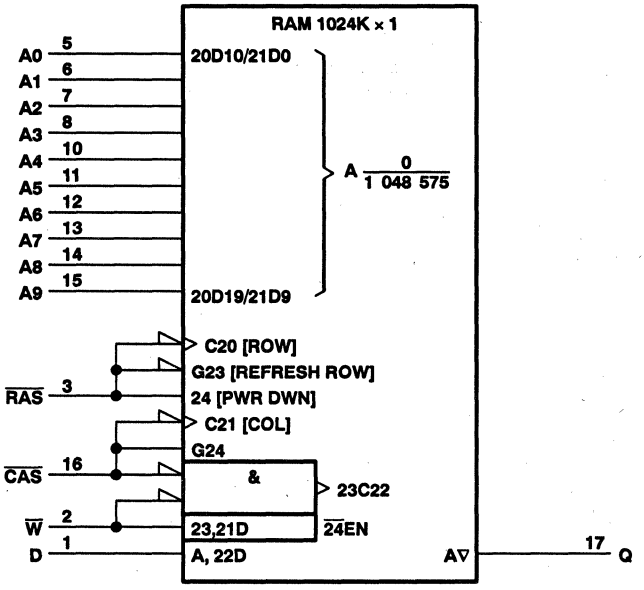
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved.

test function pin

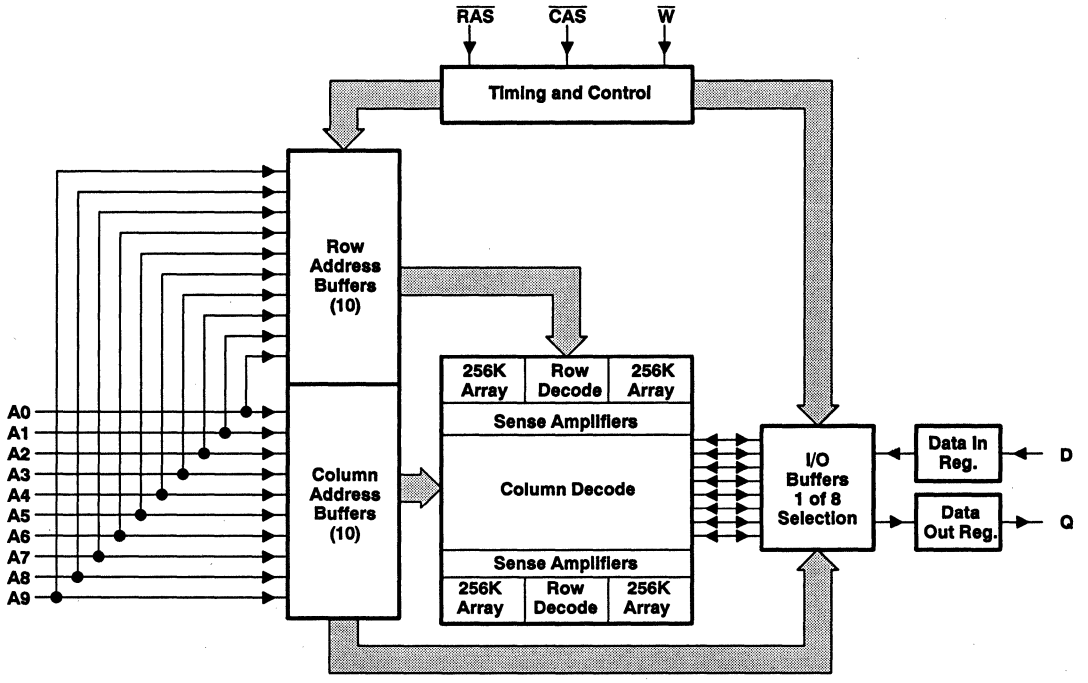
During normal device operation TF must be disconnected or biased at a voltage less than or equal to V_{CC}.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 18-pin JD package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short-circuit output current, I_{OS} ..... 50 mA
Power dissipation ..... 1 W
Operating temperature range, T_A ..... – 55°C to 125°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Minimum operating free-air temperature	– 55			°C
T_C	Maximum operating case temperature			125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'4C1024-80		'4C1024-10		'4C1024-12		'4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		75		70		60		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		3		3		3		3	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		70		65		55		50	mA
I_{CC4}	Average page current	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		45		35		30	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		HL/JD/FQ		HJ		HK		SV		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		6		7		8		9	pF
$C_{i(D)}$	Input capacitance, data input		5		5		6		7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7		7		8		8	pF
$C_{i(W)}$	Input capacitance, write-enable input		7		7		7		7	pF
C_o	Output capacitance		7		9		10		8	pF

NOTE 3: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25°C with a 1 MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER		ALT. SYMBOL	'4C1024-80		'4C1024-10		'4C1024-12		'4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		20		25		30		40	ns
$t_{t(CA)}$	Access time from column address	t_{AA}		40		45		55		70	ns
$t_{t(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}		80		100		120		150	ns
$t_{a(CP)}$	Access time from column precharge	t_{CPA}		40		40		60		75	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}		20		25		30		35	ns

NOTE 4: $t_{dis(CH)}$ is specified when the output is no longer driven. The output is disabled by bringing $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

PARAMETER		ALT. SYMBOL	'4C1024-80		'4C1024-10		'4C1024-12		'4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Cycle time, read (see Note 6)	t_{RC}	150		190		220		260		ns
$t_{c(W)}$	Cycle time, write	t_{WC}	150		190		220		260		ns
$t_{c(rdW)}$	Cycle time, read-write/read-modify-write	t_{RWC}	175		220		265		315		ns
t_c	Cycle time, page-mode read or write (see Note 7)	t_{PC}	50		55		65		80		ns
$t_{c(PM)}$	Cycle time, page-mode read-modify-write	t_{PRWC}	75		85		110		135		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	10000	25	10000	30	10000	40	10000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	60		80		90		100		ns
$t_{w(RL)}$	Pulse duration, nonpage mode, $\overline{RAS}$ low (see Note 9)	t_{RAS}	80	10000	100	10000	120	10000	150	10000	ns
$t_{w(RL)P}$	Pulse duration, page mode, $\overline{RAS}$ low (see Note 9)	t_{RASP}	80	100000	100	100000	120	100000	150	100000	ns
$t_{w(WL)}$	Pulse duration, write	t_{WP}	15		15		20		25		ns
$t_{su(CA)}$	Setup time, column address before $\overline{CAS}$ low	t_{ASC}	0		3		3		3		ns
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low	t_{ASR}	0		0		0		0		ns
$t_{su(D)}$	Setup time, data (see Note 10)	t_{DS}	0		0		0		0		ns
$t_{su(rd)}$	Setup time, read before $\overline{CAS}$ low	t_{RCS}	0		0		0		0		ns
$t_{su(WCL)}$	Setup time, W low before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		0		ns
$t_{su(WCH)}$	Setup time, W low before $\overline{CAS}$ high	t_{CWL}	20		25		30		40		ns
$t_{su(WRH)}$	Setup time, W low before $\overline{RAS}$ high	t_{RWL}	20		25		30		40		ns
$t_{h(CA)}$	Hold time, column address after $\overline{CAS}$ low	t_{CAH}	15		20		20		25		ns
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low	t_{RAH}	12		15		15		20		ns

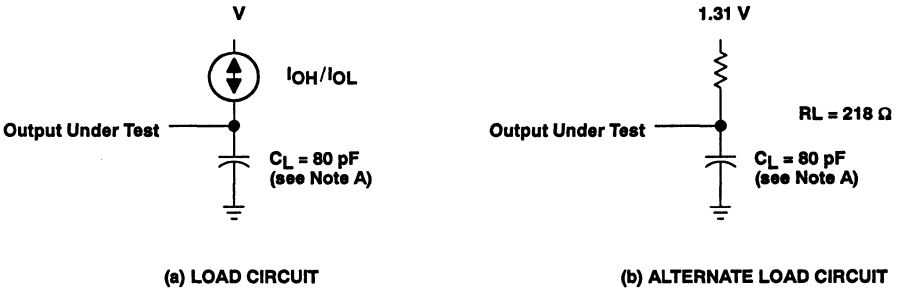
NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To assure $t_{c(P)}$ min, $t_{su(CA)}$ should be ≥ $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
11. Early write operation only

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5) (continued)

PARAMETER		ALT. SYMBOL	'4C1024-80		'4C1024-10		'4C1024-12		'4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(RCLA)}$	Hold time, column address after $\overline{RAS}$ low (see Note 12)	t_{AR}	60		70		80		100		ns
$t_{h(D)}$	Hold time, data (see Note 10)	t_{DH}	15		20		25		30		ns
$t_{h(RLD)}$	Hold time, data after $\overline{RAS}$ low (see Note 12)	t_{DHR}	60		70		85		110		ns
$t_{h(CHrd)}$	Hold time, read after $\overline{CAS}$ high (see Note 15)	t_{RCH}	0		0		0		0		ns
$t_{h(RHrd)}$	Hold time, read after $\overline{RAS}$ high (see Note 15)	t_{RRH}	10		10		10		10		ns
$t_{h(CLW)}$	Hold time, write after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		20		25		30		ns
$t_{h(RLW)}$	Hold time, write after $\overline{RAS}$ low (see Note 12)	t_{WCR}	60		70		85		100		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	80		100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 13)	t_{CWD}	20		25		40		50		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	22	60	28	75	28	90	33	110	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 14)	t_{RAD}	17	40	20	55	20	65	25	80	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	40		45		55		70		ns
$t_{d(CACH)}$	Delay time, column address to $\overline{CAS}$ high	t_{CAL}	40		45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	80		100		130		160		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 13)	t_{AWD}	40		45		65		80		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	20		25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		10		15		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8		8	ms
t_t	Transition time (see Note 17)	—	—		—		—		—		ns

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early-write operation only
12. The minimum value is measured when $t_{d(RLCL)}$ is set $t_{d(RLCL)}$ min as a reference.
13. Read-modify-write operation only
14. Maximum value specified only to assure access time.
15. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
16. CBR refresh only
17. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and a maximum of 50 ns.

PARAMETER MEASUREMENT INFORMATION



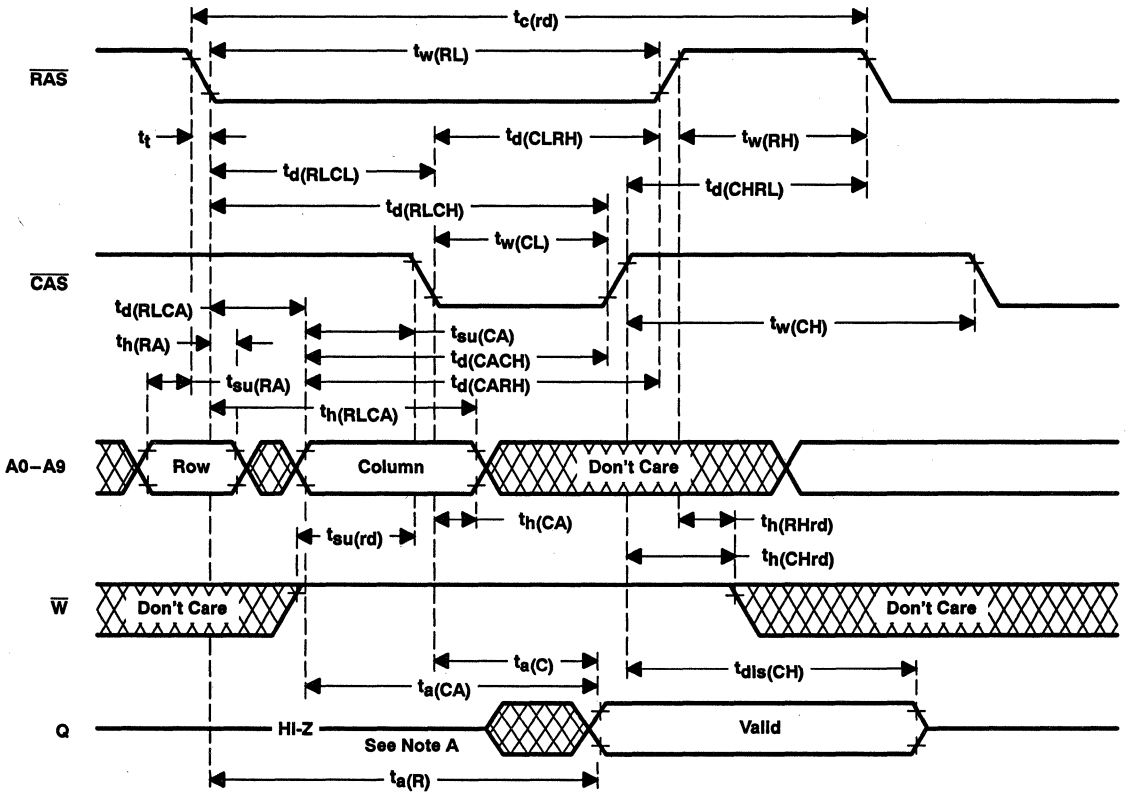
(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

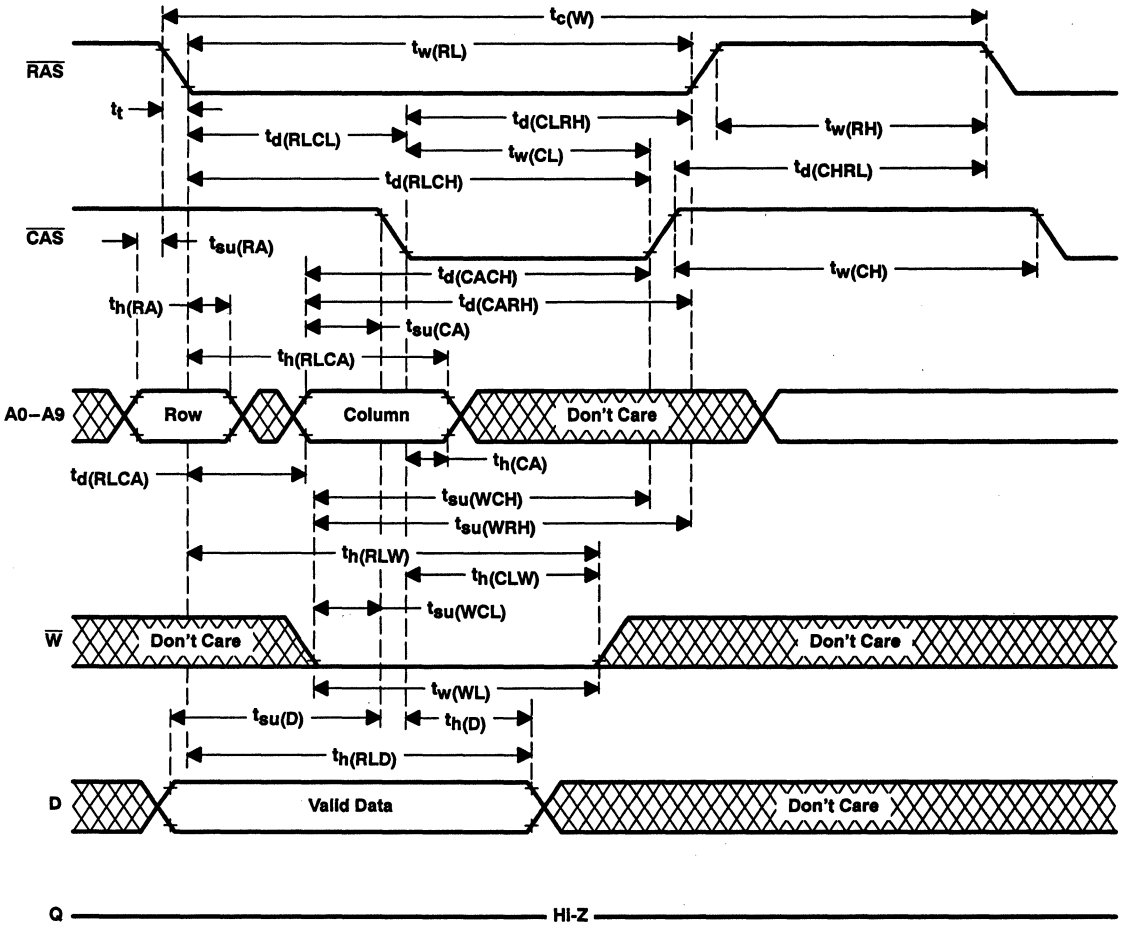


Figure 3. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

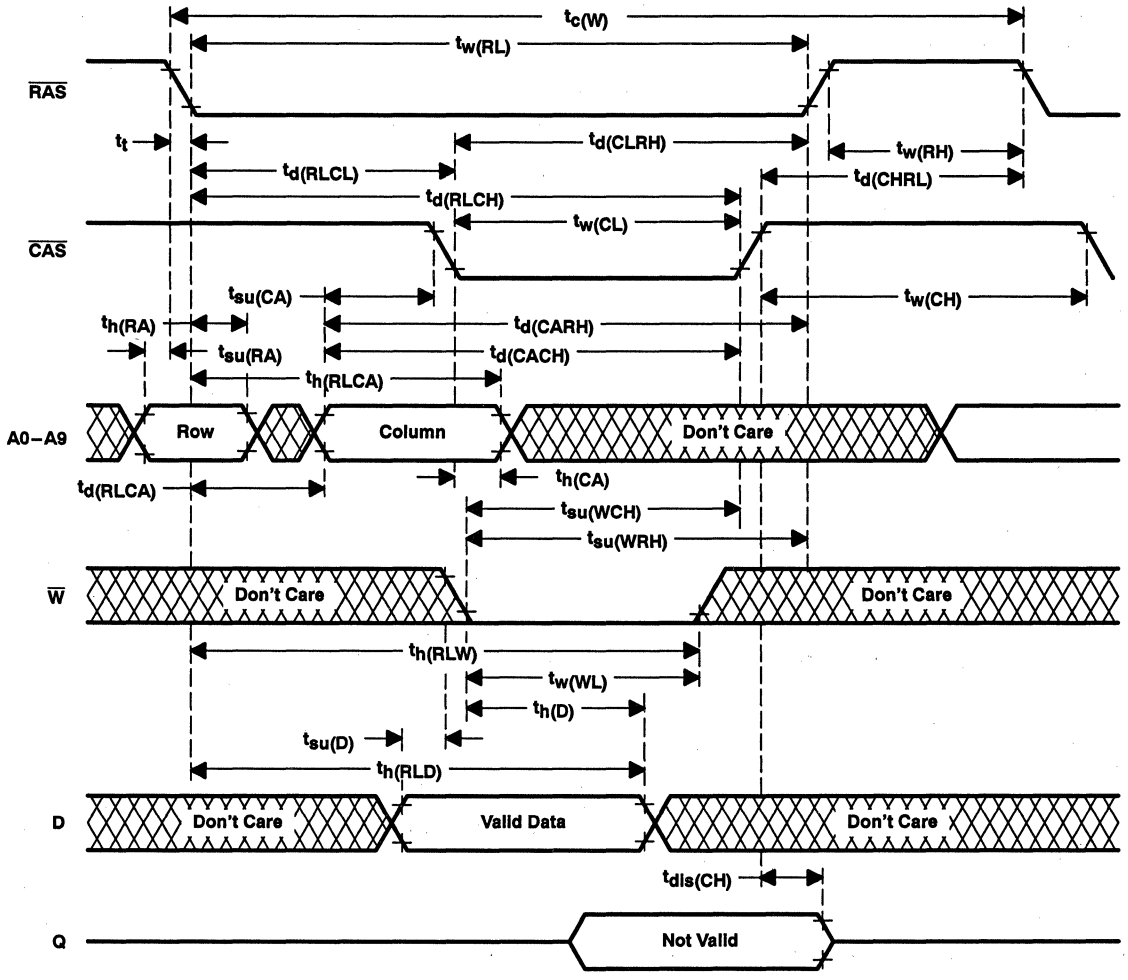
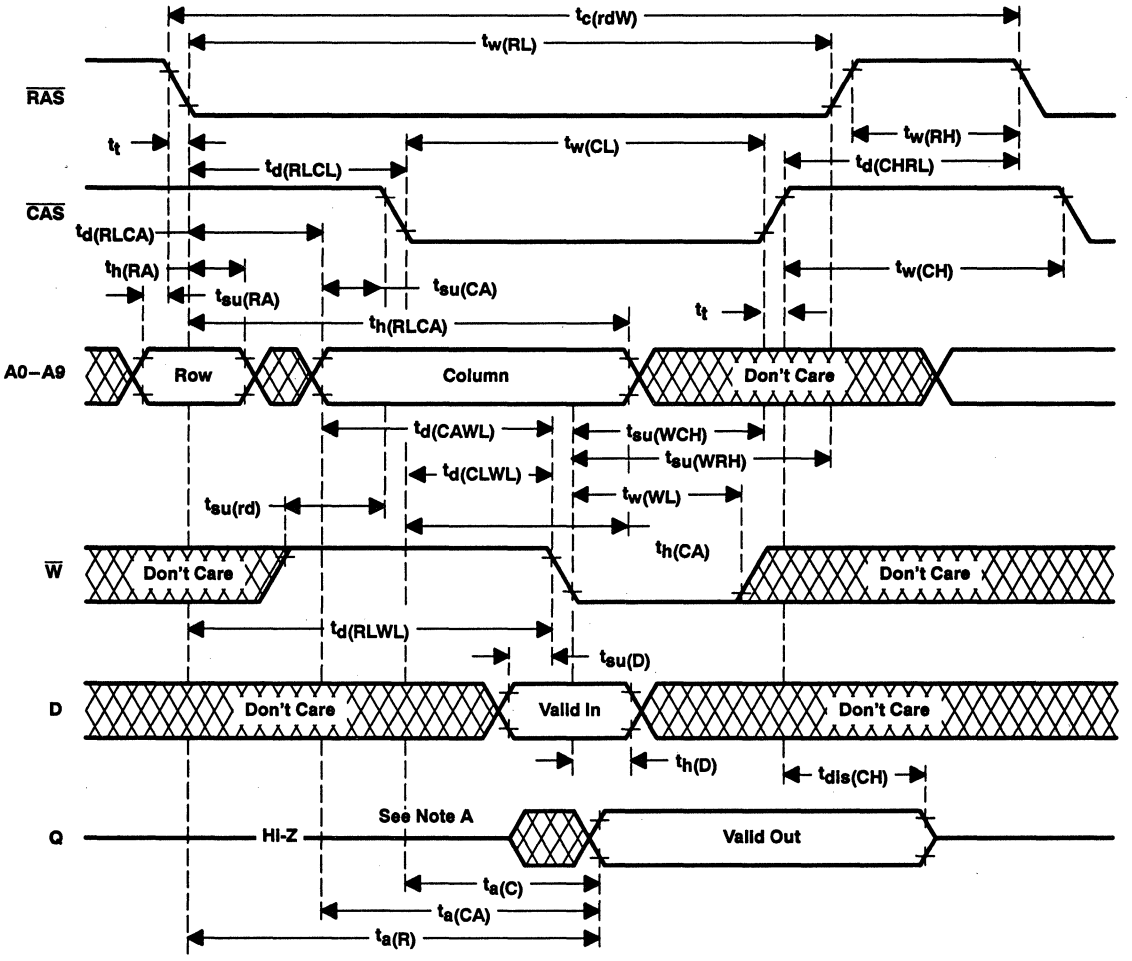


Figure 4. Write-Cycle Timing

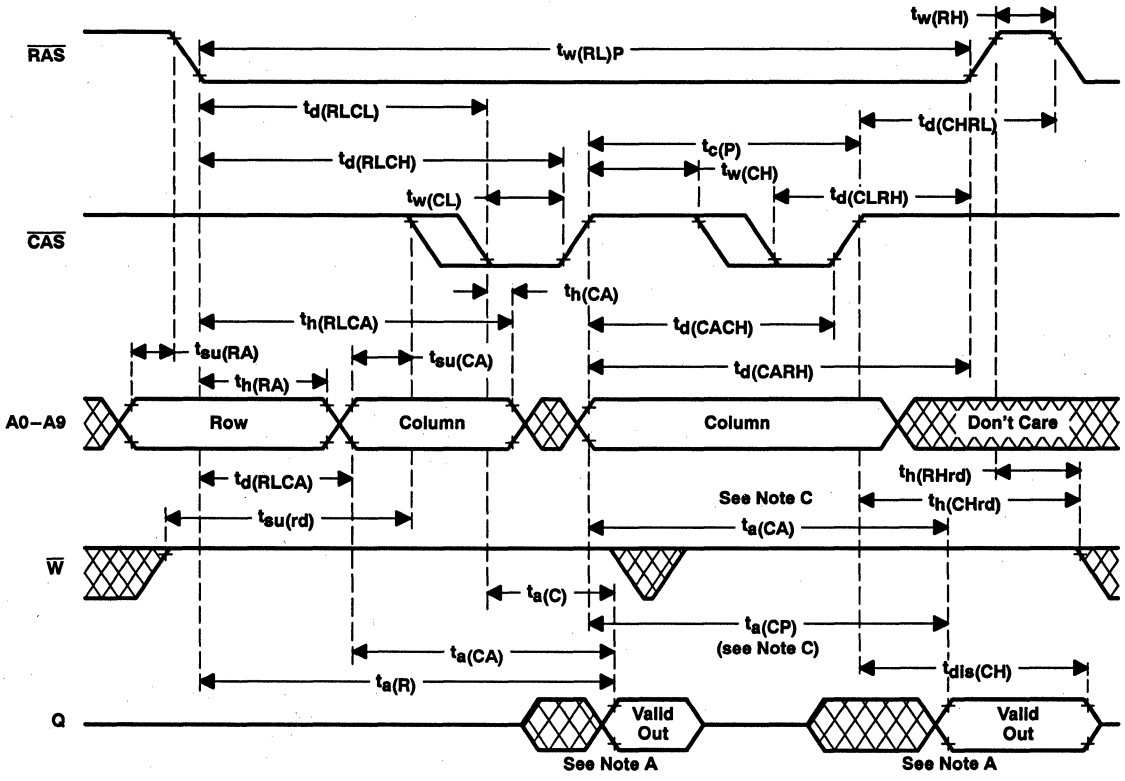
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 5. Read-Write-/Read-Modify-Write-Cycle Timing

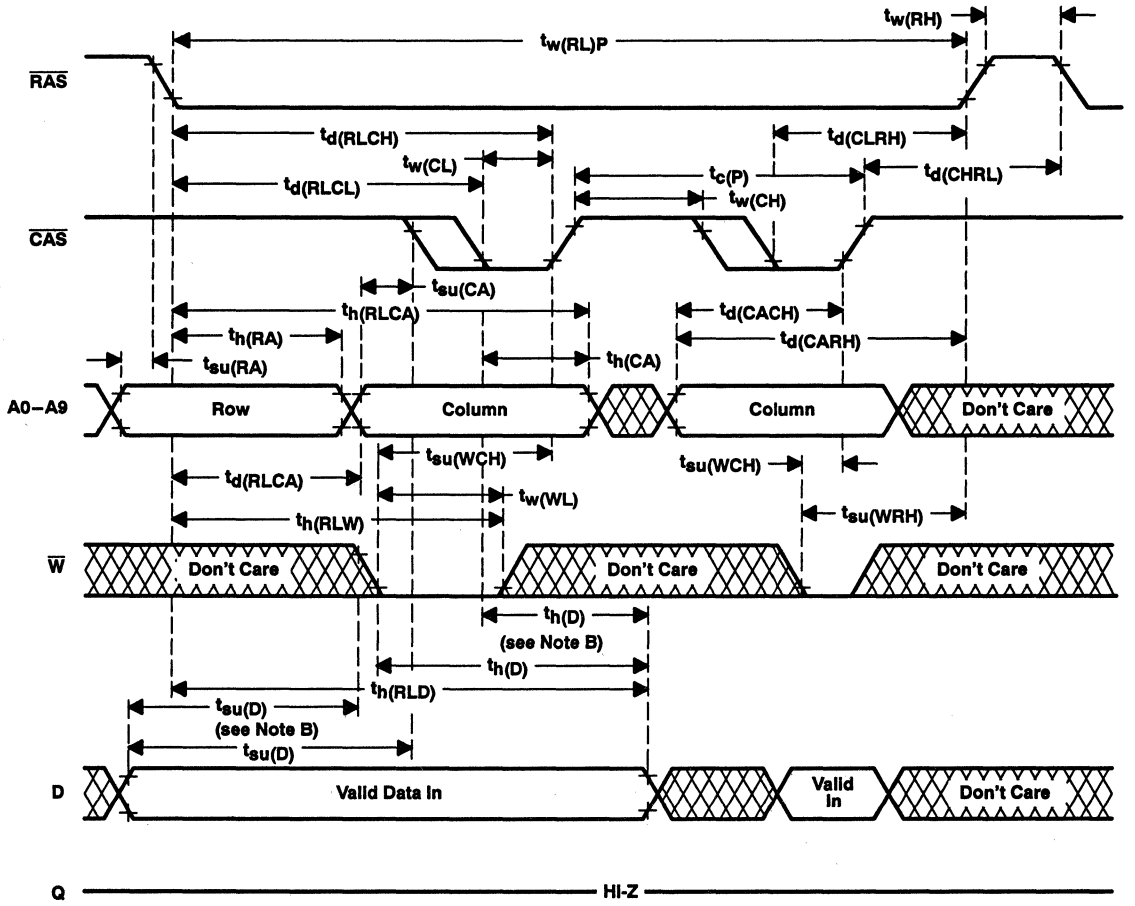
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A write cycle or a read-modify cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
C. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

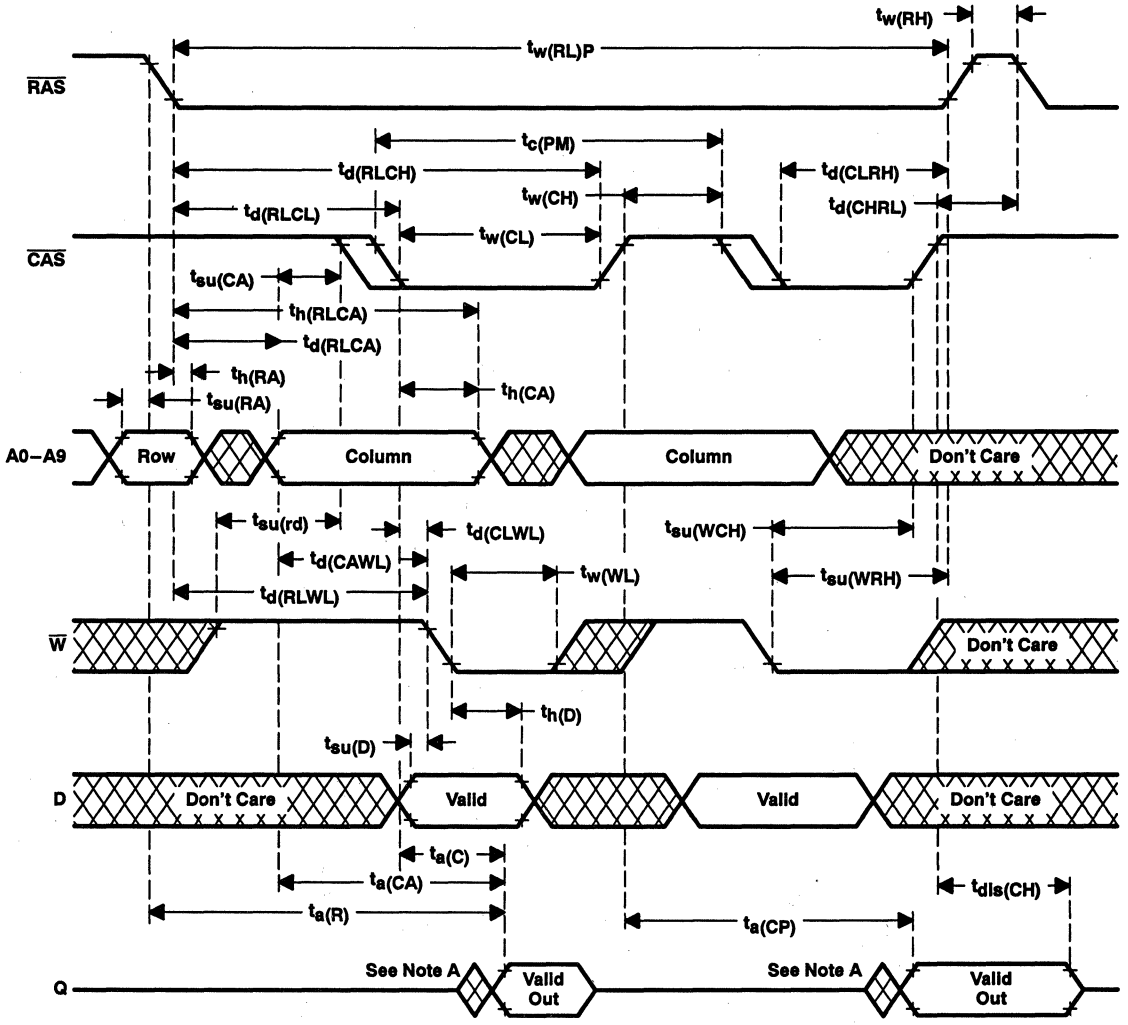
PARAMETER MEASUREMENT INFORMATION



NOTES: A. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.
B. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go the from high-impedance state to an invalid-data state prior to the specified access time.
B. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

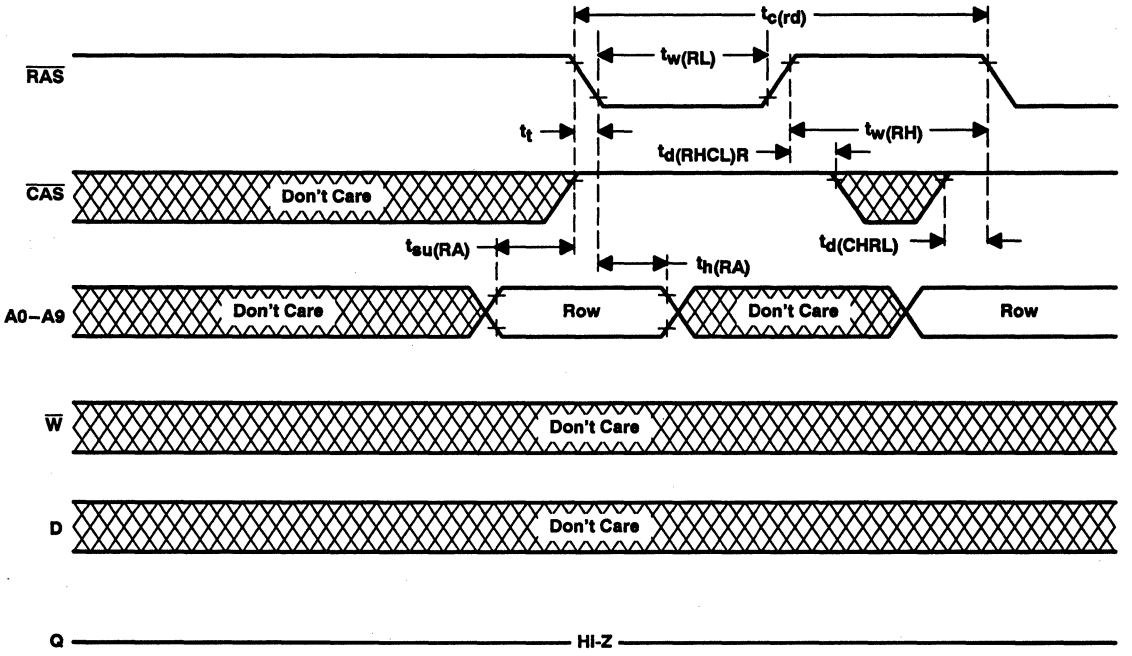


Figure 9. $\overline{RAS}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

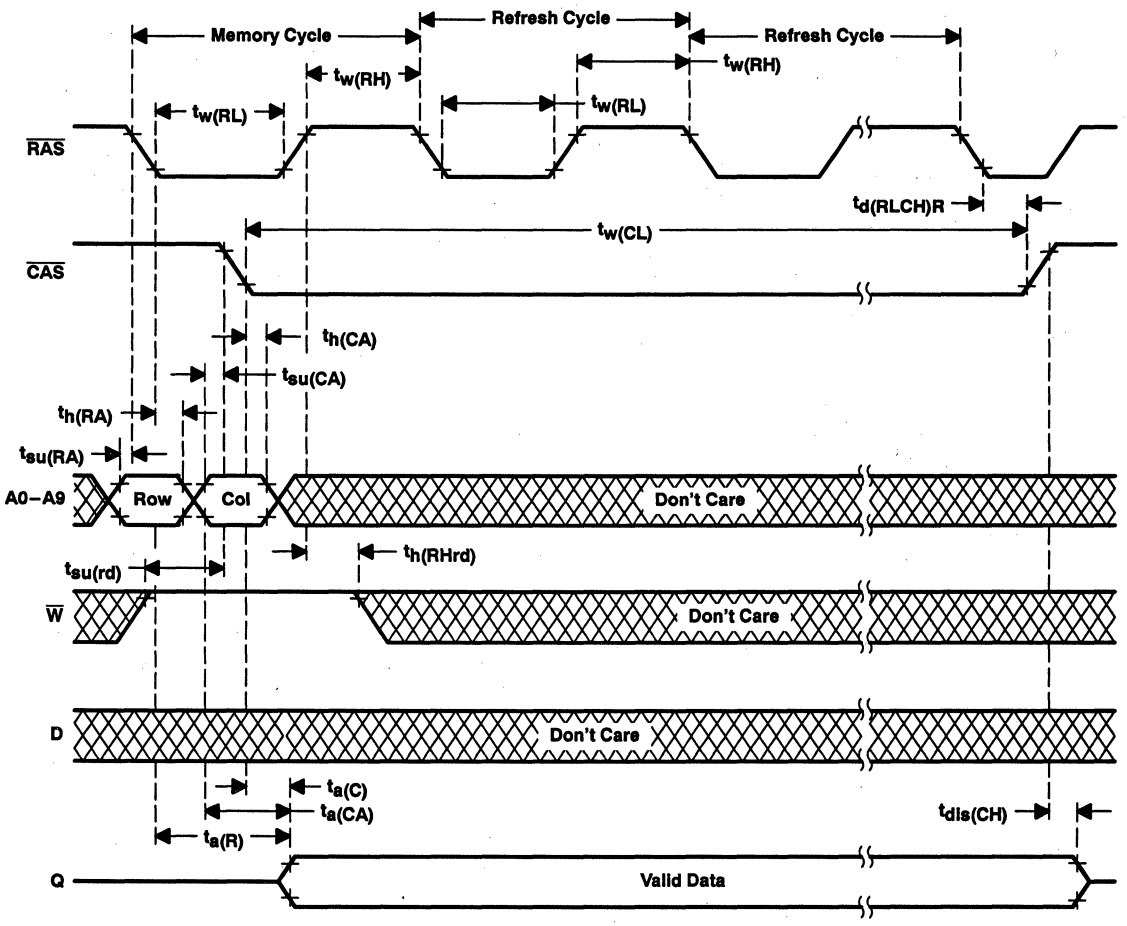


Figure 10. Hidden-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

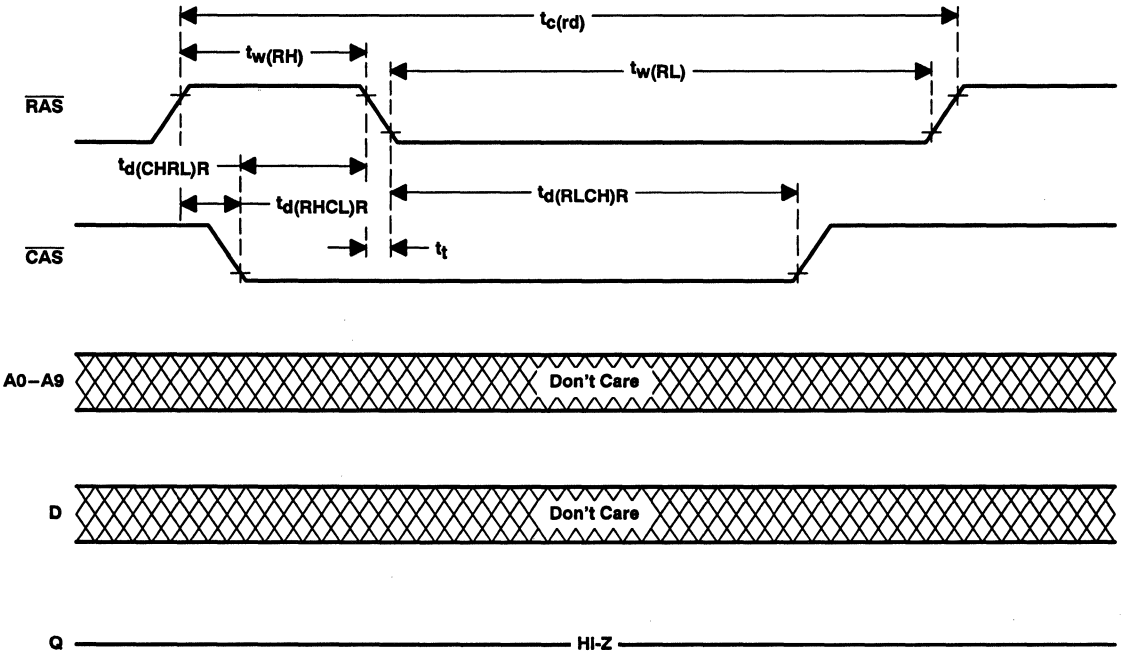


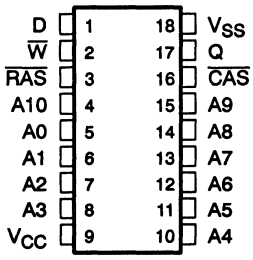
Figure 11. Automatic-CBR-Refresh-Cycle Timing

- **Processed to MIL-STD-883, Class B**
- **Organization . . . 4194304 × 1**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

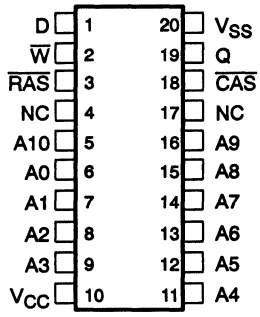
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ44100-80	80 ns	20 ns	40 ns	150 ns
SMJ44100-10	100 ns	25 ns	50 ns	180 ns
SMJ44100-12	120 ns	30 ns	55 ns	210 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
  - **Higher Data Bandwidth Than Conventional Page-Mode Parts**
  - **Random Single-Bit Access Within a Row With a Column Address**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  1024-Cycle Refresh in 16 ms (Max)
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **Packaging Options:**
  - **18-Pin, 400 mil Ceramic DIP (JD Suffix)**
  - **18-Pin, 300 mil Ceramic DIP (JDB Suffix)**
  - **20-Pin, Ceramic Flatpack (HR Suffix)**
  - **20-Pad, 350 × 675 Ceramic Chip Carrier (HL Suffix)**
  - **Additional Package Options Planned**
- **Military Temperature Range**
  –55 °C to 125°C

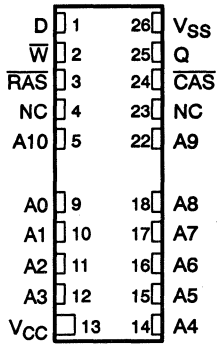
JD/JDB PACKAGES
(TOP VIEW)



HR PACKAGE
(TOP VIEW)



HL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Internal Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The SMJ44100 is a series of high-speed 4194304-bit dynamic random-access memories (DRAMs), organized as 4194304 words of one bit each. They employ state-of-the-art enhanced performance implanted CMOS EPIC™ technology for high performance, reliability, and low power operation.

The SMJ44100 features maximum row access time of 80 ns, 100 ns, and 120 ns. Maximum power dissipation is as low as 385 mW operating and 22 mW standby.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data-out lines are unlatched to allow greater system flexibility.

EPIC is a trademark of Texas Instruments Incorporated.

description (continued)

The SMJ44100 is offered in a 300-mil 18-pin ceramic dual-in-line package (JDB suffix), an 18-pin ceramic dual-in-line package (JD suffix), a 20-pin ceramic flatpack (HR suffix), and a 20-pad 350 × 675 ceramic chip carrier package (HL suffix). All packages are guaranteed for operation from – 55°C to 125°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44100 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ goes low. This performance improvement is referred to as enhanced page mode. Valid column address can be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} maximum (access time from $\overline{CAS}$ low), if t_{AA} maximum (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0–A10)

Twenty-two address bits are required to decode 1 of 4194304 storage cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by $\overline{RAS}$. The eleven column-address bits are set up on pins A0 through A10 and latched onto the chip by $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-write cycle, $\overline{CAS}$ is already low, the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The high-impedance state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{AA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-write cycle, the output follows the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every 16 ms to retain data. This can be achieved by strobing each of the1024 rows (A0–A9, A10 is ignored). A normal read or write cycle refreshes all bits in each row that is selected as well as the corresponding row relative to A10. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

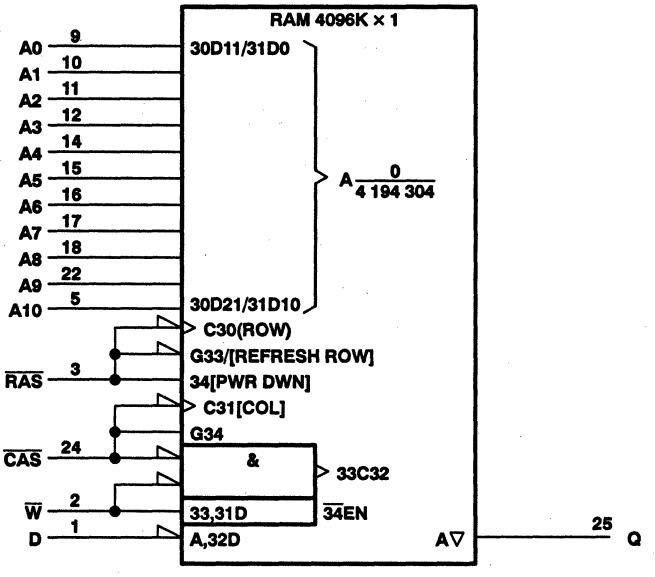
power-up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

test mode

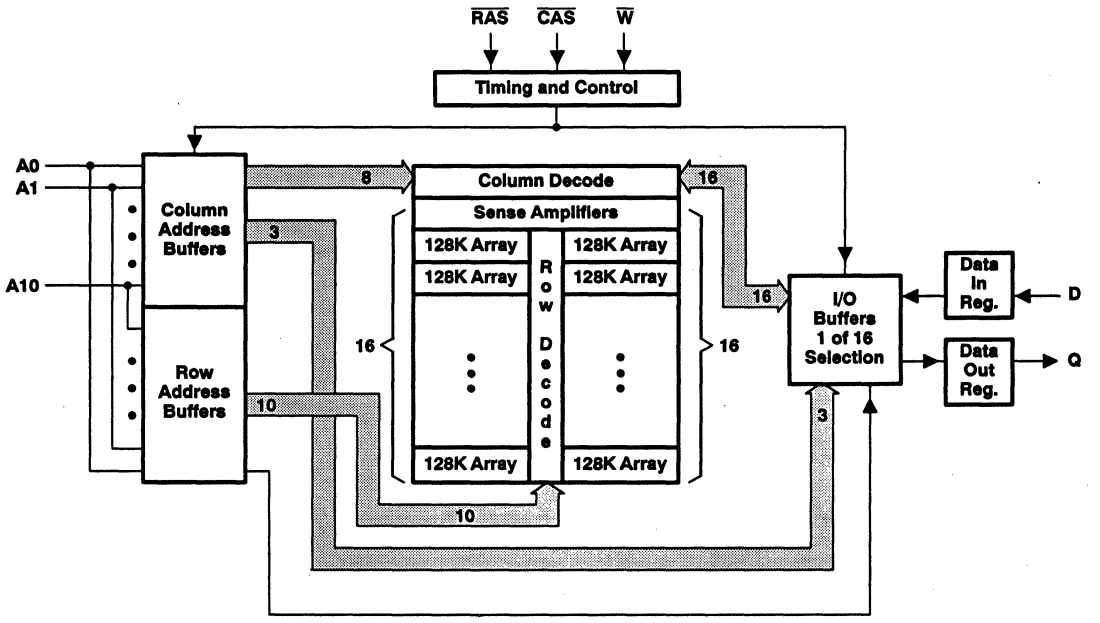
An industry standard design for test (DFT) mode is incorporated in the SMJ44100. A $\overline{CBR}$ cycle with $\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. Data is compared upon reading and if all bits are equal, the data-out pin goes high. If any one bit is different, the data-out pin goes low. Any combination read, write, read-write, or page-mode can be used in test mode. The test mode function reduces test times by enabling the 4M DRAM to be tested as if it were a 512K DRAM, where row address 10, column address 10, and also column address 0 are not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the HM package.

functional block diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... – 55°C to 125°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Minimum operating temperature	– 55			°C
T_C	Maximum operating case temperature			125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'44100-80		'44100-10		'44100-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		85		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		4		4		4	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only, or $\overline{CBR}$) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		85		75		65	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		40		35	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		7	pF
$C_{i(D)}$	Input capacitance, data inputs		7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		10	pF
$C_{i(W)}$	Input capacitance, write-enable input		10	pF
C_o	Output capacitance		10	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V and the bias on pins under test is 0 V. Capacitance is sampled only at initial design and after any major change.

switching characteristics over recommended ranges of supply voltage range and operating free-air temperature

PARAMETER		'44100-80		'44100-10		'44100-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		40		50		55	ns
t_{CAC}	Access time from $\overline{CAS}$ low		20		25		30	ns
t_{CPA}	Access time from column precharge		45		50		55	ns
t_{RAC}	Access time from $\overline{RAS}$ low		80		100		120	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)		20		25		30	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven. The output is disabled when $\overline{CAS}$ is brought high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'44100-80		'44100-10		'44100-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	150		180		210		ns
t_{RWC}	Cycle time, read-write	175		210		245		ns
t_{PC}	Cycle time, page-mode read or write (see Note 8)	50		60		65		ns
t_{PRWC}	Cycle time, page-mode read-write	70		85		95		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low (see Note 9)	80	100 000	100	100 000	120	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low (see Note 9)	80	10 000	100	10 000	120	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	20	10 000	25	10 000	30	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		15		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	60		70		80		ns
t_{WP}	Pulse duration, write	15		20		25		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 11)	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	20		25		30		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	20		25		30		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	15		20		20		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low	60		75		90		ns
t_{DH}	Hold time, data (see Note 11)	15		20		25		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 13)	60		75		90		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		15		15		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 12)	0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 12)	0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low (early-write operation only)	15		20		25		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low (see Note 10)	60		75		90		ns
t_{WHR}	Hold time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)	40		50		55		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	20		20		25		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	80		100		120		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-write operation only)	20		25		30		ns

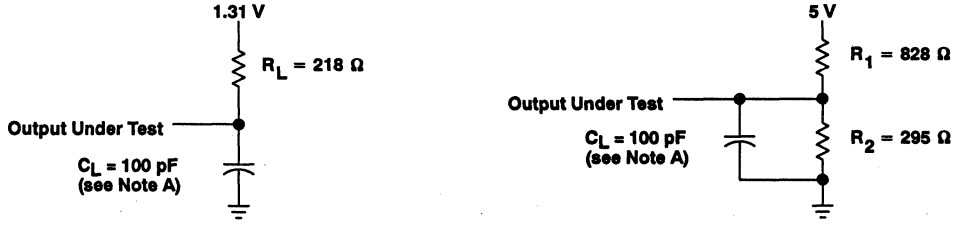
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. The minimum value is measured when t_{RDC} is set to t_{RCD} min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'44100-80		'44100-10		'44100-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 14)	15	40	20	50	20	65	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	40		50		55		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	40		50		55		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	60	25	75	25	90	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	20		25		30		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)	80		100		120		ns
t_{CLZ}	$\overline{CAS}$ to output in low Z (see Note 15)	0		0		0		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time (see Note 16)							

NOTES: 14. Maximum value specified only to assure access time.
15. Valid data is presented at the output after all access times are satisfied. The output can go from the high-impedance state to an invalid-data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.
16. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and maximum of 50 ns.

PARAMETER MEASUREMENT INFORMATION

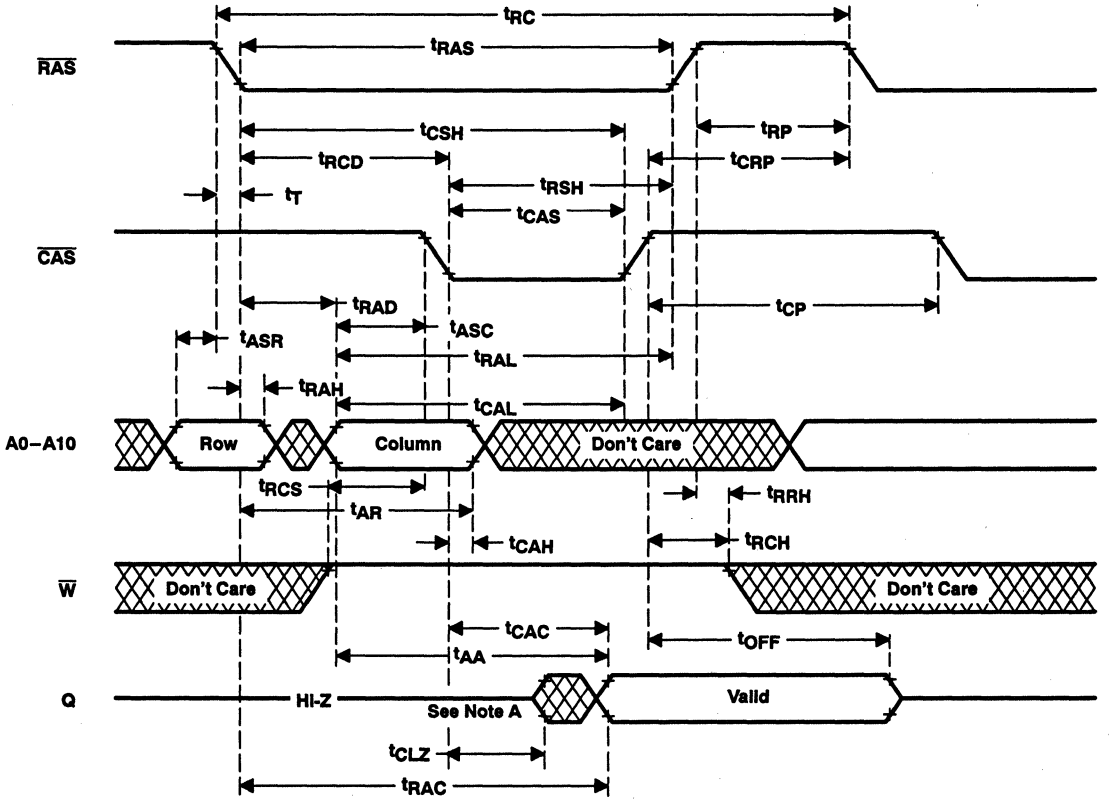


(a) LOAD CIRCUIT (b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the output after all access times are satisfied. The output can go from the high-impedance state to an invalid-data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

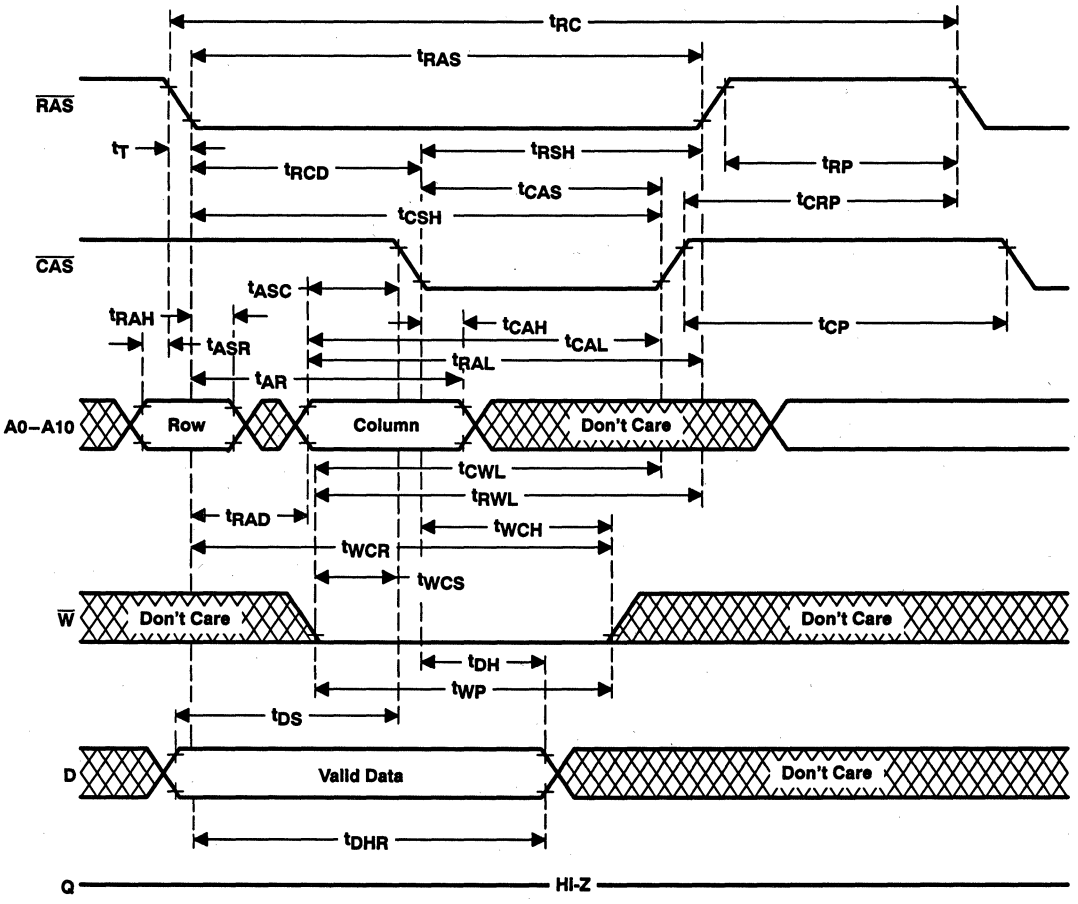
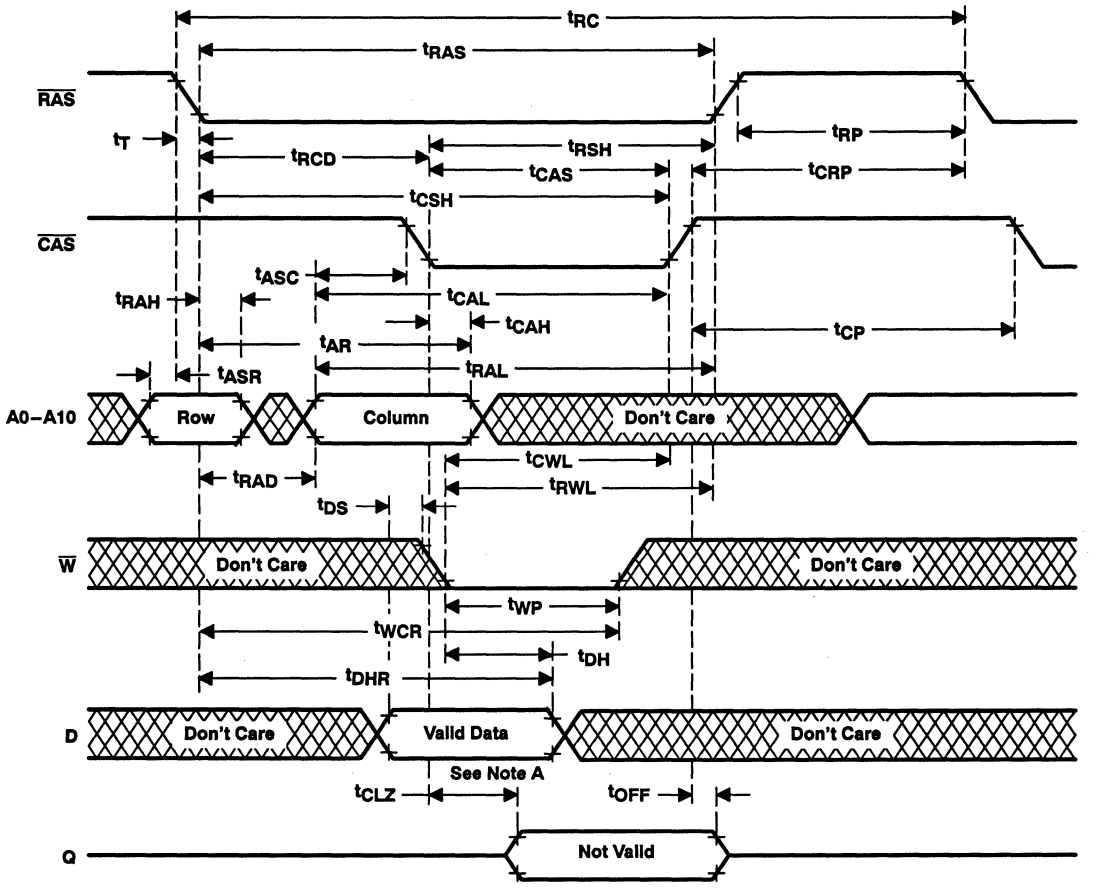


Figure 3. Early-Write-Cycle Timing

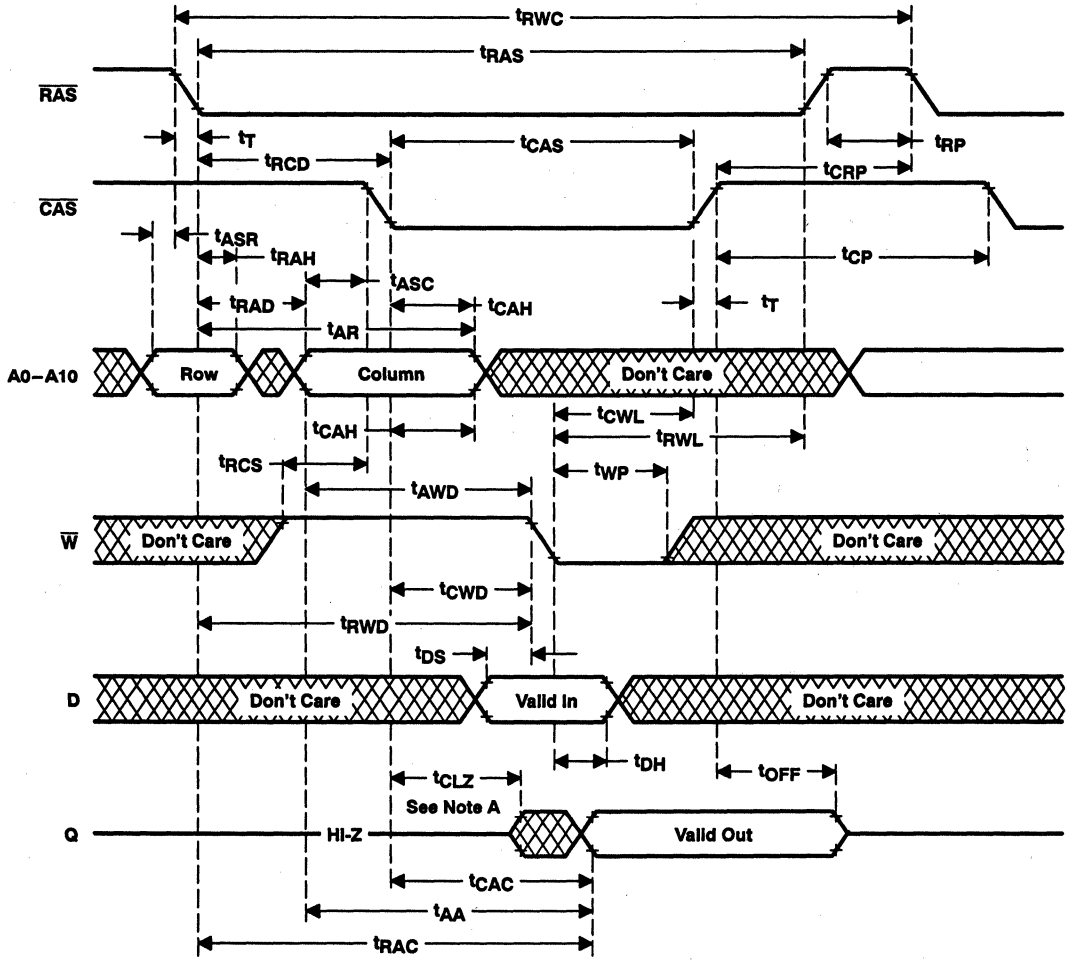
PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the output after all access times are satisfied. The output can go from the high-impedance state to an invalid-data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

Figure 4. Write-Cycle Timing

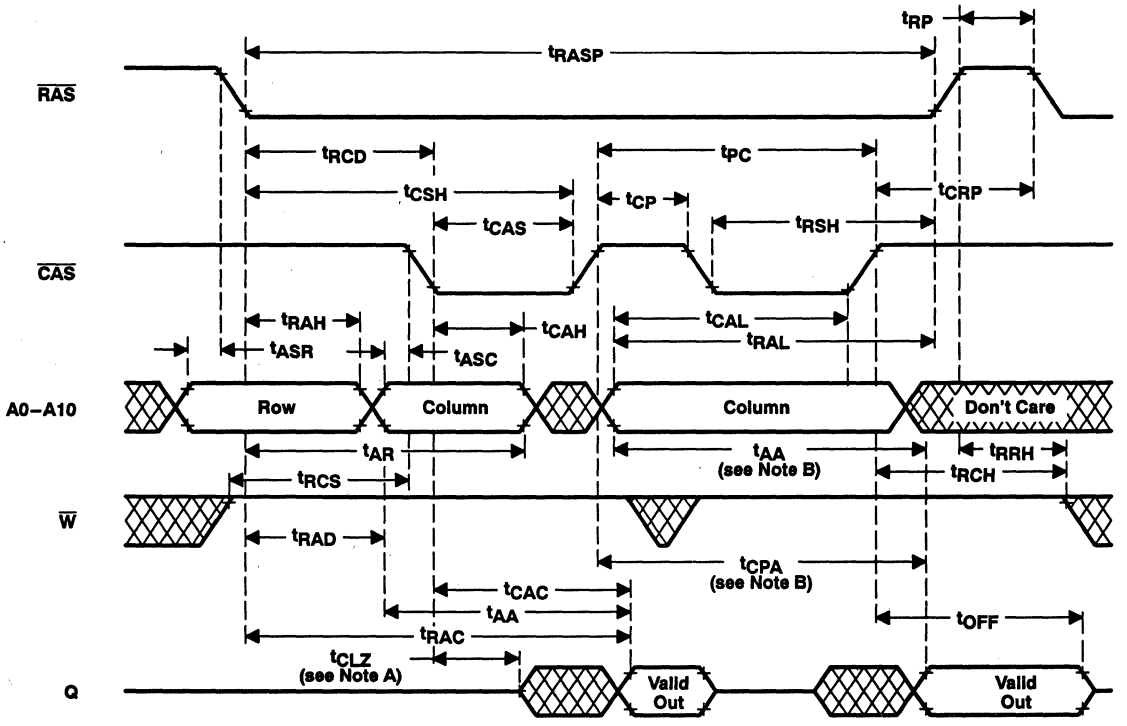
PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the output after all access times are satisfied. The output can go from the high-impedance state to an invalid-data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

Figure 5. Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

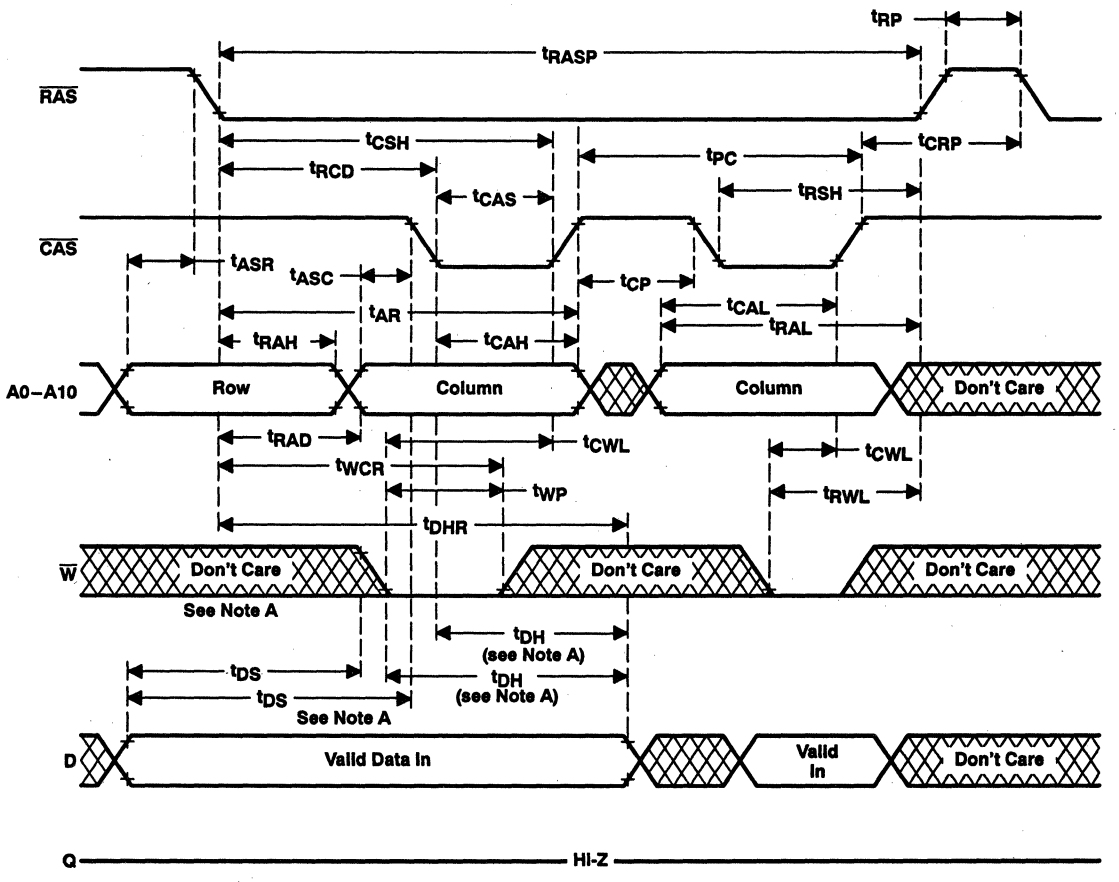


NOTES: A. Valid data is presented at the output after all access times are satisfied. The output can go from the high-impedance state to an invalid-data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

B. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

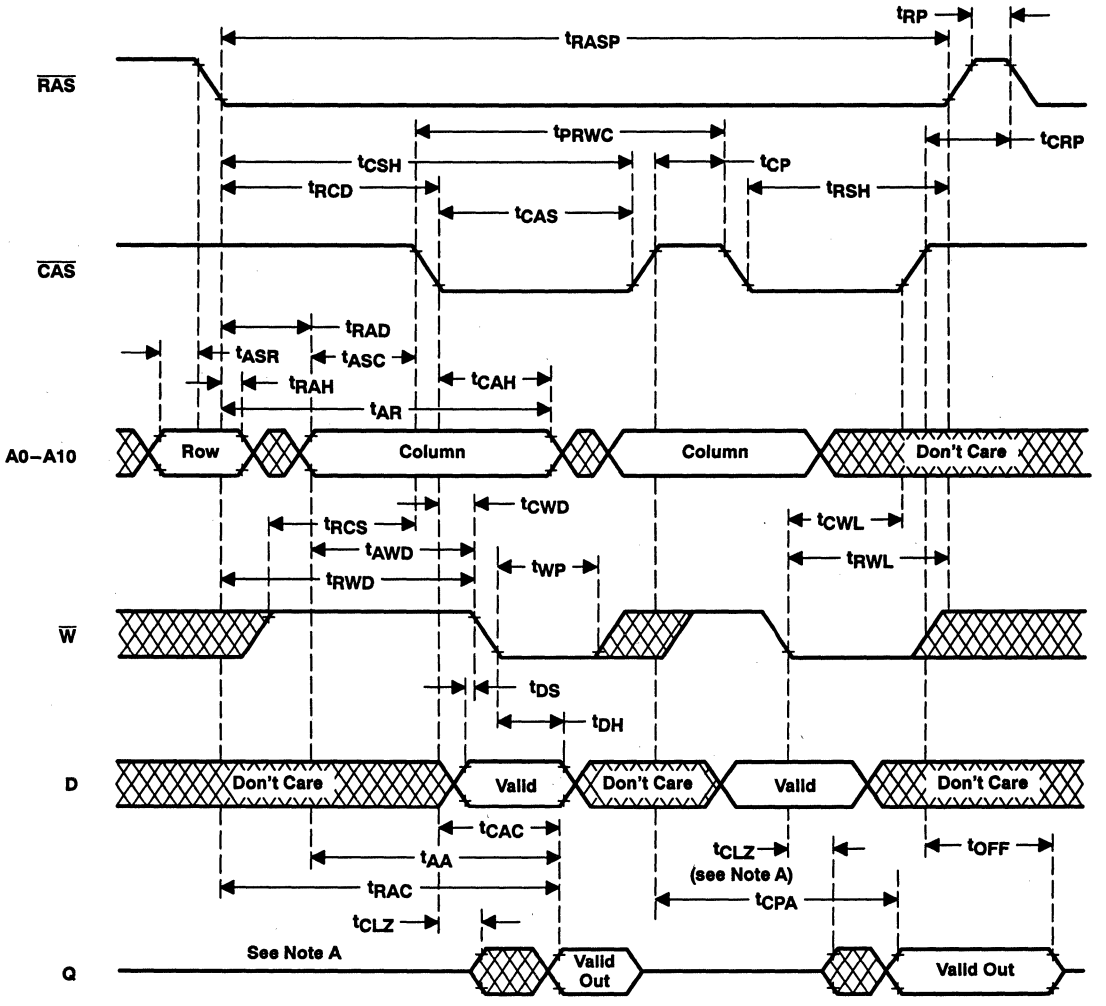
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with a write cycle as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

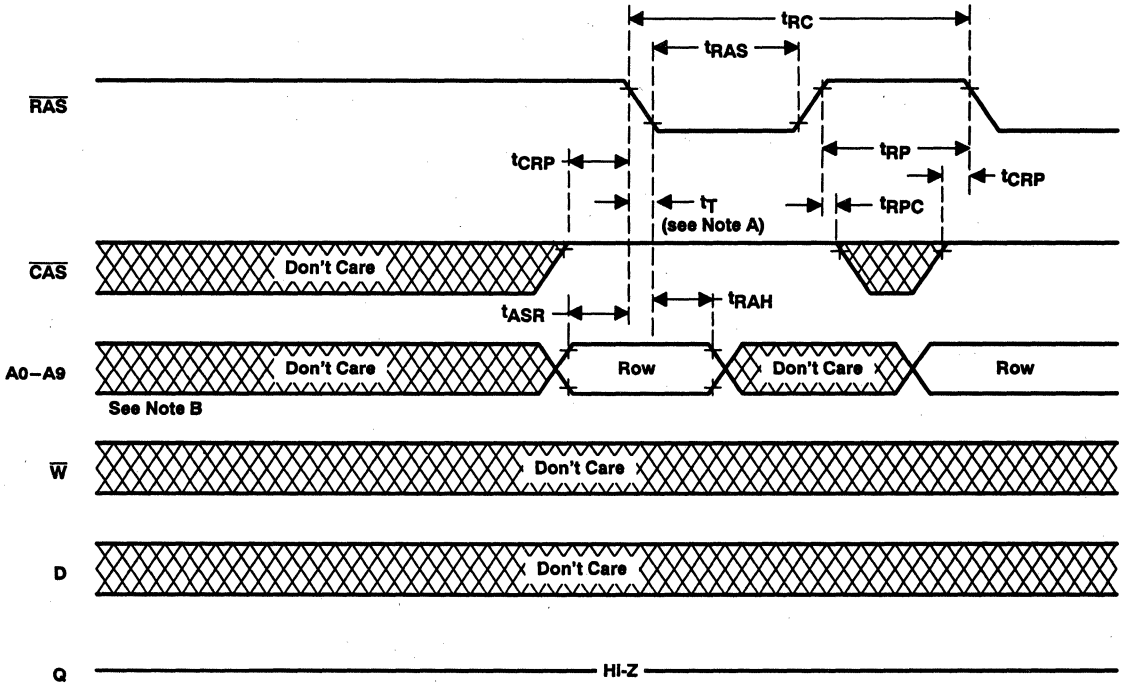
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Valid data is presented at the output after all access times are satisfied. The output can go from the high-impedance state to an invalid-data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Read-Write-Cycle Timing

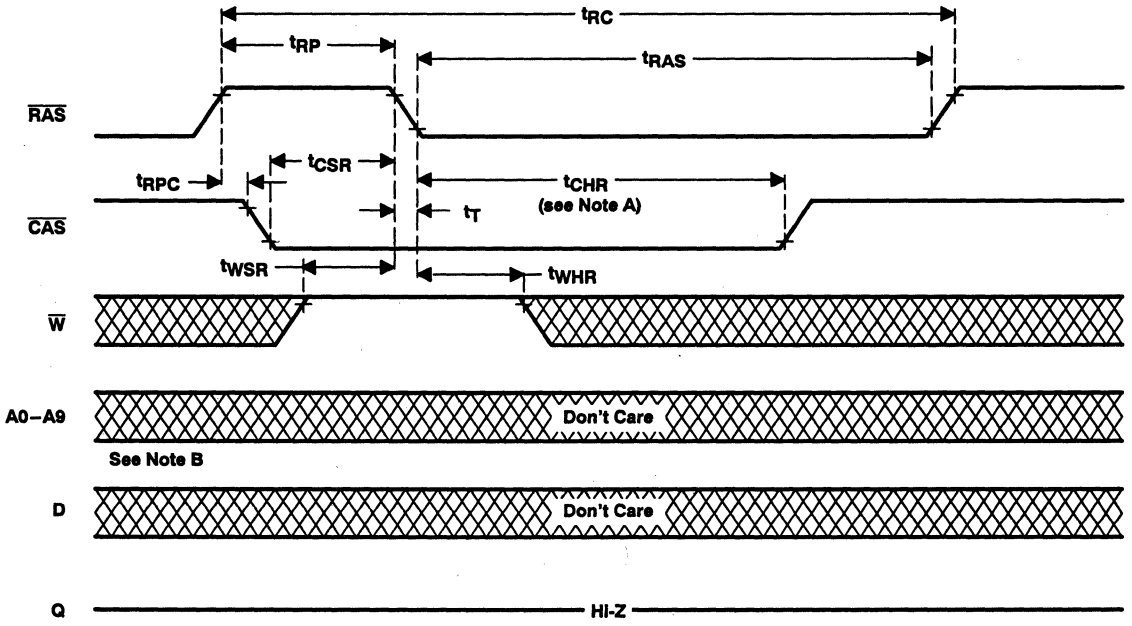
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and maximum of 50 ns.
B. A10 is a don't care.

Figure 9. $\overline{RAS}$-Only Refresh-Cycle Timing

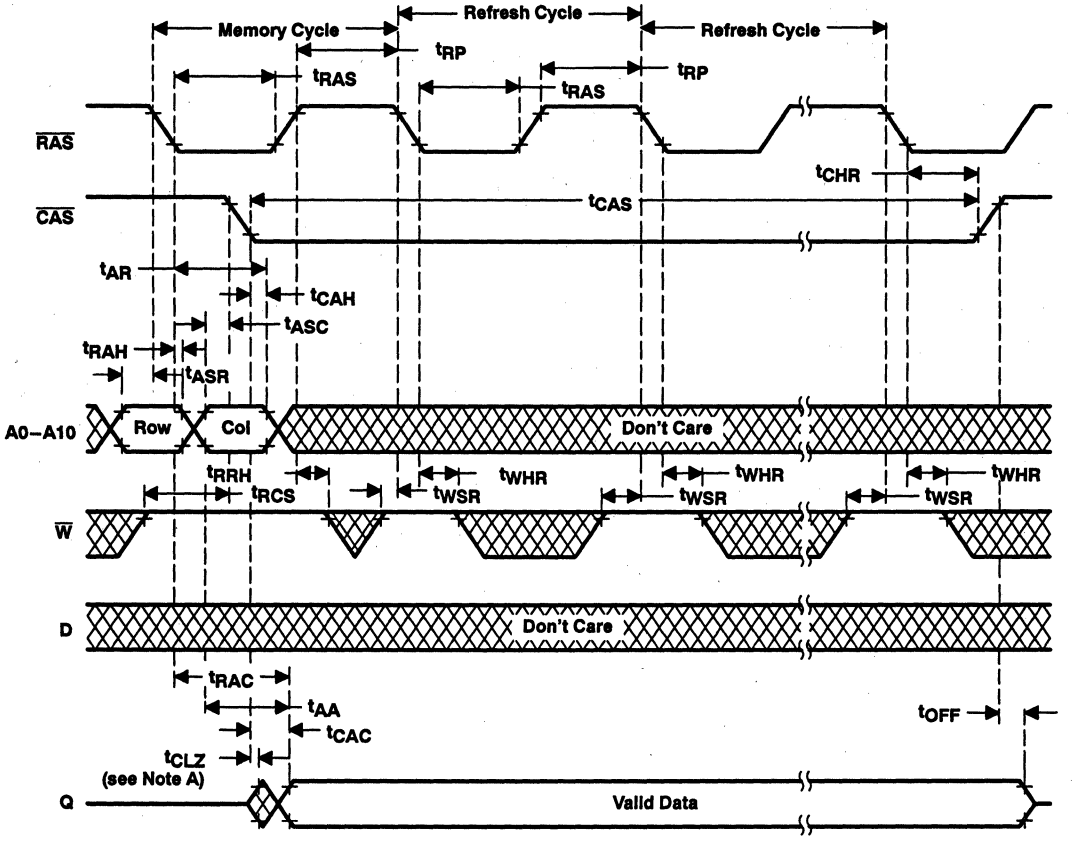
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and maximum of 50 ns.
B. A10 is a don't care.

Figure 10. Automatic CBR Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and maximum of 50 ns.

Figure 11. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

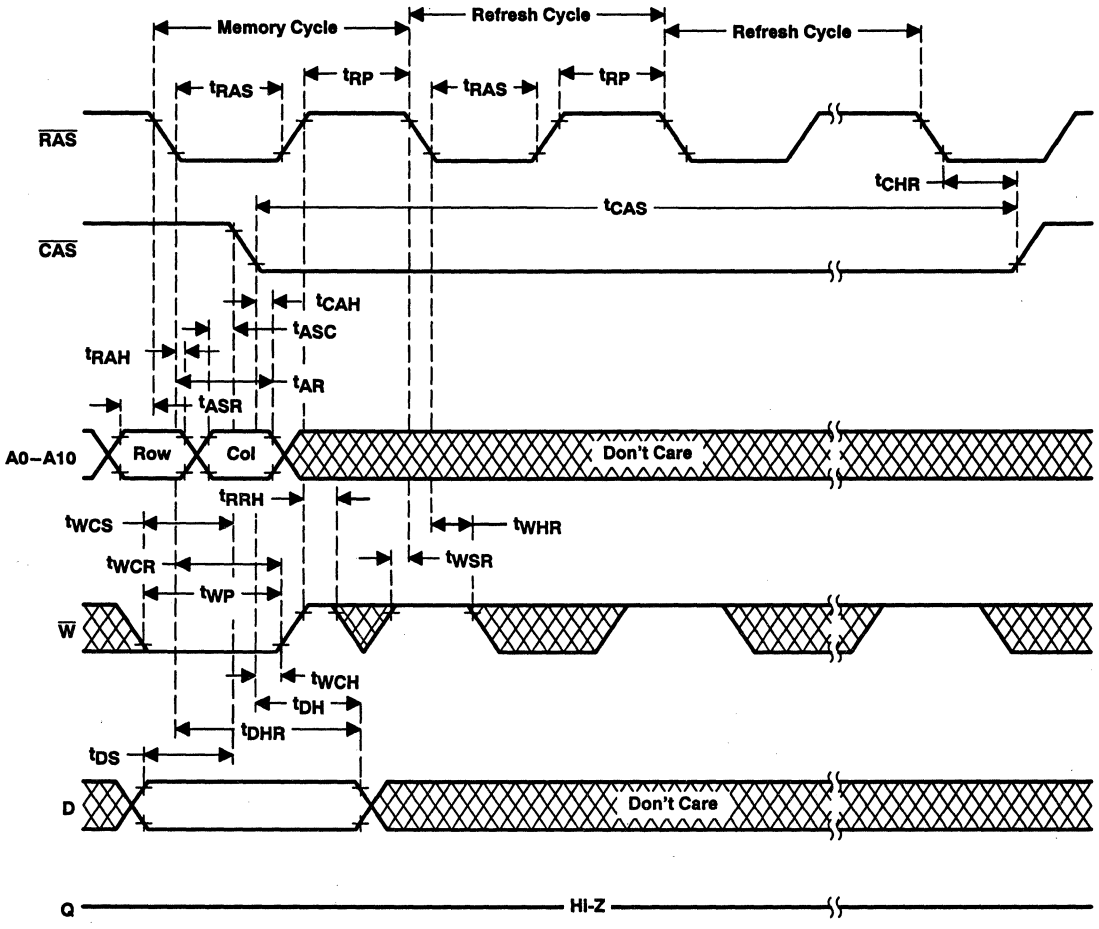


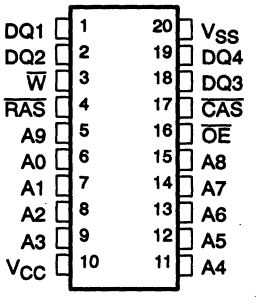
Figure 12. Hidden-Refresh-Cycle (Write) Timing

- **Processed to MIL-STD-883, Class B**
- **Organization . . . 1 048 576 × 4**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

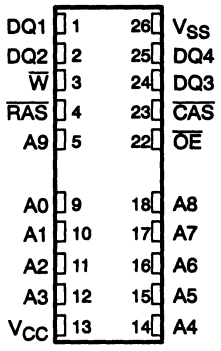
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ44400-80	80 ns	20 ns	40 ns	150 ns
SMJ44400-10	100 ns	25 ns	45 ns	180 ns
SMJ44400-12	120 ns	30 ns	55 ns	210 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
  - **Higher Data Bandwidth Than Conventional Page-Mode Parts**
  - **Random Single-Bit Access Within a Row With a Column Address**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  1024-Cycle Refresh In 16 ms (Max)
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments Enhanced Performance Implanted CMOS (EPIC™) Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **Packaging Options:**
  - **20-Pin, 300-Mil Ceramic Side-Brazed DIP (JDB suffix)**
  - **20-Pin Ceramic Flatpack (HR Suffix)**
  - **20-Pad, 350 × 675 Ceramic Chip Carrier (HL suffix)**
  - **20-Pin Ceramic ZIP (SV suffix)**
  - **Additional Package Options Planned**
- **Military Temperature Range**
  –55 to 125°C

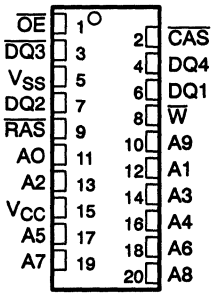
JDB OR HR PACKAGES
(TOP VIEW)



HL PACKAGE
(TOP VIEW)



SV PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The SMJ44400 is a series of high-speed 4 194 304-bit dynamic random-access memories (DRAMs), organized as 1 048 576 words of four bits each. The series employs state-of-the-art EPIC™ technology for high performance, reliability, and low-power operation.

The SMJ44400 features maximum row access times of 80 ns, 100 ns, and 120 ns. Maximum power dissipation is as low as 360 mW operating and 22 mW standby.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

EPIC is a trademark of Texas Instruments Incorporated.

description (continued)

The SMJ44400 is offered in a 300-mil, 20-pin ceramic side-brazed dual-in-line package (JDB suffix), a 20-pin ceramic flatpack (HR suffix), a 20-pad 350 x 675 ceramic chip carrier (HL suffix), and a 20-pin ceramic zig-zag in-line package (SV suffix). All packages are characterized for operation from –55°C to 125°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44400 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ goes low. This performance improvement is referred to as enhanced page mode. Valid column address can be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} maximum (access time from $\overline{CAS}$ low), if t_{AA} maximum (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0–A9)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by $\overline{RAS}$. The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early-write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ1–DQ4)

The high-impedance output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to the high-impedance state.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every 16 ms to retain data. This can be achieved by strobing each of the1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) and hidden refresh

CBR refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CSR}). For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. During CBR refresh cycles the outputs remain in the high-impedance state.

HIdden refresh can be performed while maintaining valid data at the output pins. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation. $\overline{RAS}$ is cycled after the specified read cycle parameters are met. HIdden refresh can also be used in conjunction with an early-write cycle. $\overline{CAS}$ is maintained at V_{IL} while $\overline{RAS}$ is cycled, once all the specified early-write parameters are met. Externally generated addresses must be used to specify the location to be accessed during the initial $\overline{RAS}$ cycle of a hidden refresh operation. Subsequent $\overline{RAS}$ cycles (refresh cycles) use the internally-generated addresses and the external address is ignored.

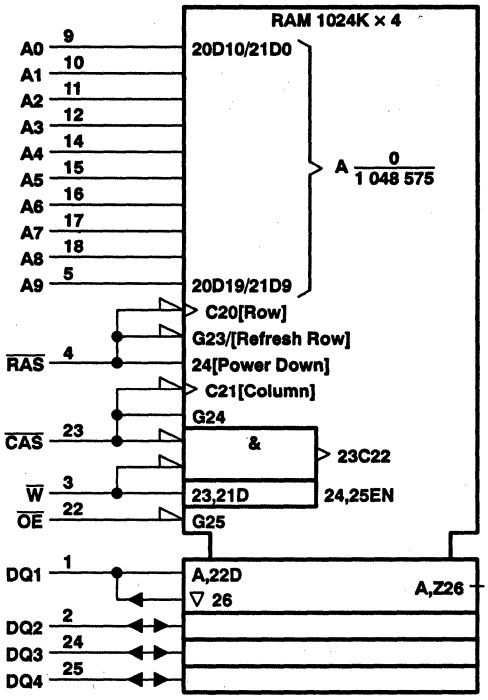
power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

test mode

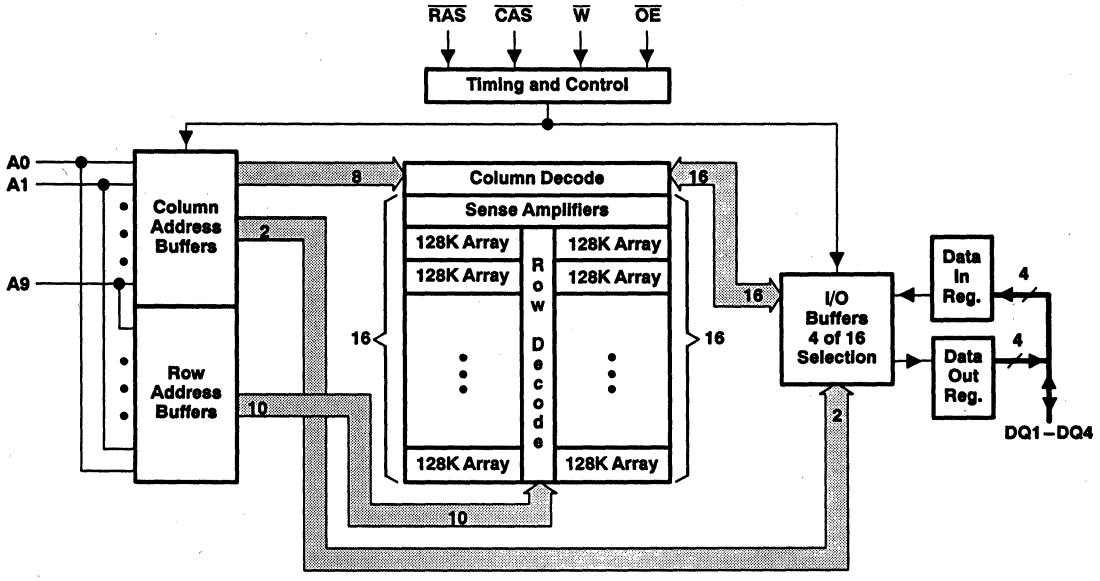
An industry standard Design For Test (DFT) mode is incorporated in the SMJ44400. A CBR with $\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. All data is written into the array through DQ1. Data is compared upon reading and if all bits are equal, all DQ pins go high. If any one bit is different, all the DQ pins go low. Any combination read, write, read-write, or page-mode can be used in the test mode. The test mode function reduces test times by enabling the 1M × 4-bit DRAM to be tested as if it were a 512K DRAM where column address 0 is not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The pinouts illustrated are for the HL package.

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating temperature range, T_A ..... – 55°C to 125°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Minimum operating temperature	– 55			°C
T_C	Maximum operating case temperature			125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'44400-80		'44400-10		'44400-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		85		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		4		4		4	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only, or $\overline{CBR}$) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low ($\overline{CBR}$)		85		75		65	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		40		35	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		10	pF
$C_{i(W)}$	Input capacitance, write-enable input		10	pF
C_O	Output capacitance		10	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V and the bias on pins under test is 0 V. Capacitance is sampled only at initial design and after any major change.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

		'44400-80		'44400-10		'44400-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		40		45		55	ns
t_{CAC}	Access time from $\overline{CAS}$ low		20		25		30	ns
t_{CPA}	Access time from column precharge		45		50		55	ns
t_{RAC}	Access time from $\overline{RAS}$ low		80		100		120	ns
t_{OEA}	Access time from $\overline{OE}$ low		20		25		30	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)		20		25		30	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)		20		25		30	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven. The outputs are disabled by bringing either $\overline{OE}$ or $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'44400-80		'44400-10		'44400-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	150		180		210		ns
t_{RWC}	Cycle time, read-write	205		245		285		ns
t_{PC}	Cycle time, page-mode read or write (see Note 8)	50		60		65		ns
t_{PRWC}	Cycle time, page-mode read-write	100		120		135		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low (see Note 9)	80	100 000	100	100 000	120	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low (see Note 9)	80	10 000	100	10 000	120	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	20	10 000	25	10 000	30	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		15		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	60		70		80		ns
t_{WP}	Pulse duration, write	15		20		25		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 11)	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	20		25		30		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	20		25		30		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	15		20		20		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low	60		75		90		ns
t_{DH}	Hold time, data (see Note 11)	15		20		25		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 10)	60		75		90		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		15		15		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 12)	0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 12)	0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low (early-write operation only)	15		20		25		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low (see Note 10)	60		75		90		ns
t_{WHR}	Hold time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{OEH}	Hold time, $\overline{OE}$ command	20		25		30		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	20		25		30		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)	70		80		90		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	20		20		25		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	80		100		120		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-write operation only)	50		60		70		ns

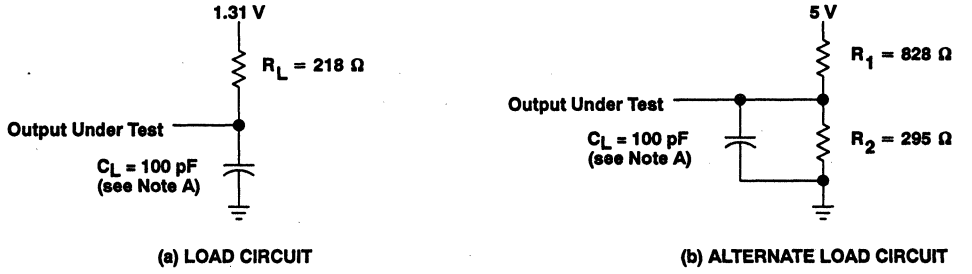
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'44400-80		'44400-10		'44400-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 13)	15	40	20	50	20	65	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	40		50		55		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	40		50		55		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)	20	60	25	75	25	90	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	20		25		30		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)	110		135		160		ns
t_{CLZ}	$\overline{CAS}$ to output in low Z (see Note 14)	0		0		0		ns
t_{OED}	$\overline{OE}$ to data delay	20		25		30		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time (see Note 15)							

NOTES: 13. Maximum value specified only to assure access time.
14. Valid data is presented at the outputs after all access times are satisfied but can go from the high-impedance state to an invalid-data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ and $\overline{OE}$ are low.
15. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

PARAMETER MEASUREMENT INFORMATION

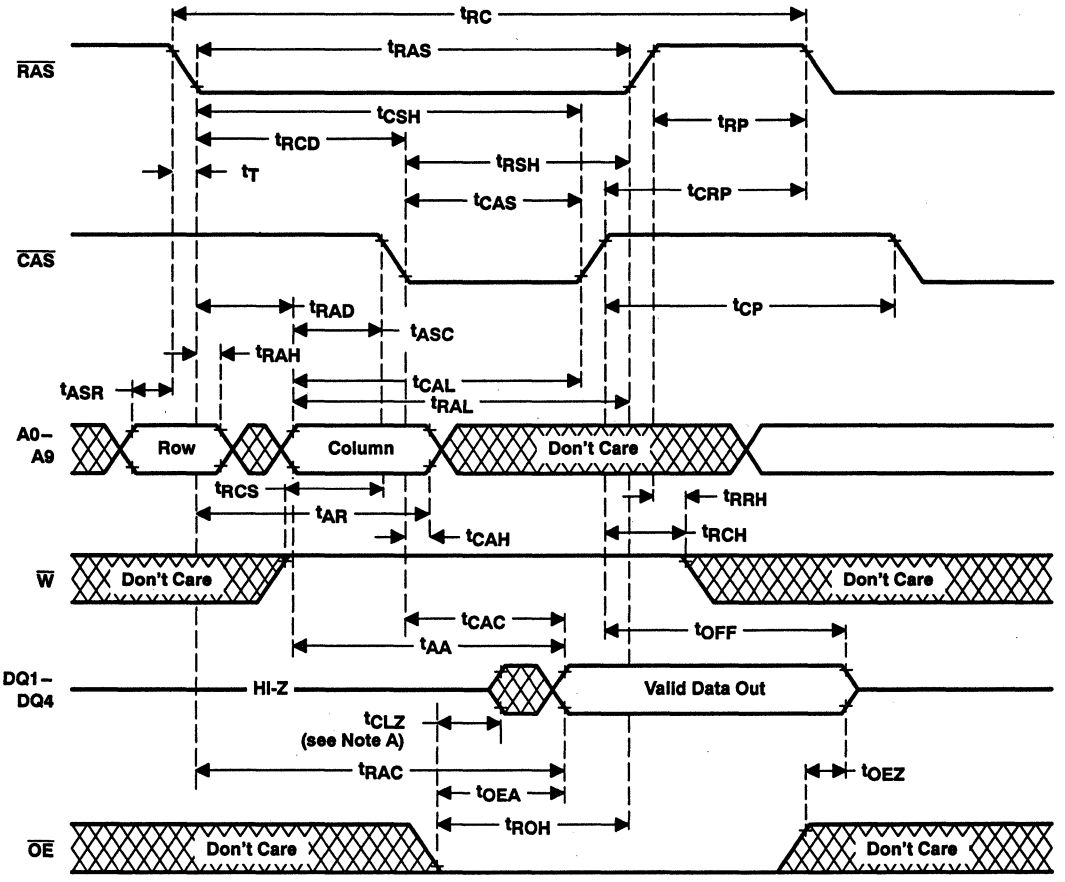


(a) LOAD CIRCUIT (b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the outputs after all access times are satisfied but can go from the high-impedance state to an invalid-data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ and $\overline{OE}$ are low.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

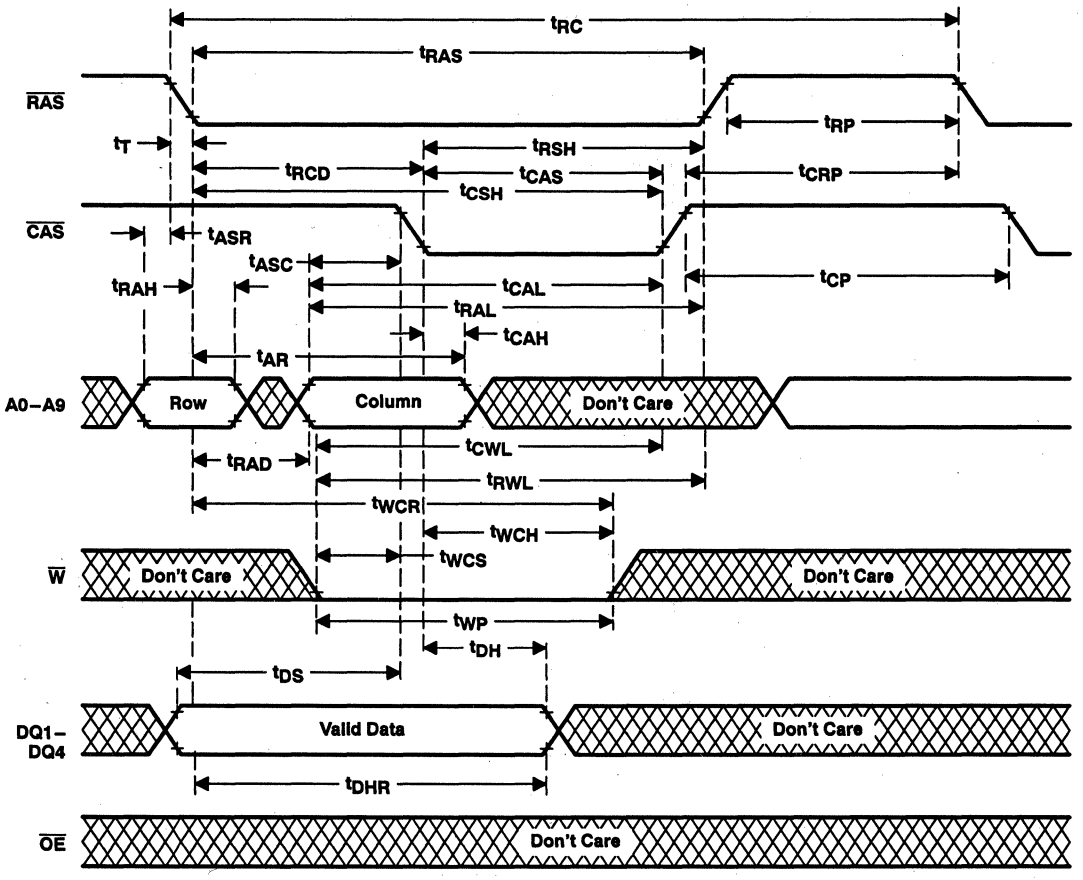


Figure 3. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

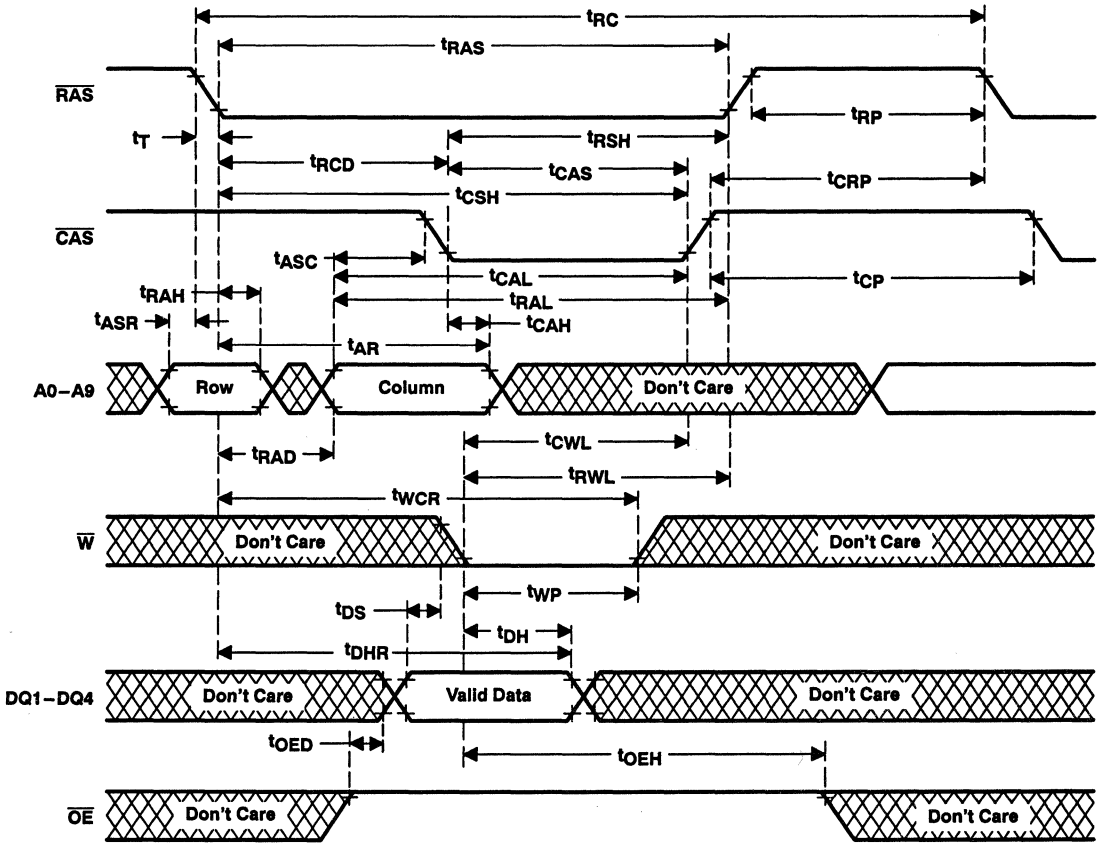
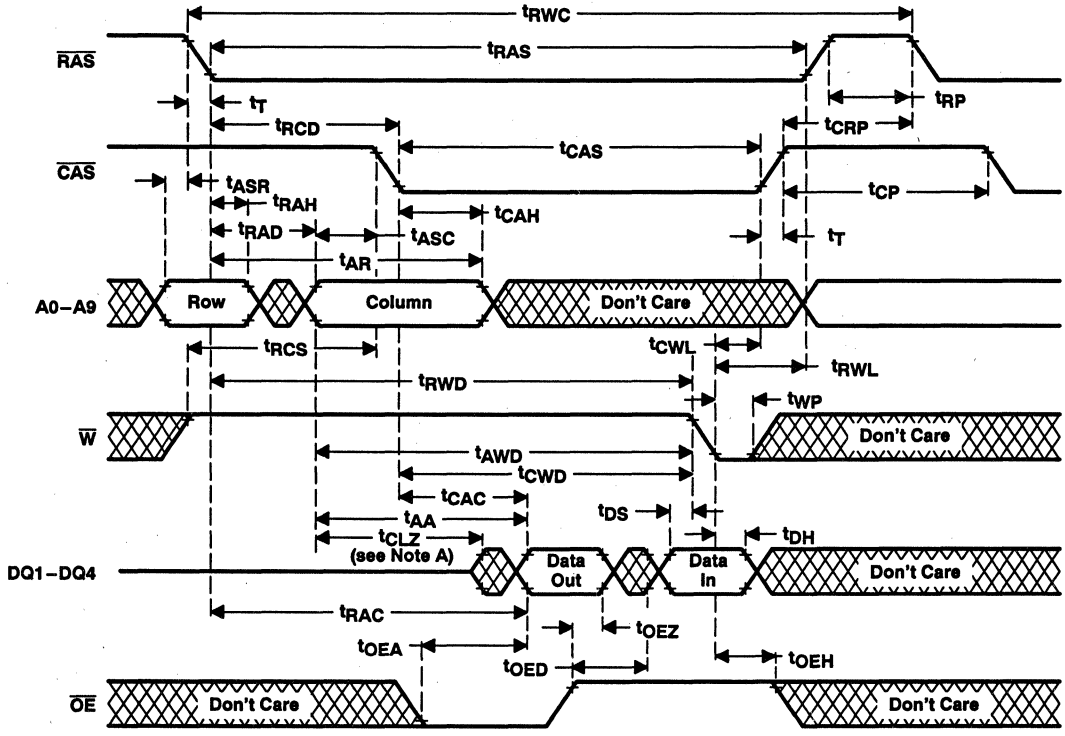


Figure 4. Write-Cycle Timing

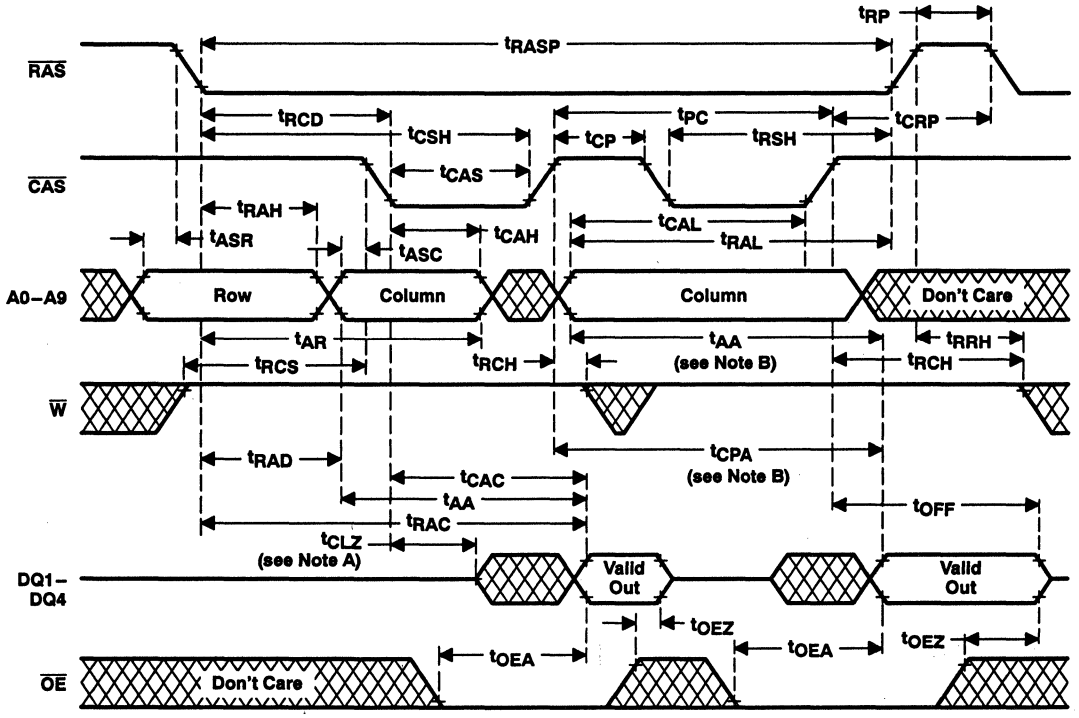
PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the outputs after all access times are satisfied but can go from the high-impedance state to an invalid-data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ and $\overline{OE}$ are low.

Figure 5. Read-Write Cycle Timing

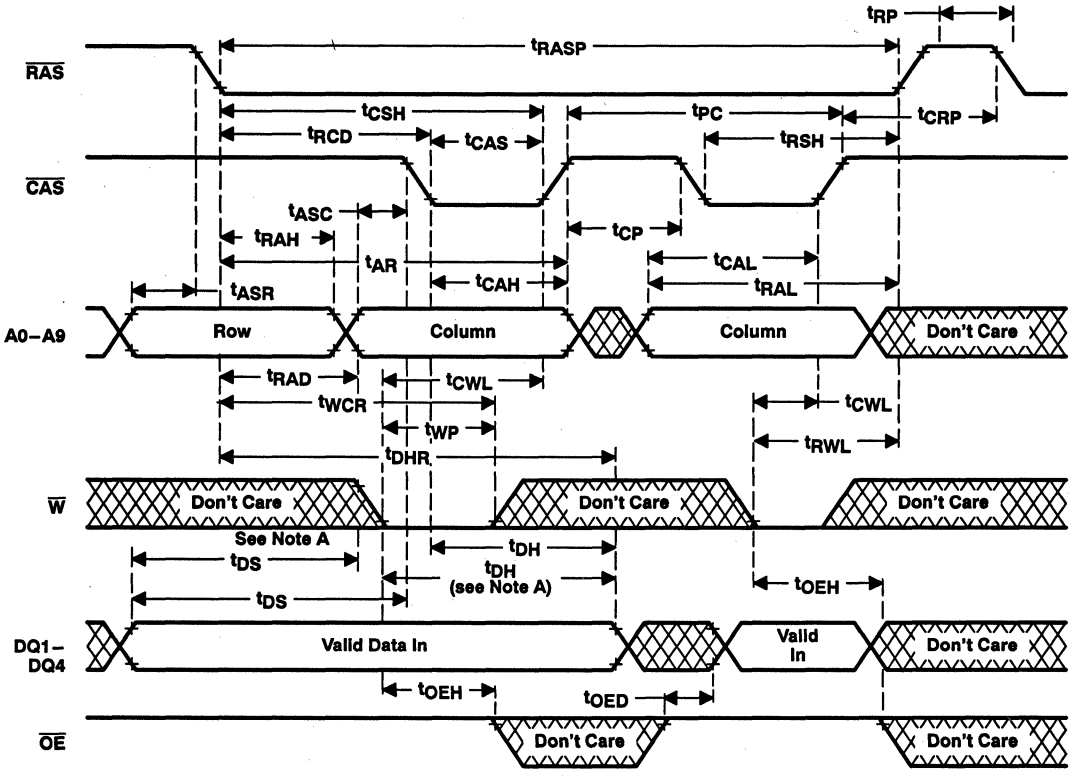
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Valid data is presented at the outputs after all access times are satisfied but can go from the high-impedance state to an invalid-data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ and $\overline{OE}$ are low.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

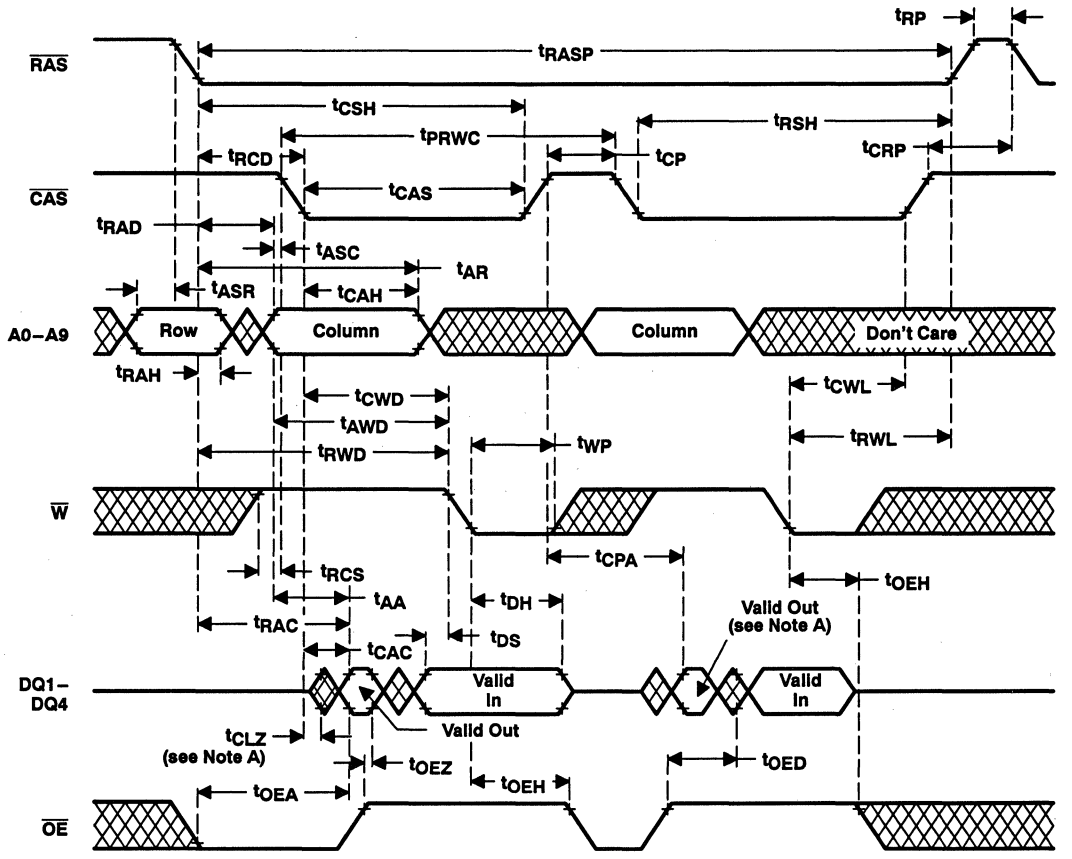
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Valid data is presented at the outputs after all access times are satisfied but can go from the high-impedance state to an invalid-data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ and $\overline{OE}$ are low.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

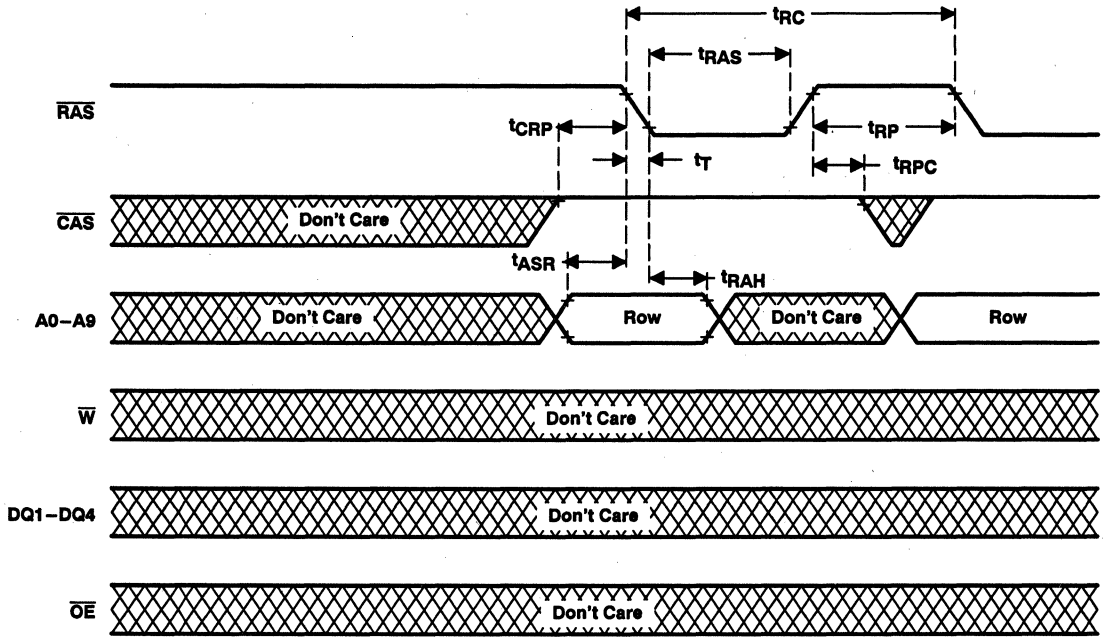


Figure 9. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

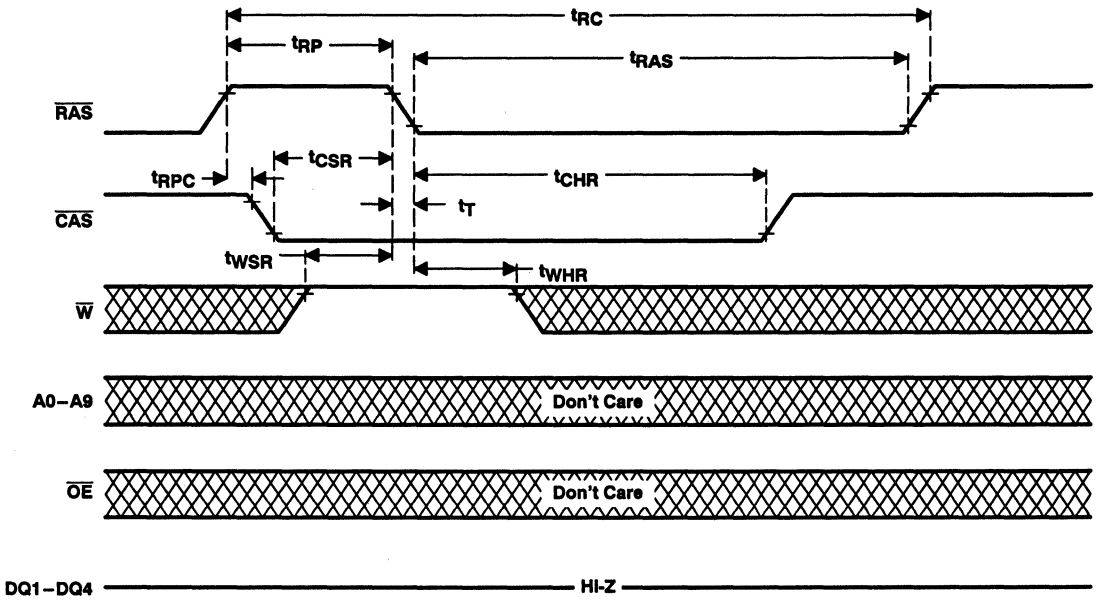
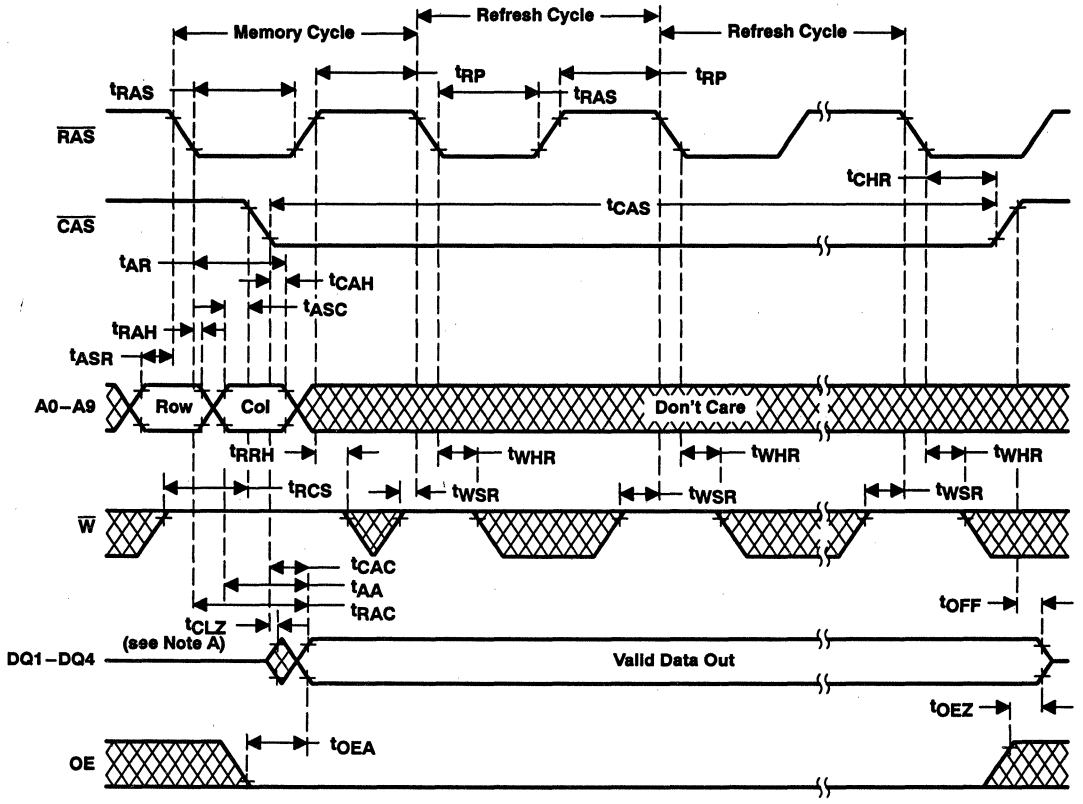


Figure 10. Automatic-CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the outputs after all access times are satisfied but can go from the high-impedance state to an invalid-data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ and $\overline{OE}$ are low.

Figure 11. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

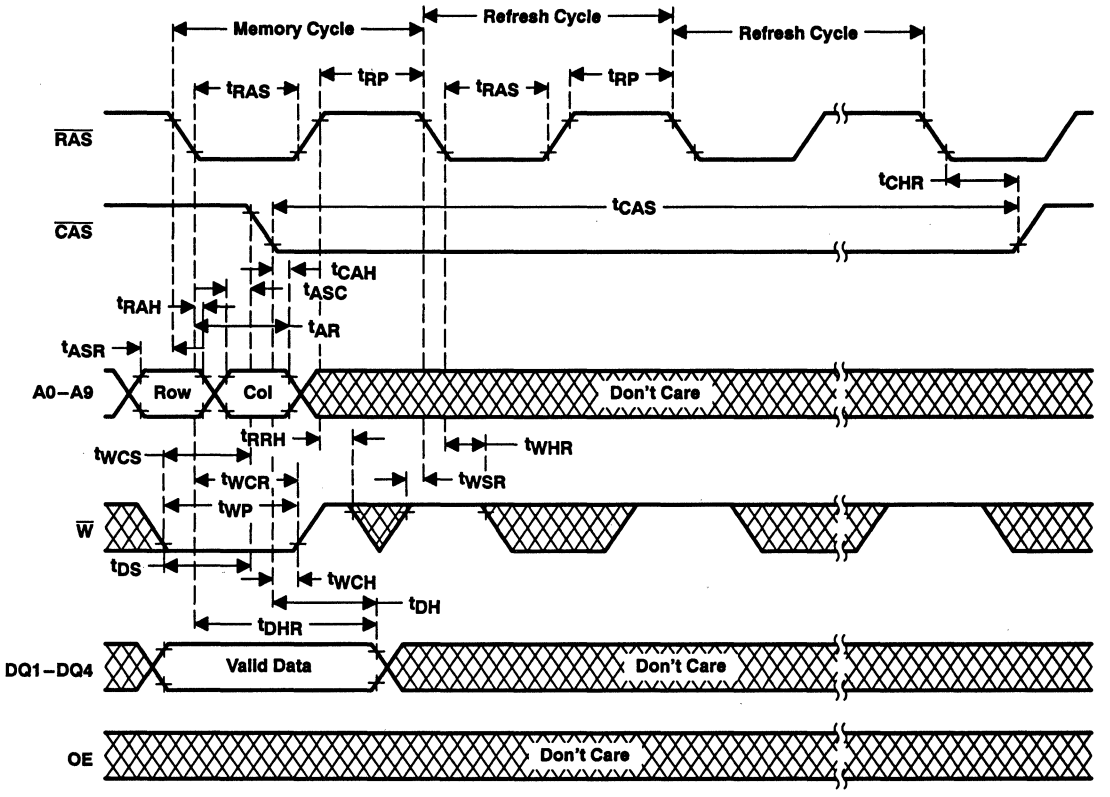


Figure 12. Hidden-Refresh-Cycle (Write) Timing

- **Organization . . . 16777216 × 1 Bits**
- **Single 5-V Power Supply (10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
'416100-70	70 ns	18 ns	35 ns	130 ns
'416100-80	80 ns	20 ns	40 ns	150 ns
'416100-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page-Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period:**
  4096 Cycles Refresh In 32 ms
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs, Outputs and Clocks Are TTL Compatible**
- **Operating Free-Air Temperature Range:**
  – 55°C to 125°C

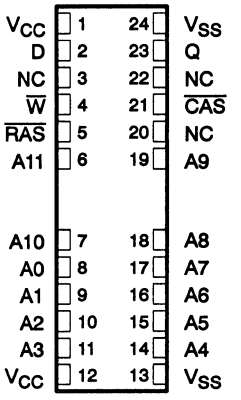
description

The SMJ416100 series is a set of high-speed 16777216-bit dynamic random-access memories (DRAMs), organized as 16777216-bit words by one bit each. They employ enhanced performance implanted CMOS (EPIC™) technology for high performance, reliability, and low power. These devices feature maximum $\overline{RAS}$ access times of 70 ns, 80 ns, and 10 ns.

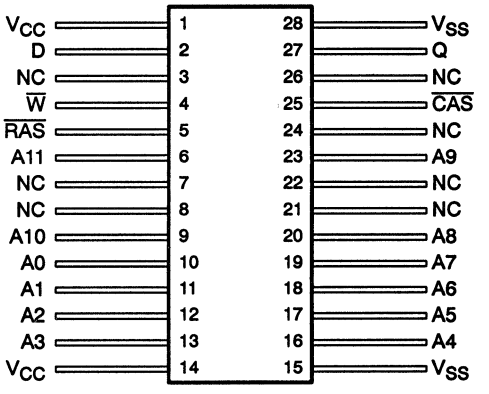
All inputs, outputs, and clocks are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ416100 is offered in a 450-mil 24/28-terminal surface-mount small-outline leadless chip carrier (FNC suffix) and a 450-mil 28-lead flatpack (HKB suffix). The packages are characterized for operation from – 55°C to 125°C.

FNC PACKAGE
(TOP VIEW)



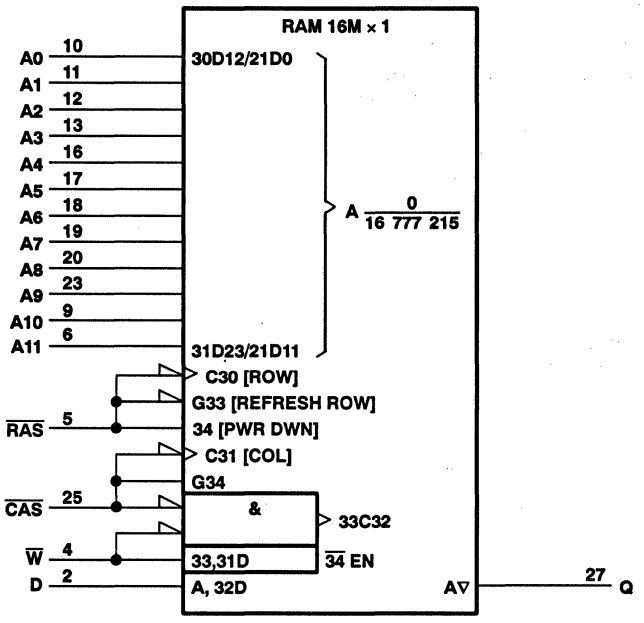
HKB PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Internal Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

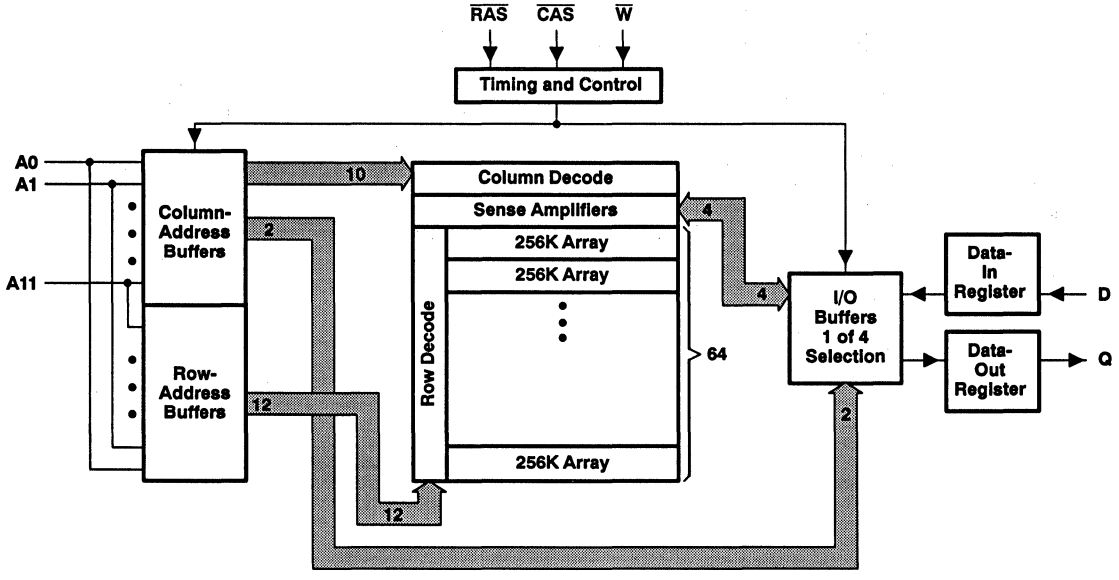
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



operation

enhanced page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. The time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$ low time.

The column-address buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output-enable. This feature allows the SMJ416100 to operate at a higher data bandwidth than conventional page-mode parts because retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after row-address hold time is satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} maximum (access time from $\overline{CAS}$ low) if t_{AA} maximum (access time from column address) and t_{RAC} are satisfied. If the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0–A11)

Twenty-four address bits are required to decode 1 of 16777216 storage-cell locations. Twelve row-address bits are set up on inputs A0 through A11 and latched during a normal access and during $\overline{RAS}$-only refresh as the device requires 4096 refresh cycles. Twelve column-address bits are set up on A0 through A11 and latched onto the chip by $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. $\overline{W}$ can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ is already low and data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The 3-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 54 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle, the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to the high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change but retains the state just read.

refresh

A refresh operation must be performed at least once every 32 ms to retain data by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, conserving power because the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden-refresh cycle. The external address is ignored and the hidden-refresh address is generated internally.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR-refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 1 V to 7 V
Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... – 55°C to 125°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	– 55		125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'416100-70		'416100-80		'416100-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		80		70		60	mA
I_{CC2}	Standby current	After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2	mA
		After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only refresh or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only refresh), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		80		70		60	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		65		60		55	mA
I_{CC7}	Standby current output enable (see Note 5)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled		5		5		5	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}
5. Measured with indicated conditions following a normal read cycle

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A11 †		9	pF
$C_{i(D)}$	Input capacitance, D †		8	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$ †		8	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ †		8	pF
C_o	Output capacitance †		14	pF

† Input capacitance for ZIP (SV suffix) package is 12 pF.

NOTE 6: Capacitance is sampled only at initial design and after any major changes. Samples are tested at 0 V and 25°C with a 1-MHz signal applied to the terminal under test. All other terminals are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		'416100-70		'416100-80		'416100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		18		20		25	ns
t_{CPA}	Access time from column precharge		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		18		18		18	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 8)	0	18	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 8)	0	18	0	20	0	25	ns

NOTES: 7. Valid data is presented at the output after all access times are satisfied. Valid data can go from the high-impedance state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

8. t_{OFF} is specified when the output is no longer driven. The output is disabled by bringing $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'416100-70		'416100-80		'416100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 9)	130		150		180		ns
t_{RWC}	Cycle time, read-write (see Note 9)	153		175		210		ns
t_{PC}	Cycle time, page mode read or write (see Notes 9 and 10)	45		50		55		ns
t_{PRWC}	Cycle time, page mode read-write (see Note 9)	68		75		85		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 11)	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 11)	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 12)	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		70		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 13)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	18		20		25		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	18		20		25		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	15		15		15		ns
t_{DH}	Hold time, data (see Note 13)	15		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 14)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 14)	0		0		5		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low (early-write operation only)	15		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	40		45		50		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)	35		40		45		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-write operation only)	18		20		25		ns

NOTES: 9. All cycle times assume t_T = 5 ns, referenced to V_{IH}(min) and V_{IL}(max).
10. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
11. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
12. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
13. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'416100-70		'416100-80		'416100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)	70		80		100		ns
t_{CPW}	Delay time, $\overline{W}$ low after $\overline{CAS}$ precharge (read-write operation only)	40		45		50		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time (see Note 16)							

NOTES: 15. The maximum value is specified only to assure access time.
16. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 30 ns.

PARAMETER MEASUREMENT INFORMATION

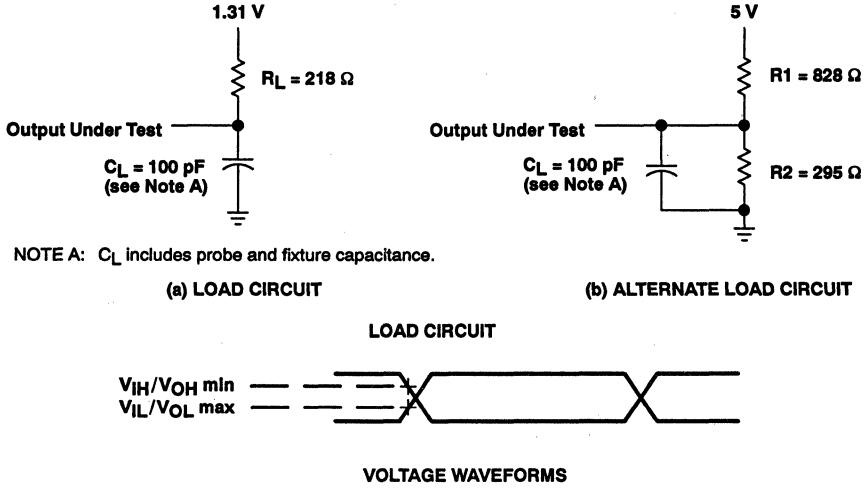
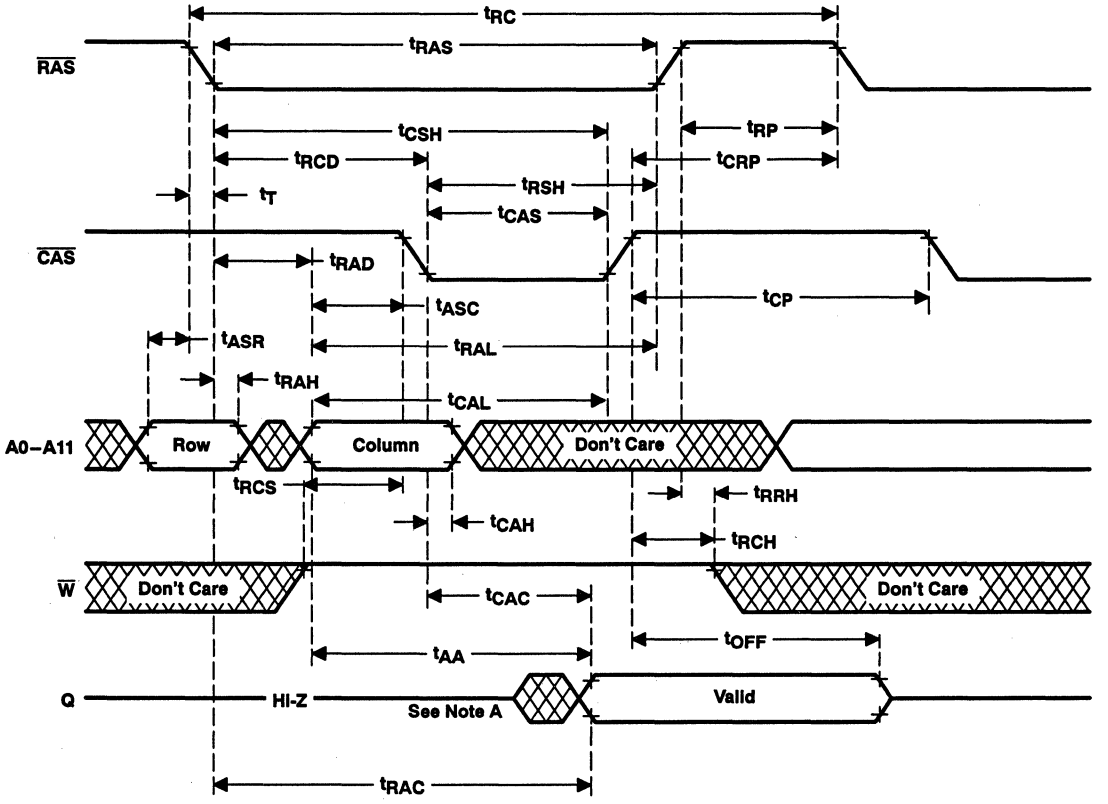


Figure 1. Load Circuits and Voltage Waveforms

The ac timing parameters are specified with reference to the minimum valid high-level voltage and the maximum valid low-level voltage for each signal. This corresponds to 2.4 V and 0.8 V for inputs; 2.4 V and 0.4 V for outputs with the given load circuit.

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

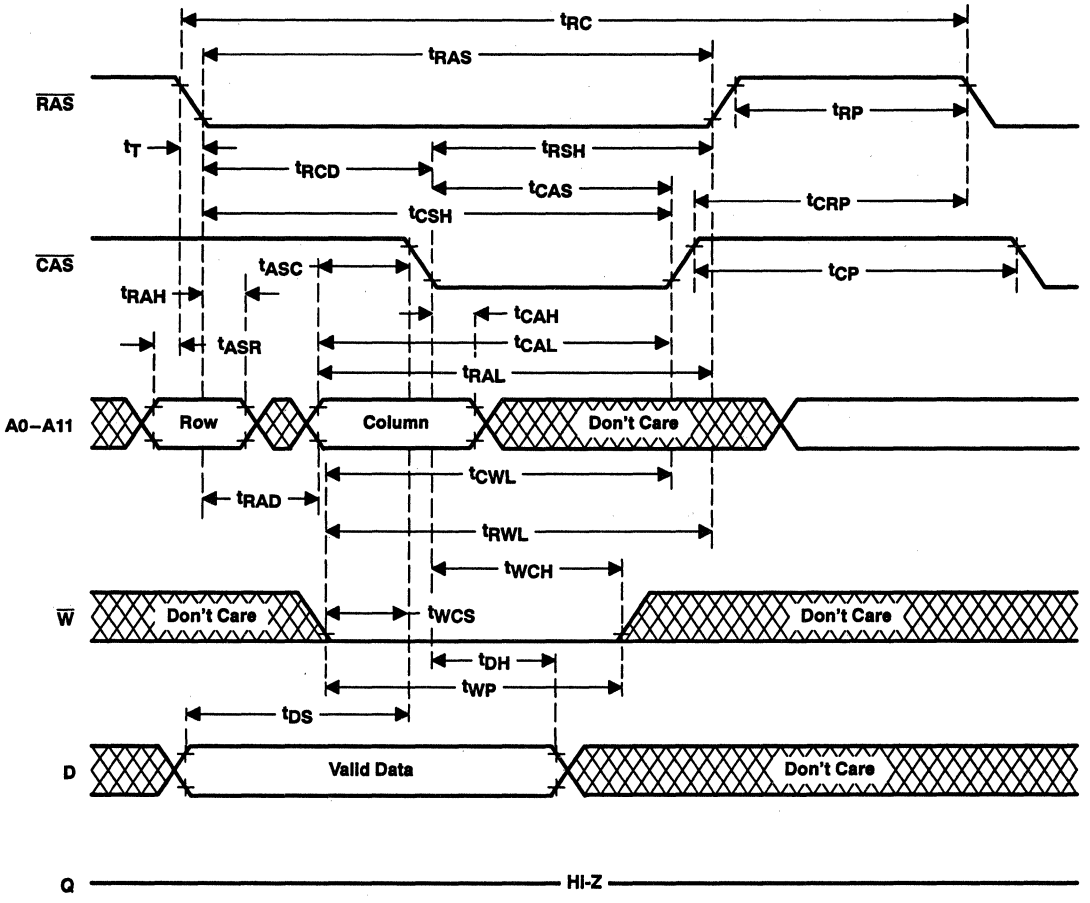


Figure 3. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

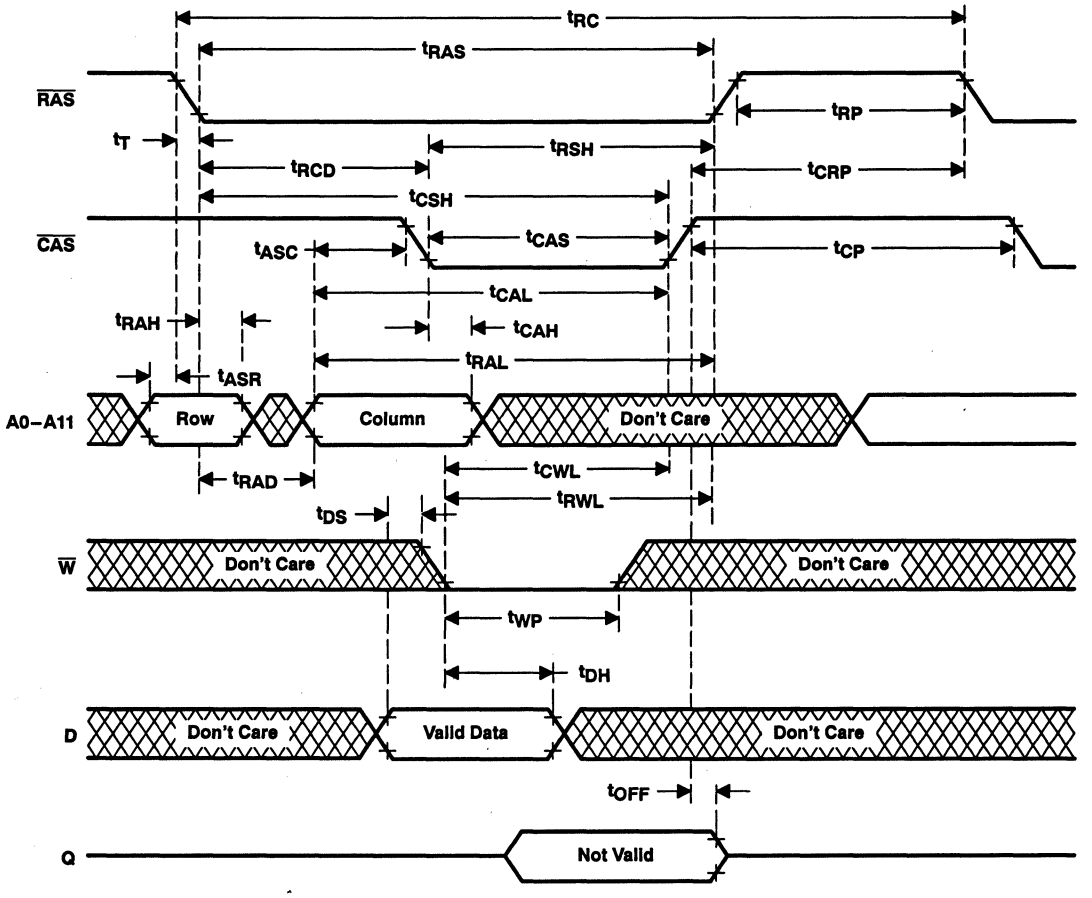
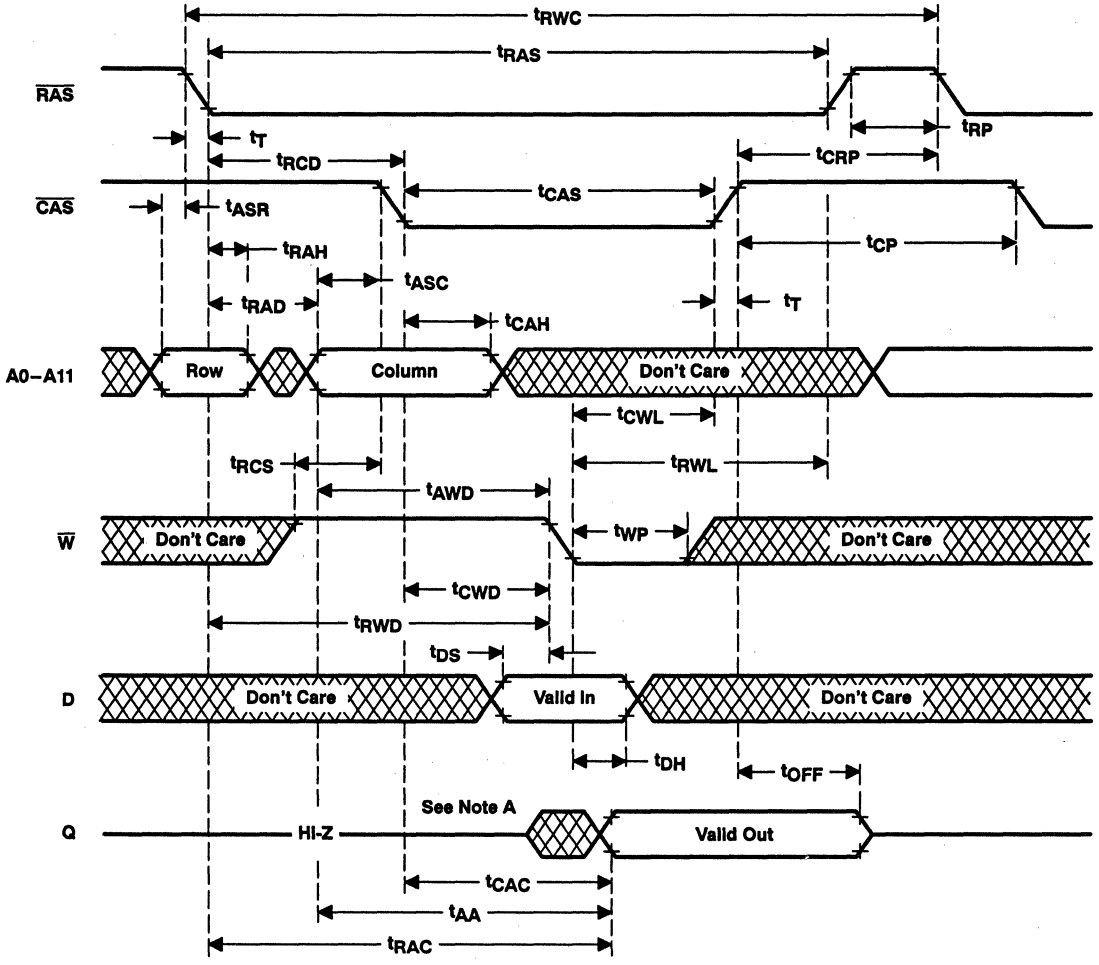


Figure 4. Write-Cycle Timing

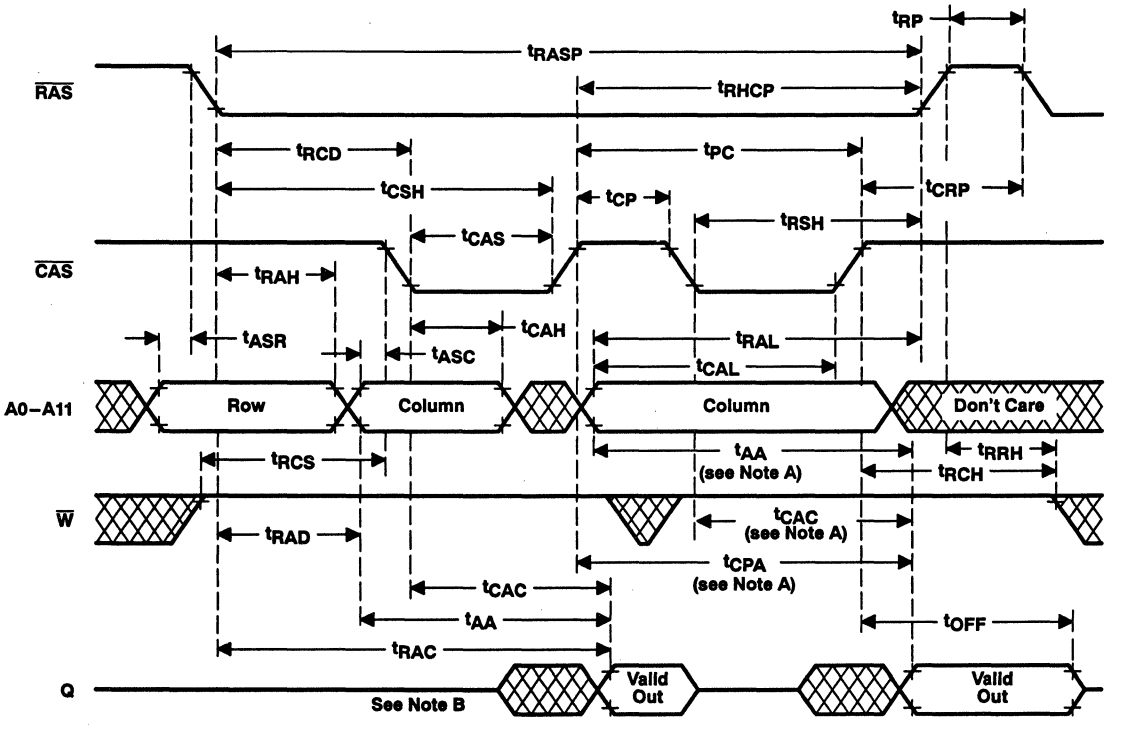
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 5. Read-Write-Cycle Timing

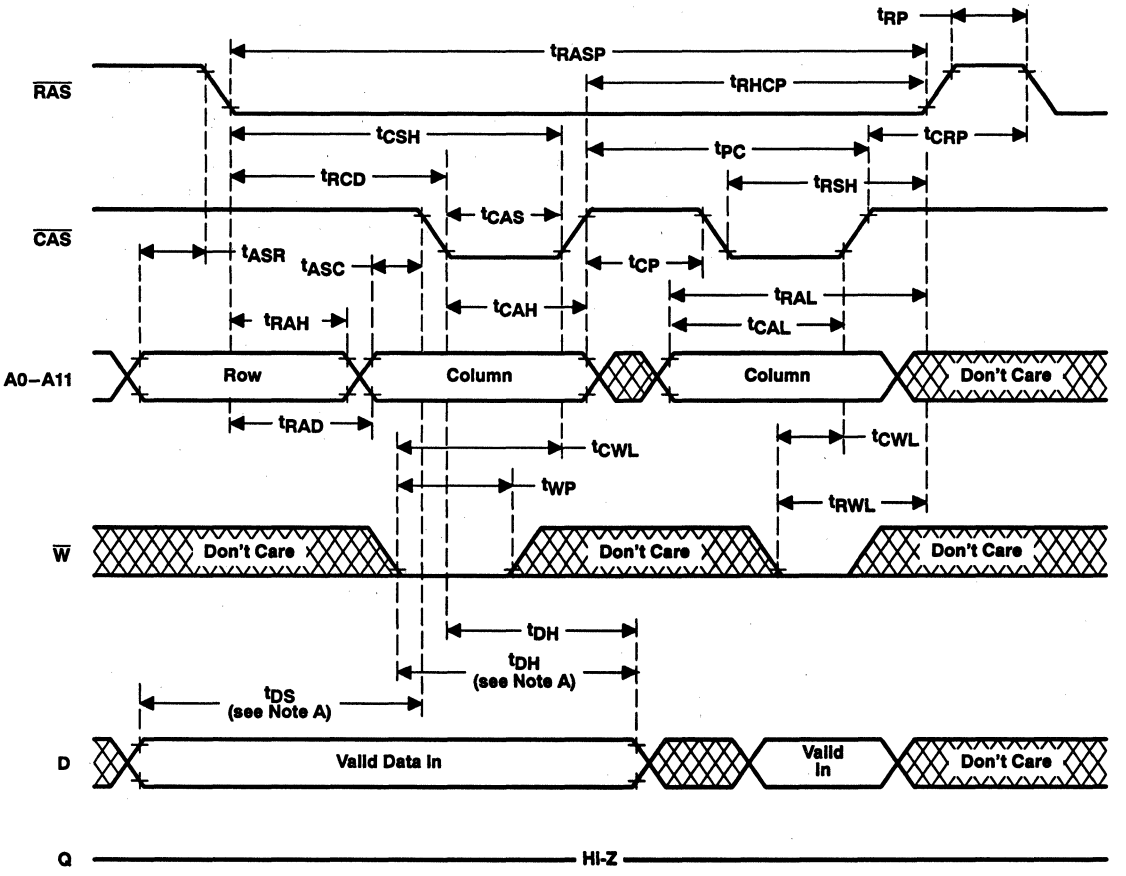
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Access time is t_{CPA}, t_{CAC} or t_{AA} dependent.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

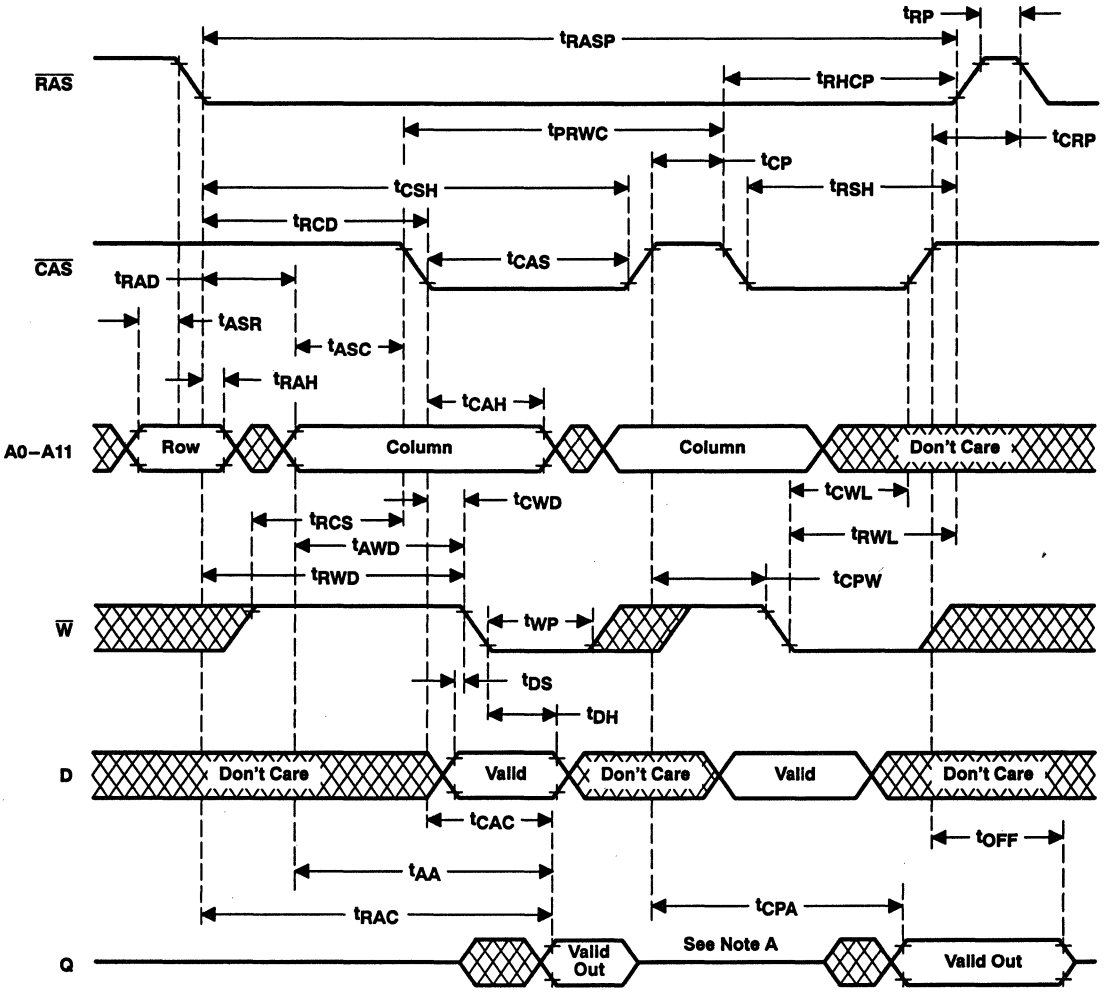
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

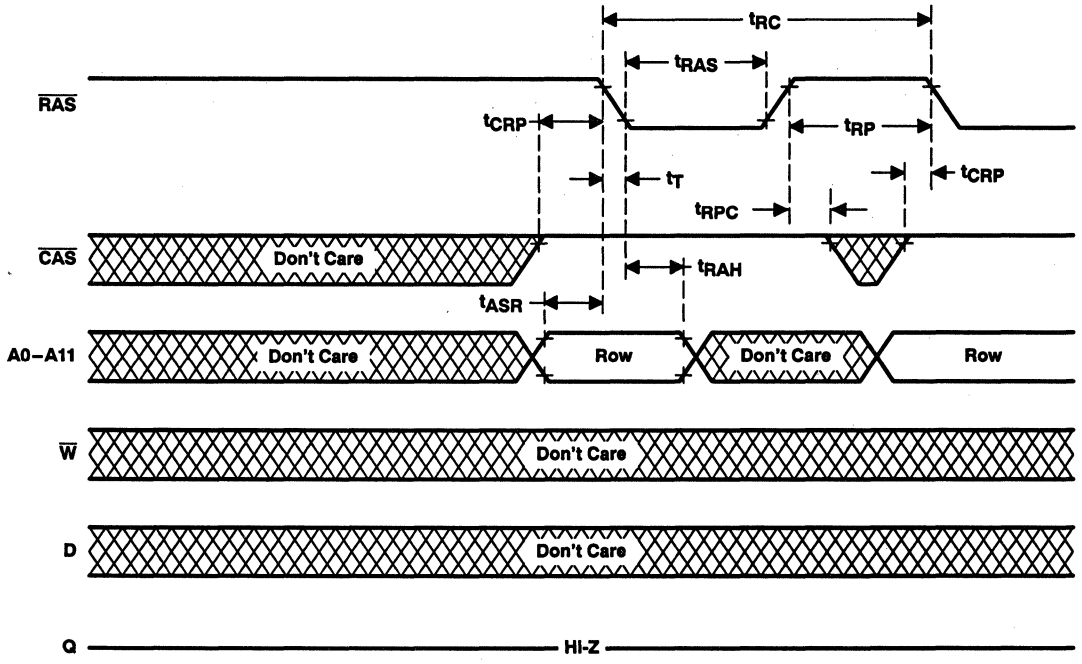


Figure 9. $\overline{\text{RAS}}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

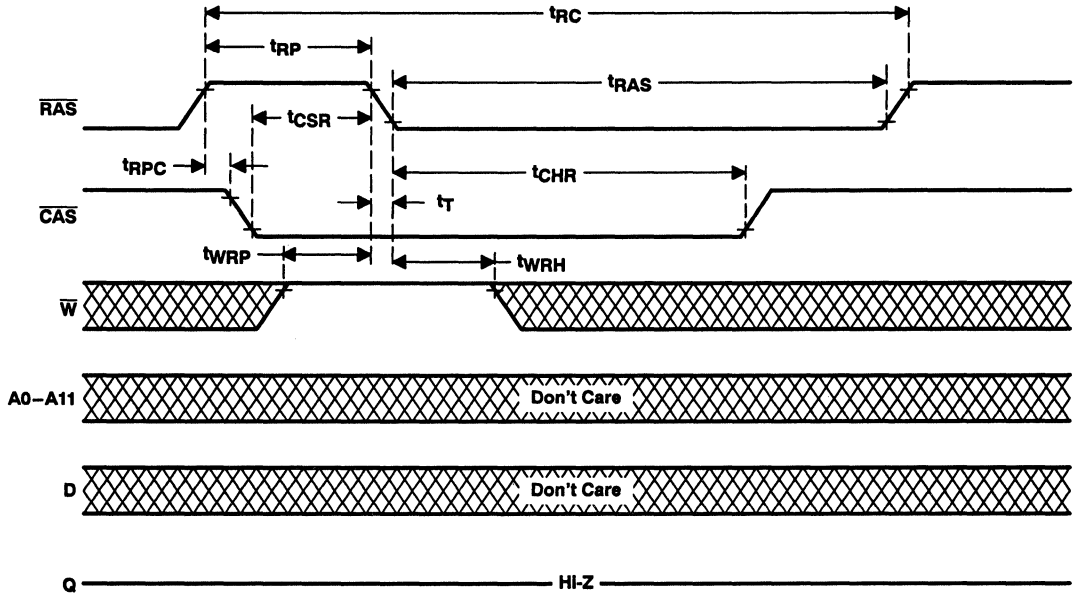


Figure 10. Automatic-CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

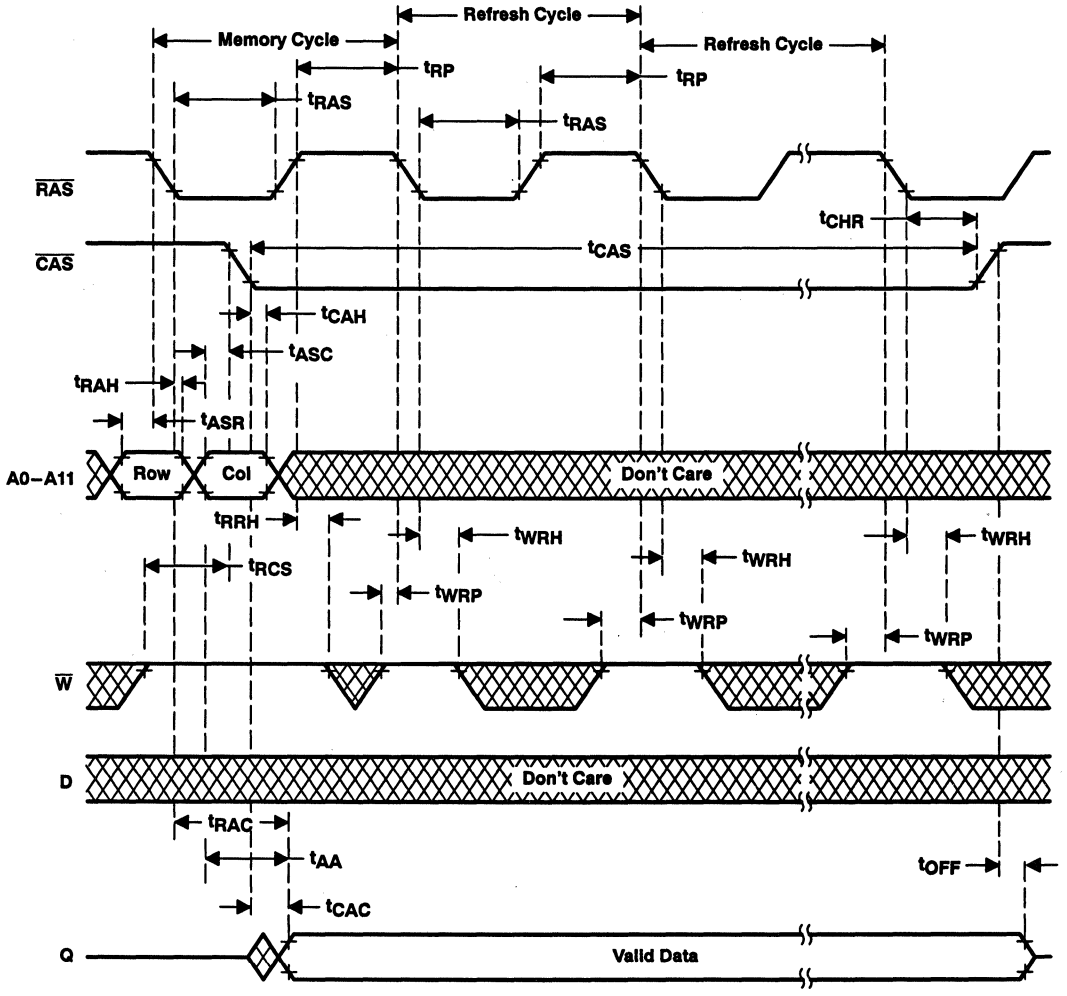


Figure 11. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

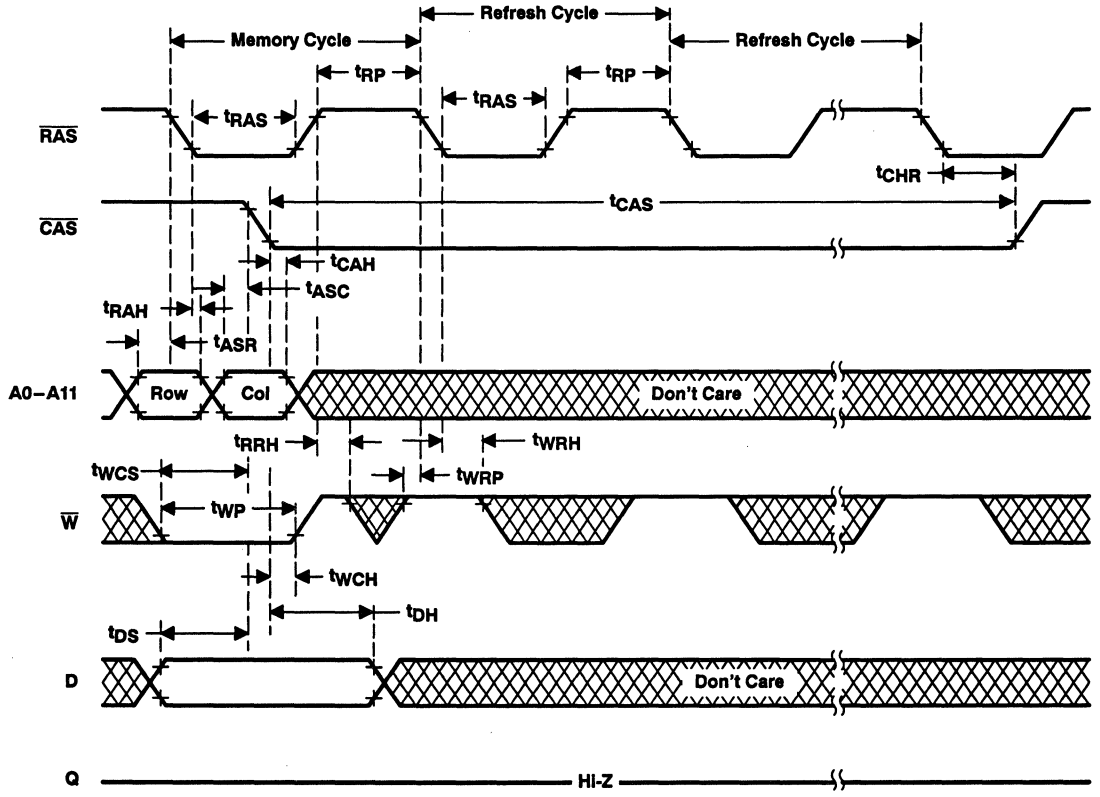


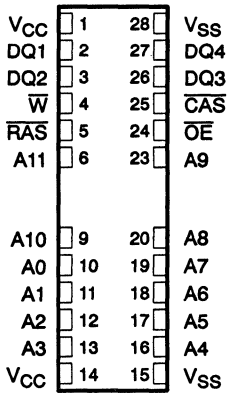
Figure 12. Hidden-Refresh-Cycle (Write) Timing

- **Organization . . . 4194304 × 4**
- **Single 5-V Power Supply (10% Tolerance)**
- **Performance Ranges:**

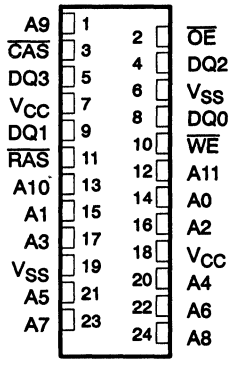
	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
'416400-70	70 ns	18 ns	35 ns	130 ns
'416400-80	80 ns	20 ns	40 ns	150 ns
'416400-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page-Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  4096 Cycles Refresh In 32 ms
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **Operating Free-Air Temperature Range**
  – 55°C to 125°C

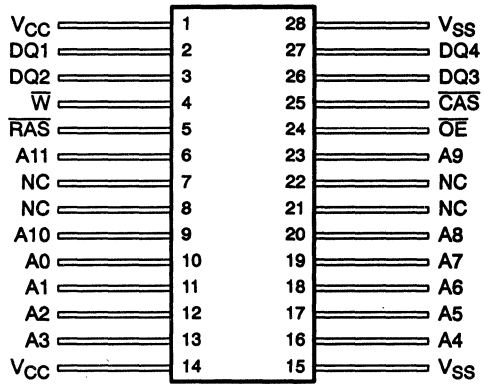
FNC PACKAGE
(TOP VIEW)



SV PACKAGE
(TOP VIEW)



HKB PACKAGE
(TOP VIEW)



description

The SMJ416400 series is a set of high-speed 16777216-bit dynamic random-access memories (DRAMs), organized as 4194304 words by four bits each. They employ enhanced performance implanted CMOS (EPIC™) technology for high performance, reliability, and low power.

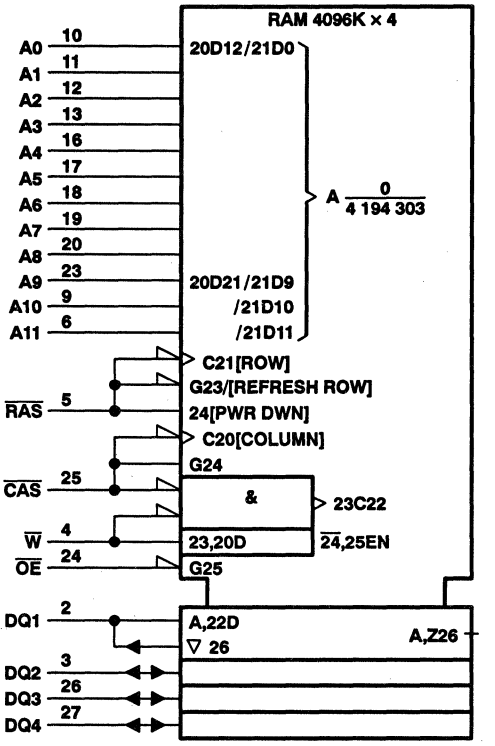
These devices feature maximum $\overline{RAS}$ access times of 70 ns, 80 ns, and 100 ns. All inputs, outputs, and clocks are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ416400 is offered in 450-mil 24/28-pin surface-mount small-outline leadless-chip carrier (FNC suffix), 28-lead flatpack (HKB suffix), and 24-lead ZIP (SV suffix) packages. The packages are characterized for operation from –55°C to 125°C.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

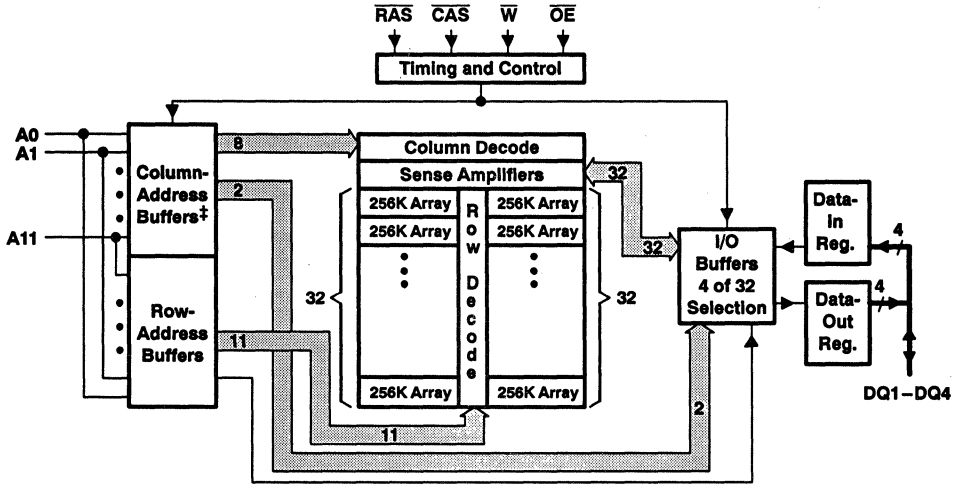
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FNC and HKB packages.

functional block diagram



‡ Column address 10 and column address 11 are not used.

operation

enhanced page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. The time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$ low width.

The column-address buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable. This feature allows the SMJ416400 to operate at a higher data bandwidth than conventional page-mode parts because retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as enhanced page mode. Valid column address can be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} maximum (access time from $\overline{CAS}$ low) if t_{AA} maximum (access time from column address) and t_{OEA} have been satisfied. When the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0–A11)

Twenty-two address bits are required to decode 1 of 4194304 storage-cell locations. Twelve row-address bits are set on inputs A0 through A11 and latched onto the chip by the row-address strobe, $\overline{RAS}$. Ten column-address bits are set on A0 through A9 and latched onto the chip by the column-address strobe, $\overline{CAS}$. Row address A11 is required during a normal access and during $\overline{RAS}$-only refresh as the device requires 4096 refresh cycles. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. $\overline{W}$ can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early-write operation to be completed with $\overline{OE}$ grounded.

data-in/data-out (DQ1–DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In the early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ is already low; data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

The 3-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two series 54 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle, the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to the high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. Both $\overline{RAS}$ and $\overline{CAS}$ must be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, the output buffers remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every 32 ms to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden-refresh cycle. An internal-refresh address provides the refresh address during hidden refresh.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

absolute maximum ratings over operating free-air temperature†

Supply voltage range, V_{CC} ..... –1 V to 7 V
Voltage range on any pin (see Note 1) ..... –1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... –55°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	–55		125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'416400-70		'416400-80		'416400-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note)	V_{CC} = 5.5 V, Minimum cycle		80		70		60	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2		2		2	mA
		V_{IH} = V_{CC} – 0.05 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)†	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		80		70		60	mA
I_{CC4}	Average page current (see Note 4)†	$\overline{RAS}$ low, $\overline{CAS}$ cycling		65		60		55	mA
I_{CC7}	Standby current output enable†	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled		5		5		5	mA

† Minimum cycle, V_{CC} = 5.5 V

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A11‡		9	pF
$C_{i(RC)}$	Input capacitance, $\overline{RAS}$ and $\overline{CAS}$‡		8	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$‡		8	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$‡		8	pF
C_o	Output capacitance		14	pF

‡ Input capacitance for ZIP (SV suffix) package is 12 pF.

NOTE 5: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25°C with a 1-MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 6)

PARAMETER		'416400-70		'416400-80		'416400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		18		20		25	ns
t_{CPA}	Access time from column precharge		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		18		20		25	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 7)	0	18	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 7)	0	18	0	20	0	25	ns

NOTES: 6. Valid data is presented at the outputs after all access times are satisfied but can go from the high-impedance state to an invalid-data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.
7. t_{OFF} and t_{OEZ} are specified when the outputs are no longer driven. The outputs are disabled by bringing either $\overline{OE}$ or $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'416400-70		'416400-80		'416400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 8)	130		150		180		ns
t_{RWC}	Cycle time, read-write (see Note 8)	181		205		245		ns
t_{PC}	Cycle time, page mode read or write (see Notes 8 and 9)	45		50		55		ns
t_{PRWC}	Cycle time, page mode read-write (see Note 8)	96		105		120		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 10)	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 10)	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 11)	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		70		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 12)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	18		20		25		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	18		20		25		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	15		15		15		ns
t_{DH}	Hold time, data (see Note 12)	15		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 13)	0		0		5		ns

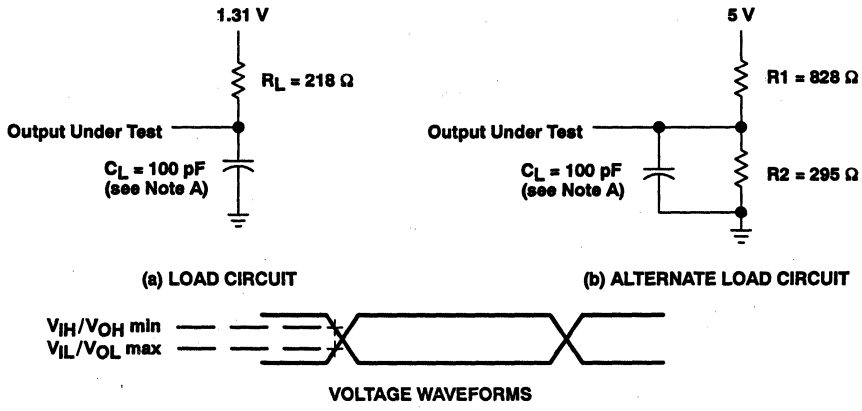
NOTES: 8. All cycle times assume t_T = 5 ns, referenced to $V_{IH(min)}$ and $V_{IL(max)}$.
9. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'416400-70		'416400-80		'416400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low (early-write operation only)	15		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{OEH}	Hold time, $\overline{OE}$ command	18		20		25		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	10		10		10		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	40		45		50		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)	63		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-write operation only)	46		50		60		ns
t_{OED}	Delay time, $\overline{OE}$ to data	18		20		25		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 14)	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)	98		110		135		ns
t_{CPW}	Delay time, $\overline{W}$ low after $\overline{CAS}$ precharge (read-write operation only)	63		70		80		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time (see Note 15)							

NOTES: 14. The maximum value is specified only to assure access time.
15. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 30 ns.

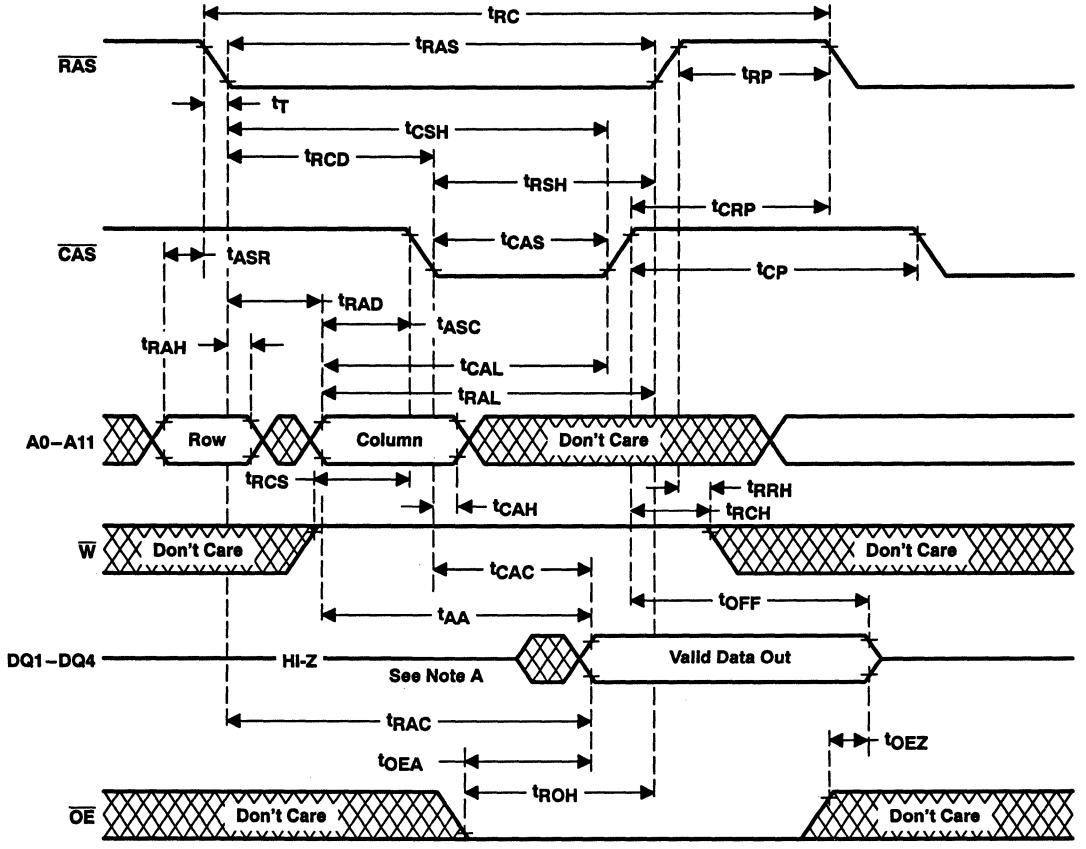
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and fixture capacitance.
B. The ac timing parameters are specified with reference to the minimum valid high-level voltage and the maximum valid low-level voltage for each signal. This corresponds to 2.4 V and 0.8 V for inputs; 2.4 V and 0.4 V for outputs with the given load circuit.

Figure 1. Load Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

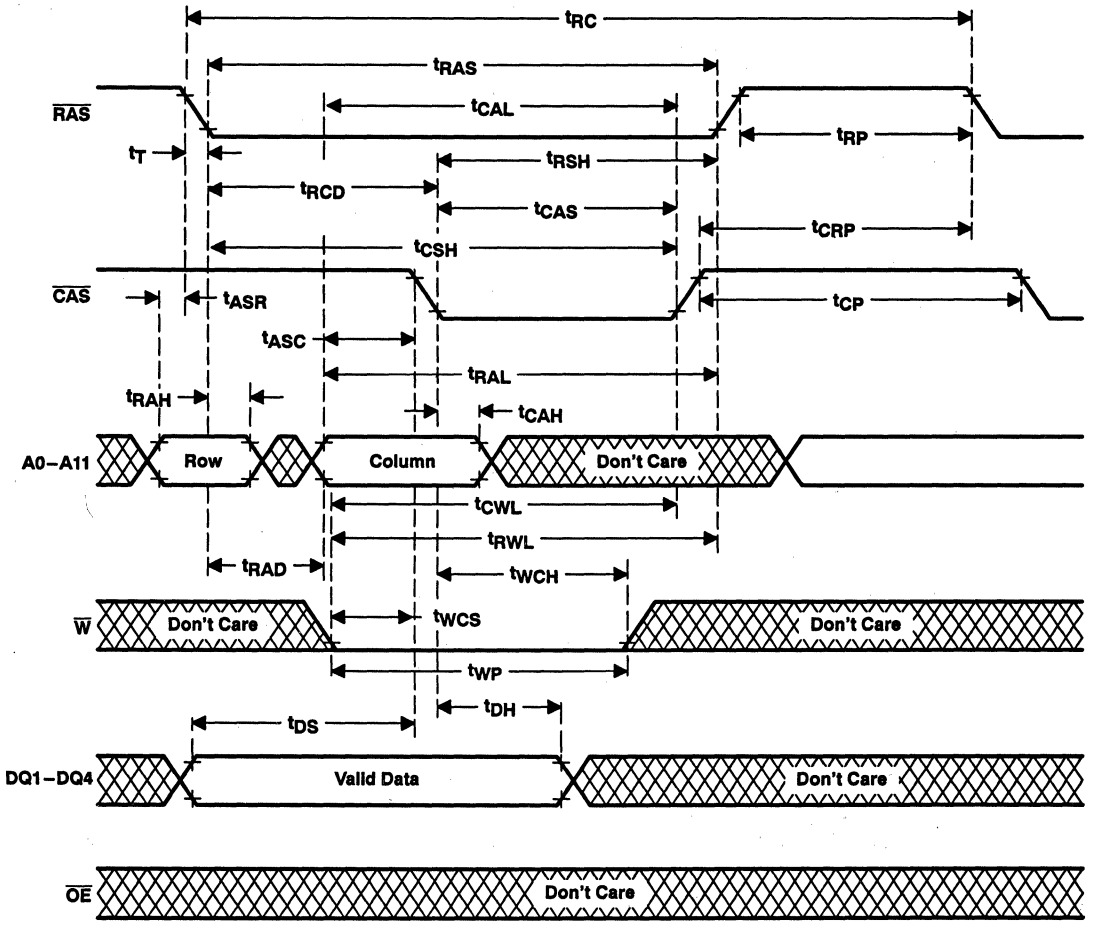


Figure 3. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

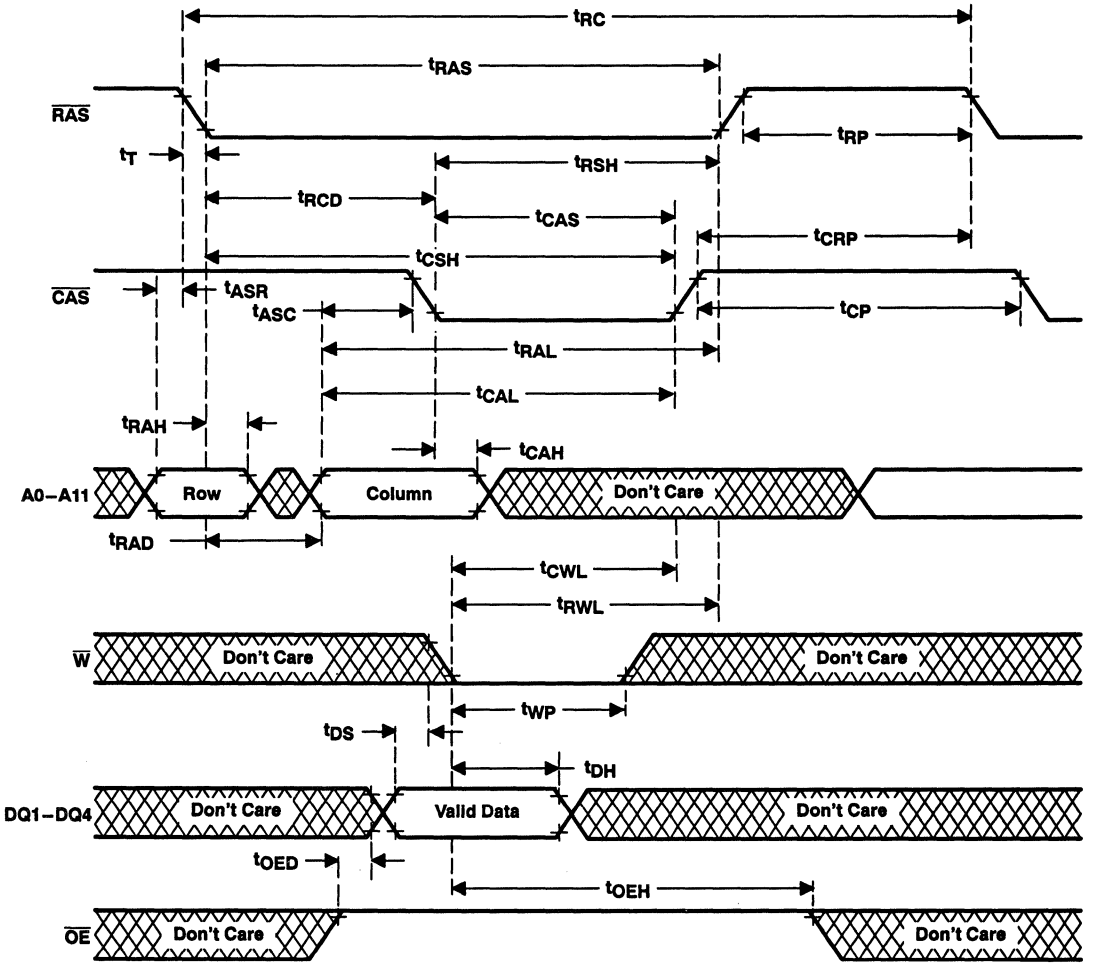
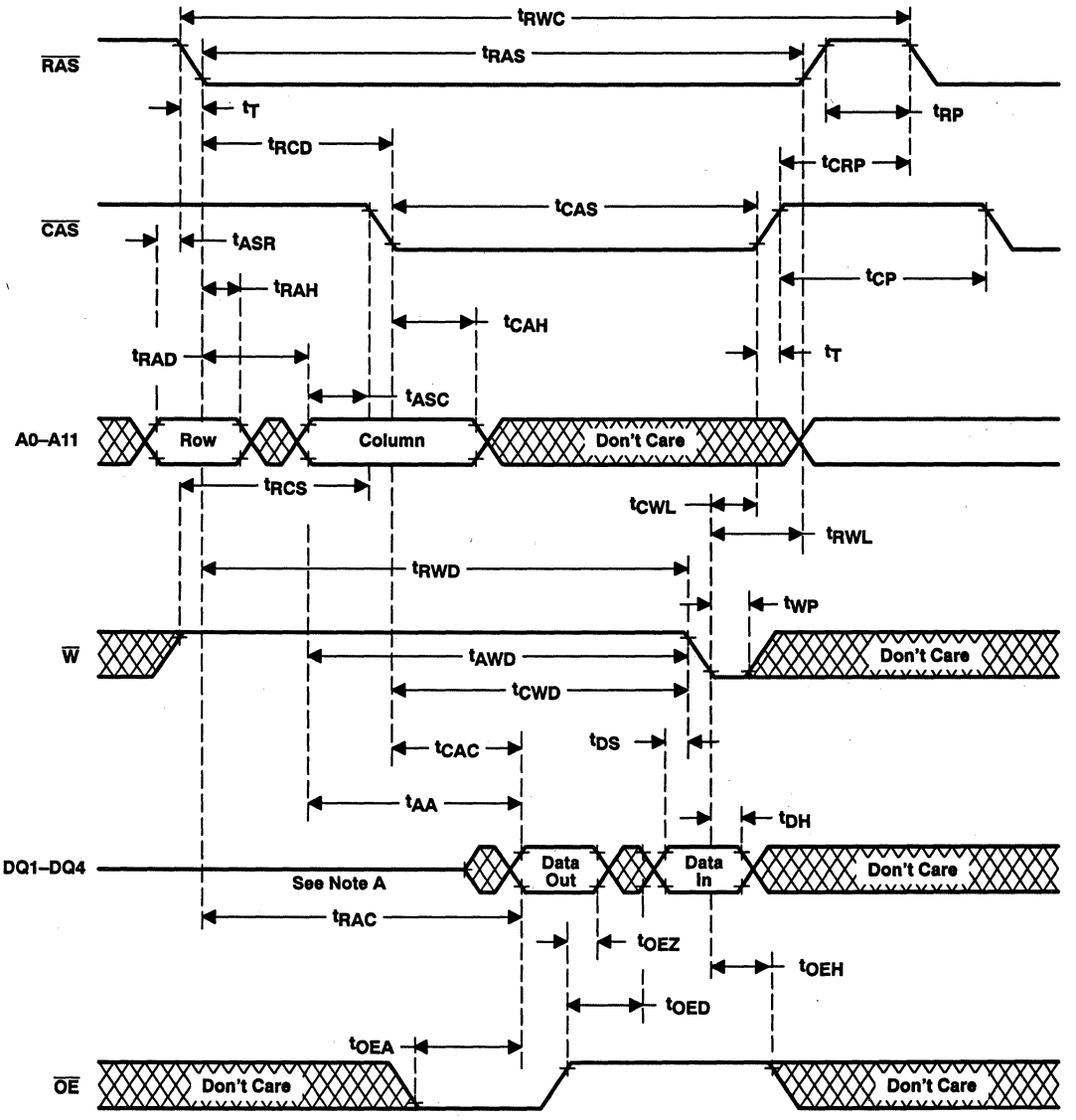


Figure 4. Write-Cycle Timing

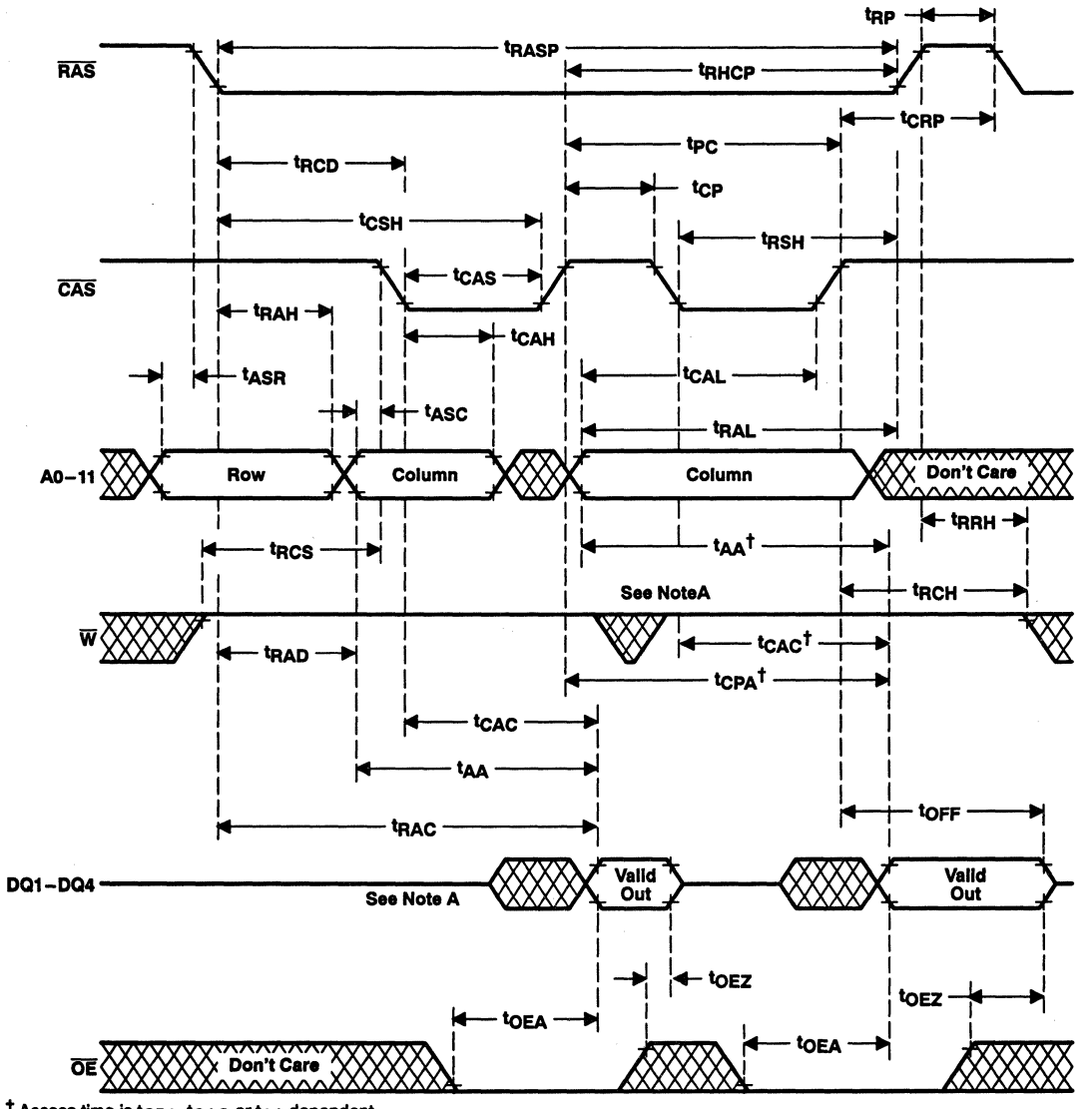
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 5. Read-Write-Cycle Timing

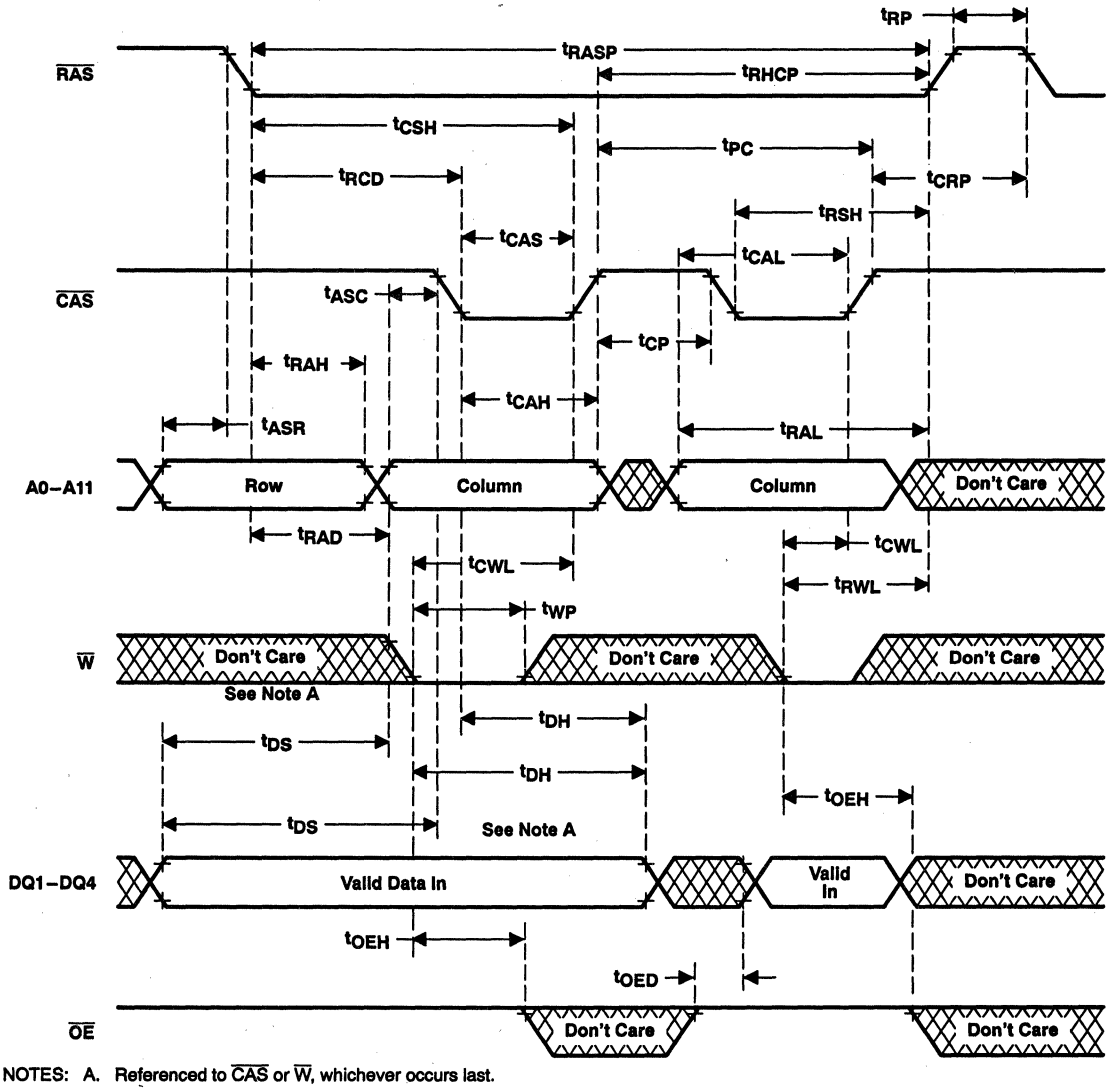
PARAMETER MEASUREMENT INFORMATION



† Access time is t_{CPA}, t_{CAC} or t_{AA} dependent.
NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

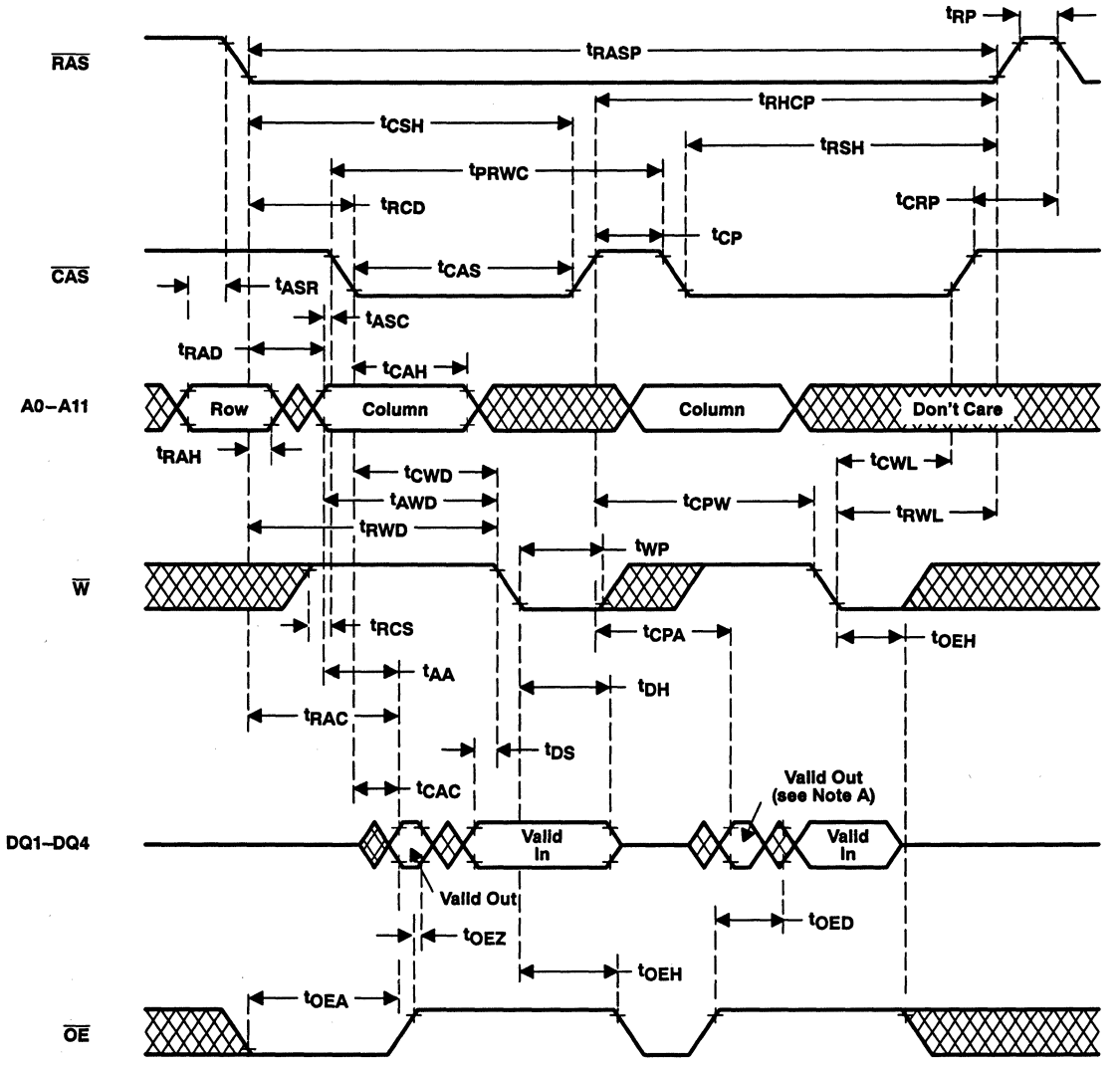
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with a write cycle as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

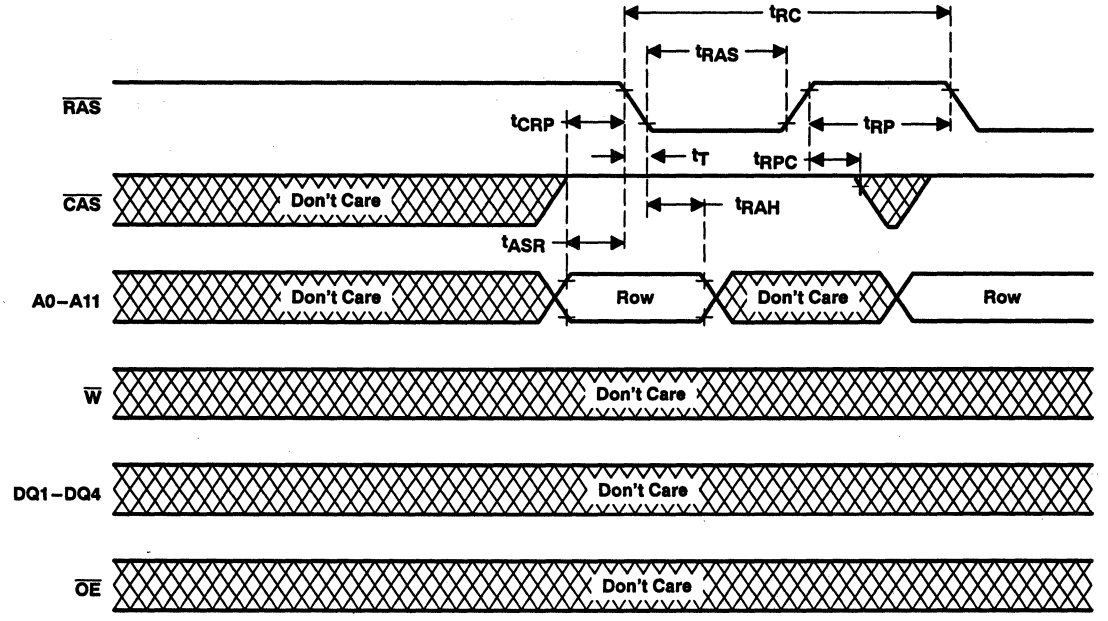


Figure 9. $\overline{RAS}$-Only Refresh Timing

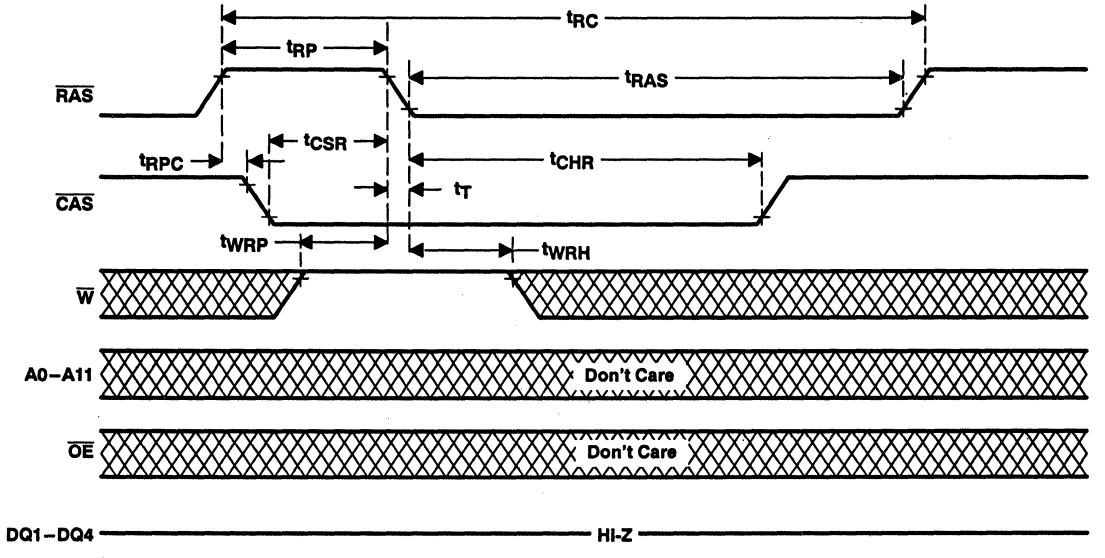


Figure 10. Automatic-CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

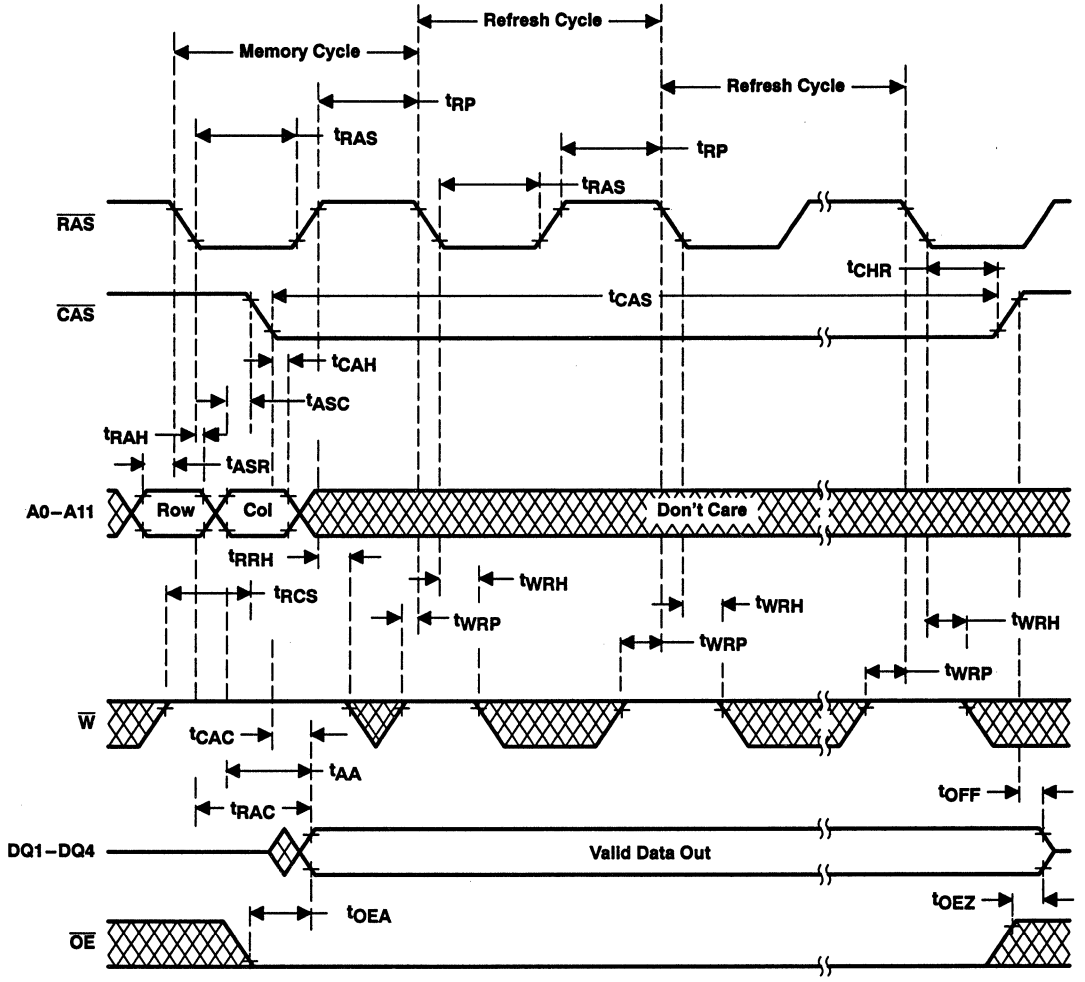


Figure 11. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

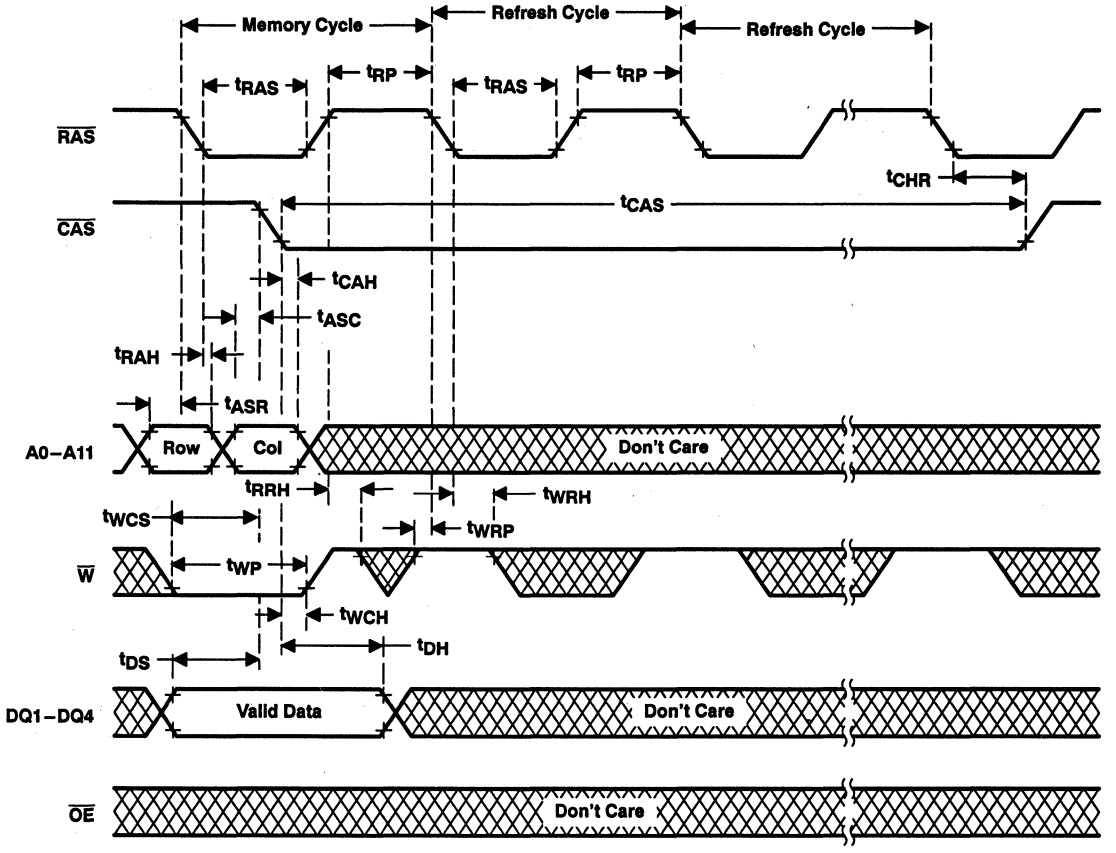


Figure 12. Hidden-Refresh-Cycle (Write) Timing

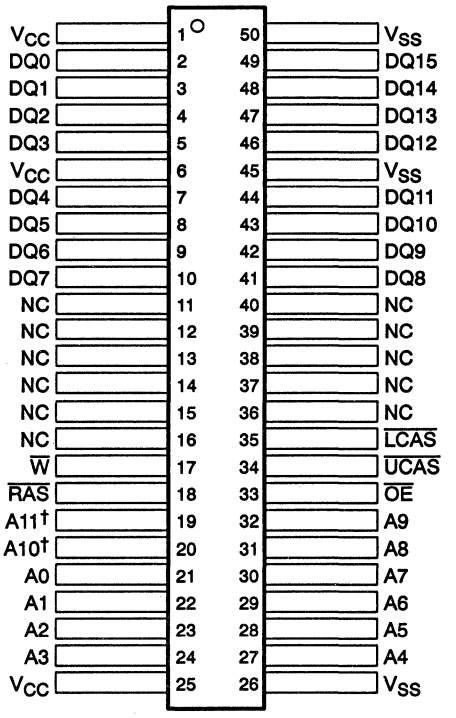
SGMS720A – APRIL 1995 – REVISED JUNE 1995

- **Organization . . . 1048576 × 16**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'41x160-60	60 ns	15 ns	30 ns	110 ns
'41x160-70	70 ns	18 ns	35 ns	130 ns
'41x160-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page-Mode Operation for Faster Memory Access**
- **$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ (CBR) Refresh**
- **Long Refresh Period**
  - **'416160 – 4096 Cycle Refresh In 32 ms (Max)**
  - **'418160 – 1024 Cycle Refresh In 8 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range –55°C to 125°C**
- **Texas Instruments Enhanced Performance Implanted CMOS (EPIC™) Process**
- **All Inputs/Outputs Are TTL Compatible**
- **Packaging**
  50-Lead, 650-Mil-Wide Ceramic Flatpack

XXX PACKAGE
(TOP VIEW)



† A10 and A11 are NC for SMJ418160.

description

The SMJ41x160 series is a set of high-speed, 16777216-bit dynamic random-access memories organized as 1048576 words of 16-bits each.

They employ state-of-the-art EPIC™ technology for high performance, reliability, and low power at low cost.

These devices feature maximum $\overline{\text{RAS}}$ access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ41x160 series is offered in a 50-lead, 650-mil-wide ceramic flatpack and is characterized for operation from –55°C to 125°C.

PIN NOMENCLATURE	
A0–A11	Address Inputs
DQ0–DQ15	Data In/Data Out
$\overline{\text{LCAS}}$	Lower Column-Address Strobe
$\overline{\text{UCAS}}$	Upper Column-Address Strobe
NC	No Internal Connection
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

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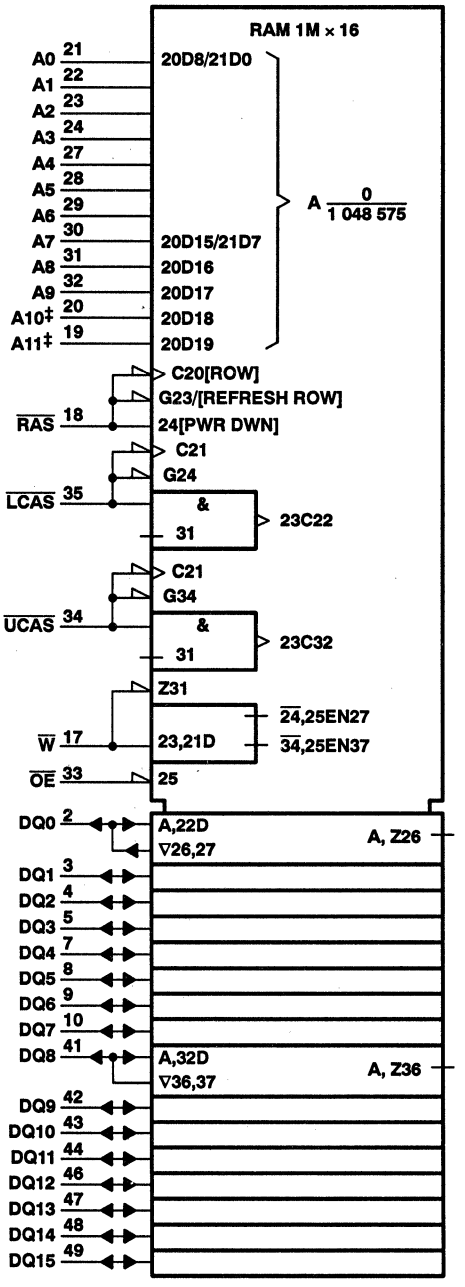
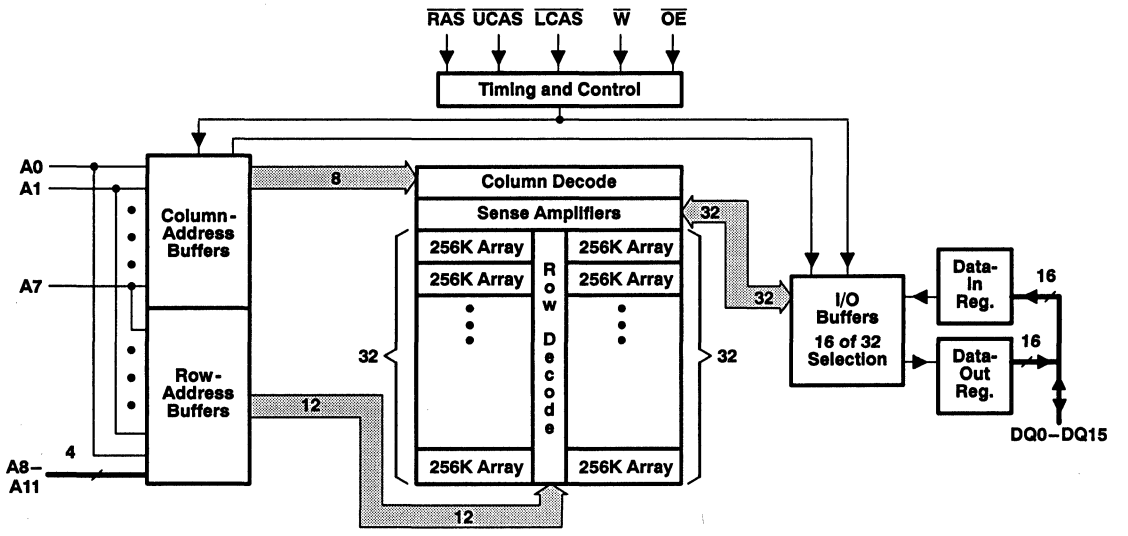
logic symbol†



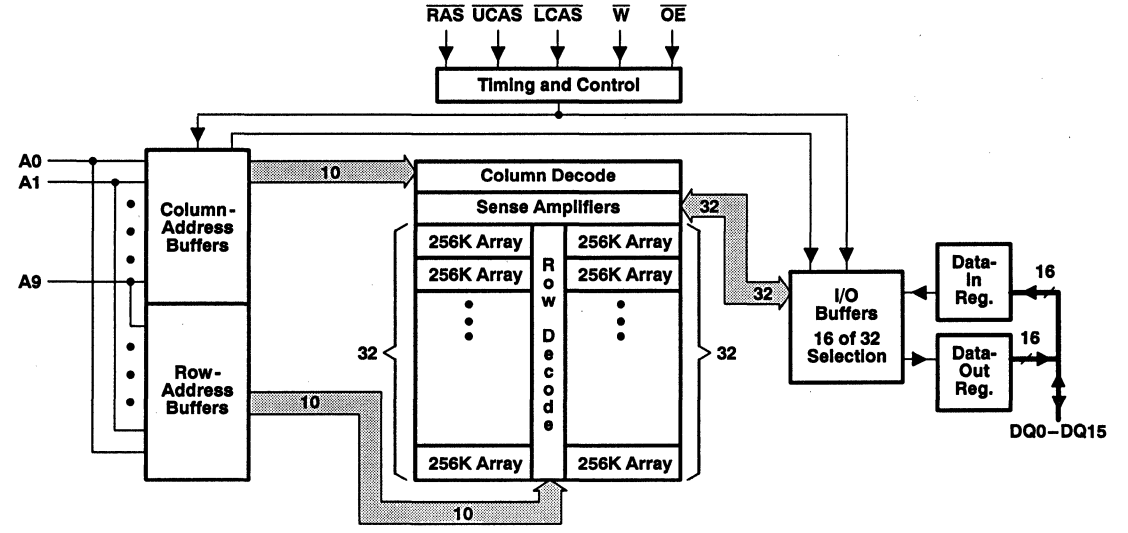
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
‡ A10 and A11 are NC for SMJ418160.

PRODUCT PREVIEW

'416160 functional block diagram



'418160 functional block diagram



PRODUCT PREVIEW

operation

dual $\overline{CAS}$

Two $\overline{CAS}$ terminals ($\overline{LCAS}$ and $\overline{UCAS}$) are provided to give independent control of the 16 data-I/O terminals (DQ0–DQ15), with $\overline{LCAS}$ corresponding to DQ0–DQ7 and $\overline{UCAS}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{xCAS}$ falling edge. Each $\overline{xCAS}$ going low enables its corresponding DQx pin with data associated with the column address latched on the first falling $\overline{xCAS}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{xCAS}$ edge.The delay time from $\overline{xCAS}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{xCAS}$ to its corresponding DQx terminal.

In order to latch in a new column address, both $\overline{xCAS}$ terminals must be brought high. The column-precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first $\overline{xCAS}$ falling edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

For early-write cycles, the data is latched on the first $\overline{xCAS}$ falling edge. Only the DQs that have the corresponding $\overline{xCAS}$ low are written into. Each $\overline{xCAS}$ must meet t_{CAS} minimum in order to ensure writing into the storage cell. To latch a new address and new data, all $\overline{xCAS}$ terminals must be high and meet t_{CP}.

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{xCAS}$ page-mode cycle time used. With minimum $\overline{xCAS}$ page-cycle time, all columns can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{xCAS}$ is high. The falling edge of the first $\overline{xCAS}$ latches the column addresses. This feature allows the device to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when $\overline{xCAS}$ transitions low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after t_{RAH} (row-address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{xCAS}$. In this case, data is obtained after t_{CAC} maximum (access time from $\overline{xCAS}$ low) if t_{AA} maximum (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{xCAS}$ goes high, minimum access time for the next cycle is determined by t_{CPA} (access time from rising edge of the last $\overline{xCAS}$).

address: A0–A11 ('416160) and A0–A9 ('418160)

Twenty address bits are required to decode one of the 1048576 storage cell locations. For the SMJ416160, 12 row-address bits are set up on A0 through A11 and latched onto the chip by $\overline{RAS}$. Eight column-address bits are set up on A0 through A7 and latched onto the chip by the first $\overline{xCAS}$. For the SMJ418160, 10 row address bits are set up on A0–A9 and latched onto the chip by $\overline{RAS}$. Ten column address bits are set up on A0–A9 and latched onto the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{OE}$ grounded.

PRODUCT PREVIEW

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{xCAS}$ and the data is strobed in by the first $\overline{xCAS}$ occurrence with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{xCAS}$ is already low and the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

data out (DQ0–DQ15)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{xCAS}$ to be brought low for the output buffers to go into the low-impedance state, and they remain in the low-impedance state until either $\overline{OE}$ or $\overline{xCAS}$ is brought high.

$\overline{RAS}$-only refresh '416160

A refresh operation must be performed at least once every 32 ms to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding both $\overline{xCAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

$\overline{RAS}$-only refresh '418160

A refresh operation must be performed at least once every 8 ms to retain data. This can be achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding both $\overline{xCAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored and the refresh address is generated internally.

$\overline{xCAS}$-before-$\overline{RAS}$ (xCBR) refresh

xCBR refresh is utilized by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive xCBR refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or xCBR) cycle.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: ..... – 1 V to 7 V
Voltage range on any pin (see Note 1): ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... – 55°C to 125°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	– 55		125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

SMJ416160

PARAMETER		TEST CONDITIONS†	'416160-60		'416160-70		'416160-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high		± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		90		80		70	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high		2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high		1		1		1	mA
I_{CC3}§	Average refresh current ($\overline{RAS}$ only refresh or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)		90		80		70	mA
I_{CC4}‡¶	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling		90		80		70	mA
I_{CC7}‡¶	Standby current, outputs enabled	$\overline{RAS}$ = V_{IH}, $\overline{xCAS}$ = V_{IL}, Data out = enabled		5		5		5	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

SMJ418160

PARAMETER		TEST CONDITIONS†	'418160-60		'418160-70		'418160-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high		± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		190		180		170	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high		2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high		1		1		1	mA
I_{CC3}§	Average refresh current ($\overline{RAS}$ only refresh or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)		190		180		170	mA
I_{CC4}‡¶	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling		190		180		170	mA
I_{CC7}‡¶	Standby current, outputs enabled	$\overline{RAS}$ = V_{IH}, $\overline{xCAS}$ = V_{IL}, Data out = enabled		5		5		5	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A11		10	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		10	pF
$C_{i(RC)}$	Input capacitance, $\overline{xCAS}$ and $\overline{RAS}$		10	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		10	pF
C_o	Output capacitance		10	pF

NOTE 3: Capacitance is sampled only at initial design and after any major changes. Samples are tested at 0 V and 25°C with a 1-MHz signal applied to the pin under test. All other pins are open.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

PARAMETER		'41x160-60		'41x160-70		'41x160-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{xCAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20	ns
t_{OFF}	Output disable time after $\overline{xCAS}$ high (see Note 5)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 5)	0	15	0	18	0	20	ns

NOTES: 4. Valid data is presented at the outputs after all access times are satisfied but can go from the high-impedance state to an invalid-data state prior to the specified access time as the outputs are driven when $\overline{xCAS}$ and $\overline{OE}$ are low.

5. t_{OFF} and t_{OEZ} are specified when the output is no longer driven. The outputs are disabled by bringing either $\overline{OE}$ or $\overline{xCAS}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'41x160-60		'41x160-70		'41x160-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read (see Note 6)	110		130		150		ns
t_{WC}	Cycle time, write (see Note 6)	110		130		150		ns
t_{RWC}	Cycle time, read-write (see Note 6)	155		181		205		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 6 and 7)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-write (see Note 6)	85		96		105		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 8)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 8)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{xCAS}$ low (see Note 9)	15	10 000	18	10 000	20	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{xCAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 10)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{xCAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ low (early-write operation only)	0		0		0		ns
t_{CAH}	Hold time, column address after $\overline{xCAS}$ low	10		15		15		ns
t_{DH}	Hold time, data (see Note 10)	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{xCAS}$ high (see Note 11)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 11)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{xCAS}$ low (early-write operation only)	10		15		15		ns

NOTES: 6. All cycle times assume t_T = 5 ns, referenced to $V_{IH(min)}$ and $V_{IL(max)}$.

7. To assure t_{PC} min, t_{ASC} should be ≥ to t_{CP}.
8. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
9. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
10. Referenced to the later of $\overline{xCAS}$ or $\overline{W}$ in write operations
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

PRODUCT PREVIEW

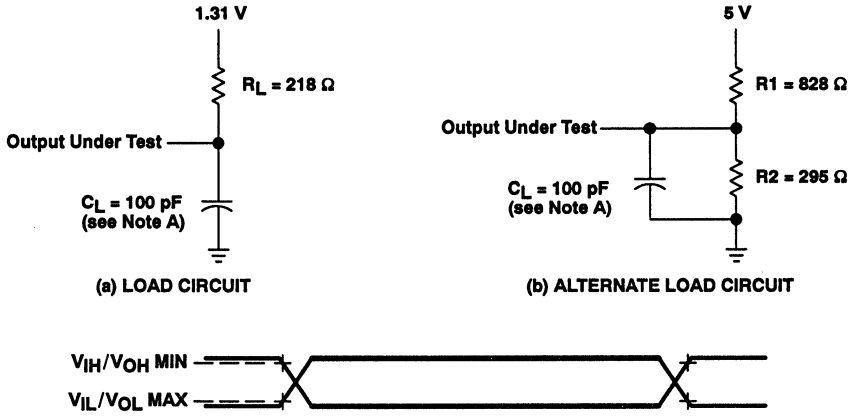
timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			'41x160-60		'41x160-70		'41x160-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CLCH}	Hold time, $\overline{xCAS}$ low to $\overline{xCAS}$ high		5		5		5		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{xCAS}$ precharge		35		40		45		ns
t_{OEH}	Hold time, $\overline{OE}$ command		15		18		20		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$		10		10		10		ns
t_{CP}	Delay time, $\overline{xCAS}$ high (precharge)		10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)		55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high (CBR refresh only)		10		10		10		ns
t_{CRP}	Delay time, $\overline{xCAS}$ high to $\overline{RAS}$ low		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high		60		70		80		ns
t_{CSR}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ low (CBR refresh only)		5		5		5		ns
t_{CWD}	Delay time, $\overline{xCAS}$ low to $\overline{W}$ low (read-write operation only)		40		46		50		ns
t_{OED}	Delay time, $\overline{OE}$ to data		15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 12)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{xCAS}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ low (see Note 12)		20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{xCAS}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ high		15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)		85		98		110		ns
t_{CPW}	Delay time, $\overline{W}$ low after $\overline{xCAS}$ precharge (read-write operation only)		60		68		75		ns
t_{REF}	Refresh time interval	'416160		32		32		32	ms
		'418160		8		8		8	
t_T	Transition time (see Note 13)								

NOTES: 12. The maximum value is specified only to assure access time.
13. Transition times (rise and fall) should be a minimum of 3 ns and a maximum of 30 ns.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

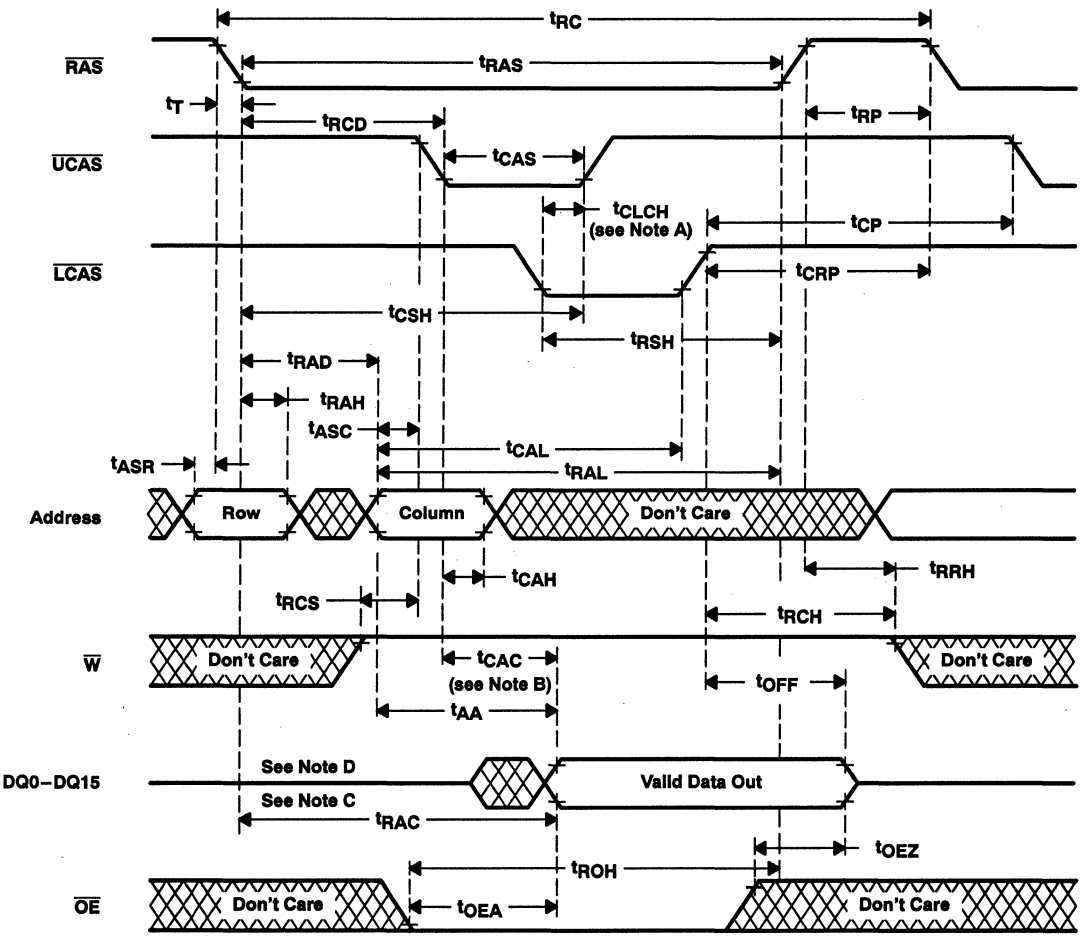


NOTES: A. C_L includes probe and fixture capacitance.
B. The ac timing parameters are specified with reference to the minimum valid high-level voltage and the maximum valid low-level voltage for each signal. This corresponds to 2.4 V and 0.8 V for inputs; 2.4 V and 0.4 V for outputs with the given load circuit.

Figure 1. Load Circuits and Voltage Waveforms

PRODUCT PREVIEW

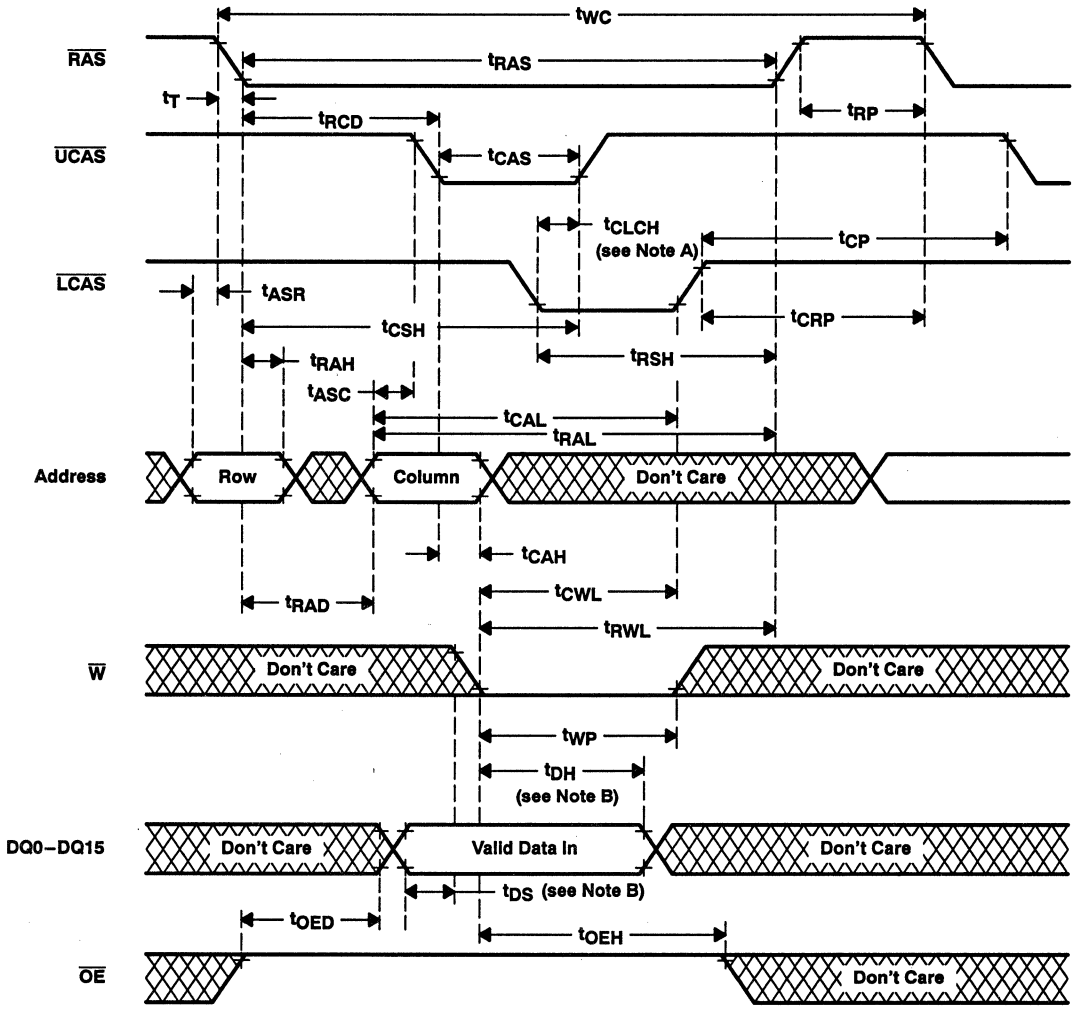
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. $\overline{xCAS}$ order is arbitrary.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

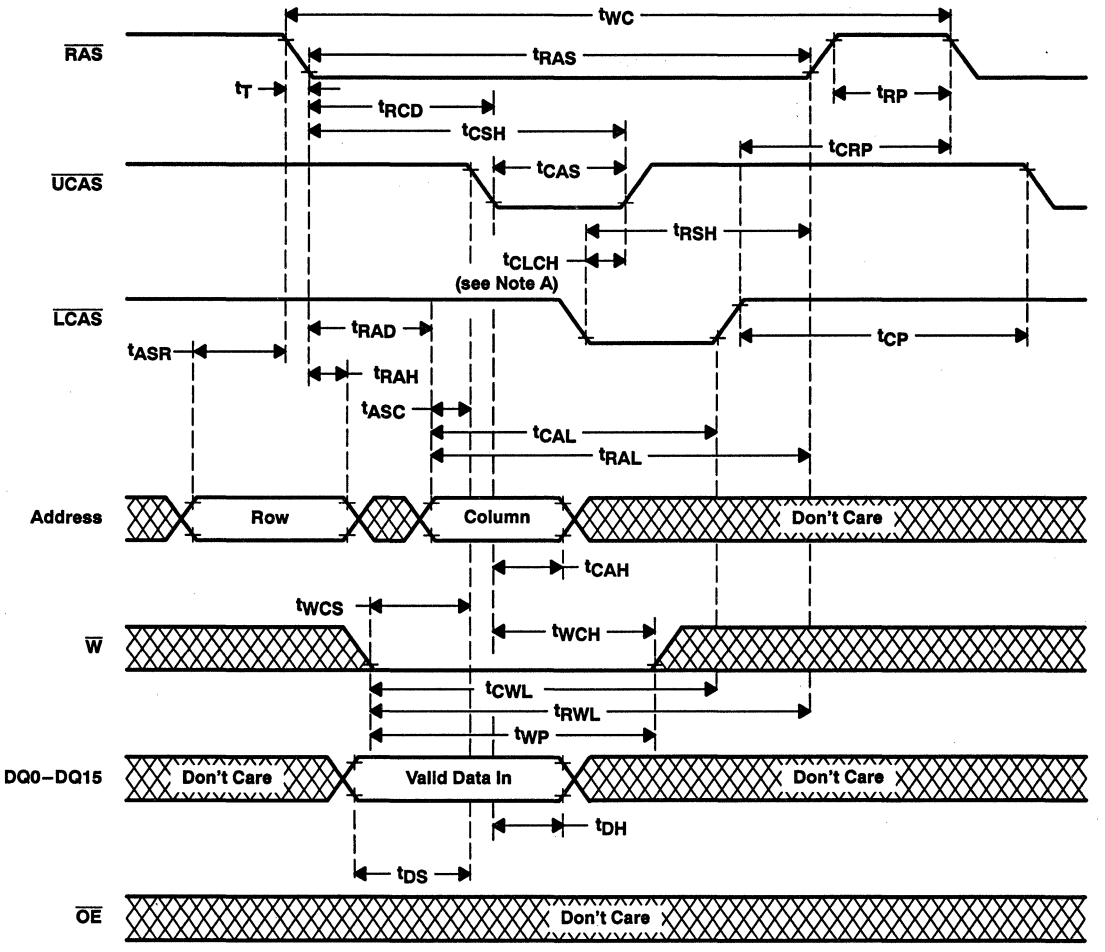


NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to the first $\overline{\text{xCAS}}$ or $\overline{\text{W}}$, whichever occurs last
C. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 3. Write-Cycle Timing

PRODUCT PREVIEW

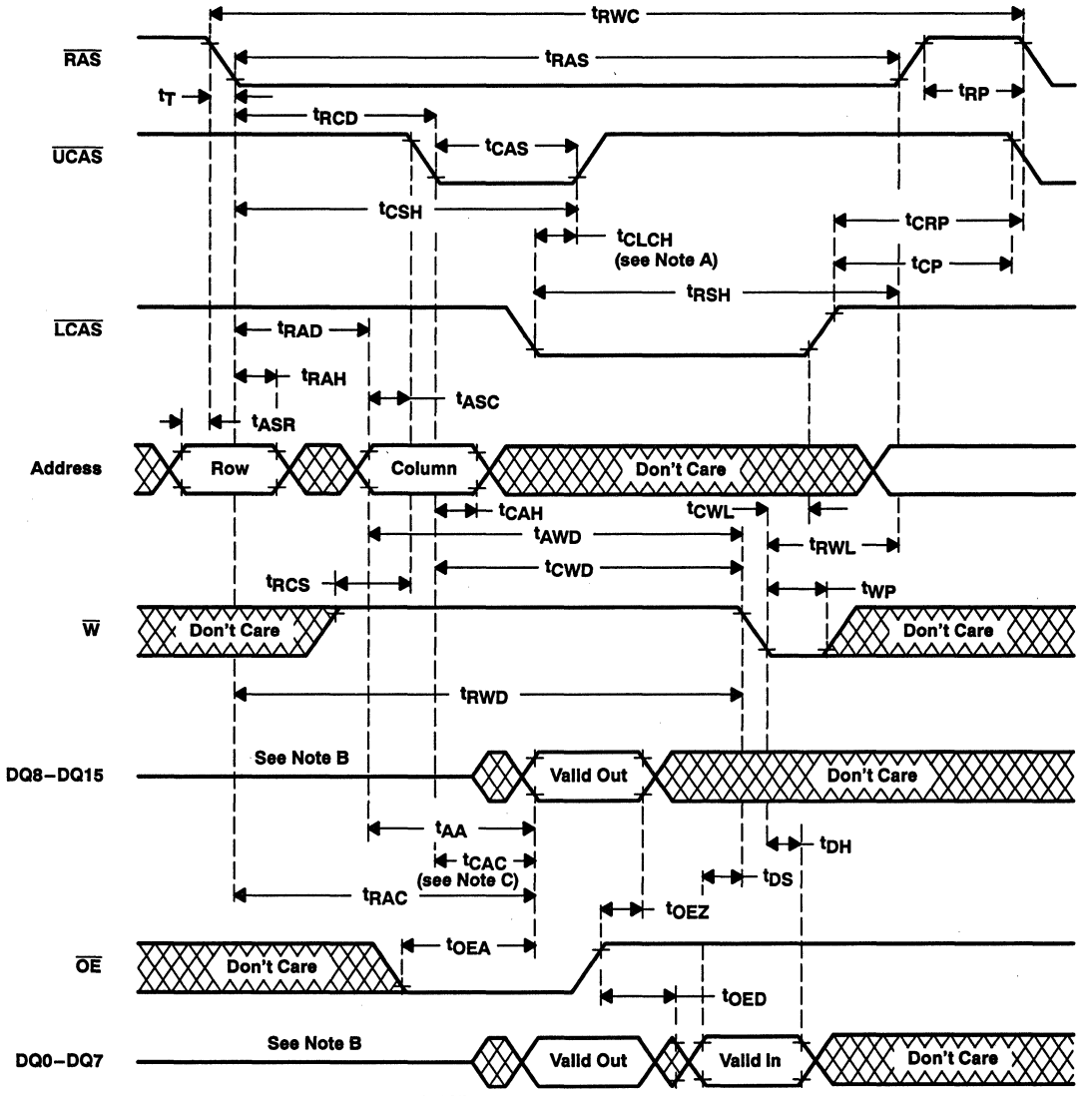
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.

Figure 4. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

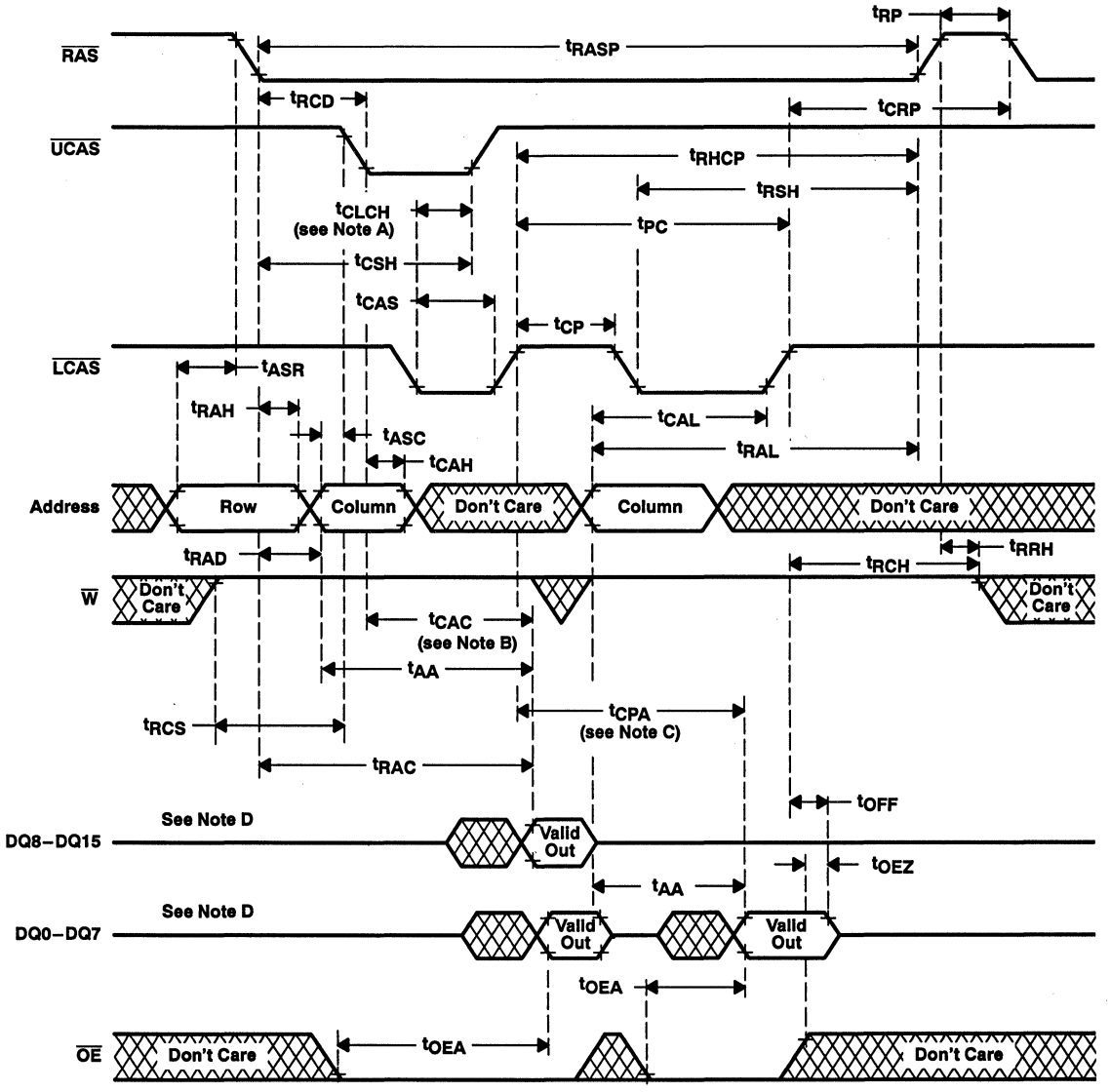


NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
C. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
D. $\overline{xCAS}$ order is arbitrary.

Figure 5. Read-Modify-Write-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

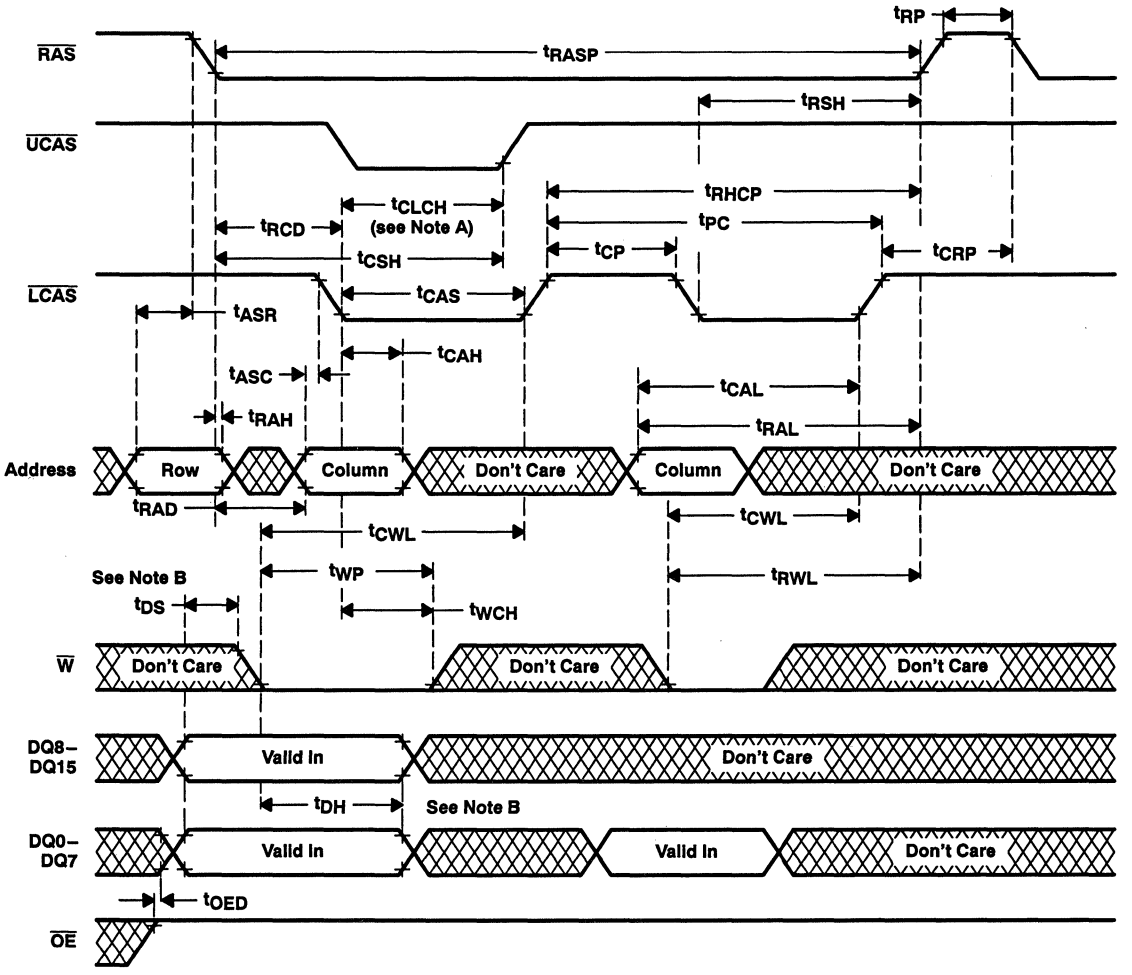


NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. Access time is t_{CPA} or t_{AA} dependent.
D. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write- and read-modify-write-timing specifications are not violated.
F. $\overline{xCAS}$ order is arbitrary.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

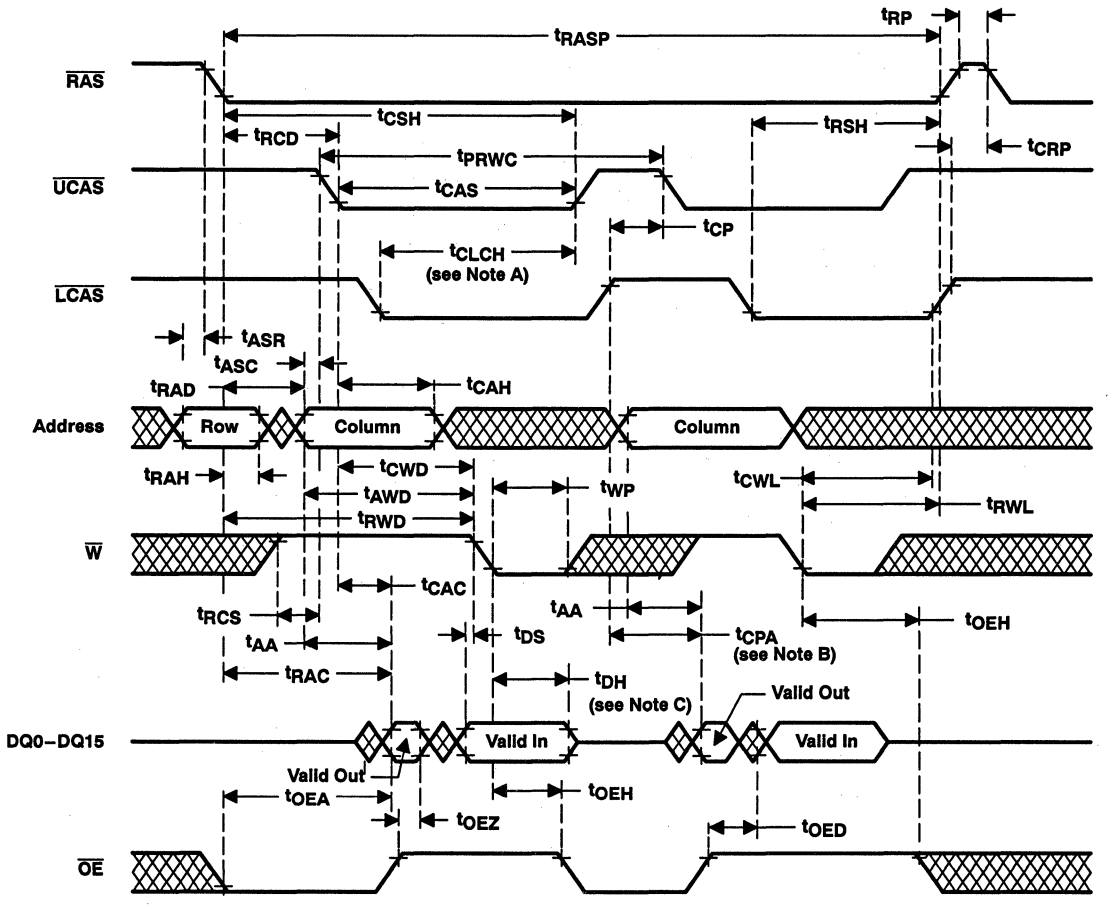


NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last
C. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read- and read-modify-write-timing specifications are not violated.
D. $\overline{xCAS}$ order is arbitrary.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

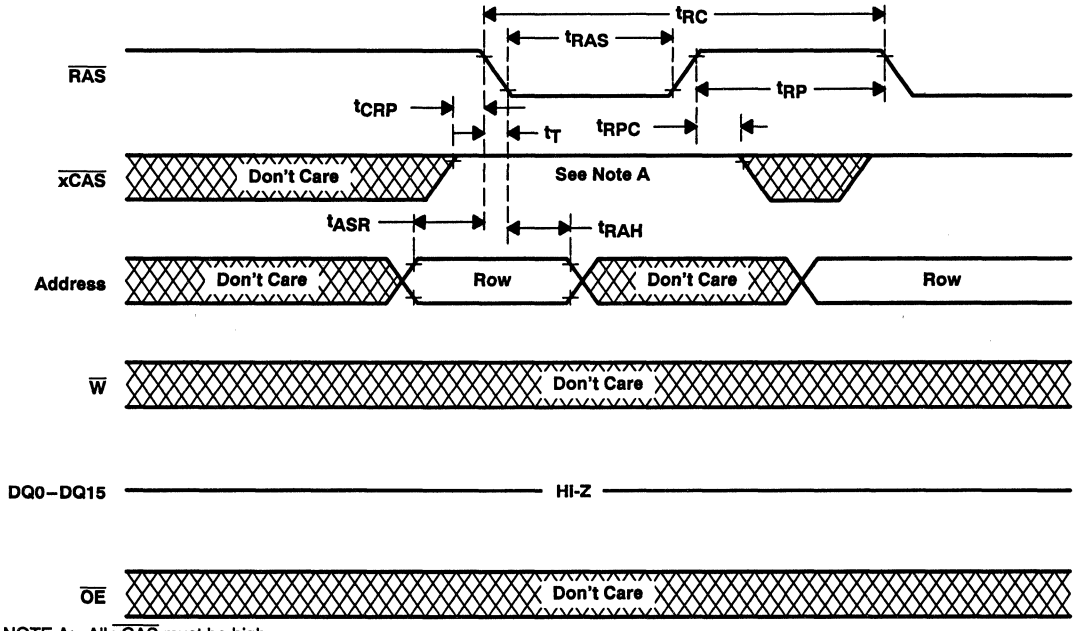


NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Access time is t_{CPA} or t_{AA} dependent.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. $\overline{xCAS}$ order is arbitrary.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read- and write-cycle timing specifications are not violated.
F. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.

Figure 8. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTE A: All xCAS must be high.

Figure 9. RAS-Only Refresh-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

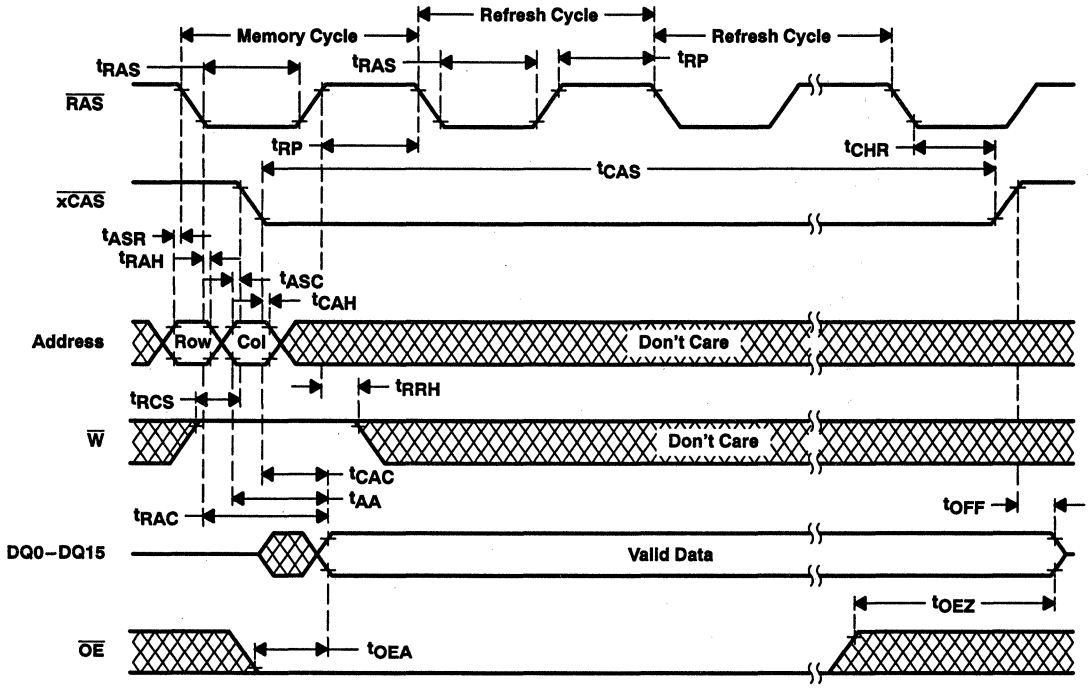
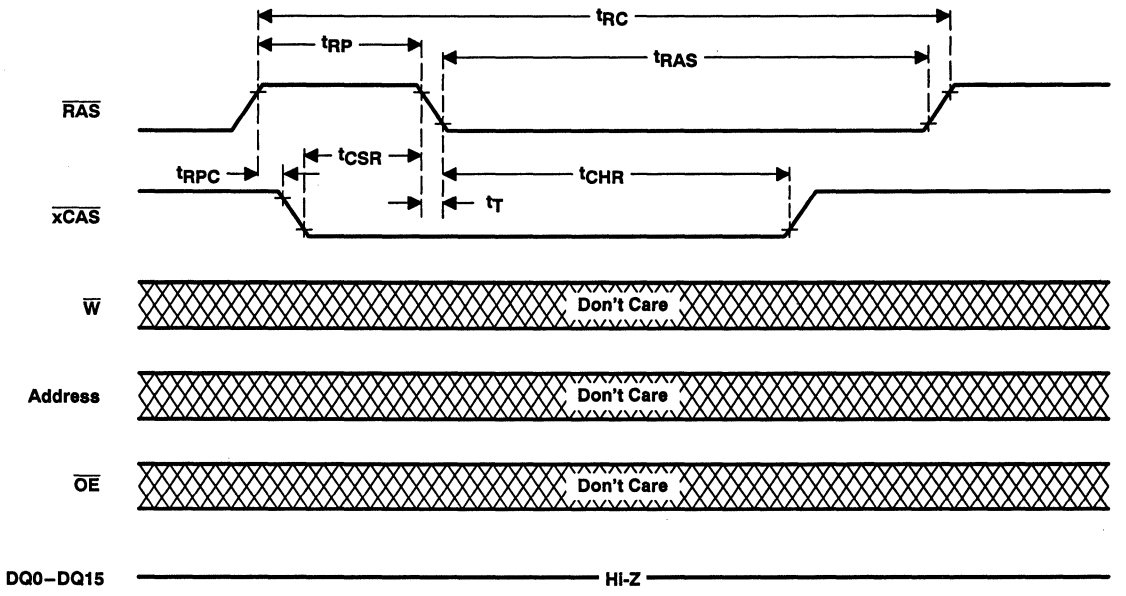


Figure 10. Hidden-Refresh-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTE A: Any $\overline{xCAS}$ can be used.

Figure 11. Automatic-xCBR-Refresh-Cycle Timing

SGMS058A – MARCH 1995 – REVISED JUNE 1995

- **Military Operating Temperature Range –55°C to 125°C**
- **Performance Ranges:**

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ENABLE (MAX)	ACCESS TIME SERIAL DATA (MAX)	ACCESS TIME SERIAL ENABLE (MAX)
	$t_{a(R)}$	$t_{a(C)}$	$t_{a(SQ)}$	$t_{a(SE)}$
'44C251B-10	100 ns	25 ns	30 ns	20 ns
'44C251B-12	120 ns	30 ns	35 ns	25 ns

- **Class B High-Reliability Processing**
- **DRAM: 262144 Words × 4 Bits SAM: 512 Words × 4 Bits**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Dual Port Accessibility–Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Bidirectional-Data-Transfer Function Between the DRAM and the Serial-Data Register**
- **4 × 4 Block-Write Feature for Fast Area Fill Operations; As Many as Four Memory Address Locations Written per Cycle From an On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O; Two Write-Per-Bit Modes to Simplify System Design**
- **Enhanced Page-Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) and Hidden Refresh Modes**
- **All Inputs/Outputs and Clocks Are TTL Compatible**
- **Long Refresh Period Every 8 ms (Max)**
- **Up to 33-MHz Uninterrupted Serial-Data Streams**
- **3-State Serial I/Os Allow Easy Multiplexing of Video-Data Streams**
- **512 Selectable Serial-Register Starting Locations**
- **Texas Instruments EPIC™ Process**
- **Packaging:**
  - **28-Pin J-Leaded Ceramic Chip Carrier Package (HJ Suffix)**
  - **28-Pin Leadless Ceramic Chip Carrier Package (HM Suffix)**
  - **28-Pin Ceramic Sidebrazed DIP (JD Suffix)**
  - **28-Pin Zig-Zag In-Line (ZIP), Ceramic Package (SV Suffix)**
- **Split Serial-Data Register for Simplified Real-Time Register Reload**

PIN NOMENCLATURE	
A0–A8	Address Inputs
$\overline{CAS}$	Column Enable
DQ0–DQ3	DRAM Data In-Out/Write-Mask Bit
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row Enable
SC	Serial Data Clock
SDQ0–SDQ3	Serial Data In-Out
$\overline{TRG}$	Transfer Register/Q Output Enable
$\overline{W}$	Write-Mask Select/Write Enable
DSF	Special Function Select
QSF	Split-Register Activity Status
V_{CC}	5-V Supply
V_{SS}	Ground
GND	Ground (Important: Not connected to internal V_{SS})

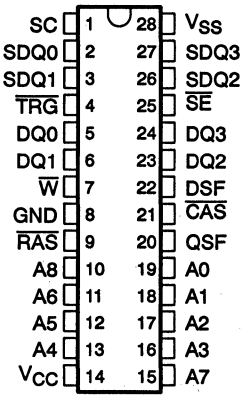
description

The SMJ44C251B multiport video RAM is a high-speed, dual-ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262144 words of 4 bits each interfaced to a serial-data register or serial-access memory (SAM) organized as 512 words of 4 bits each. The SMJ44C251B supports three types of operation: random access to and from the DRAM, serial access to and from the serial register, and bidirectional transfer of data between any row in the DRAM and the serial register. Except during transfer operations, the SMJ44C251B can be accessed simultaneously and asynchronously from the DRAM and SAM ports. During a transfer operation, the 512 columns of the DRAM are connected to the 512 positions in the serial data register. The 512 × 4-bit serial-data register can be loaded from the memory row (transfer read), or the contents of the 512 × 4-bit serial-data register can be written to the memory row (transfer write).

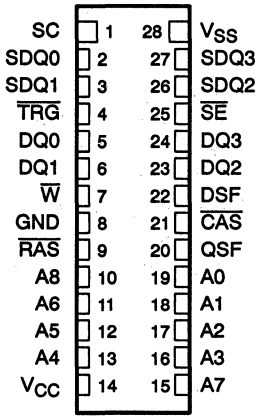
EPIC is a trademark of Texas Instruments Incorporated.

pinouts

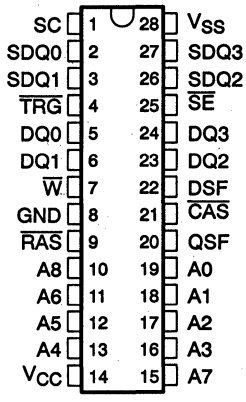
HJ PACKAGE
(TOP VIEW)



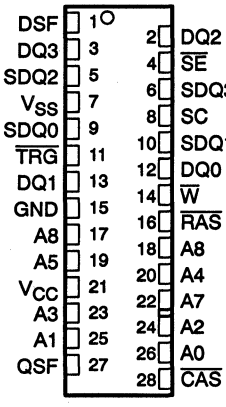
HM PACKAGE
(TOP VIEW)



JD PACKAGE
(TOP VIEW)



SV PACKAGE
(TOP VIEW)



description (continued)

The SMJ44C251B is equipped with several features designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's 4 × 4 block-write mode. The block-write mode allows four bits of data (present in an on-chip color-data register) to be written to any combination of four adjacent column-address locations. As many as 16 bits of data can be written to memory during each $\overline{CAS}$ cycle time. Also on the DRAM port, a write mask or a write-per-bit feature allows masking any combination of the four input/outputs on any write cycle. The persistent write-per-bit feature uses a mask register that, once loaded, can be used on subsequent write cycles. The mask register eliminates having to provide mask data on every mask-write cycle.

The SMJ44C251B offers a split-register transfer read (DRAM to SAM) feature for the serial tester (SAM port). This feature enables real-time register reload implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. For applications not requiring real-time register reload (for example, reloads done during CRT retrace periods), the single-register mode of operation is retained to simplify design. The SAM can also be configured in input mode, accepting serial data from an external device. Once the serial register within the SAM is loaded, its contents can be transferred to the corresponding column positions in any row in memory in a single memory cycle.

The SAM port is designed for maximum performance. Data can be input to or accessed from the SAM at serial rates up to 33 MHz. During the split-register mode of operation, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, QSF, is included to indicate which half of the serial register is active at any given time in the split-register mode.

All inputs, outputs, and clock signals on the SMJ44C251B are compatible with Series 54 TTL devices. All address lines and data-in lines are latched on-chip to simplify system design. All data-out lines are unlatched to allow greater system flexibility.

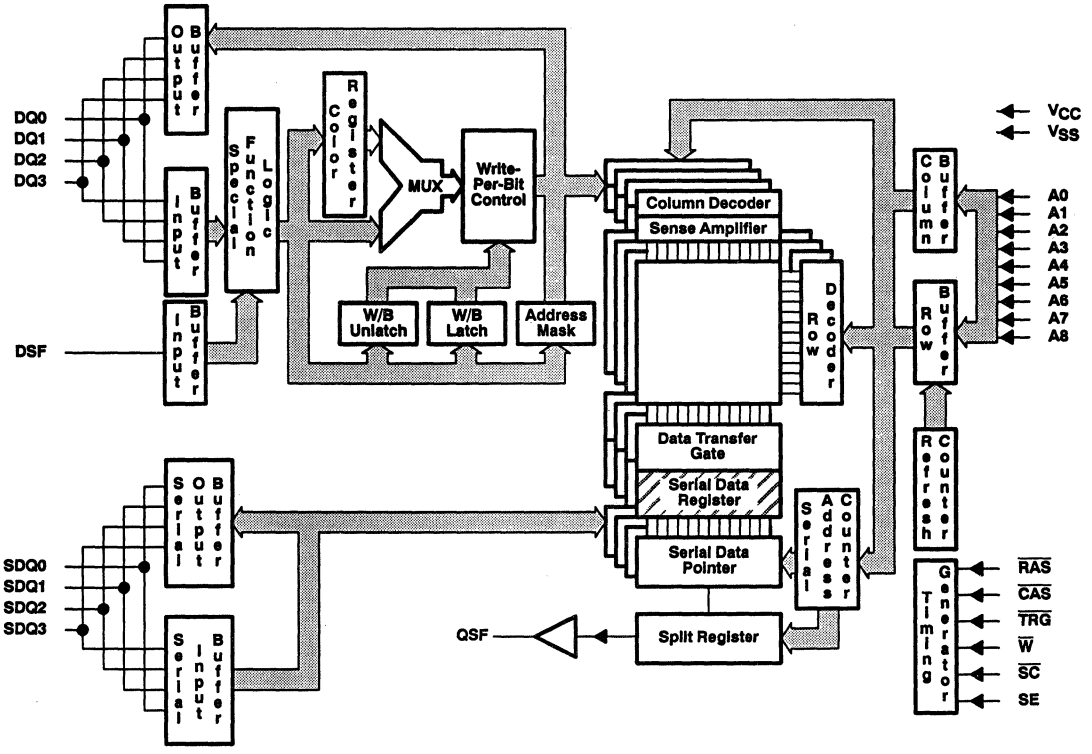
description (continued)

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup, row-address hold, and address multiplex is eliminated, and a memory cycle time reduction of up to 3× can be achieved, compared to minimum $\overline{RAS}$ cycle times. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and page-mode cycle time used. The SMJ44C251B allows a full page (512 cycles) of information to be accessed in read, write, or read-modify-write mode during a single $\overline{RAS}$-low period using relatively conservative page-mode cycle times.

The SMJ44C251B employs state-of-the-art Texas Instruments EPIC™ scaled CMOS, double-level polysilicon/polycide gate technology for very high performance combined with improved reliability. For surface mount technology, the SMJ44C251B is offered in a 28-pin J-leaded chip carrier package (HJ suffix) or a 28-pin leadless ceramic chip carrier package (HM suffix). The SMJ44C251B is offered in a 28-pin 400-mil dual-in-line ceramic sidebrazed package (JD suffix) or a 28-pin ZIP ceramic package (SV suffix) for through-hole insertion. The L suffix device is rated for operation from 0°C to 70°C. The M suffix device is rated for operation from –55°C to 125°C.

The SMJ44C251B and other multiport video RAMs are supported by a broad line of video/graphic processors from Texas Instruments, including the SMJ34010 and the SMJ34020 graphics processors.

functional block diagram



Function Table

FUNCTION	RAS FALL					CAS FALL	ADDRESS		DQ0–DQ3		TYPE†
	CAS	TRG	W‡	DSF	SE	DSF	RAS	CAS	RAS	CAS§ W	
CBR refresh	L	X	X	X	X	X	X	X	X	X	R
Register-to-memory transfer (transfer write)	H	L	L	X	L	X	Row Addr	Tap Point	X	X	T
Alternate transfer write (independent of SE)	H	L	L	H	X	X	Row Addr	Tap Point	X	X	T
Serial-write-mode enable (pseudo-transfer write)	H	L	L	L	H	X	Refresh Addr	Tap Point	X	X	T
Memory-to-register transfer (transfer read)	H	L	H	L	X	X	Row Addr	Tap Point	X	X	T
Split-register-transfer read (must reload tap)	H	L	H	H	X	X	Row Addr	Tap Point	X	X	T
Load and use write mask, Write data to DRAM	H	H	L	L	X	L	Row Addr	Col Addr	DQ Mask	Valid Data	R
Load and use write mask, Block write to DRAM	H	H	L	L	X	H	Row Addr	Blk Addr A2–A8	DQ Mask	Col Mask	R
Persistent write-per-bit, Write data to DRAM	H	H	L	H	X	L	Row Addr	Col Addr	X	Valid Data	R
Persistent write-per-bit, Block write to DRAM	H	H	L	H	X	H	Row Addr	Blk Addr A2–A8	X	Col Mask	R
Normal DRAM read/write (nonmasked)	H	H	H	L	X	L	Row Addr	Col Addr	X	Valid Data	R
Block write to DRAM (nonmasked)	H	H	H	L	X	H	Row Addr	Blk Addr A2–A8	X	Col Mask	R
Load write mask	H	H	H	H	X	L	Refresh Addr	X	X	DQ Mask	R
Load color register	H	H	H	H	X	H	Refresh Addr	X	X	Color Data	R

Legend:
H = High
L = Low
X = Don't care
† R = random access operation; T = transfer operation
‡ In persistent write-per-bit function, W must be high during the refresh cycle.
§ DQ0–DQ3 are latched on the later of W or CAS falling edge.
Col Mask = H: Write to address/column location enabled
DQ Mask = H: Write to I/O enabled

operation

Depending on the type of operation chosen, the signals of the SMJ44C251B perform different functions. Table 1 summarizes the signal descriptions and the operational modes they control.

Table 1. Detailed Signal Description Versus Operational Mode

PIN	DRAM	TRANSFER	SAM
A0–A8	Row, column address	Row, tap address	
$\overline{CAS}$	Column enable, output enable	Tap-address strobe	
DQi	DRAM data I/O, write mask bits		
DSF	Block-write enable Persistent write-per-bit enable Color-register load enable	Split-register enable Alternate write-transfer enable	
$\overline{RAS}$	Row enable	Row enable	
$\overline{SE}$		Serial-in mode enable	Serial enable
SC			Serial clock
SDQ			Serial-data I/O
$\overline{TRG}$	Q output enable	Transfer enable	
$\overline{W}$	Write enable, write-per-bit select	Transfer-write enable	
QSF			Split register Active status
NC/GND	Make no external connection or tie to system V_{SS}.		
V_{CC}	5-V supply (typical)		
V_{SS}	Device ground		

The SMJ44C251B has three kinds of operations: random-access operations typical of a DRAM, transfer operations from memory arrays to the SAM, and serial-access operations through the SAM port. The signals used to control these operations are described here, followed by discussions of the operations themselves.

address (A0–A8)

For DRAM operation, 18 address bits are required to decode one of the 262144 storage cell locations. Nine row-address bits are set up on A0–A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Nine column-address bits are set up on A0–A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

During the transfer operation, the states of A0–A8 are latched on the falling edge of $\overline{RAS}$ to select one of the 512 rows where the transfer occurs. To select one of 512 tap points (starting positions) for the serial-data input or output, the appropriate 9-bit column address (A0–A8) must be valid when $\overline{CAS}$ falls.

row-address strobe ($\overline{RAS}$)

$\overline{RAS}$ is similar to a chip enable because all DRAM cycles and transfer cycles are initiated by the falling edge of $\overline{RAS}$. $\overline{RAS}$ is a control input that latches the states of row address, $\overline{W}$, $\overline{TRG}$, $\overline{SE}$, $\overline{CAS}$, and DSF onto the chip to invoke DRAM and transfer functions.

column-address strobe ($\overline{CAS}$)

$\overline{CAS}$ is a control input that latches the states of column address and DSF to control DRAM and transfer functions. When $\overline{CAS}$ is brought low during a transfer cycle, it latches the new tap point for the serial-data input or output. $\overline{CAS}$ also acts as an output enable for the DRAM outputs DQ0–DQ3.

output enable/transfer select ($\overline{TRG}$)

$\overline{TRG}$ selects either DRAM or transfer operation as $\overline{RAS}$ falls. For DRAM operation, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. During DRAM operation, $\overline{TRG}$ functions as an output enable for the DRAM outputs DQ0–DQ3. For transfer operation, $\overline{TRG}$ must be brought low before $\overline{RAS}$ falls.

write-mask select, write enable ($\overline{W}$)

In DRAM operation, $\overline{W}$ enables data to be written to the DRAM. $\overline{W}$ is also used to select the DRAM write-per-bit mode. Holding $\overline{W}$ low on the falling edge of $\overline{RAS}$ invokes the write-per-bit operation. The SMJ44C251B supports both the normal write-per-bit mode and the persistent write-per-bit mode.

For transfer operation, $\overline{W}$ selects either a read-transfer operation (DRAM to SAM) or a write-transfer operation (SAM to DRAM). During a transfer cycle, if $\overline{W}$ is high when $\overline{RAS}$ falls, a read transfer occurs; if $\overline{W}$ is low, a write transfer occurs.

special function select (DSF)

DSF is latched on the falling edge of $\overline{RAS}$ or $\overline{CAS}$, similar to an address. DSF determines which of the following functions are invoked on a particular cycle:

- Persistent write-per-bit
- Block write
- Split-register transfer read
- Mask-register load for the persistent write-per-bit mode
- Color-register load for the block-write mode

DRAM data I/O, write-mask data (DQ0–DQ3)

DRAM data is written via DQ terminals during a write or read-modify-write cycle. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{W}$ is brought low after $\overline{CAS}$ and the data is strobed in by $\overline{W}$ with data setup and hold times referenced to this signal.

The 3-state DQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state as long as $\overline{CAS}$ and $\overline{TRG}$ are held high. Data does not appear at the outputs until both $\overline{CAS}$ and $\overline{TRG}$ are brought low. Once the outputs are valid, they remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ or $\overline{TRG}$ going high returns the outputs to the high-impedance state. In a register-transfer operation, the DQ outputs remain in the high-impedance state for the entire cycle.

The write-per-bit mask is latched into the device via the random DQ terminals by the falling edge of $\overline{RAS}$. This mask selects which of the four random I/Os are written.

serial data I/O (SDQ0–SDQ3)

Serial inputs and serial outputs share common I/O terminals. Serial-input or serial-output mode is determined by the previous transfer cycle. If the previous transfer cycle was a read transfer, the data register is in serial-output mode. While in serial-output mode, data in SAM is accessed from the least significant bit to the most significant bit. The data registers operate modulo 512; so after bit 511 is accessed, the next bits to be accessed are 00, 01, 02, etc. If the previous transfer cycle was either a write transfer or a pseudo transfer, the data register is in serial-input mode and signal data can be input to the register.

serial clock (SC)

Serial data is accessed in or out of the data register on the rising edge of SC. The SMJ44C251B is designed to work with a wide range of clock-duty cycles to simplify system design. There is no refresh requirement because the data registers that comprise the SAM are static. There is also no minimum SC clock operating frequency.

serial enable ($\overline{SE}$)

During serial-access operations $\overline{SE}$ is used as an enable/disable for SDQ in both the input and output modes. If $\overline{SE}$ is held as $\overline{RAS}$ falls during a write-transfer cycle, a pseudo-transfer write occurs. There is no actual transfer, but the data register switches from the output mode to the input mode.

no connect/ground (NC/GND)

NC/GND is reserved for the manufacturer's test operation. It is an input and should be tied to system ground or left floating for proper device operation.

special function output (QSF)

During split-register operation the QSF output indicates which half of the SAM is being accessed. When QSF is low, the serial-address pointer is accessing the lower (least significant) 256 bits of SAM. When QSF is high, the serial-address pointer is accessing the higher (most significant) 256 bits of SAM. QSF changes state upon crossing the boundary between the two SAM halves in the split-register mode.

During normal transfer operations QSF changes state upon completing a transfer cycle. This state is determined by the tap point being loaded during the transfer cycle.

power up

To achieve proper device operation, an initial pause of 200 μs is required after power-up, followed by a minimum of eight $\overline{RAS}$ cycles or eight CBR cycles, a memory-to-register transfer cycle, and two SC cycles.

random-access operation

The random-access operation functions are summarized in Table 2 and described in the following sections.

Table 2. Random-Access-Operation Functions

FUNCTION	RAS FALL					CAS FALL	ADDRESS		DQ0–DQ3	
	CAS	TRG	W†	DSF	SE	DSF	RAS	CAS	RAS	CAS‡ W
CBR refresh	L	X	X	X	X	X	X	X	X	X
Load and use write mask, Write data to DRAM	H	H	L	L	X	L	Row Addr	Col Addr	DQ Mask	Valid Data
Load and use write mask, Block write to DRAM	H	H	L	L	X	H	Row Addr	Blk Addr A2–A8	DQ Mask	Col Mask
Persistent write-per-bit, Write data to DRAM	H	H	L	H	X	L	Row Addr	Col Addr	X	Valid Data
Persistent write-per-bit, Block write to DRAM	H	H	L	H	X	H	Row Addr	Blk Addr A2–A8	X	Col Mask
Normal DRAM read/write (nonmasked)	H	H	H	L	X	L	Row Addr	Col Addr	X	Valid Data
Block write to DRAM (nonmasked)	H	H	H	L	X	H	Row Addr	Blk Addr A2–A8	X	Col Mask
Load write mask	H	H	H	H	X	L	Refresh Addr	X	X	DQ Mask
Load color register	H	H	H	H	X	H	Refresh Addr	X	X	Color Data

Legend:
H = High
L = Low
X = Don't care
† In persistent write-per-bit function, W must be high during the refresh cycle.
‡ DQ0–DQ3 are latched on the later of W or CAS falling edge.
Col Mask = H: Write to address/column location enabled
DQ Mask = H: Write to I/O enabled

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. This mode eliminates the time required for row address setup-and-hold and address multiplex. The maximum RAS low time and the CAS page cycle time used determine the number of columns that can be accessed.

Unlike conventional page-mode operation, the enhanced page mode allows the SMJ44C251B to operate at a higher data bandwidth. Data retrieval begins as soon as the column address is valid rather than when CAS transitions low. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of CAS. In this case, data can be obtained after $t_{a(C)}$ max (access time from CAS low), if $t_{a(CA)}$ max (access time from column address) has been satisfied.

refresh

There are three types of refresh available on the SMJ44C251B: RAS-only refresh, CBR refresh, and hidden refresh.

$\overline{\text{RAS}}$-only refresh

A refresh operation must be performed to each row at least once every 8 ms to retain data. Unless $\overline{\text{CAS}}$ is applied, the output buffers are in the high-impedance state, so the $\overline{\text{RAS}}$-only refresh sequence avoids any output during refresh. Externally generated addresses must be supplied during $\overline{\text{RAS}}$-only refresh. Strobing each of the 512 row addresses with $\overline{\text{RAS}}$ causes all bits in each row to be refreshed. $\overline{\text{CAS}}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ (CBR) refresh

CBR refresh is accomplished by bringing $\overline{\text{CAS}}$ low earlier than $\overline{\text{RAS}}$. The external row address is ignored and the refresh row address is generated internally when using CBR refresh. Other cycles can be performed in between CBR cycles without disturbing the internal address generation.

hidden refresh

A hidden refresh is accomplished by holding $\overline{\text{CAS}}$ low in the DRAM-read cycle and cycling $\overline{\text{RAS}}$. The output data of the DRAM-read cycle remains valid while the refresh is being carried out. Like the CBR refresh, the refreshed row addresses are generated internally during the hidden refresh.

write-per-bit

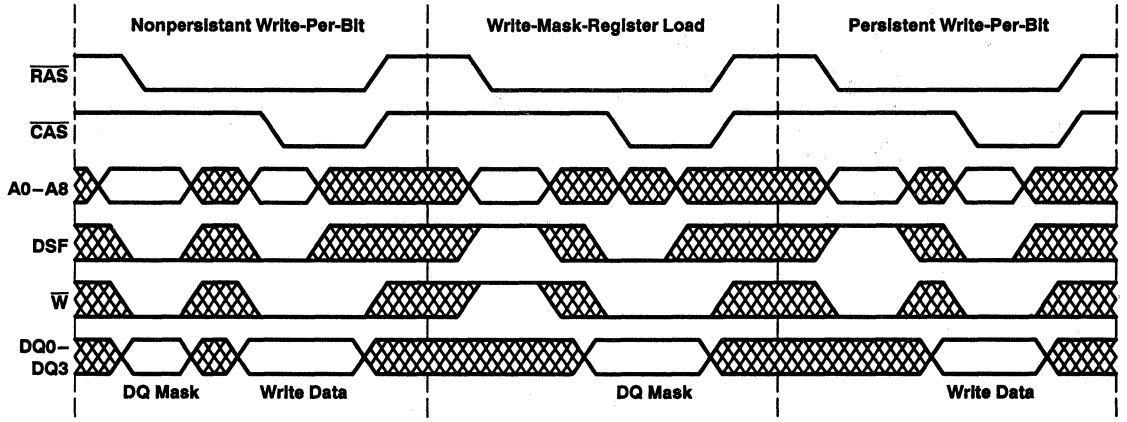
The write-per-bit feature allows masking of any combination of the four DQs on any write cycle (see Figure 1). The write-per-bit operation is invoked only when $\overline{\text{W}}$ is held low on the falling edge of $\overline{\text{RAS}}$. If $\overline{\text{W}}$ is held high on the falling edge of $\overline{\text{RAS}}$, write-per-bit is not enabled and the write operation is performed to all four DQs. The SMJ44C251B offers two write-per-bit modes: the nonpersistent write-per-bit mode and the persistent write-per-bit mode.

nonpersistent write-per-bit

When DSF is low on the falling edge of $\overline{\text{RAS}}$, the write mask is reloaded. A 4-bit code (the write-per-bit mask) is input to the device via the random DQ terminals and latched on the falling edge of $\overline{\text{RAS}}$. The write-per-bit mask selects which of the four random I/Os are written and which are not. After $\overline{\text{RAS}}$ has latched the on-chip write-per-bit mask, input data is driven onto the DQ terminals and is latched on the later falling edge of $\overline{\text{CAS}}$ or $\overline{\text{W}}$. When a data low is strobed into a particular I/O on the falling edge of $\overline{\text{RAS}}$, data is not written to that I/O. When a data high is strobed into a particular I/O on the falling edge of $\overline{\text{RAS}}$, data is written to that I/O.

persistent write-per-bit

When DSF is high on the falling edge of $\overline{\text{RAS}}$, the write-per-bit mask is not reloaded: it retains the value stored during the last write-per-bit mask reload. This mode of operation is known as persistent write-per-bit because the write-per-bit mask is persistent over an arbitrary number of write cycles. The write-per-bit mask reload can be done during the nonpersistent write-per-bit cycle or by the mask-register-load cycle.



DQ Mask = H: Write to I/O enabled
= L: Write to I/O disabled

Figure 1. Example of Write-Per-Bit Operations

block write

The block-write mode allows data (present in an on-chip color register) to be written into four consecutive column-address locations. The 4-bit color register is loaded by the color-register-load cycle. Both write-per-bit modes can be applied in the block-write cycle. The block-write mode also offers the 4 × 4 column-mask capability.

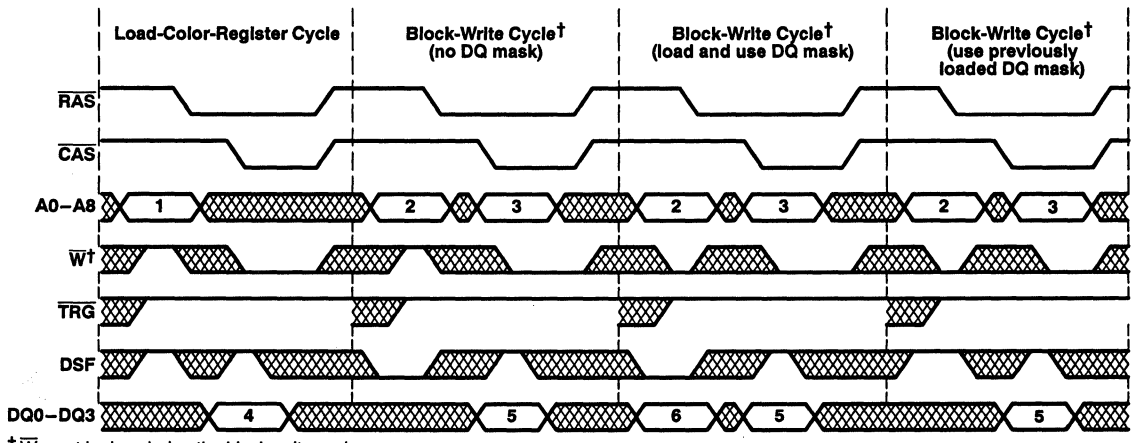
load color register

The load-color-register cycle is performed using normal DRAM write-cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. A 4-bit code is input to the color register via the random I/O terminals and latched on the later of the falling edge of $\overline{CAS}$ or $\overline{W}$. After the color register is loaded, it retains data until power is lost or until another load-color-register cycle is executed.

block write cycle

After the color register is loaded, the block-write cycle can begin as a normal DRAM write cycle with DSF held high on the falling edge of $\overline{CAS}$ (see Figures 2, 3, and 4). When the block-write cycle is invoked, each data bit in the 4-bit color register is written to selected bits of the four adjacent columns of the corresponding random I/O.

During block-write cycles, only the seven most significant column addresses (A2–A8) are latched on the falling edge of $\overline{CAS}$. The two least significant addresses (A0–A1) are replaced by four DQ bits (DQ0–DQ3), which are also latched on the later of the falling edge of $\overline{CAS}$ or $\overline{W}$. These four bits are used as a column mask, and they indicate which of the four column-address locations addressed by A2–A8 are written with the contents of the color register during the block-write cycle. DQ0 enables a write to column-address A1 = 0 (low), A0 = 0 (low); DQ1 enables a write to column-address A1 = 0 (low), A0 = 1 (high); DQ2 enables a write to column-address A1 = 1 (high), A0 = 0 (low); DQ3 enables a write to column-address A1 = 1 (high), A0 = 1 (high). A high logic level enables a write, and a low logic level disables the write. A maximum of 16 bits (4 × 4) can be written to memory during each $\overline{CAS}$ cycle in the block-write mode.



† $\overline{W}$ must be low during the block-write cycle.

NOTE: DQ0–DQ3 are latched on the later of $\overline{W}$ or $\overline{CAS}$ falling edge except in block 6 (see legend).

Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8)
4. Color-register data
5. Column-mask data
6. DQ-mask data. DQ0–DQ3 are latched on the falling edge of $\overline{RAS}$.

= don't care

Figure 2. Example Block-Write Diagram Operations

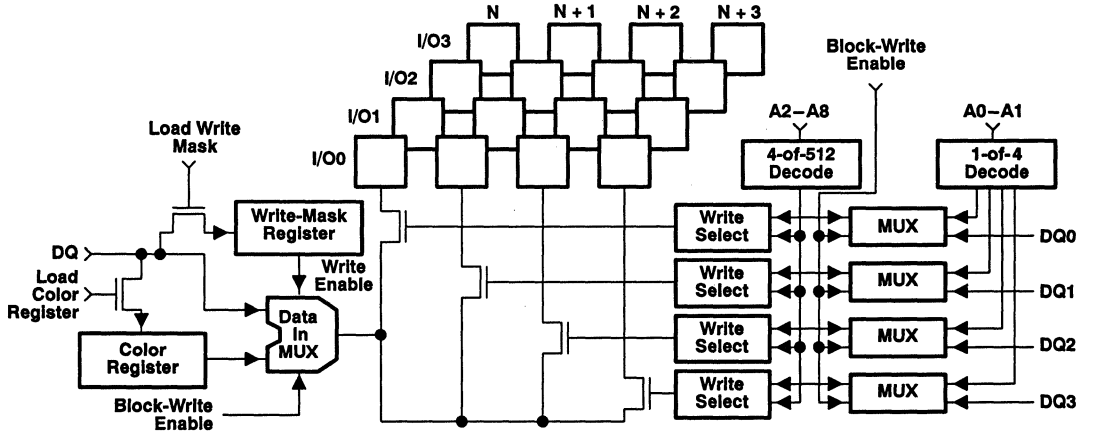


Figure 3. Block-Write Circuit Block Diagram

	DQ MASK	COLUMN MASK	COLOR REGISTER DATA
DQ0	1	0	0
DQ1	1	1	0
DQ2	0	1	1
DQ3	1	1	1

Block Write

	COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4
DQ0	Masked	0	0	0
DQ1	Masked	0	0	0
DQ2	Masked	Masked	Masked	Masked
DQ3	Masked	1	1	1

Figure 4. Example of Block Write Operation With DQ Mask and Address Mask

transfer operation

Transfer operations between the memory arrays (DRAM) and the data registers (SAM) are invoked by bringing $\overline{TRG}$ low before $\overline{RAS}$ falls. The states of $\overline{W}$, $\overline{SE}$, and DSF, which are also latched on the falling edge of $\overline{RAS}$, determine which transfer operation is invoked. Figure 5 shows an overview of data flow between the random and the serial interfaces.

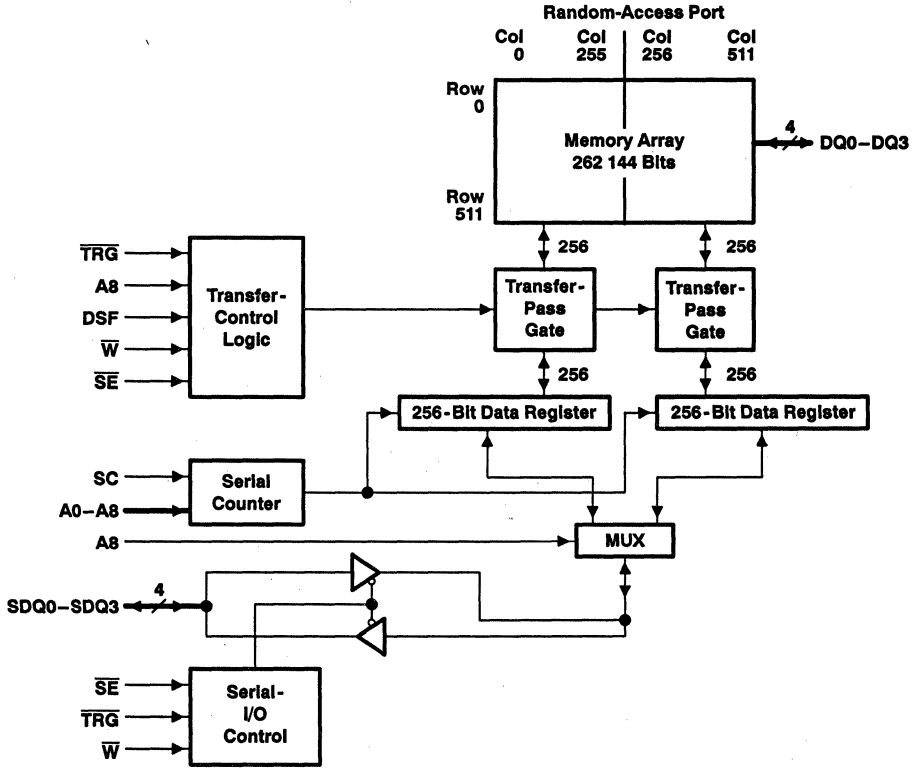


Figure 5. Block Diagram Showing One Random and One Serial-I/O Interface

As shown in Table 3, the SMJ44C251B supports five basic modes of transfer operation:

- Register-to-memory transfer (normal write transfer, SAM to DRAM)
- Alternate-write transfer (independent of the state of $\overline{SE}$)
- Memory-to-register transfer (pseudo-transfer write). Switches serial port from serial-out mode to serial-in mode. No actual data transfer takes place between the DRAM and the SAM.
- Memory-to-register transfer (normal-read transfer, transfer entire contents of DRAM row to SAM)
- Split-register-read transfer (divides the SAM into a low and a high half. Only one half is transferred to the SAM while the other half is read from the serial I/O port.)

Table 3. Transfer-Operation Functions

FUNCTION	$\overline{RAS}$ FALL					$\overline{CAS}$ FALL	ADDRESS		DQ0–DQ3	
	$\overline{CAS}$	$\overline{TRG}$	$\overline{W}$	DSF	$\overline{SE}$	DSF	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$ $\overline{W}$
Register-to-memory transfer (normal write transfer)	H	L	L	X	L	X	Row Addr	Tap Point	X	X
Alternate-write transfer (independent of $\overline{SE}$)	H	L	L	H	X	X	Row Addr	Tap Point	X	X
Serial-write-mode enable (pseudo-transfer write)	H	L	L	L	H	X	Refresh Addr	Tap Point	X	X
Memory-to-register transfer (normal read transfer)	H	L	H	L	X	X	Row Addr	Tap Point	X	X
Split-register-read transfer (must reload tap)	H	L	H	H	X	X	Row Addr	Tap Point	X	X

Legend:
H = High
L = Low
X = Don't care

write transfer

All write-transfer cycles (except the pseudo write transfer) transfer the entire content of SAM to the selected row in the DRAM. To invoke a write-transfer cycle, $\overline{W}$ must be low when $\overline{RAS}$ falls. There are three possible write-transfer operations: normal-write transfer, alternate-write transfer, and pseudo-write transfer.

All write-transfer cycles switch the serial port to the serial-in mode.

normal-write transfer (SAM-to-DRAM transfer)

A normal-write transfer cycle loads the contents of the serial-data register to a selected row in the memory array. $\overline{TRG}$, $\overline{W}$, and $\overline{SE}$ are brought low and latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available as the destination of the data transfer. The nine column-address bits (A0–A8) are latched at the falling edge of $\overline{CAS}$ to select one of the 512 tap points in SAM that are available for the next serial input.

During a write-transfer operation before $\overline{RAS}$ falls, the serial-input operation must be suspended after a minimum delay of $t_{d(SCRL)}$ but can be resumed after a minimum delay of $t_{d(RHSC)}$ after $\overline{RAS}$ goes high (see Figure 6).

normal-write transfer (SAM-to-DRAM transfer) (continued)

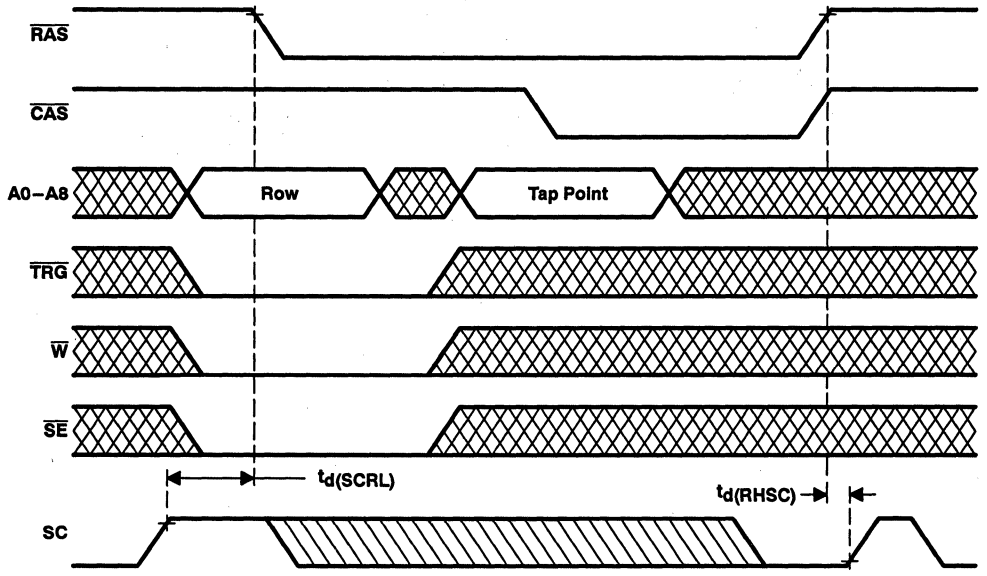


Figure 6. Normal-Write-Transfer-Cycle Timing

alternate-write transfer (refer to Figure 30)

When DSF is brought high and latched at the falling edge of $\overline{RAS}$ in the normal-write-transfer cycle, the alternate-write transfer occurs.

pseudo-write transfer (write-mode control) (refer to Figure 28)

To invoke the pseudo-write transfer (write-mode control cycle), $\overline{SE}$ is brought high and latched at the falling edge of $\overline{RAS}$. The pseudo-write transfer does not actually invoke any data transfer but switches the mode of the serial port from the serial-out (read) mode to the serial-in (write) mode.

Before serial data can be clocked into the serial port via the SDQ terminals and the SC input, the SDQ terminals must be switched into input mode. Because the transfer does not occur during the pseudo-transfer write, the row address (A0–A8) is in the don't care state and the column address (A0–A8), which is latched on the falling edge of $\overline{CAS}$, selects one of the 512 tap points in the SAM that are available for the next serial input.

read transfer (DRAM-to-SAM transfer) (refer to Figure 7)

During a read-transfer cycle, data from the selected row in DRAM is transferred to SAM. There are two read-transfer operations: normal-read transfer and split-register-read transfer.

normal-read transfer *(refer to Figure 7)*

The normal-read-transfer operation loads data from a selected row in DRAM into SAM. $\overline{TRG}$ is brought low and latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for transfer. The nine column-address bits (A0–A8) are latched at the falling edge of $\overline{CAS}$ to select one of the SAM's 512 available tap points where the serial data is read out.

A normal-read transfer can be performed in three ways: early-load read transfer, real-time or midline-load read transfer, and late-load read transfer. Each of these offers the flexibility of controlling the $\overline{TRG}$ trailing edge in the read-transfer cycle (see Figure 7).

normal-read transfer (continued)

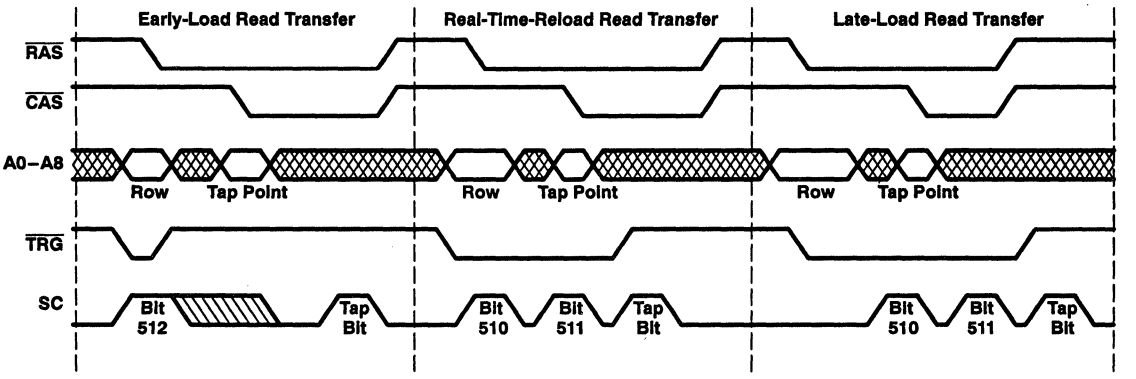


Figure 7. Normal-Read-Transfer Timings

split-register-read transfer

In split-register-read-transfer operation, the serial-data register is split into halves. The low half contains bits 0–255, and the high half contains 256–511. While one half is being read out of the SAM port, the other half can be loaded from the memory array.

To invoke a split-register read-transfer cycle, DSF is brought high, $\overline{TRG}$ is brought low, and both are latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. The nine column-address bits (A0–A8) are latched at the falling edge of $\overline{CAS}$, where address bits A0–A7 select one of the 255 tap points in the specified half of SAM and address bit A8 selects which half is to be transferred. If A8 is a logic low, the low half is transferred. If A8 is a logic high, the high half is transferred. SAM locations 255 and 511 cannot be used as tap points.

A normal-read transfer must precede the split-register-read transfer to ensure proper operation. After the normal-read-transfer cycle, the first split-register read transfer can follow immediately without any minimum SC requirement. However, there is a minimum requirement of a rising edge of SC between split-register read-transfer cycles.

QSF indicates which half of the SAM is being accessed during serial-access operation. When QSF is low, the serial-address pointer is accessing the lower (least significant) 256 bits of the SAM. When QSF is high, the pointer is accessing the higher (most significant) 256 bits of the SAM. QSF changes state upon completing a normal-read-transfer cycle. The tap point loaded during the current transfer cycle determines the state of QSF. In split-register read-transfer mode, QSF changes state when a boundary between the two register halves is reached (see Figure 12 and Figure 13).

split-register-read transfer (continued)

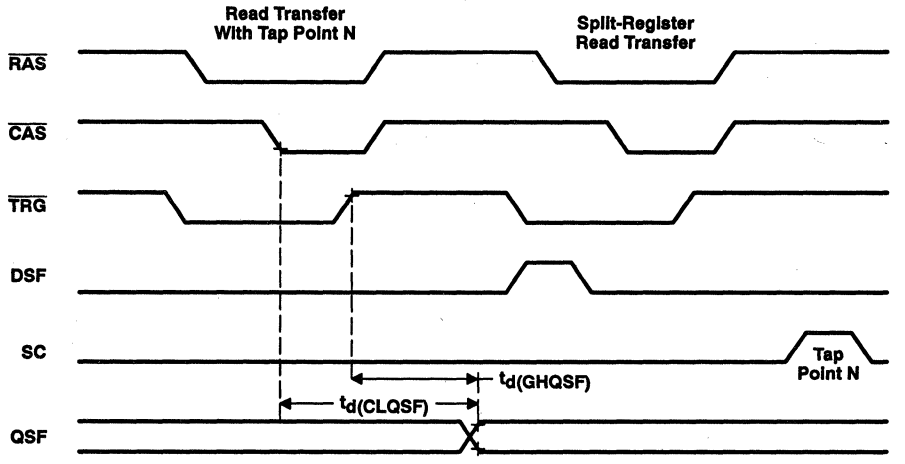


Figure 8. Example of a Split-Register Read-Transfer Cycle After a Normal Read-Transfer Cycle

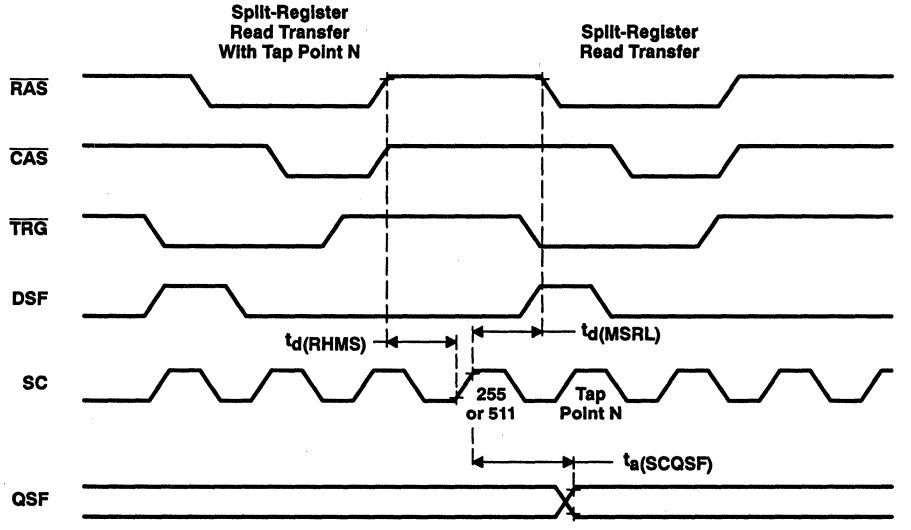


Figure 9. A Split-Register Read-Transfer Cycle After a Split-Register Read-Transfer Cycle

serial-access operation

The serial-read and serial-write operations can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during transfer operations. The preceding transfer operation determines the input or output state of the SAM port. If the preceding transfer operation is a read-transfer operation, the SAM port is in the output mode. If the preceding transfer operation is a write- or pseudo-write-transfer operation, the SAM port is in the input mode.

Serial data can be read out of or written into SAM by clocking SC starting at the tap point loaded by the preceding transfer cycle, proceeding sequentially to the most significant bit (bit 511), then wrapping around to the least significant bit (bit 0) (see Figure 10).

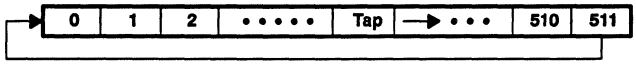


Figure 10. Serial Pointer Direction for Serial Read/Write

For split-register read-transfer operation, serial data can be read out from the active half of SAM by clocking SC starting at the tap point loaded by the preceding split-register-transfer cycle, then proceeding sequentially to the most significant bit of the half, bit 255 or bit 511. If there is a split-register-read transfer to the inactive half during this period, the serial pointer points next to the tap-point location loaded by that split register (see Figure 15, Case I). If there is no split-register read transfer to the inactive half during this period, the serial pointer points next to bit 256 or bit 0, respectively (see Figure 15, Case II).

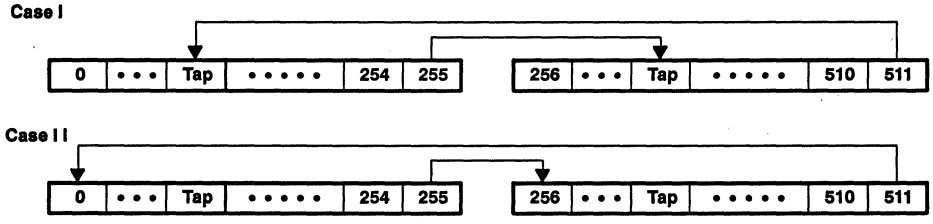


Figure 11. Serial Pointer for Split-Register Read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –1 V to 7 V
Voltage range on any pin (see Note 1) ..... –1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A: L suffix ..... 0°C to 70°C
M suffix ..... –55°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage		2.9		6.5	V
V_{IL}	Low-level input voltage (see Note 2)		–1		0.6	V
T_A	Operating free-air temperature	L suffix	0		70	°C
		M suffix	–55		125	
T_C	Operating case temperature	L suffix			70	°C
		M suffix			125	

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		V
V_{OL}	Low-level output voltage (see Note)	I_{OL} = 4.2 mA		0.4	V
I_I	Input leakage current	V_{CC} = 5 V, V_I = 0 V to 5.8 V, All others open		±10	µA
I_O	Output leakage current (see Note 4)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}		±10	µA

PARAMETER (SEE NOTE 5)		TEST CONDITIONS†	SAM PORT	'44C251B-10		'44C251B-12		UNIT
				MIN	MAX	MIN	MAX	
I_{CC1}	Operating current	$t_{c(rd)}$ and $t_{c(W)}$ = MIN	Standby		100		90	mA
I_{CC1A}	Operating current	$t_{c(SC)}$ = MIN	Active		110		100	
I_{CC2}	Standby current	All clocks = V_{CC}	Standby		15		15	
I_{CC2A}	Standby current	$t_{c(SC)}$ = MIN	Active		35		35	
I_{CC3}	$\overline{RAS}$-only refresh current	$t_{c(rd)}$ and $t_{c(W)}$ = MIN	Standby		100		90	
I_{CC3A}	$\overline{RAS}$-only refresh current	$t_{c(SC)}$ = MIN	Active		110		100	
I_{CC4}	Page-mode current	$t_{c(P)}$ = MIN	Standby		65		60	
I_{CC4A}	Page-mode current	$t_{c(SC)}$ = MIN	Active		70		65	
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ current	$t_{c(rd)}$ and $t_{c(W)}$ = MIN	Standby		90		80	
I_{CC5A}	$\overline{CAS}$-before-$\overline{RAS}$ current	$t_{c(SC)}$ = MIN	Active		110		100	
I_{CC6}	Data-transfer current	$t_{c(rd)}$ and $t_{c(W)}$ = MIN	Standby		100		90	
I_{CC6A}	Data-transfer current	$t_{c(SC)}$ = MIN	Active		110		100	

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

NOTES: 3. The SMJ44C251B may exhibit simultaneous switching noise as described in the Texas Instruments *Advanced CMOS Logic Designer's Handbook*. This phenomenon is exhibited on the DQ terminals when the SDQ terminals are switched and on the SDQ terminals when the DQ terminals are switched. This may cause V_{OL} and V_{OH} to exceed the data-book limit for a short period of time, depending upon output loading and temperature. Care should be taken to provide proper termination, decoupling, and layout of the device to minimize simultaneous switching effects.

4. $\overline{SE}$ is disabled for SDQ output leakage tests.

5. I_{CC} (standby) denotes that the SAM port is inactive (standby) and the DRAM port is active (except for I_{CC2}).
I_{CCA} (active) denotes that the SAM port is active and the DRAM port is active (except for I_{CC2}).
I_{CC} is measured with no load on DQ or SDQ.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A8		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{o(O)}$	Output capacitance, SDQs and DQs		9	pF
$C_{o(QSF)}$	Output capacitance, QSF		9	pF

NOTE 6: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25°C with a 1-MHz signal applied to the terminal under test. All other terminals are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		TEST CONDITIONS †	ALT. SYMBOL	'44C251B-10		'44C251B-12		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		25		30	ns
$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{AA}		50		60	ns
$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = MAX	t_{CPA}		55		65	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MAX	t_{RAC}		100		120	ns
$t_{a(G)}$	Access time of DQ0–DQ3 from $\overline{TRG}$ low		t_{OEA}		25		30	ns
$t_{a(SQ)}$	Access time of SDQ0–SDQ3 from SC high	C_L = 30 pF	t_{SCA}		30		35	ns
$t_{a(SE)}$	Access time of SDQ0–SDQ3 from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		20		25	ns
$t_{dis(CH)}$	Disable time, random output from $\overline{CAS}$ high (see Note 8)	C_L = 100 pF	t_{OFF}	0	20	0	20	ns
$t_{dis(G)}$	Disable time, random output from $\overline{TRG}$ high (see Note 8)	C_L = 100 pF	t_{OEZ}	0	20	0	20	ns
$t_{dis(SE)}$	Disable time, serial output from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	0	20	0	20	ns

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

NOTES: 7. Switching times assume C_L = 100 pF unless otherwise noted (see Figure 12).

8. $t_{dis(CH)}$, $t_{dis(G)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature†

		ALT. SYMBOL	'44C251B-10		'44C251B-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Cycle time, read (see Note 9)	t_{RC}	190		220		ns
$t_{c(W)}$	Cycle time, write (see Note 9)	t_{WC}	190		220		ns
$t_{c(rdW)}$	Cycle time, read-modify-write (see Note 9)	t_{RMW}	250		290		ns
$t_{c(P)}$	Cycle time, page-mode read or write (see Note 9)	t_{PC}	60		70		ns
$t_{c(rdWP)}$	Cycle time, page-mode read-modify-write (see Note 9)	t_{PRMW}	105		125		ns
$t_{c(TRD)}$	Cycle time, read transfer (see Note 9)	t_{RC}	190		220		ns
$t_{c(TW)}$	Cycle time, write transfer (see Note 9)	t_{WC}	190		220		ns
$t_{c(SC)}$	Cycle time, serial clock (see Notes 9 and 10)	t_{SCC}	30		35		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CPN}	20		30		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 11)	t_{CAS}	25	75000	30	75000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	80		90		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 12)	t_{RAS}	100	75000	120	75000	ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	t_{WP}	25		25		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		25		30		ns
$t_{w(SCH)}$	Pulse duration, SC high	t_{SC}	10		12		ns
$t_{w(SCL)}$	Pulse duration, SC low	t_{SCP}	10		12		ns
$t_{w(SEL)}$	Pulse duration, $\overline{SE}$ low	t_{SE}	35		40		ns
$t_{w(SEH)}$	Pulse duration, $\overline{SE}$ high	t_{SEP}	35		40		ns
$t_{w(GH)}$	Pulse duration, $\overline{TRG}$ high	t_{TP}	30		30		ns
$t_{w(RL)P}$	Pulse duration, $\overline{RAS}$ low (page mode)		100	75000	120	75000	ns
$t_{su(CA)}$	Setup time, column address	t_{ASC}	0		0		ns
$t_{su(SFC)}$	Setup time, DSF before $\overline{CAS}$ low	t_{FSC}	0		0		ns
$t_{su(RA)}$	Setup time, row address	t_{ASR}	0		0		ns
$t_{su(WMR)}$	Setup time, $\overline{W}$ before $\overline{RAS}$ low	t_{WSR}	0		0		ns
$t_{su(DQR)}$	Setup time, DQ before $\overline{RAS}$ low	t_{MS}	0		0		ns
$t_{su(TRG)}$	Setup time, $\overline{TRG}$ before $\overline{RAS}$ low	t_{THS}	0		0		ns
$t_{su(SE)}$	Setup time, $\overline{SE}$ before $\overline{RAS}$ low (see Note 13)	t_{ESR}	0		0		ns
$t_{su(SESC)}$	Setup time, serial write disable	t_{SWIS}	10		15		ns
$t_{su(SFR)}$	Setup time, DSF before $\overline{RAS}$ low	t_{FSR}	0		0		ns
$t_{su(DCL)}$	Setup time, data before $\overline{CAS}$ low	t_{DSC}	0		0		ns
$t_{su(DWL)}$	Setup time, data before $\overline{W}$ low	t_{DSW}	0		0		ns
$t_{su(rd)}$	Setup time, read command	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Setup time, early write command before $\overline{CAS}$ low	t_{WCS}	0		0		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. All cycle times assume t_t = 5 ns.

10. When the odd tap is used (tap address can be 0–511, and odd taps are 1, 3, 5, etc.), the cycle time for SC in the first serial data out cycle needs to be 70 ns minimum.
11. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].
12. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].
13. Register-to-memory (write) transfer cycles only

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	'44C251B-10		'44C251B-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{su(WCH)}$	Setup time, write before $\overline{CAS}$ high	t_{CWL}	25		30		ns
$t_{su(WRH)}$	Setup time, write before $\overline{RAS}$ high with $\overline{TRG}$ = $\overline{W}$ = low	t_{RWL}	25		30		ns
$t_{su(SDS)}$	Setup time, SDQ before SC high	t_{SDS}	0		0		ns
$t_{h(CLCA)}$	Hold time, column address after $\overline{CAS}$ low	t_{CAH}	20		20		ns
$t_{h(SFC)}$	Hold time, DSF after $\overline{CAS}$ low	t_{CFH}	20		20		ns
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low	t_{RAH}	15		15		ns
$t_{h(TRG)}$	Hold time, $\overline{TRG}$ after $\overline{RAS}$ low	t_{TLH}	15		15		ns
$t_{h(SE)}$	Hold time, $\overline{SE}$ after $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low (see Note 13)	t_{REH}	15		15		ns
$t_{h(RWM)}$	Hold time, write mask, transfer enable after $\overline{RAS}$ low	t_{RWH}	15		15		ns
$t_{h(RDQ)}$	Hold time, DQ after $\overline{RAS}$ low (write-mask operation)	t_{MH}	15		15		ns
$t_{h(SFR)}$	Hold time, DSF after $\overline{RAS}$ low	t_{RFH}	15		15		ns
$t_{h(RLCA)}$	Hold time, column address after $\overline{RAS}$ low (see Note 14)	t_{AR}	45		45		ns
$t_{h(CLD)}$	Hold time, data after $\overline{CAS}$ low	t_{DH}	20		25		ns
$t_{h(RLD)}$	Hold time, data after $\overline{RAS}$ low (see Note 14)	t_{DHR}	45		50		ns
$t_{h(WLD)}$	Hold time, data after $\overline{W}$ low	t_{DH}	20		25		ns
$t_{h(CHrd)}$	Hold time, read after $\overline{CAS}$ high (see Note 15)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Hold time, read after $\overline{RAS}$ high (see Note 15)	t_{RRH}	10		10		ns
$t_{h(CLW)}$	Hold time, write after $\overline{CAS}$ low	t_{WCH}	30		35		ns
$t_{h(RLW)}$	Hold time, write after $\overline{RAS}$ low (see Note 14)	t_{WCR}	50		55		ns
$t_{h(WLG)}$	Hold time, $\overline{TRG}$ after $\overline{W}$ low (see Note 16)	t_{OEH}	25		30		ns
$t_{h(SDS)}$	Hold time, SDQ after SC high	t_{SDH}	5		5		ns
$t_{h(SHSQ)}$	Hold time, SDQ after SC high	t_{SOH}	5		5		ns
$t_{h(RSF)}$	Hold time, DSF after $\overline{RAS}$ low	t_{FHR}	45		45		ns
$t_{h(SCSE)}$	Hold time, serial-write disable	t_{SWIH}	20		20		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Notes 17 and)	t_{CWD}	55		65		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 19)	t_{RCD}	25	75	25	90	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	50		60		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 17)	t_{RWD}	130		155		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 17)	t_{AWD}	85		100		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 13. Register-to-memory (write) transfer cycles only
14. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
15. Either $t_{h(RHrd)}$ or $t_{(CHrd)}$ must be satisfied for a read cycle.
16. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
17. Read-modify-write operation only
18. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ terminals.
19. The maximum value is specified only to assure $\overline{RAS}$ access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	'44C251B-10		'44C251B-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{d(RLCH)RF}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 20)	t_{CHR}	25		25		ns
$t_{d(CLRL)RF}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 20)	t_{CSR}	10		10		ns
$t_{d(RHCL)RF}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 20)	t_{RPC}	10		10		ns
$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high for DRAM read cycles		25		30		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ	t_{OED}	25		30		ns
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (real-time-reload read-transfer cycle only)	t_{RTH}	90		95		ns
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 21)	t_{RSD}	130		140		ns
$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 21)	t_{CSD}	40		45		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 21 and 22)	t_{TSL}	15		20		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Notes 22 and 23)	t_{TRD}	−10		−10		ns
$t_{d(SCRL)}$	Delay time, SC high to $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low (see Notes 13 and 26)	t_{SRS}	10		20		ns
$t_{d(SCSE)}$	Delay time, SC high to $\overline{SE}$ high in serial-input mode		20		20		ns
$t_{d(RHSC)}$	Delay time, $\overline{RAS}$ high to SC high (see Note 13)	t_{SRD}	25		30		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 22)	t_{TRP}	$t_{w(RH)}$		$t_{w(RH)}$		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Notes 22)	t_{TSD}	35		40		ns
$t_{d(SESC)}$	Delay time, $\overline{SE}$ low to SC high (see Note 25)	t_{SWS}	10		15		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split-register read-transfer cycles		15		20		ns
$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high in real-time read-transfer cycles	t_{CTH}	5		5		ns
$t_{d(CASH)}$	Delay time, column address to first SC in early-load read-transfer cycles	t_{ASD}	45		50		ns
$t_{d(CAGH)}$	Delay time, column address to $\overline{TRG}$ high in real-time read-transfer cycles	t_{ATH}	10		10		ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address	t_{RAD}	15	50	15	60	ns
$t_{d(DCL)}$	Delay time, data to $\overline{CAS}$ low	t_{DZC}	0		0		ns
$t_{d(DGL)}$	Delay time, data to $\overline{TRG}$ low	t_{DZO}	0		0		ns
$t_{d(RLSD)}$	Delay time, $\overline{RAS}$ low to serial-input data	t_{SDD}	50		50		ns
$t_{d(GLRH)}$	Delay time, $\overline{TRG}$ low to $\overline{RAS}$ high	t_{ROH}	25		30		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 13. Register-to-memory (write) transfer cycles only
19. The maximum value is specified only to assure $\overline{RAS}$ access time.
20. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only
21. Early-load read-transfer cycle only
22. Real-time-reload read-transfer cycle only
23. Late-load read-transfer cycle only
24. Memory-to-register (read) and register-to-memory (write) transfer cycles only
25. Serial data-in cycles only
26. In a read-transfer cycle, the state of SC when $\overline{RAS}$ falls is a don't care condition. However, to assure proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{RAS}$ goes low.
27. In a memory-to-register (read) transfer cycle, $t_{d(SCRL)}$ applies only when the SAM was previously in serial-input mode.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)†

		ALT. SYMBOL	'44C251B-10		'44C251B-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{d(MSRL)}$	Delay time, last (most significant) rising edge of SC to $\overline{RAS}$ low before boundary switch during split-register read-transfer cycles		25		25		ns
$t_{d(SCQSF)}$	Delay time, last (255 or 511) rising edge of SC to QSF switching at the boundary during split-register read-transfer cycles (see Note 7)	t_{SQD}		40		40	ns
$t_{d(CLQSF)}$	Delay time, $\overline{CAS}$ low to QSF switching in read-transfer or write-transfer cycles (see Note 7)	t_{CQD}		35		35	ns
$t_{d(GHQSF)}$	Delay time, $\overline{TRG}$ high to QSF switching in read-transfer or write-transfer cycles (see Note 7)	t_{TQD}		30		30	ns
$t_{d(RLQSF)}$	Delay time, $\overline{RAS}$ low to QSF switching in read-transfer or write-transfer cycles (see Note 7)	t_{RQD}		75		75	ns
t_{rf}	Refresh time interval, memory	t_{REF}		8		8	ms
t_t	Transition time	t_T	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.
NOTE 7: Switching times assume C_L = 100 pF unless otherwise noted (see Figure 12).

PARAMETER MEASUREMENT INFORMATION

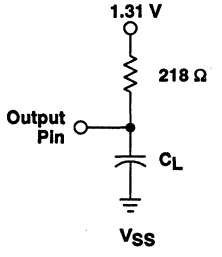


Figure 12. Load Circuit

PARAMETER MEASUREMENT INFORMATION

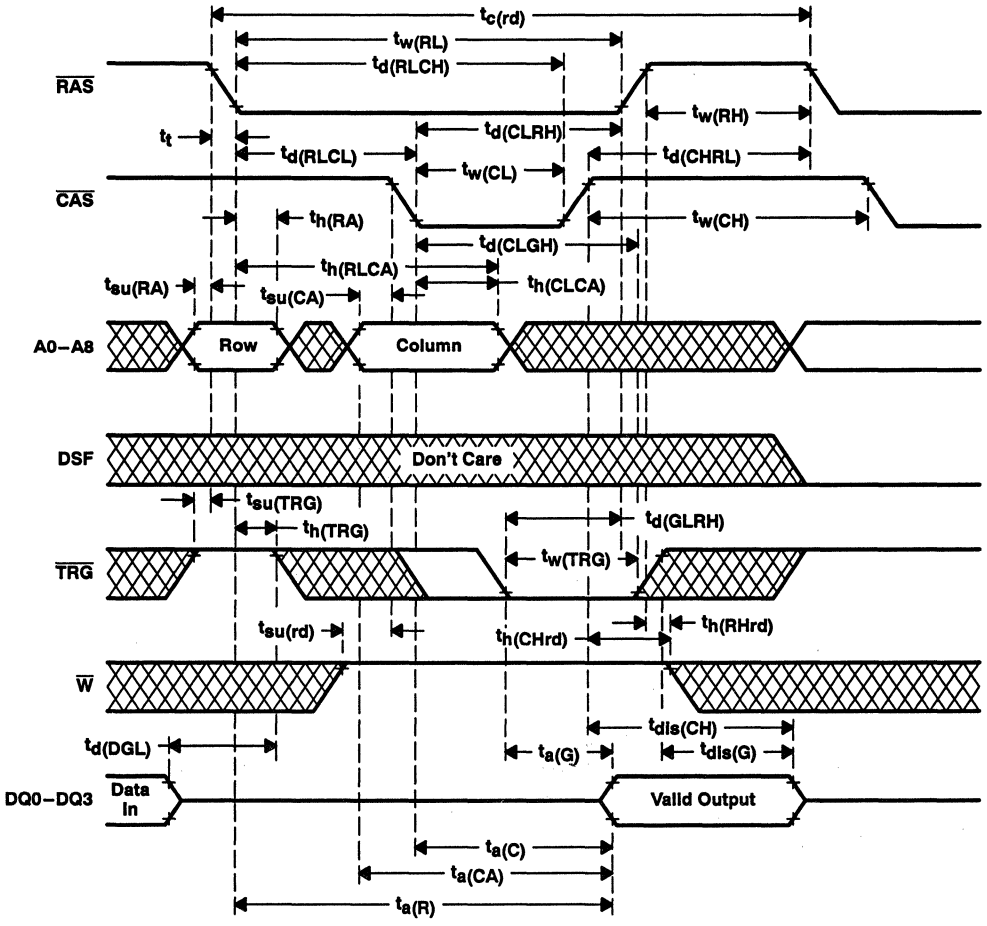


Figure 13. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

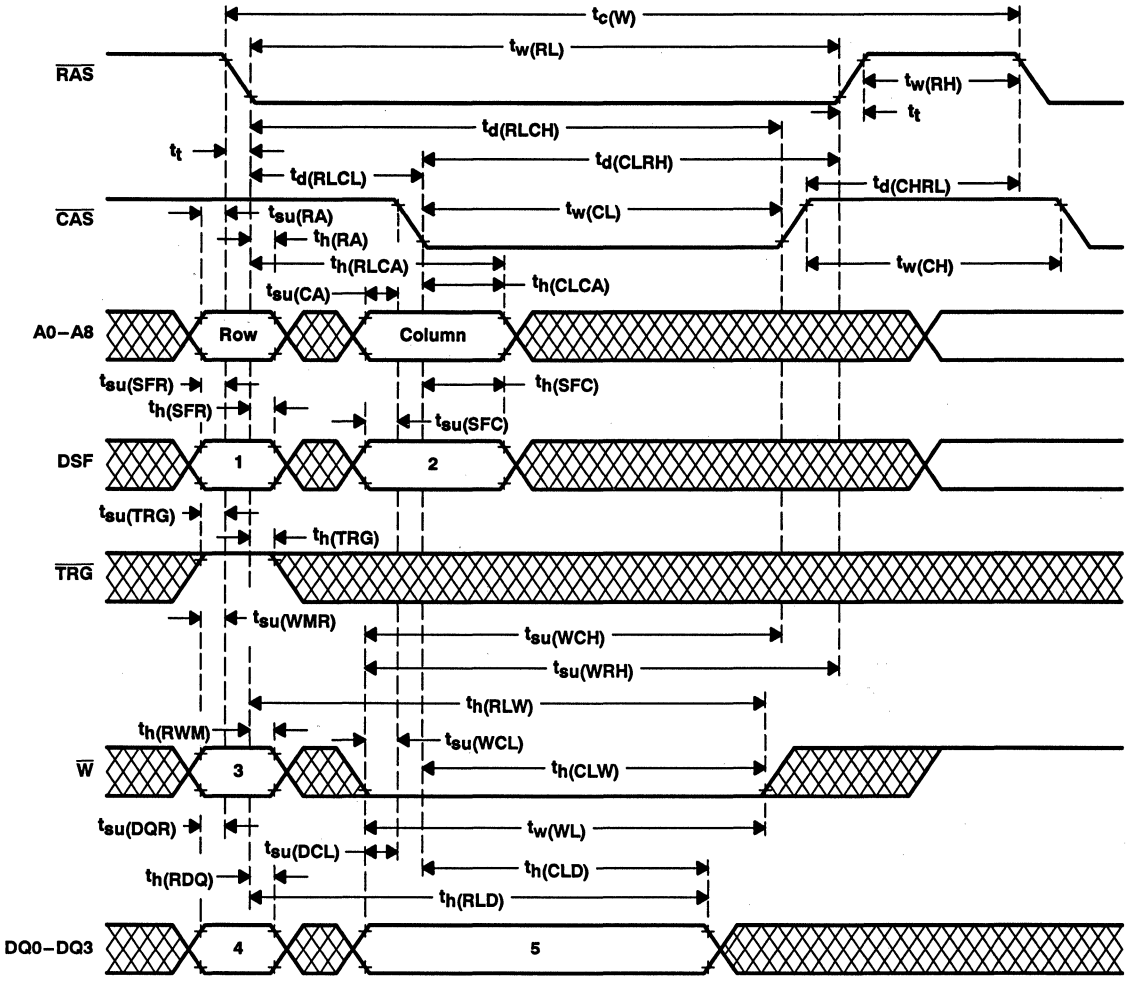


Figure 14. Early-Write-Cycle Timing

Table 4. Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation	L	L	H	Don't care	Valid data
Write-mask load/use, write DQs to I/Os	L	L	L	Write mask	Valid data
Use previous write mask, write DQs to I/Os	H	L	L	Don't care	Valid data
Load write mask on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	L	H	Don't care	Write mask

PARAMETER MEASUREMENT INFORMATION

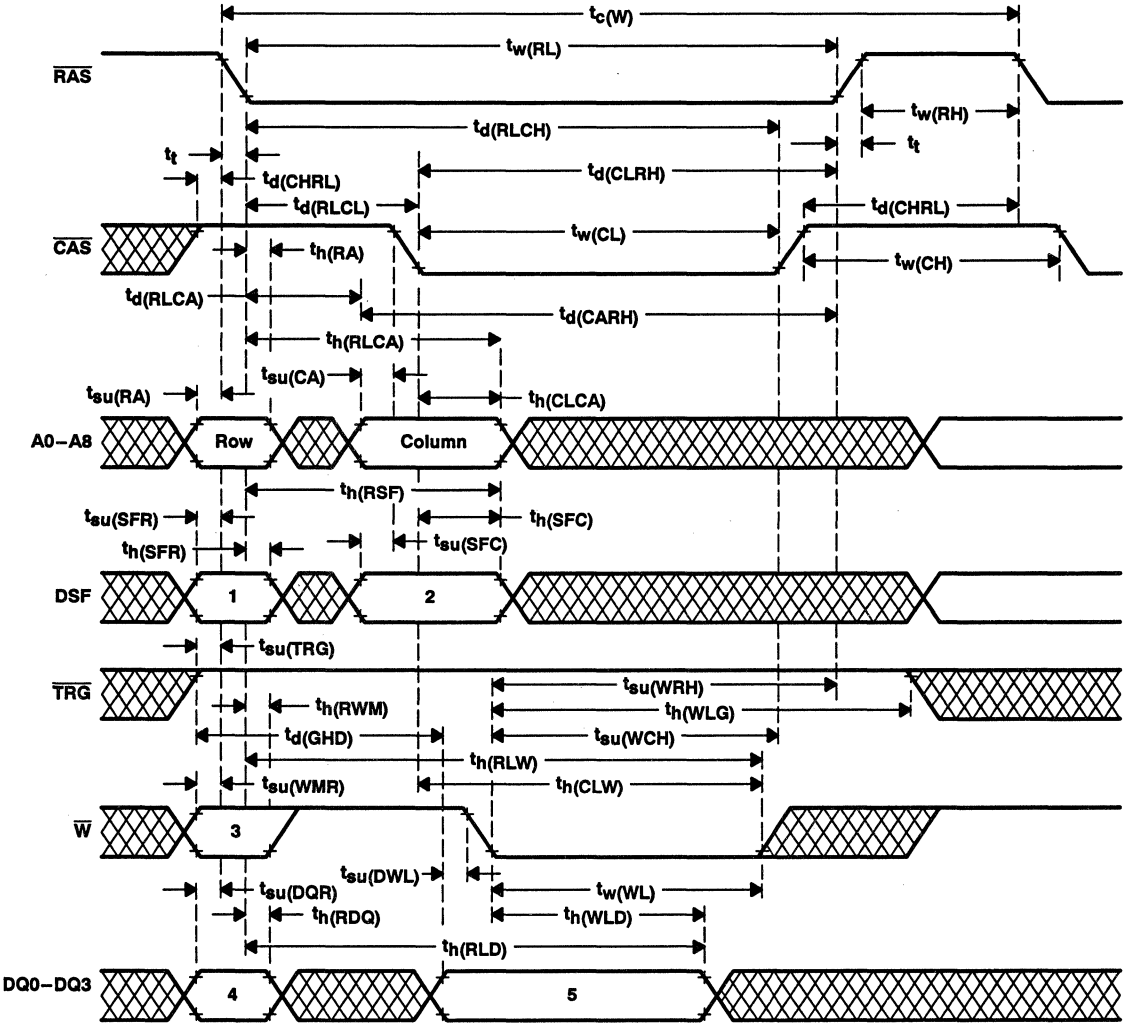


Figure 15. Delayed-Write-Cycle Timing (Output-Enable-Controlled Write)

Table 5. Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation	L	L	H	Don't care	Valid data
Write-mask load/use, write DQs to I/Os	L	L	L	Write mask	Valid data
Use previous write mask, write DQs to I/Os	H	L	L	Don't care	Valid data
Load write mask on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	L	H	Don't care	Write mask

PARAMETER MEASUREMENT INFORMATION

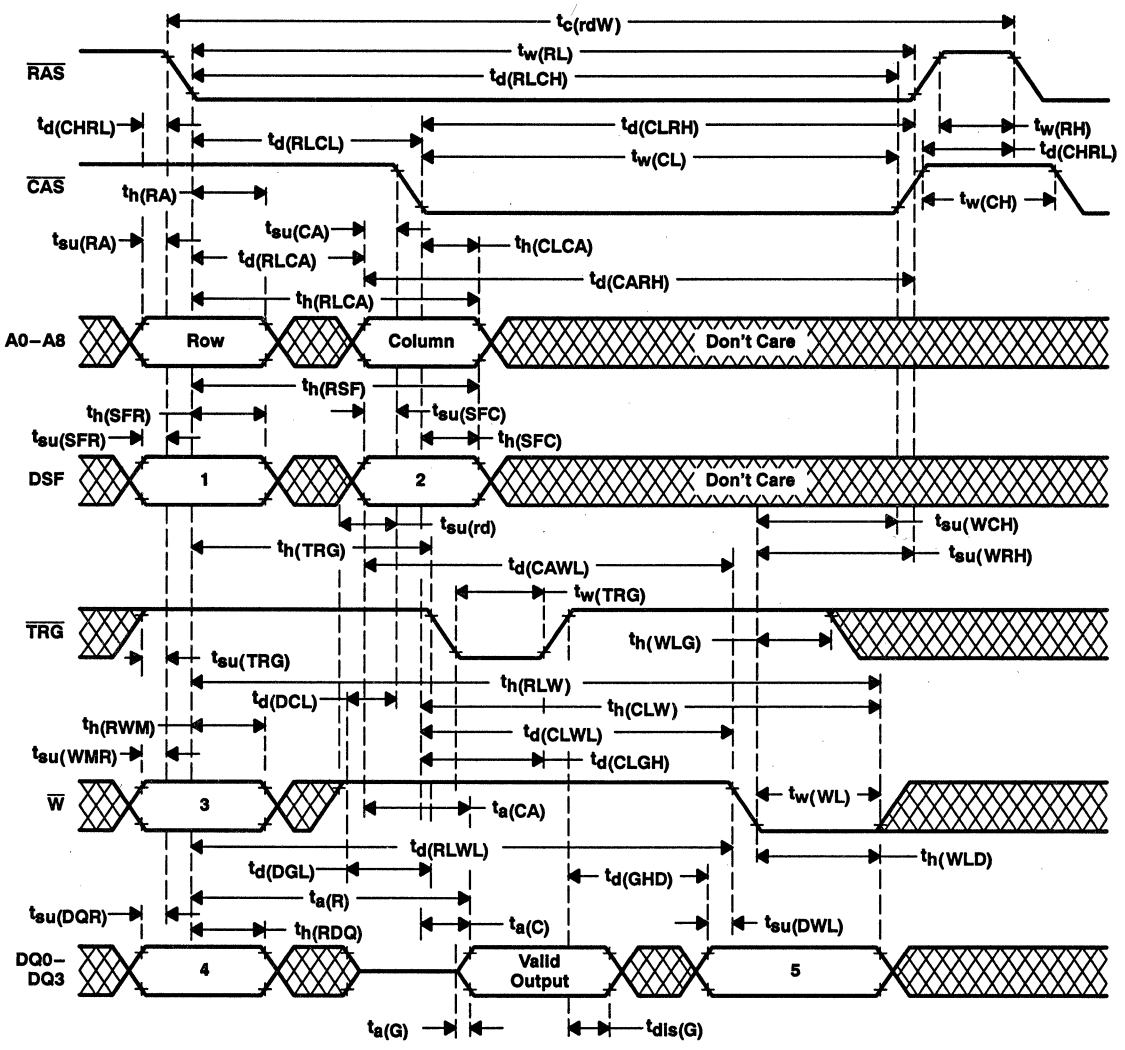
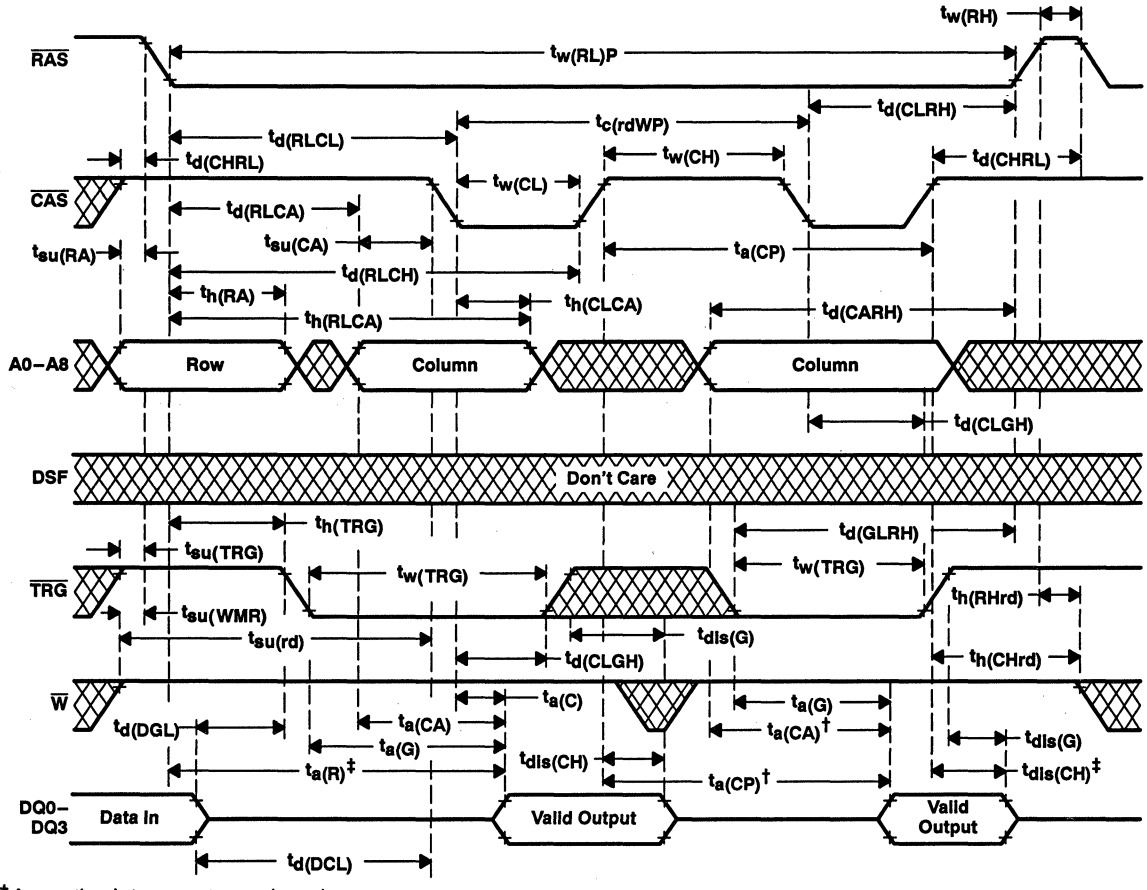


Figure 16. Read-Write/Read-Modify-Write-Cycle Timing

Table 6. Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation	L	L	H	Don't care	Valid data
Write-mask load/use, write DQs to I/Os	L	L	L	Write mask	Valid data
Use previous write mask, write DQs to I/Os	H	L	L	Don't care	Valid data
Load write mask on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	L	H	Don't care	Write mask

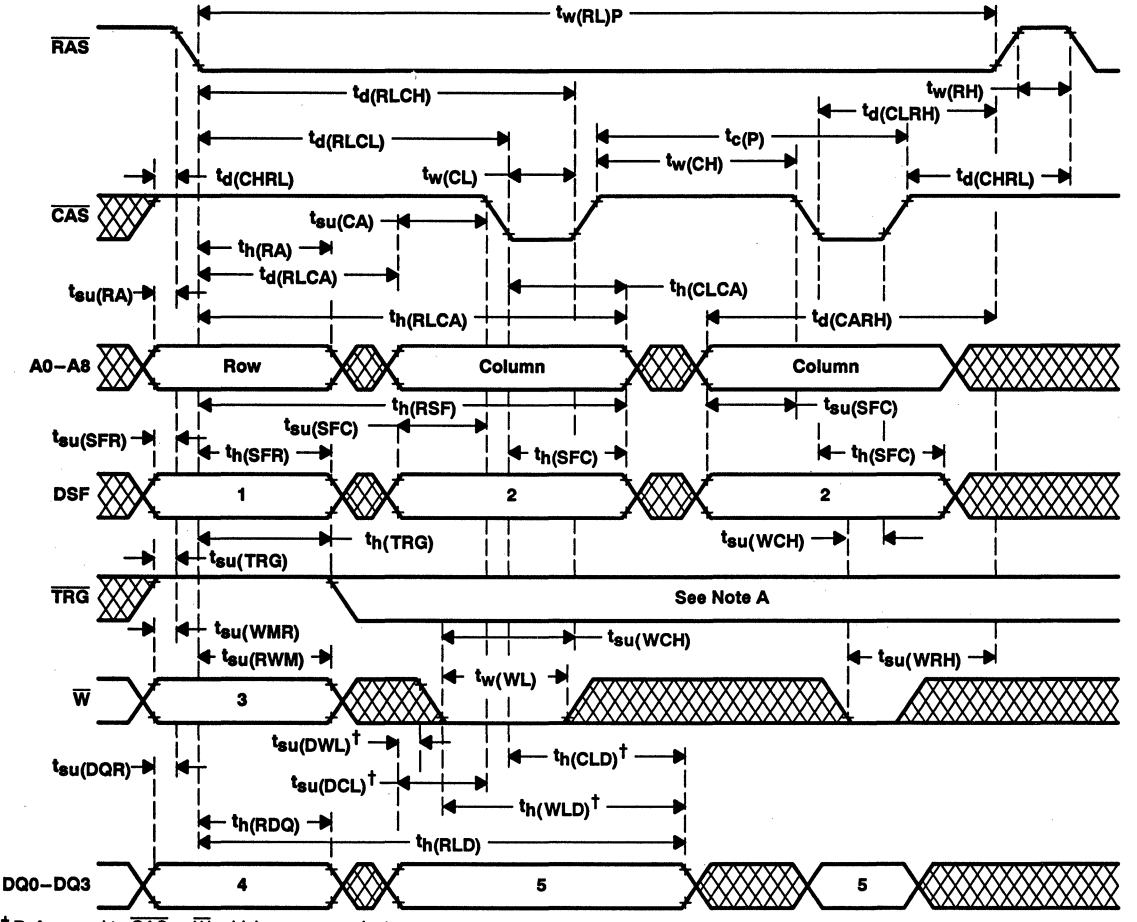
PARAMETER MEASUREMENT INFORMATION



† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output can go from the high-impedance state to an invalid data state prior to the specified access time.
NOTE: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edges of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.)

Figure 17. Enhanced-Page-Mode Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last

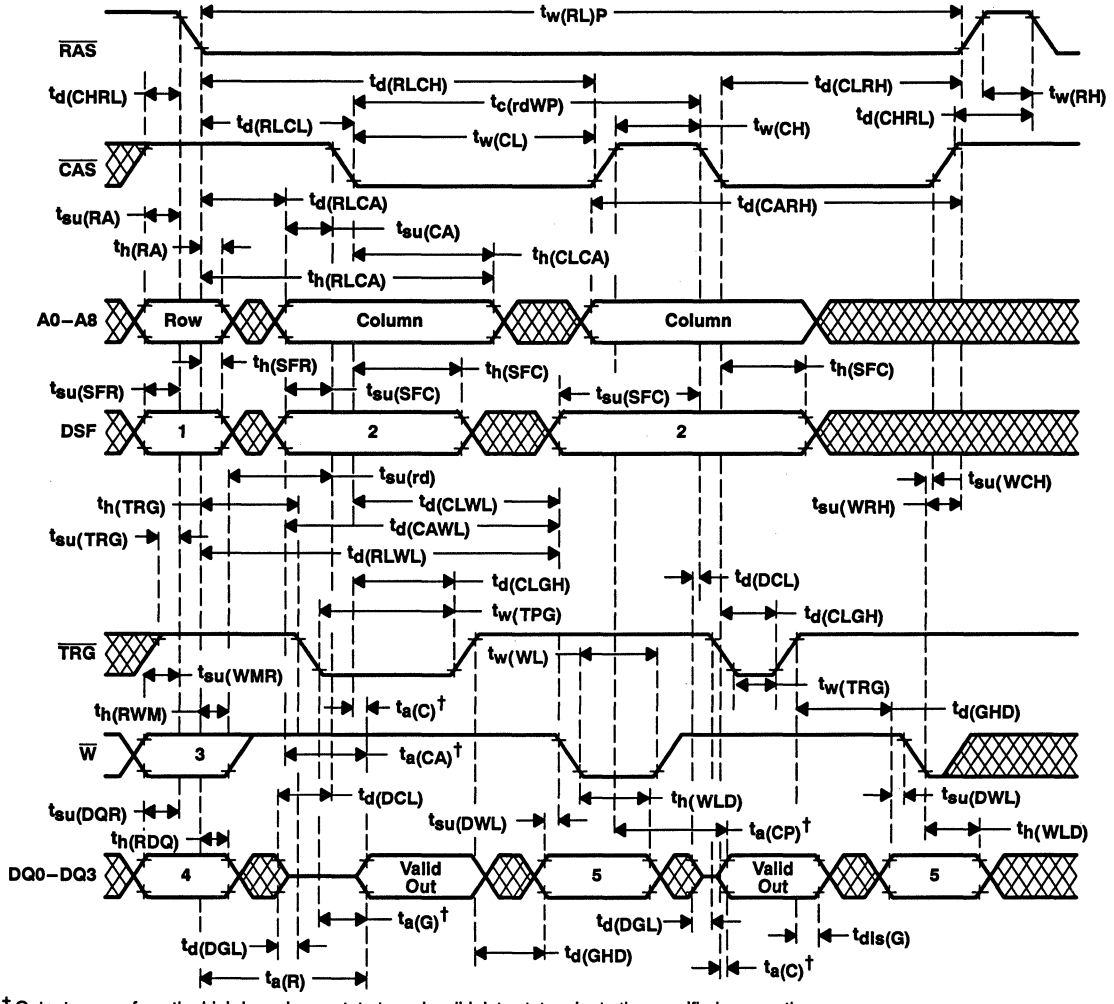
NOTE A: A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. $\overline{TRG}$ must remain high throughout the entire page-mode operation to assure page-mode cycle time if the late-write feature is used. If the early-write-cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 18. Enhanced-Page-Mode Write-Cycle Timing

Table 7. Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation	L	L	H	Don't care	Valid data
Write-mask load/use, write DQs to I/Os	L	L	L	Write mask	Valid data
Use previous write mask, write DQs to I/Os	H	L	L	Don't care	Valid data
Load write mask on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	L	H	Don't care	Write mask

PARAMETER MEASUREMENT INFORMATION



† Output can go from the high-impedance state to an invalid data state prior to the specified access time.
NOTE: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 19. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

Table 8. Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation	L	L	H	Don't care	Valid data
Write-mask load/use, write DQs to I/Os	L	L	L	Write mask	Valid data
Use previous write mask, write DQs to I/Os	H	L	L	Don't care	Valid data
Load write mask on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	L	H	Don't care	Write mask

PARAMETER MEASUREMENT INFORMATION

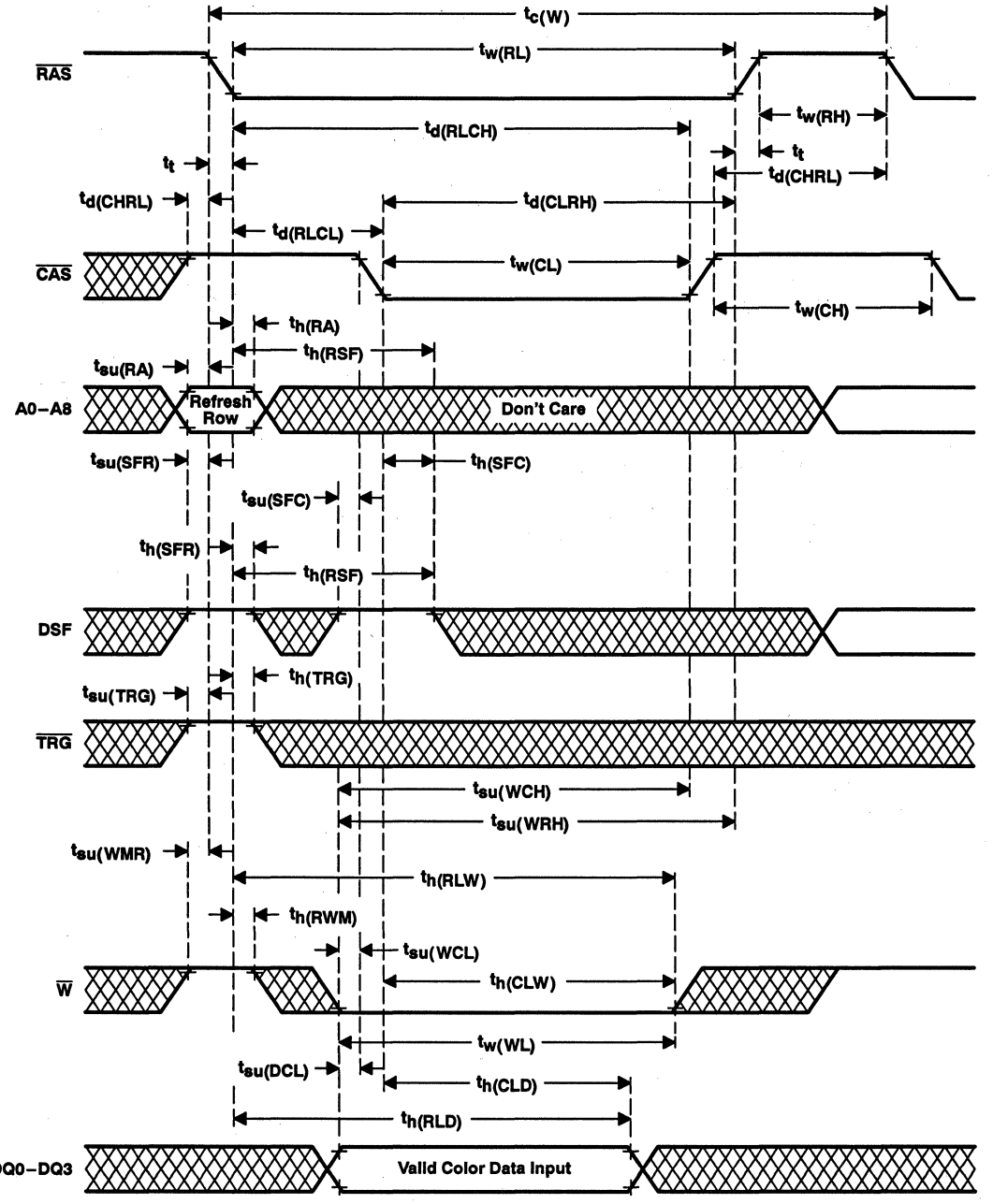


Figure 20. Load-Color-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION

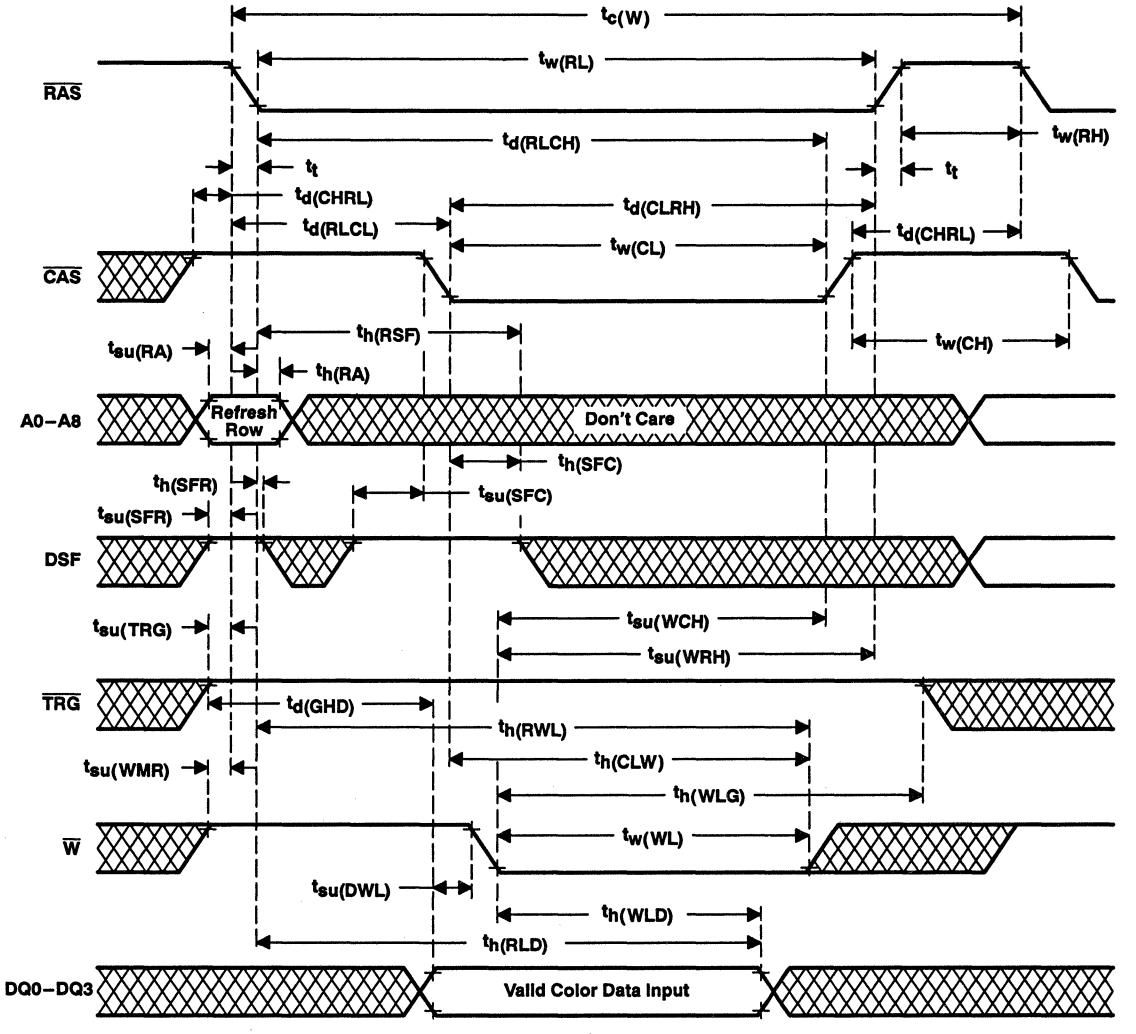


Figure 21. Load-Color-Register-Cycle Timing (Delayed-Write Load)

PARAMETER MEASUREMENT INFORMATION

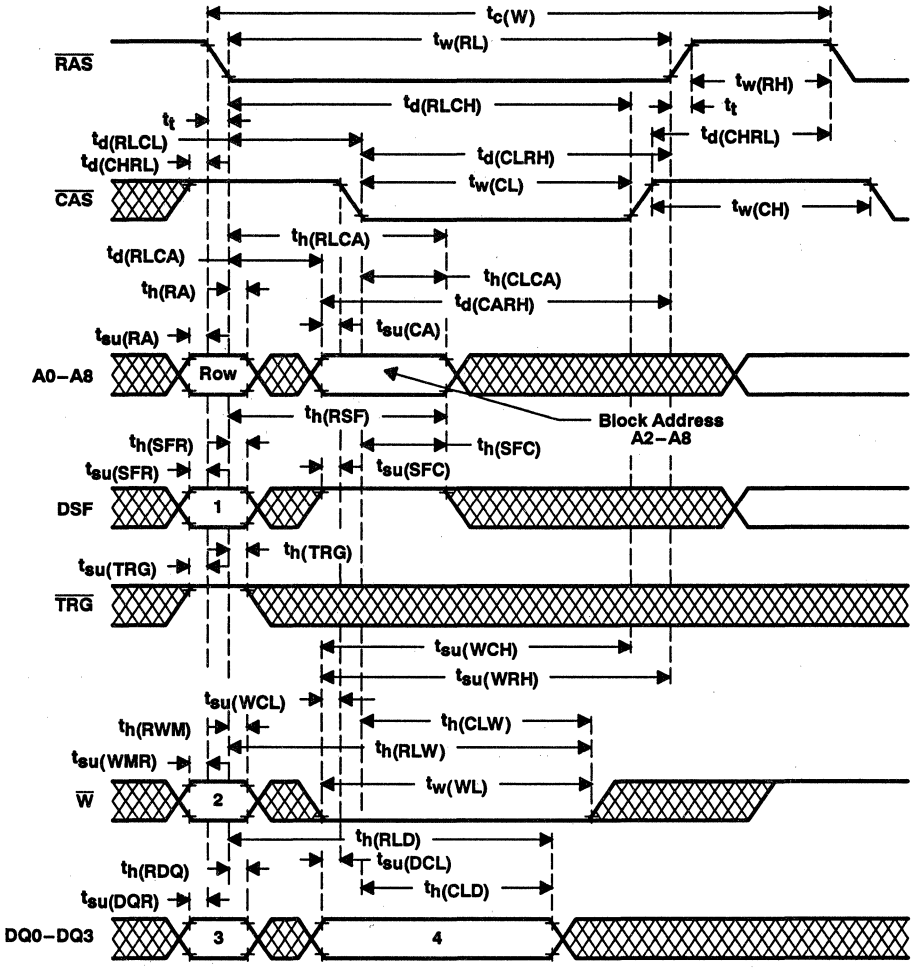


Figure 22. Block-Write-Cycle Timing (Early Write)

Table 9. Block-Write-Cycle State Table

CYCLE	STATE			
	1	2	3	4
Write-mask load/use, block write	L	L	Write mask	Column mask
Use previous write mask, block write	H	L	Don't care	Column mask
Write mask disabled, block write to all I/Os	L	H	Don't care	Column mask

Write mask data 0: I/O write disable
1: I/O write enable
Column mask data DQn = 0 column write disable
(n = 0, 1, 2, 3) 1 column write enable

DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

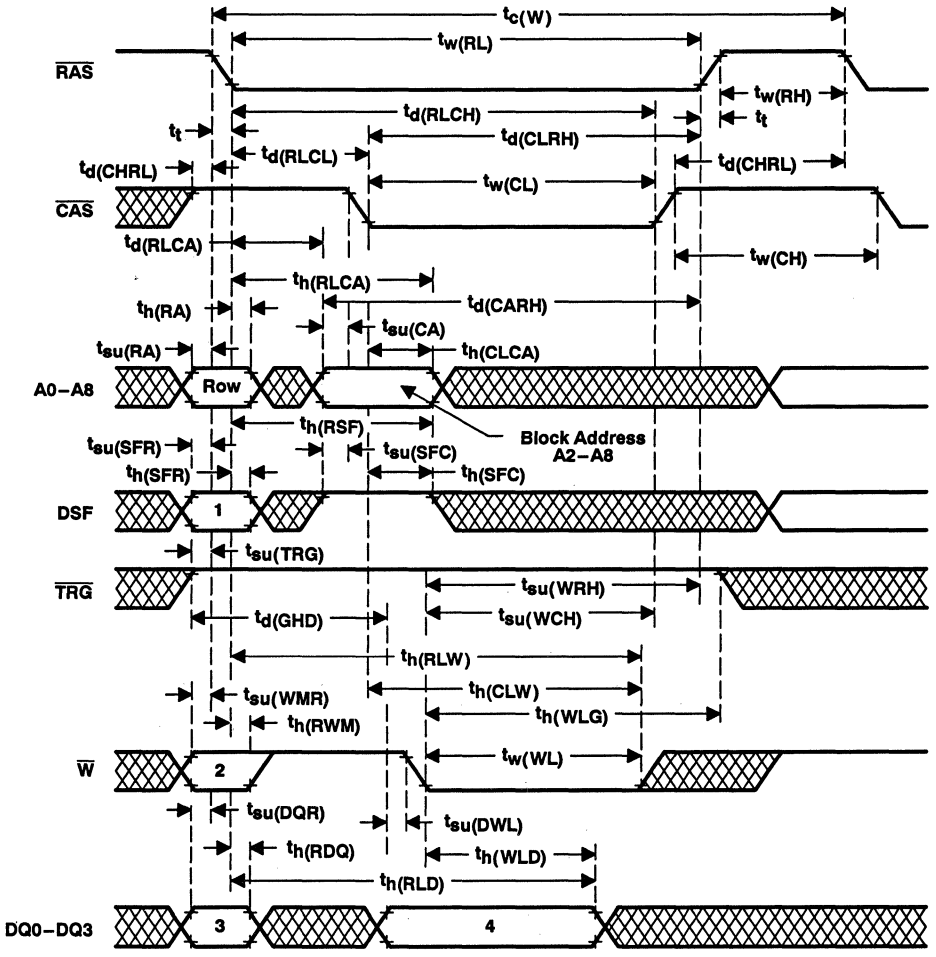


Figure 23. Block-Write-Cycle Timing (Delayed-Write)

Table 10. Block-Write-Cycle State Table

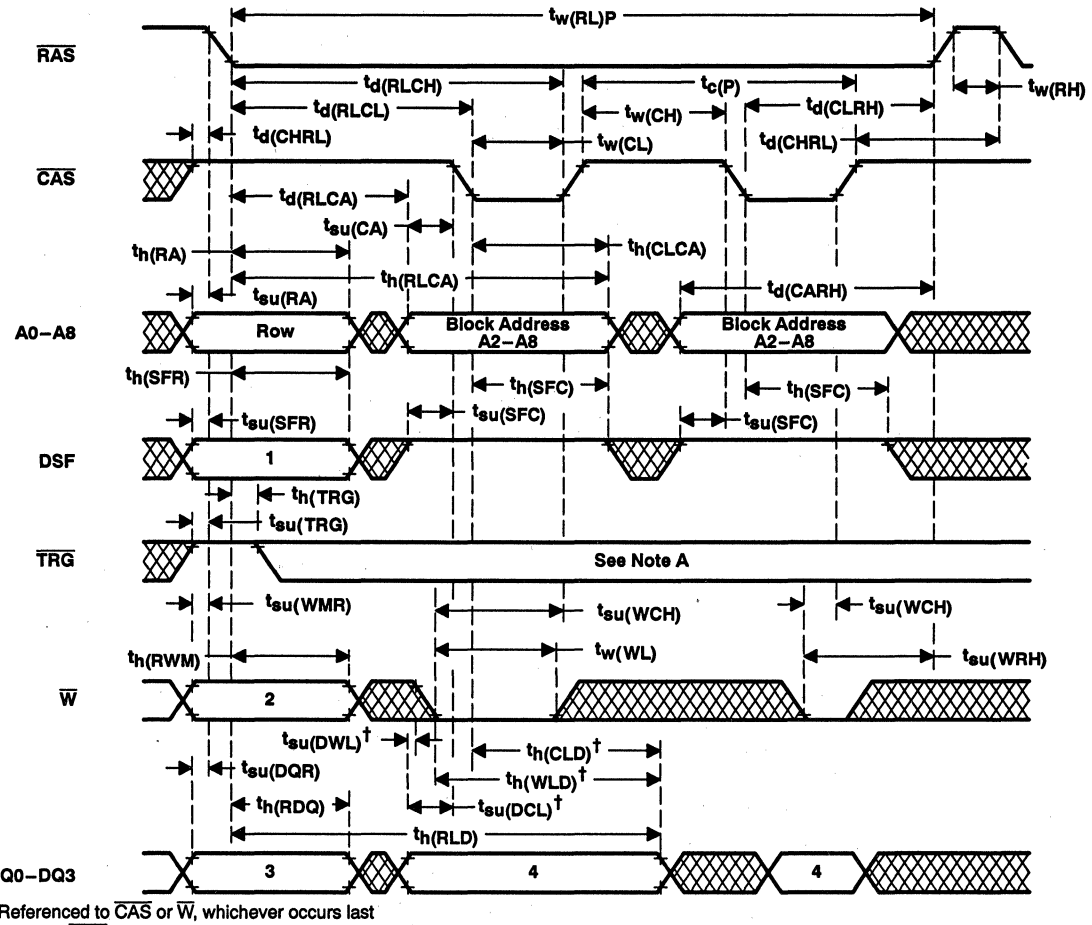
CYCLE	STATE			
	1	2	3	4
Write-mask load/use, block write	L	L	Write mask	Column mask
Use previous write mask, block write	H	L	Don't care	Column mask
Write mask disabled, block write to all I/Os	L	H	Don't care	Column mask

Write mask data 0: I/O write disable
1: I/O write enable

Column mask data DQn = 0 column write disable
(n = 0, 1, 2, 3) 1 column write enable

DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION



† Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last

NOTE A: $\overline{TRG}$ must remain high throughout the entire page-mode operation to assure page-mode cycle time if the late write feature is used. If the early-write-cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 24. Enhanced-Page-Mode Block-Write-Cycle Timing

Table 11. Enhanced-Page-Mode Block-Write-Cycle Table

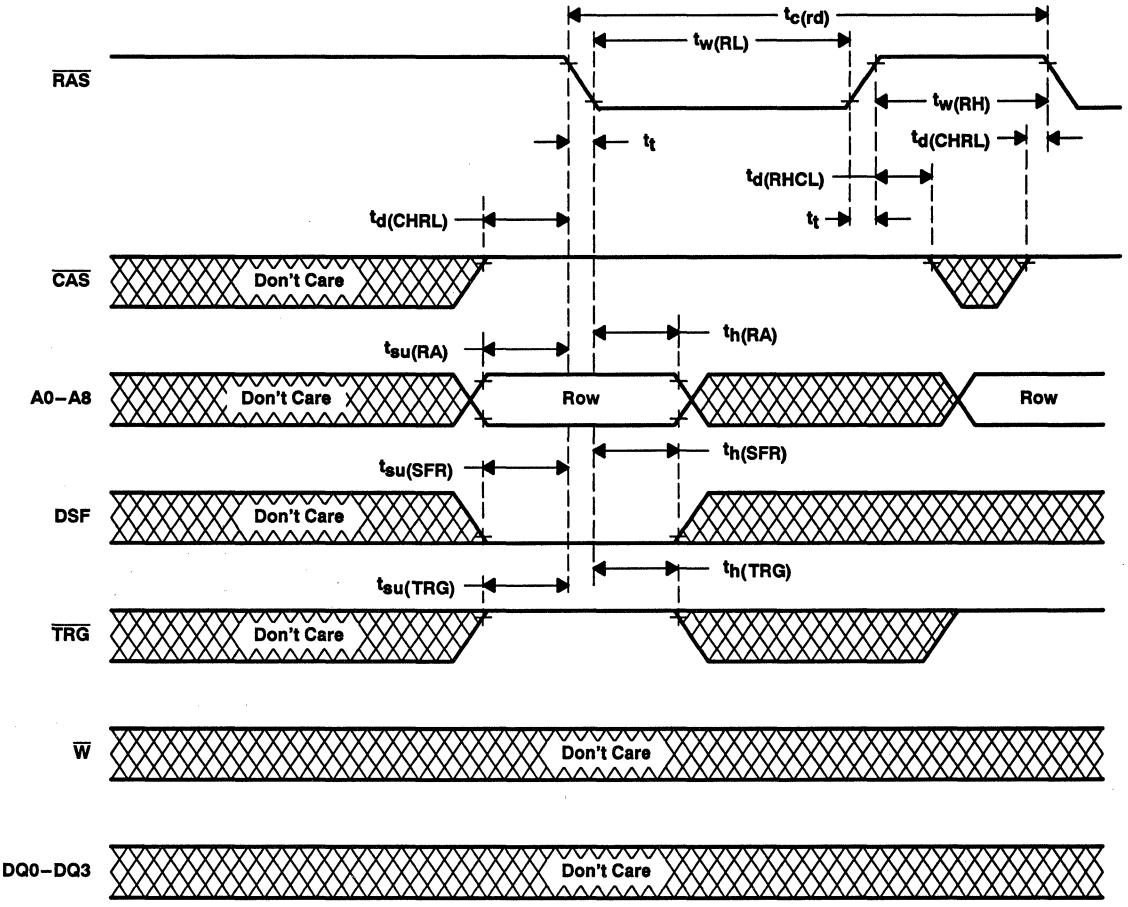
CYCLE	STATE			
	1	2	3	4
Write-mask load/use, block write	L	L	Write mask	Column mask
Use previous write mask, block write	H	L	Don't care	Column mask
Write mask disabled, block write to all I/Os	L	H	Don't care	Column mask

Write mask data 0: I/O write disable
1: I/O write enable

Column mask data DQn = (n = 0, 1, 2, 3) 0 column write disable
1 column write enable

DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

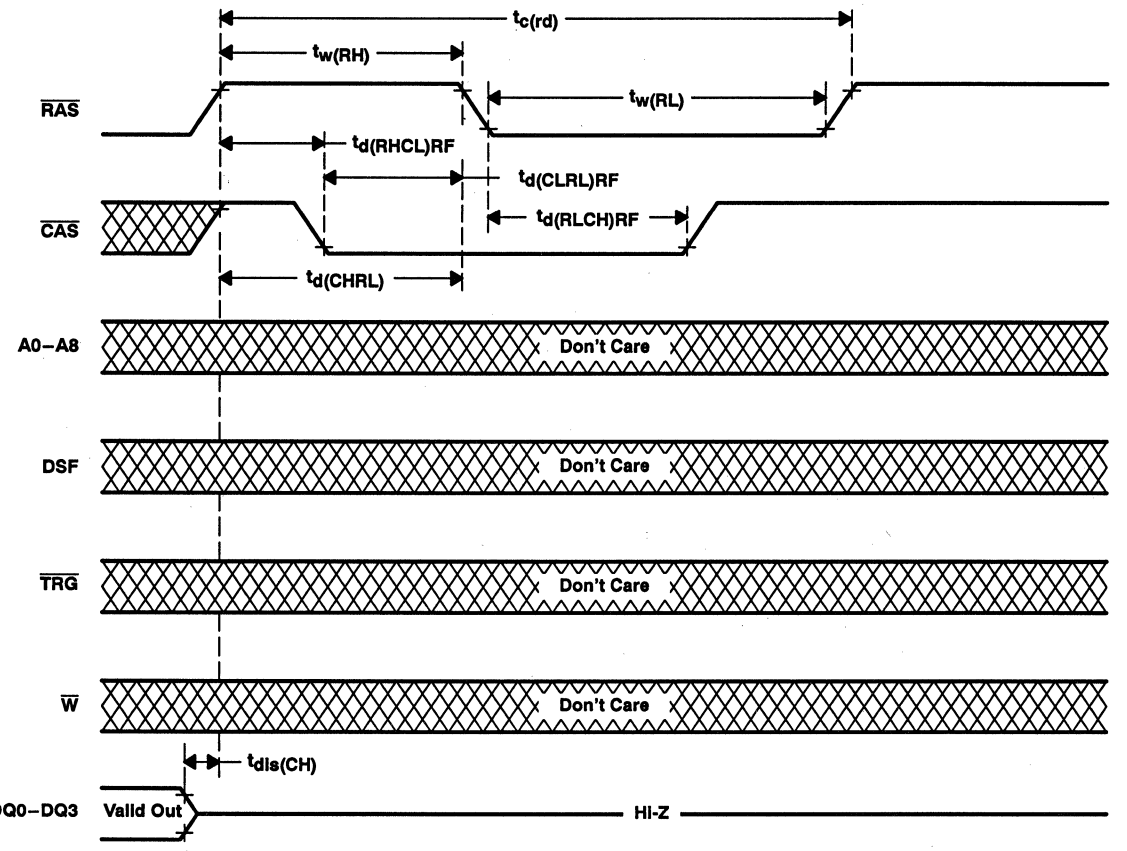
PARAMETER MEASUREMENT INFORMATION



NOTE A: In persistent write-per-bit function, $\overline{W}$ must be high at the falling edge of $\overline{RAS}$ during the refresh cycle.

Figure 25. $\overline{RAS}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: In persistent write-per-bit operation, $\overline{W}$ must be high at the falling edge of $\overline{RAS}$ during the refresh cycle.

Figure 26. CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

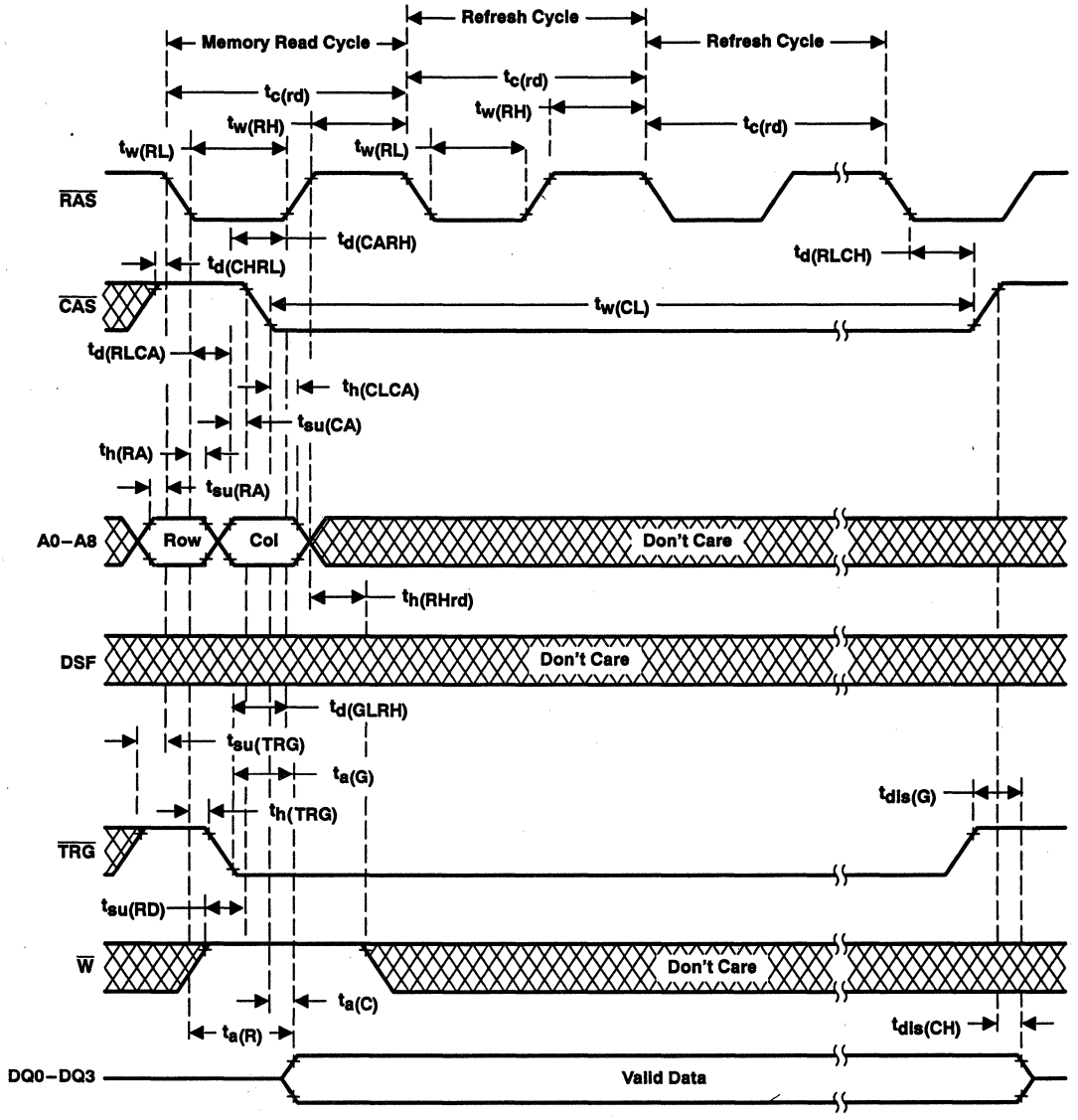
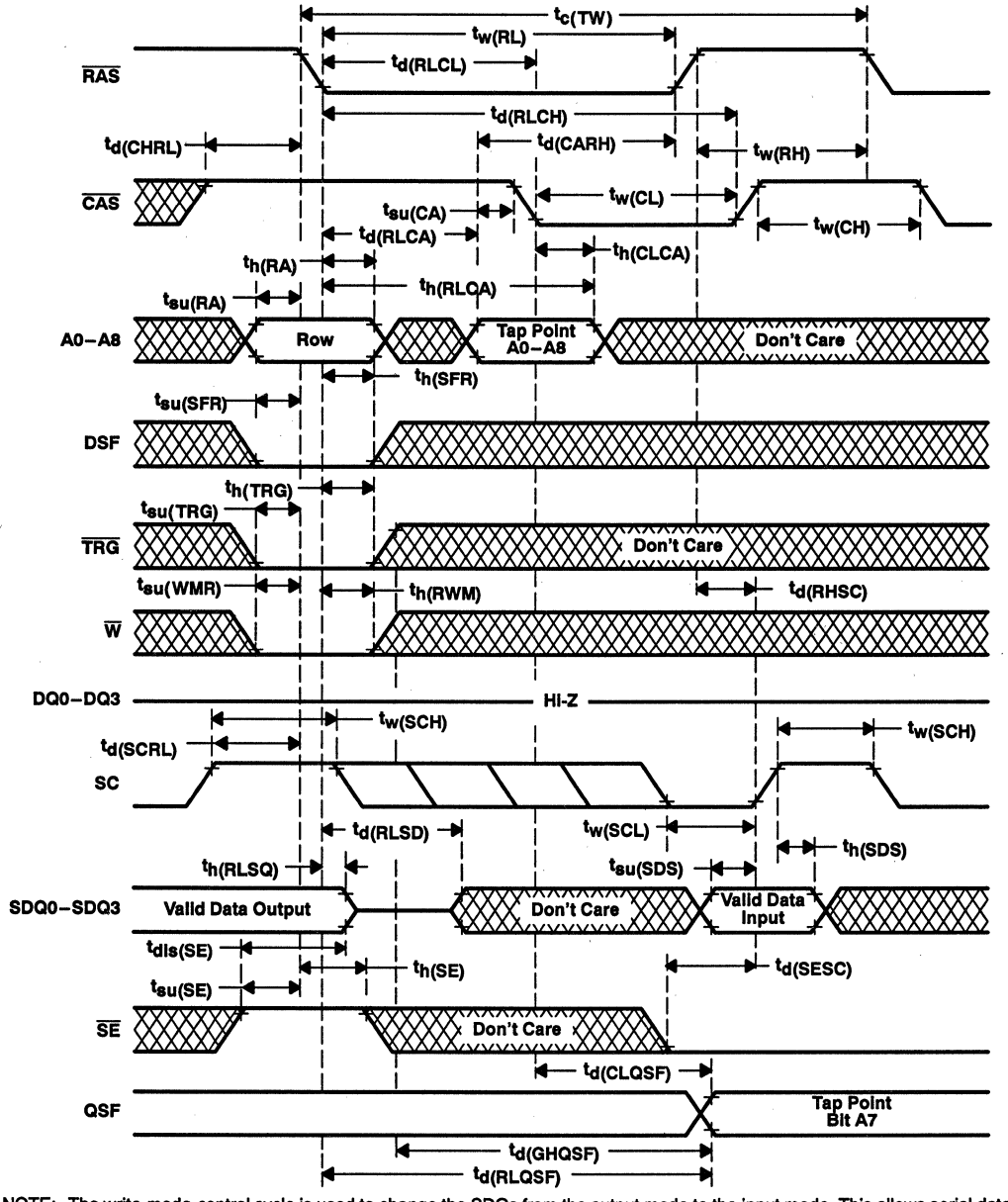


Figure 27. Hidden-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE: The write-mode-control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. This figure assumes that the device was originally in the serial-read mode.

Figure 28. Write-Mode-Control Pseudo-Transfer Timing

PARAMETER MEASUREMENT INFORMATION

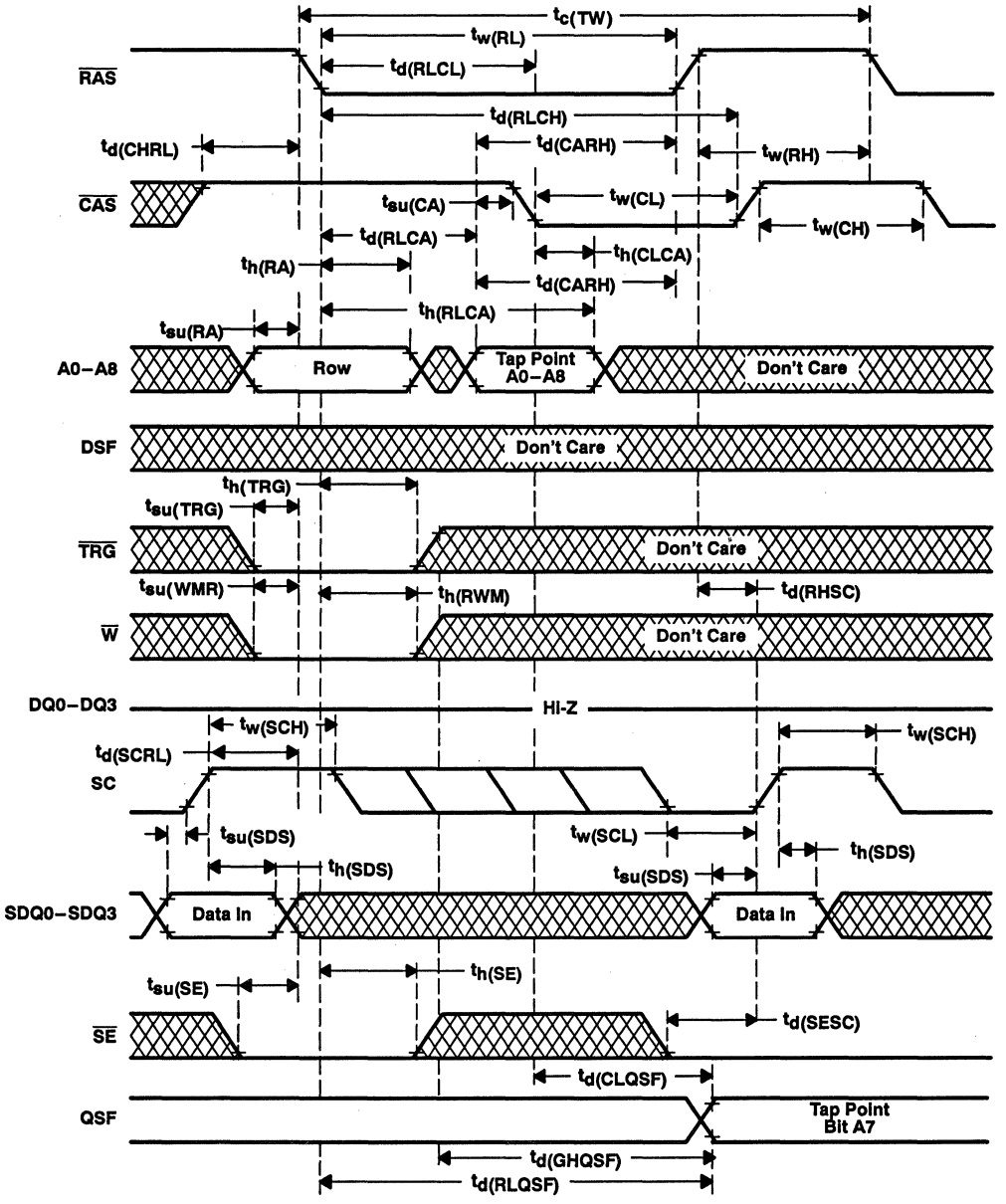


Figure 29. Data-Register-to-Memory Transfer Timing, Serial Input Enabled

PARAMETER MEASUREMENT INFORMATION

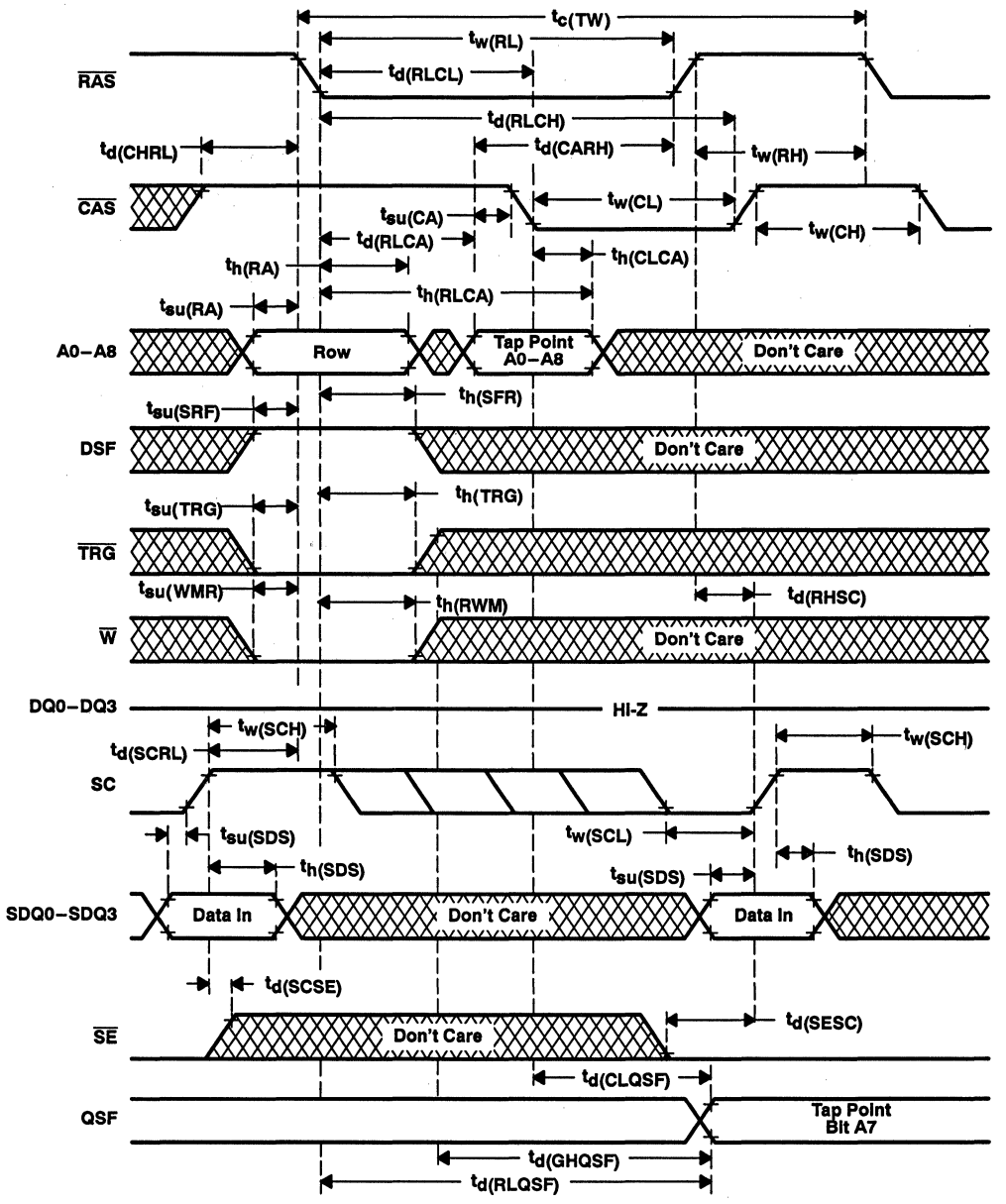
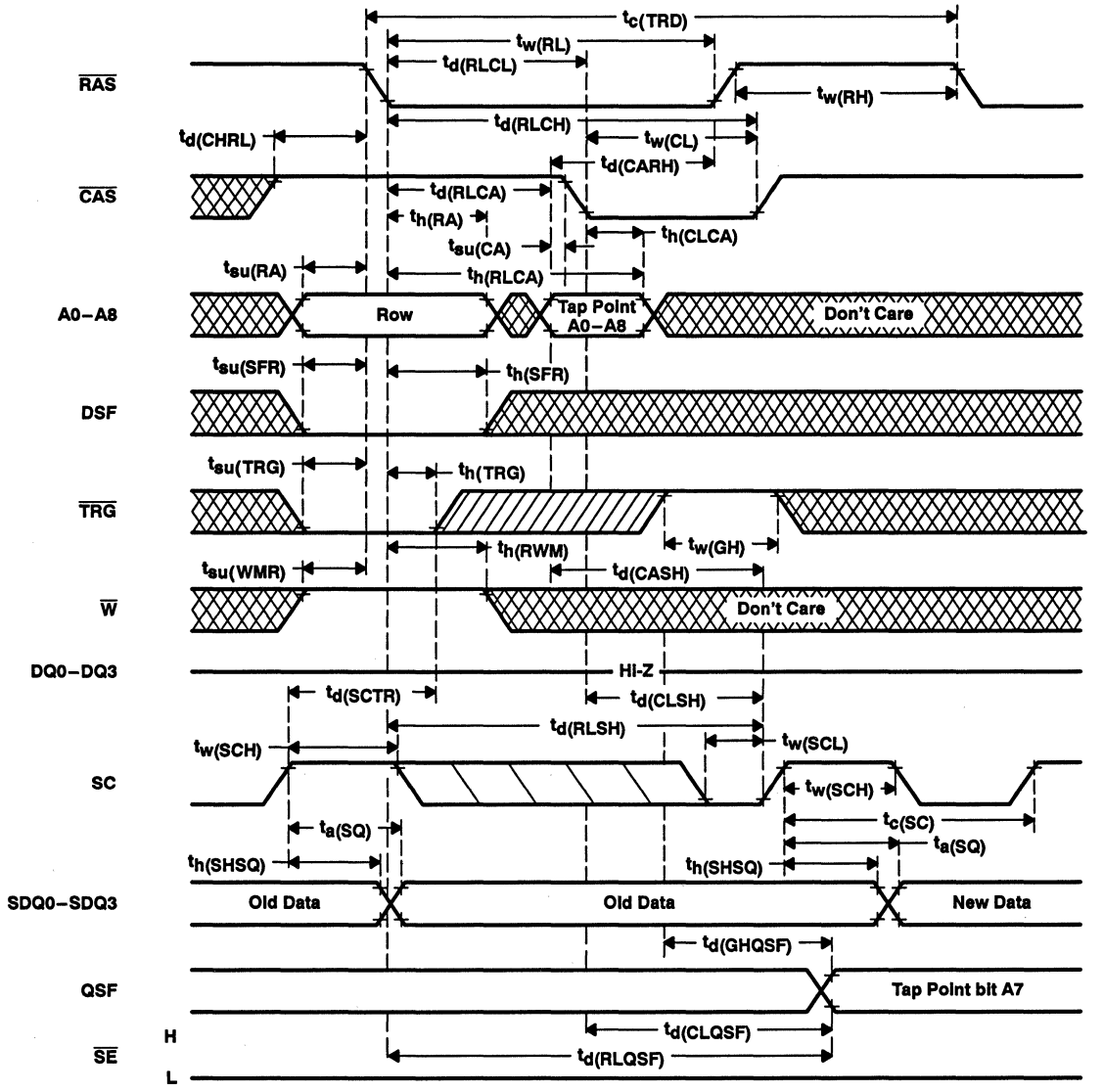


Figure 30. Alternate Data-Register-to-Memory Transfer-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



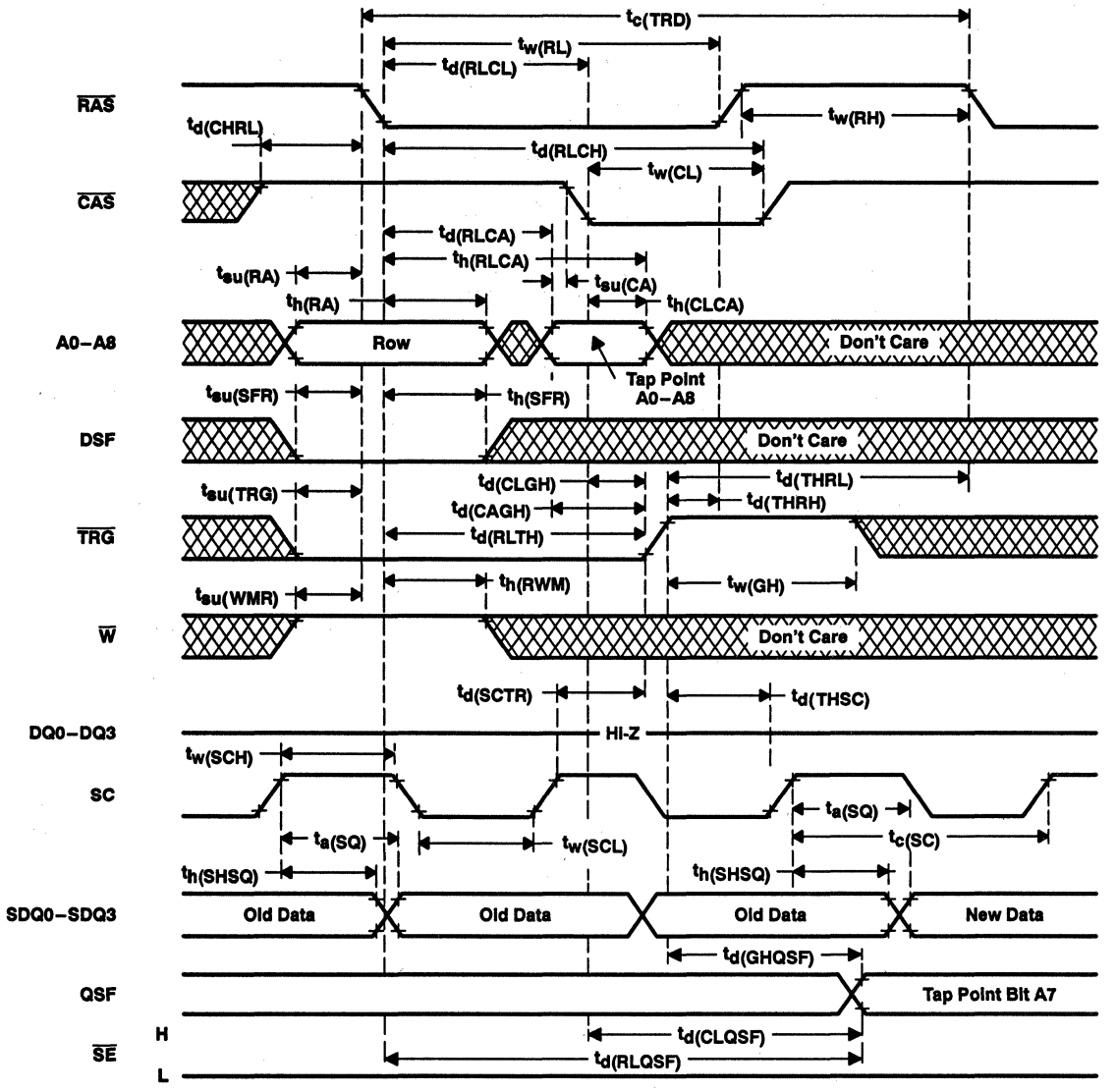
NOTES: A. Early-load operation is defined as $t_{h(TRG)}$ min < $t_{h(TRG)}$ < $t_{d(RLTH)}$ min.

B. DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written from the 512 corresponding columns of the selected row. The data that is transferred into the data registers can be either shifted out or transferred back into another row.

C. Once data is transferred into the data registers, the SAM is in the serial-read mode (i.e., SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

Figure 31. Memory-to-Data-Register Transfer-Cycle Timing, Early-Load Operation

PARAMETER MEASUREMENT INFORMATION



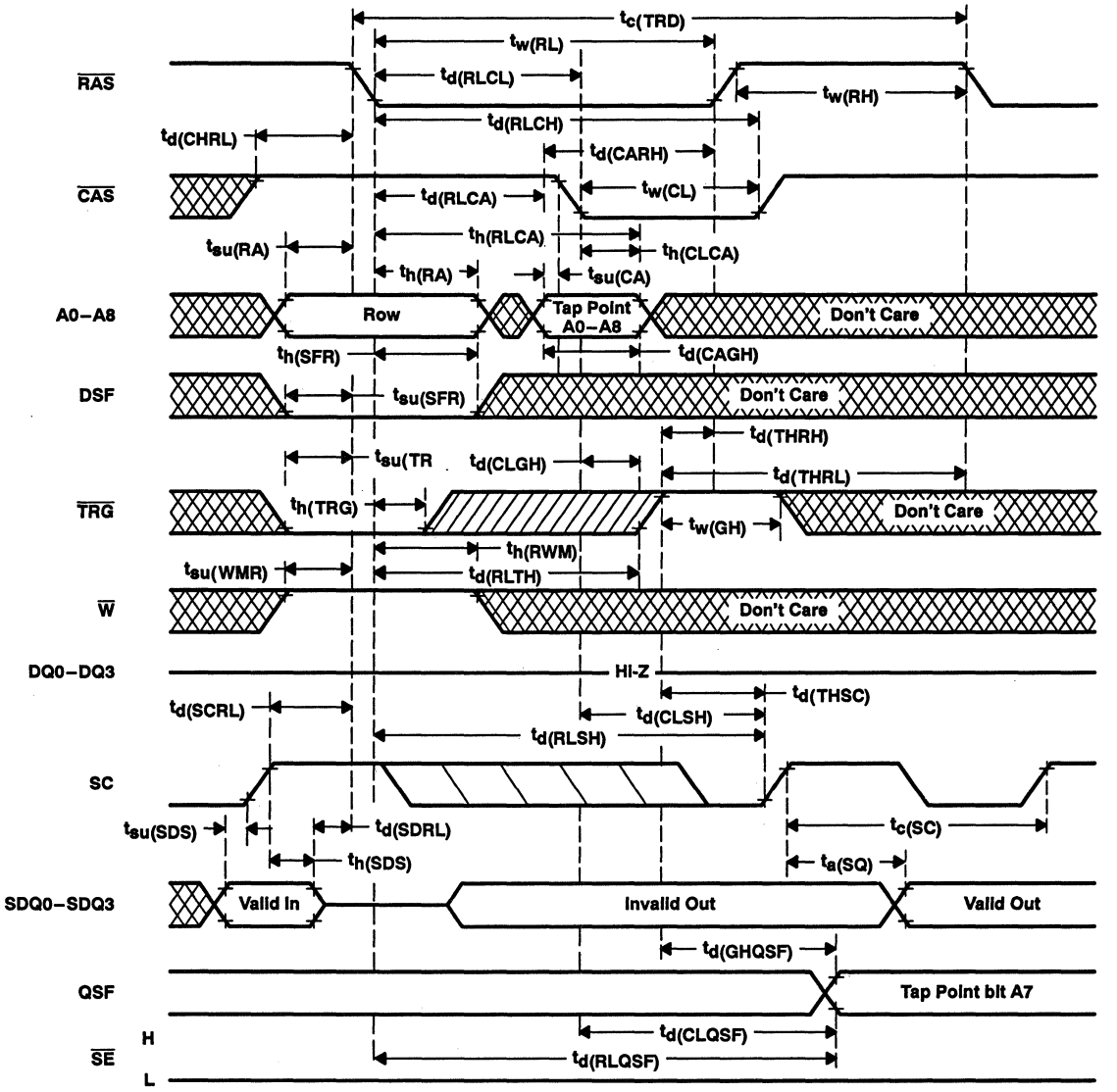
NOTES: A. Late-load operation is defined as $t_{d(THRH)} < 0$ ns.

B. DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written from the 512 corresponding columns of the selected row. The data that is transferred into the data registers can be either shifted out or transferred back into another row.

C. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

Figure 32. Memory-to-Data-Register Transfer-Cycle Timing, Real-Time-Reload Operation/Late-Load Operation

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Late-load operation is defined as $t_{d(THRH)} < 0$ ns.

B. DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

C. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

Figure 33. Memory-to-Data-Register Transfer-Cycle Timing, SDQ Ports Previously In Serial-Input Mode

PARAMETER MEASUREMENT INFORMATION

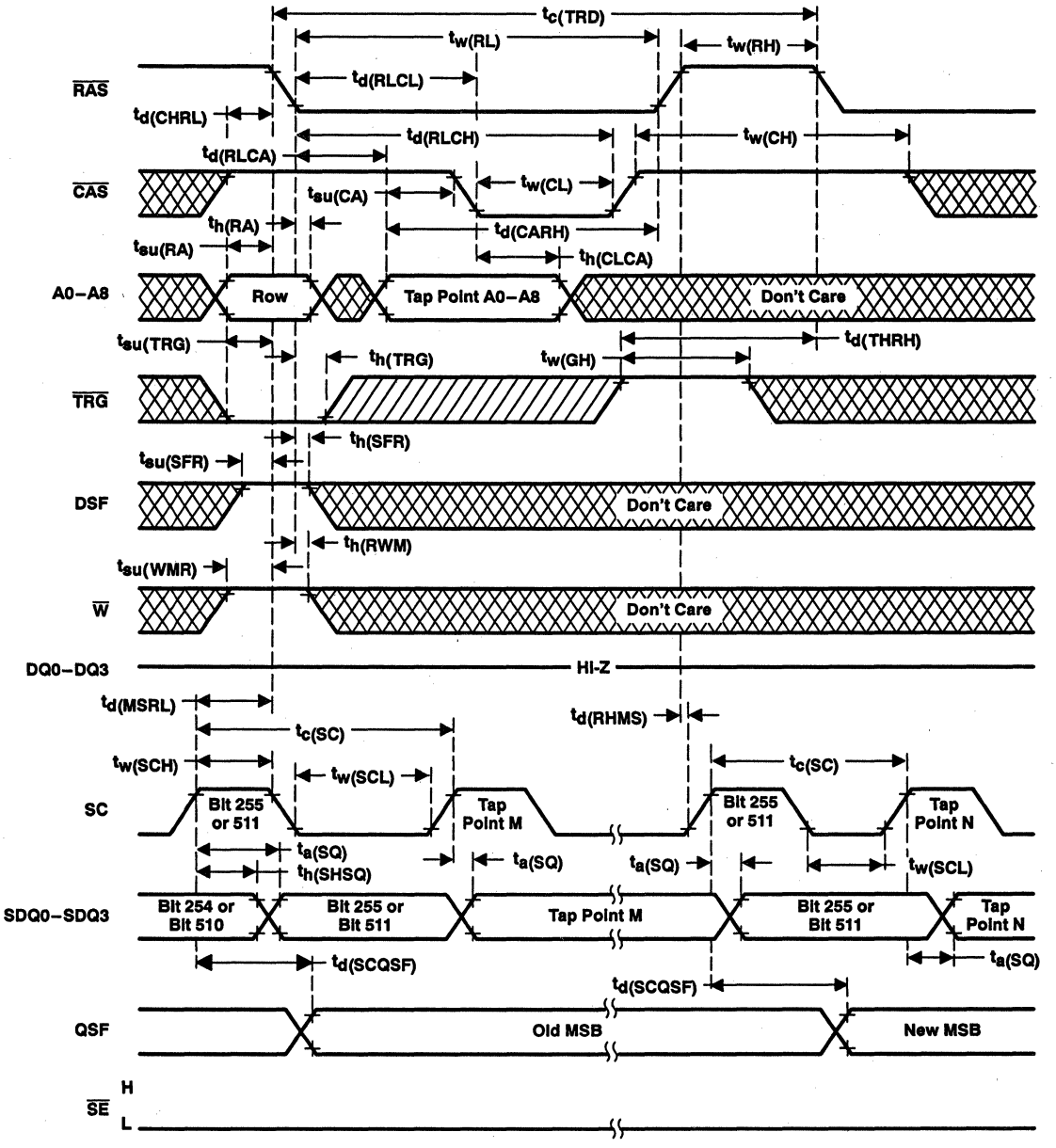
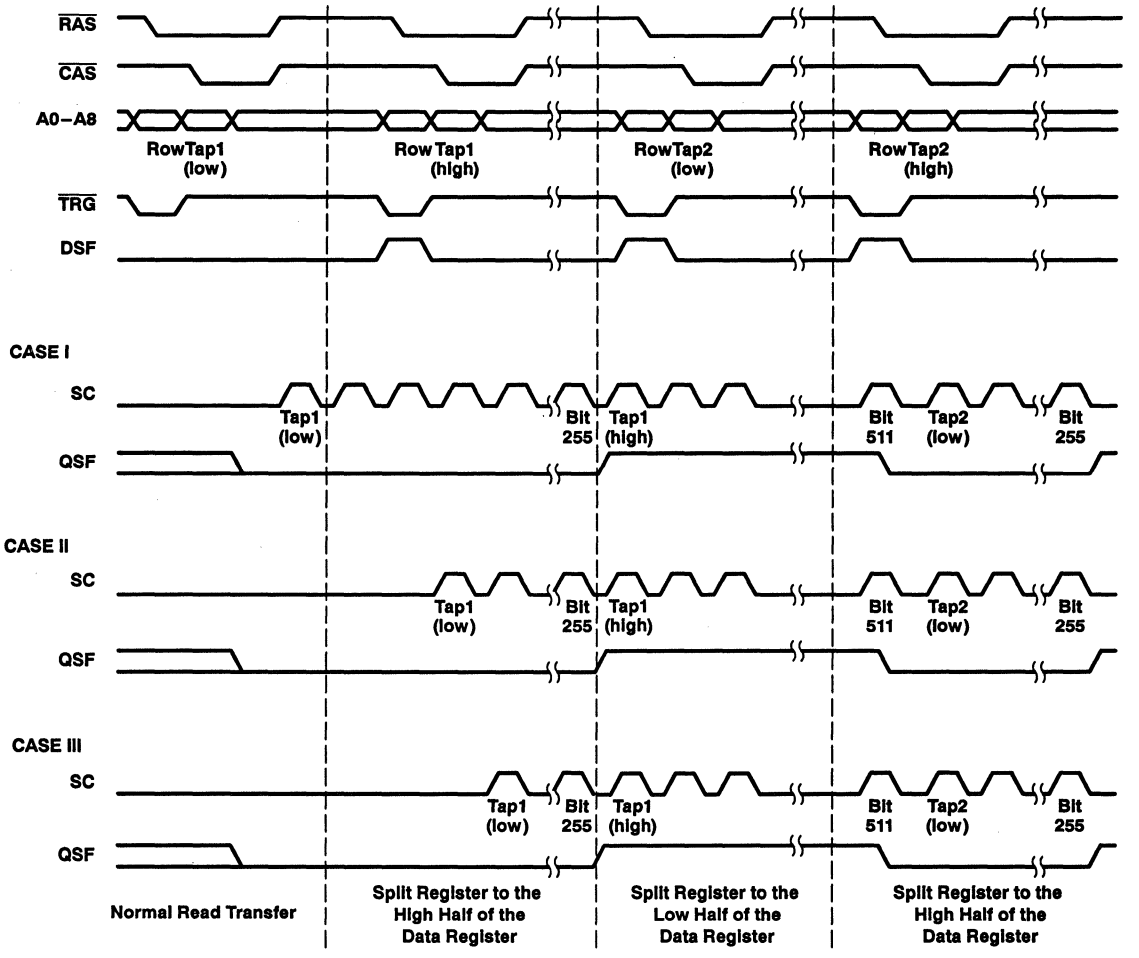


Figure 34. Split-Register-Mode Read-Transfer-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

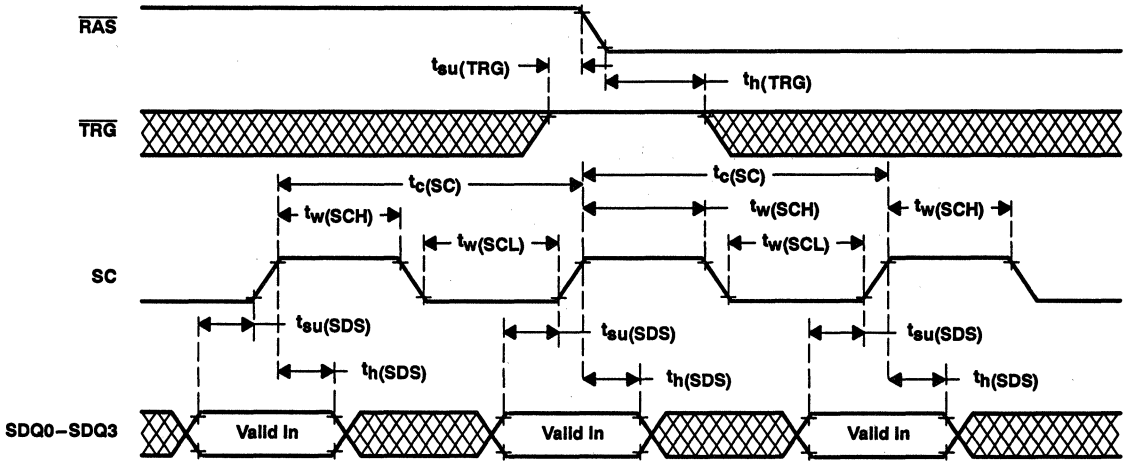


NOTES: A. In order to achieve proper split-register operation, a normal read transfer should be performed before the first split-register transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can then begin either after the normal read-transfer cycle (CASE I), during the first split-register cycle (CASE II), or even after the first split-register transfer cycle (CASE III). There is no minimum requirement of SC clock between the normal read-transfer cycle and the first split-register cycle.

B. A split register transfer into the inactive half is not allowed until $t_{d(MSRL)}$ is met. $t_{d(MSRL)}$ is the minimum delay time between the rising edge of the serial clock of the last bit (bit 255 or 511) and the falling edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half. After $t_{d(MSRL)}$ is met, the split-register transfer into the inactive half must also satisfy the $t_{d(RHMS)}$ requirement. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 255 or 511). There is a minimum requirement of one rising edge of SC clock between two split-register transfer cycles.

Figure 35. Split-Register-Transfer Operating Sequence

PARAMETER MEASUREMENT INFORMATION

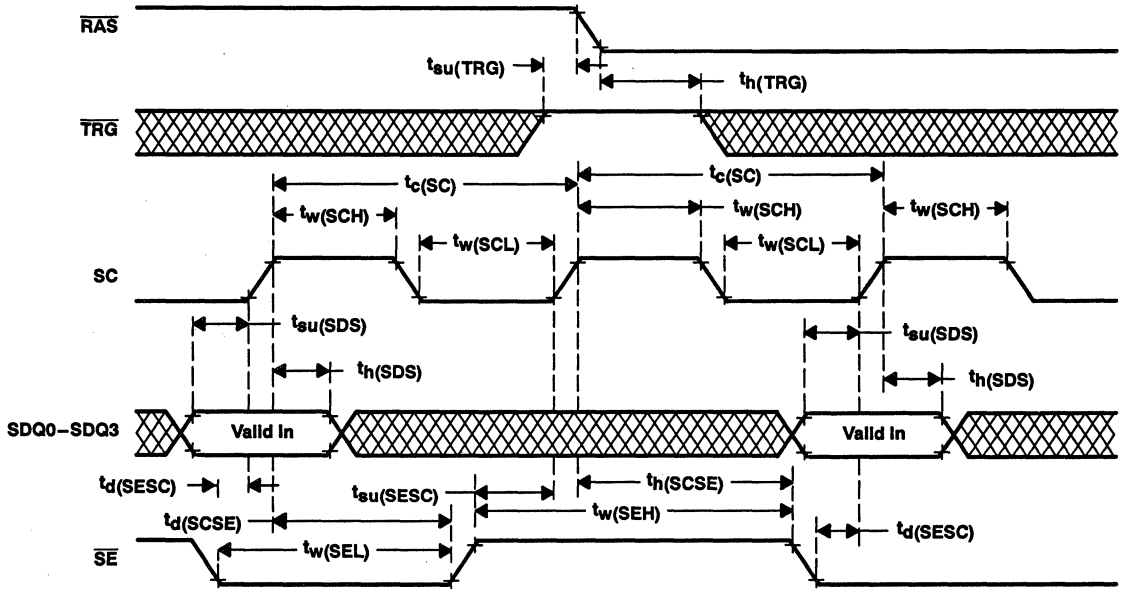


NOTES: A. The serial data-in cycle is used to input serial data into the data registers. Before data can be written into the data registers via the SDQ terminals, the device must be put into the write mode by performing a write-mode-control (pseudo-transfer) cycle or any other write-transfer cycle. A read-transfer cycle is the only cycle that takes the serial port (SAM) out of the write mode and puts it into the read mode, disabling the input data. Data is written starting at the location specified by the input address loaded on the previous transfer cycle.

B. While accessing data in the serial-data registers, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.

Figure 36. Serial-Write-Cycle Timing ($\overline{SE}$ = V_{IL})

PARAMETER MEASUREMENT INFORMATION

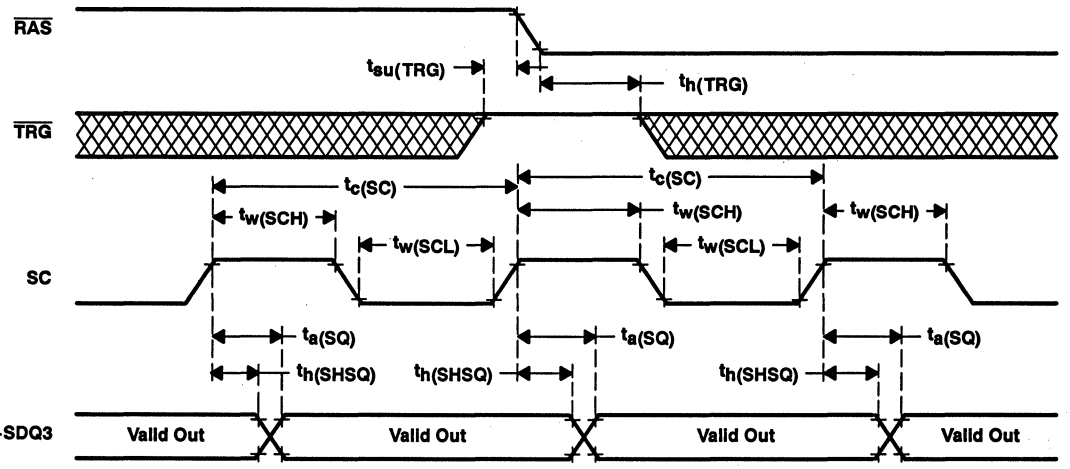


NOTES: A. The serial data-in cycle is used to input serial data into the data registers. Before data can be written into the data registers via the SDQ terminals, the device must be put into the write mode by performing a write-mode-control (pseudo-transfer) cycle or any other write-transfer cycle. A read-transfer cycle is the only cycle that takes the serial port (SAM) out of the write mode and puts it into the read mode, disabling the input data. Data is written starting at the location specified by the input address loaded on the previous transfer cycle.

B. While accessing data in the serial-data registers, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.

Figure 37. Serial-Write-Cycle Timing ($\overline{SE}$-Controlled Write)

PARAMETER MEASUREMENT INFORMATION

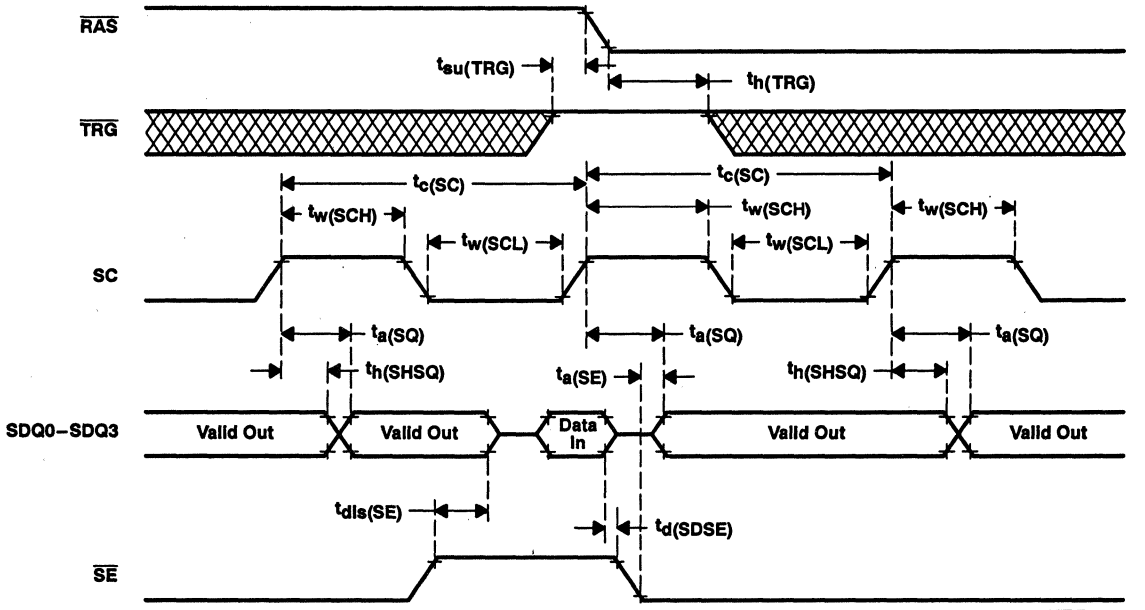


NOTES: A. While reading data through the serial-data register, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-to-memory-to-register data-transfer operation.

B. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SDQ, the device must be put into the read mode by performing a transfer-read cycle. Any transfer-write cycles occurring between the transfer-read cycle and the subsequent shifting out of data take the device out of the read mode and put it in the write mode, not allowing the reading of data.

Figure 38. Serial-Read-Cycle Timing ($\overline{SE}$ = V_{IL})

PARAMETER MEASUREMENT INFORMATION

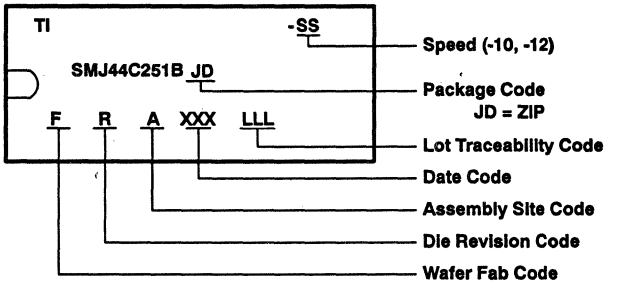


NOTES: A. While reading data through the serial-data register, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-to-memory-to-register data-transfer operation.

B. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SDQ, the device must be put into the read mode by performing a transfer-read cycle. Any transfer-write cycles occurring between the transfer-read cycle and the subsequent shifting out of data take the device out of the read mode and put it in the write mode, not allowing the reading of data.

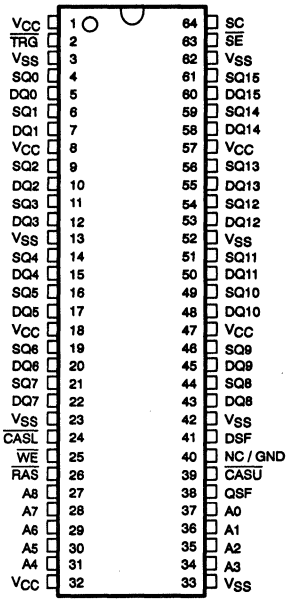
Figure 39. Serial-Read-Cycle Timing ($\overline{SE}$-Controlled Read)

device symbolization



- **Organization:**
  - **DRAM: 262 144 Words × 16 Bits**
  - **SAM: 256 Words × 16 Bits**
- **Dual-Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Data-Transfer Function From the DRAM to the Serial-Data Register**
- **(4 × 4) × 4 Block-Write Feature for Fast Area-Fill Operations; as Many as Four Memory-Address Locations Written Per Cycle From the 16-Bit On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O; Two Write-Per-Bit Modes to Simplify System Design**
- **Byte Write Control ($\overline{CASL}$, $\overline{CASU}$) Provides Flexibility**
- **Extended Data Output for Faster System Cycle Time**
- **Enhanced Page-Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) and Hidden-Refresh Modes**
- **Long Refresh Period**
  Every 8 ms (Max)
- **Up to 45-MHz Uninterrupted Serial-Data Streams**
- **256 Selectable Serial-Register Starting Locations**
- **$\overline{SE}$-Controlled Register-Status QSF**
- **Split-Register-Transfer Read for Simplified Real-Time Register Load**
- **Programmable Split-Register Stop Point**
- **3-State Serial Outputs Allow Easy Multiplexing of Video-Data Streams**
- **All Inputs/Outputs and Clocks TTL Compatible**
- **Compatible With JEDEC Standards**
- **Performance Ranges:**

HKC PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A8	Address Inputs
$\overline{CASL}$, $\overline{CASU}$	Column-Address Strobe/Byte Selects
DQ0–DQ15	DRAM Data I/O, Write Mask Data
DSF	Special-Function Select
NC/GND	No Connect/Ground (Important: Not connected internally to V_{SS})
QSF	Special-Function Output
$\overline{RAS}$	Row-Address Strobe
SC	Serial Clock
$\overline{SE}$	Serial Enable
SQ0–SQ15	Serial-Data Output
$\overline{TRG}$	Output Enable, Transfer Select
V_{CC}	5-V Supply (TYP)
V_{SS}	Ground
$\overline{WE}$	DRAM Write-Enable Select

- **Texas Instruments EPIC™ Process**
- **Designed to Work With the Texas Instruments Graphics Family**

	ACCESS TIME ROW ENABLE $t_{a(R)}$ (MAX)	ACCESS TIME SERIAL DATA $t_{a(SQ)}$ (MAX)	DRAM CYCLE TIME $t_{c(W)}$ (MIN)	DRAM PAGE MODE $t_{c(P)}$ (MIN)	SERIAL CYCLE TIME $t_{c(SC)}$ (MIN)	OPERATING CURRENT SERIAL PORT STANDBY I_{CC1} (MAX)	OPERATING CURRENT SERIAL PORT ACTIVE I_{CC1A} (MAX)
SMJ55161-70	70 ns	20 ns	130 ns	45 ns	22 ns	165 mA	210 mA
SMJ55161-80	80 ns	25 ns	150 ns	50 ns	30 ns	160 mA	195 mA

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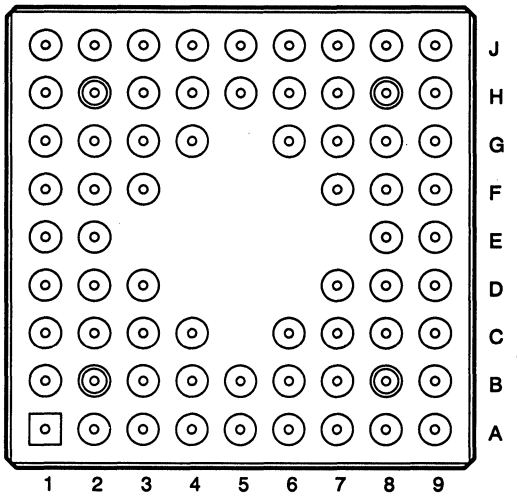
GB PACKAGE
(BOTTOM VIEW)



GB Package Pin Assignments – By Location

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
J1	DQ1	J2	SQ3	J3	DQ3	J4	DQ4	J5	DQ5	J6	DQ6	J7	SQ7	J8	$\overline{CASL}$	J9	A8
H1	DQ0	H2	SQ2	H3	DQ2	H4	SQ4	H5	SQ5	H6	SQ6	H7	DQ7	H8	$\overline{WE}$	H9	A7
G1	SQ0	G2	SQ1	G3	V_{DD2}	G4	V_{SS2}			G6	V_{DD2}	G7	V_{SS2}	G8	$\overline{RAS}$	G9	A6
F1	$\overline{TRG}$	F2	V_{SS1}	F3	V_{DD1}							F7	V_{DD1}	F8	V_{DD1}	F9	A5
E1	SC	E2	V_{DD1}											E8	V_{SS1}	E9	A4
D1	$\overline{SE}$	D2	V_{SS1}	D3	V_{DD1}							D7	V_{SS1}	D8	A3	D9	A2
C1	SQ15	C2	V_{SS1}	C3	V_{DD2}	C4	V_{SS2}			C6	V_{DD2}	C7	V_{SS2}	C8	$\overline{CASU}$	C9	A1
B1	DQ15	B2	DQ14	B3	DQ13	B4	DQ12	B5	DQ11	B6	DQ10	B7	SQ8	B8	DSF	B9	A0
A1	SQ14	A2	SQ13	A3	SQ12	A4	SQ11	A5	SQ10	A6	SQ9	A7	DQ9	A8	DQ8	A9	QSF

GB Package Pin Assignments – By Signal

PIN NAME	NO.	PIN NAME	NO.	PIN NAME	NO.	PIN NAME	NO.	PIN NAME	NO.	PIN NAME	NO.
A0	B9	DQ1	J1	DQ12	B4	SQ2	H2	SQ13	A2	V_{DD2}	G6
A1	C9	DQ2	H3	DQ13	B3	SQ3	J2	SQ14	A1	V_{DD2}	C6
A2	D9	DQ3	J3	DQ14	B2	SQ4	H4	SQ15	C1	V_{SS1}	F2
A3	D8	DQ4	J4	DQ15	B1	SQ5	H5	$\overline{TRG}$	F1	V_{SS1}	D2
A4	E9	DQ5	J5	DSF	B8	SQ6	H6	V_{DD1}	E2	V_{SS1}	C2
A5	F9	DQ6	J6	QSF	A9	SQ7	J7	V_{DD1}	F3	V_{SS1}	D7
A6	G9	DQ7	H7	$\overline{RAS}$	G8	SQ8	B7	V_{DD1}	D3	V_{SS1}	E8
A7	H9	DQ8	A8	SC	E1	SQ9	A6	V_{DD1}	F7	V_{SS2}	G4
A8	J9	DQ9	A7	$\overline{SE}$	D1	SQ10	A5	V_{DD1}	F8	V_{SS2}	C4
$\overline{CASL}$	J8	DQ10	B6	SQ0	G1	SQ11	A4	V_{DD2}	G3	V_{SS2}	G7
$\overline{CASU}$	C8	DQ11	B5	SQ1	G2	SQ12	A3	V_{DD2}	C3	V_{SS2}	C7
DQ0	H1									$\overline{WE}$	H8

description

The SMJ55161 multiport video RAM is a high-speed, dual-port memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 16 bits each interfaced to a serial-data register (serial-access memory (SAM)) organized as 256 words of 16 bits each. The SMJ55161 supports three basic types of operation: random access to and from the DRAM, serial access from the serial register, and transfer of data from any row in the DRAM to the serial register. Except during transfer operations, the SMJ55161 can be accessed simultaneously and asynchronously from the DRAM and SAM ports.

The SMJ55161 is equipped with several features designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates are achieved by the device's (4 × 4) × 4 block-write feature. The block-write mode allows 16 bits of data (present in an on-chip color-data register) to be written to any combination of four adjacent column-address locations. As many as 64 bits of data can be written to memory during each $\overline{\text{CAS}}$ cycle time. Also on the DRAM port, a write mask or a write-per-bit feature allows masking of any combination of the 16 inputs/outputs on any write cycle. The persistent write-per-bit feature uses a mask register that, once loaded, can be used on subsequent write cycles without reloading. The SMJ55161 also offers byte control. Byte control can be applied in read cycles, write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. The SMJ55161 also offers extended-data output mode. The extended-data output mode is effective in both the page-mode and standard DRAM cycles.

The SMJ55161 offers a split-register-transfer read (DRAM-to-SAM) feature for the serial register (SAM port). This feature enables real-time register load implementation for continuous serial-data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. For applications not requiring real-time register load (for example, loads done during CRT-retrace periods), the full-register mode of operation is retained to simplify system design.

The SAM port is designed for maximum performance. Data can be accessed from the SAM at serial rates up to 45 MHz. During the split-register-transfer read operations, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, QSF, is included to indicate which half of the serial register is active.

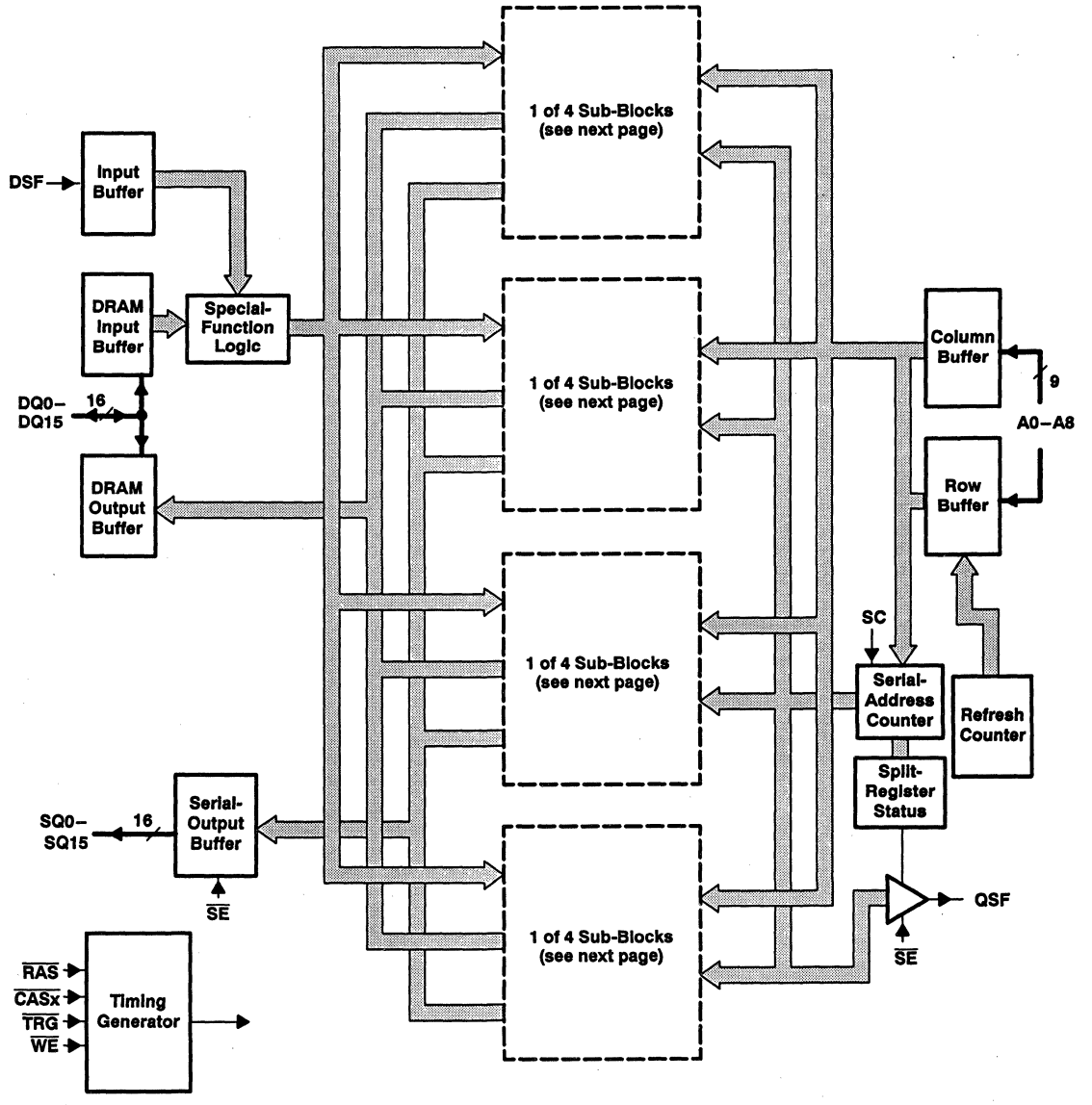
All inputs, outputs, and clock signals on the SMJ55161 are compatible with Series 74 TTL. All address lines and data-in lines are latched on-chip to simplify system design. All data-out lines are unlatched to allow greater system flexibility.

The SMJ55161 employs state-of-the-art Texas Instruments (TI) enhanced performance implanted CMOS (EPIC™) scaled-CMOS, double-level polysilicon/polycide gate technology combining very high performance with improved reliability.

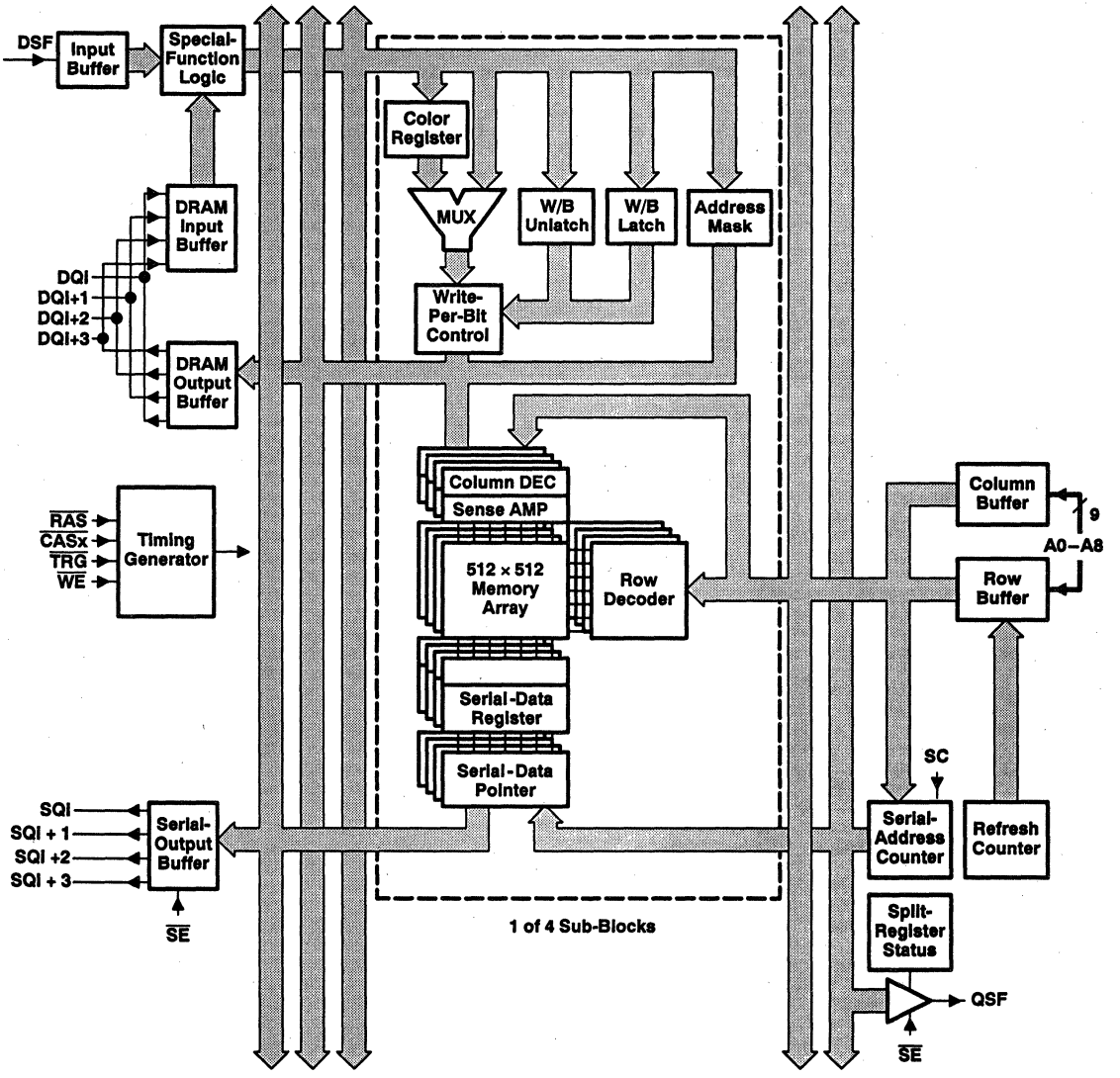
The SMJ55161 is offered in a 68-pin ceramic pin-grid-array package (GB suffix) and a 64-pin ceramic flatpack (HKC suffix).

The SMJ55161 and other TI multiport video RAMs are supported by a broad line of graphic processors and control devices from TI. Refer to Tables 1 and 2 for additional function and description information.

functional block diagram



functional block diagram (continued)



Function Table

FUNCTION	RAS FALL				CASx FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CASx‡	TRG	WE	DSF	DSF	RAS	CASx§	RAS	CASL CASU WE	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop-point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)★	L	X	H	H	X	X	X	X	X	CBRN
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
Load write-mask register□	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled
X = Don't care

† DQ0–DQ15 are latched on either the first falling edge of CASx or the falling edge of WE, whichever occurs later.
‡ Logic L is selected when either or both CASL and CASU are low.
§ The column address and block address are latched on the first falling edge of CASx.
¶ CBRS cycle should be performed immediately after the powerup initialization cycle.
# A0–A3, A8: don't care; A4–A7: stop-point code
‖ CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
★ CBR refresh (no reset) mode does not end persistent write-per-bit mode or stop-point mode.
□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.

Table 1. Pin Description Versus Operational Mode

PIN	DRAM	TRANSFER	SAM
A0 – A8	Row, column address	Row address, tap point	
$\overline{CASL}$ $\overline{CASU}$	Column-address strobe, DQ output enable	Tap-address strobe	
DQ	DRAM data I/O, write mask		
DSF	Block-write enable Write-mask-register load enable Color-register load enable CBR (option reset)	Split-register-transfer enable	
$\overline{RAS}$	Row-address strobe	Row-address strobe	
$\overline{SE}$			SQ output enable, QSF output enable
SC			Serial clock
SQ			Serial-data output
$\overline{TRG}$	DQ output enable	Transfer enable	
$\overline{WE}$	Write enable, write-per-bit enable		
QSF			Serial-register status
NC/GND	Either make no external connection or tie to system GND (V_{SS})		
V_{CC}†	5-V supply		
V_{SS}†	Ground		

† For proper device operation, all V_{CC} pins must be connected to a 5-V supply, and all V_{SS} pins must be tied to ground.

pin definitions

address (A0–A8)

Eighteen address bits are required to decode one of 262 144 storage cell locations. Nine row-address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Nine column-address bits are set up on pins A0–A8 and latched onto the chip on the first falling edge of $\overline{CASx}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and the first falling edge of $\overline{CASx}$.

During the full-register-transfer read operation, the states of A0–A8 are latched on the falling edge of $\overline{RAS}$ to select one of the 512 rows where the transfer occurs. At the first falling edge of $\overline{CASx}$, the column-address bits A0–A8 are latched. The most significant column-address bit (A8) selects which half of the row is transferred to the SAM. The appropriate 8-bit column address (A0–A7) selects one of 256 tap points (starting positions) for the serial-data output.

During the split-register-transfer read operation, address bit A7 is ignored at the falling edge of $\overline{CASx}$. An internal counter selects which half of the register is used. If the high half of the SAM is currently in use, the low half of the SAM is loaded with the low half of the DRAM half row and vice versa. Column address (A8) selects the DRAM half row. The remaining seven address bits (A0–A6) are used to select one of 127 possible starting locations within the SAM. Locations 127 and 255 are not valid tap points.

row-address strobe ($\overline{RAS}$)

$\overline{RAS}$ is similar to a chip enable so that all DRAM cycles and transfer cycles are initiated by the falling edge of $\overline{RAS}$. $\overline{RAS}$ is a control input that latches the states of the row address, $\overline{WE}$, $\overline{TRG}$, $\overline{CASL}$, $\overline{CASU}$, and DSF onto the chip to invoke DRAM and transfer-read functions of the SMJ55161.

column-address strobe ($\overline{CASL}$, $\overline{CASU}$)

$\overline{CASL}$ and $\overline{CASU}$ are control inputs that latch the states of the column address and DSF to control DRAM and transfer functions of the SMJ55161. $\overline{CASx}$ also act as output enables for the DRAM output pins DQ0–DQ15. In DRAM operation, $\overline{CASL}$ enables data to be written to or read from the lower byte (DQ0–DQ7), and $\overline{CASU}$ enables data to be written to or from the upper byte (DQ8–DQ15). In transfer operations, address bits A0–A8 are latched at the first falling edge of $\overline{CASx}$ as the start position (tap) for the serial-data output (SQ0–SQ15).

output enable/transfer select ($\overline{TRG}$)

$\overline{TRG}$ selects either DRAM or transfer operation as $\overline{RAS}$ falls. For DRAM operation, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. During DRAM operation, $\overline{TRG}$ functions as an output enable for the DRAM output pins DQ0–DQ15. For transfer operation, $\overline{TRG}$ must be brought low before $\overline{RAS}$ falls.

write-mask select, write enable ($\overline{WE}$)

In DRAM operation, $\overline{WE}$ enables data to be written to the DRAM. $\overline{WE}$ is also used to select the DRAM write-per-bit mode. Holding $\overline{WE}$ low on the falling edge of $\overline{RAS}$ invokes the write-per-bit operation. The SMJ55161 supports both the nonpersistent write-per-bit mode and the persistent write-per-bit mode.

special-function select (DSF)

The DSF input is latched on the falling edge of $\overline{RAS}$ or the first falling edge of $\overline{CASx}$, similar to an address. DSF determines which of the following functions are invoked on a particular cycle:

- CBR refresh with reset (CBR)
- CBR refresh with no reset (CBRN)
- CBR refresh with no reset and stop-point set (CBRS)
- Block write
- Loading write-mask register for the persistent write-per-bit mode (LMR)
- Loading color register for the block-write mode
- Split-register-transfer read

DRAM data I/O, write mask data (DQ0–DQ15)

DRAM data is written or read through the common I/O DQ pins. The 3-state DQ-output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 54 TTL load. Data out is the same polarity as data in. During a normal access cycle, the outputs remain in the high-impedance state until $\overline{TRG}$ is brought low. Data appears at the outputs until $\overline{TRG}$ returns high, $\overline{CASx}$ returns high following $\overline{RAS}$ returning high, or $\overline{RAS}$ returns high following $\overline{CASx}$ returning high. The write mask is latched into the device via the random DQ pins by the falling edge of $\overline{RAS}$ and is used on all write-per-bit cycles. In a transfer operation, the DQ outputs remain in the high-impedance state for the entire cycle.

serial-data outputs (SQ0–SQ15)

Serial data is read from the SQ pins. The SQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 54 TTL load. The serial outputs are in the high-impedance (floating) state as long as the serial-enable pin, $\overline{SE}$, is high. The serial outputs are enabled when $\overline{SE}$ is brought low.

serial clock (SC)

Serial data is accessed out of the data register from the rising edge of SC. The SMJ55161 is designed to work with a wide range of clock duty cycles to simplify system design. There is no refresh requirement because the data registers that comprise the SAM are static. There is also no minimum SC-clock operating frequency.

serial enable ($\overline{SE}$)

During serial-access operations, $\overline{SE}$ is used as an enable/disable for the SQ outputs. $\overline{SE}$ low enables the serial-data output. $\overline{SE}$ high disables the serial-data output. $\overline{SE}$ is also used as an enable/disable for output pin QSF.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is not disabled. External SC pulses increment the internal serial-address counter regardless of the state of $\overline{SE}$. This ungated serial-clock scheme minimizes access time of serial output from $\overline{SE}$ low because the serial-clock input buffer and the serial-address counter are not disabled by $\overline{SE}$.

special-function output (QSF)

QSF is an output pin that indicates which half of the SAM is being accessed. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of the serial register (SAM). When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM.

During full-register-transfer operations, QSF can change state upon completing the cycle. This state is determined by the tap point loaded during the transfer cycle. QSF is enabled by $\overline{SE}$. If $\overline{SE}$ is high, the QSF output is in the high-impedance state.

no connect / ground (NC/GND)

NC/GND should be tied to system ground or left floating for proper device operation.

functional operation description

random access operation

DRAM Function Table

FUNCTION	RAS FALL				CASx FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CASx‡	TRG	WE	DSF	DSF	RAS	CASx§	RAS	CASL CASU WE	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop-point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)*	L	X	H	H	X	X	X	X	X	CBRN
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
Load write-mask register □	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled
X = Don't care

† DQ0–DQ15 are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.
‡ Logic L is selected when either or both $\overline{CASL}$ and $\overline{CASU}$ are low.
§ The column address and block address are latched on the first falling edge of $\overline{CASx}$.
¶ CBRS cycle should be performed immediately after the power-up initialization cycle.
# A0–A3, A8: don't care; A4–A7: stop-point code
‖ CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
* CBR refresh (no reset) mode does not end persistent write-per-bit mode or stop-point mode.
□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. This mode eliminates the time required for row-address setup, row-address hold, and address multiplex. The maximum $\overline{RAS}$ low time and $\overline{CAS}$ page cycle time used determines the number of columns that can be accessed.

Unlike conventional page-mode operations, the enhanced page mode allows the SMJ55161 to operate at a higher data bandwidth. Data retrieval begins as soon as the column address is valid rather than when $\overline{CASx}$ transitions low. A valid column address can be presented immediately after the row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CASx}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CASx}$ low) if $t_{a(CA)}$ max (access time from column address) has been satisfied.

refresh

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refreshes are accomplished by bringing either or both $\overline{CASL}$ and $\overline{CASU}$ low earlier than $\overline{RAS}$. The external row address is ignored, and the refresh row address is generated internally. Three types of CBR refresh cycles are available. The CBR refresh (option reset) ends the persistent write-per-bit mode and the stop-point mode. The CBRN and CBRS refreshes (no reset) do not end the persistent write-per-bit mode or the stop-point mode. The 512 rows of the DRAM do not necessarily need to be refreshed consecutively as long as the entire refresh is completed within the required time period, $t_{rf(MA)}$. The output buffers remain in the high-impedance state during the CBR refresh cycles regardless of the state of $\overline{TRG}$.

hidden refresh

A hidden refresh is accomplished by holding both $\overline{CASL}$ and $\overline{CASU}$ low in the DRAM read cycle and cycling $\overline{RAS}$. The output data of the DRAM read cycle remains valid while the refresh is carried out. Like the CBR refresh, the refreshed row addresses are generated internally during the hidden refresh.

$\overline{RAS}$-only refresh

A $\overline{RAS}$-only refresh is accomplished by cycling $\overline{RAS}$ at every row address. Unless $\overline{CASx}$ and $\overline{TRG}$ are low, the output buffers remain in the high-impedance state to conserve power. Externally-generated addresses must be supplied during $\overline{RAS}$-only refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed.

extended data output

The SMJ55161 features extended data output during DRAM accesses. While $\overline{RAS}$ and $\overline{TRG}$ are low, the DRAM output remains valid. The output remains valid even when $\overline{CASx}$ returns high until $\overline{WE}$ is low, $\overline{TRG}$ is high, or both $\overline{CASx}$ and $\overline{RAS}$ are high (see Figures 1 and 2). The extended-data-output mode functions in all read cycles including DRAM read, page-mode read, and read-modify-write cycles (see Figure 3).

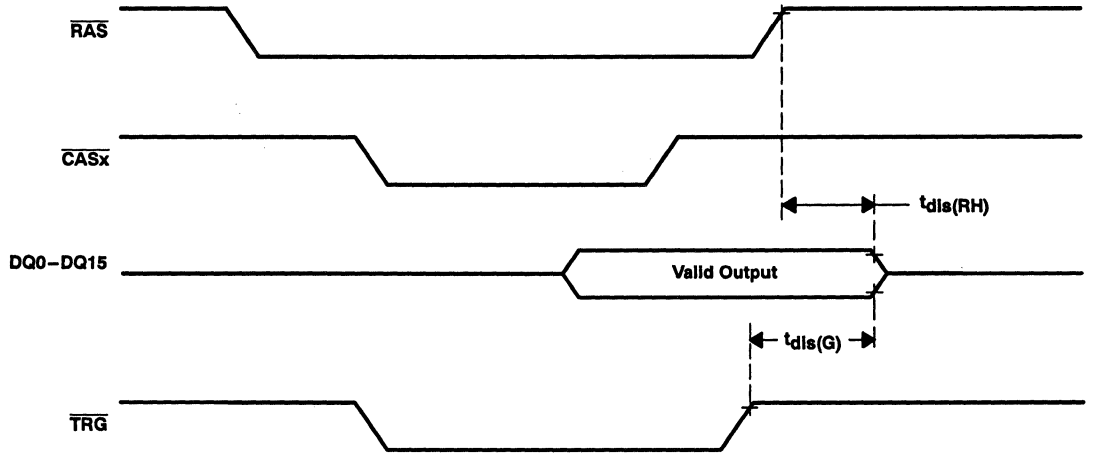


Figure 1. DRAM Read Cycle With $\overline{RAS}$-Controlled Output

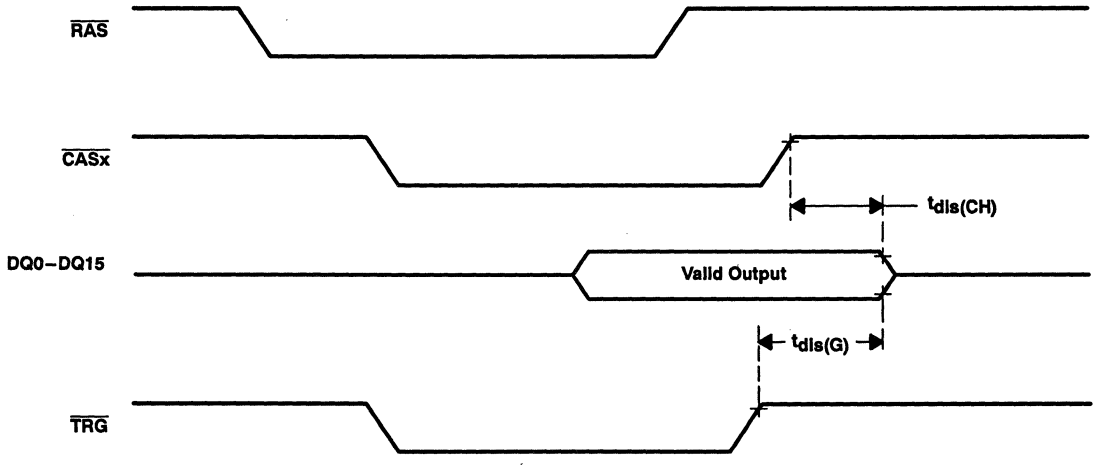


Figure 2. DRAM Read Cycle With $\overline{CASx}$-Controlled Output

extended-data output (continued)

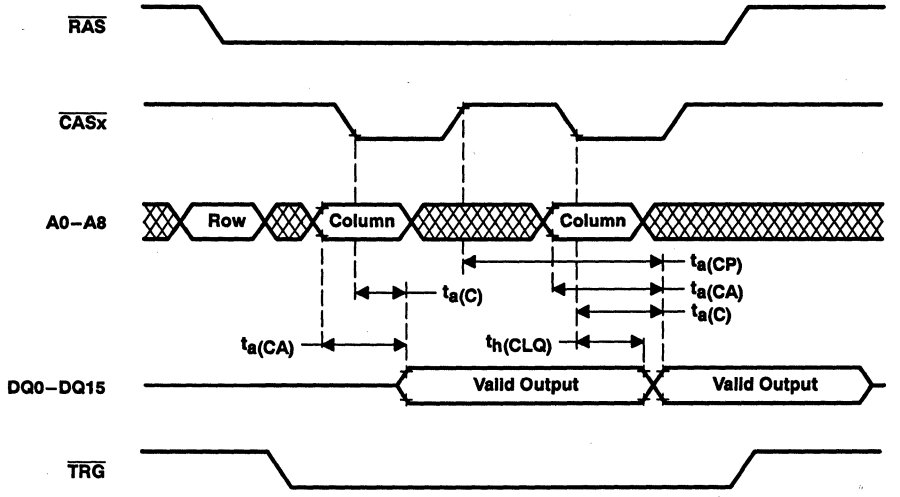


Figure 3. DRAM Page-Read Cycle With Extended Output

byte operation

Byte operation can be applied in DRAM-read cycles, write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. In byte operation, the column address (A0–A8) is latched at the first falling edge of $\overline{CASx}$. In read cycles, $\overline{CASL}$ enables the lower byte (DQ0–DQ7) and $\overline{CASU}$ enables the upper byte (DQ8–DQ15) (see Figure 4).

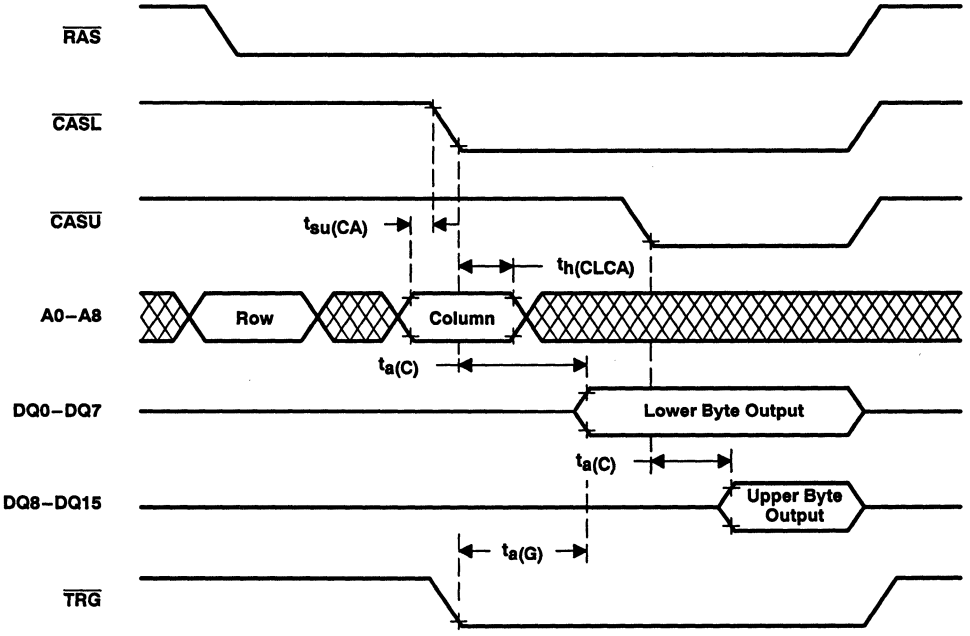


Figure 4. Example of a Byte-Read Cycle

byte operation (continued)

In byte-write operation, $\overline{CASL}$ enables data to be written to the lower byte (DQ0–DQ7), and $\overline{CASU}$ enables data to be written to the upper byte (DQ8–DQ15). In an early write cycle, $\overline{WE}$ is brought low prior to both $\overline{CASx}$ signals, and data setup and hold times for DQ0–DQ15 are referenced to the first falling edge of $\overline{CASx}$ (see Figure 5).

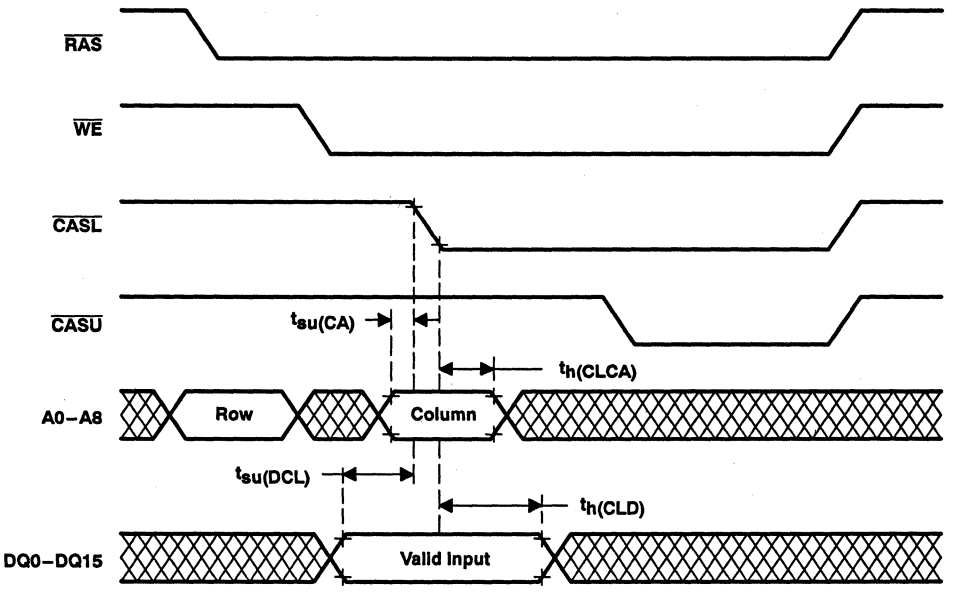


Figure 5. Example of an Early-Write Cycle

byte operation (continued)

For late-write or read-modify-write cycles, $\overline{WE}$ is brought low after either or both $\overline{CASL}$ and $\overline{CASU}$ fall. The data is strobed in with data setup and hold times for DQ0–DQ15 referenced to $\overline{WE}$ (see Figure 6).

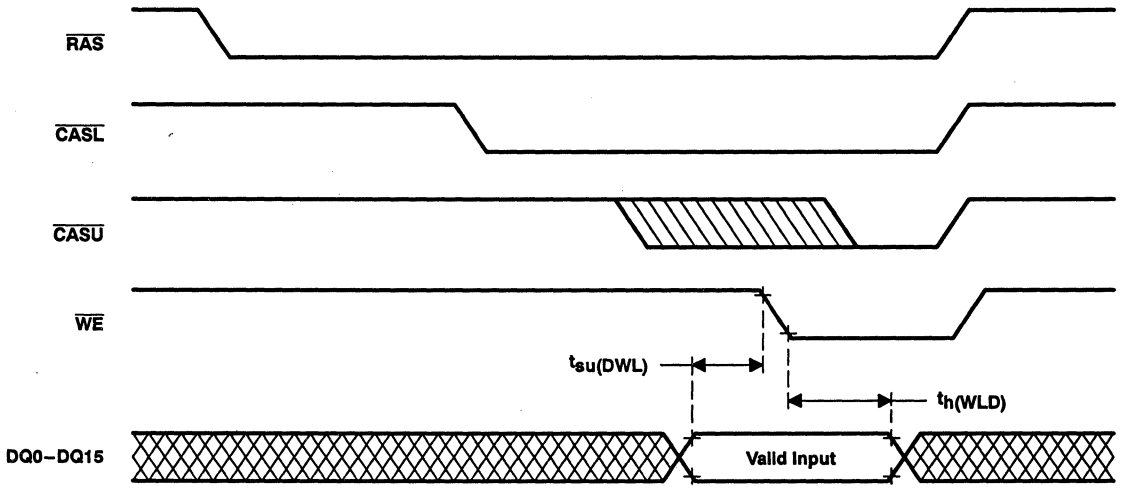


Figure 6. Example of a Late-Write Cycle

write-per-bit

The write-per-bit feature allows masking any combination of the 16 DQs on any write cycle. The write-per-bit operation is invoked when $\overline{WE}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{WE}$ is held high on the falling edge of $\overline{RAS}$, the write operation is performed without any masking. The SMJ55161 offers two write-per-bit modes: nonpersistent write-per-bit and persistent write-per-bit.

nonpersistent write-per-bit

When $\overline{WE}$ is low on the falling edge of $\overline{RAS}$, the write mask is reloaded. A 16-bit binary code (the write-per-bit mask) is input to the device via the DQ pins and latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the 16 I/Os are to be written and which are not. After $\overline{RAS}$ has latched the on-chip write-per-bit mask, input data is driven onto the DQ pins and is latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. $\overline{CASL}$ enables the lower byte (DQ0–DQ7) to be written through the mask and $\overline{CASU}$ enables the upper byte (DQ8–DQ15) to be written through the mask. If a data low (write mask = 0) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data is not written to that I/O. If a data high (write mask = 1) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data is written to that I/O (see Figure 7).

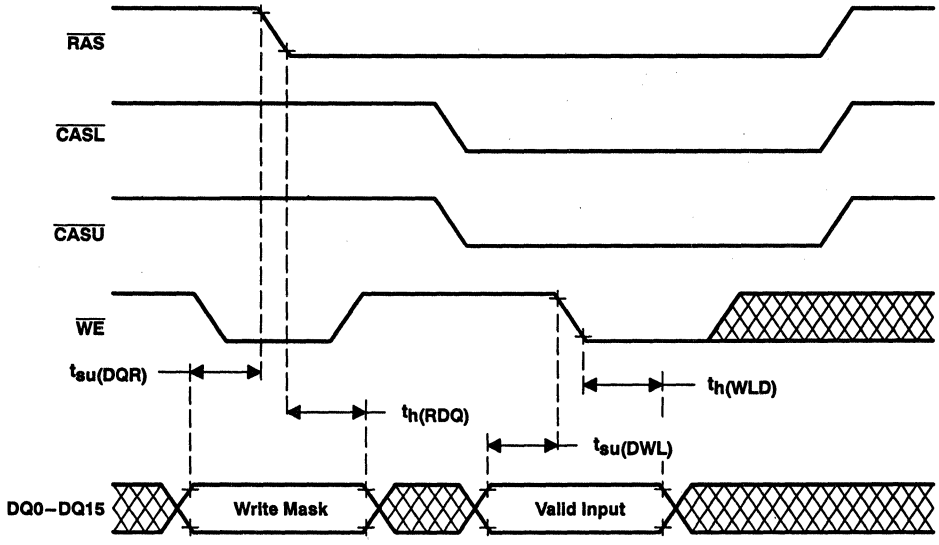


Figure 7. Example of a Nonpersistent Write-Per-Bit (Late-Write) Operation

persistent write-per-bit

The persistent write-per-bit mode is initiated by performing a load-write-mask-register (LMR) cycle. In the persistent write-per-bit mode, the write-per-bit mask is overwritten but remains valid over an arbitrary number of write cycles until another LMR cycle is performed or power is removed.

The LMR cycle is performed using DRAM write-cycle timing with DSF held high on the falling edge of $\overline{RAS}$ and held low on the first falling edge of $\overline{CASx}$. A binary code is input to the write-mask register via the random I/O pins and latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. Byte write control can be applied to the write mask during the LMR cycle. The persistent write-per-bit mode can then be used in exactly the same way as the nonpersistent write-per-bit mode except that the input data on the falling edge of $\overline{RAS}$ is ignored. When the device is set to the persistent write-per-bit mode, it remains in this mode and is reset only by a CBR refresh (option-reset) cycle (see Figure 8).

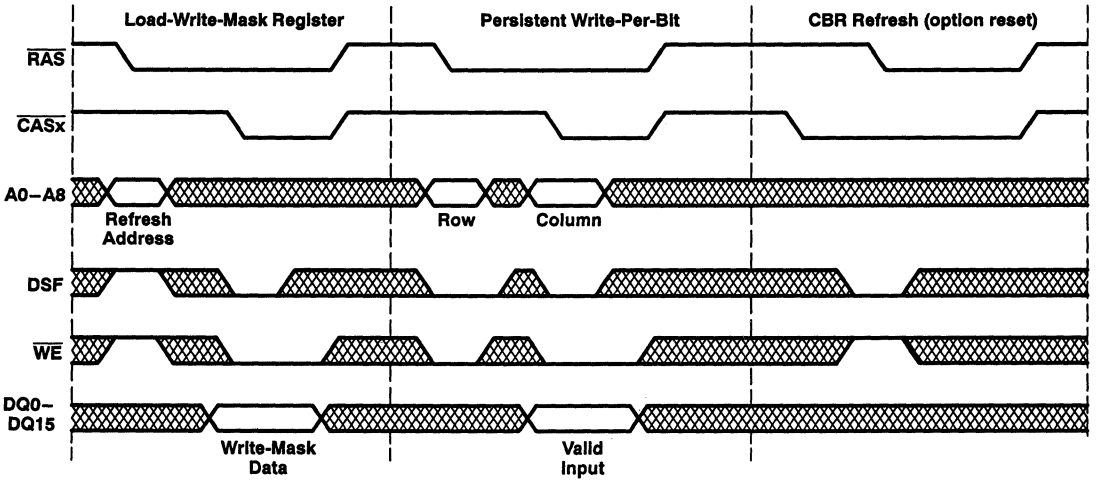


Figure 8. Example of a Persistent Write-Per-Bit Operation

block write

The block-write feature allows up to 64 bits of data to be written simultaneously to one row of the memory array. This function is implemented as 4 columns × 4 DQs and repeated in four quadrants. In this manner, each of the four 1-megabit quadrants can have up to four consecutive columns written at a time with up to 4 DQs per column (see Figure 9).

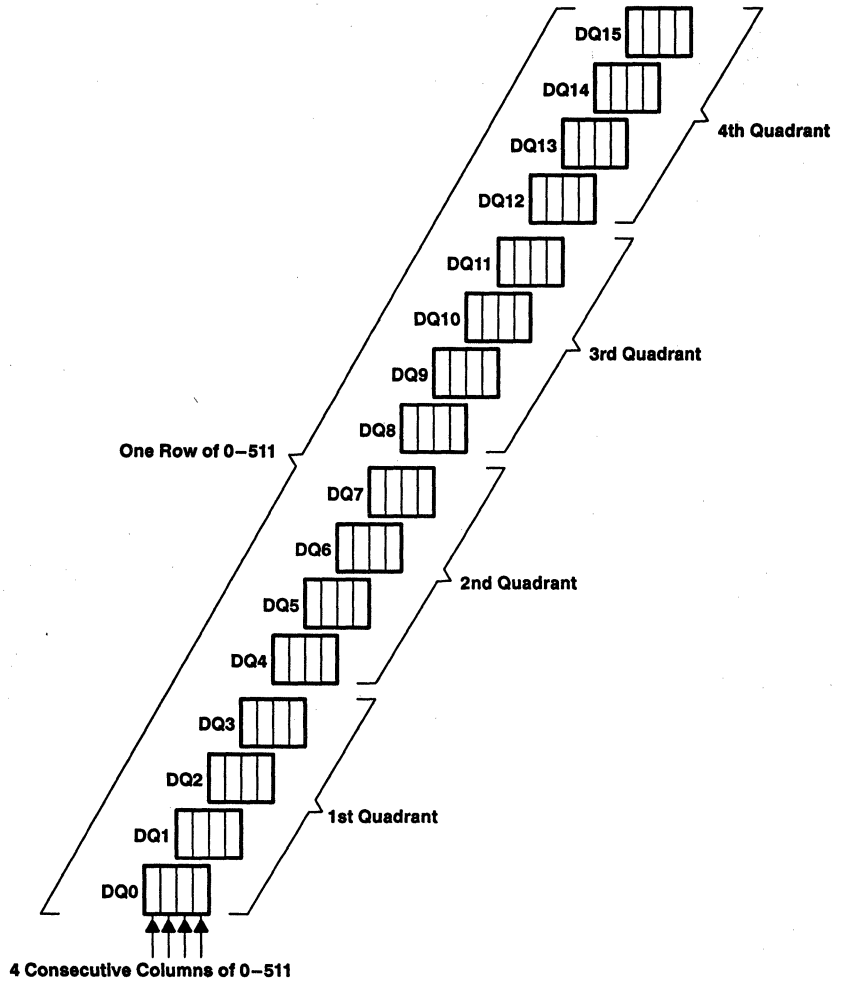


Figure 9. Block-Write Operation

Each 1-megabit quadrant has a 4-bit column mask to mask off any or all of the four columns from being written with data. Nonpersistent write-per-bit or persistent write-per-bit functions can be applied to the block-write operation to provide write-masking options. The DQ data is provided by 4 bits from the on-chip color register. Bits 0–3 from the 16-bit write-mask register, bits 0–3 from the 16-bit column-mask register, and bits 0–3 from the 16-bit color-data register configure the block write for the first quadrant, while bits 4–7, 8–11, and 12–15 of the corresponding registers control the other quadrants in a similar fashion (see Figure 14).

block write (continued)

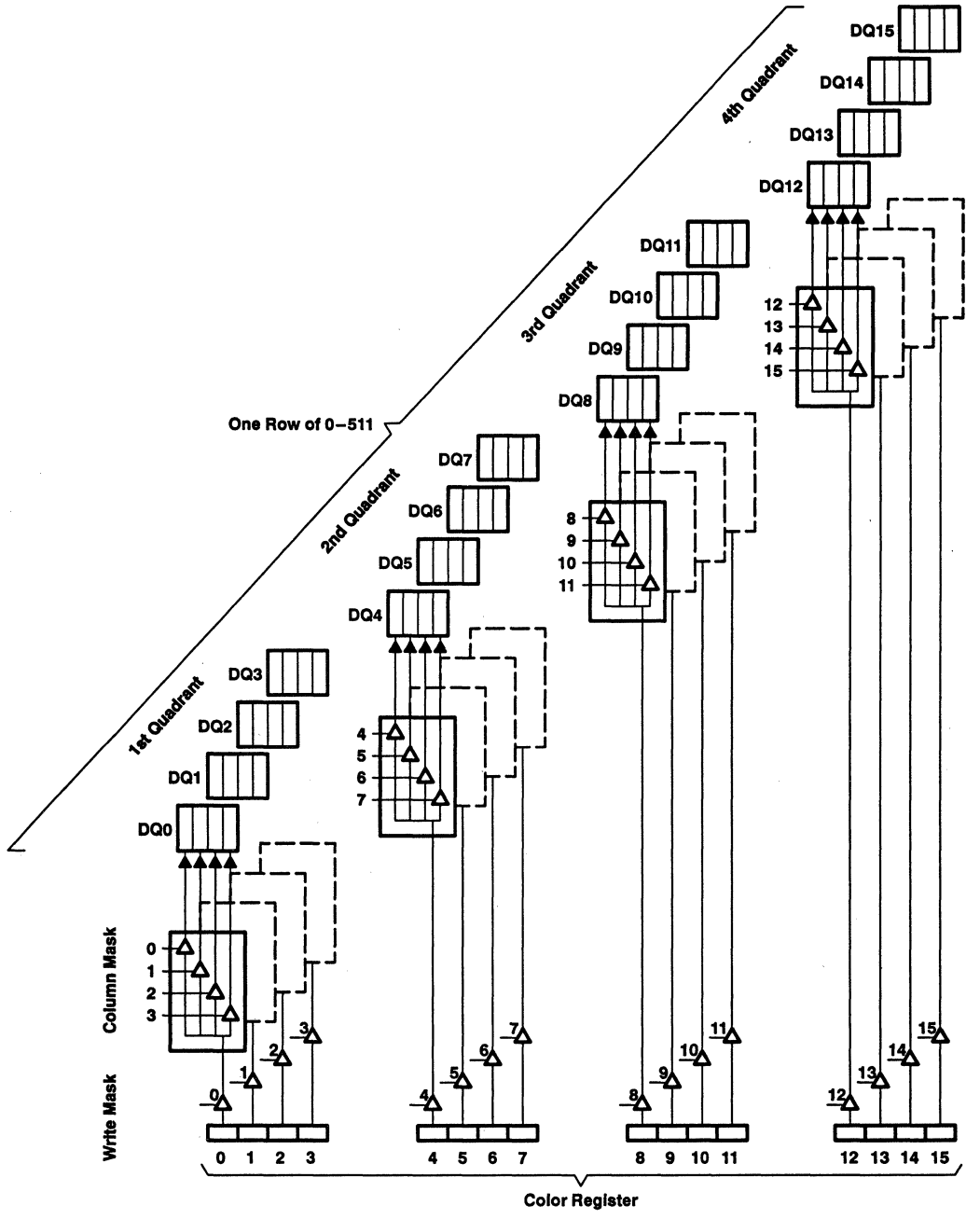


Figure 10. Block Write With Masks

block write (continued)

A set of four columns makes a block, resulting in 128 blocks along one row. Block 0 comprises columns 0–3, block 1 comprises columns 4–7, block 2 comprises columns 8–11, etc., as shown in Figure 11.

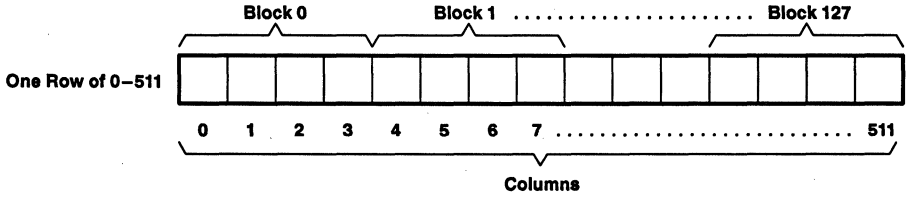


Figure 11. Block Columns Organization

During block-write cycles, only the seven most significant column addresses (A2–A8) are latched on the first falling edge of $\overline{CASx}$ to decode one of the 128 blocks. Address bits A0–A1 are ignored. Each 1-megabit quadrant has the same block selected.

A block-write cycle is entered in a manner similar to a DRAM write cycle except DSF is held high on the first falling edge of $\overline{CASx}$. As in a DRAM write operation, $\overline{CASL}$ and $\overline{CASU}$ enable the corresponding lower and upper DRAM DQ bytes to be written. The column-mask data is input via the DQs and is latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. The 16-bit color-data register must be loaded prior to performing a block write as described below. Refer to the write-per-bit section for details on use of the write-mask capability, allowing additional performance options.

Example of block write:

block-write column address = 110000000 (A0–A8 from left to right)

	bit 0			bit 15
color-data register =	1011	1011	1100	0111
write-mask register =	1110	1111	1111	1011
column-mask register =	1111	0000	0111	1010
	1st Quad	2nd Quad	3rd Quad	4th Quad

Column-address bits A0 and A1 are ignored. Block 0 (columns 0–3) is selected for each 1-megabit quadrant. The first quadrant has DQ0–DQ2 written with bits 0–2 from the color-data register (101) to all four columns of block 0. DQ3 is not written and retains its previous data due to write-mask-register-bit 3 being 0.

The second quadrant (DQ4–DQ7) has all four columns masked off due to column-mask bits 4–7 being 0, so that no data is written.

The third quadrant (DQ8–DQ11) has its four DQs written with bits 8–11 from the color-data register (1100) to columns 1–3 of its block 0. Column 0 is not written and retains its previous data on all four DQs due to column-mask-register-bit 8 being 0.

block write (continued)

The fourth quadrant (DQ12–DQ15) has DQ12, DQ14, and DQ15 written with bits 12, 14, and 15 from the color-data register to column 0 and column 2 of its block 0. DQ13 retains its previous data on all columns due to the write mask. Columns 1 and 3 retain their previous data on all DQs due to the column mask. If the previous data for the quadrant was all 0s, the fourth quadrant would contain the data pattern shown in Figure 12 after the block-write operation shown in the previous example.

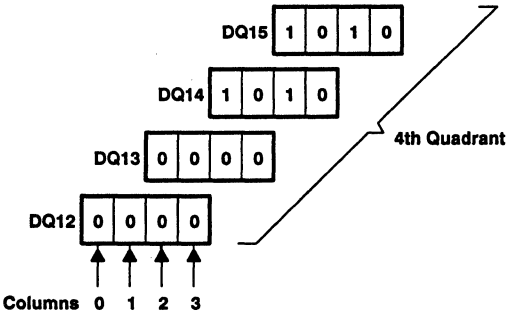
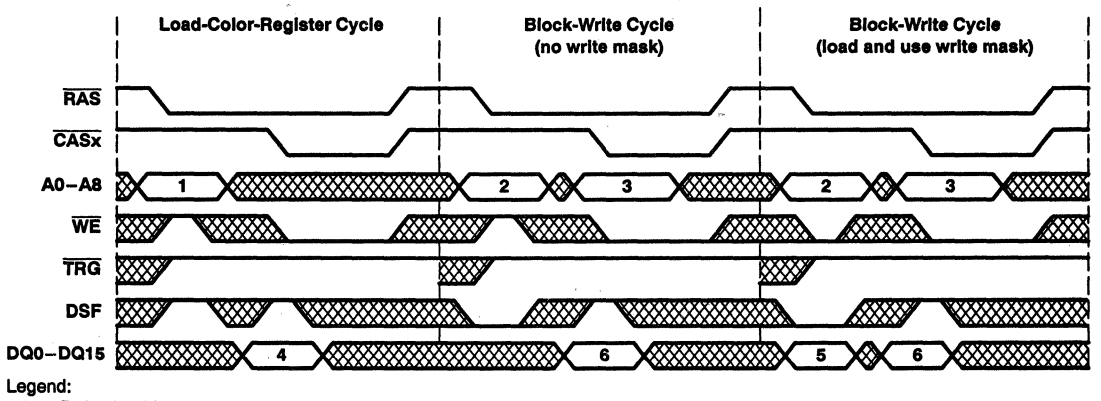


Figure 12. Example of Fourth Quadrant After a Block-Write Operation

load color register

The load-color-register cycle is performed using normal DRAM write-cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$, $\overline{CASL}$, and $\overline{CASU}$. The color register is loaded from pins DQ0–DQ15, which are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. If only one $\overline{CASx}$ is low, only the corresponding byte of the color register is loaded. When the color register is loaded, it retains data until power is lost or until another load-color-register cycle is performed (see Figures 13 and 14).



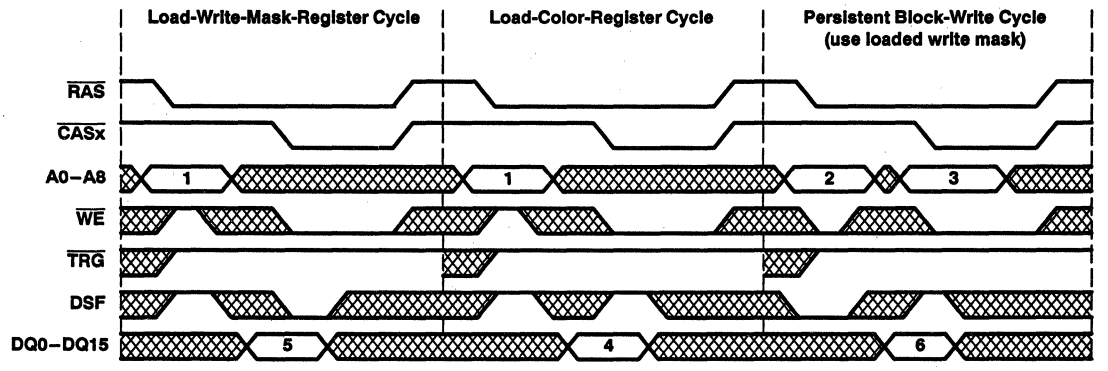
Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the first falling edge of $\overline{CASx}$.
4. Color-register data
5. Write-mask data: DQ0–DQ15 are latched on the falling edge of $\overline{RAS}$.
6. Column-mask data: DQi–DQi+3 (i = 0, 4, 8, 12) are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.

= don't care

Figure 13. Example of Block Writes

load color register (continued)



Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the first falling edge of $\overline{CASx}$.
4. Color-register data
5. Write-mask data: DQ0 – DQ15 are latched on the falling edge of $\overline{CASx}$.
6. Column-mask data: DQi – DQi+3 (i = 0, 4, 8, 12) are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.

= don't care

Figure 14. Example of a Persistent Block Write

DRAM-to-SAM transfer operation

During the DRAM-to-SAM transfer operation, one half of a row (256 columns) in the DRAM array is selected to be transferred to the 256-bit serial-data register. The transfer operation is invoked by $\overline{TRG}$ being brought low and $\overline{WE}$ being held high on the falling edge of $\overline{RAS}$. The state of DSF, which is latched on the falling edge of $\overline{RAS}$, determines whether the full-register-transfer read operation or the split-register-transfer read operation is performed.

Table 2. SAM Function Table

FUNCTION	$\overline{RAS}$ FALL				$\overline{CASx}$ FALL	ADDRESS		DQ0–DQ15		MNE CODE
	$\overline{CASx}$†	$\overline{TRG}$	$\overline{WE}$	DSF	DSF	$\overline{RAS}$	$\overline{CASx}$	$\overline{RAS}$	$\overline{CASx}$ $\overline{WE}$	
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT

† Logic L is selected when either $\overline{CASL}$ or $\overline{CASU}$ are low.
X = don't care

full-register-transfer read

A full-register-transfer read operation loads data from a selected half of a row in the DRAM into the SAM. $\overline{TRG}$ is brought low and latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. The nine column-address bits (A0–A8) are latched at the first falling edge of $\overline{CASx}$, where address bit A8 selects which half of the row is transferred. Address bits A0–A7 select one of the SAM's 256 available tap points from which the serial data is read out (see Figure 15).

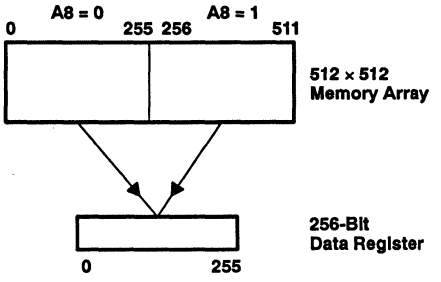


Figure 15. Full-Register-Transfer Read

A full-register-transfer read can be performed in three ways: early load, real-time load (or midline load), or late load. Each of these offers the flexibility of controlling the $\overline{TRG}$ trailing edge in the full-register-transfer read cycle (see Figure 16).

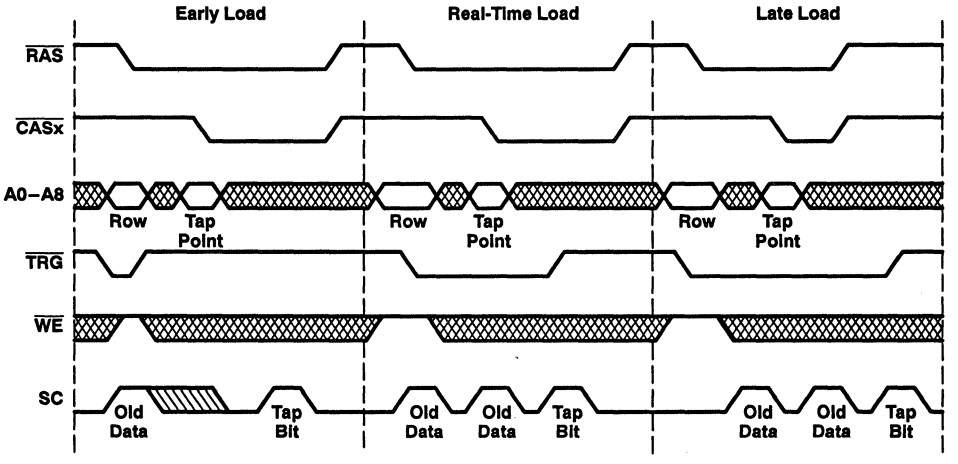


Figure 16. Example of Full-Register-Transfer Read Operations

split-register-transfer read

In the split-register-transfer-read operation, the serial-data register is split into halves. The low half contains bits 0–127, and the high half contains bits 128–255. While one half is being read out of the SAM port, the other half can be loaded from the memory array.

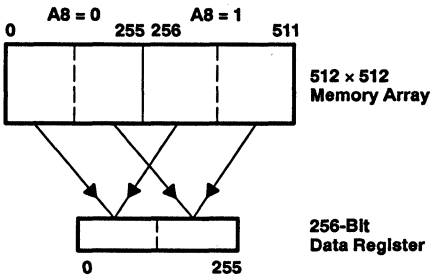
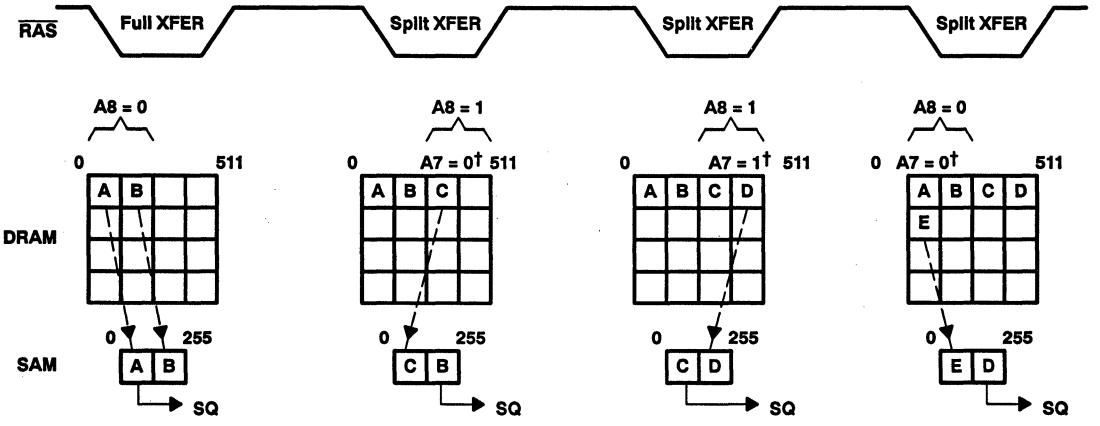


Figure 17. Split-Register-Transfer Read

To invoke a split-register-transfer-read cycle, DSF is brought high, $\overline{TRG}$ is brought low, and both are latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. Eight of the nine column-address bits (A0–A6 and A8) are latched at the first falling edge of $\overline{CASx}$. Column-address bit A8 selects which half of the row is to be transferred. Column-address bits A0–A6 selects one of the 127 tap points in the specified half of the SAM. Column-address bit A7 is ignored, and the split-register transfer is internally controlled to select the inactive register half.



† A7 shown is internally controlled.

Figure 18. Example of a Split-Register-Transfer Read Operation

A full-register-transfer read must precede the first split-register-transfer read to ensure proper operation. After the full-register-transfer read cycle, the first split-register-transfer read can follow immediately without any minimum SC clock requirement.

split-register-transfer read (continued)

QSF indicates which half of the register is being accessed during serial-access operation. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of the SAM. When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF changes state upon completing a full-register-transfer read cycle. The tap point loaded during the current transfer cycle determines the state of QSF. QSF also changes state when a boundary between two register halves is reached.

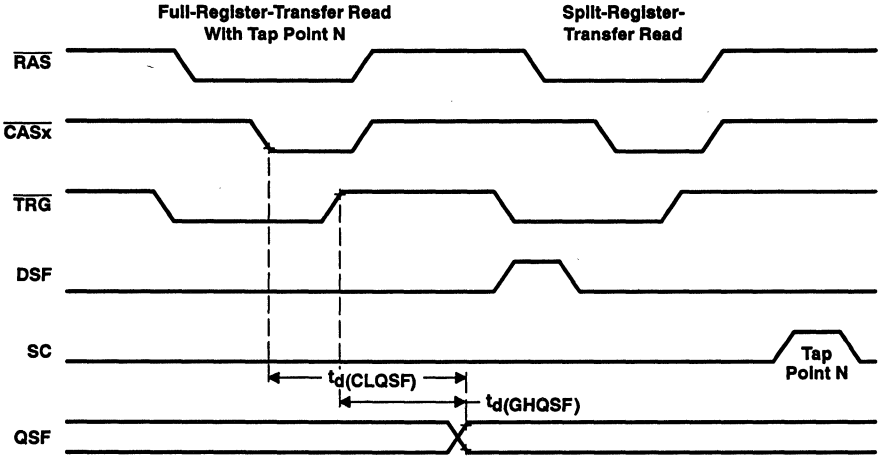


Figure 19. Example of a Split-Register-Transfer Read After a Full-Register-Transfer Read

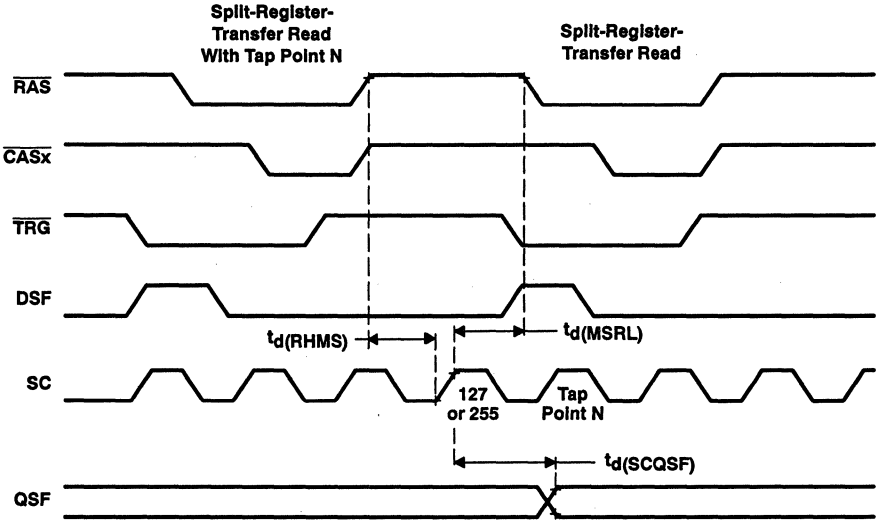


Figure 20. Example of Successive Split-Register-Transfer Read Operations

serial-read operation

The serial-read operation can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during transfer operations. Serial data can be read from the SAM by clocking SC starting at the tap point loaded by the preceding transfer cycle, proceeding sequentially to the most significant bit (bit 255), and then wrapping around to the least significant bit (bit 0), as shown in Figure 21.

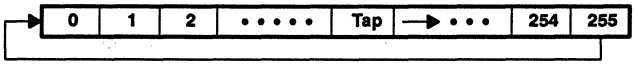


Figure 21. Serial-Pointer Direction for Serial Read

For split-register-transfer read operation, serial data can be read out from the active half of the SAM by clocking SC starting at the tap point loaded by the preceding split-register-transfer cycle. The serial pointer then proceeds sequentially to the most significant bit of the half, bit 127 or bit 255. If there is a split-register-transfer read to the inactive half during this period, the serial pointer points next to the tap point location loaded by that split-register transfer (see Figure 22).

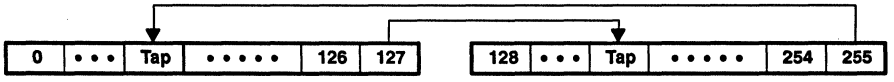


Figure 22. Serial Pointer for Split-Register Read – Case I

If there is no split-register-transfer read to the inactive half during this period, the serial pointer points next to bit 128 or bit 0, respectively (see Figure 23).

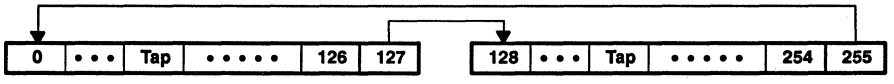


Figure 23. Serial Pointer for Split-Register Read – Case II

split-register programmable stop point

The SMJ55161 offers programmable stop-point mode for split-register-transfer read operation. This mode can be used to improve two-dimensional drawing performance in a nonscanline data format.

In split-register-transfer read operation, the stop point is defined as a register location at which the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM. While in stop-point mode, the SAM is divided into partitions whose length is programmed via row addresses A4–A7 in a CBR set (CBRS) cycle. The last serial-address location of each partition is the stop point (see Figure 24).

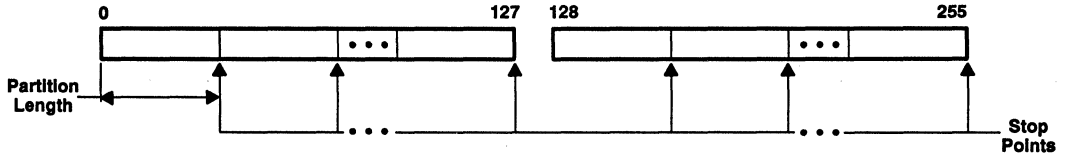


Figure 24. Example of the SAM With Partitions

split-register programmable stop point (continued)

Stop-point mode is not active until the CBRS cycle is initiated. The CBRS operation is performed by holding $\overline{CAS}$x and $\overline{WE}$ low and DSF high on the falling edge of $\overline{RAS}$. The falling edge of $\overline{RAS}$ also latches row addresses A4–A7 which are used to define the SAM's partition length. The other row-address inputs are don't cares. Stop-point mode should be initiated after the initialization cycles are performed (see Table 3).

Table 3. Programming Code for Stop-Point Mode

MAXIMUM PARTITION LENGTH	ADDRESS AT $\overline{RAS}$ IN CBRS CYCLE						NUMBER OF PARTITIONS	STOP-POINT LOCATIONS
	A8	A7	A6	A5	A4	A0–A3		
16	X	L	L	L	L	X	16	15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255
32	X	L	L	L	H	X	8	31, 63, 95, 127, 159, 191, 223, 255
64	X	L	L	H	H	X	4	63, 127, 191, 255
128 (default)	X	L	H	H	H	X	2	127, 255

In stop-point mode, the tap point loaded during the split-register-transfer read cycle determines the SAM partition in which the serial output begins and at which stop point the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM (see Figure 25).

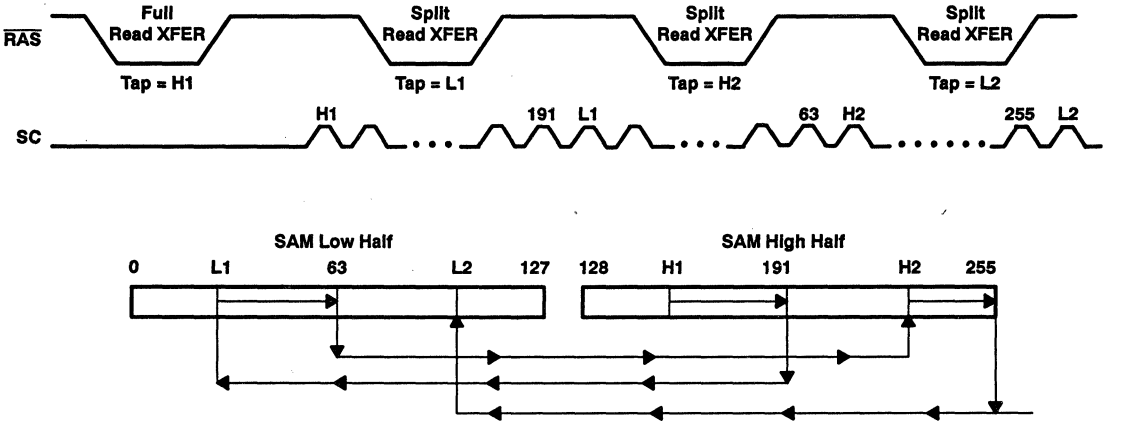


Figure 25. Example of Split-Register Operation With Programmable Stop Points

256-/512-bit compatibility of split-register programmable stop point

The stop-point mode is designed to be compatible with both 256-bit SAM and 512-bit SAM devices. After the CBRS cycle is initiated, the stop-point mode becomes active. In the stop-point mode, and only in the stop-point mode, the column-address bits AY7 and AY8 are internally swapped to assure compatibility (see Figure 26). This address-bit swap applies to the column address, and it is effective for all DRAM and transfer cycles. For example, during the split-register-transfer cycle with stop point, column-address bit AY8 is a don't care and AY7 decodes the DRAM row half for the split-register transfer. During stop-point mode, a CBR (option reset) cycle is not recommended, because this ends the stop-point mode and restores address bits AY7 and AY8 to their normal functions. Consistent use of CBR cycles ensures that the SMJ55161 remains in normal mode.

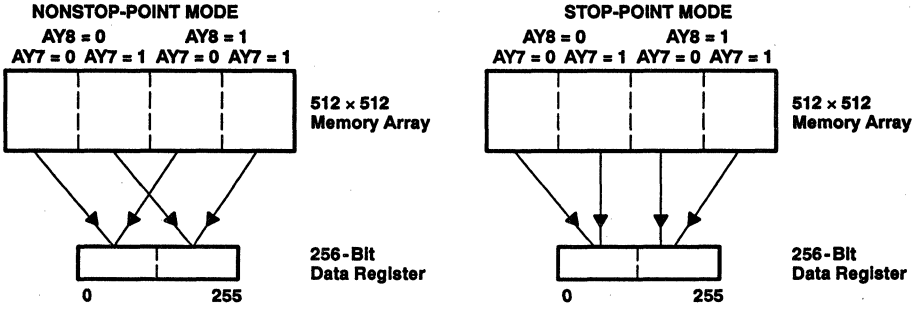


Figure 26. DRAM-to-SAM Mapping, Nonstop-Point Versus Stop Point

IMPORTANT: For proper device operation, a stop-point-mode (CBRS) cycle should be initiated immediately after the power-up initialization cycles are performed.

power up

To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight $\overline{RAS}$ cycles or eight CBR cycles to initialize the DRAM port. A full-register-transfer read cycle and two SC cycles are required to initialize the SAM port.

After initialization, the internal state of the SMJ55161 is as follows:

	STATE AFTER INITIALIZATION
QSF	Defined by the transfer cycle during initialization
Write mode	Nonpersistent mode
Write-mask register	Undefined
Color register	Undefined
Serial-register tap point	Defined by the transfer cycle during initialization
SAM port	Output mode

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −1 V to 7 V
Voltage range on any pin ..... −1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1.1 W
Operating free-air temperature range, T_A ..... −55°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	−55		125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	SAM PORT	'55161-70		'55161-80		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −1 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 5.8 V, All other pins at 0 V to V_{CC}			±10		±10	µA
I_O	Output current (leakage) (see Note 3)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}			±10		±10	µA
I_{CC1}	Operating current§	See Note 4	Standby		165		160	mA
I_{CC1A}	Operating current§	$t_{c(SC)}$ = MIN	Active		210		195	mA
I_{CC2}	Standby current	All clocks = V_{CC}	Standby		12		12	mA
I_{CC2A}	Standby current	$t_{c(SC)}$ = MIN	Active		70		65	mA
I_{CC3}	$\overline{RAS}$-only refresh current	See Note 4	Standby		165		160	mA
I_{CC3A}	$\overline{RAS}$-only refresh current	$t_{c(SC)}$ = MIN, See Note 4	Active		215		195	mA
I_{CC4}	Page-mode current§	$t_{c(P)}$ = MIN, See Note 5	Standby		100		95	mA
I_{CC4A}	Page-mode current§	$t_{c(SC)}$ = MIN, See Note 5	Active		145		130	mA
I_{CC5}	CBR current	See Note 4	Standby		165		160	mA
I_{CC5A}	CBR current	$t_{c(SC)}$ = MIN, See Note 4	Active		210		195	mA
I_{CC6}	Data-transfer current	See Note 4	Standby		180		170	mA
I_{CC6A}	Data-transfer current	$t_{c(SC)}$ = MIN	Active		225		200	mA

‡ For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

§ Measured with outputs open

NOTES: 3. $\overline{SE}$ is disabled for SQ output leakage tests.
4. Measured with one address change while $\overline{RAS}$ = V_{IL}; $t_{c(rd)}$, $t_{c(W)}$, $t_{c(TRD)}$ = MIN
5. Measured with one address change while $\overline{CASx}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		5	10	pF
$C_{i(RC)}$	Input capacitance, address-strobe inputs		8	10	pF
$C_{i(W)}$	Input capacitance, write-enable input		7	10	pF
$C_{i(SC)}$	Input capacitance, serial clock		6	10	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	10	pF
$C_{i(DSF)}$	Input capacitance, special function		7	10	pF
$C_{i(TRG)}$	Input capacitance, transfer-register input		7	10	pF
$C_{o(O)}$	Output capacitance, SQ and DQ		12	15	pF
$C_{o(QSF)}$	Output capacitance, QSF		10	12	pF

NOTE 6: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		TEST CONDITIONS†	ALT. SYMBOL	'55161-70		'55161-80		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CASx}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		20		20	ns
$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{AA}		35		40	ns
$t_{a(CP)}$	Access time from $\overline{CASx}$ high	$t_{d(RLCL)}$ = MAX	t_{CPA}		40		45	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MAX	t_{RAC}		70		80	ns
$t_{a(G)}$	Access time of DQ from $\overline{TRG}$ low		t_{OEA}		20		20	ns
$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 30 pF	t_{SCA}		20		25	ns
$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		15		20	ns
$t_{dis(CH)}$	Disable time, random output from $\overline{CASx}$ high (see Note 8)	C_L = 50 pF	t_{OFF}	0	20	0	20	ns
$t_{dis(RH)}$	Disable time, random output from $\overline{RAS}$ high (see Note 8)	C_L = 50 pF		0	20	0	20	ns
$t_{dis(G)}$	Disable time, random output from $\overline{TRG}$ high (see Note 8)	C_L = 50 pF	t_{OEZ}	0	20	0	20	ns
$t_{dis(WL)}$	Disable time, random output from $\overline{WE}$ low (see Note 8)	C_L = 50 pF	t_{WEZ}	0	20	0	20	ns
$t_{dis(SE)}$	Disable time, serial output from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	0	15	0	20	ns

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

NOTES: 7. Switching times for RAM-port output are measured with a load equivalent to 1 TTL load and 50 pF. Data-out reference level: V_{OH}/V_{OL} = 2 V/0.8 V. Switching times for SAM-port output are measured with a load equivalent to 1 TTL load and 30 pF. Serial-data out reference level: V_{OH}/V_{OL} = 2 V/0.8 V.

8. $t_{dis(CH)}$, $t_{dis(RH)}$, $t_{dis(G)}$, $t_{dis(WL)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature†

		ALT. SYMBOL	'55161-70		'55161-80		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Cycle time, read	t_{RC}	130		150		ns
$t_{c(W)}$	Cycle time, write	t_{WC}	130		150		ns
$t_{c(rdW)}$	Cycle time, read-modify-write	t_{RMW}	175		200		ns
$t_{c(P)}$	Cycle time, page-mode read, write	t_{PC}	45		50		ns
$t_{c(RDWP)}$	Cycle time, page-mode read-modify-write	t_{PRMW}	85		90		ns
$t_{c(TRD)}$	Cycle time, transfer read	t_{RC}	130		150		ns
$t_{c(SC)}$	Cycle time, serial clock (see Note 9)	t_{SCC}	22		30		ns
$t_{w(CH)}$	Pulse duration, $\overline{CASx}$ high	t_{CPN}	10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CASx}$ low (see Note 10)	t_{CAS}	20	10 000	20	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	50		60		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 11)	t_{RAS}	70	10 000	80	10 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{WE}$ low	t_{WP}	10		15		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		20		20		ns
$t_{w(SCH)}$	Pulse duration, SC high	t_{SC}	8		10		ns
$t_{w(SCL)}$	Pulse duration, SC low	t_{SCP}	8		10		ns
$t_{w(GH)}$	Pulse duration, $\overline{TRG}$ high	t_{TP}	20		20		ns
$t_{w(RL)P}$	Pulse duration, $\overline{RAS}$ low (page mode)	t_{RASP}	70	100 000	80	100 000	ns
$t_{su(CA)}$	Setup time, column address before $\overline{CASx}$ low	t_{ASC}	0		0		ns
$t_{su(SFC)}$	Setup time, DSF before $\overline{CASx}$ low	t_{FSC}	0		0		ns
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low	t_{ASR}	0		0		ns
$t_{su(WMR)}$	Setup time, $\overline{WE}$ before $\overline{RAS}$ low	t_{WSR}	0		0		ns
$t_{su(DQR)}$	Setup time, DQ before $\overline{RAS}$ low	t_{MS}	0		0		ns
$t_{su(TRG)}$	Setup time, $\overline{TRG}$ high before $\overline{RAS}$ low	t_{THS}	0		0		ns
$t_{su(SFR)}$	Setup time, DSF low before $\overline{RAS}$ low	t_{FSR}	0		0		ns
$t_{su(DCL)}$	Setup time, data valid before $\overline{CASx}$ low	t_{DSC}	0		0		ns
$t_{su(DWL)}$	Setup time, data valid before $\overline{WE}$ low	t_{DSW}	0		0		ns
$t_{su(rd)}$	Setup time, read command, $\overline{WE}$ high before $\overline{CASx}$ low	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Setup time, early-write command, $\overline{WE}$ low before $\overline{CASx}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Setup time, $\overline{WE}$ low before $\overline{CASx}$ high, write	t_{CWL}	15		20		ns
$t_{su(WRH)}$	Setup time, $\overline{WE}$ low before $\overline{RAS}$ high, write	t_{RWL}	20		20		ns
$t_{h(CLCA)}$	Hold time, column address after $\overline{CASx}$ low	t_{CAH}	10		15		ns
$t_{h(SFC)}$	Hold time, DSF after $\overline{CASx}$ low	t_{CFH}	15		15		ns
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low	t_{RAH}	10		10		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. Cycle time assumes t_t = 3 ns.

10. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this can require additional $\overline{CASx}$ low time [$t_{w(CL)}$].

11. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this can require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued) †

			ALT. SYMBOL	'55161-70		'55161-80		UNIT
				MIN	MAX	MIN	MAX	
$t_{h(TRG)}$	Hold time, $\overline{TRG}$ after $\overline{RAS}$ low		t_{THH}	15		15		ns
$t_{h(RWM)}$	Hold time, write mask after $\overline{RAS}$ low		t_{RWH}	15		15		ns
$t_{h(RDQ)}$	Hold time, DQ after $\overline{RAS}$ low (write-mask operation)		t_{MH}	15		15		ns
$t_{h(SFR)}$	Hold time, DSF after $\overline{RAS}$ low		t_{RFH}	10		10		ns
$t_{h(RLCA)}$	Hold time, column address valid after $\overline{RAS}$ low (see Note 12)		t_{AR}	30		35		ns
$t_{h(CLD)}$	Hold time, data valid after $\overline{CASx}$ low		t_{DH}	15		15		ns
$t_{h(RLD)}$	Hold time, data valid after $\overline{RAS}$ low (see Note 12)		t_{DHR}	35		35		ns
$t_{h(WLD)}$	Hold time, data valid after $\overline{WE}$ low		t_{DH}	15		15		ns
$t_{h(CHrd)}$	Hold time, read, $\overline{WE}$ high after $\overline{CASx}$ high (see Note 13)		t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Hold time, read, $\overline{WE}$ high after $\overline{RAS}$ high (see Note 13)		t_{RRH}	0		0		ns
$t_{h(CLW)}$	Hold time, write, $\overline{WE}$ low after $\overline{CASx}$ low		t_{WCH}	15		15		ns
$t_{h(RLW)}$	Hold time, write, $\overline{WE}$ low after $\overline{RAS}$ low (see Note 12)		t_{WCR}	35		35		ns
$t_{h(WLG)}$	Hold time, $\overline{TRG}$ high after $\overline{WE}$ low (see Note 14)		t_{OEH}	10		10		ns
$t_{h(SHSQ)}$	Hold time, SQ valid after SC high		t_{SOH}	2		2		ns
$t_{h(RSF)}$	Hold time, DSF after $\overline{RAS}$ low		t_{FHR}	35		35		ns
$t_{h(CLQ)}$	Hold time, output valid after $\overline{CASx}$ low		t_{DHC}	0		0		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ high		t_{CSH}	70		80		ns
		See Note 15	t_{CHR}	10		15		
$t_{d(CHRL)}$	Delay time, $\overline{CASx}$ high to $\overline{RAS}$ low		t_{CRP}	0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ high		t_{RSH}	20		20		ns
$t_{d(CLWL)}$	Delay time, $\overline{CASx}$ low to $\overline{WE}$ low (see Notes 16 and 17)		t_{CWD}	45		50		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ low (see Note 18)		t_{RCD}	20	50	20	60	ns
$t_{d(CARH)}$	Delay time, column address valid to $\overline{RAS}$ high		t_{RAL}	35		40		ns
$t_{d(CACH)}$	Delay time, column address valid to $\overline{CASx}$ high		t_{CAL}	35		40		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{WE}$ low (see Note 16)		t_{RWD}	95		105		ns
$t_{d(CAWL)}$	Delay time, column address valid to $\overline{WE}$ low (see Note 16)		t_{AWD}	60		65		ns
$t_{d(CLRL)}$	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ low (see Note 15)		t_{CSR}	0		0		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CASx}$ low (see Note 15)		t_{RPC}	0		0		ns
$t_{d(CLGH)}$	Delay time, $\overline{CASx}$ low to $\overline{TRG}$ high for DRAM read cycles			20		20		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ		t_{OED}	15		15		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{d(CHrd)}$ must be satisfied for a read cycle.
14. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
15. CBR refresh operation only
16. Read-modify-write operation only
17. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
18. The maximum value is specified only to assure $\overline{RAS}$ access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	'55161-70		'55161-80		UNIT
			MIN	MAX	MIN	MAX	
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (see Note 19)	t_{RTH}	55		60		ns
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 20)	t_{RSD}	70		80		ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address valid	t_{RAD}	15	35	15	40	ns
$t_{d(GLRH)}$	Delay time, $\overline{TRG}$ low to $\overline{RAS}$ high	t_{ROH}	20		20		ns
$t_{d(CLSH)}$	Delay time, $\overline{CASx}$ low to first SC high after $\overline{TRG}$ high (see Note 20)	t_{CSD}	20		25		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 19 and 20)	t_{TSL}	5		5		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see 19)	t_{TRD}	−10		−10		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 21)	t_{TRP}	50		60		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 19)	t_{TSD}	15		20		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split-register-transfer read cycles		20		20		ns
$t_{d(CLTH)}$	Delay time, $\overline{CASx}$ low to $\overline{TRG}$ high in real-time-transfer read cycles	t_{CTH}	15		15		ns
$t_{d(CASH)}$	Delay time, column address to first SC in early-load-transfer read cycles	t_{ASD}	25		30		ns
$t_{d(CAGH)}$	Delay time, column address to $\overline{TRG}$ high in real-time-transfer read cycles	t_{ATH}	20		20		ns
$t_{d(DCL)}$	Delay time, data to $\overline{CASx}$ low	t_{DZC}	0		0		ns
$t_{d(DGL)}$	Delay time, data to $\overline{TRG}$ low	t_{DZO}	0		0		ns
$t_{d(MSRL)}$	Delay time, last (most significant) rising edge of SC to $\overline{RAS}$ low before boundary switch during split-register-transfer read cycles		20		20		ns
$t_{d(SCQSF)}$	Delay time, last (127 or 255) rising edge of SC to QSF switching at the boundary during split-register-transfer read cycles (see Note 22)	t_{SQD}		25		30	ns
$t_{d(CLQSF)}$	Delay time, $\overline{CASx}$ low to QSF switching in transfer-read cycles (see Note 22)	t_{CQD}		30		35	ns
$t_{d(GHQSF)}$	Delay time, $\overline{TRG}$ high to QSF switching in transfer-read cycles (see Note 22)	t_{TQD}		25		30	ns
$t_{d(RLQSF)}$	Delay time, $\overline{RAS}$ low to QSF switching in transfer-read cycles (see Note 22)	t_{RQD}		70		75	ns
$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8	ms
t_t	Transition time	t_T	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 19. Real-time-load transfer read or late-load-transfer read cycle only
20. Early-load-transfer read cycle only
21. Full-register-(read) transfer cycles only
22. Switching times for QSF output are measured with a load equivalent to 1 TTL load and 30 pF, and output reference level is V_{OH} / V_{OL} = 2 V/0.8 V.

PARAMETER MEASUREMENT INFORMATION

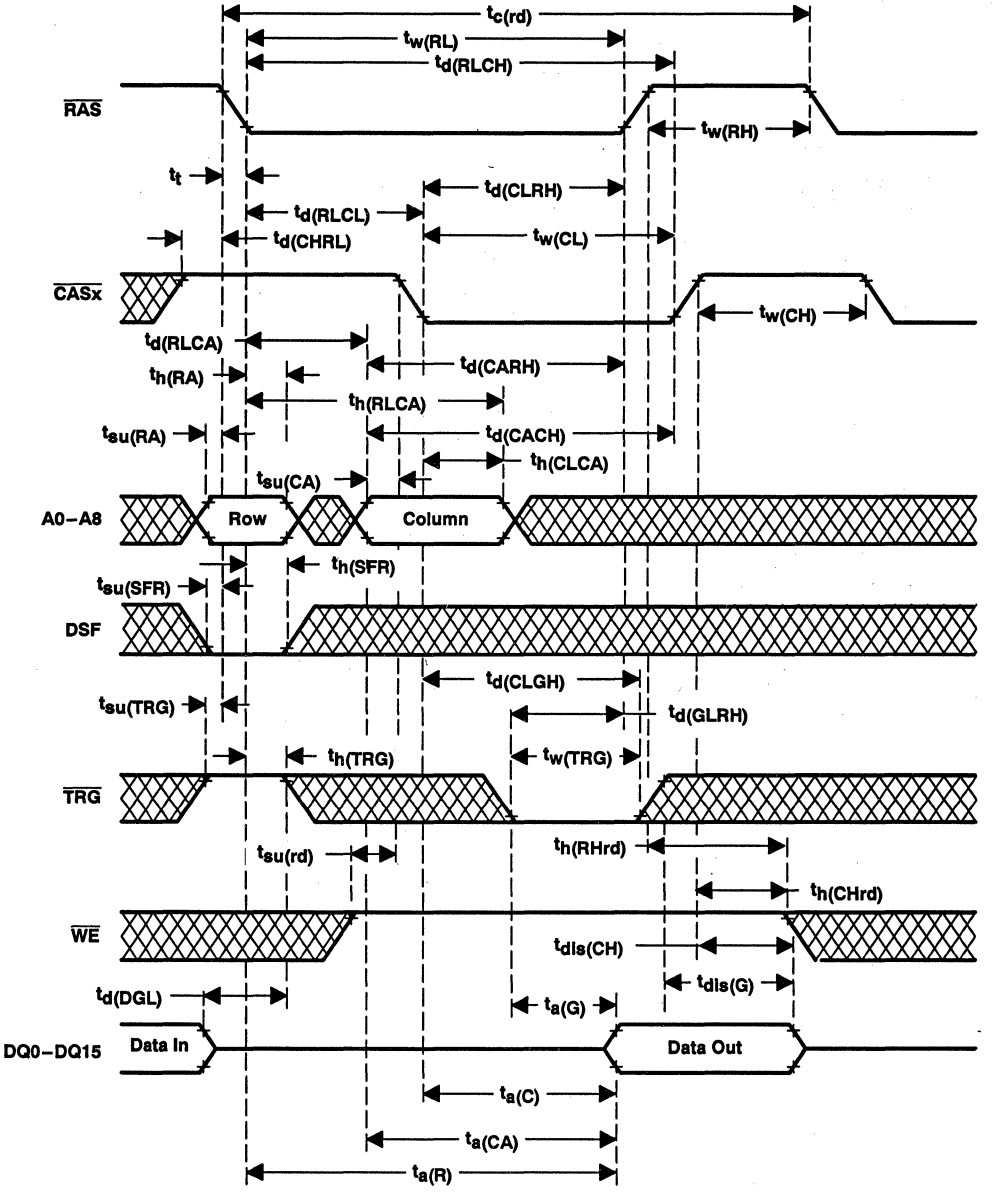


Figure 27. Read-Cycle Timing With $\overline{\text{CASx}}$-Controlled Output

PARAMETER MEASUREMENT INFORMATION

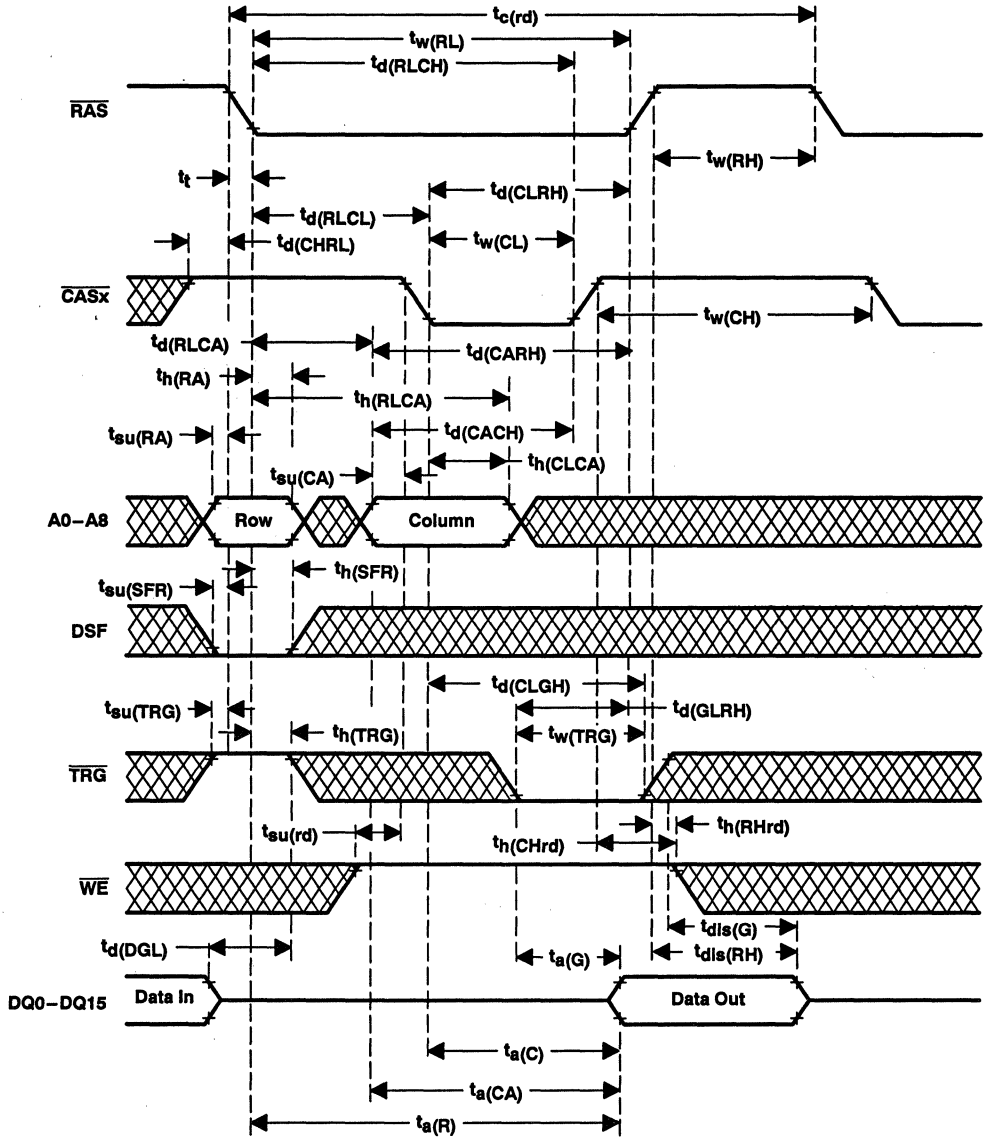


Figure 28. Read-Cycle Timing With $\overline{RAS}$-Controlled Output

PARAMETER MEASUREMENT INFORMATION

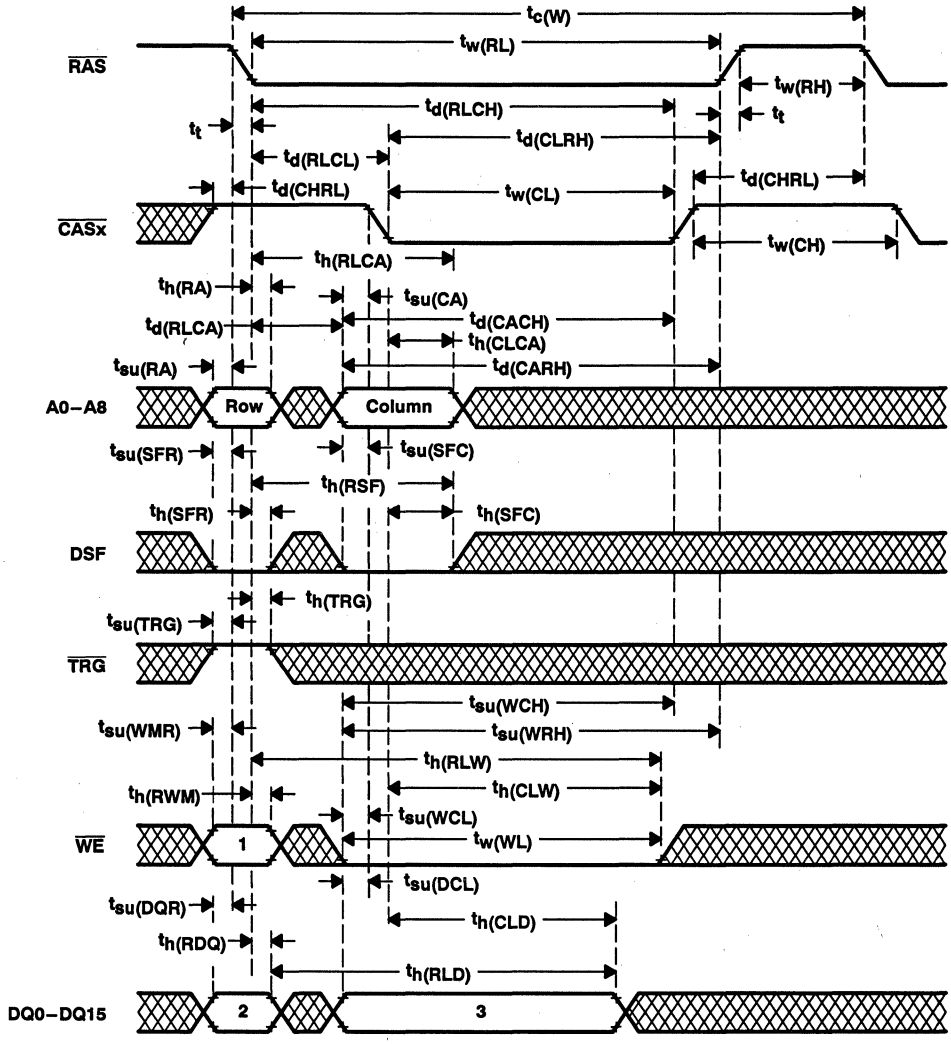


Figure 29. Early-Write-Cycle Timing

Table 4. Early-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

PARAMETER MEASUREMENT INFORMATION

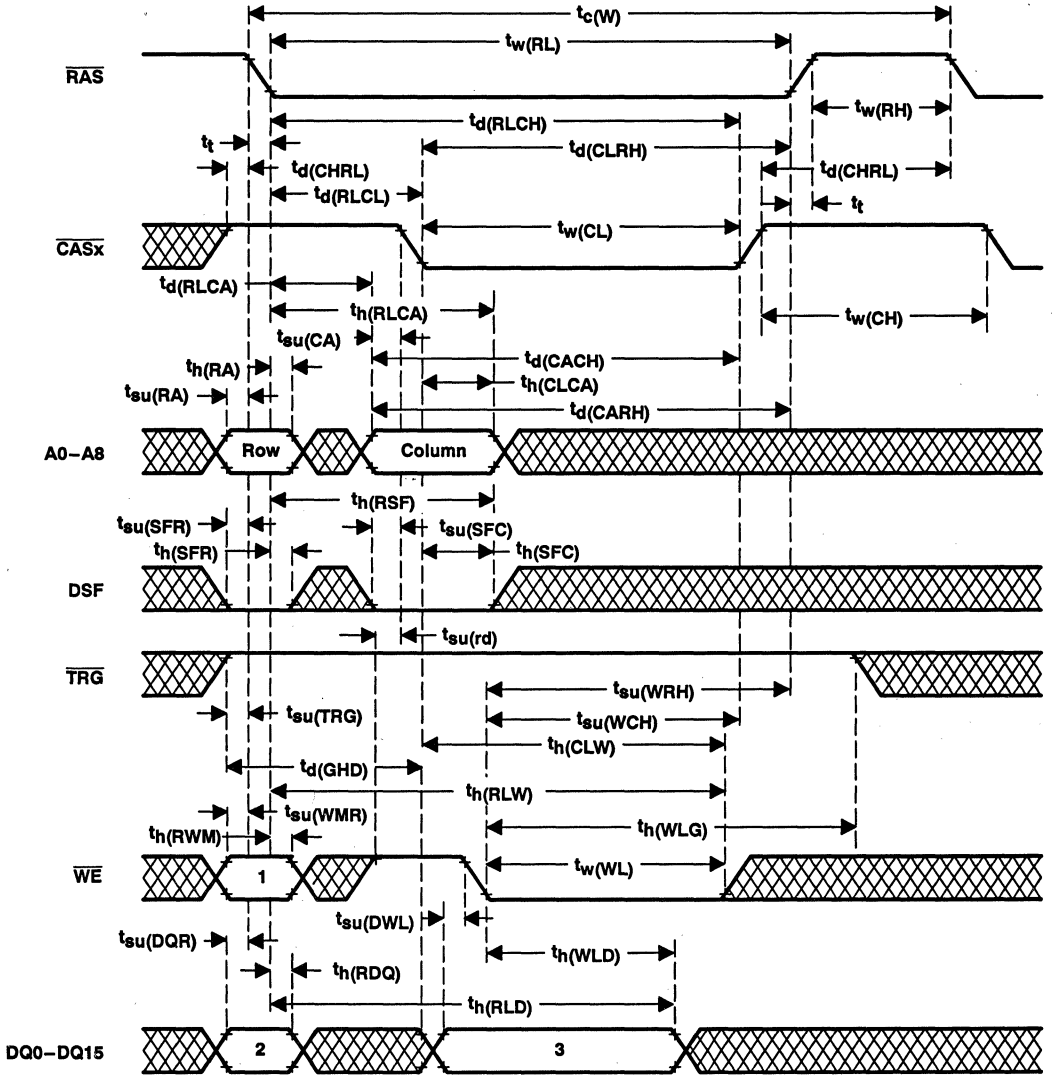
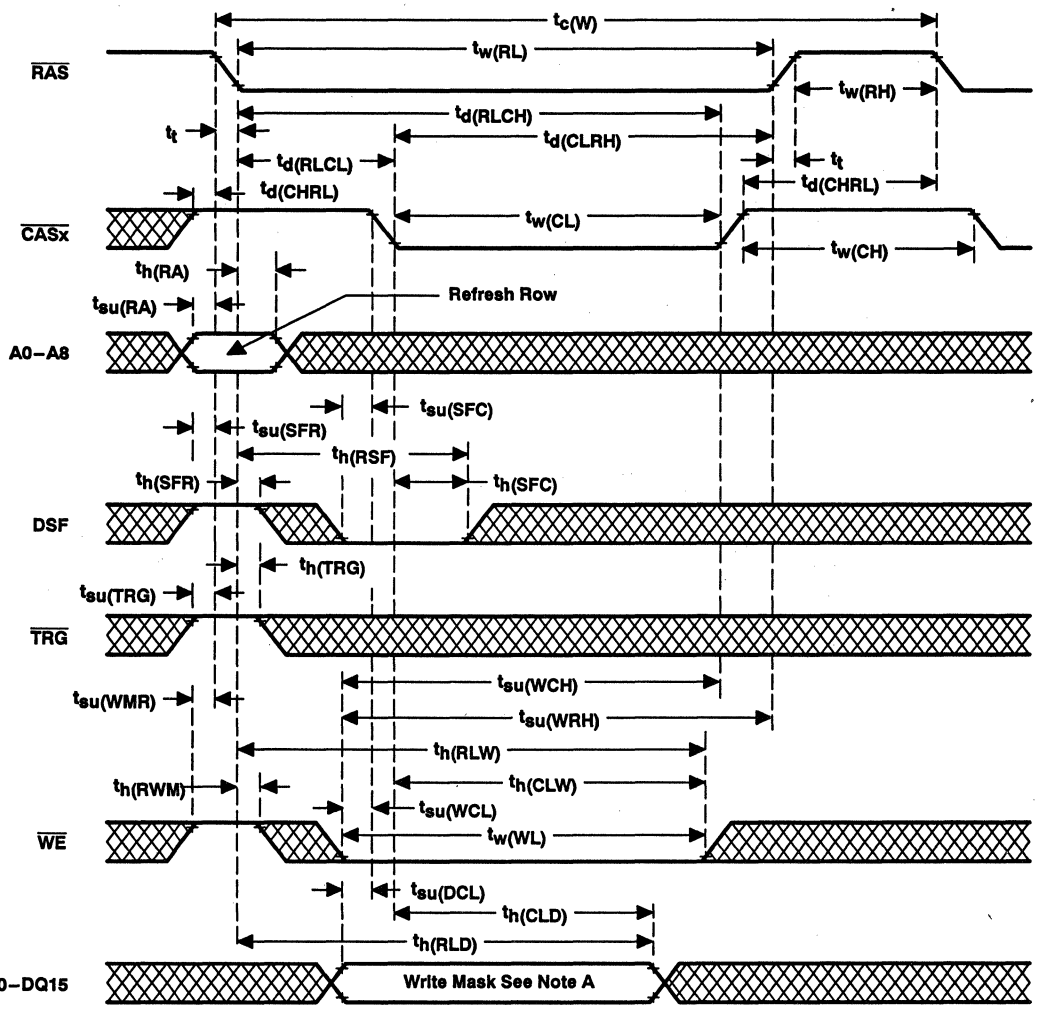


Figure 30. Late-Write-Cycle Timing (Output-Enable-Controlled Write)

Table 5. Late-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

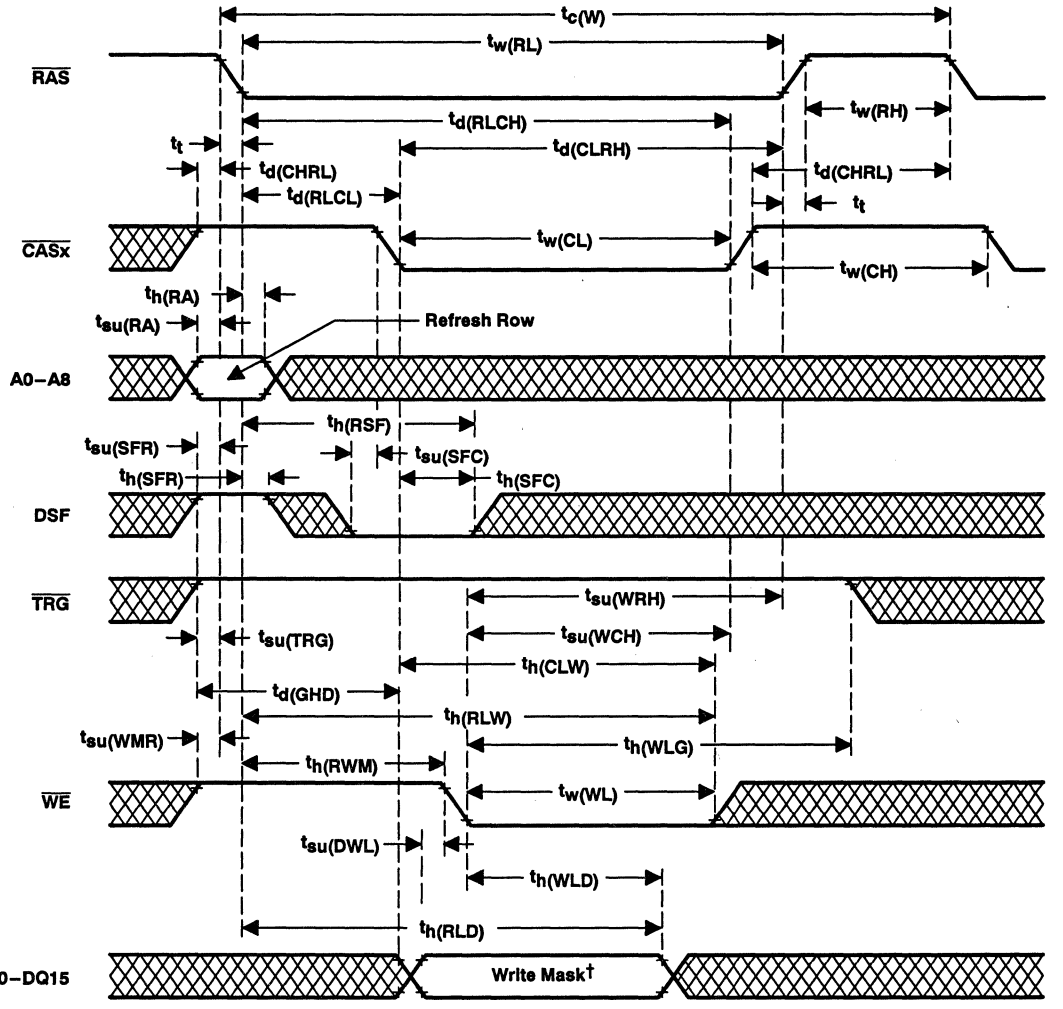
PARAMETER MEASUREMENT INFORMATION



† Load-write-mask-register cycle puts the device into the persistent write-per-bit mode.

Figure 31. Load-Write-Mask-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION



† Load-write-mask-register cycle puts the device into the persistent write-per-bit mode.

Figure 32. Load-Write-Mask-Register-Cycle Timing (Late-Write Load)

PARAMETER MEASUREMENT INFORMATION

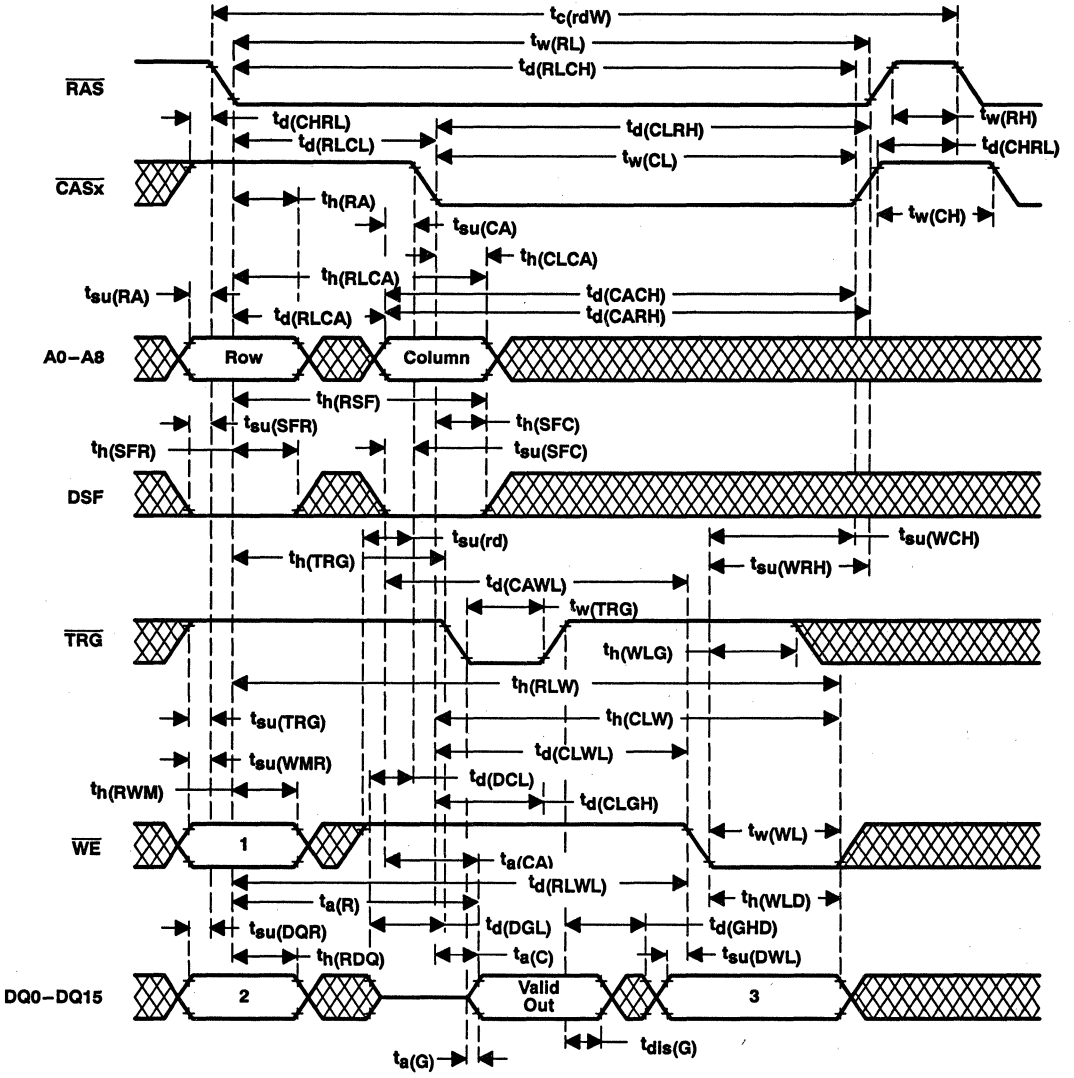
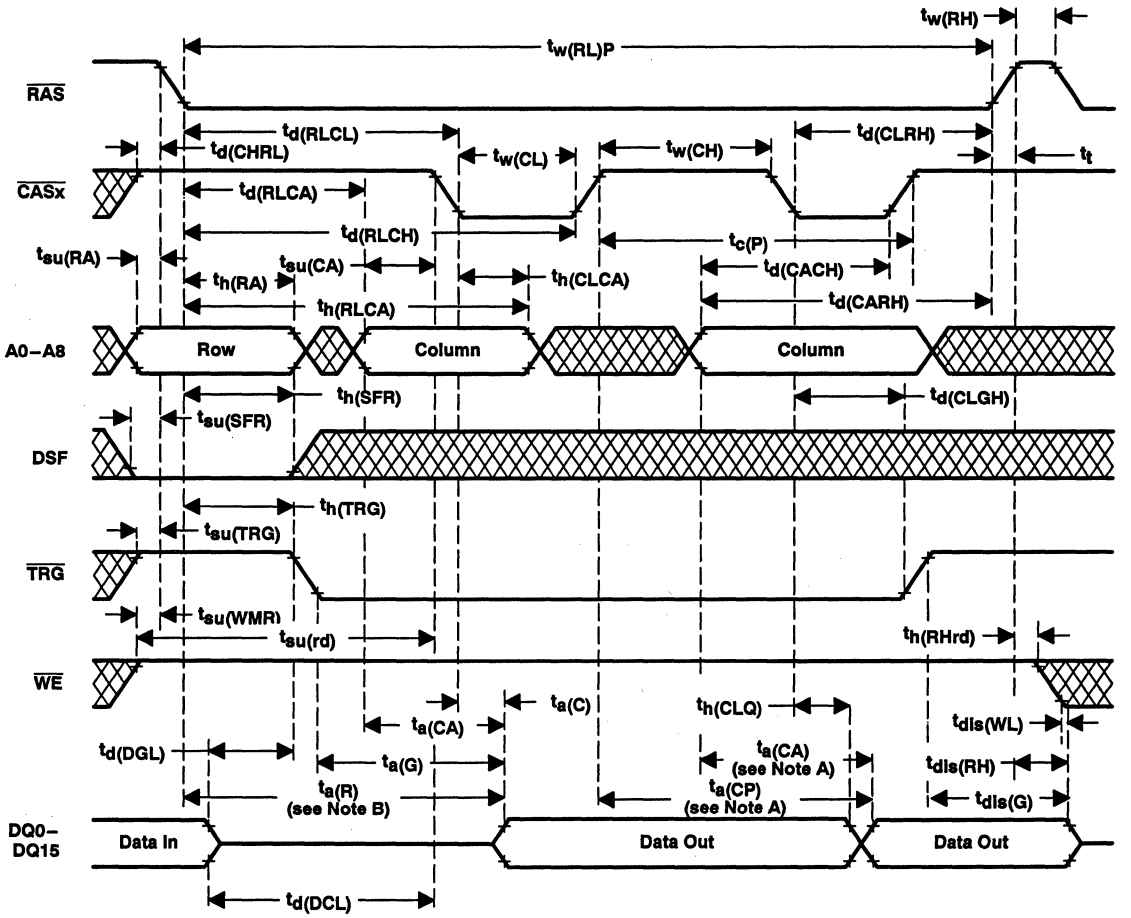


Figure 33. Read-Write-/Read-Modify-Write-Cycle Timing

Table 6. Read-Write-/Read-Modify-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

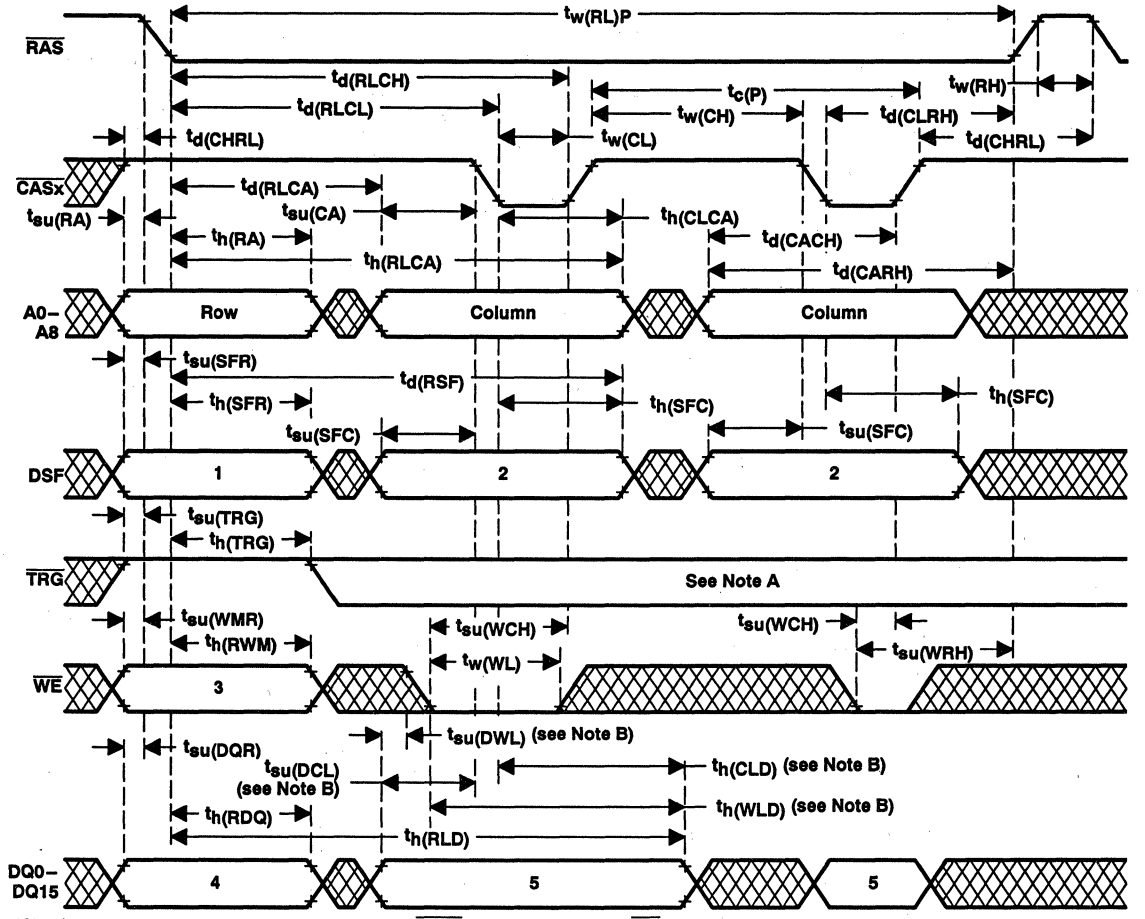
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
C. A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CASx}$ to select the desired write mode (normal, block write, etc.).

Figure 34. Enhanced-Page-Mode Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later

B. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used. If the early write-cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

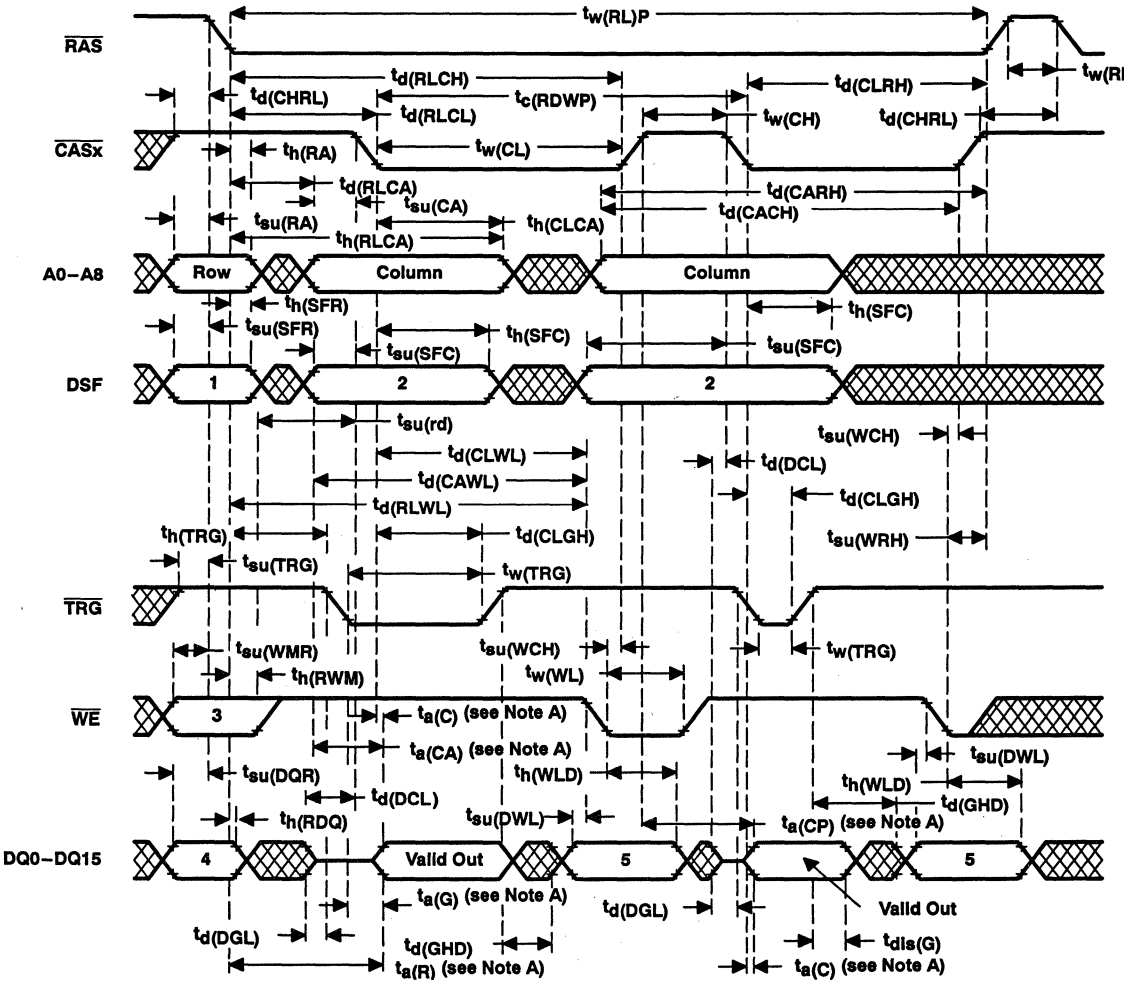
Figure 35. Enhanced-Page-Mode Write-Cycle Timing

Table 7. Enhanced-Page-Mode Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load-write mask on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.†	H	L	H	Don't care	Write mask

† Load-write-mask-register cycle puts the device in the persistent write-per-bit mode. Column address at the falling edge of $\overline{CASx}$ is a don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

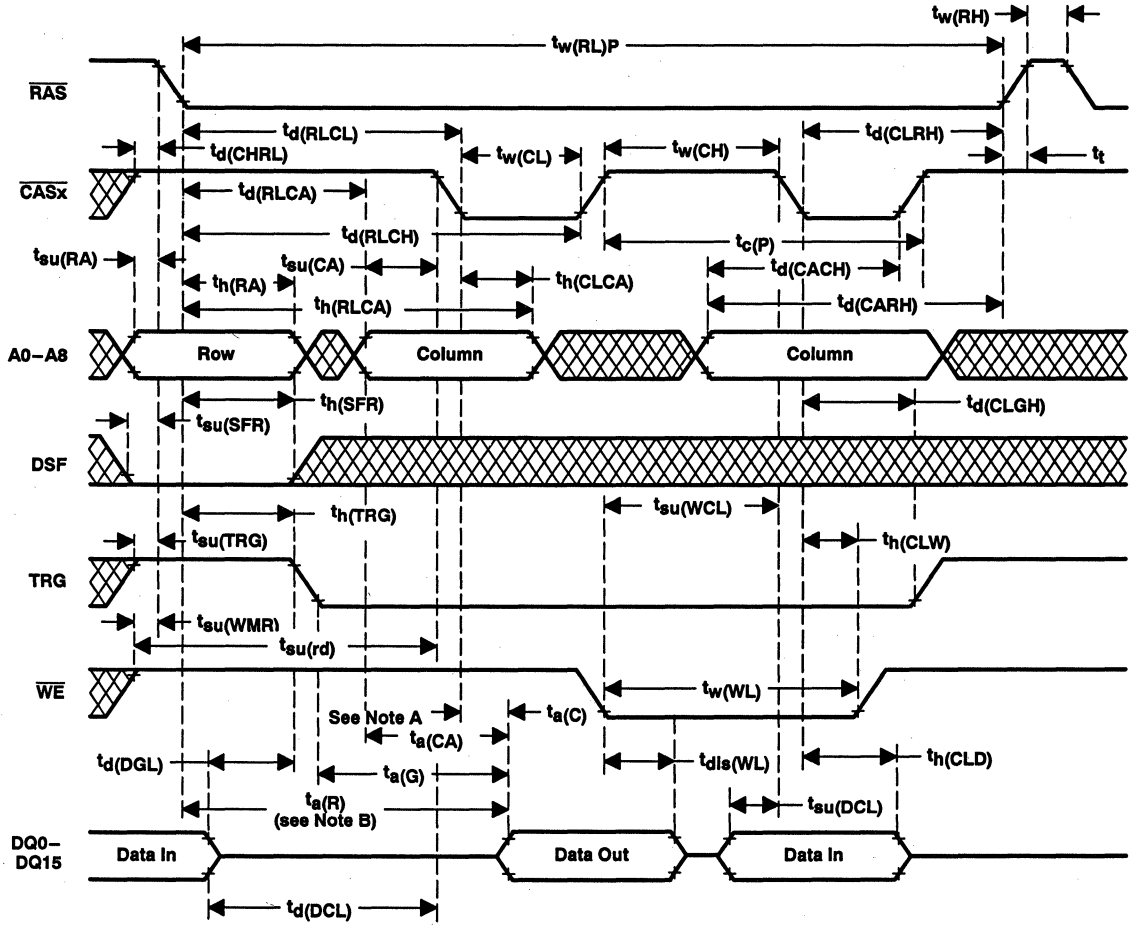
Figure 36. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

Table 8. Enhanced-Page-Mode Read-Modify-Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load write-mask register on either the first falling edge of CASx or the falling edge of WE, whichever occurs later.†	H	L	H	Don't care	Write mask

† Load-write-mask-register cycle puts the device in the persistent write-per-bit mode. Column address at the falling edge of CASx is a don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CASx}$ to select the desired write mode (normal, block write, etc.).

Figure 37. Enhanced-Page-Mode Read-/Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

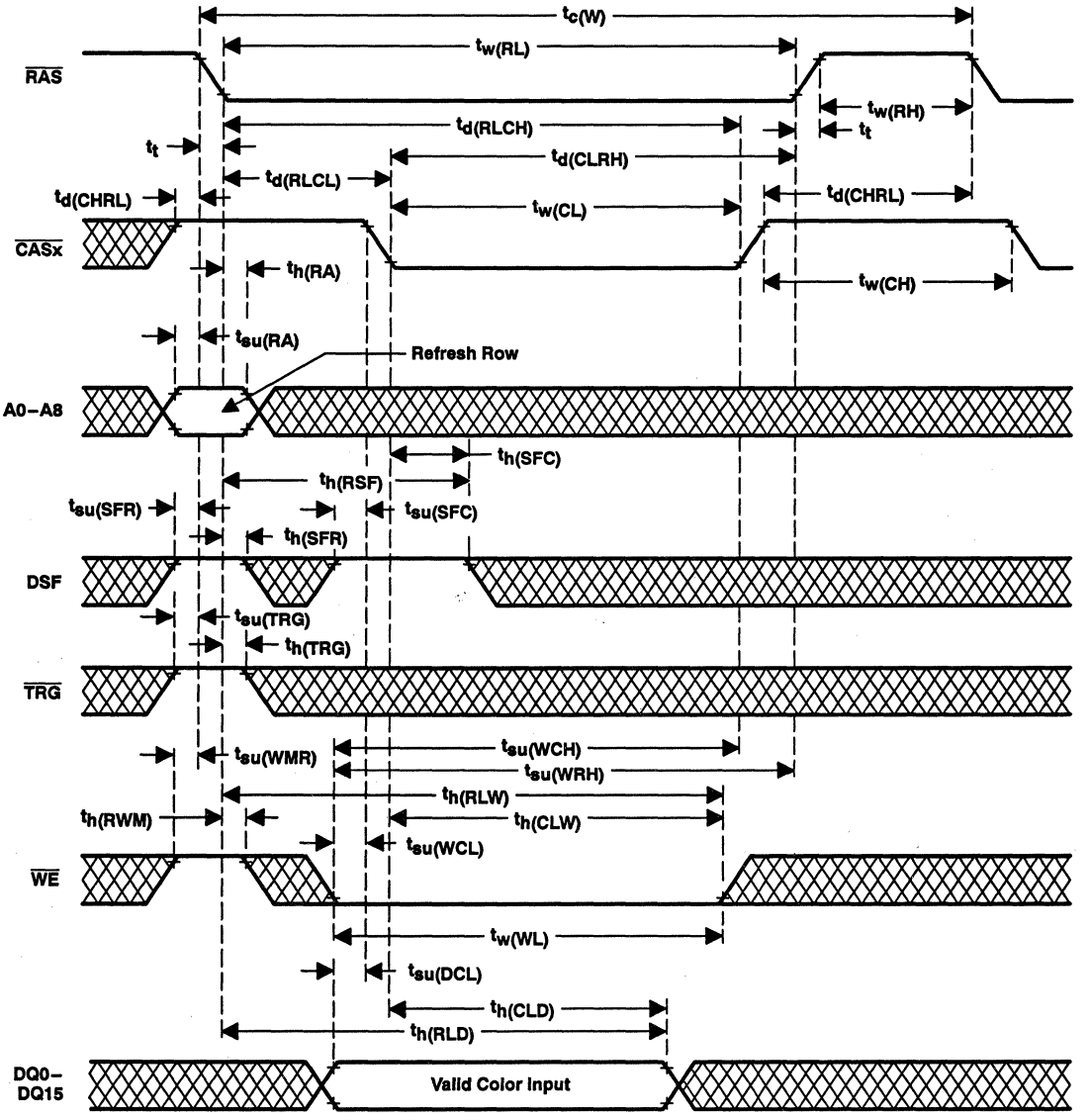


Figure 38. Load-Color-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION

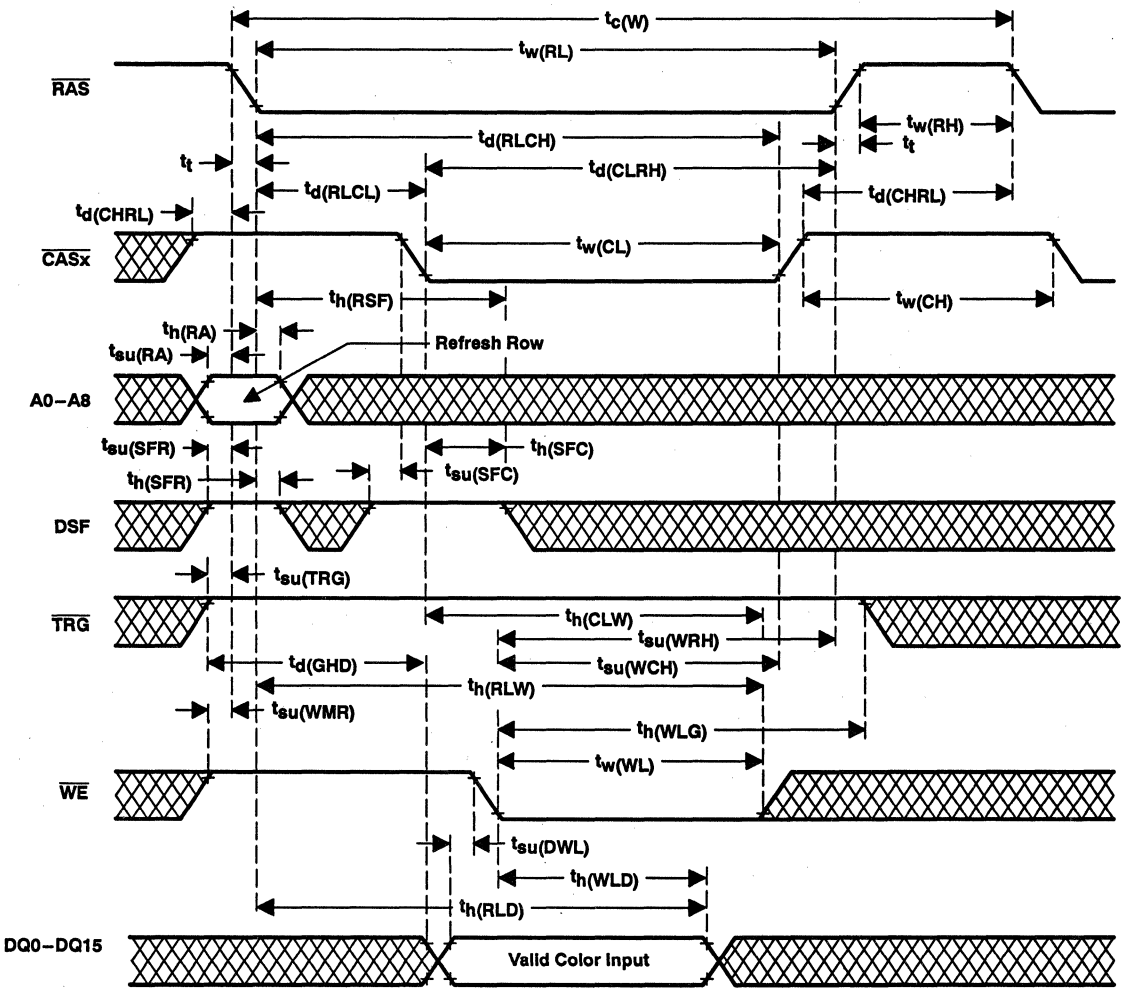


Figure 39. Load-Color-Register-Cycle Timing (Late-Write Load)

PARAMETER MEASUREMENT INFORMATION

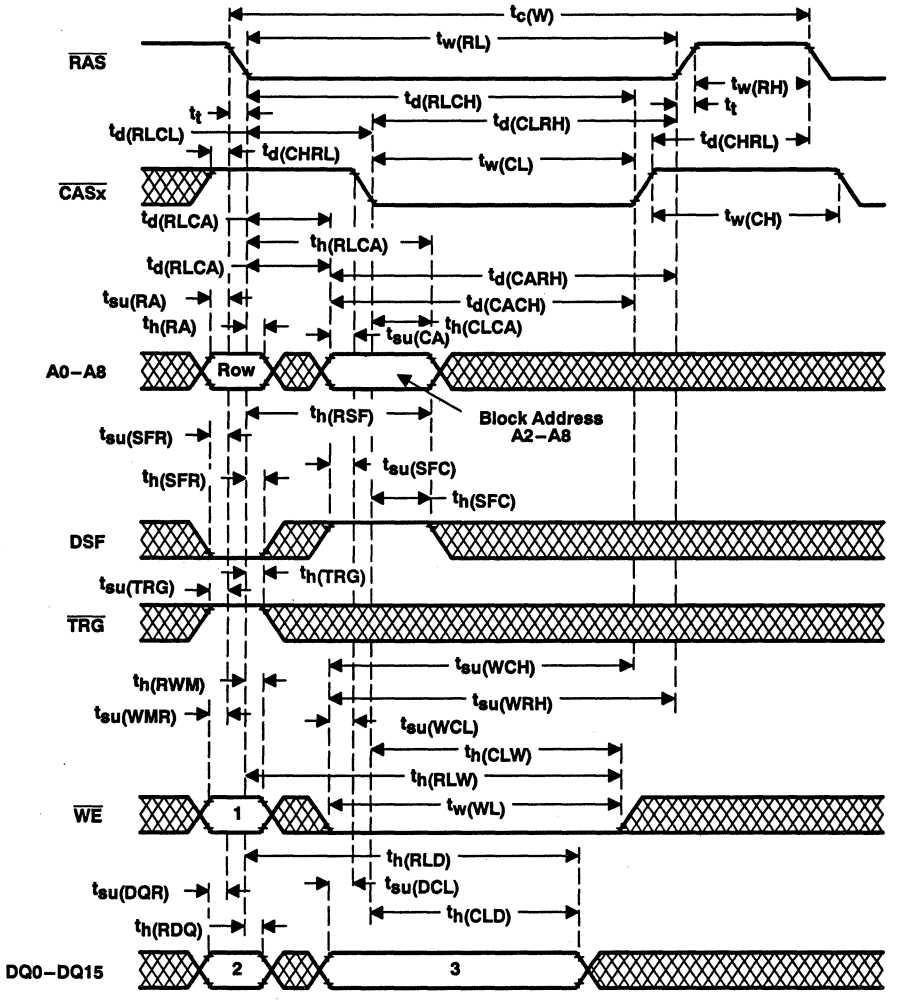


Figure 40. Block-Write-Cycle Timing (Early Write)

Table 9. Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable
Column-mask data DQi – DQi + 3 (i = 0, 4, 8, 12) 0: column-write disable
1: column-write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

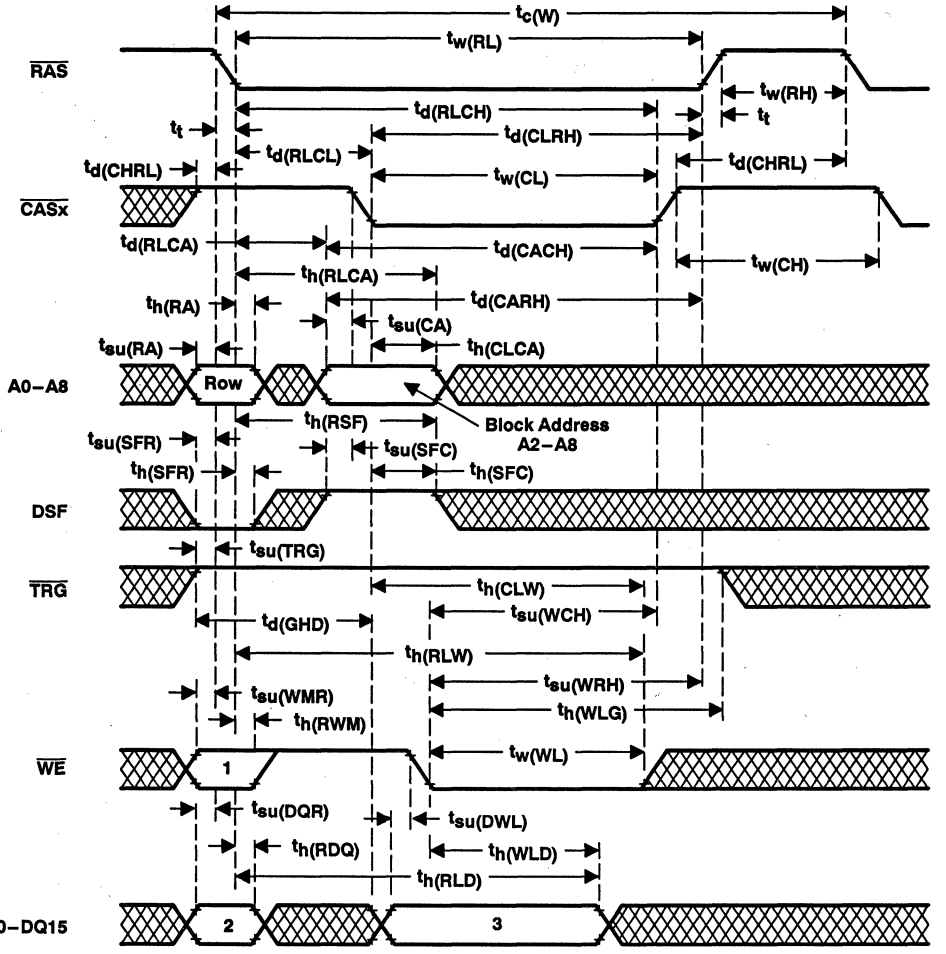


Figure 41. Block-Write-Cycle Timing (Late Write)

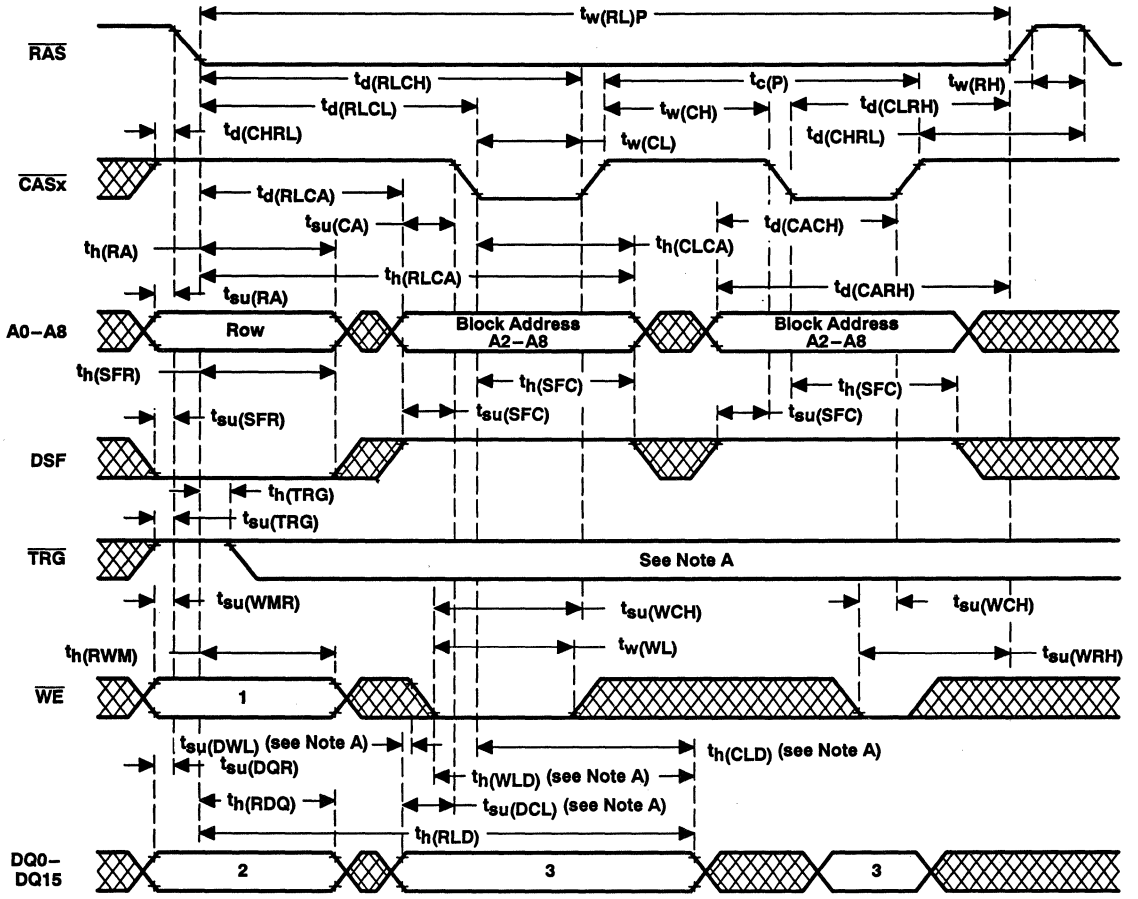
Table 10. Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable
Column-mask data DQi – DQi + 3 (i = 0, 4, 8, 12) 0: column-write disable
1: column-write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later

B. To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late-write feature is used. If the early-write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 42. Enhanced-Page-Mode Block-Write-Cycle Timing

Table 11. Enhanced-Page-Mode Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi + 3 (i = 0, 4, 8, 12) 0: column-write disable
1: column-write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

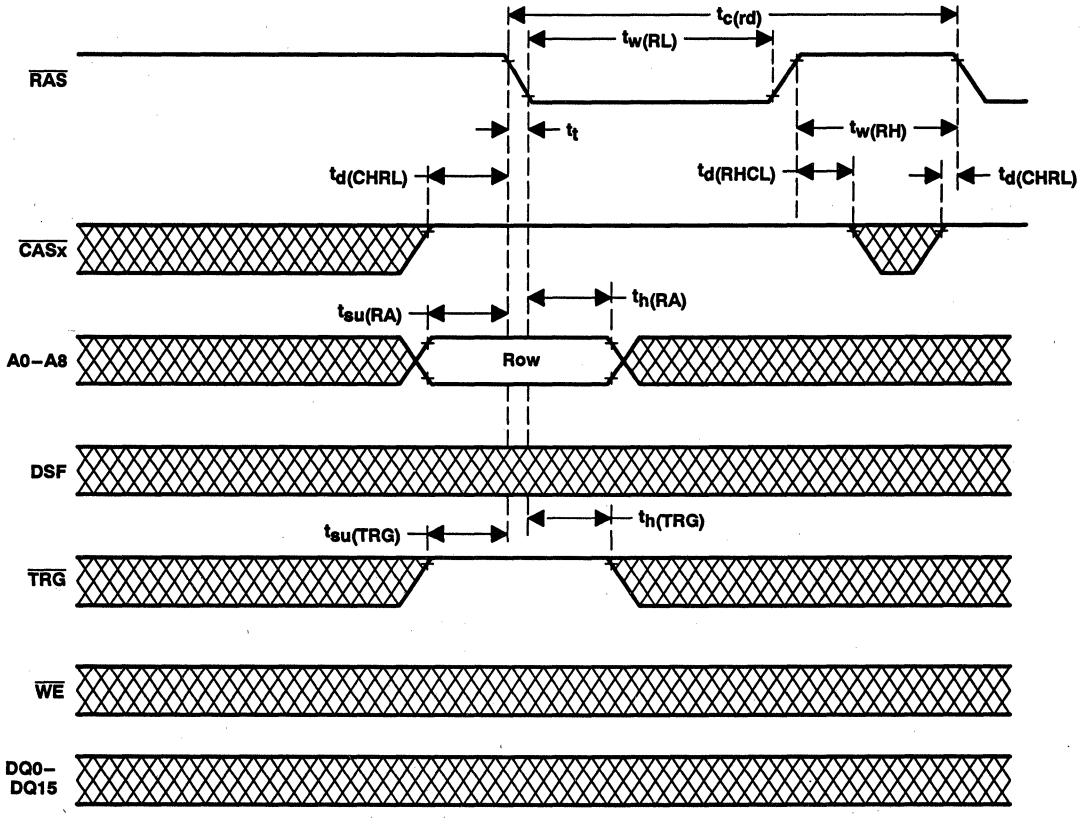


Figure 43. $\overline{\text{RAS}}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

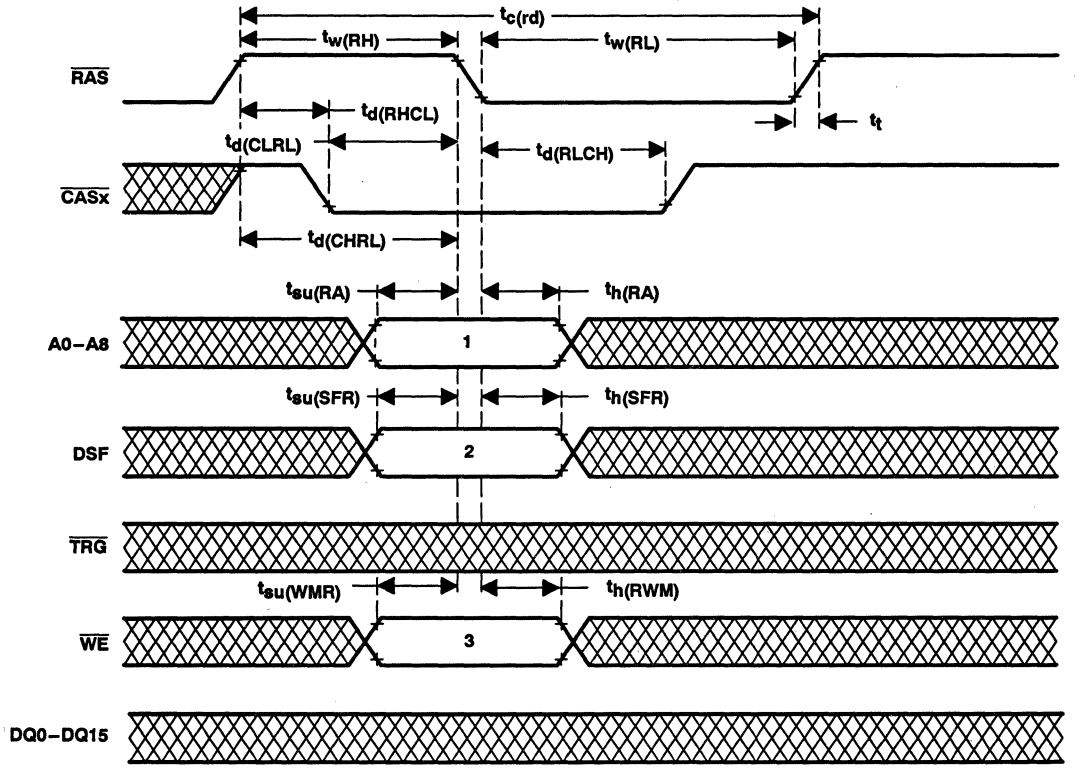


Figure 44. CBR-Refresh-Cycle Timing

Table 12. CBR-Cycle State Table

CYCLE	STATE		
	1	2	3
CBR refresh with option reset	Don't care	L	H
CBR refresh with no reset	Don't care	H	H
CBR refresh with stop-point set and no reset	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION

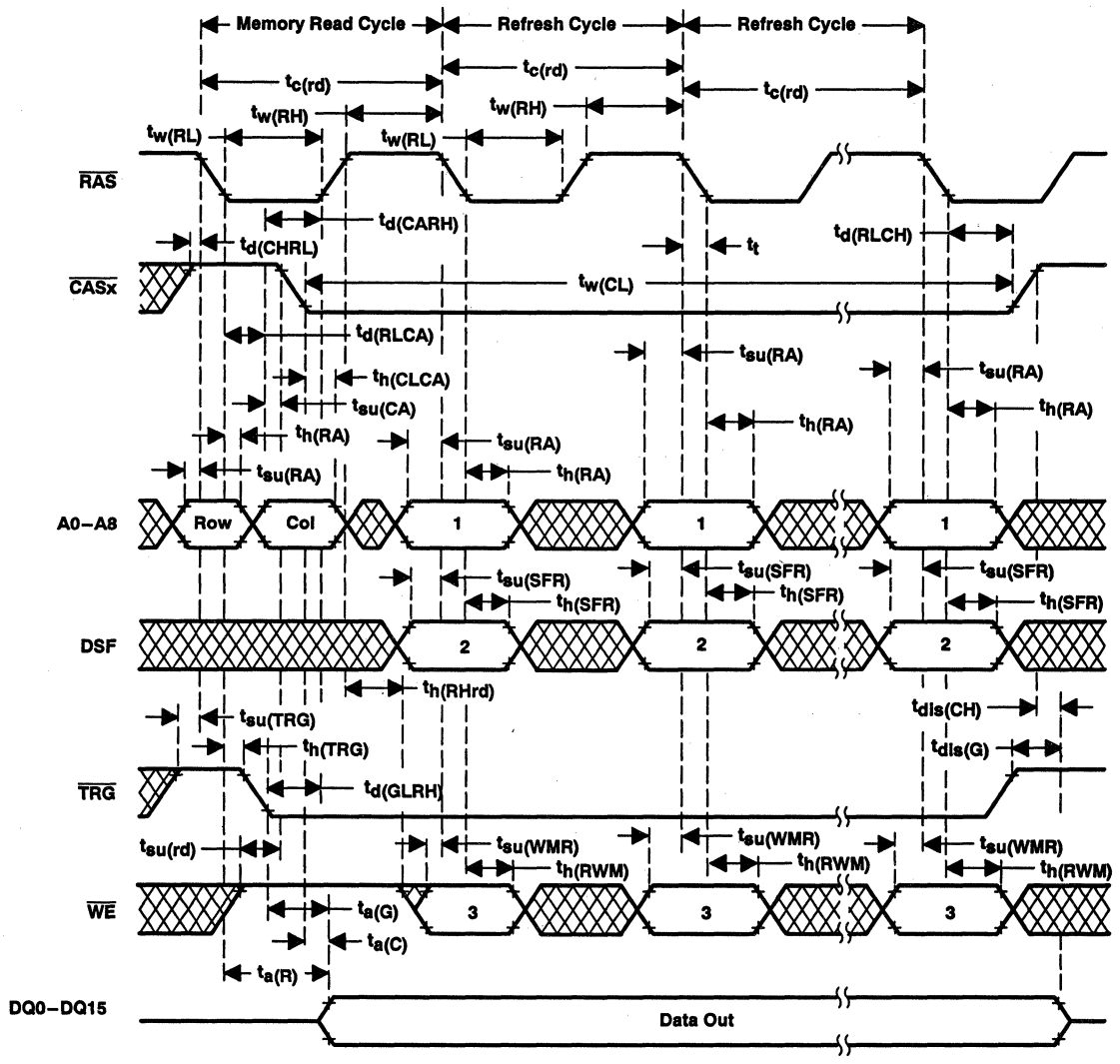
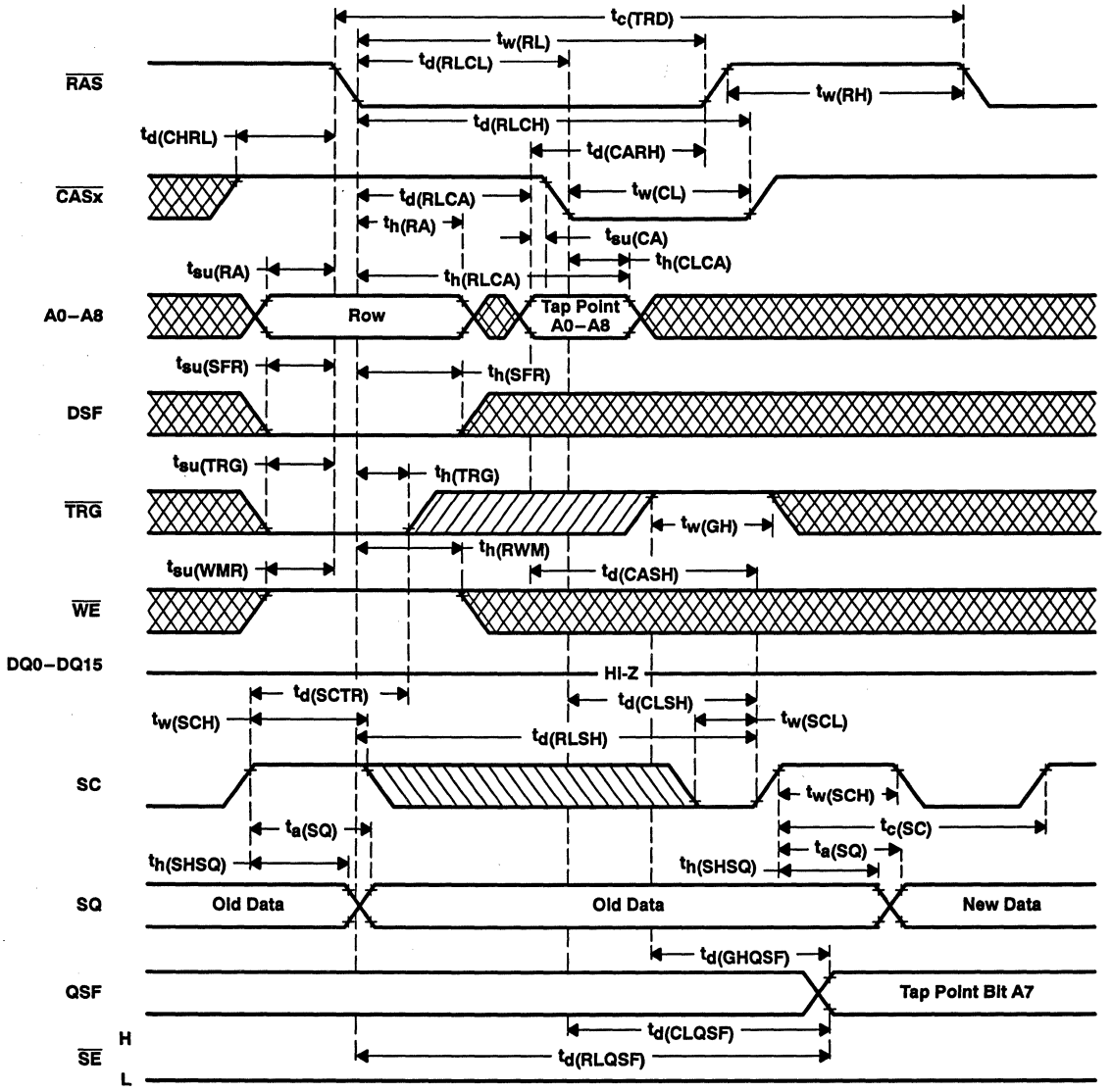


Figure 45. Hidden-Refresh-Cycle Timing

Table 13. Hidden-Refresh-Cycle State Table

CYCLE	STATE		
	1	2	3
CBR refresh with option reset	Don't care	L	H
CBR refresh with no reset	Don't care	H	H
CBR refresh with stop-point set and no option reset	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

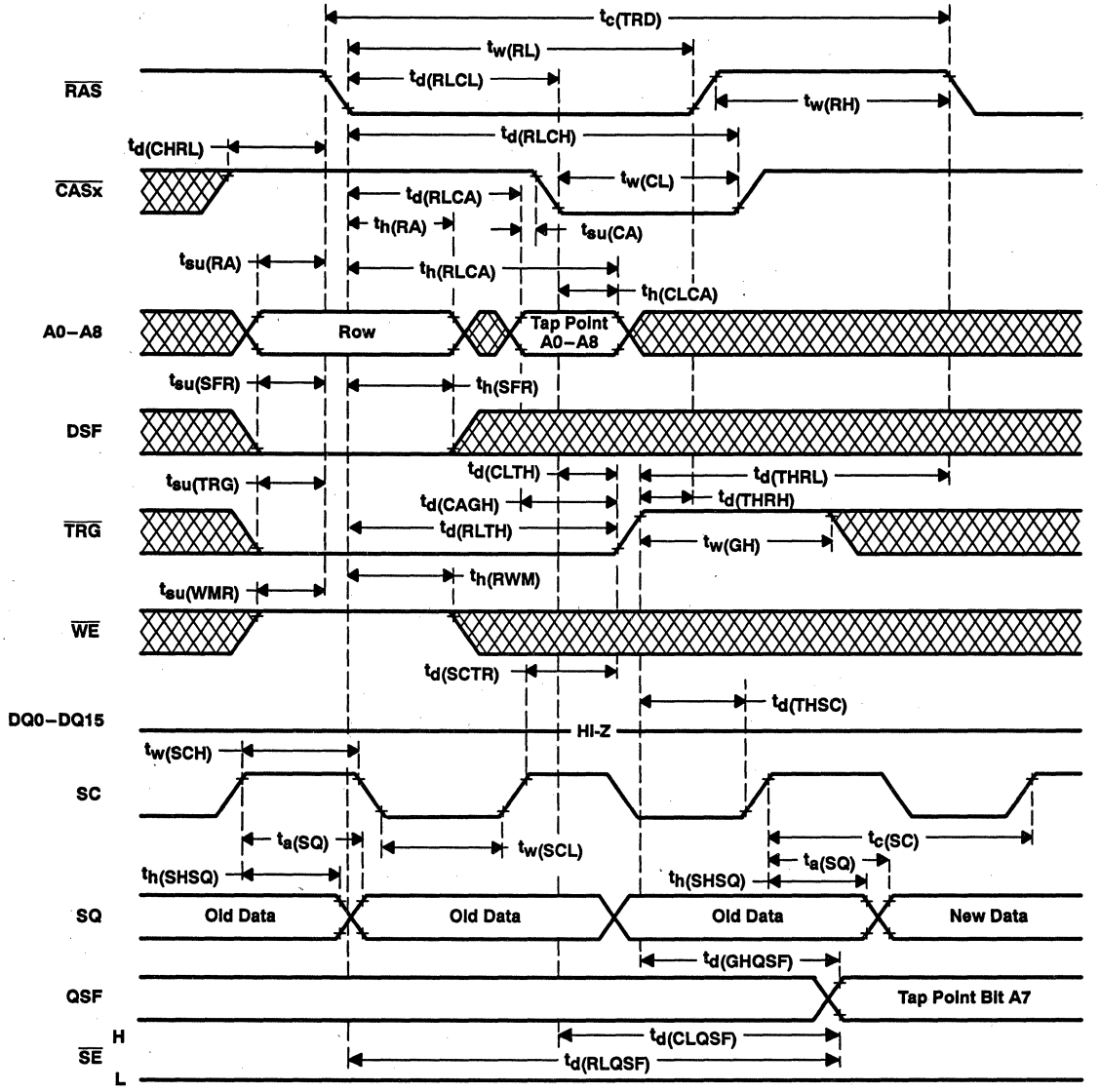
B. Once data is transferred into the data registers, the SAM is in the serial-read mode (i.e., the SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0 – A7: register tap point; A8: identifies the DRAM row half

D. Early-load operation is defined as $t_{h(TRG)}$ min < $t_{h(TRG)}$ < $t_{d(RLTH)}$ min.

Figure 46. Full-Register Transfer-Read Timing, Early-Load Operations

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

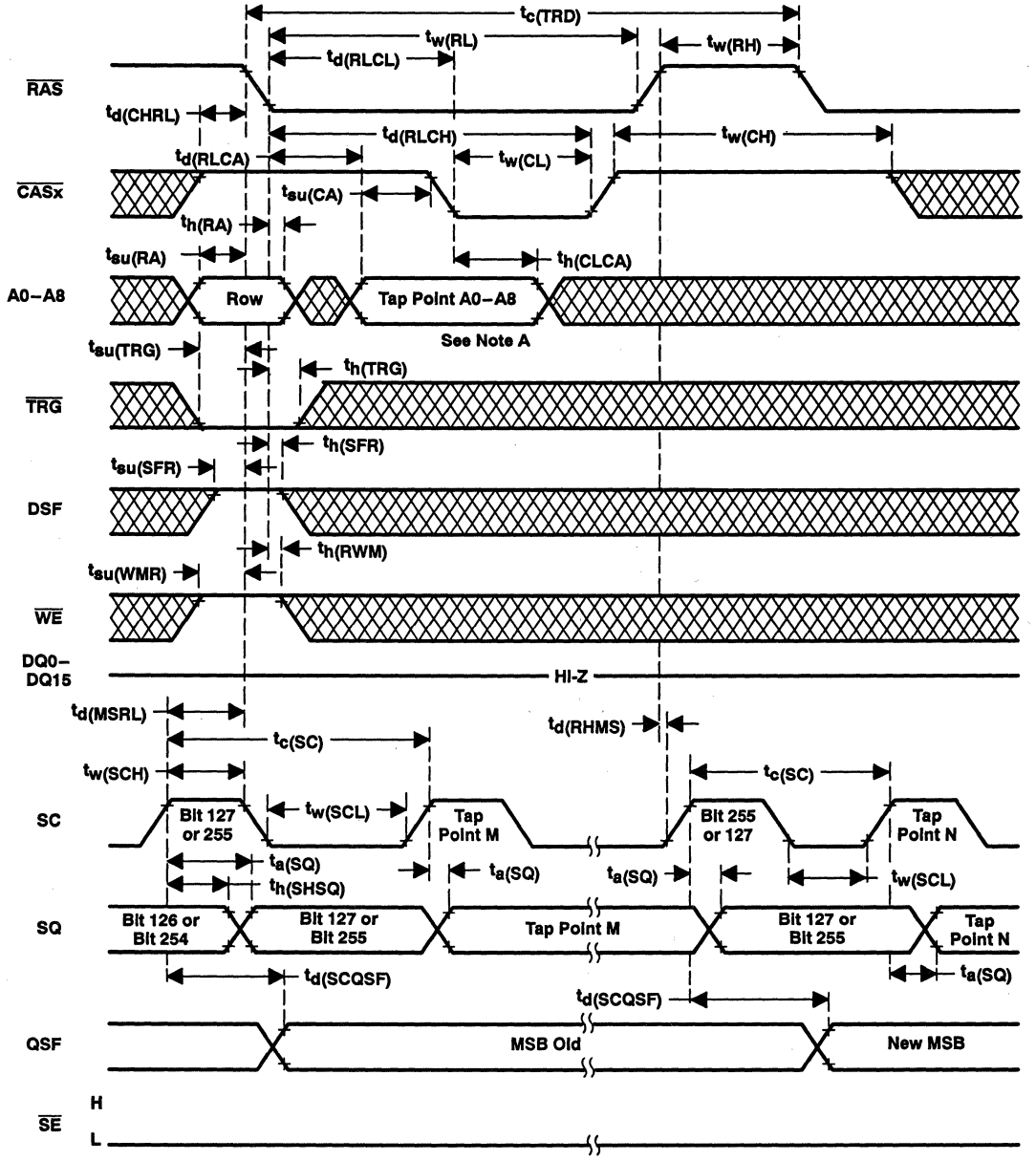
B. Once data is transferred into the data registers, the SAM is in the serial-read mode (i.e., the SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0–A7: register tap point; A8: identifies the DRAM row half

D. Late load operation is defined as $t_{d(THRH)} < 0$ ns.

Figure 47. Full-Register Transfer Read-Timing, Real-Time Load Operation/Late-Load Operation

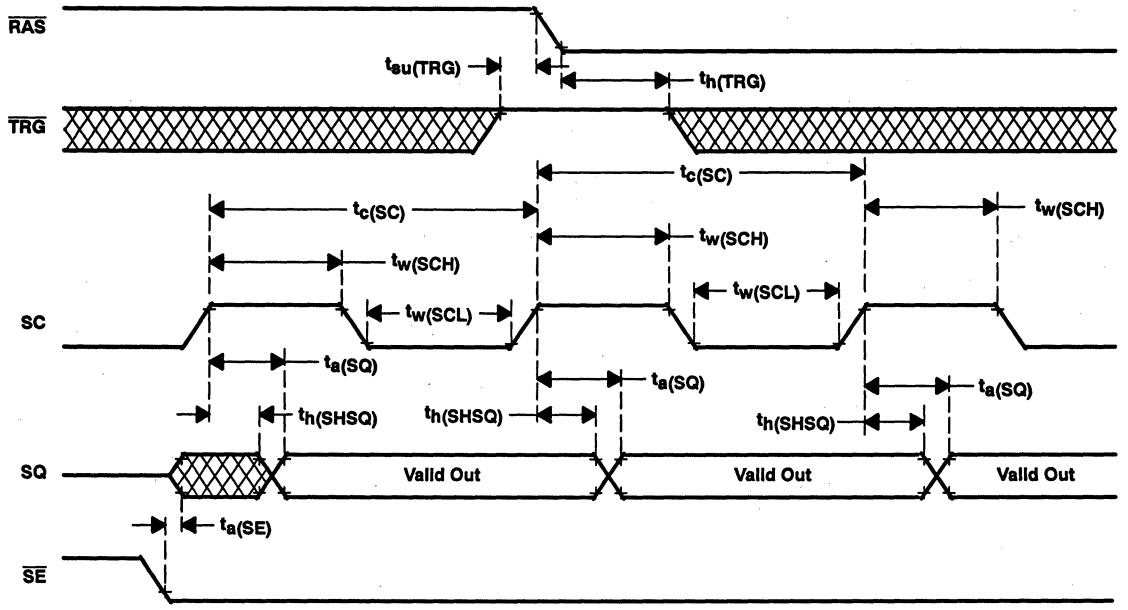
PARAMETER MEASUREMENT INFORMATION



NOTE A: A0–A6: tap point of the given half; A7: don't care; A8: identifies the DRAM row half

Figure 48. Split-Register-Transfer-Read Timing

PARAMETER MEASUREMENT INFORMATION

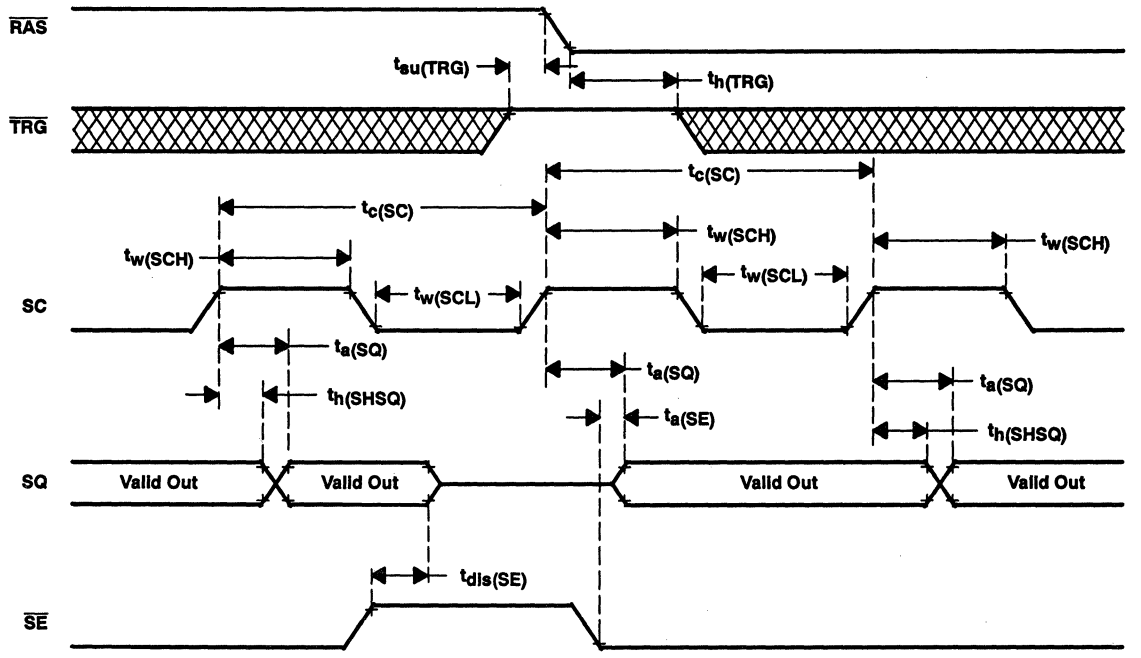


NOTES: A. While the data is being read through the serial-data register, $\overline{TRG}$ is a don't care; however $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

B. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer-read cycle.

Figure 49. Serial-Read-Cycle Timing ($\overline{SE}$ = V_{IL})

PARAMETER MEASUREMENT INFORMATION

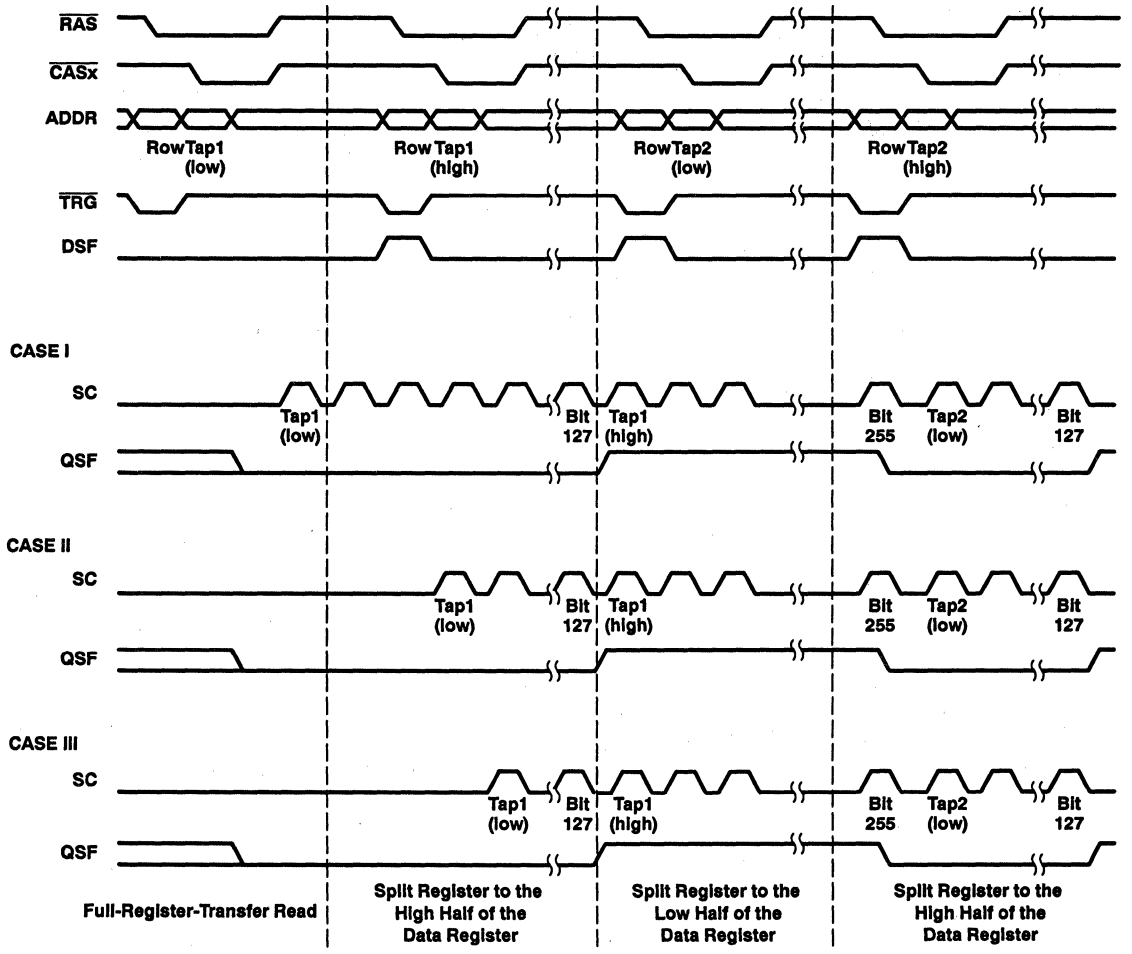


NOTES: A. While the data is being read through the serial-data register, $\overline{TRG}$ is a don't care; however $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

B. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer-read cycle.

Figure 50. Serial-Read Timing ($\overline{SE}$-Controlled Read)

PARAMETER MEASUREMENT INFORMATION

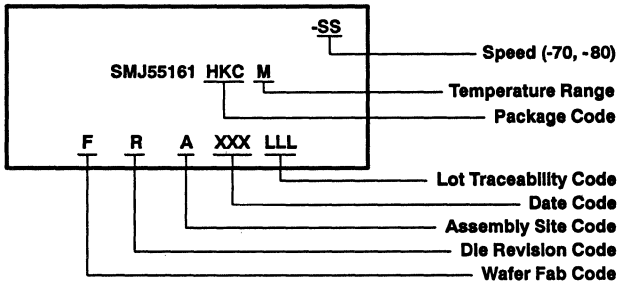


NOTES: A. To achieve proper split-register operation, a full-register-transfer read must be performed before the first split-register-transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can begin either after the full-register-transfer read cycle (CASE I), during the first split-register-transfer cycle (CASE II), or even after the first split-register-transfer cycle (CASE III). There is no minimum requirement of SC clock between the full-register transfer-read cycle and the first split-register cycle.

B. A split-register transfer into the inactive half is not allowed until $t_{d(MSRL)}$ is met. $t_{d(MSRL)}$ is the minimum delay time between the rising edge of the serial clock of the last bit (bit 127 or 255) and the falling edge of $\overline{RAS}$ of the split-register-transfer cycle into the inactive half. After the $t_{d(MSRL)}$ requirement is met, the split-register transfer into the inactive half must also satisfy the minimum $t_{d(RHMS)}$ requirement. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register-transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 127 or 255).

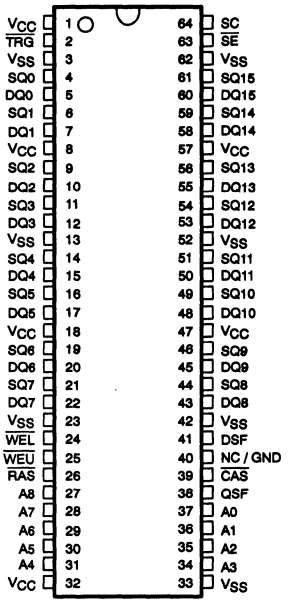
Figure 51. Split-Register Operating Sequence

device symbolization



- **Organization:**
  - **DRAM: 262144 Words × 16 Bits**
  - **SAM: 256 Words × 16 Bits**
- **Dual-Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Data-Transfer Function From the DRAM to the Serial-Data Register**
- **(4 × 4) × 4 Block-Write Feature for Fast Area-Fill Operations; As Many as Four Memory-Address Locations Written Per Cycle From the 16-Bit On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O; Two Write-Per-Bit Modes to Simplify System Design**
- **Byte Write Control ($\overline{WEL}$, $\overline{WEU}$) Provides Flexibility**
- **Extended Data Output for Faster System Cycle Time**
- **Enhanced Page-Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) and Hidden-Refresh Modes**
- **Long Refresh Period**
  Every 8 ms (Max)
- **Up to 45-MHz Uninterrupted Serial-Data Streams**
- **256 Selectable Serial-Register Starting Locations**
- **$\overline{SE}$-Controlled Register-Status QSF**
- **Split-Register-Transfer Read for Simplified Real-Time Register Load**
- **Programmable Split-Register Stop Point**
- **3-State Serial Outputs Allow Easy Multiplexing of Video-Data Streams**
- **All Inputs/Outputs and Clocks TTL Compatible**
- **Compatible With JEDEC Standards**
- **Texas Instruments EPIC™ CMOS Process**
- **Designed to Work With the Texas Instruments Graphics Family**
- **Performance Ranges:**

HKC PACKAGE
(TOP VIEW)



PIN NOMENCLATURE

A0–A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ15	DRAM Data I/O, Write Mask Data
DSF	Special-Function Select
NC/GND	No Connect/Ground (Important: Not connected internally to V_{SS})
QSF	Special-Function Output
$\overline{RAS}$	Row-Address Strobe
SC	Serial Clock
$\overline{SE}$	Serial Enable
SQ0–SQ15	Serial-Data Output
$\overline{TRG}$	Output Enable, Transfer Select
V_{CC}	5-V Supply (TYP)
V_{SS}	Ground
$\overline{WEL}$, $\overline{WEU}$	DRAM Byte-Write-Enable Selects

	ACCESS TIME ROW ENABLE $t_{a(R)}$ (MAX)	ACCESS TIME SERIAL DATA $t_{a(SQ)}$ (MAX)	DRAM CYCLE TIME $t_{c(W)}$ (MIN)	DRAM PAGE MODE $t_{c(P)}$ (MIN)	SERIAL CYCLE TIME $t_{c(SC)}$ (MIN)	OPERATING CURRENT SERIAL PORT STANDBY I_{CC1} (MAX)	OPERATING CURRENT SERIAL PORT ACTIVE I_{CC1A} (MAX)
SMJ55166-70	70 ns	20 ns	130 ns	45 ns	22 ns	165 mA	210 mA
SMJ55166-80	80 ns	25 ns	150 ns	50 ns	30 ns	160 mA	195 mA

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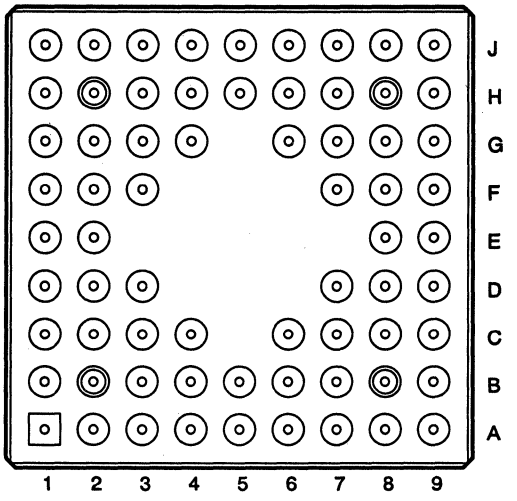
GB PACKAGE
(BOTTOM VIEW)



GB Package Pin Assignments — By Location

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
J1	DQ1	J2	SQ3	J3	DQ3	J4	DQ4	J5	DQ5	J6	DQ6	J7	SQ7	J8	$\overline{WEL}$	J9	A8
H1	DQ0	H2	SQ2	H3	DQ2	H4	SQ4	H5	SQ5	H6	SQ6	H7	DQ7	H8	$\overline{WEU}$	H9	A7
G1	SQ0	G2	SQ1	G3	V_{DD2}	G4	V_{SS2}			G6	V_{DD2}	G7	V_{SS2}	G8	$\overline{RAS}$	G9	A6
F1	$\overline{TRG}$	F2	V_{SS1}	F3	V_{DD1}							F7	V_{DD1}	F8	V_{DD1}	F9	A5
E1	SC	E2	V_{DD1}											E8	V_{SS1}	E9	A4
D1	$\overline{SE}$	D2	V_{SS1}	D3	V_{DD1}							D7	V_{SS1}	D8	A3	D9	A2
C1	SQ15	C2	V_{SS1}	C3	V_{DD2}	C4	V_{SS2}			C6	V_{DD2}	C7	V_{SS2}	C8	$\overline{CAS}$	C9	A1
B1	DQ15	B2	DQ14	B3	DQ13	B4	DQ12	B5	DQ11	B6	DQ10	B7	SQ8	B8	DSF	B9	A0
A1	SQ14	A2	SQ13	A3	SQ12	A4	SQ11	A5	SQ10	A6	SQ9	A7	DQ9	A8	DQ8	A9	QSF

GB Package Pin Assignments — By Signals

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
A0	B9	DQ2	H3	DQ13	B3	SQ3	J2	SQ14	A1	V_{DD2}	C6
A1	C9	DQ3	J3	DQ14	B2	SQ4	H4	SQ15	C1	V_{SS1}	F2
A2	D9	DQ4	J4	DQ15	B1	SQ5	H5	$\overline{TRG}$	F1	V_{SS1}	D2
A3	D8	DQ5	J5	DSF	B8	SQ6	H6	V_{DD1}	E2	V_{SS1}	C2
A4	E9	DQ6	J6	QSF	A9	SQ7	J7	V_{DD1}	F3	V_{SS1}	D7
A5	F9	DQ7	H7	$\overline{RAS}$	G8	SQ8	B7	V_{DD1}	D3	V_{SS1}	E8
A6	G9	DQ8	A8	SC	E1	SQ9	A6	V_{DD1}	F7	V_{SS2}	G4
A7	H9	DQ9	A7	$\overline{SE}$	D1	SQ10	A5	V_{DD1}	F8	V_{SS2}	C4
A8	J9	DQ10	B6	SQ0	G1	SQ11	A4	V_{DD2}	G3	V_{SS2}	G7
$\overline{CAS}$	C8	DQ11	B5	SQ1	G2	SQ12	A3	V_{DD2}	C3	V_{SS2}	C7
DQ0	H1	DQ12	B4	SQ2	H2	SQ13	A2	V_{DD2}	G6	$\overline{WEL}$	J8
DQ1	J1									$\overline{WEU}$	H8

description

The SMJ55166 multiport video RAM is a high-speed dual-ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 16 bits each interfaced to a serial-data register [serial-access memory (SAM)] organized as 256 words of 16 bits each. The SMJ55166 supports three basic types of operation: random access to and from the DRAM, serial access from the serial register, and transfer of data from any row in the DRAM to the serial register. Except during transfer operations, the SMJ55166 can be accessed simultaneously and asynchronously from the DRAM and SAM ports.

The SMJ55166 is equipped with several features designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates are achieved by the device's (4 × 4) × 4 block-write feature. The block-write mode allows 16 bits of data (present in an on-chip color-data register) to be written to any combination of four adjacent column-address locations. As many as 64 bits of data can be written to memory during each $\overline{CAS}$ cycle time. Also on the DRAM port, a write mask or a write-per-bit feature allows masking of any combination of the 16 inputs/outputs on any write cycle. The persistent write-per-bit feature uses a mask register that, once loaded, can be used on subsequent write cycles without reloading. The SMJ55166 also offers byte control. Byte control can be applied in write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. The SMJ55166 also offers extended-data-output mode. The extended-data-output mode is effective in both the page-mode and standard DRAM cycles.

The SMJ55166 offers a split-register-transfer read (DRAM to SAM) feature for the serial register (SAM port). This feature enables real-time register load implementation for truly continuous serial-data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. For applications not requiring real-time register load (for example, loads done during CRT-retrace periods), the full-register mode of operation is retained to simplify system design.

The SAM port is designed for maximum performance. Data can be accessed from the SAM at serial rates up to 45 MHz. During the split-register-transfer read operations, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, QSF, is included to indicate which half of the serial register is active.

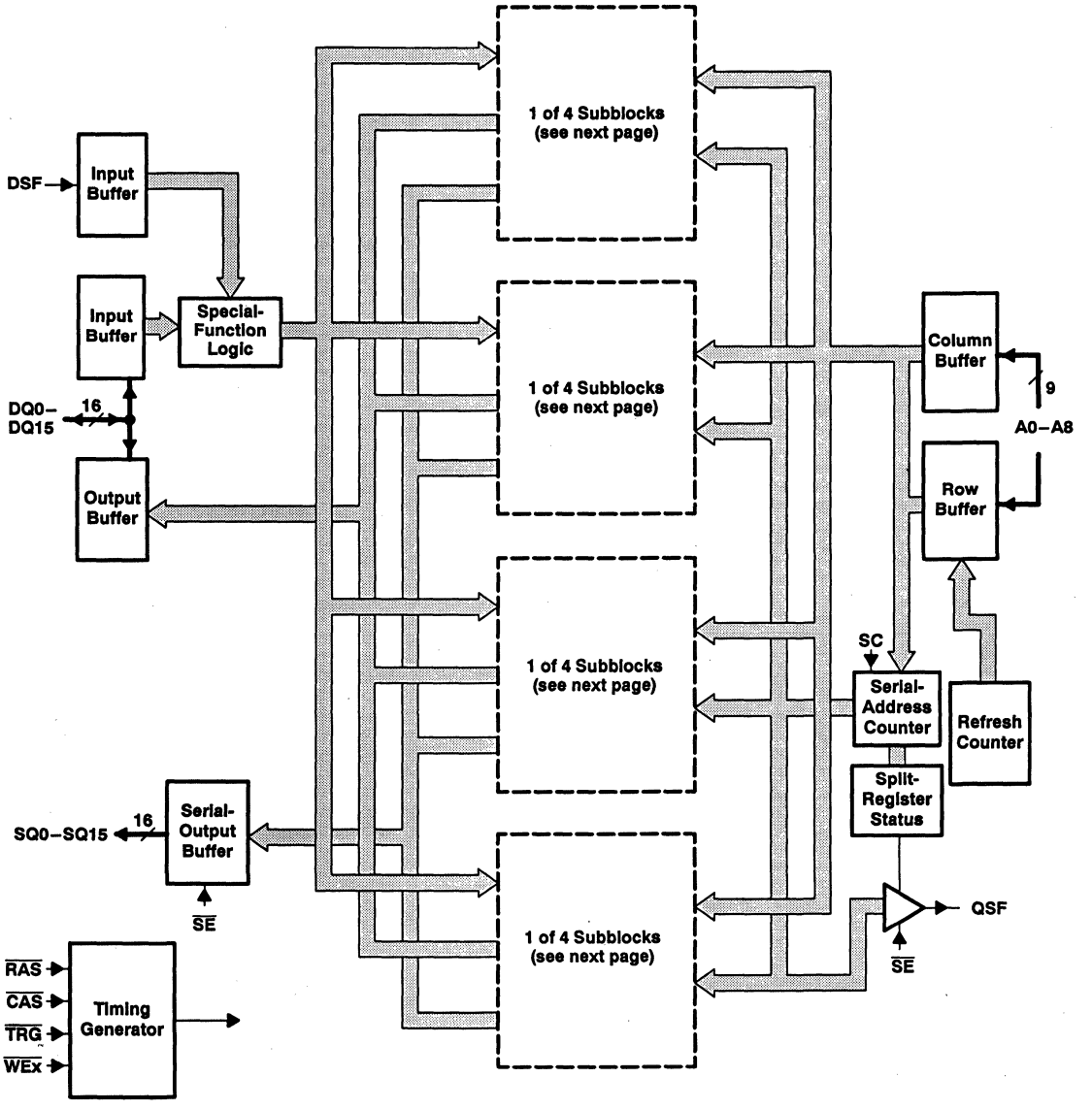
All inputs, outputs, and clock signals on the SMJ55166 are compatible with Series 54 TTL. All address lines and data-in lines are latched on chip to simplify system design. All data outs are unlatched to allow greater system flexibility.

The SMJ55166 employs state-of-the-art TI enhanced performance implanted CMOS (EPIC) scaled-CMOS, double-level polysilicon/polycide gate technology for very-high performance combined with improved reliability.

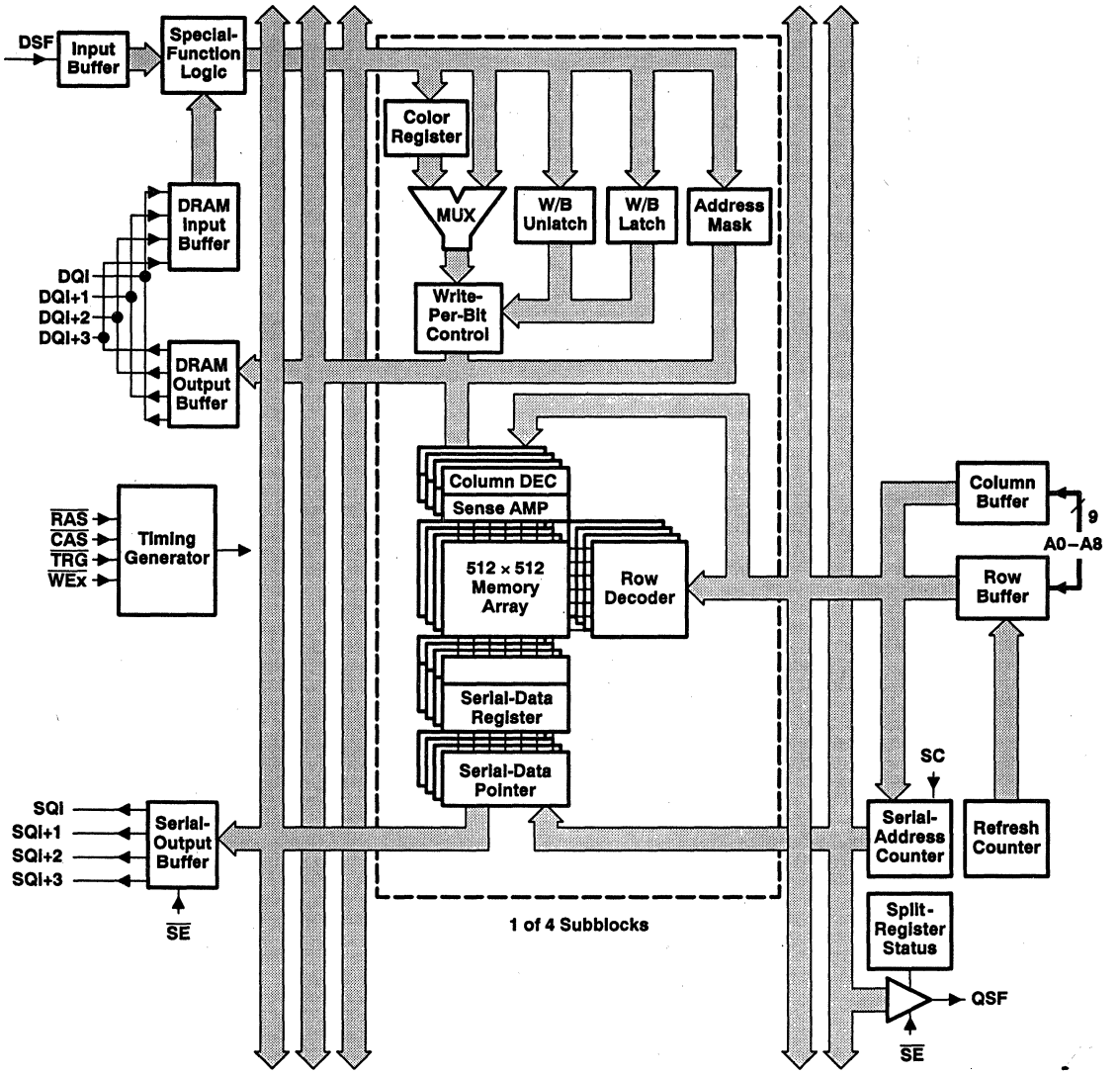
The SMJ55166 is offered in a 68-pin ceramic pin-grid-array package (GB suffix) and a 64-pin ceramic flatpack (HKC suffix).

The SMJ55166 and other TI multiport video RAMs are supported by a broad line of graphics processors and control devices from TI. Table 1 provides pin descriptions.

functional block diagram



functional block diagram (continued)



Function Table

FUNCTION	RAS FALL				CAS FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CAS	TRG	WEx‡	DSF	DSF	RAS	CAS§	RAS	WEL WEU CAS	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop-point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)★	L	X	H	H	X	X	X	X	X	CBRN
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
Load write-mask register □	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled
X = Don't care

† DQ0–DQ15 are latched on either the first falling edge of WEx or the falling edge of CAS, whichever occurs later.
‡ Logic L is selected when either or both WEL and WEU are low.
§ The column address and block address are latched on the first falling edge of CAS.
¶ CBRS cycle should be performed immediately after the powerup initialization cycle.
# A0–A3, A8: don't care; A4–A7 : stop-point code
‖ CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
★ CBR refresh (no reset) mode does not end persistent write-per-bit mode or stop-point mode.
□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.

Table 1. Pin Description Versus Operational Mode

PIN	DRAM	TRANSFER	SAM
A0–A8	Row, column address	Row address, tap point	
$\overline{CAS}$	Column-address strobe, DQ output enable	Tap-address strobe	
DQ	DRAM data I/O, write mask		
DSF	Block-write enable Write-mask-register load enable Color-register load enable CBR (option reset)	Split-register-transfer enable	
$\overline{RAS}$	Row-address strobe	Row-address strobe	
$\overline{SE}$			SQ output enable, QSF output enable
SC			Serial clock
SQ			Serial-data output
$\overline{TRG}$	DQ output enable	Transfer enable	
$\overline{WEL}$ $\overline{WEU}$	Write enable, write-per-bit enable		
QSF			Serial-register status
NC/GND	Either make no external connection or tie to system GND (V_{SS})		
V_{CC}†	5-V supply		
V_{SS}†	Ground		

† For proper device operation, all V_{CC} pins must be connected to a 5-V supply and all V_{SS} pins must be tied to ground.

pin definitions

address (A0–A8)

Eighteen address bits are required to decode one of 262 144 storage cell locations. Nine row-address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Nine column-address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and the falling edge of $\overline{CAS}$.

During the full-register-transfer read operation, the states of A0–A8 are latched on the falling edge of $\overline{RAS}$ to select one of the 512 rows where the transfer occurs. At the falling edge of $\overline{CAS}$, the column-address bits A0–A8 are latched. The most significant column-address bit (A8) selects which half of the row is transferred to the SAM. The appropriate 8-bit column address (A0–A7) selects one of 256 tap points (starting positions) for the serial-data output.

During the split-register-transfer read operation, address bit A7 is ignored at the falling edge of $\overline{CAS}$. An internal counter selects which half of the register is used. If the high half of the SAM is currently in use, the low half of the SAM is loaded with the low half of the DRAM half row and vice versa. Column address (A8) selects the DRAM half row. The remaining seven address bits (A0–A6) are used to select 1 of 127 possible starting locations within the SAM. Locations 127 and 255 are not valid tap points.

row-address strobe ($\overline{RAS}$)

$\overline{RAS}$ is similar to a chip enable so that all DRAM cycles and transfer cycles are initiated by the falling edge of $\overline{RAS}$. $\overline{RAS}$ is a control input that latches the states of the row address, $\overline{WEL}$, $\overline{WEU}$, $\overline{TRG}$, $\overline{CAS}$, and DSF onto the chip to invoke DRAM and transfer functions of the SMJ55166.

column-address strobe ($\overline{CAS}$)

$\overline{CAS}$ is a control input that latches the states of the column address and DSF to control DRAM and transfer functions of the SMJ55166. $\overline{CAS}$ also acts as output enable for the DRAM output pins DQ0–DQ15. In transfer operations, address bits A0–A8 are latched at the falling edge of $\overline{CAS}$ as the start position (tap) for the serial-data output (SQ0–SQ15).

output enable/transfer select ($\overline{TRG}$)

$\overline{TRG}$ selects either DRAM or transfer operation as $\overline{RAS}$ falls. For DRAM operation, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. During DRAM operation, $\overline{TRG}$ functions as an output enable for the DRAM output pins DQ0–DQ15. For transfer operation, $\overline{TRG}$ must be brought low before $\overline{RAS}$ falls.

write mask select, write enable ($\overline{WEL}$, $\overline{WEU}$)

In DRAM operation, $\overline{WEL}$ enables data to be written to the lower byte (DQ0–DQ7) and $\overline{WEU}$ enables data to be written to the upper byte (DQ8–DQ15) of the DRAM. Both $\overline{WEL}$ and $\overline{WEU}$ have to be held high together to select the read mode. Bringing either or both $\overline{WEL}$ and $\overline{WEU}$ low selects the write mode. $\overline{WEL}$ and $\overline{WEU}$ are also used to select the DRAM write-per-bit mode. Holding either or both $\overline{WEL}$ and $\overline{WEU}$ low on the falling edge of $\overline{RAS}$ invokes the write-per-bit operation. The SMJ55166 supports both the nonpersistent write-per-bit mode and the persistent write-per-bit mode.

special-function select (DSF)

The DSF input is latched on the falling edge of $\overline{RAS}$ or the first falling edge of $\overline{CAS}$, similar to an address. DSF determines which of the following functions are invoked on a particular cycle:

- CBR refresh with reset (CBR)
- CBR refresh with no reset (CBRN)
- CBR refresh with no reset and stop-point set (CBRS)
- Block write (BW)
- Loading write-mask register for the persistent write-per-bit mode (LMR)
- Loading color register for the block-write mode (LCR)
- Split-register-transfer read (SRT)

DRAM data I/O, write mask data (DQ0–DQ15)

DRAM data is written or read through the common I/O DQ pins. The 3-state DQ-output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 54 TTL load. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state as long as either $\overline{TRG}$ or $\overline{CAS}$ is held high. Data does not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. The write mask is latched into the device via the random DQ pins by the falling edge of $\overline{RAS}$ and is used on all write-per-bit cycles. In a transfer operation, the DQ outputs remain in the high-impedance state for the entire cycle.

serial data outputs (SQ0–SQ15)

Serial data is read from SQ. SQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 54 TTL load. The serial outputs are in the high-impedance (floating) state while the serial-enable pin, $\overline{SE}$, is high. The serial outputs are enabled when $\overline{SE}$ is brought low.

serial clock (SC)

Serial data is accessed out of the data register from the rising edge of SC. The SMJ55166 is designed to work with a wide range of clock duty cycles to simplify system design. There is no refresh requirement because the data registers that comprise the SAM are static. There is also no minimum SC clock operating frequency.

serial enable ($\overline{SE}$)

During serial-access operations, $\overline{SE}$ is used as an enable/disable for the SQ outputs. $\overline{SE}$ low enables the serial-data output. $\overline{SE}$ high disables the serial-data output. $\overline{SE}$ is also used as an enable/disable for output pin QSF.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is not disabled. External SC pulses increment the internal serial-address counter regardless of the state of $\overline{SE}$. This ungated serial-clock scheme minimizes access time of serial output from $\overline{SE}$ low because the serial-clock input buffer and the serial-address counter are not disabled by $\overline{SE}$.

special-function output (QSF)

QSF is an output pin that indicates which half of the SAM is being accessed. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of the SAM. When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF changes state upon crossing a boundary between the two SAM halves.

During full-register-transfer operations, QSF can change state upon completing the cycle. This state is determined by the tap point loaded during the transfer cycle. QSF output is enabled by $\overline{SE}$. If $\overline{SE}$ is high, the QSF output is in the high-impedance state.

no connect/ground (NC/GND)

NC/GND should be tied to system ground or left floating for proper device operation. Table 2 contains DRAM functions.

functional operation description

Table 2. DRAM Function Table

FUNCTION	RAS FALL				CAS FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CAS	TRG	WEx‡	DSF	DSF	RAS	CAS§	RAS	WEL WEU CAS	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop-point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)★	L	X	H	H	X	X	X	X	X	CBRN
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
Load write-mask register □	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled
X = Don't care

† DQ0–DQ15 are latched on either the first falling edge of WEx or the falling edge of CAS, whichever occurs later.
‡ Logic L is selected when either or both WEL and WEU are low.
§ The column address and block address are latched on the first falling edge of CAS.
¶ CBRS cycle should be performed immediately after the power-up initialization cycle.
# A0–A3, A8: don't care; A4–A7 : stop-point code
‖ CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
★ CBR refresh (no reset) mode does not end persistent write-per-bit mode or stop-point mode.
□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. This mode eliminates the time required for row-address setup, row-address hold, and address multiplex. The maximum $\overline{RAS}$ low time and $\overline{CAS}$ page cycle time used determines the number of columns that can be accessed.

Unlike conventional page-mode operations, the enhanced page mode allows the SMJ55166 to operate at a higher data bandwidth. Data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. A valid column address can be presented immediately after the row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low) if $t_{a(CA)}$ max (access time from column address) has been satisfied.

refresh

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refreshes are accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored, and the refresh row address is generated internally. Three types of CBR refresh cycles are available. The CBR refresh (option reset) ends the persistent write-per-bit mode and the stop-point mode. The CBRN and CBRS refreshes (no reset) do not end the persistent write-per-bit mode or the stop-point mode. The 512 rows of the DRAM do not necessarily need to be refreshed consecutively as long as the entire refresh is completed within the required time period, $t_{rf(MA)}$. The output buffers remain in the high-impedance state during the CBR refresh cycles regardless of the state of $\overline{TRG}$.

hidden refresh

A hidden refresh is accomplished by holding $\overline{CAS}$ low in the DRAM read cycle and cycling $\overline{RAS}$. The output data of the DRAM read cycle remains valid while the refresh is carried out. Like the CBR refresh, the refreshed row addresses are generated internally during the hidden refresh.

$\overline{RAS}$-only refresh

A $\overline{RAS}$-only refresh is accomplished by cycling $\overline{RAS}$ at every row address. Unless $\overline{CAS}$ and $\overline{TRG}$ are low, the output buffers remain in the high-impedance state to conserve power. Externally generated addresses must be supplied during $\overline{RAS}$-only refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed.

extended data output

The SMJ55166 features extended data output during DRAM accesses. While $\overline{RAS}$ and $\overline{TRG}$ are low, the DRAM output remains valid. The output remains valid even when $\overline{CAS}$ returns high until $\overline{WEx}$ is low, $\overline{TRG}$ is high, or both $\overline{CAS}$ and $\overline{RAS}$ are high (see Figure 1 and Figure 2). The extended data-output mode functions in all read cycles including DRAM read, page-mode read, and read-modify-write cycles (see Figure 3).

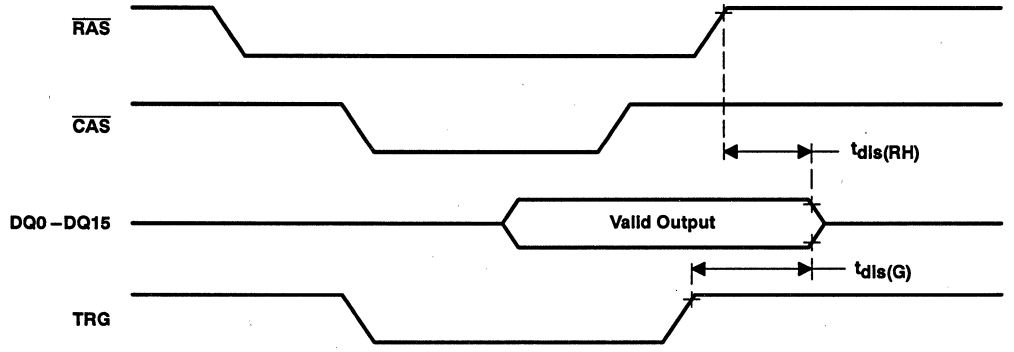


Figure 1. DRAM Read Cycle With $\overline{RAS}$-Controlled Output

extended data output (continued)

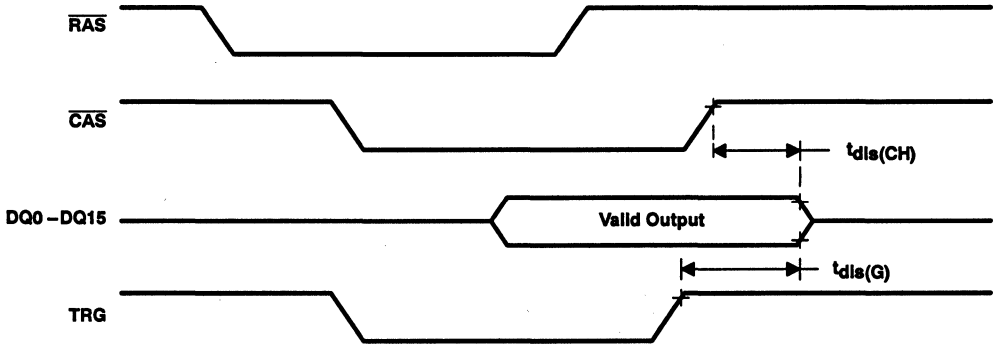


Figure 2. DRAM Read Cycle With $\overline{CAS}$-Controlled Output

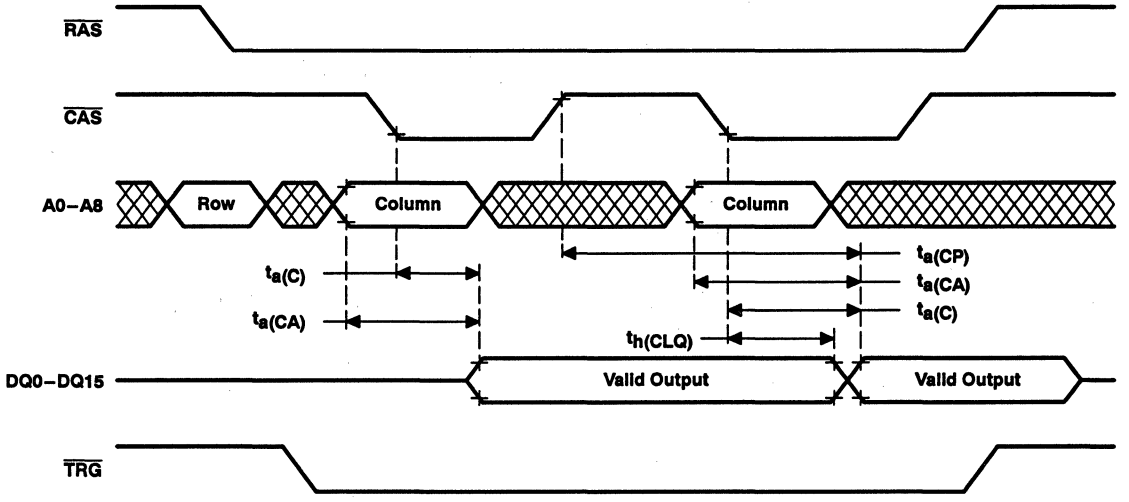
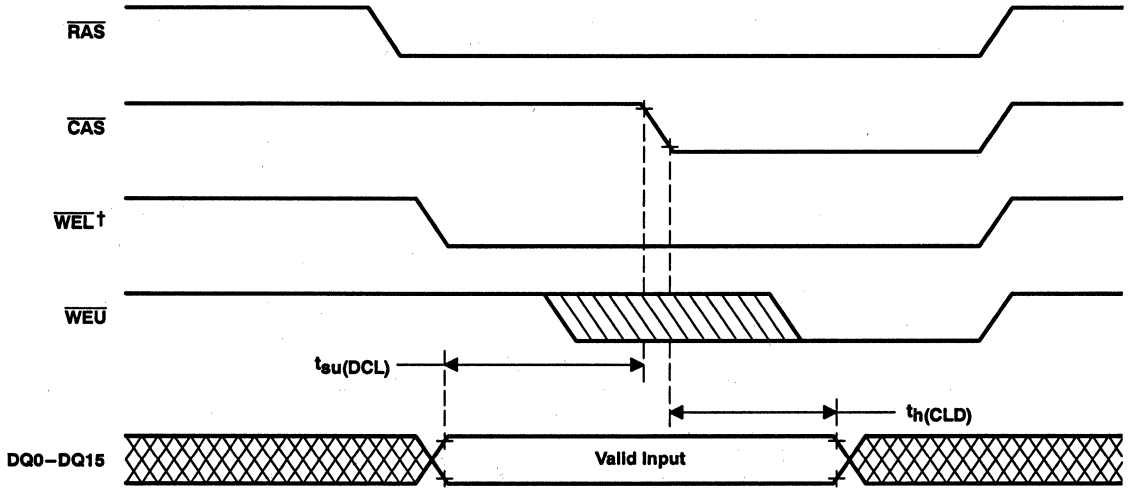


Figure 3. DRAM Page-Read Cycle With Extended Output

byte-write operation

Byte-write operations can be applied in DRAM-write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. Holding either or both $\overline{WEL}$ and $\overline{WEU}$ low selects the write mode. In normal write cycles, $\overline{WEL}$ enables data to be written to the lower byte (DQ0–DQ7) and $\overline{WEU}$ enables data to be written to the upper byte (DQ8–DQ15). For early-write cycles, one $\overline{WEx}$ is brought low before $\overline{CAS}$ falls. The other $\overline{WEx}$ can be brought low before $\overline{CAS}$ falls or after $\overline{CAS}$ falls. The data is strobed in with data setup and hold times for DQ0–DQ15 referenced to $\overline{CAS}$ (see Figure 4).



† Either $\overline{WEU}$ or $\overline{WEL}$ can be brought low prior to $\overline{CAS}$ to initiate an early-write cycle.

Figure 4. Example of an Early-Write Cycle

byte-write operation (continued)

For late-write or read-modify-write cycles, $\overline{WEL}$ and $\overline{WEU}$ are both held high before $\overline{CAS}$ falls. After $\overline{CAS}$ falls, either or both $\overline{WEL}$ and $\overline{WEU}$ are brought low to select the corresponding byte or bytes to be written. Data is strobed in by either or both $\overline{WEL}$ and $\overline{WEU}$ with data setup and hold times for DQ0–DQ15 referenced to whichever $\overline{WEx}$ falls earlier (see Figure 5).

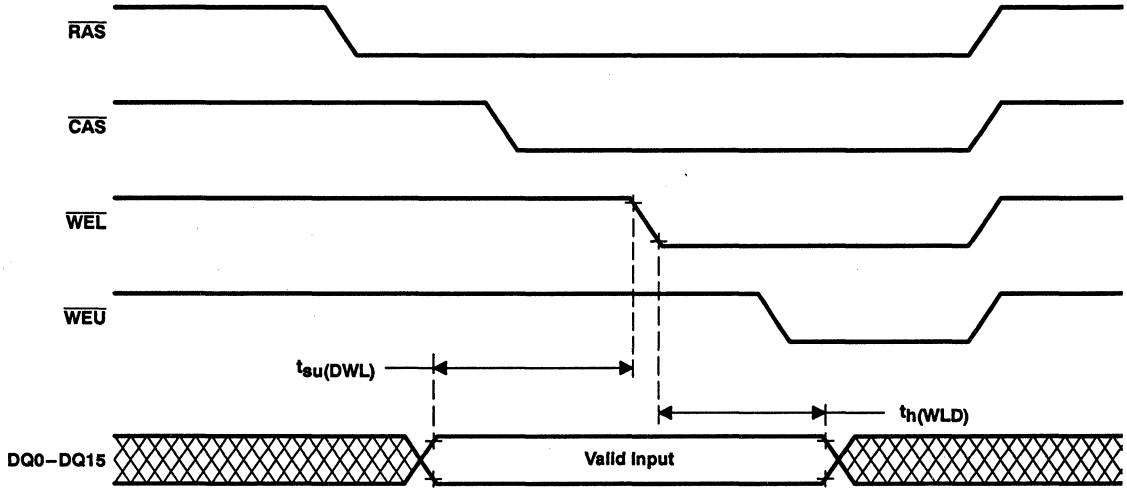


Figure 5. Example of a Late-Write Cycle

write-per-bit

The write-per-bit feature allows masking any combination of the 16 DQs on any write cycle. The write-per-bit operation is invoked when either $\overline{WEL}$ or $\overline{WEU}$ are held low on the falling edge of $\overline{RAS}$. Assertion of either individual $\overline{WEx}$ allows entry of the entire 16-bit mask on DQ0–DQ15. Byte control of the mask input is not allowed. If both $\overline{WEL}$ and $\overline{WEU}$ are held high on the falling edge of $\overline{RAS}$, the write operation is performed without any masking. The SMJ55166 offers two write-per-bit modes: nonpersistent write-per-bit and persistent write-per-bit.

nonpersistent write-per-bit

When either or both $\overline{WEL}$ and $\overline{WEU}$ are low on the falling edge of $\overline{RAS}$, the write mask is reloaded. A 16-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the 16 random I/Os are to be written and which are not. After $\overline{RAS}$ has latched the on-chip write-per-bit mask, input data is driven onto the DQ pins and is latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later. $\overline{WEL}$ enables the lower byte (DQ0–DQ7) to be written through the mask and $\overline{WEU}$ enables the upper byte (DQ8–DQ15) to be written through the mask. If a data low (write mask = 0) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data is not written to that I/O. If a data high (write mask = 1) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data is written to that I/O (see Figure 6).

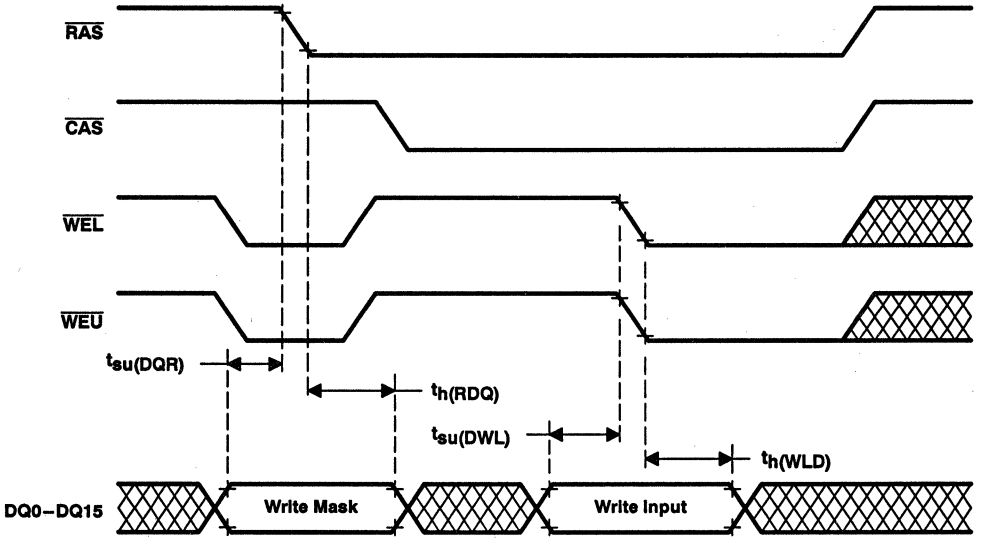


Figure 6. Example of a Nonpersistent Write-Per-Bit (Late-Write) Operation

persistent write-per-bit

The persistent write-per-bit mode is initiated by performing a load-write-mask-register (LMR) cycle. In the persistent write-per-bit mode, the write-per-bit mask is not overwritten but remains valid over an arbitrary number of write cycles until another LMR cycle is performed or power is removed.

The LMR cycle is performed using DRAM write-cycle timing with DSF held high on the falling edge of $\overline{RAS}$ and held low on the falling edge of $\overline{CAS}$. A binary code is input to the write-mask register via the random I/O pins and latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later. Byte write control can be applied to the write mask during the LMR cycle. The persistent write-per-bit mode can then be used in exactly the same way as the nonpersistent write-per-bit mode except that the input data on the falling edge of $\overline{RAS}$ is ignored. When the device is set to the persistent write-per-bit mode, it remains in this mode and is reset only by a CBR refresh (option reset) cycle (see Figure 7).

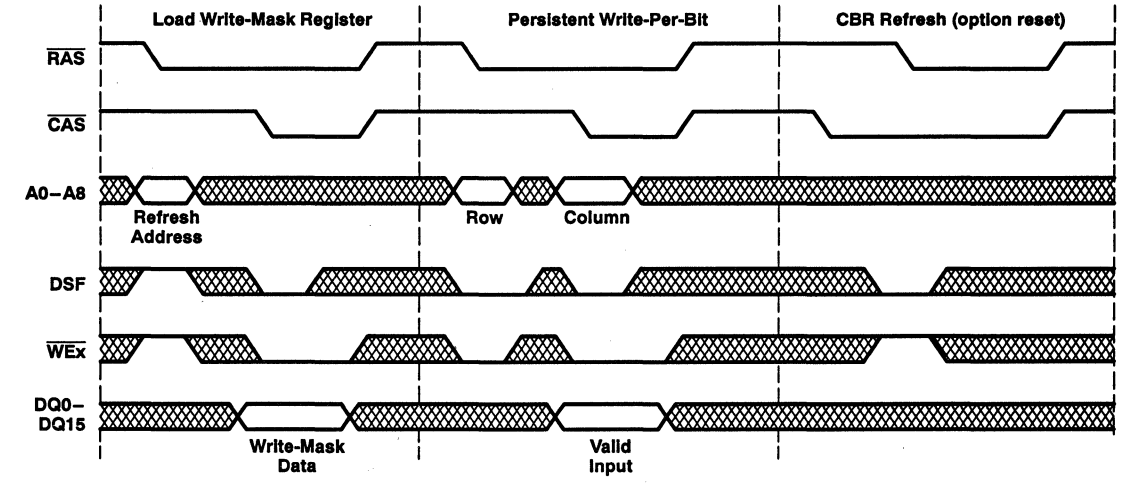


Figure 7. Example of a Persistent Write-Per-Bit Operation

block write

The block-write feature allows up to 64 bits of data to be written simultaneously to one row of the memory array. This function is implemented as 4 columns × 4 DQs and repeated in four quadrants. In this manner, each of the four one-megabit quadrants can have up to four consecutive columns written at a time with up to four DQs per column (see Figure 8).

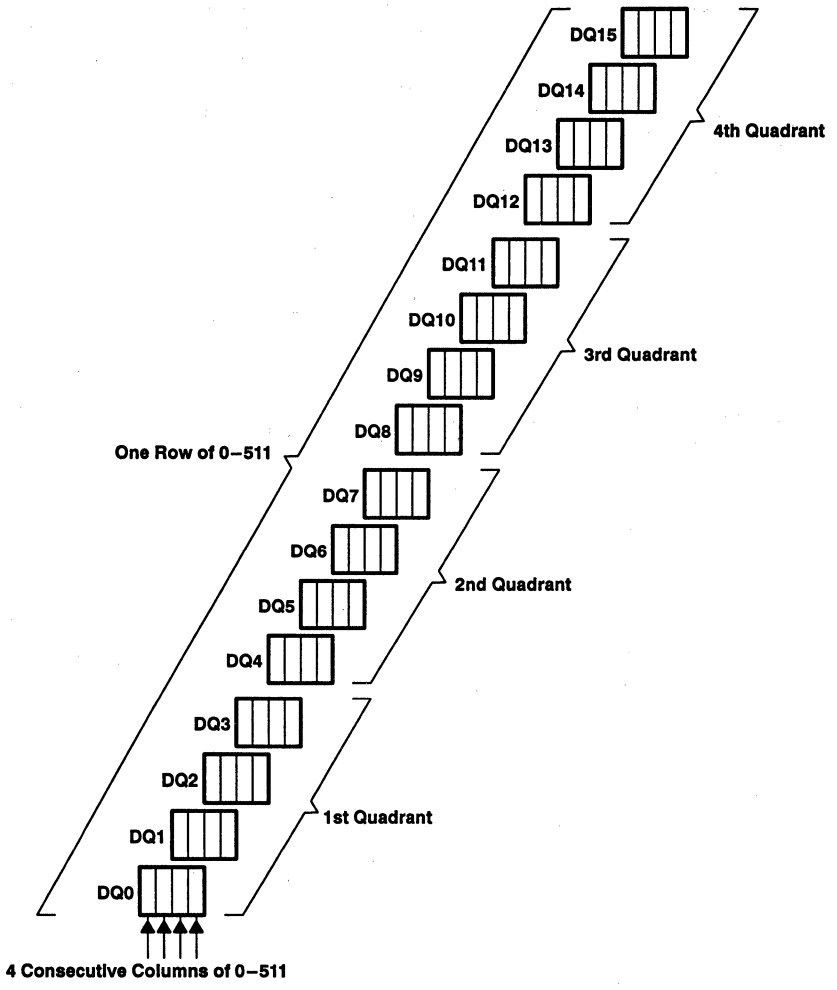


Figure 8. Block-Write Operation

Each one-megabit quadrant has a 4-bit column mask to mask off any or all of the four columns from being written with data. Nonpersistent write-per-bit or persistent write-per-bit functions can be applied to the block-write operation to provide write-masking options. The DQ data is provided by four bits from the on-chip color register. Bits 0–3 from the 16-bit write-mask register, bits 0–3 from the 16-bit column-mask register, and bits 0–3 from the 16-bit color-data register configure the block write for the first quadrant, while bits 4–7, 8–11, and 12–15 of the corresponding registers control the other quadrants in a similar fashion (see Figure 9).

block write (continued)

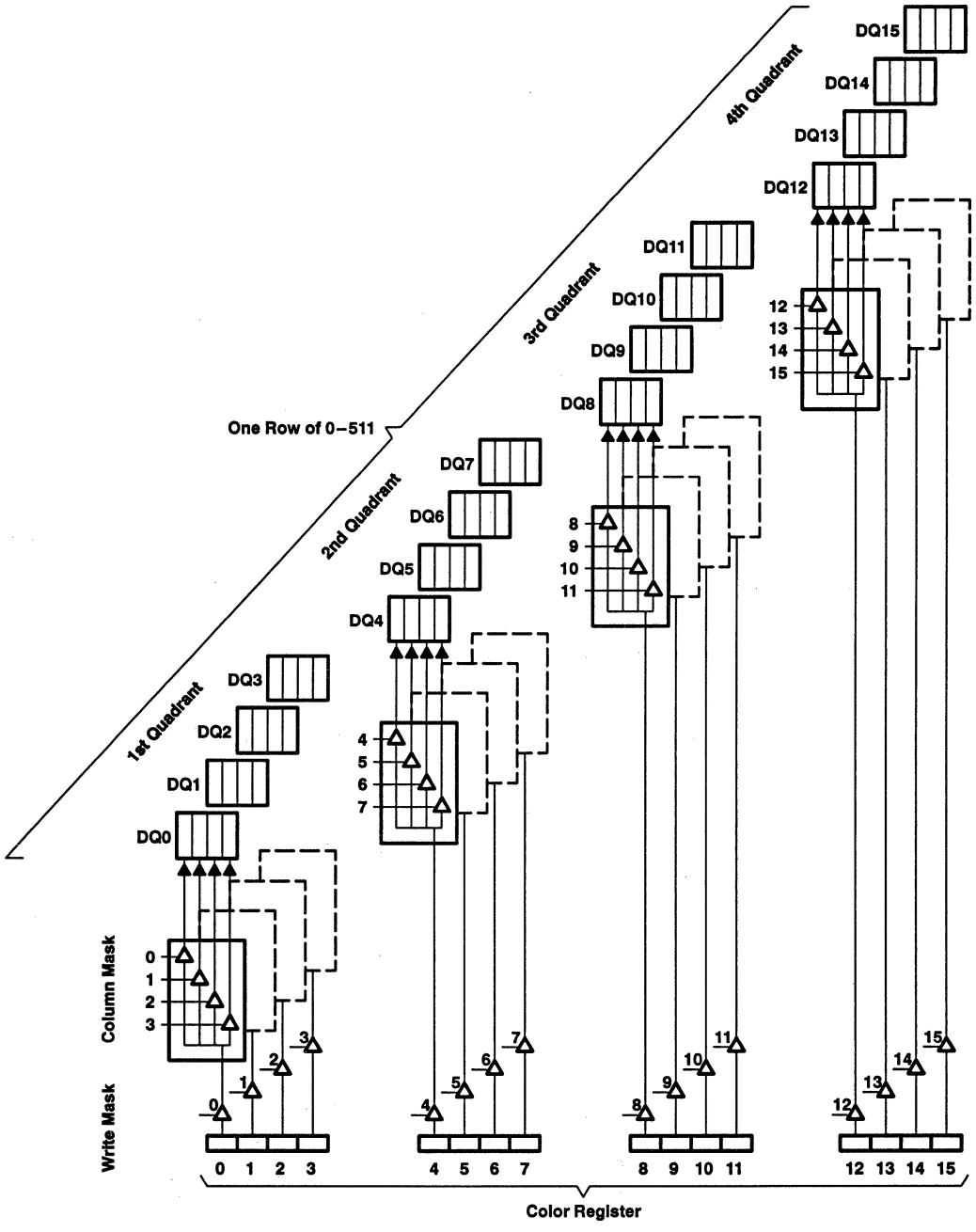


Figure 9. Block Write With Masks

block write (continued)

Every four columns make a block, which results in 128 blocks along one row. Block 0 comprises columns 0–3, block 1 comprises columns 4–7, block 2 comprises columns 8–11, etc., as shown in Figure 10.

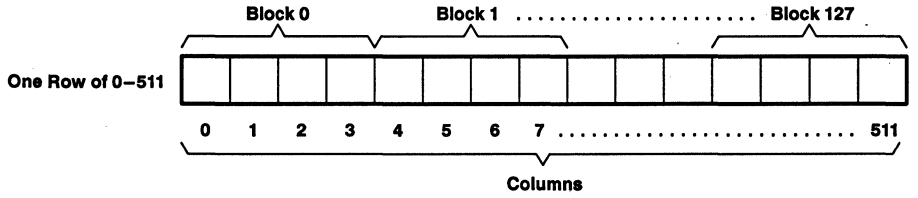


Figure 10. Block Columns Organization

During block-write cycles, only the seven most significant column addresses (A2–A8) are latched on the falling edge of $\overline{CAS}$ to decode one of the 128 blocks. Address bits A0–A1 are ignored. Each one-megabit quadrant has the same block selected.

A block-write cycle is entered in a manner similar to a DRAM write cycle except DSF is held high on the first falling edge of $\overline{CAS}$. As in a DRAM write operation, $\overline{WEL}$ and $\overline{WEU}$ enable the corresponding lower and upper DRAM DQ bytes to be written, respectively. The column-mask data is input via the DQs and is latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later. The 16-bit color-data register must be loaded prior to performing a block write as described below. Refer to the write-per-bit section for details on use of the write-mask capability, allowing additional performance options.

Example of block write:

block-write column address = 110000000 (A0–A8 from left to right)

	bit 0			bit 15
color-data register =	1011	1011	1100	0111
write-mask register =	1110	1111	1111	1011
column-mask register =	1111	0000	0111	1010
	1st Quad	2nd Quad	3rd Quad	4th Quad

Column-address bits A0 and A1 are ignored. Block 0 (columns 0–3) is selected for each one-megabit quadrant. The first quadrant has DQ0–DQ2 written with bits 0–2 from the color-data register (101) to all four columns of block 0. DQ3 is not written and retains its previous data due to write-mask-register-bit 3 being a 0.

The second quadrant (DQ4–DQ7) has all four columns masked off due to the column-mask bits 4–7 being 0, so that no data is written.

The third quadrant (DQ8–DQ11) has its four DQs written with bits 8–11 from the color-data register (1100) to columns 1–3 of its block 0. Column 0 is not written and retains its previous data on all four DQs due to column-mask-register-bit 8 being 0.

The fourth quadrant (DQ12–DQ15) has DQ12, DQ14, and DQ15 written with bits 12, 14, and 15 from the color-data register to column 0 and column 2 of its block 0. DQ13 retains its previous data on all columns due to the write mask. Columns 1 and 3 retain their previous data on all DQs due to the column mask. If the previous data for the quadrant was all 0s, the fourth quadrant would contain the data pattern shown in Figure 11 after the block-write operation shown in the previous example.

block write (continued)

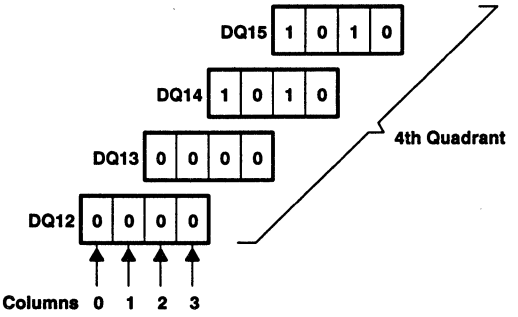
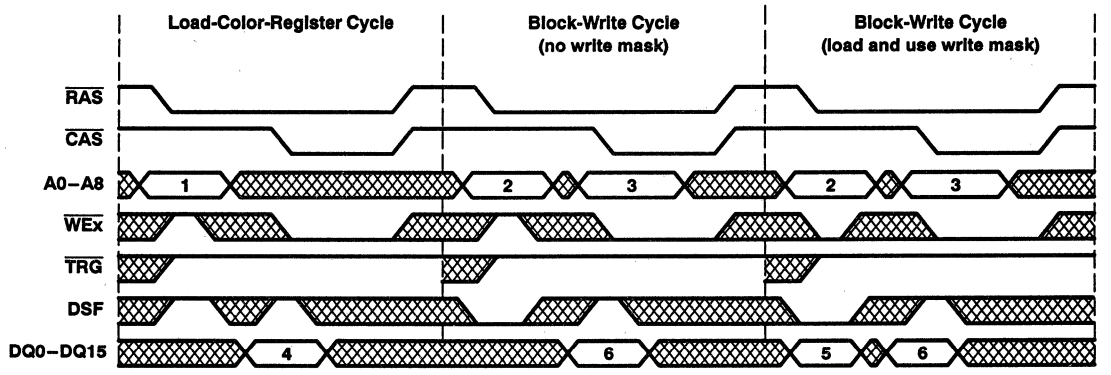


Figure 11. Example of Fourth Quadrant After Block-Write Operation

load color register

The load-color-register cycle is performed using normal DRAM write-cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. The color register is loaded from pins DQ0–DQ15, which are latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later. If only one $\overline{WEx}$ is low, only the corresponding byte of the color register is loaded. When the color register is loaded, it retains data until power is lost or until another load-color-register cycle is performed (see Figures 12 and 13).



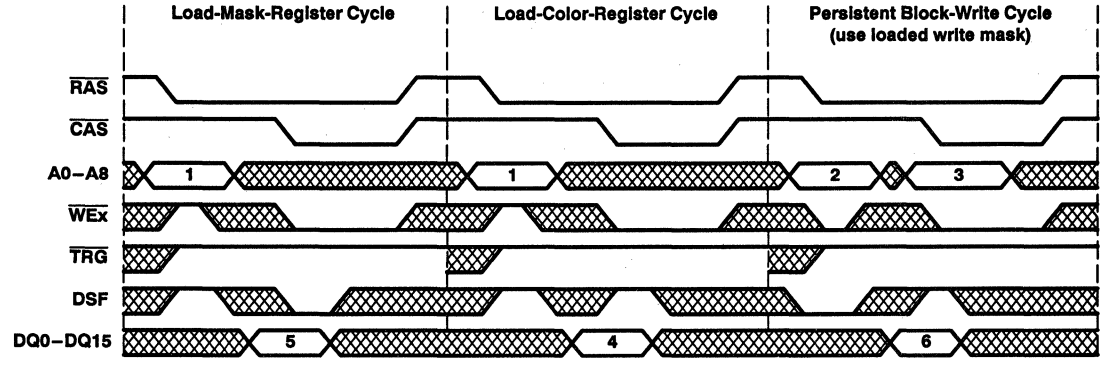
Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the falling edge of $\overline{CAS}$.
4. Color-register data
5. Write-mask data: DQ0–DQ15 are latched on the falling edge of $\overline{RAS}$.
6. Column-mask data: DQi–DQi + 3 (i = 0, 4, 8, 12) are latched on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later.

= don't care

Figure 12. Example of Block Writes

load color register (continued)



Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the falling edge of $\overline{CAS}$.
4. Color-register data
5. Write-mask data: DQ0 – DQ15 are latched on the falling edge of $\overline{CAS}$.
6. Column-mask data: DQi–DQi + 3 (i = 0, 4, 8, 12) are latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later.

= don't care

Figure 13. Example of a Persistent Block Write

DRAM-to-SAM transfer operation

During the DRAM-to-SAM transfer operation, one half of a row (256 columns) in the DRAM array is selected to be transferred to the 256-bit serial-data register. The transfer operation is invoked by bringing $\overline{TRG}$ low and holding $\overline{WEx}$ high on the falling edge of $\overline{RAS}$. The state of DSF, which is latched on the falling edge of $\overline{RAS}$, determines whether the full-register-transfer read operation or the split-register-transfer read operation is performed.

Table 3. SAM Function Table

FUNCTION	$\overline{RAS}$ FALL				$\overline{CAS}$ FALL	ADDRESS		DQ0 – DQ15		MNE CODE
	$\overline{CAS}$	$\overline{TRG}$	$\overline{WEx}$†	DSF	DSF	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$ $\overline{WEx}$	
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT

† Logic L is selected when either or both $\overline{WEL}$ and $\overline{WEU}$ are low.
X = don't care

full-register-transfer read

A full-register-transfer read operation loads data from a selected half of a row in the DRAM into the SAM. $\overline{TRG}$ is brought low and latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0 – A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. The nine column-address bits (A0 – A8) are latched at the falling edge of $\overline{CAS}$, where address bit A8 selects which half of the row is transferred. Address bits A0 – A7 select one of the SAM 256 available tap points from which the serial data is read out (see Figure 14).

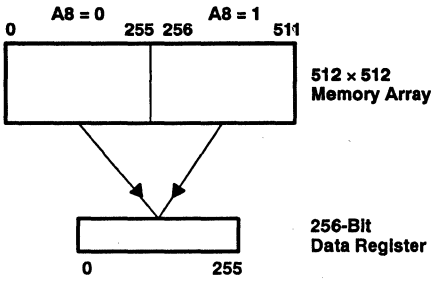


Figure 14. Full-Register-Transfer Read

A full-register-transfer read can be performed in three ways: early load, real-time load (or midline load), or late load. Each of these offers the flexibility of controlling the $\overline{TRG}$ trailing edge in the full-register-transfer read cycle (see Figure 15).

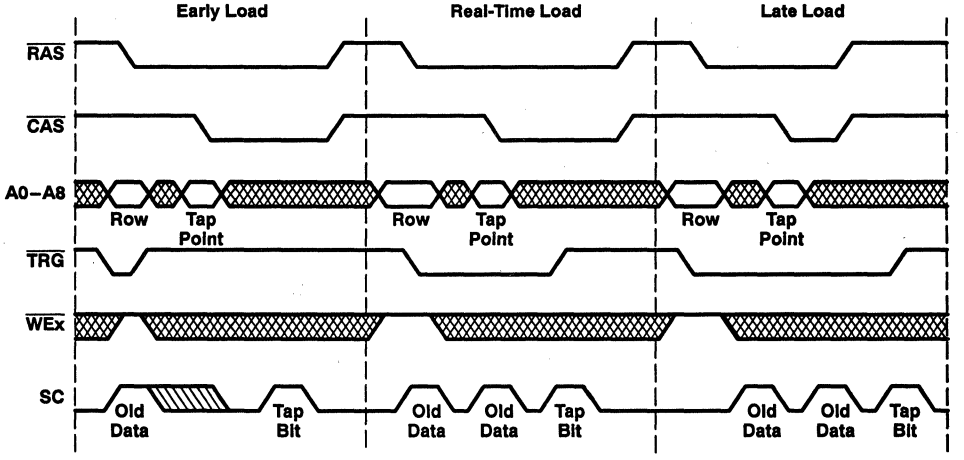


Figure 15. Example of Full-Register-Transfer Read Operations

split-register-transfer read

In the split-register-transfer read operation, the serial-data register is split into halves (see Figure 16). The low half contains bits 0 – 127, and the high half contains bits 128 – 255. While one half is being read out of the SAM port, the other half can be loaded from the memory array.

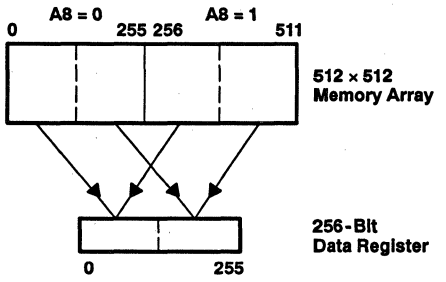
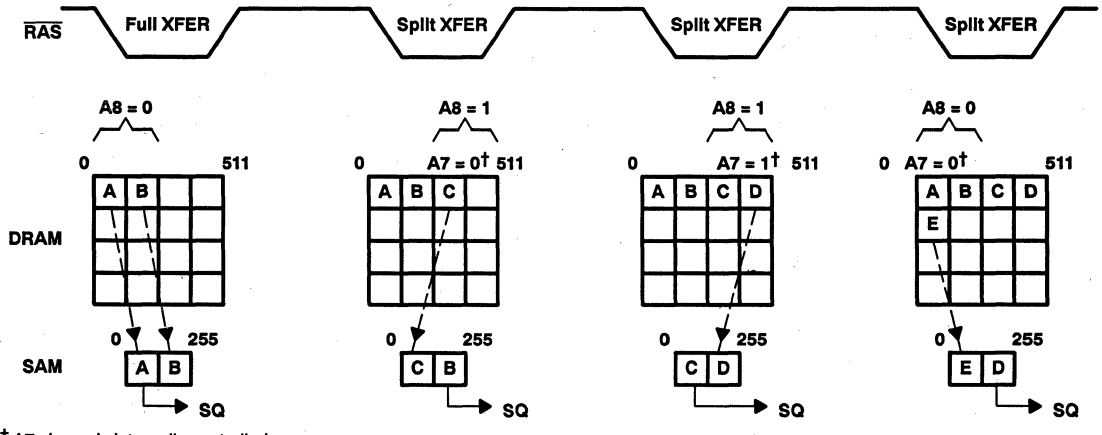


Figure 16. Split-Register-Transfer Read

To invoke a split-register-transfer read cycle, DSF is brought high, $\overline{TRG}$ is brought low, and both are latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0 – A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. Eight of the nine column-address bits (A0 – A6 and A8) are latched at the falling edge of $\overline{CAS}$. Column-address bit A8 selects which half of the row is to be transferred. Column-address bits A0 – A6 select one of the 127 tap points in the specified half of the SAM. Column-address bit A7 is ignored, and the split-register-transfer is internally controlled to select the inactive register half (see Figure 17).



† A7 shown is internally controlled.

Figure 17. Example of a Split-Register-Transfer Read Operation

A full-register-transfer read must precede the first split-register-transfer read to ensure proper operation. After the full-register-transfer read cycle, the first split-register-transfer read can follow immediately without any minimum SC clock requirement.

split-register-transfer read (continued)

QSF indicates which half of the register is being accessed during serial-access operation. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of the SAM. When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF changes state upon completing a full-register-transfer read cycle. The tap point loaded during the current transfer cycle determines the state of QSF. QSF also changes state when a boundary between two register halves is reached (see Figure 18 and Figure 19).

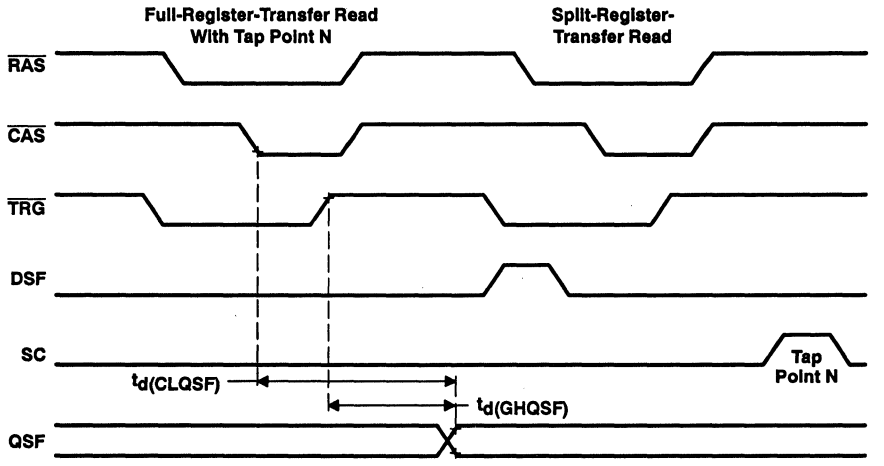


Figure 18. Example of a Split-Register-Transfer Read After a Full-Register-Transfer Read

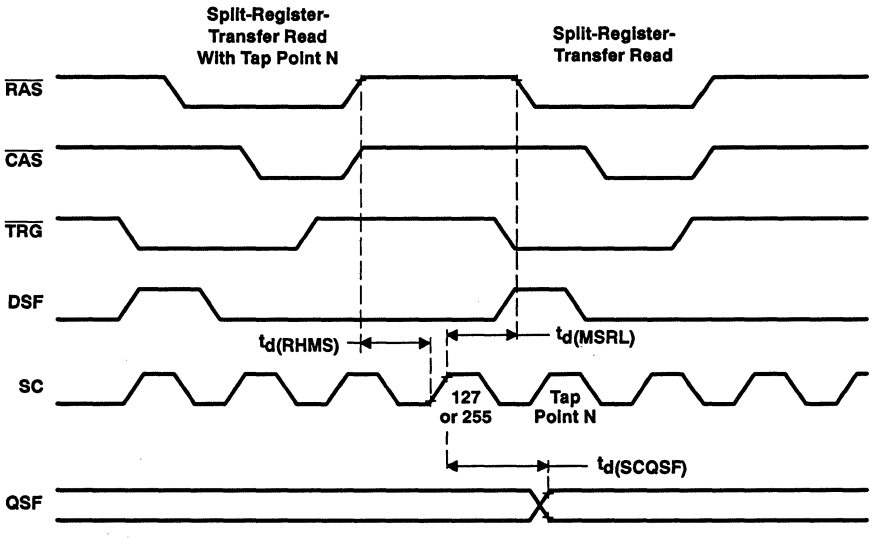


Figure 19. Example of Successive Split-Register-Transfer Read Operations

serial-read operation

The serial-read operation can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during transfer operations. Serial data can be read from the SAM by clocking SC starting at the tap point loaded by the preceding transfer cycle, proceeding sequentially to the most significant bit (bit 255), and then wrapping around to the least significant bit (bit 0), as shown in Figure 20.

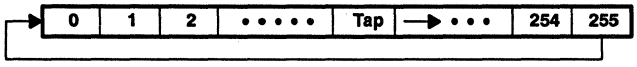


Figure 20. Serial-Pointer Direction for Serial Read

For split-register-transfer read operation, serial data can be read out from the active half of the SAM by clocking SC starting at the tap point loaded by the preceding split-register-transfer cycle. The serial pointer then proceeds sequentially to the most significant bit of the half, bit 127 or bit 255. If there is a split-register-transfer read to the inactive half during this period, the serial pointer points next to the tap point location loaded by that split-register-transfer (see Figure 21).

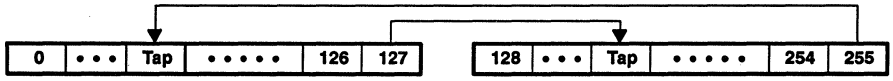


Figure 21. Serial Pointer for Split-Register-Transfer Read – Case I

If there is no split-register-transfer read to the inactive half during this period, the serial pointer points next to bit 128 or bit 0, respectively (see Figure 22).

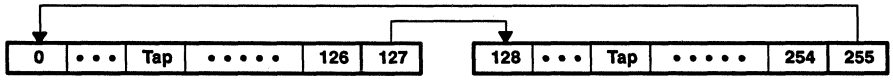


Figure 22. Serial Pointer for Split-Register-Transfer Read – Case II

split-register programmable stop point

The SMJ55166 offers programmable stop-point mode for split-register-transfer read operation. This mode can be used to improve two-dimensional drawing performance in a nonscanline data format.

In split-register-transfer read operation, the stop point is defined as a register location at which the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM. While in stop-point mode, the SAM is divided into partitions whose lengths are programmed via row addresses A4–A7 in a CBR set (CBRS) cycle. The last serial-address location of each partition is the stop point (see Figure 23).

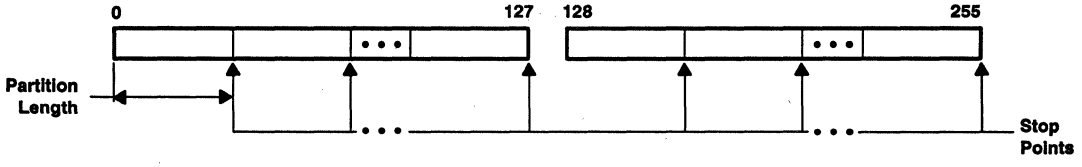


Figure 23. Example of the SAM With Partitions

split-register programmable stop point (continued)

Stop-point mode is not active until the CBRS cycle is initiated. The CBRS operation is performed by holding $\overline{CAS}$ and $\overline{WEx}$ low and DSF high on the falling edge of $\overline{RAS}$. The falling edge of $\overline{RAS}$ also latches row addresses A4–A7, which are used to define the SAM partition length. The other row-address inputs are don't cares. Stop-point mode should be initiated after the initialization cycles are performed (see Table 4).

Table 4. Programming Code for Stop-Point Mode

MAXIMUM PARTITION LENGTH	ADDRESS AT $\overline{RAS}$ IN CBRS CYCLE						NUMBER OF PARTITIONS	STOP-POINT LOCATIONS
	A8	A7	A6	A5	A4	A0–A3		
16	X	L	L	L	L	X	16	15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255
32	X	L	L	L	H	X	8	31, 63, 95, 127, 159, 191, 223, 255
64	X	L	L	H	H	X	4	63, 127, 191, 255
128 (default)	X	L	H	H	H	X	2	127, 255

In stop-point mode, the tap point loaded during the split-register-transfer read cycle determines the SAM partition in which the serial output begins and at which stop point the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM (see Figure 24).

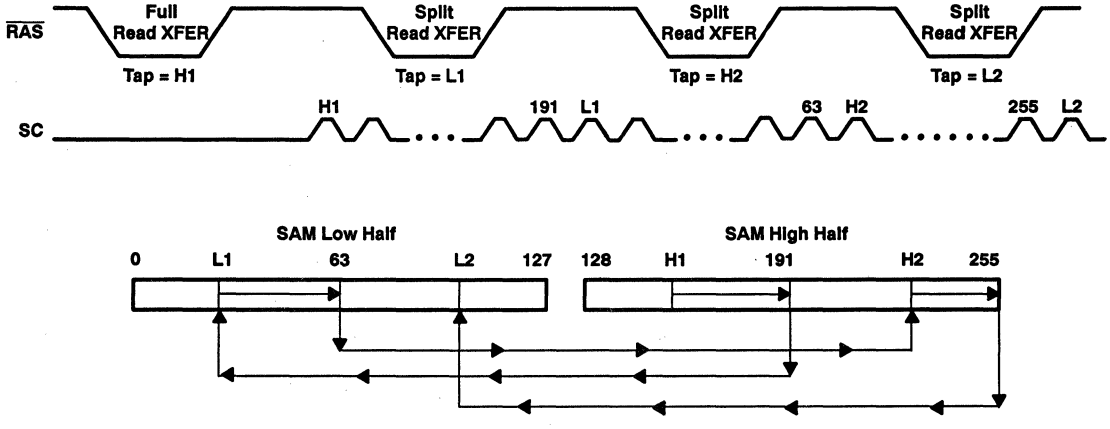


Figure 24. Example of Split-Register Operation With Programmable Stop Points

256-/512-bit compatibility of split-register programmable stop point

The stop-point mode is designed to be compatible with both 256-bit SAM and 512-bit SAM devices. After the CBRS cycle is initiated, the stop-point mode becomes active. In the stop-point mode, and only in the stop-point mode, the column-address bits AY7 and AY8 are internally swapped to assure compatibility (see Figure 25). This address-bit swap applies to the column address, and it is effective for all DRAM and transfer cycles. For example, during the split-register-transfer cycle with stop point, column-address bit AY8 is a don't care and AY7 decodes the DRAM row half for the split-register-transfer. During stop-point mode, a CBR (option reset) cycle is not recommended because this ends the stop-point mode and restores address bits AY7 and AY8 to their normal functions. Consistent use of CBR cycles ensures that the SMJ55166 remains in normal mode.

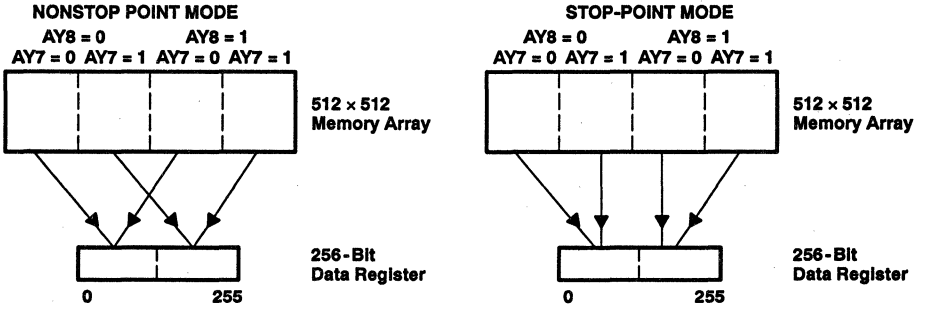


Figure 25. DRAM-to-SAM Mapping, Nonstop Point Versus Stop Point

IMPORTANT: For proper device operation, a stop-point-mode (CBRS) cycle should be initiated immediately after the power-up initialization cycles are performed.

power up

To achieve proper device operation, an initial pause of 200 µs is required after power up followed by a minimum of eight $\overline{RAS}$ cycles or eight CBR cycles to initialize the DRAM port. A full-register-transfer read cycle and two SC cycles are required to initialize the SAM port.

After initialization, the internal state of the SMJ55166 is as follows:

	STATE AFTER INITIALIZATION
QSF	Defined by the transfer cycle during initialization
Write mode	Nonpersistent mode
Write-mask register	Undefined
Color register	Undefined
Serial-register tap point	Defined by the transfer cycle during initialization
SAM port	Output mode

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −1 V to 7 V
Voltage range on any pin ..... −1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1.1 W
Operating free-air temperature range, T_A ..... −55°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	−55		125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	SAM PORT	'55166-70		'55166-80		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −1 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 5.8 V, All other pins at 0 V to V_{CC}			±10		±10	µA
I_O	Output current (leakage) (see Note 3)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}			±10		±10	µA
I_{CC1}	Operating current §	See Note 4	Standby		165		160	mA
I_{CC1A}	Operating current §	$t_{c(SC)}$ = MIN	Active		210		195	mA
I_{CC2}	Standby current	All clocks = V_{CC}	Standby		12		12	mA
I_{CC2A}	Standby current	$t_{c(SC)}$ = MIN	Active		70		65	mA
I_{CC3}	$\overline{RAS}$-only refresh current	See Note 4	Standby		165		160	mA
I_{CC3A}	$\overline{RAS}$-only refresh current	$t_{c(SC)}$ = MIN, See Note 4	Active		215		195	mA
I_{CC4}	Page-mode current §	$t_{c(P)}$ = MIN, See Note 5	Standby		100		95	mA
I_{CC4A}	Page-mode current §	$t_{c(SC)}$ = MIN, See Note 5	Active		145		130	mA
I_{CC5}	CBR current	See Note 4	Standby		165		160	mA
I_{CC5A}	CBR current	$t_{c(SC)}$ = MIN, See Note 4	Active		210		195	mA
I_{CC6}	Data-transfer current	See Note 4	Standby		180		170	mA
I_{CC6A}	Data-transfer current	$t_{c(SC)}$ = MIN	Active		225		200	mA

‡ For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

§ Measured with outputs open

NOTES: 3. $\overline{SE}$ is disabled for SQ output leakage tests.
4. Measured with one address change while $\overline{RAS}$ = V_{IL} and $t_{c(rd)}$, $t_{c(W)}$, $t_{c(TRD)}$ = MIN
5. Measured with one address change while $\overline{CASx}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A8		5	10	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		8	10	pF
$C_{i(W)}$	Input capacitance, $\overline{WEL}$ and $\overline{WEU}$		7	10	pF
$C_{i(SC)}$	Input capacitance, SC		6	10	pF
$C_{i(SE)}$	Input capacitance, $\overline{SE}$		7	10	pF
$C_{i(DSF)}$	Input capacitance, QSF		7	10	pF
$C_{i(TRG)}$	Input capacitance, $\overline{TRG}$		7	10	pF
$C_{o(O)}$	Output capacitance, SQ and DQ		12	15	pF
$C_{o(QSF)}$	Output capacitance, QSF		10	12	pF

NOTE 6: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		TEST CONDITIONS †	ALT. SYMBOL	'55166-70		'55166-80		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		20		20	ns
$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{AA}		35		40	ns
$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = MAX	t_{CPA}		40		45	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MAX	t_{RAC}		70		80	ns
$t_{a(G)}$	Access time of DQ from $\overline{TRG}$ low		t_{OEA}		20		20	ns
$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 30 pF	t_{SCA}		20		25	ns
$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		15		20	ns
$t_{dis(CH)}$	Disable time, random output from $\overline{CAS}$ high (see Note 8)	C_L = 50 pF	t_{OFF}	0	20	0	20	ns
$t_{dis(RH)}$	Disable time, random output from $\overline{RAS}$ high (see Note 8)	C_L = 50 pF		0	20	0	20	ns
$t_{dis(G)}$	Disable time, random output from $\overline{TRG}$ high (see Note 8)	C_L = 50 pF	t_{OEZ}	0	20	0	20	ns
$t_{dis(WL)}$	Disable time, random output from $\overline{WE}$ low (see Note 8)	C_L = 50 pF	t_{WEZ}	0	20	0	20	ns
$t_{dis(SE)}$	Disable time, serial output from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	0	15	0	20	ns

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

NOTES: 7. Switching times for RAM-port output are measured with a load equivalent to 1 TTL load and 50 pF. Data-out reference level: V_{OH}/V_{OL} = 2 V/0.8 V. Switching times for SAM-port output are measured with a load equivalent to 1 TTL load and 30 pF. Serial-data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V.

8. $t_{dis(CH)}$, $t_{dis(RH)}$, $t_{dis(G)}$, $t_{dis(WL)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature†

		ALT. SYMBOL	'55166-70		'55166-80		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Cycle time, read	t_{RC}	130		150		ns
$t_{c(W)}$	Cycle time, write	t_{WC}	130		150		ns
$t_{c(rdW)}$	Cycle time, read-modify-write	t_{RMW}	175		200		ns
$t_{c(P)}$	Cycle time, page-mode read, write	t_{PC}	45		50		ns
$t_{c(RDWP)}$	Cycle time, page-mode read-modify-write	t_{PRMW}	85		90		ns
$t_{c(TRD)}$	Cycle time, transfer read	t_{RC}	130		150		ns
$t_{c(SC)}$	Cycle time, SC (see Note 9)	t_{SCC}	22		30		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CPN}	10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 10)	t_{CAS}	20	10 000	20	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	50		60		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 11)	t_{RAS}	70	10 000	80	10 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{WEx}$ low	t_{WP}	10		15		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		20		20		ns
$t_{w(SCH)}$	Pulse duration, SC high	t_{SC}	8		10		ns
$t_{w(SCL)}$	Pulse duration, SC low	t_{SCP}	8		10		ns
$t_{w(GH)}$	Pulse duration, $\overline{TRG}$ high	t_{TP}	20		20		ns
$t_{w(RL)P}$	Pulse duration, $\overline{RAS}$ low (page mode)	t_{RASP}	70	100 000	80	100 000	ns
$t_{su(CA)}$	Setup time, column address before $\overline{CAS}$ low	t_{ASC}	0		0		ns
$t_{su(SFC)}$	Setup time, DSF before $\overline{CAS}$ low	t_{FSC}	0		0		ns
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low	t_{ASR}	0		0		ns
$t_{su(WMR)}$	Setup time, $\overline{WEx}$ before $\overline{RAS}$ low	t_{WSR}	0		0		ns
$t_{su(DQR)}$	Setup time, DQ before $\overline{RAS}$ low	t_{MS}	0		0		ns
$t_{su(TRG)}$	Setup time, $\overline{TRG}$ high before $\overline{RAS}$ low	t_{THS}	0		0		ns
$t_{su(SFR)}$	Setup time, DSF low before $\overline{RAS}$ low	t_{FSR}	0		0		ns
$t_{su(DCL)}$	Setup time, data valid before $\overline{CAS}$ low	t_{DSC}	0		0		ns
$t_{su(DWL)}$	Setup time, data valid before $\overline{WEx}$ low	t_{DSW}	0		0		ns
$t_{su(rd)}$	Setup time, read command, $\overline{WEx}$ high before $\overline{CAS}$ low	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Setup time, early write command, $\overline{WEx}$ low before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Setup time, $\overline{WEx}$ low before $\overline{CAS}$ high, write	t_{CWL}	15		20		ns
$t_{su(WRH)}$	Setup time, $\overline{WEx}$ low before $\overline{RAS}$ high, write	t_{RWL}	20		20		ns
$t_{h(CLCA)}$	Hold time, column address after $\overline{CAS}$ low	t_{CAH}	10		15		ns
$t_{h(SFC)}$	Hold time, DSF after $\overline{CAS}$ low	t_{CFH}	15		15		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. Cycle time assumes t_t = 3 ns.

10. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this can require additional $\overline{CAS}$ low time [$t_{w(CL)}$].

11. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this can require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

			ALT. SYMBOL	'55166-70		'55166-80		UNIT
				MIN	MAX	MIN	MAX	
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low		t_{RAH}	10		10		ns
$t_{h(TRG)}$	Hold time, $\overline{TRG}$ after $\overline{RAS}$ low		t_{THH}	15		15		ns
$t_{h(RWM)}$	Hold time, write mask after $\overline{RAS}$ low		t_{RWH}	15		15		ns
$t_{h(RDQ)}$	Hold time, DQ after $\overline{RAS}$ low (write-mask operation)		t_{MH}	15		15		ns
$t_{h(SFR)}$	Hold time, DSF after $\overline{RAS}$ low		t_{RFH}	10		10		ns
$t_{h(RLCA)}$	Hold time, column address valid after $\overline{RAS}$ low (see Note 12)		t_{AR}	30		35		ns
$t_{h(CLD)}$	Hold time, data valid after $\overline{CAS}$ low		t_{DH}	15		15		ns
$t_{h(RLD)}$	Hold time, data valid after $\overline{RAS}$ low (see Note 12)		t_{DHR}	35		35		ns
$t_{h(WLD)}$	Hold time, data valid after $\overline{WEx}$ low		t_{DH}	15		15		ns
$t_{h(CHrd)}$	Hold time, read, $\overline{WEx}$ high after $\overline{CAS}$ high (see Note 13)		t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Hold time, read, $\overline{WEx}$ high after $\overline{RAS}$ high (see Note 13)		t_{RRH}	0		0		ns
$t_{h(CLW)}$	Hold time, write, $\overline{WEx}$ low after $\overline{CAS}$ low		t_{WCH}	15		15		ns
$t_{h(RLW)}$	Hold time, write, $\overline{WEx}$ low after $\overline{RAS}$ low (see Note 12)		t_{WCR}	35		35		ns
$t_{h(WLG)}$	Hold time, $\overline{TRG}$ high after $\overline{WEx}$ low (see Note 14)		t_{OEH}	10		10		ns
$t_{h(SHSQ)}$	Hold time, SQ after SC high		t_{SOH}	2		2		ns
$t_{h(RSF)}$	Hold time, DSF after $\overline{RAS}$ low		t_{FHR}	35		35		ns
$t_{h(CLQ)}$	Hold time, Output after $\overline{CAS}$ low		t_{DHC}	0		0		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		t_{CSH}	70		80		ns
		See Note 15	t_{CHR}	10		15		
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		t_{CRP}	0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		t_{RSH}	20		20		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{WEx}$ low (see Notes 16 and 17)		t_{CWD}	45		50		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 18)		t_{RCD}	20	50	20	60	ns
$t_{d(CARH)}$	Delay time, column address valid to $\overline{RAS}$ high		t_{RAL}	35		40		ns
$t_{d(CACH)}$	Delay time, column address valid to $\overline{CAS}$ high		t_{CAL}	35		40		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{WEx}$ low (see Note 16)		t_{RWD}	85		100		ns
$t_{d(CAWL)}$	Delay time, column address valid to $\overline{WEx}$ low (see Note 16)		t_{AWD}	60		65		ns
$t_{d(CLRL)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 15)		t_{CSR}	0		0		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 15)		t_{RPC}	0		0		ns
$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high for DRAM read cycles			20		20		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ		t_{OED}	15		15		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
14. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
15. CBR refresh operation only
16. Read-modify-write operation only
17. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
18. The maximum value is specified only to assure $\overline{RAS}$ access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	'55166-70		'55166-80		UNIT
			MIN	MAX	MIN	MAX	
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (see Note 19)	t_{RTH}	55		60		ns
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 20)	t_{RSD}	70		80		ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address valid	t_{RAD}	15	35	15	40	ns
$t_{d(GLRH)}$	Delay time, $\overline{TRG}$ low to $\overline{RAS}$ high	t_{ROH}	20		20		ns
$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 20)	t_{CSD}	20		25		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 19 and 20)	t_{TSL}	5		5		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 19)	t_{TRD}	−10		−10		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 21)	t_{TRP}	50		60		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 19)	t_{TSD}	15		20		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split-register-transfer read cycles		20		20		ns
$t_{d(CLTH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high in real-time-transfer read cycles	t_{CTH}	15		15		ns
$t_{d(CASH)}$	Delay time, column address to first SC in early-load-transfer read cycles	t_{ASD}	25		30		ns
$t_{d(CAGH)}$	Delay time, column address to $\overline{TRG}$ high in real-time-transfer read cycles	t_{ATH}	20		20		ns
$t_{d(DCL)}$	Delay time, data to $\overline{CAS}$ low	t_{DZC}	0		0		ns
$t_{d(DGL)}$	Delay time, data to $\overline{TRG}$ low	t_{DZO}	0		0		ns
$t_{d(MSRL)}$	Delay time, last (most significant) rising edge of SC to $\overline{RAS}$ low before boundary switch during split-transfer read cycles		20		20		ns
$t_{d(SCQSF)}$	Delay time, last (127 or 255) rising edge of SC to QSF switching at the boundary during split-register-transfer read cycles (see Note 22)	t_{SQD}		25		30	ns
$t_{d(CLQSF)}$	Delay time, $\overline{CAS}$ low to QSF switching in transfer read cycles (see Note 22)	t_{CQD}		30		35	ns
$t_{d(GHQSF)}$	Delay time, $\overline{TRG}$ high to QSF switching in transfer read cycles (see Note 22)	t_{TQD}		25		30	ns
$t_{d(RLQSF)}$	Delay time, $\overline{RAS}$ low to QSF switching in transfer read cycles (see Note 22)	t_{RQD}		70		75	ns
$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8	ms
t_t	Transition time	t_T	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 19. Real-time-load transfer read or late-load-transfer read cycle only
20. Early-load-transfer read cycle only
21. Full-register-(read) transfer cycles only
22. Switching times for QSF output are measured with a load equivalent to 1 TTL load and 30 pF, and the output reference level is V_{OH} / V_{OL} = 2 V/0.8 V.

PARAMETER MEASUREMENT INFORMATION

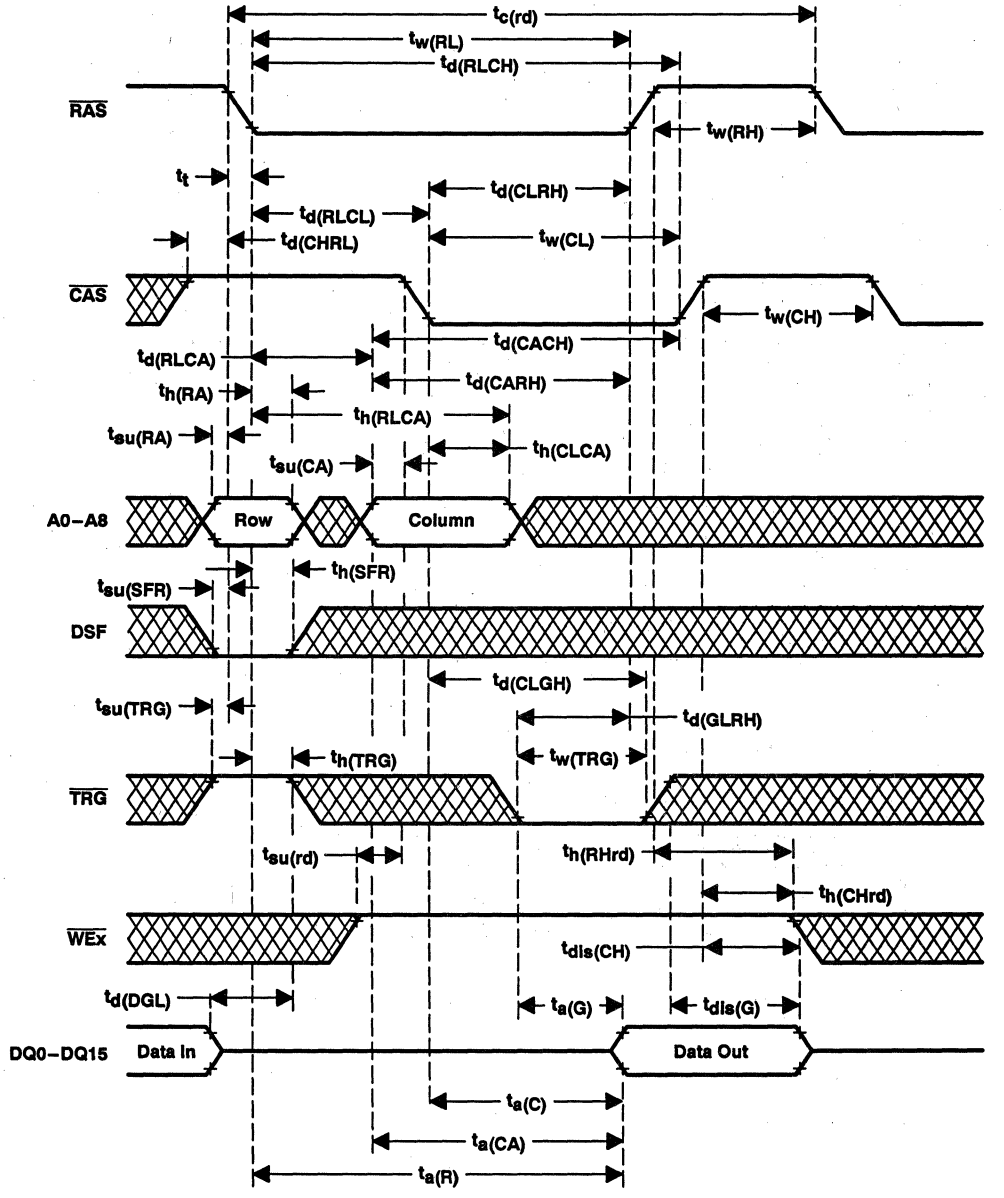


Figure 26. Read-Cycle Timing With $\overline{CAS}$-Controlled Output

PARAMETER MEASUREMENT INFORMATION

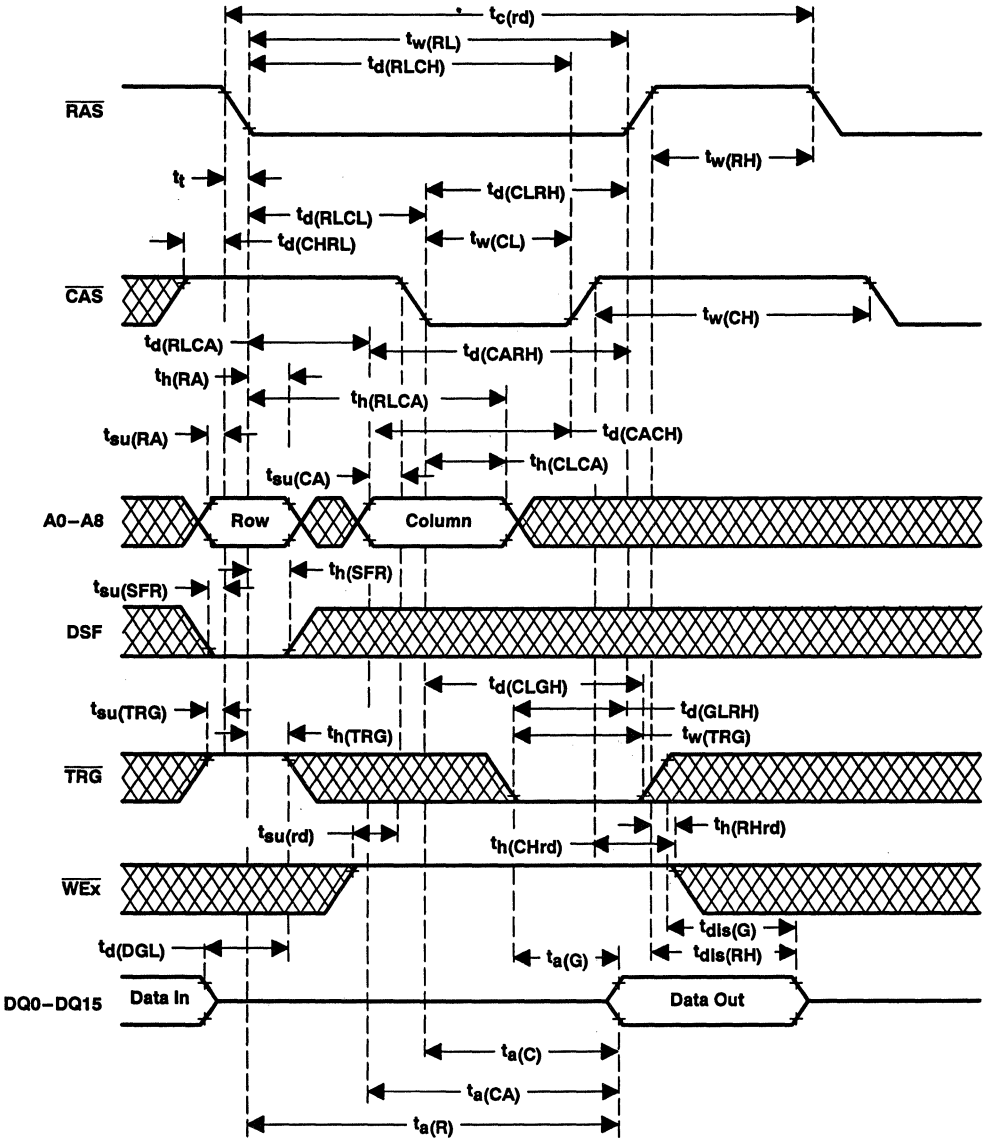


Figure 27. Read-Cycle Timing With $\overline{RAS}$-Controlled Output

PARAMETER MEASUREMENT INFORMATION

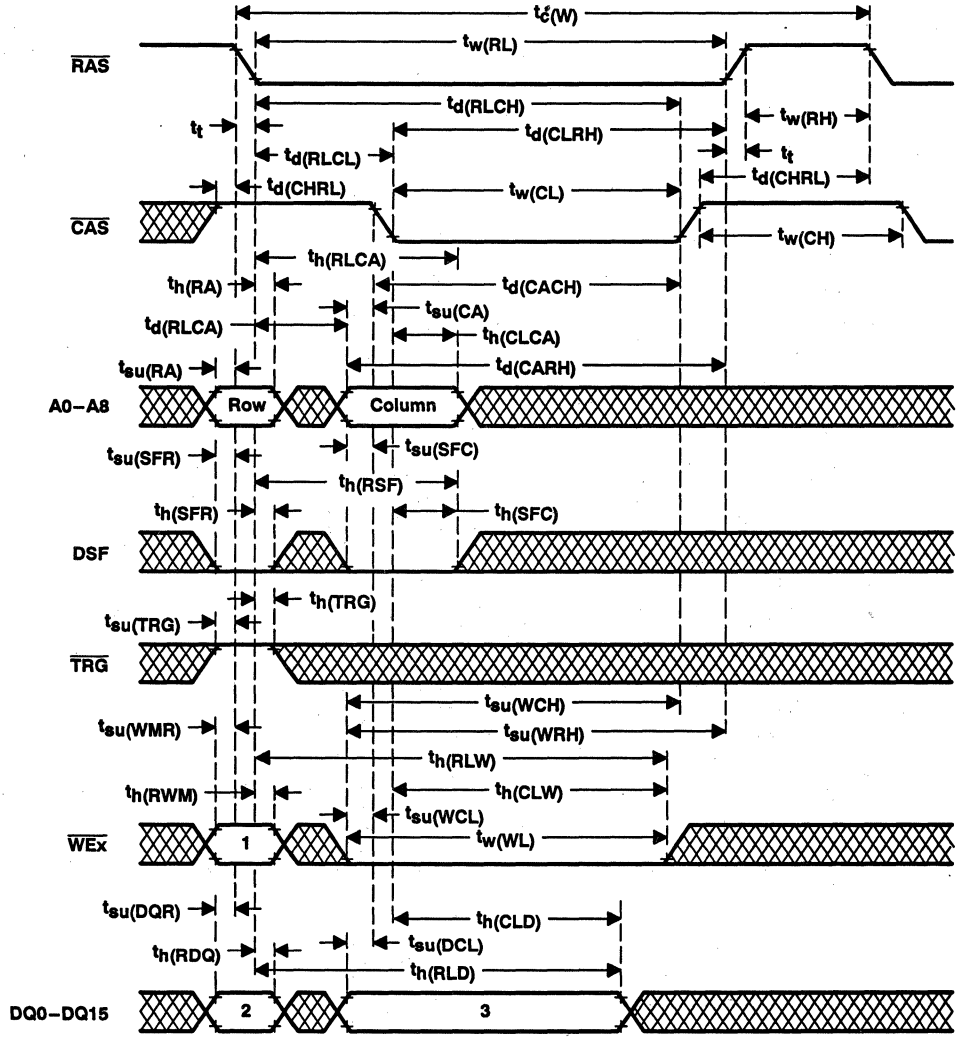


Figure 28. Early-Write-Cycle Timing

Table 5. Early-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

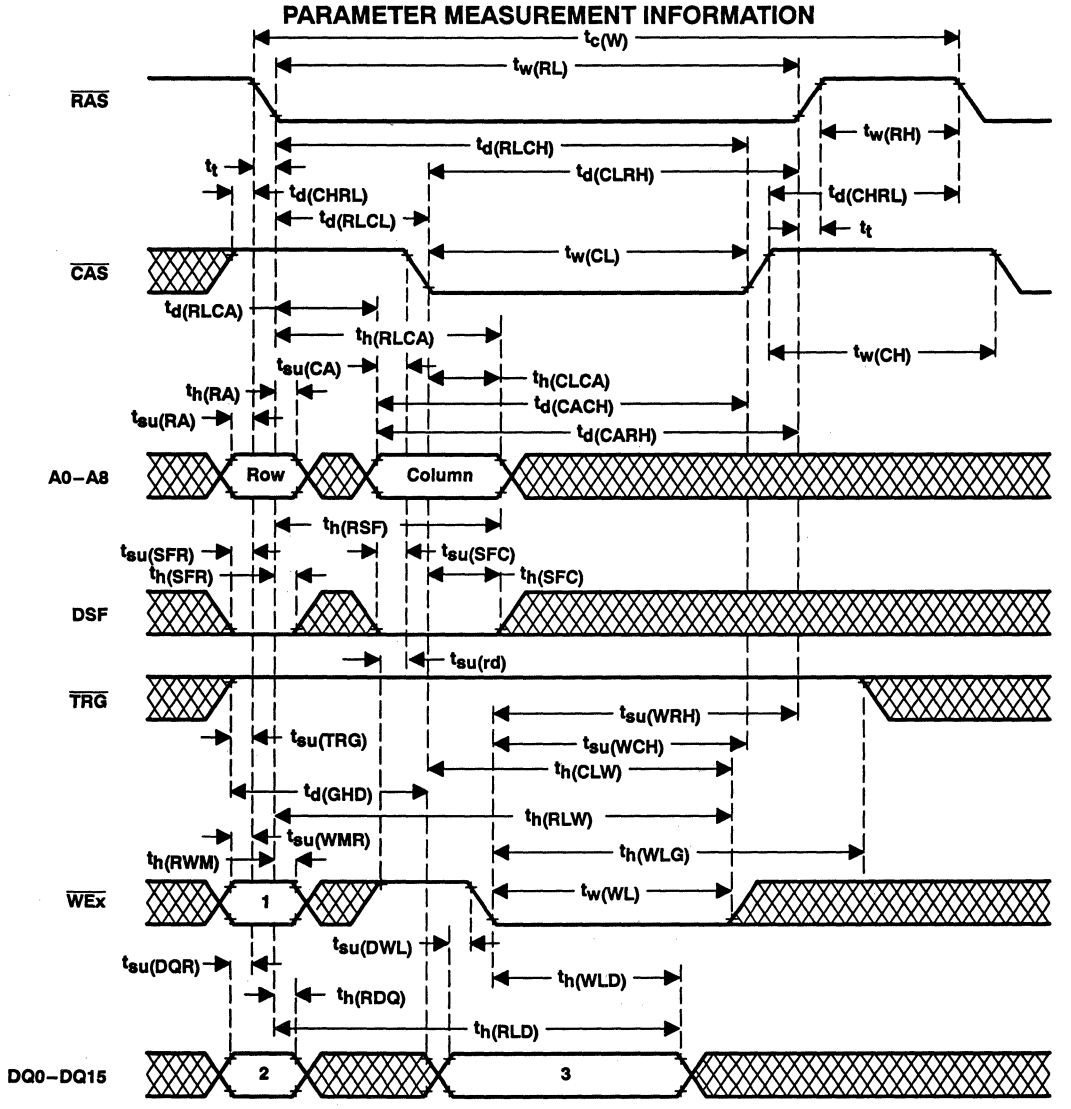
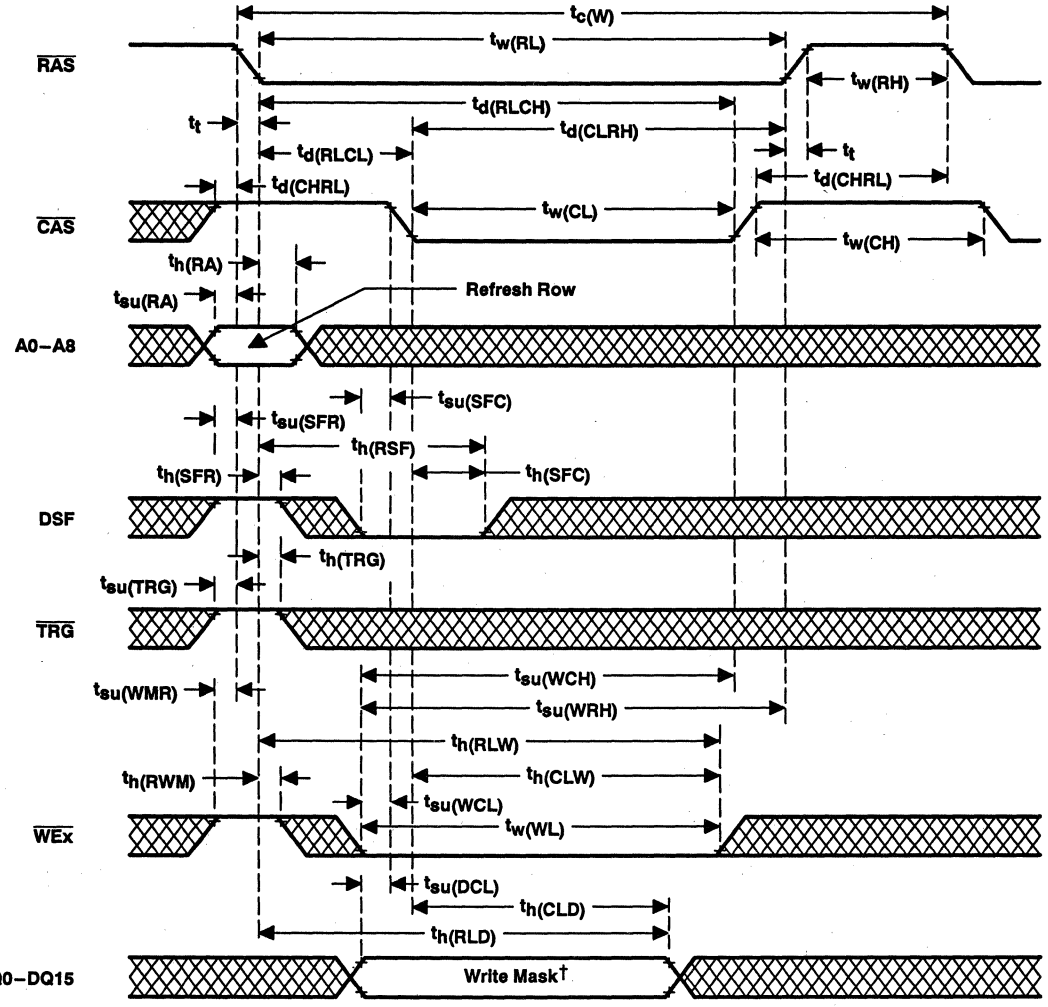


Figure 29. Late-Write-Cycle Timing (Output-Enable-Controlled Write)

Table 6. Late-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

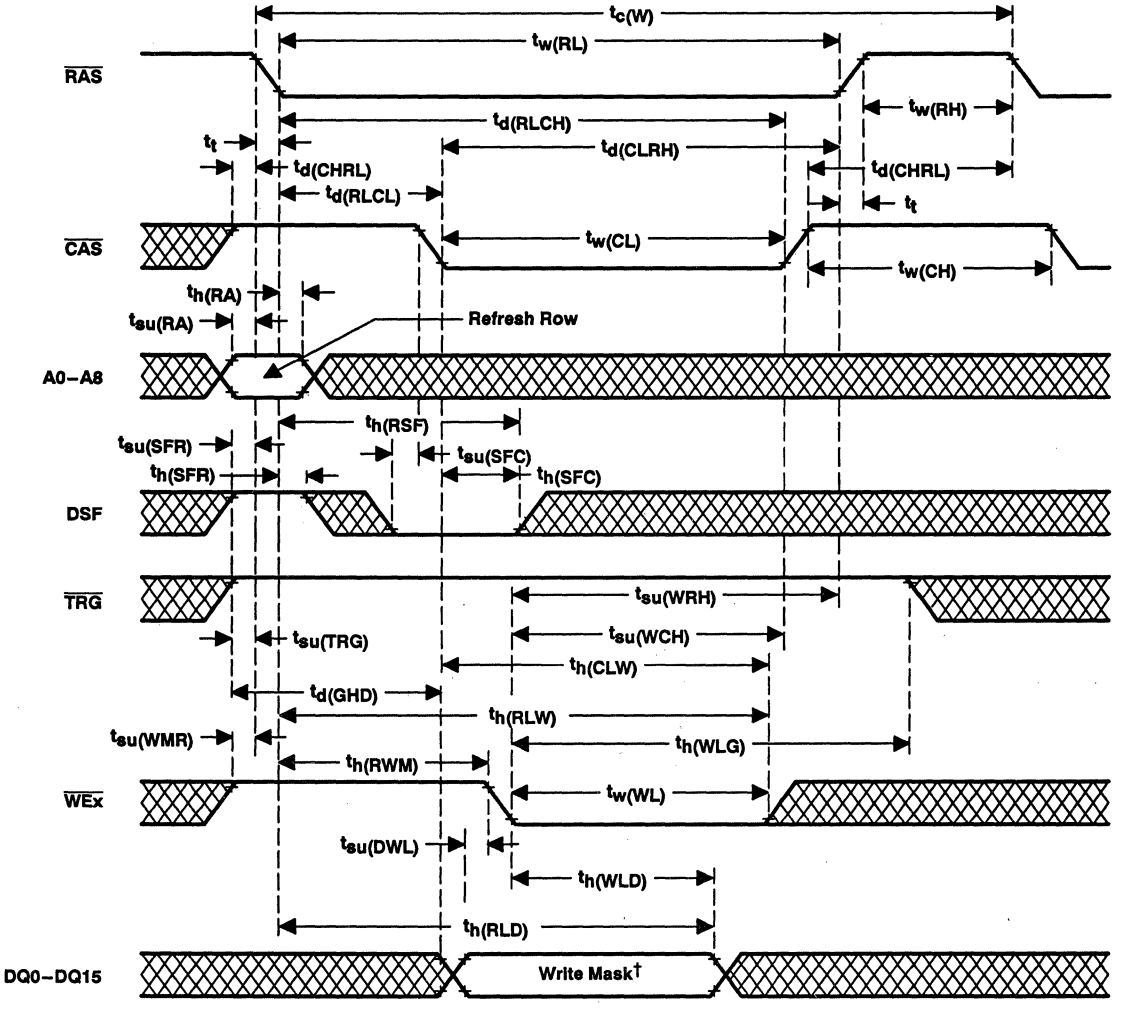
PARAMETER MEASUREMENT INFORMATION



† Load-write-mask-register cycle puts the device into the persistent write-per-bit mode.

Figure 30. Load-Write-Mask-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION



† Load-write-mask-register cycle puts the device into the persistent write-per-bit mode.

Figure 31. Load-Write-Mask-Register-Cycle Timing (Late-Write Load)

PARAMETER MEASUREMENT INFORMATION

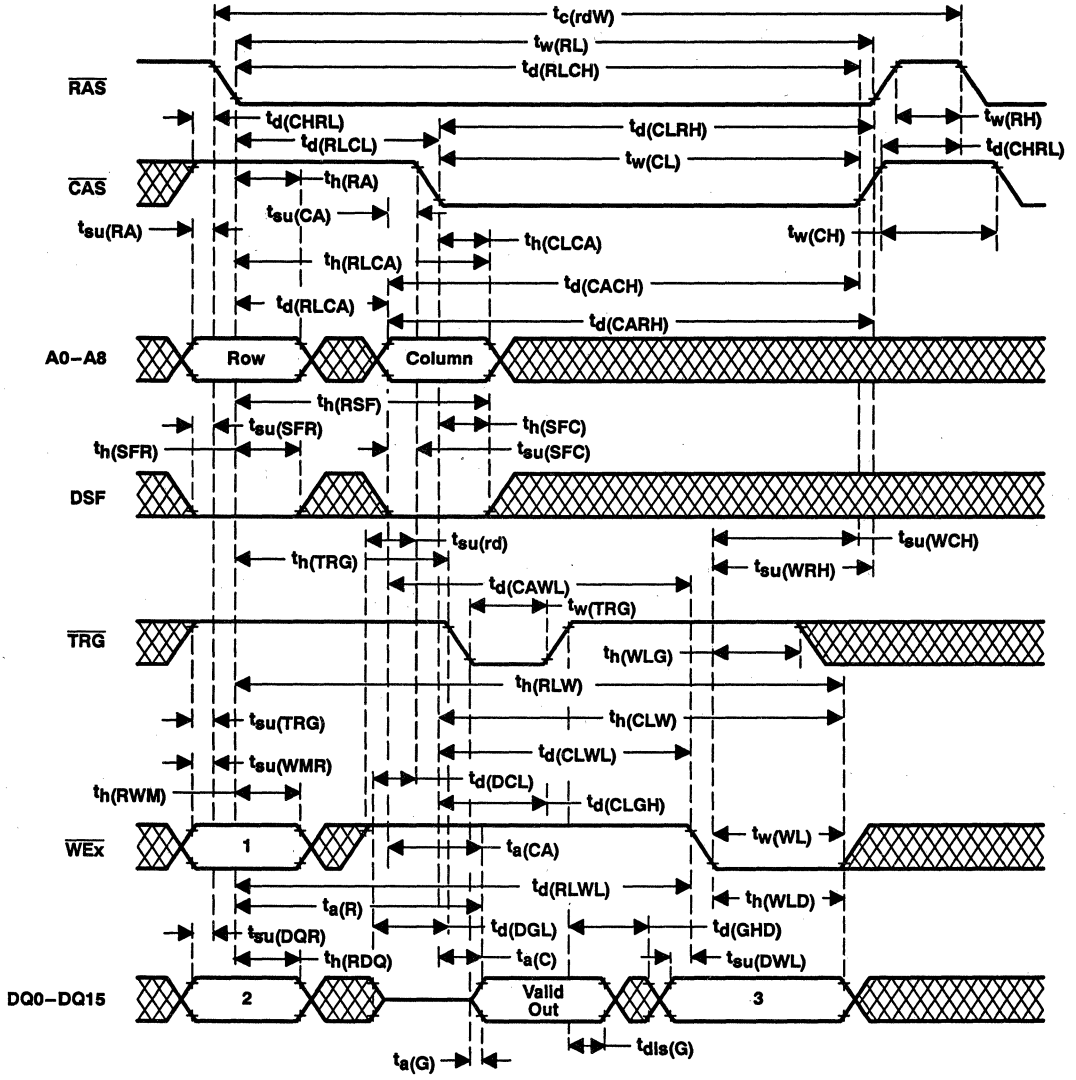
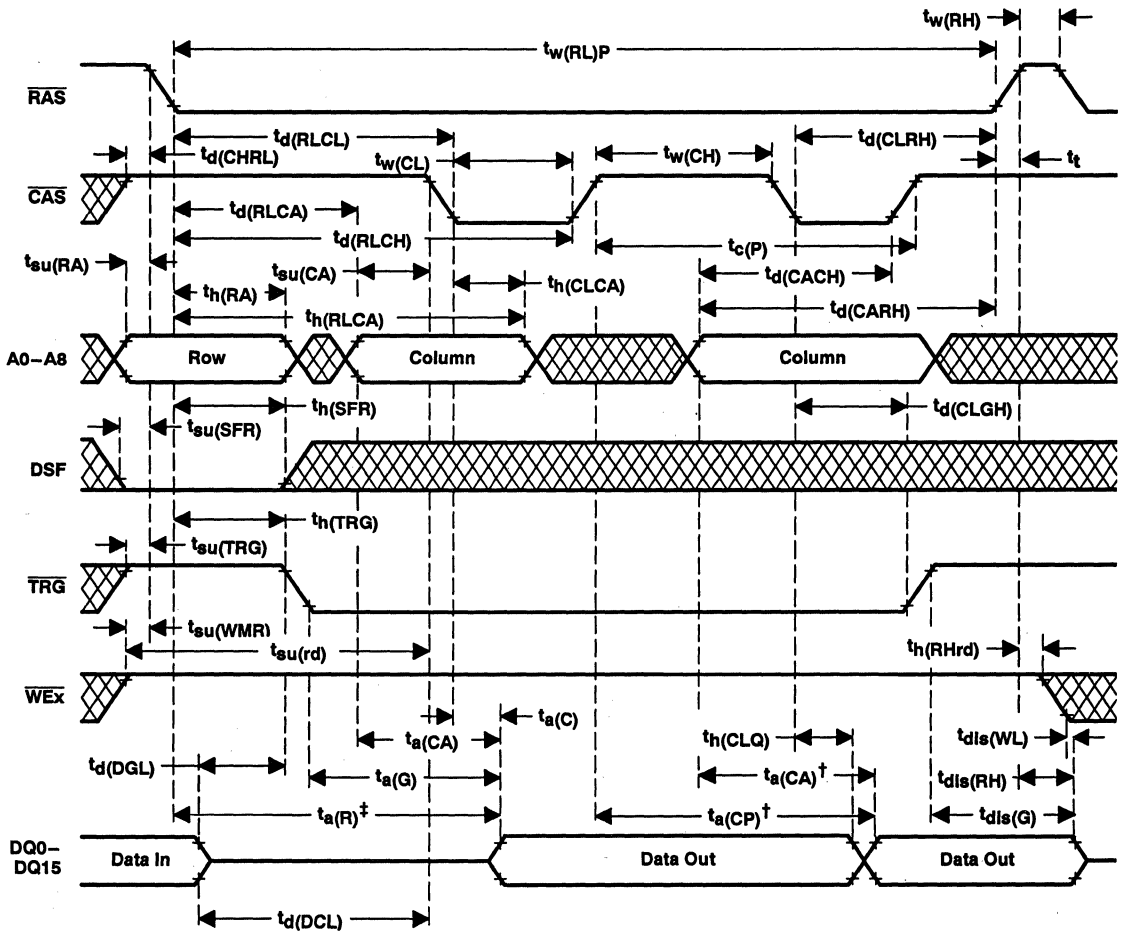


Figure 32. Read-Write-/Read-Modify-Write-Cycle Timing

Table 7. Read-Write-/Read-Modify-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

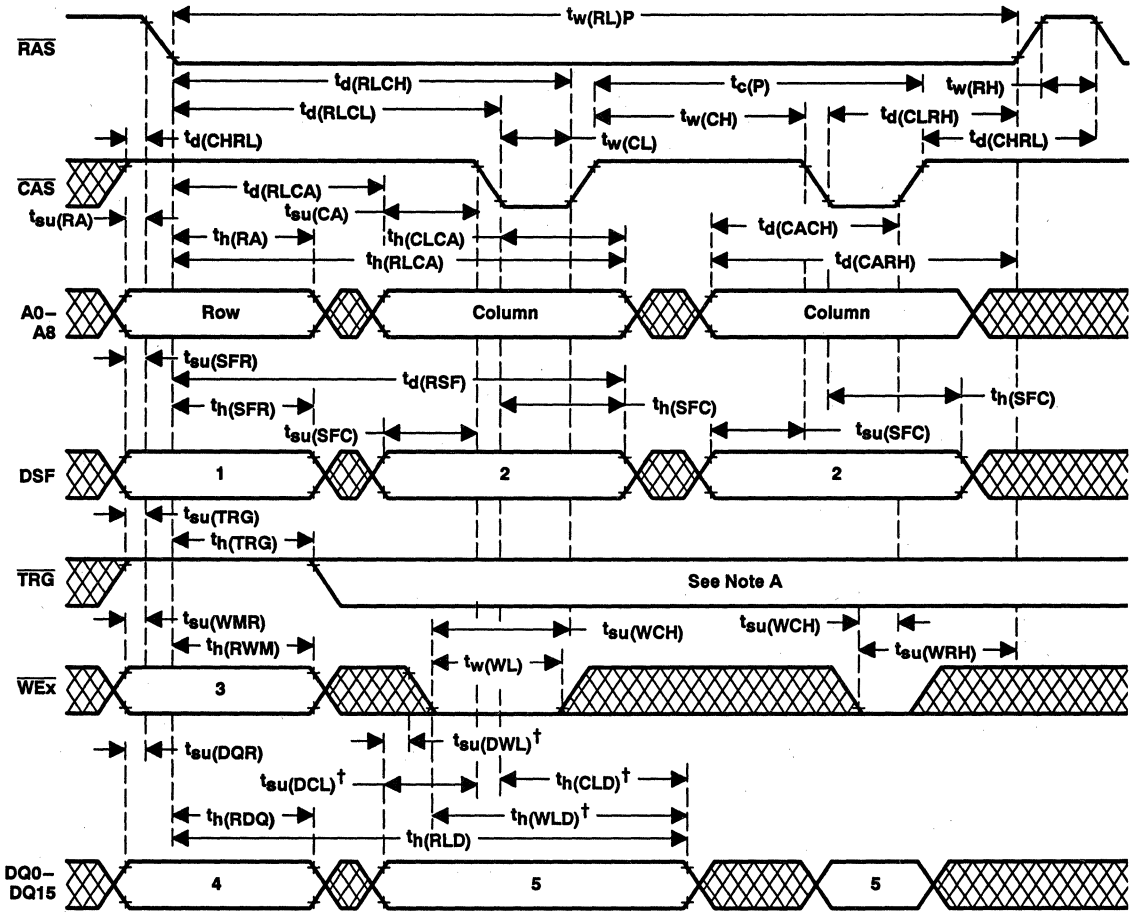
PARAMETER MEASUREMENT INFORMATION



† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.).

Figure 33. Enhanced-Page-Mode Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later

NOTE A: A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late-write feature is used. If the early-write-cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

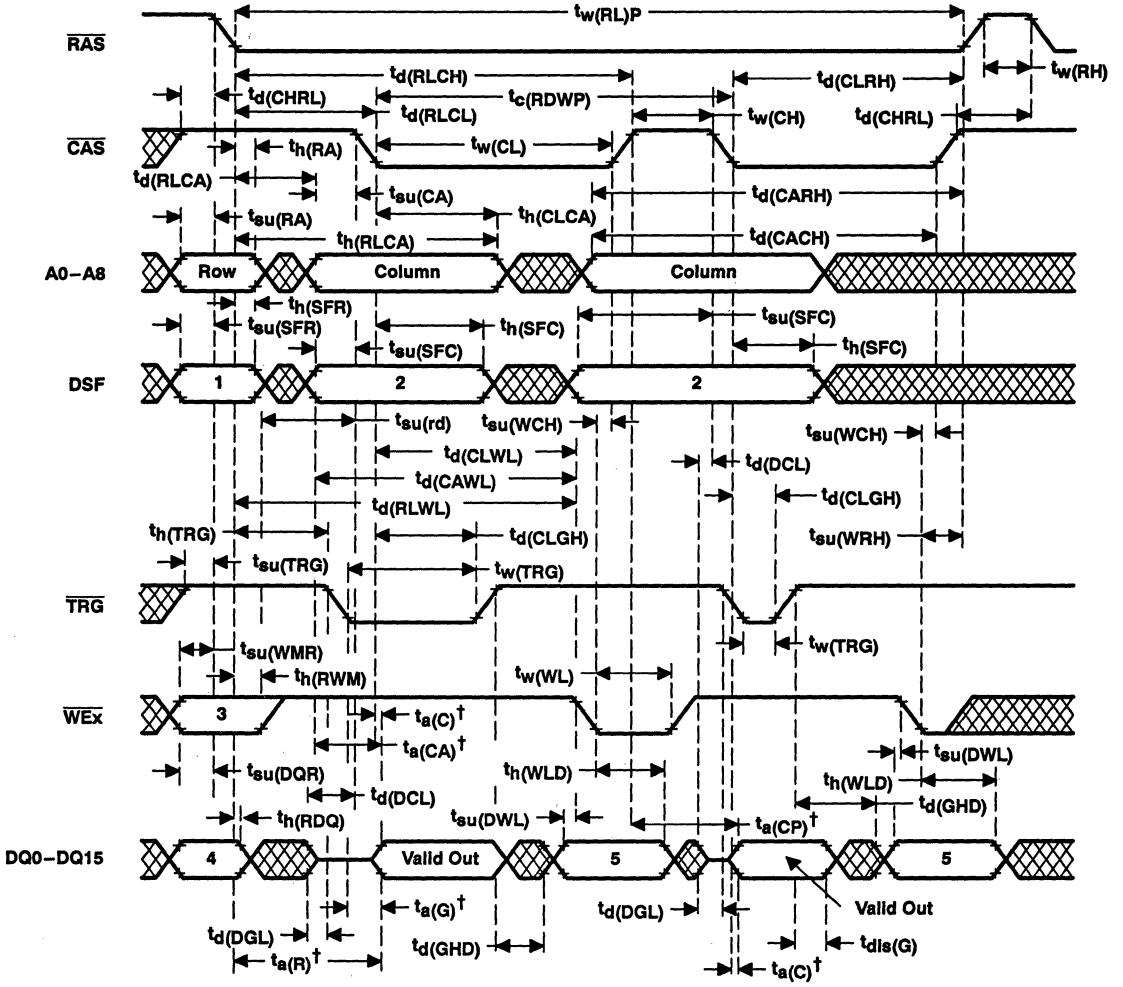
Figure 34. Enhanced-Page-Mode Write-Cycle Timing

Table 8. Enhanced-Page-Mode Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load-write-mask register on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load-write-mask-register cycle puts the device in the persistent write-per-bit mode. Column address at the falling edge of $\overline{CAS}$ is a don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



† Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

NOTE A: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

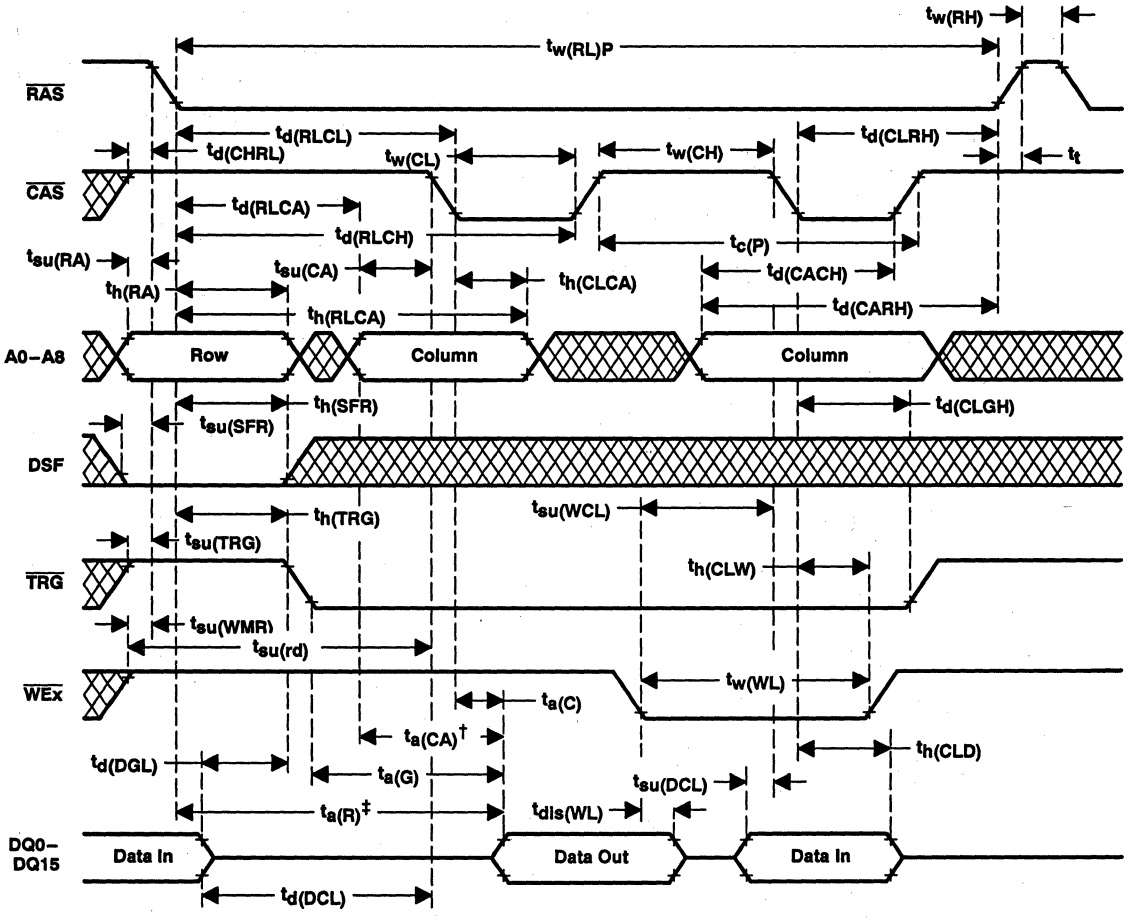
Figure 35. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

Table 9. Enhanced-Page-Mode Read-Modify-Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load-write-mask register on either the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load-write-mask-register cycle sets the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CAS}$ is a don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

‡ Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.).

Figure 36. Enhanced-Page-Mode Read-/Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

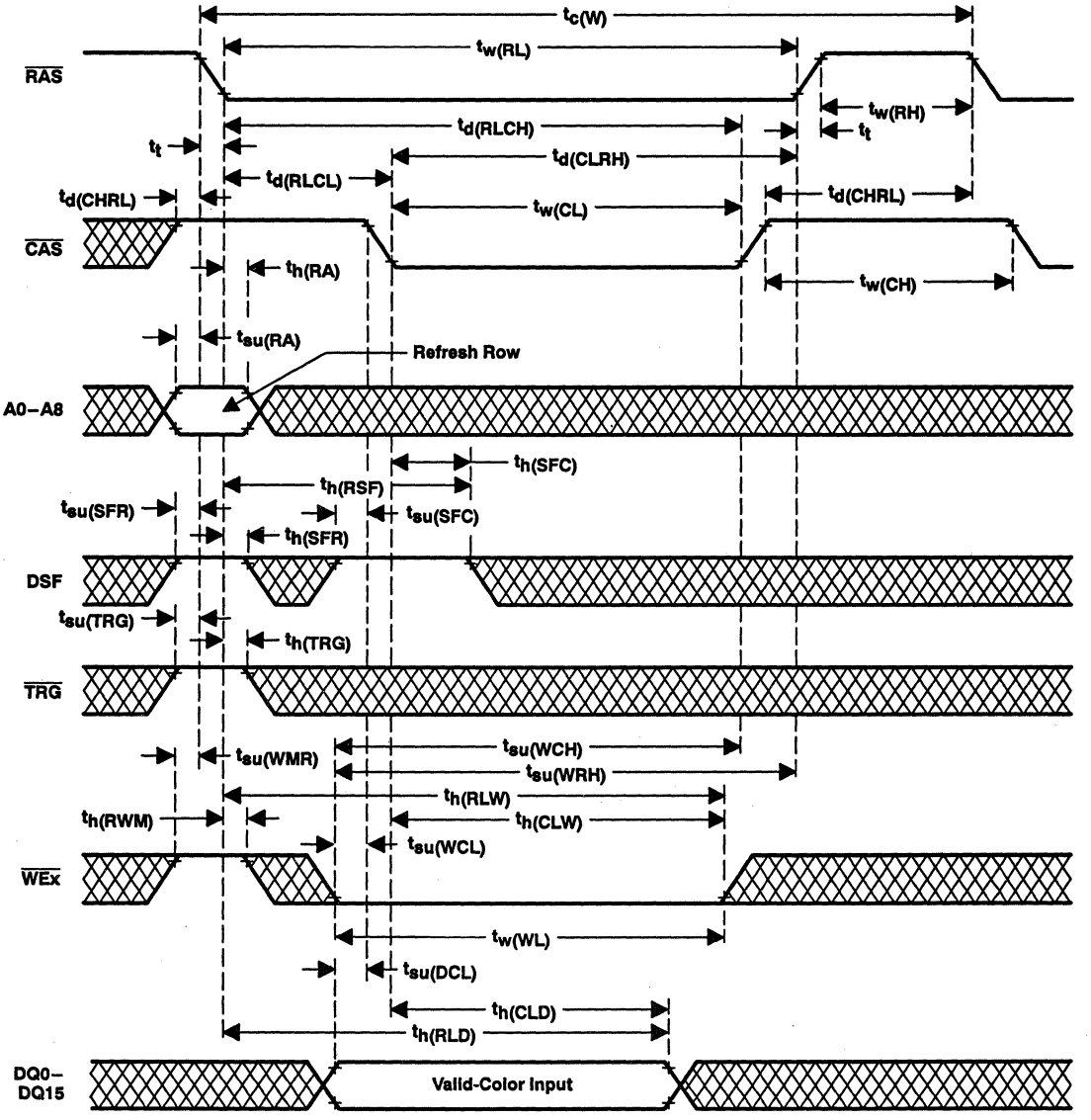


Figure 37. Load-Color-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION

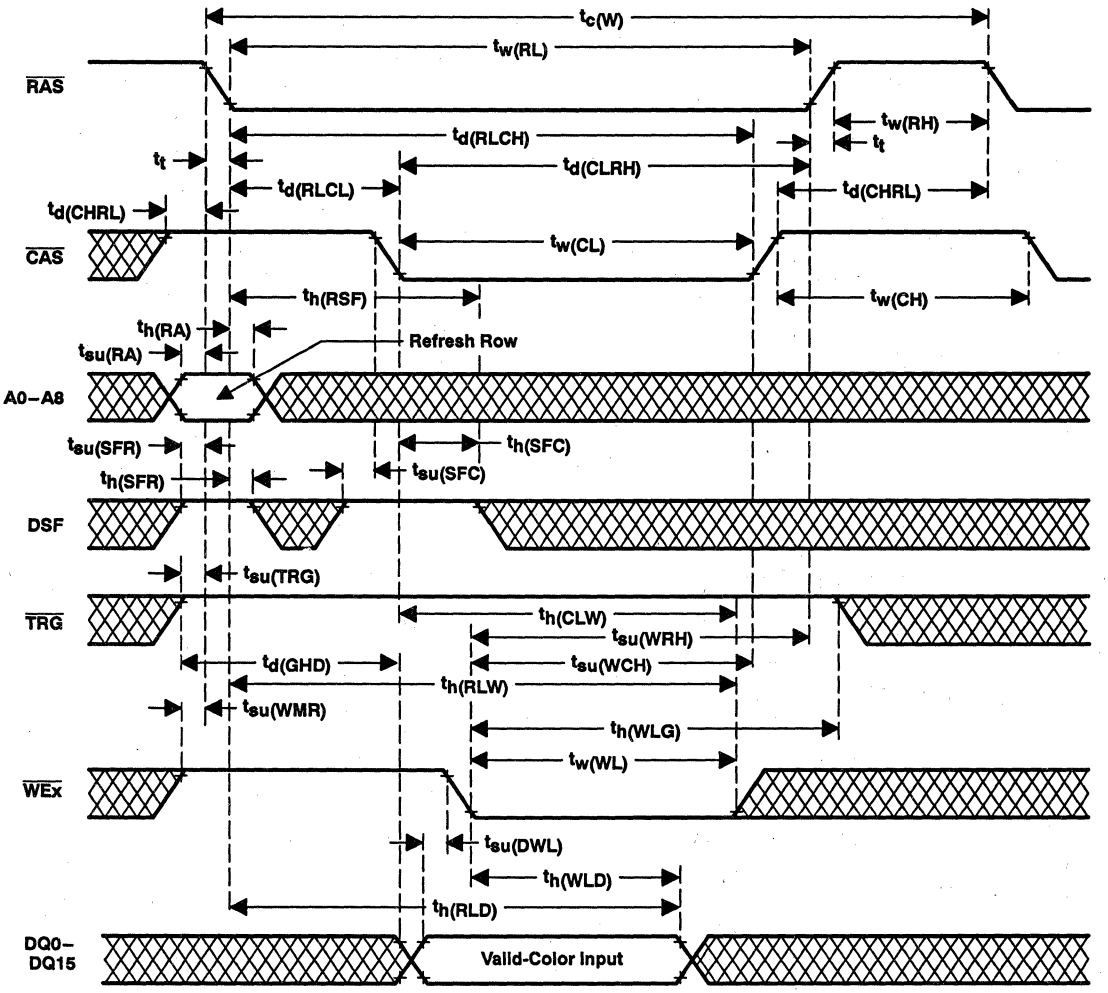


Figure 38. Load-Color-Register-Cycle Timing (Late-Write Load)

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PARAMETER MEASUREMENT INFORMATION

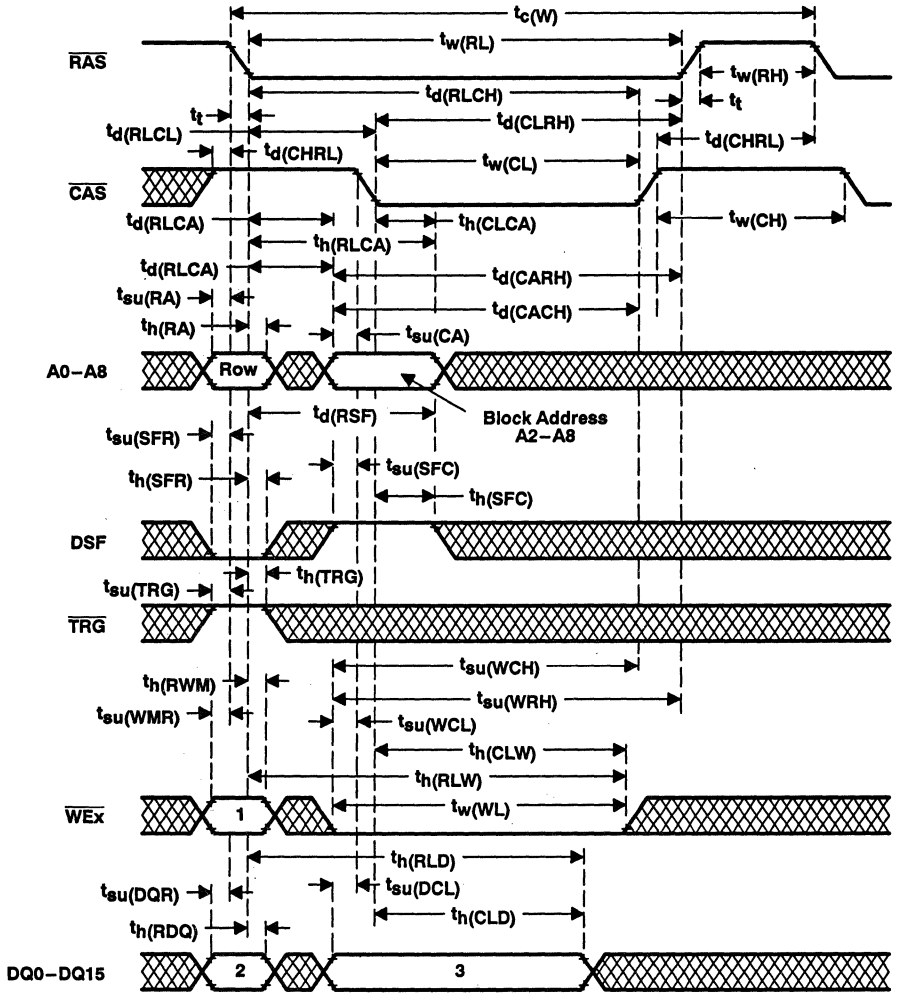


Figure 39. Block-Write-Cycle Timing (Early Write)

Table 10. Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi + 3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

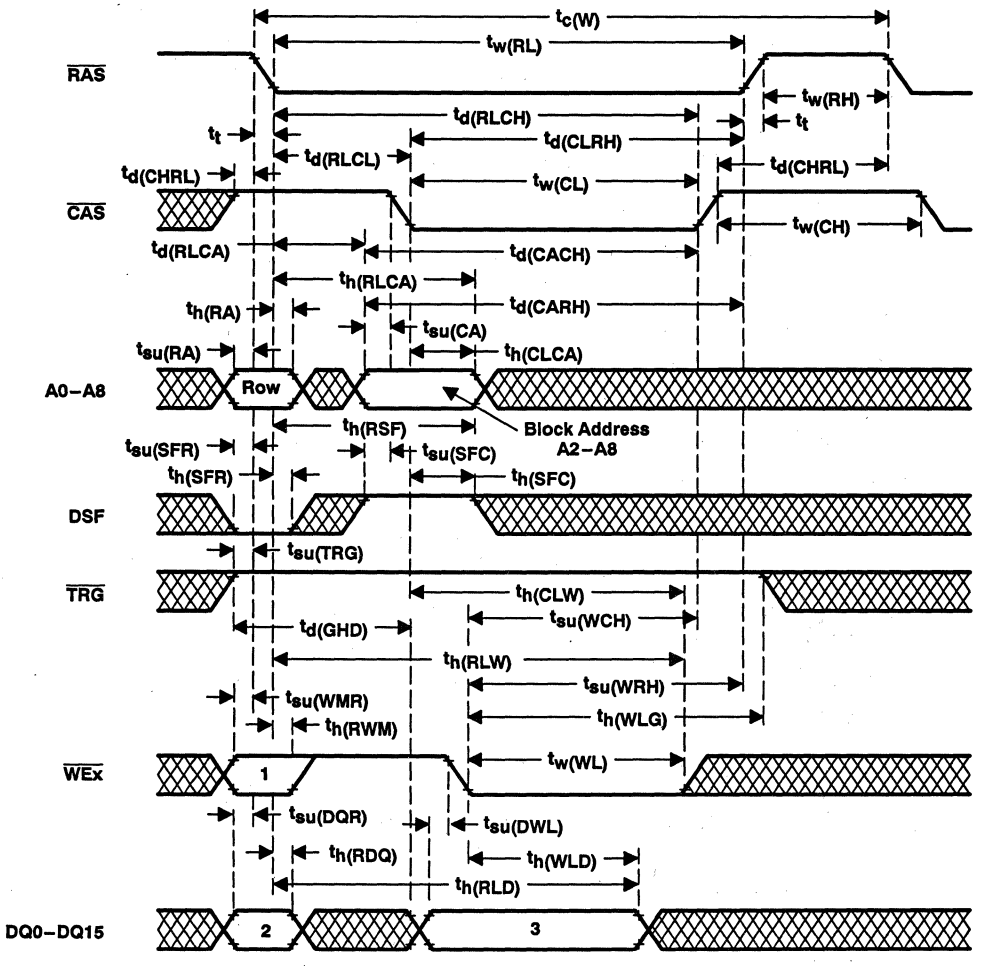


Figure 40. Block-Write-Cycle Timing (Late Write)

Table 11. Block-Write-Cycle State Table

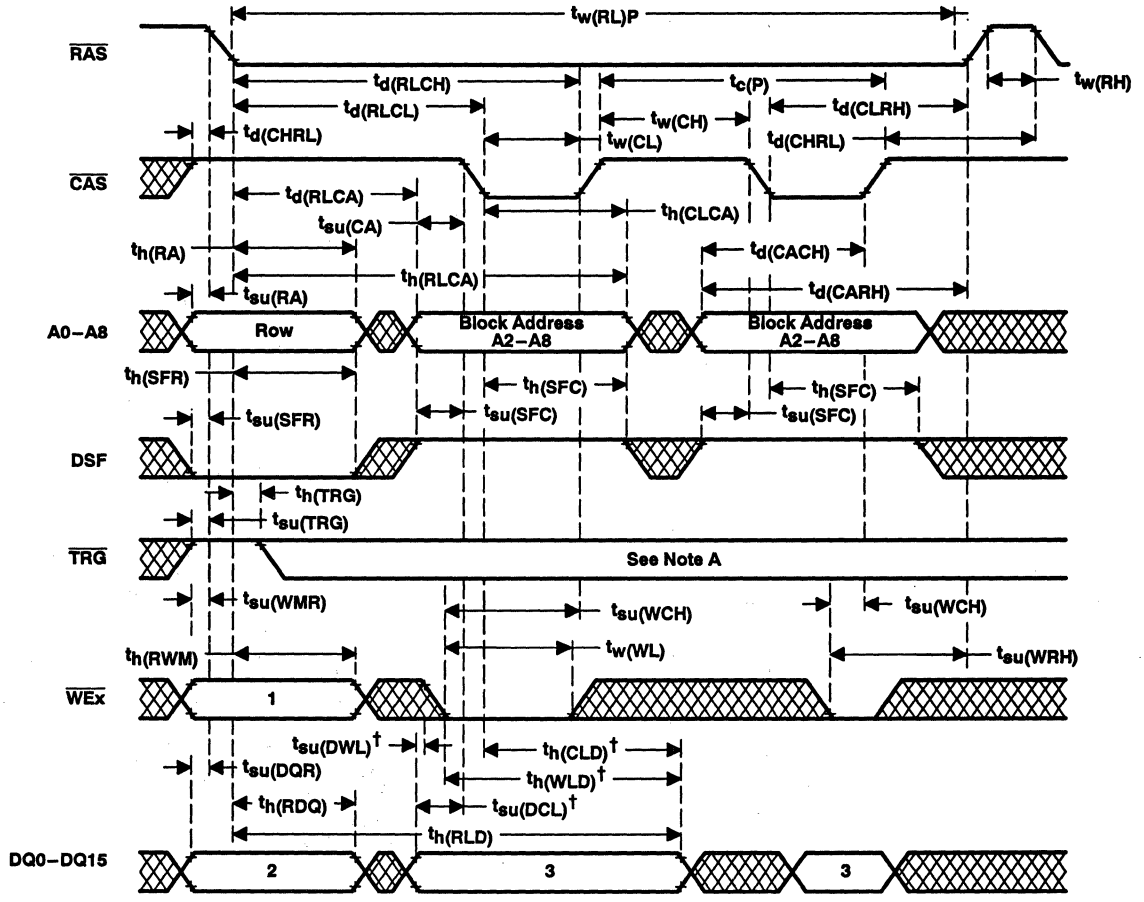
CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi + 3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first falling edge of $\overline{WEx}$ or the falling edge of $\overline{CAS}$, whichever occurs later

NOTE A: To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late-write feature is used. If the early write-cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 41. Enhanced-Page-Mode Block-Write-Cycle Timing

Table 12. Enhanced-Page-Mode Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi + 3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

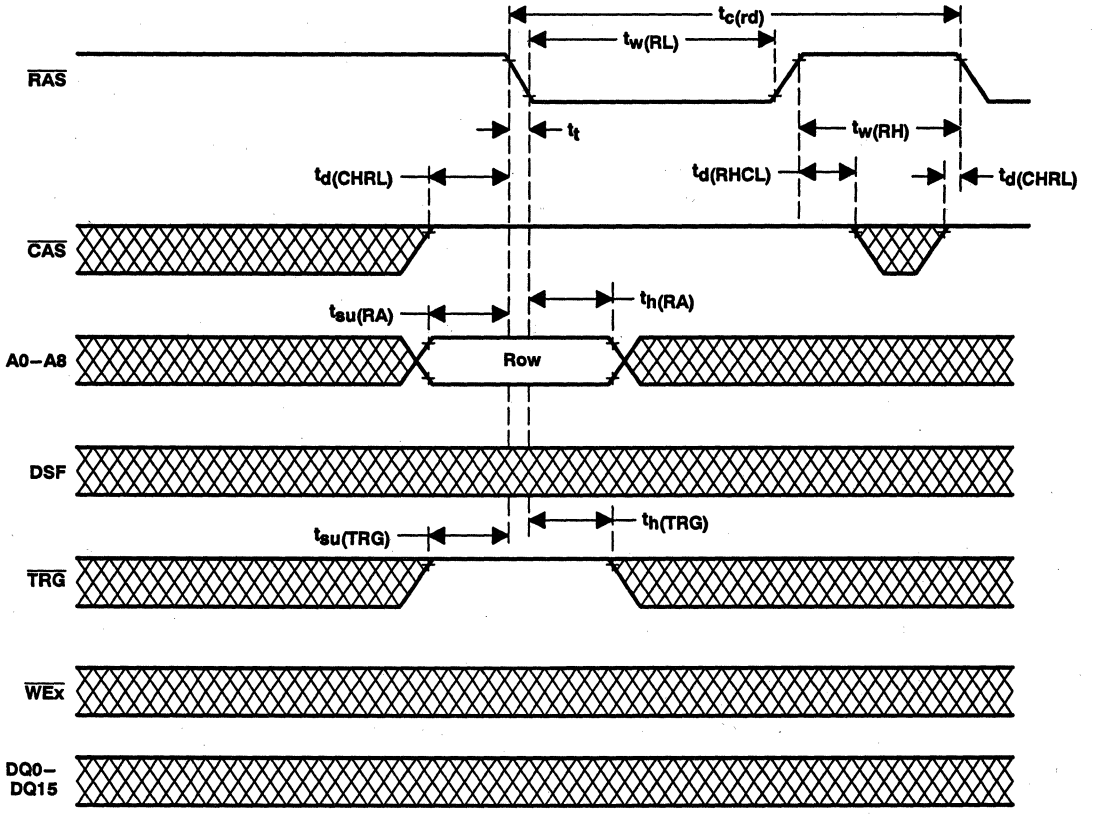


Figure 42. $\overline{RAS}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

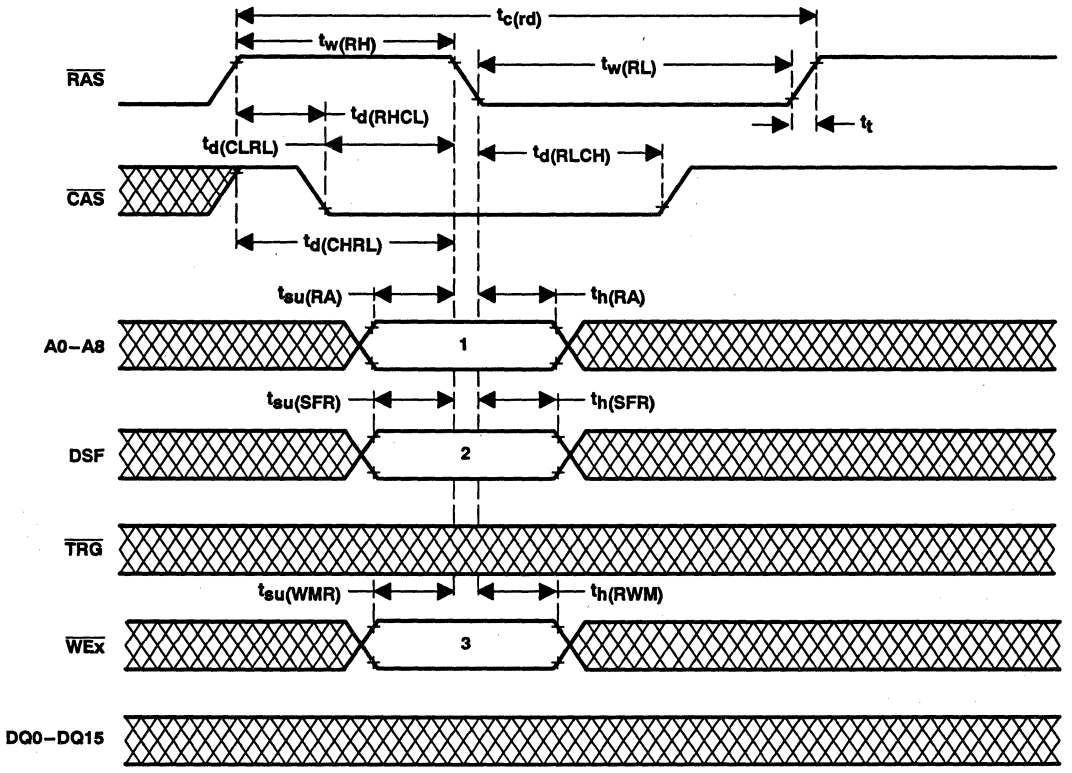


Figure 43. CBR-Refresh-Cycle Timing

Table 13. CBR-Cycle State Table

CYCLE	STATE		
	1	2	3
$\overline{\text{CBR}}$ refresh with option reset	Don't care	L	H
CBR refresh with no reset	Don't care	H	H
CBR refresh with stop-point set and no reset	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION

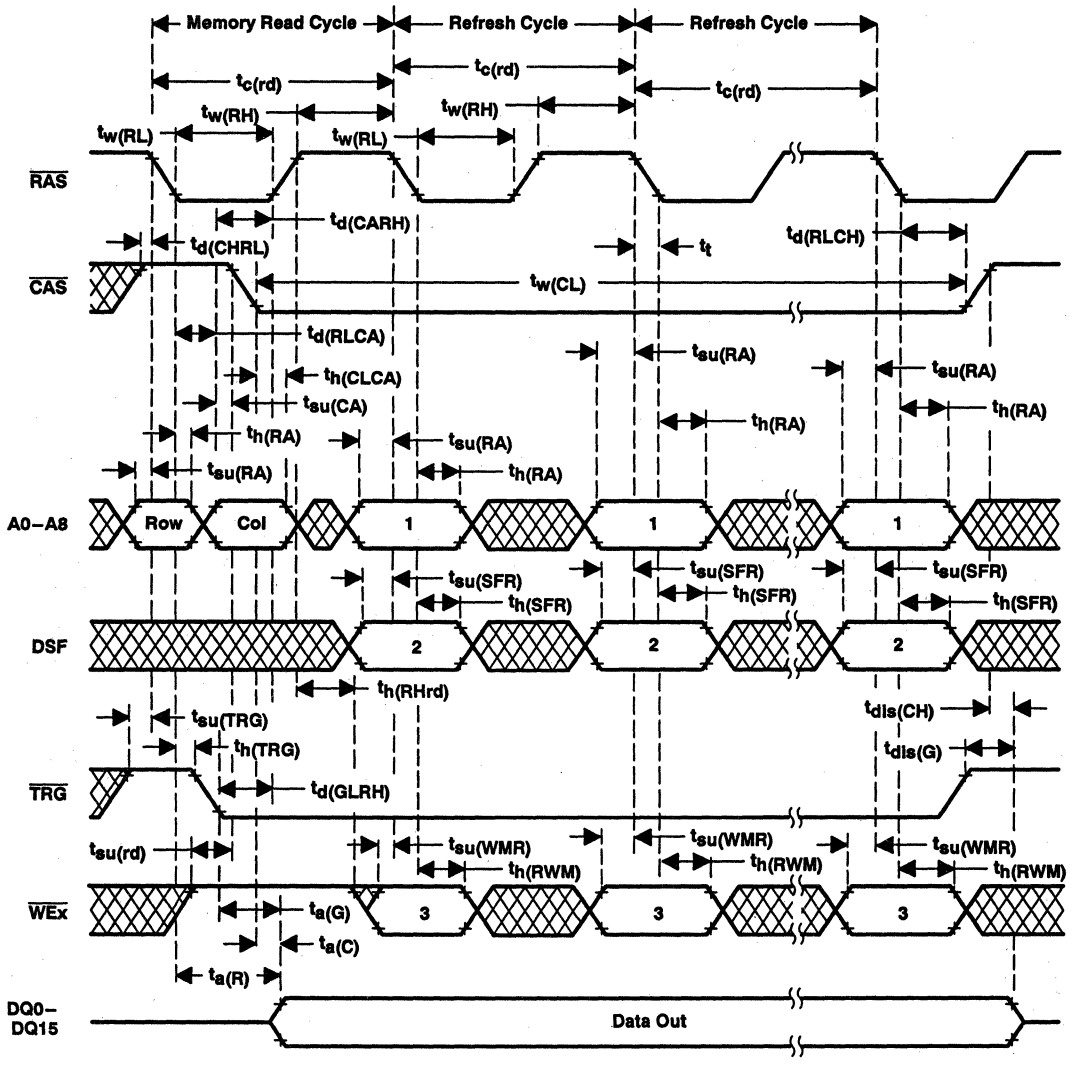
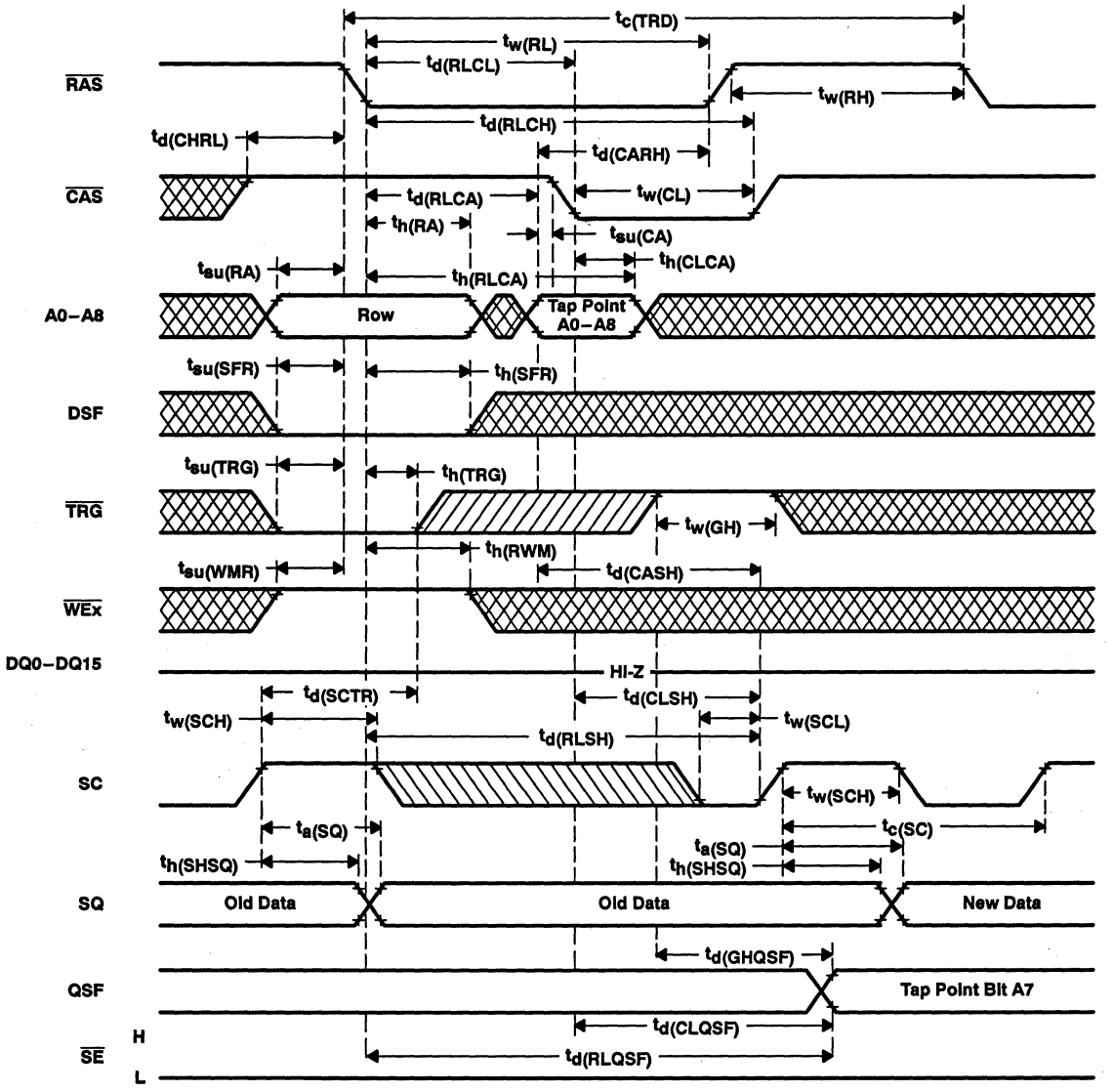


Figure 44. Hidden-Refresh-Cycle Timing

Table 14. Hidden-Refresh-Cycle State Table

CYCLE	STATE		
	1	2	3
CBR refresh with option reset	Don't care	L	H
CBR refresh with no reset	Don't care	H	H
CBR refresh with stop-point set and no option reset	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

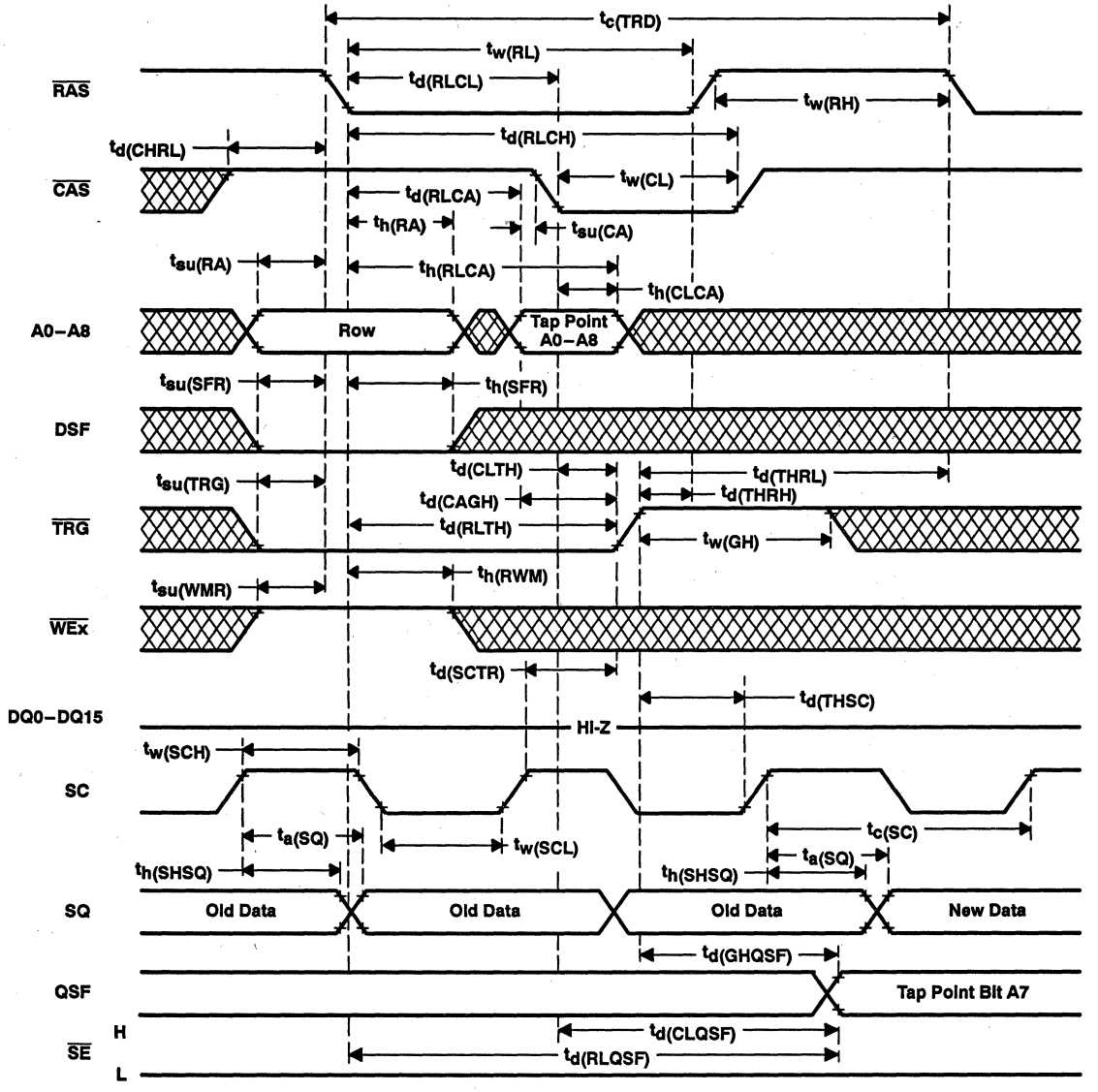
B. Once data is transferred into the data registers, the SAM is in the serial-read mode (i.e., the SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0–A7: register tap point; A8: identifies the DRAM row half

D. Early-load operation is defined as $t_{h(TRG)}$ min < $t_{h(TRG)}$ < $t_{d(RLTH)}$ min.

Figure 45. Full-Register-Transfer Read Timing, Early-Load Operations

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

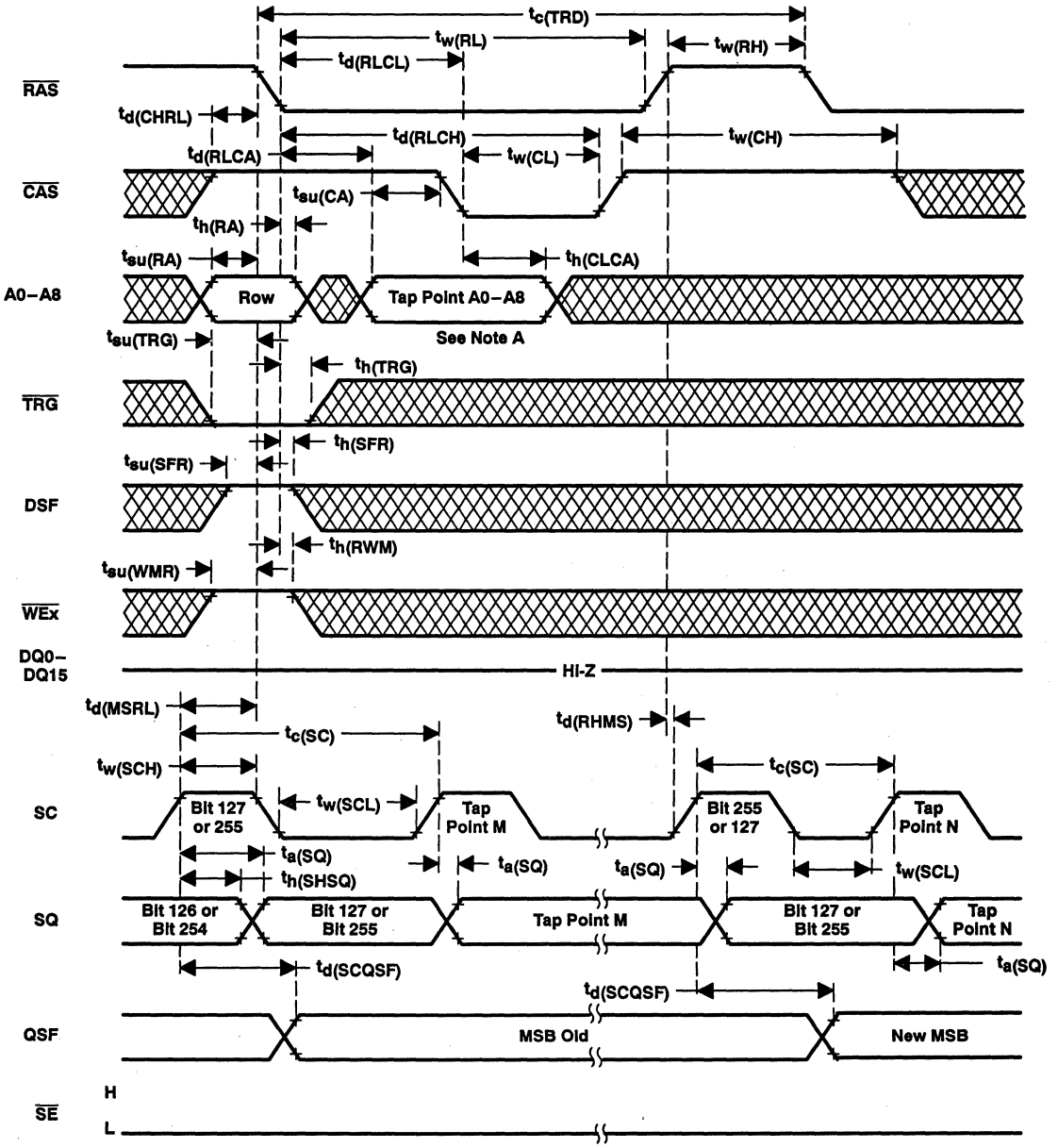
B. Once data is transferred into the data registers, the SAM is in the serial-read mode (i.e., the SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0–A7: register tap point; A8: identifies the DRAM row half

D. Late load operation is defined as $t_{d(THRH)} < 0$ ns.

Figure 46. Full-Register-Transfer Read Timing, Real-Time Load Operation/Late-Load Operation

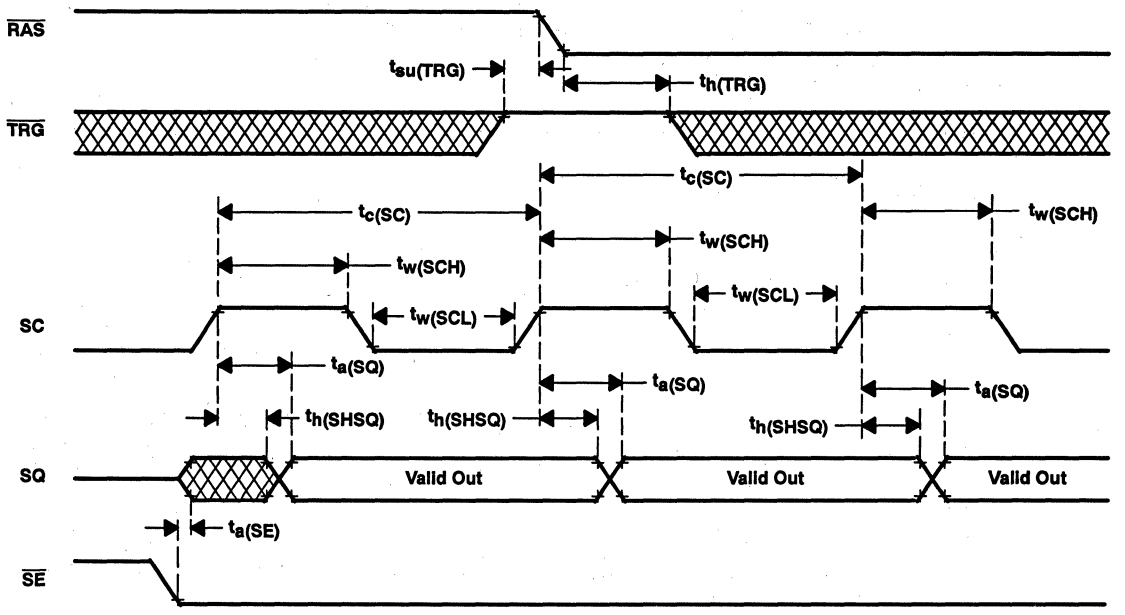
PARAMETER MEASUREMENT INFORMATION



NOTE A: A0–A6: tap point of the given half; A7: don't care; A8: identifies the DRAM row half

Figure 47. Split-Register-Transfer Read Timing

PARAMETER MEASUREMENT INFORMATION

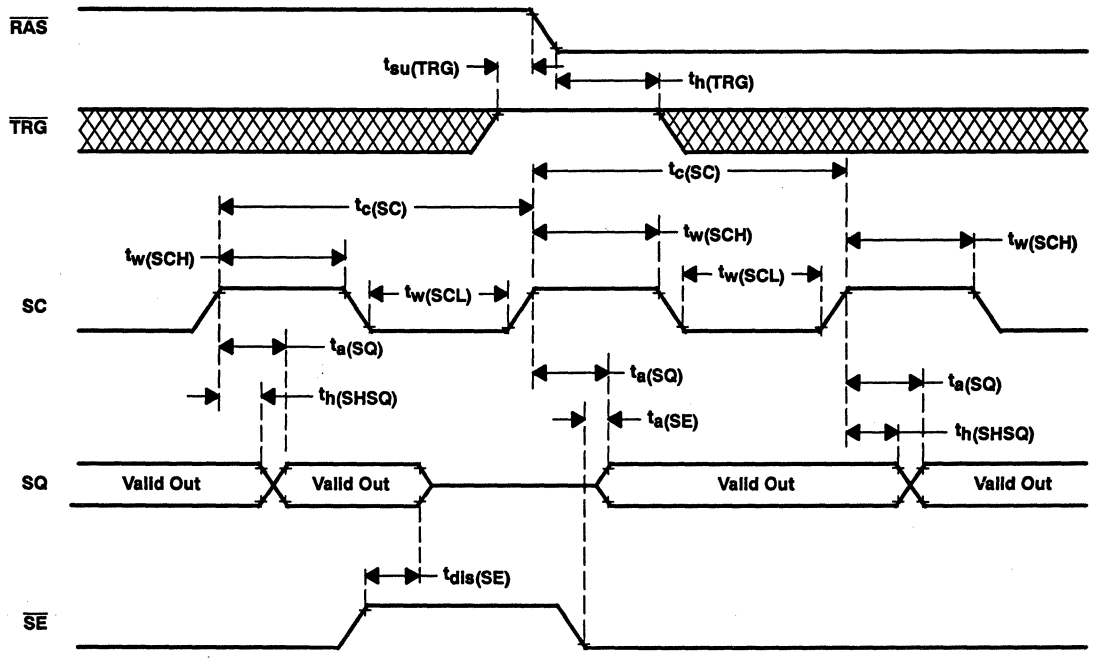


NOTES: A. While reading data through the serial-data register, $\overline{TRG}$ is a don't care; except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data-transfer operation.

B. The serial-data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer-read cycle.

Figure 48. Serial-Read-Cycle Timing ($\overline{SE}$ = V_{IL})

PARAMETER MEASUREMENT INFORMATION

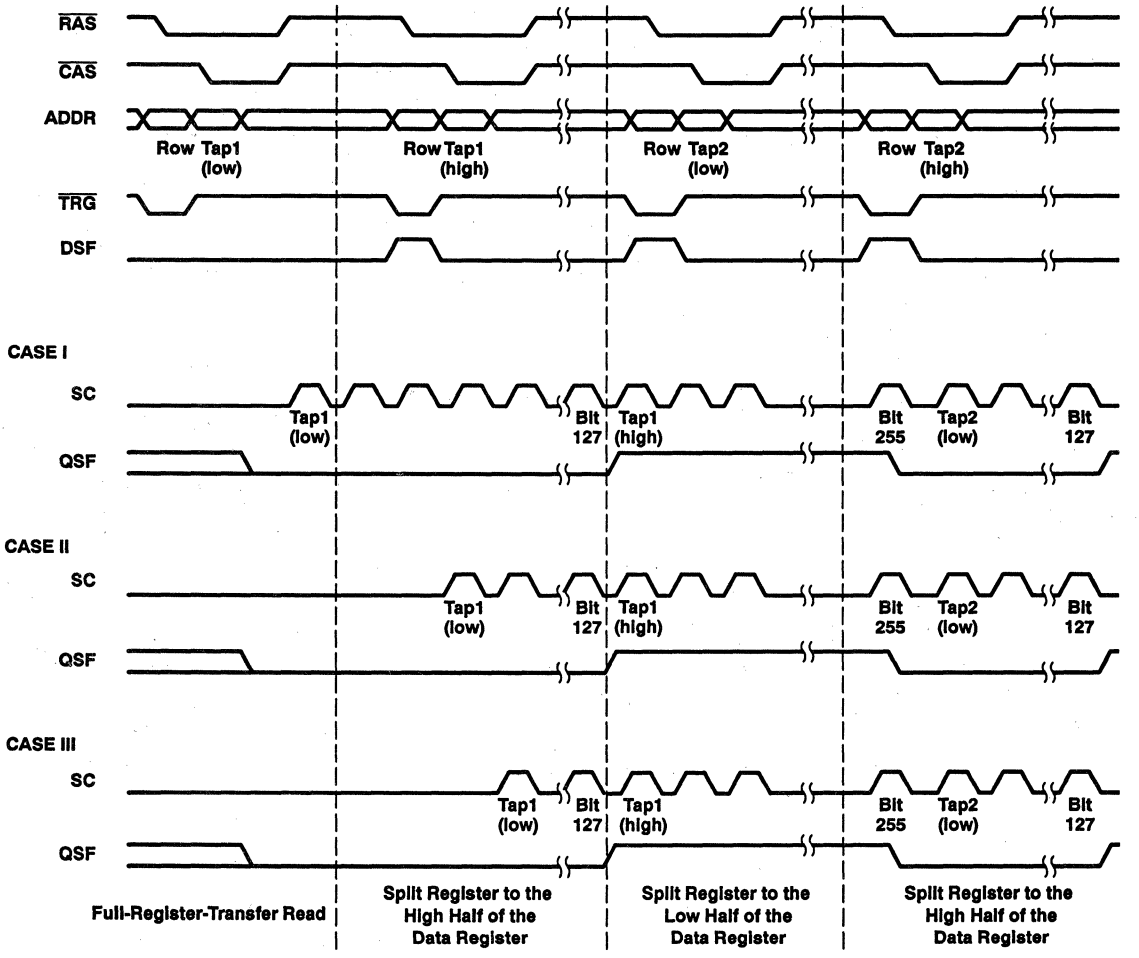


NOTES: A. While reading data through the serial-data register, $\overline{TRG}$ is a don't care except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data-transfer operation.

B. The serial-data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer-read cycle.

Figure 49. Serial-Read Timing ($\overline{SE}$-Controlled Read)

PARAMETER MEASUREMENT INFORMATION

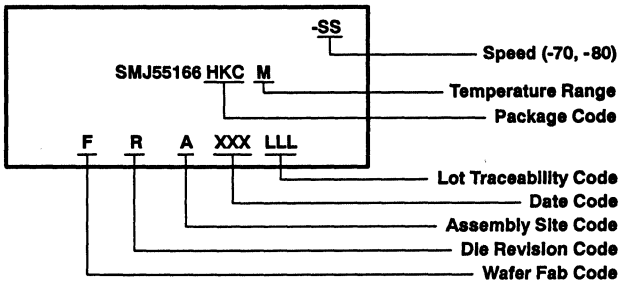


NOTES: A. In order to achieve proper split-register operation, a full-register-transfer read should be performed before the first split-register-transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can begin either after the full-register-transfer read cycle (CASE I), during the first split-register-transfer cycle (CASE II), or even after the first split-register-transfer cycle (CASE III). There is no minimum requirement of SC clock between the full-register-transfer read cycle and the first split-register cycle.

B. A split-register transfer into the inactive half is not allowed until $t_{d(MSRL)}$ is met. $t_{d(MSRL)}$ is the minimum delay time between the rising edge of the serial clock of the last bit (bit 127 or 255) and the falling edge of $\overline{RAS}$ of the split-register-transfer cycle into the inactive half. After the $t_{d(MSRL)}$ is met, the split-register transfer into the inactive half must also satisfy the minimum $t_{d(RHMS)}$ requirement. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register-transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 127 or 255).

Figure 50. Split-Register Operating Sequence

device symbolization



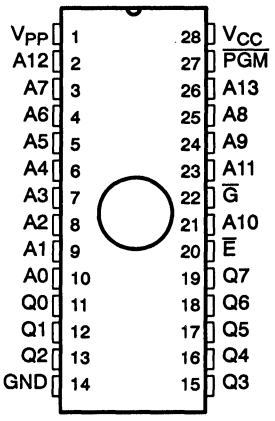
SGMS006E – AUGUST 1986 – REVISED JUNE 1995

- **Organization . . . 16K × 8**
- **Processed to MIL-STD-883, Class B**
- **Single 5-V Power Supply**
- **Pin-Compatible With Existing 64K and 128K EPROMs**
- **All Inputs/Outputs Fully TTL-Compatible**
- **Max Access/Min Cycle Times**

V_{CC} ± 5%	V_{CC} ± 10%	
'27C128-120		120 ns
	'27C128-15	150 ns
	'27C128-17	170 ns
	'27C128-20	200 ns
	'27C128-25	250 ns

- **HVCMOS Technology**
- **3-State Output Buffer**
- **Low Power Dissipation**
  - **Active . . . 138 mW Worst Case**
  - **Standby . . . 1.7 mW Worst Case (CMOS-Input Levels)**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Military Operating Temperature Range**
  - **–55°C to 125°C**

J PACKAGE
(TOP VIEW)



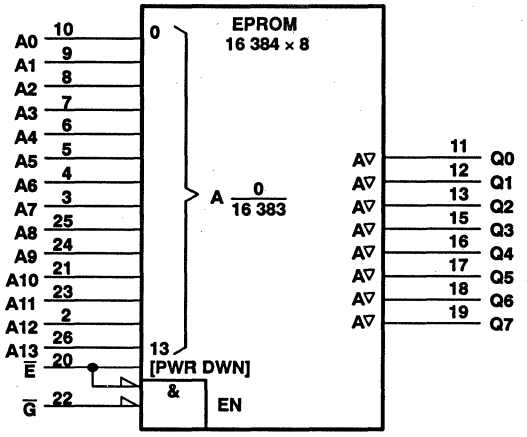
PIN NOMENCLATURE	
A0–A13	Address Inputs
$\overline{E}$	Chip Enable, Power Down
$\overline{G}$	Output Enable
GND	Ground
$\overline{PGM}$	Program
Q0–Q7	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12–13-V Power Supply

description

The SMJ27C128 series is a set of 131 072-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interfacing with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pullup resistors. The data outputs are three-state for connecting multiple devices to a common bus. The SMJ27C128 is pin-compatible with 28-pin 128K ROMs and EPROMs. They are offered in a 600-mil dual-in-line ceramic package (J suffix) rated for operation from –55°C to 125°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL-level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. The Fast programming algorithm uses a V_{PP} of 12.5 V and a V_{CC} of 6 V for a nominal programming time of two minutes. The SNAP! Pulse programming algorithm uses a V_{PP} of 13.0 V and a V_{CC} of 6.5 V for a nominal programming time of two seconds. For programming outside the system, existing EPROM programmers can be used. Locations can be programmed singly, in blocks, or at random.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

operation

The seven modes of operation for the SMJ27C128 are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL-level except for V_{PP} during programming (12.5 V for Fast or 13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION (PINS)	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
G (22)	V_{IL}	V_{IH}	X‡	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X	V_{IH}	
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H§	V_H§
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q0–Q7 (11–13, 15–19)	Data Out	Hi-Z	Hi-Z	Data In	Data Out	Hi-Z	CODE	
							MFG	DEVICE
							97	83

‡ X can be V_{IL} or V_{IH}.
§ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more SMJ27C128s are connected in parallel on the same bus, the output of any device in the circuit can be read without interference from the outputs of competing devices. To read the output of the selected SMJ27C128, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by the application of a high-level signal to one of these pins. Output data is accessed at pins Q0 through Q7.

latchup immunity

Latchup immunity on the SMJ27C128 is achieved by the application of a minimum of 250 mA on all inputs and outputs. This current provides latchup immunity beyond any potential transients at the PC-board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

For more information, see application report SMLA001, *Design Considerations; Latchup Immunity of the HVCMOS EPROM Family,* available through TI Field Sales Offices.

powerdown

Active I_{CC} supply current can be reduced from 25 mA to 500 μA (TTL-level inputs) or 300 μA (CMOS-level inputs) by applying a high input signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C128 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are in the logic 1 (high) state. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity × exposure time) is 15 W•s/cm^2. A typical 12 mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C128, the window should be covered with an opaque label.

SNAP! Pulse programming

The 128K EPROM can be programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1. The TI SNAP! Pulse programming algorithm can reduce programming time to two seconds. Actual programming time varies as a function of the programming used.

Data is presented in parallel (eight bits) on pins Q0 to Q7. Once addresses and data are stable, $\overline{PGM}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 μs followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to ten 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

Fast programming

The 128K EPROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming, data is presented in parallel (eight bits) on pins Q0 through Q7. Data is presented in parallel (eight bits) on pins Q0 to Q7. Once addresses and data are stable, $\overline{PGM}$ is pulsed.

Fast programming (continued)

The programming mode is achieved when V_{PP} = 12.5 V, V_{CC} = 6 V, $\overline{G}$ = V_{IH}, $\overline{PGM}$ = V_{IL}, and $\overline{E}$ = V_{IL}. More than one SMJ27C128 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Programming uses two types of programming pulses: prime and final. The length of the prime pulse is 1 millisecond; this pulse is applied up to 25 times. After each prime pulse, the byte being programmed is verified. If the correct data is read, the final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to 25 times. The final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6 V and V_{PP} = 12.5 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V (see Figure 2).

program inhibit

Programming can be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pin.

program verify

Programmed bits can be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10); i.e., A0 = V_{IL} accesses the manufacturer code, which is output on Q0–Q7; A0 = V_{IH} accesses the device code, which is output on Q0–Q7. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q7. The manufacturer code for these devices is 97, and the device code is 83.

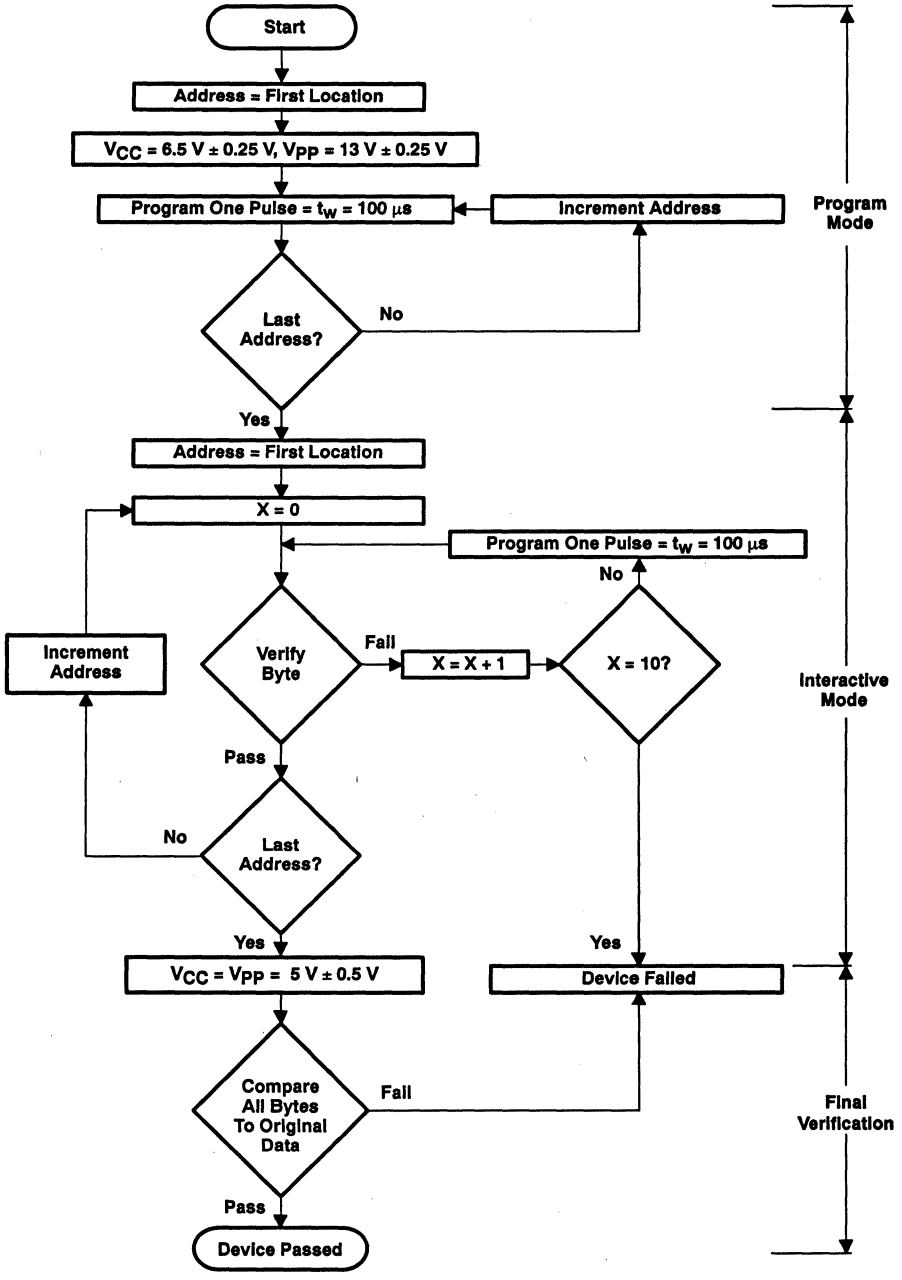


Figure 1. SNAP! Pulse Programming Flowchart

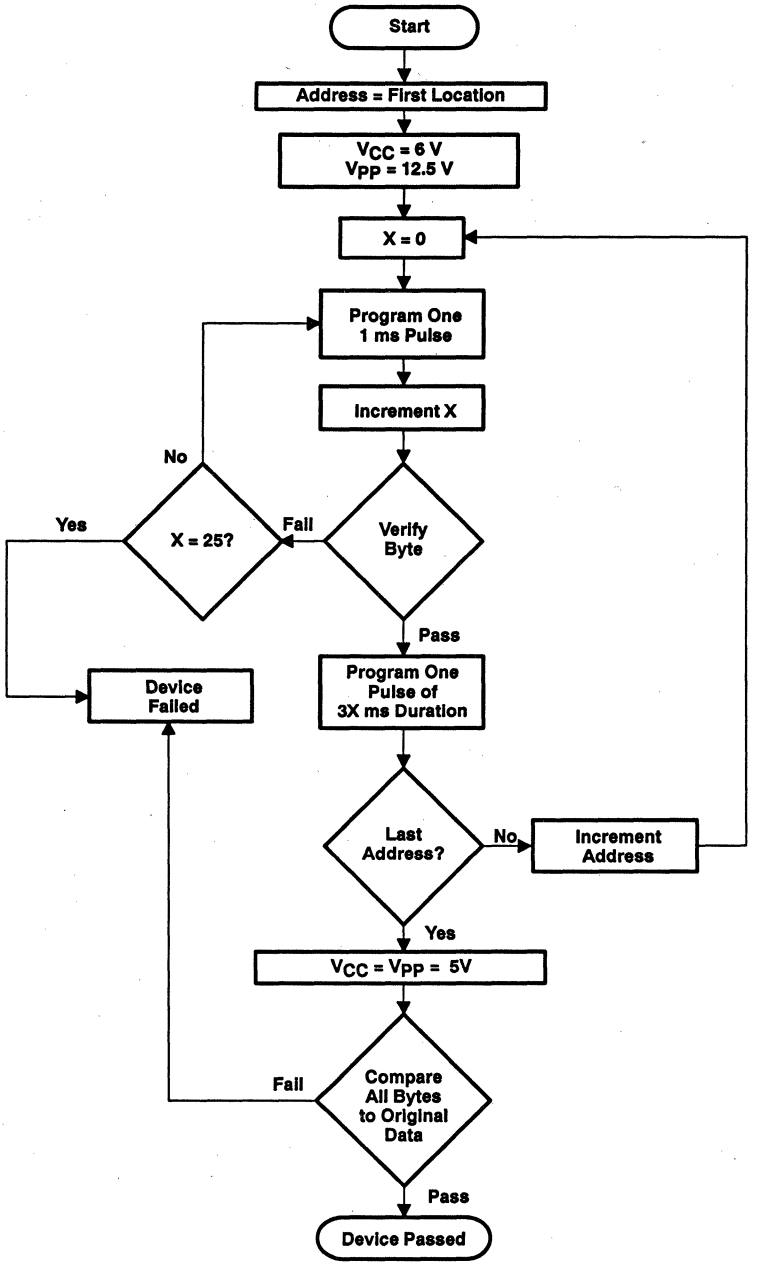


Figure 2. Fast Programming Flowchart

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... −0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... −0.6 V to 6.5 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature, T_A ..... −55° C
Maximum operating case temperature ..... 125° C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				'27C128-120			'27C128-15 '27C128-17 '27C128-20 '27C128-25			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)		4.75	5	5.25	4.5	5	5.5	V
		Fast programming algorithm		5.75	6	6.25	5.75	6	6.25	V
		SNAP! Pulse programming algorithm		6.25	6.50	6.75	6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)		$V_{CC}-0.6$		$V_{CC}+0.6$	$V_{CC}-0.6$		$V_{CC}+0.6$	V
		Fast programming algorithm		12	12.5	13	12	12.5	13	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	12.75	13	13.25	V
V_{IH}	High-level input voltage		TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
			CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	V
V_{IL}	Low-level input voltage		TTL	−0.5		0.8	−0.5		0.8	V
			CMOS	−0.5		0.2	−0.5		0.2	V
T_A	Operating free-air temperature			−55			−55			°C
T_C	Operating case temperature					125			125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case is $I_{CC} + I_{PP}$.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −400 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±1	µA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±1	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V			100	µA
I_{PP2}	V_{PP} supply current (during program pulse) (see Note 4)		V_{PP} = 13 V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			500	µA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			300	µA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_c = minimum cycle time, outputs open		10	25	mA

† Typical values are at T_A = 25°C and nominal voltages.
NOTE 4: This parameter has been characterized at 25°C and is not tested.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	10	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		8	14	pF

† Typical values are at T_A = 25°C and nominal voltages.
NOTE 5: Capacitance measurements are made on sample basis only.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C128-120		'27C128-15		'27C128-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	See Figure 3		120		150		170	ns
$t_{a(E)}$	Access time from chip enable			120		150		170	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		70		70	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C128-20		'27C128-25		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	See Figure 3		200		250	ns
$t_{a(E)}$	Access time from chip enable			200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first‡		0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first‡		0		0		ns

‡ Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not production-tested.

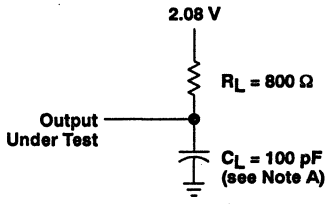
recommended timing requirements for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.5 and V_{PP} =13 V (SNAP! Pulse), T_A = 25°C (see Note 6)

			MIN	NOM	MAX	UNIT
t_{dis}	Disable time, output from $\overline{G}$		0		130	ns
t_{enG}	Enable time, output from $\overline{G}$				150	ns
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs
$t_{w(IPGM)}$	Pulse duration, initial program	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	µs
$t_{w(FPGM)}$	Pulse duration, final	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Setup time, address		2			µs
$t_{su(G)}$	Setup time, $\overline{G}$		2			µs
$t_{su(D)}$	Setup time, data		2			µs
$t_{su(VPP)}$	Setup time, V_{PP}		2			µs
$t_{su(VCC)}$	Setup time, V_{CC}		2			µs
$t_{su(E)}$	Setup time, $\overline{E}$		2			µs

NOTES: 6. For all switching characteristics and timing measurements input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2.0 V for logic high and 0.8 V for logic low for both inputs and outputs.

7. Common test conditions apply for t_{dis} except during programming.

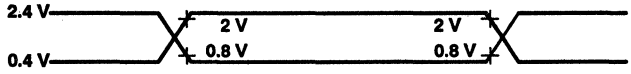
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 3. Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

PARAMETER MEASUREMENT INFORMATION

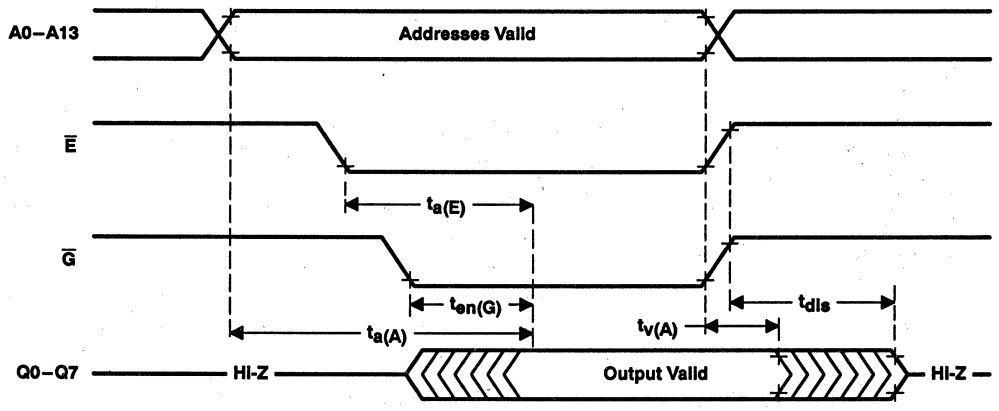


Figure 4. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

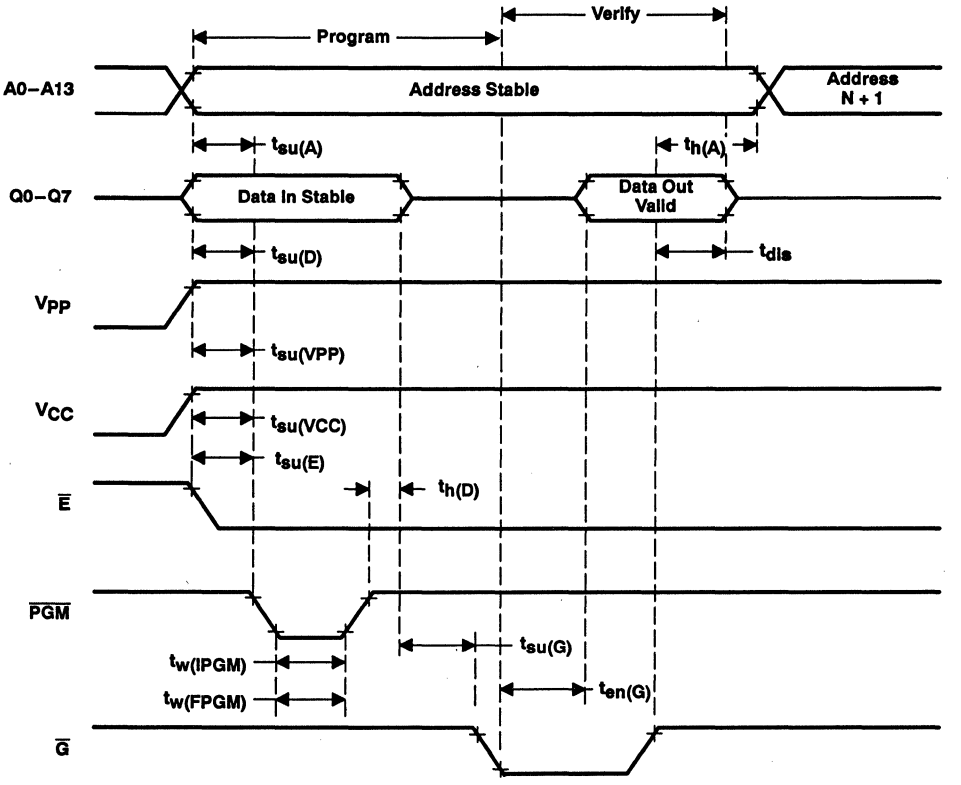


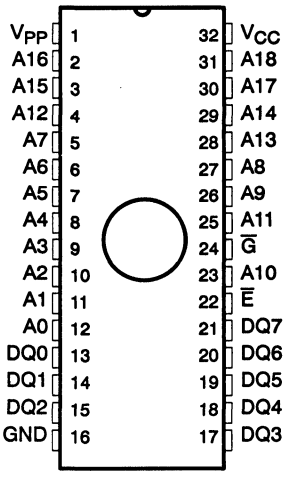
Figure 5. Program-Cycle Timing

- **Organization . . . 512K × 8**
- **Single 5-V Power Supply**
- **Industry Standard 32-Pin Dual-In-line Package**
- **All Inputs/Outputs Fully TTL Compatible**
- **Static Operation (No Clocks, No Refresh)**
- **Max Access/Min Cycle Time**

  V_{CC} ± 10%

  '27C040-10 100 ns
  '27C040-12 120 ns
  '27C040-15 150 ns
- **8-Bit Output For Use In Microprocessor-Based Systems**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV DC Assured Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 385 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**
- **Military Operating Temperature Range**
  – 55°C to 125°C

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A18	Address Inputs
DQ0–DQ7	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply†

† Only in program mode

description

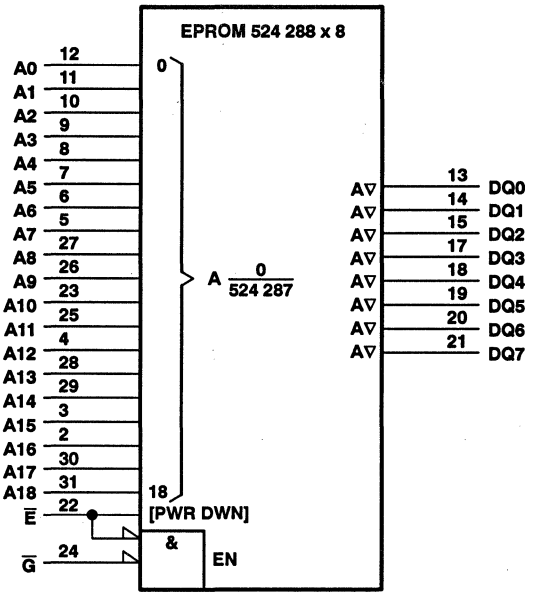
The SMJ27C040 is a set of 4194304-bit, ultraviolet-light erasable, electrically programmable read-only memories (EPROMs).

These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits. Each output can drive one Series 54. TTL circuit without external resistors. The data outputs are 3-state for connecting multiple devices to a common bus.

The SMJ27C040 is offered in a 32-pin 600-mil dual-in-line ceramic package (J suffix) rated for operation from – 55°C to 125°C.

Since this EPROM operates from a single 5-V supply (in the read mode), it is ideal for use in microprocessor-based systems. One other (13-V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J package.

operation

The seven modes of operation are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V), and V_H (12 V) on A9 for signature mode.

	FUNCTION						
	$\overline{E}$	$\overline{G}$	V_{PP}	V_{CC}	A9	A0	DQ0–DQ7
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	X	X	Data Out
Output Disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	X	Hi-Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	X	X	Hi-Z
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	Data In
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	X	X	Hi-Z
Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	Data Out
Signature Mode	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_{IH}‡	V_{IL}	MFG Code 97
						V_{IH}	Device Code 50

‡ X can be V_{IL} or V_{IH}.
§ V_H = 12 V ± 0.5 V

read/output disable

When the outputs of two or more SMJ27C040s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins. Output data is accessed at pins Q0–Q7.

latchup immunity

Latchup immunity on the SMJ27C040 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, "*Design Considerations; Latchup Immunity of the HVCMOS EPROM Family*", available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 70 mA to 1 mA for a high TTL input on $\overline{E}$ and to 100 μA for a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C040 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet-light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C040, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

SNAP! Pulse programming

The SMJ27C040 and TMS27PC040 are programmed by using the SNAP! Pulse programming algorithm. The programming sequence is shown in the SNAP! Pulse programming flow chart (Figure 1).

The initial setup is V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IH}$. Once the initial location is selected, the data is presented in parallel (eight bits) on pins DQ1 through DQ8. Once addresses and data are stable, the programming mode is achieved when $\overline{E}$ is pulsed low (V_{IL}) with a pulse duration of $t_{w(PGM)}$. Every location is programmed only once before going to interactive mode.

In the interactive mode, the word is verified at V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IL}$. If the correct data is not read, the programming is performed by pulling $\overline{G}$ high, then $\overline{E}$ low with a pulse duration of $t_{w(PGM)}$. This sequence of verification and programming is performed up to a maximum of 10 times. When the device is fully programmed, all bytes are verified with $V_{CC} = V_{PP}$ = 5 V ± 10%.

program inhibit

Programming can be inhibited by maintaining high level inputs on the $\overline{E}$ and $\overline{G}$ pins.

program verify

Programmed bits can be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, and $\overline{E} = V_{IH}$.

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. The signature code for the SMJ27C040 is 9750. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code 50 (Hex), as shown by the signature mode table below.

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	0	1	0	1	0	0	0	0	50

† $\overline{E} = \overline{G} = V_{IL}$, A1–A8 = V_{IL}, A9 = V_H, A10–A18 = V_{IL}, $V_{PP} = V_{CC}$.

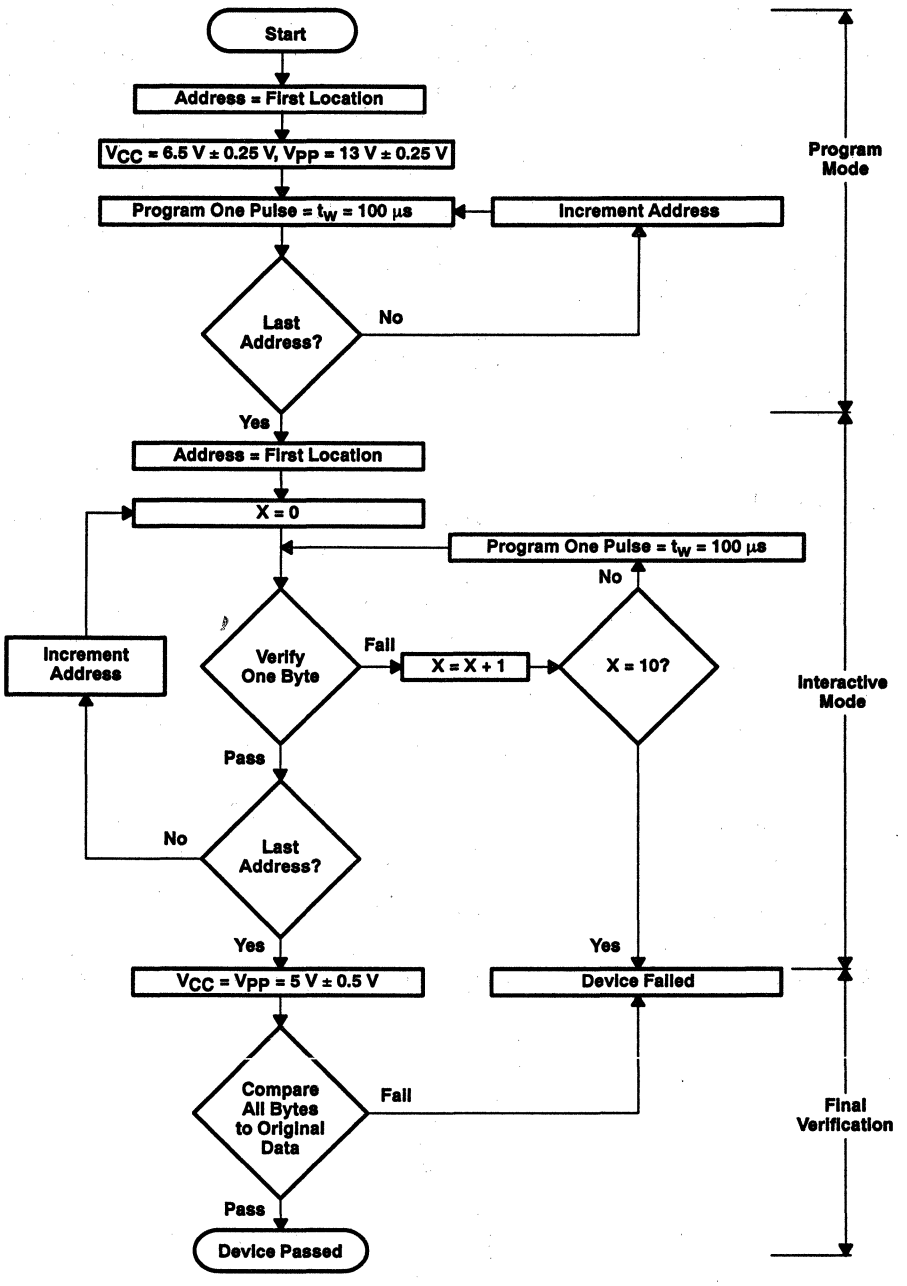


Figure 1. SNAP! Pulse Programming Flow Chart

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... −0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... −0.6 V to 6.5 V
A9 ..... −0.6 V to 13 V
Output voltage range, with respect to V_{SS} (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature ..... −55°C
Maximum operating case temperature ..... 125°C
Storage temperature range ..... −65°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)		V_{CC} – 0.6		V_{CC} + 0.6	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level input voltage		TTL	2		V_{CC}+0.5	V
			CMOS	V_{CC} – 0.2		V_{CC}+0.5	
V_{IL}	Low-level input voltage		TTL	– 0.5		0.8	V
			CMOS	– 0.5		0.2	
T_A	Operating free-air temperature			– 55			°C
T_C	Operating case temperature					125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming, V_{PP} must be maintained at 13 V ± 0.25 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 400 µA	2.4		V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA		0.4	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V		±1	µA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse) (see Note 4)		V_{PP} = 12.75 V, T_A – 25°C		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		1	mA
		CMOS-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	µA
I_{CC2}	V_{CC} supply current (active)		$\overline{E}$ = V_{IL}, V_{CC} = 5.5 V, t_{cycle} = minimum cycle time, outputs open (see Note 5)		50	mA

NOTES: 4. This parameter is only sampled and not 100% tested.
5. Minimum cycle time = maximum access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (V_{CC} = V_{PP} = 5 V ± 0.5 V)†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V		4	8	pF
C_o	Output capacitance	V_O = 0 V		8	12	pF

† Capacitance is sampled only at initial design and after any major change.
‡ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Notes 7 and 8)

PARAMETER		TEST CONDITIONS (SEE NOTE 6 AND 7)	'27C040-10		'27C040-12		'27C040-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	(see Figure 2) Input t_r ≤ 20 ns Input t_f ≤ 20 ns		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		50		50	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first (see Note 8)		0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first (see Note 8)		0		0		0		ns

NOTES: 6. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (Figure 2)
7. Common test conditions apply for t_{dis} except during programming.
8. Value calculated from 0.5-V delta to measured output level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C

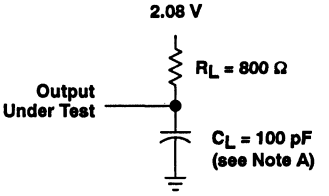
PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0	100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 6)

			MIN	TYP	MAX	UNIT
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs
$t_{w(PGM)}$	Pulse duration, program	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Setup time, address		2			µs
$t_{su(E)}$	Setup time, $\overline{E}$		2			µs
$t_{su(G)}$	Setup time, $\overline{G}$		2			µs
$t_{su(D)}$	Setup time, data		2			µs
$t_{su(VPP)}$	Setup time, V_{PP}		2			µs
$t_{su(VCC)}$	Setup time, V_{CC}		2			µs

NOTE 6: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic logic low. (Figure 2)

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

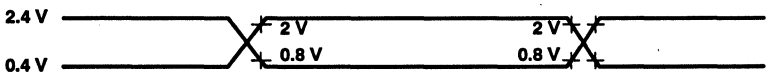


Figure 2. Output Load Circuit and Input/Output Wave Forms

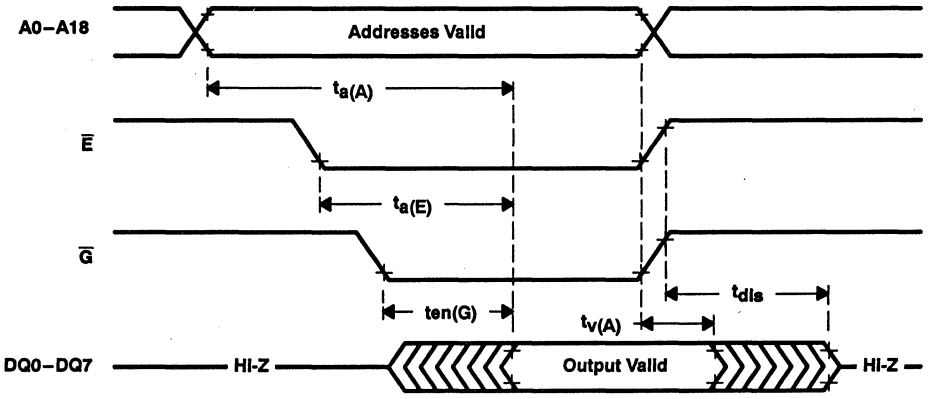
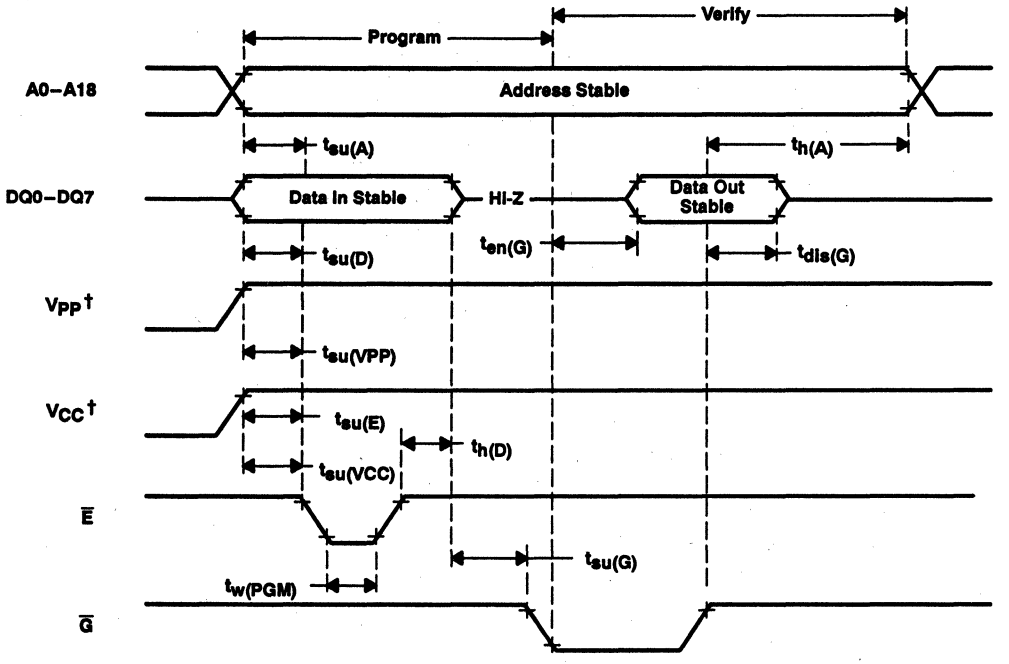


Figure 3. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

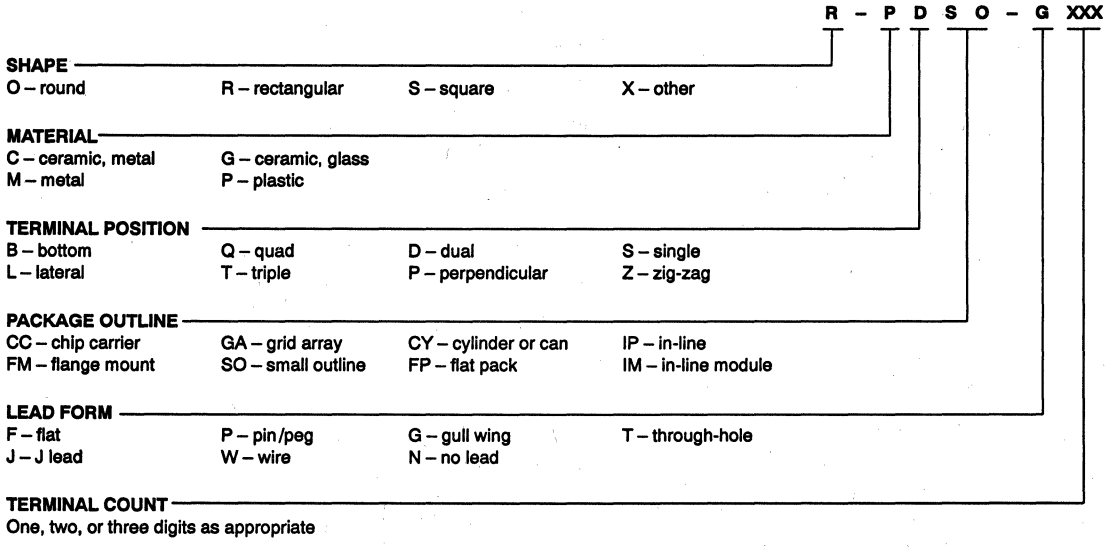
Figure 4. Program-Cycle Timing (SNAP! Pulse Programming)

Contents

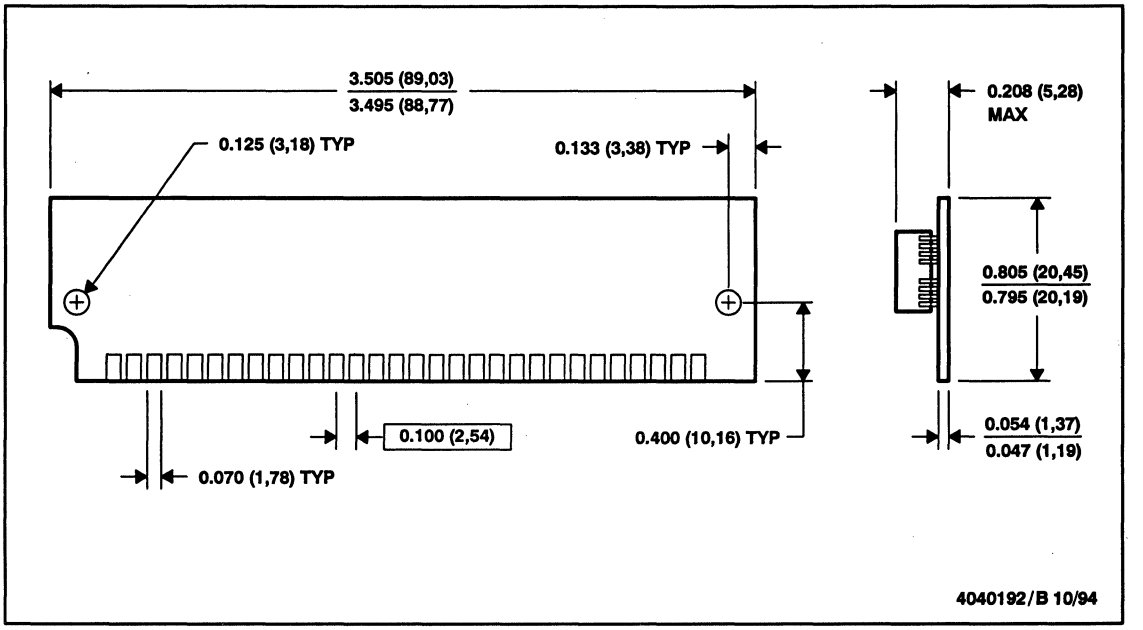
CHAPTER 13. MECHANICAL DATA

MOS Memory Commercial

Each package drawing contains a JEDEC Std 30 descriptor in the title line. This descriptor uses the following convention: shape, material, terminal position, package outline, lead form, and terminal count. The codes for each element in the JEDEC Std 30 descriptor are as follows:



AD (R-PSIM-N30) **SINGLE-IN-LINE MEMORY MODULE†**

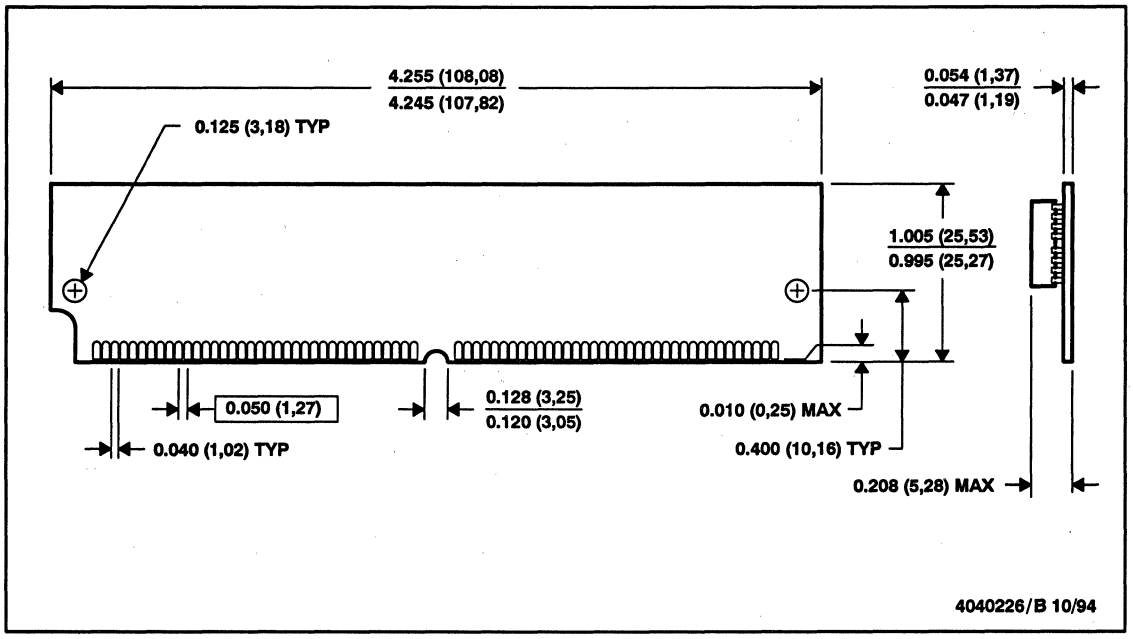


NOTES: B. All linear dimensions are in inches (millimeters).
C. This drawing is subject to change without notice.

† Applicable MOS Memory Devices:

TM4100GAD8 TM4100EAD9

BK (R-PSIM-N72) **SINGLE-IN-LINE MEMORY MODULE†**

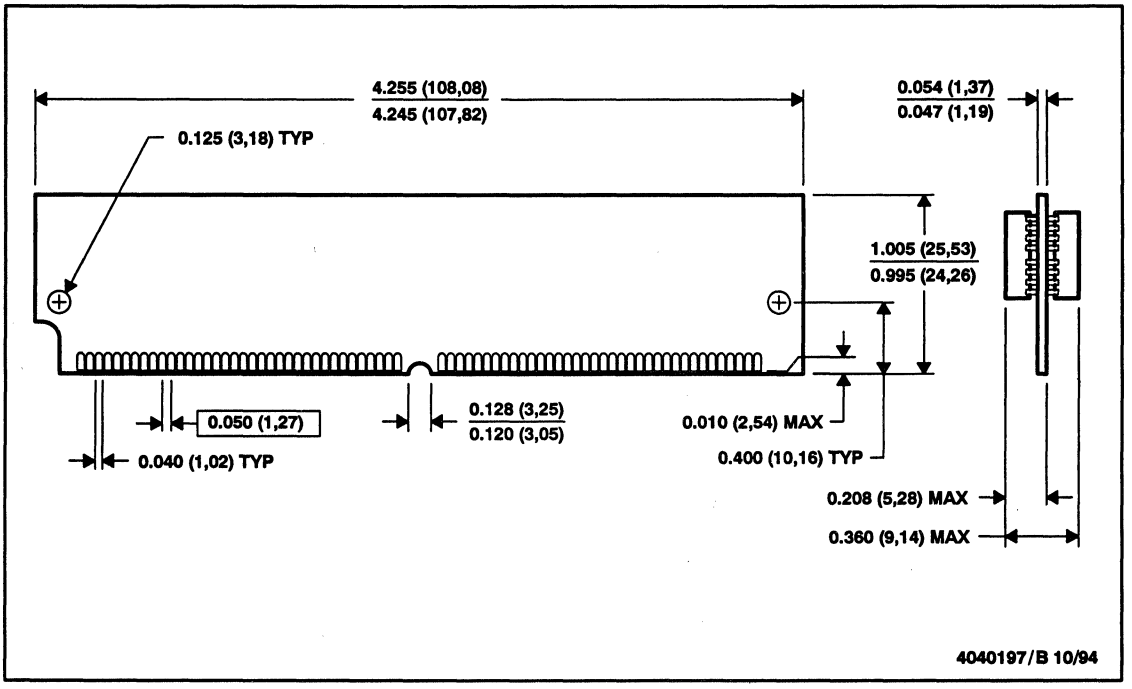


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

† Applicable MOS Memory Devices:

TM497BBK32 TM497BBK32S

BK (R-PSIM-N72) **SINGLE-/DOUBLE-SIDED IN-LINE MEMORY MODULE†**

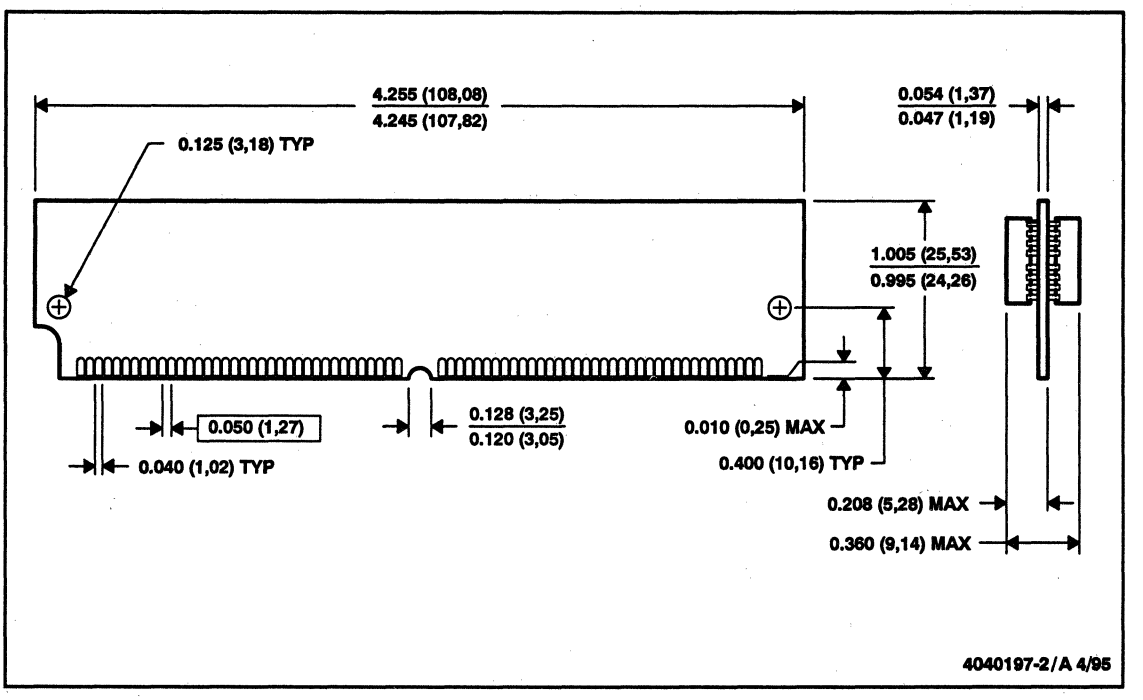


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

† Applicable MOS Memory Devices:

TM124BBK32	TM124BBK32S	TM248CBK32	TM248CBK32S
TM124MBK36B	TM124MBK36R	TM248NBK36B	TM248NBK36R
TM124MBK36C	TM124MBK36S	TM248NBK36C	TM248NBK36S

BK (R-PSIM-N72) **DOUBLE-SIDED SINGLE-IN-LINE MEMORY MODULE†**

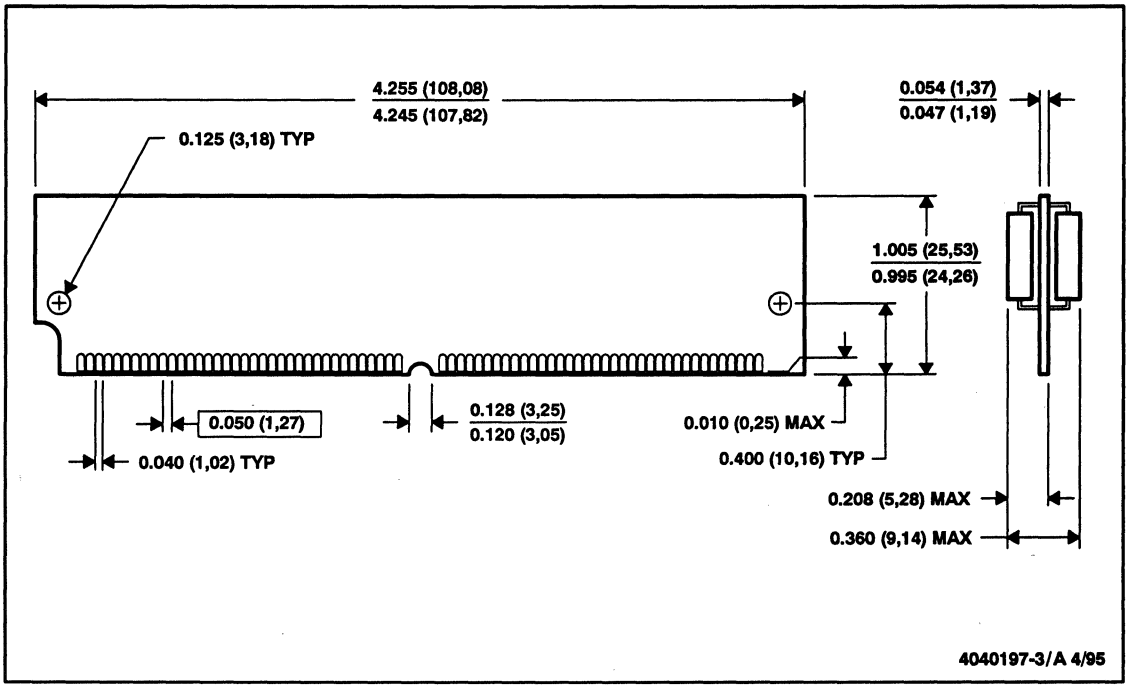


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

† Applicable MOS Memory Devices:

TM893CBK32 TM893CBK32S TM497MBK36A TM497MBK36Q

BK (R-PSIM-N72) **SINGLE-/DOUBLE-SIDED SINGLE-IN-LINE MEMORY MODULE†**

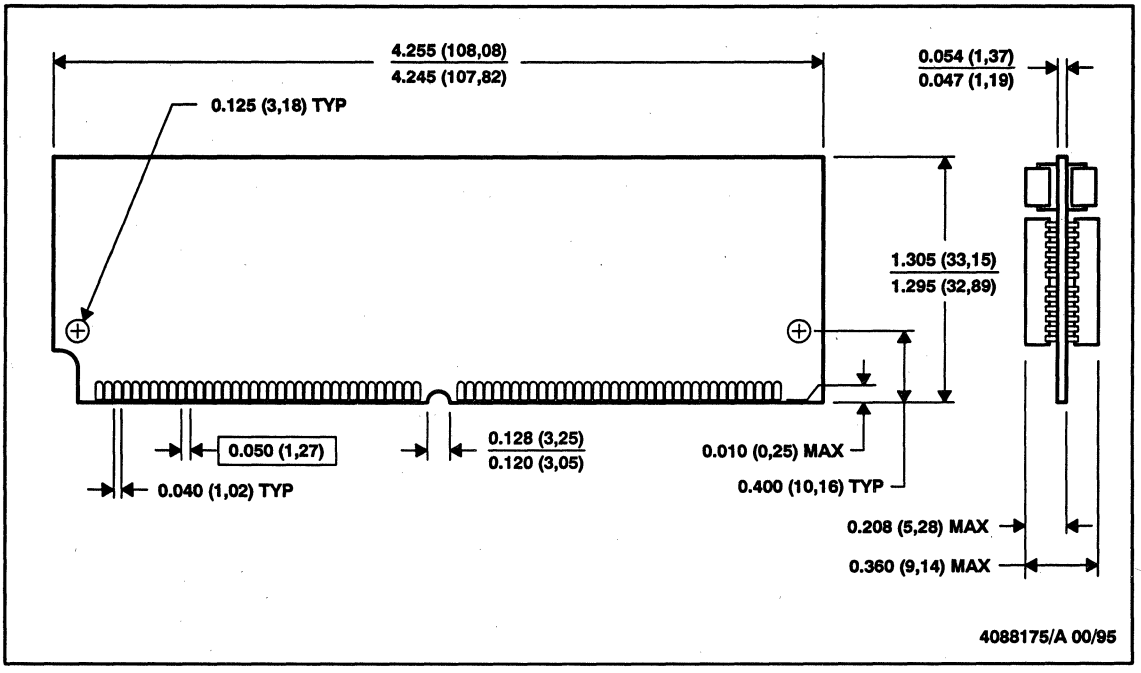


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

† Applicable MOS Memory Devices:

TM124BBK32F	TM248CBK32F	TM124MBK36F	TM248NBK36F	TM124MBK36G	TM248NCK36G
TM124BBK32U	TM248CBK32U	TM124MBK36U	TM248NBK36U	TM124MBK36V	TM248NBK36V

BM (R-PSIM-N72) **SINGLE/DOUBLE-SIDED IN-LINE MEMORY MODULE†**

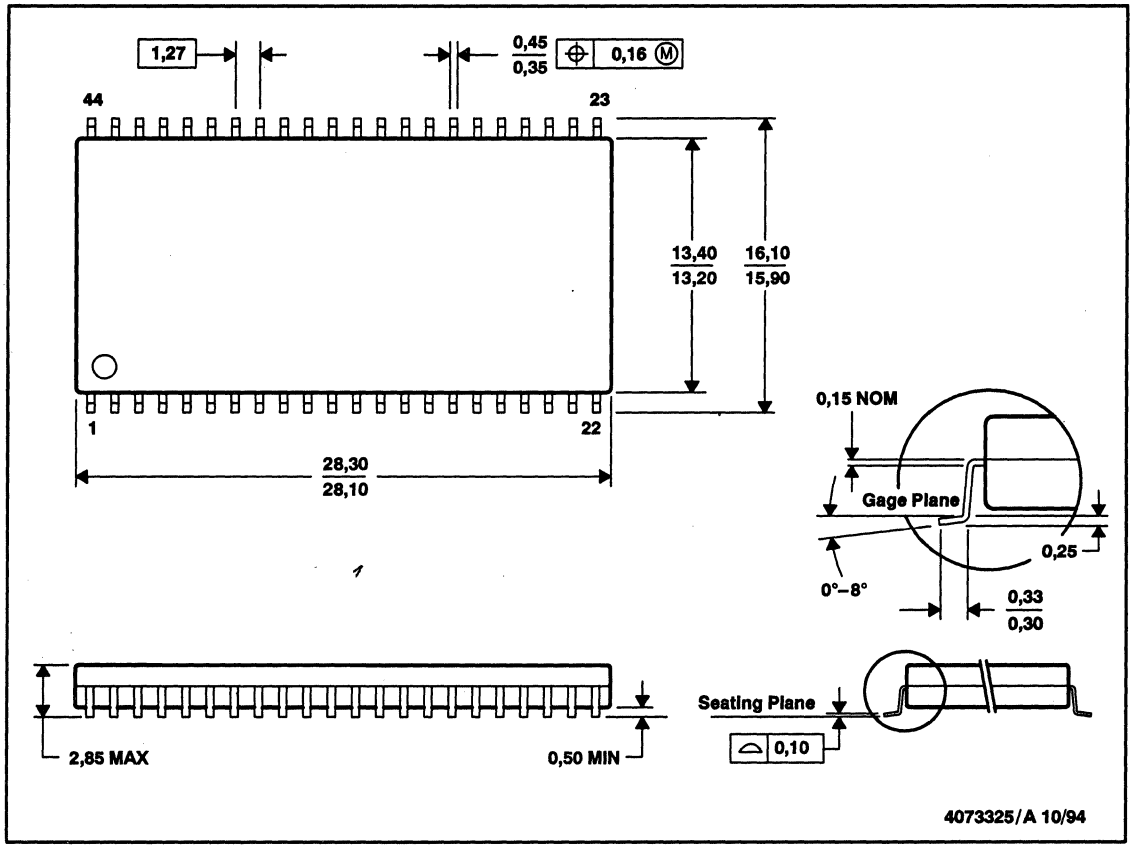


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

† Applicable MOS Memory Devices:

TM893NBM36A TM893NBM36Q TM497MBM36A TM497MBM36Q

DBJ (R-PDSO-G44) **PLASTIC SMALL-OUTLINE PACKAGE†**

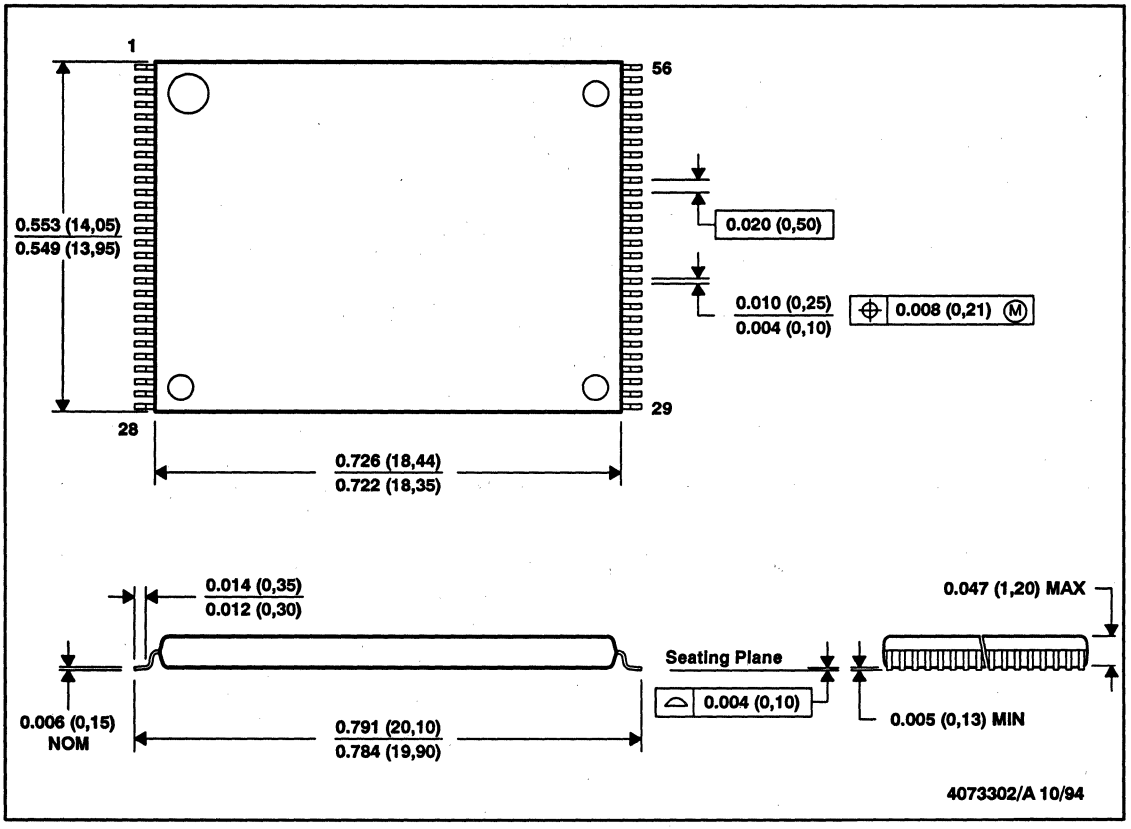


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

† Applicable MOS Memory Devices:

TMS28F200BZT TMS28F200BZB TMS28F400BZT TMS28F400BZB

DBR (R-PDSO-G56) **PLASTIC DUAL SMALL-OUTLINE PACKAGE†**

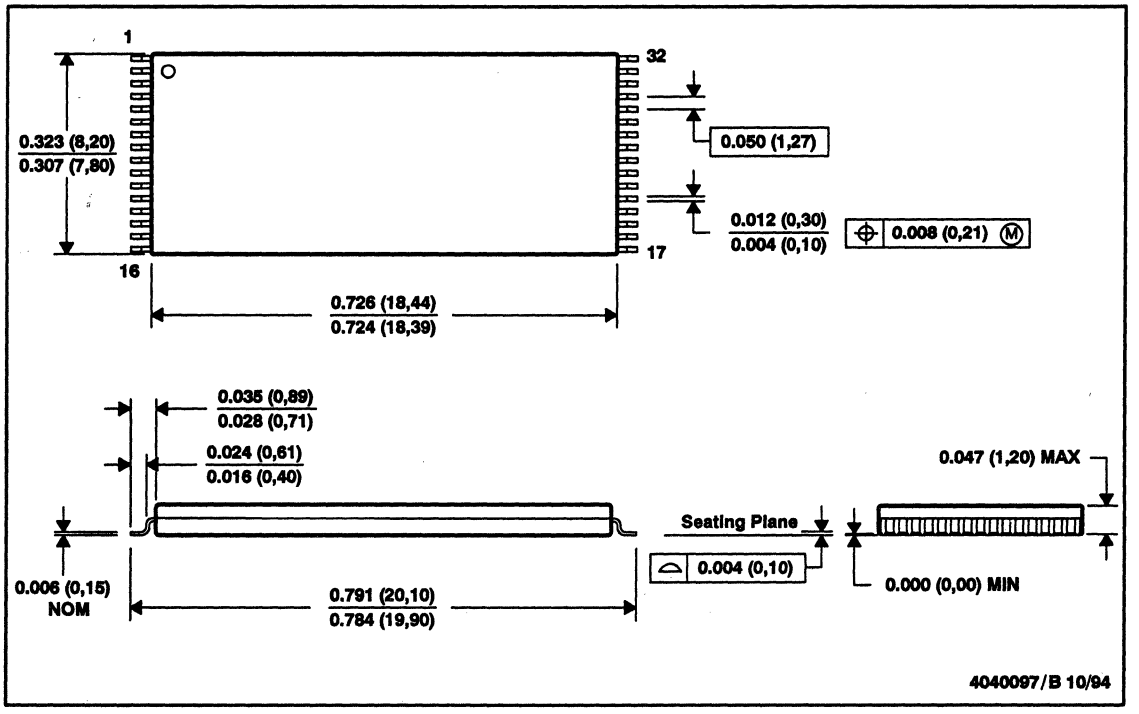


NOTES: A. All linear dimensions are in inches(millimeters).
B. This drawing is subject to change without notice.

† Applicable MOS Memory Devices:

TMS28F200BZT TMS28F200BZB TMS28F400BZT TMS28F400BZB

DD (R-PDSO-G32) **THIN SMALL-OUTLINE PACKAGE†**

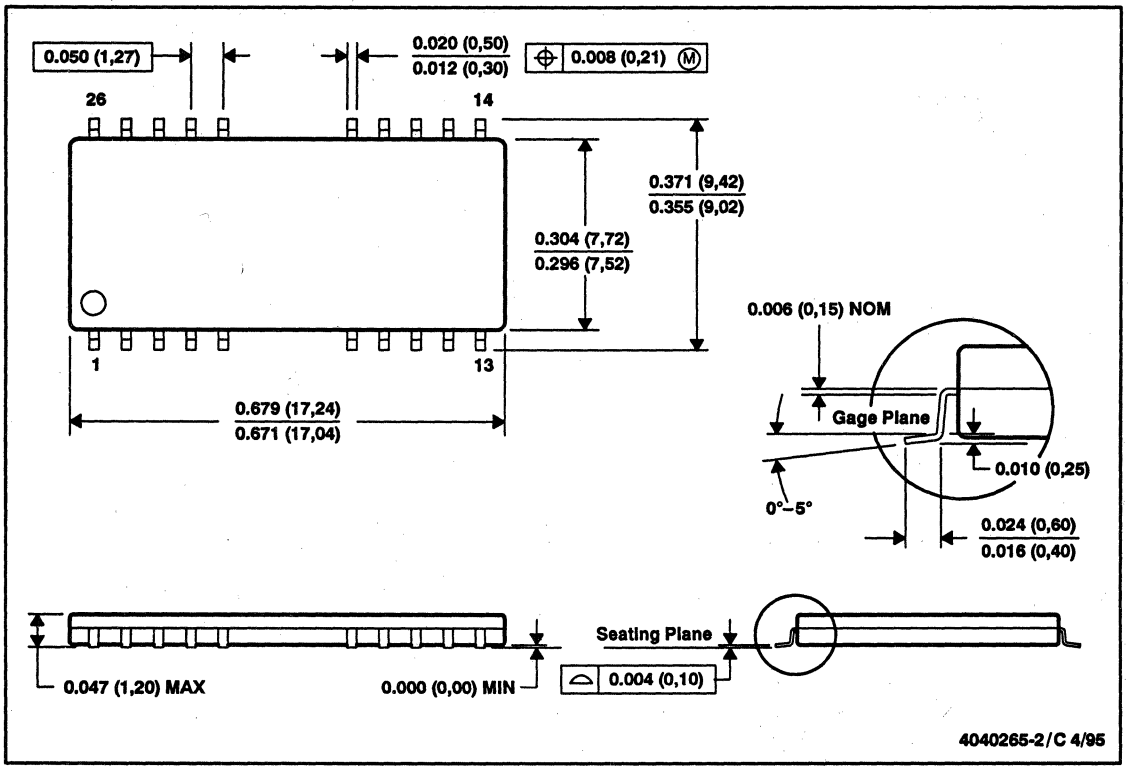


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

† Applicable MOS Memory Devices:

TMS28F512A TMS28F010B TMS27C512 TMS27PC512 TMS28C010A TMS27PC010A
TMS28F020

DGA (R-PDSO-G20/26) **PLASTIC SMALL-OUTLINE PACKAGE†**

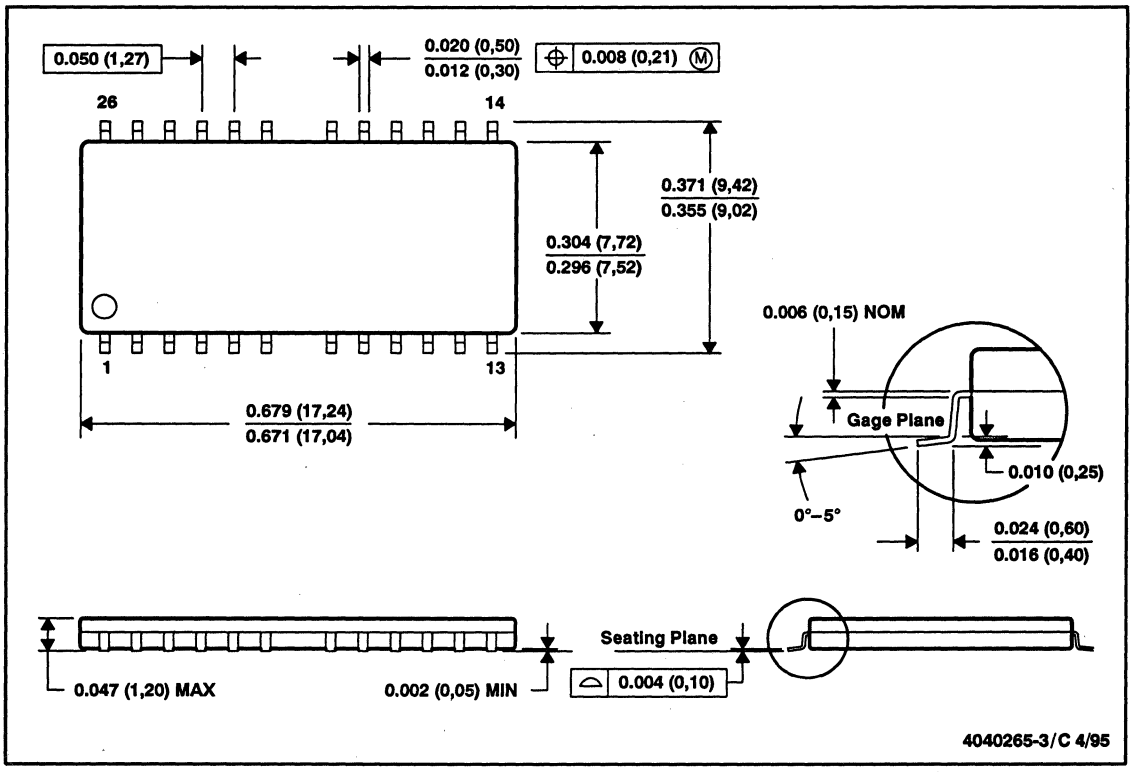


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

† Applicable MOS Memory Devices:

TMS44100	TMS44100P	TMS46100	TMS46100P	TMS44400	TMS44400P
TMS46400	TMS46400P				

DGA (R-PDSO-G24/26) **PLASTIC SMALL-OUTLINE PACKAGE†**

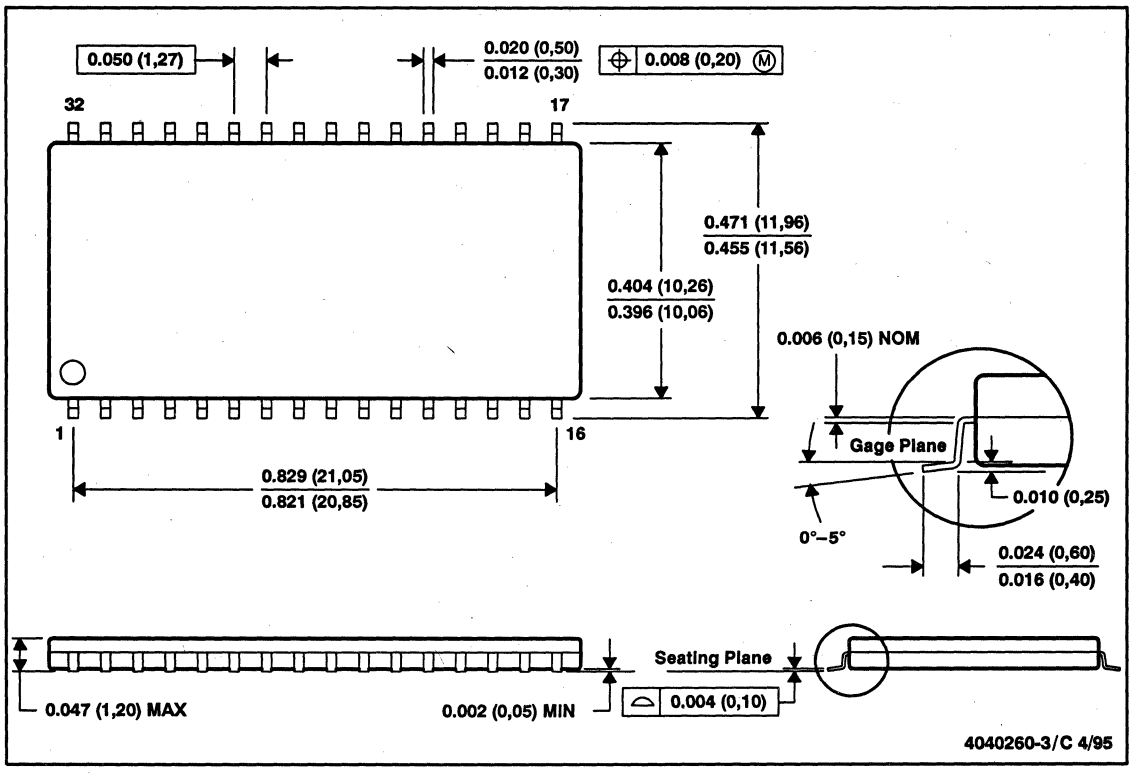


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

† Applicable MOS Memory Devices:

TMS44460	TMS44460P	TMS46460	TMS46460P	TMS416400	TMS416400P
TMS417400	TMS417400P	TMS426400	TMS426400P	TMS427400	TMS427400P

DGC (R-PDSO-G32) **PLASTIC SMALL-OUTLINE PACKAGE†**

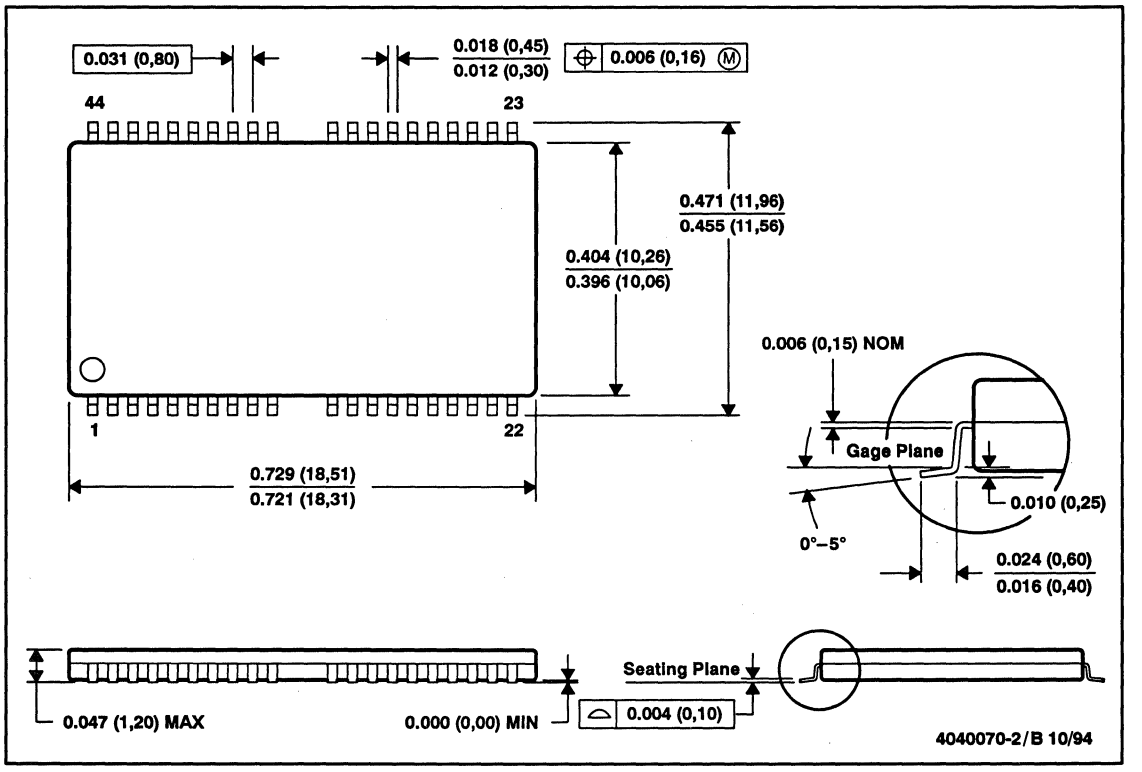


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

† Applicable MOS Memory Devices:

TMS464400 TMS464400P TMS464800 TMS464800P

DGE (R-PDSO-G40/44) **PLASTIC SMALL-OUTLINE PACKAGE†**

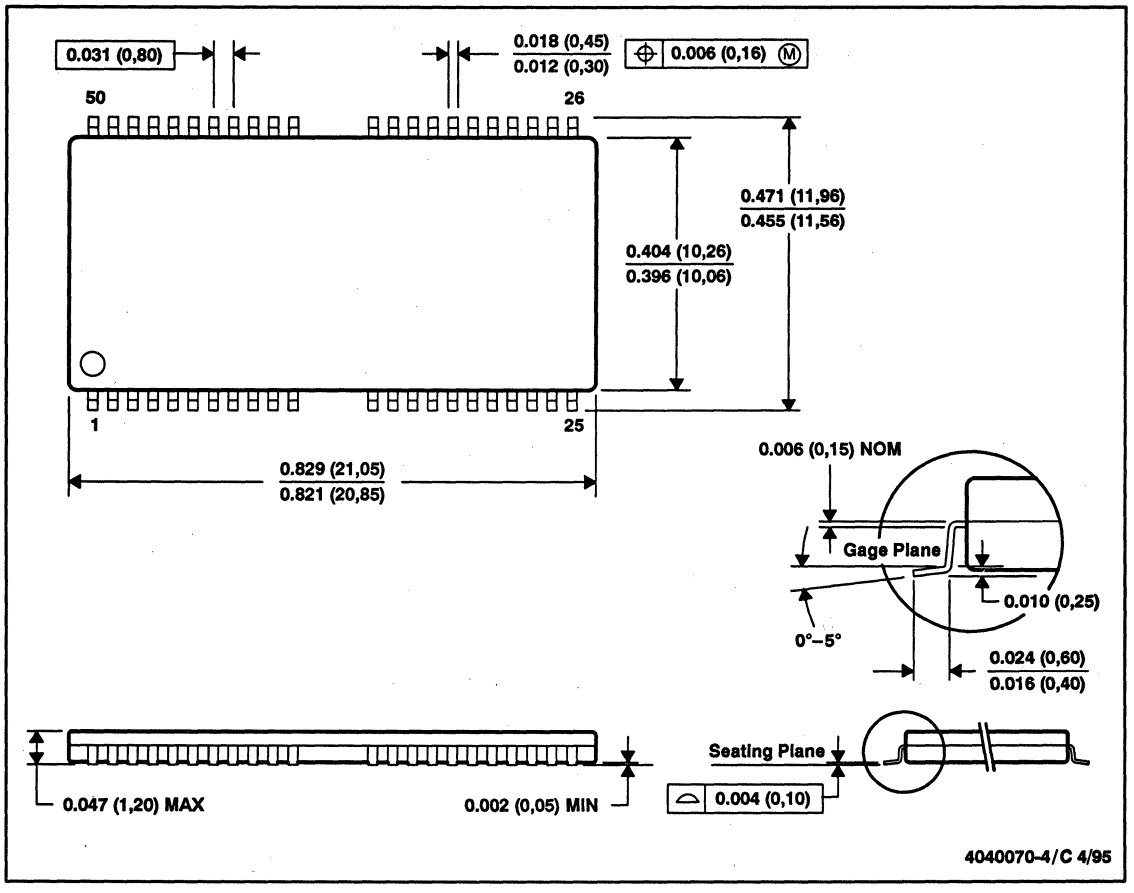


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

† Applicable MOS Memory Devices:

TMS44165 TMS44165P TMS45160 TMS45160P TMS45165 TMS45165P

DGE (R-PDSO-G44/50) **PLASTIC SMALL-OUTLINE PACKAGE†**

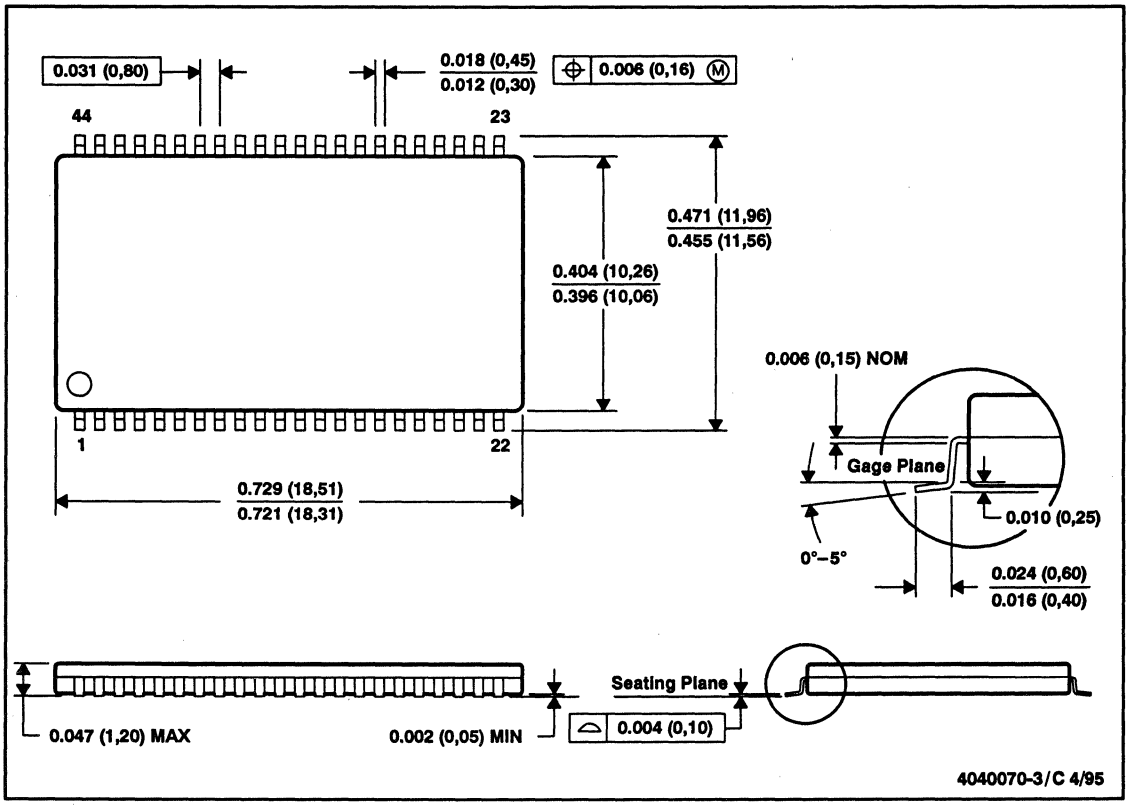


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

† Applicable MOS Memory Devices:

TMS416160	TMS416160P	TMS418160	TMS418160P	TMS426160	TMS426160P
TMS428160	TMS428160P	TMS416169	TMS416169P	TMS418169	TMS418169P
TMS426169	TMS426169P	TMS428169	TMS428169P		

DGE (R-PDSO-G44) **PLASTIC SMALL-OUTLINE PACKAGE†**

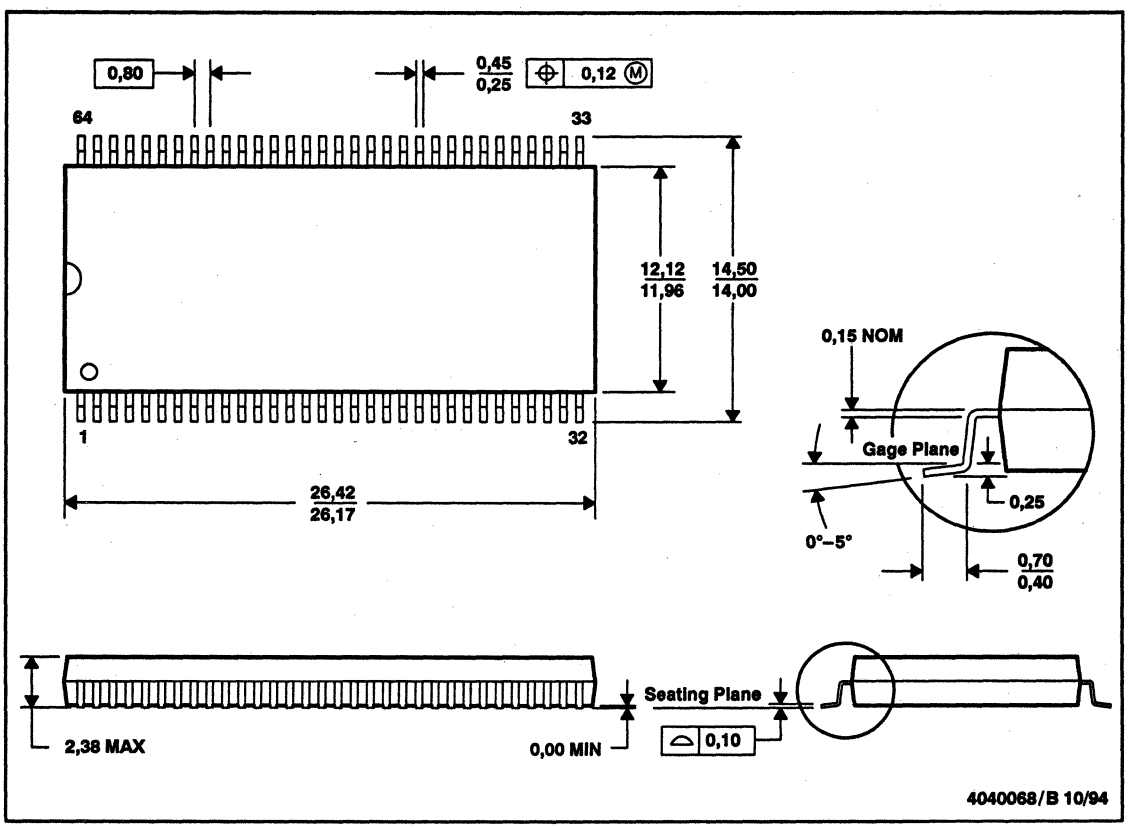


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

† Applicable MOS Memory Devices:

TMS626402 TMS626802

DGH (R-PDSO-G64) **PLASTIC SMALL-OUTLINE PACKAGE†**

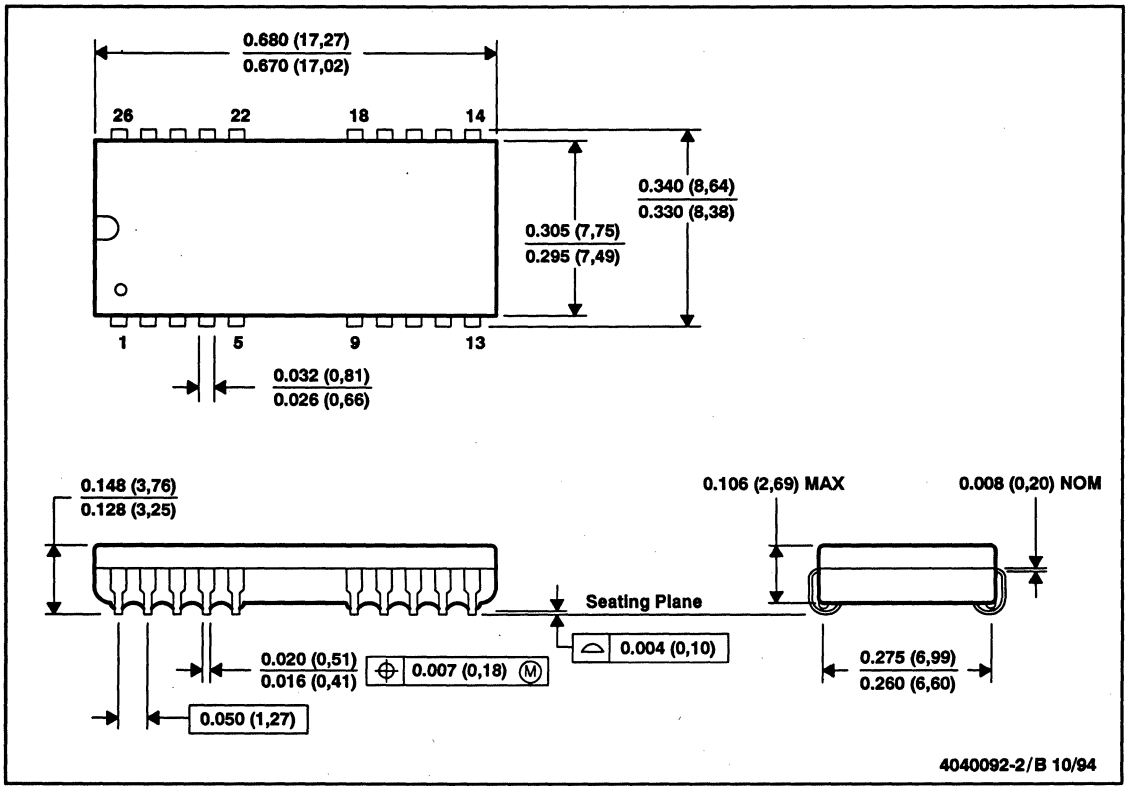


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold flash or protrusion. Maximum mold protrusion is 0,125.

† Applicable MOS Memory Devices:

TMS55160 TMS55165 TMS55161 TMS55166

DJ (R-PDSO-J20/26) **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE†**

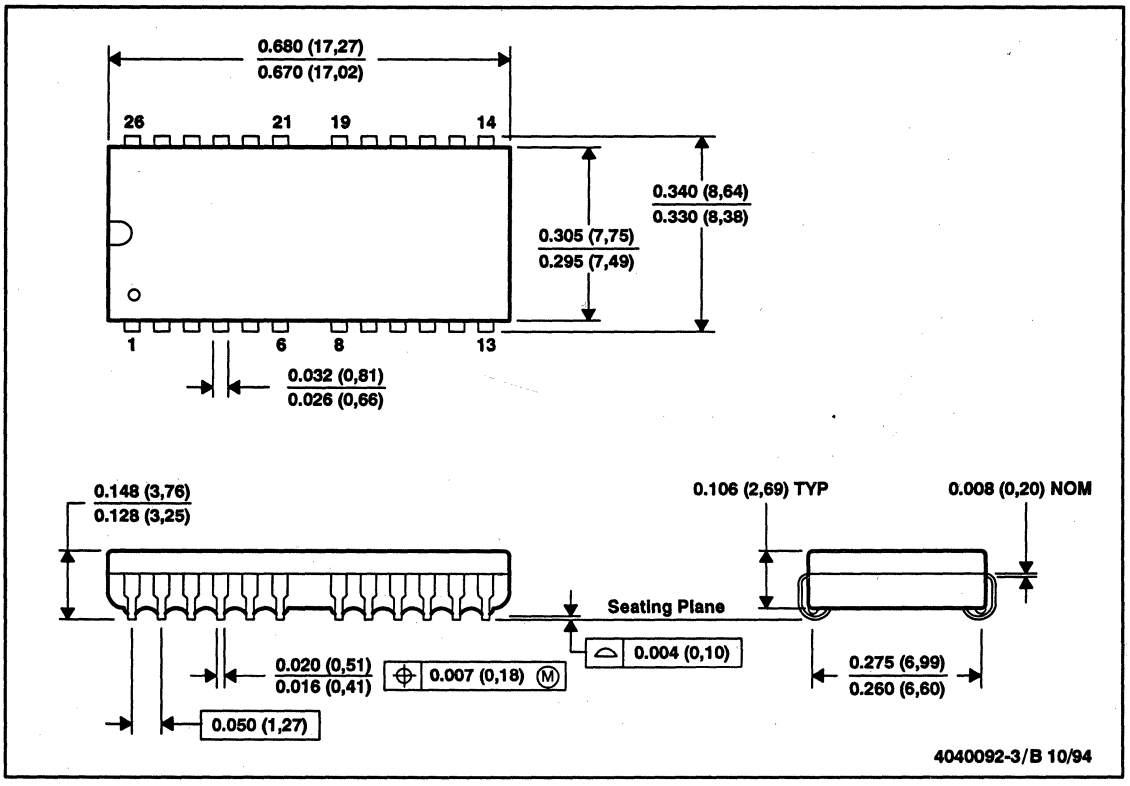


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

† Applicable MOS Memory Devices:

TMS44100	TMS44100P	TMS46100	TMS46100P	TMS44400	TMS44400P
TMS46400	TMS46400P				

DJ (R-PDSO-J24/26) **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE†**

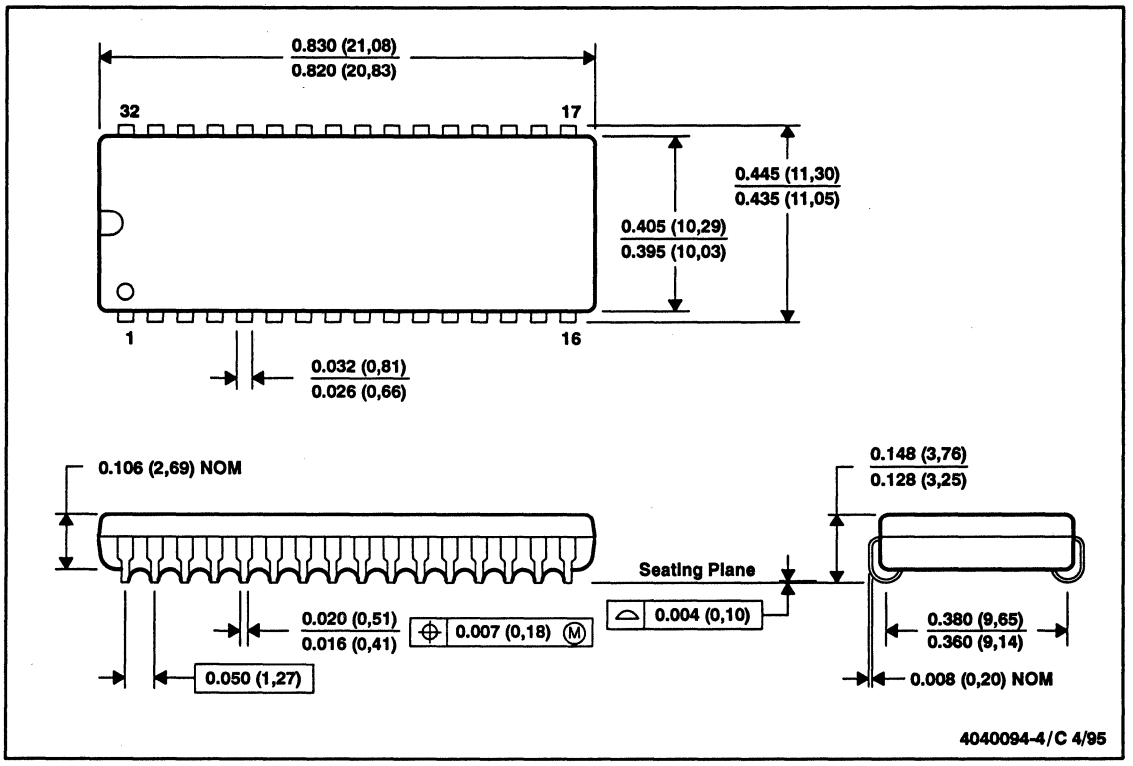


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

‡ Applicable MOS Memory Devices:

TMS44460	TMS44460P	TMS46460	TMS46460P	TMS416400	TMS416400P
TMS417400	TMS417400P	TMS426400	TMS426400P	TMS427400	TMS427400P

DZ (R-PDSO-J32) **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE†**

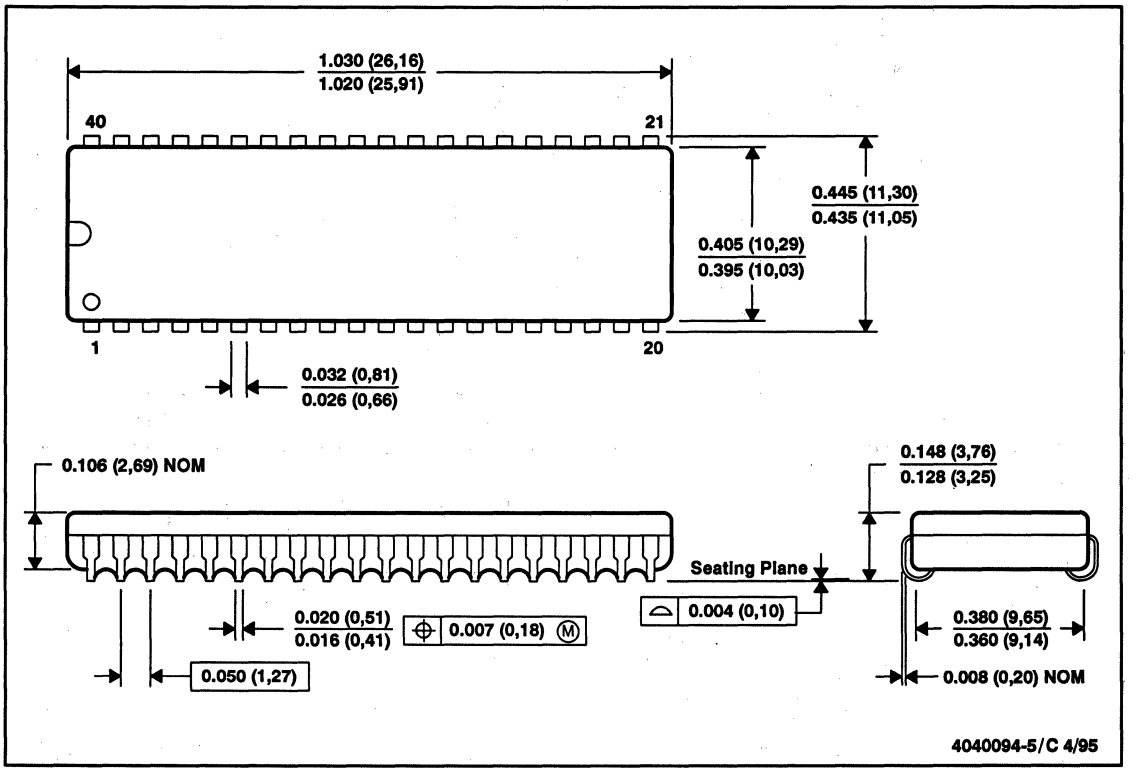


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

† Applicable MOS Memory Devices:

TMS464400 TMS464400P TMS464800 TMS464800P

DZ (R-PDSO-J40) **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE†**

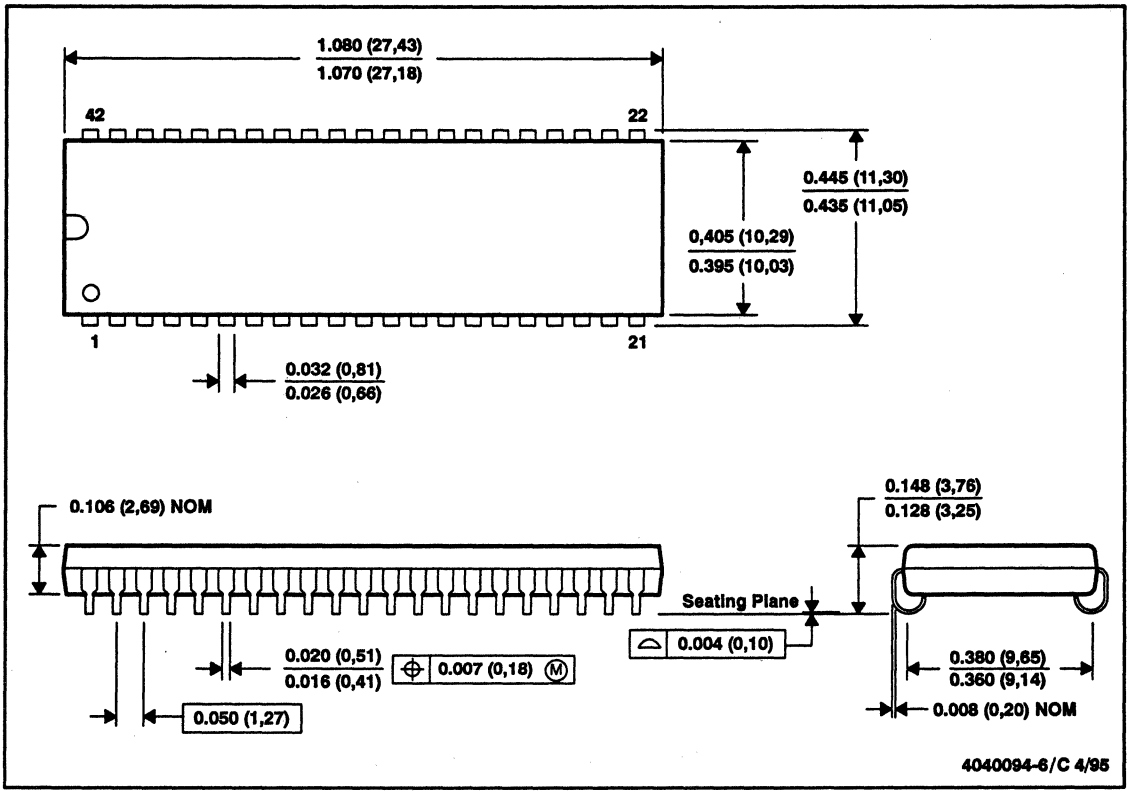


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

† Applicable MOS Memory Devices:

TMS44165 TMS44165P TMS45160 TMS45160P TMS45165 TMS45165P

DZ (R-PDSO-J42) **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE†**

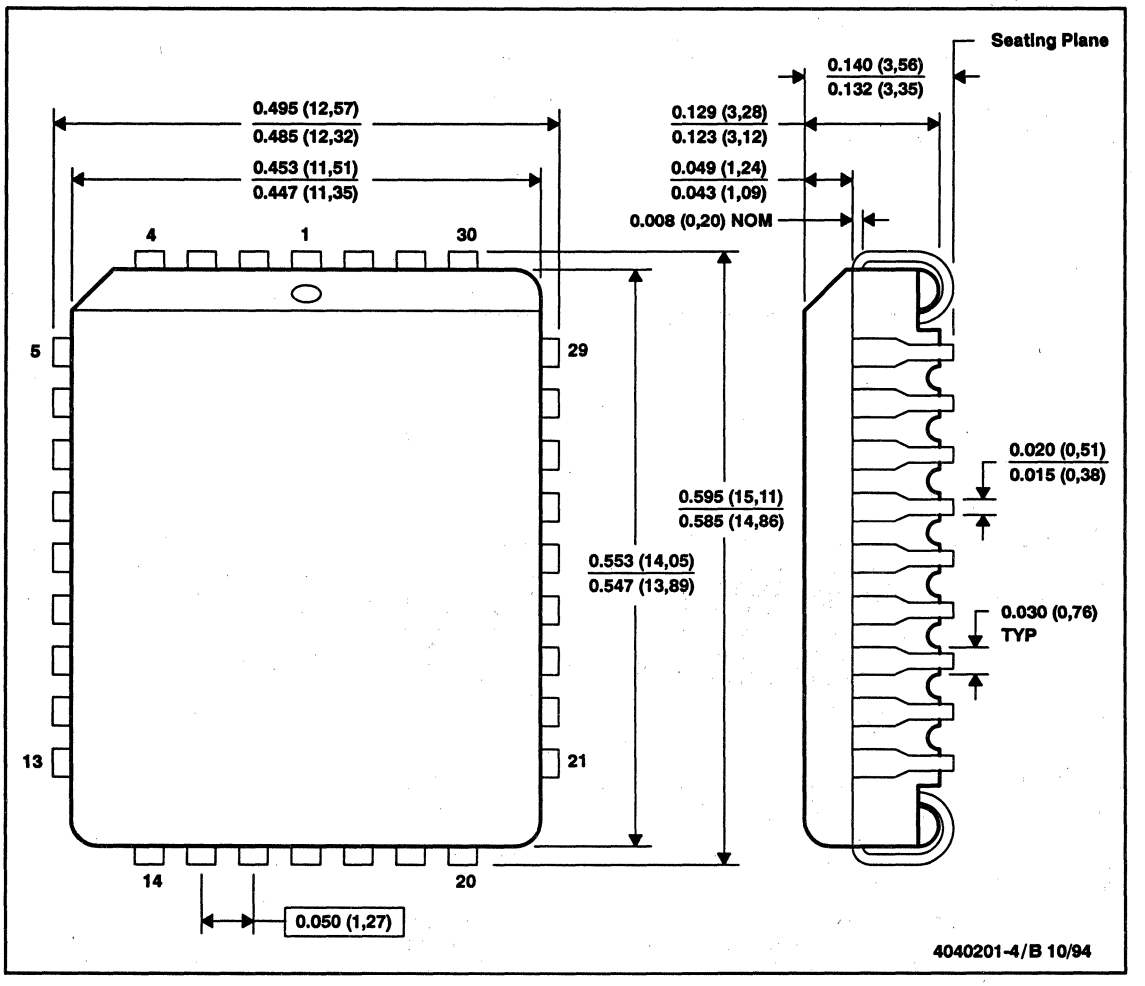


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

† Applicable MOS Memory Devices:

TMS416160	TMS416160P	TMS418160	TMS418160P	TMS426160	TMS426160P
TMS428160	TMS428160P	TMS416169	TMS416169P	TMS418169	TMS418169P
TMS426169	TMS426169P	TMS428169	TMS428169P		

FM (R-PQCC-J32) **PLASTIC J-LEADED CHIP CARRIER†**



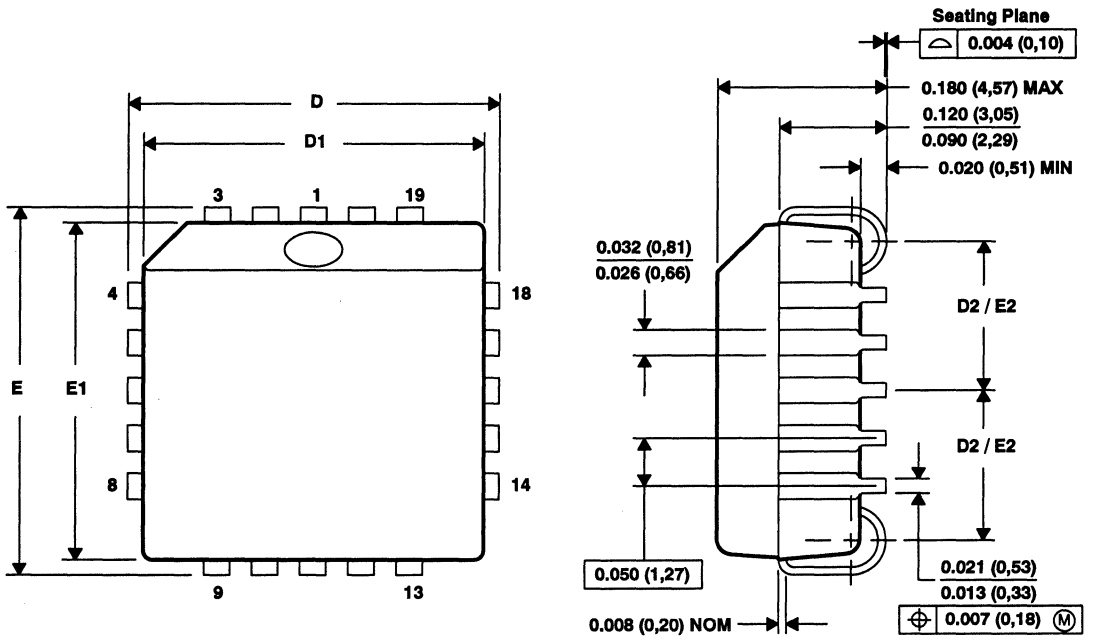
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

† Applicable MOS Memory Devices:

TMS28F512A	TMS28F010B	TMS28F020	TMS27PC256	TMS27PC510	TMS27PC512
TMS27PC010A	TMS27PC020	TMS27PC040			

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER†**

20 PIN SHOWN



NO. OF PINS **	D / E		D1 / E1		D2 / E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 10/94

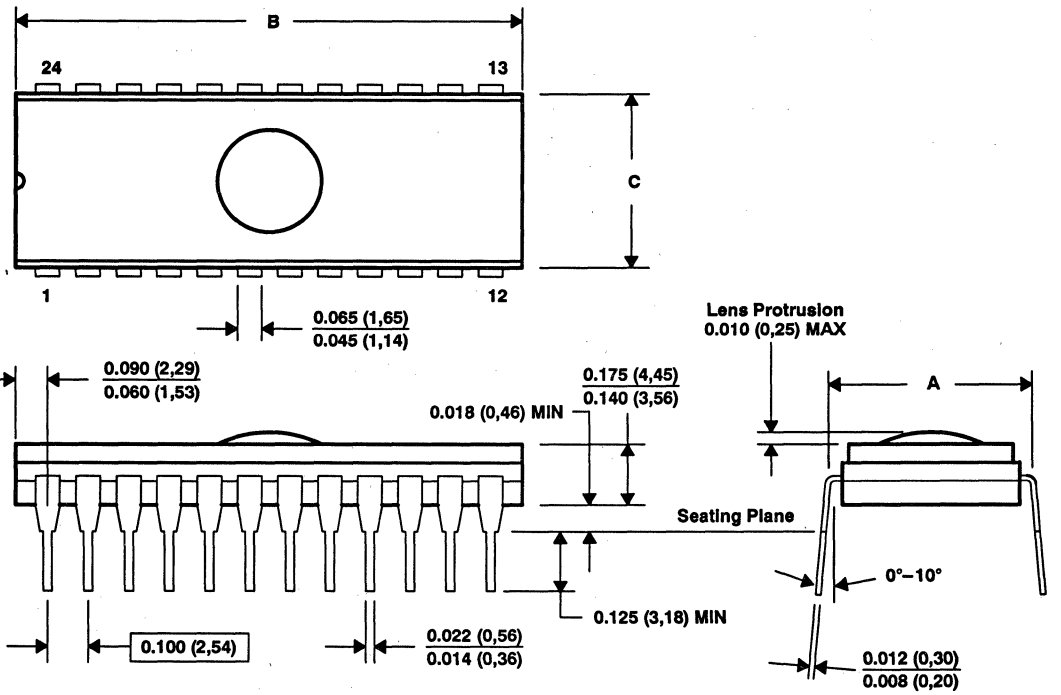
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

† Applicable MOS Memory Devices:

TMS28F210 TMS27PC210A TMS27PC240

J (R-CDIP-T*)** **CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE†**

24 PIN SHOWN



DIM	PINS**	24 NARR	24 WIDE	28 NARR	28 WIDE	32 NARR	32 WIDE	40 NARR	40 WIDE
A	MAX	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)
	MIN	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)
B	MAX	1.265(32,13)	1.265(32,13)	1.465(37,21)	1.465(37,21)	1.668(42,37)	1.668(42,37)	2.068(52,53)	2.068(52,53)
	MIN	1.235(31,37)	1.235(31,37)	1.435(36,45)	1.435(36,45)	1.632(41,45)	1.632(41,45)	2.032(51,61)	2.032(51,61)
C	MAX	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)
	MIN	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)

4040084/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only

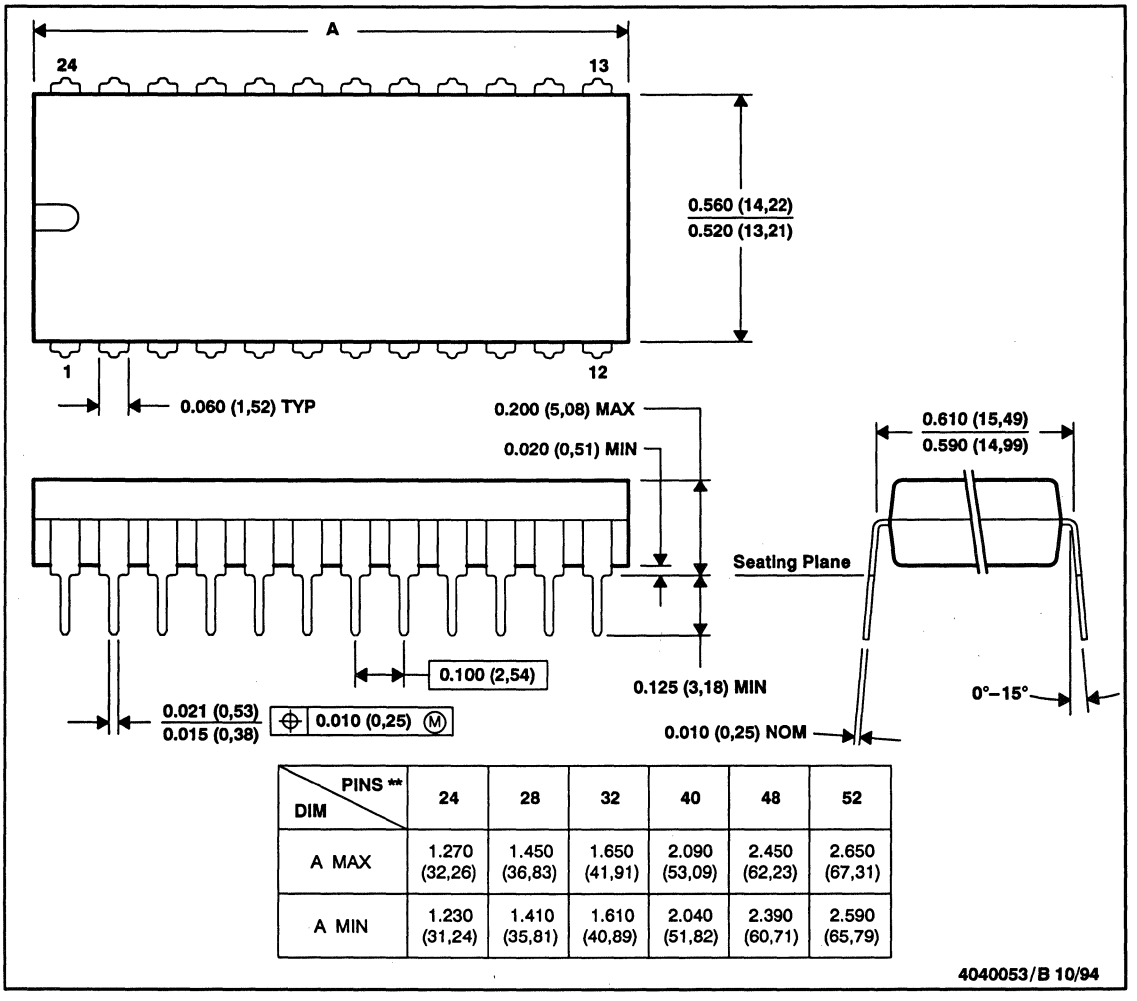
† Applicable MOS Memory Devices:

TMS27C256 TMS27C510 TMS27C512 TMS27C010A TMS27C210A TMS27C020
TMS27C040 TMS27C240

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE†

24 PIN SHOWN



DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

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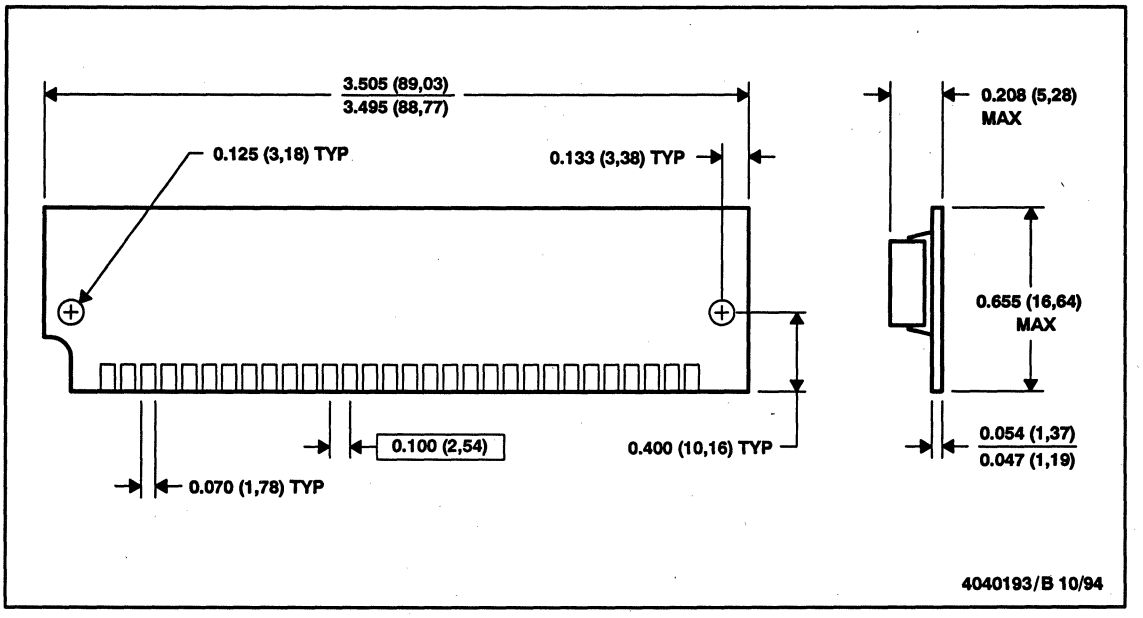
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

† Applicable MOS Memory Devices:

TMS28F512A TMS28F010B TMS28F210 TMS27PC256 TMS27PC510 TMS27PC512
TMS27PC010A

U (R-PSIM-N30) **SINGLE-IN-LINE MEMORY MODULE‡**

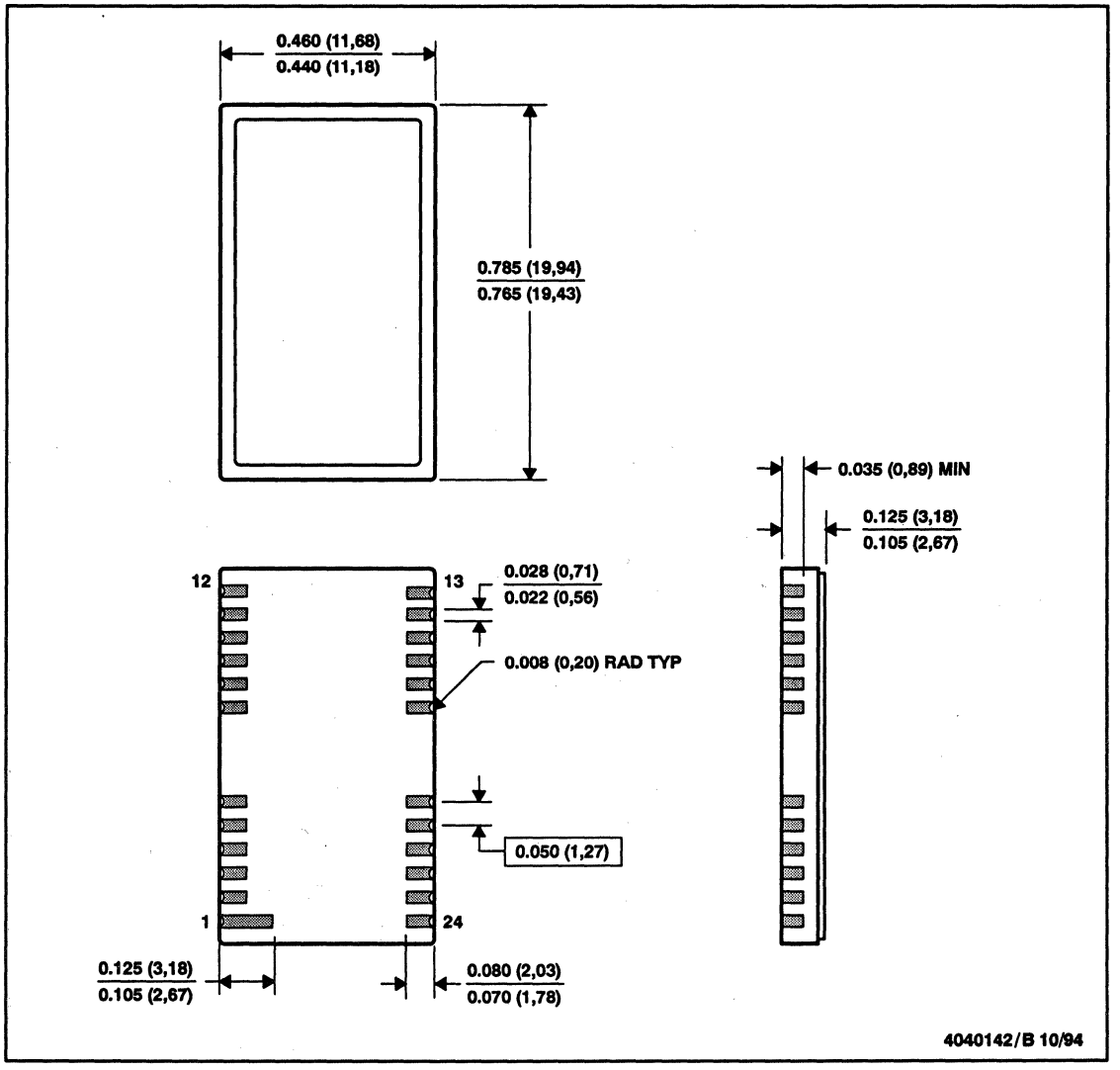


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

† Applicable MOS Memory Devices:

TM497GU8 TM497EU9

FNC (R-CDCC-N24/28) **LEADLESS CERAMIC CHIP CARRIER†**

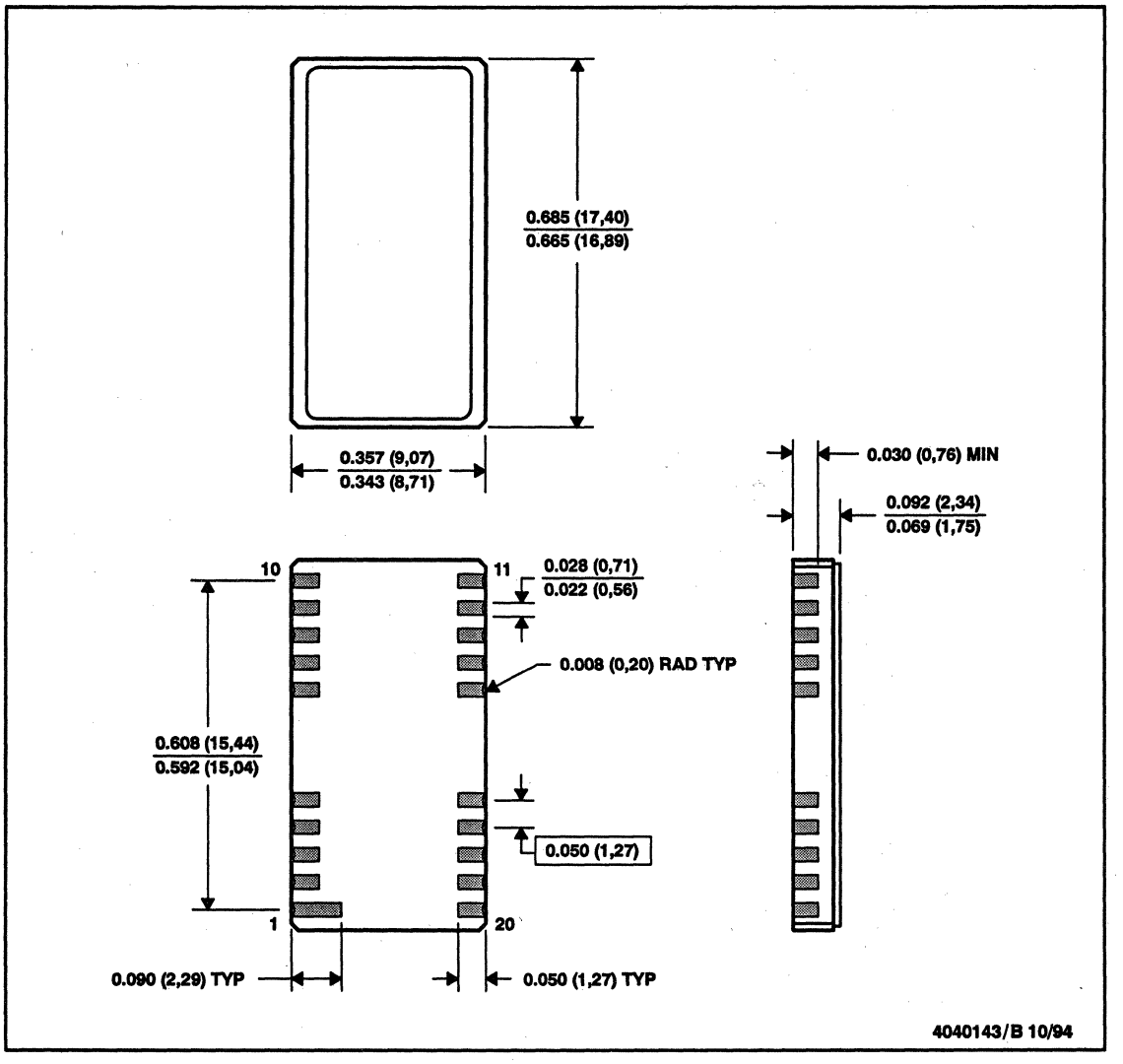


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

† Applicable MOS Memory Military Devices:

SMJ416100 SMJ416400

FQ (R-CDCC-N20) **LEADLESS CERAMIC CHIP CARRIER†**

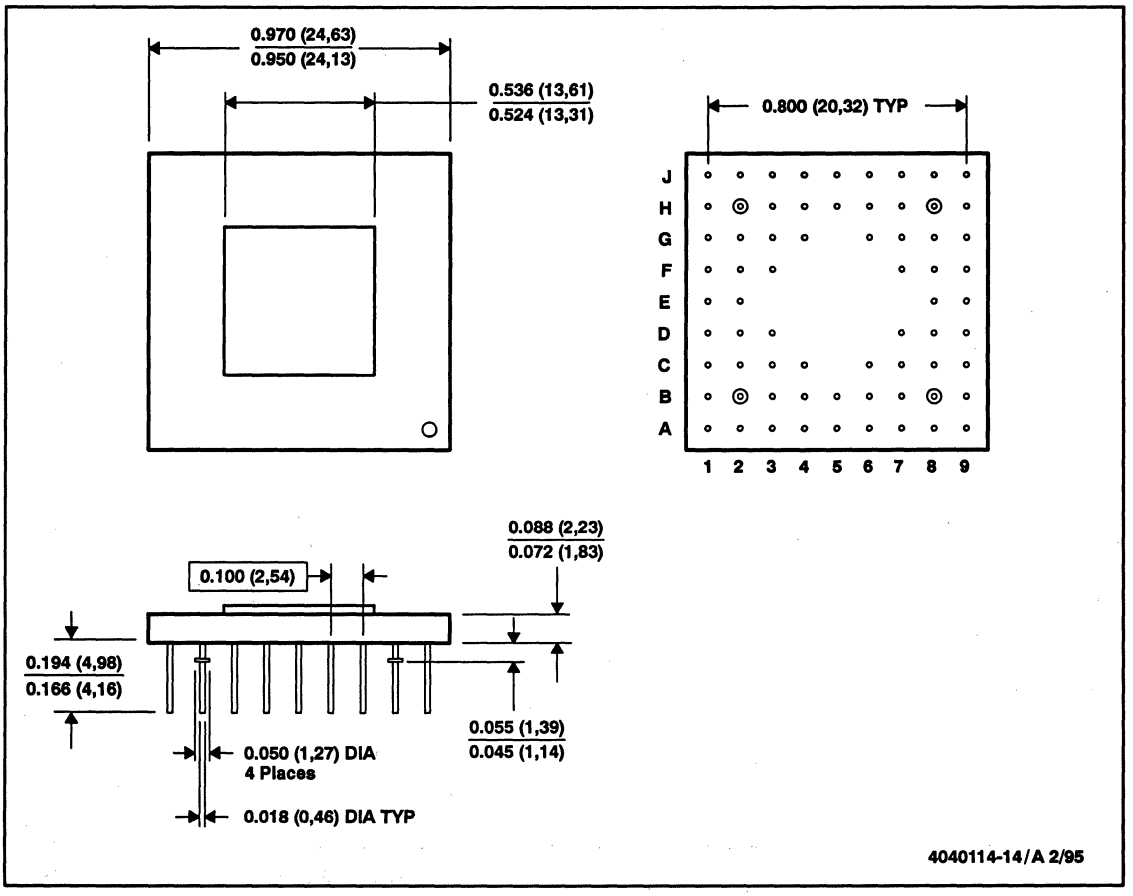


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

† Applicable MOS Memory Military Devices:

SMJ44C256 SMJ4C1024

GB (S-CPGA-P68) **CERAMIC PIN GRID ARRAY PACKAGE†**

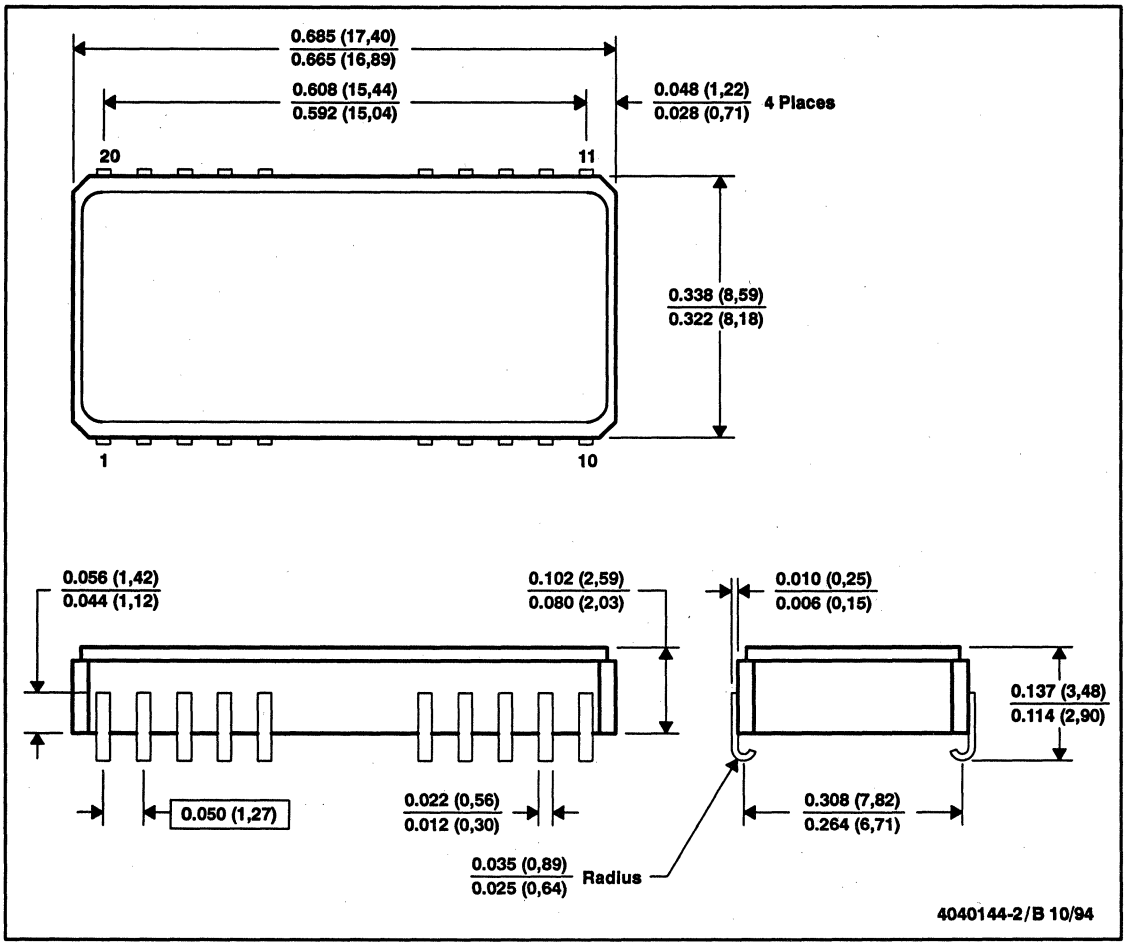


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Index mark may appear on top or bottom depending on package vendor.
D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
F. The pins can be gold plated or solder dipped.
G. Falls within MIL-STD-1835 CMGA1-PN and CMGA13-PN and JEDEC MO-067AA and MO-066AA, respectively

† Applicable MOS Memory Military Devices:

SMJ55161 SMJ55166

HJ (R-CDCC-J20) **J-LEADED CERAMIC CHIP CARRIER†**

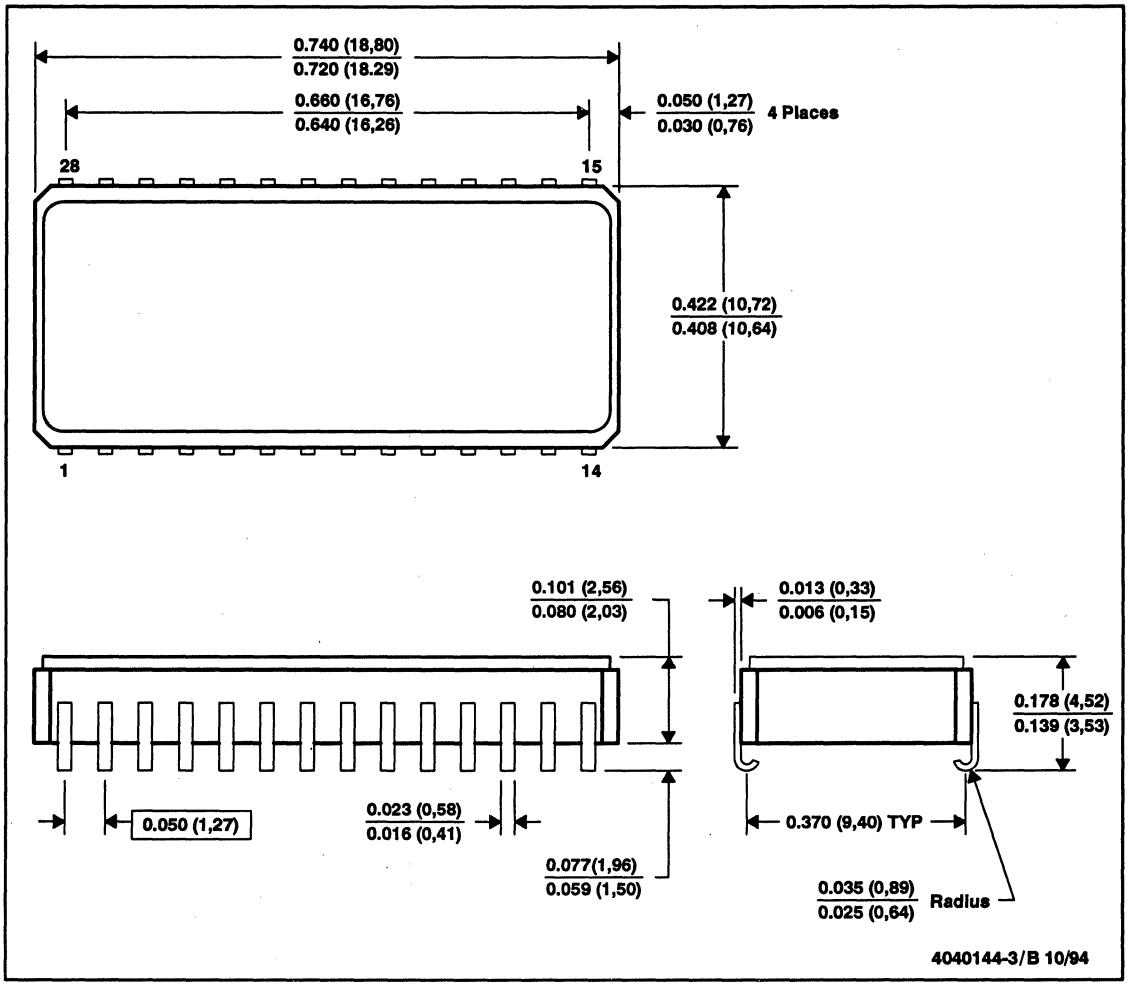


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

† Applicable MOS Memory Military Devices:

SMJ44C256 SMJ4C1024

HJ (R-CDCC-J28) **J-LEADED CERAMIC CHIP CARRIER†**

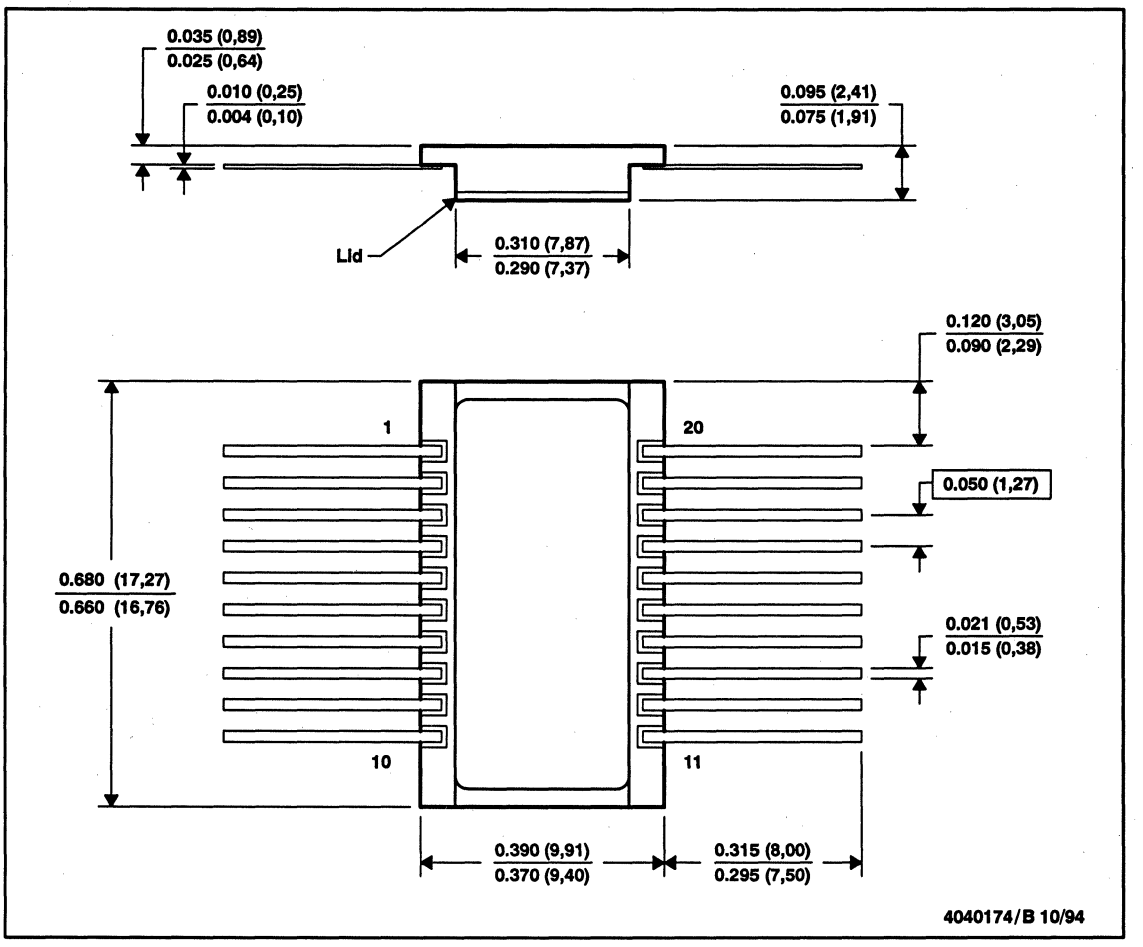


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

† Applicable MOS Memory Military Devices:

SMJ44C251B

HK (R-CDFP-F20) **CERAMIC DUAL FLATPACK†**

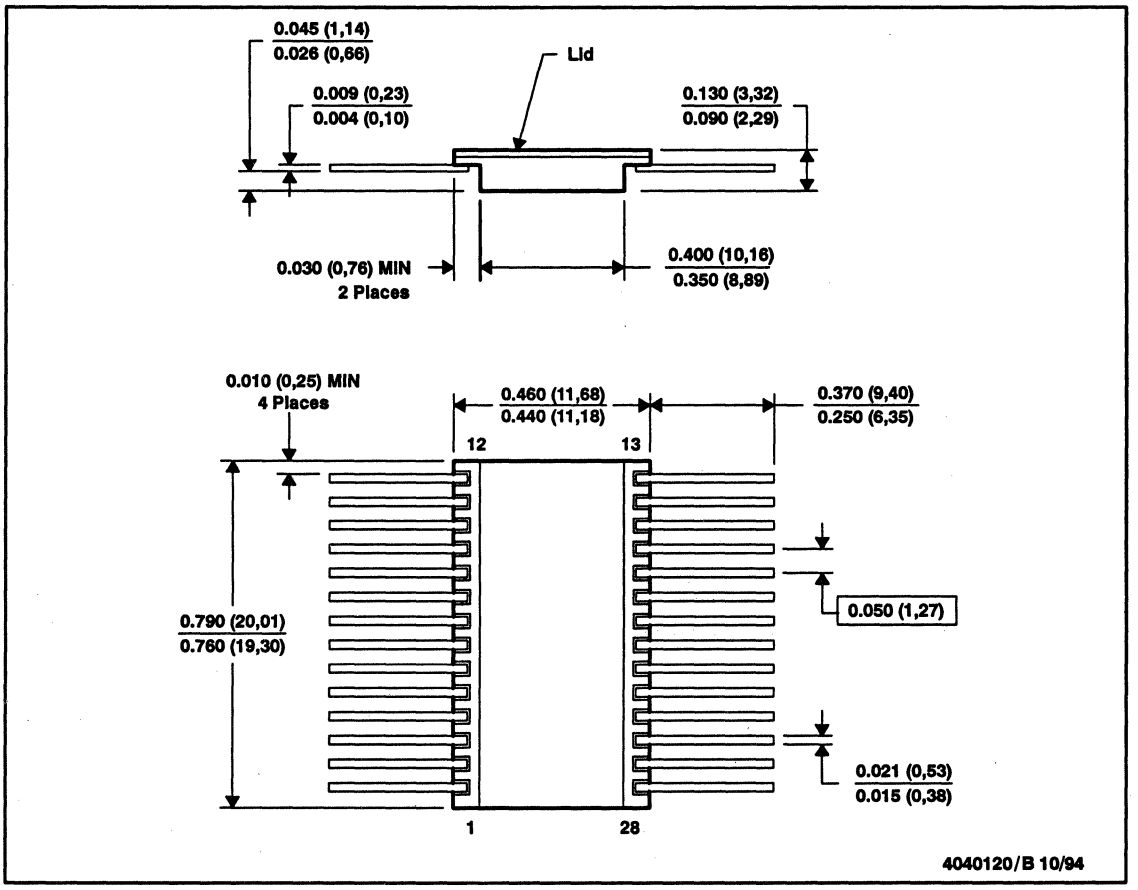


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

† Applicable MOS Memory Military Devices:

SMJ4C1024 SMJ44C256

HKB (R-CDFP-F28) **CERAMIC DUAL FLATPACK†**

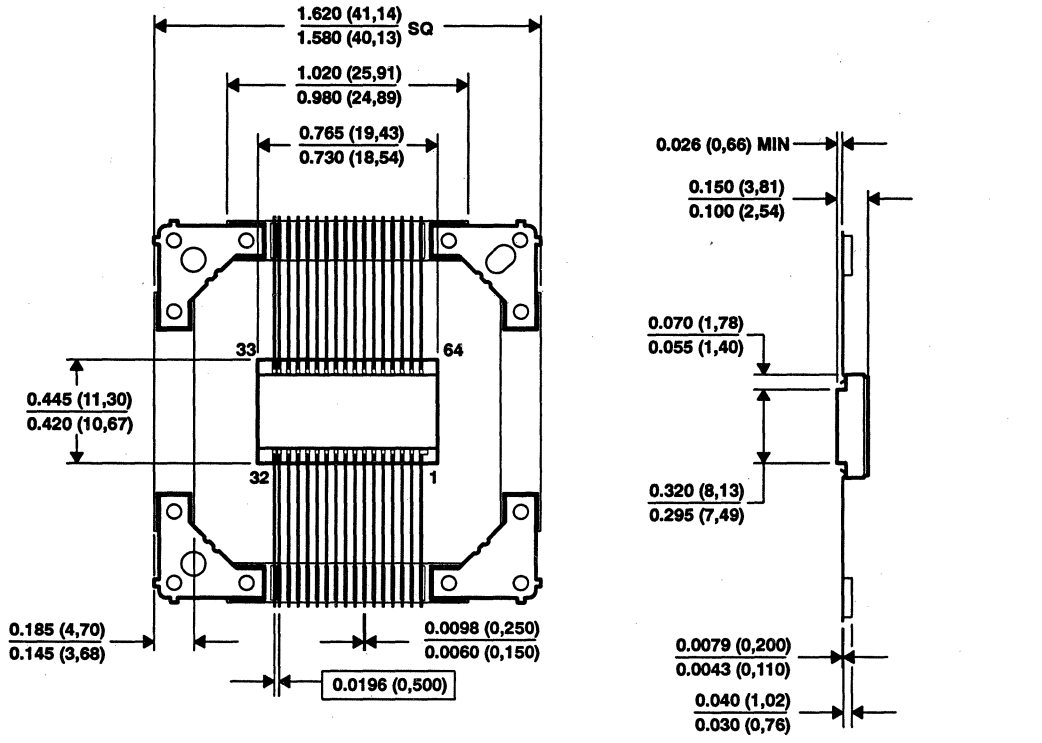


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

† Applicable MOS Memory Military Devices:

SMJ416100 SMJ416400

HKC (R-CDFP-F64) **CERAMIC DUAL FLATPACK WITH TIE BAR†**

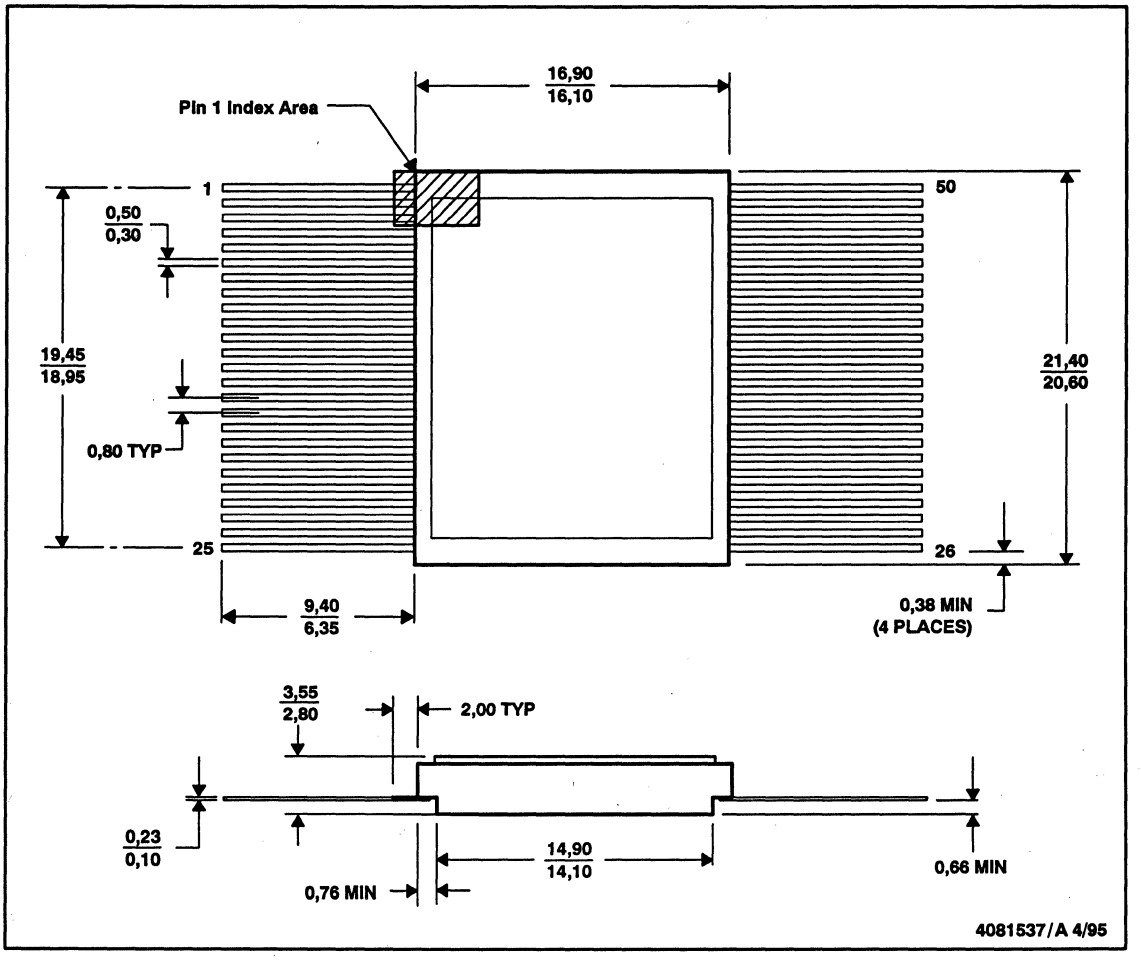


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. All leads not shown for clarity purposes.

† Applicable MOS Memory Military Devices:

SMJ55161 SMJ55166

HKD (R-CDFP-F50) **CERAMIC DUAL FLATPACK†**

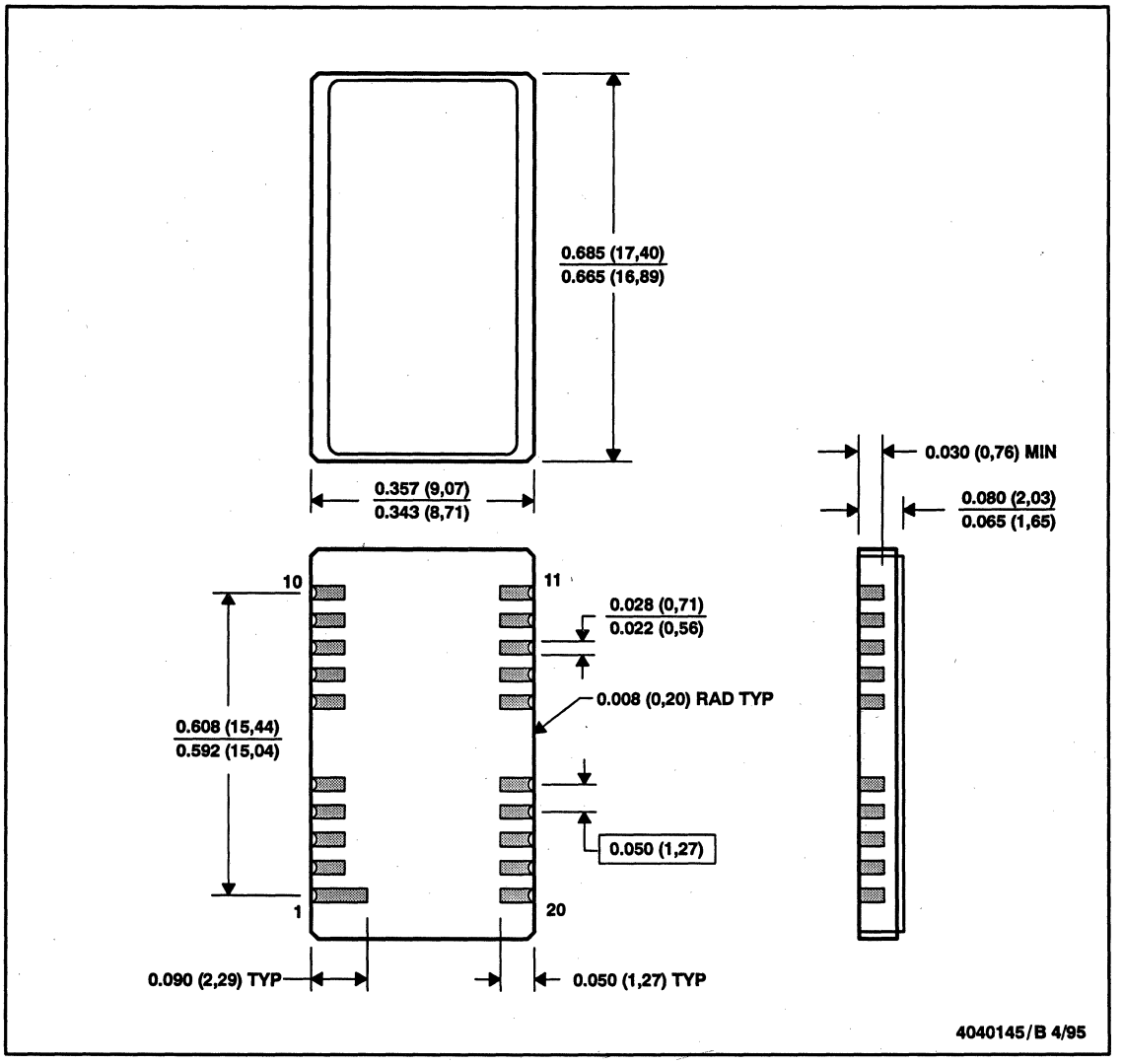


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

† Applicable MOS Memory Military Devices:

SMJ416160 SMJ418160

HL (R-CDCC-N20/26) **LEADLESS CERAMIC CHIP CARRIER†**

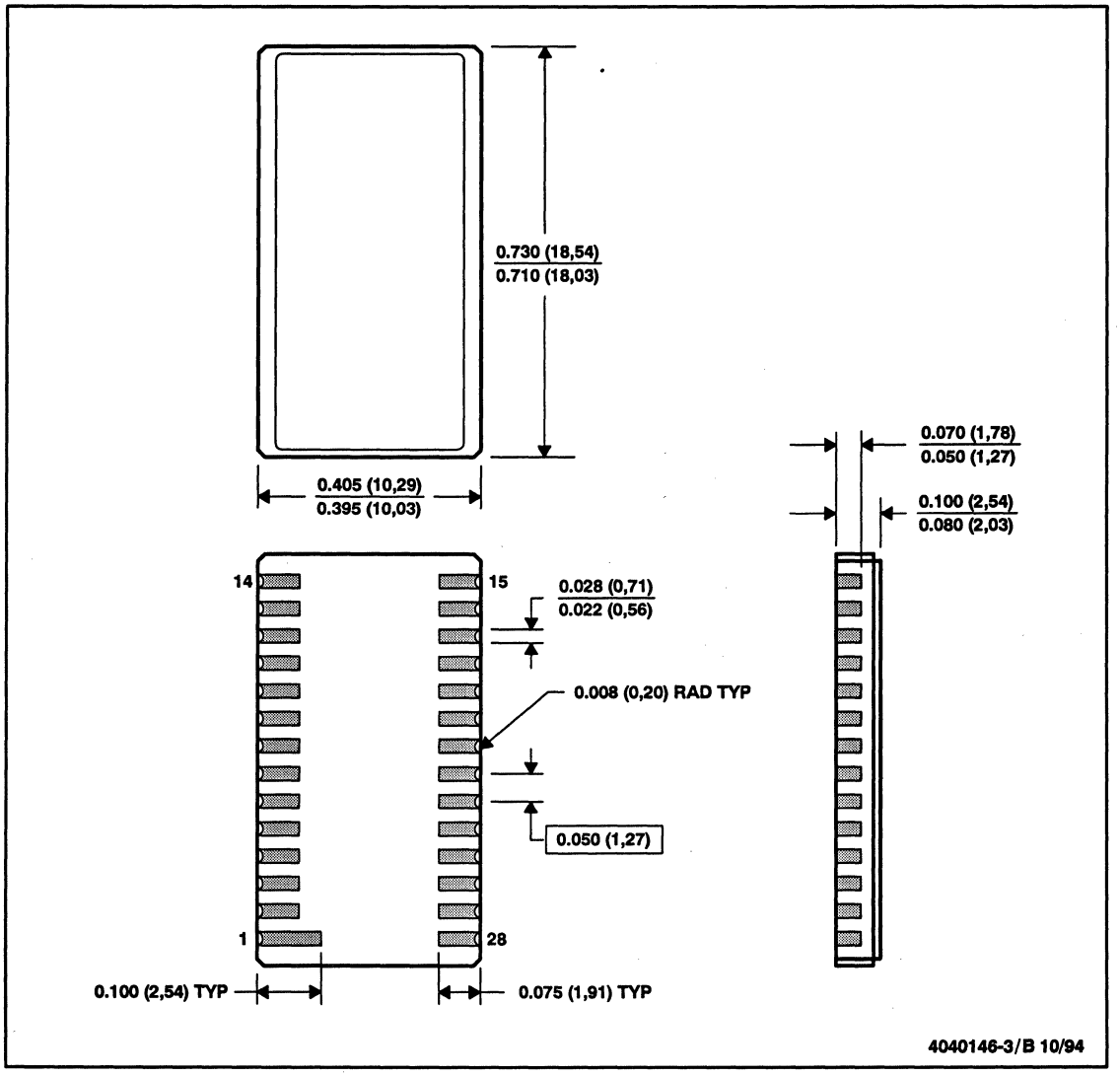


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

† Applicable MOS Memory Military Devices:

SMJ44C256 SMJ4C1024 SMJ44100 SMJ44400

HM (R-CDCC-N28) **LEADLESS CERAMIC CHIP CARRIER†**

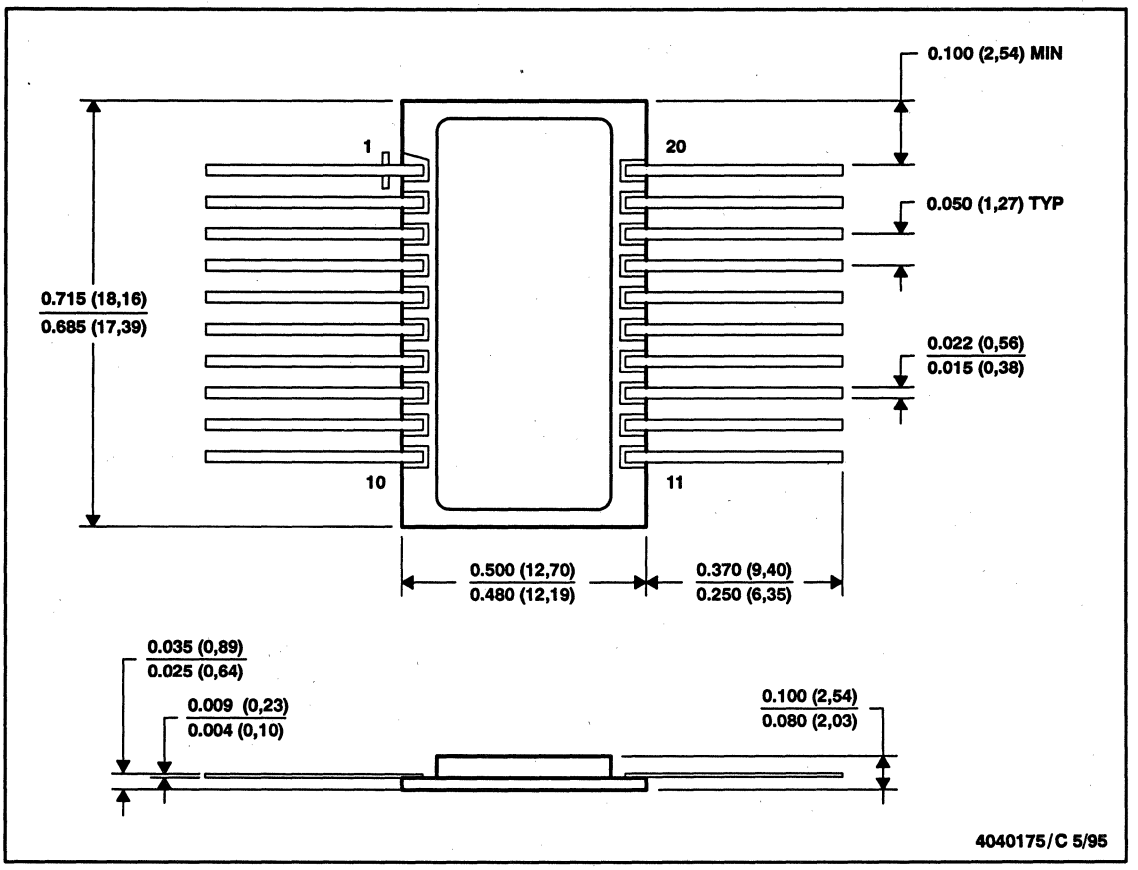


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

† Applicable MOS Memory Military Devices:

SMJ44C251B

HR (R-CDFP-F20) **CERAMIC DUAL FLATPACK†**



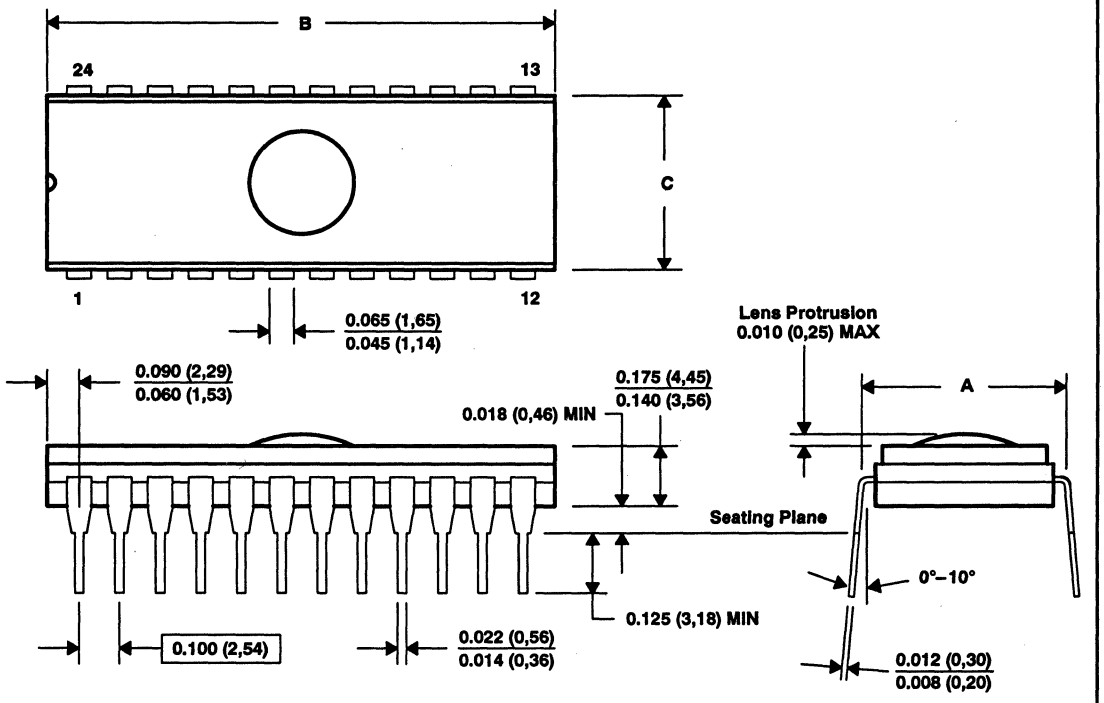
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.

† Applicable MOS Memory Military Devices:

SMJ44100 SMJ44400

J (R-CDIP-T)** **CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE†**

24 PIN SHOWN



DIM \ PINS**		24		28		32		40	
		NARR	WIDE	NARR	WIDE	NARR	WIDE	NARR	WIDE
A	MAX	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)
	MIN	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)
B	MAX	1.265(32,13)	1.265(32,13)	1.465(37,21)	1.465(37,21)	1.668(42,37)	1.668(42,37)	2.068(52,53)	2.068(52,53)
	MIN	1.235(31,37)	1.235(31,37)	1.435(36,45)	1.435(36,45)	1.632(41,45)	1.632(41,45)	2.032(51,61)	2.032(51,61)
C	MAX	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)
	MIN	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)

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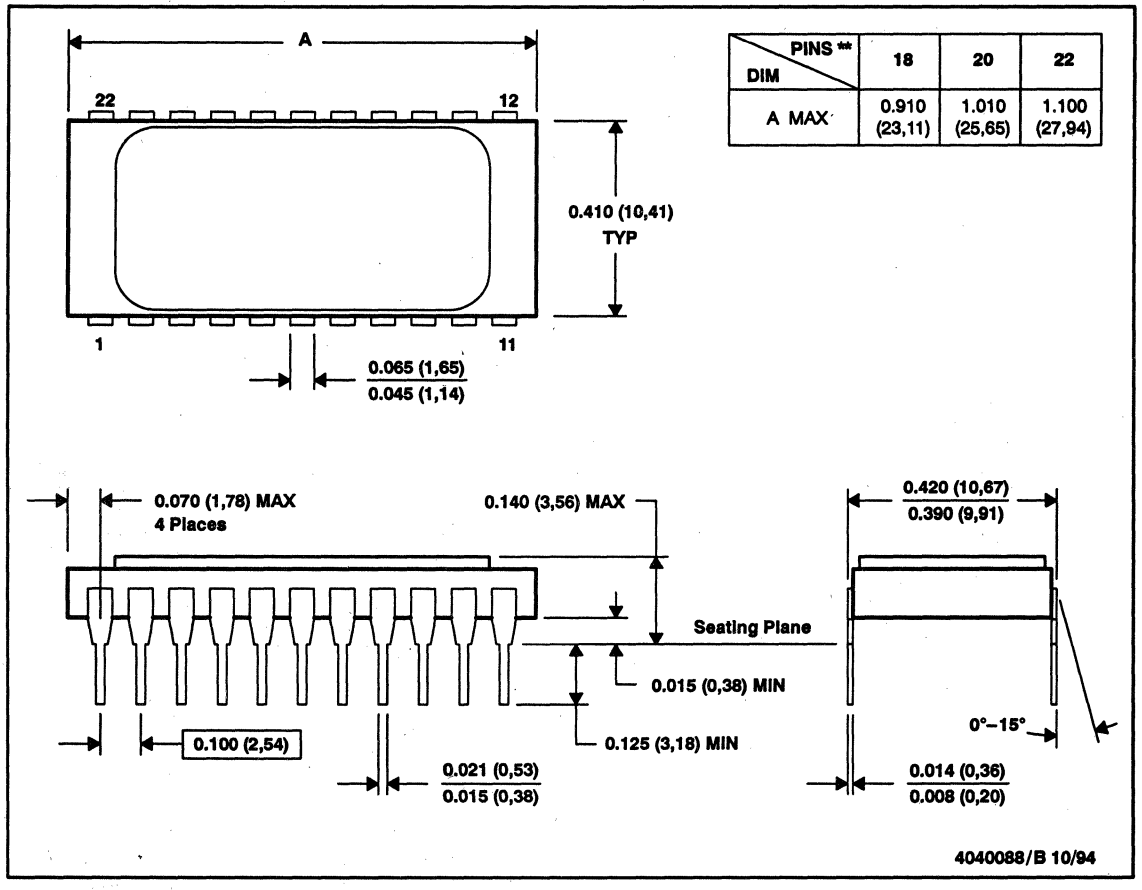
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only

† Applicable MOS Memory Military Devices:

SMJ27C128 SMJ27C040

JD(R-CDIP-T)** **CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE†**

22 PIN SHOWN



PINS ** / DIM	18	20	22
A MAX	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

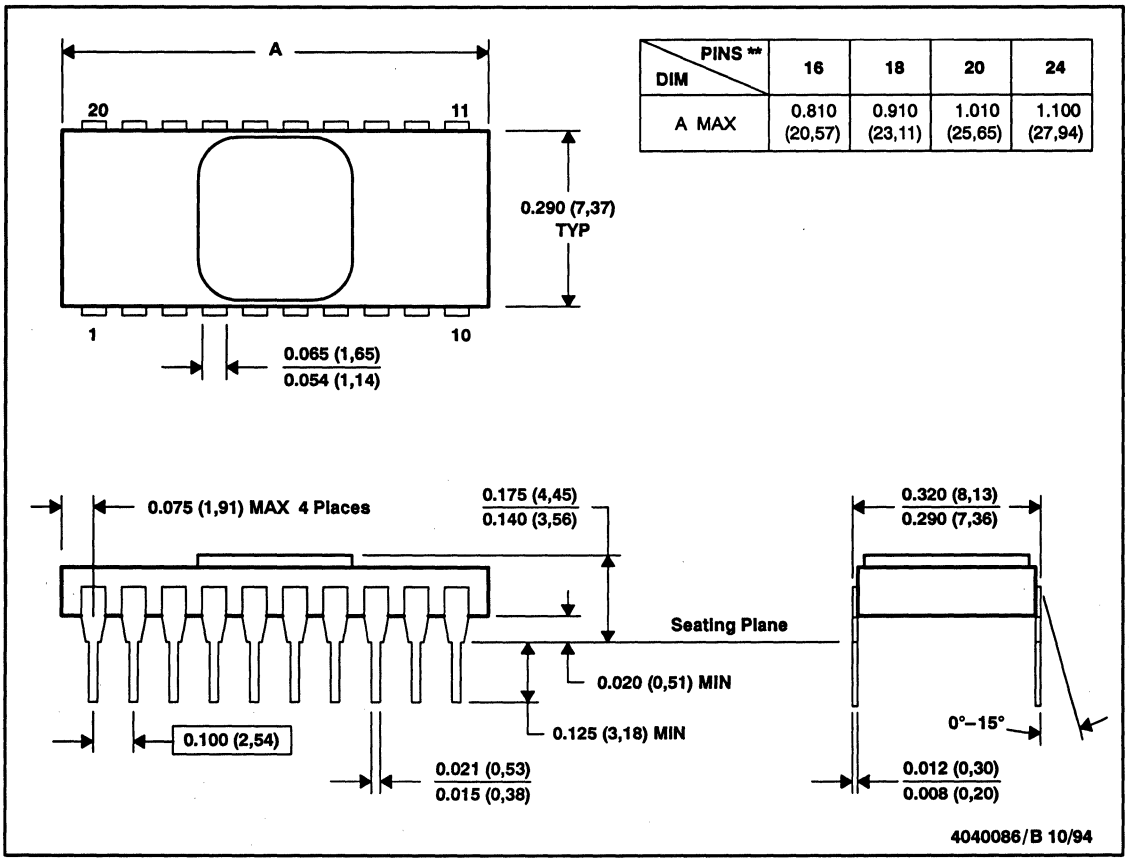
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

† Applicable MOS Memory Military Devices:

SMJ44100

JD (R-CDIP-T)** **CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE†**

20 PIN SHOWN



DIM \ PINS **	16	18	20	24
A MAX	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

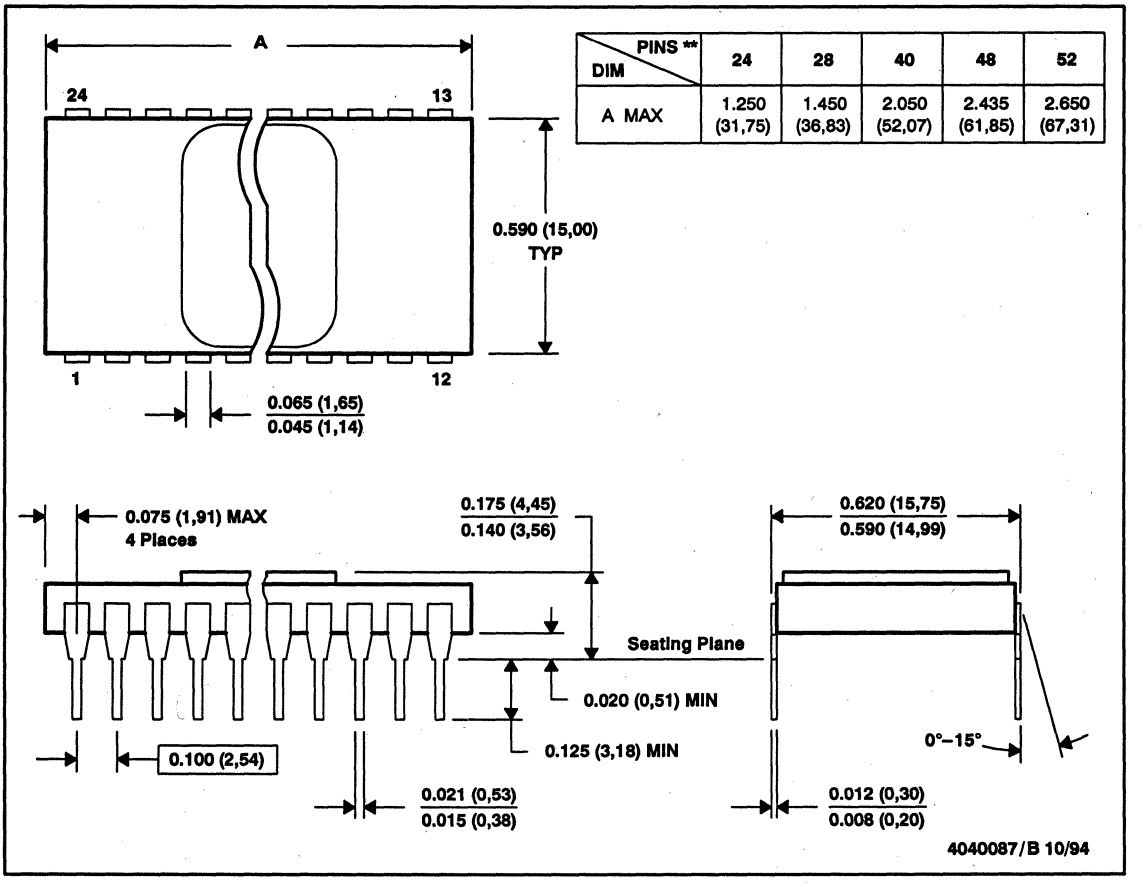
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

† Applicable MOS Memory Military Devices:

SMJ44C256 SMJ4C1024

JD (R-CDIP-T)** **CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE†**

24 PIN SHOWN



DIM \ PINS **	24	28	40	48	52
A MAX	1.250 (31,75)	1.450 (36,83)	2.050 (52,07)	2.435 (61,85)	2.650 (67,31)

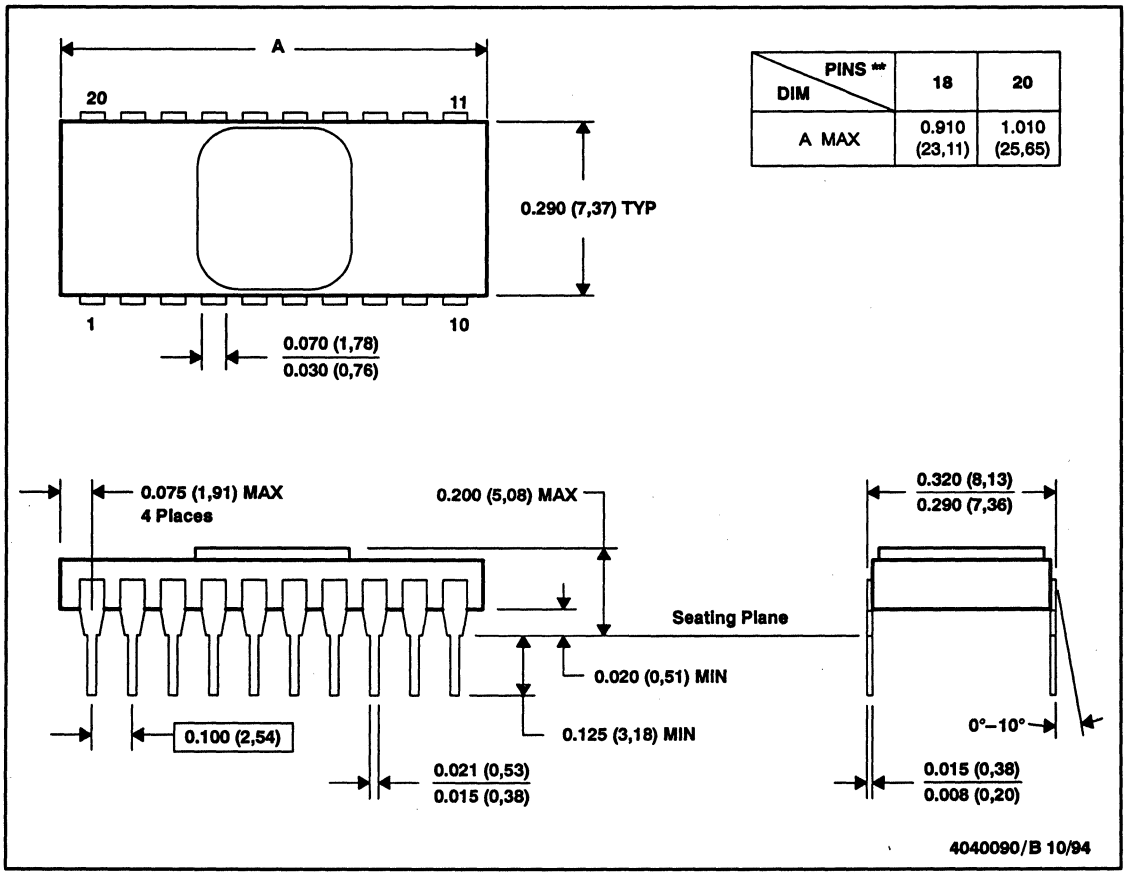
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

† Applicable MOS Memory Military Devices:

SMJ44C251B

JDB (R-CDIP-T)** **CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE†**

20 PIN SHOWN



DIM \ PINS **	18	20
A MAX	0.910 (23,11)	1.010 (25,65)

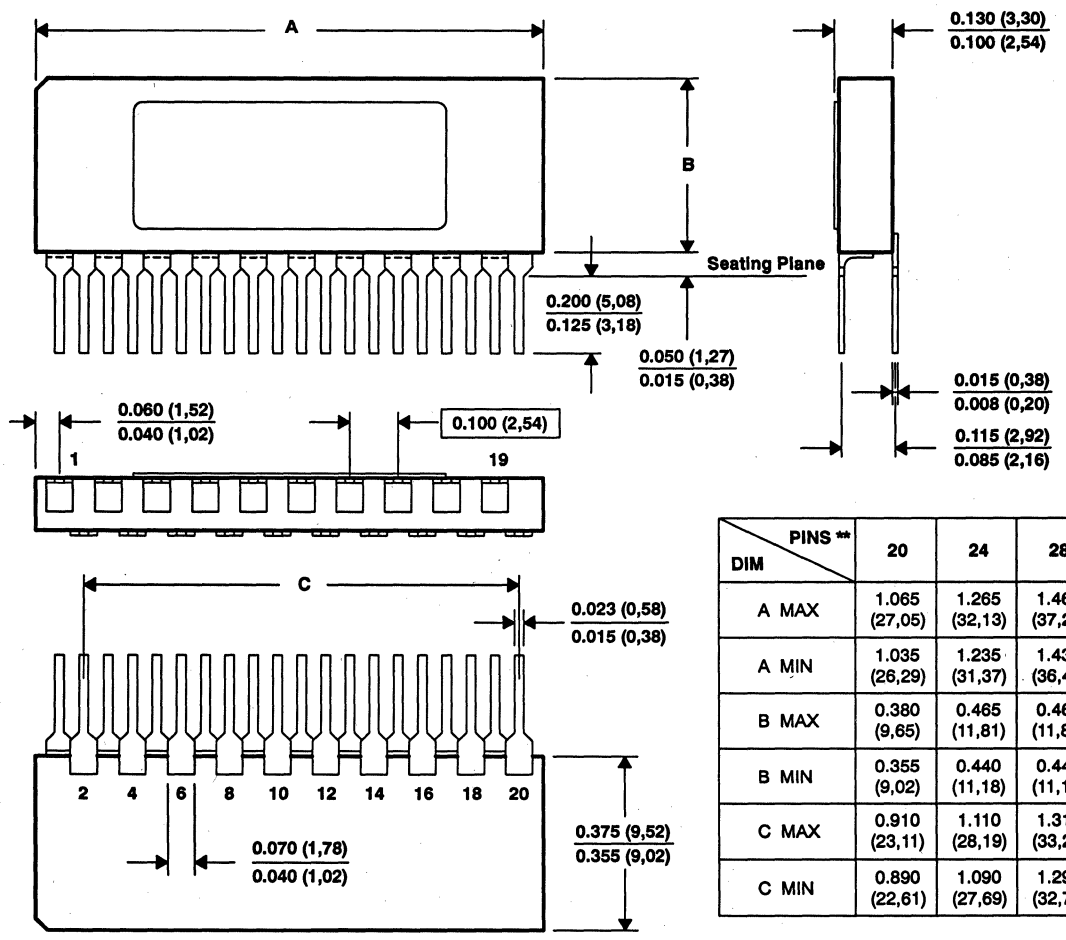
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within MIL-STD-1835 GDIP1-T18, GDIP1-T20 and JEDEC MS-015 AD, MS-015 AE

† Applicable MOS Memory Military Devices:

SMJ44100 SMJ44400

SV (R-CZIP-T)** **CERAMIC ZIG-ZAG PACKAGE†**

20 PIN SHOWN



DIM \ PINS **	20	24	28
A MAX	1.065 (27,05)	1.265 (32,13)	1.465 (37,21)
A MIN	1.035 (26,29)	1.235 (31,37)	1.435 (36,45)
B MAX	0.380 (9,65)	0.465 (11,81)	0.465 (11,81)
B MIN	0.355 (9,02)	0.440 (11,18)	0.440 (11,18)
C MAX	0.910 (23,11)	1.110 (28,19)	1.310 (33,27)
C MIN	0.890 (22,61)	1.090 (27,69)	1.290 (32,77)

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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
† Applicable MOS Memory Military Devices:

SMJ44C256 SMJ4C1024 SMJ44400 SMJ416400 SMJ44C251B

EXPLANATION OF IEEE/IEC LOGIC SYMBOLS FOR MEMORIES

Introduction

The International Electrotechnical Commission (IEC) has developed a very powerful symbolic language that shows the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which is partially explained below.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

The current standards are IEC Publication 617-12, 1983 and ANSI/IEEE Standard 91-1984. Most of the data sheets in this data book include symbols prepared in accordance with these standards. The explanation that follows is necessarily brief and greatly condensed from the explanation given in the standards. This explanation is not intended to be sufficient for people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book.

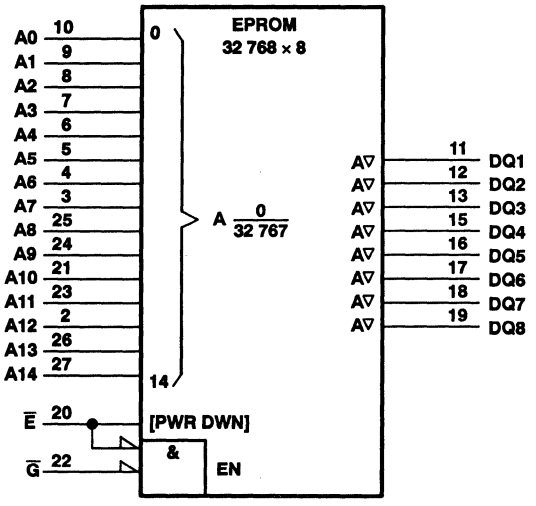
Explanation of a Typical Symbol For a Static Memory

The TMS27C400 symbol is explained in detail. This symbol includes almost all of the features found in the OTP PROMs and EPROMs.

The address inputs are arranged in order of their assigned binary weights and the range of addresses is shown as A$\frac{m}{n}$ where m is the decimal equivalent of the lowest address and n is the highest. The outputs affected by these addresses are indicated by the letter A, as data inputs also would be if the device were a RAM.

The polarity indicator ⊾ indicates that the external low level causes the internal 1-state (the active or asserted state) at an input or that the internal 1-state causes the external low level at an output. The effect is similar to specifying positive logic and using the negation symbol o.

The TMS27C400 Symbol



The ▽ symbols indicate 3-state outputs. The 3-state outputs are always controlled by an EN function. When EN stands at its internal 1-state, the outputs are enabled; when EN stands at its internal 0-state, the outputs stand at their high-impedance states. Sometimes the EN is a single input, but in the illustrated case, it is the output of a two-input AND gate. Both inputs (pins 20 and 22) are active low, so if one of them goes high, the outputs is disabled. The upper one of these two inputs (pin 20) has another function. When nonstandard labels and explanatory labels are used within symbols, they are enclosed within square brackets. Here we find the label "[PWR DWN]". This is intended to indicate that if pin 20 is high, the memory will go to a low-power standby state.

The Basics

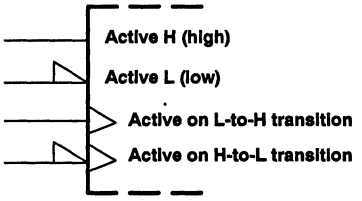
The next section shows the most common building blocks that are used in constructing symbols for memories. On the left are shown the symbols that specify the active levels for level-operated inputs and the direction of active transition for dynamic inputs.

It is preferred to show all input lines on the left and all output lines on the right. When an exception is made to this left-to-right signal flow, an arrowhead is used to show the reverse signal flow. Three symbols are shown that indicate 3-state, open-drain, and open-source outputs. If none of these is used, the output should be assumed to be totem-pole. The common control block is a point of replacement for inputs that affect an array of elements.

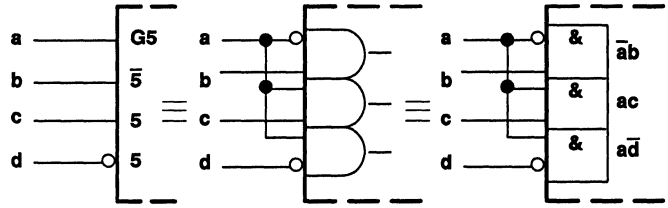
The drawings on the right define the three forms of dependency notation used in this book. At an input (or output) that affects other inputs or outputs, a letter (G, C, or Z) is placed followed by a number. That same number is placed at the affected inputs and outputs. The letter G indicates that an AND relationship exists; if the affecting input stands at the 0-state, it imposes that 0-state on the affected input or output. The letter C indicates a control relationship, usually between clock and a D (data) input. If the C input stands at its 0-state, the affected input is disabled. A D input is always an input to a storage element, which it either sets to the 1-state or resets to the 0-state, unless the D input is disabled to have no effect. Z dependency is used to transfer a signal from one place in a symbol to another, for example from the output at Z4 across to a terminal labeled "4", or from the output at Z5 back to the "5" where it serves as an input with no terminal attached.

Diagrammatic Summary

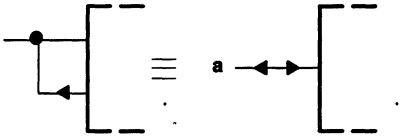
INPUTS



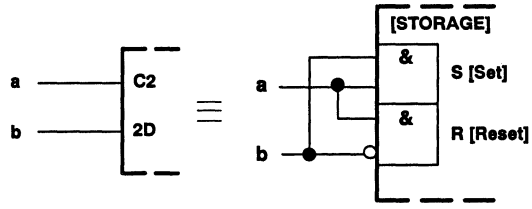
G (AND) DEPENDENCY



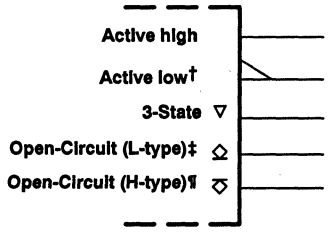
INPUT/OUTPUT



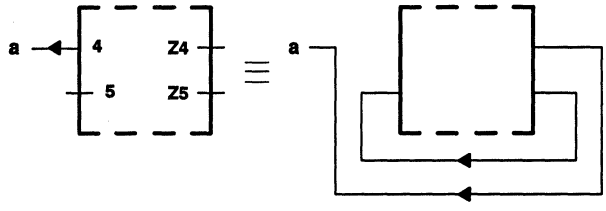
C (CONTROL) DEPENDENCY



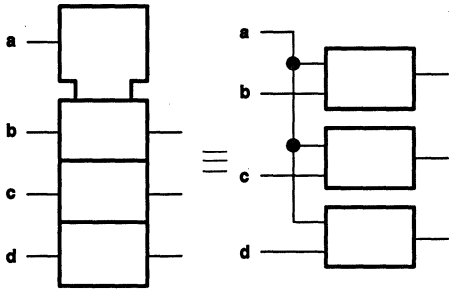
OUTPUTS



Z (INTERCONNECTION) DEPENDENCY



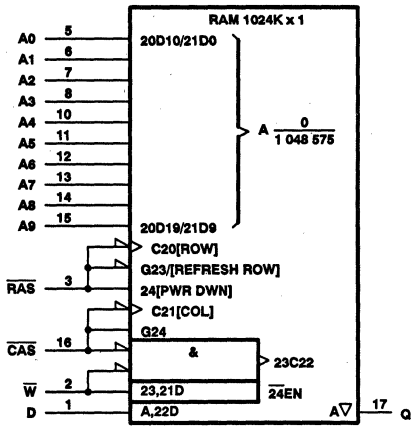
COMMON CONTROL BLOCK



† The active-low indicator may be used in combination with the 3-state and open-circuit indicators.
‡ L-types include N-channel open-drain and P-channel open-source outputs.
¶ H-types include P-channel open-drain and N-channel open-source outputs.

Explanation of a Typical Symbol for a Dynamic Memory

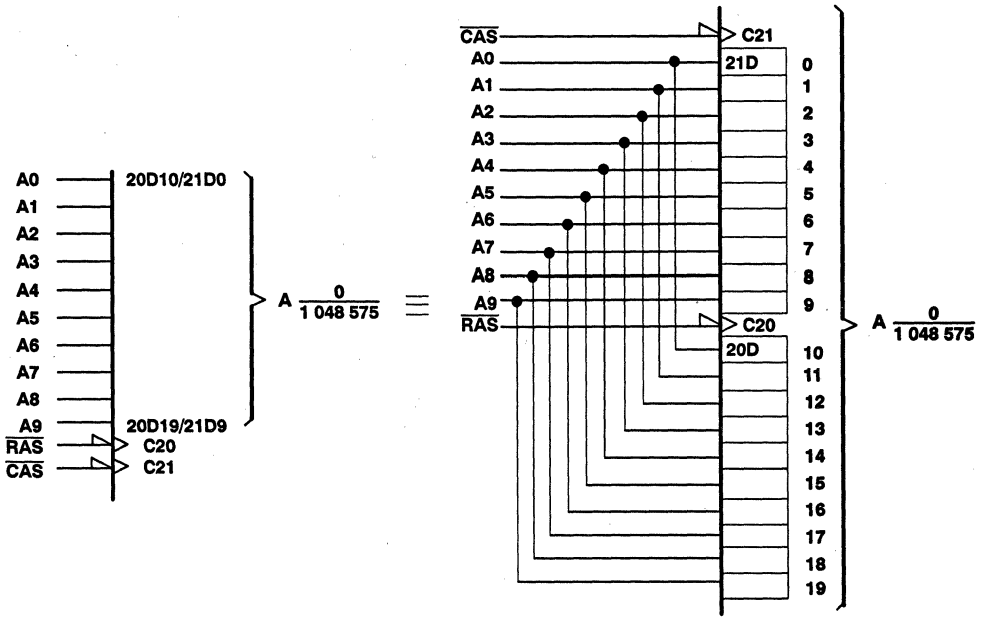
The TMS4C1024 Symbol



The TMS4C1024 symbol will be explained in detail for each operating function. The assumption is made that the previous sections have been read and understood. While this symbol is complex, so is the device it represents and the symbol shows how the part will perform depending on the sequence in which signals are applied.

Addressing

The symbol above makes use of an abbreviated form to show the multiplexed, latched addresses. The blocks representing the address latches are implied but not shown.



When $\overline{RAS}$ goes low, it momentarily enables (through C20, ▷ indicates a dynamic input) the D inputs of the ten address registers 10 through 19. When $\overline{CAS}$ goes low, it momentarily enables (through C21) the D inputs of the ten address registers 0 through 9. The outputs of the address registers are in 20 internal address lines that select 1 of 1 048 576 cells.

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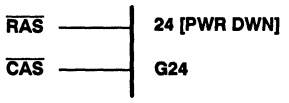
Refresh

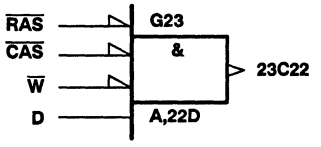
When $\overline{RAS}$ goes low, row refresh starts. It ends when $\overline{RAS}$ goes high. The other input signals required for refreshing are not indicated by the symbol.

Power Down



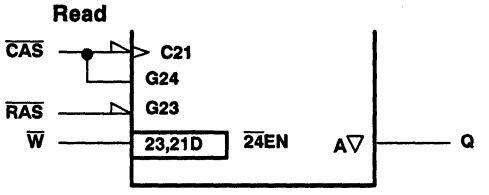
$\overline{CAS}$ is ANDed with $\overline{RAS}$ (through G24) so when $\overline{RAS}$ and $\overline{CAS}$ are both high, the device is powered down.

Write



By virtue of the AND relationship between $\overline{CAS}$ and $\overline{W}$ (explicitly shown), when either one of these inputs goes low with the other one and $\overline{RAS}$ is already low ($\overline{RAS}$ is ANDed by G23), the D input is momentarily enabled (through C22). In an "early-write" cycle it is $\overline{W}$ that goes low first; this causes the output to remain off as explained below.

Read



The ANDed result of $\overline{RAS}$ and $\overline{W}$ (produced by G23) is clocked into a latch (through C21) at the instant $\overline{CAS}$ goes low. This result will be "1" if $\overline{RAS}$ is low and $\overline{W}$ is high. The complement of $\overline{CAS}$ is shown to be ANDed with the output of the latch (by G24 and 24). Therefore, as long as $\overline{CAS}$ stays low, the output is enabled. In the "early-write" cycle referred to above, a "0" was stored in the latch by $\overline{W}$ being low when $\overline{CAS}$ went low, so the output remained disabled.

IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, New York 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, New York 10018

MOS MEMORY QUALITY AND RELIABILITY STRATEGY

Texas Instruments is committed to providing its customers with reliable, high quality memory products. MOS Memory management has applied a four-point quality and reliability strategy to:

- Provide customers with the lowest cost of product ownership through quality, reliability, and service by:
  - On-time delivery to minimize customer inventory.
  - Quality performance that justifies ship-to-stock certification and eliminates the cost of component testing.
  - No system manufacturing fallout.
  - No warranty and service costs.
- Develop partnership relationships to service and solve customer problems and anticipate upcoming needs.
- Live the quality improvement process from product creation and manufacturing through product sales via our total quality control approach of:
  - Quality Function Deployment.
  - Design-in and build-in quality and reliability.
  - In-control manufacturing.
  - Leadership customer service.
- Measure TI's performance by the customer's measurement and perception. The performance standard is continuous customer satisfaction.

Total Quality Control (TQC)

Total Quality Control (TQC) at TI is a business management process encompassing all company functions. The goal of TQC is continuous customer satisfaction. Utilizing a process of improvement through a positive feedback cycle, TQC is deployed in the MOS Memory Division from the initial design-in Q&R stage, in-control manufacturing, and customer service (see Figure 1).

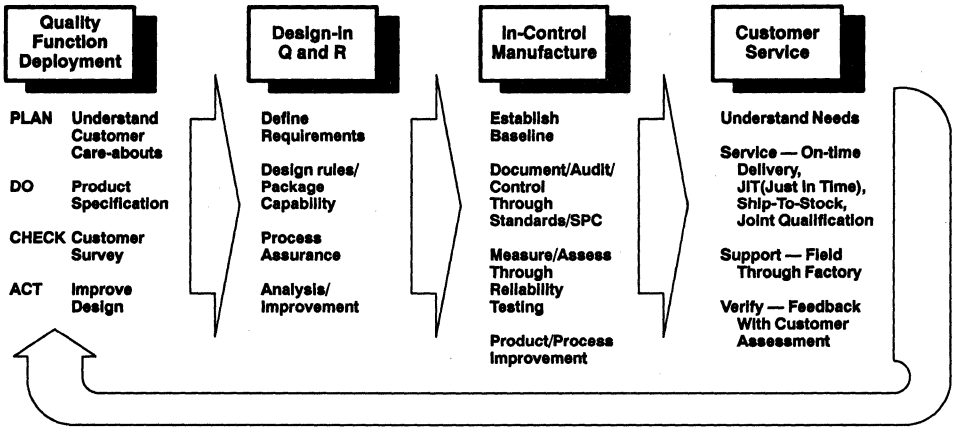


Figure 1. Total Quality Control

Total Quality Control (TQC) (Continued)

Proper application of the concept of "PLAN-DO-CHECK-ACT" allows a positive feedback loop that creates continuous improvement and breakthrough, as opposed to the "FIX-FIX-FIX-FIX" results of a negative loop (see Figure 2).

Quality Function Deployment

Continuous customer satisfaction can be achieved only by fully understanding customer needs, then introducing innovative products that satisfy those needs. Quality Function Deployment (QFD) accomplishes both purposes at TI. QFD is a technique that systematically records the voice of the customer, identifying product and service attributes most important to the customer. QFD then blends these needs with the talents and innovations of a TI design team to define a manufacturable, reliable product solution for the customer.

Design-In Quality and Reliability

Quality and reliability improvements at TI start with the chip and package design. The objective of MOS Memory's Design-In Quality and Reliability (DIR) thrust is *first-pass qualification of new products, internally and at the customer.* The TI approach to DIR has been to understand customer requirements of a product, and to formalize this knowledge into a database that incorporates both reliability modeling knowledge, and "lessons learned" from historical problems and engineering evaluations. Before any new design is approved, the design is verified against a DIR "checklist". Design verification is planned to evolve to computer verification utilizing artificial intelligence.

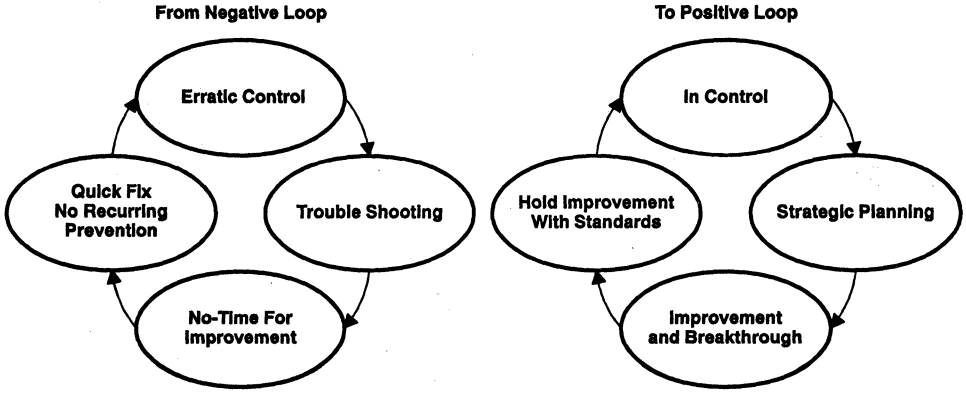


Figure 2. TQC Philosophy

In-Control Manufacturing

Documentation/Audit System

To assure in-control manufacturing, TI employs a hierarchical specification system. General specifications on all aspects of quality, reliability, and customer service are written and controlled by the central Quality and Reliability group. More detailed specifications control the operating practices of design, manufacturing, marketing, and other support organizations. These specifications follow guidelines set by the higher-level specifications, but concentrate on the type of business entity.

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In-Control Manufacturing (continued)

Regularly scheduled audits are performed within TI to ensure compliance with all specifications. The five types of audits performed are:

1. Self audit: An internal audit within each functional operation. This type of audit is conducted by persons within the operation and an additional person from outside the operation.
2. Cross-audit: An audit by persons independent of the operation being audited.
3. Group audit: An audit of an operation conducted by the Semiconductor Group audits and procedures function, which is a part of the central Quality and Reliability organization.
4. Procedures audit: An audit of lower-level specifications with respect to higher-level specifications.
5. Compliance audit: An audit of operating practices with respect to specifications.

Statistical Process Control (SPC)

Quality improvement is achieved through Statistical Process Control (SPC). SPC is applied throughout the manufacturing operations of the MOS Memory division. The objectives of SPC are:

– Control processes on a realtime basis.

– Improve process capability (CP).

– Reduce variability to target value (CPK).

– Eliminate "out-of-spec" lots.

– Achieve dependable delivery.

– Lower cost-of-quality.

Computer hardware and artificial intelligence software have been coupled to establish interactive control allowing the computer to generate realtime control charts and prompt adjustments to equipment and processes (see Figure 3).

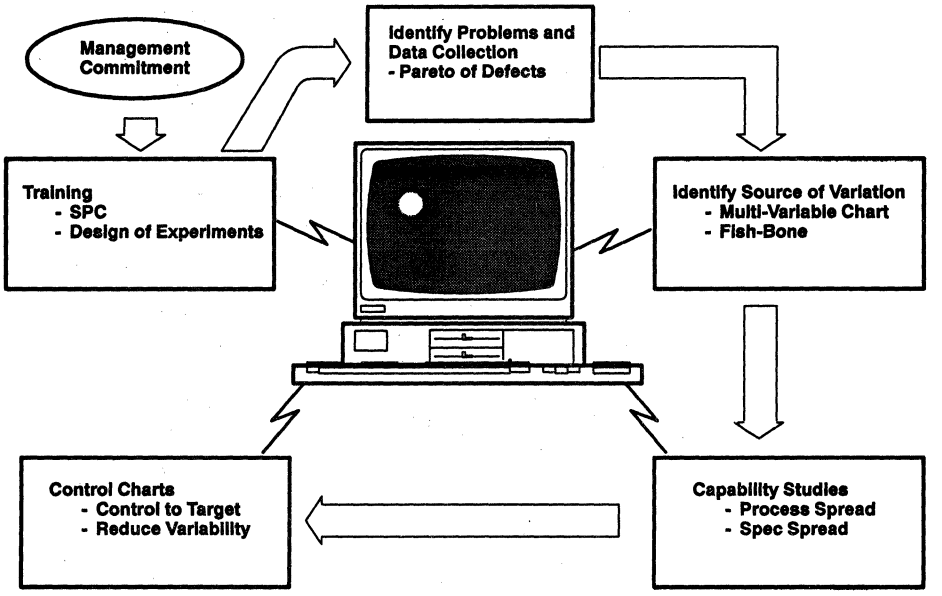

Figure 3. Computer-Aided Statistical Process Control

Die Fabrication Control

In addition to extensive SPC applications in our MOS fabrication centers, TI implements wafer-level quality and reliability controls.

Wafer-level quality control focuses on reduction of variability around target values (CPK) for key functionality parameters and controls the processes that affect these parameters. For example: Column access time (t_{CAC}) is a key DRAM parameter. One of the die manufacturing processes that affects t_{CAC} is the photo etch. To reduce variability of the target value of t_{CAC}, polysilicon-width dimension is controlled at the photo etch process.

Wafer-level reliability controls address process control of known reliability hazards. For example: Excessive phosphorus use in die processing can lead to corrosion defects in the finished device. Wafer-level reliability controls require that phosphorus level control be built into the manufacturing process and that action be prescribed for out-of-control material. Other wafer-level reliability controls are shown in the following table.

Table 1. Wafer Reliability Controls

PARAMETER	CONTROL
Metal	Electromigration Testing, Grain Size, Silicon Nodule Monitor Step Coverage/Metal Necking Monitor Stress-Induced Metal Void Testing
Protective Overcoat	P.O. Integrity Stress Testing Thickness Monitor Refraction
Corrosion	% Phosphorus In Multilevel Oxide Monitor
Gate Oxide Integrity	Breakdown Voltage

Device Assembly Control

TI has also implemented assembly level reliability controls and SPC at critical assembly points (see Table 2) to ensure highly reliable device packaging. Each parameter has certain controls performed at appropriate frequencies to ensure that assembly processing is at qualified levels. Controls may be added or reduced after extensive testing has been performed. Results are carefully studied and fed back to preclude reliability problem introduction into the assembly process. Some of the parameters and controls are shown in Table 3.

Table 2. Major Assembly Steps Using SPC/SQC†

PLASTIC DEVICE ASSEMBLY	
Process	**Control Parameter**
Mount	% Coverage of Epoxy
Bond	Bond Strength
Mold	Temperature and Molding Parameters
Trim/Form	Lead Deflection (DIP)
CERAMIC DEVICE ASSEMBLY	
Bond	Bond Strength
Seal	Seal Furnace Temperature

†Statistical Process Control/Statistical Quality Control

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Table 3. MOS Memory Assembly Level Reliability Controls

PARAMETER	CONTROL
P.O. Integrity	Contactless Wafer Mount on Tape Die Mount System Mold Compound Parameters
Chip/Crack	Visual Inspection Temp Cycle Saw Blade Conditions Poker Pin Height Wet Etch Monitor (EPROM)
Bond Integrity	Bond Strength Monitor Bond Parameters Bake/Bond Pull Monitor Capillary Change
Package Integrity	Visual Inspection Mold Press Parameters (Plastic) X-Ray Inspection (Plastic) Trim/Form (Plastic) Package Seal (Ceramic) Temp Cycle (Ceramic) Hermeticity Monitor (Ceramic)
Die Mount Integrity	Die-Shear Monitor Centrifuge Monitor X-Ray Inspect Leadframe Polyimide Pattern Inspect Pick-Up Arm Force
Contamination	Visual Inspection

Product Assessment/Improvement

Reliability Control System

The MOS Memory reliability control system (Figure 4) provides closed-loop-system feedback resulting in corrective actions and ongoing product improvements. Each new product, process, or major change to an existing product is internally qualified to industry leadership standards prior to production. This is followed by intensive monitoring during production ramp-up and reliability monitoring each month, once a product achieves final production release.

Reliability Development Issues

Soft Error: TI does extensive work in all phases of device development to minimize the effects of soft errors. Soft errors are caused by alpha particles emitted by the decay of small amounts of thorium and uranium located in device packaging materials. TI maintains an aggressive program of evaluating new mold compounds to ensure low alpha emmissivity. Certain device design and processing techniques are also applied to ensure a low soft-error rate. The goal of device design and processing is to maximize the cell capacitance by employing an oxide-nitride dielectric, as opposed to an oxide dielectric. Also, the cell capacitance increases as the dielectric thickness decreases. Testing has shown that the trench capacitor used in dynamic RAMs has competitive soft-error rates.

Channel Hot Electron: Channel hot electrons are caused by impact ionization in the drain pinch-off region. Electrons are accelerated toward the drain, collide with positive ions, and can be trapped in the gate oxide. This trapped charge can change the characteristics of the transistor by raising the V_T (threshold voltage). One method employed to reduce the effects of hot electrons is to add a lightly doped drain to reduce the electric field at the gate. Testing for channel hot electrons is performed at a low temperature (–10°C) and a high drain voltage.

Latch-up: A CMOS device can latch-up when the gain of the parasitic PNP+NPN transistors is greater than 1. These PNP+NPN transistors act as a silicon controlled rectifier (SCR). If enough current flows through the resistors, the transistors will turn on and the device will latch-up.

To control latch-up, the SCR gain must be controlled to less than or equal to one. Methods for improving latch-up immunity include incorporating guard rings between P+ and N+ diffusions, and isolating P+ and N+ diffusions.

Latch-up testing is performed to ensure our CMOS devices meet the minimum holding current for industry standards.

Customer Service

Quality, Reliability, Service, and the Cost of Ownership

The goal of Texas Instruments is to offer the best quality, reliability, and service in the semiconductor industry. The foundation for this approach is to ship consistent quality. Consistent quality allows ship-to-stock programs that foster the elimination of the customer's incoming inspection. Ship-to-stock quality, coupled with 100% on-time delivery to narrow shipping windows means support of the customer's just-in-time manufacturing program. This combination of quality, reliability, and service can be measured by a single index called "the cost of ownership". The "cost of ownership" is defined as being composed of the purchase price, quality adders (for incoming inspection and board rework), inventory adders (for maintenance of a buffer inventory for suppliers who cannot meet just-in-time delivery), in-house reliability adders (for system burn-in and rework), and field reliability adders (for warranty and post-warranty field repairs).

For more information about the cost-of-ownership concept, contact your local TI sales office and request the brochure "Texas Instruments Lowers Semiconductor Cost of Ownership", SSYB057.

Quality Improvement

Significant improvement in product quality has been achieved through:

– Better definition of customer's requirements.

– Greater emphasis on quality as a design criterion.

– Improved control of incoming materials.

– Intensive training of supervisors and operators.

– Extensive use of statistical process control.

– More automation of operations to minimize operator-related defects.

QUALIFICATION	PRODUCTION RAMP LOT ACCEPT	FINAL PRODUCTION RELEASE
Baseline process 3 – 6 diffusion lots Worst case customer qualification requirements TESTS	Baseline process Reliability lot acceptance concurrent with qualifications Review of data once sufficient lots have been sampled TESTS	Control each package/wafer fabrication site/device combination Ongoing reliability monitor of 125°C op life, data retention bake, temperature cycle, 85/85, autoclave, package integrity, and internal cavity moisture Control limits for each test based on product capability Early failure rate monitor
125°C Op life EFR† 85/85 Temperature cycle Pressure cooker test PSP/PVP‡ Static bias/storage Soft error Data retention bake Electromigration Package integrity ESD	Early Failure Rate† High temperature reverse bias§ Temperature cycle Pressure cooker test Bake 85/85§	

† DRAM – 125°C OPL, 80 hours
EPROM & OTP – 200°C bake, 44 hours (OTP in ceramic package)
‡ PSP: Pressure cooker, Solder dip, Pressure cooker
PVP: Pressure cooker, Vapor phase, Pressure cooker
§ Non–Volatile only

Figure 4. Reliability Control System

As is demonstrated in Figure 5, MOS Memory EPROM and DRAM outgoing quality has dramatically improved during the last few years. This significant improvement has occurred for all TI product lines and has been recognized publicly by many of our customers, who have given TI more than 70 major quality awards in the last several years. Included among these awards are Ford's Q-1 and TQE Awards, the U.S. Naval Quality Award, and the Deming Prize, which is Japan's most prestigious quality award.

Reliability Improvement

Low IC failure rates are achieved through design-in reliability, computer aided design, stringent qualification testing prior to product release, routine monitoring of released products, and an extensive failure mode tracking and feedback system for IC failures.

Each generation of MOS Memory products has exhibited a device failure rate improvement trend, and each new generation shows a step function improvement in quality and reliability over the previous generation (see Figures 5 and 6). Even though the memory device complexity increases in an ongoing manner, TI's failure rate by function has improved at an even faster pace. TI continues to emphasize reliability improvement as a major factor in reducing the total cost of ownership for our customers. Reliability improvement is reflected as a reduction in the expected field failures during system lifetime.

Up-to-date quality and reliability data for MOS Memory products is available. Please contact your local TI sales office for information.

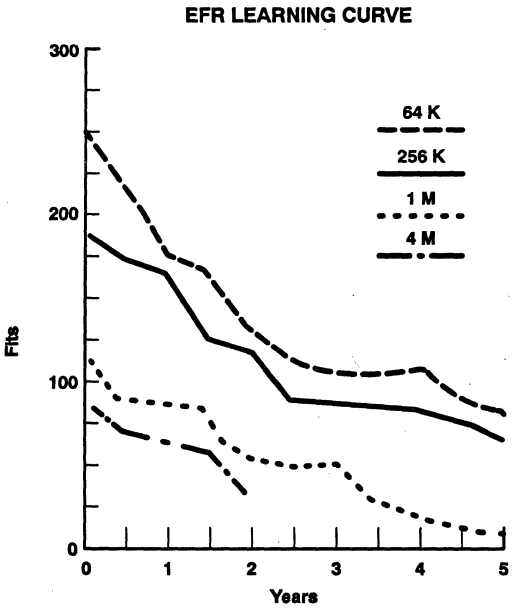

Figure 5. MOS Memory Quality Improvement

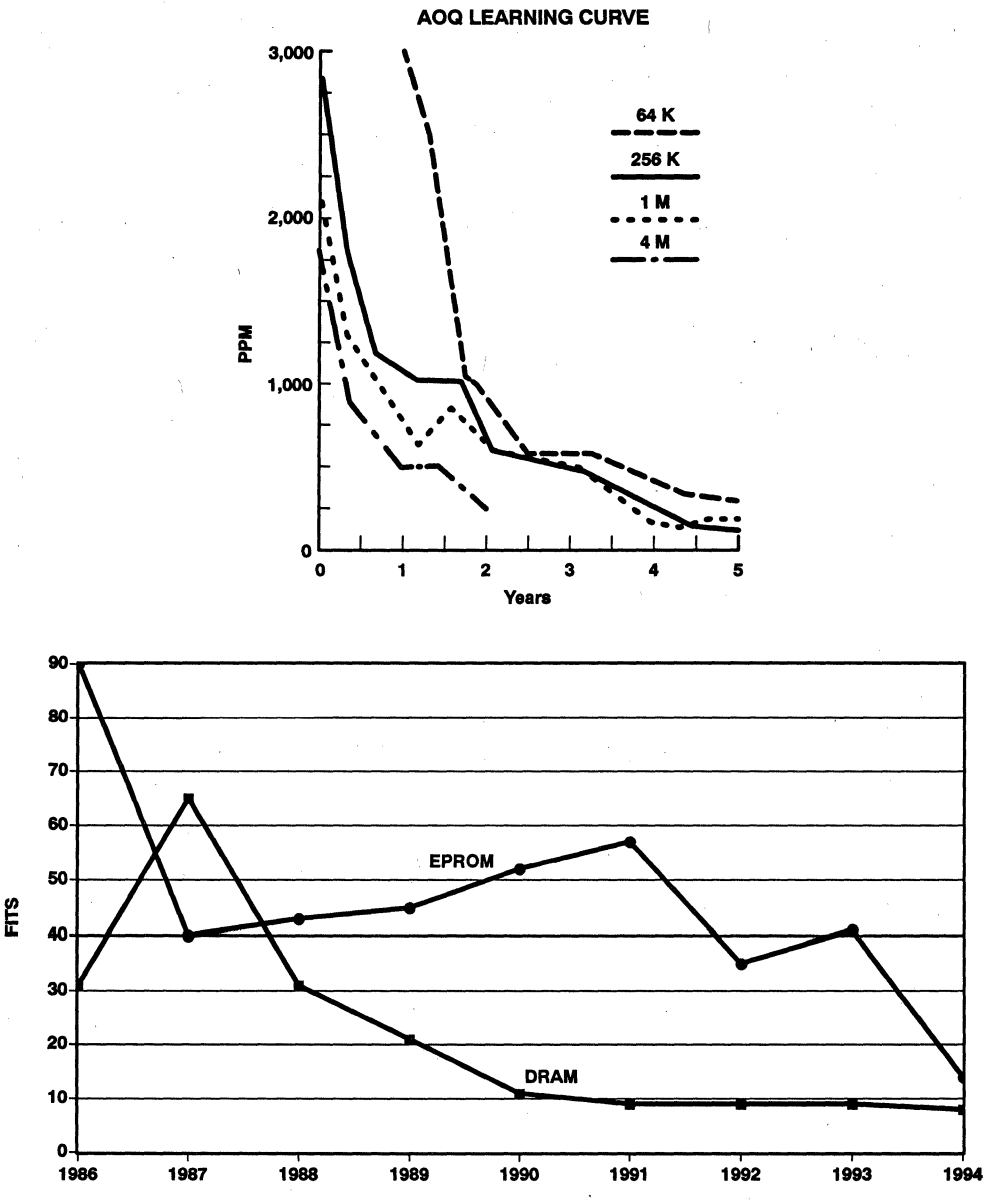

Figure 6. MOS Memory Reliability Improvement

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Scope

This guideline establishes the requirements for methods and materials used to protect electronic parts, devices, and assemblies (items) that are susceptible to damage or degradation from electrostatic discharge (ESD). The electrostatic charges referred to in this specification are generated and stored on surfaces of ordinary plastics, most common textile garments, ungrounded person's bodies, and many other commonly unnoticed static generators. The passage of these charges through an electrostatic-sensitive part may result in catastrophic failure or performance degradation of the part.

The part types for which these requirements are applicable include, but are not limited to the following:

1. All metal-oxide semiconductor (MOS) devices; e.g., CMOS, PMOS, etc.
2. Junction field-effect transistors (JFET)
3. Bipolar digital and linear circuits
4. Op-amps, monolithic microcircuits with MOS compensating networks, on-board MOS capacitors, or other MOS elements
5. Hybrid microcircuits and assemblies containing any of the types of devices listed
6. Printed circuit boards and other types of assembly containing static-sensitive devices
7. Thin-film passive devices

Definitions

1. Electrostatic Discharge (ESD): A transfer of electrostatic charges between bodies at different electrostatic potentials caused by direct contact or electrostatic field induction.
2. Conductive material: Material having a surface resistivity of 10^5 Ω/square maximum.
3. Static dissipative material: Material having a surface resistivity between 10^5 and 10^9 Ω/square.
4. Antistatic material: Material having a surface resistivity between 10^9 and 10^{14} Ω/square
5. Surface resistivity: An inverse measure of the conductivity of a material and is the resistance of unit length and unit width of a surface. Note: Surface resistivity of a material is numerically equal to the surface resistance between two electrodes forming opposite sides of a square. The size of the square is immaterial. Surface resistivity applies to both surface and volume conductive materials and has the dimension of Ω/square.
6. Volume resistivity: Also referred to as bulk resistivity, it is normally determined by measuring the resistance (R) of a square of material (surface resistivity) and multiplying this value by the thickness (T).
7. Ionizer: A blower that generates positive and negative ions, either by electrostatic means or from a radioactive energy source in an airstream and distributes a layer of low velocity ionized air over a work area to neutralize static charges.
8. Close proximity: For the purpose of this guideline, 6 inches or less.

Device Sensitivity per Test Circuit of Method 3015, MIL-STD-883C

1. Devices are categorized according to their susceptibility to damage resulting from electrostatic discharges (ESD).

Category	ESD Sensitivity
Class 1	0 V – 1999 V
Class 2	2000 V – 3999 V
Class 3	4000 V and above

2. Devices are to be protected from ESD damage from receipt at incoming inspection through assembly, test, and shipment of completed equipment.

Applicable Reference Documents

The following reference documents (of latest issue) can provide additional information on ESD controls.

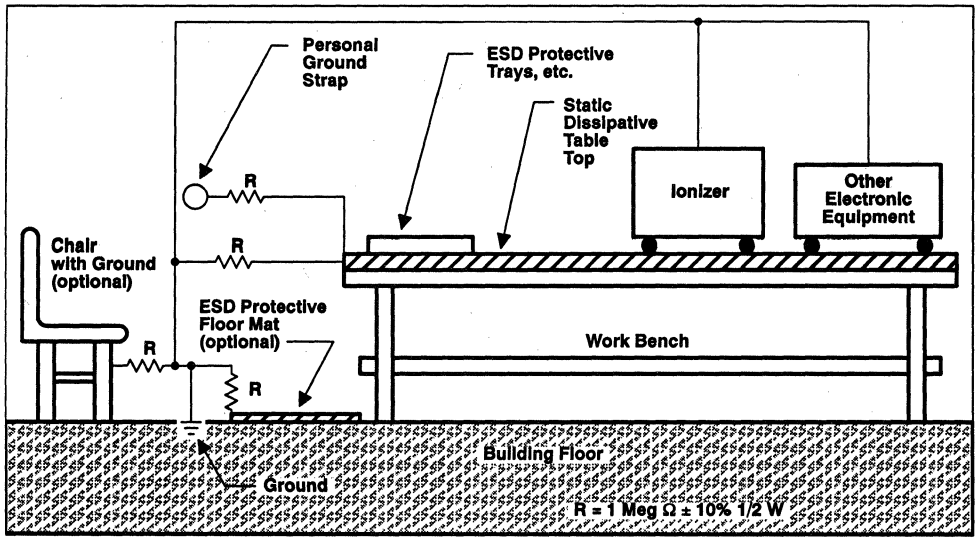
1. MIL-M-38510 Microcircuits, General Specification
2. MIL-STD-883 Test Methods and Procedures for Microelectronics
3. MIL-STD-19491 Semiconductor Devices, Packaging of
4. MIL-M-55565 Microcircuits, Packaging of
5. DOD-HDBK-263 Electrostatic Discharge Control Handbook for Protection
6. DOD-STD-1686 Electrostatic Discharge Control Program
7. NAVSEA SE 003-11-TRN-010 Electrostatic Discharge Training Manual
8. JEDEC Standard Publication 108

Facilities for Static-Free Workstation

The minimum acceptable static-free workstation shall consist of a work surface covered with static dissipative material attached to ground through a 1 MΩ ± 10% resistor, an attached grounding wrist strap with integral 1 MΩ ± 10% resistor for each operator, and air ionizer(s) of sufficient capacity for each operator. The wrist strap shall be connected to the static dissipative material. Ground shall utilize the standard building earth ground; refer to Figure 1. Conductive floor tile/carpet along with conductive shoes may be used in lieu of the conductive wrist straps for non-seated personnel. The Site Safety Engineer must review and approve all electrical connections at the static-free workstation prior to its implementation.

Air ionizers shall be positioned so that the devices at the static-free workstations are within a 4-foot arc measured by a vertical line from the face of the ionizer and 45 degrees on each side of this line.

General grounding requirements are to be in accordance with Table 1.



All electrical equipment sitting on the conductive table top must be hard grounded but must be isolated from the static dissipative work surface.
NOTE A: Earth ground is not computer ground or RF ground or any other limited-type ground.

Figure 1. Static-Free Workstation

Table 1. General Grounding Requirements

	Treated With Antistatic Solution or Made of Conductive Material	Grounded to Common Point	Static Dissipative Material
Handling Equipment/ Handtools	X		X
Metal Parts of Fixtures and Tools/Storage Racks		X	
Handling Trays/Tubes	X		X
Soldering Irons/Baths		X	
Table Tops/Floor Mats	X	X	X
Personnel		X Using Wrist Strap*	

* With 1 MΩ ± 10% resistor

Usage of Antistatic Solution in Areas to Control the Generation of Static Charges

The use of antistatic chemicals (antistats) should be a supplemental part of an overall organized ESD program. Any antistatic chemical application shall be considered as a means to reduce or eliminate static charge generation on nonconductive materials in the manufacturing or storage areas.

The application of any antistatic chemical in a clean room of class 10 000 or less shall not be permitted. Accordingly, any user of antistatic solutions must consider the following precautions:

1. Do not apply antistatic spray or solutions in any form to energized electrical parts, assemblies, panels, or equipment.
2. Do not perform antistatic chemical applications in any area when bare chips, raw parts, packages, and/or personnel are exposed to spray mists and evaporation vapors.

The need for initial application and frequency of reapplication can be established only through routing electrostatic voltage measurements using an electrostatic voltmeter. The following durability schedule is a reasonable expectation.

1. Soft surfaces (carpet, fabric seats, foam padding, etc.): each 6 months or after cleaning, by spraying.
2. Hard abused surfaces (floor, table tops, tools, etc.): each week (or day for heavy use) and after cleaning, by wiping or mopping.
3. Hard unabused surfaces (cabinets, walls, fixtures, etc.): each 6 months or annually and after cleaning, by wiping or spraying.
4. Company-furnished and maintained clothing and smocks: after each cleaning, by spraying or adding antistatic concentrate to final rinse water when cleaned.

The use of antistatic chemicals, their application, and compliance with all appropriate specifications, precautions, and requirements shall be the responsibility of the area supervisor where antistatic chemicals are used.

ESD Labels and Signs in Work Areas

ESD caution signs at workstations and labels on static-sensitive parts and containers shall be consistent in color, symbols class, voltage sensitivity identification, and appropriate instructions. Signs shall be posted at all workstations performing operations with static-sensitive items. These signs shall contain the following information or its equivalent.

CAUTION

STATIC CAN DAMAGE COMPONENTS

Do not handle ESD-sensitive items unless grounding wrist strap is properly worn and grounded. Do not let clothing or plain plastic materials contact or come in close proximity to ESD-sensitive items.

Labels shall be affixed to all containers containing static-sensitive items at a place readily visible and proper for the intended purpose. Additionally, labels must be consistently placed on containers and packages at a standard location to eliminate mishandling. Use only QC-accepted and approved signs and labels to identify static-sensitive products and work areas. The use of ESD signs and labels and their information content shall be the responsibility of the area supervisor to assure consistency and compatibility throughout the static-sensitive routing.

Relative Humidity Control

Since relative humidity has a significant impact on the generation of static electricity, when possible, the work area should be maintained within the 40%–60% relative humidity range.

Preparation for Working at Static-Free Workstation

A workstation with a static disspative work surface connected to ground through a 1 MΩ ± 10% resistor, a grounding wrist strap with the ground wire connected to the conductive work surface, and an ionizer constitute a static-free workstation (Figure 1). An operator is properly grounded when the wrist strap is in snug (no slack) contact with the bare skin, usually positioned on the left wrist for a right-handed operator. The wrist strap must be worn the entire time an operator is at a static-free workstation. The operator should first touch the grounded bench top before handling static-sensitive items. This precaution should be observed in addition to wearing the gounding wrist strap. If possible, the operator should avoid touching leads or contacts even though he or she is grounded.

CAUTION

Personnel shall never be attached without the presence of the 1 MΩ ± 10% series resistor in the ground wire.

An operator's clothing should never make contact or come in close proximity with static sensitive items. Operators must be especially careful to prevent any static-sensitive items (being handled) from touching their clothing. Long sleeves must be rolled up or covered with antistatic sleeve protector banded to the bare wrist, which shall "cage" the sleeve at least as far up as the elbow. Only antistatic finger cots may be used when handling static-sensitive items.

Any improperly prepared person, while at or near the work station, shall not touch or come in close proximity with any static-sensitive item. It is the responsibility of the operator and the area supervisor to ensure that the static-free work area is clear of unnecessary static hazards, including such personal items as plastic coated cups or wrappers, plastic cosmetic bottles or boxes, combs, tissue boxes, cigarette packages, and vinyl or plastic purses. All work-related items, including information sheets, fluid containers, tools, and part carriers must be approved for use at the static-free workstation.

General Handling Procedures and Requirements

1. All static-sensitive items must be received in an antistatic/conductive container and must not be removed from the container except at the static-free workstation. All protective folders or envelopes holding documentation (lot travelers, etc.) shall be made of nonstatic-generating material.
2. Each packing (outermost) container and package (internal or intermediate) shall have a bright yellow warning label attached, stating the following information or equivalent:

The warning label shall be legible and easily readable to normal vision at a distance of three feet.

3. Static-sensitive items are to remain in their protective containers except when actually in use at the static-free station.
4. Before removing the items from their protective container, the operator should place the container on the conductive grounded bench top and make sure the wrist strap fits snugly around the wrist and is properly plugged into the ground receptacle, then touch hands to the conductive bench top.
5. All operations on the items should be performed with the items in contact with the grounded bench top as much as possible. Do not allow conductive magazine to touch hard-grounded test gear on bench top.
6. Ordinary plastic solder-suckers and other plastic assembly aids shall not be used.
7. In cases where it is impossible or impractical to ground the operator with a wrist strap, a conductive shoe strap may be used along with conductive tile/mats.
8. When the operator moves from any other place to the static-free station, the start-up procedure shall be the same as in Preparation for Working at Static-Free Workstation.
9. The ionizer shall be in operation prior to presenting any static-sensitive items to the static-free station, and shall be in operation during the entire time period the items are at the station.
10. "Plastic snow" polystyrene foam, "peanuts," or other high-dielectric materials shall never come in contact with or be used around electrostatic sensitive items, unless they have been treated with an antistat (as evidenced by pink color and generation of less than ± 100 volts).
11. Static-sensitive items shall not be transported or stored in trays, tote boxes, vials, or similar containers made of untreated plastic material unless items are protectively packaged in conductive material.

Packaging Requirements

Packaging of static-sensitive items is to be in accordance with Device Sensitivity, item 1. The use of tape and plain plastic bags is prohibited. All outer and inner containers are to be marked as outlined in General Handling Procedures and Requirements, item 2. Conductive magazines/boxes may be used in lieu of conductive bags.

Specific Handling Procedures for Static-Sensitive Items

Stockroom Operations

1. Containers of static-sensitive items are not to be accepted into stock unless adequately identified as containing static-sensitive items.
2. Items may be removed from the protective container (magazine/bag, etc.) for the purpose of subdividing for order issue only by a properly grounded operator at an approved static-free station as defined in Facilities for and Preparation for Working at Static-Free Workstation.
3. All subdivided lots must be carefully repackaged in protective containers (magazine/bag, etc.) prior to removal from the static-free work-station and labeled to indicate that the package(s) contain static-sensitive items. If it is suspected that a static-sensitive item is not adequately protected, do not transfer it to another container; return it to the originator for disposition unless the originator is a customer. In that case, the QC engineer should contact the customer and negotiate an appropriate disposition.
4. It is the responsibility of the stockroom supervisor to ensure that all personnel assigned to this operation are familiar with handling procedures as outlined in this specification. A copy of this specification is to be posted in the vicinity so that it is accessible to the operators. Stock handlers and all others who might have occasion to move stock are to be instructed to avoid direct contact with unprotected static-sensitive items.

Module and Subassembly Operations

1. Static-sensitive items are not to be received from a stockroom, kitting, or machine insertion area unless received in approved static-protective packaging and properly labeled to indicate that the contents are static-sensitive.
2. All single station, progressive line manual assembly operators, and visual inspectors prior to wave soldering operations are to be properly grounded with a grounding wrist strap when handling static-sensitive items.
3. Progressive lines used as single stations where operators will be working on a mix of boards, both static-sensitive and nonstatic-sensitive, will require that all operators working on the line be properly grounded. This is necessary to accommodate the sliding of static-sensitive boards along the assembly bench or across positions not engaged in the assembly of this type board.
4. It is the responsibility of the area supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in the proper working order and to ensure that operators are wearing grounding wrist straps properly (snugly in contact with bare skin).

Soldering and Lead-Forming Operations

1. All soldering machines, conveyors, cleaning machines, and equipment shall be electrically grounded to ensure that they are at the same ground potential as the grounded operators working on their stations. No machine surfaces exposed to static-sensitive items are to be above ground potential.
2. All processing equipment shall be grounded, including all loading and unloading stations, that is, the stations before and after each piece of processing equipment.
3. All nonmetallic, static-generating components in the handling systems shall be treated to ensure protection from static.
4. All stations shall be identified by posting signs as outlined in ESD Labels and Signs in Work Areas.
5. Operators are to be properly grounded with a grounding wrist strap during handling, loading, unloading, inspection, rework, or proximity to static-sensitive items.
6. Unloading-operators working at a grounded station shall place static-sensitive items into approved static-protective bags or containers.

Soldering and Lead-Forming Operations (Continued)

7. All manual soldering, repair, and touch-up work stations on the solder line are to be static protected. Operators are to wear grounding wrist straps when working on static-senstive items. Only grounded-tip soldering/desoldering irons are allowed when working on static-sensitive items.
8. It is the responsibility of the area supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that the operators are wearing grounding wrist straps properly (comfortably snug in contact with bare skin).

Electrical Testing Operations

1. All electrical test stations shall be static protected. Operators shall be properly grounded when working on these items.
2. Reused antistatic magazines must be monitored for maintenance of antistatic characteristics.
3. Devices should be in an antistatic/conductive environment except at the moment when actually under test.
4. Devices should not be inserted into or removed from circuits or tester with the power on or with signals applied to inputs to prevent transient voltages from causing permanent damage.
5. All unused input leads should be biased if possible.
6. Device or module repairs must be performed at static-free stations with the operator attached to a grounding wrist strap. Grounded-tip soldering irons shall be used when working on static-sensitive items.
7. Static-sensitive items shall be handled through all electrical inspections in static protective containers. Removal of the items from the protective containers shall be done at a static-free workstation as discussed in Preparation for Working at a Static-Free Workstation. The units must be returned to the containers before leaving the station.
8. All such items shall be shipped with an ESD warning label affixed as listed.
9. It is the responsibility of the area supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

Packing Operations

1. Static-sensitive items are not to be accepted into the packing area unless they are contained in a static-protected bag or conductive container.
2. A static-sensitive item delivered to the packer within an approved container or bag and found to be in order regarding identification shall be packed in the standard shipping carton or other regular packaging material. Containers are to be labeled in accordance with General Handling Procedures and Requirements, item 2.
3. Any void-fillers shall be made of an approved antistatic material.

Burn-In Operations

1. Burn-in board loading and unloading of static-sensitive items shall be done at a static-free station.
2. Shorting clips/shorted connectors shall be installed on the board plug-in tab prior to loading any units into the board sockets. The clip/connectors shall be taken off just prior to plugging the board into the oven connector. The clip/connector shall be installed immediately upon removal of the board from the oven connector. Installation and removal of the clip/connector shall be done by a properly grounded operator.
3. All automatic or semi-automatic loading and unloading equipment shall be properly electrically grounded.

Burn-In Operations (continued)

4. It is the responsibility of the area supervisor to ensure that all personnel handling static-senstive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

Customer-Returned-Item Handling Procedure

Receipt of ESD sensitive-labeled items is to be done at a static-free workstation and handled in accordance with applicable sections within this guideline.

Quality Control Provision

Sampling

Each manufacturing, stockroom, and testing operation handling ESD sensitive devices will be audited a minimum of once each quarter for compliance with all terms of this specification by the responsible process control or QRA organization. Ground continuity and the presence of uncontrolled static voltages are considered critical and shall be checked more frequently as specified below.

Ground Continuity (minimum of once a week)

Ground connections (grounding wrist strap, ground wires on cords, etc.) shall be checked for electrical continuity. The presence of a 1 MΩ ± 10% resistor in the ground connections between both the operator wrist straps to the work surface and the work surface to ground connector must be verified.

Grounded Conditions (minimum of once a week)

A visual inspection shall be made to determine full compliance with this specification at static-free workstations during handling of static-sensitive items, including operator being grounded as required, static-sensitive items not being handled in unprotected or unauthorized areas, and no static-generating materials at the grounded workstation.

Sleeve Protectors (minimum of once a week)

A visual check shall be made to determine that each operator wearing loose-fitting or long-sleeved clothing either has sleeves properly rolled or covered with sleeve protectors properly grounded to the bare skin at the wrist.

Static Voltage Levels (minimum of once a week)

In addition to the visual inspections, a sample inspection using an electrostatic voltmeter will be used to check for uncontrolled electstatic voltages at or near electrostatic-controlled work stations.

Conductive Floor Tiles (minimum of once a month)

Conductive floors must have a resistance of not less than 100 kΩ from any point on the tile to earth ground. Also, resistance from any point-to-point on the tile floor three (3) feet apart shall be not less than100 kΩ. The test methods to be used are ASTM-F-150-72 and NFPA 99.

Records

Written records must be kept of all these QC audits.

Training

Training is applicable for all areas where individuals come in contact with ESD-sensitive devices. It is the responsibility of each area supervisor to make sure that his/her people receive ESD training initially and every 12 months thereafter to maintain proficiency. Training should include static fundamentals, a review of applicable parts of this specification, and actual applications in the work area.

NOTES

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