TEXAS INSTRUMENTS

MOS Memory

Commercial and Military Specifications

Data Book

1989

MOS Memory Data Book

Commercial and Military Specifications

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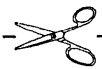

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INTRODUCTION

The 1988 MOS Memory Data Book from Texas Instruments includes complete detailed specifications on the expanding MOS Memory product line including Dynamic Random-Access Memories (DRAMs), Single-In-Line Package DRAM Memory Modules (SIPs), Video Random-Access Memories (VRAMs), First-In First-Out Pseudo Static Memories (FRAMs), Erasable Programmable Read-Only Memories (EPROMs), and MOS one-time Programmable Read-Only Memories (PROMs). Also included are military specifications for DRAMs, VRAMs, EPROMs, and Static Random-Access Memories (SRAMs). This is TI's first MOS Memory data book to include specifications for the VLSI Memory Management products.

The data book is divided into 13 sections. Section 1, General Information, includes the table of contents, an alphanumeric index for quickly finding device numbers, a part number guide with ordering information, plus device selection guides, product reference guides, and an IC Line-up chart for a quick overview of the broad TI MOS Memory product line. Page numbers are included on the product selection guides for easy access to the detailed specifications. In Section 2, an Alternate Source Directory lists alternate vendor part numbering examples in addition to alternate sources to TI devices (based on published data). Product specifications for over 100 devices can be found in Sections 4 through 8.

Recently published technical articles and product applications information can be found in Section 9. For the first time, a section on Quality and Reliability (Section 10) has been included in the TI MOS Memory data book. Because all MOS Memory devices are ESD sensitive, handling guidelines are included in Section 13.

The data sheets within each section are in alphanumeric order; Product Preview information is included at the end of the section. Data sheets listed with a "TMX" prefix and Product Preview disclaimer include target specifications for products that are currently under development at TI. The inclusion of these specifications does not imply that these products are or will be in production, or will meet these parameters.

Additional and/or updated information on these products is available from:

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DRAM/FRAM/SRAM ORDERING INFORMATION

Factory orders for DRAM/FRAM/SRAMs described in this book should include an eight-part type number as explained in the following example:

TMS 4 4 C 256 -10 DJ -

1. Prefix:

   TMS Commercial MOS
   SMJ Military MOS
   TMX Pre-production Commercial MOS

2) Product Family:

   4 DRAM/FRAM
   6 SRAM (Military Only)

3) Word Width:

   1 ×1
   Blank ×1 (256K and 1 Meg DRAMs Only)
   Blank ×4 (1 Meg FRAM Only)
   4 ×4
   8 ×8 (SRAMs Only)
   9 ×9 (SRAMs Only)

4) Technology:

   Blank NMOS
   C CMOS
   CE CMOS with Output Enable Control (SRAMs Only)
   CD CMOS with Separate I/O Pins (SRAMs Only)

5) Density:

   16 16K SRAM
   16 64K DRAM ('4416)
   64 64K DRAM ('4164)
   64 64K SRAM
   61 64K VRAM ('4161)
   72 72K SRAM
   64 256K DRAM ('4464)
   256 256K DRAM ('4256)
   257 256K DRAM ('4257)
   256 256K SRAM
   61 256K VRAM ('4461)
   288 288K SRAM
   256 1 Meg DRAM ('44C256)
   257 1 Meg DRAM ('44C257)
   1024 1 Meg DRAM ('4C1024)
   1025 1 Meg DRAM ('4C1025)
   1027 1 Meg DRAM ('4C1027)
   1050 1 Meg FRAM ('4C1050)
   251 1 Meg VRAM ('44C251)

6) Speed Designator:

DRAMs	FRAMs	SRAMs
-8 80 ns	-3 25 ns	-25 25 ns
-10 100 ns	-4 30 ns	-35 35 ns
-12 120 ns	-6 50 ns	-45 45 ns
-15 150 ns		-55 55 ns
-20 200 ns		

7) Package:

Commercial (Plastic)	Military (Ceramic)
DJ Small Outline J-lead (SOJ)	JD Dual In-line (DIP)
FM Leaded Chip Carrier (PLCC)	FG,FV Leadless Chip Carrier (CLCC)
SD Zig-zag In-line (ZIP)	HJ Small Outline J-lead (SOJ)
N Dual In-line (DIP)	

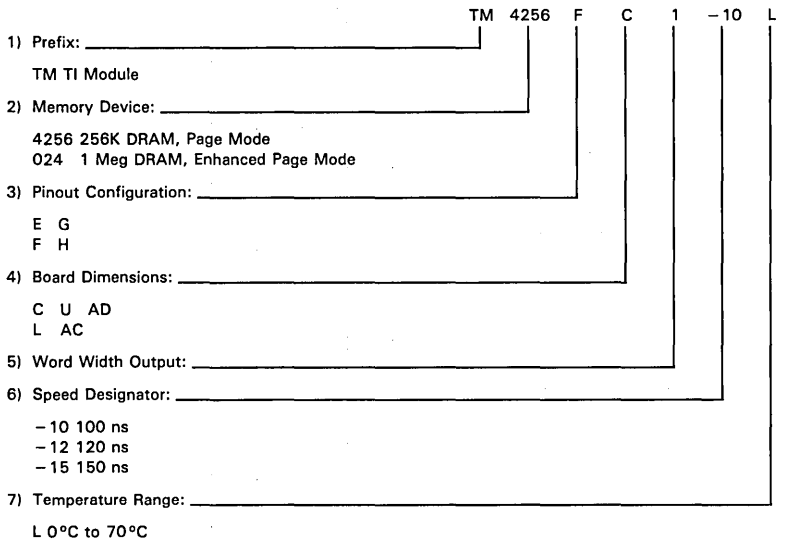
8) Temperature Range:

Commercial	Military
L 0°C to 70°C	M -55°C to 125°C
Blank 0°C to 70°C (1 Meg DRAM Only)	S -55°C to 100°C†

†Except SMJ4164 and SMJ4256, which are -55°C to 110°C.

DRAM MODULE ORDERING INFORMATION

Factory orders for DRAM modules described in this book should include a seven-part type number as explained in the following example:



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EPROM/PROM/EEPROM ORDERING INFORMATION

Factory orders for EPROMs/PROMs described in this book should include a nine-part type number as explained in the following example:

TMS 27 P C 512 -10 FM L 4

1. Prefix:

   TMS Commercial MOS
   SMJ Military MOS
   TMX Pre-production Commercial MOS

2) Product Family:

   27 EPROM/PROM
   28 EEPROM

3) Erasability:

   P Non-erasable
   Blank Erasable

4) Technology:

   C CMOS
   Blank NMOS

5) Density:

291	16K	128	128K
292	16K	256	256K
32	32K	512	512K
49	64K	010	1024K
64	64K	210	1024K

6) Speed Designator†:

35 ns	-3, -35
45 ns	Blank, -4, -45
50 ns	-5, -50
55 ns	-5, -55
100 ns	-10, -100
120 ns	-12, -120
150 ns	-1, -15, -150
170 ns	-1, -17, -170
200 ns	-2, -20, -200
250 ns	Blank, -25, -250
300 ns	-3, -30, -300
450 ns	-45

7) Package:

PROMs (Plastic)	EPROMs (Ceramic)	EEPROMs
N Dual In-line (DIP)	J Cerpak/Cerdip	J Ceramic DIP
FN Chip Carrier	JT 300-mil Cerdip (TMS27C49 Only)	N Plastic DIP
FM Chip Carrier		
NT 300-mil DIP (TMS27PC49 Only)		

8) Temperature Range:

Commercial	Military
E -40°C to 85°C	M -55°C to 125°C
L 0°C to 70°C	S -55°C to 100°C

9) 168 Hour Burn-in Option:

   4 168 Hour Burn-in
   Blank No Burn-in

†Please check individual data sheets for available speeds.

VLSI MEMORY MANAGEMENT ORDERING INFORMATION

Factory orders for VLSI Memory Management products described in this book should include a four-part type number as explained in the following example:

SN 74ACT2152 -25 JD

1) Prefix:

   SN Standard Prefix
   THCT Commercial CMOS
   TACT Commercial Advanced CMOS

2) Circuit Description:

   4 to 10 Characters

3) Speed Designator:

   -xx Speed in ns

4) Package:

   D, DW "Small Outline" Packages
   J, JD Ceramic DIPs
   N, NT Plastic DIPs
   FK Ceramic Chip Carrier
   FN Plastic Chip Carrier

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WORDS	BITS PER WORD				
	1	4	8	9	16
2K			(16K) EPROMs PROM TMS27C291 TMS27PC291 TMS27C292 SRAM SMJ68CE16		
4K		(16K) SRAM SMJ64C16	(32K) EPROMs PROM TMS2732A TMS27PC32 TMS27C32		
8K			(64K) EPROMs PROMs TMS2764 TMS27PC64 TMS27C64 TMS27PC49 TMS27C49 SRAM EEPROM SMJ68CE64 TMS28C64	(72K) SRAM SMJ69CE72	
16K	(16K) SRAM SMJ61CD16	(64K) DRAM SRAM SMJ4416 SMJ64C64	(128K) EPROMs PROM TMS27C128 TMS27PC128 SMJ27C128		
32K			(256K) EPROMs PROM TMS27C256 TMS27PC256 SMJ27C256 SRAM SMJ68CE256	(288K) SRAM SMJ69CE288	
64K	(64K) DRAM VRAM SMJ4164 SMJ4161 SRAM SMJ61CD64	(256K) DRAMs VRAMs TMS4464 TMS4461 SMJ4464 SMJ4461 SRAM SMJ64C256	(512K) EPROMs PROM TMS27C512 TMS27PC512 SMJ27C512		(1024K) EPROMs TMS27C210 SMJ27C210 PROM TMX27PC210

Numbers in parentheses indicate overall complexity.

WORDS	BITS PER WORD				
	1	4	8	9	16
128K			(1024K) EPROMs PROM TMS27C010 TMX27PC010 SMJ27C010		
256K	(256K) DRAMs SRAM TMS4256 SMJ61CD256 SMJ4256 TMS4257	(1024K) DRAMs VRAM TMS44C256 TMS44C251 SMJ44C256 TMS44C257 FRAM TMS4C1050			
1024K	(1024K) DRAMs TMS4C1024 SMJ4C1024 TMS4C1025 TMS4C1027				

Numbers in parentheses indicate overall complexity.

WORDS	BITS PER WORD				
	1	4	5	8	9
256K		(1024K) TM4256EC4		(2048K) TM4256FL8 TM4256GU8	(2304K) TM4256EL9 TM4256GU9
1024K	(1024K) TM4256FC1	(4096K) TM024HAC4		(8192K) TM024GAD8	(9216K) TM024EAD9

Numbers in parentheses indicate overall complexity.

DRAM/VRAM/FRAM SELECTION GUIDE

Density	Organization (Words X Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby TTL(mW)				
64K	64K X 1	SMJ4161-15	150	5±5%	525	132	20	JD	Military Video RAM	8-3
		SMJ4161-20	200							
		SMJ4164-12	120	5±10%	264	28	16,18	JD, FG	Military	8-29
		SMJ4164-15	150		248					
		SMJ4164-20	200		203					
	16K X 4	SMJ4416-15	150	5±10%	264	28	18	JD	Military	8-47
		SMJ4416-20	200		231					
256K	256K X 1	TMS4256-8	80	5±5%	368	24	16,18, 16	N, FM, SD	Page Mode	4-3
		TMS4256-10	100	5±10%	385	25				
		TMS4256-12	120	5±10%	358	25				
		TMS4256-15	150	5±10%	330	25				
		SMJ4256-12	120	5±5%	420	27	16,18	JD, FV	Military	8-65
		SMJ4256-15	150		394					
		SMJ4256-20	200		315					
		TMS4257-10	100	5±10%	385	25	16,18, 16	N, FM, SD	Nibble Mode	4-3
		TMS4257-12	120		358					
		TMS4257-15	150		330					
	64K X 4	TMS4461-12	120	5±10%	853	110	24,24	N, SD	Multiport Video RAM	4-27
		TMS4461-15	150		770					
		SMJ4461-15	150	5±10%	770	110	24	JD	Military VRAM	8-85
		TMS4464-10	100	5±10%	385	25	18,18	N, FM	Page Mode	4-59
		TMS4464-12	120		358					
		TMS4464-15	150		330					
		SMJ4464-12	120	5±10%	440	44	18	JD	Military	8-115
		SMJ4464-15	150		385					
		SMJ4464-20	200		330					

†N Plastic Dual In-line Package (DIP)
JD Ceramic Dual In-line Package (DIP—Military)
FG,FV Ceramic Chip Carrier (CLCC—Military)
FM Plastic Chip Carrier (PLCC)
SD Plastic Zig-zag In-line Package (ZIP)

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DRAM/VRAM/FRAM SELECTION GUIDE (CONCLUDED)

Density	Organization (Words X Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby TTL(mW)				
1024K	1024K X 1	TMS4C1024-10	100	5±10%	385	17	18, 20/26	N, DJ	CMOS Enhanced Page Mode	4-151
		TMS4C1024-12	120		330					
		TMS4C1024-15	150		303					
		SMJ4C1024-12§	120	5±10%	330	17	18, 20/26	JD, HJ	Military CMOS Enhanced Page Mode	8-135
		SMJ4C1024-15§	150		303					
		TMS4C1025-10	100	5±10%	385	17	18, 20/26	N, DJ	CMOS Nibble Mode	4-151
		TMS4C1025-12	120		330					
		TMS4C1025-15	150		303					
		TMS4C1027-10	100	5±10%	385	17	18, 20/26	N, DJ	CMOS Static Column Decode Mode	4-151
		TMS4C1027-12	120		330					
		TMS4C1027-15	150		303					
	256K X 4	TMS44C251-10‡	100	5±10%	605	28	28, 28	DJ, SD	CMOS Multiport Video RAM	4-79
		TMS44C251-12‡	120		523					
		TMS44C251-15‡	150		468					
		TMS44C256-10	100	5±10%	385	17	20, 20/26	N, DJ	CMOS Enhanced Page Mode	4-119
		TMS44C256-12	120		330					
		TMS44C256-15	150		303					
		SMJ44C256-12§	120	5±10%	330	17	20, 20/26	JD, HJ	Military CMOS Enhanced Page Mode	8-133
		SMJ44C256-15§	150		303					
		TMS44C257-10	100	5±10%	385	17	20, 20/26	N, DJ	CMOS Static Column Decode Mode	4-119
		TMS44C257-12	120		330					
		TMS44C257-15	150		303					
		TMS4C1050-3‡	25	5±10%	275	39	16,20,26	N, SD, DJ	CMOS FRAM	4-189
		TMS4C1050-4‡	30		248					
		TMS4C1050-6‡	50		193					

†N Plastic Dual In-line Package (DIP)
JD Ceramic Dual In-line Package (DIP—Military)
DJ Plastic Small Outline J-lead (SOJ)
HJ Ceramic Small Outline J-lead (SOJ—Military)
SD Plastic zig-zag in-line Package (ZIP)
‡Advance Information for product under development by TI.
§Preliminary Target Specification for product under development by TI.

DYNAMIC RAM MODULE SELECTION GUIDE

Density	Organization (Words X Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby TTL(mW)				
1024K	1024K X 1	TM4256FC1-10	100	5 ± 10%	440	99	22	Leaded	Page Mode	5-9
		TM4256FC1-12	120		413					
		TM4256FC1-15	150		385					
	256K X 4	TM4256EC4-10	100	5 ± 10%	1540	99	22	Leaded	Page Mode	5-3
		TM4256EC4-12	120		1430					
		TM4256EC4-15	150		1320					
2048K	256K X 8	TM4256FL8-10	100	5 ± 10%	3080	198	30	Leaded	Page Mode	5-15
		TM4256FL8-12	120		2860					
		TM4256FL8-15	150		2640					
		TM4256GU8-10	100	5 ± 10%	3080	198	30	Socketable with Presence Detect	Page Mode	5-15
		TM4256GU8-12	120		2860					
		TM4256GU8-15	150		2640					
2304K	256K X 9	TM4256EL9-10	100	5 ± 10%	3465	226	30	Leaded	Page Mode	5-21
		TM4256EL9-12	120		3218					
		TM4256EL9-15	150		2970					
		TM4256GU9-10	100	5 ± 10%	3465	226	30	Socketable with Presence Detect	Page Mode	5-21
		TM4256GU9-12	120		3218					
		TM4256GU9-15	150		2970					
4096K	1024K X 4	TM024HAC4-10	100	5 ± 10%	1540	66	24	Leaded	CMOS Enhanced Page Mode	5-27
		TM024HAC4-12	120		1320					
		TM024HAC4-15	150		1210					
8192K	1024K X 8	TM024GAD8-10	100	5 ± 10%	3080	132	30	Socketable	CMOS Enhanced Page Mode	5-31
		TM024GAD8-12	120		2640					
		TM024GAD8-15	150		2420					
9216K	1024K X 9	TM024EAD9-10	100	5 ± 10%	3465	149	30	Socketable	CMOS Enhanced Page Mode	5-31
		TM024EAD9-12	120		2970					
		TM024EAD9-15	150		2723					

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EPROM/EEPROM SELECTION GUIDE

Density	Organization (Words X Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby TTL(mW)				
16K	2K X 8	TMS27C291-3	35	5±5%	394	N/A	24	J	High-Speed CMOS	6-3
		TMS27C291-35	35	5±10%	413					
		TMS27C291	45	5±5%	315					
		TMS27C291-45	45	5±10%	330					
		TMS27C291-5	50	5±5%	289					
		TMS27C291-50	50	5±10%	303					
		TMS27C292-3	35	5±5%	394	N/A	24	J	High-Speed CMOS	6-3
		TMS27C292-35	35	5±10%	413					
		TMS27C292	45	5±5%	315					
		TMS27C292-45	45	5±10%	330					
		TMS27C292-5	50	5±5%	289					
		TMS27C292-50	50	5±10%	303					
32K	4K X 8	TMS27C32-100‡	100	5±5%	132	1.4	24	J	CMOS	6-21
		TMS27C32-10‡	100	5±10%	138					
		TMS27C32-120‡	120	5±5%	132					
		TMS27C32-12‡	120	5±10%	138					
		TMS27C32-150‡	150	5±5%	132					
		TMS27C32-15‡	150	5±10%	138					
		TMS27C32-2‡	200	5±5%	132					
		TMS27C32-20‡	200	5±10%	138					
		TMS27C32‡	250	5±5%	132					
		TMS27C32-25‡	250	5±10%	138					
		TMS2732A-17	170	5±5%	657	158	24	J	NMOS	6-13
		TMS2732A-20	200							
		TMS2732A-25	250							
		TMS2732A-45	450							
64K	8K X 8	TMS27C49-4‡	45	5±5%	473	N/A	24	J, JT	CMOS	6-43
		TMS27C49-45‡	45	5±10%	495					
		TMS27C49-5‡	55	5±5%	473					
		TMS27C49-55‡	55	5±10%	495					
		TMS27C64-100	100	5±5%	158	1.4	28	J	CMOS	6-55
		TMS27C64-120	120	5±5%	158					
		TMS27C64-12	120	5±10%	165					
		TMS27C64-1	150	5±5%	158					
		TMS27C64-15	150	5±10%	165					
		TMS27C64-2	200	5±5%	158					
		TMS27C64-20	200	5±10%	165					
		TMS27C64	250	5±5%	158					
		TMS27C64-25	250	5±10%	165					
		TMS2764-17	170	5±5%	788	184	28	J	NMOS	6-35
		TMS2764-20	200							
		TMS2764-25	250							
		TMS2764-45	450							
		TMS28C64-25‡	250	5±10%	110	17	28	J,N	CMOS	6-69
		TMS28C64-35‡	350							

†J Ceramic DIP
JT 300-mil Ceramic DIP (TMS27C49 only)
N Plastic DIP
‡Advance Information for product under development by TI.

EPROM/EEPROM SELECTION GUIDE (CONTINUED)

Density	Organization (Words X Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby TTL(mW)				
128K	16K X 8	TMS27C128-100	100	5±5%	158	1.4	28	J	CMOS	6-79
		TMS27C128-120	120	5±5%	158					
		TMS27C128-12	120	5±10%	165					
		TMS27C128-1	150	5±5%	158					
		TMS27C128-15	150	5±10%	165					
		TMS27C128-2	200	5±5%	158					
		TMS27C128-20	200	5±10%	165					
		TMS27C128	250	5±5%	158					
		TMS27C128-25	250	5±10%	165					
		SMJ27C128-20	200	5±10%	220	1.7	28	J	Military CMOS	8-137
		SMJ27C128-25	250							
		SMJ27C128-30	300							
256K	32K X 8	TMS27C256-120	120	5±5%	158	1.4	28	J	CMOS	6-91
		TMS27C256-12	120	5±10%	165					
		TMS27C256-150	150	5±5%	158					
		TMS27C256-15	150	5±10%	165					
		TMS27C256-1	170	5±5%	158					
		TMS27C256-17	170	5±10%	165					
		TMS27C256-2	200	5±5%	158					
		TMS27C256-20	200	5±10%	165					
		TMS27C256	250	5±5%	158					
		TMS27C256-25	250	5±10%	165					
		SMJ27C256-20	200	5±10%	220	1.7	28	J	Military CMOS	8-145
		SMJ27C256-25	250							
		SMJ27C256-30	300							
512K	64K X 8	TMS27C512-1	170	5±5%	158	1.4	28	J	CMOS	6-105
		TMS27C512-17	170	5±10%	165					
		TMS27C512-2	200	5±5%	158					
		TMS27C512-20	200	5±10%	165					
		TMS27C512	250	5±5%	158					
		TMS27C512-25	250	5±10%	165					
		TMS27C512-3	300	5±5%	158					
		TMS27C512-30	300	5±10%	165					
		SMJ27C512-20	200	5±10%	263	1.8	28	J	Military CMOS	8-153
		SMJ27C512-25	250							
		SMJ27C512-30	300							

†J Ceramic DIP
JT 300-mil Ceramic DIP (TMS27C49 only)

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EPROM/EEPROM SELECTION GUIDE (CONCLUDED)

Density	Organization (Words X Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby TTL(mW)				
1024K	128K X 8	TMS27C010-170‡	170	5±5%	210	1.4	32	J	CMOS	6-119
		TMS27C010-200‡	200	5±5%	210					
		TMS27C010-20‡	200	5±10%	220					
		TMS27C010-250‡	250	5±5%	210					
		TMS27C010-25‡	250	5±10%	220					
		TMS27C010-300‡	300	5±5%	210					
		TMS27C010-30‡	300	5±10%	220					
		SMJ27C010-250§	250	5±10%	220	1.5	32	J	Military CMOS	8-163
		SMJ27C010-300§	300							
	64K X 16	TMS27C210-170‡	170	5±5%	210	1.4	40	J	CMOS	6-131
		TMS27C210-200‡	200	5±5%	210					
		TMS27C210-20‡	200	5±10%	220					
		TMS27C210-250‡	250	5±5%	210					
		TMS27C210-25‡	250	5±10%	220					
		TMS27C210-300‡	300	5±5%	210					
		TMS27C210-30‡	300	5±10%	220					
		SMJ27C210-250§	250	5±10%	220	1.5	40	J	Military CMOS	8-165
		SMJ27C210-300§	300							

†J Ceramic DIP
JT 300-mil Ceramic DIP (TMS27C49 only)
‡Advance Information for product under development by TI.
§Preliminary Target Specification for product under development by TI.

ONE-TIME PROGRAMMABLE PROM SELECTION GUIDE

Density	Organization (Words X Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby TTL(mW)				
16K	2K X 8	TMS27PC291-3‡	35	5±5%	394	N/A	24,28	N, FN	High-Speed CMOS	6-3
		TMS27PC291-35‡	35	5±10%	413					
		TMS27PC291‡	45	5±5%	315					
		TMS27PC291-45‡	45	5±10%	330					
		TMS27PC291-5‡	50	5±5%	289					
		TMS27PC291-50‡	50	5±10%	303					
32K	4K X 8	TMS27PC32-120‡	120	5±5%	132	1.4	24	N	CMOS	6-21
		TMS27PC32-12‡	120	5±10%	138					
		TMS27PC32-150‡	150	5±5%	132					
		TMS27PC32-15‡	150	5±10%	138					
		TMS27PC32-2‡	200	5±5%	132					
		TMS27PC32-20‡	200	5±10%	138					
		TMS27PC32‡	250	5±5%	132					
		TMS27PC32-25‡	250	5±10%	138					
64K	8K X 8	TMS27PC49-4‡	45	5±5%	473	N/A	24,24, 28	N, NT, FN	CMOS	6-43
		TMS27PC49-45‡	45	5±10%	495					
		TMS27PC49-5‡	55	5±5%	473					
		TMS27PC49-55‡	55	5±10%	495					
		TMS27PC64-120	120	5±5%	158	1.4	28	N	CMOS	6-55
		TMS27PC64-12	120	5±10%	165					
		TMS27PC64-1	150	5±5%	158					
		TMS27PC64-15	150	5±10%	165					
		TMS27PC64-2	200	5±5%	158					
		TMS27PC64-20	200	5±10%	165					
		TMS27PC64	250	5±5%	158					
		TMS27PC64-25	250	5±10%	165					
128K	16K X 8	TMS27PC128-1	150	5±5%	158	1.4	28,32	N, FM	CMOS	6-79
		TMS27PC128-15	150	5±10%	165					
		TMS27PC128-2	200	5±5%	158					
		TMS27PC128-20	200	5±10%	165					
		TMS27PC128	250	5±5%	158					
		TMS27PC128-25	250	5±10%	165					
256K	32K X 8	TMS27PC256-150	150	5±5%	158	1.4	28,32	N, FM	CMOS	6-91
		TMS27PC256-15	150	5±10%	165					
		TMS27PC256-1	170	5±5%	158					
		TMS27PC256-17	170	5±10%	165					
		TMS27PC256-2	200	5±5%	158					
		TMS27PC256-20	200	5±10%	165					
		TMS27PC256	250	5±5%	158					
		TMS27PC256-25	250	5±10%	165					

†N Plastic DIP
NT 300-mil Plastic DIP (TMS27PC49 only)
FM Plastic Chip Carrier
FN Plastic Chip Carrier
‡Advance Information for product under development by TI.

TEXAS INSTRUMENTS
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ONE-TIME PROGRAMMABLE PROM SELECTION GUIDE (CONCLUDED)

Density	Organization (Words X Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby TTL(mW)				
512K	64K X 8	TMS27PC512-2	200	5±5%	158	1.4	28,32	N, FM	CMOS	6-105
		TMS27PC512-20	200	5±10%	165					
		TMS27PC512	250	5±5%	158					
		TMS27PC512-25	250	5±10%	165					
		TMS27PC512-3	300	5±5%	158					
		TMS27PC512-30	300	5±10%	165					
1024K	128K X 8	TMX27PC010-200§	200	5±5%	210	1.4	32	N	CMOS	6-143
		TMX27PC010-20§	200	5±10%	220					
		TMX27PC010-250§	250	5±5%	210					
		TMX27PC010-25§	250	5±10%	220					
		TMX27PC010-300§	300	5±5%	210					
		TMX27PC010-30§	300	5±10%	220					
	64K X 16	TMX27PC210-200§	200	5±5%	210	1.4	40	N	CMOS	6-145
		TMX27PC210-20§	200	5±10%	220					
		TMX27PC210-250§	250	5±5%	210					
		TMX27PC210-25§	250	5±10%	220					
		TMX27PC210-300§	300	5±5%	210					
		TMX27PC210-30§	300	5±10%	220					

†N Plastic DIP
NT 300-mil Plastic DIP (TMS27PC49 only)
FM Plastic Chip Carrier
FN Plastic Chip Carrier

§Preliminary Target Specification for product under development by TI.

MILITARY SRAM SELECTION GUIDE

Density	Organization (Words X Bits)	Device Number	Max Access Time (ns)	Power Supply (V)	Max Power Dissipation		Pins	Package†	Comments	Page
					Active (mW)	Standby TTL(mW)				
16K	16K X 1	SMJ61CD16-25 SMJ61CD16-35 SMJ61CD16-45	25 35 45	5±10%	650	55	20	JD, FG	CMOS Military Separate I/O Pins	8-167
	4K X 4	SMJ64C16-25‡ SMJ64C16-35‡ SMJ64C16-45‡	25 35 45	5±10%	650	55	20	JD, FG	CMOS Military	8-177
	2K X 8	SMJ68CE16-25‡ SMJ68CE16-35‡ SMJ68CE16-45‡	25 35 45	5±10%	650	55	24,32	JD, FG	CMOS Military Output Enable Control	8-187
64K	64K X 1	SMJ61CD64-25‡ SMJ61CD64-35‡ SMJ61CD64-45‡	25 35 45	5±10%	715	55	22	JD, FG	CMOS Military Separate I/O Pins	8-197
	16K X 4	SMJ64C64-25‡ SMJ64C64-35‡ SMJ64C64-45‡	25 35 45	5±10%	715	55	22	JD, FG	CMOS Military	8-207
	8K X 8	SMJ68CE64-25‡ SMJ68CE64-35‡ SMJ68CE64-45‡	25 35 45	5±10%	715	55	28,32	JD, FG	CMOS Military Output Enable Control	8-217
72K	8K X 9	SMJ69CE72-25‡ SMJ69CE72-35‡ SMJ69CE72-45‡	25 35 45	5±10%	715	55	28,32	JD, FG	CMOS Military Output Enable Control	8-227
256K	256K X 1	SMJ61CD256-35‡ SMJ61CD256-45‡ SMJ61CD256-55‡	35 45 55	5±10%	440	55	24,28	JD, FG	CMOS Military Separate I/O Pins	8-237
	64K X 4	SMJ64C256-35§ SMJ64C256-45§ SMJ64C256-55§	35 45 55	5±10%	440	55	24,28	JD, FG	CMOS Military	8-239
	32K X 8	SMJ68CE256-35§ SMJ68CE256-45§ SMJ68CE256-55§	35 45 55	5±10%	440	55	28,32	JD, FG	CMOS Military Output Enable Control	8-241
288K	32K X 9	SMJ69CE288-35§ SMJ69CE288-45§ SMJ69CE288-55§	35 45 55	5±10%	440	55	32	JD, FG	CMOS Military Output Enable Control	8-243

†JD Ceramic Dual In-line Package (DIP—Military)
FG Ceramic Chip Carrier (CLCC—Military)
‡Advance Information for product under development by TI.
§Preliminary Target Specification for product under development by TI.

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VLSI MEMORY MANAGEMENT PRODUCTS

DRAM CONTROLLERS
PROVIDE ADDRESS MULTIPLEXING AND REFRESH CONTROL

Device Type	Features	t_{pd} (ns) MAX†	Pins	Page
TMS4500A	64K DRAMs, On-chip Refresh Timing Control	250	40	7-211
THCT4502B	256K DRAMs, On-chip Refresh Timing Control	115	48	7-197
75ALS2967	256K DRAMs, >200 to 60 ns DRAMs, $\overline{RAS}$, $\overline{CAS}$	35	48	7-157
74ALS2968	256K DRAMs, >200 to 60 ns DRAMs, $\overline{RAS}$, $\overline{CAS}$	35	48	7-157
74ALS6301	1 Megabit DRAMs, >200 to 60 ns DRAMs, $\overline{RAS}$, $\overline{CAS}$	35	52	7-177
74ALS6302	1 Megabit DRAMs, >200 to 60 ns DRAMs, $\overline{RAS}$, $\overline{CAS}$	35	52	7-177

†Memory Access Time

CACHE ADDRESS COMPARATORS
ON-CHIP PARITY GENERATION AND CHECKING

Device Type	Features	t_{pd} (ns) MAX‡	Pins	Page
TACT2150	1 μm EPIC™, Fastest Available, 512 × 8 RAM	30/20	24	7-149
74ACT2151	1K × 11 Cache Tag RAM	25/35	28	7-151
74ACT2152	2K × 8 Cache Tag RAM	25/35	28	7-135
74ACT2153	1K ×11 Cache Tag RAM with Open Drain Match Pin	25/35	28	7-121
74ACT2154	2K ×8 Cache Tag RAM with Open Drain Match Pin	25/35	28	7-135

‡Address Match Time
EPIC™ is a trademark of Texas Instruments Incorporated.

ERROR DETECTION AND CORRECTION UNITS
CORRECTS 1-BIT MEMORY ERRORS AND FLAGS 2-BIT ERRORS

Device Type	Features	t_{pd} (ns) MAX§	Pins	Page
74ALS632B	32-bit, 3-state with Byte-Write Capability	30	52	7-89
74ALS634B	32-bit, 3-state, No Byte-Write	30	48	7-89
74AS632	Fastest 32-bit EDAC Available	25	52	7-107
74AS634	32-bit, 3-state, No Byte-Write (Speed Enhanced 'ALS634)	25	48	7-107

§Single Bit Detection Time

MOS MEMORY DRIVERS WITH SERIES DAMPING RESISTORS

Device Type	Features	I_{OL} (mA) MAX	Pins	Page
74BCT2827A	BiCMOS 10-bit Buffer/Driver, 3-state Output	12	24	7-235
74BCT2828A	BiCMOS 10-bit Buffer/Driver, Inverting 3-state Output	12	24	7-235
74BCT29827A	BiCMOS 10-bit Buffer/Driver, 3-state Output	48	24	7-241
74BCT29828A	BiCMOS 10-bit Buffer/Driver, Inverting 3-state Output	48	24	7-241

MEMORY ACCESS DETECTORS

Device Type	Features	t_{pd} (ns) MAX	Pins	Page
74ALS6310	Static Column and Page Mode, High Performance Compare	18	20	7-227
74ALS6311	Static Column and Page Mode, High Performance Compare	14	20	7-227

FIRST-IN FIRST-OUT (FIFO) MEMORIES

Device Type	Density	f_{max}	Depth Expansion	Pins	Page
74ALS229A	16 × 5	30	No	20	7-3
74ALS232A	16 × 4	30	No	16	7-9
74ALS233A	16 × 5	30	No	20	7-13
74ALS234	64 × 4	30	Yes	16	7-19
74ALS235	64 × 5	25	Yes	20	7-27
74ALS236†	64 × 4	30	Yes	16	7-39
74ALS2232	64 × 8	40	No	24	7-77
74ALS2233	64 × 9	40	No	28	7-83
74ACT7201A	512 × 9	28	Yes	28	7-47
74ACT7202	1K × 9	22	Yes	28	7-63

†Compatible with the '67401

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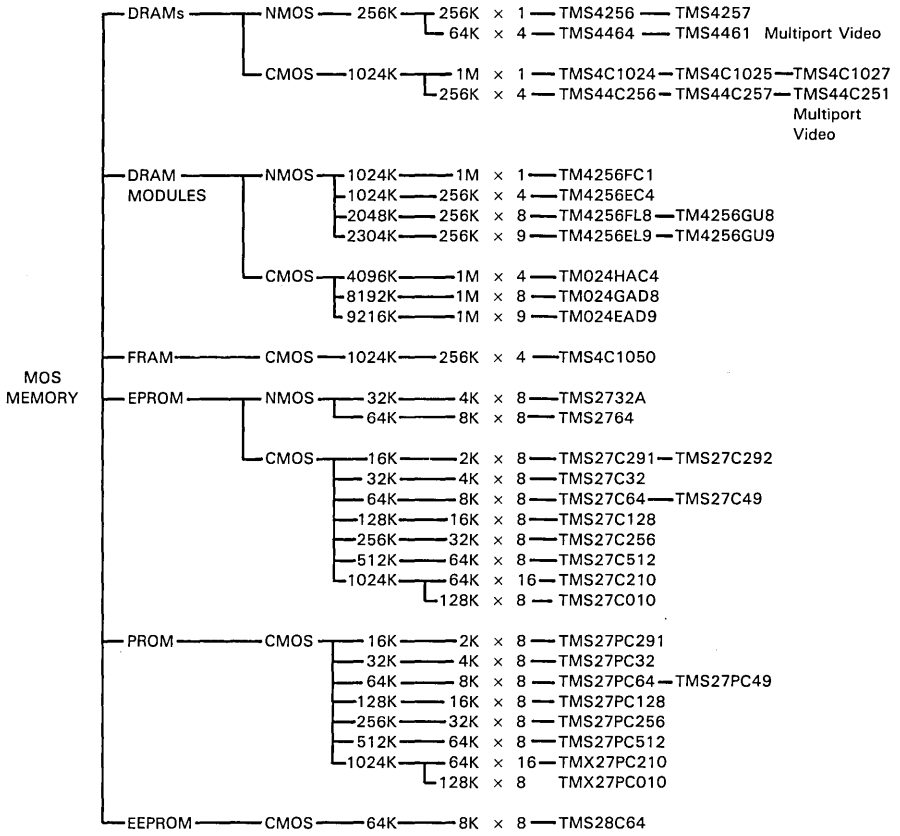
MOS MEMORY LINE-UP†



†Only commercial devices are listed.

DRAMs

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
64K X 4 VRAM	TI		TMS4461
		Fujitsu	MB81461
		Hitachi	HM53462/HM53461
		Hyundai	HY51C264
		Mitsubishi	M5M4C264P
		NEC	μPD41264/μPD42264
		Vitelic	V51C261/V51C264
64K X 4	TI		TMS4464
		Fujitsu	MB81C466/MB81464
		Hitachi	HM50464/HM50465
		Hyundai	HY51464/HY51C464
		Intel	51C259
		Micron Tech	MT4064/MT4067
		Mitsubishi	M5M4464
		NEC	μPD41464
		OKI	MSM41464
		Sharp	LH2464/LH2465
		Toshiba	TMM41464
256K X 1 PAGE MODE	TI		TMS4256
		AMD	AM90C256
		AT&T	M41256P
		Fujitsu	MB81256/MB41256
		Hitachi	HM50256
		Hyundai	HY51C256L/HY51256
		Intel	51C256H
		Micron Tech	MT1256
		Mitsubishi	M5M4256
		Mostek	MK45H6
		Motorola	MCM6256B
		NEC	μPD41256
		NMB	AAA2800
		OKI	MSM41256
		Panasonic	MN41256
		Samsung	KM41256
		Sharp	LH21256
		Toshiba	TMM41256
256K X 1 NIBBLE MODE	TI		TMS4257
		AMD	AM90C255
		AT&T	M41256N
		Fujitsu	MB81257/MB41257
		Hitachi	HM50257
		Mitsubishi	M5M4257
		NEC	μPD41257
		NMB	AAA2800
		OKI	MSM41257
		Samsung	KM41257
		Sharp	LH21257
		Toshiba	TMM41257

DRAMs (CONCLUDED)

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
256K X 4 VIDEO RAM	TI		TMS44C251
		Fujitsu	MB81C4251/MB81C4252
		Hitachi	HM534251/2/3
		OKI	MSM514251/MSM514252
		Toshiba	TC524256/TC524257
256K X 4 ENHANCED PAGE MODE	TI		TMS44C256
		AT&T	M441024
		Hitachi	HM514256
		Mitsubishi	M5M44C256
		NEC	μPD414256/μPD424256
		NMB	AAA1M104/AAA1M204
		OKI	MSM414256/MSM514256
		Sharp	LH64256
		Toshiba	TC514256
256K X 4 STATIC COLUMN DECODE	TI		TMS44C257
		Mitsubishi	M5M44C258
		NMB	AAA1M104/AAA1M204
		OKI	MSM514257
		Sharp	LH64256
		Toshiba	TC514258
1M X 1 ENHANCED PAGE MODE	TI		TMS4C1024
		AT&T	M511024
		Fujitsu	MB811000
		Hitachi	HM511000
		Hyundai	HY51C100
		Micron Tech	MT41C001
		Mitsubishi	M5M4C1000
		NEC	μPD411000
		NMB	AAA1M100/AAA1M200
		OKI	MSM411000/MSM511000
		Panasonic	MN411000
		Toshiba	TC511000
1M X 1 NIBBLE MODE	TI		TMS4C1025
		Fujitsu	MB811001
		Mitsubishi	M5M4C1001
		NEC	μPD411001
		NMB	AAA1M200
		OKI	MSM411001
		Toshiba	TC511001
1M X 1 STATIC COLUMN DECODE	TI		TMS4C1027
		Hitachi	HM511001
		Mitsubishi	M5M4C1002
		NMB	AAA1M100/AAA1M200
		OKI	MSM511001
		Toshiba	TC511002

DYNAMIC RAM MODULES

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
256K X 4	TI		TM4256EC4
		DENSE-PAC	DPD44256
		Fujitsu	MB85203/MB85204
		Hitachi	HB561004A
		Micron Tech	MT4259
		NEC	MC41256A4
256K X 8	TI		TM4256FL8
		DENSE-PAC	DPD42568
		Hitachi	HB451008B
		Micron Tech	MT8259
		Mitsubishi	MH25608A
		NEC	MC41256A8
		NMB	MM2800
		OKI	MSC2304KS8
256K X 8	TI		TM4256GU8
		DENSE-PAC	DPD42568
		Hitachi	HB561008B
		Micron Tech	MT8259
		Mitsubishi	MH25608
		NEC	MC41256A8
		NMB	MM2800
		OKI	MSC2304YS8
256K X 9	TI		TM4256EL9
		DENSE-PAC	DPD42569
		Fujitsu	MB85227
		Hitachi	HB561003/HB561009
		Micron Tech	MT9259
		Mitsubishi	MH25609A
		NMB	MM2800
		NEC	MC41256A9
		OKI	MSC2304KS9
		Toyocom	TH22569/TH32569
256K X 9	TI		TM4256GU9
		DENSE-PAC	DPD42569
		Fujitsu	MB85227
		Hitachi	HB561003/HB561009
		Micron Tech	MT9259
		Mitsubishi	MH25609
		NMB	MM2800
		NEC	MC441256A9
		OKI	MSC2304YS9
		Toyocom	TH22569/TH32569
1M X 1	TI		TM4256FC1
		DENSE-PAC	DPD411M
		EDI	DH411M-__C4/EDH411M-__C4
		Fujitsu	MB85201/MB85208
		NEC	MC411000A1
1M X 4	TI		TM024HAC4

DYNAMIC RAM MODULES (CONCLUDED)

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
1M X 8	TI		TM024GAD8
		Interplex (NAS)	1TM-S-1000-P-08
		Micron	MT8C8024MN
		Mitsubishi	MH1M08
		OKI	2310-__YS8
		Toshiba	THM81000S
1M X 9	TI		TM024EAD9
		Hitachi	HB56A19B
		Interplex (NAS)	1TM-S-1000-P-09
		Micron	MTC9024MN
		Mitsubishi	MH1M09
		OKI	2310-__YS9
		Toshiba	THM91000S

TEXAS INSTRUMENTS
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EPROMs

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
2K X 8 HIGH SPEED CMOS	TI		TMS27C292
		AMD	AM27S191A
		Cypress	CY7C292
		ICT	27CX322
		MMI	63S1681
		National	DM87S291
		Signetics	N82S191
		Waferscale	WS57C291
4K X 8 NMOS	TI		TMS2732A
		AMD	AM2732A/AM2732B
		Fujitsu	MBM2732A
		Hitachi	HN482732
		Intel	2732A
		National	NMC27C32
		Panatech	RD27C32
		SGS	M2732A
4K X 8 CMOS	TI		TMS27C32
		National	NMC27C32
		Panatech	RD27C32
8K X 8 NMOS	TI		TMS2764
		AMD	AM2764A
		Fujitsu	MBM2764
		Hitachi	HN482764
		Hyundai	HY2764
		Intel	2764A
		Mitsubishi	M5L2764
		Motorola	MSM68764
		NEC	μPD2764
		OKI	MSM2764
		SEEQ	5133/2764
		SGS	M2764
		Toshiba	TMM2764
8K X 8 CMOS	TI		TMS27C64
		Atmel	AM27HC64
		Cypress	CY7C261/CY7C263/CY7C264
		Cypress	CY7C268/CY7C269
		Fujitsu	MBM27C64
		GI	27C64
		Goldstar	GM27HC64
		Hitachi	HN27C64
		Hyundai	HY27C64
		Intel	27C64/87C64
		National	NMC27C64
		NEC	μPD27C64
		OKI	MSM27C64
		S-MOS	SPM27C64
		Signetics	27C64/87C64
		Thomson	TS27C64
		Waferscale	WS27C64F/WS27C49

EPROMs (CONTINUED)

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
16K X 8 CMOS	TI		TMS27C128
		AMD	AM27128
		Atmel	AT27C128
		Fujitsu	MBM27C128/MBM27128
		GI	27C128
		Hitachi	HN27128A/HN4827128G
		Mitsubishi	M5L27128/M5M27C128
		National	NMC27CP128
		NEC	μPD27128
		OKI	MSM27128/MSM27C128
		S-MOS	SPM27129C
		SEEQ	27128
		Toshiba	TMM27128
		VLSI	VT27C128
		VTI	VT27C128
		Waferscale	WS57C128F/WS57C251
32K X 8 CMOS	TI		TMS27C256
		AMD	AM27C256/AM27256
		Atmel	AT27C256/AT27256
		Fujitsu	MBM27C256/MBM27256
		Hitachi	HN27C256/HN27256
		GI	27C256/27256
		Intel	27256/27C256
		Mitsubishi	M5M27C256/M5L27256
		Motorola	MCM67256/9
		National	NMC27C256
		NEC	μPD27256
		OKI	MSM27C256/MSM27256
		Panatech	RD27C256
		S-MOS	SPM27C256
		SEEQ	27C256
		SGS	M27256A
		Signetics	27C256
		Thomson	TS27C256
		Toshiba	TMM27256/TC57256
		Waferscale	WS57C256F
64K X 8 CMOS	TI		TMS27C512
		AMD	AM27512/AM27C512
		Atmel	AT27C512
		Fujitsu	MBM27C512
		GI	27C512
		Hitachi	HN27512
		Intel	27512
		Mitsubishi	M5L27512
		National	NMC27C512
		NEC	μPD27C512
		OKI	MSM27512
		Panatech	TMS27C512
		Toshiba	TC57512/TMM27512

EPROMs (CONCLUDED)

ORGANIZATION	VENDOR		PART NUMBER
	TI	ALTERNATE SOURCES	
64K X 16 CMOS	TI		TMS27C210
		AMD	AM27C1024
		Atmel	AT27C1024
		Fujitsu	MBM27C1024
		Intel	27210
		National	NMC27C1024
		NEC	μPD27C1024
		OKI	MSM271024/MSM27C1024
		Toshiba	TC571024
128K X 8 CMOS	TI		TMS27C010
		Atmel	AT27C010
		Fujitsu	MBM27C1000/1
		Hitachi	HN27C101
		Intel	27010
		Mitsubishi	M5M27C100/1/2
		NEC	μPD27C1000
		OKI	MSM271000
		Toshiba	TC571000

Glossary/Timing Conventions/Data Sheet Structure

PART I — GENERAL CONCEPTS AND TYPES OF MEMORIES

Address — Any given memory location in which data can be stored or from which it can be retrieved.

Automatic Chip-Select/Power Down — (see Chip Enable Input)

Bit — Contraction of Binary digIT, i.e., a 1 or a 0; in electrical terms the value of a bit may be represented by the presence or absence of charge, voltage, or current.

Byte — A word of 8 bits (see word)

CMOS — A complementary MOS technology which uses transistors with electron (N-channel) and hole (P-channel) conduction.

Chip Enable Input — A control input to an integrated circuit that when active permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and when inactive causes the integrated circuit to be in a reduced power standby mode.

Chip Select Input — Chip select inputs are gating inputs that control the input to and output from the memory. They may be of two kinds:

1. Synchronous—Clocked/latched with the memory clock. Affects the inputs and outputs for the duration of that memory cycle.
2. Asynchronous—Has direct asynchronous control of inputs and outputs. In the read mode, an asynchronous chip select functions like an output enable.

Column Address Strobe (CAS) — A clock used in dynamic RAMs to control the input of column addresses. It can be active high (CAS) or active low ($\overline{\text{CAS}}$).

Data — Any information stored or retrieved from a memory device.

DIP — Dual In-line Package.

Dynamic (Read/Write) Memory (DRAM) — A read/write memory in which the cells require the repetitive application of control signals in order to retain the stored data.

NOTES:
1. The words "read/write" may be omitted from the term when no misunderstanding will result.
2. Such repetitive application of the control signals is normally called a refresh operation.
3. A dynamic memory may use static addressing or sensing circuits.
4. This definition applies whether the control signals are generated inside or outside the integrated circuit.

Electrically Erasable Programmable Read-Only Memory (EEPROM) — A nonvolatile memory that can be field-programmed like a PROM or EPROM, but that can be electrically erased by a combination of electrical signals at its inputs.

Erasable and Programmable Read-Only Memory (EPROM) — A field-programmable read-only memory that can have the data content of each memory cell altered more than once.

Erase — Typically associated with EPROMs and EEPROMs. The procedure whereby programmed data is removed and the device returns to its unprogrammed state.

FRAM — First-in First-out pseudo static RAM or Field RAM.

Field-Programmable Read-Only Memory — (see One-time Programmable Read-Only Memory)

Fixed Memory — A common term for ROMs, EPROMs, EEPROMs, etc., containing data that is not normally changed. A more precise term for EPROMs and EEPROMs is nonvolatile since their data may be easily changed.

Fully Static RAM — In a fully static RAM, the periphery as well as the memory array is fully static. The periphery is thus always active and ready to respond to input changes without the need for clocks. There is no precharge required for static periphery.

K — When used in the context of specifying a given number of bits of information, 1K = 2^{10} = 1024 bits. Thus, 64K = 64 X 1024 = 65,536 bits.

Large-Scale Integration (LSI) — The description of any IC technology that enables condensing more than 100 gates onto a single chip.

Mask-Programmed Read-Only Memory — A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Memory — A medium capable of storing information that can be retrieved.

Memory Cell — The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

Metal-Oxide Semiconductor (MOS) — The technology involving photolithographic layering of metal and oxide to produce a semiconductor device.

NMOS — A type of MOS technology in which the basic conduction mechanism is governed by electrons. (Short for N-channel MOS)

Nonvolatile Memory — A memory in which the data content is maintained whether the power supply is connected or not.

One-time Programmable Read-Only Memory (PROM) — A read-only memory that after being manufactured, can have the data content of each memory cell altered once.

Output Enable — A control input that, when true, permits data to appear at the memory output, and when false, causes the output to assume a high-impedance state. (See also chip select)

PLCC — Plastic Leaded Chip Carrier package.

PMOS — A type of MOS technology in which the basic conduction mechanism is governed by holes. (Short for P-channel MOS)

Parallel Access — A feature of a memory by which all the bits of a byte or word are entered simultaneously at several inputs or retrieved simultaneously from several outputs.

Power Down — A mode of a memory during which the device is operating in a low-power or standby mode. Normally read or write operations of the memory are not possible under this condition.

Program — Typically associated with EPROM and PROM memories, the procedure whereby logical 0s (or 1s) are stored into various desired locations in a previously erased device.

Program Enable — An input signal that when true, puts a programmable memory device into the program mode.

Programmable Read-Only Memory (PROM) — (see One-time Programmable Read-Only Memory)

Printed Wiring Board (PWB) — A substrate of epoxy glass, clad material, or other material upon which a pattern of conductive traces is formed to interconnect the components which will be mounted upon it.

Read — A memory operation whereby data is output from a desired address location.

Read-Only Memory (ROM) — A memory in which the contents are not intended to be altered during normal operation.

NOTE: Unless otherwise qualified, the term "read-only memory" implies that the contents is determined by its structure and is unalterable.

Read/Write Memory — A memory in which each cell may be selected by applying appropriate electrical input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electrical input signals.

Row Address Strobe (RAS) — A clock used in dynamic RAMs to control the input of the row addressed. It can be active high (RAS) or active low ($\overline{\text{RAS}}$).

SOJ — Small Outline J-lead package.

Scaled-MOS (SMOS) — MOS technology under which the device is scaled down in size in three dimensions and in operating voltages allowing improved performance.

Semi-Static (Quasi-Static, Pseudo-Static) RAM — In a semi-static RAM, the periphery is clock-activated (i.e., dynamic). Thus the periphery is inactive until clocked, and only one memory cycle is permitted per clock. The peripheral circuitry must be allowed to reset after each active memory cycle for a minimum precharge time. No refresh is required.

Serial Access — A feature of a memory by which all the bits are entered sequentially at a single input or retrieved sequentially from a single output.

SIP — Single In-line package.

Small Outline Integrated Circuit (SOIC) — A package in which an integrated circuit chip can be mounted to form a surface-mounted component. It is made of a plastic material which can withstand high temperatures and has leads formed in a gull-wing shape along its two longer sides for connection to a PWB footprint.

Static RAM (SRAM) — A read/write random-access device within which information is stored as latched voltage levels. The memory cell is a static latch that retains data as long as power is applied to the memory array. No refresh is required. The type of periphery circuitry sub-categorizes static RAMs.

Very-Large-Scale Integration (VLSI) — The description of any IC technology that is much more complex than large-scale integration (LSI), and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

Volatile Memory — A memory in which the data content is lost when power supplied is disconnected.

Word — A series of one or more bits that occupy a given address location and that can be stored and retrieved in parallel.

Write — A memory operation whereby data is written into a desired address location.

Write Enable — A control signal that when true causes the memory to assume the write mode, and when false causes it to assume the read mode.

ZIP — Zig-zag In-line package.

PART II — OPERATING CONDITIONS AND CHARACTERISTICS (INCLUDING LETTER SYMBOLS)

Capacitance

The inherent capacitance on every pin, which can vary with various inputs and outputs.

Example symbology:

C_i	Input capacitance
C_o	Output capacitance
$C_{i(D)}$	Input capacitance, data input

Current

High-level input current, I_{IH}
The current into an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}
The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input current, I_{IL}
The current into an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}
The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}
The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}
The current into* an output when the output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{BB}, I_{CC}, I_{DD}, I_{PP}
The current into, respectively, the V_{BB}, V_{CC}, V_{DD}, V_{PP} supply terminals.

*Current out of a terminal is given as a negative value.

Operating Free-Air Temperature

The temperature (T_A) range over which the device will operate and meet the specified electrical characteristics.

Operating Case Temperature

The case temperature (T_C) range over which the device will operate and meet the specified electrical characteristics.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Supply voltages, V_{BB}, V_{CC}, V_{DD}, V_{PP}

The voltages supplied to the corresponding voltage pins that are required for the device to function. From one to four of these supplies may be necessary, along with ground, V_{SS}.

Time Intervals

New or revised data sheets in this book use letter symbols in accordance with standards recently adopted by JEDEC, the IEEE, and the IEC. Two basic forms are used. The first form is usually used in this book when intervals can easily be classified as access, cycle, disable, enable, hold, refresh, setup, transition, or valid times and for pulse durations. The second form can be used generally but in this book is used primarily for time intervals not easily classifiable. The second (unclassified) form will be described first. Since some manufacturers use this form for all time intervals, symbols in the unclassified form are given with the examples for most of the classified time intervals.

Unclassified time intervals

Generalized letter symbols can be used to identify almost any time interval without classifying it using traditional or contrived definintions. Symbols for unclassified time intervals identify two signal events listed in from-to sequence using the format:

$$t_{AB\text{-}CD}$$

Subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval. Every effort is made to keep the A and C subscript length down to one letter, if possible (e.g., R for $\overline{RAS}$ and C for $\overline{CAS}$).

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high
L = low or transition to low
V = a valid steady-state level
X = unknown, changing, or "don't care" level
Z = high-impedance (off) state

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur.

For examples of symbols of this type, see TMS4256 (e.g., t_{RLCL}).

Classified time intervals (general comments, specific times follow)

Because of the information contained in the definitions, frequently the identification of one or both of the two signal events that begin and end the intervals can be significantly shortened compared to the unclassified forms. For example, it is not necessary to indicate in the symbol that an access time ends with valid data at the output. However, if both signals are named (e.g., in a hold time), the from-to sequence is maintained.

Access time

The time interval between the application of a specific input pulse and the availability of valid signals at an output.

Example symbology:

Classified	Unclassified	Description
$t_{a(A)}$	t_{AVQV}	Access time from address
$t_{a(S)}$, $t_{a(CS)}$	t_{SLQV}	Access time from chip select (low)

Cycle time

The time interval between the start and end of a cycle.

NOTE: The cycle time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval that must be allowed for the digital circuit to perform a specified function (e.g., read, write, etc.) correctly.

Example symbology:

Classified	Unclassified	Description
$t_{c(R)}$, $t_{c(rd)}$	$t_{AVAV(R)}$	Read cycle time
$t_{c(W)}$	$t_{AVAV(W)}$	Write cycle time

NOTE: R is usually used as the abbreviation for "read"; however, in the case of dynamic memories, "rd" is used to permit R to stand for RAS.

Disable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Example symbology:

Classified	Unclassified	Description
$t_{dis(S)}$	t_{SHQZ}	Output disable time after chip select (high)
$t_{dis(W)}$	t_{WLQZ}	Output disable time after write enable (low)

These symbols supersede the older forms t_{PVZ} or t_{PXZ}.

Enable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: For memories these intervals are often classified as access times.

Example symbology:

Classified	Unclassified	Description
$t_{en(SL)}$	t_{SLQV}	Output enable time after chip select low

These symbols supersede the older form t_{PZV}.

Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{h(D)}$	t_{WHDX}	Data hold time (after write high)
$t_{h(RHrd)}$	t_{RHWH}	Read (write enable high) hold time after $\overline{RAS}$ high
$t_{h(CHrd)}$	t_{CHWH}	Read (write enable high) hold time after $\overline{CAS}$ high
$t_{h(CLCA)}$	$t_{CL\text{-}CAX}$	Column address hold time after $\overline{CAS}$ low
$t_{h(RLCA)}$	$t_{RL\text{-}CAX}$	Column address hold time after $\overline{RAS}$ low
$t_{h(RA)}$	$t_{RL\text{-}RAX}$	Row address hold time (after $\overline{RAS}$ low)

These last three symbols supersede the older forms:

NEW FORM	OLD FORM
$t_{h(CLCA)}$	$t_{h(ACL)}$
$t_{h(RLCA)}$	$t_{h(ARL)}$
$t_{h(RA)}$	$t_{h(AR)}$

NOTE: The from-to sequence in the order of subscripts in the unclassified form is maintained in the classified form. In the case of hold times, this causes the order to seem reversed from what would be suggested by the terms.

Pulse duration (width)

The time interval between the specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

Classified	Unclassified	Description
$t_{w(W)}$	t_{WLWH}	Write pulse duration
$t_{w(RL)}$	t_{RLRH}	Pulse duration, $\overline{RAS}$ low

Refresh time interval

The time interval between the beginnings of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

NOTE: The refresh time interval is the actual time interval between two refresh operations and is determined by the system in which the digital circuit operates. A maximum value is specified that is the longest interval for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
t_{rf}		Refresh time interval

Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{su(D)}$	t_{DVWH}	Data setup time (before write high)
$t_{su(CA)}$	t_{CAV-CL}	Column address setup time (before $\overline{CAS}$ low)
$t_{su(RA)}$	t_{RAV-RL}	Row address setup time (before $\overline{RAS}$ low)

Transition times (also called rise and fall times)

The time interval between two reference points (10% and 90% unless otherwise specified) on the same waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

Example symbology:

Classified	Unclassified	Description
t_t		Transition time (general)
$t_{t(CH)}$	t_{CHCH}	Low-to-high transition time of $\overline{CAS}$
$t_{r(C)}$	t_{CHCH}	$\overline{CAS}$ rise time
$t_{f(C)}$	t_{CLCL}	$\overline{CAS}$ fall time

Valid time

(a) General

The time interval during which a signal is (or should be) valid.

(b) Output data-valid time

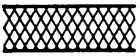
The time interval in which output data continues to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

Example symbology:

Classified	Unclassified	Description
$t_{v(A)}$	t_{AXQX}	Output data valid time after change of address.

This supersedes the older form t_{PVX}.

PART III — TIMING DIAGRAMS CONVENTIONS

TIMING DIAGRAM SYMBOL	MEANING	
	INPUT FORCING FUNCTIONS	OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low some time during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Centerline represents high-impedance (off) state.

PART IV — BASIC DATA SHEET STRUCTURE

The front page of the data sheet begins with a list of key *features* such as organization, interface, compatibility, operation (static or dynamic), access and cycle times, technology (N or P channel, silicon or metal oxide gate), and power. In addition, the top view of the device is shown with the *pinout* provided. Next a general *description* of the device, system interface considerations, and elaboration on other device characteristics are presented. The next section is an explanation of the device's *operation* which includes the function of each pin (i.e., the relationship between each input (output) and a given type of memory). The functions basically involve starting, achieving, and ending a given type of memory cycle (e.g., programming or erasing EPROMs, or reading a memory location).

Augmenting the descriptive text there appears a *logic symbol* prepared in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12 and explained in Section 11 of this book. Following the symbol is usually a *functional block diagram*, a flowchart of the basic internal structure of the device showing the signal paths for data, addresses, and control signals, as well as the internal architecture. Usually the next few pages contain the absolute maximum ratings (e.g., voltage supplies, input voltage, and temperature) applicable over the *operating free-air temperature range*. If the device is used outside of these values, it may be permanently destroyed or at least it would not function as intended. Next, typically, are the *recommended operating conditions*, (e.g., supply voltages, input voltages, and operating temperature). The memory device is guaranteed to work reliably and to meet all data sheet parameters when operated in accord with the recommended operating conditions and within the specified timing. If the device is operated outside of these limits (minimum/maximum) it is no longer guaranteed to meet the data sheet parameters. Operation beyond the absolute maximum ratings can result in catastrophic failures.

The next section provides a table of *electrical characteristics over full ranges of recommended operating conditions* (e.g., input and output currents, output voltages, etc.). These are presented as minimum, typical, and maximum values. Typical values are representative of operation at an ambient temperature of T_A = 25°C with all power supply voltages at nominal value. Next, input and output capacitances are presented. Each pin has a capacitance (whether an input, an output, or control pin). Minimum capacitances are not given, as the typical and maximum values are the most crucial.

The next few tables involve the device timing characteristics. The parameters are presented as minimum, typical (or nominal), and maximum. The *timing requirements over recommended supply voltage range and operating free-air temperature* indicate the device control requirements such as hold times, setup times, and transition times. These values are referenced to the relative positioning of signals on the timing diagrams, which follow. The *switching characteristics over recommended supply voltage range* are device performance characteristics inherent to device operation once the inputs are applied. These parameters are guaranteed for the test conditions given. The interrelationship of the timing requirements to the switching characteristics is illustrated in *timing diagrams* for each type of memory cycle (e.g., read, write, program.)

At the end of a data sheet additional *applications information* may be provided such as how to use the device, graphs of electrical characteristics, or other data on electrical characteristics.

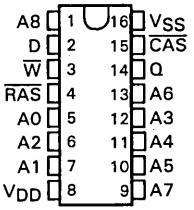
MAY 1983—REVISED JANUARY 1988

- 262,144 × 1 Organization
- Single 5-V Power Supply
  - 5% Tolerance Required for TMS4256-8
  - 10% Tolerance Required for TMS4256-10, -12, -15, and TMS4257-10, -12, -15
- JEDEC Standardized Pinouts
- Performance Ranges:

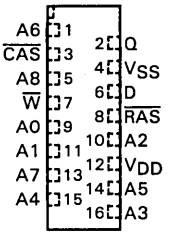
DEVICE	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	V_{DD} TOLERANCE
'4256-8	80 ns	40 ns	160 ns	± 5%
'4256-10 '4257-10	100 ns	50 ns	200 ns	±10%
'4256-12 '4257-12	120 ns	60 ns	220 ns	±10%
'4256-15 '4257-15	150 ns	75 ns	260 ns	±10%

- Long Refresh Period . . . 4 ms (Max)
- Operations of the TMS4256/TMS4257 Can Be Controlled by TI's SN74ALS2967, SN74ALS2968, and THCT4502 Dynamic RAM Controllers
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Outputs
- Common I/O Capability with "Early Write" Feature
- Page Mode ('4256) or Nibble-Mode ('4257)
- Low Power Dissipation
- $\overline{RAS}$-Only Refresh Mode
- Hidden Refresh Mode
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Mode
- Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), or S(−55°C to 100°C) Temperature Ranges (SMJ4256, with 10% Power Supply)

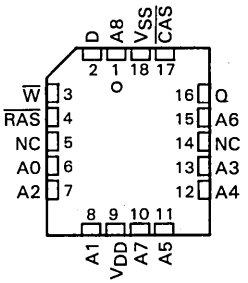
N PACKAGE
(TOP VIEW)



SD PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4256 and TMS4257 are high-speed, 262,144-bit dynamic random-access memories, organized as 262,144 words of one bit each. They employ state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The '4256-8 with a 5% voltage tolerance has a maximum $\overline{RAS}$ access time of 80 ns. The '4256/'4257-10, -12, and -15 with 10% voltage tolerances have maximum $\overline{RAS}$ access times of 100 ns, 120 ns, and 150 ns, respectively.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 125 mA typical, and a −1 V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The '4256 and '4257 are offered in 16-pin plastic dual-in-line, 16-pin plastic zig-zag in-line (ZIP), and 18-lead plastic chip carrier packages. They are guaranteed for operation from 0 °C to 70 °C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a read-modify-write cycle, the output will follow the sequence for the read cycle.

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refresh

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

The $\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}) and holding it low after $\overline{RAS}$ falls (see parameter t_{RLCHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

hidden refresh

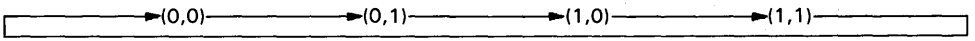
Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The external address is also ignored during the hidden refresh cycles. The data at the output pin remains valid up to the maximum $\overline{CAS}$ low pulse duration, $t_{w(CL)}$.

page mode (TMS4256)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe sequential row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by $t_{w(RL)}$, the maximum $\overline{RAS}$ low pulse duration.

nibble mode (TMS4257)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling $\overline{CAS}$ while $\overline{RAS}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of $\overline{CAS}$ will access the next bit of the circular 4-bit nibble in the following sequence:

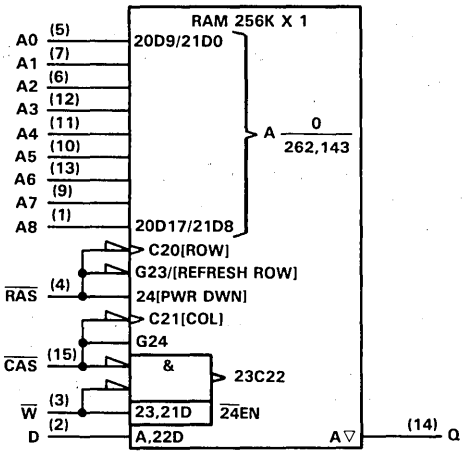


In nibble-mode, all normal memory operations (read, write, or read-modify-write) may be performed in any desired combination.

power-up

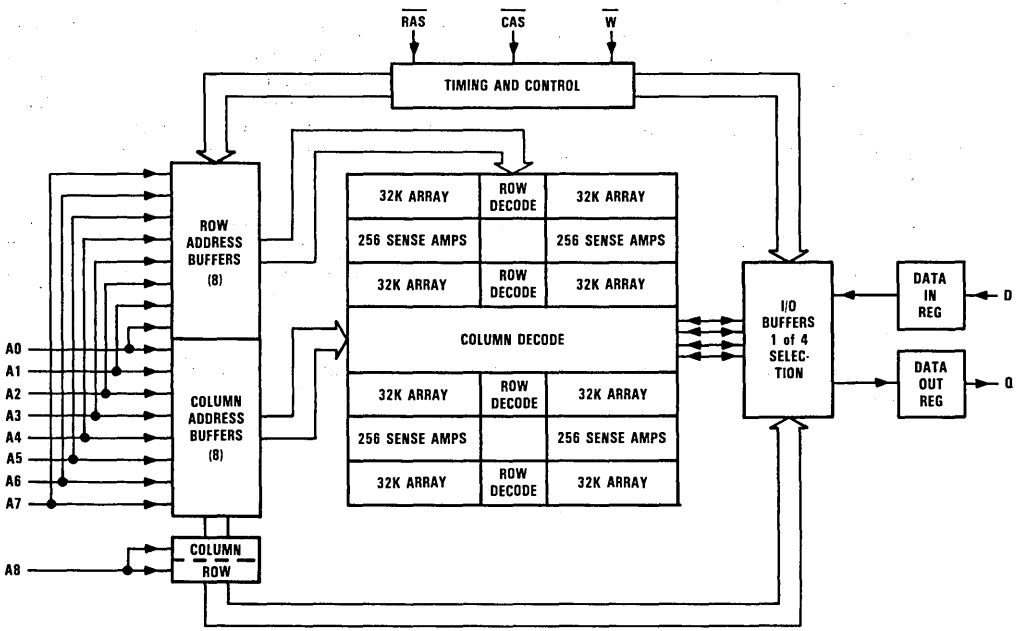
To achieve proper device operation, an initial pause of 200 μs is required after power up, followed by a minimum of eight initialization cycles.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1084 and IEC Publication 617-12.
The pin numbers shown are for the 16-pin dual-in-line package.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin, including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage ('4256/'4257-10, -12, -15)	4.5	5	5.5	V
V_{DD}	Supply voltage ('4256-8)	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4256-8		TMS4256-10 TMS4257-10		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V to 6.5 V		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high		±10		±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, Output open		70		70	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		4.5		4.5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, Output open		70		58	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		60		50	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open				45	mA

PARAMETER		TEST CONDITIONS	TMS4256-12 TMS4257-12		TMS4256-15 TMS4257-15		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V to 6.5 V		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high		±10		±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, Output open		65		60	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		4.5		4.5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, Output open		53		48	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		45		40	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		40		35	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

	PARAMETER	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	5	pF
$C_{i(D)}$	Input capacitance, data input	5	pF
$C_{i(RC)}$	Input capacitance strobe inputs	5	pF
$C_{i(W)}$	Input capacitance, write enable input	7	pF
C_o	Output capacitance	7	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

	PARAMETER	TEST CONDITIONS	ALT. SYMBOL	TMS4256-8		TMS4256-10 TMS4257-10		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		40		50	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		80		100	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	20	0	30	ns

	PARAMETER	TEST CONDITIONS	ALT. SYMBOL	TMS4256-12 TMS4257-12		TMS4256-15 TMS4257-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	30	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS4256-8		TMS4256-10 TMS4257-10		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	70		100		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	95		135		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	160		200		ns
$t_{c(W)}$	Write cycle time	t_{WC}	160		200		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	185		235		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	20		40		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	40	10,000	50	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	70		90		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	80	10,000	100	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	20		30		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	20		30		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	20		30		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	15		15		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	55		65		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	20		30		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	60		80		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	20		30		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	20		30		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	65		80		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

PARAMETER		ALT. SYMBOL	TMS4256-8		TMS4256-10 TMS4257-10		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	80		100		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	40		50		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	20		20		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	10		10		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	0		0		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	40		50		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	40	25	50	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	80		100		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

PARAMETER		ALT. SYMBOL	TMS4256-12 TMS4257-12		TMS4256-15 TMS4257-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	120		145		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	160		190		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	260		305		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	50		60		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	60	10,000	75	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	90		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	30		45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	35		45		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	35		45		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		25		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	80		100		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	30		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	90		120		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	30		45		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	30		45		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	90		120		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

PARAMETER		ALT. SYMBOL	TMS4256-12 TMS4257-12		TMS4256-15 TMS4257-15		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		75		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	25		30		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	10		20		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	0		0		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	60		70		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	60	25	75	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	120		145		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

NIBBLE-MODE CYCLE

switching characteristics over recommended supply voltage range and operating free-air temperature range

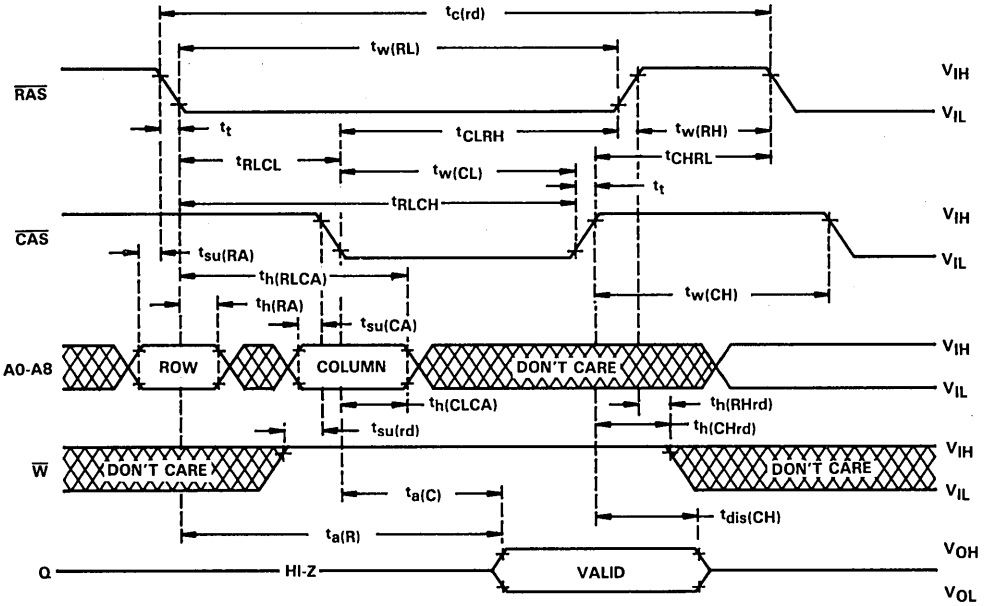
PARAMETER		ALT. SYMBOL	TMS4257-10		TMS4257-12		TMS4257-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CN)}$	Nibble-mode access from $\overline{CAS}$	t_{NCAC}		25		30		40	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS4257-10		TMS4257-12		TMS4257-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(N)}$	Nibble-mode cycle time	t_{NC}	50		60		75		ns
$t_{c(rdWN)}$	Nibble-mode read-modify-write cycle time	t_{NRMW}	70		85		105		
t_{CLRHN}	Nibble-mode delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{NRSH}	25		30		40		
t_{CLWLN}	Nibble-mode delay time, $\overline{CAS}$ to $\overline{W}$ delay	t_{NCWD}	20		25		30		
$t_{w(CLN)}$	Nibble-mode pulse duration, $\overline{CAS}$ low	t_{NCAS}	25		30		40		
$t_{w(CHN)}$	Nibble-mode pulse duration, $\overline{CAS}$ high	t_{NCP}	15		20		25		
$t_{su(WCHN)}$	Nibble-mode write command setup before $\overline{CAS}$ high	t_{NCWL}	20		25		35		

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

read cycle timing



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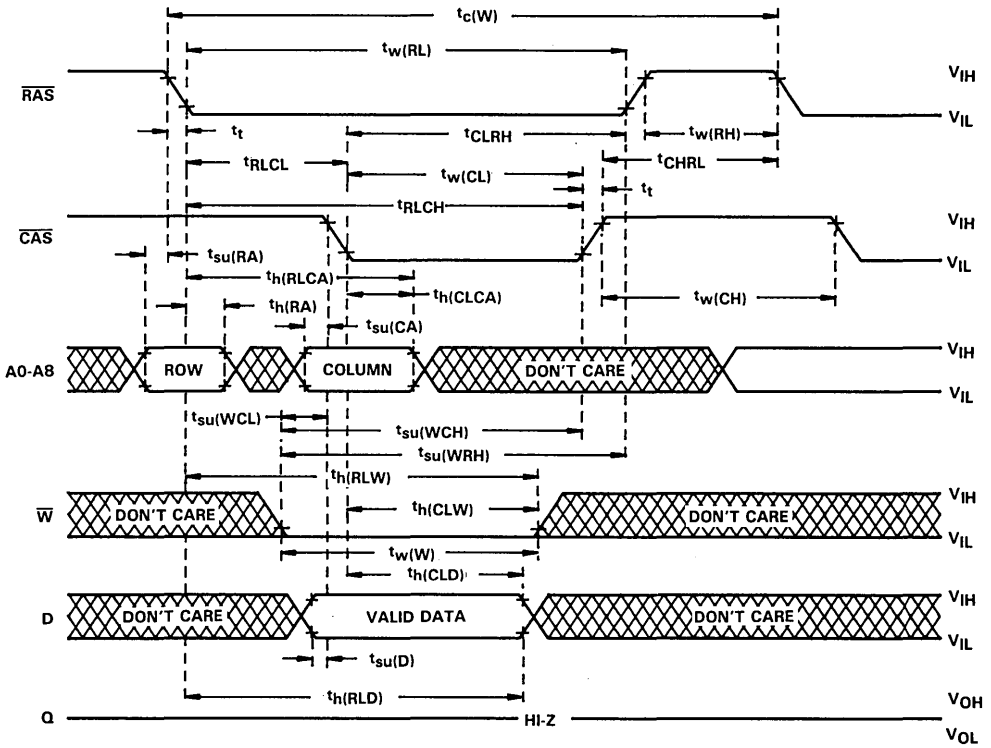
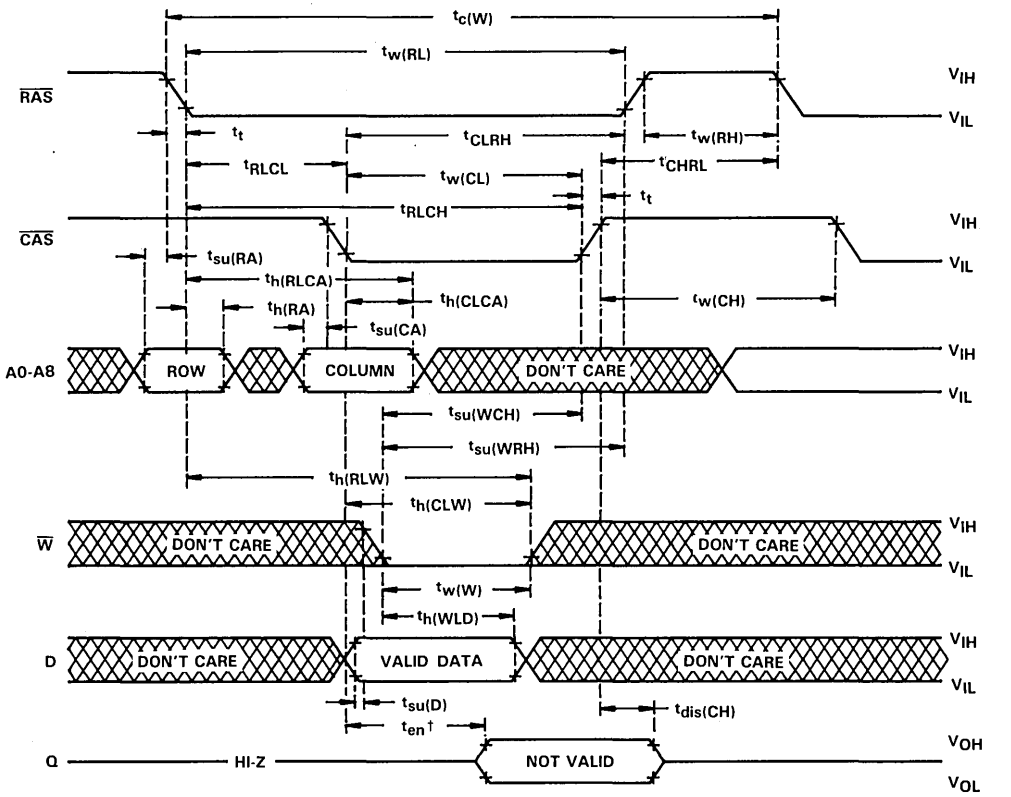
early write cycle timing

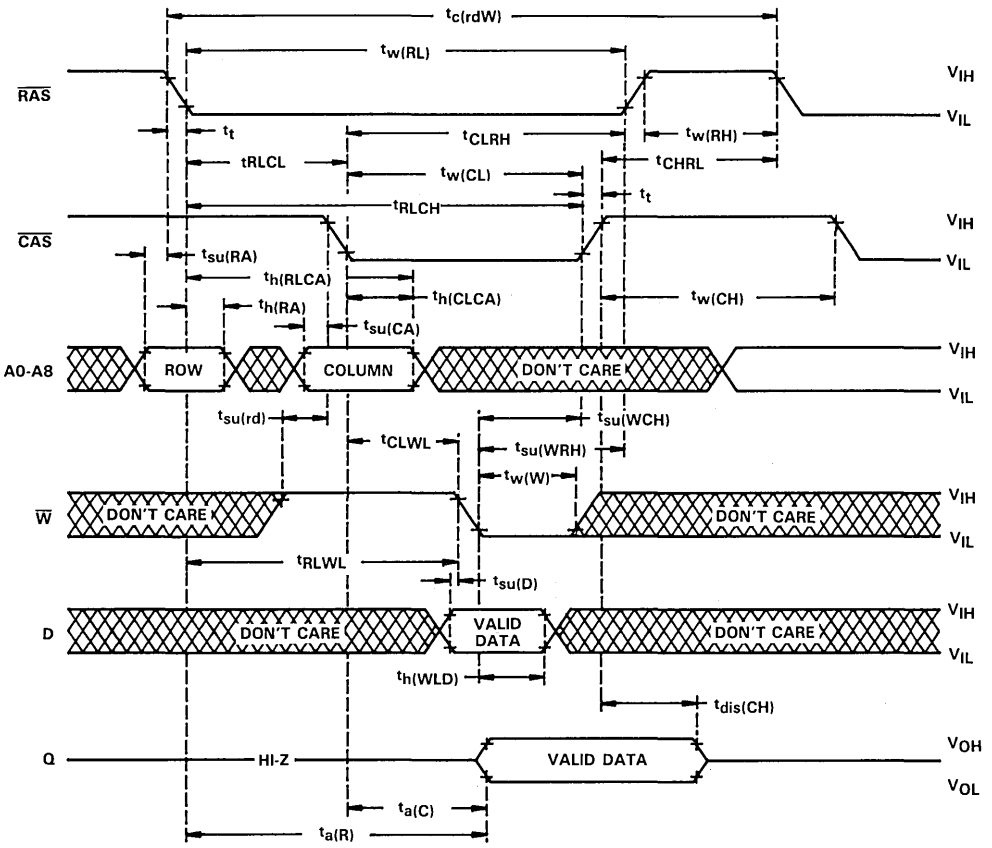


write cycle timing

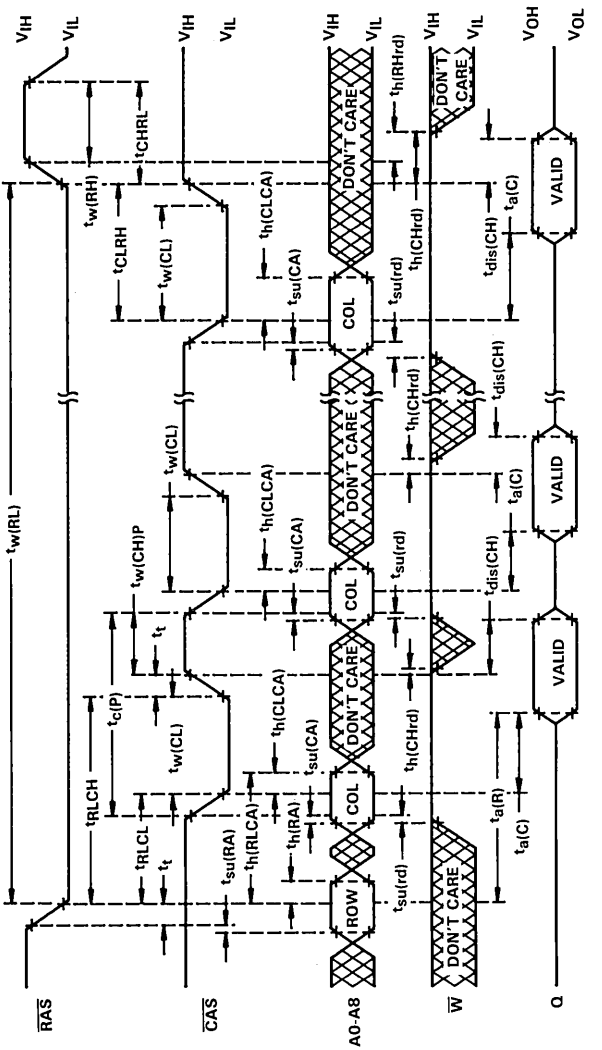


†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-write/read-modify-write cycle timing

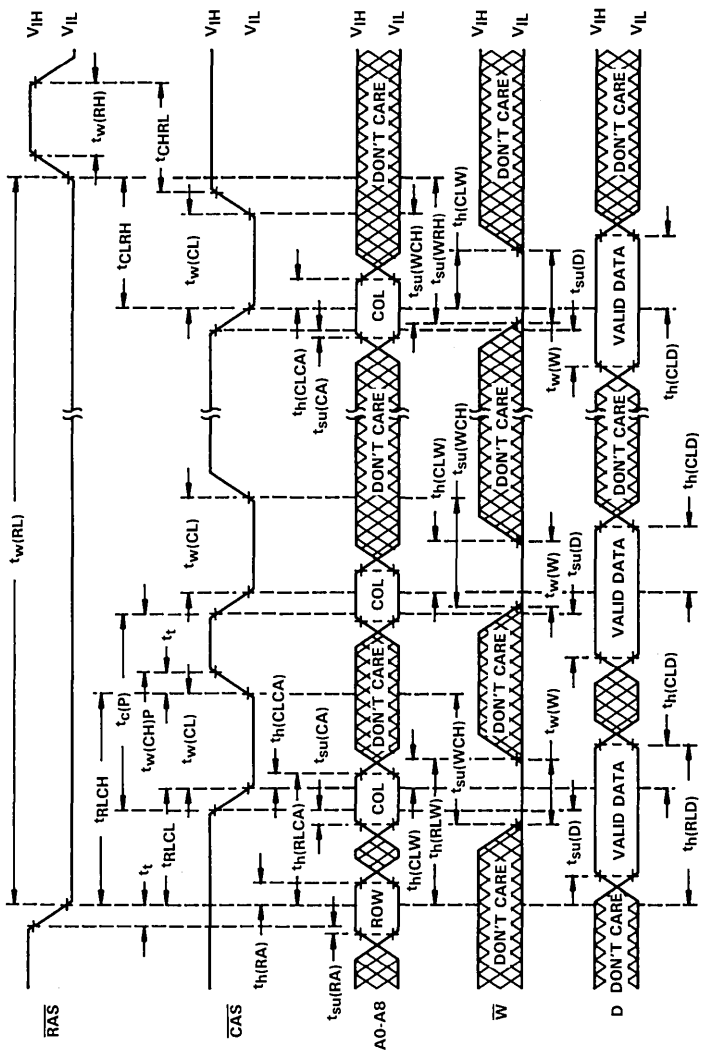


page-mode read cycle timing



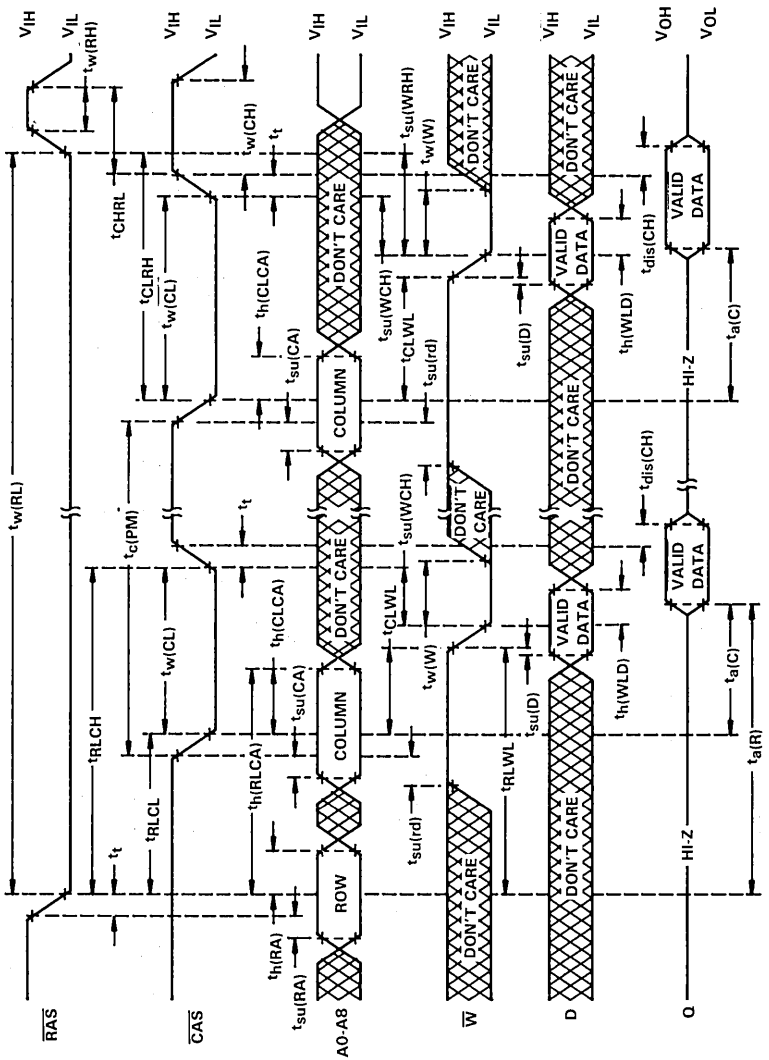
NOTE 4: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



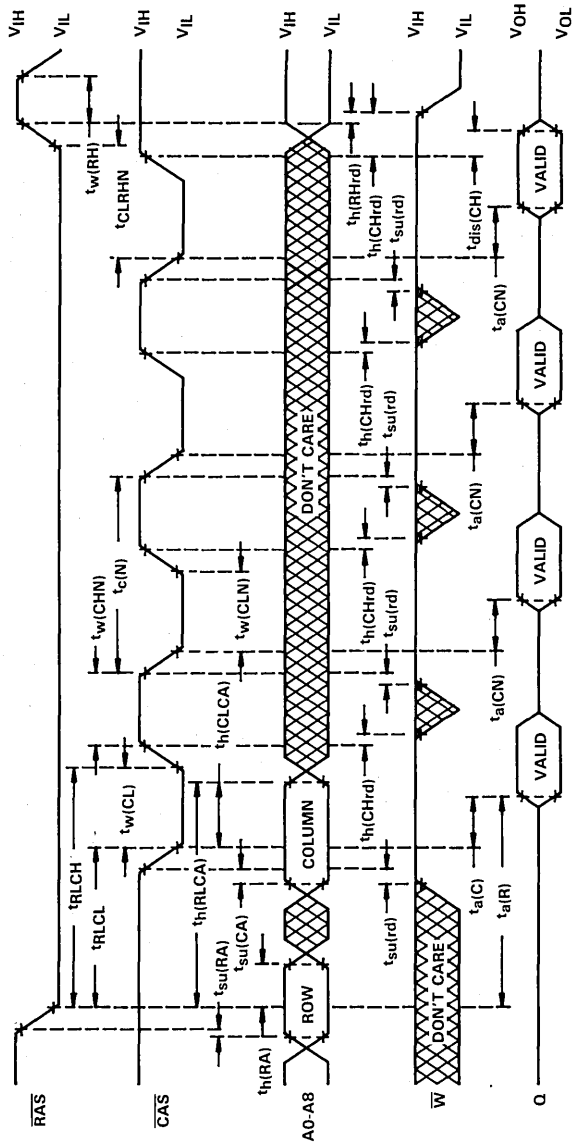
NOTE 5: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

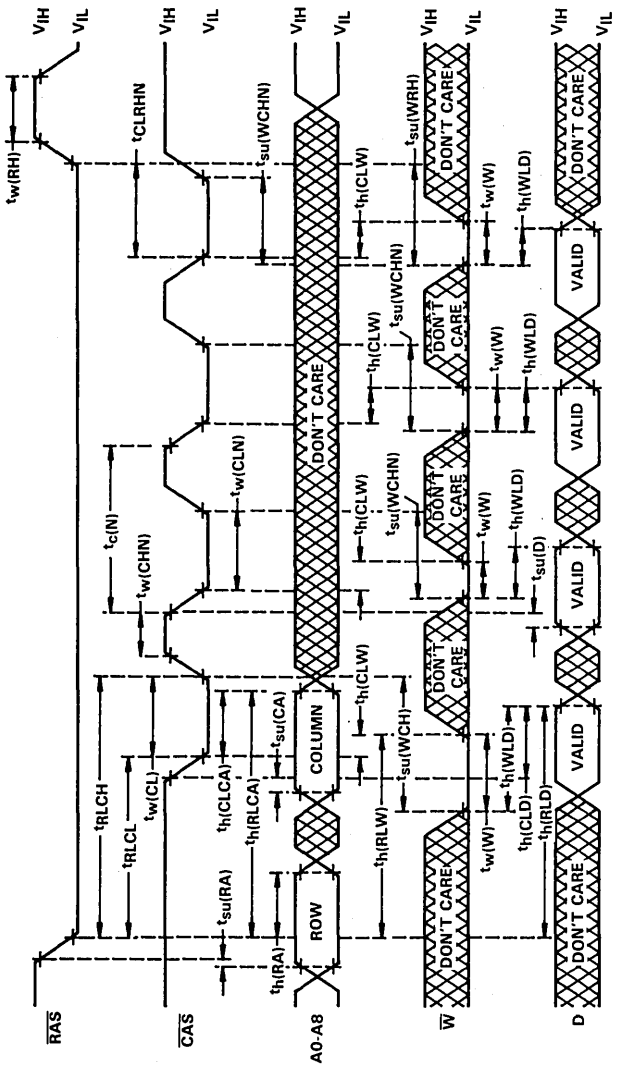


NOTE 6: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

nibble-mode read cycle timing



nibble-mode write cycle timing



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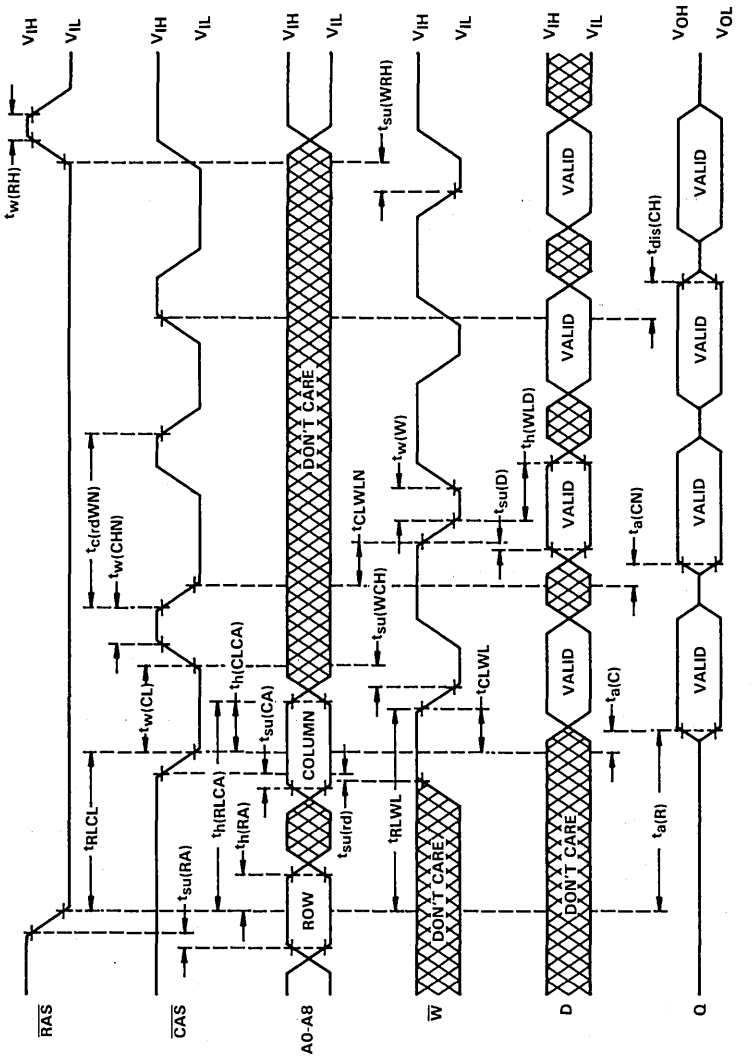
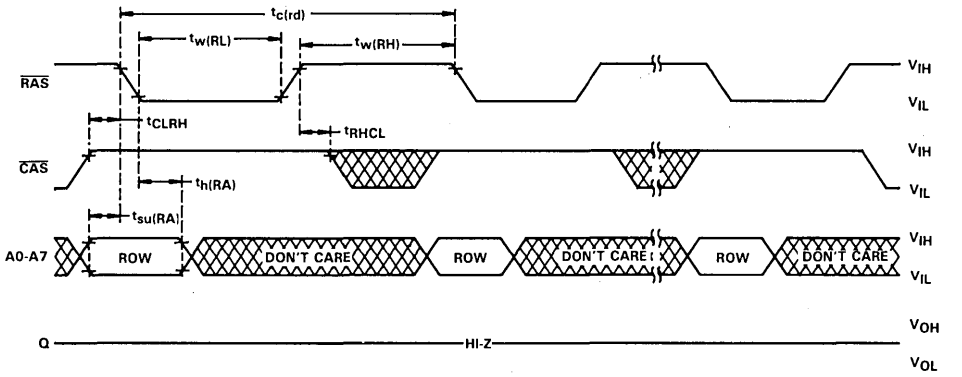
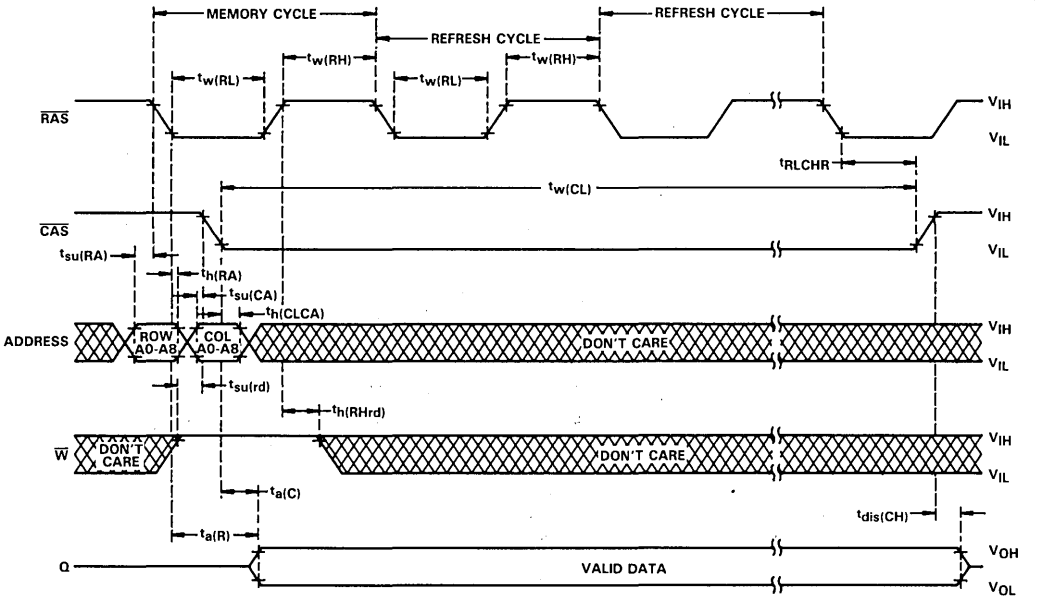
nibble-mode read-modify-write-cycle timing



RAS-only refresh cycle timing



hidden refresh cycle timing



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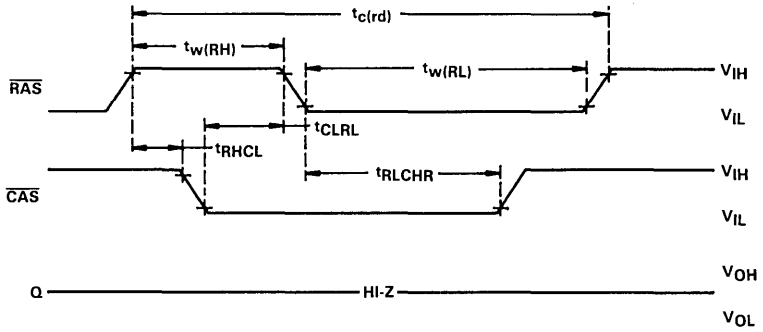
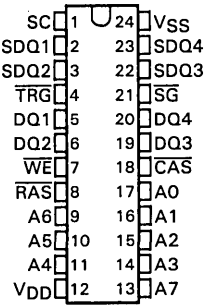
automatic ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$) refresh cycle timing



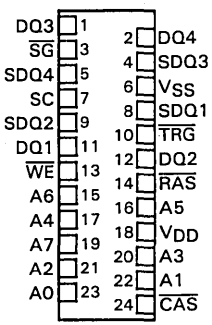
JULY 1986—REVISED FEBRUARY 1988

- 65,536 × 4 Organization
- Dual-Port Accessibility — Four I/Os for Sequential Access, Four I/Os for Random Access
- One Serial Data Register Built into Each Serial I/O for Sequential-Access Applications
- Designed for Video and Non-Video Applications
- Fast Serial Ports . . . 25-MHz Shift Rate
- Mid-Scan Load — Serial Data Streams Uninterrupted by Register Reload
- $\overline{TRG}$ as Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Random-Access Port Is Compatible with the TMS4464, 64K × 4 DRAM
- Supported by TI's TMS34061 Video System Controller and TMS34010 Graphics System Processor (GSP)
- 3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams
- Maximum Access Time from $\overline{RAS}$ . . . 120 ns
- Minimum Cycle Time (Read or Write) . . . 220 ns
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Random-Access Outputs
- Common Random-Access I/O Capability with "Early Write" Feature
- High-Speed Page-Mode Operation for Faster Access

N PACKAGE
(TOP VIEW)



SD PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Random-Access Data In/ Data-Out/Write-Mask Bit
$\overline{RAS}$	Row-Address Strobe
SC	Serial Data Clock
SDQ1-SDQ4	Serial Data In/Data Out
$\overline{SG}$	Serial Enable
$\overline{TRG}$	Transfer Register/ Q Output Enable
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{WE}$	Write-Mask Select/ Write Enable

- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh and Hidden Refresh Modes
- Low-Power Dissipation
- 24-Pin, 400-Mil Dual-in-line Package or 24-Pin, Zig-Zag In-line Package (ZIP)

description

The TMS4461 is a high-speed dual-ported 65,536×4 bit dynamic random-access memory with on-chip data registers. The random-access port makes the memory look as if it is organized as 65,536 words of four bits each, like the TMS4464. The sequential-access port is interfaced to four internal 256-bit dynamic data registers, which make the memory look as if it is organized as 256 four-bit words of up to 256 bits each that are accessed serially.

The 256K Multiport Video RAM employs state-of-the-art scaled NMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The TMS4461 features full asynchronous dual-port accessibility except when transferring data between the data register and the random-access memory.

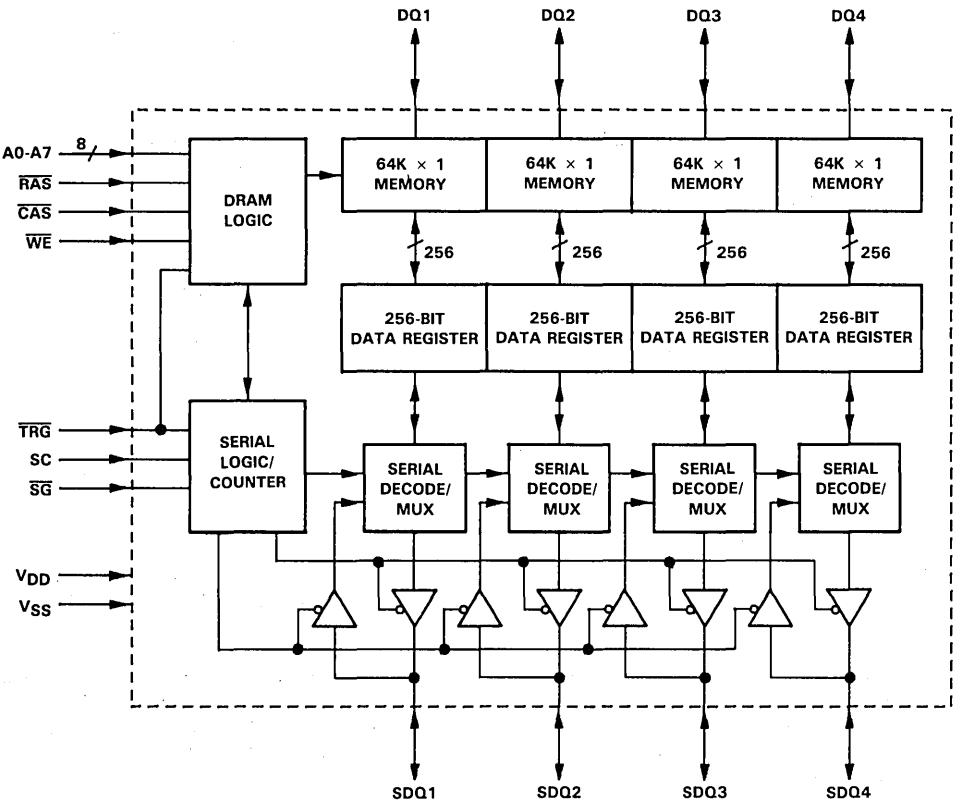
Refresh period is 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. Note that the transfer of a row of data from the memory array to the data register also refreshes that particular row. $\overline{CAS}$-before-$\overline{RAS}$ and hidden refresh modes are also available.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on-chip to simplify system design. All data outs are unlatched to allow greater system flexibility.

The 256K Multiport Video RAM is offered in a 24-pin dual-in-line plastic package (N suffix) and is guaranteed for operation from 0°C to 70°C. The package is designed for insertion in mounting-hole rows on 10,16-mm (400-mil) centers.

The TMS4461 Multiport Video RAM is also offered in a 24-pin zig-zag plastic package (SD suffix), guaranteed for operation from 0°C to 70°C.

functional block diagram



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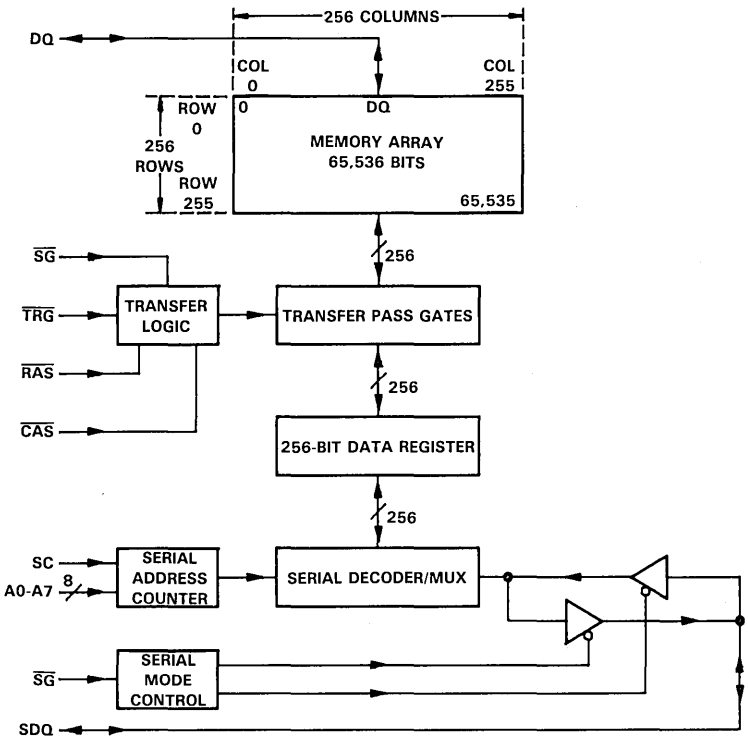
random port to serial port interface

The TMS4461 Multiport Video RAM consists of a 64K × 4 DRAM port and a 256 × 4 serial port. Each of the four random (DRAM) I/Os is interfaced to a 256-bit data register that can be loaded with 256 bits in parallel from any row in that I/O channel's memory then read out sequentially starting from one of 256 selectable locations along the data register. Conversely, each of the four data registers can be loaded with data serially from the serial input (SD) and subsequently transferred, 256 bits in parallel, into any row of memory for each respective DRAM I/O channel.

block diagram showing one random and serial interface



random-access address space to sequential-address space mapping

The 256 bits in each of the four data registers correspond to the 256 column locations of each of the four random I/Os. Data can be read out of the registers starting at any of the 256 data register bit locations.

This tap location is selected by addresses A7 through A0 on the falling edge of $\overline{CAS}$ during a transfer cycle between the memory array and the data registers. All registers are read out starting from the selected tap point proceeding from the least-significant bits to the most-significant bits. The four data registers are configured as circular data registers when reading their contents to the serial outputs. After the most-significant bit (bit 255) is read out of each register, the next bit read will be 00 (see explanation under section entitled "serial data input/output").

Note that if column address bits A7 through A0 equal 00 during the last memory-to-register transfer cycle, a total of 256 bits can be sequentially read out of each of the four data registers starting from bit position 00.

operation

random-access operation

transfer register select ($\overline{TRG}$)

The $\overline{TRG}$ selects either register transfer or random-access operation as $\overline{RAS}$ falls. To use the TMS4461 in random-access mode, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. Holding $\overline{TRG}$ high as $\overline{RAS}$ falls causes the 256 storage elements of each data register to remain disconnected from the corresponding 256 bit lines of the memory array. If serial data is to be written in or read out of the data registers, the data registers must be disconnected from the bit lines. Holding $\overline{TRG}$ low as $\overline{RAS}$ falls enables the 256 switches that connect the data registers to the bit lines and indicates that a transfer will occur between the data registers and the selected memory row.

random output enable ($\overline{TRG}$)

During random-access operations, $\overline{TRG}$ functions as an output enable for the random outputs after the read access times have been satisfied (if this is a read cycle). Whenever $\overline{TRG}$ is held high, the Q outputs will be in the high-impedance state. This feature removes the possibility of an overlap between data on the address lines and data appearing on the Q outputs making it possible to connect the address lines to the data I/O lines—although use of this organization prohibits the use of the early write cycle. It also allows read-modify-write cycles to be performed by providing a three-state condition to the common I/O pins to allow write data to be driven onto the pins after output read data has been externally latched.

address (A0 through A7)

Sixteen address bits are required to decode one of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip on the falling edge of $\overline{RAS}$. Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip on the falling edge of $\overline{CAS}$. All row and column addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$ respectively. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the device input and output buffers. $\overline{CAS}$ is also used to strobe the column address into the memory.

write-mask enable ($\overline{WE}$)

The $\overline{WE}$ pin selects the random-mode write-mask option. The TMS4461 random port is equipped with two modes of write operations. If $\overline{WE}$ is held low on the falling edge of $\overline{RAS}$ (during a random access operation), the write mask is enabled. Accordingly, a 4-bit binary code (the mask) is input to the device via the random DQ pins and is also latched on the falling edge of $\overline{RAS}$. This binary pattern determines which of the four DRAM I/Os will be written into on that access and which DRAM I/Os will not. Thus, after $\overline{RAS}$ has latched the write mask on chip, input data is driven onto the DQ pins and is latched on the falling edge of the latter of $\overline{CAS}$ or $\overline{WE}$ (for early write operation, $\overline{WE}$ can remain low for the entire $\overline{RAS}$ low period). If a 0 was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, then the write circuits for that particular I/O will be defeated and data will not be written to that I/O. If a 1 was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, then the write circuits for that particular I/O will not be defeated and data will be written to that I/O. See the corresponding timing diagrams for details.

Important: The mask operation is selected only if $\overline{WE}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{WE}$ is held high on the falling edge of $\overline{RAS}$ the mask is not enabled and the write operation is identical to standard ×4 DRAMs, with all four I/Os being written by the data appearing on the DQ pins when the latter of $\overline{WE}$ or $\overline{CAS}$ is brought low. Thus, if it is not desired to use the mask function, then a standard DRAM timing interface can be used.

WRITE MASK FUNCTION TABLE

$\overline{TRG}$	$\overline{WE}$	DQ1-DQ4	MODE
1	1	X	Write enabled at DQ1-DQ4
1	0	1	Write to DQ enabled
1	0	0	Write to DQ disabled

NOTE 1: The logic states in the table above are assumed valid on the falling edge of $\overline{RAS}$.

write enable ($\overline{WE}$)

The read or write mode is selected through the write-enable ($\overline{WE}$) input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle.

data I/O (DQ1-DQ4)

Memory data is written during a write or read-modify-write cycle. The falling edge of $\overline{WE}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low. Thus, the data will be strobed in by $\overline{WE}$ with data setup and hold times referenced to this signal. The three-state output buffers provide direct TTL compatibility (no pull-up resistors required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state as long as $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low.

Once the outputs are valid, they will remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ or $\overline{TRG}$ going high will return the outputs to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle. In a register-transfer operation (memory-to-register or register-to-memory), the outputs remain in the high impedance state for the entire cycle, regardless of transitions on $\overline{CAS}$ or $\overline{TRG}$.

write mask bits (DQ1-DQ4)

When the write mask is enabled ($\overline{WE}$ low on the falling edge of $\overline{RAS}$), the write mask bits determine which DRAM I/Os are to be written and which of the DRAM I/Os will have their write operations internally defeated. The state of the write mask bits is latched on-chip on the falling edge of $\overline{RAS}$ and selectively controls the internal write enable circuits of each corresponding DRAM I/O. If the write mask is not enabled ($\overline{WE}$ high on the falling edge of $\overline{RAS}$), then no write enable circuits will be defeated and data appearing at the DQ1-DQ4 pins on the falling edge of $\overline{RAS}$ will be ignored. See timing diagrams and the table under "write mask enable ($\overline{WE}$)" for details.

refresh

A refresh operation must be performed to each row at least once every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power. Note that the data registers are dynamic storage elements and that the data held in the registers will be lost unless SC is clocked 2 times or else the data is reloaded from the memory array. See specifications for maximum register retention times.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}). The external row address is ignored and the refresh address is generated internally.

column-address strobe ($\overline{CAS}$)

The $\overline{CAS}$ input latches the column addresses on-chip and also functions as an output enable for DQ1-DQ4.

page mode

Page-mode operation allows faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by $t_{W(RL)}$, the maximum $\overline{RAS}$ low pulse duration.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles and one memory-to-register transfer cycle with an SC cycle following the rising edge of $\overline{TRG}$ before proper device operation is achieved.

sequential-access operation

transfer register select ($\overline{TRG}$)

Memory operations involving parallel use (i.e., transfer from memory to data register or data register to memory) of the data register are invoked by bringing $\overline{TRG}$ low with the address lines A0-A7 before $\overline{RAS}$ falls. This enables the switches connecting the 256 elements of each data register to the 256 bit lines of each DRAM I/O. The states of $\overline{WE}$ and $\overline{SG}$, which are also latched on the falling edge of $\overline{RAS}$, determine whether the 256-bit data transfer will be from the memory array to the data registers or from the data registers to memory array, as well as determining if the SDQs are in read or write mode (see "transfer operation logic table").

Note that the state of $\overline{TRG}$ is latched on the falling edge of $\overline{RAS}$ just like a row address, to select the mode of operation. During read or read-modify-write cycles, $\overline{TRG}$ functions as output enable after $\overline{CAS}$ falls.

transfer write enable ($\overline{WE}$)

In register transfer mode, $\overline{WE}$ determines whether a transfer will occur from the data registers to the memory array, or from the memory array to the data registers. To transfer data from the data registers to the memory array, $\overline{WE}$ and $\overline{SG}$ are held low as $\overline{RAS}$ falls. If $\overline{SG}$ were to be high during this transition, then no transfer of data from the data register to the memory array would occur, but the SDQs would be put into the write mode. This would allow serial data to be written into the register. To transfer from the memory array to the data registers, $\overline{WE}$ is held high and $\overline{SG}$ is a don't care as $\overline{RAS}$ falls. This cycle puts the SDQs into the read mode, thus allowing serial data to be read out of the data register. Note that $\overline{WE}$ and $\overline{SG}$ setup and hold times are referenced to the falling edge of $\overline{RAS}$ for this mode of operation (see "transfer operation logic table").

row address (A0 through A7)

Eight address bits are required to select one of the 256 possible rows involved in the transfer of data to or from the data registers. (The states of A0-A7, $\overline{WE}$, $\overline{TRG}$, and $\overline{SG}$ are latched on the falling edge of $\overline{RAS}$.)

register column address (A0 through A7)

To select one of the 256 positions along each of the four data registers from which the first serial data will be read out, or to which the first serial data will be written, the appropriate 8-bit column address (A0-A7) must be valid when $\overline{CAS}$ falls during the appropriate transfer cycle.

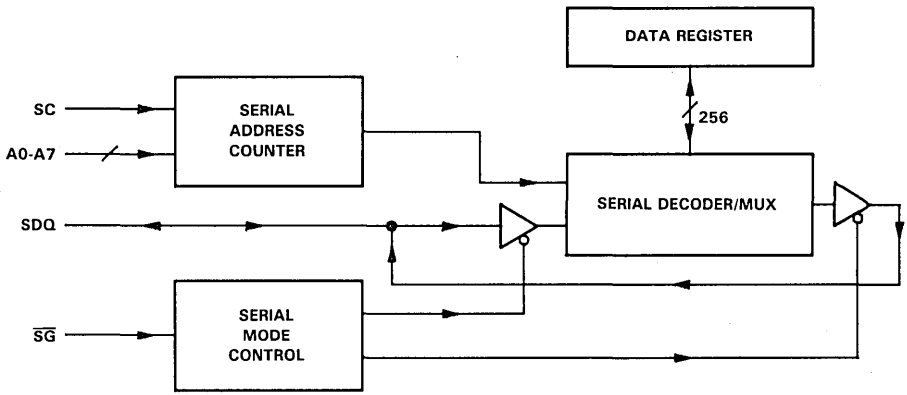
serial data clock (SC)

Data is written in or read out of the data registers on the rising edge of SC. This makes it possible to view the data registers as though they were made of 256 positive-edge-triggered D flip-flops which connect D to Q (not to be confused with the DQ random I/O pins of the TMS4461). The TMS4461 is designed to work with a wide range duty cycle clock to simplify system design.

serial data input/output (SDQ1-SDQ4)

SD and SQ share a common I/O pin. Data is written in when $\overline{SG}$ is low during write mode, and data is read out when $\overline{SG}$ is low during read mode (see "transfer operation logic table"). Note that when the serial address counter reaches its maximum value of 255, it is reset to 00 with the next positive transition of SC. This allows data to be read out in a continuous loop.

block diagram of one serial I/O



serial enable ($\overline{SG}$)

The serial enable pin has two functions. First, it is used on the falling edge of $\overline{RAS}$, with both $\overline{TRG}$ and $\overline{WE}$ low. If $\overline{SG}$ is low during this transition, then a register-to-memory transfer will occur. On the other hand, if $\overline{SG}$ were to be high as $\overline{RAS}$ falls, then a write-mode control cycle will be performed. The function of this cycle is to switch the SDQs from the output mode to the input mode, thus allowing serial data to be written into the data register. Second, $\overline{SG}$ is used as a SDQ enable/disable. In the write mode, $\overline{SG}$ is used as an input enable. $\overline{SG}$ high disables the input, and $\overline{SG}$ low enables the input. To take the device out of the write mode and into the read mode, a memory-to-register transfer cycle must be performed. The read mode allows data to be read out of the data register. $\overline{SG}$ high disables the output and $\overline{SG}$ low enables the output. Note that the serial address counter will be incremented on each SC cycle regardless of the state of $\overline{SG}$.

TRANSFER OPERATION LOGIC TABLE

$\overline{TRG}$	$\overline{WE}$	$\overline{SG}$	MODE
0	0	0	Register to memory transfer and write-mode enable
0	0	1	Write-mode enable
0	1	X	Memory-to-register transfer

NOTE 2: The logic states in the table above are assumed valid on the falling edge of $\overline{RAS}$. In a serial write-mode to read-mode sequence, the first positive transition of SCLK after the memory-to-register transfer will change the SDQs from three-state to output mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V_{DD} and data out (see Note 3) . . . . . −1 to 7 V
Voltage range for V_{DD} supply with respect to V_{SS} . . . . . −1 to 7 V
Voltage range for data out with respect to V_{SS} . . . . . −1 to V_{DD} + 0.3 V
Short circuit output current per output . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 3: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 4)	−1		0.8	V
T_A	Operating free-air temperature	0	25	70	°C

NOTE 4: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4461-12		TMS4461-15		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V		±10		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V		±10		±10	μA
I_{DD1}	Average operating current during read, write, or transfer cycle (serial port in standby)	Minimum cycle time, No load on DQ and SDQ pins		80		70	mA
I_{DD2}	Standby current (total, both ports)	After 1 memory cycle, $\overline{RAS}$, $\overline{CAS}$, SC, and $\overline{SG}$ ≥ 2.4 V, No load on DQ and SDQ pins		25		25	mA
I_{DD3}	Average refresh current	Minimum cycle time, $\overline{RAS}$ ≤ 0.8 V, $\overline{CAS}$ ≥ 2.4 V, No load on DQ and SDQ pins		75		65	mA
I_{DD4}	Average page-mode current (serial port in standby)	Minimum cycle time, $\overline{RAS}$ ≤ 0.8 V, $\overline{CAS}$ cycling, No load on DQ and SDQ pins		55		50	mA
I_{DD5}	Average current with memory array in standby and register shifting	$t_{c(SC)}$ = MIN, $\overline{RAS}$ and $\overline{CAS}$ ≥ 2.4 V, No load on DQ and SDQ pins		85		80	mA
I_{DD6}	Worst case average current	Minimum cycle time on both ports, No load on DQ and SDQ pins		155		140	mA

capacitance over recommended supply voltage and operating free-air temperature ranges, f = 1 MHz

	PARAMETER	MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		10	pF
$C_{i(WE)}$	Input capacitance, write enable input		10	pF
$C_{i(SC)}$	Input capacitance, serial clock		10	pF
$C_{i(SG)}$	Input capacitance, serial enable		5	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
C_o	Output capacitance		7	pF

switching characteristics over recommended supply voltage and operating free-air temperature ranges

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4461-12		TMS4461-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	Load = 2 Series 74 TTL gates, C_L = 100 pF, $t_{RLCL} \geq$ Max	t_{CAC}		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	Load = 2 Series 74 TTL gates, C_L = 100 pF, $t_{RLCL} \leq$ Max	t_{RAC}		120		150	ns
$t_{a(TRG)}$	Access time of DQ from $\overline{TRG}$ low	Load = 2 Series 74 TTL gates, C_L = 100 pF	t_{OEA}		35		40	ns
$t_{a(SC)}$	Access time of SQ fro SC high	Load = 2 Series 74 TTL gates, C_L = 50 pF	t_{SCA}		40		50	ns
$t_{a(SG)}$	Access time of SQ from $\overline{SG}$ low	Load = 2 Series 74 TTL gates, C_L = 50 pF	t_{SOA}		30		35	ns
$t_{dis(CH)}$	Random-output disable time from $\overline{CAS}$ high	Load = 2 Series 74 TTL gates, C_L = 15 pF	t_{OFF}	0	20	0	25	ns
		Load = 2 Series 74 TTL gates, C_L = 100 pF		0	25	0	30	ns
$t_{dis(TRG)}$	Random-output disable time from $\overline{TRG}$ high	Load = 2 Series 74 TTL gates, C_L = 15 pF	t_{OEZ}	0	20	0	25	ns
		Load = 2 Series 74 TTL gates, C_L = 100 pF		0	25	0	30	ns
$t_{dis(SG)}$	Serial-output disable time from $\overline{SG}$ high	Load = 2 Series 74 TTL gates, C_L = 15 pF	t_{SOZ}	0	15	0	20	ns
		Load = 2 Series 74 TTL gates, C_L = 50 pF		0	20	0	25	ns

timing requirements over recommended supply voltage and operating free-air temperature ranges

		ALT. SYMBOL	TMS4461-12 MIN	TMS4461-12 MAX	TMS4461-15 MIN	TMS4461-15 MAX	UNIT
$t_{c(rd)}$	Read cycle time†	t_{RC}	220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	295		345		ns
$t_{c(Trd)}$	Transfer read cycle time	t_{RC}	220		260		ns
$t_{c(TW)}$	Transfer write cycle time	t_{WC}	220		260		ns
$t_{c(P)}$	Page-mode read or write cycle time	t_{PC}	120		145		ns
$t_{c(rdWP)}$	Page-mode read-write/read-modify-write cycle time	t_{RWC}	195		230		ns
$t_{c(SC)}$	Serial clock cycle time	t_{SCC}	40	50,000	50	50,000	ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ duration (precharge time)	t_{CP}	50		60		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	60	10,000	75	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	90		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low §	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	30		45		ns
$t_{w(SCL)}$	Pulse duration, SC low	t_{SCL}	10		10		ns
$t_{w(SCH)}$	Pulse duration, SC high	t_{SCH}	10		10		ns
$t_{w(TRG)}$	$\overline{TRG}$ pulse duration low time	t_{OE}	35		40		ns
t_t	Transition times (rise and fall)	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(RW)}$	$\overline{WE}$ setup time before $\overline{RAS}$ low with $\overline{TRG}$ low (register transfer cycles)	t_{WS}	0		0		ns
$t_{su(DQ)}$	DQ setup time before $\overline{RAS}$ low with $\overline{TRG}$ high (random access, write mask select)	t_{DTS}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	35		45		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	35		45		ns
$t_{su(SD)}$	Serial data setup time before SC high	t_{SDS}	0		0		ns
$t_{su(TRG)}$	$\overline{TRG}$ setup time before $\overline{RAS}$ low	t_{TSR}	0		0		ns
$t_{su(SG)}$	$\overline{SG}$ setup time before $\overline{RAS}$ low with $\overline{TRG}$ and $\overline{WE}$ low	t_{ESR}	0		0		ns
$t_{su(WM)}$	$\overline{WE}$ setup time before $\overline{RAS}$ low (write mask select)	t_{RWS}	0		0		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		25		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		15		ns
$t_{h(RW)}$	$\overline{WE}$ hold time after $\overline{RAS}$ low with $\overline{TRG}$ low (transfer cycles)	t_{WH}	15		15		ns

Continued next page.

NOTE 5: Timing measurements referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended supply voltage and operating free-air temperature ranges (continued)

			ALT. SYMBOL	TMS4461-12 MIN	TMS4461-12 MAX	TMS4461-15 MIN	TMS4461-15 MAX	UNIT
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low		t_{AR}	80		100		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low		t_{DH}	30		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low		t_{DHR}	90		120		ns
$t_{h(WLD)}$	Data hold time after $\overline{WE}$ low		t_{DH}	30		45		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high		t_{RCH}	0		0		ns
$t_{h(RDrd)}$	Read-command hold time after $\overline{RAS}$ high		t_{RRH}	10		10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low		t_{WCH}	30		45		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low		t_{WCR}	90		120		ns
$t_{h(WQE)}$	$\overline{TRG}$ hold time after $\overline{WE}$ low		t_{OEH}	30		40		ns
$t_{h(SD)}$	Serial data-in hold time after SC high		t_{SDH}	15		15		ns
$t_{h(SQ)}$	Serial data-out hold time after SC high		t_{SOH}	8		8		ns
$t_{h(TRG)}$	$\overline{TRG}$ hold time after $\overline{RAS}$ low		t_{TSH}	15		15		ns
$t_{h(DQ)}$	DQ hold time after $\overline{RAS}$ low with $\overline{TRG}$ high and $\overline{WE}$ low		t_{DTH}	15		15		ns
$t_{h(SG)}$	$\overline{SG}$ hold time after $\overline{RAS}$ low with $\overline{TRG}$ and $\overline{WE}$ low		t_{ESH}	15		15		ns
$t_{h(WM)}$	$\overline{WE}$ hold time after $\overline{RAS}$ low (write mask select)		t_{RWH}	15		15		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		t_{CRP}	0		0		ns
t_{CLGH}	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high		t_{OEHC}	60		75		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		t_{RSH}	60		75		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{WE}$ low (read-modify-write cycle only)‖		t_{CWD}	95		110		ns
t_{RLTH}	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (memory-to-register transfer cycle)	Early load#		25		25		ns
		Mid-line real-time load	t_{RDH}	80		100		
t_{RLSH}	Delay time, $\overline{RAS}$ low to the first positive transition of SC after $\overline{TRG}$ high (register transfer cycle)		t_{SCHR}	100		125		ns
t_{THRL}	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low after a transfer cycle		t_{RSLT}	$t_{w(RH)}$		$t_{w(RH)}$		ns
t_{CLSH}	Delay time, $\overline{CAS}$ low to the first positive transition of SC after $\overline{TRG}$ high (register transfer cycle)		t_{SCHC}	40		50		ns
t_{SHRL}	Delay time, SC high to $\overline{RAS}$ low with $\overline{TRG}$ and $\overline{WE}$ low (register-to-memory transfer cycle)☆		t_{RSLS}	40		50		ns
t_{SHTH}	Delay time, SC high to $\overline{TRG}$ high (memory-to-register transfer cycle)□		t_{SDD}	10		15		ns

Continued next page.

NOTE 5: Timing measurements are referenced to V_{IL} max and V_{IH} min.

‖ $\overline{TRG}$ must disable the output buffers prior to applying data to the device.

$\overline{TRG}$ may be brought high early during a memory-to-register transfer cycle as long as the $t_{h(TRG)}$, t_{SHTH}, and t_{RLSH} specifications are met.

☆ In a register-to-memory transfer cycle, the state of SC when $\overline{RAS}$ falls is a don't care condition. However, to guarantee proper sequencing of the internal clock circuitry there can be no positive transitions of SC for at least 40 ns prior to when $\overline{RAS}$ goes low. See the section entitled "sequential access operation" for a complete explanation of the transfer operation.

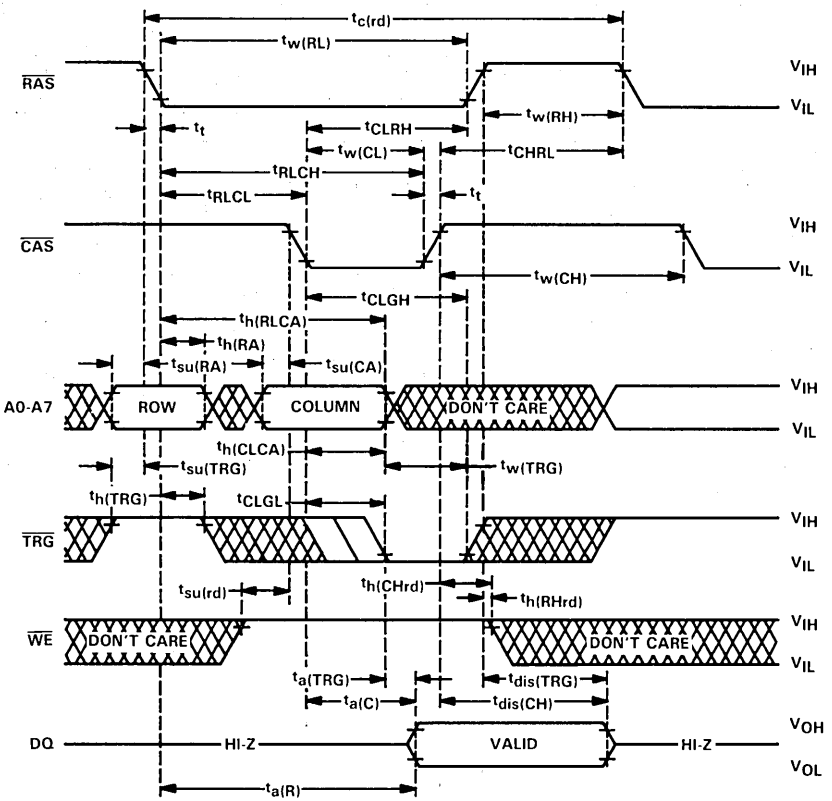
□ In a memory-to-register transfer cycle, the state of SC when $\overline{TRG}$ rises is a don't care condition. However, to guarantee proper sequencing of the internal clock circuitry there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high. See the section entitled "sequential access operation" for a complete explanation of the transfer operation.

timing requirements over recommended supply voltage and operating free-air temperature ranges (concluded)

		ALT. SYMBOL	TMS4461-12		TMS4461-15		UNIT
			MIN	MAX	MIN	MAX	
t_{THSH}	Delay time, $\overline{TRG}$ high to SC high (memory-to-register transfer cycle)	t_{SDH}	15		20		ns
t_{THRH}	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (memory-to-register transfer cycle)	t_{DTR}	0		0		ns
t_{THCH}	Delay time, $\overline{TRG}$ high to $\overline{CAS}$ high (register transfer cycles)	t_{DTC}	0		0		ns
t_{CLTH}	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high (memory-to-register transfer cycle)	t_{CDH}	20		25		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee $\overline{RAS}$ access time)	t_{RCD}	25	60	25	75	ns
t_{CLGL}	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ low (maximum value specified to guarantee column access time)	t_{DCT}		25		30	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{WE}$ low (read-modify-write cycle only)	t_{RWD}	155		185		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		20		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		25		ns
t_{SGSC}	Delay time, $\overline{SG}$ low to SC high during serial data-in shift cycle	t_{SWS}	10		10		ns
t_{GHD}	Delay time, $\overline{TRG}$ high before data applied at DQ	t_{GDD}	25		30		ns
$t_{rf(MA)}$	Refresh time interval, memory array	t_{REF1}		4		4	ms
$t_{rf(SR)}$	Refresh time interval, data register	t_{REF2}		4		4	ms

NOTE 5: Timing measurements are referenced to V_{IL} max and V_{IH} min.

read cycle timing



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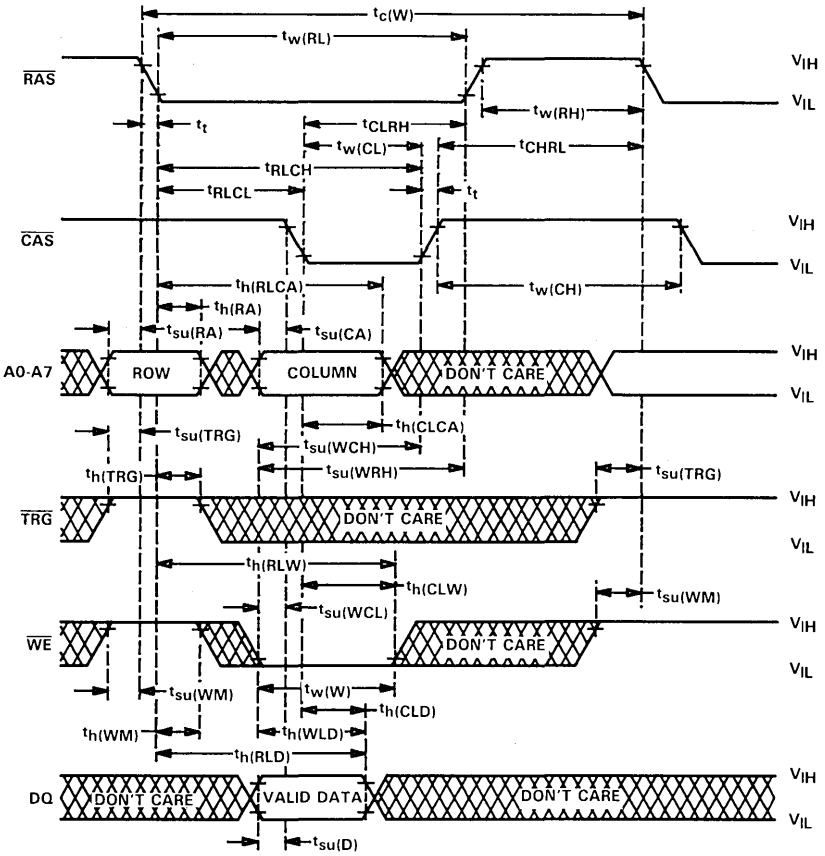
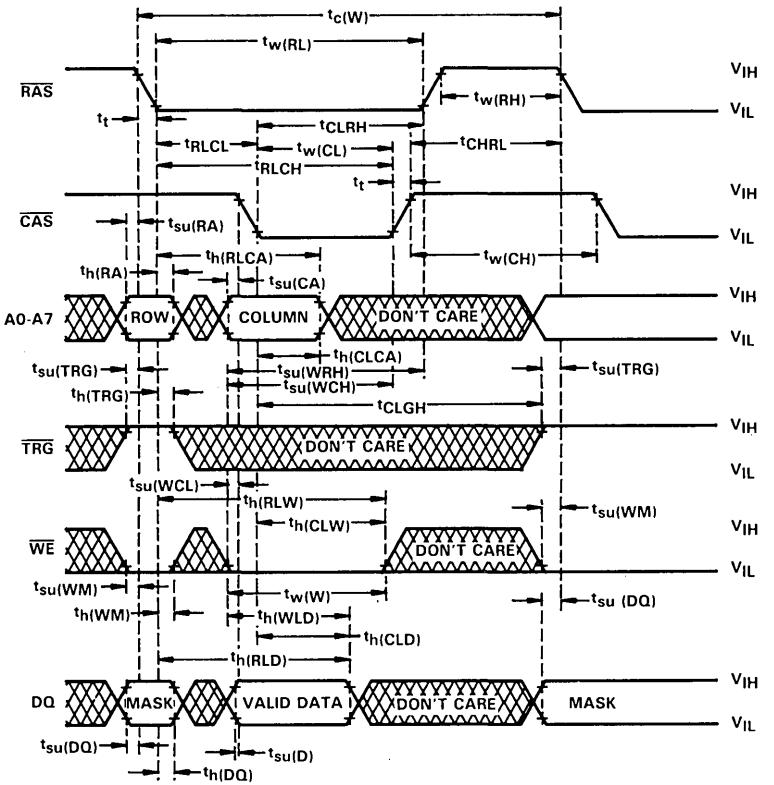
early write cycle timing, write mask unselected



early write cycle timing, write mask selected



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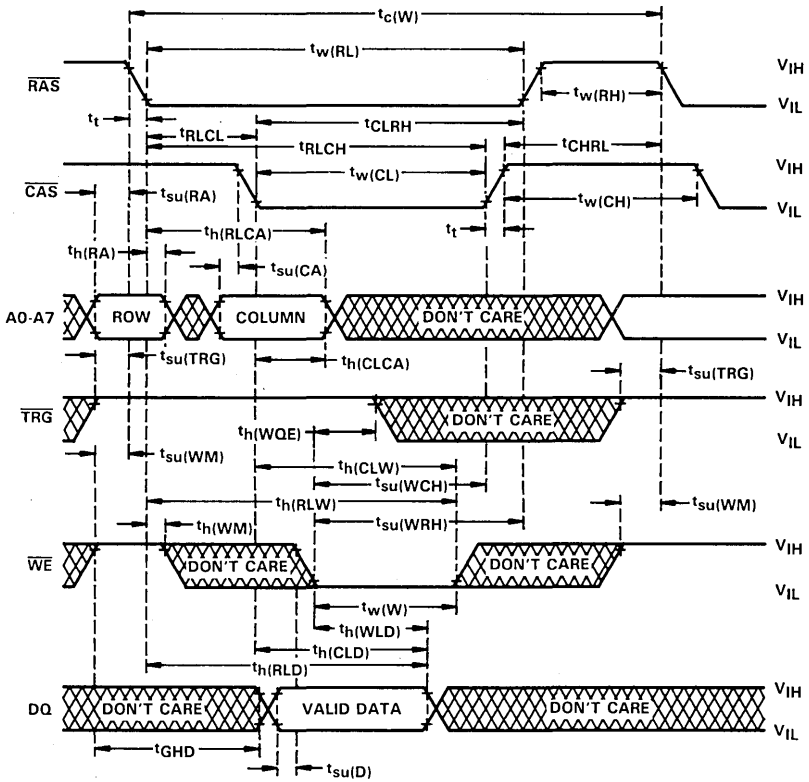
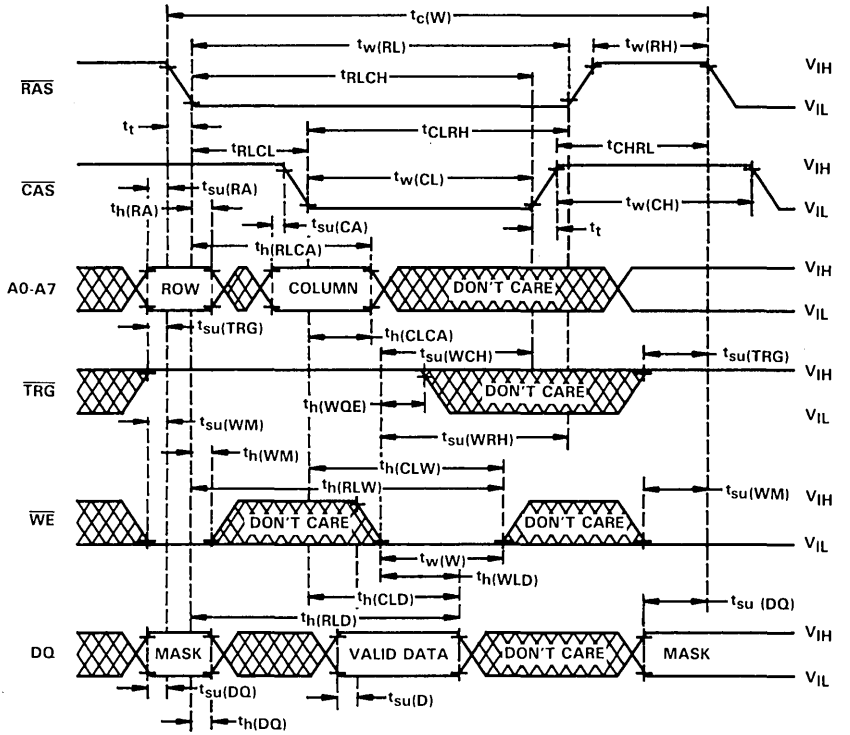
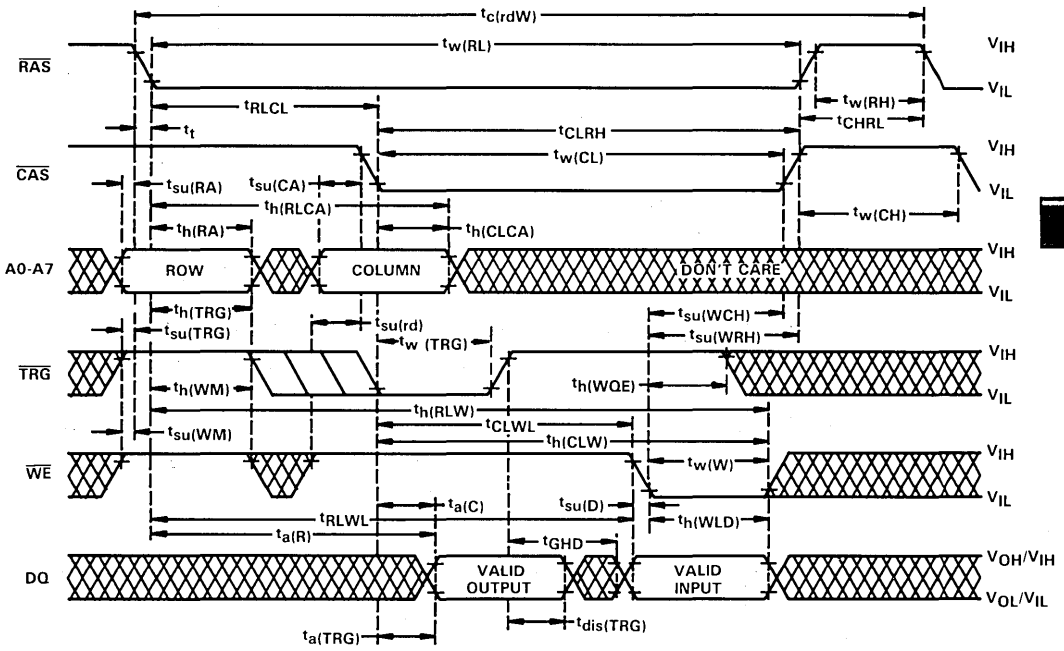
delayed write cycle timing, mask unselected



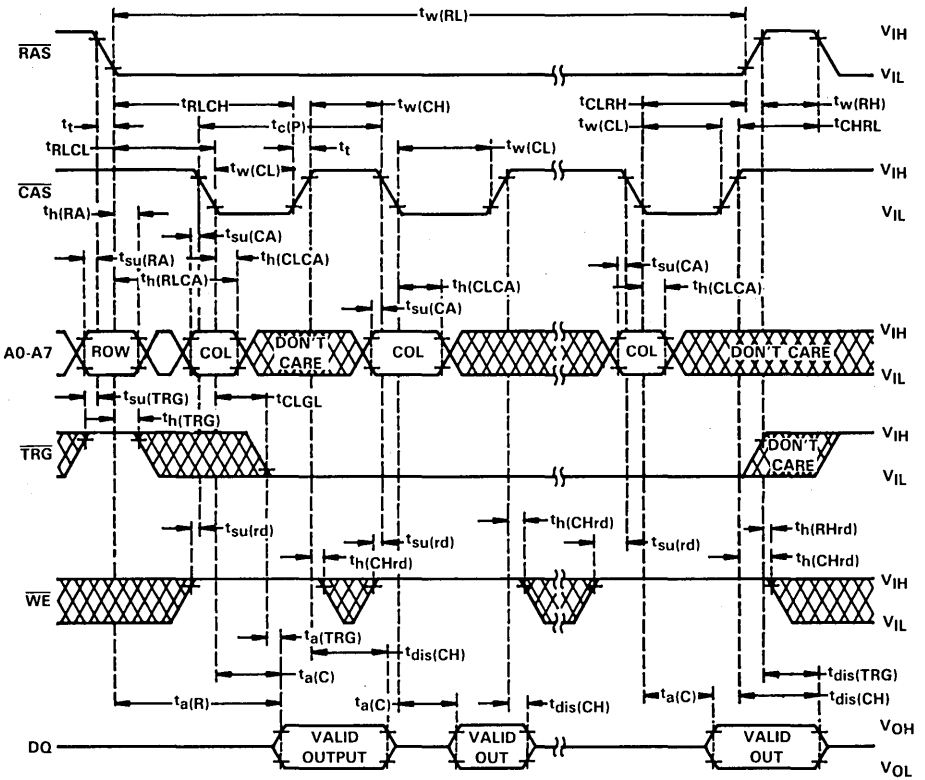
delayed write cycle timing, mask selected



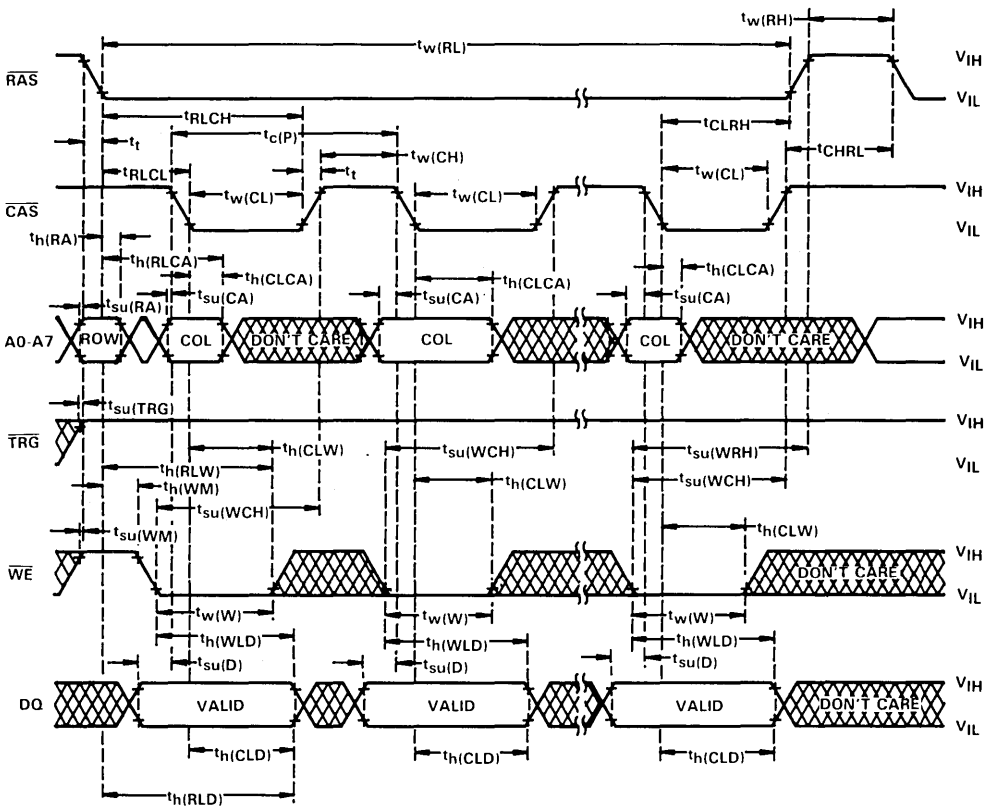
read-write/read-modify-write cycle timing



page-mode read cycle timing

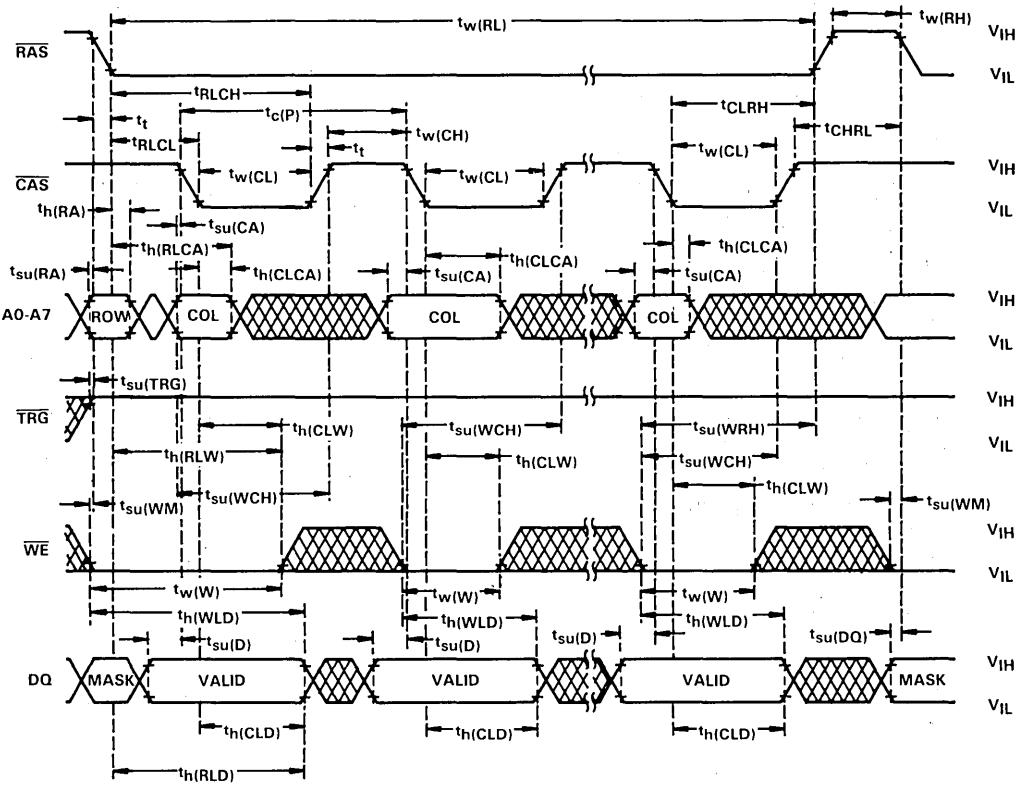


page-mode write cycle timing, write mask unselected



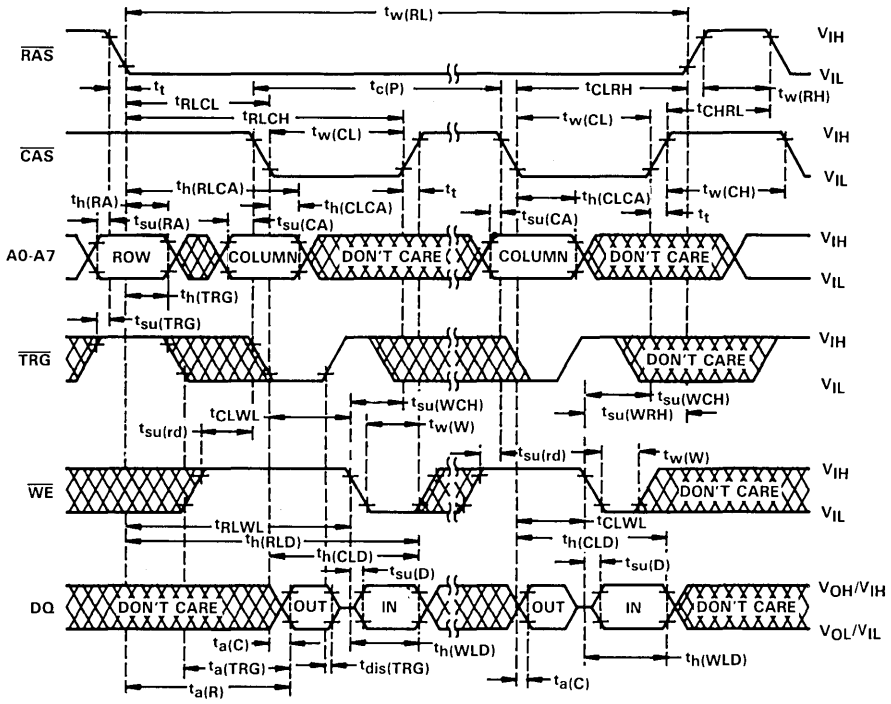
NOTE 6: Timing assumes use of the early write feature. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used to guarantee page-mode cycle time.

page-mode write cycle timing, write mask selected

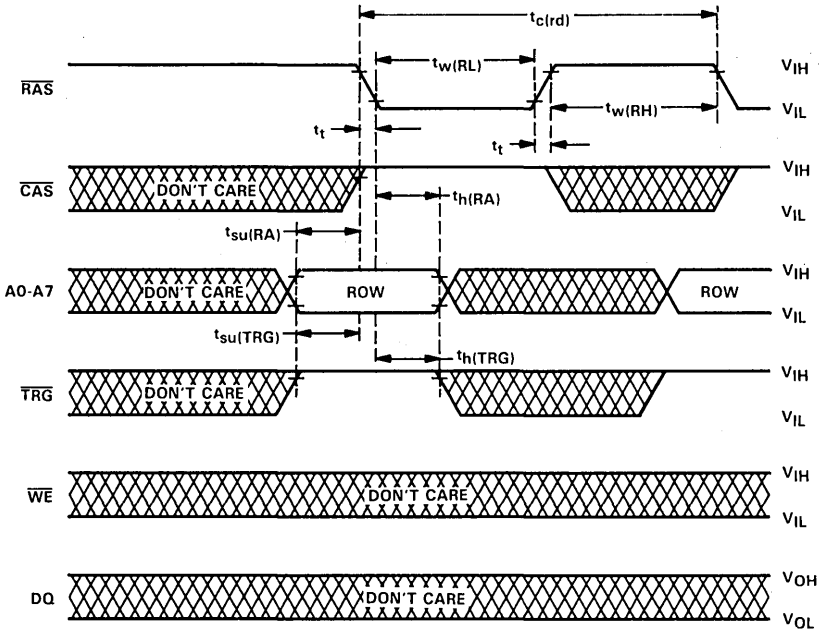


NOTE 7: Timing assumes use of the early write feature. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used to generate page-mode cycle time. Timing also assumes that only those I/Os selected by DQ1-DQ4 on the falling edge of $\overline{RAS}$ are written during page-mode operation.

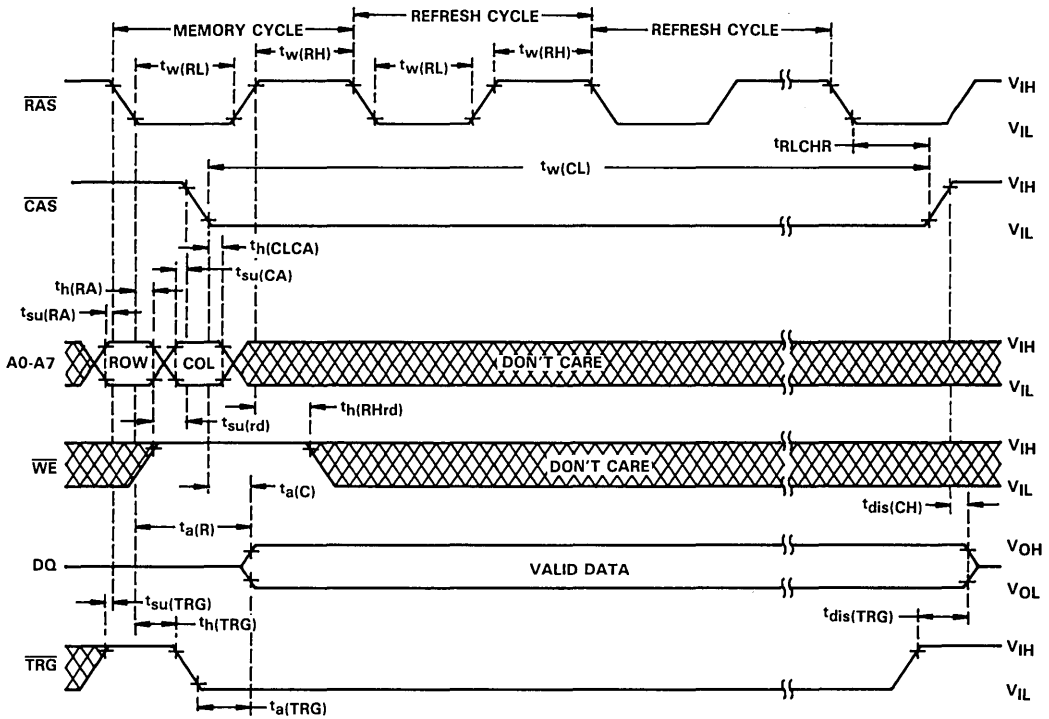
page-mode read-modify-write cycle timing



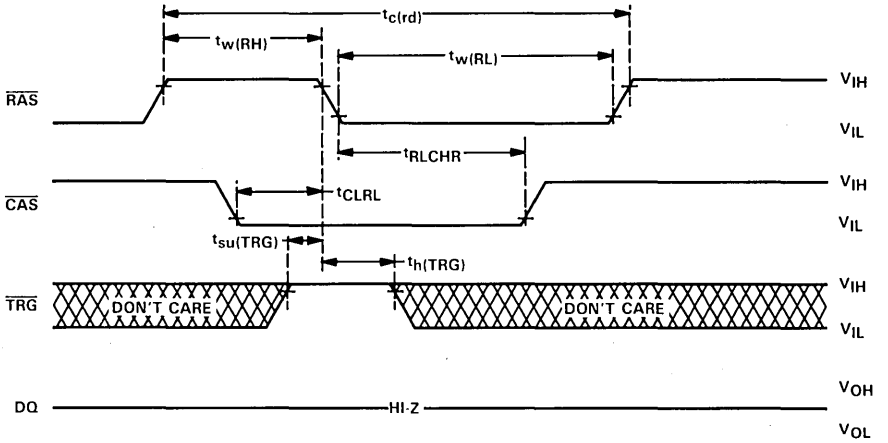
$\overline{\text{RAS}}$-only refresh timing



hidden refresh cycle timing

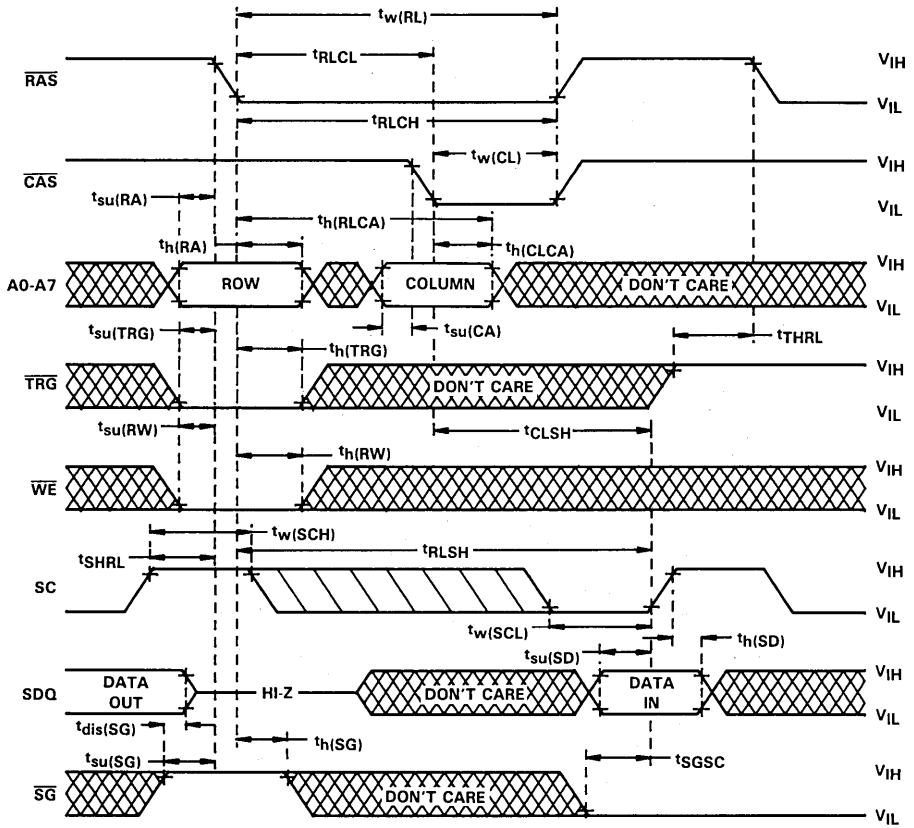


$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh



write-mode control timing

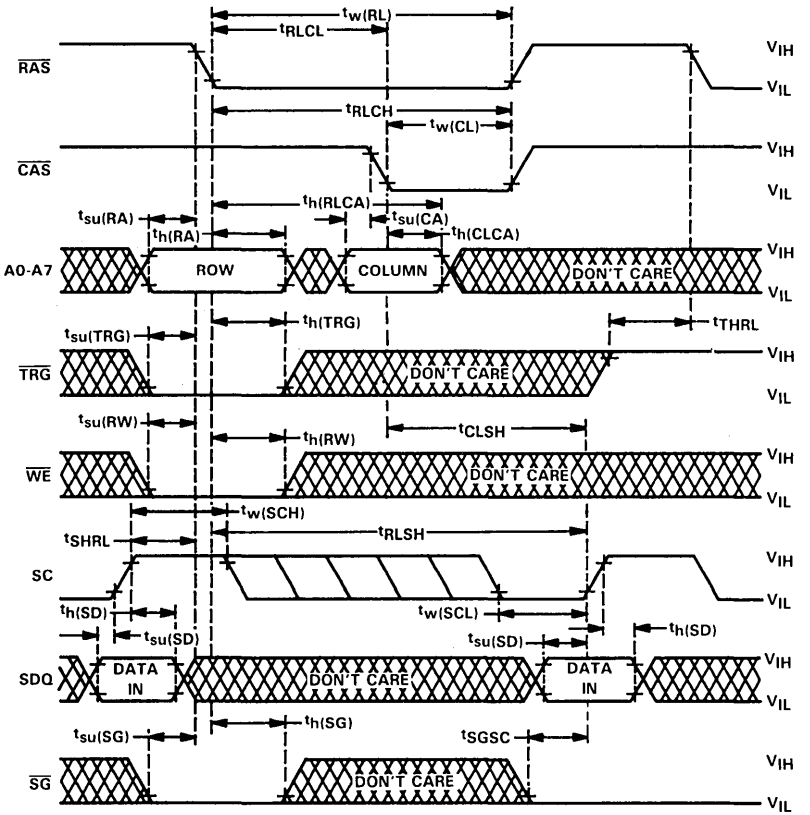
The write-mode control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. The diagram below assumes that the device was originally in the serial read mode.



NOTES: 8. Random-mode (Q outputs) remain in 3-state for the entire write-mode control.
9. $\overline{SG}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

data-register-to-memory timing, serial input enabled

The data-register-to-memory cycle is used to transfer data from the data register to the memory array. Every one of the 256 locations in the data register is written into the 256 columns of the selected row. Note that the data that was in the data register may have arrived there either from a serial write in or from a parallel load of the data register from one of the memory array rows. The diagram below assumes that the device is presently in the serial-write mode (i.e., SD is enabled by a previous write-mode control cycle, thus allowing data to be written in).

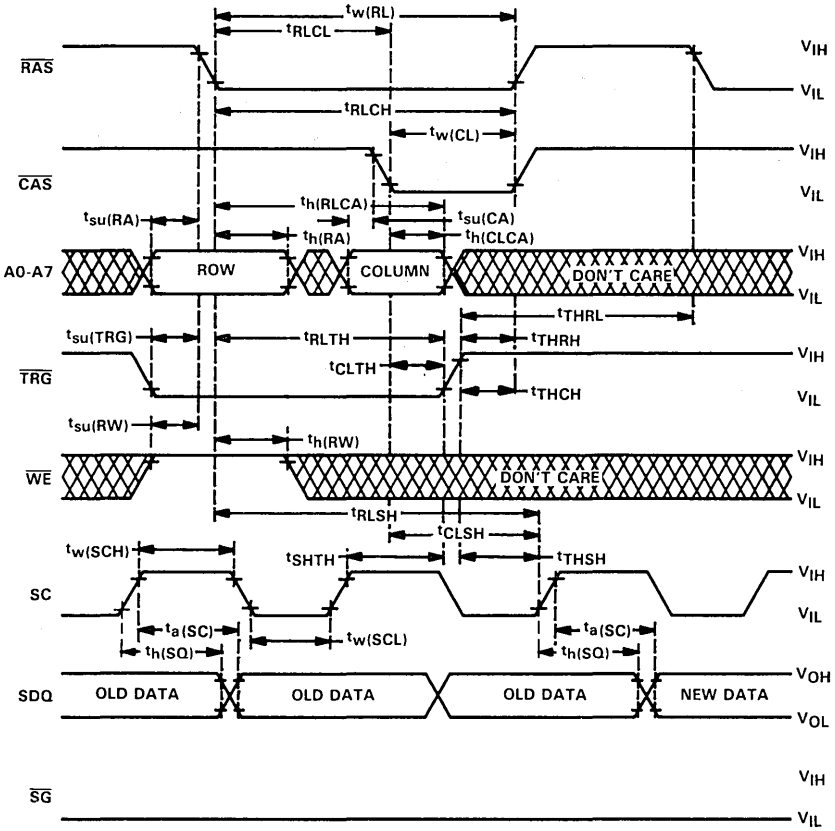


NOTES: 10. Random-mode (Q outputs) remain in 3-state for the entire data-register-to-memory transfer cycle.
11. $\overline{SG}$ must be low as $\overline{RAS}$ falls in order to perform a register-to-memory transfer.

memory-to-data register timing

The memory-to-data-register cycle is used to load the data register in parallel from the memory array. Every one of the 256 locations in the data register are written into from the 256 columns of the selected row. Note that the data that is loaded into the data register may be either read out or written back into another row. This cycle puts the device into the serial read mode (i.e., the SQ is enabled, thus allowing data to be read out of the register).

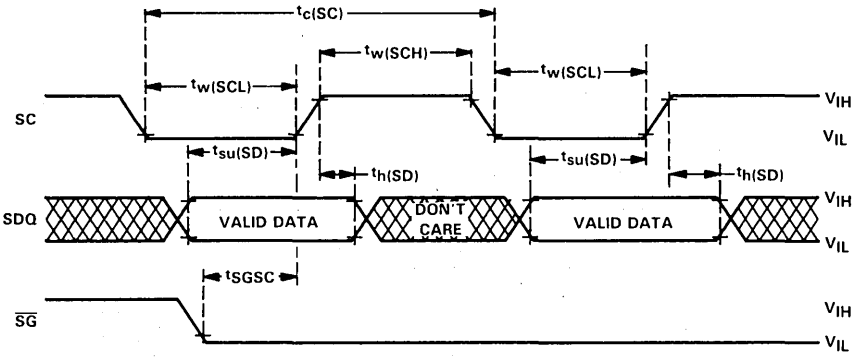
Also, the first bit to be read from the data register, after $\overline{TRG}$ has gone high, must be activated by a positive transition of SC.



NOTES: 12. Random mode (Q outputs) remain in 3-state for the entire memory-to-data-register transfer cycle.
13. Column address must be supplied to load register start address on every transfer cycle.
14. The first positive transition of SC after $\overline{TRG}$ has gone high, during a memory-to-register transfer cycle, is used to read the first bit of new data.

serial data-in timing

The serial data-in write cycle is used to write data into the data register. Before data can be written into the data register via SD, the device must be put into the write mode by performing a write-mode control cycle. Register-to-memory transfer cycles occurring between the write-mode control cycle and the subsequent writing in of data will not take the device out of the write mode. But, a memory-to-register transfer cycle during that time will take the device out of the write mode and put it into the read mode, thus not allowing the writing in of data.



NOTE 15: While writing data into the data register, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-to-memory or memory-to-register data-transfer function.

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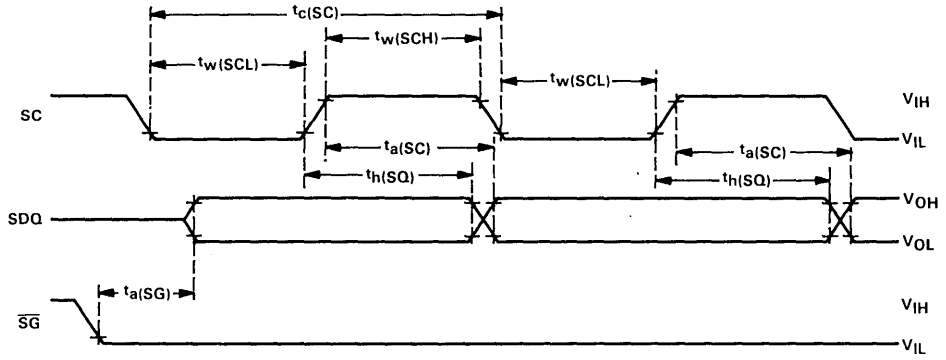
serial data-out timing

The serial data-out read cycle is used to read data out of the data register. Before data can be read out via SQ, the device must be put into the read mode by performing a memory-to-data-register transfer cycle. Register-to-memory transfer cycles occurring between the memory-to-register transfer cycle and the subsequent reading out of data will not take the device out of the read mode. But, a write-mode control cycle at that time will take the device out of the read mode and put it in the write mode, thus not allowing the reading out of data.



NOTE 16: While reading data out of the data register, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-to-memory or memory-to-register data-transfer operation.

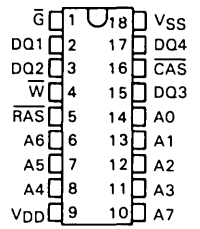
NOVEMBER 1983 – REVISED JUNE 1987

- 65,536 × 4 Organization
- Single 5-V Supply (10% Tolerance)
- JEDEC Standardized Pinout
- Pinout Identical to TMS4416 (16K × 4 Dynamic RAM)
- Performance Ranges:

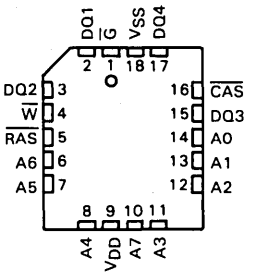
	ACCESS TIME ROW ADDRESS MAX	ACCESS TIME COLUMN ADDRESS MAX	READ OR WRITE CYCLE MIN	READ-MODIFY-WRITE CYCLE MIN
TMS4464-10	100 ns	50 ns	200 ns	270 ns
TMS4464-12	120 ns	60 ns	220 ns	295 ns
TMS4464-15	150 ns	75 ns	260 ns	345 ns

- Long Refresh Period . . . 4 ms (Max)
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- On-Chip Substrate Bias Generator
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Early Write or $\overline{G}$ to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Power Dissipation As Low As:
  - Operating . . . 330 mW (Max)
  - Standby . . . 25 mW (Max) (for 150 ns devices)
- $\overline{RAS}$-Only Refresh Mode
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Mode
- Available with MIL-STD-883C, Class B Processing and S (−55°C to 110°C) Temperature Ranges (SMJ4464)

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4464 is a high-speed, 262,144-bit dynamic random-access memory, organized as 65,536 words of four bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

This device features maximum $\overline{RAS}$ access times of 100 ns, 120 ns, or 150 ns. Power dissipation maximums are 330 mW operating and 25 mW standby for 150-ns devices.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 125 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4464 is offered in 18-pin plastic dual-in-line and 18-lead plastic chip carrier packages. It is guaranteed for operation from 0°C to 70°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed or read-modfy-write cycle, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(G)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high-impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying t_{GHD}.

output enable ($\overline{G}$)

The $\overline{G}$ input controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state they will remain in the low-impedance state until $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

The $\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}) and holding it low after $\overline{RAS}$ falls (see parameter t_{RLCHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The external address is also ignored during the hidden refresh cycles. The data at the output pin remains valid up to the maximum $\overline{CAS}$ low pulse duration, $t_{w(CL)}$.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by $t_{w(RL)}$, the maximum $\overline{RAS}$ low pulse duration.

power up

To achieve proper device operation, an initial pause of 200 μs is required after power up, followed by a minimum of eight initialization cycles.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

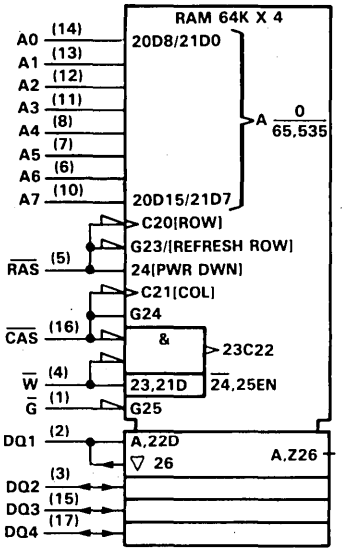
NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		V_{DD}+1	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

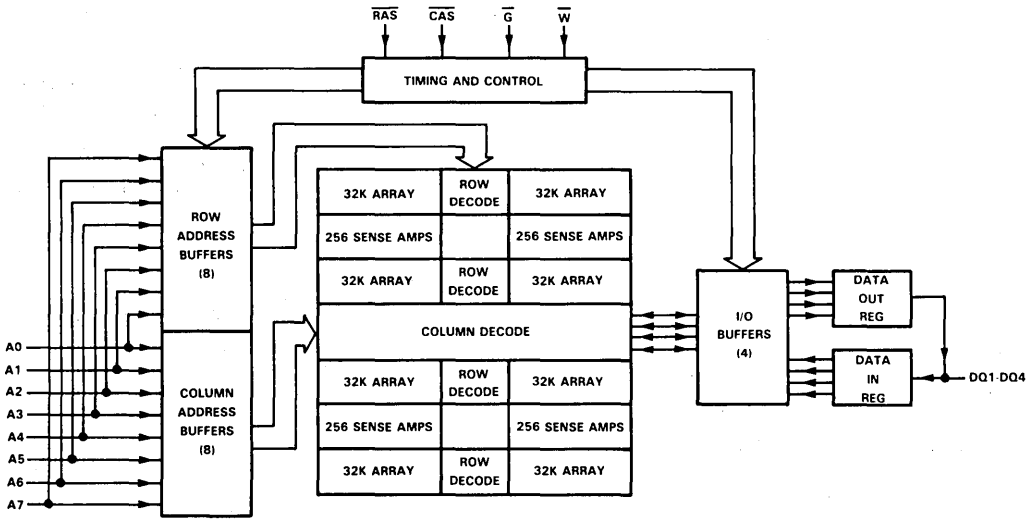
NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the dual-in-line package.

functional block diagram



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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4464-10		TMS4464-12		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V to 6.5 V		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high, All outputs open		±10		±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		70		65	mA
I_{DD2}	Standby current	After 1 memory cycle, DQ1-DQ4 held at > 0 V, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		4.5		4.5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, CAS high, All outputs open		58		53	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		50		45	mA

PARAMETER		TEST CONDITIONS	TMS4464-15		UNIT
			MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V to 6.5 V		±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high, All outputs open		±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		60	mA
I_{DD2}	Standby current	After 1 memory cycle, DQ1-DQ4 held at > 0 V, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		4.5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high, All outputs open		48	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open		40	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TMS4464		UNIT
		MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i/o}$	Output capacitance		7	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4464-10		TMS4464-12		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		50		60	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		100		120	ns
$t_{a(G)}$†	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GAC}		30		35	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GOFF}	0	30	0	30	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4464-15		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		150	ns
$t_{a(G)}$†	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GAC}		40	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GOFF}	0	30	ns

†$t_{a(C)}$ and $t_{a(R)}$ must be satisfied to guarantee $t_{a(G)}$.

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timing requirements over recommended supply voltage range and operating free-air temperature range (see Note 3)

		ALT. SYMBOL	TMS4464-10		TMS4464-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	100		120		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	170		195		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	200		220		ns
$t_{c(W)}$	Write cycle time	t_{WC}	200		220		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	270		295		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	40		50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	50	10,000	60	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	90		90		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	100	10,000	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	30		30		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	30		35		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	30		35		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	15		20		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	65		80		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	30		30		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	80		90		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	30		30		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	30		30		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	80		90		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} MAX and V_{IH} MIN.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (continued) (see Note 3)

		ALT. SYMBOL	TMS4464-10		TMS4464-12		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	20		25		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	50		60		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{CWD}	85		95		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	10		10		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	50	25	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{RWD}	135		155		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{GDD}	30		30		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} MAX and V_{IH} MIN.
¶ $\overline{CAS}$-before-$\overline{RAS}$ refresh option only.
# $\overline{G}$ must disable the output buffers prior to applying data to the device.

timing requirements over recommended supply voltage range and operating free-air temperature range (continued) (see note 3)

		ALT. SYMBOL	TMS4464-15 MIN	TMS4464-15 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	145		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	230		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	75	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} MAX and V_{IH} MIN.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).

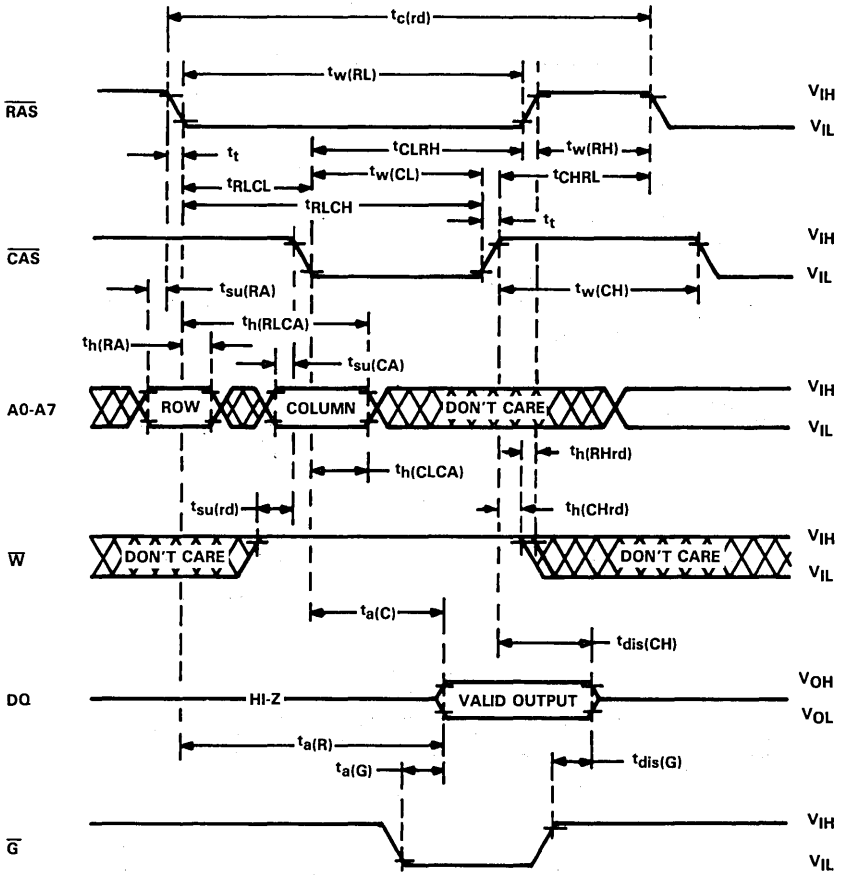
§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded) (see Note 3)

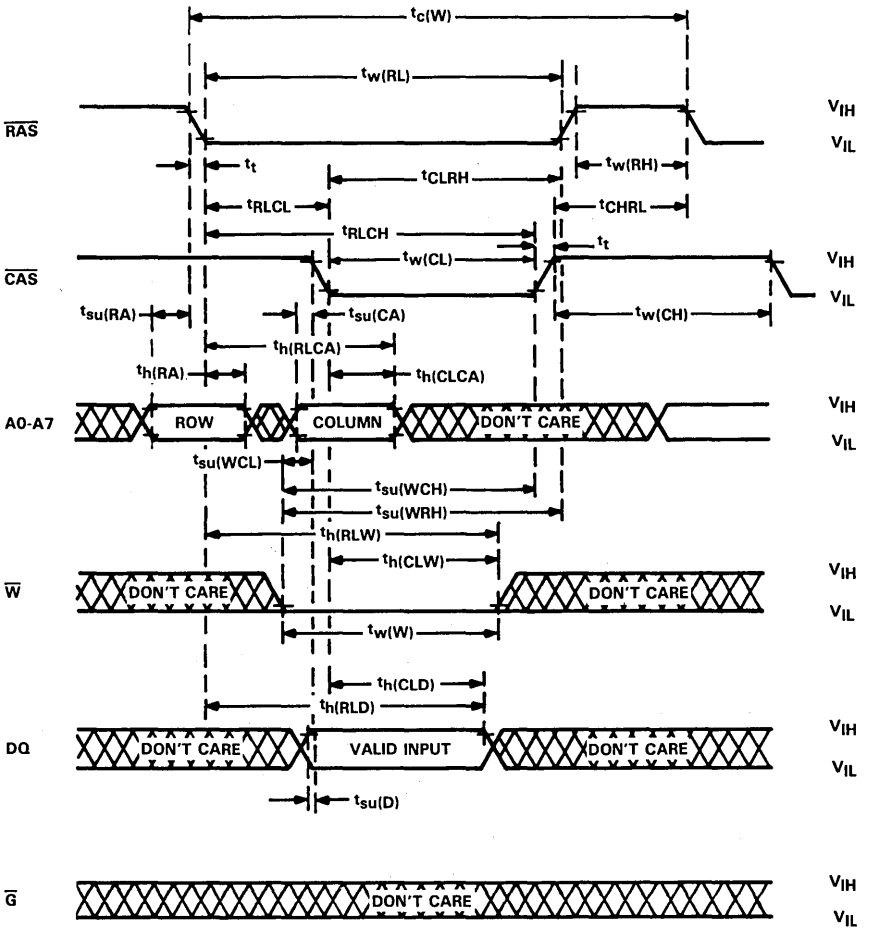
		ALT. SYMBOL	TMS4464-15 MIN	TMS4464-15 MAX	UNIT
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{CWD}	110		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	20		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	75	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{RWD}	185		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{GDD}	30		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} MAX and V_{IH} MIN.
¶ $\overline{CAS}$-before-$\overline{RAS}$ refresh option only.
# $\overline{G}$ must disable the output buffers prior to applying data to the device.

read cycle timing



early write cycle timing



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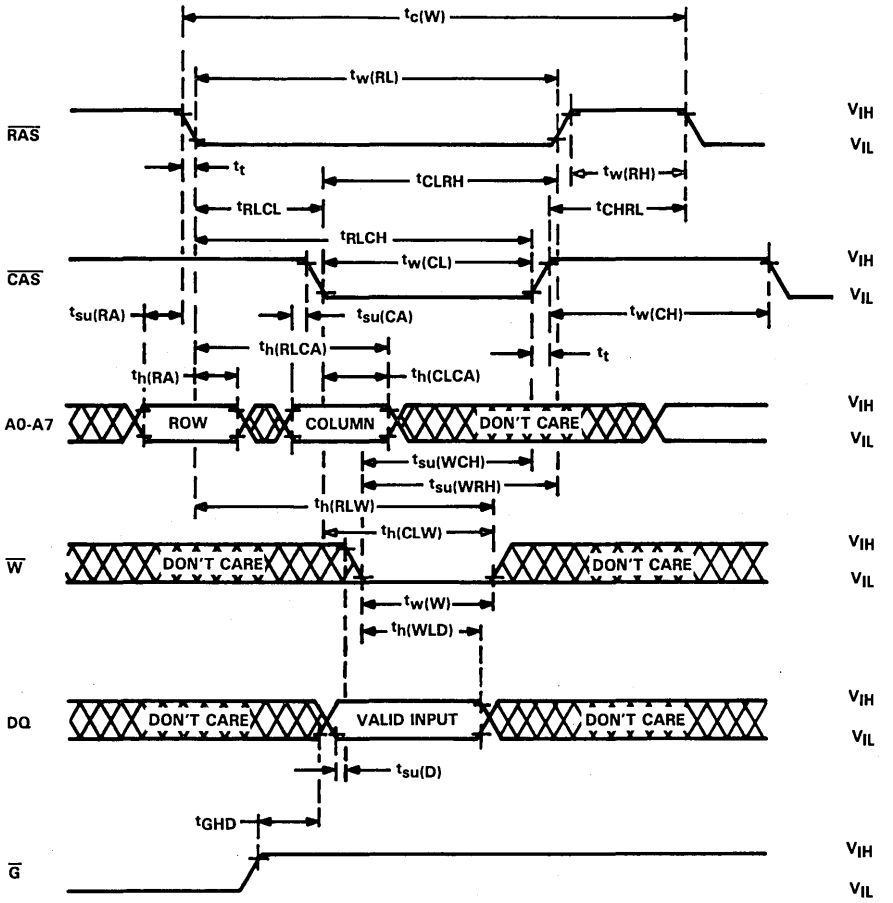
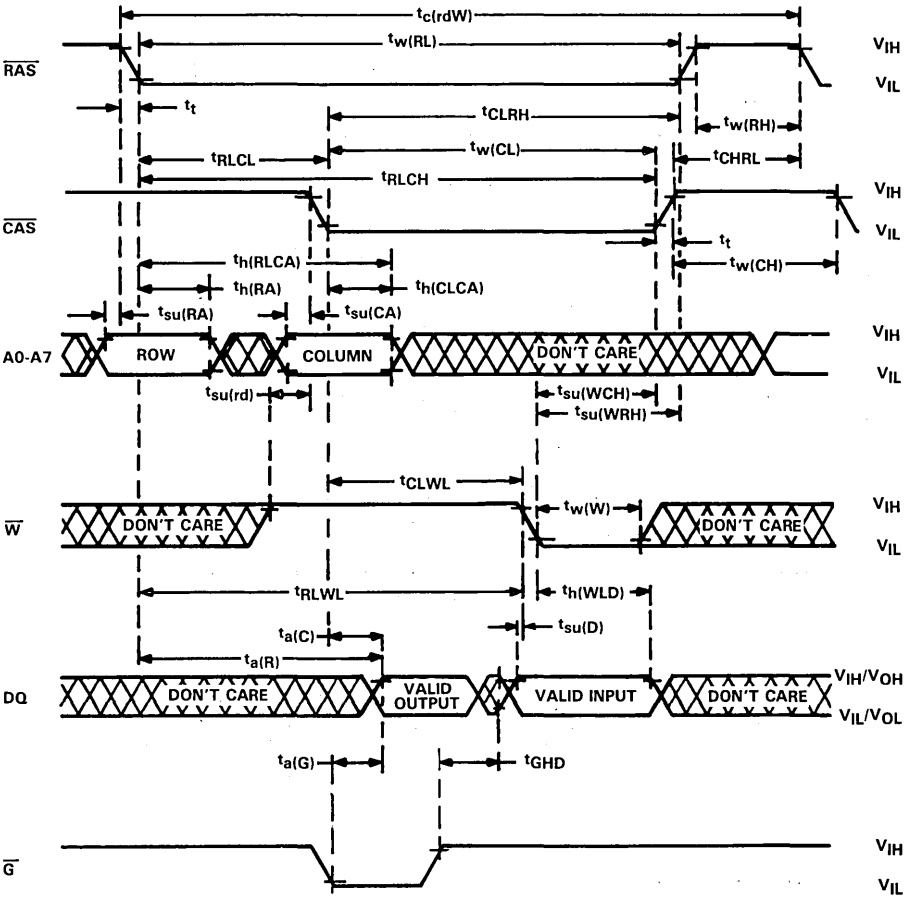
write cycle timing



read-write/read-modify-write cycle timing



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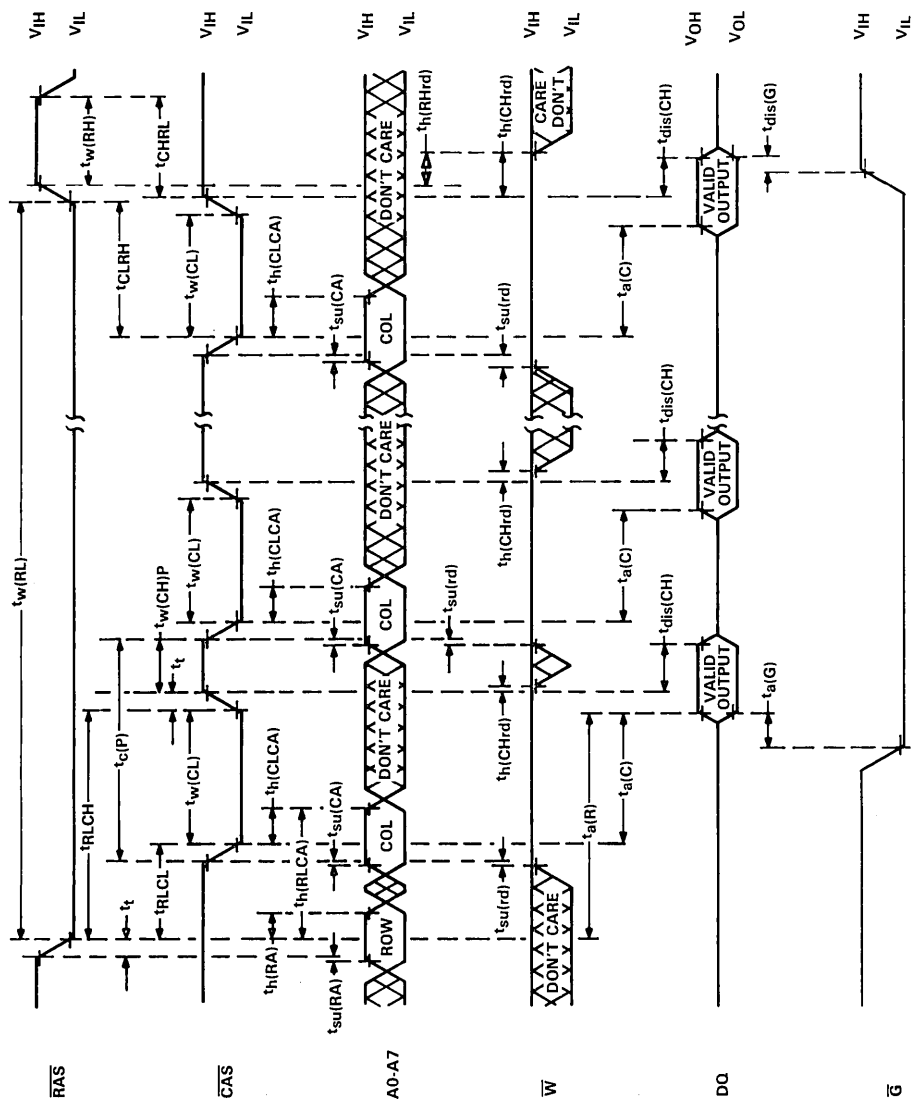
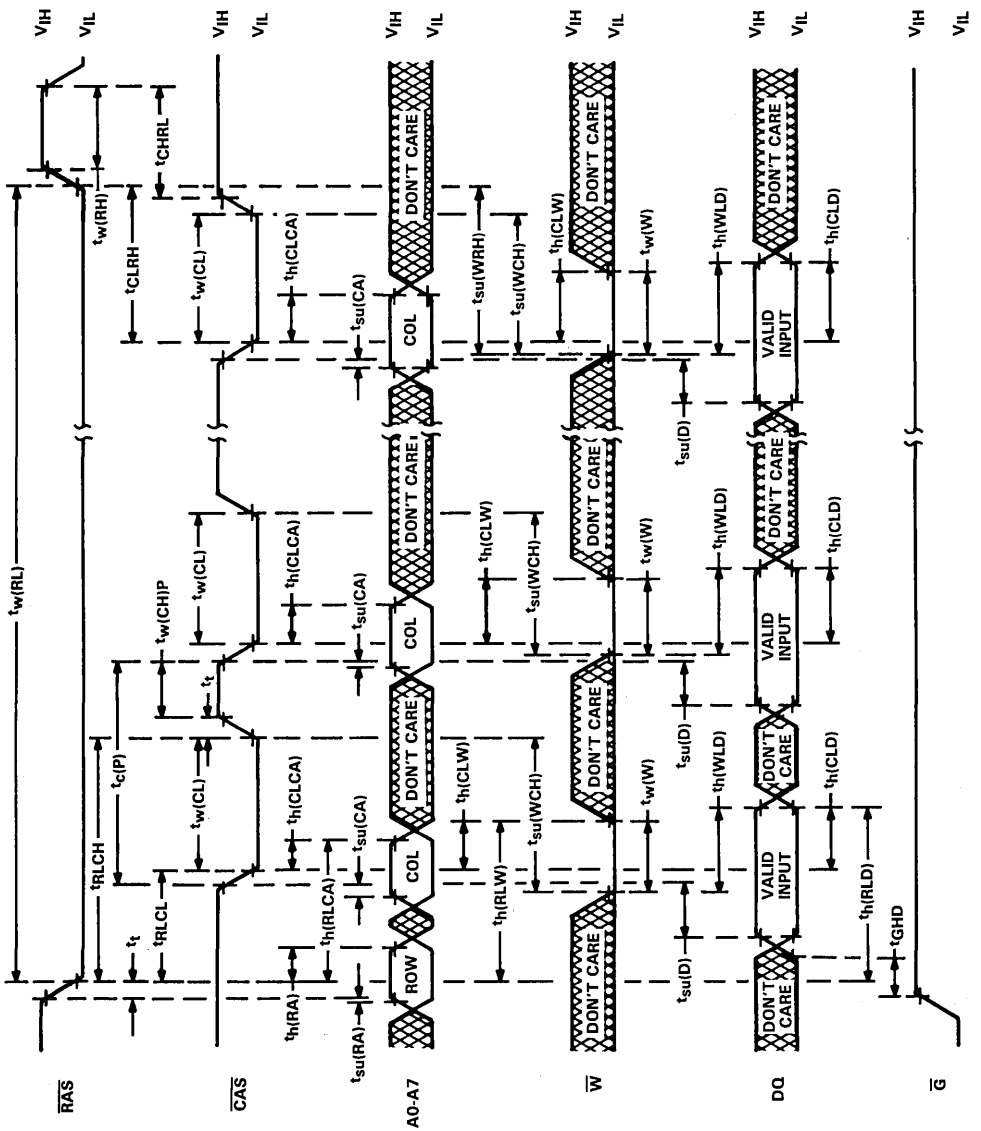
page-mode read cycle timing



NOTE 4: A write cycle or read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



NOTE 5: A write cycle or read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

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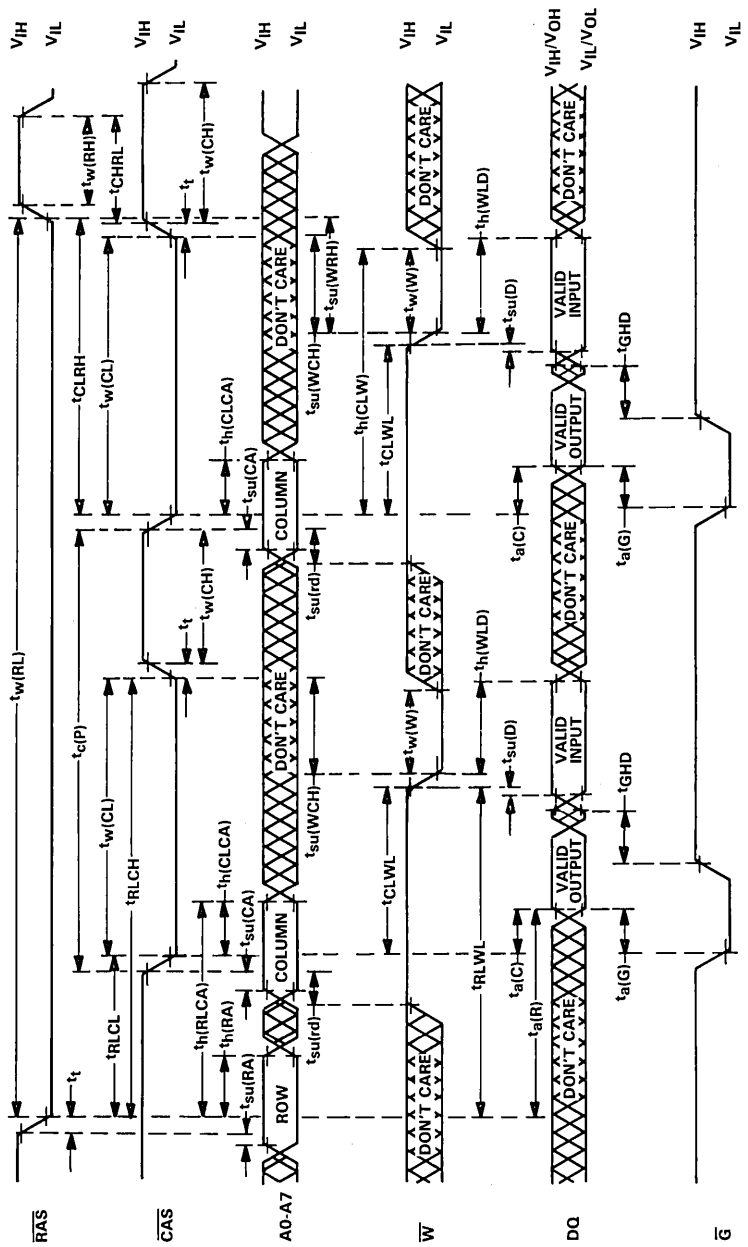
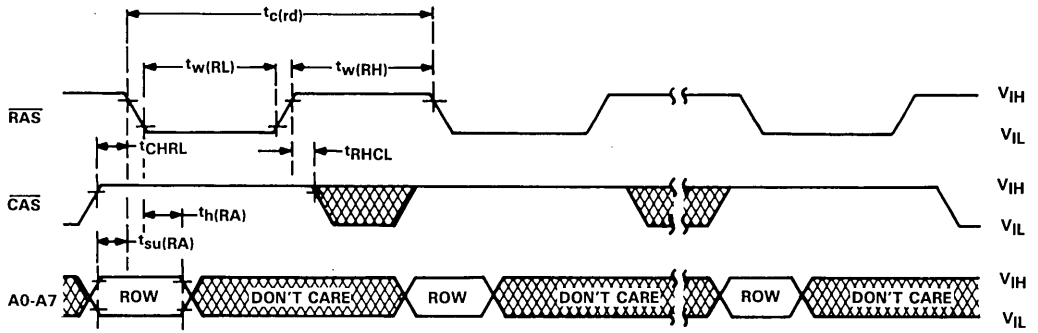
page-mode read-modify-write cycle timing

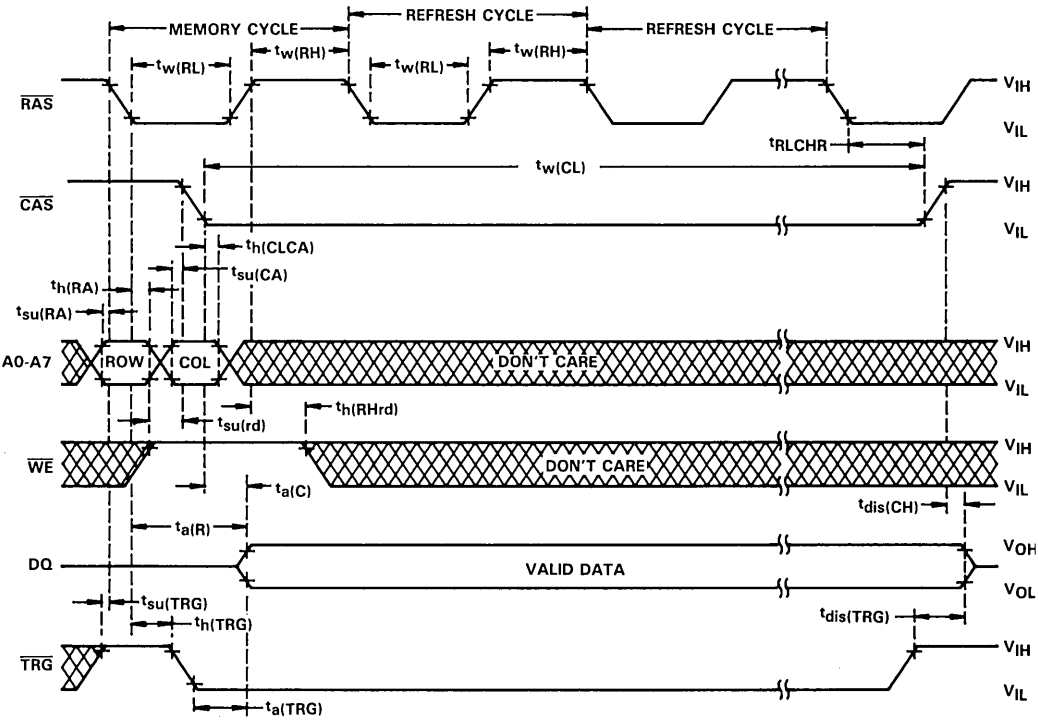


NOTE 6: A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

RAS-only refresh cycle timing



hidden refresh cycle timing



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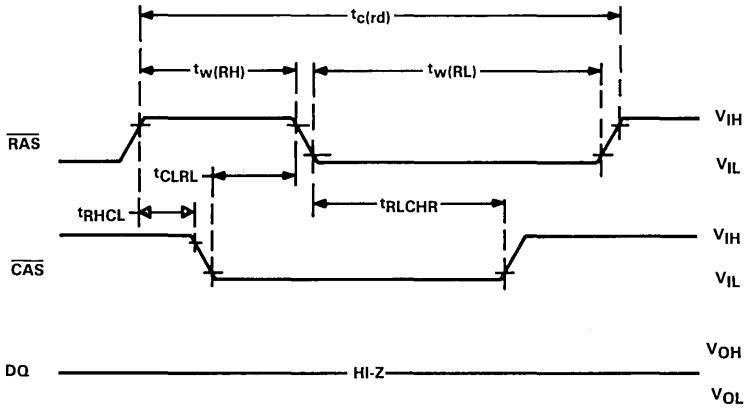
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle timing



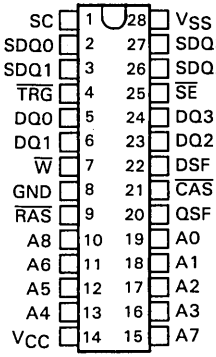
AUGUST 1988

- DRAM: 262,144 Words × 4 Bits
  SAM: 512 Words × 4 Bits
- Dual Port Accessibility—Simultaneous and Asynchronous Access from the DRAM and SAM Ports
- Bidirectional Data Transfer Function Between the DRAM and the Serial Data Register
- 4 × 4 Block Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle From an On-Chip Color Register
- Write Per Bit Feature for Selective Write to Each RAM I/O. Two Write Per Bit Modes to Simplify System Design
- Enhanced Page Mode Operation for Faster Access
- $\overline{CAS}$-before-$\overline{RAS}$ and Hidden Refresh Modes
- RAM Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Long Refresh Period . . . Every 8 ms (Max)
- DRAM Port is Compatible with the TMS44C256
- Up to 33 MHz Uninterrupted Serial Data Streams
- Split Serial Data Register for Simplified Realtime Register Reload
- 3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams
- 512 Selectable Serial Register Starting Locations
- All Inputs and Outputs TTL Compatible
- Performance Ranges:

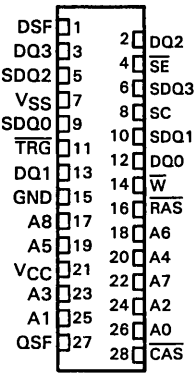
	ACCESS TIME ROW ADDRESS (MAX) $t_{a(R)}$	ACCESS TIME COLUMN ENABLE (MAX) $t_{a(C)}$	ACCESS TIME SERIAL DATA (MAX) $t_{a(SC)}$	ACCESS TIME SERIAL ENABLE (MAX) $t_{a(SE)}$
TMS44C251-10	100 ns	25 ns	30 ns	20 ns
TMS44C251-12	120 ns	35 ns	35 ns	25 ns
TMS44C251-15	150 ns	45 ns	40 ns	30 ns

- Texas Instruments EPIC™ CMOS Process

DJ PACKAGE
(TOP VIEW)



SD PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column Enable
DQ0-DQ3	DRAM Data In-Out/ Write Mask Bit
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row Enable
SC	Serial Data Clock
SDQ0-SDQ3	Serial Data In-Out
$\overline{TRG}$	Transfer Register/Q Output Enable
$\overline{W}$	Write Mask Select/ Write Enable
DSF	Special Function Select
QSF	Split Register Activity Status
V_{CC}	5-V Supply (TYP)
V_{SS}	Ground
GND	Ground (Important: not connected to internal V_{SS})

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descripton

The TMS44C251 Multiport Video RAM is a high speed, dual ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262,144 words of 4 bits each, interfaced to a serial data register, or Serial Access Memory (SAM), organized as 512 words of 4 bits each. The TMS44C251 supports three basic types of operation: random access to and from the DRAM, serial access to and from the serial register, and bidirectional transfer of data between any row in the DRAM and the serial register. Except during transfer operations, the TMS44C251 can be accessed simultaneously and asynchronously from the DRAM and SAM ports. During transfer operation, the 512 columns of the DRAM are connected to the 512 positions in the serial data register. The 512 × 4 bit serial data register can be loaded from the memory row (transfer read) or else the contents of the 512 × 4 bit serial data register can be written to the memory row (transfer write).

The TMS44C251 is equipped with several features designed to provide higher system level bandwidth and simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's novel 4 × 4 Block Write Mode. Block Write mode allows four bits of data present in an on-chip color data register to be written to any combination of four adjacent column address locations. As many as 16 bits of data can be written to memory during each $\overline{CAS}$ cycle time. Also on the DRAM port, a write mask register provides a persistent write per bit mode without repeated mask loading.

On the serial register, or SAM port, the TMS44C251 offers a split register transfer read (DRAM to SAM) option which enables realtime register reload implementation for truly continuous serial data streams, without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. This new realtime register reload implementation allows truly continuous serial data. For applications not requiring realtime register reload (for example, reloads done during CRT retrace periods), the single register mode of operation is retained to simplify system design. The SAM can also be configured in input mode, accepting serial data from an external device. Once the serial register within the SAM is loaded, its contents can be transferred to the corresponding column positions in any row in memory in a single memory cycle.

The SAM port is designed for maximum performance. Data can be input to or accessed from the SAM at serial rates up to 33 MHz. During split register mode of operation, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate open drain output, designated QSF, is included to designate which half of the serial register is active at any given time in split register mode.

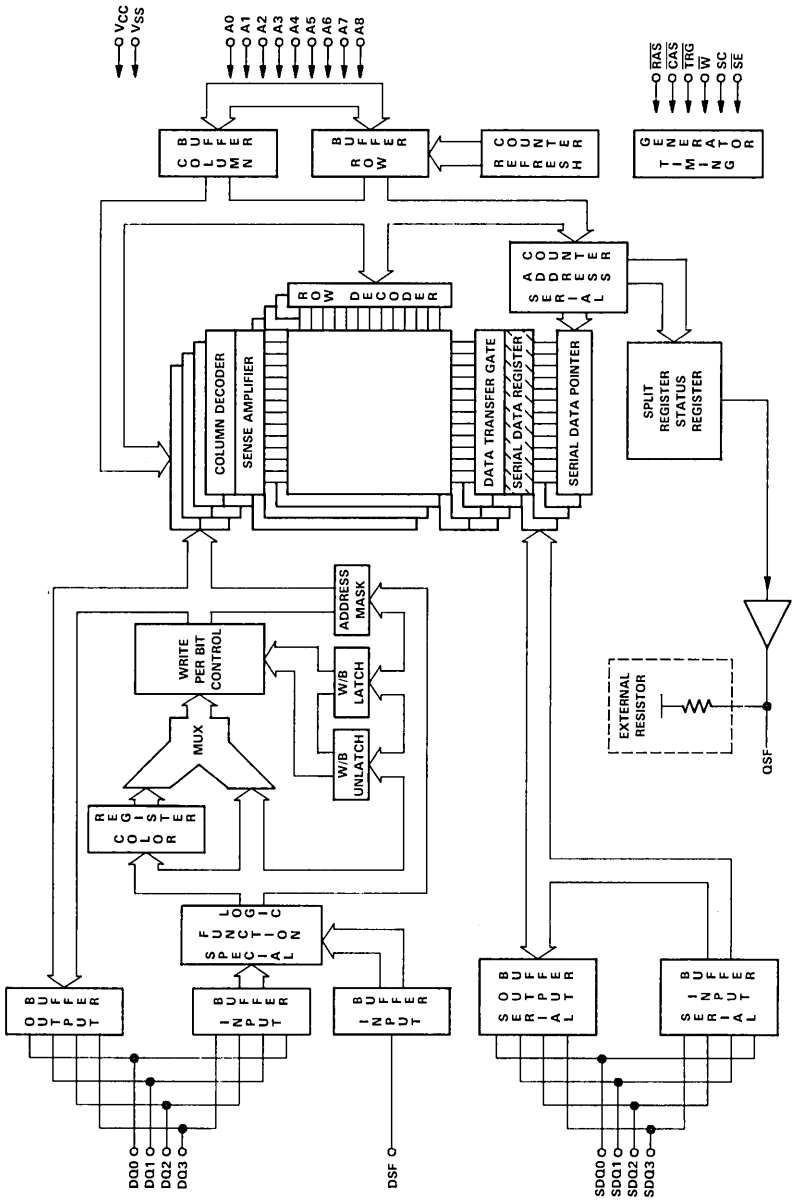
All inputs, outputs, and clock signals on the TMS44C251 are compatible with Series 74 TTL. All address lines and data-in are latched on-chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

The TMS44C251 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The TMS44C251 is offered in a 28-pin small-outline J-leaded package (DJ suffix) for direct surface mounting in rows on 400-mil (5,08-mm) centers. It is also offered in a 400-mil, 28-pin zig-zag in-line package (SD suffix). Both packages are characterized for operation from 0°C to 70°C (L suffix).

The TMS44C251 and other Multiport Video RAMs are supported by a broad line of graphics processor and control devices from Texas Instruments, including the TMS34010 Graphics System Processor.

functional block diagram



DETAILED PIN DESCRIPTION vs OPERATIONAL MODE

PIN	DRAM	TRANSFER	SAM
A0-A8	Row, Column Address	Row, Tap Address	
$\overline{CAS}$	Column Enable	Tap Address Strobe	
DQi	DRAM Data I/O Write Mask Bits		
$\overline{SE}$		Serial-In Mode Enable	Serial Enable
$\overline{RAS}$	Row Enable	Row Enable	
SC			Serial Clock
SDQi			Serial Data I/O
$\overline{TRG}$	Q Output Enable	Transfer Enable	
$\overline{W}$	Write Enable Write per Bit Select	Transfer Write Enable	
DSF	Block Write Enable	Split Register Enable	
	Persistent Write per Bit Enable	Alternate Write Transfer Enable	
	Color Register Load Enable		
	Write per Bit Mask Load Enable		
QSF			Split Register Active Status
V_{CC}	5-V Supply (typical)		
V_{SS}	Device Ground		
GND	System Ground		

operation

random access operation

Refer to Table 1, Functional Truth Table, for Random Access and Transfer Operations. Random access operations are denoted by the designator "R" and transfer operations are denoted by a "T."

transfer register select and DQ enable ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either register or random access operation as $\overline{RAS}$ falls. For random access (DRAM) mode, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. Asserting $\overline{TRG}$ high as $\overline{RAS}$ falls causes the 512 storage elements of each data register to remain disconnected from the corresponding 512-bit lines of the memory array. (Asserting $\overline{TRG}$ low as $\overline{RAS}$ falls connects the 512-bit positions in the serial register to the bit lines and indicates that a transfer will occur between the data registers and the selected memory row. See "Transfer Operation" for details.)

During random access operations, $\overline{TRG}$ also functions as an output enable for the random (Q) outputs. Whenever $\overline{TRG}$ is held high, the Q outputs are in the high-impedance state to prevent an overlap between the address and DRAM data. This organization allows the connection of the address lines to the data I/O lines but prohibits the use of the early write cycle. It also allows read-modify-write cycles to be performed by providing a three-state condition to the common I/O pins so that write data can be driven onto the pins after output read data has been externally latched.

addresses (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations. Nine row address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Then, the nine column address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{CAS}$.

$\overline{RAS}$ and $\overline{CAS}$ address strobes and device control clocks

$\overline{RAS}$ is a control input that latches the states of the row address, $\overline{W}$, $\overline{TRG}$, $\overline{SE}$, $\overline{CAS}$, and DSF onto the chip to invoke the various DRAM and Transfer functions of the TMS44C251. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplfiers as well as the row decoder. $\overline{CAS}$ is a control input that latches the states of the column address and DSF to control various DRAM and Transfer functions. $\overline{CAS}$ also acts as an output enable for the DRAM output pins.

special function select (DSF)

The Special Function Select input is latched on the falling edges of $\overline{RAS}$ and $\overline{CAS}$, similarly to an address, and serves four functions. First, during write cycles DSF invokes persistent write per bit operation. If $\overline{TRG} = 1$, $\overline{W} = 0$, and DSF = 0 on the falling edge of $\overline{RAS}$, the write mask will be reloaded with the data present on the DQ pins. If DSF = 1 , the mask will not be reloaded but will retain the data from the last mask reload cycle.

Second, DSF is used to change the internally stored write per bit mask register (or write mask) via the load write mask cycle. The data present on the DQ pins when $\overline{W}$ falls is written to the write mask rather than to the addressed memory location. See "Delayed Write Cycle Timing" and the accompanying "Write Cycle State Table" in the timing diagram section. Once the write mask is loaded, it can be used on subsequent masked write per bit cycles. This feature allows systems with a common address and data bus to use the write per bit feature, eliminating the time needed for multiplexing the write mask and input data on the data bus.

Third, DSF is used to load an on-chip four-bit data, or "color," register via the Load Color Register cycle. The contents of this register can subsequently be written to any combination of four adjacent column memory locations using a 4 × 4 Block Write feature. The load color register cycle is performed using normal write cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Once the color register is loaded, it retains data until power is lost or until another load color register cycle is performed.

After loading the color register, the block write cycle can be enabled by holding DSF high on the falling edge of $\overline{CAS}$. During block write cycles, only the seven most significant column addresses (A2-A8) are latched on the falling edge of $\overline{CAS}$. The two least significant addresses (A0-A1) are replaced by the four DQ bits, which are also latched on the later of $\overline{CAS}$ or $\overline{W}$ falling. These four bits are used as an address mask and indicate which of the four column address locations addressed by A2-A8 will be written with the contents of the color register during the write cycle, and which ones will not. DQ0 enables a write to column address A1 = 0, A0 = 0; DQ1 enables a write to A1 = 0, A0 = 1; DQ2 enables a write to A1 = 1, A0 = 0; and DQ3 enables a write to A1 = 1, A0 = 1. A logic level 1 enables a write and a logic level 0 disables the write. A maximum of 16 bits can be written to memory during each $\overline{CAS}$ cycle (see Figure 1, Block Write Diagram).

Fourth, the DSF pin is used to invoke the split register transfer and serial access operation, described in the sections "Transfer Operation" and "Serial Operation."

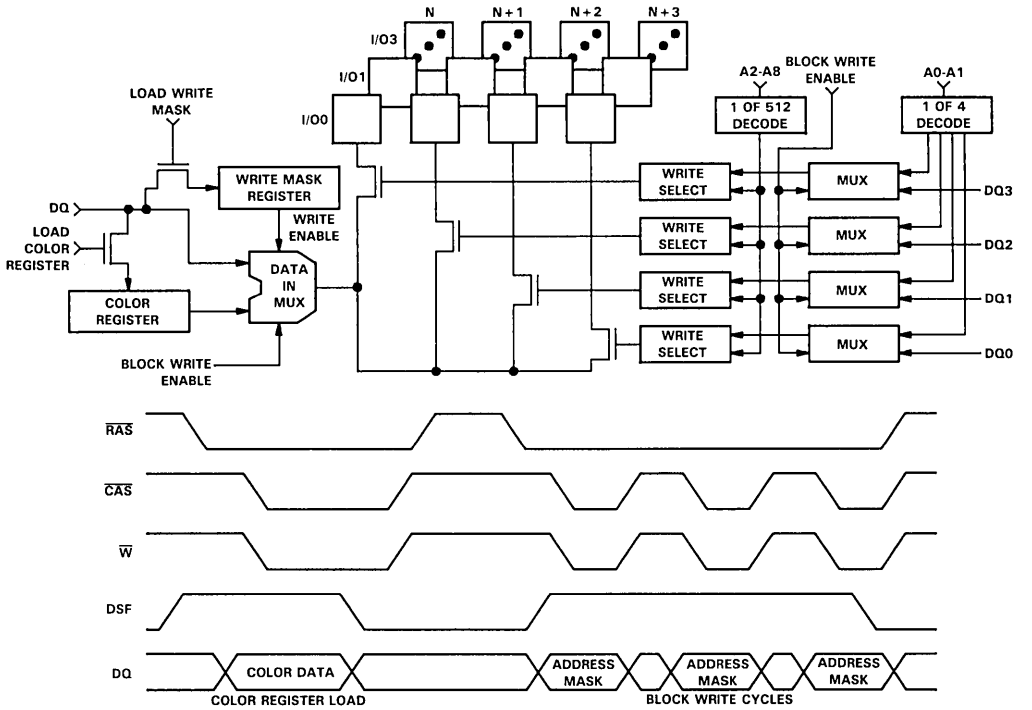


FIGURE 1. BLOCK WRITE DIAGRAM

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write enable, write per bit enable ($\overline{W}$)

The $\overline{W}$ pin enables data to be written to the DRAM and also is used to select the DRAM write per bit mode of operation. A logic high level on the $\overline{W}$ input selects the read mode and logic low level selects the write mode. In an Early Write cycle, $\overline{W}$ is brought low before $\overline{CAS}$ and the DRAM output pins (DQ) remain in the high-impedance state for the entire cycle. During DRAM write cycles, holding $\overline{W}$ low on the falling edge of $\overline{RAS}$ will invoke the write per bit operation. Two modes of write per bit operation are supported.

Case 1. If DSF = 0 on the falling edge of $\overline{RAS}$, the write mask is reloaded. Accordingly, a four-bit binary code (the write per bit mask) is input to the device via the random DQ pins and is latched on the falling edge of $\overline{RAS}$. The write per bit mask selects which of the four random I/Os are written and which are not. After $\overline{RAS}$ has latched the write mask on-chip, input data is driven onto the DQ pins and is latched on the falling edge of the later of $\overline{CAS}$ or $\overline{W}$. If a 0 was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will not be written to that I/O. If a 1 was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will be written to that I/O.

Case 2. If DSF = 1 on the falling edge of $\overline{RAS}$, the mask is not reloaded from the DQ pins but instead retains the value stored during the last write per bit mask reload. This mode of operation is known as Persistent Write per Bit, since the write per bit mask is persistent over an arbitrary number of cycles.

See the corresponding timing diagrams for details. IMPORTANT: The write per bit operation is invoked only if $\overline{W}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{W}$ is held high on the falling edge of $\overline{RAS}$, write per bit is not enabled and the write operation is identical to that of standard ×4 DRAMs.

data I/O (DQ0-DQ3)

DRAM data is written during a write or read-modify-write cycle. The falling edge of $\overline{W}$ strobes data into the on-chip data latches. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, CAS will already be low. Thus, the data will be strobed-in by $\overline{W}$ with data setup and hold times referenced to this signal.

The three-state output buffers provide direct TTL compatibility (no pull-up resistors required) with a fanout of two Series 74 TTL loads. Data-out is the same polarity as Data-in. The outputs are in the high impedance (floating) state as long as $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. Once the outputs are valid, they remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ or $\overline{TRG}$ going high returns the outputs to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a register transfer operation (memory to register or register to memory), the outputs remain in the high-impedance state for the entire cycle.

enhanced page mode

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS44C251 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page mode." Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

Enhanced page mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row address setup, row address hold, and address multiplex is thus eliminated, and a memory cycle time reduction of up to 3× can be achieved, compared to minimum $\overline{RAS}$ cycle times. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and page mode cycle time used. The TMS44C251 allows a full page (512 cycles) of information to be accessed in read, write, or read-modify-write mode during a single $\overline{RAS}$ low period using relatively conservative page mode cycle times.

During write per bit operations, the DQ pins are used to load the write per bit mask register using either mode of write per bit operation described above under the $\overline{W}$ pin description.

During block write operations, the DQ pins are used to load the on-chip color register during the load color register cycle and are also used as a write enable during block write cycles.

refresh

A refresh operation must be performed to each row at least once every eight milliseconds to retain data. Since the output buffer is in the high-impedance state (unless $\overline{CAS}$ is applied), the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

GND

This pin is reserved for the manufacturer's test operation. It is an input and should be tied to system ground to ensure proper device operation.

IMPORTANT: GND is not connected internally to V_{SS}.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored and the refresh address is generated internally.

TABLE 1. FUNCTIONAL TRUTH TABLE

TYPE†	RAS FALL					CAS FALL	ADDRESS		DQ0-3		FUNCTION
	CAS	TRG	W	DSF	SE	DSF	RAS	CAS	RAS	CAS‡ W	
R	0	X	1	X	X	X	X	X	X	X	CAS-BEFORE-RAS REFRESH
T	1	0	0	X	0	X	ROW ADDR	TAP POINT	X	X	REGISTER TO MEMORY TRANSFER (TRANSFER WRITE)
T	1	0	0	1	X	X	ROW ADDR	TAP POINT	X	X	ALTERNATE TRANSFER WRITE (INDEPENDENT OF SE)
T	1	0	0	0	1	X	REFRESH ADDR	TAP POINT	X	X	SERIAL WRITE-MODE ENABLE (PSEUDO-TRANSFER WRITE)
T	1	0	1	0	X	X	ROW ADDR	TAP POINT	X	X	MEMORY TO REGISTER TRANSFER (TRANSFER READ)
T	1	0	1	1	X	X	ROW ADDR	TAP POINT	X	X	SPLIT REGISTER TRANSFER READ (MUST RELOAD TAP)
R	1	1	0	0	X	0	ROW ADDR	COL ADDR	WRITE MASK	VALID DATA	LOAD AND USE WRITE MASK, WRITE DATA TO DRAM
R	1	1	0	0	X	1	ROW ADDR	COL A2-A8	WRITE MASK	ADDR MASK	LOAD AND USE WRITE MASK, BLOCK WRITE TO DRAM
R	1	1	0	1	X	0	ROW ADDR	COL ADDR	X	VALID DATA	PERSISTENT WRITE PER BIT, WRITE DATA TO DRAM
R	1	1	0	1	X	1	ROW ADDR	COL A2-A8	X	ADDR MASK	PERSISTENT WRITE PER BIT, BLOCK WRITE TO DRAM
R	1	1	1	0	X	0	ROW ADDR	COL ADDR	X	VALID DATA	NORMAL DRAM READ/WRITE (NON MASKED)
R	1	1	1	0	X	1	ROW ADDR	COL A2-A8	X	ADDR MASK	BLOCK WRITE TO DRAM (NON MASKED)
R	1	1	1	1	X	0	REFRESH ADDR	X	X	WRITE MASK	LOAD WRITE MASK
R	1	1	1	1	X	1	REFRESH ADDR	X	X	COLOR DATA	LOAD COLOR REGISTER

†R = RANDOM ACCESS OPERATION; T = TRANFER OPERATION
‡DQ0-3 ARE LATCHED ON THE LATER OF W OR CAS FALLING EDGE.
ADDR MASK = 1 WRITE TO ADDRESS LOCATION ENABLED
WRITE MASK = 1 WRITE TO I/O ENABLED

random port to serial port interface

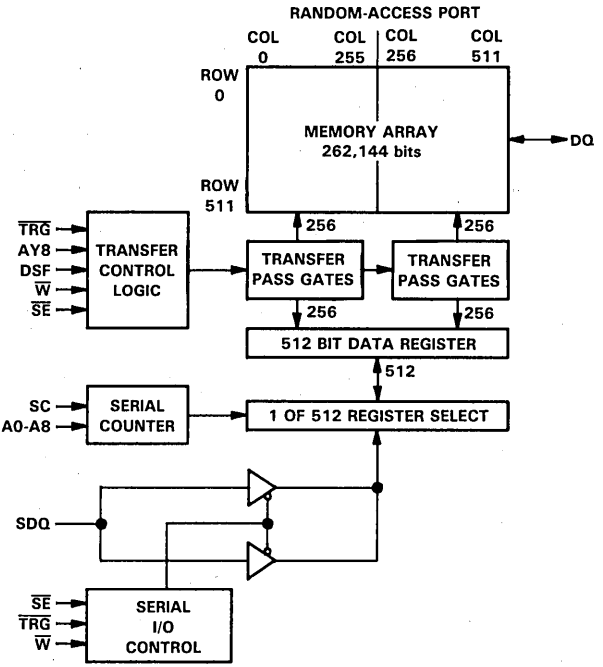

FIGURE 2. BLOCK DIAGRAM SHOWING ONE RANDOM AND ONE SERIAL I/O INTERFACE

random address space to serial address space mapping

The 512 bits in each of the four data registers of the SAM are connected to the 512 column locations of each of the four random I/Os. Data can be accessed in or out of the SAM starting at any of the 512 data bit locations. This start location is selected by addresses A0 through A8 on the falling edge of $\overline{CAS}$ during any transfer cycle. The SAM is accessed starting from the selected start address, proceeding from the lowest to the highest significant bits. After the most significant bit position (511) is accessed, the serial counter wraps around such that bit 0 is accessed on the next clock pulse. The selected start address is stored and used for all subsequent transfer cycles until $\overline{CAS}$ is again brought low during any transfer cycle. Thus, the start address can be set once and $\overline{CAS}$ held high during all subsequent transfer cycles and the start address point will not change regardless of data present on A0 through A8.

split register mode random address to serial address space mapping

In split register transfer operation, the serial data register is split into halves, the low half containing bits 0 through 255 and the high half containing bits 256 through 511. When a split register transfer cycle is performed, the tap address must be strobed in on the falling edge of $\overline{CAS}$. The most significant column address bit (A8) determines which register half will be reloaded from the memory array. The eight remaining column address bits (A0-A7) are used to select the SAM starting location for the register half selected by A8. Thus when bit 255 or 511 is reached, the next bit read out will be from the previously loaded start location.

To guarantee proper operation when using the split register read transfer feature, a non-split register transfer must precede any split register sequence. The serial start address must be supplied for every split register transfer.

transfer operations

As illustrated in Table 1, the TMS44C251 supports five basic transfer modes of operation:

1. Normal Write Transfer (SAM to DRAM)
2. Alternate Write Transfer (independent of the state of $\overline{SE}$)
3. Pseudo Write Transfer (Switches serial port from serial out mode to serial in mode. No actual data transfer takes place between the DRAM and the SAM.)
4. Normal Read Transfer (Transfer entire contents of DRAM to SAM)
5. Split Register Read Transfer (Divides the SAM into a high and a low half. Only one half is transferred to the SAM while the other half is read from the serial I/O port.)

transfer register select ($\overline{TRG}$)

Transfer operations between the memory array and the data registers are invoked by bringing $\overline{TRG}$ low before $\overline{RAS}$ falls. The states of $\overline{W}$, $\overline{SE}$, and DSF, which are also latched on the falling edge of $\overline{RAS}$, determine which transfer operation will be invoked. (See Table 2.)

During read transfer cycles, $\overline{TRG}$ going high causes the addressed row of data to be transferred into the data register. Although the previous data in the data register is overwritten, the last bit of data appearing at SDQ before $\overline{TRG}$ goes high will remain valid until the first positive transition of SC after $\overline{TRG}$ goes high. The data at SDQ will then switch to new data beginning from the selected start, or "tap," position.

transfer write enable ($\overline{W}$)

In register transfer mode, $\overline{W}$ determines whether a read or a write transfer will occur. To perform a write transfer, $\overline{W}$ and $\overline{SE}$ are held low as $\overline{RAS}$ falls. If $\overline{SE}$ is high during this transition, no transfer of data from the data register to the memory array occurs, but the SDQs are put into the input mode. This allows serial data to be input into the SAM. An alternative way to perform the transfer write cycle is by holding DSF high on the falling edge of $\overline{RAS}$. In this way, the state of $\overline{SE}$ is a Don't Care as $\overline{RAS}$ falls. To perform a read transfer operation, $\overline{W}$ is held high and $\overline{SE}$ is a Don't Care as $\overline{RAS}$ falls. This cycle also puts the SDQs into the read mode, allowing serial data to be shifted out of the data register. (See Table 2.)

column enable ($\overline{CAS}$)

If $\overline{CAS}$ is brought low during a control cycle, the address present on the pins A0 through A8 will become the new register start location. If $\overline{CAS}$ is held high during a control cycle, the previous tap address will be retained from the last transfer cycle in which $\overline{CAS}$ went low to set the tap address.

addresses (A0 through A8)

Nine address bits are required to select one of the 512 possible rows involved in the transfer of data to or from the data registers. The states of A0-A8 are latched on the falling edge of $\overline{RAS}$ to select one of 512 rows for the transfer operation.

To select one of the 512 positions in the SAM from which the first serial data will be read out, the appropriate 9-bit column address (A0-A8) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and start (tap) position need not be supplied every cycle, only when changing to a different start position.

In split register transfer mode, the most siginificant column address bit (A8) selects which half of the register will be reloaded from the memory array. The remaining eight addresses (A0-A7) determine the register starting location for the register to be reloaded.

special function input (DSF)

In read transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ selects the split register mode read transfer operation. This mode divides the serial data register into a high order half and a low order half; one active, and one inactive. When the cycle is initiated, a transfer occurs between the memory array and either the high half or the low half register, depending on the state of most significant column address bit (A8) that is strobed in on the falling edge of $\overline{CAS}$. If A8 is high, the transfer is to the high half of the register. If A8 is low, the transfer is to the low half of the register. Use of the split register mode read transfer feature allows on-the-fly read transfer operation without synchronizing $\overline{TRG}$ to the serial clock.

The transfer can be to either the active half or the inactive half register. If the transfer is to the active register, with an uninterrupted serial data stream, then the timings $t_{d(SCTR)}$ and $t_{d(THSC)}$ must be met.

In write transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ permits use of an alternate mode of transfer write. This mode allows $\overline{SE}$ to be high on the falling edge of $\overline{RAS}$ without performing a pseudo write transfer, with the serial port disabled during the entire transfer write cycle.

serial access operation

Refer to Tables 2 and 3 for the following discussion on serial access operation.

serial clock (SC)

Data (SDQ) is accessed in or out of the data registers on the rising edge of SC. The TMS44C251 is designed to work with a wide range of clock duty cycles to simplify system design. Since the data registers comprising the SAM are of static design, there are no SAM refresh requirements and there is no minimum SC clock operating frequency.

serial data input/output (SDQ0-SDQ3)

SD and SQ share a common I/O pin. Data is input to the device when $\overline{SE}$ is low during write mode and data is output from the device when $\overline{SE}$ is low during read mode. The data in the SAM will be accessed in the direction from least significant bit to most significant bit. The data registers operate modulo 512. Thus, after bit 511 is accessed, the next bits to be accessed will be bits 00, 01, 02, and so on.

serial enable ($\overline{SE}$)

The Serial Enable pin has two functions: first, it is latched on the falling edge of $\overline{RAS}$, with both $\overline{TRG}$ and $\overline{W}$ low to select one of the transfer functions (see Table 3). If $\overline{SE}$ is low during this transition, then a transfer write occurs. If $\overline{SE}$ is high as $\overline{RAS}$ falls and DSF is low, then a write mode control cycle is performed. The function of this cycle is to switch the SDQs from the output mode to the input mode, thus allowing data to be shifted into the data register. NOTE: All transfer read and serial mode enable (pseudo transfer write) operations will perform a memory refresh operation on the selected row.

Second, during serial access operations, $\overline{SE}$ is used as an SDQ enable/disable. In the write mode, $\overline{SE}$ is used as an input enable. $\overline{SE}$ high disables the input and $\overline{SE}$ low enables the input. To take the device out of the write mode and into the read mode, a transfer read cycle must be performed. The read mode allows data to be accessed from the data register. While in the read mode, $\overline{SE}$ high disables the output and $\overline{SE}$ low enables the output.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is NOT disabled. Thus, external SC pulses will increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low since the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

split register active status output (QSF)

QSF is an OPEN DRAIN output pin. During the split register mode of serial access operation, QSF indicates which half of the serial register in the SAM is being accessed. If QSF is low, then the serial address pointer is accessing the low (least significant) 256 bits of the SAM. If QSF is high, then the pointer is accessing the higher (most significant) 256 bits of the SAM.

QSF changes state upon crossing the boundary between the two register halves. When the SAM is not operating in split register mode, the QSF output remains in the high-impedance state.

QSF is designed as an open drain output to allow OR-tying of QSF outputs from several chips. Thus, an external pull-up resistor is required for the zero to one transition on QSF and the output risetime is determined by the load capacitance and the value of the pull-up resistor. The specification for QSF switching time assumes a pull-up resistor of 820 ohms and a load capacitance of 50 picofarads.

TABLE 2. TRANSFER OPERATION LOGIC

$\overline{TRG}$	$\overline{W}$	$\overline{SE}$	DSF	MODE
0	0	0	X	Register to memory (write) transfer
0	0	X	1	Alternate register to memory transfer
0	0	1	0	Serial write mode enable
0	1	X	0	Memory to register (read) transfer
0	1	X	1	Split register read transfer

NOTE: Above logic states are assumed valid on the falling edge of $\overline{RAS}$.

TABLE 3. SERIAL OPERATION LOGIC

LAST TRANSFER CYCLE	$\overline{SE}$	SDQ
Alternate register to memory	1	Input Disabled
Serial write mode enable†	0	Input Enable
Serial write mode enable†	1	Input Disable
Memory to register, split register	0	Output Enabled
Memory to register, split register	1	Hi-Z

†Pseudo transfer write

power up

After power up, the power supply must remain at its steady-state value for 1 μs. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing two $\overline{RAS}$ cycles before proper device operation is achieved.

absolute maximum ratings over operating free-air temperature†

Voltage on any pin except DQ and SDQ (see Note 1) . . . . . −1.0 V to 7.0 V
Voltage on DQ and SDQ (see Note 1) . . . . . −1.0 V to V_{CC}
Voltage range on V_{CC} (see Note 1) . . . . . 0.0 V to 7 V
Short circuit output current (per output) . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage		0.0		V
V_{IH}	High-level input voltage	2.4		V_{CC}	V
V_{IL}	Low-level input voltage (see Note 2)	−1.0		0.8	V
V_{OH}	High-level output voltage	2.4		V_{CC}	V
V_{OL}	Low-level output voltage	−1.0		0.4	V
T_A	Operating free-air temperature	0	25	70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS44C251-10		TMS44C251-12		TMS44C251-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High level output voltage	I_{OH} = −5.0 mA	2.4		2.4		2.4		V
V_{OL}	Low level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
$V_{OL(QSF)}$	QSF low level output voltage	$I_{OL(QSF)}$ = 6 mA		0.4		0.4		0.4	V
I_L	Input leakage current	V_I = 0 V to 5.8 V V_{CC} = 5.5 V All other pins = 0 V to V_{CC}		±10		±10		±10	μA
I_O	Output current leakage	V_O = 0 V to V_{CC} V_{CC} = 5.5 V		±10		±10		±10	μA

PARAMETER		SAM PORT	TMS44C251-10		TMS44C251-12		TMS44C251-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
I_{CC1}	Operation current $t_{c(RW)}$ = Minimum	Standby		90		80		70	mA
I_{CC1A}	$t_{c(SC)}$ = Minimum	Active		110		95		85	
I_{CC2}	Standby current All Clocks = V_{CC}	Standby		5		5		5	
I_{CC2A}	$t_{c(SC)}$ = Minimum	Active		35		30		30	
I_{CC3}	$\overline{RAS}$-only refresh current $t_{c(RW)}$ = Minimum	Standby		90		80		70	
I_{CC3A}	$t_{c(SC)}$ = Minimum	Active		110		95		85	
I_{CC4}	Page mode current $t_{c(P)}$ = Minimum	Standby		50		45		40	
I_{CC4A}	$t_{c(SC)}$ = Minimum	Active		60		55		50	
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ current $t_{c(RW)}$ = Minimum	Standby		80		70		65	
I_{CC5A}	$t_{c(SC)}$ = Minimum	Active		110		95		85	
I_{CC6}	Data transfer current $t_{c(RW)}$ = Minimum	Standby		90		80		70	
I_{CC6A}	$t_{c(SC)}$ = Minimum	Active		110		95		85	

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(DSF)}$	Input capacitance, special function		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
C_{oO}	Output capacitance, SDQ and DQ		7	pF
$C_{o(QSF)}$	Output capacitance, QSF		10	pF

NOTE 3: V_{CC} equal to 5.0 V ± 0.5 V and the bias on pins under test is 0.0 V.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Note 4)

PARAMETER		TEST CONDITION	ALT. SYMBOL	TMS44C251-10		TMS44C251-12		TMS44C251-15		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		25		30		35	ns
$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{CAA}		50		60		75	ns
$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = MAX	t_{CAP}		55		65		80	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MAX	t_{RAC}		100		120		150	ns
$t_{a(G)}$	Access time of Q from $\overline{TRG}$ low		t_{OEA}		25		35		45	ns
$t_{a(SQ)}$	Access time of SQ from SC high	C1 = 50 pF	t_{SCA}		30		35		40	ns
$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C1 = 50 pF	t_{SEA}		20		25		30	ns
$t_{a(QSF)}$	Access time of QSF from SC high	C1 = 50 pF See Figure 3			60		60		60	ns
$t_{dis(CH)}$	Random output disable time from $\overline{CAS}$ high	C1 = 100 pF	t_{OFF}	0	25	0	30	0	35	ns
$t_{dis(G)}$	Random output disable time from $\overline{TRG}$ high	C1 = 100 pF	t_{OEZ}	0	25	0	30	0	35	ns
$t_{dis(SE)}$	Serial output disable time from $\overline{SE}$ high	C1 = 50 pF	t_{SEZ}		20		20		25	ns

NOTE 4: Switching times assume C1 = 100 pF unless otherwise noted.

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timing requirements over recommended supply voltage range and operating free-air temperature range†

		ALT. SYMBOL	TMS44C251-10		TMS44C251-12		TMS44C251-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 5)	t_{RC}	190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		260		ns
$t_{c(rdW)}$	Read-modify-write cycle time	t_{RWC}	265		305		355		ns
$t_{c(P)}$	Page-mode read, write cycle time	t_{PC}	60		70		90		ns
$t_{c(RDWP)}$	Page-mode read-modify-write cycle time	t_{RWC}	125		150		180		ns
$t_{c(TRD)}$	Transfer read cycle time	t_{RC}	190		220		260		ns
$t_{c(TW)}$	Transfer write cycle time	t_{WC}	190		220		260		ns
$t_{c(SC)}$	Serial clock cycle time	t_{SCC}	30		35		40		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	20		25		35		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 6)	t_{CAS}	25	75,000	35	75,000	40	75,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	80		90		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 7)	t_{RAS}	100	75,000	120	75,000	150	75,000	ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	t_{WP}	25		25		35		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		25		35		40		ns
$t_{w(SCH)}$	Pulse duration, SC high	t_{SC}	10		12		15		ns
$t_{w(SCL)}$	Pulse duration, SC low	t_{SCP}	10		12		15		ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		0		ns
$t_{su(SFC)}$	DSF setup time before $\overline{CAS}$ low		0		0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		0		ns
$t_{su(WMR)}$	$\overline{W}$ setup time before $\overline{RAS}$ low	t_{WSR}	0		0		0		ns
$t_{su(DQR)}$	DQ setup time before $\overline{RAS}$ low	t_{MS}	0		0		0		ns
$t_{su(TRG)}$	$\overline{TRG}$ setup time before $\overline{RAS}$ low	t_{TLS}	0		0		0		ns
$t_{su(SE)}$	$\overline{SE}$ setup time before $\overline{RAS}$ low	t_{ESR}	0		0		0		ns
$t_{su(SFR)}$	DSF setup time before $\overline{RAS}$ low		0		0		0		ns
$t_{su(DCL)}$	Data setup time before $\overline{CAS}$ low	t_{DSC}	0		0		0		ns
$t_{su(DWL)}$	Data setup time before $\overline{W}$ low	t_{DSW}	0		0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		−5		ns
$t_{su(WCH)}$	Write setup time before $\overline{CAS}$ high	t_{CWL}	25		30		35		ns
$t_{su(WRH)}$	Write setup time before $\overline{RAS}$ high with $\overline{TRG}$ = $\overline{W}$ = low	t_{RWL}	35		40		45		ns
$t_{su(SDS)}$	SD setup time before SC high	t_{SDS}	3		3		3		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		25		ns
$t_{h(SFC)}$	DSF hold time after $\overline{CAS}$ low		20		20		25		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		20		ns
$t_{h(TRG)}$	$\overline{TRG}$ hold time after $\overline{RAS}$ low	t_{TLH}	15		15		20		ns
$t_{h(SE)}$	$\overline{SE}$ hold time after $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low	t_{REH}	15		15		20		ns
$t_{h(RWM)}$	Write mask, transfer enable hold time after $\overline{RAS}$ low	t_{RWH}	15		15		20		ns

Continued next page.

†Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 5. All cycle times assume t_t = 5 ns.

6. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).
7. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range† (continued)

		ALT. SYMBOL	TMS44C251-10		TMS44C251-12		TMS44C251-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(RDQ)}$	DQ hold time after $\overline{RAS}$ low (write mask operation)	t_{MH}	15		15		20		ns
$t_{h(SFR)}$	DSF hold time after $\overline{RAS}$ low		15		15		20		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low (see Note 8)	t_{AR}	45		45		55		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	25		30		40		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 8)	t_{DHR}	50		55		70		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	25		30		40		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ (see Note 9)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ (see Note 9)	t_{RRH}	10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	25		35		45		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low	t_{WCR}	50		60		75		ns
$t_{h(WLG)}$	$\overline{TRG}$ hold time after $\overline{W}$ low (see Note 10)	t_{OEH}	25		30		40		ns
$t_{h(SDS)}$	SD hold time after SC high	t_{SDH}	5		5		5		ns
$t_{h(SHSQ)}$	SQ hold time after SC high	t_{SOH}	10		10		10		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time $\overline{CAS}$ low to $\overline{RAS}$ high, write (see Note 11)	t_{RSH}	35		40		45		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Notes 12 and 13)	t_{CWD}	60		75		90		ns
$t_{d(RLCL)}$	Delay time, $\overline{CAS}$ low to $\overline{CAS}$ low (see Notes 14 and 15)	t_{RCD}	25	75	25	85	30	110	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	50		60		75		ns
$t_{d(CACH)}$	Delay time, column address to $\overline{CAS}$ high	t_{CAL}	50		60		75		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 12)	t_{RWD}	135		160		195		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 12)	t_{AWD}	85		100		120		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	25		25		30		ns
$t_{d(CLRL)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		15		ns
$t_{d(RHCL)}$	Delay time $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RCP}	5		5		5		ns
$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high	t_{CTH}	25		35		40		ns

Continued next page.

†Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 8. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
9. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
10. Output Enable controlled write. Output remains in the high-impedance state for the entire cycle.
11. Write cycles only.
12. Read-modify write operation only.
13. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
14. Read cycles only.
15. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.

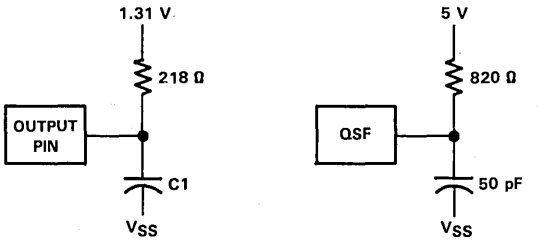
timing requirements over recommended supply voltage range and operating free-air temperature range† (concluded)

			ALT. SYMBOL	TMS44C251-10 MIN	TMS44C251-10 MAX	TMS44C251-12 MIN	TMS44C251-12 MAX	TMS44C251-15 MIN	TMS44C251-15 MAX	UNIT
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ			25		30		30		ns
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (see Notes 17 and 18)	Early load	t_{RTH}	$t_{h(TRG)}$		$t_{h(TRG)}$		$t_{h(TRG)}$		ns
		Mid-line real-time load		70		80		95		
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 18)		t_{RSD}	85		95		115		ns
$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 18)		t_{CSD}	40		45		55		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 18 and 19)		t_{TSL}	10		10		15		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 18)			−10		−10		−15		ns
$t_{d(SCRL)}$	Delay time, SC high to $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low (see Notes 20 and 21)		t_{SRS}	10		10		15		ns
$t_{d(SCSE)}$	Delay time, SC high to $\overline{SE}$ high in serial input mode		t_{SRD}	20		20		25		ns
$t_{d(RHSC)}$	Delay time, $\overline{RAS}$ high to SC high (see Note 21)		t_{TRP}	25		30		45		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 22)		t_{TSD}	$t_{w(RH)}$		$t_{w(RH)}$		$t_{w(RH)}$		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 22)		t_{SWS}	10		10		15		ns
$t_{d(SESC)}$	Delay time, $\overline{SE}$ low to SC high (see Note 23)			25		25		30		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split read transfer cycles			25		30		40		ns
$t_{d(TPRL)}$	Delay time, first (TAP) rising edge of SC after boundary switch to $\overline{RAS}$ low during split read transfer cycles			20		25		30		ns
$t_{rf(MA)}$	Refresh time interval, memory		t_{REF}		8		8		8	ms
t_t	Transition time		t_T	3	50	3	50	3	50	ns

†Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 17. $\overline{TRG}$ may be brought high "early" when real time memory to register data transfer is not required, provided that the $t_{h(TRG)}$, $t_{d(SCTR)}$, and $t_{d(RLSH)}$ specifications are met.
18. Memory to register (read) transfer cycles only.
19. In a transfer read cycle, the state of SC when $\overline{TRG}$ rises is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high.
20. In a transfer write cycle, the state of SC when $\overline{RAS}$ falls is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{RAS}$ goes low.
21. Register to memory (write) transfer cycles only.
22. Memory to register (read) and register to memory (write) transfer cycles only.
23. Serial data-in shift cycles only.

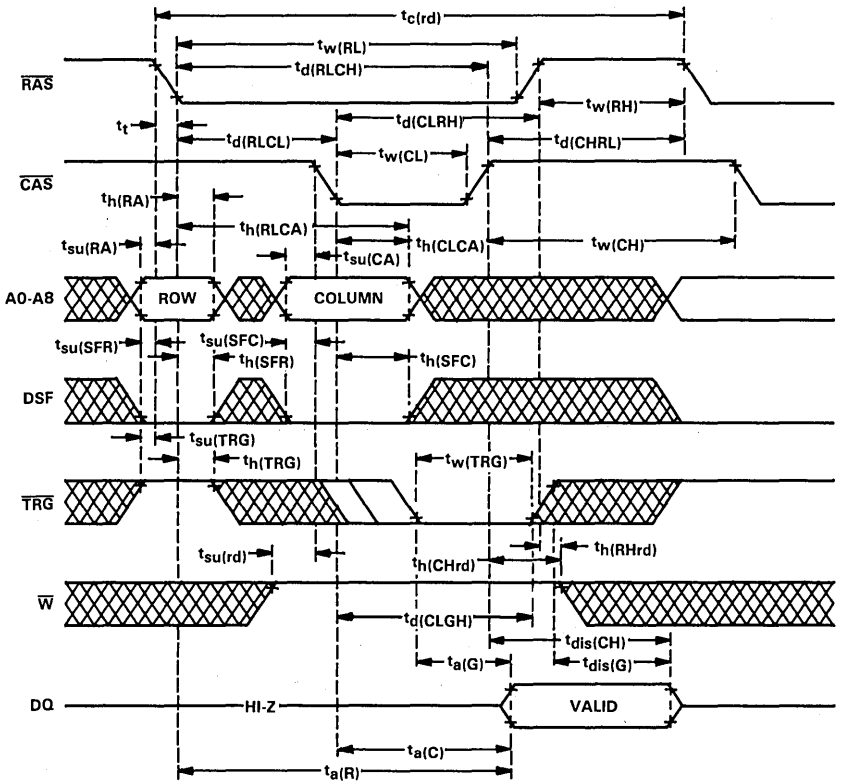
PARAMETER MEASUREMENT INFORMATION



a) LOAD CIRCUIT EXCEPT QSF b) QSF LOAD CIRCUIT

FIGURE 3. LOAD CIRCUIT

read cycle timing



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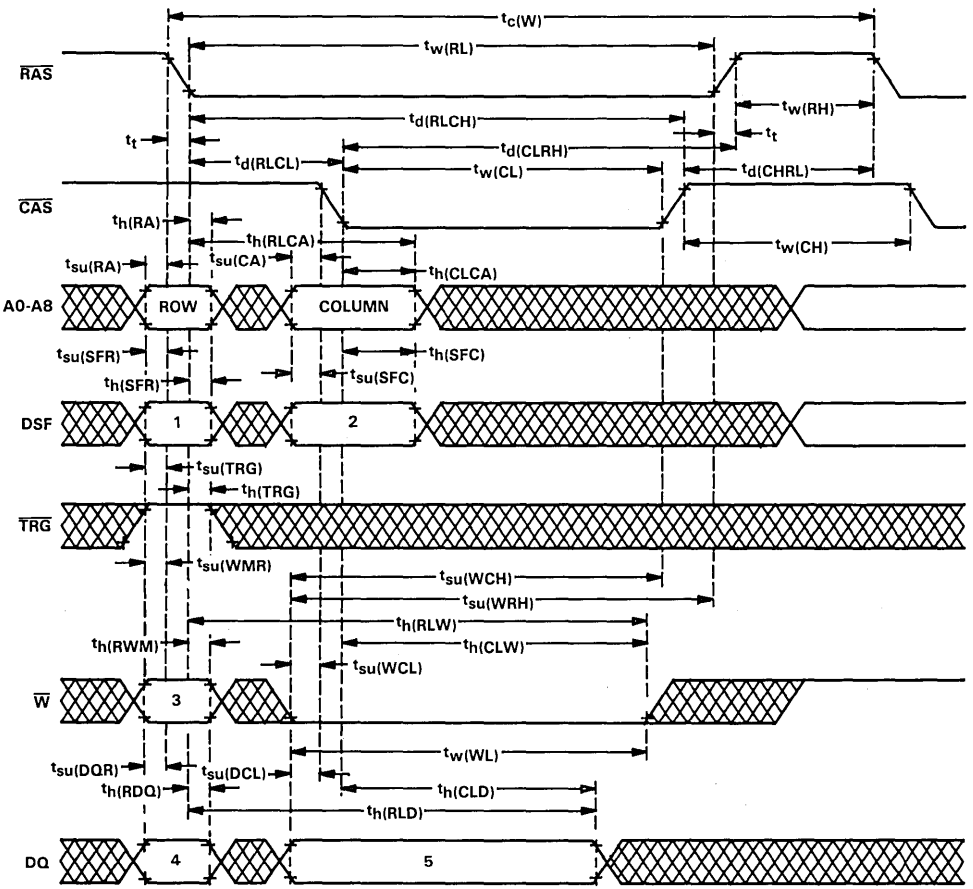
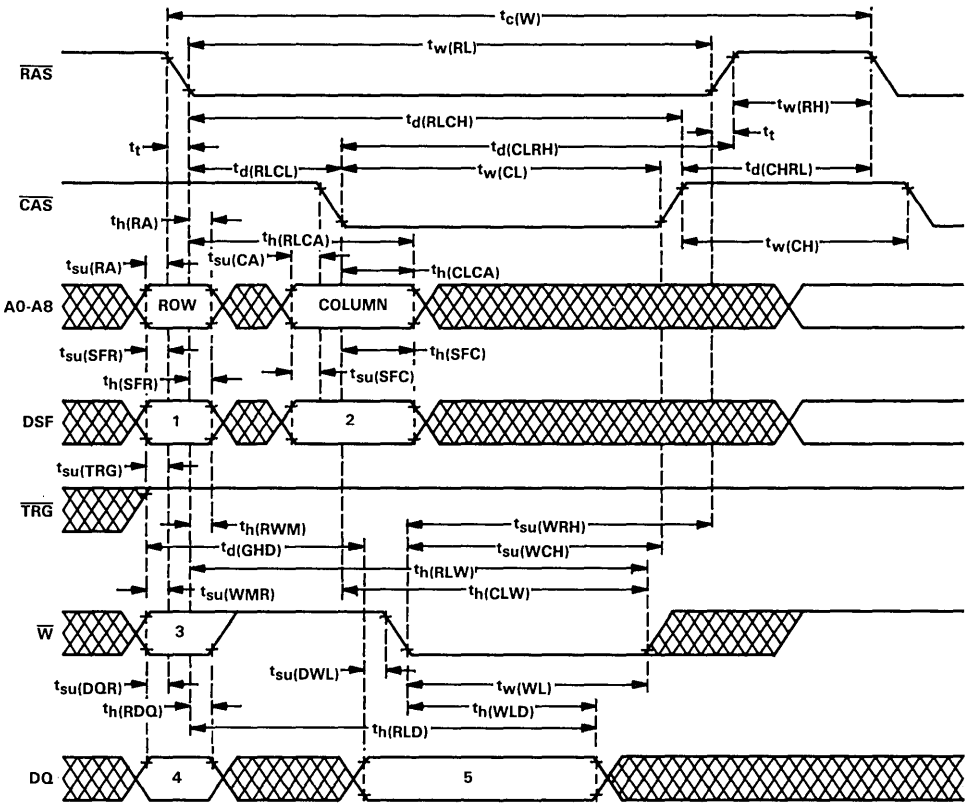
early write cycle timing



NOTE 24: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

delayed write cycle timing

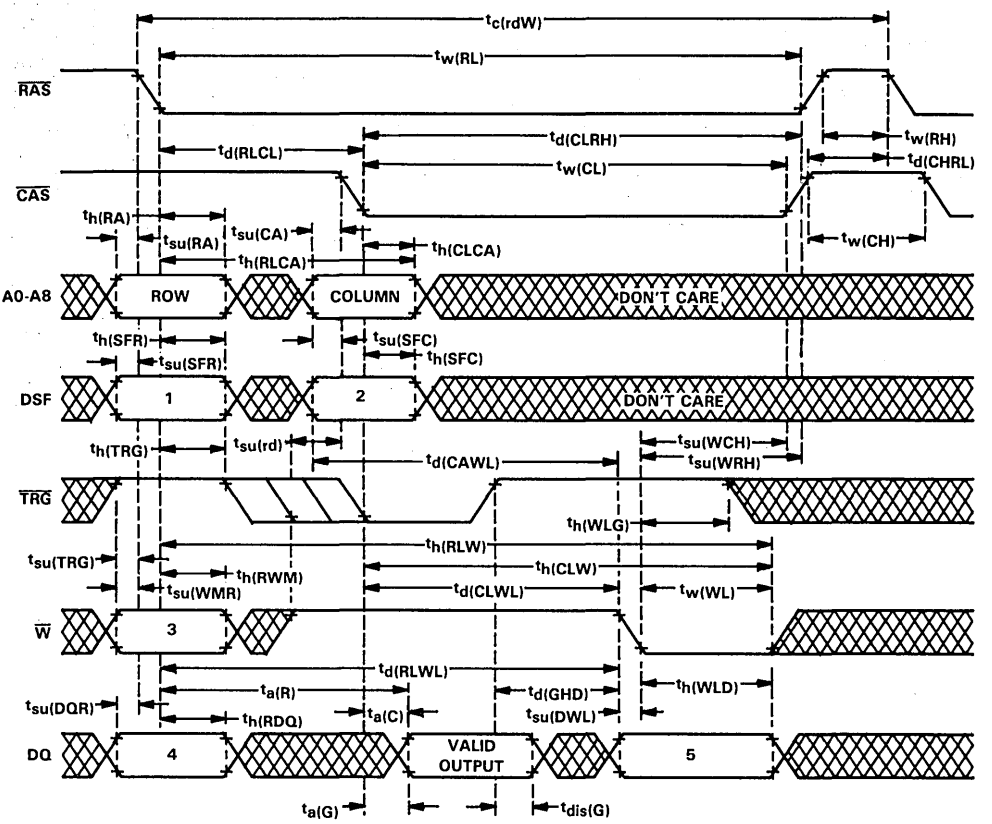


NOTE 24: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

write cycle state table

CYCLE	STATE				
	1	2	3	4	5
Write mask load/use Write DQs to I/Os	0	0	0	WRITE MASK	VALID DATA
Write mask load/use Block write	0	1	0	WRITE MASK	ADDR MASK
Use previous write mask Write DQs to I/Os	1	0	0	DON'T CARE	VALID DATA
Use previous write mask Block write	1	1	0	DON'T CARE	ADDR MASK
Load write mask on later of $\overline{W}$ fall and $\overline{CAS}$ fall	1	0	1	DON'T CARE	WRITE MASK
Load color register on later of $\overline{W}$ fall and $\overline{CAS}$ fall	1	1	1	DON'T CARE	COLOR DATA
Write mask disabled, Block write to all I/Os	0	1	1	DON'T CARE	ADDR MASK
Normal early or late Write operation	0	0	1	DON'T CARE	VALID DATA

read-write/read-modify-write cycle timing



NOTE 25: See "Write Cycle State Table" for logic state of "1", "2", "3", "4", and "5". Same logic as delayed write cycle.

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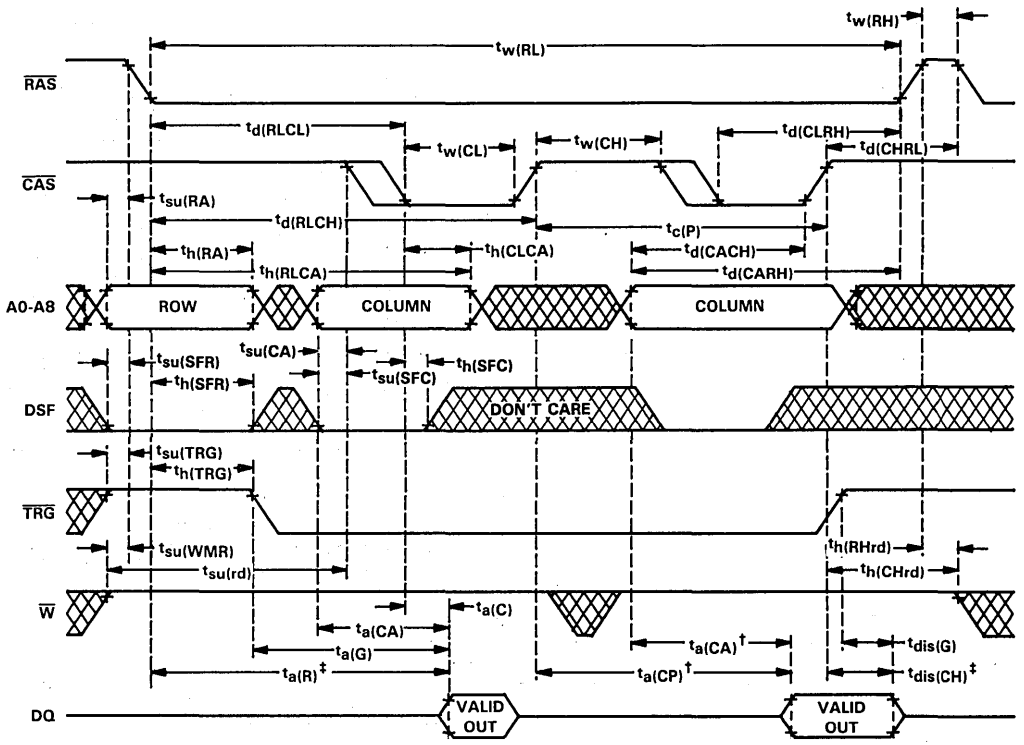
enhanced page-mode read cycle timing

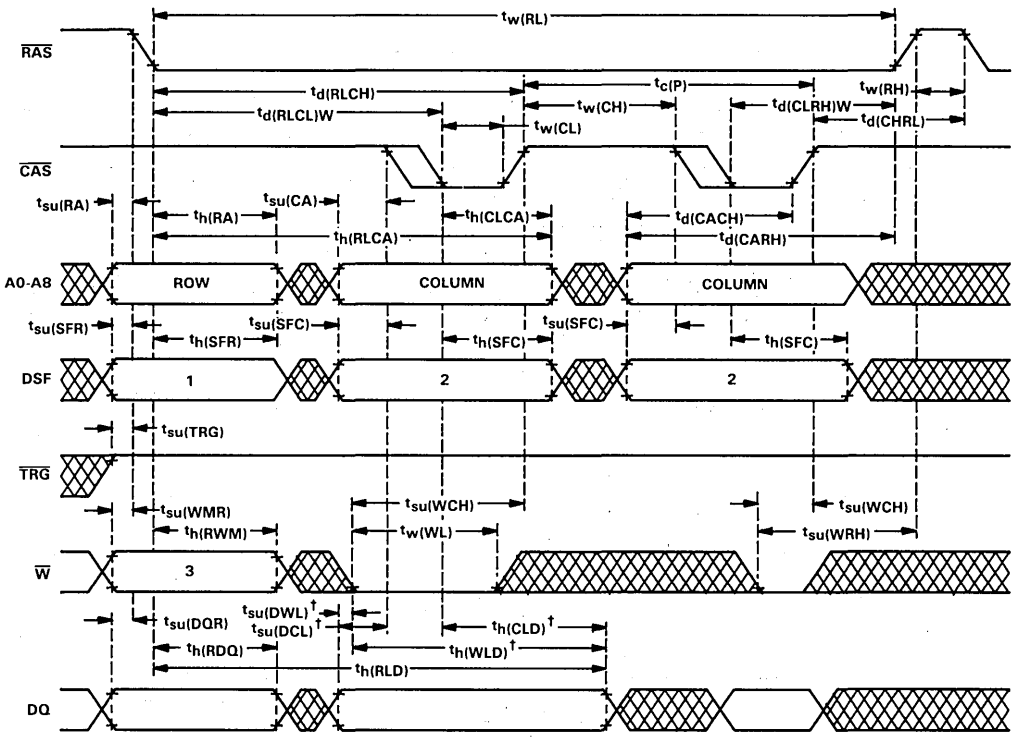


NOTE 26: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edges of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.).

†Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

‡Output may go from the high-impedance state to an invalid data state prior to the specified access time.

enhanced page mode write cycle timing

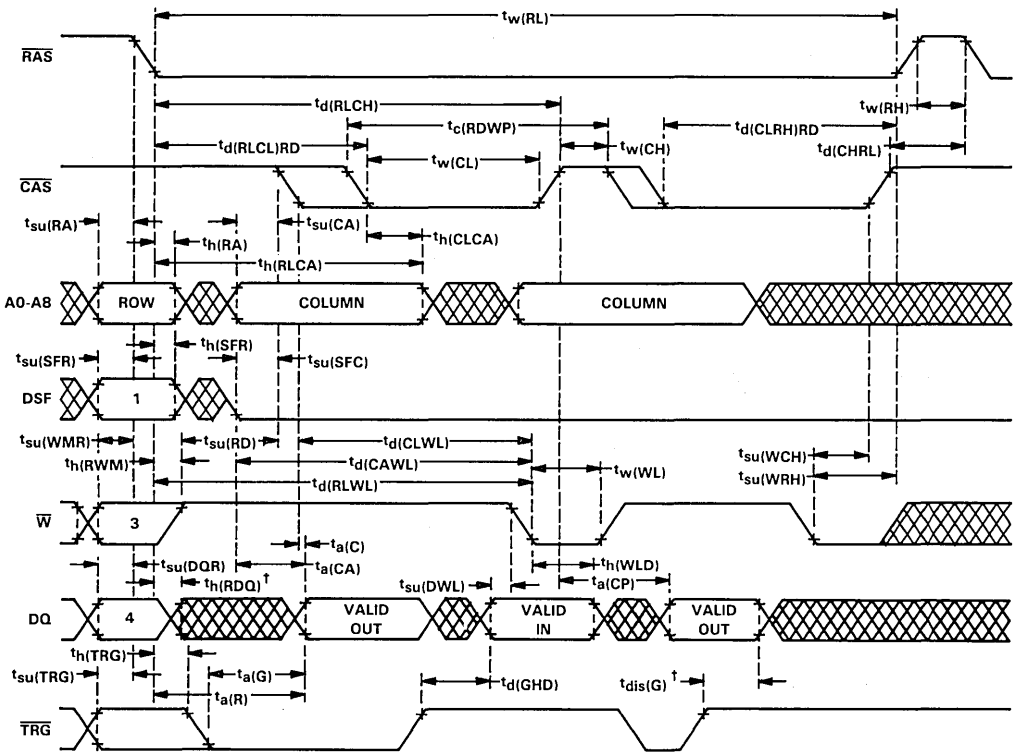


NOTES: 24. See "Write Cycle State Table" for logic state of "1", "2", "3", "4", and "5".

27. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used, to guarantee page-mode cycle time. If the early write cycle timing is used, the state of $\overline{TRG}$ is a Don't Care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

†Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

enhanced page-mode read-modify-write cycle timing

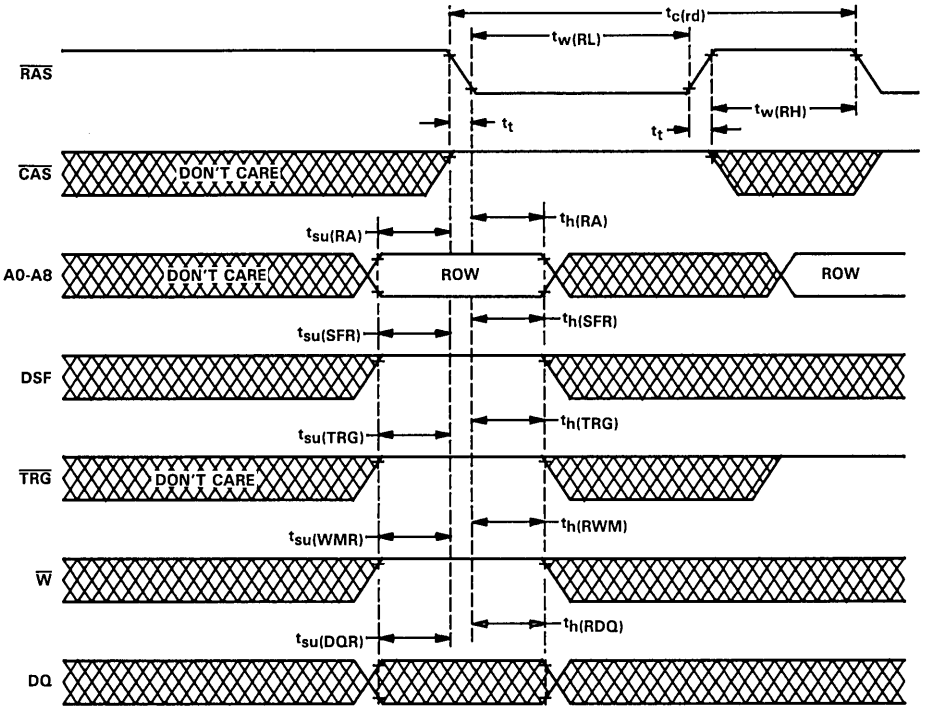


NOTES: 24. See "Write Cycle State Table" for logic state of "1", "2", "3", "4", and "5".

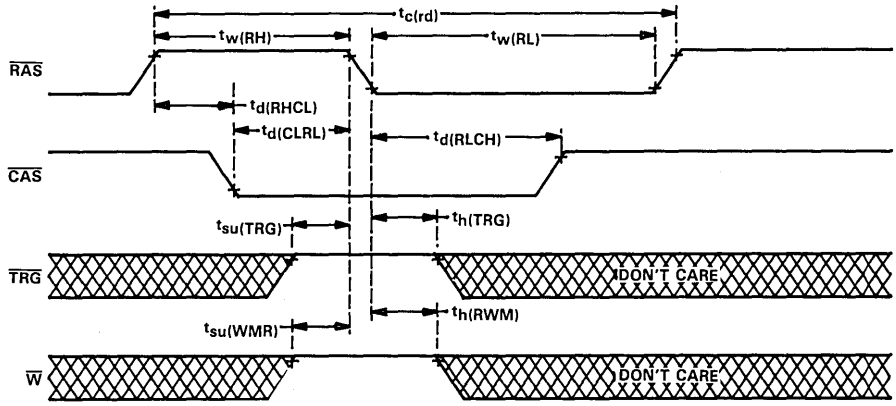
28. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

†Output may go from the high-impedance state to an invalid data state prior to the specified access time.

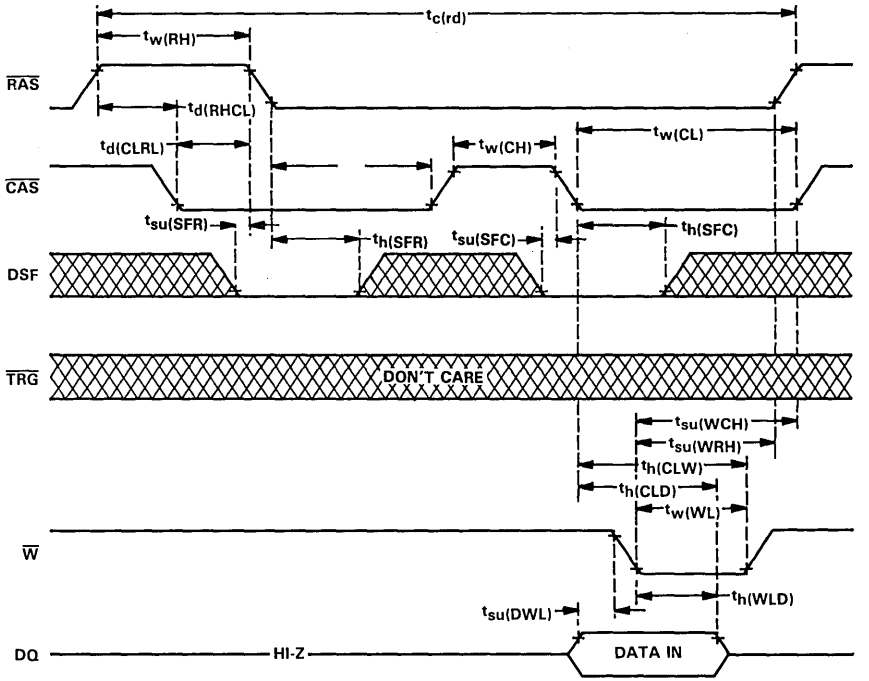
$\overline{RAS}$-only refresh timing



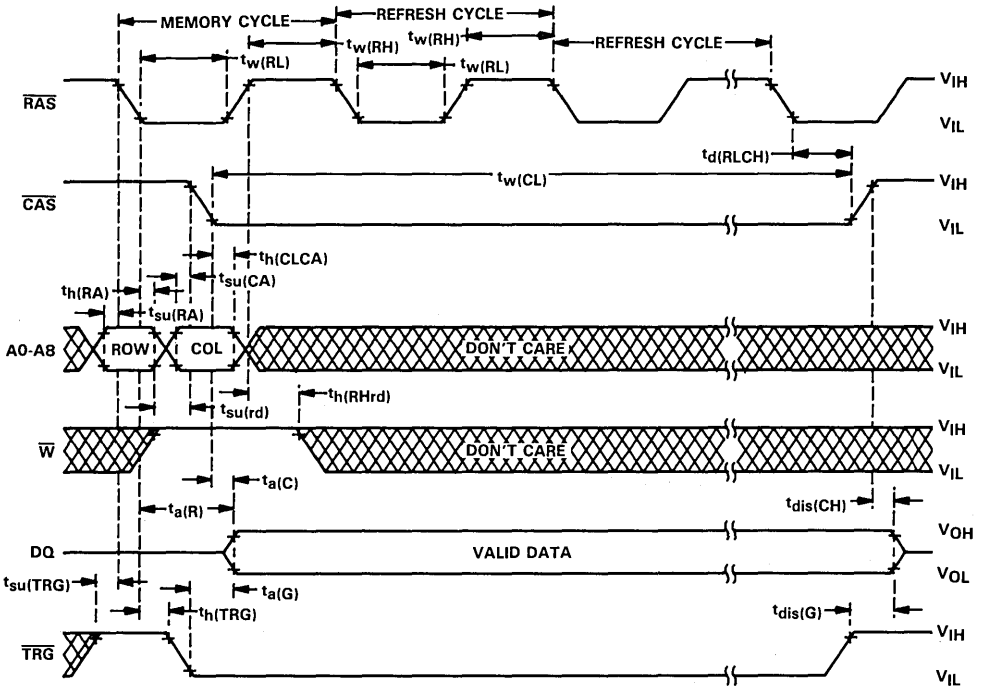
$\overline{CAS}$-before-$\overline{RAS}$ refresh



$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test timing

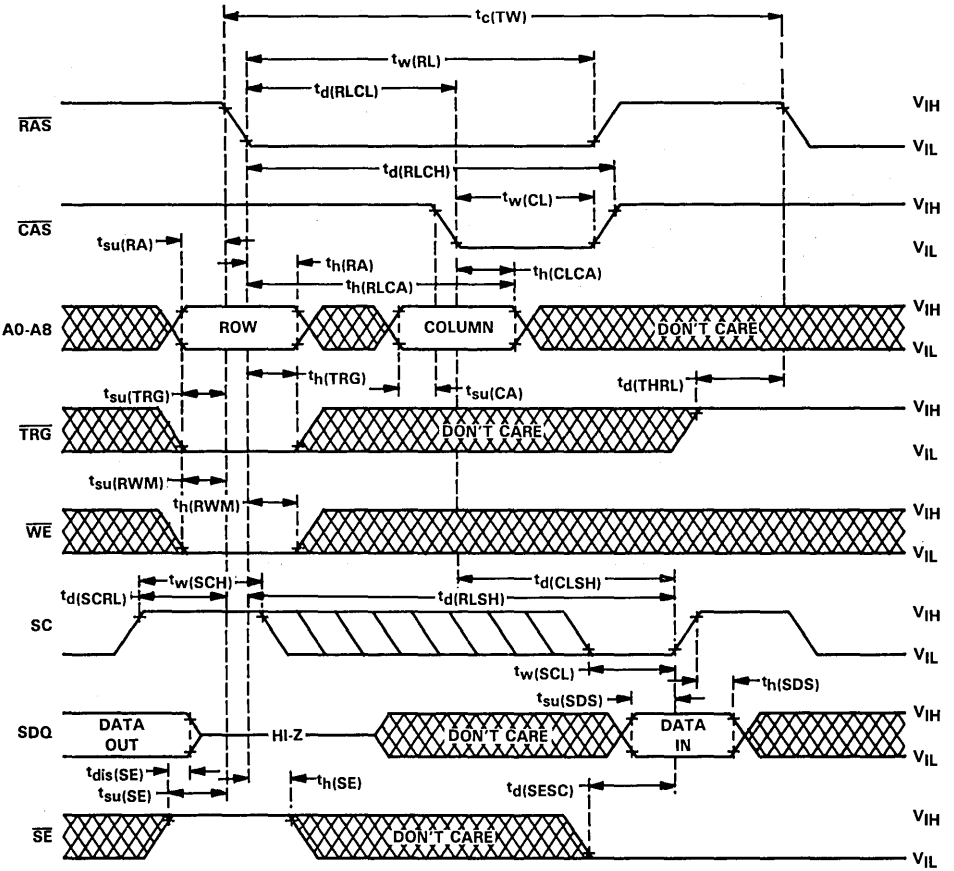


hidden refresh cycle timing



write-mode control pseudo write transfer timing

The write-mode control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. The diagram below assumes that the device was originally in the serial read mode.



NOTES: 29. Random-mode Q outputs remain in the high-impedance state for the entire write-mode control.
30. $\overline{SE}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

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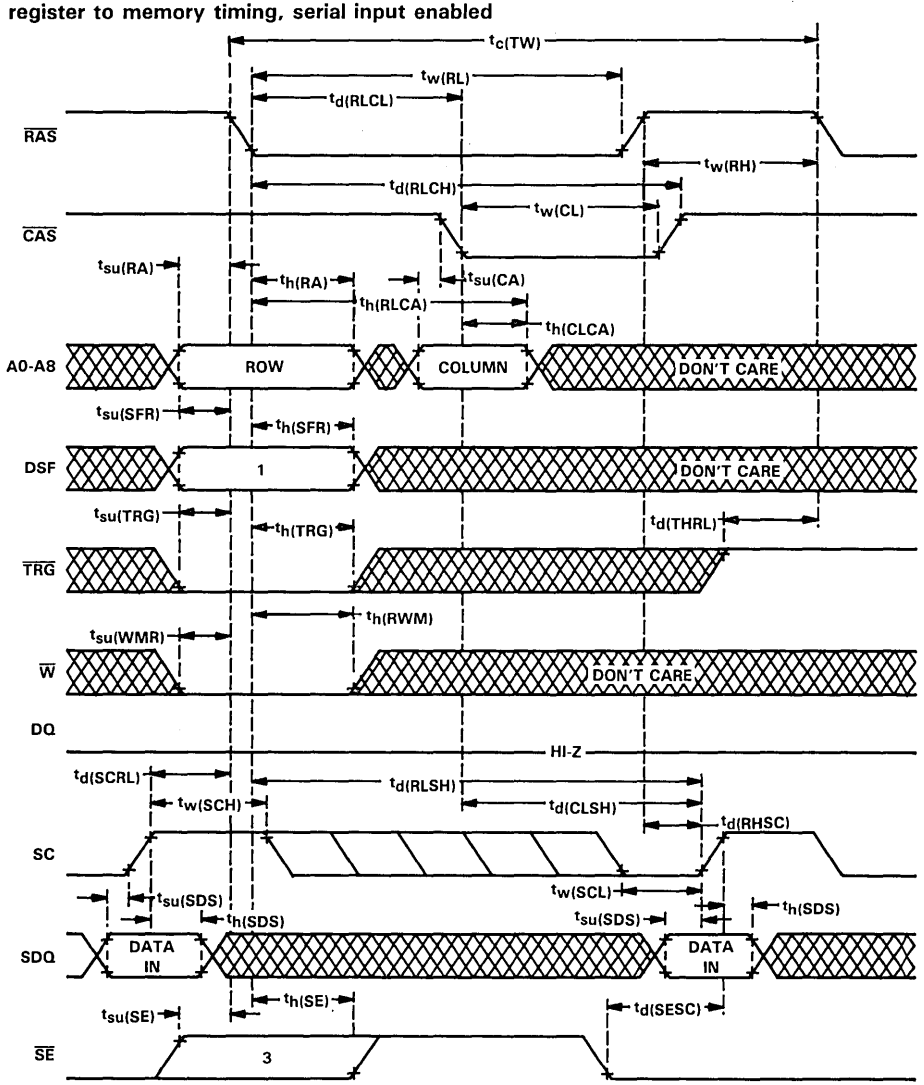
data register to memory timing, serial input enabled



NOTES: 31. Random mode Q outputs remain in the high-impedance state for the entire data register to memory transfer cycle. This cycle is used to transfer data from the data register to the memory array. Every one of the 512 locations in each data register is written into the corresponding 512 columns of the selected row. Data in the data register may proceed from a serial shift-in or from a parallel load from one of the memory array rows. The above diagram assumes that the device is in the serial write mode (i.e., SD is enabled by a previous write mode control cycle, thus allowing data to be shifted-in).

32. See "Register Transfer Functions Table" for logic state of "1" and "3".

register transfer functions table

FUNCTION	$\overline{RAS}$ FALL			
	$\overline{TRG}$	$\overline{W}$	DSF (1)	$\overline{SE}$ (3)
Register to memory transfer	0	0	X	0
Register to memory transfer	0	0	1	X
Pseudo-transfer SDQ control	0	0	X	1
Memory to register transfer	0	1	0	X
Split register transfer	0	1	1	X

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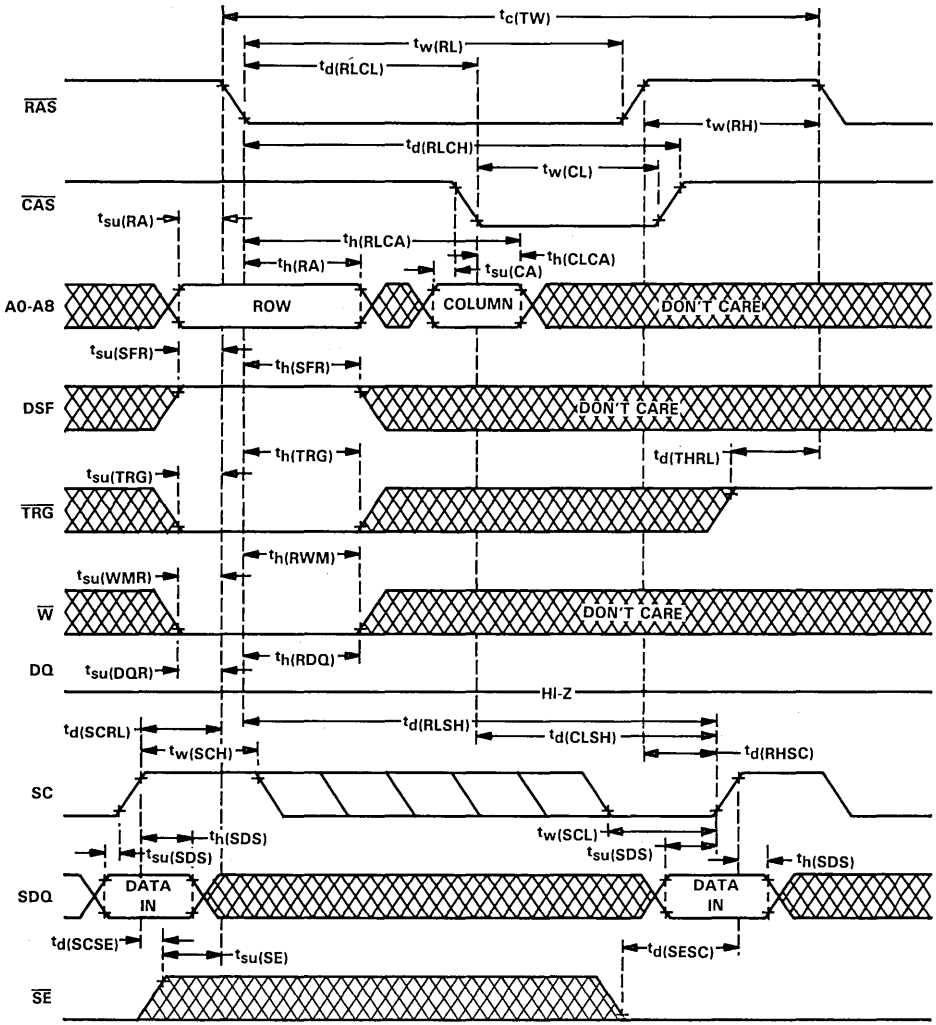
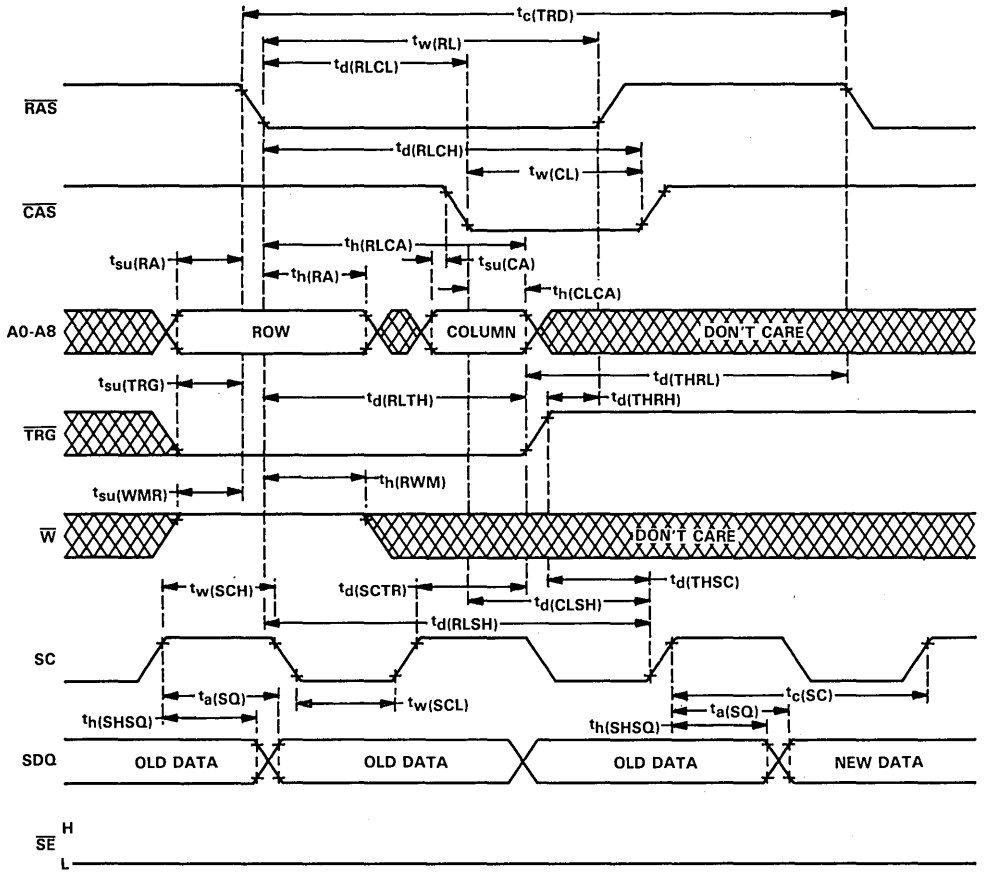
alternate data register to memory timing



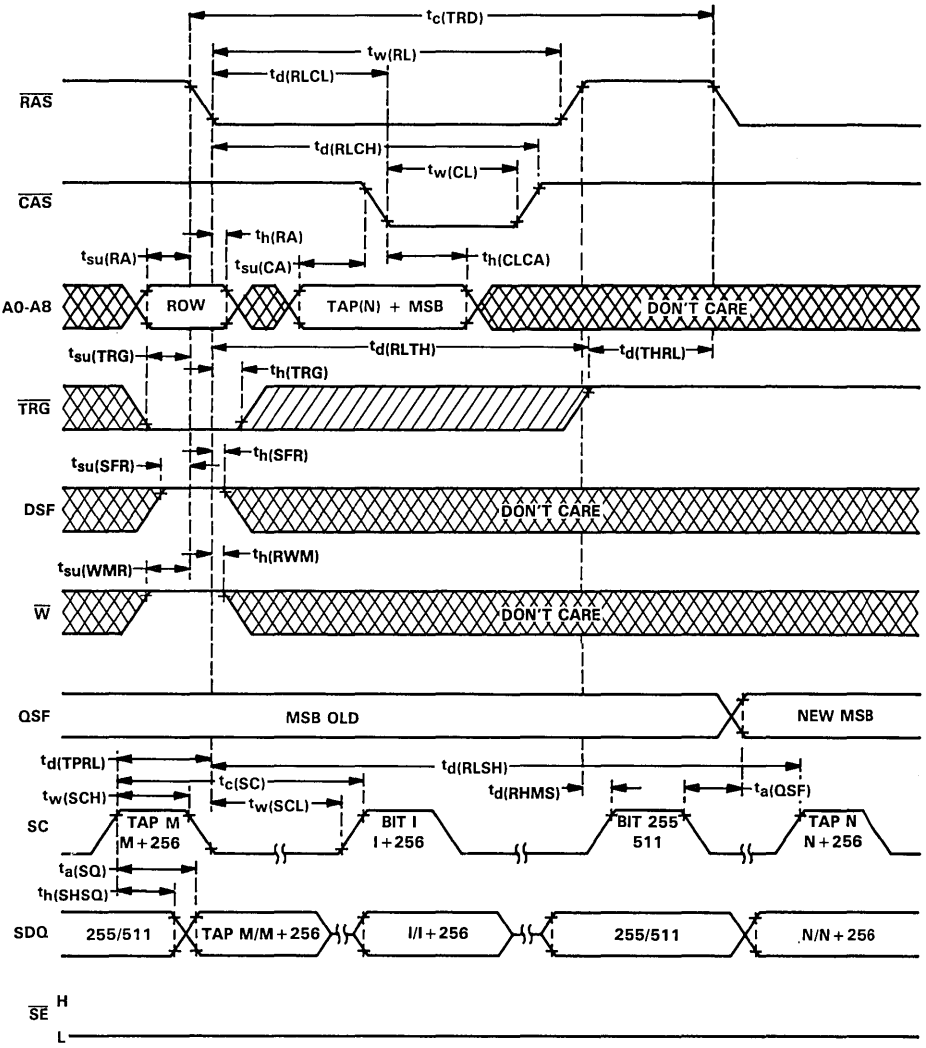
memory to data register transfer timing



NOTES: 33. Random mode (Q outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written into from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

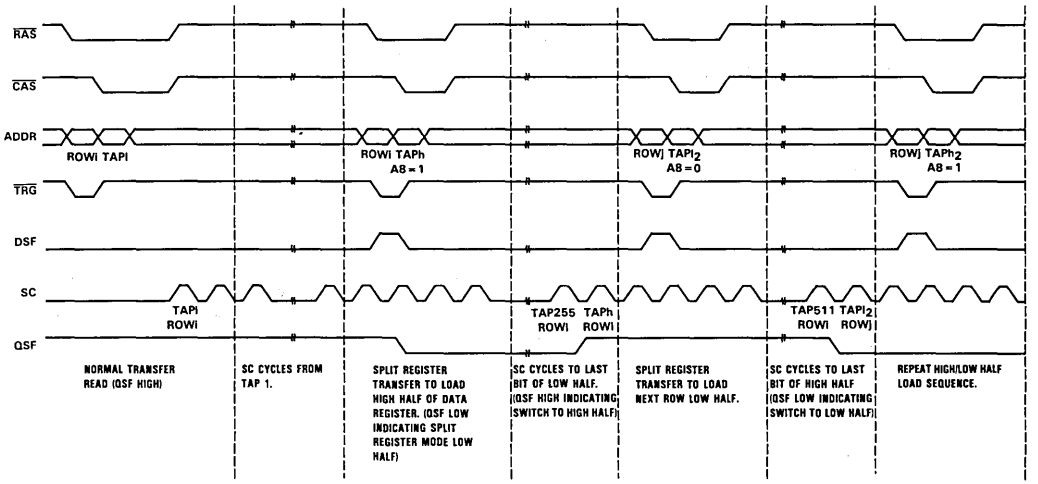
34. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

split register mode read transfer timing



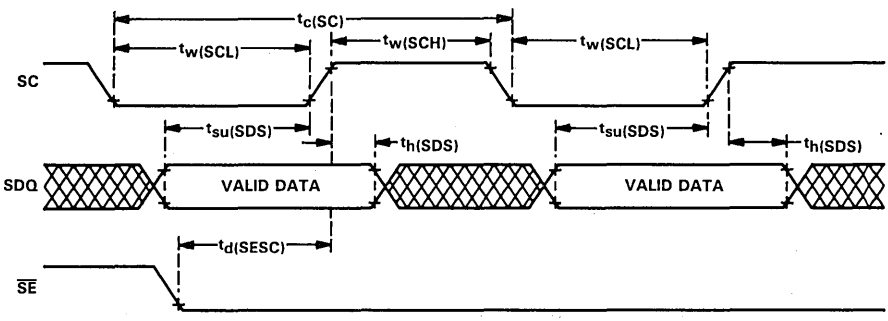
NOTE 35: There must be a minimum of one SC clock cycle between any two split register reload cycles.

split register operating sequence



NOTE 36: In split register mode, data can be transferred from different rows to the low and high halves of the data register.

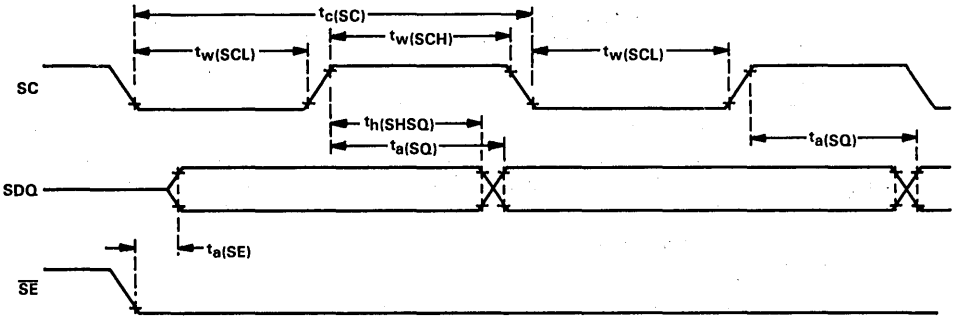
serial data-in timing



The Serial Data-in cycle is used to input serial data into the data registers. Before data can be written into the data registers via SD, the device must be put into the write mode by performing a write mode control, or pseudo-transfer, cycle. Transfer write cycles occurring between the write mode control cycle and the subsequent writing or data will not take the device out of the write mode. However, a transfer read cycle during that time will take the device out of the write mode and put it into the read mode, thus disabling the input of data. Data will be written starting at the location specified by the input address loaded on the previous transfer cycle.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.

serial data-out timing



NOTE 37: While reading data through the serial data register, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register to memory or memory to register data transfer operation.

The Serial Data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle. Transfer write cycles occurring between the transfer read cycle and the subsequent shifting out of data will not take the device out of the read mode. But a write mode control cycle at that time will take the device out of the read mode and put it in the write mode, thus not allowing the reading of data.

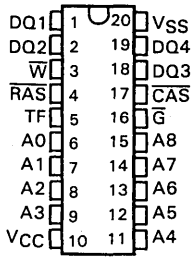
JUNE 1986 – REVISED MAY 1988

- 262,144 × 4 Organization
- Single 5-V Supply (10% Tolerance)
- Performance Ranges:

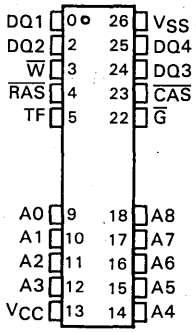
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS44C25_-10	100 ns	25 ns	45 ns	190 ns
TMS44C25_-12	120 ns	30 ns	55 ns	220 ns
TMS44C25_-15	150 ns	40 ns	70 ns	260 ns

- TMS44C256 – Enhanced Page Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- TMS44C257 – Static Column Decode Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)
- 3-State Unlatched Output
- Lower Power Dissipation
- Texas Instruments EPIC™ CMOS Process
- All Inputs and Clocks Are TTL Compatible
- High-Reliability Plastic 20-Pin 300-Mil-Wide DIP or 20/26-Lead Surface Mount (SOJ) Package
- Operation of TI's Megabit CMOS DRAMs Can Be Controlled by TI's SN74ALS6301 and SN74ALS6302 Dynamic RAM Controllers
- Operating Free-Air Temperature . . . 0°C to 70°C

N PACKAGE
(TOP VIEW)



DJ PACKAGE†
(TOP VIEW)



†The packages shown here are for pinout reference only. The DJ package is actually 75% of the length of the N package.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Data-Output Enable
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS44C256 and TMS44C257 series are high-speed, 1,048,576-bit Dynamic Random-Access Memories organized as 262,144 words of four bits each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

operation

enhanced page mode (TMS44C256)

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and

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the $\overline{CAS}$ page-mode cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS44C256 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page mode." Valid column address may be presented immediately after $t_{h(RA)}$ (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

static column decode mode (TMS44C257)

The static column decode mode of operation allows high-speed read, write, or read-modify-write by reducing the number of required signal setup, hold, and transition timings. This is achieved by first addressing the row and column in the normal manner, but after the first access maintain $\overline{CAS}$ low. Subsequently changing the column address produces valid data at the $t_{a(CA)}$. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. Similarly, write or read-modify-write cycle times can be achieved with appropriate toggling of $\overline{W}$. The addresses are latched during the write operation, but at the completion of the internal write operation the addresses are unlatched.

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. The TMS44C256 $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffers. The TMS44C257 column addresses are latched only on write cycles with the later of the $\overline{CAS}$ or $\overline{W}$ falling edge.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation with $\overline{G}$ grounded. The TMS44C257 latches the column addresses on write cycles with the later of $\overline{CAS}$ or $\overline{W}$ falling edge.

data in (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{G}$ are brought low. In a read cycle the output becomes valid after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying $t_{d(GHD)}$.

output enable ($\overline{G}$)

$\overline{G}$ controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0-A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter $t_{d(CLRL)R}$] and holding it low after $\overline{RAS}$ falls [see parameter $t_{d(RLCH)R}$]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

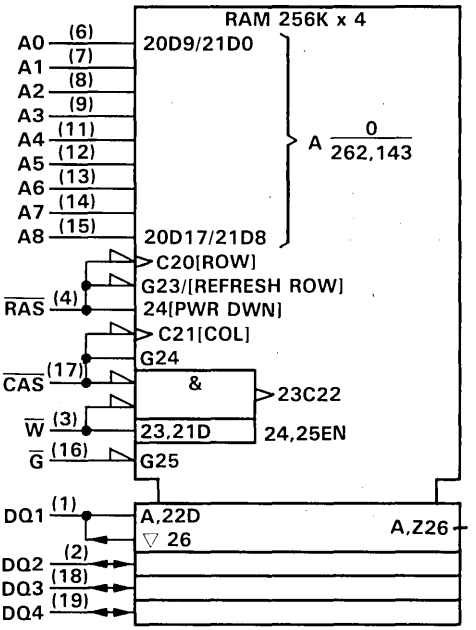
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level.

test function pin

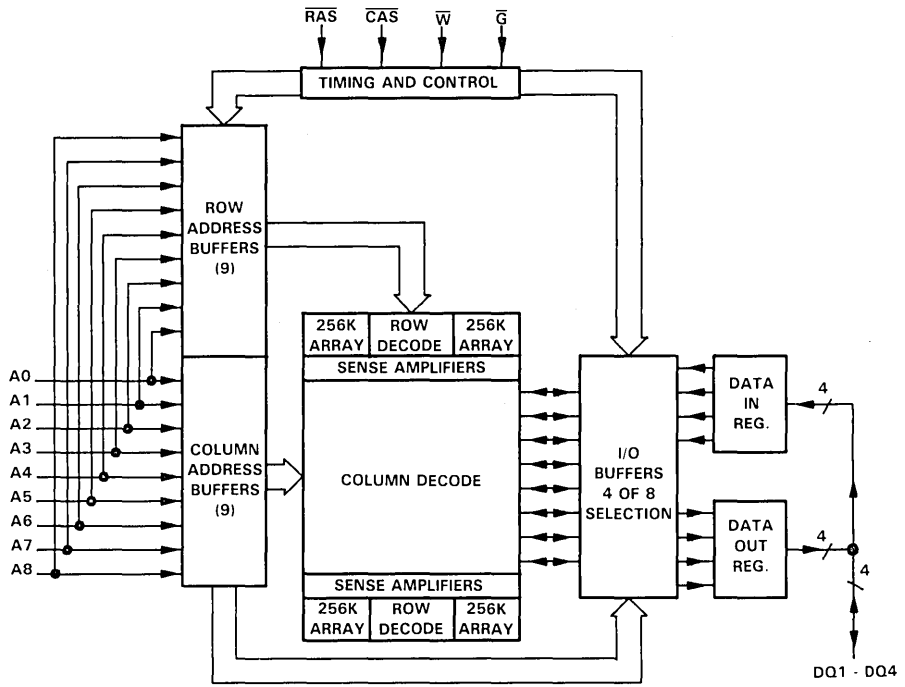
During normal device operation, the TF pin must be either disconnected or biased at a voltage less than or equal to V_{CC}.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) . . . . . −1 V to 7 V
Voltage range on V_{CC} . . . . . 0 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS44C25_-10		TMS44C25_-12		TMS44C25_-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	μA
I_{CC1}	Read/write cycle current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V		70		60		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		3		3		3	mA
I_{CC3}	Average refresh current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		65		55		50	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		45		35		30	mA
I_{CC6}	Average static column decode current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		45		35		30	mA

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capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write-enable input		7	pF
C_o	Output capacitance		7	pF

NOTE 3: V_{CC} equal to 5.0 V ± 0.5 V and the bias on pins under test is 0.0 V.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

PARAMETER		ALT. SYMBOL	TMS44C25_-10		TMS44C25_-12		TMS44C25_-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		25		30		40	ns
$t_{a(CA)}$	Access time from column address	t_{CAA}		45		55		70	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}		100		120		150	ns
$t_{a(G)}$	Access time from $\overline{G}$ low	t_{GAC}		25		30		40	ns
$t_{a(CP)}$	Access time from column precharge (TMS44C256 only)	t_{CAP}		50		60		75	ns
$t_{a(WHQ)}$	Access time from $\overline{W}$ high, Static column decode mode (see Note 4) (TMS44C257 only)	t_{WRA}		30		35		40	ns
$t_{a(WLQ)}$	Access time from $\overline{W}$ low, Static column decode mode (see Note 4) (TMS44C257 only)	t_{ALW}		95		115		120	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 5)	t_{OFF}	0	25	0	30	0	35	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high (see Note 5)	t_{GOFF}	0	25	0	30	0	35	ns

NOTES: 4. Read-modify-write operation only.
5. $t_{dis(CH)}$ and $t_{dis(G)}$ are specified when the output is no longer driven.

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS44C256-10		TMS44C256-12		TMS44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 7)	t_{RC}	190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	220		255		305		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 8)	t_{PC}	55		65		80		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PCM}	85		100		125		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 9)	t_{CAS}	25	10,000	30	10,000	40	10,000	ns
$t_{w(RH)}$	Pulse duration $\overline{RAS}$ high (precharge)	t_{RP}	80		90		100		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	t_{RAS}	100	10,000	120	10,000	150	10,000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	t_{RASP}	100	100,000	120	100,000	150	100,000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		20		25		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ low (see Note 11)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 12)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	25		30		40		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	25		30		40		ns
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$ low (see Note 11)	t_{CAH}	20		20		25		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		20		ns

Continued next page.

NOTES: 6. Timing measurements are referenced to V_{IL} max and V_{IH} min.
7. All cycle times assume t_t = 5 ns.
8. $t_{c(P)} > t_{w(CH)}$ min + $t_{w(CL)}$ min + $2t_t$.
9. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $[t_{w(CL)}]$.
10. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time $[t_{w(RL)}]$.
11. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Early write operation only.

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS44C256-10		TMS44C256-12		TMS44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 13)	t_{AR}	70		80		100		ns
$t_{h(D)}$	Data hold time after $\overline{CAS}$ low (see Note 11)	t_{DH}	20		25		30		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 13)	t_{DHR}	70		85		110		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 15)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 15)	t_{RRH}	10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 12)	t_{WCH}	20		25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 13)	t_{WCR}	70		85		100		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 4)	t_{CWD}	50		60		70		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	25	75	25	90	30	110	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 14)	t_{RAD}	20	55	20	65	25	80	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	45		55		70		ns
$t_{d(CACH)}$	Delay time, column address to $\overline{CAS}$ high	t_{CAL}	45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 4)	t_{RWD}	100		120		150		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 4)	t_{AWD}	45		55		70		ns
$t_{d(GHD)}$	Delay time, $\overline{G}$ high before data at DQ	t_{GDD}	25		30		40		ns
$t_{d(GLRH)}$	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	t_{GSR}	20		25		35		ns

Continued next page.

NOTES: 4. Read-modify-write operation only.
11. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Early write operation only.
13. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
14. Maximum value specified only to guarantee access time.
15. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS44C256-10		TMS44C256-12		TMS44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		15		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTE 16: $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS44C257-10		TMS44C257-12		TMS44C257-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 7)	t_{RC}	190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	220		255		305		ns
$t_{c(rd)SC}$	Static column decode mode read-only cycle time	t_{SCR}	50		60		90		ns
$t_{c(W)SC}$	Static column decode mode write-only cycle time	t_{CSW}	50		60		90		ns
$t_{c(rdW)SC}$	Static column decode mode read-modify-write cycle time	t_{SCRDW}	100		120		150		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 9)	t_{CAS}	20	10,000	25	10,000	35	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	80		90		100		ns
$t_{w(RL)}$	Non-static column decode mode pulse duration, $\overline{RAS}$ low (see Note 10)	t_{RAS}	100	10,000	120	10,000	150	10,000	ns
$t_{w(RL)P}$	Static column decode mode pulse duration, $\overline{RAS}$ low (see Note 10)	t_{RASP}	100	100,000	120	100,000	150	100,000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		20		25		ns
$t_{w(CA)}$	Static column decode mode column address pulse duration	t_{ADP}	45		55		70		ns
$t_{w(WH)}$	Static column decode mode $\overline{W}$ high pulse duration	t_{WI}	10		15		25		ns
$t_{su(CA)}$	Column-address setup times before $\overline{CAS}$ low or $\overline{W}$ low (see Note 11)	t_{ASC}	0		0		0		ns
$t_{su(RA)}$	Row address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ low (see Note 11)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 12)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	25		30		40		ns
$t_{su(WHCH)}$	$\overline{W}$-high setup time before $\overline{CAS}$ high (see Note 12)	t_{WHCH}	0		0		0		ns

Continued next page.

NOTES: 6. Timing measurements are referenced to V_{IL} max and V_{IH} min.
7. All cycle times assume t_t = 5 ns.
9. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].
10. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].
11. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Early write operation only.

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS44C257-10		TMS44C257-12		TMS44C257-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	25		30		40		ns
$t_{su(RLrd)}$	Read-command setup time before $\overline{RAS}$ low	t_{WRP}	0		0		0		ns
$t_{su(CAR)}$	Column-address setup time before $\overline{RAS}$ high	t_{CAR}	50		60		75		ns
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$ low, $\overline{W}$ low (see Note 11)	t_{CAH}	20		20		25		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 17)	t_{AR}	100		120		150		ns
$t_{h(D)}$	Data hold time after $\overline{CAS}$ low (see Note 11)	t_{DH}	20		25		30		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 17)	t_{DHR}	70		85		110		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 15)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 15)	t_{RRH}	10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	20		25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 17)	t_{WCR}	70		85		100		ns
$t_{h(RHCA)}$	Column-address hold time after $\overline{RAS}$ high	t_{AH}	10		15		15		ns
$t_{h(CAQ)}$	Output hold time after address change	t_{OH}	5		5		5		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 4)	t_{CWD}	25		30		40		ns

Continued next page.

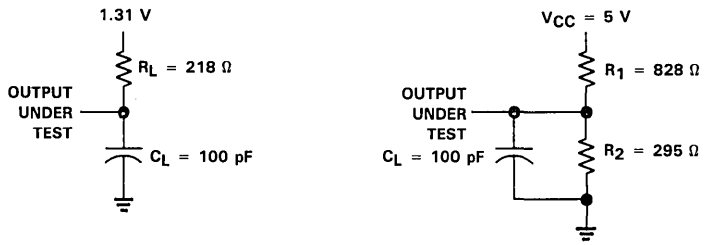
NOTES: 4. Read-modify-write operation only.
11. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
15. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
17. The minimum value is measured when $t_{d(RLCA)}$ is set to $t_{d(RLCA)}$ min as a reference.

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS44C257-10		TMS44C257-12		TMS44C257-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	25	75	25	90	30	110	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 14)	t_{RAD}	20	55	20	65	25	80	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	45		55		70		ns
$t_{d(CACH)}$	Delay time, column address to $\overline{CAS}$ high	t_{CAL}	45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 4)	t_{RWD}	100		120		150		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 4)	t_{AWD}	45		55		70		ns
$t_{d(GHD)}$	Delay time, $\overline{G}$ high before data at DQ	t_{GDD}	25		30		40		ns
$t_{d(GLRH)}$	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	t_{GSR}	20		25		35		ns
$t_{d(WQ)}$	Delay time, $\overline{W}$ high to output transition from high impedance to active	t_{OW}	0		0		0		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		15		ns
$t_{d(RHCL)R}$	Delay time $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTES: 4. Read-modify-write operation only.
14. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

PARAMETER MEASUREMENT INFORMATION

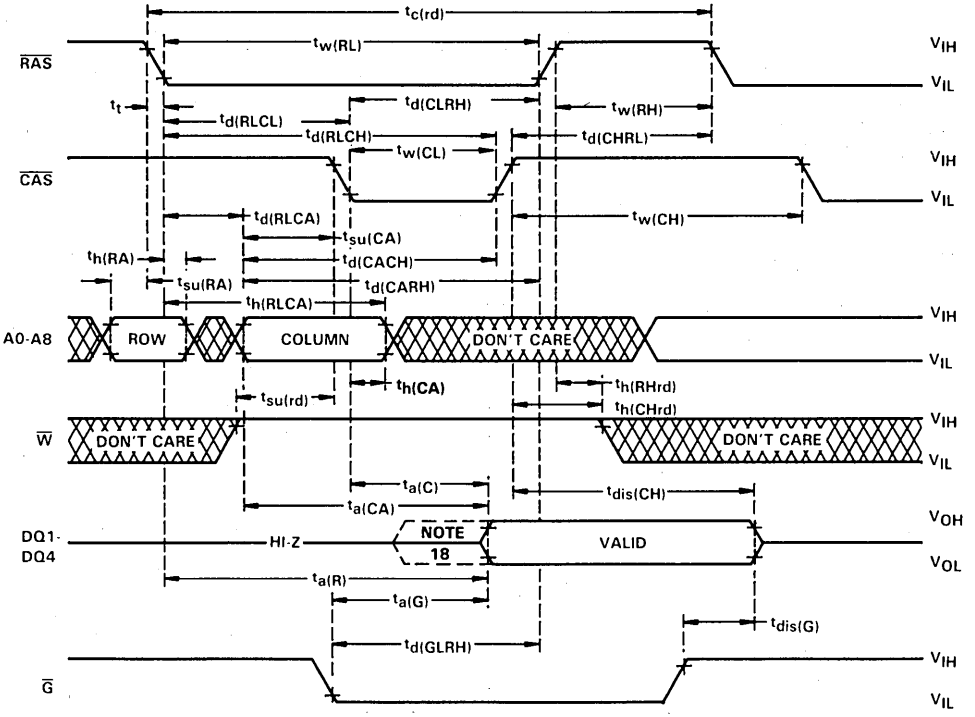


(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

FIGURE 1. LOAD CIRCUITS FOR TIMING PARAMETERS

read cycle timing



NOTE 18: Output may go from high impedance to an invalid data state prior to the specified access time.

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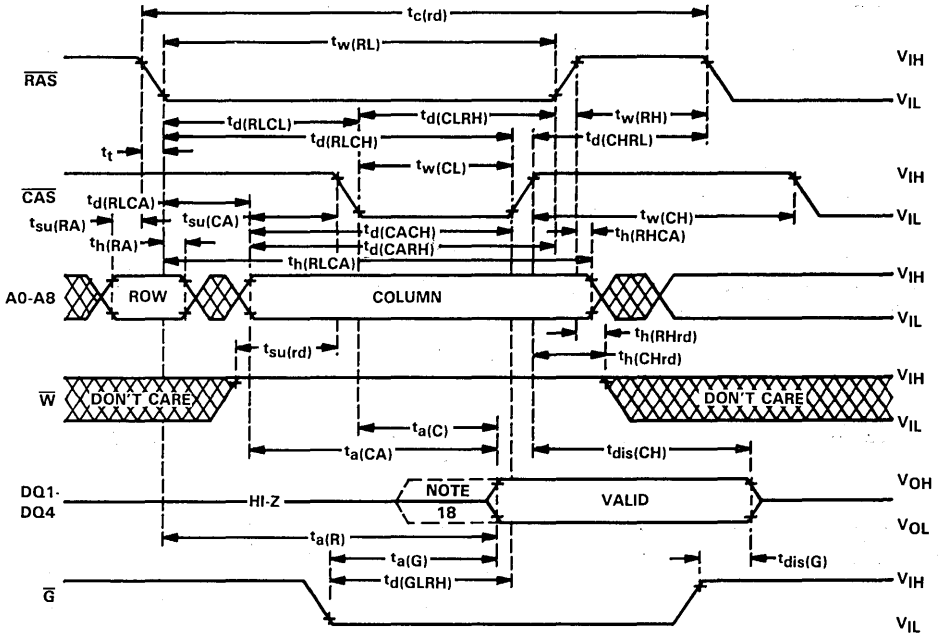
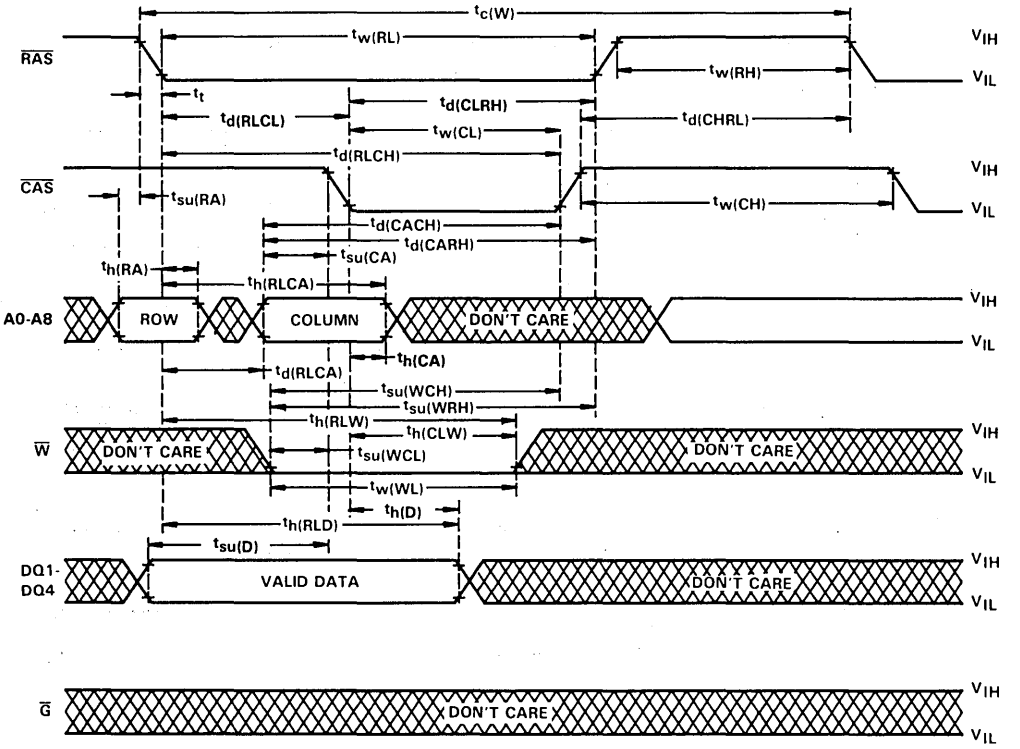
read cycle timing

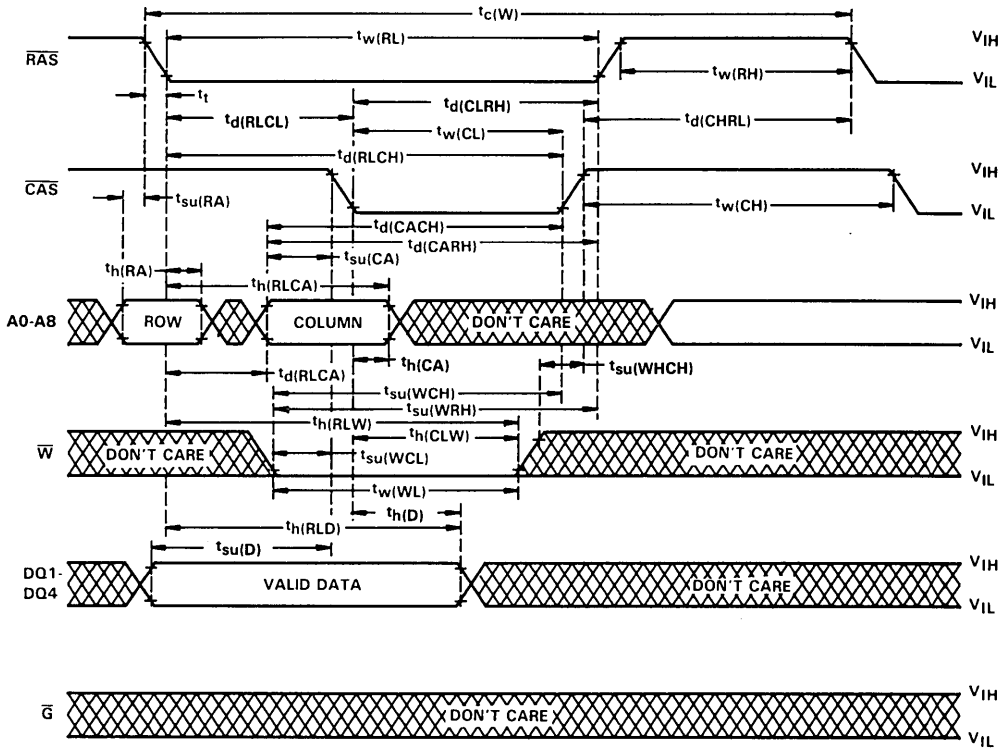


NOTE 18: Output may go from high impedance to an invalid data state prior to the specified access time.

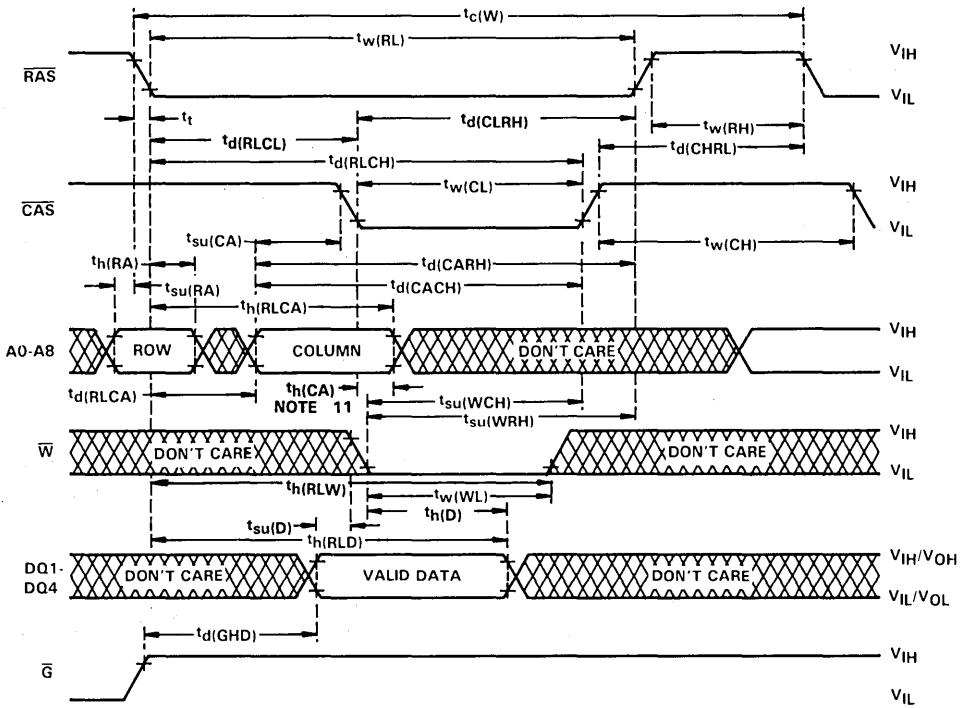
early write cycle timing



early write cycle timing

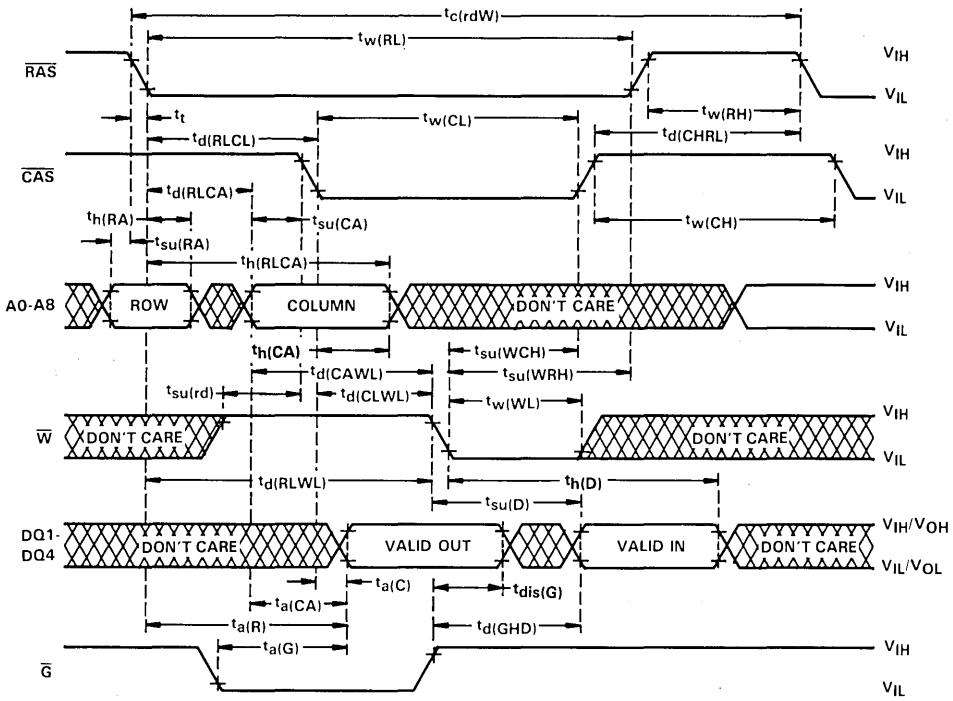


write cycle timing

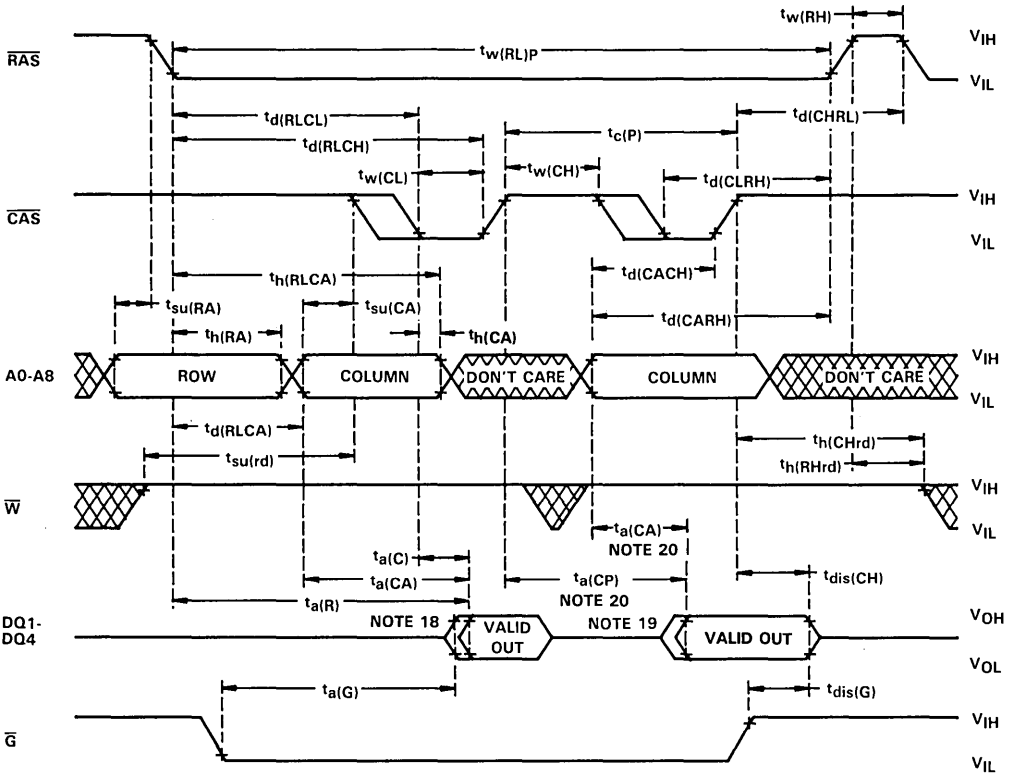


NOTE 11: Later of $\overline{CAS}$ or $\overline{W}$ in write operation.

read-write/read-modify-write cycle timing

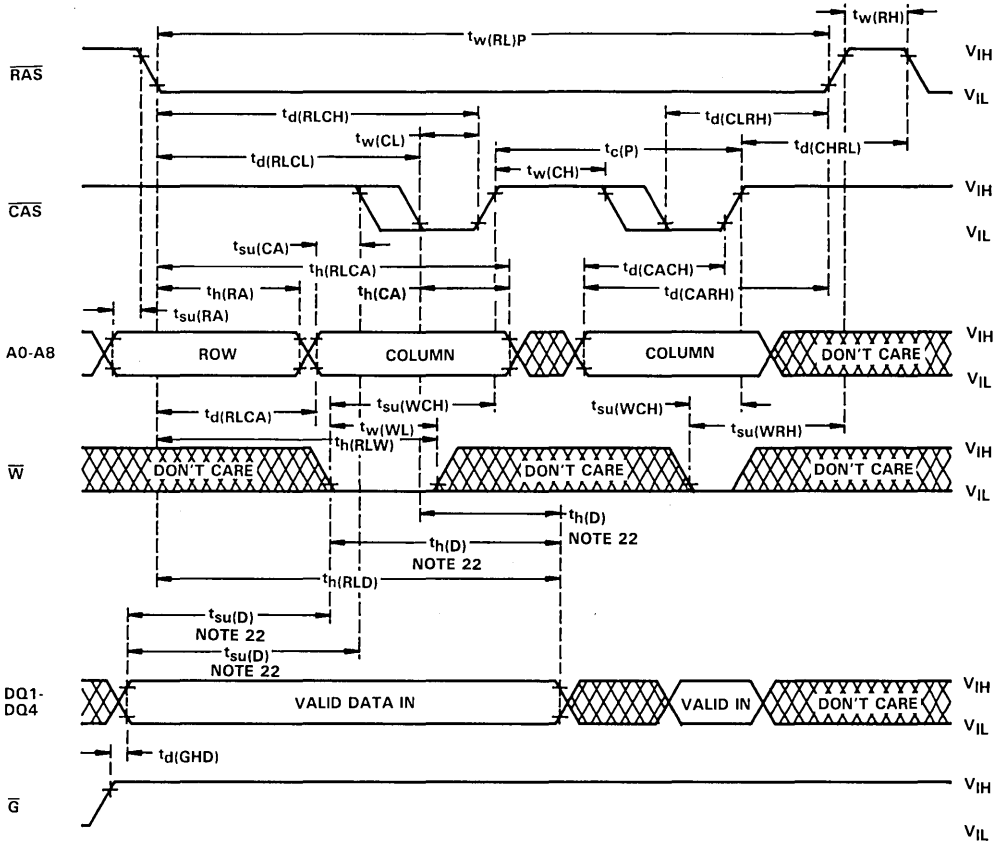


enhanced page-mode read cycle timing



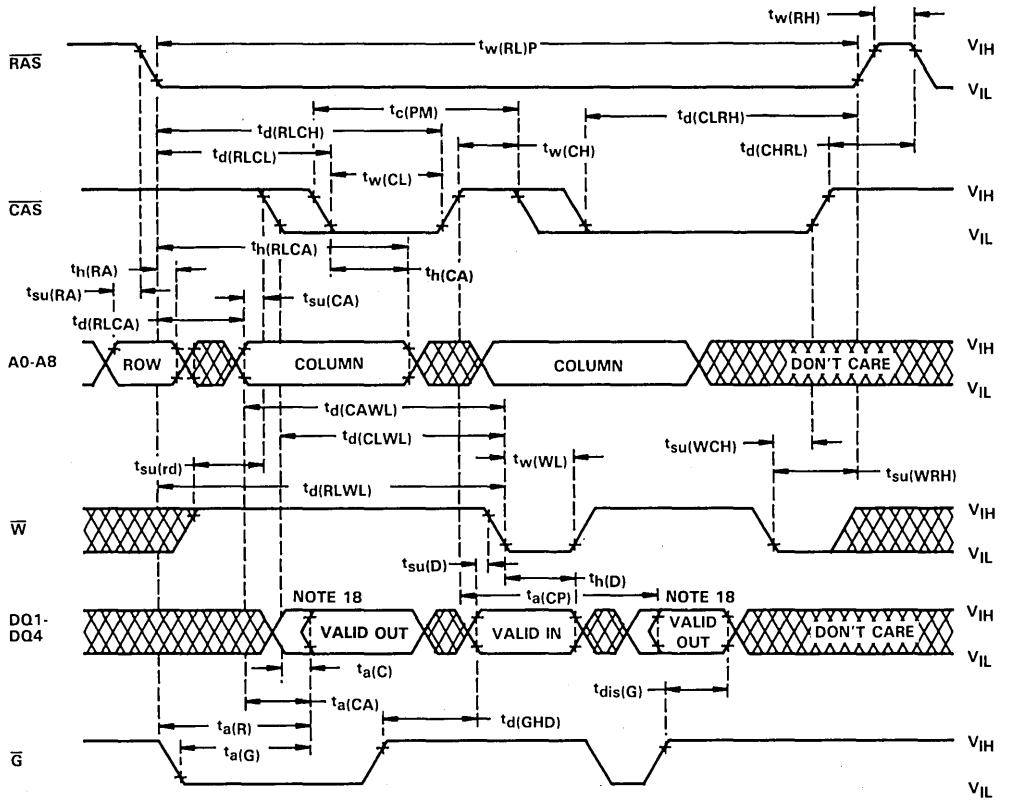
NOTES: 18. Output may go from high impedance to an invalid data state prior to the specified access time.
19. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
20. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

enhanced page-mode write cycle timing



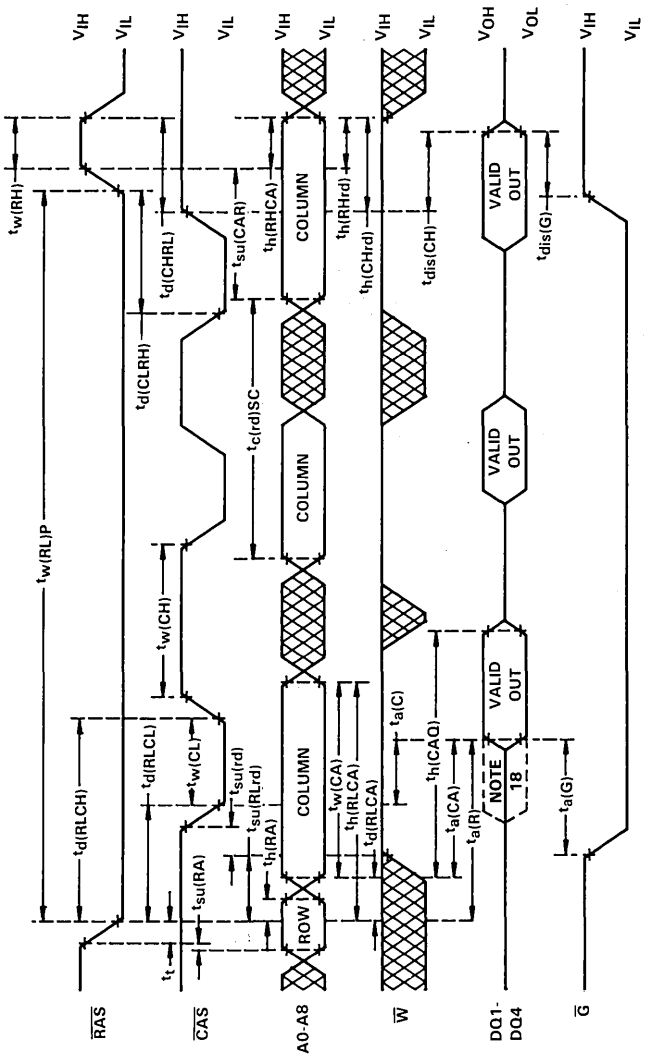
NOTES: 21. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.
22. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

enhanced page-mode read-modify-write cycle timing



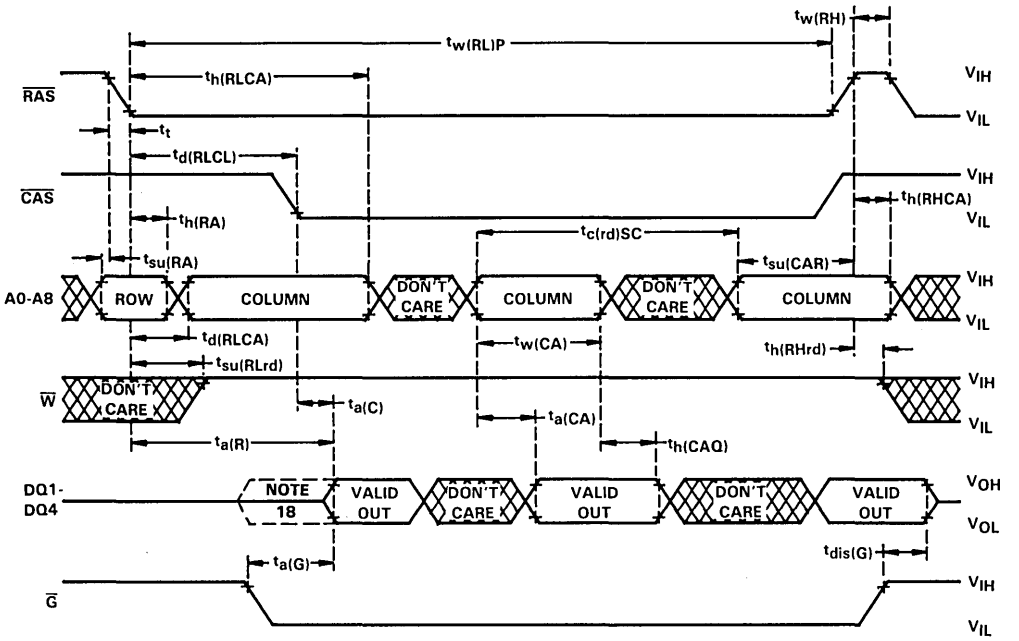
NOTES: 18. Output may go from high impedance to an invalid data state prior to the specified access time.
23. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.

static column decode mode read timing with $\overline{CAS}$ cycling



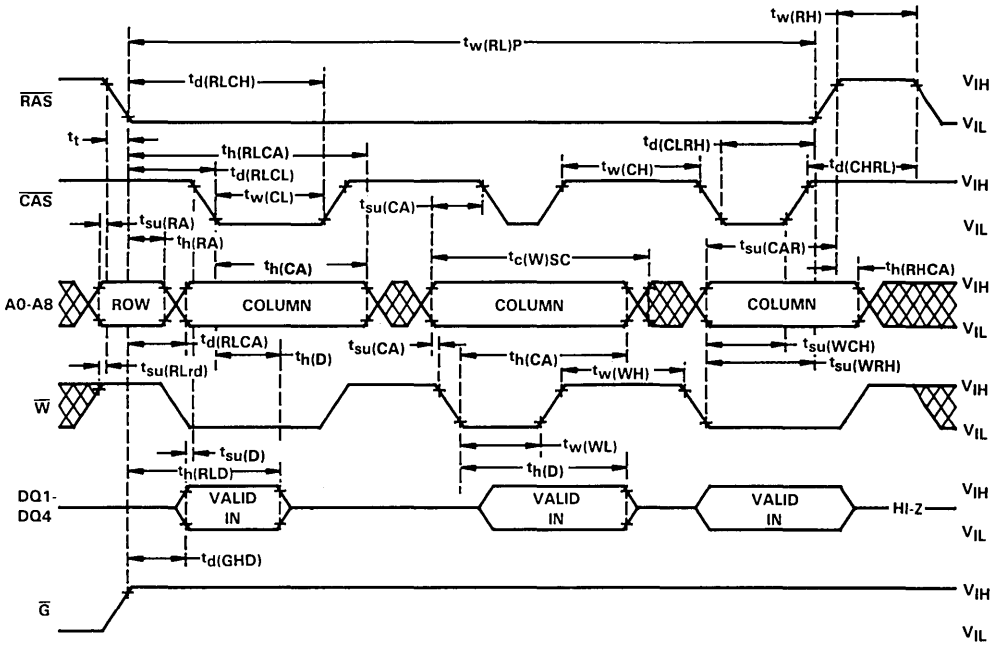
NOTE 18: Output may go from high impedance to an invalid data state prior to the specified access time.

static column decode mode read cycle timing

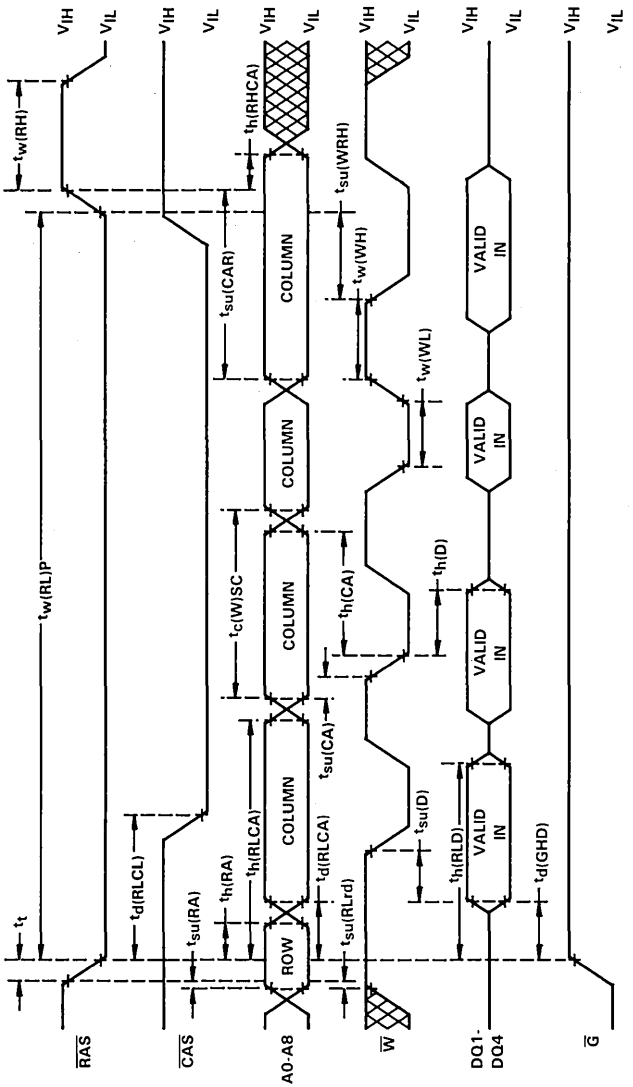


NOTE 18: Output may go from high impedance to an invalid data state prior to the specified access time.

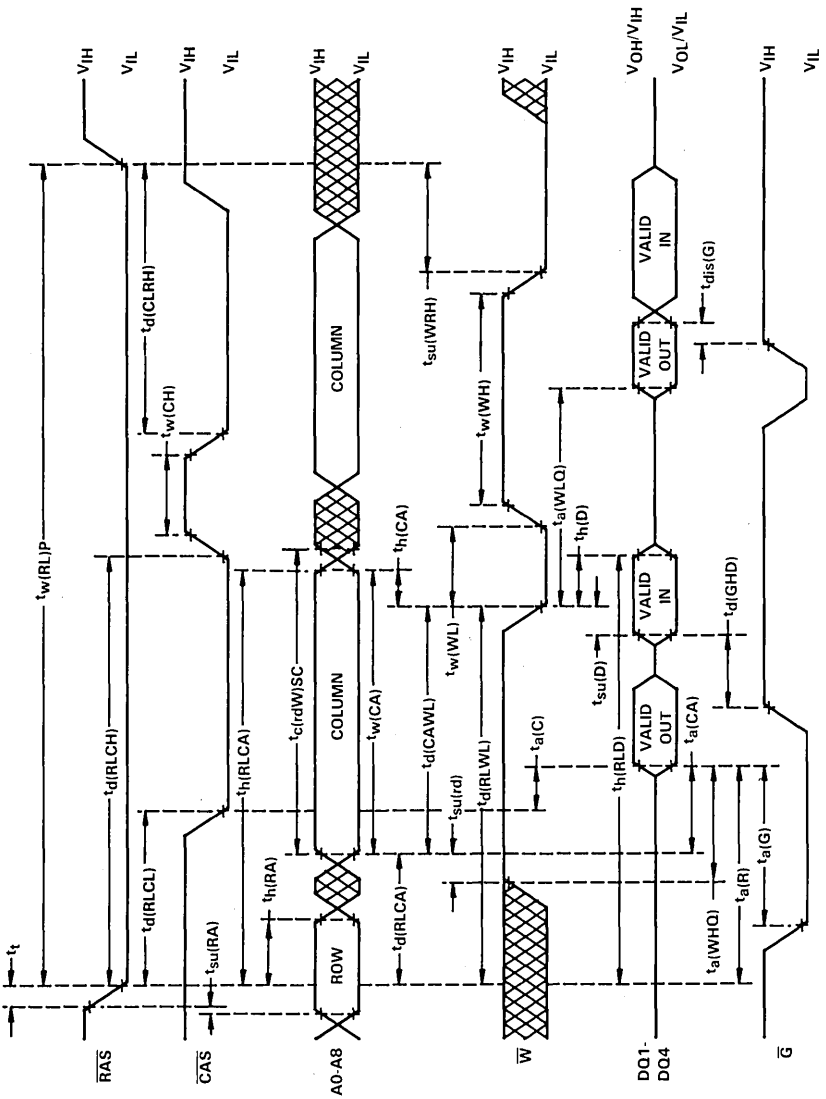
static column decode mode early write cycle timing



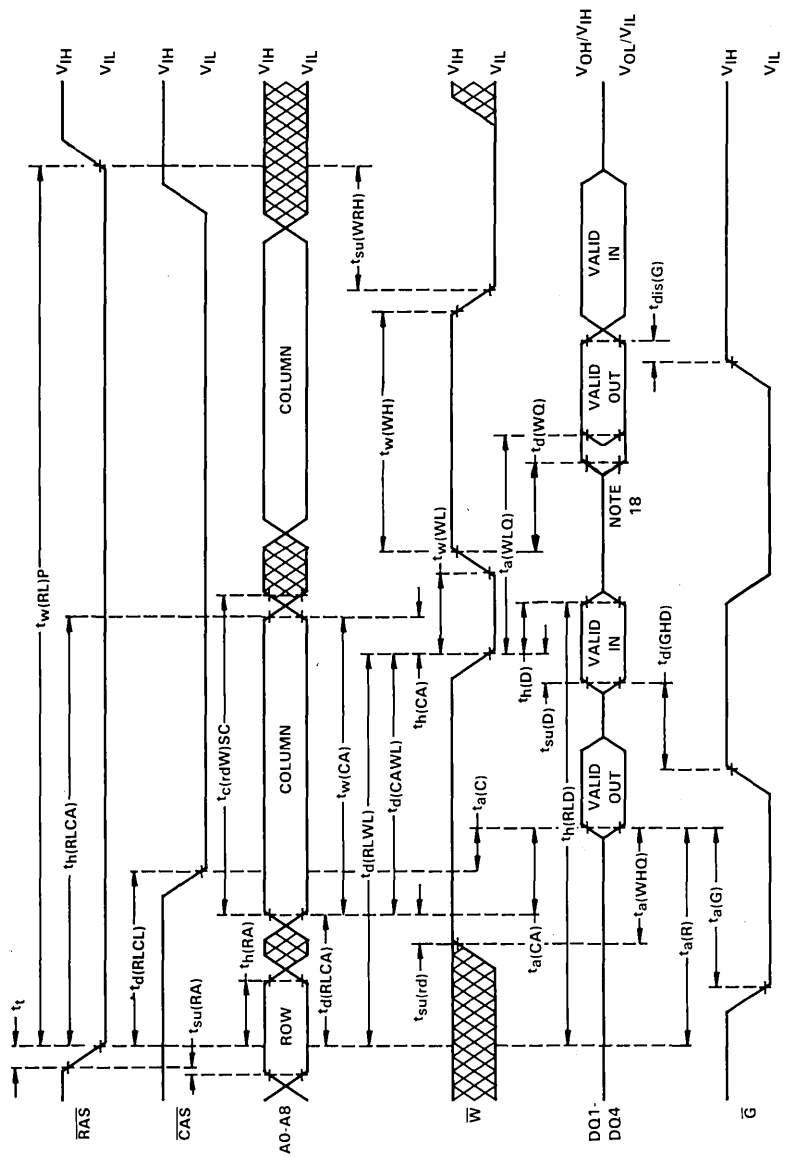
static column decode mode write cycle timing



static column decode mode read-modify-write cycle timing with $\overline{CAS}$ cycling

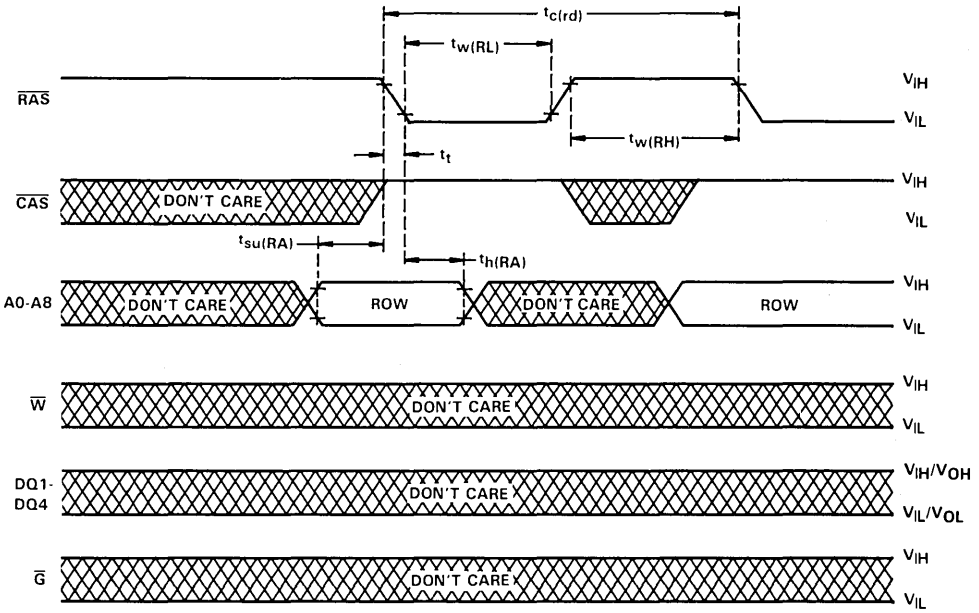


static column decode mode read-modify-write cycle timing

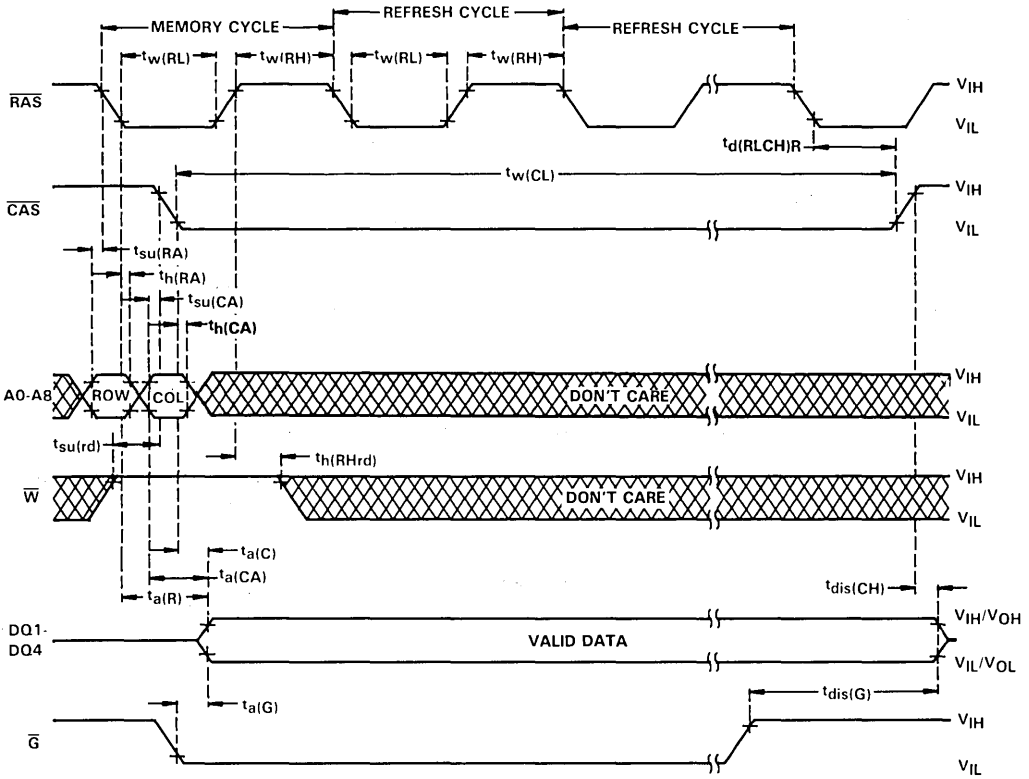


NOTE 18: Output may go from high impedance to an invalid data state prior to the specified access time.

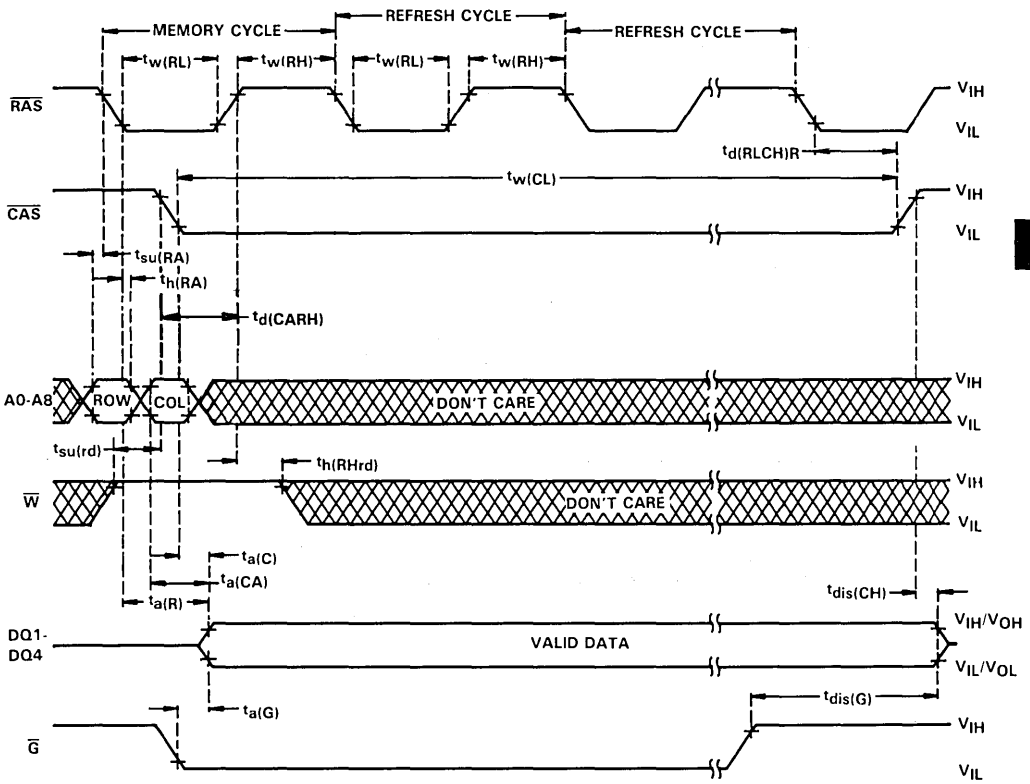
$\overline{RAS}$-only refresh timing



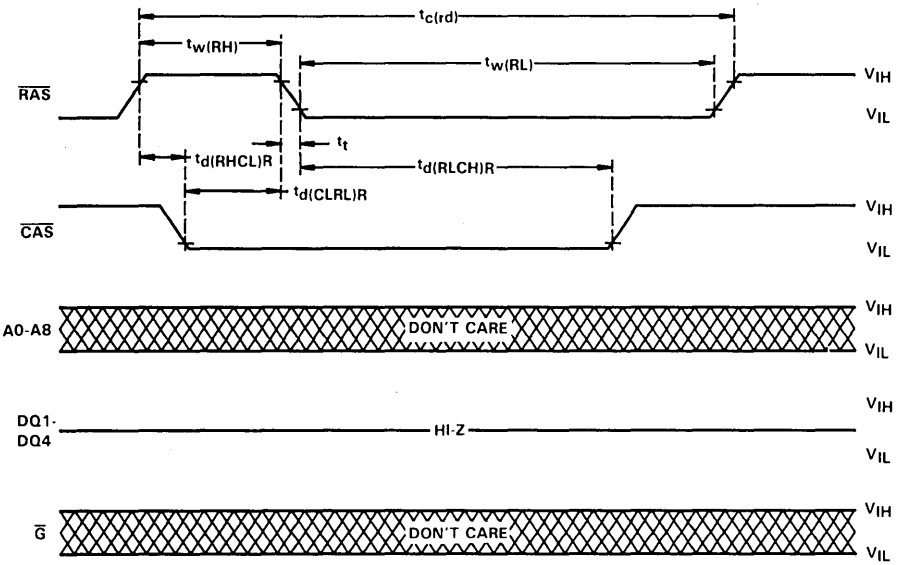
hidden refresh cycle (enhanced page mode)



hidden refresh cycle (static column decode mode)



automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



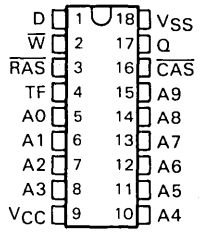
MAY 1986—REVISED MAY 1988

- 1,048,576 × 1 Organization
- Single 5-V Supply (10% Tolerance)
- Performance Ranges:

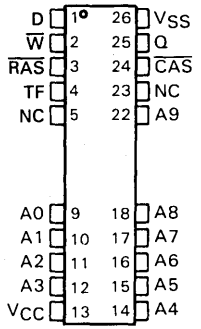
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS4C102_-10	100 ns	25 ns	45 ns	190 ns
TMS4C102_-12	120 ns	30 ns	55 ns	220 ns
TMS4C102_-15	150 ns	40 ns	70 ns	260 ns

- TMS4C1024—Enhanced Page Mode Operation for Faster Memory Access
  - Higher Data Bandwidth than Conventional Page-Mode Parts
  - Random Single-Bit Access Within a Row with a Column Address
- TMS4C1025—4-Bit Nibble Mode Operation
  - Four Sequential Single Bit Access Within a Row By Toggling $\overline{CAS}$
- TMS4C1027—Static Column Decode Mode Operation
  - Random Single-Bit Access Within a Row with Only a Column Address Change
- One of TI's CMOS Megabit DRAM Family Including:
  TMS44C256—256K × 4 Enhanced Page Mode
  TMS44C257—256K × 4 Static Column Decode
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)
- 3-State Unlatched Output
- Low Power Dissipation
- Texas Instruments EPIC™ CMOS Process
- All Inputs/Outputs and Clocks Are TTL Compatible
- High-Reliability Plastic 18-Pin 300-Mil-Wide DIP or 20/26-Lead Surface Mount (SOJ) Packages
- Operating Free-Air Temperature 0°C to 70°C
- Operations of TI's Megabit CMOS DRAMs Can Be Controlled by TI's SN74ALS6301 and SN74ALS6302 Dynamic RAM Controllers

N PACKAGE
(TOP VIEW)



DJ PACKAGE†
(TOP VIEW)



†The packages shown here are for pinout reference only. The DJ package is actually 75% of the length of the N package.

PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

EPIC is a trademark of Texas Instruments Incorporated.

description

The TMS4C1024, TMS4C1025, and TMS4C1027 are high-speed, 1,048,576-bit dynamic random-access memories, organized as 1,048,576 words of one bit each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 100 ns, 120 ns and 150 ns. Maximum power dissipation is as low as 330 mW operating and 16.5 mW standby on 120 ns devices.

The EPIC™ technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{CC} peaks are 140 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4C102_ are offered in 18-pin plastic dual-in-line (N-suffix) and 20/26-lead plastic surface mount SOJ (DJ suffix) packages. These packages are guaranteed for operation from 0°C to 70°C.

operation

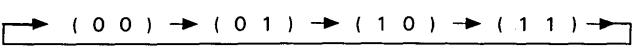
enhanced page mode (TMS4C1024)

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS4C1024 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page mode." Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

nibble mode (TMS4C1025)

Nibble-mode operation allows high-speed read, write, or read-write-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The next sequential bits can be read or written by cycling $\overline{CAS}$ while $\overline{RAS}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Row A9 and column A9 provide the two binary bits for initial selection, with row A9 being the least-significant address and column A9 being the most significant. Thereafter, the falling edge of $\overline{CAS}$ will access the next bit of the circular 4-bit nibble in the following sequence.



Data written in a sequence of more than 4 consecutive cycles shall be capable of being read back without exiting from the nibble mode. In a sequence of consecutive nibble-mode cycles the control of the high-impedance state for the data out (Q) pin is determined by each individual cycle. This facilitates fully mixed nibble-mode cycles (e.g., read/write/read-modify-write/read etc.).

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static column decode mode (TMS4C1027)

The static column decode mode of operation allows high-speed read, write, or read-modify-write by reducing the number of required signal setup, hold, and transition timings. This is achieved by first addressing the row and column in the normal manner, but after the first access, maintaining $\overline{CAS}$ low. Subsequently changing the column address produces valid data at $t_{a(CA)}$. The first bit is accessed in the normal manner with read coming out at $t_{a(R)}$ time. Similarly, write or read-modify-write cycle times can be achieved with appropriate toggling of $\overline{W}$. The addresses are latched during the write operation, but at the completion of the internal write operation the addresses are unlatched.

address (A0 through A9) (TMS4C1024, TMS4C1025)

Twenty address bits are required to decode 1 of 1,048,576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

address (A0 through A9) (TMS4C1027)

Twenty address bits are required to decode 1 of 1,048,576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9. Row addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. In a write cycle, the later of $\overline{CAS}$ or $\overline{W}$ latches the column address bits.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0-A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level,

thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter $t_{d(CLRL)R}$] and holding it low after $\overline{RAS}$ falls [see parameter $t_{d(RLCH)R}$]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh cycles.

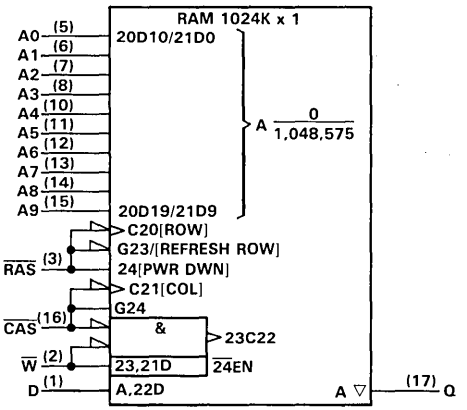
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved.

test-function pin

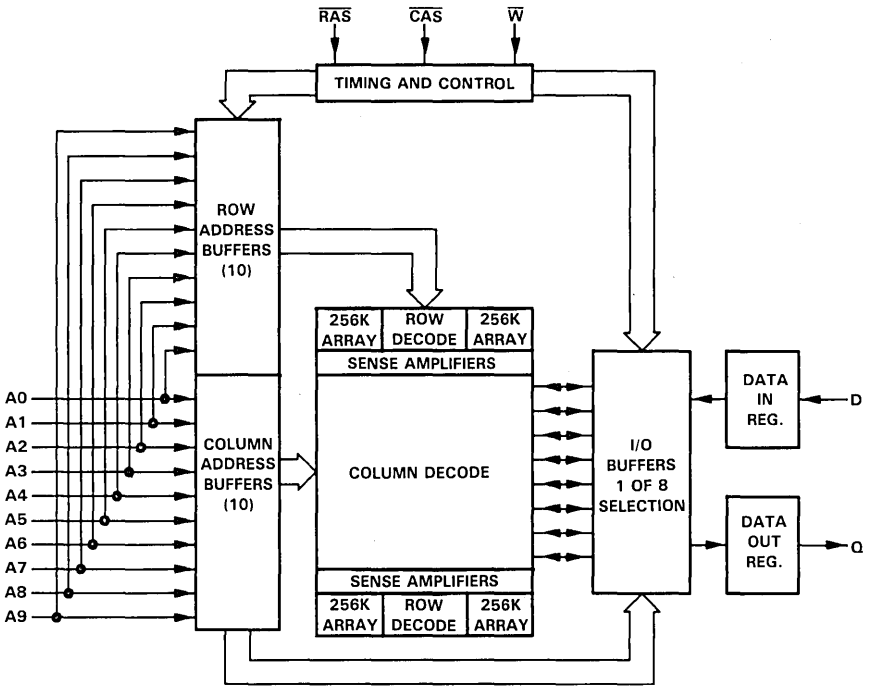
During normal device operation the TF pin must either be disconnected or biased at a voltage less than or equal to V_{CC}.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 18-pin dual-in-line package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin . . . . . −1 V to 7 V
Voltage range on V_{CC} . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4C1024-10 TMS4C1025-10 TMS4C1027-10		TMS4C1024-12 TMS4C1025-12 TMS4C1027-12		TMS4C1024-15 TMS4C1025-15 TMS4C1027-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	μA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		70		60		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		3		3		3	mA
I_{CC3}	Average refresh current	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		65		55		50	mA
I_{CC4}	Average page current (TMS4C1024)	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		45		35		30	mA
I_{CC5}	Average nibble current (TMS4C1025)	$t_{c(N)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling for 4 cycles		45		40		30	mA
I_{CC6}	Average static column decode current (TMS4C1027)	$t_{c(rdW)SC}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		45		35		30	mA

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capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(D)}$	Input capacitance, data input		5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write-enable input		7	pF
C_o	Output capacitance		7	pF

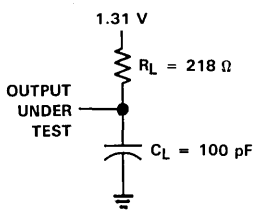
NOTE 3: V_{CC} equal to 5.0 V ± 0.5 V and the bias on pins under test is 0.0 V.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

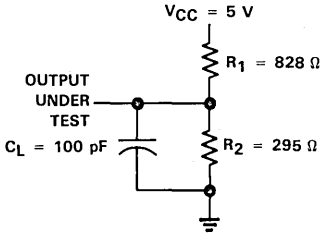
PARAMETER		ALT. SYMBOL	TMS4C102_-10		TMS4C102_-12		TMS4C102_-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low†	t_{CAC}		25		30		40	ns
$t_{a(CA)}$	Access time from column-address†	t_{CAA}		45		55		70	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low†	t_{RAC}		100		120		150	ns
$t_{a(CP)}$	Access time from column precharge (TMS4C1024 only)	t_{CAP}		50		60		75	ns
$t_{a(C)N}$	Access time from $\overline{CAS}$ low (TMS4C1025 only)	t_{NCAC}		20		25		35	ns
$t_{a(WHQ)}$	Access time from $\overline{W}$ high (TMS4C1027 only)	t_{WRA}		30		35		40	ns
$t_{a(WLQ)}$	Access time from $\overline{W}$ low (TMS4C1027 only)	t_{ALW}		95		115		120	ns
$t_{h(CAQ)}$	Static column decode mode output hold time after address change (TMS4C1027 only)	t_{AOH}	5		5		5		ns
$t_{h(WQ)}$	Static column decode mode output hold time after $\overline{W}$ low (TMS4C1027 only)	t_{WOH}	0		0		0		ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)†	t_{OFF}	0	25	0	30	0	35	ns

†Parameters apply uniformly to TMS4C1024, TMS4C1025, TMS4C1027.
NOTE 4: $t_{dis(CH)}$ is specified when the output is no longer driven.

PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT



(b) ALTERNATE LOAD CIRCUIT

FIGURE 1. LOAD CIRCUITS FOR TIMING PARAMETERS

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4C1024-10		TMS4C1024-12		TMS4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	220		255		305		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 7)	t_{PC}	55		65		80		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PCM}	85		100		125		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	25	10,000	30	10,000	40	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	80		90		100		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	100	10,000	120	10,000	150	10,000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	100	100,000	120	100,000	150	100,000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		20		25		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time (see Note 10)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	25		30		40		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	25		30		40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		25		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	70		80		100		ns
$t_{h(D)}$	Data hold time (see Note 10)	t_{DH}	20		25		30		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	70		85		110		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 15)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 15)	t_{RRH}	10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	20		25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 12)	t_{WCR}	70		85		100		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 13)	t_{CWD}	25		30		40		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	25	80	25	95	30	115	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	t_{RAD}	20	55	20	65	25	80	ns

Continued next page.

NOTES:

5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To guarantee $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Read-modify-write operation only.
14. Maximum value specified only to guarantee access time.
15. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS4C1024-10		TMS4C1024-12		TMS4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	45		55		70		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	100		120		150		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 13)	t_{AWD}	45		55		70		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high, (see Note 16)	t_{CHR}	25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low, (see Note 16)	t_{CSR}	10		10		15		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTES: 13. Read-modify-write operation only.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT.	TMS4C1025-10		TMS4C1025-12		TMS4C1025-15		UNIT
		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	220		255		305		ns
$t_{c(N)}$	Nibble-mode read or write cycle time	t_{NC}	40		50		70		ns
$t_{c(rdW)N}$	Nibble-mode read-modify-write cycle time	t_{NRMW}	65		75		110		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	10,000	25	10,000	35	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	80		90		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	100	10,000	120	10,000	150	10,000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		20		25		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time (see Note 10)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	20		25		35		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	20		25		35		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		25		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	70		80		100		ns
$t_{h(D)}$	Data hold time (see Note 10)	t_{DH}	20		25		35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	70		85		110		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high	t_{RRH}	10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	20		25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Notes 11 and 12)	t_{WCR}	70		85		100		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		25		35		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 13)	t_{CWD}	20		25		35		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	25	80	25	95	30	115	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	t_{RAD}	20	55	20	65	25	80	ns

Continued next page.

NOTES:

5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Read-modify-write operation only.
14. Maximum value specified only to guarantee access time.

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS4C1025-10		TMS4C1025-12		TMS4C1025-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	45		55		70		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	100		120		150		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 13)	t_{AWD}	45		55		70		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		15		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTES: 13. Read-modify-write operation only.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4C1027-10		TMS4C1027-12		TMS4C1027-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	220		255		305		ns
$t_{c(rd)SC}$	Static column decode mode read cycle time	t_{SCR}	50		60		90		ns
$t_{c(W)SC}$	Static column decode mode write cycle time	t_{SCW}	50		60		90		ns
$t_{c(rdW)SC}$	Static column decode mode, read-modify-write cycle time	t_{SCRDW}	100		120		150		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	25	10,000	30	10,000	40	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	80		90		100		ns
$t_{w(RL)}$	Non-static column decode mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	100	10,000	120	10,000	150	10,000	ns
$t_{w(RL)P}$	Static column decode mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	100	100,000	120	100,000	150	100,000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		20		25		ns
$t_{w(CA)}$	Static column decode mode column-address pulse duration	t_{ADP}	45		55		70		ns
$t_{w(WH)}$	Static column decode mode $\overline{W}$ high pulse duration, inactive	t_{WI}	10		15		25		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$, $\overline{W}$ low (see Note 10)	t_{ASC}	0		0		0		ns
$t_{su(CAR)}$	Column-address setup time before $\overline{RAS}$	t_{CAR}	50		60		75		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	25		30		40		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	25		30		40		ns
$t_{su(WHCH)}$	Setup time, $\overline{W}$ high to $\overline{CAS}$ high for early write, high impedance	t_{WH}	0		0		0		ns
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$, $\overline{W}$ low (see Note 10)	t_{CAH}	20		20		25		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 18)	t_{AR}	100		120		150		ns

Continued next page.

NOTES:

5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
18. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.

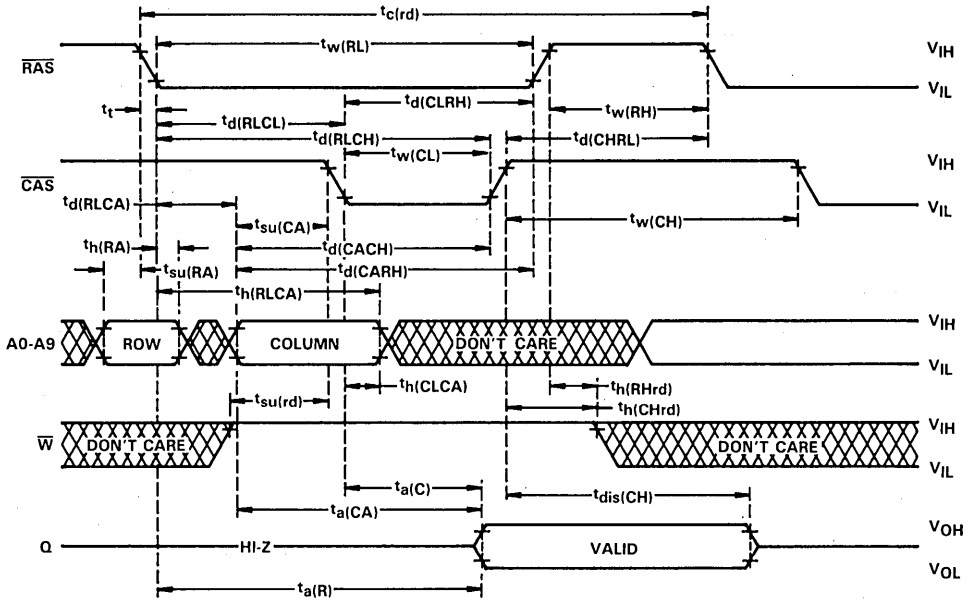
timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS4C1027-10		TMS4C1027-12		TMS4C1027-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(D)}$	Data hold time (see Note 10)	t_{DH}	20		25		30		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 17)	t_{DHR}	70		85		110		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 18)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 18)	t_{RRH}	10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	20		25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 17)	t_{WCR}	70		85		100		ns
$t_{h(RHCA)}$	Column-address hold time after $\overline{RAS}$ high	t_{AH}	10		15		15		ns
$t_{h(WLCA2)}$	Static column decode mode second column-address hold time after $\overline{W}$ low (see Note 13)	t_{AHLW}	95		115		135		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 13)	t_{CWD}	25		30		40		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	25	80	25	95	30	115	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 14)	t_{RAD}	20	55	20	65	25	80	ns
$t_{d(WLCA)}$	Delay time, $\overline{W}$ low to column address	t_{LWAD}	25	50	30	60	35	70	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	45		55		70		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	100		120		150		ns
$t_{d(RLWL2)}$	Static column decode mode delay time, $\overline{RAS}$ low to second $\overline{W}$ low	t_{RSW}	100		120		150		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 13)	t_{AWD}	45		55		70		ns
$t_{d(WQ)}$	Delay time, $\overline{W}$ high to output transition from high impedance to active	t_{OW}	0		0		0		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high, (see Note 16)	t_{CHR}	25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		15		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

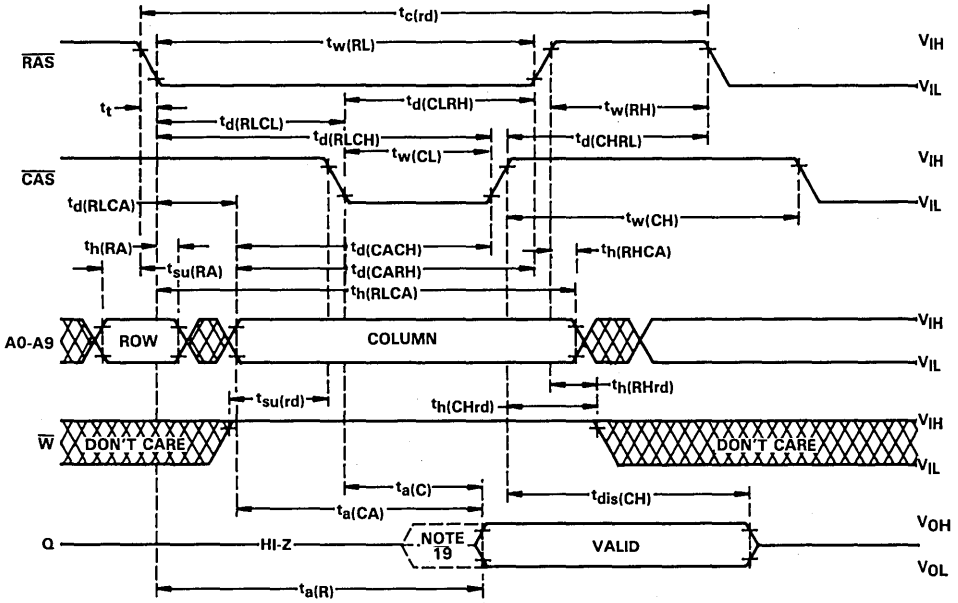
NOTES:

10. Referenced to later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
13. Read-modify-write operation only.
14. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
17. The minimum value is measured when $t_{d(RLCA)}$ is set to $t_{d(RLCA)}$ min as a reference.
18. Either $t_{h(RDrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.

read cycle timing

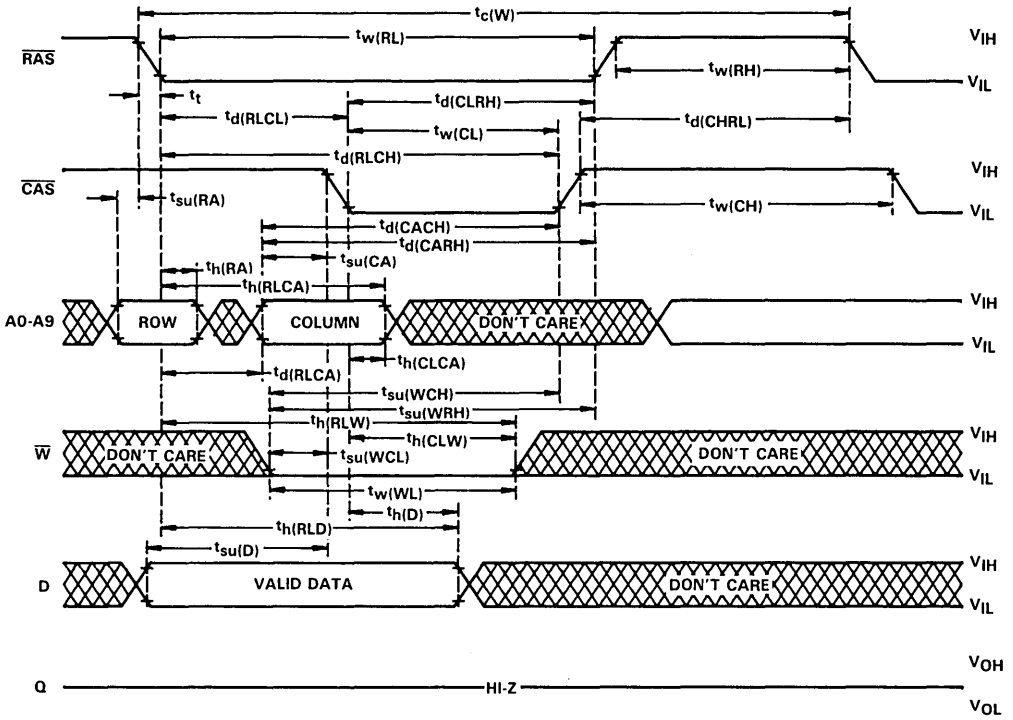


read cycle timing



NOTE 19: Output may go from high impedance to an invalid state prior to the specified access time.

early write cycle timing



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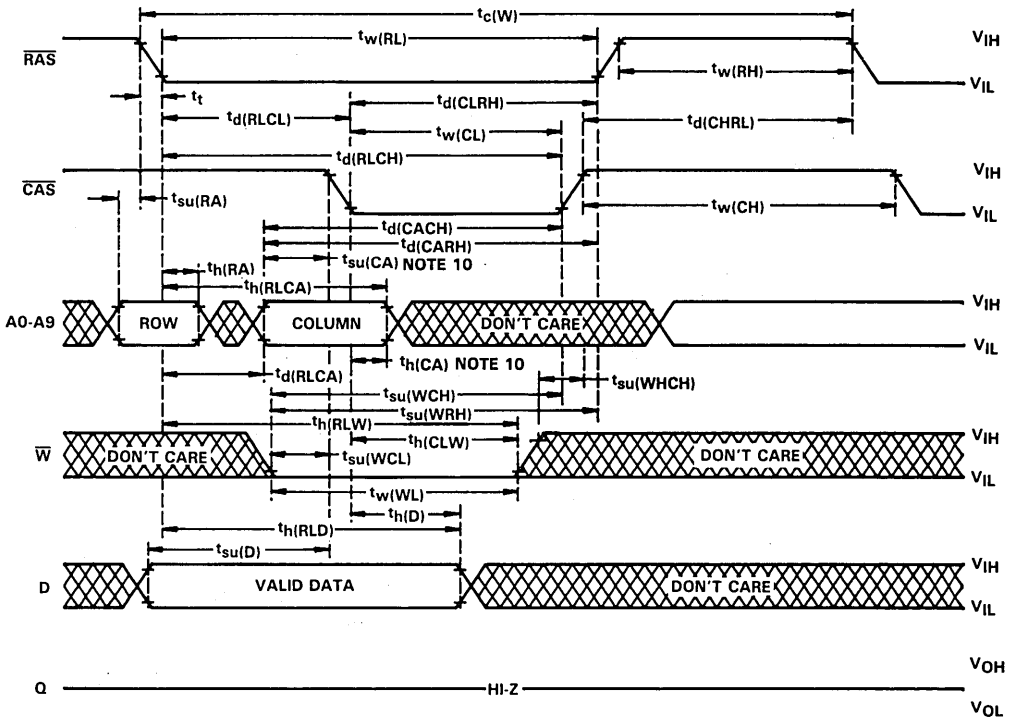
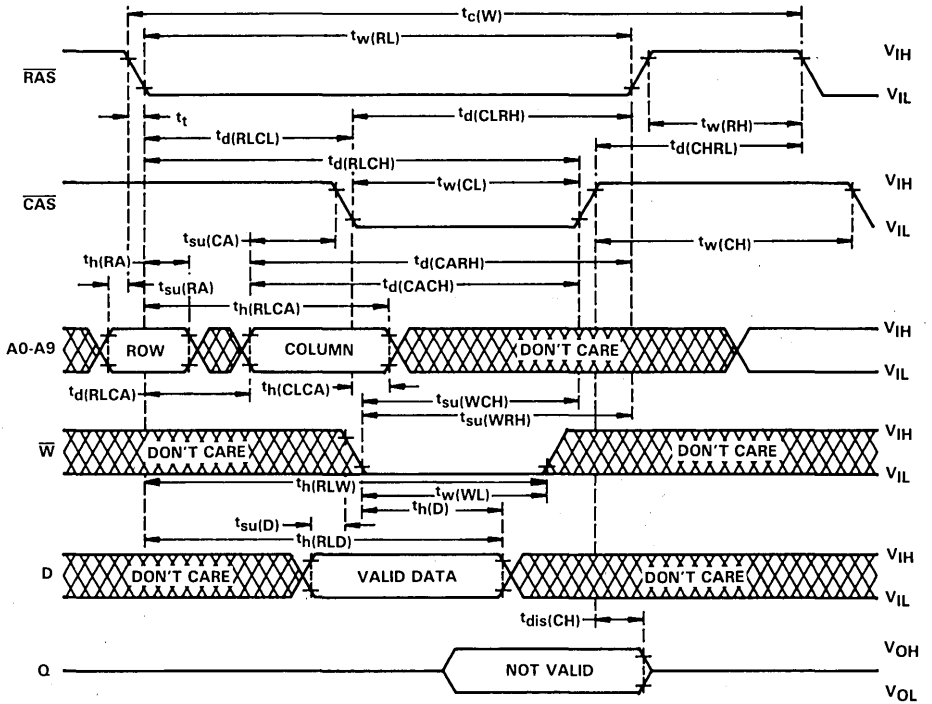
early write cycle timing



NOTE 10: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in the write operations.

write cycle timing



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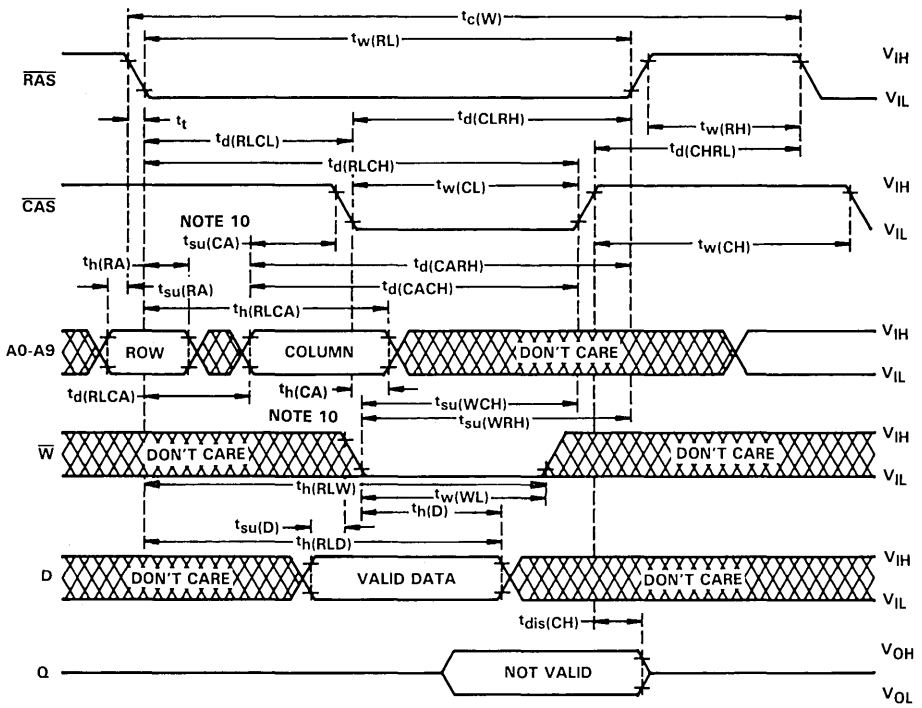
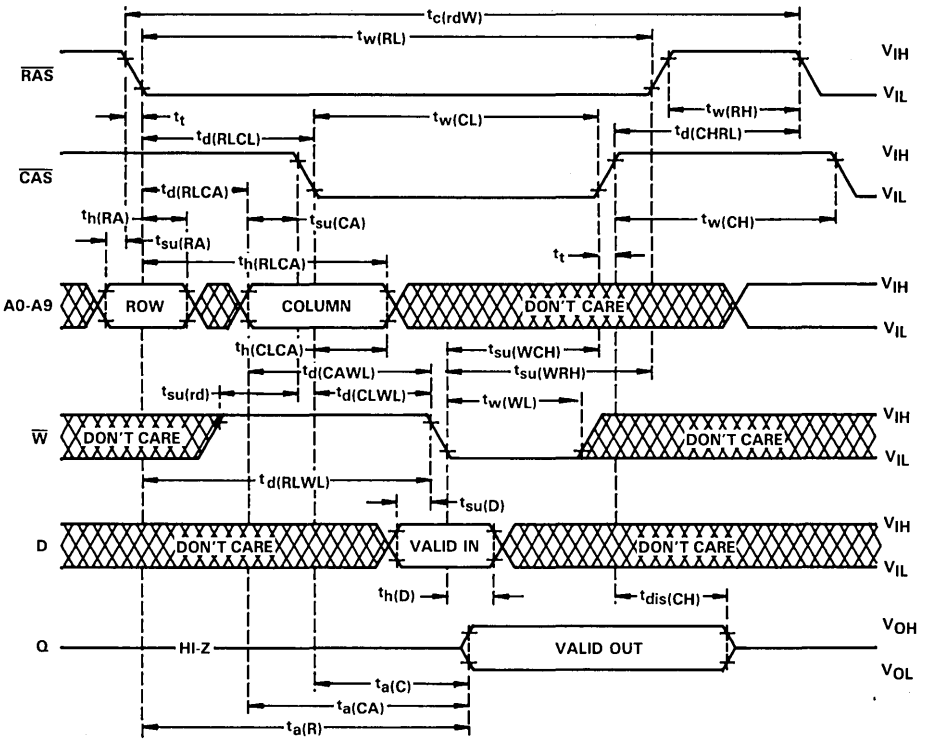
write cycle timing



NOTE 10: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in the write operation.

read-write/read-modify-write cycle timing



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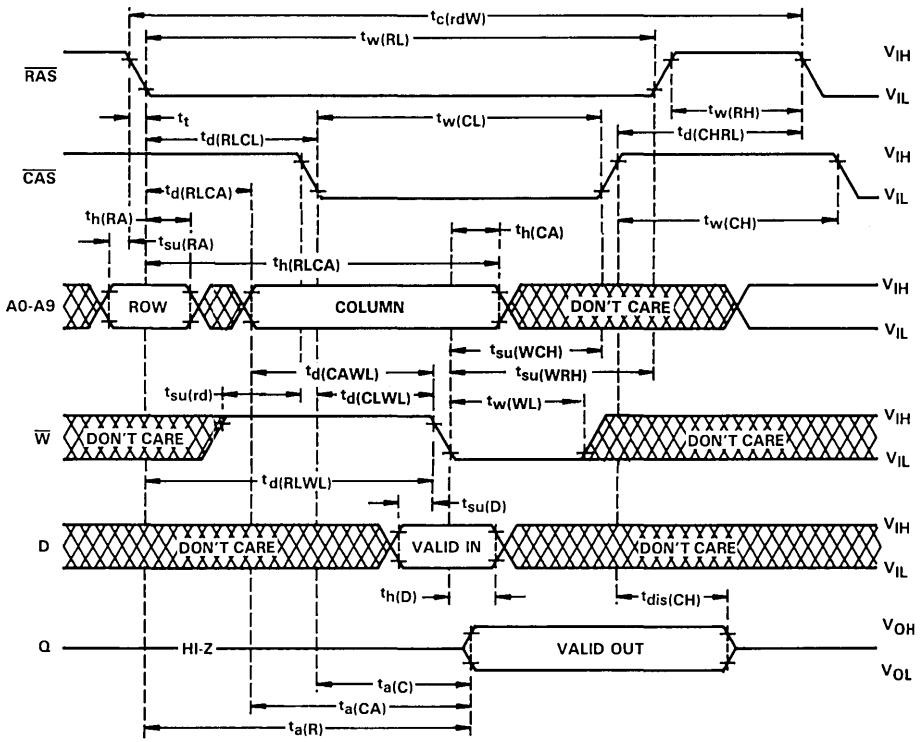
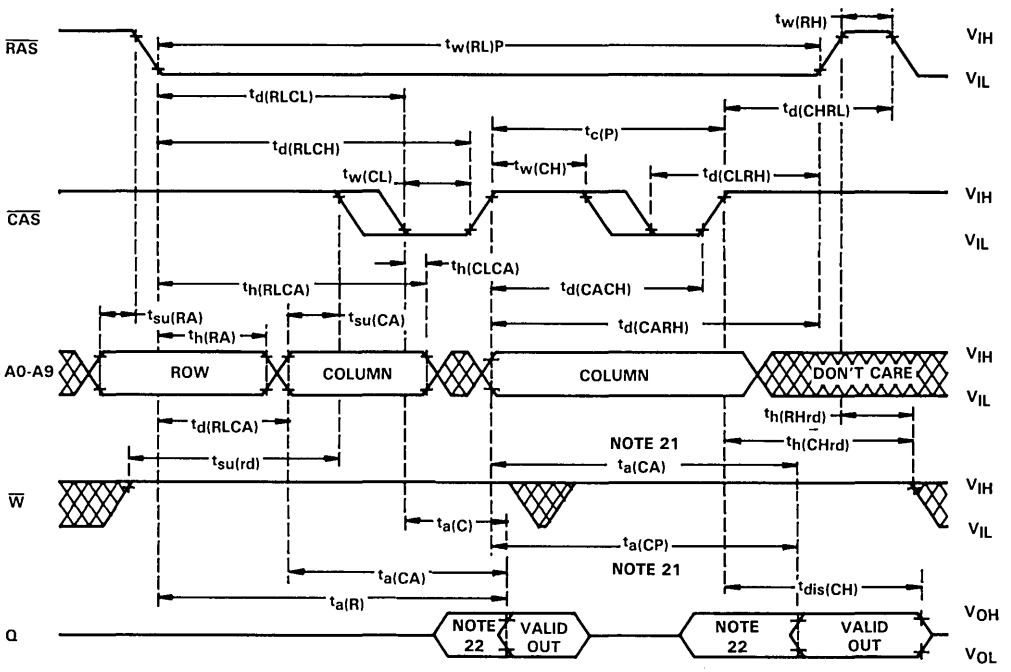
read-write/read-modify-write cycle timing

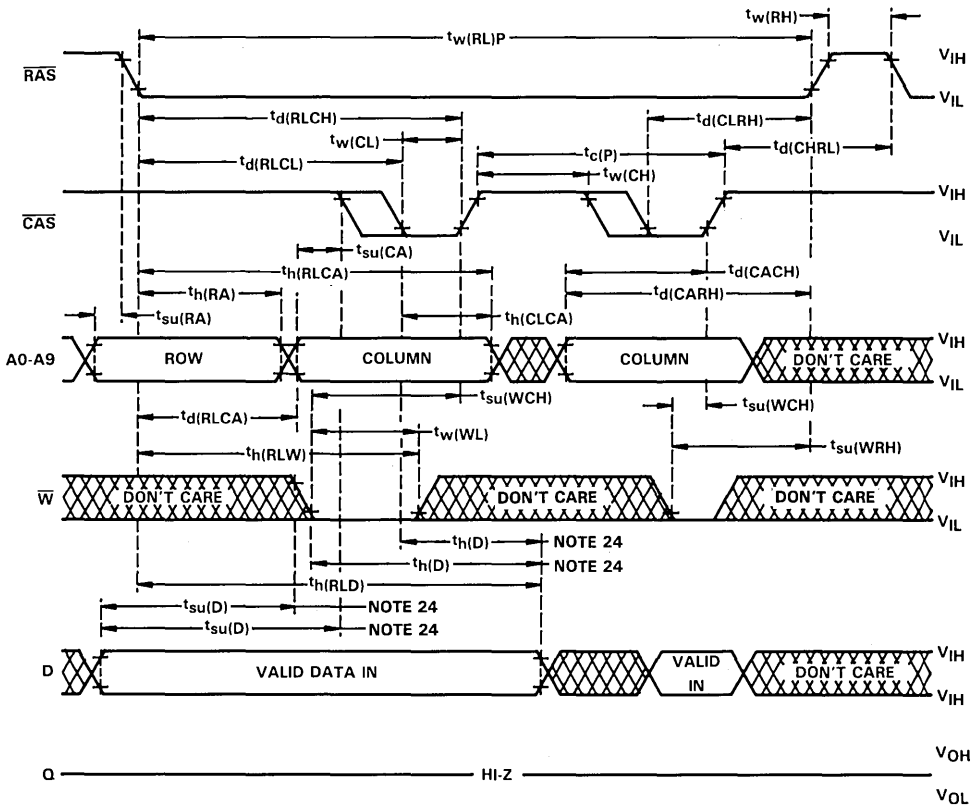


enhanced page-mode read cycle timing



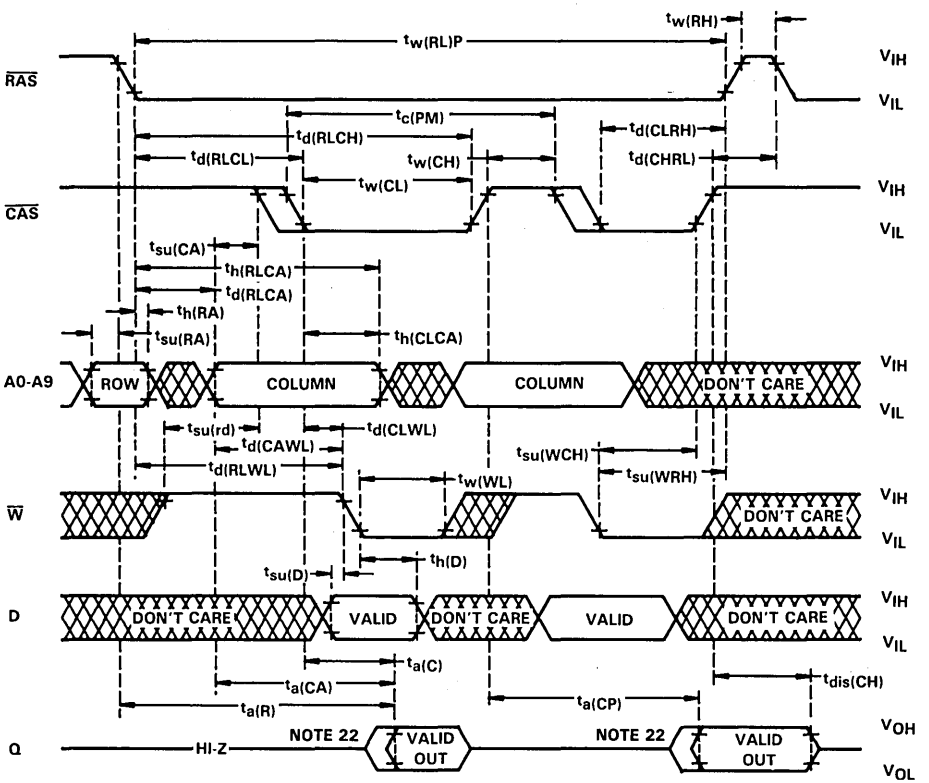
NOTES: 20. A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
21. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
22. Output may go from three-state to an invalid data state prior to the specified access time.

enhanced page-mode write cycle timing



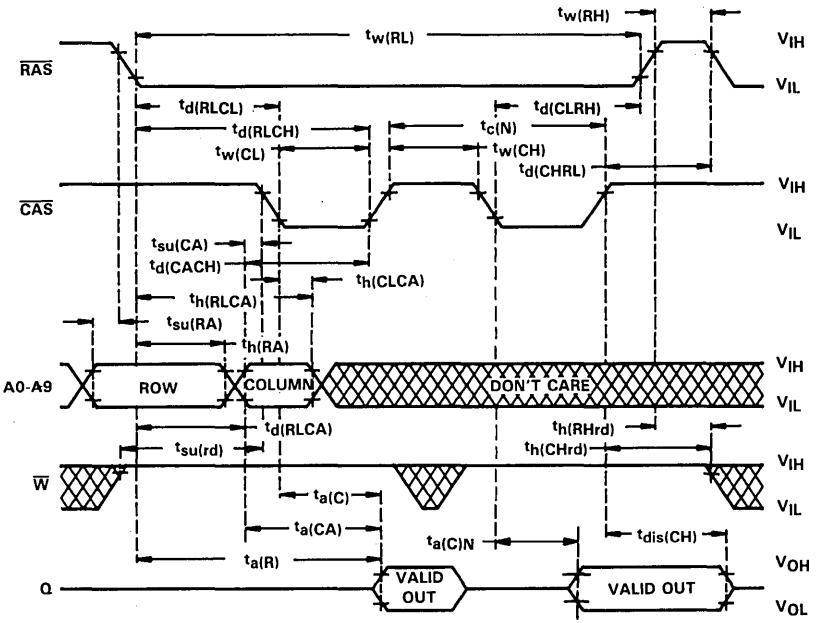
NOTES: 23. A read cycle or a read-modify-write cycles can be intermixed with write cycle as long as read and read-modify-write timing specifications are not violated.
24. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

enhanced page-mode read-modify-write cycle timing

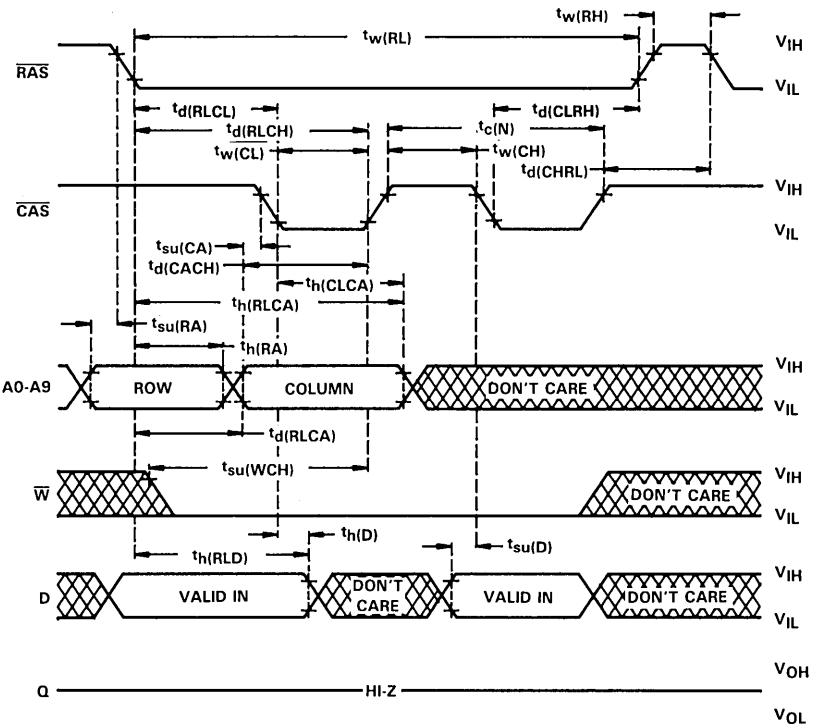


NOTES: 22. Output may go from three-state to an invalid data state prior to the specified access time.
25. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

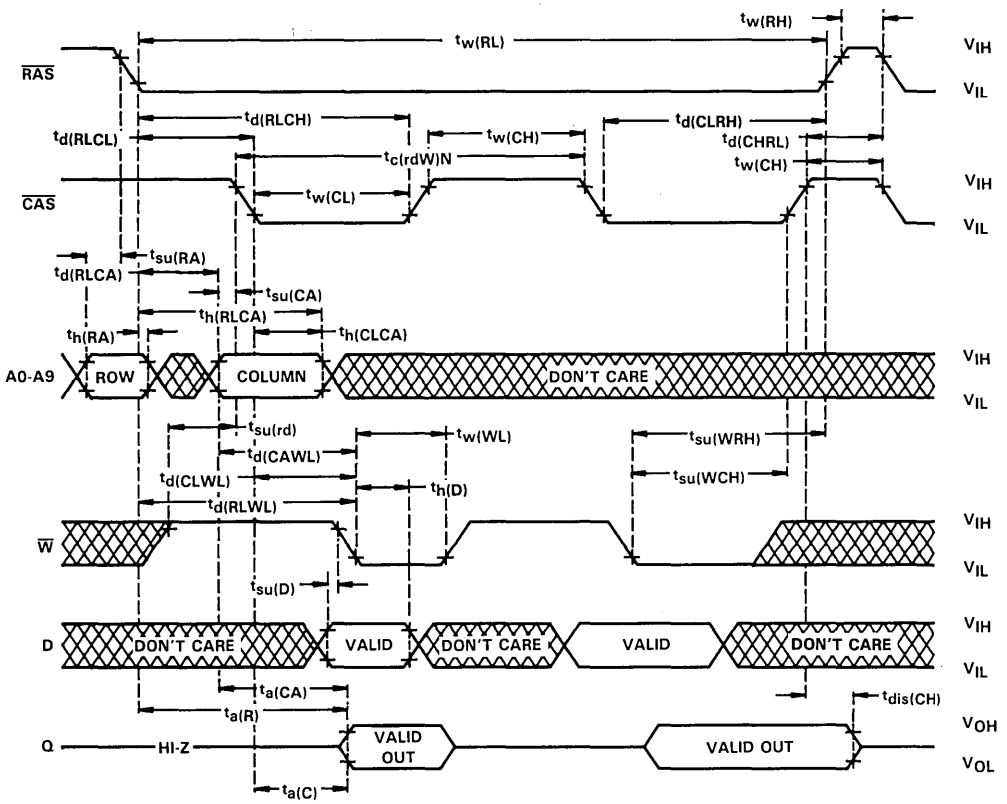
nibble-mode read cycle timing



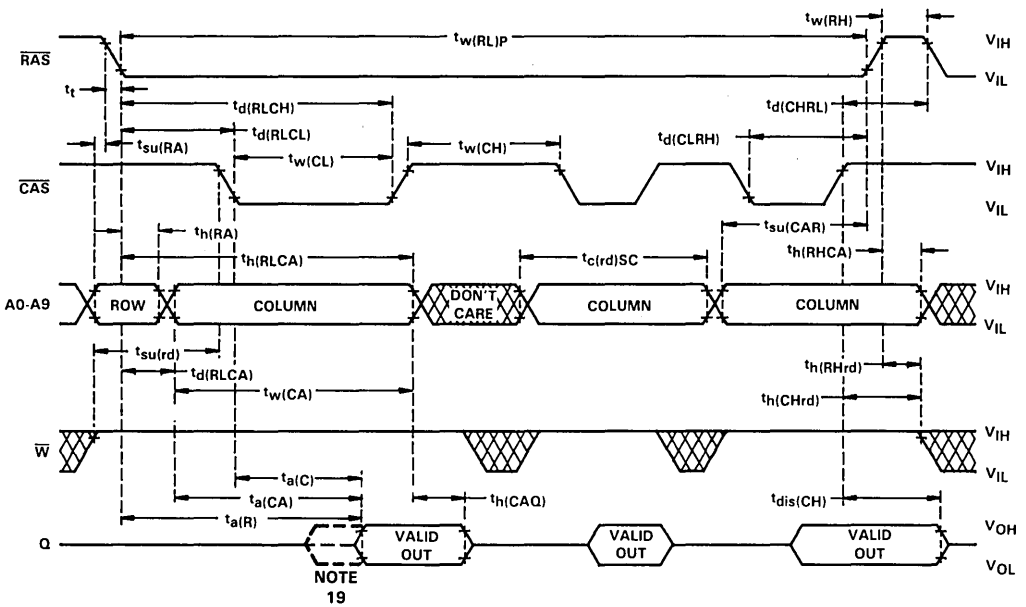
nibble-mode write cycle timing



nibble-mode read-modify-write cycle timing

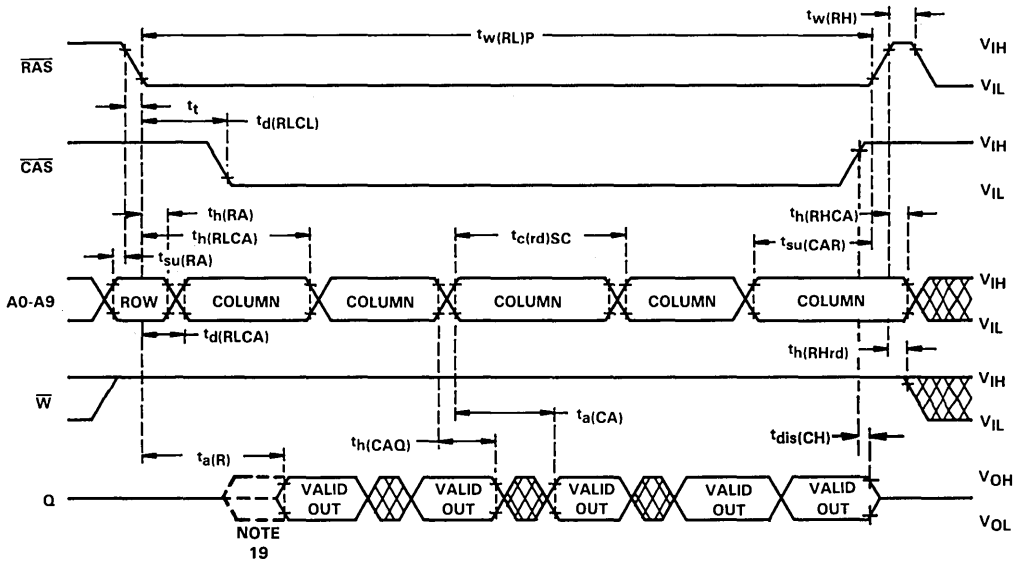


static column decode mode read timing with $\overline{CAS}$ cycling



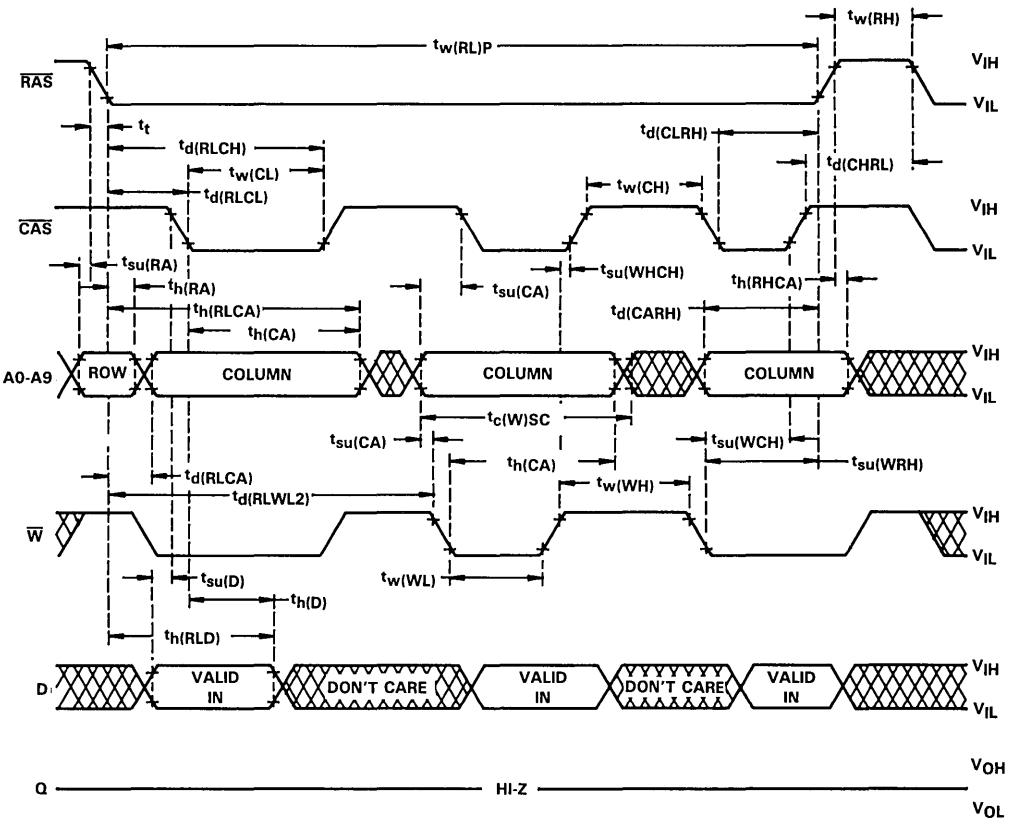
NOTE 19: Output may go from high impedance to an invalid data state prior to the specified access time.

static column decode mode read cycle timing



NOTE 19: Output may go from high impedance to an invalid data state prior to the specified access time.

static column decode mode early write cycle timing



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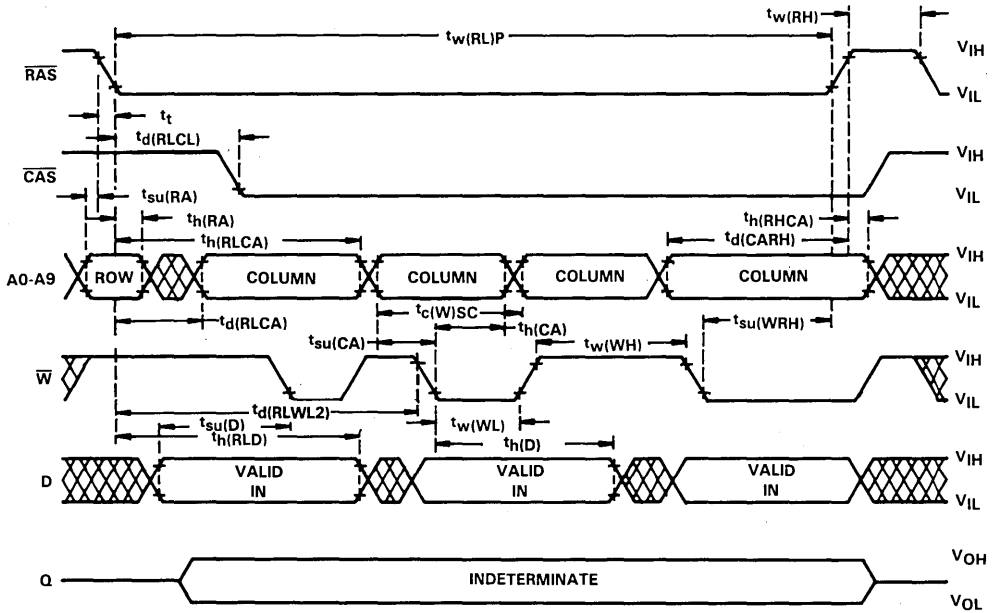
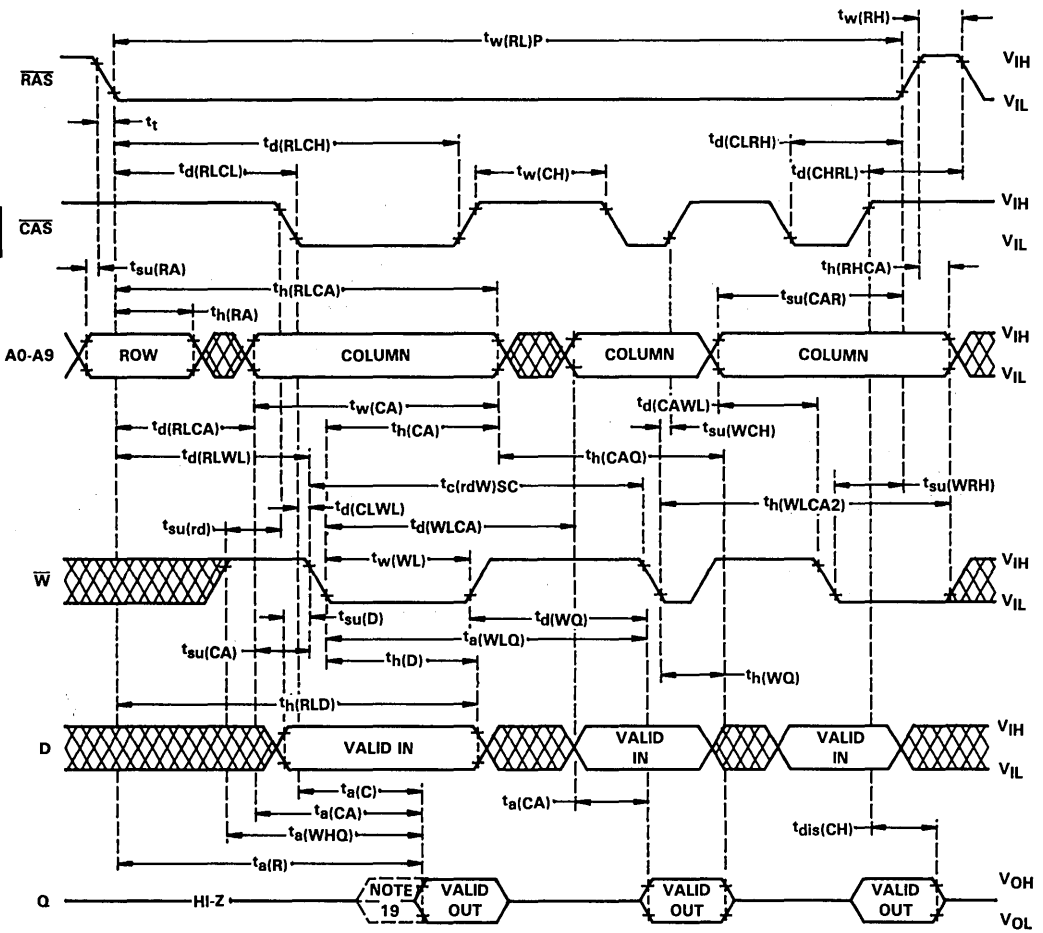
static column decode mode write cycle timing

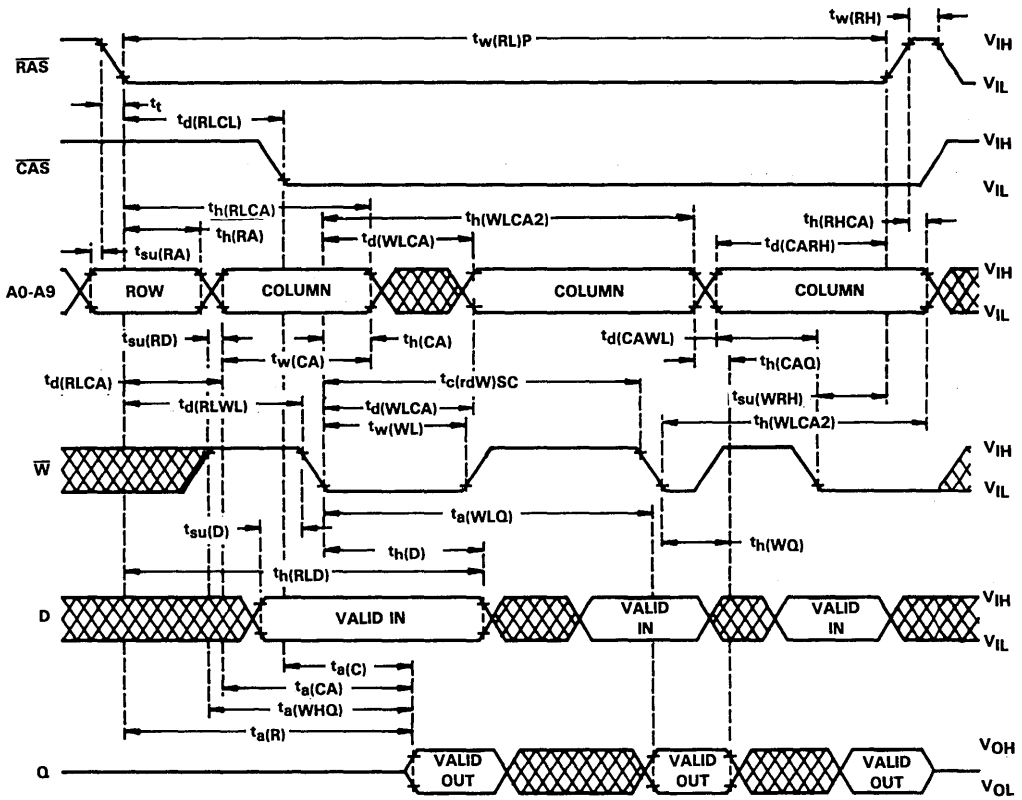


static column decode mode read-modify-write cycle timing with $\overline{CAS}$ cycling

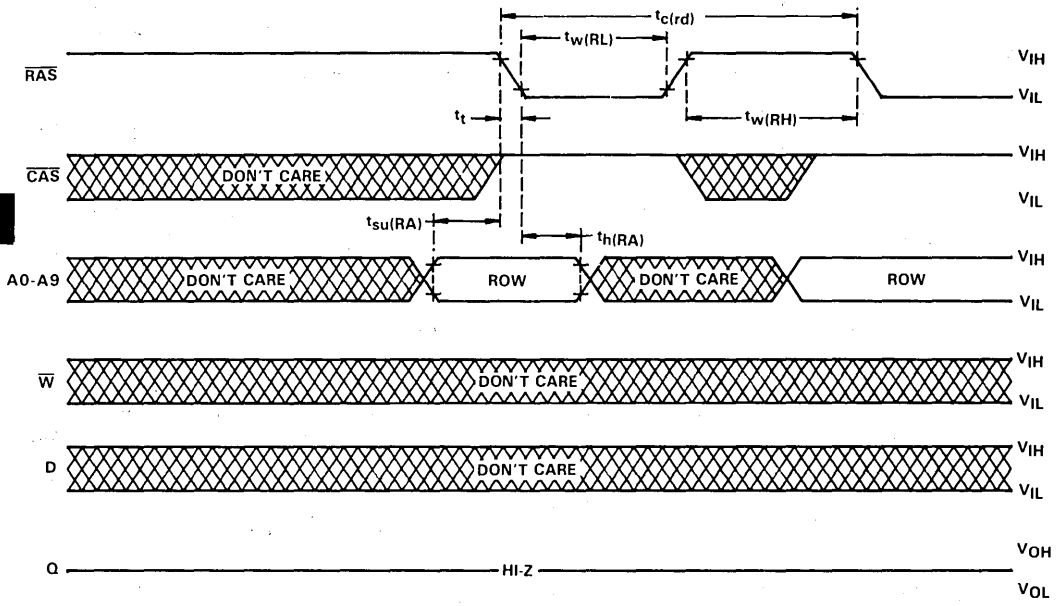


NOTE 19: Output may go from high impedance to an invalid data state prior to the specified access time.

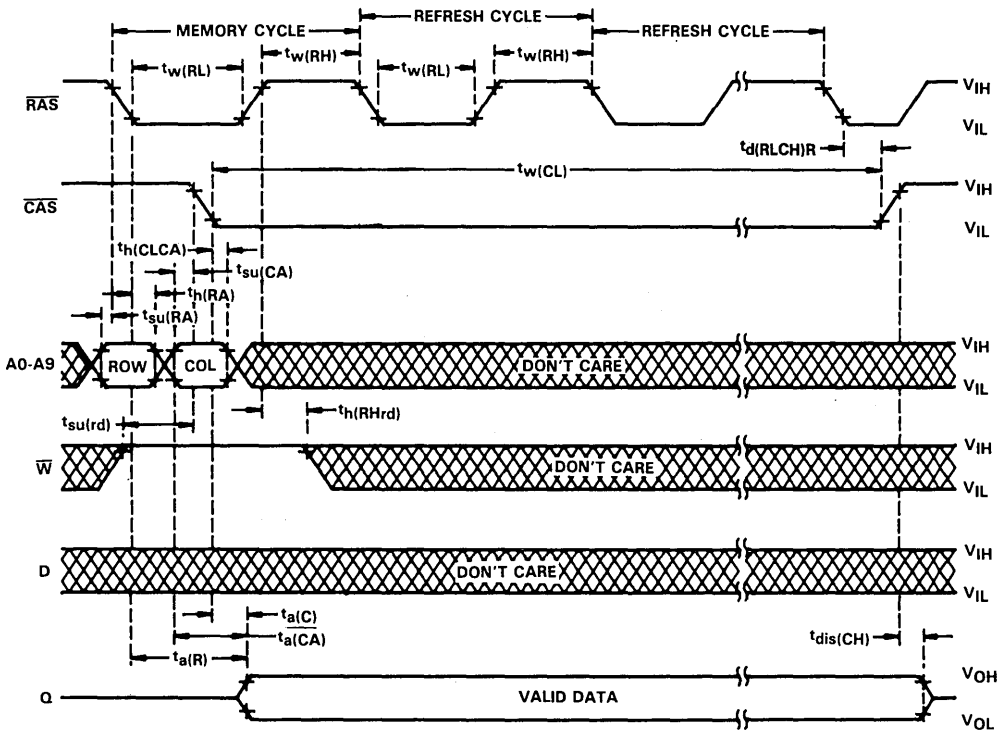
static column decode mode with read-modify-write cycle timing



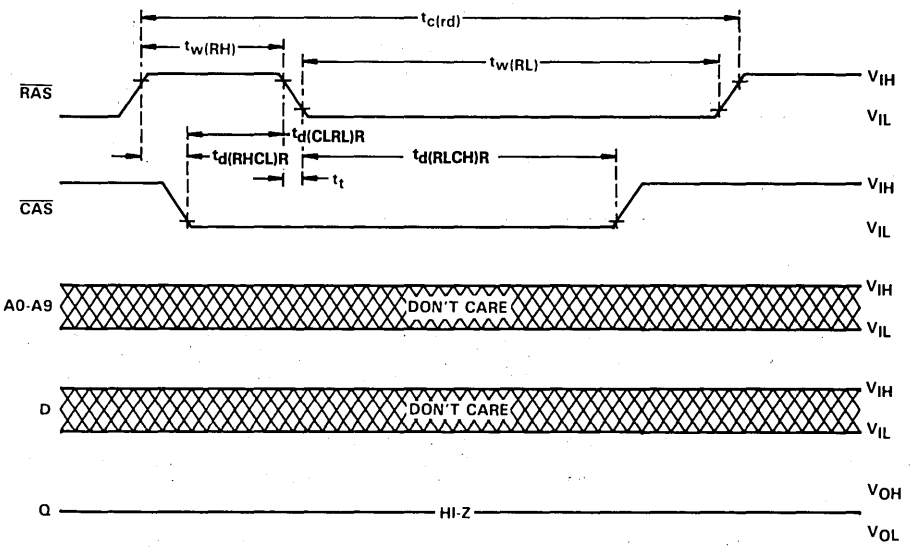
$\overline{RAS}$ only refresh timing



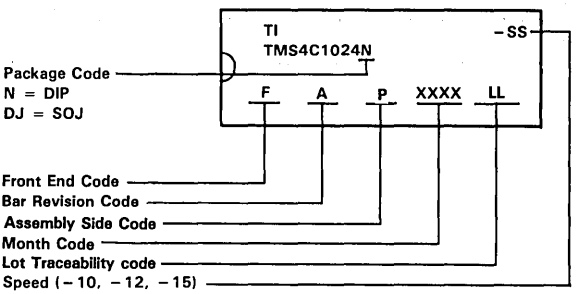
hidden refresh cycle



automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh timing



device symbolization



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SUPPORT LITERATURE AVAILABLE

The following literature is available from Texas Instruments for assistance in DRAM design. Please contact your local TI sales office to obtain a copy.

1 MEGABIT DRAM FAMILY DATA SHEETS

- TMS44C256 — Specifications for the 1 Megabit DRAM organized 256K × 4 with enhanced page mode access. (SMGS256)
- TMS44C257 — Specifications for the 1 Megabit DRAM organized 256K × 4 with static column decode. (SMGS257)

Single-In-Line Package Memory Modules

- TM024GAD8, TM024EAD9 — Specifications for the socketable 1 Megabit × 8 and 1 Megabit × 9 Single-In-line Package memory modules. (SMMS102C)
- TM024HAC4 — Specifications for the leaded 1 Megabit × 4 Single-In-line Package memory module. (SMMS104A)

DESIGN CONSIDERATIONS

- Megabit DRAM Topology — The information in this report is useful in developing algorithms for cell sensitivity tests on TI's 1 Megabit DRAM configurations. (SMGA001)

TECHNICAL ARTICLE REPRINTS

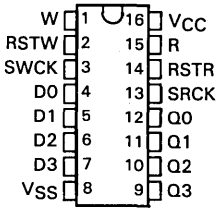
- 1 Megabit Memories Demand New Design Choices — Discusses technical, technological, operational, and packaging issues pertaining to Megabit DRAMs. (SMZY018)
- 1-Megabit DRAMs Spark Tech Advances — Chip designers are proposing technological changes promising to significantly alter the design and layout landscape of the next generation of memory boards. (SMZY020)

- 262,144 × 4 Organization
- Single 5-V Power Supply (± 10% Tolerance)
- FIFO (First-In First-Out) Operation
  - Full Word Continuous Read/Write
  - Asynchronous Read/Write
- Quasi-Static (Refresh Free)
- High Speed Read/Write Cycle (30 ns Min)

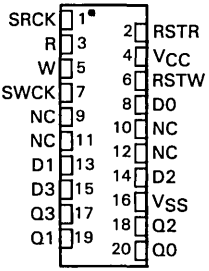
	ACCESS TIME (MAX)	CYCLE TIME READ (MIN)	CYCLE TIME WRITE (MIN)
TMS4C1050-3	25 ns	30 ns	30 ns
TMS4C1050-4	30 ns	40 ns	40 ns
TMS4C1050-6	50 ns	60 ns	60 ns

- Low Power Dissipation (Average I_{DD} = 50 mA at Minimum Cycle)
- On-Chip Substrate Bias Generator
- 1 Megabit CMOS DRAM Compatible Process Technology
- Texas Instruments EPIC™ (Enhanced Process Implanted CMOS) Technology
- Operating Free-Air Temperature . . . 0°C to 70°C

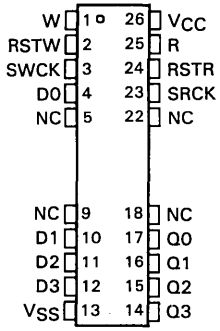
N PACKAGE
(TOP VIEW)



SD PACKAGE
(TOP VIEW)



DJ PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
D0-D3	Data-In
Q0-Q3	Data-Out
R	Read Enable
RSTR	Reset Read
RSTW	Reset Write
SRCK	Serial Read Clock
SWCK	Serial Write Clock
V_{CC}	5-V Supply
V_{SS}	Ground
W	Write Enable

description

The TMS4C1050 provides four-bit parallel and asynchronous serial read and write operations (first-in first-out feature) with each bit furnishing access to 262,144 words.

The device employs state-of-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability and lower power at low cost.

A dynamic data storage cell is employed as the main data memory to achieve high density. Arbitration logic is implemented in the TMS4C1050, supplying a refresh-free system. The built-in arbitration logic prevents any conflict between data-saving, data-loading, and memory-refresh requests.

The TMS4C1050 is offered in a 16-pin plastic dual-in-line package (N suffix) designed for insertion in mounting hole rows on 7,62-mm (300-mil) centers. This device is also offered in a 20-pin 400-mil zig-zag in-line package (SD suffix) and a 300-mil 20/26-lead plastic surface mount SOJ package (DJ suffix). The latter two versions of the TMS4C1050 are still in development, and the ADVANCE INFORMATION notices in this data sheet pertain only to the SD and DJ packaged devices.

The TMS4C1050 is guaranteed for operation from 0°C to 70°C (L suffix).

EPIC is a trademark of Texas Instruments Incorporated.

operation

write enable (W)

W is used as a D enable/disable. A logic high on the W input enables the input and a logic low disables the input and holds the internal write address pointer (head address). W disable time (low) can be expanded to 1 ms. In case W is held low over 1 ms, an RSTW operation will be required to achieve proper write operation. Note that W setup times are referenced to the rising edge of SWCK for D enable/disable.

reset write (RSTW)

RSTW input initializes the write address pointer (head address). RSTW setup and hold times [$t_{su(RW)}$, $t_{h(RW)}$] are referenced to the rising edge of SWCK.

serial write clock (SWCK)

The SWCK input latches the data inputs on chip when W is high and also increments the internal write address pointer.

data inputs (D0-D3)

Data is shifted in the data registers on the rising edge of SWCK when W is high. D setup and hold times [$t_{su(D)}$, $t_{h(D)}$] are referenced to the rising edge of SWCK.

read enable (R)

R is used as a Q enable/disable. A logic high on the R input enables the output and a logic low disables the output and holds the internal read address pointer. The outputs are in the high-impedance (floating) state as long as R is held low. R disable time (low) is required below 1 ms. If R is held low over 1 ms, an RSTR operation will be required to achieve the proper read operation. Note that R setup times are referenced to the rising edge of SRCK for Q enable/disable.

reset read (RSTR)

RSTR input initializes the read address pointer (head address). RSTR setup and hold times [$t_{su(RR)}$, $t_{h(RR)}$] are referenced to the rising edge of SRCK.

serial read clock (SRCK)

Data is shifted out of the data registers on the rising edge of SRCK when R is high during the read operation. The SRCK input increments the internal read address pointer when R is high.

data output (Q0-Q3)

The three-state output buffer provides direct TTL compatibility (no pull-up resistors required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output becomes valid after the access time interval $t_{a(RC)}$ that begins with the positive transition of SRCK. Q valid times [$t_{v(RCH)}$] are referenced to the rising edge of SRCK in the next cycle.

write cycle

The write operation is controlled by three clocks, SWCK, RSTW, and W. It is accomplished by cycling SWCK and holding W high after the write address pointer reset operation (RSTW). To transfer the last data in data register to memory array, a RSTW operation at W low is required after the write operation. The write operation must be performed by a minimum of 120 write cycles.

read cycle

The read operation is controlled by three clocks, SRCK, RSTR, and R. It is accomplished by cycling SRCK and holding R high after the read address pointer reset operation (RSTR).

power up

To achieve proper device operation, an initial pause of 100 μs is required after each power-up to the full V_{CC} level followed by a minimum of one (1) SWCK and SRCK cycle for each write and read respectively. After power-up, write/read address pointers are not valid. RSTW and RSTR operations must be performed to initialize the write/read address pointers.

new data access

To access the new data, the SWCK must be brought high at least 600 cycles ahead of the SRCK.

old data access

To access the previously preserved data, the SWCK must be brought high less than 120 cycles ahead of the SRCK.

absolute maximum ratings over operating free air temperature range (unless otherwise noted)†

Voltage range on any pin except Q0-Q3 (see Note 1) . . . . . −1.0 V to 7.0 V
Voltage range on Q0-Q3 (see Note 1) . . . . . −1.0 V to V_{CC} + 0.3 V
Voltage range on V_{CC} (see Note 1) . . . . . 0.0 V to 7.0 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1.0 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, all voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.6		V_{CC}+1	V
V_{IL}	Low-level input voltage (see Note 2)	−1.0		0.8	V
T_A	Operating free-air temperature	0	25	70	°C

NOTE 2: V_{IL} = −1.5 V undershoot is allowed when device is operated in the range of recommended supply voltage.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4C1050-3		TMS4C1050-4		TMS4C1050-6		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, R low		±10		±10		±10	μA
I_{DD1}	Average operating current	Minimum write/read cycle, output open		50		45		35	mA
I_{DD2}	Standby current	After 1 RSTW/RSTR cycle, W and R low, V_{IL} = 0.8 V				7		7	mA
		After 1 RSTW/RSTR cycle, W and R low, V_{IL} = 0 V				5		5	

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz‡

PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
C_i Input capacitance	V_I = 0 V, f = 1 MHz		7	pF
C_o Output capacitance	V_I = 0 V, f = 1 MHz		10	pF

‡Capacitance measurements are made on sample basis only.

switching characteristics over recommended supply voltage range and operating free-air temperature range

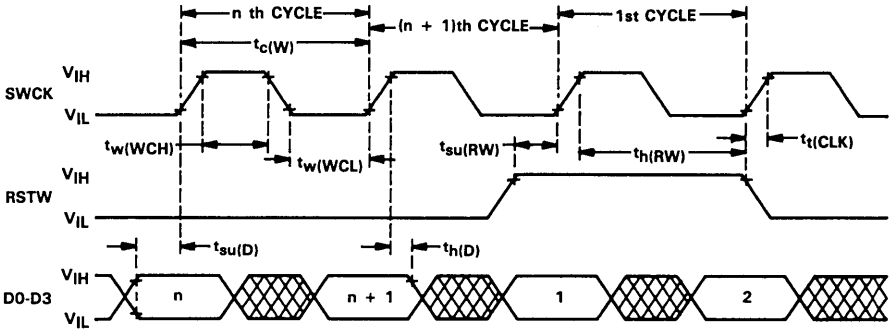
PARAMETER		TEST CONDITIONS	TMS4C1050-3		TMS4C1050-4		TMS4C1050-6		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(RC)}$	Access time from SRCK high	C_L = 50 pF		25		30		50	ns
$t_{v(RCH)}$	Output disable time after SRCK high	C_L = 50 pF	6		6		6		ns
$t_{v(RL)}$	Output disable time after R low	C_L = 50 pF	10		10		10		ns

timing requirements over recommended supply voltage range and operating free-air temperature range (see Notes 1, 3, and 4)

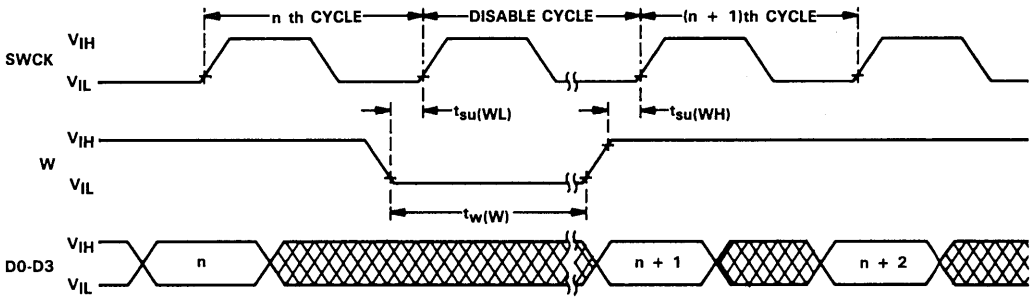
		TMS4C1050-3		TMS4C1050-4		TMS4C1050-6		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time (see Notes 5 and 6)	30	10^6	40	10^6	60	10^6	ns
$t_{c(R)}$	Read cycle time (see Notes 5 and 6)	30	10^6	40	10^6	60	10^6	ns
$t_{w(WCH)}$	Pulse duration, SWCK high (see Note 6)	12		17		20		ns
$t_{w(WCL)}$	Pulse duration, SWCK low (see Note 6)	12		17		20		ns
$t_{su(D)}$	Data setup time before SWCK high	5		5		5		ns
$t_{h(D)}$	Data hold time after SWCK high	10		10		10		ns
$t_{su(WL)}$	W low setup time before SWCK high	0		0		0		ns
$t_{su(WH)}$	W high setup time before SWCK high	0		0		0		ns
$t_{w(W)}$	Pulse duration, W low (see Notes 5 and 6)	10	10^6	15	10^6	20	10^6	ns
$t_{su(RW)}$	RSTW setup time before SWCK high (see Note 7)	0		0		0		ns
$t_{h(RW)}$	RSTW hold time after SWCK high (see Note 7)	10		15		20		ns
$t_{w(RCH)}$	Pulse duration, SRCK high (see Note 6)	12		17		20		ns
$t_{w(RCL)}$	Pulse duration, SRCK low (see Note 6)	12		17		20		ns
$t_{su(RL)}$	R low setup time before SRCK high	0		0		0		ns
$t_{su(RH)}$	R high setup time before SRCK high	0		0		0		ns
$t_{w(RL)}$	Pulse duration, R low (see Notes 5 and 6)	10	10^6	15	10^6	20	10^6	ns
$t_{su(RR)}$	RSTR setup time before SRCK high (see Note 7)	0		0		0		ns
$t_{h(RR)}$	RSTR hold time after SRCK high (see Note 7)	10		15		20		ns
t_t	Transition time	3	30	3	30	3	30	ns

NOTES: 1. Under absolute maximum ratings, all voltage values are with respect to V_{SS}.
3. Timing measurements are referenced to V_{IH} min = 2.4 V and V_{IL} max = 0.8 V. t_t is measured between V_{IH} min and V_{IL} max.
4. All cycle times assume t_t = 3 ns.
5. No restriction for maximum value as long as the write and read address pointers are addressing the first addresses.
6. When the write and read address pointers are not addressing the first addresses, $t_{c(W)}$, $t_{c(R)}$, $t_{w(WCH)}$, $t_{w(WCL)}$, $t_{w(W)}$, $t_{w(RCH)}$, $t_{w(RCL)}$, and $t_{w(RL)}$ must be less than 1 ms. After improper operation [$t_{su(RW)}$ over 1 ms], RSTW or RSTR cycle is required to initialize the write or read address pointer.
7. Reset operation is not guaranteed in case $t_{su(RW)}$, $t_{h(RW)}$, $t_{su(RR)}$, and $t_{h(RR)}$ do not meet the specification.

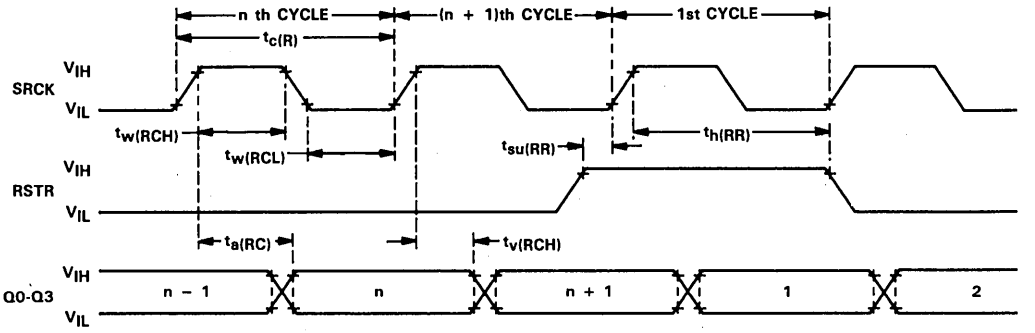
write cycle timing (reset write)



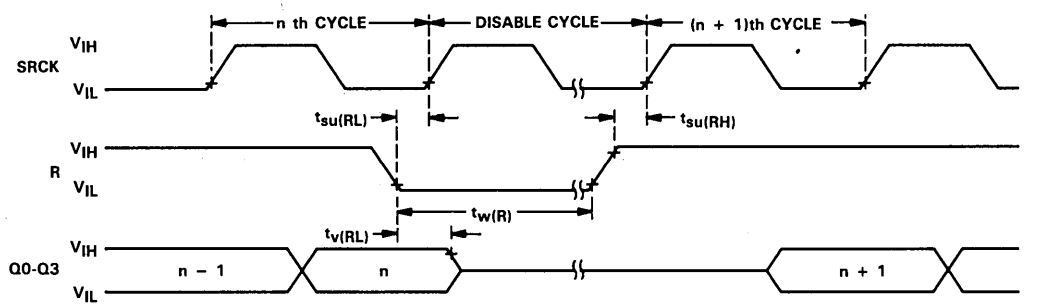
write cycle timing (write enable)



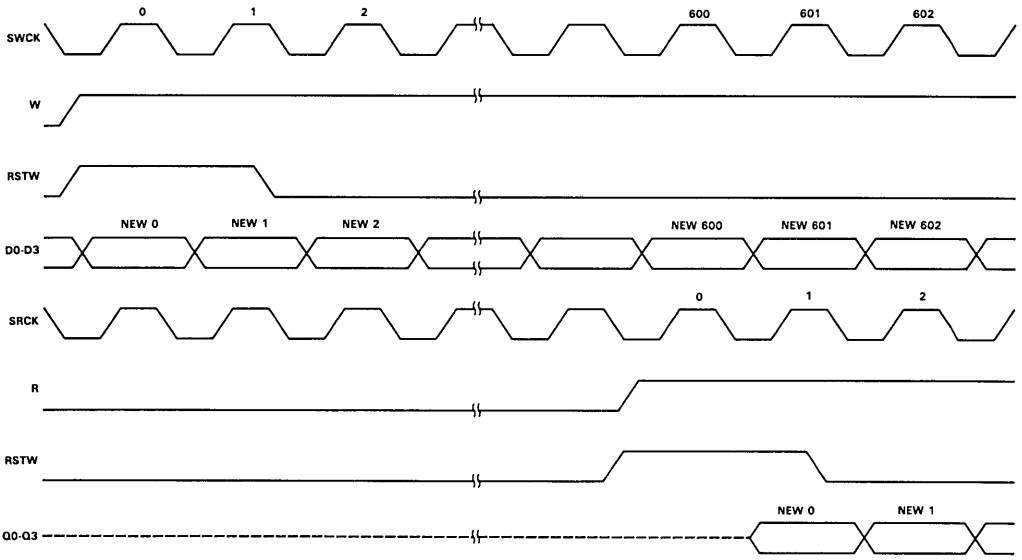
read cycle timing (reset read)



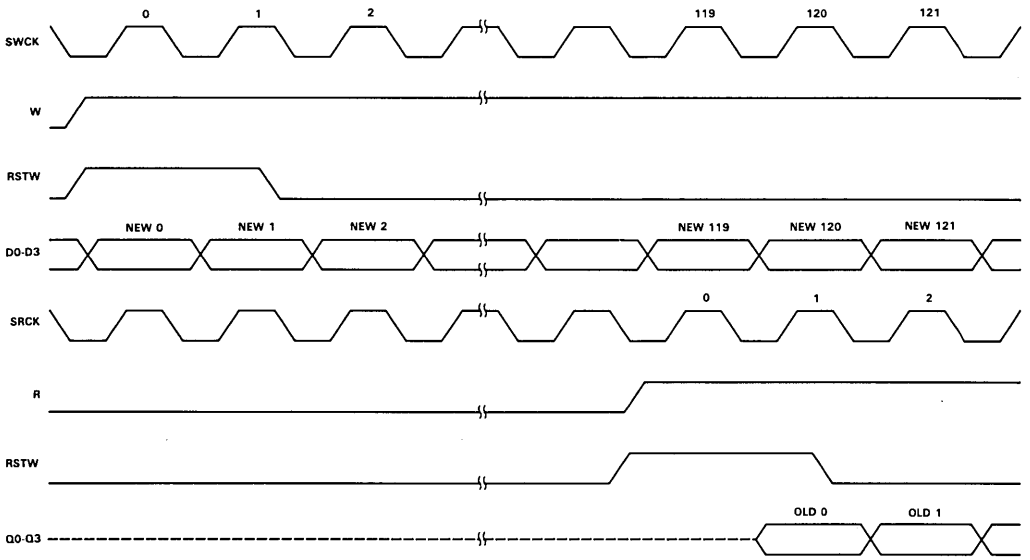
read cycle timing (read enable)



new data access mode



old data access mode



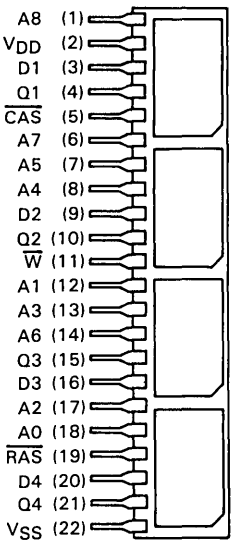
SEPTEMBER 1985—REVISED MAY 1988

- 262,144 × 4 Organization
- Single 5-V Supply (10% Tolerance)
- 22-Pin Single-In-line Package (SIP)
- Utilizes Four 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS4256-10	100 ns	50 ns	200 ns
TMS4256-12	120 ns	60 ns	230 ns
TMS4256-15	150 ns	75 ns	260 ns

- Common $\overline{CAS}$ Control with Separate Data Input and Output Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0°C to 70°C

TM4256EC4 . . . C SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE TM4256EC4	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D1-D4	Data Inputs
Q1-Q4	Data Outputs
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4256EC4 series is a 1024K, dynamic random-access memory module, organized as 262,144 × 4 bits in a 22-pin single-in-line package comprising four TMS4256FML, 262,144 × 1 bit dynamic RAMs in 18-lead plastic chip-carriers mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing, the TM4256EC4 has a density of ten devices per square inch (approximately 4 × the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated through-holes, a cost savings can be realized.

Each TMS4256FML is described in its data sheet and is fully electrically tested and processed according to TI MIL-STD-883B flows (as amended for commercial applications) prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed.

The TM4256EC4 features $\overline{RAS}$ access times of 100 ns, 120 ns, and 150 ns maximum.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4256EC4 is rated for operation from 0°C to 70°C.

operation

The TM4256EC4 operates as four TMS4256FMLs connected as shown in the functional block diagram. Refer to the TMS4256 data sheet for details of operation.

specifications

For TMS4256FML electrical specifications, refer to the TMS4256 data sheet.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

TEXAS INSTRUMENTS
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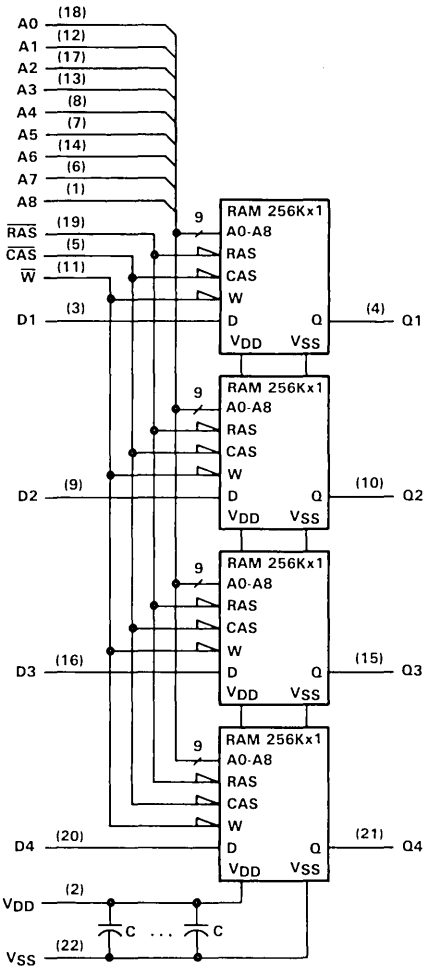
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin, including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 4 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4256EC4-10		TM4256EC4-12		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4	V_{DD}	2.4	V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0	0.4	0	0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V		±10		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high		±10		±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		280		260	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		18		18	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		232		212	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		200		180	mA

‡I_{DD1}-I_{DD4} are measured with Q1-Q4 in the same mode (i.e., operating, standby, refresh, page mode).

TEXAS INSTRUMENTS
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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4256EC4-15 MIN	TM4256EC4-15 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4	V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0	0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high		±10	μA
I_{DD1}†	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		240	mA
I_{DD2}†	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		18	mA
I_{DD3}†	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		192	mA
I_{DD4}†	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		160	mA

†I_{DD1}-I_{DD4} are measured with Q1-Q4 in the same mode (i.e., operating, standby refresh, page mode).

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		20	pF
$C_{i(D)}$	Input capacitance, data inputs		5	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input		20	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		28	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input		20	pF
$C_{o(Q)}$	Output capacitance, data outputs		7	pF
$C_{o(VDD)}$	Decoupling capacitance	0.4		μF

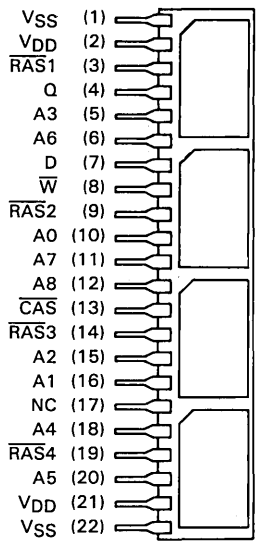
OCTOBER 1985—REVISED FEBRUARY 1988

- 1,048,576 × 1 Organization
- Single 5-V Supply (10% Tolerance)
- 22-Pin Single-In-line Package (SIP)
- Utilizes Four 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS4256-10	100 ns	50 ns	200 ns
TMS4256-12	120 ns	60 ns	230 ns
TMS4256-15	150 ns	75 ns	260 ns

- Common $\overline{CAS}$ Control with Separate Data Input and Output Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0°C to 70°C

TM4256FC1 . . . C SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data Input
NC	No Connection
Q	Data Output
$\overline{RAS}$1-$\overline{RAS}$4	Row-Address Strobes
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4256FC1 series are 1024K, dynamic random-access memory modules organized as 1,048,576 × 1 bit in a 22-pin single-in-line package comprising four TMS4256FML, 262,144 × 1 bit dynamic RAMs in 18-lead plastic chip carriers mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing, the TM4256FC1 has a density of ten devices per square inch (approximately 4 × the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated through-holes, a cost savings can be realized.

Each TMS4256FML is described in its data sheet and is fully electrically tested and processed according to TI MIL-STD-883B flows (as amended for commercial applications) prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed.

The TM4256FC1 features $\overline{RAS}$ access times of 100 ns, 120 ns, and 150 ns maximum.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data-in are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4256FC1 is rated for operation from 0°C to 70°C.

operation

The TM4256FC1 operates as four TMS4256FMLs connected as shown in the functional block diagram. Refer to the TMS4256 data sheet for details of operation.

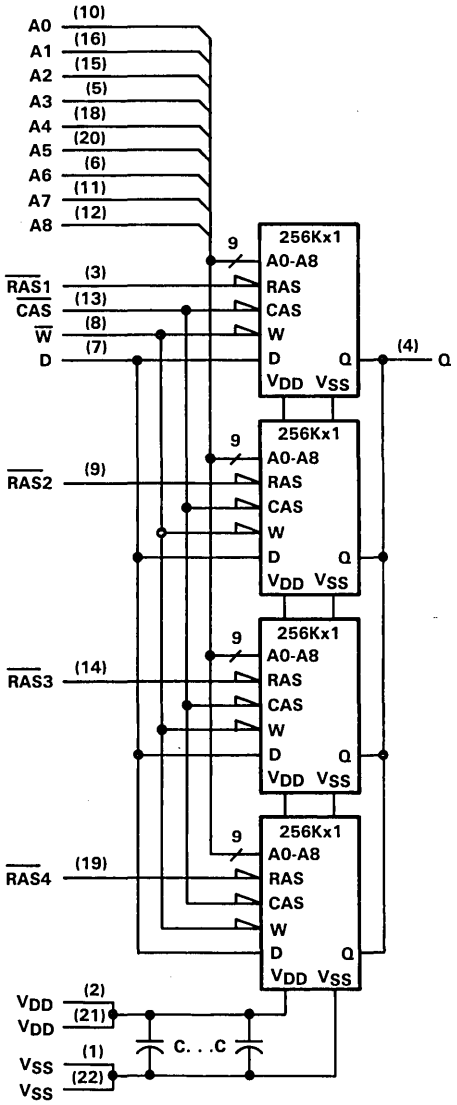
specifications

For TMS4256FML electrical specifications, refer to the TMS4256 data sheet.

single-in-line package and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness epoxy-glass
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin, including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 4 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4256FC1-10		TM4256FC1-12		TM4256FC1-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4	V_{DD}	2.4	V_{DD}	2.4	V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high		±10		±10		±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle Output open‡		80		75		70	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		18		18		18	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, Output open		232		212		192	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, Output open‡		50		45		40	mA

‡Assuming standard operation of one device access.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

	PARAMETER	MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		20	pF
$C_{i(D)}$	Input capacitance, data inputs		20	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input		5	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		28	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input		20	pF
$C_{o(Q)}$	Output capacitance, data output		28	pF
$C_{o(VDD)}$	Decoupling capacitance	0.4		μF

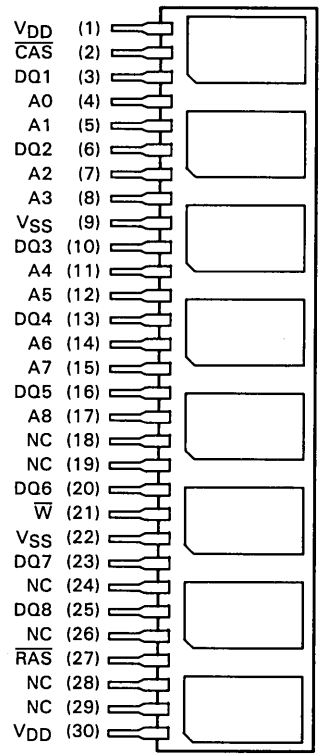
OCTOBER 1985—REVISED FEBRUARY 1988

- 262,144 × 8 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-In-line Package (SIP)
  - —Pinned Module for Through-Hole Insertion (TM4256FL8)
  - —Leadless Module for Use with Sockets (TM4256GU8)
- Utilizes Eight 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS4256-10	100 ns	50 ns	200 ns
TMS4256-12	120 ns	60 ns	230 ns
TMS4256-15	150 ns	75 ns	260 ns

- Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0°C to 70°C

TM4256FL8 . . . L SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE TM4256FL8	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4256__8 series are 2048K, dynamic random-access memory modules organized as 262,144 × 8 bits in a 30-pin single-in-line package comprising eight TMS4256FML, 262,144 × 1 bit dynamic RAMs in 18-lead plastic chip carriers mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing, the TM4256__8 has a density of ten devices per square inch (approximately 4 × the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated through-holes, a cost savings can be realized.

Each TMS4256FML is described in its data sheet and is fully electrically tested and processed according to TI MIL-STD-883B flows (as amended for commercial applications) prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed.

TEXAS INSTRUMENTS
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The TM4256__8 features $\overline{RAS}$ access times of 100 ns, 120 ns, and 150 ns maximum.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4256__8 is rated for operation from 0°C to 70°C.

presence detect

This feature is included on the TM4256GU8 to allow for hardware presence detection of the memory module. The $\overline{PRD}$ pin for each module in the system should be pulled high through a pull-up resistor, resulting in a logic one when no module is present. When a module is present, $\overline{PRD}$ is a logic zero as this pin is connected to V_{SS} on the module. $\overline{PRD}$ can be used only to detect a module's presence, not its functionality. In a system not requiring presence detect, it is recommended that this pin be left as a no connect; this allows the use of either type of module without adverse effects.

operation

The TM4256FL8 and TM4256GU8 operate as eight TMS4256FMLs connected as shown in the functional block diagram. Refer to the TMS4256 data sheet for details of operation.

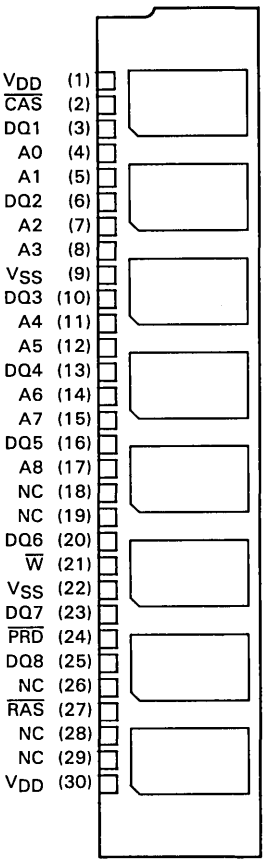
specifications

For TMS4256FML electrical specifications, refer to the TMS4256 data sheet.

single-in-line package and components

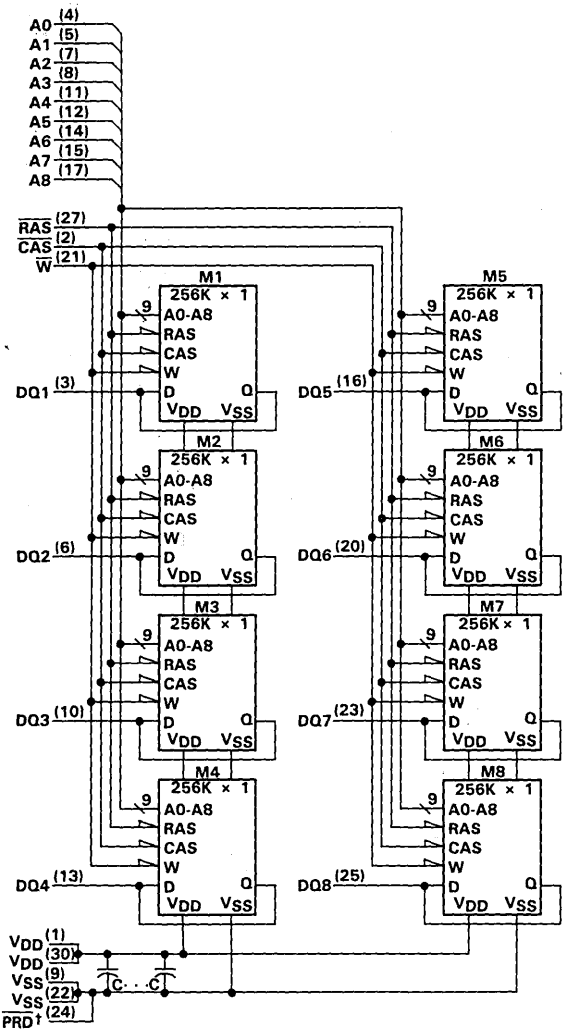
PC substrate: 1,27 mm (0.05 inch) nominal thickness epoxy-glass
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze
Contact area for socketable devices: Nickel plate and solder plate on top of copper

TM4256GU8 . . . U SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE TM4256GU8	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{PRD}$	Presence Detect (V_{SS})
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

functional block diagram



†Not available on the TM4256FL8.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 8 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4256__8-10		TM4256__8-12		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4	V_{DD}	2.4	V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0	0.4	0	0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V		±10		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high		±10		±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		560		520	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		36		36	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		464		424	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		400		360	mA

‡I_{DD1}-I_{DD4} are measured with M1-M8 in the same mode (i.e., operating, standby, refresh, page mode).

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4256__8-15 MIN	TM4256__8-15 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4	V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0	0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high		±10	μA
I_{DD1}†	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		480	mA
I_{DD2}†	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		36	mA
I_{DD3}†	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		384	mA
I_{DD4}†	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		320	mA

†I_{DD1}-I_{DD4} are measured with M1-M8 in the same mode (i.e., operating, standby, refresh, page mode).

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		40	pF
$C_{i(DQ)}$	Input capacitance, data inputs		12	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input		40	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		56	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input		40	pF
$C_{o(VDD)}$	Decoupling capacitance	0.8		μF

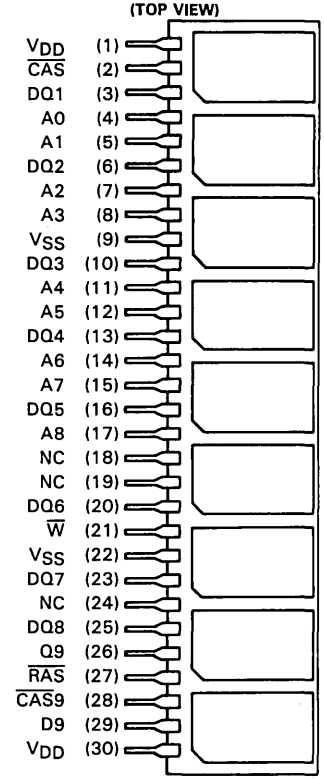
SEPTEMBER 1985—REVISED MARCH 1988

- 262,144 × 9 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-In-line Package (SIP)
  - —Pinned Module for Through-Hole Insertion (TM4256EL9)
  - —Leadless Module for Use with Sockets (TM4256GU9)
- Utilizes Nine 256K Dynamic RAMs in Plastic Chip Carriers
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS4256-10	100 ns	50 ns	200 ns
TMS4256-12	120 ns	60 ns	230 ns
TMS4256-15	150 ns	75 ns	260 ns

- Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines
- Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0°C to 70°C

TM4256EL9 . . . L SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE TM4256EL9	
A0-A8	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
D9	Data In
NC	No Connection
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4256_ _9 series are 2304K, dynamic random-access memory modules organized as 262,144 × 9 bits [bit nine (D9, Q9) is generally used for parity and is controlled by $\overline{CAS9}$] in a 30-pin single-in-line package comprising nine TMS4256FML, 262,144 × 1 bit dynamic RAMs in 18-lead plastic chip carriers mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM4256_ _9 has a density of ten devices per square inch (approximately 4 × the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer

plated through-holes, a cost savings can be realized.

Each TMS4256FML is described in its data sheet and is fully electrically tested and processed according to TI MIL-STD-883B flows (as amended for commercial applications) prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed.

The TM4256_ _9 features $\overline{RAS}$ access times of 100 ns, 120 ns, and 150 ns maximum.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4256_ _9 is rated for operation from 0°C to 70°C.

presence detect

This feature is included on the TM4256GU9 to allow for hardware presence detection of the memory module. The $\overline{PRD}$ pin for each module in the system should be pulled high through a pull-up resistor, resulting in a logic one when no module is present. When a module is present, $\overline{PRD}$ is a logic zero as this pin is connected to V_{SS} on the module. $\overline{PRD}$ can be used only to detect a module's presence, not its functionality. In a system not requiring presence detect, it is recommended that this pin be left as a no connect; this allows the use of either type of module without adverse effects.

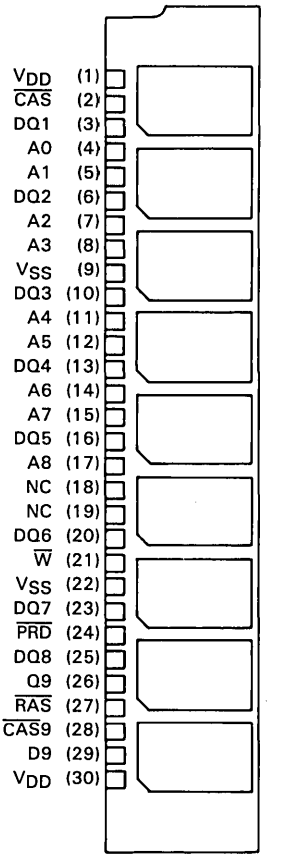
operation

The TM4256EL9 and TM4256GU9 operate as nine TMS4256FMLs connected as shown in the functional block diagram. Refer to the TMS4256 data sheet for details of operation.

specifications

For TMS4256FML electrical specifications, refer to the TMS4256 data sheet.

TM4256GU9 . . . U SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE TM4256GU9	
A0-A8	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobes
DQ1-DQ8	Data In/Data Out
D9	Data In
NC	No Connection
$\overline{PRD}$	Presence Detect (V_{SS})
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

TEXAS INSTRUMENTS
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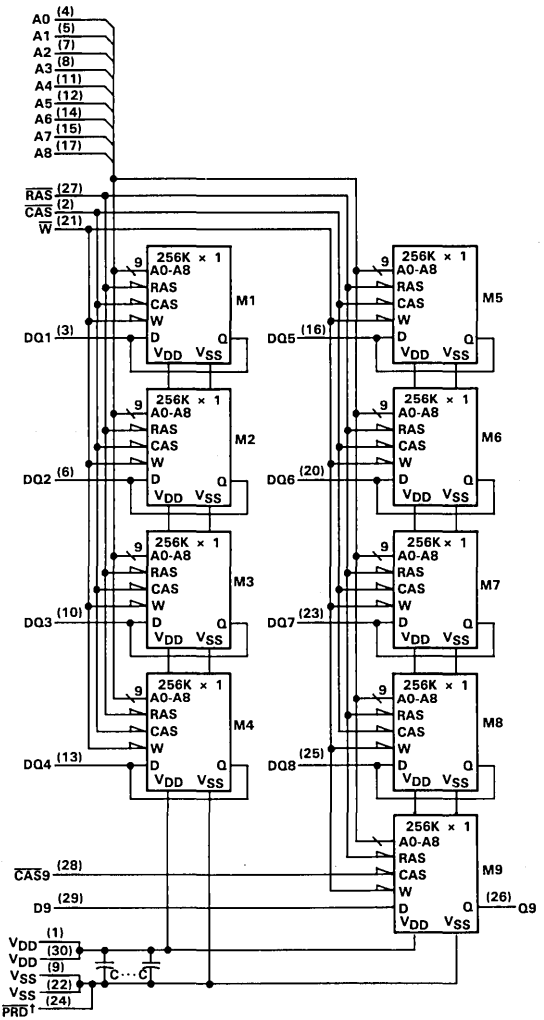
single-in-line package and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness epoxy-glass
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze
Contact area for socketable devices: Nickel plate barrier and solder finish on top of copper foil

functional block diagram



†Not available on the TM4256EL9.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 9 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4256_ _9-10		TM4256_ _9-12		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4	V_{DD}	2.4	V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0	0.4	0	0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V		±10		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high		±10		±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		630		585	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		41		41	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		522		477	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		450		405	mA

‡I_{DD1}-I_{DD4} are measured with M1-M9 in the same mode (i.e., operating, standby, refresh, page mode).

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4256_ _9-15 MIN	TM4256_ _9-15 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4	V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0	0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high		±10	μA
I_{DD1}†	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		540	mA
I_{DD2}†	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		41	mA
I_{DD3}†	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		432	mA
I_{DD4}†	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		360	mA

†I_{DD1}-I_{DD4} are measured with M1-M9 in the same mode (i.e., operating, standby, refresh, page mode).

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		45	pF
$C_{i(DQ)}$	Input capacitance, data inputs		12	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input		45	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		63	pF
$C_{i(CAS9)}$	Input capacitance, $\overline{CAS9}$ input		5	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input		40	pF
$C_{i(D9)}$	Input capacitance, D9 input		5	pF
$C_{o(Q9)}$	Output capacitance, Q9 input		7	pF
$C_{o(VDD)}$	Decoupling capacitance	0.8		μF

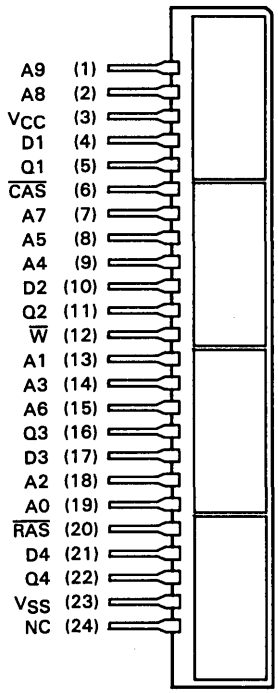
MAY 1987—REVISED MAY 1988

- 1,048,576 × 4 Organization
- Single 5-V Supply (10% Tolerance)
- 24-Pin Single-In-line Package (SIP)
- Utilizes Four 1 Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages
- Long Refresh Period . . . 8 ms (512 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS4C1024-10	100 ns	45 ns	190 ns
TMS4C1024-12	120 ns	55 ns	220 ns
TMS4C1024-15	150 ns	70 ns	260 ns

- Common $\overline{CAS}$ Control with Separate Data-In and Data-Out Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0°C to 70°C

AC SINGLE-IN-LINE PACKAGE
(TOP VIEW)



description

The TM024HAC4 is a 4,096K dynamic random-access memory module, organized as 1,048,576 × 4 bits in a 24-pin single-in-line package (SIP). The SIP is composed of four TMS4C1024DJ, 1,048,576 × 1 bit dynamic RAMs, each in a 26/20-lead plastic small outline J-lead package (SOJ), mounted on top of a substrate together with decoupling capacitors mounted beneath the SOJs. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated through-holes, a cost savings can be realized. Each TMS4C1024DJ is described in its data sheet and is fully electrically tested and processed according to TI MIL-STD-883B flows (as amended for commercial applications) prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed.

PIN NOMENCLATURE TM024HAC4	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D1-D4	Data Inputs
NC	No Connection
Q1-Q4	Data Outputs
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

The TM024HAC4 features $\overline{RAS}$ access times of 100 ns, 120 ns, and 150 ns maximum.

The refresh period is extended to 8 milliseconds, and during this period each of the 512 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

description (continued)

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM024HAC4 is rated for operation from 0°C to 70°C.

operation

The TM024HAC4 operates as four TMS4C1024s connected as shown in the functional block diagram on the following page. Refer to the TMS4C1024 data sheet for details of its operation.

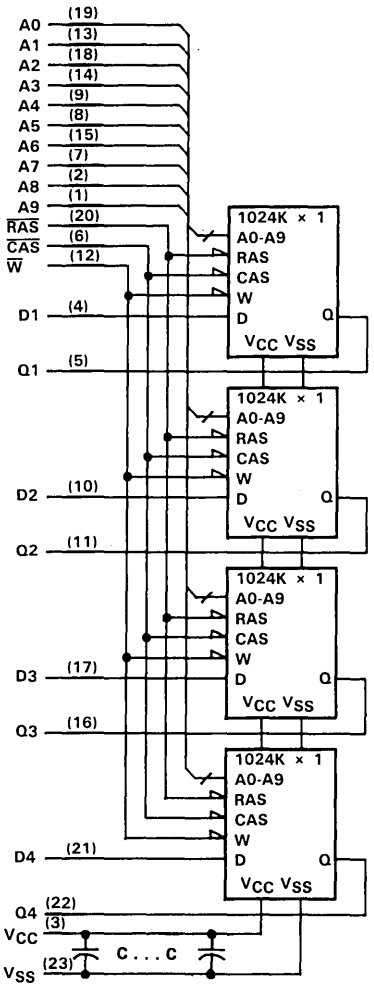
specifications

For TMS4C1024DJ electrical specifications, refer to the TMS4C1024 data sheet.

single-in-line package and components

PC substrate: 1,27 mm (0.05 in) nominal thickness; 0.005 in/in maximum warpage
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) . . . . . −1 V to 7 V
Voltage range on V_{CC} (see Note 1) . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 4 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM024HAC4-10		TM024HAC4-12		TM024HAC4-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	μA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		280		240		220	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		12		12		12	mA
I_{CC3}	Average refresh current	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		260		220		200	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		180		140		120	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		24	pF
$C_{i(D)}$	Input capacitance, data inputs		5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		28	pF
$C_{i(W)}$	Input capacitance, write-enable input		28	pF
C_o	Output capacitance		7	pF

NOTE 3: V_{CC} equal to 5.0 V ± 0.5 V and the bias on pins under test is 0.0 V.

JULY 1987—REVISED MAY 1988

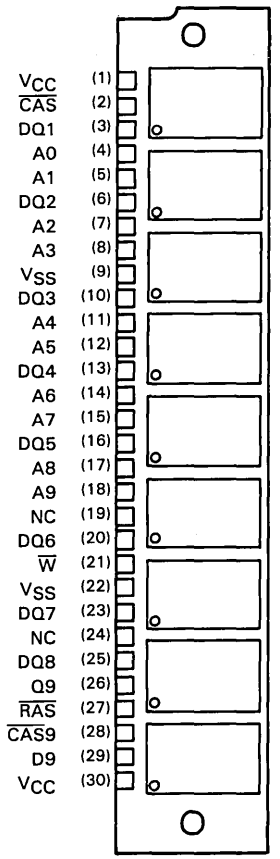
- TM024EAD9 . . . 1,048,576 × 9 Organization
- TM024GAD8 . . . 1,048,576 × 8 Organization
- Single 5-V Supply (10% Tolerance)
- 30-pin Single-In-line Package (SIP)
  — Leadless Module for Use with Sockets
- TM024EAD9 . . . Utilizes Nine 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages
- TM024GAD8 . . . Utilizes Eight 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages
- Long Refresh Period . . . 8 ms (512 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Output
- Performance of Unmounted RAMs:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS4C1024-10	100 ns	45 ns	190 ns
TMS4C1024-12	120 ns	55 ns	220 ns
TMS4C1024-15	150 ns	70 ns	260 ns

- Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines
- Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines†
- Low Power Dissipation
- Operating Free Air Temperature . . . 0°C to 70°C
- TM024EAD9 . . . Downward Compatible with TI TM4256GU9 (256K × 9)
- TM024GAD8 . . . Downward Compatible with TM4256GU8 (256K × 8) SIP

†Available only on the TM024EAD9

TM024EAD9 . . . AD SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE TM024EAD9	
A0-A9	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
D9	Data In
NC	No Connection
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

description

TM024EAD9

The TM024EAD9 is a 9216K (dynamic) random-access memory module organized as 1,048,576 × 9 bits [bit nine (D9, Q9) is generally used for parity and is controlled by $\overline{CAS}$9] in a 30-pin single-in-line package (SIP). The SIP is composed of nine TMS4C1024DJ, 1,048,576 × 1-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs) mounted on top of a substrate together with decoupling capacitors mounted beneath the SOJs. Each TMS4C1024DJ is described in the TMS4C1024 data sheet and is fully electrically tested and processed according to TI MIL-STD-883B (as amended for commercial applications) flows prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed.

The TM024EAD9 SIP is available in the AD single-sided, leadless module for use with sockets.

The TM024EAD9 SIP is rated for operation from 0°C to 70°C.

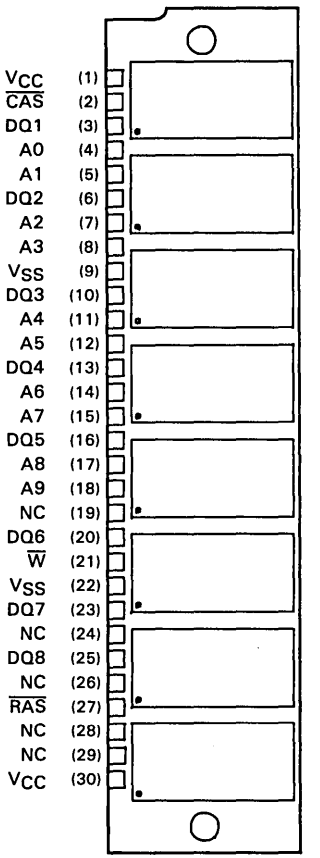
TM024GAD8

The TM024GAD8 is a 8,192K (dynamic) random-access memory module organized as 1,048,576 × 8 in a 30-pin single-in-line package (SIP). The SIP is composed of eight TMS4C1024DJ, 1,048,576 × 1 bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead package (SOJ), mounted on top of a substrate together with decoupling capacitors mounted beneath the SOJs. Each TMS4C1024DJ is described in its data sheet and is fully electrically tested and processed according to TI MIL-STD-883B flows (as amended for commercial applications) prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed.

The TM024GAD8 SIP is available in the AD single-sided, leadless module for use with sockets.

The TM024GAD8 SIP is rated for operation from 0°C to 70°C.

TM024GAD8 . . . AD SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE TM024GAD8	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

operation

TM024EAD9

The TM024EAD9 operates as nine TMS4C1024DJs connected as shown in the functional block diagram. Refer to the TMS4C1024 data sheet for details of its operation. The common I/O feature of the TM024EAD9 dictates the use of early write cycles to prevent contention on D and Q.

TM024GAD8

The TM024GAD8 operates as eight TMS4C1024DJs connected as shown in the functional block diagram. Refer to the TMS4C1024 data sheet for details of its operation. The common I/O feature of the TM024GAD8 dictates the use of early write cycles to prevent contention on D and Q.

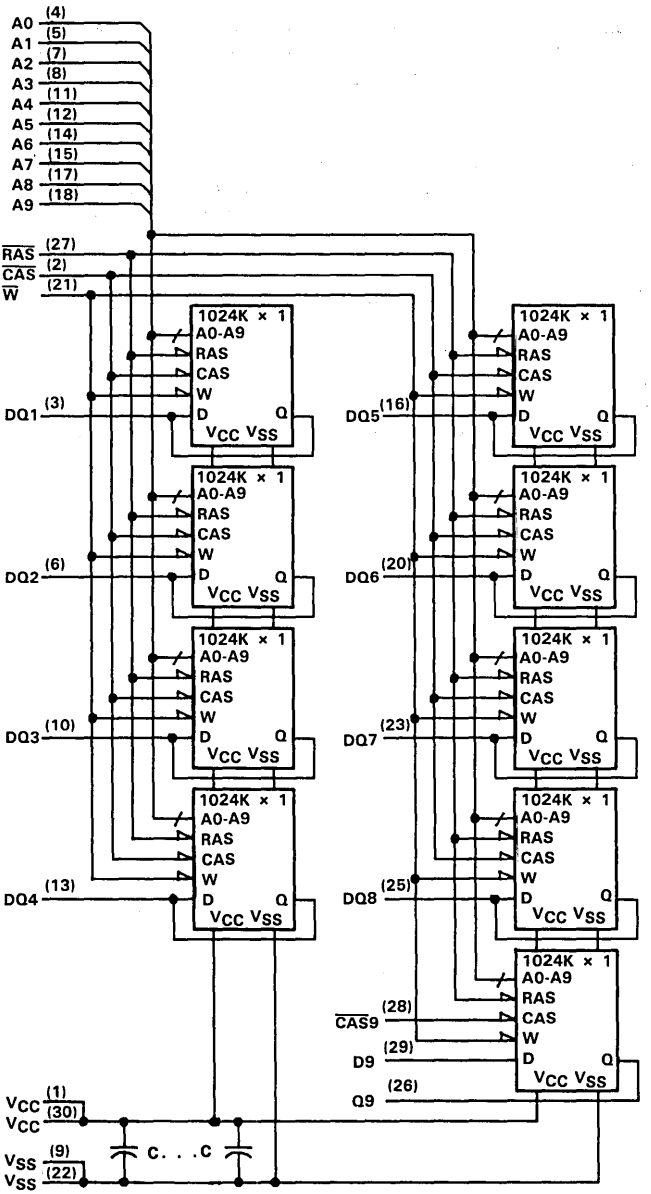
specifications

For TMS4C1024DJ electrical specifications, refer to the TMS4C1024 data sheet.

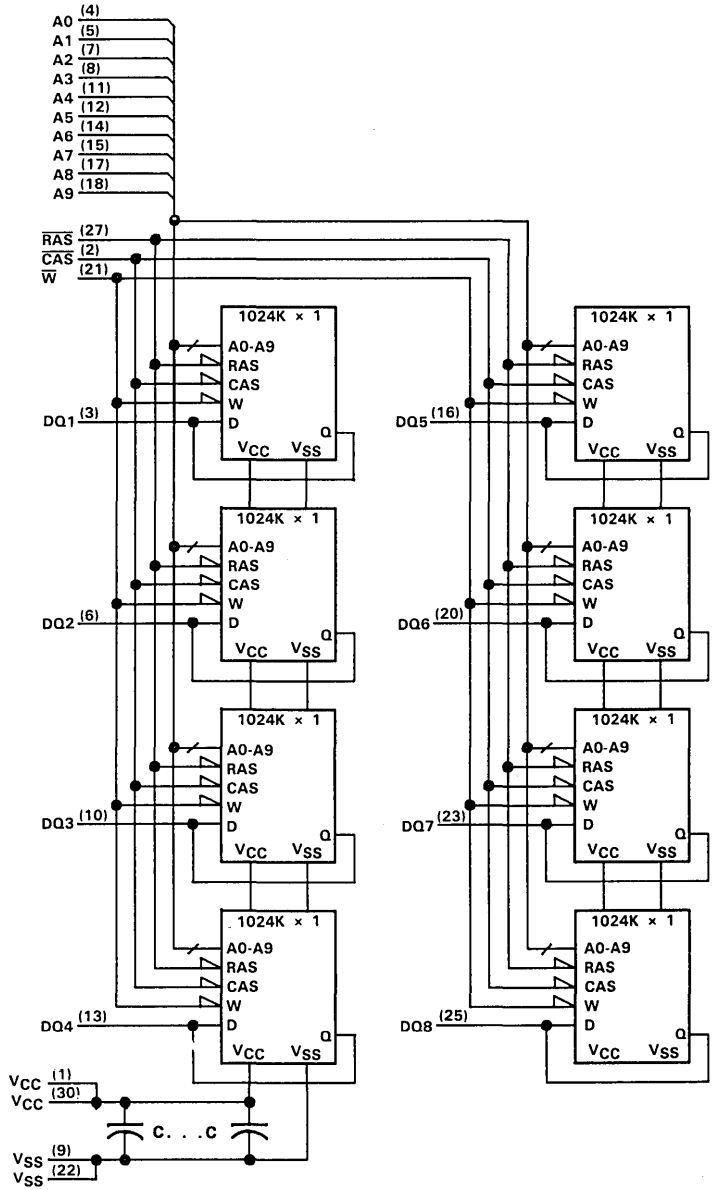
single-in-line package and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate on top of copper

functional block diagram (TM024EAD9)



functional block diagram (TM024GAD8)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) . . . . . −1 V to 7 V
Voltage range on V_{CC} (see Note 1) . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation TM024GAD8 . . . . . 8 W
TM024EAD9 . . . . . 9 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM024EAD9-10		TM024EAD9-12		TM024EAD9-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	μA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		630		540		495	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		27		27		27	mA
I_{CC3}	Average refresh current	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		585		495		450	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		405		315		270	mA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM024GAD8-10		TM024GAD8-12		TM024GAD8-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	μA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		560		480		440	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		24		24		24	mA
I_{CC3}	Average refresh current	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		520		440		400	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		360		280		240	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TM024GAD8		TM024EAD9		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		48		54	pF
$C_{i(D)}$	Input capacitance, data input		12		12	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		56		63	pF
$C_{i(W)}$	Input capacitance, write-enable input		12		12	pF
C_o	Output capacitance		56		63	pF

NOTE 3: V_{CC} equal to 5.0 V ± 0.5 V and the bias on pins under test is 0.0 V.

MEMORY INTENSIVE MODULES

Surface Mount Technology (SMT) increases the density of board assemblies through use of much smaller components than traditional technology. Texas Instruments is offering the benefits of SMT through memory modules to increase memory density in customers' systems. For several years, TI has been producing catalog and custom single in-line packages (SIPs) and now is applying this standard technology to produce denser custom memory modules referred to as "Memory Intensive Modules" or "MIMs".

TI is a world leader in DRAM technology, including silicon design and processing, and in packaging techniques. By combining these, you can get the most cost-effective memory system solution in functionality, density, quality, and reliability. MIMs also can include other logic functions, such as drivers, decoders, or passive components, in addition to memory ICs.

SMT provides many benefits, but the most compelling is increased board density. The memory system portion of a computer or work station can be reduced by a factor of 2.5 × to 3.5 × by using SIPs or MIMs. At the same time, some improvements in electrical performance of the system can be executed due to shorter electrical signal paths. Because the assemblies are smaller, multilayer boards can be used without significantly increasing board cost.

Table 1 shows a comparison of through-hole vs. surface mount components at the 1 Meg density level. Because the larger silicon chip size requires a larger package body, there is little difference among the three common package types: DIP, ZIP, and SOJ. However, when the SOJ is used on a double-sided board, which is possible only with SMT, there is a two- to three-fold reduction in board area. The SOJ, used either single-sided or double-sided, is best when the criterion is minimum system volume.

Table 1. Component Density Comparison

1 MEG DRAM COMPONENTS

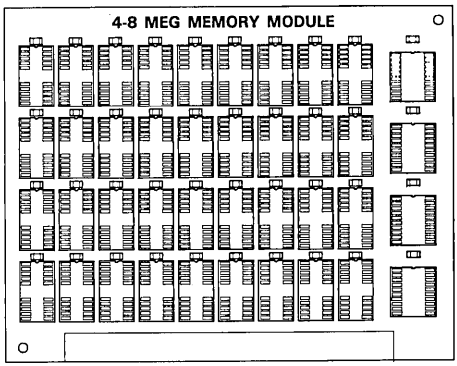
COMPONENT	X - Y COMP. PITCH (in.)	# COMP./SQ.IN.	BOARD THICKNESS W/COMP. (in.)
DIP	.4 × 1	2.5	.245
ZIP	.2 × 1.1	4.5	.412
SOJ: SS†	.4 × .7	3.6	.202
SOJ: DS†	.4 × .7	7	.342

– DS SMT OFFERS THE HIGHEST COMPONENT DENSITY
– SM BOARDS ALLOW BETTER SPACING AND COOLING IN SYSTEMS (BASED ON .5 IN. CENTERS BETWEEN BOARDS)
† SS - SINGLE SIDED, DS - DOUBLE SIDED

MIMs offer the following benefits to the customer:

1. Higher level of integration
2. Custom form factors built with standard techniques
3. Fully tested and ready for use
4. Decreased system design and development time
5. Benefits of SMT without the start-up expense
6. Easy upgrade path to the next density level
7. Reduced inventory variety if same MIM used in several systems

MIMs extend the inherent benefits of SIPs and SMT to a higher level of integration and are ideal for system manufacturers with large memory requirements. A sample MIM is shown in Figure 1. This MIM provides 4 megabytes with a single-sided assembly or 8 megabytes with a double-sided assembly. Using proven design and production techniques, a custom product can be built with a standard, high-volume, cost-effective manufacturing process. TI will turn-key the design, layout, manufacturing, and testing of the module.



DRAM	TMS4C1024DJ
CAPACITOR	0.10-0.22 μF (1206 Style)
COMPONENT PITCH	X = 0.425, Y = 0.800
AREA (sq. in.)	18.80

Figure 1. Memory Intensive Modules

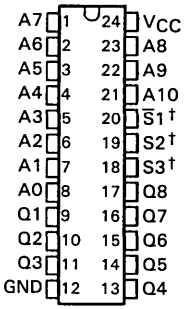
SEPTEMBER 1986—REVISED APRIL 1988

- Organization . . . 2K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 2K × 8 Bipolar/High-Speed CMOS EPROMs and PROMs
- All Inputs/Outputs TTL Compatible
- High Speed
- Max Access/Min Cycle Time

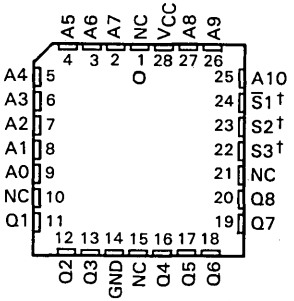
V_{CC} ± 5%		
'27C/PC291-3	'27C292-3	35 ns
'27C/PC291	'27C292	45 ns
'27C/PC291-5	'27C292-5	50 ns
V_{CC} ± 10%		
'27C/PC291-35	'27C292-35	35 ns
'27C/PC291-45	'27C292-45	45 ns
'27C/PC291-50	'27C292-50	50 ns

- Low-Power CMOS Technology
- 3-State Output Buffers
- Low Power Dissipation (V_{CC} = 5.25 V) — Active . . . 394 mW Max
- Erasable
- 100% Pretestable

J AND N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



†These pins have different pin assignments and functions in the program mode (see page 3).

description

The TMS27C291 and TMS27C292 series are 16,384-bit, ultraviolet-light erasable, electrically programmable read-only memories. The TMS27PC291 series are 16,384-bit, one-time, electrically programmable read-only memories. These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external resistors. Each output can drive eight Series 74 TTL circuits without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The J and N dual-in-line packages are pin compatible with existing 24-pin bipolar PROMs and high speed EPROMs.

READ MODE

PIN NOMENCLATURE	
A0-A10	Address Inputs
GND	Ground
NC	No Connection
Q1-Q8	Outputs
$\overline{S}1$, S2, S3	Chip Selects
V_{CC}	5-V Power Supply

The TMS27C291 and TMS27C292 are offered in dual-in-line ceramic packages (J suffix). The TMS27C291 ceramic package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers. The TMS27C292 ceramic package is designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers.

The TMS27PC291 PROM is offered in dual-in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers. This version of the device is still in development, and the ADVANCE INFORMATION notices in this data sheet pertain to the N package devices. The TMS27PC291 PROM is also offered in a 28-lead plastic-leaded chip carrier (FN suffix) for surface mounting applications on solder lands on 1,27-mm (50-mil) centers.

All devices are guaranteed for operation from 0°C to 70°C.

operation

There are eight modes of operation for the TMS27C291, TMS27C292 and the TMS27PC291 as listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL or CMOS levels except for V_{PP} during programming (13.5 V).

FUNCTION	MODE										
	Read	Output Disable#	Output Disable#	Output Disable#	Program Verify	Program Inhibit	Fast Program	Blank Check Ones	Blank Check Zeros	Signature	
$\overline{S1}/V_{PP}$†	V_{IL}	V_{IH}	X‡	X	V_{PP}	V_{PP}	V_{PP}	$V_{IL(P)}$¶	$V_{IL(P)}$	V_{IL}	
S2/$\overline{VFY}$†	V_{IH}	X	V_{IL}	X	$V_{IL(P)}$	$V_{IH(P)}$	$V_{IH(P)}$	$V_{IL(P)}$	$V_{IH(P)}$	V_{IH}	
S3/$\overline{PGM}$†	V_{IH}	X	X	V_{IL}	$V_{IH(P)}$	$V_{IH(P)}$	$V_{IL(P)}$	V_H§	V_H	V_H	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	X	X	X	V_{PP}	V_{PP}
A0	X	X	X	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8	D_{OUT}	HI-Z	HI-Z	HI-Z	D_{OUT}	HI-Z	D_{IN}	Ones	Zeros	CODE	
										MFG	DEV
										97	02

†Pin assignment for program mode.
‡X can be V_{IL} or V_{IH}.
§V_H = 12 V ± 0.5 V.
¶(P) = Programming mode.
#Output can be disabled using any of these three methods.

read/output disable

When the outputs of two or more of these devices are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a '27C291, '27PC291, or '27C292, a low-level signal is applied to $\overline{S1}$ and a high-level signal is applied to S2 and S3. Any other combination of logic states on these three inputs will disable the outputs. Output data is accessed at pins Q1 through Q8.

latchup immunity

Latchup immunity is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

erasure (TMS27C291-_ _JL and TMS27C292-_ _JL)

Before programming, the '27C291 or '27C292 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is 25 watt-seconds per square centimeter. A typical 12 milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 45 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the '27C291 or '27C292, the window should be covered with an opaque label.

programming mode pin functions

In the programming mode pins 18-20 on the dual-in-line packages or pins 22-24 on the plastic-leaded chip carrier no longer act as chip selects. Pin $\overline{S1}$ becomes the V_{PP} power supply, pin S2 becomes the $\overline{VFY}$ (verify) input, and pin S3 becomes the $\overline{PGM}$ (program) input in the programming mode. Programming mode pin assignments and nomenclature are given in the figures to the right.

blank check mode

The '27C291 and '27C292 use a differential memory cell. This means that an unprogrammed device has ambiguous states in all address locations. Prior to programming, the blank check mode is used to verify that both sides of the differential cell are erased. The blank check mode is defined as S3 to V_H and $\overline{S1}$ to V_{IL}. In this mode, S2 selects between blank check 0s and 1s.

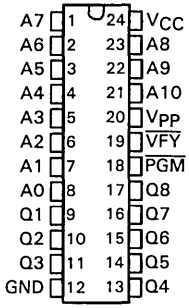
fast programming

Data is presented in parallel (eight bits) on pins Q1 through Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed. The programming mode is achieved when V_{PP} = 13.5 V, V_{CC} = 5.0 V, $\overline{VFY}$ = V_{IH}, $\overline{PGM}$ = pulsed V_{IL}. More than one '27C291, '27C292, or '27PC291 can be programmed when the devices are connected in parallel. Locations can be programmed in any order, but it is recommended that all locations be programmed.

PROGRAMMING AND BLANK CHECK MODE PIN ASSIGNMENTS

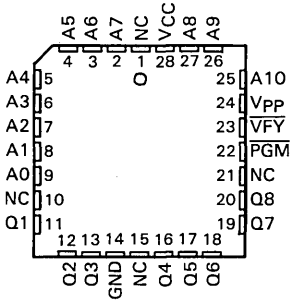
J AND N PACKAGES

(TOP VIEW)



FN PACKAGE

(TOP VIEW)



PROGRAM MODE

PIN NOMENCLATURE	
A0-A10	Address Inputs
GND	Ground
NC	No Connection
$\overline{PGM}$	Program Input
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
$\overline{VFY}$	Verify Input
V_{PP}	13.5-V Power Supply

Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 0.1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied. If correct data is not read, an additional 0.1-millisecond pulse is applied up to a maximum X of 4. The Final programming pulse is 24X long. This sequence of programming and verification is performed at V_{CC} = 5.0 V and V_{PP} = 13.5 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = 5 V ± 10% (see Figure 1).

program inhibit

Programming may be inhibited by maintaining a high-level input on the $\overline{PGM}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 13.5 V when $\overline{VFY}$ = V_{IL} and $\overline{PGM}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0, i.e., A0 = V_{IL} accesses the manufacturer code; A0 = V_{IH} accesses device code. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for these devices is 97, and the device code is 02.

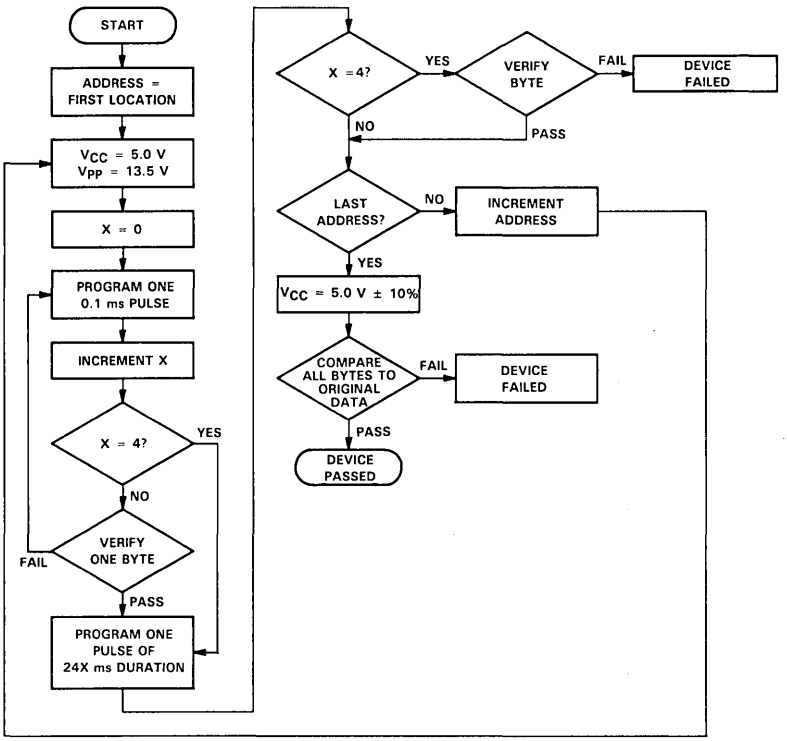
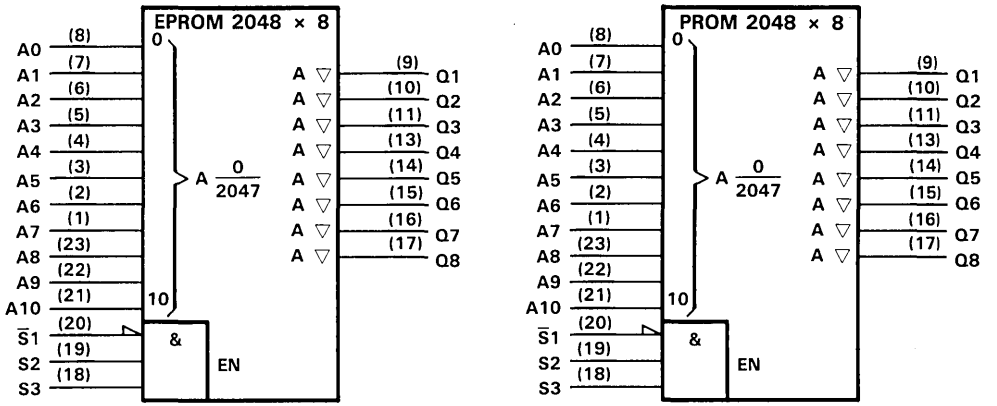


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} (programming mode) . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 and S3 . . . . . −0.6 V to 6.5 V
A9 and S3 . . . . . −0.6 V to 14 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			'27C291, '27PC291 '27C292 '27C291-3, '27PC291-3 '27C292-3 '27C291-5, '27PC291-5 '27C292-5			'27C291-35, '27PC291-35 '27C292-35 '27C291-45, '27PC291-45 '27C292-45 '27C291-50, '27PC291-50 '27C292-50			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.5	5	5.5	V
V_{IH}	High-level input voltage (see Note 2)	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	
$V_{IH(P)}$	High-level input voltage (see Note 2)	Programming	3		$V_{CC}+1$	3		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		GND+0.2	−0.5		GND+0.2	
$V_{IL(P)}$	Low-level input voltage (see Note 2)	Programming	−0.5		0.4	−0.5		0.4	V
T_A	Operating free-air temperature		0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only. These are absolute voltages with respect to device ground pin and include all overshoot due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −4 mA		2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 16 mA				0.4	V
I_I	Input current (leakage)	All inputs except $\overline{S1}$	V_I = 0 V to 5.5 V			1	±10	μA
		$\overline{S1}$	$\overline{S1}$ = 0 V to 5.5 V				±10	
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			1	±10	μA
I_{PP}	V_{PP} programming current		V_{PP} = 13.5 V				50	mA
I_{CC}	Supply current (see Note 3)	'27C291-3, '27PC291-3	V_{CC} = 5.25 V	t_c = dc		15	35	mA
		'27C292-3		t_c = min		40	75	
		'27C291-35, '27PC291-35	V_{CC} = 5.5 V	t_c = dc		15	35	mA
		'27C292-35		t_c = min		40	75	
		'27C291, '27PC291	V_{CC} = 5.25 V	t_c = dc		15	35	mA
		'27C292		t_c = min		35	60	
		'27C291-45, '27PC291-45	V_{CC} = 5.5 V	t_c = dc		15	35	mA
		'27C292-45		t_c = min		35	60	
		'27C291-5, '27PC291-5	V_{CC} = 5.25 V	t_c = dc		15	35	mA
		'27C292-5		t_c = min		30	55	
		'27C291-50, '27PC291-50	V_{CC} = 5.5 V	t_c = dc		15	35	mA
		'27C292-50		t_c = min		30	55	

†Typical I_{CC} is measured at V_{CC} = 5 V, T_A = 25°C and CMOS input levels.
NOTE 3: Assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, and addresses toggling between 0 V and 3 V.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	All inputs except $\overline{S1}$	V_I = 0 V, f = 1 MHz		8	10	pF
		$\overline{S1}$	V_I = 0 V, f = 1 MHz		16	20	pF
C_o	Output capacitance		V_O = 0 V, f = 1 MHz		12	15	pF

†Capacitance measurements are made on a sample basis only.
‡Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4 and Figure 2)

PARAMETER		'27C291-3, '27PC291-3 '27C292-3 '27C291-35, '27PC291-35 '27C292-35		'27C291, '27PC291 '27C292 '27C291-45, '27PC291-45 '27C292-45		'27C291-5, '27PC291-5 '27C292-5 '27C291-50, '27PC291-50 '27C292-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		35		45		50	ns
$t_{en(S1)}$	Enable time from $\overline{S1}$		25		35		35	ns
$t_{en(S2)}$	Enable time from S2		25		35		35	ns
$t_{en(S3)}$	Enable time from S3		25		35		35	ns
t_{dis}	Disable time from $\overline{S1}$, S2, S3	0	25	0	35	0	35	ns
$t_{v(A)}$	Output valid time	0		0		0		ns

NOTES: 3. Assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, and addresses toggling between 0 V to 3 V.
4. Minimum cycle time is equal to maximum access time.

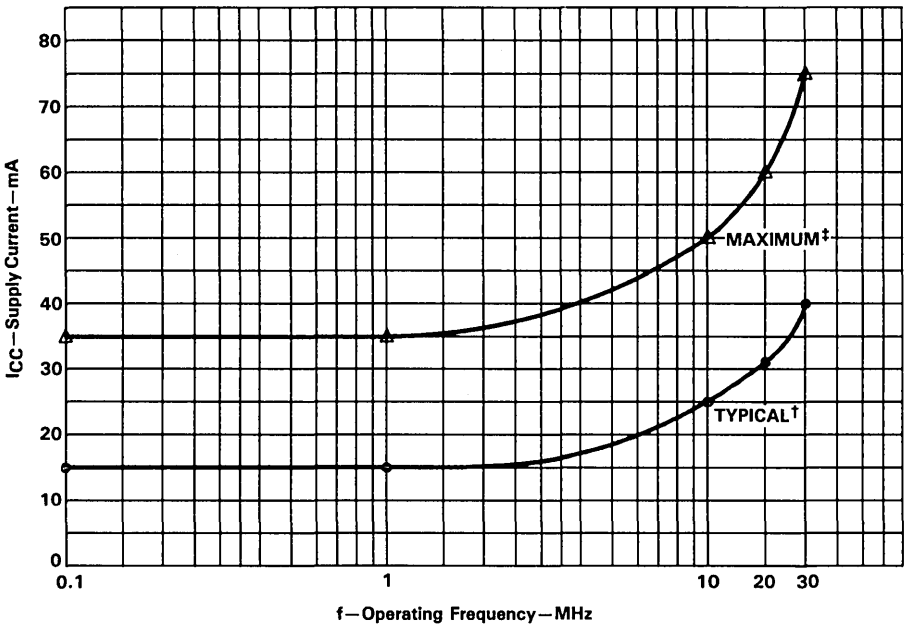
recommended timing requirements for programming

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.1		0.4	ms
$t_{w(FPGM)}$	Final program pulse duration	2.4		9.6	ms
$t_{su(A)}$	Address setup time	1			μs
$t_{su(VPP)}$	V_{PP} setup time	1			μs
$t_{su(VFY)}$	$\overline{VFY}$ setup time	1			μs
$t_{dis(VFY)}$	Output disable time from $\overline{VFY}$	0		35	ns
$t_{en(VFY)}$	Output enable time from $\overline{VFY}$			35	ns
$t_{su(D)}$	Data setup time	1			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	1			μs

supply current vs operating frequency

PARAMETER		TEST CONDITIONS	TYP†	MAX‡	UNIT
I_{CC}	Supply current	0 Hz ≤ f ≤ 1 MHz	15	35	mA
		f = 10 MHz	25	50	mA
		f = 20 MHz	32	60	mA
		f = 30 MHz	40	75	mA

SUPPLY CURRENT
vs
OPERATING FREQUENCY



†Typical I_{CC} is measured at V_{CC} = 5 V, T_A = 25°C and CMOS inputs levels.
‡Maximum I_{CC} is measured at V_{CC} = 5.5 V, T_A = 0°C and CMOS input levels.

PARAMETER MEASUREMENT INFORMATION

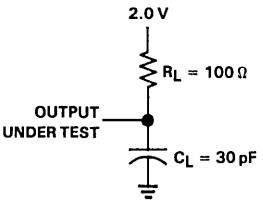
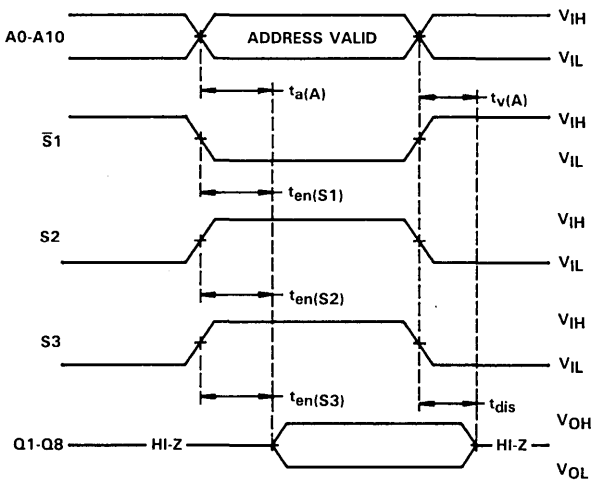
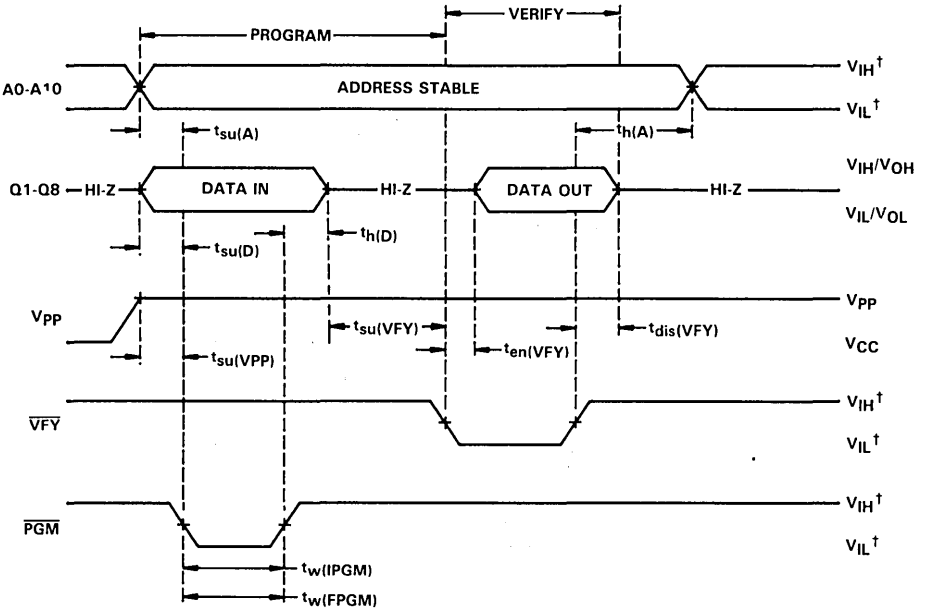


FIGURE 2. OUTPUT LOAD CIRCUIT

read cycle timing



program cycle timing

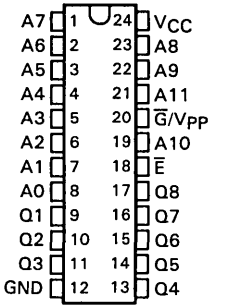


†Programming levels for V_{IH} and V_{IL}.

AUGUST 1983—REVISED FEBRUARY 1988

- **Organization . . . 4096 × 8**
- **Single 5-V Power Supply**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**
  TMS2732A-17 170 ns
  TMS2732A-20 200 ns
  TMS2732A-25 250 ns
  TMS2732A-45 450 ns
- **Low Standby Power Dissipation . . . 158 mW (Maximum)**
- **JEDEC Approved Pinout . . . Industry Standard**
- **21-V Power Supply Required for Programming**
- **N-Channel Silicon-Gate Technology**
- **PEP4 Version Available with 168 Hour Burn-In, and Extended Guaranteed Operating Temperature Range from −10°C to 85°C (TMS2732A-_ _JP4)**

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A11	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}/V_{PP}$	Output Enable/21 V
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply

description

The TMS2732A is an ultraviolet light-erasable, electrically programmable read-only memory. It has 32,768 bits organized as 4,096 words of 8-bit length. The TMS2732A only requires a single 5-volt power supply with a tolerance of ±5%.

The TMS2732A provides two output control lines: Output Enable ($\overline{G}$/Vpp) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$/Vpp control line to eliminate bus contention in multibus microprocessor systems. The TMS2732A has a power-down mode that reduces maximum power dissipation from 657 mW to 158 mW when the device is placed on standby.

This EPROM is supplied in a 24-pin dual-in-line ceramic package and is designed for operation from 0°C to 70°C. The TMS2732A is also offered in the PEP4 version with an extended guaranteed operating temperature range of −10°C to 85°C and 168 hour burn-in (TMS2732A-_ _JP4).

operation

The six modes of operation for the TMS2732A are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down (Standby)	Program	Program Verification	Inhibit Programming
$\overline{E}$ (18)	V_{IL}	X†	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}/V_{PP}$ (20)	V_{IL}	V_{IH}	X†	21 V	V_{IL}	21 V
V_{CC} (24)	5 V	5 V	5 V	5 V	5 V	5 V
Q1-Q8 (9 to 11, 13 to 17)	Q	HI-Z	HI-Z	D	Q	HI-Z

†X = V_{IH} or V_{IL}

read/output disable

The two control pins ($\overline{E}$ and $\overline{G}/V_{PP}$) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}/V_{PP}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum power dissipation from 657 mW to 158 mW. A TTL high-level signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}/V_{PP}$.

erasure

The TMS2732A is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS2732A, the window should be covered with an opaque label.

programming

Note that the application of a voltage in excess of 22 V to $\overline{G}/V_{PP}$ may damage the TMS2732A.

After erasure (all bits in logic 1 state), logic 0s are programmed into the desired locations. A logic 0 can only be erased by ultraviolet light. In the program mode, $\overline{G}/V_{PP}$ is taken from a TTL low level to 21 V and data to be programmed are applied in parallel to output pins Q1-Q8. The location to be programmed is addressed. Once data and addresses are stable, a 10-millisecond TTL low-level pulse is applied to $\overline{E}$. The maximum width of this pulse is 11 milliseconds. The programming pulse must be applied at each location that is to be programmed. Locations may be programmed in any order.

Several TMS2732As can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

program inhibit

The program inhibit is useful when programming multiple TMS2732As connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ of the device that is not to be programmed

program verify

After the EPROM has been programmed, the programmed bits should be verified. To verify bit states, $\overline{G}/V_{PP}$ and $\overline{E}$ are set to V_{IL}.

TEXAS INSTRUMENTS
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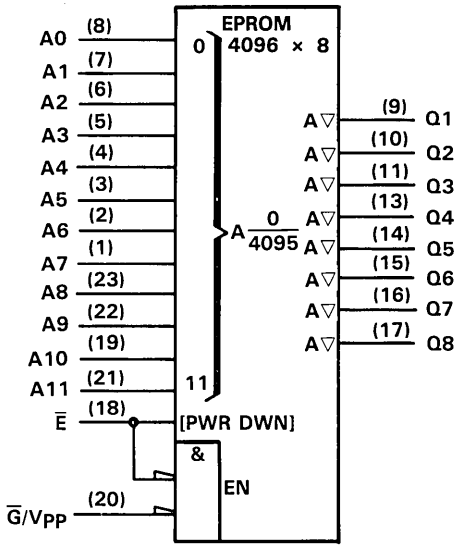
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . −0.3 V to 7 V
Supply voltage range, V_{PP} . . . . . −0.3 V to 22 V
Input voltage range (except program) . . . . . −0.3 to 7 V
Output voltage range . . . . . −0.3 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	PARAMETER	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)	4.75	5	5.25	V
V_{PP}	Supply voltage (see Note 2)		V_{CC}		V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−0.1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
2. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 21 V (±0.5 V).

electrical characteristics over full ranges of recommended operating conditions

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA		0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V		±10	μA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}, $\overline{G}/V_{PP}$ at V_{IL}		30	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}/V_{PP}$ at V_{IL}		125	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER			TEST CONDITIONS	TYP‡	MAX	UNIT
C_i	Input capacitance	All except $\overline{G}/V_{PP}$	V_I = 0 V	6	9	pF
		$\overline{G}/V_{PP}$			20	
C_o	Output capacitance		V_O = 0 V	8	12	pF

†These parameters are tested on sample basis only.
‡Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	TMS2732A-17		TMS2732A-20		TMS2732A-25		TMS2732A-45		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, $t_r \le 20$ ns, $t_f \le 20$ ns, See Figure 1 and Note 3		170		200		250		450	ns
$t_{a(E)}$	Access time from $\overline{E}$			170		200		250		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}/V_{PP}$			65		70		100		150	ns
t_{dis}†	Output disable time from $\overline{E}$ or G, whichever occurs first		0	60	0	60	0	85	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}/V_{PP}$, whichever occurs first		0		0		0		0		ns

NOTE 3: For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output reference levels are 0.8 V and 2.0 V.
†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled, not 100% tested.

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recommended conditions for programming, T_A = 25°C (see Note 4)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage	20.5	21	21.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−0.1		0.8	V
$t_{w(E)}$	$\overline{E}$ pulse duration	9	10	11	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	$\overline{G}/V_{PP}$ setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(VPP)}$	$\overline{G}/V_{PP}$ hold time	2			μs
$t_{rec(PG)}$	$\overline{G}/V_{PP}$ recovery time	2			μs
$t_{r(PG)G}$	$\overline{G}/V_{PP}$ rise time during programming	50			ns
t_{EHD}	Delay time, data valid after $\overline{E}$ low			1	μs

NOTE 4: When programming the TMS2732A, connect a 0.1 μF capacitor between $\overline{G}/V_{PP}$ and GND to suppress spurious voltage transients which may damage the device.

programming characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage		−0.1		0.8	V
V_{OH}	High-level output voltage (verify)	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage (verify)	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (all inputs)	$V_I = V_{IL}$ or V_{IH}			10	μA
I_{PP}	Supply current	$\overline{E} = V_{IL}$, $\overline{G} = V_{PP}$			50	mA
I_{CC}	Supply current				125	mA
$t_{dis(PR)}$	Output disable time		0		130	ns

PARAMETER MEASUREMENT INFORMATION

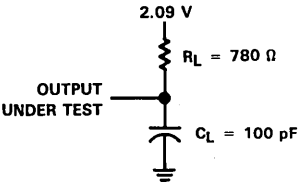
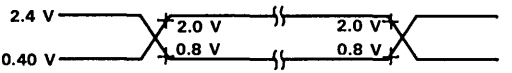


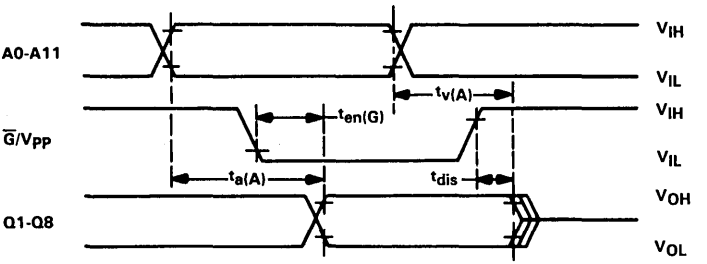
FIGURE 1. TYPICAL OUTPUT LOAD CIRCUIT

AC testing input/output wave forms

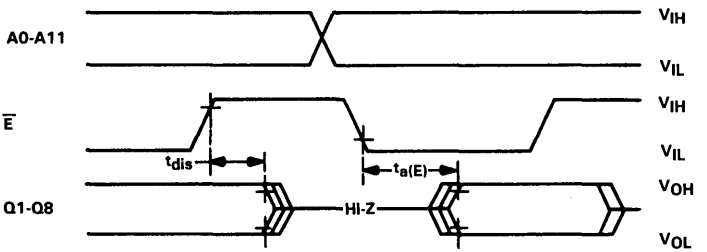


A.C. testing inputs are driven at 2.4 V for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 for both inputs and outputs.

read cycle timing

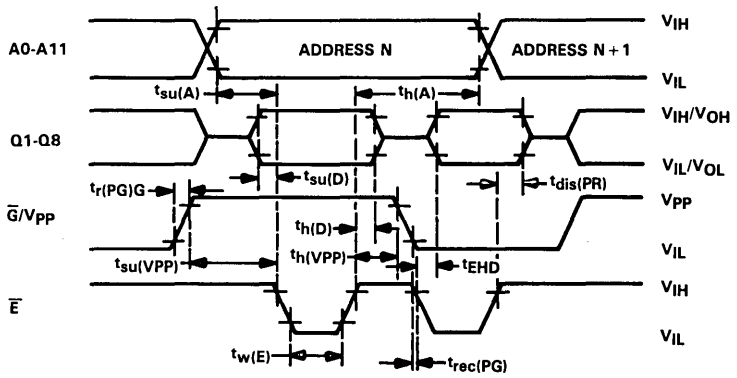


standby mode



NOTE 3: For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2.0 V.

program cycle timing



NOTE 3: For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2.0 V.

TMS27C32 32,768-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC32 32,768-BIT PROGRAMMABLE READ-ONLY MEMORY

MAY 1988

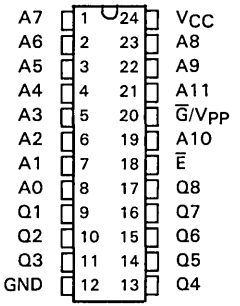
This Data Sheet is Applicable to All TMS27C32s and TMS27PC32s Symbolized with Code "A" as Described on Page 12.

- **Organization . . . 4K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible with Existing 32K MOS ROMs, PROMs, and EPROMs**
- **JEDEC Standard Pinout**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**

V_{CC} ±5%	V_{CC} ±10%	
'27C32-100	'27C32-10	100 ns
'27C/PC32-120	'27C/PC32-12	120 ns
'27C/PC32-150	'27C/PC32-15	150 ns
'27C/PC32-2	'27C/PC32-20	200 ns
'27C/PC32	'27C/PC32-25	250 ns

- **Power Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming or Fast Programming Algorithms**
- **3-State Output Buffers**
- **400 mV Guaranteed DC Noise Immunity with Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**

J & N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A11	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}/V_{PP}$	Output Enable/12-13 V Programming Power Supply
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply

- **Low Power Dissipation (V_{CC} = 5.25 V)**
  - **Active . . . 132 mW Worst Case**
  - **Standby . . . 1.4 mW Worst Case (CMOS Input Levels)**
- **PEP4 Version Available with 168 Hour Burn-In, and also Extended Guaranteed Operating Temperature Ranges**

description

The TMS27C32 series are 32,768-bit ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC32 series are 32,768-bit, one-time, electrically programmable read-only memories.

These devices are fabricated using power saving CMOS technology for high-speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C32 and the TMS27PC32 are pin compatible with 24-pin 32K MOS ROMs, PROMs, and EPROMs.

The TMS27C32 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C32 is available with two guaranteed temperature ranges of 0°C to 70°C and −40°C to 85°C (TMS27C32-_ _JL and TMS27C32-_ _JE, respectively). The TMS27C32 is also offered with 168 hour burn-in on both temperature ranges (TMS27C32-_ _JL4 and TMS27C32-_ _JE4, respectively). (See table on page 2).

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The TMS27PC32 PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC32 is guaranteed for operation from 0°C to 70°C (NL suffix).

All package styles conform to JEDEC standards.

EPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 ± 8 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C to 70°C	−40°C to 85°C	0°C to 70°C	−40°C to 85°C
TMS27C32-XXX	JL	JE	JL4	JE4

These 32K EPROMs and PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 12-13 V supply is needed for programming. All programming signals are TTL level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. Fast programming uses a V_{PP} of 12.5 V and a V_{CC} of 6.0 V for a nominal programming time of two minutes. SNAP! Pulse programming uses a V_{PP} of 13.0 V and a V_{CC} of 6.5 V for a nominal programming time of 1 second. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation listed in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V for Fast, or 13.0 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION (PINS)	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$ (18)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}/V_{PP}$ (20)	V_{IL}	V_{IH}	X†	V_{PP}	V_{IL}	V_{PP}	V_{IL}	
V_{CC} (24)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (22)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (8)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8 (9-11, 13-17)	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	CODE	
							MFG	DEVICE
							97	08

†X Can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C32s or TMS27PC32s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}/V_{PP}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8.

latchup immunity

Latchup immunity on the TMS27C32 and TMS27PC32 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001; *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family,"* available through TI Field Sales Offices.

power down

Active I_{CC} current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C32)

Before programming, the TMS27C32 EPROM is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). EPROM erasure before programming is necessary to assure that all bits are in the logic 1 (high) state. Logic 0s are programmed into the desired locations. A programmed logic 0 can be erased only by ultraviolet light. The recommended minimum ultraviolet light exposure dose (UV intensity × exposure time) is 15 watt-seconds per square centimeter. A typical 12-milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C32, the window should be covered with an opaque label.

initializing (TMS27PC32)

The one-time programmable TMS27PC32 PROM is provided with all bits in the logic 1 state, then logic 0s are programmed into the desired locations. Logic 0s programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 32K EPROM and PROM can be programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which can reduce programming time to a nominal of one second. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100 μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when $\overline{G}/V_{PP}$ = 13.0 V, V_{CC} = 6.5 V, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified when V_{CC} = 5 V, $\overline{G}/V_{PP}$ = V_{IL}, and $\overline{E}$ = V_{IL}.

fast programming

The 32K EPROM and PROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming, data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{E}$ is pulsed. The programming mode is achieved when $\overline{G}/V_{PP}$ = 12.5 V, V_{CC} = 6.0 V, and $\overline{E} = V_{IL}$. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Fast programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6.0 V and $\overline{G}/V_{PP}$ = 12.5 V. When the full Fast programming routine is complete, all bits are verified when $V_{CC} = \overline{G}/V_{PP} = 5$ V.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified when $\overline{G}/V_{PP}$ and $\overline{E} = V_{IL}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 22) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 8); i.e., A0 = V_{IL} accesses the manufacturer code which is output on Q1-Q8; A0 = V_{IH} accesses the device code which is output on Q1-Q8. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for these devices is 97, and the device code is 08.

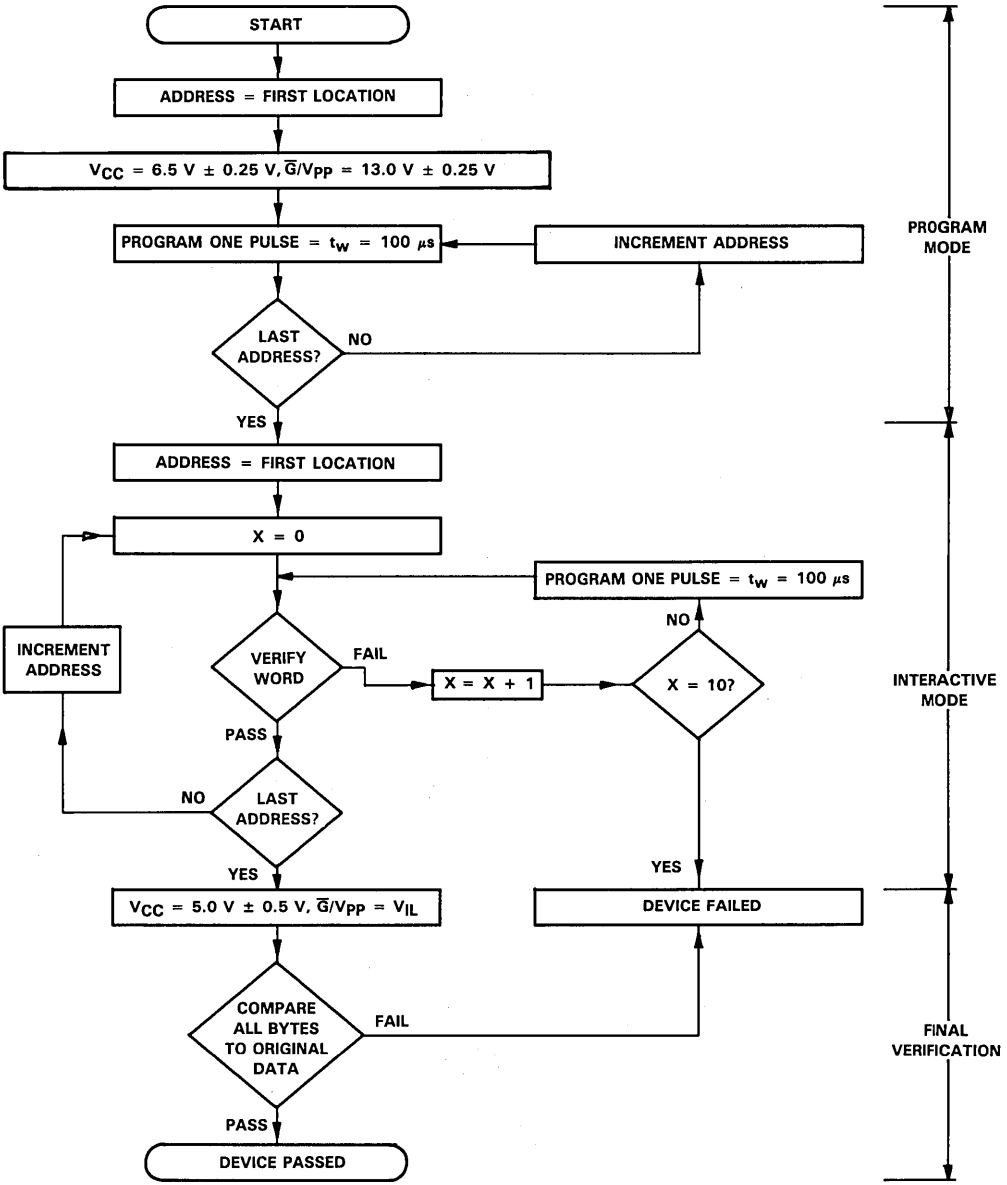


FIGURE 1. SNAP! PULSE PROGRAMMING FLOWCHART

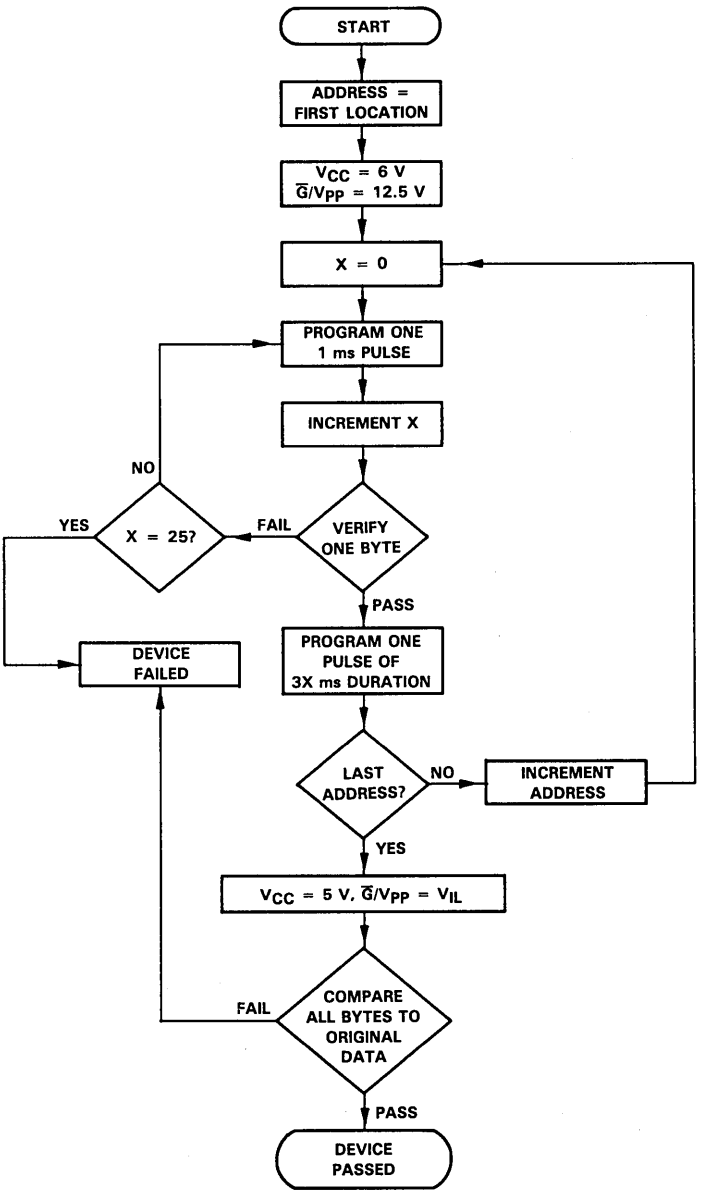
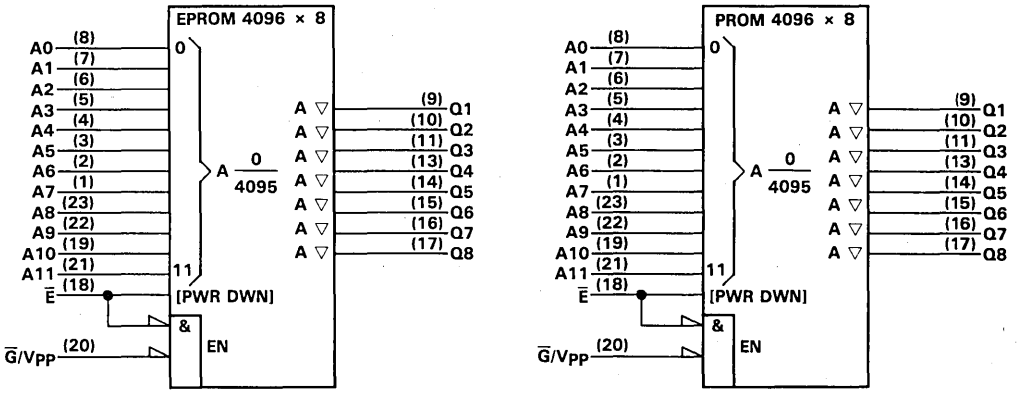


FIGURE 2. FAST PROGRAMMING FLOWCHART

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 . . . . . −0.6 V to 6.5 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C32-_ _JL and JL4; '27PC32-_ _NL) . . . . . 0°C to 70°C
Operating free-air temperature range ('27C32-_ _JE and JE4) . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

‡Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'27C32-100, '27C/PC32-120, '27C/PC32-150, '27C/PC32-2, '27C/PC32			'27C32-10, '27C/PC32-12, '27C/PC32-15, '27C/PC32-20, '27C/PC32-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.75	5	5.25	4.5	5	5.5	V
		Fast programming algorithm	5.75	6	6.25	5.75	6	6.25	
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	6.25	6.5	6.75	
$\overline{G}/V_{PP}$	Supply voltage	Fast programming algorithm	12	12.5	13	12	12.5	13	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	12.75	13	13.25	
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		0.2	−0.5		0.2	
T_A	Operating free-air temperature (See table, page 2)		(See table, page 2)			(See table, page 2)			°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −2.5 mA	3.5			V
			I_{OH} = −20 μA	$V_{CC}-0.1$			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
			I_{OL} = 20 μA			0.1	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±1	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±1	μA
I_{PP}	$\overline{G}/V_{PP}$ supply current (during program pulse)		$\overline{G}/V_{PP}$ = 13 V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		250	500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	250	μA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		10	25	mA

†Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	10	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		10	14	pF

†Typical values are at T_A = 25°C and nominal voltages.
‡Capacitance measurements are made on sample basis only.

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switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C32-100 '27C32-10		'27C/PC32-120 '27C/PC32-12		'27C/PC32-150 '27C/PC32-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input t_r ≤20 ns, Input t_f ≤20 ns		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}/V_{PP}$			50		55		75	ns
t_{dis}	Output disable time from $\overline{G}/V_{PP}$ or $\overline{E}$, whichever occurs first†		0	40	0	45	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}/V_{PP}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C/PC32-2 '27C/PC32-20		'27C/PC32 '27C/PC32-25		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input t_r ≤20 ns, Input t_f ≤20 ns		200		250	ns
$t_{a(E)}$	Access time from chip enable			200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}/V_{PP}$			75		100	ns
t_{dis}	Output disable time from $\overline{G}/V_{PP}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}/V_{PP}$, whichever occurs first†		0		0		ns

†Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6 V and $\overline{G}/V_{PP}$ = 12.5 V (Fast) or V_{CC} = 6.50 V and $\overline{G}/V_{PP}$ = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 3)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}/V_{PP}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}/V_{PP}$			150	ns

NOTES: 3. For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 (reference page 11).
4. Common test conditions apply for t_{dis} except during programming.

recommended timing requirements for programming: V_{CC} = 6 V and $\overline{G}/V_{PP}$ = 12.5 V (Fast) or V_{CC} = 6.50 V and $\overline{G}/V_{PP}$ = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 3)

			MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	μs
$t_{w(FPGM)}$	Final pulse duration	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			μs
$t_{su(D)}$	Data setup time		2			μs
$t_{su(VPP)}$	$\overline{G}/V_{PP}$ setup time		2			μs
$t_{su(VCC)}$	V_{CC} setup time		2			μs
$t_{h(A)}$	Address hold time		0			μs
$t_{h(D)}$	Data hold time		2			μs
$t_{h(VPP)}$	$\overline{G}/V_{PP}$ hold time		2			μs
$t_{rec(PG)}$	$\overline{G}/V_{PP}$ recovery time		2			μs
t_{EHD}	Data valid from $\overline{E}$ low				1	μs
$t_{r(PG)G}$	$\overline{G}/V_{PP}$ rise time		50			ns

NOTE 3: For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 (reference page 11).

PARAMETER MEASUREMENT INFORMATION

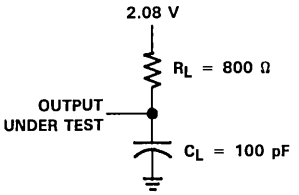
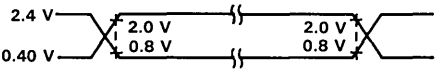


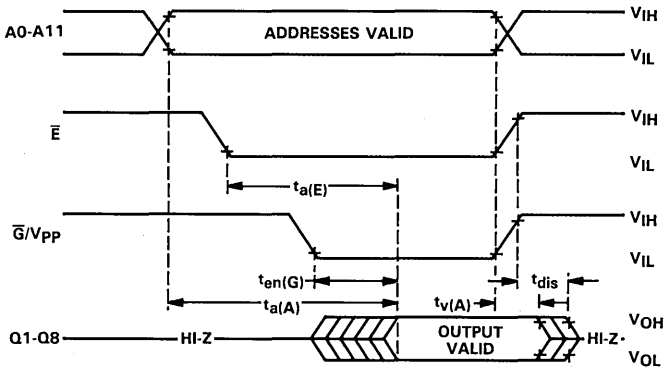
FIGURE 3. OUTPUT LOAD CIRCUIT

AC testing input/output wave forms

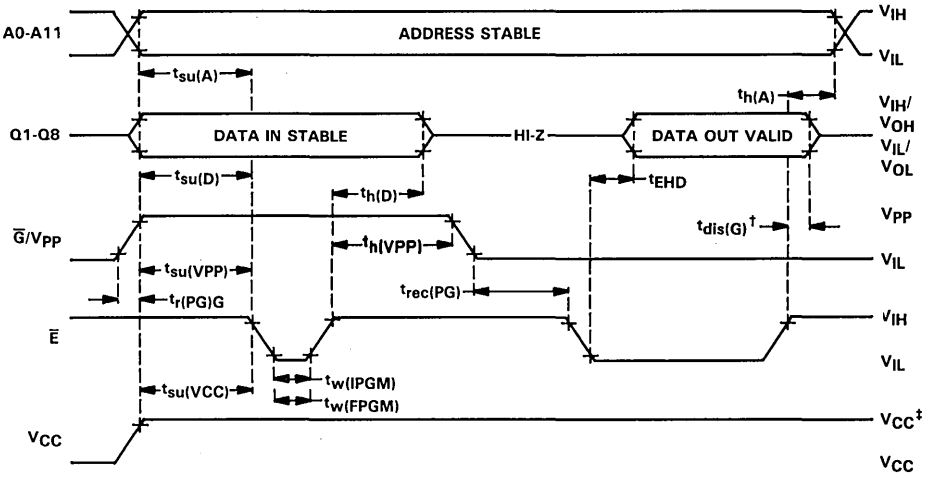


A.C. testing inputs are driven at 2.4 V for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 for both outputs.

read cycle timing



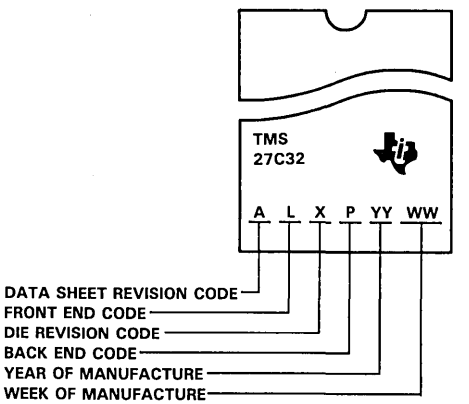
program cycle timing



†$t_{dis(G)}$ is a characteristic of the device but must be accommodated by the programmer.
‡12.5 V $\overline{G}/V_{PP}$ and 6.0 V V_{CC} for Fast programming; 13.0 V $\overline{G}/V_{PP}$ and 6.50 V V_{CC} for SNAP! Pulse programming.

device symbolization

This data sheet is applicable to all TI TMS27C32 CMOS EPROMs and TMS27PC32 CMOS PROMs with the data sheet revision code "A" as shown below.



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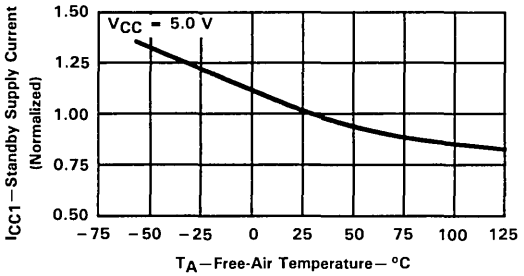
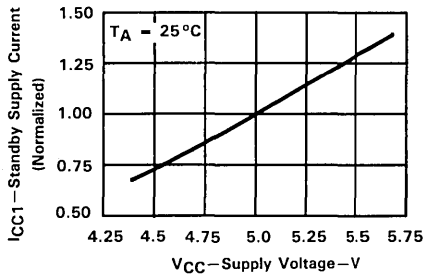
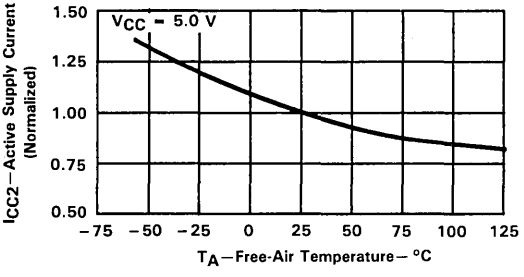
STANDBY SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



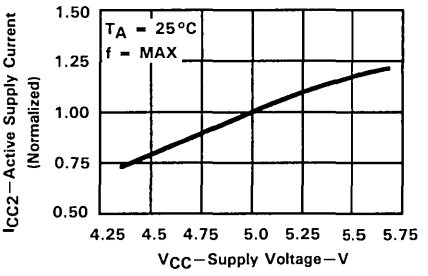
STANDBY SUPPLY CURRENT
vs
SUPPLY VOLTAGE



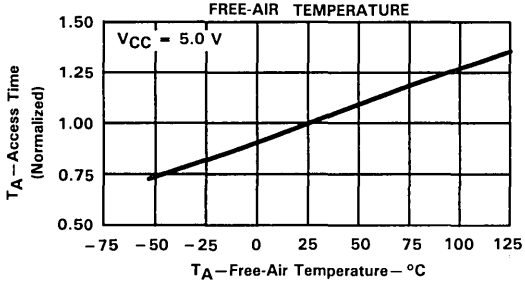
ACTIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



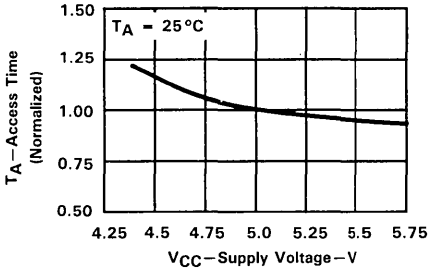
ACTIVE SUPPLY CURRENT
vs
SUPPLY VOLTAGE



ACCESS TIME
vs
FREE-AIR TEMPERATURE



ACCESS TIME
vs
SUPPLY VOLTAGE



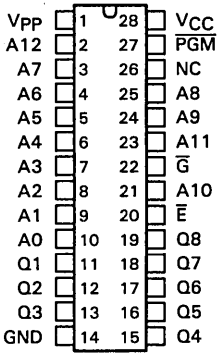
JULY 1983 – REVISED MARCH 1988

- Organization . . . 8192K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 64K EPROMs
- All Inputs and Outputs are TTL Compatible
- Max Access/Min Cycle Time

TMS2764-17	170 ns
TMS2764-20	200 ns
TMS2764-25	250 ns
TMS2764-45	450 ns

- Low Standby Power Dissipation . . . 184 mW (Maximum)
- JEDEC Approved Pinout
- 21-V Power Supply Required for Programming
- Fast Programming Algorithm
- N-Channel Silicon-Gate Technology
- PEP4 Version Available with 168 Hour Burn-in and Guaranteed Operating Temperature Range from −10°C to 85°C (TMS2764-_ _JP4)

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	21-V Power Supply

description

The TMS2764 is an ultraviolet-light erasable, electrically programmable read-only memory. It has 65,536 bits organized as 8,192 words of 8-bit length. The TMS2764 only requires a single 5-volt power supply with a tolerance of ±5%.

The TMS2764 provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in microprocessor systems. The TMS2764 has a power-down mode that reduces maximum power dissipation from 150 mA to 35 mA when the device is placed on standby.

This EPROM is supplied in a 28-pin, 15,2-mm (600-mil) dual-in-line ceramic package and is designed for operation from 0°C to 70°C. The TMS2764 is also offered in the PEP4 version with an extended guaranteed operating temperature range of −10°C to 85°C and 168 hour burn-in (TMS2764-_ _JP4).

operation

The six modes of operation for the TMS2764 are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down (Standby)	Fast Programming	Program Verification	Inhibit Programming
$\overline{E}$ (20)	V_{IL}	X†	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$ (22)	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X†
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X†	V_{IL}	V_{IH}	X†
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP} or V_{CC}
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
Q1-Q8 (11 to 13, 15 to 19)	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z

†X = V_{IH} or V_{IL}

read/output disable

The two control pins ($\overline{E}$ and $\overline{G}$) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum active current from 150 mA to 35 mA. A TTL high-level signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}$.

erasure

Before programming, the TMS2764 is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 mW/cm^2 UV lamp will erase the device in approximately 20 minutes. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS2764, the window should be covered with an opaque label.

Fast programming

Note that the application of a voltage in excess of 22 V to V_{PP} may damage the TMS2764.

After erasure, logic 0s are programmed into the desired locations. Programming consists of the following sequence of events. With the level on V_{PP} equal to 21 V and $\overline{E}$ at TTL low, data to be programmed is applied in parallel to output pins Q1-Q8. The location to be programmed is addressed. Once data and addresses are stable, a TTL low-level pulse is applied to $\overline{PGM}$. Programming pulses must be applied at each location that is to be programmed. Locations may be programmed in any order.

Programming uses two types of programming pulse: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each application, the byte being programmed is verified. If the correct data is read, the Final programming pulse is then applied. If correct data is not read, a further 1 millisecond programming pulse is applied up to a maximum X of 15. The Final programming pulse is 4X milliseconds long. This sequence of programming pulses and byte verification is done at V_{CC} = 6.0 V and V_{PP} = 21.0 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V. A flowchart of the Fast programming routine is shown in Figure 1.

multiple device programming

Several TMS2764s can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

program inhibit

The program inhibit is useful when programming multiple TMS2764s connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ or $\overline{PGM}$ of the device that is not to be programmed.

program verify

Programmed bits may be verified with V_{PP} = 21 V when $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL} and $\overline{PGM}$ = V_{IH}.

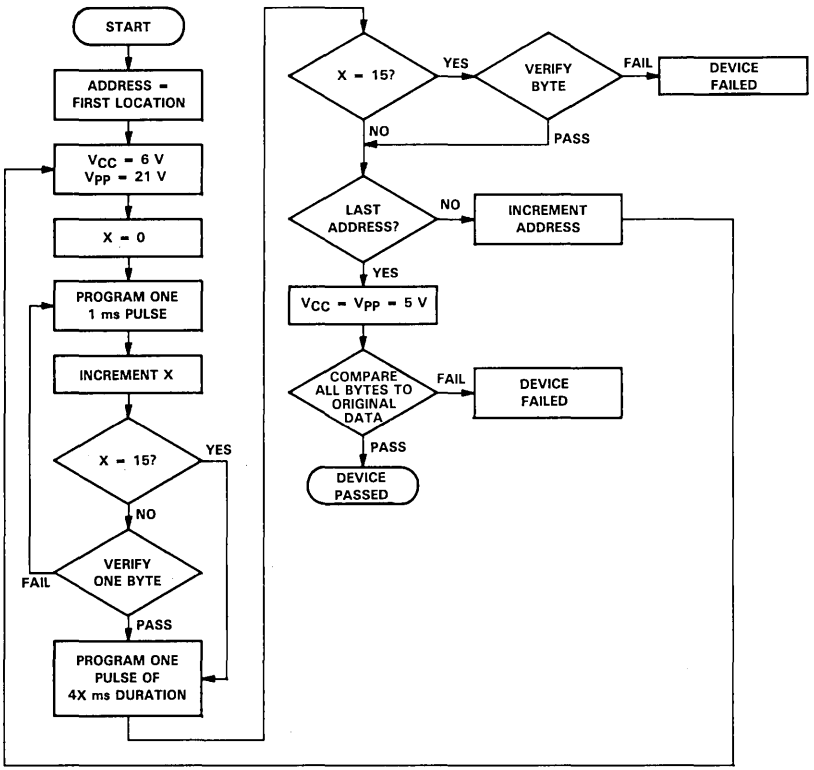
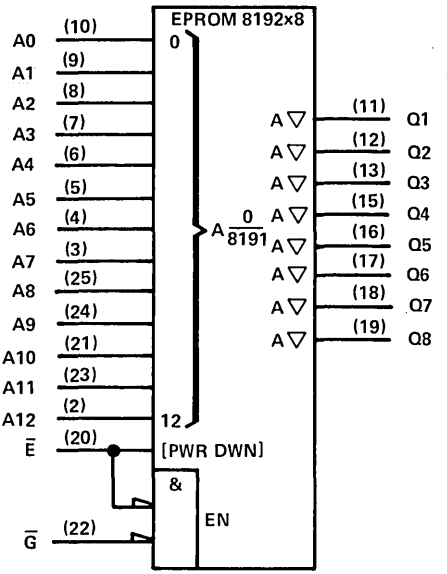


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} . . . . . −0.6 V to 22 V
Input voltage range . . . . . −0.6 V to 7 V
Output voltage range . . . . . −0.6 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage		V_{CC}		V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 1)	−0.1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 1: The algebraic convention, where the more negative (less positive) limit is designated as minimum is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA		0.45	V
I_I	Input current (load)	V_I = 0 V to 5.25 V		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V		±10	μA
I_{PP1}	V_{PP} supply current (read)	V_{PP} 5.25 V		15	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{E}$ and $\overline{PGM}$ at V_{IL}		50	mA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}		35	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}$ at V_{IL}		150	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER		TEST CONDITIONS	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V	6	9	pF
C_o	Output capacitance	V_O = 0 V	8	12	pF

†Capacitance measurements are made on a sample basis only.
‡Typical values are at T_A = 25°C and nominal voltage.

switching characteristics over recommended supply voltage range and operating free-air temperature range, C_L = 100 pF, 1 Series 74 TTL load (see Note 2 and Figure 2)

PARAMETER		TMS2764-17		TMS2764-20		TMS2764-25		TMS2764-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		170		200		250		450	ns
$t_{a(E)}$	Access time from $\overline{E}$		170		200		250		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		65		75		100		150	ns
$t_{dis(G)}$§	Output disable time from $\overline{G}$	0	60	0	60	0	85	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first	0		0		0		0		ns

NOTE 2: For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2.0 V.

§Value calculated from 0.5 V delta to measured output level; $t_{dis(G)}$ is specified from $\overline{G}$ or $\overline{E}$, whichever occurs first. Refer to read-cycle timing diagram. This parameter is only sampled and not 100% tested.

recommended conditions for Fast programming routine, T_A = 25°C (see Note 2 and Fast programming cycle time diagram)

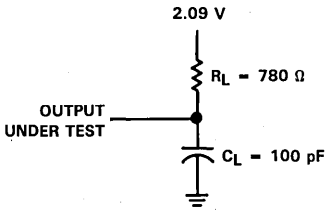
	PARAMETER	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)	5.75	6	6.25	V
V_{PP}	Supply voltage (see Note 4)	20.5	21	21.5	V
$t_{w(IPGM)}$	$\overline{PGM}$ initial program pulse duration (see Note 5)	0.95	1	1.05	ms
$t_{w(FPGM)}$	$\overline{PGM}$ final pulse duration (see Note 6)	3.8		63	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{su(E)}$	$\overline{E}$ setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs

Fast programming characteristics, T_A = 25°C (see Note 2 and Fast programming cycle timing diagram)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{dis(G)FP}$	Output disable time from $\overline{G}$ (see Note 7)	C_L = 100 pF	0		130	ns
$t_{en(G)FP}$	Output enable time from $\overline{G}$	1 Series 74 TTL Load			150	

NOTES: 2. For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2.0 V.
3. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
4. When programming the TMS2764, connect a 0.1 μF capacitor between V_{PP} and GND to suppress spurious voltage transients which may damage the device.
5. The Initial program pulse duration tolerance is 1 ms ±5%.
6. The length of the Final pulse will vary from 3.8 ms to 63 ms depending on the number of Initial pulse applications (X).
7. This parameter is only sampled and is not 100% tested.

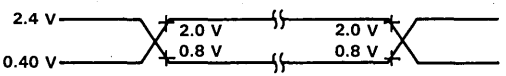
PARAMETER MEASUREMENT INFORMATION



NOTE 8: $t_f \leq 20$ ns and $t_r \leq 20$ ns.

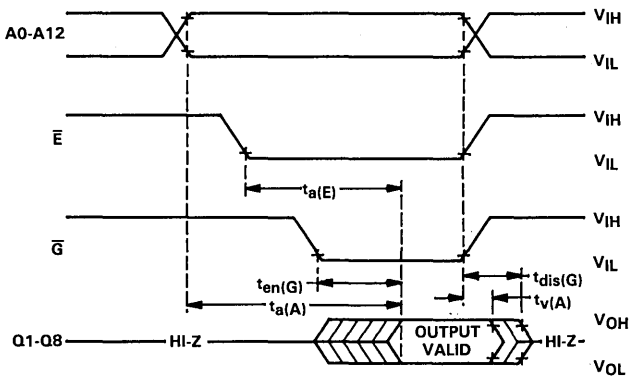
FIGURE 2. TYPICAL OUTPUT LOAD CIRCUIT

AC testing input/output wave forms

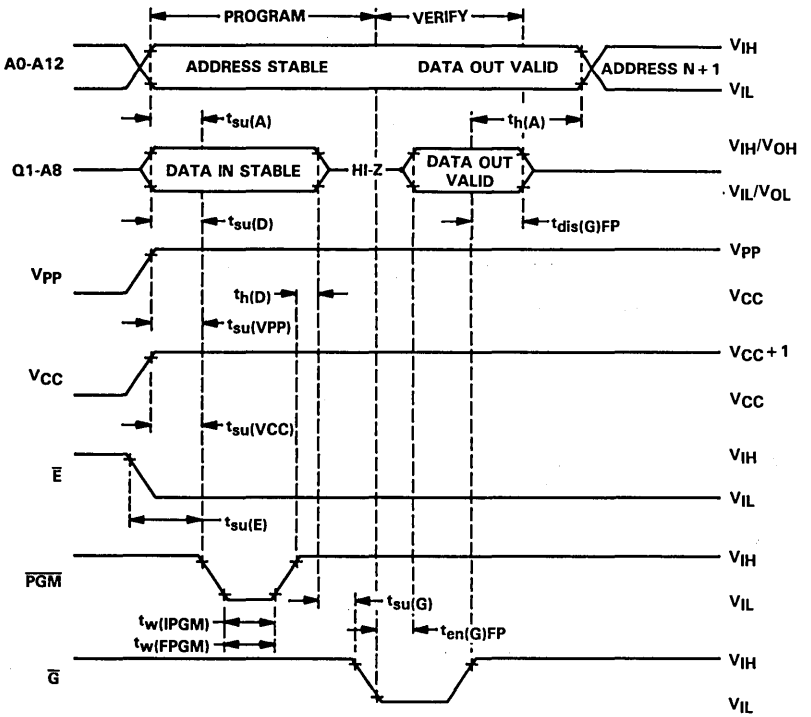


A.C. testing inputs are driven at 2.4 for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 for both inputs and outputs.

read cycle timing



fast program cycle timing



TMS27C49 65,536-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC49 65,536-BIT PROGRAMMABLE READ-ONLY MEMORY

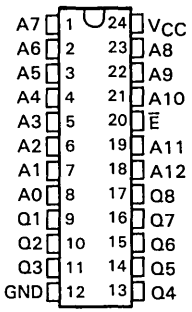
MAY 1988

- Organization . . . 8K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 8K × 8 Bipolar/High-Speed CMOS EPROMs and PROMs
- All Inputs/Outputs TTL Compatible
- High Speed
- Max Access/Min Cycle Time

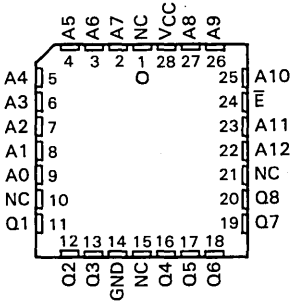
V_{CC} ± 5%	V_{CC} ± 10%	
'27C49-4	'27C49-45	45 ns
'27PC49-4	'27PC49-45	45 ns
'27C49-5	'27C49-55	55 ns
'27PC49-5	'27PC49-55	55 ns

- Low-Power CMOS Technology
- 3-State Output Buffers
- Fast Programming . . . 100 μs Pulse
- Low Power Dissipation (V_{CC} = 5.25 V)
  — Active . . . 495 mW Worst Case
- Erasable
- 100% Pretestable

J, JT, N AND NT PACKAGES† (TOP VIEW)



FN PACKAGE† (TOP VIEW)



†Pins have different pin assignments and functions in the program mode.

description

The TMS27C49 EPROM series are 65,536-bit, ultraviolet-light erasable, electrically programmable read-only memories in ceramic packages (J or JT suffix).

The TMS27PC49 PROM series are 65,536-bit, one-time, electrically programmable read-only memories in plastic packages (N, NT, or FN suffix). These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive eight Series 74 TTL circuits without pull-up resistors.

READ MODE

PIN NOMENCLATURE	
A0-A12	Address Inputs
$\overline{E}$	Chip Enable
GND	Ground
NC	No Connection
Q1-Q8	Outputs
V_{CC}	5-V Power Supply

The data outputs are three-state for connecting multiple devices to a common bus. The J, JT, N, and NT packaged devices are pin compatible with existing 24-pin high-speed EPROMs and bipolar PROMs.

The JT and NT packages are designed for insertion in mounting-hole rows on 7,62-mm (300 mil) centers. The J and N packages are designed for insertion in mounting-hole rows on 15,24-mm (600 mil) centers. The TMS27PC49 PROM is also provided in an FN plastic leaded chip carrier package for surface mounting on pads of 1,27-mm (50 mil) lead spacing.

The TMS27C49 EPROM and the TMS27PC49 PROM are guaranteed for operation from 0°C to 70°C (L suffix).

operation

There are nine modes of operation for the TMS27C49 and TMS27PC49 listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL or CMOS levels except for V_{PP}, $\overline{E}$, and $\overline{PGM}$, which can be high level voltages during specific modes.

FUNCTION	MODE								
	Read	Output Disable	Program Verify 0s	Program Verify 1s	Program Inhibit	Program	Blank Check 0s	Blank Check 1s	Signature
A12/VSEL†	X‡	X	$V_{IL(P)}$¶	$V_{IH(P)}$	$V_{IL(P)}$	$V_{IL(P)}$	$V_{IL(P)}$	$V_{IL(P)}$	X
A11/V_{PP}†	X	X	V_{PP}	V_{PP}	V_{PP}	V_{PP}	$V_{IL(P)}$	$V_{IH(P)}$	X
$\overline{E}/\overline{PE}$†	V_{IL}	V_{IH}	$V_{IL(P)}$	$V_{IL(P)}$	$V_{IH(P)}$	$V_{IL(P)}$	V_H§	V_H	V_{IL}
A10/$\overline{LAT}$†	X	X	$\overline{LAT}$	$\overline{LAT}$	$\overline{LAT}$	$\overline{LAT}$	$\overline{LAT}$	$\overline{LAT}$	X
A9/$\overline{PGM}$†	X	X	$V_{IH(P)}$	$V_{IH(P)}$	$V_{IH(P)}$	$V_{IL(P)}$	$V_{IL(P)}$	$V_{IL(P)}$	V_H
A8/$\overline{VFY}$†	X	X	$V_{IL(P)}$	$V_{IL(P)}$	$V_{IH(P)}$	$V_{IH(P)}$	$V_{IL(P)}$	$V_{IL(P)}$	X
Q1-Q8	D_{OUT}	HI-Z	D_{OUT}	D_{OUT}	HI-Z	D_{IN}	Zeros	Ones	CODE: MFG 97 / DEV F2

†Pin assignments for program mode.
‡X can be V_{IL} or V_{IH}.
§V_H = 12 V ± 0.5 V.
¶(P) = Programming mode.

read/output disable

When the outputs of two or more TMS27C49s or TMS27PC49s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of the selected TMS27C49 or TMS27PC49, a low-level signal is applied to $\overline{E}$. All other devices in the circuit should have their outputs disabled by applying a high-level signal to their $\overline{E}$ pins. Output data is accessed at pins Q1 through Q8.

latchup immunity

Latchup immunity is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

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erasure (TMS27C49-_ _JL and JTL EPROMs)

Before programming, the TMS27C49 EPROMs are erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is 25 watt-seconds per square centimeter. A typical 12 milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 45 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C49 EPROM, the window should be covered with an opaque label.

programming mode pin functions

In the programming mode, A12 becomes VSEL, A11 becomes V_{PP} supply, $\overline{E}$ becomes $\overline{PE}$ (program enable), A10 becomes $\overline{LAT}$ (latch) input, A9 becomes $\overline{PGM}$ (program) input, and A8 becomes $\overline{VFY}$ (verify) input. Latched inputs occur on pins 8 through 4 (J, JT, N, and NT packages) and on pins 9 through 5 (FN package) as A8L through A12L are multiplexed with A0 through A4 addresses on these pins.

blank check mode

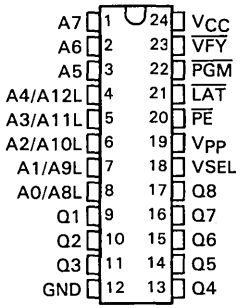
The TMS27C49 and the TMS27PC49 use a differential memory cell. This means that an unprogrammed device has ambiguous states in all address locations. Prior to programming, the blank check mode is used to verify that both sides of the differential cell are erased. The blank check mode is defined as $\overline{PE}$ to V_H; VSEL and $\overline{PGM}$ to $V_{IL(P)}$. In this mode, V_{PP} selects between blank check 0s and 1s. $\overline{VFY}$ acts as an output enable (see Figure 1).

programming mode

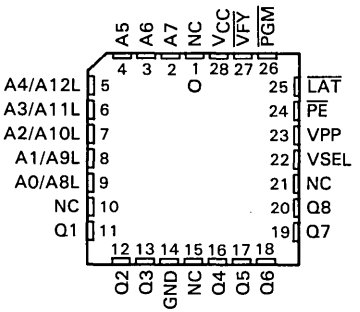
After erasure, logic 1s and 0s are programmed into the desired locations. Data is presented in parallel (eight bits) on pins Q1-Q8. High order addresses (A8L-A12L) are latched by pulsing $\overline{LAT}$. Once addresses and data are stable, $\overline{PGM}$ is pulsed. The programming mode is achieved when $V_{PP} = 13.5\,V$, $V_{CC} = 6.0\,V$, $\overline{PGM} = V_{IL(P)}$, $\overline{VFY} = V_{IH(P)}$, $\overline{PE} = V_{IL(P)}$, and VSEL = $V_{IL(P)}$.

PROGRAMMING AND BLANK CHECK MODE PIN ASSIGNMENTS

J, JT, N, AND NT PACKAGES (TOP VIEW)



FN PACKAGE (TOP VIEW)



PROGRAM MODE

PIN NOMENCLATURE	
A0-A7	Address Inputs
A8L-A12L	Latched Address Inputs
GND	Ground
$\overline{LAT}$	Latch Input
NC	No Connection
$\overline{PE}$	Program Enable
$\overline{PGM}$	Program Input
Q1-Q8	Data In/Data Out
V_{CC}	5-V Power Supply
$\overline{VFY}$	Verify Input
V_{PP}	13.5-V Power Supply
VSEL	Verify Select

More than one TMS27C49 or TMS27PC49 can be programmed when the devices are connected in parallel. Locations can be programmed in any order, but it is recommended that all locations be programmed. The length of the programming pulse is 100 μs; this pulse is applied X times. After each pulse the byte being programmed is verified. If it fails verify, another programming pulse is applied up to a maximum X = 25. If the part passes verify, the algorithm continues programming the remaining memory locations. This sequence of programming and verification is performed at V_{CC} = 6.0 V and V_{PP} = 13.5 V. When the programming routine is complete, all bits are verified with V_{CC} = 5.0 V ± 10% (see Figure 2).

program inhibit

Programming may be inhibited by maintaining a high-level input on the $\overline{PGM}$ or $\overline{PE}$ pins.

program verify

The TMS27C49 and TMS27PC49 use a differential memory cell for data storage. It is composed of two FAMOS transistors. One of the FAMOS transistors in the cell must be programmed for data to be read correctly. The condition of both FAMOS transistors in a cell being erased or both being programmed results in an undefined condition on the outputs. The TMS27C49 and the TMS27PC49 use a two-pass verify to ensure that a reliable data storage margin in the differential memory cell has been achieved without the need for an overprogramming pulse. During the program verify mode, the outputs from the differential memory cell are intentionally biased, or offset, to insure that a highly reliable program margin is achieved during normal read mode operation. Verify 1s skew the differential memory cell toward zeros and are used to check for programmed 1s. Verify 0s skew the differential memory cell towards 1s and are used to check for programmed 0s. Programmed bits may be verified with V_{PP} = 13.5 V when $\overline{VFY}$ = $V_{IL(P)}$, $\overline{PGM}$ = $V_{IH(P)}$, and VSEL = $V_{IL(P)}$ (verify 0s) or VSEL = $V_{IH(P)}$ (verify 1s).

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to V_H. Two identifier bytes are accessed by A0, ie., A0 = V_{IL} accesses the manufacturer code; A0 = V_{IH} accesses device code. Addresses A1-A4 must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for these devices is 97, and the device code is F2.

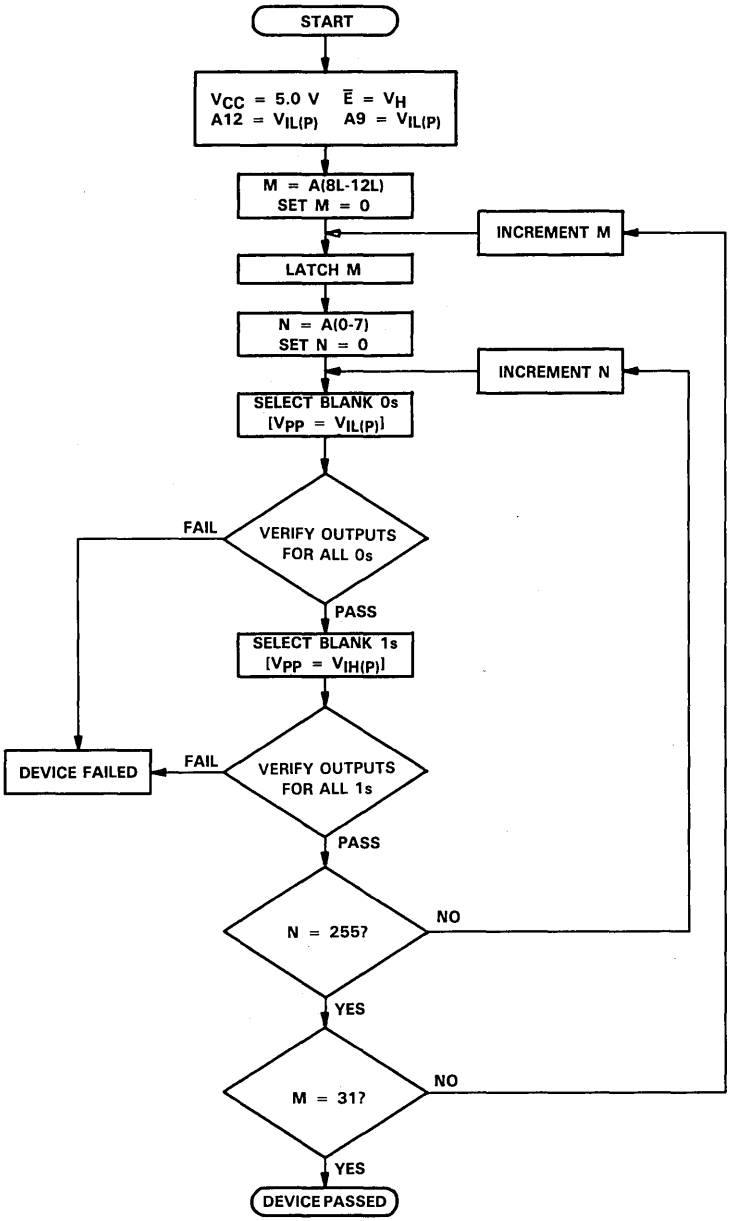


FIGURE 1. BLANK CHECK FLOWCHART

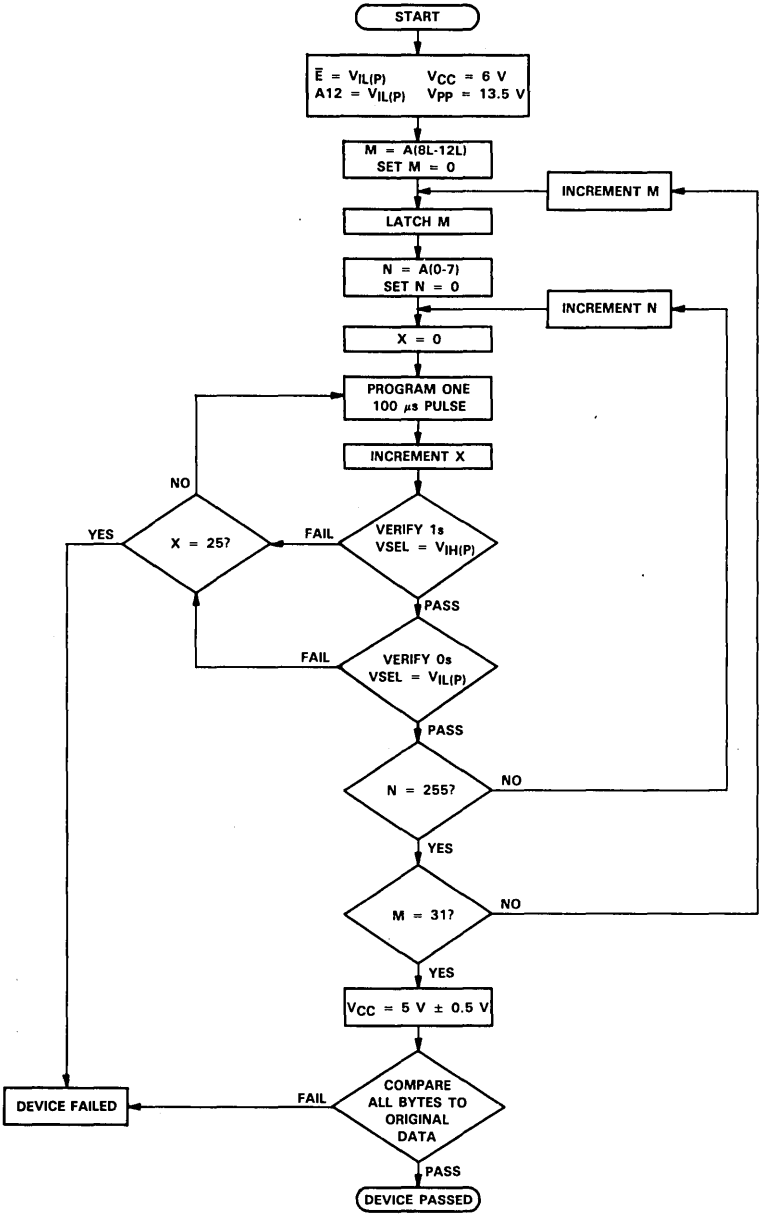


FIGURE 2. PROGRAMMING FLOWCHART

TEXAS INSTRUMENTS
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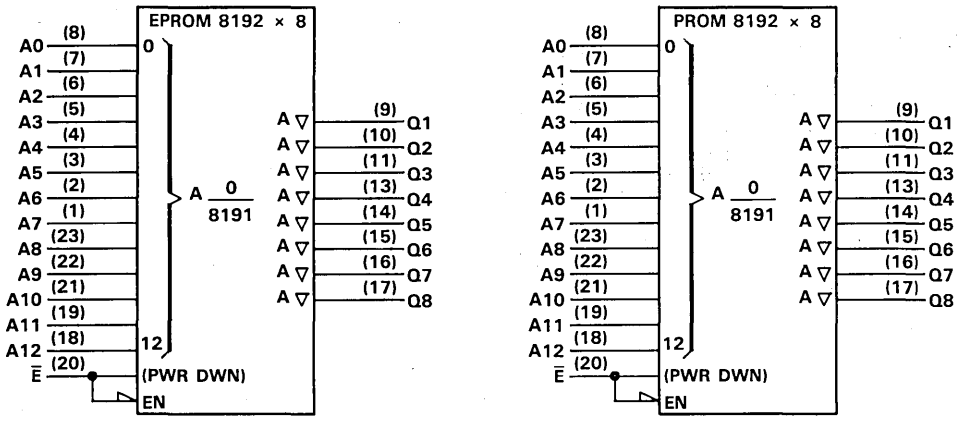
logic symbols†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J, JT, N, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} (programming mode) . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9, A11 and $\overline{E}$ . . . . . −0.6 V to 6.5 V
A9, A11 and $\overline{E}$ . . . . . −0.6 V to 14 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			'27C49-4, '27PC49-4 '27C49-5, '27PC49-5			'27C49-45, '27PC49-45 '27C49-55, '27PC49-55			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.5	5	5.5	V
V_{IH}	High-level input voltage (see Note 2)	TTL	2.0		$V_{CC}+1$	2.0		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	
$V_{IH(P)}$	High-level input voltage (see Note 2)	Programming	3		$V_{CC}+1$	3		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		GND+0.2	−0.5		GND+0.2	
$V_{IL(P)}$	Low-level input voltage (see Note 2)	Programming	−0.5		0.4	−0.5		0.4	V
T_A	Operating free-air temperature		0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum is used in this data sheet for logic voltage levels only. These are absolute voltages with respect to device ground pin and include overshoot due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −4.0 mA	2.4		V
V_{OL}	Low-level output voltage		I_{OL} = 16 mA		0.4	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V		±10	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}		±10	μA
I_{PP}	V_{PP} programming current		V_{PP} = 13.5 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		TBD	mA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC} ± 0.2 V		TBD	
I_{CC2}	V_{CC} supply current (active) (see Note 3)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		90	mA

NOTE 3: Assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, and a toggling between 0 V to 3 V. Minimum cycle time is equal to maximum access time.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	All inputs except A11	V_I = 0 V			10	pF
		A11	V_I = 0 V			20	
C_o	Output capacitance		V_O = 0 V			15	pF

†Capacitance measurements are made on a sample basis only.

switching characteristics over full ranges of recommended operating conditions (see Note 3 and Figure 3)

PARAMETER		'27C49-4, '27PC49-4 '27C49-45, '27PC49-45		'27C49-5, '27PC49-5 '27C49-55, '27PC49-55		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		45		55	ns
$t_{en(E)}$	Enable time from $\overline{E}$		35		35	ns
t_{dis}	Disable time from $\overline{E}$		35		35	ns
$t_{v(A)}$	Output valid time	0		0		ns

NOTE 3: Assume signal transition of 5 ns or less, timing reference levels of 1.5 V, and a toggling between 0 V to 3 V. Minimum cycle time is equal to maximum access time.

recommended timing requirements for programming (see Note 4)

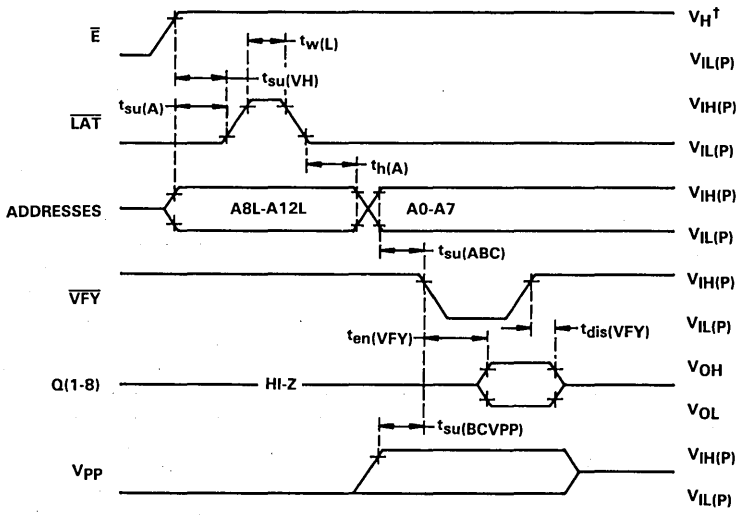
		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	95	100	105	μs
$t_{su(A)}$	Address setup time	1			μs
$t_{su(VPP)}$	V_{PP} setup time	1			μs
$t_{su(VFY)}$	$\overline{VFY}$ setup time	1			μs
$t_{dis(VFY)}$	Output disable time from $\overline{VFY}$			1	μs
$t_{en(VFY)}$	Output enable time from $\overline{VFY}$			1	μs
$t_{su(D)}$	Data setup time	1			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	1			μs
$t_{w(L)}$	Latch pulse duration	1			μs
$t_{h(LA)}$	Latched address hold time	1			μs
$t_{su(LA)}$	Latched address setup time	1			μs
$t_{su(PE)}$	$\overline{PE}$ setup time	1			μs
$t_{h(VSEL)}$	Data hold time after VSEL	0			μs
$t_{su(VSEL)}$	VSEL setup time	1			μs
$t_{v(VSEL)}$	VSEL to valid output	1			μs
$t_{su(VCC)}$	V_{CC} setup time	1			μs
V_{PP}	Programming voltage	13.25	13.5	13.75	V
V_{CC}	Supply voltage during programming	5.75	6	6.25	V
V_H	High voltage	11.5	12	12.5	V

NOTE 4: T_A = 25°C ± 5°C. Assume inputs toggling between 0 V and 3 V with timing reference made at the 10% and 90% levels.

recommended timing requirements for blank check

	PARAMETER	MIN	NOM	MAX	UNIT
$t_{su(VH)}$	V_H setup time	1			μs
$t_{su(A)}$	Address setup time	1			μs
$t_{w(L)}$	Latch pulse duration	1			μs
$t_{h(A)}$	Address hold time	1			μs
$t_{su(ABC)}$	Address setup time to Blank Check	1			μs
$t_{su(BCVPP)}$	Blank 0/Blank 1 Select setup time	1			μs
$t_{en(VFY)}$	Output enable time from $\overline{VFY}$			1	μs
$t_{dis(VFY)}$	Output disable time from $\overline{VFY}$			1	μs

blank check cycle timing



†V_H = 12.5 V ± 0.5 V

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PARAMETER MEASUREMENT INFORMATION

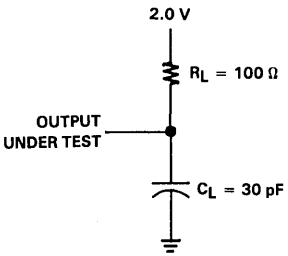
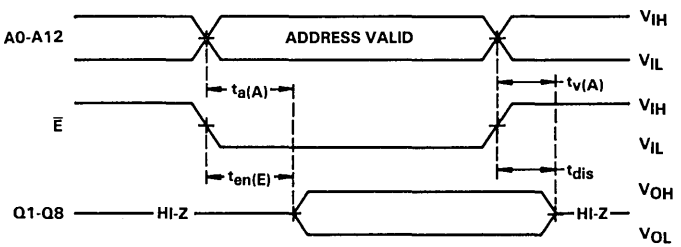
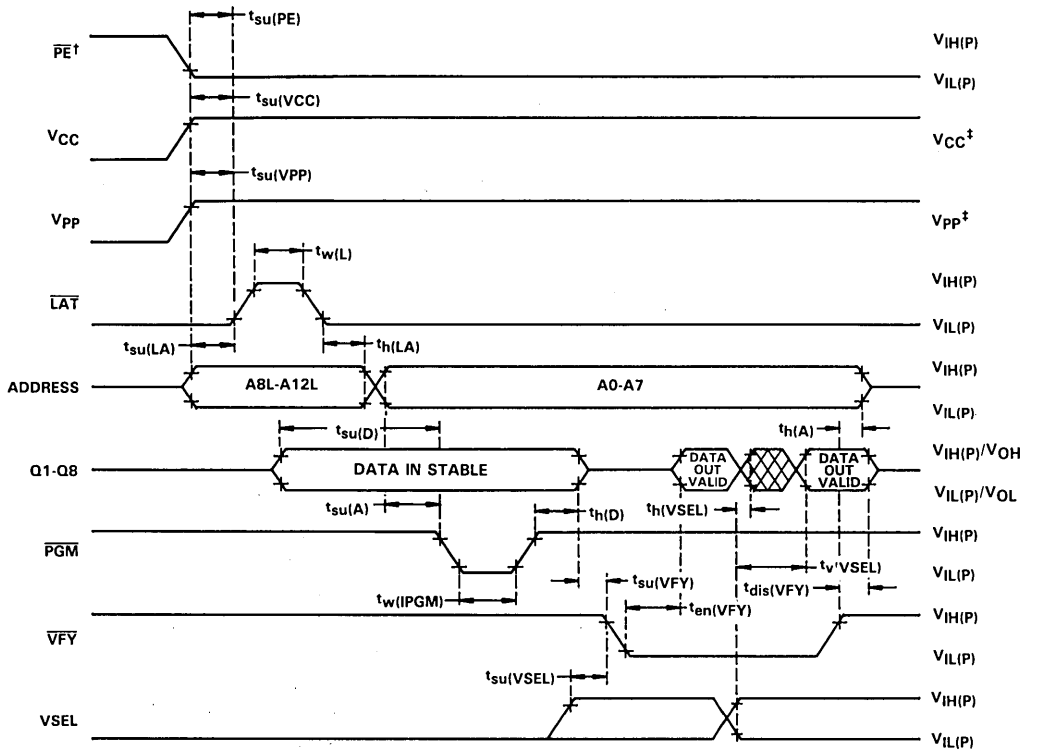


FIGURE 3. OUTPUT LOAD CIRCUIT

read cycle timing



program cycle timing



†High $\overline{PE}$ inhibits programming.
‡V_{CC} = 6.0 V and V_{PP} = 13.5 V.

TMS27C64 65,536-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC64 65,536-BIT PROGRAMMABLE READ-ONLY MEMORY

NOVEMBER 1985—REVISED APRIL 1988

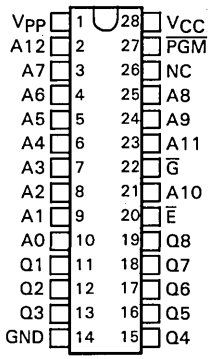
This Data Sheet is Applicable to All TMS27C64s and TMS27PC64s Symbolized with Code "A" as Described on Page 12.

- **Organization . . . 8K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible with Existing 64K MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**

V_{CC} ±5%	V_{CC} ±10%	
'27C64-100		100 ns
'27C/PC64-120	'27C/PC64-12	120 ns
'27C/PC64-1	'27C/PC64-15	150 ns
'27C/PC64-2	'27C/PC64-20	200 ns
'27C/PC64	'27C/PC64-25	250 ns

- **Power Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming or Fast Programming Algorithms**
- **3-State Output Buffers**
- **400 mV Guaranteed DC Noise Immunity with Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.25 V)**
  - **Active . . . 158 mW Worst Case**
  - **Standby . . . 1.4 mW Worst Case (CMOS Input Levels)**
- **PEP4 Version Available with 168 Hour Burn-In, and also Extended Guaranteed Operating Temperature Ranges**

J & N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Address Inputs
$\overline{E}$	Chip Enable Power Down
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
NU	Make No External Connection
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12-13 V Programming Power Supply

description

The TMS27C64 series are 65,536-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC64 series are 65,536-bit, one-time, electrically programmable read-only memories.

These devices are fabricated using power saving CMOS technology for high-speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C64 and the TMS27PC64 are pin compatible with 28-pin 64K MOS ROMs, PROMs, and EPROMs.

The TMS27C64 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C64 is available with two guaranteed temperature ranges of 0°C to 70°C and −40°C to 85°C (TMS27C64-_ _JL and TMS27C64-_ _JE, respectively). The TMS27C64 is also offered with 168-hour burn-in on both temperature ranges (TMS27C64-_ _JL4 and TMS27C64-_ _JE4, respectively). (See table below).

The TMS27PC64 PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC64 is guaranteed for operation from 0°C to 70°C.

All package styles conform to JEDEC standards.

EPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C to 70°C	−40°C to 85°C	0°C to 70°C	−40°C to 85°C
TMS27C64-XXX	JL	JE	JL4	JE4

These EPROMs and PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 12-13 V supply is needed for programming. All programming signals are TTL level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. Fast programming uses a V_{PP} of 12.5 V and a V_{CC} of 6.0 V for a nominal programming time of two minutes. SNAP! Pulse programming uses a V_{PP} of 13.0 V and a V_{CC} of 6.5 V for a nominal programming time of one second. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation listed in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V for Fast, or 13.0 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X	V_{IH}	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	CODE	
							MFG	DEVICE
							97	07

†X Can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C64s or TMS27PC64s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 through Q8.

latchup immunity

Latchup immunity on the TMS27C64 and TMS27PC64 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001; *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family,"* available through TI Field Sales Offices.

power down

Active I_{CC} current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C64)

Before programming, the TMS27C64 EPROM is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). EPROM erasure before programming is necessary to assure that all bits are in the logic 1 (high) state. Logic 0s are programmed into the desired locations. A programmed logic 0 can be erased only by ultraviolet light. The recommended minimum ultraviolet light exposure dose (UV intensity × exposure time) is 15 watt-seconds per square centimeter.

A typical 12-milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C64, the window should be covered with an opaque label.

initializing (TMS27PC64)

The one-time programmable TMS27PC64 PROM is provided with all bits in the logic 1 state, then logic 0s are programmed into the desired locations. Logic 0s programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 64K EPROM and PROM can be programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart of Figure 1, which can reduce programming time to a nominal of one second. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins Q1 through Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100 μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13.0 V, V_{CC} = 6.5 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

Fast programming

The 64K EPROM and PROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming, data is presented in parallel (eight bits) on pins Q1 through Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, V_{CC} = 6.0 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Fast programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6.0 V and V_{PP} = 12.5 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code, which is output on Q1-Q8; A0 = V_{IH} accesses the device code, which is output on Q1-Q8. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for these devices is 97, and the device code is 07.

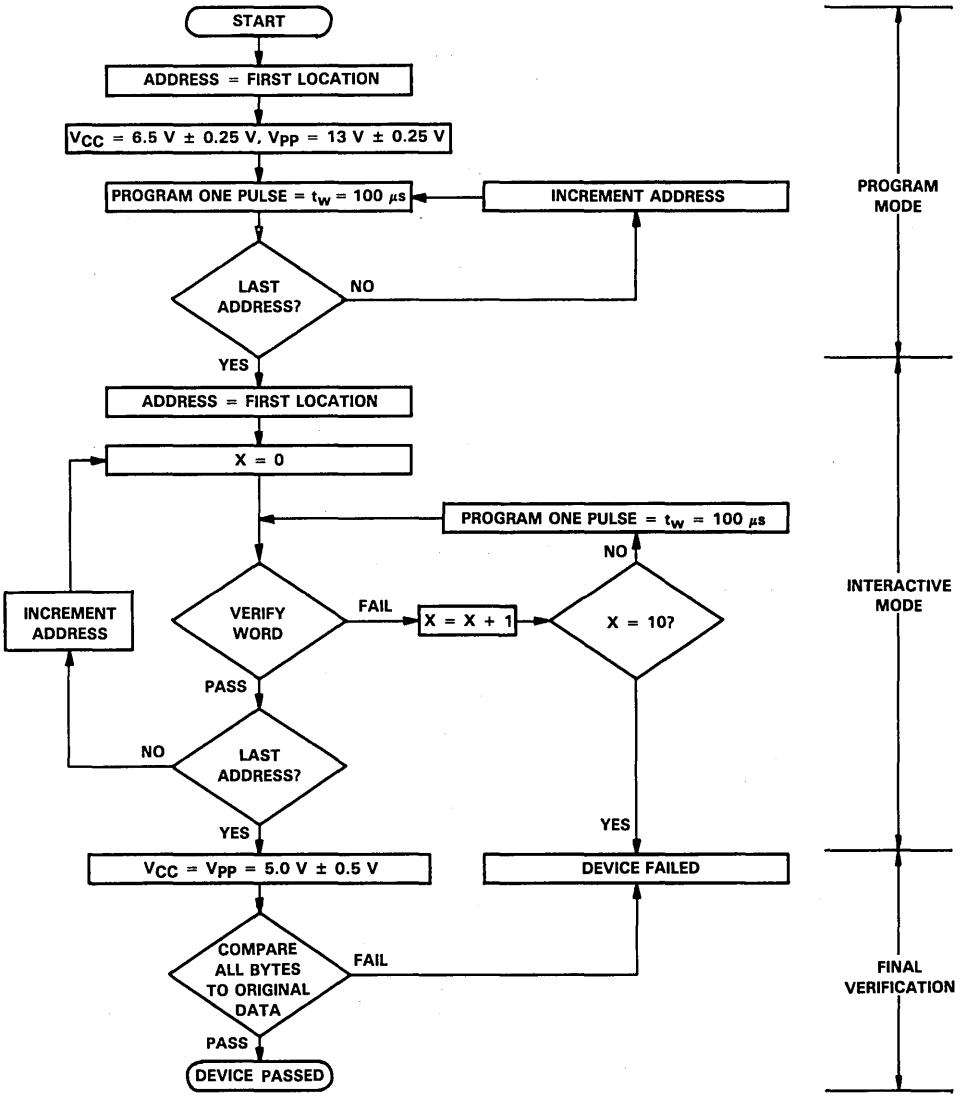


FIGURE 1. SNAP! PULSE PROGRAMMING FLOWCHART

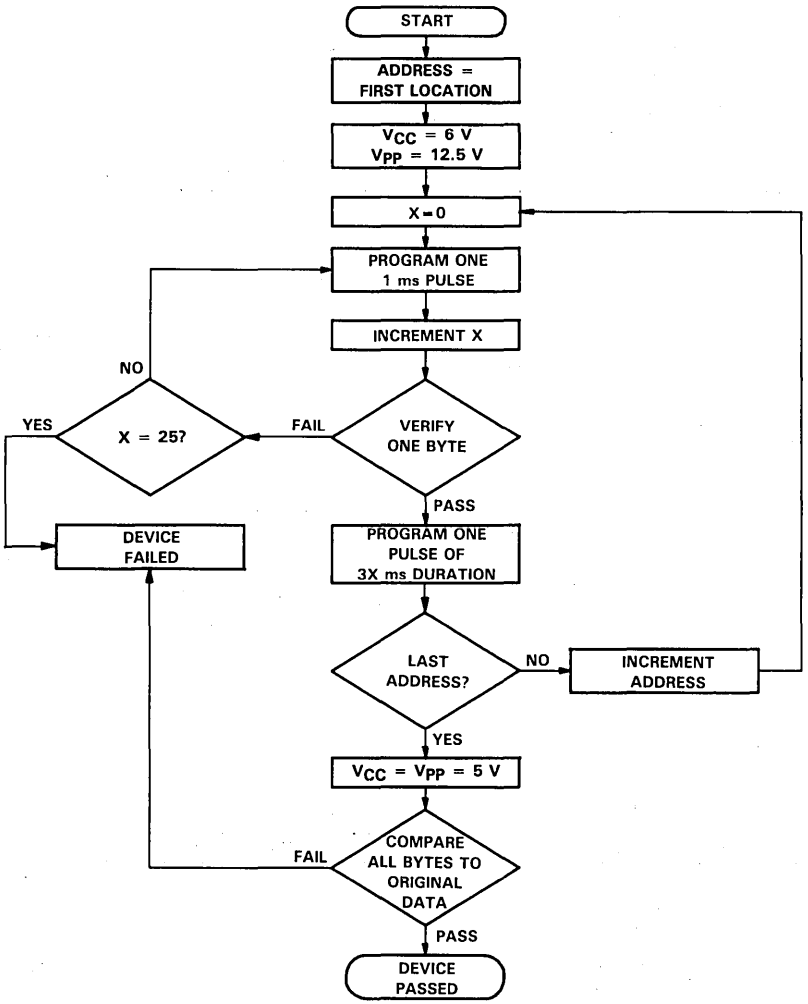


FIGURE 2. FAST PROGRAMMING FLOWCHART

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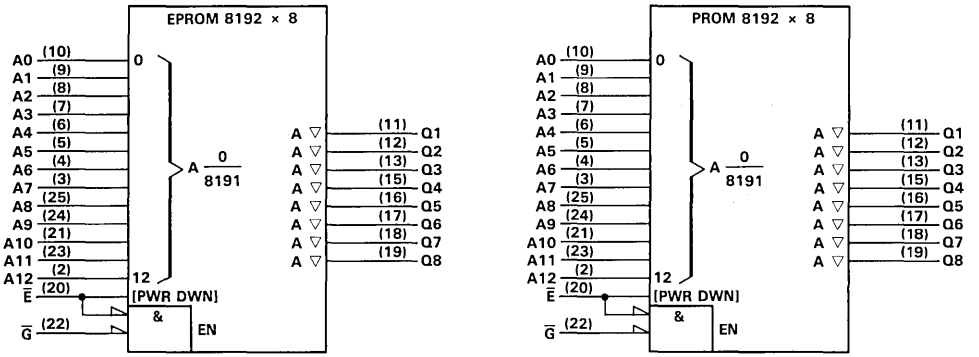
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
J and N packages illustrated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 . . . . . −0.6 V to 6.5 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C64-_ _JL and JL4; '27PC64-_ _NL) . . . . . 0°C to 70°C
Operating free-air temperature range ('27C64-_ _JE and JE4) . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			'27C64-100, '27C/PC64-120, '27C/PC64-1, '27C/PC64-2, '27C/PC64			'27C/PC64-12, '27C/PC64-15, '27C/PC64-20, '27C/PC64-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.75	5	5.25	4.5	5	5.5	V
		Fast programming algorithm	5.75	6	6.25	5.75	6	6.25	V
		SNAP! Pulse programming algorithm	6.25	6.50	6.75	6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)	$V_{CC}-0.6$		$V_{CC}+0.6$	$V_{CC}-0.6$		$V_{CC}+0.6$	V
		Fast programming algorithm	12	12.5	13	12	12.5	13	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	12.75	13	13.25	V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		0.2	−0.5		0.2	V
T_A	Operating free-air temperature (see table, page 2)		(see table, page 2)			(see table, page 2)			°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −2.5 mA	3.5			V
			I_{OH} = −20 μA	$V_{CC}-0.1$			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
			I_{OL} = 20 μA			0.1	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±1	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±1	μA
I_{PP1}	V_{PP} supply current		$V_{PP} = V_{CC}$ = 5.5 V		1	10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E} = V_{IH}$		250	500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E} = V_{CC}$		100	250	μA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		15	30	mA

†Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	10	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		10	14	pF

†Typical values are at T_A = 25°C and nominal voltages.
‡Capacitance measurements are made on sample basis only.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C64-100		'27C/PC64-120 '27C/PC64-12		'27C/PC64-1 '27C/PC64-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		55		75	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	40	0	45	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C/PC64-2 '27C/PC64-20		'27C/PC64 '27C/PC64-25		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		200		250	ns
$t_{a(E)}$	Access time from chip enable			200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

†Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.50 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

NOTES: 4. For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0. (Reference page 10.)
5. Common test conditions apply for t_{dis} except during programming.

recommended timing requirements for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.5 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 4)

			MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	μs
$t_{w(FPGM)}$	Final pulse duration	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			μs
$t_{su(E)}$	$\overline{E}$ setup time		2			μs
$t_{su(G)}$	$\overline{G}$ setup time		2			μs
$t_{su(D)}$	Data setup time		2			μs
$t_{su(VPP)}$	V_{PP} setup time		2			μs
$t_{su(VCC)}$	V_{CC} setup time		2			μs
$t_{h(A)}$	Address hold time		0			μs
$t_{h(D)}$	Data hold time		2			μs

NOTE 4: For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 (reference below).

PARAMETER MEASUREMENT INFORMATION

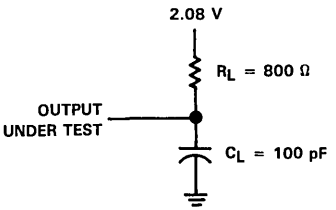
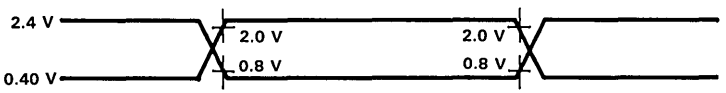


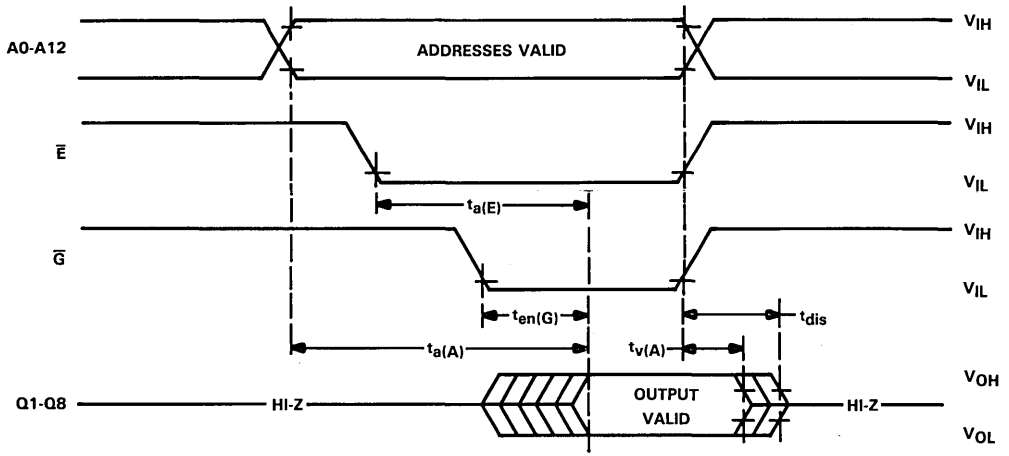
FIGURE 3. OUTPUT LOAD CIRCUIT

AC testing input/output wave forms

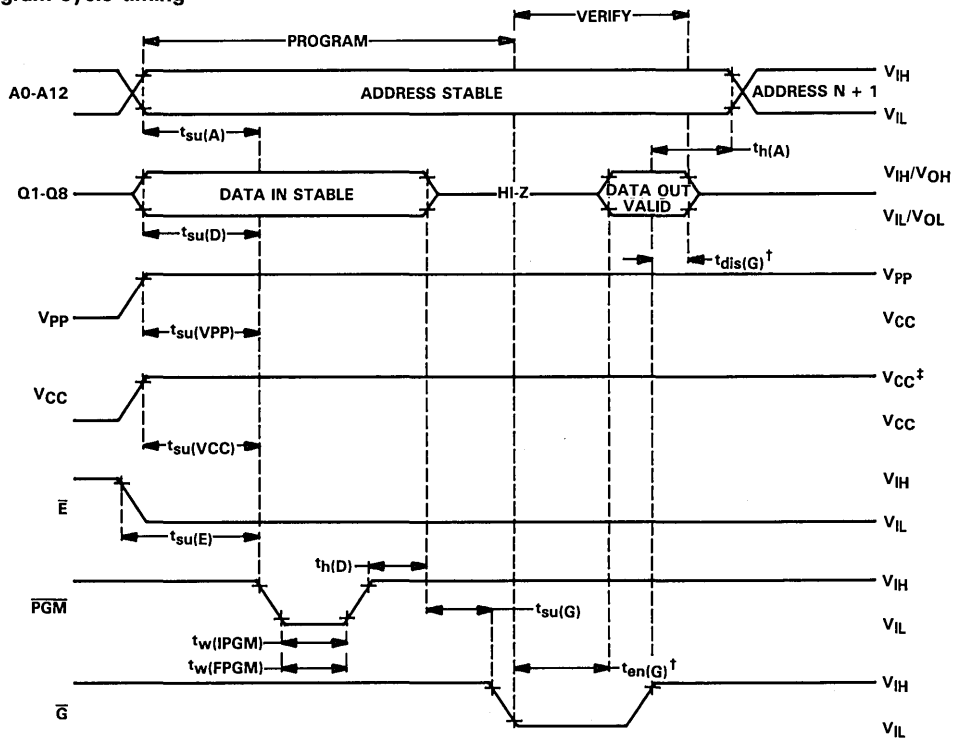


A.C. testing inputs are driven at 2.4 V for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 for both outputs.

read cycle timing



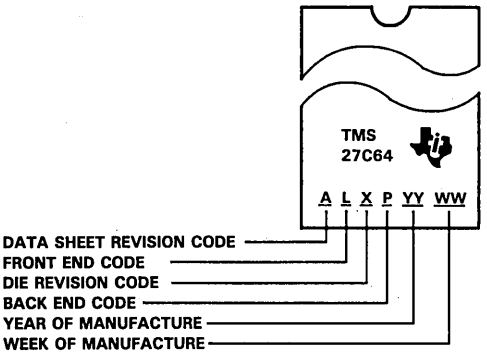
program cycle timing



†$t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡12.5 V V_{PP} and 6.0 V V_{CC} for Fast programming; 13.0 V V_{PP} and 6.5 V V_{CC} for SNAP! Pulse programming.

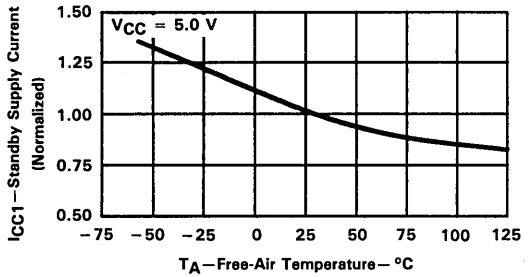
device symbolization

This data sheet is applicable to all TI TMS27C64 CMOS EPROMs and TMS27PC64 PROMs with the data sheet revision code "A" as shown below.

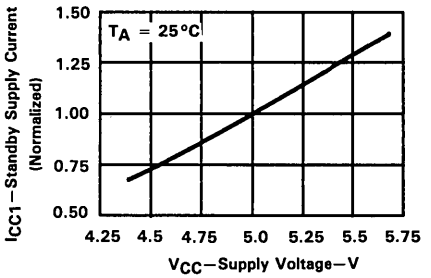


TYPICAL TMS27C/PC64 CHARACTERISTICS

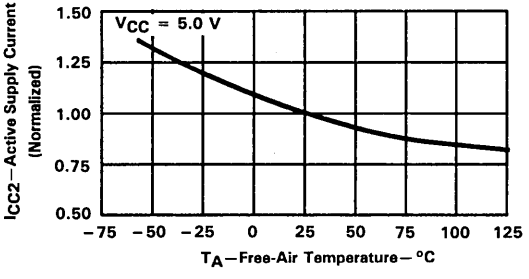
STANDBY SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



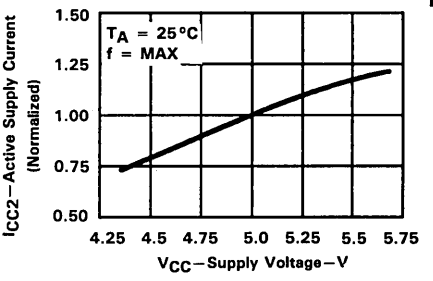
STANDBY SUPPLY CURRENT
vs
SUPPLY VOLTAGE



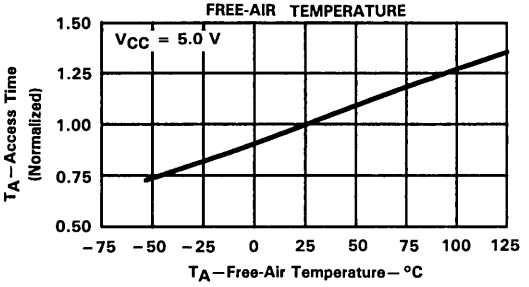
ACTIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



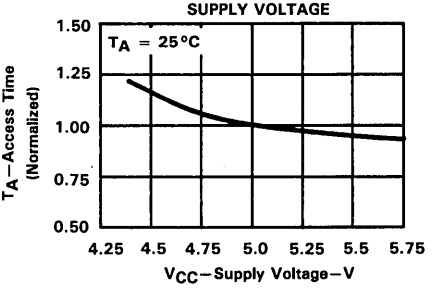
ACTIVE SUPPLY CURRENT
vs
SUPPLY VOLTAGE



ACCESS TIME
vs
FREE-AIR TEMPERATURE



ACCESS TIME
vs
SUPPLY VOLTAGE

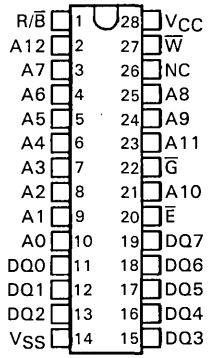


65,536-BIT ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY

JUNE 1988

- Organization 8K × 8
- Single 5-V Power Supply (± 10%)
- Compatible with Existing 64K MOS EPROMs, PROMs, ROMs, and EEPROMs
- JEDEC Standard Pinout
- All Inputs/Outputs TTL Compatible
- Max Access/Min Cycle Times
  - TMS28C64-25 250 ns
  - TMS28C64-35 350 ns
- 2-μ CMOS Silicon Gate Technology
- Single Byte and Page (32 Bytes) Write:
  - —Latched Address and Data
  - —Self-Timed Programming Operation (10 ms Typical)
  - —Data Polling and Ready/Busy Verifications
- Fast Read Mode Operation:
  - —Byte Mode (250 ns Typical Access Time)
  - —Word Mode (350 ns Typical Access Time)
- 10,000 Cycles Endurance
- Inadvertent Write Protection
- Low Power Dissipation:
  - —Active . . . 110 mW Worst Case
  - —Standby . . . 17 mW Worst Case
- Operating Free-Air Temperature 0°C to 70°C

N AND J PACKAGES
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Addresses
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
DQ0-DQ7	Inputs/Outputs
R/$\overline{B}$	Ready/Busy Output
V_{CC}	5-V Power Supply
V_{SS}	Ground
NC	No Connection

descripton

The TMS28C64 is a 65,536-bit, electrically erasable programmable read only memory. This device is fabricated using 2-μ CMOS twin-well silicon gate flotox technology for high reliability and very low power dissipation. All inputs can be driven by Series 74 TTL circuits without the use of external resistors. The data I/O are three-state for connecting multiple devices to a common bus.

The TMS28C64 EEPROM is offered in a dual-in-line ceramic package (J suffix) and a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS28C64 EEPROM is guaranteed for operation from 0°C to 70°C (L suffix).

The TMS28C64 is organized as 8K × 8 bits. It features internal circuitry to minimize external hardware interface (single 5-V power supply, internal latch of address and data buses during write operation, data polling and ready/busy pin signaling end-of-write).

The device performs the programming operation automatically and can write a single byte or any number of bytes between 1 and 32 (page mode), which the user is able to load within a time window of 200 μs from the moment the write operation is enabled.

During a programming operation, the data polling and the ready/busy functions are enabled to notify the memory to ignore any command until the operation is completed.

The device has power-up/power-down protection to prevent inadvertent write operations.

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All the mode functions and the electrical conditions to access them are listed in the following table.

FUNCTIONS (PINS)	MODE			
	READ	OUTPUT DISABLE	STANDBY AND WRITE INHIBIT	WRITE
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}
$\overline{G}$ (22)	V_{IL}	V_{IH}	X	V_{IH}
A11 (25)	X	X	X	X
A9 (24)	X	X	X	X
$\overline{W}$ (27)	V_{IH}	V_{IH}	X	V_{IL}
DQ0-DQ7 (11-13, 15-19)	D_{OUT}	HI-Z	HI-Z	D_{IN}

X = Don't care for $V < V_{CC}$

operation

read/output disable

When the outputs of two or more TMS28C64s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices.

To read the output of the TMS28C64, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ0 to DQ7.

In word read-mode (where the word is defined as two bytes whose address is different only for A0) it is possible to read the second word byte much faster (100 ns) than the first one (250 ns).

latchup immunity

Latchup immunity on the TMS28C64 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} current can be reduced from 10 mA to 1.5 mA typical by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

write

Single byte write initiates with a $\overline{W}$ low and $\overline{G}$ high applied to a selected device. This performs the writing, at the location selected by address pins, of the data present at the I/O pins.

Addresses are latched on the last falling edge of $\overline{E}$ or $\overline{W}$, while data is latched on the first rising edge of $\overline{E}$ or $\overline{W}$.

Single byte write cycle is completed in 10 ms typical.

automatic page write

The TMS28C64 performs the write operation automatically, and 1 to 32 bytes of data can be written into the EEPROM in a single write cycle (10 ms typical).

Following a byte write signal, an internal window is open. While this window is open, the user is allowed to send up to 31 further bytes, each one of them by a new byte write signal.

After 200 μs the part will perform the simultaneous writing of all the addressed bytes.

Total time for the entire array writing (256 pages) is 2.56 seconds typical.

During the page mode, the addresses A5 through A12 must be the same as the first byte. The bytes may be written in any order.

data polling

The TMS28C64 provides a software means (data polling) to signal that the device is performing a write operation. During the write cycle, after an attempt to read any byte, the device answers with the last received byte, except for DQ7, whose logical value is inverted.

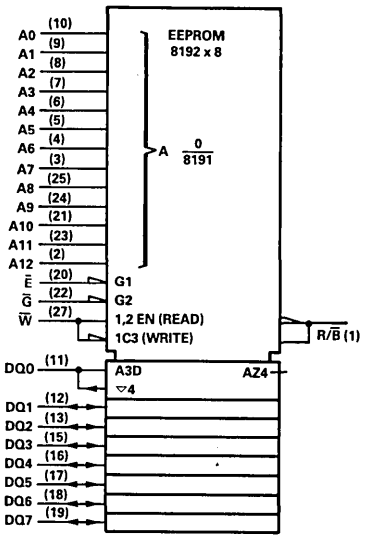
ready/busy

The TMS28C64 also provides the possibility of signaling if the device is performing a byte or a page write cycle by the ready/busy output (low during the write cycle). Ready/busy is an open-drain output with a 10 kΩ external resistor to V_{CC}.

inadvertent write operation protection

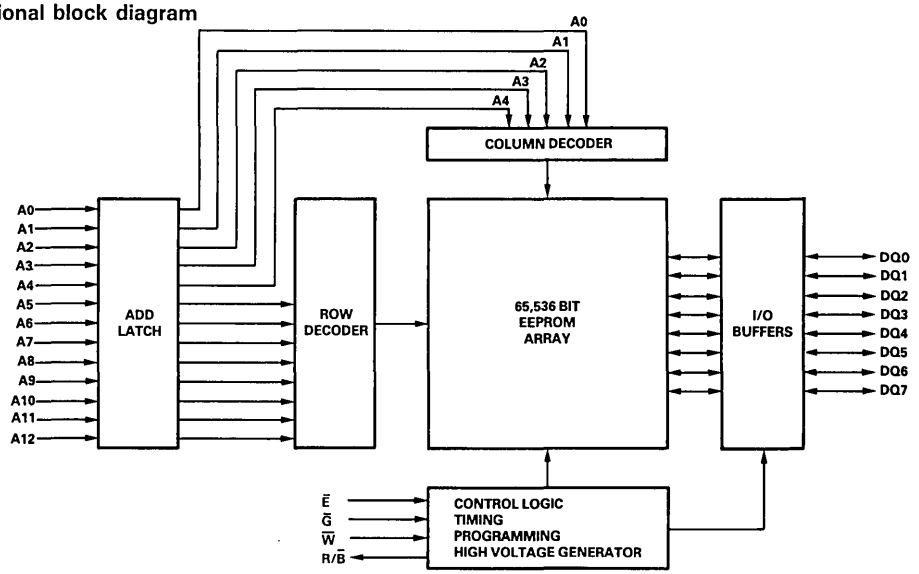
The device is protected against write command during power-up for 25 μs typical after V_{CC} reaches 4 volts. At the end of this interval, the signals at input pins, $\overline{E}$, $\overline{G}$, and $\overline{W}$ must be stable to avoid inadvertent write operation.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1985 and IEC Publication 617-12.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Input voltage range (see Note 1) . . . . . −0.6 V to 6.5 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 0.6 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 125°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage	−0.5		0.8	V
$t_{c(RD)}$	Read cycle time	(See tables, pages 6 and 7)			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over full range of operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage (except R/$\overline{B}$)	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage (including R/$\overline{B}$)	I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.5 V			±10	μA
I_O	Output current (leakage) (including R/$\overline{B}$)	V_O = 0.1 V to V_{CC}			±10	μA
I_{CC1}	V_{CC} supply current (standby)	V_{CC} =5.5 V, E = V_{IH}		1.5	3	mA
I_{CC2}	V_{CC} average supply current (active read)	t_{cycle} = min. cycle outputs open			20	mA
I_{CC3}	V_{CC} average supply current (active write)	t_{cycle} = 15 ms			10	mA

‡Typical values are T_A = 25°C and nominal voltage.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz§

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		8	12	pF

‡Typical values are at T_A = 25°C and nominal voltage.
§Capacitance measurements are made on sample basis only.

PARAMETER MEASUREMENT INFORMATION

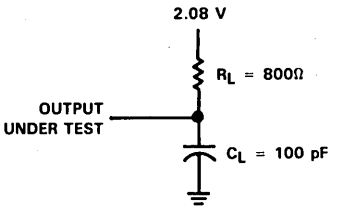
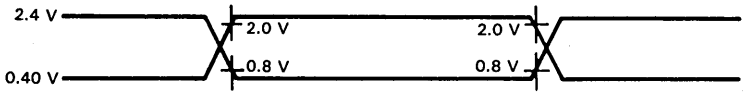


FIGURE 1. OUTPUT LOAD CIRCUIT

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for both inputs and outputs.

read cycle (byte mode)

PARAMETER		TMS28C64-25			TMS28C64-35			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(RD)}$	Read cycle time	250			350			ns
$t_{a(E)}$	Chip enable access time			250			350	ns
$t_{a(A)}$	Address access time			250			350	ns
$t_{a(G)}$	Output enable access time			100			150	ns
t_{lz}	Chip enable to output enable		50			75		ns
t_{hz}	Chip disable to output disable		100			125		ns
t_{olz}	Output enable time from $\overline{G}$		50			75		ns
t_{ohz}	Output disable time from $\overline{G}$		100			125		ns
t_{oh1}	Output hold from A0-A12 address change		20			20		ns
t_{oh2}	Output hold from A0 address change		20			20		ns

NOTE 2: For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 (reference above).

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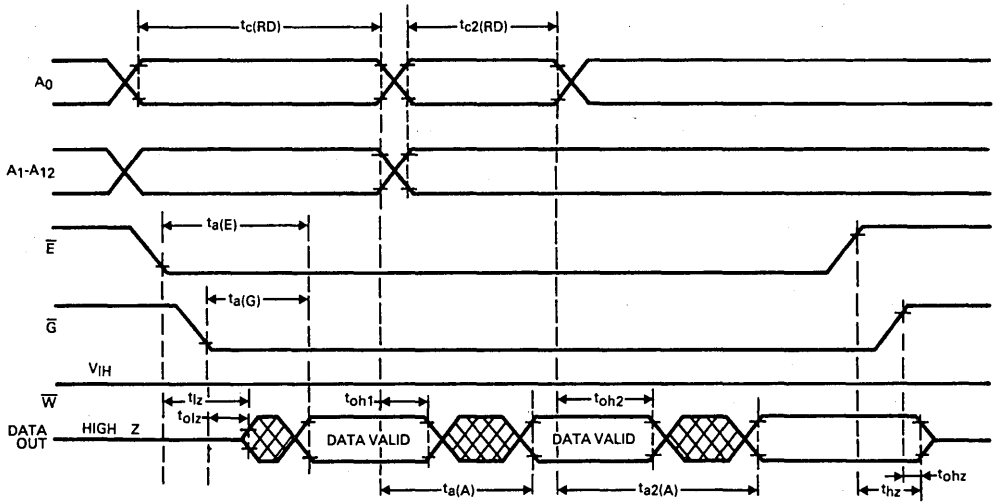
read cycle (word mode)

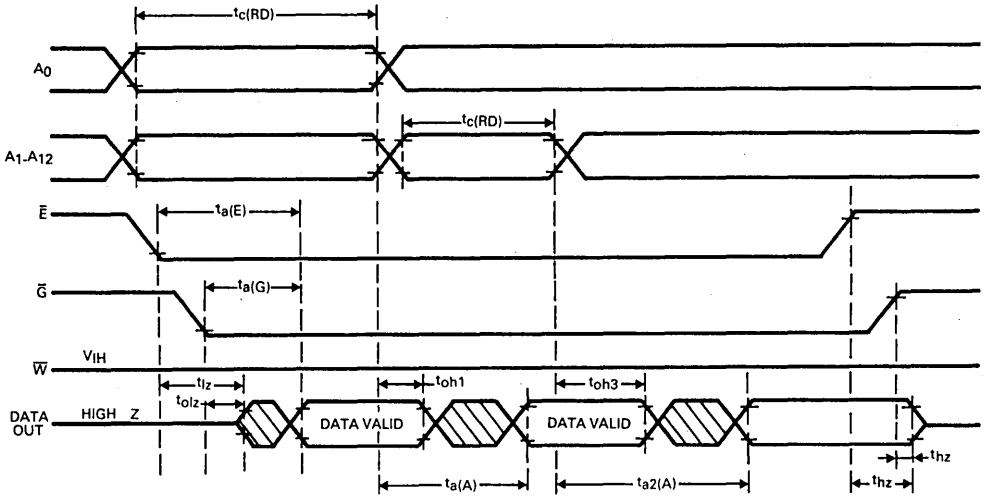
PARAMETER		TMS28C64-25			TMS28C64-35			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(RD)}$	Read cycle time 1st byte	250			350			ns
$t_{c2(RD)}$	Read cycle time 2nd byte	100			130			ns
$t_{a(E)}$	Chip enable access time			250			350	ns
$t_{a(A)}$	Address access time 1st byte			250			350	ns
$t_{a2(A)}$	A0 access time 2nd byte			100			130	ns
$t_{a(G)}$	Output enable access time			100			150	ns
t_{lz}	Chip enable to output enable		50			75		ns
t_{hz}	Chip disable to output disable		100			125		ns
t_{olz}	Output enable time from $\overline{G}$		50			75		ns
t_{ohz}	Output disable time from $\overline{G}$		100			125		ns
t_{oh1}	Output hold from A0-A12 address change		20			20		ns
t_{oh2}	Output hold from A0 address change		20			20		ns
t_{oh3}	Output hold from A1-A12 address change		50			50		ns

NOTE 2: For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 (reference page 6).

byte and word read mode (A0 change hold time)



byte and word read mode (A1-A12 change hold time)



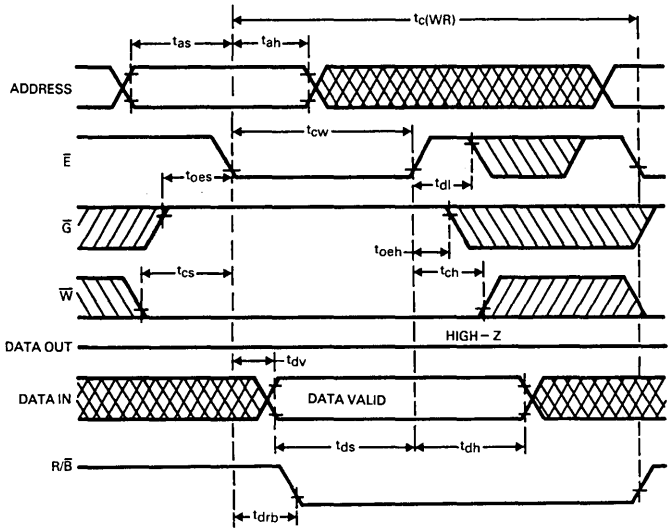
byte write cycle

PARAMETER		TMS28C64-25			TMS28C64-35			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(WR)}$	Write cycle time		10	15		10	15	ms
t_{as}	Address setup time	10			15			ns
t_{ah}	Address hold time	100			100			ns
t_{cs}	Write setup time	0			0			ns
t_{ch}	Write hold time	0			0			ns
t_{cw}	Chip enable to end of write input	150		500	150		500	ns
t_{oes}	Output enable setup time	10						ns
t_{oeh}	Output enable hold time	10			15			ns
t_{wp} †	Write pulse duration	150		500	150		500	ns
t_{dl}	Data latch time	20			30			ns
t_{dv}	Data valid time							ns
t_{ds}	Data setup time	100			130			ns
t_{dh}	Data hold time	30			30			ns
t_{drb}	Ready/Busy delay time			400			400	ns

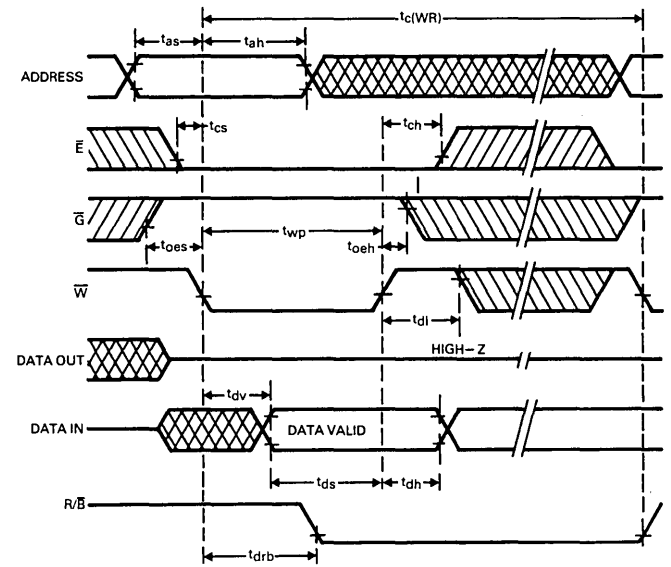
†$\overline{W}$ is noise protected. Glitches will not activate a write cycle.

NOTE 2: For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 (reference page 6).

$\overline{E}$ controlled byte write cycle



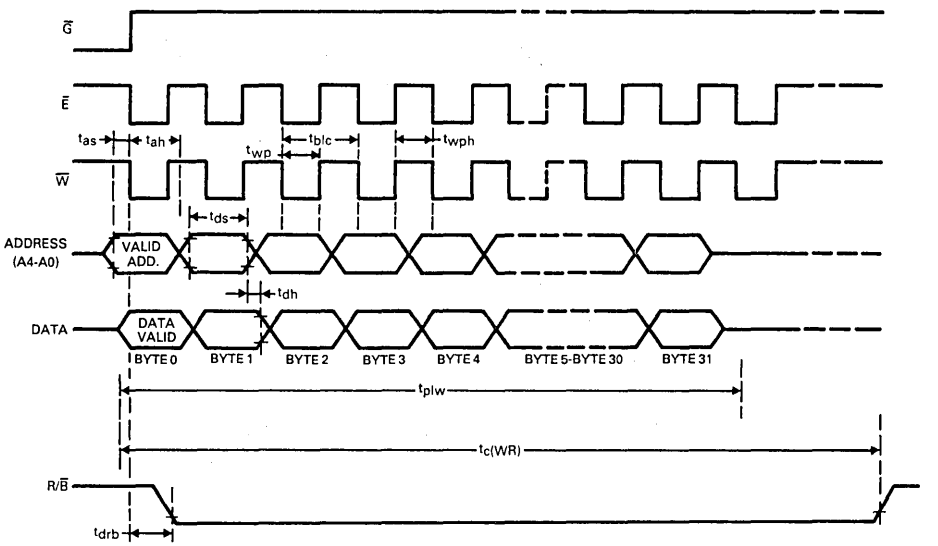
$\overline{W}$ controlled byte write cycle



page mode write

PARAMETER		TMS28C64-25			TMS28C64-35			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(WR)}$	Write cycle time		10	15		10	15	ms
t_{as}	Address setup time	10			15			ns
t_{ah}	Address hold time	100			100			ns
t_{ds}	Data setup time	100			150			ns
t_{dh}	Data hold time	30			30			ns
t_{wp}	Write pulse duration	150		500	150		500	ns
t_{blc}	Byte load cycle	3			3			μs
t_{plw}	Page load duration	150			150			μs
t_{wph}	Write pulse duration high	2.5			2.5			μs

NOTE 2: For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 (reference page 6).



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OCTOBER 1984 – REVISED MAY 1988

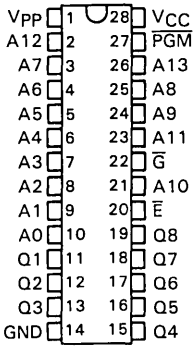
This Data Sheet is Applicable to All TMS27C128s and TMS27PC128s Symbolized with Code "A" as Described on Page 11.

- **Organization . . . 16K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible with Existing 128K MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**

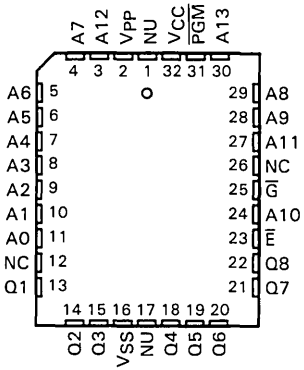
V_{CC} ±5%	V_{CC} ±10%	
'27C128-100		100 ns
'27C128-120	'27C128-12	120 ns
'27C/PC128-1	'27C/PC128-15	150 ns
'27C/PC128-2	'27C/PC128-20	200 ns
'27C/PC128	'27C/PC128-25	250 ns

- **Power Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming or Fast Programming Algorithms**
- **3-State Output Buffers**
- **400 mV Guaranteed DC Noise Immunity with Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.25 V)**
  - **Active . . . 158 mW Worst Case**
  - **Standby . . . 1.4 mW Worst Case (CMOS Input Levels)**
- **PEP4 Version Available with 168 Hour Burn-in, and also Guaranteed Operating Temperature Ranges**
- **128K EPROM Available with MIL-STD-883C Class B High Reliability Processing (SMJ27C128)**

J AND N PACKAGES
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A13	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
NU	Make No External Connection
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12-13 V Programming Power Supply

description

The TMS27C128 series are 131,072-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC128 series are 131,072-bit, one-time, electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs

(including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C128 and the TMS27PC128 are pin compatible with 28-pin 128K MOS ROMs, PROMs, and EPROMs.

The TMS27C128 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers and is rated for operation from 0 °C to 70 °C. The TMS27C128 is also offered with two guaranteed temperature ranges of 0 °C to 70 °C and −40 °C to 85 °C (TMS27C128-_ _JL and TMS27C128-_ _JE, respectively). The TMS27C128 is also offered with 168 hour burn-in on both temperature ranges (TMS27C128-_ _JL4 and TMS27C128-_ _JE4, respectively). (See table below.)

The TMS27PC128 PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC128 is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). The TMS27PC128 is guaranteed for operation from 0 °C to 70 °C.

All package styles conform to JEDEC standards.

EPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0 °C TO 70 °C	−40 °C TO 85 °C	0 °C TO 70 °C	−40 °C TO 85 °C
TMS27C128-XXX	JL	JE	JL4	JE4

These EPROMs and PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 12-13 V supply is needed for programming. All programming signals are TTL level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. Fast programming uses a V_{PP} of 12.5 V and a V_{CC} of 6.0 V for a nominal programming time of two minutes. SNAP! Pulse programming uses a V_{PP} of 13.0 V and a V_{CC} of 6.5 V for a nominal programming time of two seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation listed in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V for Fast or 13.0 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X	V_{IH}	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	CODE	
							MFG	DEVICE
							97	83

†X Can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C128s or TMS27PC128s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 through Q8.

latchup immunity

Latchup immunity on the TMS27C128 and TMS27PC128 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001; *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family,"* available through TI Field Sales Offices.

power down

Active I_{CC} current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C128)

Before programming, the TMS27C128 EPROM is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). EPROM erasure before programming is necessary to assure that all bits are in the logic 1 (high) state. Logic 0s are programmed into the desired locations. A programmed logic 0 can be erased only by ultraviolet light. The recommended minimum ultraviolet light exposure dose (UV intensity $\times$ exposure time) is 15 watt-seconds per square centimeter. A typical 12-milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C128, the window should be covered with an opaque label.

initializing (TMS27PC128)

The one-time programmable TMS27PC128 PROM is provided with all bits in the logic 1 state, then logic 0s are programmed into the desired locations. Logic 0s programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 128K EPROM and PROM can be programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which can reduce programming time to a nominal of two seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13.0 V, V_{CC} = 6.5 V, $\overline{G} = V_{IH}$, and $\overline{E} = V_{IL}$. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 5$ V.

Fast programming

The 128K EPROM and PROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming, data is presented in parallel (eight bits) on pins Q1 through Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed. The programming mode is achieved when $V_{PP} = 12.5\,V$, $V_{CC} = 6.0\,V$, $\overline{G} = V_{IH}$, and $\overline{E} = V_{IL}$. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Fast programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at $V_{CC} = 6.0\,V$ and $V_{PP} = 12.5\,V$. When the full Fast programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 5\,V$.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pin.

program verify

Programmed bits may be verified with $V_{PP} = 12.5\,V$ when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to $12\,V \pm 0.5\,V$. Two identifier bytes are accessed by A0 (pin 10); i.e., $A0 = V_{IL}$ accesses the manufacturer code, which is output on Q1-Q8; $A0 = V_{IH}$ accesses the device code, which is output on Q1-Q8. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for these devices is 97, and the device code is 83.

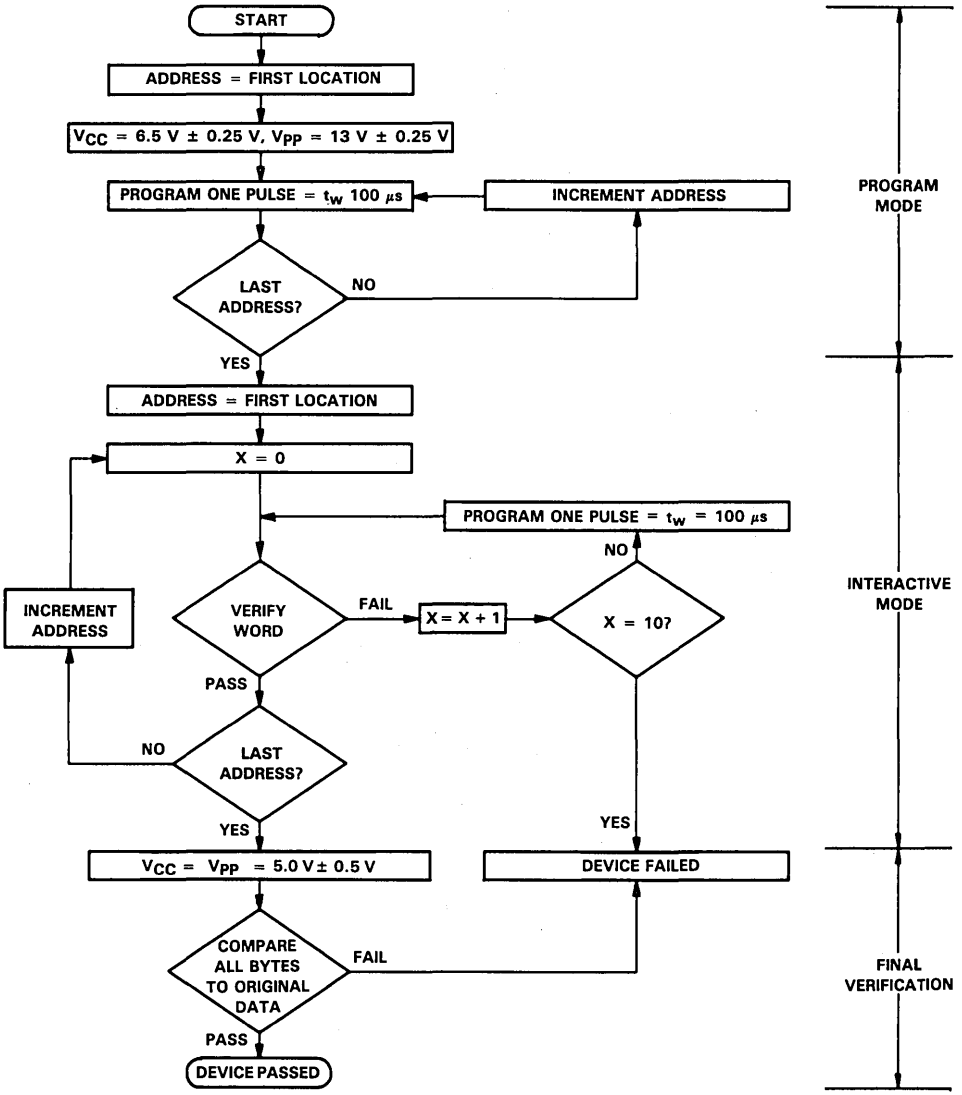


FIGURE 1. SNAP! PULSE PROGRAMMING FLOWCHART

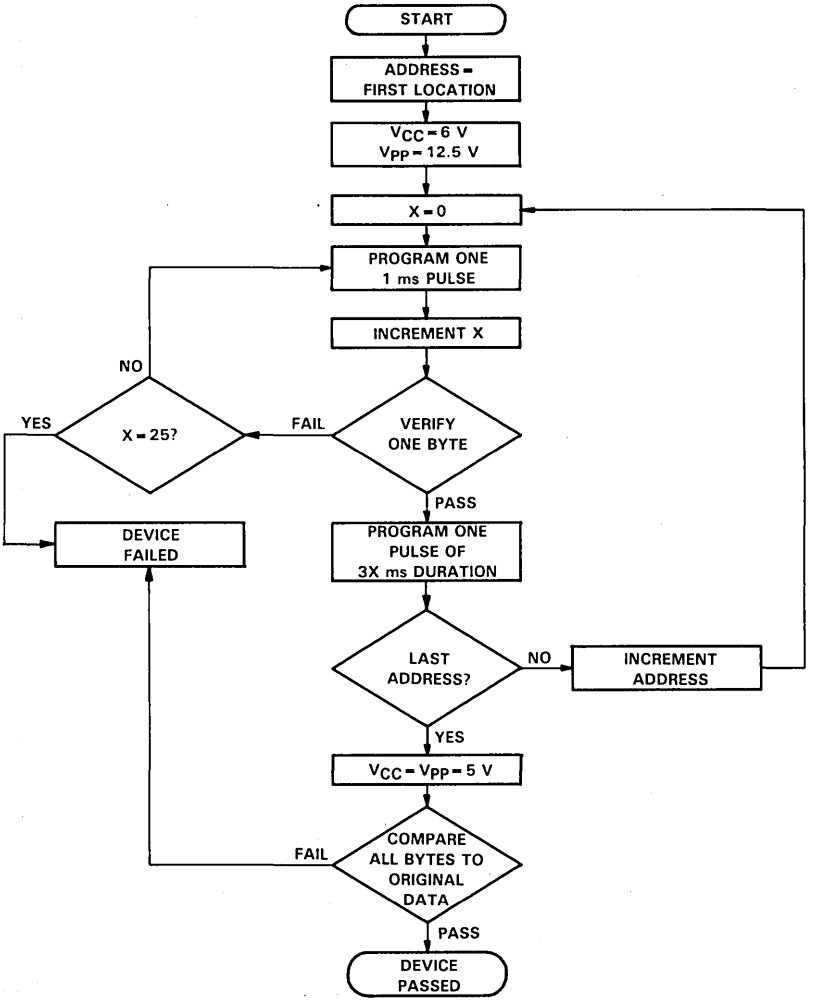
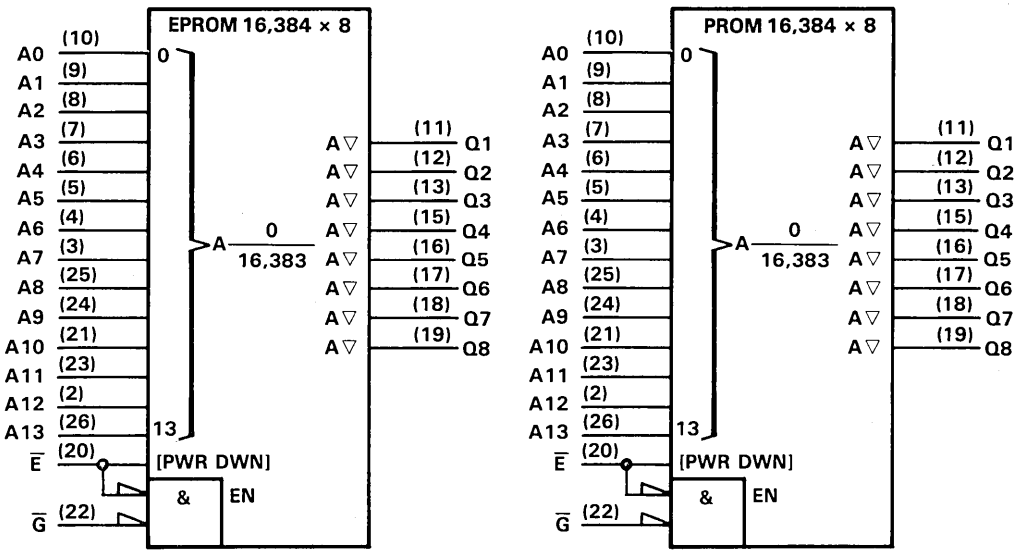


FIGURE 2. FAST PROGRAMMING FLOWCHART

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 . . . . . −0.6 V to 6.5 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C128-_ _JL and JL4; '27PC128-_ _NL and FML) . . . . . 0°C to 70°C
Operating free-air temperature range ('27C128-_ _JE and JE4) . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			'27C128-100, '27C128-120, '27C/PC128-1, '27C/PC128-2, '27C/PC128			'27C128-12, '27C/PC128-15, '27C/PC128-20, '27C/PC128-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage	Read mode (see Note 2)	4.75	5	5.25	4.5	5	5.5	V
		Fast programming algorithm	5.75	6	6.25	5.75	6	6.25	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)	$V_{CC}-0.6$		$V_{CC}+0.6$	$V_{CC}-0.6$		$V_{CC}+0.6$	V
		Fast programming algorithm	12	12.5	13	12	12.5	13	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	12.75	13	13.25	V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		0.2	−0.5		0.2	V
T_A	Operating free-air temperature (See table, page 2)		(See table, page 2)			(See table, page 2)			°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = -2.5$ mA	3.5			V
			$I_{OH} = -20\,\mu$A	$V_{CC}-0.1$			V
V_{OL}	Low-level output voltage		$I_{OL} = 2.1$ mA			0.4	V
			$I_{OL} = 20\,\mu$A			0.1	V
I_I	Input current (leakage)		$V_I = 0$ V to 5.5 V			±1	μA
I_O	Output current (leakage)		$V_O = 0$ V to V_{CC}			±1	μA
I_{PP1}	V_{PP} supply current		$V_{PP} = V_{CC} = 5.5$ V		1	10	mA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP} = 13$ V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$		250	500	μA
		CMOS-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$		100	250	μA
I_{CC2}	V_{CC} supply current (active)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		15	30	mA

†Typical values are at $T_A = 25$°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	$V_I = 0$ V, f = 1 MHz		6	10	pF
C_o	Output capacitance	$V_O = 0$ V, f = 1 MHz		10	14	pF

†Typical values are at $T_A = 25$°C and nominal voltages.
‡Capacitance measurements are made on sample basis only.

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switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C128-100		'27C128-120 '27C128-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pf, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		100		120	ns
$t_{a(E)}$	Access time from chip enable			100		120	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		55	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	40	0	45	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C/PC128-1 '27C/PC128-15		'27C/PC128-2 '27C/PC128-20		'27C/PC128 '27C/PC128-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pf, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		150		200		250	ns
$t_{a(E)}$	Access time from chip enable			150		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6 V and V_{PP} = 12.5 (Fast) or V_{CC} = 6.50 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.50 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C, (see Note 4)

			MIN	TYP	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	μs
$t_{w(FPGM)}$	Final pulse duration	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			μs
$t_{su(E)}$	$\overline{E}$ setup time		2			μs
$t_{su(G)}$	$\overline{G}$ setup time		2			μs
$t_{su(D)}$	Data setup time		2			μs
$t_{su(VPP)}$	V_{PP} setup time		2			μs
$t_{su(VCC)}$	V_{CC} setup time		2			μs
$t_{h(A)}$	Address hold time		0			μs
$t_{h(D)}$	Data hold time		2			μs

NOTES: 4. For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0. (Reference page 10).
5. Common test conditions apply for t_{dis} except during programming.

PARAMETER MEASUREMENT INFORMATION

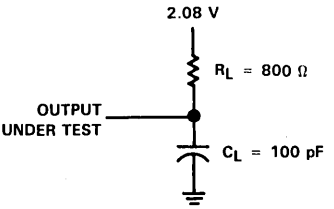
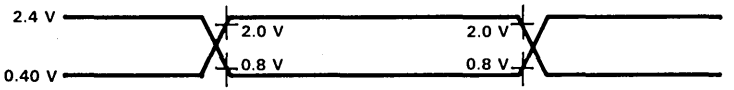


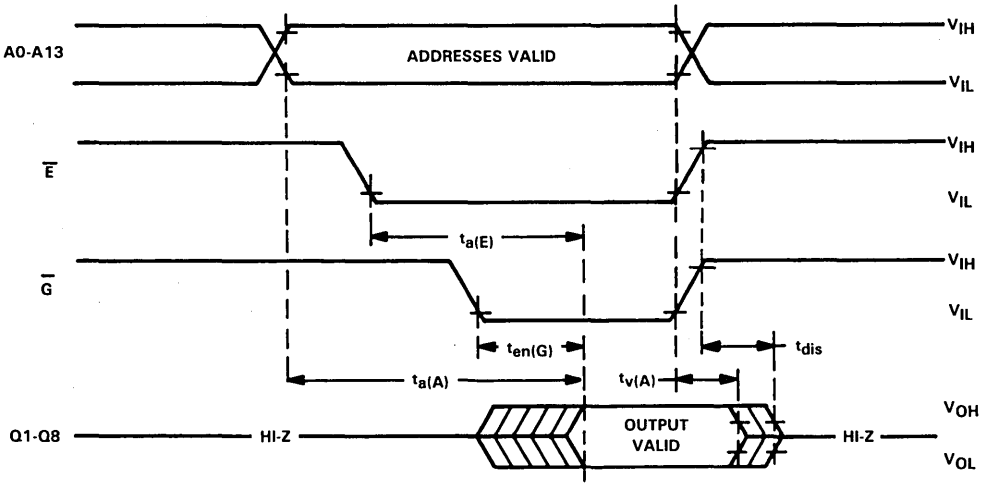
FIGURE 3. OUTPUT LOAD CIRCUIT

AC testing input/output wave forms

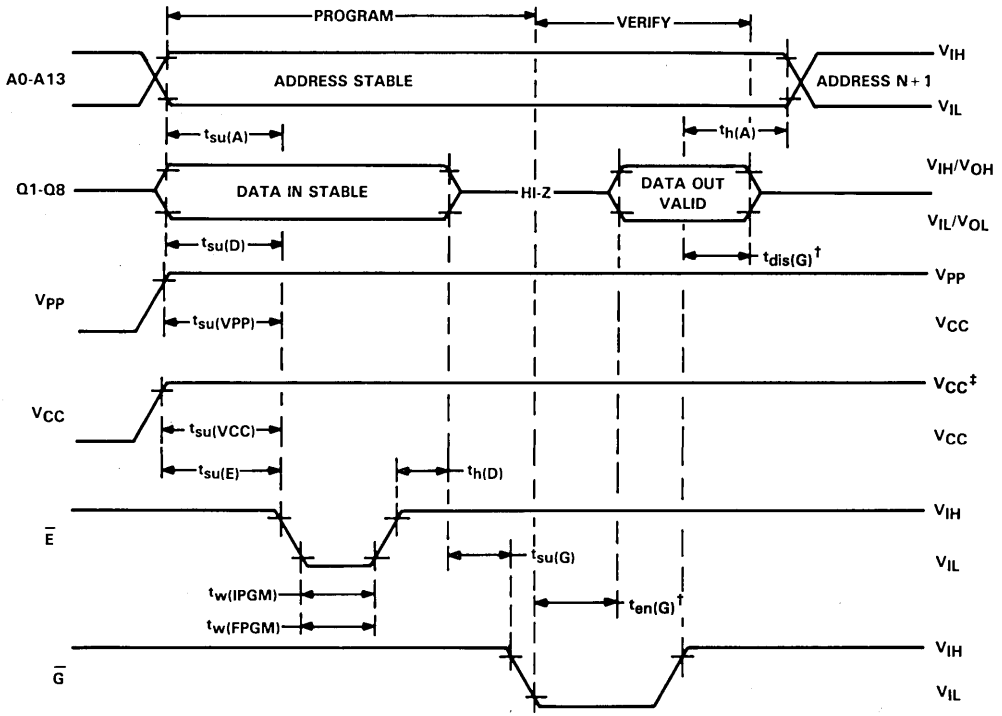


A.C. testing inputs are driven at 2.4 V for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 for both inputs and outputs.

read cycle timing



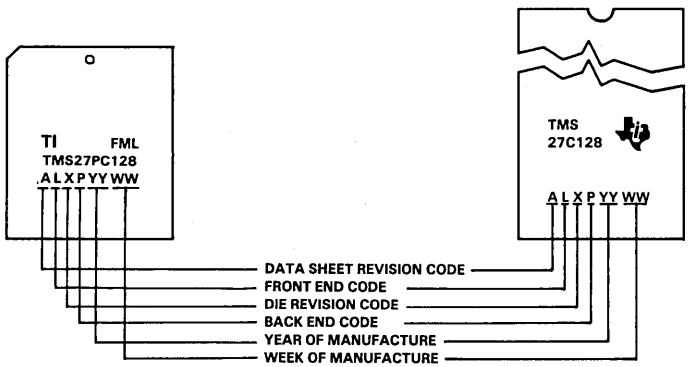
program cycle timing



†$t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡12.5 V V_{PP} and 6.0 V V_{CC} for Fast programming 13.0 V V_{PP} and 6.50 V V_{CC} for SNAP! Pulse programming.

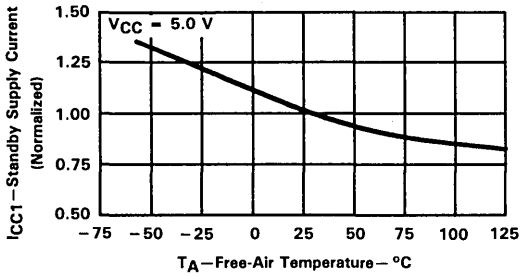
device symbolization

This data sheet is applicable to all TI TMS27C128 CMOS EPROMs and TMS27PC128 PROMs with the code "A" as shown below:

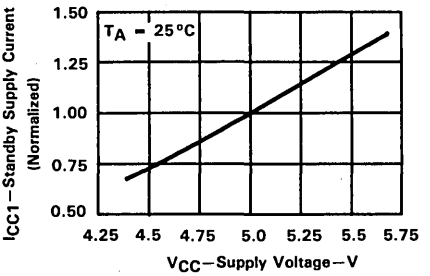


TYPICAL TMS27C/PC128 CHARACTERISTICS

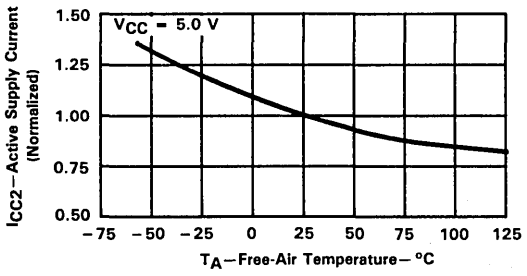
STANDBY SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



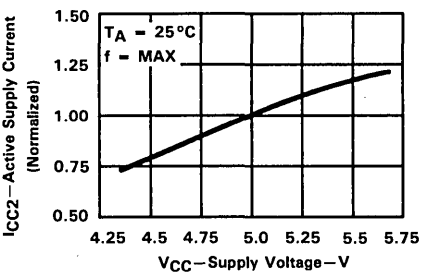
STANDBY SUPPLY CURRENT
vs
SUPPLY VOLTAGE



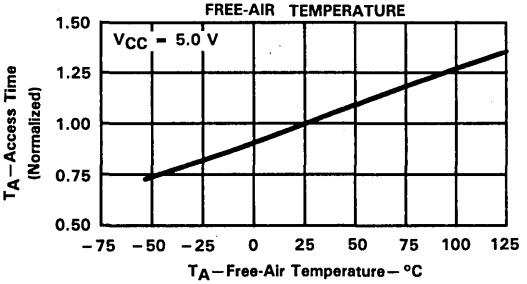
ACTIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



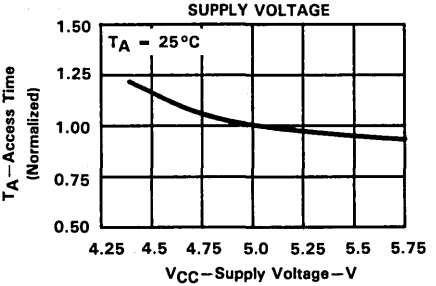
ACTIVE SUPPLY CURRENT
vs
SUPPLY VOLTAGE



ACCESS TIME
vs
FREE-AIR TEMPERATURE



ACCESS TIME
vs
SUPPLY VOLTAGE



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

TMS27C256 262,144-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC256 262,144-BIT PROGRAMMABLE READ-ONLY MEMORY

SEPTEMBER 1984—REVISED MARCH 1988

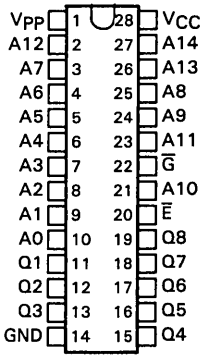
This Data Sheet is Applicable to All TMS27C256s and TMS27PC256s Symbolized with Code "A" as Described on Page 12.

- Organization . . . 32K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 256K MOS ROMs, PROMS, and EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Times

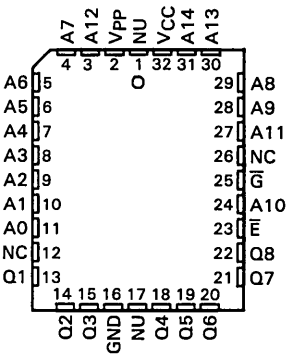
V_{CC} ±5%	V_{CC} ±10%	
'27C256-120	'27C256-12	120 ns
'27C/PC256-150	'27C/PC256-15	150 ns
'27C/PC256-1	'27C/PC256-17	170 ns
'27C/PC256-2	'27C/PC256-20	200 ns
'27C/PC256	'27C/PC256-25	250 ns

- Power Saving CMOS Technology
- Very High Speed SNAP! Pulse Programming or Fast Programming Algorithms
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Latchup Immunity of 250 mA on All Input and Output Lines
- Low Power Dissipation (V_{CC} = 5.25 V)
  - Active . . . 158 mW Worst Case
  - Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)
- PEP4 Version Available with 168 Hour Burn-in, and also Guaranteed Operating Temperature Ranges
- 256K EPROM Available with MIL-STD-883C Class B High Reliability Processing (SMJ27C256)

J AND N PACKAGES
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

The TMS27C256 series are 262,144-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC256 series are 262,144-bit, one-time, electrically programmable read-only memories.

These devices are fabricated using power saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can

PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
NU	Make No External Connecction
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12-13 V Programming Power Supply

be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C256 and the TMS27PC256 are pin compatible with 28-pin 256K MOS ROMs, PROMs, and EPROMs.

The TMS27C256 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C256 is offered with two guaranteed temperature ranges of 0°C to 70°C and −40°C to 85°C (TMS27C256-_ _JL and TMS27C256-_ _JE, respectively). The TMS27C256 is also offered with 168-hour burn-in on both temperature ranges (TMS27C256-_ _JL4 and TMS27C256-_ _JE4, respectively); see table below.

The TMS27PC256 PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC256 is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). The TMS27PC256 is guaranteed for operation from 0°C to 70°C (NL or FML suffix).

All package styles conform to JEDEC standards.

EPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 ± 8 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C to 70°C	−40°C TO 85°C	0°C TO 70°C	−40°C TO 85°C
TMS27C256-XXX	JL	JE	JL4	JE4

These EPROMs and PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 12-13 V supply is needed for programming. All programming signals are TTL level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. Fast programming uses a V_{PP} of 12.5 V and a V_{CC} of 6.0 V for a nominal programming time of two minutes. SNAP! Pulse programming uses a V_{PP} of 13.0 V and a V_{CC} of 6.5 V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation listed in the following table. Read mode requires a single 5 V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V for Fast, or 13.0 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	CODE	
							MFG	DEVICE
							97	04

†X can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C256s or TMS27PC256s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8.

latchup immunity

Latchup immunity on the TMS27C256 and TMS27PC256 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001; *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family."*

power down

Active I_{CC} current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C256)

Before programming, the TMS27C256 EPROM is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is 15 watt-seconds per square centimeter. A typical 12-milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C256, the window should be covered with an opaque label. After erasure (all bits in logic 1 state), logic 0s are programmed into the desired locations. A programmed zero can be erased only by ultraviolet light.

initializing (TMS27PC256)

The one-time programmable TMS27PC256 PROM is provided with all bits in logic 1 state, then logic 0s are programmed into the desired locations. Logic 0s programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 256K EPROM and PROM can be programmed using the TI SNAP! Pulse programming algorithm as illustrated by the flowchart of Figure 1, which can reduce programming time to a nominal of 4 seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13.0 V, V_{CC} = 6.5 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

fast programming

The 256K EPROM and PROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming, data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{E}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, V_{CC} = 6.0 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Fast programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6.0 V and V_{PP} = 12.5 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL} and $\overline{E}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code which is output on Q1-Q8; A0 = V_{IH} accesses the device code which is output on Q1-Q8. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for these devices is 97, and the device code is 04.

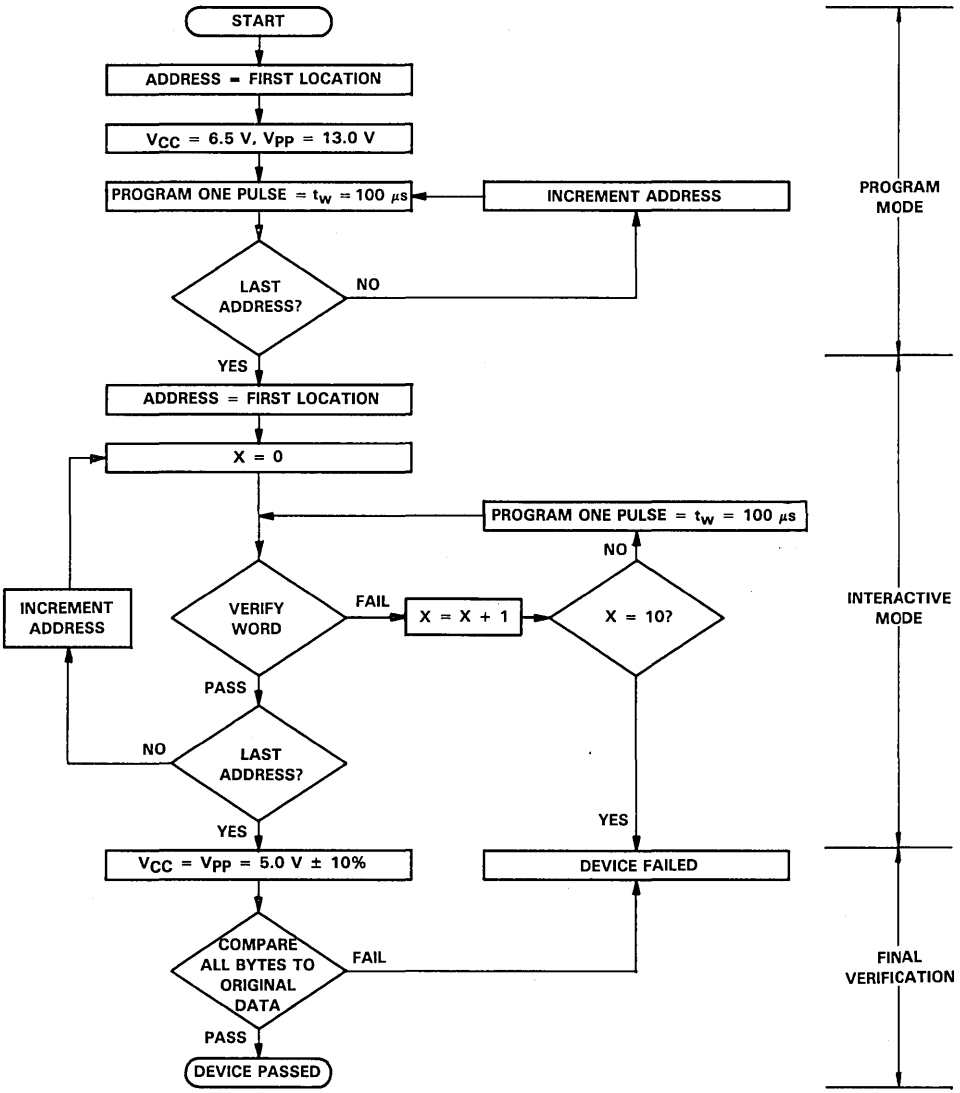


FIGURE 1. SNAP! PULSE PROGRAMMING FLOWCHART

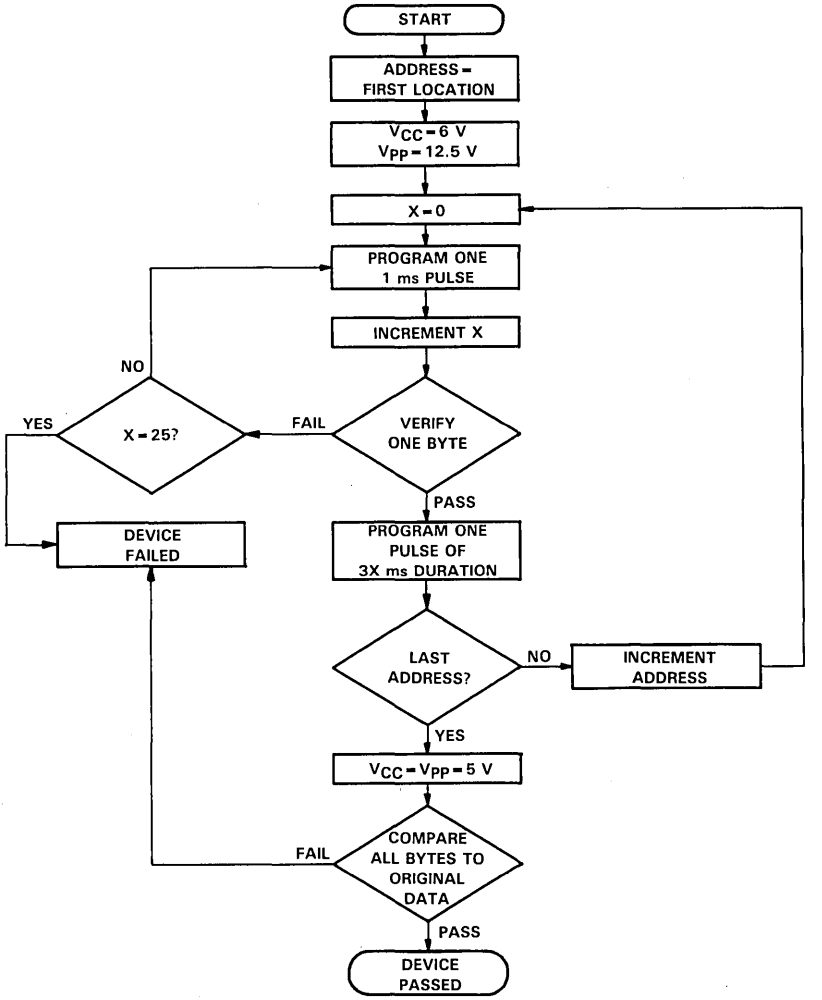


FIGURE 2. FAST PROGRAMMING FLOWCHART

TEXAS INSTRUMENTS
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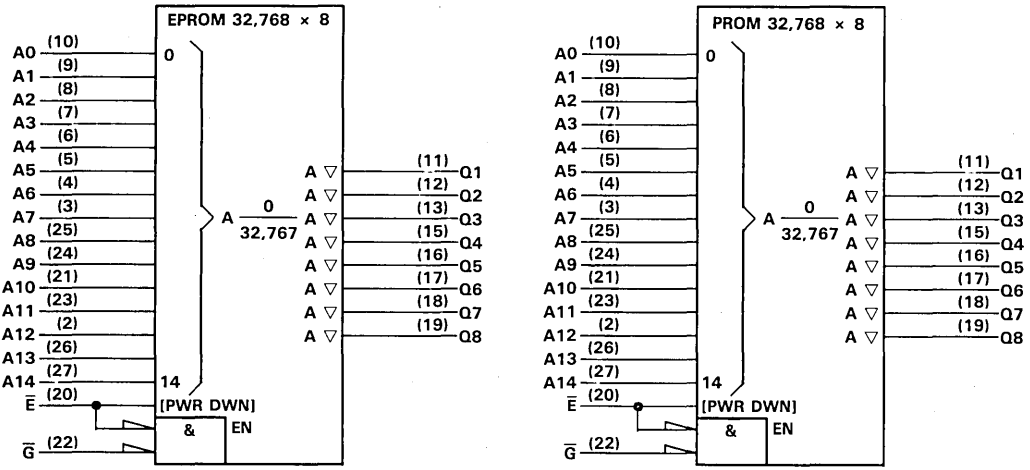
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
J and N packages illustrated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 . . . . . −0.6 V to 6.5 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C256-_ _JL and JL4; '27PC256-_ _NL and FML) . . . . . 0°C to 70°C
Operating free-air temperature range ('27C256-_ _JE and JE4) . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			'27C256-120, '27C256-150, '27PC256-150, '27C256-1, '27PC256-1, '27C256-2, '27PC256-2, '27C256, '27PC256			'27C256-12, '27C256-15, '27PC256-15, '27C256-17, '27PC256-17, '27C256-20, '27PC256-20, '27C256-25, '27PC256-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	Read mode (see Note 2)		4.75	5	5.25	4.5	5	5.5	V
	Fast programming algorithm		5.75	6	6.25	5.75	6	6.25	V
	SNAP! Pulse programming algorithm		6.25	6.5	6.75	6.25	6.5	6.75	V
V_{PP} Supply voltage	Read mode (see Note 3)		$V_{CC}-0.6$		$V_{CC}+0.6$	$V_{CC}-0.6$		$V_{CC}+0.6$	V
	Fast programming algorithm		12	12.5	13	12	12.5	13	V
	SNAP! Pulse programming algorithm		12.75	13.0	13.25	12.75	13.0	13.25	V
V_{IH} High-level input voltage		TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	V
V_{IL} Low-level input voltage		TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		0.2	−0.5		0.2	V
T_A Operating free-air temperature (See table, page 2)			(See table, page 2)			(See table, page 2)			°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC}+I_{PP}$.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −2.5 mA	3.5			V
			I_{OH} = −20 μA	$V_{CC}-0.1$			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
			I_{OL} = 20 μA			0.1	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±1	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		1	10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		250	500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	250	μA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		15	30	mA

†Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	10	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		10	14	pF

†Typical values are at T_A = 25°C and nominal voltages
‡Capacitance measurements are made on sample basis only.

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switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C256-120 '27C256-12		'27C256-150 '27PC256-150 '27C256-15 '27PC256-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		120		150	ns
$t_{a(E)}$	Access time from chip enable			120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		75	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	45	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C256-1 '27PC256-1 '27C256-17 '27PC256-17		'27C256-2 '27PC256-2 '27C256-20 '27PC256-20		'27C256 '27PC256 '27C256-25 '27PC256-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		170		200		250	ns
$t_{a(E)}$	Access time from chip enable			170		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.50 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

NOTES: 4. For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0. (Reference page 11.)
5. Common test conditions apply for the t_{dis} except during programming.

recommended timing requirements for programming, V_{CC} = 6 V, and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.5 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 4)

			MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	μs
$t_{w(FPGM)}$	Final pulse duration	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			μs
$t_{su(G)}$	$\overline{G}$ setup time		2			μs
$t_{su(E)}$	$\overline{E}$ setup time		2			μs
$t_{su(D)}$	Data setup time		2			μs
$t_{su(VPP)}$	V_{PP} setup time		2			μs
$t_{su(VCC)}$	V_{CC} setup time		2			μs
$t_{h(A)}$	Address hold time		0			μs
$t_{h(D)}$	Data hold time		2			μs

NOTES: 4. For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0. (Reference page 11.)

PARAMETER MEASUREMENT INFORMATION

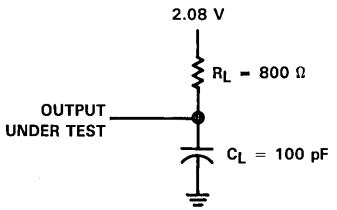
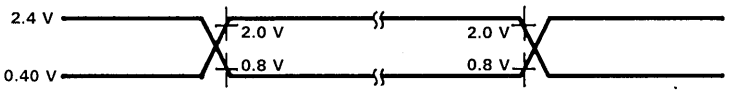


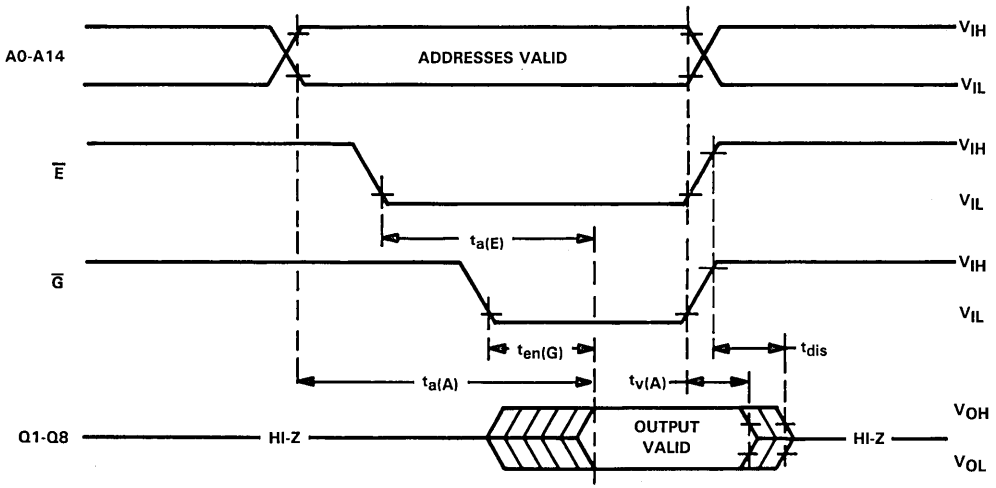
FIGURE 3. OUTPUT LOAD CIRCUIT

AC testing input/output wave forms

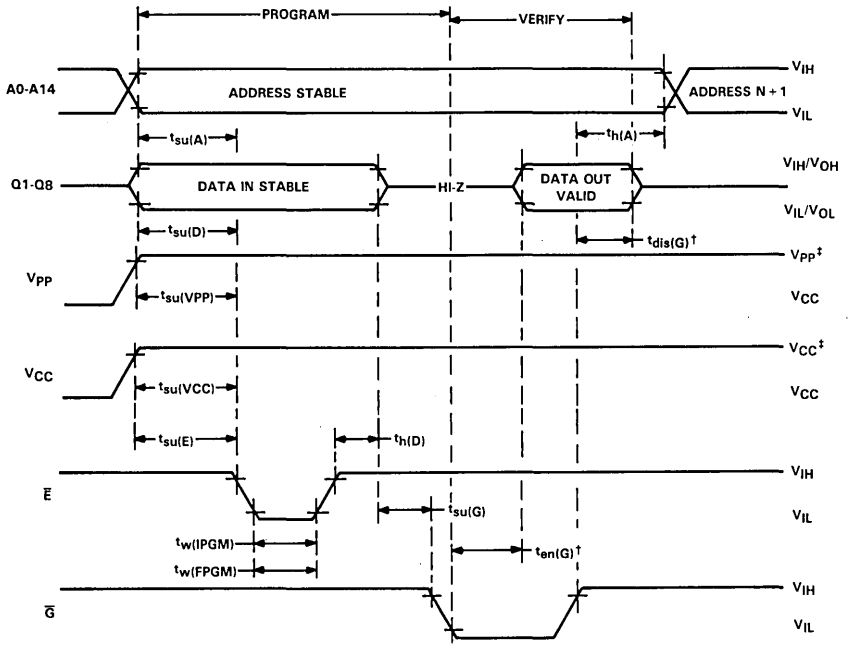


A.C. testing inputs are driven at 2.4 V for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 for both inputs and outputs.

read cycle timing



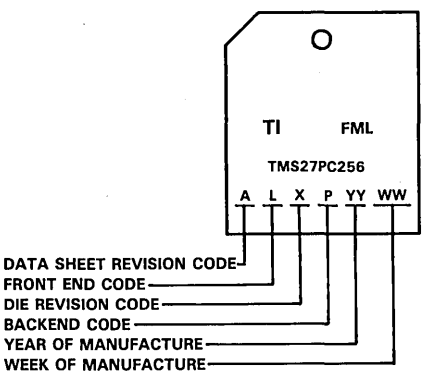
program cycle timing

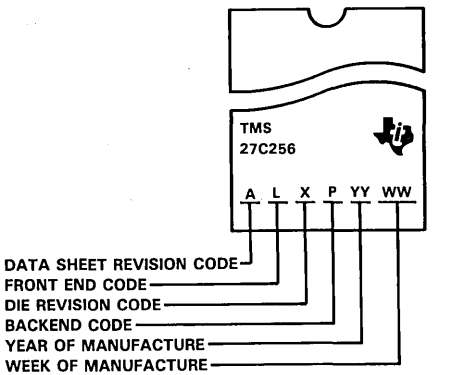


† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 12.5 V V_{PP} and 6.0 V V_{CC} for Fast programming; 13.0 V V_{PP} and 6.5 V V_{CC} for SNAP! Pulse programming.

device symbolization

This data sheet is applicable to all TI TMS27C256 CMOS EPROMs and TMS27PC256 PROMs with the data sheet revision code "A" as shown below:





TEXAS INSTRUMENTS
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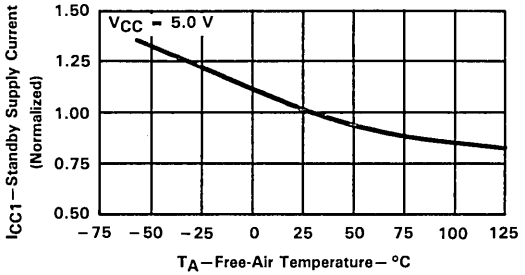
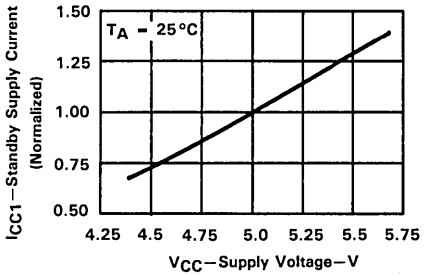
TYPICAL TMS27C/PC256 CHARACTERISTICS

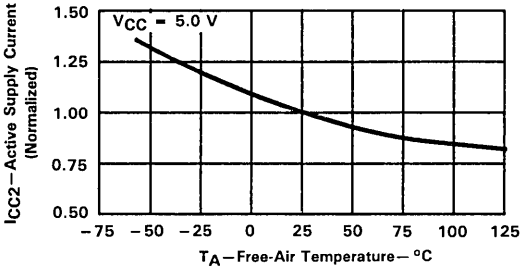
STANDBY SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



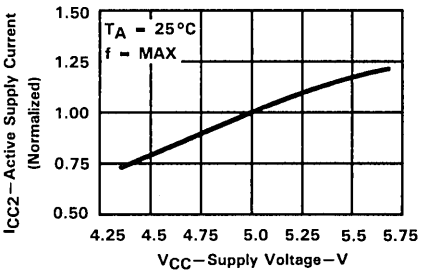
STANDBY SUPPLY CURRENT
vs
SUPPLY VOLTAGE



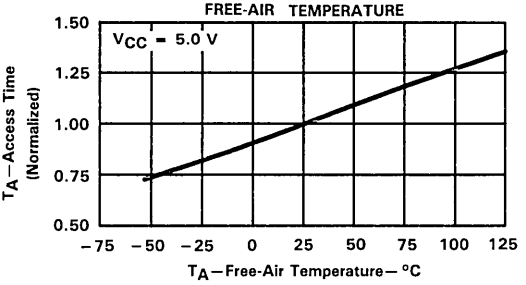
ACTIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



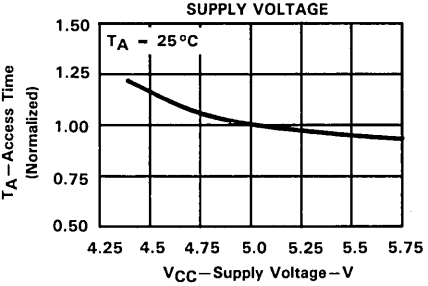
ACTIVE SUPPLY CURRENT
vs
SUPPLY VOLTAGE



ACCESS TIME
vs
FREE-AIR TEMPERATURE



ACCESS TIME
vs
SUPPLY VOLTAGE



TMS27C512 524,288-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC512 524,288-BIT PROGRAMMABLE READ-ONLY MEMORY

NOVEMBER 1985 – REVISED APRIL 1988

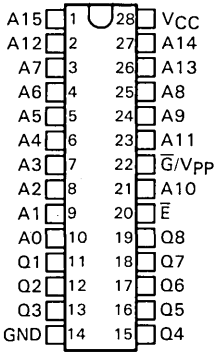
This Data Sheet is Applicable to All TMS27C512s and TMS27PC512s Symbolized with Code "A" as Described on Page 12.

- Organization . . . 64K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 512K MOS ROMs, PROMs, and EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

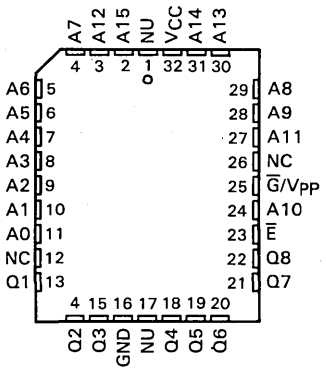
V_{CC} ±5%	V_{CC} ±10%	
'27C512-1	'27C512-17	170 ns
'27C/PC512-2	'27C/PC512-20	200 ns
'27C/PC512	'27C/PC512-25	250 ns
'27C/PC512-3	'27C/PC512-30	300 ns

- Power Saving CMOS Technology
- Very High-Speed SNAP! Pulse Programming or Fast Programming Algorithms
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Latchup Immunity of 250 mA on All Input and Output Lines
- Low Power Dissipation (V_{CC} = 5.25 V)
  - Active . . . 158 mW Worst Case
  - Standby . . . 1.4 mW Worst Case (CMOS Input Levels)
- PEP4 Version Available with 168 Hour Burn-in, and also Guaranteed Operating Temperature Ranges
- 512K EPROM Available with MIL-STD-883C Class B High Reliability Processing (SMJ27C512)

J AND N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

The TMS27C512 series are 524,288-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC512 series are 524, 288-bit, one-time, electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by

PIN NOMENCLATURE	
A0-A15	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}/V_{PP}$	12-13 V Programming Power Supply
GND	Ground
NC	No Connection
NU	Make No External Connection
Q1-Q8	Outputs
V_{CC}	5-V Power Supply

Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C512 and the TMS27PC512 are pin compatible with 28-pin 512K MOS ROMs, PROMs, and EPROMs.

The TMS27C512 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C512 is available with two guaranteed temperature ranges of 0°C to 70°C and −40°C to 85°C (TMS27C512-_ _JL and TMS27C512-_ _JE, respectively). The TMS27C512 is also offered with 168 hour burn-in on both temperature ranges (TMS27C512-_ _JL4 and TMS27C512-_ _JE4, respectively). (See table below.)

The TMS27PC512 PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC512 is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). The TMS27PC512 is guaranteed for operation from 0°C to 70°C.

All package styles conform to JEDEC standards.

EPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C TO 70°C	−40°C TO 85°C	0°C TO 70°	−40°C TO 85°C
TMS27C512-XXX	JL	JE	JL4	JE4

These EPROMs and PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 12-13 V supply is needed for programming. All programming signals are TTL level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. Fast programming uses a V_{PP} of 12.5 V and a V_{CC} of 6.0 V for a nominal programming time of two minutes. SNAP! Pulse programming uses a V_{PP} of 13.0 V and a V_{CC} of 6.5 V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation listed in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V for Fast or 13.0 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}/V_{PP}$	V_{IL}	V_{IH}	X†	V_{PP}	V_{IL}	V_{PP}	V_{IL}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	CODE	
							MFG	DEVICE
							97	85

†X Can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

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read/output disable

When outputs of two or more TMS27C512s or TMS27PC512s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}/V_{PP}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 through Q8.

latchup immunity

Latchup immunity on the TMS27C512 and TMS27PC512 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001; *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family,"* available through TI Field Sales Offices.

power down

Active I_{CC} current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C512)

Before programming, the TMS27C512 EPROM is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). EPROM erasure before programming is necessary to assure that all bits are in the logic 1 (high) state. Logic 0s are programmed into the desired locations. A programmed logic 0 can be erased only by ultraviolet light. The recommended minimum ultraviolet light exposure dose (UV intensity × exposure time) is 15 watt-seconds per square centimeter. A typical 12-milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C512, the window should be covered with an opaque label.

initializing (TMS27PC512)

The one-time programmable TMS27PC512 PROM is provided with all bits in the logic 1 state, then logic 0s are programmed into the desired locations. Logic 0s programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 512K EPROM and PROM can be programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which can reduce programming time to a nominal of four seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when $\overline{G}/V_{PP}$ = 13.0 V, V_{CC} = 6.5 V, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified when V_{CC} = 5 V, $\overline{G}/V_{PP}$ = V_{IL}, and $\overline{E}$ = V_{IL}.

Fast programming

The 512K EPROM and PROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming, data is presented in parallel (eight bits) on pins Q1 through Q8. Once addresses and data are stable, $\overline{E}$ is pulsed. The programming mode is achieved when $\overline{G}/V_{PP}$ = 12.5 V, V_{CC} = 6.0 V, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Fast programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6.0 V and $\overline{G}/V_{PP}$ = 12.5 V. When the full Fast programming routine is complete, all bits are verified when V_{CC} = 5 V and $\overline{G}/V_{PP}$ = V_{IL}.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified when $\overline{G}/V_{PP}$ and $\overline{E}$ = V_{IL}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code, which is output on Q1-Q8; A0 = V_{IH} accesses the device code, which is output on Q1-Q8. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for these devices is 97, and the device code is 85.

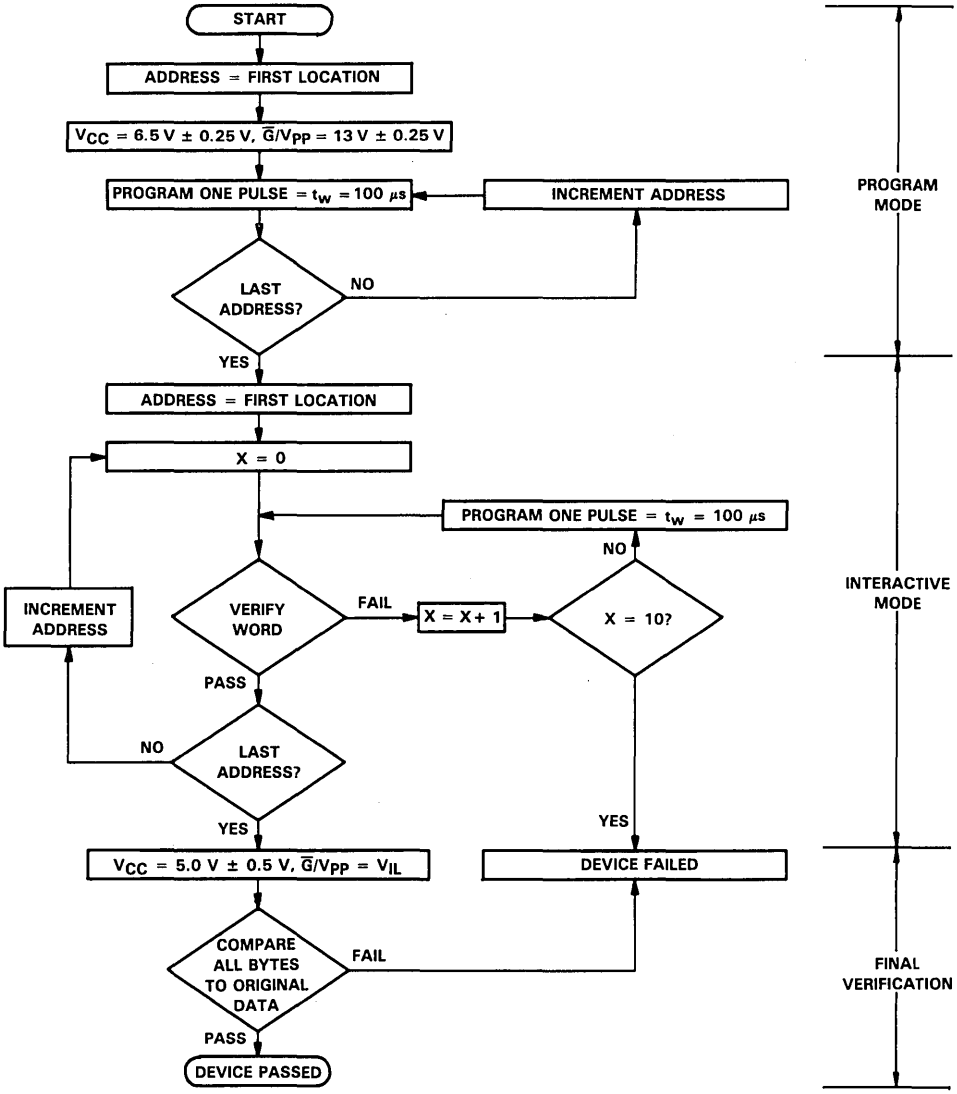


FIGURE 1. SNAP! PULSE PROGRAMMING FLOWCHART

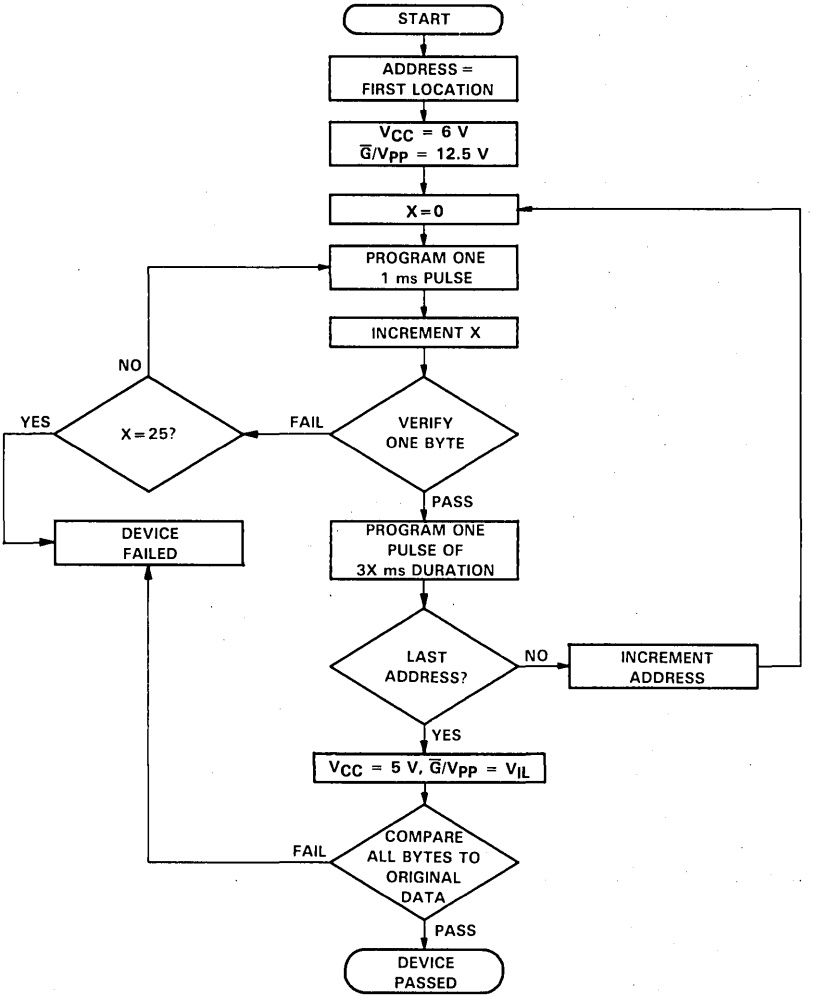
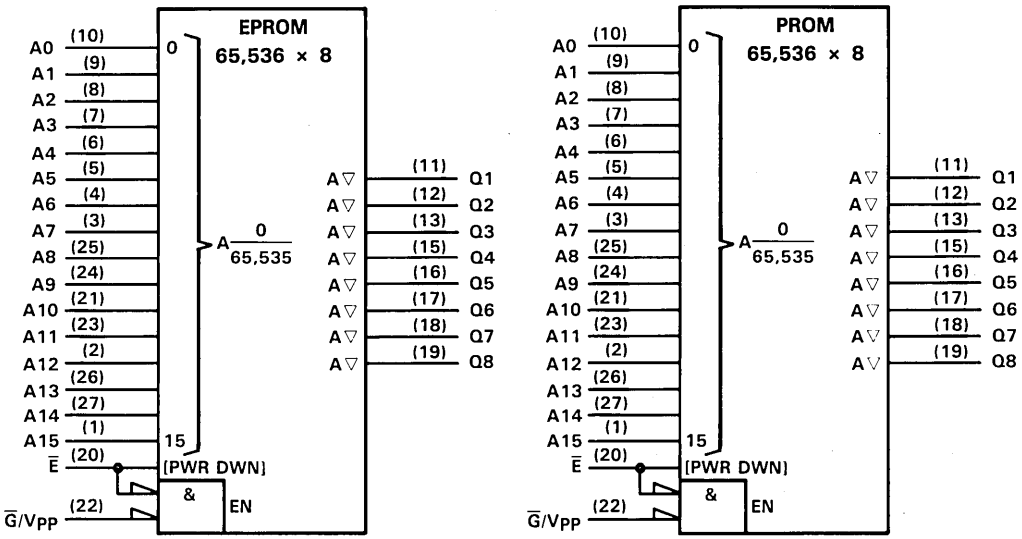


FIGURE 2. FAST PROGRAMMING FLOWCHART

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 . . . . . −0.6 V to 6.5 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C512-_ _JL and JL4; '27PC512-_ _NL and FML) . . . . . 0°C to 70°C
Operating free-air temperature range ('27C512-_ _JE and JE4) . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			'27C512-1 '27C/PC512-2 '27C/PC512 '27C/PC512-3			'27C512-17 '27C/PC512-20 '27C/PC512-25 '27C/PC512-30			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.75	5	5.25	4.5	5	5.5	V
		Fast programming algorithm	5.75	6	6.25	5.75	6	6.25	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	6.25	6.5	6.75	V
$\overline{G}/V_{PP}$	Supply voltage	Fast programming algorithm	12	12.5	13	12	12.5	13	V
		SNAP! Pulse programming algorithm	12.75	13.0	13.25	12.75	13.0	13.25	V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		0.2	−0.5		0.2	V
T_A	Operating free-air temperature (See table, page 2)		(See table, page 2)			(See table, page 2)			°C

NOTE 2: V_{CC} must be applied before or at the same time as $\overline{G}/V_{PP}$ and removed after or at the same time as $\overline{G}/V_{PP}$. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −2.5 mA	3.5			V
			I_{OH} = −20 μA	$V_{CC}-0.1$			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
			I_{OL} = 20 μA			0.1	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±1	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±1	μA
I_{PP}	$\overline{G}/V_{PP}$ supply current (during program pulse)		$\overline{G}/V_{PP}$ = 13 V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		250	500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	250	μA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		15	30	mA

†Typical values are at T_A = 25 °C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	10	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		10	14	pF
$C_{G/VPP}$	$\overline{G}/V_{PP}$ input capacitance	$\overline{G}/V_{PP}$ = 0 V, f = 1 MHz		20	25	pF

†Typical values are at T_A = 25 °C and nominal voltages.
‡Capacitance measurements are made on sample basis only.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C512-1 '27C512-17		'27C/PC512-2 '27C/PC512-20		'27C/PC512 '27C/PC512-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pf, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		170		200		250	ns
$t_{a(E)}$	Access time from chip enable			170		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}/V_{PP}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}/V_{PP}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}/V_{PP}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C/PC512-3 '27C/PC512-30		UNIT
			MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pf, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		300	ns
$t_{a(E)}$	Access time from chip enable			300	ns
$t_{en(G)}$	Output enable time from $\overline{G}/V_{PP}$			120	ns
t_{dis}	Output disable time from $\overline{G}/V_{PP}$ or $\overline{E}$, whichever occurs first†		0	105	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}/V_{PP}$, whichever occurs first†		0		ns

†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6 V and $\overline{G}/V_{PP}$ = 12.5 V (Fast) or V_{CC} = 6.50 V and $\overline{G}/V_{PP}$ = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 3)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}/V_{PP}$	0		130	ns

NOTES: 3. For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0. (Reference page 11.)
4. Common test conditions apply for t_{dis} except during programming.

recommended timing requirements for programming: V_{CC} = 6 V and $\overline{G}/V_{PP}$ = 12.5 V (Fast) or V_{CC} = 6.50 V and $\overline{G}/V_{PP}$ = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 3)

			MIN	TYP	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	μs
$t_{w(FPGM)}$	Final pulse duration	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			μs
$t_{su(D)}$	Data setup time		2			μs
$t_{su(VPP)}$	$\overline{G}/V_{PP}$ setup time		2			μs
$t_{su(VCC)}$	V_{CC} setup time		2			μs
$t_{h(A)}$	Address hold time		0			μs
$t_{h(D)}$	Data hold time		2			μs
$t_{h(VPP)}$	$\overline{G}/V_{PP}$ hold time		2			μs
$t_{rec(PG)}$	$\overline{G}/V_{PP}$ recovery time		2			μs
t_{EHD}	Data valid from $\overline{E}$ low				1	μs
$t_{r(PG)G}$	$\overline{G}/V_{PP}$ rise time		50			ns

NOTE 3. For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0. (Reference page 11.)

PARAMETER MEASUREMENT INFORMATION

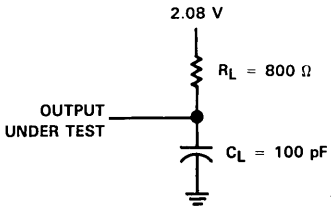
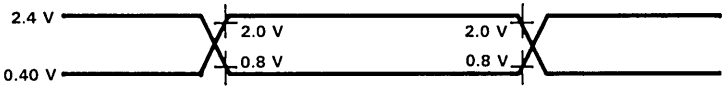


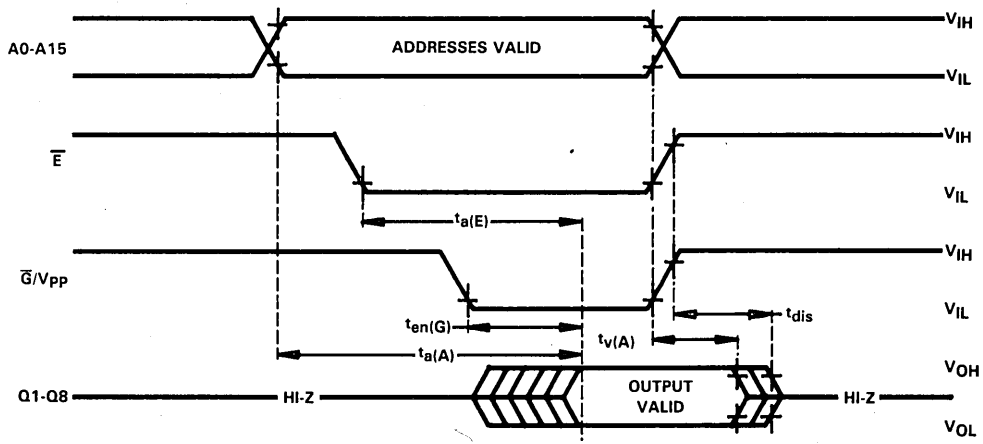
FIGURE 3. OUTPUT LOAD CIRCUIT

AC testing input/output wave forms

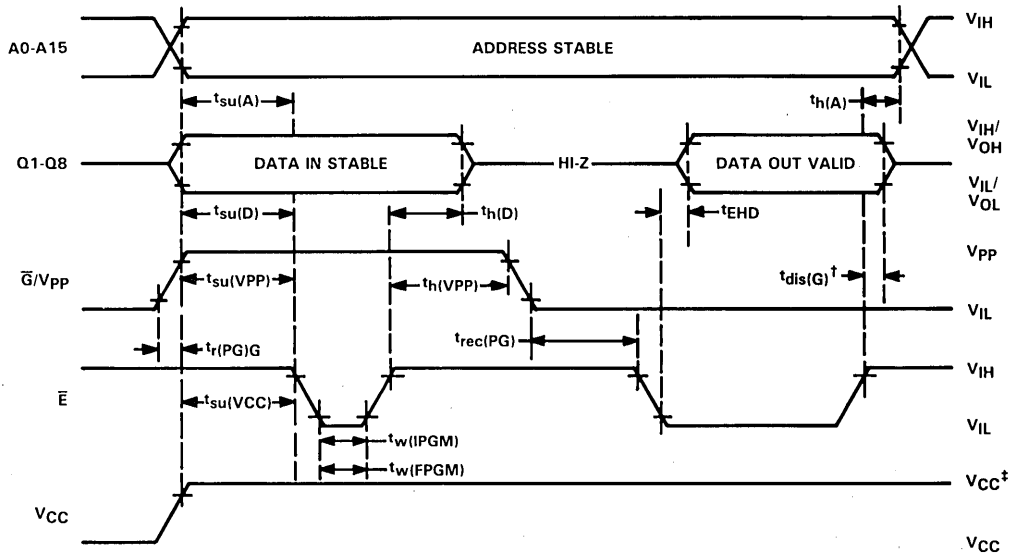


A.C. testing inputs are driven at 2.4 V for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 for both inputs and outputs.

read cycle timing



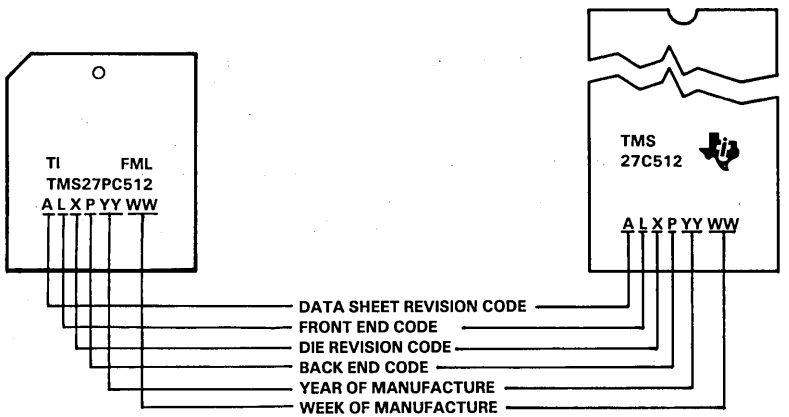
program cycle timing



†$t_{dis(G)}$ is a characteristic of the device but must be accommodated by the programmer.
‡12.5 V $\overline{G}/V_{PP}$ and 6.0 V V_{CC} for Fast programming; 13.0 V $\overline{G}/V_{PP}$ and 6.50 V V_{CC} for SNAP! Pulse programming.

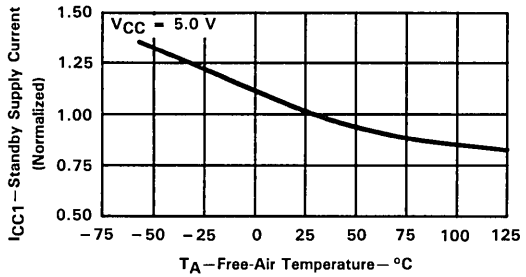
device symbolization

This data sheet is applicable to all TI TMS27C512 CMOS EPROMs and TMS27PC512 CMOS PROMs with the code "A" shown below:

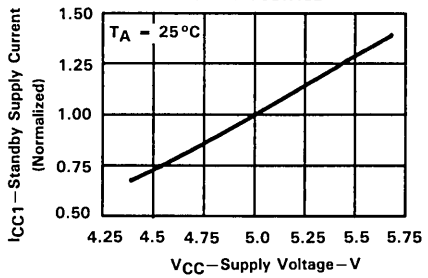


TYPICAL TMS27C/PC512 CHARACTERISTICS

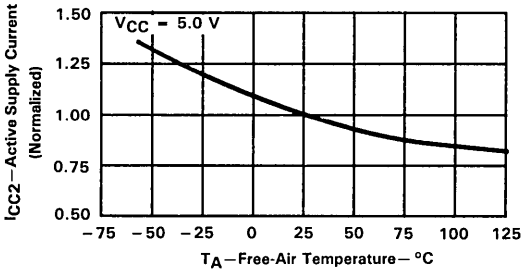
STANDBY SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



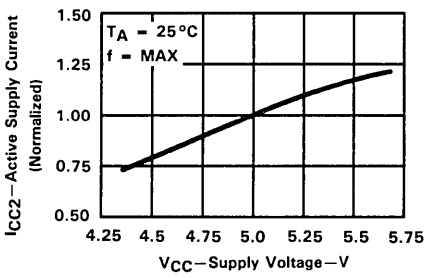
STANDBY SUPPLY CURRENT
vs
SUPPLY VOLTAGE



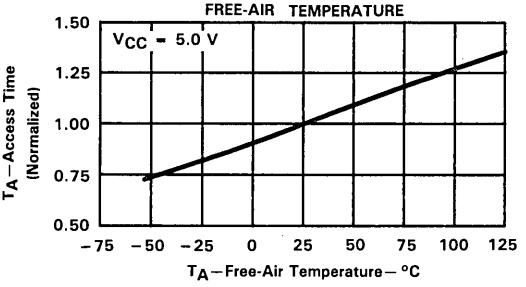
ACTIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



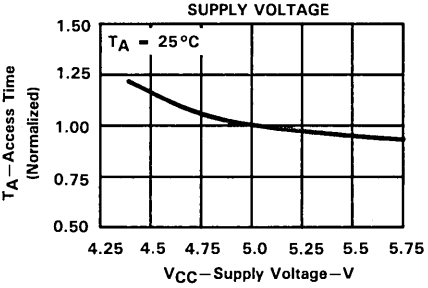
ACTIVE SUPPLY CURRENT
vs
SUPPLY VOLTAGE



ACCESS TIME
vs
FREE-AIR TEMPERATURE



ACCESS TIME
vs
SUPPLY VOLTAGE



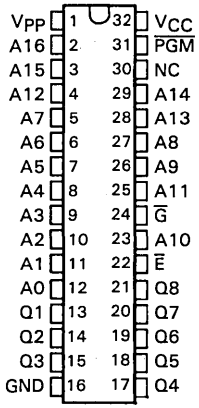
JANUARY 1988

- Organization . . . 128K × 8
- Single 5-V Power Supply
- Industry Standard 32-Pin Dual-In-line Package
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time

V_{CC} ± 5%	V_{CC} ± 10%	
'27C010-170		170 ns
'27C010-200	'27C010-20	200 ns
'27C010-250	'27C010-25	250 ns
'27C010-300	'27C010-30	300 ns

- 8-Bit Output For Use in Microprocessor-Based Systems
- 32-Bit Programming (Four Bytes) and Standard 8-Bit Programming
- Power Saving CMOS Technology
- 3-State Output Buffers
- Uses TI's Innovative ACE (Advanced Contactless EPROM) Technology for Noise Immunity and Improved Reliability
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required
- Low Power Dissipation (V_{CC} = 5.5 V)
  Active . . . 220 mW Worst Case
  Standby . . . 1.5 mW Worst Case
  (CMOS-Input Levels)
- Operating Free-Air Temperature 0°C to 70°C

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A16	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Supply
V_{PP}	12.5-V Power Supply†

†Only in program mode.

description

The TMS27C010 series are 1,048,576-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits. Each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C010 is offered in a 600-mil dual-in-line cerdip package (J suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

There are nine modes of operation for the TMS27C010 which are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and V_H (12 V) on A9 for signature mode.

MODE	FUNCTION (PINS)							
	$\overline{E}$ (22)	$\overline{G}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	A9 (26)	A0 (12)	Q1-Q8 (13-15, 17-21)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	X	X	D_{OUT}
Output Disable	X†	V_{IH}	X	V_{CC}	V_{CC}	X	X	HI-Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	X	X	HI-Z
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	D_{IN}
Programming One Byte	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	D_{IN}
Programming Four Byte	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	HI-Z
Program Inhibit	X	V_{IL}	V_{IL}	V_{PP}	V_{CC}	X	X	HI-Z
	X	V_{IH}	V_{IH}					
Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	D_{OUT}
Signature Mode	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	V_H‡	V_{IL}	MFG Code 97
							V_{IH}	Device Code 46

†X can be V_{IL} or V_{IH}
‡V_H = 12 V±0.5 V

read/output disable

When the outputs of two or more TMS27C010s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of the TMS27C010, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunty on the TMS27C010 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 40 mA to 500 μA for a high TTL input on $\overline{E}$ and to 250 μA for a high CMOS input on $\overline{E}$. In this mode all outputs are in the high impedance state.

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erasure

Before programming, the TMS27C010 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C010, the window should be covered with an opaque label. After erasure (all bits in logic 1 state), logic 0s are programmed into the desired locations. A programmed zero can be erased only by ultraviolet light.

32-bit programming

The device is programmed in 32-bit blocks by latching four successive bytes. The programming sequence is shown in the 32-bit programming flow chart (Figure 1).

The initial setup in the page data latch is V_{PP} = 12.5 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IH}, $\overline{G}$ = V_{IH}, and $\overline{PGM}$ = V_{IH}. The first location is defined as any address when A0 = logic 0 and A1 = logic 0, and the first order data is the corresponding eight bits of parallel data. Subsequently, the next three bytes of data are defined when A0 = logic 1 and A1 = logic 0, A0 = logic 0 and A1 = logic 1, and A0 = logic 1 and A1 = logic 1, respectively.

Starting at the first location, the four bytes of data are presented in sequence to the data pins Q1 through Q8. For every byte, when the addresses and data are stable, $\overline{G}$ is pulsed low (V_{IL}) and the byte is latched on the rising edge of $\overline{G}$. The 32-bit parallel programming is achieved when $\overline{PGM}$ is pulsed low (V_{IL}) with a pulse duration of $t_{w(PGM)}$. Every location is programmed only once before going to the interactive mode.

In the interactive mode, the word is verified at V_{PP} = 12.5 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}. If the correct data is not read, 8-bit programming is performed by pulling $\overline{PGM}$ low with a pulse duration of $t_{w(PGM)}$. This sequence of verification and programming is performed up to a maximum of 15 times. When the device is fully programmed, all bytes are verified with V_{CC} = V_{PP} = 5.0 V ± 10%.

8-bit programming

TMS27C010 can also be programmed by using the 8-bit programming algorithm. The programming sequence is shown in the 8-bit programming flow chart (Figure 2).

The initial setup is V_{PP} = 12.5 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, and $\overline{PGM}$ = V_{IH}. Once the initial location is selected, the data is presented in parallel (eight bits) on pins Q1 through Q8. Once addresses and data are stable, the programming mode is achieved when $\overline{PGM}$ is pulsed low (V_{IL}) with a pulse duration of $t_{w(PGM)}$. Every location is programmed only once before going to interactive mode.

In the interactive mode, the word is verified at V_{PP} = 12.5 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}. If the correct data is not read, the eight-bit programming is performed by pulling $\overline{PGM}$ low with a pulse duration of $t_{w(PGM)}$. This sequence of verification and programming is performed up to a maximum of 15 times. When the device is fully programmed, all bytes are verified with V_{CC} = V_{PP} = 5.0 V ± 10%.

program inhibit

Programming may be inhibited by maintaining a high level input on both $\overline{G}$ and $\overline{PGM}$ pins or a low level input on both $\overline{G}$ and $\overline{PGM}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}.

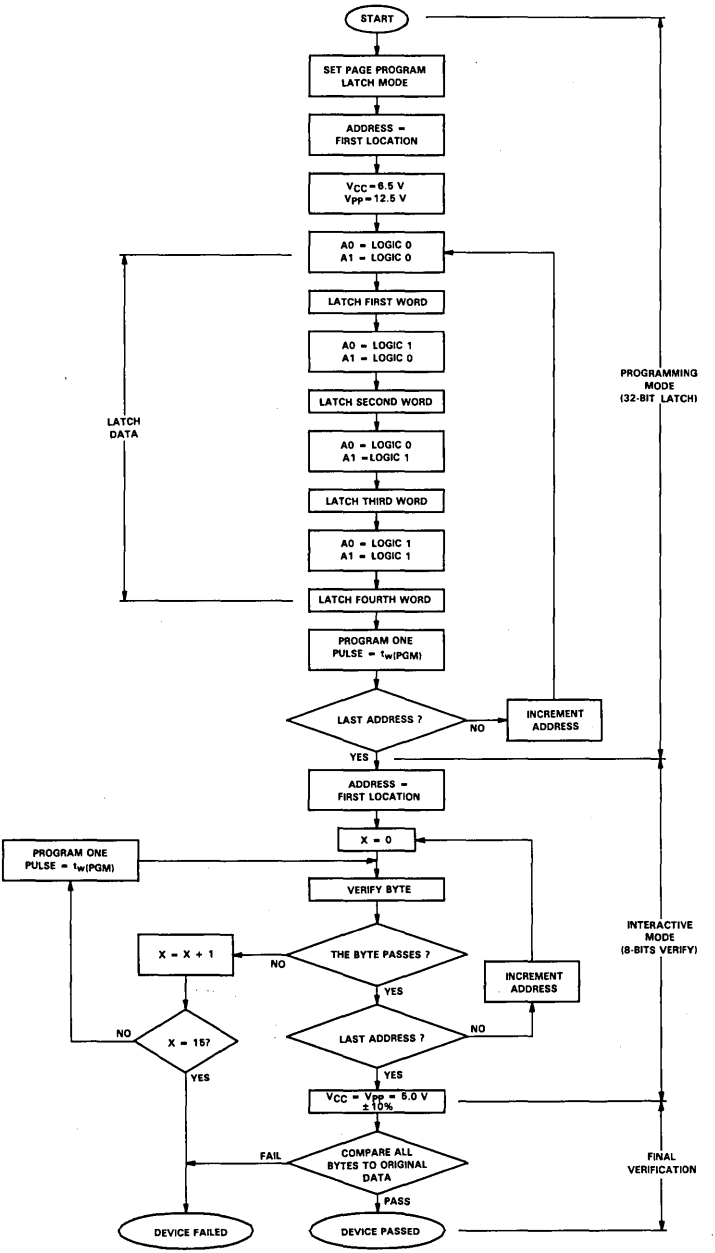

FIGURE 1. 32-BIT PROGRAMMING FLOW CHART

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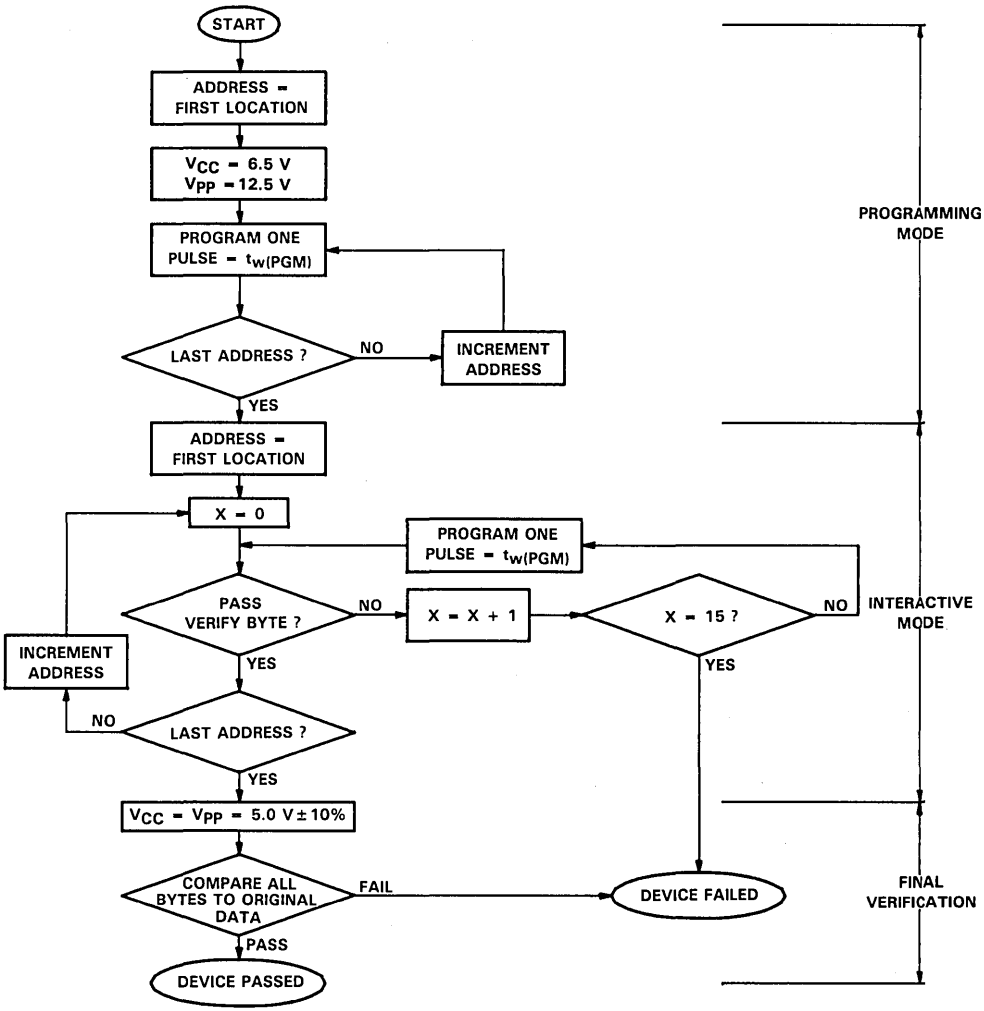


FIGURE 2. 8-BIT PROGRAMMING FLOW CHART

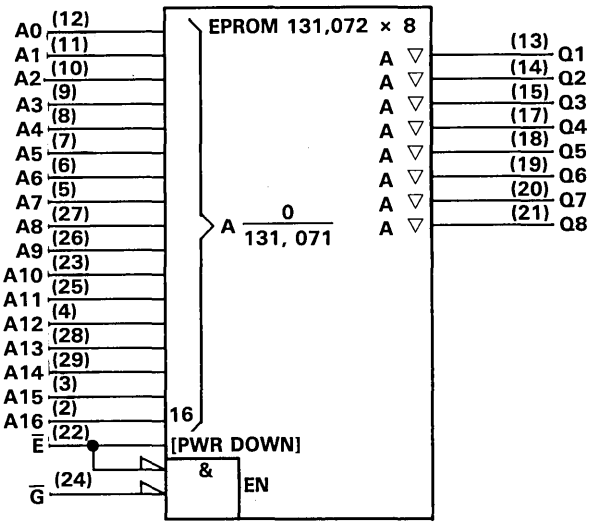
signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12.0 V. Two identifier bytes are accessed by toggling A0. All addresses must be held low. The signature code for the TMS27C010 is 9746. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code 46 (Hex), as shown by the signature mode table below.

IDENTIFIER†	PINS									
	A0	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	0	1	0	0	0	1	1	0	46

†$\overline{E} = \overline{G} = V_{IL}$, A9 = V_H, $V_{PP} = V_{CC}$.

logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7.0 V
Supply voltage range, V_{PP} (see Note 1) . . . . . −0.6 V to 13.0 V
Input voltage range (see Note 1), All inputs except A9 . . . . . −0.6 V to V_{CC} + 1.0 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range, with respect to V_{SS} (see Note 1) . . . . . −0.6 V to V_{CC} + 1.0 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			'27C010-170, '27C010-200, '27C010-250, '27C010-300			'27C010-20, '27C010-25, '27C010-30			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage—read mode (see Note 2)		4.75	5.0	5.25	4.5	5.0	5.5	V
V_{PP}	Supply voltage—read mode (see Note 3)		$V_{CC}-0.6$	V_{CC}	$V_{CC}+0.6$	$V_{CC}-0.6$	V_{CC}	$V_{CC}+0.6$	V
V_{IH}	High-level input voltage	TTL	2.0		$V_{CC}+1$	2.0		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		GND+0.2	−0.5		GND+0.2	
T_A	Operating free-air temperature		0		70	0		70	°C

NOTES: 2. V_{CC} must be applied after or at the same time as V_{PP} and removed before or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming, V_{PP} must be maintained at 12.5 V ± 0.25 V.

electrical characteristics over full range of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −20 μA	$V_{CC}-0.2$		V
			I_{OH} = −2.0 mA	2.4		
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 μA		0.1	
I_I	Input current (leakage)		V_I = 0 V to 5.5 V		±1	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}		±10	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		100	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 12.75 V (32-bit programming)		100	mA
I_{PP3}	V_{PP} supply current (during program pulse)		V_{PP} = 12.75 V (8-bit programming)		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$\overline{E}$ = V_{IH}, V_{CC} = 5.5 V		500	μA
		CMOS-input level	$\overline{E}$ = V_{CC} ± 0.2 V, V_{CC} = 5.5 V		250	
I_{CC2}	V_{CC} supply current (active) (output open)		$\overline{E}$ = V_{IL}, V_{CC} = 5.5 V, t_{cycle} = minimum cycle time, outputs open‡		40	mA

‡Minimum cycle time = maximum access time.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	10	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		10	14	pF

†Capacitance measurements are made on sample basis only.
‡All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 & 5)	'27C010-170		'27C010-200 '27C010-20		'27C010-250 '27C010-25		'27C010-300 '27C010-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \leq$ 20 ns, Input $t_f \leq$ 20 ns		170		200		250		300	ns
$t_{a(E)}$	Access time from chip enable			170		200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first§		0	60	0	60	0	80	0	80	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first		0		0		0		0		ns

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 (reference page 10.)
5. Common test conditions apply for t_{dis} except during programming.
§Value calculated from 0.5-V delta to measured output level.

recommended timing requirements for programming, T_A = 25°C (see Notes 4 and 6)

		MIN	NOM	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	0.45	0.5	0.55	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(E)}$	Chip enable setup time	2			μs
$t_{su(G)}$	Output enable setup time	2			μs
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time from $\overline{G}$	0			μs
$t_{h(G)}$	Output enable hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(A0)}$	Address hold time (programming)¶	2			μs
$t_{h(E)}$	Chip enable hold time¶	2			μs
$t_{su(D0)}$	Data setup time¶	100			ns
$t_{su(D1)}$	Data setup time¶	100			ns
$t_{su(D2)}$	Data setup time¶	100			ns
$t_{su(D3)}$	Data setup time¶	100			ns
$t_{h(D0)}$	Data hold time¶	100			ns
$t_{su(E)}$	Chip enable setup time¶	100			ns
$t_{su(G)}$	Output enable setup time¶	100			ns
t_{PL}	$\overline{G}$ pulse duration during page data latch¶	1			μs
$t_{su(PGM)}$	Programming setup time¶	1			μs

¶Denotes timing requirements for 32-bit programming only.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 (reference page 10.)

6. Input rise and fall times are ≤ 20 ns.

PARAMETER MEASUREMENT INFORMATION

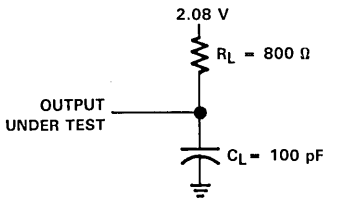
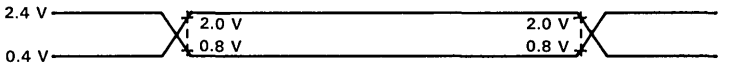


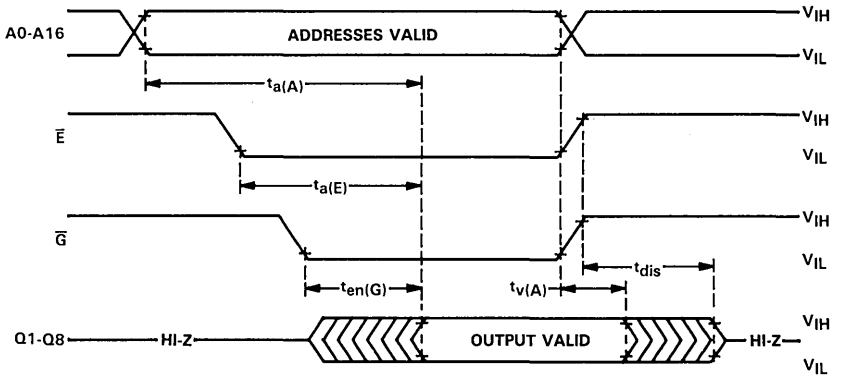
FIGURE 3. OUTPUT LOAD CIRCUIT

AC testing input/output wave forms

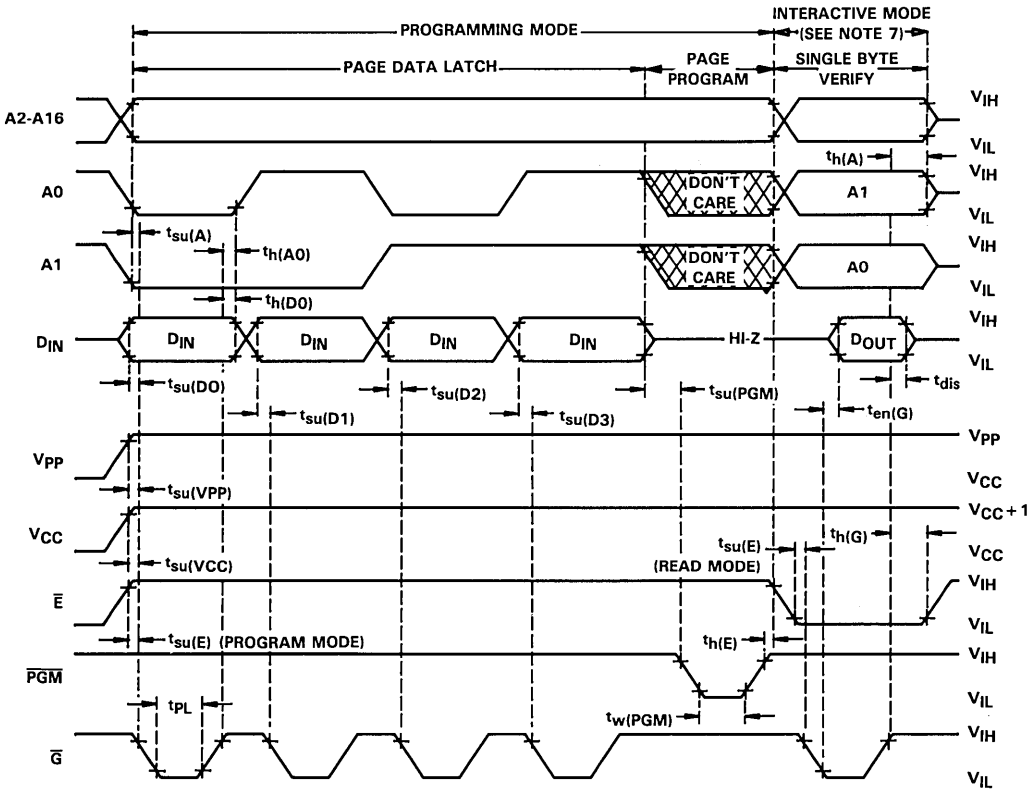


AC testing inputs are driven at 2.4 V for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 for both inputs and outputs.

read cycle timing

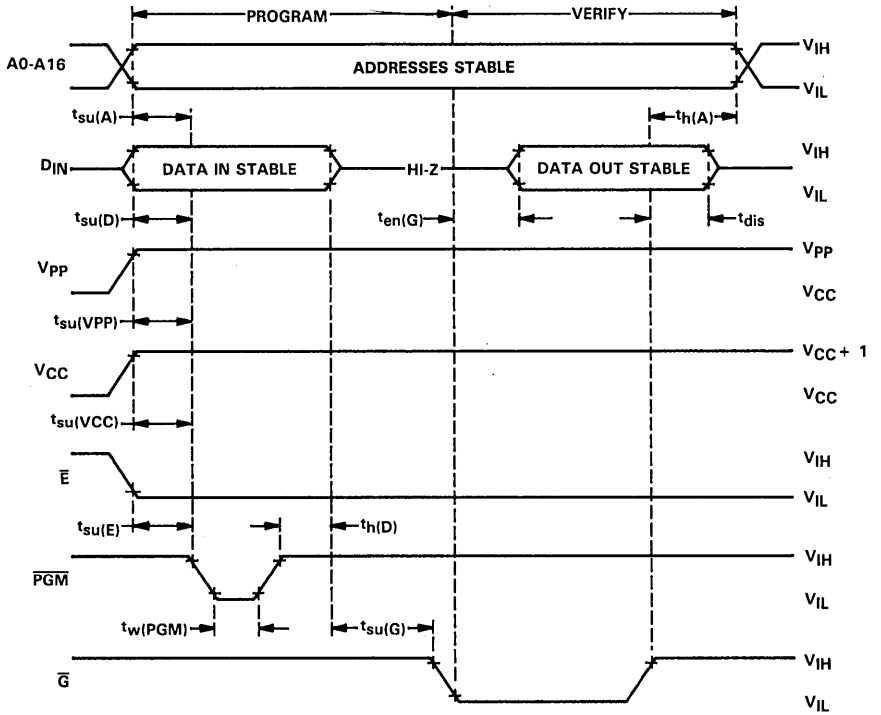


program cycle timing-32 bits



NOTE 7: 8-bit programming is applied in Interactive Mode when needed.

program cycle timing–8 bits



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

1,048,576-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY

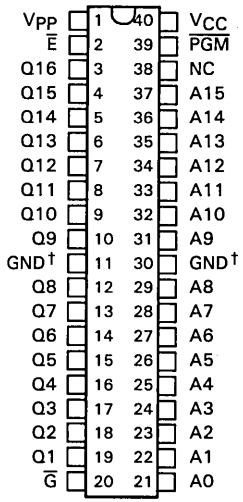
MAY 1987—REVISED JUNE 1988

- Wide-Word Organization . . . 64K × 16
- Single 5-V Power Supply
- Operationally Compatible with Existing Megabit EPROMs
- 40-Pin Dual-In-line Package
- All Inputs and Outputs Fully TTL Compatible
- Static Operations (No Clocks, No Refresh)
- Max Access/Min Cycle Time

V_{CC} ± 5%	V_{CC} ± 10%	
'27C210-170		170 ns
'27C210-200	'27C210-20	200 ns
'27C210-250	'27C210-25	250 ns
'27C210-300	'27C210-30	300 ns

- 16-Bit Output For Use in Microprocessor-Based Systems
- 32-Bit Programming (Two 16-Bit Words) and 16-Bit Programming
- 16 Seconds Typical Programming Time
- Power Saving CMOS Technology
- 3-State Output Buffers
- Uses TI's Innovative ACE (Advanced Contactless EPROM) Technology for Noise Immunity and Improved Reliability
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Latchup Immunity of 250 mA on All Input and Output Pins
- No Pull-Up Resistors Required
- Low Power Dissipation
  —Active . . . 220 mW Worst Case
  —Standby . . . 1.5 mW Worst Case (CMOS-Input Levels)
- Operating Free-Air Temperature 0°C to 70°C

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q16	Outputs
V_{CC}	5-V Supply
V_{PP}	12.5-V Supply‡

†Pins 11 and 30 must be connected externally to ground.
‡Only in program mode.

description

The TMS27C210 is a 1,048,576-bit, ultraviolet-light erasable, electrically programmable read-only memory. This device is fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C210 is offered in a dual-in-line cerdip package (J suffix) rated for operation from 0°C to 70°C.

Since this EPROM operates from a single 5-V supply (in the read mode), it is ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

There are eight modes of operation for the TMS27C210 which are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

MODE	FUNCTION PINS							
	$\overline{E}$ (2)	$\overline{G}$ (20)	$\overline{PGM}$ (39)	V_{PP} (1)	V_{CC} (40)	A9 (31)	A0 (21)	I/O (19-12) (10-3)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	X	X	Q1-Q8 Q9-Q16
Output Disable	X†	V_{IH}	X	V_{CC}	V_{CC}	X	X	HI-Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	X	X	HI-Z
Programming	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	D_{IN}
Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	X	X	HI-Z
Signature Mode (Mfg)	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	V_H‡	V_{IL}	Mfg Code 0097
Signature Mode (Device)	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	V_H‡	V_{IH}	Device Code 0086

†X can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C210s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of the TMS27C210, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunty on the TMS27C210 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

power down

Active power dissipation can be reduced from 40 mA to 1 mA for a high TTL input on $\overline{E}$ and to 250 μA for a high CMOS input on $\overline{E}$. In this mode all outputs are in the high impedance state.

erasure

Before programming, the TMS27C210 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds-per-square-centimeter. A typical 12 milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C210, the window should be covered with an opaque label.

32-bit programming

After erasure (all bits in logic 1 state), logic 0s are programmed into the desired locations. A programmed zero can be erased only by ultraviolet light. The device is programmed in 32-bit blocks. The programming sequence is shown in the 32-bit programming flow chart (Figure 1).

The initial setup in the page data latch is V_{PP} = 12.5 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, and $\overline{PGM}$ = V_{IH}. The first location is defined as any address when A0 = logic 0, and the low order word data is the corresponding 16 bits of parallel data. The high order word data is the 16 bits of parallel data for any address when A0 = logic 1.

Once the first location is selected, the low order word data is presented to the data pins Q1 to Q16. When the address and data are stable, A0 is clocked from logic 0 to logic 1. The low order word is latched on the rising edge of A0 when V_{PP} = 12.5 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, and $\overline{PGM}$ = V_{IH}. The high order word is then presented to the data pins. When the data is stable, the 32-bit parallel programming is achieved when $\overline{PGM}$ is pulsed low (V_{IL}). The length of the pulse is $t_{w(PGM)}$. Every location is programmed once before going to the interactive mode.

The interactive mode consists of a sequence of verification and programming. In the interactive mode, two 16-bit words corresponding to low and high order word data are verified at V_{PP} = 12.5 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}. If the correct data is not read in either or both words, 32-bit bit programming is performed with V_{PP} = 12.5 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, and a low pulse of $t_{w(PGM)}$ on $\overline{PGM}$. This sequence of verification and programming is performed up to a maximum of 15 times for two words. When the device is fully programmed, all bits are verified with V_{CC} = V_{PP} = 5.0 V ± 10%.

16-bit programming

TMS27C210 can also be programmed in 16-bit blocks if desired. The 16-bit programming flow is shown in Figure 2. The initial setup is the same as the 32-bit programming flow except $\overline{E} = V_{IH}$. Once the initial location is selected, the 16-bit word data is presented to the data pins Q1 through Q16. When the addresses and data are stable, $\overline{E}$ is pulled low (V_{IL}). The 16-bit programming is achieved when $\overline{PGM}$ is pulsed low (V_{IL}). The length of the pulse is $t_{w(PGM)}$. To program the next location, $\overline{E}$ is pulled high (V_{IH}) and the 16-bit data is presented to the data pins. When the data and address are are stable, programming is achieved with $\overline{E} = V_{IL}$ followed by a low pulse of $t_{w(PGM)}$ on $\overline{PGM}$. Every location is programmed once before going to the interactive mode.

In the interactive mode, 16-bit data corresponding to every location is verified at V_{PP} = 12.5 V, V_{CC} = 6.5 V, $\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, and $\overline{PGM} = V_{IH}$. If the correct data is not read, a 16-bit word programming is performed with $\overline{G} = V_{IH}$ and a low pulse of $t_{w(PGM)}$ on $\overline{PGM}$. This sequence of verification and programming is performed up to a maximum of 15 times for a word. When the device is fully programmed, all bits are verified with $V_{CC} = V_{PP} = 5.0\ V \pm 10\%$.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 31) is forced to 12.0 V. Two identifier bytes are accessed by toggling A0. Q1-Q8 contain the valid codes. Each byte possesses odd parity on bit Q8. All other addresses must be held low. The signature code for the TMS27C210 is 9786. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code 86 (Hex), as shown by the signature mode table on page 7.

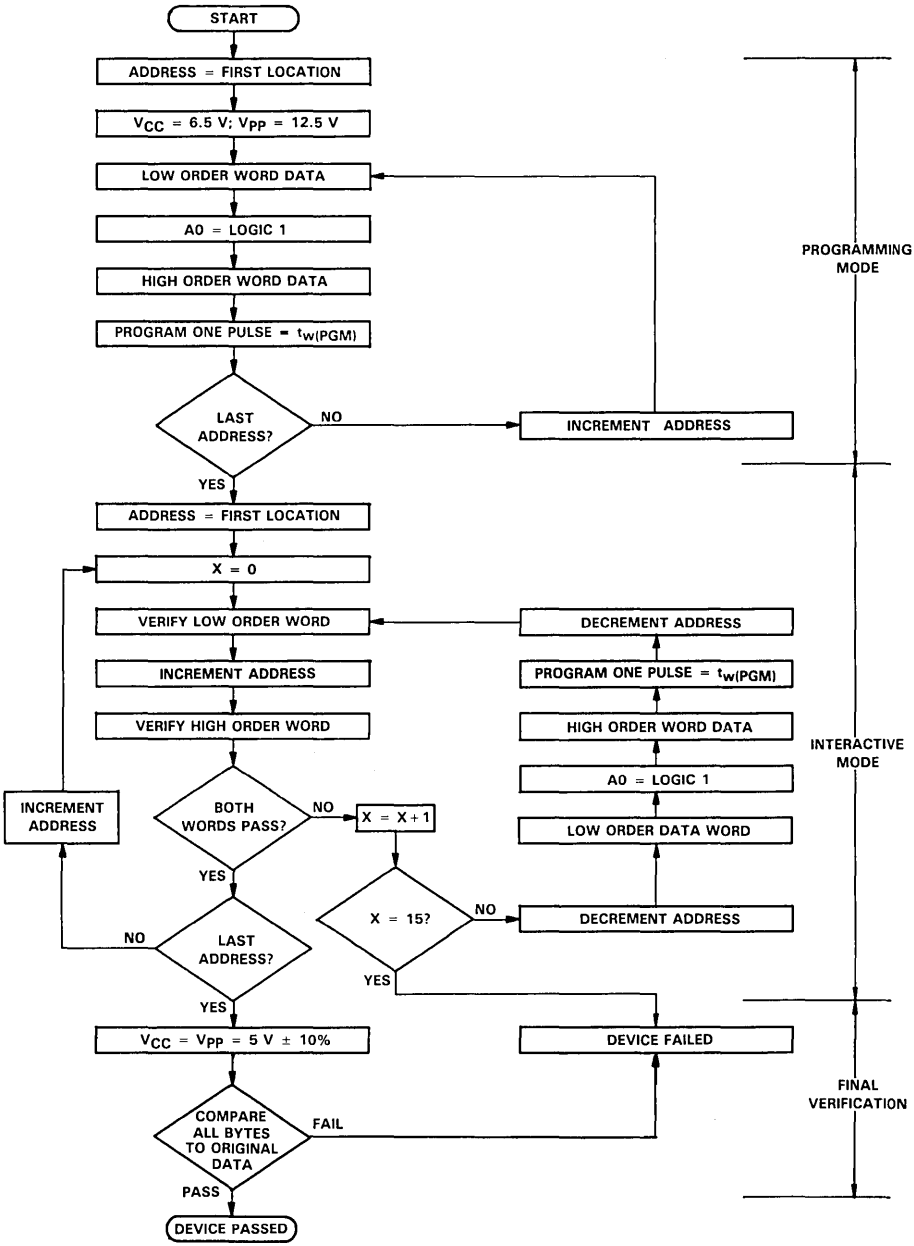


FIGURE 1. 32-BIT PROGRAMMING FLOW CHART

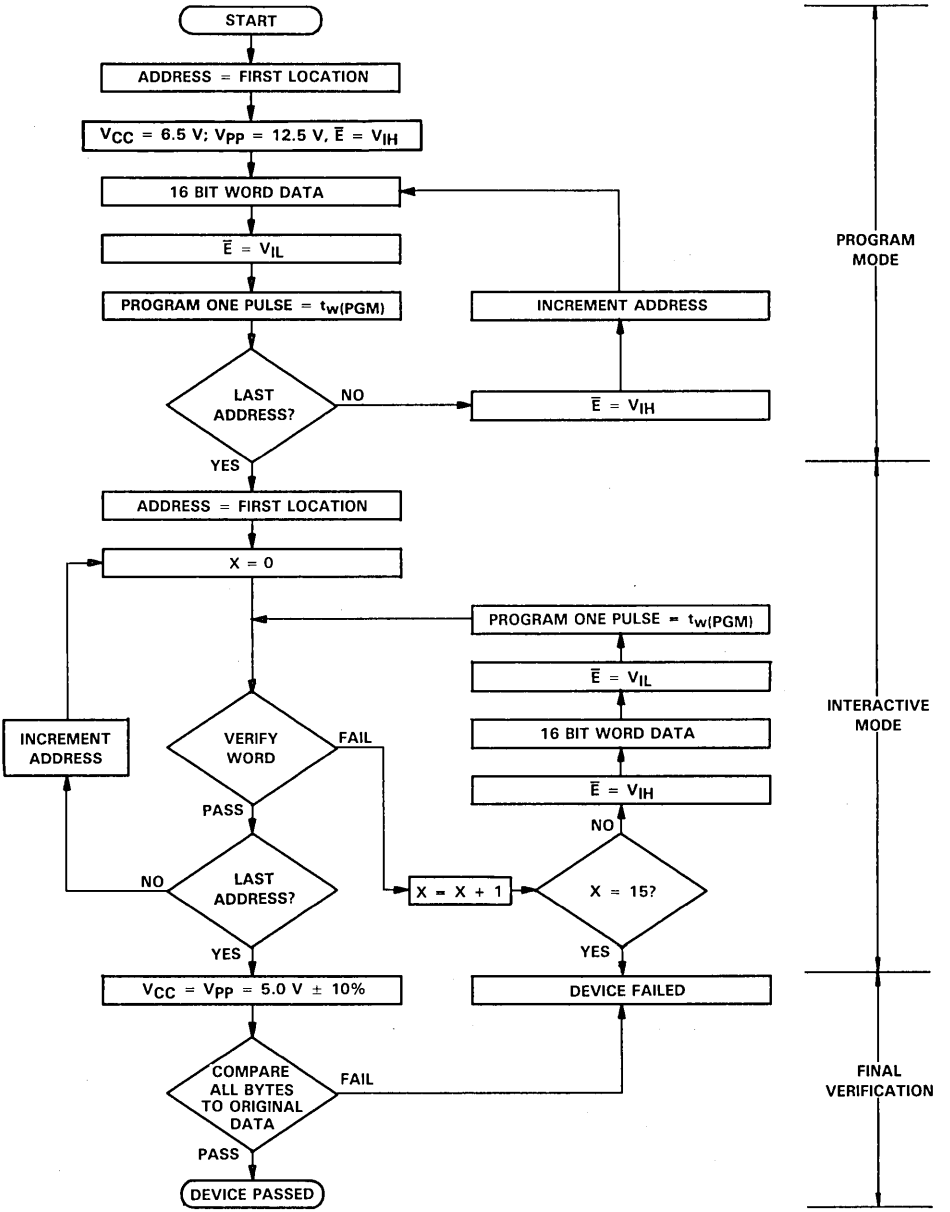


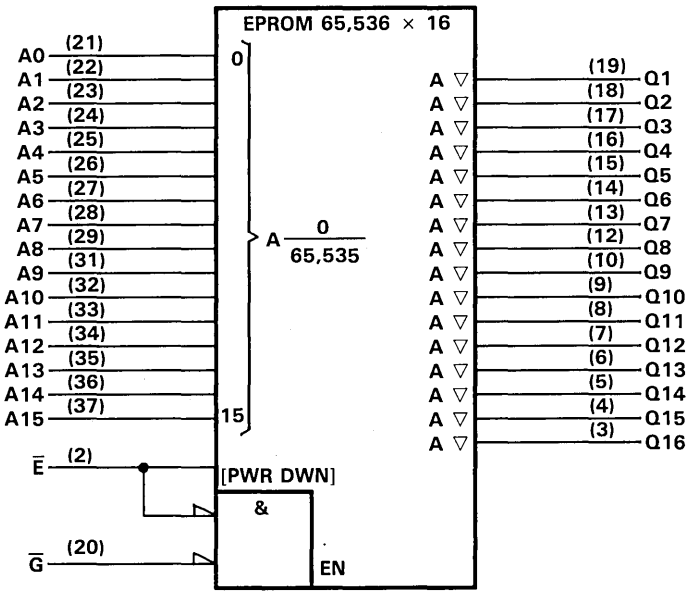
FIGURE 2. 16-BIT PROGRAMMING FLOW CHART

signature mode†

IDENTIFIER†	PINS									
	A0	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	1	0	0	0	0	1	1	0	86

†$\overline{E} = \overline{G} = V_{IL}$, A9 = V_H, A1-A8 = V_{IL}, A10-A15 = V_{IL}, $V_{PP} = V_{CC}$, $\overline{PGM} = V_{IH}$ or V_{IL}.

logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7.0 V
Supply voltage range, V_{PP} (see Note 1) . . . . . −0.6 V to 13.0 V
Input voltage range (see Note 1), All inputs except A9 . . . . . −0.6 V to V_{CC} + 1.0 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1.0 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

§Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			'27C210-170, '27C210-200, '27C210-250, '27C210-300			'27C210-20, '27C210-25, '27C210-30			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage-read mode (see Note 2)		4.75	5.0	5.25	4.5	5.0	5.5	V
V_{PP}	Supply voltage-read mode (see Note 3)		$V_{CC}-1.0$	V_{CC}	$V_{CC}+1.0$	$V_{CC}-1.0$	V_{CC}	$V_{CC}+1.0$	V
V_{IH}	High-level input voltage	TTL	2.0		$V_{CC}+1$	2.0		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		GND+0.2	−0.5		GND+0.2	
T_A	Operating free-air temperature		0		70	0		70	°C

NOTES: 2. V_{CC} must be applied after or at the same time as V_{PP} and removed before or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 12.5 V ± 0.25 V.

electrical characteristics over full range of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −20 μA	$V_{CC}-0.2$			V
			I_{OH} = −2.0 mA	2.4			
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
			I_{OL} = 20 μA			0.1	
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±1	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±10	μA
I_{PP1}	V_{PP} supply current		$V_{PP} = V_{CC}$ = 5.5 V			100	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 12.75 V (16-bit programming)			50	mA
I_{PP3}	V_{PP} supply current (during program pulse)		V_{PP} = 12.75 V (32-bit programming)			100	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E} = V_{IH}$			1	mA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E} = V_{CC}$ ± 0.2 V			250	μA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open‡		30	40	mA

†Typical values are at T_A = 25°C and nominal voltages.
‡Minimum cycle time = maximum address access time.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	10	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		10	14	pF

†Capacitance measurements are made on sample basis only.
‡Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTE 4)	'27C210-170		'27C210-20 '27C210-200		'27C210-25 '27C210-250		'27C210-30 '27C210-300		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		170		200		250		300	ns
$t_{a(E)}$	Access time from chip enable			170		200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first§		0	60	0	60	0	80	0	80	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first§		0		0		0		0		ns

§Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.
NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 (reference page 10.)

recommended timing requirements for programming, V_{CC} = 6.5 V and V_{PP} = 12.75 V, T_A = 25°C (see Notes 4 and 5)

		MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	0.45	0.5	0.55	ms
$t_{su(E)}$	Chip enable setup time	2			μs
$t_{su(A)}$	Address setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs
$t_{dis(G)}$	Output disable time from $\overline{G}$ (see Note 6)	0		100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(G)}$	Output enable hold time from data	2			μs
$t_{su(DAO)}$	Data setup time before A0 high	100			ns
$t_{h(DAO)}$	Data hold time after A0 high	100			ns
$t_{h(E)}$	Chip enable hold time	2			μs
$t_{w(E)}$	Chip enable pulse duration	200			ns

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 (reference page 10.)
5. Input signal t_r and $t_f \le$ 20 ns.
6. Common test conditions apply for $t_{dis(G)}$ except during programming.

PARAMETER MEASUREMENT INFORMATION

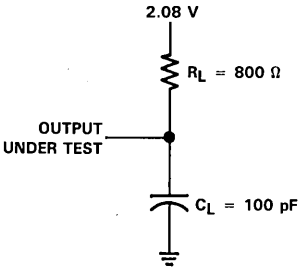
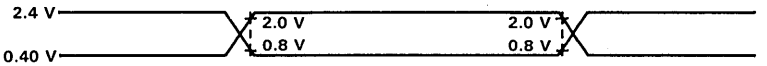


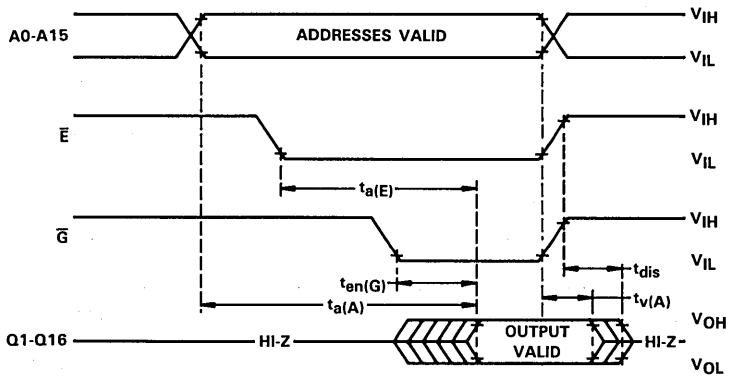
FIGURE 3. OUTPUT LOAD CIRCUIT

AC testing input/output wave forms

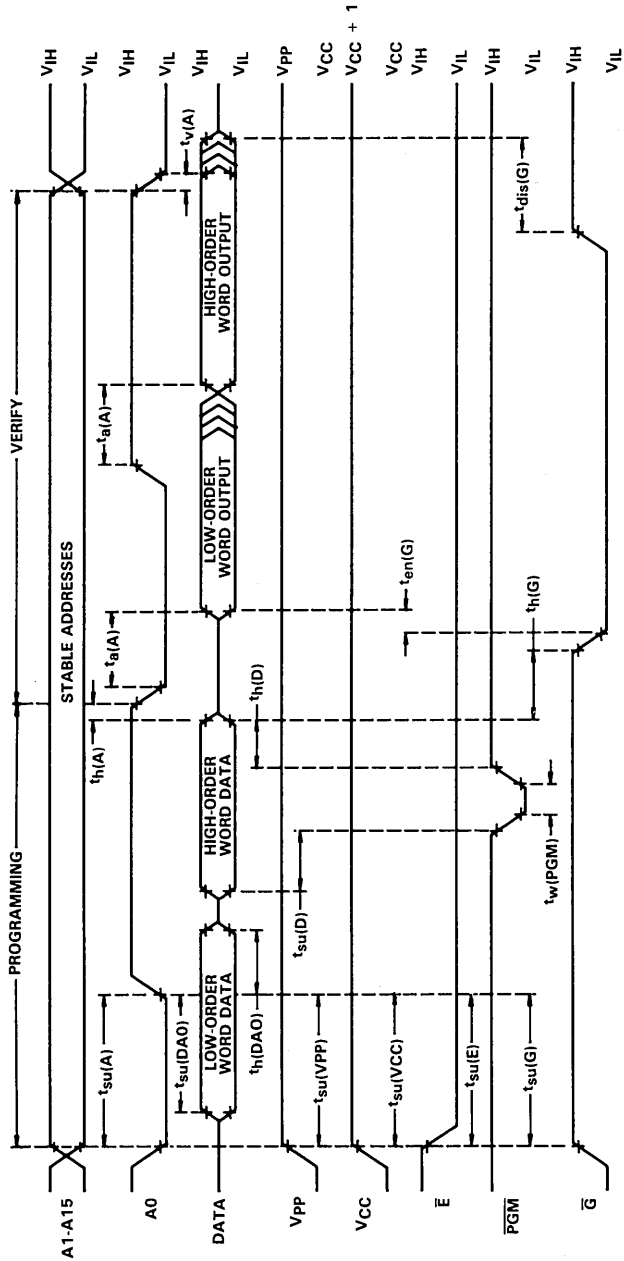


A.C. testing inputs are driven at 2.4 V for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 for both inputs and outputs.

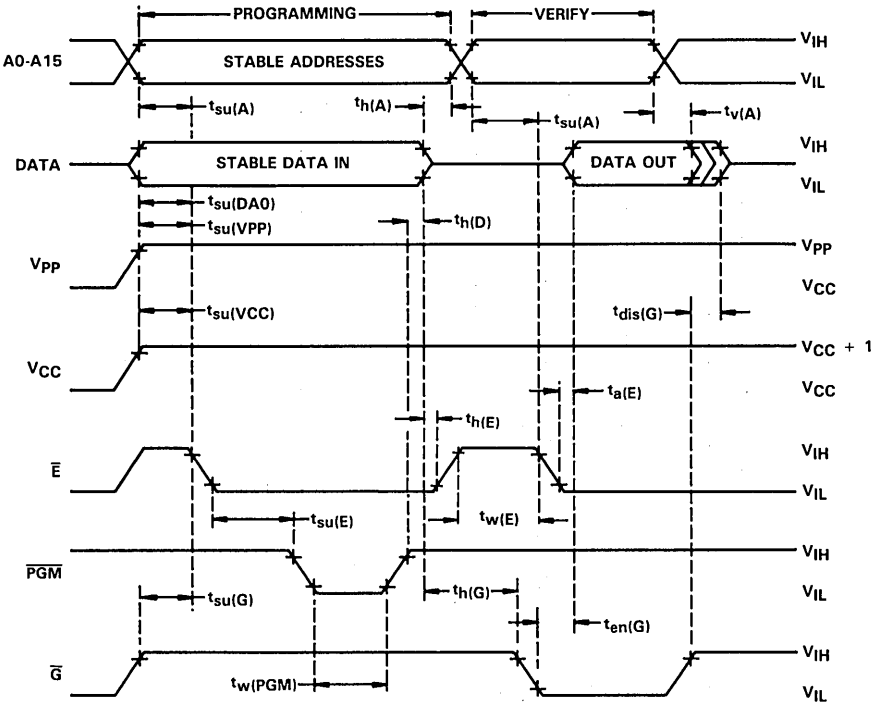
read cycle timing



32-bit programming



16-bit programming



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

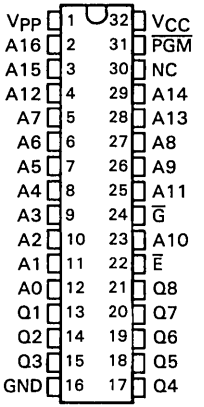
JANUARY 1988

- Organization . . . 128K × 8
- Single 5-V Power Supply
- Industry Standard 32-Pin Dual-In-line Package
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time

V_{CC} ± 5%	V_{CC} ± 10%	
'27PC010-200	'27PC010-20	200 ns
'27PC010-250	'27PC010-25	250 ns
'27PC010-300	'27PC010-30	300 ns

- 8-Bit Output For Use in Microprocessor-Based Systems
- 32-Bit Programming (Four Bytes) and Standard 8-Bit Programming
- Power Saving CMOS Technology
- 3-State Output Buffers
- Uses TI's Innovative ACE (Advanced Contactless EPROM) Technology for Noise Immunity and Improved Reliability
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required
- Low Power Dissipation (V_{CC} = 5.5 V)
  - —Active . . . 220 mW Worst Case
  - —Standby . . . 1.5 mW Worst Case (CMOS-Input Levels)
- Operating Free-Air Temperature . . . 0°C to 70°C

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A16	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Supply
V_{PP}	12.5-V Power Supply†

†Only in program mode.

description

The TMX27PC010 series are 1,048,576-bit, one-time, electrically programmable read-only memories. These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits. Each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The TMX27PC010 is offered in a 600-mil dual-in-line plastic package (N suffix) rated for operation from 0°C to 70°C.

Since these PROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing PROM programmers can be used.

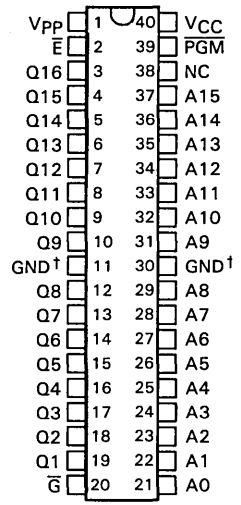
JANUARY 1988

- Wide-Word Organization . . . 64K × 16
- Single 5-V Power Supply
- Operationally Compatible with Existing Megabit EPROMs
- 40-Pin Dual-In-line Package
- All Inputs and Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time

V_{CC} ± 5%	V_{CC} ± 10%	
'27PC210-200	'27PC210-20	200 ns
'27PC210-250	'27PC210-25	250 ns
'27PC210-300	'27PC210-30	300 ns

- 16-Bit Output for Use in Microprocessor Systems
- 32-Bit Programming (Two 16-Bit Words) and 16-Bit Programming
- 16 Seconds Typical Programming Time
- Power Saving CMOS Technology
- 3-State Output Buffers
- Uses TI's Innovative ACE (Advanced Contactless EPROM) Technology for Noise Immunity and Improved Reliability
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Latchup Immunity of 250 mA on All Input and Output Pins
- No Pull-Up Resistors Required
- Low Power Dissipation
  —Active . . . 220 mW Worst Case
  —Standby . . . 1.5 mW Worst Case (CMOS-Input Levels)
- Operating Free-Air Temperature . . . 0°C to 70°C

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q16	Outputs
V_{CC}	5-V Supply
V_{PP}	12.5-V Supply‡

†Pins 11 and 30 must be connected externally to ground.
‡Only in program mode.

description

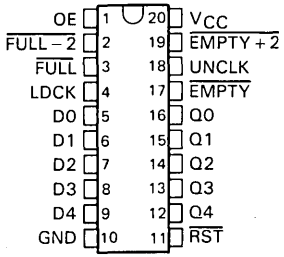
The TMX27PC210 is a 1,048,576-bit, one-time, electrically programmable read-only memory. This device is fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The TMX27PC210 is offered in a dual-in-line plastic package (N suffix) rated for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

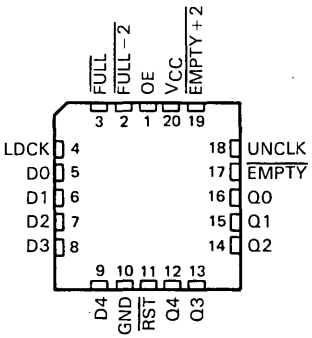
D2876, MARCH 1986—REVISED MAY 1986

- Independent Asychronous Inputs and Outputs
- 16 Words by 5 Bits Each
- Data Rates from 0 to 30 MHz
- Fall-Through Time . . . 24 ns Typ
- 3-State Outputs

SN54ALS229A . . . J PACKAGE
SN74ALS229A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS229A . . . FK PACKAGE
SN74ALS229A . . . FN PACKAGE
(TOP VIEW)



description

These 80-bit memories utilize Advanced Low-Power Schottky technology and feature high speed and fast fall-through times. They are organized as 16 words by 5 bits each.

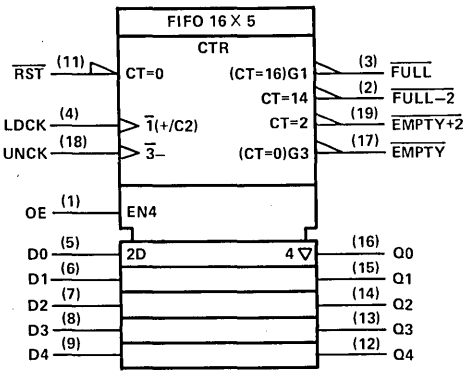
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals will have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, $\overline{\text{FULL}-2}$, and $\overline{\text{EMPTY}+2}$ output flags. The $\overline{\text{FULL}}$ output will be low whenever the memory is full, and high whenever not full. The $\overline{\text{FULL}-2}$ output will be low whenever the memory contains 14 data words. The $\overline{\text{EMPTY}}$ output will be low whenever the memory is empty, and high whenever it is not empty. The $\overline{\text{EMPTY}+2}$ output will be low whenever 2 words remain in memory.

A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$, $\overline{\text{FULL}-2}$, and $\overline{\text{EMPTY}+2}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a $\overline{\text{RST}}$ pulse or from an empty condition, will cause $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

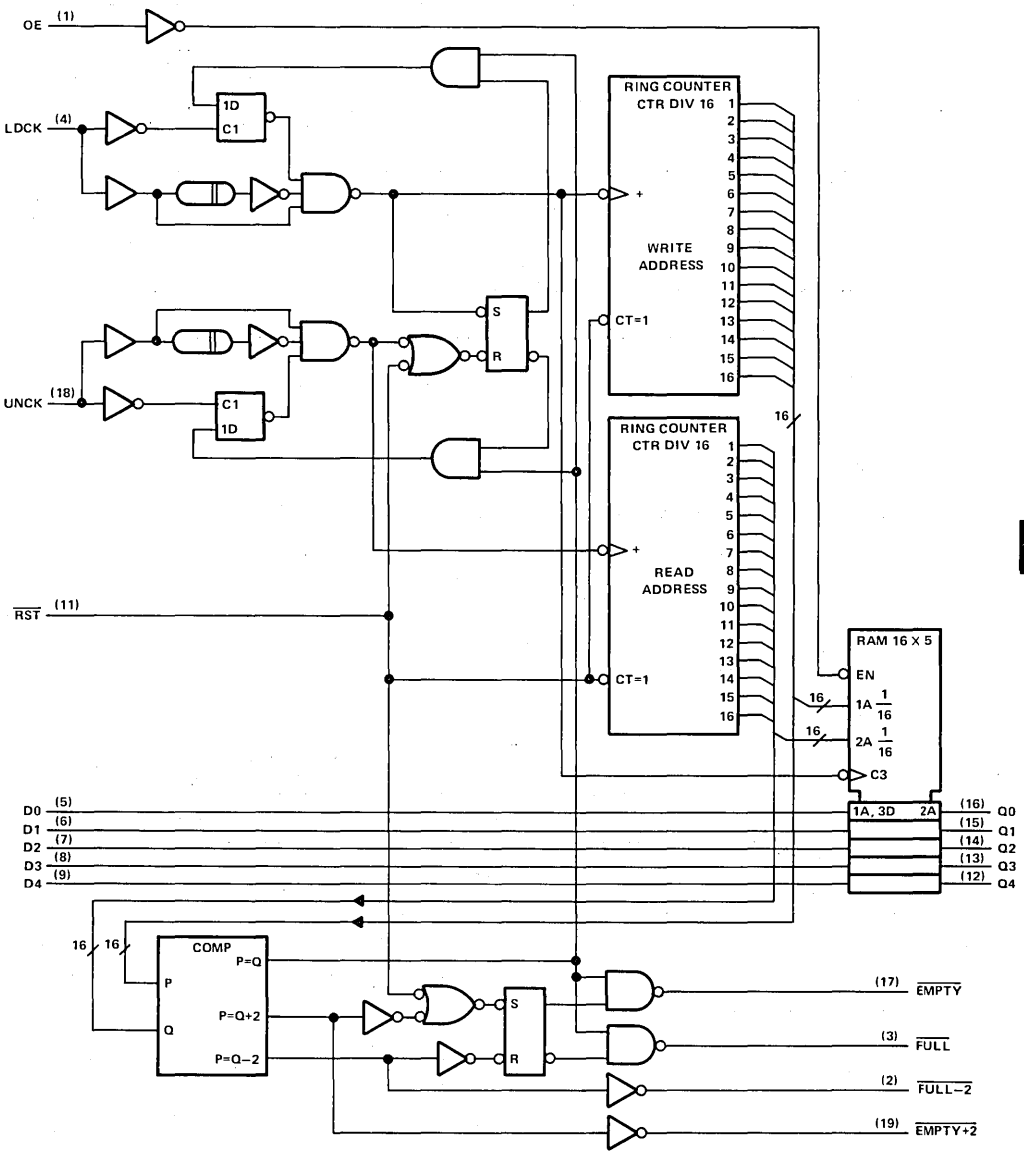
logic symbol†



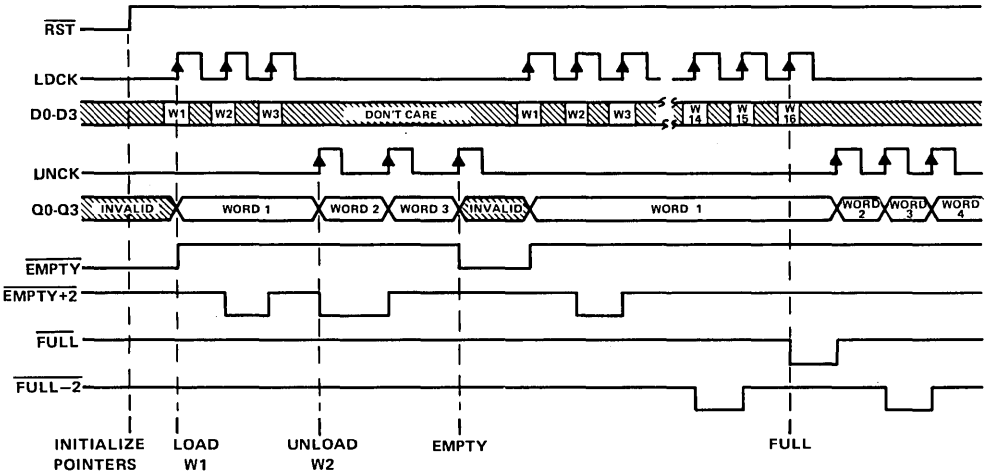
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

logic diagram (positive logic)



timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS229A . . . . . −55°C to 125°C
SN74ALS229A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS229A			SN74ALS229A			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current		Q outputs			−1.0			−1.6	mA
			Status flags			−0.4			−0.4	
I_{OL}	Low-level output current		Q outputs			12			24	mA
			Status flags			4			8	
f_{clock}	Clock frequency		LDCK	0		25	0		30	MHz
			UNCK	0		25	0		30	
t_w	Pulse duration		$\overline{RST}$ low	20			15			ns
			LDCK low	15			10			
			LDCK high	25			20			
			UNCK low	15			10			
			UNCK high	25			20			
t_{su}	Setup time	Data before LDCK↑		10			10			ns
		$\overline{RST}$ (inactive) before LDCK↑		5			5			
t_h	Hold time	Data after LDCK↑		5			5			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS229A			SN74ALS229A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			95	150		95	140	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

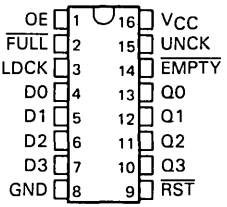
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS229A			SN54ALS229A		SN74ALS229A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK					25		30		MHz
	UNCK					25		30		
t_{pd}	LDCK↑	Any Q		24	47	7	54	7	50	ns
t_{pd}	UNCK↑	Any Q		19	29	9	35	9	33	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		18	26	9	32	9	30	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		18	25	9	32	9	29	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$		15	21	6	26	6	24	ns
t_{pd}	LDCK↑	$\overline{EMPTY+2}$		23	33	10	40	10	38	ns
t_{pd}	UNCK↑	$\overline{EMPTY+2}$		20	29	9	38	9	35	ns
t_{PLH}	$\overline{RST}$↓	$\overline{EMPTY+2}$		20	28	9	35	9	33	ns
t_{pd}	LDCK↑	$\overline{FULL-2}$		23	33	10	40	10	38	ns
t_{pd}	UNCK↑	$\overline{FULL-2}$		20	29	9	38	9	35	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL-2}$		20	28	9	35	9	33	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		21	28	10	35	10	33	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		17	23	8	29	8	27	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		18	27	8	33	8	31	ns
t_{en}	$\overline{OE}$↑	Q		8	13	1	16	2	15	ns
t_{dis}	$\overline{OE}$↓	Q		8	14	2	20	2	17	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

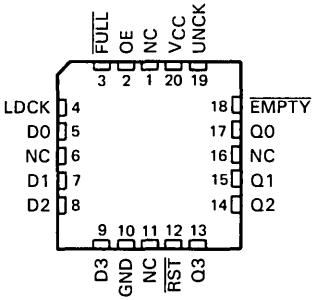
D2876, OCTOBER 1985—REVISED APRIL 1986

- Independent Asynchronous Inputs and Outputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- 16 Words by 4 Bits Each
- Data Rates from 0 to 30 MHz
- Fall-Through Time . . . 24 ns Typ
- 3-State Outputs

SN54ALS232A . . . J PACKAGE
SN74ALS232A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS232A . . . FK PACKAGE
SN74ALS232A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection.

description

These 64-bit memories use Advanced Low-Power Schottky technology and feature high speed and fast fall-through times. They are organized as 16 words by 4 bits each.

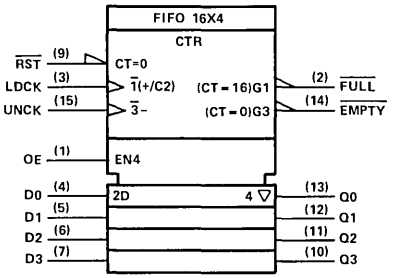
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ output flags. The $\overline{\text{FULL}}$ output will be low when the memory is full, and high when the memory is not full. The $\overline{\text{EMPTY}}$ output will be low when the memory is empty, and high when it is not empty.

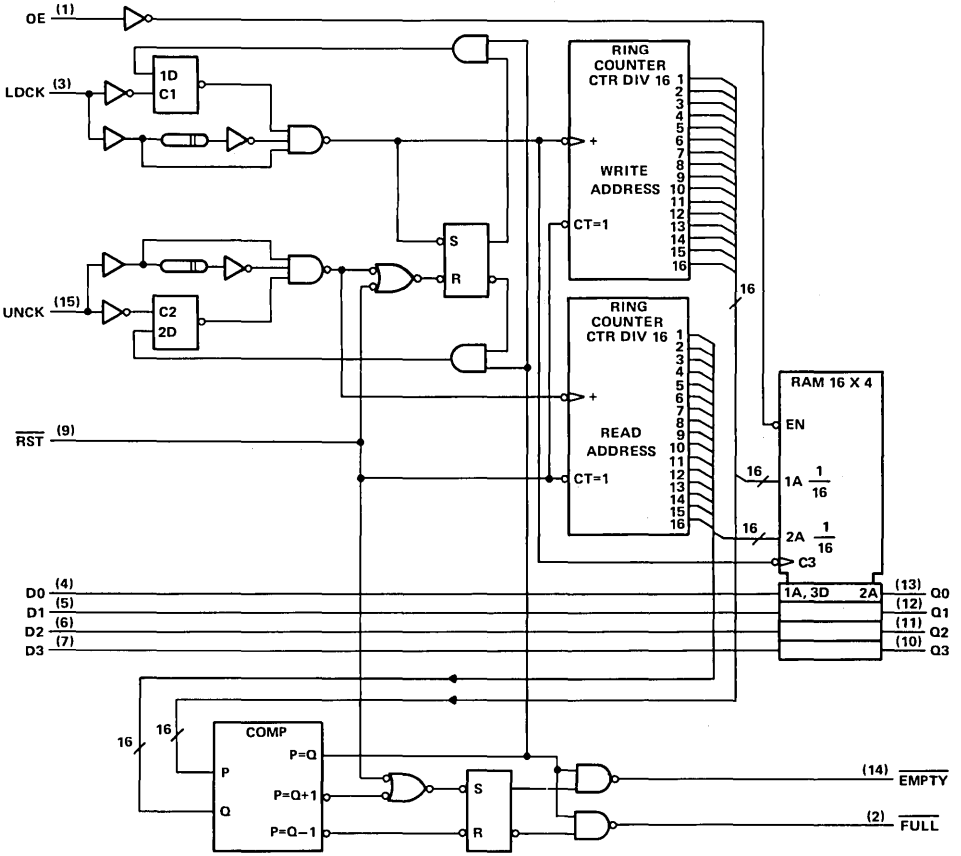
A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{\text{RST}}$ pulse or from an empty condition, will cause $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect either the $\overline{\text{FULL}}$ or $\overline{\text{EMPTY}}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

logic symbol†



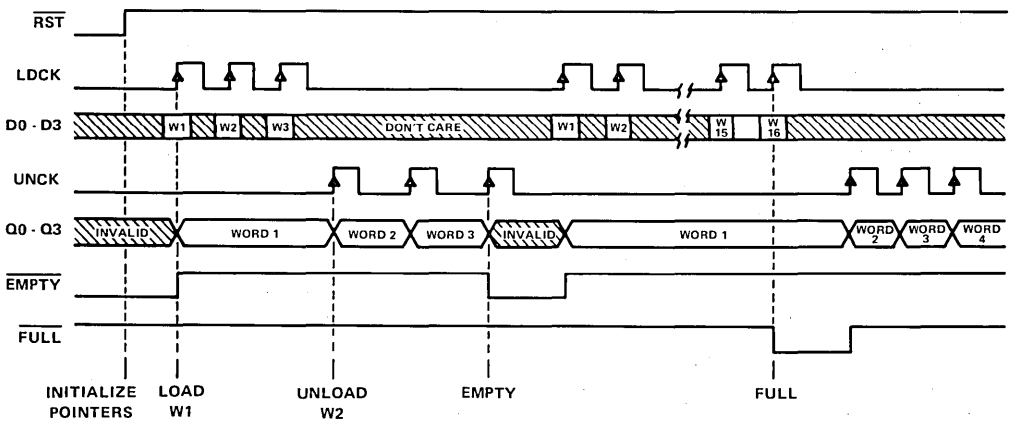
†This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS232A . . . . . −55°C to 125°C
SN74ALS232A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS232A			SN74ALS232A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current	Q outputs			−1			−1.6	mA
		$\overline{FULL}$, $\overline{EMPTY}$			−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs			12			24	mA
		$\overline{FULL}$, $\overline{EMPTY}$			4			8	
f_{clock}	Clock frequency	LDCK	0		25	0		30	MHz
		UNCK	0		25	0		30	
t_w	Pulse duration	$\overline{RST}$ low	20			15			ns
		LDCK low	15			10			
		LDCK high	25			20			
		UNCK low	15			10			
		UNCK high	25			20			
t_{su}	Setup time	Data before LDCK↑	10			10			ns
		$\overline{RST}$ (inactive) before LDCK↑	5			5			
t_h	Hold time	Data after LDCK↑	5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS232A			SN74ALS232A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	$\overline{FULL}$, $\overline{EMPTY}$	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	$\overline{FULL}$, $\overline{EMPTY}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			75	125		75	125	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS232A			SN54ALS232A		SN74ALS232A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK			40		25		30		MHz
	UNCK			40		25		30		
t_{pd}	LDCK↑	Any Q		30	40	4	50	4	46	ns
t_{pd}	UNCK↑	Any Q		20	27	7	35	7	31	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		17	23	8	29	8	26	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		19	24	10	36	10	29	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$		13	18	5	23	5	20	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		21	26	10	35	10	31	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		17	23	8	28	8	25	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		18	24	8	31	8	28	ns
t_{en}	OE↑	Q		7	12	1	16	1	14	ns
t_{dis}	OE↓	Q		10	16	2	23	2	21	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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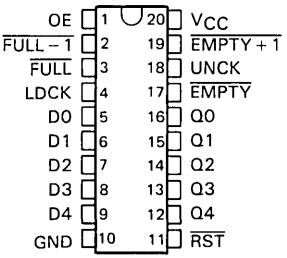
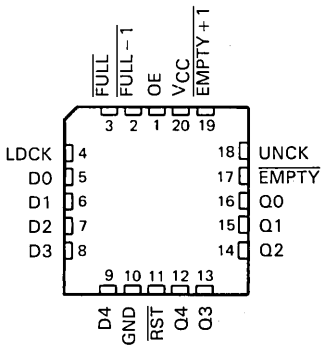
D2876, JANUARY 1986 – REVISED MAY 1986

- Independent Asynchronous Inputs and Outputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- 16 Words by 5 Bits Each
- Data Rates from 0 to 30 MHz
- Fall-Through Time . . . 24 ns Typ
- 3-State Outputs

SN54ALS233A . . . J PACKAGE
SN74ALS233A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS233A . . . FK PACKAGE
SN74ALS233A . . . FN PACKAGE
(TOP VIEW)



description

These 80-bit memories utilize Advanced Low-Power Schottky technology and feature high speed and fast fall-through times. They are organized as 16 words by 5 bits each.

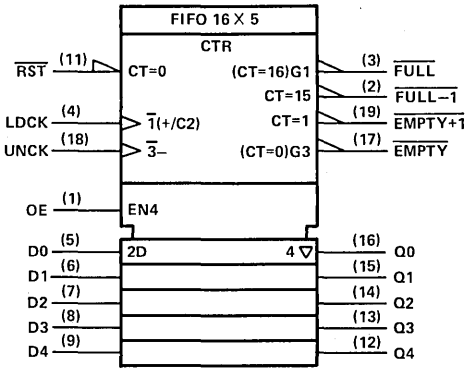
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals will have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, $\overline{\text{FULL}-1}$, and $\overline{\text{EMPTY}+1}$ output flags. The FULL output will be low whenever the memory is full, and high whenever not full. The $\overline{\text{FULL}-1}$ output will be low whenever the memory contains 15 data words. The $\overline{\text{EMPTY}}$ output will be low whenever the memory is empty, and high whenever it is not empty. The $\overline{\text{EMPTY}+1}$ output will be low whenever one word remains in memory.

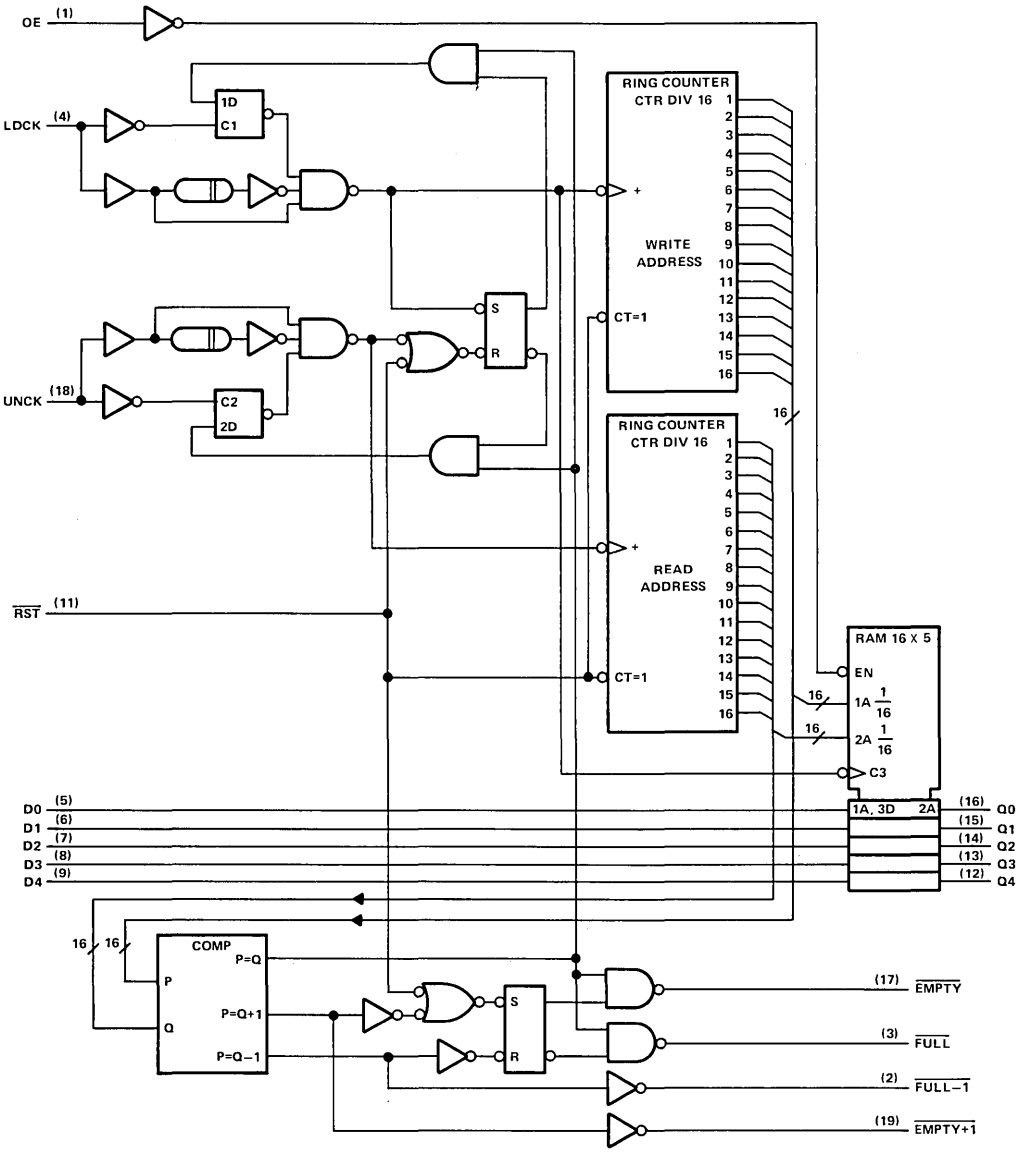
A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$, $\overline{\text{FULL}-1}$, and $\overline{\text{EMPTY}+1}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a $\overline{\text{RST}}$ pulse or from an empty condition, will cause $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

logic symbol†



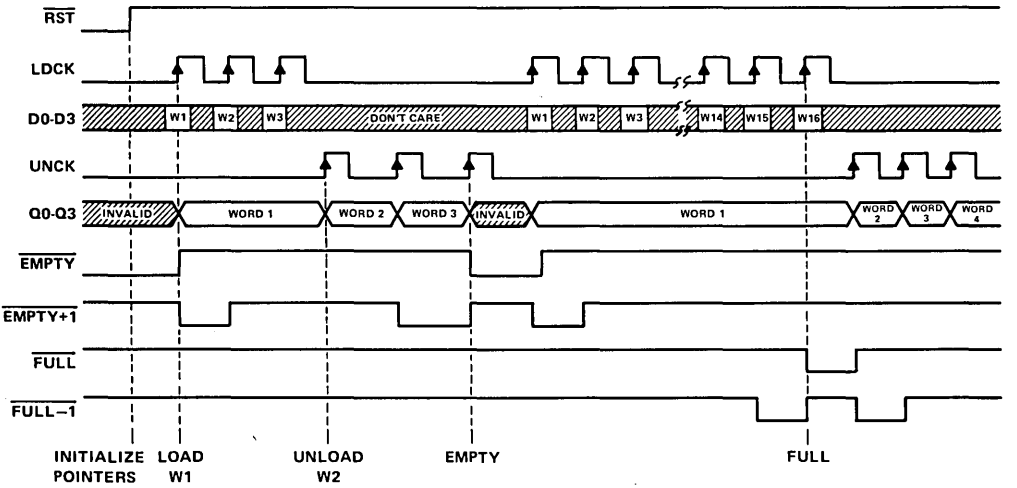
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

logic diagram (positive logic)



Pin numbers are for D, J, and N packages.

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS233A . . . . . −55°C to 125°C
SN74ALS233A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS233A			SN74ALS233A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current	Q outputs			−1			−1.6	mA
		Status flags			−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs			12			24	mA
		Status flags			4			8	
f_{clock}	Clock frequency	LDCK	0		25	0		30	MHz
		UNCK	0		25	0		30	
t_w	Pulse duration	$\overline{RST}$ low	20			15			ns
		LDCK low	15			10			
		LDCK high	25			20			
		UNCK low	15			10			
		UNCK high	25			20			
t_{su}	Setup time	Data before LDCK↑	10			10			ns
		$\overline{RST}$ inactive before LDCK↑	5			5			
t_h	Hold time	Data after LDCK↑	5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS233A			SN74ALS233A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			88	143		88	133	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

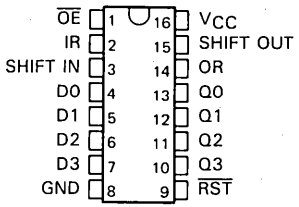
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = −MIN to MAX				UNIT
			'ALS233A			SN54ALS233A		SN74ALS233A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK			40		25		30		MHz
	UNCK			40		25		30		
t_{pd}	LDCK↑	Any Q		24	44	7	52	7	48	ns
t_{pd}	UNCK↑	Any Q		19	29	9	35	9	33	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		18	25	9	30	9	28	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		18	25	9	33	10	30	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$		13	19	6	24	6	22	ns
t_{pd}	LDCK↑	$\overline{EMPTY+1}$		22	31	10	40	10	37	ns
t_{pd}	UNCK↑	$\overline{EMPTY+1}$		22	31	9	40	10	37	ns
t_{PLH}	$\overline{RST}$↓	$\overline{EMPTY+1}$		19	27	8	32	8	31	ns
t_{pd}	LDCK↑	$\overline{FULL-1}$		23	32	11	38	12	36	ns
t_{pd}	UNCK↑	$\overline{FULL-1}$		23	32	11	39	12	36	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL-1}$		20	28	10	34	11	32	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		21	28	10	35	12	33	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		17	24	8	29	9	27	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		18	27	8	32	9	30	ns
t_{en}	OE↑	Q		8	13	1	16	2	15	ns
t_{dis}	OE↓	Q		8	12	2	20	2	17	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

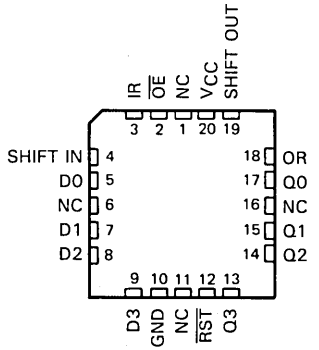
D2958, OCTOBER 1986

- Asynchronous Operation
- Organized as 64 Words of 4 Bits
- Data Rates from 0 to 30 MHz
- 3-State Outputs
- Similar to MMI67401B with Higher Speed and 3-State Outputs
- Dependable Texas Instruments Quality and Reliability

SN54ALS234 . . . J PACKAGE
SN74ALS234 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS234 . . . FK PACKAGE
SN74ALS234. . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN54ALS234 and SN74ALS234 are 256-bit memories utilizing Advanced Low-Power Schottky IMPACT™ Technology. They feature high speed with fast fall-through times and are organized as 64 words by 4 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ALS234 is designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the Shift In input. When Shift In goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional Shift In pulses have no effect. Data is shifted out of memory on the falling edge of the Shift Out input (see Figure 2). When the FIFO is empty, additional Shift Out pulses have no effect. The last data word remains at the outputs until a new word falls through or $\overline{RST}$ goes low.

Status of the 'ALS234 FIFO memory is monitored by the Output Ready (OR) and Input Ready (IR) flags. When the OR flag is high, valid data is available at the outputs. The OR flag is low when Shift Out is high and will stay low when the FIFO is empty. The IR status flag is high when the inputs are ready to receive more data. The IR flag is low when Shift In is high and stays low when the FIFO is full.

When the FIFO is empty, input data is shifted to the output automatically when Shift In goes low. If Shift Out is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

When the FIFO is full, data can be shifted in automatically by holding Shift In high and taking Shift Out low. A propagation delay after Shift Out goes low, IR will go high. If Shift In is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low when the FIFO is full and Shift In is high, only a high-level pulse is seen on the IR output (see Figure 4).

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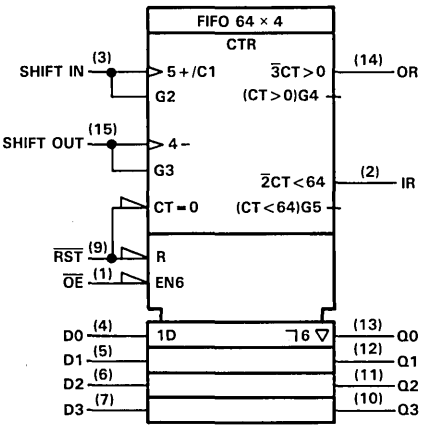
description (continued)

The FIFO must be reset after power up with a low-level pulse on the Master Reset input ($\overline{RST}$). This sets Input Ready (IR) high and Output Ready (OR) low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If Shift In is high when $\overline{RST}$ goes high, the input data is shifted in and IR goes low and remains low until Shift In goes low. If Shift In goes low before $\overline{RST}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs and are at high impedance when Output Enable ($\overline{OE}$) is high. $\overline{OE}$ does not affect the IR and OR outputs.

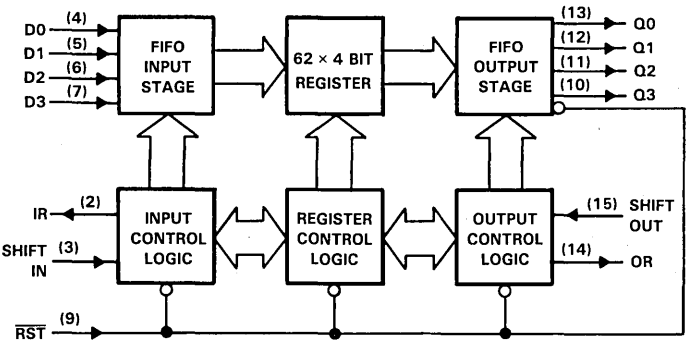
The SN54ALS234 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS234 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Pin numbers shown are for D, J, and N packages.

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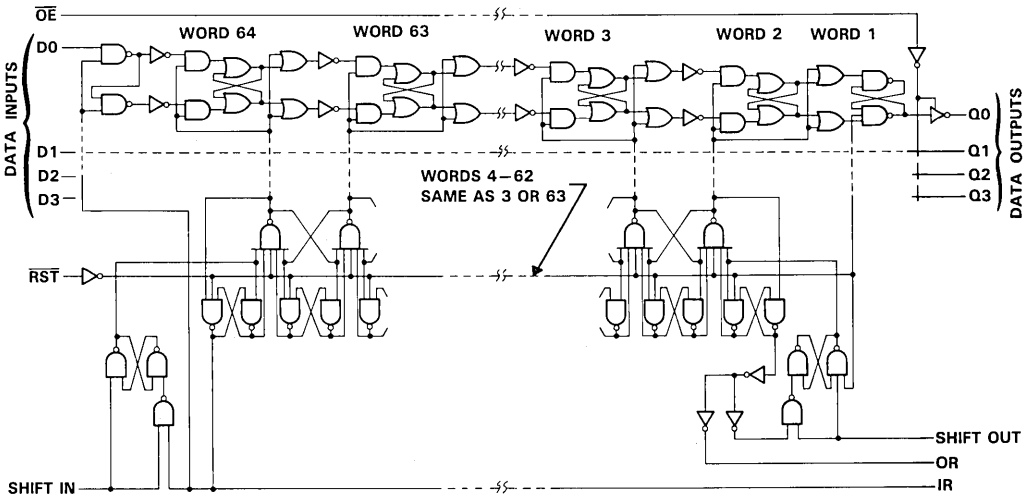
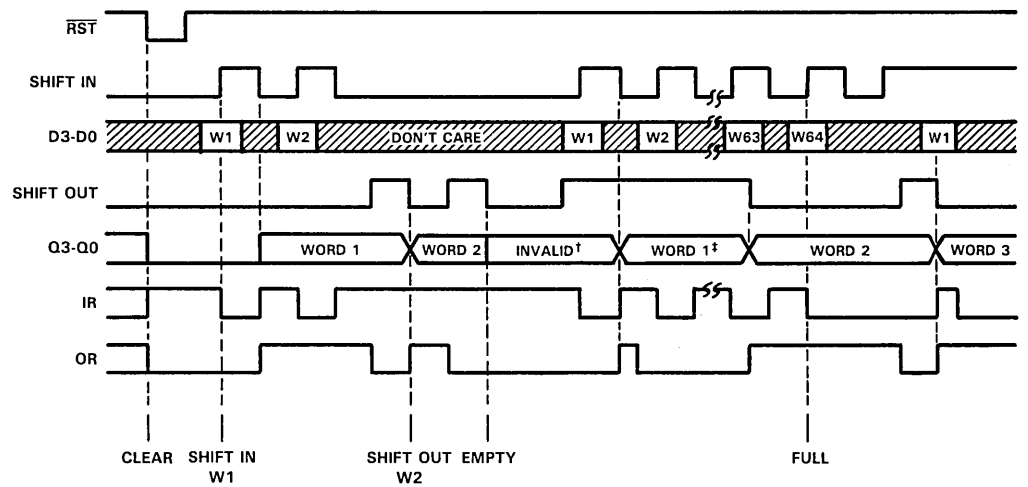
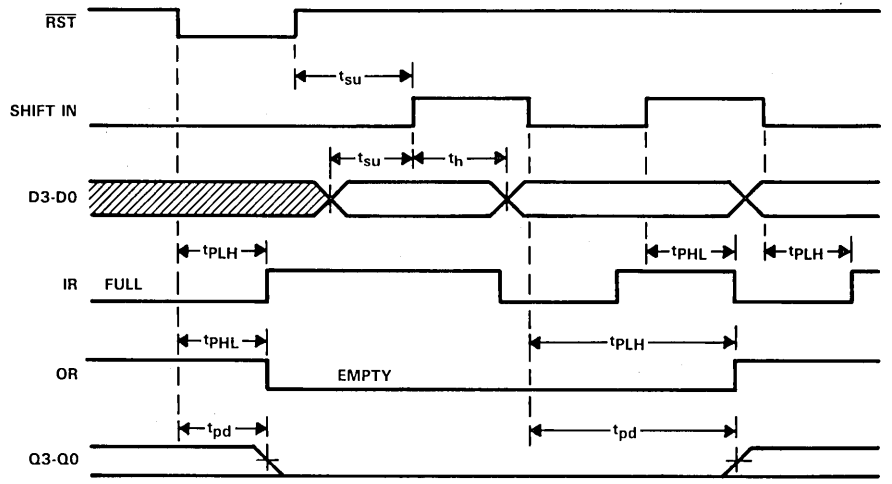
logic diagram (positive logic)



timing diagram

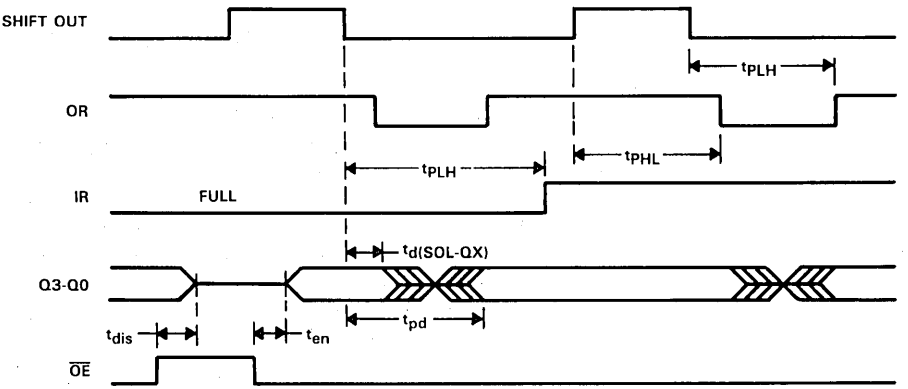


† The last data word shifted out of the FIFO remains at the output until a new word falls through or a $\overline{RST}$ pulse clears the FIFO.
‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the output. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until Shift Out is taken low.



NOTE: SHIFT OUT is low

FIGURE 1. MASTER RESET AND DATA IN WAVEFORMS



NOTE: SHIFT IN is low

FIGURE 2. DATA OUT WAVEFORMS

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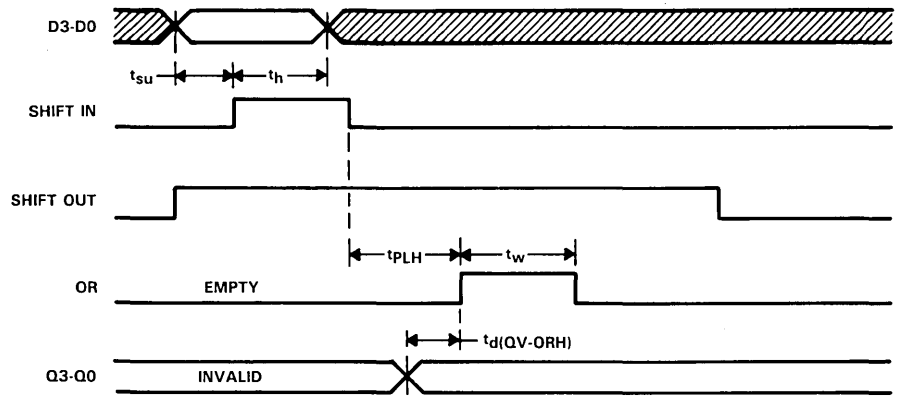

FIGURE 3. DATA FALL THROUGH WAVEFORMS

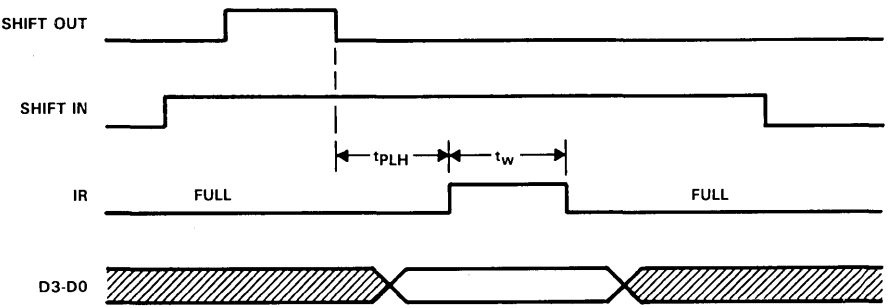

FIGURE 4. AUTOMATIC DATA IN WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS234 . . . . . −55°C to 125°C
SN74ALS234 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS234			SN74ALS234			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Q outputs			−1			−2.6	mA
		IR and OR			−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs			12			24	mA
		IR and OR			4			8	
f_{clock}	Clock frequency	SHIFT IN or SHIFT OUT	0		25	0		30	MHz
t_w	Pulse duration	SHIFT IN or SHIFT OUT high or low	17			15			ns
		$\overline{RST}$ low	20			15			
t_{su}	Setup time before SHIFT IN ↑	Data	0			0			ns
		$\overline{RST}$ high (inactive)	15			15			
t_h	Hold time, data after SHIFT IN ↑		19			17			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS234			SN74ALS234			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Q	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
	IR, OR	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		
V_{OL}	Q	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	IR, OR	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.4		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	I_{CCL}		100	155		100	145	mA
			I_{CCH}		97	152		97	142	
			I_{CCZ}		103	158		103	148	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS234			SN54ALS234		SN74ALS234		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	SHIFT IN			35		25		30		MHz
	SHIFT OUT			35		25		30		
t_w†	IR high			15		7		8		ns
t_w‡	OR high			19		7		8		ns
$t_{d(QV-ORH)}$	Q valid before OR ↑			6	9	−5	12	−5	12	ns
$t_{d(SOL-QX)}$	Q valid after SHIFT OUT ↓			13		4		4		ns
t_{pd}	SHIFT IN ↓	Q		600	800	350	1200	350	1000	ns
t_{PHL}	SHIFT IN ↑	IR		20	26	8	36	8	30	ns
t_{PLH}	SHIFT IN ↓	IR		16	21	6	28	6	25	ns
t_{PLH}§	SHIFT IN ↓	OR		600	800	350	1200	350	1000	ns
t_{pd}	SHIFT OUT ↓	Q		13	17	4	24	4	22	ns
t_{PHL}	SHIFT OUT ↑	OR		23	27	7	39	7	33	ns
t_{PLH}	SHIFT OUT ↓	OR		20	24	6	33	6	30	ns
t_{PLH}§	SHIFT OUT ↓	IR		600	800	350	1200	350	1000	ns
t_{PHL}	$\overline{RST}$ ↓	OR		22	26	10	40	10	34	ns
t_{PLH}	$\overline{RST}$ ↓	IR		17	21	6	31	6	27	ns
t_{PHL}	$\overline{RST}$ ↓	Q		14	17	5	21	5	19	ns
t_{dis}	$\overline{OE}$ ↑	Q		7	13	2	16	2	15	ns
t_{en}	$\overline{OE}$ ↓	Q		6	12	2	15	2	13	ns

† The IR output pulse occurs when the FIFO is full, Shift In is high, and Shift Out is pulsed (see Figure 4).
‡ The OR output pulse occurs when the FIFO is empty, Shift Out is high, and Shift In is pulsed (see Figure 3).
§ Data throughput or "fall through" times
NOTE 1: Load circuit and voltage waveforms are shown in Section 1 of the *LSI Logic Data Book*, 1986.

TYPICAL APPLICATION INFORMATION

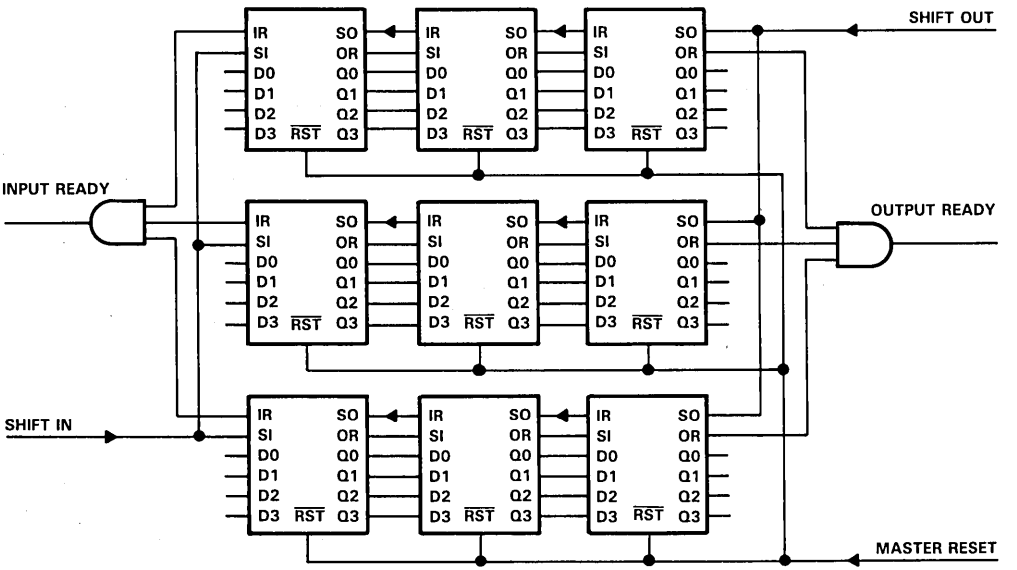
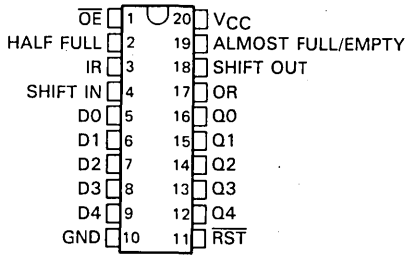


FIGURE 5. 192-WORD BY 12-BIT EXPANSION

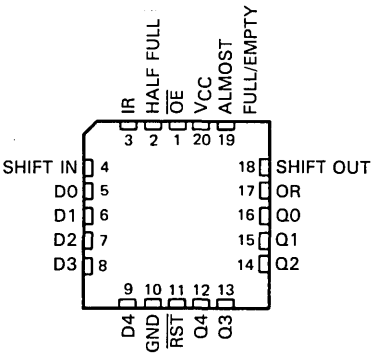
D2958, OCTOBER 1986

- **Asynchronous Operation**
- **Organized as 64 Words of 5 Bits**
- **Data Rates from 0 to 25 MHz**
- **3-State Outputs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS235 . . . J PACKAGE
SN74ALS235 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS235 . . . FK PACKAGE
SN74ALS235. . . FN PACKAGE
(TOP VIEW)



description

The SN54ALS235 and SN74ALS235 are 320-bit memories utilizing Advanced Low-Power Schottky IMPACT™ Technology. They feature high speed with fast fall-through times and are organized as 64 words by 5 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ALS235 is designed to process data at rates from 0 to 25 megahertz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the Shift In input. When Shift In goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional Shift In pulses have no effect. Data is shifted out of memory on the falling edge of the Shift Out input (see Figure 2). When the FIFO is emply, additional Shift Out pulses have no effect. The last data word remains at the outputs until a new word falls through or $\overline{RST}$ goes low.

Status of the 'ALS235 FIFO memory is monitored by the Output Ready (OR), Input Ready (IR), Almost Full/Empty, and Half Full flags. When the OR flag is high, valid data is available at the outputs. The OR flag is low when Shift Out is high and will stay low when the FIFO is empty. The IR status flag is high when the inputs are ready to receive more data. The IR flag is low when Shift In is high and stays low when the FIFO is full. The Almost Full/Empty flag is high when the FIFO contains eight or less words (see Figure 5), or fifty-six or more words (see Figure 6). The Almost Full/Empty flag is low when the FIFO contains between nine and fifty-five words. The Half Full flag is high when the FIFO contains thirty-two or more words, and is low when the FIFO contains thirty-one words or less (see Figure 7).

When the FIFO is empty, input data is shifted to the output automatically when Shift In goes low. If Shift Out is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

When the FIFO is full, data can be shifted in automatically by holding Shift In high and taking Shift Out low. A propagation delay after Shift Out goes low, IR will go high. If Shift In is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low, when the FIFO is full and Shift In is high, only a high-level pulse is seen on the IR output.

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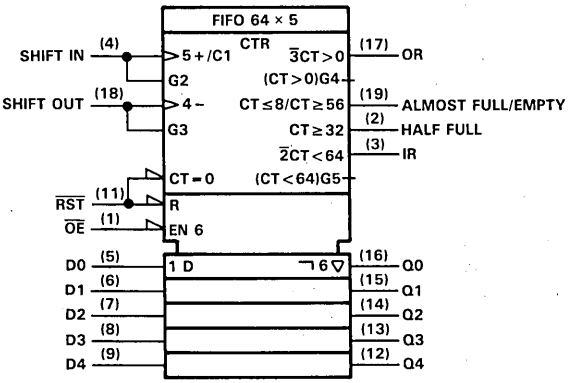
description (continued)

The FIFO must be reset after power up with a low-level pulse on the Master Reset input ($\overline{RST}$). This sets Input Ready (IR) high and Output Ready (OR) low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If Shift In is high when $\overline{RST}$ goes high, the input data is shifted in and IR goes low and remains low until Shift In goes low. If Shift In goes low before $\overline{RST}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs and are at high impedance when Output Enable ($\overline{OE}$) is high. $\overline{OE}$ does not affect the status flag outputs (see Figure 2).

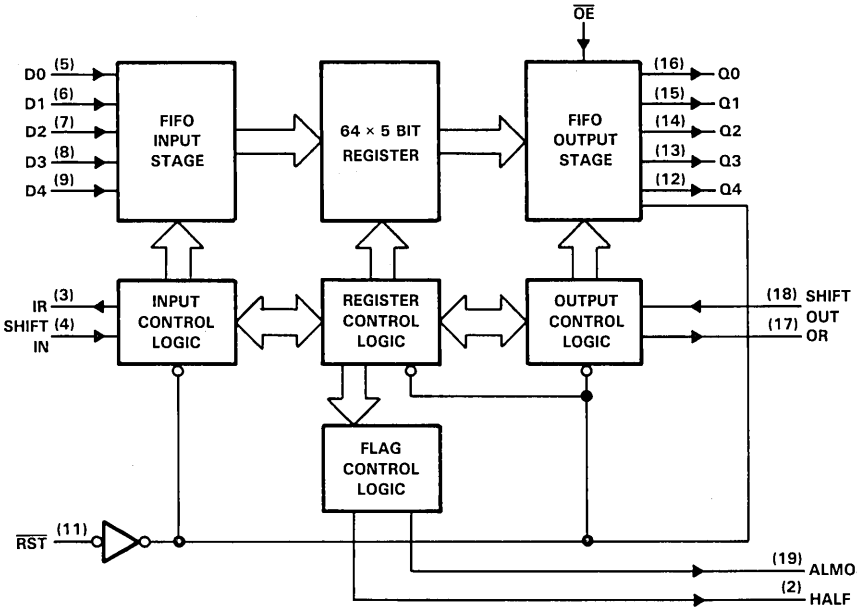
The SN54ALS235 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS235 is characterized for operation from 0°C to 70°C.

logic symbol†

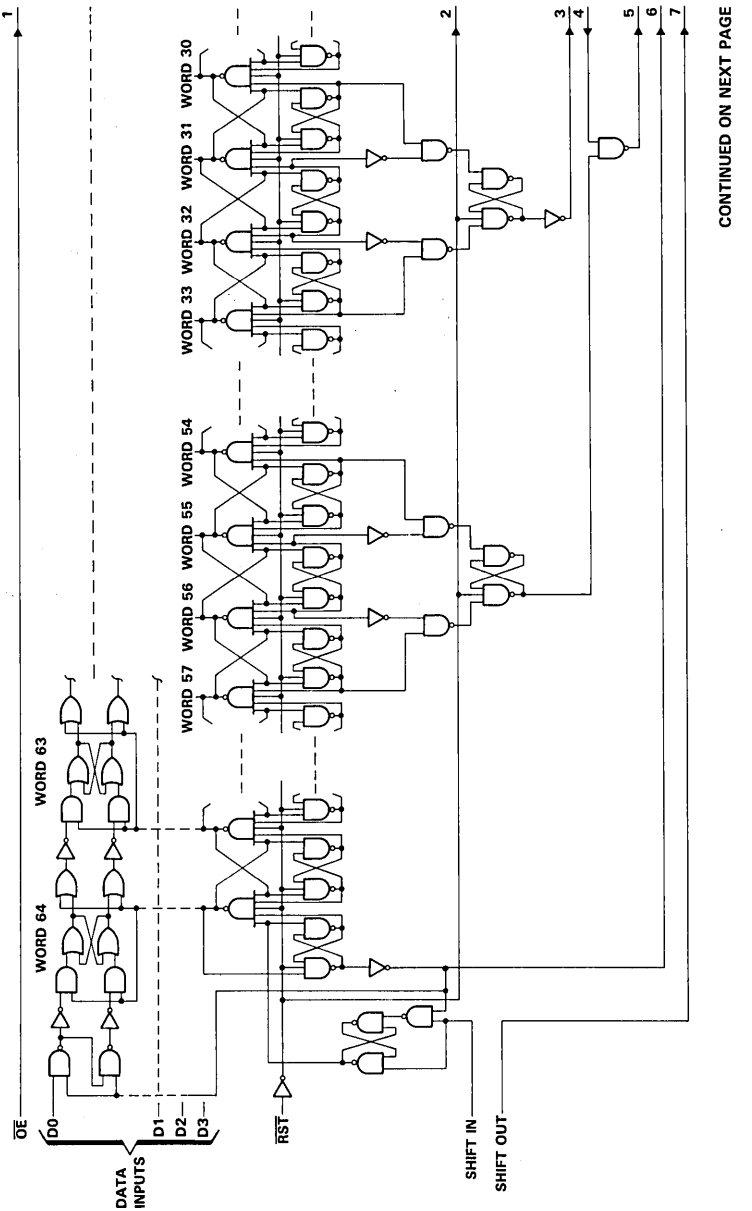


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

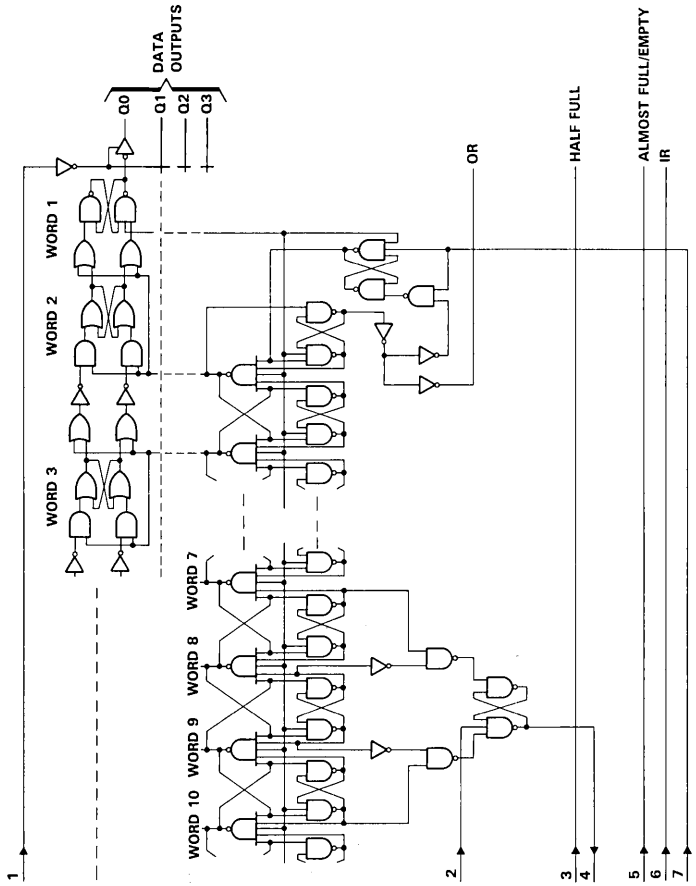
functional block diagram



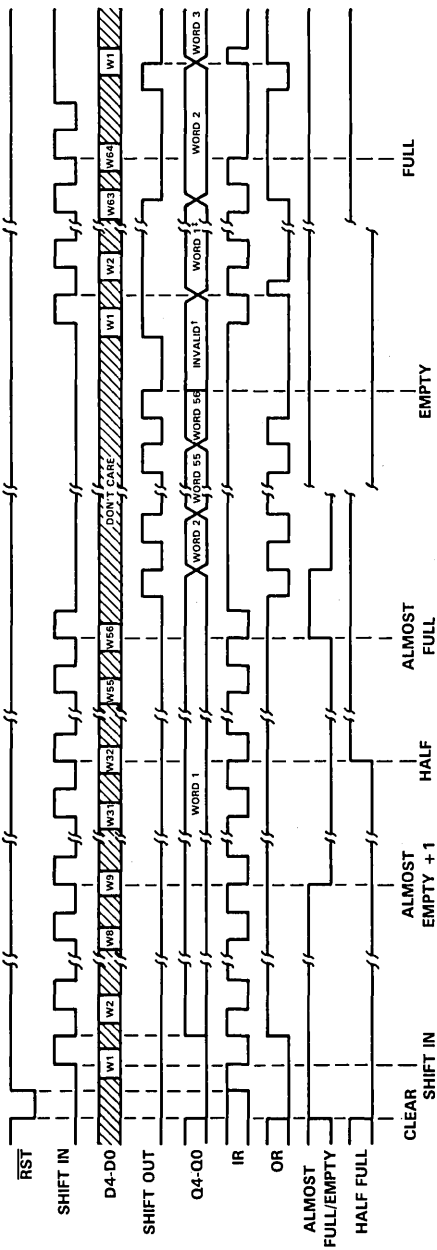
logic diagram (positive logic)



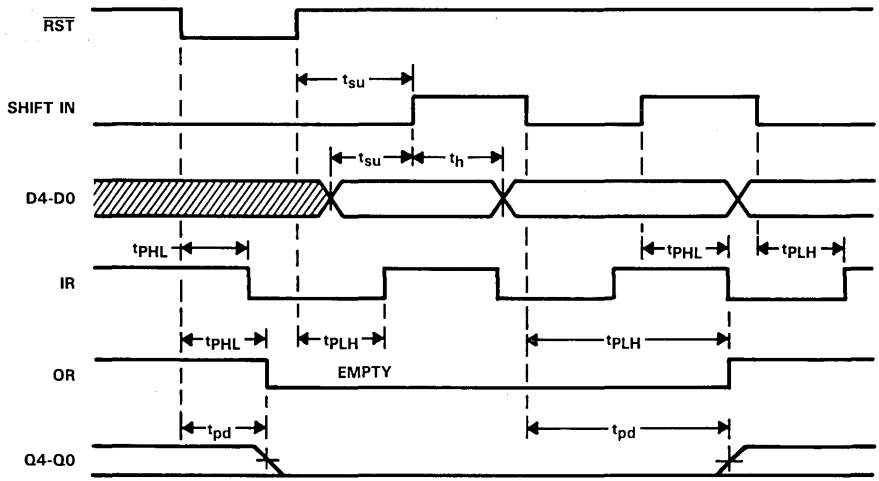
logic diagram (positive logic) (continued)



timing diagram

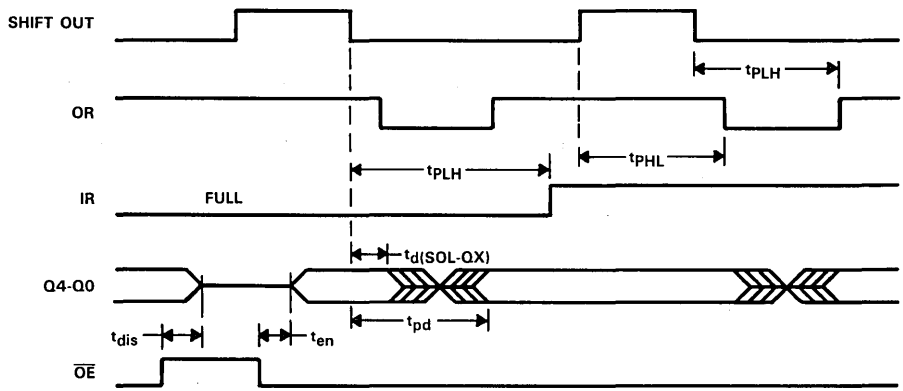


† The last data word shifted out of the FIFO remains at the output until a new word falls through or a $\overline{RST}$ pulse clears the FIFO.
‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the output. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until Shift Out is taken low.



NOTE: SHIFT OUT is low

FIGURE 1. MASTER RESET AND DATA IN WAVEFORMS



NOTE: SHIFT IN is low

FIGURE 2. DATA OUT WAVEFORMS

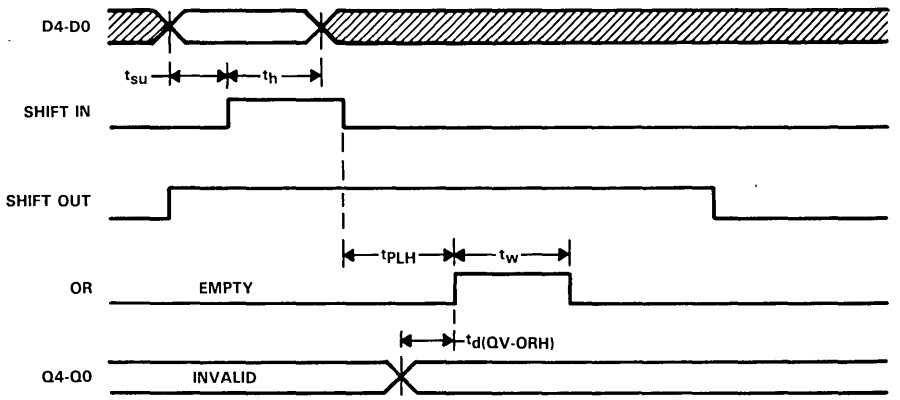


FIGURE 3. DATA FALL THROUGH WAVEFORMS

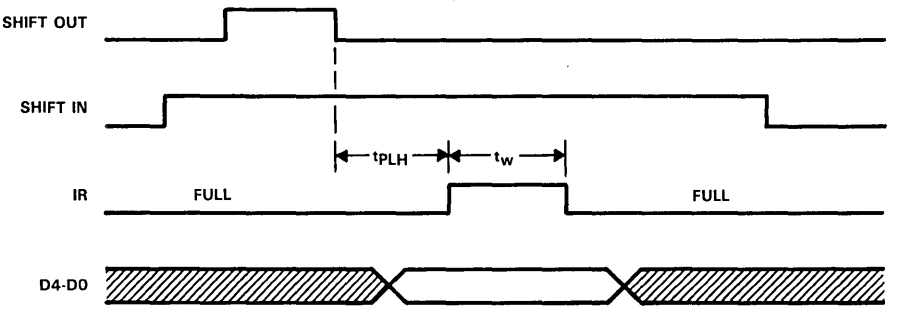


FIGURE 4. AUTOMATIC DATA IN WAVEFORMS

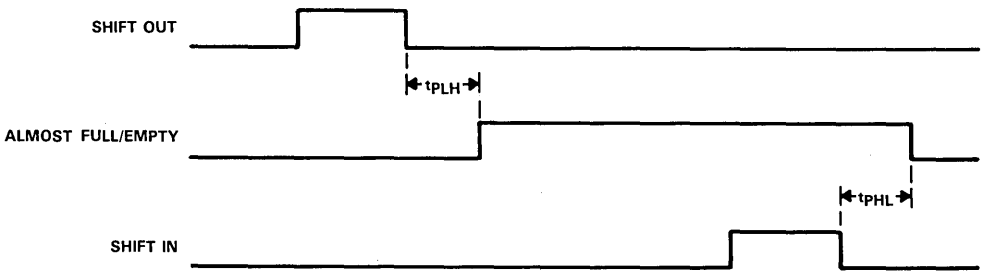


FIGURE 5. ALMOST EMPTY WAVEFORMS

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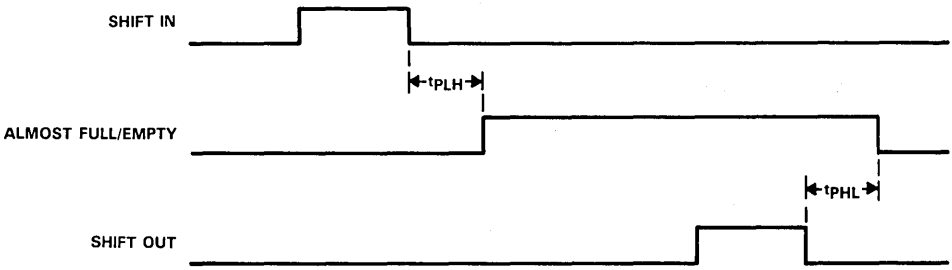

FIGURE 6. ALMOST FULL WAVEFORMS

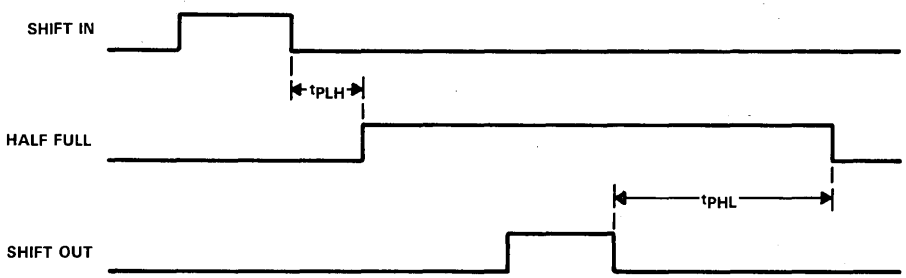

FIGURE 7. HALF FULL WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS235 . . . . . −55°C to 125°C
SN74ALS235 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS235			SN74ALS235			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Q outputs			−1			−2.6	mA
		Flags			−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs			12			24	mA
		Flags			4			8	
f_{clock}	Clock frequency	SHIFT IN or SHIFT OUT	0		20	0		25	MHz
t_w	Pulse duration	SHIFT IN or SHIFT OUT high or low	17			15			ns
		$\overline{RST}$ low	20			15			
t_{su}	Setup time before SHIFT IN ↑	Data	0			0			ns
		$\overline{RST}$ high (inactive)	15			15			
t_h	Hold time, data after SHIFT IN ↑		19			17			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS235			SN74ALS235			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Q	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
	Flags	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		
V_{OL}	Q	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	Flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.4		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	I_{CCL}		112	175		112	165	mA
			I_{CCH}		105	170		105	160	
			I_{CCZ}		115	180		115	170	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS235			SN54ALS235		SN74ALS235		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	SHIFT IN			30		20		25		MHz
	SHIFT OUT			30		20		25		
t_w†	IR high			15		7		8		ns
t_w‡	OR high			19		7		8		ns
$t_{d(QV-ORH)}$	Q valid before OR ↑			6	9	−5	12	−5	12	ns
$t_{d(SOL-QX)}$	Q valid after SHIFT OUT ↓			13		4		4		ns
t_{pd}	SHIFT IN ↓	Q		600	800	350	1200	350	1000	ns
t_{PHL}	SHIFT IN ↑	IR		20	26	8	36	8	30	ns
t_{PLH}	SHIFT IN ↓	IR		16	21	6	28	6	25	ns
t_{PLH}§	SHIFT IN ↓	OR		600	800	350	1200	350	1000	ns
t_{PHL}	SHIFT IN ↓	ALMOST F/E		550	700	290	1050	290	880	ns
t_{PLH}	SHIFT IN ↓	ALMOST F/E		85	115	40	170	40	150	ns
t_{PLH}	SHIFT IN ↓	HALF FULL		340	410	180	590	180	510	ns
t_{pd}	SHIFT OUT ↓	Q		13	17	4	24	4	22	ns
t_{PHL}	SHIFT OUT ↑	OR		23	27	7	39	7	33	ns
t_{PLH}	SHIFT OUT ↓	OR		20	24	6	33	6	30	ns
t_{PLH}§	SHIFT OUT ↓	IR		600	800	350	1200	350	1000	ns
t_{PHL}	SHIFT OUT ↓	ALMOST F/E		550	700	290	1050	290	880	ns
t_{PLH}	SHIFT OUT ↓	ALMOST F/E		85	115	35	170	35	150	ns
t_{PHL}	SHIFT OUT ↓	HALF FULL		340	410	170	590	170	510	ns
t_{PHL}	$\overline{RST}$ ↓	OR		22	26	10	40	10	34	ns
t_{PLH}	$\overline{RST}$ ↑	IR		12	18	5	24	5	22	ns
t_{PHL}	$\overline{RST}$ ↓	IR		12	18	5	24	5	22	ns
t_{PHL}	$\overline{RST}$ ↓	Q		14	17	5	21	5	19	ns
t_{dis}	$\overline{OE}$ ↑	Q		7	13	2	16	2	15	ns
t_{en}	$\overline{OE}$ ↓	Q		6	12	2	15	2	13	ns

† The IR output pulse occurs when the FIFO is full, Shift In is high, and Shift Out is pulsed (see Figure 4).
‡ The OR output pulse occurs when the FIFO is empty, Shift Out is high, and Shift In is pulsed (see Figure 3).
§ Data throughput or "fall through" times
NOTE 1: Load circuit and voltage waveforms are shown in Section 1 of the *LSI Logic Data Book*, 1986.

TYPICAL APPLICATION INFORMATION

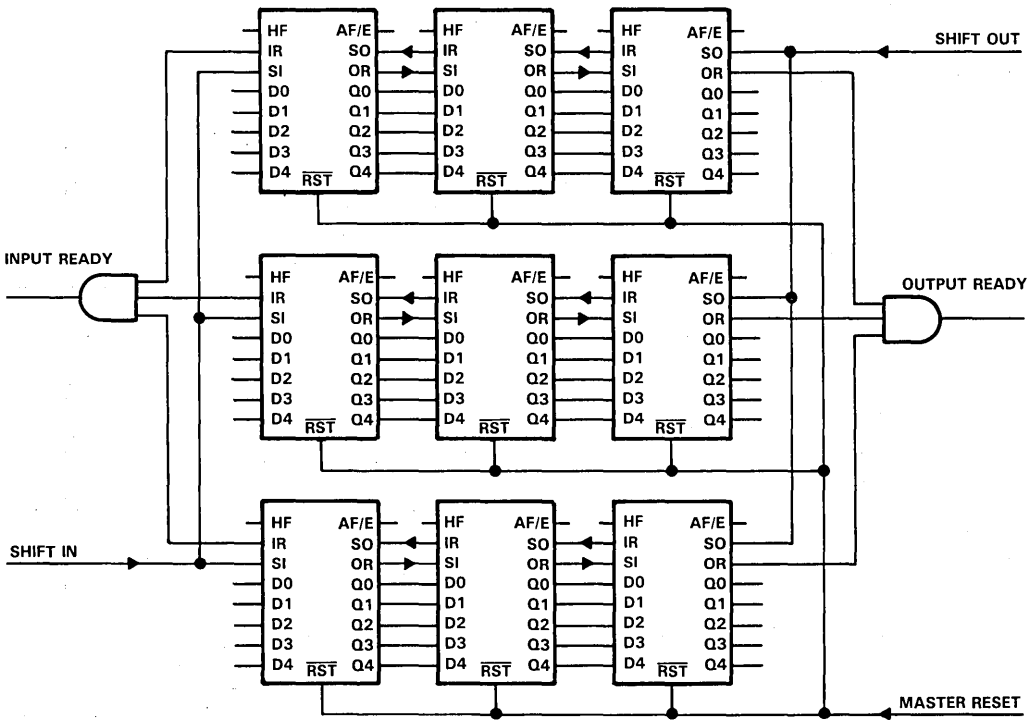

FIGURE 8. 192-WORD BY 15-BIT EXPANSION

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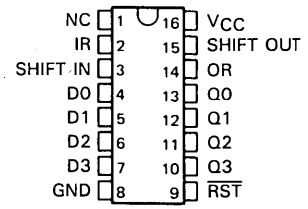
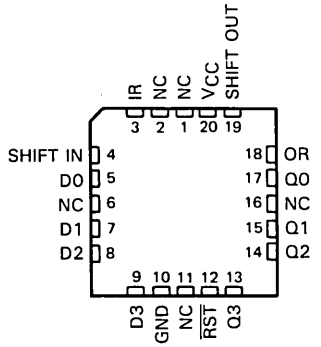
D2958, OCTOBER 1986

- Asynchronous Operation
- Organized as 64 Words of 4 Bits
- Data Rates from 0 to 30 MHz
- Pin-Compatible with MMI67401B with Higher Speed
- Dependable Texas Instruments Quality and Reliability

SN54ALS236 . . . J PACKAGE
SN74ALS236 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS236 . . . FK PACKAGE
SN74ALS236. . . FN PACKAGE
(TOP VIEW)



NC—No internal connection.

description

The SN54ALS236 and SN74ALS236 are 256-bit memories utilizing Advanced Low-Power Schottky IMPACT™ Technology. They feature high speed with fast fall-through times and are organized as 64 words by 4 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ALS236 is designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the Shift In input. When Shift In goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional Shift In pulses have no effect. Data is shifted out of memory on the falling edge of the Shift Out input (see Figure 2). When the FIFO is empty, additional Shift Out pulses have no effect. The last data word remains at the outputs until a new word falls through or $\overline{RST}$ goes low

Status of the 'ALS236 FIFO memory is monitored by the Output Ready (OR) and Input Ready (IR) flags. When the OR flag is high, valid data is available at the outputs. The OR flag is low when Shift Out is high and will stay low when the FIFO is empty. The IR status flag is high when the inputs are ready to receive more data. The IR flag is low when Shift In is high and stays low when the FIFO is full.

When the FIFO is empty, input data is shifted to the output automatically when Shift In goes low. If Shift Out is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

When the FIFO is full, data can be shifted in automatically by holding Shift In high and taking Shift Out low. A propagation delay after Shift Out goes low, IR will go high. If Shift In is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low when the FIFO is full and Shift In is high, only a high-level pulse is seen on the IR output (see Figure 4).

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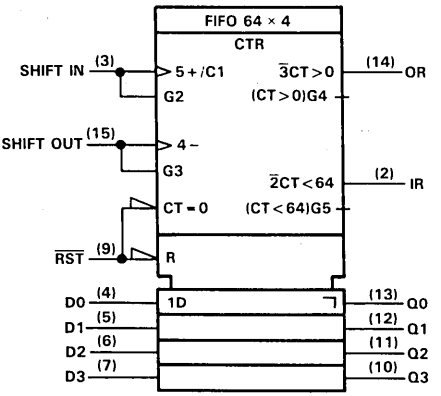
description (continued)

The FIFO must be reset after power up with a low-level pulse on the Master Reset input ($\overline{RST}$). This sets Input Ready (IR) high and Output Ready (OR) low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If Shift In is high when $\overline{RST}$ goes high, the input data is shifted in and IR goes low and remains low until Shift In goes low. If Shift In goes low before $\overline{RST}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs.

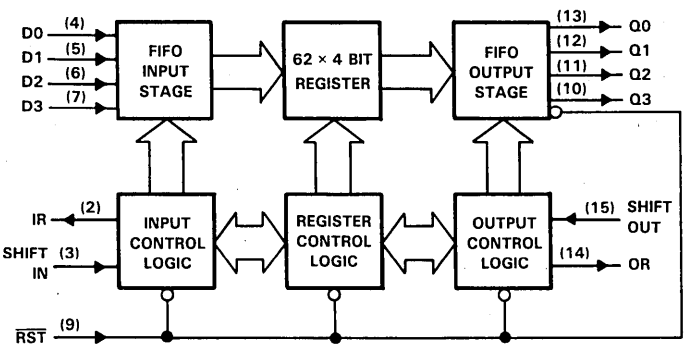
The SN54ALS236 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS236 is characterized for operation from 0°C to 70°C.

logic symbol†



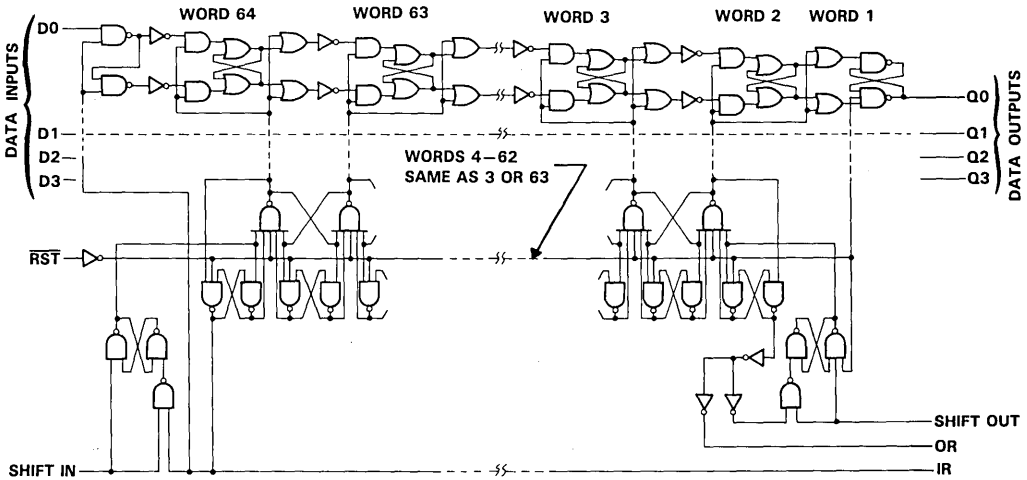
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram

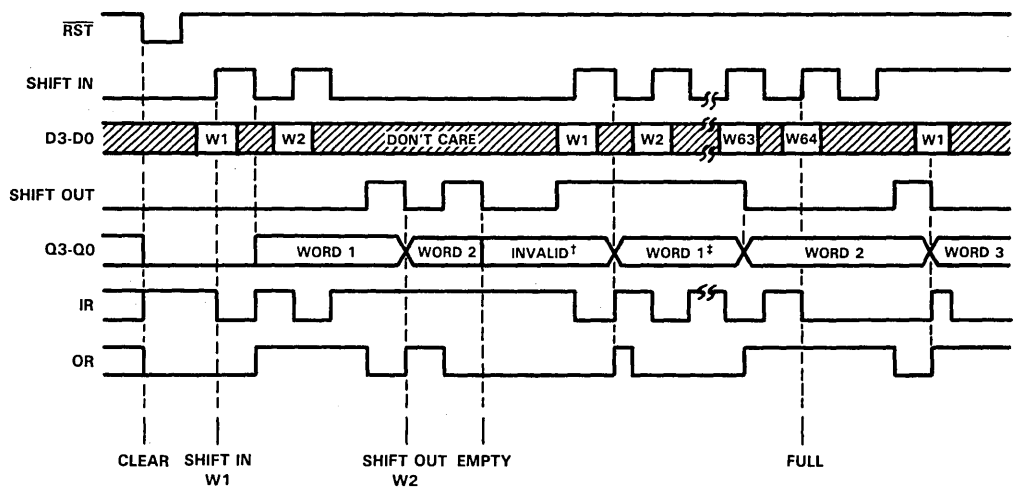


Pin numbers shown are for D, J, and N packages.

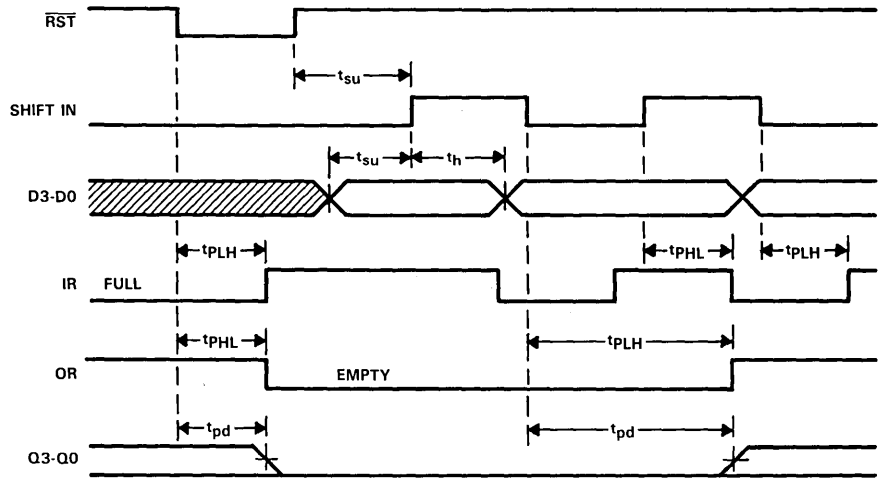
logic diagram (positive logic)



timing diagram

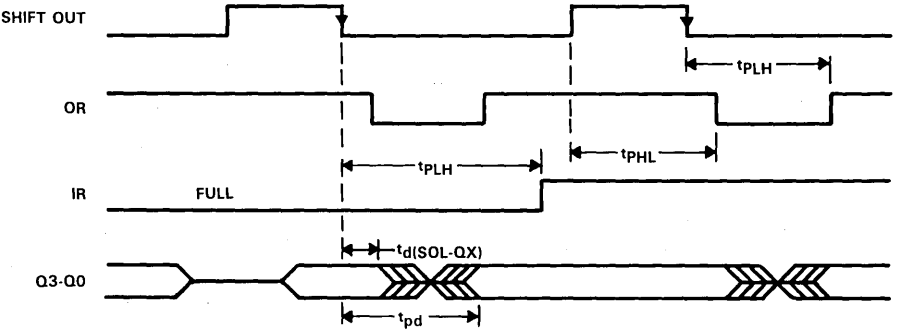


† The last data word shifted out of the FIFO remains at the output until a new word falls through or a $\overline{RST}$ pulse clears the FIFO.
‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the output. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until SHIFT OUT is taken low.



NOTE: SHIFT OUT is low

FIGURE 1. MASTER RESET AND DATA IN WAVEFORMS



NOTE: SHIFT IN is low

FIGURE 2. DATA OUT WAVEFORMS

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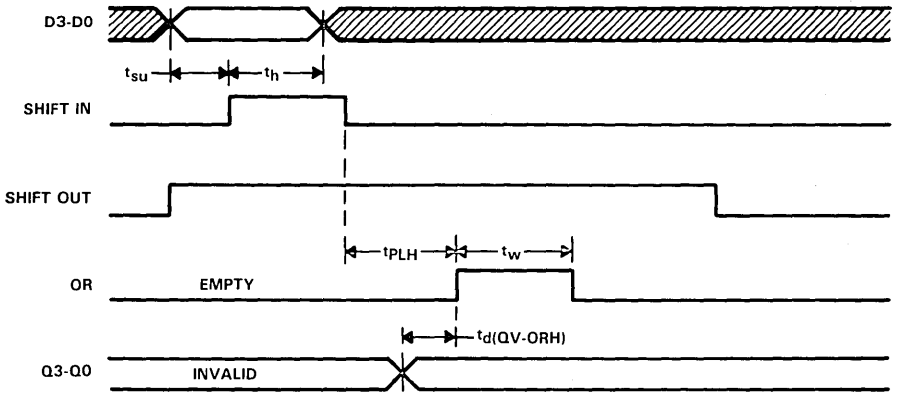

FIGURE 3. DATA FALL THROUGH WAVEFORMS

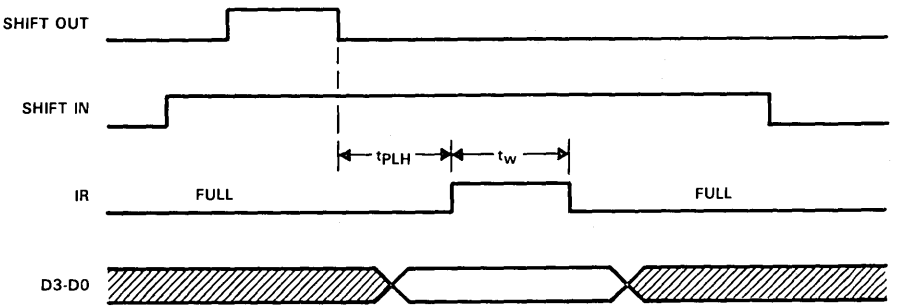

FIGURE 4. AUTOMATIC DATA IN WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS236 . . . . . −55°C to 125°C
SN74ALS236 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS236			SN74ALS236			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Q outputs			−1			−2.6	mA
		IR and OR			−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs			12			24	mA
		IR and OR			4			8	
f_{clock}	Clock frequency	SHIFT IN or SHIFT OUT	0		25	0		30	MHz
t_w	Pulse duration	SHIFT IN or SHIFT OUT high or low	17			15			ns
		$\overline{RST}$ low	20			15			
t_{su}	Setup time before SHIFT IN ↑	Data	0			0			ns
		$\overline{RST}$ high (inactive)	15			15			
t_h	Hold time, data after SHIFT IN ↑		19			17			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS236			SN74ALS236			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Q	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					V
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
	IR, OR	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		
V_{OL}	Q	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	IR, OR	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.4		0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	I_{CCL}		100	155		100	145	mA
			I_{CCH}		97	152		97	142	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS236			SN54ALS236		SN74ALS236		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	SHIFT IN			35		25		30		MHz
	SHIFT OUT			35		25		30		
t_w†	IR high			15		7		8		ns
t_w‡	OR high			19		7		8		ns
$t_{d(QV-ORH)}$	Q valid before OR ↑			6	9	−5	12	−5	12	ns
$t_{d(SOL-QX)}$	Q valid after SHIFT OUT ↓			13		4		4		ns
t_{pd}	SHIFT IN ↓	Q		600	800	350	1200	350	1000	ns
t_{PHL}	SHIFT IN ↑	IR		20	26	8	36	8	30	ns
t_{PLH}	SHIFT IN ↓	IR		16	21	6	28	6	25	ns
t_{PLH}§	SHIFT IN ↓	OR		600	800	350	1200	350	1000	ns
t_{pd}	SHIFT OUT ↓	Q		13	17	4	24	4	22	ns
t_{PHL}	SHIFT OUT ↑	OR		23	27	7	39	7	33	ns
t_{PLH}	SHIFT OUT ↓	OR		20	24	6	33	6	30	ns
t_{PLH}§	SHIFT OUT ↓	IR		600	800	350	1200	350	1000	ns
t_{PHL}	$\overline{RST}$ ↓	OR		22	26	10	40	10	34	ns
t_{PLH}	$\overline{RST}$ ↓	IR		17	21	6	31	6	27	ns
t_{PHL}	$\overline{RST}$ ↓	Q		14	17	5	21	5	19	ns

† The IR output pulse occurs when the FIFO is full, Shift In is high, and Shift Out is pulsed (see Figure 4).
‡ The OR output pulse occurs when the FIFO is empty, Shift Out is high, and Shift In is pulsed (see Figure 3).
§ Data Throughput or "fall through" times
NOTE 1: Load circuit and voltage waveforms are shown in Section 1 of the *LSI Logic Data Book*, 1986.

TYPICAL APPLICATION INFORMATION

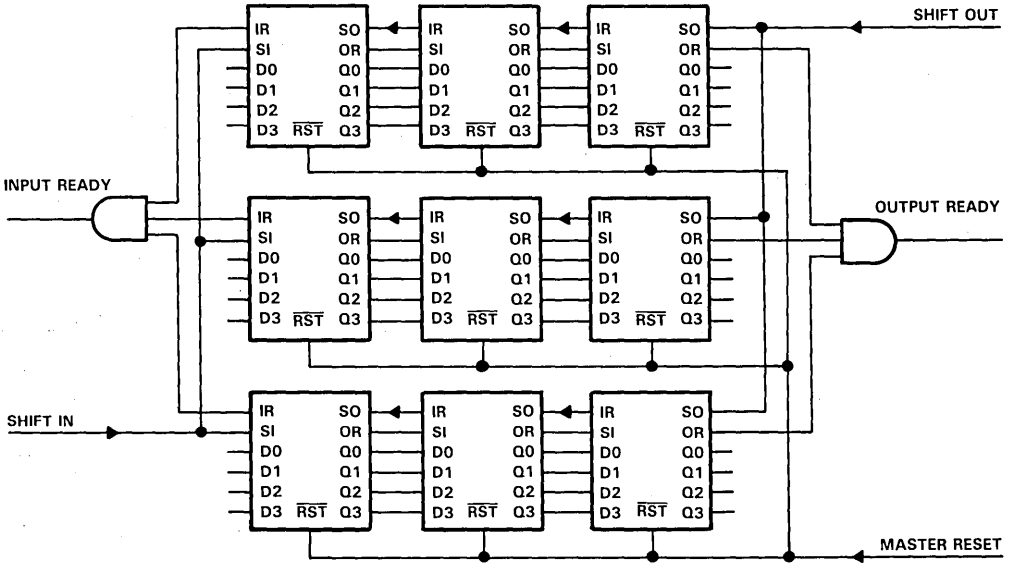
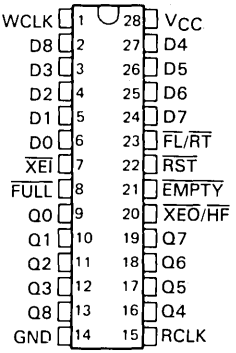


FIGURE 5. 192-WORD BY 12-BIT EXPANSION

D3101, MARCH 1988

- Asynchronous Operation
- Organized as 512 Words of 9 Bits
- Lower Power Consumption
  Active . . . 400 mW
  Power Down . . . 3 mW
  Standby . . . 44 mW
- Fully Expandable in Word Width and/or Word Depth
- Designed to be Compatible with IDT7201A But with Lower Power Consumption
- EPIC™ (Enhanced Performance Implanted CMOS) 1-µm Process
- Reliable Advanced CMOS Technology
- Fully TTL-Compatible

SN74ACT7201A . . . N PACKAGE
(TOP VIEW)



For chip carrier information contact the factory.

description

This 4608-bit memory uses Advanced CMOS Technology and features high speed and fast fall-through times. The 'ACT7201A is organized as 512 words by 9 bits each.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The function is used as a buffer to couple two buses operating at different clock rates. The 'ACT7201A is designed to process data at rates from 0 to 28.5 MHz in a bit-parallel format, word by word.

Data is written into the memory on a low-to-high transition at the Write Clock (WCLK) input, and is read out of the memory on a high-to-low transition at the Read Clock (RCLK) input, (see Figure 1). The data outputs are noninverting with respect to the data inputs and are in a high-impedance state when RCLK is high. The memory is full when the number of words clocked in exceeds by 512 the number of words clocked out. When the memory is full, write signals have no effect on the data residing in memory. When the memory is empty, read signals have no effect, and the data outputs remain in a high-impedance state.

Status of the FIFO memory is monitored by the Full Flag ($\overline{\text{FULL}}$), Empty Flag ($\overline{\text{EMPTY}}$), and Expansion Enable Out/Half Full Flag ($\overline{\text{XEO}}/\overline{\text{HF}}$). The $\overline{\text{FULL}}$ output is low when the memory is full, and high when the memory is not full (see Figure 2). The $\overline{\text{EMPTY}}$ output is low when the memory is empty, and high when it is not empty (see Figure 3). When cascading two or more devices for word-depth expansion, $\overline{\text{XEO}}/\overline{\text{HF}}$ functions as an Expansion Enable Out output. When the 'ACT7201A is used as a 512-word FIFO memory (no word-depth expansion), the $\overline{\text{XEO}}/\overline{\text{HF}}$ output functions as a Half Full Flag. This 512-word memory mode is defined by grounding the Expansion Enable In ($\overline{\text{XEI}}$) input of the device. In this mode, $\overline{\text{XEO}}/\overline{\text{HF}}$ is low whenever the FIFO contains 257 or more words, and is high whenever the FIFO contains 256 or less words (see Figure 8).

The First Load/Retransmit ($\overline{\text{FL}}/\overline{\text{RT}}$) input performs two separate functions. When cascading two or more devices for word-depth expansion, $\overline{\text{FL}}/\overline{\text{RT}}$ functions as a first-load input and is grounded on the first device in the daisy chain to indicate that it is the first device loaded and unloaded. When the 'ACT7201A is used as a 512-word FIFO memory, the $\overline{\text{FL}}/\overline{\text{RT}}$ input performs the retransmit function. In this mode, a low-level pulse on the $\overline{\text{FL}}/\overline{\text{RT}}$ input resets the read pointer to the first memory location to allow for retransmission from the beginning of data entered. The write pointer is not affected by the $\overline{\text{FL}}/\overline{\text{RT}}$ input. RCLK and WCLK must be at a high level during the low-level $\overline{\text{FL}}/\overline{\text{RT}}$ retransmit pulse (see Figure 4). The retransmit operation will affect the value of the Half Full Flag ($\overline{\text{XEO}}/\overline{\text{HF}}$) by changing the position of the read pointer relative to the write pointer.

The retransmit feature should be used only when less than 512 writes are performed between resets, otherwise, an attempt to retransmit may cause loss of some data that has not yet been read.

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description (continued)

When the FIFO is empty, a data word can be read automatically at the Q outputs by holding RCLK low when loading in the data word with a low-level pulse on the WCLK (see Figure 5).

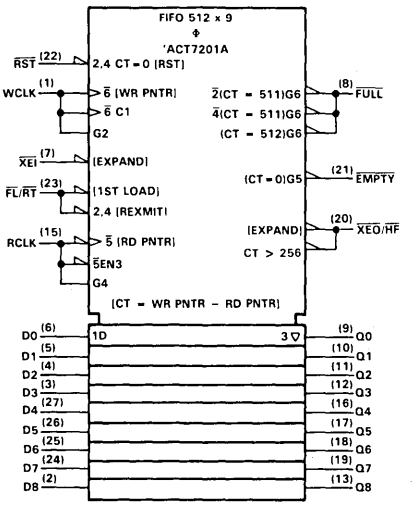
When the FIFO is full, a data word can be written automatically into memory by holding WCLK low while reading out another data word with a low-level pulse on RCLK (see Figure 6).

The FIFO must be reset after power up with a low level pulse on the Reset ($\overline{RST}$) input. This resets the read and write internal stack control pointers to the first memory location, and also sets $\overline{EMPTY}$ low, $\overline{FULL}$ high, and $\overline{XEO}/\overline{HF}$ high. Both the RCLK and WCLK inputs must be at a high level during reset (see Figure 7).

The 'ACT7201A is fully cascadable in word-width and/or word-depth over the specified temperature range. Word-width expansion (see Figure 13) is accomplished by connecting together the corresponding input control signals of the cascaded devices. The status flags ($\overline{EMPTY}$, $\overline{FULL}$, and $\overline{XEO}/\overline{HF}$) can be monitored from any one of the cascaded devices. The $\overline{XEI}$ input of each device in the word-width expansion should be grounded. Word-depth expansion (see Figure 14) is also accomplished by connecting together the corresponding input control signals of the cascaded devices. The $\overline{FL}/\overline{RT}$ input, on the first device in the daisy chain, is grounded to designate it as the first device loaded and unloaded. The $\overline{FL}/\overline{RT}$ inputs of all the other devices in the daisy chain must be tied high. The Expansion Enable Out ($\overline{XEO}/\overline{HF}$) output of each device in the word-depth expansion is connected to the $\overline{XEI}$ input of the next device in the daisy chain. After reset, the RCLK and WCLK inputs are enabled on the first device in the daisy chain. The RCLK and WCLK inputs of all the other devices are disabled. When the last word location of the first device is written into, the $\overline{XEO}$ output pulses low, enabling the WCLK of the next device in the daisy chain. Similarly, when the last word location of the first device is read from, the $\overline{XEO}$ output pulses low, enabling the RCLK of the next device in the daisy chain (see Figure 9). Control of read and write continues this progression through the daisy chain in a circular queue fashion. In word-depth expansion, a composite $\overline{EMPTY}$ and $\overline{FULL}$ must be generated by ORing the corresponding flags together. In addition, word-width and word-depth expansion can be applied together to create large FIFO arrays (see Figure 15).

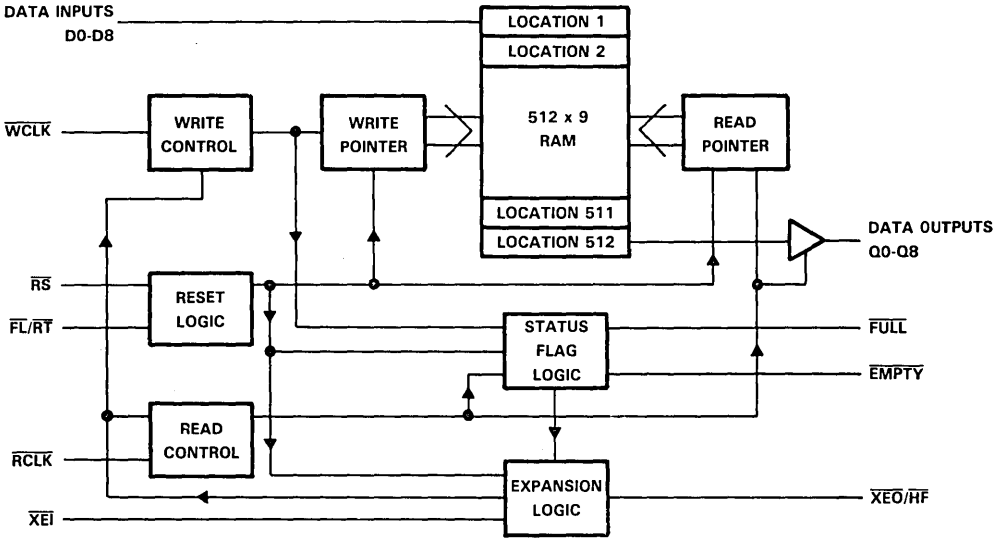
The SN74ACT7201A is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



RESET AND RETRANSMIT FUNCTION TABLE
512 WORD BY N × 9-BIT OPERATION

INPUTS			INTERNAL TO DEVICE		OUTPUTS			FUNCTION
RST	FL/RT	XEI	READ POINTER	WRITE POINTER	EMPTY	FULL	XEO/HF	
L	X	L	Location Zero	Location Zero	L	H	H	Reset Device
H	L	L	Location Zero	Unchanged	X	X	X	Retransmit
H	H	L	Increment if EMPTY high	Increment if FULL high	X	X	X	Read/Write

RESET AND FIRST LOAD FUNCTION TABLE
M × 512 WORD BY N × 9-BIT OPERATION

INPUTS			INTERNAL TO DEVICE		OUTPUTS			FUNCTION
RST	FL/RT	XEI	READ POINTER	WRITE POINTER	EMPTY	FULL	XEO/HF	
L	L	‡	Location Zero	Location Zero	L	H	H	Reset First Device
L	H	‡	Location Zero	Location Zero	L	H	H	Reset All Other Devices
H	X	‡	X	X	X	X	NA	Read/Write

‡ XEI is connected to XEO/HF of the previous device in the daisy chain.

PIN NAME	PIN NO.	I/O	DESCRIPTION
D0	6	I	Data Inputs
D1	5	I	
D2	4	I	
D3	3	I	
D4	27	I	
D5	26	I	
D6	25	I	
D7	24	I	
D8	2	I	
$\overline{EMPTY}$	21	O	Empty flag output. The empty flag ($\overline{EMPTY}$) output is low when the FIFO memory is empty, and high when the memory is not empty. When the memory is empty, additional read operations are inhibited.
$\overline{FULL}$	8	O	Full flag output. The full flag ($\overline{FULL}$) output is low when the FIFO memory is full, and high when the memory is not full. When the memory is full, additional write operations are inhibited.
$\overline{FL}/\overline{RT}$	23	I	First load/retransmit input. This input performs two separate functions. When cascading two or more devices for word-depth expansion, the $\overline{FL}/\overline{RT}$ input is grounded on the first device in the daisy chain to indicate that it is the first device loaded and unloaded. It is connected high on the other devices. In single-device operation or in word-width expansion, the $\overline{FL}/\overline{RT}$ input initiates the retransmit function. In this mode, a low-level pulse on the $\overline{FL}/\overline{RT}$ input resets the read pointer to the first memory location to allow for retransmission from the beginning of data entered. The write pointer is not affected by the $\overline{FL}/\overline{RT}$ input. The RCLK and WCLK must be at a high level during the low level $\overline{FL}/\overline{RT}$ retransmit pulse. The retransmit feature should be used only when less than 512 writes are performed between resets, otherwise, an attempt to retransmit may cause loss of some data that has not yet been read.
GND	14		Ground
Q0	9	O	Data outputs. These outputs are in the high-impedance state when the RCLK input is high or if the memory is empty.
Q1	10		
Q2	11		
Q3	12		
Q4	16		
Q5	17		
Q6	18		
Q7	19		
Q8	13		
RCLK	15	I	Read clock input. If the FIFO is not empty (i.e., $\overline{EMPTY}$ is high), data is read from the FIFO on RCLK input high-to-low transition.
$\overline{RST}$	22	I	Master Reset Input. A low level pulse on the Master Reset input ($\overline{RST}$) resets the FIFO. This sets the $\overline{EMPTY}$ output low and the $\overline{FULL}$ output high, indicating that the FIFO is empty. RCLK and WCLK must both be at a high level during reset.
V_{CC}	28		Supply voltage
WCLK	1	I	Write clock input. If the FIFO is not full (i.e., $\overline{FULL}$ is high), data is written into the FIFO on a low-to-high transition at the WCLK input.
$\overline{XEI}$	7	I	Expansion Enable Input. When cascading two or more devices for word-depth expansion, the $\overline{XEI}$ input is connected to the $\overline{XEO}$ output of the previous device in the daisy chain. The $\overline{XEI}$ input is grounded when no word-depth expansion is desired.
$\overline{XEO}/\overline{HF}$	20	O	Expansion Enable Out/Half Full Flag Output. This output performs two separate functions. When cascading two or more devices for word-depth expansion, the $\overline{XEO}/\overline{HF}$ output is connected to the $\overline{XEI}$ input of the next device in the daisy chain. When the FIFO is used as a 512-word memory, the $\overline{XEO}/\overline{HF}$ output functions as a Half Full Flag. In this mode, $\overline{XEO}/\overline{HF}$ is low whenever the FIFO contains 257 or more words, and is high whenever the FIFO contains 256 words or less.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range, any input . . . . . −0.5 V to 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−8	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −8 mA	3.8			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.4	V
I_{OZH}	High-impedance-state output current	V_O = 2.7 V				10	µA
I_{OZL}	High-impedance-state output current	V_O = 0.4 V				10	µA
I_I	Input current	V_I = 0 V to 5.5 V				10	µA
I_{CC1}	Supply current	f = 28.5 MHz for 'ACT7201A-25, f = 22.2 MHz for 'ACT7201A-35, f = 15 MHz for 'ACT7201A-50				80	mA
I_{CC2}	Standby current	RCLK, WCLK, $\overline{RST}$, and $\overline{FL}/\overline{RT}$ at V_{IH}				8	mA
I_{CC3}	Power down current	V_I = V_{CC} −0.2 V				500	µA
C_i	Input capacitance	V_I = 0,	f = 1 MHz		5		pF
C_o	Output capacitance	V_O = 0,	f = 1 MHz		7		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

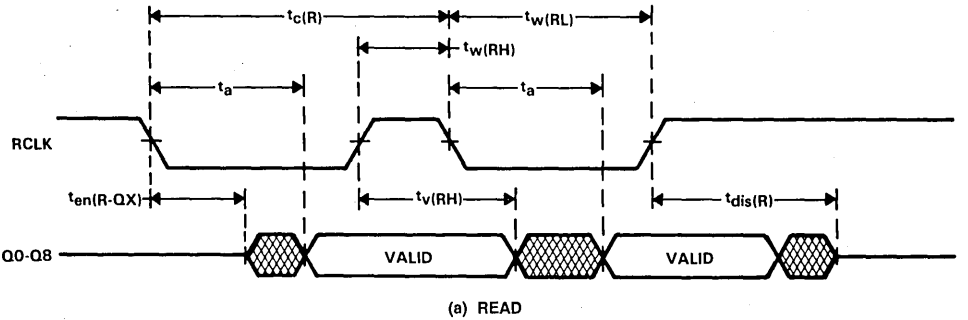
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		FIGURE	'ACT7201A-25		'ACT7201A-35		'ACT7201A-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, RCLK or WCLK			28.5		22.2		15	MHz
$t_{c(R)}$	Cycle time, read	1(a)	35		45		65		ns
$t_{c(W)}$	Cycle time, write	1(b)	35		45		65		ns
$t_{c(RS)}$	Cycle time, reset	7	35		45		65		ns
$t_{c(RT)}$	Cycle time, retransmit	4	35		45		65		ns
$t_{w(RL)}$	Pulse duration, RCLK low	1(a)	25		35		50		ns
$t_{w(WL)}$	Pulse duration, WCLK low	1(b)	25		35		50		ns
$t_{w(RH)}$	Pulse duration, RCLK high	1(a)	10		10		15		ns
$t_{w(WH)}$	Pulse duration, WCLK high	1(b)	10		10		15		ns
$t_{w(RT)}$	Pulse duration, $\overline{FL/RT}$ low	4	25		35		50		ns
$t_{w(RS)}$	Pulse duration, $\overline{RST}$ low	7	25		35		50		ns
$t_{w(XIL)}$	Pulse duration, $\overline{XEI}$ low	10	25		35		50		ns
$t_{w(XIH)}$	Pulse duration, $\overline{XEI}$ high	10	10		10		10		ns
$t_{su(D)}$	Setup time, data before WCLK↑	1(b), 6	15		18		30		ns
$t_{su(RT)}$	Setup time, RCLK and WCLK high before $\overline{FL/RT}$↑	4	25		35		50		ns
$t_{su(RS)}$	Setup time, RCLK and WCLK high before $\overline{RST}$↑	7	25		35		50		ns
$t_{su(XI-R)}$	Setup time, $\overline{XEI}$ low before RCLK↓	10	15		15		15		ns
$t_{su(XI-W)}$	Setup time, $\overline{XEI}$ low before WCLK↓	10	15		15		15		ns
$t_{h(D)}$	Hold time, data after WCLK↑	1(b), 6	0		0		5		ns
$t_{h(E-R)}$	Hold time, RCLK low after $\overline{EMPTY}$↑	5	25		35		50		ns
$t_{h(F-W)}$	Hold time, WCLK low after $\overline{FULL}$↑	6	25		35		50		ns
$t_{h(RT)}$	Hold time, RCLK and WCLK high after $\overline{FL/RT}$↑	4	10		10		15		ns
$t_{h(RS)}$	Hold time, RCLK and WCLK high after $\overline{RST}$↑	7	10		10		15		ns

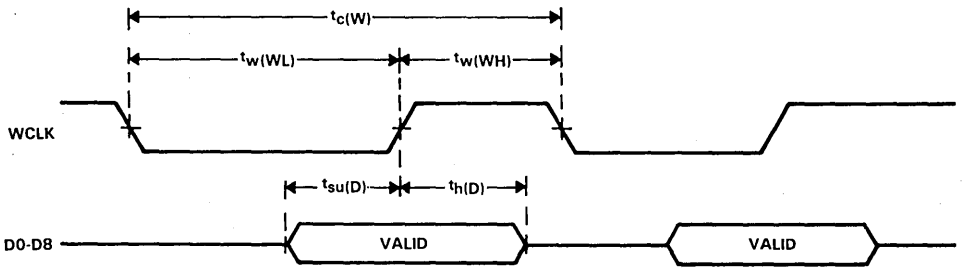
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		FIGURE	'ACT7201A-25		'ACT7201A-35		'ACT7201A-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Clock frequency, RCLK or WCLK		28.5		22.2		15		MHz
t_a	Access time, RCLK ↓ or EMPTY ↑ to data out valid	1(a), 3, 5		25		35		50	ns
$t_{v(RH)}$	Valid time, data out valid after RCLK ↑	1(a)	5		5		5		ns
$t_{en(R-QX)}$	Enable time, RCLK ↓ to Q outputs at low impedance	1(a)	5		5		10		ns
$t_{en(W-QX)}$	Enable time, WCLK ↑ to Q outputs at low impedance	5	5		10		15		ns
$t_{dis(R)}$	Disable time, RCLK ↑ to Q outputs at high impedance	1a		15		20		30	ns
$t_{w(FH)}$	Pulse duration, $\overline{FULL}$ high in automatic write mode	6		25		30		45	ns
$t_{w(EH)}$	Pulse duration, $\overline{EMPTY}$ high in automatic mode	5		25		30		45	ns
$t_{p(W-F)}$	Propagation delay time, WCLK ↓ to $\overline{FULL}$ low	2		25		30		45	ns
$t_{p(R-F)}$	Propagation delay time, RCLK ↑ to $\overline{FULL}$ high	2, 6		25		30		45	ns
$t_{p(RS-F)}$	Propagation delay time, $\overline{RST}$ ↓ to $\overline{FULL}$ high	7		20		45		65	ns
$t_{p(RS-HF)}$	Propagation delay time, $\overline{RST}$ ↓ to $\overline{XEO}$/$\overline{HF}$ high	7		20		45		65	ns
$t_{p(W-E)}$	Propagation delay time, WCLK ↑ to $\overline{EMPTY}$ high	3, 5		25		30		45	ns
$t_{p(R-E)}$	Propagation delay time, RCLK ↓ to $\overline{EMPTY}$ low	3		25		30		45	ns
$t_{p(RS-E)}$	Propagation delay time, $\overline{RST}$ ↓ to $\overline{EMPTY}$ low	7		20		45		65	ns
$t_{p(W-HF)}$	Propagation delay time, WCLK ↓ to $\overline{XEO}$/$\overline{HF}$ low	8		35		45		65	ns
$t_{p(R-HF)}$	Propagation delay time, RCLK ↑ to $\overline{XEO}$/$\overline{HF}$ high	8		35		45		65	ns
$t_{p(R-XOL)}$	Propagation delay time, RCLK ↓ to $\overline{XEO}$/$\overline{HF}$ low	9		25		35		50	ns
$t_{p(W-XOL)}$	Propagation delay time, WCLK ↓ to $\overline{XEO}$/$\overline{HF}$ low	9		25		35		50	ns
$t_{p(R-XOH)}$	Propagation delay time, RCLK ↑ to $\overline{XEO}$/$\overline{HF}$ high	9		25		35		50	ns
$t_{p(W-XOH)}$	Propagation delay time, WCLK ↑ to $\overline{XEO}$/$\overline{HF}$ high	9		25		35		50	ns

PARAMETER MEASUREMENT INFORMATION



(a) READ



(b) WRITE

FIGURE 1. ASYNCHRONOUS WAVEFORMS

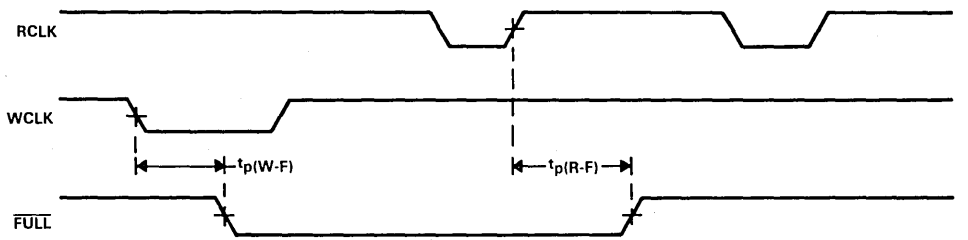


FIGURE 2. FULL FLAG WAVEFORMS

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PARAMETER MEASUREMENT INFORMATION

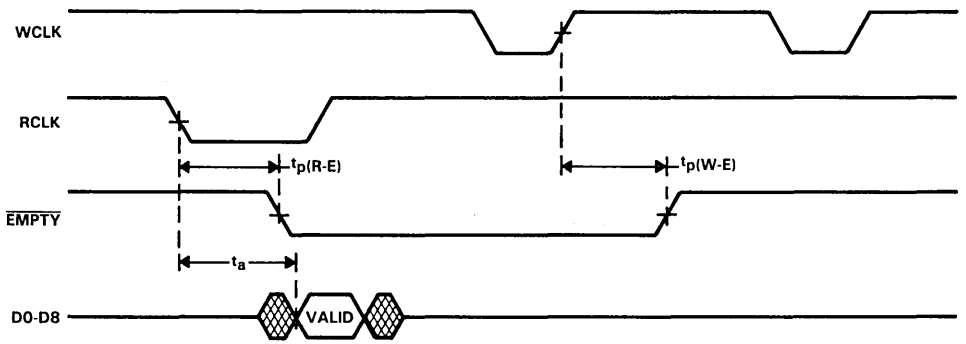


FIGURE 3. EMPTY FLAG WAVEFORMS

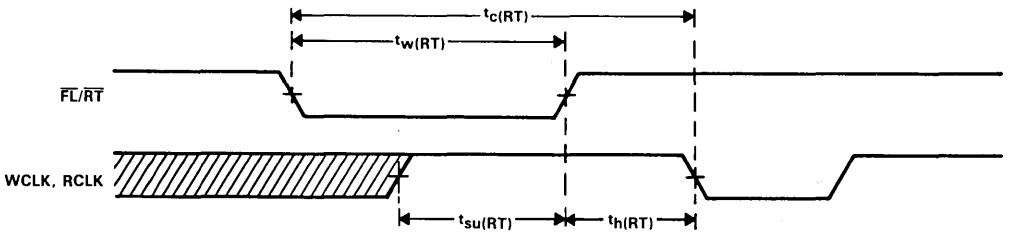


FIGURE 4. RETRANSMIT WAVEFORMS (see Note 2)

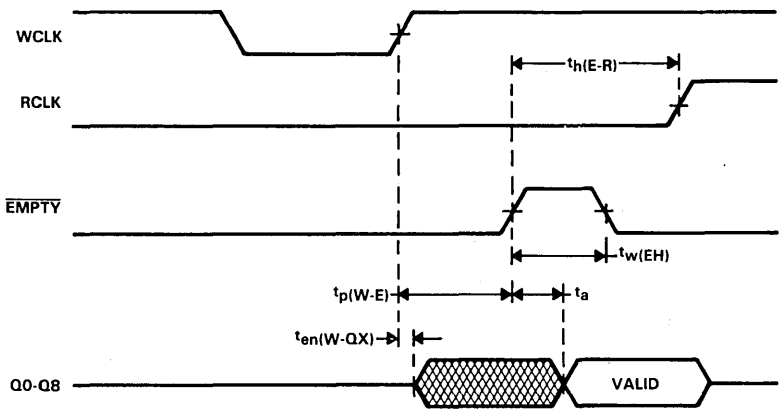


FIGURE 5. AUTOMATIC READ WAVEFORMS

NOTE 2: The $\overline{\text{EMPTY}}$, $\overline{\text{FULL}}$, and $\overline{\text{XEO}}/\overline{\text{HF}}$ status flags will be valid after completion of the retransmit cycle.

PARAMETER MEASUREMENT INFORMATION

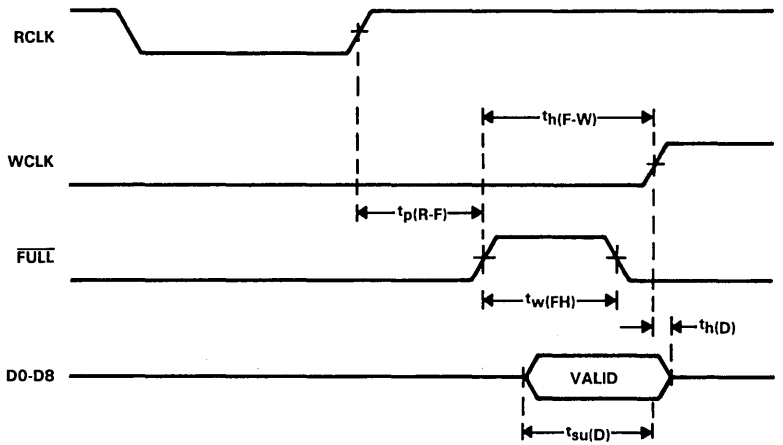


FIGURE 6. AUTOMATIC WRITE WAVEFORMS

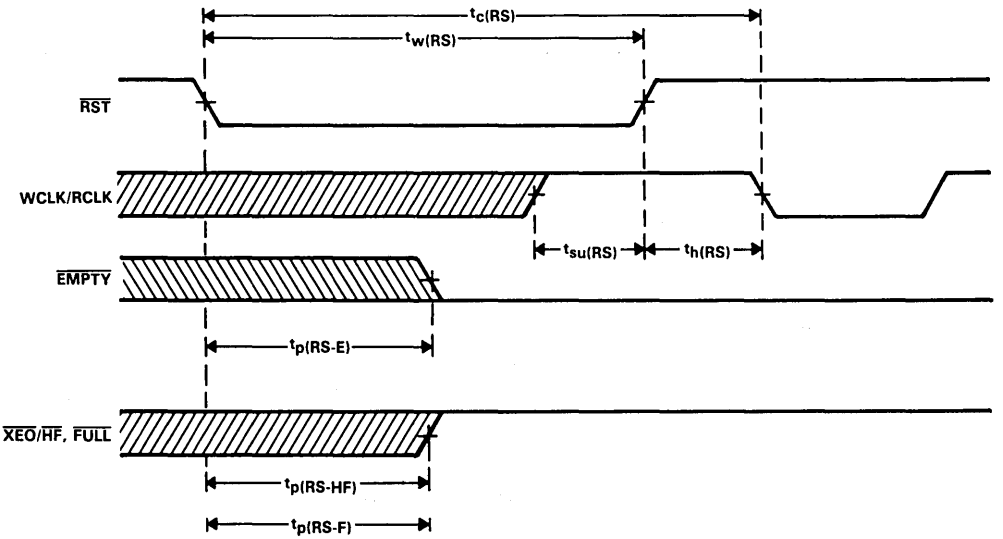


FIGURE 7. MASTER RESET WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

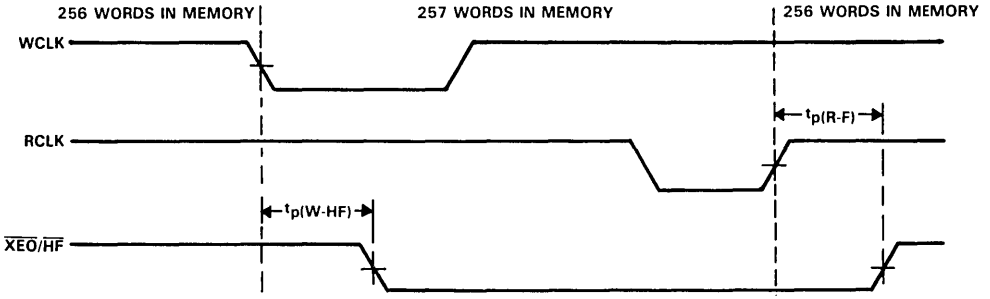


FIGURE 8. HALF-FULL FLAG WAVEFORMS

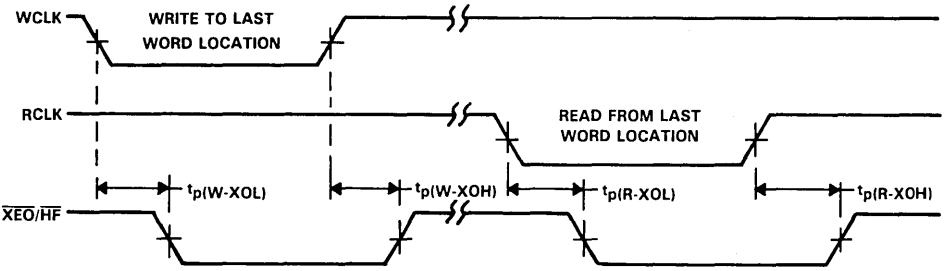


FIGURE 9. EXPANSION-OUT WAVEFORMS

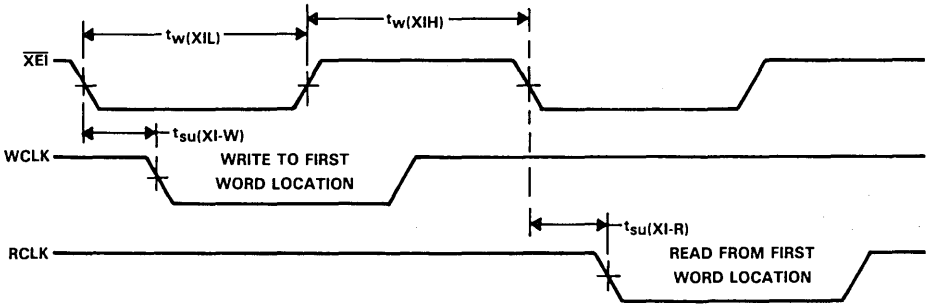
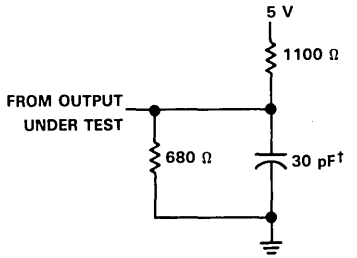


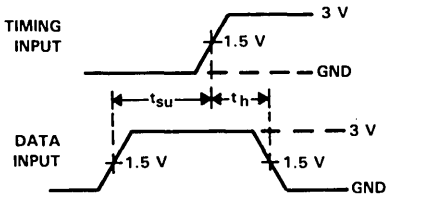
FIGURE 10. EXPANSION-IN WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

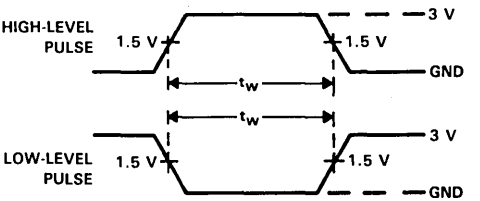


†Includes probe and jig capacitance.

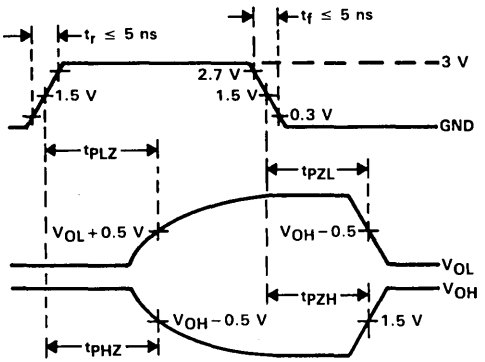
FIGURE 11. CIRCUIT



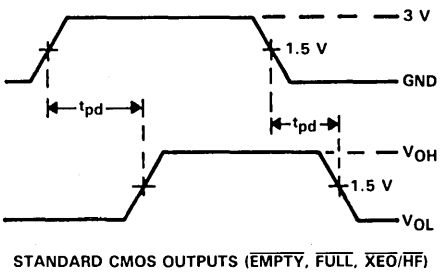
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



3-STATE OUTPUTS (Q0-Q8)



STANDARD CMOS OUTPUTS ($\overline{\text{EMPTY}}$, $\overline{\text{FULL}}$, $\overline{\text{XEO}}$/$\overline{\text{HF}}$)

FIGURE 12. TIMING REFERENCE LEVELS

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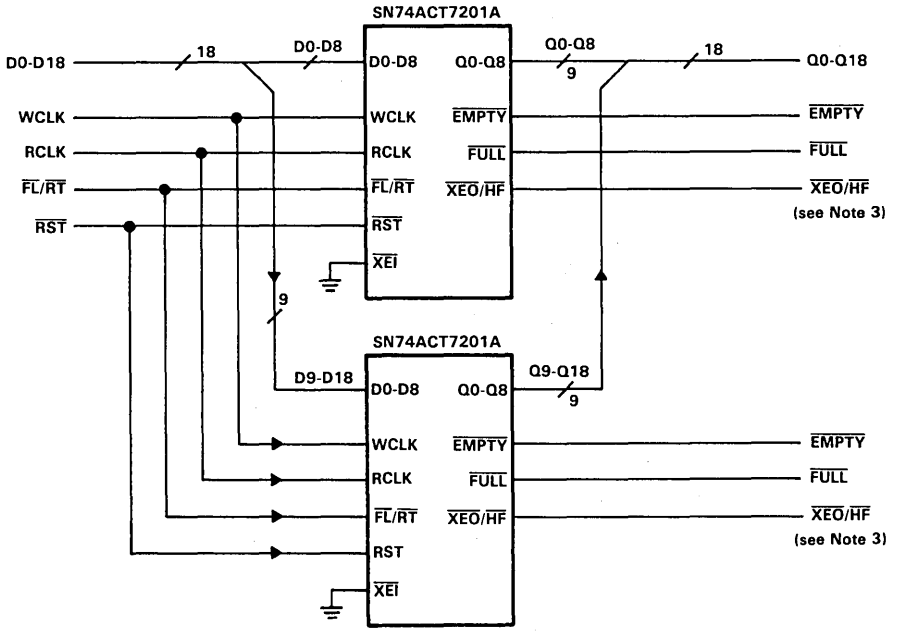
TYPICAL APPLICATION DATA



NOTE 3: In word-width expansion, the status flags $\overline{\text{EMPTY}}$, $\overline{\text{FULL}}$, and $\overline{\text{XEO}}/\overline{\text{HF}}$ can be monitored from either one of the cascaded devices. The status flag outputs must not be tied together.

FIGURE 13. WORD-WIDTH EXPANSION: 512-WORD BY 18-BIT

TYPICAL APPLICATION DATA

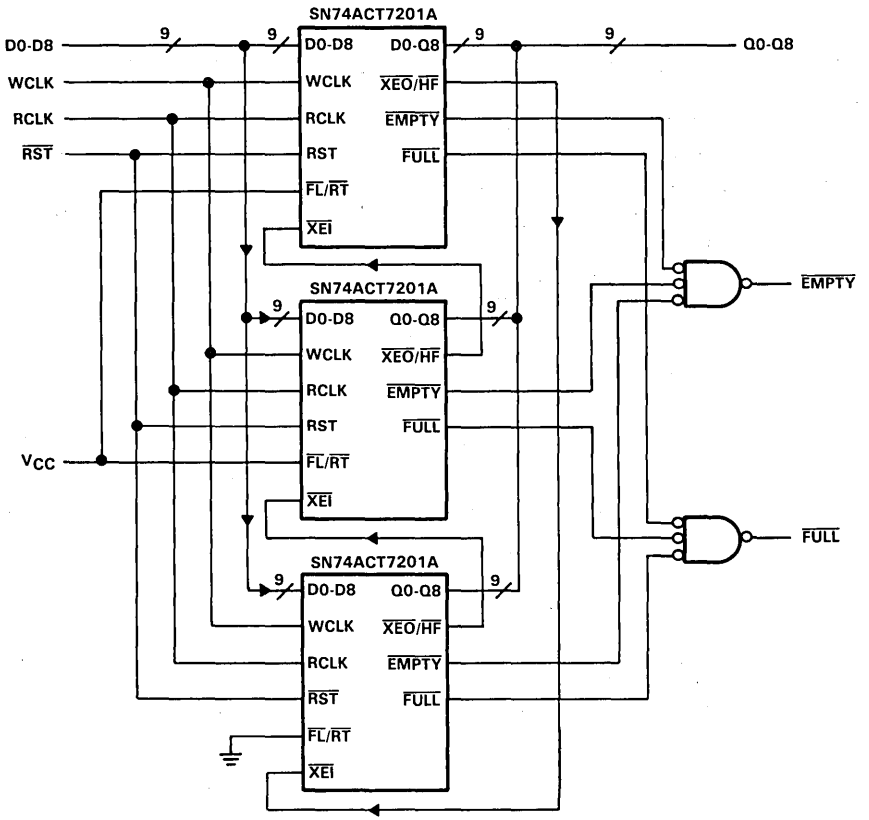


FIGURE 14. WORD-DEPTH EXPANSION: 1536-WORD BY 9-BIT

TYPICAL APPLICATION DATA

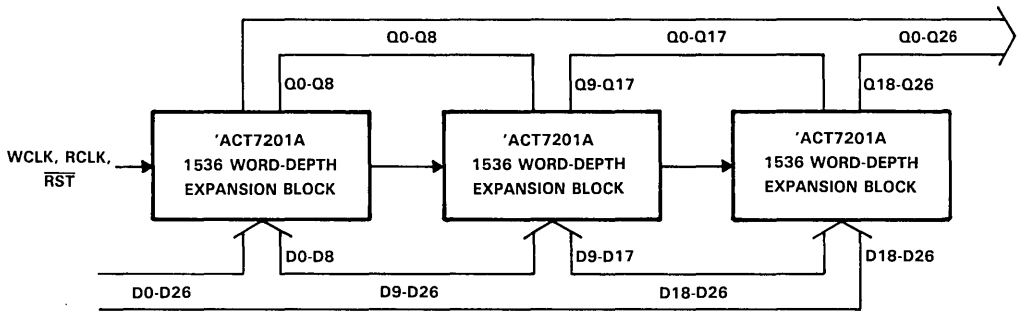
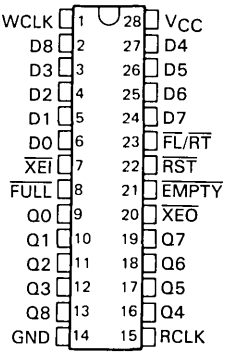


FIGURE 15. 1536-WORD BY 27-BIT EXPANSION

D3056, NOVEMBER 1987

- Asynchronous Operation
- Organized as 1024 Words of 9 Bits
- Low Power Consumption
  - Active . . . 440 mW
  - Power Down . . . 3 mW
  - Standby . . . 44 mW
- Fully Expandable in Word Width and/or Word Depth
- Designed to be Compatible with IDT7202 But with Lower Power Consumption
- EPIC™ (Enhanced Performance Implanted CMOS) 1-μm Process
- Reliable Advanced CMOS Technology
- Fully TTL-Compatible

SN74ACT7202 . . . N PACKAGE
(TOP VIEW)



For chip carrier information contact the factory.

description

This 9216-bit memory uses Advanced CMOS Technology and features high speed and fast fall-through times. The 'ACT7202 is organized as 1024 words by 9 bits each.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ACT7202 is designed to process data at rates from 0 to 22 MHz in a bit-parallel format, word by word.

Data is written into the memory on a low-to-high transition at the Write Clock (WCLK) input, and is read out of the memory on a high-to-low transition at the Read Clock (RCLK) input, (see Figure 1). The data outputs are noninverting with respect to the data inputs and are in a high-impedance state when RCLK is high. The memory is full when the number of words clocked in exceeds by 1024 the number of words clocked out. When the memory is full, write signals have no effect on the data residing in memory. When the memory is empty, read signals have no effect, and the data outputs remain in a high-impedance state.

Status of the FIFO memory is monitored by the Full Flag ($\overline{\text{FULL}}$), Empty Flag ($\overline{\text{EMPTY}}$). The $\overline{\text{FULL}}$ output is low when the memory is full, and high when the memory is not full (see Figure 2). The $\overline{\text{EMPTY}}$ output is low when the memory is empty, and high when it is not empty (see Figure 3).

The First Load/Retransmit ($\overline{\text{FL}}/\overline{\text{RT}}$) input performs two separate functions. When cascading two or more devices for word-depth expansion, $\overline{\text{FL}}/\overline{\text{RT}}$ functions as a first-load input and is grounded on the first device in the daisy chain to indicate that it is the first device loaded and unloaded. When the 'ACT7202 is used as a 1024-word FIFO memory, the $\overline{\text{FL}}/\overline{\text{RT}}$ input performs the retransmit function. This 1024-word memory mode is defined by grounding the Expansion Enable Input ($\overline{\text{XEI}}$) of the device. In this mode, a low-level pulse on the $\overline{\text{FL}}/\overline{\text{RT}}$ input resets the read pointer to the first memory location to allow for retransmission from the beginning of data entered. The write pointer is not affected by the $\overline{\text{FL}}/\overline{\text{RT}}$ input. RCLK and WCLK must be at the high level during the low-level $\overline{\text{FL}}/\overline{\text{RT}}$ retransmit pulse (see Figure 4).

The retransmit feature should be used only when less than 1024 writes are performed between resets, otherwise, an attempt to retransmit may cause loss of some data that has not yet been read.

When the FIFO is empty, a data word can be read automaticallly at the Q outputs by holding RCLK low when loading in the data word with a low-level pulse on the WCLK (see Figure 5).

When the FIFO is full, a data word can be written automatically into memory by holding WCLK low while reading out another data word with a low-level pulse on RCLK (see Figure 6).

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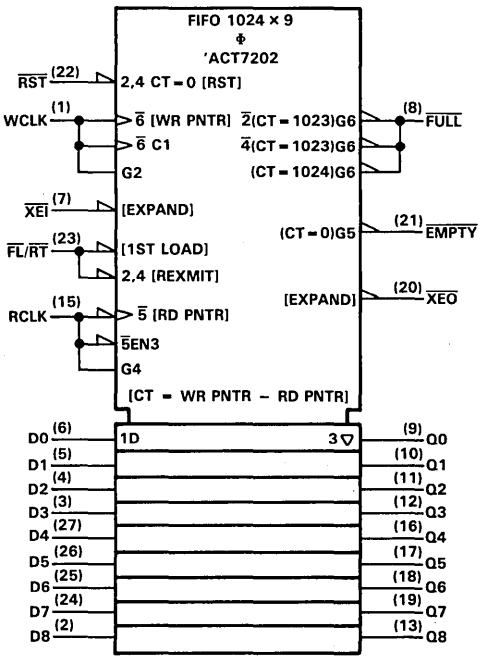
description (continued)

The FIFO must be reset after power up with a low level pulse on the Reset ($\overline{RST}$) input. This resets the read and write internal stack control pointers to the first memory location, and also sets $\overline{EMPTY}$ low and $\overline{FULL}$ high. Both the RCLK and WCLK inputs must be at a high level during reset (see Figure 7).

The 'ACT7202 is fully cascadable in word-width and/or word-depth over the specified temperature range. Word-width expansion (see Figure 10) is accomplished by connecting together the corresponding input control signals of the cascaded devices. The status flags $\overline{EMPTY}$ and $\overline{FULL}$ can be monitored from any one of the cascaded devices. The $\overline{XEI}$ input of each device in the word-width expansion should be grounded. Word-depth expansion (see Figure 11) is also accomplished by connecting together the corresponding input control signals of the cascaded devices. The $\overline{FL}/\overline{RT}$ input, on the first device in the daisy chain, is grounded to designate it as the first device loaded. The $\overline{FL}/\overline{RT}$ inputs of all the other devices in the daisy chain must be tied high. The Expansion Enable Out ($\overline{XEO}$) output of each device in the word-depth expansion is connected to the $\overline{XEI}$ input of the next device in the daisy chain. A composite $\overline{EMPTY}$ and $\overline{FULL}$ must be generated by ORing the corresponding flags together. In addition, word-width and word-depth expansion can be applied together to create large FIFO arrays (see Figure 12).

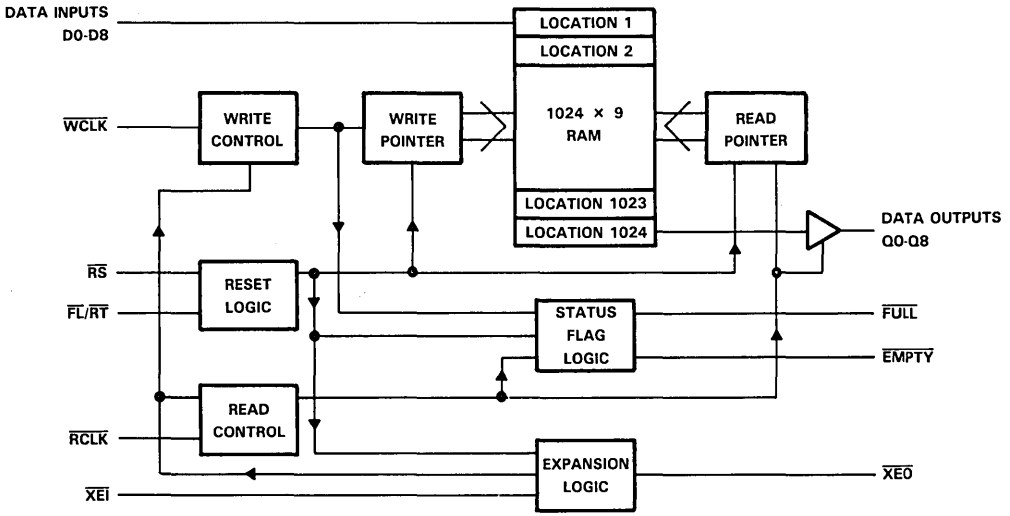
The SN74ACT7202 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

functional block diagram



RESET FUNCTION TABLE

1024 WORD BY N × 9-BIT OPERATION

INPUTS			INTERNAL TO DEVICE		OUTPUTS		FUNCTION
$\overline{RST}$	$\overline{FL}/\overline{RT}$	$\overline{XEI}$	READ POINTER	WRITE POINTER	$\overline{EMPTY}$	$\overline{FULL}$	
L	X	L	Location Zero	Location Zero	L	H	Reset Device
H	L	L	Location Zero	Unchanged	X	X	Retransmit
H	H	L	Increment if $\overline{EF}$ high	Increment if $\overline{FF}$ high	X	X	Read/Write

FIRST LOAD/RETRANSMIT FUNCTION TABLE

M × 1024 WORD BY N × 9-BIT OPERATION

INPUTS			INTERNAL TO DEVICE		OUTPUTS		FUNCTION
$\overline{RST}$	$\overline{FL}/\overline{RT}$	$\overline{XEI}$	READ POINTER	WRITE POINTER	$\overline{EMPTY}$	$\overline{FULL}$	
L	L	†	Location Zero	Location Zero	L	H	Reset First Device
L	H	†	Location Zero	Unchanged	X	X	Reset All Other Devices
H	X	†	X	X	X	X	Read/Write

†$\overline{XEI}$ is connected to $\overline{XEO}$ of the previous device in the daisy chain.

PIN NAME	PIN NO.	I/O	DESCRIPTION
D0	6	I	Data Inputs
D1	5	I	
D2	4	I	
D3	3	I	
D4	27	I	
D5	26	I	
D6	25	I	
D7	24	I	
D8	2	I	
$\overline{\text{EMPTY}}$	21	O	Empty flag output. The empty flag ($\overline{\text{EMPTY}}$) output is low when the FIFO memory is empty, and high when the memory is not empty. When the memory is empty, additional read operations are inhibited.
$\overline{\text{FULL}}$	8	O	Full flag output. The full flag ($\overline{\text{FULL}}$) output is low when the FIFO memory is full, and high when the memory is not full. When the memory is full, additional write operations are inhibited.
$\overline{\text{FL}}/\overline{\text{RT}}$	23	I	First load/retransmit input. This input performs two separate functions. When cascading two or more devices for word-depth expansion, the $\overline{\text{FL}}/\overline{\text{RT}}$ input is grounded on the first device in the daisy chain to indicate that it is the first device loaded and unloaded. It is connected high on the other devices. In single-device operation or in word-width expansion, the $\overline{\text{FL}}/\overline{\text{RT}}$ input initiates the retransmit function. In this mode, a low-level pulse on the $\overline{\text{FL}}/\overline{\text{RT}}$ input resets the read pointer to the first memory location to allow for retransmission from the beginning of data entered. The write pointer is not affected by the $\overline{\text{FL}}/\overline{\text{RT}}$ input. The RCLK and WCLK must be at a high level during the low level $\overline{\text{FL}}/\overline{\text{RT}}$ retransmit pulse. The retransmit feature should be used only when less than 1024 writes are performed between resets, otherwise, an attempt to retransmit may cause loss of some data that has not yet been read.
GND	14		Ground
Q0	9	O	Data outputs. These outputs are in the high-impedance state when the RCLK input is high or if the memory is empty.
Q1	10		
Q2	11		
Q3	12		
Q4	16		
Q5	17		
Q6	18		
Q7	19		
Q8	13		
RCLK	15	I	Read clock input. If the FIFO is not empty (i.e., $\overline{\text{EMPTY}}$ is high), data is read from the FIFO on RCLK input high-to-low transition.
$\overline{\text{RST}}$	22	I	Master Reset Input. A low level pulse on the Master Reset input ($\overline{\text{RST}}$) resets the FIFO. This sets the $\overline{\text{EMPTY}}$ output low and the $\overline{\text{FULL}}$ output high, indicating that the FIFO is empty. RCLK and WCLK must both be at a high level during reset.
V_{CC}	28		Supply voltage
WCLK	1	I	Write clock input. If the FIFO is not full (i.e., $\overline{\text{FULL}}$ is high), data is written into the FIFO on a low-to-high transition at the WCLK input.
$\overline{\text{XEI}}$	7	I	Expansion Enable Input. When cascading two or more devices for word-depth expansion, the $\overline{\text{XEI}}$ input is connected to the $\overline{\text{XEO}}$ output of the previous device in the daisy chain. The $\overline{\text{XEI}}$ input is grounded when no word-depth expansion is desired.
$\overline{\text{XEO}}$	20	O	Expansion Enable Output. When cascading two or more devices for word-depth expansion, the $\overline{\text{XEO}}$ output is connected to the $\overline{\text{XEI}}$ input of the next device in the daisy chain.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range, any input . . . . . −0.5 V to 7 V
Voltage applied to a disabled 3-state ouput . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−8	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V, I_{OH} = −8 mA	3.8			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4	V
I_{OZH}	High-impedance-state output current	V_O = 2.7 V			10	μA
I_{OZL}	High-impedance-state output current	V_O = 0.4 V			10	μA
I_I	Input current	V_I = 0 V to 5.5 V			10	μA
I_{CC1}	Supply current	f = 22 MHz			80	mA
I_{CC2}	Standby current	RCLK, WCLK, $\overline{RST}$, and $\overline{FL/RT}$ at V_{IH}			8	mA
I_{CC3}	Power down current	V_I = V_{CC} −0.2 V			500	μA
C_i	Input capacitance	V_I = 0, f = 1 MHz		5		pF
C_o	Output capacitance	V_O = 0, f = 1 MHz		7		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		FIGURE	SN74ACT7202-50		SN74ACT7202-35		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(R)}$	Cycle time, read	1a	65		45		ns
$t_{c(W)}$	Cycle time, write	1b	65		45		ns
$t_{c(RS)}$	Cycle time, reset	7	65		25		ns
$t_{c(RT)}$	Cycle time, retransmit	4	65		30		ns
$t_{w(RL)}$	Pulse duration, RCLK low	1a	50		30		ns
$t_{w(WL)}$	Pulse duration, WCLK low	1b	50		35		ns
$t_{w(RH)}$	Pulse duration, RCLK high	1a	15		15		ns
$t_{w(WH)}$	Pulse duration, WCLK high	1b	15		10		ns
$t_{w(RT)}$	Pulse duration, $\overline{FL}/\overline{RT}$ low	4	50		20		ns
$t_{w(RS)}$	Pulse duration, $\overline{RST}$ low	7	50		15		ns
$t_{su(D)}$	Setup time, data before WCLK↑	1b, 6	30		10		ns
$t_{su(RT)}$	Setup time, $\overline{FL}/\overline{RT}$ high before RCLK↓ or WCLK↓	4	15		10		ns
$t_{su(R-RS)}$	Setup time, RCLK high before $\overline{RST}$↑	7	50		30		ns
$t_{su(W-RS)}$	Setup time, WCLK high before $\overline{RST}$↑	7	50		35		ns
$t_{h(D)}$	Hold time, data after WCLK↑	1b, 6	5		3		ns
$t_{h(E-R)}$	Hold time, RCLK low after $\overline{EMPTY}$↑	5	50		30		ns
$t_{h(F-W)}$	Hold time, WCLK low after $\overline{FULL}$↑	6	50		35		ns
$t_{h(RS-W)}$	Hold time, WCLK high after $\overline{RST}$↑	7	15		10		ns
$t_{h(RS-R)}$	Hold time, RCLK high after $\overline{RST}$↑	7	15		10		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		FIGURE	SN74ACT7202-50			SN74ACT7202-35			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_a	Access time, RCLK↓ or EMPTY↑ to data out valid	1a, 3, 5		18	50		18	35	ns
$t_{v(RH)}$	Valid time, data out valid after RCLK↑	1a	5			5			ns
$t_{en(R-QX)}$	Enable time, RCLK↓ to Q outputs at low impedance	1a	10			5			ns
$t_{en(W-QX)}$	Enable time, WCLK↑ to Q outputs at low impedance	5	15			10			ns
$t_{dis(R)}$	Disable time, RCLK↑ to Q outputs at high impedance	1a		10	30		10	20	ns
$t_{w(FH)}$	Pulse duration, $\overline{FULL}$ high in automatic write mode	6		15	45		15	25	ns
$t_{w(EH)}$ •	Pulse duration, $\overline{EMPTY}$ high in automatic read mode	5		18	45		18	30	ns
$t_{p(W-F)}$	Propagation delay time, WCLK↓ to $\overline{FULL}$ low	2		15	45		15	25	ns
$t_{p(R-F)}$	Propagation delay time, RCLK↑ to $\overline{FULL}$ high	2, 6		23	45		23	35	ns
$t_{p(R-E)}$	Propagation delay time, RCLK↓ to $\overline{EMPTY}$ low	3		18	45		18	30	ns
$t_{p(W-E)}$	Propagation delay time, WCLK↑ to $\overline{EMPTY}$ high	3,5		21	45		21	30	ns
$t_{p(RS-E)}$	Propagation delay time, RST↓ to $\overline{EMPTY}$ low	6		9	65		9	20	ns
$t_{p(RS-F)}$	Propagation delay time, RST↓ to $\overline{FULL}$ high	6		7	65		7	20	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

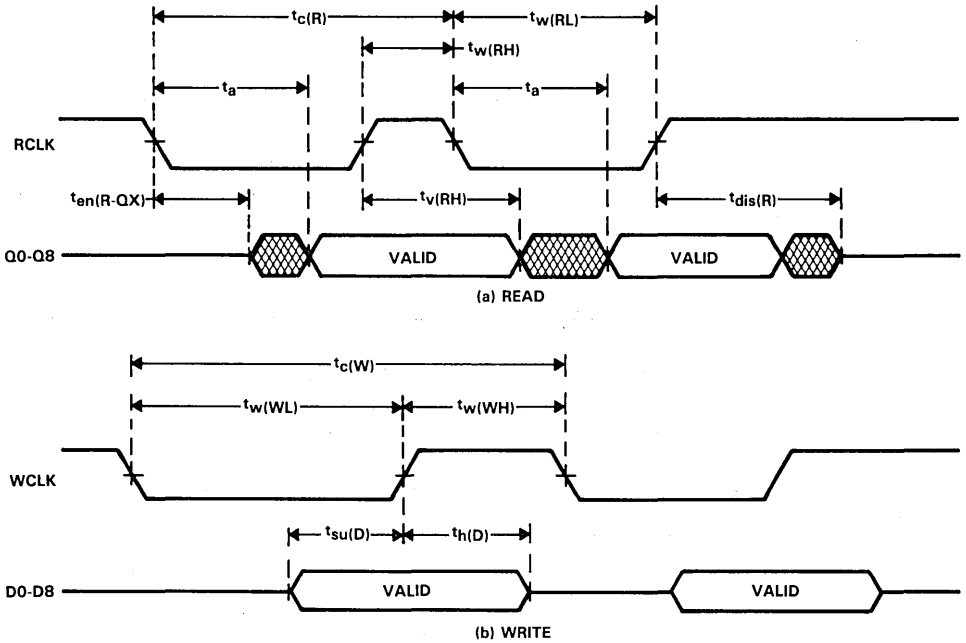


FIGURE 1. ASYNCHRONOUS WAVEFORMS

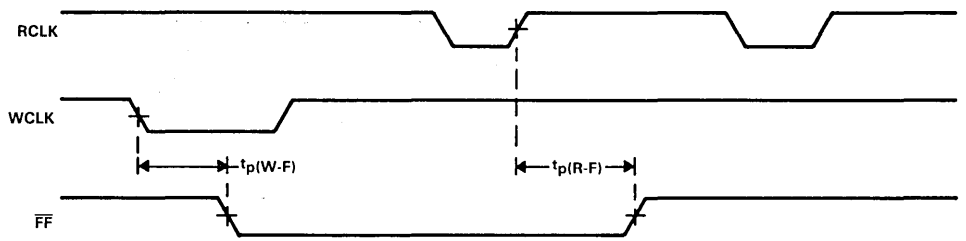


FIGURE 2. FULL FLAG WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

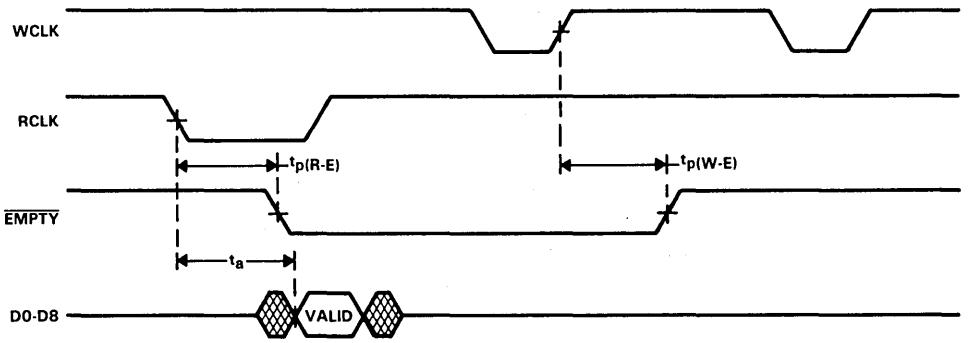


FIGURE 3. EMPTY FLAG WAVEFORMS

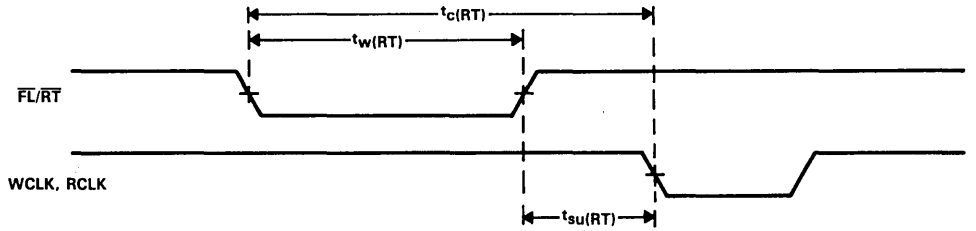


FIGURE 4. RETRANSMIT WAVEFORMS

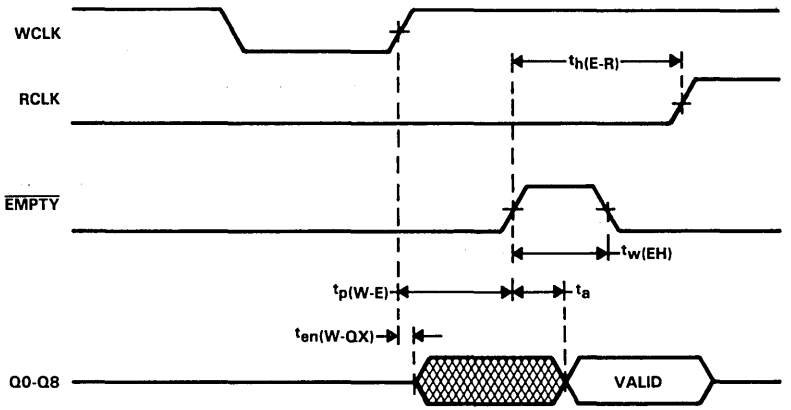


FIGURE 5. AUTOMATIC READ WAVEFORMS

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PARAMETER MEASUREMENT INFORMATION

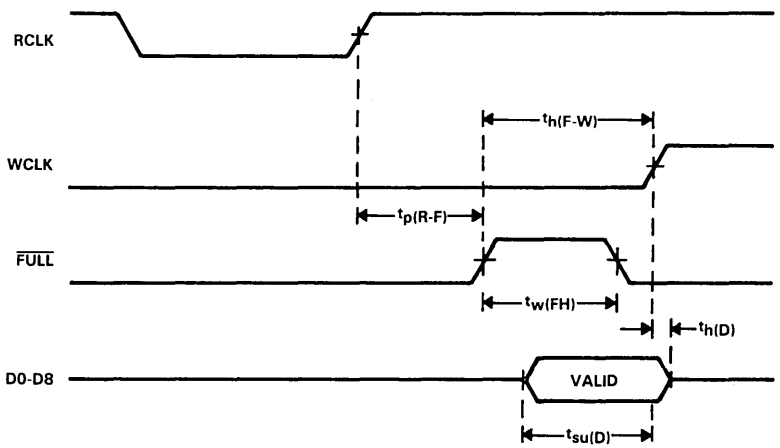
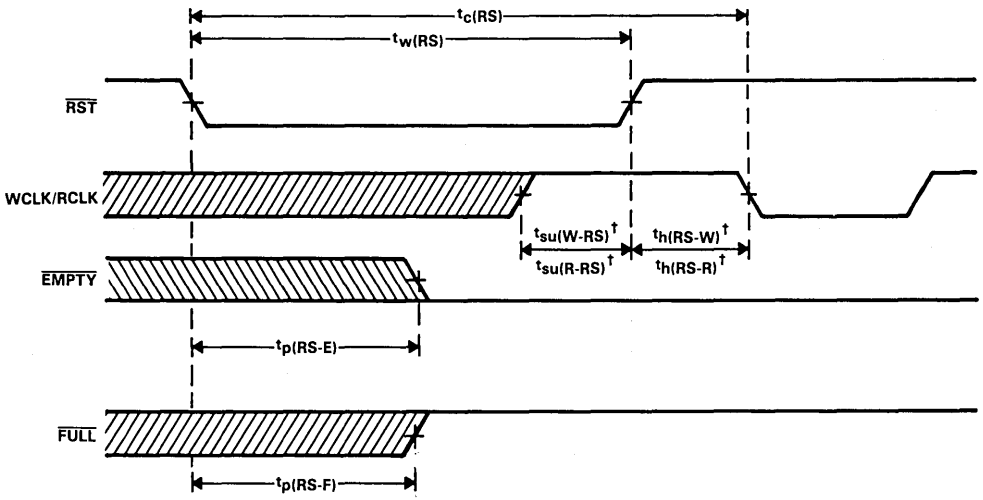


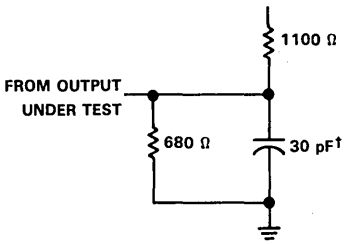
FIGURE 6. AUTOMATIC WRITE WAVEFORMS



†The WCLK input must be high for a time equal to $t_{su(W-RS)}$ before, and $t_{h(RS-W)}$ after, the rising edge of $\overline{RST}$. The RCLK input must be high for a time equal to $t_{su(R-RS)}$ before, and $t_{h(RS-R)}$ after, the rising edge of $\overline{RST}$.

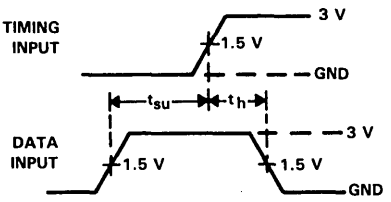
FIGURE 7. MASTER RESET WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

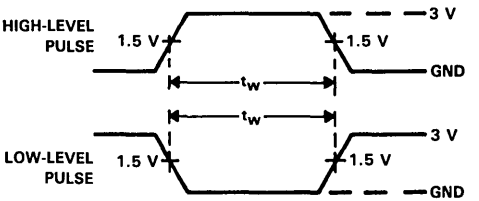


†Includes probe and jig capacitance.

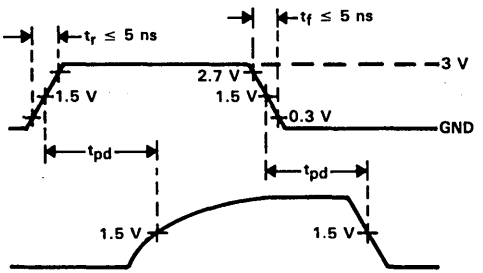
FIGURE 8. LOAD CIRCUIT



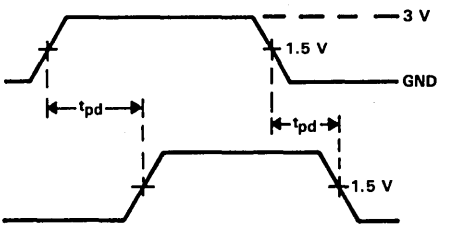
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



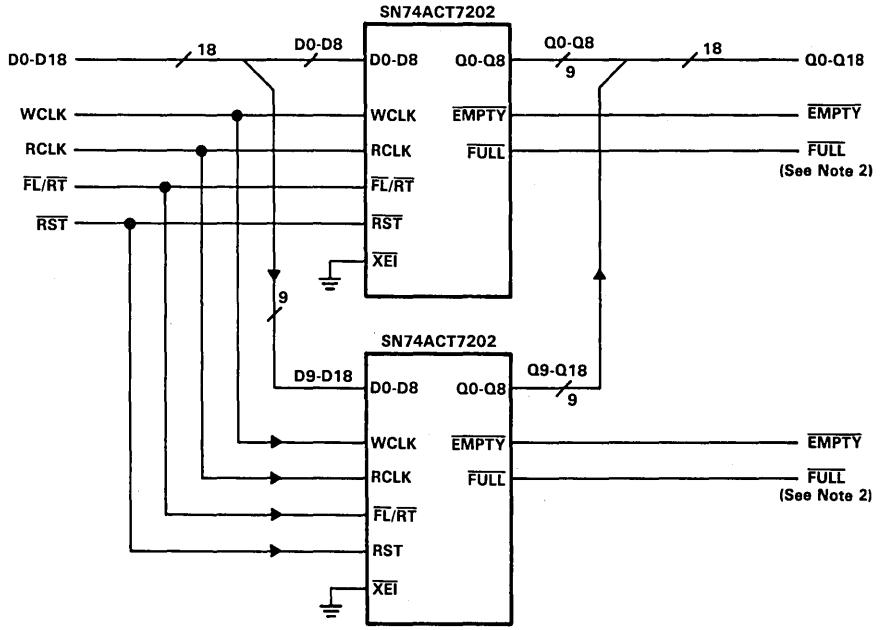
3-STATE OUTPUTS (Q0-Q8)



STANDARD CMOS OUTPUTS ($\overline{\text{EMPTY}}$, $\overline{\text{FULL}}$, $\overline{\text{XO}}$)

FIGURE 9. TIMING REFERENCE LEVELS

TYPICAL APPLICATION DATA



NOTE 2: In word-width expansion, the status flags $\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ can be monitored from either one of the cascaded devices. The status flag outputs must not be tied together.

FIGURE 10. WORD-WIDTH EXPANSION: 1024-WORD BY 18-BIT

TYPICAL APPLICATION DATA

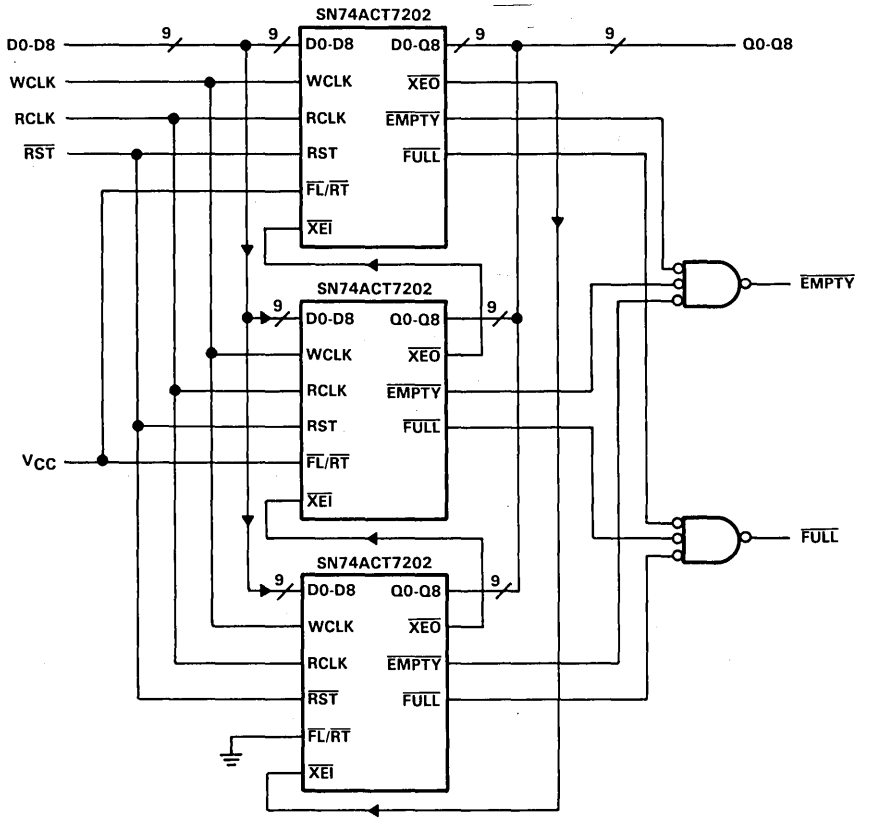


FIGURE 11. WORD-DEPTH EXPANSION: 3072-WORD BY 9-BIT

TYPICAL APPLICATION DATA

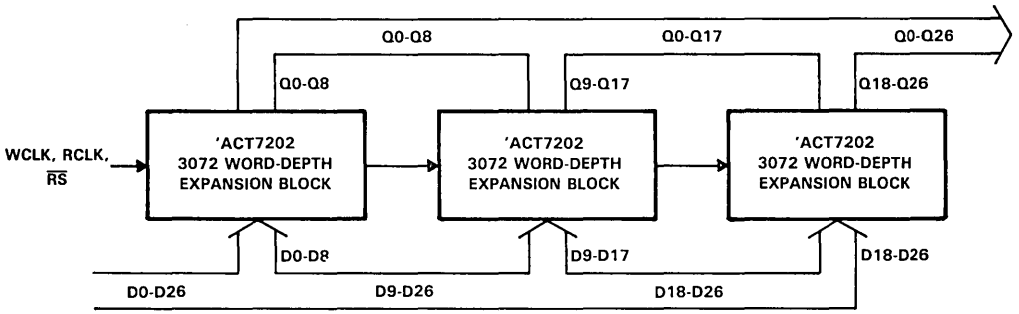
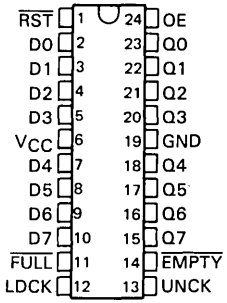


FIGURE 12. 3072-WORD BY 27-BIT EXPANSION

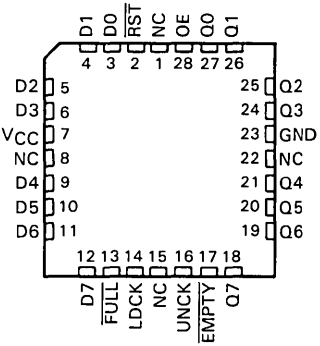
D3091, FEBRUARY 1988—REVISED MARCH 1988

- Independent Asynchronous Inputs and Outputs
- 64 Words by 8 Bits
- Data Rates from 0 to 40 MHz
- Fall-Through Time . . . 20 ns Typical
- 3-State Outputs

DW OR NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

This 512-bit memory uses Advanced Low-Power Schottky IMPACT-X™ technology and features high speed and fast fall-through times. It is organized as 64 words by 8 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The function is used as a buffer to couple two buses operating at different clock rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition of the load clock input (LDCK) and is read out on a low-to-high transition of the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 64 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

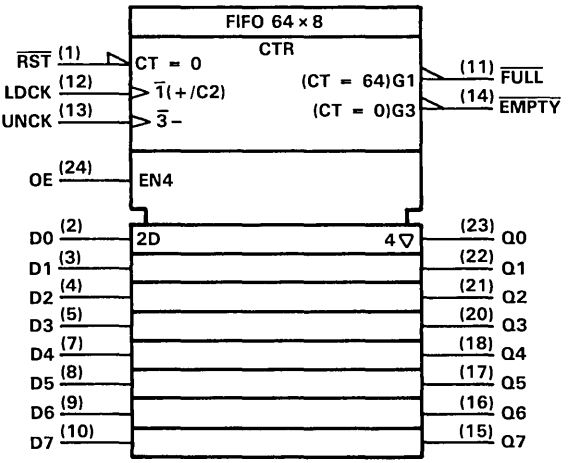
Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ output flags. The $\overline{\text{FULL}}$ output will be low when the memory is full, and high when the memory is not full. The $\overline{\text{EMPTY}}$ output will be low when the memory is empty, and high when it is not empty.

A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and $\overline{\text{FULL}}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{\text{RST}}$ pulse or from an empty condition, causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. The first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at a high-impedance state when the output-enable input (OE) is low. The OE input does not effect either the $\overline{\text{FULL}}$ or $\overline{\text{EMPTY}}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

The SN74ALS2232 is characterized for operation from 0°C to 70°C.

IMPACT—X is a trademark of Texas Instruments Incorporated.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

Pin numbers shown are for DW or NT packages.

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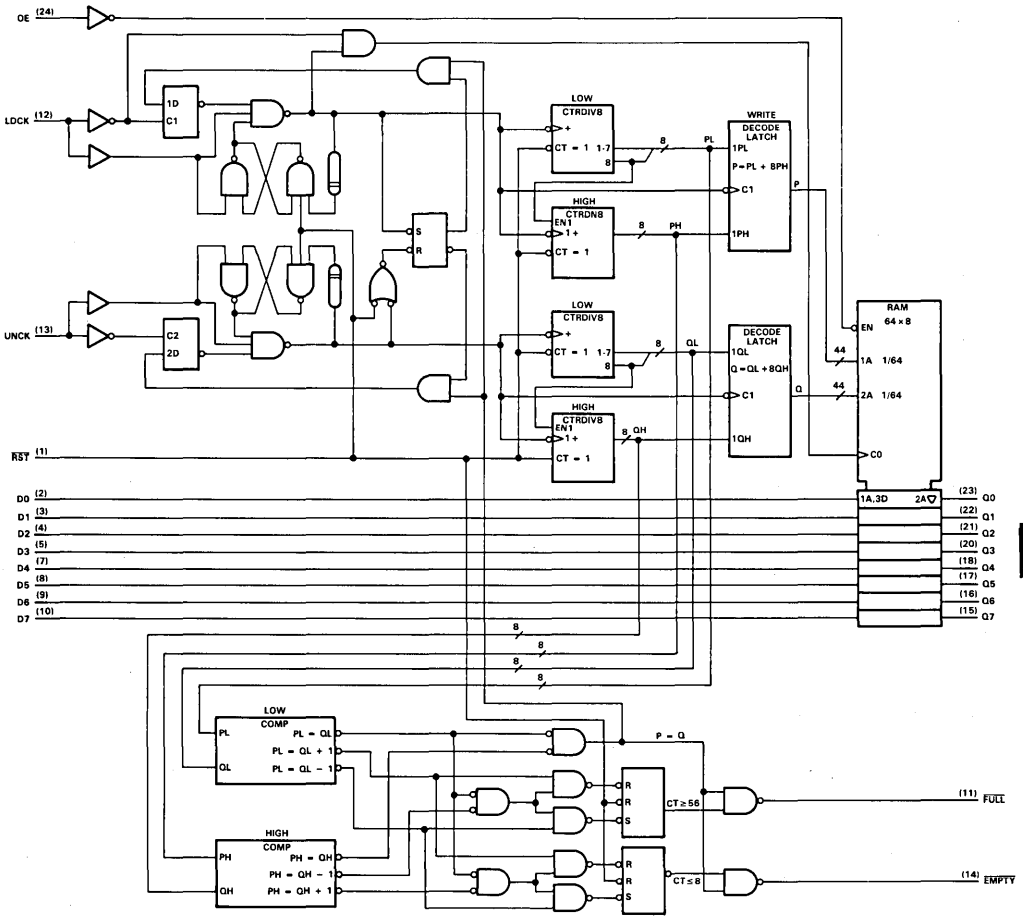
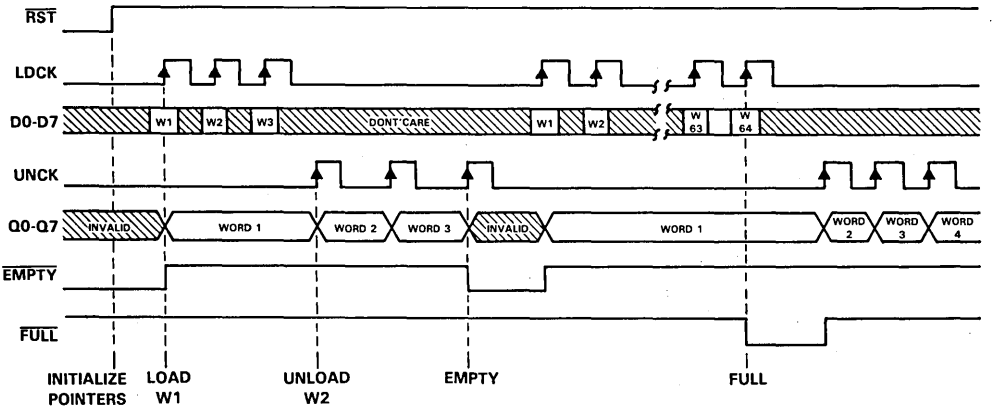
logic diagram (positive logic)



Pin numbers shown are for DW or NT packages.

timing diagram



absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		$\overline{FULL}$, $\overline{EMPTY}$			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		$\overline{FULL}$, $\overline{EMPTY}$			8	
f_{clock}	Clock frequency	LDCK, UNCK	0		40	MHz
t_w	Pulse duration	$\overline{RST}$ low	25			ns
		LDCK low	13			
		LDCK high	12			
		UNCK low	13			
		UNCK high	12			
t_{su1}	Setup time, data before LDCK↑		5			ns
t_{su2}	Setup time, $\overline{RST}$ high (inactive) before LDCK↑		5			ns
t_h	Hold time, data after LDCK↑		5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			1.2	V
V_{OH}	$\overline{FULL}$, $\overline{EMPTY}$	V_{CC} = MIN TO MAX,	I_{OH} = 0.4 mA	V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	Q outputs	V_{CC} =4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	$\overline{FULL}$, $\overline{EMPTY}$		I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O‡	Q outputs	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
	$\overline{FULL}$, $\overline{EMPTY}$			−20		−112	
I_{CC}		V_{CC} = 5.5 V			175	270	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

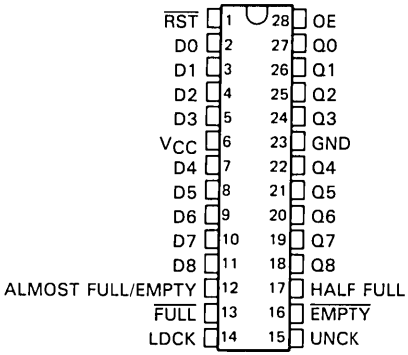
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	LDCK					40		MHz
	UNCK					40		
t_{pd}	LDCK↑	Any Q		18	26		30	ns
t_{pd}	UNCK↑	Any Q		18	24		27	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		12	16		18	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		12	17		20	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$		12	17		20	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		16	21		22	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		10	15		18	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		13	19		23	ns
t_{en}	OE↑	Q		11	15		17	ns
t_{dis}	OE↓	Q		11	17		19	ns

Note 1: Load circuit and voltage waveforms are shown in Section 1 of the *LSI Logic Data Book*, 1986.

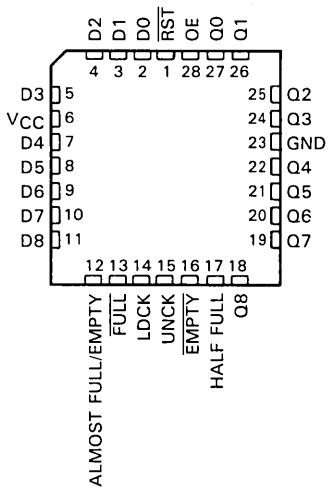
D3092, FEBRUARY 1988—REVISED APRIL 1988

- **Independent Asynchronous Inputs and Outputs**
- **64 Words by 9 Bits**
- **Data Rates from 0 to 40 MHz**
- **Fall-Through Time . . . 20 ns Typical**
- **3-State Outputs**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

This 576-bit memory uses Advanced Low-Power Schottky IMPACT—X™ technology and features high speed and fast fall-through times. It is organized as 64 words by 9 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The function is used as a buffer to couple two buses operating at different clock rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition of the load clock input (LDCK) and is read out on a low-to-high transition of the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 64 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, ALMOST FULL/EMPTY, and HALF FULL output flags. The $\overline{\text{FULL}}$ output will be low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output will be low when the memory is empty and high when it is not empty. The ALMOST FULL/EMPTY flag is high when the FIFO contains eight or less words or fifty-six or more words. The ALMOST FULL/EMPTY flag is low when the FIFO contains between nine and fifty-five words. The HALF FULL flag is high when the FIFO contains thirty-two or more words, and is low when the FIFO contains thirty-one words or less.

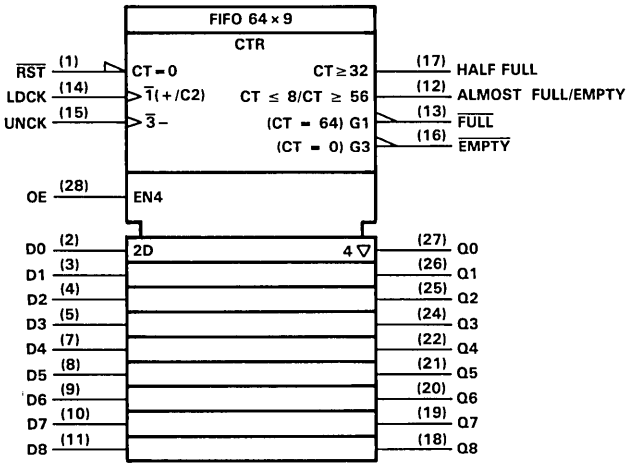
IMPACT—X is a trademark of Texas Instruments Incorporated.

description (continued)

A low level on the reset input ($\overline{RST}$) resets the internal stack control pointers and also sets EMPTY low and $\overline{FULL}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{RST}$ pulse or from an empty condition, causes $\overline{EMPTY}$ to go high and the data to appear on the Q outputs. The first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at a high-impedance state when the output-enable input (OE) is low. The OE input does not affect either the $\overline{FULL}$ or $\overline{EMPTY}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

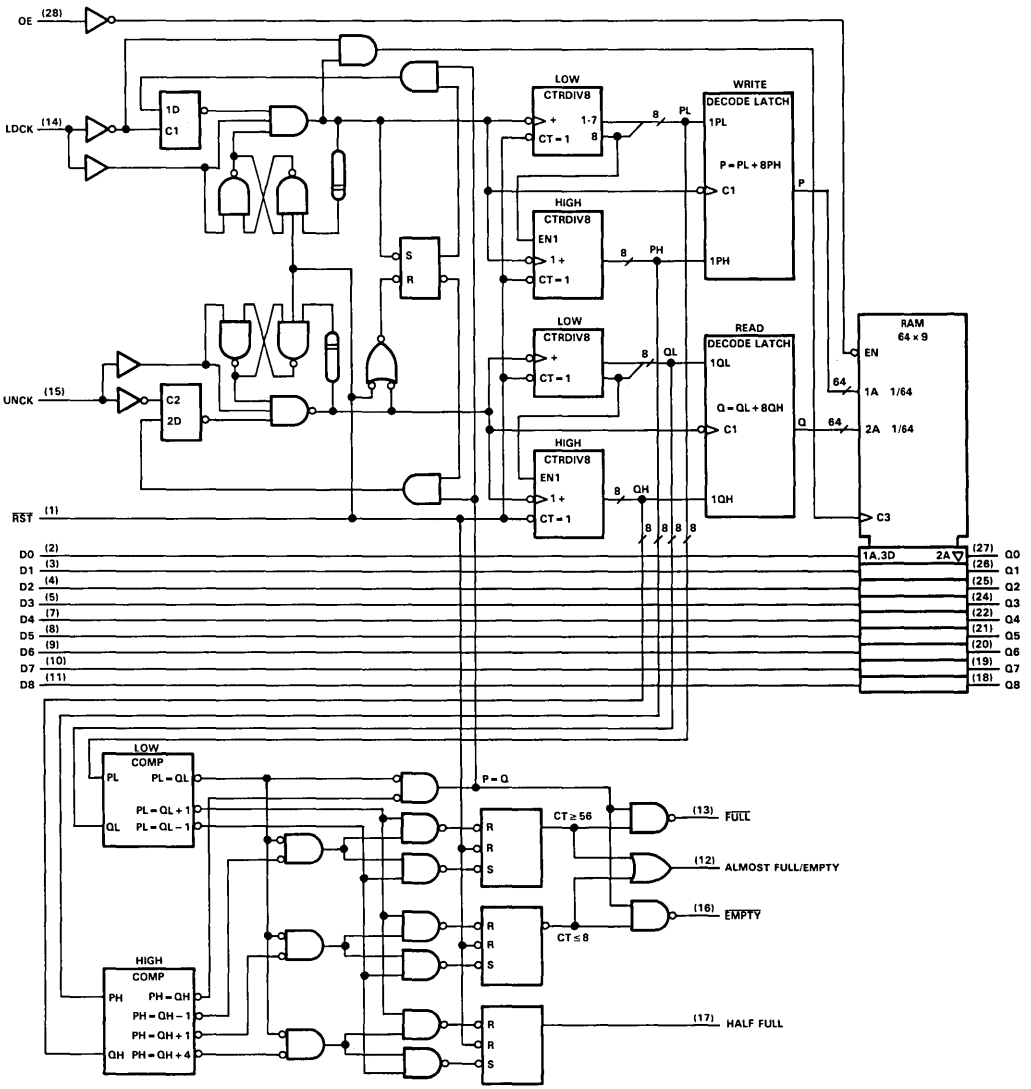
The SN74ALS2233 is characterized for operation from 0°C to 70°C.

logic symbol†

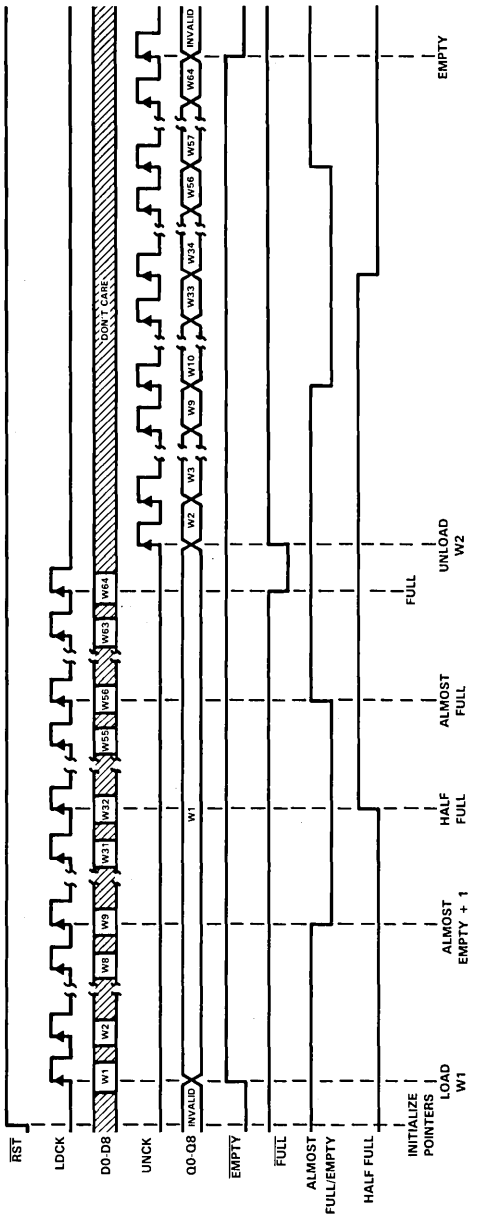


†This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

logic diagram (positive logic)



timing diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		Flag outputs			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		Flag outputs			8	
f_{clock}	Clock frequency	LDCK, UNCK	0		40	MHz
t_w	Pulse duration	$\overline{RST}$ low	25			ns
		LDCK low	13			
		LDCK high	12			
		UNCK low	13			
		UNCK high	12			
t_{su1}	Setup time, data before LDCK↑		5			ns
t_{su2}	Setup time, $\overline{RST}$ high (inactive) before LDCK↑		5			ns
t_h	Hold time, data after LDCK↑		5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDTIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			1.2	V
V_{OH}	Flag outputs	V_{CC} = MIN TO MAX,	I_{OH} = 0.4 mA	V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	Q Outputs	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	Flag outputs		I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O‡	Q outputs	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
	Flag outputs			−20		−112	
I_{CC}		V_{CC} = 5.5 V			175	290	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	LDCK					40		MHz
	UNCK					40		
t_{pd}	LDCK↑	Any Q		18	26		30	ns
t_{pd}	UNCK↑	Any Q		18	24		27	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		12	16		18	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		12	17		20	ns
t_{PHL}	RST↓	$\overline{EMPTY}$		12	17		20	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		16	21		22	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		10	15		18	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		13	19		23	ns
t_{PLH}	LDCK↑	ALMOST FULL/EMPTY		22	27		30	ns
t_{PHL}				19	25		28	
t_{PLH}	UNCK↑	ALMOST FULL/EMPTY		22	27		30	ns
t_{PHL}				17	23		26	
t_{PLH}	$\overline{RST}$↓	ALMOST FULL/EMPTY		12	16		18	
t_{PLH}	LDCK↑	HALF FULL		22	27		30	ns
t_{PHL}	$\overline{RST}$↓	HALF FULL		28	32		35	ns
t_{PHL}	UNCK↑	HALF FULL		16	22		25	ns
t_{en}	OE↑	Q		11	15		17	ns
t_{dis}	OE↓	Q		11	17		19	ns

Note 1: Load circuits and voltage waveforms are shown in Section 1 of the *LSI Logic Data Book*, 1986.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Built-In Diagnostic Capability
- Fast Write and Read Cycle Processing Times
- Byte-Write Capability . . . 'ALS632B and 'ALS633
- Dependable Texas Instruments Quality and Reliability

DEVICE	PACKAGE	BYTE-WRITE	OUTPUT
'ALS632B	52-pin	yes	3-State
'ALS633	52-pin	yes	Open-Collector
'ALS634B	48-pin	no	3-State
'ALS635	48-pin	no	Open-Collector

description

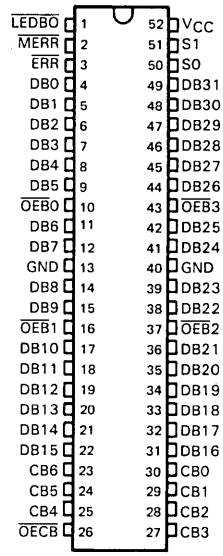
The 'ALS632B, 'ALS633, 'ALS634B and 'ALS635 devices are 32-bit parallel error detection and correction circuits (EDACs) in 52-pin ('ALS632B and 'ALS633) or 48-pin ('ALS634B and 'ALS635) 600-mil packages. The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

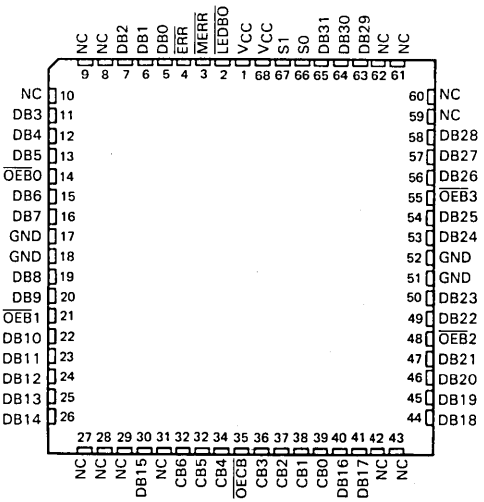
Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

'ALS632B, 'ALS633 . . . JD PACKAGE
(TOP VIEW)



'ALS632B, ALS633 . . . FN PACKAGE
(TOP VIEW)

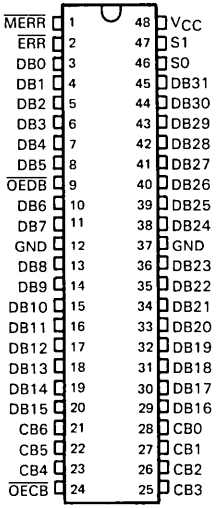


NC—No internal connection

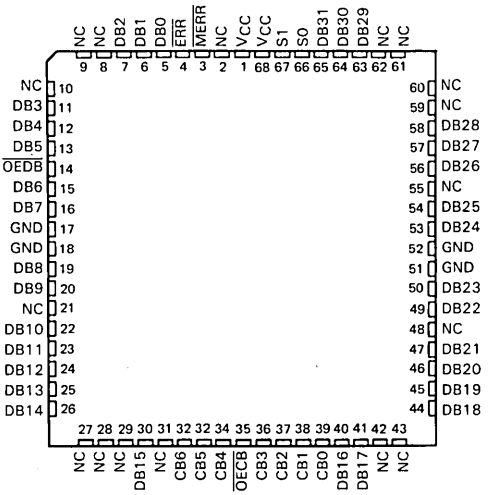
Read-modify-write (byte-control) operations can be performed with the 'ALS632B and 'ALS633 EDACs by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEB0}}$ thru $\overline{\text{OEB3}}$ byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

'ALS634B, 'ALS635 . . . JD PACKAGE
(TOP VIEW)



'ALS634B, 'ALS635 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{\text{OEBn}}$ OR $\overline{\text{OEDB}}$	DB OUTPUT LATCH ('ALS632B, 'ALS633) $\overline{\text{LEDBO}}$	CHECK I/O	CB CONTROL $\overline{\text{OECB}}$	ERROR FLAGS $\overline{\text{ERR}}$	ERROR FLAGS $\overline{\text{MERR}}$
Write	Generate check word	L	L	Input	H	X	Output check bits†	L	H	H

†See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction. CB0, CB1 and CB2 are odd parity bits and CB3, CB4, CB5, and CB6 are even parity bits. For example, for a data word of all zeros CB0-CB2 will be high and CB3-CB6 will be low.

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TABLE 2. PARITY ALGORITHM

CHECK WORD	32-BIT DATA WORD																													
BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X				X
CB1				X		X		X		X		X		X	X	X				X		X		X		X		X		X	X	X
CB2	X		X			X	X		X			X	X			X	X		X			X	X		X			X	X			X
CB3			X	X	X				X	X	X				X	X			X	X	X				X	X	X				X	X
CB4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{\text{MERR}}$ and a low on $\overline{\text{ERR}}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{\text{ERR}}$ and $\overline{\text{MERR}}$, which is the interrupt indication for the CPU.

TABLE 3. ERROR FUNCTION

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
32-BIT DATA WORD	7-BIT CHECK WORD	$\overline{\text{ERR}}$	$\overline{\text{MERR}}$	
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag ($\overline{\text{ERR}}$) will be set low while the dual error flag ($\overline{\text{MERR}}$) will remain high.

Any two-bit error will change the state of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.

TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEBn}$ OR $\overline{OEDB}$	DB OUTPUT LATCH ('ALS632B, 'ALS633) $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$ $\overline{MERR}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled†
Read	Output corrected data & syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†

†See Table 3 for error description.
‡See Table 5 for error location.

As the corrected word is made available on the data I/O port (DB0 thru DB31), the check word I/O port (CB0 thru CB6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

TABLE 5. SYNDROME DECODING

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	L	L	L	L	L	L	unc
L	L	L	L	L	L	H	2-bit
L	L	L	L	L	H	L	2-bit
L	L	L	L	L	H	H	unc
L	L	L	L	H	L	L	2-bit
L	L	L	L	H	L	H	unc
L	L	L	L	H	H	L	unc
L	L	L	L	H	H	H	2-bit
L	L	L	H	L	L	L	2-bit
L	L	L	H	L	L	H	unc
L	L	L	H	L	H	L	DB31
L	L	L	H	L	H	H	2-bit
L	L	L	H	H	L	L	unc
L	L	L	H	H	L	H	2-bit
L	L	L	H	H	H	L	2-bit
L	L	L	H	H	H	H	DB30
L	L	H	L	L	L	L	2-bit
L	L	H	L	L	L	H	unc
L	L	H	L	L	H	L	DB29
L	L	H	L	L	H	H	2-bit
L	L	H	L	H	L	L	DB28
L	L	H	L	H	L	H	2-bit
L	L	H	L	H	H	L	2-bit
L	L	H	L	H	H	H	DB27
L	L	H	H	L	L	L	DB26
L	L	H	H	L	L	H	2-bit
L	L	H	H	L	H	L	2-bit
L	L	H	H	L	H	H	DB25
L	L	H	H	H	L	L	2-bit
L	L	H	H	H	L	H	DB24
L	L	H	H	H	H	L	unc
L	L	H	H	H	H	H	2-bit

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	H	L	L	L	L	L	2-bit
L	H	L	L	L	L	H	unc
L	H	L	L	L	H	L	DB7
L	H	L	L	L	H	H	2-bit
L	H	L	L	H	L	L	DB6
L	H	L	L	H	L	H	2-bit
L	H	L	L	H	H	L	2-bit
L	H	L	L	H	H	H	DB5
L	H	L	H	L	L	L	DB4
L	H	L	H	L	L	H	2-bit
L	H	L	H	L	H	L	2-bit
L	H	L	H	L	H	H	DB3
L	H	L	H	H	L	L	2-bit
L	H	L	H	H	L	H	DB2
L	H	L	H	H	H	L	unc
L	H	L	H	H	H	H	2-bit
L	H	H	L	L	L	L	DB0
L	H	H	L	L	L	H	2-bit
L	H	H	L	L	H	L	2-bit
L	H	H	L	L	H	H	unc
L	H	H	L	H	L	L	2-bit
L	H	H	L	H	L	H	DB1
L	H	H	L	H	H	L	unc
L	H	H	L	H	H	H	2-bit
L	H	H	H	L	L	L	2-bit
L	H	H	H	L	L	H	unc
L	H	H	H	L	H	L	unc
L	H	H	H	L	H	H	2-bit
L	H	H	H	H	L	L	unc
L	H	H	H	H	L	H	2-bit
L	H	H	H	H	H	L	2-bit
L	H	H	H	H	H	H	CB6

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	L	L	L	L	L	L	2-bit
H	L	L	L	L	L	H	unc
H	L	L	L	L	H	L	unc
H	L	L	L	L	H	H	2-bit
H	L	L	L	H	L	L	unc
H	L	L	L	H	L	H	2-bit
H	L	L	L	H	H	L	2-bit
H	L	L	L	H	H	H	unc
H	L	L	H	L	L	L	unc
H	L	L	H	L	L	H	2-bit
H	L	L	H	L	H	L	2-bit
H	L	L	H	L	H	H	DB15
H	L	L	H	H	L	L	2-bit
H	L	L	H	H	L	H	unc
H	L	L	H	H	H	L	DB14
H	L	L	H	H	H	H	2-bit
H	L	H	L	L	L	L	unc
H	L	H	L	L	L	H	2-bit
H	L	H	L	L	H	L	2-bit
H	L	H	L	L	H	H	DB13
H	L	H	L	H	L	L	2-bit
H	L	H	L	H	L	H	DB12
H	L	H	L	H	H	L	DB11
H	L	H	L	H	H	H	2-bit
H	L	H	H	L	L	L	2-bit
H	L	H	H	L	L	H	DB10
H	L	H	H	L	H	L	DB9
H	L	H	H	L	H	H	2-bit
H	L	H	H	H	L	L	DB8
H	L	H	H	H	L	H	2-bit
H	L	H	H	H	H	L	2-bit
H	L	H	H	H	H	H	CB5

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	H	L	L	L	L	L	unc
H	H	L	L	L	L	H	2-bit
H	H	L	L	L	H	L	2-bit
H	H	L	L	L	H	H	DB23
H	H	L	L	H	L	L	2-bit
H	H	L	L	H	L	H	DB22
H	H	L	L	H	H	L	DB21
H	H	L	L	H	H	H	2-bit
H	H	L	H	L	L	L	2-bit
H	H	L	H	L	L	H	DB20
H	H	L	H	L	H	L	DB19
H	H	L	H	L	H	H	2-bit
H	H	L	H	H	L	L	DB18
H	H	L	H	H	L	H	2-bit
H	H	L	H	H	H	L	2-bit
H	H	L	H	H	H	H	CB4
H	H	H	L	L	L	L	2-bit
H	H	H	L	L	L	H	DB16
H	H	H	L	L	H	L	unc
H	H	H	L	L	H	H	2-bit
H	H	H	L	H	L	L	DB17
H	H	H	L	H	L	H	2-bit
H	H	H	L	H	H	L	2-bit
H	H	H	L	H	H	H	CB3
H	H	H	H	L	L	L	unc
H	H	H	H	L	L	H	2-bit
H	H	H	H	L	H	L	2-bit
H	H	H	H	L	H	H	CB2
H	H	H	H	H	L	L	2-bit
H	H	H	H	H	L	H	CB1
H	H	H	H	H	H	L	CB0
H	H	H	H	H	H	H	none

CB X= error in check bit X
DB Y= error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'ALS632B and 'ALS633 devices are capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{\text{LEDBO}}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{\text{OEB0}}$ through $\overline{\text{OEB3}}$ controls. $\overline{\text{OEB0}}$ controls DB0-DB7 (byte 0), $\overline{\text{OEB1}}$ controls DB8-DB15 (byte 1), $\overline{\text{OEB2}}$ controls DB16-DB23 (byte 2), and $\overline{\text{OEB3}}$ controls DB24-DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	BYTEn†	$\overline{OEBn}$†	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL	ERROR FLAG $\overline{ERR}$	ERROR FLAG $\overline{MERR}$
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled	
Read	Latch input data & check bits	H	H	Latched Input data	H	L	Latched input check word	H	Enabled	
Read	Latch corrected data word into output latch	H	H	Latched output data word	H	H	Hi-Z	H	Enabled	
							Output Syndrome bits	L		
Modify /write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTE0	H	H	Output check word	L	H	H
				Output unchanged BYTE0	L					

†$\overline{OEB0}$ controls DB0-DB7 (BYTE0), $\overline{OEB1}$ controls DB8-DB15 (BYTE1), $\overline{OEB3}$ controls DB16-DB23 (BYTE2), $\overline{OEB3}$ controls DB24-DB31 (BYTE3).

diagnostic operations

The 'ALS632B, 'ALS633, 'ALS634B and 'ALS635 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the $\overline{ERR}$ flag should be low. If a diagnostic data word with two errors in any bit location is applied, the $\overline{MERR}$ flag should be low. After the checkword is latched into the input latch, it can be verified by taking $\overline{OECB}$ low. This outputs the latched checkword. With the 'ALS632B and 'ALS633, the diagnostic data word can be latched into the output data latch and verified. It should be noted that the 'ALS634B and 'ALS635 do not have this pass-through capability because they do not contain an output data latch. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 ('ALS632B and 'ALS633) and Table 8 ('ALS634B and 'ALS635) list the diagnostic functions.

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TABLE 7. 'ALS632B, 'ALS633 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB BYTE CONTROL $\overline{OEBn}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains transparent	L	H	Input diagnostic data word†	H	L	Latched input check bits	H	Enabled	
Latch diagnostic data word into output latch	L	H	Input diagnostic data word†	H	H	Output latched check bits	L	Enabled	
						Hi-Z	H		
Latch diagnostic data word into input latch	H	H	Latched input diagnostic data word	H	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output diagnostic data word & syndrome bits	H	H	Output diagnostic data word	L	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output corrected diagnostic data word & output syndrome bits	H	H	Output corrected diagnostic data word	L	L	Output syndrome bits	L	Enabled	
						Hi-Z	H		

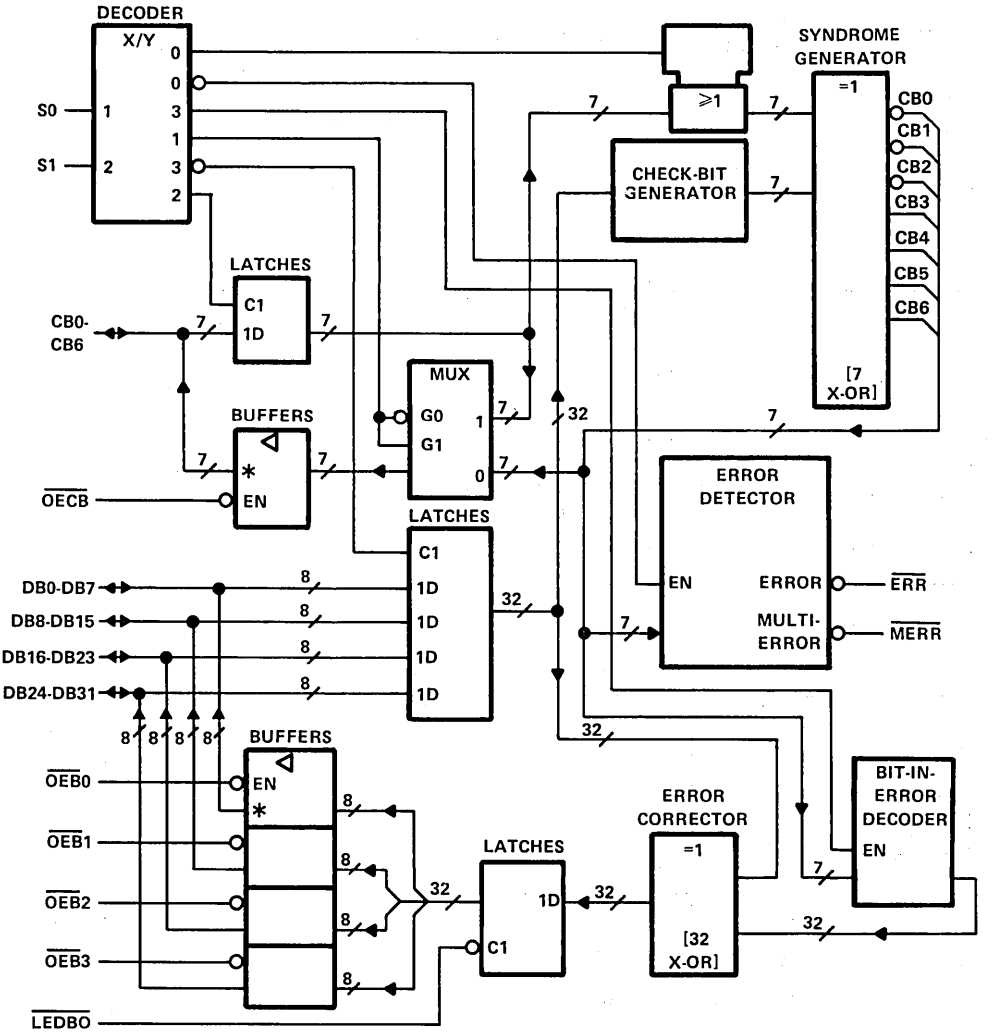
†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

TABLE 8. 'ALS634B, 'ALS635 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEDB}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	Input correct check bits	H	H	H
Latch input check bits while data input latch remains transparent	L	H	Input diagnostic data word†	H	Latched input check bits	H	Enabled	
Output input check bits	L	H	Input diagnostic data word†	H	Output input check bits	L	Enabled	
Latch diagnostic data into input latch	H	H	Latched input diagnostic data word	H	Output syndrome bits	L	Enabled	
					Hi-Z	H		
Output corrected diagnostic data word	H	H	Output corrected diagnostic data word	L	Output syndrome bits	L	Enabled	
					Hi-Z	H		

†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

'ALS632B, 'ALS633 logic diagram (positive logic)



*'ALS632B has a 3-state (▽) check-bit and data outputs.
'ALS633 has open-collector (◇) check-bit and data outputs.

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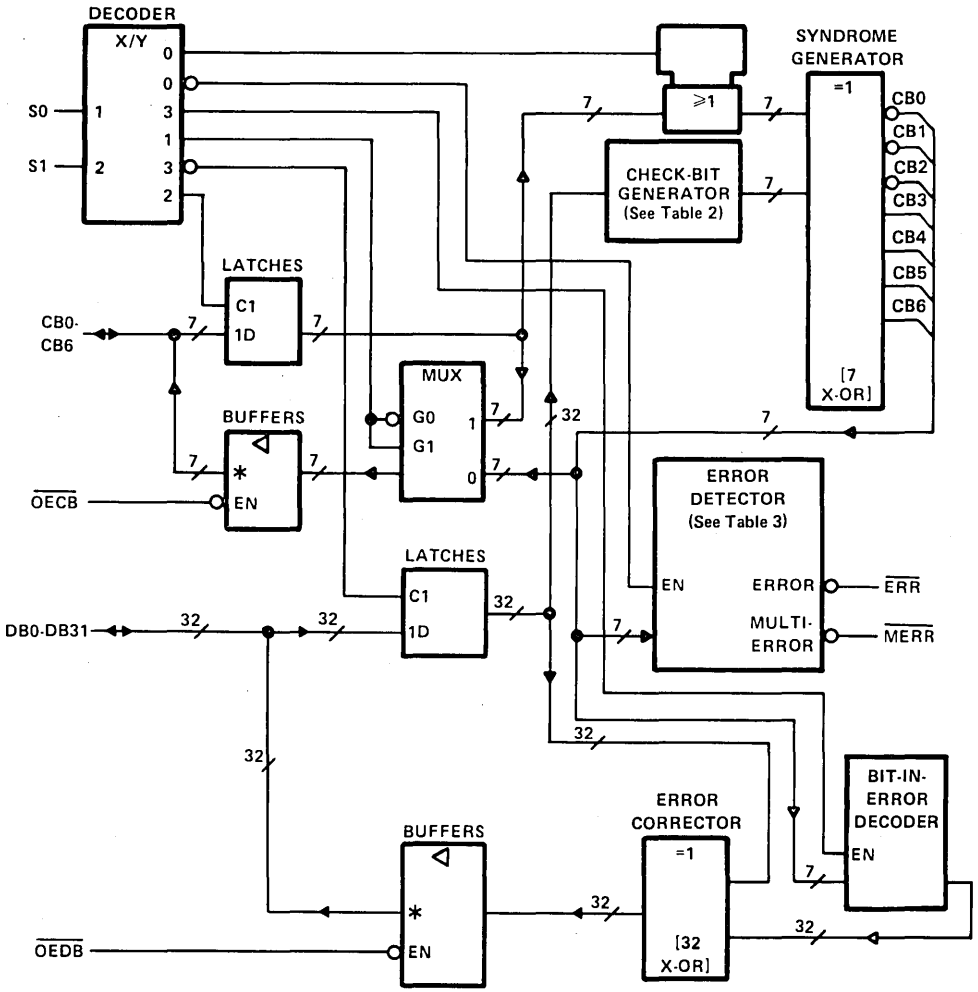
'ALS634B, 'ALS635 logic diagram (positive logic)



*'ALS634B has a 3-state (▽) check-bit and data outputs.
'ALS635 has open-collector (◇) check-bit and data outputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: CB and DB . . . . . 5.5 V
All others . . . . . 7 V
Operating free-air temperature range:
SN74ALS632B, SN74ALS634B . . . . . 0°C to 70°C
Operating case temperature range:
SN54ALS632B, SN54ALS634B . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS632B SN54ALS634B			SN74ALS632B SN74ALS634B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.6			0.8	V
I_{OH}	High-level output current	$\overline{ERR}$ or $\overline{MERR}$			−0.4			−0.4	mA
		DB or CB			−1			−2.6	
I_{OL}	Low-level output current	$\overline{ERR}$ or $\overline{MERR}$			4			8	mA
		DB or CB			12			24	
t_w	Pulse duration	$\overline{LEDBO}$ low	20			20			ns
t_{su}	Setup time	(1) Data and check word before S0↑ (S1 = H)	7			5			ns
		(2) S0 high before $\overline{LEDBO}$↑ (S1 = H)†	30			30			
		(3) $\overline{LEDBO}$ high before the earlier of S0↓ or S1↓†	0			0			
		(4) $\overline{LEDBO}$ high before S1↑ (S0 = H)	0			0			
		(5) Diagnostic data word before S1↑ (S0 = H)	7			5			
		(6) Diagnostic check word before the later of S1↓ or S0↑	10			7			
		(7) Diagnostic data word before $\overline{LEDBO}$↑ (S1 = L and S0 = H)‡	17			15			
t_h	Hold time	(8) Read-mode, S0 low and S1 high	27			25			ns
		(9) Data and check word after S0↑ (S1 = H)	12			10			
		(10) Data word after S1↑ (S0 = H)	12			10			
		(11) Check word after the later of S1↓ or S0↑	12			10			
		(12) Diagnostic data word after $\overline{LEDBO}$↑ (S1 = L, S0 = H)‡	0			0			
t_{corr}	Correction time (see Figure 1)§		43			37			ns
T_C	Operating case temperature				125				°C
T_A	Operating free-air temperature		−55			0		70	°C

† These times ensure that corrected data is saved in the output data latch.
‡ These times ensure that the diagnostic data word is saved in the output data latch.
§ The t_{corr} specification includes the minimum setup time $t_{su(1)}$. The correction time from S0 going high to valid data is equal to t_{corr} minus $t_{su(1)}$.

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electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION		SN54ALS632B			SN74ALS632B			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = Open,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	DB or CB	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others‡					20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	All others‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		157	250		157	250	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

switching characteristics over recommended ranges of supply voltage and operating temperature (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS632B		SN74ALS632B		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500Ω	5	32	5	30	ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500Ω	5	32	5	30	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500Ω	6	39	6	37	ns
	DB	$\overline{MERR}$	S1 = L, S0 = H, R_L = 500Ω	6	39	6	37	
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500Ω	5	35	5	32	ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500Ω	3	21	3	19	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500Ω	5	33	5	30	ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500Ω	3	20	3	18	ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500Ω	4	26	4	24	ns
t_{en}	$\overline{OECB}$↓	CB	S0 = H, S1 = X, R1 = R2 = 500Ω	1	24	1	22	ns
t_{dis}	$\overline{OECB}$↑	CB	S0 = H, S1 = X, R1 = R2 = 500Ω	1	22	1	20	ns
t_{en}	$\overline{OEB0}$ thru $\overline{OEB3}$↓	DB	S0 = H, S1 = X, R1 = R2 = 500Ω	1	24	1	22	ns
t_{dis}	$\overline{OEB0}$ thru $\overline{OEB3}$↑	DB	S0 = H, S1 = X, R1 = R2 = 500Ω	1	22	1	20	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1 of the *LSI Logic Data Book*, 1986.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS634B			SN74ALS634B			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	DB or CB	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others‡					20			20	
I_{IL}	S0, S1, or OEDB	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	All others‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		150	250		150	250	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

switching characteristics over recommended supply voltage range and operating temperature range (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS634B		SN74ALS634B		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	5	34	5	30	ns
			S1 = L, S0 = H, R_L = 500 Ω	5	34	5	30	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	6	39	6	37	ns
			S1 = L, S0 = H, R_L = 500 Ω	6	39	6	37	
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω	5	35	5	32	
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω	3	21	3	19	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω	5	33	5	30	ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω	4	26	4	24	ns
t_{en}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R1 = R2 = 500 Ω	1	24	1	22	ns
t_{dis}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R1 = R2 = 500 Ω	1	22	1	20	ns
t_{en}	$\overline{OEDB}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	1	24	1	22	ns
t_{dis}	$\overline{OEDB}$↑	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	1	22	1	20	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1 of the *LSI Logic Data Book,* 1986.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: CB and DB . . . . . 5.5 V
All others . . . . . 7 V
Operating free-air temperature range:
SN74ALS633 and SN74ALS635 . . . . . 0°C to 70°C
Operating case temperature range:
SN54ALS633 and SN54ALS635 . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS633 SN54ALS635			SN74ALS633 SN74ALS635			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.6			0.8	V
I_{OH}	High-level output current	$\overline{ERR}$ or $\overline{MERR}$			−0.4			−0.4	mA
		DB or CB 'ALS634A			−1			−2.6	
I_{OL}	Low-level output current	$\overline{ERR}$ or $\overline{MERR}$			4			8	mA
		DB or CB			12			24	
t_w	Pulse duration	$\overline{LEDBO}$ low	45			25			ns
t_{su}	Setup time	(1) Data and check word before S0↑ (S1 = H)	15			10			ns
		(2) S0 high before $\overline{LEDBO}$↑ (S1 = H)†	45			45			
		(3) $\overline{LEDBO}$ high before the earlier of S0↓ or S1↓†	0			0			
		(4) $\overline{LEDBO}$ high before S1↑ (S0 = H)	0			0			
		(5) Diagnostic data word before S1↑ (S0 = H)	28			10			
		(6) Diagnostic check word before the later of S1↓ or S0↑	15			10			
		(7) Diagnostic data word before $\overline{LEDBO}$↑ (S1 = L and S0 = H)‡	35			20			
t_h	Hold time	(8) Read-mode, S0 low and S1 high	35			30			ns
		(9) Data and check word after S0↑ (S1 = H)	20			15			
		(10) Data word after S1↑ (S0 = H)	20			15			
		(11) Check word after the later of S1↓ or S0↑	20			15			
		(12) Diagnostic data word after $\overline{LEDBO}$↑ (S1 = L, S0 = H)‡	0			0			
t_{corr}	Correction time (see Figure 1)§		65			58			ns
T_C	Operating case temperature				125				°C
T_A	Operating free-air temperature		−55			0		70	°C

† These times ensure that corrected data is saved in the output data latch.
‡ These times ensure that the diagnostic data word is saved in the output data latch.
§ The t_{corr} specification includes the minimum setup time $t_{su(1)}$. The correction time from S0 going high to valid data is equal to t_{corr} minus $t_{su(1)}$.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS633			SN74ALS633			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
I_{OH}	DB or CB	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others‡					20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	All others‡					−0.1			−0.1	
I_O§	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		150	250		150	250	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

switching characteristics over recommended ranges of supply voltage and operating temperature (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS633		SN74ALS633		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	10	43	10	40	ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω	10	43	10	40	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	15	67	15	55	ns
			S1 = L, S0 = H, R_L = 500 Ω	15	67	15	55	
t_{pd}	S0↓ and S1↓	CB	R_L = 680 Ω	10	75	10	60	ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω	5	30	5	25	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680 Ω	10	70	10	60	ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω	15	70	15	50	ns
t_{pd}	S1↑	CB	S0 = H, R_L = 680 Ω	10	60	10	45	ns
t_{PLH}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R_L = 680 Ω	2	35	2	30	ns
t_{PHL}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R_L = 680 Ω	2	35	2	30	ns
t_{PLH}	$\overline{OEB0}$ thru $\overline{OEB3}$↑	DB	S1 = X, S0 = H, R_L = 680 Ω	2	35	2	30	ns
t_{PHL}	$\overline{OEB0}$ thru $\overline{OEB3}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω	2	35	2	30	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1 of the *LSI Logic Data Book*, 1986.

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electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS635			SN74ALS635			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
I_{OH}	DB or CB	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V							mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V							
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	All others‡									
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
	All others‡									
I_O§	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		150			150		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

switching characteristics over recommended ranges of supply voltage and operating temperature (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS635			SN74ALS635			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω		26			26		ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω		26			26		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω		40			40		ns
			S1 = L, S0 = H, R_L = 500 Ω		40			40		
t_{pd}	S0↓ and S1↓	CB	R_L = 680 Ω		40			40		ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω		14			14		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680 Ω		40			40		ns
t_{pd}	S1↑	DB	S0 = H, R_L = 680 Ω		40			40		ns
t_{PLH}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PHL}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PLH}	$\overline{OEDB}$↑	DB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PHL}	$\overline{OEDB}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1 of the *LSI Logic Data Book*, 1986.

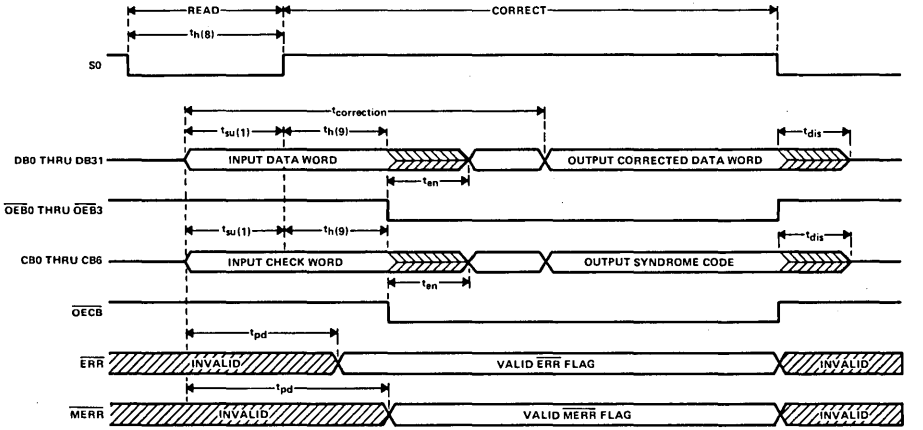

FIGURE 1. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

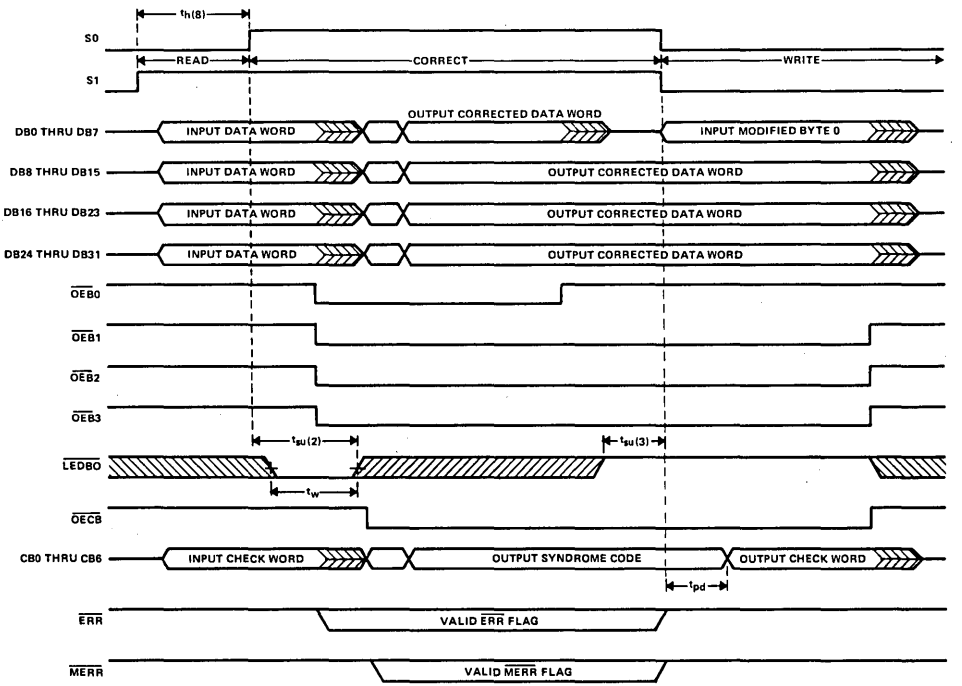

FIGURE 2. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

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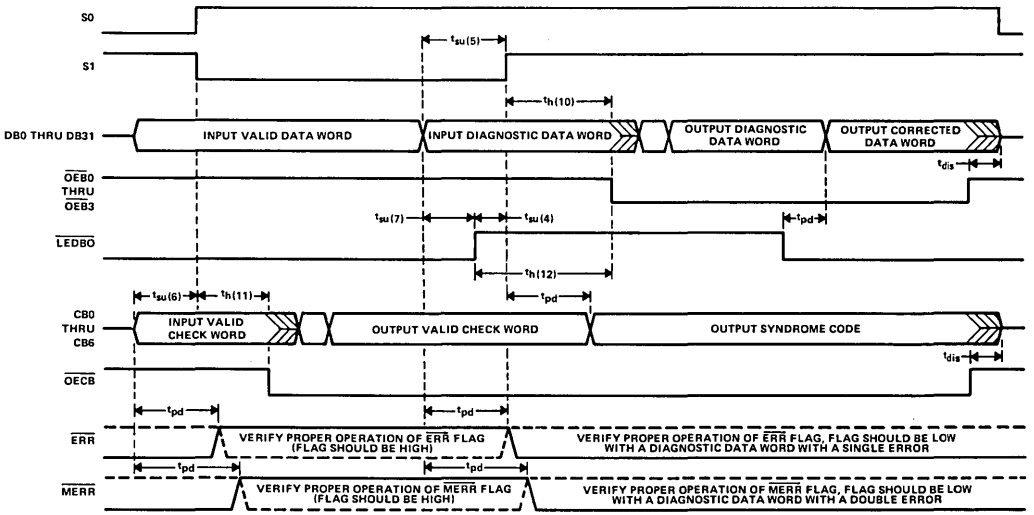


FIGURE 3. DIAGNOSTIC MODE SWITCHING WAVEFORM

32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

D2661, JANUARY 1986–REVISED JUNE 1987

- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Built-In Diagnostic Capability
- Fast Write and Read Cycle Processing Times
- Byte-Write Capability . . . 'AS632
- Dependable Texas Instruments Quality and Reliability

DEVICE	PACKAGE	BYTE-WRITE	OUTPUT
'AS632	52-pin	yes	3-State
'AS634	48-pin	no	3-State

description

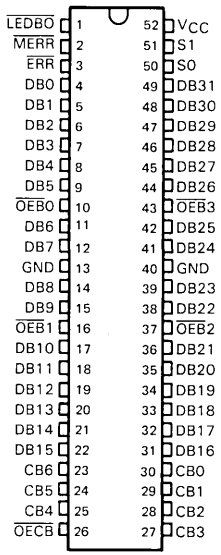
The 'AS632 and 'AS634 devices are 32-bit parallel error detection and correction circuits (EDACs) in 52-pin ('AS632) or 48-pin ('AS634) 600-mil packages. The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

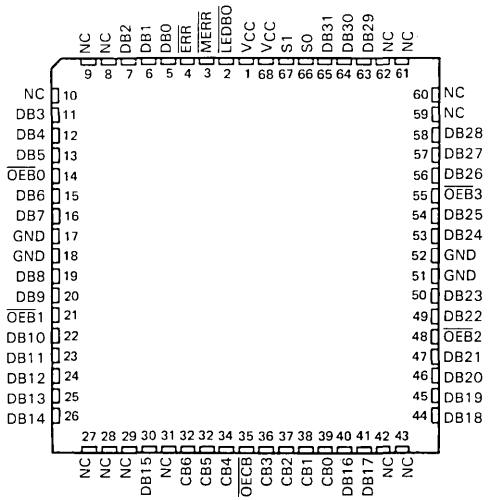
Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

'AS632 . . . JD PACKAGE
(TOP VIEW)



'AS632 . . . FN PACKAGE
(TOP VIEW)

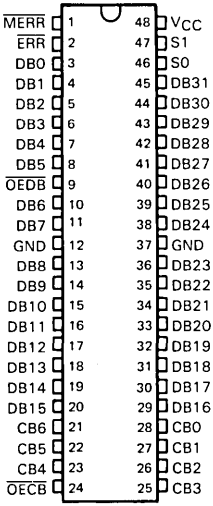


NC–No internal connection

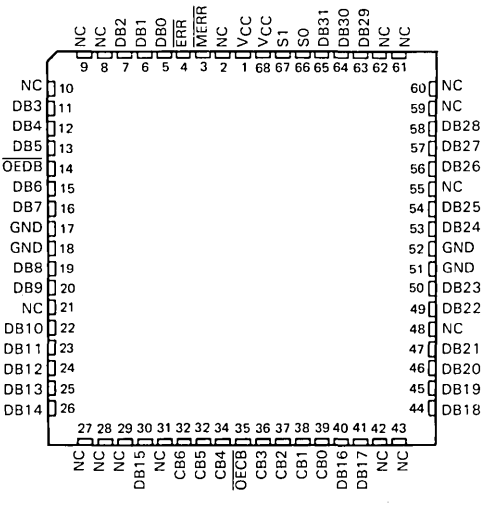
Read-modify-write (byte-control) operations can be performed with the 'AS632 EDAC by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEB0}}$ thru $\overline{\text{OEB3}}$ byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

'AS634 . . . JD PACKAGE
(TOP VIEW)



'AS634 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{\text{OEBn}}$ OR $\overline{\text{OEDB}}$	DB OUTPUT LATCH ('AS632) $\overline{\text{LEDBO}}$	CHECK I/O	CB CONTROL $\overline{\text{OECB}}$	ERROR FLAGS $\overline{\text{ERR}}$	ERROR FLAGS $\overline{\text{MERR}}$
Write	Generate check word	L	L	Input	H	X	Output check bits†	L	H	H

†See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction. CB0, CB1 and CB2 are odd parity bits and CB3, CB4, CB5, and CB6 are even parity bits. For example, for a data word of all zeros CB0-CB2 will be high and CB3-CB6 will be low.

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TABLE 2. PARITY ALGORITHM

CHECK WORD BIT	32-BIT DATA WORD																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X				X
CB1				X		X		X		X		X		X	X	X				X		X		X		X		X		X	X	X
CB2	X		X			X	X		X			X	X			X	X		X				X	X			X		X	X		X
CB3			X	X	X				X	X	X				X	X			X	X	X				X	X	X			X	X
CB4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{\text{MERR}}$ and a low on $\overline{\text{ERR}}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{\text{ERR}}$ and $\overline{\text{MERR}}$, which is the interrupt indication for the CPU.

TABLE 3. ERROR FUNCTION

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
32-BIT DATA WORD	7-BIT CHECK WORD	$\overline{\text{ERR}}$	$\overline{\text{MERR}}$	
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag ($\overline{\text{ERR}}$) will be set low while the dual error flag ($\overline{\text{MERR}}$) will remain high.

Any two-bit error will change the state of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.

TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEBn}$ OR $\overline{OEDB}$	DB OUTPUT LATCH ('AS632) $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$ $\overline{MERR}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled†
Read	Output corrected data & syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†

†See Table 3 for error description.
‡See Table 5 for error location.

As the corrected word is made available on the data I/O port (DB0 thru DB31), the check word I/O port (CB0 thru CB6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

TABLE 5. SYNDROME DECODING

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	L	L	L	L	L	L	unc
L	L	L	L	L	L	H	2-bit
L	L	L	L	L	H	L	2-bit
L	L	L	L	L	H	H	unc
L	L	L	L	H	L	L	2-bit
L	L	L	L	H	L	H	unc
L	L	L	L	H	H	L	unc
L	L	L	L	H	H	H	2-bit
L	L	L	H	L	L	L	2-bit
L	L	L	H	L	L	H	unc
L	L	L	H	L	H	L	DB31
L	L	L	H	L	H	H	2-bit
L	L	L	H	H	L	L	unc
L	L	L	H	H	L	H	2-bit
L	L	L	H	H	H	L	2-bit
L	L	L	H	H	H	H	DB30
L	L	H	L	L	L	L	2-bit
L	L	H	L	L	L	H	unc
L	L	H	L	L	H	L	DB29
L	L	H	L	L	H	H	2-bit
L	L	H	L	H	L	L	DB28
L	L	H	L	H	L	H	2-bit
L	L	H	L	H	H	L	2-bit
L	L	H	L	H	H	H	DB27
L	L	H	H	L	L	L	DB26
L	L	H	H	L	L	H	2-bit
L	L	H	H	L	H	L	2-bit
L	L	H	H	L	H	H	DB25
L	L	H	H	H	L	L	2-bit
L	L	H	H	H	L	H	DB24
L	L	H	H	H	H	L	unc
L	L	H	H	H	H	H	2-bit

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	H	L	L	L	L	L	2-bit
L	H	L	L	L	L	H	unc
L	H	L	L	L	H	L	DB7
L	H	L	L	L	H	H	2-bit
L	H	L	L	H	L	L	DB6
L	H	L	L	H	L	H	2-bit
L	H	L	L	H	H	L	2-bit
L	H	L	L	H	H	H	DB5
L	H	L	H	L	L	L	DB4
L	H	L	H	L	L	H	2-bit
L	H	L	H	L	H	L	2-bit
L	H	L	H	L	H	H	DB3
L	H	L	H	H	L	L	2-bit
L	H	L	H	H	L	H	DB2
L	H	L	H	H	H	L	unc
L	H	L	H	H	H	H	2-bit
L	H	H	L	L	L	L	DB0
L	H	H	L	L	L	H	2-bit
L	H	H	L	L	H	L	2-bit
L	H	H	L	L	H	H	unc
L	H	H	L	H	L	L	2-bit
L	H	H	L	H	L	H	DB1
L	H	H	L	H	H	L	unc
L	H	H	L	H	H	H	2-bit
L	H	H	H	L	L	L	2-bit
L	H	H	H	L	L	H	unc
L	H	H	H	L	H	L	unc
L	H	H	H	L	H	H	2-bit
L	H	H	H	H	L	L	unc
L	H	H	H	H	L	H	2-bit
L	H	H	H	H	H	L	2-bit
L	H	H	H	H	H	H	CB6

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	L	L	L	L	L	L	2-bit
H	L	L	L	L	L	H	unc
H	L	L	L	L	H	L	unc
H	L	L	L	L	H	H	2-bit
H	L	L	L	H	L	L	unc
H	L	L	L	H	L	H	2-bit
H	L	L	L	H	H	L	2-bit
H	L	L	L	H	H	H	unc
H	L	L	H	L	L	L	unc
H	L	L	H	L	L	H	2-bit
H	L	L	H	L	H	L	2-bit
H	L	L	H	L	H	H	DB15
H	L	L	H	H	L	L	2-bit
H	L	L	H	H	L	H	unc
H	L	L	H	H	H	L	DB14
H	L	L	H	H	H	H	2-bit
H	L	H	L	L	L	L	unc
H	L	H	L	L	L	H	2-bit
H	L	H	L	L	H	L	2-bit
H	L	H	L	L	H	H	DB13
H	L	H	L	H	L	L	2-bit
H	L	H	L	H	L	H	DB12
H	L	H	L	H	H	L	DB11
H	L	H	L	H	H	H	2-bit
H	L	H	H	L	L	L	2-bit
H	L	H	H	L	L	H	unc
H	L	H	H	L	H	L	DB10
H	L	H	H	L	H	H	DB9
H	L	H	H	L	H	L	2-bit
H	L	H	H	L	H	H	2-bit
H	L	H	H	H	L	L	DB8
H	L	H	H	H	L	H	2-bit
H	L	H	H	H	H	L	2-bit
H	L	H	H	H	H	H	CB5

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	H	L	L	L	L	L	unc
H	H	L	L	L	L	H	2-bit
H	H	L	L	L	H	L	2-bit
H	H	L	L	L	H	H	DB23
H	H	L	L	H	L	L	2-bit
H	H	L	L	H	L	H	DB22
H	H	L	L	H	H	L	DB21
H	H	L	L	H	H	H	2-bit
H	H	L	H	L	L	L	2-bit
H	H	L	H	L	L	H	DB20
H	H	L	H	L	H	L	DB19
H	H	L	H	L	H	H	2-bit
H	H	L	H	H	L	L	DB18
H	H	L	H	H	L	H	2-bit
H	H	L	H	H	H	L	2-bit
H	H	L	H	H	H	H	CB4
H	H	H	L	L	L	L	2-bit
H	H	H	L	L	L	H	DB16
H	H	H	L	L	H	L	unc
H	H	H	L	L	H	H	2-bit
H	H	H	L	H	L	L	DB17
H	H	H	L	H	L	H	2-bit
H	H	H	L	H	H	L	2-bit
H	H	H	L	H	H	H	CB3
H	H	H	H	L	L	L	unc
H	H	H	H	L	L	H	2-bit
H	H	H	H	L	H	L	2-bit
H	H	H	H	L	H	H	CB2
H	H	H	H	H	L	L	2-bit
H	H	H	H	H	L	H	CB1
H	H	H	H	H	H	L	CB0
H	H	H	H	H	H	H	none

CB X= error in check bit X
DB Y= error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'AS632 is capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{\text{LEDBO}}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{\text{OEB0}}$ through $\overline{\text{OEB3}}$ controls. $\overline{\text{OEB0}}$ controls DB0-DB7 (byte 0), $\overline{\text{OEB1}}$ controls DB8-DB15 (byte 1), $\overline{\text{OEB2}}$ controls DB16-DB23 (byte 2), and $\overline{\text{OEB3}}$ controls DB24-DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	BYTEn†	$\overline{OEB}$n†	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL	ERROR FLAG $\overline{ERR}$	ERROR FLAG $\overline{MERR}$
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled	
Read	Latch input data & check bits	H	H	Latched Input data	H	L	Latched input check word	H	Enabled	
Read	Latch corrected data word into output latch	H	H	Latched output data word	H	H	Hi-Z	H	Enabled	
							Output Syndrome bits	L		
Modify /write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTE0	H	H	Output check word	L	H	H
				Output unchanged BYTE0	L					

†$\overline{OEB}$0 controls DB0-DB7 (BYTE0), $\overline{OEB}$1 controls DB8-DB15 (BYTE1), $\overline{OEB}$3 controls DB16-DB23 (BYTE2), $\overline{OEB}$3 controls DB24-DB31 (BYTE3).

diagnostic operations

The 'AS632 and 'AS634 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the $\overline{ERR}$ flag should be low. If a diagnostic data word with two errors in any bit location is applied, the $\overline{MERR}$ flag should be low. After the checkword is latched into the input latch, it can be verified by taking $\overline{OECB}$ low. This outputs the latched checkword. With the 'AS632, the diagnostic data word can be latched into the output data latch and verified. It should be noted that the 'AS634 does not have this pass-through capability because they do not contain an output data latch. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 ('AS632) and Table 8 ('AS634) list the diagnostic functions.

TABLE 7. 'AS632 DIAGNOSTIC FUNCTION

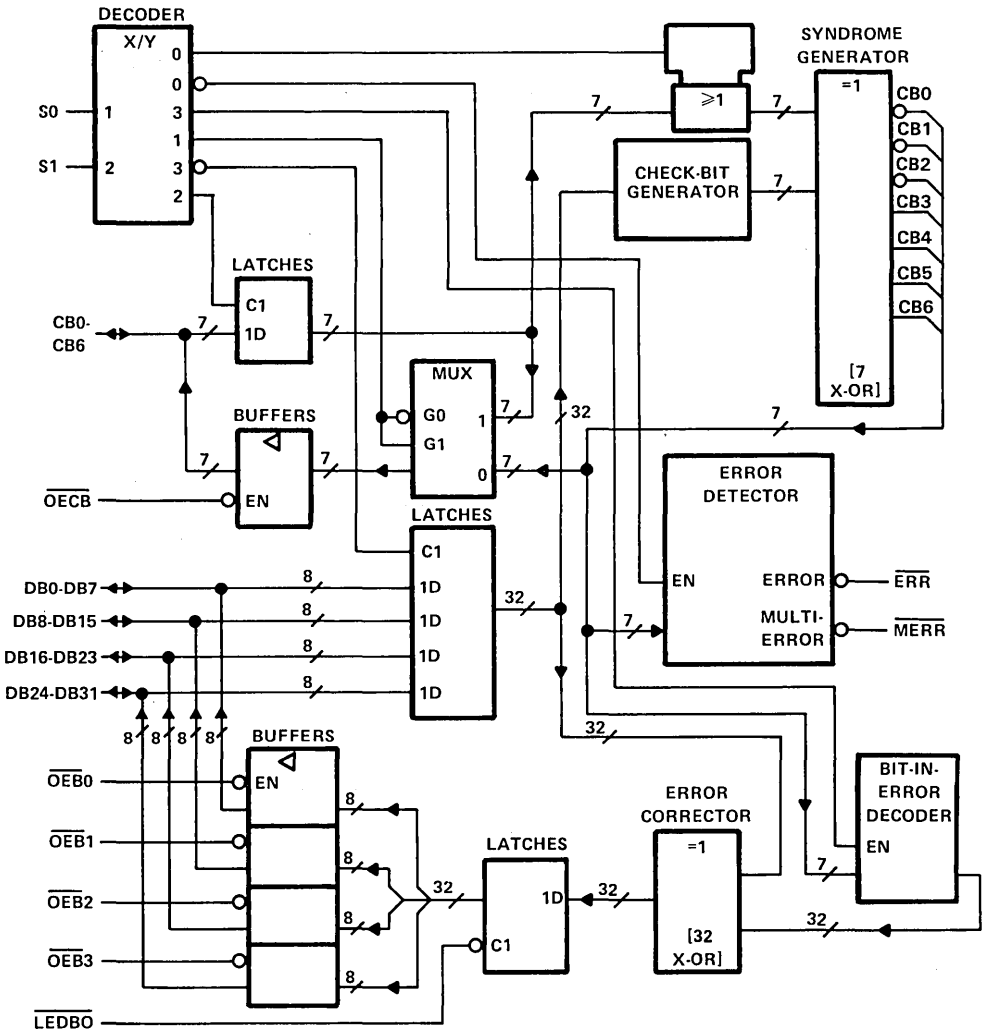
EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB BYTE CONTROL $\overline{OEBn}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains transparent	L	H	Input diagnostic data word†	H	L	Latched input check bits	H	Enabled	
Latch diagnostic data word into output latch	L	H	Input diagnostic data word†	H	H	Output latched check bits	L	Enabled	
						Hi-Z	H		
Latch diagnostic data word into input latch	H	H	Latched input diagnostic data word	H	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output diagnostic data word & syndrome bits	H	H	Output diagnostic data word	L	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output corrected diagnostic data word & output syndrome bits	H	H	Output corrected diagnostic data word	L	L	Output syndrome bits	L	Enabled	
						Hi-Z	H		

TABLE 8. 'AS634 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEDB}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	Input correct check bits	H	H	H
Latch input check bits while data input latch remains transparent	L	H	Input diagnostic data word†	H	Latched input check bits	H	Enabled	
Output input check bits	L	H	Input diagnostic data word†	H	Output input check bits	L	Enabled	
Latch diagnostic data into input latch	H	H	Latched input diagnostic data word	H	Output syndrome bits	L	Enabled	
					Hi-Z	H		
Output corrected diagnostic data word	H	H	Output corrected diagnostic data word	L	Output syndrome bits	L	Enabled	
					Hi-Z	H		

†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

'AS632 logic diagram (positive logic)



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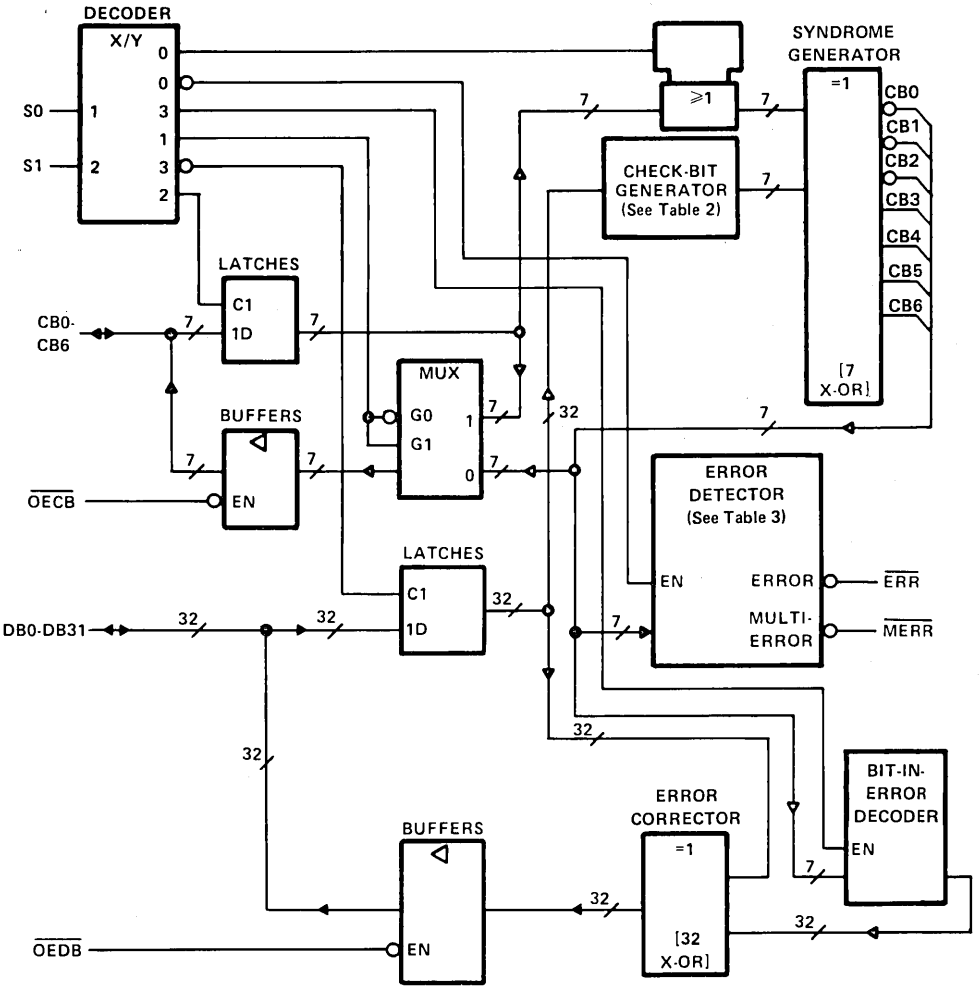
'AS634 logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: CB and DB . . . . . 5.5 V
All others . . . . . 7 V
Operating free-air temperature range:
SN74AS632, SN74AS634 . . . . . 0°C to 70°C
Operating case temperature range:
SN54AS632, SN54AS634 . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS632 SN54AS634			SN74AS632 SN74AS634			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	$\overline{ERR}$ or $\overline{MERR}$			−0.4			−0.4	mA
		DB or CB			−1			−2.6	
I_{OL}	Low-level output current	$\overline{ERR}$ or $\overline{MERR}$			4			8	mA
		DB or CB			12			24	
t_w	Pulse duration	$\overline{LEDBO}$ low	20			20			ns
t_{su}	Setup time	(1) Data and check word before S0↑ (S1 = H)	7			5			ns
		(2) S0 high before $\overline{LEDBO}$↑ (S1 = H)†	25			25			
		(3) $\overline{LEDBO}$ high before the earlier of S0↓ or S1↓†	0			0			
		(4) $\overline{LEDBO}$ high before S1↑ (S0 = H)	0			0			
		(5) Diagnostic data word before S1↑ (S0 = H)	7			5			
		(6) Diagnostic check word before the later of S1↓ or S0↑	10			7			
		(7) Diagnostic data word before $\overline{LEDBO}$↑ (S1 = L and S0 = H)‡	17			15			
t_h	Hold time	(8) Read-mode, S0 low and S1 high	27			25			ns
		(9) Data and check word after S0↑ (S1 = H)	12			10			
		(10) Data word after S1↑ (S0 = H)	12			10			
		(11) Check word after the later of S1↓ or S0↑	12			10			
		(12) Diagnostic data word after $\overline{LEDBO}$↑ (S1 = L, S0 = H)‡	0			0			
t_{corr}	Correction time (see Figure 1)§		38			32			ns
T_C	Operating case temperature				125				°C
T_A	Operating free-air temperature		−55			0		70	°C

† These times ensure that corrected data is saved in the output data latch.
‡ These times ensure that the diagnostic data word is saved in the output data latch.
§ The t_{corr} specification includes the minimum setup time $t_{su(1)}$. The correction time from S0 going high to valid data is equal to t_{corr} minus $t_{su(1)}$.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS632			SN74AS632			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = Open,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	DB or CB	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	DB or CB‡	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others‡					20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	All others‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		200	300		200	300	mA

NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

switching characteristics over recommended supply voltage range and operating temperature range (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54AS632		SN74AS632		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	4	27	4	25	ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω	4	27	4	25	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	5	34	5	32	ns
	DB	$\overline{MERR}$	S1 = L, S0 = H, R_L = 500 Ω	5	34	5	32	
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω	4	32	4	28	ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω	2	19	2	17	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500Ω	4	29	4	26	ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500Ω	2	18	2	16	ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500Ω	3	22	3	20	ns
t_{en}	$\overline{OECB}$↓	CB	S0 = H, S1 = X, R1 = R2 = 500Ω	1	19	1	17	ns
t_{dis}	$\overline{OECB}$↑	CB	S0 = H, S1 = X, R1 = R2 = 500Ω	1	17	1	15	ns
t_{en}	$\overline{OEB0}$ thru $\overline{OEB3}$↓	DB	S0 = H, S1 = X, R1 = R2 = 500Ω	1	19	1	17	ns
t_{dis}	$\overline{OEB0}$ thru $\overline{OEB3}$↑	DB	S0 = H, S1 = X, R1 = R2 = 500Ω	1	17	1	15	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1 of the *LSI Logic Data Book*, 1986.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS634			SN74AS634			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	DB or CB	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	DB or CB‡	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others‡					20			20	
I_{IL}	S0, S1 or OEDB	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	All others‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		200	300		200	300	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

switching characteristics over recommended supply voltage range and operating temperature range (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54AS634		SN74AS634		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	4	30	4	25	ns
			S1 = L, S0 = H, R_L = 500 Ω	4	30	4	25	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	5	34	5	32	ns
			S1 = L, S0 = H, R_L = 500 Ω	5	34	5	32	
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω	4	32	4	28	
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω	2	19	2	17	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω	4	29	4	26	ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω	3	22	3	20	ns
t_{en}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R1 = R2 = 500 Ω	1	19	1	17	ns
t_{dis}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R1 = R2 = 500 Ω	1	17	1	15	ns
t_{en}	$\overline{OEDB}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	1	19	1	17	ns
t_{dis}	$\overline{OEDB}$↑	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	1	17	1	15	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1 of the *LSI Logic Data Book*, 1986.

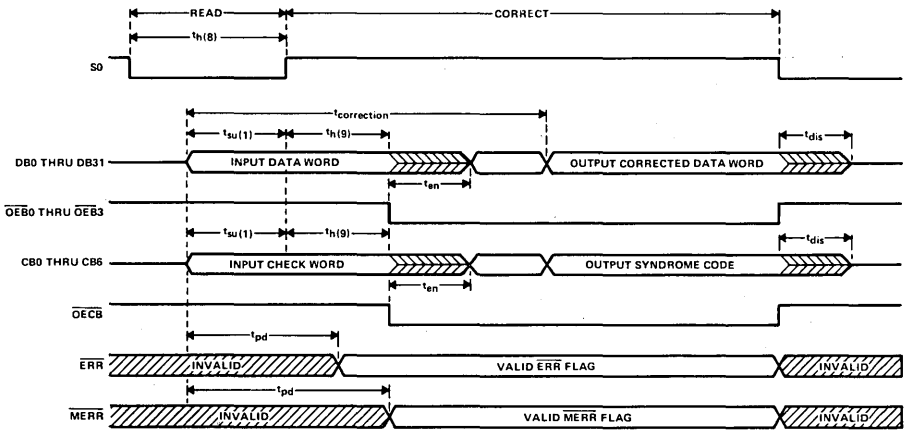


FIGURE 1. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

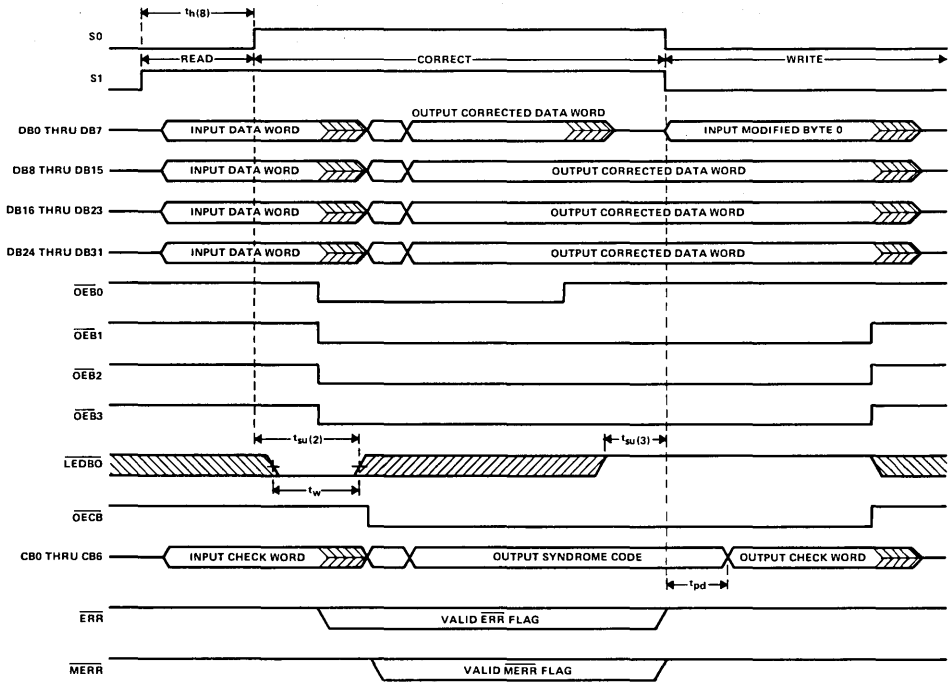


FIGURE 2. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

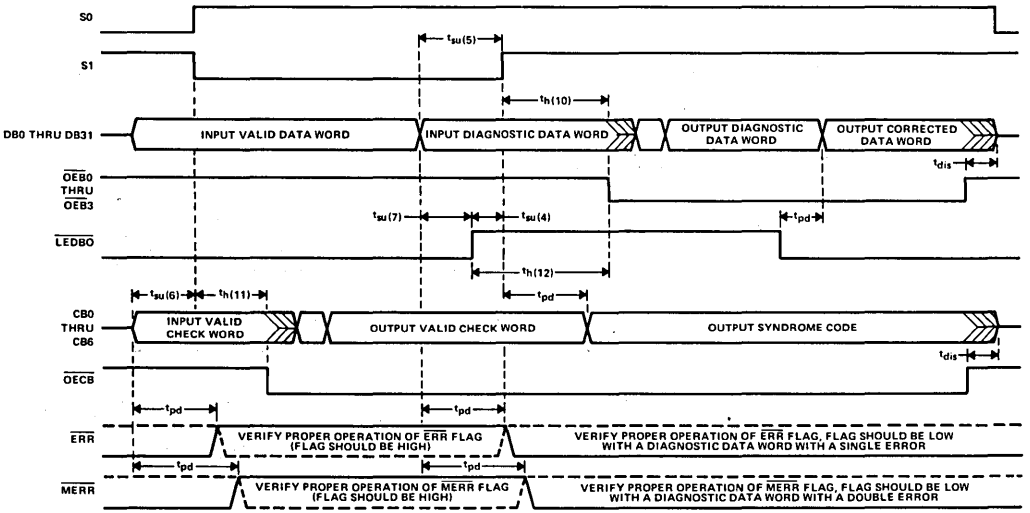
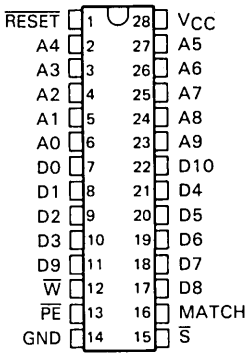


FIGURE 3. DIAGNOSTIC MODE SWITCHING WAVEFORM

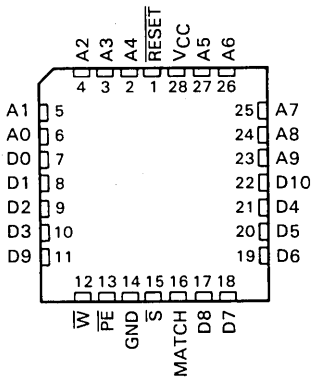
D3105, SEPTEMBER 1987 – REVISED MARCH 1988

- Fast Address to Match Delay
  'ACT2151 25 and xx ns Max
  'ACT2153 28 and xx ns Max
- On-Chip Address/Data Comparator
- On-Chip Parity Generator and Checking
- Parity Error Output, Force Parity Error Input
- Easily Expandable
- Choice of Open-Drain or Totem-Pole MATCH Output
- EPIC™ (Enhanced Performance Implanted CMOS) 1-μm Process
- Fully TTL-Compatible

JD OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The 'ACT2151 and 'ACT2153 cache address comparators consist of a high-speed 1K × 12 static RAM array, parity generator, parity checker, and 12-bit high-speed comparator. They are fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. These cache address comparators are easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with these devices. The 'ACT2151 has a totem-pole match output while the 'ACT2153 has an open-drain MATCH output for easy AND-tying.

If $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A9 with the data D0-D10 plus generated parity. An equality is indicated by a high level on the MATCH output. A low-level output on $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D10 plus generated odd parity are written in the 12-bit memory location addressed by A0-A10. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 1K × 12 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high after reset for every addressed memory location, indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit must be tied high regardless of the address width.

EPIC is a trademark of Texas Instruments Incorporated.

These cache address comparators operate from a single 5-V supply and are offered in 28-pin 600-mil ceramic side-brazed, plastic dual-in-line, or PLCC packages.

The SN74ACT2151 and SN74ACT2153 are characterized for operation from 0°C to 70°C.

MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: (A0-A9) = D0-D10 + parity,
or: $\overline{RESET}$ = V_{IL},
or: $\overline{S}$ = V_{IH},
or: $\overline{W}$ = V_{IL}

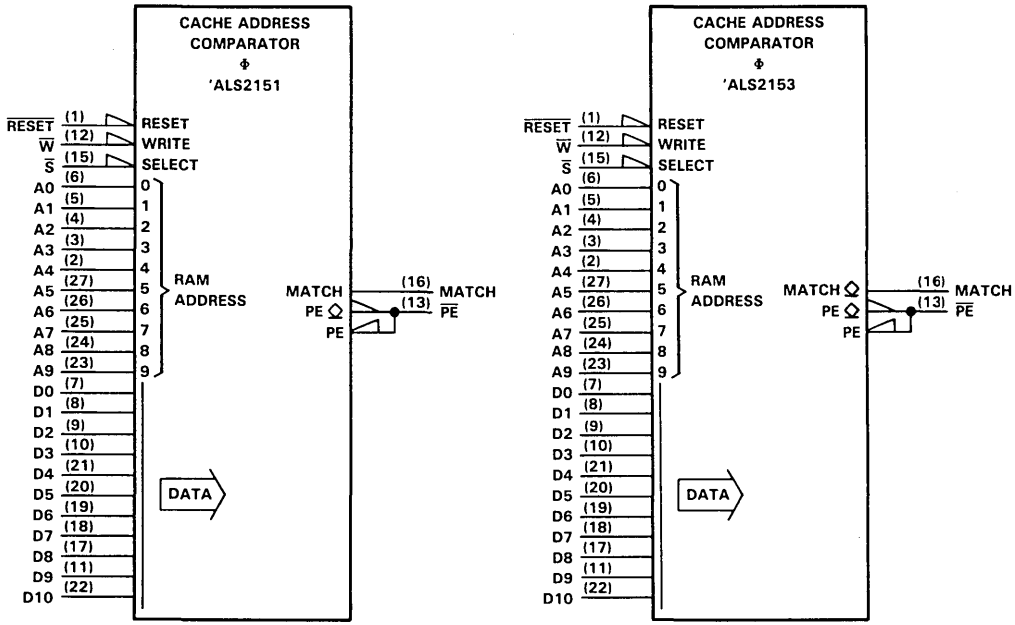
MATCH = V_{OL} if: (A0-A9) ≠ D0-D10 + parity,
with $\overline{RESET}$ = V_{IH},
$\overline{S}$ = V_{IL}, and $\overline{W}$ = V_{IH}

FUNCTION TABLE

INPUTS			OUTPUTS		FUNCTION
$\overline{W}$	$\overline{S}$	$\overline{RESET}$	MATCH	$\overline{PE}$	
H	L	H	L	L	Parity error
			L	H	Not equal
			H	L	Undefined error
			H	H	Equal
L	L	H	H	IN	Write
X	H	H	H	H	Device disabled
X	X	L	H	†	Memory reset

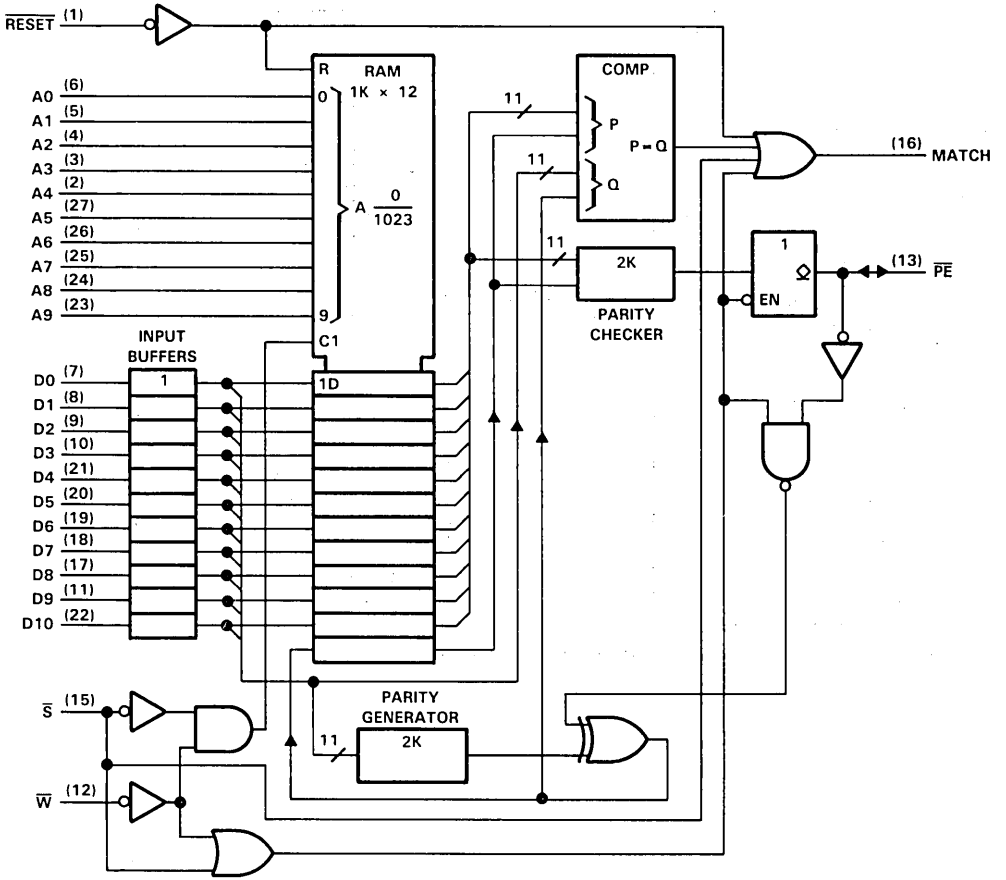
† The state of $\overline{PE}$ is dependent on inputs $\overline{W}$ and $\overline{S}$.

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
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PIN NAME	PIN NO.	DESCRIPTION
A0	6	Address inputs, Addresses 1 of 1024 random access memory locations. Must be stable for the duration of the write cycle.
A1	5	
A2	4	
A3	3	
A4	2	
A5	27	
A6	26	
A7	25	
A8	24	
A9	23	
D0	7	Data inputs. Compared with memory locations addressed by A0-A9 when $\overline{W}$ is at V_{IH} and $\overline{S}$ is at V_{IL}. Provides input data to the RAM when $\overline{W}$ and $\overline{S}$ are at V_{IL}.
D1	8	
D2	9	
D3	10	
D4	21	
D5	20	
D6	19	
D7	18	
D8	17	
D9	11	
D10	22	
GND	14	Ground
MATCH	16	When MATCH output is at V_{OH} during a compare cycle, D0-D10 plus generated parity equals the contents of the 12-bit memory location addressed by A0-A10. MATCH is also driven high during deselect and reset. Since the 'ACT2153 features an open-drain MATCH output, an external pull-up resistor of 220 Ω minimum is required.
$\overline{PE}$	13	Parity error input/output. During compare cycles. $\overline{PE}$ at V_{OL} indicates a parity error in the stored data. During write cycles, $\overline{PE}$ can force a parity error into the 12th-bit location specified by A0-A9 when $\overline{PE}$ is taken to V_{IL}. $\overline{PE}$ is an open-drain output so an external pull-up resistor of 220 Ω minimum is required.
$\overline{RESET}$	1	Reset input. Asynchronously clears entire RAM array to zero and forces MATCH high when $\overline{RESET}$ is at V_{IL}.
$\overline{S}$	15	Chip select input. Enables device when $\overline{S}$ is at V_{IL}. Deselects device and forces MATCH and $\overline{PE}$ high when $\overline{S}$ is at V_{IH}.
V_{CC}	28	Supply voltage
$\overline{W}$	12	Write control input. Writes D0-D0 and generated parity into RAM and forces MATCH high when $\overline{W}$ and $\overline{S}$ are at V_{IL}. Places selected device in compare mode when $\overline{W}$ is at V_{IH}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −1.5 to 7 V
Input voltage, any input . . . . . −1.5 to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range. . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2.2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage (See Note 2)		−0.5		0.8	V
V_{OH}	High-level output voltage, MATCH ('ACT2153) and $\overline{PE}$ outputs only				5.5	V
I_{OH}	High-level output current, MATCH ('ACT2151)				−8	mA
I_{OL}	Low-level output current	MATCH – 'ACT2151			8	mA
		MATCH – 'ACT2153			24	mA
		$\overline{PE}$			24	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, in which the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN74ACT2151-25 SN74ACT2153-28			SN74ACT2151-xx SN74ACT2153-xx			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{OH}	High-level output current	MATCH ('ACT2153) and $\overline{PE}$	V_{OH} = 5.5 V, V_{CC} = 5.5 V			5			5	μA
V_{OH}	High-level output voltage	MATCH ('ACT2151)	I_{OH} = −8 mA, V_{CC} = 4.5 V	3.7			3.7			V
V_{OL}	Low-level output voltage	MATCH - 'ACT2153	I_{OL} = 24 mA, V_{CC} = 4.5 V			0.4			0.4	V
		MATCH - 'ACT2151	I_{OL} = 8 mA, V_{CC} = 4.5 V			0.4			0.4	
		$\overline{PE}$	I_{OL} = 24 mA, V_{CC} = 4.5 V			0.4			0.4	
I_I	Input current		V_I = 0–V_{CC}, V_{CC} = 5.5 V			±1			±1	μA
I_{OS}‡	Short-circuit output current	MATCH ('ACT2151)	V_O = 0, V_{CC} = 5.5 V	50		150	50		150	mA
I_{CC1}	Supply current (operative)		$\overline{RESET}$ at 3 V, $\overline{S}$ at 0 V, V_{CC} = 5.5 V		85			85		mA
I_{CC2}	Supply current (reset)		$\overline{RESET}$ at 0 V, $\overline{S}$ at 0 V, V_{CC} = 5.5 V		5			5		mA
I_{CC3}	Supply current (deselected)		$\overline{RESET}$ at 3 V, $\overline{S}$ at 3 V, V_{CC} = 5.5 V		75			75		mA
C_i	Input capacitance		f = 1 MHz			5			5	pF
C_o	Output capacitance		f = 1 MHz			6			6	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), see Figures 1, 2, and 3

PARAMETER		SN74ACT2151-25			SN74ACT2151-xx			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A-M)}$	Access time from address to MATCH		19			28		ns
$t_{a(A-PH)}$	Access time from address to $\overline{PE}$ high		21			27		ns
$t_{a(A-PL)}$	Access time from address to $\overline{PE}$ low		23			29		ns
$t_{a(S-M)}$	Access time from $\overline{S}$ to MATCH		9			15		ns
$t_{p(D-M)}$	Propagation time, data inputs to MATCH		10			15		ns
$t_{p(RST-MH)}$	Propagation time, $\overline{RESET}$ low to MATCH high		7			11		ns
$t_{p(S-MH)}$	Propagation time, $\overline{S}$ high to MATCH high		5			8		ns
$t_{p(W-MH)}$	Propagation time, $\overline{W}$ low to MATCH high		5			8		ns
$t_{p(W-PH)}$	Propagation time, $\overline{W}$ low to $\overline{PE}$ high		7			9		ns
$t_{v(A-M)}$	MATCH valid time after change of address		5			5		ns
$t_{v(D-M)}$	MATCH valid time after change of data		5			5		ns
$t_{v(S-M)}$	MATCH valid time (low) after $\overline{S}$ high		5			5		ns
$t_{v(A-P)}$	$\overline{PE}$ valid time after change of address		10			10		ns

PARAMETER		SN74ACT2153-25			SN74ACT2153-xx			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A-M)}$	Access time from address to MATCH		19			28		ns
$t_{a(A-PH)}$	Access time from address to $\overline{PE}$ high		23			29		ns
$t_{a(A-PL)}$	Access time from address to $\overline{PE}$ low		25			31		ns
$t_{a(S-M)}$	Access time from $\overline{S}$ to MATCH		9			15		ns
$t_{p(D-M)}$	Propagation time, data inputs to MATCH		10			15		ns
$t_{p(RST-MH)}$	Propagation time, $\overline{RESET}$ low to MATCH high		7			11		ns
$t_{p(S-MH)}$	Propagation time, $\overline{S}$ high to MATCH high		5			8		ns
$t_{p(W-MH)}$	Propagation time, $\overline{W}$ low to MATCH high		5			8		ns
$t_{p(W-PH)}$	Propagation time, $\overline{W}$ low to $\overline{PE}$ high		7			9		ns
$t_{v(A-M)}$	MATCH valid time after change of address		5			5		ns
$t_{v(D-M)}$	MATCH valid time after change of data		5			5		ns
$t_{v(S-M)}$	MATCH valid time (low) after $\overline{S}$ high		5			5		ns
$t_{v(A-P)}$	$\overline{PE}$ valid time after change of address		10			10		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	SN74ACT2151-25 SN74ACT2153-28			SN74ACT2151-xx SN74ACT2153-xx			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{w(RSTL)}$	Pulse duration, $\overline{RESET}$ low	30			30			ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low, without writing $\overline{PE}$	15			15			ns
$t_{w(WL)PE}$	Pulse duration, $\overline{W}$, writing $\overline{PE}$ (see Note 3)	15			15			ns
$t_{su(A)}$	Address setup time before $\overline{W}$ low	0			0			ns
$t_{su(D)}$	Data setup time before $\overline{W}$ high	10			10			ns
$t_{su(P)}$	$\overline{PE}$ setup time before $\overline{W}$ high (see Note 3)	10			20			ns
$t_{su(S)}$	Chip select setup time before $\overline{W}$ high	10			20			ns
$t_{su(RST)}$	$\overline{RESET}$ inactive setup time before $\overline{W}$ high	15			15			ns
$t_{h(A)}$	Address hold time after $\overline{W}$ high	0			0			ns
$t_{h(WH-D)}$	Data hold time after $\overline{W}$ high	5			5			ns
$t_{h(WL-D)}$	Data hold time after $\overline{W}$ low with MATCH high, (see Note 4)	10			10			ns
$t_{h(P)}$	$\overline{PE}$ hold time after $\overline{W}$ high	0			0			ns
$t_{h(S)}$	Chip select hold time after $\overline{W}$ high	0			0			ns
t_{AVWH}	Address valid to write enable high	15			15			ns

NOTES: 3. Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle timing when writing a parity error.

4. $t_{h(WL-D)}$ guarantees that when $\overline{W}$ is taken low during a compare cycle with MATCH high, match will remain high without a glitch low. (As shown in the function table, $\overline{W}$ low forces MATCH high). $t_{h(WL-D)}$ is guaranteed indirectly by $t_{v(D-M)}$ and $t_{p(W-MH)}$.

PARAMETER MEASUREMENT INFORMATION

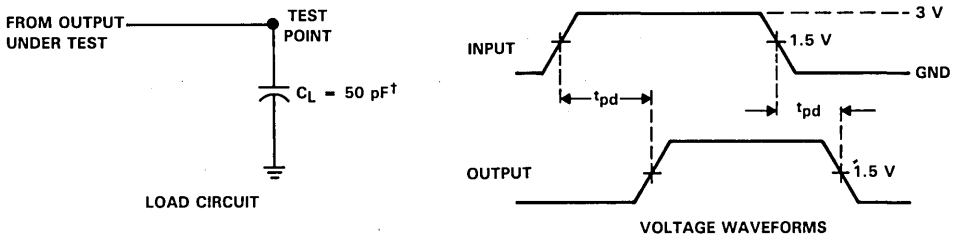


FIGURE 1. TACT2151 MATCH OUTPUT

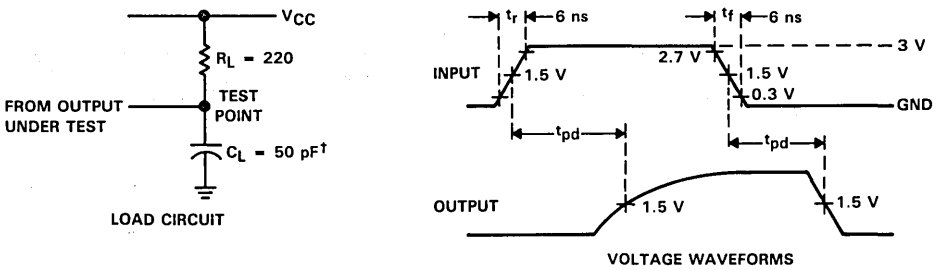


FIGURE 2. OPEN-DRAIN MATCH AND $\overline{PE}$ OUTPUTS

PARAMETER		R_L	C_L†	S1	S2
t_{en}	t_{PZH}	640 Ω	50 pF	OPEN	CLOSED
	t_{PZL}			CLOSED	OPEN
t_{dis}	t_{PHZ}	640 Ω	50 pF	OPEN	CLOSED
	t_{PLZ}			CLOSED	OPEN
t_{pd} or t_t		—	50 pF	OPEN	OPEN

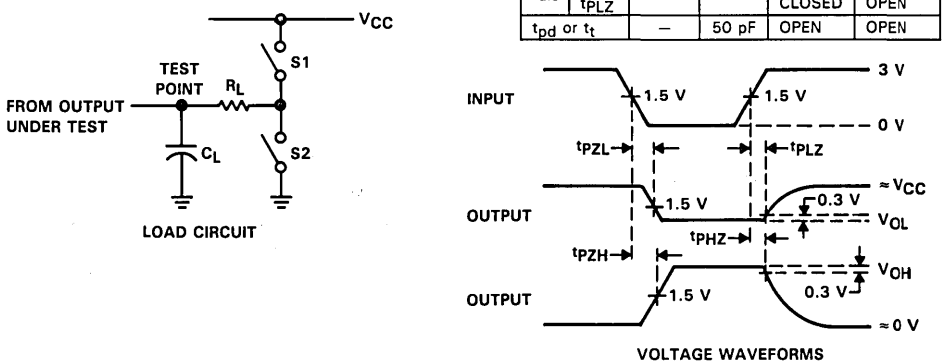
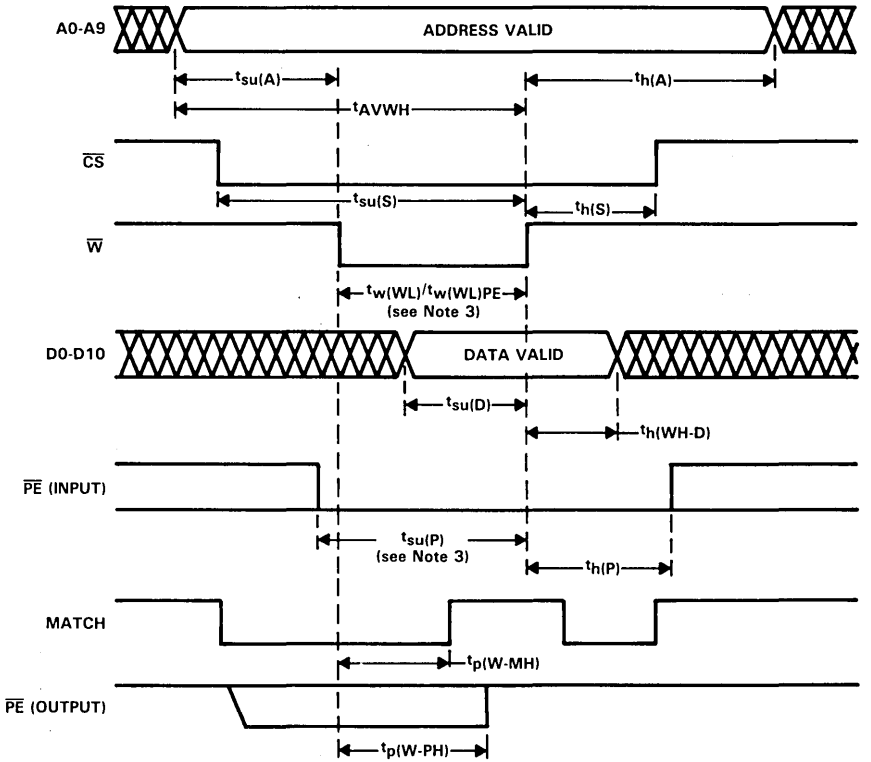


FIGURE 3. 3-STATE DATA OUTPUTS

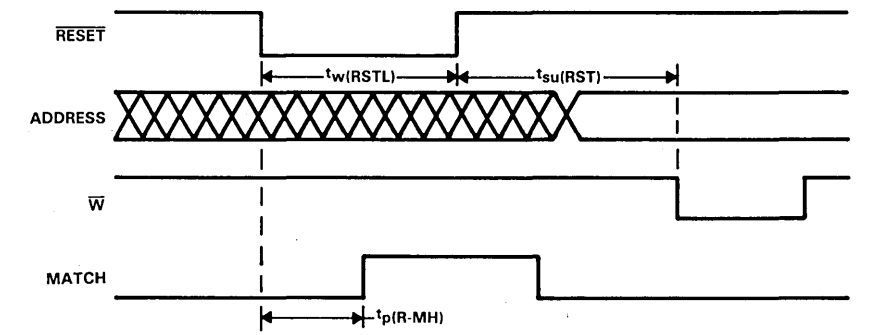
†C_L includes probe and test fixture capacitance.

PARAMETER MEASUREMENT INFORMATION

write cycle timing



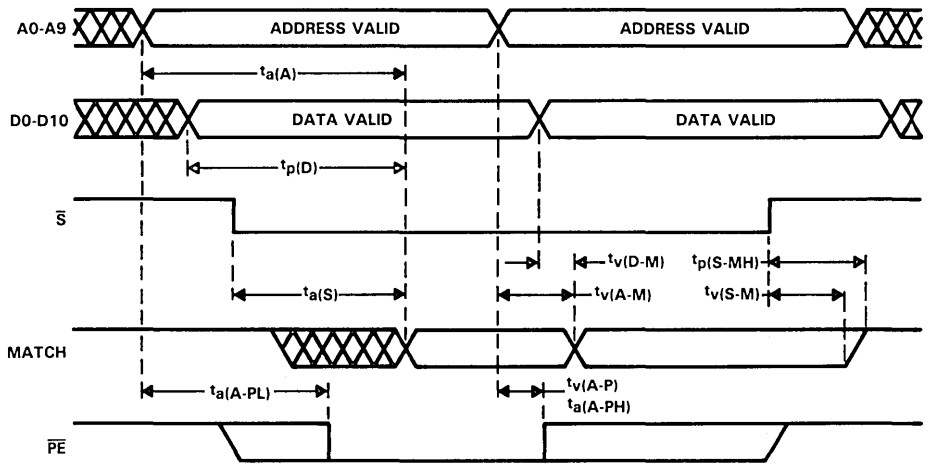
reset cycle timing



NOTE 3: Parameters $t_{w(WL)PE}$ and $t_{su(P)}$ apply only during the write cycle when writing a parity error.

PARAMETER MEASUREMENT INFORMATION

compare cycle timing



TYPICAL APPLICATION INFORMATION

cascading the 'ACT2151 and 'ACT2153

The 'ACT2151 and 'ACT2153 are easily cascaded in width and depth. Wider addresses can be compared by driving the A0-A9 inputs of each device with the same index and applying the additional address bits to the D0-D10 inputs. The select ($\overline{S}$) input allows these devices to be cascaded in depth. When a device is deselected, the MATCH output is driven high. It should be noted that a decoder can be used to drive the select inputs since the propagation delay from select to match is much faster than from address to match. MATCH on the 'ACT2153 is an open-drain output for easy AND-tying. Figure 4 shows the 'ACT2153 cascaded.

cache coherency through bus watching

When cache designs are implemented, the problem of cache coherency is always a concern. One solution to this problem is to implement bus-watching using the 'ACT2151 or 'ACT2153. By storing the same tags in the bus-watcher RAM as are stored in the cache tag RAM, the bus-watcher will indicate a hit every time a cache address passes down the main address bus. If data is being modified in main memory, the index can be passed to the cache tag RAM for invalidation. Figure 5 shows a possible bus-watcher implementation.

application

Due to the high-performance switching characteristics of the 'ACT2151 and 'ACT2153, it is necessary that the address inputs not be allowed to float in the three-state condition. Proper termination techniques should be employed. It is recommended that the RC time constant associated with the address inputs (63.2% of rise time at A0-A9) not exceed 60 ns.

TYPICAL APPLICATION INFORMATION

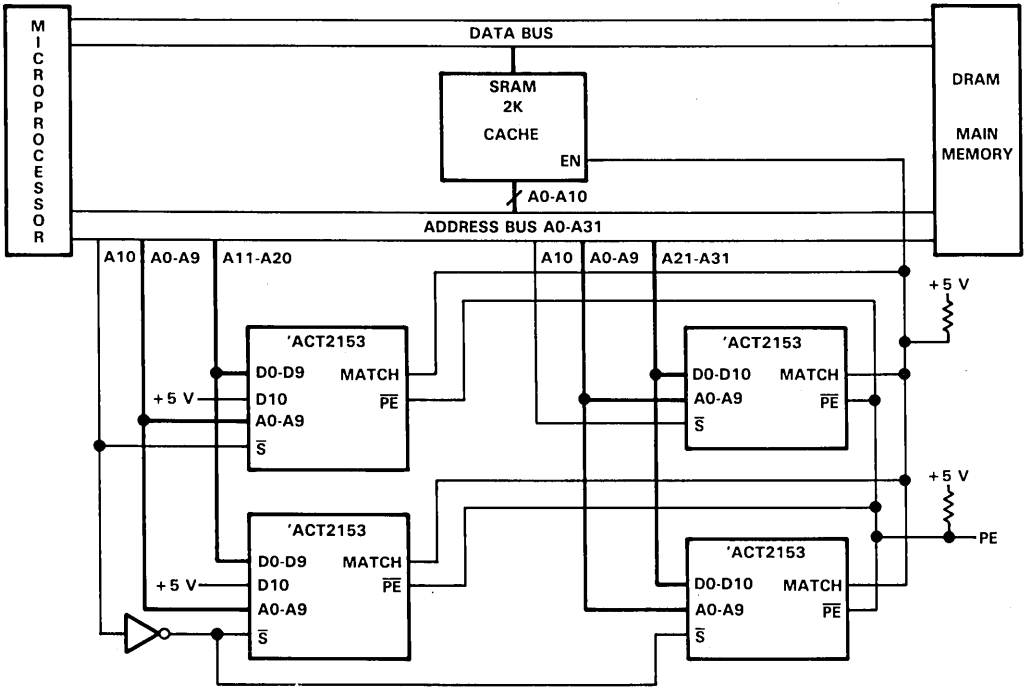


FIGURE 4. CASCADING THE 'ACT2153

TYPICAL APPLICATION INFORMATION

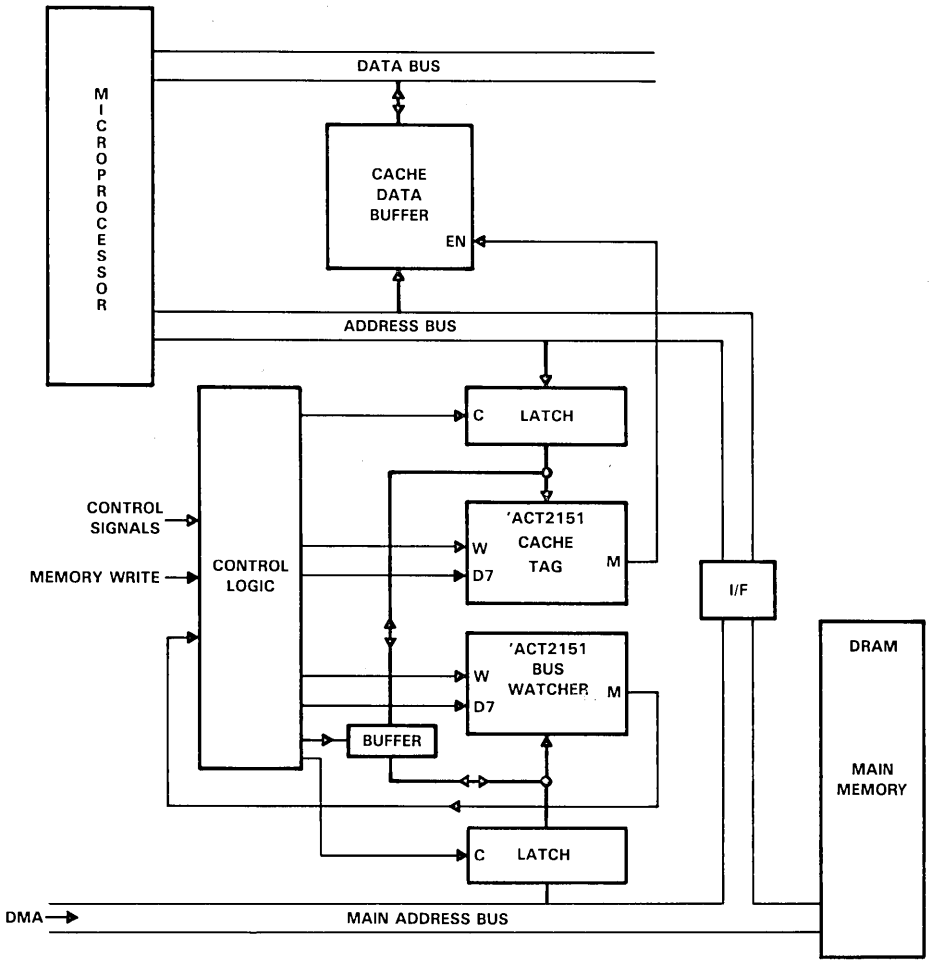
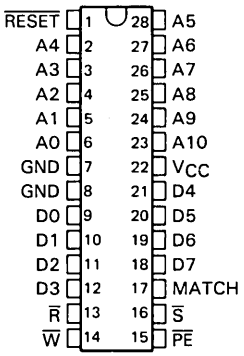


FIGURE 5. BUS WATCHING USING THE 'ACT2151

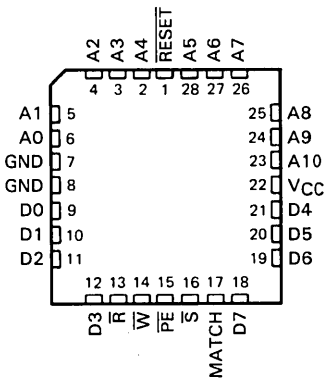
D3050, SEPTEMBER 1987—REVISED NOVEMBER 1987

- Fast Address to Match Delay 25 or 35 ns Max
- Common I/O with Read Feature
- On-Chip Address/Data Comparator
- On-Chip Parity Generator and Checking
- Parity Error Output, Force Parity Error Input
- Easily Expandable
- Choice of Open-Drain or Totem-Pole MATCH Output
- EPIC™ (Enhanced Performance Implanted CMOS) 1-μm Process
- Fully TTL-Compatible

JD OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The 'ACT2152 and 'ACT2154 cache address comparators consist of a high-speed 2K × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. They are fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. These cache address comparators are easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with these devices. The 'ACT2152 has a totem-pole MATCH output while the 'ACT2154 has an open-drain MATCH output for easy AND-tying.

If $\overline{S}$ is low and $\overline{W}$ and $\overline{R}$ are high, the cache address comparator compares the contents of the memory location addressed by A0-A10 with the data D0-D7 plus generated parity. An equality is indicated by a high level on the MATCH output. A low-level output on $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated odd parity are written in the 9-bit memory location addressed by A0-A10. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

EPIC is a trademark of Texas Instruments Incorporated.

A read mode is provided with the 'ACT2152 and 'ACT2154, which allows the contents of RAM to be read at the D0-D7 pins. The read mode is selected when $\overline{R}$ and $\overline{S}$ are low, and $\overline{W}$ is high.

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 2K × 9 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high after reset for every addressed memory location, indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit must be tied high regardless of the address width.

These cache address comparators operate from a single +5-V supply and are offered in 28-pin 600-mil ceramic side-brazed, plastic dual-in-line, or PLCC packages.

The 'ACT2152 and 'ACT2154 are characterized for operation from 0°C to 70°C.

MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A10] = D0-D7 + parity,
or: $\overline{RESET}$ = V_{IL},
or: $\overline{S}$ = V_{IH},
or: $\overline{W}$ = V_{IL}

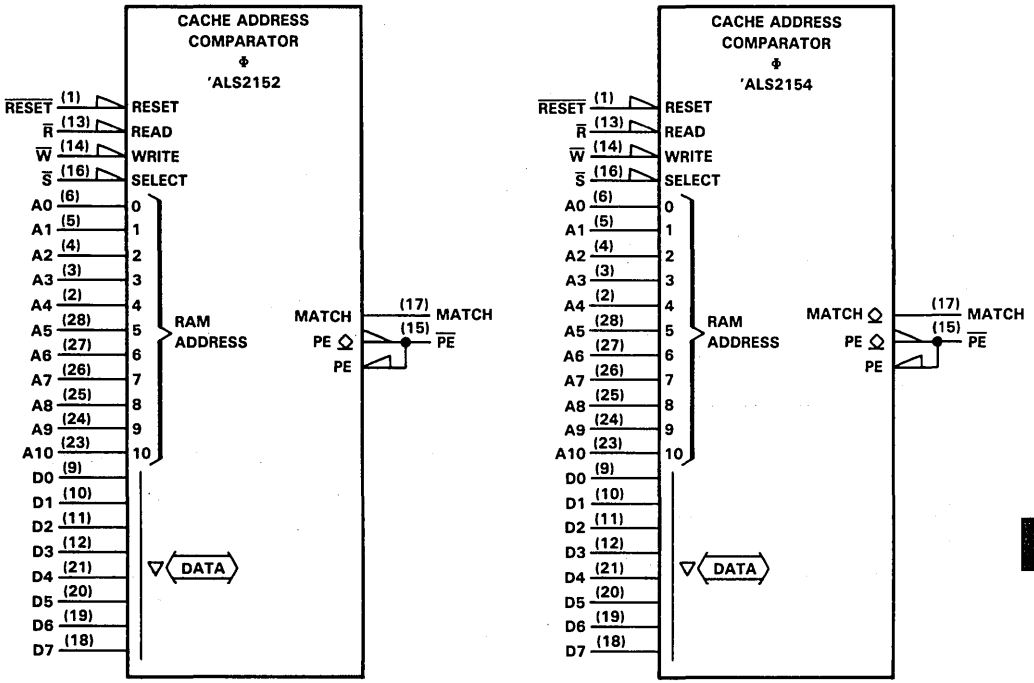
MATCH = V_{OL} if: [A0-A10] ≠ D0-D7 + parity,
with $\overline{RESET}$ = V_{IH},
$\overline{S}$ = V_{IL}, and $\overline{W}$ = V_{IH}

FUNCTION TABLE

INPUTS				OUTPUTS		I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{RESET}$	MATCH	$\overline{PE}$	D0-D7	
H	L	L	H	L	H	Output	Read
H	H	L	H	L	L	Input	Parity error
				L	H		Not equal
				H	L		Undefined error
				H	H		Equal
L	X	L	H	H	IN	Input	Write
X	X	H	H	H	H	Hi-Z	Device disabled
X	X	X	L	H	†	†	Memory reset

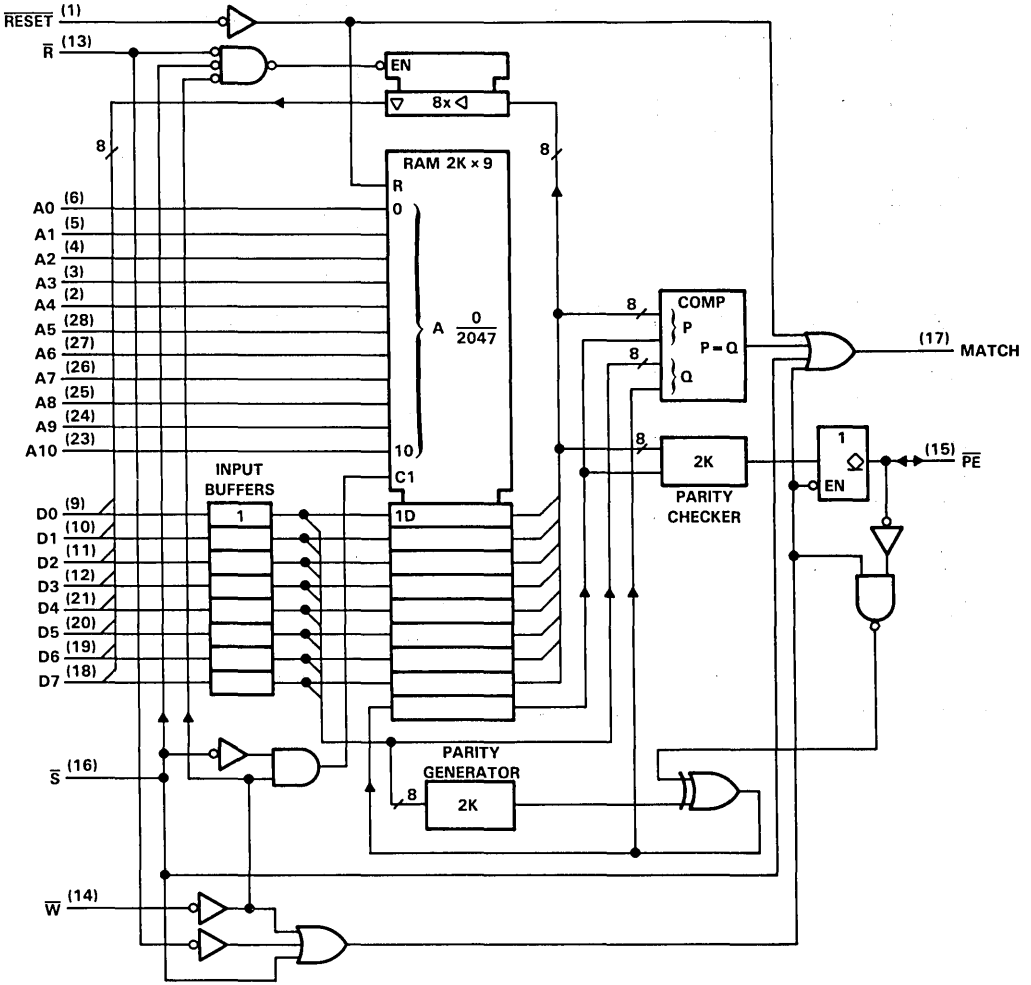
†The state of these pins is dependent on inputs $\overline{W}$, $\overline{R}$, and $\overline{S}$.

logic symbol†



†These symbols are in accordance with ANSI/IEEE Std 91-1984.

functional block diagram (positive logic)



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PIN NAME	PIN NO.	DESCRIPTION
A0	6	Address inputs. Addresses 1 of 2048 random access memory locations. Must be stable for the duration of the write cycle.
A1	5	
A2	4	
A3	3	
A4	2	
A5	28	
A6	27	
A7	26	
A8	25	
A9	24	
A10	23	
D0	9	Data inputs/outputs. D0-D7 are data inputs during the compare and write modes. D0-D7 are data outputs during the read mode.
D1	10	
D2	11	
D3	12	
D4	21	
D5	20	
D6	19	
D7	18	
GND	7,8	Ground
MATCH	17	When MATCH output is at V_{OH} during a compare cycle, D0-D7 plus generated parity equals the contents of the 9-bit memory location addressed by A0-A10. MATCH is also driven high during deselect, reset, and read. Since the 'ACT2154 features an open-drain MATCH output, an external pull-up resistor of 220 Ω minimum is required.
$\overline{PE}$	15	Parity error input/output. During compare cycles, $\overline{PE}$ at V_{OL} indicates a parity error in the stored data. During write cycles, $\overline{PE}$ can force a parity error into the 9th-bit location specified by A0-A10 when $\overline{PE}$ is taken to V_{IL}. $\overline{PE}$ is an open-drain output so an external pull-up resistor of 220 Ω minimum is required.
$\overline{R}$	13	Read input. When $\overline{R}$ and $\overline{S}$ are at V_{IL} and $\overline{W}$ is at V_{IH}, addressed data is output to the D0-D7 pins and the MATCH and $\overline{PE}$ outputs are forced high.
$\overline{RESET}$	1	Reset input. Asynchronously clears entire RAM array to zero and forces MATCH high when $\overline{RESET}$ is at V_{IL}.
$\overline{S}$	16	Chip select input. Enables device when $\overline{S}$ is at V_{IL}. Deselects device and forces MATCH and $\overline{PE}$ high when $\overline{S}$ is at V_{IH}.
V_{CC}	22	Supply voltage
$\overline{W}$	14	Write control input. Writes D0-D7 and generated parity into RAM and forces MATCH high when $\overline{W}$ and $\overline{S}$ are at V_{IL}. Places selected device in compare mode when $\overline{W}$ and $\overline{R}$ are at V_{IH}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −1.5 to 7 V
Input voltage, any input . . . . . −1.5 to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage, write or compare cycles		2.2		V_{CC}+0.5	V
V_{IH}	High-level input voltage, read cycle		2.6		V_{CC}+0.5	
V_{IL}	Low-level input voltage (See Note 2)		−0.5		0.8	V
V_{OH}	High-level output voltage, MATCH ('ACT2154) and $\overline{PE}$ outputs only				5.5	V
I_{OH}	High-level output current, MATCH ('ACT2152) and D0-D7				−8	mA
I_{OL}	Low-level output current	MATCH — 'ACT2152			8	mA
		MATCH — 'ACT2154			24	mA
		$\overline{PE}$			24	mA
		D0-D7			8	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, in which the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN74ACT2152-25 SN74ACT2154-25			SN74ACT2152-35 SN74ACT2154-35			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{OH}	High-level output current	MATCH ('ACT2154) and $\overline{PE}$	V_{OH} = 5.5 V, V_{CC} = 5.5 V			5			5	μA
V_{OH}	High-level output voltage	MATCH ('ACT2152) and D0-D7	I_{OH} = −8 mA, V_{CC} = 4.5 V	3.7			3.7			V
V_{OL}	Low-level output voltage	MATCH - 'ACT2154	I_{OL} = 24 mA, V_{CC} = 4.5 V			0.4			0.4	V
		MATCH - 'ACT2152	I_{OL} = 8 mA, V_{CC} = 4.5 V			0.4			0.4	
		$\overline{PE}$	I_{OL} = 24 mA, V_{CC} = 4.5 V			0.4			0.4	
		D0-D7	I_{OL} = 8 mA, V_{CC} = 4.5 V			0.4			0.4	
I_I	Input current		V_I = 0−V_{CC}, V_{CC} = 5.5 V			±1			±1	μA
I_{OZ}	Off-state output current		V_O = 0−V_{CC}, V_{CC} = 5.5 V, $\overline{S}$ at V_{IH}			±5			±5	μA
I_{OS}‡	Short-circuit output current	MATCH ('ACT2152) and D0-D7	V_O = 0, V_{CC} = 5.5 V	50		150	50		150	mA
I_{CC1}	Supply current (operative)		$\overline{RESET}$ at 3 V, V_{CC} = 5.5 V, $\overline{S}$ at 0 V		85	125		85	125	mA
I_{CC2}	Supply current (reset)		$\overline{RESET}$ at 0 V, V_{CC} = 5.5 V, $\overline{S}$ at 0 V		5	25		5	25	mA
I_{CC3}	Supply current (deselected)		$\overline{RESET}$ at 3 V, V_{CC} = 5.5 V, $\overline{S}$ at 3 V		75	105		75	105	mA
C_i	Input capacitance		f = 1 MHz			5			5	pF
C_o	Output capacitance		f = 1 MHz			6			6	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), see Figures 1, 2, and 3

compare cycle

PARAMETER		SN74ACT2152-25 SN74ACT2154-25			SN74ACT2152-35 SN74ACT2154-35			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A-M)}$	Access time from address to MATCH		19	25		20	35	ns
$t_{a(A-P)}$	Access time from address to $\overline{PE}$ high or low		21	28		27	38	ns
$t_{a(S-M)}$	Access time from $\overline{S}$ to MATCH		12	15		13	18	ns
$t_{p(D-M)}$	Propagation time, data inputs to MATCH		11	16		12	18	ns
$t_{p(RST-MH)}$	Propagation time, $\overline{RESET}$ low to MATCH high		12	18		13	20	ns
$t_{p(S-MH)}$	Propagation time, $\overline{S}$ high to MATCH high		6	12		8	15	ns
$t_{p(W-MH)}$	Propagation time, $\overline{W}$ low to MATCH high		9	14		9	15	ns
$t_{p(W-PH)}$	Propagation time, $\overline{W}$ low to $\overline{PE}$ high		7	14		8	18	ns
$t_{v(A-M)}$	MATCH valid time after change of address	4			4			ns
$t_{v(D-M)}$	MATCH valid time after change of data	2			2			ns
$t_{v(S-M)}$	MATCH valid time (low) after $\overline{S}$ high	2			2			ns
$t_{v(A-P)}$	$\overline{PE}$ valid time after change of address	6			6			ns

read cycle

PARAMETER			SN74ACT2152-25 SN74ACT2154-25			SN74ACT2152-35 SN74ACT2154-35			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A-D)}$	Read Access time from address to D0-D7			25	30		26	35	ns
$t_{en(S-D)}$	Enable time, $\overline{S}$ low to D0-D7			12	20		14	20	ns
$t_{en(R-D)}$	Enable time, $\overline{R}$ low to valid D0-D7 output			16	20		18	20	ns
$t_{p(R-MH)}$	Propagation time, $\overline{R}$ low to MATCH high			7	12		8	15	ns
$t_{p(R-PH)}$	Propagation time, $\overline{R}$ low to $\overline{PE}$ high			7	15		8	18	ns
t_{dis}	D0-D7 output disable time from high or low level	From $\overline{R}$, $\overline{S}$, $\overline{W}$		15	20		16	20	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		SN74ACT2152-25 SN74ACT2154-25			SN74ACT2152-35 SN74ACT2154-35			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{w(RSTL)}$	Pulse duration, $\overline{RESET}$ low	30			35			ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low, without writing $\overline{PE}$	15			20			ns
$t_{w(WL)PE}$	Pulse duration, $\overline{W}$ low, writing $\overline{PE}$ (see Note 3)	15			20			ns
$t_{su(A)}$	Address setup time before $\overline{W}$ low	0			0			ns
$t_{su(D)}$	Data setup time before $\overline{W}$ high	10			15			ns
$t_{su(P)}$	$\overline{PE}$ setup time before $\overline{W}$ high (see Note 3)	10			15			ns
$t_{su(S)}$	Chip select setup time before $\overline{W}$ high	10			15			ns
$t_{su(RST)}$	$\overline{RESET}$ inactive setup time before $\overline{W}$ high	15			20			ns
$t_{h(A)}$	Address hold time after $\overline{W}$ high	0			0			ns
$t_{h(WH-D)}$	Data hold time after $\overline{W}$ high	5			5			ns
$t_{h(WL-D)}$	Data hold time after $\overline{W}$ low with MATCH high, (see Note 4)	10			10			ns
$t_{h(P)}$	$\overline{PE}$ hold time after $\overline{W}$ high	5			5			ns
$t_{h(S)}$	Chip select hold time after $\overline{W}$ high	0			0			ns
t_{AVWH}	Address valid to write enable high	15			20			ns

NOTES: 3. Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle timing when writing a parity error.
4. $t_{h(WL-D)}$ guarantees that when $\overline{W}$ is taken low during a compare cycle with MATCH high, match will remain high without a glitch low. (As shown in the function table, $\overline{W}$ low forces MATCH high). $t_{h(WL-D)}$ is guaranteed indirectly by $t_{v(D-M)}$ and $t_{p(W-MH)}$.

PARAMETER MEASUREMENT INFORMATION

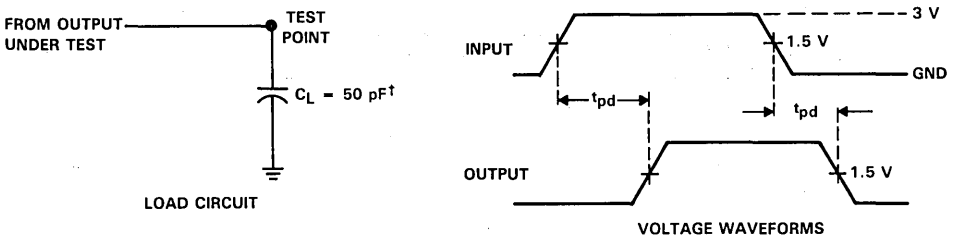


FIGURE 1. TACT2152 MATCH OUTPUT

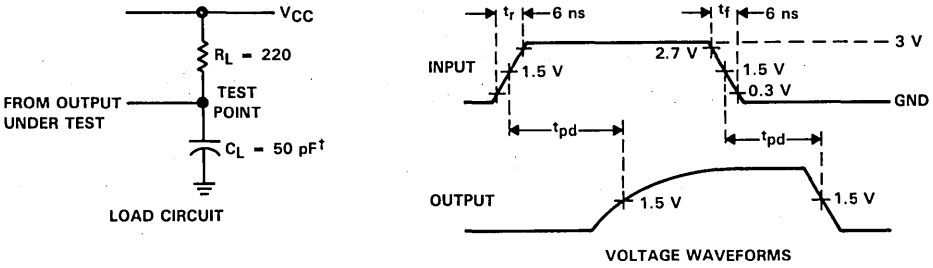


FIGURE 2. OPEN-DRAIN MATCH AND $\overline{PE}$ OUTPUTS

PARAMETER		R_L	C_L†	S1	S2
t_{en}	t_{PZH}	640 Ω	50 pF	OPEN	CLOSED
	t_{PZL}			CLOSED	OPEN
t_{dis}	t_{PHZ}	640 Ω	50 pF	OPEN	CLOSED
	t_{PLZ}			CLOSED	OPEN
t_{pd} or t_t		—	50 pF	OPEN	OPEN

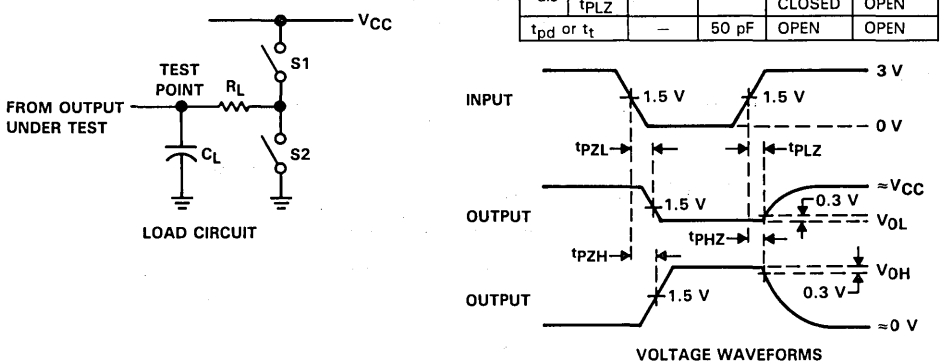
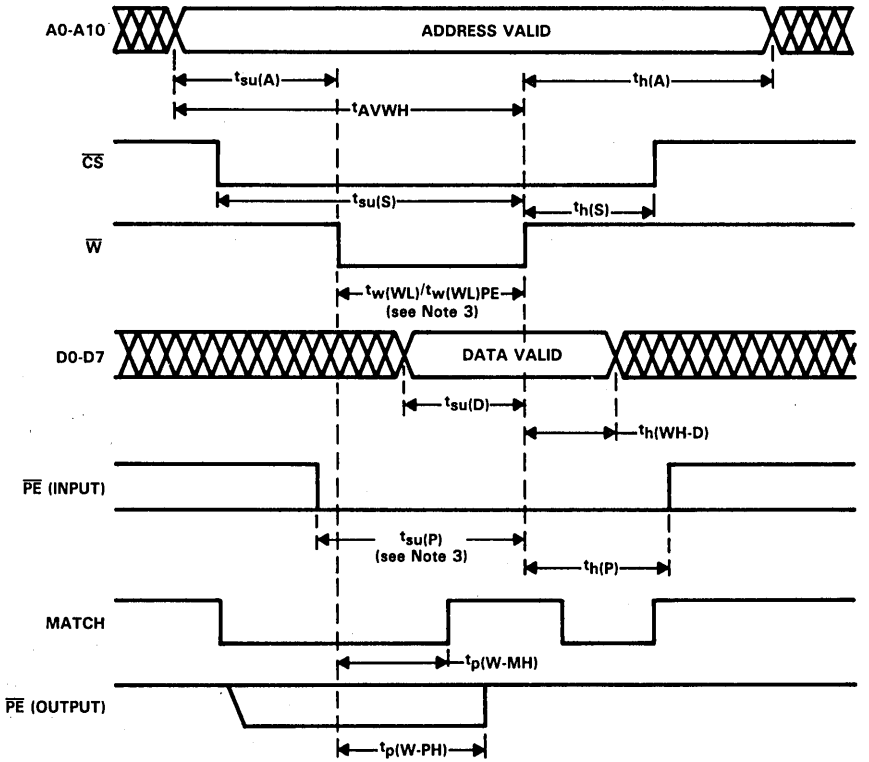


FIGURE 3. 3-STATE DATA OUTPUTS

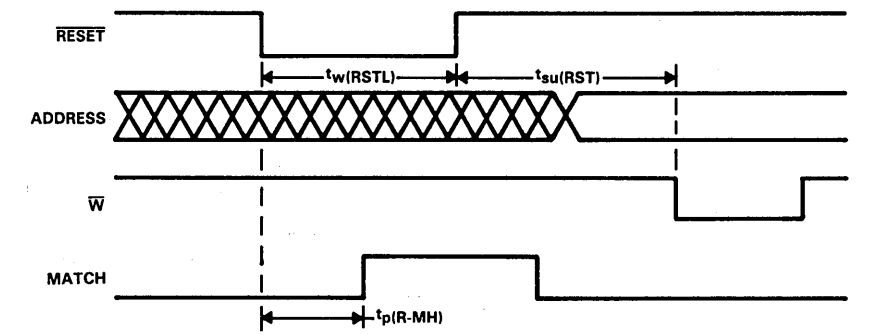
†C_L includes probe and test fixture capacitance.

PARAMETER MEASUREMENT INFORMATION

write cycle timing



reset cycle timing



NOTE 3: Parameters $t_{w(WL)PE}$ and $t_{su(P)}$ apply only during the write cycle when writing a parity error.

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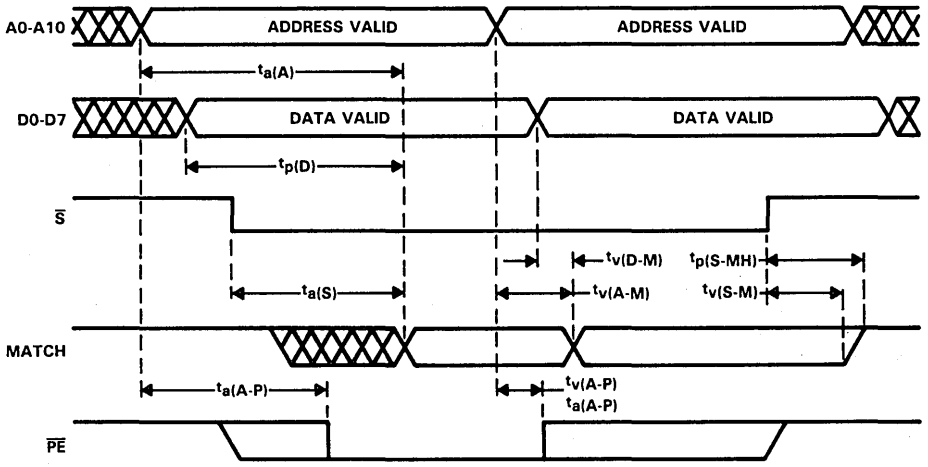
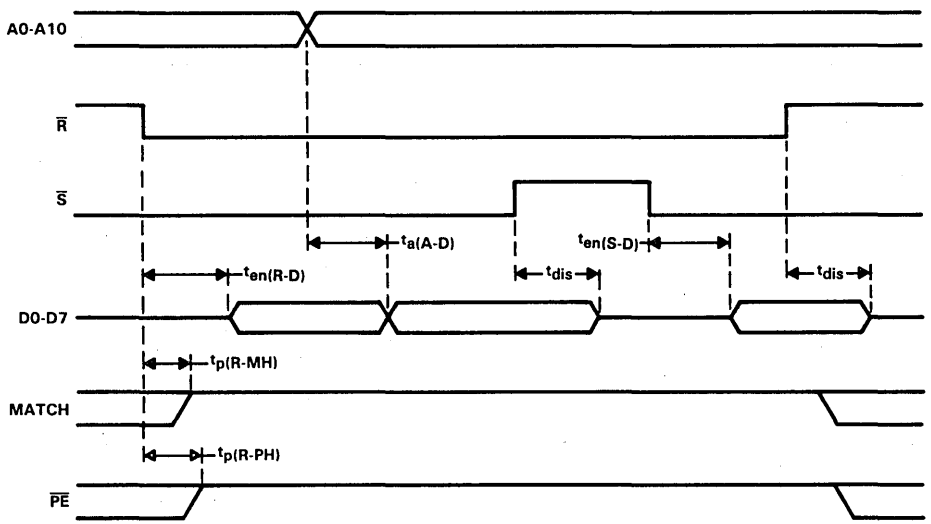
PARAMETER MEASUREMENT INFORMATION

compare cycle timing



read cycle timing



TYPICAL APPLICATION INFORMATION

cascading the 'ACT2152 and 'ACT2154

The 'ACT2152 and 'ACT2154 are easily cascaded in width and depth. Wider addresses can be compared by driving the A0-A10 inputs of each device with the same index and applying the additional address bits to the D0-D7 inputs. The select ($\overline{S}$) input allows these devices to be cascaded in depth. When a device is deselected, the MATCH output is driven high. It should be noted that a decoder can be used to drive the select inputs since the propagation delay from select to match is much faster than from address to match. MATCH on the 'ACT2154 is an open-drain output for easy AND-tying. Figure 4 shows the 'ACT2154 cascaded.

cache coherency through bus watching

When cache designs are implemented, the problem of cache coherency is always a concern. One solution to this problem is to implement bus-watching using the 'ACT2152 or 'ACT2154. By storing the same tags in the bus-watcher RAM as are stored in the cache tag RAM, the bus-watcher will indicate a hit every time a cache address passes down the main address bus. If data is being modified in main memory, the index can be passed to the cache tag RAM for invalidation. Figure 5 shows a possible bus-watcher implementation.

application

Due to the high-performance switching characteristics of the 'ACT2152 and 'ACT2154, it is necessary that the address inputs not be allowed to float in the three-state condition. Proper termination techniques should be employed. It is recommended that the RC time constant associated with the address inputs (63.2% of rise time at A0-A10) not exceed 60 ns.

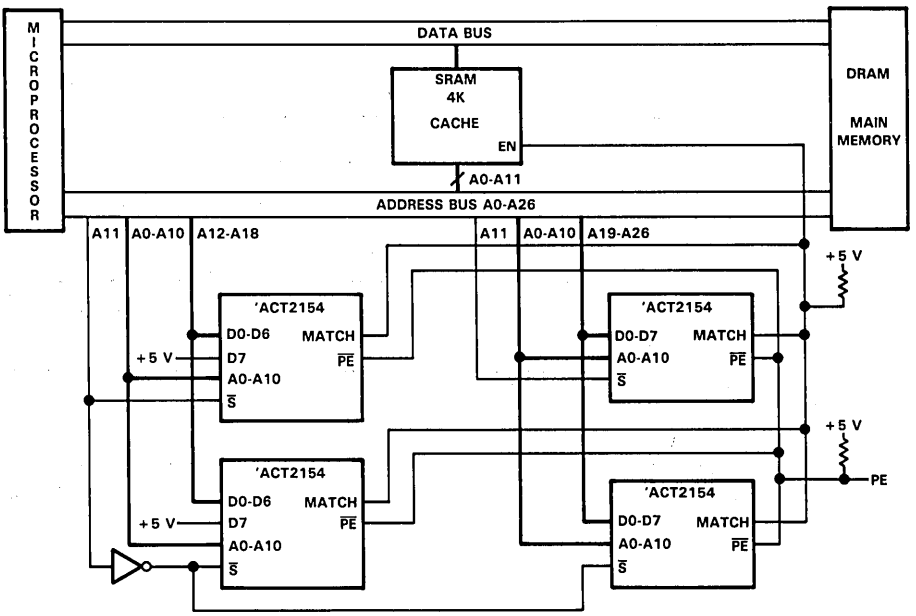


FIGURE 4. CASCADING THE 'ACT2154

TYPICAL APPLICATION INFORMATION

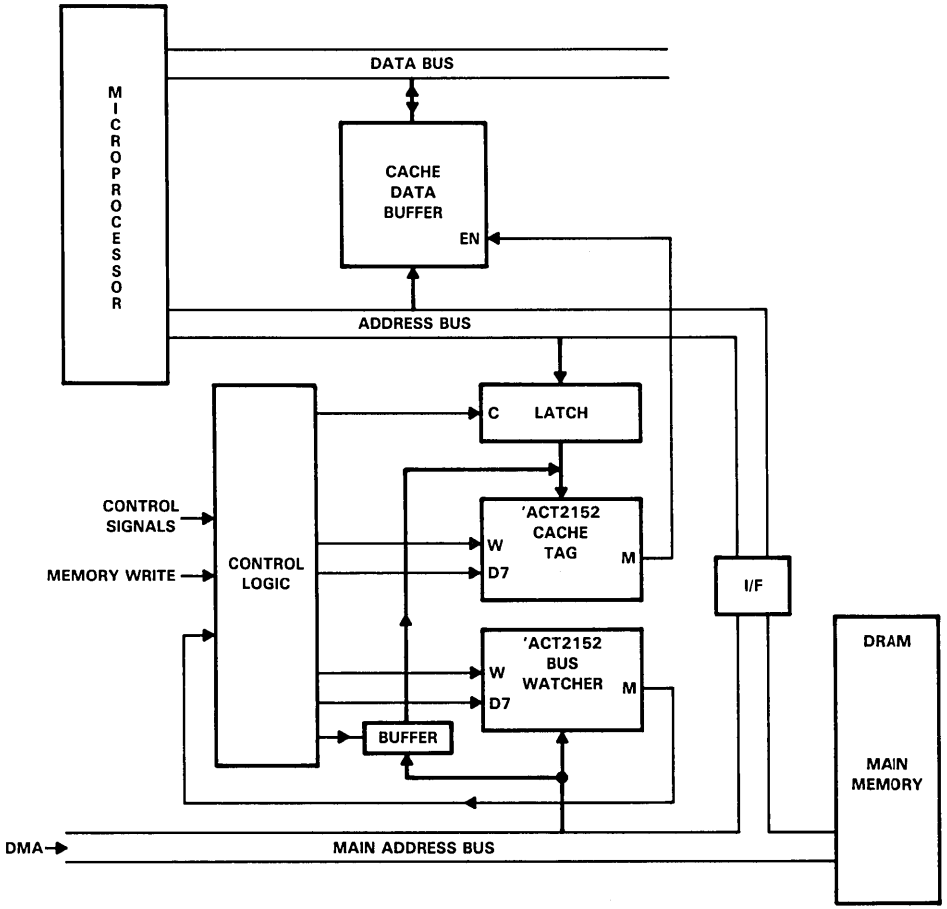
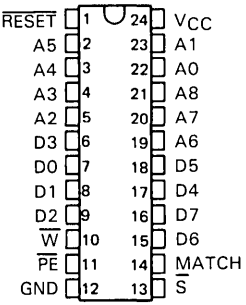


FIGURE 5. BUS WATCHING USING THE 'ACT2152

D2993, JANUARY 1987—REVISED SEPTEMBER 1987

- Address to MATCH Valid Time
  TACT2150-20 . . . 20 ns max
  TACT2150-30 . . . 30 ns max
- 300-Mil 24-Pin Ceramic Side-Brazed or Plastic Dual-In-Line or Small Outline Packages
- 53 mA Typical Supply Current
- On-Chip Parity Generation and Checking
- Parity Error Output/Force Parity Error Input
- On-Chip Address/Data Comparator
- Asynchronous, Single-Cycle Reset
- Easily Expandable
- Fully Static
- Reliable Advanced CMOS Technology
- Fully TTL Compatible

DW, JD, OR NT PACKAGE
(TOP VIEW)



description

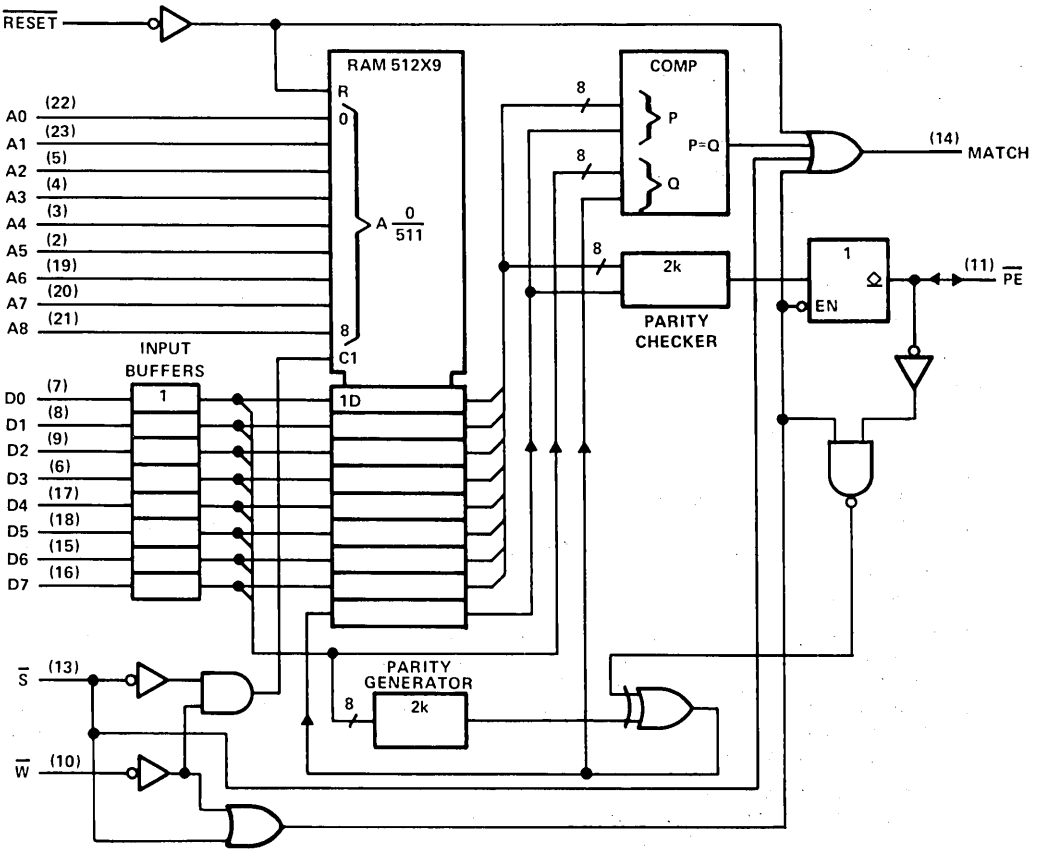
This 8-bit-slice cache address comparator consists of a high-speed 512 × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. It is fabricated using Advanced CMOS technology for high-speed, low-power interface with bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by the high level on the MATCH output. A low-level output from $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 512 × 9 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high for every addressed memory location after reset indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit needs to be tied high regardless of the address width.

The TACT2150 operates from a single 5 V supply and is offered in a 24-pin 300-mil ceramic side-brazed or plastic dual-in-line packages and plastic "Small Outline" packages. The device is fully TTL compatible and is characterized for operation from 0°C to 70°C.

functional block diagram (positive logic)



MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A8] = D0-D7 + parity,
or: $\overline{RESET} = V_{IL}$,
or: $\overline{S} = V_{IH}$,
or: $\overline{W} = V_{IL}$

MATCH = V_{OL} if: [A0-A8] ≠ D0-D7 + parity,
with $\overline{RESET} = V_{IH}$,
$\overline{S} = V_{IL}$, and $\overline{W} = V_{IH}$

FUNCTION TABLE

OUTPUT		FUNCTION
MATCH	$\overline{PE}$	DESCRIPTION
L	L	Parity Error
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

Where $\overline{S} = V_{IL}$, $\overline{W} = V_{IH}$, $\overline{RESET} = V_{IH}$

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PIN FUNCTIONAL DESCRIPTION

PIN NAME	PIN NO.	DESCRIPTION
A0	22	Address inputs. Address 1 of 512-by-9-bit random-access memory locations. Must be stable for the duration of the write cycle.
A1	23	
A2	5	
A3	4	
A4	3	
A5	2	
A6	19	
A7	20	
A8	21	
D0	7	Data inputs. Compared with memory location addressed by A0-A8 when $\overline{W}$ is at V_{IH} and $\overline{S}$ is at V_{IL}. Provide input data to RAM when $\overline{W}$ is at V_{IL} and $\overline{S}$ is at V_{IL}.
D1	8	
D2	9	
D3	6	
D4	17	
D5	18	
D6	15	
D7	16	
GND	12	Ground
MATCH	14	When MATCH output is at V_{OH} during a compare cycle, D0 through D7 plus parity equal the contents of the 9-bit memory location addressed by A0 through A8.
$\overline{PE}$	11	Parity error input/output. During write cycles, $\overline{PE}$ can force a parity error into the 9-bit location specified by A0 through A8 when $\overline{PE}$ is at V_{IL}. For compare cycles, $\overline{PE}$ at V_{OL} indicates a parity error in the stored data. $\overline{PE}$ is an open-drain output so an external pull-up resistor is required.
$\overline{RESET}$	1	$\overline{RESET}$ input. Asynchronously clears entire RAM array and forces MATCH high when $\overline{RESET}$ is at V_{IL} and $\overline{W}$ is at V_{IH}.
$\overline{S}$	13	Chip select input. Enables device when $\overline{S}$ is at V_{IL}. Deselects device and forces MATCH high when $\overline{S}$ is at V_{IH}.
V_{CC}	24	5-V supply voltage
$\overline{W}$	10	Write control input. Writes D0 through D7 and generated parity into RAM and forces MATCH high when $\overline{W}$ is at V_{IL} and $\overline{S}$ is at V_{IL}. Places selected device in compare mode if $\overline{W}$ is at V_{IH}.

application

Due to the high-performance switching characteristics of the TACT2150, it is necessary that the address inputs not be allowed to float. Proper termination techniques should be employed. It is recommended that the RC time constant associated with the address inputs (63.2% of rise time on A0-A8) not exceed 60 ns.

absolute maximum ratings over operating free-air temperature range (unless otherwise specified)

Supply voltage range, V_{CC} (see Note 1) . . . . . −1.5 to 7 V
Input voltage range, any input . . . . . −1.5 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage (See Note 2)		−0.5		0.8	V
V_{OH}	High-level output voltage	$\overline{PE}$			5.5	V
I_{OH}	High-level output current	MATCH			−8	mA
I_{OL}	Low-level output current	MATCH			8	mA
		$\overline{PE}$			16	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TACT2150-20			TACT2150-30			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{OH(M)}$	MATCH high-level output voltage	I_{OH} = −8 mA, V_{CC} = 4.5 V	2.4			2.4			V
		I_{OH} = −20 μA, V_{CC} = 4.5 V	3.5			3.5			
$V_{OL(M)}$	MATCH low-level output voltage	I_{OL} = 8 mA, V_{CC} = 4.5 V			0.4			0.4	V
$V_{OL(PE)}$	$\overline{PE}$ low-level output voltage	I_{OL} = 16 mA, V_{CC} = 4.5 V,			0.4			0.4	V
I_I	Input current	V_I = 0 V to 5.5 V			10			10	μA
I_{OS}	Short-circuit MATCH output current	V_O = GND, V_{CC} = 5.5 V			−150			−150	mA
I_{CC1}	Supply current (operative)	$\overline{RESET}$ = V_{IH}		53	95		53	95	mA
I_{CC2}	Supply current (reset)	$\overline{RESET}$ = V_L		2.75	6		2.75	6	mA
C_i	Input capacitance	f = 1 MHz			5			5	pF
C_o	Output capacitance	f = 1 MHz			6			6	pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TACT2150-20		TACT2150-30		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(A-M)}$	Access time from address to MATCH		20		30	ns
$t_{a(A-PL)}$	Access time from address to $\overline{PE}$ low		22		30	ns
$t_{a(A-PH)}$	Access time from address to $\overline{PE}$ high		30		35	ns
$t_{a(S-M)}$	Access time from $\overline{S}$ to MATCH		10		15	ns
$t_{p(D)}$	Propagation time, data inputs to MATCH		15		20	ns
$t_{p(R-MH)}$	Propagation time, $\overline{RESET}$ low to MATCH high		10		15	ns
$t_{p(S-MH)}$	Propagation time, $\overline{S}$ high to MATCH high		10		12	ns
$t_{p(W-MH)}$	Propagation time, $\overline{W}$ low to MATCH high		10		12	ns
$t_{p(W-PH)}$	Propagation time, $\overline{W}$ low to $\overline{PE}$ high		15		20	ns
$t_{v(A-M)}$	MATCH valid time after change of address	3		3		ns
$t_{v(A-P)}$	$\overline{PE}$ valid time after change of address	5		5		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TACT2150-20		TACT2150-30		UNIT
		MIN	MAX	MIN	MAX	
$t_{w(RL)}$	Pulse duration, $\overline{RESET}$ low	35		40		ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low, without writing $\overline{PE}$	20		25		ns
$t_{wPE(WL)}$	Pulse duration, $\overline{W}$ low, writing $\overline{PE}$ (see Note 3)	20		25		ns
$t_{su(A)}$	Address setup time before $\overline{W}$ low	0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ high	20		25		ns
$t_{su(P)}$	$\overline{PE}$ setup time before $\overline{W}$ high (see Note 3)	20		25		ns
$t_{su(S)}$	Chip select setup time before $\overline{W}$ high	20		25		ns
$t_{su(RH)}$	$\overline{RESET}$ inactive setup time before first tag cycle	0		0		ns
$t_{h(A)}$	Address hold time after $\overline{W}$ high	0		0		ns
$t_{h(D)}$	Data hold time after $\overline{W}$ high	0		0		ns
$t_{h(P)}$	$\overline{PE}$ hold time after $\overline{W}$ high	0		0		ns
$t_{h(S)}$	Chip select hold time after $\overline{W}$ high	0		0		ns
t_{AVWH}	Address valid to write enable high	20		25		ns

NOTE 3: Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle time when writing a parity error, $t_{cPE(W)}$.

PARAMETER MEASUREMENT INFORMATION

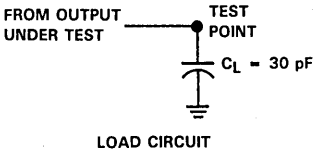

FIGURE 1. TOTEM-POLE OUTPUTS

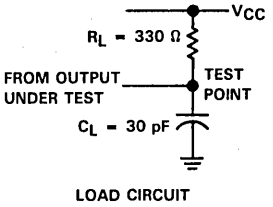

FIGURE 2. OPEN-DRAIN OUTPUTS

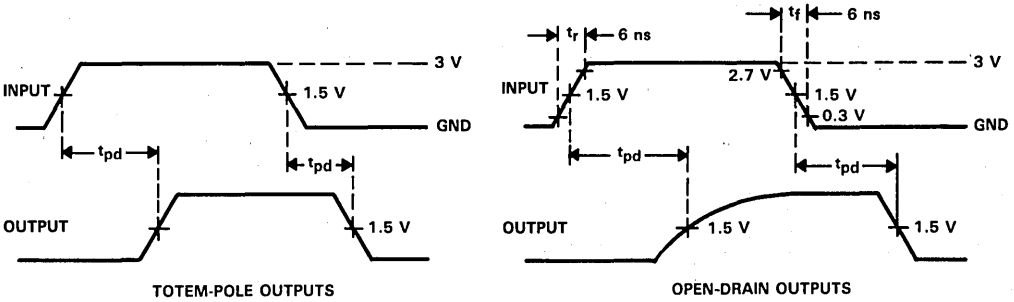

FIGURE 3. TIMING REFERENCE LEVELS

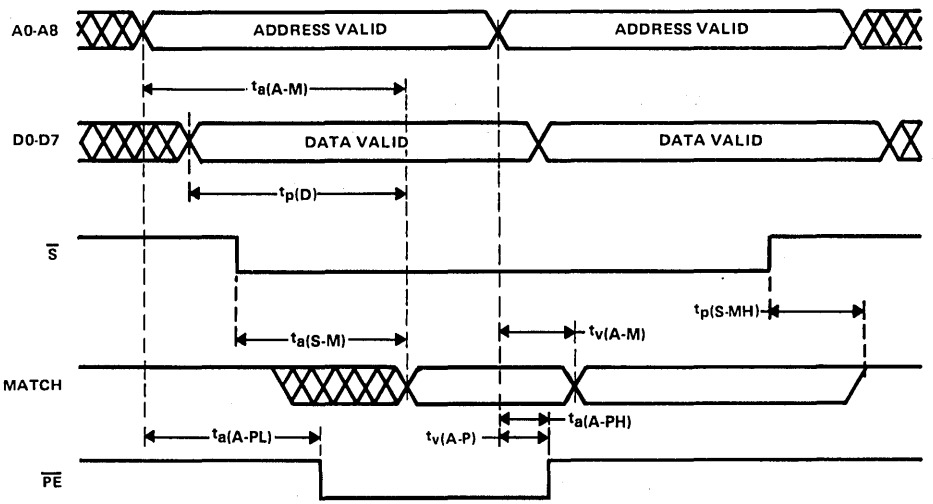

FIGURE 4. COMPARE CYCLE TIMING

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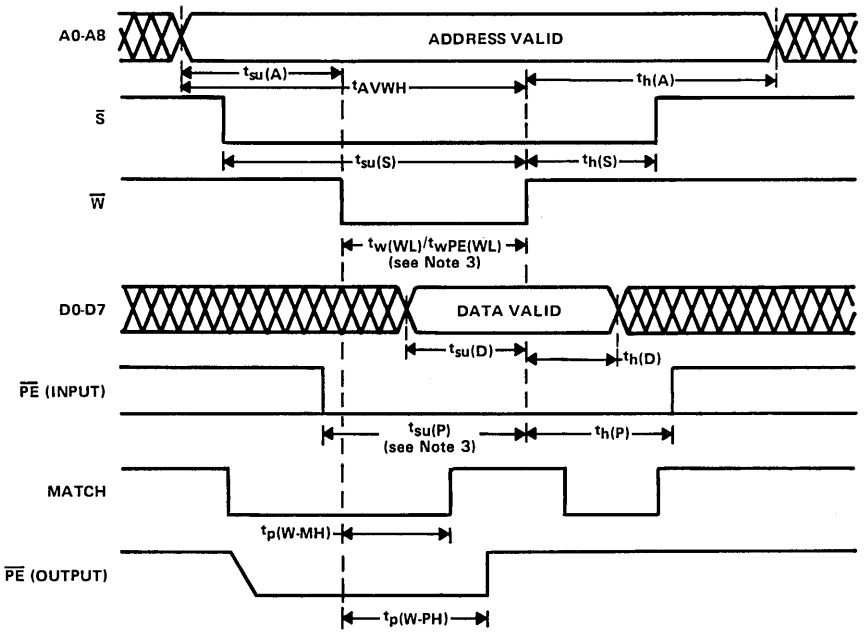
PARAMETER MEASUREMENT INFORMATION



NOTE 3: Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle time when writing a parity error, $t_{cPE(W)}$.

FIGURE 5. WRITE CYCLE TIMING

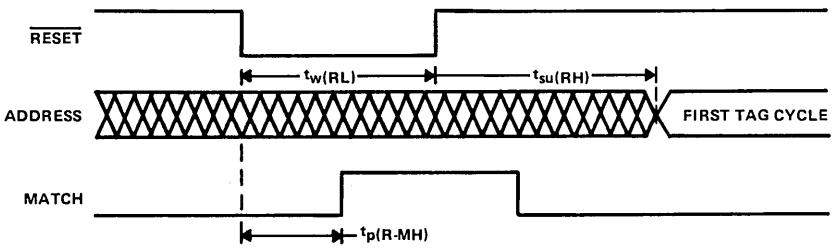


FIGURE 6. RESET CYCLE TIMING

D2900, JANUARY 1986 – REVISED MARCH 1988

- **Provides Control for 16K, 64K, and 256K Dynamic RAMs**
- **Highest-Order Two-Address Bits Select One of Four Banks of RAMs**
- **Supports Scrubbing Operations and Nibble-Mode Access**
- **Separate Output Enable for Multi-Channel Access to Memory**
- **48-Pin Dual-In-Line Package**

description

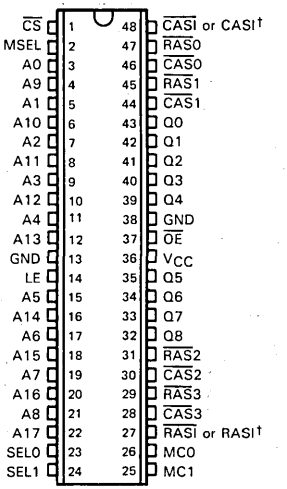
The 'ALS2967 and 'ALS2968 dynamic memory controllers (DMCs) are designed for use in today's high-performance memory systems. The DMC acts as the address controller between any processor and dynamic memory array.

Two versions are provided that help simplify interfacing to the system dynamic timing controller. The 'ALS2967 offers active-low Row Address Strobe Input ($\overline{RASI}$) and Column Address Strobe Input ($\overline{CASI}$), while the 'ALS2968 offers active-high Row Address Strobe Input (RASI) and Column Address Strobe Input (CASI) inputs.

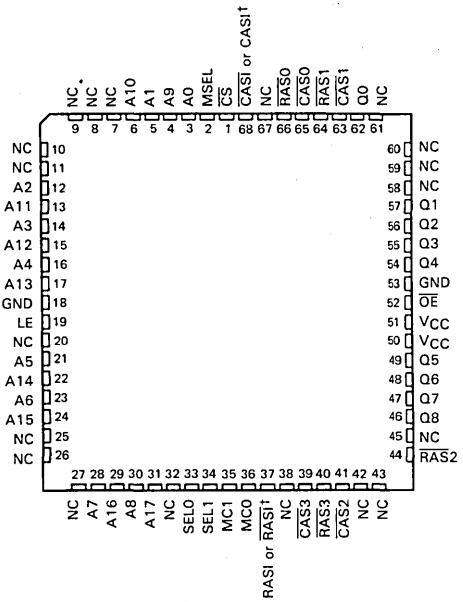
Using two 9-bit address latches, the DMC will hold the row and column addresses for any DRAM up to 256K. These latches and the two row/column refresh address counters feed into a 9-bit, 4-input MUX for output to the dynamic RAM address lines. A 2-bit bank select latch is provided to select one of the four $\overline{RAS}$ and $\overline{CAS}$ outputs. The two bits are normally obtained from the two highest-order address bits.

The 'ALS2967 and 'ALS2968 have two basic modes of operation, read/write and refresh. During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM, with the corresponding $\overline{RAS}$ and $\overline{CAS}$ signals activated to strobe the addresses into the RAM. In the refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the row counter is used. When memory scrubbing is being performed, both the row and column counters are used to perform read-modify-write cycles. In this mode all $\overline{RAS}$ outputs will be active (low) while only one $\overline{CAS}$ output is active at a time.

SN74ALS2967, SN74ALS2968 . . . JD OR N PACKAGE
(TOP VIEW)



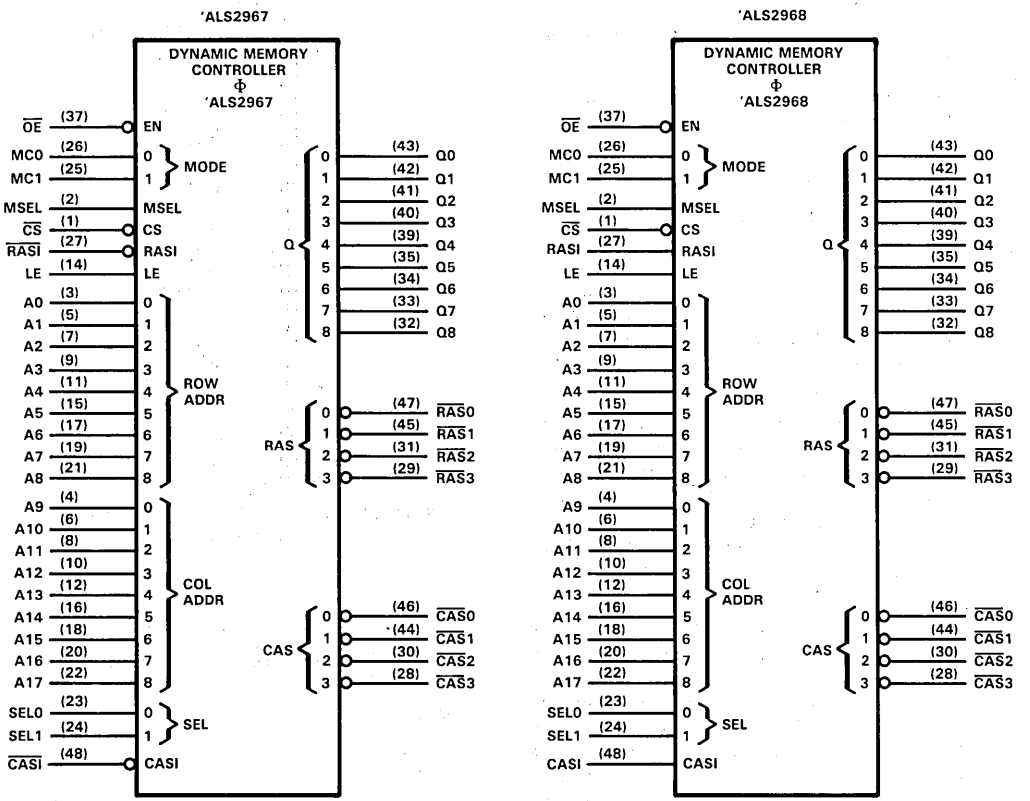
SN74ALS2967, SN74ALS2968 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection
† 'ALS2967 has active-low inputs $\overline{CASI}$ and $\overline{RASI}$; 'ALS2968 has active-high inputs CASI and RASI.

The SN74ALS2967 and SN74ALS2968 are characterized for operation from 0°C to 70°C.

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

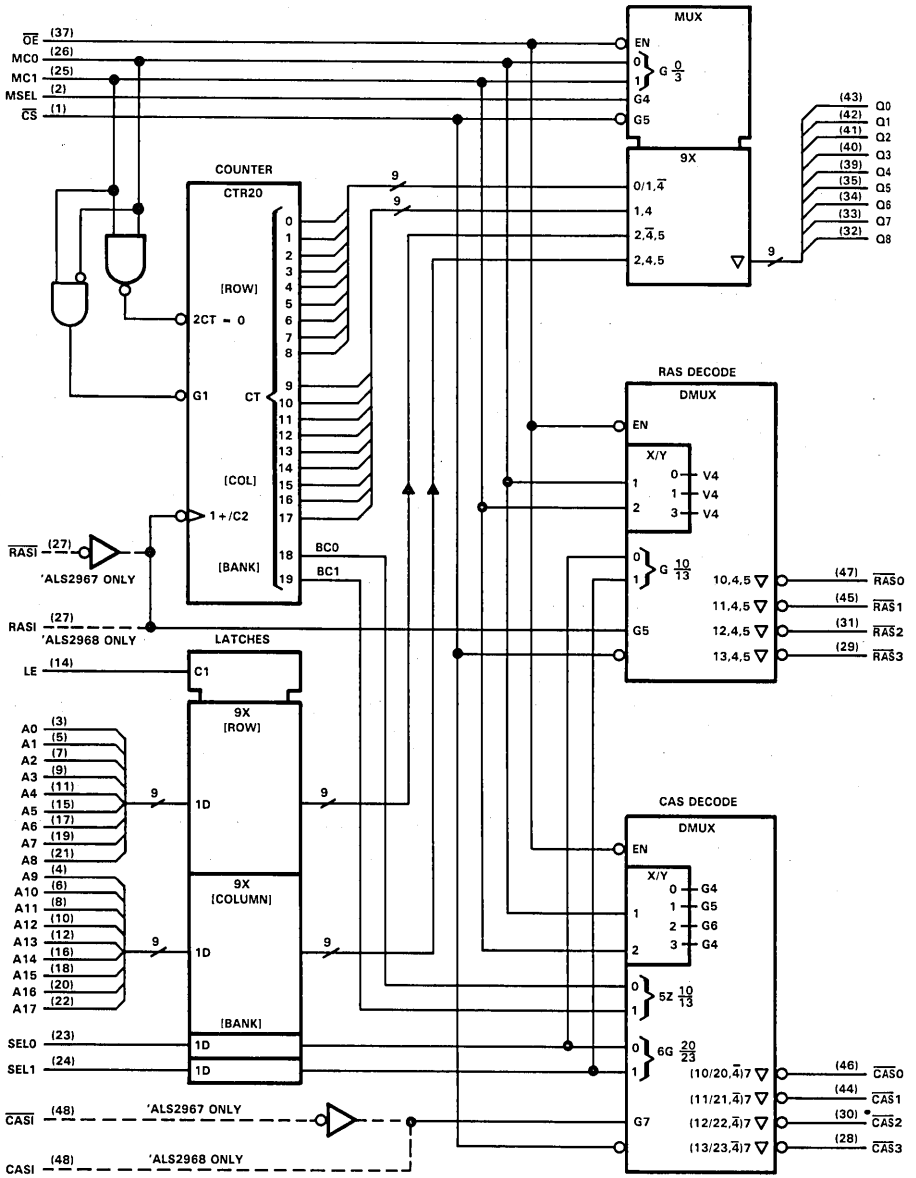


TABLE 1. PIN FUNCTION

PIN NAME	DESCRIPTION
A0-A17	Address Inputs. A0-A8 are latched in as the nine-bit row address for the DRAM. These inputs drive Q0-Q8 when the DMC is in the read/write mode and MSEL is low. A9-A17 are latched in as the column address, and will drive Q0-Q8 when MSEL is high and the DMC is in the read/write mode. The addresses are latched when the Latch Enable (LE) input signal is low.
SEL0, SEL1	Bank Select. These two inputs are normally the two highest-order address bits and are used in the read/write mode to select which bank of memory will be receiving the $\overline{RAS}$ and $\overline{CAS}$ signals after $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968) and $\overline{CASI}$ ('ALS2967) or CASI ('ALS2968) go active.
LE	Latch Enable. This active-high input causes the row, column, and bank select latches to become transparent, allowing the latches to accept new input data. A low input on LE latches the input data.
MSEL	Multiplexer Select. This input determines whether the row or column address will be sent to the memory address inputs. When MSEL is high, the column address is selected, while the row address is selected when MSEL is low. The address may come from either the address latch or refresh address counter depending on MC0 and MC1 (see Mode Control Function Table).
$\overline{CS}$	Chip Select. This active-low input is used to enable the DMC. When $\overline{CS}$ is active, the DMC operates normally in all four modes. When $\overline{CS}$ goes high, the device will not enter the read/write mode. This allows other devices to access the same memory that the DMC is controlling.
$\overline{OE}$	Output Enable. This active-low input enables/disables the output signals. When $\overline{OE}$ is high, the outputs of the DMC enter the high-impedance state.
MC0-MC1	Mode Controls. These inputs determine in which of the four modes the DMC operates. The description of each of the four operating modes is given in Table 2.
Q0-Q8	Address Outputs. These address outputs feed the DRAM address inputs and provide drive for memory systems having capacitance of up to 500 picofarads.
$\overline{RASI}$ or RASI	Row Address Strobe Input. During the normal memory cycles, the decoded $\overline{RAS}$n output ($\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, or $\overline{RAS3}$) is forced low after receipt of an active Row Address Strobe Input signal. In either Refresh mode, all four $\overline{RAS}$ outputs will be low while the Row Address Strobe Input signal is active. The $\overline{RASI}$ on the 'ALS2967 is an active-low input while on the 'ALS2968, RASI is an active-high input. (For more details see timing diagrams).
$\overline{RAS0}$-$\overline{RAS3}$	Row Address Strobe. Each of the Row Address Strobe outputs provides a $\overline{RAS}$ signal to one of the four banks of dynamic memory. Each $\overline{RAS}$n output will go low when selected by SEL0 and SEL1 after $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968) goes active. All four go low in response to $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968) while in the refresh mode.
$\overline{CASI}$ or CASI	Column Address Strobe Input. This input going active causes the selected $\overline{CAS}$ output to be forced low. The $\overline{CASI}$ input on the 'ALS2967 is active low input while on the 'ALS2968, CASI is active high input. (For more details see timing diagrams.)
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe. During normal Read/Write cycles the two selected bits (SEL0, SEL1) determine which $\overline{CAS}$ output will go active following $\overline{CASI}$ ('ALS2967) or CASI ('ALS2968) going active. When memory scrubbing is being performed, only the $\overline{CAS}$n signal selected will be active. For non-scrubbing cycles, all four $\overline{CAS}$ outputs will remain high.

TABLE 2. MODE-CONTROL FUNCTION TABLE

MC1	MC0	OPERATING MODE
L	L	Refresh Mode without Scrubbing. Refresh cycles are performed with only the row counter being used to generate the addresses. In this mode, all four $\overline{RAS}$ outputs are active while the four $\overline{CAS}$ outputs remain high.
L	H	Refresh with Scrubbing/Initialize. During this mode, refresh cycles are done with both the row and column counters generating the addresses. MSEL is used to select either the row or the column counter. All four $\overline{RAS}$ outputs go low in response to $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968), while only one $\overline{CAS}$n output goes low in response to $\overline{CASI}$ ('ALS2967) or CASI ('ALS2968). The bank counter keeps track of which $\overline{CAS}$ output goes active. This mode can also be used during system power-up so that the memory can be written with a known data pattern.
H	L	Read/Write. This mode is used to perform read/write cycles. Both the Row and Column addresses are multiplexed to the address output lines using MSEL. SEL0 and SEL1 are decoded to determine which $\overline{RAS}$n and $\overline{CAS}$n outputs will be active. The refresh counter is disabled while in this mode.
H	H	Clear Refresh Counters. This mode clears the three refresh counters (row, column, and bank) on the inactive transition of $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968), putting them at start of the refresh sequence (see timing diagrams for more detail). In this mode, all four $\overline{RAS}$ outputs are driven low after the active edge of $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968) so that DRAM wake-up cycles may also be performed.

TABLE 3. ADDRESS OUTPUT FUNCTIONS

MODE	INPUTS				OUTPUTS Q0-Q8
	MC1	MC0	MSEL	$\overline{CS}$	
Refresh without scrubbing	L	L	X	X	Row counter address
Refresh with scrubbing	L	H	L	X	Row counter address
			H	X	Column counter address
Read/write	H	L	L	L	Row address†
			H	L	Column address†
			X	H	All L
Clear refresh counter‡	H	H	X	X	All L

TABLE 4. RAS OUTPUT FUNCTIONS

INPUTS							OUTPUTS			
'ALS2967 $\overline{RASI}$	'ALS2968 RASI	MC1	MC0	SEL1†	SEL0†	$\overline{CS}$	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{RAS2}$	$\overline{RAS3}$
L	H	L	L	X	X	X	L	L	L	L
L	H	L	H	X	X	X	L	L	L	L
L	H	H	L	L	L	L	L	H	H	H
				L	H	L	H	L	H	H
				H	L	L	H	H	L	H
				H	H	L	H	H	H	L
				X	X	H	H	H	H	H
L	H	H	H	X	X	X	L	L	L	L
H	L	X	X	X	X	X	H	H	H	H

TABLE 5. CAS OUTPUT FUNCTIONS

INPUTS									OUTPUTS			
'ALS2967 $\overline{CASI}$	'ALS2968 CASI	MC1	MC0	SEL1†	SEL0†	INTERNAL BC1	INTERNAL BC0	$\overline{CS}$	$\overline{CAS0}$	$\overline{CAS1}$	$\overline{CAS2}$	$\overline{CAS3}$
L	H	L	L	X	X	X	X	X	H	H	H	H
L	H	L	H	X	X	L	L	X	L	H	H	H
						L	H	X	H	L	H	H
						H	L	X	H	H	L	H
						H	H	X	H	H	H	L
L	H	H	L	L	L	X	X	L	L	H	H	H
				L	H	X	X	L	H	L	H	H
				H	L	X	X	L	H	H	L	H
				H	H	X	X	L	H	H	H	L
				X	X	X	X	H	H	H	H	H
L	H	H	H	X	X	X	X	X	H	H	H	H
H	L	X	X	X	X	X	X	X	H	H	H	H

† If LE is low, outputs will be the levels entered when LE was last high. If LE is high, outputs will follow address inputs as selected by MSEL.
‡ For 'ALS2967, clearing occurs on the low-to-high transition of $\overline{RASI}$; for 'ALS2968, clearing occurs on the high-to-low transition of RASI.

read/write operation details

During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM controlled by the MSEL input. The corresponding $\overline{RAS}$n and $\overline{CAS}$n output signals strobe the addresses into memory. The block diagram in Figure 1 shows a typical system interface for a one-megaword dynamic memory. The DMC is used to control the four banks of 256K memory.

For systems where addresses and data are multiplexed onto a single bus, the DMC uses latches, (row, column, and bank) to hold the address information. Figure 5 shows a typical timing diagram using the input latches. The twenty input latches are transparent when latch enable (LE) is high, and latch the input data whenever LE is taken low. For systems in which the processor has separate address and data buses, LE may be permanently high (see timing diagram in Figure 4).

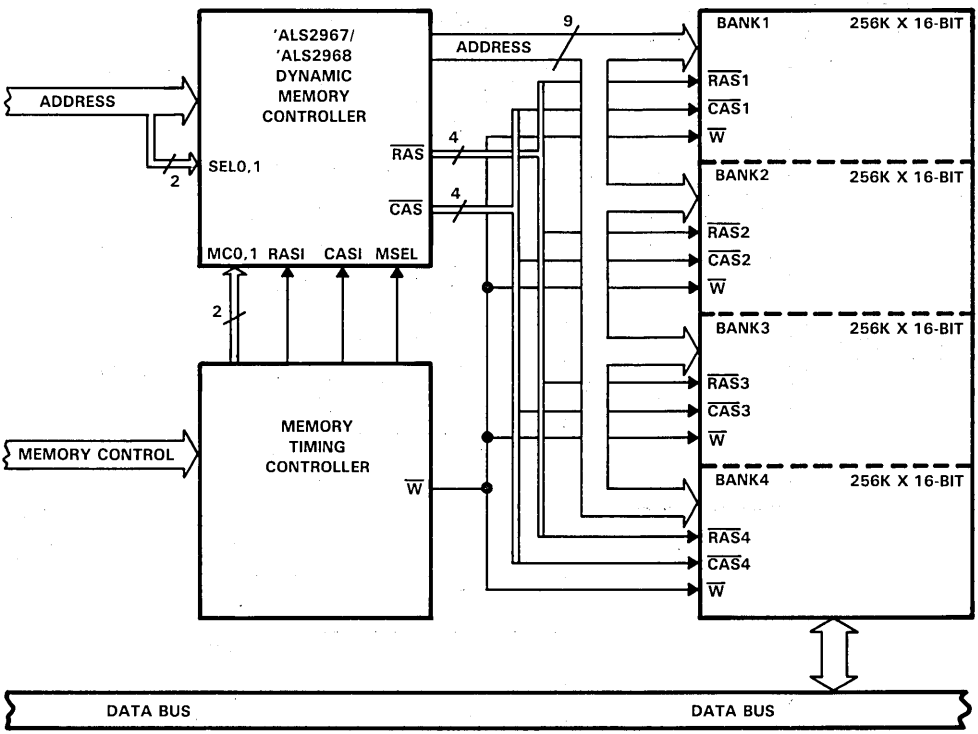


FIGURE 1. 1-MEGAWORD X 16-BIT DYNAMIC MEMORY

read/write operations (continued)

The DMC is designed with heavy-duty outputs that are capable of driving four banks of 16-bit words, including six checkbits used for error detection and correction.

In addition to heavy-duty output drivers, the outputs are designed with balanced output impedances (25 Ω both high and low). This feature optimizes the drive low characteristics, based on safe undershoot, while providing symmetrical drive high characteristics. It also eliminates the external resistors required to pull the outputs up to the MOS V_{OH} level (V_{CC} – 1.5 V).

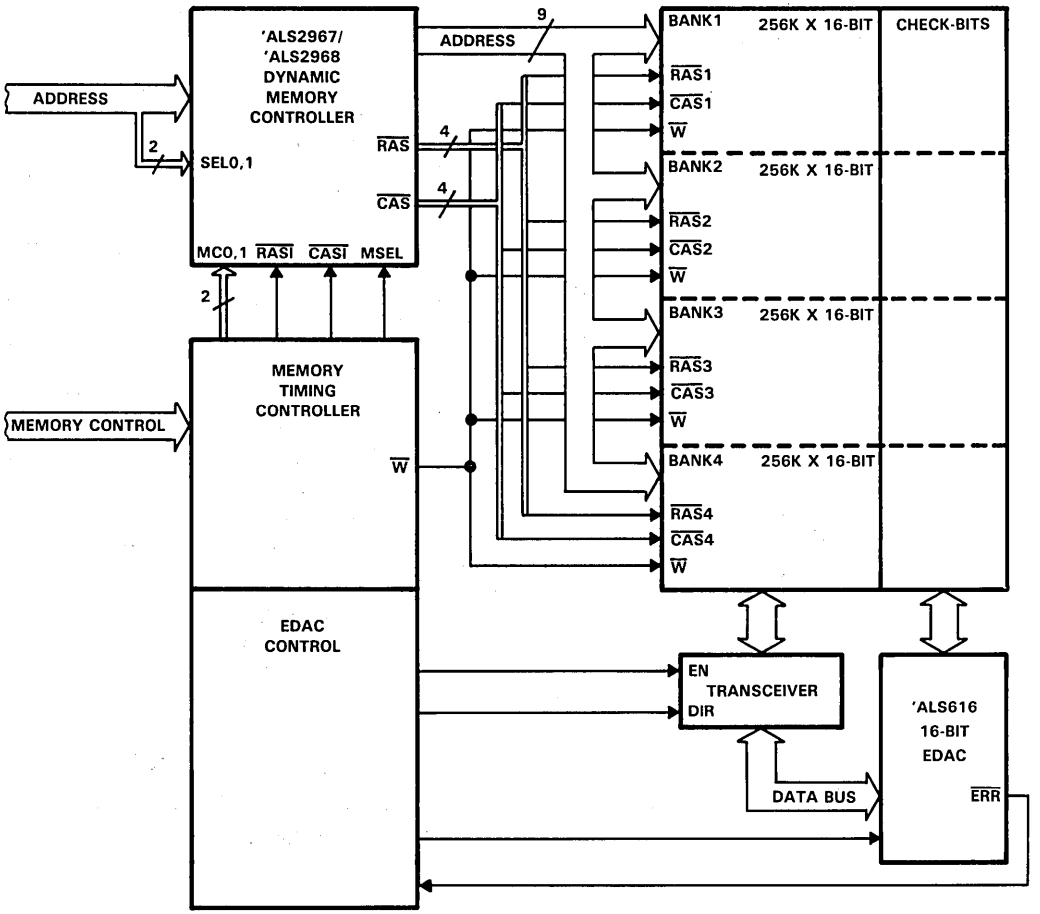


FIGURE 2. 1-MEGAWORD X 16-BIT DYNAMIC MEMORY WITH ERROR DETECTION AND CORRECTION

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memory expansion

With a 9-bit address path, the DMC can control up to one megaword when using 256K dynamic RAMs. If a larger memory size is desired, the DMC's chip select ($\overline{CS}$) makes it easy to expand the memory size by using additional DMCs. A four-megaword memory system is shown in Figure 3.

To maintain maximum performance in 32-bit applications, it is recommended that individual bus drivers be used for each bank.

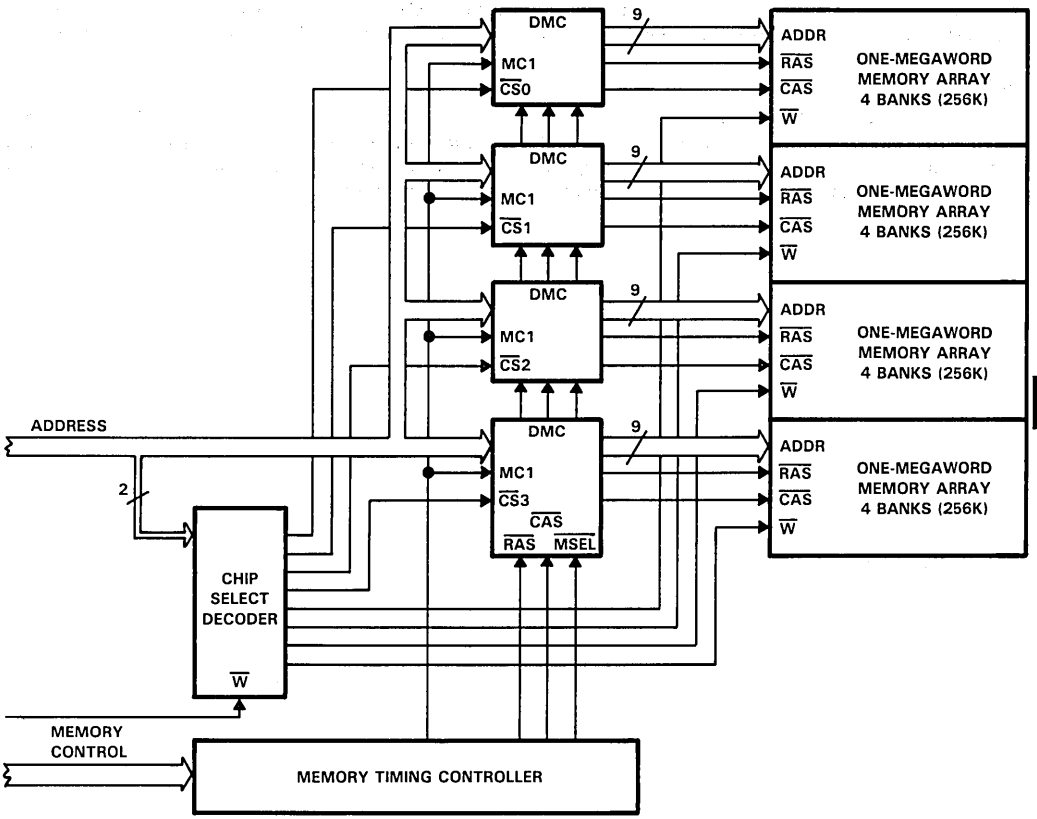

FIGURE 3. 4-MEGAWORD X 16-BIT DYNAMIC MEMORY

refresh operations

The two 9-bit counters in the 'ALS2967 and 'ALS2968 support 128-, 256-, and 512-line refresh operations. Transparent, burst, synchronous, or asynchronous refresh modes are all possible. The refresh counters are advanced on the low-to-high transition of $\overline{\text{RASI}}$ on the 'ALS2967, and on the high-to-low transition of RASI on the 'ALS2968. The refresh counters are reset to zero on the low-to-high transition of $\overline{\text{RASI}}$ on the 'ALS2967, and on the high-to-low transition of RASI on the 'ALS2968, if MC1 and MC0 are at a high logic level. See Figure 8 for additional timing details.

When performing refresh cycles without memory scrubbing (MC1 and MC0 both low), all four $\overline{\text{RAS}}$ outputs go low, while all $\overline{\text{CAS}}$ outputs are driven high. Typical timing for this mode of operation is shown in Figure 6.

decoupling

Due to the high switching speed and high drive capability of the 'ALS2967 and 'ALS2968, it is necessary to decouple the device for proper operation. Multilayer ceramic 0.1 μF to 1 μF capacitors are recommended for decoupling. It is important to mount the capacitors as close as possible to the power pins (V_{CC} and GND) to minimize lead inductance and noise. A ground plane is recommended.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2.6	mA
I_{OL}	Low-level output current				12	mA
t_w	Pulse duration	(23) $\overline{RASI}$ low or RASI high	15			ns
		(24) $\overline{RASI}$ high or RASI low	15			
		(25) LE high	20			
t_{su}	Setup time	(26) An before LE↓	5			ns
		(27) SELn before LE↓	5			
		(28) MC0 or MC1 before $\overline{RASI}$↑ or RASI↓	25			
		(29) SELn before $\overline{RASI}$↓ or RASI↑	15			
t_h	Hold time	(30) An after LE↓	5			ns
		(31) SELn after LE↓	5			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8	
I_{OL}‡	V_{CC} = 4.5 V,	V_O = 2 V	30			mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,			136	200	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and duration should not exceed 1 second.
§ The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, I_{OS}.

switching characteristics, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	$\overline{RASI}$ or RASI	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	9	18	25	ns
$t_{pd(2)}$	$\overline{RASI}$ or RASI	$\overline{RAS}$n		3	10	18	ns
$t_{pd(3)}$	$\overline{CASI}$ or CASI	$\overline{CAS}$n		3	9	17	ns
$t_{pd(4)}$	Any A	Any Q		3	9	18	ns
$t_{pd(5)}$	MSEL	Any Q		3	12	20	ns
$t_{pd(6)}$	LE↑	Any Q			13	25	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			13	25	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			13	24	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		7	13	24	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		3	10	21	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		3	9	19	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			13	23	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			9	20	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			9	19	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			10	20	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			11	18	ns
$t_{en(17)}$	$\overline{OE}$↓	Any Q			10	19	ns
$t_{en(18)}$	$\overline{OE}$↓	Any $\overline{RAS}$			11	19	ns
$t_{en(19)}$	$\overline{OE}$↓	Any $\overline{CAS}$			11	19	ns
$t_{dis(20)}$	$\overline{OE}$↑	Any Q			10	20	ns
$t_{dis(21)}$	$\overline{OE}$↑	Any $\overline{RAS}$			10	20	ns
$t_{dis(22)}$	$\overline{OE}$↑	Any $\overline{CAS}$			9	20	ns

switching characteristics, C_L = 150 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	$\overline{RASI}$ or RASI	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	12	20	27	ns
$t_{pd(2)}$	$\overline{RASI}$ or RASI	$\overline{RAS}$n		5	12	23	ns
$t_{pd(3)}$	$\overline{CASI}$ or CASI	$\overline{CAS}$n		4	12	22	ns
$t_{pd(4)}$	Any A	Any Q		5	12	20	ns
$t_{pd(5)}$	MSEL	Any Q		8	15	26	ns
$t_{pd(6)}$	LE↑	Any Q			15	27	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			15	28	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			16	27	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		7	14	28	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		5	12	25	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		4	11	23	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			14	27	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			11	22	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			12	22	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			13	23	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			13	22	ns

† See Figures 10, 11, 12, and 13 for test circuit and switching waveforms.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

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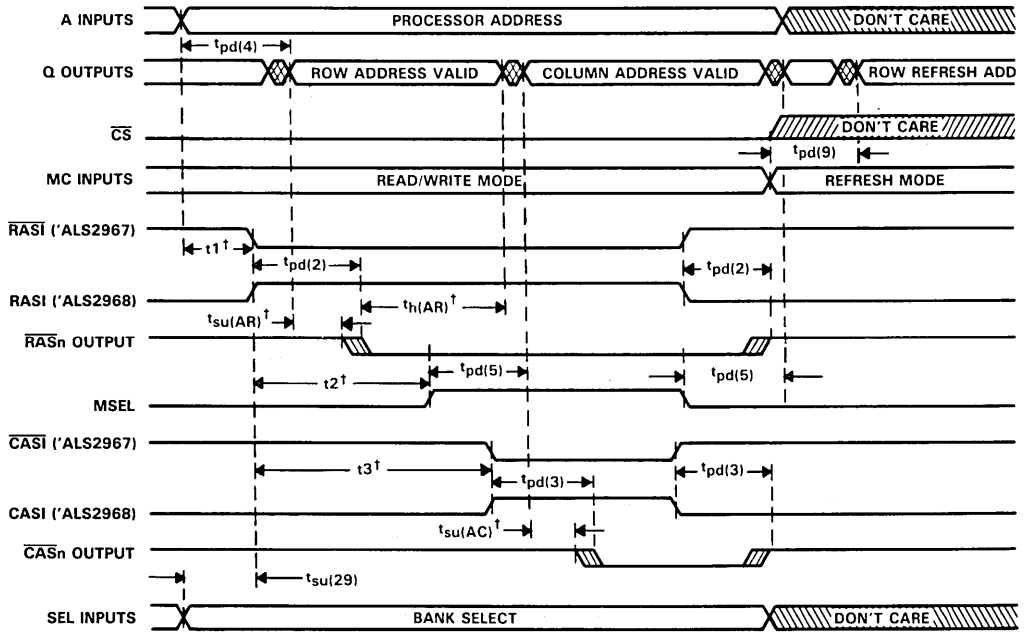

FIGURE 4. READ/WRITE CYCLE TIMING (MC1, MC0 = 1, 0), (LE = H)

† Parameters $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. Parameters t1, t2, and t3 represent the minimum timing requirements at the inputs to the DMC that guarantee DRAM timing specifications and maximum system performance. The minimum requirements for t1, t2, and t3 are as follows:

$t1(min) = t_{pd(4)}\ max + t_{su(AR)}\ min - t_{pd(2)}\ min$
$t2(min) = t_{pd(2)}\ max + t_{h(AR)}\ min - t_{pd(5)}\ min$
$t3(min) = t2\ min + t_{pd(5)}\ max + t_{su(AC)} - t_{pd(3)}\ min$

See the DRAM data sheet for applicable $t_{su(AR)}$, $t_{su(AR)}$, and $t_{h(AR)}$. In addition, note that propagation delay times given in the above equations are functions of capacitive loading. The values used in these equations must relate to actual system capacitive loading.

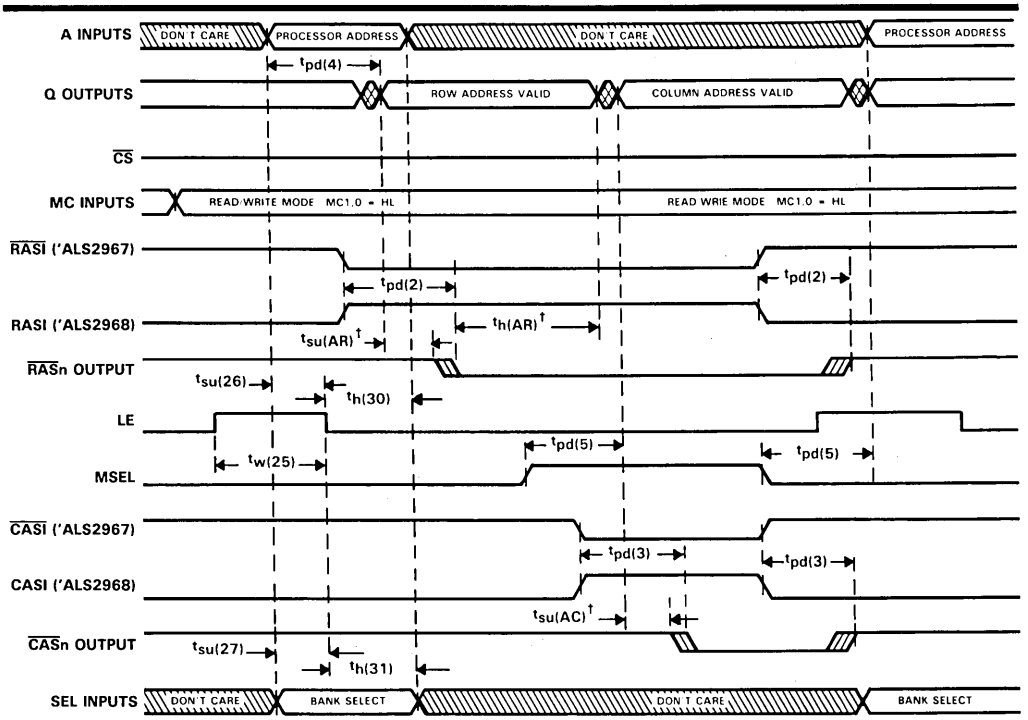

FIGURE 5. READ/WRITE CYCLE TIMING USING INPUT LATCHES (MC1, MC0 = H, L)

† $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. See the DRAM data sheet for applicable specifications.

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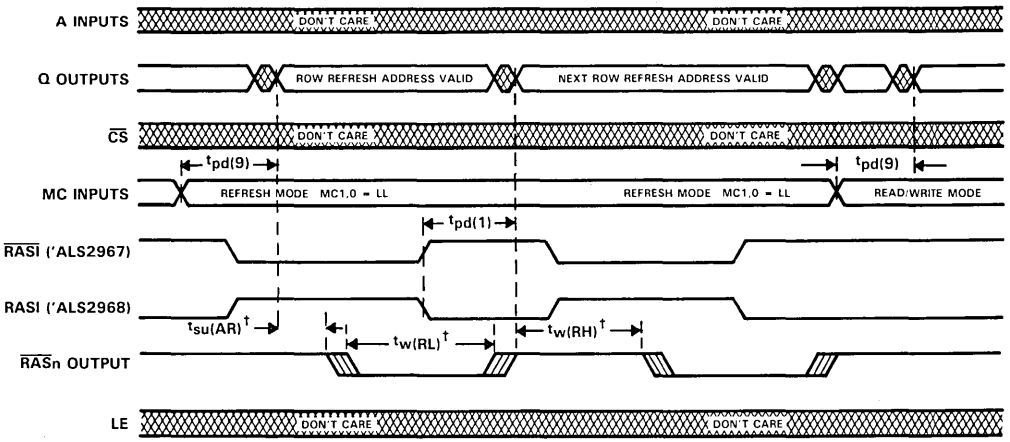


FIGURE 6. REFRESH CYCLE TIMING (MC1, MC0 = L, L) WITHOUT SCRUBBING

† $t_{su(AR)}$, $t_{w(RL)}$, and $t_{w(RH)}$ are timing requirements of the dynamic RAM. See DRAM data sheet for applicable specifications.

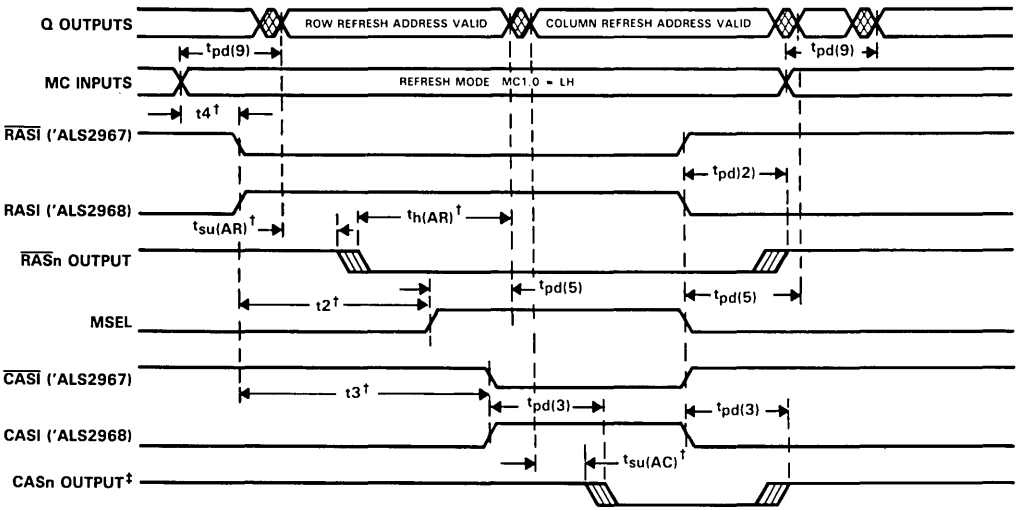


FIGURE 7. REFRESH CYCLE TIMING (MC1, MC0 = L, H) WITH MEMORY SCRUBBING

† Parameters $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. Parameters t2, t3, and t4 represent the minimum timing requirements at the inputs to the DMC that guarantee DRAM timing specifications and maximum system performance. The minimum requirement for t2, t3, and t4 are as follows:

$t2(min) = t_{pd(2)}\ max + t_{h(AR)}\ min - t_{pd(5)}\ min$
$t3(min) = t2\ min + t_{pd(5)}\ max + t_{su(AC)} - t_{pd(3)}\ min$
$t4(min) = t_{pd(9)}\ max + t_{su(AR)}\ min - t_{pd(2)}\ min$

See the DRAM data sheet for applicable $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$. In addition, note that propagation delay times given in the above equations are functions of capacitive loading. The values used in these equations must correspond to actual system capacitive loading.

‡ A $\overline{CAS}$n output is selected by the bank counter. All other $\overline{CAS}$n outputs will remain high.

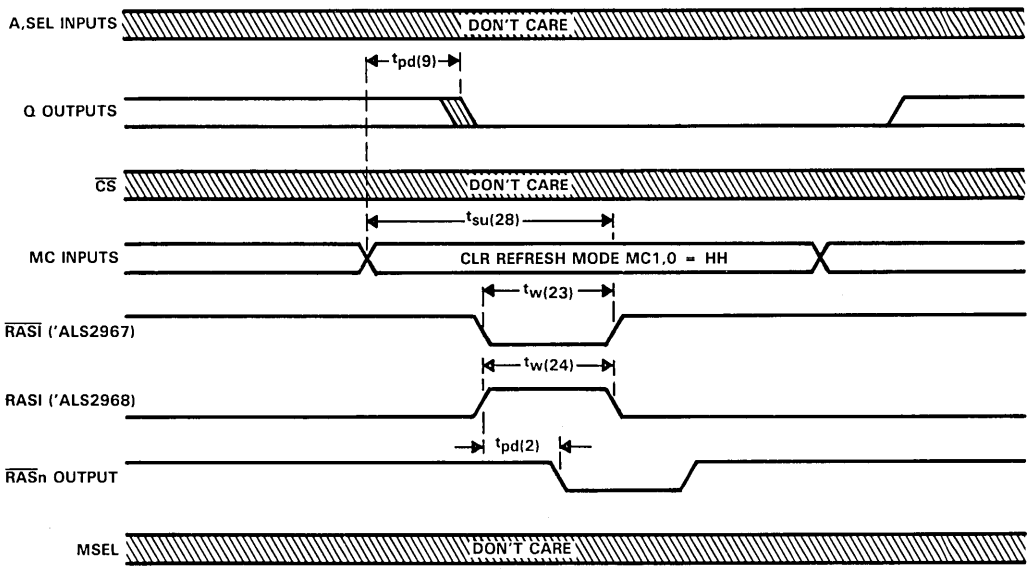
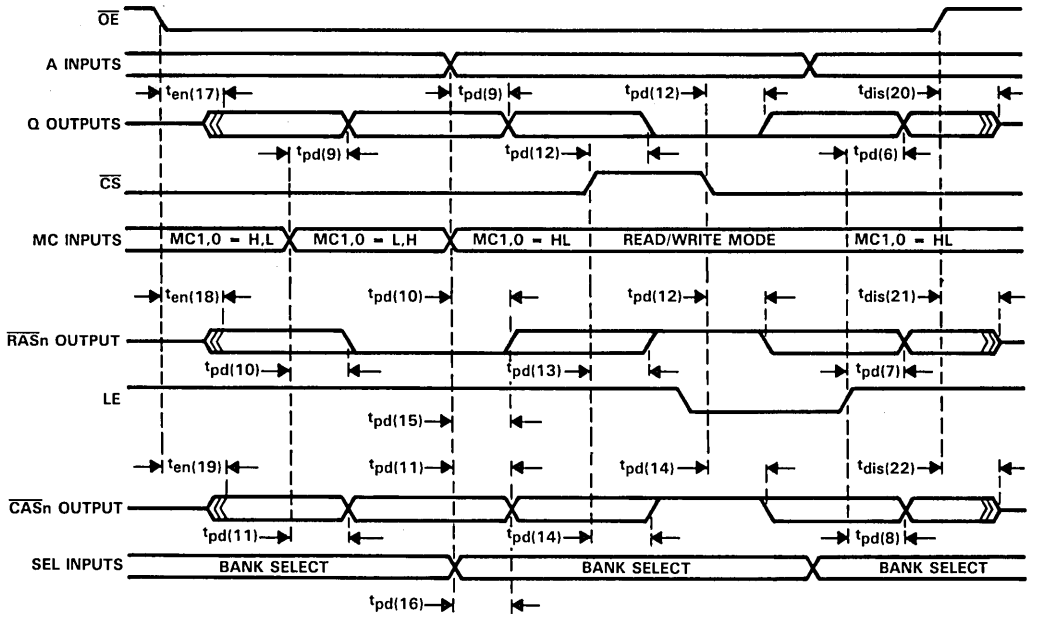


FIGURE 8. REFRESH COUNTER RESET (MC1, MC0 = H, H)



$\overline{RAS}$I ('ALS2967) = L, RASI ('ALS2968) = H, MSEL = H or L, $\overline{CAS}$I ('ALS2967) = L, CASI ('ALS2968) = H

FIGURE 9. MISCELLANEOUS TIMING

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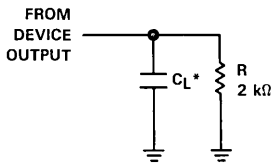
SWITCHING TEST CIRCUIT



* t_{pd} specified at C_L = 50, 150 pF

FIGURE 10. CAPACITIVE LOAD SWITCHING

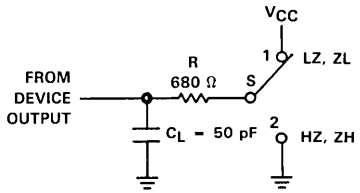


FIGURE 11. THREE-STATE ENABLE/DISABLE

TYPICAL SWITCHING CHARACTERISTICS

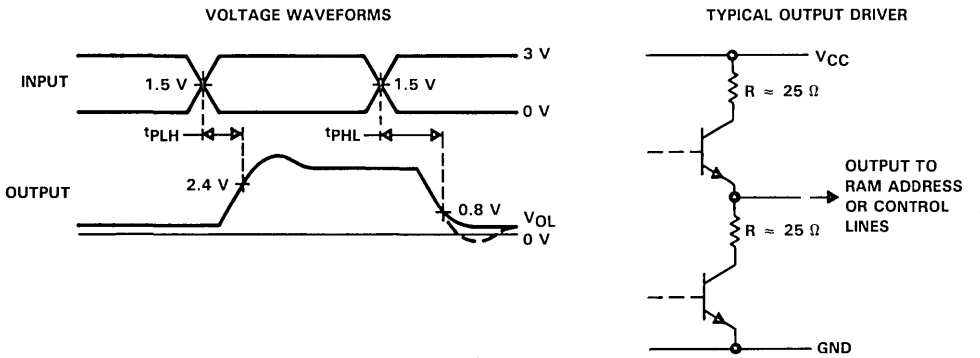
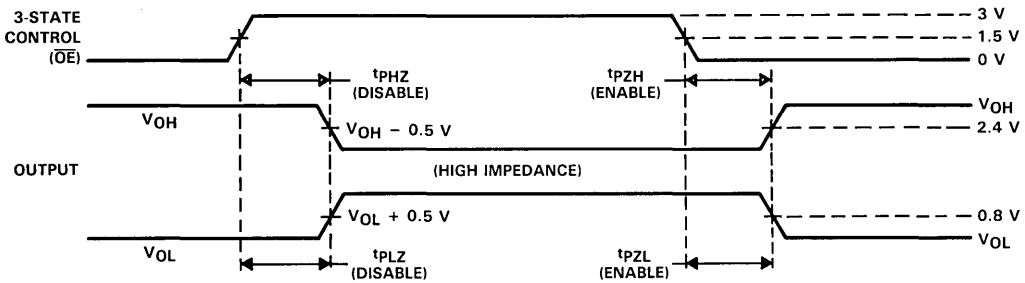


FIGURE 12. OUTPUT DRIVE LEVELS

THREE-STATE TIMING



NOTE: Decoupling is needed for all AC tests

FIGURE 13. THREE-STATE CONTROL LEVELS

D2900, JANUARY 1986–REVISED MARCH 1988

- **Provides Control for 16K, 64K, 256K, and 1M Dynamic RAMs**
- **Highest-Order Two-Address Bits Select One of Four Banks of RAMs**
- **Supports Scrubbing Operations and Nibble-Mode Access**
- **Separate Output Enable for Multi-Channel Access to Memory**
- **52-Pin Dual-In-Line Package**

description

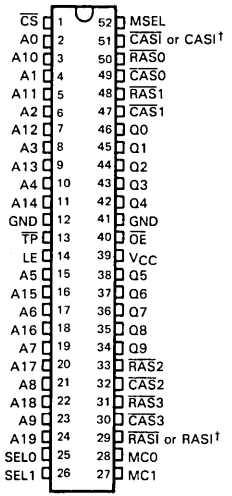
The 'ALS6301 and 'ALS6302 dynamic memory controllers (DMCs) are designed for use in today's high-performance memory systems. The DMC acts as the address controller between any processor and dynamic memory array.

Two versions are provided that help simplify interfacing to the system dynamic timing controller. The 'ALS6301 offers active-low Row Address Strobe Input ($\overline{RASI}$) and Column Address Strobe Input ($\overline{CASI}$), while the 'ALS6302 offers active-high Row Address Strobe Input (RASI) and Column Address Strobe Input (CASI) inputs.

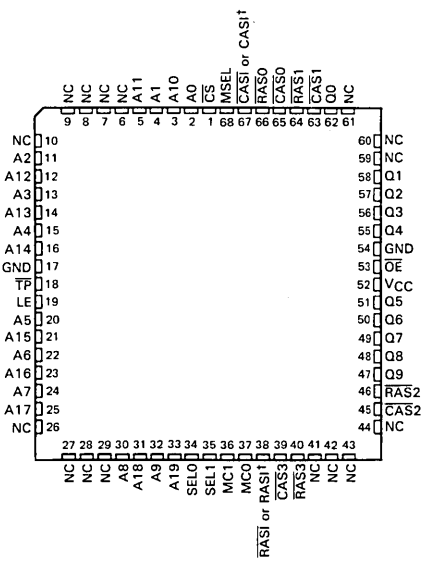
Using two 10-bit address latches, the DMC will hold the row and column addresses for any DRAM up to 1M. These latches and the two row/column refresh address counters feed into a 10-bit, 4-input MUX for output to the dynamic RAM address lines. A 2-bit bank select latch is provided to select one of the four $\overline{RAS}$ and $\overline{CAS}$ outputs. The two bits are normally obtained from the two highest-order address bits.

The 'ALS6301 and 'ALS6302 have two basic modes of operation, read/write and refresh. During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM, with the corresponding $\overline{RAS}$ and $\overline{CAS}$ signals activated to strobe the addresses into the RAM. In the refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the row counter is used. When memory scrubbing is being performed, both the row and column counters are used to perform read-modify-write cycles. In this mode all $\overline{RAS}$ outputs will be active (low) while only one $\overline{CAS}$ output is active at a time.

SN74ALS6301, SN74ALS6302 . . . JD OR N PACKAGE
(TOP VIEW)



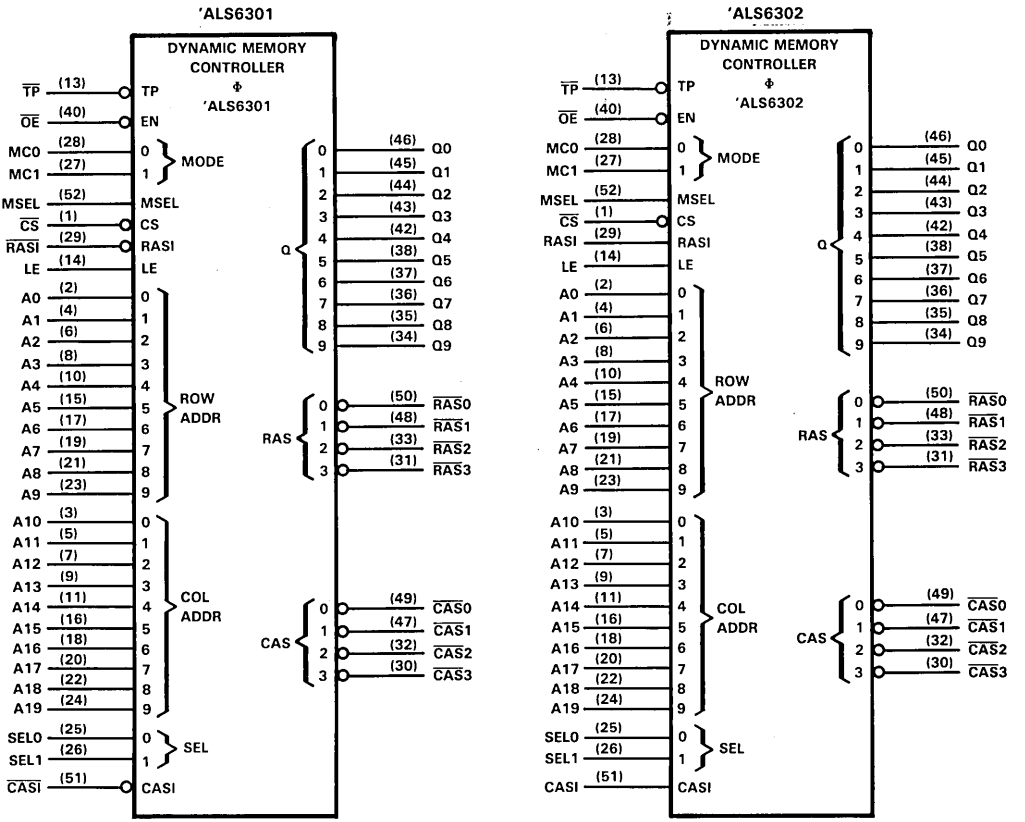
SN74ALS6301, SN74ALS6302 . . . FN PACKAGE
(TOP VIEW)



† 'ALS6301 has active-low inputs $\overline{CASI}$ and $\overline{RASI}$; 'ALS6302 has active-high inputs CASI and RASI.

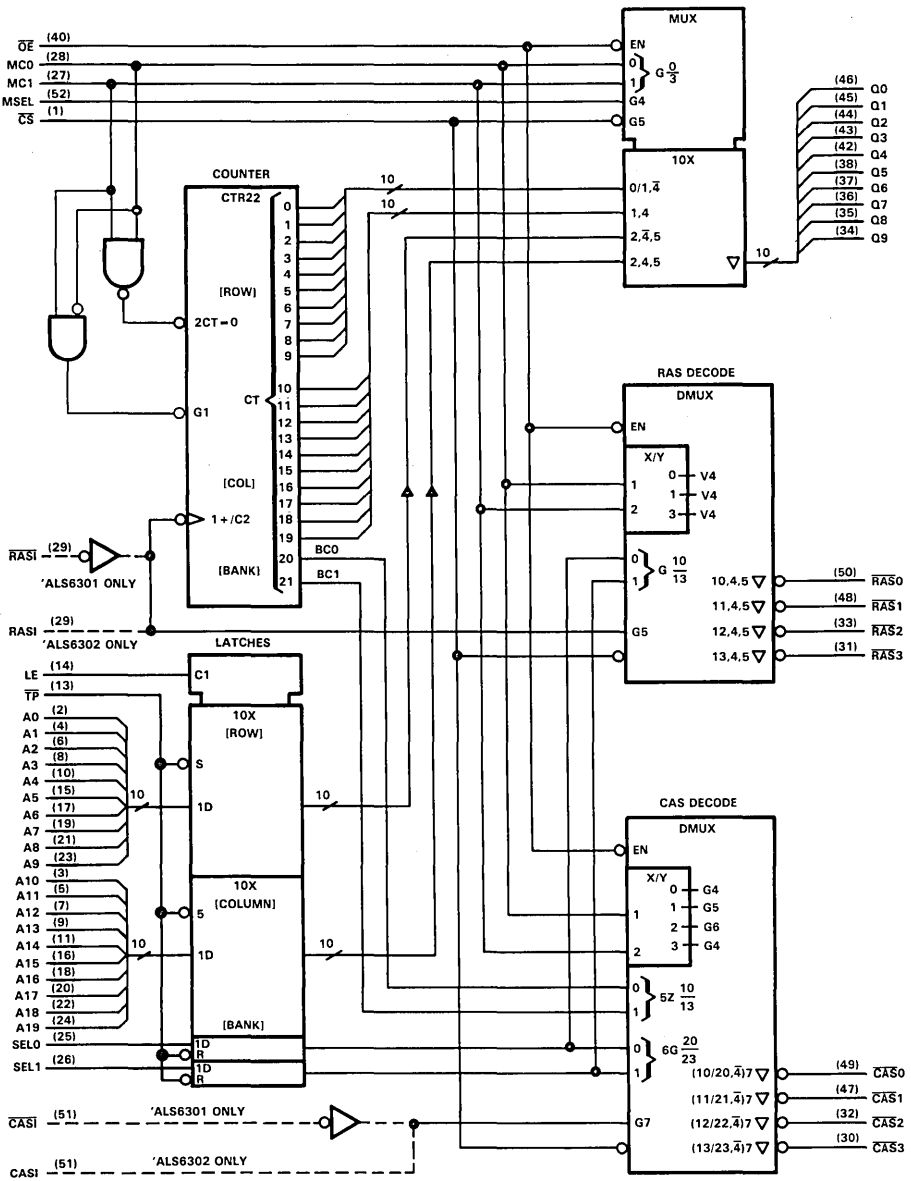
The SN74ALS6301 and SN74ALS6302 are characterized for operation from 0°C to 70°C.

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std-91-1984 and IEC Publication 617-12.
Pin numbers shown are for JD and N packages.

logic diagram (positive logic)



Pin numbers shown are for JD and N packages.

TABLE 1. PIN FUNCTION

PIN NAME	DESCRIPTION
A0-A19	Address Inputs. A0-A9 are latched in as the nine-bit row address for the DRAM. These inputs drive Q0-Q9 when the DMC is in the read/write mode and MSEL is low. A10-A19 are latched in as the column address, and will drive Q0-Q9 when MSEL is high and the DMC is in the read/write mode. The addresses are latched when the Latch Enable (LE) input signal is low.
SEL0, SEL1	Bank Select. These two inputs are normally the two highest-order address bits and are used in the read/write mode to select which bank of memory will be receiving the $\overline{RAS}$ and $\overline{CAS}$ signals after $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302) and $\overline{CASI}$ ('ALS6301) or CASI ('ALS6302) go active.
LE	Latch Enable. This active-high input causes the row, column, and bank select latches to become transparent, allowing the latches to accept new input data. A low input on LE latches the input data.
MSEL	Multiplexer Select. This input determines whether the row or column address will be sent to the memory address inputs. When MSEL is high, the column address is selected, while the row address is selected when MSEL is low. The address may come from either the address latch or refresh address counter depending on MC0 and MC1 (see Mode Control Function Table).
$\overline{CS}$	Chip Select. This active-low input is used to enable the DMC. When $\overline{CS}$ is active, the DMC operates normally in all four modes. When $\overline{CS}$ goes high, the device will not enter the read/write mode. This allows other devices to access the same memory that the DMC is controlling.
$\overline{OE}$	Output Enable. This active-low input enables/disables the output signals. When $\overline{OE}$ is high, the outputs of the DMC enter the high-impedance state.
MC0-MC1	Mode Controls. These inputs determine in which of the four modes the DMC operates. The description of each of the four operating modes is given in Table 2.
Q0-Q9	Address Outputs. These address outputs feed the DRAM address inputs and provide drive for memory systems having capacitance of up to 500 picofarads.
$\overline{RASI}$ or RASI	Row Address Strobe Input. During the normal memory cycles, the decoded $\overline{RAS}$n output ($\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, or $\overline{RAS3}$) is forced low after receipt of an active Row Address Strobe Input signal. In either Refresh mode, all four $\overline{RAS}$ outputs will be low while the Row Address Strobe Input signal is active. The $\overline{RASI}$ on the 'ALS6301 is an active-low input while on the 'ALS6302, RASI is an active-high input. (For more details see timing diagrams).
$\overline{RAS0}$-$\overline{RAS3}$	Row Address Strobe. Each of the Row Address Strobe outputs provides a $\overline{RAS}$ signal to one of the four banks of dynamic memory. Each $\overline{RAS}$n output will go low when selected by SEL0 and SEL1 after $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302) goes active. All four go low in response to $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302) while in the refresh mode.
$\overline{CASI}$ or CASI	Column Address Strobe Input. This input going active causes the selected $\overline{CAS}$ output to be forced low. The $\overline{CASI}$ input on the 'ALS6301 is active low input while on the 'ALS6302, CASI is active high input. (For more details see timing diagrams.)
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe. During normal Read/Write cycles the two selected bits (SEL0, SEL1) determine which $\overline{CAS}$ output will go active following $\overline{CASI}$ ('ALS6301) or CASI ('ALS6302) going active. When memory scrubbing is being performed, only the $\overline{CAS}$n signal selected will be active. For non-scrubbing cycles, all four $\overline{CAS}$ outputs will remain high.
$\overline{TP}$	This active-low test input asynchronously sets the row and column input latches high, while forcing the two bank select latches low. In normal operation, $\overline{TP}$ is tied high.

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TABLE 2. MODE-CONTROL FUNCTION TABLE

MC1	MC0	OPERATING MODE
L	L	Refresh Mode without Scrubbing. Refresh cycles are performed with only the row counter being used to generate the addresses. In this mode, all four $\overline{RAS}$ outputs are active while the four $\overline{CAS}$ outputs remain high.
L	H	Refresh with Scrubbing/Initialize. During this mode, refresh cycles are done with both the row and column counters generating the addresses. MSEL is used to select either the row or the column counter. All four $\overline{RAS}$ outputs go low in response to $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302), while only one $\overline{CAS}$n output goes low in response to $\overline{CASI}$ ('ALS6301) or CASI ('ALS6302). The bank counter keeps track of which $\overline{CAS}$ output goes active. This mode can also be used during system power-up so that the memory can be written with a known data pattern.
H	L	Read/Write. This mode is used to perform read/write cycles. Both the Row and Column addresses are multiplexed to the address output lines using MSEL. SEL0 and SEL1 are decoded to determine which $\overline{RAS}$n and $\overline{CAS}$n outputs will be active. The refresh counter is disabled while in this mode.
H	H	Clear Refresh Counters. This mode clears the three refresh counters (row, column, and bank) on the inactive transition of $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302), putting them at start of the refresh sequence (see timing diagrams for more detail). In this mode, all four $\overline{RAS}$ outputs are driven low after the active edge of $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302) so that DRAM wake-up cycles may also be performed.

TABLE 3. ADDRESS OUTPUT FUNCTIONS

MODE	INPUTS				OUTPUTS Q0-Q9
	MC1	MC0	MSEL	$\overline{CS}$	
Refresh without scrubbing	L	L	X	X	Row counter address
Refresh with scrubbing	L	H	L	X	Row counter address
			H	X	Column counter address
Read/write	H	L	L	L	Row address†
			H	L	Column address†
			X	H	All L
Clear refresh counter‡	H	H	X	X	All L

TABLE 4. RAS OUTPUT FUNCTIONS

INPUTS							OUTPUTS			
'ALS6301 $\overline{RASI}$	'ALS6302 RASI	MC1	MC0	SEL1†	SEL0†	$\overline{CS}$	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{RAS2}$	$\overline{RAS3}$
L	H	L	L	X	X	X	L	L	L	L
L	H	L	H	X	X	X	L	L	L	L
L	H	H	L	L	L	L	L	H	H	H
				L	H	L	H	L	H	H
				H	L	L	H	H	L	H
				H	H	L	H	H	H	L
				X	X	H	H	H	H	H
L	H	H	H	X	X	X	L	L	L	L
H	L	X	X	X	X	X	H	H	H	H

TABLE 5. CAS OUTPUT FUNCTIONS

INPUTS									OUTPUTS			
'ALS6301 $\overline{CASI}$	'ALS6302 CASI	MC1	MC0	SEL1†	SEL0†	INTERNAL BC1	INTERNAL BC0	$\overline{CS}$	$\overline{CAS0}$	$\overline{CAS1}$	$\overline{CAS2}$	$\overline{CAS3}$
L	H	L	L	X	X	X	X	X	H	H	H	H
L	H	L	H	X	X	L	L	X	L	H	H	H
						L	H	X	H	L	H	H
						H	L	X	H	H	L	H
						H	H	X	H	H	H	L
L	H	H	L	L	L	X	X	L	L	H	H	H
				L	H	X	X	L	H	L	H	H
				H	L	X	X	L	H	H	L	H
				H	H	X	X	L	H	H	H	L
				X	X	X	X	H	H	H	H	H
L	H	H	H	X	X	X	X	X	H	H	H	H
H	L	X	X	X	X	X	X	X	H	H	H	H

† If $\overline{TP}$ is low, the row and column address latch will be high. If $\overline{TP}$ is high, the row and column address latch will be at the levels entered when LE was last high.

‡ For 'ALS6301, clearing occurs on the low-to-high transition of $\overline{RASI}$; for 'ALS6302, clearing occurs on the high-to-low transition of RASI.

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read/write operation details

During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM controlled by the MSEL input. The corresponding $\overline{RAS}$n and $\overline{CAS}$n output signals strobe the addresses into memory. The block diagram in Figure 1 shows a typical system interface for a four-megaword dynamic memory. The DMC is used to control the four banks of 1M memory.

For systems where addresses and data are multiplexed onto a single bus, the DMC uses latches, (row, column, and bank) to hold the address information. Figure 5 shows a typical timing diagram using the input latches. The twenty-two input latches are transparent when latch enable (LE) is high, and latch the input data whenever LE is taken low. For systems in which the processor has separate address and data buses, LE may be permanently high (see timing diagram in Figure 4).

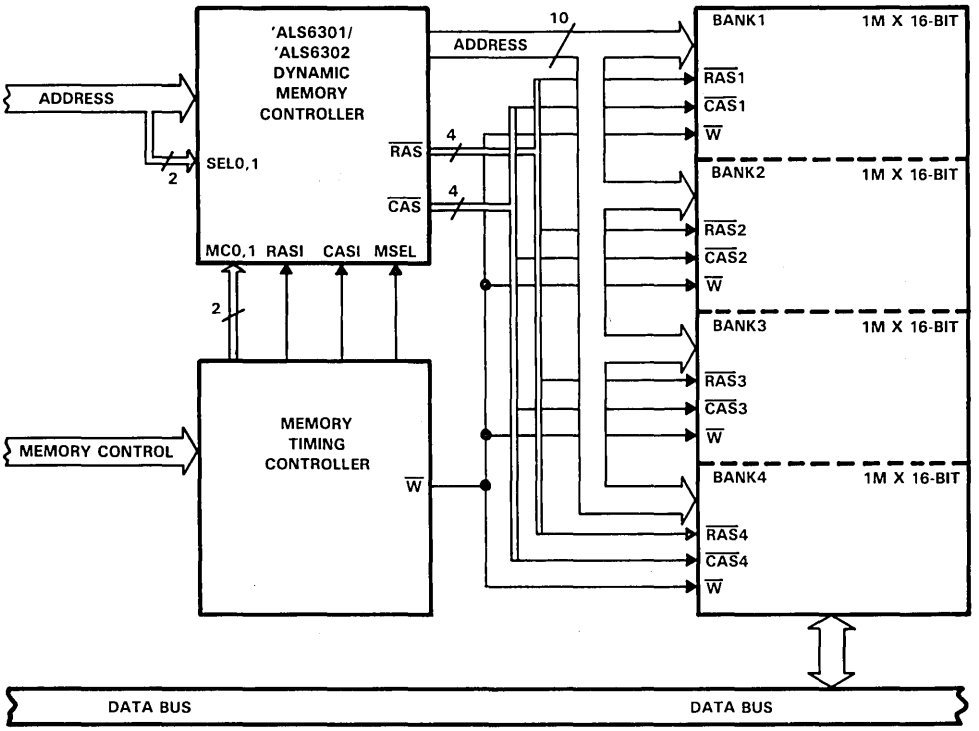

FIGURE 1. 4-MEGAWORD X 16-BIT DYNAMIC MEMORY

read/write operations (continued)

The DMC is designed with heavy-duty outputs that are capable of driving four banks of 16-bit words, including six checkbits used for error detection and correction.

In addition to heavy-duty output drivers, the outputs are designed with balanced output impedances (25 Ω both high and low). This feature optimizes the drive low characteristics, based on safe undershoot, while providing symmetrical drive high characteristics. It also eliminates the external resistors required to pull the outputs up to the MOS V_{OH} level (V_{CC} – 1.5 V).

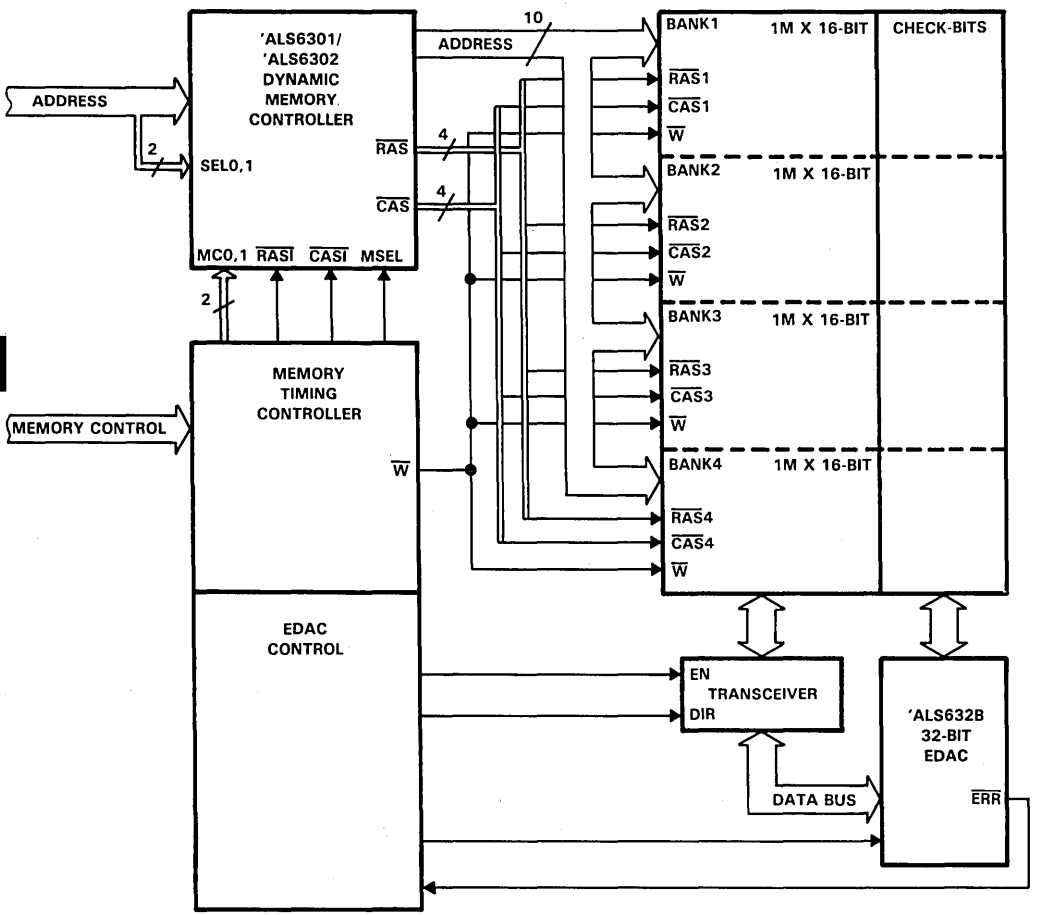

FIGURE 2. 4-MEGAWORD X 16-BIT DYNAMIC MEMORY WITH ERROR DETECTION AND CORRECTION

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memory expansion

With a 10-bit address path, the DMC can control up to four megaword when using 1M dynamic RAMs. If a larger memory size is desired, the DMC's chip select ($\overline{CS}$) makes it easy to expand the memory size by using additional DMCs. A sixteen-megaword memory system is shown in Figure 3.

To maintain maximum performance in 32-bit applications, it is recommended that individual bus drivers be used for each bank.

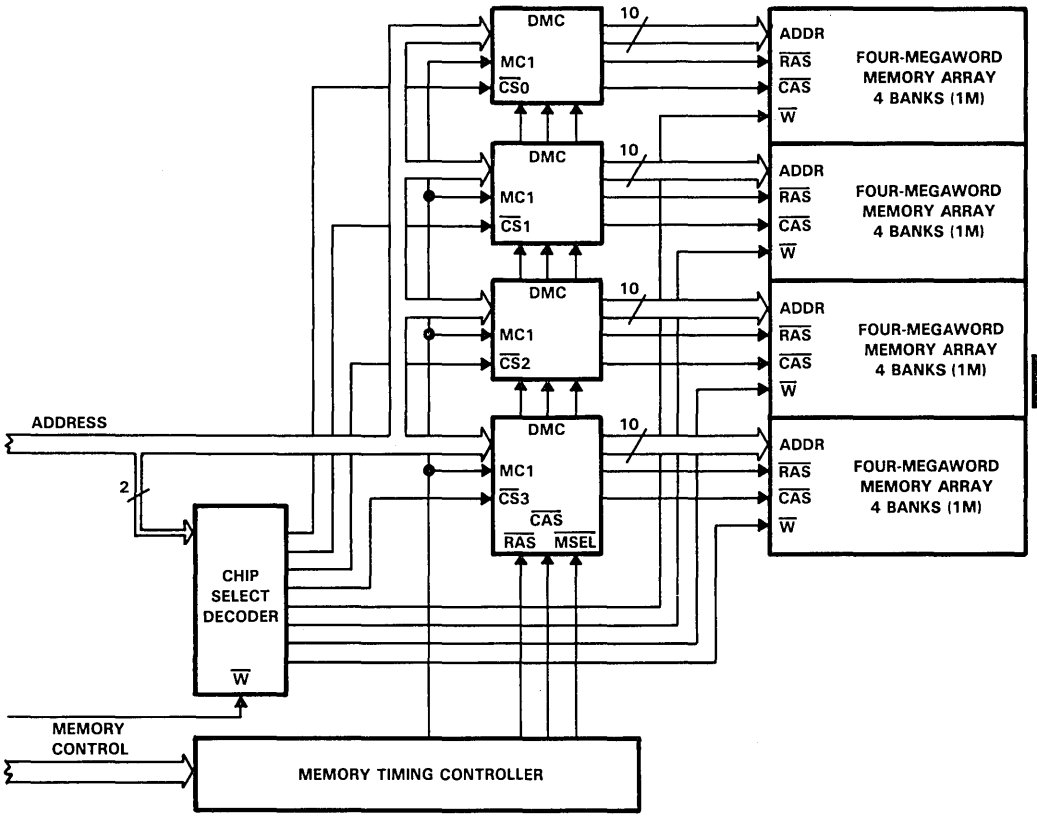

FIGURE 3. 16-MEGAWORD X 16-BIT DYNAMIC MEMORY

refresh operations

The two 10-bit counters in the 'ALS6301 and 'ALS6302 support 128-, 256-, 512-, and 1024-line refresh operations. Transparent, burst, synchronous, or asynchronous refresh modes are all possible. The refresh counters are advanced on the low-to-high transition of $\overline{\text{RASI}}$ on the 'ALS6301, and on the high-to-low transition of RASI on the 'ALS6302. The refresh counters are reset to zero on the low-to-high transition of $\overline{\text{RASI}}$ on the 'ALS6301, and on the high-to-low transition of RASI on the 'ALS6302, if MC1 and MC0 are at a high logic level. See Figure 8 for additional timing details.

When performing refresh cycles without memory scrubbing (MC1 and MC0 both low), all four $\overline{\text{RAS}}$ outputs go low, while all $\overline{\text{CAS}}$ outputs are driven high. Typical timing for this mode of operation is shown in Figure 6.

decoupling

Due to the high switching speed and high drive capability of the 'ALS6301 and 'ALS6302, it is necessary to decouple the device for proper operation. Multilayer ceramic 0.1-μF to 1-μF capacitors are recommended for decoupling. It is important to mount the capacitors as close as possible to the power pins (V_{CC} and GND) to minimize lead inductance and noise. A ground plane is recommended.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2.6	mA
I_{OL}	Low-level output current				12	mA
t_w	Pulse duration	(23) $\overline{RASI}$ low or RASI high	10			ns
		(24) $\overline{RASI}$ high or RASI low	10			
		(25) LE high	10			
t_{su}	Setup time	(26) An before LE↓	5			ns
		(27) SELn before LE↓	5			
		(28) MC0,1 high before $\overline{RASI}$↑ or RASI↓	10			
		(29) SELn before $\overline{RASI}$↓ or RASI↑	5			
t_h	Hold time	(30) An after LE↓	5			ns
		(31) SELn after LE↓	5			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8	
I_{OL}‡	V_{CC} = 4.5 V,	V_O = 2 V	30			mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			136	220	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and duration should not exceed 1 second.
§ The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, I_{OS}.

'ALS6301 switching characteristics, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	$\overline{RASI}$	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	5	16	30	ns
$t_{pd(2)}$	$\overline{RASI}$	$\overline{RAS}$n		2	10	14	ns
$t_{pd(3)}$	$\overline{CASI}$	$\overline{CAS}$n		2	7	14	ns
$t_{pd(4)}$	Any A	Any Q		3	9	17	ns
$t_{pd(5)}$	MSEL	Any Q		5	13	22	ns
$t_{pd(6)}$	LE↑	Any Q			13	22	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			13	22	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			13	22	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		6	14	24	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		2	10	15	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		2	10	15	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			13	24	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			7	13	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			9	13	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			9	15	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			9	15	ns
$t_{en(17)}$	$\overline{OE}$↓	Any Q			10	18	ns
$t_{en(18)}$	$\overline{OE}$↓	Any $\overline{RAS}$			10	18	ns
$t_{en(19)}$	$\overline{OE}$↓	Any $\overline{CAS}$			10	18	ns
$t_{dis(20)}$	$\overline{OE}$↑	Any Q			12	20	ns
$t_{dis(21)}$	$\overline{OE}$↑	Any $\overline{RAS}$			12	20	ns
$t_{dis(22)}$	$\overline{OE}$↑	Any $\overline{CAS}$			12	20	ns

'ALS6301 switching characteristics, C_L = 150 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	$\overline{RASI}$	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	10	20	35	ns
$t_{pd(2)}$	$\overline{RASI}$	$\overline{RAS}$n		3	9	18	ns
$t_{pd(3)}$	$\overline{CASI}$	$\overline{CAS}$n		2	7	18	ns
$t_{pd(4)}$	Any A	Any Q		5	11	18	ns
$t_{pd(5)}$	MSEL	Any Q		5	15	24	ns
$t_{pd(6)}$	LE↑	Any Q			13	24	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			13	24	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			13	24	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		8	15	25	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		5	10	16	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		5	10	16	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			16	25	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			9	15	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			9	15	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			10	17	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			10	17	ns

†See Figures 10, 11, 12, and 13 for test circuit and switching waveforms.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

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'ALS6302 switching characteristics, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	RASI	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	5	16	30	ns
$t_{pd(2)}$	RASI	$\overline{RAS}$n		2	10	14	ns
$t_{pd(3)}$	CASI	$\overline{CAS}$n		2	7	14	ns
$t_{pd(4)}$	Any A	Any Q		3	9	17	ns
$t_{pd(5)}$	MSEL	Any Q		5	13	22	ns
$t_{pd(6)}$	LE↑	Any Q			13	22	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			13	22	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			13	22	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		6	14	24	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		2	10	15	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		2	10	15	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			13	24	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			7	13	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			9	13	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			9	15	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			9	15	ns
$t_{en(17)}$	$\overline{OE}$↓	Any Q			10	18	ns
$t_{en(18)}$	$\overline{OE}$↓	Any $\overline{RAS}$			10	18	ns
$t_{en(19)}$	$\overline{OE}$↓	Any $\overline{CAS}$			10	18	ns
$t_{dis(20)}$	$\overline{OE}$↑	Any Q			12	20	ns
$t_{dis(21)}$	$\overline{OE}$↑	Any $\overline{RAS}$			12	20	ns
$t_{dis(22)}$	$\overline{OE}$↑	Any $\overline{CAS}$			12	20	ns

'ALS6302 switching characteristics, C_L = 150 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	RASI	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	10	20	35	ns
$t_{pd(2)}$	RASI	$\overline{RAS}$n		3	9	18	ns
$t_{pd(3)}$	CASI	$\overline{CAS}$n		2	7	18	ns
$t_{pd(4)}$	Any A	Any Q		5	11	18	ns
$t_{pd(5)}$	MSEL	Any Q		5	15	24	ns
$t_{pd(6)}$	LE↑	Any Q			13	24	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			13	24	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			13	24	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		8	15	25	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		5	10	16	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		5	10	16	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			16	25	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			9	15	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			9	15	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			10	17	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			10	17	ns

†See Figures 10, 11, 12, and 13 for test circuit and switching waveforms.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

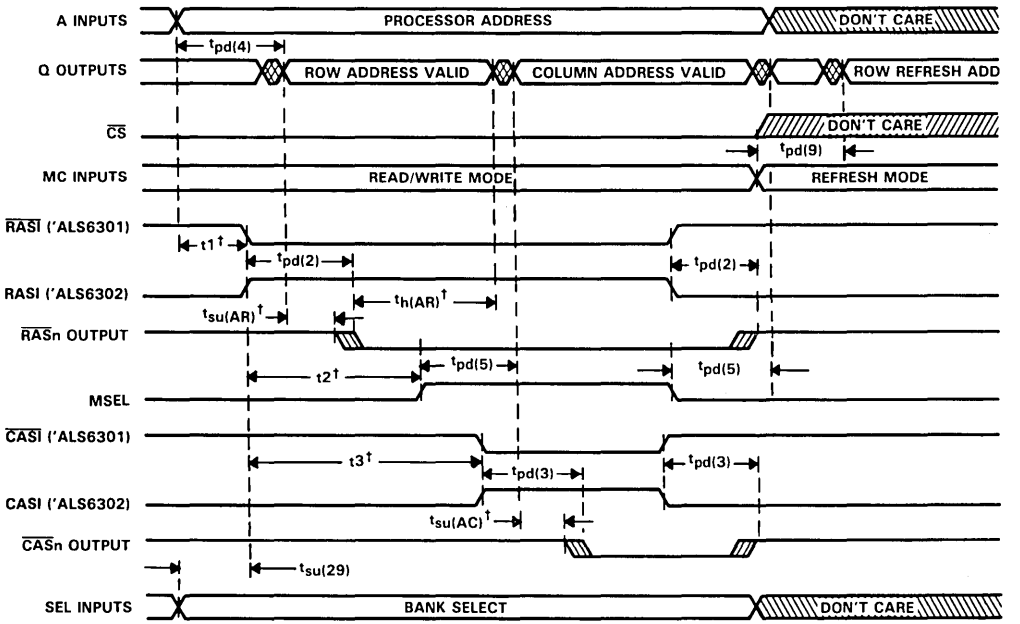

FIGURE 4. READ/WRITE CYCLE TIMING (MC1, MC0 = 1, 0), (LE = H)

† Parameters $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. Parameters t1, t2, and t3 represent the minimum timing requirements at the inputs to the DMC that guarantee DRAM timing specifications and maximum system performance. The minimum requirements for t1, t2, and t3 are as follows:

$t1(min) = t_{pd(4)}\ max + t_{su(AR)}\ min - t_{pd(2)}\ min$
$t2(min) = t_{pd(2)}\ max + t_{h(AR)}\ min - t_{pd(5)}\ min$
$t3(min) = t2\ min + t_{pd(5)}\ max + t_{su(AC)} - t_{pd(3)}\ min$

See the DRAM data sheet for applicable $t_{su(AR)}$, $t_{su(AR)}$, and $t_{h(AR)}$. In addition, note that propagation delay times given in the above equations are functions of capacitive loading. The values used in these equations must relate to actual system capacitive loading.

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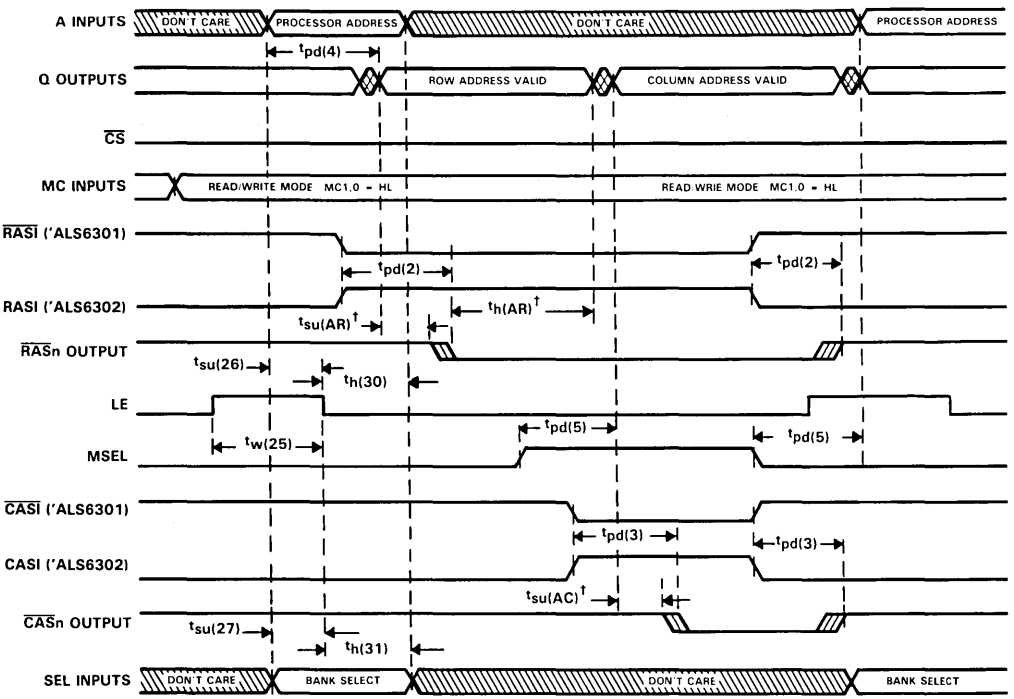

FIGURE 5. READ/WRITE CYCLE TIMING USING INPUT LATCHES (MC1, MC0 = H, L)

† $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. See the DRAM data sheet for applicable specifications.

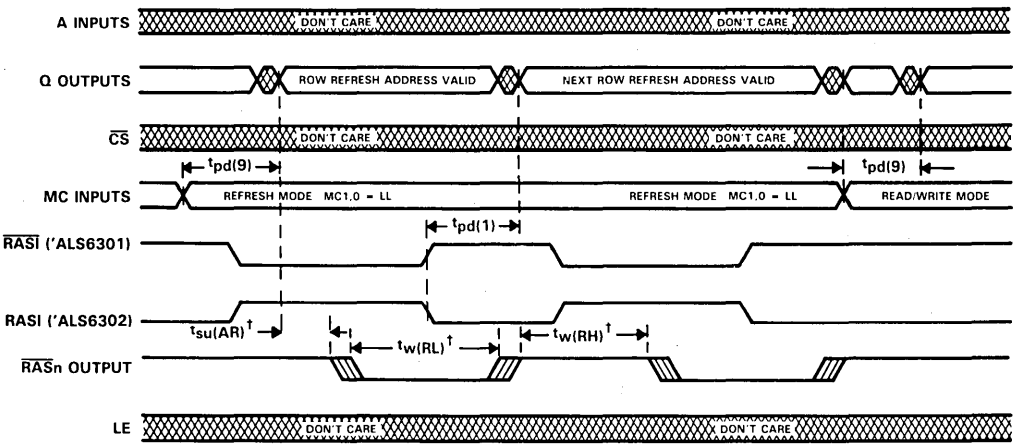

FIGURE 6. REFRESH CYCLE TIMING (MC1, MC0 = L, L) WITHOUT SCRUBBING

† $t_{su(AR)}$, $t_{w(RL)}$, and $t_{w(RH)}$ are timing requirements of the dynamic RAM. See DRAM data sheet for applicable specifications.

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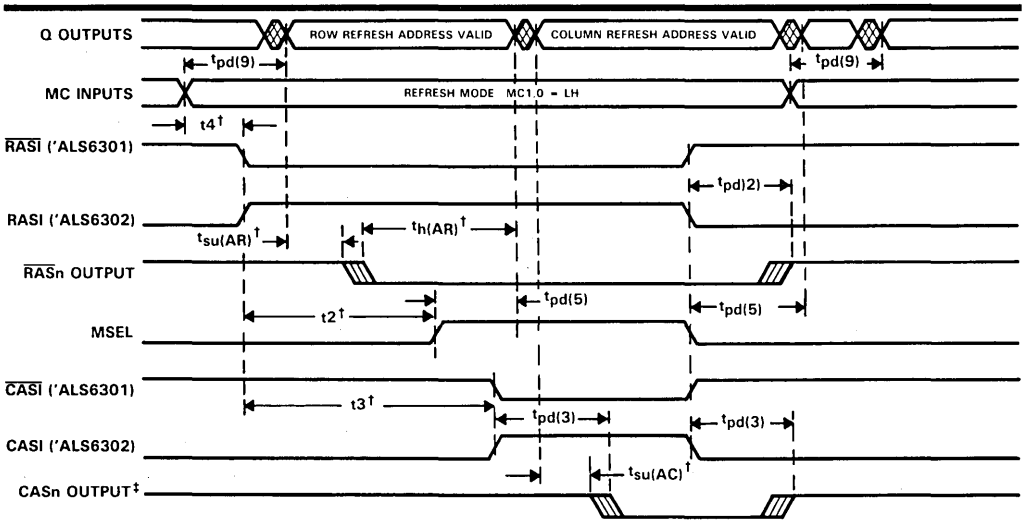

FIGURE 7. REFRESH CYCLE TIMING (MC1, MC0 = L, H) WITH MEMORY SCRUBBING

† Parameters $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. Parameters t2, t3, and t4 represent the minimum timing requirements at the inputs to the DMC that guarantee DRAM timing specifications and maximum system performance. The minimum requirement for t2, t3, and t4 are as follows:

$t2(min) = t_{pd(2)}\ max + t_{h(AR)}\ min - t_{pd(5)}\ min$
$t3(min) = t2\ min + t_{pd(5)}\ max + t_{su(AC)} - t_{pd(3)}\ min$
$t4(min) = t_{pd(9)}\ max + t_{su(AR)}\ min - t_{pd(2)}\ min$

See the DRAM data sheet for applicable $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$. In addition, note that propagation delay times given in the above equations are functions of capacitive loading. The values used in these equations must correspond to actual system capacitive loading.

‡ A $\overline{CAS}$n output is selected by the bank counter. All other $\overline{CAS}$n outputs will remain high.

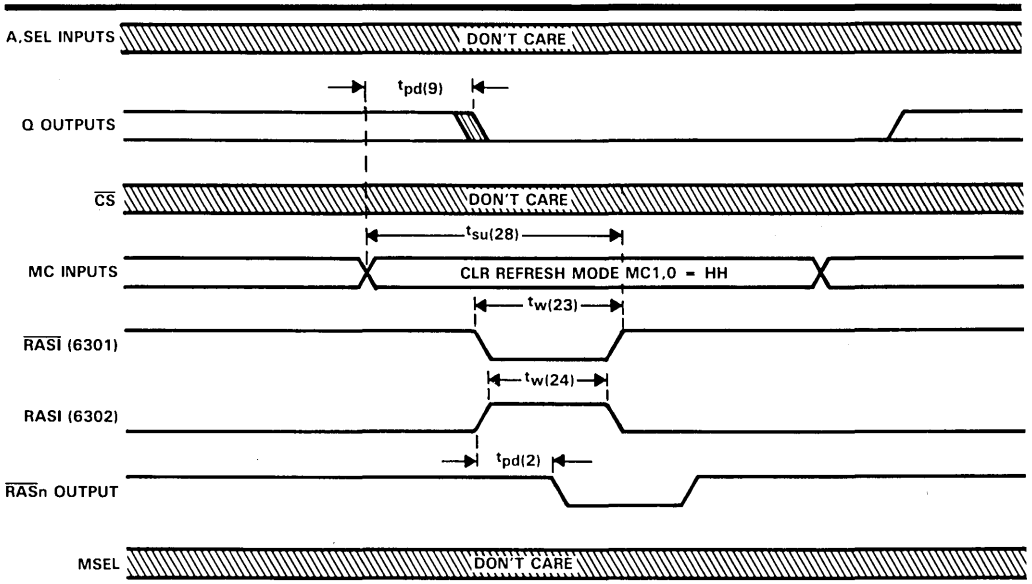

FIGURE 8. REFRESH COUNTER RESET (MC1, MC0 = H, H)

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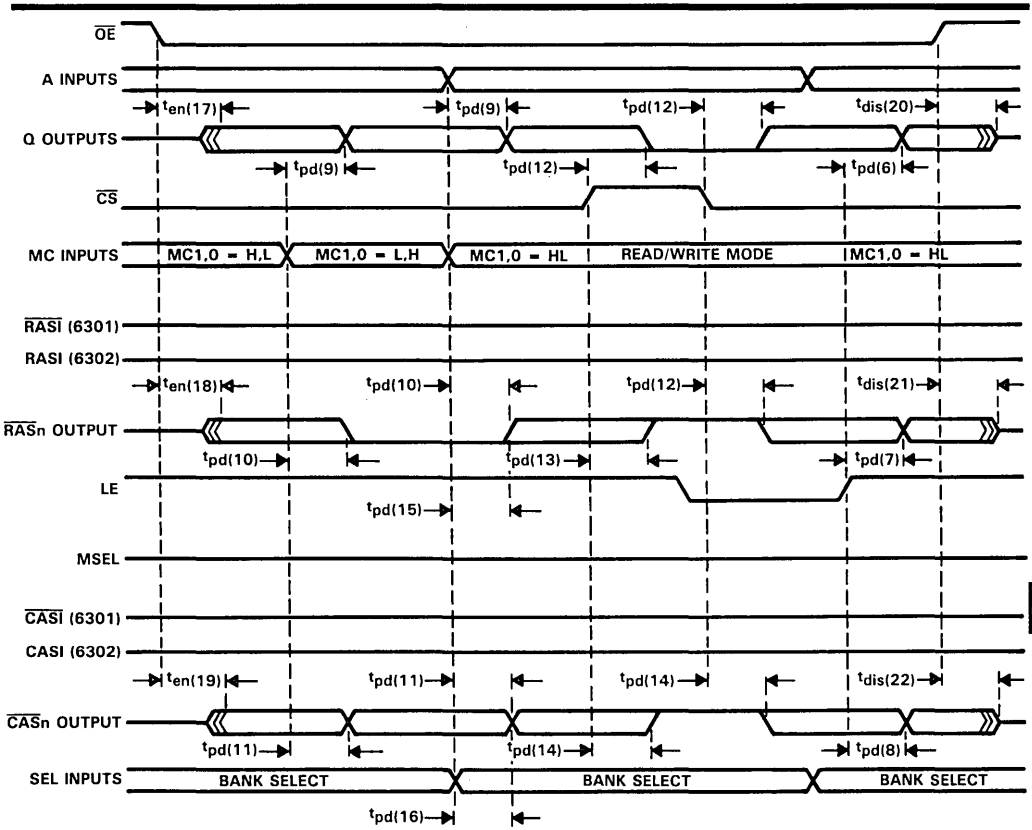
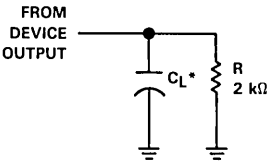


FIGURE 9. MISCELLANEOUS TIMING

SWITCHING TEST CIRCUIT



* t_{pd} specified at C_L = 50, 150 pF

FIGURE 10. CAPACITIVE LOAD SWITCHING

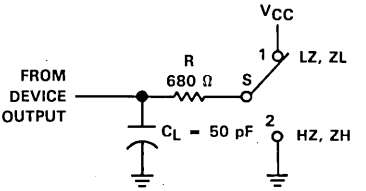


FIGURE 11. THREE-STATE ENABLE/DISABLE

TYPICAL SWITCHING CHARACTERISTICS

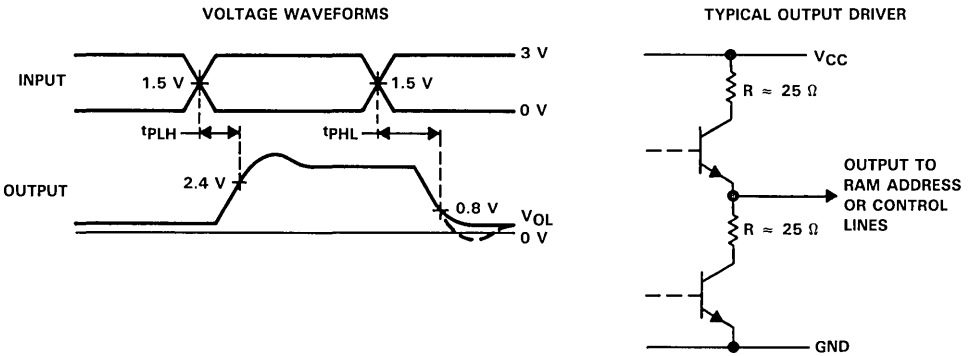
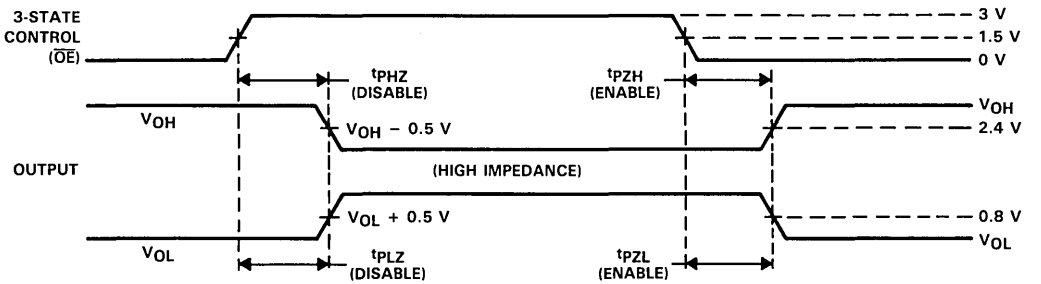


FIGURE 12. OUTPUT DRIVE LEVELS

THREE-STATE TIMING



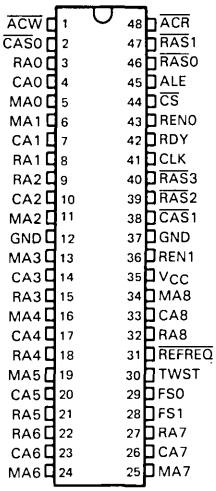
NOTE: Decoupling is needed for all AC tests

FIGURE 13. THREE-STATE CONTROL LEVELS

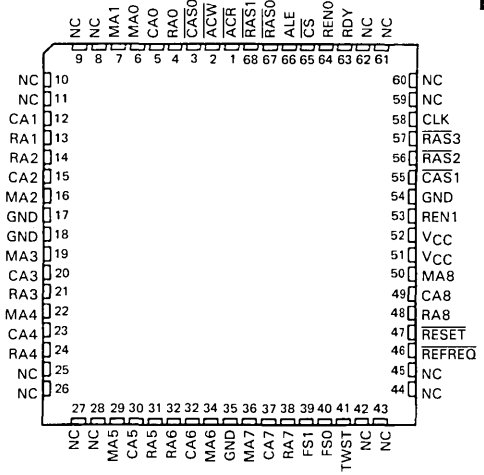
D2989, JUNE 1987

- Inputs are TTL- and CMOS-Voltage Compatible
- Controls Operation of 64K and 256K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 2 Megabytes of Memory Without External Drivers
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
  - Asynchronous $\overline{\text{RESET}}$ Function Provided in FK and FN Packages
- High-Performance Si-Gate CMOS Technology
- Strap-Selected Wait State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- 3-State Outputs Allow Multiport Memory Configuration
- Performance Range:
  115 ns ALE low to $\overline{\text{CAS}}$ low
- Functionally Equivalent to TMS4500A/B and to VTI VL4500A and VL4502
- Available in Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

JD OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The THCT4502B is a monolithic DRAM system controller providing address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

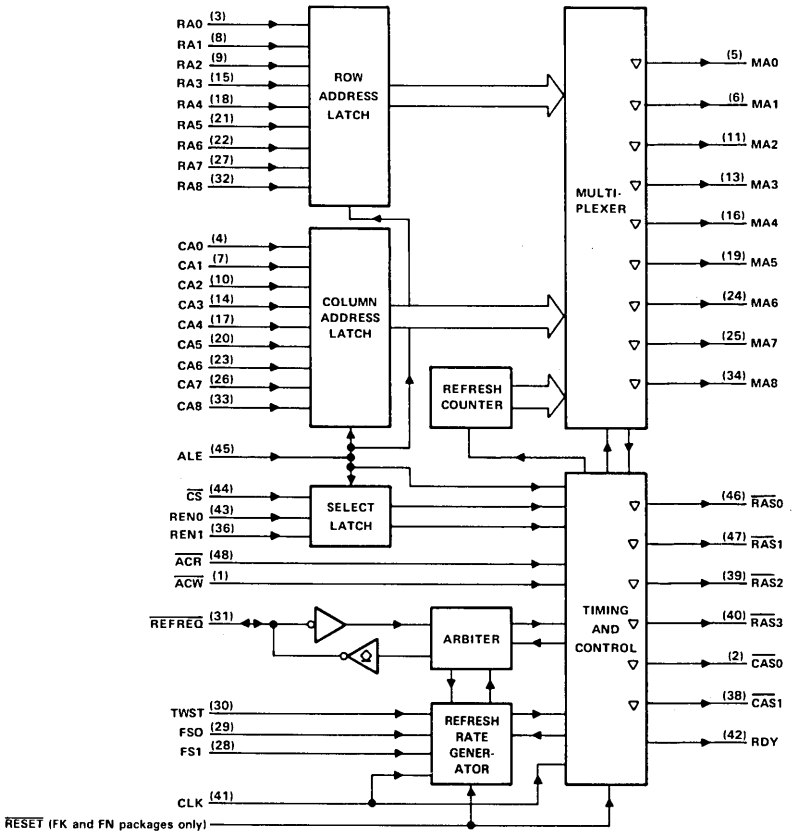
The controller contains an 18-bit multiplexer that generates the address lines for the memory device from the 18 system address bits and provides the strobe signals required by the memory to decode the address. A 9-bit refresh counter generates up to 512 row addresses required to refresh.

A refresh timer is provided to generate the necessary timing to refresh the dynamic memories and ensure data retention.

The THCT4502B also contains refresh/access arbitration circuitry to resolve conflicts between access requests and memory-refresh cycles.

The THCT4502B is characterized for operation from 0°C to 70°C.

functional block diagram



Pin numbers shown are for JD and N packages.

pin descriptions

RA0-RA8	Input	Row Address — These address inputs are used to generate the row address for the multiplexer.
CA0-CA8	Input	Column Address — These address inputs are used to generate the column address for the multiplexer.
MA0-MA8	Output	Memory Address — These three-state outputs are designed to drive the addresses of the dynamic RAM array.
ALE	Input	Address Latch Enable — This input is used to latch the 18 address inputs, $\overline{CS}$, REN0, and REN1. This also initiates an access cycle if $\overline{CS}$ is low. The rising edge (low level to high level) of ALE returns all $\overline{RAS}$ outputs to the high level.
$\overline{CS}$	Input	Chip Select — A low on this input enables an access cycle. The trailing edge of ALE latches the chip select input.
REN0, REN1	Inputs	$\overline{RAS}$ Enable 0 and 1 — These inputs are used to select one of four banks of RAM when $\overline{CS}$ is low. When REN1 is low, the lower banks are enabled via $\overline{CAS0}$, $\overline{RAS0}$, and $\overline{RAS1}$. When REN1 is high, the higher banks are enabled via $\overline{CAS1}$, $\overline{RAS2}$ and $\overline{RAS3}$. REN0 selects $\overline{RAS0}$ and $\overline{RAS2}$ when low, or $\overline{RAS1}$ and $\overline{RAS3}$ when high. (see Table 2).
$\overline{ACR}$, $\overline{ACW}$	Input	Access Control, Read; Access Control, Write — A low on either of these inputs causes the column address to appear on MA0-MA8 and a low-going pulse from $\overline{CAS}$. The rising edge of $\overline{ACR}$ or $\overline{ACW}$ terminates the cycle by forcing $\overline{RAS}$ and $\overline{CAS}$ high. When $\overline{ACR}$ and $\overline{ACW}$ are both low, MA0-MA8, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$, $\overline{CAS0}$ and $\overline{CAS1}$ go into a high-impedance (floating) state.
CLK	Input	System Clock — This input provides the master timing to generate refresh cycle timings and refresh rate. Refresh rate is determined by the TWST, FS1, and FS0 inputs.
$\overline{REFREQ}$	I/O	Refresh Request — This input should be driven by an open-collector or open-drain output. On input, a low-going edge initiates a refresh cycle and will cause the internal refresh timer to be reset on the next falling edge of the CLK. As an output, a low-going edge signals an internal refresh request and that the refresh timer will be reset on the next low-going edge of CLK. $\overline{REFREQ}$ will remain low until the refresh cycle is in progress and the current refresh address is present on MA0-MA8. (Note: $\overline{REFREQ}$ contains an internal active pullup with a nominal resistance of 10 kΩ, which is disabled when $\overline{REFREQ}$ is low).
$\overline{RAS0}$, $\overline{RAS1}$ $\overline{RAS2}$, $\overline{RAS3}$	Output	Row Address Strobe — These three-state outputs are used to latch the row address into the bank of DRAMs selected by REN0 and REN1. On refresh, all $\overline{RAS}$ signals are active.
$\overline{CAS0}$, $\overline{CAS1}$	Output	Column Address Strobe — These three-state outputs are used to latch the column address into the DRAM array.
RDY	Output	Ready — This totem-pole output synchronizes memories that are too slow to guarantee microprocessor access time requirements. This output is also used to inhibit access cycles during refresh when in cycle-steal mode.

pin descriptions (continued)

TWST	Input	Timing/Wait Strap — A high on this input indicates a wait state should be added to each memory cycle. In addition it is used in conjunction with FS0 and FS1 to determine refresh rate and timing or initialize the controller.
FS0, FS1	Inputs	Frequency Select 0; Frequency Select 1 — These are strap inputs to select Mode and Frequency of operation as shown in Table 1.
$\overline{\text{RESET}}$†	Input	$\overline{\text{RESET}}$ — Active-low input to initialize the controller asynchronously. Refresh Address is set to IFF_{16}, internal refresh requests, synchronizer, and frequency divider are cleared. (Note: $\overline{\text{RESET}}$ contains an internal pullup resistor with a nominal resistance of 100 kΩ, which allows this pin to be left open.)

†This function is available only in the FK and FN packages.

TABLE 1. STRAP CONFIGURATION

STRAP INPUT MODES			WAIT STATES FOR MEMORY ACCESS	REFRESH RATE	MINIMUM CLOCK FREQUENCY (MHz)	REFRESH FREQUENCY (kHz)	CLOCK CYCLES FOR EACH REFRESH
TWST	FS1	FS0					
L	L	L†	0	EXTERNAL	–	REFREQ	4
L	L	H	0	EXTERNAL	–	REFREQ	3
L	H	L	0	CLK ÷ 61	3.904	64-95‡	3
L	H	H	0	CLK ÷ 91	5.824	64-88§	4
H	L	L	1	CLK ÷ 61	3.904	64-95‡	3
H	L	H	1	CLK ÷ 91	5.824	64-75‡	4
H	H	L	1	CLK ÷ 106	6.784	64-73‡	4
H	H	H	1	CLK ÷ 121	7.744	64-83¶	4

† This strap configuration resets the Refresh Timer Circuitry.
‡ Upper figure in refresh frequency is the frequency that is produced if the minimum clock frequency of the next select state is used.
§ Refresh frequency if clock frequency is 8 MHz.
¶ Refresh frequency if clock frequency is 10 MHz.

TABLE 2. OUTPUT STROBE SELECTION

CONTROL INPUT		SELECTED OUTPUT					
REN1	REN0	$\overline{\text{RAS0}}$	$\overline{\text{RAS1}}$	$\overline{\text{RAS2}}$	$\overline{\text{RAS3}}$	$\overline{\text{CAS0}}$	$\overline{\text{CAS1}}$
L	L	X				X	
L	H		X			X	
H	L			X			X
H	H				X		X

NOTE: Changing the logic value of REN1 after a low-to-high transition of ALE and before $\overline{\text{ACX}}$ rises causes the other $\overline{\text{CAS}}$ to fall. Both $\overline{\text{CAS}}$ signals remain low until $\overline{\text{ACX}}$ rises.

functional description

The THCT4502B consists of six basic blocks: address and select latches, refresh rate generator, refresh counter, the multiplexer, the arbiter, and the timing and control block.

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address and select latches

The address and select latches allow the DRAM controller to be used in systems that multiplex address and data on the same lines without external latches. The row address latches are transparent, meaning that while ALE is high, the output at MA0-MA8 follows the inputs RA0-RA8.

refresh rate generator

The refresh rate generator is a counter that indicates to the arbiter that it is time for a refresh cycle. The counter divides the clock frequency according to the configuration straps as shown in Table 1. The counter is reset when a refresh cycle is requested or when TWST, FS1, and FS0 are low. The configuration straps allow the matching of memories to the system access time. Upon power-up it is necessary to provide a reset signal by driving all three straps to the controller (or $\overline{\text{RESET}}$ for devices in the FK and FN packages only) low. A systems power-on reset ($\overline{\text{RESET}}$) can be used to do this by connecting it to those straps that are desired high during operation. During this reset period, at least four clock cycles should occur.

refresh counter

The refresh counter contains the address of the row to be refreshed. The counter is decremented after each refresh cycle. A low-to-high transition on TWST sets the refresh counter to $1FF_{16}$ (511_{10}).

multiplexer

The multiplexer provides the DRAM array with row, column, and refresh addresses at the proper times. Its inputs are the address latches and the refresh counter. The outputs provide up to 18 multiplexed addresses on nine lines.

arbiter

The arbiter provides two operational cycles: access and refresh. The arbiter resolves conflicts between cycle requests and cycles in execution, and schedules the inhibited cycle when used in cycle-steal mode.

timing and control block

The timing and control block executes the operational cycle at the request of the arbiter. It provides the DRAM array with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals. It provides the CPU with a RDY signal. It controls the multiplexer during all cycles. It resets the refresh rate generator and decrements the refresh counter during refresh cycles.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (See Note 1)	−1.5 V to 7 V
Input diode current, I_{IK} ($V_I < 0$, $V_I > V_{CC}$)	±20 mA
Output diode current, I_{OK} ($V_O < 0$, $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±35 mA
Continuous current through V_{CC} or GND pins	±70 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: FK or JD package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FN or N package	260°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network ground.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+0.5$	V
V_{IL}	Low-level input voltage	-0.5†		0.8	V
V_O	Output voltage	-0.5		$V_{CC}+0.5$	V
t_t	Input transition (rise and fall) time	0		500	ns
T_A	Operating free-air temperature	0		70	°C

† The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
V_{OH}	High-level output voltage	MA0–MA8, $\overline{RAS0}$–$\overline{RAS3}$, $\overline{CAS0}$–$\overline{CAS1}$	I_{OH} = -20 μA	4.5 V	4.4			4.4		V
			I_{OH} = -6 mA	4.5 V	3.86			3.76		
		RDY	I_{OH} = -20 μA	4.5 V	4.4			4.4		
			I_{OH} = -4 mA	4.5 V	3.86			3.76		
		$\overline{REFREQ}$	I_{OH} = -20 μA	4.5 V	4			3.8		
V_{OL}	Low-level output voltage	RDY, $\overline{REFREQ}$	I_{OL} = 20 μA	4.5 V			0.1		0.1	V
			I_{OL} = 4 mA	4.5 V			0.32		0.37	
		MA0–MA8, $\overline{RAS0}$–$\overline{RAS3}$, $\overline{CAS0}$, $\overline{CAS1}$	I_{OL} = 20 μA	4.5 V			0.1		0.1	
			I_{OL} = 6 mA	4.5 V			0.32		0.37	
I_{IH}	High-level input current except $\overline{REFREQ}$		V_I = 5.5 V	5.5 V			0.1		1	μA
I_{IL}	Low-level input current	$\overline{REFREQ}$	V_I = 0	5.5 V			-5		-50	μA
		$\overline{RESET}$					-100		-250	
		All others					-0.1		-1	
I_{OZ}‡	Off-state output current (3-state outputs only)		V_O = 0 to 5.5 V	5.5 V			±5		±50	μA
I_{CC}	Supply current		V_I = V_{CC} or 0, I_O = 0	5.5 V			5		15	mA
ΔI_{CC}§	Supply current change		One input at 0.5 V or 2.4 V, Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3	mA
C_i	Input capacitance		V_I = 0, f = 1 MHz	5.5 V		5	10		10	pF

‡ This parameter, I_{OZ}, the high impedance-state output current, applies only for three-state outputs and transceiver I/O pins.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		THCT4502B-115		UNIT
		MIN	MAX	
$t_{c(C)}$	CLK cycle time	100		ns
$t_{w(CH)}$	CLK high pulse duration	45		ns
$t_{w(CL)}$	CLK low pulse duration	45		ns
t_{AEL-CL}	Time delay, ALE low to CLK starting low (see Note 1)	15		ns
t_{CL-AEL}	Time delay, CLK low to ALE starting low (see Note 1)	15		ns
t_{CL-AEH}	Time delay, CLK low to ALE	15		ns
$t_{w(AEH)}$	Pulse width ALE high	45		ns
t_{AV-AEL}	Time delay, address RENO, REN1, $\overline{CS}$ valid to ALE low	10		ns
t_{AEL-AX}	Time delay, ALE low to address not valid	15		ns
$t_{AEL-ACL}$	Time delay, ALE low to $\overline{ACX}$ low (see Notes 3, 4, 5, and 6)	$t_{h(RA)}+30$		ns
t_{ACH-CL}	Time delay, $\overline{ACX}$ high to CLK low (see Notes 3 and 7)	30		ns
t_{ACL-CH}	Time delay, $\overline{ACX}$ low to CLK starting high (to remove RDY)	30		ns
t_{RQL-CL}	Time delay, $\overline{REFREQ}$ low to CLK starting low (see Note 8)	35		ns
$t_{w(RQL)}$	Pulse width $\overline{REFREQ}$ low	30		ns
$t_{w(ACL)}$	$\overline{ACX}$ low width (see Note 9)	120		ns
t_{reset}	Power-up reset	$4t_{cCLK}$		ns

NOTES:
1. Coincidence of the trailing edge of CLK and the trailing edge of ALE should be avoided as the refresh/access occurs on the trailing CLK edge.
2. If ALE rises before $\overline{ACX}$ and a refresh request is present, the falling edge of CLK after t_{CL-AEH} will output the refresh address to MA0-MA7 and initiate a refresh cycle.
3. These specifications relate to system timing and do not directly reflect device performance.
4. On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ low depends on the relative occurrence of ALE low to $\overline{ACX}$ low. If $\overline{ACX}$ occurs prior to or coincident with ALE, then $\overline{CAS}$ is timed from the CLK high transition that causes $\overline{RAS}$ low. If $\overline{ACX}$ occurs 20 ns or more after ALE, then $\overline{CAS}$ is timed from the CLK low transition following the CLK high transition causing $\overline{RAS}$ low.
5. For maximum speed access (internal delays on both access and access grant cycles), $\overline{ACX}$ should occur prior to or coincident with ALE.
6. $t_{h(RA)}$ is the dynamic memory row address hold time. $\overline{ACX}$ should follow ALE by $t_{AEL-CEL}$ in systems where the required $t_{h(RA)}$ is greater than $t_{REL-MAX}$ minimum.
7. The minimum of 30 ns is specified to ensure arbitration will occur on falling CLK edge, t_{ACH-CL} also affects precharge time such that the minimum t_{ACH-CL} should be equal or greater than: $t_{w(RH)} - t_{w(CL)} + 30$ ns (for a cycle where $\overline{ACX}$ high occurs prior to ALE high) where $t_{w(RH)}$ is the DRAM $\overline{RAS}$ precharge time.
8. This parameter is necessary only if refresh arbitration is to occur on this low-going CLK edge (in systems where refresh is synchronized to external events).
9. The specification $t_{w(ACL)}$ is designed to allow a $\overline{CAS}$ pulse. This assures normal operation of the device in testing and system operation.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS	THCT4502B-115		UNIT
			MIN	MAX	
$t_{AEL-REL}$	Time delay, ALE low to $\overline{RAS}$ starting low	C_L = 180 pF		35	ns
$t_{RAV-MAV}$	Time delay, row address valid to memory address valid	C_L = 360 pF		42	ns
$t_{AEH-MAV}$	Time delay, ALE high to valid memory address	C_L = 360 pF		60	ns
$t_{AEL-RYL}$	Time delay, ALE to RDY starting low (TWST = 1 or refresh in progress)	C_L = 40 pF		33	ns
$t_{AEL-CEL}$	Time delay, ALE low to $\overline{CAS}$ starting low (see Note 10)	C_L = 360 pF	50	115	ns
$t_{AEH-REH}$	Time delay, ALE high to $\overline{RAS}$ starting high	C_L = 180 pF		35	ns
$t_{ACL-MAX}$	Row address valid after $\overline{ACX}$	C_L = 360 pF	10		ns
$t_{MAV-CEL}$	Time delay, memory address valid to $\overline{CAS}$ starting low	C_L = 360 pF	0		ns
$t_{ACL-CEL}$	Time delay, $\overline{ACX}$ low to $\overline{CAS}$ starting low (see Note 10)	C_L = 360 pF	25	80	ns
$t_{ACH-REH}$	Time delay, $\overline{ACX}$ to $\overline{RAS}$ starting high	C_L = 180 pF		40	ns
$t_{ACH-CEH}$	Time delay, $\overline{ACX}$ high to $\overline{CAS}$ starting high	C_L = 360 pF	5	30	ns
$t_{ACH-MAX}$	Column address valid after $\overline{ACX}$ high	C_L = 360 pF	5		ns
t_{CH-RYH}	Time delay, CLK high to RDY starting high (after $\overline{ACX}$ low) (see Note 11)	C_L = 40 pF		42	ns
$t_{RFL-RFL}$	Time delay, $\overline{REFREQ}$ external till supported by $\overline{REFREQ}$ internal	C_L = 40 pF		35	ns
t_{CH-RFL}	Time delay, CLK high till $\overline{REFREQ}$ internal starting low	C_L = 40 pF		50	ns
t_{CL-MAV}	Time delay, CLK low till refresh address valid	C_L = 360 pF		70	ns
t_{CH-RRL}	Time delay, CLK high till refresh $\overline{RAS}$ starting low	C_L = 180 pF	5	50	ns
$t_{MAV-RRL}$	Time delay, refresh address valid till refresh $\overline{RAS}$ low	C_L = 180 pF	5		ns
t_{CL-RFH}	Time delay, CLK low to $\overline{REFREQ}$ starting high (3 cycle refresh)	C_L = 40 pF		50	ns
t_{CH-RFH}	Time delay, CLK high to $\overline{REFREQ}$ starting high (4 cycle refresh)	C_L = 40 pF		50	ns
t_{CH-RRH}	Time delay, CLK high to refresh $\overline{RAS}$ starting high	C_L = 180 pF	5	30	ns
t_{CH-MAX}	Refresh address valid after CLK high	C_L = 360 pF	10		ns

NOTES: 10. The falling edge of $\overline{CAS}$ occurs when both ALE low to $\overline{CAS}$ low time delay ($t_{AEL-CEL}$) and $\overline{ACX}$ low to $\overline{CAS}$ low time delay ($t_{ACL-CEL}$) have elapsed, i.e., if $\overline{ACX}$ goes low prior to ($t_{AEL-CEL} - t_{ACL-CEL}$) after the falling edge of ALE, the falling edge of $\overline{CAS}$ is measured from the falling edge of ALE ($t_{AEL-CEL}$). Otherwise, the access time increases and the falling edge of $\overline{CAS}$ is measured from the falling edge of $\overline{ACX}$ ($t_{ACL-CEL}$).

11. RDY returns high on the rising edge of CLK. If TWST = 0, then on an access grant cycle RDY goes high on the same edge that causes access $\overline{RAS}$ low. If TWST = 1, then RDY goes to the high level on the first rising CLK edge after $\overline{ACX}$ goes low on access cycles and on the next rising edge after the edge that causes access $\overline{RAS}$ low on access grant cycles (assuming $\overline{ACX}$ low).

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1) (continued)

PARAMETER		TEST CONDITIONS	THCT4502B-115		UNIT
			MIN	MAX	
$t_{CH\text{-}REL}$	Time delay, CLK high till access $\overline{RAS}$ starting low	C_L = 180 pF		45	ns
$t_{CL\text{-}CEL}$	Time delay, CLK low to access $\overline{CAS}$ starting low (see Note 12)	C_L = 360 pF		70	ns
$t_{CL\text{-}MAX}$	Row address valid after CLK low	C_L = 360 pF	15		ns
$t_{REL\text{-}MAX}$	Row address valid after $\overline{RAS}$ low	C_L = 360 pF	20		ns
$t_{AEH\text{-}MAX}$	Column address valid after ALE high	C_L = 360 pF	10		ns
t_{dis}	Output disable time (3-state outputs)	C_L = 360 pF		90	ns
t_{en}	Output enable time (3-state outputs)	C_L = 360 pF		55	ns
$t_{CAV\text{-}CEL}$	Time delay, column address valid to $\overline{CAS}$ starting low after refresh (see Note 12)	C_L = 360 pF	0		ns
$t_{CH\text{-}CEL}$	Time delay, CLK high to access $\overline{CAS}$ starting low (see Note 13)	C_L = 360 pF		140	ns
$t_{t(CEL)}$	$\overline{CAS}$ fall time	C_L = 360 pF		20	ns
$t_{t(CEH)}$	$\overline{CAS}$ rise time	C_L = 360 pF		30	ns
$t_{t(REL)}$	$\overline{RAS}$ fall time	C_L = 180 pF		20	ns
$t_{t(REH)}$	$\overline{RAS}$ rise time	C_L = 180 pF		30	ns
$t_{t(MAV)}$	Address transition time	C_L = 360 pF		30	ns
$t_{t(RYL)}$	RDY fall time	C_L = 40 pF		20	ns
$t_{t(RYH)}$	RDY rise time	C_L = 40 pF		27	ns

NOTES: 12. The occurrence of $\overline{CAS}$ low is guaranteed not to occur until the column address is valid on MAX.

13. On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ low depends on the relative occurrence of ALE low to $\overline{ACX}$ low. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK high transition that causes $\overline{RAS}$ low. If $\overline{ACX}$ occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK low transition following the CLK high transition causing $\overline{RAS}$ low. (See Refresh Cycle Timing Diagram)

PARAMETER MEASUREMENT INFORMATION

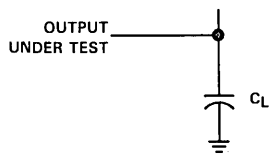
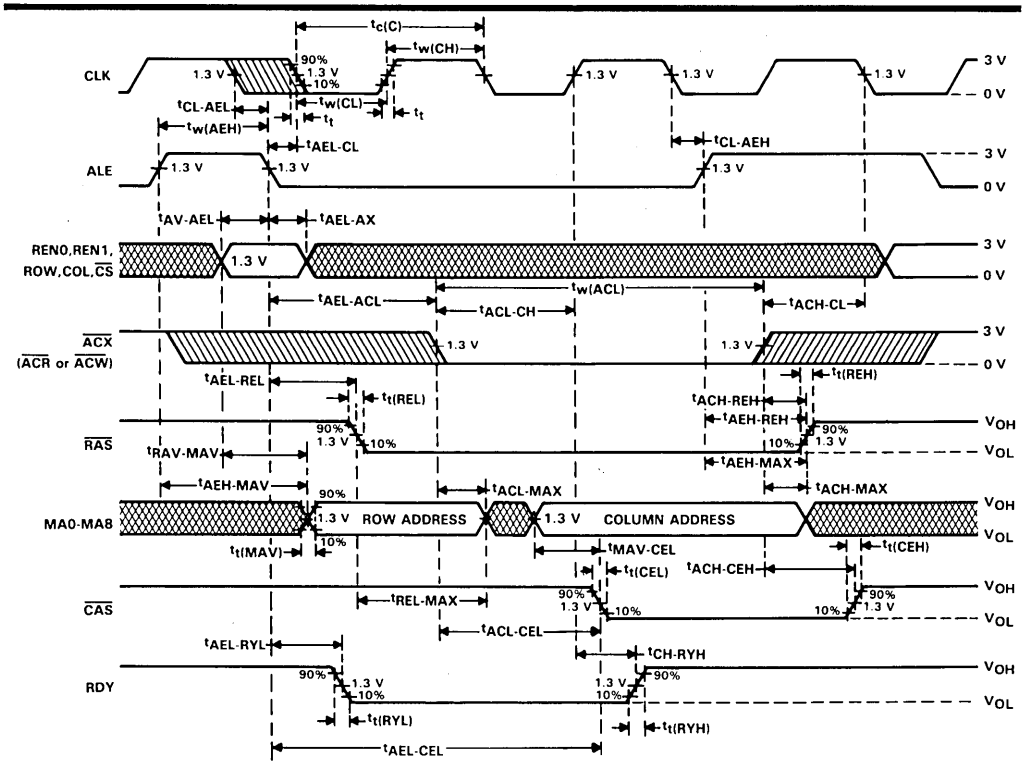


FIGURE 1. LOAD CIRCUIT



NOTE 14: All transition times (t_t) are measured between 10% and 90% points.

FIGURE 2. ACCESS CYCLE TIMING

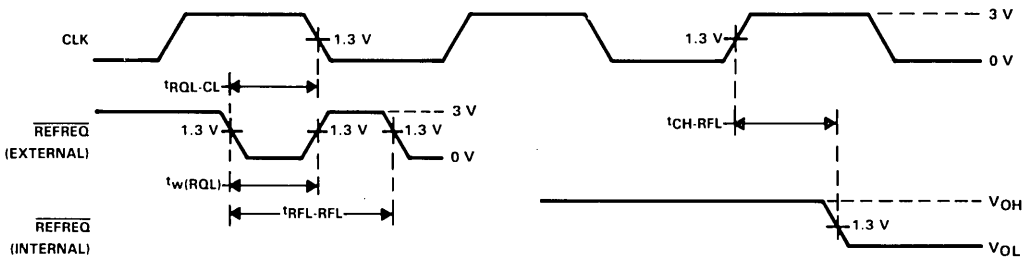


FIGURE 3. REFRESH REQUEST TIMING

NOTE 15: All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50 Ω, t_r = 6 ns, t_f = 6 ns.

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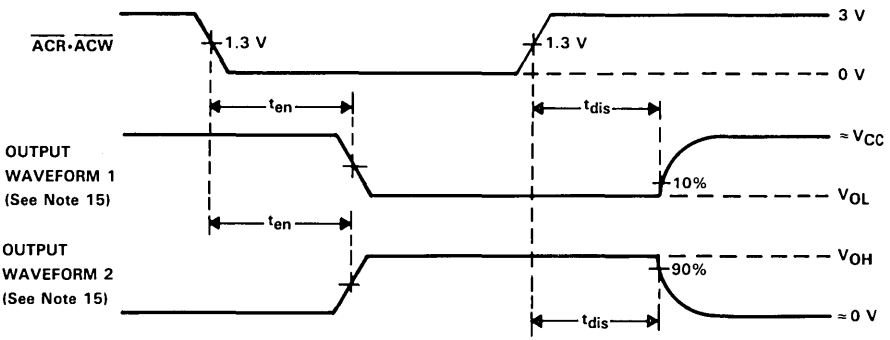
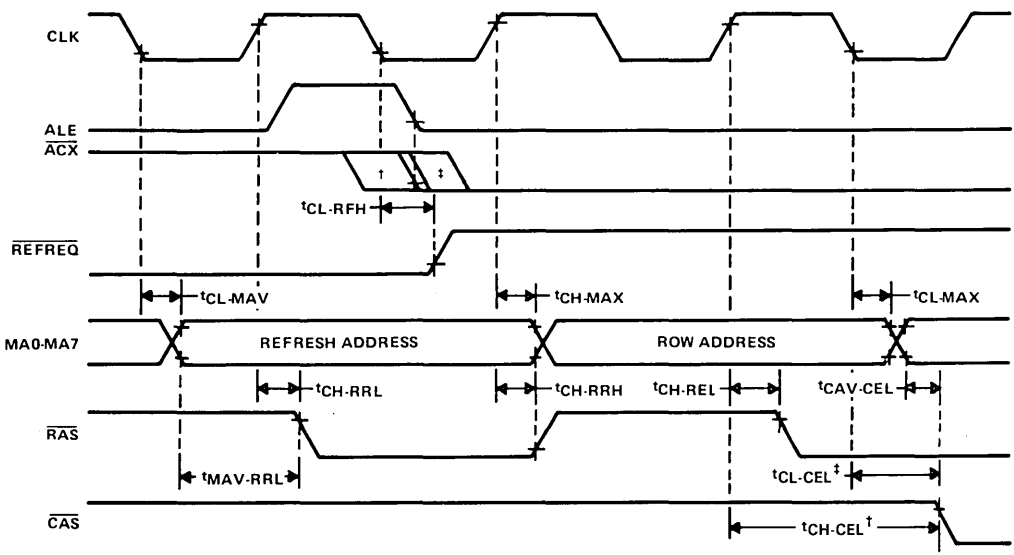


VOLTAGE WAVEFORMS

NOTE 16: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the access controls. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the access controls.

FIGURE 4. ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

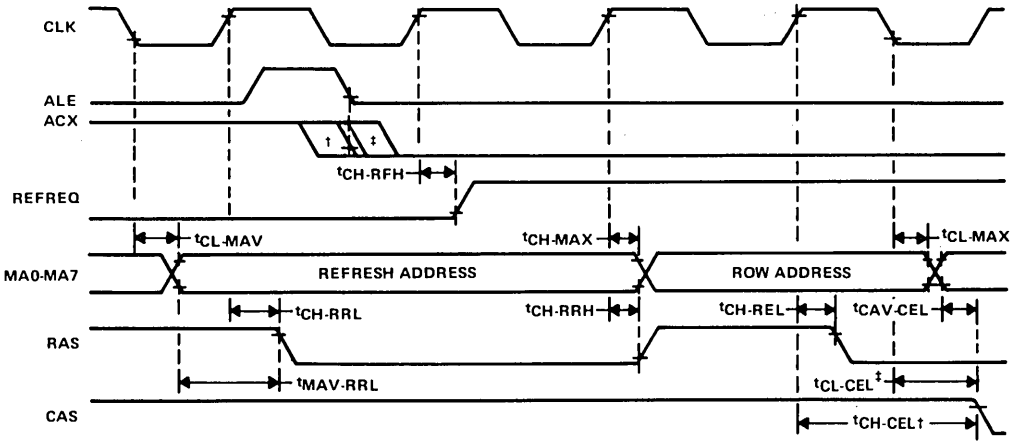


† On access grant cycle following refresh, $\overline{CAS}$ low and address multiplexing are timed from CLK high transition ($t_{CH\text{-}CEL}$) if $\overline{ACX}$ low occurs prior to or coincident with the falling edge of ALE.

‡ On access grant cycle following refresh, $\overline{CAS}$ low and address multiplexing are timed from CLK low transition ($t_{CL\text{-}CEL}$) if $\overline{ACX}$ low occurs 20 ns or more after the falling edge of ALE.

FIGURE 5. REFRESH CYCLE TIMING (THREE CYCLE)

NOTE 15: All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50 Ω, t_r = 6 ns, t_f = 6 ns.



† On access grant cycle following refresh, $\overline{CAS}$ low and address multiplexing are timed from CLK high transition (t_{CH-CEL}) if $\overline{ACX}$ low occurs prior to or coincident with the falling edge of ALE.

‡ On access grant cycle following refresh, $\overline{CAS}$ low and address multiplexing are timed from CLK low transition (t_{CL-CEL}) if $\overline{ACX}$ low occurs 20 ns or more after the falling edge of ALE.

NOTE 15: All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50 Ω, t_r = 6 ns, t_f = 6 ns.

FIGURE 6. REFRESH CYCLE TIMING (FOUR CYCLE)

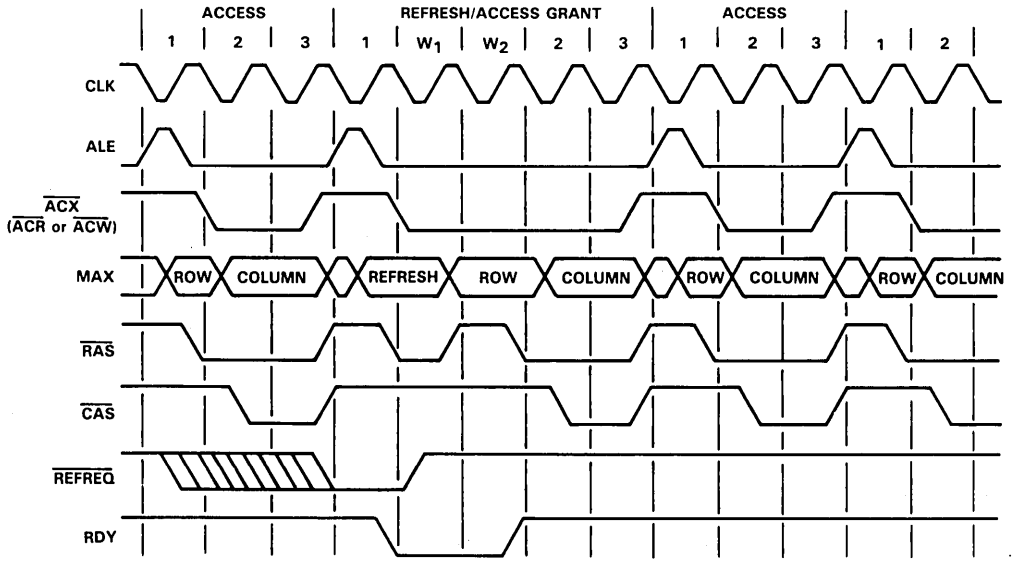


FIGURE 7. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (THREE-CYCLE, TWST IS LOW)

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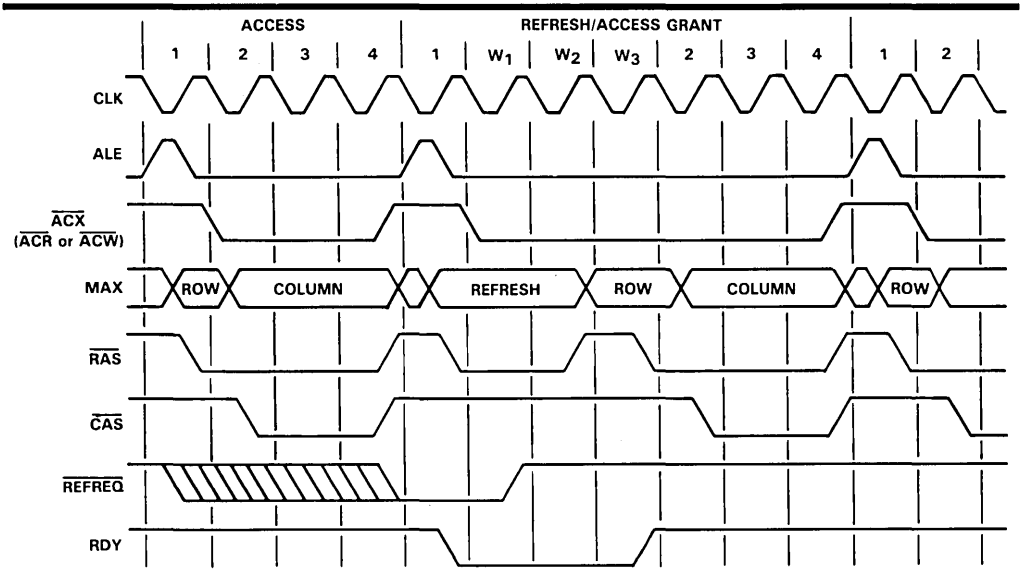


FIGURE 8. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (FOUR-CYCLE, TWST IS LOW)

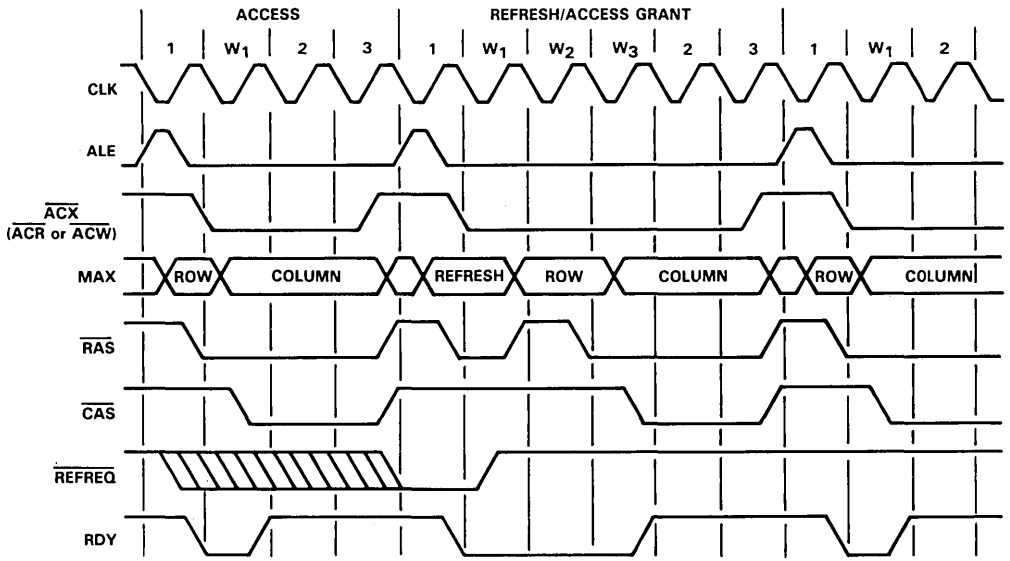


FIGURE 9. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (THREE-CYCLE, TWST IS HIGH)

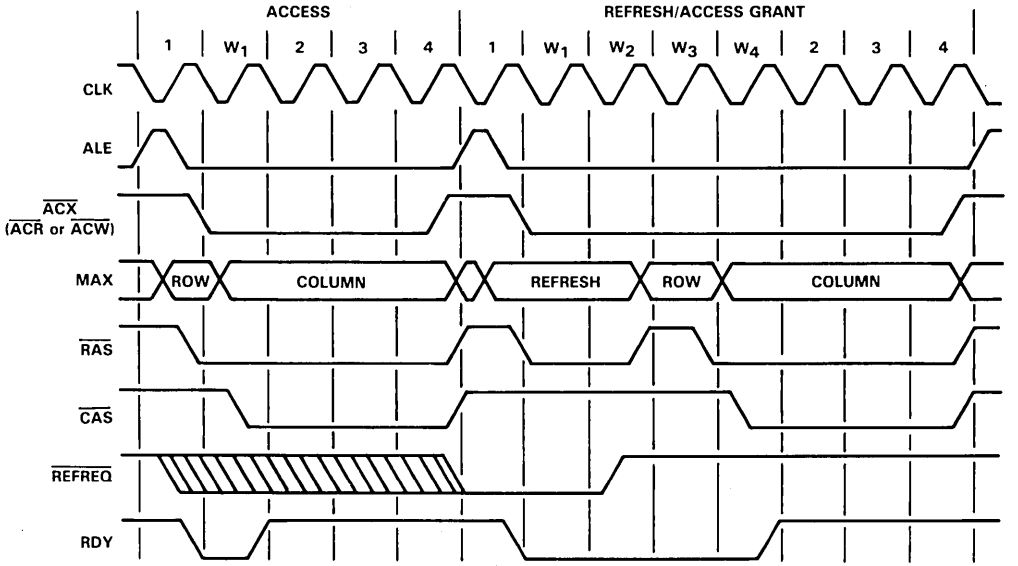
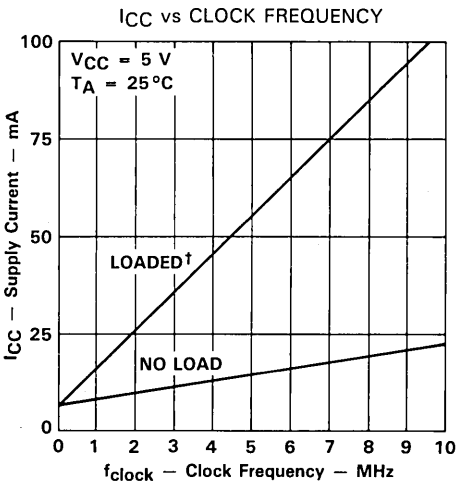


FIGURE 10. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (FOUR-CYCLE, TWST IS HIGH)

TYPICAL CHARACTERISTICS



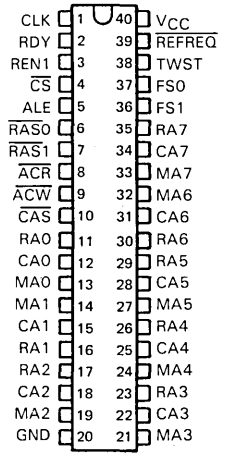
†Load is 360 pF for $\overline{CAS}$ and MA outputs, 180 pF, for all $\overline{RAS}$ outputs.

FIGURE 11

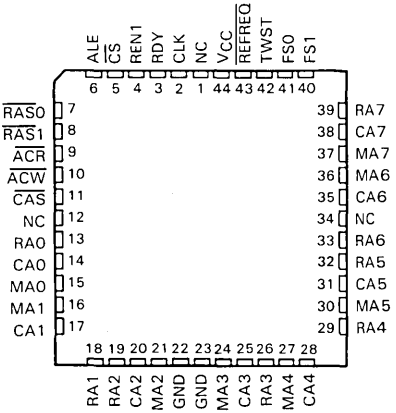
D2674, JANUARY 1982—REVISED AUGUST 1985

- Controls Operation of 8K, 16K, 32K, and 64K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 256K Bytes of Memory Without External Drivers
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
- Strap-Selected Wait-State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (including Multiple Controllers)
- 3-State Outputs Allow Multiport Memory Configuration
- Performance Ranges of 150 ns, 200 ns, or 250 ns

TMS4500A . . . NL PACKAGE
(TOP VIEW)



TMS4500A . . . FN PACKAGE
(TOP VIEW)



description

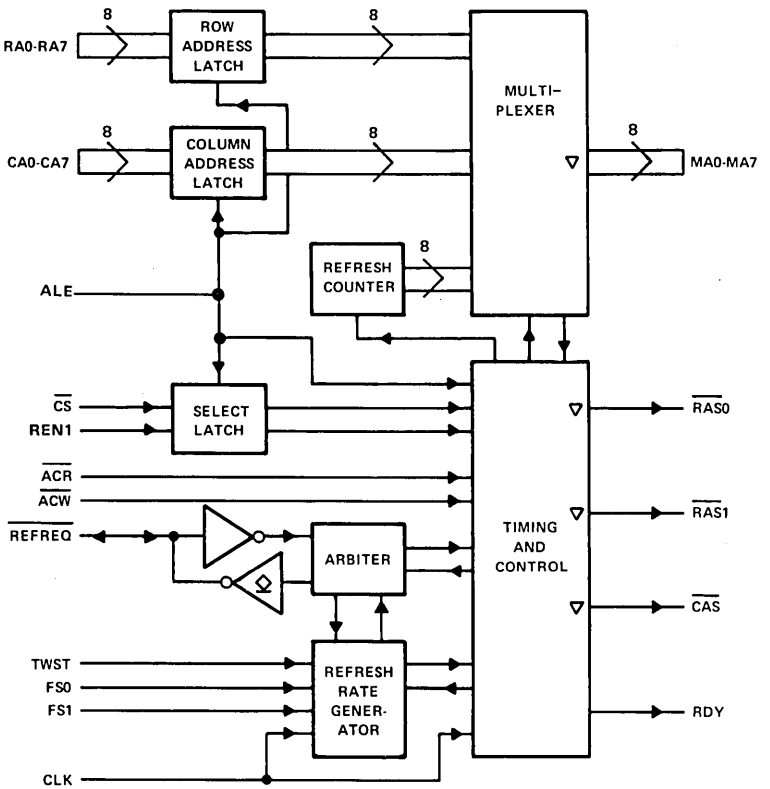
The TMS4500A is a monolithic DRAM system controller designed to provide address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

The controller contains a 16-bit multiplexer that generates the address lines for the memory device from the 16 system address bits and provides the strobe signals required by the memory to decode the address. An 8-bit refresh counter generates the 256-row addresses required for refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention.

The TMS4500A also contains refresh/access arbitration circuitry to resolve conflicts between memory access requests and memory refresh cycles. The TMS4500A is offered in a 40-pin, 600-mil dual-in-line plastic package and 44-pin, 650-mil square plastic chip carrier package. It is characterized for operation from 0°C to 70°C.

BLOCK DIAGRAM



pin descriptions

RA0—RA7	Input	Row Address — These address inputs are used to generate the row address for the multiplexer.
CA0—CA7	Input	Column Address — These address inputs are used to generate the column address for the multiplexer.
MA0—MA7	Output	Memory Address — These three-state outputs are designed to drive the addresses of the dynamic RAM array.
ALE	Input	Address Latch Enable — This input is used to latch the 16 address inputs, $\overline{CS}$ and REN1. This also initiates an access cycle if chip select is valid. The rising edge (low level to high level) of ALE returns $\overline{RAS}$ to the high level.
$\overline{CS}$	Input	Chip Select — A low on this input enables an access cycle. The trailing edge of ALE latches the chip select input.

pin descriptions (continued)

REN1	Input	RAS Enable 1 — This input is used to select one of two banks of RAM via the $\overline{RAS0}$ and $\overline{RAS1}$ outputs when chip select is present. When it is low, $\overline{RAS0}$ is selected; when it is high, $\overline{RAS1}$ is selected.
$\overline{ACR}$, ACW	Input	Access Control, Read; Access Control, Write — A low on either of these inputs causes the column address to appear on MA0—MA7 and the column address strobe. The rising edge of $\overline{ACR}$ or $\overline{ACW}$ terminates the cycle by ending $\overline{RAS}$ and $\overline{CAS}$ strobes. When $\overline{ACR}$ and $\overline{ACW}$ are both low, MA0—MA7, $\overline{RAS0}$, $\overline{RAS1}$, and $\overline{CAS}$ go into a high-impedance (floating) state.
CLK	Input	System Clock — This input provides the master timing to generate refresh cycle timings and refresh rate. Refresh rate is determined by the TWST, FS1, FS0 inputs.
$\overline{REFREQ}$	Input/Output	Refresh Request — (This input should be driven by an open-collector output.) On input, a low-going edge initiates a refresh cycle and will cause the internal refresh timer to be reset on the next falling edge of the CLK. As an output, a low-going edge signals an internal refresh request and that the refresh timer will be reset on the next low-going edge of CLK. $\overline{REFREQ}$ will remain low until the refresh cycle in progress and the current refresh address is present on MA0—MA7. (Note: $\overline{REFREQ}$ contains an internal pull-up resistor with a nominal resistance of 10 kilohms.)
$\overline{RAS0}$, $\overline{RAS1}$	Output	Row Address Strobe — These three-state outputs are used to latch the row address into the bank of DRAMs selected by REN1. On refresh both signals are driven.
$\overline{CAS}$	Output	Column Address Strobe — This three-state output is used to latch the column address into the DRAM array.
RDY	Output	Ready — This totem-pole output synchronizes memories that are too slow to guarantee microprocessor access time requirements. This output is also used to inhibit access cycles during refresh when in cycle-steal mode.
TWST	Input	Timing/Wait Strap — A high on this input indicates a wait state should be added to each memory cycle. In addition it is used in conjunction with FS0 and FS1 to determine refresh rate and timing.
FS0, FS1	Input	Frequency Select 0; Frequency Select 1 — These are strap inputs to select Mode and Frequency of operation as shown in Table 1.

TABLE 1. STRAP CONFIGURATION

STRAP INPUT MODES			WAIT STATES FOR MEMORY ACCESS	REFRESH RATE	MINIMUM CLK FREQ. (MHz)	REFRESH FREQ. (kHz)	CLOCK FOR EACH FOR EACH REFRESH
TWST	FS1	FS0					
L	L	L†	0	EXTERNAL	–	REFREQ	4
L	L	H	0	CLK÷31	1,984	64-95‡	3
L	H	L	0	CLK÷46	2,944	64-85‡	3
L	H	H	0	CLK÷61	3,904	64-82§	4
H	L	L	1	CLK÷46	2,944	64-85‡	3
H	L	H	1	CLK÷61	3,904	64-80‡	4
H	H	L	1	CLK÷76	4,864	64-77‡	4
H	H	H	1	CLK÷91	5,824	64-88¶	4

† This strap configuration resets the Refresh Timer circuitry.
‡ The highest frequency in the refresh frequency column is the frequency that is produced if the minimum CLK frequency of the next select state is used.
§ The highest frequency in the refresh column is the refresh frequency if the CLK frequency is 5 MHz.
¶ The highest frequency in the refresh column is the refresh frequency if the CLK frequency is 8 MHz.

functional description

TMS4500A consists of six basic blocks; address and select latches, refresh rate generator, refresh counter, the multiplexer, the arbiter, and timing and control block.

address and select latches

The address and select latches allow the DRAM controller to be used in systems that multiplex address and data on the same lines without external latches. The row address latches are transparent, meaning that while ALE is high, the output at MA0—MA7 follows the inputs RA0—RA7.

refresh rate generator

The refresh rate generator is a counter that indicates to the arbiter that it is time for a refresh cycle. The counter divides the clock frequency according to the configuration straps as shown in Table 1. The counter is reset when a refresh cycle is requested or when TWST, FS1 and FS0 are low. The configuration straps allow the matching of memories to the system access time.

Upon Power-Up it is necessary to provide a reset signal by driving all three straps to the controller low to initialize internal counters. A system's low-active, power-on reset ($\overline{\text{RESET}}$) can be used to accomplish this by connecting it to those straps that are desired high during operation. During this reset period, at least four clock cycles should occur.

refresh counter

The refresh counter contains the address of the row to be refreshed. The counter is decremented after each refresh cycle. [A low-to-high transition on TWST sets the refresh counter to FF_{16} (255_{10}).]

multiplexer

The multiplexer provides the DRAM array with row, column, and refresh addresses at the proper times. Its inputs are the address latches and the refresh counter. The outputs provide up to 16 multiplexed addresses on eight lines.

arbiter

The arbiter provides two operational cycles: access and refresh. The arbiter resolves conflicts between cycle requests and cycles in execution, and schedules the inhibited cycle when used in cycle-steal mode.

timing and control block

The timing and control block executes the operational cycle at the request of the arbiter. It provides the DRAM array with $\overline{RAS}$ and $\overline{CAS}$ signals. It provides the CPU with a RDY signal. It controls the multiplexer during all cycles. It resets the refresh rate generator and decrements the refresh counter during refresh cycles.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −1.5 V to 7 V
Input voltage range (any input) . . . . . −1.5 V to 7 V
Continuous power dissipation . . . . . 1.2 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to the ground terminal.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2.4		6	V
Low-level input voltage, V_{IL}	−1‡		0.8	V
High-level output current, I_{OH}			−1	mA
Low-level output current, I_{OL}			4	mA
Short-circuit output current, I_{OS}§			−50	mA
Operating free-air temperature, T_A	0		70	°C

‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

§ Not more than one output should be shorted at a time.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP¶	MAX	UNIT
V_{OH}	High-level output voltage	MA0-MA7, RDY	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4			V
		$\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS}$			2.7			
		$\overline{REFREQ}$	V_{CC} = 4.5 V,	I_{OH} = −100 μA	2.4			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	I_{OL} = 4 mA			0.4	V
I_{IH}	High-level input current except $\overline{REFREQ}$		V_I = 5.5 V				10	μA
I_{IL}	Low-level input current	$\overline{REFREQ}$	V_I = 0				−1.25	mA
		All others					−10	μA
I_{OZ}	Off-state output current		V_{CC} = 5.5 V,	V_O = 0 to 4.5 V			±50	μA
I_{CC}	Operating supply current		T_A = 0°C			100	140	mA
C_i	Input capacitance		V_I = 0,	f = 1 MHz		5		pF
C_o	Output capacitance		V_O = 0,	f = 1 MHz		6		pF

¶ All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended supply voltage range and operating free-air temperature (unless otherwise noted)

PARAMETER		TMS4500A-15		TMS4500A-20		TMS4500A-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(C)}$	CLK cycle time	100		120		140		ns
$t_{w(CH)}$	CLK high pulse duration	40		40		40		
$t_{w(CL)}$	CLK low pulse duration	40		45		45		
t_t	Transition time, all inputs		50		50		50	
t_{AEL-CL}	Time delay, ALE low to CLK starting low (see Note 1)	10		10		15		
t_{CL-AEL}	Time delay, CLK low to ALE starting low (see Note 1)	10		10		15		
t_{CL-AEH}	Time delay, CLK low to ALE starting high (see Note 2)	15		20		20		
$t_{w(AEH)}$	Pulse duration, ALE high	50		60		60		
t_{AV-AEL}	Time delay, address REN1, $\overline{CS}$ valid to ALE low	5		10		15		
t_{AEL-AX}	Time delay, ALE low to address not valid	10		10		10		
$t_{AEL-ACL}$	Time delay, ALE low to $\overline{ACX}$ low (see Notes 3, 4, 5, and 6)	$t_{h(RA)}+30$		$t_{h(RA)}+40$		$t_{h(RA)}+50$		
t_{ACH-CL}	Time delay, $\overline{ACX}$ high to CLK low (see Notes 3 and 7)	20		20		20		
t_{ACL-CH}	Time delay, $\overline{ACX}$ low to CLK starting high (to remove RDY)	30		30		30		
t_{RQL-CL}	Time delay, $\overline{REFREQ}$ low to CLK starting low (see Note 8)	20		20		20		
$t_{w(RQL)}$	Pulse duration, $\overline{REFREQ}$ low	20		20		20		
$t_{w(ACL)}$	$\overline{ACX}$ low duration (see Note 9)	110		140		175		

NOTES:
1. Coincidence of the trailing edge of CLK and the trailing edge of ALE should be avoided as the refresh/access occurs on the trailing CLK edge. A trailing edge of CLK should occur during the interval from $\overline{ACX}$ high to ALE low.
2. If ALE rises before $\overline{ACX}$ and a refresh request is present, the falling edge of CLK after t_{CL-AEH} will output the refresh address to MA0-MA7 and initiate a refresh cycle.
3. These specifications relate to system timing and do not directly reflect device performance.
4. On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ low depends on the relative occurrence of ALE low to $\overline{ACX}$ low. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK high transition that causes $\overline{RAS}$ low. If $\overline{ACX}$ occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK low transition following the CLK high transition causing $\overline{RAS}$ low.
5. For maximum speed access (internal delays on both access and access grant cycles), $\overline{ACX}$ should occur prior to or coincident with ALE.
6. $t_{h(RA)}$ is the dynamic memory row address hold time. $\overline{ACX}$ should follow ALE by $t_{AEL-CEL}$ in systems where the required $t_{h(RA)}$ is greater than $t_{REL-MAX}$ minimum.
7. The minimum of 20 ns is specified to ensure arbitration will occur on falling CLK edge, t_{ACH-CL} also affects precharge time such that the minimum t_{ACH-CL} should be equal or greater than: $t_{w(RH)} - t_{w(CL)} + 30$ ns (for a cycle where $\overline{ACX}$ high occurs prior to ALE high) where $t_{w(RH)}$ is the DRAM $\overline{RAS}$ precharge time.
8. This parameter is necessary only if refresh arbitration is to occur on this low-going CLK edge (in systems where refresh is synchronized to external events).
9. The specification $t_{w(ACL)}$ is designed to allow a $\overline{CAS}$ pulse. This assures normal operation of the device in testing and system operation.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS	TMS4500A-15		TMS4500A-20		TMS4500A-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{AEL-REL}$	Time delay, ALE low to $\overline{RAS}$ starting low	C_L = 160 pF		35		40		50	ns
$t_{RAV-MAV}$	Time delay, row address valid to memory address valid	C_L = 160 pF		45		50		60	ns
$t_{AEH-MAV}$	Time delay, ALE high to valid memory address	C_L = 160 pF		65		75		90	ns
$t_{AEL-RYL}$	Time delay, ALE to RDY starting low (TWST = 1 or refresh in progress)	C_L = 40 pF		40		40		40	ns
$t_{AEL-CEL}$	Time delay, ALE low to $\overline{CAS}$ starting low (see Note 10)	C_L = 160 pF	60	150	70	200	80	250	ns
$t_{AEH-REH}$	Time delay, ALE high to $\overline{RAS}$ starting high	C_L = 160 pF		30		30		40	ns
$t_{ACL-MAX}$	Row address valid after $\overline{ACX}$ low	C_L = 160 pF	15		20		25		ns
$t_{MAV-CEL}$	Time delay, memory address valid to $\overline{CAS}$ starting low	C_L = 160 pF	0		0		0		ns
$t_{ACL-CEL}$	Time delay, $\overline{ACX}$ low to $\overline{CAS}$ starting low (see Note 10)	C_L = 160 pF	40	100	45	130	50	165	ns
$t_{ACH-REH}$	Time delay, $\overline{ACX}$ to $\overline{RAS}$ starting high	C_L = 160 pF		30		40		50	ns
$t_{ACH-CEH}$	Time delay, $\overline{ACX}$ high to $\overline{CAS}$ starting high	C_L = 160 pF	5	30	10	40	15	50	ns
$t_{ACH-MAX}$	Column address valid after $\overline{ACX}$ high	C_L = 160 pF	10		15		15		ns
t_{CH-RYH}	Time delay, CLK high to RDY starting high (after $\overline{ACX}$ low) (see Note 11)	C_L = 40 pF		40		45		60	ns
$t_{RFL-RFL}$	Time delay, $\overline{REFREQ}$ external till supported by $\overline{REFREQ}$ internal	C_L = 40 pF		30		35		35	ns
t_{CH-RFL}	Time delay, CLK high till $\overline{REFREQ}$ internal starting low	C_L = 40 pF		30		35		45	ns
t_{CL-MAV}	Time delay, CLK low till refresh address valid	C_L = 160 pF		75		100		125	ns
t_{CH-RRL}	Time delay, CLK high till refresh $\overline{RAS}$ starting low	C_L = 160 pF	10	50	15	60	20	80	ns
$t_{MAV-RRL}$	Time delay, refresh address valid till refresh $\overline{RAS}$ low	C_L = 160 pF	5		5		5		ns
t_{CL-RFH}	Time delay, CLK low to $\overline{REFREQ}$ starting high (3 cycle refresh)	C_L = 160 pF		50		55		75	ns
t_{CH-RFH}	Time delay, CLK high to $\overline{REFREQ}$ starting high (4 cycle refresh)	C_L = 160 pF		50		55		75	ns
t_{CH-RRH}	Time delay, CLK high to refresh $\overline{RAS}$ starting high	C_L = 160 pF	5	35	10	45	10	60	ns
t_{CH-MAX}	Refresh address valid after CLK high	C_L = 160 pF	15		20		25		ns

NOTES: 10. The falling edge of $\overline{CAS}$ occurs when both ALE low to $\overline{CAS}$ low time delay ($t_{AEL-CEL}$) and $\overline{ACX}$ low to $\overline{CAS}$ low time delay ($t_{ACL-CEL}$) have elapsed, i.e., if $\overline{ACX}$ goes low prior to ($t_{AEL-CEL} - t_{ACL-CEL}$) after the falling edge of ALE, the falling edge of $\overline{CAS}$ is measured from the falling edge of ALE ($t_{AEL-CEL}$). Otherwise, the access time increases and the falling edge of $\overline{CAS}$ is measured from the falling edge of $\overline{ACX}$ ($t_{ACL-CEL}$).

11. RDY returns high on the rising edge of CLK. If TWST = 0, then on an access grant cycle RDY goes high on the same edge that causes access $\overline{RAS}$ low. If TWST = 1, then RDY goes to the high level on the first rising CLK edge after $\overline{ACX}$ goes low on access cycles and on the next rising edge after the edge that causes access $\overline{RAS}$ low on access grant cycles (assuming $\overline{ACX}$ low).

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1) (continued)

PARAMETER		TEST CONDITIONS	TMS4500A-15		TMS4500A-20		TMS4500A-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CH-REL}	Time delay, CLK high till access $\overline{RAS}$ starting low	C_L = 160 pF		60		70		95	ns
t_{CL-CEL}	Time delay, CLK low to access $\overline{CAS}$ starting low (see Note 12)			125		140		185	
t_{CL-MAX}	Row address valid after CLK low		25		30		40		
$t_{REL-MAX}$	Row address valid after $\overline{RAS}$ low		25		30		35		
$t_{AEH-MAX}$	Column address valid after ALE high	C_L = 160 pF	10		15		20		
t_{dis}	Output disable time (3-state outputs)			100		125		165	
t_{en}	Output enable time (3-state outputs)			75		80		105	
$t_{CAV-CEL}$	Time delay, column address valid to $\overline{CAS}$ starting low after refresh		0		0		0		
t_{CH-CEL}	Time delay, CLK high to access $\overline{CAS}$ starting low (see Note 12)			180		200		235	
t_{ACL-CL}	$\overline{ACX}$ low to CLK starting low	C_L = 40 pF	25		35		45		
$t_{ACL-RYH}$	$\overline{ACX}$ low to RDY starting high	C_L = 40 pF		40		50		60	
t_{CL-ACL}	CLK low to $\overline{ACX}$ starting low	C_L = 40 pF	0		0		0		
$t_{t(CEL)}$	$\overline{CAS}$ fall time	C_L = 320 pF		15		20		25	
$t_{t(CEH)}$	$\overline{CAS}$ rise time			30		35		45	
$t_{t(REL)}$	$\overline{RAS}$ fall time	C_L = 160 pF		15		20		25	
$t_{t(REH)}$	$\overline{RAS}$ rise time			15		20		25	
$t_{t(MAV)}$	Address transition time			20		20		25	
$t_{t(RYL)}$	RDY fall time	C_L = 40 pF		10		15		20	
$t_{t(RYH)}$	RDY rise time			20		25		35	

NOTE 12: On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ low depends on the relative occurrence of ALE low to $\overline{ACX}$ low. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK high transition that causes $\overline{RAS}$ low. If $\overline{ACX}$ occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK low transition following the CLK high transition causing $\overline{RAS}$ low. (See Refresh Cycle Timing Diagram)

PARAMETER MEASUREMENT INFORMATION

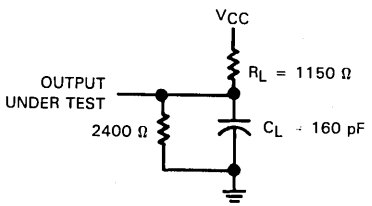
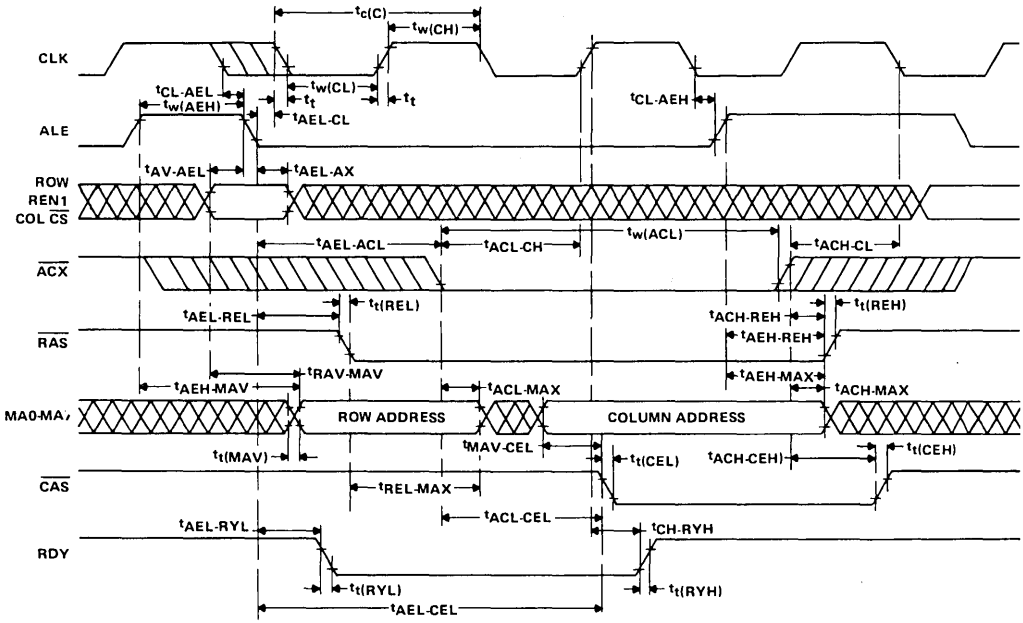
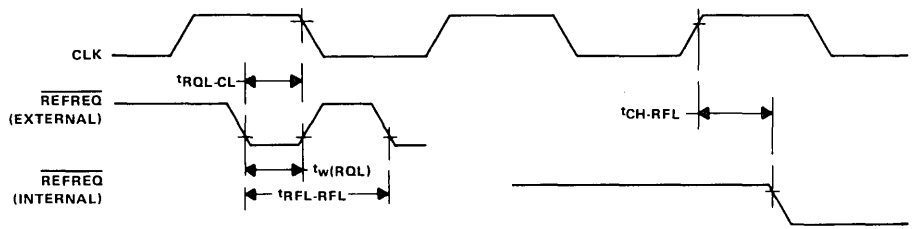


FIGURE 1 – LOAD CIRCUIT

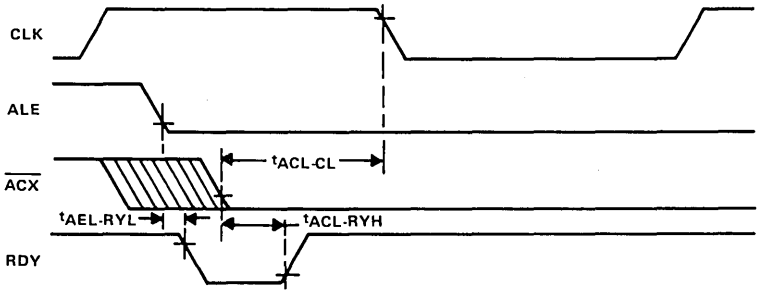
access cycle timing



refresh request timing

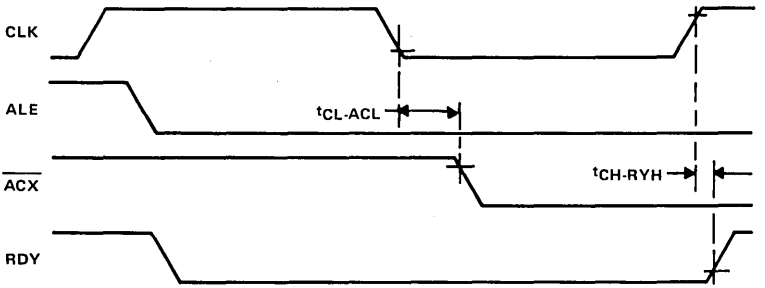


ready timing (ACX during CLK high) (see notes 13 thru 16)



RDY starting high is timed from $\overline{ACX}$ low ($t_{ACL-RYH}$) for the condition $\overline{ACX}$ going low while CLK high.

ready timing (ACX during CLK low) (see notes 13 thru 16)



RDY starting high is timed from CLK high (t_{CH-RYH}) for the condition ACX going low while CLK low.

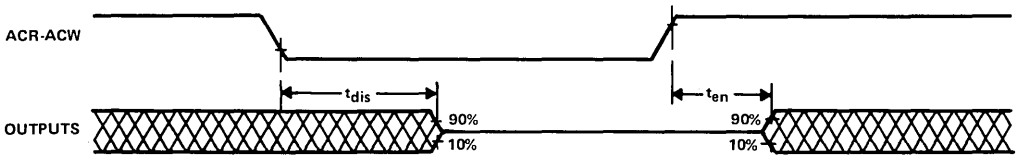
NOTES: 13. For RDY high transition (during normal access) to be timed from the rising edge of CLK, $\overline{ACX}$ must occur t_{CL-ACL} after the falling edge of CLK.

14. For $\overline{ACX}$ prior to the falling edge of CLK by t_{ACL-CL}, the RDY high transition will be $t_{ACL-RYH}$.

15. t_{ACL-CL} is a limiting parameter for control of RDY to be dependent upon $\overline{ACX}$ low.

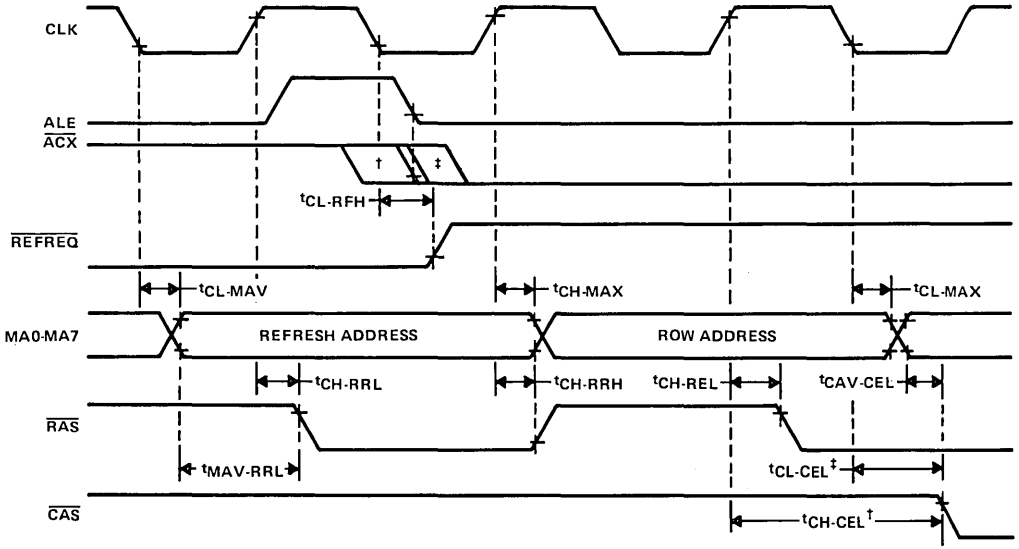
16. During the interval for t_{ACL-CL} < MINIMUM to t_{CL-ACL} > MINIMUM, the control of RDY may vary between the rising clock edge or falling edge of $\overline{ACX}$.

output 3-state timing

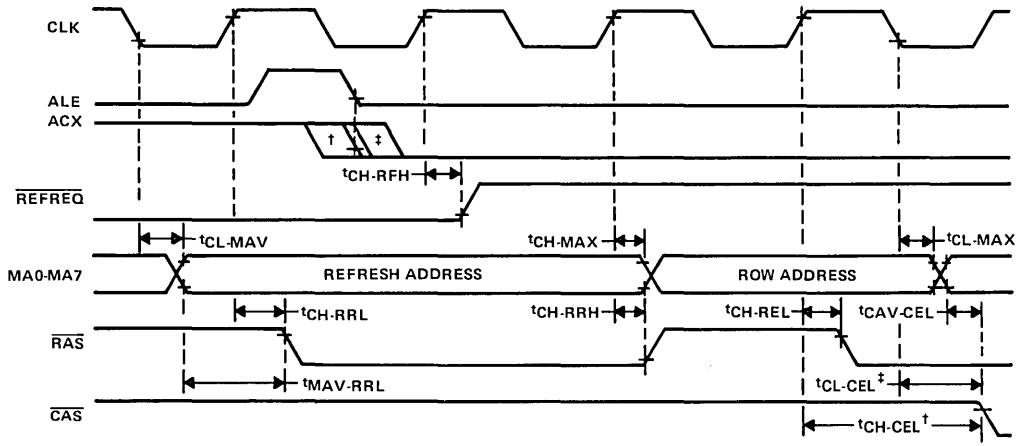


TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

refresh cycle timing (three-cycle)



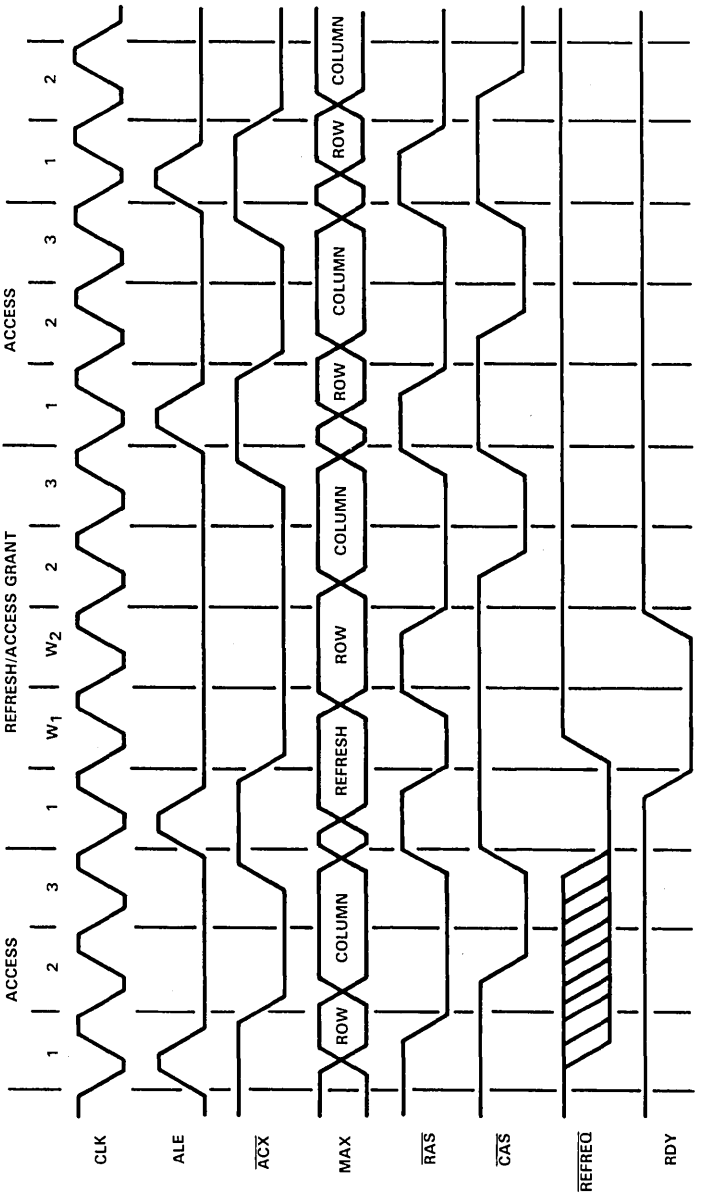
refresh cycle timing (four-cycle)



† On access grant cycle following refresh, $\overline{CAS}$ low and address multiplexing are timed from CLK high transition ($t_{CH\text{-}CEL}$) if $\overline{ACX}$ low occurs prior to or coincident with the falling edge of ALE.

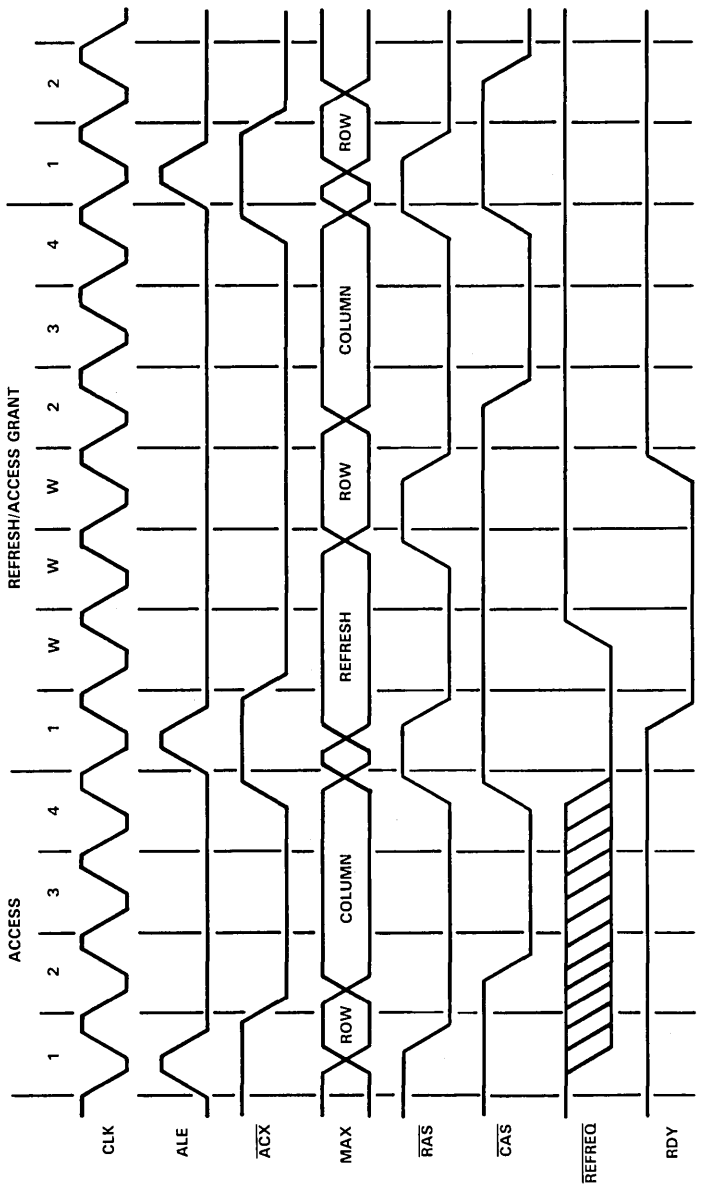
‡ On access grant cycle following refresh, $\overline{CAS}$ low and address multiplexing are timed from CLK low transition ($t_{CL\text{-}CEL}$) if $\overline{ACX}$ low occurs 20 ns or more after the falling edge of ALE.

typical access/refresh/access cycle
(three-cycle, TWST is low)

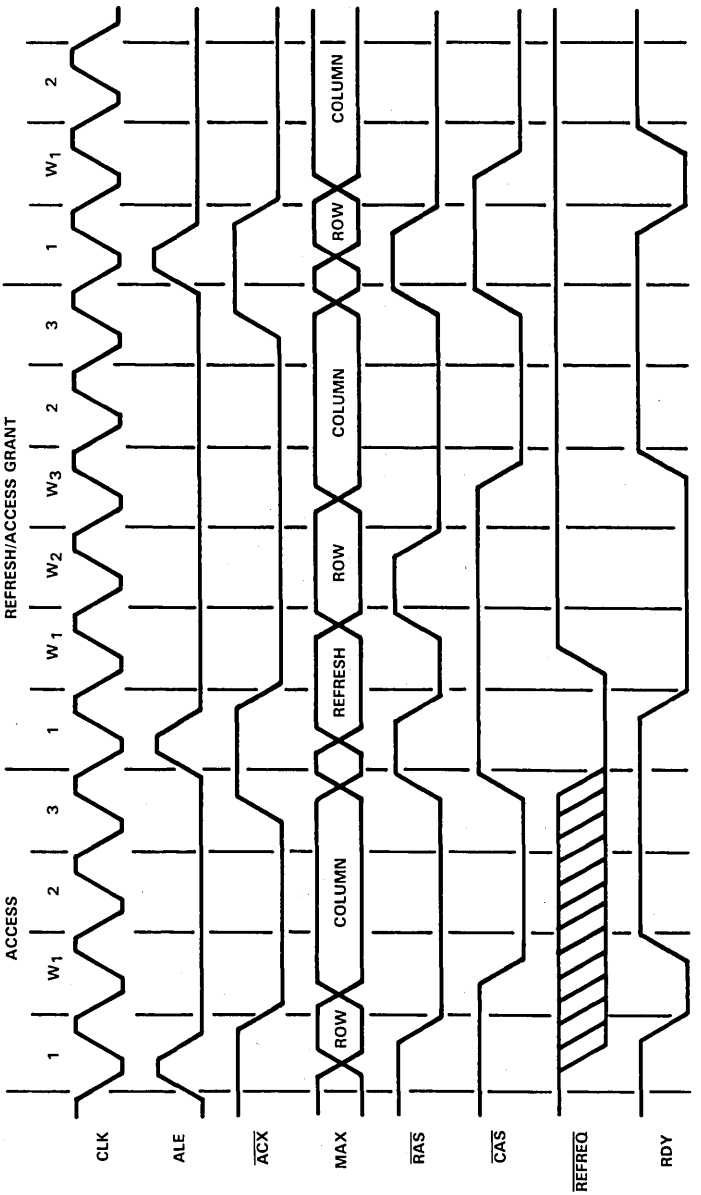


TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

typical access/refresh/access cycle
(four-cycle, TWST is low)

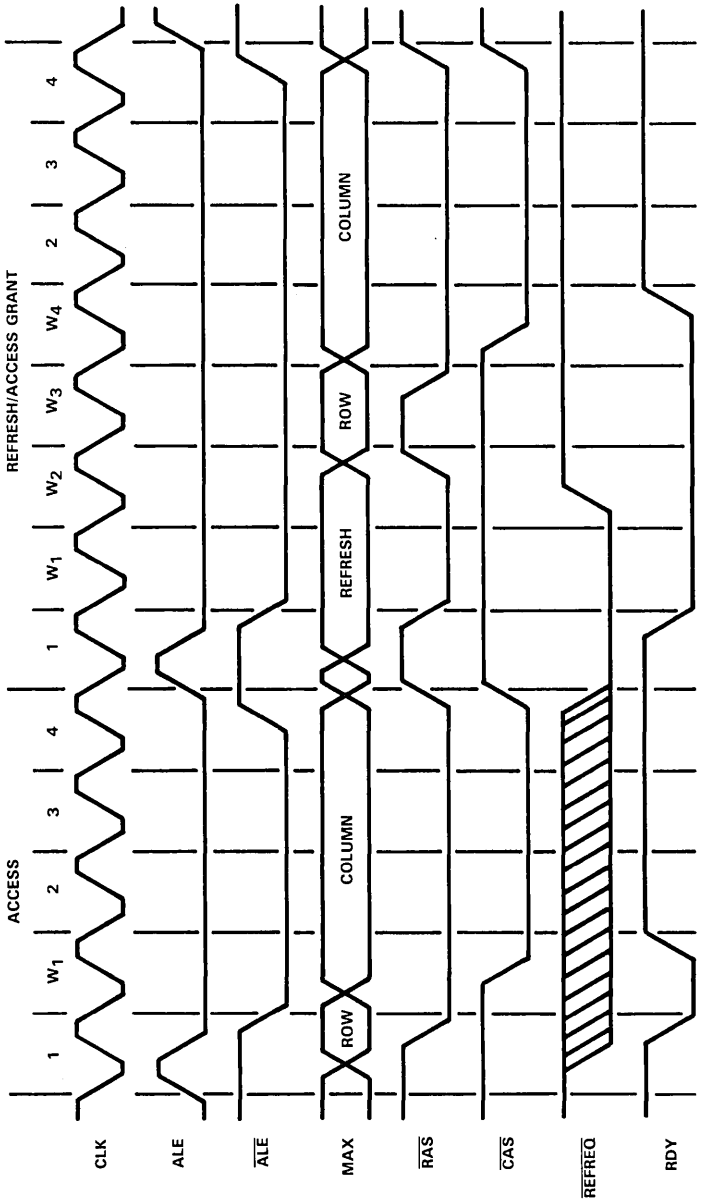


typical access/refresh/access cycle
(three-cycle, TWST is high)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

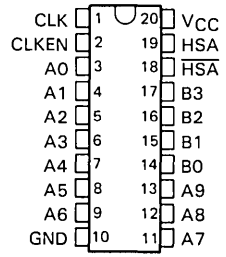
typical access/refresh/access cycle
(four-cycle, TWST is high)



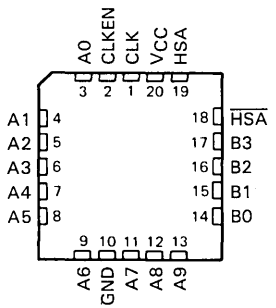
D3020, JUNE 1987—REVISED APRIL 1988

- Detects Present Row Equal to Last Row Address
- High-Performance Compare:
  'ALS6310 CLK to HSA = 18 ns
  'ALS6311 Address to HSA = 14 ns
- Compatible with 16K to 1M DRAMs
- Easily Interfaced with Microprocessor and Memory Timing Controller
- Dependable Texas Instruments Quality and Reliability

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



escription

The 'ALS6310 and 'ALS6311 are high-performance address comparators designed for implementing static column and page-mode access cycles.

When interfaced with the memory timing controller, these devices will detect if the present row being accessed is the same as the last row accessed. This is the fundamental requirement for implementing static column decode or page-mode access cycles.

The 'ALS6310 features two 14-bit registers and a high-speed address comparator. The first register is used to save the present row address while the second register is used to save the previous row address. On the high-to-low transition of CLK, the first register loads the new row address present on A0-A9. At the same time, the second register loads the address previously saved in the first register. The two row addresses are then compared. The High-Speed Access outputs (HSA and $\overline{\text{HSA}}$) will signal if the two addresses are equal.

The B0-B1 inputs are provided to monitor access cycles to different banks of memory. When used in conjunction with the 'ALS2968 and 'ALS6302 series DRAM controllers, the 'ALS6310 and 'ALS6311 can monitor up to 16 banks of memory. The CLK input on the 'ALS6310 can typically be interfaced with the microprocessor's Address Latch Enable (ALE) or Address Strobe (AS) outputs. This configuration simplifies the memory timing controller interface. Refer to the typical application diagram for further information.

The 'ALS6311 features one 14-bit register feeding a high-speed address comparator. This architecture offers a faster address match time, but does require the memory timing controller to generate the CLK input. Typically, the 14-bit register would only be updated if there was a change in row or bank address. Refer to the application diagram for further information.

More information on static column DRAM access can be found in the Texas Instruments application report *System Solutions for Static Column Decode*.

The SN74ALS6310 and SN74ALS6311 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE ('ALS6310)

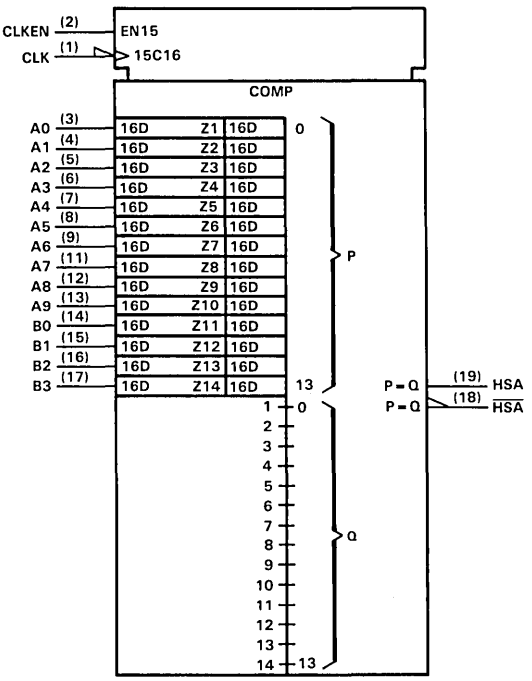
INPUTS				OUTPUTS	
CLKEN	CLK	A0-A9	B0-B3	HSA	$\overline{HSA}$
H	↓	P=Q	P=Q	H	L
H	↓	P=Q	P≠Q	L	H
H	↓	P≠Q	P=Q	L	H
H	↓	P≠Q	P≠Q	L	H
L	X	X	X	HSA_0	HSA_0

FUNCTION TABLE ('ALS6311)

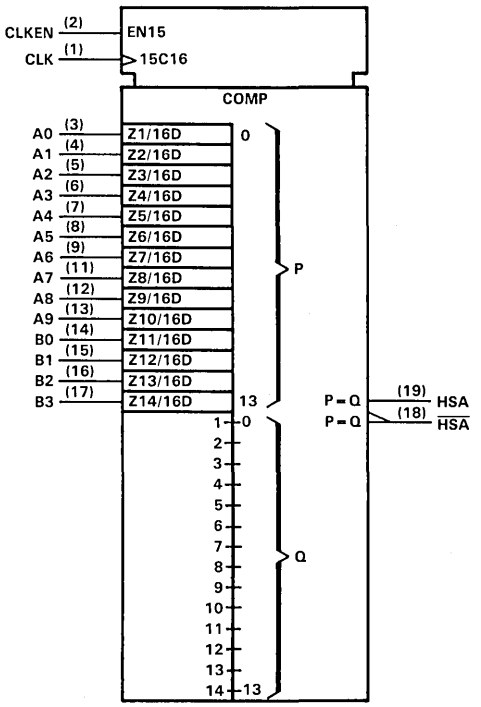
INPUTS				OUTPUTS	
CLKEN	CLK	A0-A9	B0-B3	HSA	$\overline{HSA}$
H	↑	P=Q	P=Q	H	L
H	↑	P=Q	P≠Q	L	H
H	↑	P≠Q	P=Q	L	H
H	↑	P≠Q	P≠Q	L	H
H	↑	X	X	H	L
L	X	X	X	HSA_0†	$\overline{HSA_0}$†

logic symbols

'ALS6310



'ALS6311

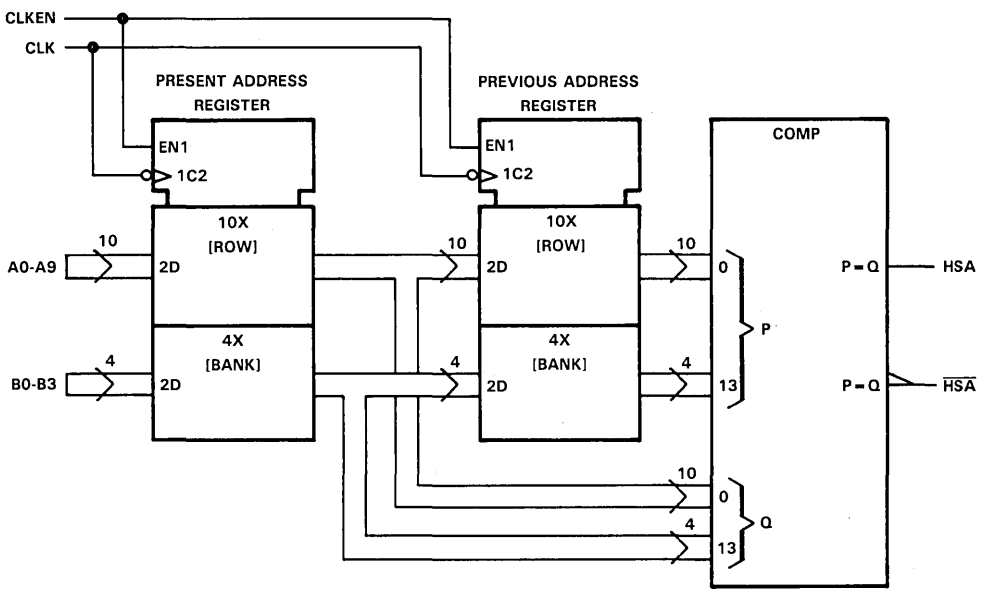


†Only if A0-A9 and B0-B3 inputs do not change from the time HSA and $\overline{HSA}$ were detected.

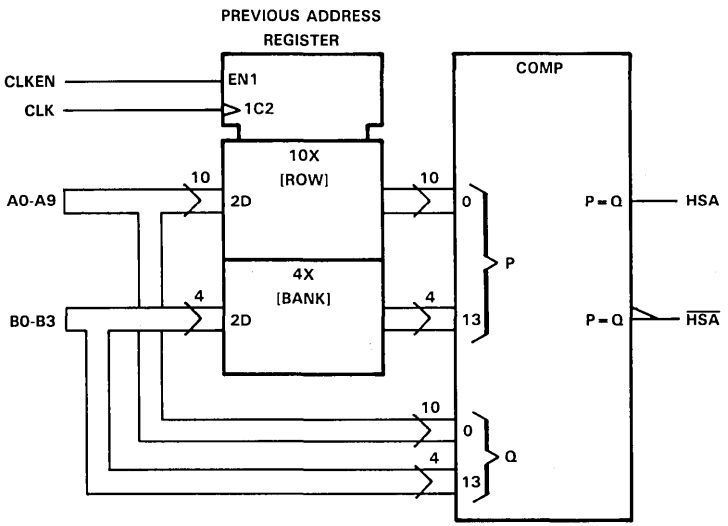
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

logic diagrams (positive logic)

'ALS6310



'ALS6311



absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN74ALS6310 SN74ALS6311			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2.6	mA
I_{OL}	Low-level output current				24	mA
t_w	Pulse duration, CLK high or low		10			ns
t_{su}	Setup time before CLK↓ ('ALS6310)	A0-A9 or B0-B3	8			ns
		CLKEN high or low	8			
t_{su}	Setup time before CLK↑ ('ALS6311)	A0-A9 or B0-B3	8			ns
		CLKEN high or low	8			
t_h	Hold time after CLK↓ ('ALS6310)	A0-A9 or B0-B3	5			ns
		CLKEN	5			
t_h	Hold time after CLK↑ ('ALS6311)	A0-A9 or B0-B3	5			ns
		CLKEN	5			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS6310 SN74ALS6311			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	'ALS6310		50	80	mA
		'ALS6311		40	70	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS INSTRUMENTS
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'ALS6310 switching characteristics (see Note 1)

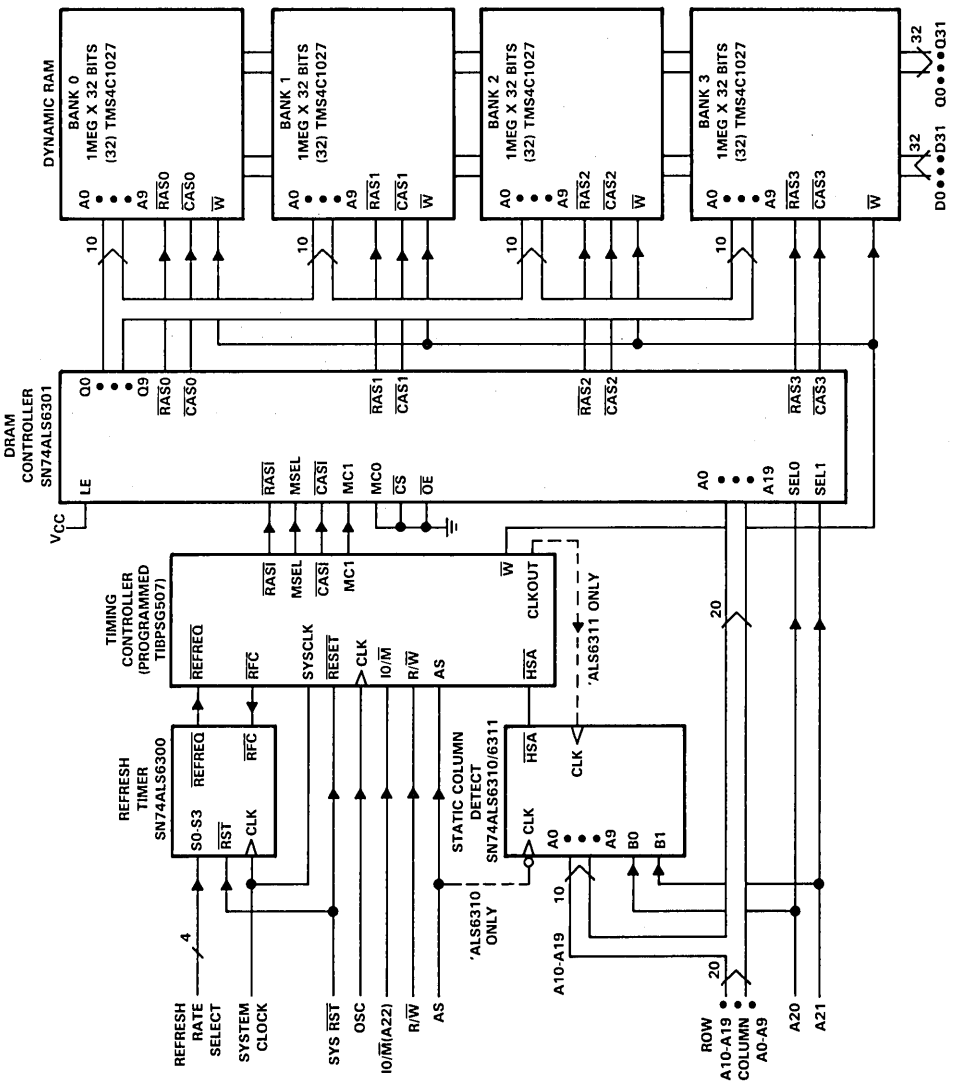
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	CLK↓	HSA		12	11	4	18	ns
t_{PHL}				12	18	4	18	ns
t_{PLH}	CLK↓	$\overline{HSA}$		12	18	4	18	ns
t_{PHL}				12	11	4	18	ns

'ALS6311 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	CLK↑	HSA		7	11	4	12	ns
t_{PHL}	CLK↑	$\overline{HSA}$		7	11	4	12	ns
t_{PLH}	A0-A9 or B0-B3	HSA		7	10	3	12	ns
t_{PHL}				9	14	4	14	ns
t_{PLH}	A0-A9 or B0-B3	$\overline{HSA}$		9	14	4	14	ns
t_{PHL}				7	10	3	12	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1 of *The LSI Logic Data Book*.

TYPICAL APPLICATION DATA



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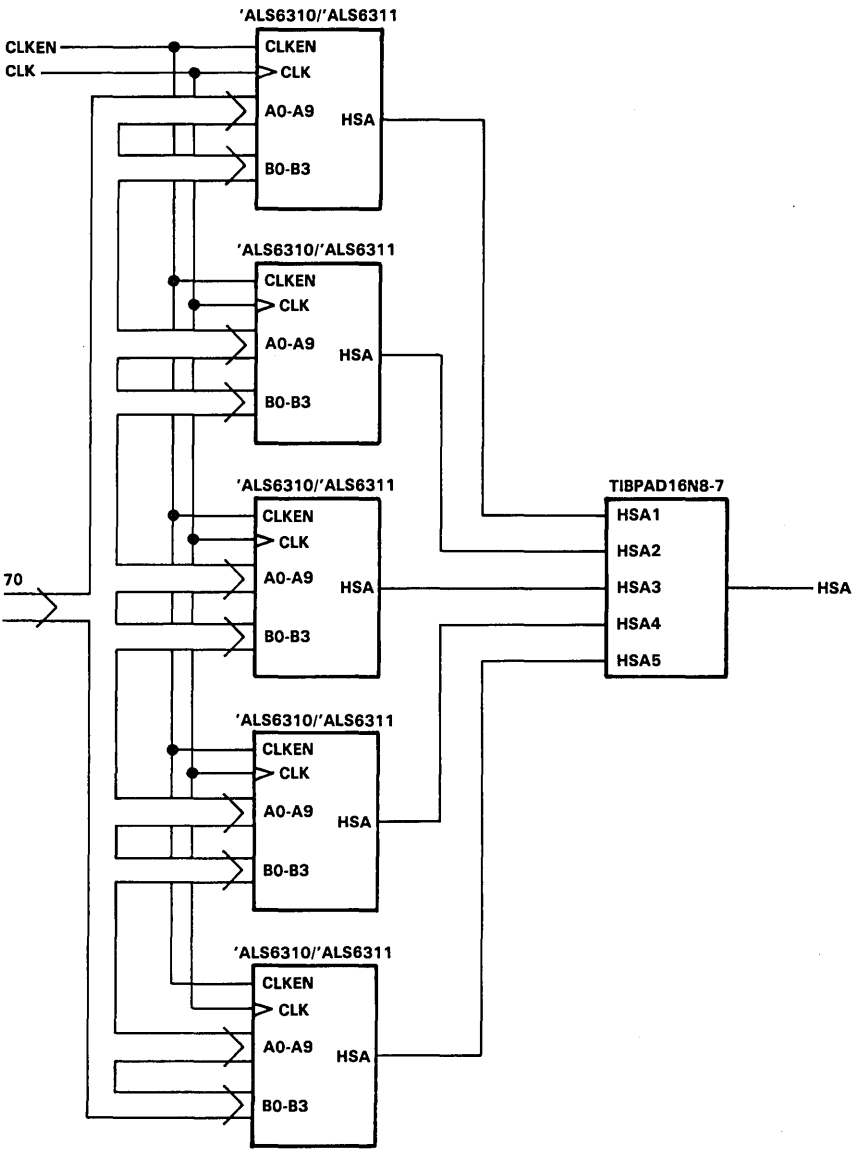
TYPICAL APPLICATION DATA

'ALS6310/'ALS6311 WORD LENGTH EXPANSION



D2977, APRIL 1987—REVISED APRIL 1988

- **BiCMOS Design Substantially Reduces Standby Current**
- **25-Ω Series Resistors at Outputs Significantly Reduce Overshoot and Undershoot**
- **Specifically Designed to Drive MOS DRAMs**
- **3-State Outputs**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic DIPs**

description

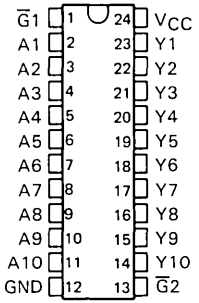
These 10-bit buffers and bus drivers are specifically designed to drive the capacitive input characteristics of MOS DRAMs. They provide high-performance bus interface for wide data paths or buses carrying parity.

The three-state control gate is a 2-input positive NOR gate so if either $\overline{G}1$ or $\overline{G}2$ is high, all 10 outputs are in the high-impedance state.

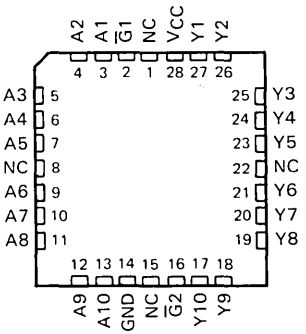
The SN74BCT2827A provides true data and the SN74BCT2828A provides inverted data at the outputs.

These devices are characterized for operation from 0°C to 70°C.

DW OR NT PACKAGE
(TOP VIEW)



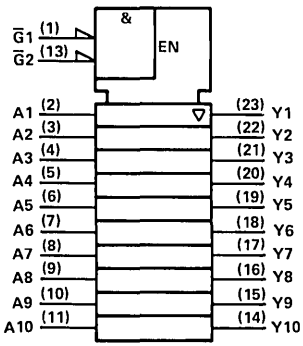
FN PACKAGE
(TOP VIEW)



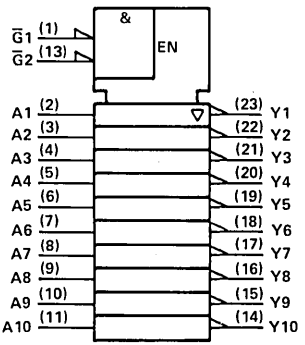
NC—No internal connection

logic symbols†

SN74BCT2827A



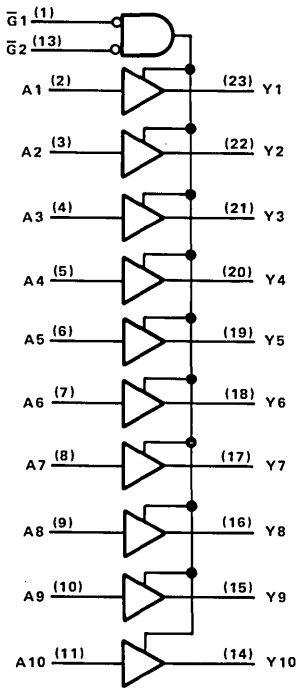
SN74BCT2828A



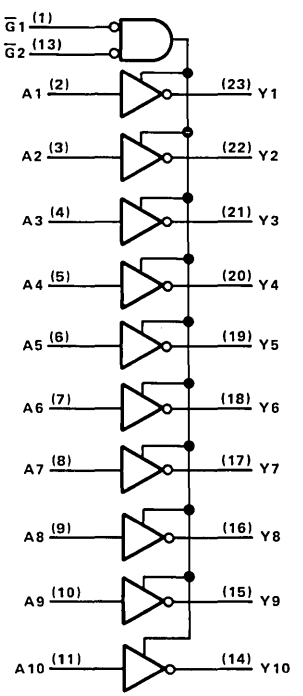
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN74BCT2827A



SN74BCT2828A



Pin numbers shown are for DW and NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

ıbsolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

ecommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	0		70	°C

lectrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −1 mA	V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_{OL}	V_{CC} = 4.5 V,	V_O = 2 V	50			mA
I_{OH}	V_{CC} = 4.5 V,	V_O = 2 V	−35			mA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open		28	40	mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open		3.5	6	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C,			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y		4	6		7	ns
t_{PHL}				6	8		9	
t_{PZH}	$\overline{G}$	Y		8	10		13	ns
t_{PZL}				11	14		17	
t_{PHZ}	$\overline{G}$	Y		8	12		15	ns
t_{PLZ}				7	11		13	

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} 7
Input voltage 5.5
Voltage applied to a disabled 3-state output 5.5
Operating free-air temperature range . . . . . 0°C to 70°
Storage temperature range . . . . . −65°C to 150°

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature (unless otherwise noted

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −1 mA	V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_{OL}	V_{CC} = 4.5 V,	V_O = 2 V	50			mA
I_{OH}	V_{CC} = 4.5 V,	V_O = 2 V	−35			mA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open		28	40	mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open		4.5	8	

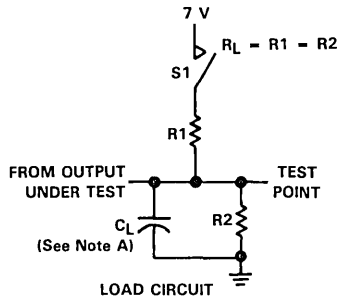
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a curent that closely approximates one half of the true short-circuit output current, I_{OS}

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C,			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y		5	7		8	ns
t_{PHL}				5	7		8	
t_{PZH}	$\overline{G}$	Y		8	11		12	ns
t_{PZL}				10	14		16	
t_{PHZ}	$\overline{G}$	Y		10	14		16	ns
t_{PLZ}				8	12		14	

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

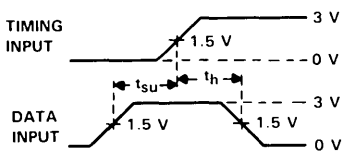
PARAMETER MEASUREMENT INFORMATION



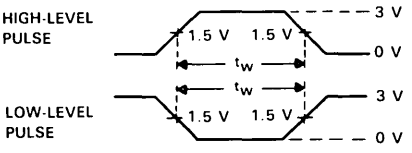
LOAD CIRCUIT

SWITCH POSITION TABLE

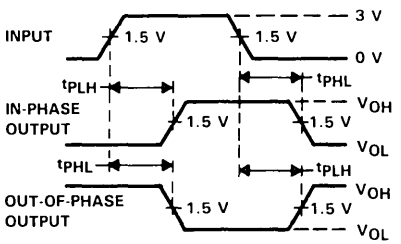
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



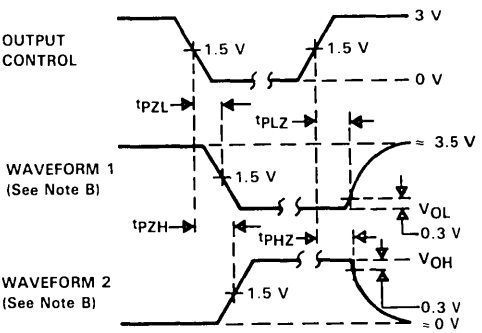
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal condition such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1. SWITCHING CHARACTERISTICS

D2977, APRIL 1987—REVISED MAY 1988

- **BiCMOS Design Substantially Reduces Standby Current**
- **Functionally Equivalent to AM29827, AM29828, SN74ALS29827, and SN74ALS29828**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic Chip Carriers, in Addition to Plastic and Ceramic DIPs**
- **BiCMOS Process with TTL Inputs and Outputs**
- **Dependable Texas Instruments Quality and Reliability**

description

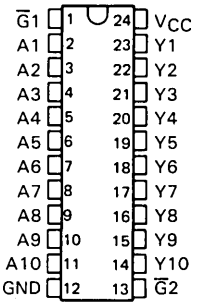
These 10-bit buffers and bus drivers provide high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input positive NOR gate so if either $\overline{G}1$ or $\overline{G}2$ is high, all 10 outputs are in the high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down.

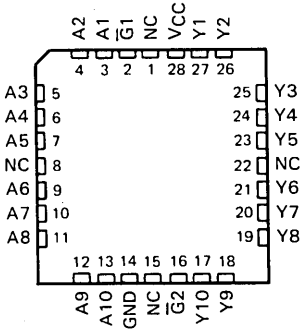
The SN74BCT29827A provides true data and the SN74BCT29828A provides inverted data at the outputs.

The SN74BCT29827A and SN74BCT29828A are characterized for operation from 0°C to 70°C.

DW OR NT PACKAGE
(TOP VIEW)



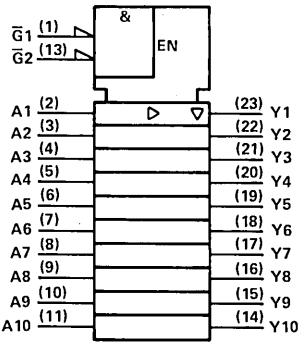
FN PACKAGE
(TOP VIEW)



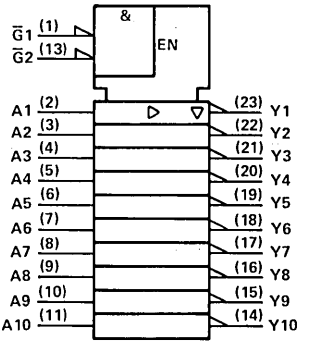
NC—No internal connection

logic symbols†

SN74BCT29827A



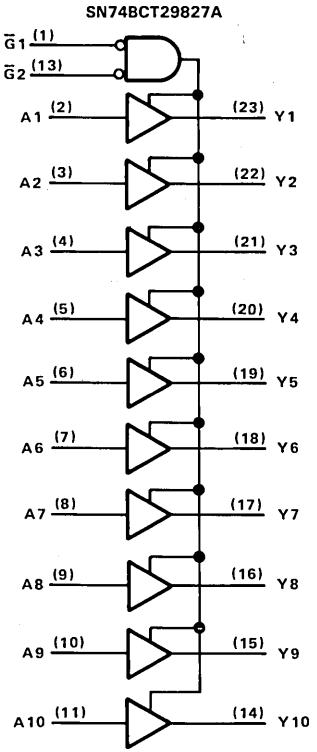
SN74BCT29828A



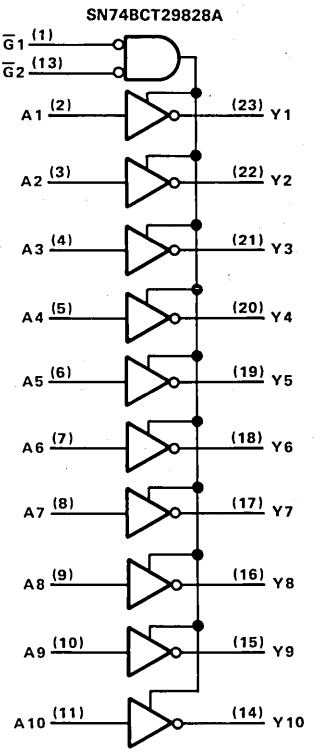
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN74BCT29827A



SN74BCT29828A



Pin numbers shown are for DW and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage (all inputs and I/O ports) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN	I_{OH} = −15 mA	2.4			V
		I_{OH} = −24 mA	2			
V_{OL}	V_{CC} = MIN,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.2	mA
I_{OS}§	V_{CC} = MAX,	V_O = 0	−75		−250	mA
I_{CCL}	V_{CC} = MAX,	Outputs open		28	40	mA
I_{CCZ}	V_{CC} = MAX,	Outputs open		3.5	6	mA

† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed 1 second.

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y		3.5	6		7	ns
t_{PHL}				5	7		9	
t_{PZH}	$\overline{G}$	Y		7	10		12	ns
t_{PZL}				10	13		15	
t_{PHZ}	$\overline{G}$	Y		7	10		12	ns
t_{PLZ}				7	10		12	

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage (all inputs and I/O ports) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN	I_{OH} = −15 mA	2.4			V
		I_{OH} = −24 mA	2			
V_{OL}	V_{CC} = MIN,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.2	mA
I_{OS}§	V_{CC} = MAX,	V_O = 0	−75		−250	mA
I_{CCL}	V_{CC} = MAX,	Outputs open		28	40	mA
I_{CCZ}	V_{CC} = MAX,	Outputs open		3.5	6.5	mA

† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed 1 second.

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y		3.5	6		7	ns
t_{PHL}				3.5	6		7	
t_{PZH}	$\overline{G}$	Y		7	9		11	ns
t_{PZL}				9	13		15	
t_{PHZ}	$\overline{G}$	Y		6	9		10	ns
t_{PLZ}				6	10		11	

TEXAS INSTRUMENTS
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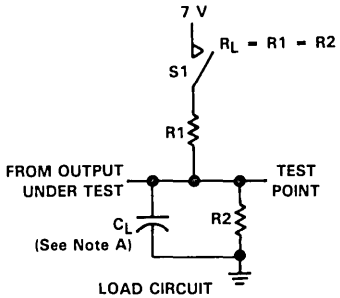
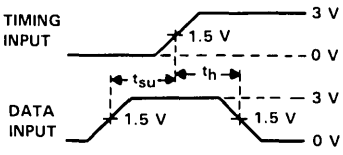
PARAMETER MEASUREMENT INFORMATION



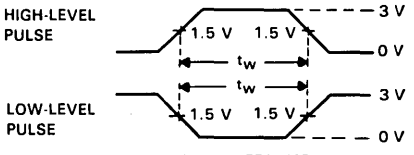
LOAD CIRCUIT

SWITCH POSITION TABLE

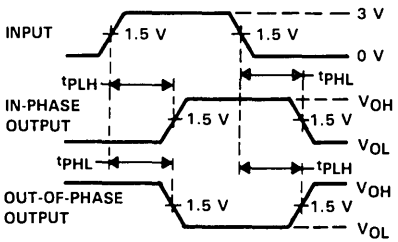
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



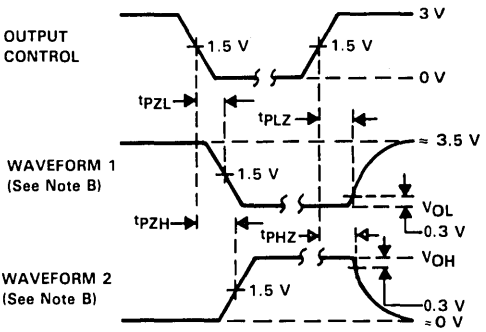
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



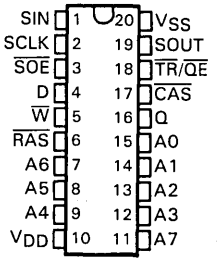
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

JUNE 1985 – REVISED FEBRUARY 1988

- MIL-STD-883C High-Reliability Processed and −55°C to 100°C (S Designator) Temperature Range, 20-Pin 300-Mil Ceramic Sidebrazed Package
- Dual Accessibility — One Port Sequential Access, One Port Random Access
- Four Cascaded 64-Bit Serial Shift Registers for Sequential Access Applications
- Designed for both Video and Non-Video Applications
- Fast Serial Port . . . Can Be Configured for Video Data Rates in Excess of 150 MHz
- $\overline{TR}/\overline{QE}$ as Output Enable Allows Direct Connection of D, Q, and Address Lines to Simplify System Design
- Random-Access Port Looks Exactly Like a SMJ4164
- Separate Serial In and Serial Out to Allow Simultaneous Shift In and Out
- 65,536 × 1 Organization
- Supported by TI's Video System Controller (VSC)
- Maximum Access Time from $\overline{RAS}$ Less Than 150 ns
- Minimum Cycle Time (Read or Write) Less Than 240 ns
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.7% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs for Both Random and Serial Access
- Common I/O Capability with Early Write Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation (SMJ4161-15)
  - Operating . . . 250 mW (Typical)
  - Standby . . . 80 mW (Typical)
- New SMOS (Scaled-MOS) N-Channel Technology
- $\overline{SOE}$ Simplifies Multiplexing of Serial Data Streams

JD PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Random-Access Data In
Q	Random-Access Data Out
$\overline{RAS}$	Row-Address Strobe
SCLK	Serial Data Clock
SIN	Serial Data In
$\overline{SOE}$	Serial Output Enable
SOUT	Serial Data Out
$\overline{TR}/\overline{QE}$	Register Transfer/Q Output Enable
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The SMJ4161 is a high-speed, dual-access 65,536-bit dynamic random-access memory. The random-access port makes the memory look like it is organized as 65,536 words of one bit each, like the SMJ4164. The sequential access port is interfaced to an internal 256-bit dynamic shift register organized as four cascaded 64-bit shift registers which makes the memory look like it is organized as up to 256 words of up to 256 bits each which are accessed serially. One, two, three, or four 64-bit shift registers can be sequentially read out after a transfer cycle, depending on a two-bit code applied to the two most significant column address inputs. The SMJ4161 employs state-of-the-art SMOS (Scaled-MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The SMJ4161 features full asynchronous dual access capability except when transferring data between the shift register and the memory array.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. Note that the transfer of a row of data from the memory array to the shift register also refreshes that row.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All address lines and data in are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ4161 is offered in a 20-pin ceramic dual-in-line package. It is guaranteed for operation from $T_A = -55°C$ to $T_C = 100°C$. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

random access address space to sequential address space mapping

The SMJ4161 is designed with each row divided into four, 64-column sections (see functional block diagram). The first column section to be shifted out is selected by the two most significant column address bits. If the two bits represent binary 00, then one to four registers can be shifted out in order. If the two bits represent binary 01, then only 1 to 3 (the most significant) registers can be shifted out in order. If the two bits represent binary 10, then one to two of the most significant registers can be shifted out in order. Finally, if the two bits represent 11, only the most significant registers can be shifted out. All registers are shifted out with the least significant bit (bit 0) first and the most significant bit (bit 63) last. Note that if the two column address bits equal 00 during the last register transfer cycle ($\overline{TR}/\overline{QE}$ at logic level 0 as $\overline{RAS}$ falls) a total of 256 bits can be sequentially read out.

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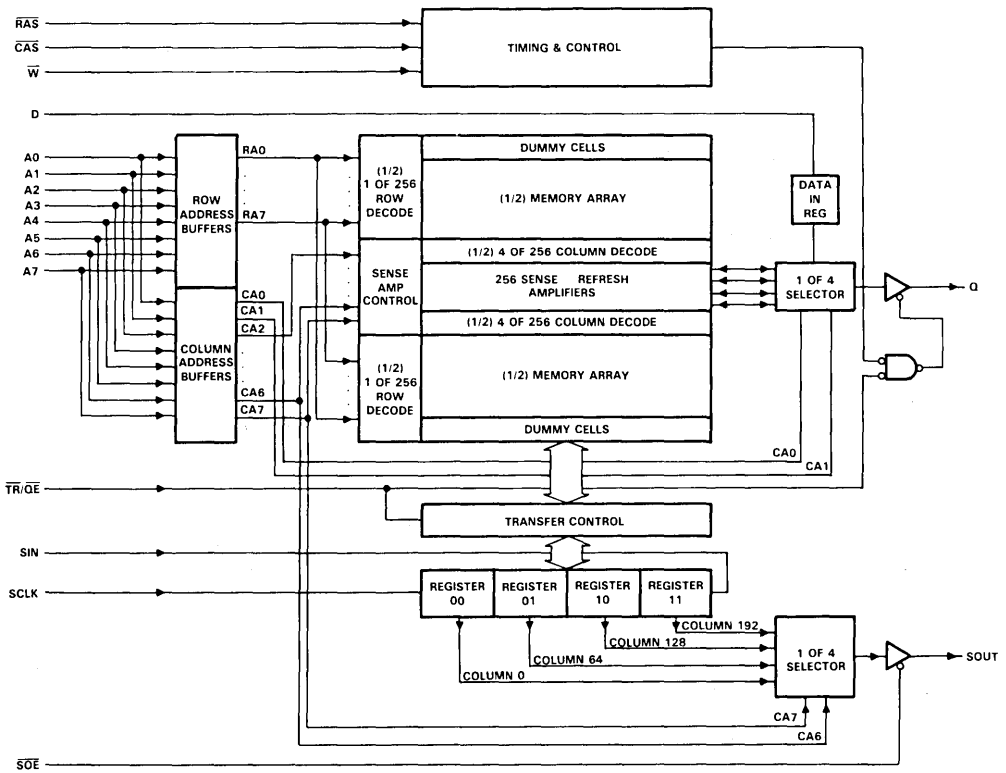
functional block diagram



random-access operation

TR/QE

The TR/QE pin has two functions. First, it selects either register transfer or random-access operation as RAS falls, and second, if this is a random-access operation, it functions as an output enable after CAS falls.

To use the SMJ4161 in the random-access mode, TR/QE must be high as RAS falls. Holding TR/QE high as RAS falls keeps the 256 elements of the shift registers disconnected from the corresponding 256 bit lines of the memory array. If data is to be transferred, the shift registers must be connected to the bit lines. Holding TR/QE low as RAS falls enables the 256 switches that connect the shift register to the bit lines and indicates that a transfer will occur between the shift registers and one of the memory rows.

During random-access operation, once CAS has been pulled low, TR/QE controls when the data will appear at the Q output (if this is a read cycle). Whenever TR/QE is held high during random-access operation, the Q output will be in the high-impedance state. This feature removes the possibility of an overlap between data on the address lines and data appearing on the Q output, making it possible to connect the address lines to the Q and D lines (use of this organization prohibits the use of the early write cycle).

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatability (no pull-up resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state as long as $\overline{CAS}$ or $\overline{TR}/\overline{QE}$ is held high. Data will not appear on the output until after both $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ have been brought low. In a read cycle, the guaranteed maximum output enable access time is valid only if t_{CQE} is greater than t_{CQE} MAX and t_{RLCL} is greater than t_{RLCL} MAX. Likewise, $t_{a(C)}$ MAX is valid only if t_{RLCL} is greater than t_{RLCL} MAX. Once the output is valid, it will remain valid while $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ are both low; $\overline{CAS}$ or $\overline{TR}/\overline{QE}$ going high will return the output to a high-impedance state. In an early write cycle, the output is always in a high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle. In a register transfer cycle, the output will always be in a high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address strobing successive column addresses onto the chip. Thus, the time required to set up and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

sequential access operation

$\overline{TR}/\overline{QE}$

Memory transfer operations involving parallel use of the shift register are first indicated by bringing $\overline{TR}/\overline{QE}$ low before $\overline{RAS}$ falls low. This enables the switches connecting the 256 elements of the shift register to the 256 bit lines of the memory array. The $\overline{W}$ line determines whether the data will be transferred from or to the shift registers.

write enable ($\overline{W}$)

In the sequential access mode, $\overline{W}$ determines whether a transfer will occur from the shift registers to the memory array, or from the memory array to the shift registers. To transfer from the shift registers to the memory array, $\overline{W}$ is held low as $\overline{RAS}$ falls, and, to transfer from the memory array to the shift registers, $\overline{W}$ is held high as $\overline{RAS}$ falls. Thus, reads and writes are always with respect to the memory array. The write setup and hold times are referenced to the falling edge of $\overline{RAS}$ for this mode of operation.

row address (A0 through A7)

Eight address bits are required to select one of the 256 possible rows involved in the transfer of data to or from the shift registers. A0-A7, $\overline{W}$, and $\overline{TR}/\overline{QE}$ are latched on the falling edge of $\overline{RAS}$.

register column address (A7, A6)

To select one of the four shift registers (transfer from memory to register only), the appropriate 2-bit column address (A7, A6) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and register address signals need not be supplied every cycle, only when it is desired to change or select a new register.

SCLK

Data is shifted in and out on the rising edge of SCLK. This makes it possible to view the shift registers as though they were made of 256 rising edge D flip-flops connected D to Q. The SMJ4161 is designed to work with a wide range duty cycle clock to simplify system design. Note that data will appear at the SOUT pin not only on the rising edge of SCLK but also after an access time of $t_{a(RSO)}$ from $\overline{RAS}$ high during a parallel load of the shift registers.

SIN and SOUT

Data is shifted in through the SIN pin and is shifted out through the SOUT pin. The SMJ4161 is designed such that it requires 3 ns hold time on SIN as SCLK rises. SOUT is guaranteed not to change for at least 6 ns after SCLK rises. These features make it possible to easily connect SMJ4161s together, to allow SOUT to be connected to SIN, and to give external circuitry a full SCLK cycle time to allow manipulation of the serial data. If SOUT is connected to SIN, the SCLK cycle time must include $t_{su(SI)}$. When loading data into the shift register from the serial input in preparation for a shift-register-to-memory transfer operation, the serial clock must be clocked an even number of times. To guarantee proper serial clock sequence after power up, a transfer cycle must be initiated before a serial data stream is applied at SIN.

$\overline{SOE}$

The serial output enable pin controls the impedance of the serial output, allowing multiplexing of more than one bank of SMJ4161 memories into the same external video circuitry. When $\overline{SOE}$ is at a logic low level, SOUT will be enabled and the proper data read out. When $\overline{SOE}$ is at a logic high level, SOUT will be disabled and be in the high-impedance state.

refresh

The shift registers are also dynamic storage elements. The data held in the registers will be lost unless SCLK goes high to shift the data one bit position, a transfer write operation is invoked, or the data is reloaded from the memory array. See specifications for maximum register data retention times.

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Minimum operating free-air temperature . . . . . −55°C
Operating case temperature . . . . . 100°C
Storage temperature range . . . . . −65°C to 150°C

†Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		$V_{DD}+0.3$	V
V_{IL}	Low-level input voltage (see Notes 2 and 3)	−0.6		0.8	V
T_A	Operating free-air temperature	−55			°C
T_C	Operating case temperature			100	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V; test conditions must comprehend this occurrence.

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electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4161-15			SMJ4161-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage (Q, SOUT)	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage (Q, SOUT)	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, Outputs = open			±10			±10	μA
I_O‡	Output current (leakage) (Q, SOUT)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	$t_{c(rd)}$ = minimum cycle time, $\overline{TR/QE}$ low after $\overline{RAS}$ falls,§ SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		50	75		45	75	mA
I_{DD2}¶	Standby current	After 1 −$\overline{RAS}$ cycle, $\overline{RAS}$ and $\overline{CAS}$ high, SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		16	25		16	25	mA
I_{DD3}	Average refresh current	$t_{c(rd)}$ = minimum cycle time, $\overline{CAS}$ high, $\overline{RAS}$ cycling, SCLK and SIN low, $\overline{SOE}$ high, $\overline{TR/QE}$ high, No load on Q and SOUT		42	60		37	60	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle time, $\overline{RAS}$ low, $\overline{CAS}$ cycling, $\overline{TR/QE}$ low after $\overline{RAS}$ falls, SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		45	75		40	75	mA
I_{DD5}	Average shift register current (includes I_{DD2})	$\overline{RAS}$ and $\overline{CAS}$ high, No load on Q and SOUT, $t_{c(SCLK)}$ = $t_{c(SCLK)}$ min		30	45		30	45	mA
I_{DD6}	Worst case average DRAM and shift register current	$t_{c(rd)}$ = minimum cycle time, $t_{c(SCLK)}$ = minimum cycle time, $\overline{TR/QE}$ low after $\overline{RAS}$ falls, No load on Q and SOUT		85	100		85	100	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡SOUT output current (leakage) is guaranteed but not tested.
§See appropriate timing diagram.
¶V_{IL} > −0.6 V.

capacitance over recommended supply voltage and operating temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4		pF
$C_{i(D)}$	Input capacitance, data input	4		
$C_{i(RC)}$	Input capacitance, strobe inputs	8		
$C_{i(W)}$	Input capacitance, write enable input	8		
$C_{i(CK)}$	Input capacitance, serial clock	8		
$C_{i(SI)}$	Input capacitance, serial in	4		
$C_{i(SOE)}$	Input capacitance, serial output enable	4		
$C_{i(TR)}$	Input capacitance, register transfer input	4		
$C_{o(Q)}$	Output capacitance, random-access data	5		
$C_{o(SOUT)}$	Output capacitance, serial out	5		

†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS‡	ALT. SYMBOL	SMJ4161-15		SMJ4161-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 80 pF, I_{OL} = 4.2 mA, I_{OH} = −5 mA	t_{CAC}		100		135	ns
$t_{a(QE)}$	Access time of Q from $\overline{TR}/\overline{QE}$ low				40		50	
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = max, C_L = 80 pF, I_{OL} = 4.2 mA, I_{OH} = −5 mA	t_{RAC}		150		200	
$t_{a(RSO)}$	SOUT access time from $\overline{RAS}$ high	C_L = 80 pF, I_{OL} = 4.2 mA, I_{OH} = −5 mA			65		85	
$t_{a(SOE)}$	Access time from $\overline{SOE}$ low to SOUT				45		50	
$t_{a(SO)}$	Access time from SCLK				45		55	
$t_{dis(CH)}$	Q output disable time from $\overline{CAS}$ high		t_{OFF}		40		40	
$t_{dis(QE)}$	Q output disable time from $\overline{TR}/\overline{QE}$ high				30		40	
$t_{dis(SOE)}$	Serial output disable time from $\overline{SOE}$ high				20		25	

‡Figure 1 shows the load circuit; C_L values shown are typical for test system used.

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timing requirements over recommended supply voltage range and operating temperature range

PARAMETER		ALT. SYMBOL	SMJ4161-15		SMJ4161-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	160		225		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	240		315		ns
$t_{c(W)}$	Write cycle time	t_{WC}	240		315		ns
$t_{c(TW)}$	Transfer write cycle time‡		240		315		ns
$t_{c(Trd)}$	Transfer read cycle time		240		315		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	265		330		ns
$t_{c(SCLK)}$	Serial clock cycle time (see Note 4)	t_{SCC}	45	50,000	55	50,000	ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)§	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low¶	t_{CAS}	100	10,000	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		105		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low#	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		45		ns
$t_{w(CKL)}$	Pulse duration, SCLK low‖		20		20		ns
$t_{w(CKH)}$	Pulse duration, SCLK high‖		20		20		ns
$t_{w(QE)}$	$\overline{TR}/\overline{QE}$ pulse duration low time (read cycle)		50		50		ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(RW)}$	$\overline{W}$ setup time before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	5		5		ns
$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	40		60		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	40		60		ns
$t_{su(TR)}$	$\overline{TR}/\overline{QE}$ setup time before $\overline{RAS}$ low		5		5		ns
$t_{su(SI)}$	Serial data setup time before SCLK high		6		6		ns
$t_{h(SI)}$	Serial data in hold time after SCLK high		3		3		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	45		55		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	20		25		ns
$t_{h(RW)}$	$\overline{W}$ hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		30		30		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	95		120		ns

Continued next page.

NOTES: 4. $t_{c(SCLK)}$ min is tested by connecting SIN to SOUT and test conditions include $t_{su(SI)}$; see paragraph entitled SIN and SOUT on page 5.

5. Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

6. System transition times (rise and fall) for $\overline{RAS}$, $\overline{CAS}$, and SCLK are to be a minimum of 3 ns and a maximum of 50 ns.

†All cycle times assume t_t = 5 ns except $t_{c(SCLK)}$ which assumes t_t = 3 ns.

‡Multiple transfer write cycles require separation by either a 1-μs $\overline{RAS}$-precharge interval or any other active $\overline{RAS}$-cycle.

§Page-mode only.

¶In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

#In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

‖This parameter is guaranteed but not tested.

timing requirements over recommended supply voltage range and operating temperature range (concluded)

PARAMETER		ALT. SYMBOL	SMJ4161-15		SMJ4161-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	60		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	110		145		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	60		80		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	110		145		ns
$t_{h(RSO)}$	Serial data out hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low‖		30		30		ns
$t_{h(SO)}$	Serial data out hold time after SCLK high		6		6		ns
$t_{h(TR)}$	$\overline{TR}/\overline{QE}$ hold time after $\overline{RAS}$ low (tansfer)		40		40		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLQEH}	Delay time $\overline{CAS}$ low to QE high		100		135		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	100		135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	65		75		ns
t_{CQE}	Delay time, $\overline{CAS}$ low to QE low (maximum value specified only to guarantee $t_{a(QE)}$ access time)			60		85	ns
t_{RHSC}	Delay time, $\overline{RAS}$ high to SCLK high		80		80		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	50	30	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	135		150		ns
t_{CKRL}	Delay time, SCLK high before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low☆		10		10		ns
$t_{rf(MA)}$	Refresh time interval, memory array	t_{REF1}		4		4	ms
$t_{rf(SR)}$	Refresh time interval, shift register□	t_{REF2}		50,000		50,000	ns

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

‖ This parameter is guaranteed but not tested.

☆SCLK may be high or low during $t_{w(RL)}$, but there cannot be any positive edge transitions on SLCK for a minimum of 10 ns prior to $\overline{RAS}$ going low with $\overline{TR}/\overline{QE}$ low (i.e., before a transfer cycle).

□See "refresh" on page 5.

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PARAMETER MEASUREMENT INFORMATION

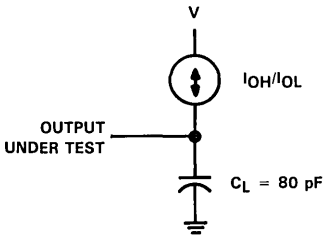
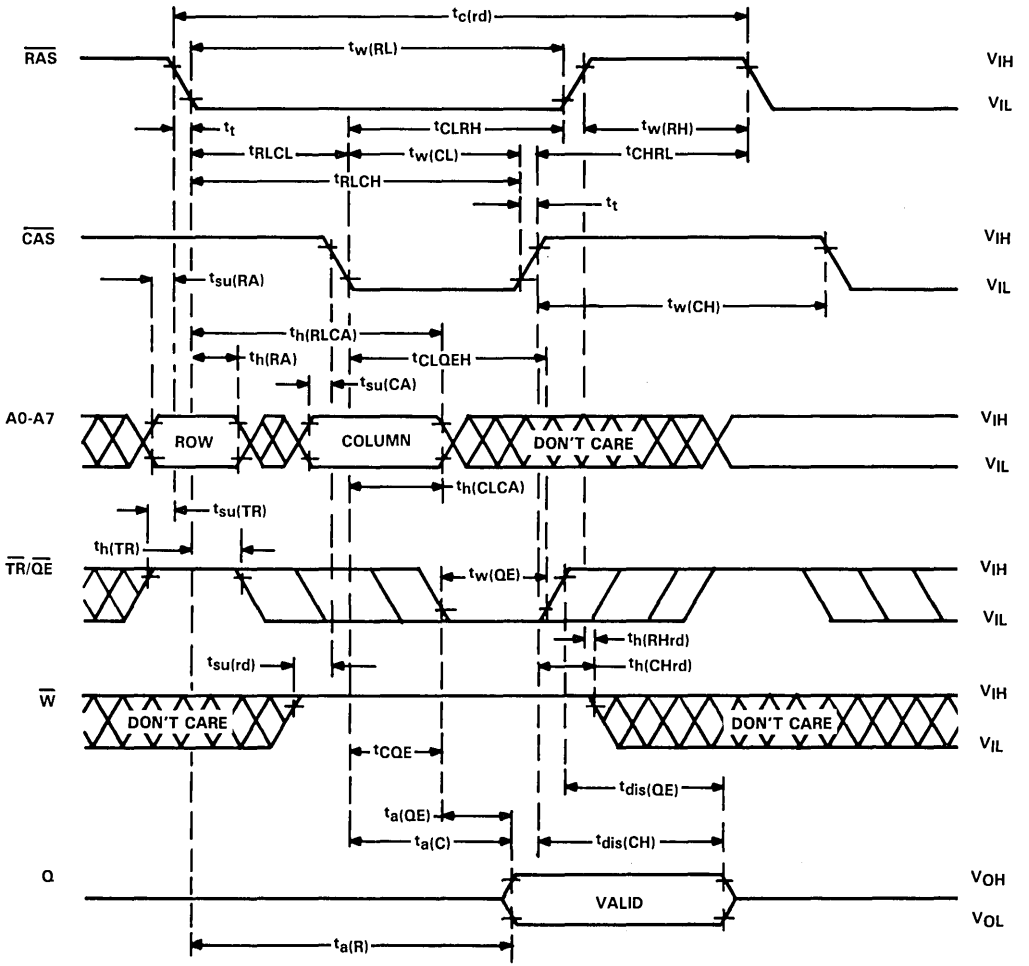


FIGURE 1. EQUIVALENT LOAD CIRCUIT

read cycle timing



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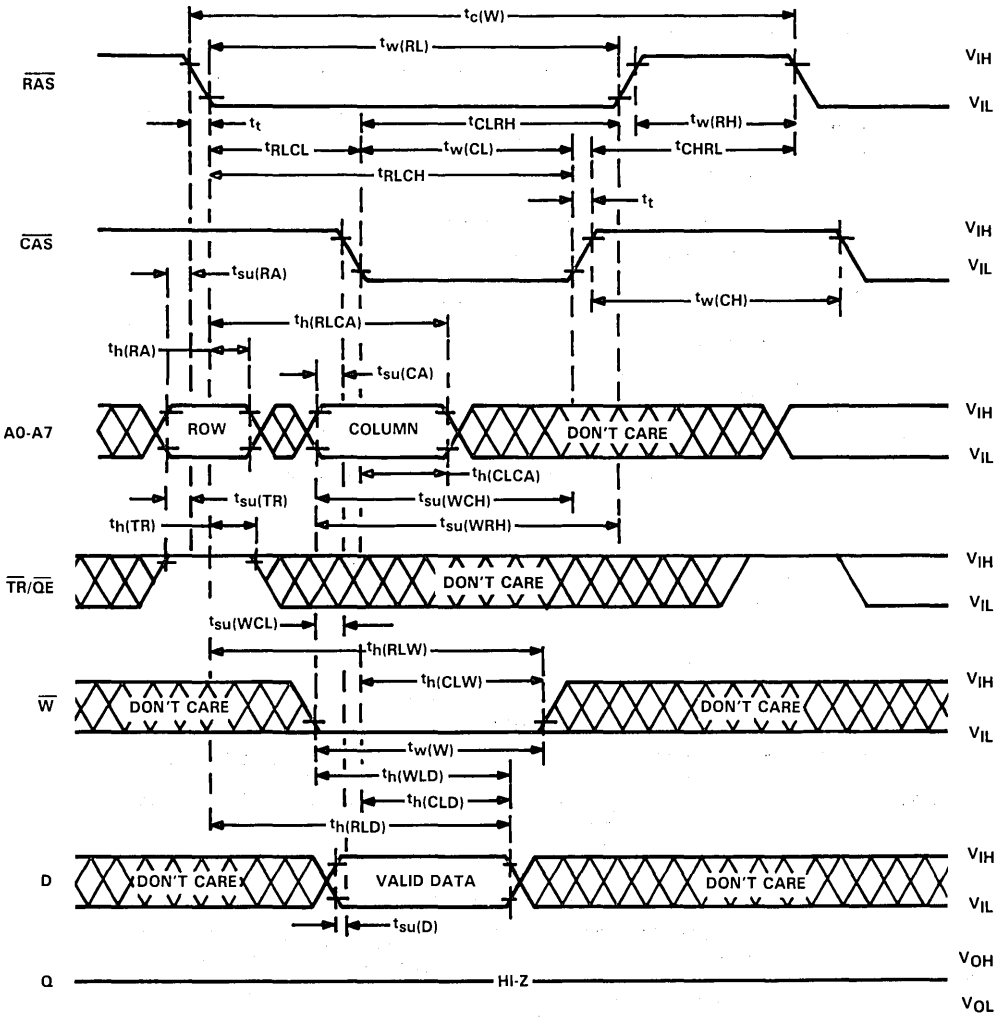
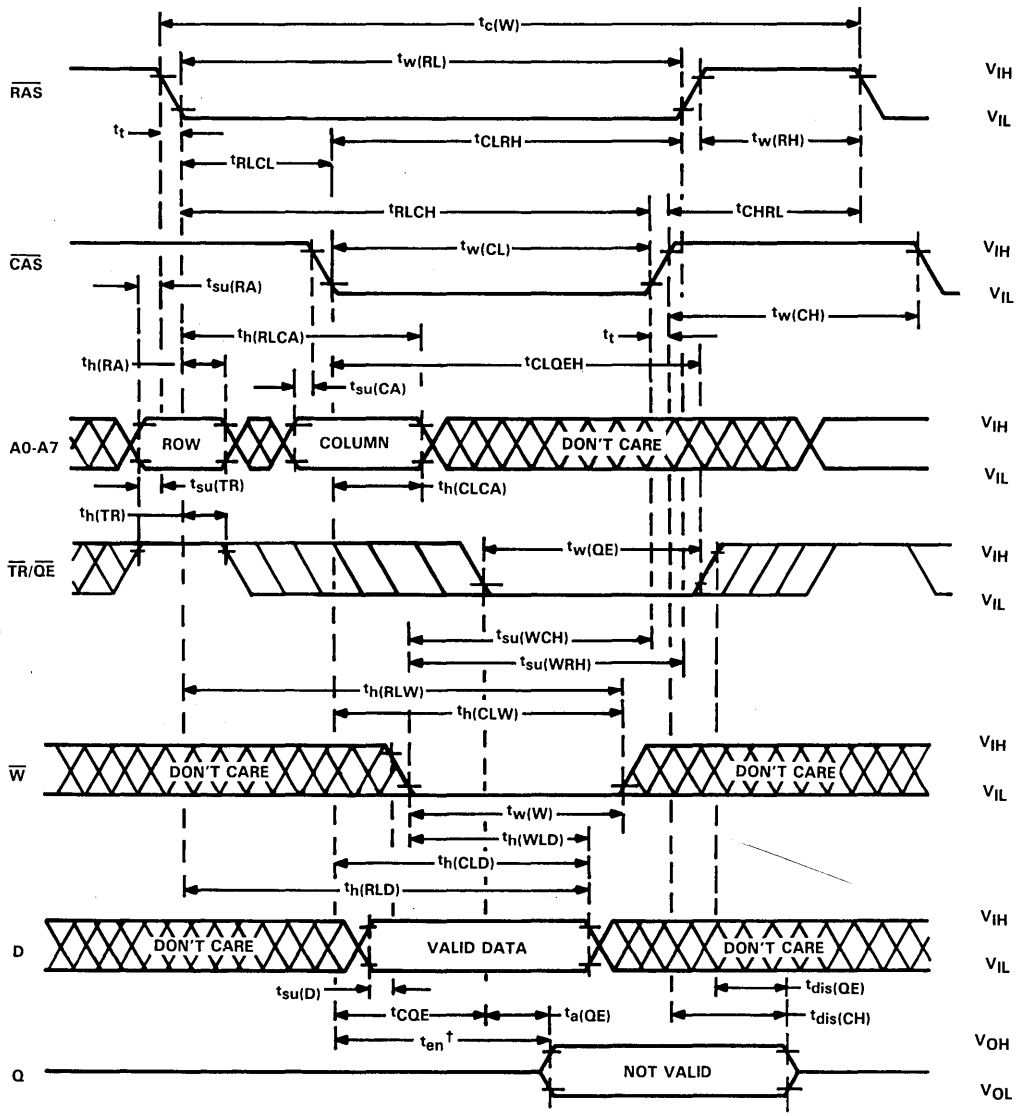
early write cycle timing



write cycle timing



†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

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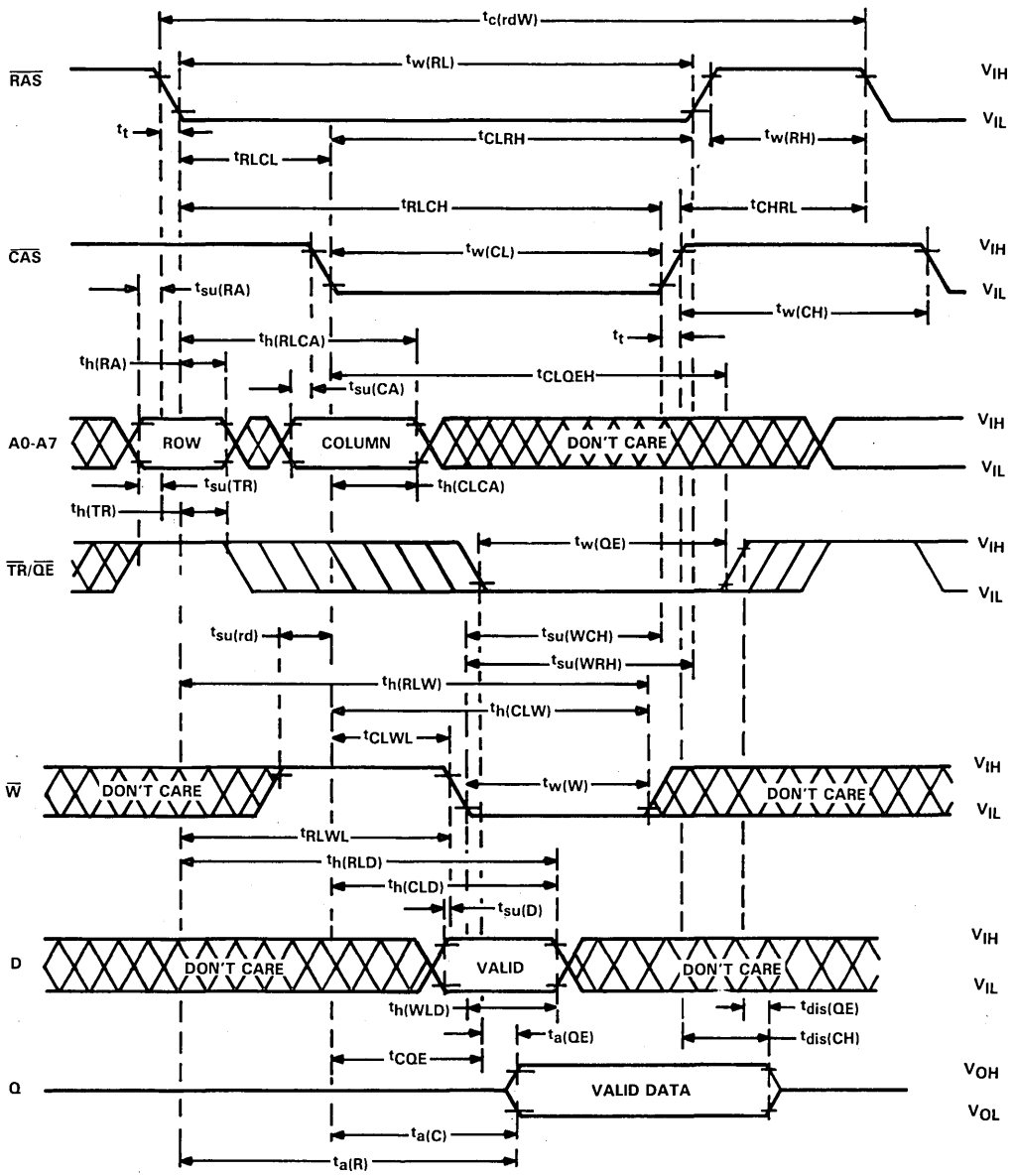
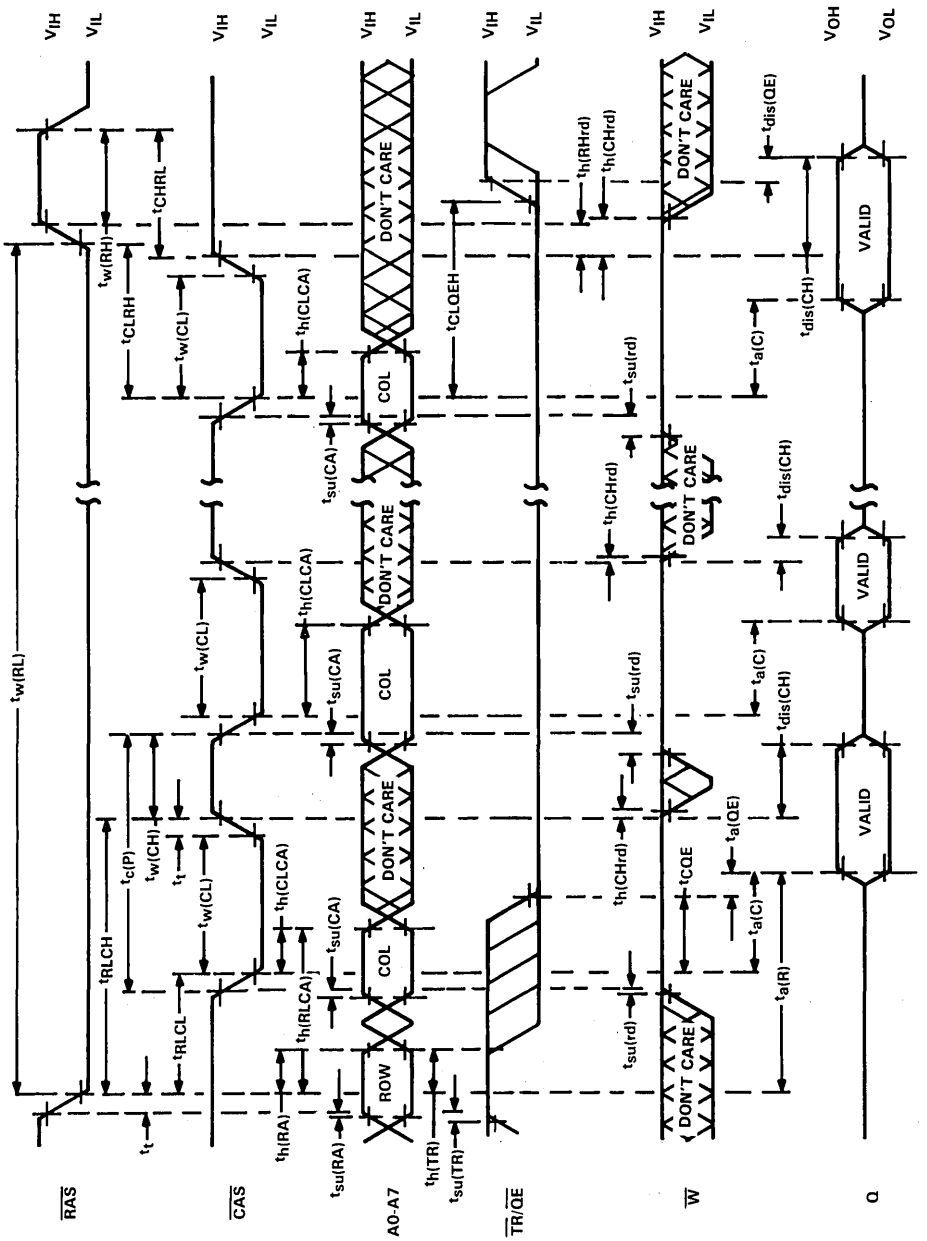
read-write/read-modify-write cycle timing

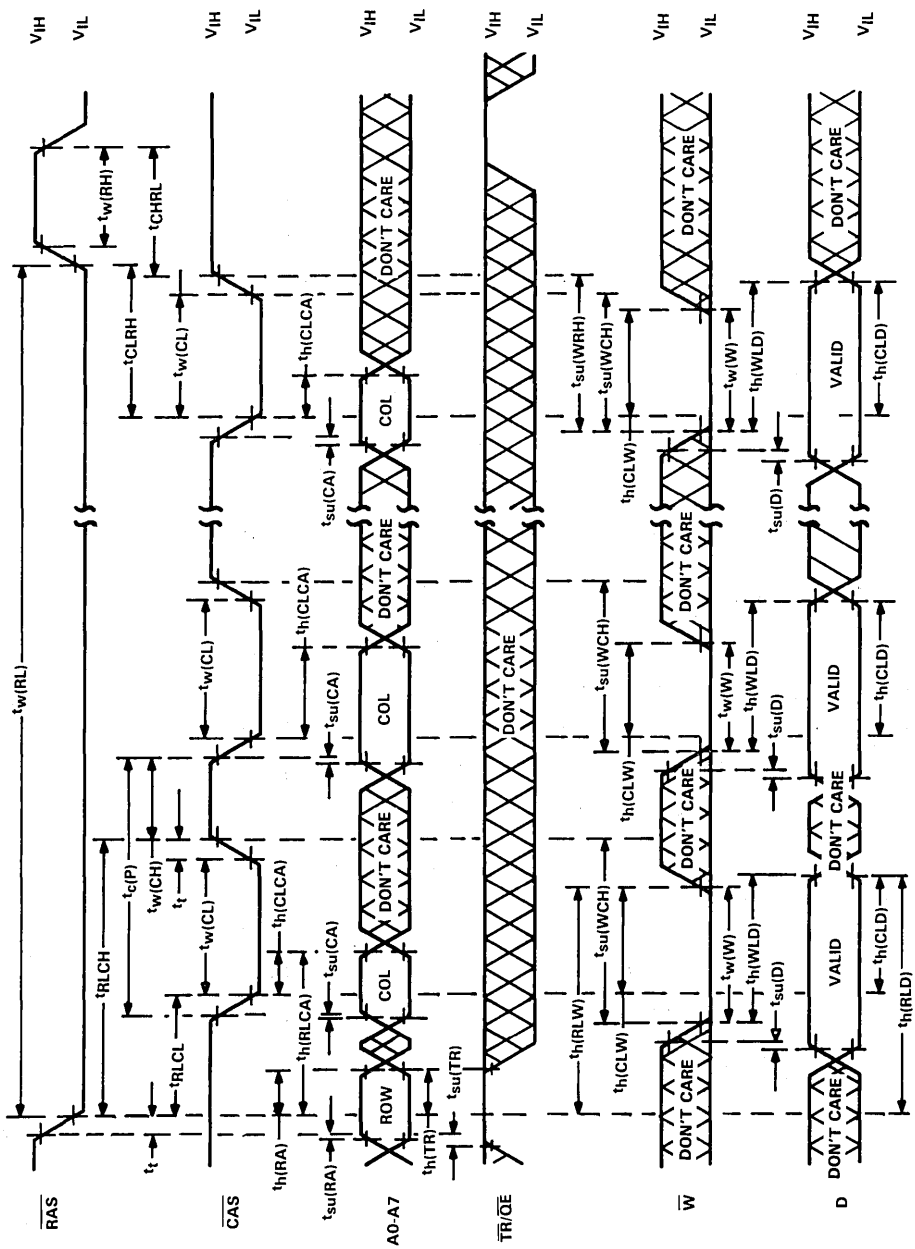


page-mode read cycle timing



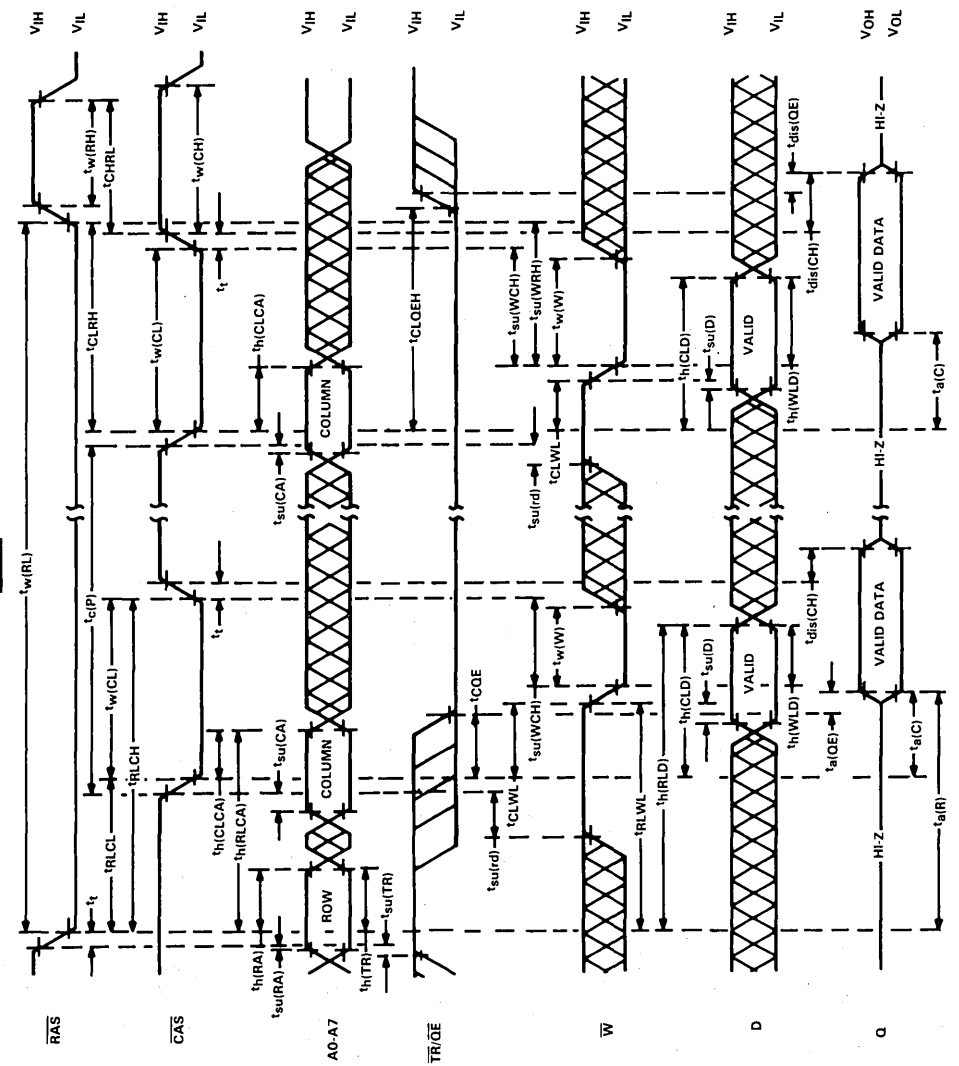
NOTES: 7. Timing is for non-multiplexed D, Q, and Address lines.
8. A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



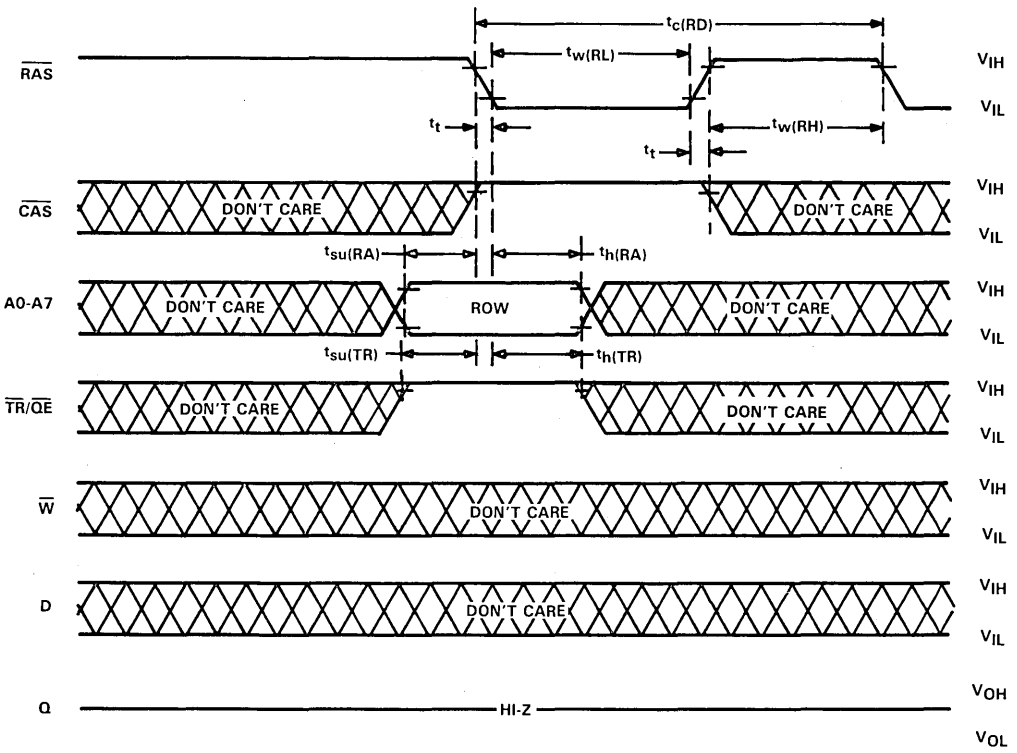
NOTES: 7. Timing is for non-multiplexed D, Q, and Address lines.
9. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

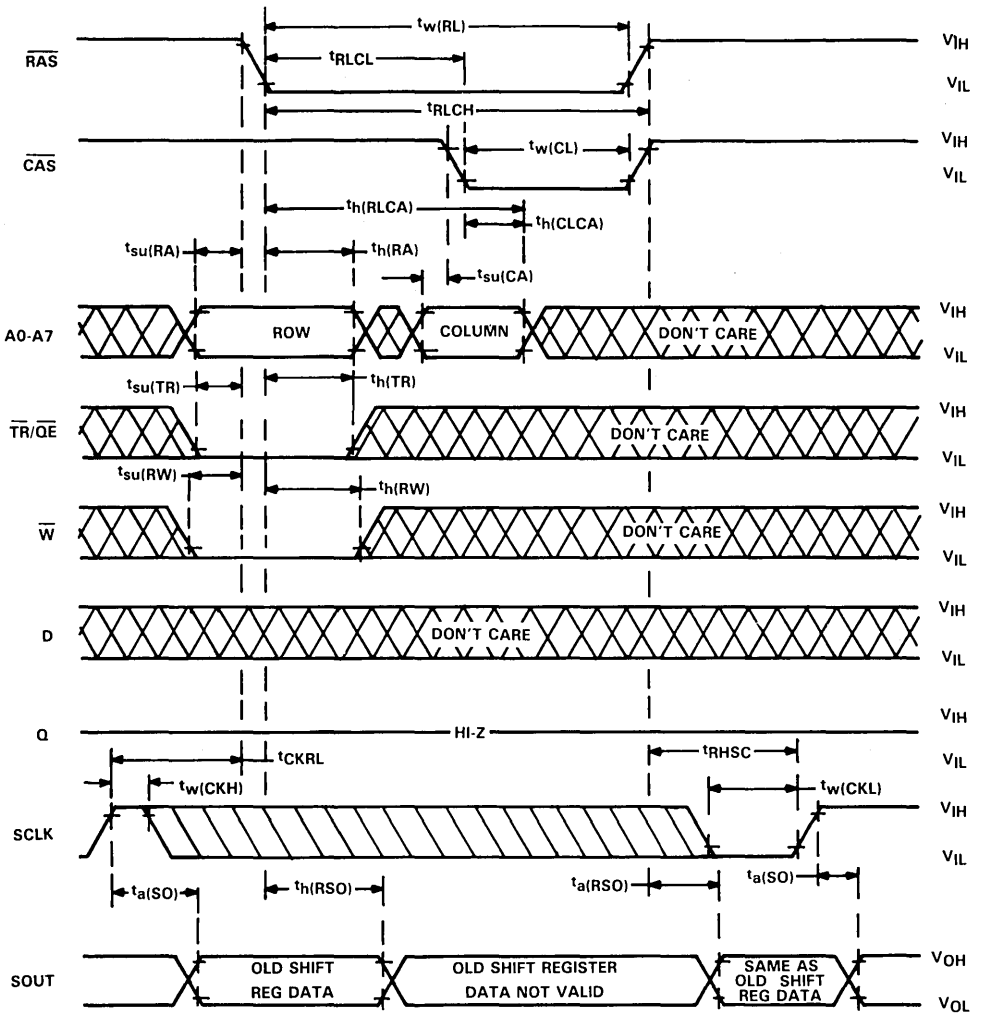


NOTES: 7. Timing is for non-multiplexed D, Q, and Address lines.
10. A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



shift register to memory timing



NOTES: 11. The shift register to memory cycle is used to transfer data from the shift register to the memory array. Every one of the 256 locations in the shift register is written into the 256 columns of the selected row. Note that the data that was in the shift register may have resulted either from a serial shift in or from a parallel load of the shift register from one of the memory rows.

12. $\overline{SOE}$ assumed low.

13. SCLK may be high or low during $t_{w(RL)}$.

14. Multiple transfer write cycles require either a 1-μs $\overline{RAS}$-precharge interval or any other active $\overline{RAS}$ cycle before initiation of the transfer write cycles and separation between any two consecutive transfer write cycles.

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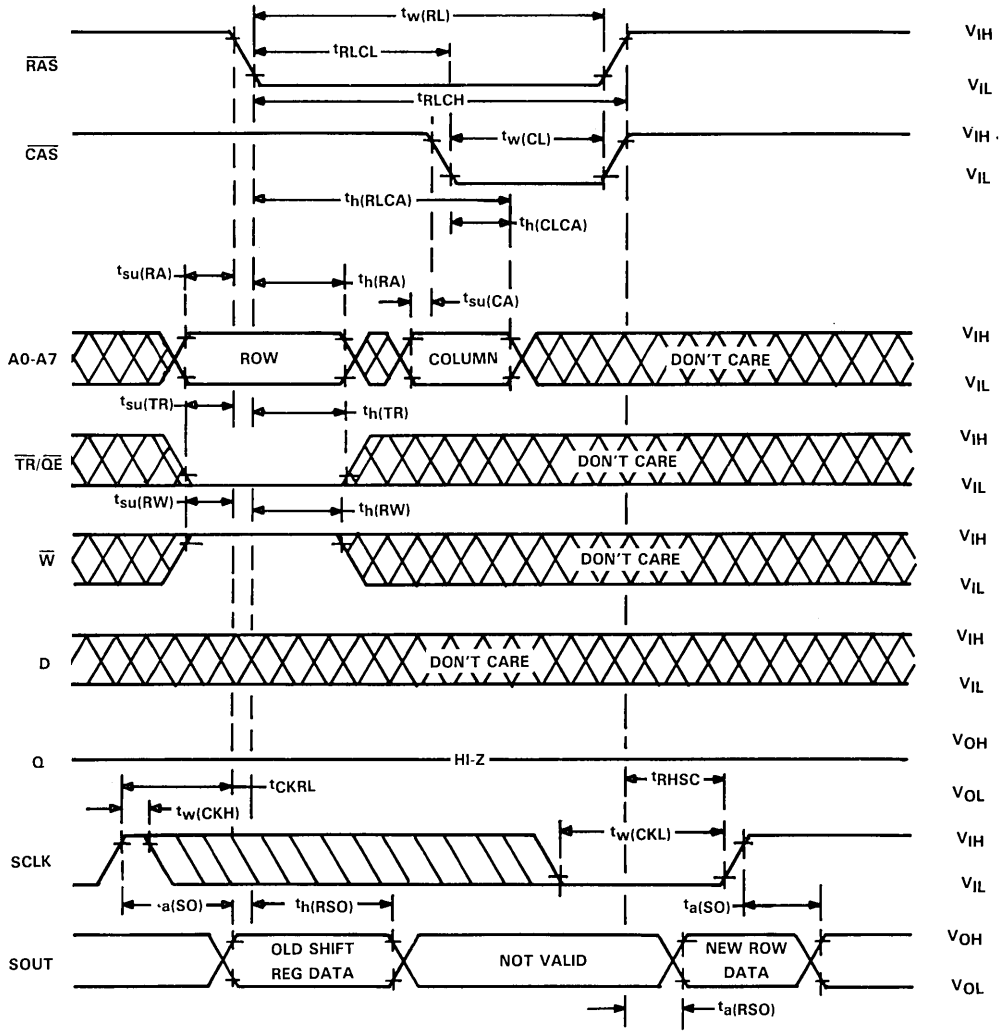
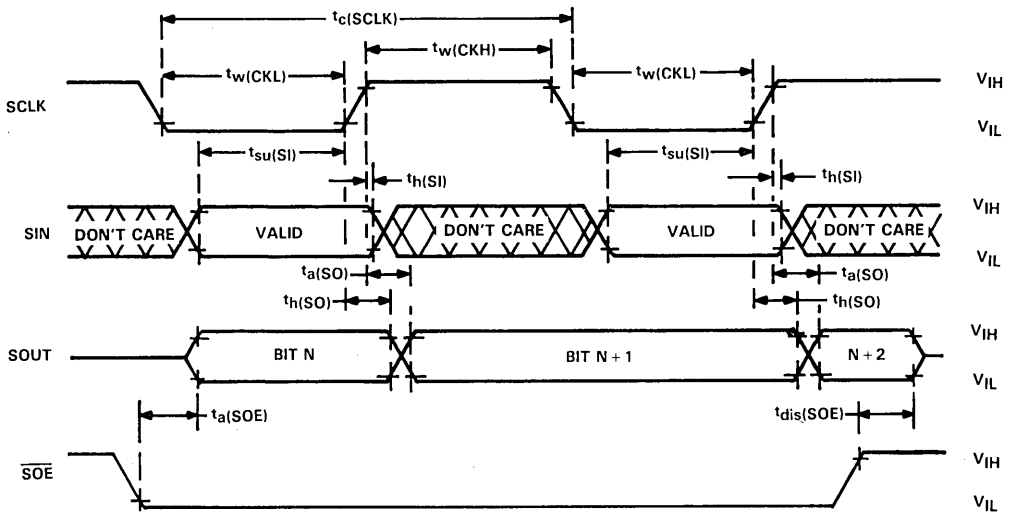
memory to shift register timing



NOTES: 12. $\overline{SOE}$ assumed low.

13. SCLK may be high or low during $t_{w(RL)}$.
14. Multiple transfer write cycles require either a 500-ns $\overline{RAS}$-precharge interval or any other active $\overline{RAS}$ cycle before initiation of the transfer write cycles and separation between any two consecutive transfer write cycles.
15. The memory to shift register cycle is used to load the shift register in parallel from the memory array. Every one of the 256 locations in the shift register are written into from the 256 columns of the selected row. Note that the data that is loaded into the shift register may be either shifted out or written back into another row.

serial data shift timing



NOTES: 4. $t_{c(SCLK)}$ min is tested by connecting SIN to SOUT and test conditions include $t_{SU(SI)}$; see paragraph entitled SIN and SOUT on page 5.

16. While shifting data through the serial shift register, the state of $\overline{TR}/\overline{QE}$ is a don't care as long as $\overline{TR}/\overline{QE}$ is held high when $\overline{RAS}$ goes low and $t_{su(TR)}$ and $t_{h(TR)}$ timings are observed. This requirement avoids the initiation of a register-to-memory or memory-to-register data transfer operation. The serial data transfer cycle is used to shift data in and/or out of the shift register.
17. When loading data into the shift register from the serial input in preparation for a shift-register-to-memory transfer operation, the serial clock must be clocked an even number of times.

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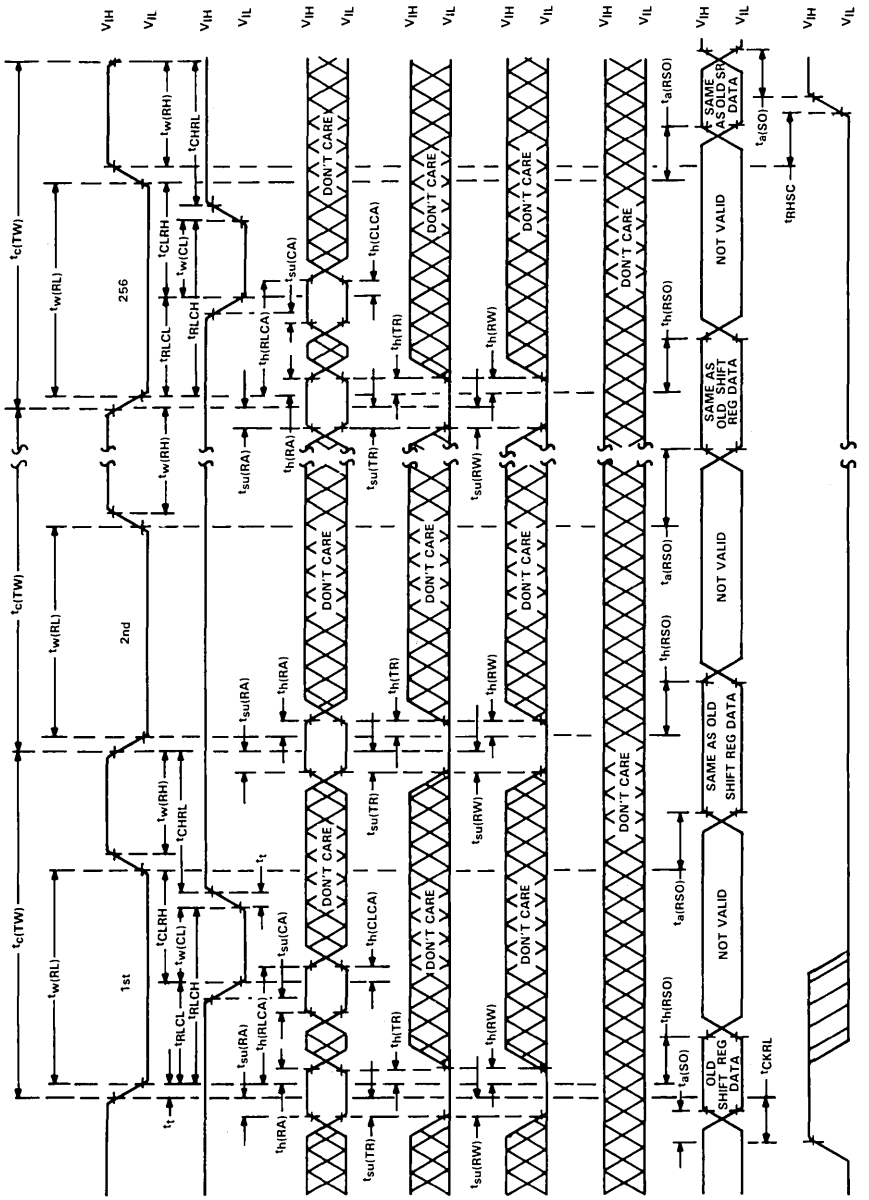
shift register to memory multiple timing



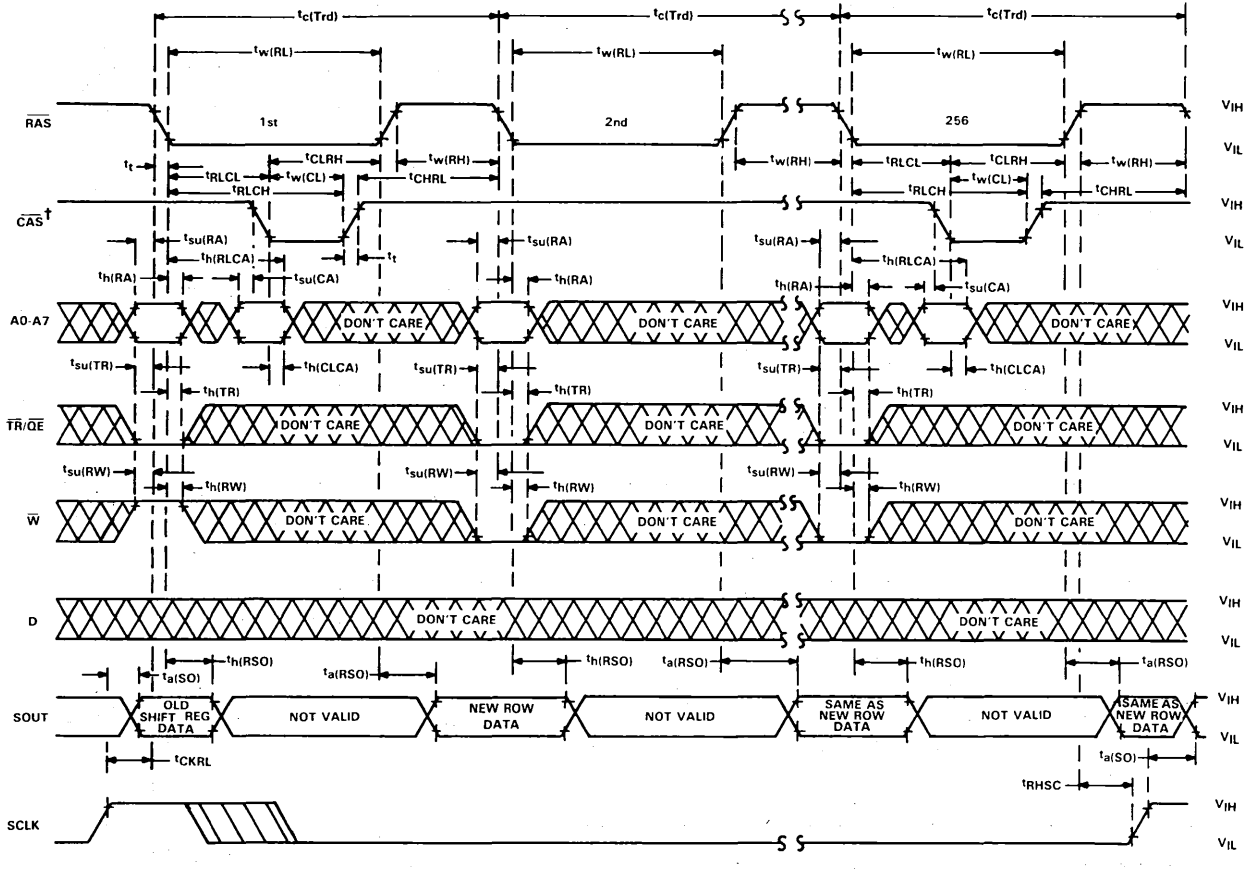
†CAS and register address need not be supplied every cycle, only when it is desired to change or select a new register length.

NOTES: 12. SOE assumed low.

18. The shift register to memory multiple cycle is used to write the shift register data to more than one row of the memory array. An application of this could be clearing all memory. To do this, the SIN line would be held at 0 to fill all locations in the shift register with 0s. The shift register would then be written into all 256 rows of the memory array in 256 cycles. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.

19. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to tCKRL prior to RAS falling with TR/QE low.

memory to shift register to memory multiple timing



†$\overline{CAS}$ and register address need not be supplied every cycle, only when it is desired to change from one register to another.

NOTES: 12. $\overline{SOE}$ assumed low.

19. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to t_{CKRL} prior to $\overline{RAS}$ falling with $\overline{TR/QE}$ low.
20. The memory to shift register to memory multiple cycle is used to reorder the rows within the memory array itself. First, the data in a row is stored in the shift register and then it is written into other selected rows. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.

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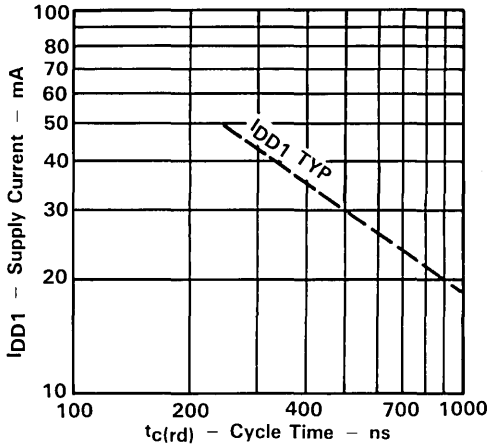
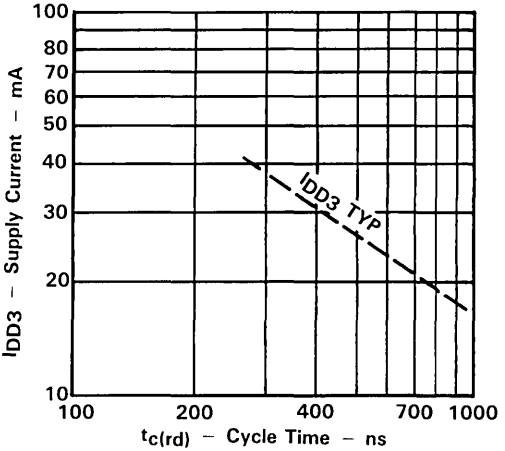
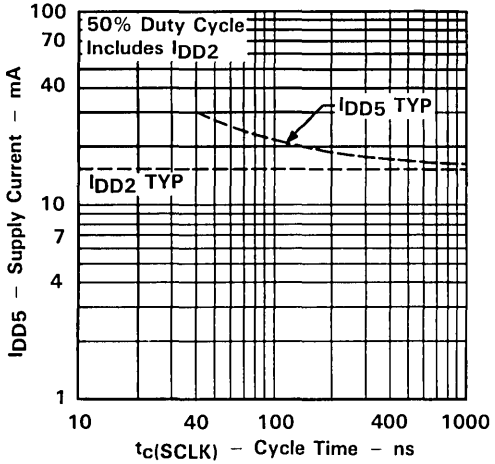
I_{DD1}
vs
CYCLE TIME



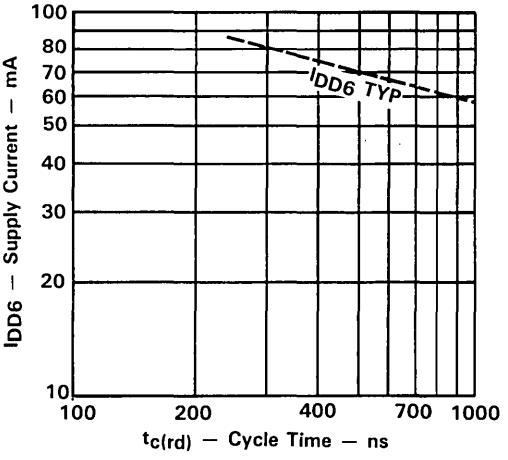
I_{DD3}
vs
CYCLE TIME



I_{DD5}
vs
CYCLE TIME



I_{DD6}
vs
CYCLE TIME



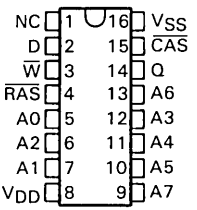
JULY 1985 – REVISED MAY 1988

- 65,536 × 1 Organization
- Single 5-V Supply (± 10% Tolerance)
- Upward Pin Compatible with '4116 (16K Dynamic RAM)
- Available Temperature Ranges with MIL-STD-883C High-Reliability Class B Processing:
  —S . . . −55°C to 110°C
  —L . . . 0°C to 70°C
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.8% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with Early Write Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  —Operating . . . 125 mW (Typ)
  —Standby . . . 17.5 mW (Typ)
- Performance Ranges:

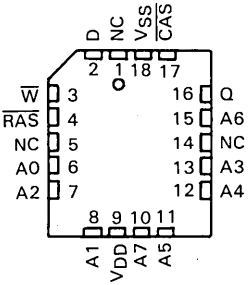
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
'4164-12	120 ns	70 ns	230 ns	260 ns
'4164-15	150 ns	85 ns	260 ns	285 ns
'4164-20	200 ns	135 ns	326 ns	345 ns

- SMOS (Scaled-MOS) N-Channel Technology

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

8 Military Products

description

The SMJ4164 is a Military high-speed, 65,536-bit, dynamic random-access memory, organized as 65,536 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The SMJ4164 features $\overline{RAS}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation is 125 mW typical operating and 17.5 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 54/74 TTL. All address lines and data in are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility. Pin 1 has no internal connection to allow compatibility with other 64K RAMs that use this pin for an additional function.

The SMJ4164 is offered in a 16-pin dual-in-line ceramic sidebraze package (JD suffix) and in a leadless ceramic chip carrier package (FG suffix). The JD package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers, whereas the FG package is intended for surface mounting on solder lands on 1,27-mm (0.050-inch) centers. The FG package is a three-layer, 18-pad, rectangular ceramic chip carrier with dimensions of 7,37 × 10,8 × 1,65 mm (0.290 × 0.425 × 0.065 inches).

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 54/74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

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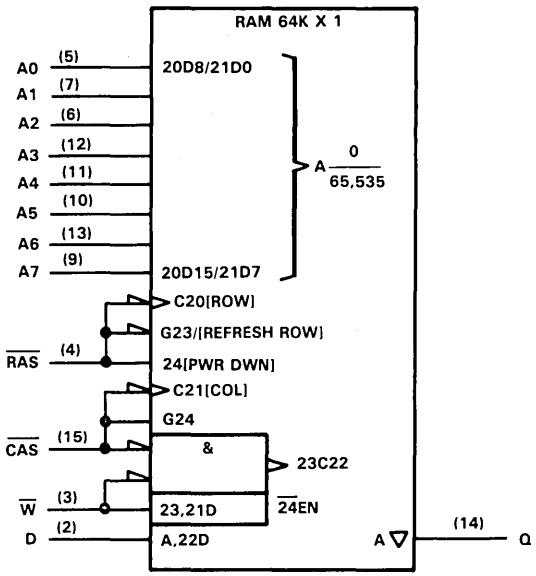
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to set up and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

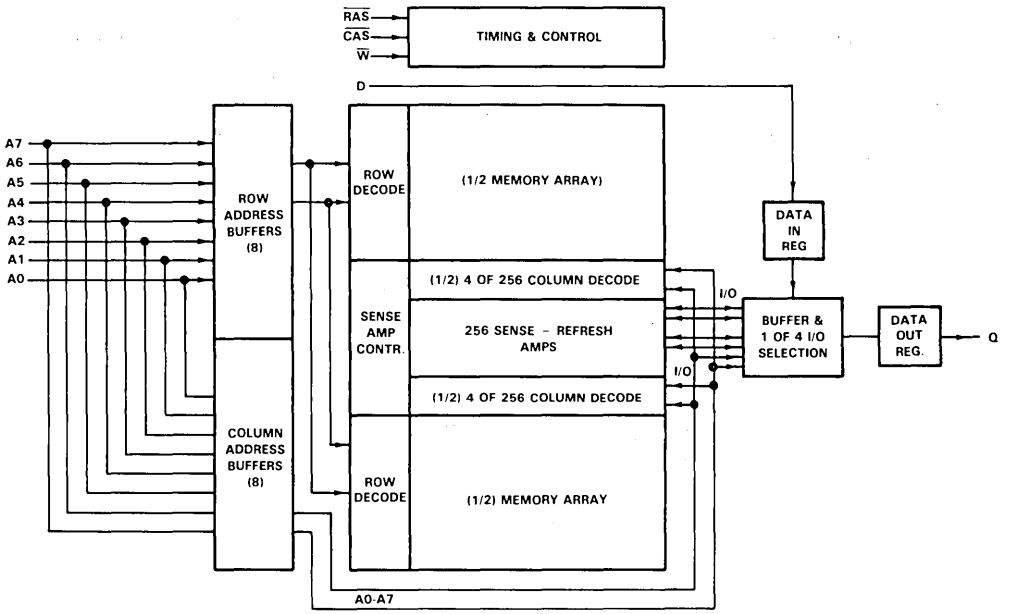
After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the dual-in-line package.

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1)	−1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS}	−1 V to 6 V
Short circuit output current	50 mA
Power dissipation	1 W
Minimum operating free-air temperature: S version	−55°C
L version	0°C
Operating case temperature: S version	110°C
L version	70°C
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

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recommended operating conditions

		S VERSION			L VERSION			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{DD}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{SS}	Supply voltage		0			0		V
V_{IH}	High-level input voltage	2.4		$V_{CC}+0.3$	2.4		$V_{CC}+0.3$	V
V_{IL}	Low-level input voltage (see Notes 3 and 4)	−0.6		0.8	−0.6		0.8	V
T_A	Operating free-air temperature	−55			0			°C
T_C	Operating case temperature			110			70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions must comprehend this occurrence.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4164-12			SMJ4164-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5.5 V, All outputs open			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		40	48		35	45	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		3.5	5		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		28	40		25	37	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		28	40		25	37	mA

†All typical values are at T_C = 25°C and nominal supply voltages.
‡Additional information on last page of data sheet.
§V_{IL} ≤ −0.6 V.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4164-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5.5 V, Output = open			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle All outputs open		27	37	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		20	32	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		20	32	mA

†All typical values are at T_C = 25°C and nominal supply voltages.
‡Additional information on last page of data sheet.
§V_{IL} > −0.6 V.

capacitance over recommended supply voltage range and recommended temparature range, f = 1 MHz¶

PARAMETER		SMJ4164		UNIT
		TYP†	MAX	
$C_{i(A)}$	Input capacitance, address inputs	4	7	pF
$C_{i(D)}$	Input capacitance, data input	4	7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
C_o	Output capacitance	5	8	pF

†All typical values are at T_C = 25°C and nominal supply voltages.
¶These parameters are guaranteed but not tested.

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switching characteristics over recommended supply voltage range and recommended operating temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4164-12		SMJ4164-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 80 pF, see Figure 1	t_{CAC}		70		85	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	C_L = 80 pF, t_{RLCL} = MAX, see Figure 1	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 80 pF, see Figure 1	t_{OFF}	0	40	0	40	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4164-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 80 pF, see Figure 1	t_{CAC}		135	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	C_L = 80 pF, t_{RLCL} = MAX, see Figure 1	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 80 pF, see Figure 1	t_{OFF}	0	50	ns

timing requirements over recommended supply voltage range and recommended operating temperature range

PARAMETER		ALT. SYMBOL	SMJ4164-12		SMJ4164-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	130		160		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	260		285		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	70	10,000	85	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		45		ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	−5		−5		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	50		50		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	50		50		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	40		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	85		95		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	40		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	85		95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	40		45		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high‖	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high‖	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	40		45		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	85		95		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	70		85		ns

Continued next page.

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns. The recommended rise and fall times for the $\overline{CAS}$ and $\overline{RAS}$ inputs are a minimum of 3 ns and a maximum of 50 ns.

‡Page-mode only.

§In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

¶In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

‖These parameters are guaranteed but not tested.

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timing requirements over recommended supply voltage range and recommended operating temperature range (continued)

PARAMETER		ALT. SYMBOL	SMJ4164-12		SMJ4164-15		UNIT
			MIN	MAX	MIN	MAX	
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	40		60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	15	45	20	50	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	85		100		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

timing requirements over recommended supply voltage range and recommended operating temperature range (continued)

PARAMETER		ALT. SYMBOL	SMJ4164-20		UNIT
			MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	225		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	55		ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	−5		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	80		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	80		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	140		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	145		ns

Continued next page.

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns. The recommended rise and fall times for the $\overline{CAS}$ and $\overline{RAS}$ inputs are a minimum of 3 ns and a maximum of 50 ns.

‡Page-mode only.

§In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

¶In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and recommended operating temperature range (concluded)

PARAMETERS		ALT. SYMBOL	SMJ4164-20		UNIT
			MIN	MAX	
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high‖	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high‖	t_{RRH}	5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	80		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	145		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	65		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	130		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

‖These parameters are guaranteed but not tested.

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PARAMETER MEASUREMENT INFORMATION

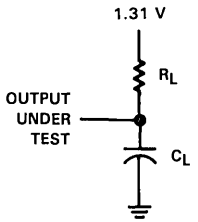
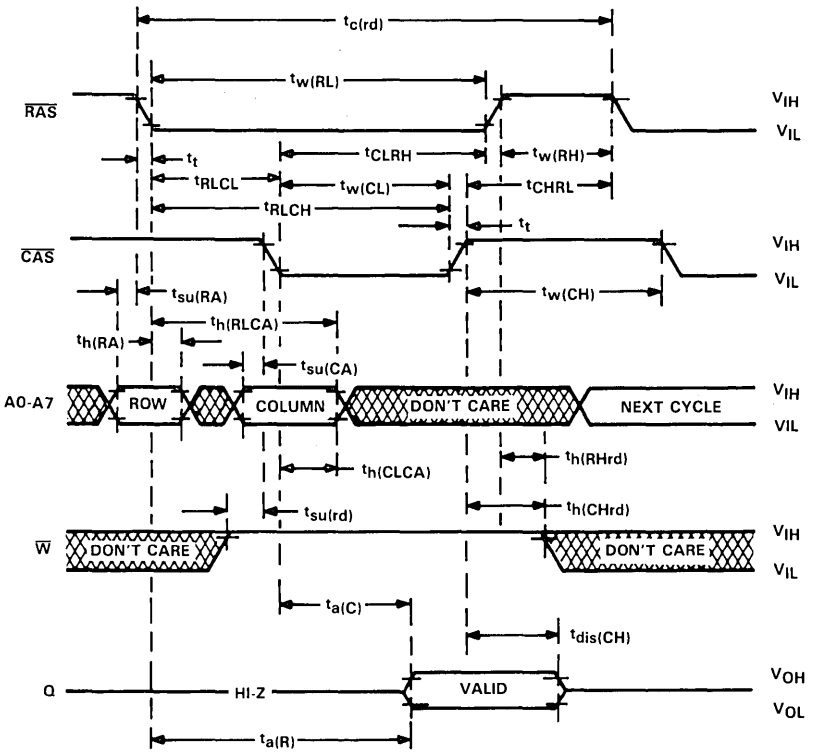
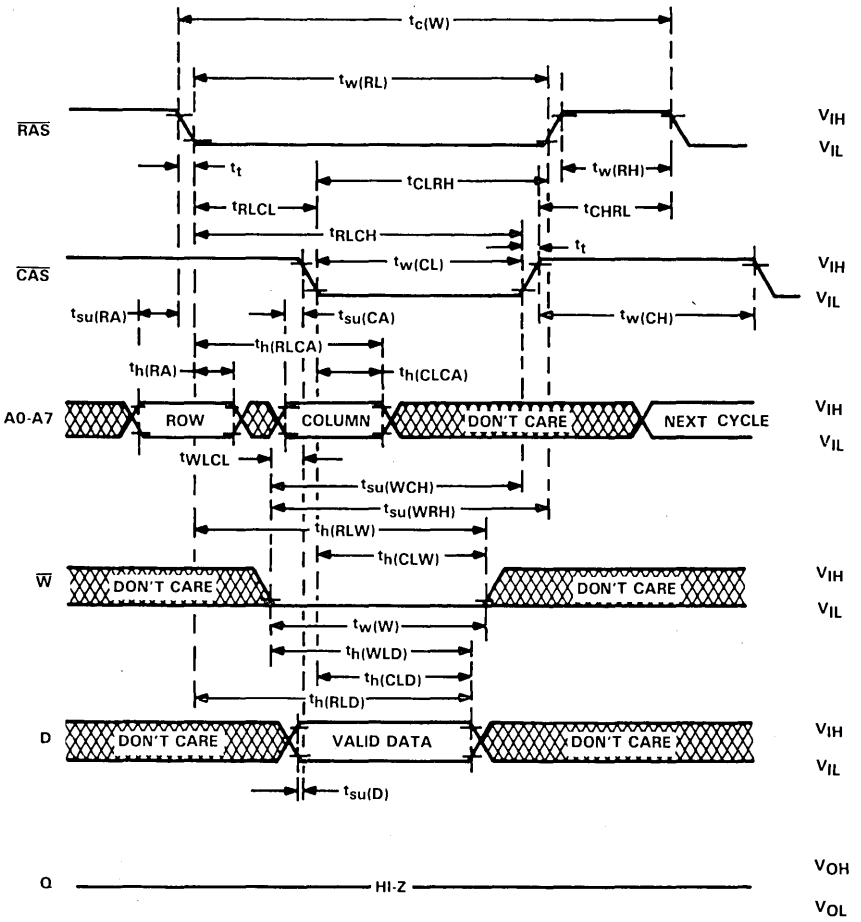


FIGURE 1. LOAD CIRCUIT

read cycle timing



early write cycle timing



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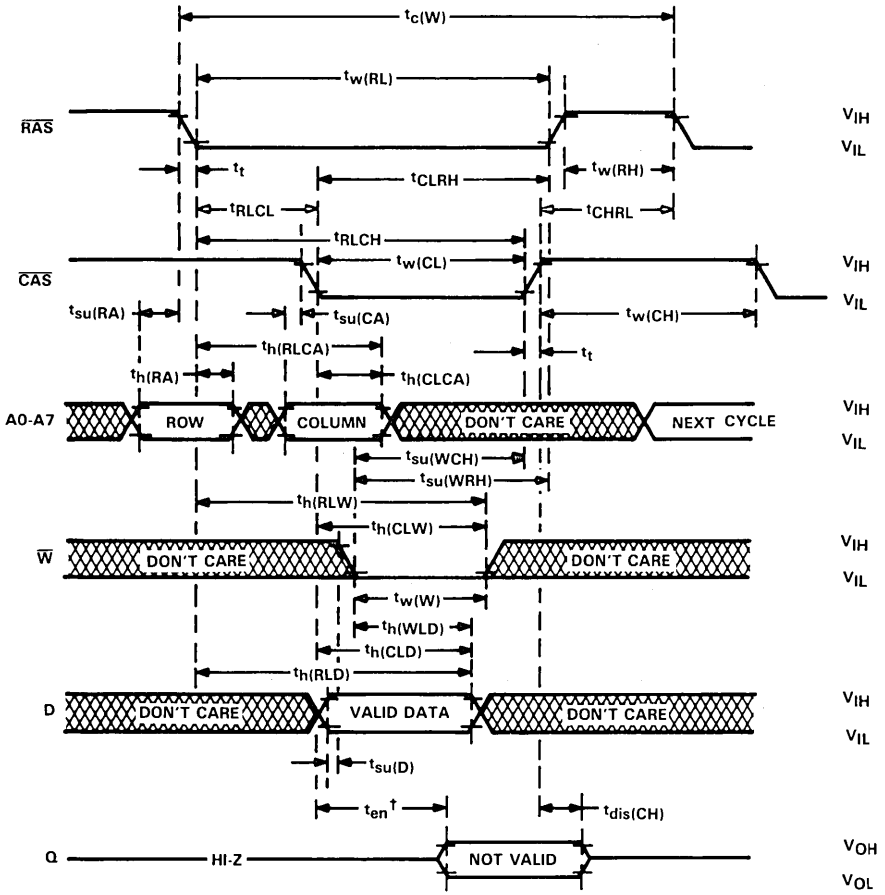
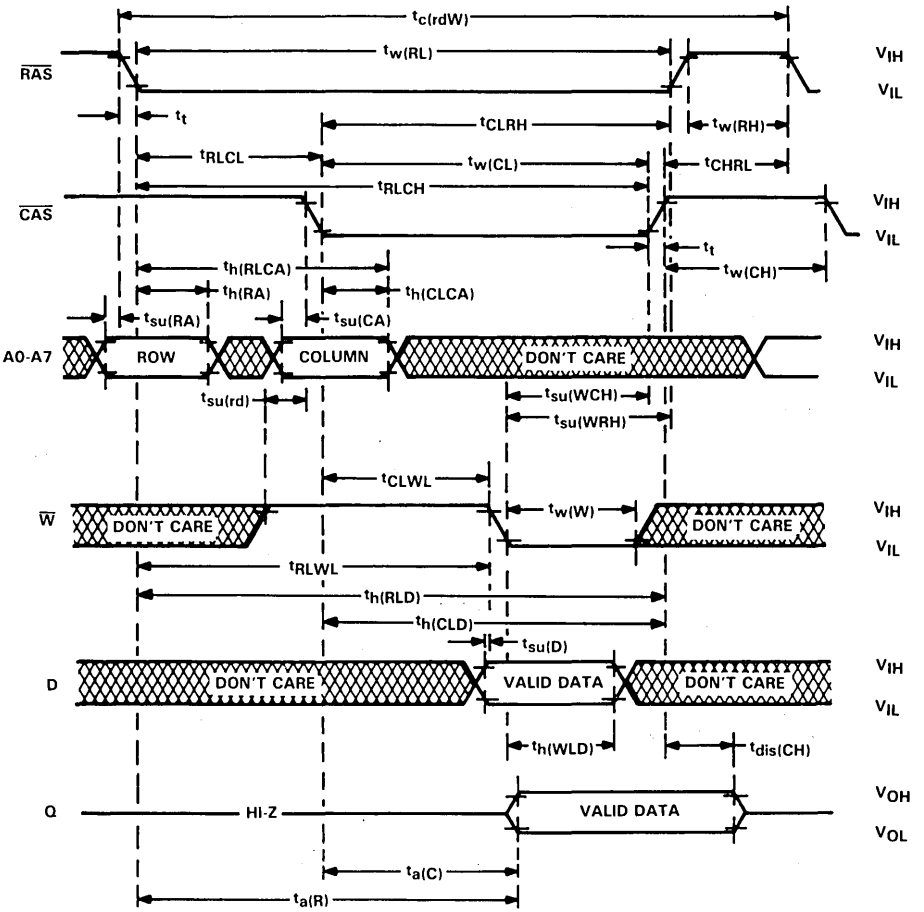
write cycle timing



read-write/read-modify-write cycle timing



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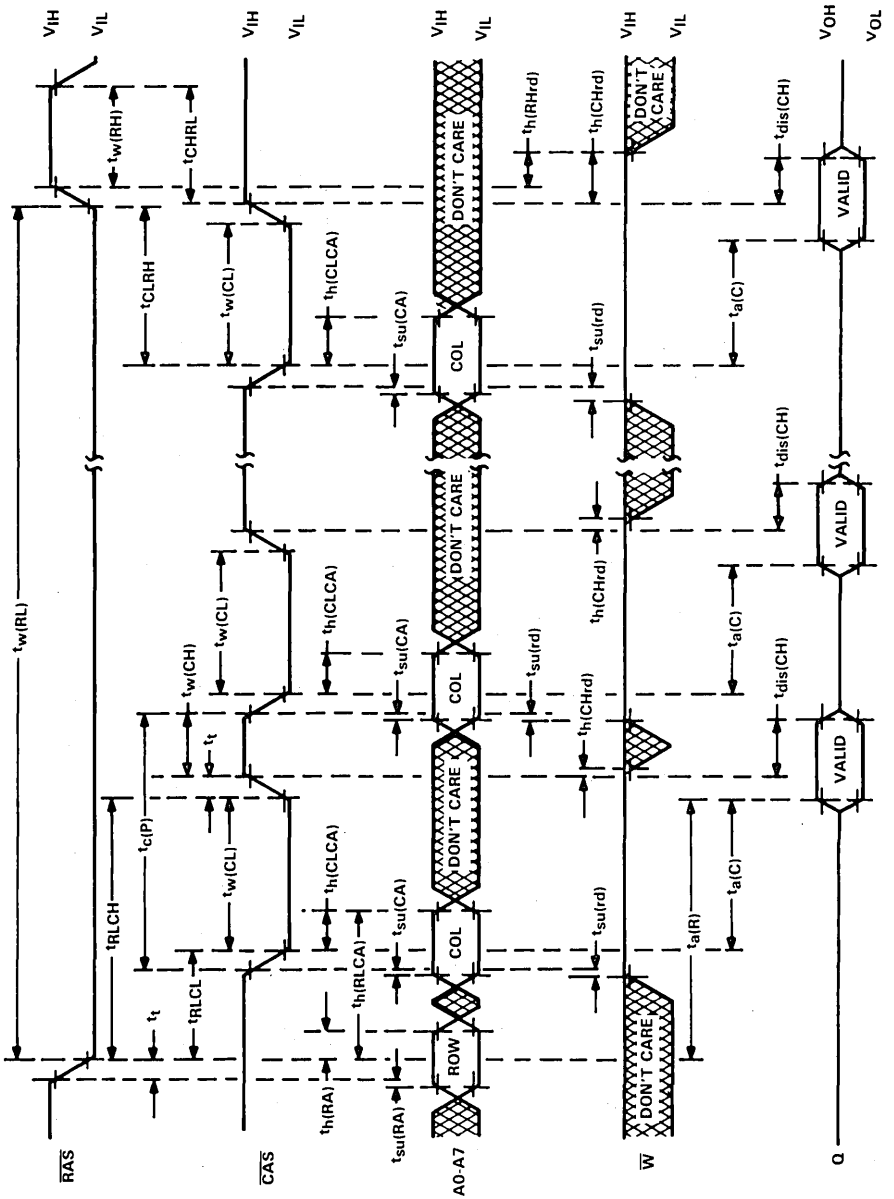
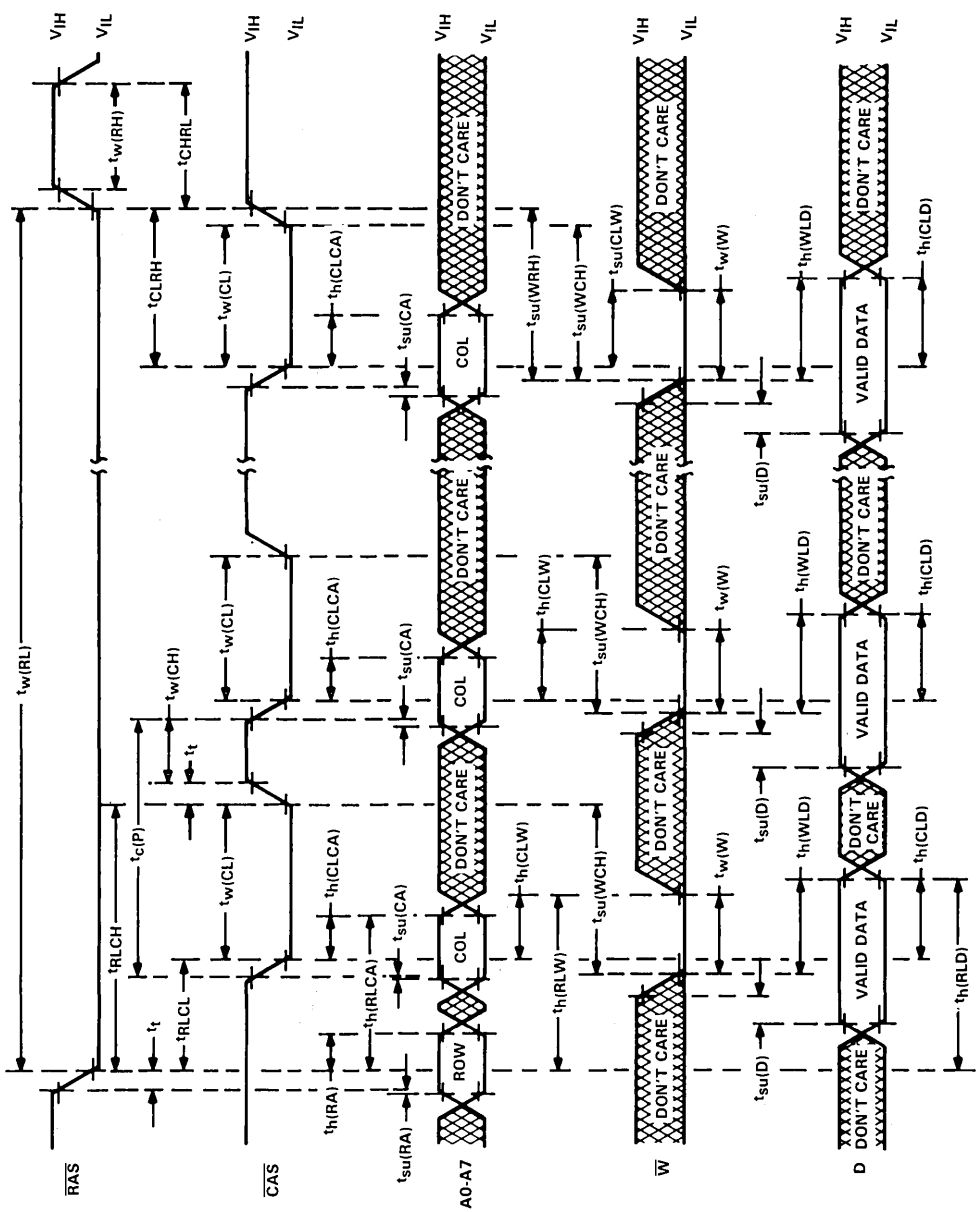
page-mode read cycle timing



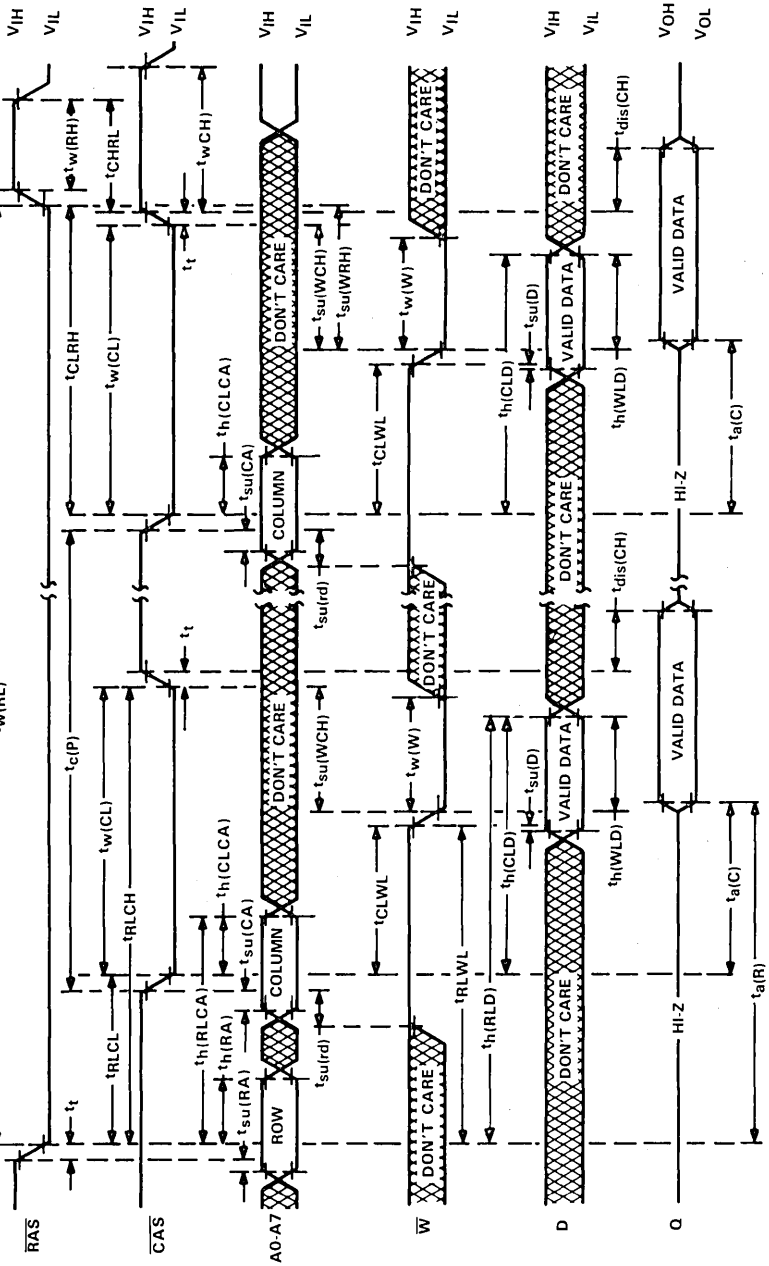
NOTE 5: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



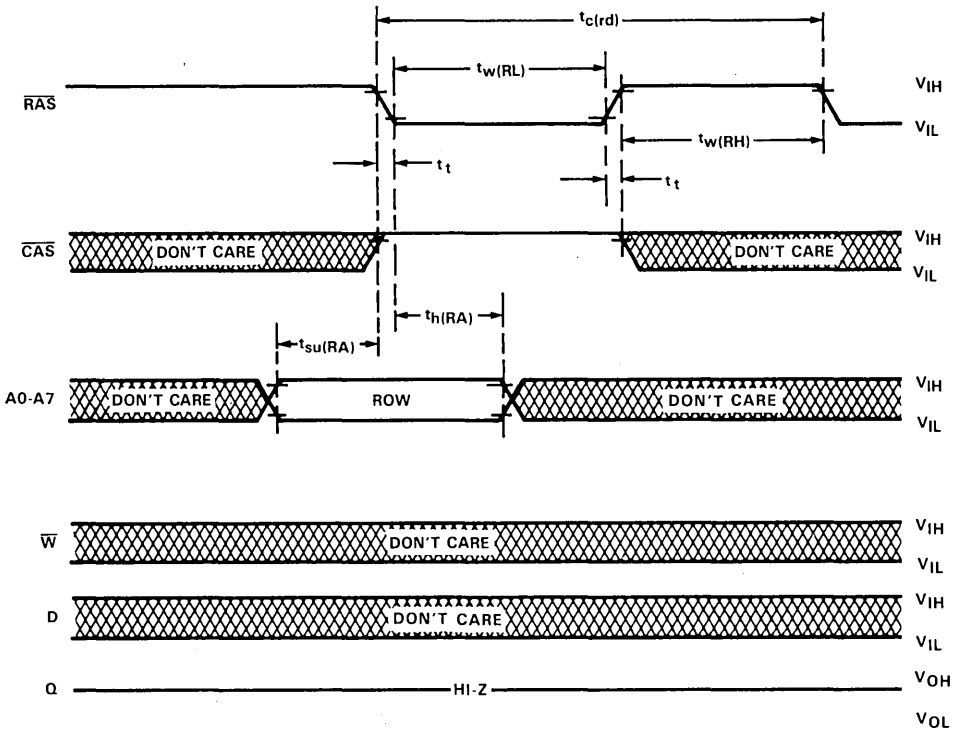
NOTE 6: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

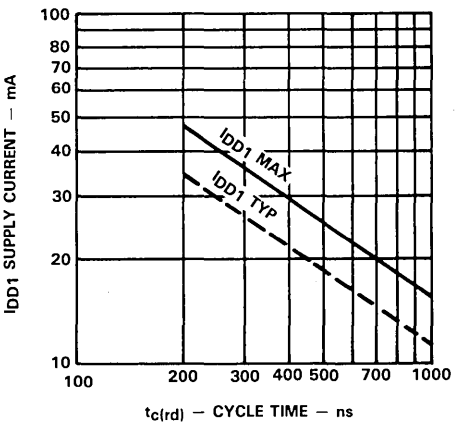


NOTE 7: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and the write timing specifications are not violated.

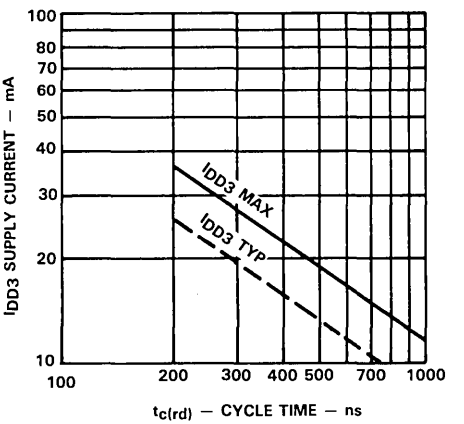
$\overline{\text{RAS}}$-only refresh timing



I_{DD1} vs. CYCLE TIME



I_{DD3} vs. CYCLE TIME



8 Military Products

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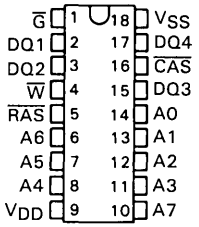
AUGUST 1980 – REVISED FEBRUARY 1988

- 16,384 × 4 Organization
- Single 5-V Supply (±10% Tolerance)
- Performance Ranges

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
'4416-12	120 ns	70 ns	230 ns	320 ns
'4416-15	150 ns	80 ns	260 ns	330 ns
'4416-20	200 ns	120 ns	330 ns	440 ns

- Available Temperature Ranges with MIL-STD-883C Class B High-Reliability Processing
  —S . . . −55°C to 100°C
  —L . . . 0°C to 70°C
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.7% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs
- Early Write or $\overline{G}$ to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  —Operation . . . 200 mW (Typ)
  —Standby . . . 17.5 mW (Typ)
- SMOS (Scaled-MOS) N-Channel Technology

JD PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The SMJ4416 is a Military high-speed, 65,536-bit, dynamic random-access memory organized as 16,384 words of 4 bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The SMJ4416 features $\overline{RAS}$ access times to 150 ns maximum. Power dissipation is 200 mW typical operating, 17.5 mW typical standby.

SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks have been reduced to 60 mA typical, and a −1 V input voltage undershoot can be tolerated, minimizing system noise considerations. Input clamp diodes are used to ease system design.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 54/74 TTL. All address lines and data in are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ4416 is offered in 18-pin 300-mil ceramic side-braze dual-in-line package. It is available in −55°C to 100°C and 0°C to 70°C temperature ranges. Dual-in-line packages are designed for insertion in mounting-hole rows on 7,62 mm (300-mil) centers.

operation

address (A0 through A7)

Fourteen address bits are required to decode 1 of 16,384 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the six column-address bits are set up on pins A1 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state allowing a write cycle with $\overline{G}$ grounded.

data in (DQ1 through DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In delayed write or read-modify-write, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1 through DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 54/74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(E)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high-impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying t_{GHD}.

output enable ($\overline{G}$)

The $\overline{G}$ signal controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until $\overline{G}$ or $\overline{CAS}$ is brought high.

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refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

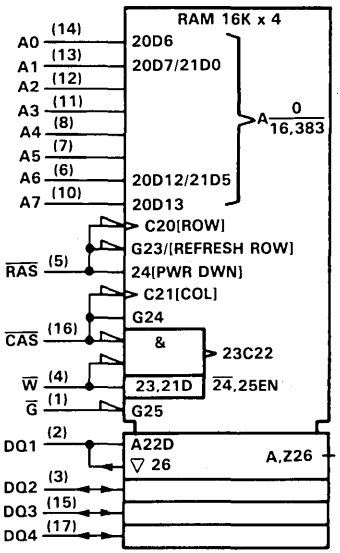
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to set up and strobe sequential row addresses for the same page is eliminated. To extend beyond the 64 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 16K × 4 RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

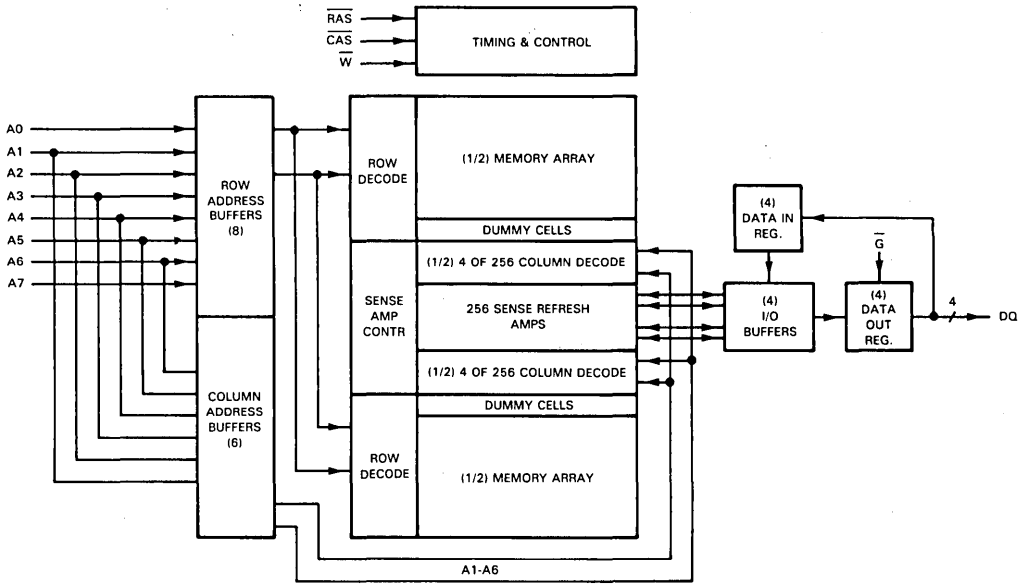
After power up, the power supply must remain at its steady-state value for 1 ms. In addition, the $\overline{RAS}$ input must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the dual-in-line package.

functional block diagram



8

Military Products

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Minimum operating free-air temperature: S version . . . . . −55°C
L version . . . . . 0°C
Operating case temperature: S version . . . . . 100°C
L version . . . . . 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1. All voltage values in this data sheet are with respect to V_{SS}.

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refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

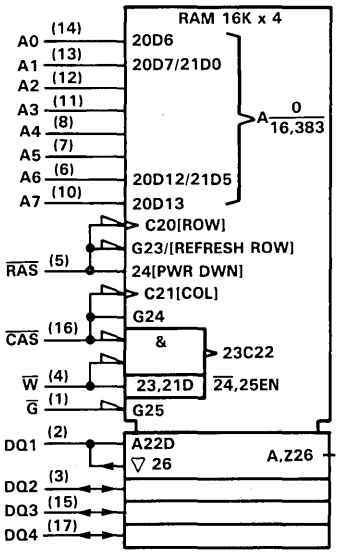
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to set up and strobe sequential row addresses for the same page is eliminated. To extend beyond the 64 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 16K × 4 RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

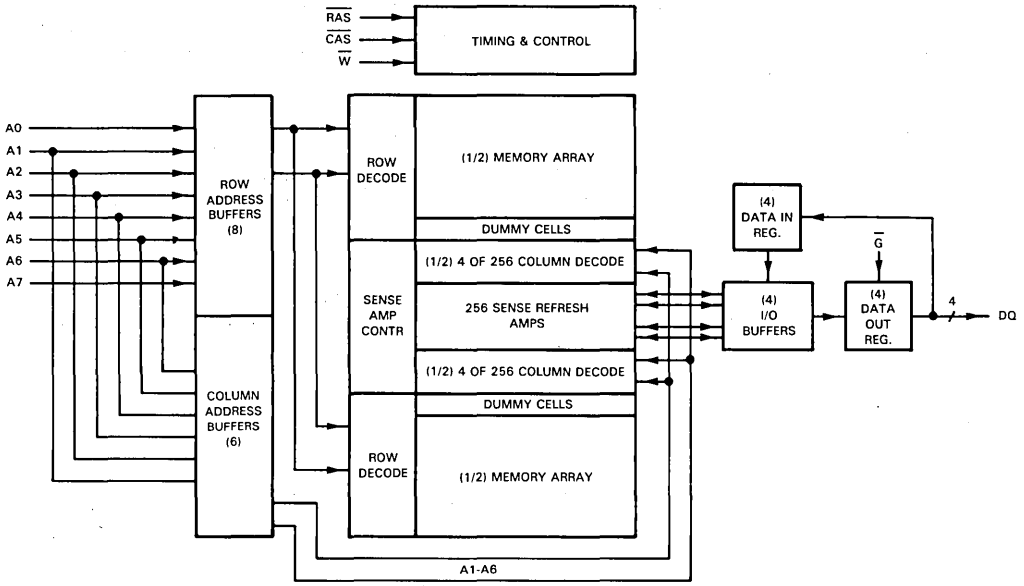
After power up, the power supply must remain at its steady-state value for 1 ms. In addition, the $\overline{RAS}$ input must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the dual-in-line package.

functional block diagram



8

Military Products

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Minimum operating free-air temperature: S version . . . . . −55°C
L version . . . . . 0°C
Operating case temperature: S version . . . . . 100°C
L version . . . . . 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1. All voltage values in this data sheet are with respect to V_{SS}.

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recommended operating conditions

			S VERSION			L VERSION			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{DD}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{SS}	Supply voltage			0			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		5.8	2.4		5.8	
V_{IL}	Low-level input voltage		−0.6		0.8	−0.6		0.8	V
T_A	Operating free-air temperature		−55			0			°C
T_C	Operating case temperature				100			70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions must comprehend this occurrence.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	SMJ4416-15			SMJ4416-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −2 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	At t_c = minimum cycle		40	48		35	42	mA
I_{DD2}‡	Standby current (see Note 4)	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high		25	40		21	34	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		25	40		21	34	mA

†All typical values are at T_C = 25°C and nominal supply voltages.
‡I_{DD1}-I_{DD4} are measured with open outputs.
NOTE 4. $V_{IL} \geq -0.6$ V on all inputs.

capacitance over recommended supply voltage range and recommended temparature range, f = 1 MHz§

PARAMETER		SMJ4416		UNIT
		TYP†	MAX	
$C_{i(A)}$	Input capacitance, address inputs	5	7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
$C_{i/o}$	Input/output capacitance, data ports	8	10	pF

†All typical values are at T_C = 25°C and nominal supply voltages.
§These parameters are guaranteed but not tested.

switching characteristics over recommended supply voltage range and recommended operating temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4416-15		SMJ4416-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{CAC}		70		120	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{RAC}		150		200	ns
$t_{a(G)}$	Access time after $\overline{G}$ low	C_L = 100 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA			40		50	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, I_{OH} = 5 mA, I_{OL} = 4.2 mA	t_{OFF}	0	30	0	40	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA		0	30	0	40	ns

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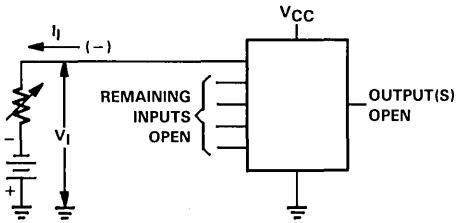
timing requirements over recommended supply voltage range and recommended operating temperature range

PARAMETER		ALT. SYMBOL	SMJ4416-15		SMJ4416-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	140		210		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	360		440		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	70	5000	120	5000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	150	5000	200	5000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		50		ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	70		80		ns
$t_{su(WCH)R}$	Write-command setup time before $\overline{CAS}$ high for RMW cycles		60		80		ns
$t_{su(RMW)R}$	Write-command setup time before $\overline{RAS}$ high for RMW cycles		60		80		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	70		80		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	40		50		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	110		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	50		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	130		160		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	40		50		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high‖	t_{RRH}	10		10		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high‖	t_{RCH}	0		0		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	50		80		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	130		160		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	70		120		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{CWD}	110		170		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	70	80	70	80	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{RWD}	190		250		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ		30		40		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

†All cycle times assume t_t = 5 ns.
‡Page mode only.
§In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$.
¶In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition time, this may require additional $\overline{RAS}$ low time $t_{w(RL)}$.
‖These parameters are guaranteed but not tested.
#Necessary to insure $\overline{G}$ has disabled the output buffers prior to applying data to the device.

PARAMETER MEASUREMENT INFORMATION



NOTE 5. Each input is tested separately.

FIGURE 1. INPUT CLAMP VOLTAGE TEST CIRCUIT

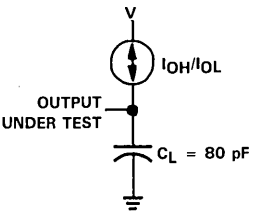
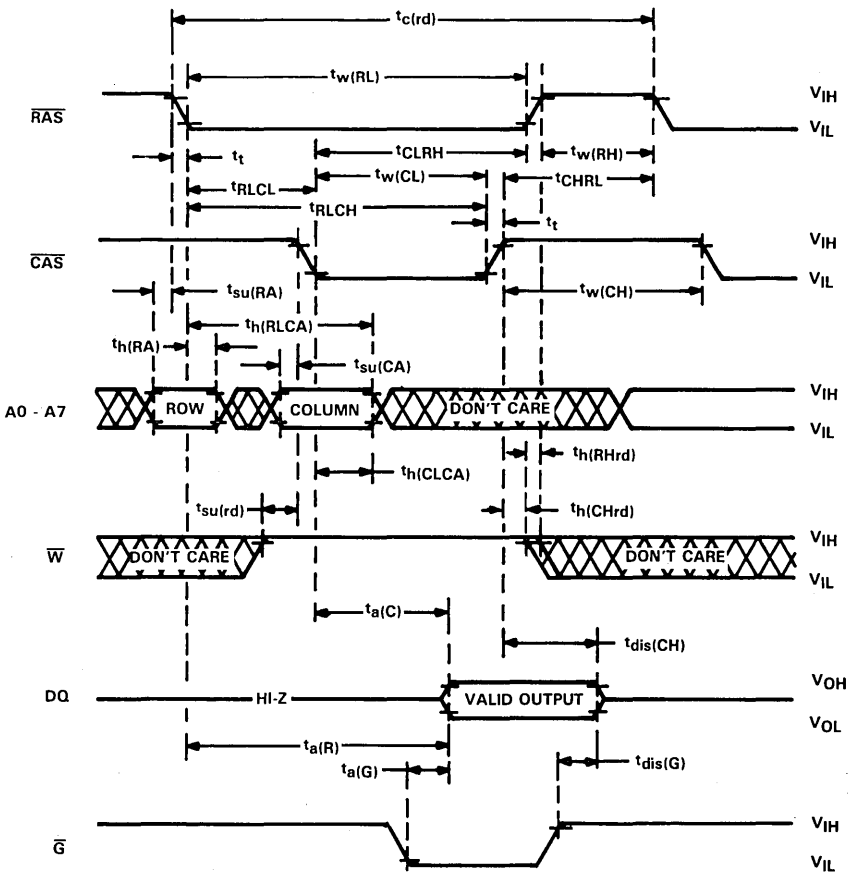


FIGURE 2. EQUIVALENT LOAD CIRCUIT

read cycle timing



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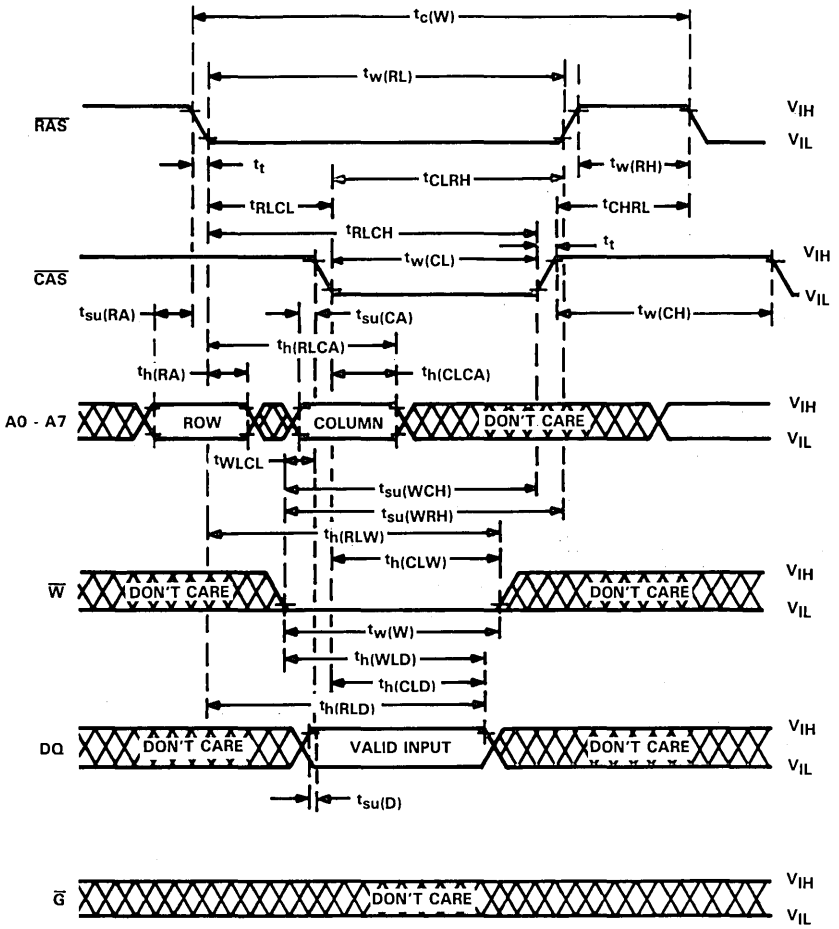
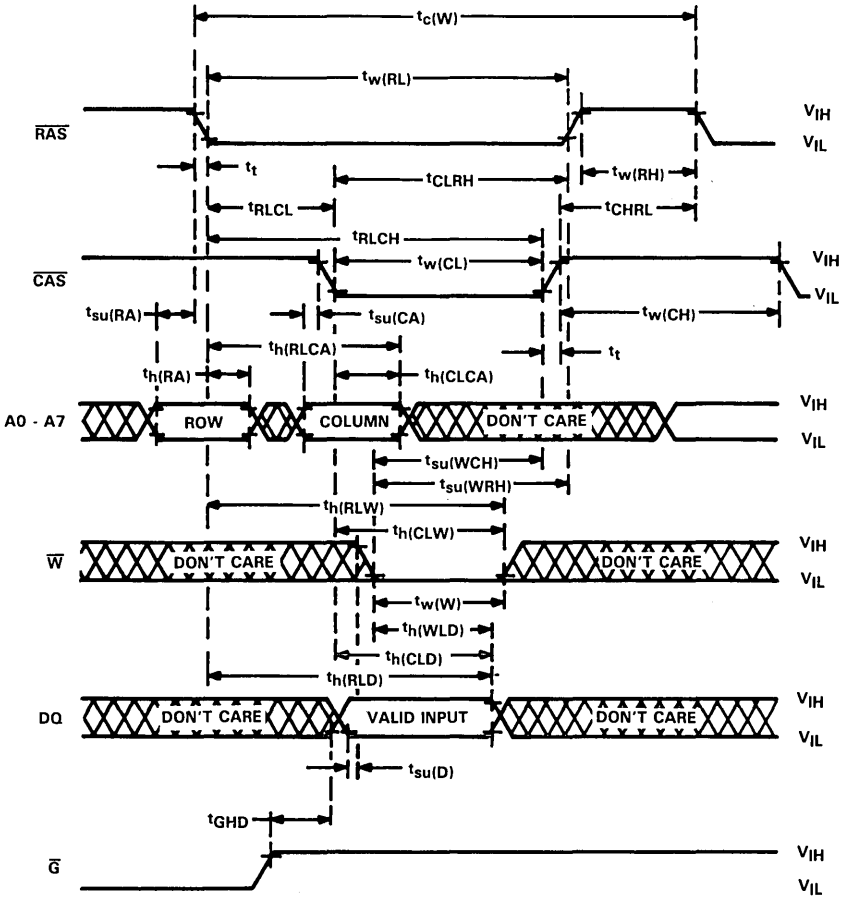
early write cycle timing



write cycle timing



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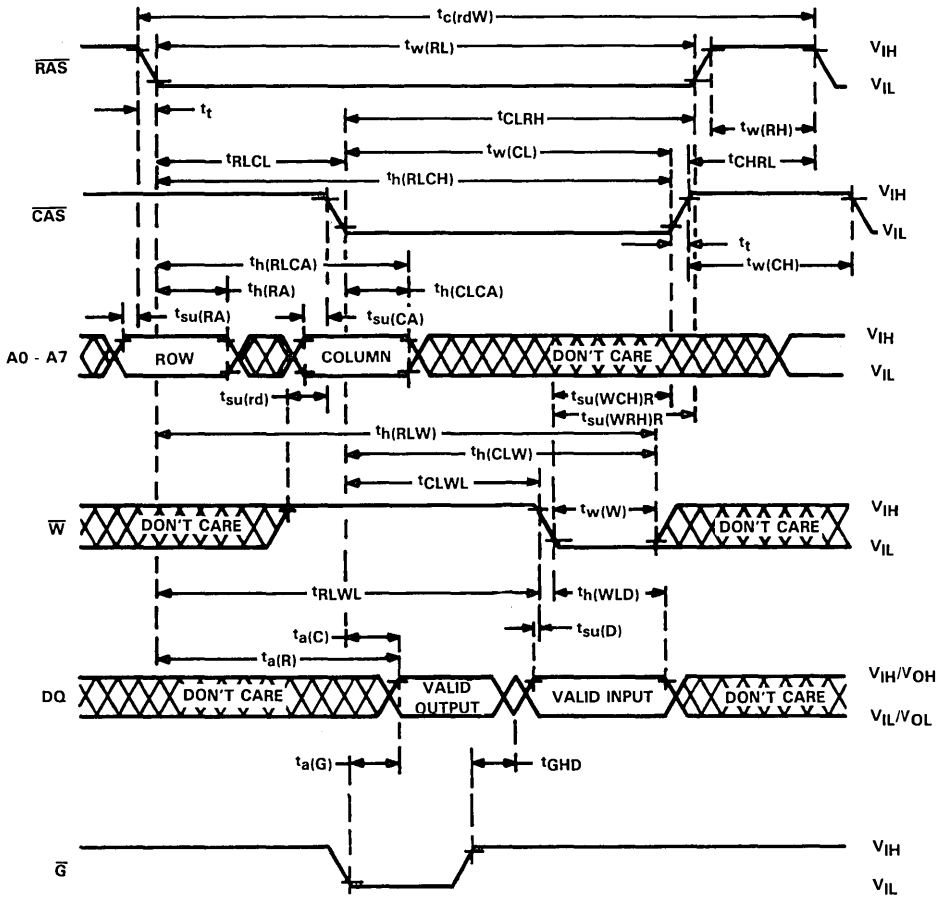
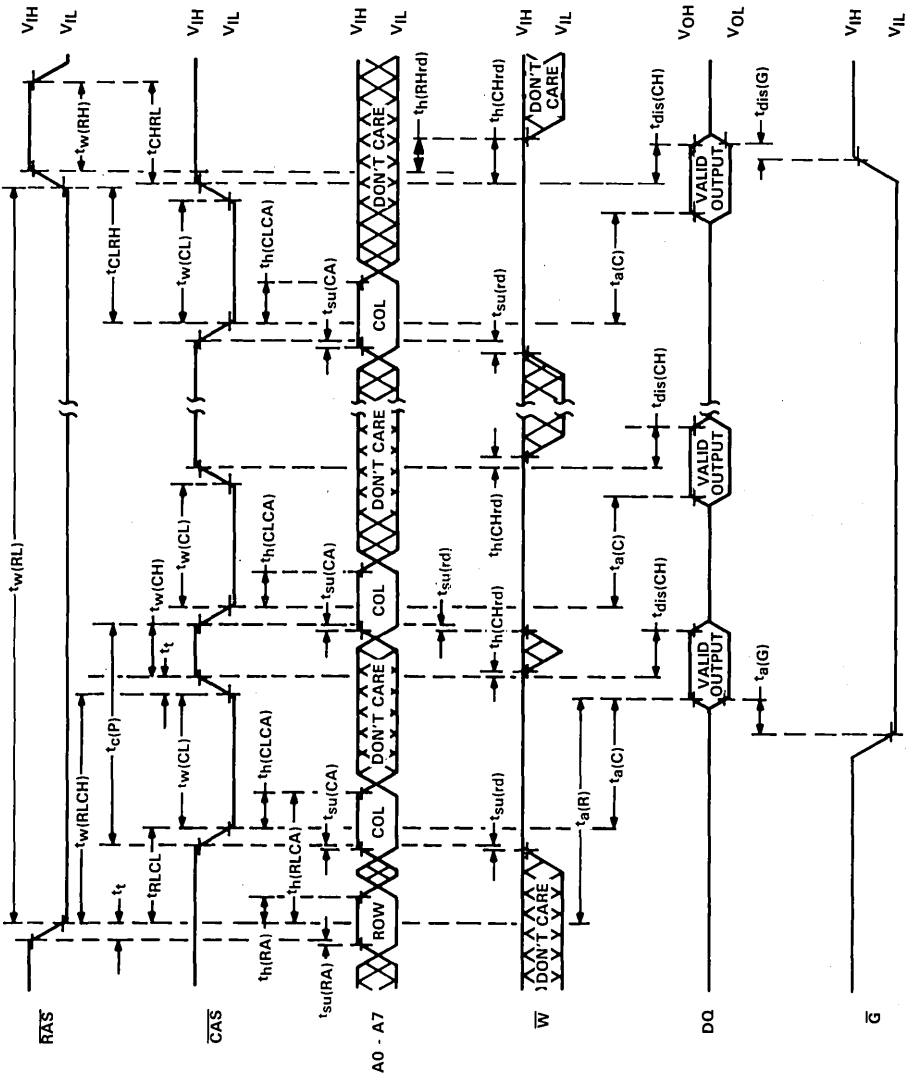
read-write/read-modify-write cycle timing



page-mode read cycle timing



NOTE 6. A write cycle or read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

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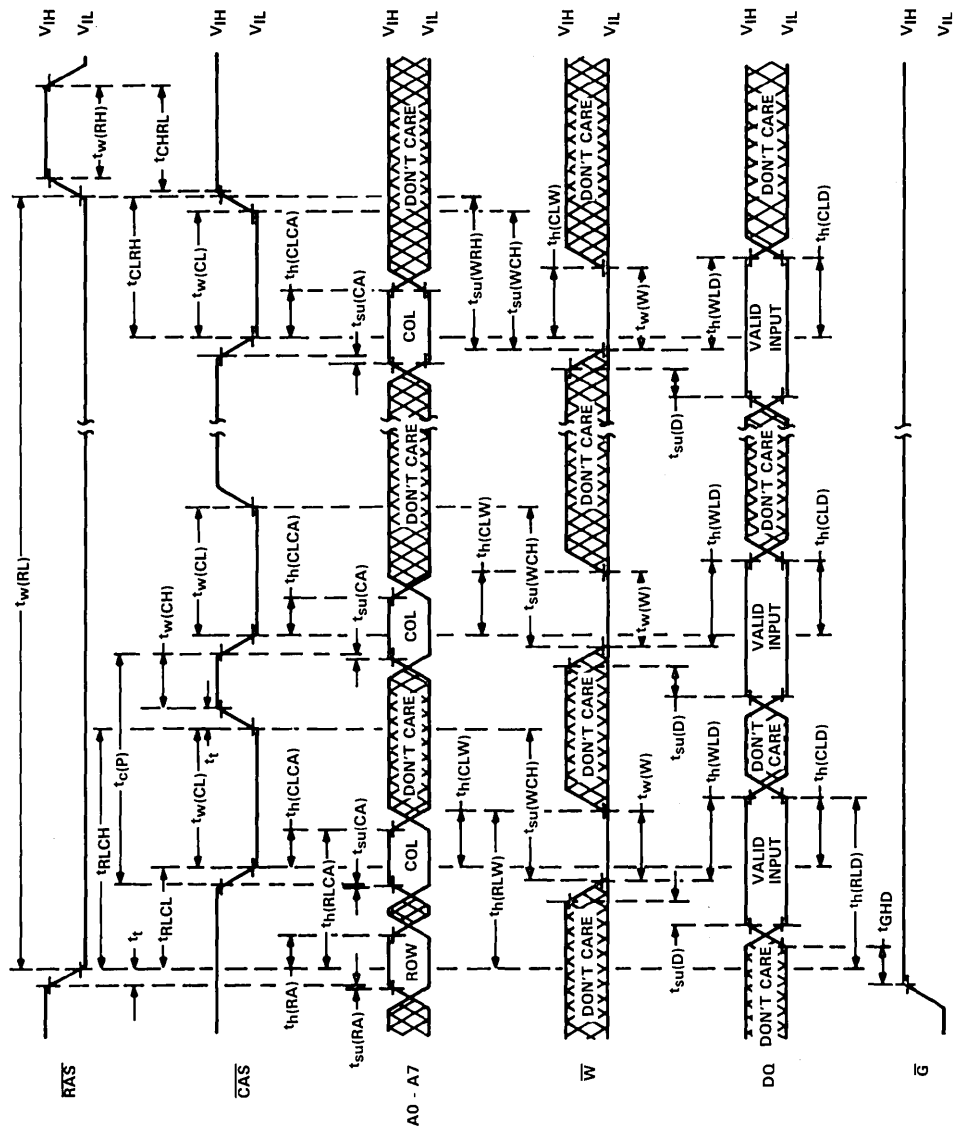
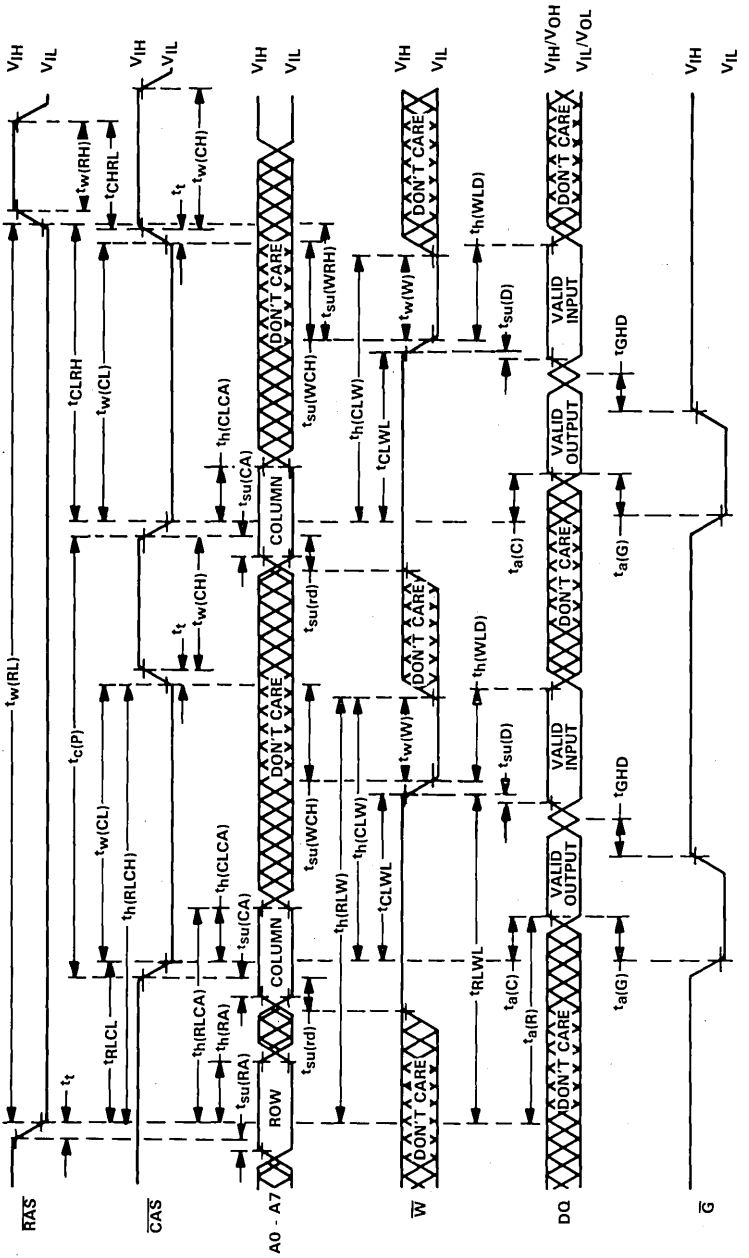
page-mode write cycle timing



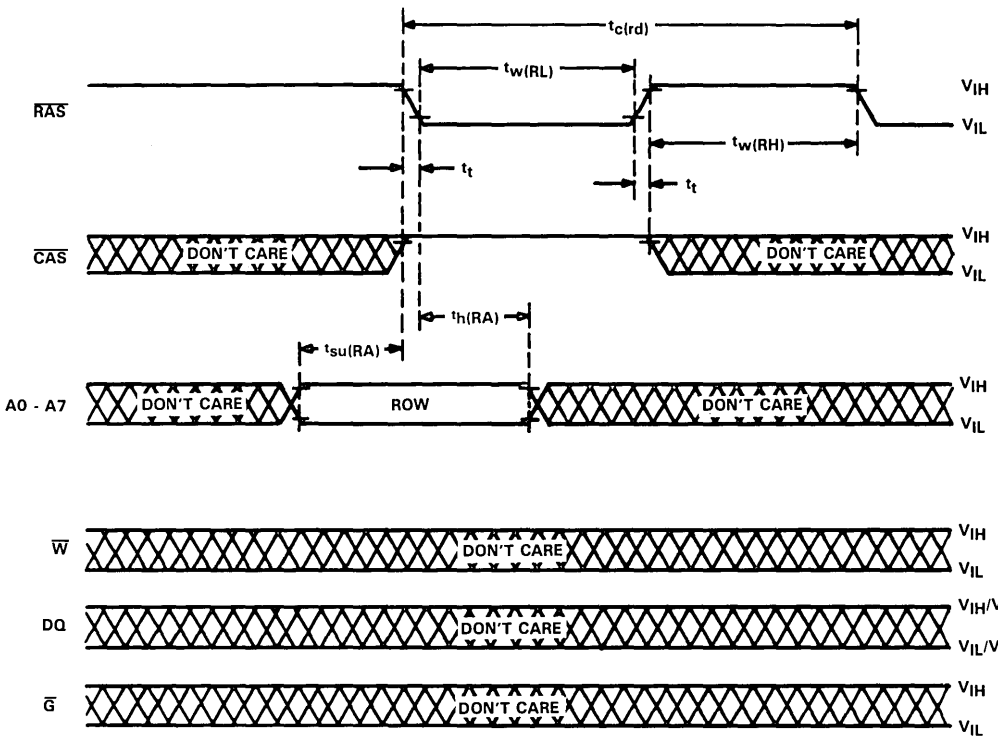
NOTE 7. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

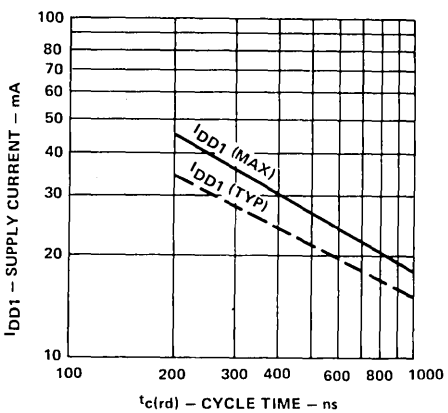
page-mode read-modify-write timing

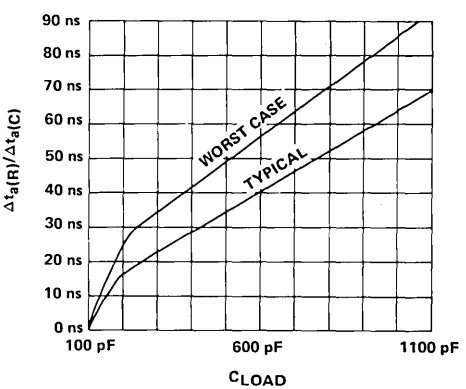


NOTE 8. A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as read and write timing specifications are not violated.

$\overline{RAS}$-only refresh timing







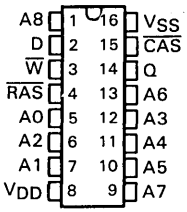
NOVEMBER 1985 – REVISED MARCH 1988

- 262,144 × 1 Organization
- Single 5-V Supply
- JEDEC Standardized Pinout
- Upward Pin Compatible with SMJ4164 (64K Dynamic RAM)
- Performance Ranges:

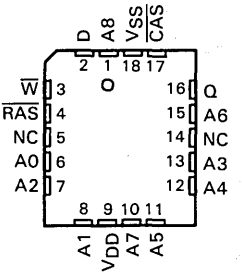
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
SMJ4256-12	120 ns	65 ns	230 ns
SMJ4256-15	150 ns	80 ns	260 ns
SMJ4256-20	200 ns	100 ns	330 ns

- Long Refresh Period . . . 4 ms (Max)
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- On-Chip Substrate Bias Generator
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with "Early Write" Feature
- Power Dissipation as Low As
  - Operating . . . 300 mW (Typ)
  - Standby . . . 12.5 mW (Typ)
- MIL-STD-883C Class B High-Reliability Processing
- $\overline{RAS}$-Only Refresh Mode
- Hidden Refresh Mode
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Mode
- Full Military DRAM Temperature Range Operation . . . −55°C to 110°C

JD PACKAGE
(TOP VIEW)



FV PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connect
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

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description

The SMJ4256 is a high-speed, 262,144-bit dynamic random-access memory, organized as 262,144 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level ploysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The SMJ4256 features maximum $\overline{RAS}$ access times of 120 ns, 150 ns, or 200 ns. Typical power dissipation is as low as 300 mW operating and 12.5 mW standby.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 125 mA typical, and a −0.5-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All address and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ4256 is offered in 16-pin 300-mil ceramic side-braze dual-in-line and 18-pad ceramic chip carrier packages. It is guaranteed for operation from −55°C to 110°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

The $\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}) and holding it low after $\overline{RAS}$ falls (see parameter t_{RLCHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

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hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a "$\overline{RAS}$-only" refresh cycle. The external address is also ignored during the hidden refresh cycles.

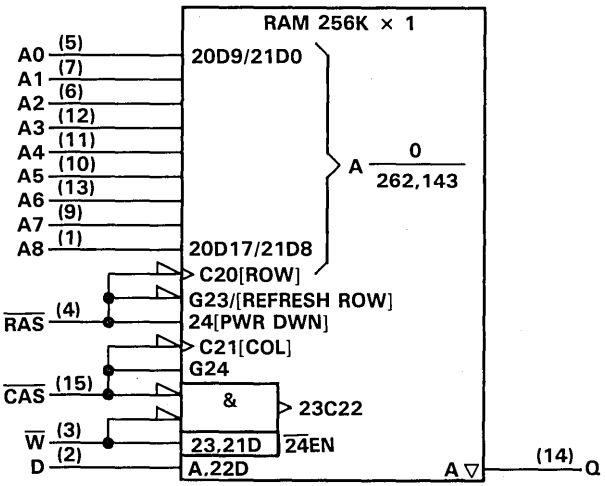
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe sequential row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by $t_{w(RL)}$, the maximum $\overline{RAS}$ low pulse duration.

power-up

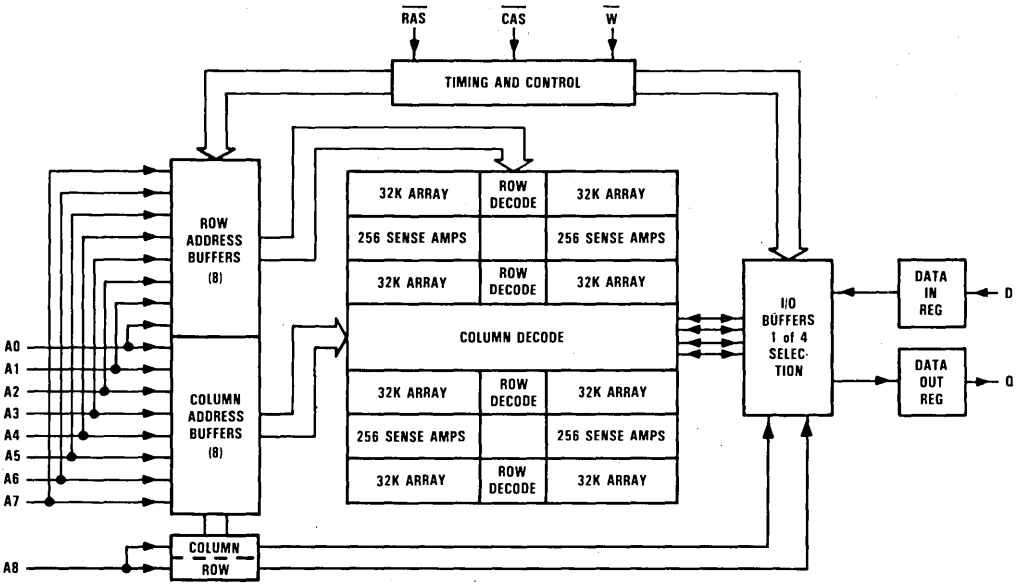
To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JD package.

functional block diagram



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absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage range for any pin, including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Minimum operating free-air temperature . . . . . −55°C
Operating case temperature . . . . . 110°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		5	V
V_{IL}	Low-level input voltage (see Note 2)	−0.5		0.8	V
T_A	Operating free-air temperature	−55			°C
T_C	Operating case temperature			110	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4256-12			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5 V, V_{DD} = 5.25 V, Output open			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5.25 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, Output open		60	80	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		2.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, Output open		45	63	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		35	50	mA

PARAMETER		TEST CONDITIONS	SMJ4256-15			SMJ4256-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5 V, V_{DD} = 5.25 V, Output open			±10			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5.25 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, Output open		60	75		45	60	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		2.5	5		2.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, Output open		45	60		35	45	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		35	50		25	45	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating temparature range, f = 1 MHz

PARAMETER		TYP†	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	pF
$C_{i(D)}$	Input capacitance, data input	4	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	4	pF
$C_{i(W)}$	Input capacitance, write enable input	4	pF
C_o	Output capacitance	5	pF

†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS‡	ALT. SYMBOL	SMJ4256-12		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 80 pF, I_{OH} = 5 mA, I_{OL} = 4.2 mA	t_{CAC}		65	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{RAC}		120	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{OFF}	0	30	ns

PARAMETER		TEST CONDITIONS‡	ALT. SYMBOL	SMJ4256-15		SMJ4256-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{CAC}		80		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 80, pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{RAC}		150		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{OFF}	0	30	0	35	ns

‡Figure 1 shows the load circuit; C_L values shown are typical for test system used.

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timing requirements over recommended supply voltage range and operating temperature range

		ALT. SYMBOL	SMJ4256-12 MIN	SMJ4256-12 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	125		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	172		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	277		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	65	10,000	ns
$t_{w(RH)P}$	Pulse duration, $\overline{RAS}$ high (page mode)	t_{RP}	115		ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (non-page mode)	t_{RPN}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	3		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	5		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	75		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	40		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	40		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	40		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		ns

Continued next page.

NOTES: 3. Timing measurements are referenced to V_{IL} max and V_{IH} min.

4. System transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating temperature range (continued)

		ALT. SYMBOL	SMJ4256-12		UNIT
			MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	5		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	65		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RCP}	25		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	67		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time	t_{RCD}	25	55	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	122		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

Continued next page.

NOTE 3: Timing requirements are referenced to V_{IL} max and V_{IH} min.

¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

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timing requirements over recommended supply voltage range and operating temperature range (continued)

		ALT. SYMBOL	SMJ4256-15		SMJ4256-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	145		190		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	205		250		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	315		390		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	30		40		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	80	10,000	100	10,000	ns
$t_{w(RH)P}$	Pulse duration, $\overline{RAS}$ high (page mode)	t_{RP}	120		120		ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (non-page mode)	t_{RPN}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	3		3		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	5		5		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		65		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		65		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	30		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		145		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	50		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	50		55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns

Continued next page.

NOTES: 3. Timing measurements are referenced to V_{IL} max and V_{IH} min.

4. System transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating temperature range (concluded)

		ALT. SYMBOL	SMJ4256-15		SMJ4256-20		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	5		5		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	80		100		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RCP}	25		25		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		40		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		35		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	85		90		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	70	35	100	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	155		190		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

PARAMETER MEASUREMENT INFORMATION

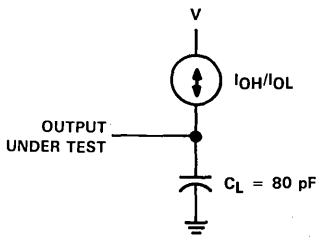

FIGURE 1. EQUIVALENT LOAD CIRCUIT

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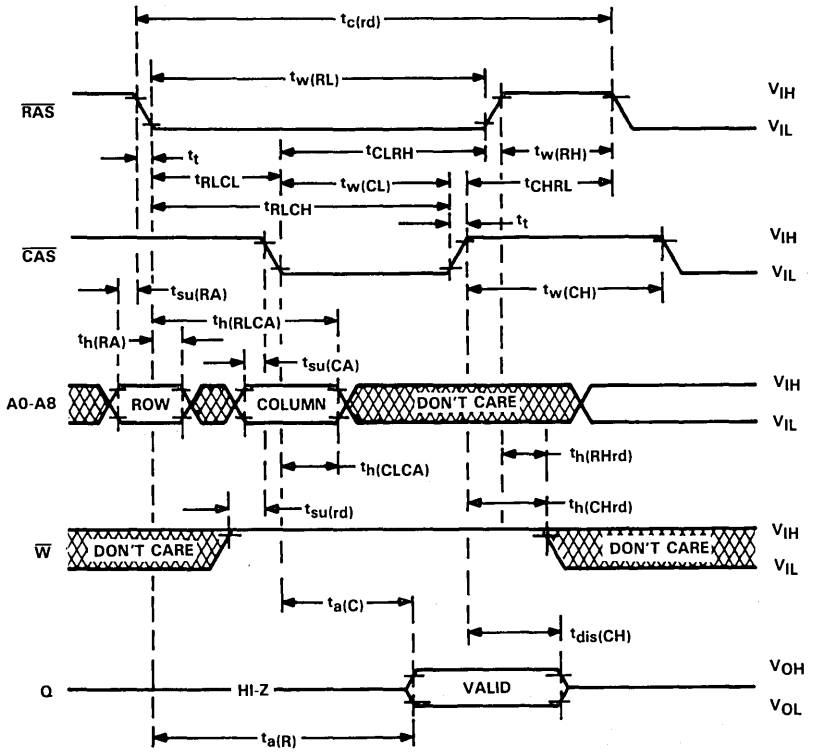
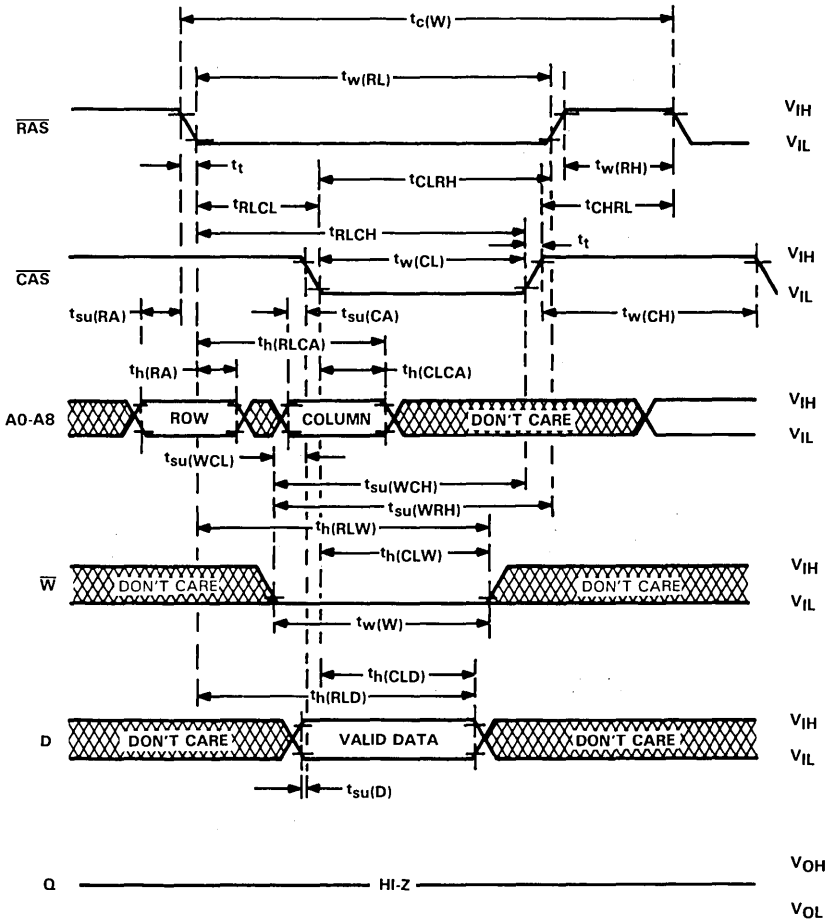
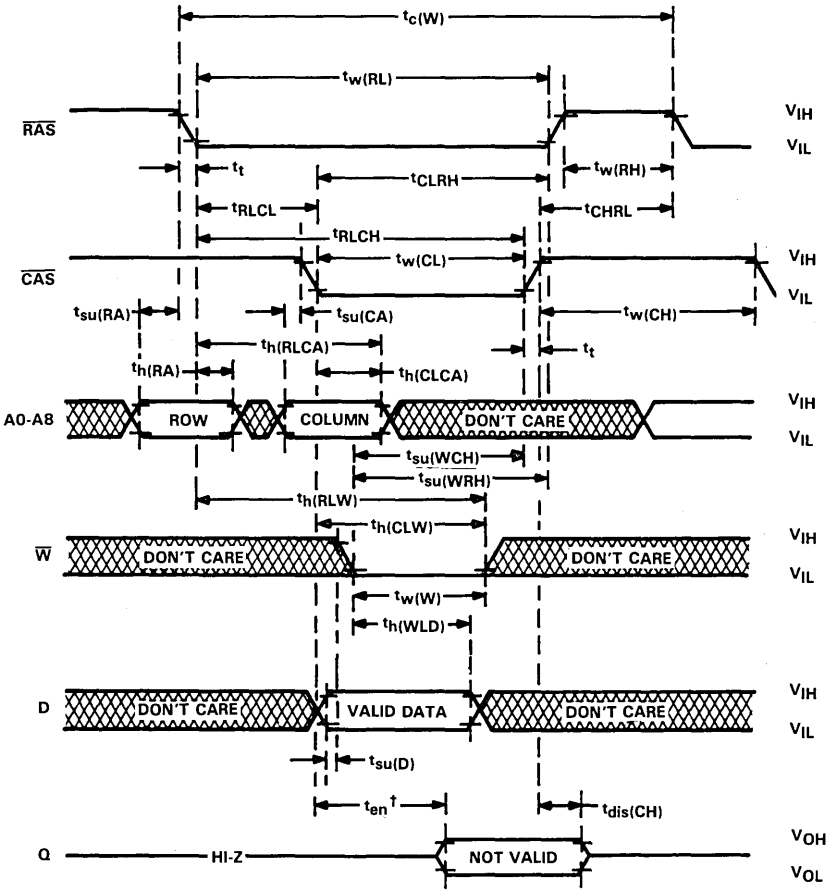
read cycle timing



early write cycle timing

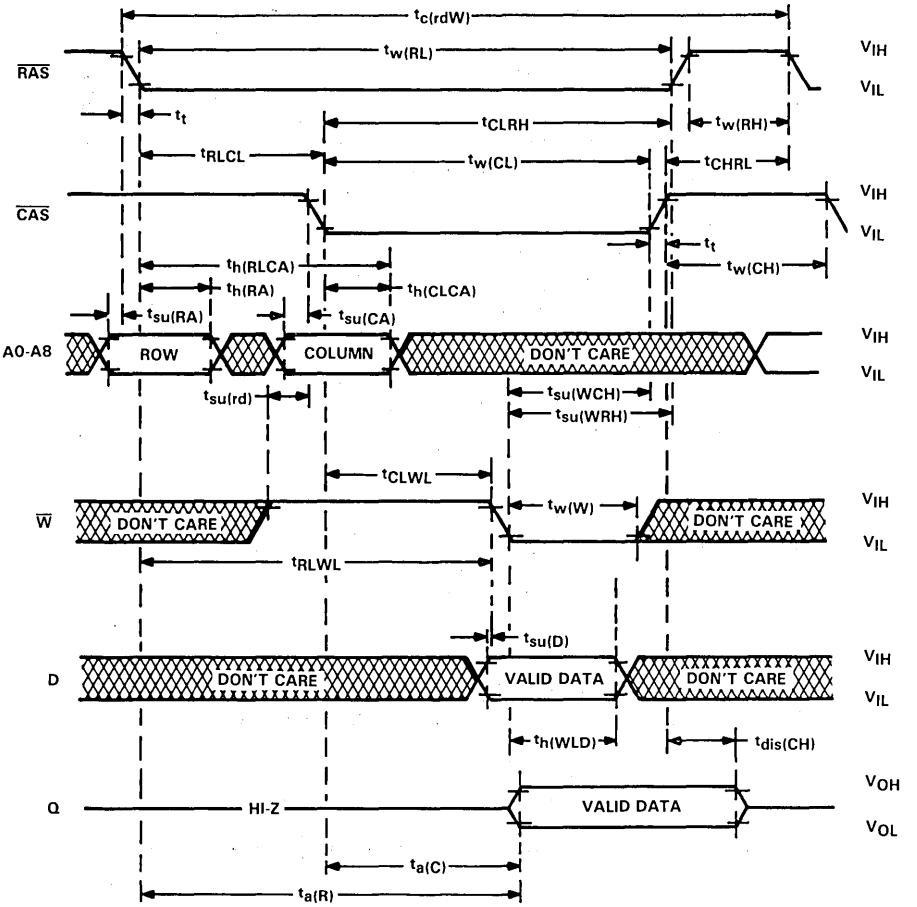


write cycle timing



†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle, but the active levels at the output are invalid.

read-write/read-modify-write cycle timing



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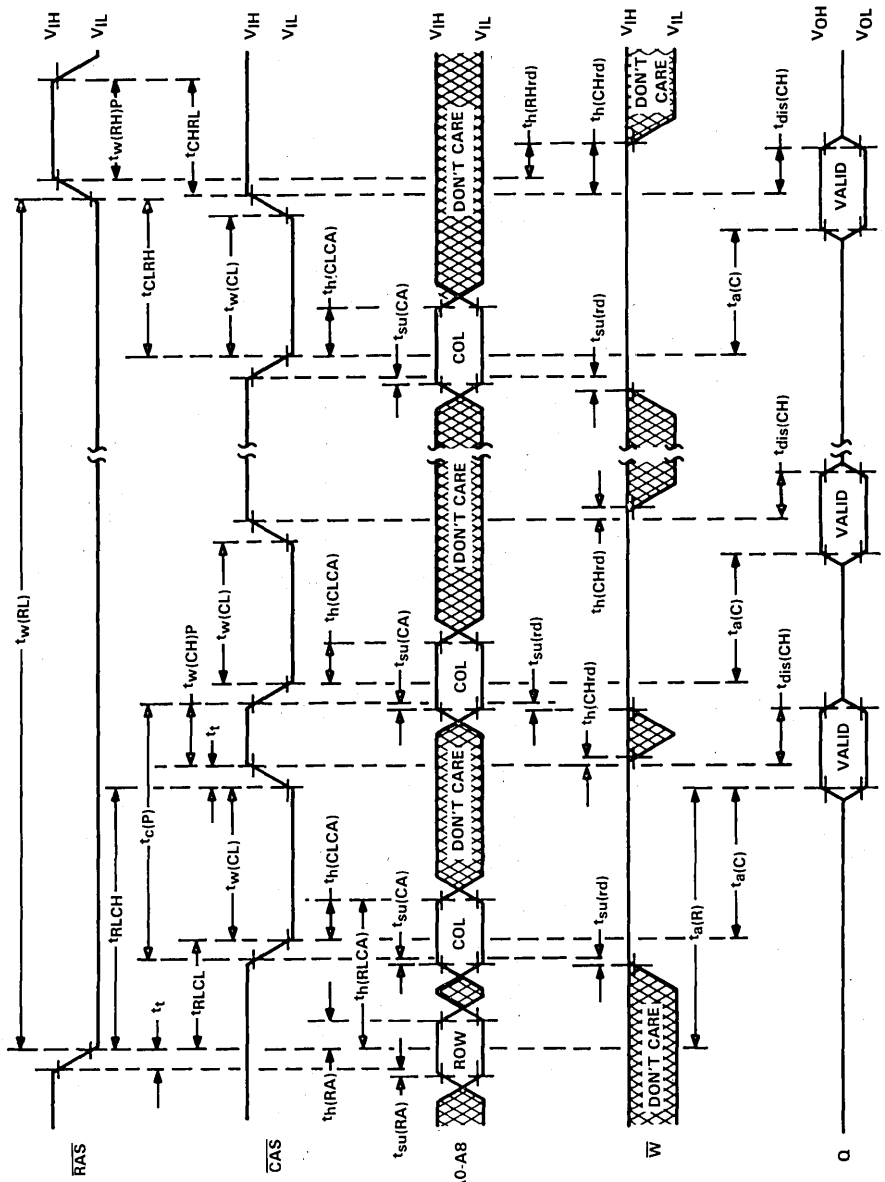
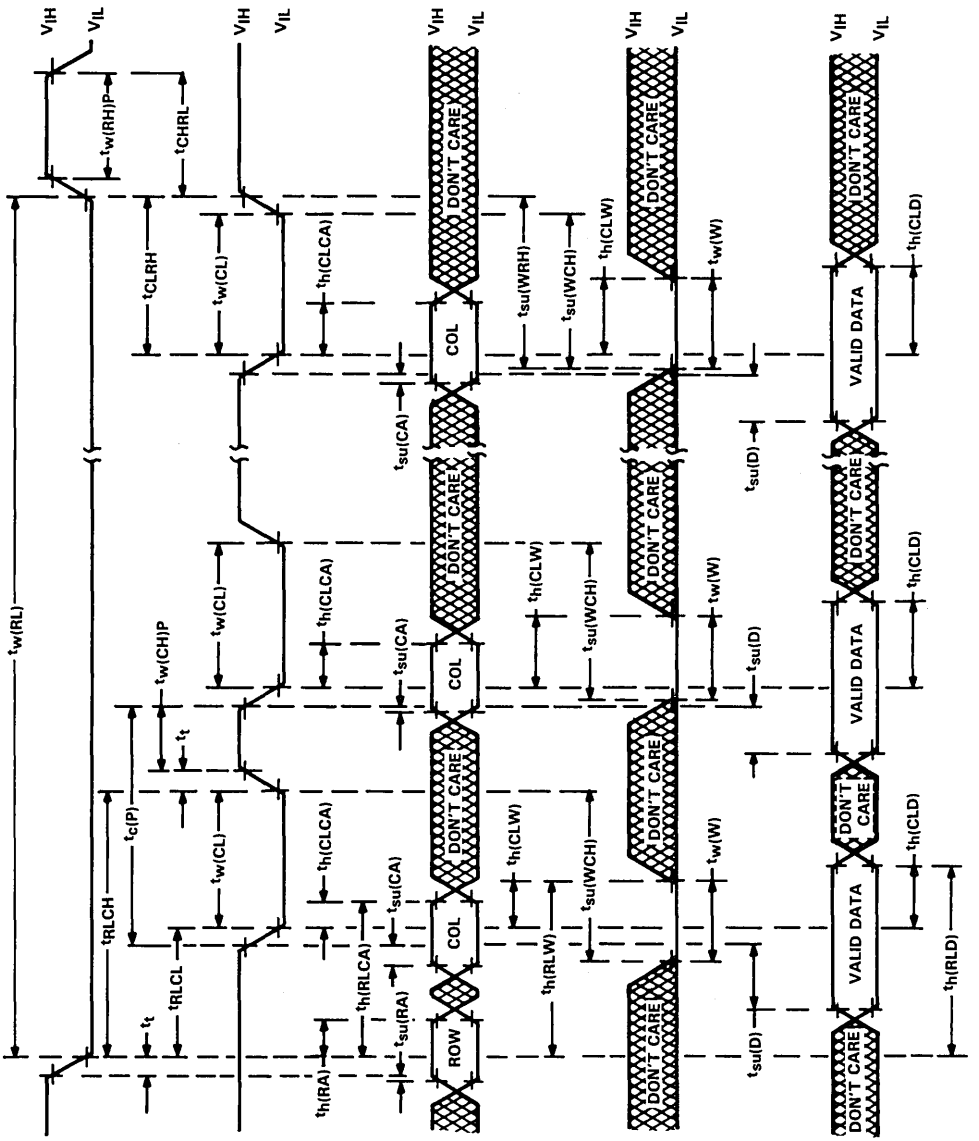
page-mode read cycle timing



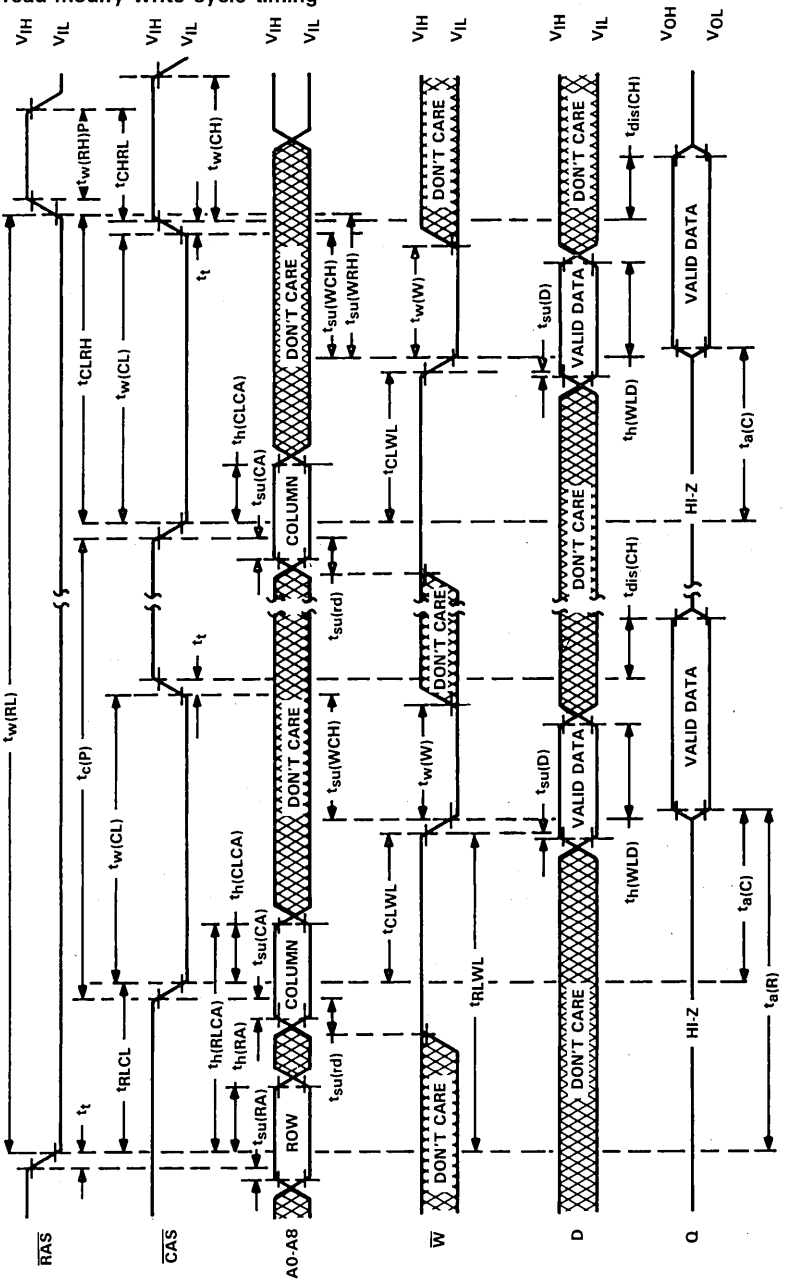
NOTE 5: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



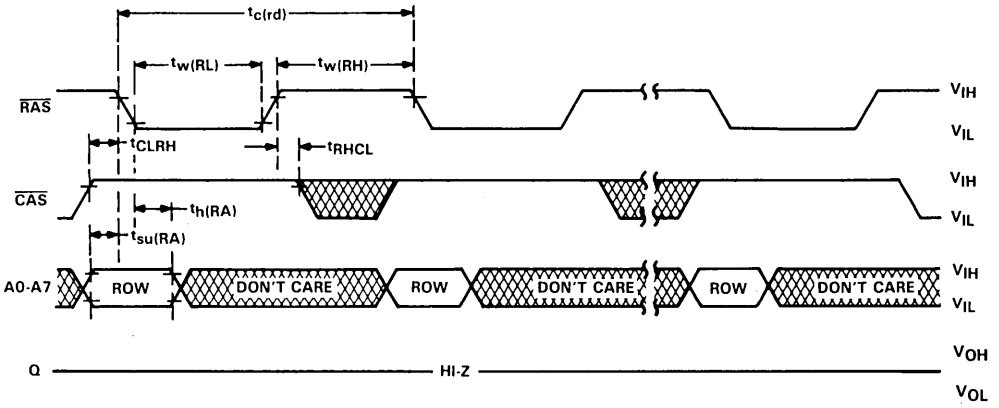
NOTE 6: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

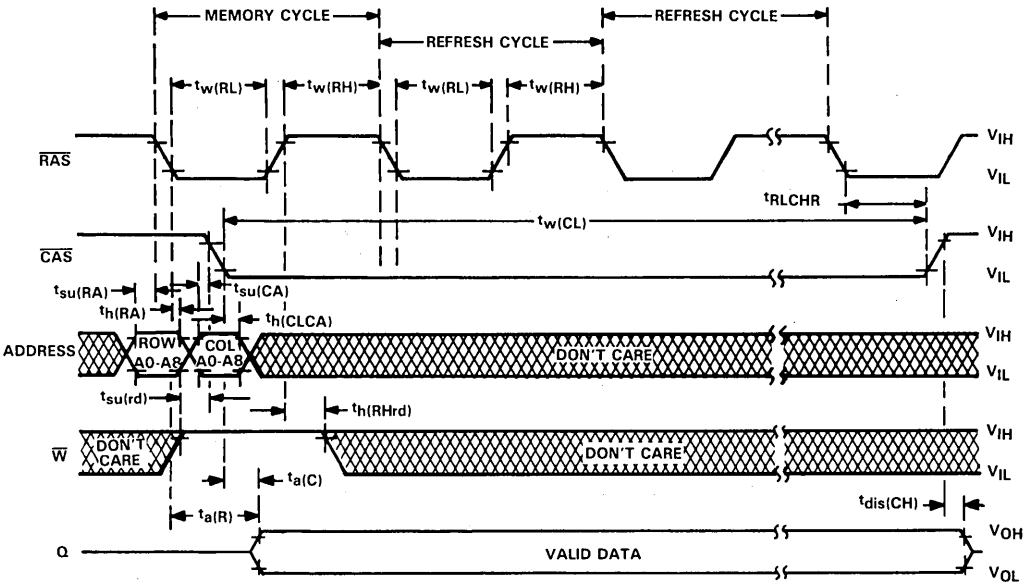


NOTE 7: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh cycle timing



hidden refresh cycle timing†



†This timing is guaranteed but not tested.

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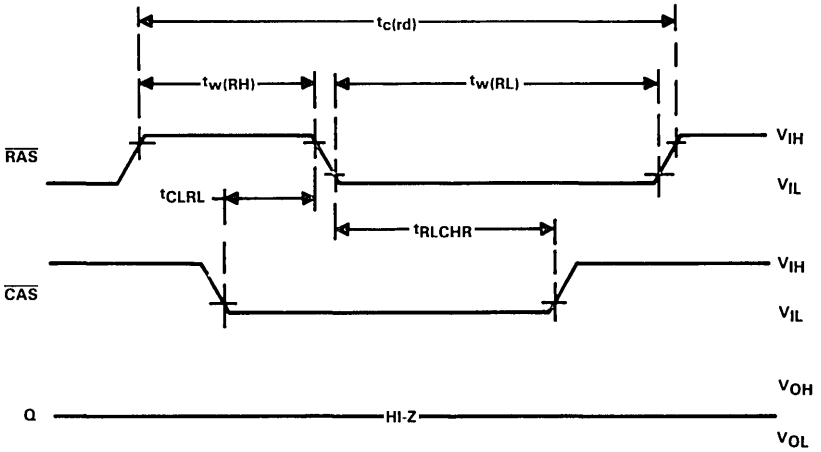
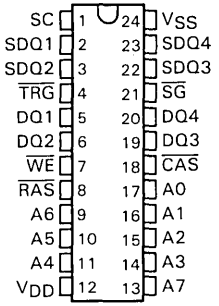
automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



MAY 1988

- 65,536 × 4 Organization
- Dual-Port Accessibility — Four I/Os for Sequential Access, Four I/Os for Random Access
- One Serial Data Register Built into Each Serial I/O for Sequential-Access Applications
- Designed for Video and Non-Video Applications
- Fast Serial Ports . . . 20-MHz Shift Rate
- Mid-Scan Load — Serial Data Streams Uninterrupted by Register Reload
- $\overline{TRG}$ as Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Random-Access Port is Compatible with the SMJ4464, 64K × 4 DRAM
- Supported by TI's SMJ34061 Video System Controller and SMJ34010 Graphics System Processor (GSP)
- 3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams
- Maximum Access Time from $\overline{RAS}$ . . . 150 ns
- Minimum Cycle Time (Read or Write) . . . 260 ns
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Random-Access Outputs
- Common Random-Access I/O Capability with "Early Write" Feature
- Available Temperature Ranges with MIL-STD-883-C Class B High-Reliability Processing:
  —S . . . −55°C to 110°C
  —L . . . 0°C to 70°C

JD PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Random-Access Data In/ Data Out/Write-Mask Bit
$\overline{RAS}$	Row-Address Strobe
SC	Serial Data Clock
SDQ1-SDQ4	Serial Data In/Data Out
$\overline{SG}$	Serial Enable
$\overline{TRG}$	Transfer Register/ Q Output Enable
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{WE}$	Write-Mask Select/ Write Enable

- JEDEC Standardized Pinout
- High-Speed Page-Mode Operation for Faster Access
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh and Hidden Refresh Modes
- Low Power Dissipation
- 24-Pin, 400-Mil Dual-In-line Package

description

The SMJ4461 is a high-speed dual-ported 65,536 × 4 bit dynamic random-access memory with on-chip data registers. The two ports are the random-access port and the sequential-access port. The random-access port makes the memory appear to be organized as 65,536 words of four bits each, similar to the

SMJ4464. The sequential-access port is interfaced to four internal 256-bit dynamic data registers which make the memory appear to be organized as 256 four-bit words of up to 256 bits each which are accessed serially.

The 256K Multiport Video RAM employs state-of-the-art scaled NMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

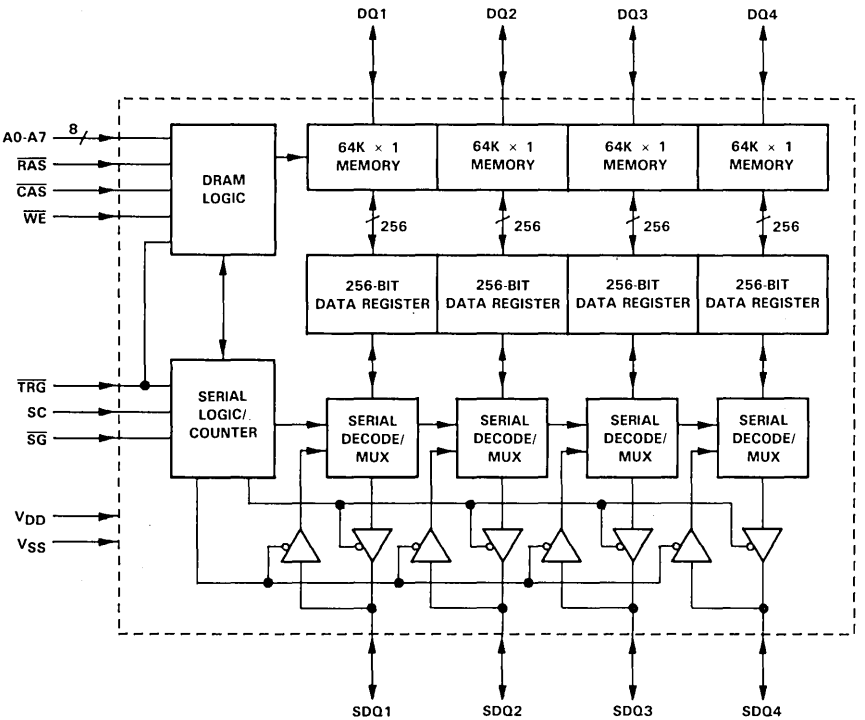
The SMJ4461 features full asynchronous dual-port accessibility except when transferring data between the data register and the random-access memory.

The refresh period is four milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. Note that the transfer of a row of data from the memory array to the data register also refreshes that particular row. $\overline{CAS}$-before-$\overline{RAS}$ and hidden refresh modes are also available.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on-chip to simplify system design. All data outs are unlatched to allow greater system flexibility.

The 256K Multiport Video RAM is offered in a 24-pin dual-in-line ceramic package and is guaranteed for operation from −55°C to 110°C. Packages are designed for insertion in mounting-hole rows on 10,16-mm (400-mil) centers.

functional block diagram



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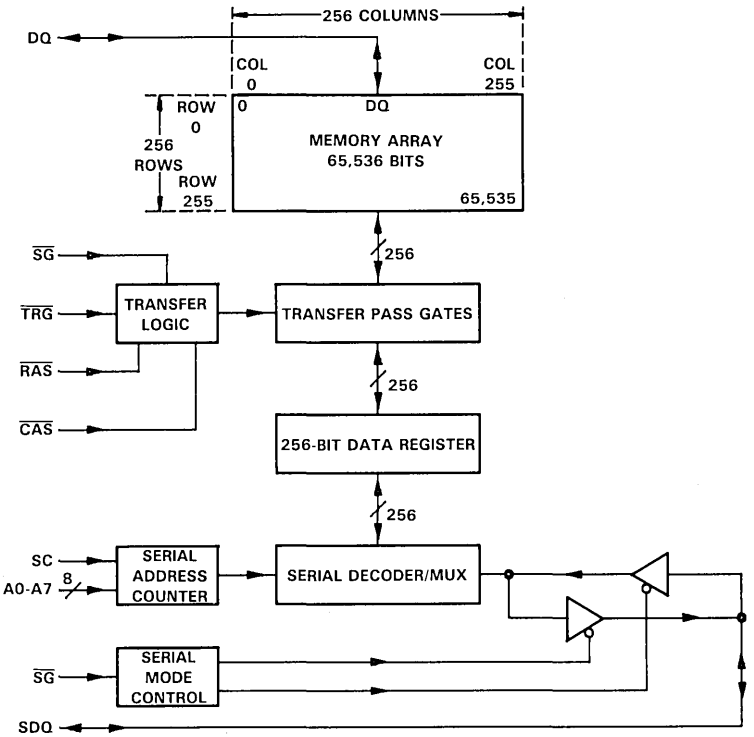
random port to serial port interface

The 256K Multiport Video RAM consists of a 64K × 4 DRAM port and a 256 × 4 serial port. Each of the four random (DRAM) I/Os is interfaced to a 256-bit data register, which can be loaded with 256 bits in parallel from any row in that I/O channel's memory and then read out sequentially, starting from one of 256 selectable locations along the data register. Conversely, each of the four data registers can be loaded serially with data from the serial input (SD) and subsequently transferred, 256 bits in parallel, into any row of memory for each respective DRAM I/O channel.

block diagram showing one random and serial interface



random-access address space to sequential-address space mapping

The 256 bits in each of the four data registers correspond to the 256 column locations of each of the four random I/Os. Data can be read out of the registers starting at any of the 256 data register bit locations.

This tap location is selected by addresses A7 through A0 on the falling edge of $\overline{CAS}$ during a transfer cycle between the memory array and the data registers. All registers are read out starting from the selected tap point proceeding from the least-significant bits to the most-significant bits. The four data registers are configured as circular data registers when reading their contents to the serial outputs. After the most-significant bit (bit 255) is read out of each register, the next bit read will be bit 00 (see explanation under section entitled "serial data input/output").

Note that if column address bits A7 through A0 equal 00 during the last memory-to-register transfer cycle, a total of 256 bits can be sequentially read out of each of the four data registers starting from bit position 00.

operation

random-access operation

transfer register select ($\overline{TRG}$)

The $\overline{TRG}$ selects either register transfer or random-access operation as $\overline{RAS}$ falls. To use the SMJ4461 in random-access mode, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. This causes the 256 storage elements of each data register to remain disconnected from the corresponding 256 bit lines of the memory array. If serial data is to be written in or read out of the data registers, the data registers must be disconnected from the bit lines. Holding TRG low as RAS falls enables the 256 switches that connect the data registers to the bit lines and indicates that a transfer will occur between the data registers and the selected memory row.

random output enable ($\overline{TRG}$)

During random-access operations, $\overline{TRG}$ functions as an output enable for the random outputs after the read access times have been satisfied (if this is a read cycle). Whenever $\overline{TRG}$ is held high, the Q outputs will be in the high-impedance state. This feature removes the possibility of an overlap between data on the address lines and data appearing on the Q outputs, making it possible to connect the address lines to the data I/O lines — although use of this organization prohibits the use of the early write cycle. It also allows read-modify-write cycles to be performed by providing a three-state condition to the common I/O pins to allow write data to be driven onto the pins after output read data has been externally latched.

address (A0 through A7)

Sixteen address bits are required to decode one of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip on the falling edge of $\overline{RAS}$. Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip on the falling edge of $\overline{CAS}$. All row and column addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$ respectively. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the device input and output buffers. $\overline{CAS}$ is also used to strobe the column address into the memory.

write-mask enable ($\overline{WE}$)

The $\overline{WE}$ pin selects the random-mode write-mask option. The SMJ4461 random port is equipped with two modes of write operations. If $\overline{WE}$ is held low on the falling edge of $\overline{RAS}$ (during a random access operation), the write mask is enabled. Accordingly, a 4-bit binary code (the mask) is input to the device via the random D/Q pins and is also latched on the falling edge of $\overline{RAS}$. This binary pattern determines which of the four DRAM I/Os will will be written into on that access and which DRAM I/Os will not. Thus,

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after $\overline{RAS}$ has latched the write mask on chip, input data is driven onto the DQ pins and is latched on the falling edge of the latter of $\overline{CAS}$ or $\overline{WE}$ (for early write operation, $\overline{WE}$ can remain low for the entire $\overline{RAS}$ low period). If a 0 was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, then the write circuits for that particular I/O will be defeated and data will not be written to that I/O. If a 1 was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, then the write circuits for that particular I/O will not be defeated and data will be written to that I/O. See the corresponding timing diagrams for details.

Important: The mask operation is selected only if $\overline{WE}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{WE}$ is held high on the falling edge of $\overline{RAS}$, the mask is not enabled and the write operation is identical to standard × 4 DRAMs, with all four I/Os being written by the data appearing on the DQ pins when the latter of $\overline{WE}$ or $\overline{CAS}$ is brought low. Thus, if it is not desired to use the mask function, then a standard DRAM timing interface can be used.

WRITE MASK FUNCTION TABLE

$\overline{TRG}$	$\overline{WE}$	DQ1-DQ4	MODE
1	1	X	Write enabled at DQ1-DQ4
1	0	1	Write to DQ enabled
1	0	0	Write to DQ disabled

NOTE 1: The logic states in the table above are assumed valid on the falling edge of $\overline{RAS}$.

write enable ($\overline{WE}$)

The read or write mode is selected through the write-enable ($\overline{WE}$) input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle.

data I/O (DQ1-DQ4)

Memory data is written during a write or read-modify-write cycle. The falling edge of $\overline{WE}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low. Thus, the data will be strobed in by $\overline{WE}$ with data setup and hold times referenced to this signal. The three-state output buffers provide direct TTL compatibility (no pull-up resistors required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state as long as $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low.

Once the outputs are valid, they will remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ or $\overline{TRG}$ going high will return the outputs to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle. In a register-transfer operation (memory-to-register or register-to-memory), the outputs remain in the high-impedance state for the entire cycle, regardless of transitions on $\overline{CAS}$ or $\overline{TRG}$.

write mask bits (DQ1-DQ4)

When the write mask is enabled ($\overline{WE}$ low on the falling edge of $\overline{RAS}$), the write mask bits determine which DRAM I/Os are to be written and which of the DRAM I/Os will have their write operations internally defeated. The states of the write mask bits are latched on-chip on the falling edge of $\overline{RAS}$ and selectively control the internal write enable circuits of each corresponding DRAM I/O. If the write mask is not enabled ($\overline{WE}$ high on the falling edge of $\overline{RAS}$), then no write enable circuits will be defeated and data appearing at the DQ1-DQ4 pins on the falling edge of $\overline{RAS}$ will be ignored. See timing diagrams and the table under "write mask enable ($\overline{WE}$)" for details.

refresh

A refresh operation must be performed to each row at least once every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power. Note that the data registers are dynamic storage elements and that the data held in the registers will be lost unless SC is clocked two times or else the data is reloaded from the memory array. See specifications for maximum register retention times.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}). The external row address is ignored and the refresh address is generated internally.

column-address strobe ($\overline{CAS}$)

The $\overline{CAS}$ input latches the column addresses on-chip and also functions as an output enable for DQ1-DQ4.

power up

After power up, the power supply must remain at its steady-state value for one millisecond. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles and one memory-to-register transfer cycle with an SC cycle following the rising edge of $\overline{TRG}$ before proper device operation is achieved.

sequential-access operation

transfer register select ($\overline{TRG}$)

Memory operations involving parallel use (i.e., transfer from memory to data register or data register to memory) of the data register are invoked by bringing $\overline{TRG}$ low with the address lines A0-A7 before $\overline{RAS}$ falls. This enables the switches connecting the 256 elements of each data register to the 256 bit lines of each DRAM I/O. The states of $\overline{WE}$ and $\overline{SG}$, which are also latched on the falling edge of $\overline{RAS}$, determine whether the 256-bit data transfer will be from the memory array to the data registers or from the data registers to memory array, as well as determining if the SDQs are in read or write mode (see "transfer operation logic table").

Note that the state of $\overline{TRG}$ is latched on the falling edge of $\overline{RAS}$ just like a row address to select the mode of operation. During read or read-modify-write cycles, $\overline{TRG}$ functions as output enable after $\overline{CAS}$ falls.

transfer write enable ($\overline{WE}$)

In register transfer mode, $\overline{WE}$ determines whether a transfer will occur from the data registers to the memory array, or from the memory array to the data registers. To transfer data from the data registers to the memory array, $\overline{WE}$ and $\overline{SG}$ are held low as $\overline{RAS}$ falls. If $\overline{SG}$ were to be high during this transition, then no transfer of data from the data register to the memory array would occur, but the SDQs would be put into the write mode. This would allow serial data to be written into the register. To transfer from the memory array to the data registers, $\overline{WE}$ is held high and $\overline{SG}$ is a don't care as $\overline{RAS}$ falls. This cycle puts the SDQs into the read mode, thus allowing serial data to be read out of the data register. Note that $\overline{WE}$ and $\overline{SG}$ setup and hold times are referenced to the falling edge of $\overline{RAS}$ for this mode of operation (see "transfer operation logic" table).

row address (A0 through A7)

Eight address bits are required to select one of the 256 possible rows involved in the transfer of data to or from the data registers. (The states of A0-A7, $\overline{WE}$, $\overline{TRG}$, and $\overline{SG}$ are latched on the falling edge of $\overline{RAS}$).

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register column address (A0 through A7)

To select one of the 256 positions along each of the four data registers from which the first serial data will be read out, or to which the first serial data will be written, the appropiate 8-bit column address (A0-A7) must be valid when $\overline{CAS}$ falls during the appropriate transfer cycle.

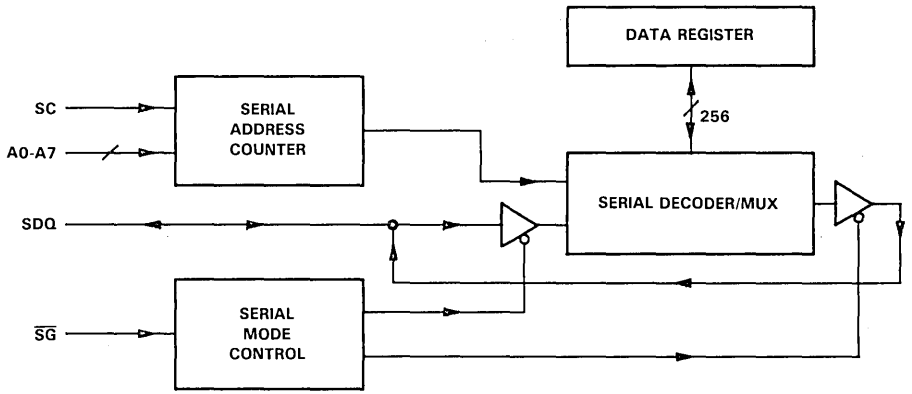
serial data clock (SC)

Data is written in or read out of the data registers on the rising edge of SC. This makes it possible to view the data registers as though they were made of 256 positive-edge-triggered D flip-flops connected D to Q (not to be confused with the DQ random I/O pins of the SMJ4461). The SMJ4461 is designed to work with a wide range duty cycle clock to simplify system design.

serial data input/output (SDQ1-SDQ4)

SD and SQ share a common I/O pin. Data is written in when $\overline{SG}$ is low during write mode and data is read out when $\overline{SG}$ is low during read mode (see "transfer operation logic table"). Note that when the serial address counter reaches its maximum value of 255, it is reset back to 00 with the next positive transition of SC. This allows data to be read out in a continuous loop.

block diagram of one serial I/O



serial enable ($\overline{SG}$)

The serial enable pin has two functions. First, it is used on the falling edge of $\overline{RAS}$, with both $\overline{TRG}$ and $\overline{WE}$ low. If $\overline{SG}$ is low during this transition, then a register-to-memory transfer will occur. On the other hand, if $\overline{SG}$ were to be high as $\overline{RAS}$ falls, then a write-mode control cycle will be performed. The function of this cycle is to switch the SDQs from the output mode to the input mode, thus allowing serial data to be written into the data register. Second, $\overline{SG}$ is used as a SDQ enable/disable. In the write mode, $\overline{SG}$ is used as an input enable. $\overline{SG}$ high disables the input, and $\overline{SG}$ low enables the input. To take the device out of the write mode and into the read mode, a memory-to-register transfer cycle must be performed. The read mode allows data to be read out of the data register. $\overline{SG}$ high disables the output and $\overline{SG}$ low enables the output. Note that the serial address counter will be incremented on each SC cycle regardless of the state of $\overline{SG}$.

TRANSFER OPERATION LOGIC TABLE

$\overline{TRG}$	$\overline{WE}$	$\overline{SG}$	MODE
0	0	0	Register-to-memory transfer
0	0	1	Write-mode enable
0	1	X	Memory-to-register transfer

NOTE 2: The logic states in the table above are assumed valid on the falling edge of $\overline{RAS}$.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V_{DD} and data out (see Note 3) . . . . . −1.0 V to 7 V
Voltage range for V_{DD} supply with respect to V_{SS} . . . . . −1 V to 7 V
Voltage range for data out with respect to V_{SS} . . . . . −1 V to V_{DD} + 0.3 V
Short circuit output current per output . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating temperature range . . . . . −55°C to 110°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 3: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	All inputs except SC	2.4		5.5	V
		SC	2.6		5.5	
V_{IL}	Low-level input voltage (see Note 4)		−1		0.8	V
T_A	Operating free-air temperature		−55			°C
T_C	Operating case temperature				110	°C

NOTE 4: The algebraic convention where the more negative (less positive) limit is designated as minimum is used in this data sheet for logic voltage levels only.

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electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4461-15			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All outputs open			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V			±10	μA
I_{DD1}	Average operating current during read, write or transfer cycle (serial port in standby)	Mininum cycle time, No load on DQ and SDQ pins		50	80	mA
I_{DD2}	Standby current (total, both ports)	After 1 memory cycle, $\overline{RAS}$, $\overline{CAS}$, SC, and $\overline{SG}$ ≥ 2.4 V, No load on DQ and SDQ pins		15	20	mA
I_{DD3}	Average refresh current	Minimum cycle time, $\overline{RAS}$ ≤ 0.8 V, $\overline{CAS}$ ≥ 2.4 V, No load on DQ and SDQ pins		45	75	mA
I_{DD4}	Average page-mode current (serial port in standby)	Minimum cycle time, $\overline{RAS}$ ≤ 0.8 V, $\overline{CAS}$ cycling, No load on DQ and SDQ		35	60	mA
I_{DD5}	Average current with memory array in standby and register shifting	$t_{c(SC)}$ = MIN, $\overline{RAS}$ and $\overline{CAS}$ ≥ 2.4 V, No load on DQ and SDQ pins		70	80	mA
I_{DD6}	Worst case average current	Minimum cycle time on both ports, No load on DQ and SDQ pins		110	140	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance at 25°C with nominal supply voltage, f = 1 MHz

PARAMETER‡		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		4		pF
$C_{i(RC)}$	Input capacitance, strobe inputs		8		pF
$C_{i(WE)}$	Input capacitance, write enable input		8		pF
$C_{i(SC)}$	Input capacitance, serial clock		8		pF
$C_{i(SG)}$	Input capacitance, serial enable		4		pF
$C_{i(TRG)}$	Input capacitance, transfer register input		4		pF
C_o	Output capacitance		5		pF

‡Capacitance data collected for major design or process changes only.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (see Figure 1)

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4461-15		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 80 pF, t_{RLCL} ≥ MAX	t_{CAC}		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	C_L = 80 pF, t_{RLCL} ≤ MAX	t_{RAC}		150	ns
$t_{a(TRG)}$	Access time of DQ from $\overline{TRG}$ low	C_L = 80 pF			45	ns
$t_{a(SC)}$	Access time of SQ from SC high	C_L = 80 pF			50	ns
$t_{a(SG)}$	Access time of SQ from $\overline{SG}$ low	C_L = 80 pF			40	ns
$t_{dis(CH)}$	Random-output disable time from $\overline{CAS}$ high	C_L = 80 pF	t_{OFF}	0	30	ns
$t_{dis(TRG)}$	Random-output disable time from $\overline{TRG}$ high	C_L = 80 pF		0	30	ns
$t_{dis(SG)}$	Serial-output disable time from $\overline{SG}$ high	C_L = 80 pF			30	ns

timing requirements over recommended supply voltage and operating free-air temperature ranges

		ALT.	SMJ4461-15		UNIT
		SYMBOL	MIN	MAX	
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		ns
$t_{c(Trd)}$	Transfer read cycle time	t_{RC}	260		ns
$t_{c(TW)}$	Transfer write cycle time	t_{WC}	260		ns
$t_{c(P)}$	Page-mode read or write cycle time	t_{PC}	145		ns
$t_{c(rdWP)}$	Page-mode read-write/read-modify-write cycle time	t_{RWC}	230		ns
$t_{c(SC)}$	Serial clock cycle time	t_{SCC}	50	20,000	ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ duration (precharge time)	t_{CP}	60		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	75	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		ns
$t_{w(SCL)}$	Pulse duration, SC low		10		ns
$t_{w(SCH)}$	Pulse duration, SC high		10		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		45		ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(RW)}$	$\overline{WE}$ setup time before $\overline{RAS}$ low with $\overline{TRG}$ low (register transfer cycles)		0		ns
$t_{su(DQ)}$	DQ setup time before $\overline{RAS}$ low with $\overline{TRG}$ high (random access, write mask select)		8		ns
$t_{su(D)}$	Data setup time	t_{DS}	5		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		ns
$t_{su(SD)}$	Serial data setup time before SC high		5		ns
$t_{su(TRG)}$	$\overline{TRG}$ setup time before $\overline{RAS}$ low		0		ns
$t_{su(SG)}$	$\overline{SG}$ setup time before $\overline{RAS}$ low with $\overline{TRG}$ and $\overline{WE}$ low		0		ns
$t_{su(WM)}$	$\overline{WE}$ setup time before $\overline{RAS}$ low (write mask select)		0		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RW)}$	$\overline{WE}$ hold time after $\overline{RAS}$ low with $\overline{TRG}$ low (transfer cycles)		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		ns
$t_{h(WLD)}$	Data hold time after $\overline{WE}$ low	t_{DH}	45		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns

Continued next page.

NOTES: 5. Timing measurements referenced to V_{IL} max and V_{IH} min.
6. System transition times (rise and fall) are to be a minimum of 3 ns and a maximum of 50 ns.

† All cycle times assume t_t = 5 ns.

‡ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).

§ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage and operating free-air temperature ranges (continued)

			ALT.	SMJ4461-15		UNIT
			SYMBOL	MIN	MAX	
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low		t_{WCH}	45		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low		t_{WCR}	120		ns
$t_{h(WQE)}$	$\overline{TRG}$ hold time after $\overline{WE}$ low			40		ns
$t_{h(SD)}$	Serial data-in hold time after SC high			15		ns
$t_{h(SQ)}$	Serial data-out hold time after SC high□			6		ns
$t_{h(TRG)}$	$\overline{TRG}$ hold time after $\overline{RAS}$ low			15		ns
$t_{h(DQ)}$	DQ hold time after $\overline{RAS}$ low with $\overline{TRG}$ high and $\overline{WE}$ low			15		ns
$t_{h(SG)}$	$\overline{SG}$ hold time after $\overline{RAS}$ low with $\overline{TRG}$ and $\overline{WE}$ low			15		ns
$t_{h(WM)}$	$\overline{WE}$ hold time after $\overline{RAS}$ low (write mask select)			15		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		t_{CSH}	150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		t_{CRP}	5		ns
t_{CLGH}	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high			80		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		t_{RSH}	75		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{WE}$ low (read-modify-write cycle only)¶		t_{CWD}	110		ns
t_{RLTH}	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (memory-to-register transfer cycle)	Early load#		25		ns
		Mid-line real-time load		100		
t_{RLSH}	Delay time, $\overline{RAS}$ low to the first positive transition of SC after $\overline{TRG}$ high (register transfer cycle)			125		ns
t_{THRL}	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low after a transfer cycle			100		ns
t_{CLSH}	Delay time, $\overline{CAS}$ low to the first positive transition of SC after $\overline{TRG}$ high (register transfer cycle)			50		ns
t_{SHRL}	Delay time, SC high to $\overline{RAS}$ low with $\overline{TRG}$ and $\overline{WE}$ low (register-to-memory transfer cycle)‖			50		ns
t_{SHTH}	Delay time, SC high to $\overline{TRG}$ high (memory-to-register transfer cycle) ☆			15		ns

Continued next page.

NOTE 5: Timing measurements are referenced to V_{IL} max and V_{IH} min.

¶ $\overline{TRG}$ must disable the output buffers prior to applying data to the device.

$\overline{TRG}$ may be brought high early during a memory-to-register transfer cycle as long as the $th_{(TRG)}$, t_{SHTH}, and t_{RLSH} specifications are met.

‖ In a register-to-memory transfer cycle, the state of SC when $\overline{RAS}$ falls is a don't care condition. However, to guarantee proper sequencing of the internal clock circuitry there can be no positive transitions of SC for at least 40 ns prior to when $\overline{RAS}$ goes low. See the section entitled "sequential access operation" for a complete explanation of the transfer operation.

☆ In a memory-to-register transfer cycle, the state of SC when $\overline{TRG}$ rises is a don't care condition. However, to guarantee proper sequencing of the internal clock circuitry there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high. See the section entitled "sequential access operation" for a complete explanation of the transfer operation.

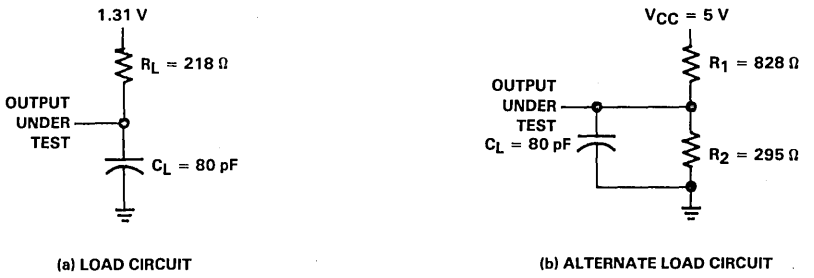
□ This parameter is guaranteed but not tested.

timing requirements over recommended supply voltage and operating free-air temperature ranges (concluded)

		ALT.	SMJ4461-15		UNIT
		SYMBOL	MIN	MAX	
t_{THSH}	Delay time, $\overline{TRG}$ high to SC high (memory-to-register transfer cycle)		20		ns
t_{THRH}	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (memory-to-register transfer cycle)		0		ns
t_{THCH}	Delay time, $\overline{TRG}$ high to $\overline{CAS}$ high (register transfer cycles)		0		ns
t_{CLTH}	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high (memory-to-register transfer cycle)		25		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee $\overline{RAS}$ access time)	t_{RCD}	25	75	ns
t_{CLGL}	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ low (maximum value specified to guarantee column access time)			30	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{WE}$ low (read-modify-write cycle only)	t_{RWD}	185		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	25		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	25		ns
t_{SGSC}	Delay time, $\overline{SG}$ low to SC high during serial data-in shift cycle		10		ns
t_{GHD}	Delay time, $\overline{TRG}$ high before data applied at DQ	t_{GDD}	30		ns
$t_{rf(MA)}$	Refresh time interval, memory array	t_{REF1}		4	ms
$t_{rf(SR)}$	Refresh time interval, shift register	t_{REF2}		20,000	ns

NOTE 5: Timing measurements are referenced to V_{IL} max and v_{IH} min.

PARAMETER MEASUREMENT INFORMATON



(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

FIGURE 1. LOAD CIRCUITS FOR TIMING PARAMETERS

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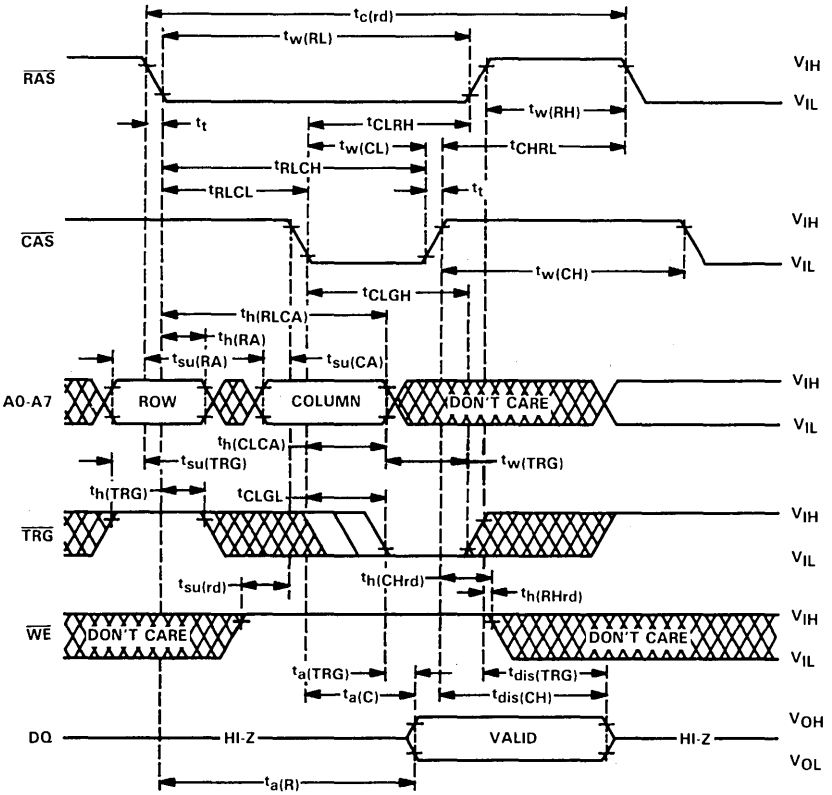
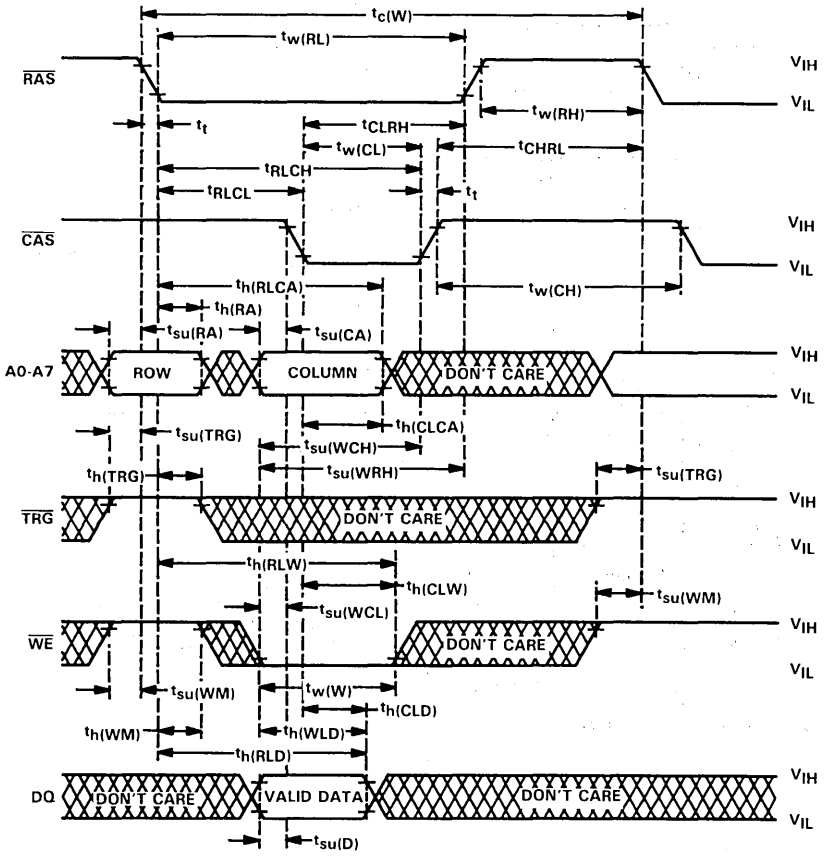
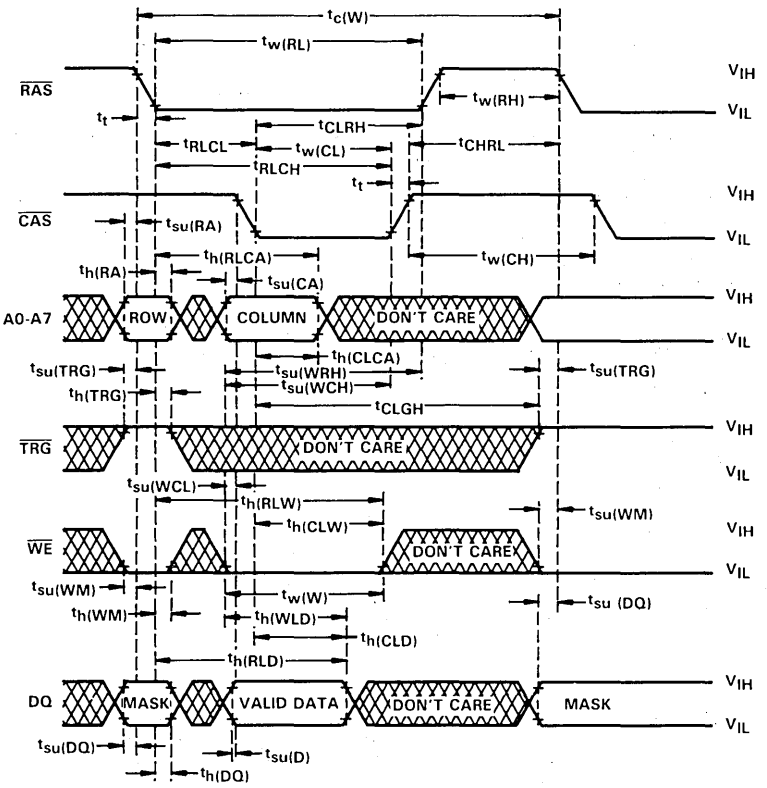
read cycle timing



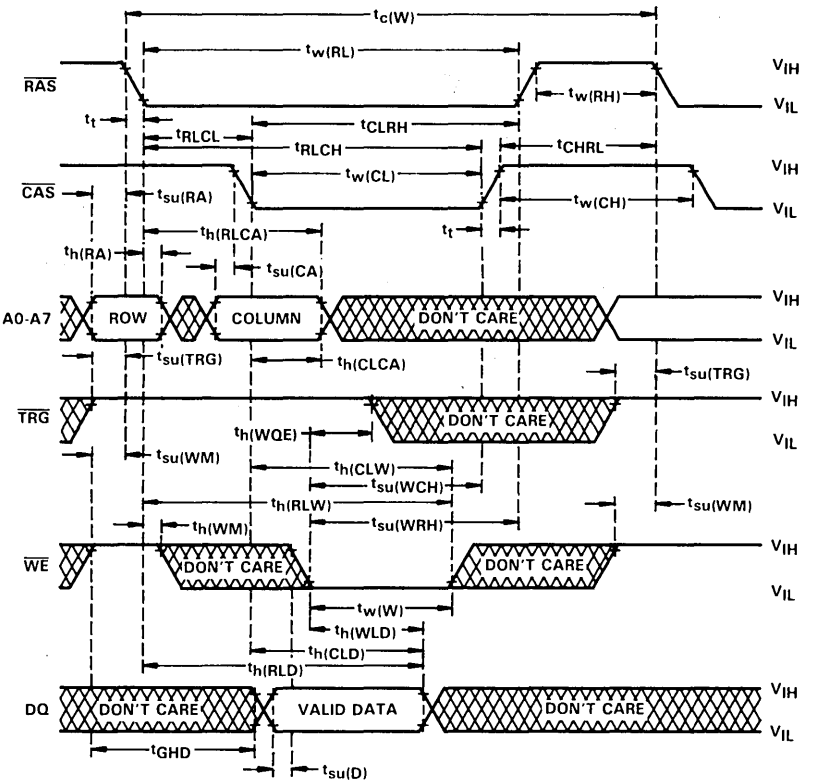
early write cycle timing, write mask unselected



early write cycle timing, write mask selected



delayed write cycle timing, mask unselected



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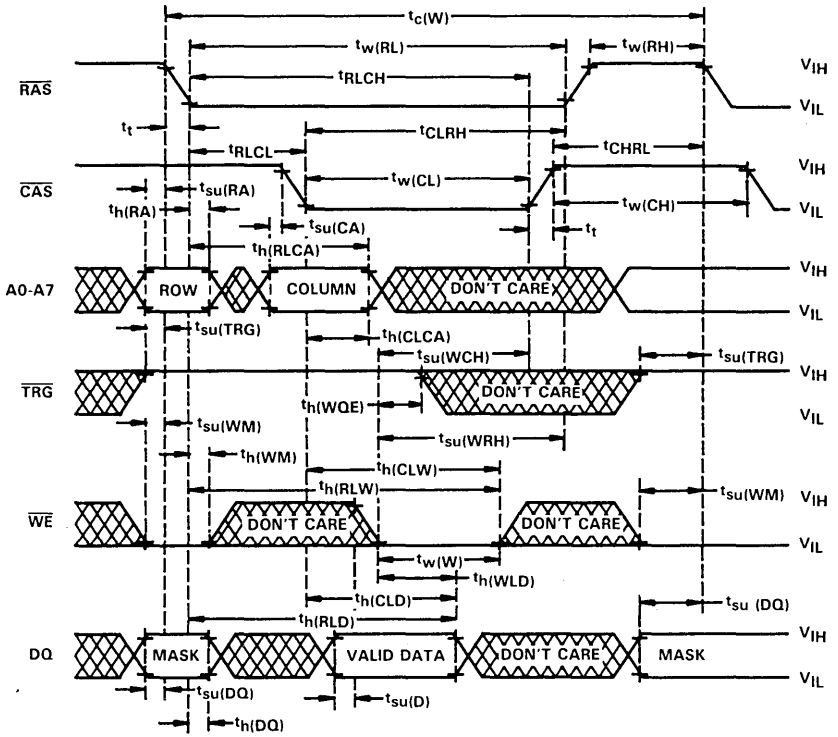
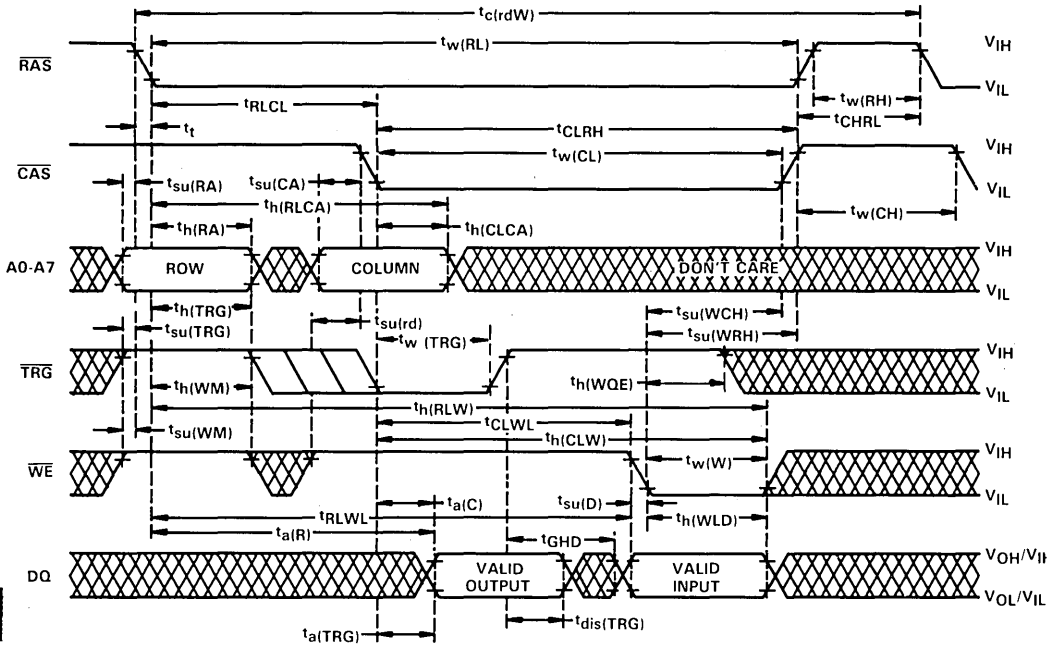
delayed write cycle timing, mask selected



read-write/read-mofidy-write cycle timing



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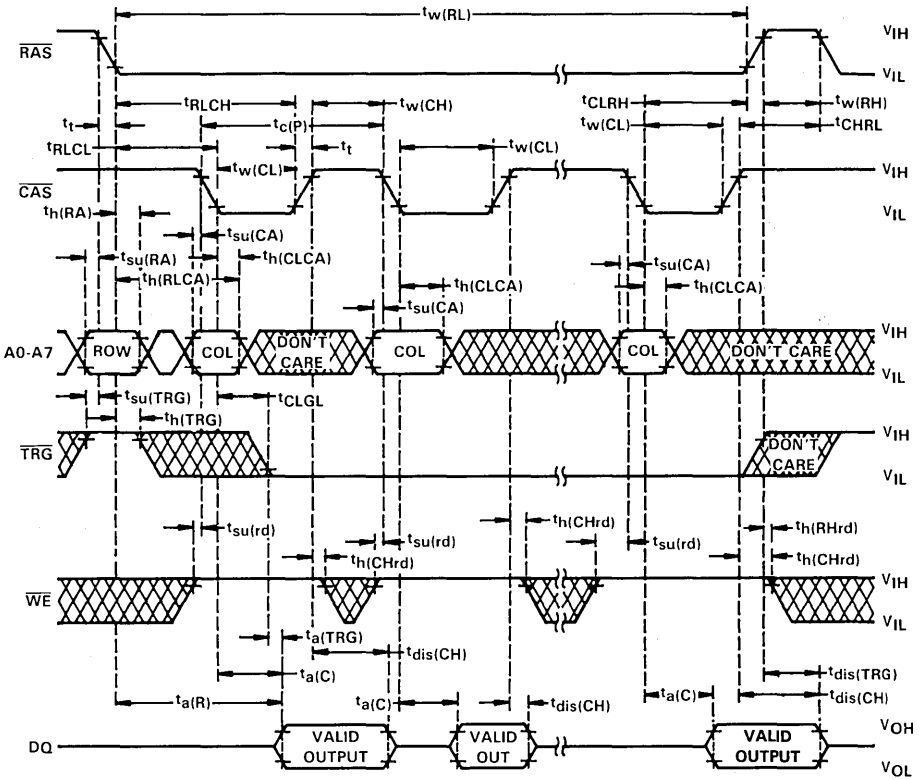
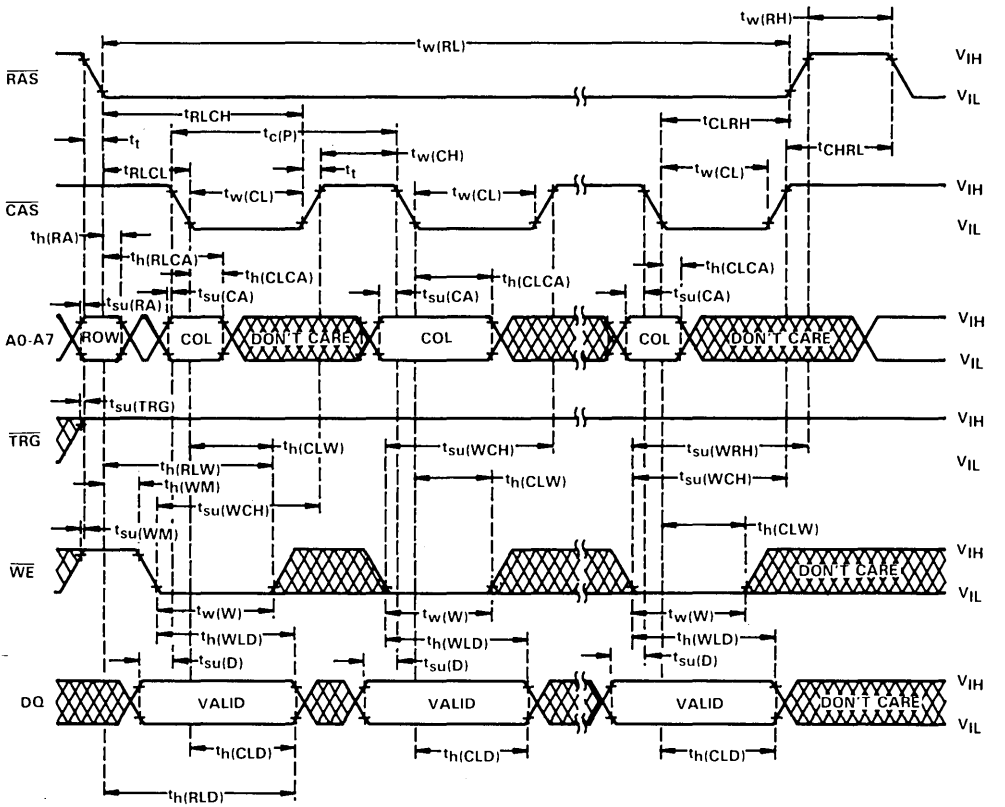
page-mode read cycle timing



page-mode write write cycle timing, write mask unselected



NOTE 7: Timing assumes use of the early write feature. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used to guarantee page-mode cycle time.

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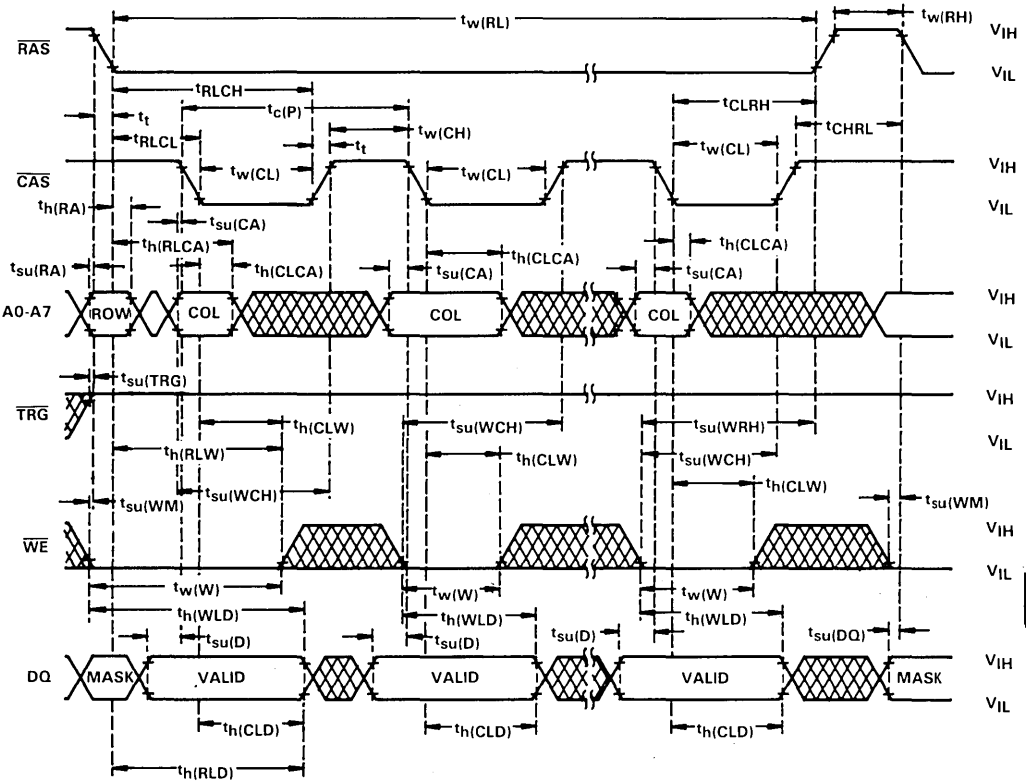
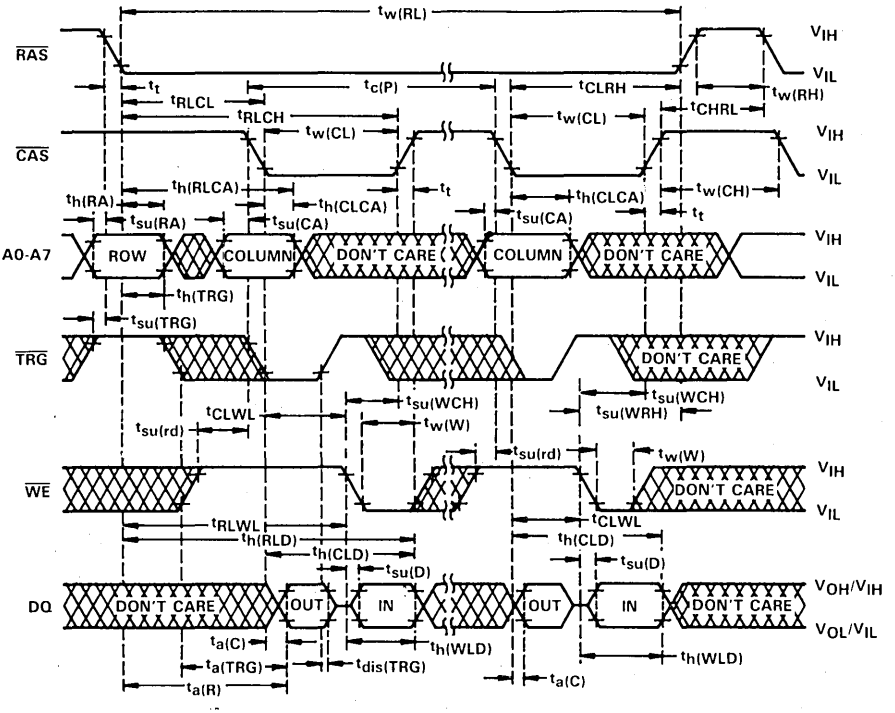
page-mode write cycle timing, write mask selected



NOTE 8: Timing assumes use of the early write feature. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used to guarantee page-mode cycle time. Timing also assumes that only those I/Os selected by DQ1-DQ4 on the falling edge of $\overline{RAS}$ are written during page-mode operation.

page-mode read-modify-write cycle timing



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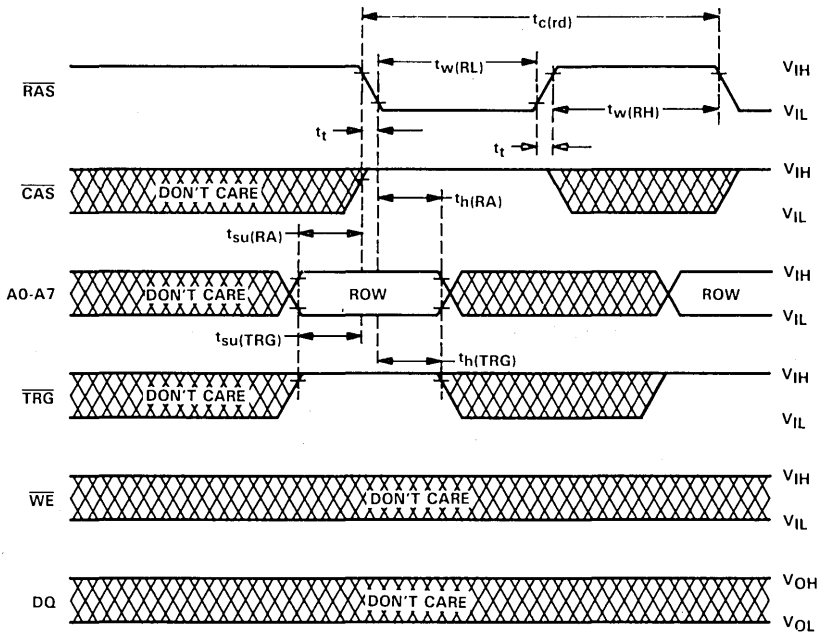
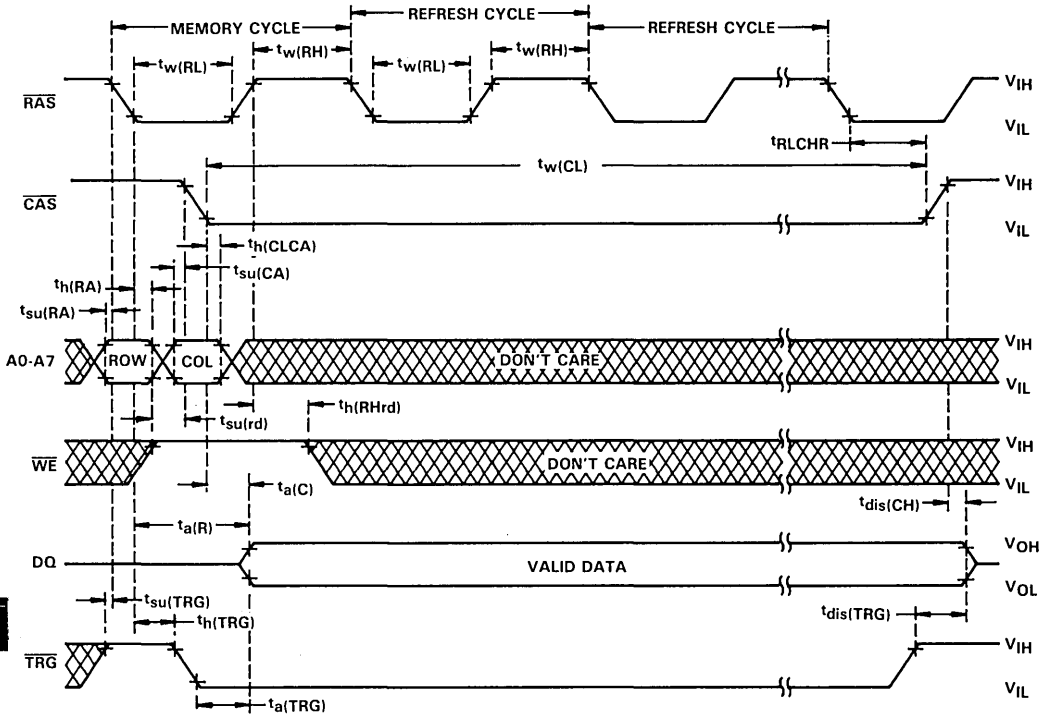
$\overline{\text{RAS}}$-only refresh timing



hidden refresh cycle timing



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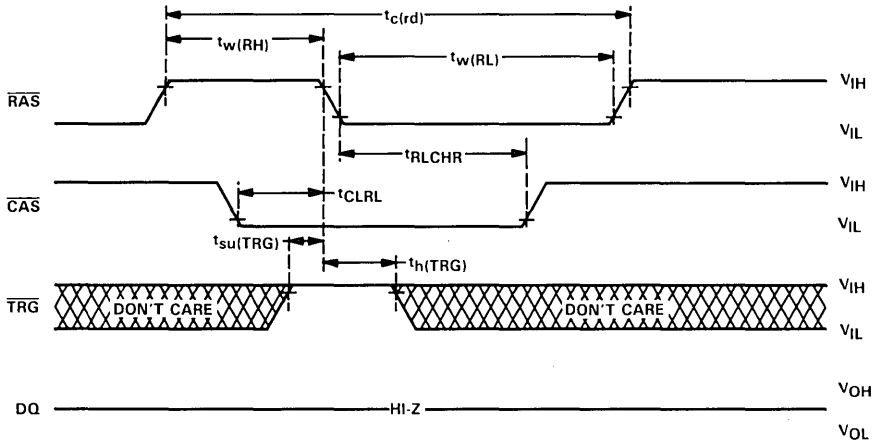
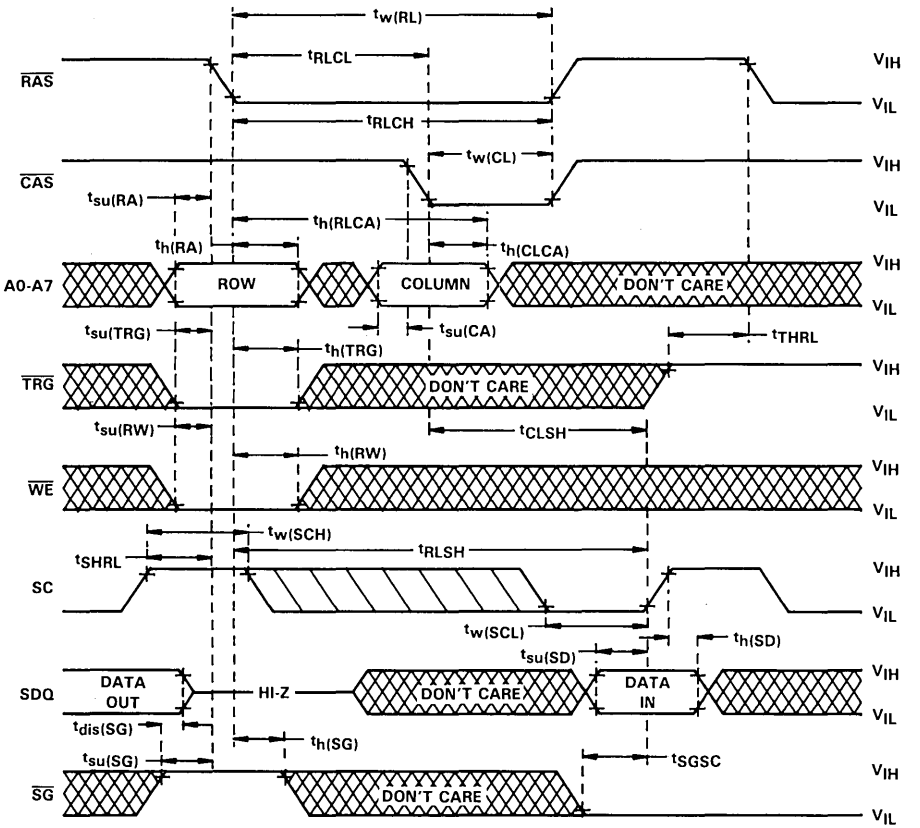
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh



write-mode control timing

The write-mode control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. The diagram below assumes that the device was originally in the serial read mode.



NOTES: 9. Random-mode (Q outputs) remain in 3-state for the entire write-mode control cycle.
10. $\overline{SG}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

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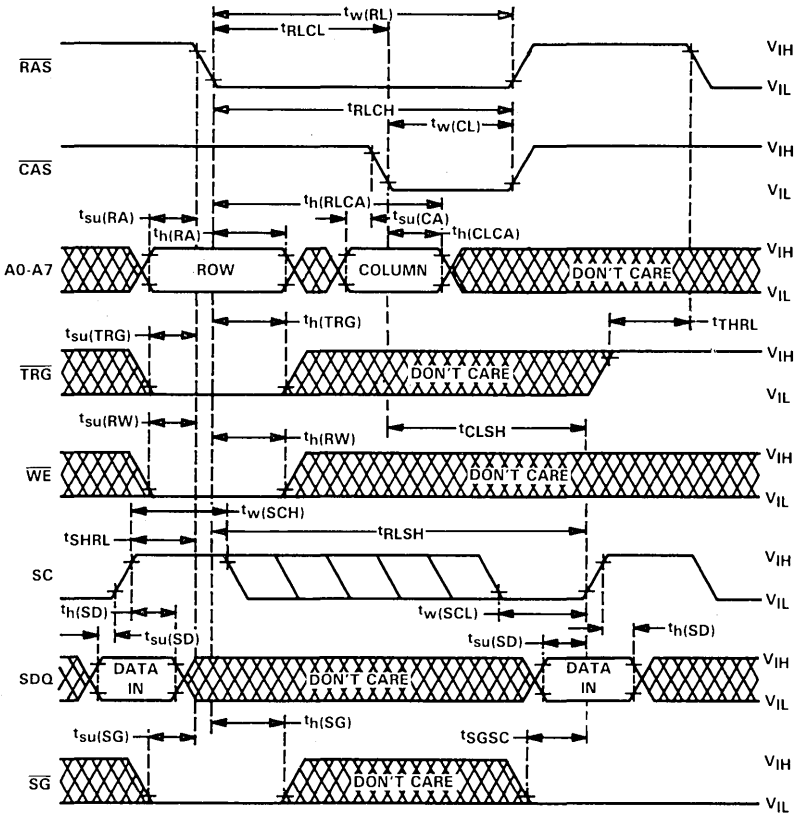
data-register-to-memory timing, serial input enabled

The data-register-to-memory cycle is used to transfer data from the data register to the memory array. Every one of the 256 locations in the data register is written into the 256 columns of the selected row. Note that the data that was in the data register may have arrived there either from a serial write in or from a parallel load of the data register from one of the memory array rows. The diagram below assumes that the device is presently in the serial-write mode (i.e., SD is enabled by a previous write-mode control cycle, thus allowing data to be written in).

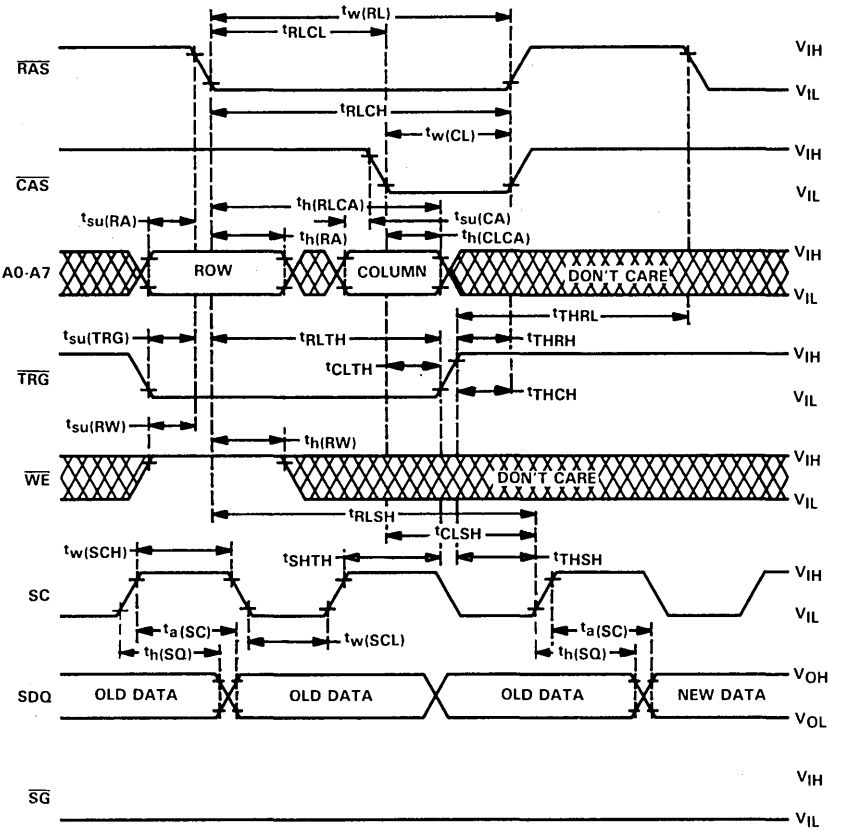


NOTES: 11. Random-mode (Q outputs) remain in 3-state for the entire data-register-to-memory transfer cycle.
12. $\overline{SG}$ must be high as $\overline{RAS}$ falls in order to perform a register-to-memory transfer.

memory-to-data-register timing

The memory-to-data-register cycle is used to load the data register in parallel from the memory array. Every one of the 256 locations in the data register are written into from the 256 columns of the selected row. Note that the data that is loaded into the data register may be either read out or written back into another row. This cycle puts the device into the serial read mode (i.e., the SQ is enabled, thus allowing data to be read out of the register).

Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.



NOTES: 13. Random-mode (Q outputs) remain in 3-state for the entire memory-to-data-register transfer cycle.
14. Column address must be supplied to load register start address on every transfer cycle.
15. The first positive transition of SC after $\overline{TRG}$ has gone high during a memory-to-register transfer cycle is used to read the first bit of new data.

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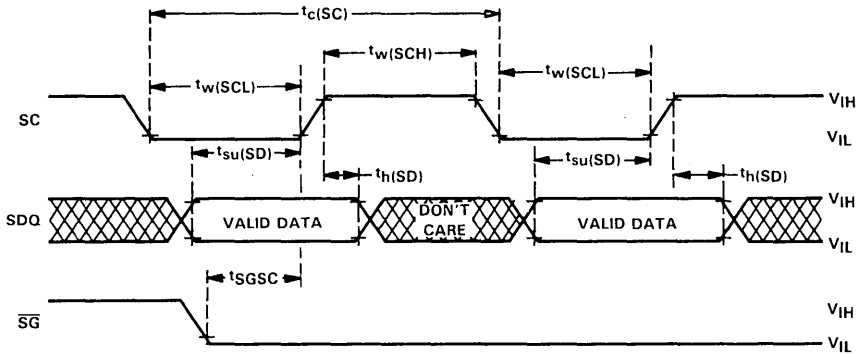
serial data-in timing

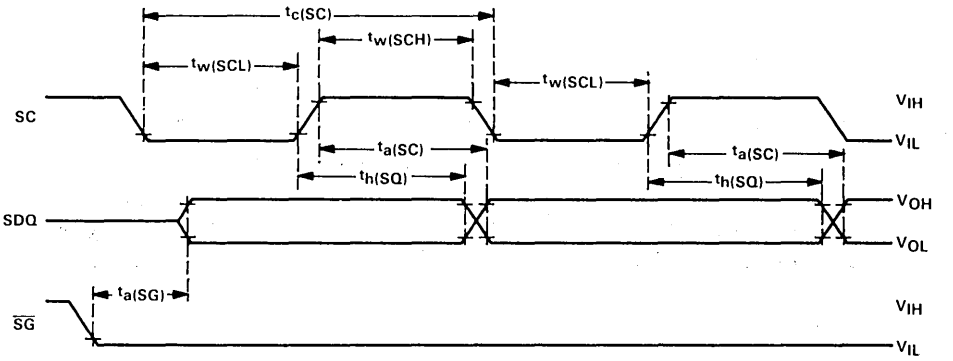
The serial data-in write cycle is used to write data into the data register. Before data can be written into the data register via SD, the device must be put into the write mode by performing a write-mode control cycle. Register-to-memory transfer cycles occurring between the write-mode control cycle and the subsequent writing in of data will not take the device out of the write mode. But a memory-to-register transfer cycle during that time will take the device out of the write mode and put it into the read mode, thus not allowing the writing in of data.



NOTE 16: While writing data into the data register, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-to-memory or memory-to-register data-transfer function.

serial-data-out timing

The serial data-out read cycle is used to read data out of the data register. Before data can be read out via SQ, the device must be put into the read mode by performing a memory-to-data-register transfer cycle. Register-to-memory transfer cycles occurring between the memory-to-register transfer cycle and the subsequent reading out of data will not take the device out of the read mode. But, a write-mode control cycle at that time will take the device out of the read mode and put it in the write mode, thus not allowing the reading out of data.



NOTE 17: While reading data out of the data register, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-to-memory or memory-to-register data-transfer operation.

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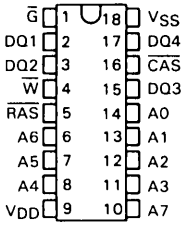
SEPTEMBER 1987

- 65,536 × 4 Organization
- Single 5-V Supply (10% Tolerance)
- JEDEC Standardized Pinout
- Pinout Identical to SMJ4416 (16K × 4 Dynamic RAM)
- Performance Ranges:

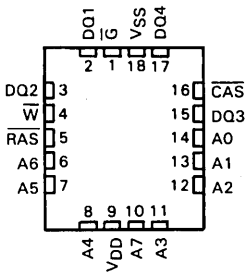
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
SMJ4464-12	120 ns	60 ns	230 ns	320 ns
SMJ4464-15	150 ns	75 ns	260 ns	345 ns
SMJ4464-20	200 ns	100 ns	330 ns	435 ns

- Long Refresh Period . . . 4 ms (Max)
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- On-Chip Substrate Bias Generator
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Early Write or $\overline{G}$ to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Power Dissipation As Low As:
  - Operating . . . 275 mW (Typ)
  - Standby . . . 12.5 mW (Typ)
- $\overline{RAS}$-Only Refresh Mode
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Mode

JD PACKAGE
(TOP VIEW)



FV PACKAGE
(TOP VIEW)



NOTE: Pin 1 indicator on back.

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Addreess Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The SMJ4464 is a high-speed, 262,144-bit dynamic random-access memory, organized as 65,536 words of four bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

This device features maximum $\overline{RAS}$ access times of 120 ns, 150 ns, or 200 ns. Typical power dissipation is as low as 275 mW operating and 12.5 mW standby.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks of 125 mA are typical, and a −0.7-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All address and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ4464 is offered in 18-pin 300-mil ceramic side-braze dual-in-line and 18-pad leadless ceramic chip carrier packages. It is guaranteed for operation from −55°C to 110°C for the S version and from 0°C to 70°C for the L version. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers).

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (DQ1-DQ4)

Data is written during a write or a read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or a read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed or read-modify write cycle, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(G)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high-impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying t_{GHD}.

output enable ($\overline{G}$)

The $\overline{G}$ input controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state they will remain in the low-impedance state until $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state.

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operation (continued)

CAS-before-RAS refresh

The CAS-before-RAS refresh is utilized by bringing CAS low earlier than RAS (see parameter t_{CLRL}) and holding it low after RAS falls (see parameter t_{RLCHR}). For successive CAS-before-RAS refresh cycles, CAS can remain low while cycling RAS. The external address is ignored and the refresh address is generated internally.

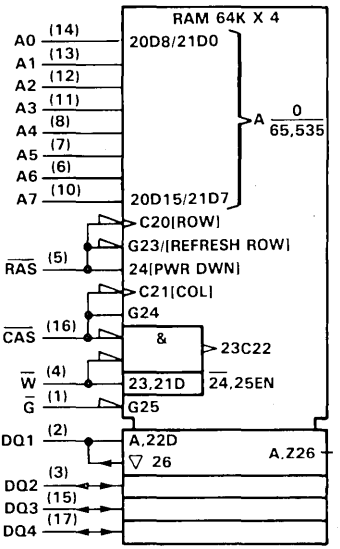
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe sequential row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by $t_{W(RL)}$, the maximum RAS low pulse duration.

power up

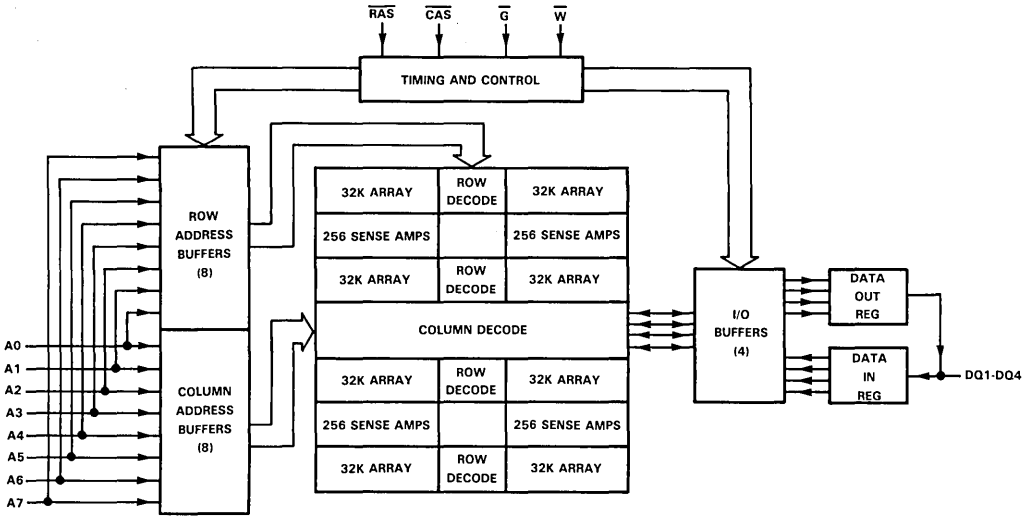
To achieve proper device operation, an initial pause of 200 μs is required after power up, followed by a minimum of eight initialization cycles.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the dual-in-line package.

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage on any pin including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Minimum operating free-air temperature: S version . . . . . −55°C
L version . . . . . 0°C
Maximum operating case temperature: S version . . . . . 110°C
L version . . . . . 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		S VERSION			L VERSION			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{DD}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{SS}	Supply voltage		0			0		V
V_{IH}	High-level input voltage	2.4		$V_{DD}+0.3$	2.4		$V_{DD}+0.3$	V
V_{IL}	Low-level input voltage (see Note 2)	−0.7		0.7	−0.7		0.7	V
T_A	Operating free-air temperature	−55			0			°C
T_C	Operating case temperature			110			70	°C

NOTE 2: The algebraic convention, where the negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4464-12			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All outputs open			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		65	80	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		2.5	8	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high, All outputs open		50	60	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open		45	55	mA

PARAMETER		TEST CONDITIONS	SMJ4464-15			SMJ4464-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All outputs open			±10			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		55	70		50	60	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		2.5	8		2.5	8	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high, All outputs open		45	55		40	50	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open		40	50		30	40	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating temperature range, f = 1 MHz

PARAMETER		SMJ4464		UNIT
		TYP†	MAX	
$C_{i(A)}$	Input capacitance, address inputs	4		pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8		pF
$C_{i(W)}$	Input capacitance, write enable input	8		pF
$C_{i/o}$	Output capacitance	8		pF

†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS‡	ALT. SYMBOL	SMJ4464-12		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{CAC}		60	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{RLCL} \geq$ MAX, C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{RAC}		120	ns
$t_{a(G)}$§	Access time after $\overline{G}$ low	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{GAC}		35	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{OFF}	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{GOFF}	0	38	ns

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS‡	ALT. SYMBOL	SMJ4464-15		SMJ4464-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{CAC}		75		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{RLCL} \geq$ MAX, C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{RAC}		150		200	ns
$t_{a(G)}$§	Access time after $\overline{G}$ low	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{GAC}		45		55	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{OFF}	0	30	0	35	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{GOFF}	0	38	0	38	ns

‡Figure 1 shows the load circuit; C_L values shown are typical for test system used.
§$t_{a(C)}$ and $t_{a(R)}$ must be satisfied to guarantee $t_{a(G)}$.

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timing requirements over recommended supply voltage range and operating temperature range

		ALT. SYMBOL	SMJ4464-12 MIN	SMJ4464-12 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	120		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	205		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	320		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	60	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	10		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early-write command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	80		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	35		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	35		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	25		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RCP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{CWD}	100		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	25		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{RWD}	160		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{GDD}	25		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

† All cycle times assume t_t = 5 ns.
‡ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).
§ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).
¶ $\overline{CAS}$-before-$\overline{RAS}$ refresh option only.
# $\overline{G}$ must disable the output buffers prior to applying data to the device.
NOTE 3: System transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

timing requirements over recommended supply voltage range and operating temperature range

		ALT. SYMBOL	SMJ4464-15 MIN	SMJ4464-15 MAX	SMJ4464-20 MIN	SMJ4464-20 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	145		190		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	230		295		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		435		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	60		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	75	10,000	100	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	10		10		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early-write command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		145		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		35		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RCP}	10		15		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		100		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{CWD}	110		140		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		35		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	75	30	100	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{RWD}	185		240		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{GDD}	25		35		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

† All cycle times assume t_t = 5 ns.
‡ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).
§ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).
¶ $\overline{CAS}$-before-$\overline{RAS}$ refresh option only.
# $\overline{G}$ must disable the output buffers prior to applying data to the device.
NOTE 3: System transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

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PARAMETER MEASUREMENT INFORMATION

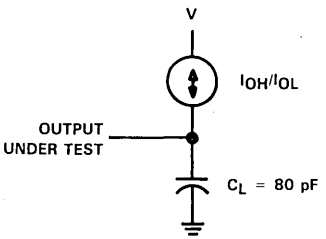
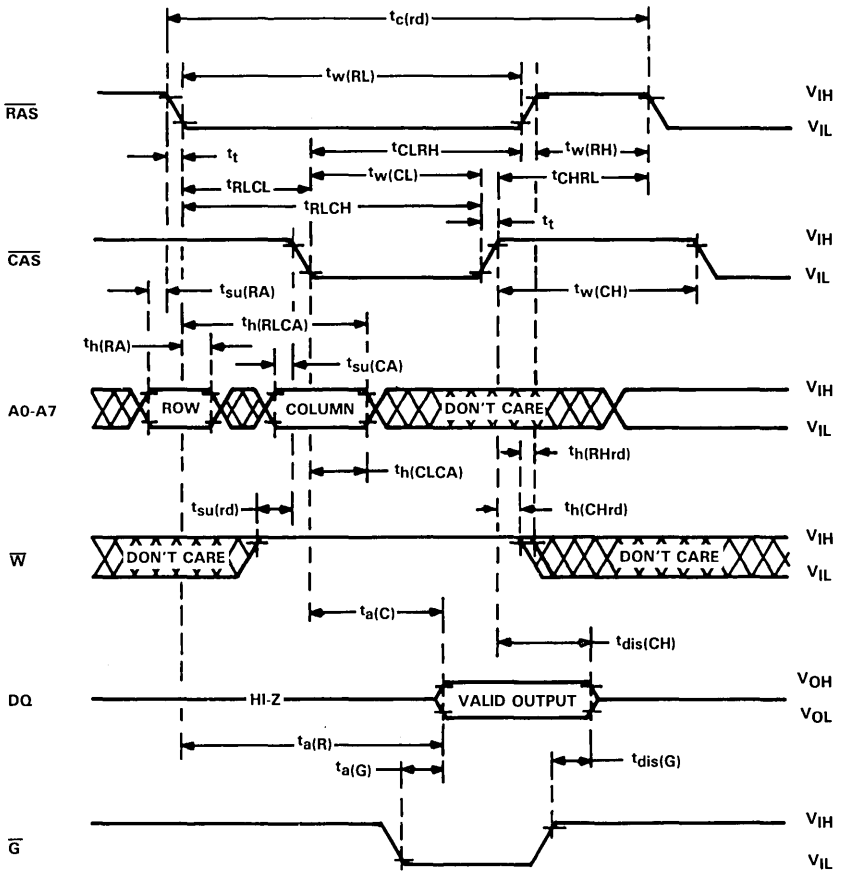


FIGURE 1. TYPICAL LOAD CIRCUIT

read cycle timing



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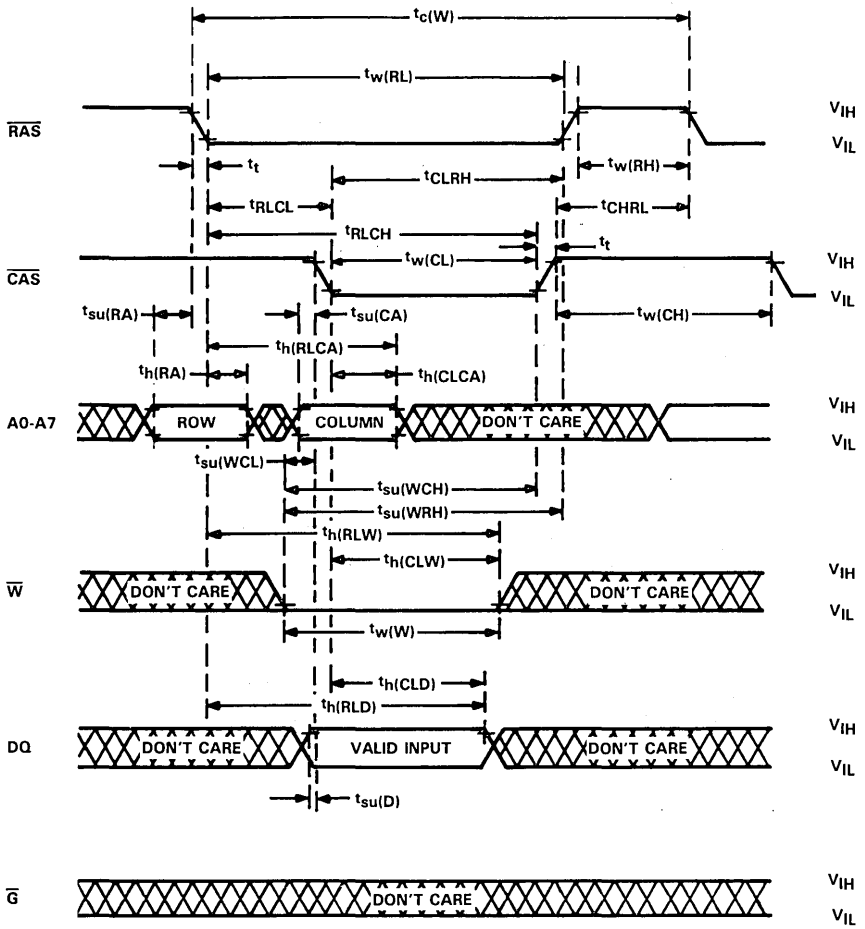
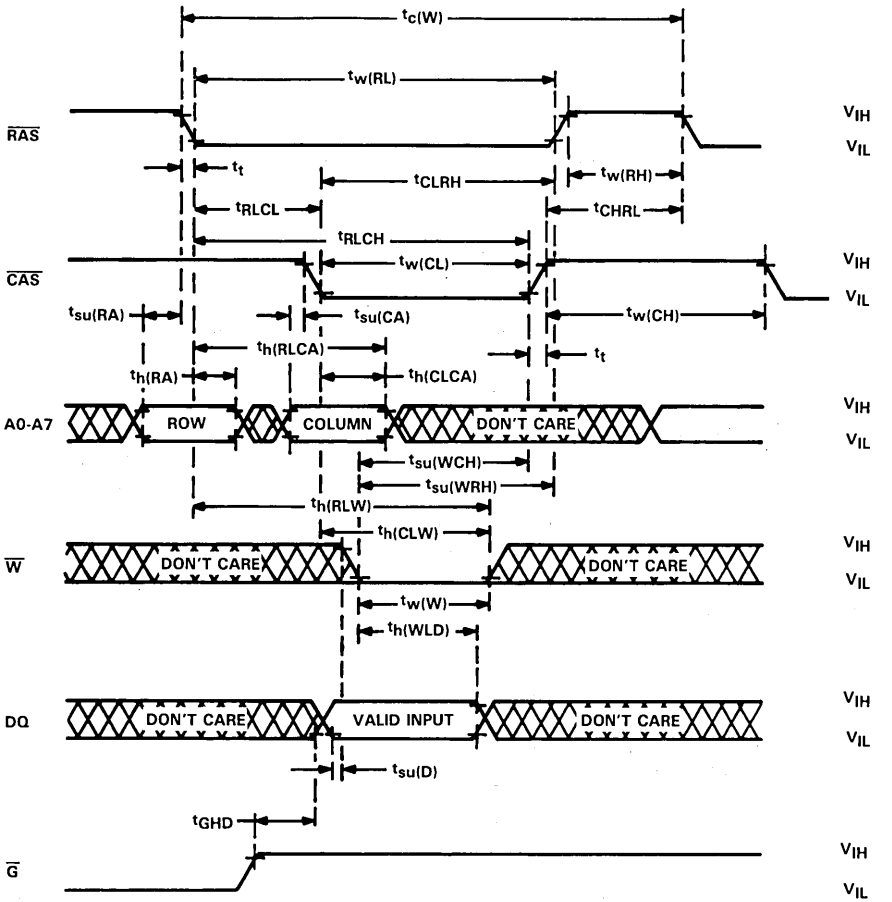
early write cycle timing



write cycle timing



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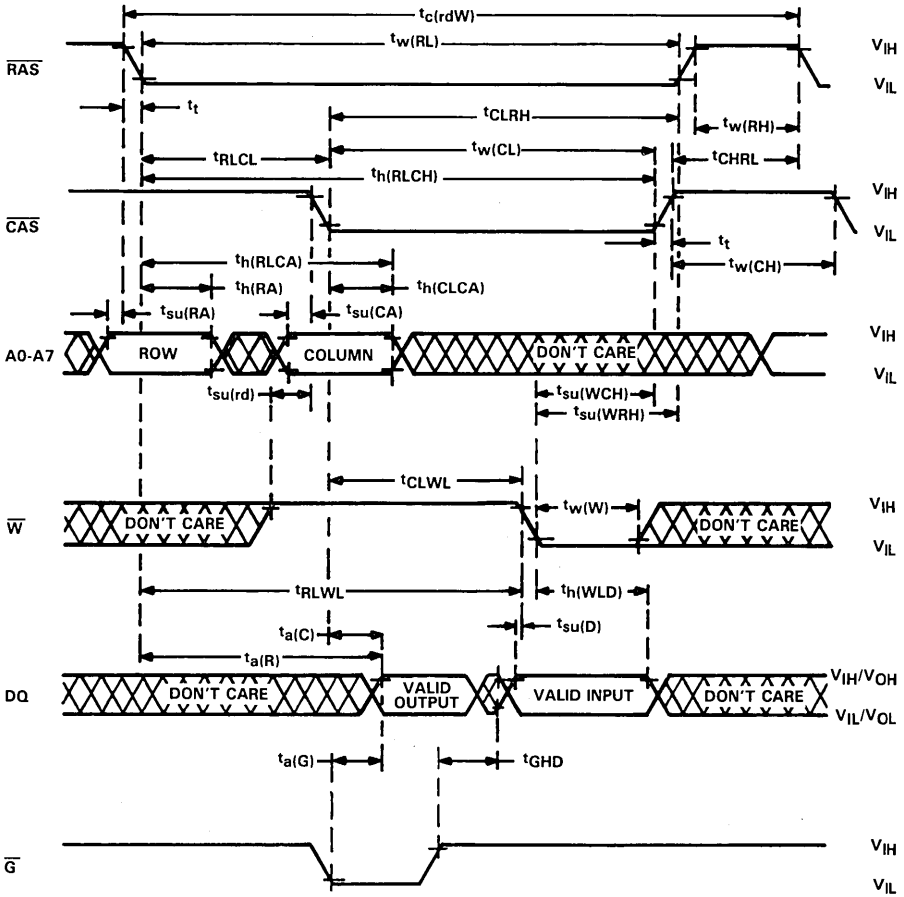
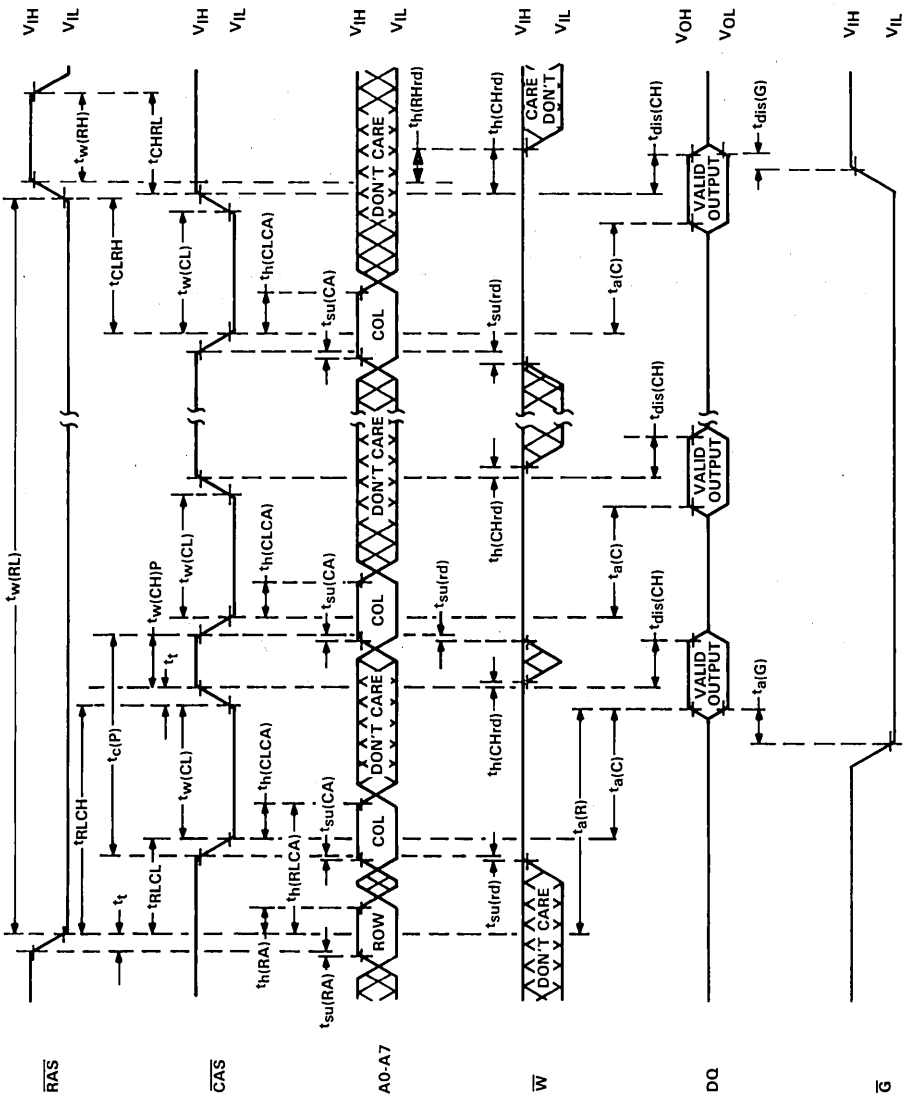
read-write/read-modify-write cycle timing



page-mode read cycle timing



NOTE 4: A write cycle or read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

8 Military Products

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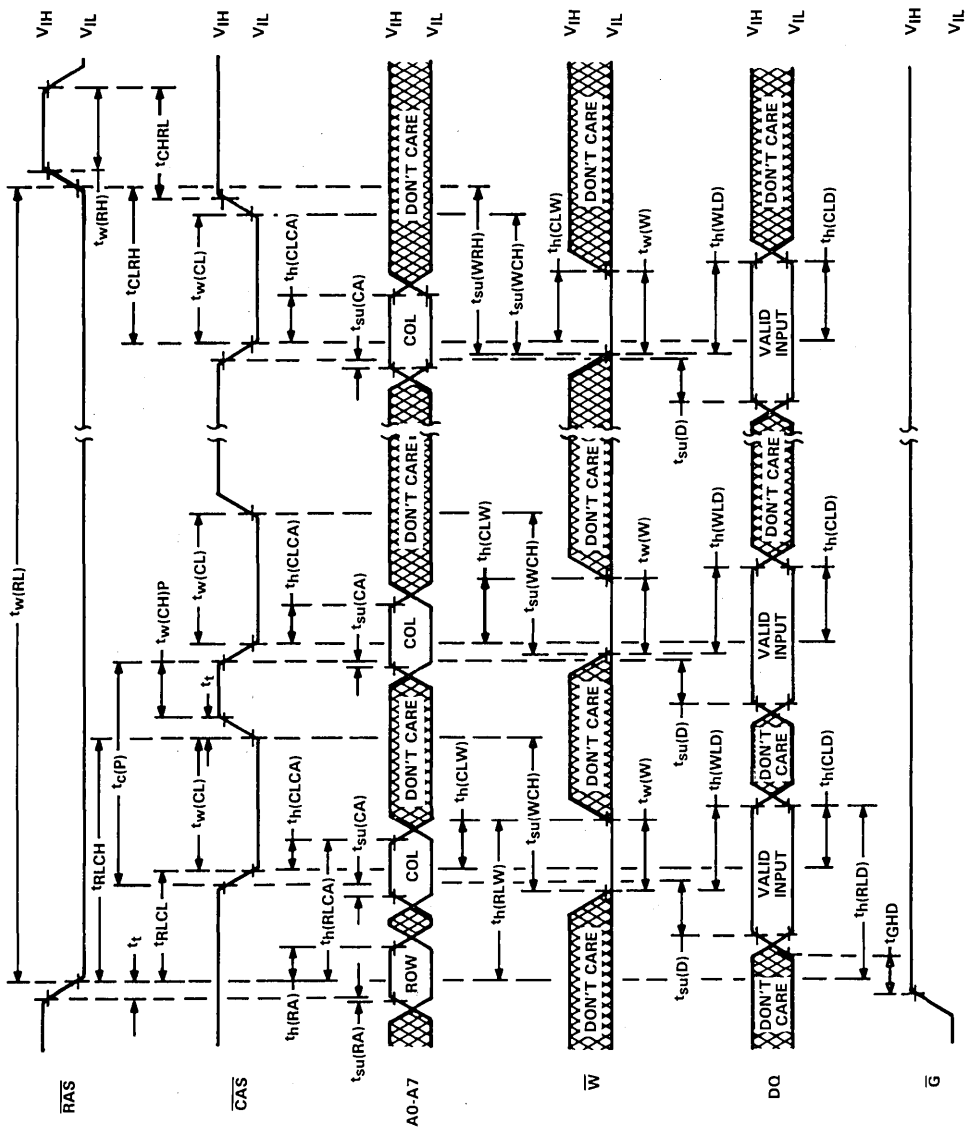
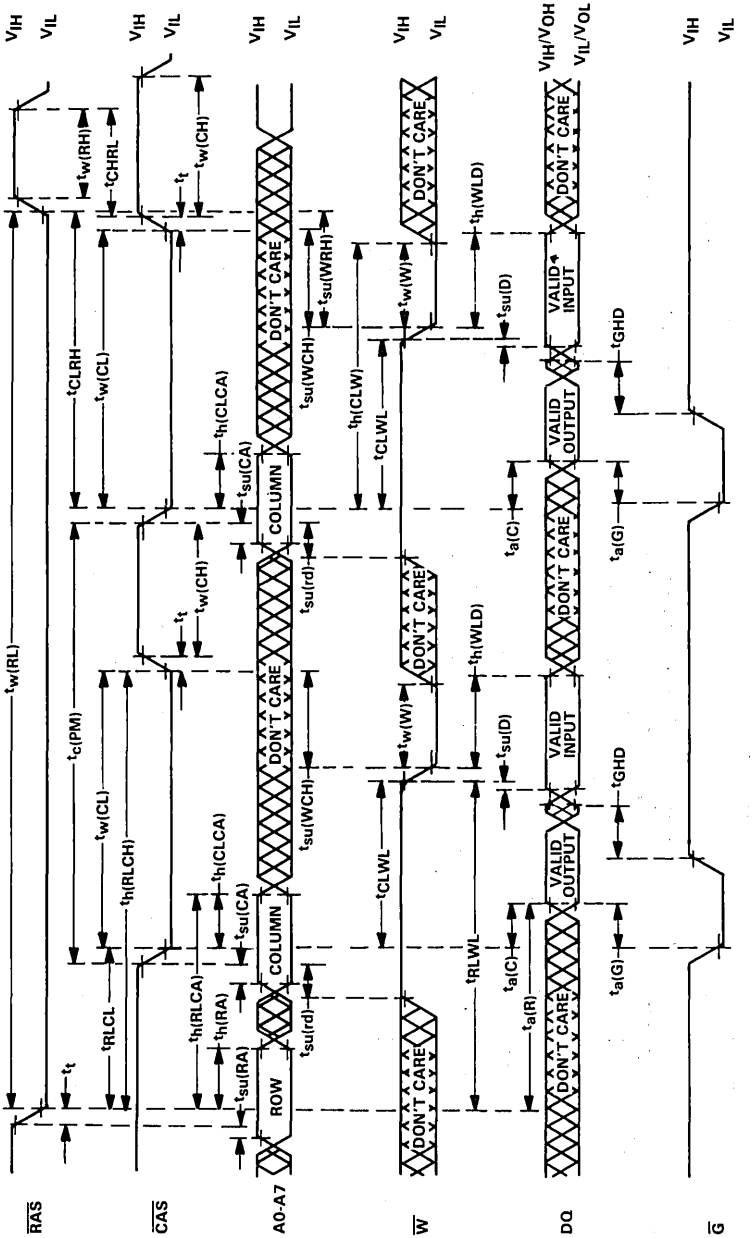
page-mode write cycle timing



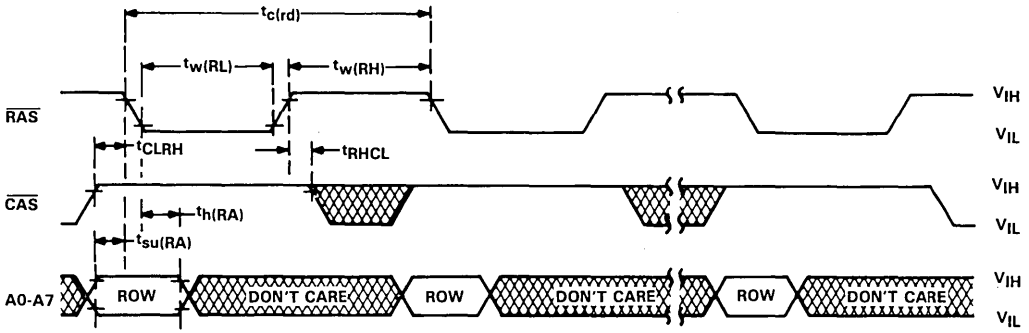
NOTE 5: A read cycle or read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

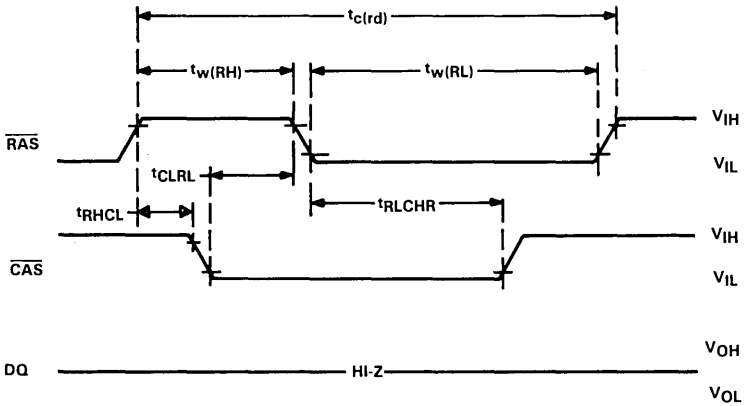


NOTE 6: A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{RAS}$-only refresh cycle timing



$\overline{CAS}$-before-$\overline{RAS}$ refresh cycle timing



8 Military Products

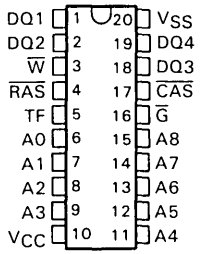
FEBRUARY 1988

- **262,144 × 4 Organization**
- **Single 5-V Supply (10% Tolerance)**
- **Performance Ranges:**

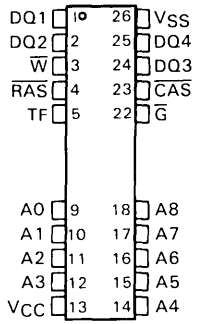
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ44C256-12	120 ns	35 ns	60 ns	230 ns
SMJ44C256-15	150 ns	45 ns	75 ns	270 ns

- **SMJ44C256 — Enhanced Page Mode Operation**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  512-Cycle Refresh in 8 ms (Max)
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs and Clocks Are TTL Compatible**
- **High-Reliability Ceramic 20-Pin 300-Mil-Wide DIP or 20/26-Lead Ceramic Surface Mount (CSOJ) Package**
- **−55°C to 125°C Operating Temperature Range**
- **Standard and Class B Processing**
  −SM44C256 . . . Standard
  −SMJ44C256 . . . Class B

JD PACKAGE
(TOP VIEW)



HJ PACKAGE†
(TOP VIEW)



†The packages shown here are for pinout reference only. The HJ package is actually 75% of the length of the JD package.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Data-Output Enable
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The SMJ44C256 is a high-speed, 1,048,576-bit dynamic random-access memory organized as 262,144 words of four bits each. It employs state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold, and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

EPIC is a trademark of Texas Instruments Incorporated.

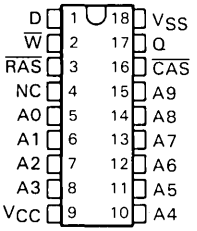
FEBRUARY 1988

- 1,048,576 × 1 Organization
- Single 5-V Supply (10% Tolerance)
- Performance Ranges:

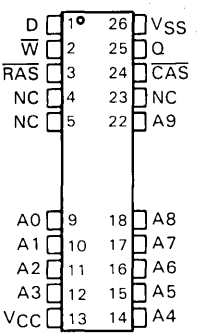
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ4C1024-12	120 ns	35 ns	60 ns	230 ns
SMJ4C1024-15	150 ns	45 ns	75 ns	270 ns

- SMJ4C1024 — Enhanced Page Mode Operation
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)
- 3-State Unlatched Output
- Low Power Dissipation
- Texas Instruments EPIC™ CMOS Process
- All Inputs and Clocks Are TTL Compatible
- High-Reliability Ceramic 18-Pin 300-Mil-Wide DIP or 20/26 Ceramic Surface Mount (CSOJ) Package
- −55°C to 125°C Operating Temperature Range
- Standard and Class B Processing
  —SM4C1024 . . . Standard
  —SMJ4C1024 . . . Class B

JD PACKAGE
(TOP VIEW)



HJ PACKAGE†
(TOP VIEW)



†The packages shown here are for pinout reference only. The HJ package is actually 75% of the length of the JD package.

PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The SMJ4C1024 is a high-speed, 1,048,576-bit dynamic random-access memory organized as 1,048,576 words of one bit each. It employs state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

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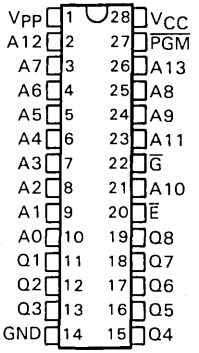
AUGUST 1986—REVISED JULY 1987

- Organization . . . 16K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 64K and 128K EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time
  SMJ27C128-20 200 ns
  SMJ27C128-25 250 ns
  SMJ27C128-30 300 ns
- HVCMOS Technology
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation (V_{CC} = 5.5 V)
  —Active . . . 220 mW Worst Case
  —Standby . . . 1.7 mW Worst Case (CMOS-Input Levels)
- Temperature Range . . .
  −55°C to 125°C

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A13	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12.5-V Power Supply

description

The SMJ27C128 series are 131,072-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 54 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The SMJ27C128 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation from −55°C to 125°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed individually, in blocks, or at random.

operation

There are seven modes of operation for the SMJ27C128 listed on the following page. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

FUNCTION (PINS)	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$ (22)	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	V_{IH}	V_{IL}	
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X	V_{IH}	
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8 (11-13, 15-19)	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	CODE	
							MFG	DEVICE
							97	04

†X can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more SMJ27C128's are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the SMJ27C128, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8.

power down

Active I_{CC} current can be reduced from 40 mA to 500 μA (TTL-level inputs) or 300 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C128 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 milliwat per square centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C128, the window should be covered with an opaque label.

fast programming

After erasure (all bits in logic '1' state), logic '0's are programmed into the desired locations. A programmed '0' can only be erased by ultraviolet light. Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, V_{CC} = 6.0 V, $\overline{G}$ = V_{IH}, $\overline{PGM}$ = V_{IL}, and $\overline{E}$ = V_{IL}. More than one SMJ27C128 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified.

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If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6.0 V and V_{PP} = 12.5 V. When the full fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V (see Figure 1).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin or $\overline{PGM}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10) i.e., A0 = V_{IL} – manufacturer; A0 = V_{IH} – device. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for this device is 97, and the device code is 04.

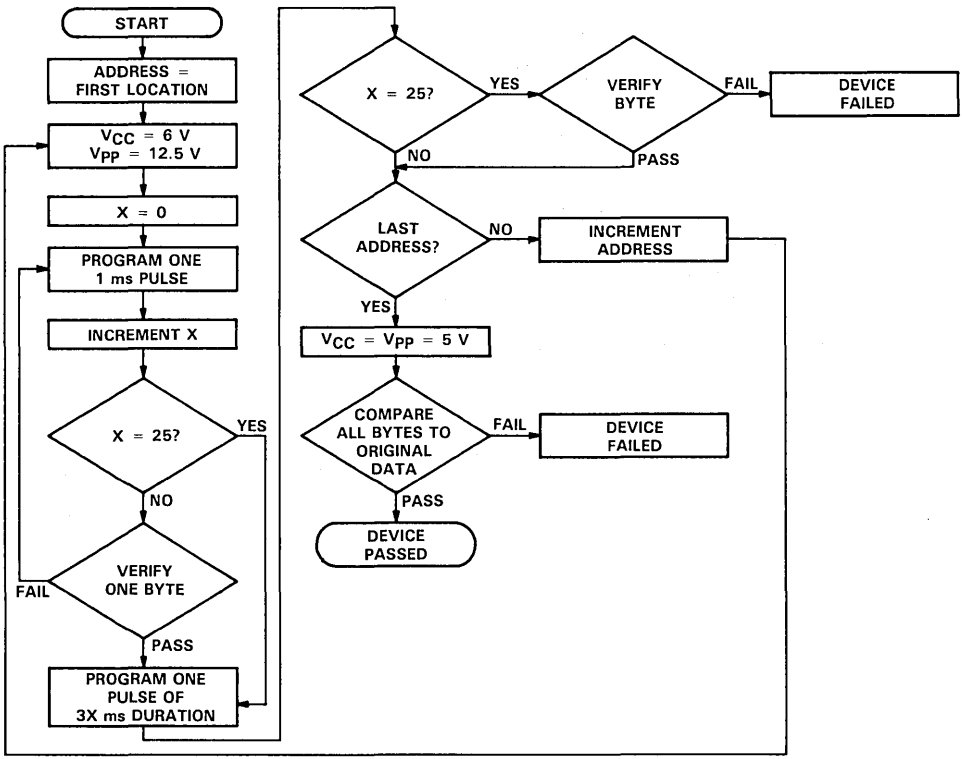
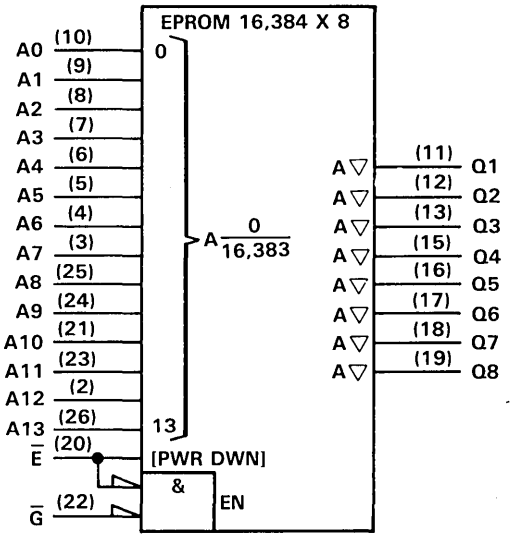


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1)	−0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9	−0.6 V to 6.5 V
A9	−0.6 V to 13.5 V
Output voltage range (see Note 1)	−0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature	−55°C
Operating case temperature	125°C
Storage temperature range	−65°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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recommended operating conditions

			SMJ27C128-20 SMJ27C128-25 SMJ27C128-30			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		4.5	5	5.5	V
V_{PP}	Supply voltage (see Note 3)			V_{CC}		V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+0.2$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	V
		CMOS	GND−0.2		GND+0.2	V
T_A	Operating free-air temperature		−55			°C
T_C	Operating case temperature				125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC}+I_{PP}$. During programming, V_{PP} must be maintained at 12.5 V (±0.5V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±10	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±10	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V			100	μA
I_{PP2}	V_{PP} supply current‡ (during program pulse)		V_{PP} = 13 V		30	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			300	μA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		10	25	mA

†Typical values are at T_A = 25°C and nominal voltages.
‡This parameter has been characterized at 25°C and is not tested.

capacitance, T_C = 25°C, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	10	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		8	14	pF

†Capacitance measurements are made on sample basis only.
‡Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C128-20		'27C128-25		'27C128-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	See Figure 2.		200		250		300	ns
$t_{a(E)}$	Access time from chip enable			200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100		120	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	105	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.40 V to 2.4 V and V_{PP} = 12.5 V ±0.5 V during programming. $t_r \leq 20$ ns and $t_f \leq 20$ ns.
5. Common test conditions apply for $t_{dis(G)}$ except during programming.
†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

recommended timing requirements for programming, T_A = 25°C, V_{CC} = 6 V, V_{PP} = 12.5 V (see Note 4)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	2.85		78.75	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs

NOTES: 4. For all switching characteristics and timing measurements input pulse levels are 0.40 V to 2.4 V and V_{PP} = 12.5 V ±0.5 V during programming.
5. Common test conditions apply for $t_{dis(G)}$ except during programming.

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PARAMETER MEASUREMENT INFORMATION

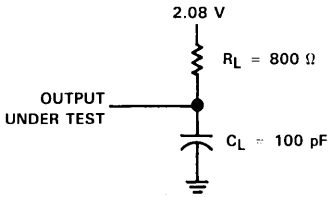
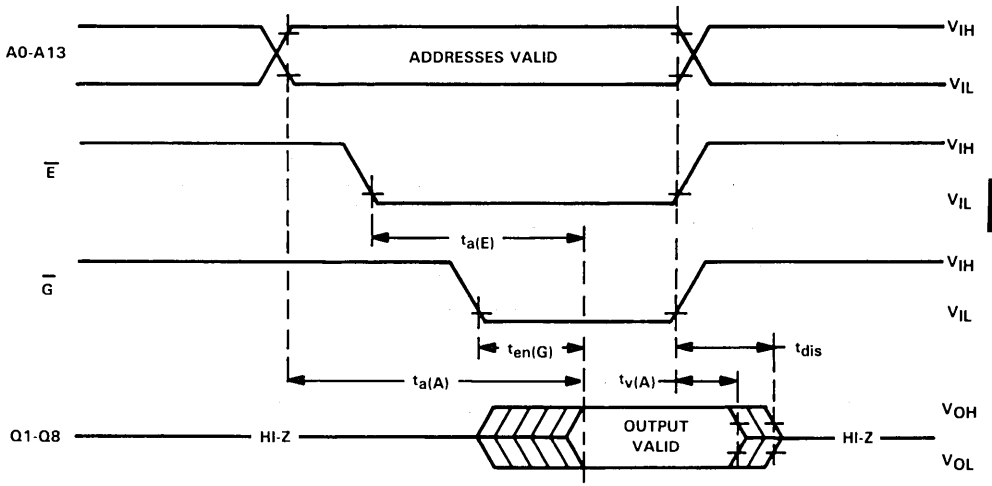
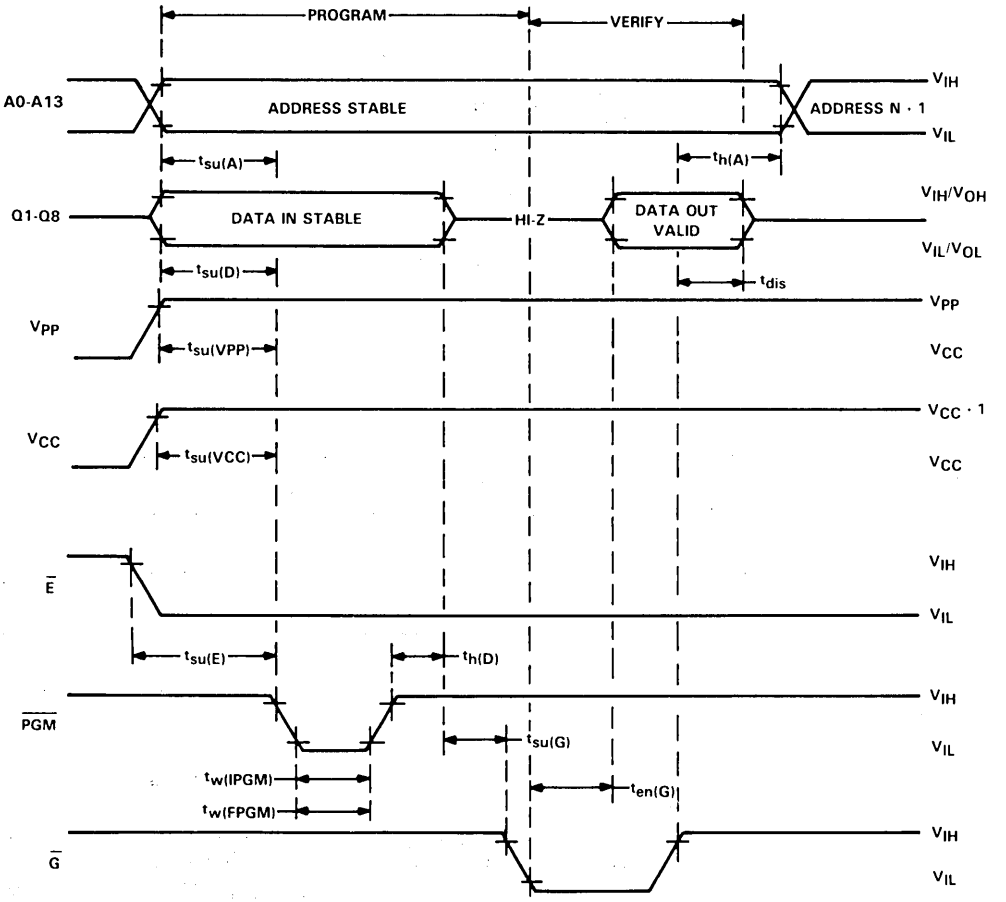


FIGURE 2. OUTPUT LOAD CIRCUIT

read cycle timing



program cycle timing



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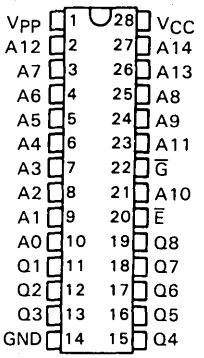
MAY 1986—REVISED JULY 1987

- Organization . . . 32K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 128K and 256K EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time
  SMJ27C256-20 200 ns
  SMJ27C256-25 250 ns
  SMJ27C256-30 300 ns
- HVCMOS Technology
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation (V_{CC} = 5.5 V)
  —Active . . . 220 mW Worst Case
  —Standby . . . 1.7 mW Worst Case (CMOS-Input Levels)
- Temperature Range . . .
  —55°C to 125°C
- MIL-STD-883C Class B High-Reliability Processing

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12.5-V Power Supply

description

The SMJ27C256 series are 262,144-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 54 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The SMJ27C256 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation from −55°C to 125°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation for the SMJ27C256 listed on the following page. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

FUNCTION (PINS)	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$ (22)	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	V_{IH}	V_{IL}	
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8 (11-13, 15-19)	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	CODE	
							MFG	DEVICE
							97	04

†X can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more SMJ27C256's are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the SMJ27C256, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8.

power down

Active I_{CC} current can be reduced from 40 mA to 500 μA (TTL-level inputs) or 300 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C256 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 milliwat per square centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C256, the window should be covered with an opaque label.

fast programming

After erasure (all bits in logic '1' state), logic '0's are programmed into the desired locations. A programmed '0' can only be erased by ultraviolet light. Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{E}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, V_{CC} = 6.0 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one SMJ27C256 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional

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1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6.0 V and V_{PP} = 12.5 V. When the full fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V (see Figure 1).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL}, and $\overline{E}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10) i.e., A0 = V_{IL} – manufacturer; A0 = V_{IH} – device. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for this device is 97, and the device code is 04.

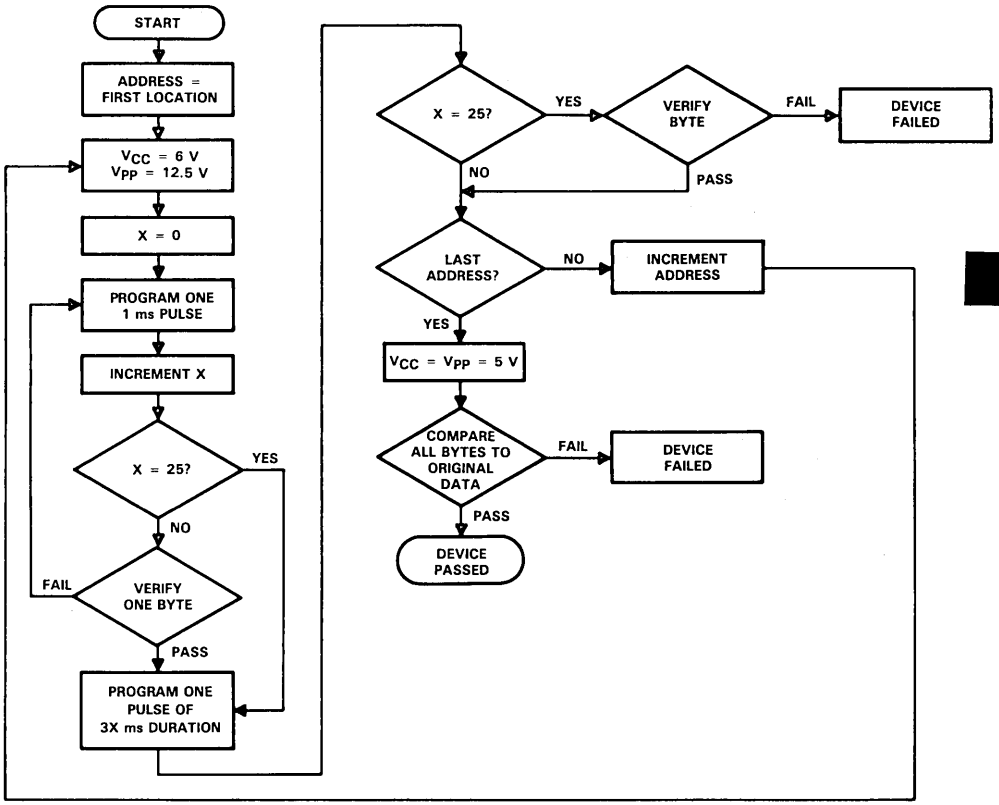
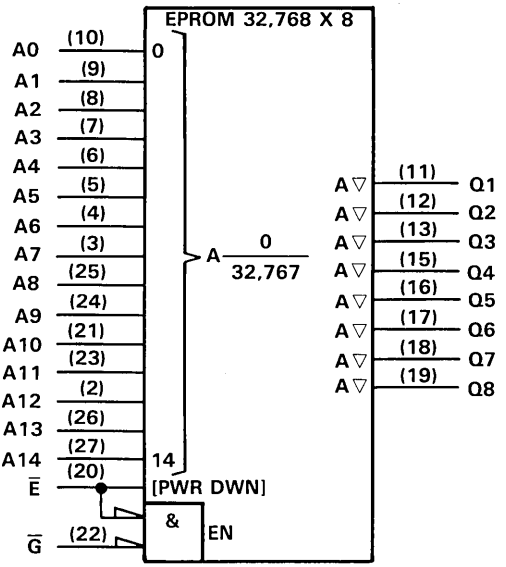


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1)	−0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9	−0.6 V to 6.5 V
A9	−0.6 V to 13.5 V
Output voltage range (see Note 1)	−0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature	−55°C
Maximum operating case temperature	125 °C
Storage temperature range	−65°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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recommended operating conditions

			SMJ27C256-20 SMJ27C256-25 SMJ27C256-30			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		4.5	5	5.5	V
V_{PP}	Supply voltage (see Note 3)			V_{CC}		V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+0.2$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	V
		CMOS	GND−0.2		GND+0.2	V
T_A	Operating free-air temperature		−55			°C
T_C	Operating case temperature				125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC}+I_{PP}$. During programming, V_{PP} must be maintained at 12.5 V (±0.5V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±10	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±10	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V			100	μA
I_{PP2}	V_{PP} supply current‡ (during program pulse)		V_{PP} = 13 V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			300	μA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		10	25	mA

†Typical values are at T_A = 25°C and nominal voltages.
‡This parameter has been characterized at 25°C and is not tested.

capacitance, T_C = 25°C, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	9	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		8	12	pF

†Capacitance measurements are made on sample basis only.
‡Typical values are at T_C = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C256-20		'27C256-25		'27C256-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 54 TTL Load, Input $t_r \leq$20 ns, Input $t_f \leq$20 ns		200		250		300	ns
$t_{a(E)}$	Access time from chip enable			200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100		120	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	105	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.40 V to 2.4 V and V_{PP} = 12.5 V ±0.5 V during programming.
5. Common test conditions apply for $t_{dis(G)}$ except during programming.
†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

recommended timing requirements for programming, T_A = 25°C, V_{CC} = 6 V, V_{PP} = 12.5 V (see Note 4)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	2.85		78.75	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs

NOTES: 4. For all switching characteristics and timing measurements input pulse levels are 0.40 V to 2.4 V and V_{PP} = 12.5 V ±0.5 V during programming.
5. Common test conditions apply for $t_{dis(G)}$ except during programming.

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PARAMETER MEASUREMENT INFORMATION

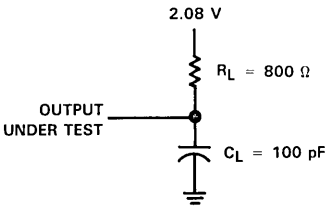
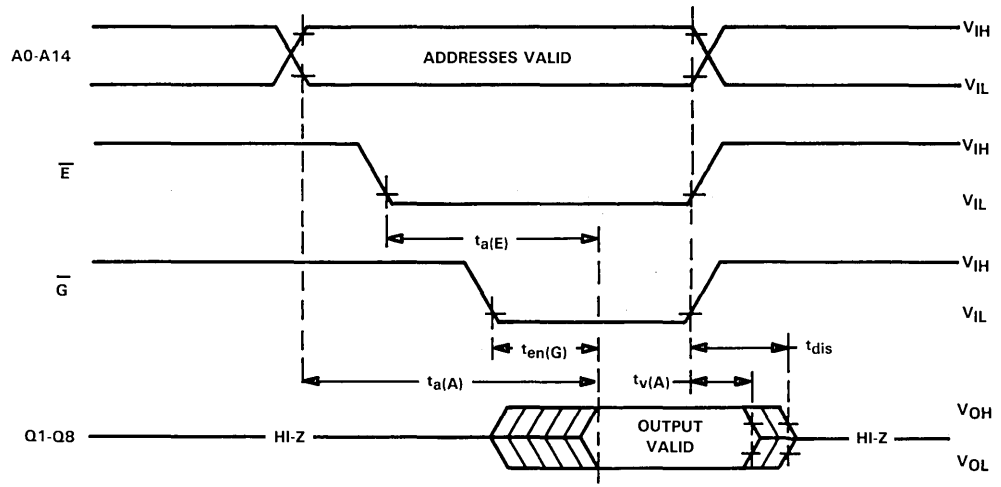
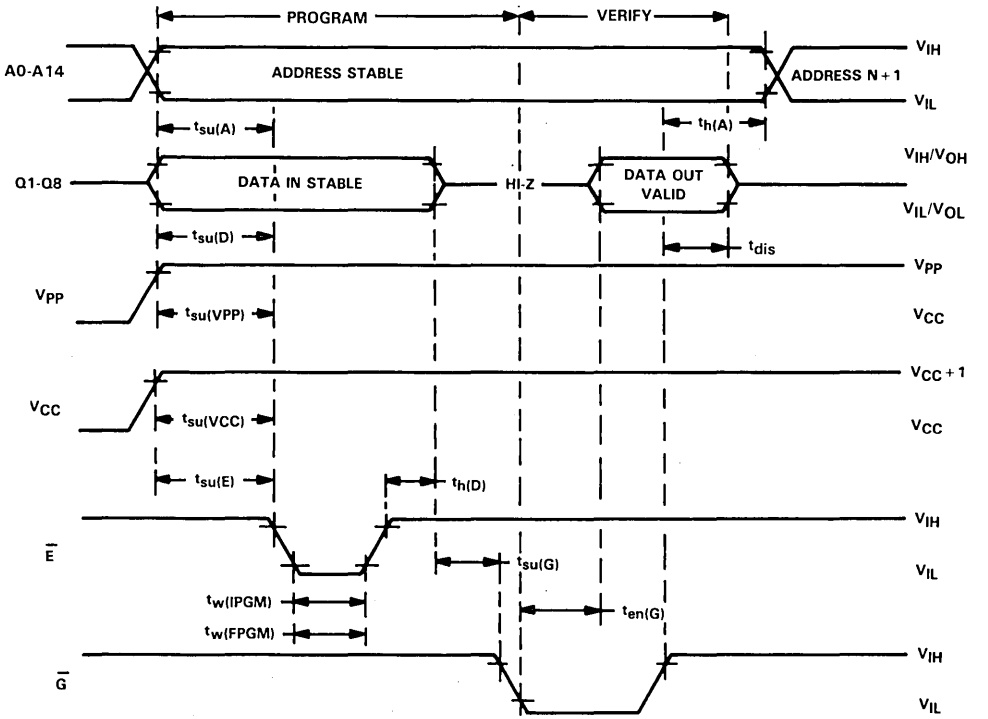


FIGURE 2. OUTPUT LOAD CIRCUIT

read cycle timing



program cycle timing



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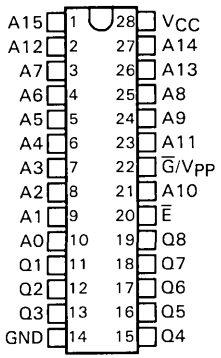
SEPTEMBER 1987 – REVISED DECEMBER 1987

- Organization . . . 64K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 512K EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time
  - '27C512-20 200 ns
  - '27C512-25 250 ns
  - '27C512-30 300 ns
- HVCMOS Technology
- 3-State Output Buffers
- Latchup Immunity of 250 mA on all Input and Output Pins
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation (V_{CC} = 5.5 V)
  - Active . . . 263 mW (MAX)
  - Standby . . . 1.8 mW (MAX) (CMOS Input Levels)
- −55°C to 125°C Operating Temperature Range
- Standard and Class B Processing
  - SM27C512 . . . Standard
  - SMJ27C512 . . . Class B

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A15	Address Inputs
$\overline{E}$	Chip Enable/Power Down
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
$\overline{G}/V_{PP}$	12.5-V Power Supply/ Output Enable

description

The SMJ27C512 series is a 524,288-bit, ultraviolet-light erasable, electrically programmable read-only memory. This device is fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 54 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The SMJ27C512 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation from −55°C to 125°C.

Since this EPROM operates from a single 5-V supply (in the read mode), it is are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation for the SMJ27C512 listed on the following page. Read mode requires a single 5-V supply. All inputs are TTL level except for Vpp during programming (12.5 V) and 12 V on A9 for signature mode.

FUNCTION (PINS)	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}/V_{PP}$ (22)	V_{IL}	V_{IH}	X†	V_{PP}	V_{IL}	V_{PP}	V_{IL}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8 (11-13, 15-19)	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	CODE	
							MFG	DEVICE
							97	85

†X Can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more SMJ27C512s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the SMJ27C512, a low-level signal is applied to the $\overline{E}$ and $\overline{G}/V_{PP}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8.

power down

Active I_{CC} current can be reduced from 50 mA to 500 μA (TTL-level inputs) or 350 μA (CMOS-level inputs) by applying a high logic signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C512 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is 15 watt-seconds-per-square-centimeter. A typical 12 milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C512, the window should be covered with an opaque label.

fast programming

After erasure (all bits in logic 1 state), logic 0s are programmed into the desired locations. A programmed 0 can be erased only by ultraviolet light. Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{E}$ is pulsed. The programming mode is achieved when $\overline{G}/V_{PP}$ = 12.5 V, V_{CC} = 6.0 V, and $\overline{E}$ = V_{IL}. More than one SMJ27C512 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6.0 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = 5 V (see Figure 1).

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program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with $\overline{G}/V_{PP}$ and $\overline{E} = V_{IL}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10); i.e., $A0 = V_{IL}$ accesses the manufacturer code; $A0 = V_{IH}$ accesses the device code. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for this device is 97, and the device code is 85.

latchup immunity

Latchup immunity on the SMJ27C512 is minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001; *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family,"* available through TI Field Sales Offices.

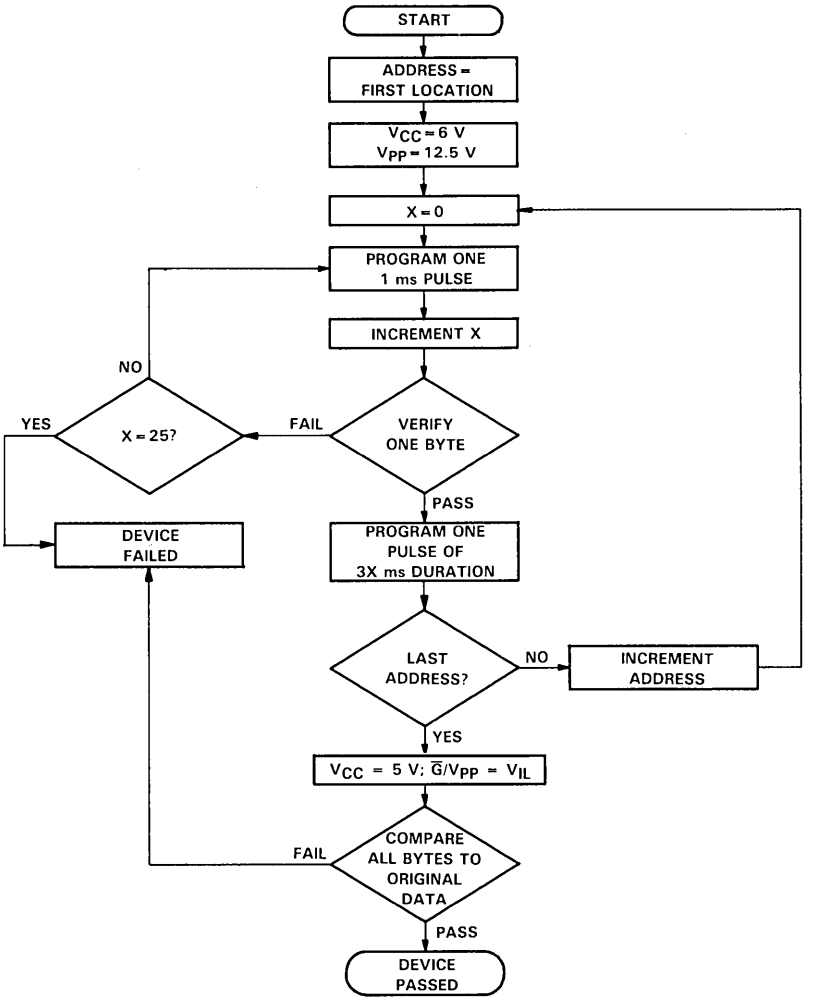

FIGURE 1. FAST PROGRAMMING FLOWCHART

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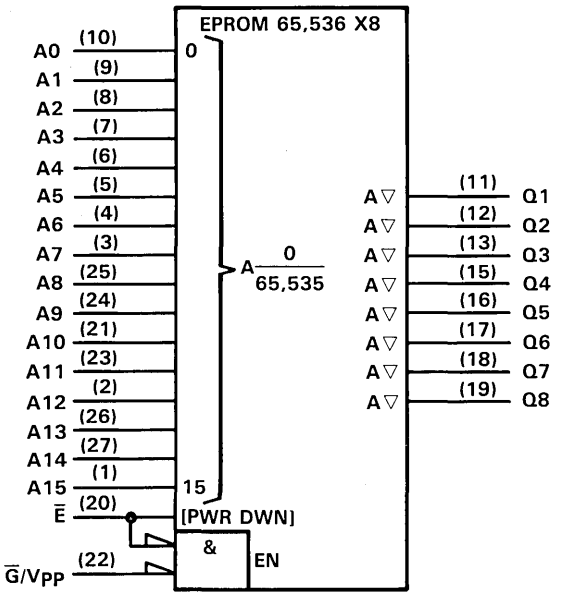
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1)	−0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9	−0.6 to 6.5 V
A9	−0.6 V to 13.5 V
Output voltage range (see Note 1)	−0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature	−55°C
Maximum operating case temperature	125°C
Storage temperature range	−65°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SM/SMJ27C512-25 SM/SMJ27C512-30 SM/SMJ27C512-45			UNIT
		MIN	NOM	MAX	
V_{CC} Supply voltage (see Note 2)		4.5	5	5.5	V
V_{PP} Supply voltage (see Note 3)			V_{CC}		V
V_{IH} High-level input voltage	TTL	2		$V_{CC}+1$	V
	CMOS	$V_{CC}-0.2$		$V_{CC}+0.2$	V
V_{IL} Low-level input voltage	TTL	−0.5		0.8	V
	CMOS	GND − 0.2		GND + 0.2	V
T_A Operating free-air temperature		−55			°C
T_C Operating case temperature				125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 12.5 V (±0.5 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±10	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±10	μA
I_{PP}	V_{PP} supply current (during program pulse)		$\overline{G}/V_{PP}$ = 13 V		35	70	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			350	μA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		35	50	mA

†Typical values are at T_A = 25°C and nominal voltages.

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capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		8	pF
$C_{\overline{G}/V_{PP}}$	$\overline{G}/V_{PP}$ input capacitance	$\overline{G}/V_{PP}$ = 0 V, f = 1 MHz		20	pF

†Typical values are at T_A = 25°C and nominal voltages.

PARAMETER		TEST CONDITIONS (SEE NOTE 4)	'27C512-20		'27C512-25		'27C512-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	See Figure 2		200		250		300	ns
$t_{a(E)}$	Access time from chip enable			200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100		120	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first‡		0	60	0	60	0	105	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first‡		0		0		0		ns

‡Value calculated from 0.5 V delta to measured output level.

NOTE 4: For all switching characteristics and timing measurements input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 (reference page 8, AC testing waveforms).

recommended timing requirements for programming, T_A = 25°C, V_{CC} = 6 V, V_{PP} = 12.5 V (see Note 4)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	2.85		78.75	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
t_{EHD}	Data valid from $\overline{E}$ low			1	μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{r(PG)G}$	V_{PP} rise time	50			ns
$t_{h(VPP)}$	V_{PP} hold time	2			μs
$t_{rec(PG)}$	V_{PP} recovery time	2			μs

NOTE 4: For all switching characteristics and timing measurements input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 (reference below).

PARAMETER MEASUREMENT INFORMATION

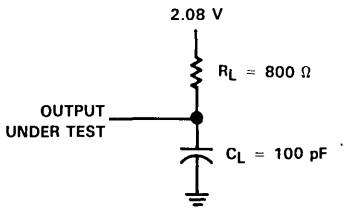
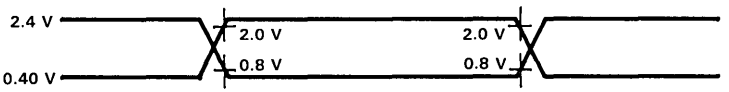


FIGURE 2. OUTPUT LOAD CIRCUIT



AC testing input/output wave forms

A.C. testing inputs are driven at 2.4 V for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0.

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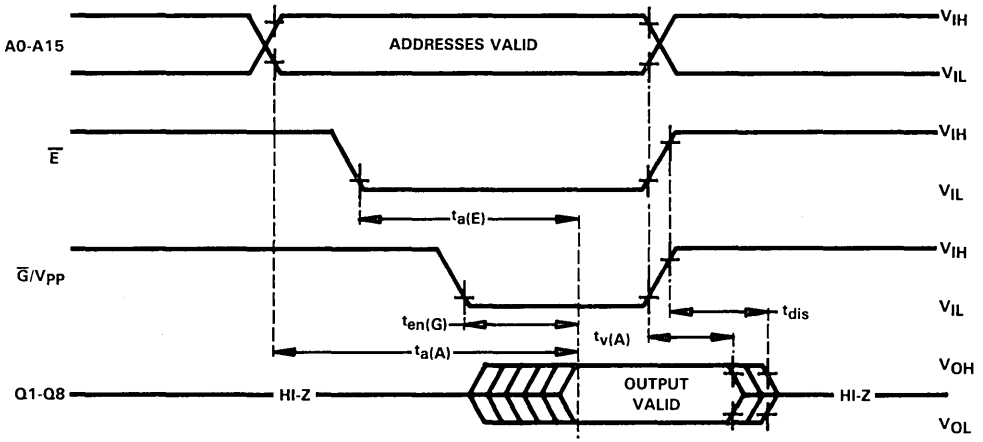
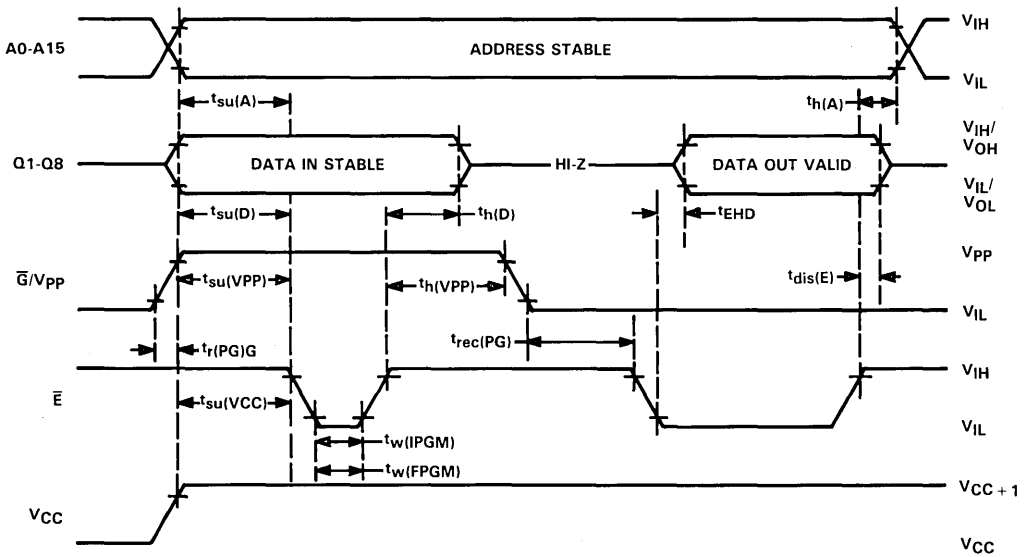
read cycle timing

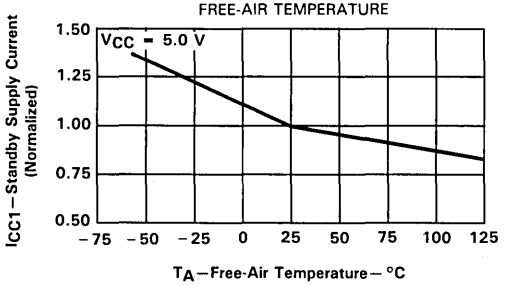


program cycle timing

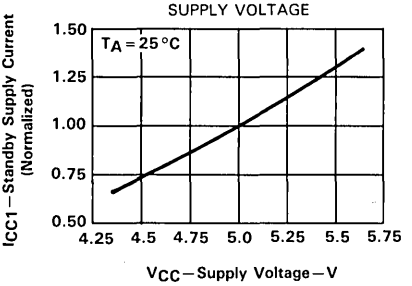


TYPICAL SMJ27C512 CHARACTERISTICS

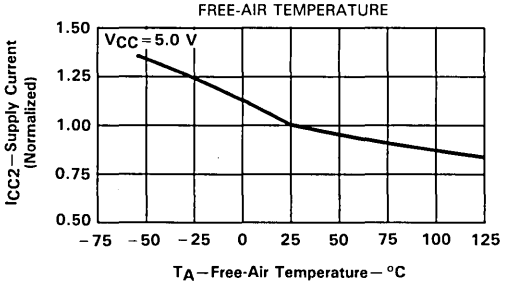
STANDBY SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



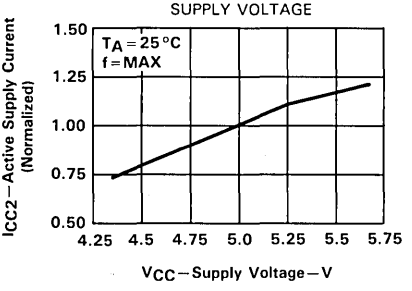
STANDBY SUPPLY CURRENT
vs
SUPPLY VOLTAGE



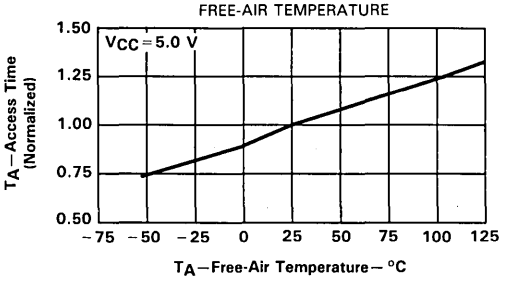
ACTIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



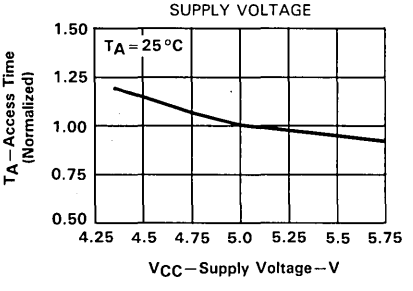
ACTIVE SUPPLY CURRENT
vs
SUPPLY VOLTAGE



ACCESS TIME
vs
FREE-AIR TEMPERATURE



ACCESS TIME
vs
SUPPLY VOLTAGE



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

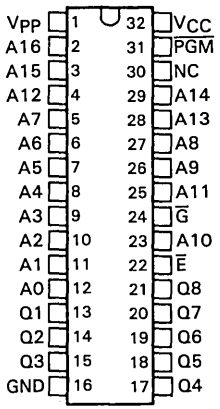
MARCH 1988—REVISED JULY 1988

- Organization . . . 128K × 8
- Single 5-V Power Supply
- Industry Standard 32-Pin Dual-In-line Package
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time

  V_{CC} ± 10%

  SMJ27C010-25 250 ns
  SMJ27C010-30 300 ns
- 8-Bit Output For Use in Microprocessor-Based Systems
- 32-Bit Programming (Four Bytes) and Standard 8-Bit Programming
- Power Saving CMOS Technology
- 3-State Output Buffers
- Uses TI's Innovative ACE (Advanced Contactless EPROM) Technology for Noise Immunity and Improved Reliability
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required
- Low Power Dissipation (V_{CC} = 5.5 V)
  —Active . . . 220 mW Worst Case
  —Standby . . . 1.5 mW Worst Case (CMOS-Input Levels)
- Operating Free-Air Temperature −55°C to 125°C

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A16	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Supply
V_{PP}	12.5-V Power Supply†

†Only in program mode.

description

The SMJ27C010 series are 1,048,576-bit, ultraviolet-light erasable electrically programmable read-only memories. These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits. Each output can drive one Series 54 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The SMJ27C010 is offered in a 600-mil dual-in-line cerdip package (J suffix) rated for operation from −55°C to 125°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing PROM programmers can be used.

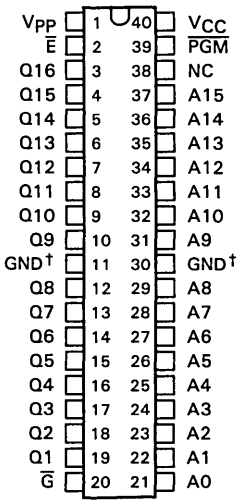
MARCH 1988

- Wide-Word Organization . . . 64K × 16
- Single 5-V Power Supply
- Operationally Compatible with Existing Megabit EPROMs
- 40-Pin Dual-In-line Package
- All Inputs and Outputs Fully TTL Compatible
- Static Operations (No Clocks, No Refresh)
- Max Access/Min Cycle Time

  V_{CC} ± 10%

  SMJ27C210-25 250 ns
  SMJ27C210-30 300 ns
- 16-Bit Output For Use in Microprocessor-Based Systems
- 32-Bit Programming (Two 16-Bit Words) and 16-Bit Programming
- 16 Seconds Typical Programming Time
- Power Saving CMOS Technology
- 3-State Output Buffers
- Uses TI's Innovative ACE (Advanced Contactless EPROM) Technology for Noise Immunity and Improved Reliability
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Latchup Immunity of 250 mA on All Input and Output Pins
- No Pull-Up Resistors Required
- Low Power Dissipation
  —Active . . . 220 mW Worst Case
  —Standby . . . 1.5 mW Worst Case (CMOS-Input Levels)
- Operating Free-Air Temperature −55°C to 125°C

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q16	Outputs
V_{CC}	5-V Supply
V_{PP}	12.5-V Supply‡

†Pins 11 and 30 must be connected externally to ground.
‡Only in program mode.

description

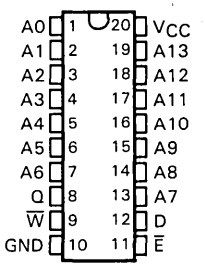
The SMJ27C210 is a 1,048,576-bit, ultraviolet-light erasable, electrically programmable read-only memory. This device is fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The SMJ27C210 is offered in a 600-mil dual-in-line cerdip package (J suffix) rated for operation from −55°C to 125°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

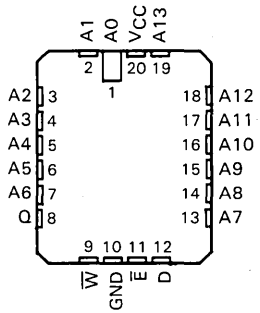
APRIL 1987—REVISED NOVEMBER 1987

- 16,384 × 1 Organization
- Separate I/O
- Military Temperature Range . . . −55°C to 125°C (M Suffix)
- Fast Static Operation
- Battery Back-Up Operation . . . 2 Volt Data Retention
- Maximum Access Time from Address or Chip Enable
  '61CD16-25 . . . 25 ns
  '61CD16-35 . . . 35 ns
  '61CD16-45 . . . 45 ns
- Single 5-V Supply (10% Tolerance)
- JEDEC Standardized Pinout
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- Automatic Powerdown When Deselected
  — 125 μA MAX Standby Current at CMOS Levels
- Low Power Dissipation (V_{CC} = 5.5 V)
  — Active . . . 660 mW MAX
  — Standby . . . 110 mW MAX (TTL Inputs)
  — Standby . . . 0.68 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  — SM Prefix . . . Standard Processing
  — SMJ Prefix . . . Class B Processing
- Three State Output
- Packaging Options:
  — 20-Pin Ceramic 300-mil DIP
  — 20-Pad Leadless Ceramic Chip Carrier

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A13	Address Inputs
D	Data Input
Q	Data Output
$\overline{E}$	Chip Enable/Power Down
GND	Ground
V_{CC}	5-V Supply
$\overline{W}$	Write Enable

description

The '61CD16 is a separate I/O, 16,384-bit static random-access memory organized as 16,384 words by 1 bit. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six transistor cell) memory array. The six transistor cell provides for inherently lower soft error rates, improved stability across the operating temperature range, and extremely low standby power compared to the four transistor/two poly load cell making it ideal for military applications.

The '61CD16's static design and control signals ($\overline{E}$ and $\overline{W}$) remove the need for refresh circuitry and simplify timing requirements. The chip-enable pin allows for easy memory expansion and automatic power-down. Access time from either address or chip enable is a maximum of 25, 35, or 45 ns, allowing speed upgrades for new and existing designs.

operation

addresses (A0-A13)

The 14 address inputs select one of the 16,384 -bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable/power down ($\overline{E}$)

The chip enable/power down terminal, which can be driven directly by standard TTL circuits, affects the data-in and data-out terminals and the internal functioning of the chip itself. Whenever the chip enable/power down is low (enabled), the device is operational, input and output terminals are enabled, and data can be read or written. When the chip enable/power down terminal is high (disabled), the device is deselected and put into a reduced-power standby mode. Data is retained during standby.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{E}$ must be high when changing addresses to prevent inadvertently writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

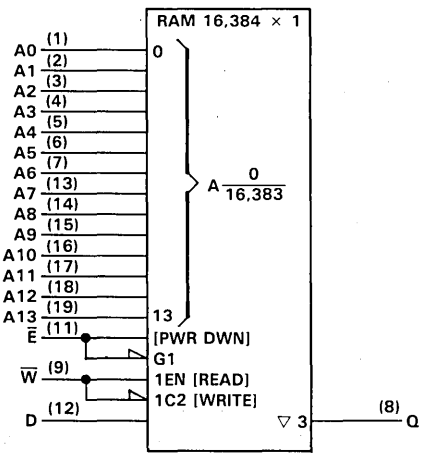
data in (D)

Data can be written into a selected device when the write-enable input is low. The input terminal can be driven directly from standard TTL circuits. Data on the input pin (D) is written into the memory location specified on the address pins (A0-A13).

data out (Q)

The three-state output buffer provides direct TTL compatability with a fanout of two Series 54 TTL gates, one Series 54S TTL gate, or eight Series 54LS TTL gates. The output terminal is in the high-impedance state when chip enable ($\overline{E}$) is high or whevever a write operation is being performed. Data out is the same polarity as data in.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JD package.

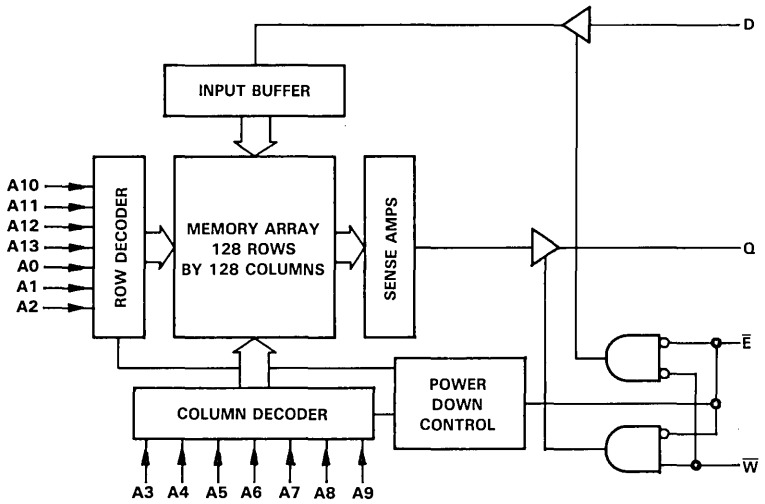
FUNCTION TABLE

INPUTS		OUTPUTS	MODE	POWER
$\overline{E}$	$\overline{W}$	Q		
H	X	HI-Z	Standby	Standby
L	H	Data Output	Read	Active
L	L	HI-Z	Write	Active

X = Don't Care.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range (see Note 2) . . . . . −1 V to 7 V
Output voltage range in high-impedance state . . . . . −0.5 V to 7 V
Output current . . . . . 20 mA
Minimum operating free-air temperature . . . . . −55°C
Maximum operating case-temperature . . . . . 125°C
Storage temperature range . . . . . −65°C to 150°C
Latch-up current . . . . . 200 mA

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to GND.
2. V_{IL} (MIN) of −3 V for short pulse durations of 20 ns or less. Prolonged operation at V_{IL} levels below −1 V will result in excessive currents that may damage the device.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_C	Operating case temperature			125	°C
T_A	Operating free-air temperature	−55			°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	'61CD16-25			'61CD16-35			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	−10		10	μA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−50		50	−50		50	μA
I_{OS}	Short circuit output current (see Note 3)		V_{CC} = 5.5 V, V_O = GND			−350			−350	mA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			120			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}$ ≥ V_{IH}, V_{CC} = 5.5 V			20			20	mA
		CMOS-level inputs	Inputs = V_{CC}±0.3, V_{CC} = 5.5 V			125			125	μA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	'61CD16-45			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	μA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−50		50	μA
I_{OS}	Short circuit output current (see Note 3)		V_{CC} = 5.5 V, V_O = GND			−350	mA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}$ ≥ V_{IH}, V_{CC} = 5.5 V			20	mA
		CMOS-level inputs	Inputs = V_{CC}±0.3, V_{CC} = 5.5 V			125	μA

NOTE 3: Not more than one output should be shorted at a time. The duration of the short circuit should not exceed 30 seconds.

TEXAS INSTRUMENTS
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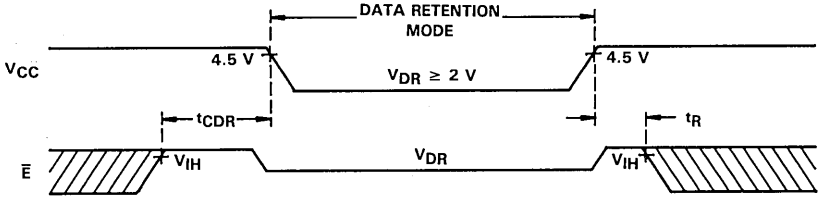
data retention characteristics

PARAMETER		TEST CONDITION	MIN	TYP† V_{CC} @ 2.0 V	TYP† V_{CC} @ 3.0 V	MAX V_{CC} @ 2.0 V	MAX V_{CC} @ 3.0 V	UNIT
V_{DR}	V_{CC} for data retention	$\overline{E} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $\leq$ GND + 0.2 V	2.0		–	–	–	V
I_{CCDR}	Data retention current			3	5	50	75	μA
t_{CDR}	Chip deselect to data retention time		0	–		–		ns
t_R	Operation recovery time		$t_{c(RD)}$‡	–		–		ns
I_{LI}§	Input leakage current			–		1		μA

†TYP values listed are typical values at 25°C.
‡$t_{c(RD)}$ = read cycle time.
§This parameter is guaranteed but not tested.

data retention waveform



capacitance, T_A = 25°C, f = 1 MHz¶

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5 V			4	pF
C_o	Output capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5 V			7	pF

¶Capacitance measurements are made on sample basis only.

timing requirements over recommended supply voltage range and operating temperature range

		'61CD16-25 MIN	'61CD16-25 TYP	'61CD16-25 MAX	'61CD16-35 MIN	'61CD16-35 TYP	'61CD16-35 MAX	UNIT
$t_{c(rd)}$	Read cycle time	25			35			ns
$t_{c(wr)}$	Write cycle time	25			35			ns
$t_{w(W)}$	Write-enable pulse duration	15			20			ns
t_{ELWH}	Chip-enable low to end of write	25			30			ns
$t_{su(A)}$	Address setup time to write start	0			0			ns
$t_{su(D)}$	Data setup time to write end	12			15			ns
$t_{h(A)}$	Address hold from write end	0			0			ns
$t_{h(D)}$	Data hold from write end	0			0			ns
t_{ELIH}	Delay time, chip-enable low to power up§	5			5			ns
t_{EHIL}	Delay time, chip-enable high to power down§			35			35	ns
t_{AVWH}	Address setup to write end	25			30			ns

§This parameter is guaranteed but not tested.

timing requirements over recommended supply voltage range and operating temperature range

		'61CD16-45			UNIT
		MIN	TYP	MAX	
$t_{c(rd)}$	Read cycle time	45			ns
$t_{c(wr)}$	Write cycle time	45			ns
$t_{w(W)}$	Write-enable pulse duration	20			ns
t_{ELWH}	Chip-enable low to end of write	40			ns
$t_{su(A)}$	Address setup time to write start	0			ns
$t_{su(D)}$	Data setup time to write end	15			ns
$t_{h(A)}$	Address hold from write end	0			ns
$t_{h(D)}$	Data hold from write end	0			ns
t_{ELIH}	Delay time, chip-enable low to power up†	5			ns
t_{EHIL}	Delay time, chip-enable high to power down†			35	ns
t_{AVWH}	Address setup to write end	40			ns

†This parameter is guaranteed but not tested.

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS	'61CD16-25			'61CD16-35			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{a(A)}$	Access time from address	I_{OH} = −4 mA, I_{OL} = 8 mA			25			35	ns
$t_{a(E)}$	Access time from chip enable low	C_L = 30 pF,			25			35	ns
$t_{v(A)}$	Output data valid after address change	See Figure 1a.	0	3		0	3		ns
$t_{en(W)}$	Output enable time from write enable high‡		0		15	0		20	ns
$t_{en(E)}$	Output enable time from chip enable low‡	R1 = 481 Ω, R2 = 255 Ω,	5			5			ns
$t_{dis(E)}$	Output disable time from chip enable high‡	C_L = 5 pF, See Figure 1b.			10			15	ns
$t_{dis(W)}$	Output disable time from write enable low‡				10			15	ns

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS	'61CD16-45			UNIT
			MIN	TYP	MAX	
$t_{a(A)}$	Access time from address	I_{OH} = −4 mA, I_{OL} = 8 mA			45	ns
$t_{a(E)}$	Access time from chip enable low	C_L = 30 pF,			45	ns
$t_{v(A)}$	Output data valid after address change	See Figure 1a.	0	3		ns
$t_{en(W)}$	Output enable time from write enable high‡		0		20	ns
$t_{en(E)}$	Output enable time from chip enable low‡	R1 = 481 Ω, R2 = 255 Ω,	5			ns
$t_{dis(E)}$	Output disable time from chip enable high‡	C_L = 5 pF, See Figure 1b.			20	ns
$t_{dis(W)}$	Output disable time from write enable low‡				20	ns

‡Transition is measured ±500 mV from steady state voltage; this parameter is guaranteed but not tested.

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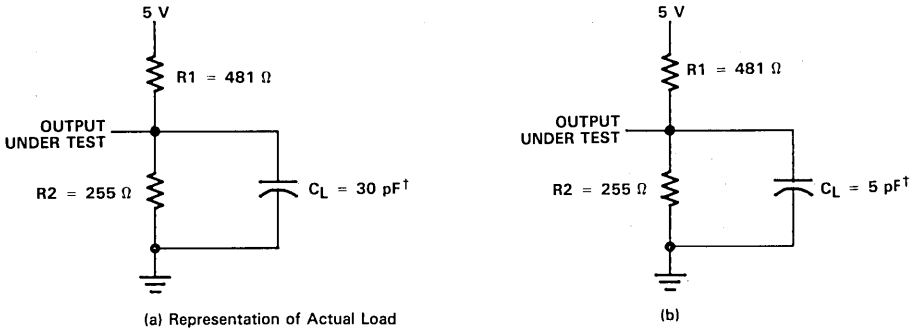
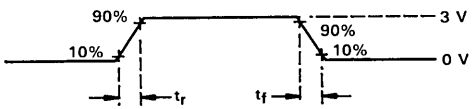
PARAMETER MEASUREMENT INFORMATION



†C_L includes jig and scope capacitances.

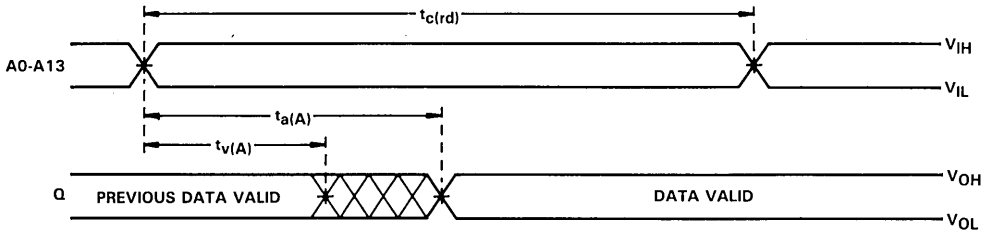
FIGURE 1. OUTPUT LOAD CIRCUIT



NOTE 4: t_r and $t_f \leq 5$ ns.

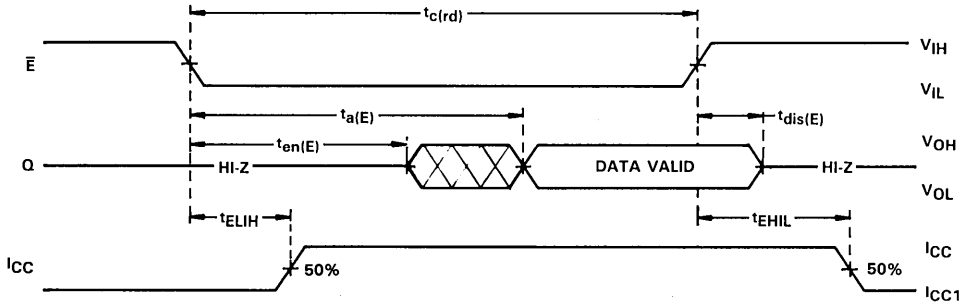
FIGURE 2. TRANSITION TIMES

read cycle timing from address†



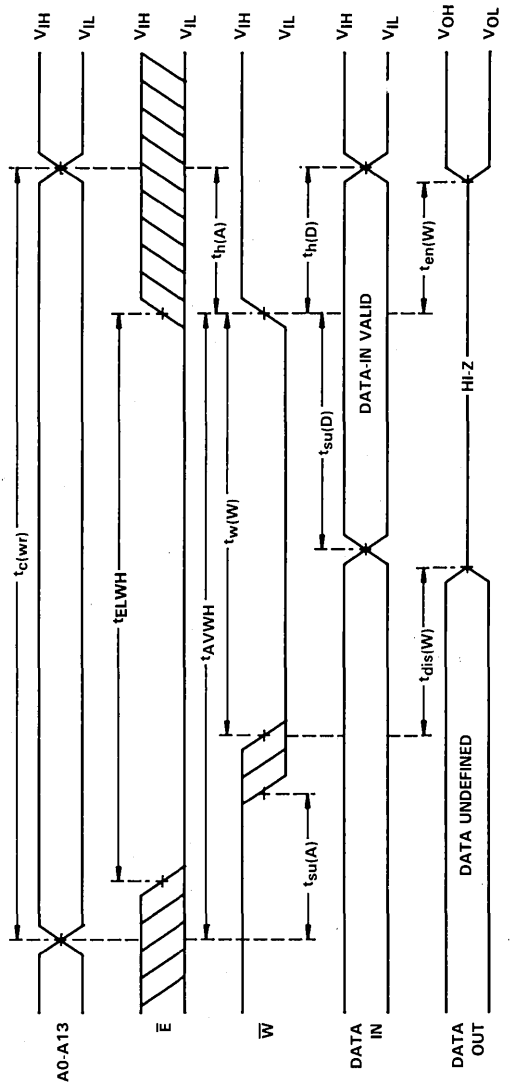
†$\overline{W}$ is high, and $\overline{E}$ is low.

read cycle timing from chip enable‡



‡$\overline{W}$ is high, address is valid prior to or simultaneously with the high-to-low transition of $\overline{E}$.

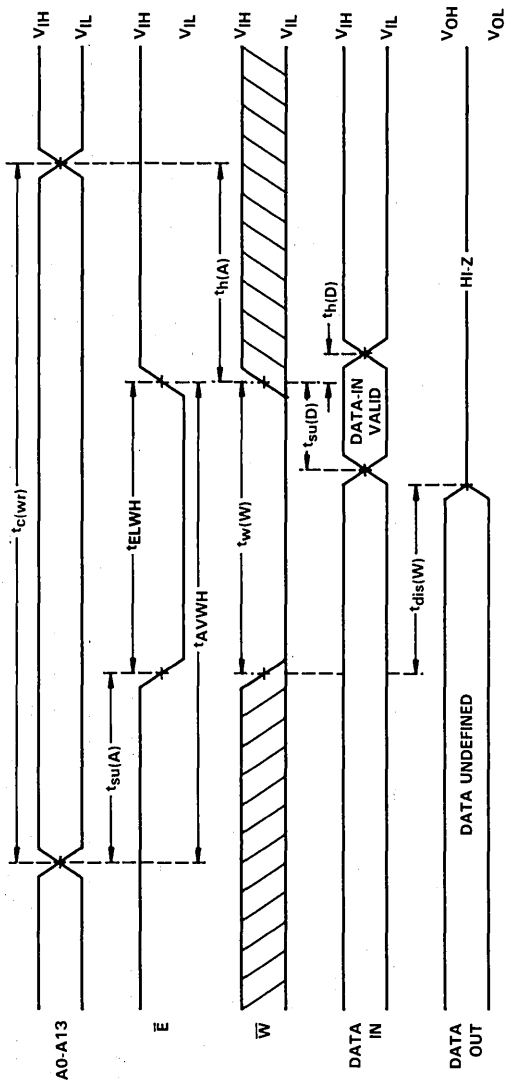
write cycle timing controlled by write enable†



†$\overline{E}$ or $\overline{W}$ must be high during address transitions.

NOTE: For both $\overline{W}$-controlled and $\overline{E}$-controlled Write operations, the internal write time of the memory is defined by the overlap of $\overline{E}$ low and $\overline{W}$ low. Both signals must be low to initiate a write, and either signal can terminate a write by going high. The data input setup and hold times should be referenced to the edge that terminates the write.

write cycle timing controlled by chip enable†



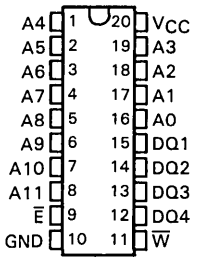
†E or W must be high during address transitions.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

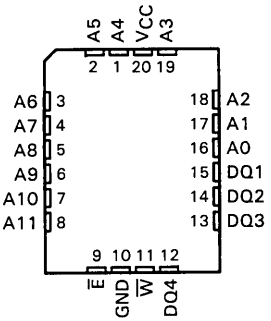
MARCH 1987—REVISED NOVEMBER 1987

- 4096 × 4 Organization
- Common I/O
- Military Temperature Range . . . −55°C to 125°C (M Suffix)
- Fast Static Operation
- Battery Back-Up Operation . . . 2-Volt Data Retention
- Maximum Access Time from Address or Chip Enable
  '64C16-25 . . . 25 ns
  '64C16-35 . . . 35 ns
  '64C16-45 . . . 45 ns
- Single 5-V Supply (10% Tolerance)
- JEDEC Standarized Pinout
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- Automatic Power Down when Deselected
  — 125 μA MAX Standby Current at CMOS Levels
- Low Power Dissipation (V_{CC} = 5.5 V)
  — Active . . . 660 mW
  — Standby . . . 55 mW MAX (TTL Levels)
  — Standby . . . 0.68 mW MAX (CMOS Levels)
- Standard and Class B Processing
  — SM Prefix . . . Standard Processing
  — SMJ Prefix . . . Class B Processing
- Packaging Options:
  — 20-Pin Ceramic 300-mil DIP
  — 20-Pad Leadless Ceramic Chip Carrier

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A11	Addresses
DQ1-DQ4	Data In/Data Out
Ē	Chip Enable/Power Down
GND	Ground
V_{CC}	5-V Supply
W̄	Write Enable

Description

The '64C16 is a common I/O, 16,384-bit static random-access memory organized as 4096 words by 4 bits. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six-transistor cell) memory array. The six-transistor cell provides for inherently lower soft error rates, improved stability across the operating temperature range, and extremely low standby power compared to the four-transistor/two-poly load cell, making it ideal for military applications.

The '64C16's static design and control signals (Ē and W̄) remove the need for refresh circuitry and simplify timing requirements. The chip enable pin provides for easy memory expansion and for an automatic powerdown feature. Access time from either address or chip enable is a maximum of 25, 35, or 45 ns.

operation

addresses (A0-A11)

The 12 address inputs select one of the 4096 4-bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable/power down ($\overline{E}$)

The chip enable/power down terminal, which can be driven directly by standard TTL circuits, affects the data-in and data-out terminals and the internal functioning of the chip itself. Whenever the chip enable/power down is low (enabled), the device is operational, input and output terminals are enabled, and data can be read or written. When the chip enable/power down terminal is high (disabled), the device is deselected and put into a reduced-power standby mode. Data is retained during standby.

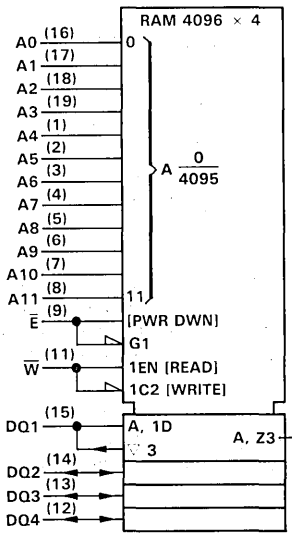
write enable ($\overline{W}$)

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{E}$ must be high when changing addresses to prevent erroneously writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

data in/data out (DQ1-DQ4)

Data can be written into a selected device when the write-enable input is low. The DQ terminals can be driven directly from standard TTL circuits. The three-state output buffer provides direct TTL compatibility with a fanout of two Series 54 TTL gates, one Series 54S TTL gate, or eight Series 54LS TTL gates. The DQ terminals are in the high-impedance state when chip enable ($\overline{E}$) is high or whenever a write operation is being performed. Data out is the same polarity as data in.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JD package.

FUNCTION TABLE

INPUTS		OUTPUTS	MODE	POWER
$\overline{E}$	$\overline{W}$	DQ1-DQ4		
H	X	HI-Z	Standby	Standby
L	H	Data Output	Read	Active
L	L	HI-Z	Write	Active

X = Don't Care.

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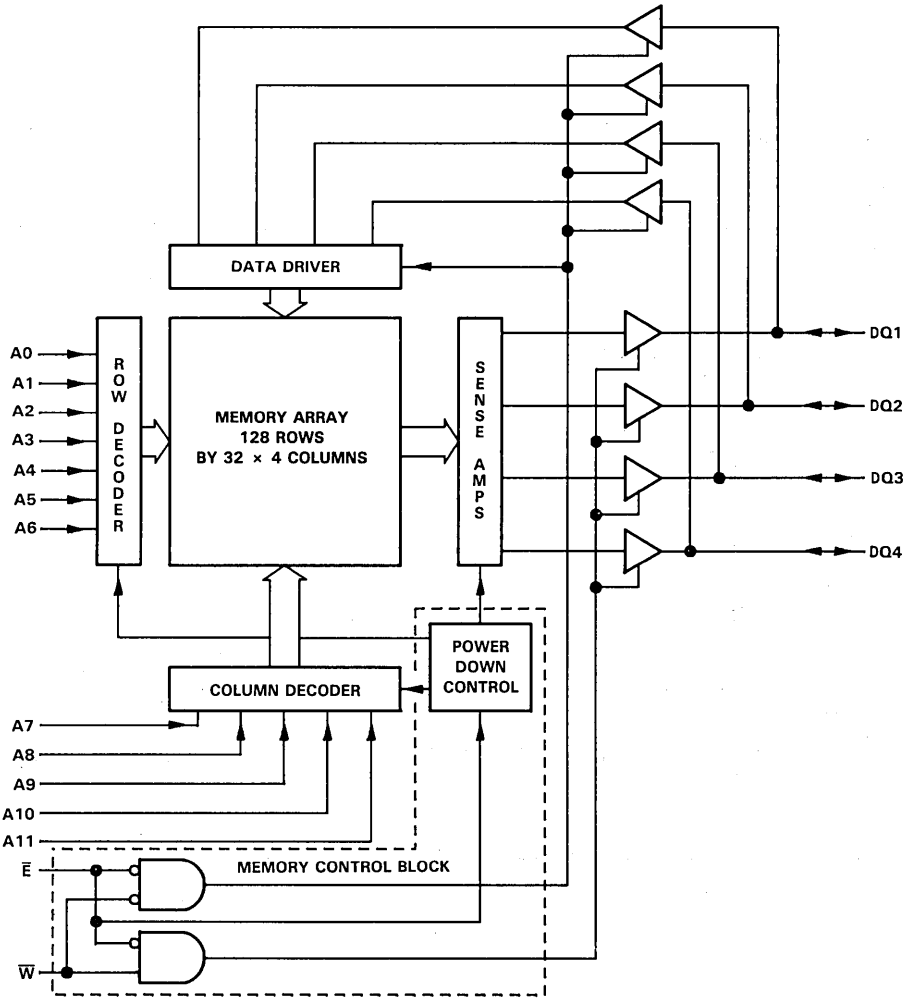
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range (see Note 2) . . . . . −1 V to 7 V
Output voltage range in high-impedance state . . . . . −0.5 V to 7 V
Output current . . . . . 20 mA
Minimum operating free-air temperature . . . . . −55°C
Maximum operating case-temperature . . . . . 125°C
Storage temperature range . . . . . −65°C to 150°C
Latch-up current . . . . . 200 mA

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to GND.
2. V_{IL} (min) of −3 V for short pulse durations. Prolonged operation at V_{IL} levels below −1 V will result in excessive currents that may damage the part.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_C	Operating case temperature			125	°C
T_A	Operating free-air temperature	−55			°C

NOTE 2: V_{IL} (min) of −3 for short pulse durations. Prolonged operation at V_{IL} levels below −1 V will result in excessive currents that may damage the part.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	'64C16-25			'64C16-35			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	−10		10	μA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−50		50	−50		50	μA
I_{OS}	Short circuit output current (see Note 3)		V_{CC} = 5.5 V, V_O = GND			−350			−350	mA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			120			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}$ ≥ V_{IH}, V_{CC} = 5.5 V			20			20	mA
		CMOS-level inputs	Inputs = V_{CC} ± 0.3, V_{CC} = 5.5 V			125			125	μA

NOTE 3: Not more than one output should be shorted at a time. The duration of the short circuit should not exceed 30 seconds.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	'64C16-45 MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	μA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−50		50	μA
I_{OS}	Short circuit output current (see Note 3)		V_{CC} = 5.5 V, V_O = GND			−350	mA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}$ ≥ V_{IH}, V_{CC} = 5.5 V			20	mA
		CMOS-level inputs	Inputs = V_{CC} ±0.3, V_{CC} = 5.5 V			125	μA

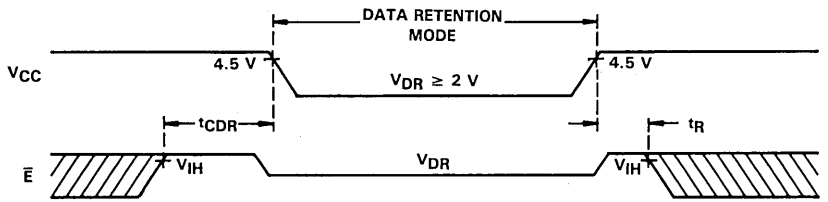
NOTE 3: Not more than one output should be shorted at a time. The duration of the short circuit should not exceed 30 seconds.

data retention characteristics

PARAMETER		TEST CONDITION	MIN	TYP† V_{CC} @ 2.0 V	TYP† V_{CC} @ 3.0 V	MAX V_{CC} @ 2.0 V	MAX V_{CC} @ 3.0 V	UNIT
V_{DR}	V_{CC} for data retention	$\overline{E}$ ≥ V_{CC} − 0.3 V, V_{IN} ≥ V_{CC} − 0.3 V or ≤ GND + 0.3 V	2.0	—	—	—	—	V
I_{CCDR}	Data retention current			3	5	50	75	μA
t_{CDR}	Chip deselect to data retention time		0	—		—		ns
t_R	Operation recovery time		$t_{c(RD)}$‡	—		—		ns
I_{LI}§	Input leakage current			—		1		μA

†TYP values listed are typical values at 25°C.
‡$t_{c(RD)}$ = read cycle time.
§This parameter is guaranteed but not tested.

data retention waveform



capacitance, T_A = 25°C, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5 V			4	pF
C_o	Output capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5 V			7	pF

†Capacitance measurements are made on sample basis only.

timing requirements over recommended supply voltage range and operating temperature range

		'64C16-25			'64C16-35			'64C16-45			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(rd)}$	Read cycle time	25			35			45			ns
$t_{c(wr)}$	Write cycle time	25			35			45			ns
$t_{w(W)}$	Write-enable pulse duration	20			30			35			ns
$t_{su(W)rd}$	Write enable high to chip enable low (read command setup)	0			0			0			ns
t_{ELWH}	Chip-enable low to end of write	25			30			35			ns
$t_{su(A)}$	Address setup time to write start	0			0			0			ns
$t_{su(D)}$	Data setup time to write end	10			15			15			ns
$t_{h(W)rd}$	Write enable low from chip enable high (read command hold)	0			0			0			ns
$t_{h(A)}$	Address hold time from write end	0			0			0			ns
$t_{h(D)}$	Data hold time from write end	0			0			3			ns
t_{ELIH}	Delay time, chip-enable low to power up‡	5			5			5			ns
t_{EHIL}	Delay time, chip-enable high to power down‡			35			35			35	ns
t_{AVWH}	Address setup to write end	20			30			35			ns

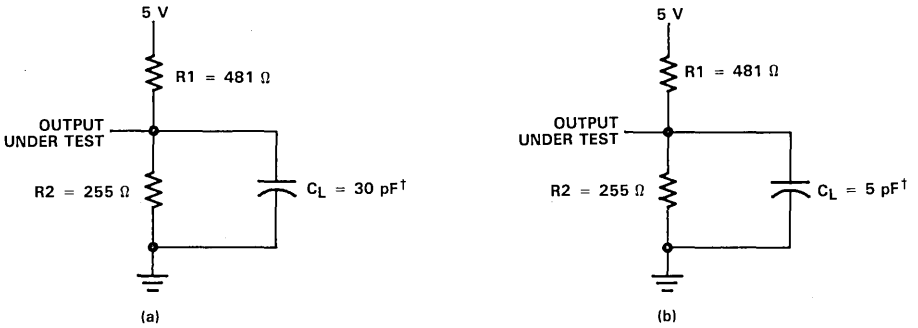
‡This parameter is guaranteed but not tested.

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS	'64C16-25		'64C16-35		'64C16-45		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	R1 = 481 Ω, R2 = 255 Ω, C_L = 30 pF, See Figure 1a.		25		35		45	ns
$t_{a(E)}$	Access time from chip enable low			25		35		45	ns
$t_{v(A)}$	Output data valid after address change		0		0		0		ns
$t_{en(W)}$	Output enable time from write enable high†		6		6		6		ns
$t_{en(E)}$	Output enable time from chip enable low	R1 = 481 Ω, R2 = 255 Ω, C_L = 5 pF, See Figure 1b.	5		5		5		ns
$t_{dis(E)}$	Output disable time from chip enable high‡			15		20		25	ns
$t_{dis(W)}$	Output disable time from write enable low‡			10		15		20	ns

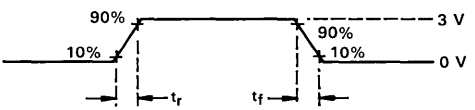
†Transition is measured ±500 mV from steady state voltage. This parameter is guaranteed but not tested.
‡This parameter is guaranteed but not tested.

PARAMETER MEASUREMENT INFORMATION



†C_L includes jig and scope capacitances.

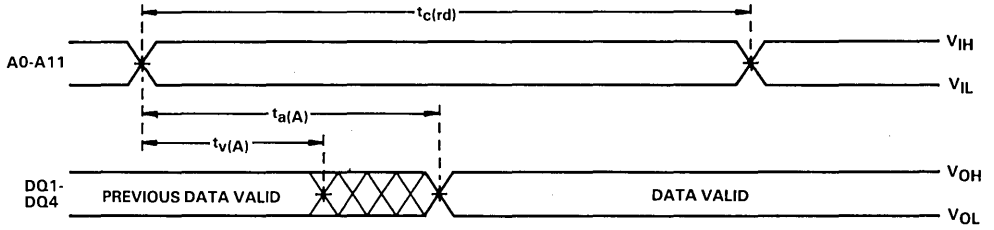
FIGURE 1. OUTPUT LOAD CIRCUIT



NOTE 4: t_r and $t_f \leq 5$ ns.

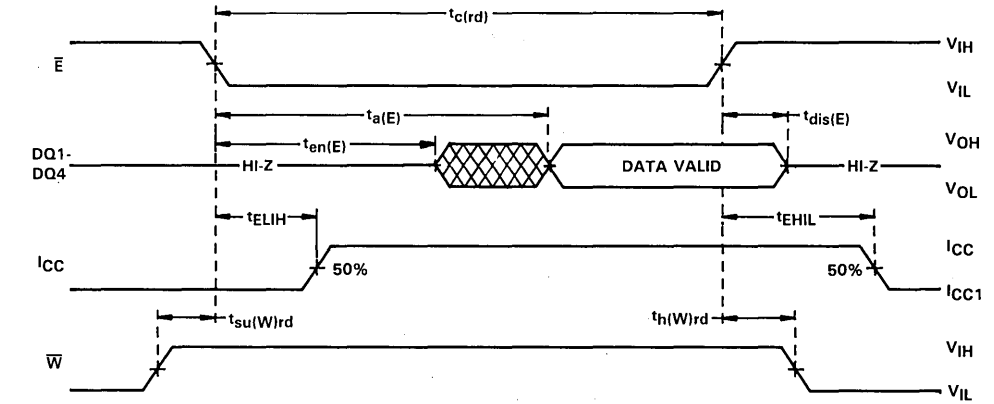
FIGURE 2. TRANSITION TIMES

read cycle timing from address†



†$\overline{W}$ is high, and $\overline{E}$ is low.

read cycle timing from chip enable‡



‡$\overline{W}$ is high, address is valid prior to or simultaneously with the high-to-low transition of $\overline{E}$.

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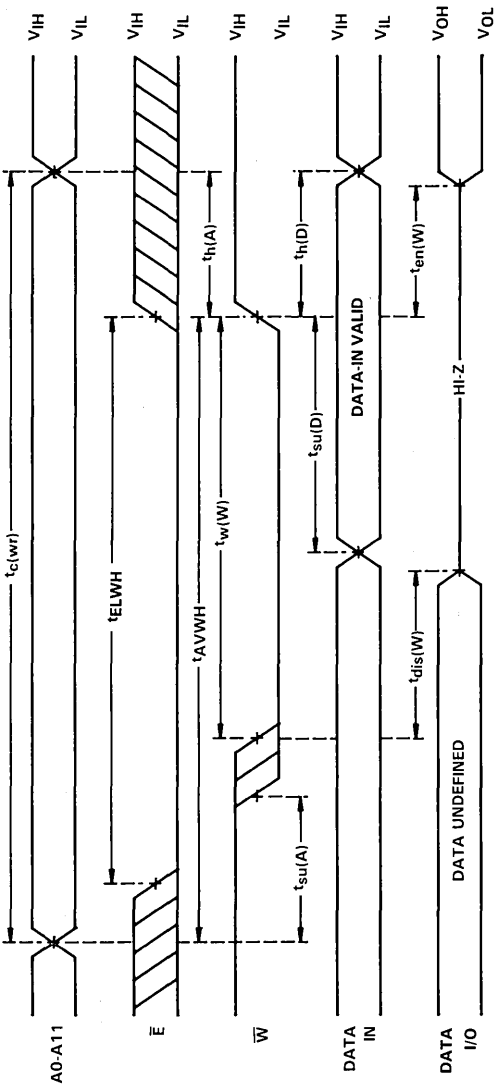
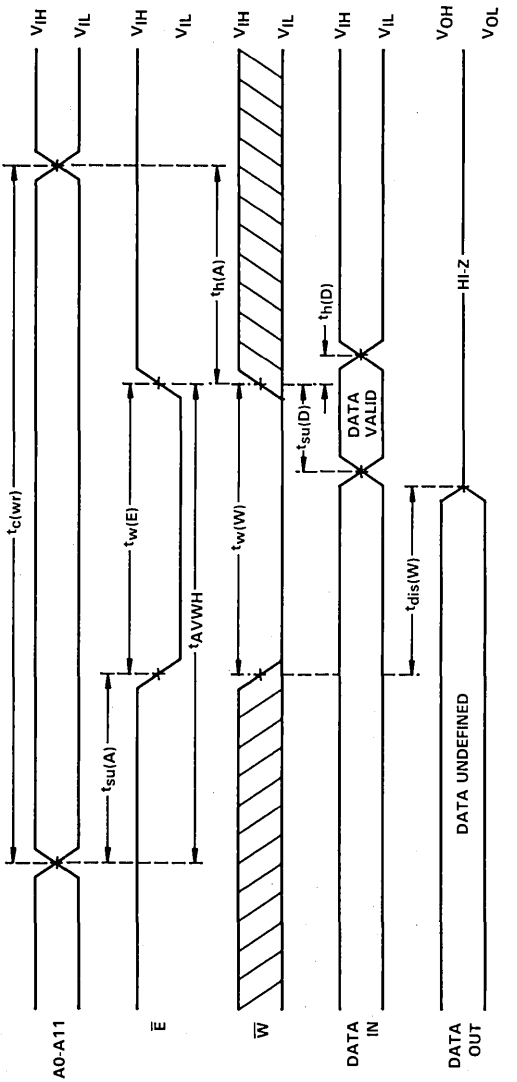
write cycle timing controlled by write enable†



†Ē or W̄ must be high during address transitions.

NOTE: For both WE-controlled and CE-controlled write operations, the internal write time of the memory is defined by the overlap of Ē low and W̄ high. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold times should be referenced to the edge which terminates the write.

write cycle timing controlled by chip enable†



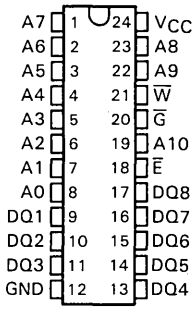
†Ē or W̄ must be high during address transitions.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

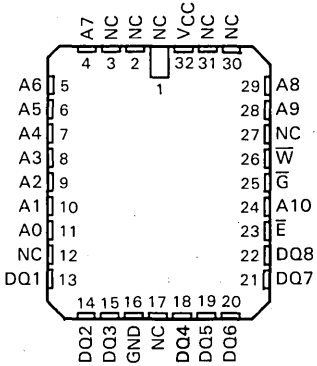
APRIL 1987—REVISED APRIL 1988

- 2048 × 8 Organization
- Common I/O
- Military Temperature Range . . . −55°C to 125°C (M Suffix)
- Fast Static Operation
- Battery Back-Up Operation . . . 2-Volt Data Retention
- Maximum Access Time from Address or Chip Enable
  '68CE16-25 . . . 25 ns
  '68CE16-35 . . . 35 ns
  '68CE16-45 . . . 45 ns
- Single 5-V Supply (10% Tolerance)
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- Automatic Powerdown When Deselected
- TTL Compatible Inputs and Outputs
- 3-State Output
- Low Power Dissipation (V_{CC} = 5.5 V)
  — Active . . . 660 mW MAX
  — Standby . . . 110 mW MAX (TTL Inputs)
  — Standby . . . 5.5 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  — SM Prefix . . . Standard Processing
  — SMJ Prefix . . . Class B Processing
- Output Enable for Bus Control
- Packaging Options:
  — 24-Pin Ceramic 300-mil DIP
  — 32-Pad Leadless Ceramic Chip Carrier

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A10	Address Inputs
DQ1-DQ8	Data Input/Data Out
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
V_{CC}	5-V Supply
$\overline{W}$	Write Enable

description

The '68CE16 is a common I/O, 16,384-bit static random-access memory organized as 2048 words by 8 bits. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six transistor cell) memory array.

The '68CE16's static design and control signals ($\overline{E}$, $\overline{G}$, and $\overline{W}$) remove the need for refresh circuitry and simplify timing requirements. The chip-enable pin allows for easy memory expansion and automatic power-down. This feature, in conjunction with the full CMOS array, allows for low standby power operation when the memory is deselected, greatly reducing the overall memory power requirements. The output-enable pin minimizes bus contention problems and adds flexibility.

Access time from either address or chip enable is a maximum of 25, 35, or 45 ns, allowing speed upgrades for new and existing designs.

operation

addresses (A0-A10)

The 11 address inputs select one of the 2048 8-bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable/power down ($\overline{E}$)

The chip enable/power down terminal, which can be driven directly by standard TTL circuits, affects the data-in and data-out terminals and the internal functioning of the chip itself. Whenever the chip enable/power down is low (enabled), the device is operational, input and output terminals are enabled, and data can be read or written. When the chip enable/power down terminal is high (disabled), the device is deselected and put into a reduced-power standby mode. Data is retained during standby.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{E}$ must be high when changing addresses to prevent inadvertently writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

output enable ($\overline{G}$)

The output-enable terminal affects only the data-out terminals. When output enable is at a logic high level, the output terminals are disabled to the high-impedance state. Output enable provides greater output control flexibility, simplifying data bus design.

data in/data out (DQ1-DQ8)

Data can be written into a selected device when the write-enable input is low. The DQ terminals can be driven directly from standard TTL circuits. The three-state output buffer provides direct TTL compatibility with a fanout of twenty Series 54LS or 54ALS TTL gates, sixteen Series 54AS TTL gates, or thirteen Series 54F TTL gates. The DQ terminals are in the high-impedance state when chip enable ($\overline{E}$) is high or whenever a write operation is being performed. Data out is the same polarity as data in.

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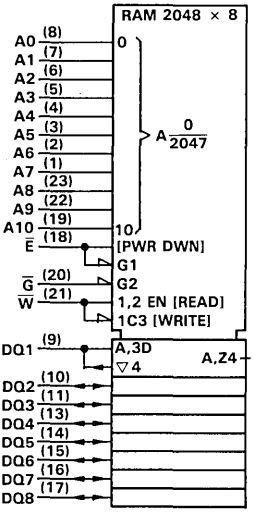
logic symbol†



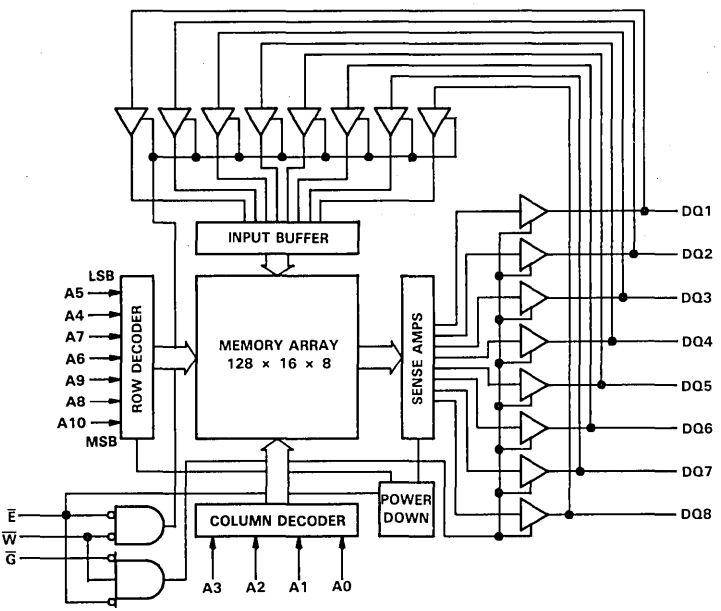
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JD package.

FUNCTION TABLE

INPUTS			OUTPUTS	MODE	POWER
Ē	W̅	G̅	DQ1-DQ8		
H	X	X	HI-Z	Standby	Standby
L	H	L	Data Output	Read	Active
L	H	H	HI-Z	Read	Active
L	L	X	Data Input	Write	Active

X = Don't Care.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range (see Note 2) . . . . . −1 V to 7 V
Output voltage range in high-impedance state . . . . . −0.5 V to 7 V
Output current . . . . . 20 mA
Minimum operating free-air temperature . . . . . −55°C
Maximum operating case-temperature . . . . . 125°C
Storage temperature range . . . . . −65°C to 150°C
Latch-up current . . . . . 200 mA

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to GND.
2. V_{IL} (min) of −3 V for short pulse durations. Prolonged operation at V_{IL} levels below −1 V will result in excessive currents that may damage the device.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_C	Operating case temperature			125	°C
T_A	Operating free-air temperature	−55			°C

NOTE 2: V_{IL} (min) of −3 V for short pulse durations. Prolonged operation at V_{IL} levels below −1 V will result in excessive currents that may damage the device.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	'68CE16-25			'68CE16-35			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	−10		10	μA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−10		10	−10		10	μA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			120			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E} \geq V_{IH}$, V_{CC} = 5.5 V			20			20	mA
		CMOS-level inputs	$\overline{E} = V_{CC}\pm0.3$, V_{CC} = 5.5 V			0.9			0.9	mA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

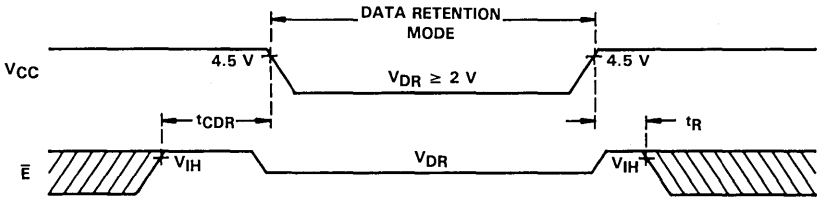
PARAMETER			TEST CONDITIONS	'68CE16-45 MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	μA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−10		10	μA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}$ ≥ V_{IH}, V_{CC} = 5.5 V			20	mA
		CMOS-level inputs	$\overline{E}$ = V_{CC} ± 0.3, V_{CC} = 5.5 V			0.9	mA

data retention characteristics

PARAMETER		TEST CONDITION	MIN	TYP† V_{CC} @ 2.0 V	TYP† V_{CC} @ 3.0 V	MAX V_{CC} @ 2.0 V	MAX V_{CC} @ 3.0 V	UNIT
V_{DR}	V_{CC} for data retention	$\overline{E}$ ≥ V_{CC} − 0.2 V, V_{IN} ≥ V_{CC} − 0.2 V or ≤ GND + 0.2 V	2.0	—	—	—	—	V
I_{CCDR}	Data retention current			3	5	100	200	μA
t_{CDR}§	Chip deselect to data retention time		0	—		—		ns
t_R§	Operation recovery time		$t_{c(RD)}$‡	—		—		ns
I_{LI}§	Input leakage current			—		1		μA

†TYP values listed are typical values at 25°C.
‡$t_{c(RD)}$ = read cycle time.
§This parameter is guaranteed but not tested.

data retention waveform



capacitance, T_A = 25°C, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5 V			5	pF
C_o	Output capacitance				7	pF

†Capacitance measurements are made on sample basis only.

timing requirements over recommended supply voltage range and operating temperature range

		'68CE16-25			'68CE16-35			'68CE16-45			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(rd)}$	Read cycle time	25			35			45			ns
$t_{c(wr)}$	Write cycle time	25			35			45			ns
$t_{w(W)}$	Write-enable pulse duration	20			30			30			ns
$t_{su(E)}$	Chip-enable low to end of write	20			30			40			ns
$t_{su(A)}$	Address setup time to write start	0			0			0			ns
$t_{su(D)}$	Data setup time to write end	10			15			20			ns
$t_{h(A)}$	Address hold time from write end	0			0			0			ns
$t_{h(D)}$	Data hold time from write end	0			0			0			ns
t_{PU}	Delay time, chip-enable low to power up‡	5			5			5			ns
t_{PD}	Delay time, chip-enable high to power down‡			35			35			35	ns
t_{AW}	Address setup to write end	20			30			40			ns

‡This parameter is guaranteed but not tested.

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS	'68CE16-25	'68CE16-35	'68CE16-45	UNIT
			MIN MAX	MIN MAX	MIN MAX	
$t_{a(A)}$	Access time from address	R1 = 481 Ω, R2 = 255 Ω, C_L = 30 pf, See Figure 1a	25	35	45	ns
$t_{a(E)}$	Access time from chip enable low		25	35	45	ns
$t_{a(G)}$	Output enable low to data valid		15	20	25	ns
$t_{v(A)}$	Output data valid after address change		0	0	0	ns
$t_{en(W)}$	Output enable time from write enable high§	R1 = 481 Ω, R2 = 255 Ω, C_L = 5 pF, See Figure 1b	0	0	0	ns
$t_{en(E)}$	Output enable time from chip enable low§		5	5	5	ns
$t_{en(G)}$	Output enable time from output enable ($\overline{G}$) low§		0	0	0	ns
$t_{dis(E)}$	Output disable time from chip enable high§		15	20	20	ns
$t_{dis(W)}$	Output disable time from write enable low§		10	15	20	ns
$t_{dis(G)}$	Output disable time from output enable ($\overline{G}$) high§		12	15	15	ns

§Transition is measured ±500 mV from steady state voltage. This parameter is guaranteed but not tested.

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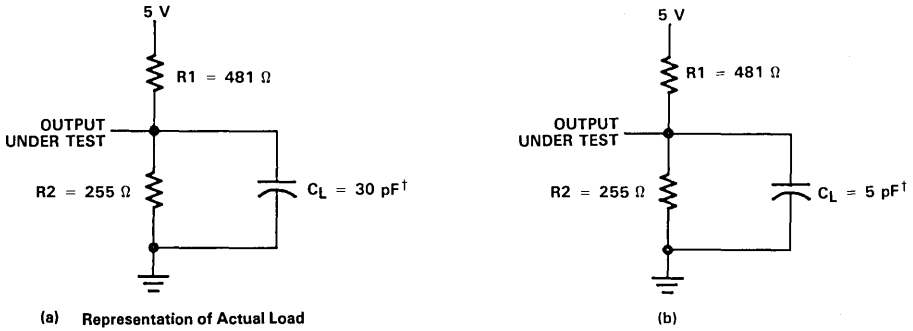
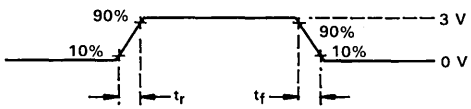
PARAMETER MEASUREMENT INFORMATION



†C_L includes jig and scope capacitances.

FIGURE 1. OUTPUT LOAD CIRCUIT

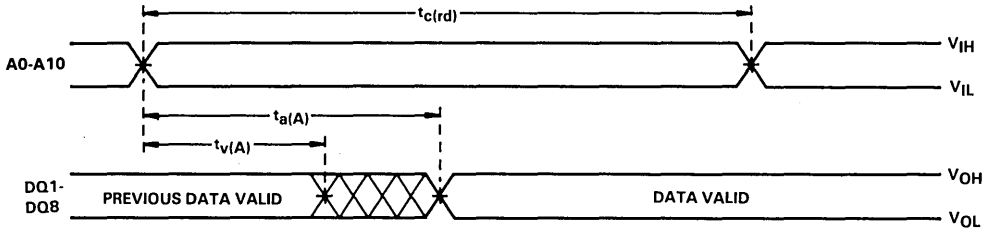


NOTE 4: t_r and $t_f \leq 5$ ns.

FIGURE 2. TRANSITION TIMES

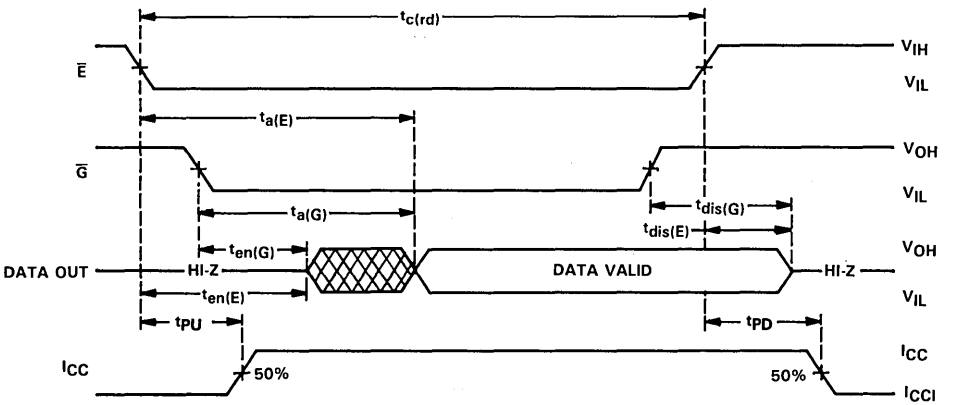
NOTE: All switching characteristics and timing requirements assume test conditions as depicted in Figures 1 and 2 with timing references of 1.5 V (50% reference point) as shown in the subsequent timing diagrams.

read cycle timing from address†



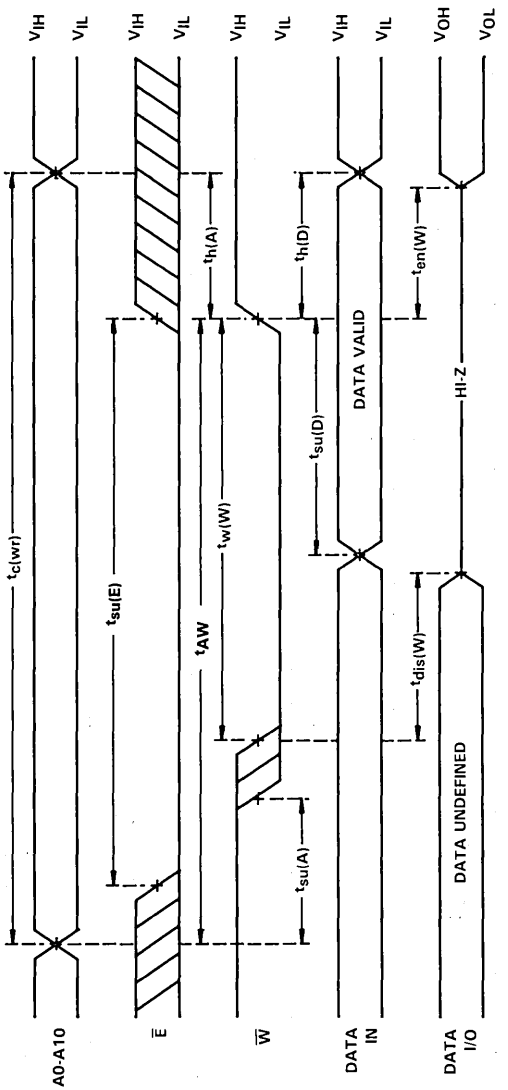
†When $\overline{W}$ is high, $\overline{E}$ is low, and $\overline{G}$ is low, device is continuously selected.

read cycle timing from chip enable‡



‡When $\overline{W}$ is high, address is valid prior to or simultaneously with the high-to-low transition of $\overline{E}$.

rite cycle timing controlled by write enable†

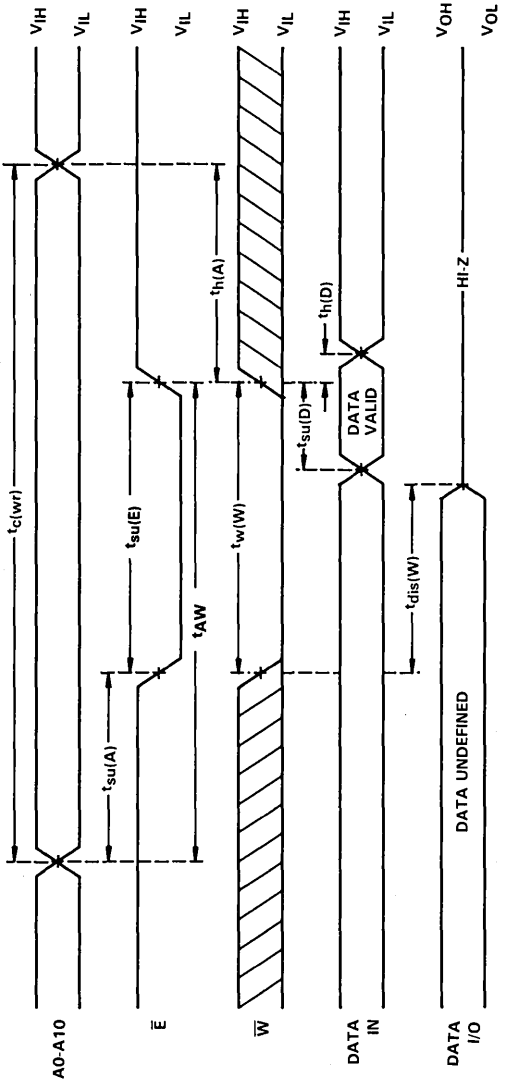


†$\overline{E}$ or $\overline{W}$ must be high during address transitions.

NOTES: 4. The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write, and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

5. Data I/O pins enter high-impedance state, as shown when $\overline{G}$ is held low during write.

write cycle timing controlled by chip enable†

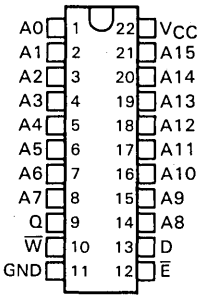


†Ē or W̄ must be high during address transitions.
NOTE 5: Data I/O pins enter high-impedance state, as shown when Ḡ is held low during write.

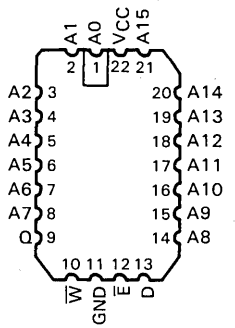
JULY 1987—REVISED APRIL 1988

- 65,536 × 1 Organization
- Separate I/O
- Military Temperature Range . . . −55°C to 125°C (M Suffix)
- Fast Static Operation
- Maximum Access Time from Address or Chip Enable
  '61CD64-25 . . . 25 ns
  '61CD64-35 . . . 35 ns
  '61CD64-45 . . . 45 ns
- Battery Backup Operation . . . 2 Volt Data Retention
- Single 5-V Supply (10% Tolerance)
- Automatic Powerdown when Deselected
- 3-State Output
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- Low Power Dissipation (V_{CC} = 5.5 V)
  —Active . . . 715 mW MAX
  —Standby . . . 55 mW MAX (TTL Inputs)
  —Standby . . .5.5 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  —SM Prefix . . . Standard Processing
  —SMJ Prefix . . . Class B Processing
- Packaging Options:
  —22 Pin Ceramic 300-mil DIP
  —22-Pad Leadless Ceramic Chip Carrier

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A15	Address Inputs
D	Data Input
Q	Data Output
$\overline{E}$	Chip Enable/Power Down
GND	Ground
V_{CC}	5-V Supply
$\overline{W}$	Write Enable

description

The '61CD64 is a separate I/O, 65,536-bit static random-access memory organized as 65,536 words by 1 bit. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six-transistor cell) memory array. The six-transistor cell provides for inherently lower soft error rates, improved stability across the operating temperature range, and low standby power compared to the four-transistor/two-poly load cell, making it ideal for military applications.

The '61CD64's static design and control signals ($\overline{E}$ and $\overline{W}$) remove the need for refresh circuitry and simplify timing requirements. The chip-enable pin provides for easy memory expansion and for automatic power-down. This feature, in conjunction with the full CMOS array, greatly reduces the overall memory power requirements.

Access time from either address or chip enable is a maximum of 25, 35, or 45 ns, allowing speed enhancements for new and existing designs.

operation

addresses (A0-A15)

The 16 address inputs select one of the 65,536 1-bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable/power down ($\overline{E}$)

The chip enable/power down terminal, which can be driven directly by standard TTL circuits, affects the data-in and data-out terminals and the internal functioning of the chip itself. Whenever the chip enable/power down is low (enabled), the device is operational, input and output terminals are enabled, and data can be read or written. When the chip enable/power down terminal is high (disabled), the device is deselected and put into a reduced-power standby mode. Data is retained during standby.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{E}$ must be high when changing addresses to prevent inadvertently writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

data in (D)

Data can be written into a selected device when the write-enable input is low. The input terminal can be driven directly from standard TTL circuits. Data on the input pin (D) is written into the memory location specified on the address pins (A0-A15).

data out (Q)

The three-state output buffer provides direct TTL compatibility with a fanout of twenty Series 54LS or 54ALS TTL gates, sixteen Series 54AS TTL gates, or thirteen Series 54F TTL gates. The output terminal is in the high-impedance state when chip enable ($\overline{E}$) is high or whenever a write operation is being performed. Data out is the same polarity as data in.

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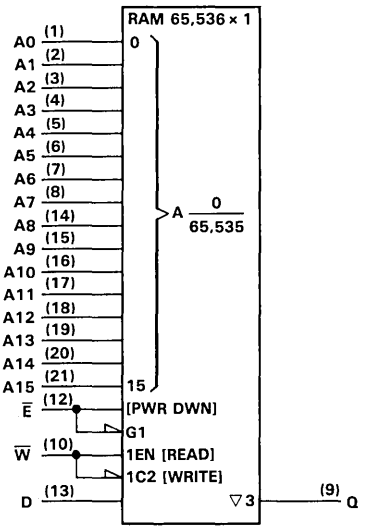
logic symbol†



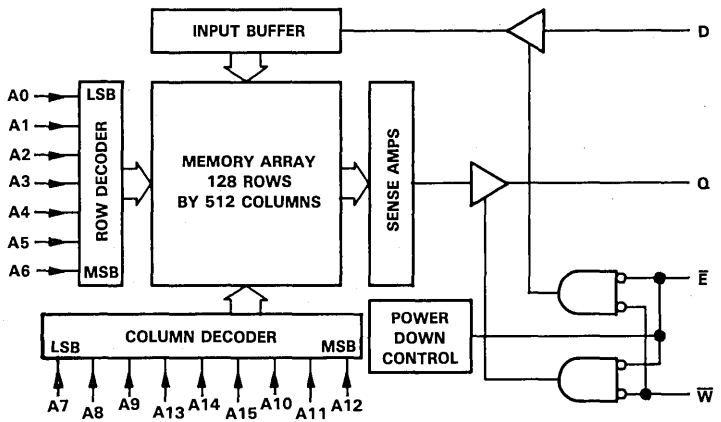
FUNCTION TABLE

INPUTS		OUTPUTS	MODE	POWER
Ē	W̄	Q		
H	X	HI-Z	Standby	Standby
L	H	Data Output	Read	Active
L	L	HI-Z	Write	Active

X = Don't Care.

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JD package.

functional block diagram



NOTE: Memory array shown is functionally equivalent to 256 rows by 256 columns.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range (see Note 2) . . . . . −1 V to 7 V
Output voltage range in high-impedance state . . . . . −0.5 V to 7 V
Output current . . . . . 20 mA
Minimum operating free-air temperature . . . . . −55°C
Maximum operating case-temperature . . . . . 125°C
Storage temperature range . . . . . −65°C to 150°C
Latch-up current . . . . . 200 mA

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to GND.
2. V_{IL} (MIN) of −3 V for short pulse durations of 20 ns or less. Prolonged operation at V_{IL} levels below −1 V will result in excessive currents that may damage the device.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_C	Operating case temperature			125	°C
T_A	Operating free-air temperature	−55			°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	'61CD64-25			'61CD64-35			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	−10		10	μA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−10		10	−10		10	μA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			130			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}$ ≥ V_{IH}, V_{CC} = 5.5 V			10			10	mA
		CMOS-level inputs	$\overline{E}$ = V_{CC} ± 0.3, V_{CC} = 5.5 V			0.9			0.9	mA

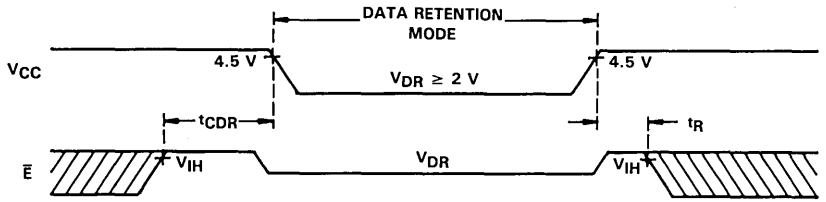
PARAMETER			TEST CONDITIONS	'61CD64-45			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	μA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−50		50	μA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}$ ≥ V_{IH}, V_{CC} = 5.5 V			10	mA
		CMOS-level inputs	$\overline{E}$ = V_{CC} ± 0.3, V_{CC} = 5.5 V			0.9	mA

data retention characteristics

PARAMETER		TEST CONDITION	MIN	TYP†		MAX		UNIT
				V_{CC} @ 2.0 V	V_{CC} @ 3.0 V	V_{CC} @ 2.0 V	V_{CC} @ 3.0 V	
V_{DR}	V_{CC} for data retention	$\overline{E} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, or $\leq$ GND + 0.2 V	2.0	—	—	—	—	V
I_{CCDR}	Data retention current			3	5	100	200	μA
t_{CDR}§	Chip deselect to data retention time		0	—		—		ns
t_R§	Operation recovery time		$t_{c(RD)}$‡	—		—		ns
I_{LI}§	Input leakage current			—		1		μA

†TYP values listed are typical values at 25°C.
‡$T_{c(RD)}$ = read cycle time.
§This parameter is guaranteed but not tested.

data retention waveform



capacitance, T_A = 25°C, f = 1 MHz¶

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5 V			5	pF
C_o	Output capacitance				7	pF

¶Capacitance measurements are made on sample basis only.

timing requirements over recommended supply voltage range and operating temperature range

		'61CD64-25			'61CD64-35			'61CD64-45			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(rd)}$	Read cycle time	25			35			45			ns
$t_{c(wr)}$	Write cycle time	25			35			45			ns
$t_{w(W)}$	Write-enable pulse duration	15			20			20			ns
$t_{su(E)}$	Chip-enable low to end of write	20			30			35			ns
$t_{su(A)}$	Address setup time to write start	0			0			0			ns
$t_{su(D)}$	Data setup time to write end	10			15			15			ns
$t_{h(A)}$	Address hold time from write end	0			0			0			ns
$t_{h(D)}$	Data hold time from write end	0			0			0			ns
t_{PU}	Delay time, chip-enable low to power up§	0			0			0			ns
t_{PD}	Delay time, chip-enable high to power down§			20			30			35	ns
t_{AW}	Address setup to write end	20			25			35			ns

§This parameter is guaranteed but not tested.

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS	'61CD64-25		'61CD64-35		UNIT
			MIN	TYP MAX	MIN	TYP MAX	
$t_{a(A)}$	Access time from address	I_{OH} = −4 mA, I_{OL} = 8 mA		25		35	ns
$t_{a(E)}$	Access time from chip enable low	C_L = 30 pF,		25		35	ns
$t_{v(A)}$	Output data valid after address change	See Figure 1a.	5		5		ns
$t_{en(W)}$	Output enable time from write enable high†		3		3		ns
$t_{en(E)}$	Output enable time from chip enable low†	R1 = 481 Ω, R2 = 255 Ω,	5		5		ns
$t_{dis(E)}$	Output disable time from chip enable high†	C_L = 5 pF, See Figure 1b.		10		15	ns
$t_{dis(W)}$	Output disable time from write enable low†			7		10	ns

PARAMETER		TEST CONDITIONS	'61CD64-45		UNIT
			MIN	TYP MAX	
$t_{a(A)}$	Access time from address	I_{OH} = −4 mA, I_{OL} = 8 mA		45	ns
$t_{a(E)}$	Access time from chip enable low	C_L = 30 pF,		45	ns
$t_{v(A)}$	Output data valid after address change	See Figure 1a.	5		ns
$t_{en(W)}$	Output enable time from write enable high†		3		ns
$t_{en(E)}$	Output enable time from chip enable low†	R1 = 481 Ω, R2 = 255 Ω,	5		ns
$t_{dis(E)}$	Output disable time from chip enable high†	C_L = 5 pF, See Figure 1b.		15	ns
$t_{dis(W)}$	Output disable time from write enable low†			15	ns

†Transition is measured ±500 mV from steady voltage; this parameter is guaranteed but not tested.

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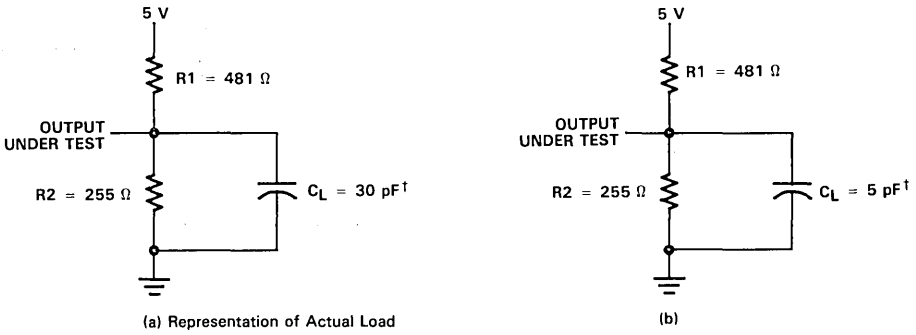
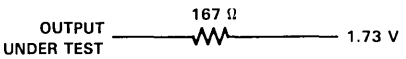
PARAMETER MEASUREMENT INFORMATION



(a) Representation of Actual Load

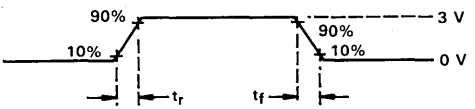
(b)

THEVENIN EQUIVALENT OF (a) OR (b)



†C_L includes jig and scope capacitances.

FIGURE 1. OUTPUT LOAD CIRCUIT

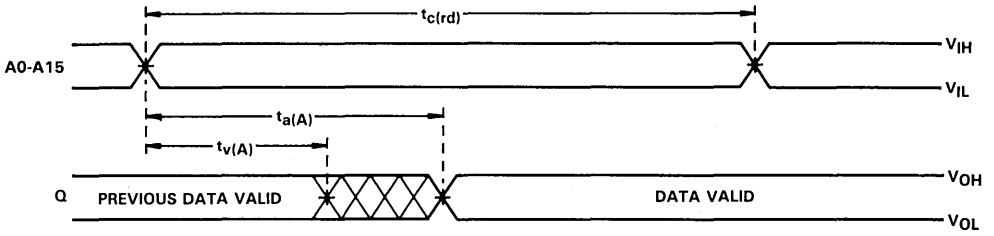


NOTE 4: t_r and $t_f \leq 5$ ns.

FIGURE 2. TRANSITION TIMES

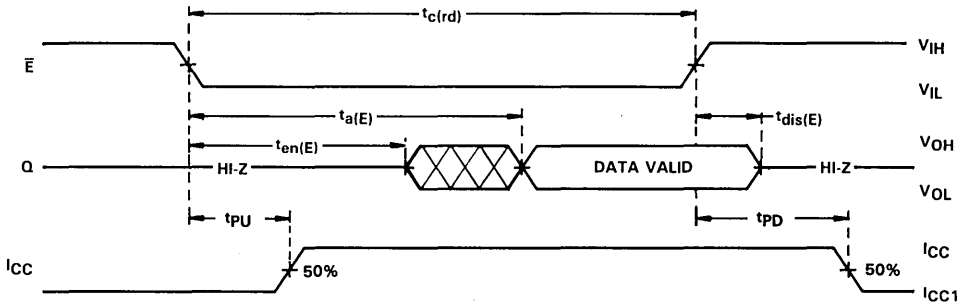
NOTE: All switching characteristics and timing requirements assume test conditions as depicted in Figures 1 and 2 with timing references of 1.5 V (50% reference point) as shown in the subsequent timing diagrams.

read cycle timing from address†



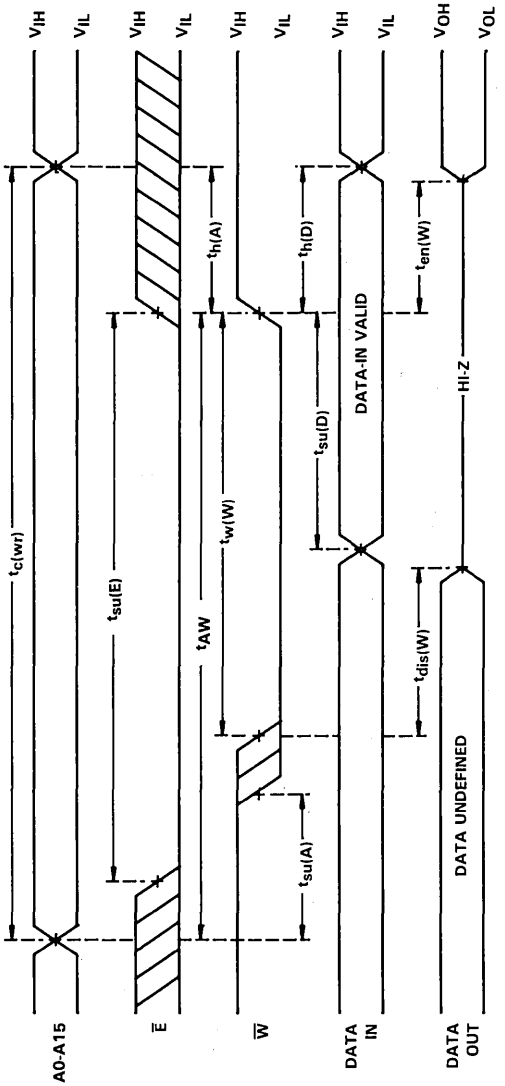
†$\overline{W}$ is high, and $\overline{E}$ is low.

read cycle timing from chip enable‡



‡$\overline{W}$ is high, address is valid prior to or simultaneously with the high-to-low transition of $\overline{E}$.

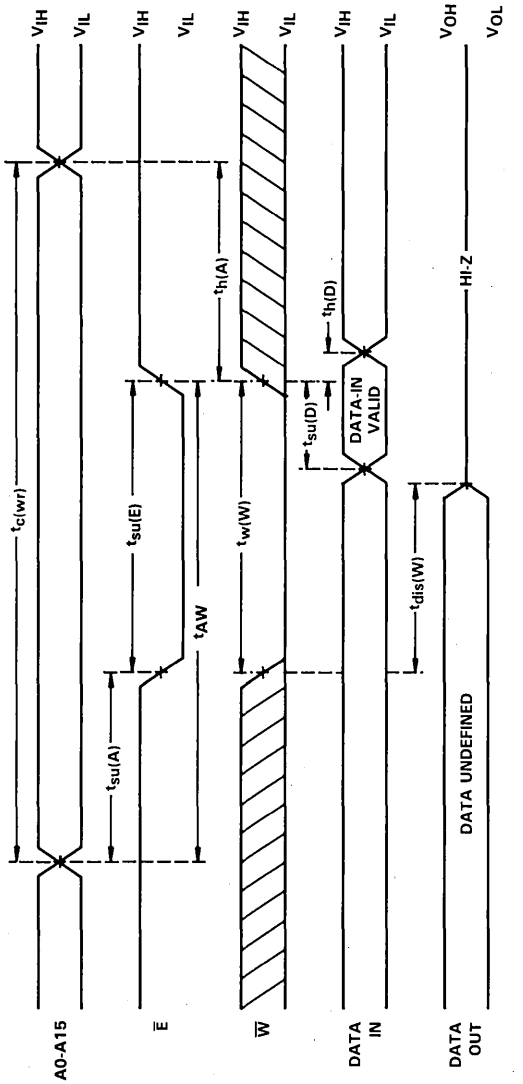
Write cycle timing controlled by write enable†



†$\overline{E}$ or $\overline{W}$ must be high during address transitions.

NOTE: For both $\overline{W}$-controlled and $\overline{E}$-controlled Write operations, the internal write time of the memory is defined by the overlap of $\overline{E}$ low and $\overline{W}$ low. Both signals must be low to initiate a write, and either signal can terminate a write by going high. The data input setup and hold times should be referenced to the edge that terminates the write.

write cycle timing controlled by chip enable†

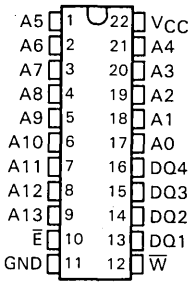


†Ē or W̄ must be high during address transitions.

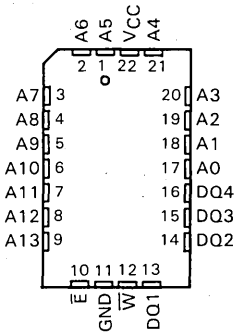
JULY 1987 – REVISED MAY 1988

- 16,384 × 4 Organization
- Common I/O
- Military Temperature Range . . . −55°C to 125°C (M Suffix)
- Fast Static Operation
- Maximum Access Time from Address or Chip Enable
  '64C64-25 . . . 25 ns
  '64C64-35 . . . 35 ns
  '64C64-45 . . . 45 ns
- Single 5-V Supply (10% Tolerance)
- Battery Backup Operation . . . 2 Volt Data Retention
- Automatic Powerdown When Deselected
- 3-State Output
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- Low Power Dissipation (V_{CC} = 5.5 V)
  — Active . . .715 mW MAX
  — Standby . . . 55 mW MAX (TTL Inputs)
  — Standby . . . 5.5 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  — SM Prefix . . . Standard Processing
  — SMJ Prefix . . . Class B Processing
- Packaging Options:
  — 22-Pin Ceramic 300-mil DIP
  — 22-Pad Leadless Ceramic Chip Carrier

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A13	Address Inputs
DQ1-DQ4	Data In/Data Out
$\overline{E}$	Chip Enable/Power Down
GND	Ground
V_{CC}	5-V Supply
$\overline{W}$	Write Enable

description

The '64C64 is a common I/O, 65,536-bit static random-access memory organized as 65,536 words by 4 bits. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six transistor cell) memory array. The six transistor cell provides for inherently lower soft error rates, improved stability across the operating temperature range, and low standby power compared to the four-transistor/two-poly load cell, making it ideal for military applications.

The '64C64's static design and control signals ($\overline{E}$ and $\overline{W}$) remove the need for refresh circuitry and simplify timing requirements. The chip-enable pin provides for easy memory expansion and for automatic power-down. This feature, in conjunction with the full CMOS array, greatly reduces the overall memory power requirements. Access time from either address or chip enable is a maximum of 25, 35, or 45 ns, allowing speed enhancements for new and existing designs.

operation

addresses (A0-A13)

The 14 address inputs select one of the 16,384 4-bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable/power down ($\overline{E}$)

The chip enable/power down terminal, which can be driven directly by standard TTL circuits, affects the data-in and data-out terminals and the internal functioning of the chip itself. Whenever the chip enable/power down is low (enabled), the device is operational, input and output terminals are enabled, and data can be read or written. When the chip enable/power down terminal is high (disabled), the device is deselected and put into a reduced-power standby mode. Data is retained during standby.

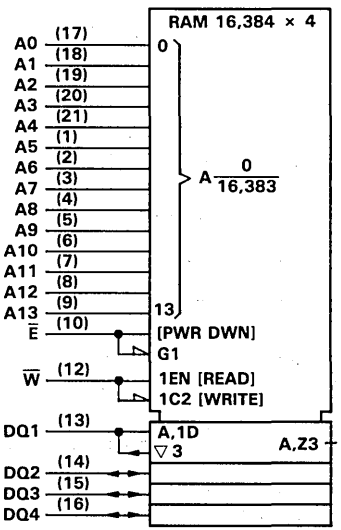
write enable ($\overline{W}$)

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{E}$ must be high when changing addresses to prevent inadvertently writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

data in/data out (DQ1-DQ4)

Data can be written into a selected device when the write-enable input is low. The DQ terminals can be driven directly from standard TTL circuits. The three-state output buffer provides direct TTL compatibility with a fanout of twenty Series 54LS or 54ALS TTL gates, sixteen Series 54AS TTL gates, or thirteen Series 54F TTL gates. The DQ terminals are in the high-impedance state when chip enable ($\overline{E}$) is high or whenever a write operation is being performed. Data out is the same polarity as data in.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JD package.

FUNCTION TABLE

INPUTS		OUTPUTS	MODE	POWER
$\overline{E}$	$\overline{W}$	Q		
H	X	HI-Z	Standby	Standby
L	H	Data Output	Read	Active
L	L	HI-Z	Write	Active

X = Don't Care.

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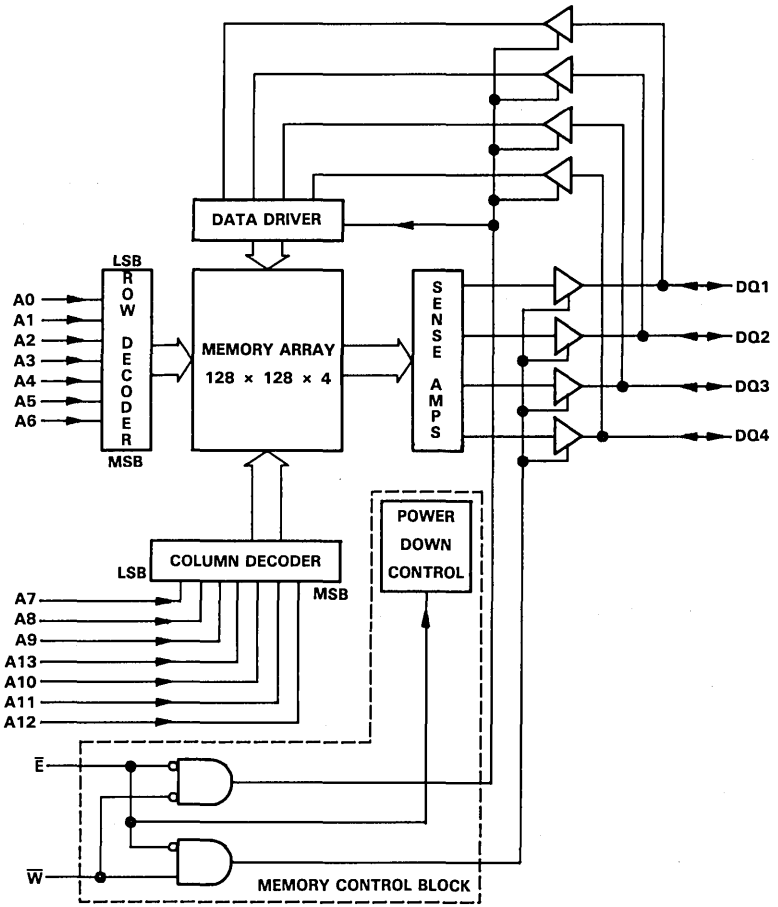
functional block diagram



NOTE: Memory array shown is functionally equivalent to 256 × 64 × 4.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1) . . . . . −0.5 V to 7
Input voltage range (see Note 2) . . . . . −1 V to 7
Output voltage range in high-impedance state . . . . . −1.0 V to 7
Output current . . . . . 20 n
Minimum operating free-air temperature . . . . . −55
Maximum operating case-temperature 125
Storage temperature range . . . . . −65°C to 150
Latch-up current . . . . . 200 n

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rat only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operat Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may aff device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to GND.
2. V_{IL} (MIN) of −3 V for short pulse durations of 20 ns or less. Prolonged operation at V_{IL} levels below −1 V will resul excessive currents that may damage the device.

recommended operating conditions

		MIN	NOM	MAX	UNI
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_C	Operating case temperature			125	°C
T_A	Operating free-air temperature	−55			°C

NOTE 2: V_{IL} (MIN) of −3 V for short pulse durations of 20 ns or less. Prolonged operation at V_{IL} levels below −1 V will result in excess currents that may damage the device.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise note

PARAMETER			TEST CONDITIONS	'64C64-25			'64C64-35			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	−10		10	μA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−10		10	−10		10	μA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			130			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E} \geq V_{IH}$, V_{CC} = 5.5 V			10			10	mA
		CMOS-level inputs	$\overline{E} = V_{CC}\pm0.3$ V, V_{CC} = 5.5 V			0.9			0.9	mA

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

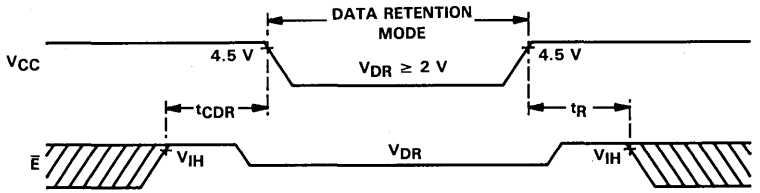
PARAMETER			TEST CONDITIONS	'64C64-45 MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	μA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−10		10	μA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}$ ≥ V_{IH}, V_{CC} = 5.5 V			10	mA
		CMOS-level inputs	$\overline{E}$ = V_{CC} ± 0.2 V, V_{CC} = 5.5 V			0.9	mA

data retention characteristics

PARAMETER		TEST CONDITION	MIN	TYP† V_{CC} @ 2.0 V	TYP† V_{CC} @ 3.0 V	MAX V_{CC} @ 2.0 V	MAX V_{CC} @ 3.0 V	UNIT
V_{DR}	V_{CC} for data retention	$\overline{E}$ ≥ V_{CC} − 0.2 V, V_{IN} ≥ V_{CC} − 0.2 V or ≤ GND + 0.2 V	2.0	—	—	—	—	V
I_{CCDR}	Data retention current			3	5	100	200	μA
t_{CDR}§	Chip deselect to data retention time		0	—		—		ns
t_R§	Operation recovery time		$t_{c(RD)}$‡	—		—		ns
I_{LI}§	Input leakage current			—		1		μA

†TYP values listed are typical values at 25°C.
‡$t_{c(RD)}$ = read cycle time.
§This parameter is guaranteed but not tested.

data retention waveform



capacitance, T_A = 25°C, = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5 V			5	pF
C_o	Output capacitance				7	

†Capacitance measurements are made on sample basis only.

timing requirements over recommended supply voltage range and operating temperature range

		'64C64-25			'64C64-35			'64C64-45			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(rd)}$	Read cycle time	25			35			45			ns
$t_{c(wr)}$	Write cycle time	25			35			45			ns
$t_{w(W)}$	Write-enable pulse duration	20			25			35			ns
$t_{su(E)}$	Chip-enable low to end of write	20			30			35			ns
$t_{su(A)}$	Address setup time to write start	0			0			0			ns
$t_{su(D)}$	Data setup time to write end	10			15			15			ns
$t_{h(A)}$	Address hold time from write end	0			0			0			ns
$t_{h(D)}$	Data hold time from write end	0			0			0			ns
t_{PU}	Delay time, chip-enable low to power up‡	0			0			0			ns
t_{PD}	Delay time, chip-enable high to power down‡			25			35			35	ns
t_{AW}	Address setup to write end	20			25			35			ns

‡This parameter is guaranteed but not tested.

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS	'64C64-25		'64C64-35		'64C64-45		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	R1 = 481 Ω, R2 = 255 Ω, C_L = 30 pF, See Figure 1a.		25		35		45	ns
$t_{a(E)}$	Access time from chip enable low			25		35		45	ns
$t_{v(A)}$	Output data valid after address change		5		5		5		ns
$t_{en(W)}$	Output enable time from write enable high§	R1 = 481 Ω, R2 = 255 Ω, C_L = 5 pF, See Figure 1b.	3		3		3		ns
$t_{en(E)}$	Output enable time from chip enable low§		5		5		5		ns
$t_{dis(E)}$	Output disable time from chip enable high§			10		15		15	ns
$t_{dis(W)}$	Output disable time from write enable low§			7		10		15	ns

§Transition is measured ±500 mV from steady state voltage. This parameter is guaranteed but not tested.

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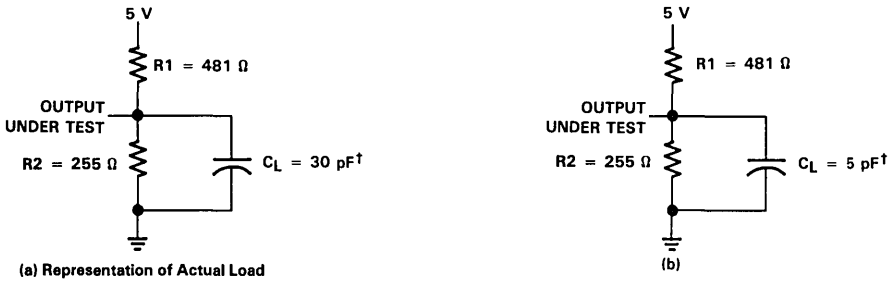
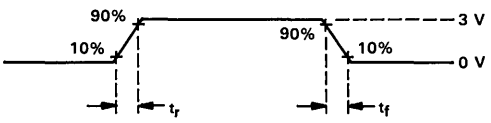
PARAMETER MEASUREMENT INFORMATION



†C_L includes jig and scope capacitances.

FIGURE 1. OUTPUT LOAD CIRCUIT

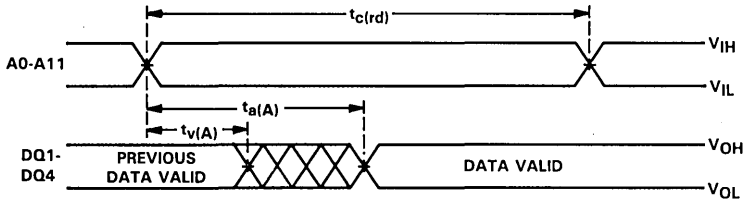


NOTE 5: t_r and $t_f \leq 5$ ns.

FIGURE 2. TRANSITION TIMES

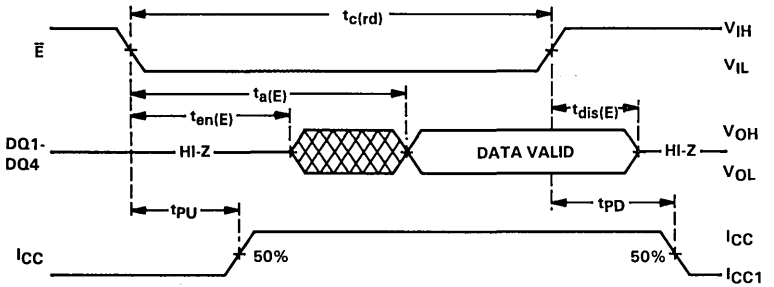
NOTE: All switching characteristics and timing requirements assume test conditions as depicted in Figures 1 and 2 with timing references of 1.5 V (50% point) as shown in the subsequent timing diagrams.

read cycle timing from address†



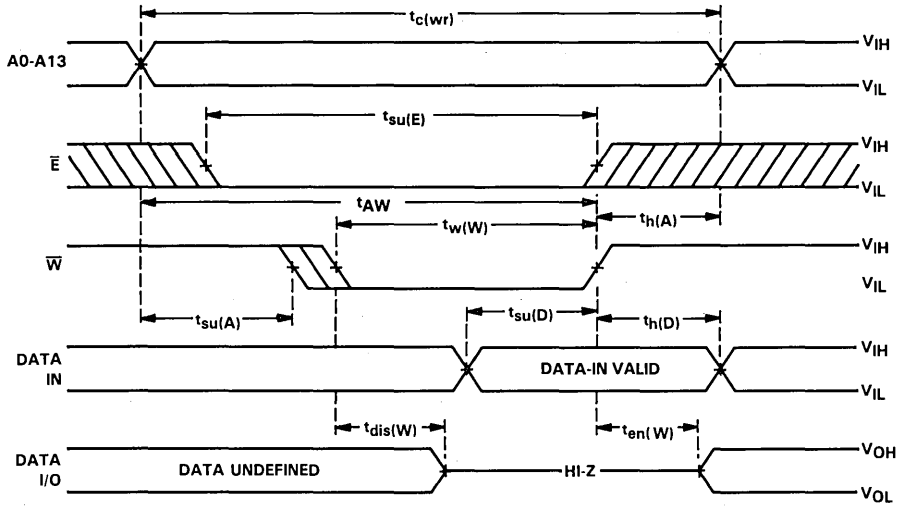
†$\overline{W}$ is high, and $\overline{E}$ is low.

read cycle timing from chip enable‡



‡$\overline{W}$ is high, address is valid prior to or simultaneously with the high-to-low transition of $\overline{E}$.

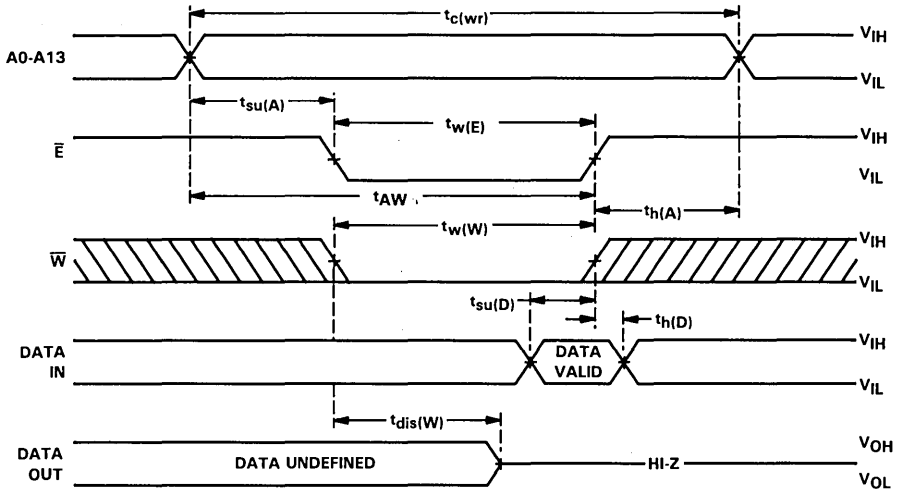
write cycle timing controlled by write enable†



†$\overline{E}$ or $\overline{W}$ must be high during address transitions.

NOTE: For both $\overline{W}$-controlled and $\overline{E}$-controlled Write operations, the internal write time of the memory is defined by the overlap of $\overline{E}$ low and $\overline{W}$ low. Both signals must be low to initiate a write, and either signal can terminate a write by going high. The data input setup and hold times should be referenced to the edge that terminates the write.

write cycle timing controlled by chip enable†

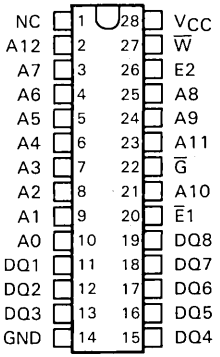


†$\overline{E}$ or $\overline{W}$ must be high during address transitions.

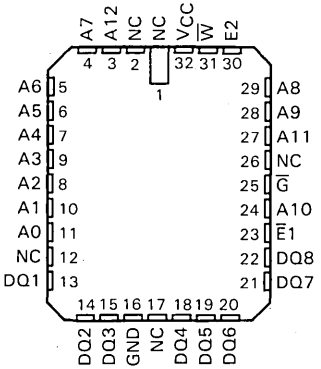
APRIL 1987 – REVISED MAY 1988

- 8192 × 8 Organization
- Common I/O
- Military Temperature Range . . . −55°C to 125°C (M Suffix)
- Fast Static Operation
- Battery Back-Up Operation . . . 2-Volt Data Retention
- Maximum Access Time from Address or Chip Enable
  '68CE64-25 . . . 25 ns
  '68CE64-35 . . . 35 ns
  '68CE64-45 . . . 45 ns
- Single 5-V Supply (10% Tolerance)
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- 3-State Outputs
- Low Power Dissipation (V_{CC} = 5.5 V)
  — Active . . . 660 mW MAX
  — Standby . . . 55 mW MAX (TTL Inputs)
  — Standby . . . 5.5 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  — SM Prefix . . . Standard Processing
  — SMJ Prefix . . . Class B Processing
- Output Enable for Bus Control
- Two Chip-Enable Pins for Increased Flexibility
- Packaging Options:
  — 28-Pin Ceramic 300-mil DIP
  — 32-Pad Leadless Ceramic Chip Carrier

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Address Inputs
DQ1-DQ8	Data In-Data Out
$\overline{E}1$	Chip Enable/Power Down
E2	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
V_{CC}	5-V Supply
$\overline{W}$	Write Enable

description

The '68CE64 is a common I/O, 65,536-bit static random-access memory organized as 8192 words by 8 bits. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six transistor cell) memory array. Access time from chip enable or address is available for 25, 35, or 45 ns cycle times, while maximum power dissipation is less than 660 mW. This reduces to 55 mW (TTL Inputs) or 5.5 mW (CMOS Inputs) during standby operation.

The '68CE64's static design and control signals ($\overline{E}1$, E2, $\overline{G}$, and $\overline{W}$) remove the need for refresh circuitry and simplify timing requirements. The two enable pins add flexibility and simplify memory expansion/design. The output-enable pin minimizes bus contention problems.

The '68CE64 static RAM provides single 5-V operation with all inputs and outputs compatible with standard TTL and CMOS voltage levels.

operation

addresses (A0-A12)

The 13 address inputs select one of the 8192 8-bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL without external pull-up resistors.

chip enable/power down ($\overline{E}1$)

The chip enable/power down terminal ($\overline{E}1$) can be driven directly by standard TTL circuits, and affects the powerdown/deselect function of the chip. Whenever $\overline{E}1$ is high (disabled), the device is put into a reduced power standby mode. Data is retained during the standby mode.

chip enable (E2)

The chip enable terminal (E2) affects the chip deselect function. Whenever chip enable (E2) is high (enabled), and chip enable/powerdown ($\overline{E}1$) is low (enabled) the device is operational, and data may be written or read provided input and output terminals are enabled. Whenever chip enable (E2) is low and chip enable/powerdown ($\overline{E}1$) is low, the device is in the powered-up deselected state.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{E}1$ must be high or E2 must be low when changing addresses to prevent inadvertently writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

output enable ($\overline{G}$)

The output-enable terminal, which can be driven directly from standard TTL circuits, affects only the data-out terminals. When output enable is at a logic high level, the output terminals are disabled to the high-impedance state. Output enable provides greater output control flexibility, simplifying data bus design.

data in/data out (DQ1-DQ9)

Data can be written into a selected device when the write-enable ($\overline{W}$) input is low, chip enable/powerdown ($\overline{E}1$) is low, and chip enable (E2) is high. Data can be read when write enable ($\overline{W}$) is high, chip enable/powerdown ($\overline{E}1$) is low, chip enable (E2) is high, and output enable ($\overline{G}$) is low. The DQ terminals can be driven directly from standard TTL circuits. The three-state output buffers provide direct TTL compatibility with a fanout of twenty Series 54LS or 54ALS TTL gates, sixteen Series 54AS TTL gates, or thirteen Series 54F TTL gates.

TEXAS INSTRUMENTS
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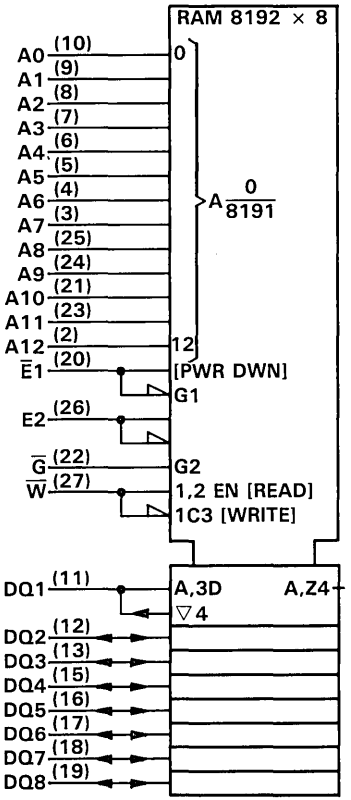
logic symbol†



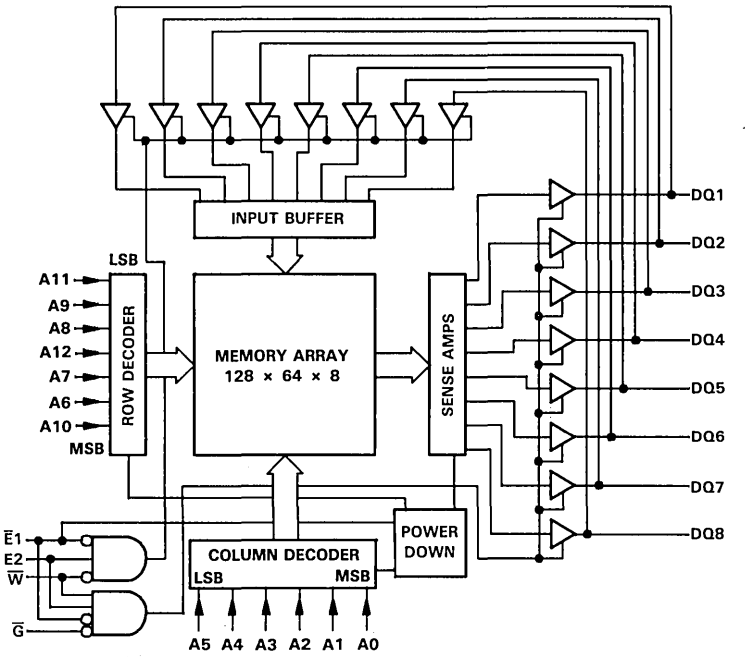
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JD package.

FUNCTION TABLE

Ē1	E2	W̅	G̅	Input/Outputs	Mode
H	X	X	X	High Z	Deselect Power Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

X = Don't Care.

functional block diagram



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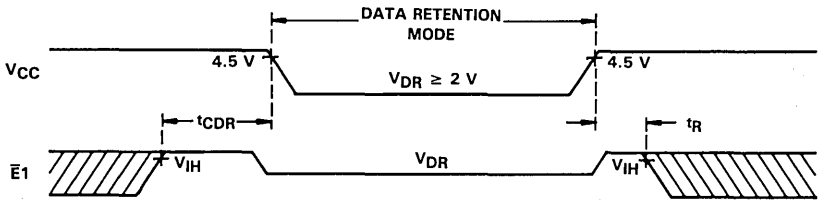
data retention characteristics

PARAMETER		TEST CONDITION	MIN	TYP† V_{CC} @ 2.0 V	TYP† V_{CC} @ 3.0 V	MAX V_{CC} @ 2.0 V	MAX V_{CC} @ 3.0 V	UNIT
V_{DR}	V_{CC} for data retention	$\overline{E}1 \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, or $\leq$ GND + 0.2 V	2.0	—	—	—	—	V
I_{CCDR}	Data retention current			3	5	100	200	μA
t_{CDR}§	Chip deselect to data retention time		0	—		—		ns
t_R§	Operation recovery time		$t_{c(RD)}$‡	—		—		ns
I_{LI}§	Input leakage current			—		1		μA

†TYP values listed are typical values at 25°C.
‡$T_{c(RD)}$ = read cycle time.
§This parameter is guaranteed but not tested.

data retention waveform



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range (see Note 2) . . . . . −1 V to 7 V
Output voltage range in high-impedance state . . . . . −0.5 V to 7 V
Output current . . . . . 20 mA
Minimum operating free-air temperature . . . . . −55°C
Maximum operating case-temperature . . . . . 125°C
Storage temperature range . . . . . −65°C to 150°C
Latch-up current . . . . . 200 mA

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values in this data sheet are with respect to GND.
2. V_{IL} (min) for short pulse durations of 20 ns or less. Prolonged operation at V_{IL} levels below −1 V will result in excessive currents that may damage the device input.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_C	Operating case temperature			125	°C
T_A	Operating free-air temperature	−55			°C

NOTE 2: V_{IL} (min) for short pulse durations of 20 ns or less. Prolonged operation at V_{IL} levels below −1 V will result in excessive current that may damage the device input.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	'68CE64-25			'68CE64-35			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	−10		10	μA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−10		10	−10		10	μA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			130			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}1 \geq V_{IH}$, V_{CC} = 5.5 V			10			10	mA
		CMOS-level inputs	$\overline{E}1 = V_{CC}\pm0.3$, V_{CC} = 5.5 V			0.9			0.9	mA

PARAMETER			TEST CONDITIONS	'68CE64-45			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	μA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−10		10	μA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}1 \geq V_{IH}$, V_{CC} = 5.5 V			10	mA
		CMOS-level inputs	$\overline{E}1 = V_{CC}\pm0.3$, V_{CC} = 5.5 V			0.9	mA

capacitance, T_A = 25°C, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5 V			5	pF
C_o	Output capacitance				7	pF

†Capacitance measurements are made on sample basis only.

timing requirements over recommended supply voltage range and operating temperature range

		'68CE64-25			'68CE64-35			'68CE64-45			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(rd)}$	Read cycle time	25			35			45			ns
$t_{c(wr)}$	Write cycle time	25			35			45			ns
$t_{w(W)}$	Write-enable pulse duration	15			20			25			ns
$t_{su(E1)}$	Chip-enable 1 low to end of write	20			30			40			ns
$t_{su(E2)}$	Chip-enable 2 high to end of write	15			20			25			ns
$t_{su(A)}$	Address setup time to write start	0			0			0			ns
$t_{su(D)}$	Data setup time to write end	10			15			20			ns
$t_{h(A)}$	Address hold time from write end	0			0			0			ns
$t_{h(D)}$	Data hold time from write end	0			0			0			ns
t_{PU}	Delay time, chip-enable $\overline{E}1$ low to power up‡	0			0			0			ns
t_{PD}	Delay time, chip-enable $\overline{E}1$ high to power down‡			20			20			25	ns
t_{AW}	Address setup to write end	25			30			40			ns

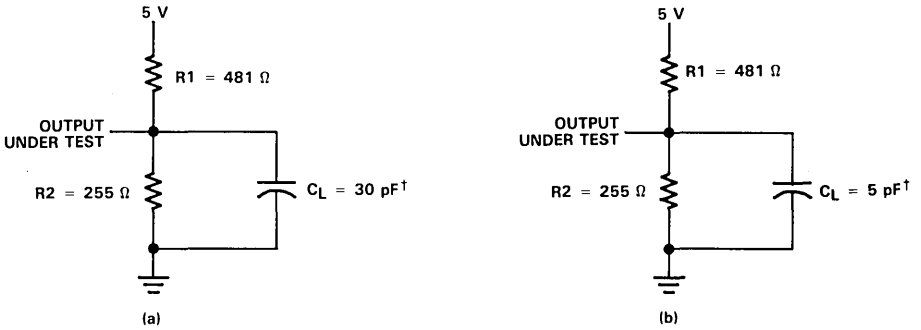
switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS	'68CE64-25	'68CE64-35	'68CE64-45	UNIT
			MIN MAX	MIN MAX	MIN MAX	
$t_{a(A)}$	Access time from address	R1 = 481 Ω, R2 = 255 Ω, C_L = 30 pF, See Figure 1a	25	35	45	ns
$t_{a(E1)}$	Access time from chip enable $\overline{E}1$ low		25	35	45	ns
$t_{a(E2)}$	Access time from chip enable E2 high		20	25	30	
$t_{a(G)}$	Access time from output enable low		15	20	20	
$t_{v(A)}$	Output data valid after address change		3	3	3	ns
$t_{en(W)}$	Output enable time from write enable high	R2 = 255 Ω, R1 = 481 Ω, C_L = 5 pF, See Figure 1b and Note 4	0	0	3	ns
$t_{en(E1)}$	Output enable time from chip enable $\overline{E}1$ low		0	0	3	ns
$t_{en(E2)}$	Output enable time from chip enable E2 high		0	0	3	ns
$t_{en(G)}$	Output enable time from output enable low		0	0	0	ns
$t_{dis(E1)}$	Output disable time from chip enable $\overline{E}1$ high		15	15	20	
$t_{dis(E2)}$	Output disable time from chip enable E2 low		15	15	20	
$t_{dis(W)}$	Output disable time from write enable low		10	15	20	
$t_{dis(G)}$	Output disable time from output enable high		10	15	20	ns

‡This parameter is guaranteed but not tested.

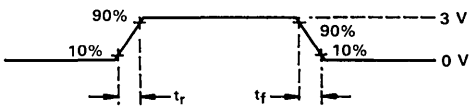
NOTE 4: Transition is measured ±500 mV from steady state voltage. This parameter is guaranteed but not tested.

PARAMETER MEASUREMENT INFORMATION



†C_L includes jig and scope capacitances.

FIGURE 1. OUTPUT LOAD CIRCUIT

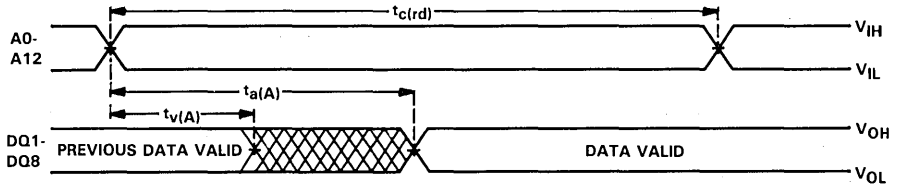


NOTE 5: t_r and $t_f \leq 5$ ns.

FIGURE 2. TRANSITION TIMES

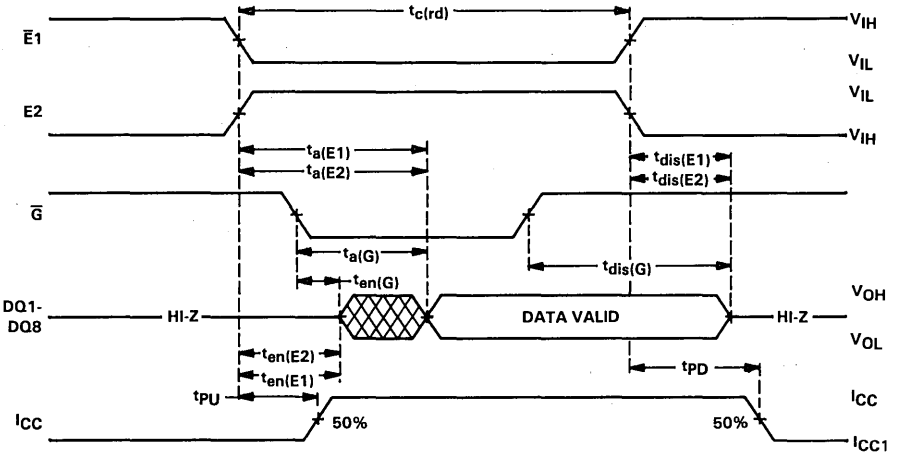
NOTE: All switching characteristics and timing requirements assume test conditions as depicted in Figures 1 and 2 with timing references of 1.5 V (50% reference point) as shown in the subsequent timing diagrams.

read cycle timing from address†



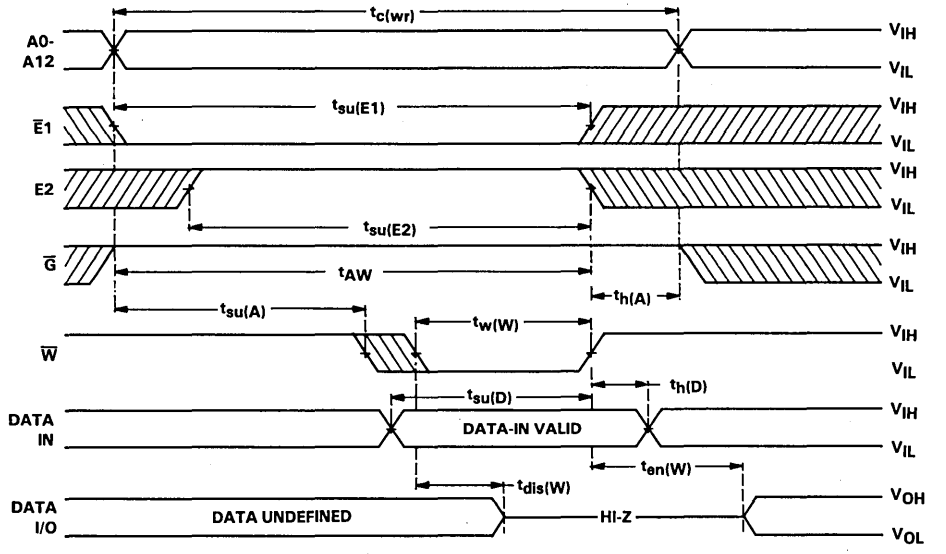
†$\overline{W}$ is high, and $\overline{E}$ is low.

read cycle timing from chip enable‡



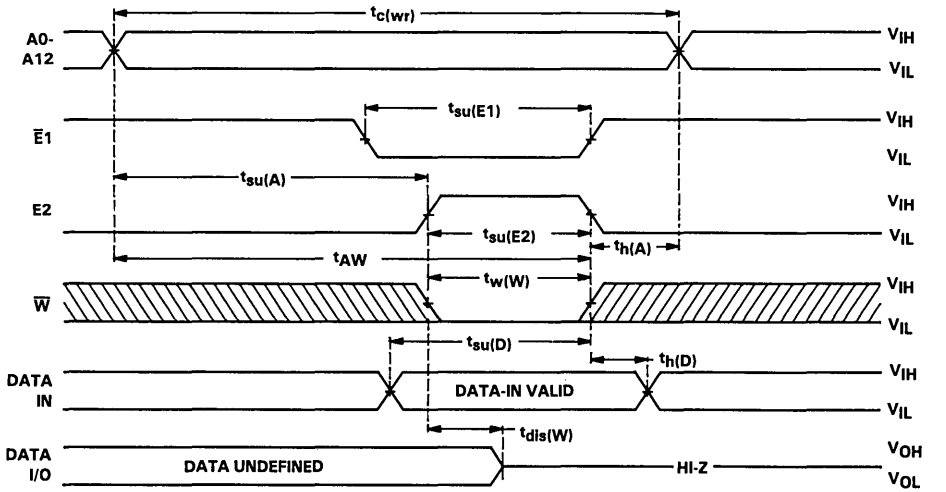
‡$\overline{W}$ is high, address is valid prior to or simultaneously with the high-to-low transition of $\overline{E}$.

write cycle timing controlled by write enable†



†$\overline{E}1$ or $\overline{W}$ must be high during address transitions.

write cycle timing controlled by chip enable†

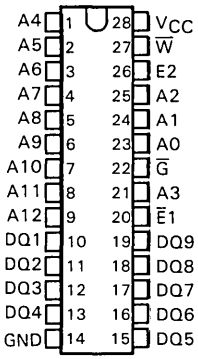


†$\overline{E}$ or $\overline{W}$ must be high during address transitions.

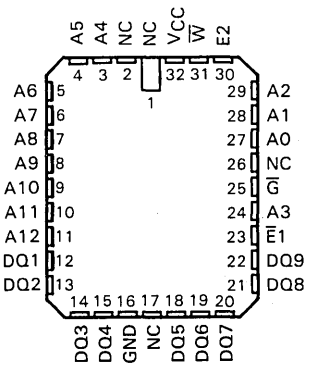
APRIL 1987—REVISED MAY 1988

- 8192 × 9 Organization
- Common I/O
- Military Temperature Range . . . −55°C to 125°C (M Suffix)
- Fast Static Operation
- Battery Back-Up Operation . . . 2-Volt Data Retention
- Maximum Access Time from Address or Chip Enable
  '69CE72-25 . . . 25 ns
  '69CE72-35 . . . 35 ns
  '69CE72-45 . . . 45 ns
- Single 5-V Supply (10% Tolerance)
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- 3-State Outputs
- Low Power Dissipation (V_{CC} = 5.5 V)
  — Active . . . 660 mW MAX
  — Standby . . . 55 mW MAX (TTL Inputs)
  — Standby . . . 5.5 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  — SM Prefix . . . Standard Processing
  — SMJ Prefix . . . Class B Processing
- Output Enable for Bus Control
- Two Chip-Enable Pins for Increased Flexibility
- Packaging Options:
  — 28-Pin Ceramic 300-mil DIP
  — 32-Pad Leadless Ceramic Chip Carrier

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Address Inputs
DQ1-DQ9	Data In/Data Out
$\overline{E}1$	Chip Enable/Power Down
E2	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
V_{CC}	5-V Supply
$\overline{W}$	Write Enable

description

The '69CE72 is a common I/O, 73,728-bit static random-access memory organized as 8192 words by 9 bits. Bit nine is generally used for parity bit storage for improved system reliability. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six transistor cell) memory array. Access time from chip enable or address is available for 25, 35, or 45 ns cycle times, while maximum power dissipation is less than 660 mW. This reduces to 55 mW (TTL Inputs) or 5.5 mW (CMOS Inputs) during standby operation.

The '69CE72's static design and control signals ($\overline{E}1$, E2, $\overline{G}$ and $\overline{W}$) remove the need for refresh circuitry and simplify timing requirements. The two enable pins add flexibility and simplify memory expansion/design. The output-enable pin minimizes bus contention problems.

The '69CE72 static RAM provides single 5-V operation with all inputs and outputs fully compatible with standard TTL and CMOS voltage levels.

operation

addresses (A0-A12)

The 13 address inputs select one of the 8192 9-bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL without external pull-up resistors.

chip enable/power down ($\overline{E}1$)

The chip enable/power down terminal ($\overline{E}1$) can be driven directly by standard TTL circuits, and affects the powerdown/deselect function of the chip. Whenever $\overline{E}1$ is high (disabled), the device is put into a reduced power standby mode. Data is retained during the standby mode.

chip enable (E2)

The chip enable terminal (E2) affects the chip deselect function. Whenever chip enable (E2) is high (enabled), and chip enable/powerdown ($\overline{E}1$) is low (enabled) the device is operational, and data may be written or read provided input and output terminals are enabled. Whenever chip enable (E2) is low and chip enable/powerdown ($\overline{E}1$) is low, the device is in the powered-up deselected state.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{E}1$ must be high or E2 must be low when changing addresses to prevent inadvertently writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

output enable ($\overline{G}$)

The output-enable terminal, which can be driven directly from standard TTL circuits, affects only the data-out terminals. When output enable is at a logic high level, the output terminals are disabled to the high-impedance state. Output enable provides greater output control flexibility, simplifying data bus design.

data in/data out (DQ1-DQ9)

Data can be written into a selected device when the write-enable ($\overline{W}$) input is low, chip enable/powerdown ($\overline{E}1$) is low, and chip enable (E2) is high. Data can be read when write enable ($\overline{W}$) is high, chip enable/powerdown ($\overline{E}1$) is low, chip enable (E2) is high, and output enable ($\overline{G}$) is low. The DQ terminals can be driven directly from standard TTL circuits. The three-state output buffers provide direct TTL compatibility with a fanout of twenty Series 54LS or 54ALS TTL gates, sixteen Series 54AS TTL gates, or thirteen Series 54F TTL gates.

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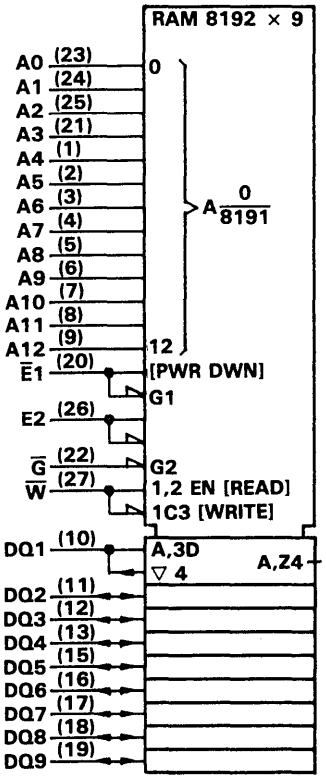
logic symbol†



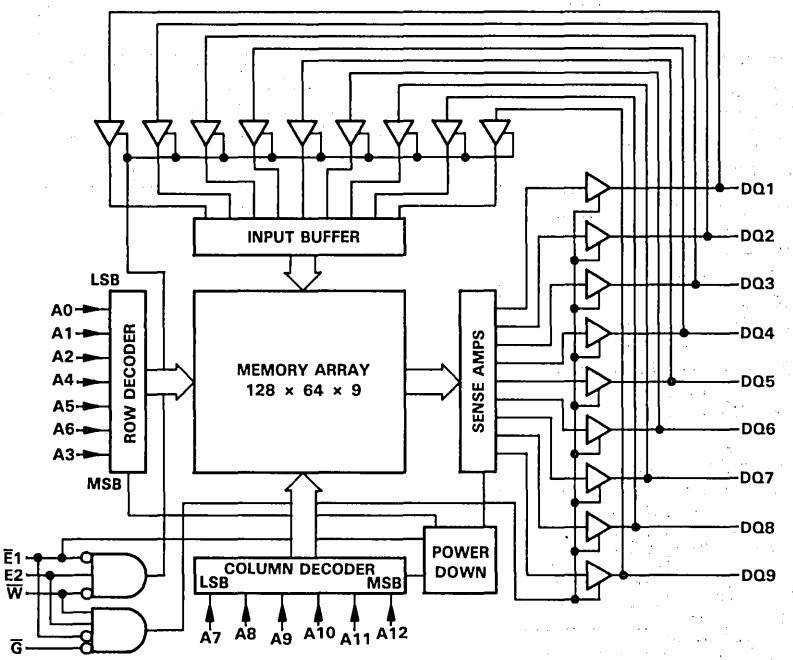
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JD package.

FUNCTION TABLE

Ē1	E2	W̅	G̅	Input/Outputs	Mode
H	X	X	X	High Z	Deselect Power Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

X = Don't Care.

functional block diagram



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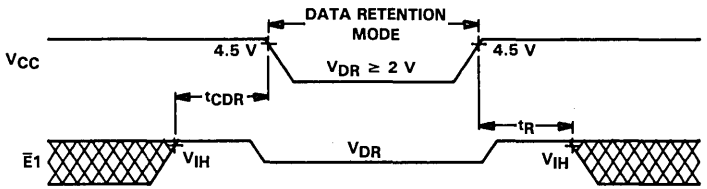
data retention characteristics

PARAMETER		TEST CONDITION	MIN	TYP† V_{CC} @ 2.0 V	TYP† V_{CC} @ 3.0 V	MAX V_{CC} @ 2.0 V	MAX V_{CC} @ 3.0 V	UNIT
V_{DR}	V_{CC} for data retention	$\overline{E}1 \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, or $\leq$ GND + 0.2 V	2.0	–	–	–	–	V
I_{CCDR}	Data retention current			3	5	100	200	μA
t_{CDR}§	Chip deselect to data retention time		0	–		–		ns
t_R§	Operation recovery time		$t_{c(RD)}$‡	–		–		ns
I_{LI}§	Input leakage current			–		1		μA

†TYP values listed are typical values at 25°C.
‡$t_{c(RD)}$ = read cycle time.
§This parameter is guaranteed but not tested.

data retention waveform



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range (see Note 2) . . . . . −1 V to 7 V
Output voltage range in high-impedance state . . . . . −0.5 V to 7 V
Output current . . . . . 20 mA
Minimum operating free-air temperature . . . . . −55°C
Maximum operating case-temperature . . . . . 125°C
Storage temperature range . . . . . −65°C to 150°C
Latch-up current . . . . . 200 mA

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to GND.
2. Prolonged operation at V_{IL} levels below −1 V will result in excessive currents that may damage the device input.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 3)	−1		0.8	V
T_C	Operating case temperature			125	°C
T_A	Operating free-air temperature	−55			°C

NOTE 3: V_{IL} (min) for short pulse durations of 20 ns or less. Prolonged operation at V_{IL} levels below −1 V will result in excessive currents that may damage the device input.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	'69CE72-25			'69CE72-35			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	−10		10	μA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−10		10	−10		10	μA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			130			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}1 \geq V_{IH}$, V_{CC} = 5.5 V			10			10	mA
		CMOS-level inputs	$\overline{E}1 = V_{CC} \pm 0.3$, V_{CC} = 5.5 V			0.9			0.9	

PARAMETER			TEST CONDITIONS	'69CE72-45			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	μA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−10		10	μA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}1 \geq V_{IH}$, V_{CC} = 5.5 V			10	mA
		CMOS-level inputs	$\overline{E}1 = V_{CC} \pm 0.3$, V_{CC} = 5.5 V			0.9	

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capacitance, T_A = 25°C, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5 V			5	pF
C_o	Output capacitance				7	

†Capacitance measurements are made on sample basis only.

timing requirements over recommended supply voltage range and operating temperature range

		'69CE72-25			'69CE72-35			'69CE72-45			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(rd)}$	Read cycle time	25			35			45			ns
$t_{c(wr)}$	Write cycle time	25			35			45			ns
$t_{w(W)}$	Write-enable pulse duration	15			20			25			ns
$t_{su(E1)}$	Chip-enable 1 low to end of write	20			30			40			ns
$t_{su(E2)}$	Chip-enable 2 high to end of write	15			20			25			ns
$t_{su(A)}$	Address setup time to write start	0			0			0			ns
$t_{su(D)}$	Data setup time to write end	10			15			20			ns
$t_{h(A)}$	Address hold time from write end	0			0			0			ns
$t_{h(D)}$	Data hold time from write end	0			0			0			ns
t_{PU}	Delay time, chip-enable $\overline{E}1$ low to power up‡	0			0			0			ns
t_{PD}	Delay time, chip-enable $\overline{E}1$ high to power down ‡			20			20			25	ns
t_{AW}	Address setup to write end	25			30			40			ns

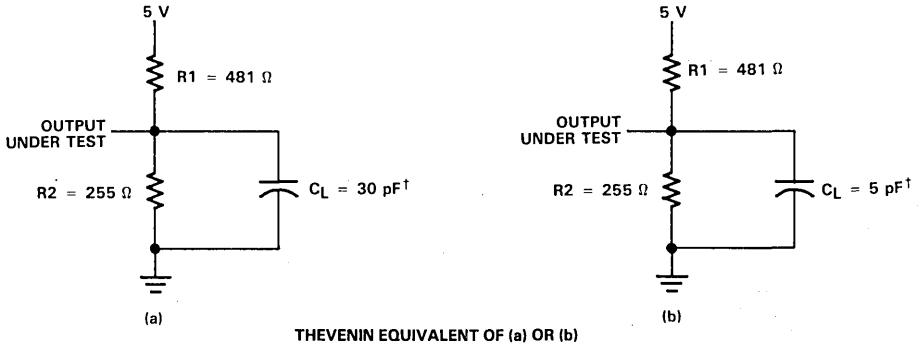
switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS	'69CE72-25	'69CE72-35	'69CE72-45	UNIT
			MIN MAX	MIN MAX	MIN MAX	
$t_{a(A)}$	Access time from address	R1 = 481 Ω, R2 = 255 Ω, C_L = 30 pF, See Figure 1a	25	35	45	ns
$t_{a(E1)}$	Access time from chip enable $\overline{E}1$ low		25	35	45	ns
$t_{a(E2)}$	Access time from chip enable E2 high		20	25	30	
$t_{a(G)}$	Access time from output enable low		15	20	20	ns
$t_{v(A)}$	Output data valid after address change		3	3	3	
$t_{en(W)}$	Output enable time from write enable high	R1 = 481, R2 = 255 Ω, C_L = 5 pF, See Figure 1b and Note 4	0	0	3	ns
$t_{en(E1)}$	Output enable time from chip enable $\overline{E}1$ low		0	0	3	ns
$t_{en(E2)}$	Output enable time from chip enable E2 high		0	0	3	ns
$t_{en(G)}$	Output enable time from output enable low		0	0	0	ns
$t_{dis(E1)}$	Output disable time from chip enable $\overline{E}1$ high		15	15	20	ns
$t_{dis(E2)}$	Output disable time from chip enable E2 low		15	15	20	ns
$t_{dis(W)}$	Output disable time from write enable low		10	15	20	ns
$t_{dis(G)}$	Output disable time from output enable high		10	15	20	ns

‡This parameter is guaranteed but not tested.

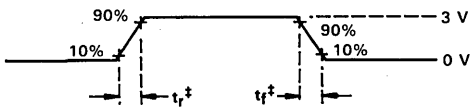
NOTE 4: Transition is measured ±500 mV from steady state voltage. This parameter is guaranteed but not tested.

PARAMETER MEASUREMENT INFORMATION



†C_L includes jig and scope capacitances.

FIGURE 1. OUTPUT LOAD CIRCUIT

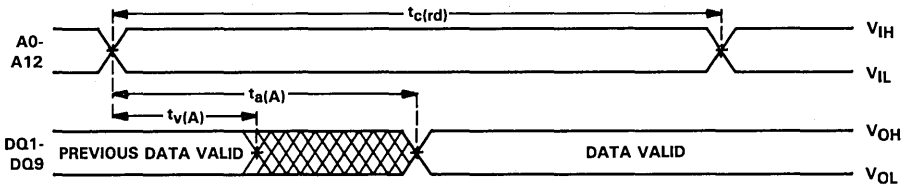


‡t_r and $t_f \leq 5$ ns.

FIGURE 2. TRANSITION TIMES

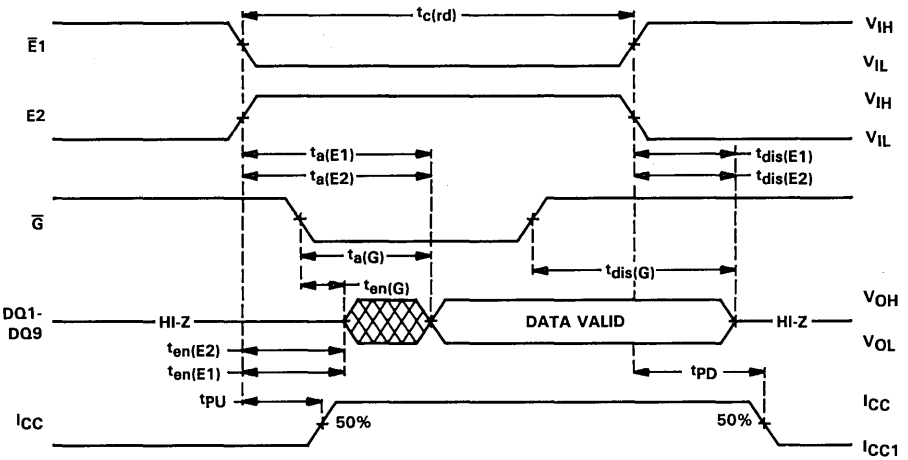
NOTE 5: All switching characteristics and timing requirements assume test conditions as depicted in Figures 1 and 2 with timing references of 1.5 V (50% reference point) as shown in subsequent timing diagrams.

ead cycle timing from address†



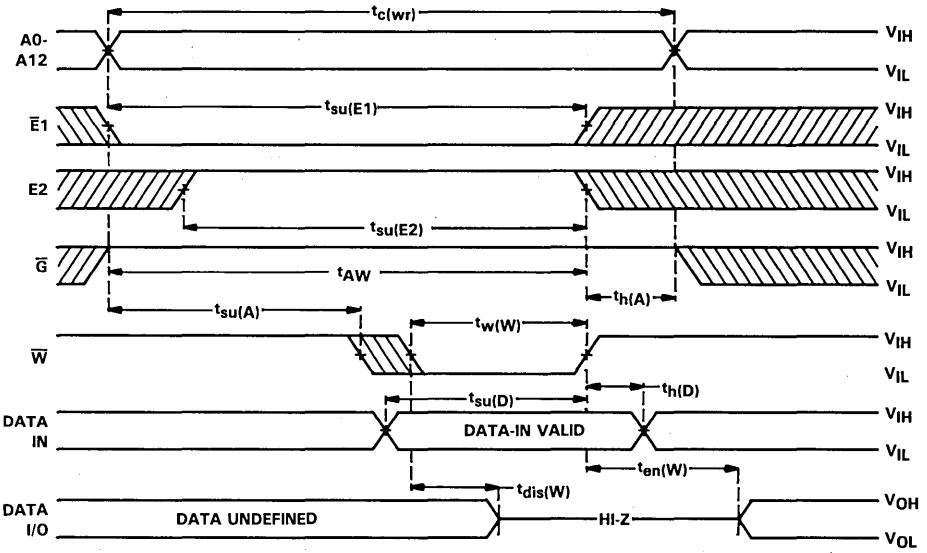
$\overline{W}$ is high, and $\overline{E}$ is low.

ead cycle timing from chip enable‡



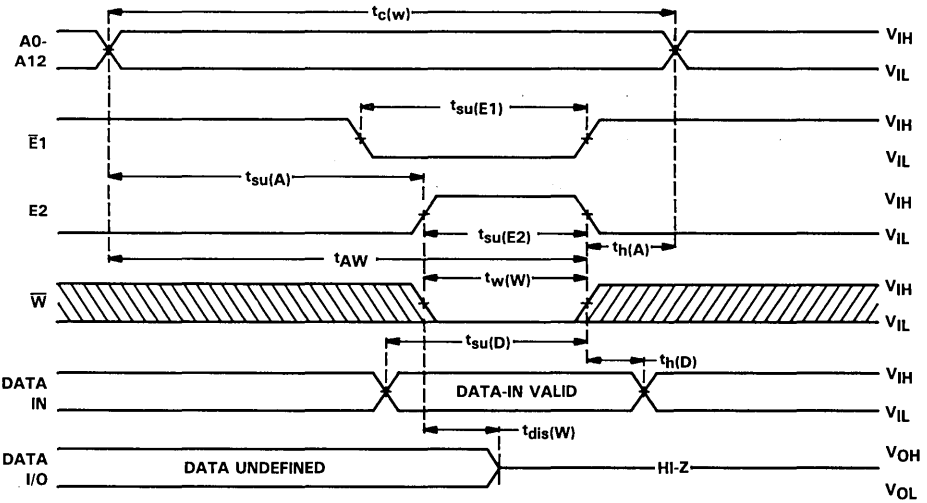
‡$\overline{W}$ is high, address is valid prior to or simultaneously with the high-to-low transition of $\overline{E}$.

write cycle timing controlled by write enable†



†$\overline{E}$ or $\overline{W}$ must be high during address transitions.

write cycle timing controlled by chip enable†

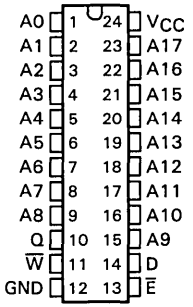


†$\overline{E}$ or $\overline{W}$ must be high during address transitions.

DECEMBER 1987—REVISED FEBRUARY 1988

- 262,144 × 1 Organization
- Separate I/O
- Military Temperature Range . . . −55°C to 125°C (M Suffix)
- Fast Static Operation
- Maximum Access Time from Address or Chip Enable
  '61CD256-35 . . . 35 ns
  '61CD256-45 . . . 45 ns
  '61CD256-55 . . . 55 ns
- Single 5-V Supply (10% Tolerance)
- Automatic Powerdown when Deselected
- 3-State Output
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- Low Power Dissipation (V_{CC} = 5.5 V)
  —Active . . . 660 mW MAX
  —Standby . . . 27.5 mW MAX (TTL Inputs)
  —Standby . . .1.1 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  —SM Prefix . . . Standard Processing
  —SMJ Prefix . . . Class B Processing
- Packaging Options:
  —24-Pin Ceramic 300-mil DIP
  —28-Pad Leadless Ceramic Chip Carrier
- Chip Enable Pin for Memory Expansion and Standby Operation

JD PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A17	Address Inputs
D	Data Input
Q	Data Output
$\overline{E}$	Chip Enable/Power Down
GND	Ground
V_{CC}	5-V Supply
$\overline{W}$	Write Enable

description

The '61CD256 is a separate I/O, 262,144-bit static random-access memory organized as 262,144 words by 1 bit. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six-transistor cell) memory array. The six-transistor cell provides inherently lower soft error rates, improved stability over the operating temperature range, and very low standby power compared to the four-transistor/two-poly load cell, making it ideal for military applications.

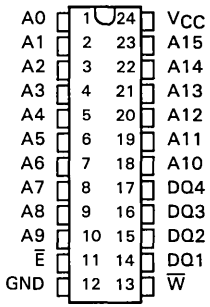
The '61CD256's static design and control signals ($\overline{E}$ and $\overline{W}$) remove the need for refresh circuitry and simplify timing requirements. The chip-enable pin provides for easy memory expansion and for automatic power-down. This feature, in conjunction with the full CMOS array, provides for very low standby power operation when the memory is deselected, greatly reducing the overall memory power requirements.

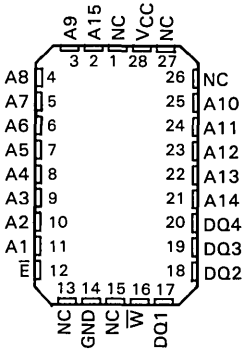
Access time from either address or chip enable is a maximum of 35, 45, or 55 ns, allowing speed enhancements for new and existing designs.

JANUARY 1988

- 65,536 × 4 Organization
- Common I/O
- Military Temperature Range . . . −55°C to 125°C (M Suffix)
- Fast Static Operation
- Maximum Access Time from Address or Chip Enable
  '64C256-35 . . . 35 ns
  '64C256-45 . . . 45 ns
  '64C256-55 . . . 55 ns
- Single 5-V Supply (10% Tolerance)
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- Low Power Dissipation (V_{CC} = 5.5 V)
  —Active . . . 660 mW MAX
  —Standby . . . 27.5 mW MAX (TTL Inputs)
  —Standby . . . 1.1 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  —SM Prefix . . . Standard Processing
  —SMJ Prefix . . . Class B
- Chip Enable Pin for Memory Expansion and Standby Operation
- Packaging Options:
  —24-Pin Ceramic 300-mil DIP
  —28-Pad Leadless Ceramic Chip Carrier

JD PACKAGE
(TOP VIEW)





description

The '64C256 is a common I/O, 262,144-bit static random-access memory organized as 65,536 words by 4 bits. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six-transistor cell) memory array. The six-transistor cell provides for inherently lower soft error rates, improved stability over the operating temperature range, and very low standby power compared to the four-transistor/two-poly load cell, making it ideal for military applications.

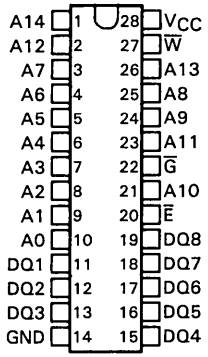
PIN NOMENCLATURE	
A0-A15	Address Inputs
DQ1-DQ4	Data In/Data Out
$\overline{E}$	Chip Enable/Power Down
GND	Ground
V_{CC}	5-V Supply
$\overline{W}$	Write Enable

The '64C256's static design and control signals ($\overline{E}$ and $\overline{W}$) remove the need for refresh circuitry and simplify timing requirements. The chip-enable pin provides for simplified memory expansion/design and for automatic powerdown. Access time from either address or chip enable is a maximum of 35, 45, or 55 ns.

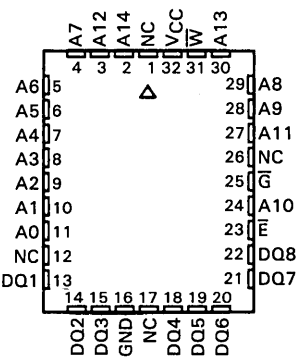
JULY 1987—REVISED NOVEMBER 1987

- 32,768 × 8 Organization
- Common I/O
- Military Temperature Range . . . −55°C to 125°C (M Suffix)
- Fast Static Operation
- Maximum Access Time from Address or Chip Enable
  '68CE256-35 . . . 35 ns
  '68CE256-45 . . . 45 ns
  '68CE256-55 . . . 55 ns
- Single 5-V Supply (10% Tolerance)
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- Low Power Dissipation (V_{CC} = 5.5 V)
  — Active . . .660 mW MAX
  — Standby . . . 27.5 mW MAX (TTL Inputs)
  — Standby . . . 1.1 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  — SM Prefix . . . Standard Processing
  — SMJ Prefix . . . Class B
- Output Enable for Simplified Bus Control
- Chip Enable Pin for Memory Expansion and Standby Operation
- Packaging Options:
  — 28-Pin Ceramic 400-mil DIP
  — 28-Pin Ceramic 600-mil DIP
  — 32-Pad Leadless Ceramic Chip Carrier

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A14	Address Inputs
DQ1-DQ8	Data In/Data Out
$\overline{E}$	Chip Enable/Power Down
GND	Ground
V_{CC}	5-V Supply
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable

description

The '68CE256 is a common I/O, 262,144-bit static random-access memory organized as 32,768 words by 8 bits. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six transistor cell) memory array. The six transistor cell provides for inherently lower soft error rates, improved stability over the operating temperature range, and very low standby power compared to the four-transistor/two-poly load cell, making it ideal for military applications.

The '68CE256's static design and control signals ($\overline{E}$, $\overline{G}$, and $\overline{W}$) remove the need for refresh circuitry and simplify timing requirements. The chip-enable pin provides for simplified memory expansion/design and for automatic powerdown. Access time from either address or chip enable is a maximum of 35, 45, or 55 ns. The output enable-pin minimizes bus contention problems.

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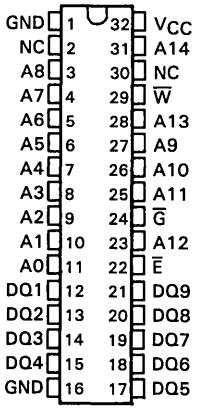
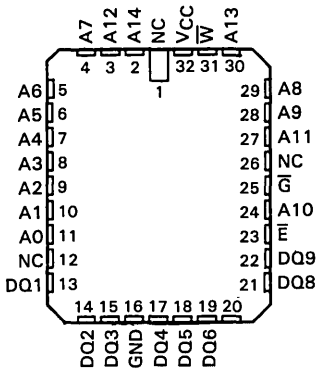
JULY 1987—REVISED FEBRUARY 1988

- 32,768 × 9 Organization
- Common I/O
- Military Temperature Range . . . −55°C to 125°C (M Suffix)
- Fast Static Operation
- Maximum Access Time from Address or Chip Enable
  '69CE288-35 . . . 35 ns
  '69CE288-45 . . . 45 ns
  '69CE288-55 . . . 55 ns
- Single 5-V Supply (10% Tolerance)
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- Low Power Dissipation (V_{CC} = 5.5 V)
  — Active . . . 660 mW MAX
  — Standby . . . 27.5 mW MAX (TTL Inputs)
  — Standby . . . 1.1 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  — SM Prefix . . . Standard Processing
  — SMJ Prefix . . . Class B
- Output Enable for Simplified Bus Control
- Chip Enable Pin for Memory Expansion and Standby Operation
- Packaging Options:
  — 32-Pin Ceramic 400-mil DIP
  — 32-Pad Leadless Ceramic Chip Carrier

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A14	Address Inputs
DQ1-DQ9	Data In/Data Out
$\overline{E}$	Chip Enable/Power Down
GND	Ground
V_{CC}	5-V Supply
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
NC	No Connection

description

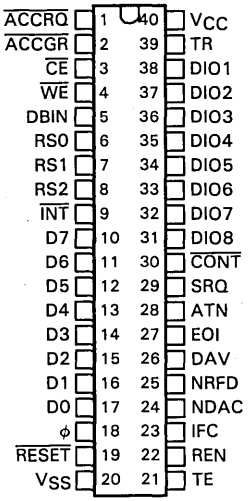
The '69CE288 is a common I/O, 294,912-bit static random-access memory organized as 32,768 words by 9 bits. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six-transistor cell) memory array. The six-transistor cell provides for inherently lower soft error rates, improved stability over the operating temperature range, and very low standby power compared to the four-transistor/two-poly load cell, making it ideal for military applications.

The '69CE288's static design and control signals ($\overline{E}$, $\overline{G}$, and $\overline{W}$) remove the need for refresh circuitry and simplify timing requirements. The chip-enable pin provides for simplified memory expansion/design and for automatic powerdown. Access time from either address or chip enable is a maximum of 35, 45, or 55 ns. The output enable-pin minimizes bus contention problems.

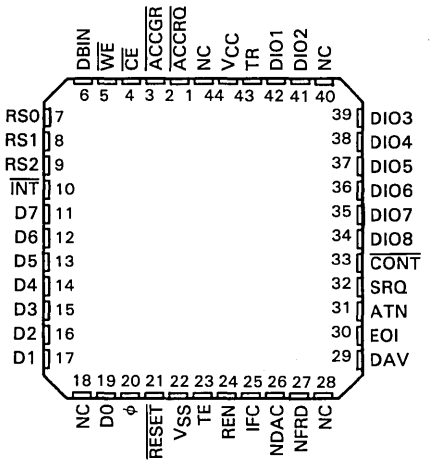
JUNE 1986 – REVISED MARCH 1988

- Handles All IEEE-488 1975/78 Functions
- Compatible with IEEE-488A 1980 Supplement
- Maximum Transfer Rate . . . Greater Than 360 Kilobytes/Second
- Talker and Listener Function (T, TE, L, LE)
- Automatic Source and Acceptor Handshakes (SH, AH)
- Controller with Pass Control
- System Controller Capabilities
- Device Trigger and Device Clear Capabilities (DT, DC)
- Optional Automatically Cleared 'Request Service Bit'
- Parallel and Serial Poll Facilities (PP)
- Remote/Local Function with Local Lockout (RL)
- Single or Dual Primary Addressing
- Secondary Address Capabilities
- Direct Interface to SN75160/161/162 Bus Transceivers with No Additional Logic
- Compatible with Most Microprocessors
- Direct-Memory-Access Facilities
- Memory-Mapped Microprocessor Interface
- Temperature Range . . . −55°C to 110°C (S Suffix)

JD PACKAGE
(TOP VIEW)



FD PACKAGE
(TOP VIEW)



description

The SMJ9914A provides an interface between a Microprocessor System and the General Purpose Interface Bus (GPIB) specified in the IEEE-488 1975/78 standards and the IEEE-488A 1980 supplement. The device is controlled and configured through 8-bit memory-mapped registers and enables all aspects of the standards to be implemented, including talker, listener and controller. The functional block diagram is shown on page 3.

The GPIB is designed to allow up to 15 instruments within a localized area to communicate with each other over a common bus. Each device has a unique address, read from external switches at power-on, to which it responds. Information is transmitted by byte-serial bit-parallel format and may consist of either device-dependent data or interface messages, commonly referred to as data or command, respectively. A typical application is shown in Figure 1. Auxiliary commands are listed in Table 1.

Device data may be sent by any one device (the talker) and received by a number of other devices (listeners). Instructions, such as select range, select function, or measurement data for processing or printout, may be sent in this way.

The SMJ9914A performs the interface function between the microprocessor and GPIB bus and relieves the processor of the task of maintaining the IEEE protocol. By utilizing the interrupt capabilities of the device, the bus does not have to be continually polled, and fast responses to changes in the interface configuration can be achieved.

The GPIB input/output pins are connected to the IEEE-488 bus via bus tranceivers. The direction of data flow is controlled by the TE and $\overline{\text{CONT}}$ outputs generated on the SMJ9914A. The SN75160, 75161 and 75162 bus transceivers are designed specifically for use with a GPIB interface. The TE and $\overline{\text{CONT}}$ signals are routed within the devices so that the buffers on particular lines are controlled as required by the SMJ9914A. Other buffers may be used, but they may require a small amount of external logic, particularly around the EOI line buffer.

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functional block diagram

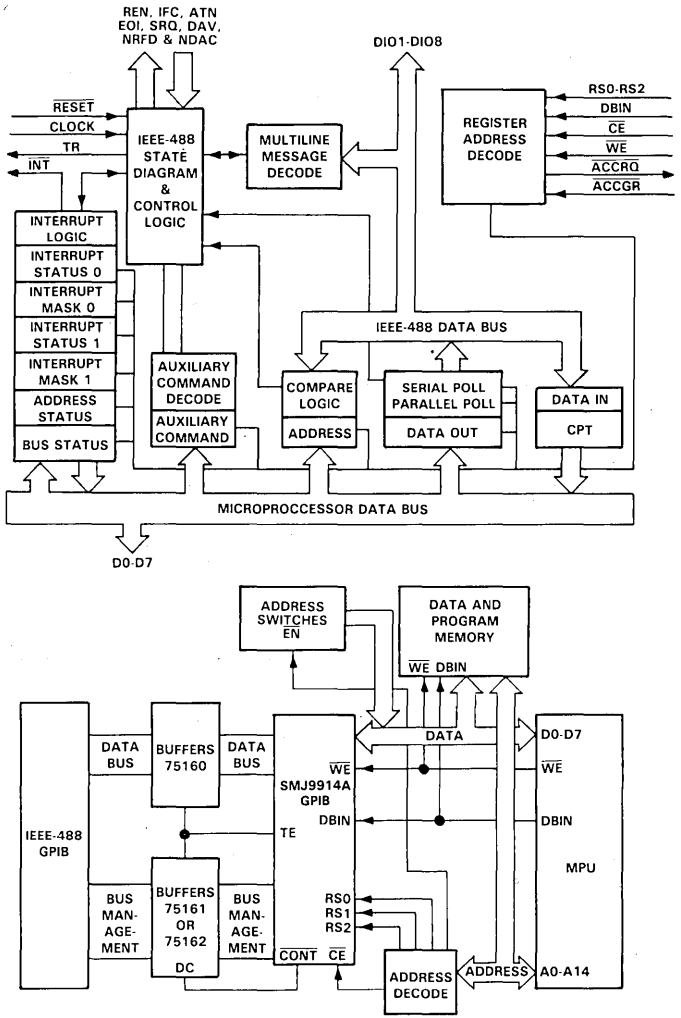

FIGURE 1. TYPICAL SMJ9914A APPLICATION

pin descriptions

PIN NO.	PIN NAME	I/O (TYPE)	DESCRIPTION
1	$\overline{\text{ACCRQ}}$	O†	Access Request. This pin becomes active (low) to request a direct memory access.
2	$\overline{\text{ACCGR}}$	I	Access Granted. When received from the direct-memory-access control logic, this enables the byte onto the data bus. $\overline{\text{ACCGR}}$ must be high when not participating in DMA transfer.
3	$\overline{\text{CE}}$	I	Chip Enable. $\overline{\text{CE}}$ allows access of read and write registers. If $\overline{\text{CE}}$ is high, D0-D7 are in high impedance unless $\overline{\text{ACCGR}}$ is low.
4	$\overline{\text{WE}}$	I	Write Enable. When active (low), indicates to the SMJ9914A that data is being written to one of its registers.
5	DBIN	I	Data Bus In. An active (high) state indicates to the SMJ9914A that a read is about to be carried out by the MPU.
6 7 8	RS0 RS1 RS2	I I I	Register Select Lines. Determine which register is addressed by the MPU during a read or write operation.
9	$\overline{\text{INT}}$	O‡	Interrupt. Sent to the MPU to cause a branch to a service routine.
17-10	D0-D7	I/O†	Data transfer lines on the MPU side of the device. D0 is the most-significant bit.
18	ϕ	I	Clock Input. 500 kHz to 5 MHz. Need not be synchronous to system clock.
19	$\overline{\text{RESET}}$§	I	Initializes the SMJ9914A at power-on.
20	V_{SS}		Ground reference voltage.
21	TE	O†	Talk Enable. Controls the direction of the transfer of the line transceivers. Logically, it is: [CACS + TACS + EIO.ATN.(CIDS + CADS) $\overline{\text{SWRST}}$].
22	REN	I/O¶	Remote Enable. Sent by system controller to select control either from the front panel or from the IEEE bus.
23	IFC	I/O¶	Interface Clear. Sent by the system controller to set the interface system into a known quiescent state. The system controller becomes the controller in charge.
24	NDAC	I/O†	Not Data Accepted. Handshake line. Acceptor sets this false (high) when it has latched the data from the I/O lines.
25	NRFD	I/O†	Not Ready For Data. Handshake line. Sent by acceptor to indicate readiness for the next byte.
26	DAV	I/O†	Data Valid. Handshake line controlled by source to show acceptors when valid data is present to the bus.
27	EOI	I/O†	End Or Identify. If $\overline{\text{ATN}}$ is false (high), this indicates the end of a message block. If $\overline{\text{ATN}}$ is true (low), the controller is requesting a parallel poll.
28	ATN	I/O†	Attention. Sent by controller in charge. When true (low), interface commands are being sent over the DIO lines. When false (high), these lines carry data.
29	SRQ	I/O†	Service Request. Set true (low) by a device to indicate a need for service.
30	$\overline{\text{CONT}}$	O†	Indicates (low) if a device is controller in charge. It is used to control direction of SRQ and ATN in pass control systems. Logically, it is (CIDS + CADS).
31-38	DIO8-DIO1	I/O†	DIO8 through DIO1 are the data input/output lines on the GPIB side. These pins connect to the IEEE-488 bus via non-inverting transceivers.
39	TR	O†	Trigger. Activated when the GET command is received over the interface or the fget command is given by the MPU.
40	V_{CC}		Supply voltage (5 V nominal).

†Push-pull output
‡Open-drain output with no internal pullup
§The hardware RESET pin has the following effect on the SMJ9914A:
—Serial and Parallel Poll registers cleared
—All clear/set auxiliary commands cleared except 'swrst'
—'swrst' auxiliary command set. This holds the SMJ9914A in known states.
¶Open-drain output with internal pullup

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Communication between the microprocessor and SMJ9914A is carried out via memory-mapped registers. There are 13 registers within the SMJ9914A, 6 of which are read and 7 are write. These registers both pass control data to and get status information from the device. These registers are listed in Table 2 and shown in Figure 2.

The three least-significant address lines from the MPU are connected to register select lines RS0, RS1, and RS2 and determine the particular register selected. The high-order address lines are decoded by external logic to cause the $\overline{CE}$ input to the SMJ9914A to be pulled low when any one of eight consecutive addresses are selected. Thus the internal registers appear to be situated at eight consecutive locations within the MPU address space. Reading or writing to these locations transfers information between the SMJ9914A and the microprocessor. Note that reading and writing to the same location will not access the same register within the SMJ9914A since they are either read-only or write-only registers. For example, a read operation with RS2-RS0 = 011 gives the current status of the GPIB interface control lines, whereas a write to this location loads the auxiliary-command register.

Each device on the bus interface is given a 5-bit address enabling it to be addressed as a talker or listener. This address is set on an external DIP switch (usually at the rear of an instrument) before power-on.

Typical SMJ9914A configuration utilizes registers 100 or 101 as an address switch register (see Table 2.). This register may consist of a DIP switch which drives the data lines via 3-state buffers when one of these addresses is read. This allows the host MPU to read a device address which is manually set and write this address into the address register of the SMJ9914A for device identification on the bus. The SMJ9914A responds by causing a My Address (MA) interrupt and entering the required addressed state when this address is detected on the GPIB data lines.

TABLE 1. AUXILIARY COMMANDS

MNEMONIC	DESCRIPTION	CLEAR	SET	C/S NA CODE
dacr	Release DAC holdoff	01	81	
dai	Disable all interrupts	13	93	
feoi	Send EOI with next byte			08
fget	Force group execute trigger	06	86	
gts	Go to standby			0B
hdfa	Holdoff on all data	03	83	
hdfe	Holdoff on EOI only	04	84	
lon	Listen only	09	89	
nbaf	New byte available false			05
pts	Pass through next secondary			14
rhdf	Release RFD holdoff			02
rlc	Release control			12
rpp	Request parallel poll	0E	8E	
rqc	Request control			11
rsv2	Request service bit 2	18	98	
rtl	Return to local	07	87	
shdw	Shadow handshake	16	96	
sic	Send interface clear	0F	8F	
sre	Send remote enable	10	90	
std1	Short T1 settling time	15	95	
tca	Take control asynchronously			0C
tcs	Take control synchronously			0D
ton	Talk only	0A	8A	
vstd1	Very short T1 delay	17	97	

TABLE 2. REGISTER ADDRESSES

ADDRESS RS2	RS1	RS0	READ REGISTERS	WRITE REGISTERS
0	0	0	Interrupt Status 0	Interrupt Mask 0
0	0	1	Interrupt Status 1	Interrupt Mask 1
0	1	0	Address Status	‡
0	1	1	Bus Status	Auxiliary Command
1	0	0	†	Address
1	0	1	†	Serial Poll
1	1	0	Command Pass Thru	Parallel Poll
1	1	1	Data In	Data Out

†The SMJ9914A host interface data lines will remain in the high-impedance state when these register locations are addressed. An Address Switch Register may therefore be included in the address space of the device at these locations.

‡This address is not decoded by the SMJ9914A. A write to this location will have no effect on the device, as if a write had not occurred.

reference documentation

- TMS9914A GPIB Controller User's Guide (SPPU013)
- TMS9914A General Purpose Interface Bus (GPIB) Controller Data Manual (MP033A)

DATA-IN REGISTER										
ADDRESS			BIT ASSIGNMENT							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
1	1	1	DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01

GPIB

DATA-OUT REGISTER										
ADDRESS			BIT ASSIGNMENT							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
1	1	1	DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01

GPIB

AUXILIARY-COMMAND REGISTER										
ADDRESS			BIT ASSIGNMENT							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
0	1	1	cs	xx	xx	f4	f3	f2	f1	f0

cs Clear or Set
f4-f0 Auxiliary command select

INTERRUPT MASK/STATUS REGISTER 0											
ADDRESS			BIT ASSIGNMENT								
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7	
0	0	0	xx	xx	BI	BO	END	SPAS	RLC	MAC	INT MASK 0
0	0	0	INT0	INT1	BI	BO	END	SPAS	RLC	MAC	INT STAT0

INT1 Interrupt Status Register 1
INT0 Interrupt Status Register 0
BI Byte In
BO Byte Out
END Last byte in string received
SPAS Device has been serial polled
RLC Remote/Local Change
MAC My Address Change

INTERRUPT MASK/STATUS REGISTER 1											
ADDRESS			BIT ASSIGNMENT								
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7	
0	0	1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC	INT MASK 1
0	0	1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC	INT STAT 1

GET Group Execute Trigger
ERR Error
UNC Unrecognized Command
APT Address Pass Through
DCAS Device Clear Active State
SRQ Service Request
MA My Address
IFC Interface Clear

ADDRESS STATUS REGISTER										
ADDRESS			BIT ASSIGNMENT							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
0	1	0	REM	LLO	ATN	LPAS	TPAS	LADS	TADS	ulpa

REM Remote State
LLO Local Lockout
ATN Attention
LPAS Listener Primary Addressed State
TPAS Talker Primary Addressed Stat
LADS Addressed to listen
TADS Addressed to talk
ulpa LSB last address

ADDRESS REGISTER										
ADDRESS			BIT ASSIGNMENT							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
1	0	0	edpa	dal	dat	A5	A4	A3	A2	A1

edpa Enable dual-primary addressing mode
das Disable listener function
dat Disable talker function
A5-A1 Primary address

BUS STATUS REGISTER										
ADDRESS			BIT ASSIGNMENT							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
0	1	1	ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN

SERIAL POLL REGISTER										
ADDRESS			BIT ASSIGNMENT							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
1	0	1	S8	rsv1	S6	S5	S4	S3	S2	S1
			DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01

GPIB

S8,S6-S1 Device Status
rsv1 Request Service bit 1

COMMAND PASS THROUGH REGISTER										
ADDRESS			BIT ASSIGNMENT							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
1	1	0	DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01

GPIB

PARALLEL POLL REGISTER										
ADDRESS			BIT ASSIGNMENT							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
1	1	0	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1
			DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01

GPIB

FIGURE 2. INTERNAL REGISTERS

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absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Supply voltage range V_{CC}‡ . . . . . −0.3 V to 20 V
All input and output voltage ranges . . . . . −0.3 V to 20 V
Continuous power dissipation . . . . . 1.0 W
Operating case temperature range . . . . . −55°C to 110°C
Storage temperature range . . . . . −55°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	All outputs except REN, IFC, $\overline{INT}$			−400	μA
		REN, IFC only			−100	μA
I_{OL}	Low-level output current				2	mA
T_C	Operating case temperature		−55		110	°C

electrical characteristics over full range of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All outputs except REN,IFC,$\overline{INT}$	I_{OH} = −400 μA	2.4			V
		REN, IFC only	I_{OH} = −100 μA	2.2			
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.4	V
I_I	Input current (any input)		V_{CC} = 5.25 V, V_I = V_{SS} to V_{CC}			±10	μA
I_{OZ}	Off-state output current		V_{CC} = 5.25 V, V_O = 2.4 V			20	μA
			V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
I_{CC}	V_{CC} supply current		V_{CC} = 5.25 V			200	mA
C_i	Input capacitance (any input)†		f = 1 MHz, all other pins at 0 V			15	pF

†Parameter guaranteed via characterization data.

clock and host interface timing requirements over full range of operating conditions

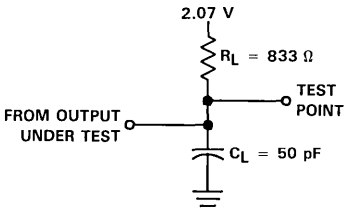
		MIN	NOM	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time	200		2000	ns
$t_{w(\phi H)}$	Clock high pulse duration			1955	ns
$t_{w(\phi L)}$	Clock low pulse duration	45			ns
$t_{su(AD)}$	Address setup time	0			ns
$t_{su(DBIN)}$	DBIN setup time†	0			ns
$t_{su(CE)}$	$\overline{CE}$ setup time	100			ns
$t_{su(WE)}$	$\overline{WE}$ setup time†	0			ns
$t_{w(WE)}$	$\overline{WE}$ low pulse duration	80			ns
$t_{su(DA)}$	Data setup time	80			ns
$t_{h(DA)}$	Data hold time	15			ns
$t_{h(AD)}$	Address hold time	0			ns
$t_{h(DBIN)}$	DBIN hold time†	0			ns
$t_{h(CE)}$	$\overline{CE}$ hold time	80			ns
$t_{su(GR)}$	$\overline{ACCGR}$ setup time	100			ns
$t_{h(GR)}$	$\overline{ACCGR}$ hold time	80			ns

†Parameter guaranteed via characterization data.

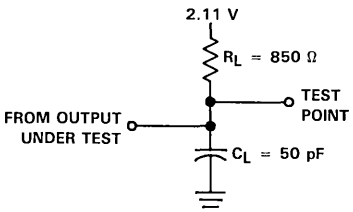
host interface timing characteristics over full range of operating conditions

	PARAMETER	MIN	NOM	MAX	UNIT
$t_{a(CE)}$	Access time from $\overline{CE}$			150	ns
$t_{a(DBIN)}$	Access time from DBIN low			150	ns
$t_{su(AD)}$	Address setup time to $\overline{CE}$	0			ns
$t_{d(DBINL-DZ)}$	DBIN low to data high impedance		50	100	ns
$t_{d(CEH-DZ)}$	$\overline{CE}$ high to data high impedance		50	100	ns
$t_{a(GR)}$	Access time from $\overline{ACCGR}$ low			150	ns
$t_{d(AGRH-DZ)}$	$\overline{ACCGR}$ high to data high impedance		50	100	ns
$t_{d(GRL-RQH)}$	Delay of $\overline{ACCRQ}$ high from $\overline{ACCGR}$ low			100	ns

PARAMETER MEASUREMENT INFORMATION



(a) ALL OUTPUTS EXCEPT REN AND IFC



(b) IFC AND REN

NOTE 1: Timing measurements are referenced to or from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. TEST LOAD CIRCUITS

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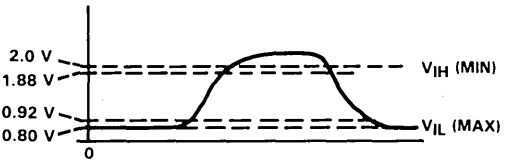
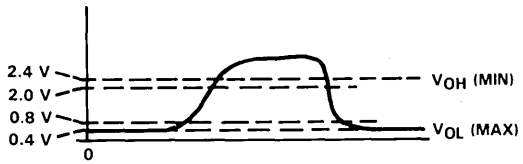


(a) INPUT



(b) OUTPUTS

FIGURE 4. VOLTAGE REFERENCE LEVELS

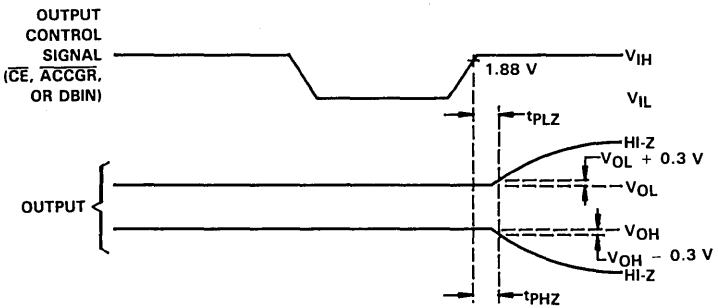
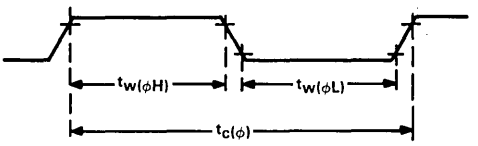
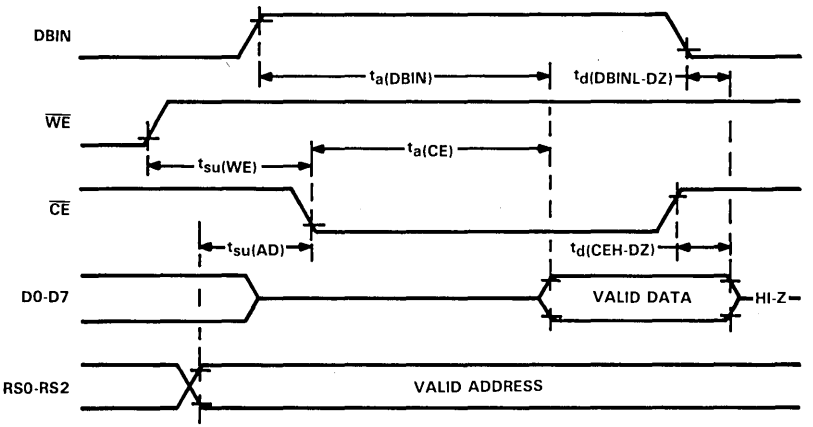


FIGURE 5. HIGH-IMPEDANCE MEASUREMENTS

clock cycle timing



read cycle timing



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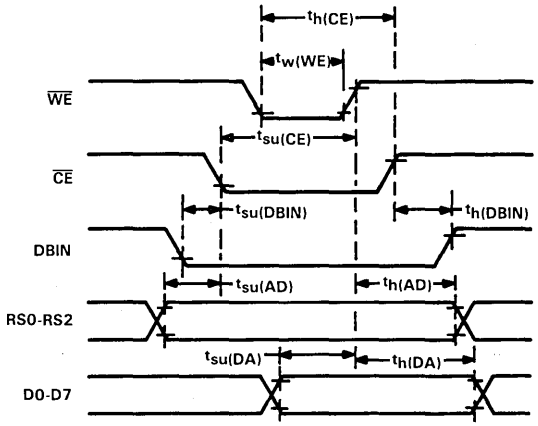
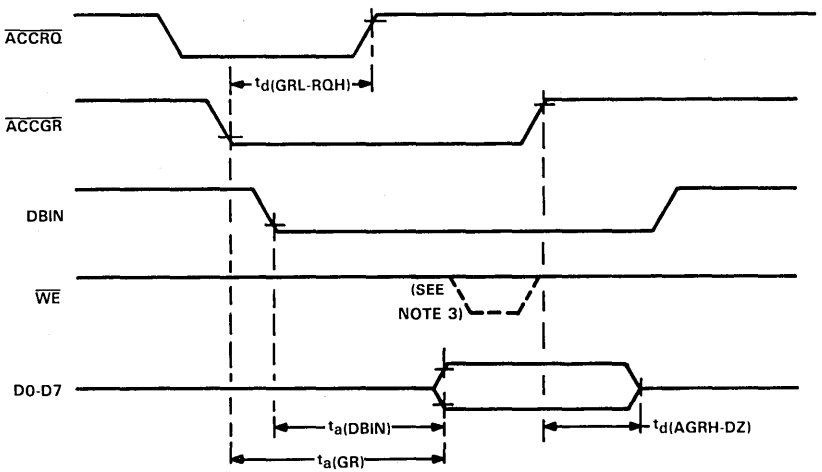
write cycle timing



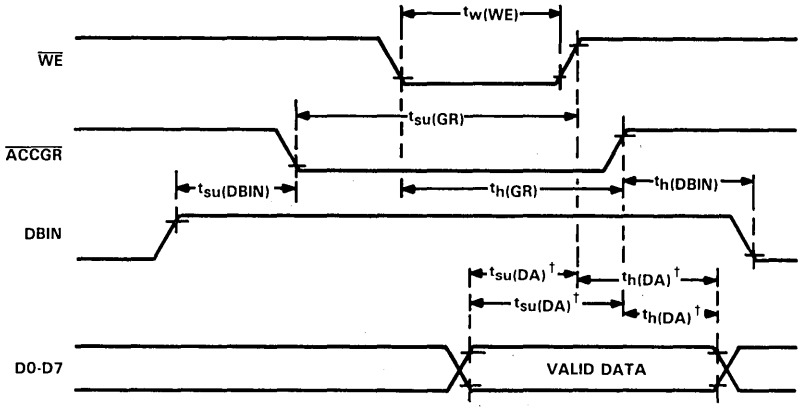
NOTE 2: $t_{h(AD)}$ and $t_{h(DA)}$ are shown measured from the rising edge of $\overline{WE}$. This is the correct reference point in this figure, since the measurements should be from the rising edge of $\overline{WE}$ or $\overline{CE}$ — whichever comes first.

DMA read operation



NOTE 3: A write-enable pulse may occur in a DMA read operation. A write-enable pulse may therefore be provided for system memory and need not be suppressed at the SMJ9914A.

DMA write operation



†$t_{su(DA)}$ and $t_{h(DA)}$ are only applicable to the first signal to become inactive, whether it is $\overline{WE}$ or $\overline{ACCGR}$.

source handshake timing characteristics over full range of operating conditions (see Note 4)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}	Delay of DAV true from end of write operation to data out register	Normal T_1 (see Note 5)	12(ϕ)†	12(ϕ)† + 310	ns
		Short T_1 (see Note 5)	8(ϕ)†	8(ϕ)† + 310	ns
		Very short T_1 (see Note 5)	4(ϕ)†	4(ϕ)† + 310	ns
t_{d2}	Delay of valid GPIB data lines from end of write cycle			140	ns
t_{d3}	Delay of BO interrupt from DAC true	BO interrupt unmasked		300	ns
t_{d4}	Delay of $\overline{ACCRQ}$ DAC true			300	ns
t_{d5}	Delay of DAV false from DAC true			160	ns

NOTES: 4. The timing of the source handshake is the same whether ATN is true or false; i.e., whether the device is in TACS, CACS, or SPAS.
5. A very short bus settling time (T_1) occurs on the second and subsequent data byte when ATN is false if the "vstd1" feature is set. A slightly longer bus settling time takes place if "std1" is set unless there is a very short bus settling time. In all other instances, a normal bus settling time occurs.

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acceptor handshake timing characteristics over full range of operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d6}	Delay of BI interrupt from DAV true	BI interrupt unmasked, ATN = false, device in LACS	2(ϕ)↑	2(ϕ)↑ + 415	ns
t_{d7}	Delay of $\overline{\text{ACCRQ}}$ from DAV true	ATN = false, device is in LACS	2(ϕ)↑	2(ϕ)↑ + 290	ns
t_{d8}	Delay of NDAC false from DAV true	ATN = false, device in LACS	3(ϕ)↑	3(ϕ)↑ + 445	ns
t_{d9}	Delay of NRFD false from end of read operation of Data-In register	ATN = false, device is in LACS		220	ns
t_{d10}	Delay of interface message interupt from DAV true	ATN = false, device not in CACS, all interface message interrupts (except UNC)	2(ϕ)↑	2(ϕ)↑ + 415	ns
		UNC interrupt only	5(ϕ)↑	5(ϕ)↑ + 415	ns
t_{d11}	Delay of NDAC false from DAV true	ATN = true, device not in CACS, no DAC holdoff	7(ϕ)↑	7(ϕ)↑ + 415	ns
t_{d12}	Delay of NDAC false from end of write operation			230	ns
t_{d13}	Delay of NRFD false from DAV false	ATN = true, device not in CACS		180	ns

NOTE 6: The interrupts generated by interface messages are shown in Table 3-15 of the TMS9914A General Purpose Interface Bus (GPIB) Controller Data Manual (MP033A).

ATN, EOI, and IFC timing characteristics over full range of operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d14}	Delay of NDAC true from ATN true	Device is not in CACS		195	ns
t_{d15}	Delay of TE high from EOI true	Device is not in CACS		125	ns
t_{d16}	Delay of valid data from EOI true	Device is not in CACS		140	ns
t_{d17}	Delay of TE low from EOI false	Device is not in CACS		125	ns
t_{d18}	Delay of NRFD true from ATN false	Device is in LADS/LACS		140	ns
t_{d19}	Response time to IFC		$16t_{c(0)}$	$30t_{c(0)}$	ns

controller timing characteristics over full range of operating conditions

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d20}	Delay of ATN true from end of tca auxiliary command		$8t_{c(0)}$	$10(\phi)\uparrow + 220$	ns
t_{d21}	Delay of BO interrupt from end of tca auxiliary command		$18t_{c(0)}$	$22(\phi)\uparrow + 415$	ns
t_{d22}	Delay of ATN true from end of tcs auxiliary command	BO unmasked, device is in ANRS	$8t_{c(0)}$	$10(\phi)\uparrow + 220$	ns
t_{d23}	Delay of BO interrupt from end of tcs auxiliary command	BO unmasked, device is in ANRS	$18t_{c(0)}$	$22(\phi)\uparrow + 415$	ns
t_{d24}	Delay of EOI true from rpp auxiliary command set			230	ns
t_{d25}	Delay of EOI false from rpp auxiliary command set			230	ns
t_{d26}	Delay of BO interrupt from rpp auxiliary command cleared	BO unmasked	$8t_{c(0)}$	$10(\phi)\uparrow + 415$	ns
t_{d27}	Delay of ATN false from gts auxiliary command	Device is not in SDYS or STRS		210	ns

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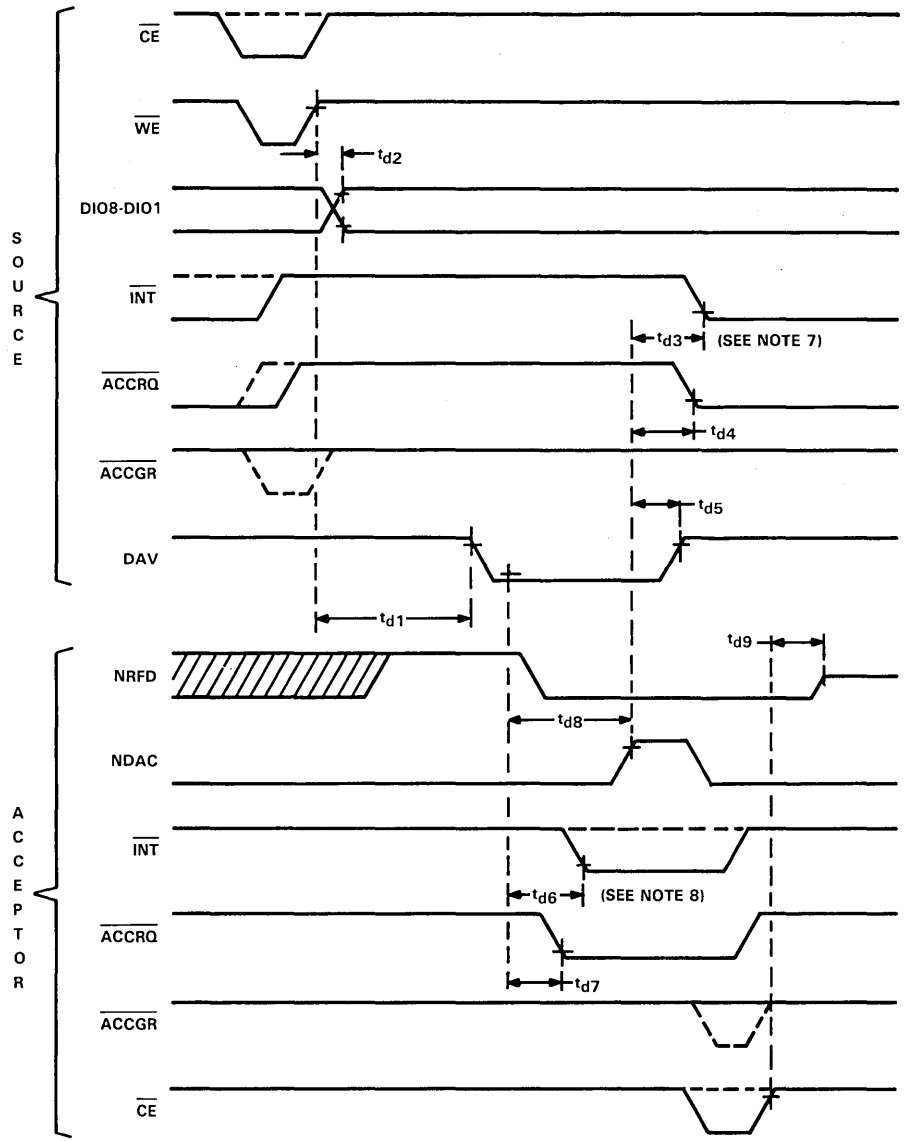
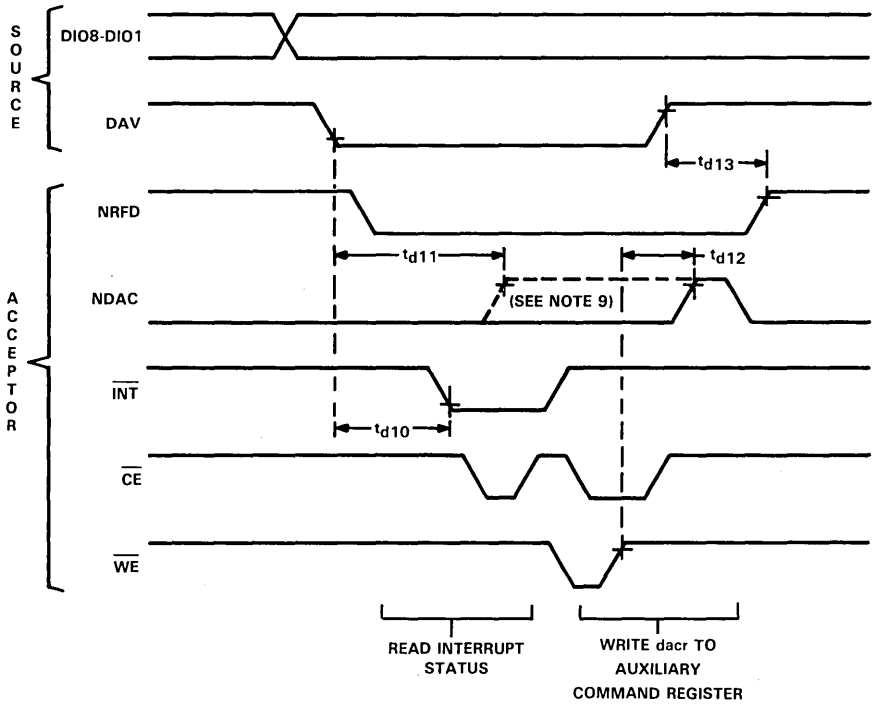
SMJ9914A source and acceptor handshake timing(s)



NOTES: 7. The interrupt line is taken low by a BO interrupt.
8. The interrupt line is taken low by a BI interrupt.

SMJ9914A acceptor handshake timing "ATN" true



NOTE 9: The broken line shows the waveform if there is no DAC holdoff. The solid lines assume there is a DAC holdoff.

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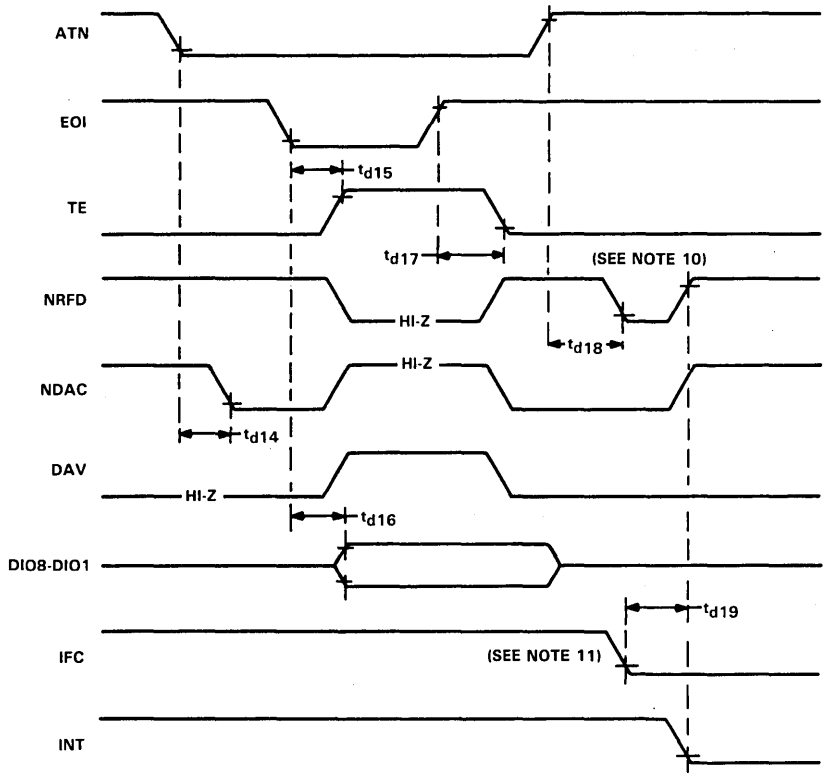
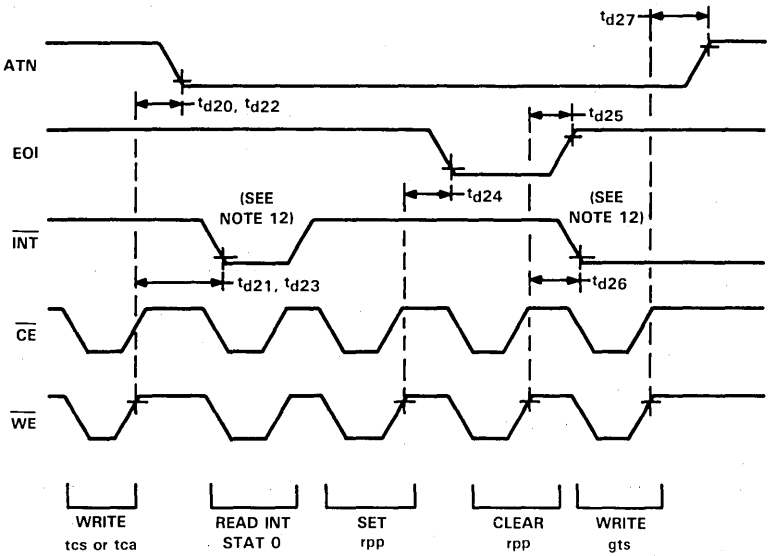
SMJ9914A response to 'ATN' and 'EOI'



NOTES: 10. This assumes that an RFD holdoff occurs.
11. IFC causes the SMJ9914A to be unaddressed and an IFC interrupt occurs.

SMJ9914A controller timing



NOTE 12: A BO interrupt occurs as the SMJ9914A enters CACS.

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Designing and Manufacturing Surface Mount Assemblies

Elizabeth Gunther, Charles Hutchins, and Paul Peterson

The competitive nature of the semiconductor industry has driven vendors to minimize the size of electronic components, so that more functions can be achieved in a given volume. In addition, improved electrical performance, decreased mass, and the potential for lower system cost are all by-products of compacted packaging and circuitry which hold interest to component manufacturers and users alike.

Surface Mount Technology (SMT) offers an excellent method of reducing component size. A typical memory array can be reduced to 50 percent of its original PWB size with single-sided mounting, and 25 to 30 percent with double-sided mounting. Logic designs cannot achieve the same dramatic reduction, but decreases up to 40 to 60 percent can be achieved for single-sided and double-sided assemblies respectively.

The key design and manufacturing process issues must be understood in order to fully reap the benefits of Surface Mount Technology. This article gives a general overview of the key aspects of design, process, and manufacturing of surface mounted assemblies, and offers surface mount as an opportunity to lower a system's cost without sacrificing reliability.

Components

Most surface mount components are at least one-third the size of the comparable through-hole mounted device (Figure 1). The 68-pin chip carrier is approxmiately one square inch, while the 64-pin DIP is approximately three square inches. The 20-pin chip carrier is slightly larger than 0.1 square inch, while the 20-pin DIP is 0.3 square inch. Similarly, other IC packages are reduced to approximately one-third the size of comparable lead count packages. The passive components occupy approximately one-tenth the board area, and this is why they have been used in most small consumer products built in the last couple of years.

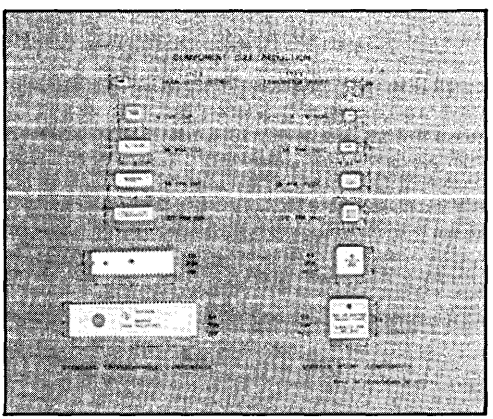


Figure 1. Component Site Reduction

There were many references in the recent past to problems with component availability, cost, and standardization. This area of SMT has probably received more attention than any other. Several recent magazine articles now state that significantly more components (particularly actives) are now available and that cost parity has been achieved on most of them. The effort by various industry committees on standardization has also been effective.

Thus, although more needs to be accomplished in these areas, a designer can begin a project with confidence that there will be no insurmountable barriers in this area. There are several consultants and subcontract assembly companies to assist in this effort. It is strongly recommended that all new designs utilize some form of SMT, particularly when space is an important consideration.

Process

The process to manufacture a surface mount assembly (SMA) is very simple. It consists of four basic steps, as shown in Figure 2. First, the solder paste is screened on the PWB. Then the component is placed on the board, with due care to get it positioned correctly. Typical geometries require placement accuracy of less than plus/minus 4 mils. Next the solder is reflowed with either a vapor phase or infrared system. Finally, the assembly is cleaned and is now ready for test. This process, although simple in concept, relies on board and component planarity and solderability. These are easily achievable with the chip carriers and memory modules we will discuss later.

Texas Instruments has installed a Surface Mount Technology Center at its plant in Houston, Texas. At this center, we have a complete and flexible engineering line to assist our customers in converting to Surface Mount Technology.

The engineering line is equipped with a screen printer, pick and place system, vapor phase reflow, and clean-up station that will easily handle PWBs up to 9″ × 10″. Larger boards up to 14″ × 16″ can be processed with some additional care. TI uses this engineering line to produce its prototype and demo boards. It is also available to any of TI's customers, free of charge, for use in building test or prototype boards.

The effectiveness of the assembly process can be characterized by the number of unacceptable solder joints formed during the process. Unacceptable joints are defined by their electrical and mechanical (strength and reliability) characteristics. The major problem is open solder joints, followed by bridging and misregistration.

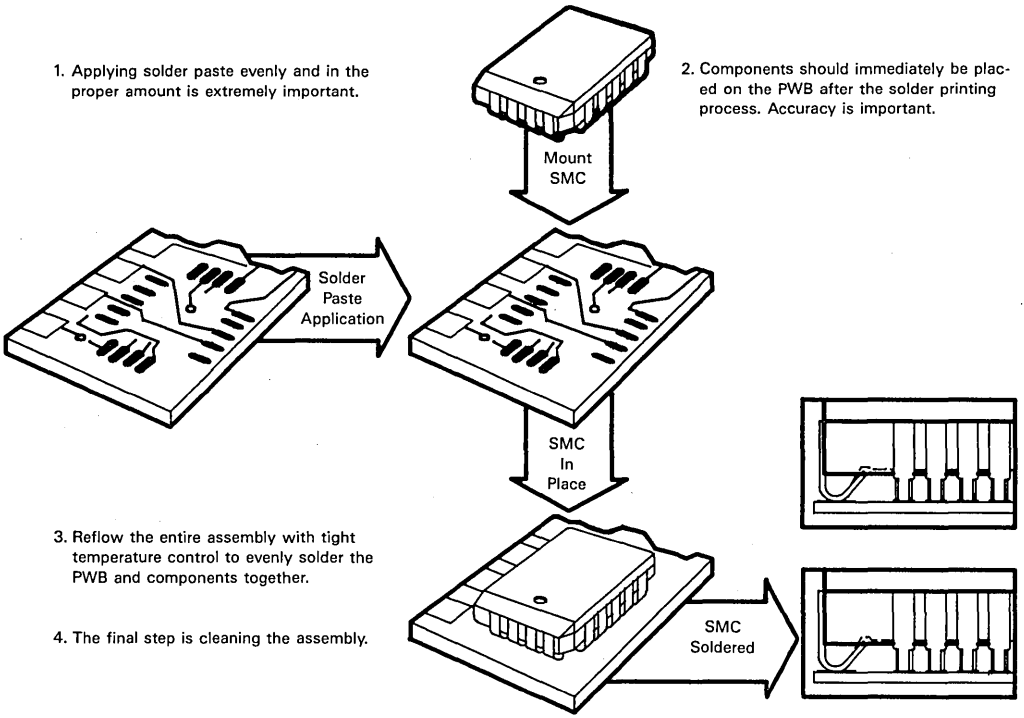


Figure 2. Basic Process Steps

Open circuits are detected at electrical test and are the first defects detected after soldering. At Texas Instruments, 10 PPM or less is the desirable defect level. Several factors that contribute to open solder joints were identified during production start-up. Lead tip planarity of the J-leaded plastic chip carriers is the most important factor in obtaining acceptable process yields. Lead position, lead finish, solder paste composition, and PWB solderability affect process yield as well.

Experiments in which lead tip planarity was confined to specific limits between 1 to 7 mils indicate that a 2 mil planarity requirement produces acceptable results with the process currently in use. Little gain in yield was noted at a 1 mil planarity requirement.

Another interesting result showed that silver in the process, either as a lead finish or in the solder paste, improves yields significantly. One explanation may have to do with the dynamics of the solder during the reflow process as they are affected by the different surface forces acting in the silver and non-silver process.

Design

The design of the PWB, in addition to providing the component interconnections, will provide the proper amount and correct placement of solder paste for a strong fillet formation. The wave soldering process, by comparison, provides a semi-infinite amount of solder, whereas the SMT process will provide only a predetermined amount. Thus, the component connection pad must be correctly placed and be of the proper size.

Further, consideration must be given for inspection, testing, and rework. The density achievable can lead to severe problems at these points if understanding and due care are not exercised in the design. The project team should include members from manufacturing, testing, QA, and purchasing, in addition to the design engineers, from the start. The design and processing of test boards is strongly recommended to provide experience and direction for the major project.

A very practical set of design guidelines is given in Figure 3. These have been used on a number of SMT designs and have given good results. With proper manufacturing techniques as described later, a high yield can be achieved. Component spacings should be approximately equal to the height of the tallest component. This allows an angle of 45 degrees for visual inspection of test probes.

Figure 4 shows the standard footprint for all Small Outline (SO) packages. The larger and more important fillet of an SO package is on the inside of the gull-wing lead. The solder pad, or land, should therefore be designed to extend slightly under the body of the package in order to optimize this fillet. From Table 1 we can see all packages have 50 mil centers with 25 mil spacings between lands. This allows the designer enough space to put traces between pads, and also reduces the occurrence of solder bridging of adjacent lands. Table 1 also summarizes the suggested land lengths and placement, depending on the terminal count of the SO. While not an absolute solution, these land sizes offer a conservative design solution that will meet most vendors' specifications and provide a mechanically and electrically sound solder joint.

- **Geometries**
  - **Trace Width/Space** — **8/8 MIL Min., 10/10 MIL Typ.**
  - **IC Lead Solder Pad Size** — **25 ± 5 MIL × 70 ± 10 MIL**
  - **Via Hole Size** — **20 MIL DIA**
  - **Via Pad Size** — **40 MIL DIA**
  - **Cap/Resistor Pad Size** — **W = MAX Dimensions of Component**
    L = 20 MIL Beyond Metallization
    10 MIL Inside Metallization
  - **Solder Mask** — **5 MIL Larger than IC/Component Pad**

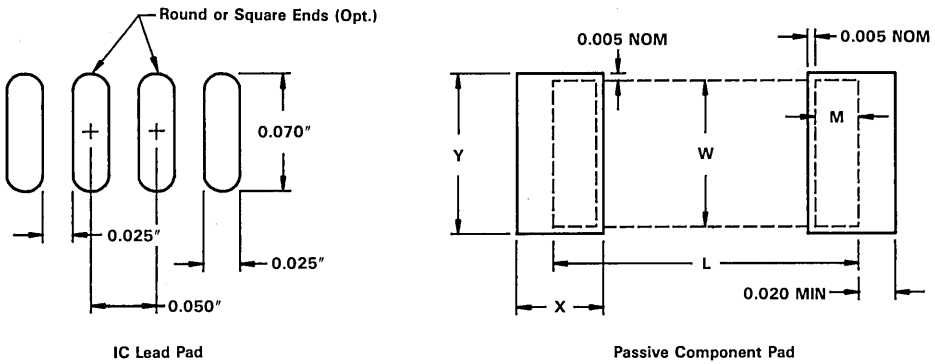


Figure 3. PWB Design Guidelines

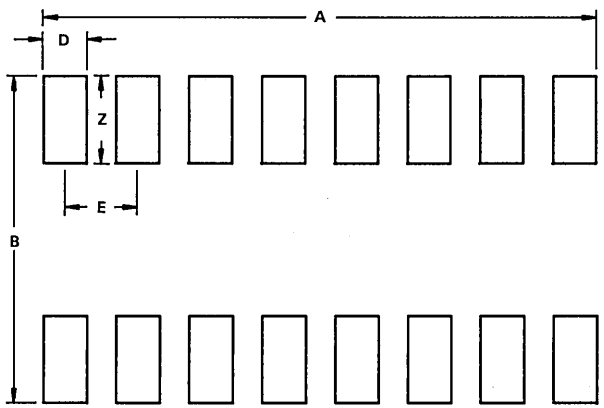


Figure 4. Standard SOIC Footprint

Table 1. SOIC Footprint Dimensions

No. of Terminals	A	B	Z	D	E
8	.175	.250	.050	.025	.050
14	.325	.250	.050	.025	.050
16	.375	.250	.050	.025	.050
20	.475	.430	.070	.025	.050
24	.575	.430	.070	.025	.050

Test	4164A PLCC	4164 DIP	Units
Life Test, 125°C	42	64	Fits*—60% UCL
85°C/85% RH	0.17	0.37	%/1000 Hours
Autoclave	0.17	0.96	%/240 Hours
T/C—65/150	0.52	1.44	%/1000 Cycles
T/C 0/125	0.0	0.0	%/2000 Cycles

*Derated to 55°C Assuming 0.5EV Activation Energy

Figure 5. Failure Rate Comparison 4164A PLCC VS DIP

Manufacturing

The SMT manufacturing area must have the following basic equipment:

- Solder Paste Printer
- Component Pick and Place Machine
- Solder Paste Reflow Machine
- Clean-up System
- Inspection/Process Control Aids
- Electrical Test

The criteria for choosing the above is determined mainly by the size(s) and quantity of PWBs per month, the gross number of components per PWB, and the number of different components per PWB.

The size of the largest PWB is an important criterion in the choice of all of the major items. The printer, pick and place, reflow, and clean-up must all be able to handle it with no difficulty or process nonuniformity. The number and size of the various PWBs that may be produced will secondarily be considered for ease of set up and changeover in the printer and pick and place. The pick and place machine(s) will probably be the most expensive item in the list above and therefore, should get the most attention.

The gross number of components and PWBs will provide data for choosing the pick and place. Component per hour placement speed should be checked in actual operation, as the interrelationship may affect ultimate speed. The number of different components per board will determine how many feeders and what types of feeders will be required. This is a very key issue, as well as the accuracy of placement.

Reflow

The solder reflow is easily achieved with any of the commercially available equipment. Subtle differences between vapor phase, either batch or in-line, and infrared are overshadowed by the choice of solder paste and the solderability/planarity issue. A batch vapor phase is extremely flexible for different sizes of boards with different component counts. The in-line vapor phase is a good choice for a more automated processing line with standard or similar sized boards. The infrared has the advantage of being less expensive to operate, but requires more alteration to set up the time-temperature profile for a different size PWB. This would be a minimal problem on a manufacturing line building high volumes of the same board.

Clean-up

The most popular flux for SMT is the mildly activated rosin flux (RMA). This was developed in the days of vacuum tube assembly when clean-up was next to impossible. It is noncorrosive but provides sufficient fluxing action for good quality components and PWBs. Thus it is the preferred choice for SMAs with small spacings under most passives and SOICs, where complete cleaning is difficult. A mild solvent, such as Freon TMS, is generally sufficient to achieve a good visual cleanup, and there are several systems available that provide hot vapor, spray, or ultrasonic de-fluxing.

Reliability

With the smaller surface mount packages, there is some concern about component reliability. Texas Instruments addressed the overall DRAM reliability issue several years ago. Through an extensive task force effort, the major problems of the life test, humidity performance, and temperature cycle were identified. The best solutions to these problems required several changes in the design and process of the silicon chip. In doing so, the reliability of the DRAM chip became independent of the package used. Thus, the 64K DRAM in the plastic chip carrier package performs equivalently to the same chip in a DIP as shown in Figure 5. Similar data is available on most semiconductor ICs.

An additional reliability concern originates in the surface mount solder reflow process, which submits components to higher reflow temperatures more suddenly than the wave-soldering methods of DIP components, with oftentimes repeated reflow cycles for rework and repair.

The best method for resolving this issue involves comparing the temperature-time differential of the vapor phase or infrared solder reflow process to the standard temperature

cycling reliability tests to which surface mount components are routinely submitted. Figures 6 and 7 show temperature profiles of the vapor phase and infrared solder reflow processes. In the vapor phase process, the maximum temperature change with time is:

$$\frac{215°C - 25°C}{45 \text{ sec}} = \frac{190°C}{45 \text{ sec}}$$

equaling approximately 4°C/sec. The infrared solder reflow method submits the ICs to a similar, yet less severe temperature over time change of 3°C/second. Comparing these temperature profile ramp-ups to that which a surface mount component undergoes in a temperature cycling reliability test proves that there should be no concern over damage to the component during reflow. In the temp cycling test, the surface mount components were submitted to 1000 cycles of sudden cycling from 150°C to −65°C within three seconds. This represents a temperature-time differential of:

$$\frac{150°C-(-65°C)}{3} = \frac{215°C}{3 \text{ sec}} = \frac{70°C}{\text{sec}}$$

with less than 0.5 percent failures.

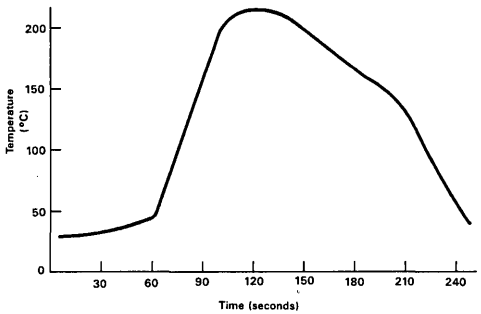


Figure 6. Typical Temperature Profile for In-Line Vapor Phase Reflow

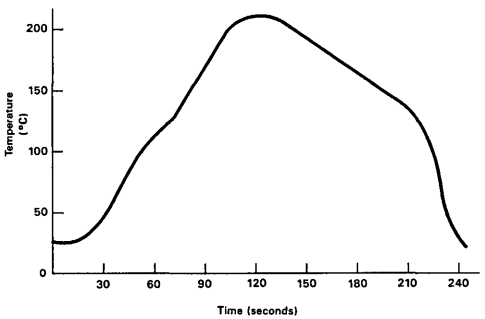


Figure 7. Typical IR Reflow System Profile

Since the surface mounted components were able to withstand a 70°C/second temperature change of 1000 cycles, they should be able to withstand the less severe conditions of a 4°C/second damage during reflow without reliability degradation.

Another concern in the solder reflow processing of surface mount components is the dwell time in reflow temperatures of 215°C or above. The dwell time for a small PWB populated with surface mount devices is about 20 seconds. For a larger board of about 10″×12″ up to 50 seconds is needed for reflow. A generalized component degradation curve, relating accumulated time and temperature, can be assumed to exist. The shape of the curve for this discussion is assumed to be a decaying parabolic for simplicity and conservatism. There are two generally known points of this curve. The flame retardant mold compound (FRMC) of a plastic package starts to break down at 300°C in two to three seconds. Also, the molding and curing of a surface mount device is performed over several hours at 175°C. These two points are shown on the generalized curve shown in Figure 8, with the "safe" region being the area under the curve. Two points that fall within this region are the industry standard practice of solder dipping leads of several types of ICs, and of the soldering plastic devices on the bottom with Type III surface mount assembly, each submerges the component for three to four seconds in a solder wave.

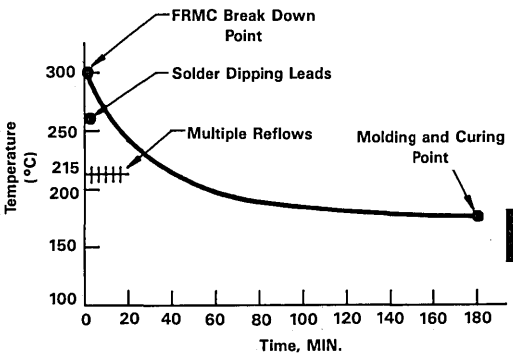


Figure 8. General Plastic Degradation Curve

Summary

Surface mount assembly techniques provide a significant advantage in cost, volume, and reliability over the current "thru-hole" technology. These are well documented, and the manufacturing equipment and related products are becoming readily available to support new production lines. Also, as experience grows, improved products and ideas are developed from the cooperative efforts of vendors and users in standardization organizations and in problem-solving sessions. The broad selection of package types and product technologies available now are sufficient to begin conversion of existing electronic system products for size reduction or feature enhancement. Definitely, new products should be designed with surface mount technology.

2 Memory Timing Controllers

2.1 Introduction

As processor and memory speeds increase, so do dynamic memory controller requirements. Typical processor speeds today range from 8 to 10 MHz. This increase in processor speed has created a need for faster memories, as well as faster memory timing controllers. The 'ALS2967, 'ALS2968, 'ALS6301, and 'ALS6302 are Memory Timing Controllers that are designed to meet the need of high performance memory systems.

In addition to offering better system performance, a faster memory controller typically allows the designer to use slower-rated dynamic random access memories (DRAMs). This results in significant cost savings because of the large number of DRAMs required. In other words, a faster dynamic memory controller can reduce overall dynamic memory costs.

The 'ALS2967, 'ALS2968, 'ALS6301, and 'ALS6302 feature address multiplexing, memory bank selection, and an address latch for systems which multiplex both data and address on the same bus. A row counter is provided for normal refresh operations. Column and bank counters are available for systems which use memory scrubbing.

This Section describes the functional operation of the 'ALS2967, 'ALS2968, 'ALS6301, and 'ALS6302 and shows how they can be interfaced to a typical processor. For illustration purposes, a simple timing controller generated from programmable logic is used to interface both the 'ALS2967 and the 'ALS6301 to the microprocessor. The 'ALS2967 is interfaced with an Intel 8086 and the 'ALS6301 is interfaced with a Motorola 68000.

This Section also presents a circuit configuration which interfaces the MC68000 to DRAM memory using the THCT4502B dynamic RAM Controller. The memory array is organized as 4 banks of 256K memory (TMS4256/4257) providing a 1M byte deep system architecture.

2.2 Memory Timing Controllers Using the SN54/74ALS2967, SN54/74ALS2968

2.2.1 Functional Description

The 'ALS2967 and 'ALS2968 are capable of controlling 16K, 64K, and 256K DRAMs. The two devices typically operate in a read/write or a refresh mode. During normal read/write operations, the row and column addresses are multiplexed to the DRAM, and the corresponding $\overline{RAS}$ and $\overline{CAS}$ signals are activated to strobe the addresses into memory. In the refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the row counter is used. When memory scrubbing is being performed, both the row and column counters are used to perform read-modify-write cycles using an error detection and correction circuit such as the 'ALS632A. In this mode, all $\overline{RAS}$ outputs will be active (low) while only one $\overline{CAS}$ output is active at a time.

Two device types are offered to help simplify interfacing with the system dynamic timing controller. The 'ALS2967 offers active-low row address strobe input ($\overline{RASI}$) and column address strobe input ($\overline{CASI}$) signals, while the 'ALS2968 offers active-high RASI and CASI inputs. Figure 2-1 is a functional block diagram of the two devices.

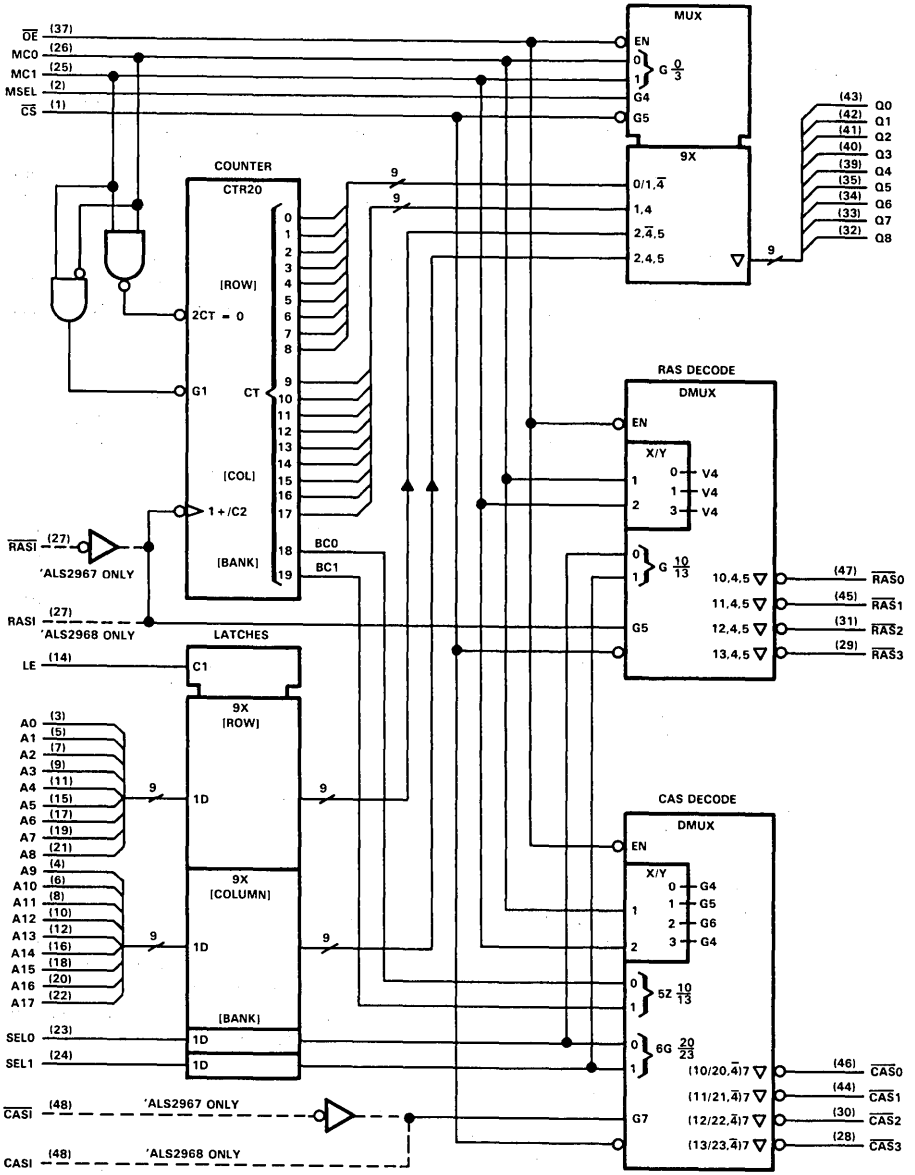


Figure 2-1. 'ALS2967, 'ALS2968 Functional Block Diagram

Table 2-1 describes the four operating modes of the 'ALS2967 and 'ALS2968 as controlled by inputs MC0 and MC1. During normal read/write operations, the row and column addresses are multiplexed to the DRAM. When MSEL is high, the column address is selected; when MSEL is low, the row address is selected. The corresponding $\overline{RAS}$n and $\overline{CAS}$n output signals strobe the addresses into the selected memory bank or banks. A single 'ALS2967 or 'ALS2968 can control as many as four banks of 256K memory. Additional banks of memory can be controlled by using additional 'ALS2967 or 'ALS2968 devices and decoding each chip select ($\overline{CS}$) input.

Table 2-1. 'ALS2967, 'ALS2968 Mode-Control Function Table

SIGNAL		MODE SELECTED
MC1	MC0	
L	L	Refresh without Scrubbing. Refresh cycles are performed using the row counter to generate the addresses. In this mode, all four $\overline{RAS}$ outputs are active while the four $\overline{CAS}$ outputs remain high.
L	H	Refresh with Scrubbing/Initialize. Refresh cycles are performed using both the row and column counters to generate the addresses. MSEL selects the row or the column counter. All four $\overline{RAS}$ outputs go low in response to $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968), while only one $\overline{CAS}$n output goes low in response to $\overline{CASI}$ ('ALS2967) or CASI ('ALS2968). The bank counter keeps track of which $\overline{CAS}$ output goes active. This mode can also be used during system power-up so that the memory can be written with a known data pattern.
H	L	Read/Write. This mode is used to perform read/write cycles. Both the row and column addresses are multiplexed to the address output lines using MSEL. SEL0 and SEL1 are decoded to determine which $\overline{RAS}$n and $\overline{CAS}$n outputs will be active.
H	H	Clear Refresh Counters. This mode clears the three refresh counters (row, column, and bank) on the inactive transition of $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968), putting them at the beginning of the refresh sequence. In this mode, all four $\overline{RAS}$ outputs are driven low after the active edge of $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968) so that DRAM wake-up cycles can also be performed.

In systems where addresses and data are both multiplexed onto a single bus, the 'ALS2967 and 'ALS2968 use latches (row, column and bank) to hold the address information. The 20 input latches are transparent when the latch enable input (LE) is high; the input data is latched whenever LE goes low. For systems in which the processor has separate address and data buses, LE may be tied high.

The two 9-bit counters in the 'ALS2967 and 'ALS2968 support 128, 256, and 512 line refresh operations. Transparent, burst, synchronous, or asynchronous refresh modes are all possible as determined by the memory timing controller. The refresh counters are advanced on the low-to-high transition of $\overline{RASI}$ on the 'ALS2967, and on the high-to-low transition of RASI on the 'ALS2968. This is true in either refresh mode. In the clear refresh counter mode, the refresh counters (row, column, and bank) can be reset to zero on the low-to-high transition of $\overline{RASI}$ on the 'ALS2967 or on the high-to-low transition of RASI on the 'ALS2968.

2.2.2 Typical Implementation

Figure 2-2 shows a system interface using the 'ALS2967 between an Intel 8086 and four banks of 256K DRAMs. Addresses A18 and A19 are used to select one of the four memory banks. Since members of the 8086 processor family multiplex both data and addresses onto the same data bus, input latches on the 'ALS2967 must be used to store the row, column, and bank information. The ALE signal from the 8086 can be directly connected to the latch enable (LE) input on the 'ALS2967.

The $\overline{RASI}$, $\overline{CASI}$, MSEL and mode control (MC0, MC1) inputs on the 'ALS2967 must be generated by the memory timing controller. The memory timing controller functions as an arbitrator between refresh cycles and 8086 access cycles. It also guarantees that timing requirements of the DRAM will be met.

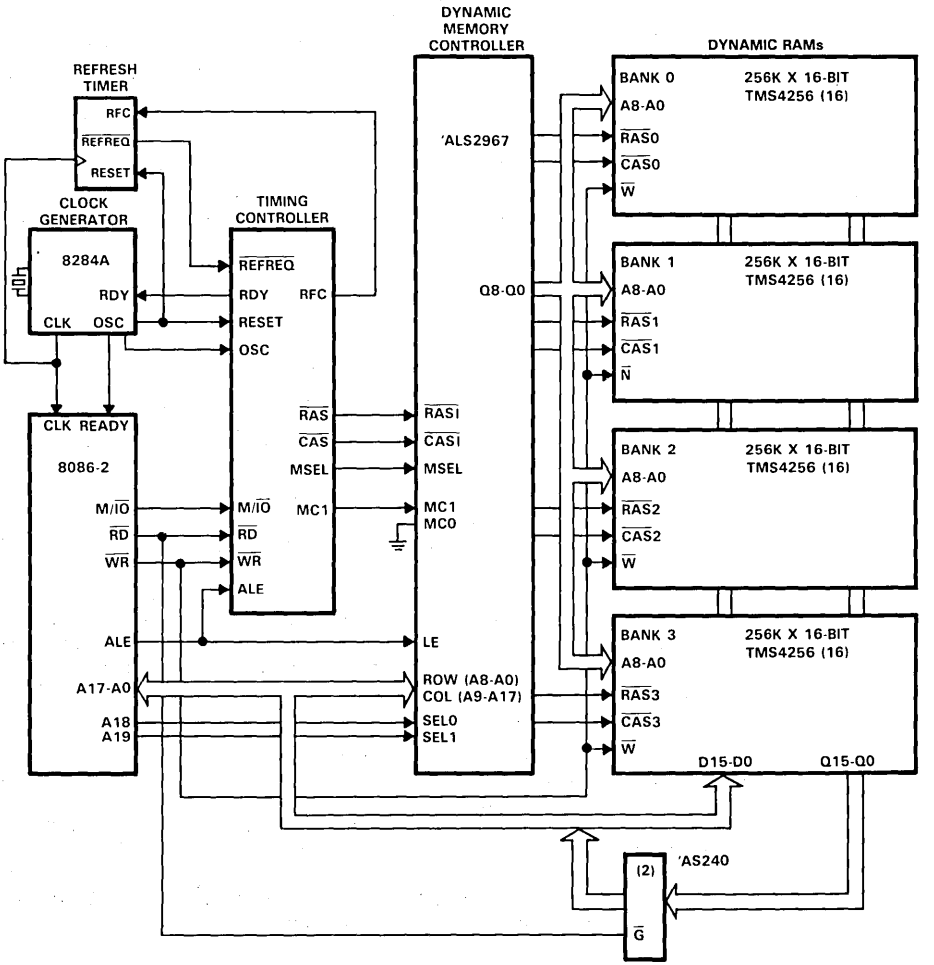


Figure 2-2. 'ALS2967, 'ALS2968 Timing Controller Interface

2.2.3 Timing Controller Details

Figure 2-3 is a timing diagram for a typical 8086 access cycle. The 'ALS2967 control signals required to execute the access cycle are also shown. Control signals for the 'ALS2967 are referenced from the OSC output of the 8284A clock generator. The timing controller in this example is generated from a state machine referenced from the OSC output of the 8284A. In critical timing situations, it may be necessary to tightly control the phase relationship of the system clock to the OSC signal. This can be accomplished by using a phase lock loop or similar method to generate the OSC signal.

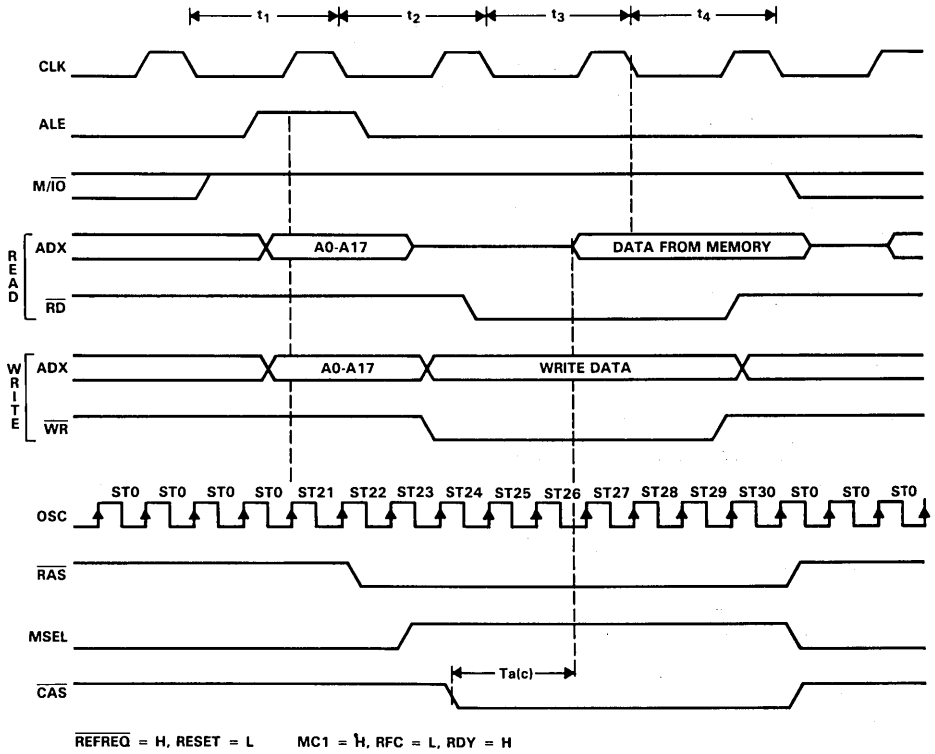


Figure 2-3. 8086 Access Cycle

In this example, refresh requests ($\overline{\text{REFREQ}}$) are generated every 122 clock cycles. The timing controller will perform the refresh cycle ($\overline{\text{RAS}}$ only) immediately if the processor is not in the middle of an access cycle. If the controller is in the middle of an access cycle, the refresh cycle will be delayed until the access cycle is complete. If the controller is asked to perform an access cycle during a refresh, the controller will place the processor in a wait state (RDY low) until the refresh is complete. Figure 2-4 shows the timing diagram for a refresh/access cycle as explained above. To implement memory scrubbing, the controller must execute a read/write cycle during the refresh cycle and then place the 'ALS2967 in the memory scrubbing mode (This example executes $\overline{\text{RAS}}$ only refresh).

Figure 2-5 is a flow chart for the timing controller. ABEL™ and CUPL™ software was used to generate fuse maps from the present state of the inputs and present condition of the state machine. These fuse maps were then used in programming the field programmable logic devices. The files used to generate the fuse maps have been included for reference at the end of this application note.

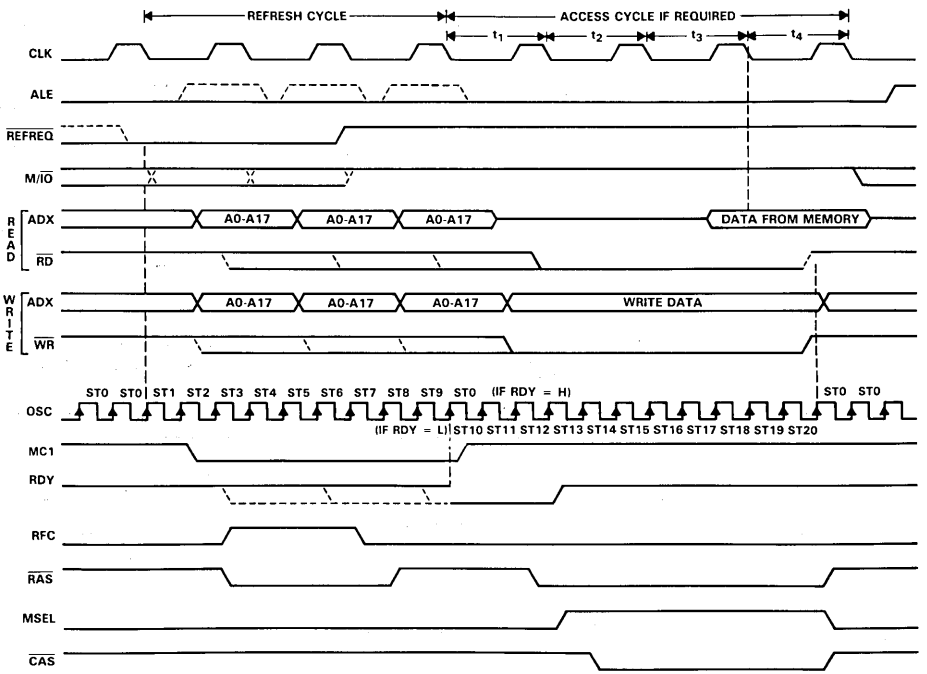


Figure 2-4. Refresh/Access Cycle

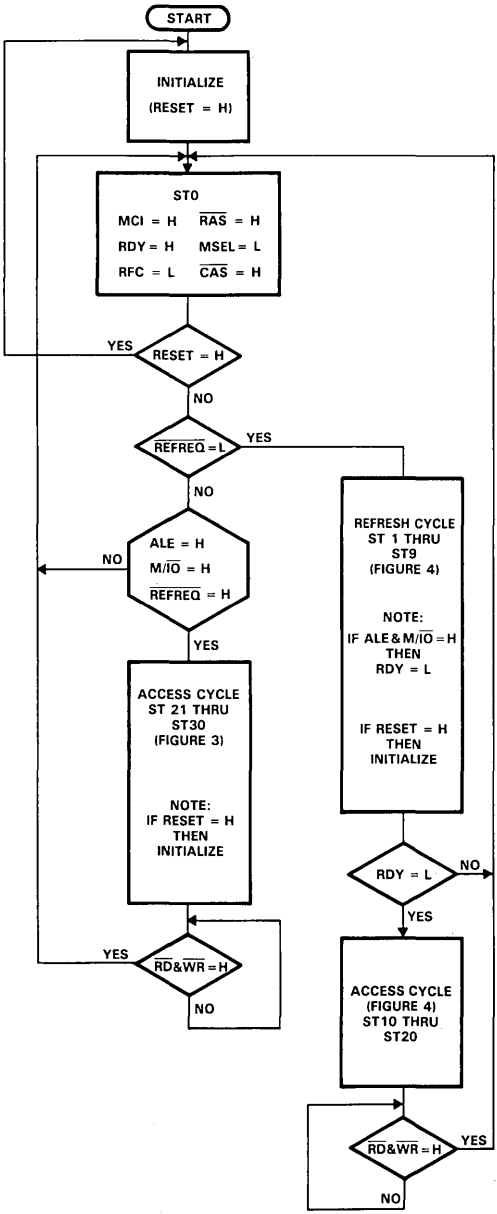


Figure 2-5. 'ALS2967, 'ALS2968 Memory Timing Controller Flow Chart

Figure 2-6 shows the actual circuit implementation of the refresh and memory timing controller. The refresh timer signals the controller whenever it is time to execute a refresh cycle. As required by memory, every row (256 on the TMS4256 DRAM) must be addressed every 4 ms. This implies that one row should be refreshed at least once every 15.6 μs. With an 8-MHz system clock, the refresh timer should use approximately a division factor of 122. This results in a refresh request every 15.3 μs. The refresh complete input (RFC) is used to signal the refresh timer that the refresh has been completed. It is important that the timer not stop so that the 4-ms memory requirement is maintained.

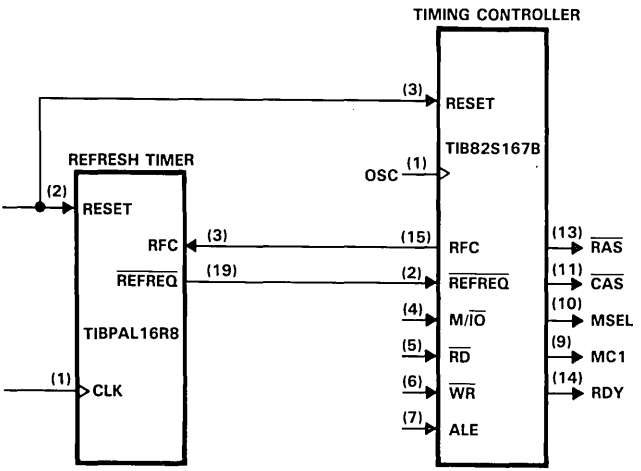


Figure 2-6. Refresh/Memory Timing Controller

The TIBPAL16R8 circuit shown in Figure 2-6 is used to generate the refresh request signal every 122 clock cycles. The refresh request signal (active low) will remain active (low) until a refresh complete (RFC) signal is received from the timing controller. During a system reset, the refresh request output is set to a high-logic level. When using different clock rates or memory sizes, the division circuit in the refresh timer should be adjusted accordingly.

The TIB82S167B field programmable sequencer shown in Figure 2-6 is configured as a state machine to execute the flow chart shown in Figure 2-5. In cases with different system timings, the CUPL™ file can be modified to fit the processor requirements. In addition, a slight modification to the file will allow an 'ALS2968 to be used instead of an 'ALS2967.

A preprogrammed sample of the refresh and timing controllers shown in Figure 2-6 can be obtained by calling PAL/PROM Applications, 214/995-2980.

2.2.4 Summary

The 'ALS2967 and 'ALS2968, coupled with programmable logic, offer the system designer a solution to high-speed dynamic memory requirements. Programmable logic allows the designer to tailor the timing controller to a selected processor and memory. In many cases, the generation of a high-speed timing controller from programmable logic will allow the designer to use slower DRAMs without affecting system speed. This results in lower total system cost because of the large number of memory devices used.

2.2.5 ABEL™ and CUPL™ Files

2.2.5.1 ABEL™ File

```
module  RF_TIMER
title   'REFRESH TIMER
        R. K. BREUNINGER  TEXAS INSTRUMENTS, DALLAS, 08/12/86'

        RFT   DEVICE   'P16R8';

"input declarations

CLK             pin 1;              "  SYSTEM CLOCK (8086)
RESET           pin 2;              "  RESETS WHEN HIGH
RFC             pin 3;              "  REFRESH COMPLETE
OE              pin 11;             "  MUST BE TIED LOW

"output declarations

Q0,Q1,Q2        pin 12,13,14;       "  COUNTER STATES
Q3,Q4,Q5,Q6     pin 15,16,17,18;    "  COUNTER STATES
REFREQ_         pin 19;             "  REFRESH REQUEST - ACTIVE LOW

"intermediate variables

CNT_REF  =  Q0 & !Q1 & !Q2 & Q3 & Q4 & Q5 & Q6;
SCLR     =  RESET # CNT_REF;
count    = [Q6,Q5,Q4,Q3,Q2,Q1,Q0];
C,H,L    = .C.,1,0;

equations

REFREQ_  :=  RFC # !CNT_REF &  REFREQ_ #  RESET;
Q0       :=  (!Q0 ) & !SCLR;
Q1       :=  ( Q1 $  Q0) & !SCLR;
Q2       :=  ( Q2 $  Q1 &  Q0) & !SCLR;
Q3       :=  ( Q3 $ (Q2 &  Q1 &  Q0)) & !SCLR;
Q4       :=  ( Q4 $ (Q3 &  Q2 &  Q1 &  Q0)) & !SCLR;
Q5       :=  ( Q5 $ (Q4 &  Q3 &  Q2 &  Q1 &  Q0)) & !SCLR;
Q6       := !(!Q5 & !Q6 # !Q4 & !Q6 # !Q3 & !Q6
            # !Q0 & !Q6 # !Q2 & !Q6 # !Q1 & !Q6 # SCLR);

test_vectors                    ([OE,RESET,CLK,RFC] -> [count,REFREQ_])
                                 [ 0,  1  , C , 0 ] -> [  0  ,   H   ];
@CONST cnt = 1; @REPEAT 121  { [ 0,  0  , C , 0 ] -> [ cnt ,   H   ];
                                 @CONST cnt = cnt + 1;}

                                 [ 0,  0  , C , 0 ] -> [  0  ,   L   ];
@CONST cnt = 1; @REPEAT 20   { [ 0,  0  , C , 0 ] -> [ cnt ,   L   ];
                                 @CONST cnt = cnt + 1;}

                                 [ 0,  0  , C , 1 ] -> [ 21  ,   H   ];
                                 [ 0,  0  , C , 0 ] -> [ 22  ,   H   ];
                                 [ 0,  0  , C , 0 ] -> [ 23  ,   H   ];
                                 [ 0,  0  , C , 0 ] -> [ 24  ,   H   ];

end RF_TIMER
```

2.2.5.2 *CUPL™ Source File*

```
Partno          MTC-S167;
Name            MTC-S167;
Date            08/13/86;
Revision        03;
Designer        BREUNINGER;
Company         TEXAS INSTRUMENTS;
Assembly        None;
Location        DALLAS, TEXAS;
/*****************************************************************/
/*                  DYNAMIC TIMING CONTROLER                     */
/*                     (FOR ALS2967)                             */
/*****************************************************************/
/* Allowable Target Device Types: TIB82S167B                     */
/*****************************************************************/

/**  Inputs  **/
pin 1 =  OSC;              /*  OSCILLATOR (8284A)                */
pin 2 = REFREQ;            /*  REFRESH REQUEST                   */
pin 3 = RESET;             /*  RESET - INITIALIZES WHEN HIGH     */
pin 4 = MIO;               /*  MEMORY I/O                        */
pin 5 = RD;                /*  READ                              */
pin 6 = WR;                /*  WRITE                             */
pin 7 = ALE;               /*  ADDRESS LATCH ENABLE              */
pin 16 = GND;              /*  PIN 16 MUST BE TIED LOW           */

/**  Outputs  **/
pin  9 = MCI_;             /*  MODE CONTROL                      */
pin 10 = MSEL;             /*  MULTIPLEXER SELECT                */
pin 11 = CAS;              /*  COLUMN ADDRESS STROBE             */
pin 13 = RAS;              /*  ROW ADDRESS STOBE                 */
pin 14 = RDY;              /*  READY                             */
pin 15 = RFC;              /*  REFRESH COMPLETE                  */

/** Internal Node Group  -   State bits declared as nodes       **/
node [P4_,P3_,P2_,P1_,P0_];

/** Declarations and Intermediate Variable Definitions          **/
Field State  = [P4_,P3_,P2_,P1_,P0_];

$define  ST0 'b'00000
$define  ST1 'b'00001
$define  ST2 'b'00010
$define  ST3 'b'00011
$define  ST4 'b'00100
$define  ST5 'b'00101
$define  ST6 'b'00110
$define  ST7 'b'00111
$define  ST8 'b'01000
$define  ST9 'b'01001
$define ST10 'b'01010
$define ST11 'b'01011
$define ST12 'b'01100
```

```
$define ST13 'b'01101
$define ST14 'b'01110
$define ST15 'b'01111
$define ST16 'b'10000
$define ST17 'b'10001
$define ST18 'b'10010
$define ST19 'b'10011
$define ST20 'b'10100
$define ST21 'b'10101
$define ST22 'b'10110
$define ST23 'b'10111
$define ST24 'b'11000
$define ST25 'b'11001
$define ST26 'b'11010
$define ST27 'b'11011
$define ST28 'b'11100
$define ST29 'b'11101
$define ST30 'b'11110
$define ST31 'b'11111

/** Logic Equations **/
Sequence State
(Present ST0 IF  RESET              NEXT ST0 OUT [MC1_, RDY,!RFC, RAS,!MSEL, CAS];
             IF !RESET & !REFREQ    NEXT ST1;
             IF !RESET &  REFREQ & ALE & MIO NEXT ST21;
             DEFAULT                NEXT ST0;

/** REFRESH CYCLE **/
Present ST1 IF  ALE & MIO&!RESET NEXT ST2 OUT [!MC1_,!RDY];
            IF !RESET            NEXT ST2 OUT [!MC1_];
Present ST2 IF  ALE & MIO&!RESET NEXT ST3 OUT [!RDY, RFC,!RAS];
            IF !RESET            NEXT ST3 OUT [ RFC,!RAS];
Present ST3 IF  ALE & MIO&!RESET NEXT ST4 OUT [!RDY];
            IF !RESET            NEXT ST4;
Present ST4 IF  ALE & MIO&!RESET NEXT ST5 OUT [!RDY];
            IF !RESET            NEXT ST5;
Present ST5 IF  ALE & MIO&!RESET NEXT ST6 OUT [!RDY];
            IF !RESET            NEXT ST6;
Present ST6 IF  ALE & MIO&!RESET NEXT ST7 OUT [!RDY,!RFC];
            IF !RESET            NEXT ST7 OUT [!RFC];
Present ST7 IF  ALE & MIO&!RESET NEXT ST8 OUT [!RDY, RAS];
            IF !RESET            NEXT ST8 OUT [ RAS];
Present ST8 IF  ALE & MIO&!RESET NEXT ST9 OUT [!RDY];
            IF !RESET            NEXT ST9;
Present ST9 IF  RDY & !RESET     NEXT ST0 OUT [ MC1_, RDY,!RFC, RAS,!MSEL, CAS];
            IF !RDY & !RESET     NEXT ST10 OUT [ MC1_];
```

```
/** ACCESS IMMEDIATELY AFTER REFRESH WHEN REQUESTED **/
Present ST10 IF !RESET              NEXT ST11;
Present ST11 IF !RESET              NEXT ST12 OUT [!RAS];
Present ST12 IF !RESET              NEXT ST13 OUT [ RDY, MSEL];
Present ST13 IF !RESET              NEXT ST14 OUT [!CAS];
Present ST14 IF !RESET              NEXT ST15;
Present ST15 IF !RESET              NEXT ST16;
Present ST16 IF !RESET              NEXT ST17;
Present ST17 IF !RESET              NEXT ST18;
Present ST18 IF !RESET              NEXT ST19;
Present ST19 IF !RESET              NEXT ST20;
Present ST20 IF RD & WR & !RESET NEXT ST0 OUT [ MC1_, RDY,!RFC, RAS,!MSEL, CAS];
             IF !RESET              NEXT ST20;

/** ACCESS TIMING CYCLE **/
Present ST21 IF !RESET              NEXT ST22 OUT [!RAS];
Present ST22 IF !RESET              NEXT ST23 OUT [ MSEL];
Present ST23 IF !RESET              NEXT ST24 OUT [!CAS];
Present ST24 IF !RESET              NEXT ST25;
Present ST25 IF !RESET              NEXT ST26;
Present ST26 IF !RESET              NEXT ST27;
Present ST27 IF !RESET              NEXT ST28;
Present ST28 IF !RESET              NEXT ST29;
Present ST29 IF !RESET              NEXT ST30;
Present ST30 IF RD & WR & !RESET NEXT ST0 OUT [ MC1_, RDY,!RFC, RAS,!MSEL, CAS];
             IF !RESET              NEXT ST30;}

APPEND  MC1_.s = RESET;    APPEND  RDY.s = RESET;    APPEND  RFC.r = RESET;
APPEND  RAS.s = RESET;     APPEND  MSEL.r= RESET;    APPEND  CAS.s = RESET;
APPEND  P0_.r = RESET;     APPEND  P1_.r = RESET;    APPEND  P2_.r = RESET;
APPEND  P3_.r = RESET;     APPEND  P4_.r = RESET;
```

2.2.5.3 *CUPL™ Simulation File*

```
Partno          MTC-S167;
Name            MTC-S167;
Date            08/13/86;
Revision        03;
Designer        BREUNINGER;
Company         TEXAS INSTRUMENTS;
Assembly        None;
Location        DALLAS, TEXAS;
/*****************************************************************/
/*          DYNAMIC TIMING CONTROLLER SIMULATION FILE            */
/*                        (FOR ALS2967)                          */
/*****************************************************************/
/* Allowable Target Device Types: TIB82S167B                     */
/*****************************************************************/

ORDER:
GND,%3,OSC,%3,RESET,%6,REFREQ,%4,MIO,%3,RD,%2,WR,%2,ALE,%5,
MCI_,%4,MSEL,%3,CAS,%3,RAS,%3,RDY,%3,RFC;

VECTORS:

$msg"REFRESH WITH ACCESS FOLLOWING";
$msg"     ------------ INPUT ---------------   -------- OUTPUT --------";
$msg"    GND OSC RESET REFREQ MIO RD WR ALE    MCI MSEL CAS RAS RDY RFC";
$msg"     ------------------------------------------------------------";
/*RESET*/ 0   C   1      X     X   X  X  X      H   L    H   H   H   L
/* ST0*/  0   C   0      0     X   X  X  X      H   L    H   H   H   L
/* ST1*/  0   C   0      X     0   X  X  0      L   L    H   H   H   L
/* ST2*/  0   C   0      X     0   X  X  0      L   L    H   L   H   H
/* ST3*/  0   C   0      X     0   X  X  0      L   L    H   L   H   H
/* ST4*/  0   C   0      X     1   X  X  1      L   L    H   L   L   H
/* ST5*/  0   C   0      X     X   X  X  X      L   L    H   L   L   H
/* ST6*/  0   C   0      X     X   X  X  X      L   L    H   L   L   L
/* ST7*/  0   C   0      X     X   X  X  X      L   L    H   H   L   L
/* ST8*/  0   C   0      X     X   X  X  X      L   L    H   H   L   L
/* ST9*/  0   C   0      X     X   X  X  X      H   L    H   H   L   L
/*ST10*/  0   C   0      1     X   X  X  X      H   L    H   H   L   L
/*ST11*/  0   C   0      X     X   X  X  X      H   L    H   L   L   L
/*ST12*/  0   C   0      X     X   X  X  X      H   H    H   L   H   L
/*ST13*/  0   C   0      X     X   X  X  X      H   H    L   L   H   L
/*ST14*/  0   C   0      X     X   X  X  X      H   H    L   L   H   L
/*ST15*/  0   C   0      X     X   X  X  X      H   H    L   L   H   L
/*ST16*/  0   C   0      X     X   X  X  X      H   H    L   L   H   L
/*ST17*/  0   C   0      X     X   X  X  X      H   H    L   L   H   L
/*ST18*/  0   C   0      X     X   X  X  X      H   H    L   L   H   L
/*ST19*/  0   C   0      X     X   X  X  X      H   H    L   L   H   L
/*ST20*/  0   C   0      X     X   0  0  X      H   H    L   L   H   L
/*ST20*/  0   C   0      X     X   1  1  X      H   L    H   H   H   L
```

```
$msg"    ";
$msg"REFRESH WITHOUT ACCESS FOLLOWING";
$msg"    ------------ INPUT ---------------   -------- OUTPUT --------";
$msg"    GND OSC RESET REFREQ MIO RD WR ALE   MC1 MSEL CAS RAS RDY RFC";
/*RESET*/ 0   C    1      X    X  X  X  X     H    L   H   H   H   L
/* ST0*/  0   C    0      0    X  X  X  X     H    L   H   H   H   L
/* ST1*/  0   C    0      X    0  X  X  0     L    L   H   H   H   L
/* ST2*/  0   C    0      X    0  X  X  0     L    L   H   L   H   H
/* ST3*/  0   C    0      X    0  X  X  0     L    L   H   L   H   H
/* ST4*/  0   C    0      X    0  X  X  0     L    L   H   L   H   H
/* ST5*/  0   C    0      X    0  X  X  0     L    L   H   L   H   H
/* ST6*/  0   C    0      X    0  X  X  0     L    L   H   L   H   L
/* ST7*/  0   C    0      X    0  X  X  0     L    L   H   H   H   L
/* ST8*/  0   C    0      X    0  X  X  0     L    L   H   H   H   L
/* ST9*/  0   C    0      X    0  X  X  0     H    L   H   H   H   L

$msg"    ";
$msg"ACCESS TIMING CYCLE ";
$msg"    ------------ INPUT ---------------   -------- OUTPUT --------";
$msg"    GND OSC RESET REFREQ MIO RD WR ALE   MC1 MSEL CAS RAS RDY RFC";
/*RESET*/ 0   C    1      X    X  X  X  X     H    L   H   H   H   L
/* ST0*/  0   C    0      1    1  X  X  1     H    L   H   H   H   L
/*ST21*/  0   C    0      X    X  X  X  X     H    L   H   L   H   L
/*ST22*/  0   C    0      X    X  X  X  X     H    H   H   L   H   L
/*ST23*/  0   C    0      X    X  X  X  X     H    H   L   L   H   L
/*ST24*/  0   C    0      X    X  X  X  X     H    H   L   L   H   L
/*ST25*/  0   C    0      X    X  X  X  X     H    H   L   L   H   L
/*ST26*/  0   C    0      X    X  X  X  X     H    H   L   L   H   L
/*ST27*/  0   C    0      X    X  X  X  X     H    H   L   L   H   L
/*ST28*/  0   C    0      X    X  X  X  X     H    H   L   L   H   L
/*ST29*/  0   C    0      X    X  X  X  X     H    H   L   L   H   L
/*ST30*/  0   C    0      X    X  0  0  X     H    H   L   L   H   L
/*ST30*/  0   C    0      X    X  1  1  X     H    L   H   H   H   L
```


2.3 Memory Timing Controllers Using the SN54/74ALS6301, SN54/74ALS6302

2.3.1 Functional Description

The 'ALS6301 and 'ALS6302 are capable of controlling any DRAM up to 1M. The two devices typically operate in a read/write or a refresh mode. During normal read/write operations, the row and column addresses are multiplexed to the DRAM, and the corresponding $\overline{RAS}$ and $\overline{CAS}$ signals are activated to strobe the addresses into memory. In the refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the row counter is used. When memory scrubbing is being performed, both the row and column counters are used to perform read-modify-write cycles using an error detection and correction circuit such as the 'ALS632A. In this mode, all $\overline{RAS}$ outputs will be active (low) while only one $\overline{CAS}$ output is active at a time.

Two device types are offered to help simplify interfacing with the system dynamic timing controller. The 'ALS6301 offers active-low row address strobe input ($\overline{RASI}$) and column address strobe input ($\overline{CASI}$) signals, while the 'ALS6302 offers active-high RASI and CASI inputs. Figure 2-7 is a functional block diagram of the two devices.

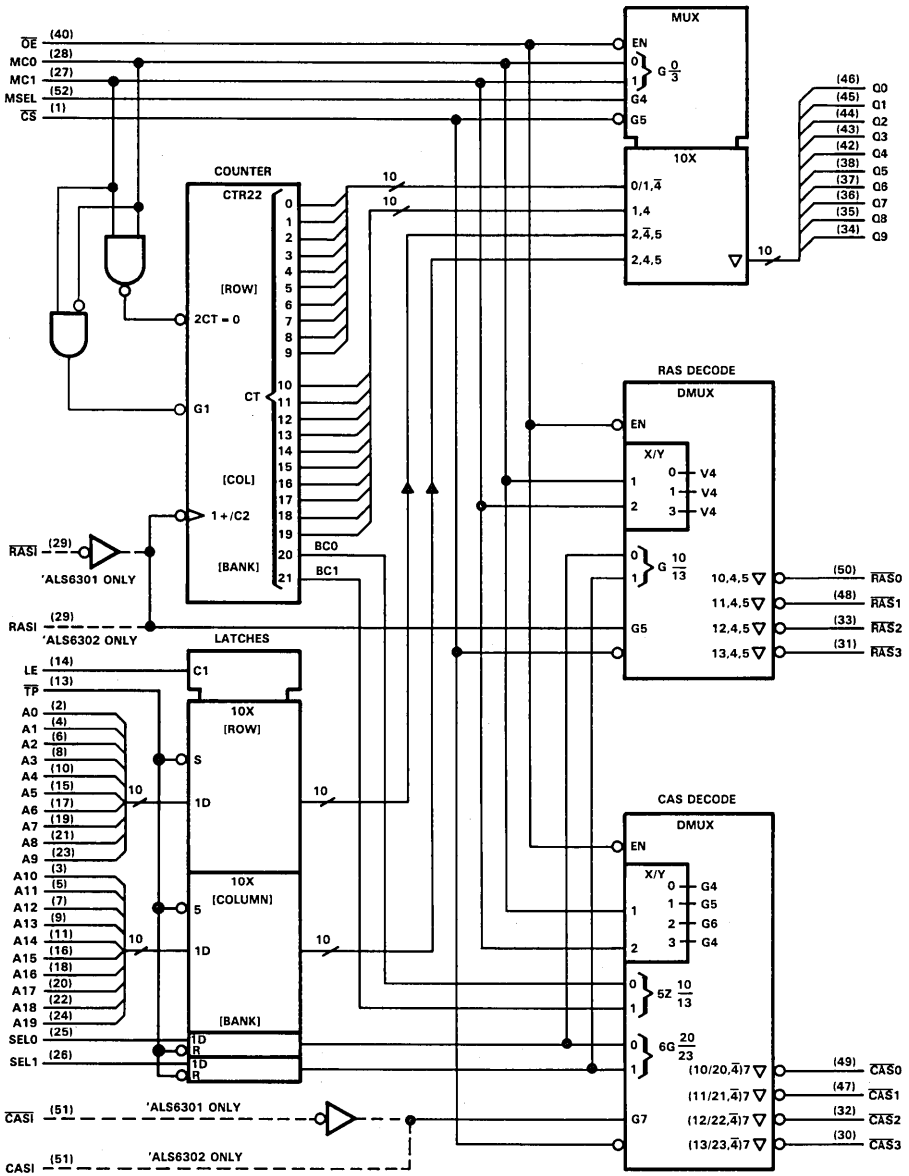


Figure 2-7. 'ALS6301, 'ALS6302 Functional Block Diagram

Table 2-2 describes the four operating modes of the 'ALS6301 and 'ALS6302 as controlled by inputs MC0 and MC1. During normal read/write operations, the row and column addresses are multiplexed to the DRAM. When MSEL is high, the column address is selected; when MSEL is low, the row address is selected. The corresponding $\overline{RAS}$n and $\overline{CAS}$n output signals strobe the addresses into the selected memory bank or banks. A single 'ALS6301 or 'ALS6302 can control as many as four banks of 1M memory. Additional banks of memory can be controlled by using additional 'ALS6301 or 'ALS6302 devices and decoding each chip select ($\overline{CS}$) input.

Table 2-2. 'ALS6301, 'ALS6302 Mode-Control Function Table

SIGNAL		MODE SELECTED
MC1	MC0	
L	L	Refresh without Scrubbing. Refresh cycles are performed using the row counter to generate the addresses. In this mode, all four $\overline{RAS}$ outputs are active while the four $\overline{CAS}$ outputs remain high.
L	H	Refresh with Scrubbing/Initialize. Refresh cycles are performed using both the row and column counters to generate the addresses. MSEL selects the row or the column counter. All four $\overline{RAS}$ outputs go low in response to $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302), while only one $\overline{CAS}$n output goes low in response to $\overline{CASI}$ ('ALS6301) or CASI ('ALS6302). The bank counter keeps track of which $\overline{CAS}$ output goes active. This mode can also be used during system power-up so that the memory can be written with a known data pattern.
H	L	Read/Write. This mode is used to perform read/write cycles. Both the row and column addresses are multiplexed to the address output lines using MSEL. SEL0 and SEL1 are decoded to determine which $\overline{RAS}$n and $\overline{CAS}$n outputs will be active.
H	H	Clear Refresh Counters. This mode clears the three refresh counters (row, column, and bank) on the inactive transition of $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302), putting them at the beginning of the refresh sequence. In this mode, all four $\overline{RAS}$ outputs are driven low after the active edge of $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302) so that DRAM wake-up cycles can also be performed.

In systems where addresses and data are both multiplexed onto a single bus, the 'ALS6301 and 'ALS6302 use latches (row, column and bank) to hold the address information. The 22 input latches are transparent when the latch enable input (LE) is high; the input data is latched whenever LE goes low. For systems in which the processor has separate address and data buses, LE may be tied high.

The two 10-bit counters in the 'ALS6301 and 'ALS6302 support 128, 256, and 512 line refresh operations. Transparent, burst, synchronous, or asynchronous refresh modes are all possible as determined by the memory timing controller. The refresh counters are advanced on the low-to-high transition of $\overline{RASI}$ on the 'ALS6301, and on the high-to-low transition of RASI on the 'ALS6302. This is true in either refresh mode. In the clear refresh counter mode, the refresh counters (row, column, and bank) can be reset to zero on the low-to-high transition of $\overline{RASI}$ on the 'ALS6301 or on the high-to-low transition of RASI on the 'ALS6302.

2.3.2 Typical Implementation

Figure 2-8 shows a system interface using the 'ALS6301 between a Motorola 68000L10 and four banks of 1M DRAMs. Addresses A21 and A22 are used to select one of the four memory banks. Since members of the 68000 processor family have separate address and data busses, the input latches on the 'ALS6301 are left transparent by tying the latch enable (LE) input high. The $\overline{CAS0}$ thru $\overline{CAS3}$ outputs of the 'ALS6301 are fed into the byte controller along with processor signals $\overline{LDS}$ and $\overline{UDS}$. The byte controller made from programmable logic allows the processor to determine whether upper, lower or both bytes are accessed.

The $\overline{RASI}$, $\overline{CASI}$, MSEL and mode control (MC0, MC1) inputs on the 'ALS6301 must be generated by the memory timing controller. The memory timing controller functions as an arbitrator between refresh cycles and 68000L10 access cycles. It also guarantees that timing requirements of the DRAM will be met.

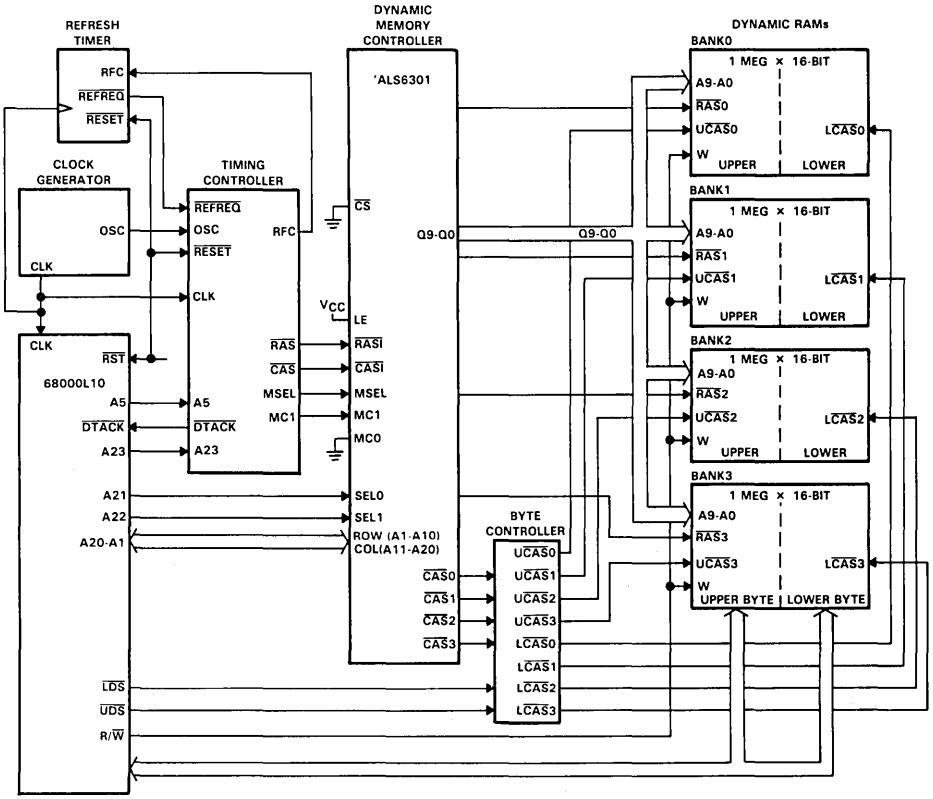
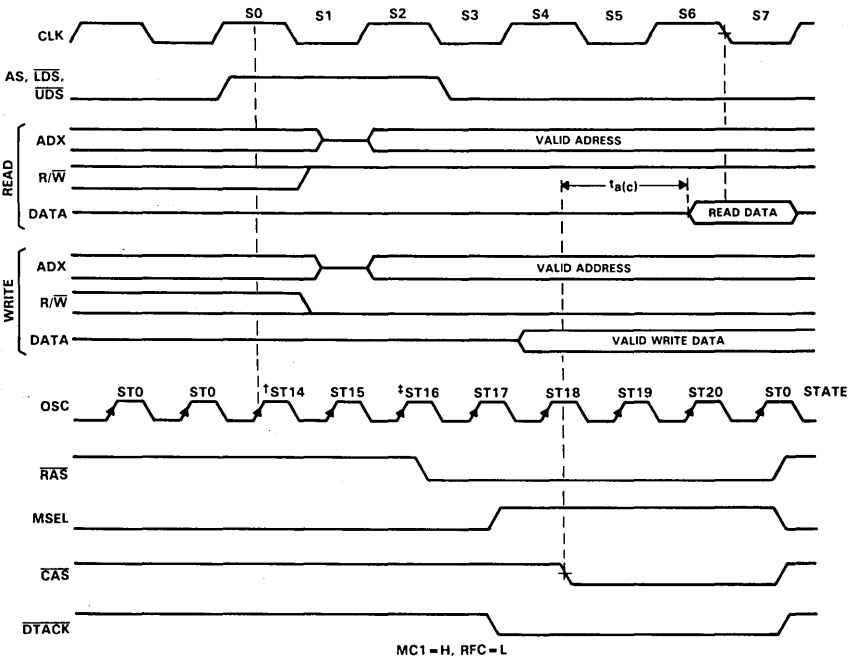


Figure 2-8. 'ALS6301, 'ALS6302 Timing Controller Interface

2.3.3 Timing Controller Details

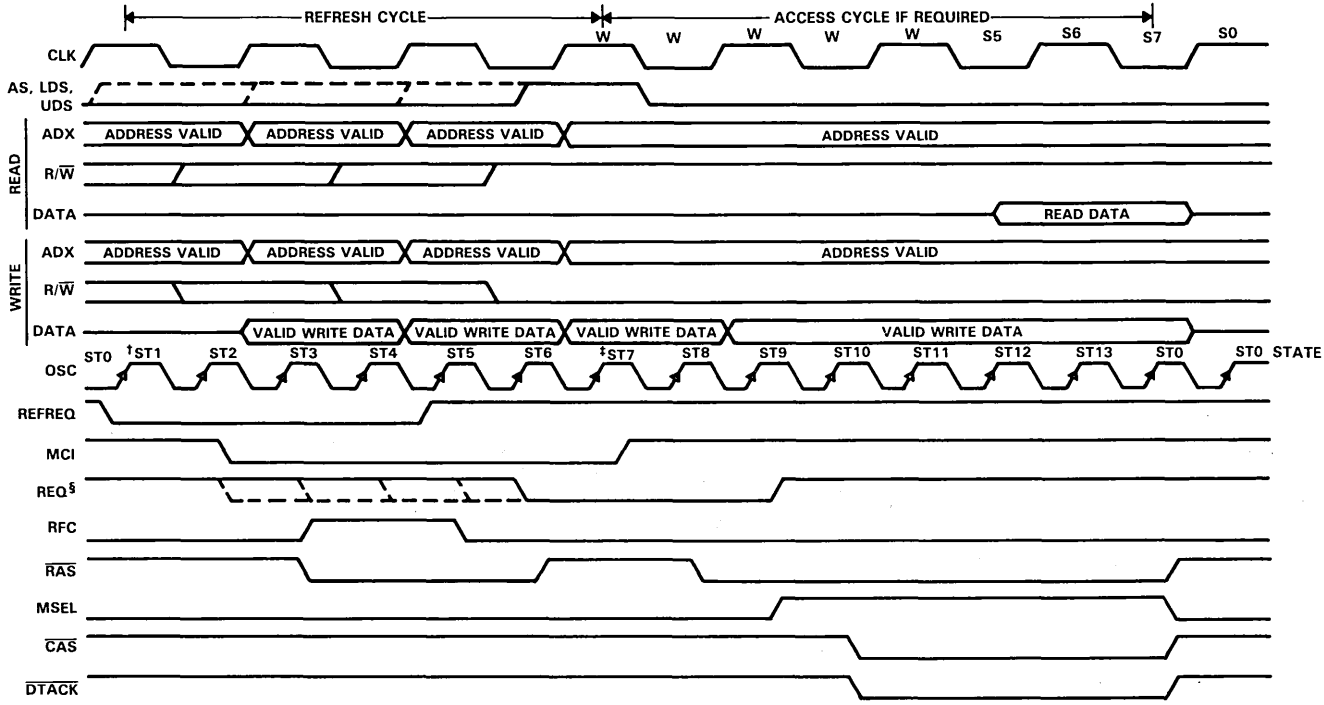
Figure 2-9 is a timing diagram for a typical 68000L10 access cycle. The 'ALS6301 control signals required to execute the access cycle are also shown. Control signals for the 'ALS6301 are referenced from the OSC output of the 8284A clock generator. OSC runs at 2 times the speed of the system clock, that is CLK = 10 MHz and OSC = 20 MHz. By running the timing controller at a higher speed than the system clock, the system performance is improved. A programmable logic sequencer, the TIB82S167B, was programmed for use as the timing controller.

In this example, refresh requests ($\overline{\text{REFREQ}}$) are generated every 155 clock cycles. The timing controller will perform the refresh cycle ($\overline{\text{RAS}}$ only) immediately if the processor is not in the middle of an access cycle. If the controller is in the middle of an access cycle, the refresh cycle will be delayed until the access cycle is complete. If the controller is asked to perform an access cycle during a refresh, the access cycle will begin immediately after the refresh cycle is completed. Address bit A23 indicates whether the access requested is a memory access (A23 = L) or an I/O access (A23 = H). The timing controller will perform an access cycle only if Address bit A23 is low. Figure 2-10 is a timing diagram of the refresh/access cycle as explained above. To implement memory scrubbing, the controller must execute a read/write cycle during the refresh cycle and then place the 'ALS6301 in the memory scrubbing mode. (This example executes a $\overline{\text{RAS}}$ only refresh.) The flowchart in Figure 2-11 outlines the required functionality of the timing controller. This flowchart was used along with the timing diagrams in Figures 2-9 and 2-10 to design the timing controller.



†Start sequence when AS = H, CLK = H, $\overline{\text{REFREQ}}$ = H, STATE = 0
‡Return to ST0 if A23 is high

Figure 2-9. 68000 Access Cycle



† Start sequence when $\overline{\text{REFREQ}}$ = L, STATE = 0
‡ Return to STATE 0 if REQ = H or A23 = H
§ REQ is internal status register used to store an access request during a refresh cycle. (If AS = H during refresh cycle ST1-ST5)

Figure 2-10. Refresh/Access Cycle

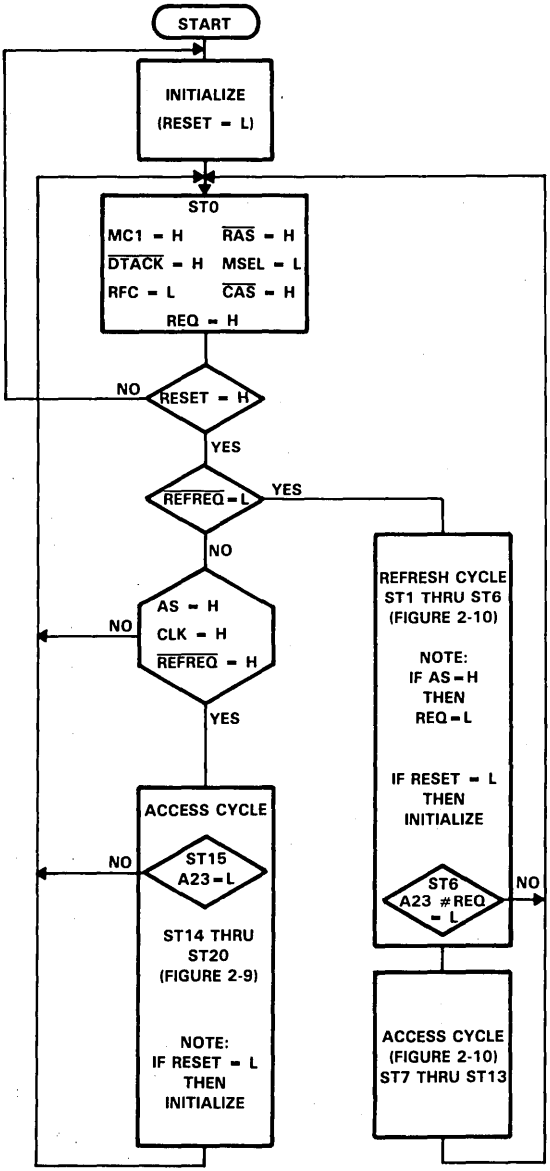


Figure 2-11. 'ALS6301, 'ALS6302 Memory Timing Controller Flow Chart

2.3.4 Refresh Timer Details

Figure 2-12 shows the actual circuit implementation of the refresh and memory timing controller. The refresh timer signals the controller whenever it is time to execute a refresh cycle. As required by memory, every row (512 on the TMS4C1025 DRAM) must be addressed every 8 ms. This implies that one row should be refreshed at least once every 15.6 ms. With a 10-MHz system clock, the refresh timer should use approximately a division factor of 155. This results in a refresh request every 15.3 ms. The refresh complete input (RFC) is used to signal the refresh timer that the refresh has been completed. It is important that the timer not stop so that the 8 ms memory requirement is maintained.

The TIBPAL22V10 circuit shown in Figure 2-12 is used to generate the refresh request signal every 155 clock cycles. The refresh request signal (active low) will remain active (low) until a refresh complete (RFC) signal is received from the timing controller. During a system reset, the refresh request output is set to a high logic level. When using different clock rates or memory sizes, the division circuit in the refresh timer should be adjusted accordingly.

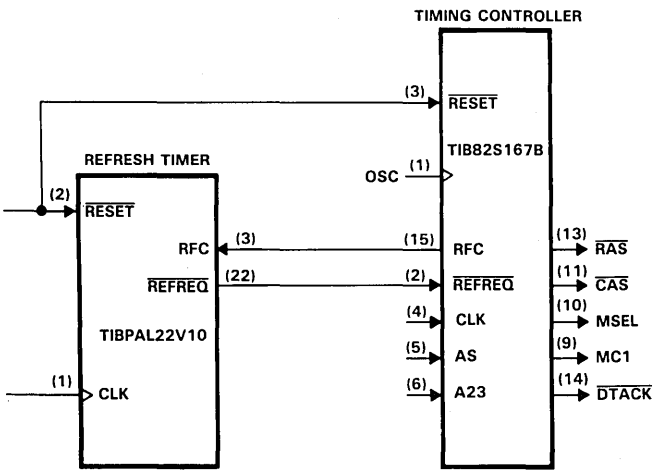


Figure 2-12. Refresh/Memory Timing Controller

2.3.5 Programmable Logic Designs

As mentioned previously, the timing controller, byte controller, and the refresh timer used in this example are created using programmable logic. ABEL™ and CUPL™ software packages have been used to reduce equations and generate the fuse maps needed to program these devices. The files used to generate the fuse maps have been included for reference at the end of this application report. Test vectors are included with the device files so software simulation can be performed on the computer. If the proper instruction is provided, the software will attach the test vectors to the end of the fuse map. This allows programming equipment to run a functional test on each device immediately after programming. To help familiarize the reader with these software tools, the timing controller design was done in both ABEL™ and CUPL™.

The TIB82S167B field programmable sequencer shown in Figure 2-12 is configured as a state machine to execute the flow chart shown in Figure 2-11. As shown in the flowchart, the timing controller is initialized by taking the reset input low. From the initialization state, state 0, the timing controller can perform either an access or a refresh cycle depending on the signals AS, CLK, and $\overline{\text{REFREQ}}$. If an access is requested (AS = H) during a refresh cycle, an internal status register, REQ, will flag the request and as soon as the refresh cycle is completed, an access cycle will be started. At the start of an access cycle, the timing controller checks the state of the A23 address bit. If A23 is high, indicating an I/O access, the timing controller terminates the access cycle and returns to state 0.

As seen in Figures 2-9, 2-10, and 2-11, a state, ST0-ST30, has been assigned to each clock cycle. The appended ABEL™ and CUPL™ files can be easily understood by comparing the state equations to the states shown in these figures. Since the only difference between the 'ALS6301 and the 'ALS6302 is that the $\overline{\text{RAS}}$I and the $\overline{\text{CAS}}$I inputs are active-high instead of active-low, a slight modification to the timing controller software file will allow an 'ALS6302 to be used instead of an 'ALS6301. The TIBPAL22V10 refresh timer and the TIBPAL16L8 byte controller designs are straight forward and easily achieved as can be seen in the appended files.

In applications with different systems timings, the ABEL™ and CUPL™ files can be modified to fit the processor requirements. A preprogrammed sample of the timing controller, refresh timer and byte controller can be obtained by calling LSI/PAL/PROM Applications, 214/995-2980. If a basic understanding of programmable logic is needed, see the Texas Instruments Field Programmable Logic Applications note.

2.3.6 Summary

The 'ALS6301 and 'ALS6302, coupled with programmable logic, offer the system designer a solution to high speed dynamic memory requirements. Programmable logic allows the designer to tailor the timing controller to a selected processor and memory. In many cases, the generation of a high speed timing controller from programmable logic will allow the designer to use slower DRAMs without affecting system speed. This results in lower total system cost because of the large number of memory devices used.

2.3.7 ABEL™ Files

module DMC S167

```
module DMC_S167 flag '-KY','-R2' "leave unused OR terms connected
title 'DYNAMIC MEMORY CONTROLLER FOR THE ALS6301 APPLICATION
Loren Schiele   Texas Instruments,  August 15, 1986'

        DMC  device 'F82S167';

" Input pin assignments

OSC     pin   1;                        " OSCILLATOR
REFREQ  pin   2;                        " REFRESH REQUEST
RESET   pin   3;                        " RESET - INITIALIZES WHEN LOW
CLK     pin   4;                        " OSC DIVIDED BY 2
AS      pin   5;                        " ADDRESS STROBE
A23     pin   6;                        " MOST SIGNIFICANT ADDRESS BIT
GND     pin  16;                        " PIN 16 MUST BE TIED LOW

" Output pin and node assignments

MC1     pin   9;  MC1_R    node 25;     " MODE CONTROL
MSEL    pin  10;  MSEL_R   node 26;     " MULTIPLEXER SELECT
CAS     pin  11;  CAS_R    node 27;     " COLUMN ADDRESS STROBE
RAS     pin  13;  RAS_R    node 28;     " ROW ADDRESS STROBE
DTACK   pin  14;  DTACK_R  node 29;     " DATA ACKNOWLEDGE
RFC     pin  15;  RFC_R    node 30;     " REFRESH COMPLETE

" Internal status and counter nodes

P0      node 36;  P0_R     node 42;     " INTERNAL COUNTER REGISTER
P1      node 35;  P1_R     node 41;     " INTERNAL COUNTER REGISTER
P2      node 34;  P2_R     node 40;     " INTERNAL COUNTER REGISTER
P3      node 33;  P3_R     node 39;     " INTERNAL COUNTER REGISTER
P4      node 32;  P4_R     node 38;     " INTERNAL COUNTER REGISTER
REQ     node 31;  REQ_R    node 37;     " REFRESH REQUEST STATUS REGISTER

" Define Set and Reset inputs to output and status flip-flops
MC1_    = [MC1,MC1_R];
MSEL_   = [MSEL,MSEL_R];
CAS_    = [CAS,CAS_R];
RAS_    = [RAS,RAS_R];
DTACK_  = [DTACK,DTACK_R];
RFC_    = [RFC,RFC_R];
REQ_    = [REQ,REQ_R];

" 'high' and 'low' are used to set or reset the output and status
"  registers.  Example: MC1_ := high & RESET; will cause pin 9 to
"  go high on the next clock edge if input pin 3 is high.

high    = [ 1,  0];
low     = [ 0,  1];
Count   = [P4,P3,P2,P1,P0];             " STATE REGISTER SET DEFINED
Cnt     = [P4,P3,P2,P1,P0];             " STATE REGISTER SET DEFINED
H,L,clk,X = 1, 0, .C., .X.;

@page
```

```
state_diagram Count                                          " NEXT
        State 0:        case                                 " STATE
                         !REFREQ   & RESET                    : 1;
                          REFREQ   & AS & CLK & RESET         :14;
                          REFREQ   & (!AS # !CLK)             : 0;
                        endcase;

" REFRESH TIMING CYCLE
        State 1:        MC1_  := low  & RESET;
                        REQ_  := low  & (AS & RESET);
                        case     RESET==1                    : 2; endcase;
        State 2:        RFC_  := high & RESET;
                        RAS_  := low  & RESET;
                        REQ_  := low  & (AS & RESET);
                        case     RESET==1                    : 3; endcase;
        State 3:        REQ_  := low  & (AS & RESET);
                        case     RESET==1                    : 4; endcase;
        State 4:        RFC_  := low  & RESET;
                        REQ_  := low  & (AS & RESET);
                        case     RESET==1                    : 5; endcase;
        State 5:        RAS_  := high;
                        REQ_  := low  & (AS & RESET);
                        case     RESET == 1                  : 6; endcase;

" DETERMINE IF ACCESS HAS BEEN REQUESTED
        State 6:        REQ_  := high & A23;
                        MC1_  := high & RESET;
                        case     REQ # A23                   : 0;
                                !A23  & !REQ & RESET         : 7;
                        endcase;

" ACCESS AFTER REFRESH
        State 7:        RAS_  := low  & RESET;
                        case     RESET==1                    : 8; endcase;
        State 8:        REQ_  := high & RESET;
                        MSEL_ := high & RESET;
                        case     RESET==1                    : 9; endcase;
        State 9:        CAS_  := low  & RESET;
                        DTACK_:= low  & RESET;
                        case     RESET==1                    :10; endcase;
        State 10:       case     RESET==1                    :11; endcase;

        State 11:       case     RESET==1                    :12; endcase;

        State 12:       case     RESET==1                    :13; endcase;

        State 13:       RAS_  := high;
                        MSEL_ := low;
                        CAS_  := high;
                        DTACK_:= high;
                        case     RESET==1                    : 0; endcase;
@page
```

```
" ACCESS TIMING CYCLE
        State 14:       case     RESET==1              :15; endcase;
        State 15:       RAS_  := low  & !A23 & RESET;
                        case A23 == 1                  : 0;
                            !A23 & RESET               :16;
                        endcase;
        State 16:       MSEL_ := high & RESET;
                        DTACK_:= low  & RESET;
                        case     RESET==1              :17; endcase;
        State 17:       CAS_  := low  & RESET;
                        case     RESET==1              :18; endcase;
        State 18:       case     RESET==1              :19; endcase;
        State 19:       case     RESET==1              :20; endcase;
        State 20:       RAS_  := high;
                        MSEL_ := low;
                        CAS_  := high;
                        DTACK_:= high;
                        case     RESET==1              : 0; endcase;

equations
        enable MC1 = 1;  "always enabled, pin 19 is preset

" INITIALIZATION WHEN RESET IS LOW
        [ MC1,RAS,DTACK,REQ,CAS]                  :=  !RESET;
        [ P0_R,P1_R,P2_R,P3_R,P4_R,MSEL_R,RFC_R] :=  !RESET;

test_vectors ' REFRESH WITH ACCESS FOLLOWING'

([GND,OSC,RESET,REFREQ,CLK,AS,A23] -> [MC1,MSEL,CAS,RAS,DTACK,RFC,REQ,Cnt])
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   0  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 1 ];
 [ 0 ,clk,  1  ,   X  , X , 1, X ] -> [ L ,  L , H , H ,  H  , L , L , 2 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ L ,  L , H , L ,  H  , H , L , 3 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ L ,  L , H , L ,  H  , H , L , 4 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ L ,  L , H , L ,  H  , L , L , 5 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ L ,  L , H , H ,  H  , L , L , 6 ];
 [ 0 ,clk,  1  ,   X  , X , X, 0 ] -> [ H ,  L , H , H ,  H  , L , L , 7 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  L , H , L ,  H  , L , L , 8 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , H , L ,  H  , L , H , 9 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,10 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,11 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,12 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,13 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 0 , 0, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 0 , 1, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 1 , 0, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];

test_vectors ' REFRESH WITHOUT ACCESS FOLLOWING'

([GND,OSC,RESET,REFREQ,CLK,AS,A23] -> [MC1,MSEL,CAS,RAS,DTACK,RFC,REQ,Cnt])
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   0  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 1 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , H ,  H  , L , H , 2 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , L ,  H  , H , H , 3 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , L ,  H  , H , H , 4 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , L ,  H  , L , H , 5 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ L ,  L , H , H ,  H  , L , H , 6 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   0  , X , 0, X ] -> [ H ,  L , H , H ,  H  , L , H , 1 ];
@page
```

```
test_vectors   REFRESH WITH ACCESS REQUEST BUT DATA NOT IN DRAM (A23=H) '

([GND,OSC,RESET,REFREQ,CLK,AS,A23] -> [MC1,MSEL,CAS,RAS,DTACK,RFC,REQ,Cnt])
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   0  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 1 ];
 [ 0 ,clk,  1  ,   X  , X , 1, X ] -> [ L ,  L , H , H ,  H  , L , L , 2 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , L ,  H  , H , L , 3 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , L ,  H  , H , L , 4 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , L ,  H  , L , L , 5 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , H ,  H  , L , L , 6 ];
 [ 0 ,clk,  1  ,   X  , X , 0, 1 ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 0 , 0, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];

test_vectors ' ACCESS TIMING CYCLE '

([GND,OSC,RESET,REFREQ,CLK,AS,A23] -> [MC1,MSEL,CAS,RAS,DTACK,RFC,REQ,Cnt])
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 1 , 1, X ] -> [ H ,  L , H , H ,  H  , L , H ,14 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H ,15 ];
 [ 0 ,clk,  1  ,   X  , X , X, 0 ] -> [ H ,  L , H , L ,  H  , L , H ,16 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , H , L ,  L  , L , H ,17 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,18 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,19 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,20 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 0 , 0, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];

test_vectors ' ACCESS TIMING CYCLE BUT DATA NOT IN DRAM (A23=H) '

([GND,OSC,RESET,REFREQ,CLK,AS,A23] -> [MC1,MSEL,CAS,RAS,DTACK,RFC,REQ,Cnt])
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 1 , 1, X ] -> [ H ,  L , H , H ,  H  , L , H ,14 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H ,15 ];
 [ 0 ,clk,  1  ,   X  , X , X, 1 ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 0 , 0, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];

test_vectors ' RESET DURING ACCESS TIMING CYCLE '

([GND,OSC,RESET,REFREQ,CLK,AS,A23] -> [MC1,MSEL,CAS,RAS,DTACK,RFC,REQ,Cnt])
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 1 , 1, X ] -> [ H ,  L , H , H ,  H  , L , H ,14 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H ,15 ];
 [ 0 ,clk,  1  ,   X  , X , X, 0 ] -> [ H ,  L , H , L ,  H  , L , H ,16 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , H , L ,  L  , L , H ,17 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,18 ];
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];

end DMC_S167
```

module TIMER154

```
module  TIMER154 flag '-r2','-f'
title  'REFRESH TIMER
        LOREN SCHIELE  TEXAS INSTRUMENTS, DALLAS, 08/15/86'

        T154  DEVICE   'P22V10';

"input declarations

CLK             pin 1;              "  SYSTEM CLOCK
RESET           pin 2;              "  RESETS WHEN LOW
RFC             pin 3;              "  REFRESH COMPLETE

"output declarations

Q0,Q1,Q2,Q3    pin 14,15,16,17;     "  COUNTER STATES
Q4,Q5,Q6,Q7    pin 18,19,20,21;     "  COUNTER STATES
REFREQ_        pin 22;              "  REFRESH REQUEST - ACTIVE LOW

"intermediate variables

CNT_154_   =  !Q0 & Q1 & !Q2 & Q3 & Q4 & !Q5 & !Q6 & Q7;
SCLR       =  !RESET # CNT_154_;
count      = [Q7,Q6,Q5,Q4,Q3,Q2,Q1,Q0];
C,H,L,X    = .C.,1,0,.X.;

equations

REFREQ_   :=  RFC # !CNT_154_ &  REFREQ_ # !RESET;
Q0        :=  (!Q0 ) & !SCLR;
Q1        :=  ( Q1 $  Q0) & !SCLR;
Q2        :=  ( Q2 $  Q1 &  Q0) & !SCLR;
Q3        :=  ( Q3 $ (Q2 &  Q1 &  Q0)) & !SCLR;
Q4        :=  ( Q4 $ (Q3 &  Q2 &  Q1 &  Q0)) & !SCLR;
Q5        :=  ( Q5 $ (Q4 &  Q3 &  Q2 &  Q1 &  Q0)) & !SCLR;
Q6        :=  ( Q6 $ (Q5 &  Q4 &  Q3 &  Q2 &  Q1 &  Q0)) & !SCLR;
Q7        :=  ( Q7 $ (Q6 &  Q5 &  Q4 &  Q3 &  Q2 &  Q1 &  Q0)) & !SCLR;

test_vectors              ([RESET,CLK,RFC] -> [count,REFREQ_])
                           [  0  , C , 0 ] -> [  0  ,   H   ];
@CONST cnt = 1;
@REPEAT 154 {              [  1  , C , 0 ] -> [ cnt ,   H   ];
@CONST cnt = cnt + 1;}
                           [  1  , C , 0 ] -> [  0  ,   L   ];
@CONST cnt = 1;
@REPEAT 20  {              [  1  , C , 0 ] -> [ cnt ,   L   ];
@CONST cnt = cnt + 1;}
                           [  1  , C , 1 ] -> [ 21  ,   H   ];
                           [  1  , C , 0 ] -> [ 22  ,   H   ];
                           [  1  , C , X ] -> [ 23  ,   H   ];
                           [  0  , C , X ] -> [  0  ,   H   ];
end TIMER154
```

2.3.8 CUPL™ Files

DYNAMIC MEMORY CONTROLLER

```
Partno          DMC-S167;
Name            DMC-S167;
Date            08/15/86;
Revision        01;
Designer        SCHIELE;
Company         TEXAS INSTRUMENTS;
Assembly        None;
Location        DALLAS, TEXAS;
/*****************************************************************/
/*                  DYNAMIC MEMORY CONTROLLER                    */
/*                        FOR ALS6301                            */
/*****************************************************************/
/* Allowable Target Device Types: TIB82S167B                     */
/*****************************************************************/

/**  Inputs  **/
pin 1 =  OSC;              /*  OSCILLATOR                       */
pin 2 = REFREQ;            /*  REFRESH REQUEST                  */
pin 3 = RESET;             /*  RESET - INITIALIZES WHEN LOW     */
pin 4 = CLK;               /*  OSC DIVIDED BY 2                 */
pin 5 = AS;                /*  ADDRESS STROBE                   */
pin 6 = A23_;              /*  MOST SIGNIFICANT ADDRESS BIT     */
pin 16 = GND;              /*  PIN 16 MUST BE TIED LOW          */

/**  Outputs  **/
pin  9 = MCI_;             /*  MODE CONTROL                     */
pin 10 = MSEL;             /*  MULTIPLEXER SELECT               */
pin 11 = CAS;              /*  COLUMN ADDRESS STROBE            */
pin 13 = RAS;              /*  ROW ADDRESS STOBE                */
pin 14 = DTACK;            /*  DATA ACKNOWLEDGE                 */
pin 15 = RFC;              /*  REFRESH COMPLETE                 */

/** Internal Node Group  -   State bits declared as nodes      **/
node [REQ,P4_,P3_,P2_,P1_,P0_];

/** Declarations and Intermediate Variable Definitions         **/
Field State  = [P4_,P3_,P2_,P1_,P0_];

$define  ST0 'b'00000
$define  ST1 'b'00001
$define  ST2 'b'00010
$define  ST3 'b'00011
$define  ST4 'b'00100
$define  ST5 'b'00101
$define  ST6 'b'00110
$define  ST7 'b'00111
$define  ST8 'b'01000
$define  ST9 'b'01001
$define ST10 'b'01010
$define ST11 'b'01011
$define ST12 'b'01100
$define ST13 'b'01101
$define ST14 'b'01110
$define ST15 'b'01111
$define ST16 'b'10000
$define ST17 'b'10001
$define ST18 'b'10010
$define ST19 'b'10011
$define ST20 'b'10100
```

```
/** Logic Equations **/

Sequence State
{Present ST0 IF  RESET & !REFREQ            NEXT ST1;
             IF  RESET &  REFREQ & AS & CLK NEXT ST14;
             DEFAULT                        NEXT ST0;

/*  REFRESH TIMING CYCLE */
Present ST1 IF  AS & RESET  NEXT ST2  OUT [!MC1_,!REQ];
            IF  RESET       NEXT ST2  OUT [!MC1_];
Present ST2 IF  AS & RESET  NEXT ST3  OUT [ RFC,!RAS,!REQ];
            IF  RESET       NEXT ST3  OUT [ RFC,!RAS];
Present ST3 IF  AS & RESET  NEXT ST4  OUT [!REQ];
            IF  RESET       NEXT ST4;
Present ST4 IF  AS & RESET  NEXT ST5  OUT [!RFC,!REQ];
            IF  RESET       NEXT ST5  OUT [!RFC];
Present ST5 IF  AS & RESET  NEXT ST6  OUT [ RAS,!REQ];
            IF  RESET       NEXT ST6  OUT [ RAS];
/** DETERMINE IF ACCESS HAS BEEN REQUESTED **/
Present ST6 IF  A23_ # REQ  NEXT ST0  OUT [ MC1_,REQ];
            IF !A23_ & RESET & !REQ NEXT ST7 OUT [ MC1_];

/** ACCESS AFTER REFRESH **/
Present ST7  IF  RESET      NEXT ST8  OUT [!RAS];
Present ST8  IF  RESET      NEXT ST9  OUT [ REQ, MSEL];
Present ST9  IF  RESET      NEXT ST10 OUT [!CAS,!DTACK];
Present ST10 IF  RESET      NEXT ST11;
Present ST11 IF  RESET      NEXT ST12;
Present ST12 IF  RESET      NEXT ST13;
Present ST13                NEXT ST0  OUT [ RAS,!MSEL, CAS, DTACK];

/** ACCESS TIMING CYCLE **/
Present ST14 IF  RESET      NEXT ST15;
Present ST15 IF  A23_       NEXT ST0;
             IF !A23_ & RESET NEXT ST16 OUT [!RAS];
Present ST16 IF  RESET      NEXT ST17 OUT [ MSEL,!DTACK];
Present ST17 IF  RESET      NEXT ST18 OUT [!CAS];
Present ST18 IF  RESET      NEXT ST19;
Present ST19 IF  RESET      NEXT ST20;
Present ST20                NEXT ST0  OUT [ RAS,!MSEL, CAS, DTACK];}

APPEND MC1_.s  = !RESET;  APPEND REQ.s  = !RESET;  APPEND RFC.r = !RESET;
APPEND RAS.s   = !RESET;  APPEND MSEL.r = !RESET;  APPEND CAS.s = !RESET;
APPEND DTACK.s = !RESET;  APPEND P0_.r  = !RESET;  APPEND P1_.r = !RESET;
APPEND P2_.r   = !RESET;  APPEND P3_.r  = !RESET;  APPEND P4_.r = !RESET;
```

DYNAMIC MEMORY SIMULATION

```
Partno          DMC-S167;
Name            DMC-S167;
Date            08/15/86;
Revision        01;
Designer        SCHIELE;
Company         TEXAS INSTRUMENTS;
Assembly        None;
Location        DALLAS, TEXAS;
/*************************************************************/
/*                  DYNAMIC TIMING CONTROLLER                */
/*                       SIMULATION FILE                     */
/*                         FOR ALS6301                       */
/*************************************************************/
/* Allowable Target Device Types: TIB82S167B                 */
/*************************************************************/

ORDER:  GND,%3,OSC,%3,RESET,%6,REFREQ,%4,CLK,%3,AS,%2,A23_,%6,
        MC1_,%4,MSEL,%3,CAS,%3,RAS,%4,DTACK,%4,RFC,%4,REQ;

VECTORS:
$msg" REFRESH WITH ACCESS FOLLOWING";
$msg"     ";
$msg"     ------------ INPUT -------------   -------- OUTPUT ---------- ACCESS";
$msg"    GND OSC RESET REFREQ CLK AS A23    MC1 MSEL CAS RAS DTACK RFC  REQ";
$msg"    ------------------------------------------------------------------";
/*RESET*/ 0   C    0      X    X   X  X      H    L   H   H    H     L    H
/* ST0*/  0   C    1      0    X   X  X      H    L   H   H    H     L    H
/* ST1*/  0   C    1      X    X   1  X      L    L   H   H    H     L    L
/* ST2*/  0   C    1      X    X   X  X      L    L   H   L    H     H    L
/* ST3*/  0   C    1      X    X   X  X      L    L   H   L    H     H    L
/* ST4*/  0   C    1      X    X   X  X      L    L   H   L    H     L    L
/* ST5*/  0   C    1      X    X   X  X      L    L   H   H    H     L    L
/* ST6*/  0   C    1      X    X   X  0      H    L   H   H    H     L    L
/* ST7*/  0   C    1      X    X   X  X      H    L   H   L    H     L    L
/* ST8*/  0   C    1      X    X   X  X      H    H   H   L    H     L    H
/* ST9*/  0   C    1      X    X   X  X      H    H   L   L    L     L    H
/*ST10*/  0   C    1      X    X   X  X      H    H   L   L    L     L    H
/*ST11*/  0   C    1      X    X   X  X      H    H   L   L    L     L    H
/*ST12*/  0   C    1      X    X   X  X      H    H   L   L    L     L    H
/*ST13*/  0   C    1      X    X   X  X      H    L   H   H    H     L    H
/*ST0 */  0   C    1      1    0   0  X      H    L   H   H    H     L    H
/*ST0 */  0   C    1      1    0   1  X      H    L   H   H    H     L    H
/*ST0 */  0   C    1      1    1   0  X      H    L   H   H    H     L    H

$msg"     ";
$msg"     ";
$msg"REFRESH WITHOUT ACCESS FOLLOWING";
$msg"     ";
$msg"     ------------ INPUT -------------   -------- OUTPUT ---------- ACCESS";
$msg"    GND OSC RESET REFREQ CLK AS A23    MC1 MSEL CAS RAS DTACK RFC  REQ  ";
$msg"    ------------------------------------------------------------------";
/*RESET*/ 0   C    0      X    X   X  X      H    L   H   H    H     L    H
/* ST0*/  0   C    1      0    X   X  X      H    L   H   H    H     L    H
/* ST1*/  0   C    1      X    X   0  X      L    L   H   H    H     L    H
/* ST2*/  0   C    1      X    X   0  X      L    L   H   L    H     H    H
/* ST3*/  0   C    1      X    X   0  X      L    L   H   L    H     H    H
/* ST4*/  0   C    1      X    X   0  X      L    L   H   L    H     L    H
/* ST5*/  0   C    1      X    X   0  X      L    L   H   H    H     L    H
/* ST6*/  0   C    1      X    X   X  0      H    L   H   H    H     L    H
/* ST0*/  0   C    1      X    X   0  X      H    L   H   H    H     L    H
```

```
$msg"     ";
$msg"     ";
$msg"REFRESH WITH ACCESS REQUEST BUT DATA NOT IN DRAM (A23=H)";
$msg"     ";
$msg"     ------------ INPUT -------------    -------- OUTPUT ---------- ACCESS";
$msg"     GND OSC RESET REFREQ CLK AS A23     MCI MSEL CAS RAS DTACK RFC  REQ  ";
$msg"     ---------------------------------------------------------------------";
/*RESET*/ 0   C    0      X    X   X  X       H    L   H   H    H     L    H
/* ST0*/  0   C    1      0    X   X  X       H    L   H   H    H     L    H
/* ST1*/  0   C    1      X    X   1  X       L    L   H   H    H     L    L
/* ST2*/  0   C    1      X    X   0  X       L    L   H   L    H     H    L
/* ST3*/  0   C    1      X    X   0  X       L    L   H   L    H     H    L
/* ST4*/  0   C    1      X    X   0  X       L    L   H   L    H     L    L
/* ST5*/  0   C    1      X    X   0  X       L    L   H   H    H     L    L
/* ST6*/  0   C    1      X    X   0  1       H    L   H   H    H     L    H
/* ST0*/  0   C    1      1    0   0  X       H    L   H   H    H     L    H

$msg"     ";
$msg"     ";
$msg"ACCESS TIMING CYCLE ";
$msg"     ";
$msg"     ------------ INPUT -------------    -------- OUTPUT ---------- ACCESS";
$msg"     GND OSC RESET REFREQ CLK AS A23     MCI MSEL CAS RAS DTACK RFC  REQ  ";
$msg"     ---------------------------------------------------------------------";
/*RESET*/ 0   C    0      X    X   X  X       H    L   H   H    H     L    H
/*ST0 */  0   C    1      1    1   1  X       H    L   H   H    H     L    H
/*ST14*/  0   C    1      X    X   X  X       H    L   H   H    H     L    H
/*ST15*/  0   C    1      X    X   X  0       H    L   H   L    H     L    H
/*ST16*/  0   C    1      X    X   X  X       H    H   H   L    L     L    H
/*ST17*/  0   C    1      X    X   X  X       H    H   L   L    L     L    H
/*ST18*/  0   C    1      X    X   X  X       H    H   L   L    L     L    H
/*ST19*/  0   C    1      X    X   X  X       H    H   L   L    L     L    H
/*ST20*/  0   C    1      X    X   X  X       H    L   H   H    H     L    H
/*ST0 */  0   C    1      1    0   0  X       H    L   H   H    H     L    H

$msg"     ";
$msg"     ";
$msg"ACCESS TIMING CYCLE BUT DATA NOT IN DRAM (A23=H)";
$msg"     ";
$msg"     ------------ INPUT -------------    -------- OUTPUT ---------- ACCESS";
$msg"     GND OSC RESET REFREQ CLK AS A23     MCI MSEL CAS RAS DTACK RFC  REQ  ";
$msg"     ---------------------------------------------------------------------";
/*ST0 */  0   C    1      1    1   1  X       H    L   H   H    H     L    H
/*ST14*/  0   C    1      X    X   X  X       H    L   H   H    H     L    H
/*ST15*/  0   C    1      X    X   X  1       H    L   H   H    H     L    H
/*ST0 */  0   C    1      1    0   0  X       H    L   H   H    H     L    H

$msg"     ";
$msg"     ";
$msg"RESET DURING ACCESS TIMING CYCLE ";
$msg"     ";
$msg"     ------------ INPUT -------------    -------- OUTPUT ---------- ACCESS";
$msg"     GND OSC RESET REFREQ CLK AS A23     MCI MSEL CAS RAS DTACK RFC  REQ  ";
$msg"     ---------------------------------------------------------------------";
/*RESET*/ 0   C    0      X    X   X  X       H    L   H   H    H     L    H
/*ST0 */  0   C    1      1    1   1  X       H    L   H   H    H     L    H
/*ST14*/  0   C    1      X    X   X  X       H    L   H   H    H     L    H
/*ST15*/  0   C    1      X    X   X  0       H    L   H   L    H     L    H
/*ST16*/  0   C    1      X    X   X  X       H    H   H   L    L     L    H
/*ST17*/  0   C    1      X    X   X  X       H    H   L   L    L     L    H
/*ST18*/  0   C    0      X    X   X  X       H    L   H   H    H     L    H
/*ST0 */  0   C    0      X    X   X  X       H    L   H   H    H     L    H
/*ST0 */  0   C    0      X    X   X  X       H    L   H   H    H     L    H
```

BYTE CONTROLLER

```
Partno          BYTE_CON;
Name            BYTE_CON;
Date            08/15/86;
Revision        01;
Designer        SCHIELE;
Company         TEXAS INSTRUMENTS;
Assembly        None;
Location        DALLAS, TEXAS;
/*****************************************************************/
/*                      BYTE CONTROLLER                          */
/*              FOR ALS6301/MC68000L10 APPLICATION               */
/*****************************************************************/
/* Allowable Target Device Types: TIBPAL16L8                     */
/*****************************************************************/
/**  Inputs  **/
pin 1 = CAS0;           /*  CAS BANK SELECT                      */
pin 2 = CAS1;           /*       "                               */
pin 3 = CAS2;           /*       "                               */
pin 4 = CAS3;           /*       "                               */
pin 5 = LDS;            /*  LOWER DATA STROBE                    */
pin 6 = UDS;            /*  UPPER DATA STROBE                    */

/**  Outputs  **/
pin 12 = UCAS0;         /*  UPPER BYTE SELECT - BANK 0           */
pin 13 = LCAS0;         /*  LOWER BYTE SELECT - BANK 0           */
pin 14 = UCAS1;         /*  UPPER BYTE SELECT - BANK 1           */
pin 15 = LCAS1;         /*  LOWER BYTE SELECT - BANK 1           */
pin 16 = UCAS2;         /*  UPPER BYTE SELECT - BANK 2           */
pin 17 = LCAS2;         /*  LOWER BYTE SELECT - BANK 2           */
pin 18 = UCAS3;         /*  UPPER BYTE SELECT - BANK 3           */
pin 19 = LCAS3;         /*  LOWER BYTE SELECT - BANK 3           */

/*  equations     */
UCAS0  = CAS0 # UDS;
LCAS0  = CAS0 # LDS;
UCAS1  = CAS1 # UDS;
LCAS1  = CAS1 # LDS;
UCAS2  = CAS2 # UDS;
LCAS2  = CAS2 # LDS;
UCAS3  = CAS3 # UDS;
LCAS3  = CAS3 # LDS;
```

BYTE CONTROLLER SIMULATION

```
Partno          BYTE_CON;
Name            BYTE_CON;
Date            08/15/86;
Revision        01;
Designer        SCHIELE;
Company         TEXAS INSTRUMENTS;
Assembly        None;
Location        DALLAS, TEXAS;
/*****************************************************************/
/*              BYTE CONTROLLER SIMULATION FILE                  */
/*            FOR ALS6301/MC68000L10  APPLICATION                */
/*****************************************************************/
/* Allowable Target Device Types: TIBPAL16L8                     */
/*****************************************************************/

ORDER:
CAS0,%2,CAS1,%2,CAS2,%2,CAS3,%3,LDS,%2,UDS,%4,LCAS0,%2,UCAS0,%2,
LCAS1,%2,UCAS1,%2,LCAS2,%2,UCAS2,%2,LCAS3,%2,UCAS3;

VECTORS:

$msg"      ----- INPUT -----     -------- OUTPUT --------   ";
$msg"                                L  U  L  U  L  U  L  U   ";
$msg"      C  C  C  C              C  C  C  C  C  C  C  C   ";
$msg"      A  A  A  A  L  U        A  A  A  A  A  A  A  A   ";
$msg"      S  S  S  S  D  D        S  S  S  S  S  S  S  S   ";
$msg"      0  1  2  3  S  S        0  0  1  1  2  2  3  3   ";
$msg"      ---------------------------------------------   ";
           1  1  1  1  X  X        H  H  H  H  H  H  H  H
           X  X  X  X  1  1        H  H  H  H  H  H  H  H

           0  1  1  1  0  0        L  L  H  H  H  H  H  H
           1  0  1  1  0  0        H  H  L  L  H  H  H  H
           1  1  0  1  0  0        H  H  H  H  L  L  H  H
           1  1  1  0  0  0        H  H  H  H  H  H  L  L

           0  1  1  1  0  1        L  H  H  H  H  H  H  H
           1  0  1  1  0  1        H  H  L  H  H  H  H  H
           1  1  0  1  0  1        H  H  H  H  L  H  H  H
           1  1  1  0  0  1        H  H  H  H  H  H  L  H

           0  1  1  1  1  0        H  L  H  H  H  H  H  H
           1  0  1  1  1  0        H  H  H  L  H  H  H  H
           1  1  0  1  1  0        H  H  H  H  H  L  H  H
           1  1  1  0  1  0        H  H  H  H  H  H  H  L
```

2.4 THCT4502B/MC68000L8 Interface

2.4.1 Introduction

This application report presents a circuit configuration which interfaces the MC68000L8 to DRAM memory via the THCT4502B dynamic RAM controller. The memory array is four banks of 256K-byte memory (TMS4256/4257) that provides a 1M byte deep system architecture.

Figure 2-13 is a schematic diagram of the circuit and Figure 2-14 a timing diagram for two consecutive read cycles. Figure 2-15 shows a write access, followed by a refresh, followed by a read-access grant. The THCT4502B uses the MC68000L8 system clock and requires no wait states on normal access cycles. When incorporating DRAMs and a DRAM controller into a microprocessor based system, the following timing specifications should be satisfied to guarantee a correct match between processor and memory.

ALE-to-Clock Relationship
DRAM Refresh Time
DRAM Precharge Time
Row Address Setup and Hold Time
Data Valid to Write Enable Time
Read Access Time

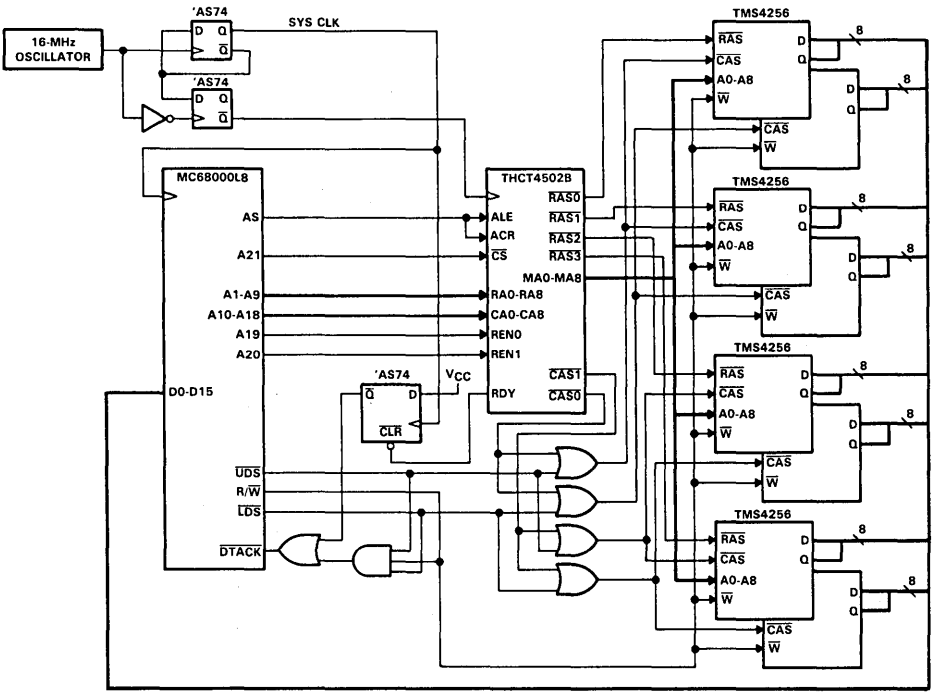


Figure 2-13. THCT4502B/MC68000L8 Interface Block Diagram

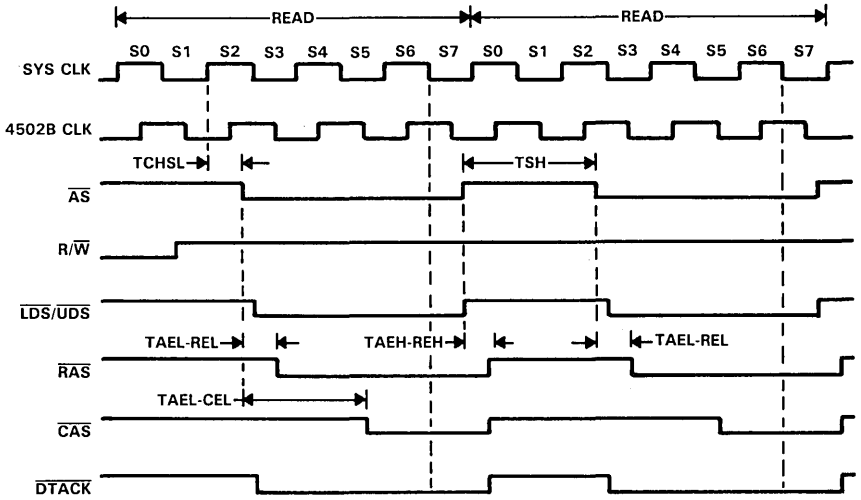


Figure 2-14. THCT4502B/MC68000L8 Read Cycle Timing Diagram

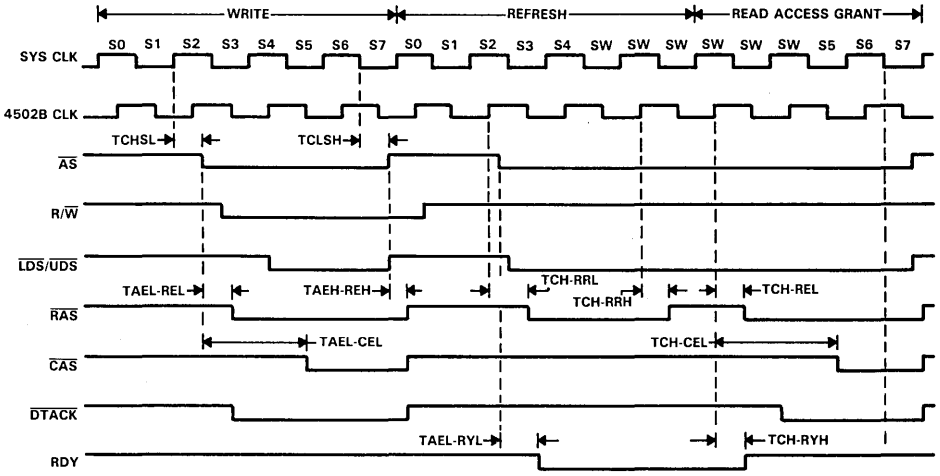


Figure 2-15. THCT4502B/MC68000L8 Write Access, Refresh, and Read Access Timing Diagram

2.4.2 ALE-to-Clock Relationship

When using the THCT4502B, the high-to-low transition of ALE should not occur between 15 ns before and 15 ns after the falling edge of the clock signal. This condition guarantees the proper selection between refresh and access cycles.

When connecting the Address Strobe (AS) of the MC68000 processor directly to ALE, ensure that the following condition is met.

$$15 < 0.5T - t_{CHSL}$$
$$15 < 0.5(125) - 60$$
$$15 < 2.5$$

At 8 MHz, this condition cannot be guaranteed. Therefore a circuit is required to shift the input phase of the THCT4502B clock signal by 90 degrees. As shown in Figure 2-13, this circuit can be built using standard 'AS74 D-type flip-flops. With the THCT4502B CLK shifted by 90 degrees, the new equation becomes:

$$15 < 0.5T + 0.25T - t_{CHSL}$$
$$15 < 0.5(125) + 0.25(125) - 60$$
$$15 < 33.75$$

It should be noted that all of the following equations take into account the 90 degree phase shift. At lower clock frequencies, such as 6 MHz, the AS signal can be directly connected to the THCT4502B and the phase shift circuits are not required.

2.4.3 DRAM Refresh Time

The refresh clock frequency is controlled by the strap input pins (TWST, FS1, and FS0) on the THCT4502B. Table 2-3 shows the strap configuration for the THCT4502B. At 8 MHz, with no wait states, setting TWST low, FS1 high, and FS0 high yields a refresh rate of 11.375 μs/row. The TMS4256/4257 requires that each of the 256 rows be refreshed at least once every 4 ms. With a refresh rate of 11.375 μs/row, the time required to refresh all 256 rows will be 2.9 ms. This easily satisfies the 4-ms refresh requirement.

Table 2-3. Refresh Clock Frequency Input Pin Strap Configuration

STRAP INPUT MODES			WAIT STATES FOR MEMORY ACCESS	REFRESH RATE	MINIMUM CLOCK FREQUENCY (MHz)	REFRESH FREQUENCY (kHz)	CLOCK CYCLES FOR EACH REFRESH
TWST	FS1	FS0					
L	L	L†	0	EXTERNAL	–	REFREQ	4
L	L	H	0	EXTERNAL	–	REFREQ	3
L	H	L	0	CLK ÷ 61	3.904	64-95‡	3
L	H	H	0	CLK ÷ 91	5.824	64-88§	4
H	L	L	1	CLK ÷ 61	3.904	64-95‡	3
H	L	H	1	CLK ÷ 91	5.824	64-75‡	4
H	H	L	1	CLK ÷ 106	6.784	64-73‡	4
H	H	H	1	CLK ÷ 121	7.744	64-83¶	4

† This strap configuration resets the Refresh Timer Circuitry.
‡ Upper figure in refresh frequency is the frequency that is produced if the minimum clock frequency of the next select state is used.
§ Refresh frequency if clock frequency is 8 MHz.
¶ Refresh frequency if clock frequency is 10 MHz.

2.4.4 DRAM Precharge Time

The precharge time is the time required between access cycles to allow internal nodes on the DRAM to charge to their correct reference levels. This is specified on the DRAM data sheet as $t_{W(RH)}$ min. As with most DRAMs, there is a choice of performance ranges. For the TMS4256/4257, $t_{W(RH)}$ ranges from 100 ns on the −12 device to 120 ns on the −20 device.

When using the THCT4502B, there are three precharge conditions which can occur during normal operation. Each condition must be checked to be sure the precharge condition is met. The following equations check these three conditions.

1. Access-to-Access cycle

   $t_{W(RH)} < t_{SH} - t_{AEH\text{-}REH} - t_{t(REH)} + t_{AEL\text{-}REL}$
   $t_{W(RH)} < 150 - 35 - 30 + 35$
   $t_{W(RH)} < 120$

2. Access-to-Refresh cycle

   $t_{W(RH)} < 1.5T + 0.25T + t_{CH\text{-}RRL} - t_{CLSH} - t_{AEH\text{-}REH} - t_{t(REH)}$
   $t_{W(RH)} < 1.5(125) + 0.25(125) + 50 - 70 - 35 - 30$
   $t_{W(RH)}$ h 133.75

3. Refresh-to-Access cycle

   $t_{W(RH)} < T - t_{CH\text{-}RRH} - t_{t(REH)} + t_{CH\text{-}REL}$
   $t_{W(RH)} < 125 - 30 - 30 + 45$
   $t_{W(RH)} < 110$

When the listed equations are correct, the THCT4502B guarantees the precharge condition for either the −12 or −15 TMS4256/4257 DRAMs.

2.4.5 Row Address Setup and Hold Time

To meet the row address setup-time requirement, the address must be present at the RA0-RA8 and CA0-CA8 inputs to the THCT4502B for at least 10 ns ($t_{AV\text{-}AEL}$) before ALE goes low. The row address setup time from the MC68000L8 is defined by the t_{AVSL} specification. At 8 MHz, t_{AVSL} is 30 ns minimum. This meets the THCT4502B specification. The row address setup time to the DRAM must also be satisfied. For the TMS4256/4257, $t_{su(RA)}$ is specified as 0-ns minimum. The following equation applies:

$0 \text{ ns} < t_{AVSL} + t_{AEL\text{-}REL} - t_{RAV\text{-}MAV}$
$0 \text{ ns} < 30 + 35 - 42$
$0 \text{ ns} < 23$

When the equation is correct, the THCT4502B guarantees the row address setup time to the DRAM. The row address hold time required by the TMS4256/4257 is 15 ns. This specification is guaranteed by the THCT4502B. From the data sheet, $t_{REL\text{-}MAX}$ is specified as 20 ns min.

2.4.6 Data Valid to Write Enable Setup Time

Data can be written into DRAM by two different methods. Depending upon the mode of operation, the falling edge of $\overline{CAS}$ or the the falling edge of $\overline{W}$ will strobe the data into memory. When $\overline{W}$ goes low prior to $\overline{CAS}$ going low, data out will remain in the high-impedance state for the entire cycle. This permits common input/output operation. This type of cycle is referred to as an early write cycle. When $\overline{W}$ goes low after $\overline{CAS}$ goes low, the type of cycle is referred to as delayed-write or read-modify-write cycle. To avoid bus contention, this operation requires a buffer between the Q outputs and the microprocessor.

The circuit shown in Figure 2-13 generates an early write cycle. Therefore, data valid to write enable needs to be referenced to the falling edge of $\overline{CAS}$. The TMS4256/4257 requirement for an early write cycle is $t_{su(WCL)}$, which is 0 ns minimum. The following equation applies:

$$0 \text{ ns} < t_{CHSL} + t_{AEL\text{-}CEL} - 0.5T - t_{CLDO}$$
$$0 \text{ ns} < 60 + 115 - 0.5(125) - 70$$
$$0 \text{ ns} < 42.5$$

When the equation is correct, the MC68000/THCT4502B combination guarantees that data will be valid before $\overline{CAS}$ goes low.

2.4.7 Read Access Time from CAS

When the microprocessor tries to read data from memory, the Read-Access-Time guarantees that data is available. When using the THCT4502B, there are two possible access situations. The most common is the normal access cycle. Another possible access situation is the access-grant cycle. The access-grant cycle occurs when an access cycle immediately follows a refresh cycle.

For the TMS4256/4257, access from $\overline{CAS}$ is specified as $t_{a(C)}$. When using the TMS4256/4257, three speed types are available for selection. The three speed types are as follows:

Speed type -12 $t_{a(CA)} = 60$ ns
Speed type -15 $t_{a(CA)} = 75$ ns
Speed type -20 $t_{a(CA)} = 100$ ns

The following equations apply to the circuit shown in Figure 2-14.

1. Normal Access Cycles

$$t_{a(C)} < 2.5T - t_{CHSL} - t_{AEL\text{-}CEL} - t_{t(CEL)} - t_{p(OR)} - t_{DICL}$$
$$t_{a(C)} < 2.5(125) - 60 - 115 - 20 - 15 - 15$$
$$t_{a(C)} < 87.5$$

2. Access Grant Cycles

$$t_{a(C)} < 2.5T - 0.25T - t_{CH\text{-}CEL} - t_{t(CEL)} - t_{p(OR)} - t_{DICL}$$
$$t_{a(C)} < 2.5(125) - 0.25(125) - 140 - 20 - 15 - 15$$
$$t_{a(C)} < 91.25$$

As shown by the equations, the only speed type that does not meet the access time requirement is the -20 device. The -12 and -15 devices both meet $t_{a(C)}$.

2.4.8 Other Considerations

The $\overline{DTACK}$ input on the MC68000L8 informs the microprocessor that data is available. Wait states are inserted by holding $\overline{DTACK}$ high. This process for the access-grant cycle is illustrated in Figure 2-15. If an access request occurs during a refresh cycle, the THCT4502B completes the refresh cycle, then finishes the access request. In this situation, the $\overline{DTACK}$ signal is held high until data is available. The AS74 flip-flop shown in Figure 2-13 is used to time the $\overline{DTACK}$ signal in relationship to the falling edge of S6.

On normal accesses, the RDY signal is high allowing either $\overline{UDS}$, $\overline{LDS}$ or R/$\overline{W}$ to force $\overline{DTACK}$ low. During write cycles, R/$\overline{W}$ will force $\overline{DTACK}$ low. During read cycles, $\overline{UDS}$ and/or $\overline{LDS}$ will force $\overline{DTACK}$ low. During access-grant cycles, the low RDY signal holds $\overline{DTACK}$ high until it is released.

2.4.9 Summary

This application report provides an example of how to interface the THCT4502B with the MC68000L8. The major design criteria has been calculated and checked against typical DRAM specifications. When using processor speeds lower than 8 MHz, the interface is simplified further because it is not necessary to shift the THCT4502B input clock frequencies. Additional design ideas can be obtained from an Applications Brief "TMS4500B/MC68000 INTERFACE", Texas Instruments publication SMCA008.

2.5 Programmer and Software Manufacturers Addresses†

2.5.1 Programmer Manufacturers Addresses

ECI Semiconductor
975 Comstock St.
Santa Clara, CA 95054
(408) 727-6562

DATA I/O
10525 Willows Rd. NE
Redmond, WA 98073-9746
(206) 881-6444

DIGITAL MEDIA
11770 Warner Ave. Suite 225
Fountain Valley, CA 92708
(714) 751-1373

Kontron Electronics
1230 Charleston Rd.
Mountain View, CA 94039-7230
(415) 965-7020

Stag Micro Systems
528-5 Weddell Drive
Sunnyvale, CA 94089
(408) 745-1991

Storey Systems
3201 N. Hwy 67, Suite E
Mesquite, TX 75150
(214) 270-4135

Structured Design
988 Bryant Way
Sunnyvale, CA 94087
(408) 988-0725

Sunrise Electronics
524 S. Vermont Avenue
Glendora, CA 91740
(818) 914-1926

Valley Data Sciences
2426 Charleston Rd.
Mountain View, CA 94043
(415) 968-2900

Varix
1210 Campbell Rd. Suite 100
Richardson, TX 75081
(214) 437-0777

Digelec
1602 Lawerence Ave. Suite 113
Ocean, NJ 07712
(201) 493-2420

2.5.2 Software Manufacturer Addresses

Assisted Technologies Division (CUPL)
Personal CAD Systems
1290 Parkmoor Avenue
San Jose, CA 95126
(408) 971-1300

DATA I/O (ABEL)
10525 Willows Rd. NE
Redmond, WA 98073-9746
(206) 881-6444

†Texas Instruments does not endorse or warrant the suppliers referenced.

3 Cache Memory Systems

3.1 Introduction

As the typical operating speeds of processors have increased to provide for the ever increasing need for computing power, the necessity of developing a memory hierarchy (the incorporation of two or more memory technologies in the same system) has become apparent. One of these memory technologies is selected on the basis of fast access time (with associated high cost per bit) to allow minimum system cycle time. The other technologies are chosen with the lowest possible cost per bit relative to speed in order to achieve the maximum system memory capacity. In a system with a multiple level hierarchy, the speed-to-cost relationship depends upon the frequency of access and the total memory requirement at that level. By proper use of this hierarchy through coordination of hardware, system software, and in some cases user software, the overall memory system will reflect the characteristics that approximate the fast access time of the fast memory technology and the low cost per bit of the low cost memory technology. Large computer systems have made use of this memory optimization technique to maintain very large data bases and high throughput (see Figure 3-1). Many smaller processor systems use this technique to allow mass storage of data, where a tape or a disk is the low-cost memory and Random Access Memory (RAM) is the fast memory technology.

Because of the increase in processor speeds, memory hierarchy is now extending to the RAM memory used in microcomputer systems. Typically, Dynamic RAM (DRAM) is used as the bulk or main memory and High-Speed Static RAM (HSS) serves as the fast-access memory. This HSS RAM is usually 1K to 8K words deep and serves as a fast buffer memory between the processor and the main memory. This small fast buffer memory is called "cache" memory because it is the storage location for a carefully selected portion of the data from the main memory. The addresses for that portion of memory currently in the buffer memory is saved in the cache tag RAM (a small memory that is used to store the addresses of the data that has been mapped to cache).

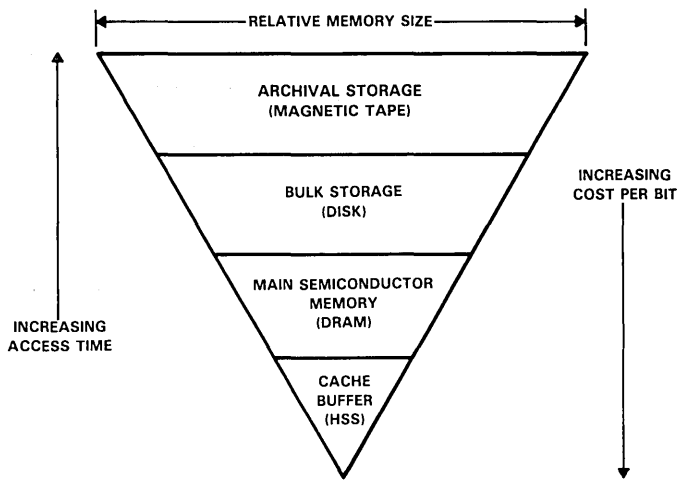


Figure 3-1. Memory Size vs Access Time and Cost Per Bit

3.2 Memory Systems with Cache

When the processor accesses main memory, the processor address is compared to the addresses currently present in the cache tag RAM. When a match occurs, the required data is resident in the cache and the access is called a "hit" and is completed in the cycle time of the fast memory. When a match does not occur (a "miss"), the main memory is accessed and the processor must be delayed to allow for the slower access cycle of the main memory. Whether a hit has occurred is determined by the cache-tag RAM. Figure 3-2 shows the relative placement of the processor, main memory, cache, and cache-tag RAM within a system.

Since there must be comparisons made between the current processor address and the addresses in the cache, the cache-tag RAM must have a very fast access time to prevent the degradation of processor accesses even when a match occurs. Previously, the memory used for the cache-tag RAM was the same as that used for the cache, which (because of added delays through comparison logic) meant that the full benefits of the cache were not realized.

The Cache Address Comparators were designed to reduce this cache access degradation to a minimum by incorporating the matching logic on-chip. This provides match-recognition times that are compatible to the access time of the cache-buffer memory.

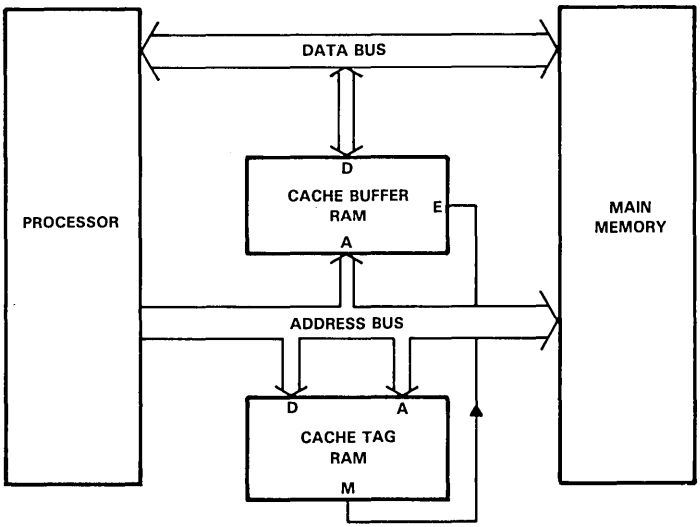
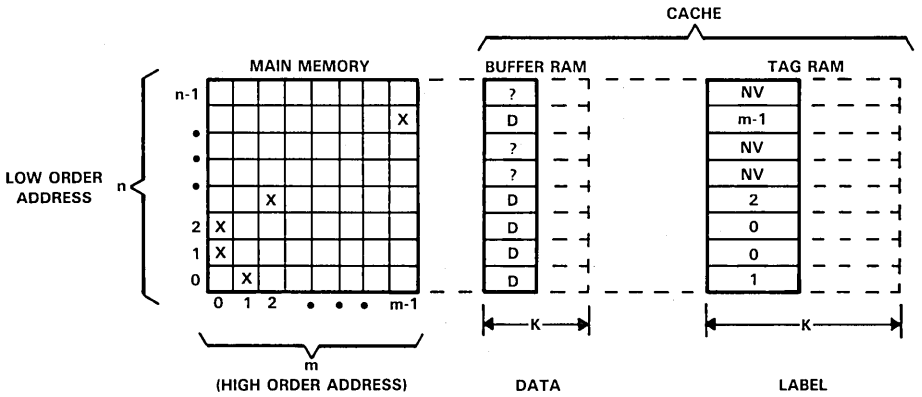


Figure 3-2. Typical Memory System with Cache

3.3 Cache Memory Systems Using 'ACT2151 and 'ACT2152

3.3.1 Set-Associative Cache Address Matching

The 'ACT2151 and 'ACT2152 implement the set-associative type of cache address matching. This algorithm may be more clearly understood by considering main memory as an (m) by (n) array of blocks and the cache is an (n) by (k) array (see Figure 3-3). Each block is composed of (x) words, and transfers between main memory and cache memory always move all (x) words in that block. Corresponding to every block in the buffer RAM is a tag address specifying which block of main memory is currently resident in the buffer RAM at that location. The set-associative algorithm maps each modulo (n) group of (m) blocks into the corresponding (n) row of the cache. The low order address lines of the processor covering the sets (n) select a row of the cache buffer and the corresponding row in the tag RAM. The data is stored in the cache buffer and the high-order address specifying the block (m) is saved in the tag RAM. The high-order address then becomes the tag.



K = Number of BUFFER/TAG groups for multiple cache systems
X = Blocks moved to cache
D = Valid data from main memory
? = Areas of cache that have not been loaded from main memory
NV = Code to indicate non-valid label
0, 1, 2, m-1 = Labels from high order address specifying the block moved from main memory.

Figure 3-3. Set-Associative Cache Address Matching

3.3.2 Cycle Time Improvement

There are several algorithms used to determine which areas of main memory should be resident in cache and which should be replaced (first-in, first-out; least recently used; or random). Since programs typically have the property of locality (over short periods of time most accesses are to a small group of memory addresses), these replacement algorithms can make the cache have the majority of processor accesses resulting in hits. The hit ratio (number of hits × 100%/number of memory accesses) runs 90% and higher in systems with well coordinated memory to cache mapping routines. As the block size (x) increases, the replacement mapping algorithm options have greater impact on the cache performance.

When running at maximum frequency, many microprocessors are operating with memory access times of 100 ns or less. After allowing for address buffering, decoding, and propagation delays through data buffers, the maximum access time that can be tolerated is 60 ns or less before processor throughput is affected. For large memory systems, DRAM can be used to achieve a cost effective memory.

However, these cannot meet a 60-ns access requirement. If the actual system throughput for a system with cache and one without cache are compared, the advantages of cache become obvious.

For comparison of the two architectures, assume that a processor is implemented in which 30% of the active cycle involve main memory (the other 70% used for instruction decoding and internal operations). Also assume that the processor cycles at 125 ns with a required memory access time of 60 ns. If the memory is not ready, the cycle time is extended by 125-ns increments till satisfied. This processor using 120-ns DRAMs would require one delay increment on main memory accesses and 200-ns DRAMs would require two delay increments. The average cycle time can be calculated for each memory speed as follows:

Average Cycle Time = [(INT) × (CYC)] + [(MEM) × (CYC + DEL)]

where INT = percent of time doing internal operations
CYC = processor cycle time
MEM = percent of time doing memory accesses
DEL = number of delay increments × 100 ns

For a processor using 120-ns DRAMs:

Average Cycle Time = [(70%) × (125 ns)] + [(30%) × (125 + 125)]
Average Cycle Time = 163 ns

For a processor using 200-ns DRAMs:

Average Cycle Time = [(70%) × (125 ns)] + [(30%) × (125 + 250)]
Average Cycle Time = 200 ns

For the same system with cache memory assume a 90% hit ratio with 60-ns cache and 120-ns DRAM:

Average Cycle Time = [INT × CYC] + [MEM × [(HIT × CAC) + (MIS × (CYC + DEL))]]

where INT = percent of time doing internal operations
CYC = processor cycle time
MEM = percent of time doing memory accesses
DEL = number of delay increments × 100 ns
HIT = percent of memory accesses hit cache
MIS = percent of memory accesses miss cache
CAC = cache memory access cycle time

Average Cycle Time = [70% × 125] + [30% × [(90% × 125) + (10% × 125 + 125))]]
Average Cycle Time = 129 ns

This value represents a 20% improvement with 120-ns devices over the non-cache implementation with 120-ns devices and 35% using 200-ns devices. This performance improvement can be further demonstrated for those systems using custom or bit-slice processors where the memory cycle time as well as access time is of concern. For this example, consider a processor with a cycle time of 50 ns and main memory cycle time of 100 ns (use the same access ratios as in the previous example):

Average Cycle Time = [(70%) × (50)] + [(30%) × (100)] = 65 ns
(Without Cache)

Average Cycle Time = [70% × 50] + [30% × [(90% × 50) + (10% × 100)]
(With Cache) = 52 ns

This represents a 20% decrease in average cycle time for the processor using 50-ns cache memory. If the main memory was rated at a cycle time of 200 ns, either using slow main memory or due to allocation of alternate cycles for some other activity (multiprocessors, direct memory access, display refresh, etc.), the cache would still give an average cycle time of 55 ns. This is an improvement of 63% over the 95 ns average cycle time for a non-cache system.

3.3.3 Cache Memory Configurations

Figures 3-4, 3-5, and 3-6 illustrate applications for the 'ACT2151 and the 'ACT2152 in cache memory systems. Figure 3-4 shows a cache-memory configuration that has a 512M-byte main memory with a block size of 4 32-bit words. In this particular application, a cache containing 1024 four-word blocks was chosen thus defining the main (n) × (m) array as being 1024 sets of 32,728 four word blocks. The 128M-word memory requires an address bus of 27 lines. The least significant bits (A2-A3) are used as a word select for one of the four words in each block. The next least significant address lines (A4-A13) are used as the set select inputs to the cache buffer RAM and the cache tag RAM. The remaining high order address lines (A14-A28) form the label or tag which is stored and compared by the tag RAM.

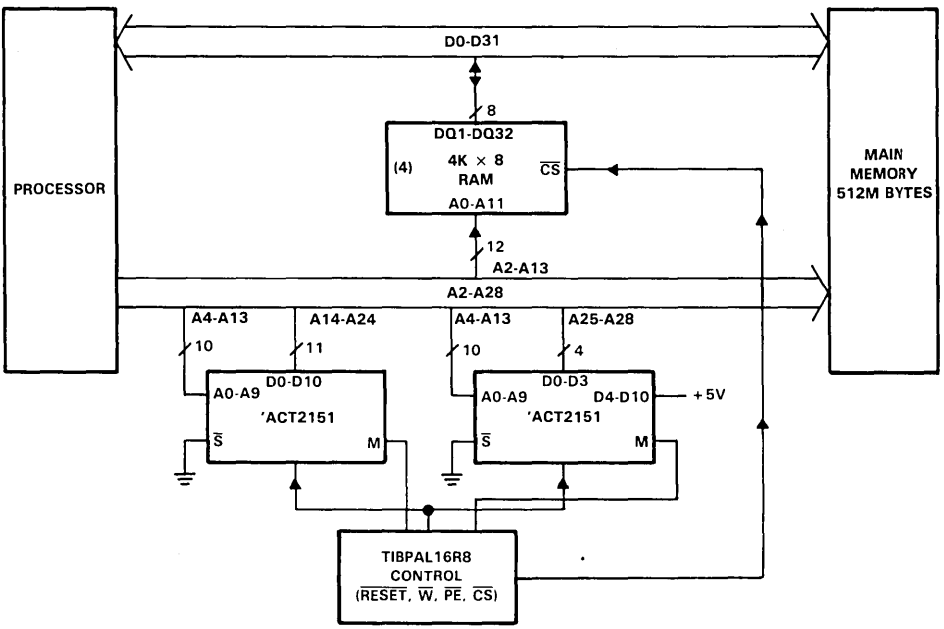


Figure 3-4. Cache Memory Configuration (Block Size = 4)

Since the label in this example is composed of 15 address lines, two 'ACT2151 devices are used to expand the tag. The 15 address lines are the data inputs to the tag RAM. The other data inputs are tied to 5 V so that, after Reset, invalid data cannot force a match. The match output of the two 'ACT2151 devices are combined to form the enable for the cache data buffer. If the contents of either 'ACT2151 do not contain a match, the cache is not enabled. These signals are also used by the control circuits to inform the system that the address is not present in the cache so that main memory might be accessed. The control circuit also resets the cache upon power-up. This is accomplished by taking the $\overline{\text{RESET}}$ input of the 'ACT2151 low. After reset, no matches will occur at any locations until that location has been written.

In the application shown in Figure 3-5, the expansion of the cache RAM is carried out in both depth (more sets) and width (wider tag). The block size was chosen as one such that the 4K cache now represents 4096 blocks of one word each. The high-order addresses are still used as the label to the tag RAM. A13 is used to select between two 'ACT2152 pairs. Each pair contains labels for 2048 of the cache-memory blocks. Address lines A2 thru A12 are used as the set-address inputs. If the chip select ($\overline{\text{CS}}$) is at a logic high (deselected), the 'ACT2152 match output (M) is high. An AND function can be used to enable the cache data buffers and also notify the control circuit if access needs to be made into the main memory. The logic for this system illustrates that the upper pair are compared for the first 2048 blocks within cache and the lower pair are compared for the second depending on the state of address A13.

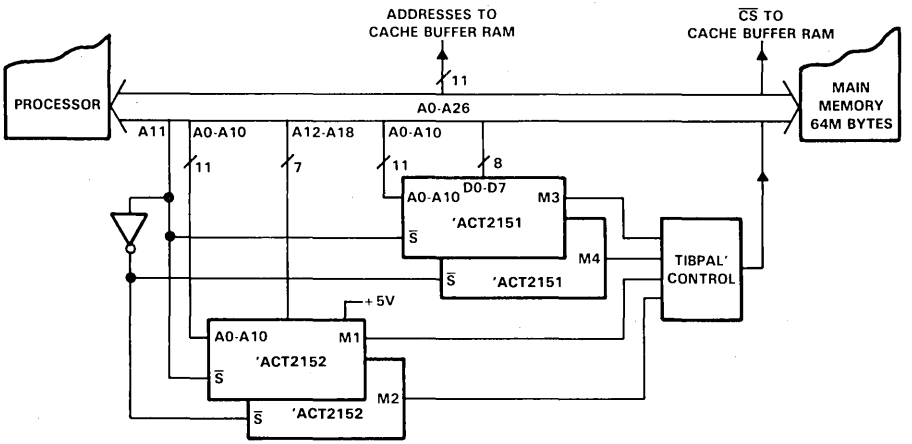


Figure 3-5. Cache Memory Configuration (Block Size = 1)

A dual cache structure (K = 2) is shown in Figure 3-6. The M-word memory is divided into 4096 sets of 256 four-word blocks. In this example, A0 and A1 are used to select which one of the four words within a block are accessed. A2-A12 select which of the 2048 block labels are to be compared. Addresses A14-A21 form the eight-bit label for the block. Address A13 is used by the cache control logic in conjunction with the possible processor status lines as chip select inputs. The match outputs from the two 'ACT2152 devices, A1 and A2, are NANDed to form an active-low enable to the cache data buffers and to serve as a request to the control logic. The match outputs from B1 and B2 also are NANDed to perform a similar function for cache RAM B. If no match is found in cache RAM A or B, the control logic will initiate an access from main memory. The purpose of the dual-cache architecture is to allow for rapid switching between multiple tasks or programs since the processor can have access to one cache while the controller moves data between main memory and the other cache. The dual or multiple cache approach also yields more replacement options than the single cache architecture. When an access results in a miss in the single cache system, the data in cache is replaced by the current data even though the old data may still be useful. By using independent caches, the control can determine which data is most expendable and replace that block while the other caches keep their potentially useful data.

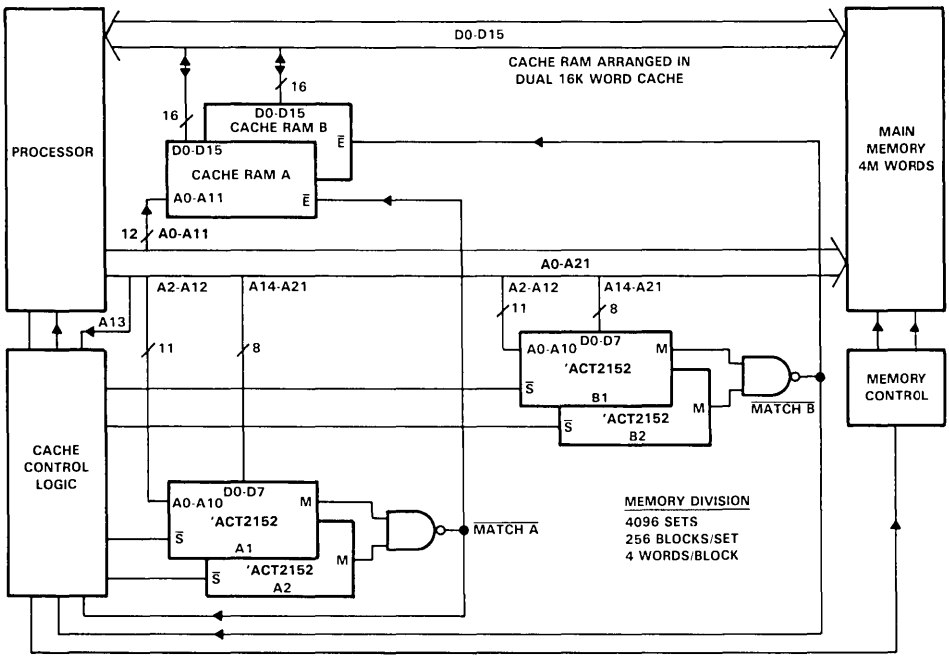


Figure 3-6. Cache Memory Configuration, Dual Cache (K = 2)

3.3.4 Summary

Cache-memory architecture can enhance the throughput of many microprocessor systems. This allows large low-cost memory to perform like a high-speed RAM. The 'ACT2151 and 'ACT2152 reduce the tag memory implementation cost and complexity and provides label comparison times comparable to the access times of high-speed memories. These additional benefits make high-performance microprocessor designs that can use the same techniques of optimizing cost, memory size, and throughput that had previously been available only in larger computer applications.

3.4 Article Reprints

The following three articles are being reprinted in this report for your convenience. The articles are "Caches Keep Main Memories From Slowing Down Fast CPUs", "Cache-Memory Functions Surface on VLSI Chip", and "Match Cache Architecture to Computer System".

Until main-memory speeds catch up to CPU processing speeds, cache memories can be called upon to keep overall throughput rates up—especially as main-memory sizes grow.

Caches keep main memories from slowing down fast CPUs

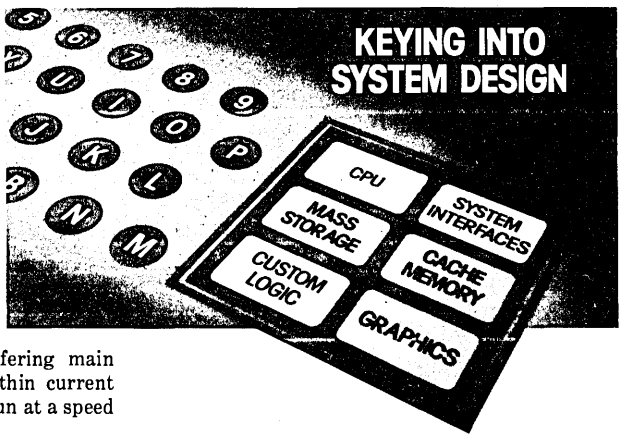
This article begins a series on cache-memory systems long employed in mainframes and high-end minicomputers, and just now ready to enter microcomputers as large, but slow dynamic RAMs become available. The strategy of Texas Instruments is sketched by Richard N. Gossen, manager of advanced development, in this issue (p. 32).

Whenever a speed mismatch occurs between main-memory bulk storage and a fast-processing CPU, a cache memory can provide the interface to take full advantage of the CPU's processing speed. From the main memory, the cache memory extracts and temporarily stores enough data to satisfy immediate CPU needs. Writing from the main memory is at the main-memory's slow speed, but reading to the CPU is at the CPU's high speed. As the word "cache" implies, the memory's operation is hidden from (or rather, transparent to) the user.

Figure 1a exemplifies an 8-Mbyte main-and-cache-memory system in a typical large computer (see "Caches Needed as Main Memories Grow"). The main memory alone can attain a cycle time of about 400 ns, but with error-detection-and-correction circuitry added to the system, a cycle time of about 500 ns is more likely. On the other hand, an ECL- or TTL-based CPU can be ten times faster with about a 50-ns cycle time. Buffering main memory with a 50-ns cache—well within current technology—enables the computer to run at a speed close to the CPU's maximum speed.

Figure 1b shows a more detailed block diagram of a typical cache memory. It represents a set-associative cache system with 2-kbytes of data storage capacity in a single-set configuration and it serves a 16-bit microprocessor system with a 22-bit address bus. The basic storage elements are two RAM arrays: one, a 1024 × 16-bit-word unit for data storage; and the other, a 1024 × 13-bit-word unit for address, or tag, storage. Addresses that arrive via the CPU data bus (A_0 to A_{21}) are compared with those held in the tag RAM. If they match, the desired data are located in the cache's data RAM and the main memory can be bypassed.

When first turned on, or should the computer system malfunction or be shut down momentarily, the cache would then probably contain improper or erroneous data. Thus, a most important function not



Cliff Rhodes, Static-RAM Design Manager
Texas Instruments Inc.
4000 Greenbriar Dr., Stafford, TX 77477

specifically shown in the block diagram is a special control-logic section to perform initialization operations for loading the cache with valid initial data. Particularly important is the proper loading of the tag RAM to prevent false matches.

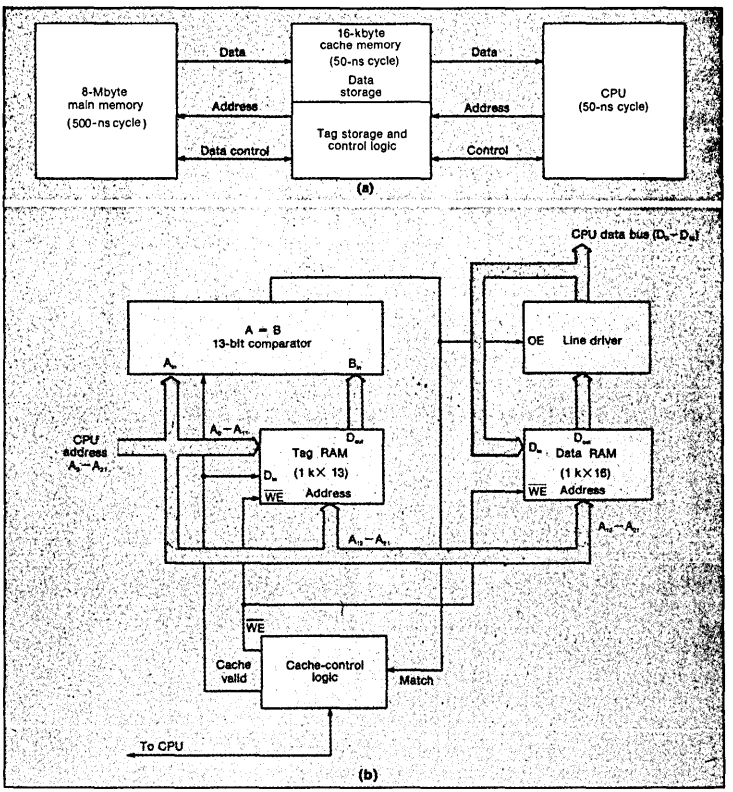
Traditionally, cache memories have been constructed with static-RAM bipolar-semiconductor technology, but recent improvements have given NMOS static RAMs an edge by requiring less power at the same speeds as bipolars. The CPUs, of course, are built from high-speed ECL or Schottky TTL, whereas main memories usually are composed of dynamic RAMs that are about an order of magnitude slower than the CPU.

Cache concept based on probability

No matter what the cache is made of or how it is configured, its operation is based on "property-of-locality" probability principles, which experience has shown to have the following characteristics: First, over short time periods, most CPU memory accesses are made to adjacent, small groups of locations; therefore, even a small cache, storing carefully selected data, will have data the CPU needs most of the time. Second, data stored in the cache and recently used will likely be reused shortly thereafter. Finally, data adjacent to data that have been recently used will most likely be used next.

Usually, then, several adjacent words are transferred from main memory into the cache: The immediate need may be for just one of the words, but eventually the subsequent words are likely to be required. This procedure reduces repeated accesses to main memory ("misses"), and increases the probability of finding the data in the cache, or "hits."

To demonstrate the effectiveness of a cache, consider a typical system, where 20% of all CPU operations are memory accesses (misses), the CPU cycle-



1. In a computer system with a main memory, whose cycle time is a relatively slow 500 ns, a fast 50-ns cache memory is interposed to match the CPU's 50-ns cycle time (a). In more detail, a set-associative cache system has address tag words stored in one RAM, while the data words are stored in a separate RAM (b).

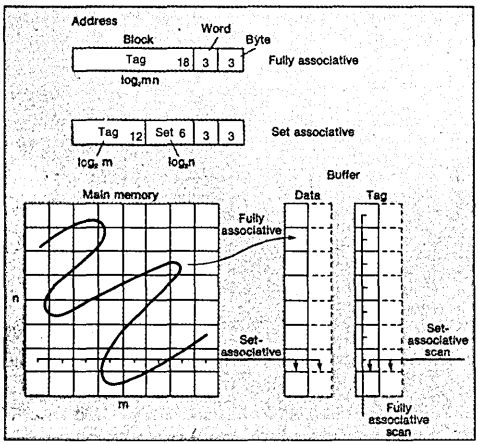
time is 50 ns, and main-memory cycle-time is 500 ns. Accordingly, average machine-cycle time is

$$\frac{20 \times 500 + 80 \times 50}{100} = 140 \text{ ns.}$$

However, with a 90%-efficient, 50-ns cache, the average cycle time is

$$\frac{2 \times 500 + 18 \times 50 + 80 \times 50}{100} = 59 \text{ ns.}$$

Note that with an effective 90% hit ratio, the CPU is forced to access the main memory on just 2% of all machine cycles (10% of 20% of the cycles). Thus, most memory accesses are handled through the cache, and the average machine cycle-time is cut to almost a third. However, these calculations are simplified, because only a monoprogram instruction stream is considered. Indeed, properly designed cache memories routinely achieve considerably better performance in mainframes and minicomputers with actual, more complex programs.



2. A fully associative mapping algorithm allows any one of the m × n main-memory blocks to be placed into any one of the cache-memory blocks.

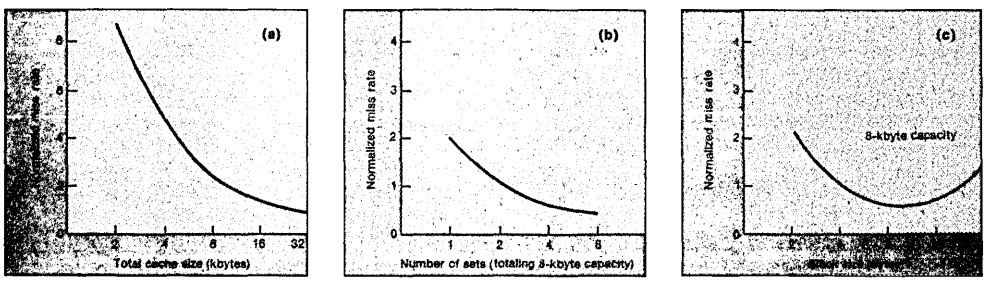
A cache memory's data-storage section can be implemented fairly simply with standard, high-speed static RAMs. However, the address, or tag-storage, section must do more than just store—it must also compare addresses on the CPU bus with those it stores. This is best done with an associative-addressing technique.

Data access by association

Data in an associative or content-addressable memory are not accessed merely by a location, or address, code as in conventional memories, but are found according to some property or "value" of the data. Instead of an address word, a so-called search key, or descriptor, is presented to the cache, which represents particular values of all or some of the bits of a stored word. When it is compared together with a "lock"—the so-called tag bits—with all the words stored in the cache, the search key ferrets out all associated words. If the key has few attributes—is therefore said to be "loose"—many words can match and be accessed.

Though simple in concept, the associative-search procedure is very complex in execution. The two most common mapping algorithms that associate a set of data in main memory—called a "block"—with a corresponding block in the cache are designated "fully associative mapping" and "minimal set-associative mapping."

In fully associative mapping (Fig. 2), any one of the m × n blocks in main memory can be placed in any one of the cache blocks, which then has a tag address associated with it that specifies from which main-memory block it came. (One of the tag bits—a control bit—checks the validity of the block, and



3. The larger the cache, the smaller the number of misses (a). Splitting the cache into several independent sets further reduces the miss ratio (b); however, in both these cases the improvement rate tapers off sharply beyond some specific point. And when block-size and block-quantity are traded off against each other (c), miss rates are minimized sharply at some particular optimum size/number relationship.

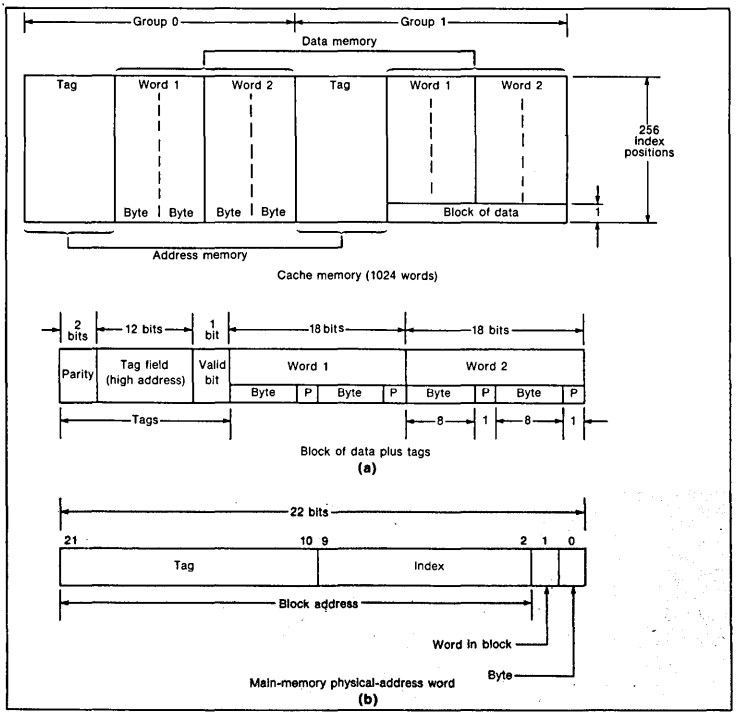
the low-order address bits can define bytes and data-transfer units, or words.) Each address generated by the CPU must be compared with all of the tags, and the field of address tags must span all main-memory m × n blocks, regardless of the cache's capacity. In this case, the cache acts as a linear array.

In set-associative mapping, a selection from an n row of m blocks is placed into the corresponding row of the cache. Then only those bits covering dimension m become the tag of the set n. Thus, for each CPU address only the tags in that row must be compared. However, for the minimum effective set—having a dimension of two—a linear array must swap blocks frequently because the cache cannot hold more than one block from a row at any time.

Whether fully associative or set-associative mapping, if data-block addresses in the cache tag-store match those on the CPU address-bus, the data are made available from the cache. And if no match, or a miss, occurs, the CPU is delayed while the needed data are fetched from main memory. In this process, the entire block containing the data sought is transferred into the cache.

Of course, the larger the cache, the smaller the number of misses on each CPU cycle. However, for a normalized miss-rate-vs-cache-size plot that assumes a fixed number of blocks in the cache and a main-memory size from 2 to 4 Mbytes, the rate of improvement in miss rate diminishes rapidly above 8 kbytes of cache size (Fig. 3a). Thus, the cost of a very large cache is not paid back in higher performance, when optimum size is exceeded.

However, further improvement can be obtained by breaking the cache capacity into a number of sets —defined as the number of parallel, independent caches in a system. For the same 2-to-4-Mbyte main memory and with the total cache size fixed at 8 kbytes, two separate caches of 4 kbytes each offer better performance than a single 8-kbyte implementation, because another quick data-replacement trial is available whenever a miss occurs the first time (Fig. 3b). With a single set, a miss forces accessing the slow main memory, which replaces all the data in the cache, even though the replaced data may soon be required again in the program. However, again performance increase slows significantly above an



4. The cache for the PDP 11/70 is organized into two 256 blocks of data totaling 1024 words (a). Every block has a tag field representative of the physical address of the word in the main memory (b).

optimum size—in this case, above between two and three independent sets for the 8-kbyte cache capacity.

Naturally, block size and the number of blocks also affect miss rate. However, in a constant-capacity cache, trading the number of blocks against their size seems to raise a conflict: Large blocks accommodate more adjacent data and thus would tend to reduce the miss rate. But a higher number of smaller blocks also would help reduce misses by providing more data choices. Figure 3c shows a minimum miss rate at about 8 bytes per block, or 1000 blocks, for a total 8-kbyte cache capacity. For block sizes between 2 and 16 bytes, an 8-, 16-, or 32-kbyte cache offers the same normalized miss-rate performance, although larger the total capacity, the smaller the absolute miss-rate.

To complete this general overall description of cache operation, one additional important function must be examined—the data-replacement algorithm. Again, any time a cache memory records a miss, a new block containing the required data must

Caches needed as main memories grow

Although advanced microprocessor-based systems are beginning to see the dawn of the cache-memory era, large systems like the IBM 360 class and large minicomputers like the DEC PDP-11 series have been "caching-in" for years. On a cost-effective basis, a cache system offers higher system speed for the cost of just a small quantity of fast memory plus its associated logic.

The resulting speed depends on the size and organization of the cache, not the size of main memory, and no programming changes follow when a cache system is used. Nevertheless, it is the increased main-memory size that will fuel the growth of cache-type systems in the upcoming high-performance microcomputers and microprocessor systems.

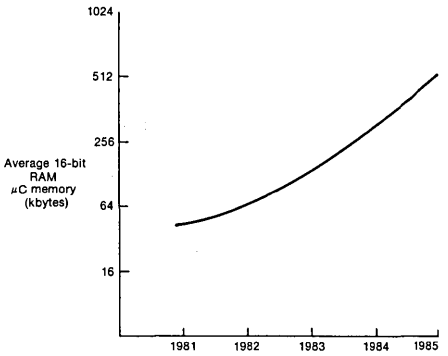
The high-density RAM chips that will significantly increase the main-memory sizes that microprocessors and microcomputers will be called upon to support are relatively slow dynamic units (see table). By 1983, as the 64-kbit dynamic RAM becomes a cost-effective chip, the average 16-bit processor will be operating with 128 kbytes of memory. And by 1985, with the expected maturity of the 256-kbit dynamic RAM, ½-Mbyte memories will be commonplace in 16-bit processor systems (see curve). Already, TI's 16-bit 99000 processors can address up to 16 Mbytes with the addition of a memory-management unit. Systems of this size, like mainframes and large minicomputers, will demand cache memories to enhance performance.

While physical memory size encourages the growth of cache systems, improved microprocessor performance also contributes to wider cache use. Processor speeds will certainly increase, necessitating fast cache memories to enable CPUs to make full use of their improved capabilities. The accompanying table projects the expected speed performance in 1982 of several of the best known processors.

For example, TI's 99000, with a maximum clock-rate of 6 MHz, is expected to support memory access times of 90 ns. This meshes perfectly with the new generations of NMOS static RAMs, whose access times are now in the 30-to-50 ns range. A 99000 will almost certainly benefit from a cache-memory system when it supports main memories in the megabyte range. Indeed, the Zilog Z8001A, the Motorola M68000, and the Intel 8086-2 are somewhat slower than the 99000 in memory-access times; therefore, they should most definitely benefit from a cache for high-performance applications.

1982 projected 16-bit μC performance

Processor	Maximum clock rate	Fastest supportable memory access
99000	6 MHz	90 ns
8001A	6 MHz	215 ns
68000	8 MHz	225 ns
8086-?	8 MHz	280 ns



In such microprocessor systems, dynamic RAM used as the main memory will always remain the limiting factor to improved system performance because it is slower than a microprocessor. Even a dynamic RAM with access time as fast as 150 ns slows considerably when operated in a 1-Mbyte memory system using error-detection-and-correction circuitry. The best performance of such a RAM is in the range of 400 to 500 ns, minimum. If a processor is forced to interface at this slow speed, severe performance penalties result in the system.

be fetched from main memory to replace the block already in the cache. But which block should be removed to make way for the new information?

Clearly, replacement should be based on some type of index of value for maximum effectiveness, not randomly performed. An index of value can be based on the chronology of the data, such as FIFO (first-in, first-out), or the frequency of use, LRU (least recently used), or a combination of the two. Of these, LRU is one of the most popular techniques. It is based on the theory that if information has been often and recently referenced, it is likely to be referenced again in the near future.

LRU offers some advantage over the FIFO algorithm. Even though FIFO eliminates the possibility of loading data and immediately removing it, FIFO has a serious disadvantage: Even when a block of data is frequently and continually used, eventually it becomes the oldest and is removed, although experience shows it likely will be needed again, soon. In addition, FIFO can introduce some unusual side effects.

The associative cache in the PDP-11

In an actual cache system, say the PDP-11/70, a 1024-word (2048-byte) memory is organized as an associative cache in two groups, or sets—each group containing 256 blocks of data and each block containing two words divided into two bytes (Fig. 4a). Every block also has a tag field to represent the physical address in main memory, where the original copy of the data-block resides.

Data from main memory can be stored in the cache in an index position determined by its main-memory physical address (Fig. 4b). An 8-bit index field (bits 2 to 9) of the main memory's 22-bit physical-address word determines which of the 256 cache-memory-array blocks will contain the data (either in group 0 or group 1 as determined by the hit or miss conditions). And the lowest two bits (bits 1 and 2) select word-1 or word-2 and byte locations in the block. But only the high-address field (bits 10 to 21) —the tag field—is stored in the cache.

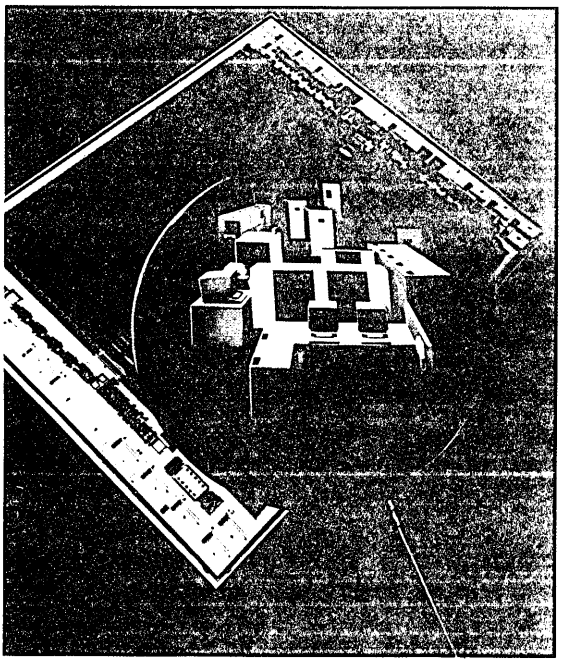
Data are always sought in the cache first. If the information is not present—a miss—a two-word block of data is transferred (written) from main to cache memory. In a typical program, writes to the cache occur just 10% and reads from the cache, 90% of the time. Read hits average 80 to 95% of all memory operations in a typical program.□

Design

A cache-tag store and comparator on a single chip will reduce parts count, save space, and also greatly simplify cache systems in upcoming minicomputers and microcomputers having large memories.

Cache-memory functions surface on VLSI chip

This is the second article in a series on cache-memory systems. The first article, which covers the basic philosophy of cache systems, appeared in the Jan. 21 issue (p. 179). The overall approach was sketched by Richard N. Gossen, manager of advanced memory development at Texas Instruments, in the same issue (p. 32).



Given the growth now occurring, and in the offing, in the main-memory size of minicomputer and microcomputer systems, cache memories will be needed to take full advantage of their CPUs' speed. The TMS2150 cache-address and comparator IC represents a major step in simplifying the cache designer's task, as it handles most of the so-called tag functions—cache-address storage and comparison.

A cache memory is a small, fast buffer memory interposed between a fast CPU and a relatively slow main memory, like a dynamic RAM. In this way, with anticipated and frequently used information prestored in the cache, the CPU can obtain most of the data and addresses it needs at a speed comparable to its own. By proper design, the number of information accesses to the large but slow main memory can be reduced to a minimum. With a special memory-mapping technique, a small number of cache storage locations can represent large blocks of backing-memory information.

The cache, a fast static RAM, is divided into two sections—the tag store for the cache addresses; and the data store for numerical, program, or other types of data. Cache memories, however, require more than mere storage. Just as important is high-speed data comparison to check a portion of the CPU address field against the tag addresses previously stored in the static RAM. This operation determines whether the data addressed by the CPU resides in the cache.

The 2150 (Fig. 1) stores the cache tags (or addresses) in a 512-word × 9-bit static RAM, and also contains a 9-bit comparator. In addition, it generates and checks parity. The RAM's high speed, of course, matches or exceeds that of most available

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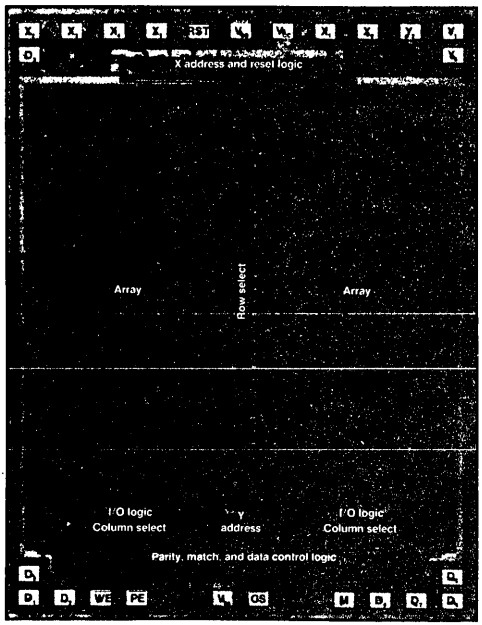
microprocessors, and the 9-bit comparator circuit, which is integrated into the chip's memory-sensing amplifiers, is about 50% faster than bipolar comparators currently found in cache systems.

Housed in a 24-pin, 300-mil ceramic DIP, the 2150 works over an ambient temperature range of 0° to 70°C. Operation is from a single +5-V power supply, and the chip interfaces directly with both TTL and MOS logic circuits. Because of the ceramic package, power dissipation can go as high as 660 mW; typical dissipation, however, is 400 mW. To simplify cache-system design, the 2150 works fully statically—no clock or synchronizing signals needed—and it is easily expandable to fit any size processor bus or memory system (see "VLSI Built with Proven Techniques").



1. The TMS2150 cache-tag store and comparator, a single VLSI chip housed in a ceramic 24-pin DIP, occupies 24,600-mil² of silicon and is fabricated with proven 4.5-μm design rules and NMOS technology.

The use of the 2150 makes for a minimum chip-count cache system, especially in conjunction with the companion TMS2149 1-k-×-4-bit static RAMs to store the data. The 2150 alone replaces 14 chips in conventional systems. Still, even the simplest cache-control circuit with the 2150 requires several TTL devices for buffering and control and some fast RAMs (like the 2149s) for storage.

In the block diagram of the 2150 (Fig. 2), the tag static-memory array of 64 rows by 72 columns is organized into the 512 words of 9 bits each, for a total of 4608 bits.

Initializing this memory is simple: Merely pulsing the $\overline{\text{Reset}}$ terminal low to clear all 512 memory locations forces the chip's Match output terminal high; and the reset pulse can be as short as 35 ns. Initializing a conventional cache memory, however, is much more complex. It requires a set of sequential operations that is time-consuming and demands far more hardware than the 2150's asynchronous single pulse.

A read cycle is enabled when the chip-select ($\overline{\text{CS}}$) input is driven low while the write-control input ($\overline{\text{W}}$) is held high (Fig. 3a). During this cycle, nine input-address bits (A_0-A_8) select a 9-bit word in the memory array for comparison with eight input-data bits (D_0-D_7) and an internally generated parity bit. Upon a valid match, the Match output terminal goes high. However, if the parity check indicates an error in the internal-memory data, the parity-error output ($\overline{\text{PE}}$) and the Match output go low. The $\overline{\text{PE}}$ output is an open-collector type, allowing simple $\overline{\text{OR}}$-tie connections to other devices.

For a write cycle, both $\overline{\text{CS}}$ and $\overline{\text{W}}$ must be driven low. Then, the data on the D_0-D_7 terminals, plus an even parity bit from the internal parity generator are written into the memory-array location addressed (or rather tagged) by A_0-A_8. A parity error can be forced by holding the $\overline{\text{PE}}$ terminal low, which is very useful for testing.

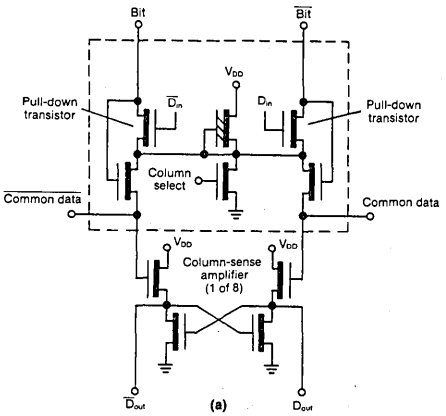
The 512-×-9-bit tag memory-array structure permits the system to be expanded in building-block fashion for either wider or deeper tag stores. Patterned after bit-slice techniques, the 2150 can be considered an 8-bit-slice cache-address and comparator; accordingly, a 16-bit word could be divided into two 8-bit segments and operated on in parallel by two cache systems, speeding up performance in comparison with serial operation.

A key speed specification of a cache-address comparator is the delay time, $t_d(A)$, needed for the signal to go from the address input to the match outputs. Generally, this specification is a worst-case delay path in a cache-memory system. The 2150 is available with four delay versions—maximums of 45, 55, 70, and 90 ns—to meet a variety of cache-memory

VLSI built with proven techniques

Occupying just 24,600 mil² of silicon, the TMS2150 cache-address store and comparator is fabricated with conservative, 4.5-μm design rules and 2.5-μm NMOS polysilicon gate lengths. Many of the 2150's circuit techniques were first proven on the TMS2147H and TMS2149 4-k low-power, fast static RAMs. One such circuit, a distributed column-sensing amplifier (Fig. a), significantly improves the speed-power product over that of previous high-speed MOS designs.

During read cycles, tag data stored in the 2150's on-board memory are not directly accessible; instead, they are compared with the input data and checked for parity. Since this parity check must be performed at high speed, the sense amplifiers must reach valid



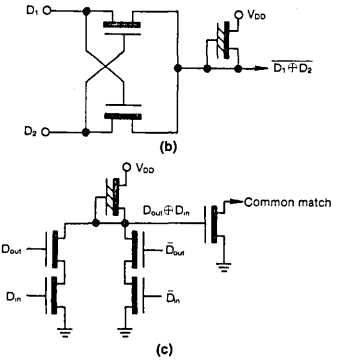
logic levels very quickly. That is beyond conventional differential amplifiers, but does not faze the distributed, column-sensing amplifier in the 2150. One method employed in the sense amplifier to help achieve the required speed is to isolate the bit lines (BIT and $\overline{BIT}$) fully from the data lines (D_{out} and $\overline{D}_{out}$) thus reducing the amplifier loading, which would hold speed down.

A cross-coupled pair of FETs driven by data-line source-followers acts as the main sense amplifier. This circuit provides fast level shifting, high gain, and excellent performance over the total expected range of semiconductor processing variations and operating temperatures.

Reading occurs when a column is selected by a high-level signal to the circuit's column-select input. This input activates the column amplifier, which differentially drives the pair of common-data lines to the sensed state, which is then quickly transformed into sharp, clean logic levels by the sense amplifier.

To write data into the on-board memory, the pair of data-in signal lines (D_{in} and $\overline{D}_{in}$) must activate the gates of the bit-line pull-down transistors. With the desired column selected, forcing a data-in line to the V_{DD} voltage level pulls the associated bit line low to write the data in. At the same time, the complementary Data In line is held low, which permits the complementary bit line to rise to V_{DD} via the bit-line bias circuitry (not shown).

Because the bit lines are fully isolated from data-line loading, they can be driven efficiently by the



chip's small memory-cell transistors. Also, the sense-amplifier circuit has a precisely controlled differential-voltage gain. Moreover, the dynamic requirements for the column-decoding circuitry (also not shown) are light, because only one small transistor activates the column selection. And since the transistor's source terminal is at ground potential, a relatively low column-selection voltage is sufficient to activate the column.

In addition, the Exclusive-NOR gates were specially designed to minimize chip real estate. To simplify the layout, the parity circuit's Exclusive-NOR gate (Fig. b) requires just a single-polarity input signal, minimizing the needed interconnection area. Similarly, the comparator's Exclusive-NOR circuit (Fig. c) uses a common match line for the 9-bit comparator circuit to hold down the interconnection area.

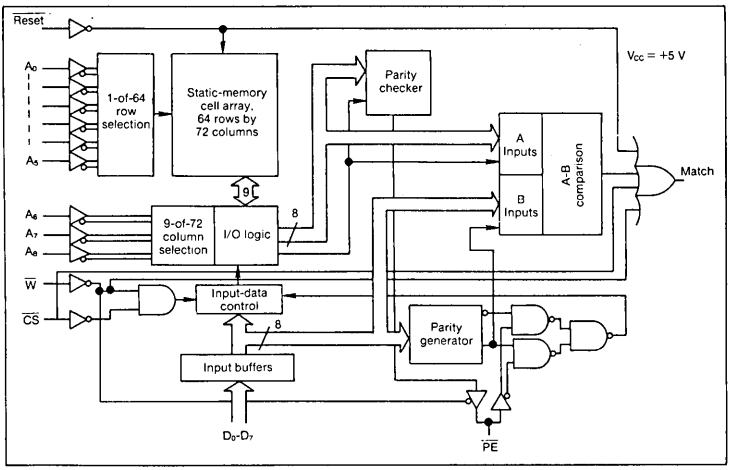
system speeds (Fig. 3a shows a unit whose t_d (A) is about 30 ns).

The fastest specified version (45 ns) is about 20% faster than the fastest conventional bipolar RAM and external TTL comparator circuit. In addition to being fast, the address-to-match signal time of the 2150 is relatively stable over the operating temperature range, increasing just 20% from its 25°C value with the Match output driving a 30-pF load (Fig. 4). In addition, t_d (A) changes little with supply-voltage variations.

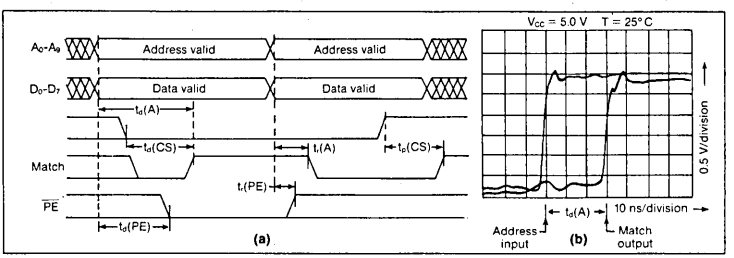
Other important timing parameters include the chip-select-to-match delay time, t_d (CS), which is about 25 ns maximum in the fastest 2150 version, and the input-address-to-PE delay time, t_d (PE), which is specified at a maximum of 55 ns for the same version.

Applying the 2150

With the tag-store and comparator circuitry on a single chip, the 2150, of course, is a large saver of circuit-board space. One or more 2150s together with several 2149 static RAMs can be placed on a single board, rather than the 1½ to 2 boards usually



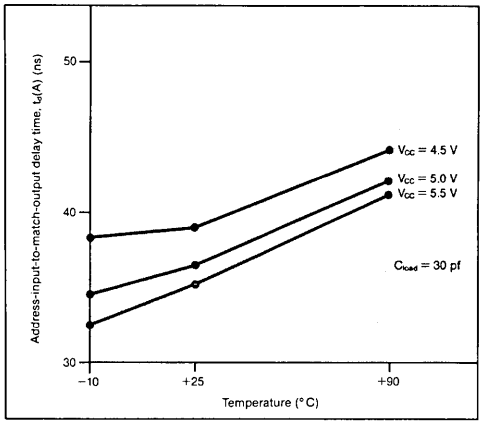
2. The 2150 contains a 64-row-×-72-column static-RAM memory array organized as 512 words of 9 bits each. The RAM stores tag-address data for the cache system, and the rest of the chip provides the logic for comparing the stored tag address with the address on the data-bus line for validity, and providing or checking the data's parity.



3. The timing cycles for 2150 start with a $\overline{CS}$-low signal. After comparison and matching, either a Match high or a parity error ($\overline{PE}$) low is obtained (a). The worst-case time delay between the address input and match output, t_d(A), is a key 2150 specification, and is available as one of four maximum values. A unit actually measured has a typical 30-ns t_d(A) delay (b).

required. Moreover, a single-board cache memory virtually eliminates the delay times from the capacitances introduced by buffers, conductor traces, board connectors, and backplane wiring.

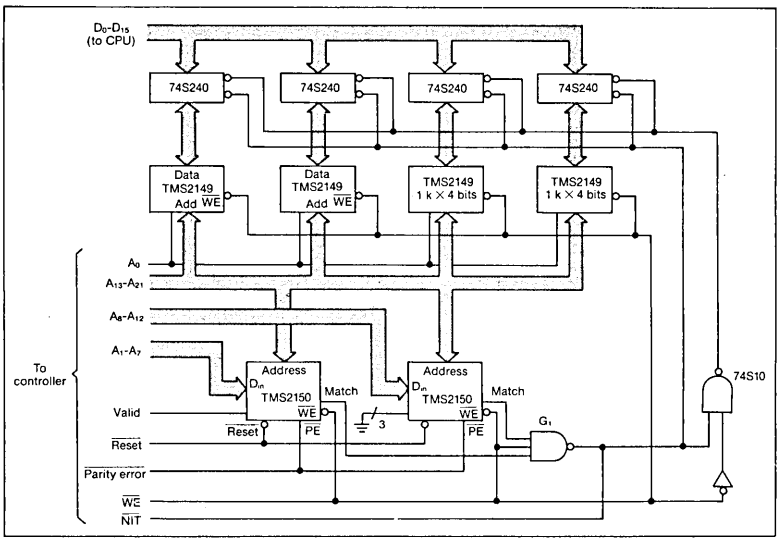
For example, the board can contain a single-set, 2-kbyte cache memory for 16-bit words (Fig. 5). Two 2150s serve for tag storage and comparison and four 2149s hold the 16-bit data words. Taken together with some TTL packages—four 74S240 octal buffers and one 74S10—they make an 11-package tag and data-storage system that requires only a controller (not shown) to support a two-way interleaved backing dynamic memory. This cache board, which operates at a total delay from address input to valid-data output of less than 80 ns, can be applied to almost any 16-bit minicomputer or microprocessor system having a 22-bit address field.



4. The delay between the address input and the match output, $t_d(A)$, of the 2150 is relatively insensitive to variations in temperature or V_{CC}.

Acting as 8-bit-slice devices, the two 2150s split the processor address bus into two sections when comparing and matching addresses. When an address match is verified by both chips, the Match outputs—gated through G_1—supply an enable signal to the 74S240s configured as bidirectional buffers. In that way, address-input data can move from the 2149 static RAMs to the processor data bus.

When the write-enable ($\overline{WE}$) line is pulled low, data are entered into the 2149 RAMs from the processor, while the tag addresses of the data are entered into the 2150's internal tag-store RAM.□



5. The 2150 readily lends itself to building-block implementations of cache-memory systems, as in this 2-kbyte single-set cache that employs two 2150s for a 16-bit processor with a 22-bit address field. In addition, the cache system requires four TMS2149 static RAMs, four 74S240 bidirectionally connected buffers, and a 74S10 gate chip. Thus the cache circuit comprises 11 chips. Not shown is the hit/miss and controller circuit that a cache also requires.

Performance could be improved by fitting cache-memory hardware to the system software or fine-tuning the software to the cache hardware.

Match cache architecture to the computer system

The following article is the third in a series on cache-memory systems. The previous article covered the details of a particular cache tag-store and comparator IC (Feb. 18, 1982, p. 159). The first article covered the basic cache philosophy (Jan. 21, 1981, p. 179). Texas Instruments' overall approach was sketched by Richard N. Gossen, manager of Advanced Memory Development, in the Jan. 21 issue (p. 32).

Cache-system architecture can take many forms, each with its own performance advantages and disadvantages and differing degrees of economy. But for optimum performance, the architecture of a cache-memory system should be matched specifically to the architecture of the overall computer system. Moreover, the cache's hardware and operational logic should be fitted to both the statistical and structural properties of the computer system's software and be highly transparent to it.

Of course, existing software can also be tuned to fit a particular cache hardware and its functional properties. A properly configured and finely tuned cache software-hardware system can approach well over 80% of the throughput that a very expensive all-high-speed memory could deliver. What's more, a cache system can do it with a slow, low-cost bulk memory plus a small amount of additional high-speed hardware for the cache.

Very high speed memory is expensive; therefore, the typical computer system cannot afford too much. On the other hand, bulk memory offers a large amount of low-cost capacity, but it is slow. A cache-memory system can combine the advantages of the two types of memories economically: small, but fast memory in the cache with large but slow memory for bulk storage.

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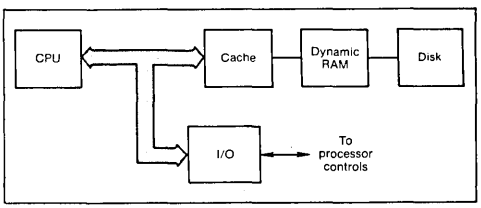
A well-designed cache-memory system can manage to keep the few most-likely-to-be-accessed data in the cache for quick reference, while the bulk memory serves as a backup on those occasions when the processor references data not contained in the cache. When successfully implemented, this approach yields an almost transparent, economical memory system with the capacity of the bulk storage, but with the quick response of the cache.

The memory system of an inexpensive microcomputer system today is likely to be made up of a relatively low-cost disk and dynamic RAMs. Such a two-level memory hierarchy is well-suited to the needs of the less expensive popular microprocessor, whose minimum memory cycle times are on the order of 500 ns. Some of the newer high-performance microprocessors, however, have much shorter cycle times. An example is the 24-MHz 16-bit TMS99000, whose minimum memory cycle is 167 ns. For such a processor to access a block of relatively slow dynamic RAM, it must be slowed down by adding wait states to each memory cycle. This can be avoided by adding a third level to the memory hierarchy in the form of a high-speed cache of relatively simple design. The performance of such a processor can be improved dramatically, and the cache itself will represent only an incremental cost to the total



1. Even a simple single-microprocessor system can benefit from a cache system. With it, the number of accesses that must be made to disks and slow main memories like dynamic RAMs can be reduced substantially.

system—especially with the help of support chips such as the TMS2150 cache address comparator to keep the chip count low.

Although the per-bit cost of disk and semiconductor memory has decreased dramatically in recent years, microcomputers remain expensive largely because each decrease in the per-bit cost of memory devices is countered by a proportionate increase in the size of the average memory system. However, adding a cache to a memory system can produce a more than proportionate yield on the user's investment in his memory system—in the form of more memory-access cycles per second per dollar.

But even though the addition of a cache to a conventional, centralized high-performance microcomputer can greatly increase memory effectiveness, even greater improvements are possible with a distributed-intelligence architecture. The centralized-processor arrangement shown in Fig. 1 is based on the economics of past years, when the processor part of the system represented a much larger part of the overall system cost than it does today. Now, the situation is different: to have a single $20 microprocessor control $1000 worth of memory no longer makes economic sense. Low-cost independent microprocessors with local I/O arrangements in a distributed-intelligence system not only makes more economic sense, but can provide substantially better overall performance by using more of the available memory bandwidth (Figs. 2 through 5).

Moreover, the amount of memory bandwidth available can be effectively improved through the addition of caches; hence, the distributed-intelligence processing system can benefit from properly applied caching even more than the centralized-processor system of Fig. 1. In the simplest distributed system (Fig. 2), a central, global, bulk-storage memory can serve many independent microprocessors along a common bus. As the number of processors on the bus increases, the system throughput at first increases proportionately. But the bus gradually saturates—its bandwidth capability can handle no more data (Fig. 3). Adding more processors soon does not improve overall throughput: Since access to the memory for all data and instructions, as well as messages between the processors, is via the bus, the bus quickly becomes very busy. As more processors are added, contention for the bus mounts, and delays become longer.

Distribute memory too

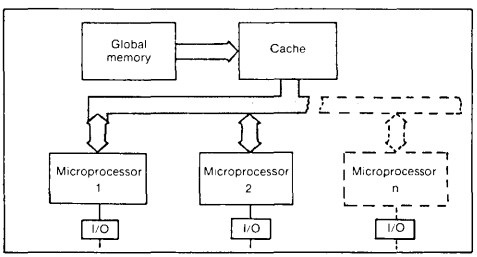
Moving some of the memory to the local sites of execution (Fig. 4)—in a so-called function-to-function architecture (FFA)[1]—will help alleviate bus-contention problems by locally storing most of the instructions and data needed for the special functions performed at that site. In this way, the global memory need contain just the shared data and those instructions needed for overall coordination, which together with interprocessor messages now have more "room" on the bus. This arrangement then allows still more processors to be handled with a given bus bandwidth.

Depending on the effort expended in organizing the software and the amount of local memory, the traffic on the bus can be cut way down—perhaps to as little as 10% of that of a nondistributed memory architecture. But to allow a high-performance microprocessor to operate at full speed, this local memory should be the fast, static-RAM type, which unfortunately is expensive and, in practice, limited to small capacities. However, configuring this small memory into a cache system would help matters since its capacity, though small, will be filled continually with current data (in a properly designed system). The small cache capacity would be as effective as a much larger static-RAM block mapped into a fixed set of memory addresses.

Moreover, with more of the bus bandwidth made available, entire blocks of data can be moved with each global-memory access. Block transfers from the global memory can have much the same advantage as moving blocks from a disk: Following the initial access time, the overhead time for each additional data word in the block is merely incremental.

For example, the global memory is likely to be made up of several dynamic RAMs, which support paged-mode operation. In this mode, only one row address is needed for a subsequent series of column addresses, which decreases the amount of overhead time per access. Or, the global-memory circuit may access not one, but several words in parallel, and then feed these to the system one-by-one at the maximum transfer rate of the bus. (Recent bus interfaces, such as the proposed IEEE-P896 standard, have been designed to support such efficient block transfers.)

Block transfers are particularly beneficial to



2. A distributed-intelligence, or function-to-function, system, having several local microprocessors instead of one centralized CPU, not only makes more economic sense, but can provide substantially better overall throughput.

caches because of their locality property, which characterizes the memory-access patterns of all programs. Basically, if a program accesses one word in a data or instruction block, it is likely to access other words in the same block subsequently. By reading the entire block into the cache at once, there's a good chance that the cache will be able to satisfy a greater number of additional access requests from the local processor without requiring more trips to the global memory for data.

Where to locate the cache

After the decision has been made to go with block transfers of data to the cache in the distributed-intelligence system, the next thing to determine is the location of the cache. In Fig. 2, the cache is located on the global-memory board. This cache location can decrease the time on the bus for memory accesses; accordingly, the bus is available for more data transfers. While this cache location decreases the overhead time per memory-data bus transfer, the number of such bus transfers remains the same as without the cache.

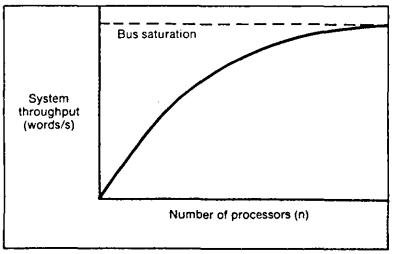
However, if the cache memory is located as in Fig. 4, the number of transfers over the bus is reduced. A block of data is accessed from main memory just once, but locally the same data can be used many times over without having to go back to the main memory via the bus. The bus bandwidth, thus freed up, now allows an increase in the amount of data transferred in each block. In addition, the cache block can be made large enough to achieve a desired hit ratio.

But if the processors run very long, uninterrupted programs and need just a few global-memory accesses, a simple FFA configuration (Fig. 4 without a cache, but with ordinary local memory) could be the most economical approach. With such programs, each processor executes the same on-board routines and accesses the same data locations repeatedly. Then the global memory need handle just messages between processors and system-wide instructions and data.

With the traffic on the bus reduced substantially, more processors can be added to the bus. And global-to-local-memory transfers could proceed via a direct-memory-access (DMA) system, which of course would be initialized under software control. Transfers via a local cache system (Fig. 4 with cache systems), however, would carry out the transfers automatically, transparent to the software.

Almost transparent

When a distributed system is implemented with local caches, the software is virtually unaware of the split between the local and global memories:



3. When a multiprocessor system shares a single bus, throughput rises proportionately at first with the number of processors, but tapers off as the bus's data-handling capacity saturates.

Hardware—the cache's control logic—maps the contents of each local cache into the global memory, and the cache is largely transparent to the software. (By comparison, in a DMA arrangement, the software would have to be totally involved in the local-global memory split.) Accordingly, with distributed cache systems, existing software (such as Pascal) for centralized-CPU systems can be used, with but minor modifications, for a higher-performance distributed-intelligence system.

Clearly, the distributed cache-system approach is general-purpose: All data and instructions can be mapped into the global memory as in the centralized system, and the local caches will then (almost) transparently remap the information for local use. In other words, the distributed system with local cache can best serve a general-purpose processing environment, where the specific functions of the individual processors cannot be predicted in advance, and thus where the contents of the local memories cannot be fixed at the time the system hardware is configured.

On the other hand, with a fairly fixed and predictable installation, perhaps with Fortran software, or in a plant-process-control application, where the data and software needed on each processor (board) are firmly established, the FFA approach could be used in place of local caches. But to achieve even greater performance, a distributed memory system can combine two or more of the approaches described. For example, cache memories can be employed for both the local and global memories—a combination of Figs. 2 and 4. The local cache decreases the number of references to the global memory, and the global cache decreases the average length of the bus cycles when global accesses do become necessary. Or, in a variation of the distributed-processor system of Fig. 2c, local memory and local cache can be used on the same processor. In Fig. 2d, the addition of a cache improves the performance of a large but slow local memory composed of 64-kbyte (or larger) dynamic RAMs.

Although, in general, employing local caches in a distributed system (like the one in Fig. 2c) will remove local instruction and data traffic from the bus and speed throughput substantially, trying to make the caches appear totally transparent can introduce interference problems with messages between processors. In the distributed system of Fig. 2c, for example, messages between processors should not be accessed through the local caches because this class of data is not held there: The caches contain only local current instructions and data from the global memory. As a result, in Fig. 3, when microprocessor 1 writes a message to microprocessor 2, the data should pass via a particular location in the global memory that acts as a message buffer. In the process, the local cache on the microprocessor-1 board must be prevented from intercepting the message. And when microprocessor 2 tries to read the message, its cache also must be removed from the message path. Otherwise, microprocessor 2 will encounter stale data in cache memory, and not the new message from microprocessor 1, which had just been deposited into the global-memory.

A write-through (as opposed to nonwrite through or write-back) caching policy can ensure microprocessor 1 writes its message to global memory, but additional steps are needed to ensure that microprocessor 2 reads the message from global memory without interference from its cache. Software recognition of the special status of interprocessor messages can easily solve this potential problem. But this approach constitutes a lack of total transparency for the caches.

One approach passes all interprocessor messages through the microprocessor's I/O space. Since I/O data are not cached, this strategy automatically avoids the interference problem. Interprocessor messages pass through the I/O space, bypassing the caches altogether. So if the software is initially written to handle the interprocessor messages via the I/O space, then when caches are introduced, they will automatically be transparent to the caches.

Alternately, a particular set of addresses in the global-memory space can be dedicated to message passing. The control logic in each processor-board's cache could incorporate a comparison circuit that recognized the message-space addresses and allows access to the message area in global memory to bypass the cache.

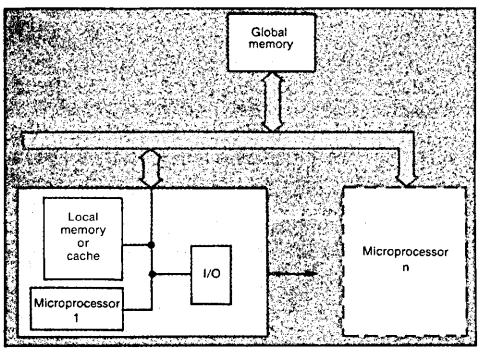
System data should also bypass the caches and be taken by a processor directly from the master copy in the main memory: Such data are constantly being updated by the other processors. If passed via the local caches, such data would invariably be perceived as stale because of the constant updating. If allocated to specific and exclusive global-memory addresses, these system data can be handled like the interprocessor messages to bypass the caches.

Similarly, each processor should have exclusive access to its own private instruction and data segments in the global memory. In this way, the data are "protected," with some support from bus hardware, from a processor that may go "berserk" and corrupt the instruction and data segments of the other processors in the system.

Clearly, with caches in distributed-intelligence systems, the memory accesses must be organized rationally to optimize throughput, avoid inefficient data thrashing and, most important of all, avoid using data belonging to other processors. Of course, with a single cache (as in Figs. 1 and 2), it is rather difficult to mix up the data, since the cache should always contain updated master versions of the corresponding blocks of memory (which is never changed without knowledge of the cache). In a multiprocessor system like Fig. 4, however, each local cache is supposed to keep a separate, accurate copy of some portion of the global memory—as it pertains to its own processor. But a mixup is possible because of the multiplicity of processors.

The point of all this is that it is exceedingly difficult to make the cache memories in a distributed system totally transparent to software, while simultaneously ensuring that each processor is provided with a coherent, updated version of the contents of global memory. Methods have been proposed for accomplishing just this, but they tend to be expensive in terms of the hardware required, and are therefore beyond the reach of the typical microprocessor-based system.

In some systems, the entire contents of the cache may have to be "flushed," if for any reason its

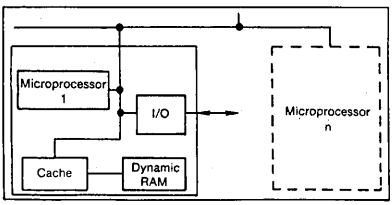


4. A cache, located at the slow global memory as in Fig. 2, can reduce the number of required slow accesses to main memory, thus leaving the bus more time for other activities. But locating part of the memory at each processor—in a distributed architecture—is even better.

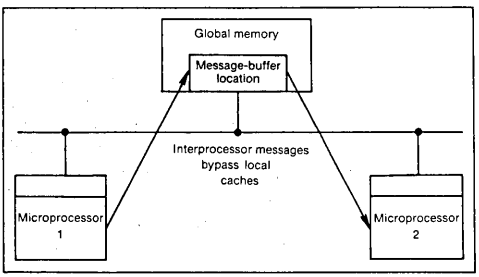
contents have become invalid. For example, a DMA device may alter the contents of main memory, invalidating the contents of the cache. Also, consider the case of a processor attached to a memory mapper (like a 74LS610), which translates the logical addresses output from the processor into the physical addresses used to access the memory. A cache will usually be attached directly to the processor to avoid lengthening the cache access time with the propagation delay through the mapper circuitry. However, this means that the cache contents are mapped into the logical rather than the physical address space. Consequently, when the map file is altered, this makes the cache contents invalid since the mapping of the logical into the physical address space is no longer the same.

For applications where the cache contents must frequently be flushed, a cache-reset function is essential. Without the ability to flush the cache instantaneously, the system would be forced to clear each cache block, one by one.

But flushing the entire cache when just a small portion of its contents needs updating is wasteful. Naturally, a more complex reloading arrangement can be designed to provide higher caching efficiency where only part of the cache data must be replaced frequently, but only at the expense of increased overhead in logic and software. Selectively dumping only the affected areas of the cache capacity—such as when a DMA operation partially alters the contents of the global memory—instead of a total reset, would be more efficient, but also much more expensive. It would also occupy more board space.



5. The local memory can be in "ordinary" RAM form (as in function-to-function architecture) or in cache form. Or, both a cache and a local dynamic RAM can be used.



6. Interprocessor messages should bypass caches to avoid interference. This can be accomplished with the software or special overhead hardware, or by employing the microprocessor's I/O space to carry the messages.

Complexity requires board space. With the trend to smallness in electronic packaging, sometimes compromises must be made. CPU speed is generally compromised when going from a multiboard minicomputer design to a design that just barely crams a CPU onto a single board. To put substantial memory onto the board as well usually requires going to a slower microcomputer design, which puts the CPU into a chip, and leaves board room for the memory. However, the speed lost because of these compromises can be partially recovered by incorporating a cache on the board (or even on the microprocessor chip). The cache effectively raises the individual processor's memory access speed when it is used with a slow on-board dynamic RAM (Fig. 5).

The TMS9995 microprocessor is a precache step in this direction: It contains a modest chunk (256 bytes) of high-speed random-access memory, which is mapped into a fixed area of the processor's address space. Thus, it does not qualify strictly as a cache. However, it can be used to the same effect by loading the RAM—under explicit software control—with currently needed data and instructions.

The next step would be to put a cache on the processor board (or chip) with as much memory as the board space allows, all of which would be almost transparent to the system software. Equally important, a cache could make the most of the limited amount of memory that now can be put onto a board with the microprocessor and I/O.

Despite the transparency, a programmer who is aware of the cache's capability can fine-tune the software to maximize its efficiency. On the other hand, overly refined software for one hardware system can produce poor efficiency on another, while remaining transportable in the sense that it executes without error. But as software can be adapted to maximize the efficiency of cache configuration and minimize its limitations, so can cache-system hardware be designed to best fit very extensive existing software. It is a two-way street.□

References

1. "Functional Architecture Threatens Central CPU," ELECTRONIC DESIGN, Sept. 3, 1981, p. 141-156.

4 Error Detection and Correction (EDAC)

4.1 Use of an Error Detection and Correction (EDAC) Device

4.1.1 Introduction

The DRAM technology of today (i.e., 256K/M) has enabled system designers to use much larger memory sizes than ever before. However, as with most advances in technology, this has brought a new problem. For system memory sizes larger than 1/2 million bits, it is generally considered that error detection and correction is required to guarantee system reliability without a tradeoff in performance. Although present methods of parity checking will identify errors, they are not able to correct them. And not correcting these errors can be costly. For example, in personal computers when parity errors are encountered, the system has to be reset to eliminate the problem. This system reset destroys any data stored in RAM and it must be reentered. Obviously this is unacceptable to your customers. To eliminate this problem, TI has produced a cost effective Error Detection and Correction (EDAC) device.

4.1.2 Error Types and Sources in Dynamic Memories

Two kinds of errors occur in memory devices; soft and/or hard errors. A hard error is a physical failure of the memory device (e.g., an internal short or an open lead). This type of error causes the memory location to always be either a high or a low. A soft error is a random occurrence of a memory location change from a high level to low level. These errors may be caused by system noise, alpha particle radiation, or power surges.

In spite of design techniques used by memory chip manufactures to reduce these errors, they are still a source of major concern in your system. Table 4-1 indicates that as the density of memory chips increase their probability of errors also increase. Therefore, your data integrity decreases in larger memory arrays.

Table 4-1. Chip Densities vs Soft-Error Rates

CHIP DENSITY BITS/CHIP	TYPICAL SOFT-ERROR RATE (% PER 1000 HOURS)
64K	0.10 – 0.20
256K	0.15 – 0.30
1M	0.20 – 0.35

4.1.3 Solutions to Boost System Reliability

There are several alternatives available that will either decrease or eliminate these errors in your system. One method used to determine data integrity is the incorporation of parity checking. This can be accomplished by using an SN74ALS29833 Parity Bus Transceiver. To identify an error, the data word and the generated parity are compared by performing an exclusive-OR operation. If several bits in the data word are in error or the parity has changed, the exclusive-OR output would be low. While data integrity can be determined using this method, it is unable to correct errors.

To obtain the desired level of quality, some type of error-correction scheme must be incorporated. An EDAC chip provides the simple solution to the problem, while dramatically extending the system Mean Time Between Failures (MTBF). This is accomplished by detecting and correcting single bit errors and detecting double bit errors. See Table 4-2.

Table 4-2. System MTBF Increases with an EDAC

	MTBF†	
	Without EDAC	With EDAC
CORRECTABLE SOFT ERROR (SINGLE BIT)	7 Months	>200 Years

†Based on 16M-Bit memory system using 256K DRAMs with a 0.30% per 1000 hour soft error rate.

When you include the other system variables causing errors (power surges, noisy systems, etc.), your memory system MTBF, without an EDAC could be reduced to several days. These types of memory-cell errors can be corrected using an EDAC.

4.1.4 EDAC Operation

When data is written to memory, the TI SN74AS632 (32-Bit EDAC) generates parity check bits. Each check bit is generated by performing a specific parity check on the 32-bit data word. For example, CB0 is obtained by comparing specific bits of the 32-bit word with those corresponding to an "X" in the Hamming Code Parity Algorithm (see Table 4-3). CB0 will be at a high level if the total number of highs corresponding to these locations is an odd number. CB0 will be at a low level if this number is even. This procedure is repeated 7 times to obtain the 7 check bits, CB0-CB6 of the Hamming Code. Check bits CB0-CB2 are used to determine odd parity. Check bits CB3-CB6 are used for even parity.

Table 4-3. Hamming Code Parity Algorithm

CHECK WORD BIT	32-BIT DATA WORD																														
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X				X
CB1				X		X		X		X		X		X	X	X				X		X		X		X		X		X	X	X
CB2	X		X			X	X		X			X	X			X	X		X			X	X		X			X	X			X
CB3			X	X	X				X	X	X				X	X			X	X	X				X	X	X				X	X
CB4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

These check bits are stored along with the data in your systems main memory. This additional memory requirement is the only overhead involved with the use of an EDAC. Figure 4-1 shows a typical system using an EDAC and illustrates this overhead.

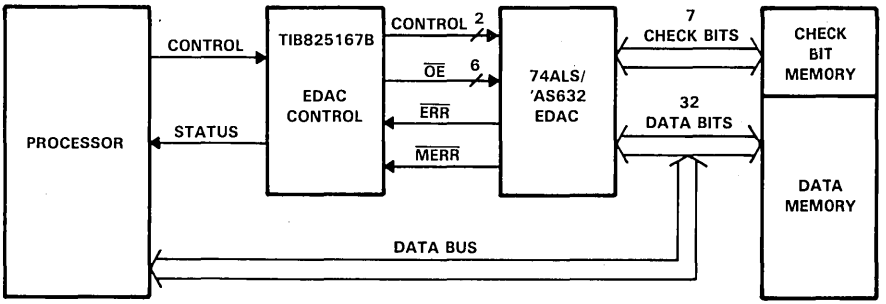


Figure 4-1. Typical 'AS632 System

During a read cycle, the data and check bits are read from memory, any of which may be invalid. New check bits are computed from the stored data bits. To determine the validity of the data, the new and old check bits are exclusive-ORed producing a 7-bit syndrome code. When decoded, these syndrome bits describe the condition of the data word: free of errors, having a single bit error, or having multiple errors. See Table 4-4. Any single error in the 32-bit word can be corrected. Both single and double bit errors are indicated to the processor via single and double bit error flags.

There are two additional options for implementing EDAC into your system; detect only and correct always. Of these two, correct always is the easiest to implement. The EDAC always corrects single-bit errors and writes this corrected word onto the system data bus or into memory.

Because days can elapse between errors, correction can be done only when needed. The detect-only option increases your system performance during a read cycle by allowing data to be written directly to the system processor. If a single or double bit error occurs, the EDAC will flag the processor. This enables the processor to enter a wait cycle until the word is corrected. This method of implementation does not use the error correction portion of the EDAC until the processor determines what action to take in the event of an error.

Another method of ensuring data integrity in your system is to use an EDAC unit during memory refresh. The EDAC will "clean" every memory location of errors during the mandatory refresh cycles. This process is known as memory scrubbing. The data can then be checked again during a memory-access cycle. By checking the data twice, the time between corrections is reduced. Therefore, the probability of multibit errors in your system declines.

Table 4-4. 'AS632 Syndrome Decoding

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	L	L	L	L	L	L	unc
L	L	L	L	L	L	H	2-bit
L	L	L	L	L	H	L	2-bit
L	L	L	L	L	H	H	unc
L	L	L	L	H	L	L	2-bit
L	L	L	L	H	L	H	unc
L	L	L	L	H	H	L	unc
L	L	L	L	H	H	H	2-bit
L	L	L	H	L	L	L	2-bit
L	L	L	H	L	L	H	unc
L	L	L	H	L	H	L	DB31
L	L	L	H	L	H	H	2-bit
L	L	L	H	H	L	L	unc
L	L	L	H	H	L	H	2-bit
L	L	L	H	H	H	L	2-bit
L	L	L	H	H	H	H	DB30
L	L	H	L	L	L	L	2-bit
L	L	H	L	L	L	H	unc
L	L	H	L	L	H	L	DB29
L	L	H	L	L	H	H	2-bit
L	L	H	L	H	L	L	DB28
L	L	H	L	H	L	H	2-bit
L	L	H	L	H	H	L	2-bit
L	L	H	L	H	H	H	DB27
L	L	H	H	L	L	L	DB26
L	L	H	H	L	L	H	2-bit
L	L	H	H	L	H	L	2-bit
L	L	H	H	L	H	H	DB25
L	L	H	H	H	L	L	2-bit
L	L	H	H	H	L	H	DB24
L	L	H	H	H	H	L	unc
L	L	H	H	H	H	H	2-bit

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	H	L	L	L	L	L	2-bit
L	H	L	L	L	L	H	unc
L	H	L	L	L	H	L	DB7
L	H	L	L	L	H	H	2-bit
L	H	L	L	H	L	L	DB6
L	H	L	L	H	L	H	2-bit
L	H	L	L	H	H	L	2-bit
L	H	L	L	H	H	H	DB5
L	H	L	H	L	L	L	DB4
L	H	L	H	L	L	H	2-bit
L	H	L	H	L	H	L	2-bit
L	H	L	H	L	H	H	DB3
L	H	L	H	H	L	L	2-bit
L	H	L	H	H	L	H	DB2
L	H	L	H	H	H	L	unc
L	H	L	H	H	H	H	2-bit
L	H	H	L	L	L	L	DB0
L	H	H	L	L	L	H	2-bit
L	H	H	L	L	H	L	2-bit
L	H	H	L	L	H	H	unc
L	H	H	L	H	L	L	2-bit
L	H	H	L	H	L	H	DB1
L	H	H	L	H	H	L	unc
L	H	H	L	H	H	H	2-bit
L	H	H	H	L	L	L	2-bit
L	H	H	H	L	L	H	unc
L	H	H	H	L	H	L	unc
L	H	H	H	L	H	H	2-bit
L	H	H	H	H	L	L	unc
L	H	H	H	H	L	H	2-bit
L	H	H	H	H	H	L	2-bit
L	H	H	H	H	H	H	CB6

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	L	L	L	L	L	L	2-bit
H	L	L	L	L	L	H	unc
H	L	L	L	L	H	L	unc
H	L	L	L	L	H	H	2-bit
H	L	L	L	H	L	L	unc
H	L	L	L	H	L	H	2-bit
H	L	L	L	H	H	L	2-bit
H	L	L	L	H	H	H	unc
H	L	L	H	L	L	L	unc
H	L	L	H	L	L	H	2-bit
H	L	L	H	L	H	L	2-bit
H	L	L	H	L	H	H	DB15
H	L	L	H	H	L	L	2-bit
H	L	L	H	H	L	H	unc
H	L	L	H	H	H	L	DB14
H	L	L	H	H	H	H	2-bit
H	L	H	L	L	L	L	unc
H	L	H	L	L	L	H	2-bit
H	L	H	L	L	H	L	2-bit
H	L	H	L	L	H	H	DB13
H	L	H	L	H	L	L	2-bit
H	L	H	L	H	L	H	DB12
H	L	H	L	H	H	L	DB11
H	L	H	L	H	H	H	2-bit
H	L	H	H	L	L	L	2-bit
H	L	H	H	L	L	H	DB10
H	L	H	H	L	H	L	DB9
H	L	H	H	L	H	H	2-bit
H	L	H	H	H	L	L	DB8
H	L	H	H	H	L	H	2-bit
H	L	H	H	H	H	L	2-bit
H	L	H	H	H	H	H	CB5

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	H	L	L	L	L	L	unc
H	H	L	L	L	L	H	2-bit
H	H	L	L	L	H	L	2-bit
H	H	L	L	L	H	H	DB23
H	H	L	L	H	L	L	2-bit
H	H	L	L	H	L	H	DB22
H	H	L	L	H	H	L	DB21
H	H	L	L	H	H	H	2-bit
H	H	L	H	L	L	L	2-bit
H	H	L	H	L	L	H	DB20
H	H	L	H	L	H	L	DB19
H	H	L	H	L	H	H	2-bit
H	H	L	H	H	L	L	DB18
H	H	L	H	H	L	H	2-bit
H	H	L	H	H	H	L	2-bit
H	H	L	H	H	H	H	CB4
H	H	H	L	L	L	L	2-bit
H	H	H	L	L	L	H	DB16
H	H	H	L	L	H	L	unc
H	H	H	L	L	H	H	2-bit
H	H	H	L	H	L	L	DB17
H	H	H	L	H	L	H	2-bit
H	H	H	L	H	H	L	2-bit
H	H	H	L	H	H	H	CB3
H	H	H	H	L	L	L	unc
H	H	H	H	L	L	H	2-bit
H	H	H	H	L	H	L	2-bit
H	H	H	H	L	H	H	CB2
H	H	H	H	H	L	L	2-bit
H	H	H	H	H	L	H	CB1
H	H	H	H	H	H	L	CB0
H	H	H	H	H	H	H	none

CB X = error in check bit X
DB Y = error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

The circuit illustrated in Figure 4-2 is an example of a memory system that used scrubbing. This circuit consists of the TI SN74ALS6302, a 1M-DRAM Controller, the TMS4C1024, 1M DRAMs, the SN74AS632, a 32-bit EDAC, and control circuits.

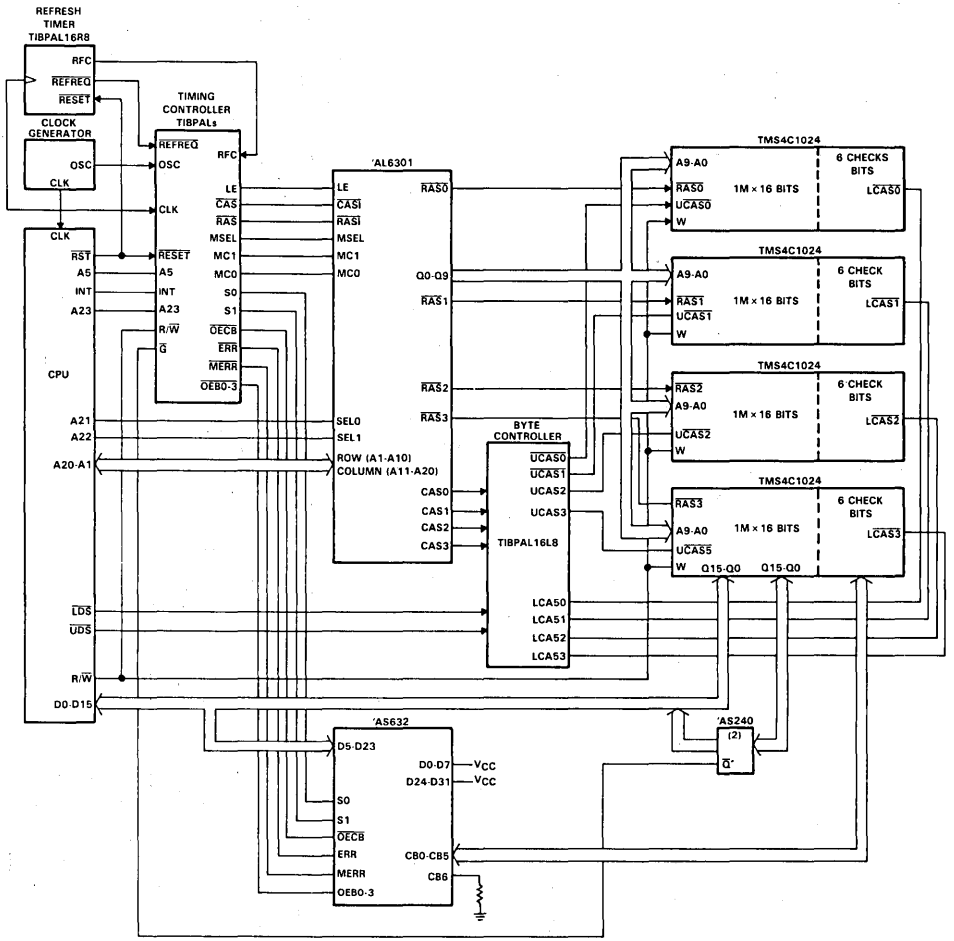


Figure 4-2. Memory Management Systems Using Scrubbing

4.1.5 Texas Instruments EDAC Family

Because of the increase in MTBF, the SN74AS632 can increase system reliability typically by well over 500-fold. The 'AS632 provides built-in diagnostics to assure reliable device operation. Byte-write capability is included to allow operation on 8-bit, 16-bit, or 32-bit word widths in 3-state bus applications. The 'AS632 provides the fastest correction time, 32 ns, and error-detection time, 25 ns, available today. The architecture of the 'AS632 is illustrated in Figure 4-3.

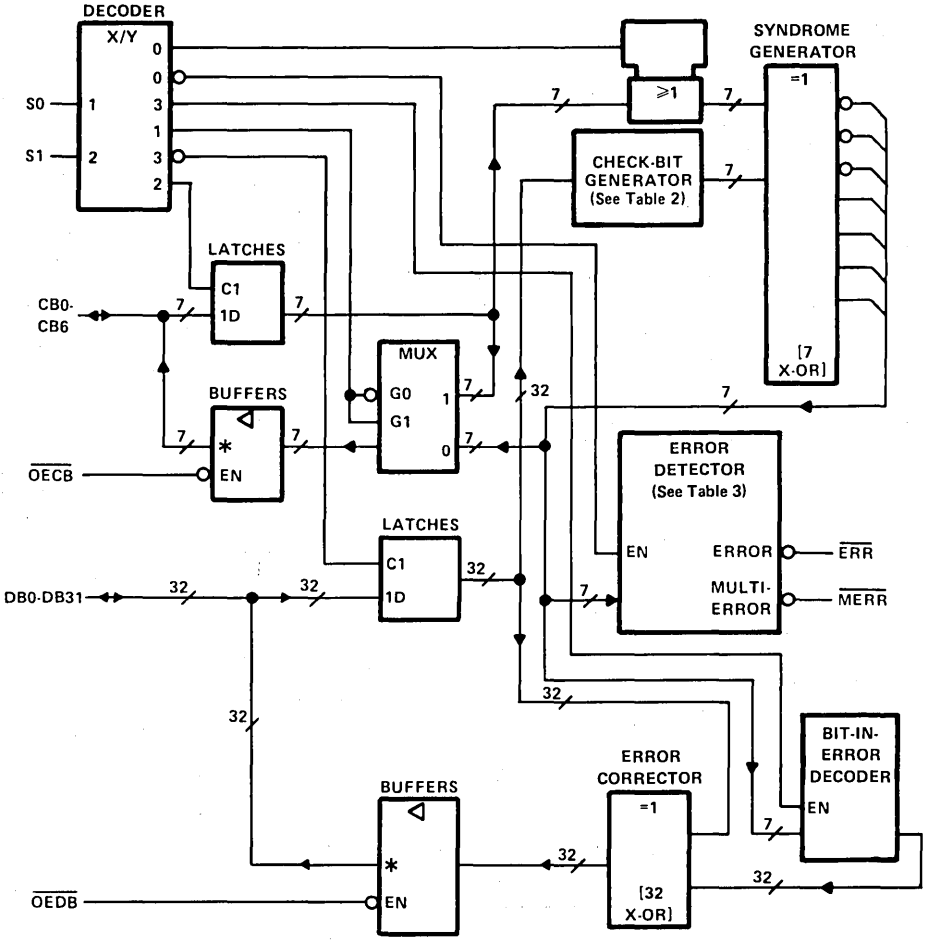


Figure 4-3. 'AS632 Logic Diagram

Along with the 'AS632 32-bit EDAC, TI has a complete family of high-performance EDAC products to fit your particular application. See Table 4-5.

Table 4-5. Texas Instruments Error Detection and Correction Devices

DIP PINS	DEVICE TYPE	DETECTION† TIME (MAX)	CORRECTION TIME (MAX)	FEATURES	AVAILABLE
40	ALS616	40	65	16-BIT, 3-STATE	NOW
40	AS616	25‡	32	SPEED ENHANCED ALS616	2Q87
28	LS630	30	65	16-BIT, NO BYTE-WRITE, 3-STATE	NOW
28	LS631	30	65	16-BIT, NO BYTE-WRITE, OPEN COLLECTOR	NOW
52	ALS632A	40	58	32-BIT, 3-STATE	NOW
52	ALS632B	30	37	SPEED ENHANCED ALS632A	NOW
52	AS632	25	32	FASTEST EDAC AVAILABLE	NOW
48	ALS634A	40	58	32-BIT, NO BYTE-WRITE, 3-STATE	NOW
48	AS634	25‡	32	SPEED ENHANCED ALS634	1Q87

†Single Bit Error
‡Design Goals

All of the products listed in Table 4-5 offer the following:

1. Built-in Diagnostic Capabilities
2. Modified Hamming Code Operation
3. Dependable Texas Instruments Quality and Reliability

4.1.6 Summary

Memory errors are becoming a very important concern to the system designer. To effectively ensure data integrity, a method of correcting data errors is necessary. An EDAC unit provides you with this essential function along with increasing system MTBF from days to years. The TI EDAC family offers you ease of implementation, high performance, and a device that is compatible with any microprocessor you might be using.

For more information on the TI family of EDAC devices, please contact your local TI Sales Representative or the Customer Response Center at 1-800-232-3200.

For your convenience, the TI documentation is listed below.

	TI Reference Number
Error Detection and Correction Application Reports:	
SN54/74LS630 or SN54/74LS631	SDLA003
SN54/74ALS632B, 'ALS633, 'ALS634A, 'ALS635	SDAS102
Data Sheets:	
SN54/74AS632	SDAS101
SN54/74ALS632B, 'ALS633, 'ALS634A, 'ALS635	SDAS105B
SN54/74ALS616, 'ALS617	SDAS047
SN54/74LS630, 'LS631 (TTL Data Book Vol. 2)	SDLD001
LSI Data Book	SDVD001

4.2 Error Detection and Correction Using 'ALS632B, 'ALS633, 'ALS634A, and 'ALS635

4.2.1 Introduction

With memory systems continuing to expand and the expectation of 256K-byte DRAMs in the near future, error detection and correction has become increasingly important. Generally, the larger the chip density, the greater the probability for device errors. It is easy to recognize this probability when one considers that a 32-bit × 64K-byte memory, using 64K-byte DRAMs, equals approximately 2.1 million bits of information. This expands to 8.4 million bits of information when using 256K-byte DRAMs. For memory sizes larger than 0.5 million bits, error detection and correction is required to guarantee high reliability.

The SN54/74ALS632B, SN54/74ALS633, SN54/74ALS634A, and SN54/74ALS635 provide a solution to these requirements in 32-bit machines. In addition, the 'ALS632B and 'ALS633 provide the necessary hardware to perform byte-write operations which are typically used in the more advanced systems. To ensure the integrity of the error detection and correction circuit, diagnostic capabilities have been provided in all four devices.

The 'ALS632B series devices are not limited to 32-bit systems. They can be implemented in 16- or 24-bit systems. In the case of 16-bit systems, the additional memory needed for holding the check bits can be reduced when compared to conventional 16-bit EDACs.

The pin functions are listed in Table 4-6. Mechanical data for the 'ALS632B, 'ALS633, 'ALS634A, and 'ALS635 is shown in Figure 4-4.

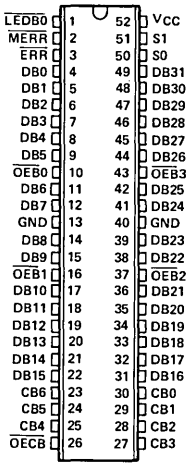
Table 4-6. Pin Function for 'ALS632B, 'ALS633, 'ALS634A, and 'ALS635

PIN NAME	DESCRIPTION
S1, S0	Selects the operating mode of the EDAC S1 S0 MODE OPERATION L L WRITE Input dataword and output checkword H L READ & FLAG Input dataword and output error flags H H CORRECT Latched input data and checkword/output corrected Data and error syndrome code L H DIAGNOSTIC Input various datawords against latched checkword/output valid error flags
DB0 through DB31	I/O port for entering or outputing data
$\overline{OEB0}$ through $\overline{OEB3}$ ('ALS632B, 'ALS633)	Three state control for the data I/O port. A high allows data to be entered, and low outputs the data. Each pin controls 8 data I/O ports (or one byte). $\overline{OEB0}$ controls DB0 through DB7, $\overline{OEB1}$ controls DB8 through DB15, $\overline{OEB2}$ controls DB16 through DB23, and $\overline{OEB3}$ controls DB24 through DB31.
$\overline{OEDB}$ (ALS634, ALS635)	Three state control for the data 1/O port. When low allows data to outputed and a high allows data to be entered.
$\overline{LEDB0}$	Controls the dataword output latch. When low, the data output latch is transparent. When high, the latch stores whatever data was setup at its inputs when the last low to high transistion occured on the pin.
CS0 through CS6	I/O Port for entering or outputing the checkword. It is also used to output the syndrome error code during the error correction mode.
$\overline{OECS}$	Three state control for the checkword I/O port. A high allows data to be entered and a low allows either the checkword or syndrome code (depending on EDAC mode) to be outputed.
$\overline{ERR}$	Single error output flag, a low indicates at least a single bit error.
$\overline{MERR}$	Multiple error output flag, when low indicates two or more errors present

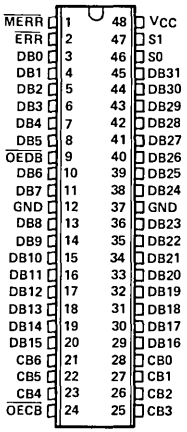
ceramic packages – side-braze (JD suffix)

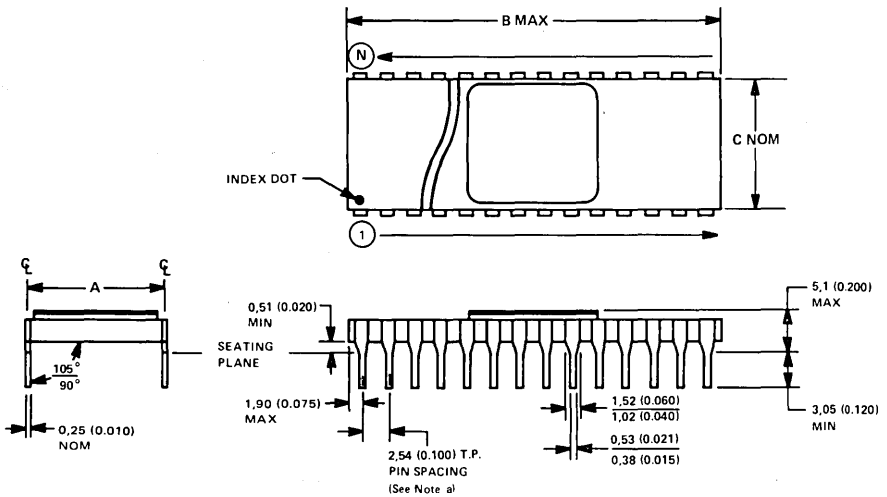
This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

'ALS632B, 'ALS633 . . . JD PACKAGE
(TOP VIEW)



'ALS634A, 'ALS635 . . . JD PACKAGE
(TOP VIEW)





DIM \ PINS	48	52
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)
B MAX	62,2 (2.45)	67,3 (2.65)
C NOM	15,0 (0.590)	15,0 (0.590)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

Figure 4-4. Mechanical Data

4.2.2 Operational Description

4.2.2.1 Write Mode

During a memory write cycle, the EDAC is required to generate a 7-bit check word to accompany the 32-bit data word before being written into memory. To place the 'ALS632B, 'ALS633, 'ALS634A and 'ALS635 in the write mode, take S1 and S0 low. Output-enable controls $\overline{OEB0}$ through $\overline{OEB3}$ for the 'ALS632B, 'ALS633 or $\overline{OEDB}$ for the 'ALS634A, 'ALS635 must be taken high before the data word can be applied. Output-enable control $\overline{OECS}$ must be taken low to pass the check word to the external bus.

The check word will be generated in not more than 30 ns after the data word has been applied. During the write mode, the 'ALS632B series EDACs can be made to appear transparent to memory, because typical write times of most DRAMs are much larger than the propagation delay of data to check word.

4.2.2.2 Read-Flag-Correct Operation

During a memory read cycle, the function of the 'ALS632B series EDACs is to compare the 32-bit data word against the 7-bit check word previously stored in memory. It will then flag and correct any single-bit error which may have occurred. Single-bit errors will be detected through the ERR flag and double-bit errors will be detected through the MERR flag. Figure 4-5 shows a typical timing diagram of the read-flag-correct operation.

When S0 is taken high, the EDAC will begin the internal correction process, although the error flags are enabled while in the read mode. For many applications, the simplest operation can be obtained by always executing the correction cycle, regardless if a single-bit error has occurred.

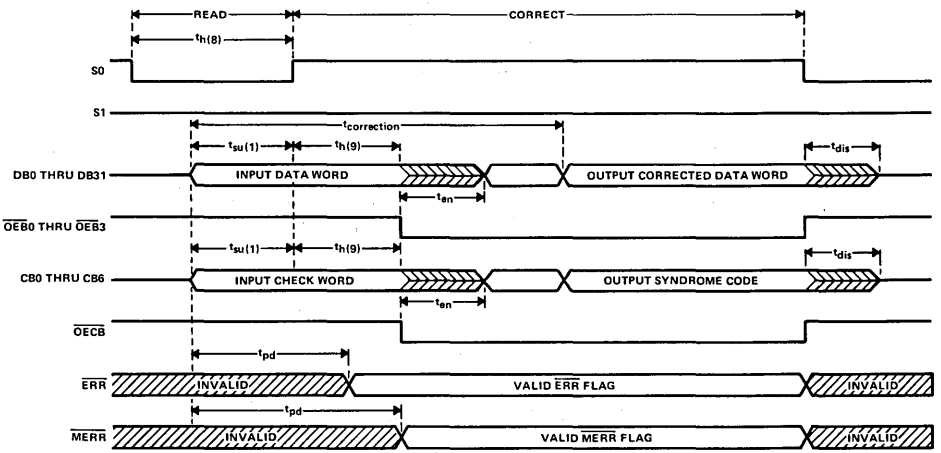


Figure 4-5. Read-Flag-Correct Timing Diagram

4.2.2.3 *Important Timing Considerations for Read-Flag-Correct Mode*

The most frequently asked question for an EDAC is how fast can a correction cycle be executed. Before S0 can be taken high, the data and check word must be set up for at least 5 ns. In addition, the data and check word must be held for at least 10 ns after S0 goes high. This ensures that the data and check word are saved in the EDAC input latches. After the hold time has been satisfied, the source which is driving the data bus can be placed in high impedance and the EDAC's output drivers can be enabled. This is accomplished by taking $\overline{OEB0}$ through $\overline{OEB3}$ ('ALS632B, 'ALS633) or $\overline{OEDB}$ ('ALS634A, 'ALS635) low.

If the minimum data setup time is used as a reference and the output drivers are enabled after the minimum data hold time, then correction will be accomplished in 37 ns or less.

4.2.2.4 *Read-Modify-Write Operations*

The 'ALS632B and 'ALS633 contain the necessary hardware to perform byte-write operations. The 'ALS634A and 'ALS635 are not capable of byte-write operations because they do not contain an output data latch or individual byte controls. When performing a read-modify-write function, perform the read-flag-correct cycle as previously discussed and shown in Figure 4-5. This ensures that corrected data is used at the start of the modify-write operation.

The corrected data is then latched into the output data latch by taking $\overline{LEDBO}$ from low to high. Upon completing this, modifying any byte or bytes is accomplished by taking the appropriate byte control $\overline{OEB0}$ through $\overline{OEB3}$ high. This allows the user to place the modified byte or bytes back onto the data bus while retaining the other byte or bytes. An example of a read-modify-write for byte 0 is shown in Figure 4-6.

Since the check word is no longer valid for the modified data word, a new one is generated by taking S0 and S1 low. After the appropriate propagation delay, the new check word will be available.

4.2.2.5 *Important Timing Considerations for Read-Modify Write Operations*

$\overline{LEDBO}$ should not be transitioned from low to high for 30 ns after S0 goes high. This ensures that corrected data is latched into the data output latches. However, $\overline{LEDBO}$ should be taken high before either S0 or S1 go low. Again, this is to ensure that the corrected data is stored into the data output latches. It is important that the new check word be available no later than 32 ns after S0 and S1 go low.

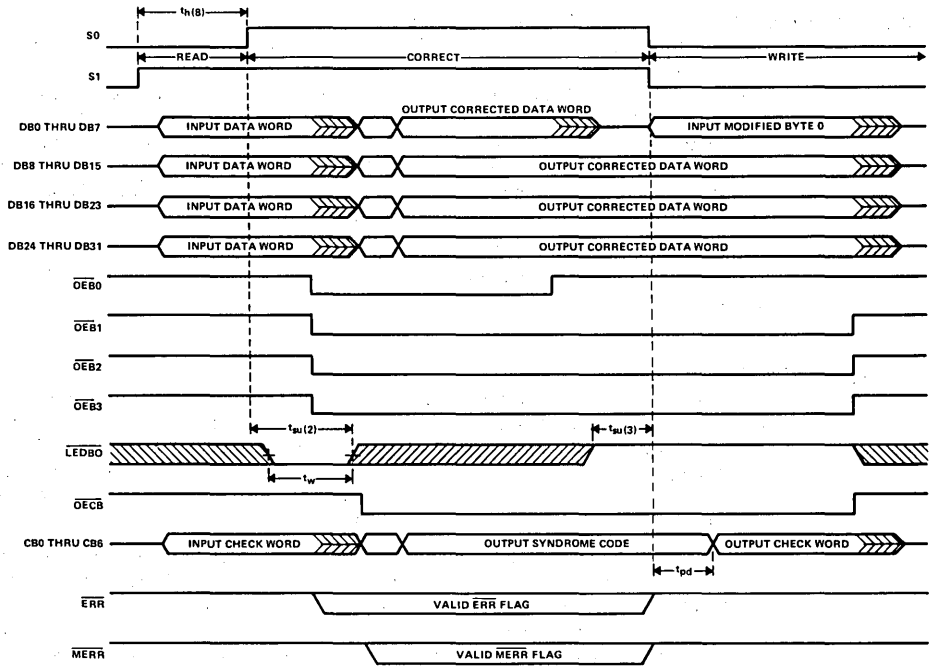


Figure 4-6. Read-Modify-Write Operation

4.2.2.6 Diagnostic Mode Operation

The purpose of the diagnostic mode is to provide the capability of detecting when the EDAC or memory is failing. There are several possible methods of using this feature. Figure 4-7 shows a typical timing diagram of some diagnostics which can be performed with these devices. Generally, the EDAC is first placed in the read mode (S0 = L, S1 = H) and a valid check word and data word are applied. A valid check word is one in which the associated data word is known. The EDAC is next placed into the diagnostic mode by taking S0 high and S1 low. This latches the valid check word into the input latches but leaves the data input latches transparent. To verify that the valid check word was properly latched, $\overline{OECS}$ can be taken low causing the valid check word to be placed back onto the bus. Since the data input latches remain transparent, this allows various diagnostic data words to be applied against the valid check word. A diagnostic data word is one in which either a single- or double-bit error exists. In either case, the error flags respond. The output data latch can be verified by taking $\overline{LEDBO}$ high and confirming the stored diagnostic data word is the same. This is possible because error correction is disabled while in the diagnostic mode (S0 = H, S1 = L). Taking S1 high and $\overline{LEDBO}$ low will verify that the EDAC will correct the data word. In addition, the error-syndrome code can be verified by taking $\overline{OECS}$ low. It should be noted that only the 'ALS632B and 'ALS633 are capable of this pass through verification of the diagnostic data word. The 'ALS634A and 'ALS635 do not have the output data latch required to perform this function.

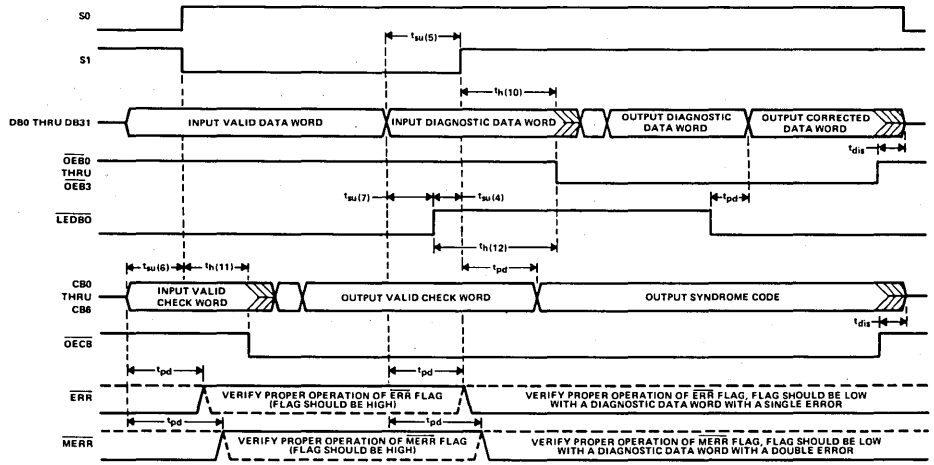


Figure 4-7. Diagnostic Mode Timing Diagram

4.2.2.7 16-Bit Systems Using the 'ALS632B Series EDACs

The 'ALS632B series EDACs can reduce the memory size required in 16-bit systems where conventional 16-bit EDACs (6 check bits, 16 data bits) are presently used. Figure 4-8 shows the typical system architecture for the 16-bit EDAC. In this system, 88 devices would be required for the 22-bit × 256K-byte memory array, assuming 64K-byte DRAMs are used. It is easy to see that 27.3%, or 24 devices, are required for storing the check bits. When using the 'ALS632B series EDACs, the memory required for the check bits can be reduced to 17.9%, or only 14 devices. This reduces the total number of DRAMs required by 10 devices. Figure 4-9 shows the architecture using the 32-bit EDAC. The four 'LS646s are used to group two 16-bit data words into one 32-bit data word. In addition, this type of system can be used in byte-write operations where the other system cannot.

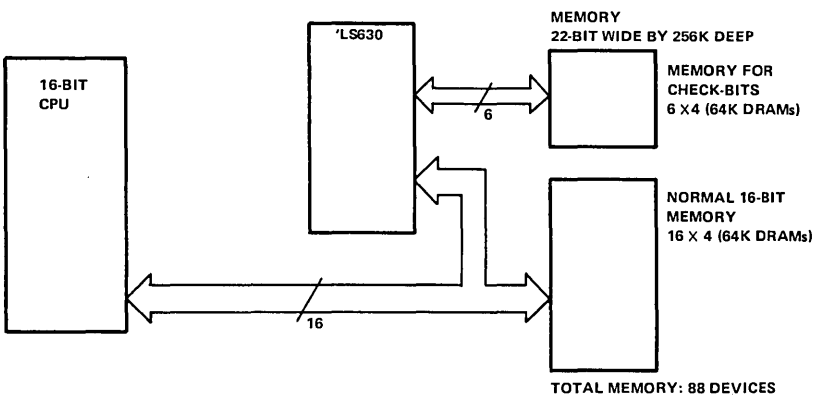


Figure 4-8. 16-Bit System Using Conventional 16-Bit EDAC

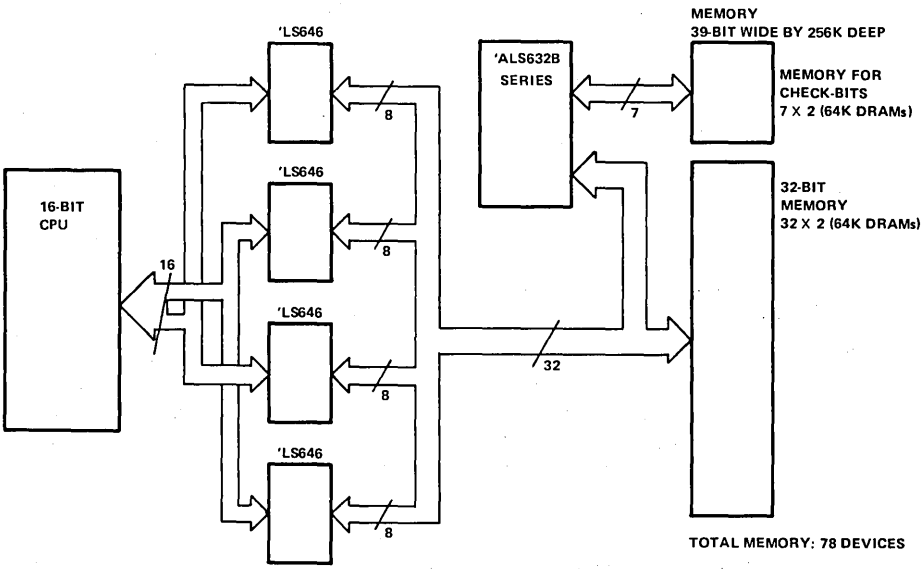


Figure 4-9. 16-Bit System Using 32-Bit EDAC

5 First-In First-Out Memories (FIFO)

5.1 High-Speed Bus Coupling Considerations - FIFO Memory Buffers

5.1.1 Introduction

High-speed First-In-First-Out (FIFO) memory buffers are becoming very important tools for those system design engineers looking for innovative ways to increase system performance. Texas Instruments (TI) brought you the first monolithic FIFO (SN74S225). But many of present day systems require more than the SN74S225 can provide. To meet the needs of those systems, TI has designed an enhanced family of IMPACT™ Bipolar and EPIC™ CMOS FIFO products. Table 5-1 lists some typical applications, key requirements, and the TI FIFO available to meet those needs.

Table 5-1. FIFO Applications

APPLICATION	KEY REQUIREMENTS	FIFO PRODUCTS
CPU Buffering	Data rate of processor Word width/depth Zero fall-through	'LS222/224/227/228 'ALS229A/232A/233A 'ALS2232/2233/2234
Peripheral I/O	Deep/fast Data-path synchronization Status flags	'ALS234/235/236 'ALS2232/2233/2234 TACT7202 TACT2202
Data Acquisition	High data rate	'ALS229A/232A/233A 'ALS234/235/236 'ALS2232/2233/2234
Data/Telecom	Low power/large depth Status flags	TACT7202 TACT2202

This report explains how a TI FIFO can help boost your system performance by maximizing data transfer rates, handling large data streams, or matching different transfer rates. It will also define FIFO architectures and the details of the design considerations needed.

A FIFO is a dual-port buffer memory that is organized in a manner that the first data entered into the memory is the first removed. One port is the input, where the data "producer" enters words into the buffer. The other port is the output, where the data "consumer" removes words. Data in the buffer cannot be randomly addressed like a RAM. A FIFO operates much like a line of people at a checkout counter.

There are two major architectures used in single-chip FIFO; toggle fall-through and zero fall-through.

5.1.2 Toggle Fall-Through Architecture

The toggle fall-through type of FIFO consists of an array of registers. Figure 5-1 illustrates this architecture for an M-word by N-bit FIFO. The output of each register is connected to the input of the following register in a chain-like fashion. Data is input to the first register and is removed from the last register. As each word is input into the FIFO, internal control logic toggles the word through the series of registers to the last one available. As each word is output from the FIFO, all the words are shifted down one register.

EPIC is a trademark of Texas Instruments Incorporated

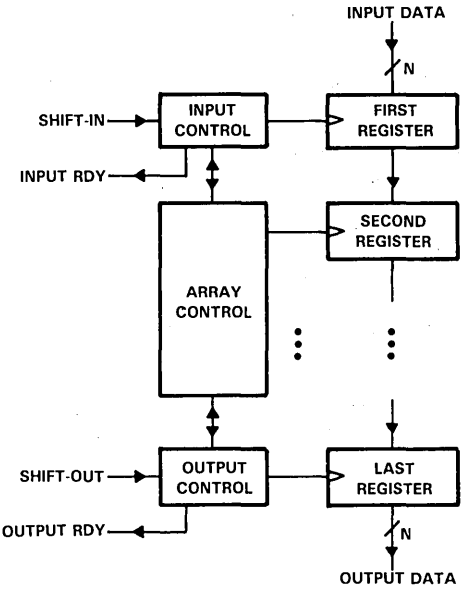


Figure 5-1. Toggle Fall-Through FIFO (M words by N bits)

A toggle fall-through FIFO is described by the number of words in depth, number of bits in width, maximum input and output clocking rates, and fall-through time. The fall-through time is the maximum delay required for a word to travel from the input to the output in an empty FIFO. The complement to this specification is the bubble-through time or the delay it takes for all words to ripple down one register after a word has been read from a full FIFO. However, these two specifications are roughly equivalent so only the greater value is included in the data sheet.

TI offers several toggle fall-through FIFO products. The SN74S225 is a 16 × 5, 10 MHz FIFO. It has 3-state outputs and is cascadable in depth. The SN74ALS234 is a 16 × 4, 30 MHz, cascadable FIFO with 3-state outputs. The SN74ALS235 is a 16 × 5, 25 MHz, cascadable FIFO. It has 3-state outputs and includes half-full and almost full/empty flags. The SN74ALS236 is a bi-state version of the SN74ALS234.

5.1.3 Zero Fall-Through Architecture

The zero fall-through type of FIFO consists of a dual-port RAM with read and write address pointers. Figure 5-2 illustrates this architecture for an M-word by N-bit FIFO. Data is input to the word addressed by the write pointer and data is output from the word addressed by the read pointer. Upon reset, both pointers are cleared to a value of zero. After each word is read or written, the respective pointer is incremented by one. Internal comparison logic is used to generate condition flags such as full and to prevent overrun and under-run (too much writing and too much reading of data).

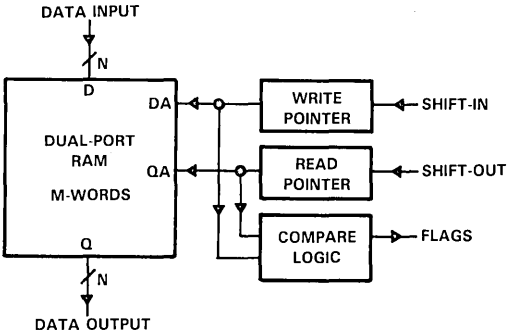


Figure 5-2. Zero Fall-Through FIFO (M words by N bits)

A zero fall-through FIFO is described in terms similar to the toggle products. However, the fall-through time now consists of the delay for incrementing the pointer and comparing the new pointer values. This time is roughly equivalent to the time between shift clocks for the input and the output, or "zero". In many applications zero fall-through FIFOs are preferred to toggle FIFOs for this reason.

TI offers several zero fall-through FIFO products. The SN74LS222 and SN74LS224 are 16 × 4, 10-MHz FIFOs with 3-state outputs. The SN74LS227 and SN74LS228 are open-collector versions of the SN74LS222 and SN74LS224. The SN74ALS229A is a 16 × 5, 30-MHz, 3-state FIFO. It has 4 flags: full, empty, full − 2, and empty + 2. The SN74ALS232A is a 16 × 4, 30-MHz, 3-state FIFO with full and empty flags. The SN74ALS233A is a version of the SN74ALS229A with full − 1 and empty + 1 flags instead of the full − 2 and empty + 2.

The SN74ALS2232 is a 64 × 8, 40-MHz FIFO with 3-state outputs and both full and empty flags. The SN74ALS2233 is a 64 × 9, 40-MHz FIFO with 3-state outputs and four flags: full, empty, almost full/empty, and half full. The SN74ALS22XX is a 64 × 9, 40-MHz, cascadable FIFO with 3-state outputs and both full and empty flags. The TACT7202 is a 1K × 9, 16-MHz cascadable FIFO with full and empty flags. The TACT2202 is a 1K × 8, 16-MHz FIFO with full and empty flags.

5.1.4 Buffering Design Considerations

A FIFO can be used as a buffer between two communication devices. In buffering applications where the delay from input to output is not critical (e.g., CPU to printer) either a toggle or zero fall-through FIFO can be used. In this instance, only the input and output clocking rates and the depth of the FIFO are critical. In buffering applications where the fall-through delay is important (e.g., bus interface) then the zero fall-through architecture should be used.

The rare case for FIFO operation is when the consumer is faster than the producer. A FIFO depth of one word would suffice. The other situation (see Figure 5-3) requires more words.

Figure 5-3. Buffering Application

The following equations can be used, to determine the depth needed. If the data producer writes a frame of (L) words at a rate of (X) MHz and the data consumer reads words at a rate of (Y) MHz, the resulting equations are:

1. L • 1/X + (BUFFER DELAY) = L • 1/Y
2. MAX (BUFFER DELAY) = DEPTH • 1/X
3. MAX (L) • 1/X + DEPTH • 1/X = MAX (L) • 1/Y
4. DEPTH • 1/X = MAX (L) • (1/Y − 1/X)
5. DEPTH = MAX (L) • (X/Y − 1)

For example, with L = 100 words maximum, X = 8 MHz, and Y = 5 MHz, the necessary depth = 60 words. In this case, a 64-word FIFO would suffice.

The reverse of equation 5 gives the maximum length of a frame for a given FIFO depth:

6. $\text{MAX (L)} = \text{DEPTH} \bullet \frac{1}{(X/Y - 1)}$

For example, with depth = 64, X = 1 MHz, and Y = 0.8 MHz, the maximum length of a frame = 256 words.

5.1.5 Synchronization Design Considerations

In synchronizing applications, the data producer and consumer can operate continuously but asynchronously. The maximum throughput of the FIFO depends on both the clock rate at each port (F_{in} and F_{out}) and the fall-through time (T_F). (f_{max}) is derived from the maximum one-word time delay through the FIFO. The equations are:

7. $\text{MAXIMUM DELAY} = \frac{1}{F_{in}} + T_F$
8. $\frac{1}{f_{max}} = \frac{1}{F_{in}} + T_F$
9. $f_{max} = \frac{1}{1/F_{in} + T_F}$

For a toggle fall-through FIFO in these conditions f_{max} is considerably less than F_{in}. For example, if F_{in} = 30 MHz and T_F = 1000 ns, then f_{max} = 967 KHz. For a zero fall-through FIFO, f_{max} approaches F_{in}. For example, if F_{in} = 35 MHz and T_F = 40 ns, then f_{max} = 14.6 MHz. To ensure only a single-clock delay from the input and to output ports, the FIFO must be clocked at a rate less than f_{max}.

The FIFO may be operated at higher rates by working near the half-full condition. The number of words that can be written into an empty FIFO in the fall-through time (or read from a full FIFO) determines the margins from the empty condition for operating the FIFO at its maximum rate (F_{in}). The numbers correspond to:

10. $\text{MARGIN} = \frac{F_{in}}{1/T_F}$

For example, if F_{in} = 30 MHz and T_F = 1000 ns, then the margin = 30 words. For a 64-word FIFO this would mean that the FIFO could be operated at its maximum throughput rate (F_{in}) when it is between 30 words and 64 words full. Figure 5-4 shows the throughput curve for this type FIFO.

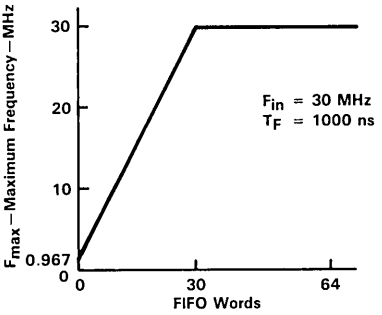


Figure 5-4. Throughput Curve for 64-Word, 30-MHz FIFO

In general, cascading N FIFOs in depth causes equations 9 and 10 to change to:

11. $$f_{max} = \frac{1}{1/(F_{in} + N \bullet T_F)}$$

12. $$MARGIN = \frac{F_{in}}{1/(N \bullet T_F)}$$

5.1.6 Summary

FIFOs are versatile building blocks for the design of data communication products. The need for buffering and/or synchronization of data can be met by selecting the appropriately-sized toggle or zero fall-through FIFO using the methods presented in this report. TI produces many different single-chip FIFO products for a wide range of applications. Contact your local TI representative to obtain individual FIFO data sheets for further information about a particular product.

6 BiCMOS

6.1 BiCMOS Memory Drivers Boost Performance

In current memory management systems, the replacement of discrete logic with single-chip solutions for DRAM control, Error Detection and Correction, and Cache Tag control has greatly improved memory access times. However, in large MOS memory applications the use of external drivers in conjunction with the memory management products can provide added drive to maintain maximum performance. These drivers must meet the requirements of high drive for high capacitive loads, high speed for maximum system throughput, and low power for system power constraints. The designer can now meet these needs with the TI 2000 series Bus Interface devices with improved performance and reliability. The devices offered in new BiCMOS, 'AS, and 'ALS technologies provide designers with the characteristics needed to drive the high capacitive loads in MOS memory and bus-intensive systems while reducing undershoot for reliable system performance.

6.1.1 Reducing Undershoot Problems

In order to maintain maximum system throughput, memory drivers require high-speed operation with very fast switching speeds. As a result, these switching speeds together with the high inductance and capacitance in bus intensive environments can create problems with output signal undershoot and overshoot. This undershoot and overshoot can cause system reliability problems such as false reads at the input to DRAMs. Commonly, these problems with undershoot and overshoot are controlled with an external series resistor, which increases package count and board space. The 2000 series devices provide on-chip 25-Ω series damping resistors on all outputs to reduce undershoot and overshoot without adding to board real estate. Figure 6-1 compares the initial undershoot of the 'AS640 and the 'AS2640 with on-chip series damping resistors. The 'AS2640 can reduce initial undershoot by 58% thus supplying a more reliable input to systems susceptible to undershoot problems.

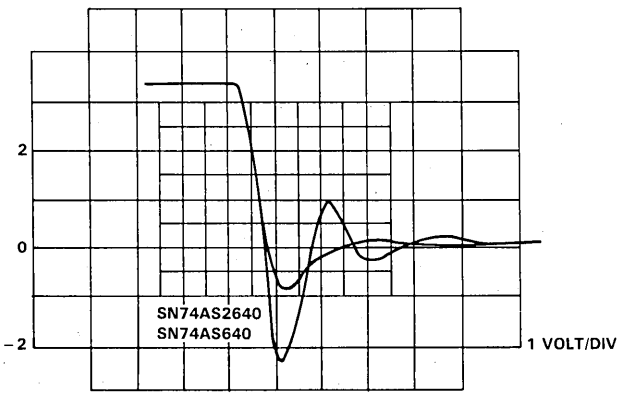


Figure 6-1. Effect of On-Chip Series Output Resistors

6.1.2 BiCMOS Drivers Match MOS Memory Needs

The 2000 series devices offered in the new TI BiCMOS technology provide the advantages of both bipolar and CMOS. BiCMOS combines 2-μM IMPACT^{TM} bipolar with 1.5-μM CMOS to provide the high drive and speeds of bipolar and the low power of CMOS. These interface devices have TTL input and output transistors with CMOS internal circuits. The output transistors supply 48/64 mA of drive current necessary for bus structures such as VME and MULTIBUS II, while the CMOS internal circuits provide low power during disabled or 3-state operation. As with all 2000 series devices, the BiCMOS parts have series damping resistors to reduce undershoot and overshoot.

The BiCMOS drivers can provide the drive and speed necessary in MOS memory applications with a power savings over bipolar devices. Figure 6-2 shows a 4-M word × 32-bit memory configuration consisting of a SN74ALS6301 Dynamic Memory Controller (DMC), a SN74BCT2828 Memory Driver and 4-M words of memory comprised of four banks of TMS4C1024 DRAMs. Each SN74ALS6301 can control up to 4M words of memory. The memory driver provides extra drive to maintain maximum performance in a 32-bit system.

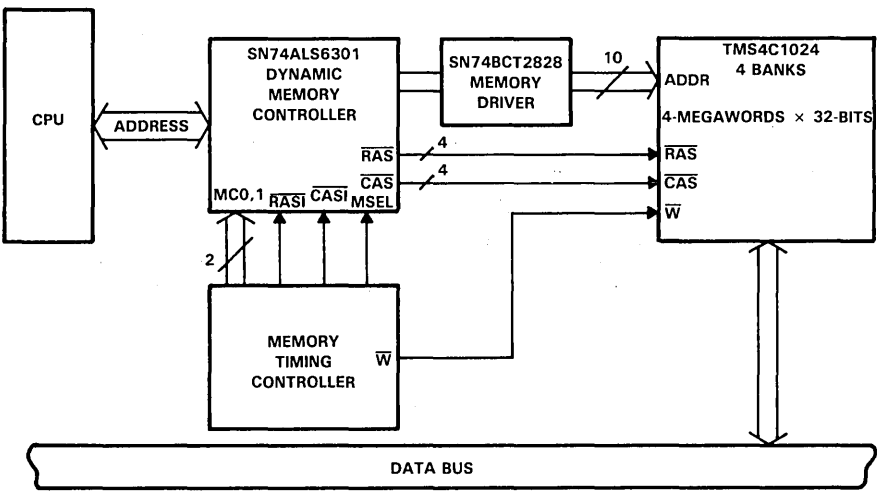


Figure 6-2. 4M Word × 32-Bit Memory System

6.1.3 BiCMOS Lowers Power by 50% or More

When comparing the performance of the SN74BCT2828 to the functionally equivalent AM29828, there is a considerable power reduction. As shown below, there is a 50% reduction in supply current while enabled. However, the real savings comes from the disabled operation. There is more than a 95% supply current reduction while disabled. Since the amount of time a driver is enabled varies with each system, power reduction will vary with the minimum being 50% improvement.

	AM29828	'BCT2828
I_{CC} enabled	80 mA	40 mA
I_{CC} disabled	80 mA	3 mA

In applications that involve multiple drivers the power savings is even more apparent. For example, if a system requires five drivers with only one enabled at any given time, the AM29828 would use almost 8 times more current then the SN74BCT2828.

	AM29828	'BCT2828
I_{CC} enabled	1 × 80 mA	1 × 40 mA
I_{CC} disabled	4 × 80 mA	4 × 3 mA
Total	400 mA	52 mA

Result = 87% power savings

6.1.4 Less Undershoot Means Higher Reliability

The use of the 2000 series BiCMOS drivers also provides the reduced undershoot to prevent false reads at the inputs to the DRAMs without the addition of external resistors. Figure 6-3 shows the improvement of initial undershoot of the SN74BCT2828 compared with the AM29828. The SN74BCT2828 undershoot is 40% less than the AM29828 providing a more reliable signal with the same package count.

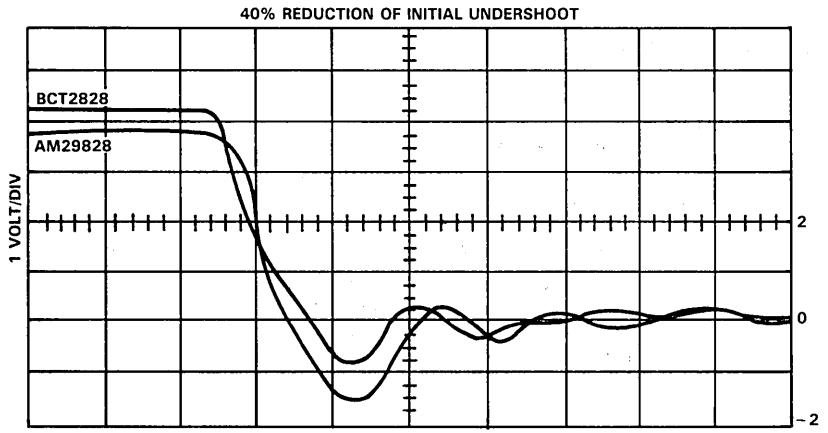


Figure 6-3. Initial Undershoot Comparison of 74BCT2828 vs AM2928

6.1.5 How Do I Get More Information

Each of the 2000 Bus Interface series devices provide the designer with reliable signals without increasing package count and board real estate. The high drive and speed complement Memory Management products for use in large memory and bus applications. The onset of BiCMOS also brings a tremendous power savings which can be appreciated in all designs. Below is a listing of the 2000 series offered. For more information on these Bus Interface and Memory Management products, contact your local Texas Instruments field sales representative or authorized distributor.

Device	Description	Output	I_{OL} (mA)
'BCT2240	Octal Buffer/Driver	Inverting	35
'BCT2241	Octal Buffer/Driver	True	35
'BCT2244	Octal Buffer/Driver	True	35
'BCT2540	Octal Buffer/Driver	Inverting	35
'BCT2541	Octal Buffer/Driver	True	35
'BCT2827	10-bit Buffer/Driver	True	12
'BCT2828	10-bit Buffer/Driver	Inverting	12
'ALS2240	Octal Buffer/Driver	Inverting	15
'ALS2242	Octal Transceiver	Inverting	30
'ALS2244	Octal Buffer/Driver	True	30
'ALS2540	Octal Buffer/Driver	Inverting	30
'ALS2541	Octal Buffer/Driver	True	30
'AS2620	Octal Transceiver	Inverting	35
'AS2623	Octal Transceiver	True	35
'AS2640	Octal Transceiver	Inverting	35
'AS2645	Octal Transceiver	True	35

6.2 BiCMOS Bus Interface

6.2.1 Abstract

Bipolar and CMOS processes have their individual advantages. The advantages of bipolar are speed and output drive current capability. The advantage of CMOS is significantly lower power consumption with continually improving speed performance. The merge of the two processes in order to use their individual advantages for optimal product development was therefore a predictable technology transition.

This portion of this report concerns the use of such a process, BiCMOS, and the advantages provided in bus-interface logic. Ultimately, the system advantage gained from the use of BiCMOS bus interface logic results in a 25% reduction of total system power.

6.2.2 Introduction

Bus-interface logic requires very high output-drive currents of 48/64 mA. These currents are required to drive high-capacitive loads and backplanes and to meet the required specifications of established standards. Advanced speed performance is also a necessity to allow the rapid transfer of information and to complement the performance of other system components.

Excessive power consumption was the tradeoff that system designers were forced to accept to achieve the desired output-drive current and speed performance. In an average system, 30% of the total device supply current is required to support the bus interface logic. The use of BiCMOS bus-interface logic can reduce the required device supply current by more than 90%. This results in an overall system power savings of more than 25%.

6.2.3 Reduction of Supply Current Demand Without Sacrificing Performance

The combination of bipolar and CMOS components makes the power savings a reality without sacrificing required output drive current or speed performance. An examination of bus-interface logic in system operation reveals that the device is either enabled

(active) or disabled. Since in bus configurations only one device is active at any given time, the remaining devices tied to the bus are disabled. Therefore, for the majority of the time, devices tied to the bus are in a disabled mode. Further evaluation reveals that the currently available bipolar devices that are capable of meeting the specifications required for bus-interface logic require supply currents ranging from 75 mA to 160 mA per device depending upon the function.

BiCMOS requires approximately 10 mA maximum (I_{CCZ}) when disabled and further reduces the active supply current demand by approximately 50% compared to equivalent bipolar devices. Table 6-1 is a comparison of the SN74BCT29861 and AM29861 supply currents. Figure 6-4 illustrates typical switching performance and disabled supply current demand between the two devices.

Table 6-1. SN74BCT29861/AM29861 I_{CC} Comparison

	SN74BCT29861		
I_{CC}	Supply current	Enable	30 mA (Max)
	(VCC = 5.5 V @ 70°C)	Disable	7 mA (Max)
	AM29861		
†I_{CC}	Supply current		150 mA (Max)
	(V_{CC} = 5.5 V @ 70°C)		

†Advanced Micro Devices Bipolar Microprocessor Logic and Interface 1985 Data Book. No breakout given for enable or disable I_{CC}.

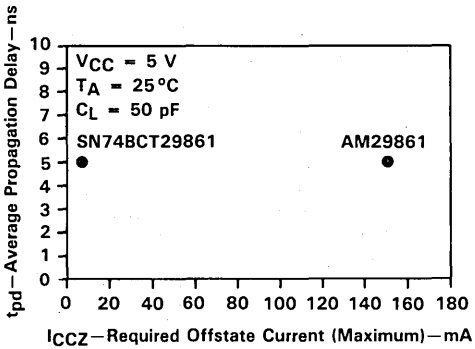


Figure 6-4. SN74BCT29861 and AM29861 Required Off-State Current vs Average Propagation Delay

To highlight the system power savings advantage exhibited by BiCMOS bus-interface products, see the conditions in Figure 6-5. Assuming a bus network contains a fanout of ten bus interface devices, Figure 6-5 illustrates that only one device is enabled, while the other nine are disabled.

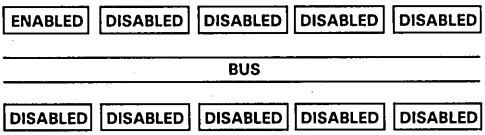


Figure 6-5. Bus Network

Assumption:

		Advanced Bipolar	BiCMOS
ICC	(Enable)	150 mA	30 mA
ICCZ	(Disable)	150 mA	10 mA
		Advanced Bipolar	
ICC	(Enable)	1 x 150 mA = 150 mA	
ICCZ	(Disable)	9 x 150 mA = 1350 mA	
ICC	(Total)	1500 mA	
		BiCMOS	
ICC	(Enable)	1 x 30 mA = 30 mA	
ICCZ	(Disable)	9 x 7 mA = 63 mA	
ICC	(Total)	93 mA	

Result: 94% power savings.

6.2.4 Combinational Bipolar and CMOS Optimal Process Solution

BiCMOS bus-interface logic is a TTL-to-TTL interface product that provides the optimal combination of speed performance, output drive, and low power. To achieve these characteristics, TI combines 2-μm bipolar IMPACT^{TM} (Implanted Advanced Composed Technology) process with 1.5-μm CMOS process is shown in Figure 6-6.

The bipolar process provides output transistors capable of supplying the required 48/64 mA. The transistors also use the smaller TTL voltage swings of -0.5 V- to -3.5 V as compared to their rail-to-rail or GND-to-V_{CC} voltage swings that are associated with CMOS transistors. The smaller voltage swings associated with TTL outputs reduce the overall effect of transient voltage noise on the ground pins. Excessive noise spikes can be detrimental to reliable system performance due to output glitching, loss of stored data, increase of system noise, etc.

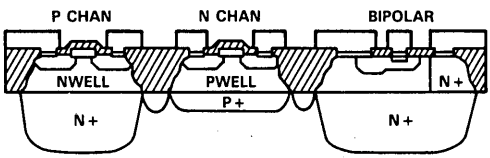


Figure 6-6. BiCMOS Process

The following equation is a simple method of calculating the induced voltage on the ground and V_{CC} pins due to transient currents caused by switching capacitive loads.

$$V_L(t) = -L_P C_L \frac{d^2V_O(t)}{dt^2}$$

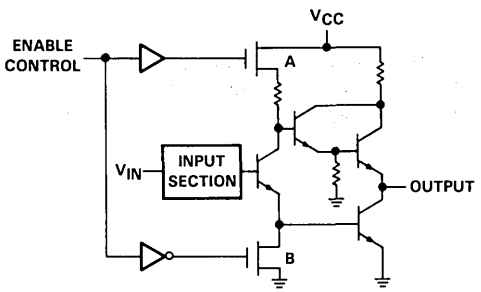
Where:

$V_{L(t)}$ = Voltage transient
L_P = Package inductance
C_L = Load capacitance
$d^2V_O(t)$ = Change in the slope of the transition edge
dt = Transition edge time

Since L_P, C_L, and dt are the same, the amount of voltage level transition swing is the only difference between the bipolar and CMOS transistors. Since CMOS transistors require a wider voltage swing, it becomes apparent that a CMOS output transistor will produce a larger amount of voltage noise that, if excessive, could cause system reliability problems.

The CMOS process provides a disable circuit that consumes considerably less current than a pure bipolar circuit. Figure 6-7 illustrates how the CMOS components combine with the bipolar components to interrupt the flow of supply current during the disable mode or three state. The remaining internal components are also fabricated from CMOS which further reduces the required amount of supply current.

Both the bipolar and CMOS processes provide the capability to adequately meet the advanced speed performance required for bus interface.



- DURING OPERATION: A SHORTED, B OPEN
- DURING THREE-STATE: A OPEN, B SHORTED

Figure 6-7. BiCMOS Three-State Gate Schematic

6.2.5 Variety of Functional Options in Two-Package Configurations

Additional design support for bus-interface logic is the availability of popular functions in multiple variation such as true or inverting outputs and synchronous or asynchronous operation. BiCMOS will be offered with two pinout options; 1) The traditional pinout for pin-to-pin compatibility with existing bipolar devices. 2) Flow through architecture with center power pins to further reduce the voltage noise associated with multiple output switching.

As indicated by the $V_{L(t)}$ equation, the amount of switching noise can be reduced through a decrease in the package inductance.

The functional options that will be available in BiCMOS are as follows:

FUNCTION	DESCRIPTION
'240 Series	Octal Buffers/Drivers
'245 Series	Octal Transceivers
'373 Series	Octal Latches
'543 Series	Octal Registered Transceivers
'646 Series	Octal Registered Transceivers
'2000 Series	Memory Drivers
'29818/819	Pipeline Registers
'29820 Series	8-10 Bit Buffers and Registers
'29830 Series	Bidirectional Parity Transceivers
'29840 Series	8-10 Bit Latches and D-Latches
'29850 Series	Bidirectional Parity Transceivers with Latches
'29860 Series	9-10 Bit Transceivers

6.2.6 Summary

BiCMOS bus-interface logic is a TTL-to-TTL product that provides a 95% reduction in standby current demand. This results in a 25% total system power savings without sacrificing high output drive or speed performance.

System Solutions for Static Column Decode

Robert K. Breuninger, Loren Schiele,
and Joshua K. Peprah

TEXAS INSTRUMENTS

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Appendixes

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List of Illustrations

INTRODUCTION

The new 32-bit microprocessors are capable of addressing 4G bytes of physical memory and typically feature clock frequencies greater than 16 Mhz. However, clock speed alone does not guarantee increased system performance; if the processor must wait for data, then memory bandwidth will be the limiting factor.

This situation exists between today's microprocessors and the access times of affordable DRAMs. One solution to optimizing system performance is to mix and match memory, using lower cost dynamic RAM in conjunction with fast, more expensive static RAM caches. However, this approach is only attractive to high end systems where cost and board space is a less significant factor.

Another approach to improving system performance is to utilize the new accessing modes available on certain 1 meg DRAMs, such as static column decode. This method does not improve system performance as much as caches, but it does involve less hardware, resulting in lower system cost. This approach can also be used in systems already using caches, further improving system performance.

This application note describes the theory of using static column decode and also describes how it might be implemented in a typical system. In addition, it highlights three new products from Texas Instruments. The SN74ALS6300 "Selectable Refresh Timer", the SN74ALS6310 "Static Column Access Detector", and the TIBPSG507 "Programmable Sequence Generator".

STATIC COLUMN DECODE

The TMS4C1027 is a 1,048,576-bit × 1 dynamic RAM featuring static column decode. Static column decode allows high-speed read and write operations by reducing the number of required signal setup, hold, and transition timings. This is achieved by first strobing the row and column addresses in the normal manner by taking $\overline{RAS}$ and $\overline{CAS}$ low. If $\overline{RAS}$ and $\overline{CAS}$ are kept low, new data can be accessed by simply changing the column addresses, assuming the new address is in the same row. If the new address is not in the same row, then a normal access cycle must be performed.

Figure 1 is a timing diagram taken from the TMS4C1027 datasheet showing static column decode mode read cycle timing.

If the assumption is made that the majority of memory references tend to be sequential, which is a similar assumption made when using caches, then it is logical to assume that a large percentage of memory accesses will be within the same row. The trick is how to implement a timing controller which will take full advantage of the static column mode of operation.

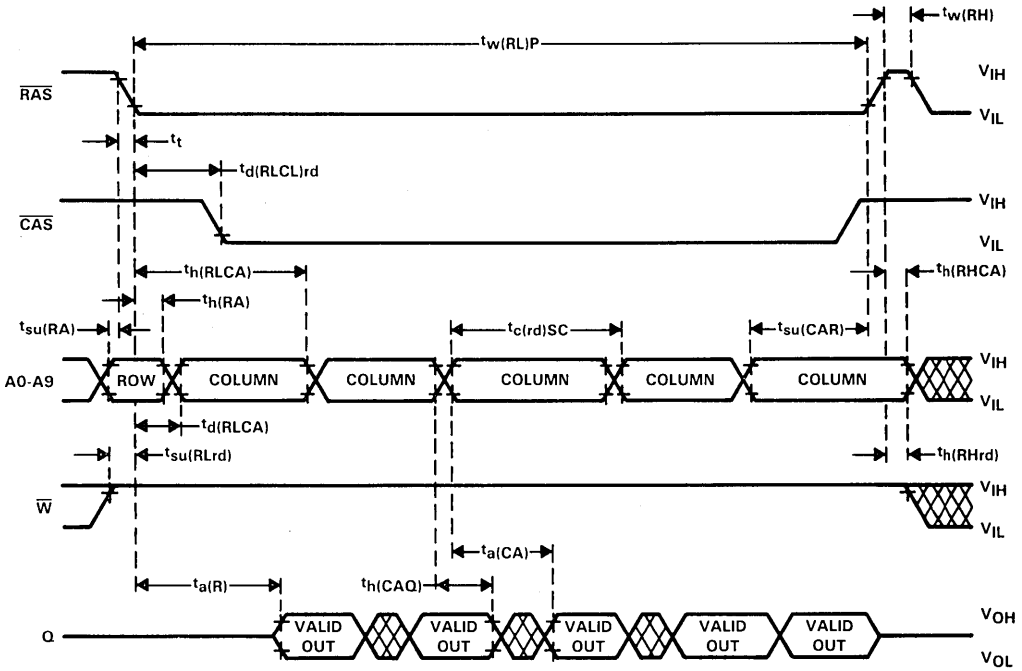


Figure 1. Static Column Decode Mode Read Cycle Timing

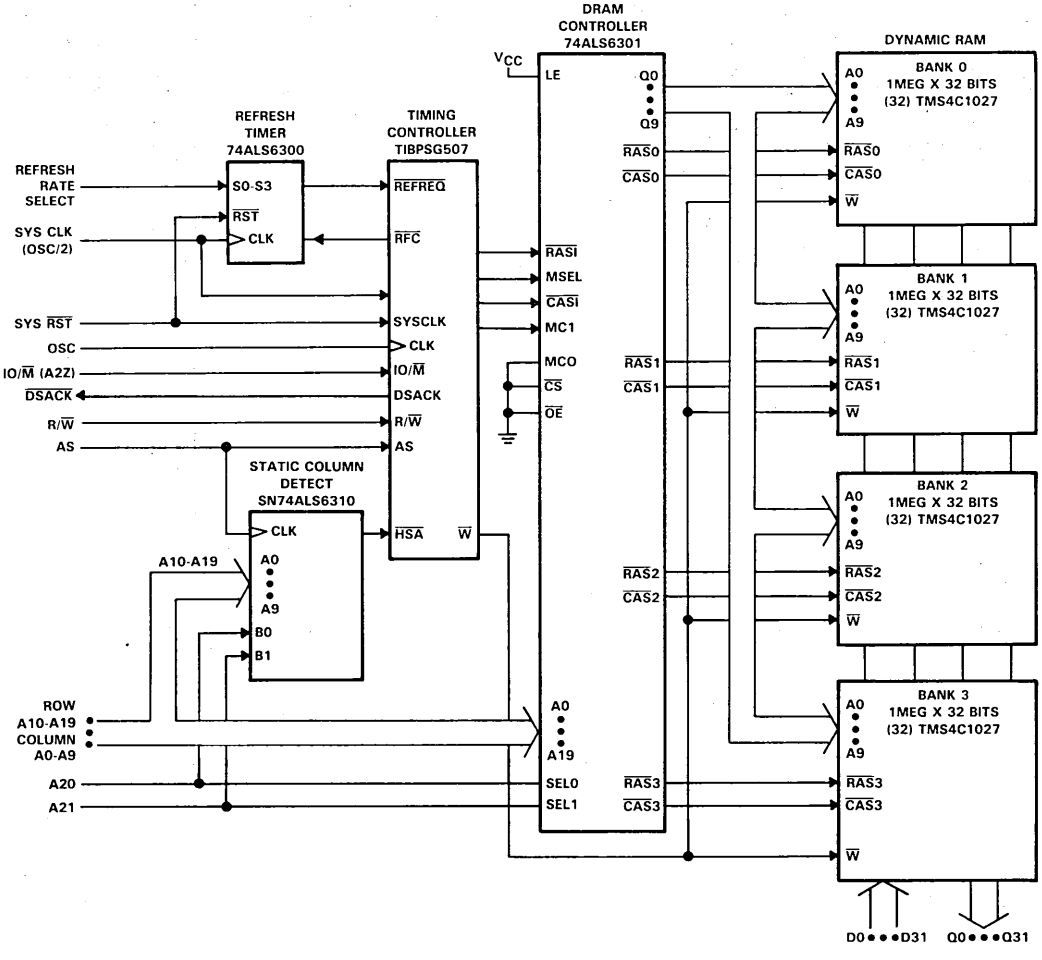


Figure 2. 68020 Static Column Memory Controller

TYPICAL MEMORY CONTROLLER

Figure 2 shows a block diagram of a memory system utilizing static column decode. The ALS6310 is a new circuit offered by Texas Instruments which detects if the present row being accessed is the same as last row accessed. This is the fundamental requirement for implementing static column decode. Note that the row addresses from the 68020 are used as the most significant bits (A10-A19) and the column addresses are used as the least significant bits (A0-A9). Figure 3 shows a block diagram of the ALS6310.

In circuit operation, when address strobe (AS) from the 68020 is taken low, the present row (A10-A19) and bank address (B0, B1) is clocked into the first register of the ALS6310. The previous bank and row address, stored in the first register, is clocked into the second register at the same time. The two addresses are then compared to see if they are equal. If they are equal, the high speed access output ($\overline{HSA}$) will be logically low. If not, $\overline{HSA}$ will be high.

The function of the PSG507 is to generate the required memory timing control signals ($\overline{RAS}$, $\overline{CAS}$, etc.) for the ALS6301 dynamic memory controller. The ALS6301 is responsible for multiplexing row and column addresses into DRAM. The ALS6301 is also capable of driving 4 banks of 1M-byte memory.

Supporting the PSG507 is the ALS6300 refresh timer. This device is responsible for generating a refresh request signal ($\overline{REFREQ}$) every 15.5 μs. The input select lines are hardwired to match the microprocessor clock frequency. The refresh complete input ($\overline{RFC}$), resets the $\overline{REFREQ}$ signal after the timing controller completes the refresh cycle.

TIMING CONTROLLER DETAILS

Figure 4 shows a typical flow chart for implementing static column decode. As stated before, the PSG507 is responsible for implementing the flow chart shown in Figure 4. A breakdown of this flow chart reveals 9 states (ST0-ST8), associated with 5 different sequences. States ST0, ST1, ST3, and ST4 are holding and transition states, leading into the various sequences. The five possible sequences are listed below.

ST2 Normal Access Sequence
ST5 Extended Access Sequence
ST6 High-Speed Access Sequence
ST7 Normal Refresh Sequence
ST8 Extended Refresh Sequence

Notice that the $\overline{HSA}$ signal from the ALS6310 decides if the timing controller will execute ST5, the Extended Access Sequence, or ST6, the High-Speed Access Sequence. A brief description of each sequence follows.

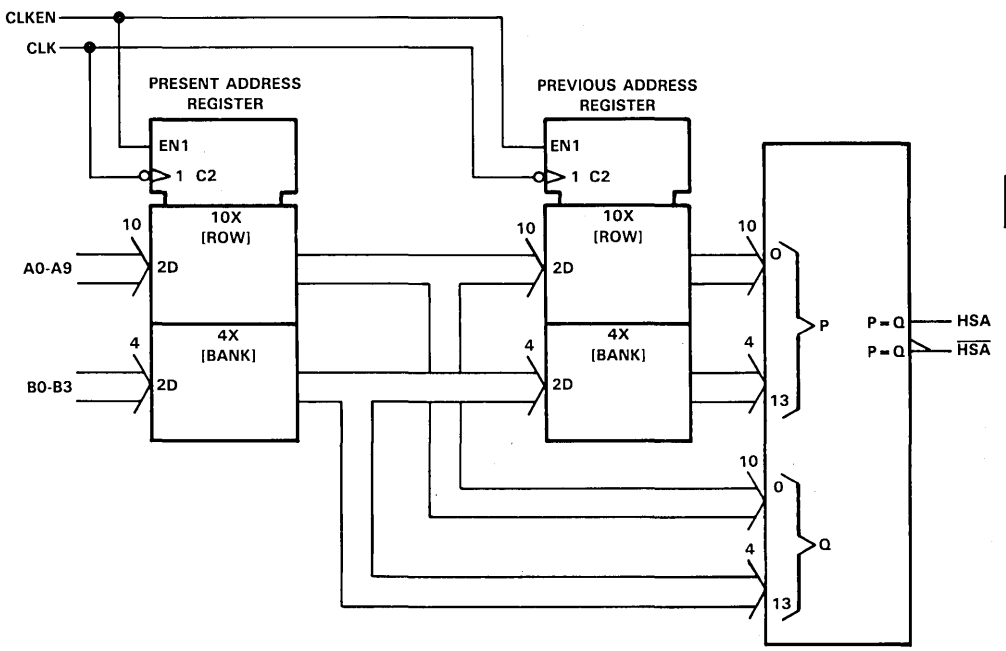


Figure 3. ALS6310 Static Column Page Mode Access Detector

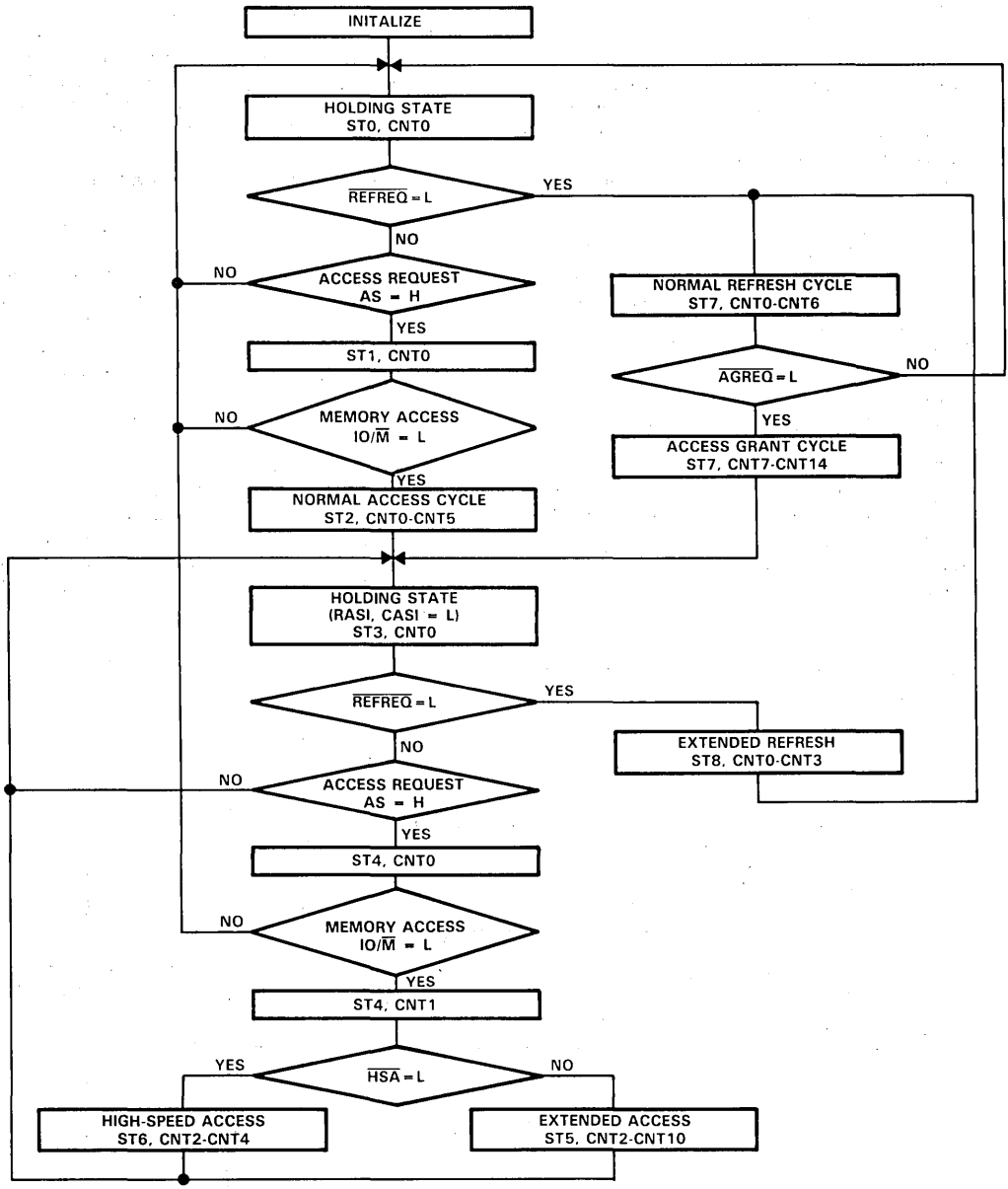


Figure 4. Timing Controller Flowchart

NORMAL ACCESS SEQUENCE

The normal access sequence is shown in Figure 5. This sequence begins by executing a normal $\overline{RAS}/\overline{CAS}$ cycle. Notice that a wait state of one clock cycle is needed to guarantee that data is valid for the 68020. This is the problem mentioned in the introduction; if all access cycles had to be performed in this manner, then the processor would face a wait state every access cycle. As will be shown later, this wait state can be eliminated if the next address is from the same row.

Notice also, at the end of this sequence, the $\overline{RAS}$ and $\overline{CAS}$ output signals are left active low. Here we are making the assumption that the next access cycle will be a high-speed access. We will not know if this assumption is true until the next address is presented by the 68020. At that time, the ALS6310 will signal the timing controller if it can execute a high-speed access.

HIGH-SPEED ACCESS SEQUENCE

For a high-speed access sequence to be executed, two conditions must be met. The $\overline{RAS}$ and $\overline{CAS}$ inputs must already be low, and secondly, the static column access detector must be indicating the present row is the same as the last row ($\overline{HSA}$ = L). The bank addresses must also be unchanged as detected by the ALS6310.

Figure 6 shows the timing diagram for the high-speed access sequence. Notice that no wait states are required. If the assumption is made that the majority of memory references are sequential, then this sequence will be the one typically used. In other words, this sequence is similar to accessing data from a static RAM, or just like taking data from cache.

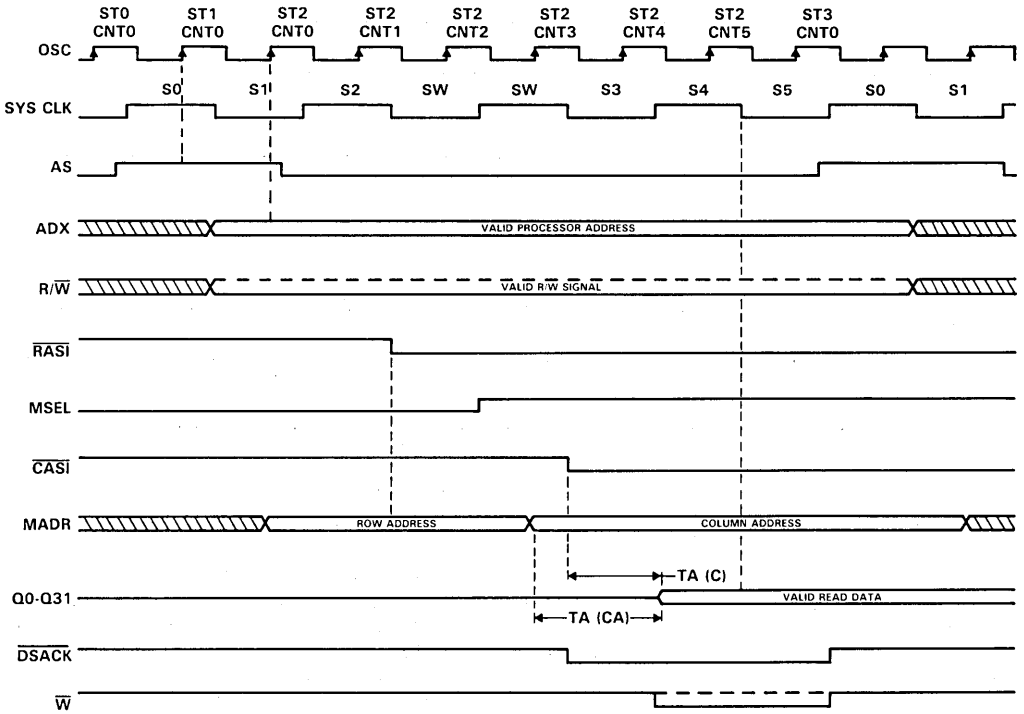


Figure 5. Normal Access Cycle

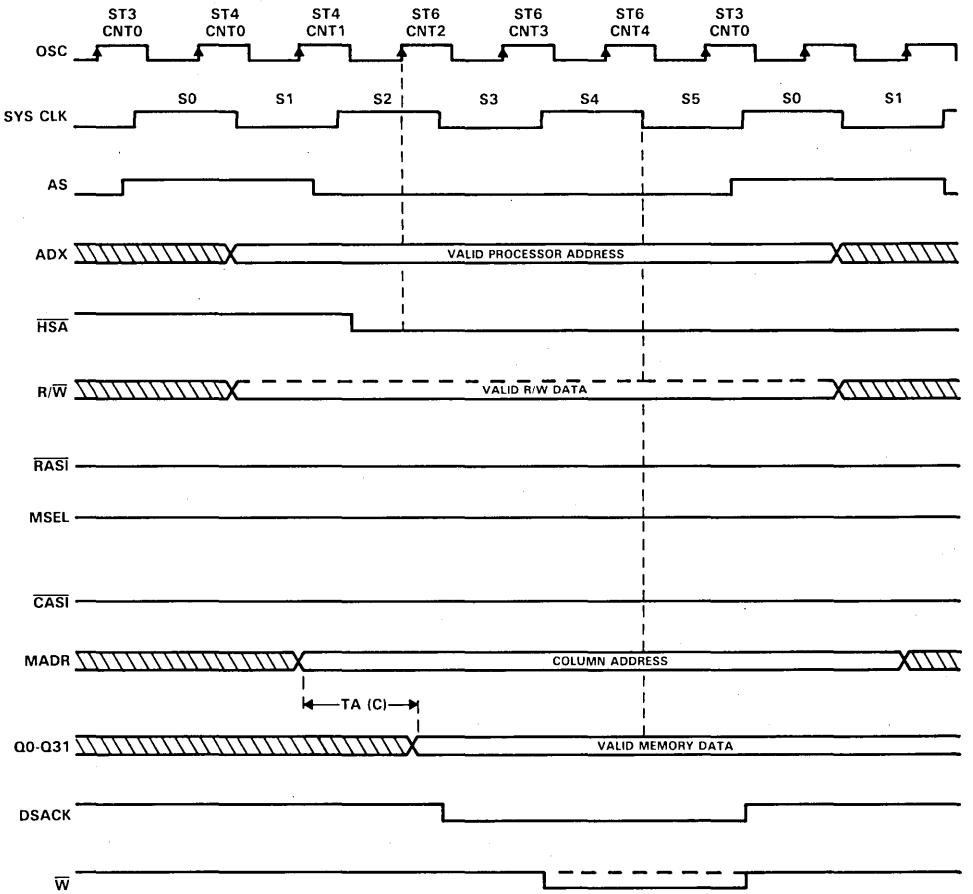


Figure 6. High-Speed Access Cycle

EXTENDED ACCESS SEQUENCE

The extended access sequence is executed if the ALS6310 detects a difference between the present, and last row addresses.. This cycle is called extended because $\overline{RAS}$ and $\overline{CAS}$ are presently low and both must be brought high to strobe in the new row and column addresses. The precharge time of the DRAM has to be met before taking $\overline{RAS}$ and $\overline{CAS}$ low. From the timing diagram in Figure 7, it can be seen that wait states of three clock cycles are generated when executing this timing sequence.

In systems where sequential data is not the general rule, it would be more efficient to execute only normal access sequences, since this generates fewer wait states. The system designer must understand what type of memory accesses will be used. For example, the designer may want only to enter the high-speed access portion of the flow chart when the system is performing DMA access cycles.

NORMAL/EXTENDED REFRESH SEQUENCES

Figures 8 and 9 show the timing diagrams for the normal and extended refresh sequences. The refresh sequence selected is a function of the present condition of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ and $\overline{CAS}$ are presently low, an extended refresh cycle is performed. If $\overline{RAS}$ and $\overline{CAS}$ are presently high, a normal refresh cycle is executed. At the end of each refresh sequence, the controller checks to see if an access request has been generated. If there has been an access request, the controller will perform an access grant sequence at the end of the refresh cycle before returning to normal process flow.

Referring back to Figure 1, there is a maximum time that $\overline{RAS}$ and $\overline{CAS}$ can be held low, $t_W(RL)P$. For the TMS4C1027, $t_W(RL)P$ must not exceed 100 μs. Since our refresh timer forces a refresh cycle every 15.5 μs, $t_W(RL)P$ cannot be violated. If the designer chooses to use a different refresh scheme, then $t_W(RL)P$ must be considered.

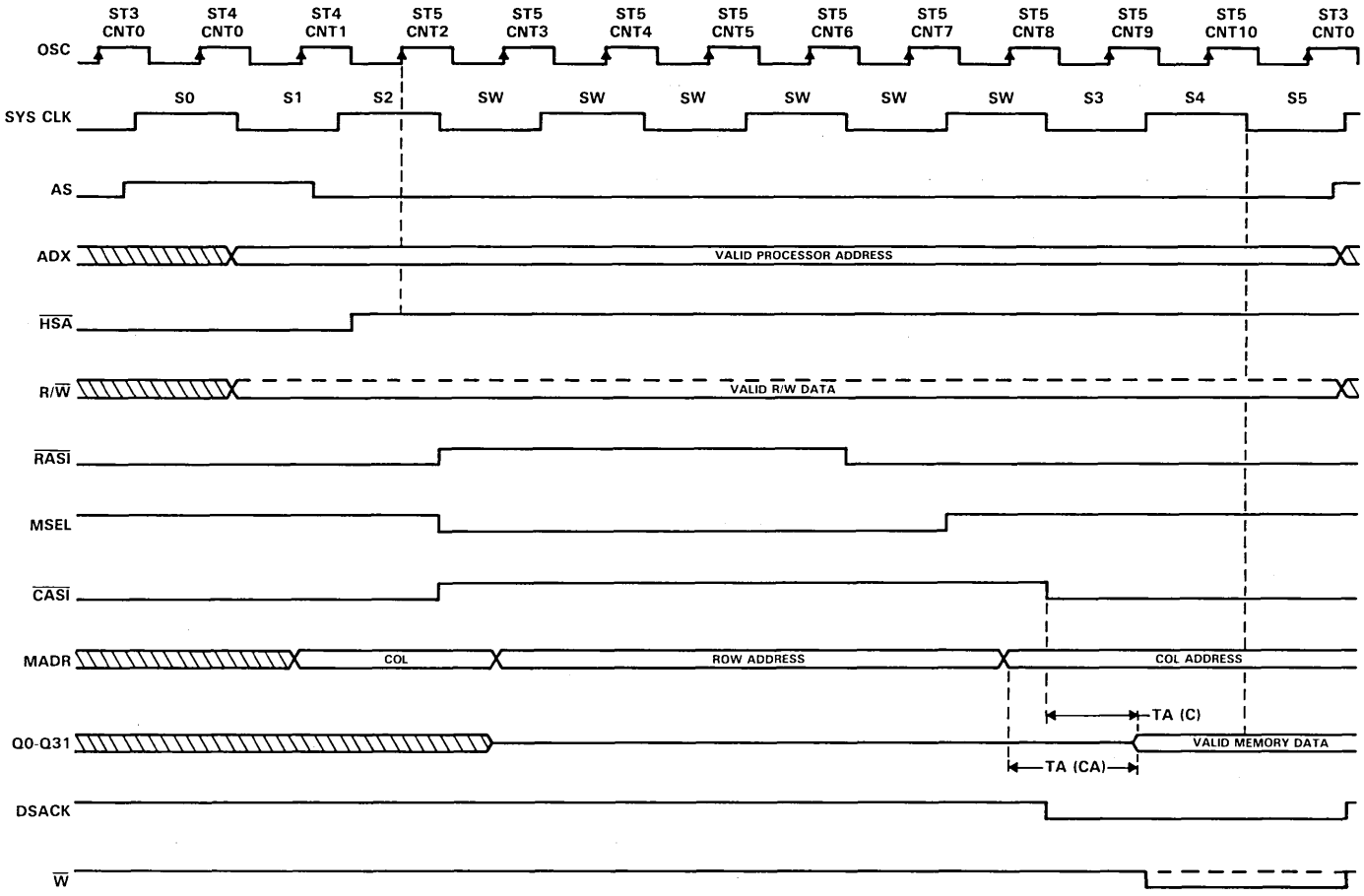


Figure 7. Extended Access Cycle

6 Applications Information

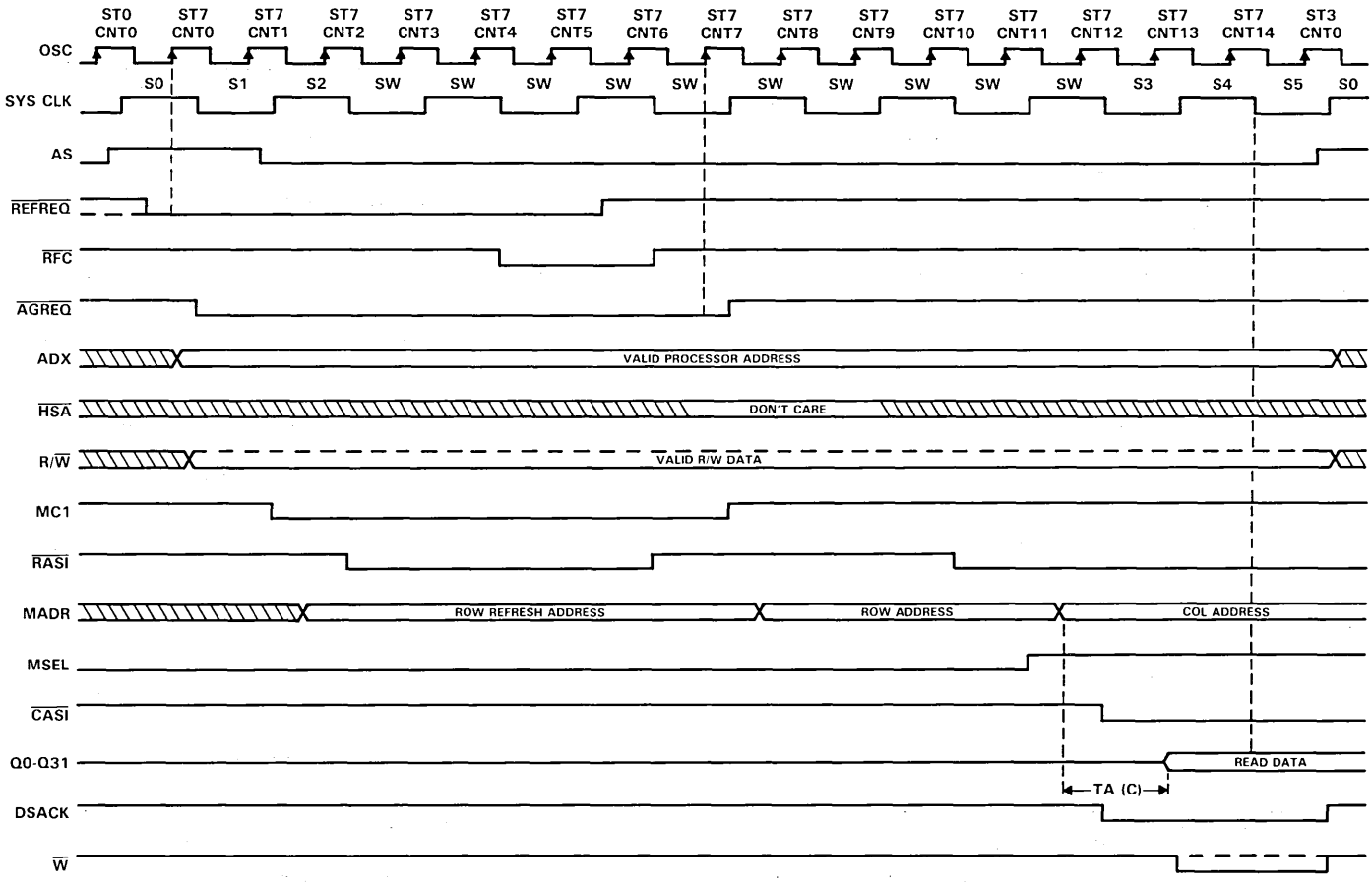


Figure 8. Normal Refresh/Access Grant Cycle

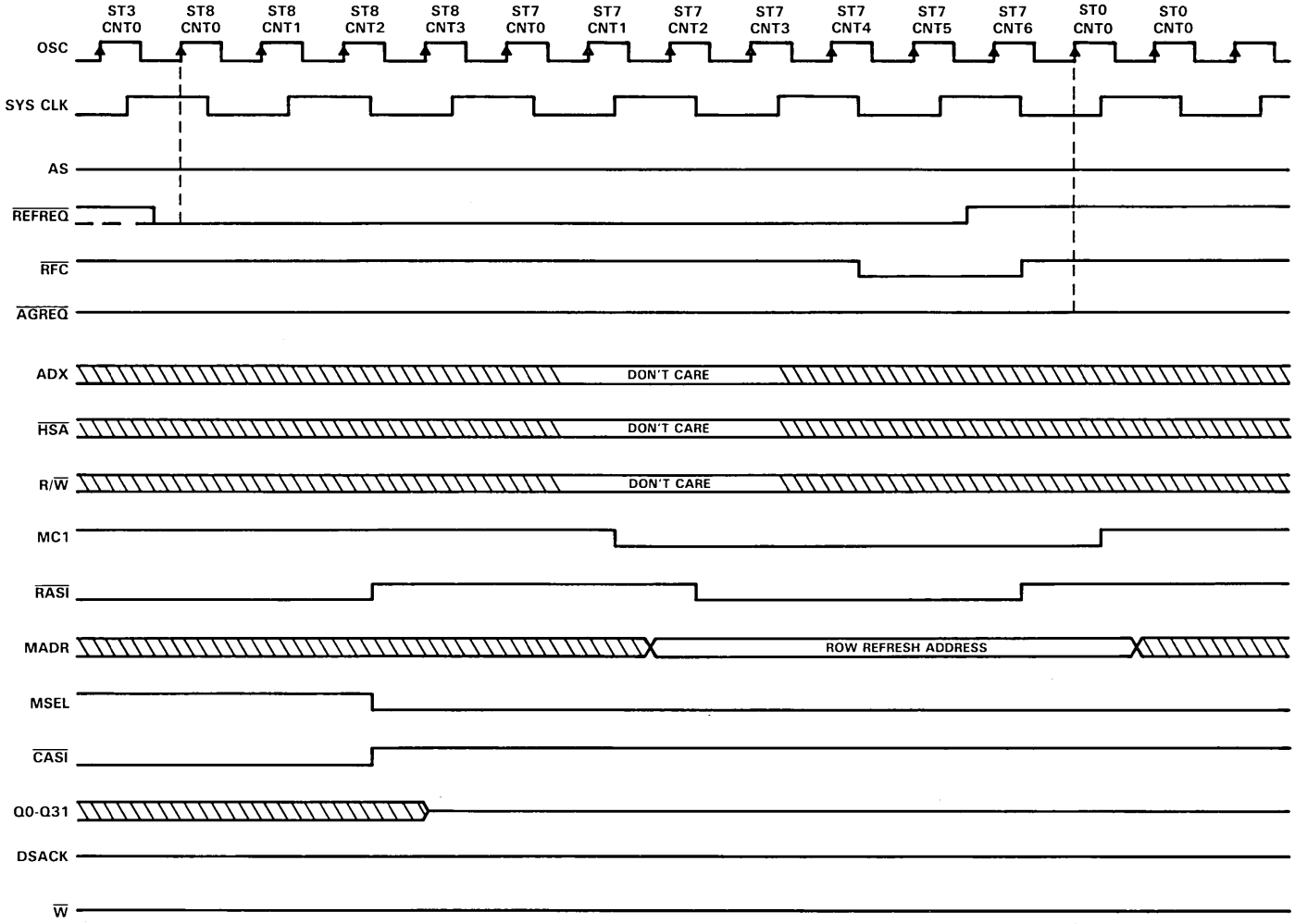


Figure 9. Extended Refresh Cycle

SOFTWARE SUPPORT

The PSG507 is supported by two software packages. CUPL which was created by and is supported by Assisted Technologies, a division of Personal CAD Systems Inc. and ABEL which was created by and is supported by FutureNet a division of Data I/O Corp. Both of these software packages have been used to reduce equations and to generate the fusemap necessary to program the PSG507. Appendices A and B show the ABEL™ and CUPL™ source files for the described static column memory timing controller are attached to assist the designer in programming the PSG507.

Since only 54% (43 out of 80) of the PG507's product terms were used in this design, it will be easy to modify or add to the sequences used to meet specific system requirements. For detailed information on designing with the PSG507 see "A Designer's Guide to the PSG507" application report.

SUMMARY

Static column decode offers the system designer a method for improving system performance in applications where the microprocessor can outperform conventional DRAM access times. By utilizing the ALS6310 "Static Column Access Detector", the ALS6300 "Refresh Timer", and the TIBPSG507 "Programmable Sequence Generator" a high performance memory timing controller can be easily developed to take full advantage of static column decode.

APPENDIX A

```
module SCDECODE
title  'ABEL EXAMPLE FOR THE STATIC COLUMN DECODER
                JOSH PEPRAH, TEXAS INSTRUMENTS, OCT 29, 1987'

      DECODE device 'F507';

" Input pin assignments
OSC           pin   1;                        " OSCILLATOR
RESET         pin   2;                        " SYSTEM RESET - WHEN LOW
A22           pin   3;                        " IO/MEMORY - MEMORY ACCESS
RW            pin   4;                        " READ / WRITE ENABLE
REFREQ        pin   5;                        " REFRESH REQUEST
AS            pin   6;                        " ADDR STROBE - ACCESS REQ
HSA           pin   7;                        " HIGH SPEED ACCESS
SYSCLK        pin  17;                        " SYSTEM CLOCK - (OSC/2)

" Output pin and node assignments
RFC           pin   8;  RFC_r    node 47;   " REFRESH COMPLETE
RASI          pin   9;  RASI_r   node 48;   " ROW ADDRESS STROBE
MSEL          pin  10;  MSEL_r   node 49;   " MULTIPLEXER SELECT
CASI          pin  11;  CASI_r   node 50;   " COLUMN ADDRESS STROBE
MC1           pin  13;  MC1_r    node 51;   " MODE CONTROL
W             pin  14;  W_r                 node 52;   " WRITE
DSACK         pin  15;  DSACK_r  node 53;   " DATA STROBE ACKNOWLEDGE


" Internal counter bits & control, and state reg - node declarations
C0,C1,C2,C3,C4,C5  node 55,56,57,58,59,60;
SCLR0         node 25;
CNTHOLD0 node 28;
CNTHOLD1 node 29;  CNTHOLD1_r node 30; " COUNT/HOLD CONTROL REGISTER

" Buried state registers - node declarations

P0     node 31;  P0_r      node 39;       " STATE REGISTER
P1     node 32;  P1_r      node 40;       " STATE REGISTER
P2     node 33;  P2_r      node 41;       " STATE REGISTER
P3     node 34;  P3_r      node 42;       " STATE REGISTER
AGREQ  node 35; AGREQ_r node 43;       " ACCESS GRANT REQUEST STATUS REGISTER

" Set notation is used to represent control, buried state, and output
" registers. This is done to simplify the equations.  The following
" sets are in the form;  register name_ = [set input, reset input]. Note
" that the ouput register pin name specifies the set input.

RFC_          = [RFC, RFC_r];
RASI_         = [RASI, RASI_r];
MSEL_         = [MSEL, MSEL_r];
CASI_         = [CASI, CASI_r];
MC1_          = [MC1, MC1_r];
W_            = [W, W_r];
DSACK_        = [DSACK, DSACK_r];
AGREQ_        = [AGREQ, AGREQ_r];
```

```
" Intermediate declarations for simplification.
" The sets 'high' and 'low' are used to set or reset the S/R
" registers.  Example: RASI_ := high & RESET; will cause pin 9
" to go high on the next clock edge if input pin 6 is high.

high            = [ 1,  0];
low             = [ 0,  1];
COUNT           = [C3,C2,C1,C0];
STATE_          = [P3,P2,P1,P0];              " STATE REGISTER SET DEFINED
H,L,clk,X   = 1, 0, .C., .X.;

equations

enable RFC  = 1;  "outputs always enabled, pin 17 is only an input

" Initialization when RESET is low
    [RASI,CASI,RFC,W,AGREQ,DSACK,MC1,SCLR0] := !RESET;
    [MSEL_r,P0_r,P1_r,P2_r,P3_r]            := !RESET;

" Counter controls defined

SCLR0           =  !RESET
                  # (STATE_==2) & (COUNT==5)
                  # (STATE_==4) & (COUNT==0) & A22
                  # (STATE_==5) & (COUNT==10)
                  # (STATE_==6) & (COUNT==4)
                  # (STATE_==7) & (COUNT==6) & (A22 # AGREQ)
                  # (STATE_==7) & (COUNT==14)
                  # (STATE_==8) & (COUNT==3);

CNTHOLD1   :=  !RESET
                  # (STATE_==2) & (COUNT==5)
                  # (STATE_==4) & (COUNT==0) & A22
                  # (STATE_==5) & (COUNT==10)
                  # (STATE_==6) & (COUNT==4)
                  # (STATE_==7) & (COUNT==6) & (A22 # AGREQ)
                  # (STATE_==7) & (COUNT==14)
                  # (STATE_==8) & (COUNT==3);

CNTHOLD1_r := (STATE_==0) & !REFREQ & RESET
                  # (STATE_==1) & !A22 & RESET
                  # (STATE_==3) & !REFREQ & RESET
                  # (STATE_==3) &  REFREQ &  AS & SYSCLK & RESET;

" Execution of access and refresh sequences
state_diagram STATE_
   State 0:                                                    " NEXT
                                 case                          " STATE
                                  !RESET                              : 0;
                                   REFREQ & (!AS  # !SYSCLK)    : 0;
                                   REFREQ &  AS & SYSCLK & RESET: 1;
                                  !REFREQ &  RESET                    : 7;
                                 endcase;
```

```
" NORMAL ACCESS CYCLE

   State 1:                                                    " NEXT
                                                               " STATE
                        case
                          (COUNT==0) & !A22                  : 2;
                          (COUNT==0) &  A22                  : 0;
                        endcase;

   State 2:
                        RASI_  := (COUNT==0)  & low  & RESET;
                        MSEL_  := (COUNT==1)  & high;
                        CASI_  := (COUNT==2)  & low  & RESET;
                       DSACK_  := (COUNT==2)  & low  & RESET;
                          W_   := (COUNT==3)  & low  & RESET;
                          W_   := (COUNT==5)  & high;
                       DSACK_  := (COUNT==5)  & high;
                      if (COUNT==5) then 3 else 2;

"HOLDING STATE
   State 3:                                                    " NEXT
                                                               " STATE
                        case
                      (!AS # !SYSCLK) & REFREQ & RESET      : 3;
                       REFREQ &  AS & SYSCLK & RESET        : 4;
                       !REFREQ & RESET                                : 8;
                       endcase;

   State 4:
                       CASI_  := (COUNT==0)  &  high &  A22;
                       RASI_  := (COUNT==0)  &  high &  A22;
                       MSEL_  := (COUNT==0)  &  low  &  A22;
                       RASI_  := (COUNT==1)  &  high &  HSA;
                       DSACK_ := (COUNT==1)  &  low  & !HSA;
                       MSEL_  := (COUNT==1)  &  low  &  HSA;
                       CASI_  := (COUNT==1)  &  high &  HSA;

                                                                        " NEXT
                        case                                            " STATE
                          (COUNT==0) &  A22  & RESET          : 0;
                          (COUNT==0) & !A22  & RESET          : 4;
                          (COUNT==1) &  HSA  & RESET          : 5;
                          (COUNT==1) & !HSA  & RESET          : 6;
                        endcase;

"EXTENDED ACCESS CYCLE
   State 5:
                        RASI_  := (COUNT==5)  & low & RESET;
                        MSEL_  := (COUNT==6)  & high & RESET;
                        CASI_  := (COUNT==7)  & low & RESET;
                       DSACK_  := (COUNT==7)  & low & RESET;
                                W_  := (COUNT==8)  & low & RESET;
                                W_  := (COUNT==10) & high;
                       DSACK_  := (COUNT==10) & high;
                          if (COUNT==10) & RESET then 3 else 5;
```

```
"HIGH SPEED ACCESS
   State 6:
                                    W_ := (COUNT==2)  & low & RESET;
                                    W_ := (COUNT==4)  & high;
                                DSACK_ := (COUNT==4)  & high;
                                   if (COUNT==4) then 3 else 6;

"NORMAL REFRESH CYCLE
   State 7:
                                AGREQ_ := AS           & low  & RESET;
                                 MC1_ := (COUNT==0)  & low  & RESET;
                                RASI_ := (COUNT==1)  & low  & RESET;
                                 RFC_ := (COUNT==3)  & low  & RESET;
                                 RFC_ := (COUNT==5)  & high;
                                RASI_ := (COUNT==5)  & high;
                                 MC1_ := (COUNT==6)  & high;
                                RASI_ := (COUNT==9)  & low  & RESET;
                                MSEL_ := (COUNT==10) & high & RESET;
                                CASI_ := (COUNT==11) & low  & RESET;
                               DSACK_ := (COUNT==11) & low  & RESET;
                                    W_ := (COUNT==12) & low  & RESET;
                                    W_ := (COUNT==14) & high;
                               DSACK_ := (COUNT==14) & high;
                               if (COUNT==6) & (A22 # AGREQ) then 0 else 7;
                               if (COUNT==14) then 3 else 7;

"EXTENDED REFRESH CYCLE
   State 8:
                                RASI_ := (COUNT==1)  & high;
                                MSEL_ := (COUNT==1)  & low ;
                                CASI_ := (COUNT==1)  & high;
                                if (COUNT==3) then 7 else 8;


test_vectors  'NORMAL ACCESS CYCLE'

([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,      L , X , X,  X            , X, X ,   X  ,  X  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0      ];
 [clk,      H , X , X,  H            , L, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0      ];
 [clk,      H , X , X,  H            , H, X ,   H  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  1      ];
 [clk,      H , L , X,  X            , X, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  2      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  0  ] -> [ H ,  L ,  L ,  H , H ,H,  H  ,  2      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  1  ] -> [ H ,  L ,  H ,  H , H ,H,  H  ,  2      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  2  ] -> [ H ,  L ,  H ,  L , H ,H,  L  ,  2      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  3  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  2      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  4  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  2      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  5  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3      ];

test_vectors  'HOLDING STATE 4 WITH EXTENDED ACCESS REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,      H , H , X,  H            , H, X ,   H  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4      ];
 [clk,      H , L , X,  X            , X, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4      ];
 [clk,      H , X , X,  X            , X, H ,   X  ,  1  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5      ];
```

```
test_vectors  'EXTENDED ACCESS'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H , X , X,  X              , X, X ,   X  ,  2  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  3  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  4  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  5  ] -> [ H ,  L ,  L ,  H , H ,H,  H  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  6  ] -> [ H ,  L ,  H ,  H , H ,H,  H  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  7  ] -> [ H ,  L ,  H ,  L , H ,H,  L  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  8  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  9  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  , 10  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3       ];

test_vectors  'HOLDING STATE 4 WITH HIGH SPEED ACCESS REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H , H , X,  H              , H, X ,   H  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4       ];
 [clk,       H , L , X,  X              , X, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4       ];
 [clk,       H , L , X,  X              , X, L ,   X  ,  1  ] -> [ H ,  L ,  H ,  L , H ,H,  L  ,  6       ];

test_vectors  'HIGH SPEED ACCESS'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H , X , X,  X              , X, X ,   X  ,  2  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  6       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  3  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  6       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  4  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3       ];

test_vectors  'NON-MEMORY ACCESS FOLLOWED BY REFRESH REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H , H , X,  H              , H, X ,   H  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4       ];
 [clk,       H , H , X,  X              , X, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0       ];
 [clk,       H , X , X,  H              , L, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0       ];
 [clk,       H , X , X,  H              , X, X ,   L  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0       ];
 [clk,       H , X , X,  L              , X, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  7       ];

test_vectors  'NORMAL REFRESH CYCLE'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H , X , X,  X              , L, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , L ,H,  H  ,  7       ];
 [clk,       H , X , X,  X              , L, X ,   X  ,  1  ] -> [ H ,  L ,  L ,  H , L ,H,  H  ,  7       ];
 [clk,       H , X , X,  X              , L, X ,   X  ,  2  ] -> [ H ,  L ,  L ,  H , L ,H,  H  ,  7       ];
 [clk,       H , X , X,  X              , L, X ,   X  ,  3  ] -> [ L ,  L ,  L ,  H , L ,H,  H  ,  7       ];
 [clk,       H , X , X,  X              , L, X ,   X  ,  4  ] -> [ L ,  L ,  L ,  H , L ,H,  H  ,  7       ];
 [clk,       H , X , X,  H              , L, X ,   X  ,  5  ] -> [ H ,  H ,  L ,  H , L ,H,  H  ,  7       ];
 [clk,       H , X , X,  X              , L, X ,   X  ,  6  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0       ];
```

```
test_vectors  'NORMAL REFRESH CYCLE FOLLOWED BY ACCESS GRANT REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
[clk,  H , X , X,  L      , X, X ,   X ,  0  ] -> [ H ,          H ,  L ,  H , H ,H,  H     ,  7  ];
[clk,  H , X , X,  X      , L, X ,   X ,  0  ] -> [ H ,          H ,  L ,  H , L ,H,  H     ,  7  ];
[clk,  H , X , X,  X      , L, X ,   X ,  1  ] -> [ H ,          L ,  L ,  H , L ,H,  H     ,  7  ];
[clk,  H , X , X,  X      , H, X ,   X ,  2  ] -> [ H ,          L ,  L ,  H , L ,H,  H     ,  7  ];
[clk,  H , X , X,  X      , H, X ,   X ,  3  ] -> [ L ,          L ,  L ,  H , L ,H,  H     ,  7  ];
[clk,  H , X , X,  X      , L, X ,   X ,  4  ] -> [ L ,          L ,  L ,  H , L ,H,  H     ,  7  ];
[clk,  H , L , X,  H      , L, X ,   X ,  5  ] -> [ H ,          H ,  L ,  H , L ,H,  H     ,  7  ];
[clk,  H , L , X,  X      , L, X ,   X ,  6  ] -> [ H ,          H ,  L ,  H , H ,H,  H     ,  7  ];
[clk,  H , L , X,  X      , L, X ,   X ,  7  ] -> [ H ,          H ,  L ,  H , H ,H,  H     ,  7  ];
[clk,  H , L , X,  X      , L, X ,   X ,  8  ] -> [ H ,          H ,  L ,  H , H ,H,  H     ,  7  ];
[clk,  H , L , X,  X      , L, X ,   X ,  9  ] -> [ H ,          L ,  L ,  H , H ,H,  H     ,  7  ];
[clk,  H , L , X,  X      , L, X ,   X , 10  ] -> [ H ,          L ,  H ,  H , H ,H,  H     ,  7  ];
[clk,  H , L , X,  X      , L, X ,   X , 11  ] -> [ H ,          L ,  H ,  L , H ,H,  L     ,  7  ];
[clk,  H , L , X,  X      , L, X ,   X , 12  ] -> [ H ,          L ,  H ,  L , H ,L,  L     ,  7  ];
[clk,  H , L , X,  X      , L, X ,   X , 13  ] -> [ H ,          L ,  H ,  L , H ,L,  L     ,  7  ];
[clk,  H , L , X,  X      , L, X ,   X , 14  ] -> [ H ,          L ,  H ,  L , H ,H,  H     ,  3  ];

test_vectors  'HOLDING STATE 3 WITH EXTENDED REFRESH REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H , X , X,  H            , X, X ,   L ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3     ];
 [clk,       H , X , X,  H            , L, X ,   X ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3     ];
 [clk,       H , X , X,  L            , X, X ,   X ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  8     ];

test_vectors  'EXTENDED REFRESH CYCLE'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H , X , X,  X            , X, X ,   X ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  8     ];
 [clk,       H , X , X,  X            , X, X ,   X ,  1  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  8     ];
 [clk,       H , X , X,  X            , X, X ,   X ,  2  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  8     ];
 [clk,       H , X , X,  X            , X, X ,   X ,  3  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  7     ];


end SCDECODE
```

APPENDIX B

```
NAME      SCDECODE;
PARTNO    T10004;
DATE      05/07/87 ;
REV       01 ;
DESIGNER  Breuninger/Peprah;
COMPANY   Texas Instruments;
ASSEMBLY  None ;
LOCATION  Dallas;

/*************************************************************************************/
/*   Static Column Decode                                                            */
/*                                                                                   */
/*                                                                                   */
/*        This is an example of how the PSG507 can be used to generate the           */
/*   required memory timing control signals (RAS, CAS, MSEL etc) for static          */
/*   column decode implementation using the ALS6301, ALS6310 and the ALS630          */
/*   ALS6300, in a system environment.                                               */
/*                                                                                   */
/*                                                                                   */
/*************************************************************************************/
/*   Allowable Target Device Types :  TEXAS INSTRUMENTS  PSG507                      */
/*************************************************************************************/

/**  Inputs  **/

pin  1          =  OSC      ;          /* Oscillator                          */
pin  2          =  RESET    ;          /* System Reset - when low             */
pin  3          =  A22      ;          /* IO/!M - Memory access               */
pin  4          =  RW       ;          /* Read / Write  Enable                */
pin  5          =  REFREQ   ;          /* Refresh Request                     */
pin  6          =  AS       ;          /* Addr Strobe - access request        */
pin  7          =  HSA      ;          /* High Speed Access                   */
pin 18          =  SYSCLK   ;          /* System Clock - (OSC/2)              */

/**  Outputs  **/

pin  8          =  RFC      ;          /* Refresh Complete                    */
pin  9          =  RASI     ;          /* Row Address Strobe                  */
pin 10          =  MSEL     ;          /* Multiplexer Select                  */
pin 11          =  CASI     ;          /* Column Address Strobe               */
pin 13          =  MCI_     ;          /* Mode Control                        */
pin 14          =  W        ;          /* Write                               */
pin 15          =  DSACK    ;          /* Data Strobe Acknowledge             */

/** Node Declarations **/
pinnode [33..38] = [C0..5]  ;          /* Built-in 6-Bit counter              */
pinnode 39       = SCLR0    ;          /* Counter Cclear- non registered      */
pinnode 41       = CNTHOLD0 ;          /* Counter Hold - non registered       */
pinnode 42       = CNTHOLD1 ;          /* Counter Hold - registered           */
node               [P3..0]  ;          /* Buried State Registers              */
node               AGREQ    ;          /* Access Grant Request                */
```

```
/** Declarations and Intermediate Variable Definition **/
field COUNT     = [C5..0]   ;
field STATE     = [P3..0]   ;
$define ST0       'b'0000
$define ST1       'b'0001
$define ST2       'b'0010
$define ST3       'b'0011
$define ST4       'b'0100
$define ST5       'b'0101
$define ST6       'b'0110
$define ST7       'b'0111
$define ST8       'b'1000

/* BUILT-IN COUNTER CONTROL EQUATIONS */

SCLR0       = !RESET                          /* Clear counter when RESET is low      */
            # ST2 & COUNT:'d'5                /* and during transitions at the end    */
            # ST4 & COUNT:'d'0                /* the indicated states and counts.     */
            # ST5 & COUNT:'d'10               /*                                      */
            # ST6 & COUNT:'d'4                /*                                      */
            # ST7 & COUNT:'d'6 & (A22 & AGREQ)/*                                      */
            # ST7 & COUNT:'d'14               /*                                      */
            # ST8 & COUNT:'d'3;               /*                                      */

CNTHOLD1.s  = !RESET                          /* Set count hold while clearing        */
            # ST2 & COUNT:'d'5                /* the counters accordingly.            */
            # ST4 & COUNT:'d'0                /*                                      */
            # ST5 & COUNT:'d'10               /*                                      */
            # ST6 & COUNT:'d'4                /*                                      */
            # ST7 & COUNT:'d'6 & (A22 & AGREQ)/*                                      */
            # ST7 & COUNT:'d'14               /*                                      */
            # ST8 & COUNT:'d'3;               /*                                      */

 CNTHOLD1.r = ST0 & !REFREQ & RESET           /* Reset count hold on transition to ST7 */
            # ST1 & !A22 & RESET              /* Reset count hold on transition to ST2 */
            # ST3 & !REFREQ & RESET           /* Reset count hold on transition to ST8 */
            # ST3 &  REFREQ &  AS             /* Reset count hold on transition to ST4 */
                 & SYSCLK & RESET;

/** State Machine Equations **/
sequence STATE {
present ST0:
       if(REFREQ & (!AS  # !SYSCLK))       next ST0;
       if(REFREQ &  AS & SYSCLK & RESET)   next ST1;
       if(!REFREQ &  RESET)                next ST7;
       default                             next ST0;

present ST1:
       if(COUNT:'d'0 & !A22)               next ST2;
       if(COUNT:'d'0 &  A22)               next ST0;
       default                             next ST1;

present ST2:
       /* NORMAL ACCESS CYCLE */
       if(COUNT:'d'0) &  RESET             next ST2 out !RAS1;
       if(COUNT:'d'1)                      next ST2 out  MSEL;
       if(COUNT:'d'2) & RESET              next ST2 out [!CAS1,!DSACK];
       if(COUNT:'d'3) & RESET              next ST2 out !W;
       if(COUNT:'d'5)                      next ST3 out [W,DSACK];
       default                             next ST2;
```

```
present ST3:
        /* HOLDING STATE    */
        if(!AS # !SYSCLK) & REFREQ & RESET   next ST3;
        if(REFREQ &  AS & SYSCLK & RESET)    next ST4;
        if(!REFREQ & RESET)                  next ST8;
        default                              next ST3;

present ST4:
        if(COUNT:'d'0) & A22 & RESET         next ST0 out [RASI,!MSEL,CASI];
        if(COUNT:'d'0) & !A22 & RESET        next ST4;
        if(COUNT:'d'1) & HSA & RESET         next ST5 out [RASI,!MSEL,CASI];
        if(COUNT:'d'1) & !HSA & RESET        next ST6 out !DSACK;
        default                              next ST4;

present ST5:
        /* EXTENDED ACCESS CYCLE */
        if(COUNT:'d'5) & RESET               next ST5 out !RASI;
        if(COUNT:'d'6) & RESET               next ST5 out  MSEL;
        if(COUNT:'d'7) & RESET               next ST5 out [!CASI,!DSACK];
        if(COUNT:'d'8) & RESET               next ST5 out !W;
        if(COUNT:'d'10) & RESET              next ST3 out [W,DSACK];
        default                              next ST5;

present ST6:
        /* HIGH SPEED ACCESS    */
        if(COUNT:'d'2) & RESET               next ST6 out !W;
        if(COUNT:'d'4)                       next ST3 out [W,DSACK];
        default                              next ST6;

present ST7:
        /* NORMAL REFRESH CYCLE */
        if AS                                next ST7 out !AGREQ;
        if(COUNT:'d'0) & RESET               next ST7 out !MC1_;
        if(COUNT:'d'1) & RESET               next ST7 out !RASI;
        if(COUNT:'d'3) & RESET               next ST7 out !RFC;
        if(COUNT:'d'5)                       next ST7 out [RFC,RASI];
        if(COUNT:'d'6) & (A22 # AGREQ)       next ST0 out  MC1_;
        if(COUNT:'d'6) & !A22 & !AGREQ       next ST7 out  MC1_;
        if(COUNT:'d'9) & RESET               next ST7 out !RASI;
        if(COUNT:'d'10) & RESET              next ST7 out  MSEL;
        if(COUNT:'d'11) & RESET              next ST7 out [!CASI,!DSACK];
        if(COUNT:'d'12) & RESET              next ST7 out !W;
        if(COUNT:'d'14)                      next ST3 out [W,DSACK];
        default                              next ST7;

present ST8:
        /* EXTENDED REFRESH CYCLE   */
        if(COUNT:'d'1)                       next ST8 out [RASI,!MSEL,CASI];
        if(COUNT:'d'3)                       next ST7;
        default                              next ST8; }

APPEND RASI.s = !RESET; APPEND CASI.s  = !RESET; APPEND RFC.s   = !RESET;
APPEND W.s    = !RESET; APPEND AGREQ.s = !RESET; APPEND DSACK.s = !RESET;
APPEND MC1_.s = !RESET; APPEND SCLR0   = !RESET; APPEND MSEL.r  = !RESET;
APPEND P0_.r  = !RESET; APPEND P1_.r   = !RESET; APPEND P2_.r    = !RESET;
APPEND P3_.r  = !RESET;
```

```
NAME      SCDECODE;
PARTNO    T10004;
DATE      05/07/87 ;
REV       01 ;
DESIGNER  Breuninger/Peprah;
COMPANY   Texas Instruments;
ASSEMBLY  None ;
LOCATION  Dallas;

/*************************************************************************************************/
/* Static Column Decode                                                                          */
/*                                                                                               */
/*      CUPL simulation file for the Static Column Decode Application                            */
/*                                                                                               */
/*************************************************************************************************/
/*  Allowable Target Device Types :  TEXAS INSTRUMENTS  PSG507                                   */
/*************************************************************************************************/

ORDER:  OSC,%4,RESET,%4,A22,%3,RW,%3,REFREQ,%5,AS,%2,HSA,%5,SYSCLK,%3,COUNT,
        %2,RFC,%4,RASI,%4,MSEL,%4,CASI,%3,MC1_,%2,W,%3,DSACK,%4,STATE;

BASE: DECIMAL;

VECTORS:

$msg"   ";
$msg"   ";
$msg"NORMAL ACCESS CYCLE";
$msg"   ";
$msg"     ----------------- INPUT -----------------  ------------- OUTPUT -------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------- ";
          C   0   X  X  X    X  X    X   'X'   H   H   L   H  H  H  H   "0"
          C   1   X  X  1    0  X    X   '0'   H   H   L   H  H  H  H   "0"
          C   1   X  X  1    1  X    1   '0'   H   H   L   H  H  H  H   "1"
          C   1   0  X  X    X  X    X   '0'   H   H   L   H  H  H  H   "2"
          C   1   X  X  X    X  X    X   '0'   H   L   L   H  H  H  H   "2"
          C   1   X  X  X    X  X    X   '1'   H   L   H   H  H  H  H   "2"
          C   1   X  X  X    X  X    X   '2'   H   L   H   L  H  H  L   "2"
          C   1   X  X  X    X  X    X   '3'   H   L   H   L  H  L  L   "2"
          C   1   X  X  X    X  X    X   '4'   H   L   H   L  H  L  L   "2"
          C   1   X  X  X    X  X    X   '5'   H   L   H   L  H  H  H   "3"

$msg"   ";
$msg"   ";
$msg"HOLDING STATE 4 WITH EXTENDED ACCESS REQUEST";
$msg"   ";
$msg"     ----------------- INPUT -----------------  ------------- OUTPUT -------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------- ";
          C   1   1  X  1    1  X    1   '0'   H   L   H   L  H  H  H   "4"
          C   1   0  X  X    X  X    X   '0'   H   L   H   L  H  H  H   "4"
          C   1   X  X  X    X  1    X   '1'   H   H   L   H  H  H  H   "5"
```

```
$msg"   ";
$msg"   ";
$msg"EXTENDED ACCESS";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------- OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
           C   1   X  X  X    X  X    X   '2'   H   H   L   H  H  H  H   "5"
           C   1   X  X  X    X  X    X   '3'   H   H   L   H  H  H  H   "5"
           C   1   X  X  X    X  X    X   '4'   H   H   L   H  H  H  H   "5"
           C   1   X  X  X    X  X    X   '5'   H   L   L   H  H  H  H   "5"
           C   1   X  X  X    X  X    X   '6'   H   L   H   H  H  H  H   "5"
           C   1   X  X  X    X  X    X   '7'   H   L   H   L  H  H  L   "5"
           C   1   X  X  X    X  X    X   '8'   H   L   H   L  H  L  L   "5"
           C   1   X  X  X    X  X    X   '9'   H   L   H   L  H  L  L   "5"
           C   1   X  X  X    X  X    X  '10'   H   L   H   L  H  H  H   "3"

$msg"   ";
$msg"   ";
$msg"HOLDING STATE 4 WITH HIGH SPEED ACCESS REQUEST";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------- OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
           C   1   1  X  1    1  X    1   '0'   H   L   H   L  H  H  H   "4"
           C   1   0  X  X    X  X    X   '0'   H   L   H   L  H  H  H   "4"
           C   1   0  X  X    X  0    X   '1'   H   L   H   L  H  H  L   "6"

$msg"   ";
$msg"   ";
$msg"HIGH SPEED ACCESS";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------- OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
           C   1   X  X  X    X  X    X   '2'   H   L   H   L  H  L  L   "6"
           C   1   X  X  X    X  X    X   '3'   H   L   H   L  H  L  L   "6"
           C   1   X  X  X    X  X    X   '4'   H   L   H   L  H  H  H   "3"

$msg"   ";
$msg"   ";
$msg"NON-MEMORY ACCESS FOLLOWED BY REFRESH REQUEST";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------- OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
           C   1   1  X  1    1  X    1   '0'   H   L   H   L  H  H  H   "4"
           C   1   1  X  X    X  X    X   '0'   H   H   L   H  H  H  H   "0"
           C   1   X  X  1    0  X    X   '0'   H   H   L   H  H  H  H   "0"
           C   1   X  X  1    X  X    0   '0'   H   H   L   H  H  H  H   "0"
           C   1   X  X  0    X  X    X   '0'   H   H   L   H  H  H  H   "7"
```

```
$msg"   ";
$msg"   ";
$msg"NORMAL REFRESH CYCLE";
$msg"   ";
$msg"     ----------------- INPUT -----------------  -------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RAS1,MSEL,CAS1,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------- ";
          C   1   X  X  X    0  X    X   '0'   H   H   L   H  L  H  H   "7"
          C   1   X  X  X    0  X    X   '1'   H   L   L   H  L  H  H   "7"
          C   1   X  X  X    0  X    X   '2'   H   L   L   H  L  H  H   "7"
          C   1   X  X  X    0  X    X   '3'   L   L   L   H  L  H  H   "7"
          C   1   X  X  X    0  X    X   '4'   L   L   L   H  L  H  H   "7"
          C   1   X  X  1    0  X    X   '5'   H   H   L   H  L  H  H   "7"
          C   1   X  X  X    0  X    X   '6'   H   H   L   H  H  H  H   "0"

$msg"   ";
$msg"   ";
$msg"NORMAL REFRESH CYCLE FOLLOWED BY ACCESS GRANT REQUEST";
$msg"   ";
$msg"     ----------------- INPUT -----------------  -------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RAS1,MSEL,CAS1,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------- ";
          C   1   X  X  0    X  X    X   '0'   H   H   L   H  H  H  H   "7"
          C   1   X  X  X    0  X    X   '0'   H   H   L   H  L  H  H   "7"
          C   1   X  X  X    0  X    X   '1'   H   L   L   H  L  H  H   "7"
          C   1   X  X  X    1  X    X   '2'   H   L   L   H  L  H  H   "7"
          C   1   X  X  X    1  X    X   '3'   L   L   L   H  L  H  H   "7"
          C   1   X  X  X    0  X    X   '4'   L   L   L   H  L  H  H   "7"
          C   1   0  X  X    0  X    X   '5'   H   H   L   H  L  H  H   "7"
          C   1   0  X  X    0  X    X   '6'   H   H   L   H  H  H  H   "7"
          C   1   0  X  X    0  X    X   '7'   H   H   L   H  H  H  H   "7"
          C   1   0  X  X    0  X    X   '8'   H   H   L   H  H  H  H   "7"
          C   1   0  X  X    0  X    X   '9'   H   L   L   H  H  H  H   "7"
          C   1   0  X  X    0  X    X  '10'   H   L   H   H  H  H  H   "7"
          C   1   0  X  X    0  X    X  '11'   H   L   H   L  H  H  L   "7"
          C   1   0  X  X    0  X    X  '12'   H   L   H   L  H  L  L   "7"
          C   1   0  X  X    0  X    X  '13'   H   L   H   L  H  L  L   "7"
          C   1   0  X  X    0  X    X  '14'   H   L   H   L  H  H  H   "3"

$msg"   ";
$msg"   ";
$msg"HOLDING STATE 3 WITH EXTENDED REFRESH REQUEST";
$msg"   ";
$msg"     ----------------- INPUT -----------------  -------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RAS1,MSEL,CAS1,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------- ";
          C   1   X  X  1    X  X    0   '0'   H   L   H   L  H  H  H   "3"
          C   1   X  X  1    0  X    X   '0'   H   L   H   L  H  H  H   "3"
          C   1   X  X  0    X  X    X   '0'   H   L   H   L  H  H  H   "8"
```

```
$msg"   ";
$msg"   ";
$msg"EXTENDED REFRESH CYCLE";
$msg"   ";
$msg"     ----------------- INPUT -----------------  ------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------- ";
          C    I    X   X   X     X  X     X    '0'    H    L    H    L   H  H   H    "8"
          C    I    X   X   X     X  X     X    '1'    H    H    L    H   H  H   H    "8"
          C    I    X   X   X     X  X     X    '2'    H    H    L    H   H  H   H    "8"
          C    I    X   X   X     X  X     X    '3'    H    H    L    H   H  H   H    "7"
```

MOS Memory Quality and Reliability Strategy

Texas Instruments is committed to providing its customers with reliable, high quality memory products. MOS Memory management has applied a four point quality and reliability strategy to:

- Provide customers with the lowest cost of product ownership through quality, reliability, and service by:
  - — On-time delivery to minimize customer inventory.
  - — Quality performance that justifies ship-to-stock certification and eliminates the cost of component testing.
  - — No system manufacturing fallout.
  - — No warranty and service costs.
- Develop partnership relationships to service and solve customer problems and anticipate upcoming needs.
- Living quality improvement process from product creation and manufacture through product sales via our total quality control approach of:
  - — Design-in and build-in quality and reliability.
  - — In-control manufacturing.
  - — Leadership customer service.
- TI's performance measurement shall be by the customer's measurement and perception. The performance standard is continuous customer satisfaction.

Total Quality Control (TQC)

Total Quality Control at TI is a business management process encompassing all company functions. The goal of Total Quality Control (TQC) is continuous customer satisfaction. Utilizing a process of improvement through a positive feedback cycle, TQC is deployed in the MOS Memory Division from the initial design-in Q&R stage through in-control manufacturing and customer service (see Figure 1).

Proper application of the concept of "PLAN-DO-CHECK-ACT" allows a positive feedback loop that creates continuous improvement and breakthrough, as opposed to the "FIX-FIX-FIX-FIX" results of a negative loop (see Figure 2).

A. Design-In Quality and Reliability

Quality and reliability improvements at TI start with the chip and package design. The objective of MOS Memory's Design-In Quality and Reliability (DIR) thrust is: First pass qualification of new products, internally and at the customer. The TI approach to DIR has been to understand customer requirements of a product, and to formalize this knowledge into a database which incorporates both reliability modeling knowledge and "lessons learned" from historical problems and data evaluations. Before any new design is approved, the design is verified against a DIR "checklist". Design verification is planned to evolve to computer verification utilizing artificial intelligence.

B. In-Control Manufacturing

Documentation/Audit System

To assure in-control manufacturing, TI employs a hierarchical specification system. General specifications on all aspects of quality, reliability, and customer service are written and controlled by the central Quality and Reliability group. More detailed specifications control the operating practices of Product Customer Centers (PCC), Fabrication Customer Centers (FCC), and other support organizations. These specifications follow guidelines set by the higher level specifications but concentrate on the type of semiconductor product built by the PCC and FCC.

Regularly scheduled audits are performed within TI to ensure compliance with all specifications. The five types of audits performed are:

1. Self-audit: An internal audit within each PCC, FCC, or functional operation. This type of audit is conducted by persons within the operation and an additional person from outside of the operation.
2. Cross-audit: An audit by persons independent of the operation being audited.
3. Group audit: An audit of an operation conducted by the semiconductor group audits and procedures function, which is a part of the central Quality and Reliability organization.
4. Procedures audit: An audit of lower level specifications with respect to higher level specifications.
5. Compliance audit: An audit of operating practices with respect to specifications.

Statistical Process Control (SPC)

Quality improvement is achieved through Statistical Process Control (SPC). SPC is applied throughout the manufacturing operations of the MOS Memory division. The objectives of SPC are:

- — Control processes on a realtime basis.
- — Improve process capability (CP).
- — Reduce variability to target value (CPK).
- — Eliminate "out-of-spec" lots.
- — Achieve dependable delivery.
- — Lower cost-of-quality.

Computer hardware and artificial intelligence software have been coupled to establish interactive control allowing the computer to generate realtime control charts and prompt adjustments to equipment and processes (see Figure 3).

Die Fabrication Control

In addition to extensive SPC applications in our MOS fabrication centers, TI implements wafer level quality and reliability controls.

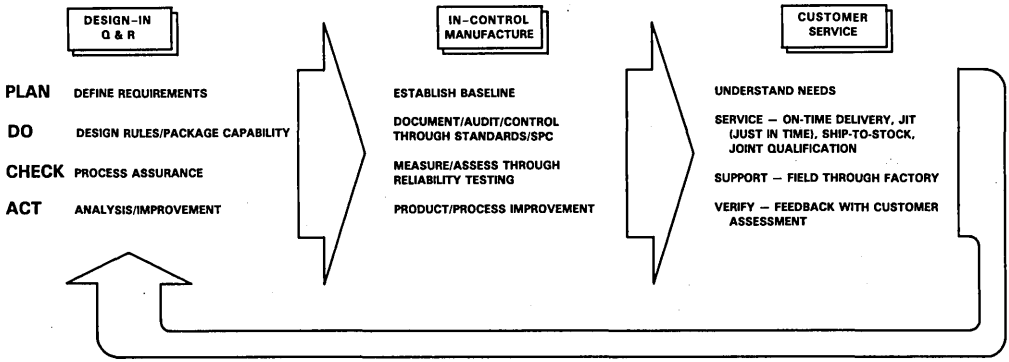


Figure 1. Total Quality Control

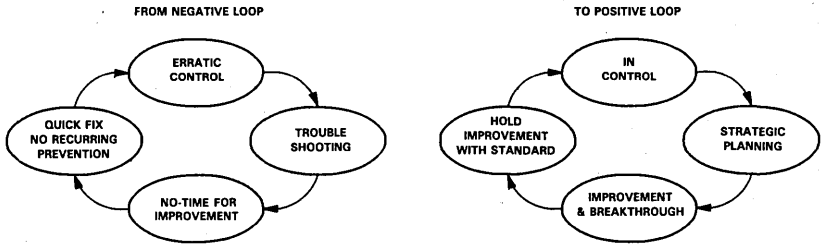


Figure 2. TQC Philosophy

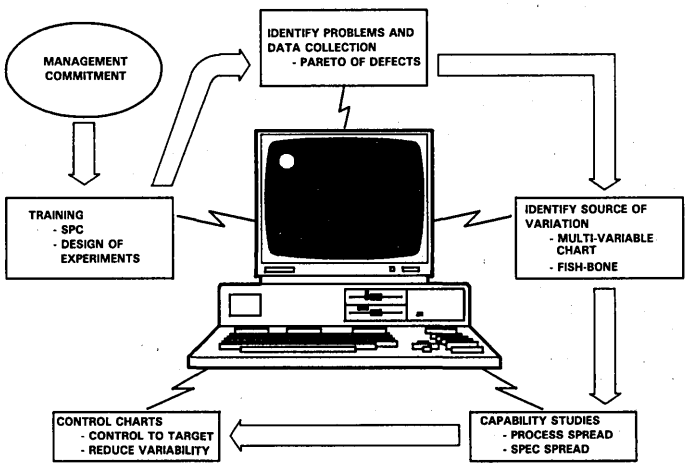


Figure 3. Computer Aided Statistical Process Control

Wafer (slice) level quality control focuses on reduction of variability around target values (CPK) for key functionality parameters and controls the processes that affect parameters. For example: Column access time (t_{CAC}) is a key DRAM parameter. One of the die manufacturing processes that affects t_{CAC} is the photo etch. To reduce variability of the target value of t_{CAC}, we control polysilicon width dimension at the photo etch process.

Wafer level reliability controls address process control of known reliability hazards. For example: Excessive phosphorus use in die processing can lead to corrosion defects in the finished device. Wafer level reliability controls require that phosphorus level control is built into the manufacturing process and that action is prescribed for out of control material. Other wafer level reliability controls are shown.

Table 1. Wafer Reliability Controls

PARAMETER	CONTROL
METAL	ELECTROMIGRATION TESTING GRAIN SIZE, SILICON NODULE MONITOR STEP COVERAGE/METAL NECKING MONITOR STRESS INDUCED METAL VOID TESTING
PROTECTIVE OVERCOAT	P.O. INTEGRITY STRESS TESTING THICKNESS MONITOR REFRACTION
CORROSION	% PHOSPHORUS IN MULTI-LEVEL OXIDE MONITOR
GATE OXIDE INTEGRITY	BREAKDOWN VOLTAGE

Device Assembly Control

TI has also implemented assembly level reliability controls and SPC at critical assembly points (see Table 2) to ensure highly reliable device packaging. Each parameter has certain controls performed at appropriate frequencies to ensure that assembly processing is progressing at qualified levels. Controls may be added or reduced after extensive testing has been performed and results studied carefully to preclude reliability problem introduction into the assembly process. The parameters and controls are shown in Table 3.

Table 2. Major Assembly Steps Using SPC/SQC†

PROCESS	CONTROL PARAMETER
PLASTIC DEVICE ASSEMBLY	
MOUNT	% COVERAGE OF EPOXY
BOND	BOND STRENGTH
MOLD	TEMPERATURE AND MOLDING PARAMETERS
TRIM/FORM	LEAD DEFLECTION (DIP)
CERAMIC DEVICE ASSEMBLY	
BOND	BOND STRENGTH
SEAL	SEAL FURNACE TEMPERATURE

†Statistical Process Control/Statistical Quality Control

Table 3. MOS Memory Assembly Level Reliability Controls

PARAMETER	CONTROL
P.O. INTEGRITY	CONTACTLESS WAFER MOUNT ON TAPE DIE MOUNT SYSTEM MOLD COMPOUND PARAMETERS
CHIP/CRACK	VISUAL INSPECTION TEMP CYCLE SAW BLADE CONDITIONS POKER PIN HEIGHT WET ETCH MONITOR (EPROM)
BOND INTEGRITY	BOND STRENGTH MONITOR BOND PARAMETERS BAKE/BOND PULL MONITOR CAPILLARY CHANGE
PACKAGE INTEGRITY	VISUAL INSPECTION MOLD PRESS PARAMETERS (PLASTIC) X-RAY INSPECTION (PLASTIC) TRIM/FORM (PLASTIC) PACKAGE SEAL (CERAMIC) TEMP CYCLE (CERAMIC) HERMETICITY MONITOR (CERAMIC)
DIE MOUNT INTEGRITY	DIE-SHEAR MONITOR CENTRIFUGE MONITOR X-RAY INSPECT LEADFRAME POLYIMIDE PATTERN INSPECT PICK-UP ARM FORCE
CONTAMINATION	VISUAL INSPECTION

C. Product Assessment/Improvement

Reliability Control System

The MOS Memory reliability control system (Figure 4) provides closed loop system feedback resulting in corrective actions and ongoing product improvements. Each new product, process, or major change to an existing product is internally qualified to industry leadership standards prior to production. This is followed by eight weeks of monitoring during production ramp-up and routine monitoring of more than 20,000 units a month once product achieves final production release. In 1986, almost one million memory devices were tested in all phases of the reliability control system.

Reliability Development Issues

Soft Error. TI has been doing much work in all phases of device development to minimize the effects of soft error. Soft errors are caused by alpha particles emitted by the decay of small amounts of thorium and uranium located in device packaging materials. TI maintains an aggressive program of evaluating new mold compounds to ensure low alpha emissivity. Certain device design and processing techniques are also applied to ensure a low soft error rate. The goal of device design and processing is to maximize the cell capacitance by employing an oxide-nitride dielectric, as opposed to an oxide dielectric. Also, the cell capacitance increases as the dielectric thickness decreases. Testing has shown that the trench capacitor used in dynamic RAMs has competitive soft error rates.

Channel Hot Electron. Channel hot electrons are caused by impact ionization in the drain pinch-off region. Electrons are accelerated toward the drain, collide with positive ions and can be trapped in the gate oxide. This trapped charge can change the characteristics of the transistor by raising the V_T (threshold voltage). One method employed to reduce the effects of hot electrons is to add a lightly doped drain to reduce the electric field at the gate. Testing for channel hot electrons is performed at a low temperature (−10°C) and a high drain voltage.

Latch-up. A CMOS device can latch up when the gain of the parasitic PNP+NPN transistors is greater than 1. These PNP+NPN transistors act as a silicon controlled rectifier (SCR). If enough current flows through the resistors, the transistors will turn on and the device will latch up.

To control latch-up, the SCR gain must be controlled to less than or equal to one. Methods for improving latch-up immunity include using an epitaxial substrate, incorporating guard rings between P+ and N+ diffusions, and isolating P+ and N+ diffusions.

Latch-up testing is performed to ensure our CMOS devices meet the minimum holding current for industry standards.

D. Customer Service

Quality, Reliability, Service, and the Cost of Ownership

The goal of Texas Instruments is to offer the best quality, reliability, and service in the semiconductor industry. The foundation for this approach is to ship consistent quality. Consistent quality allows ship-to-stock programs that foster the elimination of the customer's incoming inspection. Ship-to-stock quality, coupled with 100% on-time delivery to narrow shipping windows mean support of the customer's just-in-time manufacturing program. This combination of quality, reliability, and service can be measured by a single index called "the cost of ownership." The "cost of ownership" is defined as being composed of the purchase price, quality adders (for incoming inspection and board rework), inventory adders (for maintenance of a buffer inventory for suppliers who cannot meet just-in-time delivery), in-house reliability adders (for system burn-in and rework), and field reliability adders (for warranty and post warranty field repairs).

For more information about the cost of ownership concept, contact your local TI sales office and request the brochure "Texas Instruments Lowers Semiconductor Cost of Ownership," SSYB057.

Quality Improvement

Significant improvement in product quality has been achieved through:

- — Better definition of customer requirements.
- — Greater emphasis on quality as a design criterion.
- — Improved control of incoming materials.
- — Intensive training of supervisors and operators.
- — Extensive use of statistical process control.
- — More automation of operations to minimize operator related defects.

QUALIFICATION

- Process baseline
- 3 - 6 Diffusion lots
- Up to 7000 units tested

TEST	DRAM	EPROM	PROM†
125°C op. life	1100	300	200
EFR‡	2000	1000	500
85/85	300	–	200
Temp. cycle	600	150	600
Autoclave	300	–	200
Static bias/ Storage	250	300	150
Soft error	2000	–	–
Data retention Bake	–	600	150
Electromigration	150	–	–
Package integrity	470	400	200
ESD	30	20	20

†One-time programmable
‡EFR (Early Failure Rate)
DRAM - 125°C, 168 hr. op. life
EPROM, PROM - 200°C bake (PROM in ceramic package)

PRODUCTION RAMP MONITOR

- Up to 6400 units tested over 8 weeks

TEST	DRAM (WEEKLY)	EPROM (BI-MONTHLY)	PROM† (WEEKLY)
125°C op. life	200	200	120
85/85	200	–	120
Temp. cycle	200	200	120
Autoclave	200	–	120
200°C bake	–	200	–

- Scrap analysis
  - Die test escapes
  - Assembly defects
  - Test marginality
- Failure analysis studies
  - Failure mechanism
  - Activation energy

†One-time programmable

FINAL PRODUCTION RELEASE

- Control each package/wafer fabrication site/ device combination
- Ongoing reliability monitor of 125°C op. life, data retention bake, temp. cycle, 85/85, autoclave, package integrity, and internal cavity moisture
- Control limits set for each test
- Approximately 20,000 units tested each month
- Early failure rate monitor (devices tested monthly)

TEST	DRAM	EPROM
125°C op. life, 168 hr.	25,000	–
200°C bake, 44 hr.	–	1000-2000

- DRAMs receive 100% burn-in and burn-in lot acceptance
- EPROMs receive 100% 32 hr. data retention bake and/or 32 hr. data retention bake lot acceptance

Figure 4. Reliability Control System

As is demonstrated in Figure 5, MOS Memory EPROM and DRAM outgoing quality has dramatically improved during the last few years. This significant improvement has occurred for all TI product lines and has been recognized publicly by many of our customers, who have given TI more than 70 major quality awards in the last three years. Included among these awards are Ford's Q-1 award, the Naval Quality award, and the Deming Prize, which is Japan's most prestigious quality award.

Reliability Improvement

Low IC failure rates are achieved through design-in reliability, computer aided design, stringent qualification testing prior to product release, routine monitoring of released products, and an extensive failure mode tracking and feedback system for IC failures.

Since the early '80's, MOS Memory products have exhibited a device failure rate improvement trend which has resulted in highly reliable memory devices (see Figure 6). Since the memory device complexity also increases in an ongoing manner, the failure rate by function has improved at an even faster pace. TI continues to emphasize reliability improvement as a major factor in reducing the total cost of ownership for our customers. Reliability improvement is reflected as a reduction in the expected field failures during system lifetime.

Up-to-date quality and reliability data for MOS Memory products is available. Please contact your local TI sales office for information.

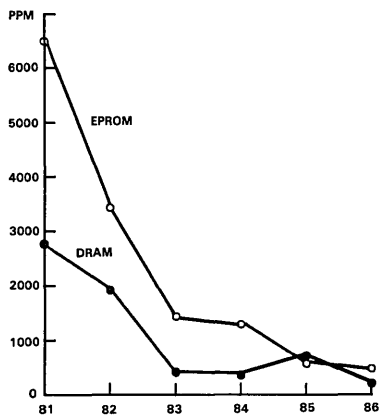


Figure 5. MOS Memory Quality Improvement

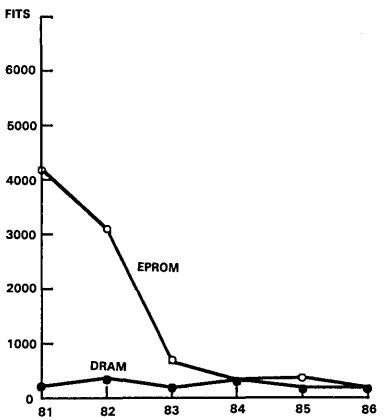


Figure 6. MOS Memory Reliability Improvement

EXPLANATION OF IEEE/IEC LOGIC SYMBOLS FOR MEMORIES

1. INTRODUCTION

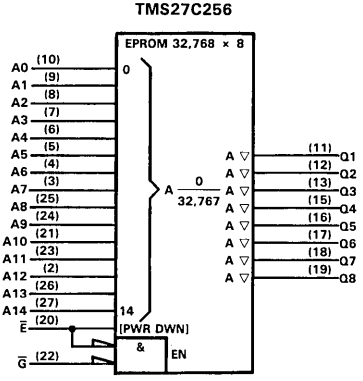
The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be partially explained below.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32. 14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

The current standards are IEC Publication 617-12, 1983, and ANSI/IEEE Standard 91-1984. Most of the data sheets in this data book include symbols prepared in accordance with these standards. The explanation that follows is necessarily brief and greatly condensed from the explanation given in the standards. This is not intended to be sufficient for people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book.

2. EXPLANATION OF A TYPICAL SYMBOL FOR A STATIC MEMORY

The TMS27C256 symbol will be explained in detail. This symbol includes almost all the features found in the PROMs and EPROMs.



The address inputs are arranged in the order of their assigned binary weights and the range of addresses are shown as A$\frac{m}{n}$ where m is the decimal equivalent of the lowest address and n is the highest. The outputs affected by these addresses are designated by the letter A, as data inputs would also be if the device were a RAM.

The polarity indicator ◺ indicates that the external low level causes the internal 1-state (the active or asserted state) at an input or that the internal 1-state causes the external low level at an output. The effect is similar to specifying positive logic and using the negation symbol ○ .

The ▽ symbols indicate three-state outputs. Three-state outputs will always be controlled by an EN function. When EN stands at its internal 1-state, the outputs are enabled; when EN stands at its internal 0-state, the outputs stand at their high-impedance states. Sometimes the EN is a single input but in the illustrated case, it is the output of a two-input AND gate. Both inputs (pins 20 and 22) are active low so if either one of them goes high, the outputs will be disabled. The upper one of these two inputs (pin 20) has another function. When nonstandard labels and explanatory labels are used within symbols, they are enclosed within square brackets. Here we find the label "[PWR DWN]". This is intended to indicate that if pin 20 is high, the memory will go to a low-power standby state.

3. THE BASICS

Section 3.1 illustrates the most common building blocks that are used in constructing symbols for memories. On the left are shown the symbols that specify the active levels for level-operated inputs, and the direction of active transition for dynamic inputs.

It is preferred to show all input lines on the left and all output lines on the right. When an exception is made to this left-to-right signal flow, an arrowhead is used to show the reverse signal flow.

Three symbols are shown that indicate three-state, open-drain, and open-source outputs. If none of these are used, the output should be assumed to be totem-pole. The common control block is a point of placement for inputs that affect an array of elements.

The drawings on the right define the three forms of *dependency notation* used in this book. At an input (or output) that affects other inputs or outputs, a letter (G, C, or Z) is placed followed by a number. That same number is placed at the affected inputs and outputs. The letter G indicates that an AND relationship exists; if the affecting input stands at the 0-state, it imposes that 0-state on the affected input or output. The letter C indicates a control relationship, usually between a clock and a D (data) input. If the C input stands at its 0-state, the affected input is disabled. A D input is always an input to a storage element, which it either sets to the 1-state or resets to the 0-state, unless the D input is disabled to have no effect. Z dependency is used to transfer a signal from one place in a symbol to another, for example from the output at Z4 across to a terminal labeled "4", or from the output at Z5 back to the "5" where it serves as an input with no terminal attached.

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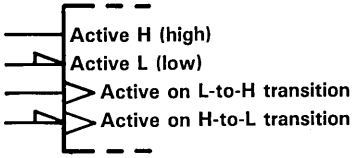
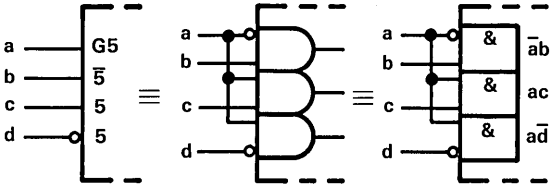
3.1 DIAGRAMATIC SUMMARY

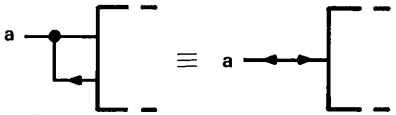
INPUTS



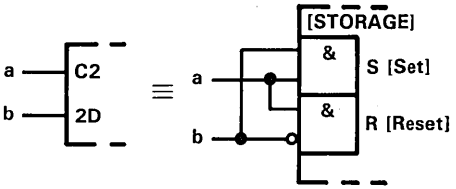
G (AND) DEPENDENCY



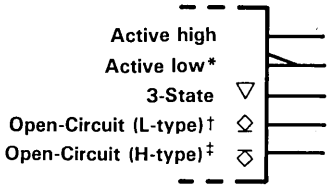
INPUT/OUTPUT



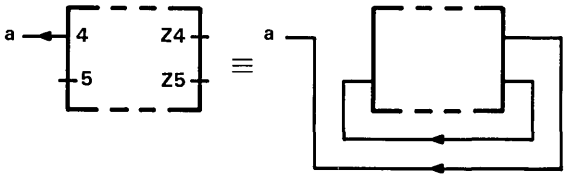
C (CONTROL) DEPENDENCY



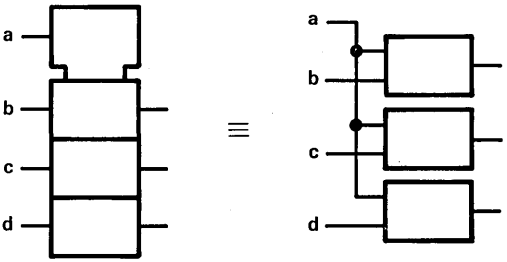
OUTPUTS



Z (INTERCONNECTION) DEPENDENCY



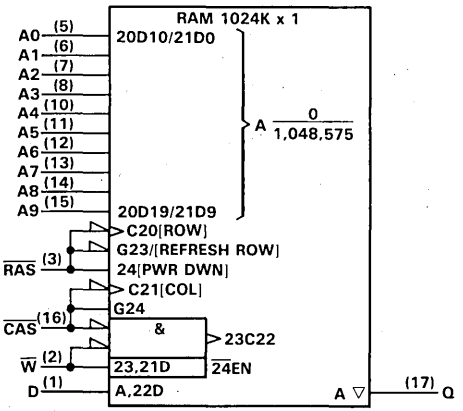
COMMON CONTROL BLOCK



*The active-low indicator may be used in combination with the 3-state and open-circuit indicators.
†L-types include N-channel open-drain and P-channel open-source outputs.
‡H-types include P-channel open-drain and N-channel open-source outputs.

4. EXPLANATION OF A TYPICAL SYMBOL FOR A DYNAMIC MEMORY

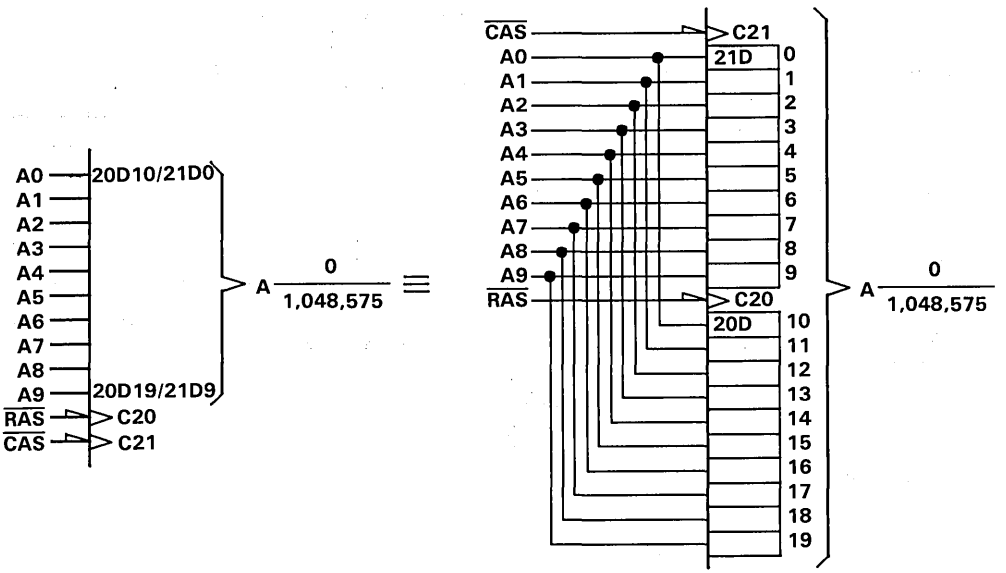
4.1 THE TMS4C1024 SYMBOL



The TMS4C1024 symbol will be explained in detail for each operating function. The assumption is made that Sections 2 and 3 have been read and understood. While this symbol is complex, so is the device it represents and the symbol shows how the part will perform depending on the sequence in which signals are applied.

4.2 ADDRESSING

The symbol above makes use of an abbreviated form to show the multiplexed, latched addresses. The blocks representing the address latches are implied but not shown.



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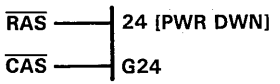
When $\overline{RAS}$ goes low, it momentarily enables (through C20, ▷ indicates a dynamic input) the D inputs of the ten address registers 10 through 19. When $\overline{CAS}$ goes low, it momentarily enables (through C21) the D inputs of the ten address registers 0 through 9. The outputs of the address registers are in 20 internal address lines that select 1 of 1,048,576 cells.

4.3 REFRESH

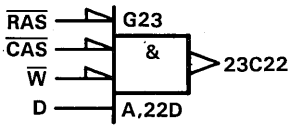
When $\overline{RAS}$ goes low, row refresh starts. It ends when $\overline{RAS}$ goes high. The other input signals required for refreshing are not indicated by the symbol.

4.4 POWER DOWN



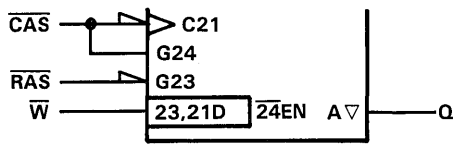
$\overline{CAS}$ is ANDed with $\overline{RAS}$ (through G24) so when $\overline{RAS}$ and $\overline{CAS}$ are both high, the device is powered down.

4.5 WRITE



By virtue of the AND relationship between $\overline{CAS}$ and $\overline{W}$ (explicitly shown), when either one of these inputs goes low with the other one and $\overline{RAS}$ already low ($\overline{RAS}$ is ANDed by G23), the D input is momentarily enabled (through C22). In an "early-write" cycle it is $\overline{W}$ that goes low first; this causes the output to remain off as explained below.

4.6 READ



The ANDed result of $\overline{RAS}$ and $\overline{W}$ (produced by G23) is clocked into a latch (through C21) at the instant $\overline{CAS}$ goes low. This result will be a "1" if $\overline{RAS}$ is low and $\overline{W}$ is high. The complement of $\overline{CAS}$ is shown to be ANDed with the output of the latch (by G24 and $\overline{24}$). Therefore, as long as $\overline{CAS}$ stays low, the output is enabled. In the "early-write" cycle referred to above, a "0" was stored in the latch by $\overline{W}$ being low when $\overline{CAS}$ went low, so the output remained disabled.

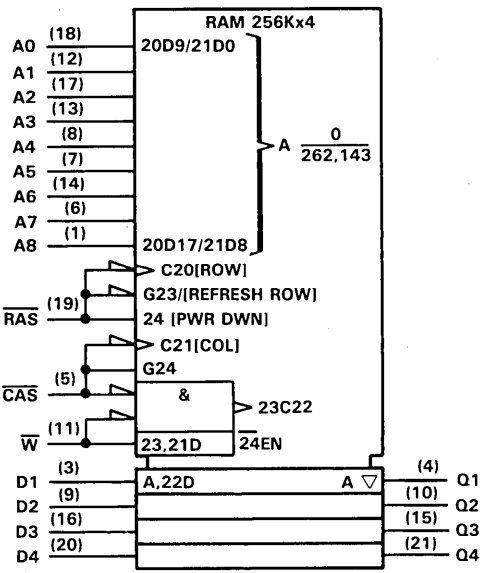
5. SYMBOLS FOR DYNAMIC RAM MODULES

A dynamic RAM module is created by attaching separate DRAMs in chip-carrier packages to a commor substrate. The symbols for the composite memory thus created starts with the symbol for the origina DRAM and is used with as little change as possible.

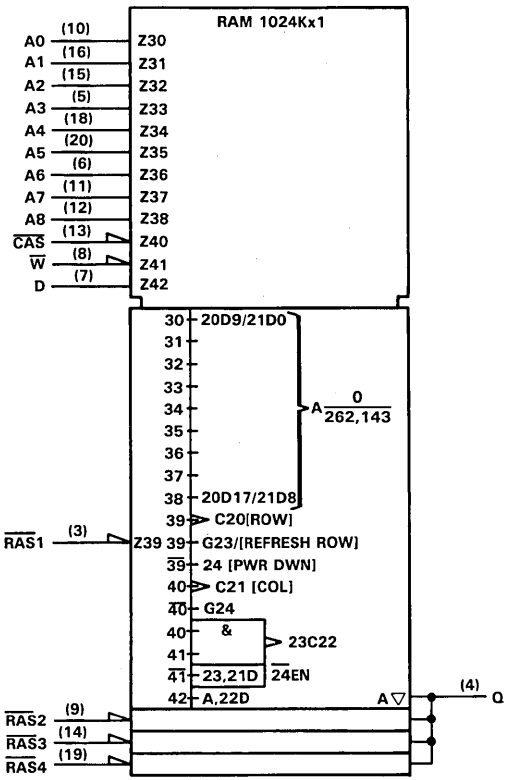
So far, two types of organizations have evolved. In the first, all like address and control inputs are connectec in parallel between the separate packages. Taking the TM4256EC4 as typical of this group, the symbo starts with that of the TMS4256 with the qualifying symbol changed from "RAM 256K × 1" to "RAM 256 × 4", and this becomes a common control block for an array of four input-output elements showr below it.

In the second type of organization, of which the TM4256FC1 is typical, most of the address and contro lines are parallel connected, but some are brought out separately for each of the DRAM packages. Tc maintain the recognizability of the original TMS4256 symbol, it has now been placed in the first element of the array. The empty rectangles located below the first element represents three other identical elements. Now interconnection (Z) dependency has been used (see 2 and 2.1) to show how $\overline{CAS}$, $\overline{W}$, D, and the address inputs connect to the first element, and since these inputs are located in the common contro block, the connections apply equally to all the elements. The connections for $\overline{RAS}1$, $\overline{RAS}2$, $\overline{RAS}3$, anc $\overline{RAS}4$ apply only to the individual elements.

TM4256EC4



TM4256FC1



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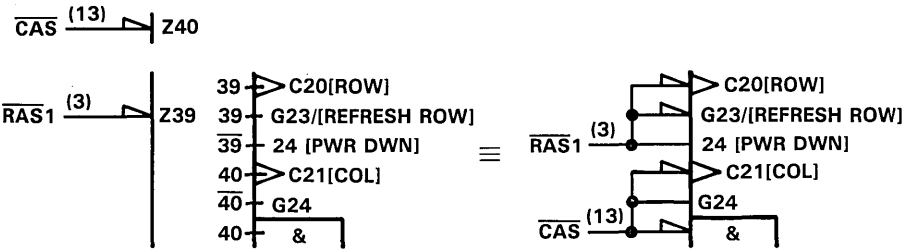
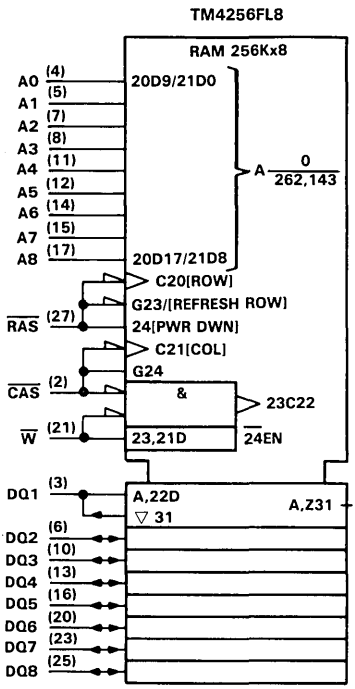
The drawings below illustrate the handling of control lines that in the original symbol were broken up into active-high and active-low functions. To make the combined symbol, the one of the two levels that seemed most appropriate was chosen, and then bars were used over the dependency numbers if necessary. For example, PWR DWN is an active-high function of pin 3, but it was decided that pin 3, $\overline{\text{RAS}}$, should be considered active low. The bar over the number 39 indicates that PWR DWN is a function of the *complement* of Z39 (ANDed with the complement of Z40 through G24), and the complement of active low is active high.



Another modification of the basic symbols that can occur in either organization is illustrated by the TM4256FL8. The TMS4256 has separate input and output pins. In the module, these have been connected together to form a single I/O port. In the module symbol, this is indicated using Z dependency to transfer the output signal from the right side to the left side.



If you have questions on this Explanation of IEEE/IEC Logic Symbols, please contact:

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Texas Instruments Incorporated
P.O. Box 225012
Dallas, Texas 75265
Telephone (214) 995-2659

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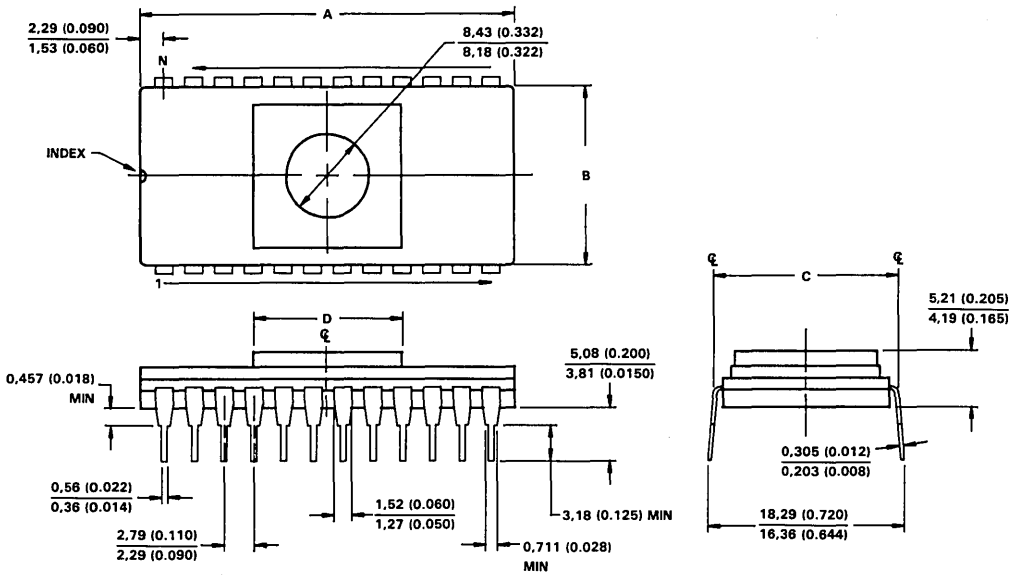
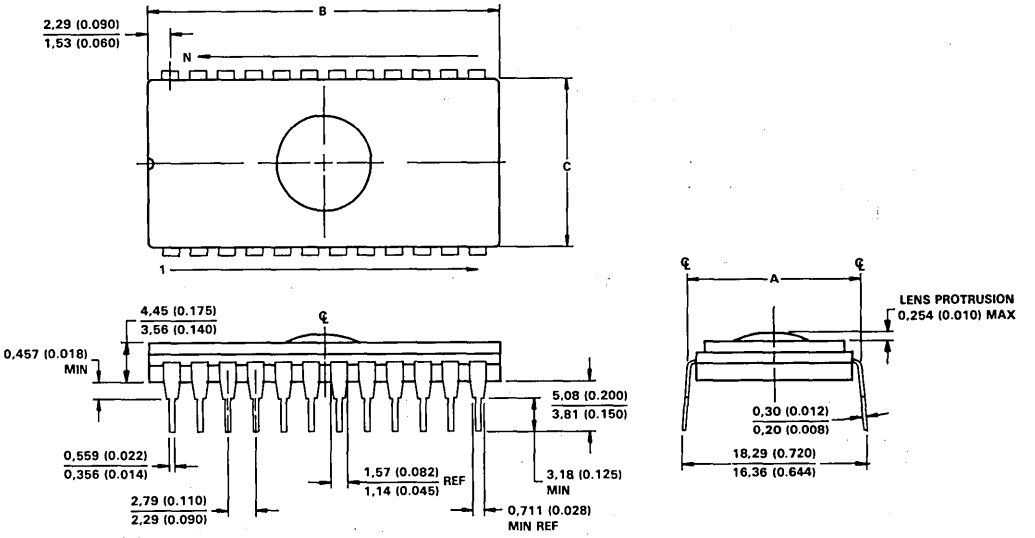
600-mil cerpak (J suffix)



DIM \ PIN	24	28
A (MAX)	15,75 (0.620)	15,75 (0.620)
(MIN)	14,99 (0.590)	14,99 (0.590)
B (MAX)	32,13 (1.265)	37,21 (1.465)
(MIN)	31,37 (1.235)	36,45 (1.435)
C (MAX)	13,74 (0.541)	13,74 (0.541)
(MIN)	12,67 (0.499)	1267 (0.499)
D (MAX)	12,90 (0.508)	17,02 (0.670)
(MIN)	12,50 (0.492)	16,51 (0.650)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

600-mil cerdip (J suffix)



DIM \ PIN	24 NARR	24 WIDE	28 NARR	28 WIDE	32 NARR	32 WIDE	40 NARR	40 WIDE
A (MAX)	15,85 (0.624)	15,85 (0.624)	15,85 (0.624)	15,85 (0.624)	15,85 (0.624)	15,85 (0.624)	15,85 (0.624)	15,85 (0.624)
(MIN)	14,99 (0.590)	14,99 (0.590)	14,99 (0.590)	14,99 (0.590)	14,99 (0.590)	14,99 (0.590)	14,99 (0.590)	14,99 (0.590)
B (MAX)	32,13 (1.265)	32,13 (1.265)	37,21 (1.465)	37,21 (1.465)	42,37 (1.668)	42,37 (1.668)	52,53 (2.068)	52,53 (2.068)
(MIN)	31,37 (1.235)	31,37 (1.235)	36,45 (1.435)	36,45 (1.435)	41,45 (1.632)	41,45 (1.632)	51,61 (2.032)	51,61 (2.032)
C (MAX)	13,74 (0.541)	15,19 (0.598)	13,74 (0.541)	15,19 (0.598)	13,74 (0.541)	15,19 (0.598)	13,74 (0.541)	15,19 (0.598)
(MIN)	13,06 (0.514)	14,50 (0.571)	13,06 (0.514)	14,50 (0.571)	13,06 (0.514)	14,50 (0.571)	13,06 (0.514)	14,50 (0.571)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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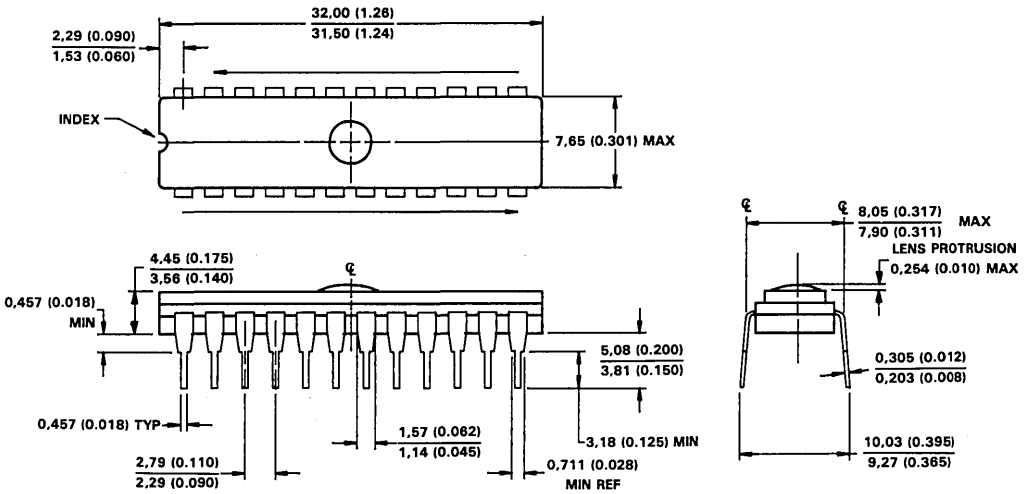
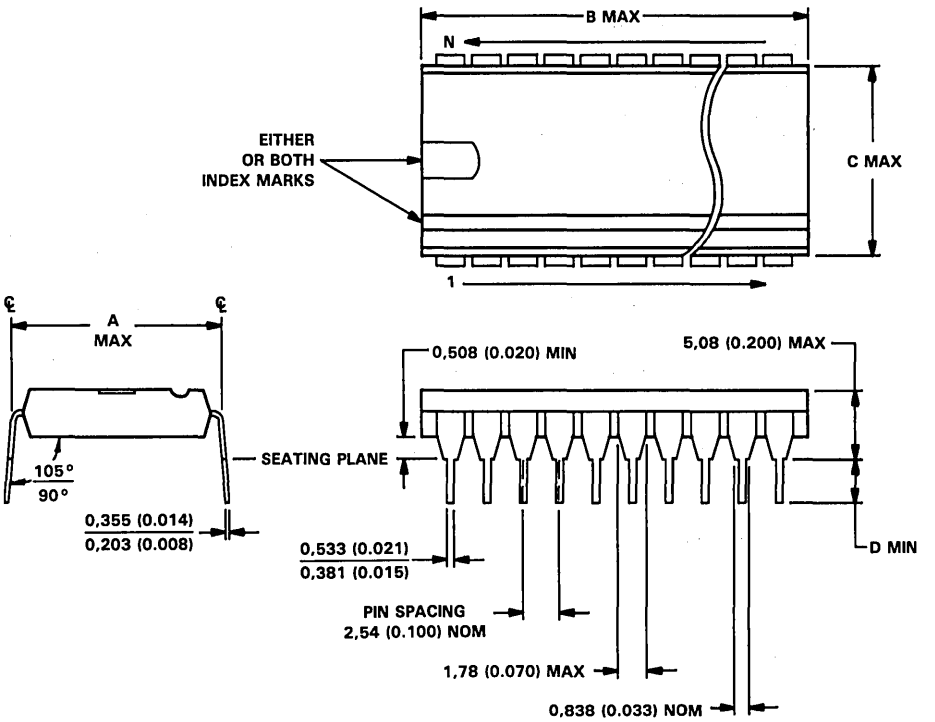
300-mil cerdip (J, JT suffixes)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

plastic packages (N suffix)



DIM \ PIN	16	18	20	22	24	24	24	28	32	40
A (MAX)	8,26 (0.325)	8,26 (0.325)	8,26 (0.325)	10,80 (0.425)	7,62 (0.300)	10,80 (0.425)	15,88 (0.625)	15,88 (0.625)	15,88 (0.625)	15,49 (0.610)
B (MAX)	22,10 (0.870)	23,37 (0.920)	27,18 (1.070)	28,45 (1.120)	31,75 (1.252)	31,04 (1.222)	32,26 (1.270)	36,83 (1.450)	41,94 (1.651)	53,09 (2.090)
C (MAX)	6,86 (0.270)	6,86 (0.270)	6,86 (0.270)	9,02 (0.355)	6,60 (0.260)	9,14 (0.360)	13,97 (0.550)	13,97 (0.550)	13,97 (0.550)	13,97 (0.550)
D (MIN)	3,18 (0.125)	2,921 (0.115)	2,92 (0.115)	3,18 (0.125)	3,30 (0.130)	3,18 (0.125)	2,92 (0.115)	2,92 (0.115)	3,18 (0.125)	3,18 (0.125)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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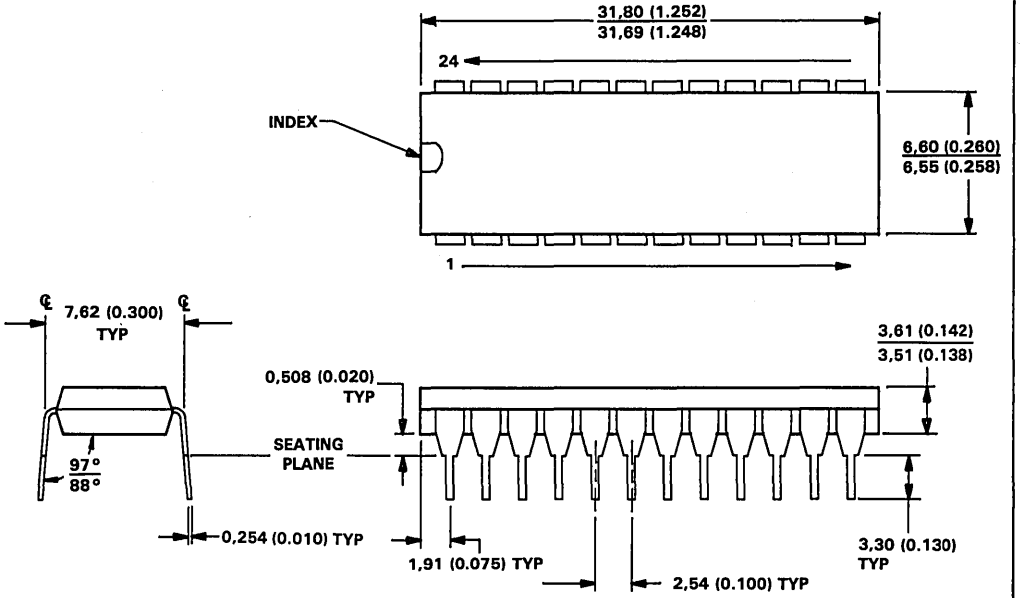
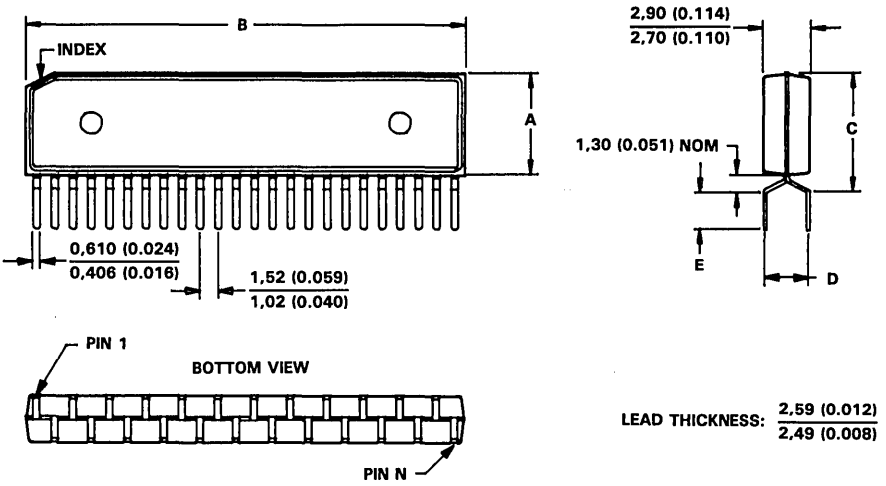
24-pin 300-mil plastic dual-in-line package (N, NT suffixes)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

zig-zag plastic package (SD suffix)



DIM \ PIN	16	24	28
A	7,00 (0.276) 6,80 (0.268)	8,74 (0.344) MAX	6,09 (0.342) NOM
B	20,70 (0.815) 20,30 (0.799)	31,29 (1.232) MAX	36,07 (1.420) NOM
C (MAX)	8,26 (0.325)	10,16 (0.400)	10,16 (0.400)
D	2,79 (0.110) 2,29 (0.090)	2,64 (0.104) 2,44 (0.096)	2,64 (0.104) 2,44 (0.096)
E	3,30 (0.130) 3,00 (0.120)	3,25 (0.128) 2,95 (0.116)	3,25 (0.128) 2,95 (0.116)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

TEXAS INSTRUMENTS
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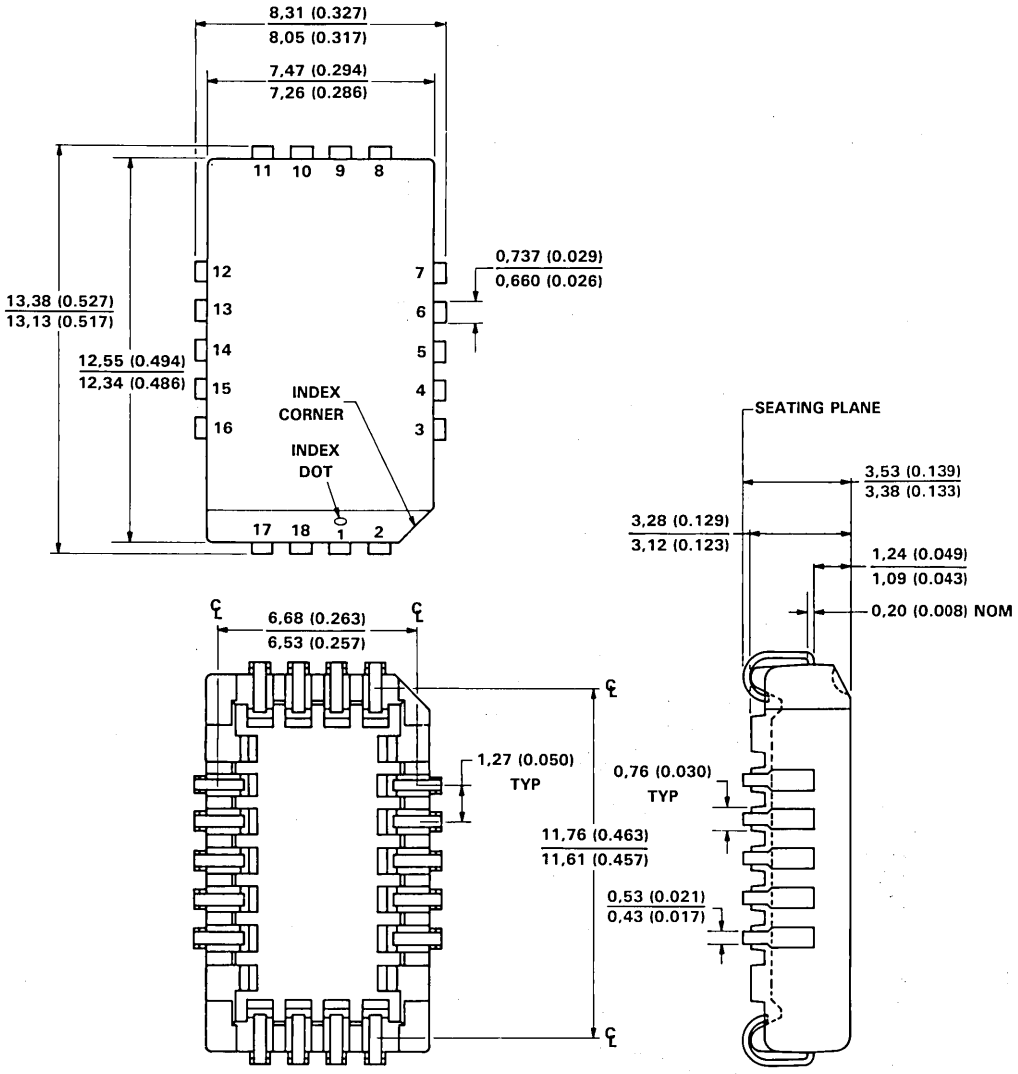
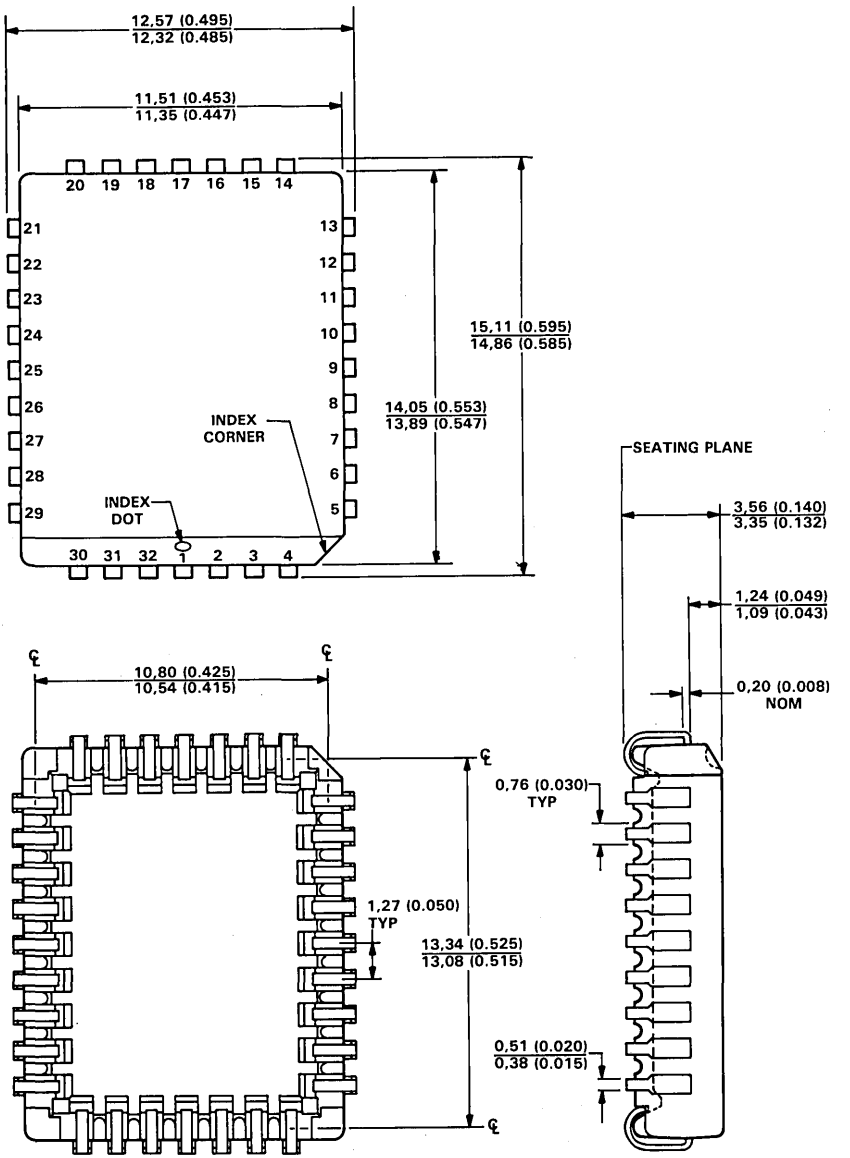
plastic chip carrier packages

18-lead plastic chip carrier package (FM suffix)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

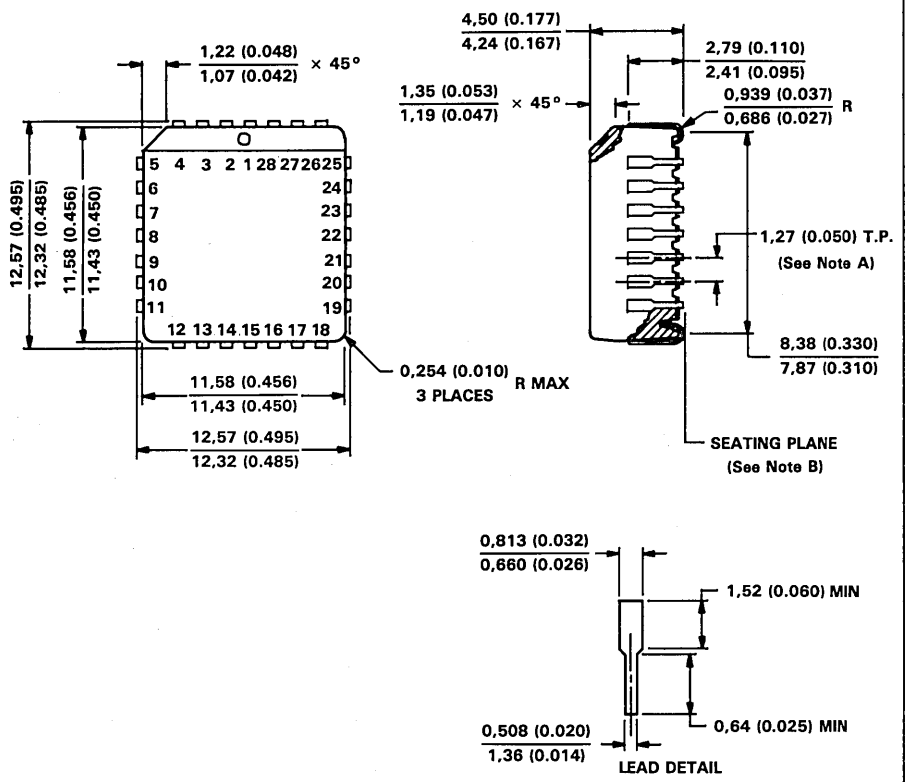
32-lead plastic chip carrier package (FM suffix)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

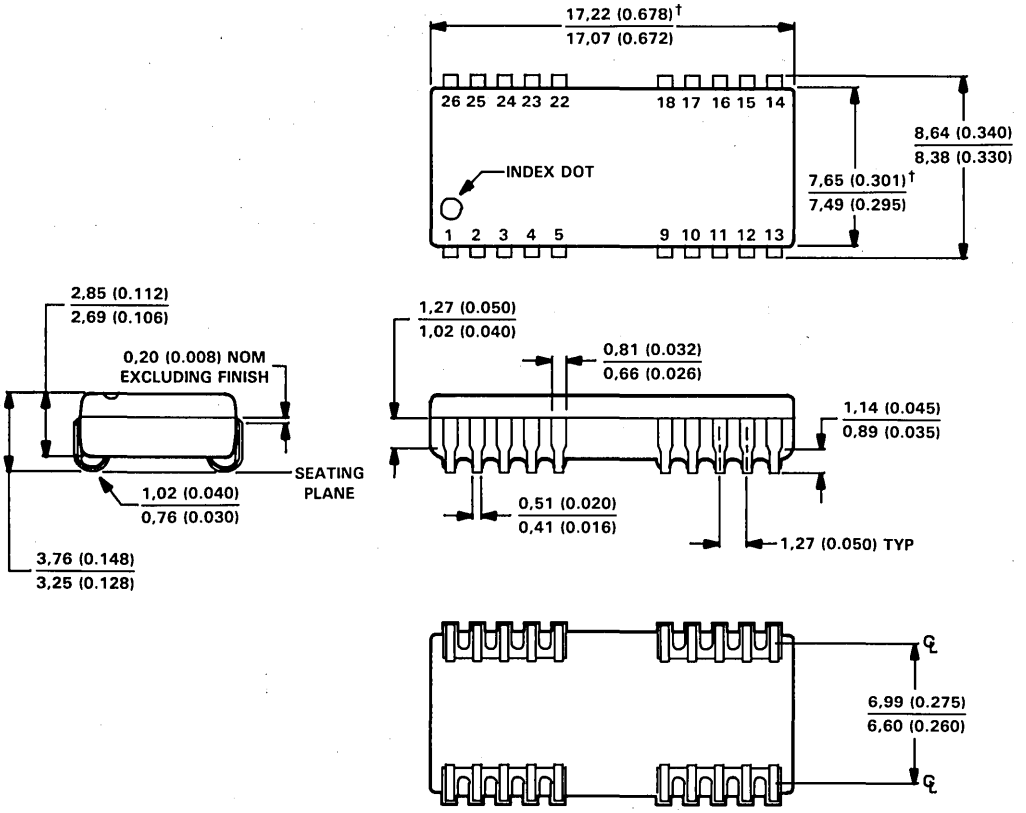
TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

28-lead plastic chip carrier package (FN suffix)



NOTES: A. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
B. The lead contact points are planar within 0,101 (0.004).

20/26-lead plastic small outline J-lead surface mount package (DJ suffix)

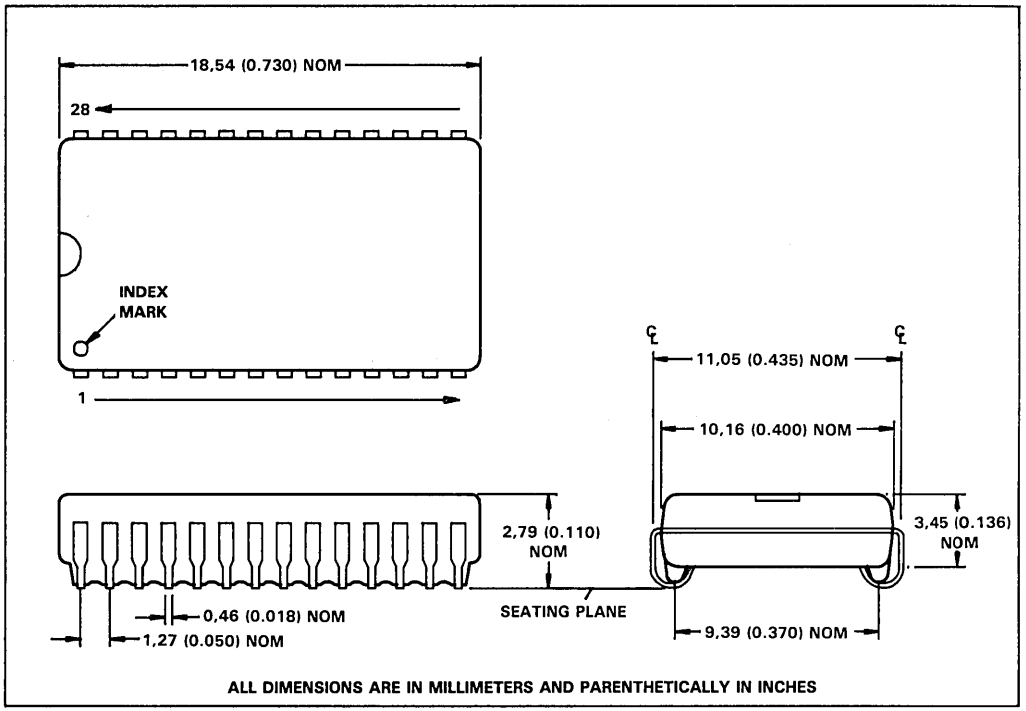


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

†Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0,125 (0.005).

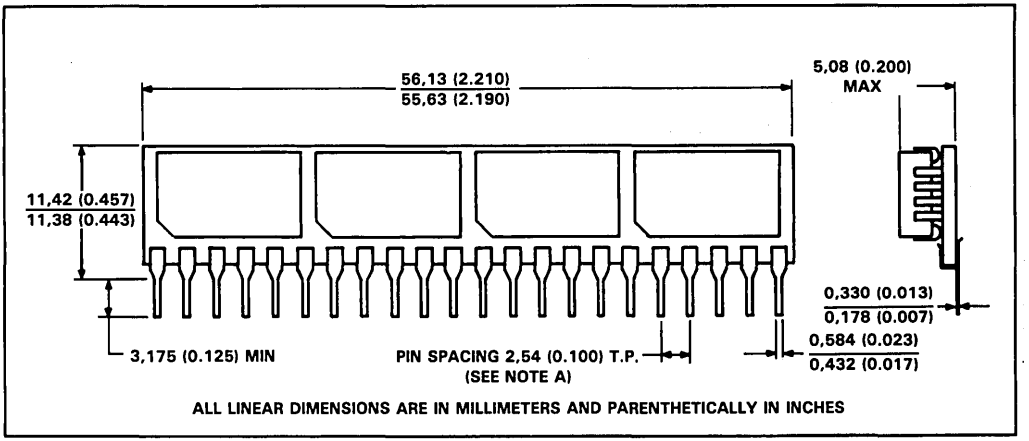
TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

28-lead plastic small outline J-lead surface mount package (DJ suffix)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

22-pin C single-in-line package



NOTE A: Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.

TEXAS INSTRUMENTS
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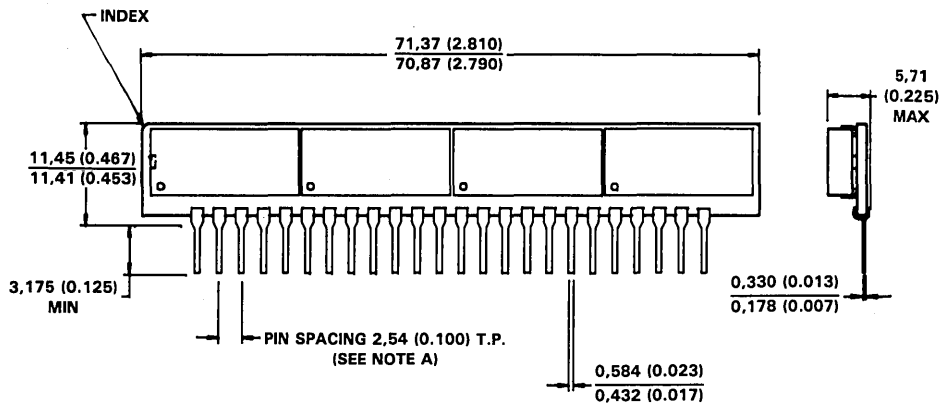
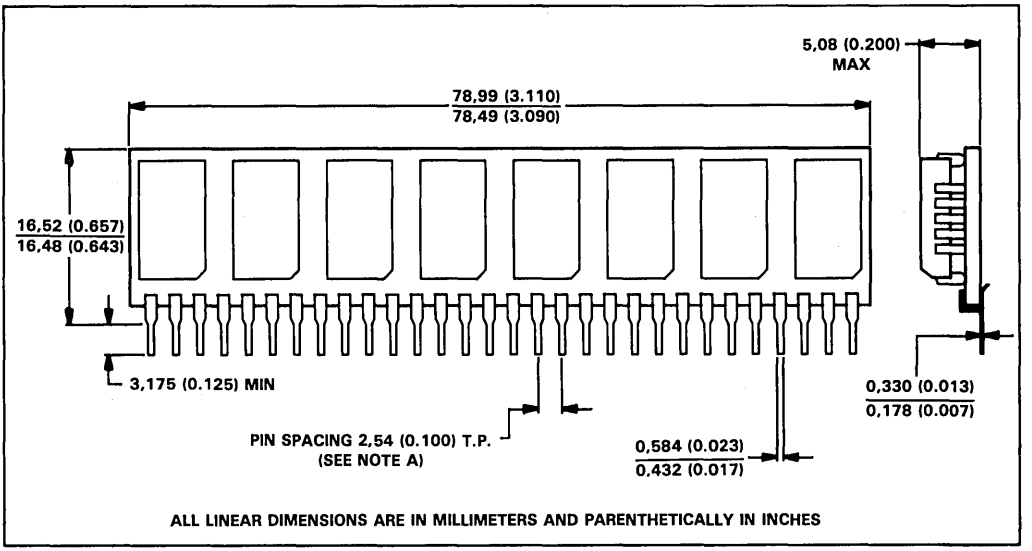
24-pin AC single-in-line package



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

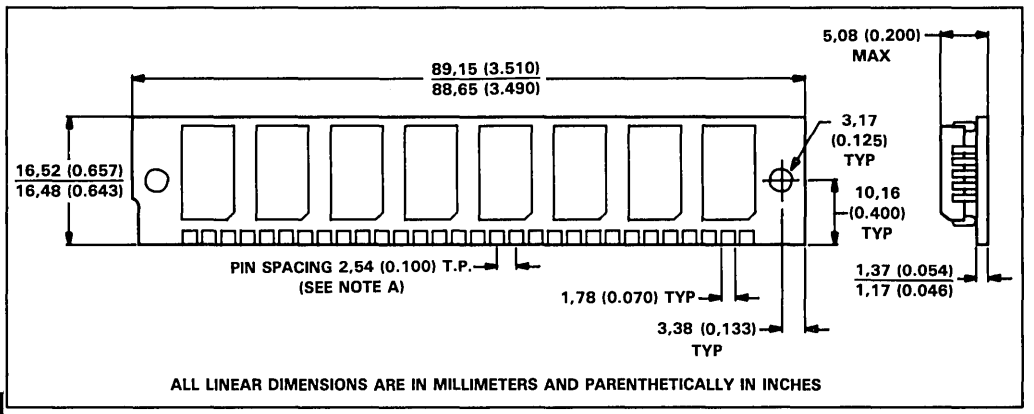
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

30-pin L single-in-line package



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

30-pin U single-in-line package



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

TEXAS INSTRUMENTS
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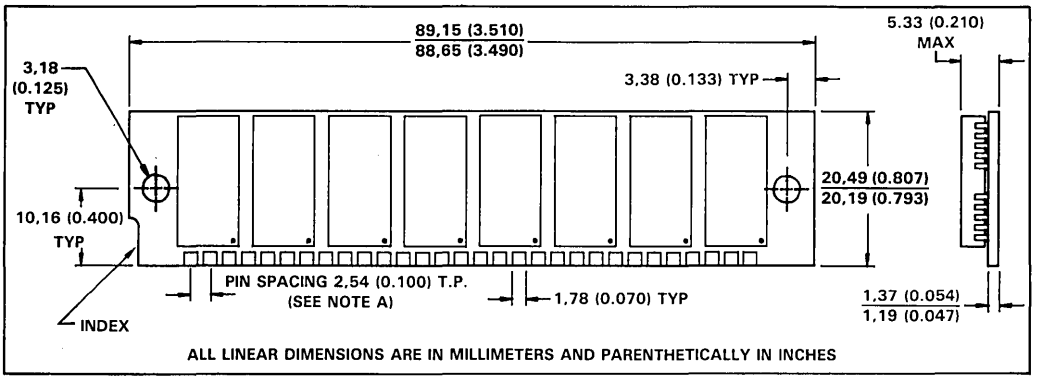
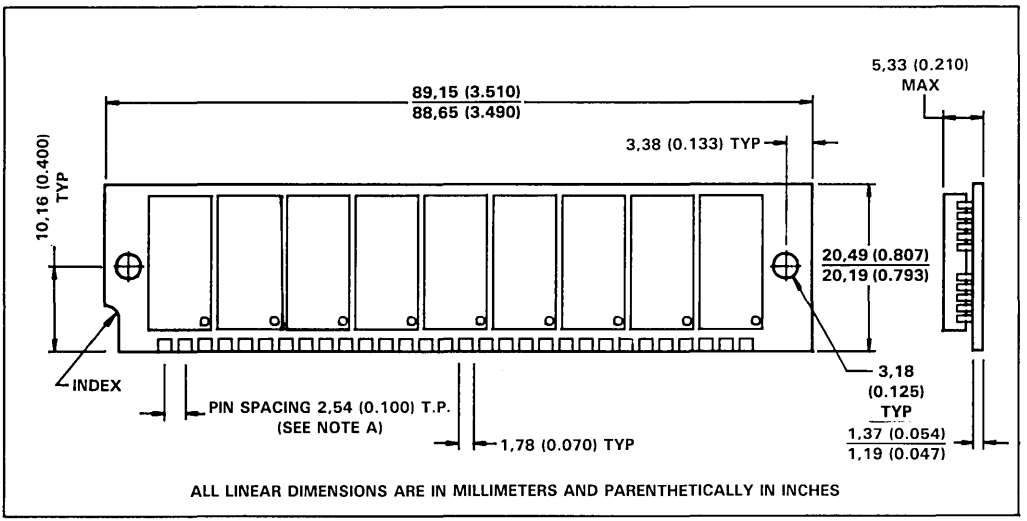
30-pin AD single-in-line package (TM024GAD8)



30-pin AD single-in-line package (TM024EAD9)



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

Military Packages

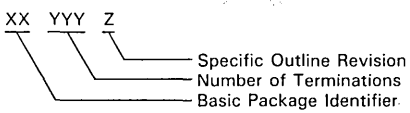
The packages offered by the Military Products Division of Texas Instruments Semiconductor Group are designed to provide the most efficient and cost-effective method of meeting Military system requirements. Products are offered in hermetic ceramic dual-in-line, ceramic flatpack, leadless ceramic chip carrier, leaded ceramic chip carrier, and ceramic pin grid array packages. All packages conform to the mechanical outlines contained in Appendix C of MIL-M-38510 except for package types that are not included in that specification. In the event of a conflict between dimensions contained in MIL-M-38510 Appendix C and other TI published mechanical outlines, MIL-M-38510 will take precedence.

Physical dimensions of the packages not contained in MIL-M-38510 Appendix C are contained in this document. This document also includes packages that are not completely defined in MIL-M-38510.

CERAMIC PACKAGES AVAILABLE

Package Designator	Description
GB	PGA
FD	Three-Layer Square LLCC – Non-JEDEC Pinouts
FG, FV	Three-Layer Rectangular LLCC – JEDEC Pinouts
FJ	Three-Layer Square "J" Formed LDCC
FK	Three Square LLCC – JEDEC Pinouts
J, JG, JT	Glass-Sealed CDIP
JD	Side-Brazed CDIP
HJ	"J" Formed Small Outline LDCC
HQ	Glass-Sealed Square LDCC
W, WA, WC, U	CPAK

The TI published mechanical outlines for a given package type may vary slightly from product to product. To identify the detailed outline drawing for a particular product, refer to the specific data sheet for that product. There will be detail outline subsets within a generic package category that will be identified as follows:



For example, there are two "FV" package outlines identified in this book:

Mechanical Outline	Description
FV018	18-Pad Leadless Ceramic Chip Carrier used for SMJ4256-XXFV
FV018A	18-Pad Leadless Ceramic Chip Carrier used for SMJ4464-XXFV

MIL-M-38510 APPENDIX C OUTLINES

Number Leads/ Contacts	Ceramic Dual-In-Line			Flat Package			Chip Carrier Pin Grid Array		
	MIL ID	TI ID	Appendix C Outline	MIL ID	TI ID	Appendix C Outline	MIL ID	TI ID	Appendix C Outline
8	P	JG	D-4						
10				H	U	F-4			
14	C	J	D-1	D, B	W, WA	F-2, F-3			
16	E	J, JD	D-2	F	W	F-5			
18	V	J, JD	D-6					FG	C-10
20	R	J, JD	D-8	S	W	F-9	2	FD, FK	C-2
20								FG	C-13A
24	L	JT	D-9	K	W	F-6			
24	J	J, JD	D-3						
28		J, JD	D-10				3	FD, FK	C-4
28								FG	C-11
32								FG	C-12
40	Q	JD	D-5						
44								FD, FJ	C-5, C-J4
68								FD, GB, FJ	C-7, P-BC, C-J5
84								FJ	C-J6

TEXAS INSTRUMENTS
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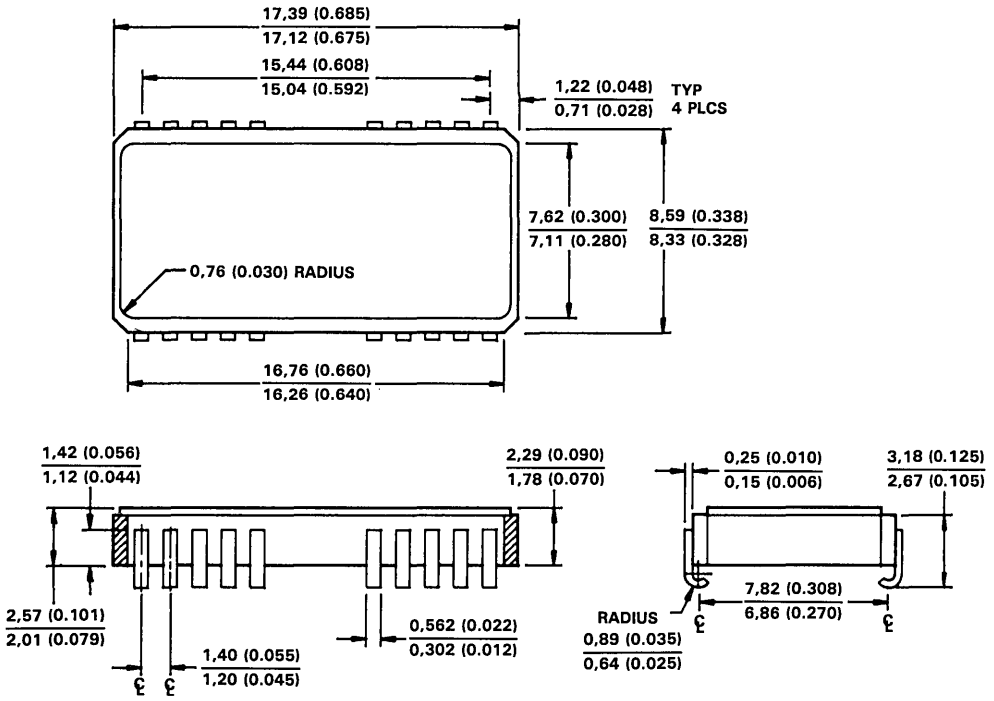
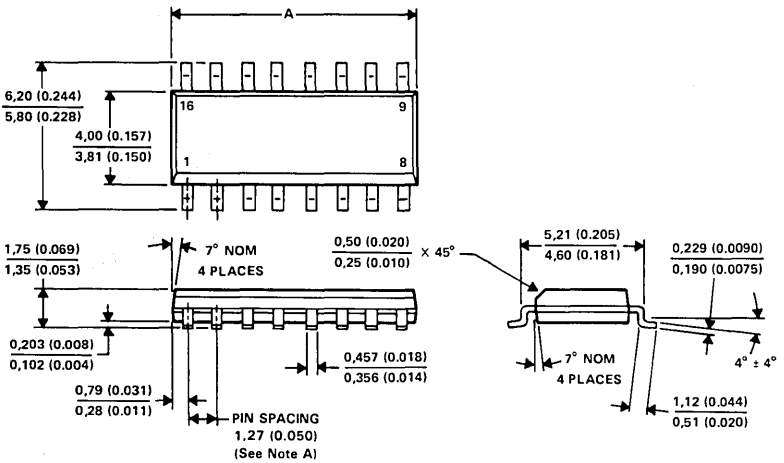
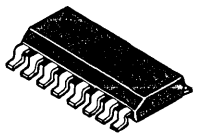
20-pin leaded ceramic chip carrier (HJ suffix)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALY IN INCHES

D PLASTIC PACKAGE
(16-pin package used for illustration)



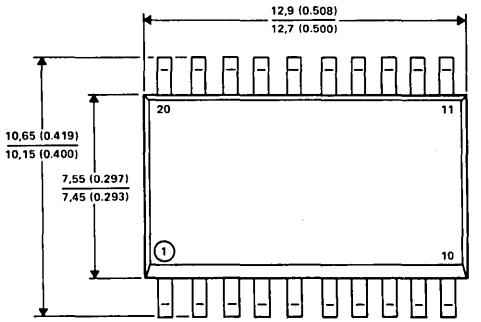


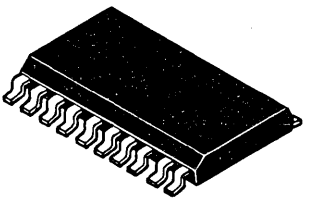
DIM \ PINS	8	14	16
A MIN	4,80	8,55	9,80
	(0.189)	(0.337)	(0.386)
A MAX	5,00	8,74	10,00
	(0.197)	(0.344)	(0.394)

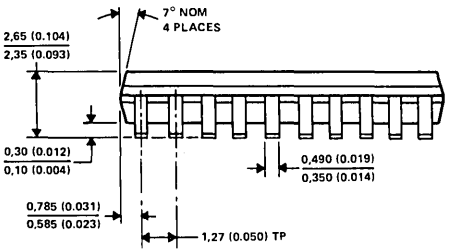
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

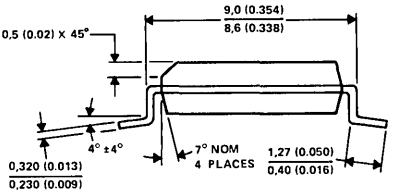
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

20-PIN DW









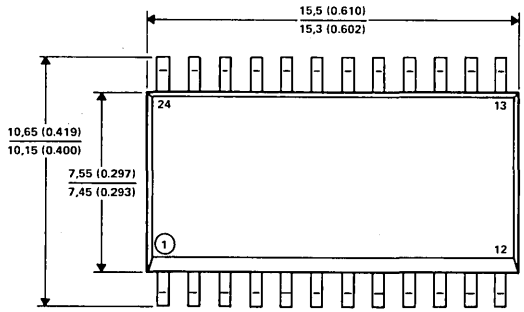
NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

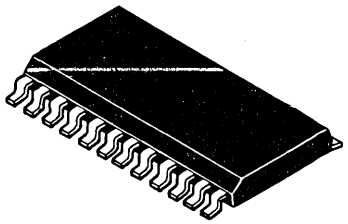
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

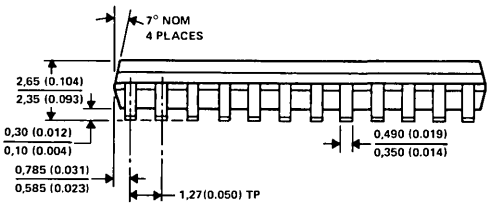
TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

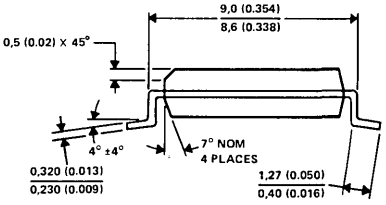
DW plastic "small outline" packages

24-PIN DW





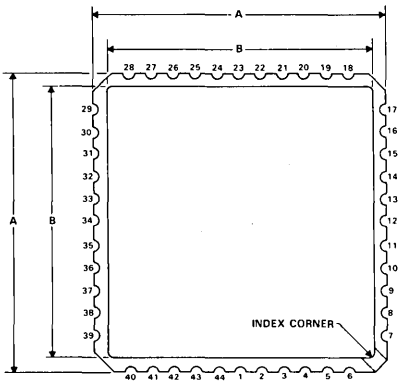




NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

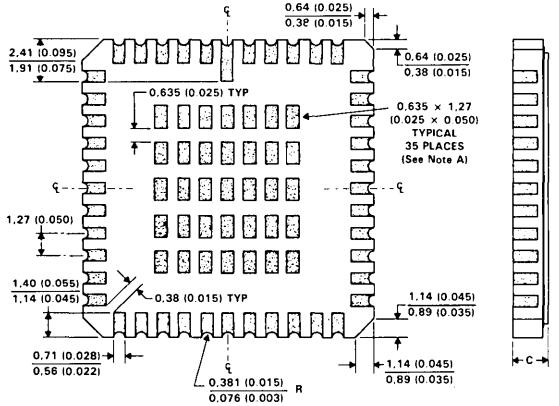
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

44-TERMINAL FD and FK



FD AND FK PACKAGES

NO. OF TERMINALS	A MIN	A MAX	B MAX	C MIN	C MAX
20	8,69 (0.342)	9,09 (0.358)	9,09 (0.358)	1,63 (0.064)	2,03 (0.080)
28	11,23 (0.442)	11,63 (0.458)	11,63 (0.458)	1,63 (0.064)	2,03 (0.080)
44	16,26 (0.640)	16,76 (0.660)	14,22 (0.560)	1,75 (0.069)	3,05 (0.120)
52	18,78 (0.739)	19,33 (0.761)	14,22 (0.560)	2,08 (0.082)	3,05 (0.120)
68	23,83 (0.938)	24,43 (0.962)	21,89 (0.862)	2,08 (0.082)	3,05 (0.120)
84	28,83 (1.135)	29,59 (1.165)	27,05 (1.065)	2,08 (0.082)	3,05 (0.120)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: The checkerboard pattern is aligned vertically with the contact pads and is symmetrical horizontally as shown; it is applicable to some 44-terminal packages only.

TEXAS INSTRUMENTS
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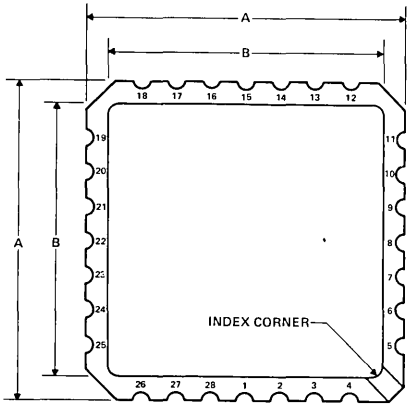
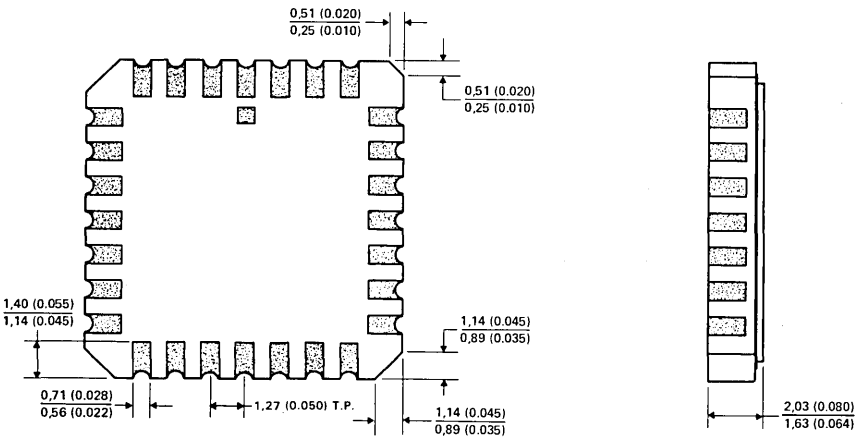
FK CERAMIC CHIP CARRIER
(28-terminal package shown)



CERAMIC CHIP CARRIERS

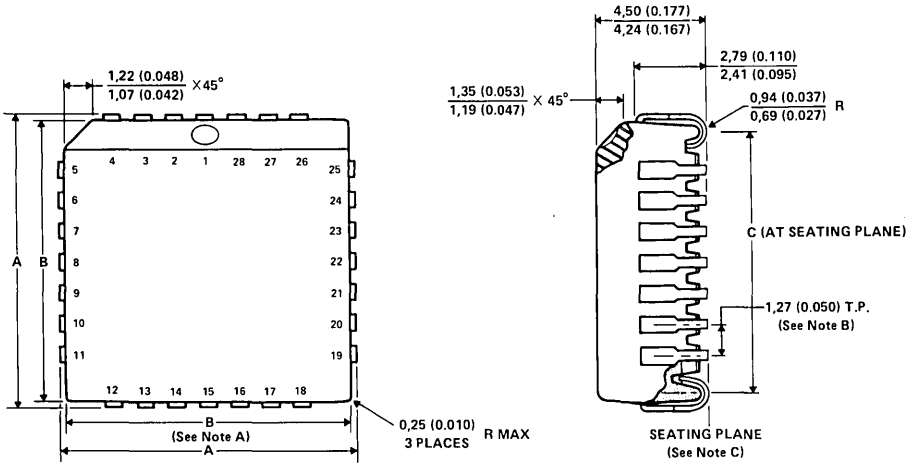
JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)

*All dimensions and notes for the specified JEDEC outline apply.

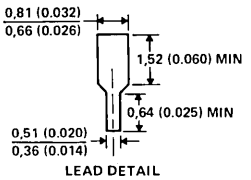


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

FN PLASTIC CHIP CARRIER
(28-terminal package used for illustration)



JEDEC OUTLINE	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
MO-047AA	20	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,87 (0.310)	8,38 (0.330)
MO-047AB	28	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,41 (0.410)	10,92 (0.430)
MO-047AC	44	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,49 (0.610)	16,00 (0.630)
MO-047AE	68	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.956)	23,11 (0.910)	23,62 (0.930)



All dimensions and notes for the specified JEDEC outline apply.

NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar within 0,10 (0.004).

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

TEXAS INSTRUMENTS
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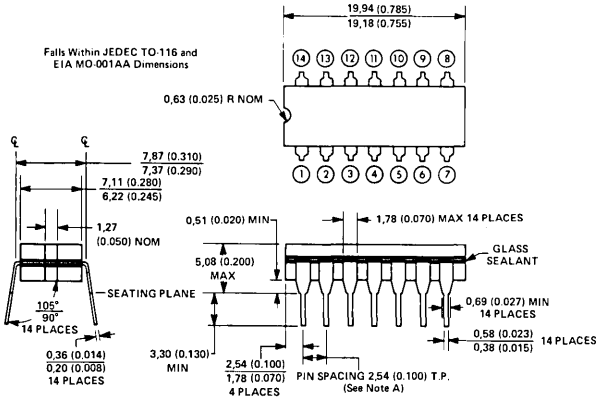
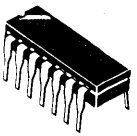
NOTE: For the 14-, 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing. For the 24-pin packages, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

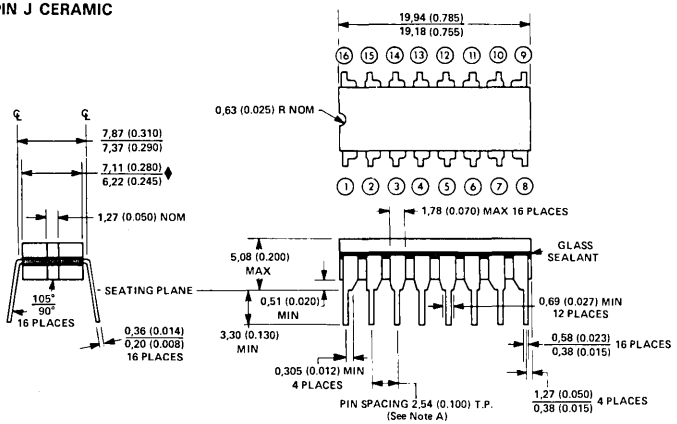
14-PIN J CERAMIC

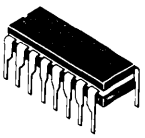




ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

16-PIN J CERAMIC





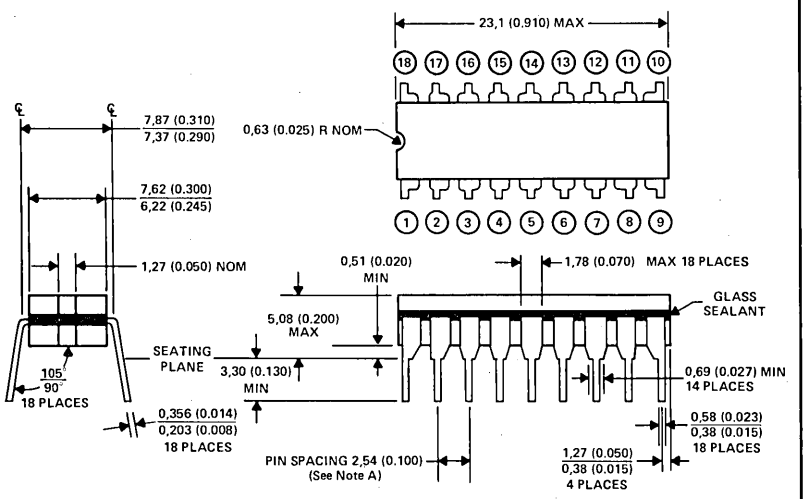
♦ For memories of 64 bits and up and a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, this maximum is 7,62 (0.300). All other dimensions apply without modification.

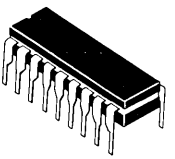
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line packages (continued)

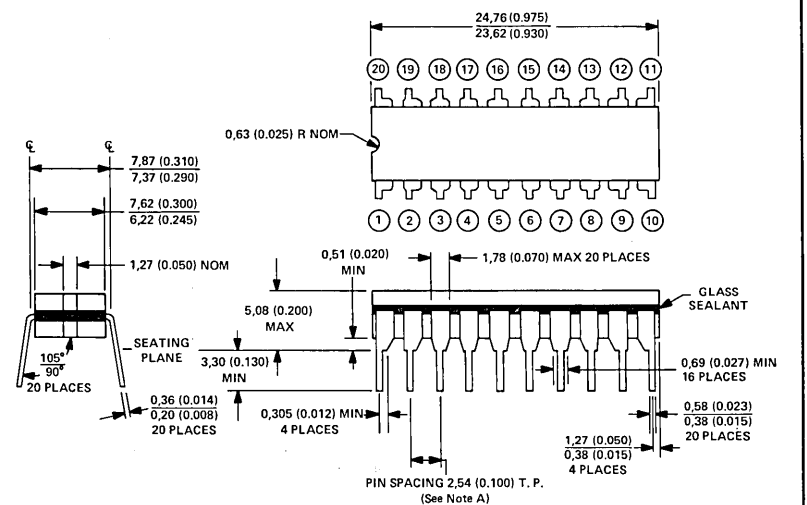
18-PIN J CERAMIC

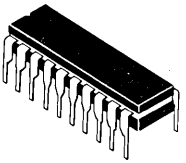




ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

20-PIN J CERAMIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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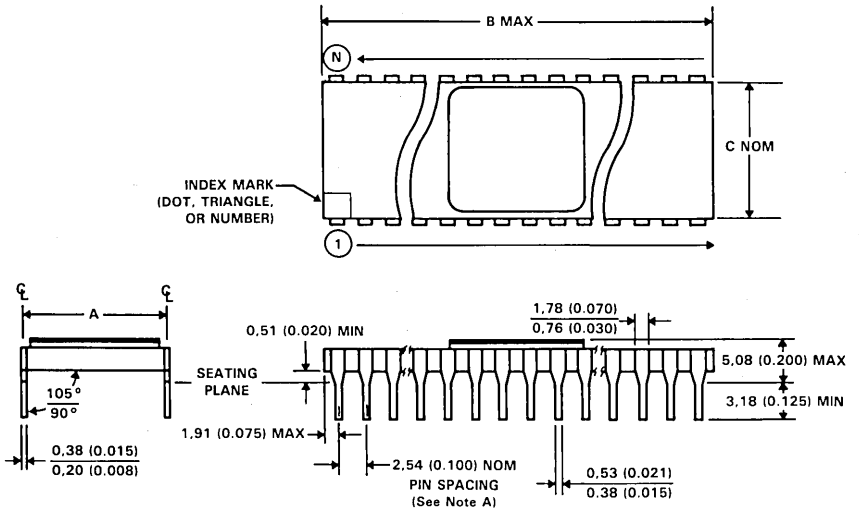
J ceramic dual-in-line packages (continued)

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

JD CERAMIC–SIDE BRAZE



DIM \ PINS (N)	16	18	20	22	24
A +0,51 (+0.020) −0,25 (−0.010)	7,62 (0.300)	7,62 (0.300)	7,62 (0.300)	7,62 (0.300)	7,62 (0.300)
B (MAX)	20,57 (0.810)	23,11 (0.910)	25,65 (1.010)	27,94 (1.100)	30,86 (1.215)
C (NOM)	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)	9,91 (0.390)	7,37 (0.290)

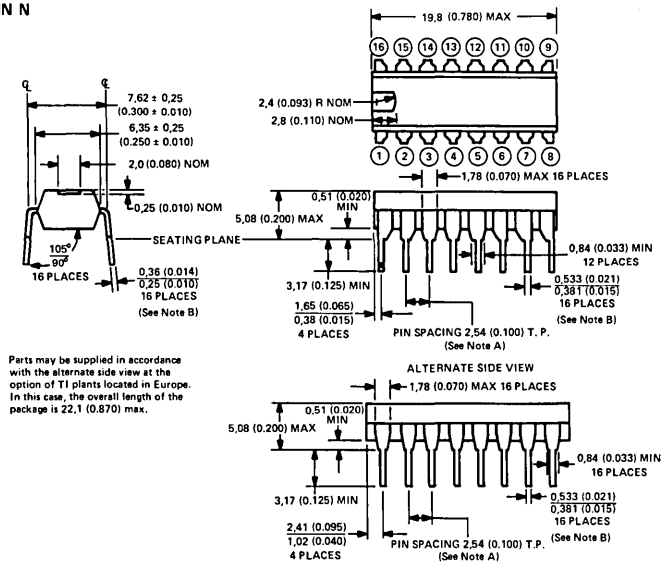
DIM \ PINS (N)	24	28	40	48	52	64
A +0,51 (+0.020) −0,25 (−0.010)	15,24 (0,600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B (MAX)	31,8 (1.250)	36,8 (1,450)	52,1 (2.050)	62,2 (2.450)	67,3 (2.650)	82,6 (3.250)
C (NOM)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	22,6 (0.890)

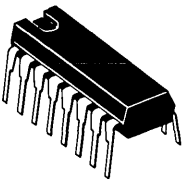
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

N plastic dual-in-line packages

16-PIN N

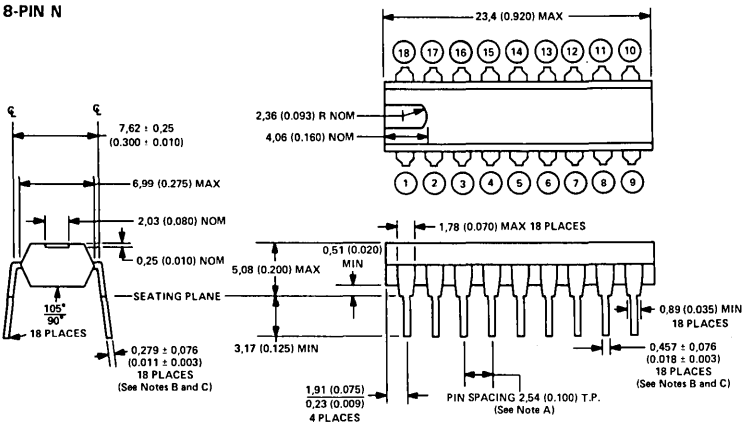


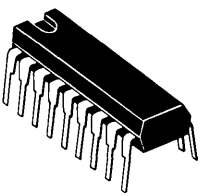


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

18-PIN N





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located with 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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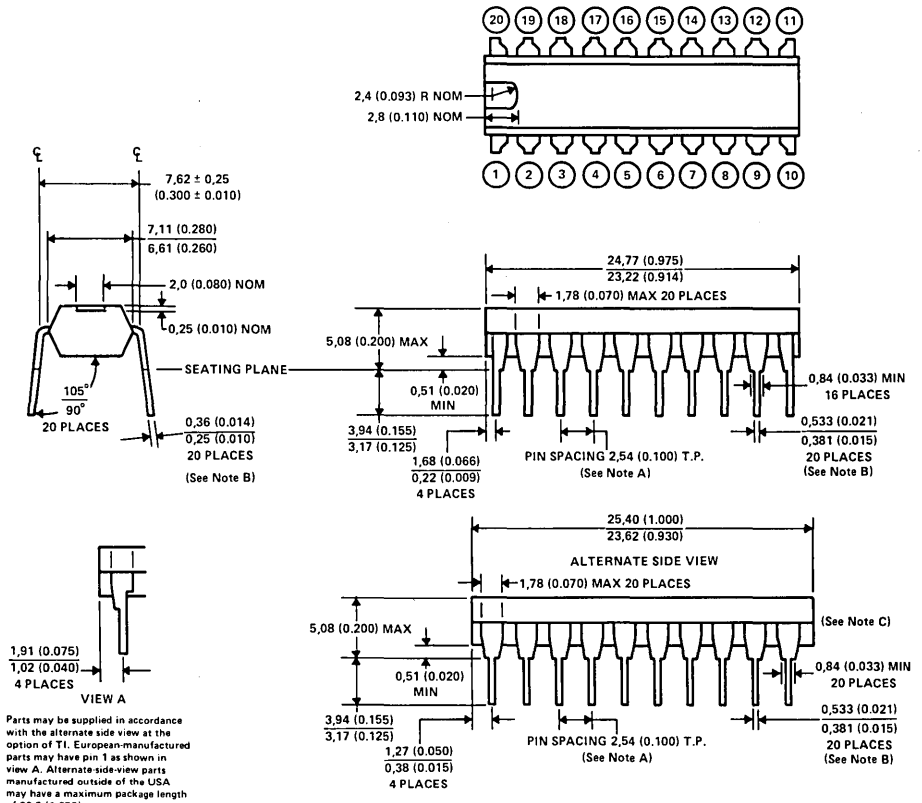
N plastic dual-in-line packages (continued)

20-PIN N

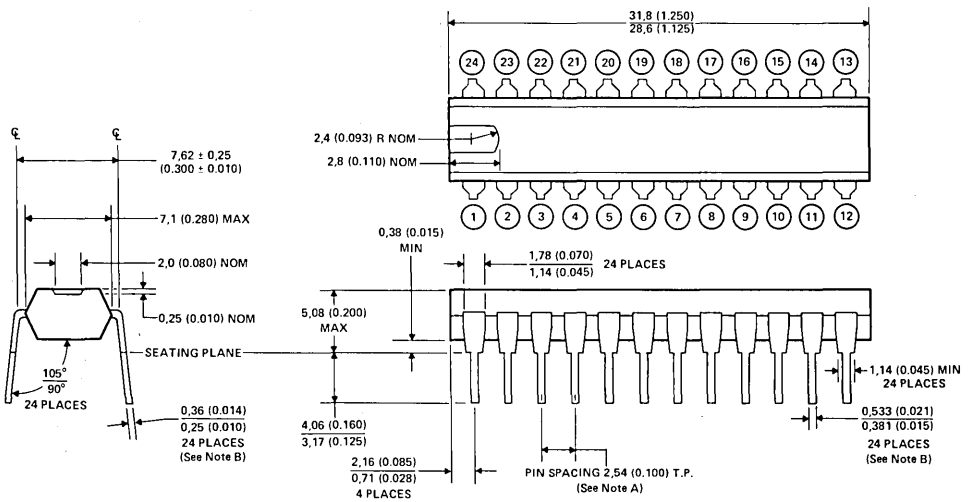


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.
C. Parts may be supplied with a draft angle of 7° typical at the option of TI.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

N plastic dual-in-line packages (continued)

24-PIN NT PLASTIC



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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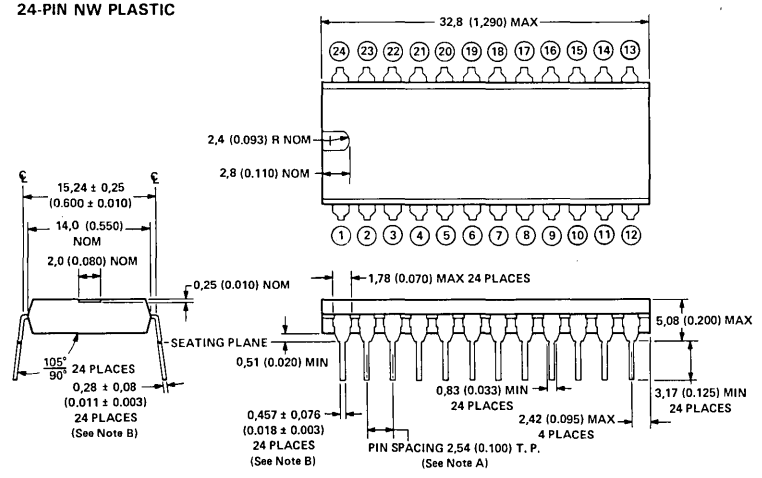
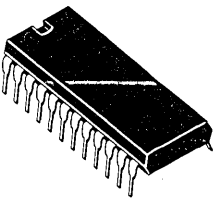
N plastic dual-in-line packages (continued)

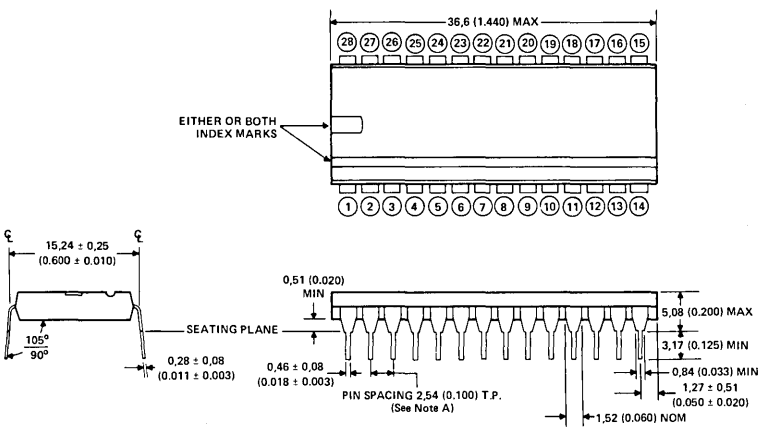
24-PIN NW PLASTIC

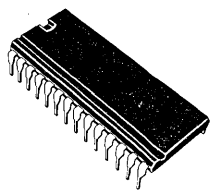




ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

28-PIN N PLASTIC



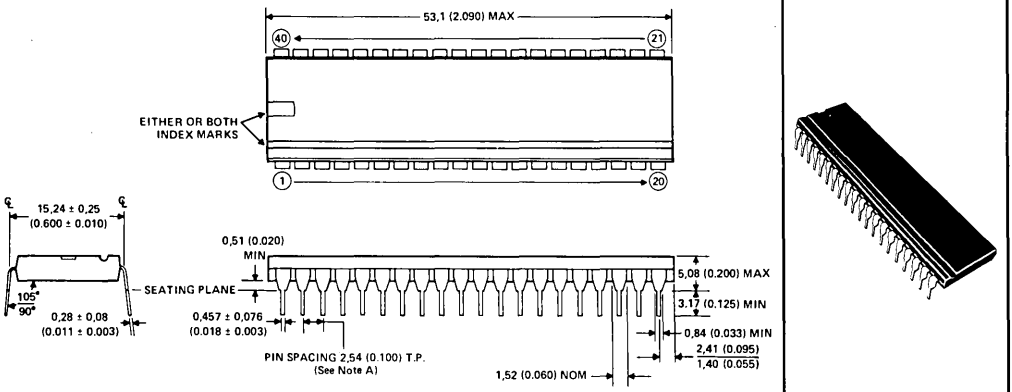


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

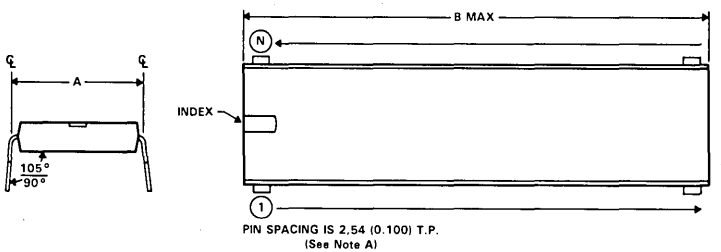
N plastic dual-in-line packages (continued)

40-PIN N PLASTIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

48-PIN, 52-PIN, AND 64-PIN N PLASTIC



DIM \ PINS (N)	48	52	64
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B MAX	62,2 (2.45)	67,3 (2.65)	81,3 (3.20)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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INTRODUCTION

Texas Instruments has developed solutions for today's high density packaging needs. The TI facility at Attleboro, Massachusetts (one of the world's largest suppliers of multimetal systems) provides leading-edge technology which, combined with reliable, high-volume, off-the-shelf interconnection products, allows TI to quickly meet volume commercial applications.

During the last decade, TI has produced one of the largest IC socket families. TI's sockets include every type and size socket in common use today and are available in a wide choice of contact materials and designs.

Our sockets are designed for:

- easy and efficient hand assembly
- compatibility with automatic assembly equipment
- maximum performance and board density

This section provides information on the following types of IC socket products.

PRODUCTION SOCKETS	TYPE
Plastic Leaded Chip Carrier	PLCC
Single-in-Line Packages	SIP
Pin-Grid Arrays	PGA
Dual In-Line	DIP
Dual In-Line 0.070-inch spacing	Shrink Pack
Quad In-Line	QUIP

BURN-IN/TEST SOCKETS	TYPE
Plastic Leaded Chip Carrier	PLCC
Pin Grid Array	PGA
Small Outline	J Lead
Dual In-Line	DIP
Dual In-Line 0.070-inch spacing	Shrink Pack
Small Outline	Flat Pack
Quad	Flat Pack

Specially formulated alloys give the TI contact springs:

- Low Contact Resistance
- High Contact Strength (to stand up to repetitive insertions and withdrawals)
- High normal forces assure gas-tight reliability

A full line of reliable, readily available, low-cost interconnection systems means premium performance at an economical price.

Additional information on these and other TI products, including pricing and delivery quotations, may be obtained from your nearest authorized TI Distributor, TI Sales Representative or:

Texas Instruments Incorporated
Connector Systems Department, MS 14-3 Telephone: (617) 699-5242/5375
Attleboro, Massachusetts 02703 TELEX: 92-7708

MECHANICAL DATA
IC SOCKETS
PLASTIC LEADED CHIP CARRIER

PERFORMANCE SPECIFICATIONS

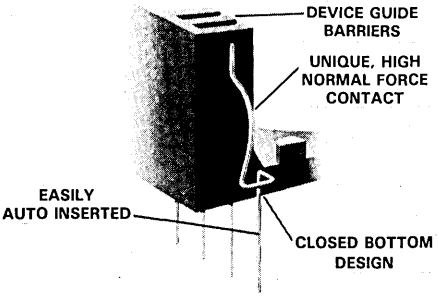
Mechanical
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Vibration: 15 G max
Shock: 100 G max
Insertion force: 0.59 lbs per position typ
Withdrawal force: 0.25 lbs per position typ
Normal force: 200 g min, 450 g typ
Wipe: 0.075 in min
Durability: 5 cycles min
Contact retention: 1.5 lbs min

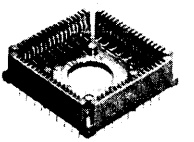
Electrical
Current carrying capacity: 1 A per contact
Insulation resistance: 5000 MΩ min
Dielectric withstanding voltage: 1000 V ac rms min
Capacitance: 1 pF max

Environmental
Operating temperature:
Operating: – 40°C to 85°C
Storage: –40°C to 95°C
Temperature cycling with humidity: will conform to final EIA specifications

MATERIALS
Body — Ryton R-4 (40% glass) UL 94 V-0 rating
Contacts — CDA 510 spring temper
Contact finish — 90/10 tin/lead (200 μin –400 μin) over 40 μin copper

Extraction tool available, consult factory
Contact factory for detailed information



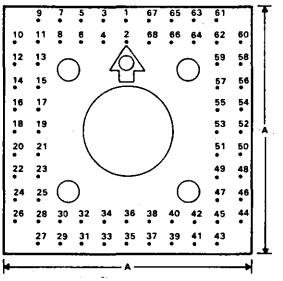


PART NUMBER SYSTEM

CPR PH XXX – X – X – O

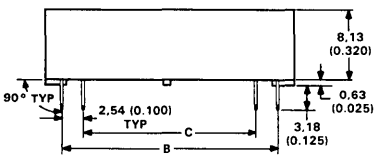
- O — Contact surface 1 – tin/lead plating
- X — Contact spacing 1 - 0.050 in
- XXX — Number of pos (044, 052, 068, 084)
- PH — Plated thru hole, solder tail
- CPR — TI socket Series
  Plastic leaded chip carrier

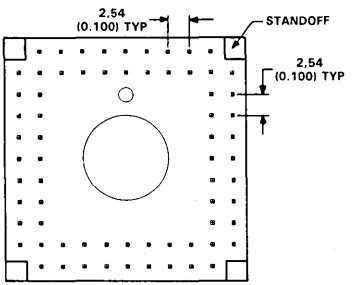
PLASTIC LEADED CHIP CARRIER CPR SERIES



68-Pin shown

NOTE: Socket electrical pin-out pattern represents component side of P.C.B. layout. (TYP. counter clockwise numbering pin-out system.)





Pos	A	B	C
44	21,43 (0.844)	17,78 (0.700)	12,70 (0.500)
52	23,98 (0.944)	20,32 (0.800)	15,24 (0.600)
68	29,06 (1.144)	25,40 (1.000)	20,32 (0.800)
84	34,14 (1.344)	30,48 (1.200)	25,40 (1.000)

Dimensions in parentheses are in inches

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PRODUCT FEATURES

Can be loaded by top actuated insertion or press-in insertion, either manually or automatically
High reliability due to high pressure contact point
Open body and high stand-off design provide high efficiency in heat dissipation
High durability up to 10,000 cycles
Compact design

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 10,000 cycles 10 mΩ max contact resistance change
Insertion force: Zero g
Withdrawal force: Zero g†

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ per MIL-STD 202, Method 302, Condition B
Dielectric withstanding voltage: 500 V ac rms per MIL-STD 202, Method 301

Environmental

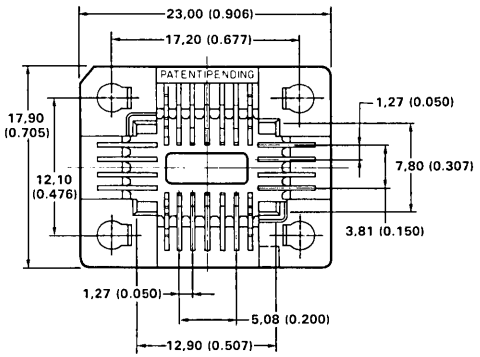
Thermal shock: 100 cycles, −25°C to +150°C
Temperature soak: 150°C for 48 hours
Operating temperature: −40°C to +150°C

MATERIALS

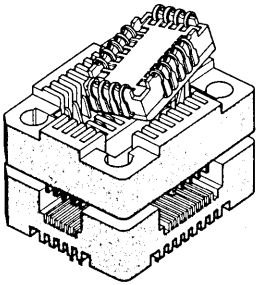
Body — ULTEM glass filled (UL 94 V-0)
Contact — copper alloy
Plating‡ — overall gold plate 4 μin over min 70 μin nickel plating

†After IC is unlocked from the socket
‡For additional plating options contact factory
For complete test report contact the factory

PLCC BURN-IN/TEST SOCKETS CPJ SERIES



Dimensions in parentheses are inches
Contact factory for detailed information

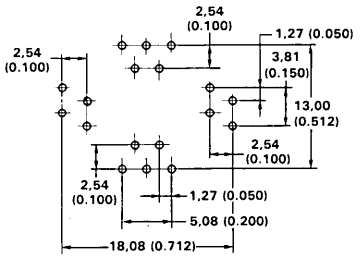


PART NUMBER SYSTEM

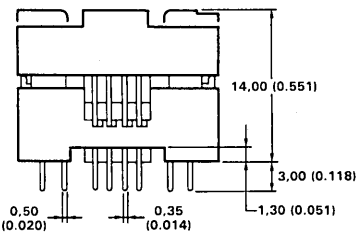
CPJ XX XX X – XXX – B

- CPJ: TI Burn-in PLCC series
- XX: Material — AA = copper alloy
- XX: Contact finish — 33 = overall gold plate
- X: Pitch — A = 0.050
- XXX: Number of contacts
- B

18 PIN FOOTPRINT SHOWN



SIZES: 18 PIN
22 PIN



PERFORMANCE SPECIFICATIONS†

Mechanical

Vibration: MIL-STD-202
Durability: 30 cycles
Insertion force: Zero g
Withdrawal force: Zero g‡
Contact (normal) force: 200 g min
Contact retention force: 2 lbs per circuit min

Electrical

Contact rating: 1 A
Contact resistance: 30 mΩ max initial
Insulation resistance: 1000 MΩ at 500 dc
Dielectric strength: 1500 V ac rms
Capacitance: 2 pF max

†Values may vary due to test sequence and SIP module configuration
‡After module is unlocked from the receptacle
For a complete test report, please contact factory

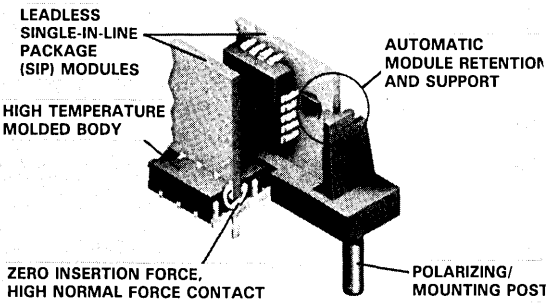
Environmental

(20 mΩ max contact resistance change after all tests)
Operating and storage temperature: −40°C to 100°C
Humidity: MIL-STD 202, Method 106D, 10 days
Temperature soak: 85°C for 160 hours
Thermal Shock: 5 cycles, −40°C to 85°C per MIL-STD 202, Method 107E

MATERIALS

Body — PES polyether sulfone, glass filled, UL 94 V-0
Contact — Beryllium copper C17000; phosphor bronze alloy CA510
Contact finishes — Post plate min 200 μin tin/lead over min 50μin nickel overall
Post plate min 30 μin hard gold over min 75 μin nickel overall

For additional plating options contact the factory.



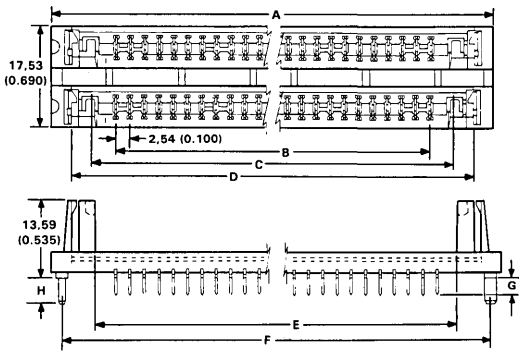
PART NUMBER SYSTEM

TS8X XX XX X −XX − XX

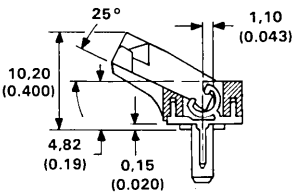
- XX (last): Variations — 00 — standard product
- −XX: Size (number of contacts per row)
- X: Housing material — A — PES
- XX: Contact base material/plating
  - 01—C17000/30 μin gold
  - 02—CA510/30 μin gold
  - 03—C17000/200 μin tin/lead
  - 04—CA510/200 μin tin/lead
- XX: Configuration/row-to-row spacing
  - 01—single row/N/A
  - 03—dual row/0.300 in
  - 04—dual row/0.400 in
  - 05—dual row/0.500 in
- TS8X: Series number denotes
  - 0—0.100 in pitch, vertical mount
  - 1—0.100 in pitch, low-profile (25°) mount

Consult factory for availability of configurations, materials, and sizes.

DUAL ROW VERTICAL



SINGLE ROW LOW PROFILE



Ckt. Size	A	B	C	D	E	F	G	H
30	96,52 (3.800)	73,66 (2.900)	82,14 (3.234)	89,28 (3.515)	80,52 (3.170)	92,71 (3.650)	2,79 (0.110)	3,86 (0.152)

Contact factory for detailed information

Dimensions in parentheses are in inches

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.015 in to 0.021 in diameter
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Recommended hole grid pattern: 0.100 in ± 0.002 in each direction
Vibration: 15 G, 10-2000 Hz per MIL-STD 1344A, Method 2005.1 Test Condition III
Shock: 100 G, sawtooth waveform, 2 shocks each direction per MIL-STD 202, Method 213, Test Condition I
Durability: 5 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016
Insertion force: 3.6 oz (102 g) per pin typ using 0.018 in diameter test pin
Withdrawal force: 0.5 oz (14 g) per pin min using 0.018 in diameter test pin

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc per MIL-STD 1344, Method 3003.1
Dielectric withstanding voltage: 1000 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

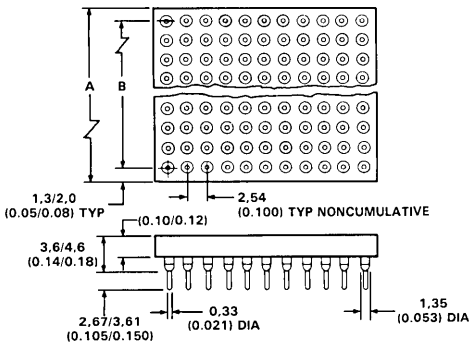
Environmental

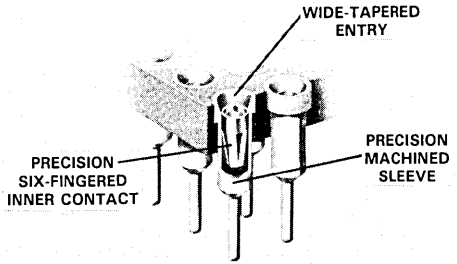
Operating temperature: −65°C to 125°C, gold; −40°C to 100°C, tin/lead
Corrosive atmosphere: 10 mΩ max contact resistance change when exposed to 22% ammonium sulfide for 4 hours
Gas tight: 10 mΩ max contact resistance change when exposed to nitric acid vapor for 1 hour
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

MATERIALS

Body — PBT polyester UL 94 V-0
On request, G10/FR4 or Mylar film
Outer sleeve — Machined Brass (QQ-B-626)
Inner contact — Beryllium copper (QQ-C-530) heat treated
Plating: (specified by part number)

PIN GRID ARRAY





Inner contact — 30 μin gold over 50 μin nickel or 100 μin tin/lead over 50 μin nickel
Outer sleeve — 10 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel

PART NUMBER SYSTEM

C X G XX – XXX X X – X X

Pin Length

WIRE WRAP	SOLDER TAIL
3-0.510 long	9-0.105/0.150

Plating

P/N	Sleeve	Clip
0	Gold	Gold
5	Tin	Gold

Body Style and Orientation
Contact Loading Pattern
Number of Pins 024 to 324
Overall Grid Size 5×5=05 to 18×18=18
Pin Grid Array
BODY MATERIAL
G — Glass Filled Epoxy
P — PBT Polyester
TI Socket

Insulator Size	A ±0.010	B ±0.005†
9×9	(0.950) 24,13	(0.800) 20,32
10×10	(1.050) 26,67	(0.900) 22,86
11×11	(1.150) 29,21	(1.000) 25,40
12×12	(1.250) 31,75	(1.100) 27,94
13×13	(1.350) 34,29	(1.200) 30,48
14×14	(1.450) 36,83	(1.300) 33,02
15×15	(1.550) 39,37	(1.400) 35,56
16×16	(1.650) 41,91	(1.500) 38,10
17×17	(1.750) 44,45	(1.600) 40,64
18×18	(1.850) 46,99	(1.700) 43,18

†Noncumulative
Dimensions in parentheses are inches
Consult factory for detailed information

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 10,000 cycles, 20 mΩ max contact resistance change
Insertion force: 1.3 oz per position max
Withdrawal force: 8.8 grams per position min

Electrical

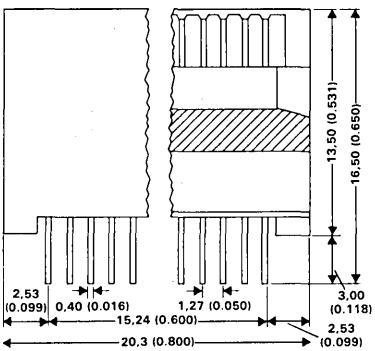
Contact rating: 1.0 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ per MIL-STD 202, Method 302, Condition B
Dielectric withstanding voltage: 700 V ac rms per MIL-STD 202, Method 301

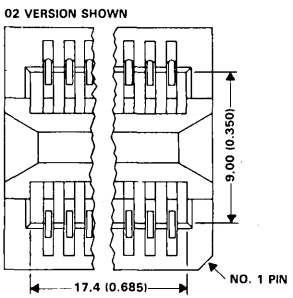
Environmental

Thermal shock: 100 cycles, −25°C to +180°C, 1 hour
Temperature soak: 180°C for 1000 hours, 80 mΩ max change
Operating temperature: −65°C to +180°C

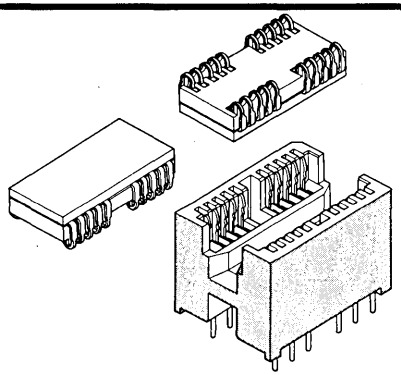
MATERIALS

Body — PES glass filled UL 94 V-0
Contact — copper alloy
Plating — overall gold plate min 4 μin over min 70 μin nickel plating





Dimensions in parentheses are inches
Contact factory for detailed information



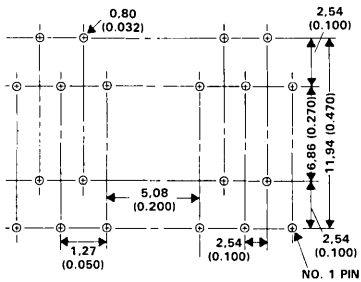
PART NUMBER SYSTEM

CSJT XXX – XX – XX X

- CSJT — TI SOJ series
- XXX — Number of Contacts
- XX — Contact Finish
  - 37 = Overall gold plate 4 μin
  - 38 = Overall gold plate 30 μin
  - 57 = Selective gold plate 4 μin
  - 58 = Selective gold plate 30 μin
- XX — Body Variation
  - 02 = Standard 1 forward/backward insertion
  - 03 = Special/orientation pin
  - 04 = Special/high standoff
  - 05 = Special/24-pin
  - 06 = Standard 2 forward insertion, BECU
- X — Body Material
  - Blank = G.F. PES
  - A = PPS R4-03
  - B = G.F. PEI

SIZES: 20 pin
26 pin

20-PIN (02 VERSION) FOOTPRINT SHOWN



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.011 ± 0.003 in by 0.018 ± 0.003
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Recommended hole grid pattern: 0.100 in ± 0.003 in each direction
Vibration: 15 G, 10-2000 Hz per MIL-STD 1344A, Method 2005.1 Test Condition III.
Shock: 100 G, sawtooth waveform, 2 shocks each direction per MIL-STD 202, Method 213, Test Condition I
Durability: 5 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016
Insertion force (C7X and C86): 16 oz (454 g) per pin max
Withdrawal force: (40 g) per pin min

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc per MIL-STD 1344, Method 3003
Dielectric withstanding voltage: 1000 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

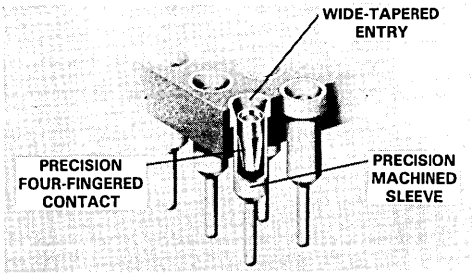
Environmental

Operating temperature: −55°C to 125°C, gold; −40°C to 100°C, tin
Corrosive atmosphere: 10 mΩ max contact resistance change when exposed to 22% ammonium sulfide for 4 hours
Gas tight: 10 mΩ max contact resistance change when exposed to nitric acid vapor for 1 hour
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

Materials (C7X and C86)

Body — PBT polyester UL 94 V-0
C7X Contacts — Outer sleeve: brass
Clip: BECU
Contact finish — clip 30 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel
Specified by Part Number — sleeve 10 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel
C86 Contacts — Phosphor bronze base metal
C86 Contact-finish — Tin plate 200 μin over copper flash

C7X SERIES — SCREW MACHINE

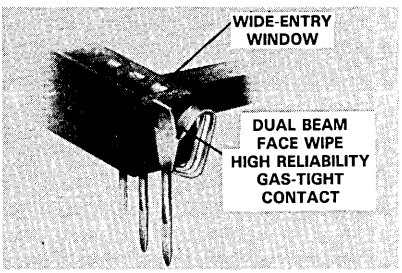


C7X SERIES — SCREW MACHINE PART NUMBER SYSTEM

C7X (X) XX – X X

- X (last): Variations
  - Solder Tail : 9
    Pin length 0.125 Typ
  - Wire Wrap : 3
    Pin length 0.510
- X: Plating (Sleeve/Clip)
  - 0 — Gold/Gold
  - 5 — Tin/Gold
- XX: Number of Positions
- (X): S — Single-in-line package (where applicable)
- C7X: Screw Machine Socket
  - 1 — wire wrap
  - 2 — solder tail

C86 SERIES — STAMPED AND FORMED

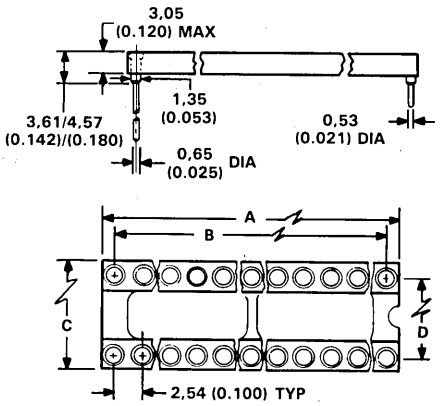


C86 SERIES PART NUMBER SYSTEM

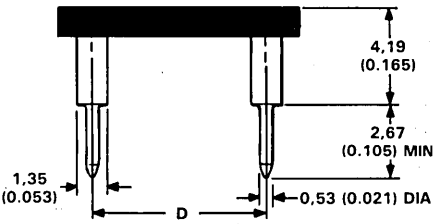
C 86 XX – 01

- 01: Variation
  - 01 — Standard product
- XX: Number of positions
- 86: Tin Dual Beam Face Wipe
- C: TI Socket Series

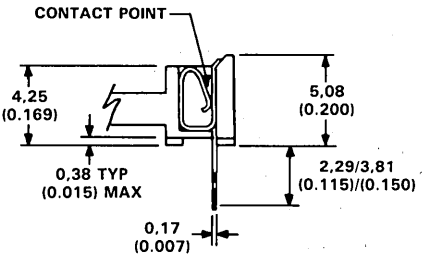
DUAL-IN-LINE
C7X AND C86 SERIES



C7X SERIES



C86 SERIES



DIPS

Positions	Dim A Max	Dim B ±0.005	Dim C Max	Dim D ±0.005	Positions	Dim A Max	Dim B ±0.005	Dim C Max	Dim D ±0.005
6	7,62 (0.300)	5,08 (0.200)	10,16 (0.400)	7,62 (0.300)	†24	30,48 (1.200)	27,94 (1.100)	12,76 (0.500)	10,16 (0.400)
8	10,16 (0.400)	7,62 (0.300)	10,16 (0.400)	7,62 (0.300)	28	35,56 (1.400)	33,02 (1.300)	17,78 (0.700)	15,24 (0.600)
14	17,78 (0.700)	15,24 (0.600)	10,16 (0.400)	7,62 (0.300)	32	40,64 (1.600)	38,10 (1.500)	17,78 (0.700)	15,24 (0.600)
16	20,32 (0.800)	17,78 (0.700)	10,16 (0.400)	7,62 (0.300)	34	45,72 (1.800)	43,18 (1.700)	17,78 (0.700)	15,24 (0.600)
18	22,86 (0.900)	20,32 (0.800)	10,16 (0.400)	7,62 (0.300)	40	50,80 (2.000)	48,26 (1.900)	17,78 (0.700)	15,24 (0.600)
20	25,40 (1.000)	22,86 (0.900)	10,16 (0.400)	7,62 (0.300)	48	60,96 (2.400)	58,42 (2.300)	17,78 (0.700)	15,24 (0.600)
22	27,94 (1.100)	25,40 (1.000)	12,76 (0.500)	10,16 (0.400)	50	63,50 (2.500)	60,96 (2.400)	25,40 (1.000)	7,62 (0.900)
24	30,48 (1.200)	27,94 (1.100)	17,78 (0.700)	15,24 (0.600)	64	81,28 (3.200)	78,74 (3.100)	25,40 (1.000)	22,86 (0.900)
†24	30,48 (1.200)	27,94 (1.100)	10,16 (0.400)	7,62 (0.300)					

†Nonstandard sizes
Not all sizes available in each series
Dimensions apply to all series

Dimensions in parentheses are inches
Contact factory for detailed information

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.011 in by 0.018 in
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hold size range: 0.032 in to 0.042 in
Durability: 10K cycles — CM Series, 5K cycles — CP/CQ

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc
Dielectric withstanding voltage: 1000 V ac rms
Capacitance: 1 pF max per MIL-STD 202, Method 305

Environmental

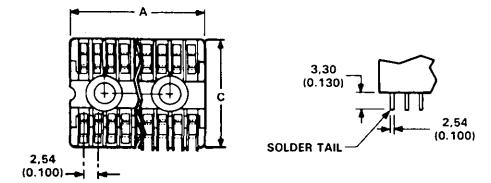
Operating temperature: −65°C to 170°C — CP/CM Series,
−65°C to 150°C — CQ Series
Humidity: 10 mΩ max contact resistance
Temperature Soak: 10 mΩ max contact resistance change

MATERIALS

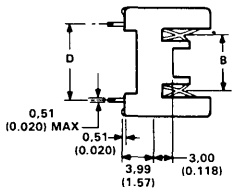
Body — PPS (polyphenylen sulfide) UL 94 V-0
Contacts — Higher performance copper nickel alloy
Plating:† 4 μin of gold min over 100 μin of nickel min

†For additional plating options consult the factory

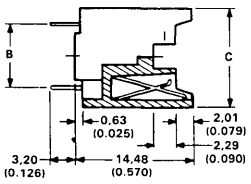
BURN-IN/TEST DIP SOCKETS



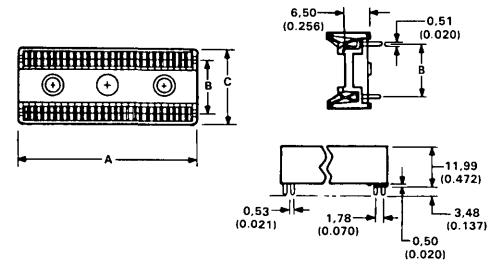
CQ37 SERIES



CP37 SERIES



CM37 SERIES



PART NUMBER SYSTEM

C X 37 XX − 22 S X

- C — TI Socket Series
- X — Series Features: Q — Auto unloadable; P — High density mounting; M — Shrink 0.070 centers
- 37 — Overall gold plate
- XX — Number of positions
- 22 — Copper nickel alloy Soldertail
- S — PPS high temperature body material
- X — Pin to pin: A — 0.100 centers; B — 0.070 centers

CQ37 SERIES

Number of Positions	A ±0.01 Length	D ±0.02	C ±0.01 Width	B ±0.01 Contact
14	20,32 (0.800)			
16	22,35 (0.880)	12,70	15,24	7,62
18	24,89 (0.980)	(0.500)	(0.600)	(0.300)
20	27,43 (1.080)			
24	32,51 (1,280)			
28	37,59 (1.480)	19,05	22,86	15,24
40	52,83 (2.080)	(0.750)	(0.900)	(0.600)
42	55,37 (2.180)			

CP37 SERIES

Number of Positions	A max Length	B ±0.02	C max Width
8	11,68 (0.460)		
14	17,78 (0.700)		
16	20,32 (0.800)	7,62	12,70
18	22,86 (0.900)	(0.300)	(0.500)
20	25,40 (1.000)		
24	30,48 (1.200)		
28	35,56 (1.400)	15,24	20,32
40	50,80 (2.000)	(0.600)	(0.800)

CM37 SERIES

Number of Positions	A ±0.016 Length	B ±0.02	C ±0.016 Width
28	27,18 (1.070)	10,67 (0.420)	17,20 (0.677)
40	37,85 (1.490)		
42	39,62 (1.560)	16,51	23,11
54	50,29 (1.980)	(0.650)	(0.910)
64	59,18 (2.330)	20,32 (0.800)	26,92 (1.060)

Dimensions in parentheses are inches
Contact factory for detailed information

For more information contact your local distributor or contact TI directly:

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Phone: 011-49-89-915081

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

Guidelines for Handling Electrostatic-Discharge Sensitive (ESDS) Devices and Assemblies

SCOPE

This specification establishes the requirements for methods and materials used to protect electronic parts, devices, and assemblies (items) susceptible to damage or degradation from electrostatic discharge (ESD). The electrostatic charges referred to in this specification are generated and stored on surfaces of ordinary plastics, most common textile garments, ungrounded people's bodies, and many other commonly unnoticed static generators. The passage of these charges through an electrostatic-sensitive part may result in catastrophic failure or performance degradation of the part.

The part types for which these requirements are applicable include, but are not limited to, those listed:

1) All metal-oxide semiconductor (MOS) devices, e.g., CMOS, PMOS, etc.
2) Junction field-effect transistors (JFET)
3) Bipolar digital and linear circuits
4) Op Amps, monolithic microcircuits with MOS compensating networks, on-board MOS capacitors, or other MOS elements
5) Hybrid microcircuits and assemblies containing any of the types of devices listed
6) Printed circuit boards and any other type of assembly containing static-sensitive devices.

Definitions

1. Antistatic material: ESD protective material having a surface resistivity between 10^9 and 10^{14} Ω/square.
2. Static dissipative material: ESD protective material having surface resistivity between 10^5 and 10^9 Ω/square.
3. Conductive material: ESD protective material having a surface resistivity of 10^5 Ω/square maximum.
4. Electrostatic discharge (ESD): A transfer of electrostatic charge between bodies at different electrostatic potentials caused by direct contact or induced by an electrostatic field.
5. Surface resistivity: An inverse measure of the conductivity of a material and is the resistance of unit length and unit width of a surface. Note: Surface resistivity of a material is numerically equal to the surface resistance between two electrodes forming opposite sides of a square. The size of the square is immaterial. Surface resistivity applies to both surface and volume conductive materials and has the dimension of Ω/square.
6. Volume resistivity: Also referred to as bulk resistivity. It is normally determined by measuring the resistance (R) of a square of material (surface resistivity) and multiplying this value by the thickness (T).
7. Ionizer: A blower that generates positive and negative ions, either by electrostatic means or by means of a radioactive energy source, in an airstream, and distributes a layer of low velocity ionized air over a work area to neutralize static charges.
8. Close proximity: For the purpose of this specification, is 6 inches or less.

Device Sensitivity per Test Circuit of Method 3015, MIL-STD-883

Devices are categorized according to their susceptibility to damage resulting from electrostatic discharge (ESD), and the type packaging required to adequately protect them.

1) Device electrostatic sensitivity:

Category	ESD Sensitivity (V)	Minimum Protective Packaging
A	20-2000	Antistatic Magazine & Conductive Bag/Box
B	> 2000	Antistatic Magazine & Antistatic Bag

2) Devices are to be categorized by their sensitivity
3) Devices are to be protected from ESD damage from receipt at incoming inspection through assembly, test and shipment of completed equipment.

APPLICABLE REFERENCE DOCUMENTS

The following reference documents (of latest issue) can provide additional information on ESD controls.

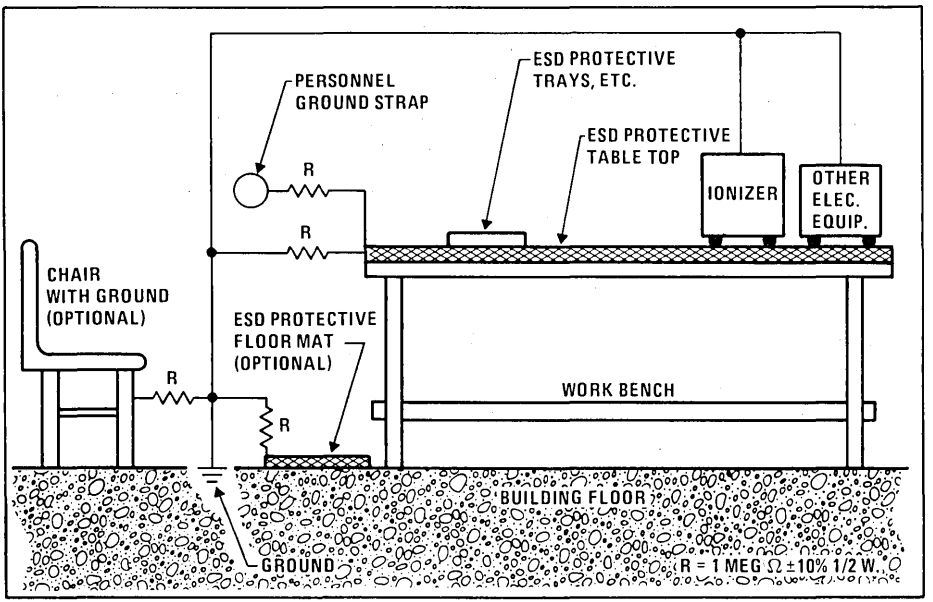
1) MIL-M-38510 Microcircuits, General Specification
2) MIL-STD-883 Test Methods and Procedures for Microelectronics
3) MIL-S-19491 Semiconductor Devices, Packaging of
4) MIL-M-55565 Microcircuits, Packaging of
5) DOD-HDBK-263 Electrostatic Discharge Control Handbook for Protection
6) DOD-STD-1686 Electrostatic Discharge Control Program
7) NAVSEA SE 003-11-TRN-010 Electrostatic Discharge Training Manual

FACILITIES FOR STATIC-FREE WORK STATION

The minimum acceptable static-free work station shall consist of the work surface covered with an ESD protective material attached to ground through a 1 MΩ ±10% resistor, an attached grounding wrist strap with integral 1 MΩ ±10% resistor for each operator, and air ionizer(s) of sufficient capacity for each operator. The wrist strap shall be connected to the ESD protective material. Ground shall utilize the standard building earth ground, refer to Figure 1. Conductive floor tile along with conductive shoes may be used in lieu of the conductive wrist straps. The Site Safety Engineer must review and approve all electrical connections at the static-free work station prior to its implementation.

Air ionizers shall be positioned so that the devices at the static-free work stations are within a 4-foot arc measured by a vertical line from the face of the ionizer and 45 degrees on each side of this line.

General grounding requirements are to be in accordance with Table 1.



All electrical equipment sitting on the conductive table top must be hard grounded but must be isolated from the conductive table top.

NOTE: Earth ground is not computer ground or RF ground or any other limited type ground.

Figure 1. Static-Free Work Station

Table 1. General Grounding Requirements

	TREATED WITH ANTISTATIC SOLUTION OR MADE OF CONDUCTIVE MATERIAL	GROUNDED TO COMMON POINT
Handling Equipment/Handtools	X	
Metal Parts of Fixtures and Tools/Storage Racks		X
Handling Trays/Tubes	X	
Soldering Irons/Bath		X
Table Tops/Floor Mats	X	X
Personnel		X Using Wrist Strap*

*With 1 MΩ ± 10% resistor

Usage of Antistatic Solution in Areas to Control the Generation of Static Charges

The use of antistatic chemicals (antistats) should be a supplemental part of an overall organized ESD program. Any antistatic chemical application shall be considered as a means to reduce or eliminate static charge generation on nonconductive materials in the manufacturing or storage areas.

The application of any antistatic chemical in a clean room of class 10,000 or less shall not be permitted. Accordingly, any user of antistatic solutions must consider the following precautions:

1. Do not apply antistatic spray or solutions in any form to energized electrical parts, assemblies, panels, or equipment.
2. Do not perform antistatic chemical applications in any area when bare chips, raw parts, packages, and/or personnel are exposed to spray mists and evaporation vapors.

The need for initial application and frequency of reapplication can only be established through routine electrostatic voltage measurements using an electrostatic voltmeter. The following durability schedule is a reasonable expectation.

1) Soft surfaces (carpet, fabric seats, foam padding, etc.): each 6 months or after cleaning, by spraying.
2) Hard abused surfaces (floors, table tops, tools, etc.): each week (or day for heavy use) and after cleaning, by wiping or mopping.
3) Hard unabused surfaces (cabinets, walls, fixtures, etc.): each 6 months or annually and after cleaning, by wiping or spraying.
4) Company-furnished and maintained clothing and smocks: after each cleaning, by spraying or adding antistatic concentrate to final rinse water when cleaned.

The use of antistatic chemicals, their application, and compliance with all appropriate specifications, precautions, and requirements shall be the responsibility of the Area Supervisor where antistatic chemicals are used.

ESD Labels and Signs in Work Areas

ESD caution signs at work stations and labels on static-sensitive parts and containers shall be consistent in color, symbols, class, and voltage sensitivity identification, and appropriate instructions. Signs shall be posted at all work stations performing any handling operations with static-sensitive items. These signs shall contain the following information.

> **CAUTION**
>
> **STATIC CAN DAMAGE COMPONENTS**
>
> Do not handle ESDS items unless grounding wrist strap is properly worn and grounded. Do not let clothing or plain plastic materials contact or come in close proximity to ESDS items.

Labels shall be affixed to all containers containing static-sensitive items at a place readily visible and proper for the intended purpose. Additionally, labels must be consistently placed on containers and packages at a standard location to eliminate mishandling. Use only QC accepted and approved signs and labels to identify static-sensitive products and work areas. The use of ESD signs and labels, and their information content shall be the responsibility of the Area Supervisor to assure consistency and compatibility throughout the static-sensitive routing.

Relative Humidity Control

Since relative humidity has a significant impact on the generation of static electricity, when possible, the work area should be maintained within the following relative humidity ranges: incoming/assembly/test/storage 50%-65% (ref. Ashrae, 55—74), within ±5% to avoid static voltage monitor variations.

PREPARATION FOR WORKING AT STATIC-FREE WORK STATION

A work station with a conductive work surface connected to ground through a 1 MΩ ± 10% resistor, a grounding wrist strap with the ground wire connected to the conductive work surface, and an ionizer constitute a static-free work station (Figure 42). An operator is properly grounded when the wrist strap is in snug (no slack) contact with the bare skin, usually positioned on the left wrist for a right-handed operator. The wrist strap must be worn the entire time an operator is at a static-free work station. The operator should first touch the grounded bench top before handling static-sensitive items. This precaution should be observed in addition to wearing the grouding wrist strap. If possible, operators should avoid touching leads or contacts even though grounded.

CAUTION

Personnel shall never be attached to ground without the presence of the 1 MΩ ±10% series resistor in the ground wire.

An operator's clothing should never make contact or come in close proximity with static sensitive items. They must be especially careful to prevent any static-sensitive items (being handled) from touching their clothing. Long sleeves must be rolled up or covered with antistatic sleeve protector banded to the bare wrist which shall "cage" the sleeve at least as far up as the elbow. Only antistatic finger cots may be used when handling static-sensitive items.

Any person not properly prepared, while at or near the work station, shall not touch or come in close proximity with any static-sensitive items. It is the responsibility of the operator and the Area Supervisor to ensure that the static-free work area is clear of unnecessary static hazards, including such personal items as plastic coated cups or wrappers, plastic cosmetic bottles or boxes, combs, tissue boxes, cigarette packages, and vinyl or plastic purses. All work-related items, including information sheets, fluid containers, tools, and parts carriers must be those approved for use at the static-free work station.

GENERAL HANDLING PROCEDURES AND REQUIREMENTS

1. All static-sensitive items must be received in an antistatic/conductive container and must not be removed from the container except at static-free work station. All protective folders or envelopes holding documentation (lot travelers, etc.) shall be made of nonstatic-generating material.
2. Each packing (outermost) container and package (internal or intermediate) shall have a bright yellow warning label attached, stating the following information or equivalent:

   The warning label shall be legible and easily readable to normal vision at a distance of 3 feet.
3. Static-sensitive items are to remain in their protective containers except when actually in work at the static-free station.
4. Before removing the items from their protective container, the operator should place the container on the conductive grounded bench top and make sure the wrist strap fits snugly around the wrist and is properly plugged into the ground receptacle, then touch hands to the conductive bench top.
5. All operations on the items should be performed with the items in contact with the grounded bench top as much as possible. Do not allow conductive magazine to touch hard grounded test gear on bench top.

6. Ordinary plastic solder-suckers and other plastic assembly aids shall not be used.
7. In cases where it is impossible or impractical to ground the operator with a wrist strap, a conductive shoe strap may be used along with conductive tile/mats.
8. When the operator moves from any other place to the static-free station, the start-up procedure shall be the same as in PREPARATION FOR WORKING AT STATIC-FREE WORK STATION.
9. The ionizer shall be in operation prior to presenting any static-sensitive items to the static-free station, and shall be in operation during the entire time period the items are at the station.
10. "Plastic snow" polystyrene foam, "peanuts," or other high-dielectric materials shall never come in contact with or be used around electrostatic sensitive items, unless they have been treated with an antistat (as evidenced by pink color and generation of less than ± 100 volts).
11. Static-sensitive items shall not be transported or stored in trays, tote boxes, vials, or similar containers made of untreated plastic material unless items are protectively packaged in conductive material.

PACKAGING REQUIREMENTS

Packaging of static-sensitive items is to be in accordance with Device Sensitivity, item 1). The use of tape and plain plastic bags is prohibited. All outer and inner containers are to be marked as outlined in GENERAL HANDLING PROCEDURES AND REQUIREMENTS, item 2, and conductive magazines/boxes may be used in lieu of conductive bags.

SPECIFIC HANDLING PROCEDURES FOR STATIC-SENSITIVE ITEMS

Stockroom Operations

1. Containers of static-sensitive items are not to be accepted into stock unless adequately identified as containing static-sensitive items.
2. Items may be removed from the protective container (magazine/bag, etc.) for the purpose of subdividing for order issue only by a properly grounded operator at an approved static-free station as defined in FACILITIES FOR and PREPARATION FOR WORKING AT STATIC-FREE WORK STATION.
3. All subdivided lots must be carefully repackaged in protective containers (magazine/bag, etc.) prior to removal from the static-free work station and labeled to indicate that the package(s) contain static-sensitive items. If it is suspected that a static-sensitive item is not adequately protected, do not transfer it to another container, return it to the originator for disposition unless the originator is a Customer. In that case, the QC Engineer should contact the Customer and negotiate an appropriate disposition.
4. It is the responsibility of the Stockroom Supervisor to ensure that all personnel assigned to this operation are familiar with handling procedures as outlined in this specification. A copy of this specification is to be posted in the vicinity so that it is accessible to the operators. Stock handlers and all others who might have occasion to move stock are to be instructed to avoid direct contact with unprotected static-sensitive items.

Module and Subassembly Operations

1. Static-sensitive items are not to be received from a stockroom, kitting, or machine insertion area unless received in approved static-protective packaging, and properly labeled to indicate that its contents are static sensitive.
2. All single station, progressive line manual assembly operators, and visual inspectors prior to wave soldering operations are to be properly grounded with a grounding wrist strap when handling static-sensitive items.
3. Progressive lines used as single stations where operators will be working on a mix of boards, both static-sensitive and nonstatic-sensitive, will require that all operators working on the line be properly grounded. This is necessary to accommodate the sliding of static-sensitive boards along the assembly bench or across positions not engaged in the assembly of this type board.
4. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding wrist straps properly (snugly in contact with bare skin).

Soldering and Lead-Forming Operations

1. All soldering machines, conveyors, cleaning machines, and equipment shall be electrically grounded to ensure that they are at the same ground potential as the grounded operators working on their stations. No machine surfaces exposed to static-sensitive items are to be above the ground potential.
2. All processing equipment shall be grounded, including all loading and unloading stations, that is, the stations before and after each piece of processing equipment.
3. All nonmetallic, static-generating components in the handling systems shall be treated to ensure protection from static.
4. All stations shall be identified by posting signs as outlined in **ESD Labels and Signs in Work Areas.**
5. Operators are to be properly grounded with a grounding wrist strap during any handling, loading, unloading, inspection, rework, or proximity to static-sensitive items.
6. Unloading operators working at a grounded station shall place static-sensitive items into approved static-protective bags or containers.
7. All manual soldering, repair, and touch-up work stations on the solder line are to be static protected. Operators are to wear grounding wrist straps when working on static-sensitive items. Only grounded-tip soldering/desoldering irons are allowed when working on static-sensitive items.
8. It is the responsibility of the Area Spervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding wrist straps properly (comfortably snug in contact with bare skin).

Electrical Testing Operations

1. All electrical test stations shall be static protected. Operators shall be properly grounded when working on these items.
2. Reused antistatic magazines must be monitored for maintenance of antistatic characteristics.
3. Devices should be in an antistatic/conductive environment except at the moment when actually under test.
4. Devices should not be inserted into or removed from circuits or tester with the power on or with signals applied to inputs to prevent transient voltages from causing permanent damage.
5. All unused input leads should be biased if possible.
6. Device or module repairs must be performed at static-free stations with the operator attached to a grounding wrist strap. Grounded-tip soldering irons shall be used when working on static-sensitive items.
7. Static-sensitive items shall be handled through all electrical inspections in static protective containers. Removal of the items from the protective containers shall be done at a static-free work station as discussed in **PREPARATION FOR WORKING AT A STATIC-FREE WORK STATION**. The units must be returned to the containers before leaving the station.
8. All such items shall be shipped with an ESD warning label affixed as listed.
9. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

Packing Operations

1. Static-sensitive items are not to be accepted into the packing area unless they are contained in a static-protected bag or conductive container.
2. A static-sensitive item delivered to the packer within an approved container or bag and found to be in order regarding identification shall be packed in the standard shipping carton or other regular packaging material. Containers are to be labeled in accordance with **GENERAL HANDLING PROCEDURES AND REQUIREMENTS,** item 2.
3. Any void-fillers shall be made of an approved antistatic material.

Burn-In Operations

1. Burn-in board loading and unloading of static-sensitive items shall be done at a static-free station.
2. Shorting clips/shorted connectors shall be installed on the board plug-in tab prior to loading any units into the board sockets. The clip/connector shall be taken off just prior to plugging the board into the oven connector. The clip/connector shall be installed immediately upon removal of the board from the oven connector. Installation and removal of the clip/connector shall be done by a properly grounded operator.
3. All automatic or semiautomatic loading and unloading equipment shall be properly electrically grounded.
4. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

CUSTOMER RETURNED ITEM HANDLING PROCEDURE

Receipt of ESDS-labeled items is to be done at a static-free work station and handled in accordance with applicable sections within this guideline.

QUALITY CONTROL PROVISIONS

Sampling

Each manufacturing, stockroom, and testing operation handling ESDS devices will be audited a minimum of once each quarter for compliance with all terms of this specification by the responsible process control or QRA organization. Ground continuity and the presence of uncontrolled static voltages are considered critical and shall be checked more frequently as specified below.

Ground Continuity (minimum of once a week).

Ground connections (grounding wrist strap, ground wires on cords, etc.) shall be checked for electrical continuity. The presence of a 1 MΩ ±10% resistor in the ground connections between both the operator wrist straps to the work surface and the work surface to ground connector must be verified.

Grounded Conditions (minimum of once a week).

A visual inspection shall be made to determine full compliance with this specification at static-free work stations during handling of static-sensitive items, including operator being grounded as required, static-sensitive items not being handled in unprotected or unauthorized areas, and no static-generating materials at the grounded work station.

Sleeve Protectors (minimum of once a week).

A visual check shall be made to determine that each operator wearing loose-fitting or long-sleeved clothing either has sleeves properly rolled or covered with sleeve protectors properly grounded to the bare skin at the wrist.

Static Voltage Levels (minimum of once a week).

In addition to the visual inspections, a sample inspection using an electrostatic voltmeter will be used to check for uncontrolled electrostatic voltages at or near electrostatic-controlled work stations.

Conductive Floor Tiles (minimum of once a month).

Conductive floors must have a resistance of not less than 25 kΩ from any point on the tile to earth ground. Also, resistance from any point-to-point on the tile floor 3 feet apart shall be not less than 25 kΩ. The test methods to be used are ASTM-F-150-72 and NFPA 56.

Records

Written records must be kept of all these QC audits.

TRAINING

Training is applicable for all areas where individuals come in contact with ESDS (category A) devices. It is the responsibility of each Area Supervisor to make sure that his/her people receive ESD training initially and every 12 months thereafter to maintain proficiency. Training should include static fundamentals, a review of applicable parts of this specification, and actual applications in the work area.

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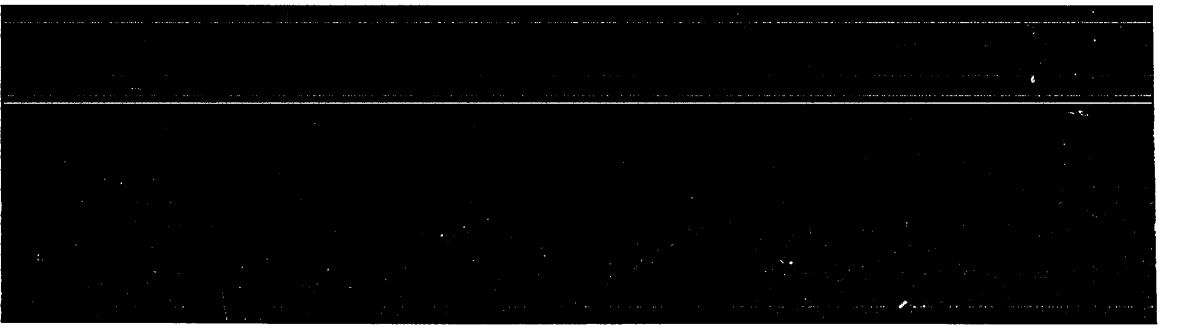

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