TEXAS INSTRUMENTS

Improving Man's Effectiveness Through Electronics

Model 990 Computer

TTY/EIA Interface Module
Depot Maintenance Manual

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PREFACE

This manual provides maintenance instructions for the Texas Instruments TTY/EIA Terminal Interface Module. The manual also provides theory of operation for the module. The information in this manual is divided into the following sections:

I. General Description - This section briefly describes the module, including its operation and characteristics.

II. Installation - This section provides instructions for unpacking, inspecting, and installing the module into a Model 990 Computer mainframe or expansion chassis.

III. Operating Instructions - This section provides programming instructions for the module and a description of how the software controls the operation of the module.

IV. Theory of Operation - This section contains a detailed block diagram description of the TTY/EIA Terminal Interface Module, describes the module's interfaces with the Model 990 Computer and a peripheral device, and provides a discussion of the module's operation.

V. Maintenance - This section provides troubleshooting and fault isolation procedures for the module.

Alphabetical Index - The alphabetical index provides an alphabetical listing of key words and concepts within the manual and locates them for easy reference.

Additional information related to the TTY/EIA Terminal Interface Module may be found in the following documents.

Title	TI Part Number
990 Computer Family Systems Handbook	945250-9701
Model 990 Computer TMS 9990 Microprocessor Assembly Language Programmer's Guide	943441-9701
Model 990 Computer Programming Card	943440-9701
Model 990 Computer 733 ASR/KSR Terminal Installation and Operation	945259-9701
Model 990/4 Computer System Hardware Reference Manual	945251-9701
Model 990/10 Computer System Hardware Reference Manual	945417-9701
Model 990 Computer Family Maintenance Drawings	945421-9701 and 945421-9702
Model 990 Computer Diagnostic Handbook	945400-9701

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SECTION I

GENERAL DESCRIPTION

1.1 GENERAL

The Teletypewriter/Electronic Industries Association (TTY/EIA) Terminal Interface Module (figure 1-1) provides a communication path from Texas Instruments Series 990 Computers to peripheral devices that operate from either a current loop interface or an interface that conforms to EIA Standard RS-232C. The TTY/EIA module can be wired for transmit and receive rates ranging from 75 to 9600 baud, and character code formats of 10 or 11 bits. Typical devices which can interface with the computer through this module include Texas Instruments Model 733 ASR or 733/743 KSR Data Terminals, Texas Instruments Model 306 and 588 Line Printers, and Bell 103 (A or F) or 202 (C or D) data sets, or their equivalents.

1.2 EQUIPMENT OVERVIEW

Figure 1-2 is a simplified diagram of the TTY/EIA module. The module consists of transmit logic, receive logic, and diagnostic logic. The transmit and receive logic can be exercised simultaneously to achieve full duplex operation. Module timing is accomplished by a 4-MHz oscillator and a group of counters that provide a jumper-selected divide network necessary for generating the desired transmit/receive frequency. Prior to data transmission by the computer,

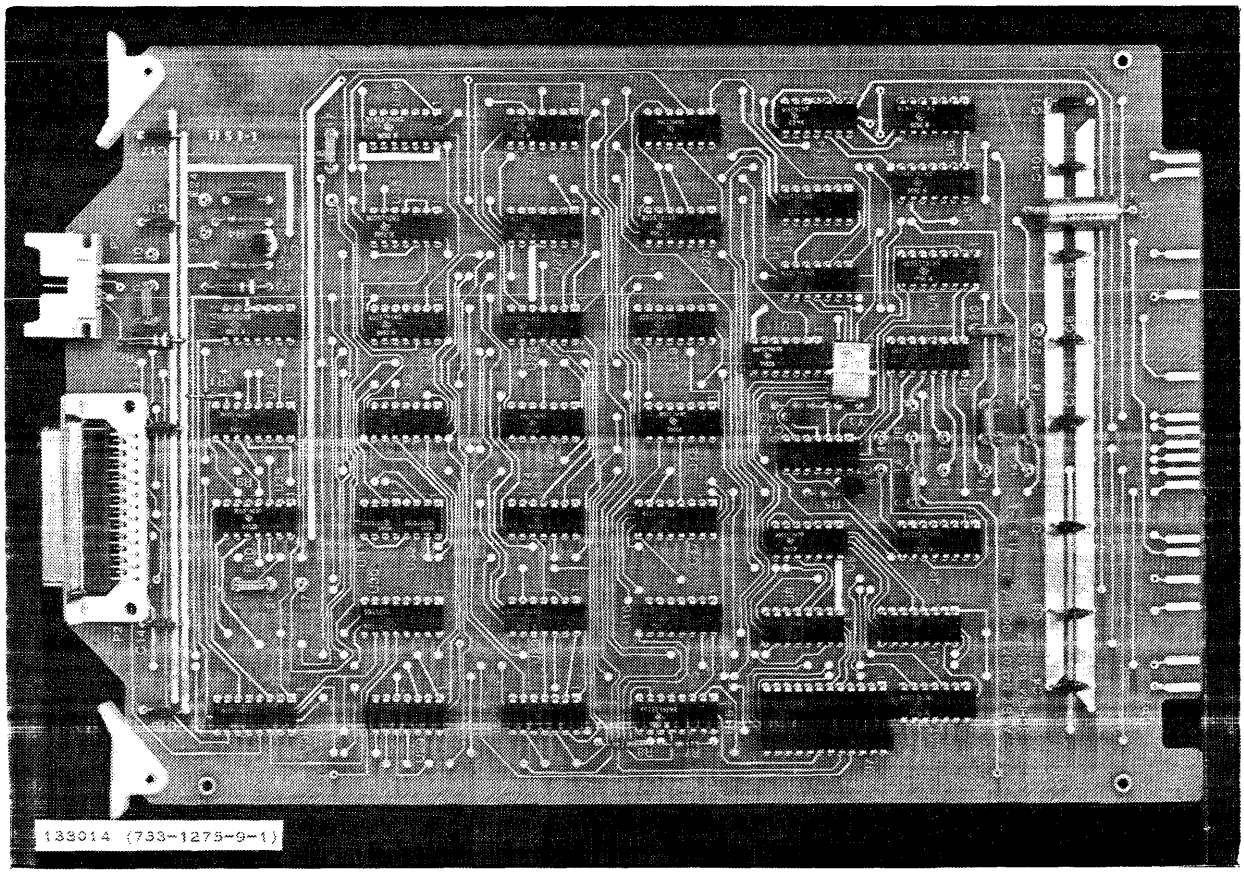


Figure 1-1. TTY/EIA Terminal Interface Module

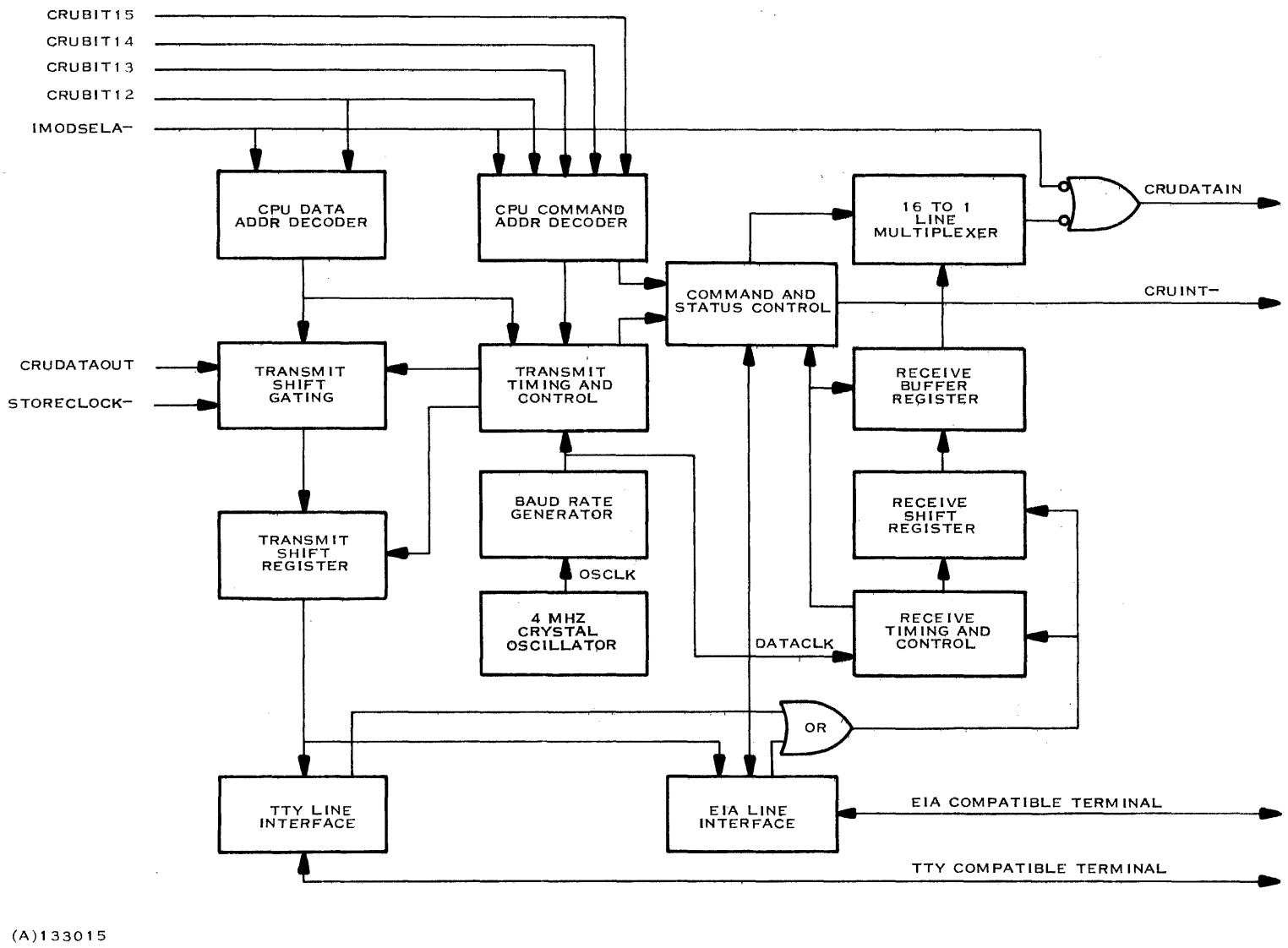


Figure 1-2. Full Duplex TTY/EIA Interface Module Simplified Block Diagram

the request to send and data terminal ready flags are set by the I/O service routine to establish communications with an EIA data terminal. The Data Set Ready signal is then checked to ensure the data terminal is ready for communications.

1.2.1 **TRANSMIT MODE.** In the transmit mode, the computer transfers serial data into the transmit shift register with a STORECLK- signal. Address bits and a module enable signal allow the shifting process to continue until an 8-bit character has been loaded into the shift register. When a full character has been received from the computer, the transmit go flag is set. The transmit go flag enables development of a transmit shift clock whose frequency is determined by the oscillator/counter network. The transmit shift clock serially transfers the start bit, the 8-bit character, and one or two stop bits to the attached data terminal. The write request flag is set to indicate that the character has been output to the data terminal and the module is ready for another transmission cycle.

1.2.2 **RECEIVE MODE.** In the receive mode, the data terminal holds either the TTY or EIA input in a "mark" (logic 1) condition until a "space" (logic 0) condition indicates that a new character is about to be transmitted to the module. The "space" condition sets the receive go flag, which enables the development of a receive shift clock whose frequency is determined by the oscillator/counter network. The receive shift clock gates the serial input data into an 8-bit shift register until a full character has been received. The shift register character is transferred in parallel to a buffer register and applied to a multiplexer for reading by the computer. The read request interrupt logic is set to indicate that the buffer register holds a character for the computer. The computer then enters a service routine that supplies the necessary module enable and address bits to fetch the character.

1.2.3 **INTERRUPT RESPONSE.** An interrupt line from the module informs the computer when the write request flag or read request interrupt logic is set, or when a transition occurs in the Data Set Ready or Data Carrier Detect signals from the data terminal. All four signals are applied to the multiplexer and can be read by the computer to determine the source of the interrupt. The computer instruction repertoire includes single (SBO, SBZ, and TB) and multiple (LDCR and STCR) bit instructions that can be used to control operation of the module. The SBO and SBZ instructions set and clear the addressed control flip-flop; the TB instruction tests the addressed input status line. The LDCR instruction serially transfers an 8-bit character from memory to the module transmit shift register, and the STCR instruction reads an 8-bit character from the module receive buffer register into the computer memory, one bit at a time.

1.2.4 **CHARACTER FORMAT.** The module transmits and receives 10- or 11-bit format code as illustrated in figure 1-3. Eight data bits are provided by either the computer or the attached terminal. The terminal also supplies with its input data a start bit and either one or two stop bits. The terminal requires these start and stop bits in data transmitted to it. The module removes the start and stop bits from data before transmitting the data to the computer. The start and stop bits synchronize the receiving circuitry with the remote transmitter for each character transmitted. Thus, characters may be transmitted in blocks or in random bursts. The 10- or 11-bit code formats are selected by jumper connections on the module.

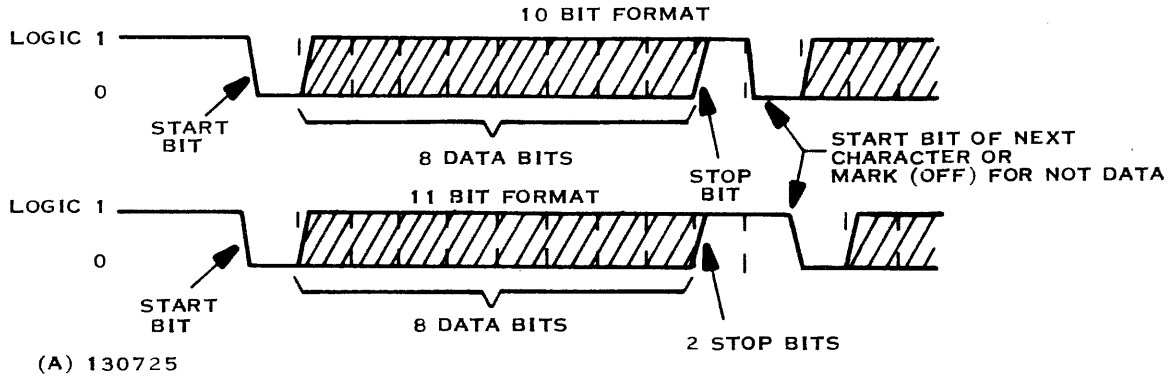


Figure 1-3. Asynchronous (START/STOP) Data Transmission Formats

1.2.5 DIAGNOSTIC MODE. The diagnostic mode is enabled by setting Communications Register Unit (CRU) output bit 15 to a one. In this mode the EIA outputs are gated back into the EIA inputs. Also, the following output signals are gated back to the following input signals:

Output Signal	Input Signal
DTR	DSR
RTS	DCD
XMDT	RCYD
RTS negated	RCR.

1.3 PHYSICAL CHARACTERISTICS

The TTY/EIA Terminal Interface Module is implemented on a half-size printed circuit board that can be inserted into any CRU slot of any Model 990 Computer chassis or expansion chassis. The circuit board is a double-sided board that is 177.8 millimetres (7.00 inches) wide and 274.3 millimetres (10.80 inches) high as oriented in figure 1-1. The board is made to be inserted into an 80-contact, printed circuit board slot connector located in the backpanel of the chassis. There are two connectors located at the top of the board: a 10-pin flat cable connector (the smaller of the two) and a connector that conforms to the industry standard for RS-232 EIA interface. There are eight sets of pluggable jumper sockets on the module labeled E1 through E27. Jumper plugs are provided to be plugged into the desired sockets prior to installation of the module as described in Section II.

1.4 ELECTRICAL CHARACTERISTICS

The interface logic levels and power requirements for the TTY/EIA Terminal Interface Module are listed in table 1-1.

1.5 MODULE ADDRESS

The location of the module within the computer chassis (or expansion chassis) determines the CRU base address that the module recognizes. Therefore, before selecting a chassis location, determine the address that the software handling routine expects the module to recognize.

Table 1-1. TTY/EIA Terminal Interface Module Electrical Characteristics

Specification	Requirement
Peripheral Inputs	(EIA Data) -3V to -25V = Logic 1 (Marking) 3V to 25V = Logic 0 (Spacing) (EIA Control) 3V to 25V = Logic 1 (on) -3V to -25V = Logic 0 (off) (TTY) Short Circuit = Logic 1 Open Circuit = Logic 0
Module Outputs	(EIA Data) -5V to -11V = Logic 1 5V to 11V = Logic 0 (EIA Control) 5V to 11V = Logic 1 -5V to -11V = Logic 0 (TTY) 20ma Current Loop = Logic 1 Open Circuit = Logic 0
Power (from computer or expansion chassis)	EIA Interface { +5Vdc at 0.38A ±12Vdc at 20 mA 20 mA
Transmission Rates Available	75, 110, 300, 1200, 2400, 4800 and 9600 baud

SECTION II

INSTALLATION

2.1 GENERAL

This section provides instructions for unpacking, inspecting, and installing a TTY/EIA Terminal Interface Module. Particular attention is given to the connection of the jumper plugs provided with the circuit board.

2.2 UNPACKING

The module is packed in one box and wrapped in plastic bubble-pack wrapping. Visually inspect the box for signs of damage. Open the box and remove the module from the bubble-pack wrapping. Verify that at least eight jumper plugs have been received (they are shipped plugged into the circuit board). Do not discard any packing material until all equipment is accounted for.

2.3 INSPECTION AND PREPARATION FOR INSTALLATION

Perform the following steps prior to installing the module into a chassis slot:

1. Visually inspect the circuit board for cracks, corrosion, loose components, and loose connectors.

2. Remove all jumper plugs from their sockets.

3. According to the predetermined operating requirements for the module, insert the jumper plugs into the sockets. Table 2-1 gives the connections for possible options; figure 2-1 illustrates the locations of the jumper connections.

4. Install a center card guide (if one is not present) for the selected chassis slot.

2.4 INSTALLATION

After defining a location for the module and checking the jumper plug configuration, perform the following steps to install the module in the desired location:

1. Ensure that chassis power is off.

2. Insert the circuit board, component side up, into the selected slot until the sides of the board slide into the card guides on either side of the slot (one guide is in a center card guide which must have been installed before card insertion).

3. Gently push the board straight in until the card edge connector engages the slotted connector in the backpanel.

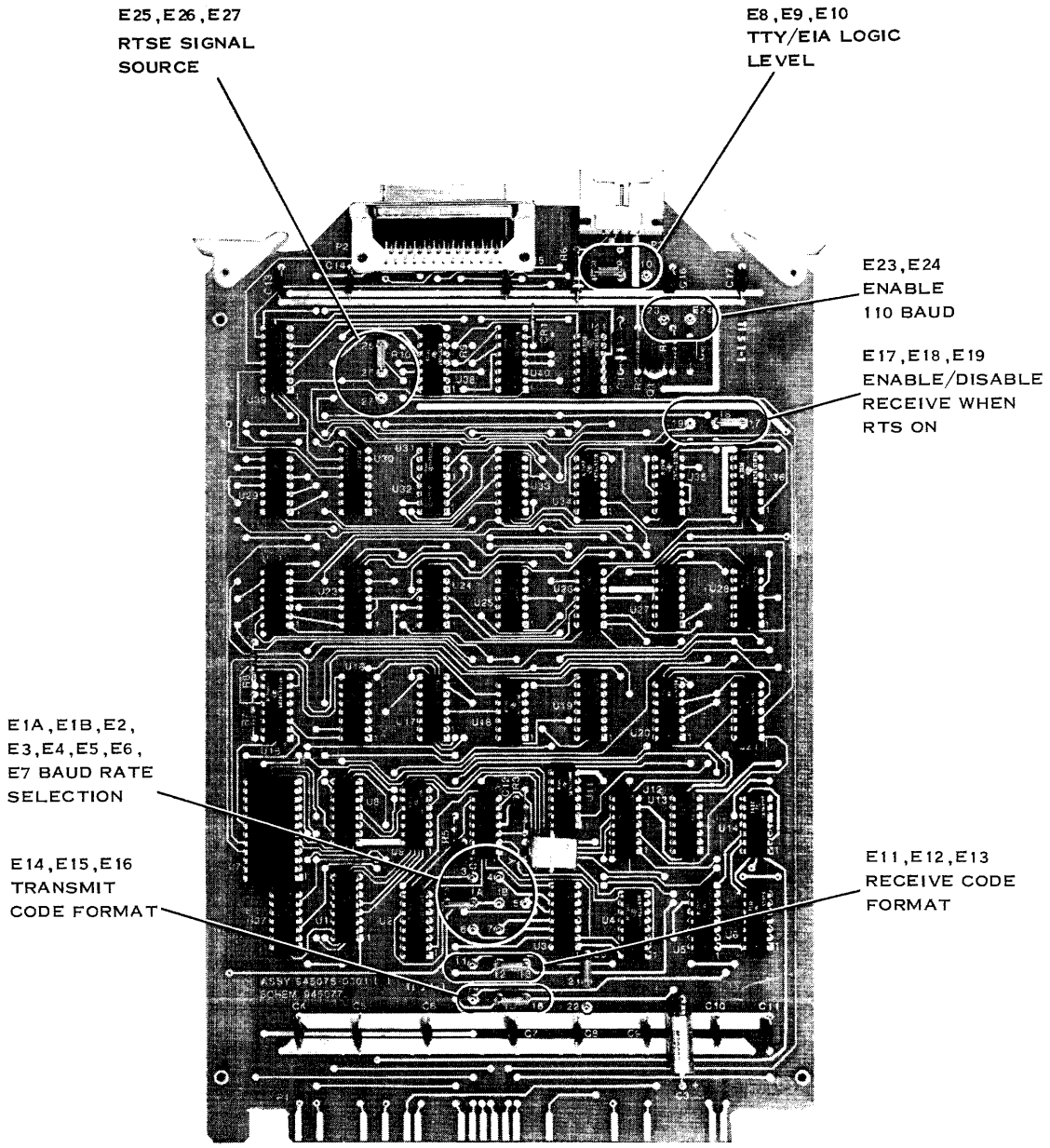
4. Insert the appropriate cable into the proper cable connector.

5. Dress the cable out of the chassis (toward the rear of the chassis).

6. Connect the other end of the cable to the desired peripheral device in accordance with the installation instructions for the device.

Table 2-1. Jumper Schedule

Option	Jumper From	Jumper To	733 ASR	733/743 KSR	306/588 Line Printer
Baud Rate = 75	E1A	E2			
110	E1A	E2			
300	E1A	E3		X	
1200	E1B	E4	X		
2400	E1B	E5			
4800	E1B	E6			X
9600	E1A	E7			
Logic Level = EIA	E8	E9	X	X	X
TTY	E9	E10			
Code Format = 10-bit (receive)	E11	E12	X	X	X
11-bit	E12	E13			
Code Format = 10-bit (transmit)	E14	E15	X	X	X
11-bit	E15	E16			
Enable receive during RTS	E17	E18	X	X	X
Disable 110 baud	E20	E21	X	X	X
Enable 110 baud	E21	E22			
Enable 110 baud	E23	E24			
RTSE = RTSE	E25	E26	X	X	
RTSE = $\overline{\text{DTR}}$E	E26	E27			X



(B)135215 (733-1275-9-1)

Figure 2-1. Jumper Socket Locations

SECTION III

OPERATING INSTRUCTIONS

3.1 GENERAL

Operation of the TTY/EIA Terminal Interface Module consists of the programming required to perform the necessary interface functions with the attached data terminal. The service routines implemented to handle this interface use the SBO, SBZ, TB, LDCR, and STCR instructions. These instructions normally use an effective CRU address that addresses bit zero of the module under consideration. Since the module can be inserted into any of the available CRU chassis locations and the locations are wired for preestablished addresses, the base address depends upon that hardware configuration.

The only consideration other than programming that affects the module's operation is the selection of the proper jumper configuration to match the transfer rate and code format of the attached data terminal. Refer to Section II of this manual for the details of the various jumper configurations.

3.2 PROGRAMMING

The interface between the computer and the module consists of 16 addressable I/O bits. The output bits can be divided into two groups of eight, as shown in figure 3-1. The first eight bits

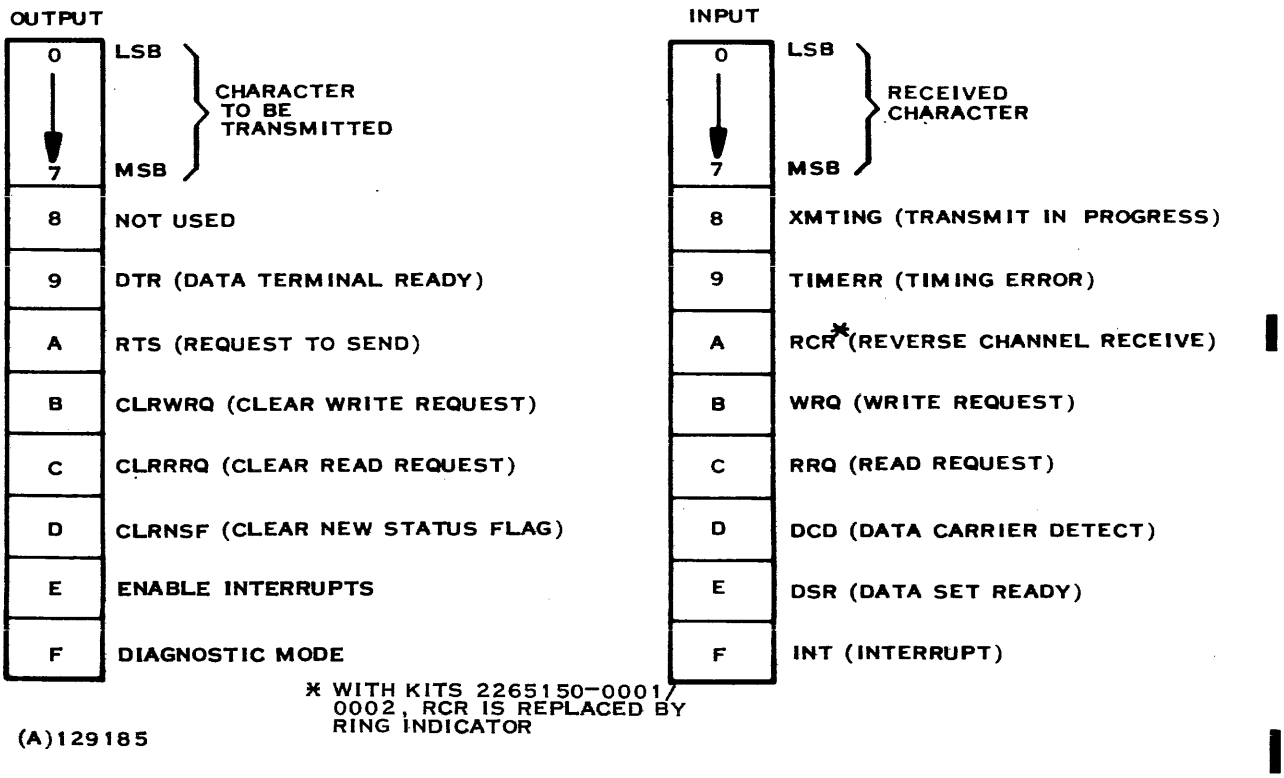


Figure 3-1. TTY/EIA Terminal Interface Module Addressable Input/Output Lines

make up the character to be sent to the data terminal, and the last eight bits are used primarily for control. The first eight bits of input make up the character being received from the data terminal, and the last eight bits provide the computer with status data. Tables 3-1 and 3-2 describe the output command bits and input status bits, respectively.

Table 3-1. TTY/EIA Terminal Interface Module Output Command Signals

Signal	Description
Data Terminal Ready	Enables data terminal operation (must be on before any communication using the TTY/EIA module).
Request to Send	Places data terminal in transmit mode (not used with teletypewriters).
Clear Write Request	Clears write request flag on module to prepare for another character write (transmit).
Clear Read Request	Clears read request interrupt logic on module to prepare for another character read (receive).
Clear New Status Flag	Clears new status flag on module to enable new interrupts.
Enable Interrupts	Enables interrupt generating logic on module. (DTR must also be on.)
Diagnostic Mode	Gates EIA outputs to EIA inputs.

Table 3-2. TTY/EIA Terminal Interface Module Input Status Signals

Signal	Description
Transmit In-Progress	Module is currently transmitting to a data terminal.
Timing Error	Indicates data in receive buffer register may be in error because two or more characters have been loaded in the buffer and no read operation has been performed by the computer.
Reverse Channel Receive*	Indicates reverse channel receive status of 202 type dataset (not used by teletypewriter).
Write Request	Write request flag set to indicate a character has been sent to the data terminal.
Read Request	Read request flag set to indicate a character has been received from the data terminal and is ready to be read by the computer.
Data Carrier Detect	Indicates carrier is detected at the data terminal (not used by teletypewriter).
Data Set Ready	Indicates data terminal is ready to communicate (not used by teletypewriter).
Interrupt	Module interrupt flag set when the write request flag or read request flags are set or when a transition occurs in the Data Set Ready or Data Carrier Detect signals. DTR must have been set.

*With kits 2265150-0001/0002, this signal is Ring Indicator signifying a remote station is calling the host.

The I/O routines written to handle communications with the data terminals attached to the module vary with each device type. This is due to the difference in the controls accepted and status returned by the data terminals. Generally, the I/O routine must first establish communications with the data terminal and then proceed to read/write data on a character-by-character basis. At the same time, the routine must be prepared for irregular status indicators and be capable of handling interrupts.

3.2.1 **INTERRUPTS.** An interrupt is a signal that informs the computer that the module requires attention. The interrupt flag for the TTY/EIA Terminal Interface Module is input bit F_{16}. This bit sets whenever one of three conditions occurs:

- Write Request (input bit B_{16}) – When the module has completed transmission of a character and requires a new character from the computer, it sets input bit B and sets the Interrupt Flag, input bit F, to a one. This flag is reset by a CPU output to bit B (Clear Write Request).

- Read Request (input bit C_{16}) – One-half bit time after the module receives an input character and loads it into the receive buffer register, it sets input bit C and sets the Interrupt Flag, input bit F, to a one. This flag is reset by a CPU output to bit C (Clear Read Request).

- New Status Flag – Whenever a status transition occurs in either Data Carrier Detect (input bit D) or Data Set Ready (input bit E), the module sets the interrupt flag, input bit F, to a one. Table 3-3 lists the status changes that set the new status flag. This flag is reset by a CPU output to bit D (Clear New Status Flag).

The interrupt signal to the computer is generated when the interrupt flag is set, and interrupts are enabled by setting the Enable Interrupt latch, CRU output bit E_{16}, to a one. This interrupt signal is connected to an interrupt level by jumper wiring on the computer backpanel. Refer to the *Model 990/4 Computer System Hardware Reference Manual* (Manual Number 945251-9701) or the *Model 990/10 Computer System Hardware Reference Manual* (Manual Number 945417-9701) for information on this wiring.

Table 3-3. Status Transitions Affecting New Status Flag

CRU Output Bit D	CRU Input Bits (EIA Status)		New Status Flag
	E (DSR)	D (DCD)	
0	0 to 1	0	1
0	1	1 to 0	1
0	X	0 to 1	1
0	1 to 0	X	1
pulse	X	X	0

X = either 1 or 0

When the interrupt signal is recognized by the computer and the interrupt occurs at a level less than or equal to the interrupt level in the computer status register, then the following actions occur:

1. The new workspace pointer and program-counter contents are fetched from memory locations determined by the interrupt level.

2. The current workspace pointer, program-counter and status-register contents are stored in workspace registers 13, 14 and 15 of the new workspace.

3. The new status register contents are set to inhibit interrupts of lower priority than the level of the interrupt.

4. The interrupt processing routine is entered at the address specified by the new program counter.

The interrupt-processing routine determines which module generated the interrupt by interrogating bit F_{16} of all modules corresponding to the interrupt level until it finds an active interrupt bit. The program then examines input bits B (Write Request), C (Read Request), D (Data Carrier Detect), and E (Data Set Ready) of that module to determine the condition that caused the interrupt, and the routine must clear the interrupt condition by generating an output (either a 1 or a 0) to the applicable address bit.

3.2.2 **TIMING CONSIDERATIONS.** When data is being transferred to the CPU, a timing error can occur if the program does not store a received character into memory before a new character is received. When such an overrun occurs, CRU input bit 9 (TIMERR) from the module sets to flag the condition. This bit clears automatically when the read request interrupt logic is reset.

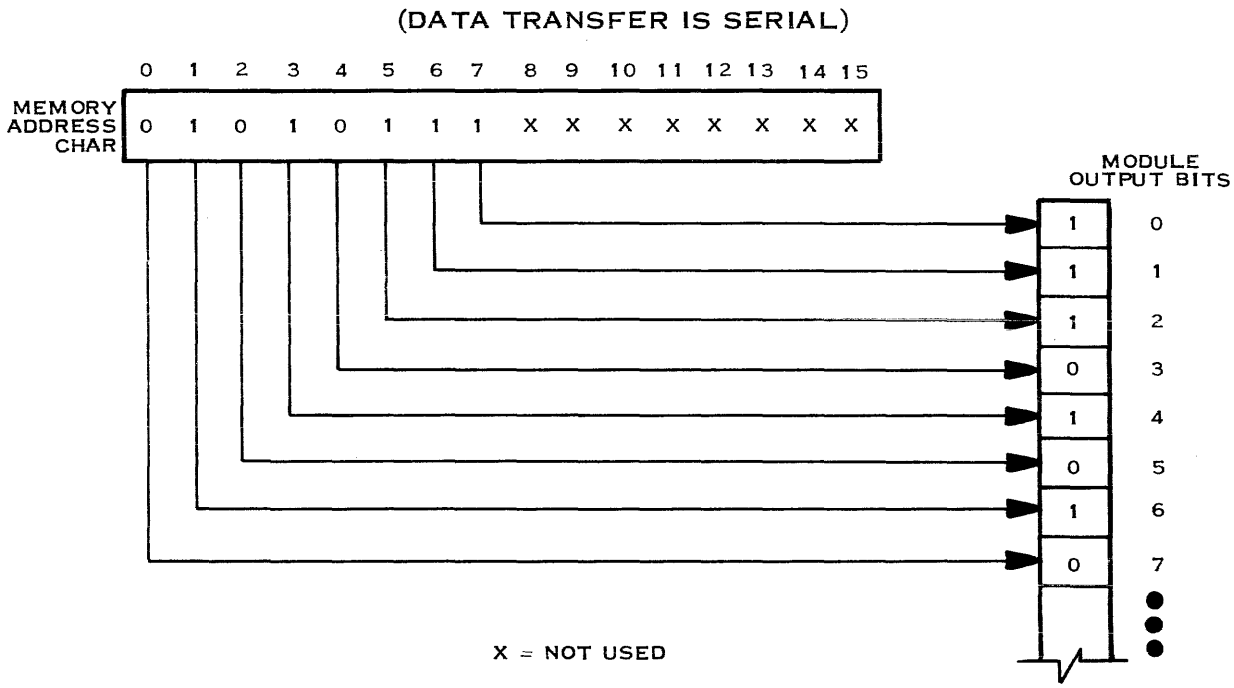
Timing is not critical when data is being transferred from the CPU. However, efficient use of the communication line requires that the next character to be transmitted be presented to the interface within one bit time following the Writer Request interrupt. The time interval, in seconds, between characters for a particular format and baud rate is given by the number of bits per character (including start and stop bits) divided by the baud rate. The reciprocal of this character time is the character rate. The interval between bits (bit time) is the reciprocal of the baud rate.

3.2.3 **OUTPUT OPERATION.** A character may be output from the computer to the module using an 8-bit Load CR (LDCR) instruction. Any of the addressing modes of the 990 Computer may be used. The direct-addressing mode is of the form:

```
LDCR @CHAR, 8
```

This instruction results in an 8-bit transfer from memory location CHAR to the current CRU base address starting with bit 0 and incremented through bit 7. Figure 3-2 illustrates this transfer. Initiating this sequence starts data transmission from the module when the entire 8-bit character is present in the module. The data is sent serially on the communication line.

During the transfer operation, CRU bit 8 (Transmit in Progress) remains true; it resets when the character has been completely transmitted and Write Request (bit B) has been set. A new character output to the module must not be started until Transmit in Progress drops and Write Request sets. Outputs to clear interrupt bits reset independently of the output data lines.



(A)130727A

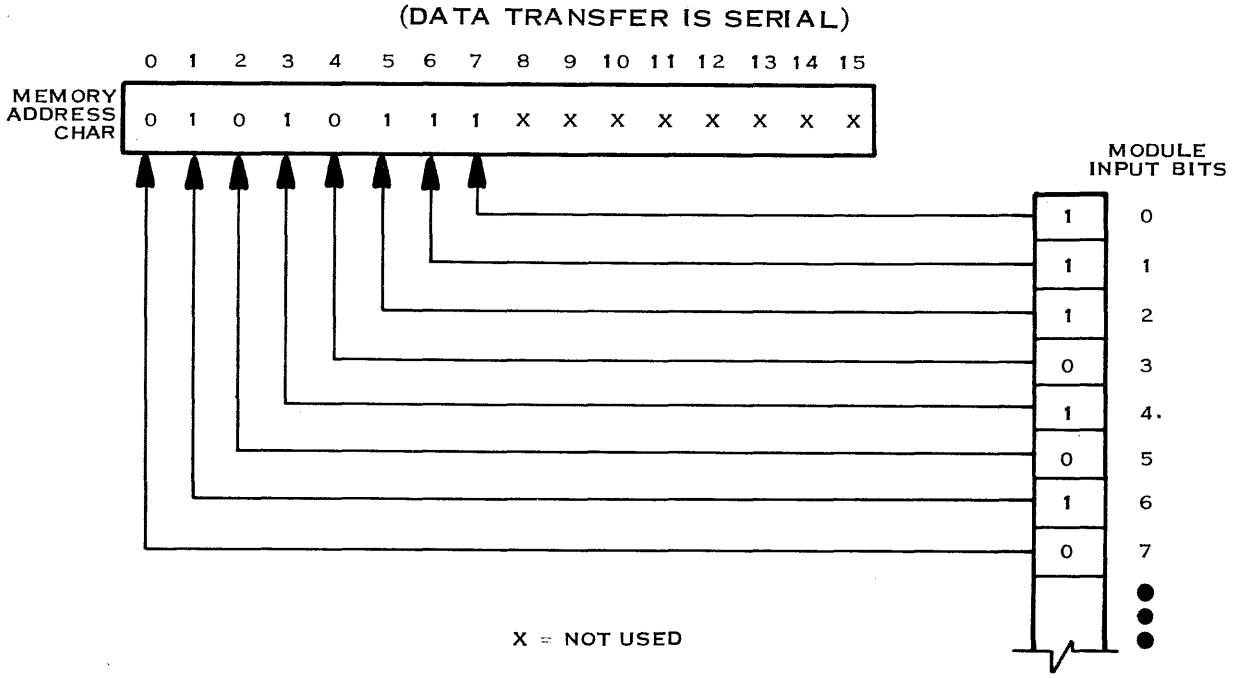
Figure 3-2. Output Character Transfer

3.2.4 **INPUT OPERATION.** A character is input to the computer from the module using an 8-bit Store CR (STCR) instruction. Any of the addressing modes of the 990 Computer may be used. The direct addressing mode is of the form:

STCR @CHAR, 8

This instruction results in an 8-bit transfer from the current CRU base address (bits 0 through 7) to memory location CHAR. Figure 3-3 illustrates this transfer. The Store CR operation usually occurs after the module has notified the program that data is ready for transfer by the Read Request (bit C) and the Interrupt (bit F). The program must then transfer the data and reset the interrupt before the next character arrives from the input device and is transferred into the module buffer register. Failure to respond within this time constraint results in a data overrun error, and sets the Timing Error input bit (bit 9).

3.2.5 **ERROR DETECTION.** All data error detection, except data overrun conditions, is the responsibility of the data-handling program. If one of the eight bits from the module represents a parity bit, the program must check the input data character parity. This is done by testing the parity bit in the computer status register after the LDCR instruction. Similarly, if the device connected to the module requires a parity bit, the program must generate that bit. Cyclical redundancy check characters to maintain the integrity of a data stream, if used, must also be generated and checked by the program. Module input bit 9 (Timing Error) indicates a data overrum condition.



(A)130728A

Figure 3-3. Input Character Transfer

3.2.6 **SAMPLE PROGRAM SEQUENCES.** This paragraph contains sample program sequences to illustrate the fundamental mechanics required for input and output operations. Actual routines are more efficient by controlling these low-speed input/output operations with interrupts.

3.2.6.1 **Echo Character.** Figure 3-4 illustrates an instruction sequence that reads a character typed on the keyboard of a 733 ASR/KSR Data Terminal, echoes that character to the printer of that device, and loops to read another character.

3.2.6.2 **Output Character String.** Figures 3-5 through 3-7 illustrate an instruction sequence that outputs a character string to the printer of a Model 733 ASR Data Terminal. Figure 3-5 illustrates the definition of the input and output CRU bits to the module. This is not necessary, but makes subsequent reference to these bits easier. Figure 3-6 shows code that fetches a string of characters for transfer to the data terminal.

This routine is called as follows:

```
BLWP @OUTASR
DATA BUFFER
```

where BUFFER is the name of the buffer containing the character string to be output. The final character of this string must be the two's complement of the desired character.

Figure 3-7 illustrates a sequence that must be observed when transmitting a string of characters to the printer of a Model 733 ASR Data Terminal. Since the baud rate of the module is set to four times that of the data terminal printer, three null characters must be sent by the module to the terminal with each character that is to be printed by the terminal.

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MODEL 990/TMS 9900 ASSEMBLY LANGUAGE CODING FORM

LABEL (1–6)	OPER (8–11)	OPERAND (13–25)	COMMENTS (31–60)
* SAMPLE	EQU	PRØGRAM SEQUENCE -	ECHØ TYPED INPUT TØ PRINTER
	LI	R12,0	SET 733 ASR/KSR CRU BASE
	SBØ	DTR	SET DATA TERMINAL READY
	SBØ	RTS	SET REQUEST TØ SEND
* GET INPUT	CHARACTER		
LØØP	CLR	R11	CLEAR R11
TBRRQ	TB	RRQ	EXAMINE READ REQUEST
	JNE	TBRRQ	WAIT UNTIL RRQ = 0
	STCR	R11,8	GET KEYBØARD ENTRY
	SBZ	CLRRR	RESET READ REQUEST
* ECHØ	CHARACTER		
	LDCR	R11,8	PUT CHARACTER ØUT
TBWRQ	TB	WRQ	EXAMINE WRITE REQUEST
	JNE	TBWRQ	WAIT UNTIL WRQ = 0
	SBZ	CLRWRQ	SET WRITE REQUEST FLAG
	B	LØØP	REPEAT

PROGRAM: ECHO PRINT | PROGRAMMED BY | CHARGE | PAGE 1 | OF 1

(A)133016B

Figure 3-4. Echo Character Sample Routine

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MODEL 990/TMS 9900 ASSEMBLY LANGUAGE CODING FORM

LABEL (1–6)	OPER (8–11)	OPERAND (13–25)	COMMENTS (31–60)
* SAMPLE PROGRAM SEQUENCE -			DEFINE INPUT AND OUTPUT BITS
* INPUT BITS			
XMTING	EQU	8	TRANSMIT IN PROGRESS
TIMERR	EQU	9	TIMING ERROR
RCR	EQU	10	REVERSE CHANNAL RECEIVE
WRQ	EQU	11	WRITE REQUEST
RRQ	EQU	12	READ REQUEST
DCD	EQU	13	DATA CARRIER DETECT
DSR	EQU	14	DATA SET READY
INT	EQU	15	INTERRUPT
* OUTPUT BITS			
DTR	EQU	9	DATA TERMINAL READY
RTS	EQU	10	REQUEST TO SEND
CLRWRQ	EQU	11	CLEAR WRITE REQUEST
CLRRRQ	EQU	12	CLEAR READ REQUEST
CLRNSF	EQU	13	CLEAR NEW STATUS FLAG
ENAINT	EQU	14	ENABLE INTERRUPTS
DIAG	EQU	15	DIAGNOSTIC MODE

PROGRAM	PROGRAMMED BY	CHARGE	PAGE	OF
OUTPUT TO 733 ASR			1	3

(A)133017B

Figure 3-5. I/O Definition

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INCORPORATED

MODEL 990/TMS 9900 ASSEMBLY LANGUAGE CODING FORM

LABEL (1–6)	OPER (8–11)	OPERAND (13–25)	COMMENTS (31–60)
* SAMPLE	EQU	PROGRAM SEQUENCE -	FETCH A CHARACTER STRING
OUTENT	LI	R12,0	SET 733 ASR CRU BASE
	LIMI	1	DISABLE INTERRUPTS
	CLR	R4	CLEAR LAST CHARACTER FLAG
	MOV	*R14+,R10	GET BUFFER ADDRESS
	SBO	DTR	SET DATA TERMINAL READY
	SBO	RTS	SET REQUEST TO SEND
GETOUT	MOVB	*R10+,R9	GET OUTPUT CHARACTER
	JGT	PRINT	JUMP TO OUTPUT ROUTINE
	JEQ	PRINT	IF NOT LAST CHARACTER
	INC	R4	SET LAST CHARACTER FLAG
	INV	R9	COMPLEMENT CHARACTER
	AI	R9,>0100	MAKE LEFT CHARACTER 2'S COMP
PRINT	BL	NULL	JUMP TO NULL SEQUENCE
	MOV	R4,R4	CHECK LAST CHARACTER FLAG
	JEQ	GETOUT	REPEAT UNTIL LAST CHARACTER
	SBO	CLRRRQ	CLEAR READ REQUEST
	SBO	CLRWRQ	CLEAR WRITE REQUEST
	SBO	CLRNSF	CLEAR NEW STATUS FLAG
	RTWP		RETURN TO CALLING PROGRAM
* BLWP	ENTRY,	WORKSPACE	
OUTASR	DATA	OUTWS,OUTENT	BLWP ENTRY DATA
OUTWS	BSS	32	WORKSPACE

PROGRAM: OUTPUT TO 733 ASR | PROGRAMMED BY: | CHARGE: | PAGE: 2 | OF: 3

(A)133386A

Figure 3-6. Fetch Character String Sample Routine

TEXAS INSTRUMENTS
INCORPORATED

MODEL 990/TMS 9900 ASSEMBLY LANGUAGE CODING FORM

LABEL (1–6)	OPER (8–11)	OPERAND (13–25)	COMMENTS (31–60)
* SAMPLE	EQU	PRØGRAM SEQUNCE	ØUTPUT A CHARACTER STRING
NULL	SBØ	CLRRRQ	CLEAR READ REQUEST
	SBØ	CLRWRQ	CLEAR WRITE REQUEST
	LDCR	R9,8	ØUTPUT CHARACTER FRØM R9
	SETØ	R3	SET MAX LØØP CØUNT TØ R3
DØWN	DEC	R3	DECREMENT LØØP CØUNT
	TB	WRQ	EXAMINE WRITE REQUEST
	JNE	DØWN	LØØP IF NØT SET
	LI	R6,3	SET TØ ØUTPUT 3 CHARACTERS
ØUTPUT	SBØ	CLRWRQ	CLEAR WRITE REQUEST
	LDCR	R7,8	ØUTPUT CHARACTER
	SETØ	R3	SET MAX LØØP CØUNT TØ R3
DECLØØ	DEC	R3	DECREMENT LØØP CØUNT
	JEQ	DECHAR	JUMP IF LØØP CØUNT = 0
	TB	WRQ	EXAMINE WRITE REQUEST
	JNE	DECLØØ	LØØP
DECHAR	DEC	R6	DECREMENT CHARACTER CØUNT
	JNE	ØUTPUT	ØUTPUT NEXT CHARACTER
CRET	CB	R9,R8	CHECK FØR CARRIAGE RETURN
	JNE	END	NØ DELAY IF NØ CR
	SETØ	R6	SET MAX LØØP CØUNT TØ R6
DEC1	DEC	R6	DECREMENT R6
	JNE	DEC1	LØØP
END	SBØ	CLRRRQ	CLEAR READ REQUEST
	SBØ	CLWRRQ	CLEAR WRITE REQUEST
	RTWA		RETURN TO CALLING ROUTINE

PROGRAM: OUTPUT TO 733 ASR | PROGRAMMED BY: | CHARGE: | PAGE: 3 | OF: 3

(A)133387A

Figure 3-7. Output Character String Sample Routine

SECTION IV

THEORY OF OPERATION

4.1 GENERAL

This section contains a detailed block diagram description of the Full Duplex TTY/EIA Module, describes the module's interfaces with the Model 990 Computer and a peripheral device, and provides a discussion of the module's operation.

4.2 BLOCK DIAGRAM DESCRIPTION

Figure 4-1 is a detailed functional block diagram of the Full Duplex TTY/EIA module. The following discussion is based on figure 4-1.

4.2.1 4-MHz OSCILLATOR. The 4-MHz crystal-controlled oscillator produces a square wave (OSCLK) whenever power is applied to the module. The oscillator's output is used by the baud rate clock to produce DATACLK, the basis for all the timing signals on the module.

4.2.2 BAUD RATE CLOCK. The baud rate clock consists of three cascaded 4-bit binary counters as shown in figure 4-2. The first counter is preset to count from 3 through 15 ,and divides the frequency of OSCLK by 13. A jumper connecting either E20 or E22 to E21 presets the second counter to count from 0 through 15 (E20 to E21; divides the frequency of MOD13CRY by 16) or from 5 through 15 (E22 to E21; divides the frequency of MOD13CRY by 11). The E22-to-E21 jumper plug produces a 110-baud output at E2, while connecting E20 to E21 enables outputs of 75, 300, 1200, 2400, 4800, and 9600 baud at E2 through E7. The third counter is preset to count from 0 through 15 to frequency-divide MOD11CRY by 16 and produce the 75- and 300-baud signals at E2 and E3, respectively.

A jumper plug connecting E1A or E1B to one of E2 through E7 selects the frequency of DATACLK according to the schedule given in table 4-1. The baud-rate clock is active as long as power is applied to the module.

4.2.3 ADDRESS DECODER. The address decoder examines bits 12 through 15 of the 12-bit CRU address word from the 990 to decode seven signals ((ADDS,9-15)-) to control status and interrupt latches on the module. Table 4-2 shows the outputs generated by the address decoder for the CRUBIT,12-15 combinations with bit 12 equal to logic 1. For CRUBIT,12-15 combinations with bit 12 equal to logic 0, all address decoder outputs are held at logic 1 (inactive). Each address decoder output is a low-active pulse having the same pulse width as STORECLK-. Table 4-2 also lists the action caused by the address decoder outputs.

4.2.4 TRANSMIT SHIFT GATING LOGIC. Transmit shift gating logic consists of several gates and inverters whose function is to provide the transmit shift generator with data and clock inputs during data transmission from the computer to the device attached to the module. Transmit shift gating logic provides the serial data from the computer (CRUDATAOUT) to the transmit shift register as XMSRIN whenever the transmit go flag is reset. If the transmit go flag is set, the input to the transmit shift register is held at logic 1. The clock signal provided to the transmit shift register (XMSRCLK) is either Transmit Shift Clock (XSCLK) from the transmit shift clock generator or Store Clock (STORECLK-) from the computer. If the transmit go flag is set, XMSRCLK is equivalent to XSCLK. If the transmit go flag is reset, bit 12 of the CRU address word (CRUBIT,12-15) is logic 0, and the module has been selected (CRUSELO = 1) XMSRCLK is equivalent to STORECLK- inverted.

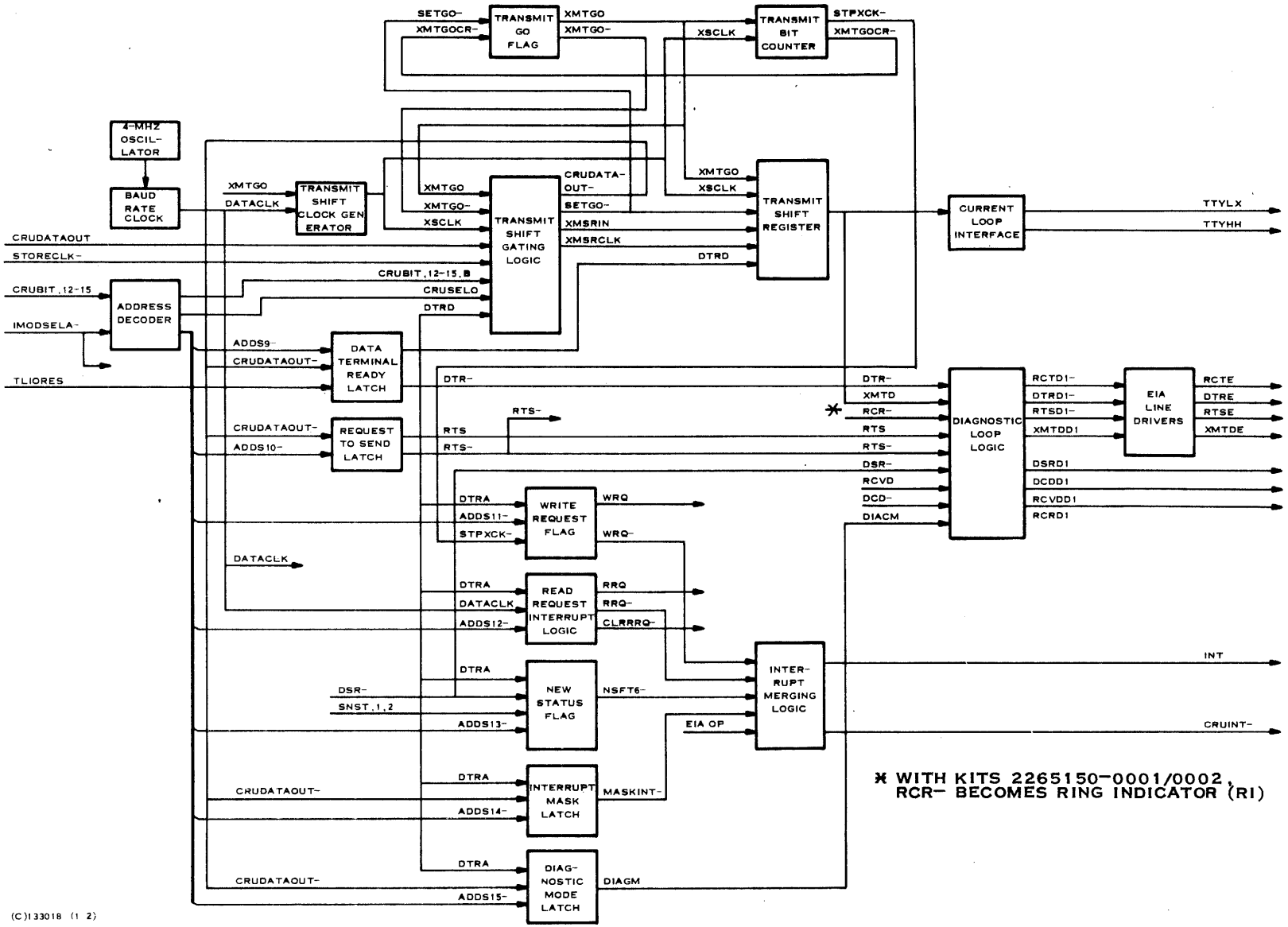

Figure 4-1. TTY/EIA Terminal Interface Module Detailed Functional Block Diagram (Sheet 1 of 2)

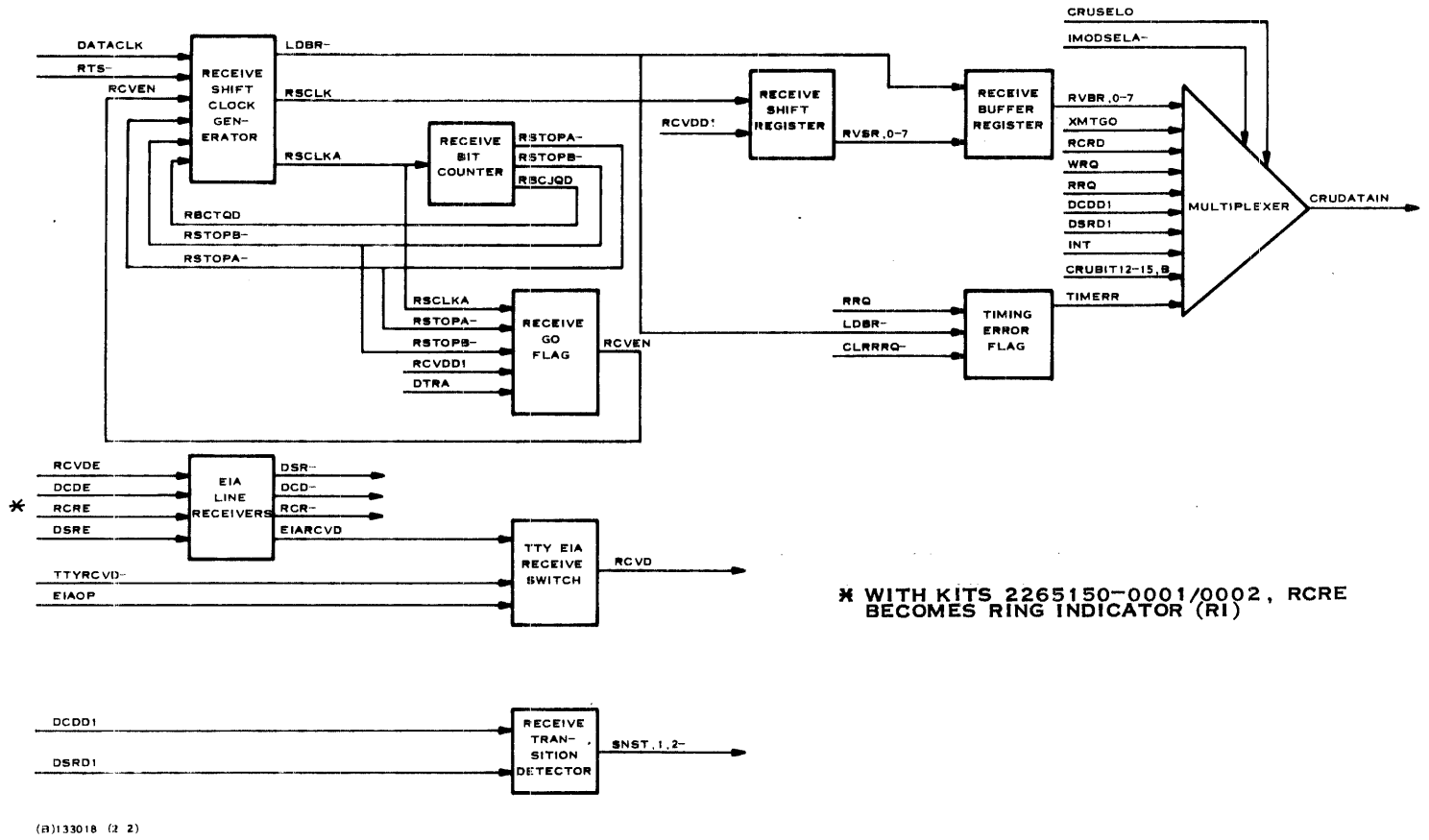

Figure 4-1. TTY/EIA Terminal Interface Module Detailed Functional Block Diagram (Sheet 2 of 2)

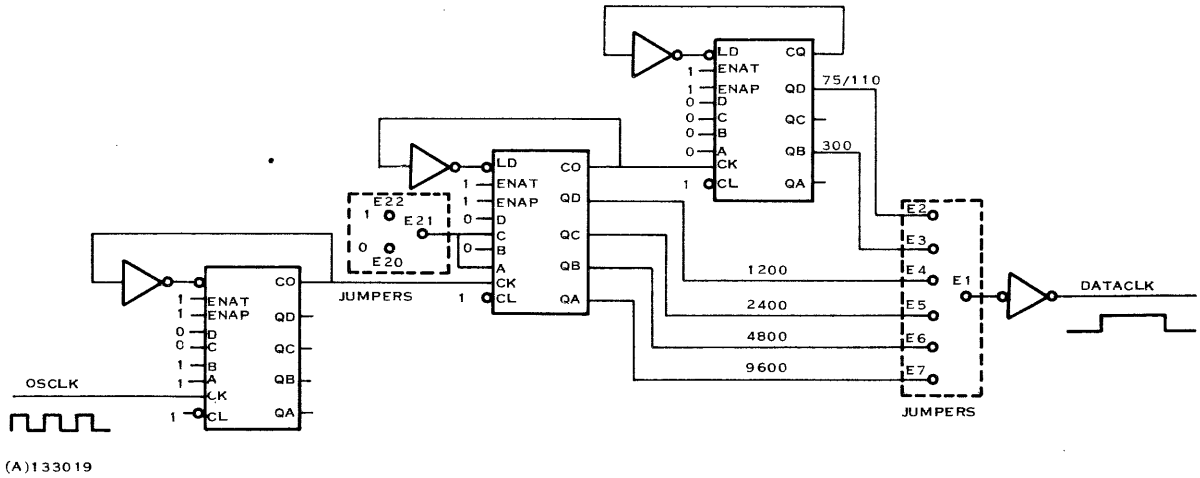

Figure 4-2. Baud Rate Clock Logic Diagram

Table 4-1. DATACLK Baud Rate Selection

From	To	Baud Rate	
	E2	110	E21 connected to E22
	E2	75	E21 connected to E20
	E3	300	
E1	E4	1200	
	E5	2400	
	E6	4800	
	E7	9600	

Table 4-2. Active Address Decoder Output for CRUBIT,12-15

CRUBIT,12-15	Active (ADDS,9-15)-	Action
1000	———	———
1001	ADDS9-	Sets data terminal ready latch according to CRUDATAOUT-.
1010	ADDS10-	Sets request to send latch according to CRUDATAOUT-.
1011	ADDS11-	Sets write request flag if data terminal ready flag reset and transmit bit counter active.
1100	ADDS12-	Resets read request flag and timing error flag.
1101	ADDS13-	Resets new status flag.
1110	ADDS14-	Sets interrupt mask latch according to CRUDATAOUT-.
1111	ADDS15-	Sets diagnostic mode latch according to CRUDATAOUT-.

4.2.5 **TRANSMIT GO FLAG.** The transmit go flag is a flip-flop that controls the gating of data from the computer to a peripheral device. When set, the transmit go flag enables the transmit shift clock generator and the transmit bit counter, causes the transmit shift register to be loaded with ones, causes the transmit shift register to be clocked by Transmit Shift Clock (XSCLK), and gates the output of the transmit shift register to the output logic. When reset, the transmit go flag disables the transmit shift clock generator and transmit bit counter, allows CRUDATAOUT to be loaded into the transmit shift register when clocked by STORECLK–, forces the transmit shift register's output (XMTD) to logic 1 until the register is filled, and prepares SETGO– to set the transmit go flag prior to the transmission of another data word by the computer. The transmit go flag is reset by the transmit bit counter at the completion of each data word transfer.

4.2.6 **TRANSMIT SHIFT CLOCK GENERATOR.** The transmit shift clock generator, a 4-bit binary counter and two gates, produces, from DATACLK, Transmit Shift Clock (XSCLK), a clock signal with a pulse width equal to that of DATACLK and a period 16 times as long as DATACLK's. The frequency of XSCLK is equal to the transmit baud rate. The transmit shift clock generator is active whenever the transmit go flag is set, and clocks the transmit bit counter and the transmit shift register.

4.2.7 **TRANSMIT BIT COUNTER.** The transmit bit counter consists of a 4-bit binary counter, a jumper connection, and a gate. When the transmit go flag is set, the transmit bit counter monitors Transmit Shift Clock (XSCLK) from the transmit shift clock generator. After counting 10 or 11 Transmit Shift Clock pulses, depending upon the jumper connection, the transmit bit counter issues STPXCK- = 0 to reset the transmit go flag and set the write request flag.

4.2.8 **TRANSMIT SHIFT REGISTER.** The transmit shift register consists of an 8-bit parallel-out shift register, a flip-flop, and an output gate. During the transfer of data from the computer to a peripheral device, serial data (XMSRIN) is clocked into the shift register by XMSRCLK, then the data is serially clocked through the flip-flop by Transmit Shift Clock (XSCLK) into the output gate where it is gated to the peripheral device if the transmit go flag is set. During this data transfer, the transmit shift register is clocked eight times by XMSRCLK = STORECLK, then 10 or 11 times by XSCLK (depending upon the jumper plug connection in the transmit bit counter) to clock the data from the shift register through the flip-flop. During the 10th or 11th XSCLK pulses, ones are loaded into the shift register to provide the appropriate stop bits for either 10- or 11-bit code. Figure 4-3 shows the logic making up the transmit shift register.

4.2.9 **CURRENT LOOP INTERFACE.** The current loop interface circuitry allows the module to transmit serial data (XMTD) to equipment using a 20-mA current loop interface. The current loop interface circuitry converts the TTL-level data into Mark/Space data for the transmit current loop.

4.2.10 **DIAGNOSTIC LOOP LOGIC.** The diagnostic loop logic consists of eight 2-to-1 selectors (in two packages) and three inverters. During normal data transfer to a device requiring an EIA interface, the diagnostic loop logic passes the output signals for the device to the EIA line drivers. When the diagnostic mode latch is set, diagnostic loop logic gates the EIA output signals to the input multiplexer for examination by the computer and gates ones to the EIA line drivers.

4.2.11 **EIA LINE DRIVERS.** The two packages of EIA line drivers convert the TTL-level signals at their inputs into signals having voltage levels compatible with EIA Standard RS-232C.

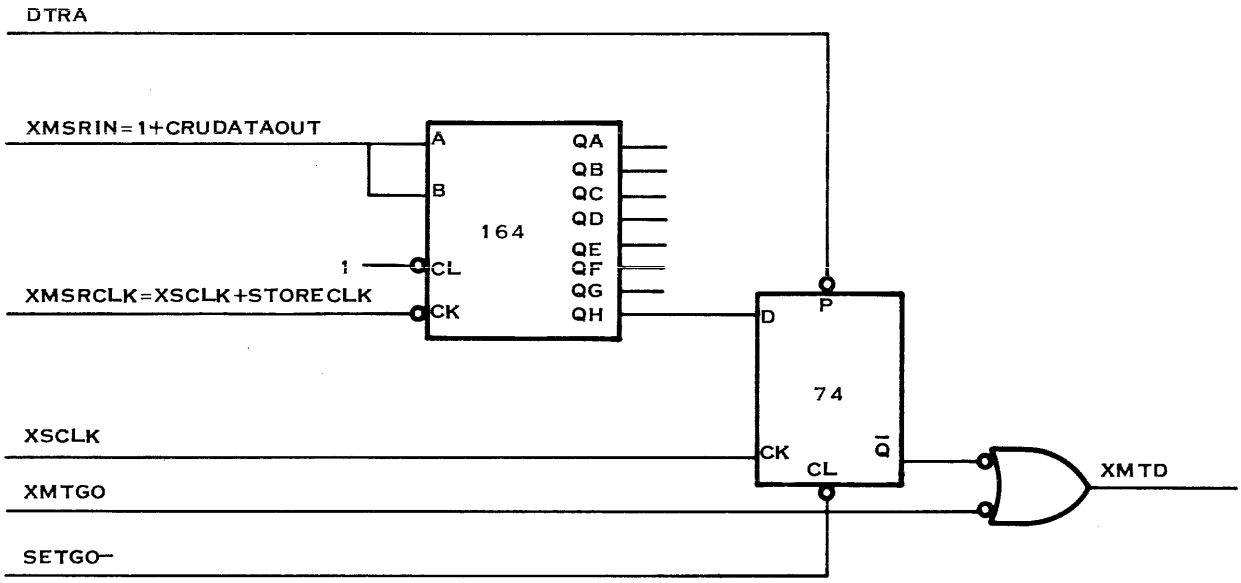

Figure 4-3. Transmit Shift Register Logic

4.2.12 **STATUS AND INTERRUPT LOGIC.** Combinational logic and several latches on the module provide status and interrupt information to the computer. The following paragraphs discuss that circuitry.

4.2.12.1 **Data Terminal Ready Latch.** The data terminal ready latch is a flip-flop that is reset by TILINE I/O Reset (TILORES-) from the 990 during the computer's power-up sequence or by a RSET instruction from the computer. When the data terminal ready latch is reset, it disables data transfer through the module. The data terminal ready flag is also reset whenever bit 9 of the CRU output word is logic 0 and the CRU address bits (CRUBIT,12-15) are set to 1001_2 (ADDS9- = 0). When the latch is set, it drives Data Terminal Ready (DTRE) high and enables the remainder of the module's circuitry for data transfer.

4.2.12.2 **Request To Send Latch.** The request to send latch is a flip-flop used to control the Request To Send (RTSE) signal to the peripheral device. During initialization, the request to send latch is set by the data terminal ready latch (DTRA) and drives RTSE low. During preparation to send data from the computer to the peripheral device, ADDS10- resets this latch and drives RTSE high.

4.2.12.3 **Write Request Flag.** The write request flag is a flip-flop used to produce an interrupt and a status signal. The flag is set whenever STPXCK- from the transmit bit counter is low signifying the end of a transmitted character, and reset by DTRA during initialization or by ADDS11-. When the write request flag is set while in use with an EIA device and the interrupt mask latch is not set, an interrupt is sent to the device, and the write request flag notifies the computer of its status via the multiplexer.

4.2.12.4 **Read Request Interrupt Logic.** The read request interrupt logic consists of a 4-bit binary counter and two flip-flops. During initialization, the output flip-flop is reset. During normal operation the logic is reset by ADDS12-. If the data terminal ready latch is set and ADDS12- is high when STPRCK- from the receive go latch goes low, the read request interrupt logic output flip-flop is set after a delay of one-half bit time (10-bit code) or one and one-half bit time (11-bit code). When reset, the read request interrupt logic produces an interrupt to the device (if the interrupt mask latch is not set) and provides its status to the computer via the multiplexer.

4.2.12.5 **New Status Flag.** The new status flag is made up of a flip-flop with an AND gate at each input (data and clock). The flag is set whenever Data Carrier Detect (DCDE) on the device input interface changes state or when Data Set Ready (DSRE) on that same interface goes low. The flag is reset whenever the data terminal ready latch is reset or when ADDS13- is low. When the new status flag is set, NSTFG- provides an interrupt to the device (if the interrupt mask latch is not set).

4.2.12.6 **Interrupt Mask Latch.** The interrupt mask latch is a flip-flop whose output is used to disable the CRUINT– signal to the computer. This latch is set during initialization by DTRA, or during normal operation by ADDS14-. When the interrupt mask latch is set, MASKINT- disables CRU Interrupt (CRUINT-). When reset, MASKINT- enables the interrupt merging logic.

4.2.12.7 **Diagnostic Mode Latch.** The diagnostic mode latch is a flip-flop that controls the operation of the diagnostic loop logic. The latch is set during initialization by DTRA, and is set and reset during normal operation by ADDS15-. When the diagnostic mode latch is set, DIAGM gates DSR-, DCD-, RCVD, and RCR- through diagnostic loop logic to the multiplexer and gates RTS, XMTD, DTR-, and RTS- to the EIA line drivers. When reset, the diagnostic mode latch gates DTR-, RTS-, XMTD, and RTS to the multiplexer and sends ones to the EIA line drivers.

4.2.12.8 **Interrupt Merging Logic.** Interrupt merging logic consists of three gates which perform the OR function for Write Request (WRQ-), Read Request (RRQ-), and New Status (NSTFG-) when the module is being used with an EIA device and the interrupt mask latch is reset.

4.2.13 **RECEIVE SHIFT CLOCK GENERATOR.** The receive shift clock generator consists of a 4-bit binary counter and four gates that produce, from DATACLK, Receive Shift Clock (RSCLK), a clock signal with a pulse width equal to that of DATACLK and a period 16 times as long as DATACLK's. The frequency of RSCLK is equal to the receive baud rate, and the active pulse is delayed by one-half bit time from the time the generator begins to count DATACLK. The receive shift clock generator is active when the receive go latch is set and data is being received from a peripheral device. The receive shift clock generator clocks the receive bit counter, the receive go latch, and the receive shift register.

4.2.14 **RECEIVE BIT COUNTER.** The receive bit counter consists of a 4-bit binary counter and two gates that are used to stop the Receive Shift Clock (RSCLK) from clocking data from the device into the receive shift register. Whenever RCVDE from the device is low, the receive shift clock generator and receive bit counter are activated. After one-half bit time, the receive bit counter sets the receive go flag (RSCLKA) allowing the receive shift clock generator and receive bit counter to remain active independently of RCVDE. After counting 10 or 11 RSCLKA pulses, the receive bit counter disables the receive go flag and terminates the operation for that character.

4.2.15 **RECEIVE GO FLAG.** The receive go flag is made up of the circuitry shown in figure 4-4. Whenever RCVDDI (RCVDE from the device) is low, RCVEN is high and activates the receive shift clock generator and the receive bit counter. Upon receipt of RSTOPA- (11-bit code)

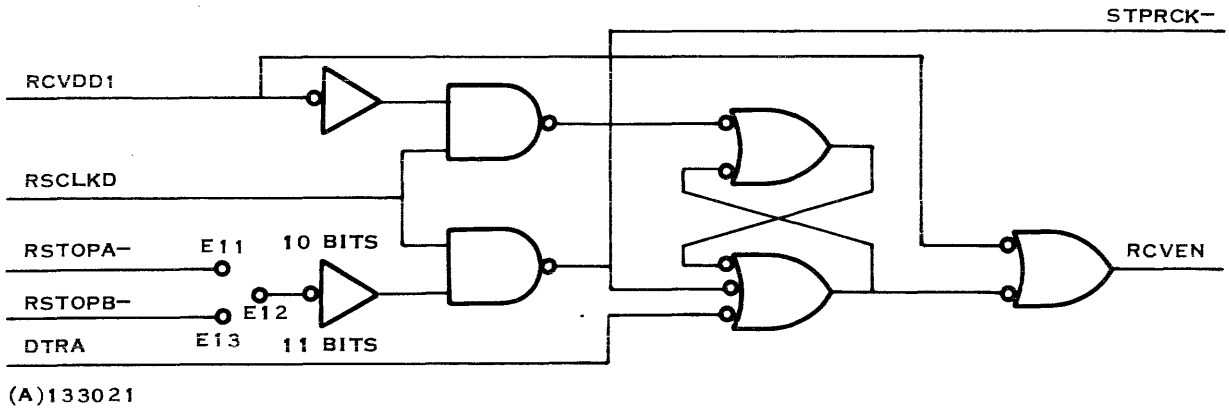

Figure 4-4. Receive Go Latch Logic Diagram

or RSTOPB- (10-bit code), the receive go flag is reset after one-half bit time elapses by RSCLKA. When reset, STPRCK- resets the write request flag, the read request interrupt logic, and the timing error flag. The receive go flag is also reset by DTRA during initialization or a software-initiated clear operation.

4.2.16 **TTY/EIA RECEIVE SWITCH.** The TTY/EIA receive switch performs the gating function to produce Received Data (RCVD) whenever either TTY or EIA data is being received by the module. A jumper within this logic enables one, and only one, type of data to be received by the module at a given time.

4.2.17 **EIA LINE RECEIVERS.** The EIA line receivers convert input signals compatible with EIA Standard RS-232C into TTL-compatible logic levels to be used by the module.

4.2.18 **RECEIVE TRANSITION DETECTOR.** The receive transition detector is a retriggerable monostable multivibrator that produces a low-active pulse on one of its outputs (SNST1- or SNST2-) whenever Data Set Ready (DSRE) or Data Carrier Detect (DCDE) changes states. The outputs of the receive transition detector are used to set the new status flag.

4.2.19 **RECEIVE SHIFT REGISTER.** The receive shift register is an 8-bit parallel-out shift register. When clocked by RSCLK from the receive shift clock generator at the center of each bit period, the receive shift register accepts one bit of serial data being transmitted by the peripheral device and places it on the lines to the receive buffer register (RVSR,0-7).

4.2.20 **RECEIVE BUFFER REGISTER.** The receive buffer register is a flip-flop register that accepts the eight bits of data from the receive shift register (RVSR,0-7) in parallel and provides them to the multiplexer (RVBR,0-7) when gated by LDBR- at the end of 10 or 11 bit periods according to the code selected by the jumper plug in the receive go flag.

4.2.21 **MULTIPLEXER.** The multiplexer is a 16-to-1 data selector that passes one of its inputs to an output gate each time it is strobed by IMODSELA- from the computer. The input passed is selected by the CRU address bits, CRUBIT,12-15. Table 4-3 lists the input passed to the output gate for each binary combination of CRUBIT,12-15. Once passed to the output of the multiplexer, the data is gated to the computer if IMODSELA- = 0.

4.2.22 **TIMING ERROR FLAG.** The timing error flag is a flip-flop that is set whenever the read request interrupt logic is set and another character is presented to the receive buffer register, indicating that an attempt has been made to load a second character into the buffer before the first character has been sent to the computer. During initialization, the timing error flag is reset by DTRA.

Table 4-3. Multiplexer Output for CRUBIT,12-15

CRUBIT,12-15	Output
0000	RVBR7
0001	RVBR6
0010	RVBR5
0011	RVBR4
0100	RVBR3
0101	RVBR2
0110	RVBR1
0111	RVBR0
1000	XMTGO
1001	TIMERR
1010	RCRDI
1011	WRQ
1100	RRQ
1101	DCDDI
1110	DSRDI
1111	INT

4.3 DETAILED INTERFACE DISCUSSION

Figure 4-5 shows the interfaces between the Full Duplex TTY/EIA Module and a Model 990 Computer and both a current-loop (TTY) device and an EIA device. All the interfaces are shown in one diagram even though the module can be used only with a current-loop device or an EIA device for a given set of jumper plug connections. The following paragraphs describe the signals on the module's interfaces.

4.3.1 FULL DUPLEX TTY/EIA MODULE-TO-MODEL 990 COMPUTER INTERFACE. The following paragraphs describe the TTY/EIA Module-to-Model 990 Computer interface.

4.3.1.1 CRUDATAOUT. CRUDATAOUT is serial information from the computer to the module. The 16 bits of data represented by CRUDATAOUT are addressable, and provide both data and control signals for the module. Figure 4-6 illustrates the information contained on CRUDATAOUT.

Data Character. The first eight bits of information are data bits to be transmitted to the peripheral device.

Data Terminal Ready (DTR). Logic 1 sets the data terminal ready latch.

Request To Send (RTS). Logic 1 sets the request to send latch.

Clear Write Request (CLRWRQ). Logic 0 or 1 resets write request flag.

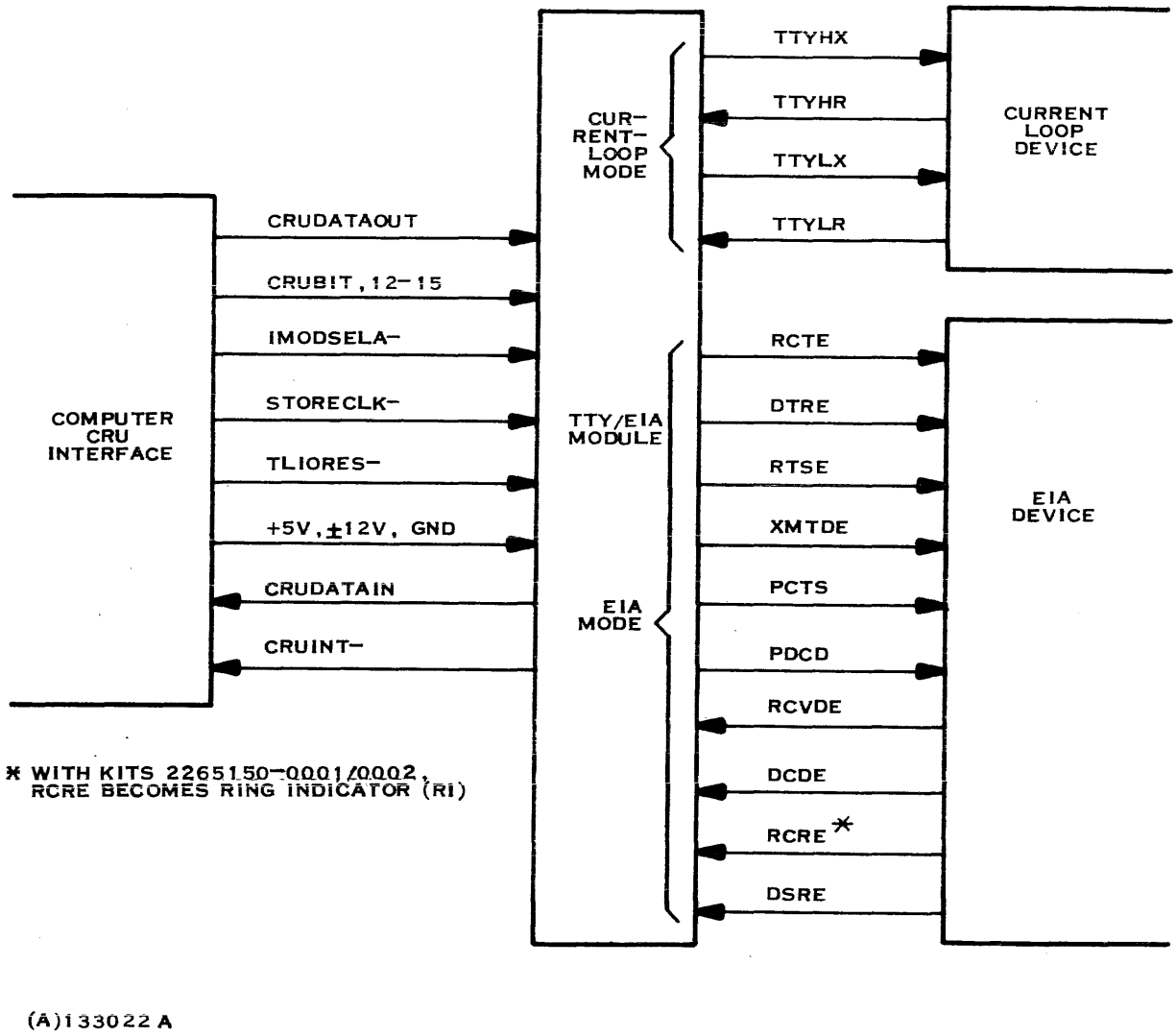

Figure 4-5. Full Duplex TTY/EIA Module Interface Diagram

Clear Read Request (CLRRRQ). Logic 0 or 1 resets read request interrupt logic.

Clear New Status Flag (CLRNSF). Logic 0 or 1 resets new status flag.

Enable Interrupts. Logic 1 sets interrupt mask latch.

Diagnostic Mode. Logic 1 sets diagnostic mode latch.

4.3.1.2 **CRUBIT,12-15.** CRUBIT,12-15 are the CRU bit select field of the 12-bit address word from the computer. They are used by the module to activate the latches and logic mentioned in paragraph 4.3.1.1.

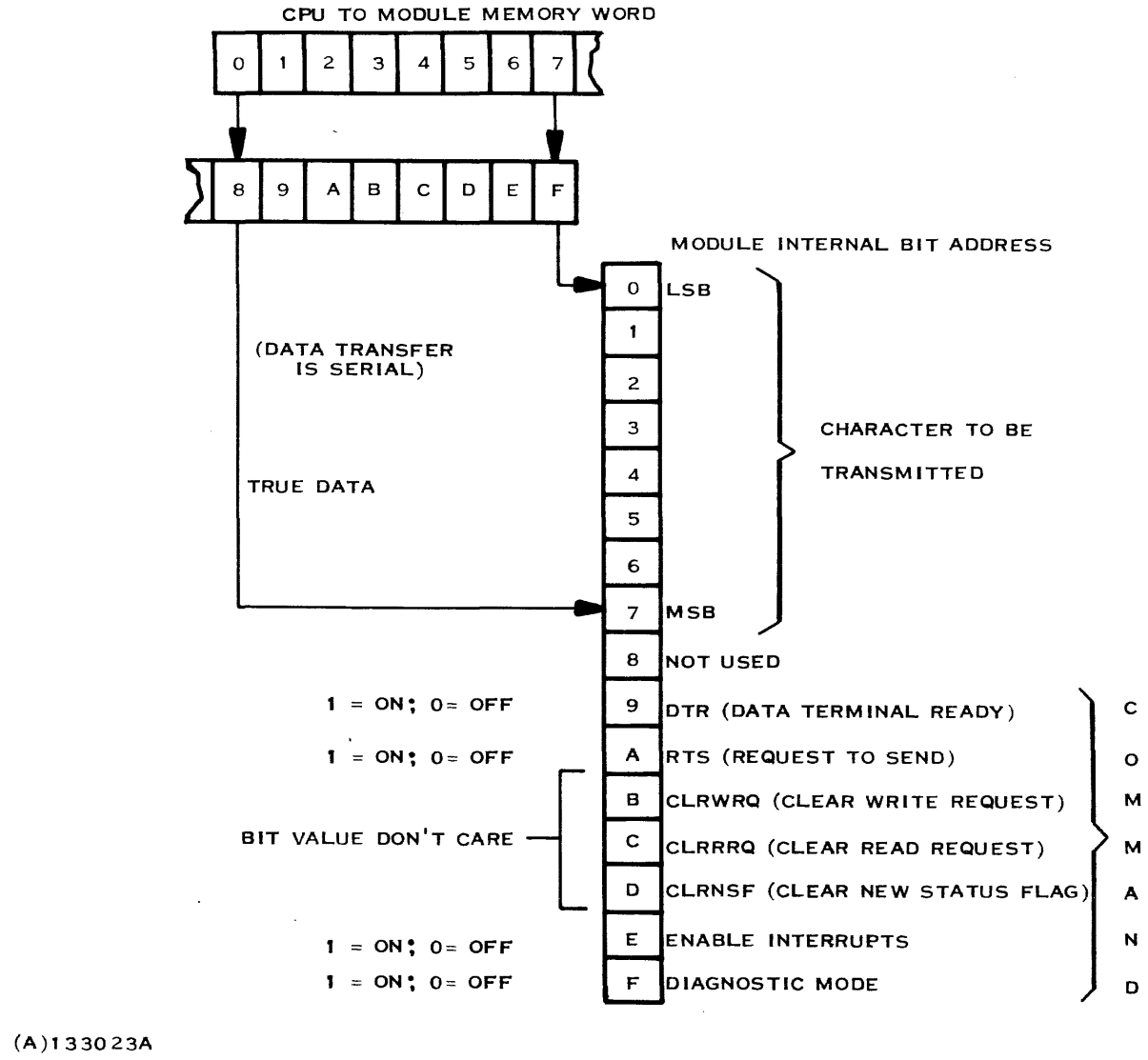

Figure 4-6. Full Duplex TTY/EIA Module Addressable Input Lines

4.3.1.3 **IMODSELA-**. IMODSELA- is the address module select of a CRU chassis slot. IMODSELA- is wired into the computer backpanel and addressed by software. IMODSELA- is a low-active signal that enables the module to send and receive information between the computer and a peripheral device.

4.3.1.4 **STORECLK-**. STORECLK- is a low-active pulse from the computer that indicates to the module that the operation is a write operation (SETB or LDCR). STORECLK- transfers the data on CRUDATAOUT to the module serially.

4.3.1.5 **TLIORES-**. TLIORES- is the TILINE I/O reset signal. It is low-active and is generated either by an RSET instruction or during the computer's power-up sequence.

4.3.1.6 **CRUDATAIN.** CRUDATAIN is serial information from the module to the computer. The 16 bits of information represented by CRUDATAIN are addressable and provide data, status, and interrupts to the computer. Figure 4-7 illustrates the information contained by CRUDATAIN.

Data Character. The first eight bits of information are data bits to be transmitted to the computer.

Transmit In Progress (XMTING). Logic 1 active.

Timing Error (TIMERR). Logic 1 active.

Reverse Channel Receive (RCR). Logic 1 active.

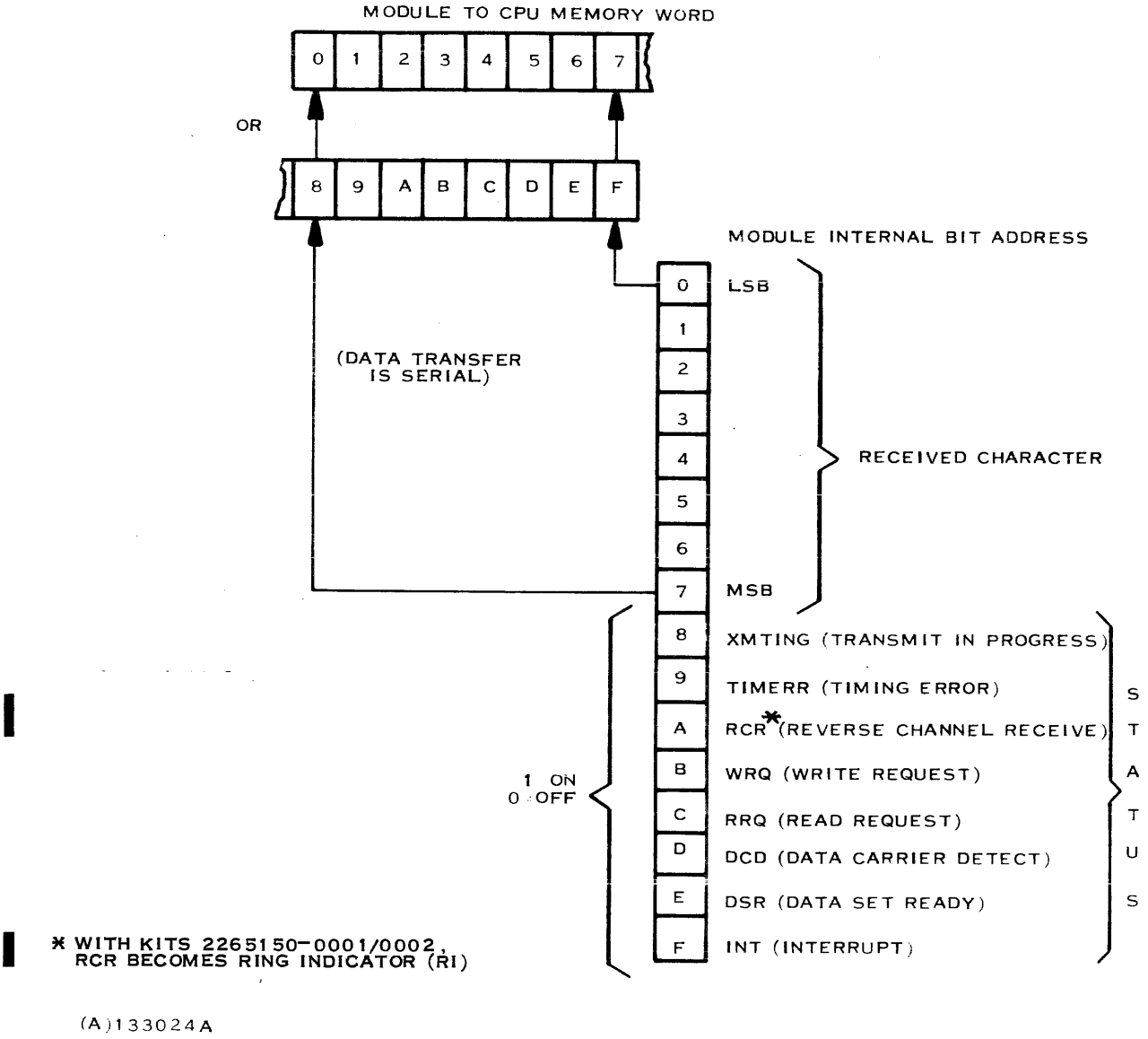

Figure 4-7. Full Duplex TTY/EIA Module Addressable Output Lines

Write Request (WRQ). Logic 1 active.

Read Request (RRQ). Logic 1 active.

Data Carrier Detect (DCD). Logic 1 active.

Data Set Ready (DSR). Logic 1 active.

Interrupt (INT). Logic 1 active.

The CRUDATAIN signals should be recognizable as the outputs of the multiplexer described in paragraph 4.2.21.

4.3.1.7 **CRUINT-.** CRUINT- is the logical OR of Read Request, Write Request, and New Status and is always active (low) when bit F of the output word is set.

4.3.2 **FULL DUPLEX TTY/EIA MODULE-TO-CURRENT LOOP DEVICE INTERFACE.** The current loop interface consists of two pairs of lines. TTYHX and TTYLX from the transmit loop, and TTYHR and TTYLR from the receive loop. A closed-loop current of 20 mA is defined as a "marking" condition, or logic 1. Any break in this circulating current is sensed as a "break" condition, or logic 0.

4.3.3 **FULL DUPLEX TTY/EIA MODULE-TO-EIA DEVICE INTERFACE.**

4.3.3.1 **Reverse Channel Transmit (RCTE).** Reverse Channel Transmit is used only when the module interfaces with a Bell 202 (C or D) data set or its equivalent. RCTE directs the data set to turn on/off the reverse channel carrier.

4.3.3.2 **Data Terminal Ready (DTRE).** Data Terminal Ready indicates to the peripheral device that the computer is ready to transmit or receive data. When the peripheral device is equipped for automatic answering of incoming calls, the off condition of DTRE prevents the data set from answering calls.

4.3.3.3 **Request To Send (RTSE).** Request To Send establishes the transmit condition for a Bell 103F data set. RTSE simulates Data Carrier Detect for direct interface to the terminal. Request To Send is not used with a Bell 103A data set.

4.3.3.4 **Transmitted Data (XMTDE).** Transmitted Data is the serial data from the computer for the device.

4.3.3.5 **Pseudo Clear To Send (PCTS).** Pseudo Clear To Send is high whenever the module's power is active and provides a simulated Clear To Send signal to the peripheral.

4.3.3.6 **Pseudo Data Carrier Detect (PDCD).** Pseudo Data Carrier Detect is high whenever the module's power is active and provides a simulated Data Carrier Detect to the peripheral.

4.3.3.7 **Received Data (RCVDE).** Received data is the serial data from the device to be transmitted to the computer.

4.3.3.8 **Data Carrier Detect (DCDE).** Data Carrier Detect, when high, indicates that the peripheral has detected a carrier. When directly interfaced to the peripheral, DCDE reflects the Request To Send signal.

4.3.3.9 **Reverse Channel Receive (RCRE)***. Reverse Channel Receive indicates that the peripheral device is ready to receive data. RCRE is used only when interfacing with a Bell 202 data set with reverse channel option.

4.3.3.10 **Data Set Ready (DSRE)**. Data Set Ready indicates that the peripheral is operative.

4.4 MODULE OPERATION

4.4.1 PREPARATION TO TRANSMIT. Prior to any character transmission, a typical I/O routine uses a SBO instruction to develop the DTRE and RTSE signals. The SBO instruction that develops DTRE places a logic 1 on CRUDATAOUT, sets CRUBIT,12-15 to 1001_2, and issues IMODSELA- and STORECLK-. This action sets the data terminal ready latch and drives DTRE to EIA logic 1. A second SETB instruction, identical to the first except that CRUBIT,12-15 = 1010_2, resets the request to send latch and drives RTSE to EIA logic 1.

4.4.2 DATA TRANSMISSION. When the I/O routine determines that the attached peripheral device is ready to accept a character, an LDCR instruction is issued to transmit an 8-bit character from computer memory to the transmit shift register. The LDCR instruction directs the computer to do the following: place eight bits of data serially on CRUDATAOUT, accompanying each bit with a STORECLK- pulse and an address (CRUBIT,12-15) that begins with 0000_2 and increments by one for each successive bit; issue IMODSELA- to enable the module. Upon receipt of the eighth bit of data (with its accompanying address and clock) the transmit go flag is set and enables the transmit shift clock generator, the transmit bit counter, and the transmit shift register. After the eighth bit is shifted out of the shift register into the transmit shift register's output flip-flop, one or two (depending on the code length) more clock pulses clock ones into the shift register to be clocked out as stop bits. After the last stop bit has been shifted out, the transmit go flag is reset, disabling the transmit shift clock generator, transmit bit counter, and transmit shift register. The write request flag is set to notify the computer that the module is ready to accept the next character.

4.4.3 INTERRUPTS. The interrupt logic on the module monitors the write request flag, read request interrupt logic, and new status flag for set conditions. The computer uses the status of these circuits to control the starting and stopping of the applicable I/O routines to ensure efficient use of computer time. Write Request indicates that a new character can be transmitted from the computer to the peripheral. Read Request indicates that the module has a character ready for transmission to the computer. New Status indicates a transition in the state of DSRE or DCDE from the peripheral.

4.4.4 DATA RECEPTION. The receiving data input is normally held in the "mark" (logic 1) condition. The occurrence of a "space" condition on the line activates the receive shift clock generator and the receive bit counter. The input line is examined after one-half bit time to determine whether a start bit has been received. If a start bit has been received, the receive go flag is set allowing the receive shift clock generator and receive bit counter to remain active independently of the receiving data input. The received data is shifted into the receive shift register at the center of each bit period. The ninth shift pulse loads the receive buffer register (parallel). At the beginning of the last (10th or 11th) shift pulse, the receive go flag is reset which terminates the character reception. The receive go flag sets the read request interrupt logic to inform the computer that a character is on the receive buffer register's output. The computer then addresses the multiplexer with successive CRUBIT,12-15 combinations to fetch the character, one bit at a time.

*With kits 2265150-0001/0002, RCRE becomes Ring Indicator (RI) signifying a remote station is calling the host.

4.4.5 TESTING. The Full Duplex TTY/EIA Module has the capability of gating the EIA outputs from the computer back to the computer for examination. This is accomplished by setting the diagnostic mode latch and addressing the proper input lines of the multiplexer.

SECTION V

MAINTENANCE

5.1 GENERAL

This section describes the depot maintenance philosophy for the TTY/EIA Terminal Interface Module and provides troubleshooting procedures to allow fault isolation to the component level. Component replacement procedures are described in *Model 990/4 Computer System Depot Maintenance Manual* (Manual Number 945403-9701) and *Model 990/10 Computer System Depot Maintenance Manual* (Manual No. 945404-9701).

5.2 MAINTENANCE PHILOSOPHY

Depot maintenance for the TTY/EIA Terminal Interface Module is based on the use of a hot mock-up system incorporating a Model 990 Computer, a Model 990 Maintenance Unit, and a combination dual-trace oscilloscope/digital multimeter as shown in figures 5-1 and 5-2.

Suspect modules from the field maintenance repair facilities are serviced by placing the module on an extender board in the hot mock-up computer chassis. Initial testing is controlled by a diagnostic program, either the Full Duplex TTY/EIA Interface Module Test (TTYEIA, part no. 945453), or the Remote Dial-Up Test (REMEIA, part no. 2250242). TTYEIA performs a complete check of the TTY/EIA interface module; REMEIA is used with kits 2265150-0001/0002 to check communications between the host computer and remote terminal connected with the standard TTY/EIA interface module and cable 2265151. Either diagnostic may be read into computer memory from a cassette transport located in a Model 990 Maintenance Unit or a Model 733 ASR Terminal. Resulting error messages are printed by the teleprinter. Refer to the *Model 990 Computer Diagnostic Handbook* (Manual Number 945400-9701) for detailed operating procedures for this diagnostic.

Faults are then isolated to the component level by establishing and tracing scoping loops that isolate the circuits indicated by the diagnostic testing.

5.3 SPECIAL TEST EQUIPMENT

The special test equipment required to perform depot maintenance on the TTY/EIA Terminal Interface Module includes:

- Model 990 Computer hot mock-up system
- Model 990 Maintenance Unit

Operating procedures for the special test equipment are provided in *Model 990/4 Computer System Depot Maintenance Manual* (Manual No. 945403-9701) and *Model 990/10 Computer System Depot Maintenance Manual* (Manual No. 945405-9701). Operating procedures for the oscilloscope/multimeter are contained in the manufacturer-supplied user manual(s) for the equipment.

5.4 TROUBLESHOOTING PROCEDURES

Upon receipt of a defective TTY/EIA Terminal Interface Module from a field maintenance repair facility, inspect the module for visible indications of damage (loose or missing components or jumpers, breaks in the board or etched circuits, foreign materials which may have caused short circuits, etc.).

If no visible indications are found, place the module on an extender card in a hot mock-up system and perform the procedures listed in table 5-1.

5.4.1 **SCOPING LOOPS.** A scoping loop is a short repetetive software program which establishes and maintains a set of conditions in the circuitry under observation so that an error of brief duration may be observed and isolated. Once a malfunction has been discovered, a scoping loop is entered into the hot mock-up computer from the programmer panel on either the computer chassis or the Model 990 Maintenance Unit. The scoping loop permits data to be written into or read from a desired memory location or block of memory locations. Dynamic troubleshooting may then be performed in accordance with the procedures in table 5-1.

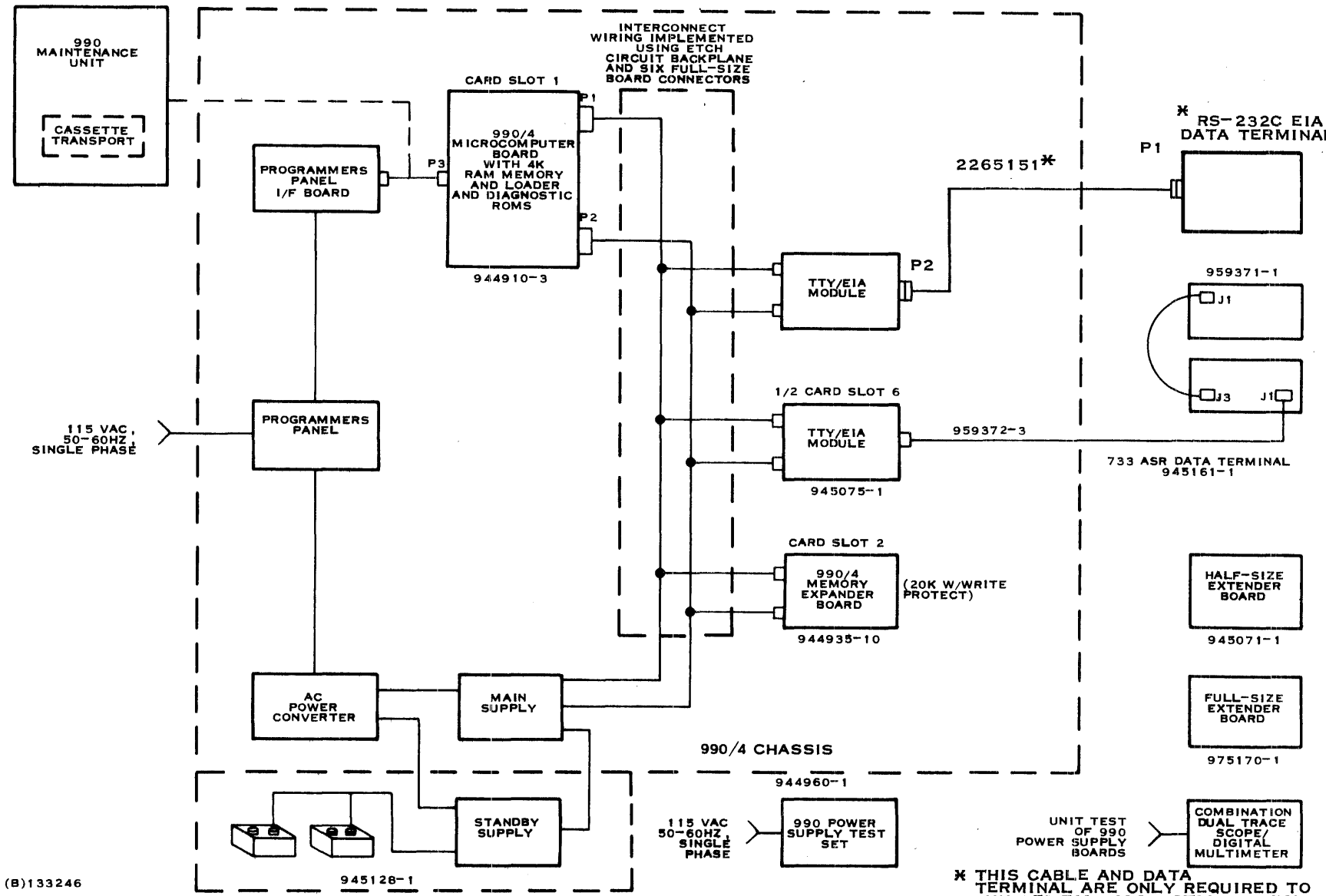

Figure 5-1. Model 990/4 Computer Hot Mock-up System

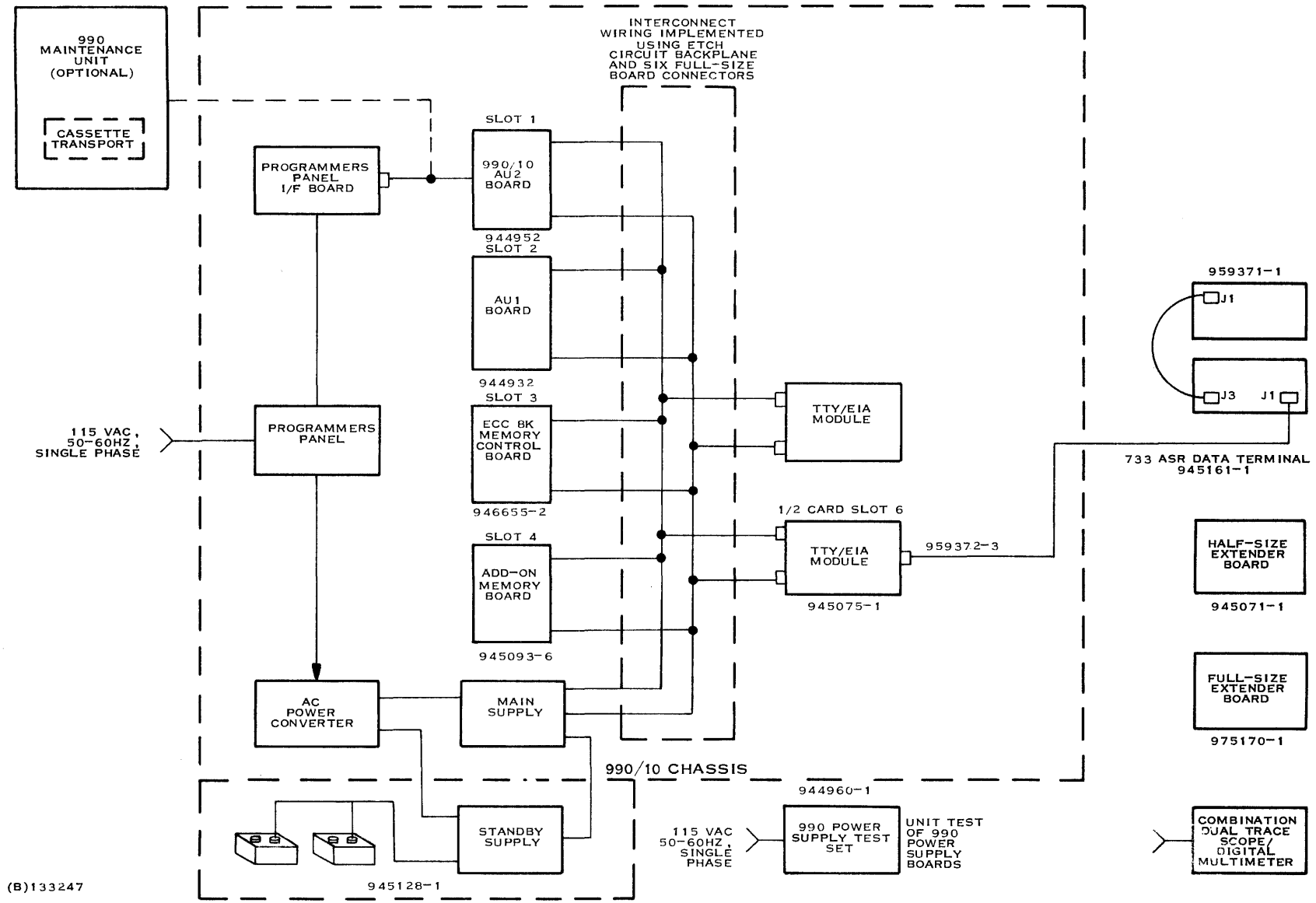

Figure 5-2. Model 990/10 Computer Hot Mock-up System

Table 5-1. Troubleshooting Procedures

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	DTRE=0 when CRU output bit 9 set	Address decoder or data terminal ready flag	Set up scoping loop to set Data Terminal Ready (CRU output bit 9)	DTRE=1 at U31-6	Check circuit beginning at U31-6 through U31, U40, U24, U26, U17, U35, U12, U37, U38. Replace faulty component(s)
2	RTSE=0 or RCTE=0 when CRU output bit A set	Address decoder or request to send flag	Set up scoping loop to set Request To Send (CRU output bit A).	RTSE=1 at E26, RCTE=1 at U31-7	Check circuit beginning at E26 and U31-7 through U31, U32, U40, U24, U17. Replace faulty component(s).
3	TTYLX=0 or XMTDE=0 after character sent by computer	Transmit go flag	Set up scoping loop to send a character to terminal.	XMTGO sets to 1 on 8th character bit (see figure 5-3).	Check circuit beginning at U21-5 through U21, U34, U28, U20. Replace faulty component(s).
4	Bad data to terminal	Oscillator	Apply power to module.	4-MHz square wave at U10-6.	Check OSCLK at U10-6. Check circuit. Replace faulty component(s).
		Baud rate clock	Apply power to module	See table 5-2.	Check circuit beginning at U29-10 through U29, U2, U3, U4. Replace faulty component(s).

Table 5-1. Troubleshooting Procedures (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
		Transmit shift clock generator	Set up scoping loop to send a character to terminal.	See figure 5-4.	Check circuit back from U14-12 through U14, U6. Replace faulty component(s).
		Transmit bit counter	Set up scoping loop to send a character to terminal.	See figure 5-5.	Check circuit back from U13-12 through U13, U5. Replace faulty component(s).
		Transmit shift register	Set up scoping loop to send a character to terminal.	See figure 5-6.	Check circuit back from U21-8 through U21, U11, U20. Replace faulty component(s).
5	Bad data transfer from terminal	Link driver receiver	Actuate terminal	RCVD=0	Check circuit back from U41-8 through U41, U30. Replace faulty component(s).
		Loop back logic	Set up scoping loop to read back a CRU character	RCVEN=1	Check circuit back from U35-11 through U35, U39, U20. Replace faulty component(s).
		Receive shift clock generator	Set up scoping loop to read back a CRU character	See figure 5-7.	Check signals in figure 5-7. Replace faulty component(s).
		Receive bit counter	Set up scoping loop to read back a CRU character.	See figure 5-8.	Check signals in figure 5-8. Replace faulty component(s).

Table 5-1. Troubleshooting Procedures (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
6	No data from terminal	Multiplexer, receive shift/buffer registers	Set up scoping loop to read back a CRU character.	CRUDATAIN= CRUDATAOUT	Check circuit beginning at U33-11 through U33, U7, U8, U1, U9. Replace faulty component(s).
7	No write request interrupt	Address decoder, write request flag	Set up scoping loop to set Clear Write Request (CRU output bit B).	WRQ=0	Check circuit beginning at U18-9 through U18, U17, U37, U35, U12, U26.
8	No read request interrupt	Address decoder, read request interrupt logic	Set up scoping loop to set Clear Read Request (CRU output bit C).	RRQ=1	Check circuit beginning at U25-9 through U25, U19, U25, U23, U17. Replace faulty component(s).
9	No new status interrupt	Address decoder, new status flag	Set up scoping loop to set Clear New Status Flag (CRU output bit D)	NSFTG¬=1	Check circuit beginning at U22-6 through U22, U23, U15, U39. Replace faulty component(s).

Table 5-2. Baud Rate Clock Signals

Signal	Location	Pulse Width	Period
OSCLK	U10-6	125 nsec	250 nsec
MOD13CRY	U4-15	125 nsec	1.75 μsec
DATACLK (9600 BAUD)	U3-14	1.75 μsec	3.5 μsec
DATACLK (4800 BAUD)	U3-13	3.5 μsec	7 μsec
DATACLK (2400 BAUD)	U3-12	7 μsec	14 μsec
DATACLK (1200 BAUD)	U3-11	14 μsec	28 μsec
MOD11CRY (ALL OTHER)	U3-15	1.75 μsec	28 μsec
MOD11CRY (110 BAUD)	U3-15	1.75 μsec	21 μsec
DATACLK (300 BAUD)	U2-13	56 μsec	114 μsec
DATACLK (110 BAUD)	U2-11	228 μsec	456 μsec

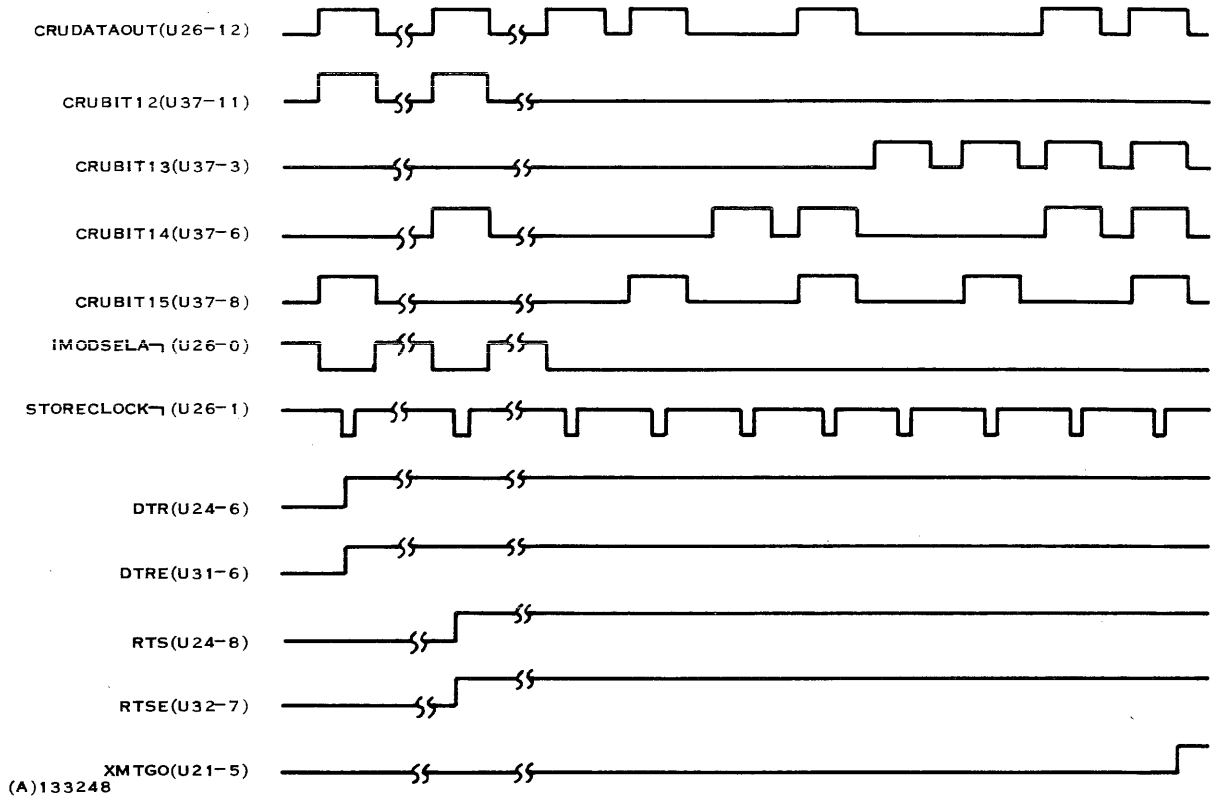

Figure 5-3. Transmit Go Flag Timing

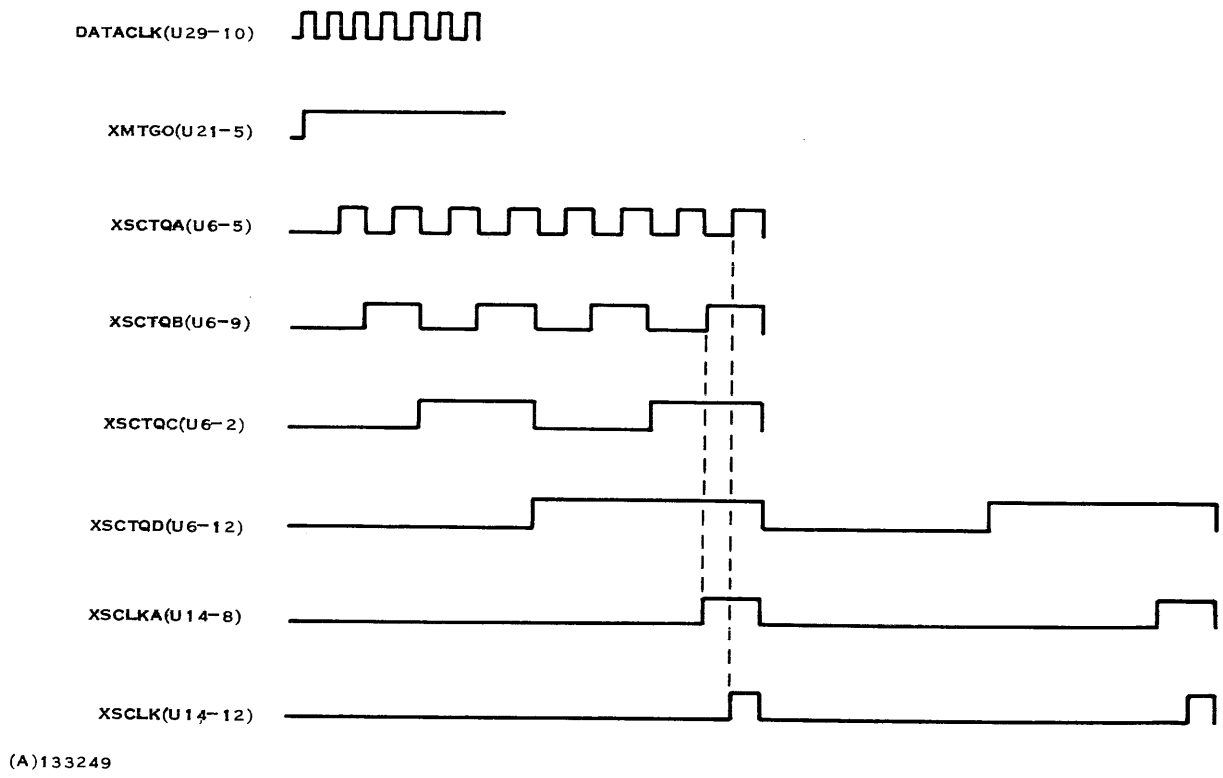

Figure 5-4. Transmit Shift Clock Generation

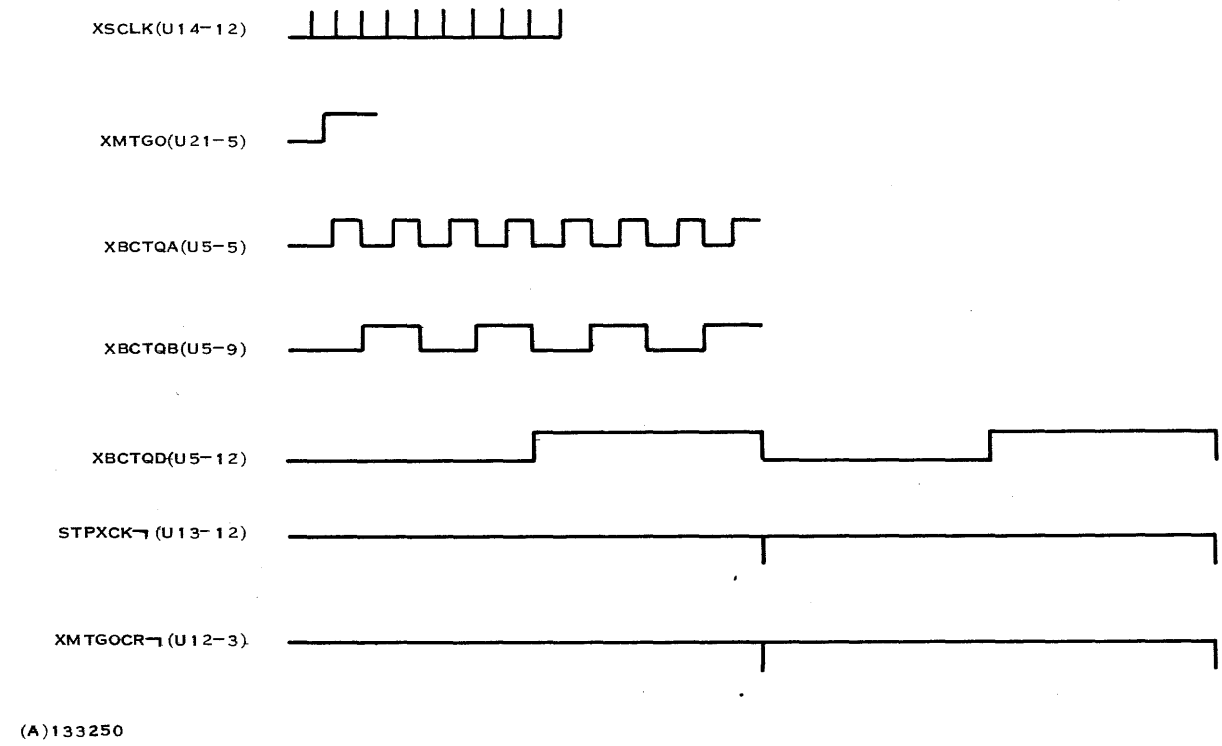

Figure 5-5. Transmit Bit Counter Signals

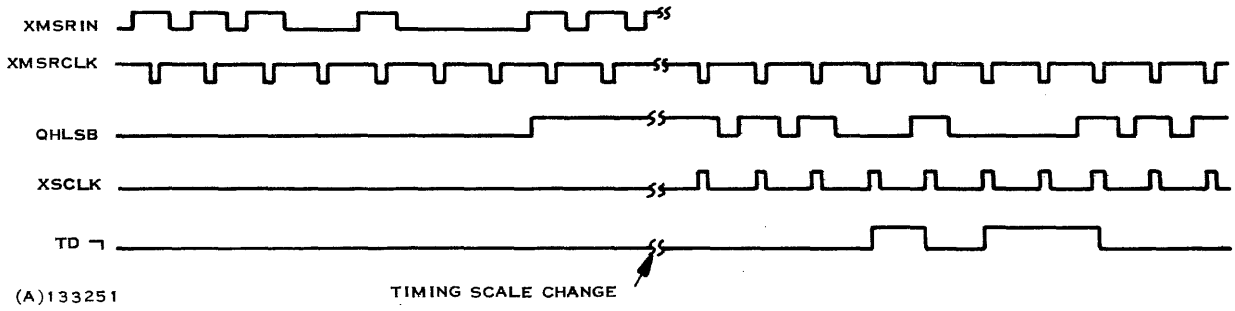

Figure 5-6. Transmit Shift Register Signals

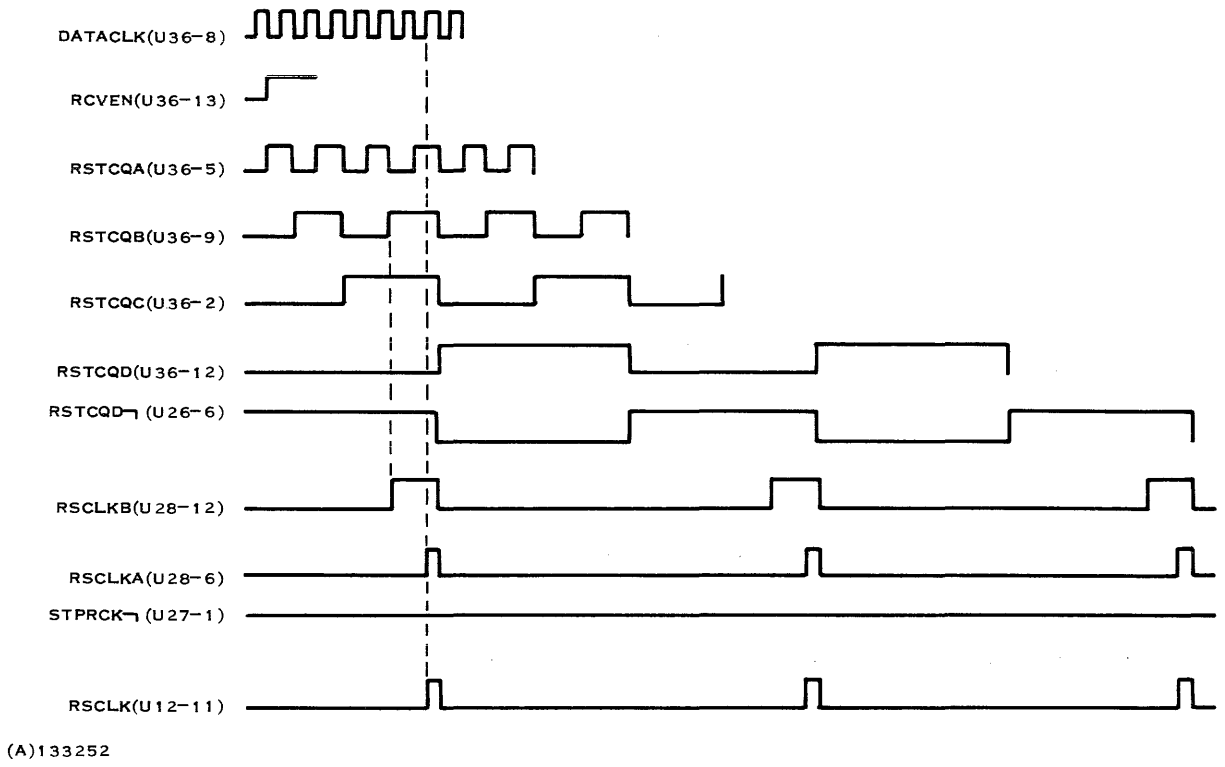

Figure 5-7. Receive Shift Clock Signals

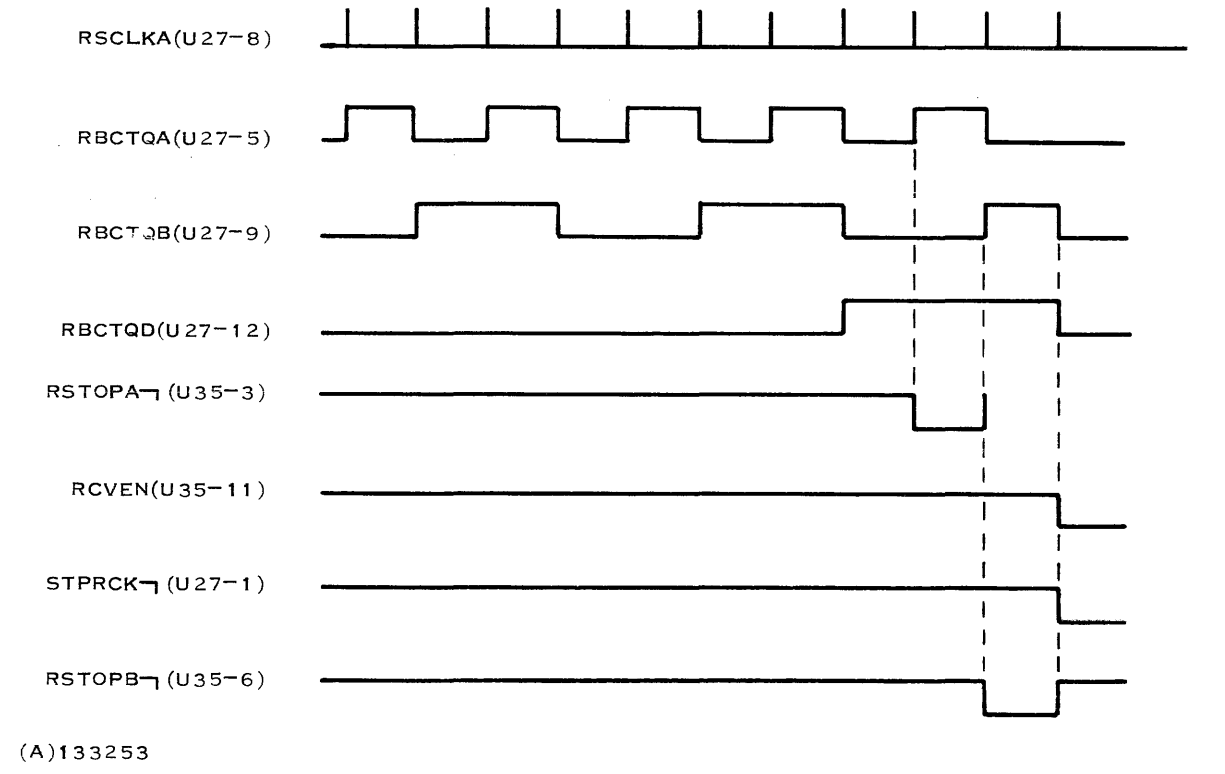

Figure 5-8. Receive Bit Counter Signals

ALPHABETICAL INDEX

INTRODUCTION

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections - References to Sections of the manual appear as "Section x" with the symbol x representing any numeric quantity.
- Appendixes - References to Appendixes of the manual appear as "Appendix y" with the symbol y representing any capital letter.
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- Tables - References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number:

  Tx-yy

- Figures - References to figures in the manual are represented by the capital letter F followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the figure). The second character is followed by a dash (-) and a number:

  Fx-yy

- Other entries in the Index - References to other entries in the index are preceded by the word "See" followed by the referenced entry.

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