TEXAS INSTRUMENTS

Improving Man's Effectiveness Through Electronics

Block Transfer Controller

Maintenance Manual

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PREFACE

This manual provides information and instructions necessary to enable maintenance personnel to install, operate and maintain peripheral device controllers that use the Block Transfer Controller (BTC). This manual consists of seven sections and an Alphabetical Index. A brief description of each section follows.

Section I General Description–This section contains a brief functional and physical description of the BTC and its relationship to a device controller and a CPU.

Section II Installation–This section contains a general installation procedure. Address information and preliminary testing information is also given.

Section III Operation and Programming–This section contains general information about the instructions and list words used for communication. Programming examples are also given.

Section IV Theory of Operation–This section contains detailed interface data and the theory of operation of the BTC.

Section V Maintenance–This section contains a fault isolation technique to aid in isolating problems within the BTC.

Section VI Parts List–This section contains assembly drawings and parts lists for the BTC circuit boards.

Section VII Diagrams–This section contains the logic diagrams for the BTC circuit boards. Integrated circuit data for the individual circuits used is also contained in this section.

Reference Documents–The following documents supplement the information contained in this manual.

Title	Part Number
Model 960/980 Computers Direct Memory Access Channel Manual	966312-9701
Model 960/980 Computers Direct Memory Access Channel Controller Manual	966312-9702

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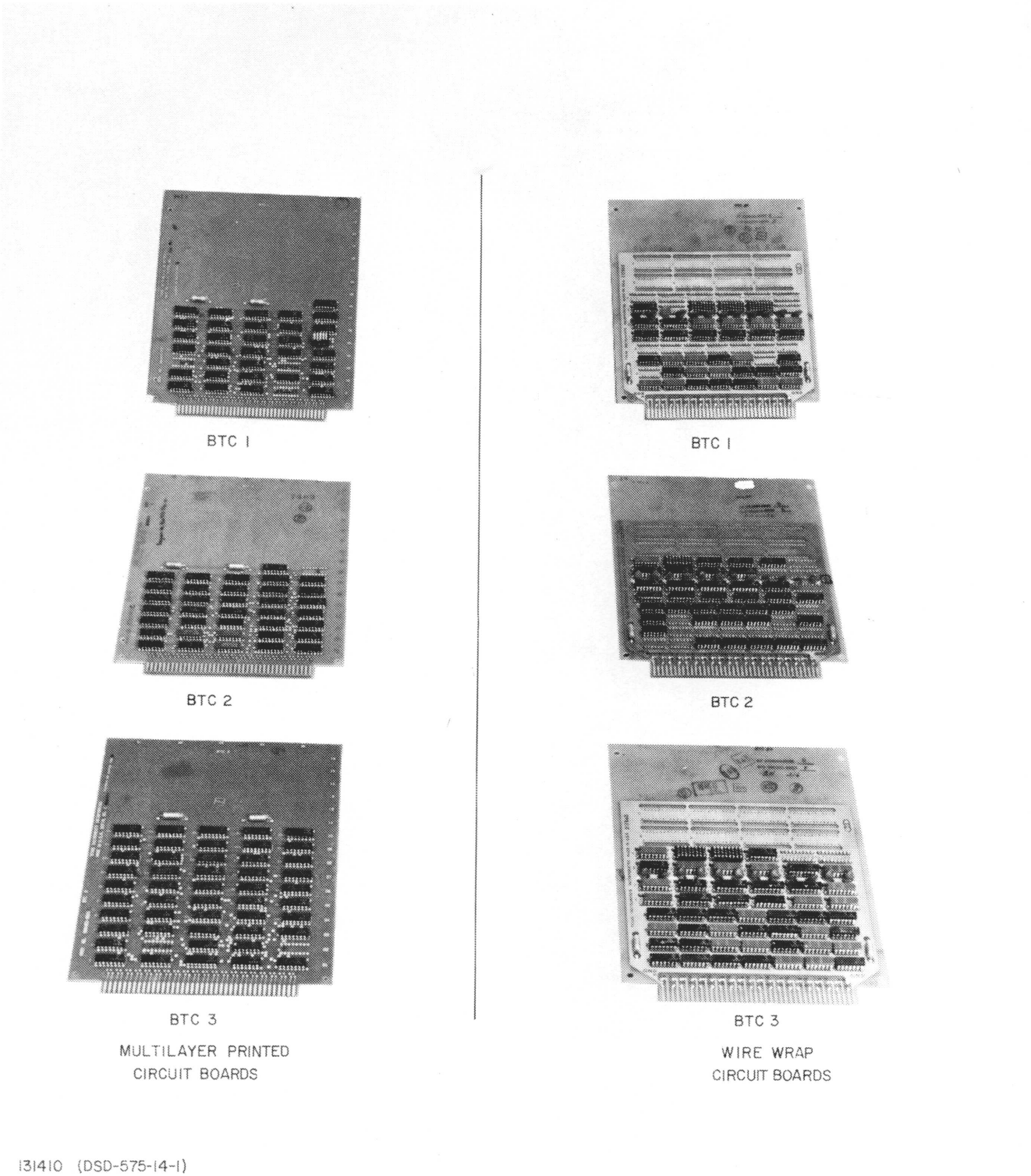


Figure 1-1. Block Transfer Controller

SECTION I

GENERAL DESCRIPTION

1.1 GENERAL

This section provides a brief functional and physical description of the Block Transfer Controller (BTC) shown in figure 1-1. The relationship of the BTC to other components of a Direct Memory Access (DMA) system for either a Model 960 or 980 computer is shown. Characteristics for the BTC are also given.

1.2 FUNCTIONAL DESCRIPTION

The BTC provides direct access to CPU memory for high-speed peripheral devices. The BTC is part of a peripheral controller which consists of a BTC for CPU interface and a device controller for peripheral interface. A block diagram of a typical peripheral controller is shown in figure 1-2. The BTC performs routine tasks such as CPU command and monitoring, list acquisition, memory management, status storage, interrupt control, data word counting, and data buffering as directed by the device controller. Figure 1-3 illustrates the use of a BTC in single controller and multiple controller applications.

1.3 PHYSICAL DESCRIPTION

A BTC consists of either three multilayer printed circuit boards or three wire wrap circuit boards as shown in figure 1-1. The two types are directly interchangeable. All interface signal lines to and from the BTC come through 80-pin connectors at the bottom of the circuit boards.

1.4 CHARACTERISTICS

The characteristics of a BTC are summarized in table 1-1.

1.4.1 DATA TRANSFER RATE. The maximum data transfer rate through a BTC is 500,000, 16-bit words per second. During a list acquisition the BTC takes four sequential memory cycles. During block transfers of data the BTC will allow the device controller to request only every other memory cycle. Consequently, only half of the CPU DMAC interface data transfer rate of 1,000,000 words per second can be used by a single peripheral controller. Typically, the data transfer rate of a peripheral controller will be less than 500,000 words per second due to other considerations such as memory refresh, list acquisitions for chaining, and initialization and memory cycle requirements of other peripherals. When two or more peripheral controllers are attached to the DMAC interface through the DMAC expander, the maximum data transfer rate of the CPU is reduced to approximately 800,000 words per second, effectively reducing the data transfer of the BTC in each peripheral controller to 400,000 words per second. When two or more peripheral controllers are attached to the DMAC expander and data transfer rates approach 800,000 words per second, CPU memory cycles will not be granted and will result in CPU lockout.

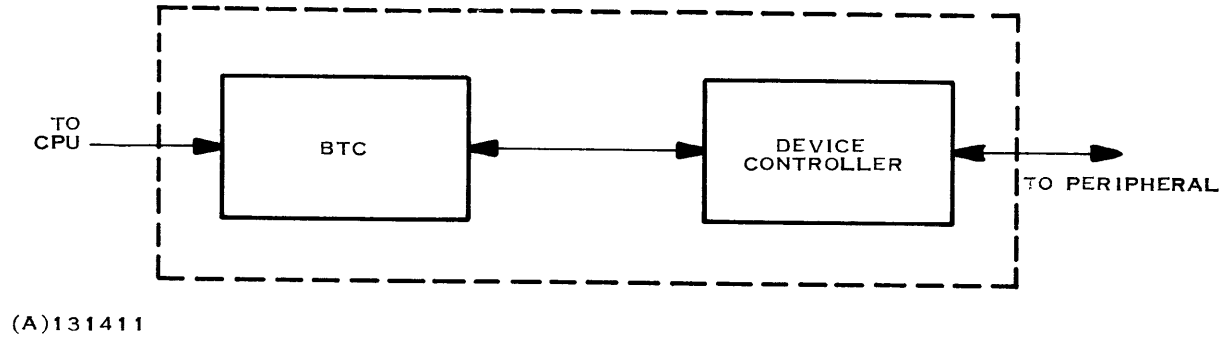


Figure 1-2. Typical Peripheral Controller

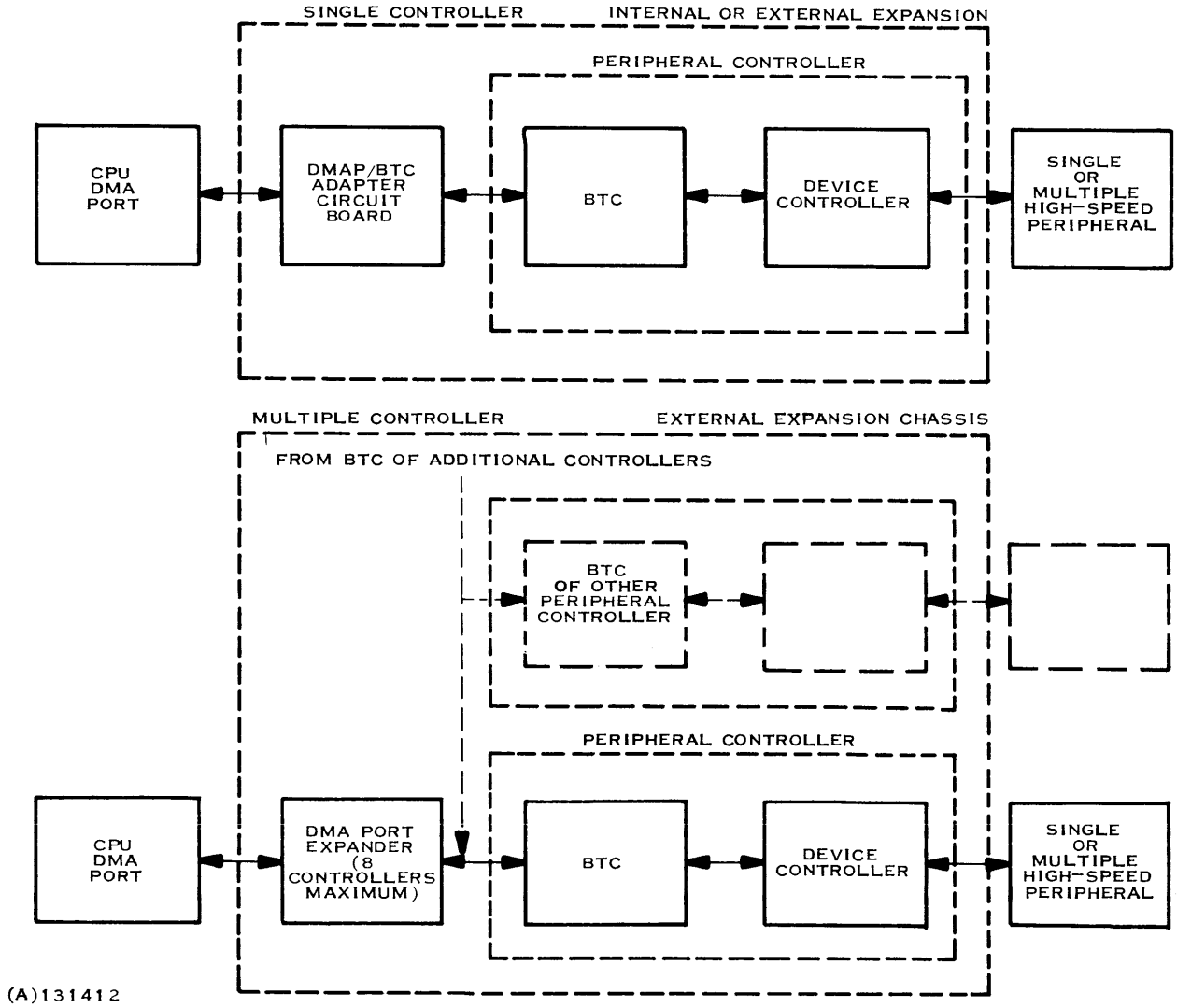


Figure 1-3. Block Transfer Controller Applications

Table 1-1. BTC Characteristics

Characteristic	Specification
Available Channels	Any one of eight DMA channel addresses.
Data Transfer Rate	500,000, 16-bit words per second maximum (see text)
Logic Type	Series 74N TTL integrated circuits.
Logic Levels	Logic low = 0.0 – 0.8 Volts Logic high = 2.4 – 5.0 Volts
Output Signal Drive Capabilities	All output signals can drive a maximum of four, series 74 or 74H TTL loads.
Input Signal Requirements	Input signals to the BTC shall be generated by open-collector devices. Loads (pull-up resistors) for these devices are on the BTC circuit boards.
Environmental:	
Temperature	Operating range = 0° to 70°C Storage range = –40° to 100°C
Humidity (No condensation)	Operating range = 5 to 85% Storage range = 5 to 95%
Pressure	Operating and storage range = 20 to 32 in. Hg.
Power Requirement	5.0 ±0.1 Volts dc at 2 Amperes.

SECTION II

INSTALLATION

2.1 GENERAL

The BTC cannot operate independently and is always part of a peripheral controller. Peripheral controllers can be implemented as single controllers, either internal or external to the CPU chassis. Multiple controllers are contained in an external expansion chassis. Figure 2-1 illustrates these standard DMA configurations. All circuit boards are installed in their associated chassis during system test. When system test is complete, all cables are disconnected and the circuit boards are left in place for shipment. For shipping, a piece of filament tape may be put across the top of all circuit boards in a chassis.

2.2 INSTALLATION PROCEDURE

Perform the following general procedure to install a DMA system. Since the BTC is installed at the factory, this installation procedure describes general DMA installation rather than specific BTC installation. Proceed as follows:

1. Unpack all system components.

2. Set up all peripheral equipment as outlined in vendor manuals.

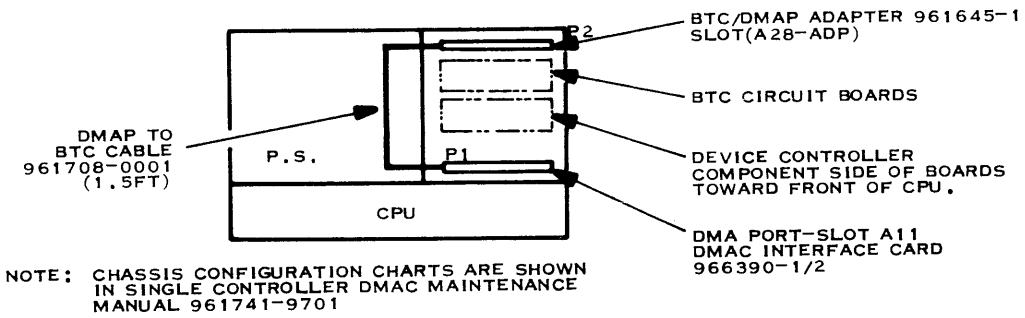
3. Verify that the circuit boards of all peripheral controllers are installed in the locations specified in the DMA chassis configuration chart. Configuration charts showing standard chassis motherboard layouts are located in the applicable DMAC Maintenance Manual. Refer to the *DMA Port Expander Maintenance Manual,* part number 216759-9701 for standard, multiple port, chassis configuration charts. Refer to the *Single Controller DMAC Maintenance Manual*, part number 961741-9701, for standard chassis configuration charts of single port DMAC controllers. Configuration charts showing layouts of nonstandard (custom) chassis are found in an accessory kit drawing. An accessory kit drawing describes the layout of the chassis, motherboard, installation of the motherboard in the chassis and placement of the circuit boards and interconnecting cables. An accessory kit drawing accompanies all non-standard hardware.

4. Verify that the channel address on each BTC No. 1 circuit board (PWB assembly part number 966466-0001, or wire wrap board part number 240656-0001) in each peripheral controller is the address required by the driving software. Standard channel assignments are shown in table 2-1. Refer to paragraph 2.4 for address information.

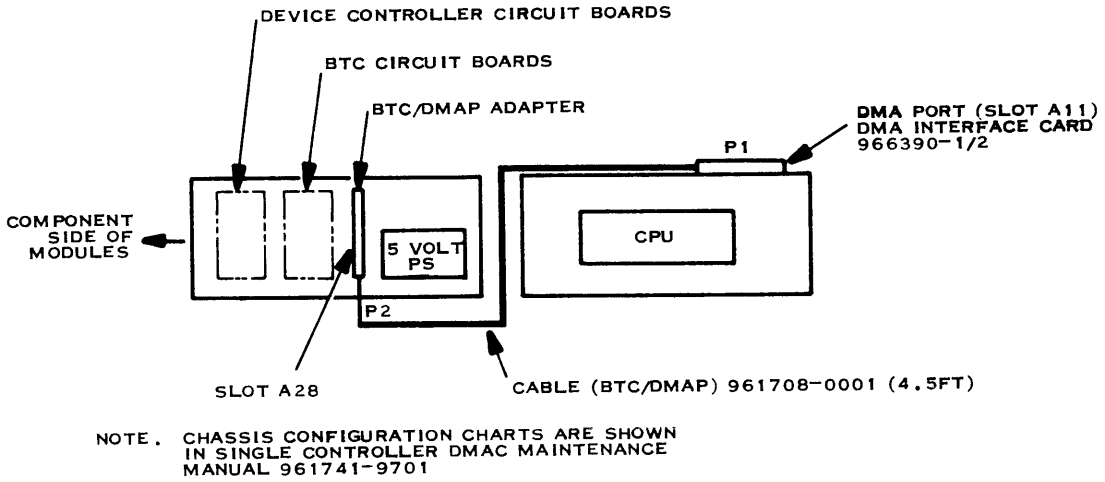
5. Interconnect all peripheral devices to their associated controllers. Refer to *Model 960/980 Computers Direct Memory Access Channel Controller Manual,* part number 966312-9702, for the interconnecting diagrams of standard peripheral devices.

6. Interconnect the DMAC interface circuit board and either the DMAP/BTC adapter circuit board or the expander interface circuit boards as shown in figure 2-1.

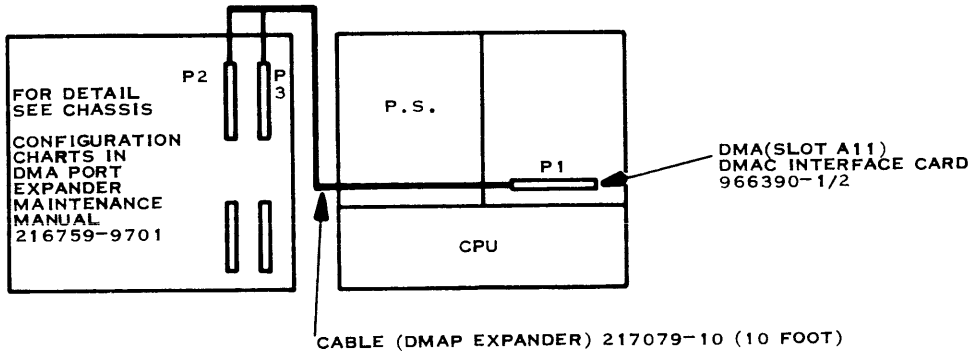
7. Verify that ac power is available and confirm that the voltage and frequency are correct. Power up the computer and the external expansion chassis, if applicable. The computer ac power is turned on by the power switch at the rear of the machine. The DMAC expansion chassis is turned on by a power switch at the rear of the chassis. A single DMAC expansion chassis is turned on when the power cable is plugged into an ac source. Turn on the peripherals as described in the vendor manuals.



SINGLE DMA CONTROLLER IN CPU MOUNTED EXPANSION CHASSIS



SINGLE DMA CONTROLLER IN EXTERNAL EXPANSION CHASSIS



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DMA CONTROLLER IN LARGE EXPANSION CHASSIS

Figure 2-1. Standard DMA Chassis Configurations

Table 2-1. Standard Device Addresses

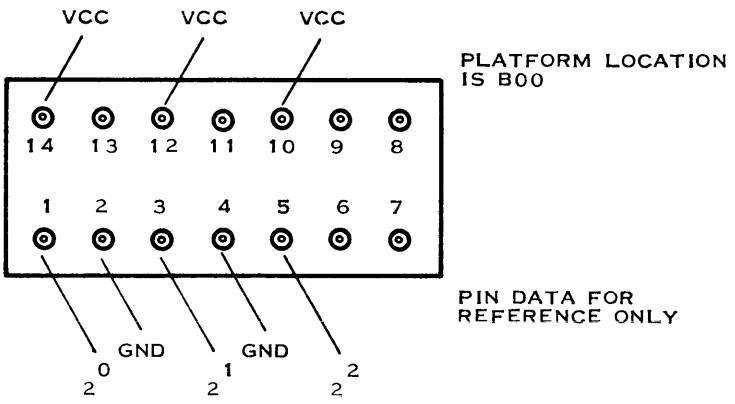
Device	Channel Number
Fixed-Head Disc	0
Moving-Head Disc	1
Magnetic Tape Transport	2

2.3 TESTING

Individual BTC testing is done by performing the Performance Demonstration Test (PDT) for the connected devices. A program description, paper tape object code, and operating instructions for each PDT is contained in a documentation kit included with the system. A documentation kit lists all documents to be shipped with a system and references other useful and relevant documents. These documents may include drawings, manuals, program media, program descriptions, flow charts and listings. Systems with card reader or cassette input devices also have complete card or cassette libraries of PDTs.

2.4 CHANNEL ADDRESS DATA

The channel address is defined on the wire wrap circuit boards by a wired, 14-pin platform. Refer to figure 2-2 for address data. Channel address for the multilayer printed wiring circuit boards is entered into the circuitry using either a rocker or a slide switch mounted on the circuit board. Refer to figure 2-3 for address data.



CHANNEL NO.	CONNECTIONS		
0	1-14	3-12	5-10
1	1-2	3-12	5-10
2	1-14	3-4	5-10
3	1-2	3-4	5-10
4	1-14	3-12	5-6
5	1-2	3-12	5-6
6	1-14	3-4	5-6
7	1-2	3-4	5-6

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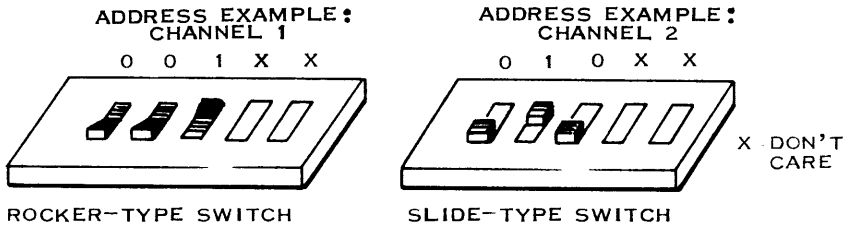
Figure 2-2. Wire Wrap Circuit Board Address Data



CHANNEL NUMBER	SWITCH SETTINGS				
	1	2	3	4	5
0	OFF	OFF	OFF	DON'T CARE	DON'T CARE
1	OFF	OFF	ON		
2	OFF	ON	OFF		
3	OFF	ON	ON		
4	ON	OFF	OFF		
5	ON	OFF	ON		
6	ON	ON	OFF		
7	ON	ON	ON		

NOTE: OFF = LOGIC 1; ON = LOGIC 0

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Figure . Multilayer Circuit Board Address Data

SECTION III

OPERATION AND PROGRAMMING

3.1 GENERAL

This section contains general information about the instructions and list words used for communication between the CPU and the BTC, and between the BTC and a device controller. Operation of the BTC is dependent upon instructions from the CPU and enabling signals from the device controller. Specific information about the 980 computer Automatic Transfer Instructions (ATI) or the 960 computer Activate Direct Access Channel (ADAC) and the list words is given in *960/980 Computers Direct Memory Access Channel Controller Manual,* part number 966312-9702.

3.2 CHANNEL ADDRESSING

The BTC may be assigned any channel address from channel 0 through channel 7. Circuitry within the BTC uses the assigned channel address to determine when to respond to the ATI or ADAC instruction from the computer. The assigned channel is entered into the BTC circuitry as outlined in Section II.

3.3 ATI AND ADAC FORMAT

Transfer of data and commands between the CPU and the BTC of a peripheral controller are initiated by execution of either an ATI or ADAC instruction from the computer. This instruction consists of two, 16-bit words as shown in figure 3-1.

3.3.1 FIRST INSTRUCTION WORD. The first 8 bits are dedicated to the CPU and are not used by the peripheral controller. Bits 8 through 12 are used by the device controller. This field usually contains command and unit selection information (for daisy-chained devices). However, no action will be taken unless bits 13 through 15 contain the correct channel address. For some device controllers, such as the magnetic tape controller, a reset or rewind command in this field may cause the second instruction word to be ignored. The second instruction word is always sent by the CPU and the specific device controller decides whether to accept or ignore it.

Bits 13 through 15 are the channel address for the peripheral device. When the bits agree with the switch-selected or wired address, the BTC generates a one-clock time strobe (ATI1) which indicates to the device controller that the information on data lines 8 through 12 is for this channel. If the instruction is received while the device controller is not busy, this instruction word will be stored in BTC register file 1 (RF1) and instruction word 2 will be stored in RF3. If the instruction is received while the device controller is busy, the two instruction words are not stored in the register file. The first instruction word is presented to the device controller during the ATI1 strobe. The next action is dependent upon the device controller. It may, for instance, check to see if a reset function is to be performed to abort the present operation.

3.3.2 SECOND INSTRUCTION WORD. The 16 bits of the second instruction word are the starting address location in CPU memory of a 4-word list used for either initialization or for channel operations. If the instruction is received when the device controller is not busy, the BTC stores the word in RF3. If the instruction is received when the device controller is busy, the word is not stored in the register file.

3.4 INITIALIZATION/CHAIN LIST WORD

For data transfers, more information is usually required by the device controller than can be supplied in the 2-word, ATI or ADAC instruction. Therefore, a 4-word list is used. Figure 3-2 illustrates a typical set of list words and the following paragraphs explain the content of each word. The list words may be used for purposes other than described in the following paragraphs.

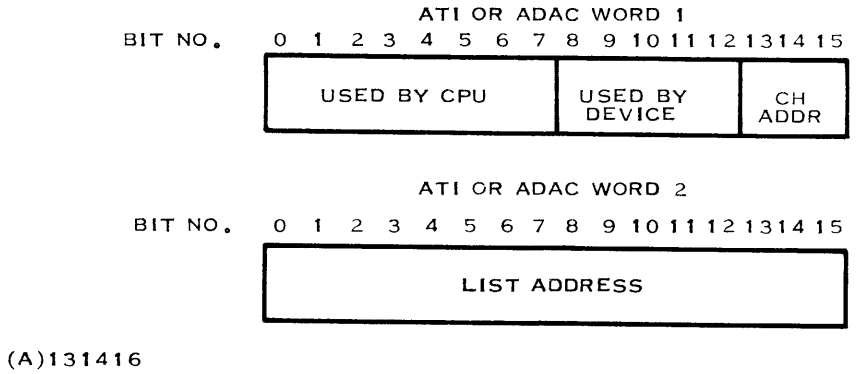

Figure 3-1. ATI or ADAC Instruction Format

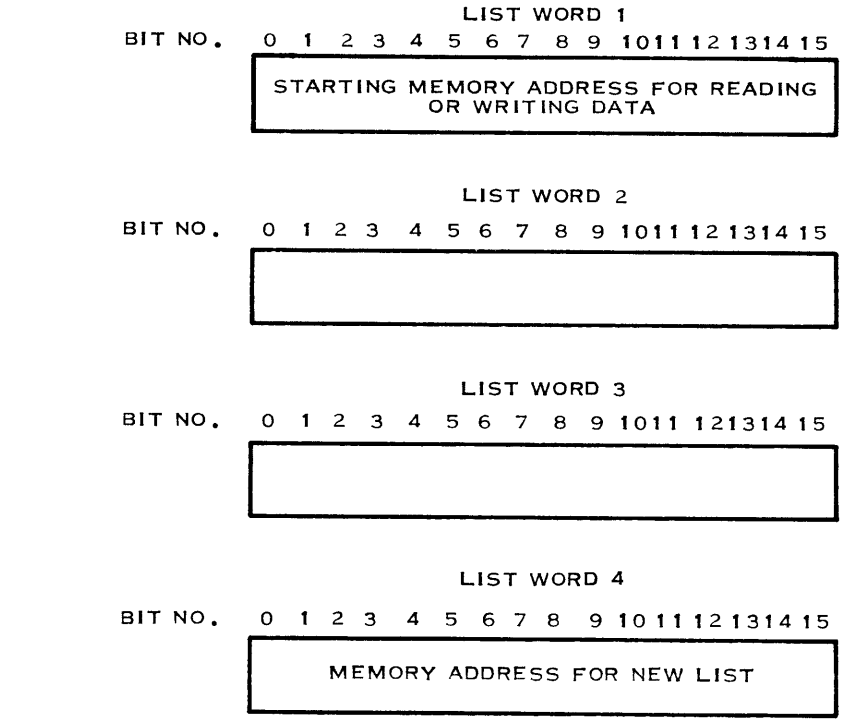

Figure 3-2. List Word Format

3.4.1 **LIST WORD 1.** List word 1 contains the starting address in CPU memory that data will either be read from or written into. This word is stored in RF2. After the last list word is fetched from memory this address information is transferred to the memory address register in the BTC. The list word is on the data lines to the device controller during the one clock time list 1 strobe (LIST1).

3.4.2 **LIST WORD 2.** List word 2 usually contains a count which is to be decremented by the device controller. The count usually specifies the number of words, sectors or bytes to be transferred by the device controller. This list word is on the data lines to the device controller during the one-clock time, list 2 strobe (LIST2).

3.4.3 **LIST WORD 3.** List word 3 usually contains command, interrupt, chain operation and address information for the device controller. This word is applied to the device controller after all the list words have been fetched and is on the data lines to the device controller during the one-clock time, list 3 strobe (LIST3).

3.4.4 **LIST WORD 4.** List word 4 contains the starting address in CPU memory of another set of list words to be used for chained operations. During the initial list acquisition, list word 4 is placed in register file 4 (RF4). If chaining is selected, list word 4 will be stored in RF3 during the first chain list acquisition. In subsequent chain list acquisitions, list word 4 will be stored alternately in RF3 and RF4.

3.5 STATUS/INTERRUPTS

Status information is transferred to the CPU from a peripheral controller through direct memory access of the reserved status locations. Two memory locations are reserved for each of the eight DMA channels. Status storage may consist of one or two memory accesses depending upon the device controller requirements. An interrupt may, or may not, accompany the status storage operation. When the device controller requests a status cycle, it must also select whether an interrupt is to occur. The capability of the device controller to enable or disable interrupts permits interrupts from one peripheral controller to be disabled while the other peripheral controllers continue to present interrupts to the CPU. When DMAC interrupts are disabled by the CPU, no interrupt requests are acknowledged. Interrupts within the device controller are usually controlled by a bit in one of the list words.

When interrupts are enabled within the device controller, DMAC interrupts are enabled within the CPU and a status storage is requested by the device controller, a DMAC interrupt occurs. The program being executed by the CPU is interrupted and the active program address register is set to 92_{16} on a Model 960 computer or location 4_{16} on a Model 980 computer. Locations 92_{16} and 93_{16} on the Model 960 computer and 4_{16} and 5_{16} on the Model 980 computer are referred to as the DMAC trap locations. These trap locations usually contain a Store Status Block (SSB) instruction which stores the status of the CPU the instant before the interrupt was recognized, and then transfers program control to the interrupt processing routine. When interrupts are enabled by the device controller, the status storage cycle requested by the device controller is not accomplished until the accompanying interrupt is recognized. A status storage sequence is explained in the following paragraph.

3.5.1 **STATUS STORAGE SEQUENCE.** The Status Enable pulse (STATEN–) from the device controller initiates the status storage sequence. If the Interrupt Enable signal (INTEN–) is high when STATEN– is presented, the BTC will request the next available memory cycle. If INTEN– is low when STATEN– is presented, the BTC issues an interrupt request to the CPU. The BTC waits for an interrupt recognition from the CPU before proceeding. An Interrupt Recognized (INTRECDEV, N–) signal is sent from the CPU when the DMAC interrupt bit in the CPU status register is set and an SSB instruction has been executed. Receipt of the interrupt recognition signal enables the BTC to proceed by requesting the next available memory cycle. If the interrupt has been disabled by the device controller, the BTC proceeds with status storage as soon as STATEN– is received. If interrupts have been disabled in the CPU, status storage is delayed until the device controller interrupt is recognized.

3.5.2 **RESERVED STATUS LOCATIONS.** The locations shown in table 3-1 are reserved for DMAC status storage in both Model 960 and 980 computers.

Location 96_{16} is reserved for the DMAC expander interrupt status word. This word indicates which of the eight expander peripheral controllers have interrupts pending. A logic 1 appears in the bit position corresponding to the channels that have registered interrupt requests (e.g., DMAC channel number 2 will set bit 2 of location 96_{16}). This word is applicable only to DMA expander interfaces

and not single controller configurations through the BTC/DMAC adapter card. Only bits 0 through 7 (corresponding to the eight expander chassis channels) are used, and bits 8 through 15 are written as zeros when expander status is stored. The channel address switches (or wire jumpers) on each BTC card number 1 establish the memory address used for status storage. One or two status words may be stored.

Table 3-1. Reserved Status Locations

DMAC Channel	Location (Hex)
Expander	96
0	98, 99
1	9A, 9B
2	9C, 9D
3	9E, 9F
4	A0, A1
5	A2, A3
6	A4, A5
7	A6, A7

3.6 STATUS WORD

The BTC stores either one or two status words depending on the device controller. The first status word is taken from the device controller data bus (RFOUT) and applied to the CPU. The second status word (if used) is taken from either the register file (RF3 or RF4) or the data counter circuit. The register file contains the list in progress starting address, and the data counter circuit contains the remaining data count. The number of status words and the origin of the second status word is directly controlled by the device controller. The store status cycle has memory access priority over data transfers within the BTC.

3.7 PROGRAMMING EXAMPLES

The following program examples are given to point out general techniques and considerations of DMAC programming. The examples include brief descriptions of the tasks being performed. Refer to the applicable *Assembly Language Programmers Reference Manual* for programming details.

3.7.1 MODEL 980 COMPUTER EXAMPLE. The following programming example (figure 3-3) writes a 500 character record on magnetic tape unit 1 from reserved memory named BUFFER. Following the write, a check is made to determine if the operation is complete. Chaining is not used but the magnetic tape unit will issue an interrupt when the write is complete. This sequence implies that DMAC interrupts are inhibited and that the progress of the specified operation is being followed by monitoring the status register. Typically, when operating with interrupts, the ATI would be followed by an idle (IDL) instruction to await completion of the operation.

TI 960/980 ASSEMBLY CODING FORM

LABEL (1–6)	OPER (8–11)	OPERAND (13–25)	COMMENTS (26–60)
	LDA	=0	
	STA	*STATUS	CLEAR STATUS
* >CA	SELECT	S LIST ACQUISION,TAPE	UNIT 1 AND BTC CHANNEL 2
	ATI	>CA	ISSUE ATI
	DATA	LIST	ATI LIST POINTER
	LDA	*STATUS	OBTAIN STATUS
	SNZ	A	TEST FOR CHANGE
	BRU	$-2	REPEAT IF NO CHANGE
	CPL	LEGAL	TEST FOR WRITE COMPLETE
	SEQ		CONTINUE IF COMPLETE
	BRU	ERROR	BRANCH TO ERROR ROUTINUE
	BRU	CONT	CONTINUE
STATUS	DATA	>9C	RESERVED LOCATION POINTER
LIST	DATA	BUFFER,500,>9000,0	
* LIST	WORD	1 = STARTING ADDRESS OF DATA	
* LIST	WORD	2 = CHARACTER COUNT	
* LIST	WORD	3 = WRITE COMMAND WITH INTERRUPTS ENABLED	
* LIST	WORD	4 = CHAIN LIST ADDRESS	
LEGAL	EQU	>8000	
BUFFER	BSS	250	

PROGRAM | PROGRAMMED BY | CHARGE | PAGE | OF

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Figure 3-3. Model 980 Computer Programming Example

3.7.2 **MODEL 960 COMPUTER EXAMPLE.** The programming example in figure 3-4 reads a 500 character record from magnetic tape unit 1 and stores the data in memory starting at location BUFFER. Following the read, a check is made to determine whether the operation is completed without error. Chaining is not selected. The program assumes that DMAC interrupts are enabled by the CPU and that the data and procedure registers were previously initialized.

TI 960/980 ASSEMBLY CODING FORM

LABEL (1–6)	OPER (8–11)	OPERAND (13–25)	COMMENTS (26–60)
	LA	0,X'7882'	STORE SSB INSTRUCTION 1ST WORD
	ST	0,X'92'	FOR INTERRUPT TRAP
	LA	0,INTTRP	STORE SSB OPERAND ADDRESS
	ST	0,*'93'	
	LA	0,0	
	ST	0,*STATUS	CLEAR STATUS REGISTER-CHANNEL 2
	ADAC	2,LIST,AQUIR+TP1	INITIATE INPUT - TRANSPORT 1
	B	$	WAIT FOR INTERRUPT
	CONTINUE		
	'		
	'		
ERROR	SUBROUTINE		
	'		
	'		
	'		
BUFFER	BSS	250	
LIST	DATA	BUFFER,500,X'8000',0	
*	LIST	WORD 1 = STARTING ADDRESS OF DATA	
*	LIST	WORD 2 = CHARACTER COUNT	
*	LIST	WORD 3 = READ COMMAND WITH INTERRUPTS ENABLED	
*	LIST	WORD 4 = CHAIN LIST ADDRESS	
INTTRP	DATA	0	SAVE PC
	DATA	0	SAVE STATUS(CPU)
	DATA	TRAP	ADDRESS OF INTERRUPT HANDLER
AQUIR	EQU	X'18'	LIST ACQUISITION
TP1	EQU	1	TRANSPORT 1

PROGRAM | PROGRAMMED BY | CHARGE | PAGE | OF

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Figure 3-4. Model 960 Computer Programming Example (Sheet 1 of 2)

TI 960/980 ASSEMBLY CODING FORM

LABEL (1–6)	OPER (8–11)	OPERAND (13–25)	COMMENTS (26–60)
STATUS	DATA	X'9C'	
TRAP	AMI	INTTRP,2	ADVANCE PC OVER WAIT INST.
	LA	0,X'8000'	EXPECTED STATUS
	CR	0,*STATUS	ACTUAL STATUS
	BC	11,OPCOM	EQUAL? CLEAR INTERRUPT MASK
*			AND CONTINUE IF TRUE
	B	ERROR	ERROR SUBROUTINE CALL
OPCOM	LDS	INTTRP	GO CONTINUE DATA PROCESSING

PROGRAM | PROGRAMMED BY | CHARGE | PAGE | OF

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Figure 3-4. Model 960 Computer Programming Example (Sheet 2 of 2)

SECTION IV

THEORY OF OPERATION

4.1 GENERAL

This section contains detailed interface data and theory of operation information.

4.2 INTERFACE SIGNALS

The BTC interfaces with the DMA port of either a 960 or 980 computer and with one of four peripheral devices. Interface signals at these interfaces are shown in figure 4-1 and summarized in the following tables. Additional data about these interface signals between the BTC and the device controller is given in the paragraphs following the tables to assist in interfacing a BTC with a device controller other than the four standard controllers. Additional data about the signals between the CPU and BTC is given in *Model 960/980 Computers Direct Memory Access Channel Manual*, part number 966312-9701.

4.3 INTERFACE SIGNAL TABLES

Tables 4-1 through 4-4 provide a brief description of the interface signals shown in figure 4-1. The circuit board that receives an input or is the source of an output signal is given in the Input/Source column.

4.4 BTC TO DEVICE CONTROLLER SIGNALS

The following signals are generated by the BTC for use by a device controller:

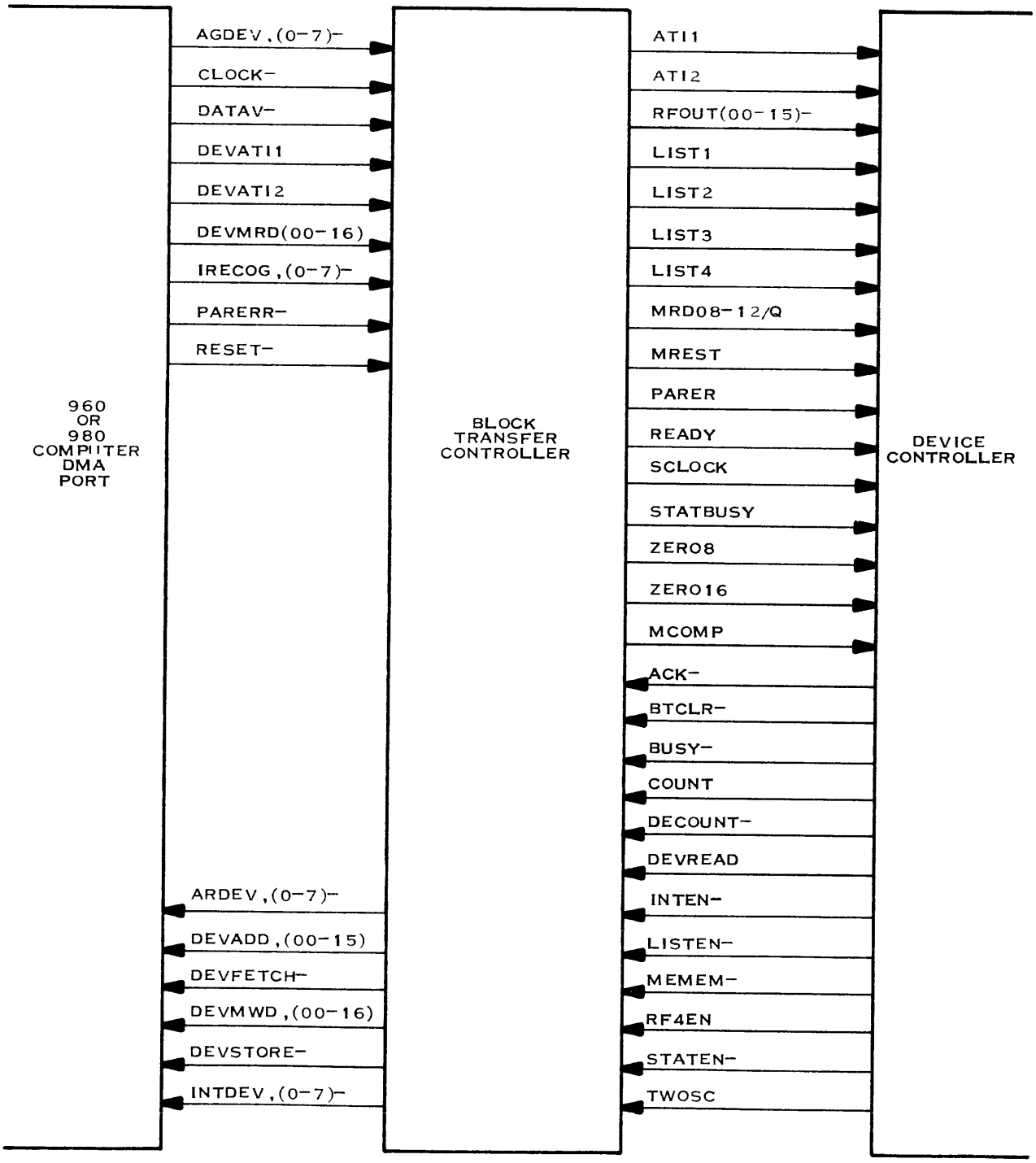
ATI1. This signal is a one clock time signal generated from the ATI or ADAC word 1 strobe (DEVATI1–). This pulse is generated when an ATI or ADAC command is addressing the selected device address. MRD(08-12)/Q contains the device field of instruction word 1 during this pulse. Word 1 data will be stored in RF2.

ATI2. This signal is a one clock time signal generated from the ATI or ADAC instruction word 2 strobe (DEVATI2–). This signal is generated only if the ATI or ADAC command is received while the device controller is not busy (BUSY–). The RFOUT lines contain word 2 data during this pulse. Word 2 data is stored in RF3.

MRD(08-12)/Q. These signals are the memory read data register output bits 8 through 12. The MRD register is loaded with every ATI, ADAC or data available pulse generated by the CPU; therefore, these bits should be decoded for the instruction word 1 device field only during the ATI1 pulse. The BTC MRD register outputs, MRD(08-12)/Q, must be sampled by the device controller at either the trailing edge of the ATI1 pulse or at system clock "true" in order to assure stability of the MRD data.

LIST,N(N=1,2,3 or 4). One clock time signals that indicate list word N is on the RFOUT lines.

RFOUT,N-(N=00-15). These signals represent a bi-directional data bus. The device controller receives and sends all data by these lines. The device controller can place data or a status word on this bus only when READY is true. RF1 will be on the bus unless some other register file has been selected or unless READY is true. The signals on these lines are inverted logic. Signal sources must be open collector.



(A)131420

Figure 4-1. BTC Interface Signals

Table 4-1. CPU to BTC Signals

Signal Name	Input/Source Board No.	Pins	Description
AGDEV, N–	3	5–12	Indicates that CPU has granted access to device N. (N = 0 through 7)
CLOCK–	1	8	CPU clock signals: 960 = 3 MHz 960A, 960B, 980, 980A, 980B = 4 MHz
DATAV–	1	9	Indicates solid data on DEVMRD (00-15) lines
DEVATI1	1	15	Indicates that data on DEVMRD (00-15) lines is a valid first ATI or ADAC word
DEVATI2	1	16	Indicates that data on DEVMRD (00-15) lines is a valid second ATI or ADAC word
DEVMRD (00-16)	1	17–33	Data lines to BTC
INCOG,N–	3	41–48	Indicates that CPU has recognized the interrupt from device N. (N = 0 through 7)
PARERR–	1	47	Indicates a parity error in the data from the CPU.
RESET–	1	48	Signal to reset the BTC.

Table 4-2. BTC to CPU Signals

Signal Name	Input/Source Board No.	Pins	Description
ARDEV, N–	3	14–21	Indicates that device N is requesting access to CPU memory. (N = 0 through 7)
DEVADD (00-15)	3	7–22	Address lines to the CPU.
DEVFETCH–	2	25	Command to initiate a fetch cycle.
DEVMWD (00-16)	2	26–42	Data lines to the CPU. Bit 16 is parity bit.
DEVSTORE–	2	44	Command to initiate a store cycle.
INTDEV, N–	3	32–39	Indicates that device N is requesting an interrupt of the program being executed. (N = 0 through 7).

Table 4-3. BTC to Device Controller Signals

Signal Name	Input/Source Board No.	Pins	Description
ATI1	1	4	Indicates that device controller is being addressed.
ATI2	1	5	Indicates that ATI or ADAC word 2 is stored in BTC.
RFOUT (00-15)	1	50–65	Bi-directional data bus.
LIST, N	3	52–55	Indicates that list word N is on the RFOUT lines. (N = 1, 2, 3 or 4)
MRD08-12/Q	1	41–45	Data lines to apply ATI or ADAC word 1 data to the device controller.
MREST	1	76	Reset signal.
PARER	1	46	Indicates a parity error in the data or the RF OUT lines.
READY	3	60	Indicates origin of next data word.
SCLOCK	1	69	CPU clock to device controller (Ref. CLOCK–, table 4-1)
STATBUSY	3	70	Indicates that BTC has CPU memory access.
ZERO8	2	74	Indicates that low order 8 bits of data counter equal zero.
ZERO16	2	73	Indicates that all 16 bits of data counter equal zero.

Table 4-4. Device Controller to BTC Signals

Signal Name	Input/Source Board No.	Pins	Description
ACK–	3	3	Indicates that data is ready for the BTC or accepted from the BTC.
BTCLR	1	6	Signal to clear all BTC controllers and flip flops.
BUSY–	1	7	Indicates that device controller is busy.
COUNT	2	5	Determines data for second status word.
DECOUNT–	3	26	Decrements data counter in BTC.

Table 4-4. Device Controller to BTC Signals (Continued)

Signal Name	Input/Source Board No.	Pins	Description
DEVREAD	3	30	Indicates whether device controller is reading or writing.
INTEN–	3	40	Indicates that interrupt is enabled.
LISTEN–	3	51	Starts list subcontroller in BTC.
MEMEN–	3	58	Initializes data control flip flop and starts data subcontrollers in BTC.
RF4EN	3	65	Indicates the register file containing list starting address.
STATEN–	3	71	Initiates status subcontroller in BTC.
TWOSC	3	73	Indicates number of status cycles for the status subcontroller.

READY. This signal indicates that either the device controller shall place the next data word or the first status word on the RFOUT lines, or that the BTC is ready to put the next write data word on the RFOUT lines. If STATBUSY and READY are true, the device controller places the first status word on the RFOUT lines. READY will be true for over four clock times.

If READY is true, STATBUSY false, and DEVREAD from the device controller true, the device controller places the next data word on the RFOUT lines. READY will be true for one clock time.

If READY is true, STATBUSY false, and DEVREAD false, the next data is ready to be placed on the RFOUT. The data word is placed on the RFOUT lines when ACK– from the device controller is true. READY will be true as long as there are data words in the register file. The device controller can place data on the RFOUT lines only when READY is true.

PARER. This signal indicates that the data transfer between the BTC and the CPU did not have correct parity. The action to be taken about this signal is left to the device controller. PARER will remain true until the next status cycle or BTCLR.

STATBUSY. This signal indicates that the status subcontroller in the BTC has access granted from the CPU for storing the status word or words into memory and has interrupt recognized if interrupts are enabled. This signal will remain true until the status word or words have been stored.

MCOMP. This one clock time signal indicates that a memory cycle has been completed by the BTC.

ZERO8,ZERO16. These signals indicate that the low order 8 bits of the data counter (ZERO8) or all 16 bits of the data counter (ZERO16) are equal to zero. The signals come true during the decrement pulse (DECOUNT–) and remain true until the next list initiation (LISTEN–).

MREST. This signal indicates that the CPU master reset switch or the power clear has been actuated. This signal may have a maximum of 10 standard TTL H or N series loads.

SCLOCK. This signal is the CPU system clock. The early 960 computer has a 3 MHz clock rate. 960/980 A and B models have a 4 MHz clock rate. The BTC uses the clock signals generated by the device controller without buffering. Therefore, the device controller must use clocks with the same delays as those used by the BTC. This signal is capable of supporting a maximum of 10 standard TTL H or N series loads.

4.5 DEVICE CONTROLLER TO BTC SIGNALS

The following signals are generated by the device controller for BTC control and data inputs. All signal sources are open collector and synchronized with SCLOCK.

LISTEN–. This one clock time signal starts the list subcontroller in the BTC. The list subcontroller will fetch four list words. There are some restrictions on the use of this signal while storing status. Refer to the STATEN– signal description.

RF4EN. This signal indicates which register file contains the starting list address. When true (high), the address is in RF4. When false (low), the address is in RF3. This signal must be set with or before LISTEN– and not be changed until the next list enable pulse. The ATI or ADAC word 2 is always put into RF3. Therefore, before the LISTEN– signal is given (after the ATI or ADAC command), RF4EN must be reset or in the false state. This signal is also used by the status subcontroller to designate the register file containing the current list starting address.

MEMEN–. This one clock time signal starts the data subcontrollers. Once activated, the subcontrollers continue fetching or storing to, or from, sequential memory locations until the next LISTEN– signal is received. MEMEN– is used to initialize the data control flip flop. Therefore, it should be sent only once for each list.

DEVREAD. This signal indicates whether the device controller is reading or writing data. When true, the device is reading data. When false, the device is writing data. DEVREAD must be set with or before MEMEN– and stay set until the next LIST3 pulse.

ACK–. This signal indicates that data is ready to be transferred to the register file in device read mode (DEVREAD true) or that data has been taken from the data bus (RFOUT lines) in the device write mode (DEVREAD false). In the device read mode, this signal remains true until the READY signal is received. In the device write mode, this signal is a one clock time signal and can be set only if READY is true.

DECOUNT–. This one clock time signal decrements the data counter in the BTC by one. The signal shall not come true while STATBUSY is true if the data counter is to be stored as the second status word.

STATEN–. This one clock time signal starts the status subcontroller. One or two status words are stored, depending on the logic level of TWOSC. The following restrictions must be observed when generating STATEN– and LISTEN–.

1. Do not initiate STATEN– and LISTEN– at the same time.
2. If LISTEN– has been issued, do not issue STATEN– until all list words have been fetched (LIST4).

INTEN–. This signal indicates that the interrupt is enabled and is usually controlled by a list word bit assignment. INTEN– must be true before and during STATEN– if an interrupt is to accompany status storage.

TWOSC. This signal indicates two status cycles. TWOSC, when true, indicates that two status words are to be stored. TWOSC, when false, indicates one status word is to be stored. This signal must stay set as long as STATBUSY is true.

COUNT. This signal, when true, indicates that the data counter data will be stored as the second status word. When false, this signal indicates that the starting list address will be stored as the second status word. COUNT false and RF4EN true indicate that RF4 data will be stored as the second status word. COUNT false and RF4EN false indicate that RF3 data will be stored as the second status word. COUNT must stay set as long as STATBUSY is true.

BUSY–. This signal indicates that the device subcontroller is busy. It is used to inhibit storing ATI1 and ATI2 instructions in the register file and also inhibits generation of the ATI2 strobe.

BTCLR–. This signal resets all active subcontrollers and flip-flops in the BTC. It is ORed with MREST in the BTC; therefore, it has the same effect as pushing the reset pushbutton. This signal may cause data parity errors if sent while the BTC is addressing the CPU memory.

4.6 THEORY OF OPERATION

Figure 4-2 is a detailed block diagram of the BTC. Refer to this diagram and the referenced figures within the subcontroller descriptions to aid in understanding the operation of the BTC.

4.7 INITIALIZATION SUBCONTROLLER

The initialization subcontroller monitors the ATI or the ADAC instruction from the CPU. When executing the ATI or ADAC instruction, the CPU sends out two strobe signals (DEVATI1 and DEDATI2), one for each word. With each strobe the DEVMRD bus data is clocked into the MRD register. Each strobe is also latched in the control section. When the first strobe is latched, the next system clock (CLOCK–) advances the subcontrollers to state 1 (IN1/Q). ATI timing is shown in figure 4-3. Figure 4-4 is a flowchart of the initialization subcontroller.

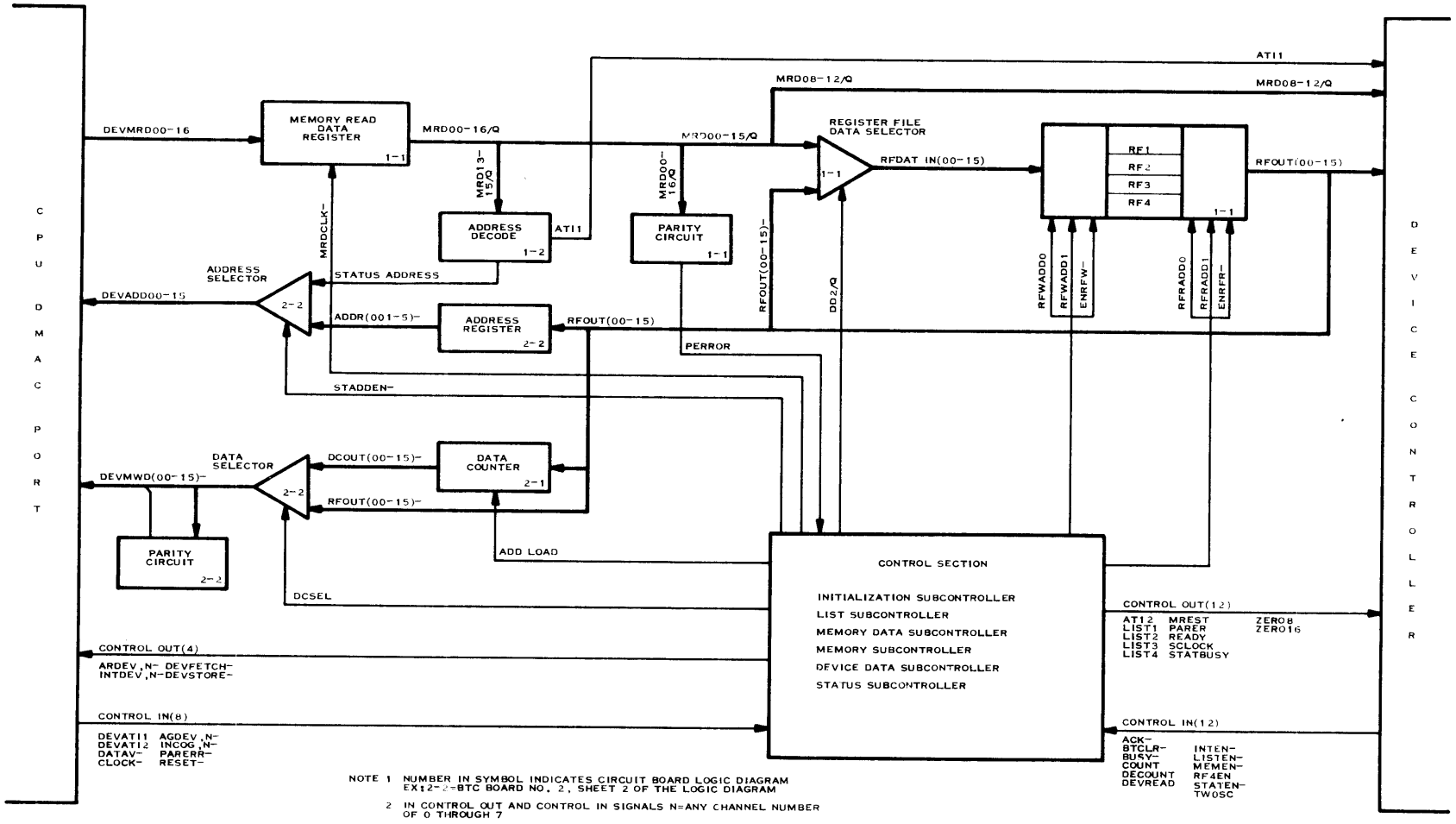


Figure 4-2. BTC Block Diagram

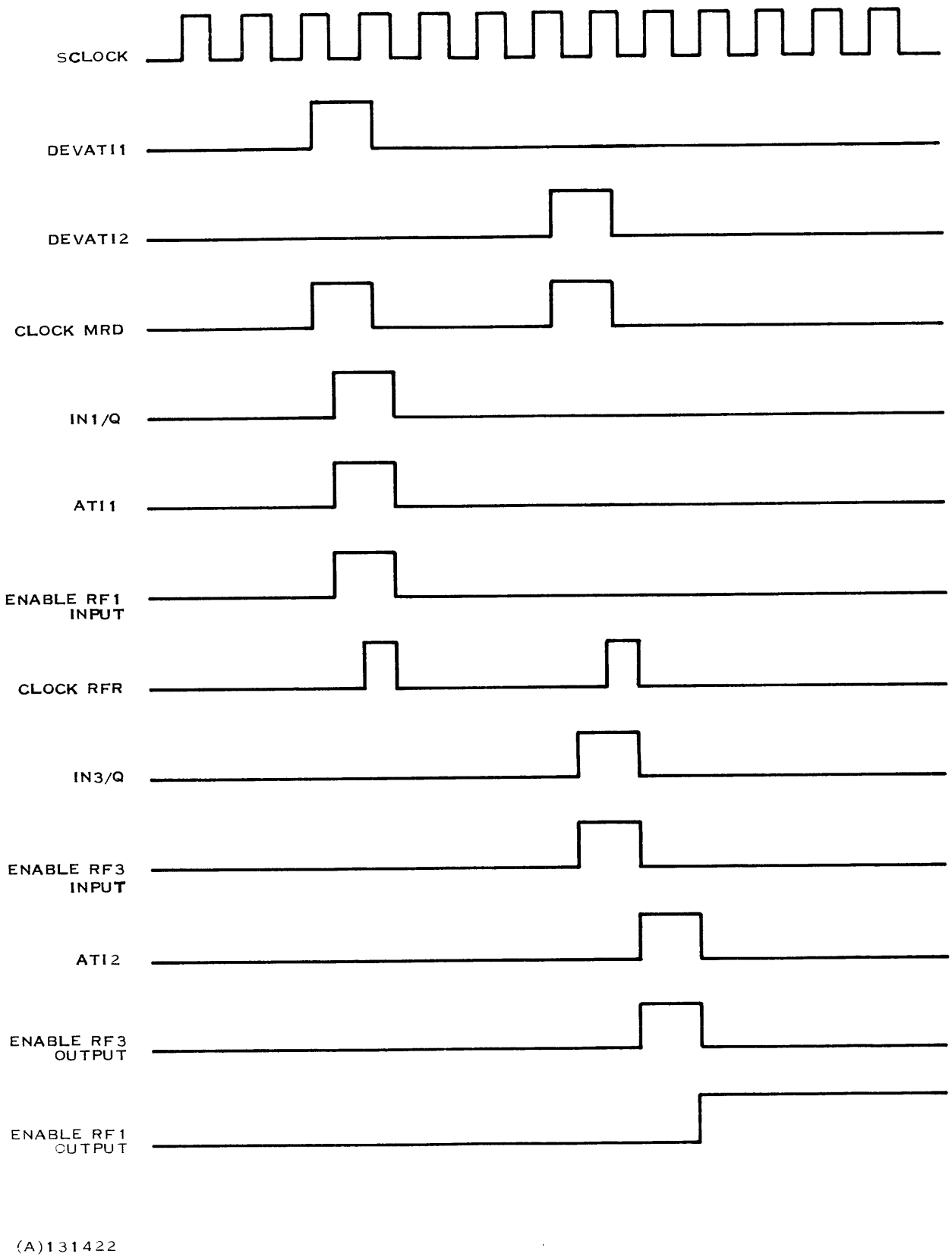


Figure 4-3. ATI Timing Diagram

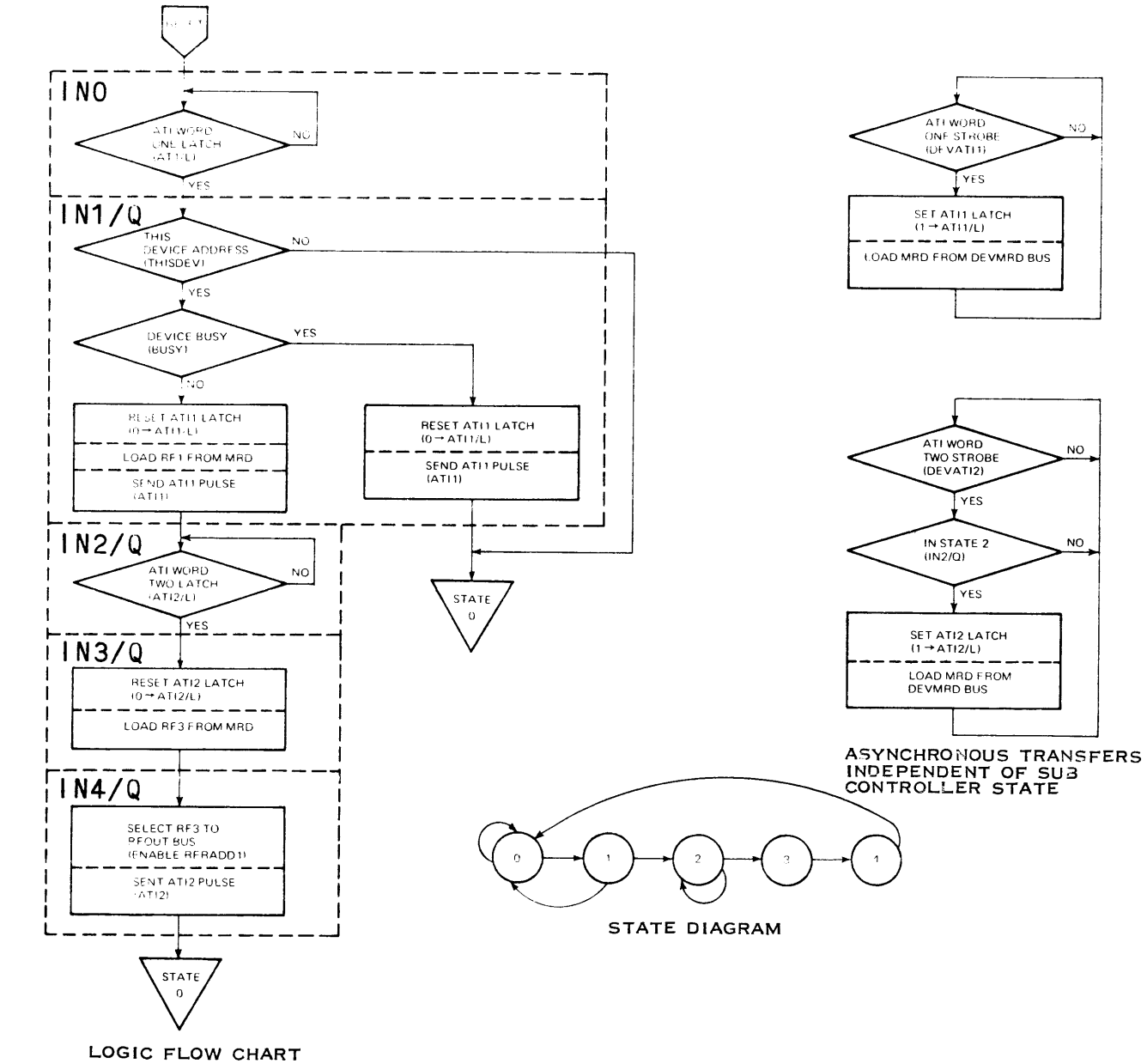


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Figure 4-4. Initialization Subcontroller Flowchart

In state 1, MRD bits 13 through 15 are compared with the address assigned to the controller. If a comparison is found, an ATI1 signal is sent to the device controller. If a comparison is found and the BUSY– signal is high, the subcontroller returns to state 0. Any action to be taken is up to the device controller. If a comparison is found and the BUSY– signal is low, MRD is clocked into RF1 and the subcontroller advances to state 2 (IN2/Q).

The subcontroller waits in state 2 until DEVATI2 strobe is latched and then advances to state 3 (IN3/Q). In state 3, MRD register data is transferred to RF3 and the subcontroller advances to state 4 (IN4/Q). In state 4, RF3 is selected to the RFOUT data bus, an ATI2 signal is sent to the device controller to transfer the data to the controller, and the subcontroller returns to state 0.

4.8 LIST SUBCONTROLLER

The list subcontroller is activated and advanced to state 1 by the list enable (LISTEN–) signal from the device controller. List acquisition timing is shown in figure 4-5. Figure 4-6 is the flowchart for the list subcontroller.

In state 1 (LC1/Q), a check for the three following conditions is made:

1. A memory cycle is not in progress (MCIP–), and one is not about to start. The signal MCIP– indicates that memory cycle request AR/Q is not set and is not imminent due to a status subcontroller state (STATBUSY or SC3/Q).

2. If DEVREAD is false, the memory data subcontroller is not about to start a memory cycle request due to MD2/Q or MD2/D.

3. If DEVREAD is true, all data transferred to the BTC from the previous list acquisition has been stored in the CPU memory. This is indicated by the buffer empty (BUFRMTY–) signal.

When these conditions are met, the subcontroller advances to state 2 on the next system clock. As the subcontroller advances to state 2, AR/Q is set, the memory data and device data subcontrollers are set to their state 0, and the register file flip-flops RF1/Q and RF2/Q are reset. The signal AR/Q causes the memory access request AR,N- signal to be sent to the CPU memory controller.

In state 2 (LC2/Q), the list starting address is loaded into the address register and the subcontroller is advanced to state 3. If register file 4 enable (RF4EN) is high, the list starting address is loaded in RF4. If RF4EN is low, it is loaded in RF3. Also, in state 2 the list counter is set to logic 1 (LCNT1).

The list counter is a 4-bit shift register that is loaded with logic 1 in the low order bit position in state 2 and shifted each time the subcontroller is in state 4.

The subcontroller waits in state 3 (LC3/Q) until the data available latch (DATAVL) is set by the DATAV– signal from the CPU memory controller. When memory is available, the CPU memory controller sends access granted (AGDEV,N–) in response to the ARDEV,N– sent to it when the subcontroller was advancing to state 2. The symbol, N, denotes one of the BTC channel addresses, 0 through 7. Access granted initiates the memory subcontroller which starts fetching the four list words. The first DATAVL indicates that list word 1 is in the MRD register.

In state 3, list word 1 is transferred from the MRD register to RF2. The next system clock steps the subcontroller to state 4.

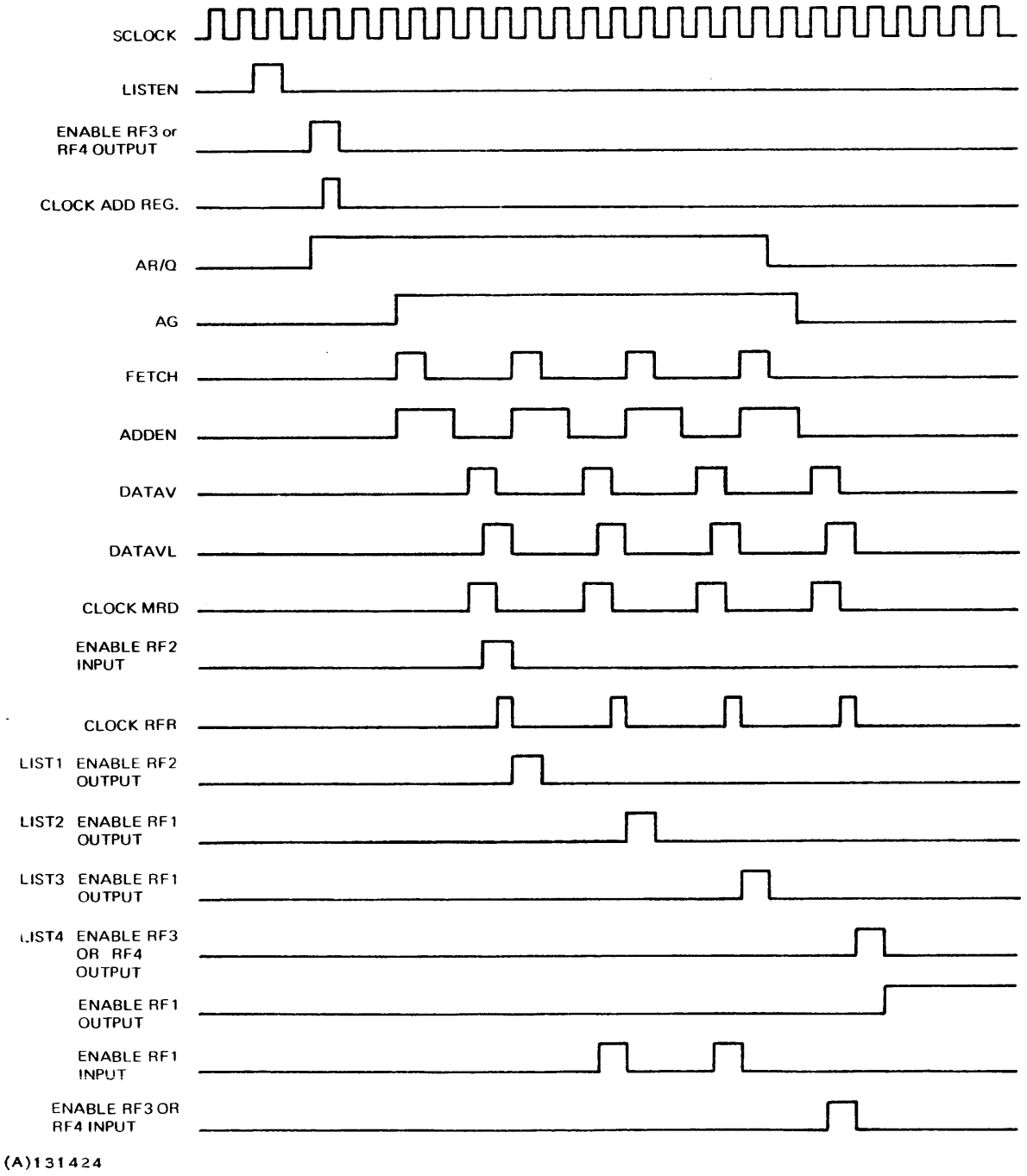

Figure 4-5. List Acquisition Timing Diagram

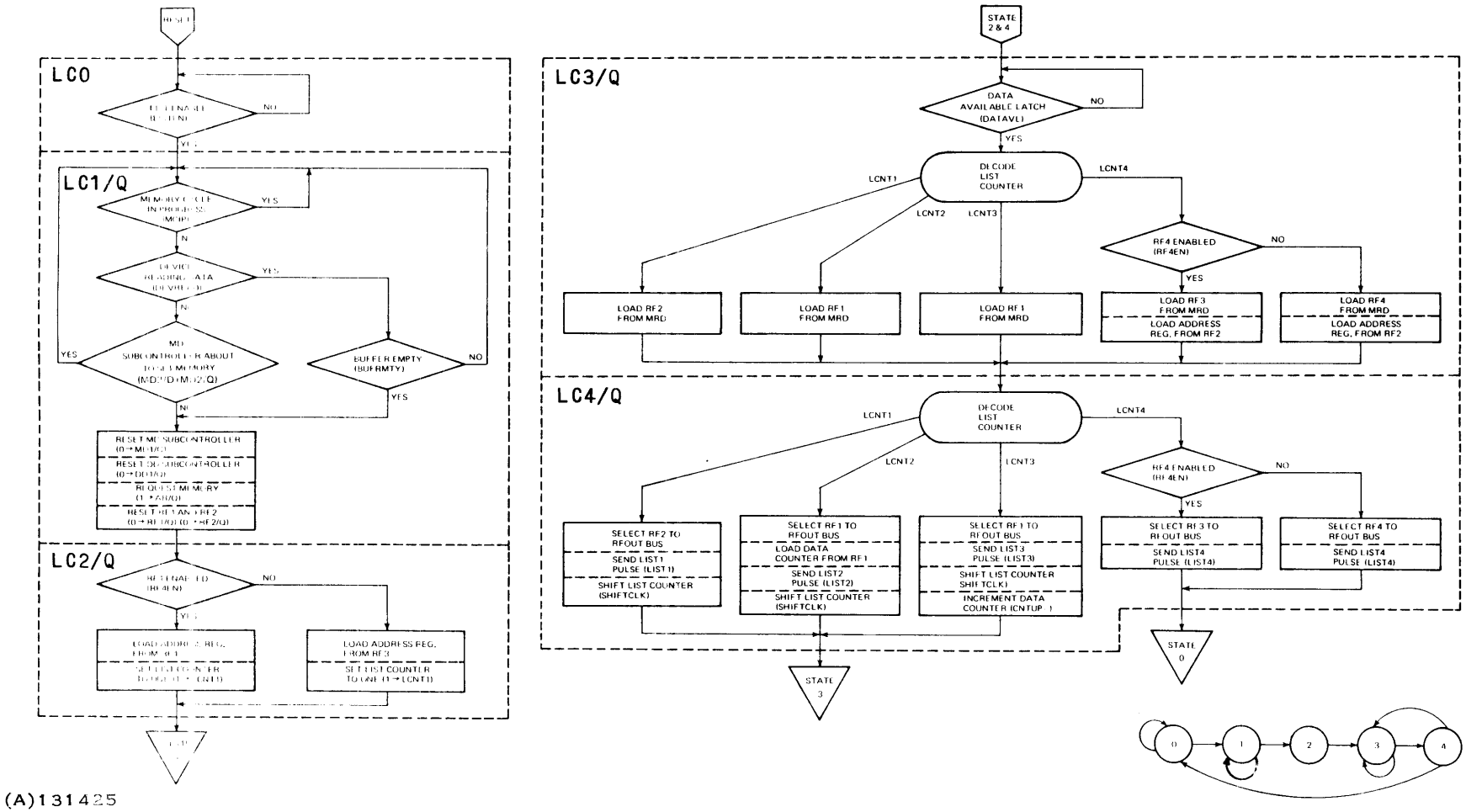

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Figure 4-6. List Subcontroller Flowcharts

In state 4 (LC4/Q), RF2 is selected to the RFOUT lines and the LIST1 signal is sent to the device controller. On the next system clock, the list counter is shifted one time and the subcontroller returns to state 3 to wait for the next DATAVL. The subcontroller continues alternating between state 3 and state 4 transferring the list words to the register file in state 3 and sending the LIST signals to the device controller in state 4.

The second list word is the data count. The data count is transferred to the data counter in state 4 when LCNT2 is high. To make it easier to decode data counter zero (ZERO8 or ZERO16), the data counter is initialized with a two's complement number by loading a one's complement number and then incrementing once. Data counter incrementing is accomplished in state 4 when LCNT3 is high. With the data counter loaded with a two's complement number and incremented with each decrement counter (DECOUNT–) pulse from the device controller, the carry out of the counter indicates data counter zero.

When in state 3 with LCNT4 high, the data starting address (first list word), which was transferred to RF2, is now transferred to the address register (ADDR). The fourth list word, which is the chain address, is transferred from the MRD register to either RF3 or RF4 depending on the logic level of RF4EN.

When the subcontroller is in state 4 and LCNT4 is high, the next clock pulse returns the subcontroller to state 0.

In summary, a list acquisition places list word 1 in the BTC memory address register, list word 2 in the data counter register (in two's complement form), and list word 4 into register file location 3 or 4. List word 3 is not used by the BTC controller. All list words are presented to the device interface. When a list word is on the device interface bi-directional bus, a signal (LIST N, where N=1 to 4) is sent to indicate that list word N is available. During initialization list acquisition, register file four should receive the chain address, list word four. Thereafter, the chain list acquisitions should alternately place the chain address in register files three and four. The destination is controlled by the device controller signal RF4EN which points to the starting data address. Note it is necessary for the BTC to maintain the present list address and next list address.

4.9 MEMORY SUBCONTROLLER

Memory requests in the BTC are initiated by the individual subcontrollers. The subcontroller requiring memory sets the memory access-request flip-flop which causes signal AR,N– to be sent to the CPU memory controller. When memory is available, the CPU sends access granted (AGDEV,N–) which activates the memory subcontroller. The memory subcontroller manages data flow between the CPU memory and the BTC. The memory subcontroller is divided into three sections as follows:

Memory read–States 1, 2 and 3

Memory write–States 4 and 5

Status–States 6, 7 and 3

The memory controller flowchart is presented in figure 4-7.

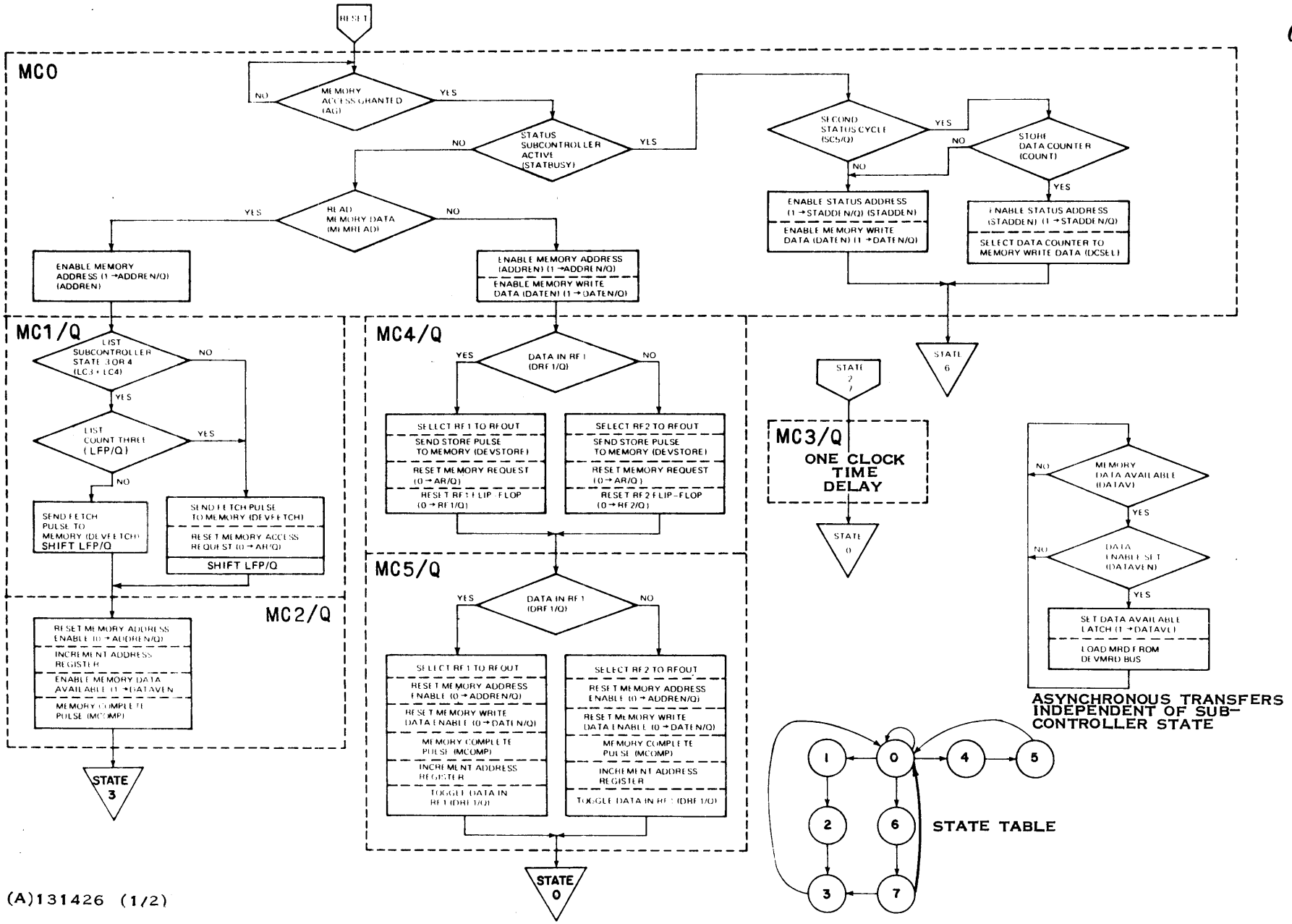

Figure 4-7. Memory Subcontroller Flowchart (Sheet 1 of 2)

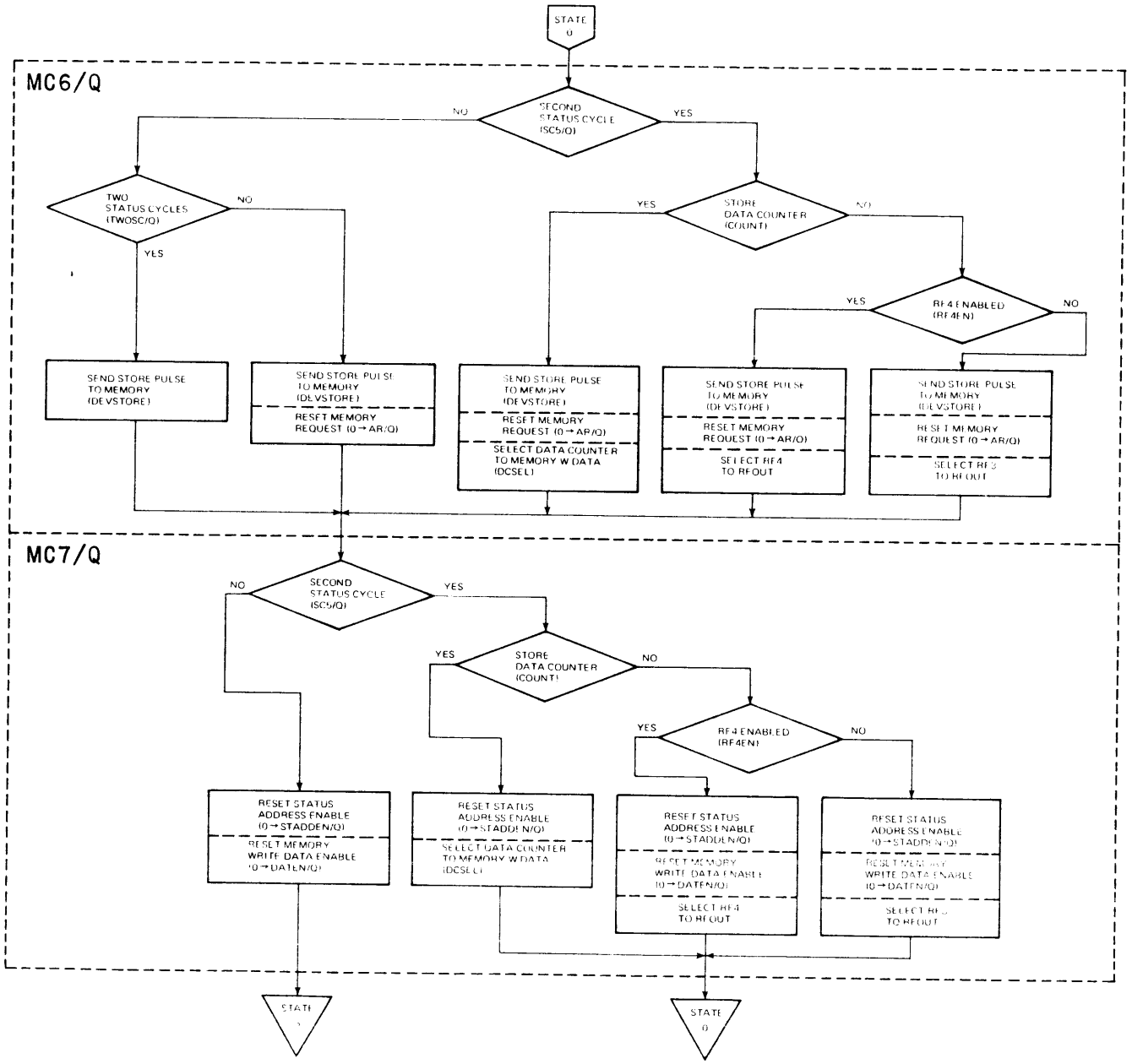

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Figure 4-7. Memory Subcontroller Flowchart (Sheet 2 of 2)

4.9.1 MEMORY READ–DATA AND LIST WORDS. Memory read (MEMREAD) is high if the list subcontroller is active, or if the device read (DEVREAD) signal is low and status busy (STATBUSY) is low. The device address lines (DEVADD) are enabled to the CPU memory controller as soon as AGDEV,N– is low. They stay enabled through the next two complete clock cycles. The DEVADD lines can be fed either address register data (ADDR) or status address data by use of the status address enable (STADDEN–) signal.

When AGDEV,N– is high, STATBUSY low, and MEMREAD high, the memory subcontroller advances to state 1 (MC1/Q). In state 1, the fetch pulse (DEVFETCH–) is sent to the CPU memory controller and the subcontroller advances to state 2 (MC2/Q). Also in state 1, AR,N– is reset if the memory cycle was for fetching data, or if it is the fourth memory cycle during a list acquisition.

During list acquisition, memory is not released until all four list words have been accessed. In state 2, the address register is incremented and a memory complete (MCOMP) signal is sent to the device controller. There is only one data available line coming from the CPU memory controller. The BTC must select the DATAV pulses that are for fetch cycles it initiated. The data available flip-flop (DATAVEN) is set in state 2 and is used to enable the data available latch (DATAVL). DATAVL resets DATAVEN. The subcontroller advances through state 3 (MC3/Q) to state 0. State 3 provides a 1-microsecond delay between consecutive fetch pulses.

4.9.2 MEMORY WRITE–DATA. When AGDEV,N– is high, STATBUSY low, and MEMREAD low, the subcontroller will be storing data and will advance to state 4. The device address lines (DEVADD) and the device data lines (DEVMWD) are enabled to the CPU when memory access is granted. In state 4 (MC4/Q), the store pulse (DEVSTORE–) is sent to the CPU memory controller and AR/Q is reset. The data to be stored is in either RF1 or RF2. The state of the register file control flip-flop (DRF1/Q) indicates which register file the data is stored in. If DRF1/Q is high, data is in RF1. If DRF1/Q is low, data is in RF2. The appropriate register file is selected to the RFOUT lines. The register file flip-flop (RF1/Q or RF2/Q) is reset when data is taken out of that register file and the subcontroller advances to state 5.

The register file flip-flops (RF1/Q and RF2/Q) outputs are used by the data subcontrollers (memory and device) to indicate where the next data word is to be stored or read from, and whether or not the register file is empty or full. In state 5 (MC5/Q), the address register is incremented, the DRF1/Q flip-flop toggled, and the subcontroller returns to state 0.

4.9.3 MEMORY WRITE STATUS. When AG is high, and STATBUSY high, the subcontroller will be storing status and will advance to state 6 (MC6/Q). When storing status, there may be one or two words to be stored as indicated by the two store cycles (TWOSC) signal from the device controller. The second word will be either the remaining data count in the data counter circuit or the starting address of the list that was being executed when the store status was requested. The count signal from the device controller selects the source of the second status word. The list address can be in either RF3 or RF4; RF4EN high indicates it is in RF4, and RF4EN low indicates it is in RF3. The second status word is being stored when status controller state 5 (SC5/Q) is high.

The first status word always comes from the device controller. The device controller puts this word on the RFOUT lines when STATBUSY and READY are both high. The first status word is not stored in the register file but goes directly to the DEVMWD lines. When two status words are to be stored (TWOSC) and the remaining data count is to be selected as the second status word (COUNT), then the data counter output (DCOUT) is gated onto the memory data input (DEVMWD) lines.

4.10 MEMORY DATA SUBCONTROLLER

The memory data subcontroller uses register file locations 1 and 2 as a 2-word buffer for data being transferred to or from memory. The memory data subcontroller starts a memory cycle (sets AR/Q) when the device is writing data and the register file is not full or if the device is reading data and the register file has data in it. AR/Q cannot be set if there is a memory cycle in progress. Figure 4-8 is a flowchart of the memory data subcontroller.

The register file that data will be stored in depends on the states of the DRF1/Q, RF1/Q and RF2/Q flip-flops. Table 4-5 illustrates the file that data will be stored in. Note that control flip-flop DRF1/Q is set to the true state when the memory data subcontroller enters the state MD1/Q. Subsequent control of the DRF1/Q flip-flop, until the next list is acquired, will be steered by the device data subcontroller. DRF1/Q will indicate to the device data subcontroller which register file location contains the next word to be written by the device, or the register file destination of the data read by the device.

Table 4-5. Register File Storage

	Signal State			
DRF1/Q	**RF1/Q**	**RF2/Q**	**Storage File**	**Access File**
H	L	X	RF1	RF1
H	H	X	RF2	RF1
L	X	H	RF1	RF2
L	X	L	RF2	RF2

Note: X = don't care

When the device is reading data and the BTC is transferring data to memory, the memory data subcontroller requests a memory cycle each time the register file buffer contains data [BUFRMTY (low), buffer empty false]. The memory data subcontroller selects the appropriate register file location for data to be transferred to memory. The device data subcontroller selects the appropriate register file location as destination for device data.

If the device is writing data, as soon as the memory enable (MEMEN–) signal is received from the device controller, the subcontroller issues requests for two words to fill the buffer (register file locations 1 and 2). After the buffer is full, the subcontroller initiates a memory cycle request every time a word is taken by the device controller. When the device is writing data, READY stays set as long as the buffer is not empty or status busy is not high.

If the BTC is fetching data from memory, the subcontroller advances to state 2 when AR/Q is set and waits for the DATAVL signal from the memory subcontroller, When DATALL is high, the data in the MRD register will be stored in RF1 or RF2.

4-11. DEVICE DATA SUBCONTROLLER

The device data subcontroller is the data interface with the device controller. Figure 4-9 is a flowchart for the device data subcontroller. The device data subcontroller supplies data when the device is writing and takes data when the device is reading. The MEMEN– signal enables the subcontroller and advances it to state 1 (DD1/Q). It will remain in state 1 until the next list

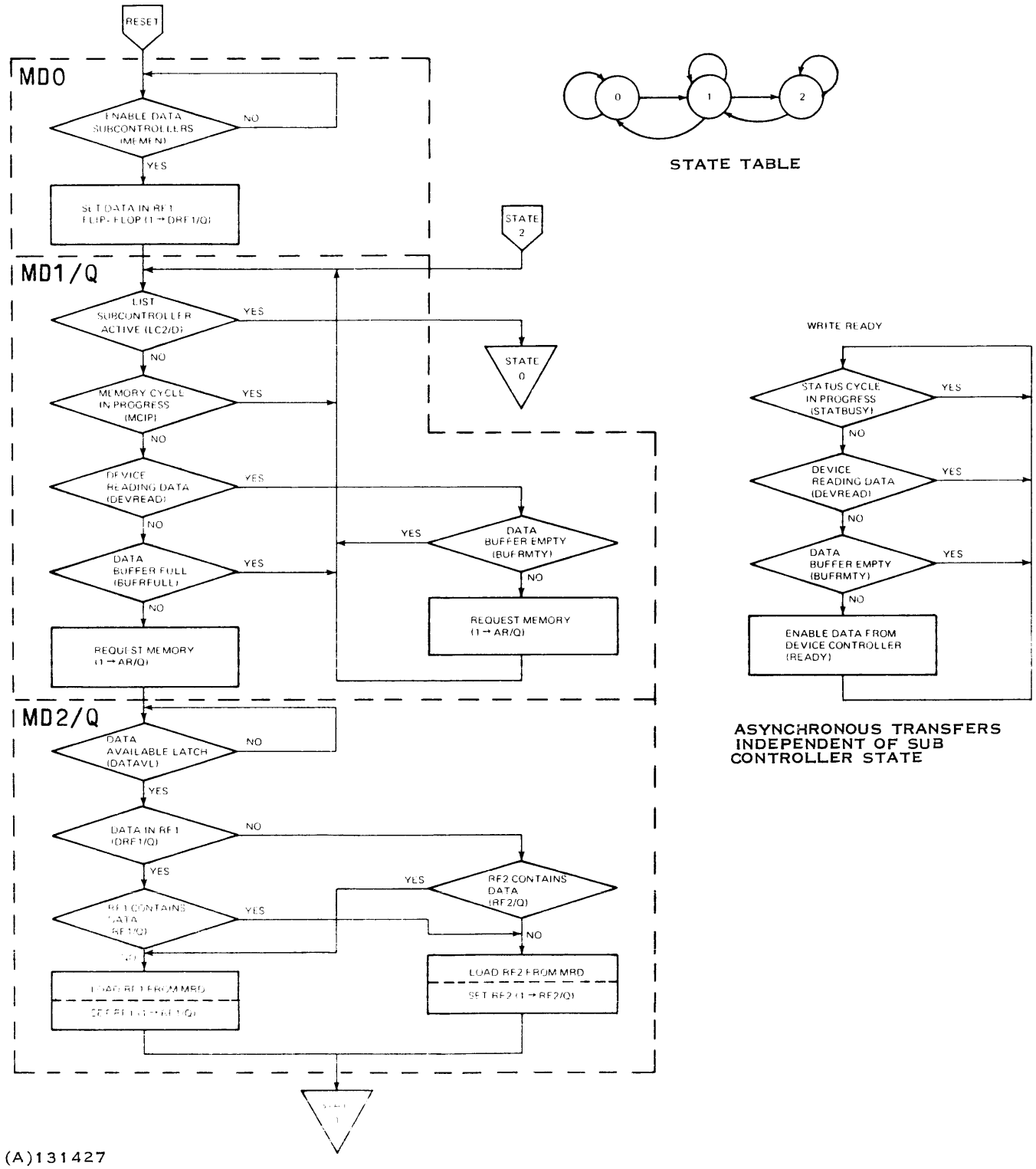


Figure 4-8. Memory Data Subcontroller Flowchart

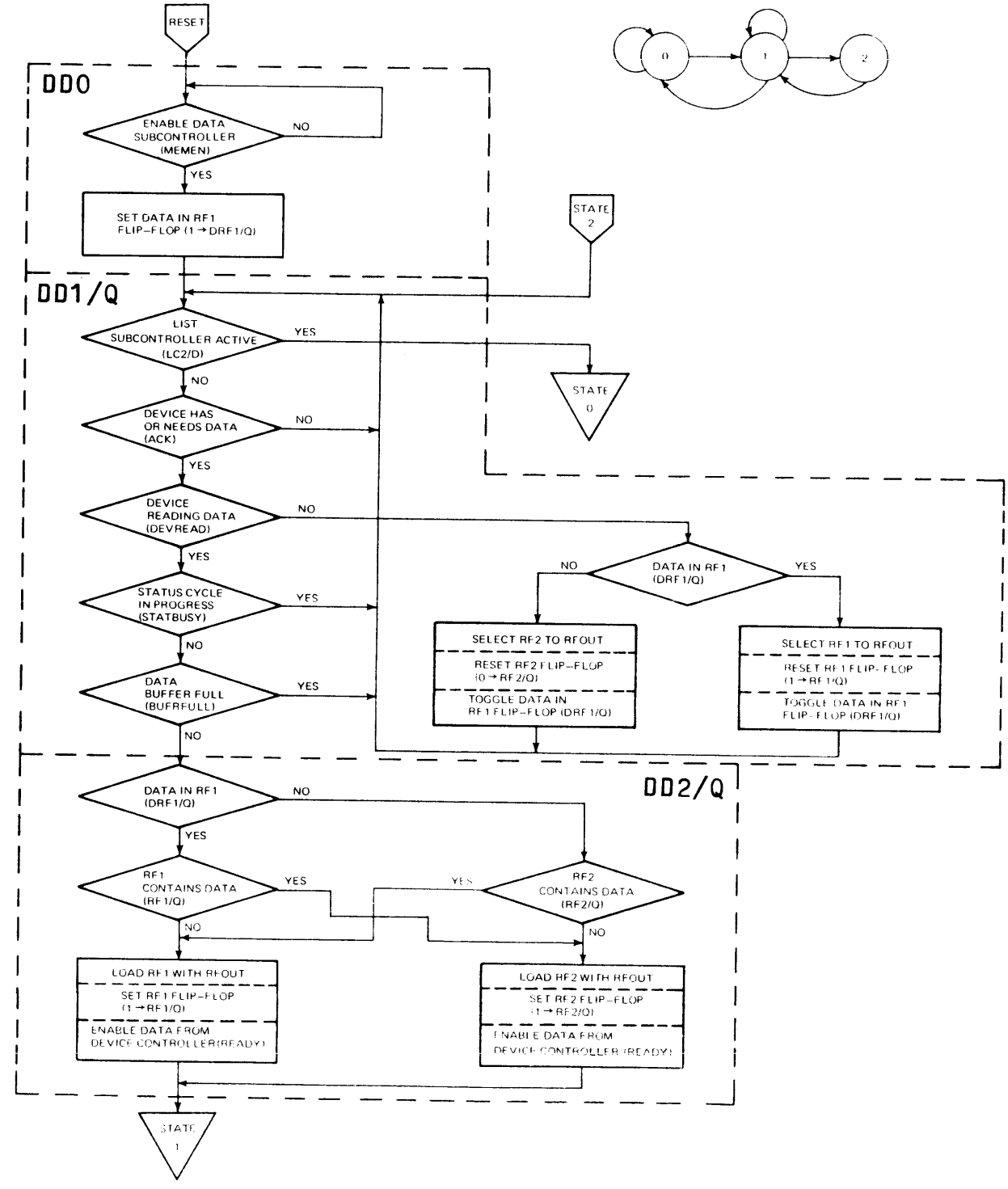


Figure 4-9. Device Data Subcontroller Flowchart

actuation (LC2/D + ATI2), and BTC clear (BTCLR–), or a reset (RESET–) occurs and then it will return to state 0. As the subcontroller advances, the register file 1 control flip-flop (DRF1/Q) is set. This flip-flop controls which register file (RF1 or RF2) the next data word will be taken from. Register file locations 1 and 2 have associated flip-flops (RF1/Q or RF2/Q) that are set when that register file contains a data word. DRF1/Q is toggled each time a word is taken from either RF1 or RF2. The device data subcontroller toggles DRF1/Q when the device is writing data; the memory subcontroller toggles DRF1/Q when the device is reading data.

When the device is writing data, DEVREAD is low. The memory data subcontroller sends the READY signal to the device controller when write data is available in the register file buffer. The device controller responds with the signal ACK– when it is ready to receive the data on the RFOUT bus. The device data subcontroller waits for the data request signal ACK–. The ACK– signal is low for one clock time. With these signal conditions set, DRF1/Q is checked for its state. If DRF1/Q is set, RF1 is selected to the RFOUT lines and RF1/Q is reset. If DRF1/Q is not set, RF2 is selected to the RFOUT lines and RF2/Q is reset. RF1 and RF2 are loaded and their flip-flops are set by the memory data subcontroller.

When the device is reading data, the ACK– signal remains high until the READY signal is sent to the device and the subcontroller advances to state 2, if the status subcontroller is not activated and the register file is not full. The register file full (BUFRFULL) signal is generated when both RF1 and RF2 contain data.

In state 2 (MC2/Q), data is clocked into RF1 or RF2 according to the signal levels on the DRF1/Q, RF1/Q, and RF2/Q signal lines. Table 4-5 illustrates the file that data is stored in for the specific states of DRF1/Q, RF1/Q, and RF2/Q.

4-12. STATUS SUBCONTROLLER

The status subcontroller is activated by the status enable (STATEN–) signal from the device controller. Figure 4-10 is a flowchart of the status subcontroller. If interrupt enable (INTEN–) is low, the subcontroller advances to state 2 (SC2/Q) with the next system clock. If INTEN– is high, it advances to state 3 (SC3/Q).

In state 2, the interrupt device (INTDEV,N–) signal for the selected channel (N = 0–7) to the CPU is enabled. The subcontroller remains in state 2 and INTDEV,N– remains low until interrupt recognized (IRECOG–) for the requesting channel is received from the CPU. IRECOG,N– and system clock advance the subcontroller to state 3.

In state 3, the subcontroller sets AR/Q if it is not already set and if ACK– is not high. AR/Q set means that some other subcontroller is using memory. ACK– low means that the device controller has data to transfer to or from the RFOUT bus. The access granted (AGDEV–) signal from the CPU activates the memory subcontroller. The memory subcontroller stores the status words.

In state 4 (SC4/Q) the subcontroller waits for a memory complete (MCOMP) signal from the memory subcontroller. If the two status cycles (TWOSC) signal is high, the data counter is decremented, and the subcontroller advances to state 5. If TWOSC is low, the data counter is not decremented, and the subcontroller returns to state 0. Status cycle busy (STATBUSY) will be high as long as the subcontroller is in state 4 or 5.

The data counter was loaded with a two's complement number. Therefore, when storing the data counter as the second status word, it must first be decremented and then inverted to store the correct count. At the end of the second status cycle, the data counter is incremented to get the counter back to a two's complement number. In state 5 (SC5/Q), the subcontroller waits for state 7 of the memory controller (MC7/Q), increments the data counter, and returns to state 0.

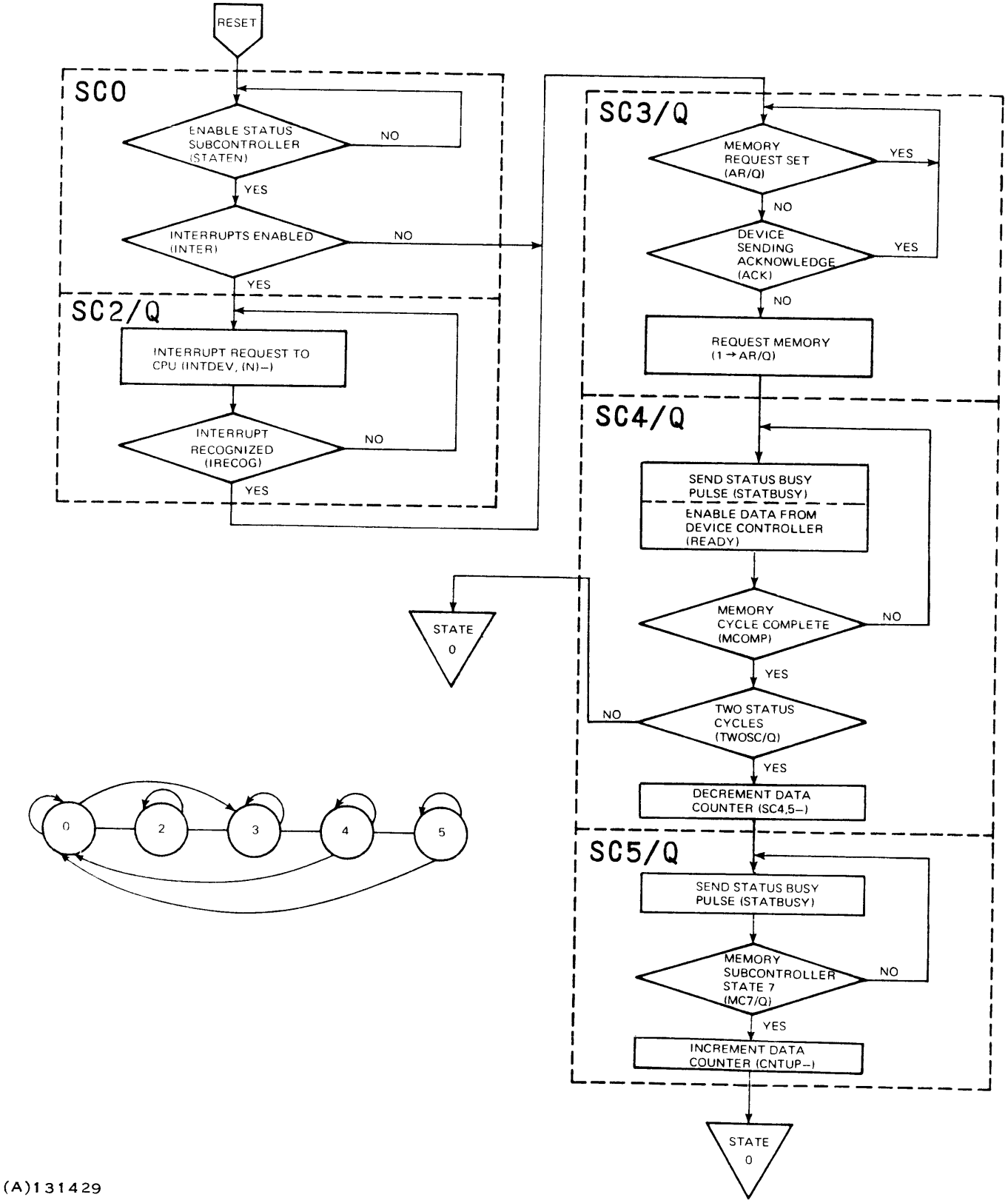


Figure 4-10. Status Subcontroller Flowchart

SECTION V

MAINTENANCE

5.1 GENERAL

This section contains maintenance information for circuit board isolation and replacement. Preventive maintenance is not required for the block transfer controller circuit boards.

5.2 FAULT ISOLATION

Fault isolation in any direct memory access system is complicated by the number of interfaces involved. A general list of the potential problem areas is given in table 5-1.

Table 5-1. Potential Problem Areas

System Area	Possible Component
CPU	1. AU circuit board. 2. Memory controller circuit board. 3. DMAC interface circuit board.
Internal Expansion	1. Cable–DMAC interface circuit board to BTC/DMAP adapter circuit board. 2. BTC/DMAP adapter board. 3. BTC circuit boards (3). 4. Device controller boards.
External Expansion	1. Cable–DMAC interface circuit board to expander circuit boards. 2. Expander circuit boards (4). 3. Expansion chassis power source and internal power supplies. 4. BTC circuit boards. 5. Device controller circuit boards.
Peripherial Device	1. Device controller circuit board to peripherial cable. 2. Peripherial device power source and internal power supplies. 3. Daisy-chain cabling to additional devices. 4. Cable terminators (if required).

Review the following suggestions to help isolate the cause of a system failure.

1. Visually inspect the system for the following conditions:

   a. AC power available and power switches turned on.

   b. Circuit boards oriented correctly and in correct locations (refer to Section II Installation).

   c. Peripheral devices are powered correctly and on line.

d. All connecting cables in place and secure.

e. Line terminators installed in peripherals (if required).

2. Check the channel address on BTC No. 1 circuit card and ensure that it agrees with the requirements of the software being executed. Ensure that no other BTC No. 1 circuit card has the same channel address.

3. Perform the device performance demonstration test (PDT). PDT kits are provided with each DMA peripheral. The kit includes object code in the appropriate media, and operating instructions which include the source listings and flowcharts. Again, ensure that the channel address on BTC No. 1 circuit card is the address required by the PDT, and that following testing, it is returned to the address required by the system software.

4. If the PDT fails to execute properly, check for a device failure. The peripheral is the most likely failure due to its mechanical nature. Test the device offline, if possible. Inspect and clean read or write mechanisms where applicable.

5. Perform the PDTs of other devices in the system to verify that the CPU to DMA interface is operating correctly.

6. Exchange the block transfer controller circuit cards of the failed device with the block transfer controller circuit cards of a device that is operating properly. Ensure that the channel address is changed when interchanging boards. The circuitry on the individual circuit cards is as follows:

Board Name	Circuits on Board
BTC No. 1	Initialization subcontroller, Memory read data, and Register files.
BTC No. 2	Memory subcontroller, Data subcontroller, Address register, and Memory write data.
BTC No. 3	Device data subcontroller, Memory data subcontroller, List subcontroller, and Status subcontroller.

7. Verify that the CPU is functioning properly by performing the CPU Performance Assurance Tests contained in the documentation kit.

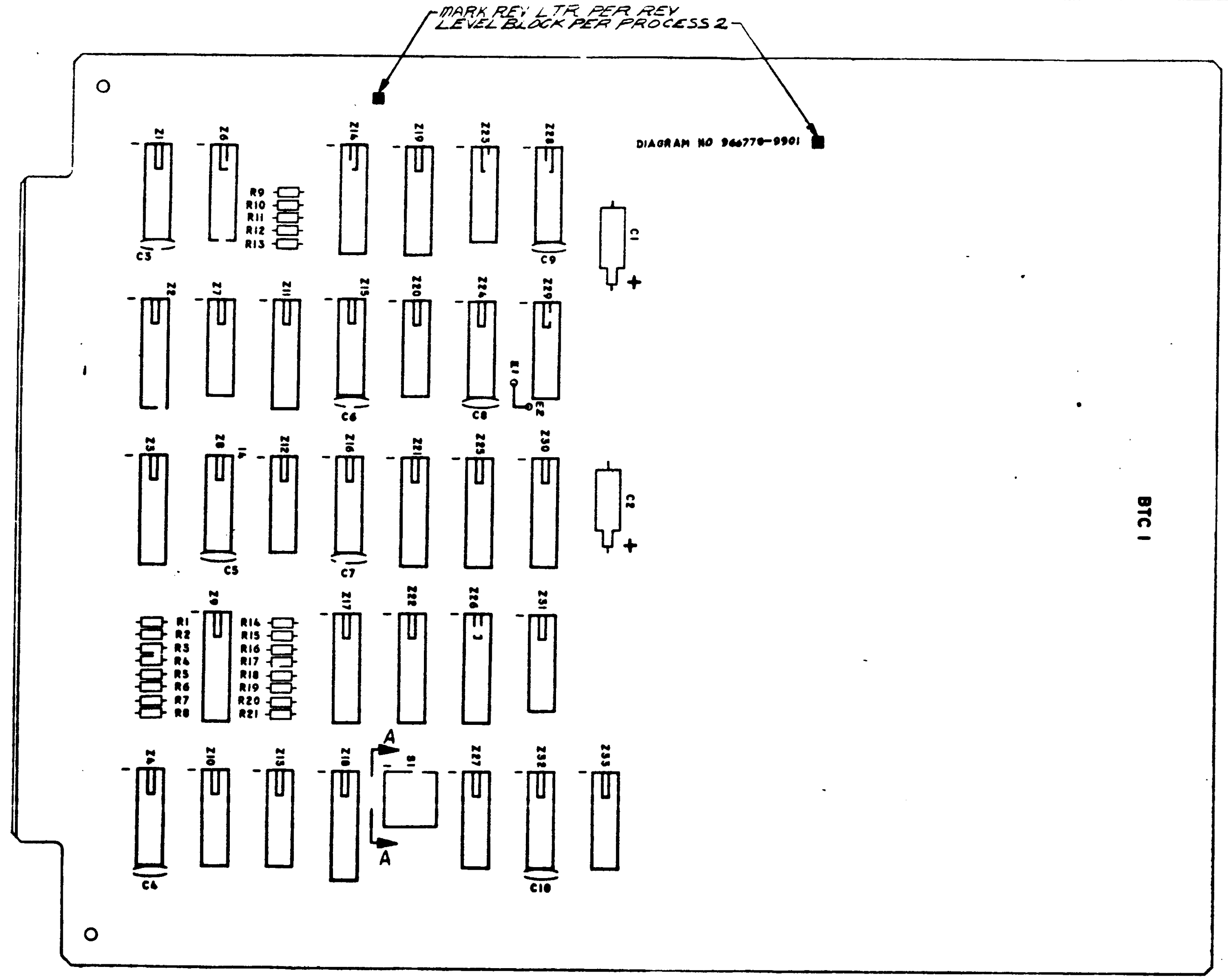
8. Remove all other device controllers and their associated block transfer controller circuit cards to eliminate any possible interaction between the failing controller and the other controllers in the system. Perform the PDT for the device associated with the failing controller.

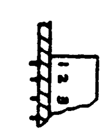
SECTION VI

PARTS LIST

6.1 GENERAL

This section contains assembly drawings and parts lists for the block transfer controller circuit boards. The block transfer controller is implemented on both multilayer and wire wrap circuit boards. The drawings for both types of circuit boards are included in this section.





SECTION A-A
SCALE: NONE

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	374189 (D) ... 3/22/73 ADDED 1) PROCESS 2 REV LTR BLOCK 2) DIAGRAM NO ...	4/29/73	
	B	386001 (B) 8-31-73 1. Added NOTE 4 & ITEM 21 TO L/M & E1 & E2 A/D		
	C	N 384505 (C) (1) UPDATED REV STATUS BLOCK (2) ADDED ITEM 22 TO L/M	5/7/74	
	D	CN 393235 (E) (1) ITEM 15 WAS 772923-0002 (2) UPDATED REV LEVEL BLOCK	7/25/74	
	E	397338 (C) (1) REVISED REVISION BLOCK	1/4/75	
	F	383751 (C) (1) UPDATED REV LEVEL BLOCK	7/16/75	
	G	383789 (D) (1) UPDATED REV LEVEL BLOCK	11/5/75	
	H	407377 (C) (1) UPDATED REV LEVEL BLOCK	7/16/76	
	J	411208 (C) S. Vallejo (1) DELETED NOTE 4 (2) UPDATED REV LEVEL BLOCK		

NOTES:

1. MAXIMUM COMPONENT HEIGHT FROM COMPONENT SIDE OF BOARD IS .31
2. MAXIMUM LEAD LENGTH FROM CONDUCTOR SIDE OF BOARD IS .075
3. TO PREVENT SOLDER FROM WICKING DOWN CONNECTOR FINGERS, WHEN SOLDERING, MASK ALL CONNECTOR FINGERS ON BOTH SIDES OF BOARD
4. ~~ADD JUMPER WIRE FROM E1 TO E2 (ITEM 21) FOR ALL APPLICATIONS. MEMORY READ DATA PARITY CHECKER INHIBITED WITH E1 TO E2 JUMPERED. PARITY CHECKER NOT USED FOR ANY STANDARD APPLICATIONS.~~

PROCESSES:

1. SOLDER ALL ELEC COMPONENTS PER F-124 AND/OR F-127
2. RUBBER STAMP, F-100, HEIGHT .12, COLOR BLACK

REV LEVEL

LOGIC DIAGRAM FOR -0001 (965778-9901)				A	A	B	B	B	B	B	C
PRINTED WIRING BOARD FOR -0001 (966467-0001)					C	C	E	G	H		
MASTER FILE FOR -0001 (966586-9901)			R			A	A	A	A	A	
ASSEMBLY			A	B		D	E	F	G	H	J

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIR
- DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
- IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
- INTERPRET DRAWING IN ACCORDANCE WITH MIL STD 100

HOLE TOLERANCE: .013 THRU .125 +.004 −.001; .126 THRU .250 +.005 −.001; .251 THRU .500 +.006 −.001; .501 THRU .750 +.008 −.001; .751 THRU 1.000 +.010 −.001; 1.001 THRU 2.000 +.012 −.001

NEXT ASSY	USED ON
965810	7503
COMMON	7503
COMMON	7502
COMMON	-100/-101

APPLICATION

QTY REQD -2	QTY REQD -1	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±1°; 3 PLACE DECIMALS ±.010; 2 PLACE DECIMALS ±.02

MATERIAL

DWN B. Nelson 1-10-73
CHK 5 Jan 73
ENGR 1-18-73
1-18-73
APVD 2/5/73
CONTR NO
DESIGN ACTIVITY RELEASE 1/13/72

TEXAS INSTRUMENTS INCORPORATED, Equipment Group, Dallas, Texas

BTC #1, PWB ASSY

SIZE D | CODE IDENT NO 96214 | DRAWING NO 966466
SCALE 1/1 | SHEET

32

TEXAS INSTRUMENTS INCORPORATED

DATE 05/01/75 — **LIST OF MATERIAL** — PAGE 1 of

PART NUMBER LM 966466-0001 REV J

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		966467-0001	PW BD-BTC 1	
0002	00003.000	EA		222222-7400	NETWORK SN7400N	-SN7400N
0002A					Z10,Z28,Z31	
0003	00001.000	EA		222222-7402	NETWORK SN7402N	TI--SN7402N
0003A					Z8	
0004	00003.000	EA		222222-7404	NETWORK SN7404N	
0004A					Z4,Z6,Z7	
0005	00001.000	EA		222222-7408	NETWORK-SN7408N	
0005A					Z27	
0006	00002.000	EA		222222-7410	NETWORK SN7410N	-SN7410N
0006A					Z12,Z23	
0007	00002.000	EA		222222-7437	NETWORK SN7437N	
0007A					Z1,Z13	
0008	00003.000	EA		222222-7474	NETWORK SN7474N	-SN7474N
0008A					Z15,Z29,Z32	
0009	00002.000	EA		222222-7486	NETWORK-SN7486N	
0009A					Z24,Z33	
0010	00004.000	EA		222222-7170	NETWORK SN74170N	
0010A					Z9,Z19,Z25,Z26	
0011	00004.000	EA		222222-7174	NETWORK SN74174N	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: BTC 1,PWB ASSY

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO 8101 | PART NUMBER LM 966466-0001 REV J

TEXAS INSTRUMENTS INCORPORATED

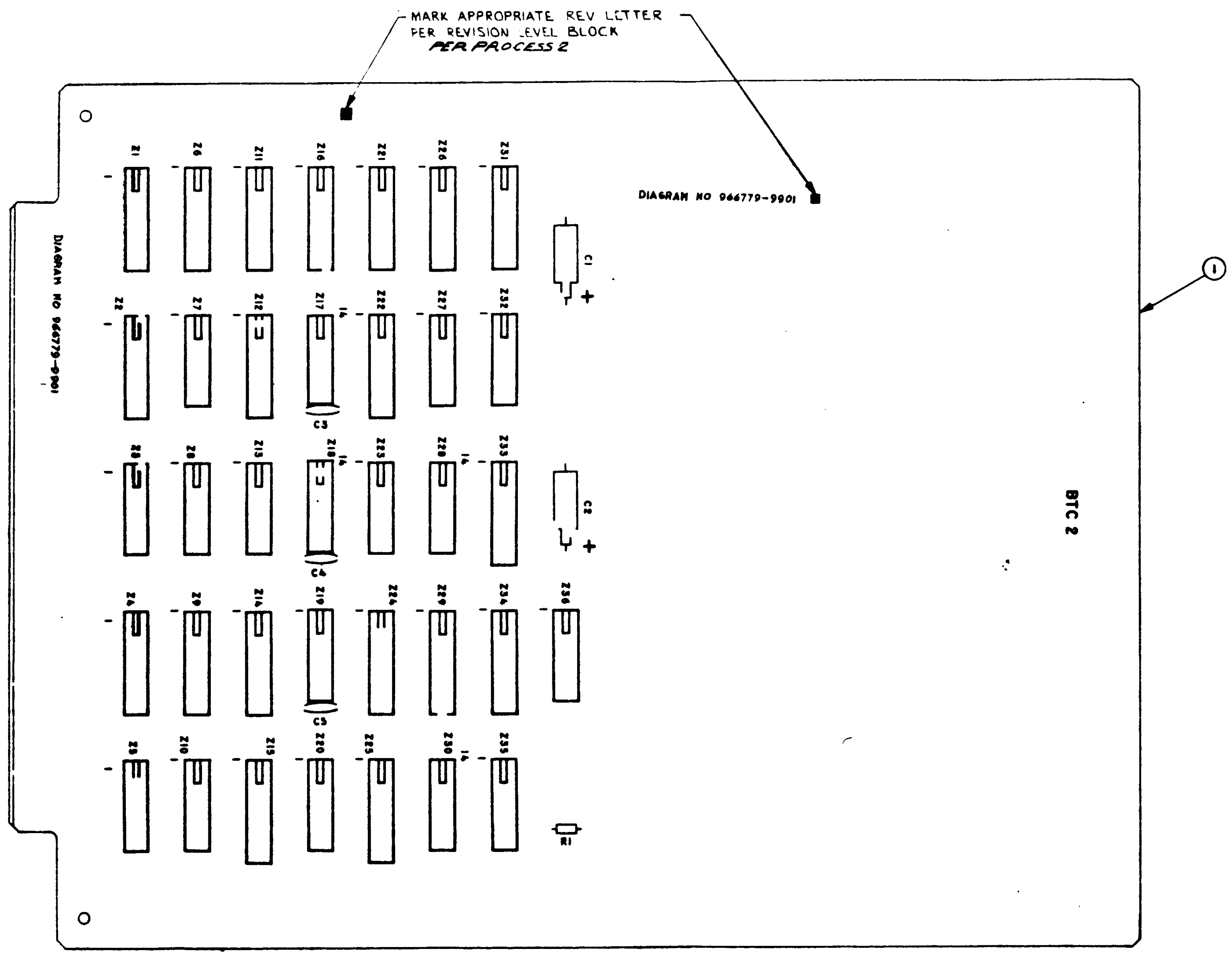
DATE 05/01/75 — **LIST OF MATERIAL** — PAGE 2 of

PART NUMBER LM 966466-0001 REV J

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0011A					Z2,Z3,Z11,Z17	
0012	00001.000	EA		222222-7175	NETWORK SN74175N	
0012A					Z30	
0013	00002.000	EA		222222-7180	NETWORK SN74180N	
0013A					Z16,Z20	
0014	00004.000	EA		244712-8266	NETWORK-8266 2-INPUT,4-BIT DIGITAL MXPR	
0014A					Z14,Z18,Z21,Z22	
0015	00001.000	EA		972547-0005	SWITCH,SLIDE-SPST,DIP 5 SWITCHES	KEE-CTS206005
0015A					S1	
0016	00002.000	EA		972924-0010	CAP FIX TANT SOLID 22 MFD 10 % 15 VOLT	QPL-M39003/1-2271
0016A					C1,C2	
0017	00008.000	EA		230590-9000	CAP .05 MF 12 V 20. % CER TRANSCAP	ERI-5635-000-Y5F0503M
0017A					C3 THRU C10	
0018	00021.000	EA		972975-0041	RES FIX COMP 470 OHMS 5 % 1/8 WATT	QPL- RC05G471JS
0018A					R1 THRU R21	
0019	REF	EA		966586-9901	SOURCE TAPE,MASTERFILE-BTC	
0020	REF	EA		966778-9901	DIAGRAM,LOGIC,DET-BTC #1 (PWB)	
0021	00001.000	FT		417671-3999	WIRE HOOKUP 28 AWG TYPE ET INS WHITE	QPL- MIL-W-16878/6A
0022	REF	EA		973601-9901	TEST PROCEDURE,BTC #1	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: BTC 1,PWB ASSY

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM 966466-0001 REV J



ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	381111 (D) 3/16/73 G. Amas LM: 1) ADDED Z5 & Z32 TO ITEM 3A 2) ADDED Z3 & Z8 TO ITEM 5A 3) ITEM 7A DELETED Z25 & ADDED Z30	3/13/73	Booth
	B	374189 (D) 6/22/73 1) ADDED DIAGRAM NO & PER PROCESS 2		
	C	386002(D) 8-31-73 CHG 1) MASTER FILE DECK TO DIAGRAM LOGIC 2) TITLE WAS "BTC 2". ADDED DIAGRAM LOGIC TO REV LEVEL BLOCK		
	D	396449 (C) (1) L/M; ADDED ITEM 21 (2) UPDATED REV LEV BLK	1/7/74	
	E	394634 (C) (1) UPDATED REV LEVEL BLOCK	1/16/75	
	F	383739 (D) (1) UPDATED REV LEVEL BLOCK	1/5/75	
	G	413221 (C) (1) UPDATED REV LEVEL BLOCK	6/25/76	

NOTES:

1. MAXIMUM COMPONENT HEIGHT FROM COMPONENT SIDE OF BOARD IS .31
2. MAXIMUM LEAD LENGTH FROM CONDUCTOR SIDE OF BOARD IS .075
3. TO PREVENT SOLDER FROM WICKING DOWN CONNECTOR FINGERS, WHEN SOLDERING, MASK ALL CONNECTOR FINGERS ON BOTH SIDES OF BOARD

PROCESSES:

1. SOLDER ALL ELEC COMPONENTS PER F-124 AND/OR F-127
2. RUBBER STAMP, F100, HEIGHT .12, COLOR BLACK

REV LEVEL										
PRINTED WIRING BOARD FOR -0001 (966465-0001)			A			B			D
DIAGRAM LOGIC, DET-BTC #2 (PWB) FOR-0001 (966779-9901)	★					A		A	A
ASSEMBLY	★	★	A			D		F	G

-2	-1	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION
QTY REQD						

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIR
- DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
- IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
- INTERPRET DRAWING IN ACCORDANCE WITH MIL STD 100

HOLE TOLERANCE

APPLICATION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES
ANGLES ±1
3 PLACE DECIMALS ±.010
2 PLACE DECIMALS ±.02

MATERIAL

DWN 1-8-73
CHK JAN 73
ENGR 1-18-73
1-18-73
CONTR NO
DESIGN ACTIVITY RELEASE

TEXAS INSTRUMENTS INCORPORATED
Equipment Group Dallas Texas

BTC 2, PWB ASSY

SIZE D | CODE IDENT NO 96214 | DRAWING NO 966464
SCALE 1/1 | SHEET

32

TI-79141 PS

TEXAS INSTRUMENTS INCORPORATED

DATE 05/01/75 — **LIST OF MATERIAL** — PAGE 1 of

LM PART NUMBER 9E6464-0001 REV G

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		9E6465-0001	PW BD-BTC 2	
0002	00002.000	EA		222222-7400	NETWORK SN7400N	-SN7400N
0002A					Z20,Z35	
0003	00002.000	EA		222222-7402	NETWORK SN7402N	TI--SN7402N
0003A					Z5,Z32	
0004	00001.000	EA		222222-7404	NETWORK SN7404N	
0004A					Z19	
0005	00003.000	EA		222222-7405	NETWORK SN7405N	
0005A					Z3,Z7,Z8	
000E	00001.000	EA		222222-740E	NETWORK-SN740EN	
000EA					Z13	
0007	00002.000	EA		222222-7408	NETWORK-SN7408N	
0007A					Z10,Z30	
0008	00002.000	EA		222222-748E	NETWORK-SN748EN	
0008A					Z23,Z3E	
0009	00004.000	EA		222222-7157	NETWORK SN74157N	
0009A					Z4,Z9,Z14,Z15	
0010	00002.000	EA		222222-7174	NETWORK SN74174N	
0010A					Z24,Z25	
0011	00001.000	EA		222222-7175	NETWORK SN74175N	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: BTC 2,PWB ASSY

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO: 8100/9101 | LM PART NUMBER 9E6464-0001 REV G

TEXAS INSTRUMENTS INCORPORATED

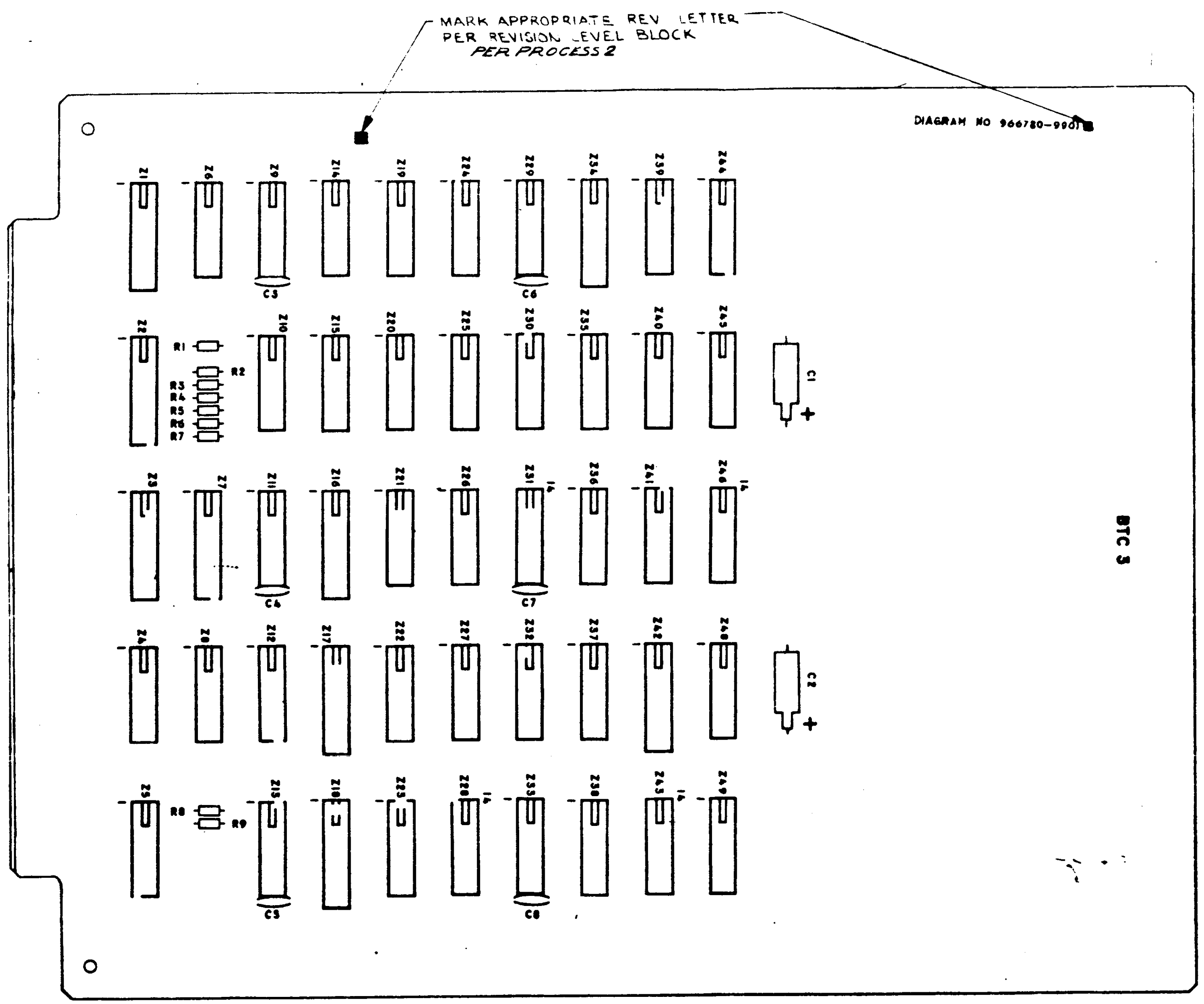
DATE 05/01/75 — **LIST OF MATERIAL** — PAGE 2 of

LM PART NUMBER 9E6464-0001 REV G

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0011A					Z33	
0012	00003.000	EA		222222-7180	NETWORK SN74180N	
0012A					Z18,Z27,Z28	
0013	00008.000	EA		222222-7193	NETWORK SN74193N	-SN74193N
0013A					Z11,Z16,Z21,Z22,Z26,Z29,31,	
0013B					Z34	
0014	00001.000	EA		240000-7411	NETWORK-SN74H11N	
0014A					Z17	
0015	00004.000	EA		244712-8267	NETWORK,DM82678	
0015A					Z1,Z2,Z6,Z12	
001E	00001.000	EA		972975-0041	RES FIX COMP 470 OHMS 5 % 1/8 WATT	QPL- RC05G471JS
001EA					R1	
0017	00003.000	EA		230590-9000	CAP .05 MF 12 V 20. % CER TRANSCAP	ERI-5E35-000-Y5F0503M
0017A					C3,C4,C5	
0018	00002.000	EA		972924-0010	CAP FIX TANT SOLID 22 MFD 10 % 15 VOLT	QPL-M39003/1-2271
0018A					C1,C2	
0019	REF	EA		9E658E-9901	SOURCE TAPE,MASTERFILE-BTC	
0020	REF	EA		9E6779-9901	DIAGRAM,LOGIC,DET-BTC #2 (PWB)	
0021	REF	EA		973E02-9901	TEST PROCEDURE,BTC #2	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: BTC 2,PWB ASSY

APPD MFG DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | LM PART NUMBER 9E6464-0001 REV G



ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	374189(D) [illegible] ADDED 1) ITEM 21 TO LM, 2) [illegible] 3) [illegible] 2 PER THE LTR	[illegible]	[illegible]
	B	386003(D) 8-31-73 CHG 1) MASTER FILE DECK TO DIAGRAM LOGIC 2) TITLE WAS "BTC 3" ADDED DIAGRAM LOGIC TO REV LEVEL BLOCK	[illegible]	[illegible]
	C	396448(C) [illegible] (1) [illegible], ADDED ITEM 22 (2) UPDATE REV LEV BLK	7/30/74	[illegible]
	D	392350(D) (1) UPDATED REV LEVEL BLOCK	1/14/75	[illegible]
	E	383752(C) (1) UPDATED REV LEVEL BLOCK	7/16/75	[illegible]
	F	CN 383789 (D) (1) UPDATED REV LEVEL	11/5/75	[illegible]
	G	CN 413220 (C) (1) UPDATED REV LEVEL BLOCK	4/25/76	[illegible]
	H	CN 417324 (C) (1) ADDED NOTE 4 (2) UPDATED REV LEVEL BLOCK (3) ADDED ITEM 23 TO LM	9/21/76	[illegible]

NOTES:

1. MAXIMUM COMPONENT HEIGHT FROM COMPONENT SIDE OF BOARD IS .31
2. MAXIMUM LEAD LENGTH FROM CONDUCTOR SIDE OF BOARD IS .075
3. TO PREVENT SOLDER FROM WICKING DOWN CONNECTOR FINGERS, WHEN SOLDERING, MASK ALL CONNECTOR FINGERS ON BOTH SIDES OF BOARD
4. CUT Z4 PIN 8 AND ISOLATE FROM ETCH. ADD THE FOLLOWING WIRES USING ITEM 23:

FROM:	TO:
Z4-8	Z49-9
Z35-10	Z49-10
Z49-8	Z21-1

PROCESSES:

1. SOLDER ALL ELEC COMPONENTS PER F-124 AND/OR F-127
2. RUBBER STAMP, F 100. HEIGHT .12, COLOR BLACK

REV LEVEL

PRINTED WIRING BOARD FOR -0001 (966463-0001)	*	A	B	B	C	D	F	G	G
DIAGRAM LOGIC, DET-BTC #3 (PWB) FOR-0001 (966780-9901	*	*	*	A	A	B	B	E	E
ASSEMBLY	*	*	A	C	D	E	F	G	H

-2	-1	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION
QTY REQD						

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIR
- DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
- IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
- INTERPRET DRAWING IN ACCORDANCE WITH MIL STD 100

HOLE TOLERANCE

.013 THRU .125 ± .004 / .001	.126 THRU .250 ± .005 / .001	.251 THRU .500 ± .006 / .001
.501 THRU .750 ± .008 / .001	.751 THRU 1.000 ± .010 / .001	1.001 THRU 2.000 ± .012 / .001

NEXT ASSY | USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES ANGLES ± 1°
3 PLACE DECIMALS ± .010
2 PLACE DECIMALS ± .02

MATERIAL

DWN K. Vakil DATE 1-9-73

CHK

ENGR 1-18-73

APP

CONTR NO

DESIGN ACTIVITY RELEASE

TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas Texas

BTC 3, PWB ASSY

SIZE D | CODE IDENT NO 96214 | DRAWING NO 966462

SCALE 1/1 | SHEET

32

TEXAS INSTRUMENTS INCORPORATED

DATE 05/16/76 — **LIST OF MATERIAL** — PAGE 1 of

PART NUMBER LM966462 -0001 REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		966463 -0001	PW EC- BTC 3	
0002	00010.000	EA		222222 -7400	NETWORK SN7400N	-SN7400N
0002A					Z9,Z11,Z14,Z19,Z24,Z25,Z33,	
C002B					Z40,Z46,Z48	
0003	00004.000	EA		222222 -7402	NETWORK SN7402N	TI- -SN7402N
C003A					Z12,Z23,Z27,Z44	
C004	00005.000	EA		222222 -7404	NETWORK SN7404N	
C004A					Z4,Z6,Z26,Z35,Z45	
C005	00004.000	EA		222222 -7408	NETWORK-SN7408N	
C005A					Z5,Z15,Z28,Z49	
0006	00006.000	EA		222222 -7410	NETWORK SN7410N	-SN7410N
C006A					Z8,Z30,Z32,Z36,Z37,Z41	
C007	00002.000	EA		222222 -7420	NETWORK SN7420N	-SN7420N
C007A					Z22,Z31	
C008	00004.000	EA		222222 -7451	NETWORK SN7451N	-SN7451N
C008A					Z20,Z21,Z38,Z39	
0009	00001.000	EA		222222 -7474	NETWORK SN7474N	-SN7474N
C009A					Z29	
0010	00001.000	EA		222222 -7486	NETWORK-SN7486N	
C010A					Z13	

DRAFTSMAN DATE — CRD DRAFTSMAN 9/11/76 DATE — DESIGN ENGINEER DATE — TITLE: BTC 3,PWB ASSY

APPD MFG DATE — APPD PROJECT ENGINEER DATE — RELEASED DATE — PROJECT NO 5100/8101

PART NUMBER LM966462 -0001 REV H

TEXAS INSTRUMENTS INCORPORATED

DATE 05/16/76 — **LIST OF MATERIAL** — PAGE 2 of

PART NUMBER LM966462 -0001 REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0011	00001.000	EA		222222 -7495	NETWORK SN7495N	-SN7495N
0011A					Z43	
0012	00002.000	EA		222222 -7145	NETWORK SN74145N	
C012A					Z2,Z3	
0013	00002.000	EA		222222 -7151	NETWORK SN74151N	
0013A					Z1,Z7	
0014	00002.000	EA		222222 -7174	NETWORK SN74174N	
C014A					Z17,Z34	
0015	00003.000	EA		222222 -7175	NETWORK SN74175N	
0015A					Z16,Z18,Z42	
0016	00001.000	EA		240000 -7411	NETWORK-SN74H11N	
0016A					Z10	
0017	00002.000	EA		972924 -0010	CAP FIX TANT SOLID 22 MFD 10 % 15 VOLT	QPL -M39003/1-2271
C017A					C1,C2	
0018	00006.000	EA		230590 -9000	CAP .05 MF 12 V 20. % CER TRANSCAP	ERI -5635-000-Y5F05
C018A					C3 THRU C8	
0019	00009.000	EA		972975 -0041	RES FIX COMP 470 OHMS 5 % 1/8 WATT	QPL - RC05G471JS
C019A					R1 THRU R9	
C020	REF	EA		966586 -9901	SOURCE TAPE,MASTERFILE-BTC	
C021	REF	EA		966780 -9901	DIAGRAP,LCCIC,DET-BTC #3 (PWB)	

DRAFTSMAN DATE — CRD DRAFTSMAN DATE — DESIGN ENGINEER DATE — TITLE: BTC 3,PWB ASSY

APPD MFG DATE — APPD PROJECT ENGINEER DATE — RELEASED DATE — PROJECT NO

PART NUMBER LM966462 -0001 REV H

TEXAS INSTRUMENTS
INCORPORATED

DATE 05/16/74 **LIST OF MATERIAL** PAGE 3 of

PART NUMBER LM966462 -0001 REV H

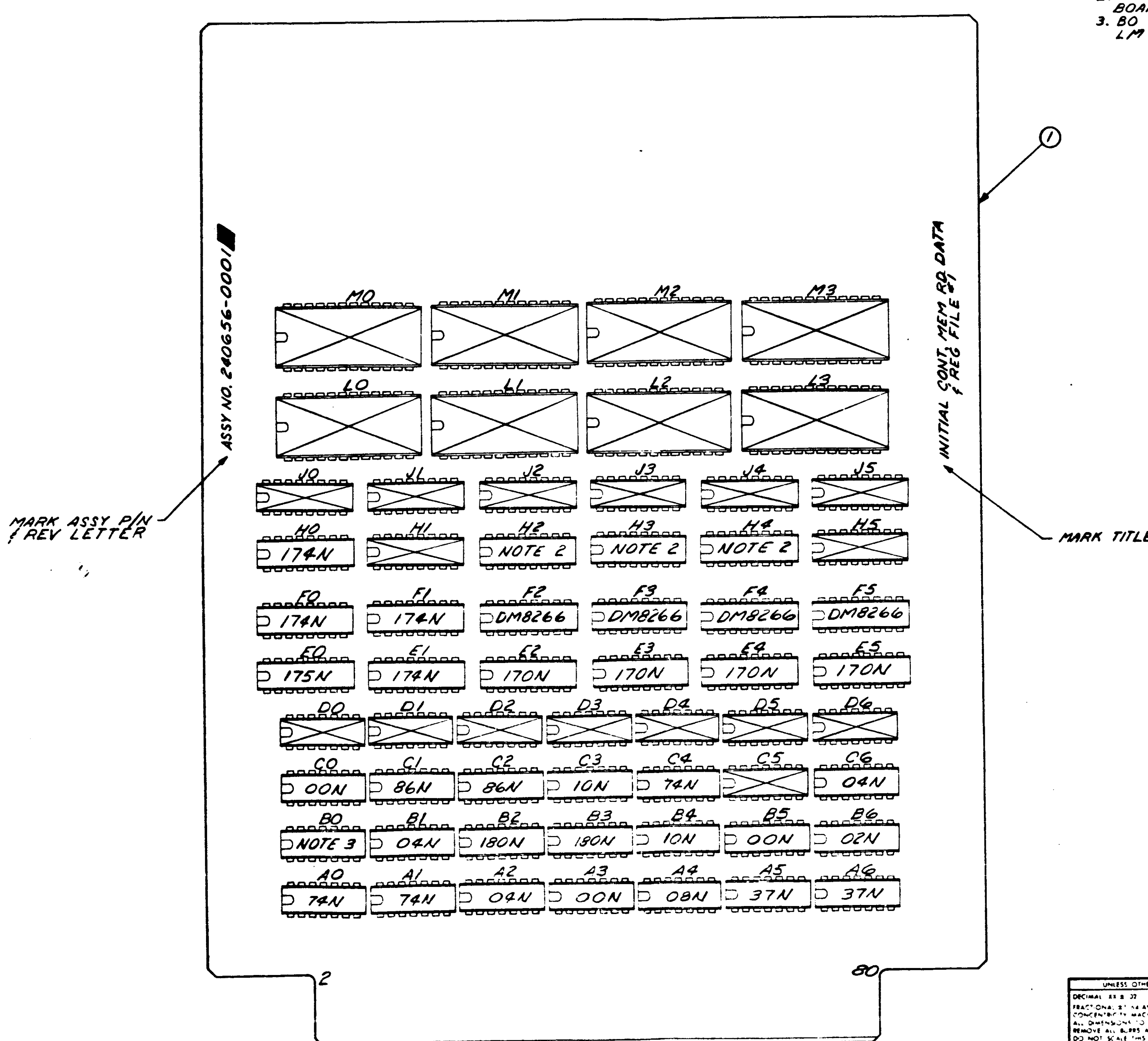
ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
C022	REF	EA		973603 -9901	TEST PROCECURE, BTC#3	
0023	AR	EA		535578 -CC06	WIRE, ELEC, SOLID, 24AWG	

DRAFTSMAN	DATE	CAD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						BTC 3,PWB ASSY
APPD MFG	DATE	APPD PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO

PART NUMBER LM966462 -0001 REV H

NOTES: UNLESS OTHERWISE SPECIFIED
1. NETWORKS ARE SN74 SERIES
2. H2, H3, & H4 ARE TERM. BOARDS LM ITEM NO. 15
3. B0 IS A WIRED PLUG LM ITEM NO. 16

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
A	365974(E) 11-2-72 F/D: INSERT ⊠ FOR ALL UNUSED LOCATIONS L/M: ITEM 14 QTY WAS 5	11/2/72	
B	374189(D) 1/22/73 ADDED ITEM 17 TO LM		



-0002	-0001	ITEM NO	UNIT OF MEAS	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
QTY REQD						LIST OF MATERIALS	

UNLESS OTHERWISE SPECIFIED
DECIMAL .XX ± .02 .XXX ± .010
FRACTIONAL ± 1/64 ANGULAR ± 1°
CONCENTRICITY MACHINED DIAMETERS .004 TIR
ALL DIMENSIONS TO BE MET BEFORE PLATING
REMOVE ALL BURRS AND SHARP EDGES
DO NOT SCALE THIS DRAWING
ALL DIMENSIONS IN INCHES
SURFACES MARKED ✓ TO HAVE ✓
DRILLED HOLE TOLERANCES
.013 TO .136 +.003 −.002 .136 TO .250 ±.003 .250 AND ABOVE ±.003

PROCESSES
1. RUBBER STAMP F10C, HEIGHT .12, COLOR BLK

NEXT ASSY: 8960/8980 | SIZE: A | DWG NO: 217536

TEXAS INSTRUMENTS INCORPORATED
INDUSTRIAL PRODUCTS DIVISION
HOUSTON, TEXAS

INITIAL CONT. MEM RD DATA & REG FILE #1
BLOCK TRANSFER CONT
COMPUTER

SCALE: NONE D 240656

TEXAS INSTRUMENTS INCORPORATED

DATE 05/01/75 **LIST OF MATERIAL** PAGE 1 of

LM PART NUMBER 240656-0001 REV B

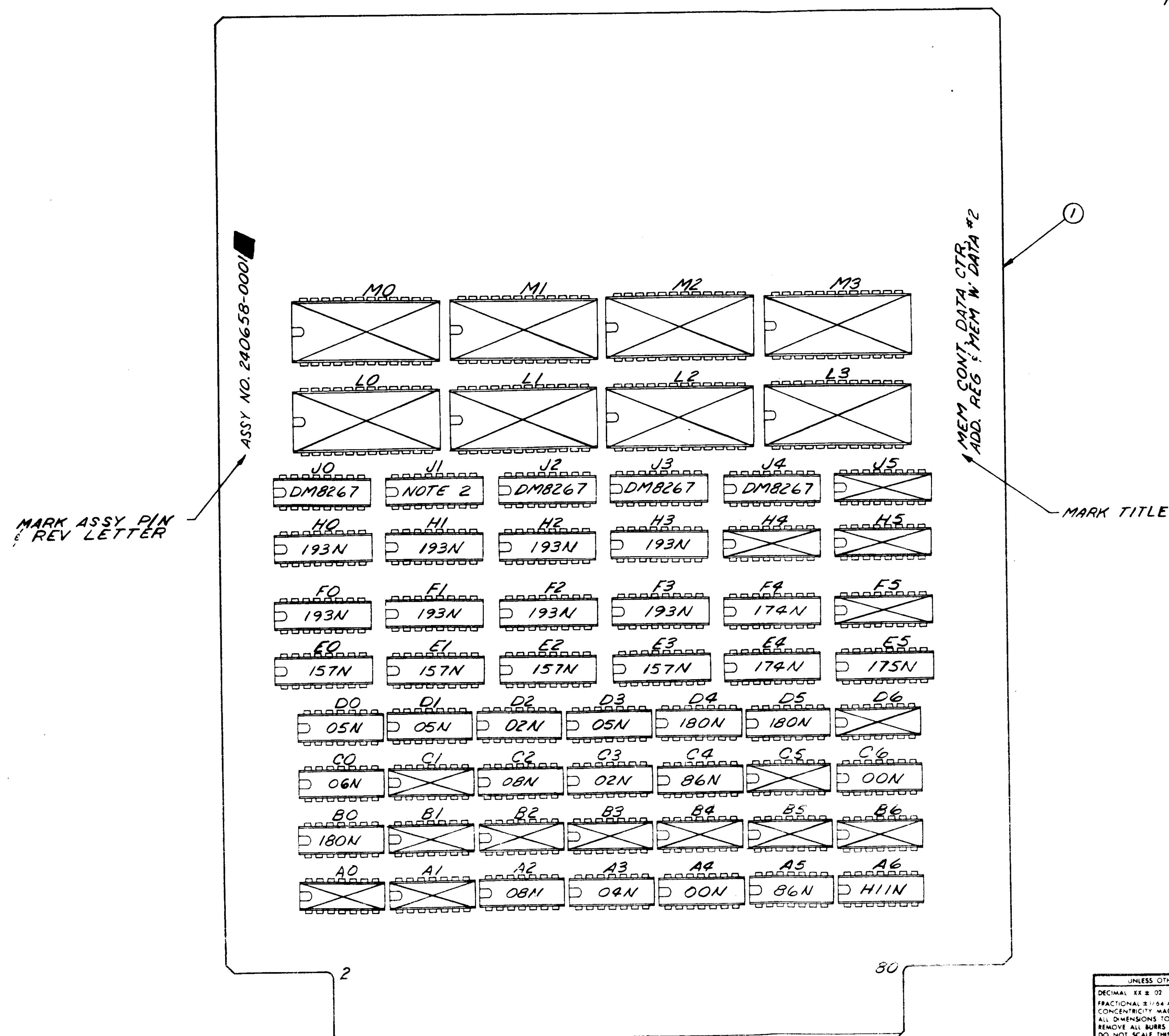
PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		240655-0001	INITIAL CONT,MEM RD DATA&REG FILE ASSY	
0002	00003.000	EA		222222-7400	NETWORK SN7400N	-SN7400N
0003	00001.000	EA		222222-7402	NETWORK SN7402N	TI--SN7402N
0004	00003.000	EA		222222-7404	NETWORK SN7404N	
0005	00001.000	EA		222222-7408	NETWORK-SN7408N	
0006	00002.000	EA		222222-7410	NETWORK SN7410N	-SN7410N
0007	00002.000	EA		222222-7437	NETWORK SN7437N	
0008	00003.000	EA		222222-7474	NETWORK SN7474N	-SN7474N
0009	00002.000	EA		222222-7486	NETWORK-SN7486N	
0010	00004.000	EA		222222-7170	NETWORK SN74170N	
0011	00004.000	EA		222222-7174	NETWORK SN74174N	
0012	00001.000	EA		222222-7175	NETWORK SN74175N	
0013	00002.000	EA		222222-7180	NETWORK SN74180N	
0014	00004.000	EA		244712-8266	NETWORK-8266 2-INPUT,4-BIT DIGITAL MXPR	
0015	00003.000	EA		958474-0006	TERMINATION BOARD-C16-6	
0016	00001.000	EA		960313-0001	PLUG,WIRED,DEVICE ADDRESS SELECT-CHAN 1	
0017	REF	EA		966757-9901	DIAGRAM,LOGIC,DET-BTC #1 (WIRE WRAP)	

DRAFTSMAN DATE	CED DRAFTSMAN DATE	DESIGN ENGINEER DATE	TITLE
			INITIAL CONT,MEM RD DATA&REG FILE #1
APPD MFG DATE	APPD PROJECT ENGINEER DATE	RELEASED DATE	PROJECT NO 6961/8920

LM PART NUMBER 240656-0001 REV B

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
A	373236 (B) 2-16-72 AT LOCATION CO NETWORK SN7406N WAS A SN7405N ADDED ITEM 16 TO LM CHG QTY OF ITEM 5 WAS 4	2-16-72	
B	374189 (D) 6/22/73 ADDED ITEM 17 TO LM	6/29/73	

NOTES: UNLESS OTHERWISE SPECIFIED
1. NETWORKS ARE SN74 SERIES
2. J1 IS A TERM. BOARD LM ITEM NO. 15



QTY REQD -0002	QTY REQD -0001	ITEM NO	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED
DECIMAL XX ± .02 XXX ± .010
FRACTIONAL ± 1/64 ANGULAR ± 1
CONCENTRICITY MACHINED DIAMETERS .004 TIR
ALL DIMENSIONS TO BE MET BEFORE PLATING
REMOVE ALL BURRS AND SHARP EDGES
DO NOT SCALE THIS DRAWING
ALL DIMENSIONS IN INCHES
SURFACES MARKED ✓ TO HAVE ✓
DRILLED HOLE TOLERANCES
.013 TO .136 +.003 −.002 .136 TO .250 +.004 −.003
.250 AND ABOVE ± .005

PROCESSES
1. RUBBER STAMP F100, HEIGHT .12, COLOR BLK

PROJ NO.	SIZE	NEXT ASSY DWG NO.
8960/6980	A	217536

DRAFTSMAN 7-14-71
DESIGN ENGINEER 8/13/71
8/16/71
8/17/71

TEXAS INSTRUMENTS INCORPORATED
INDUSTRIAL PRODUCTS DIVISION
HOUSTON, TEXAS

TITLE MEM CONT, DATA CTR. ADD. REG. & MEM W DATA #2
UNIT BLOCK TRANSFER CONT
SYSTEM COMPUTER
SCALE NONE D 240658 B

32

FILMED LM

TEXAS INSTRUMENTS INCORPORATED

DATE 06/22/73 **LIST OF MATERIAL** PAGE 1 of 1

LM PART NUMBER 240658-0001 REV B

PRINT ITEM # NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		240657-0001	MEM CONT,DATA CTR,ADD REGSMEM W/DATA	
0002	00002.000	EA		222222-7400	X-NETWORK-SN7400N	
0003	00002.000	EA		222222-7402	NETWORK SN7402N	
0004	00001.000	EA		222222-7404	NETWORK SN7404N	
0005	00003.000	EA		222222-7405	NETWORK SN7405N	
0006	00002.000	EA		222222-7408	NETWORK-SN7408N	
0007	00002.000	EA		222222-7486	NETWORK-SN7486N	
0008	00004.000	EA		222222-7157	NETWORK SN74157N	
0009	00002.000	EA		222222-7174	NETWORK SN74174N	
0010	00001.000	EA		222222-7175	NETWORK SN74175N	
0011	00003.000	EA		222222-7180	NETWORK SN74180N	
0012	00008.000	EA		222222-7193	NETWORK SN74193N	-SN74193N
0013	00001.000	EA		240000-7411	NETWORK-SN74H11N	
0014	00004.000	EA		244712-8267	NETWORK,DM82678	
0015	00001.000	EA		958474-0006	TERMINATION BOARD-16-6	
0016	00001.000	EA		222222-7406	NETWORK-SN7406N	
0017	REF	EA		966758-9901	DIAGRAM,LOGIC,DET-BTC #2 (WIRE WRAP)	

DRAFTSMAN DATE 6/21/73 CKD DRAFTSMAN DATE 6/25/73 DESIGN ENGINEER DATE

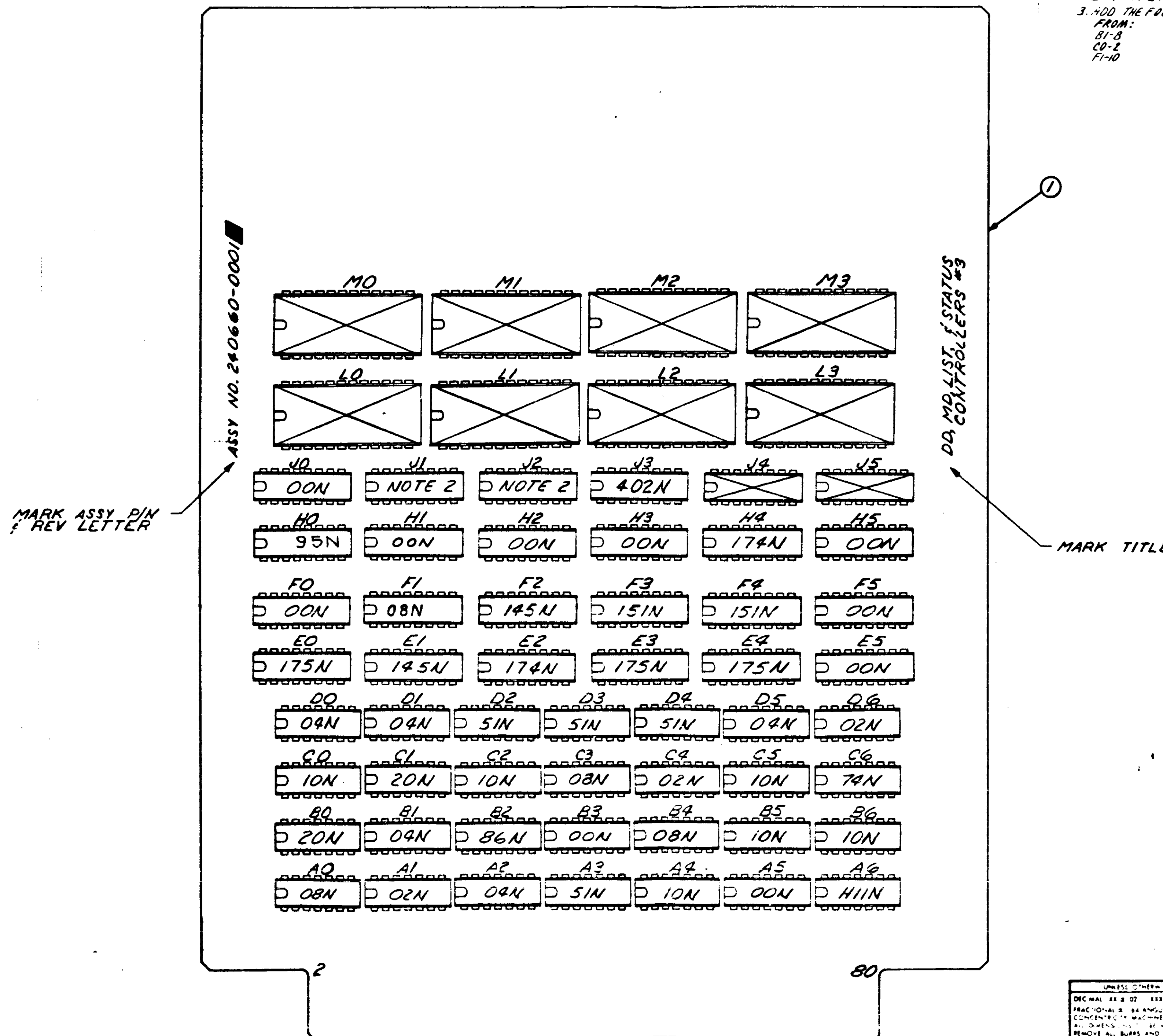
MFG DATE APPD PROJECT ENGINEER DATE RELEASED DATE

TITLE MEM CONT,DATA CTR,ADD REGSMEM W/DATA #2

PROJECT NO 8960 FILMED LM PART NUMBER 240658-0001 REV B

1849

32



NOTES:
1. NETWORKS ARE SN74 SERIES
2. J1 & J2 ARE TERM. BOARDS LM ITEM NO. 16
3. ADD THE FOLLOWING WIRES:

FROM:	TO:	SIGNAL:
B1-8	F1-11	DATEN
C0-2	F1-12	STATBUSY-
F1-10	A3-2	DATENSTAB

REVISIONS

LTR	DESCRIPTION	DATE	APPD
A	371597(D) J. Pierney 10-5-71 DELETED: 1) NETWORK H0 WAS "00N" ADDED: 1) "00N" TO NETWORK H1		
B	371236 (B) J. Pierney 12-3-71 ADDED 1) NETWORK SN7495N TO LOCATION H0 2) ITEM 17 TO LM		
C	371990 (B) J. Pierney 1-18-72 CHG: 1) LM IT. 5, QTY WAS 3. ADDED: NETWORK 08N TO POSITION F1	1-18-72	
D	376790 (C) 9-15-72 ADD: 7402N IN LOCATION J3 CHG: QTY LM IT. # 3 WAS 3		
E	374189 (D) 6/22/73 ADDED 1) ITEM 18 TO LM		
F	CN417325(C) 1) ADDED NOTE 3 & REVISION LEVEL BLOCK	9/21/76	

REVISION LEVEL	
DIAGRAM (966759-9901)	A
ASSEMBLY (240660-0001)	F

LIST OF MATERIALS

PROCESSES
1. RUBBER STAMP F100, HEIGHT .12, COLOR BLACK

NEXT ASSY DWG NO: A 217536 (8960, 8530)

TEXAS INSTRUMENTS INCORPORATED
INDUSTRIAL PRODUCTS DIVISION
HOUSTON, TEXAS

DD, MD, LIST, & STATUS CONTROLLERS #3
BLOCK TRANSFER CONT
COMPUTER

SCALE: NONE D 240660

UNLESS OTHERWISE SPECIFIED
DECIMAL .XX ± .02 .XXX ± .010
FRACTIONAL ± 1/64 ANGULAR ± 1°
REMOVE ALL BURRS AND SHARP EDGES
DO NOT SCALE THIS DRAWING
ALL DIMENSIONS IN INCHES

TEXAS INSTRUMENTS INCORPORATED

DATE 05/01/75 **LIST OF MATERIAL** PAGE 1 of

PART NUMBER LM 240660-0001 REV F0

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		240659-0001	DD,MD,LIST&STATUS CONTROLLERS SUBASSY	
0002	00010.000	EA		222222-7400	NETWORK SN7400N	-SN7400N
0003	00004.000	EA		222222-7402	NETWORK SN7402N	TI--SN7402N
0004	00005.000	EA		222222-7404	NETWORK SN7404N	
0005	00004.000	EA		222222-7408	NETWORK-SN7408N	
0006	00006.000	EA		222222-7410	NETWORK SN7410N	-SN7410N
0007	00002.000	EA		222222-7420	NETWORK SN7420N	-SN7420N
0008	00004.000	EA		222222-7451	NETWORK SN7451N	-SN7451N
0009	00001.000	EA		222222-7474	NETWORK SN7474N	-SN7474N
0010	00001.000	EA		222222-7486	NETWORK-SN7486N	
0011	00002.000	EA		222222-7145	NETWORK SN74145N	
0012	00002.000	EA		222222-7151	NETWORK SN74151N	
0013	00002.000	EA		222222-7174	NETWORK SN74174N	
0014	00003.000	EA		222222-7175	NETWORK SN74175N	
0015	00001.000	EA		240000-7411	NETWORK-SN74H11N	
0016	00002.000	EA		958474-0006	TERMINATION BOARD-C16-6	
0017	00001.000	EA		222222-7495	NETWORK SN7495N	-SN7495N
0018	REF	EA		966759-9901	DIAGRAM,LOGIC,DET-BTC #3 (WIRE WRAP)	

DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						DD,MD,LIST & STATUS CONTROLLERS #3
APPD MFG	DATE	APPD PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO / PART NUMBER / REV
						696-18920 / LM 240660-0001 / F0

SECTION VII

DIAGRAMS

7.1 GENERAL

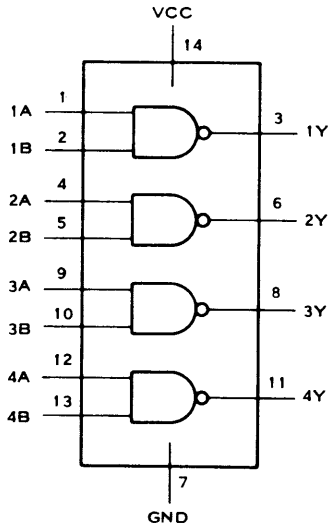
This section contains the logic diagrams for the block transfer controller circuit boards. The logic is implemented on both multilayer and wire wrap circuit boards. The two types are directly interchangeable. Use the appropriate set of logic diagrams when troubleshooting, as device locations and pin numbers differ considerably between the two types.

7.2 INTEGRATED CIRCUIT DATA

Figure 7-1 contains diagrams for the integrated circuits used on the block transfer controller circuit boards. These diagrams can be used with the logic diagrams to better understand the circuitry.

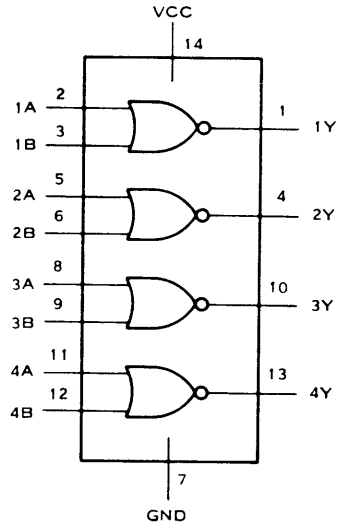
7.3 LIST OF DRAWINGS

The block transfer controller circuit board drawings follow the integrated circuit diagrams and are:



SN7400

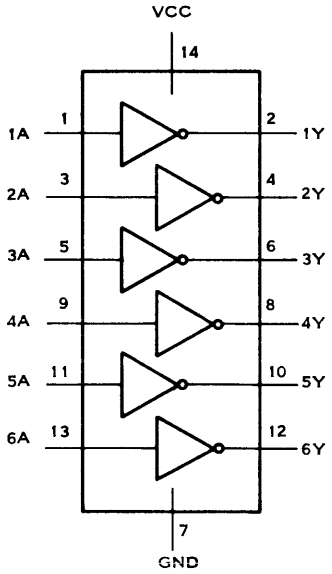
QUADRUPLE
2 – INPUT POSITIVE
NAND GATES



SN7402

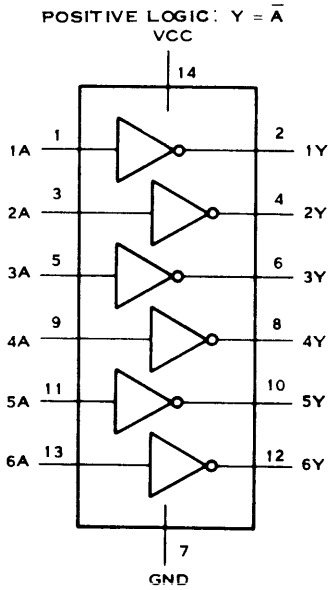
QUADRUPLE
2 – INPUT POSITIVE
NOR GATES

POSITIVE LOGIC: $Y = \overline{A}$



SN7404

POSITIVE LOGIC: $Y = \overline{A}$



SN7405
HEX INVERTERS
(WITH OPEN–
COLLECTOR OUTPUT)

(B)131565

Figure 7-1. Integrated Circuit Diagrams (Sheet 1 of 8)

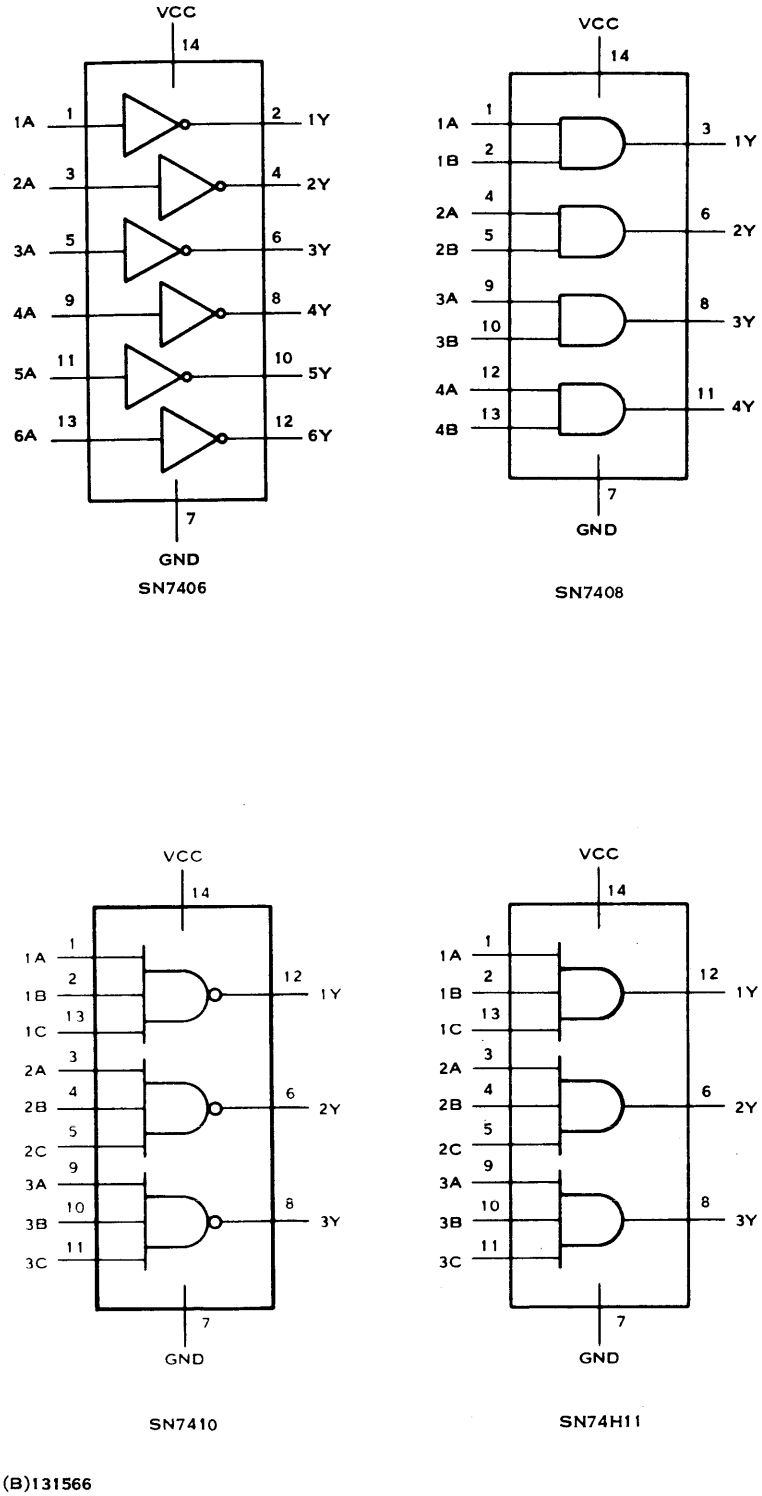
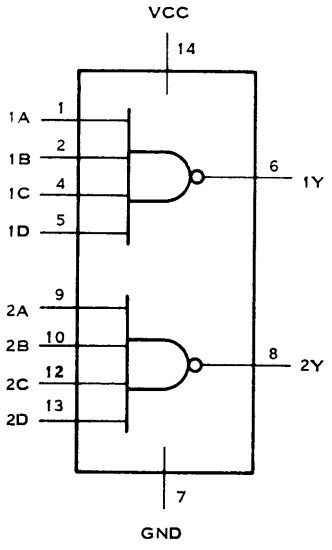
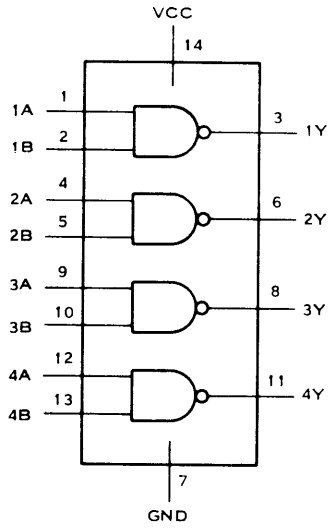


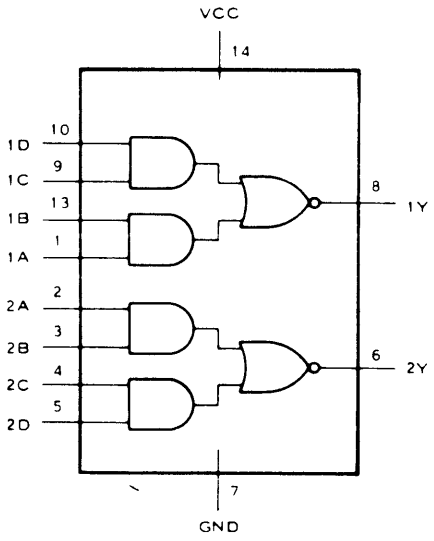
Figure 7-1. Integrated Circuit Diagrams (Sheet 2 of 8)



SN7420
DUAL 4-INPUT
POSITIVE NAND
GATES

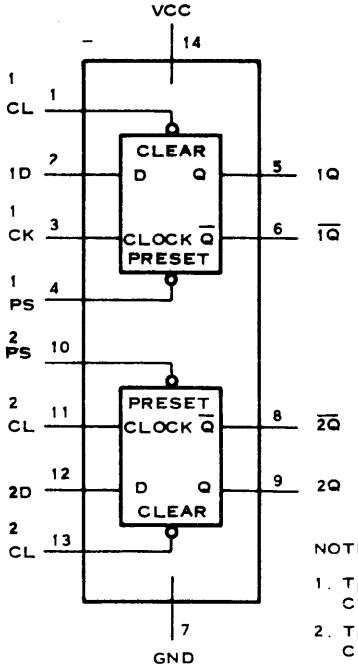


SN7437
QUAD2 - INPUT
POSITIVE NAND
GATES AND BUFFERS



SN7451
DUAL
2 - WIDE, 2 - INPUT
AND - OR - INVERT GATES

POSITIVE LOGIC:
LOW INPUT TO PRESET SETS Q TO LOGICAL 1
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
PRESET AND CLEAR ARE INDEPENDENT OF CLOCK



TRUTH TABLE		
T_N	T_N+1	
INPUT	OUTPUTS	
D	Q	$\overline{Q}$
0	0	1
1	1	0

NOTE :

1. T_N = BIT TIME BEFORE CLOCK PULSE.
2. T_N+1 = BIT TIME AFTER CLOCK PULSE.
3. PRESET AND CLEAR INPUTS INDEPENDENT OF CLOCK
4. INPUT DATA TRANSFERRED TO Q OUTPUT ON POSITIVE EDGE OF CLOCK PULSE.

SN7474
DUAL D-TYPE
EDGE TRIGGERED
FLIP-FLOPS

(B)131567

Figure 7-1. Integrated Circuit Diagrams (Sheet 3 of 8)

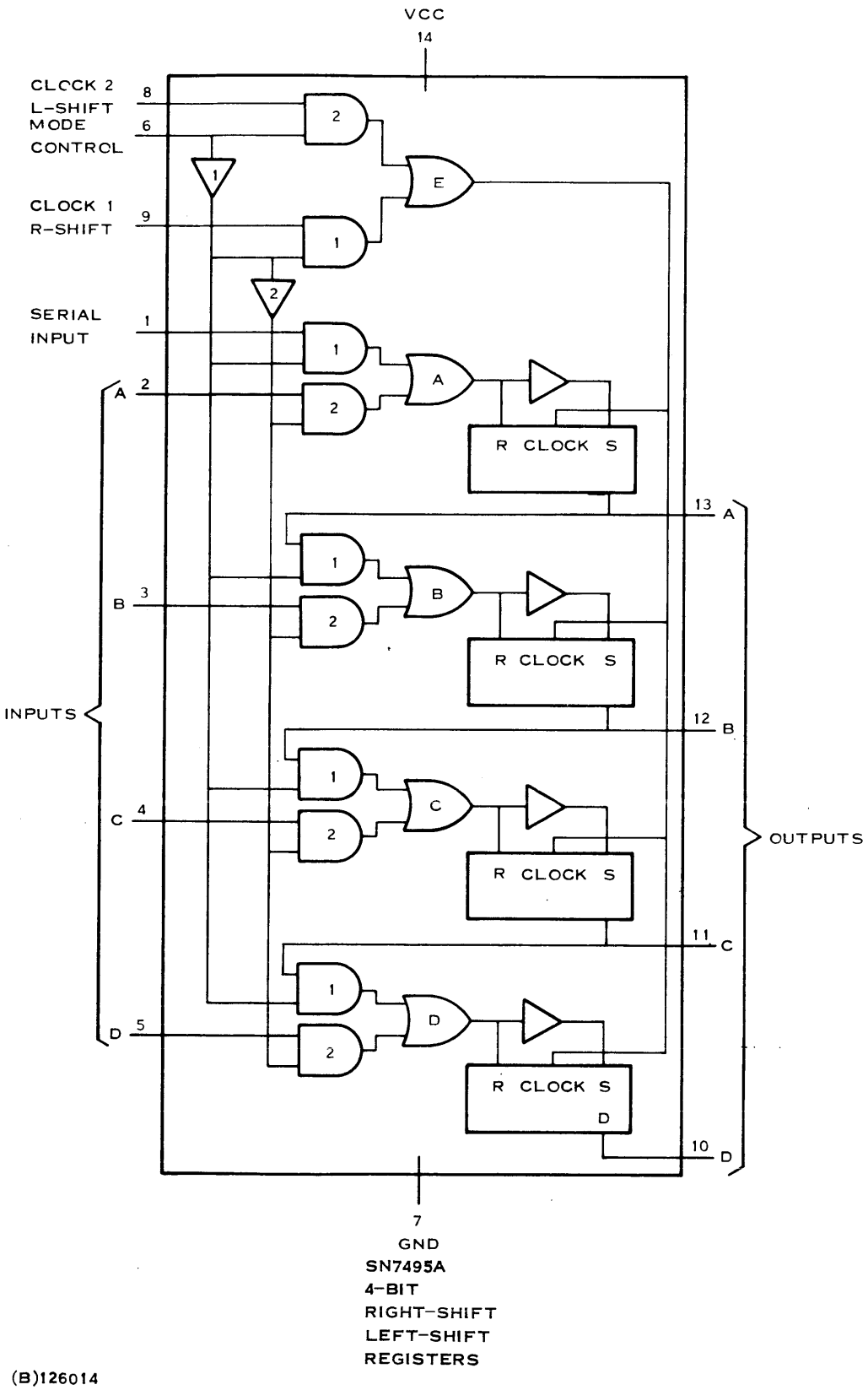
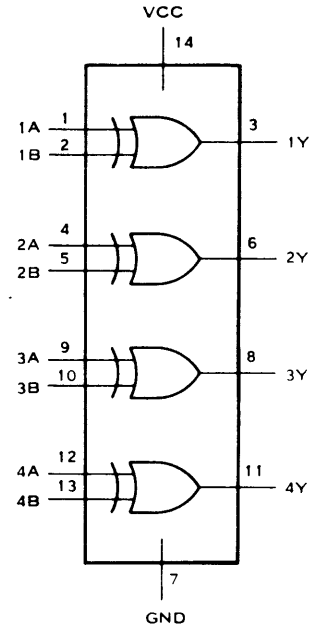
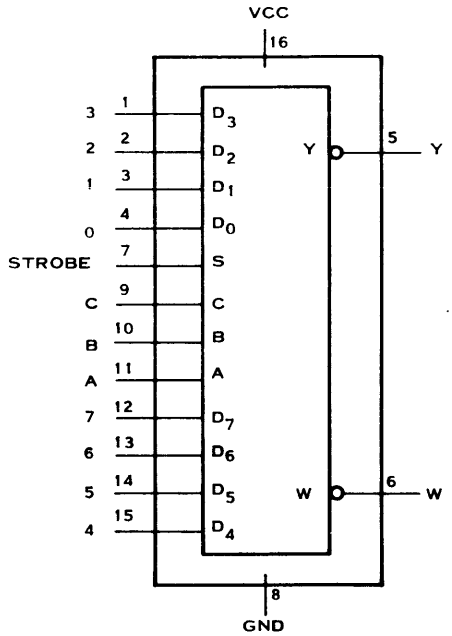


Figure 7-1. Integrated Circuit Diagrams (Sheet 4 of 8)

POSITIVE LOGIC $Y = A \oplus B$

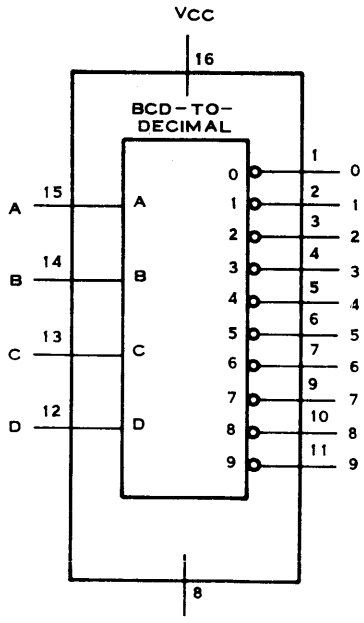


SN7486
QUAD 2-INPUT
EXCLUSIVE-OR
GATES



SN74151/SN54151
DATA SELECTORS
MULTIPLEXERS

POSITIVE LOGIC: SEE TRUTH TABLE



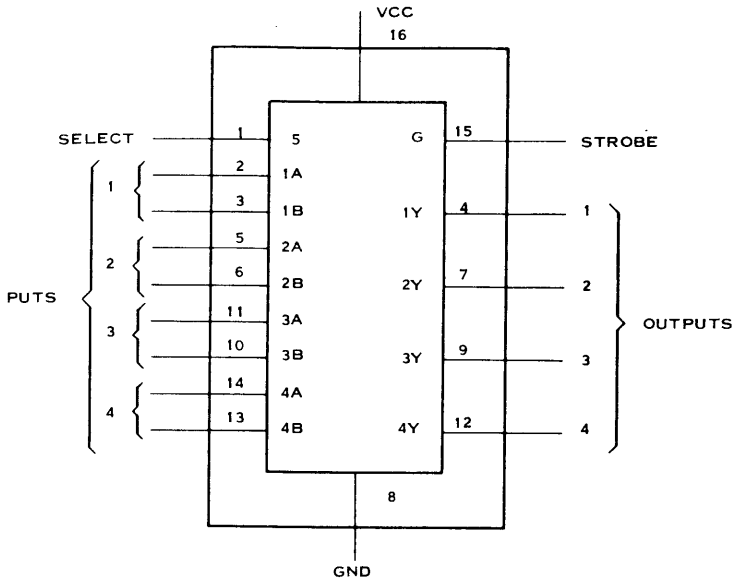
SN74145
BCD-TO-DECIMAL
DECODER/DRIVERS

TRUTH TABLE

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

(B)131568

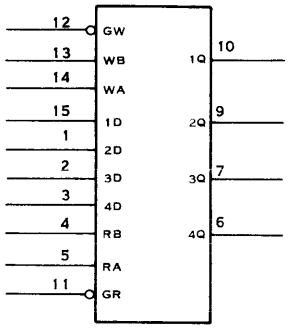
Figure 7-1. Integrated Circuit Diagrams (Sheet 5 of 8)



SN74157

FUNCTION TABLE				
INPUTS				OUTPUTS
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

SN74157, SN74S157, SN74L157
QUADRUPLE
2-LINE-TO-1LINE
DATA SELECTORS/MULTIPLEXERS



SN74170

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q=D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q=D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q=D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q=D
X	X	H	Q_0	Q_0	Q_0	Q_0

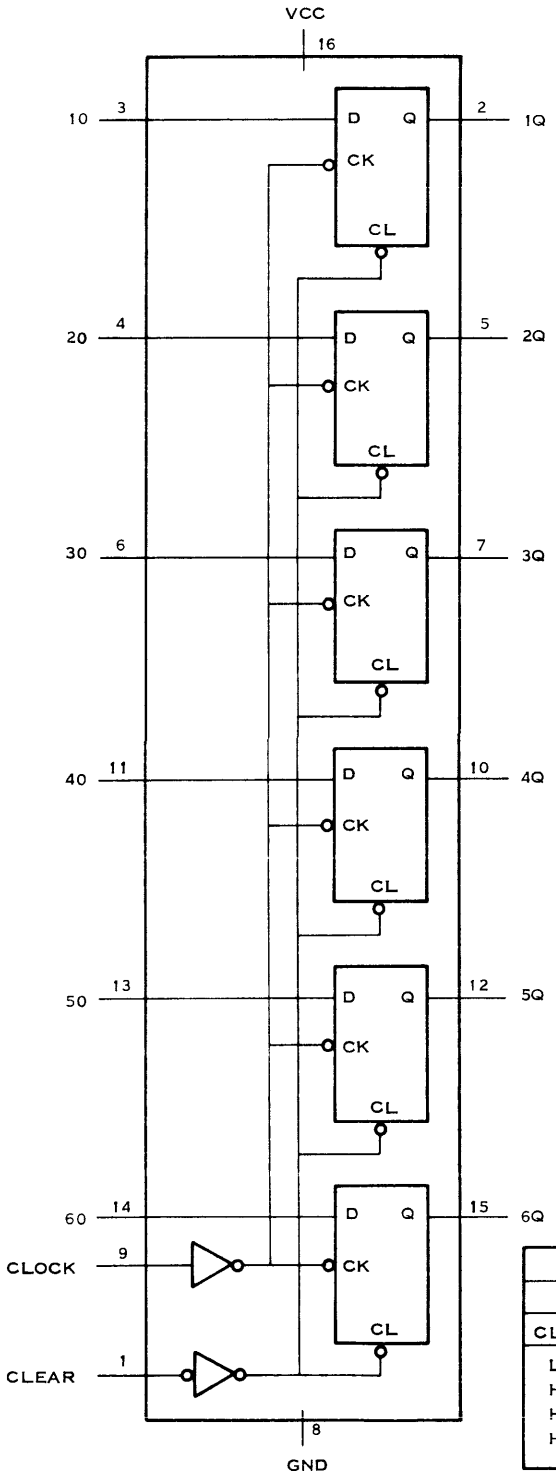
READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: A. H=HIGH LEVEL, L=LOW LEVEL, X=IRRELEVANT
B. (Q=D)=THE FOUR SELECTED INTERNAL FLIP-FLOP OUTPUTS WILL ASSUME THE STATES APPLIED TO THE FOUR EXTERNAL DATA INPUTS.
C. Q_0=THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.
D. W0B1=THE FIRST BIT OF WORD 0, ETC.

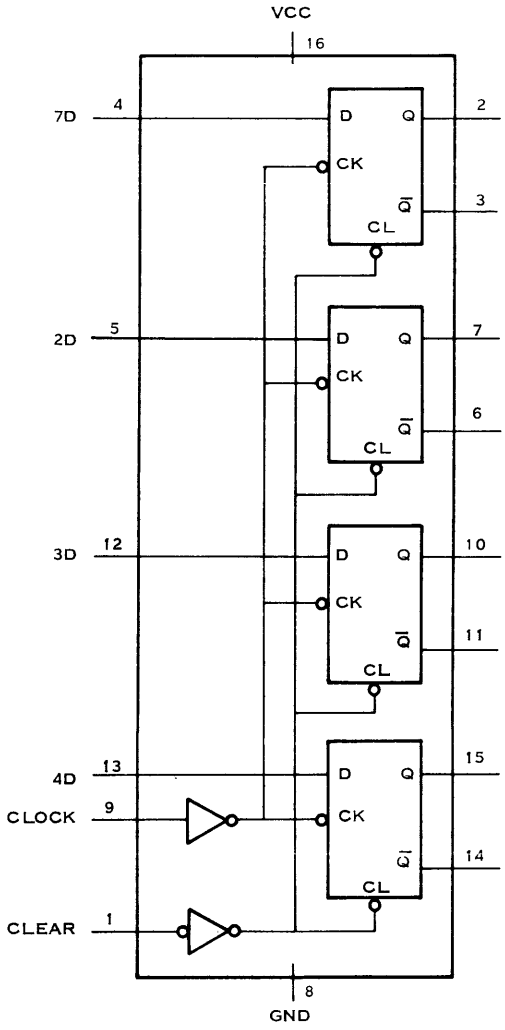
(B)131569

Figure 7-1. Integrated Circuit Diagrams (Sheet 6 of 8)



SN74174
HEX/QUADRUPLE
D-TYPE FLIP-FLOP WITH CLEAR

(B)131571



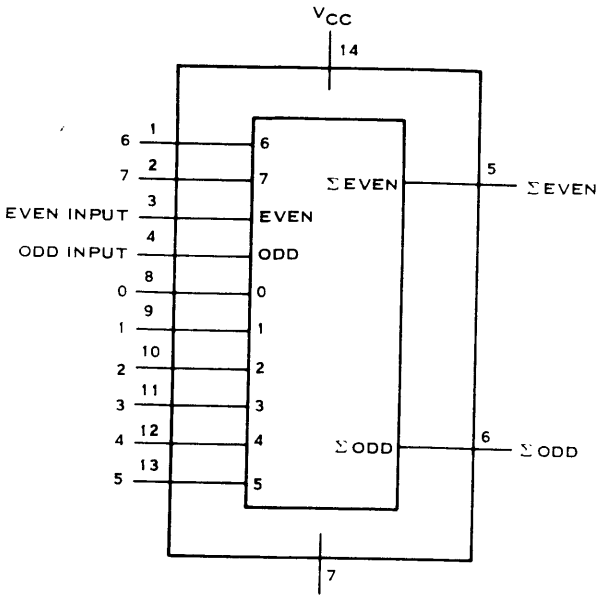
SN74175
HEX/QUADRUPLE
D-TYPE FLIP-FLOP WITH CLEAR

TRUTH TABLE				
INPUTS			OUTPUT	
CLR	CK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

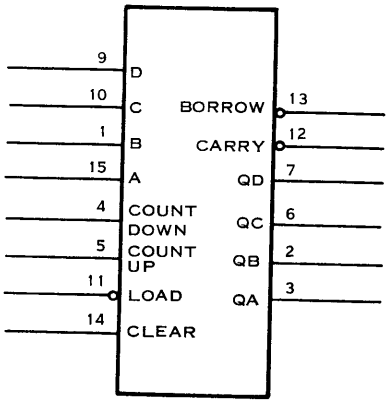
TRUTH TABLE				
INPUTS			OUTPUT	
CLR	CK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H=HIGH LEVEL (STEADY STATE)
L=LOW LEVEL (STEADY STATE)
X=IRRELEVANT
↑=TRANSITION FROM LOW TO HIGH LEVEL
Q_D=THE LEVEL OF Q BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED

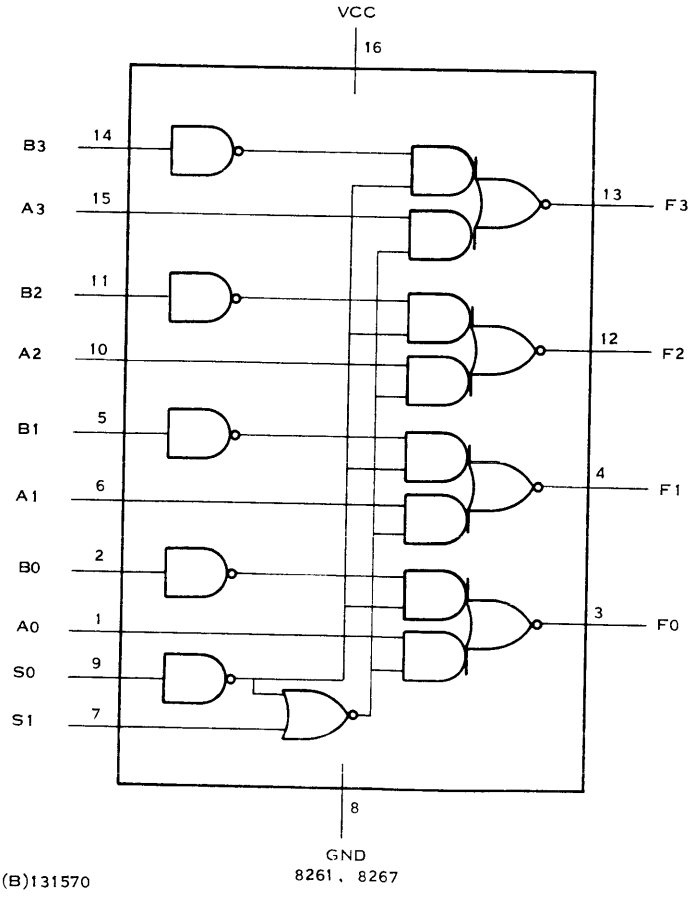
Figure 7-1. Integrated Circuit Diagrams (Sheet 7 of 8)



SN74180
8-BIT ODD/EVEN PARITY
GENERATORS/CHECKERS



SN74193

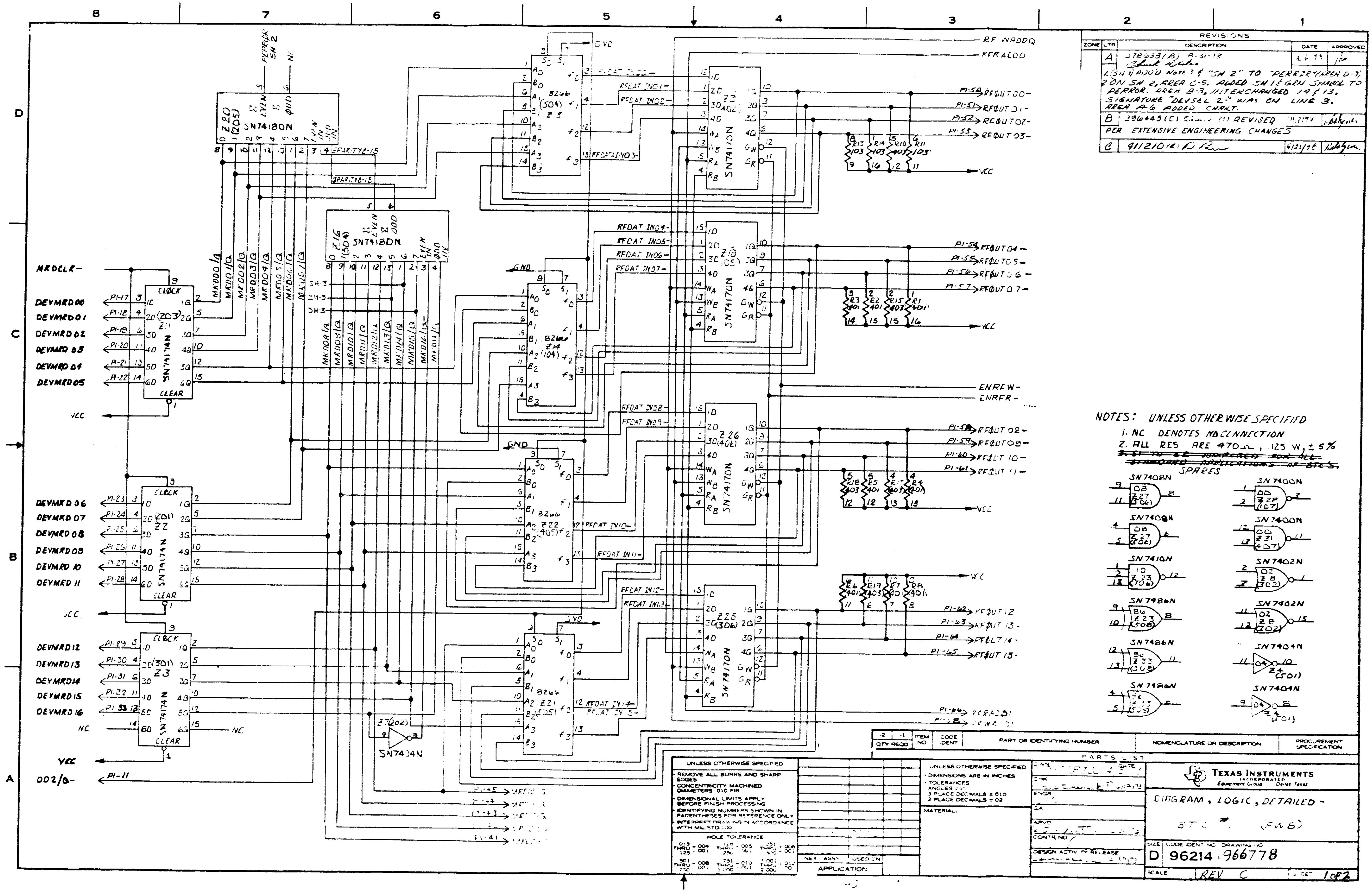


8261, 8267

TRUTH TABLE

SELECT LINES		OUTPUT
S_0	S_1	fn(0,1,2,3)
0	0	B_n
0	1	B_n
1	0	A_n
1	1	1

Figure 7-1. Integrated Circuit Diagrams (Sheet 8 of 8)



REVISIONS
NOTES: UNLESS OTHERWISE SPECIFIED
1. NC DENOTES NO CONNECTION
2. ALL RES ARE 470 Ω, .125 W, ± 5%
SPARES
SN7408N
SN7400N
SN7410N
SN7402N
SN7486N
SN7404N
SN74180N
SN74174N
SN7417ON
SN7404N
MRDCLK-
DEVMRD00
DEVMRD01
DEVMRD02
DEVMRD03
DEVMRD04
DEVMRD05
DEVMRD06
DEVMRD07
DEVMRD08
DEVMRD09
DEVMRD10
DEVMRD11
DEVMRD12
DEVMRD13
DEVMRD14
DEVMRD15
DEVMRD16
CLOCK
CLEAR
VCC
NC
GND
RF WADDQ
RFRADDQ
ENREW-
ENRFR-
TEXAS INSTRUMENTS
DIAGRAM, LOGIC, DETAILED
PARTS LIST
D 96214 966778
REV C
1 OF 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

ADRESS SELECT SWITCH (LOCATION 595)			
CHANNEL	SI-1	SI-2	SI-3
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

UNLESS OTHERWISE SPECIFIED
• REMOVE ALL BURRS AND SHARP EDGES
• CONCENTRICITY MACHINED DIAMETERS .010 FIR
• DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
• IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
• INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100

HOLE TOLERANCE			
.013 THRU .064	± .001	.125 THRU .500	± .003
.501 THRU .750	± .002	1.001 THRU 2.000	± .005

UNLESS OTHERWISE SPECIFIED
• DIMENSIONS ARE IN INCHES
• TOLERANCES ANGLES ±1° 3 PLACE DECIMALS ± .010 2 PLACE DECIMALS ± .02
MATERIAL

NEXT ASSY	USED ON
APPLICATION	

QTY REQD	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION

PARTS LIST

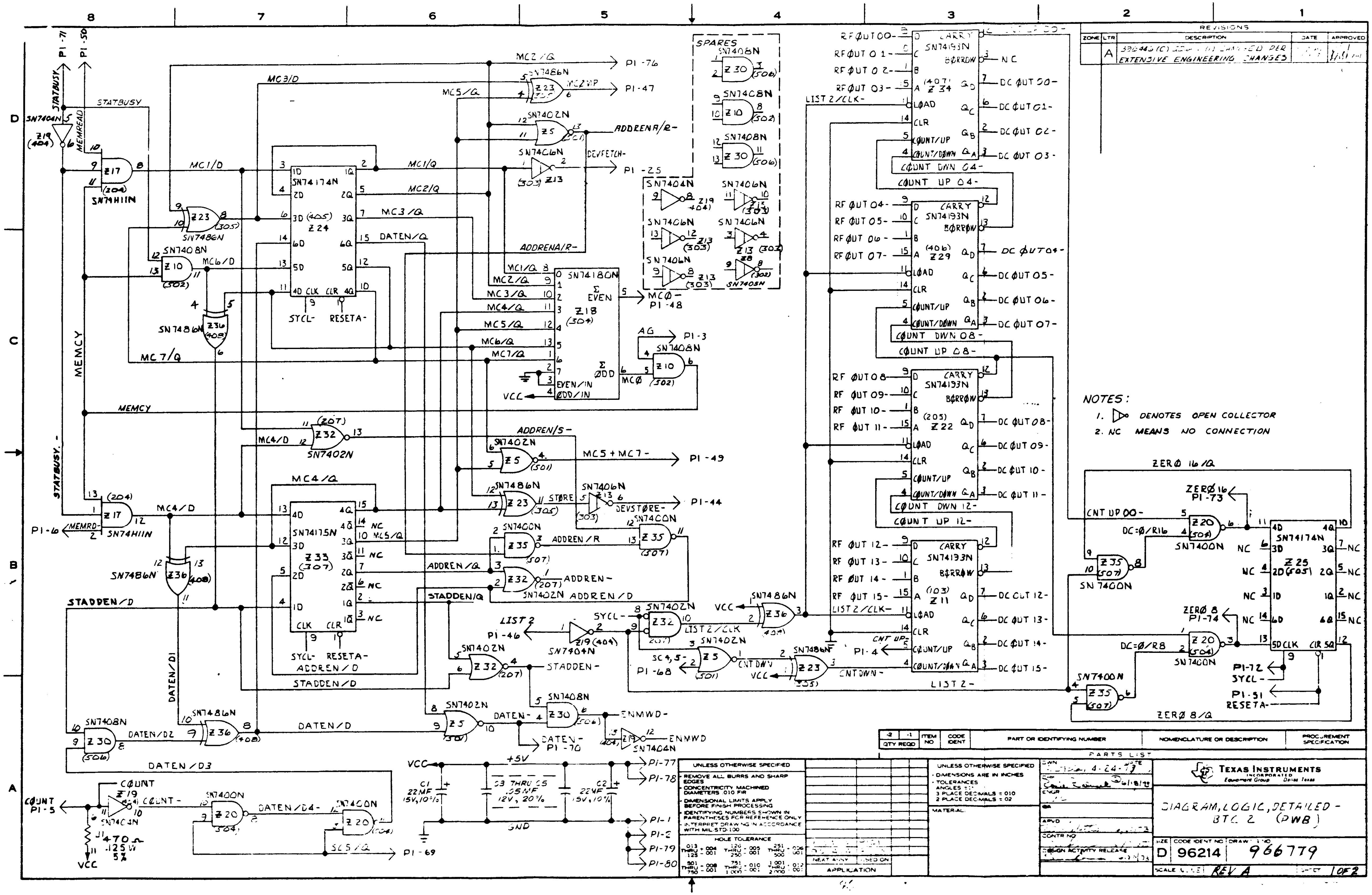
DWN	DATE
CHK	
ENGR	
QA	
APVD	
CONTR NO	
DESIGN ACTIVITY RELEASE	

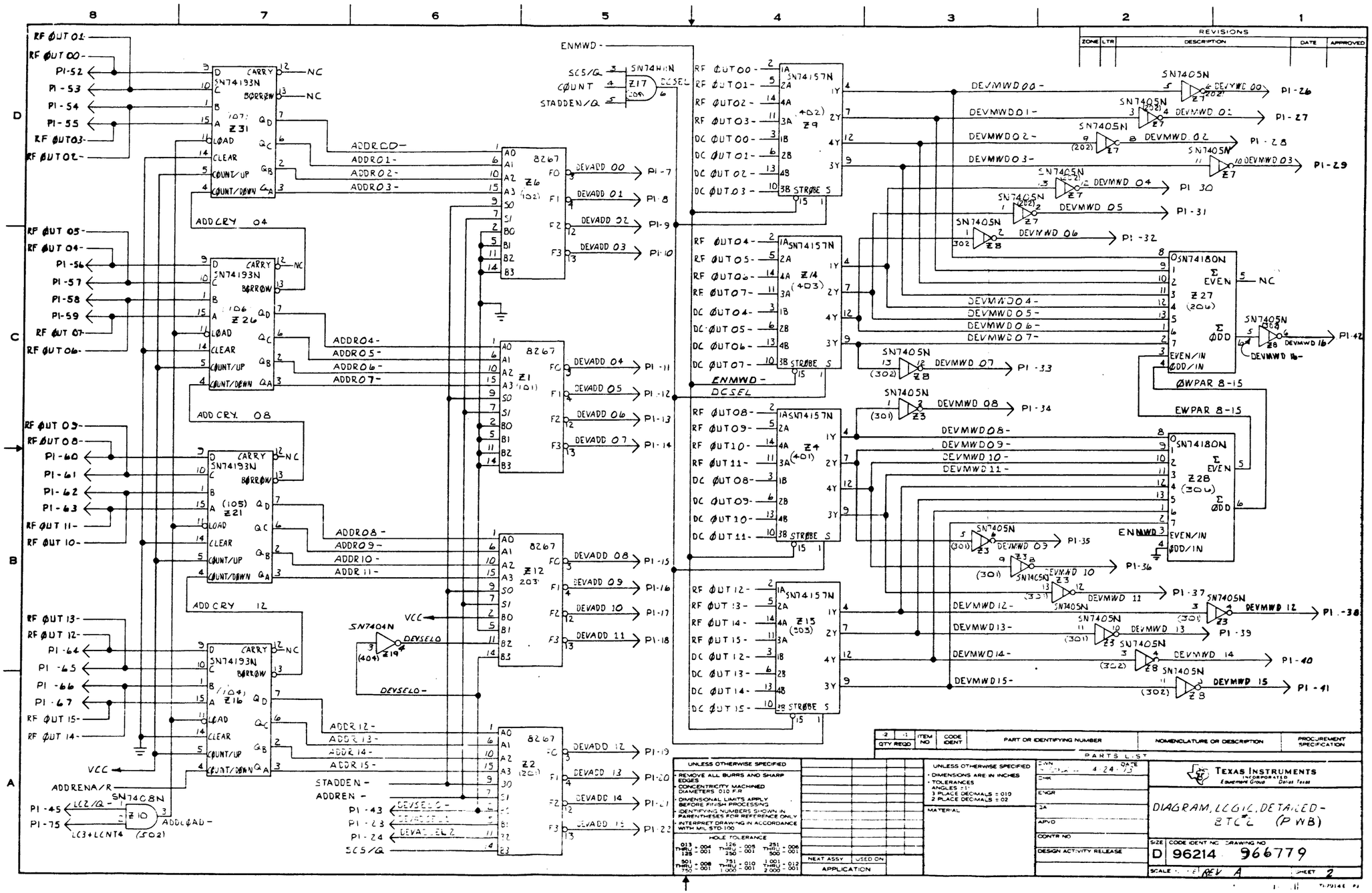
TEXAS INSTRUMENTS
INCORPORATED
Equipment Group Dallas, Texas

DIAGRAM, LOGIC, DETAILED
BTC I (PWB)

SIZE	CODE IDENT NO	DRAWING NO
D	96214	966778

SCALE — REV C — SHEET 2


NOTES:
1. DENOTES OPEN COLLECTOR
2. NC MEANS NO CONNECTION
REVISIONS
A EXTENSIVE ENGINEERING CHANGES
SPARES
PARTS LIST
UNLESS OTHERWISE SPECIFIED
TEXAS INSTRUMENTS
DIAGRAM, LOGIC, DETAILED - BTC 2 (PWB)
D 96214 966779
REV A
1 OF 2
SN74174N
SN74175N
SN74180N
SN74193N
SN7486N
SN7408N
SN7402N
SN7400N
SN7404N
SN7406N
SN74H11N
MEMCY
STATBUSY
MEMREAD
ADDRENA/R-
DEVFETCH-
DEVSTORE-
MC5 + MC7-
STADDEN/D
DATEN/D
ENMWD-
COUNT
LIST 2/CLK-
CNT UP 00-
ZERO 16/Q
ZERO 8/Q
RESETA-
SYCL-
+5V
GND
VCC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RF OUT 01-
RF OUT 00-
P1-52
P1-53
P1-54
P1-55
RF OUT 03-
RF OUT 02-
SN74193N
Z31
(107)
ADDR 00-
ADDR 01-
ADDR 02-
ADDR 03-
ADD CRY 04
RF OUT 05-
RF OUT 04-
P1-56
P1-57
P1-58
P1-59
RF OUT 07-
RF OUT 06-
Z26
(106)
ADDR 04-
ADDR 05-
ADDR 06-
ADDR 07-
ADD CRY 08
RF OUT 09-
RF OUT 08-
P1-60
P1-61
P1-62
P1-63
RF OUT 11-
RF OUT 10-
Z21
(105)
ADDR 08-
ADDR 09-
ADDR 10-
ADDR 11-
ADD CRY 12
RF OUT 13-
RF OUT 12-
P1-64
P1-65
P1-66
P1-67
RF OUT 15-
RF OUT 14-
Z16
(104)
ADDR 12-
ADDR 13-
ADDR 14-
ADDR 15-
VCC
ADDRENA/R
SN74C8N
Z10
(502)
P1-45
P1-75
LC2/Q-
ADDLOAD-
LC3+LCNT4
8267
Z6
(102)
Z1
(101)
Z12
(203)
Z2
(201)
DEVADD 00
DEVADD 01
DEVADD 02
DEVADD 03
DEVADD 04
DEVADD 05
DEVADD 06
DEVADD 07
DEVADD 08
DEVADD 09
DEVADD 10
DEVADD 11
DEVADD 12
DEVADD 13
DEVADD 14
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P1-11
P1-12
P1-13
P1-14
P1-15
P1-16
P1-17
P1-18
P1-19
P1-20
P1-21
P1-22
SN74H11N
Z17
(204)
ENMWD-
SCS/Q
COUNT
STADDEN/Q
DCSEL
SN7404N
Z19
(404)
DEVSELO
DEVSELO-
STADDEN-
ADDREN-
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P1-23
P1-24
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SN74157N
Z9
(402)
Z14
(403)
Z4
(401)
Z15
(303)
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RF OUT01-
RF OUT02-
RF OUT03-
DC OUT00-
DC OUT01-
DC OUT02-
DC OUT03-
RF OUT04-
RF OUT05-
RF OUT06-
RF OUT07-
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DC OUT05-
DC OUT06-
DC OUT07-
RF OUT08-
RF OUT09-
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DC OUT10-
DC OUT11-
RF OUT12-
RF OUT13-
RF OUT14-
RF OUT15-
DC OUT12-
DC OUT13-
DC OUT14-
DC OUT15-
STROBE
SN7405N
Z7
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Z8
(302)
Z3
(301)
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DEVMWD03-
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DEVMWD08-
DEVMWD09-
DEVMWD10-
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DEVMWD12-
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P1-39
P1-40
P1-41
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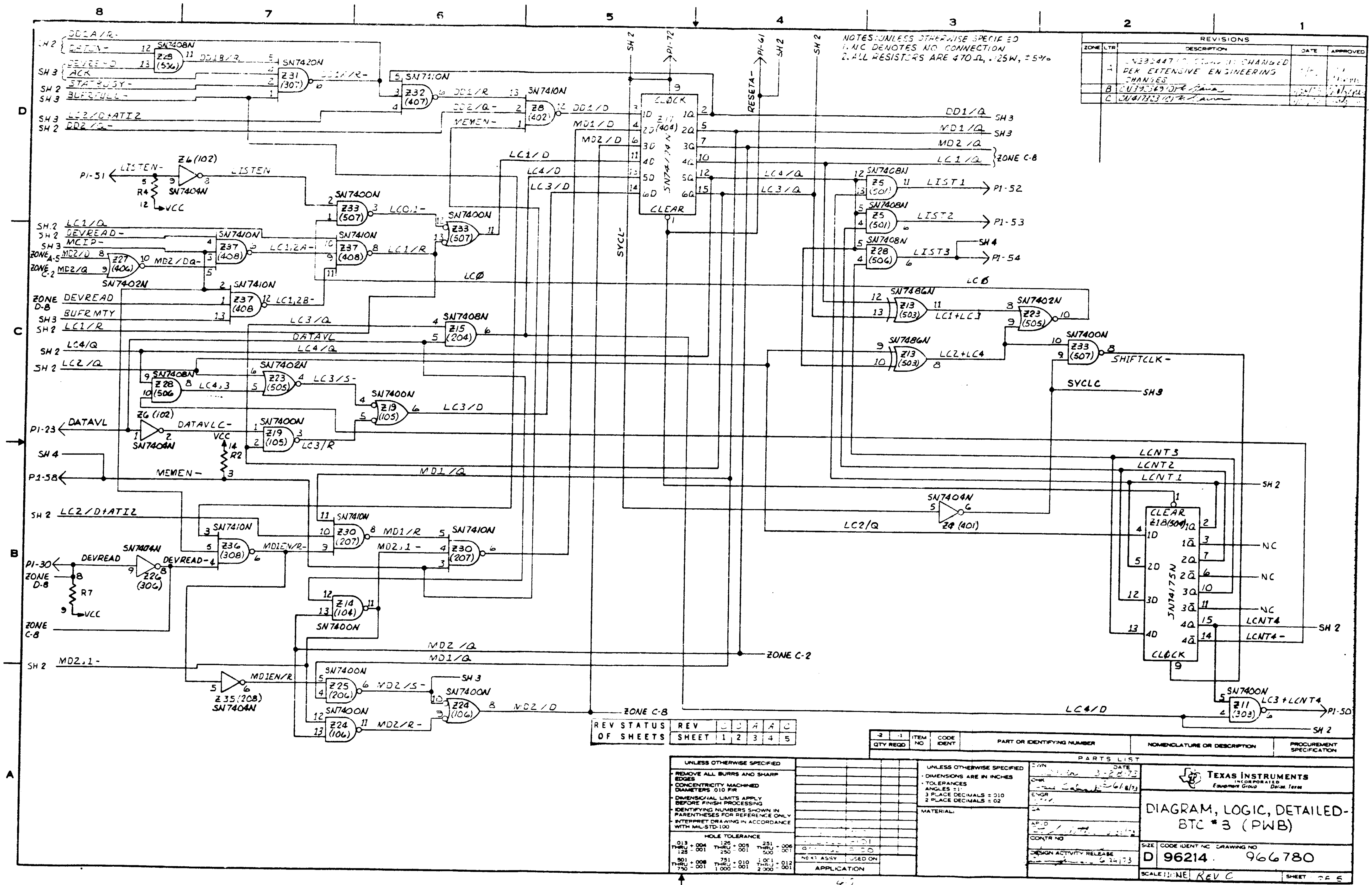
Z27
(204)
Z28
(304)
EVEN
ODD
EVEN/IN
ODD/IN
NC
DEVMWD 16
DEVMWD 16-
P1-42
ENMWD
ØWPAR 8-15
EWPAR 8-15
DCSEL
UNLESS OTHERWISE SPECIFIED
REMOVE ALL BURRS AND SHARP EDGES
CONCENTRICITY MACHINED DIAMETERS .010 F.I.R.
DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
INTERPRET DRAWING IN ACCORDANCE WITH MIL STD 100
HOLE TOLERANCE
NEXT ASSY
USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±1°
3 PLACE DECIMALS = 010
2 PLACE DECIMALS = 02
MATERIAL
DESIGN ACTIVITY RELEASE
QTY REQD
ITEM NO
CODE IDENT
PART OR IDENTIFYING NUMBER
NOMENCLATURE OR DESCRIPTION
PROCUREMENT SPECIFICATION
PARTS LIST
DWN
CHK
ENGR
PJA
APVD
CONTR NO
DATE 4-24-73
TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas Texas
DIAGRAM, LCOIL, DETAILED - 8TCC (PWB)
SIZE D
CODE IDENT NO 96214
DRAWING NO 966779
SCALE
REV A
SHEET 2


NOTES: UNLESS OTHERWISE SPECIFIED
1. NC DENOTES NO CONNECTION
2. ALL RESISTORS ARE 470 Ω, .125W, ±5%
REVISIONS
REV STATUS OF SHEETS
PARTS LIST
TEXAS INSTRUMENTS
DIAGRAM, LOGIC, DETAILED-
BTC #3 (PWB)
D 96214 966780
Rev C
SN7400N
SN7404N
SN7408N
SN7410N
SN7420N
SN7402N
SN7486N
SN74174N
SN74175N
LISTEN
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MEMEN
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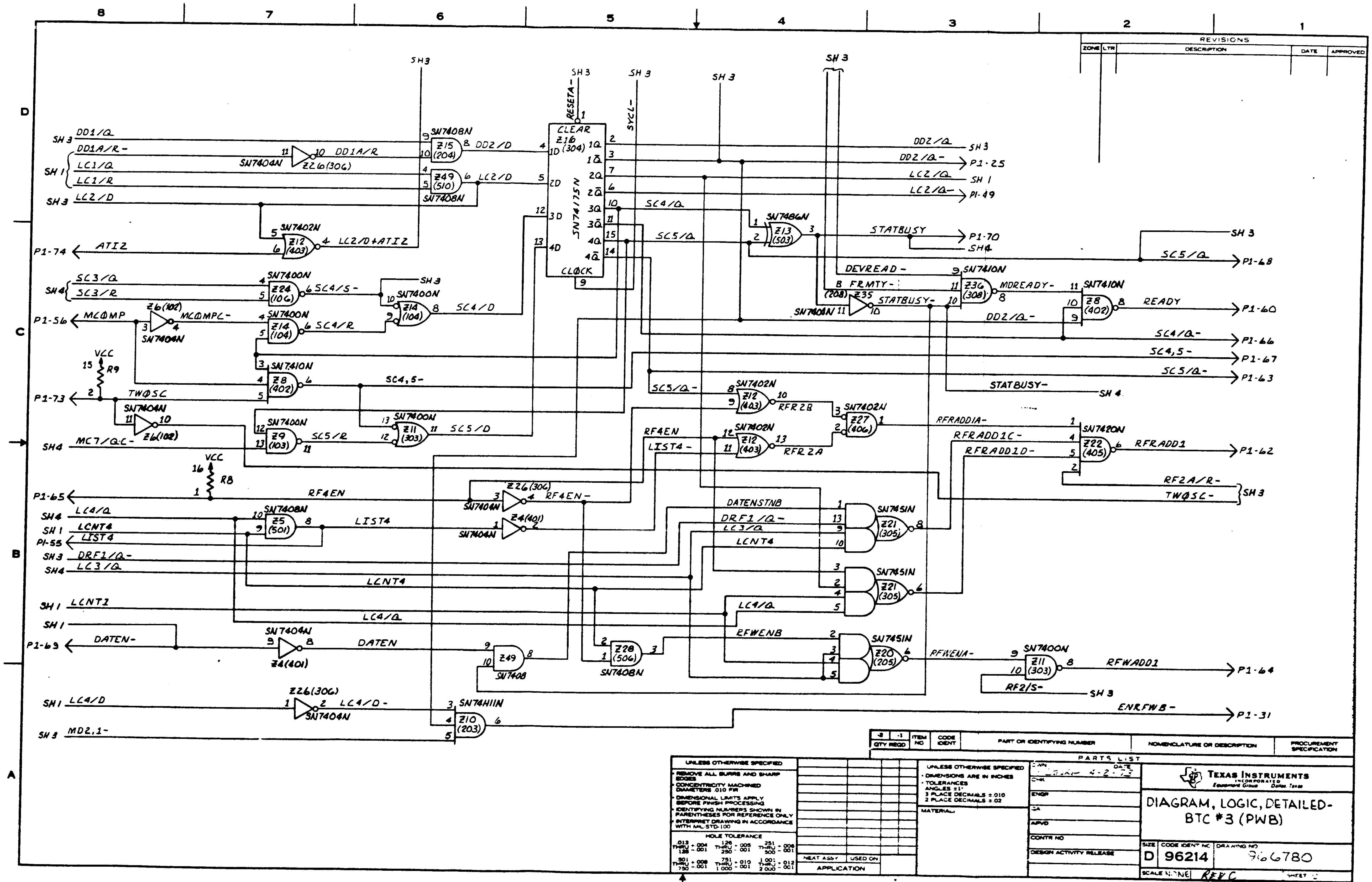
SYCLC
LCNT1
LCNT2
LCNT3
LCNT4
ZONE C-2
ZONE C-8
CLEAR
CLOCK



REVISIONS
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LTR
DESCRIPTION
DATE
APPROVED
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SH 4
DD1/Q
DD1A/R-
DD1A/R
LC1/Q
LC1/R
LC2/D
DD2/D
SN7408N
SN7404N
SN7402N
SN7400N
SN7410N
SN7486N
SN7420N
SN74S1N
SN74H11N
SN74175N
CLEAR
CLOCK
RESETA-
SYCL-
DD2/Q
DD2/Q-
LC2/Q
LC2/Q-
SC4/Q
SC5/Q
STATBUSY
DEVREAD-
FRMTY-
MDREADY-
READY
SC4/Q-
SC4,5-
SC5/Q-
P1-25
P1-49
P1-70
P1-68
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P1-31
P1-74
P1-56
P1-73
P1-65
P1-55
P1-69
ATI2
LC2/D+ATI2
SC3/Q
SC3/R
SC4/S-
SC4/D
SC4/R
MCOMP
MCOMPC-
VCC
R9
R8
TWOSC
MC7/QC-
SC5/R
SC5/D
RF4EN
RF4EN-
RFR2B
RFR2A
LIST4-
RFRADD1A-
RFRADD1C-
RFRADD1D-
RFRADD1
RF2A/R-
TWOSC-
DATENSTNB
DRF1/Q-
LC3/Q
LCNT4
LC4/Q
LIST4
LCNT1
DATEN-
DATEN
RFWENB
RFWENA-
RFWADD1
RF2/S-
ENRFWB-
LC4/D
LC4/D-
MD2,1-
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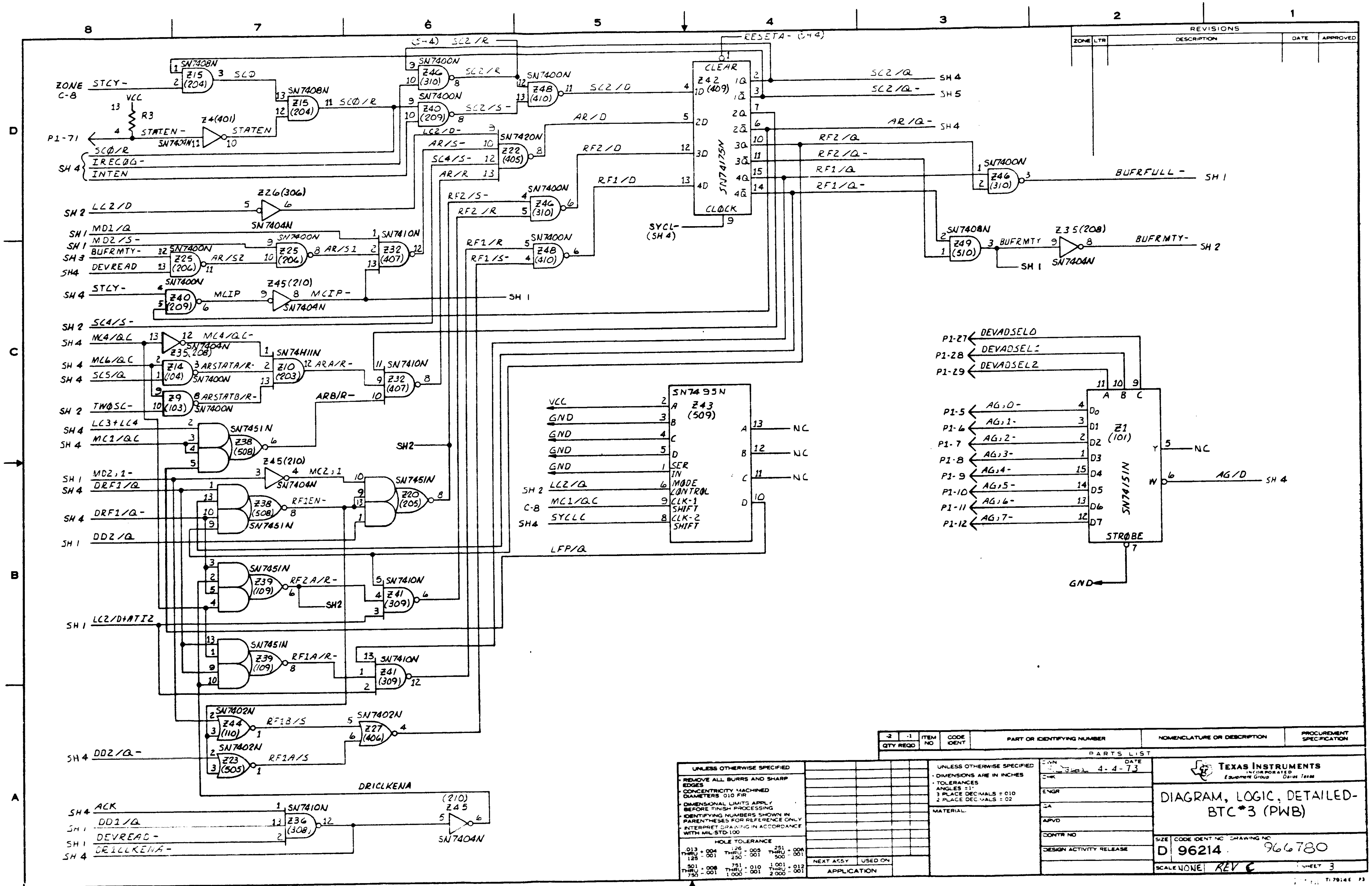
QTY REQD
ITEM NO
CODE IDENT
PART OR IDENTIFYING NUMBER
NOMENCLATURE OR DESCRIPTION
PROCUREMENT SPECIFICATION
UNLESS OTHERWISE SPECIFIED
REMOVE ALL BURRS AND SHARP EDGES
CONCENTRICITY MACHINED DIAMETERS .010 FIR
DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100
HOLE TOLERANCE
DIMENSIONS ARE IN INCHES
TOLERANCES
MATERIAL
NEXT ASSY
USED ON
APPLICATION
TEXAS INSTRUMENTS
INCORPORATED
Equipment Group Dallas, Texas
DIAGRAM, LOGIC, DETAILED-
BTC #3 (PWB)
SIZE
CODE IDENT NO
DRAWING NO
D
96214
966780
SCALE NONE
REV C
SHEET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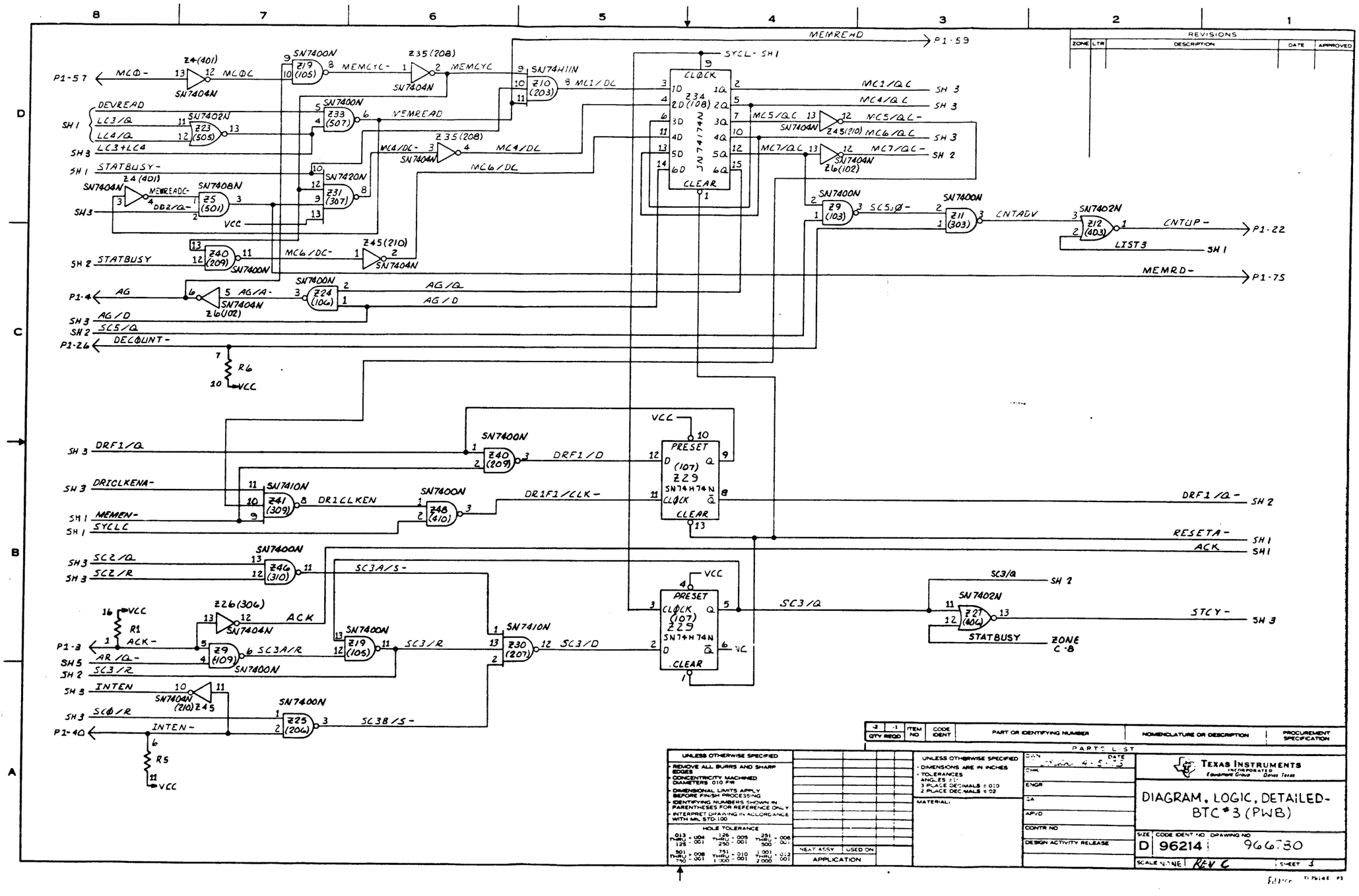
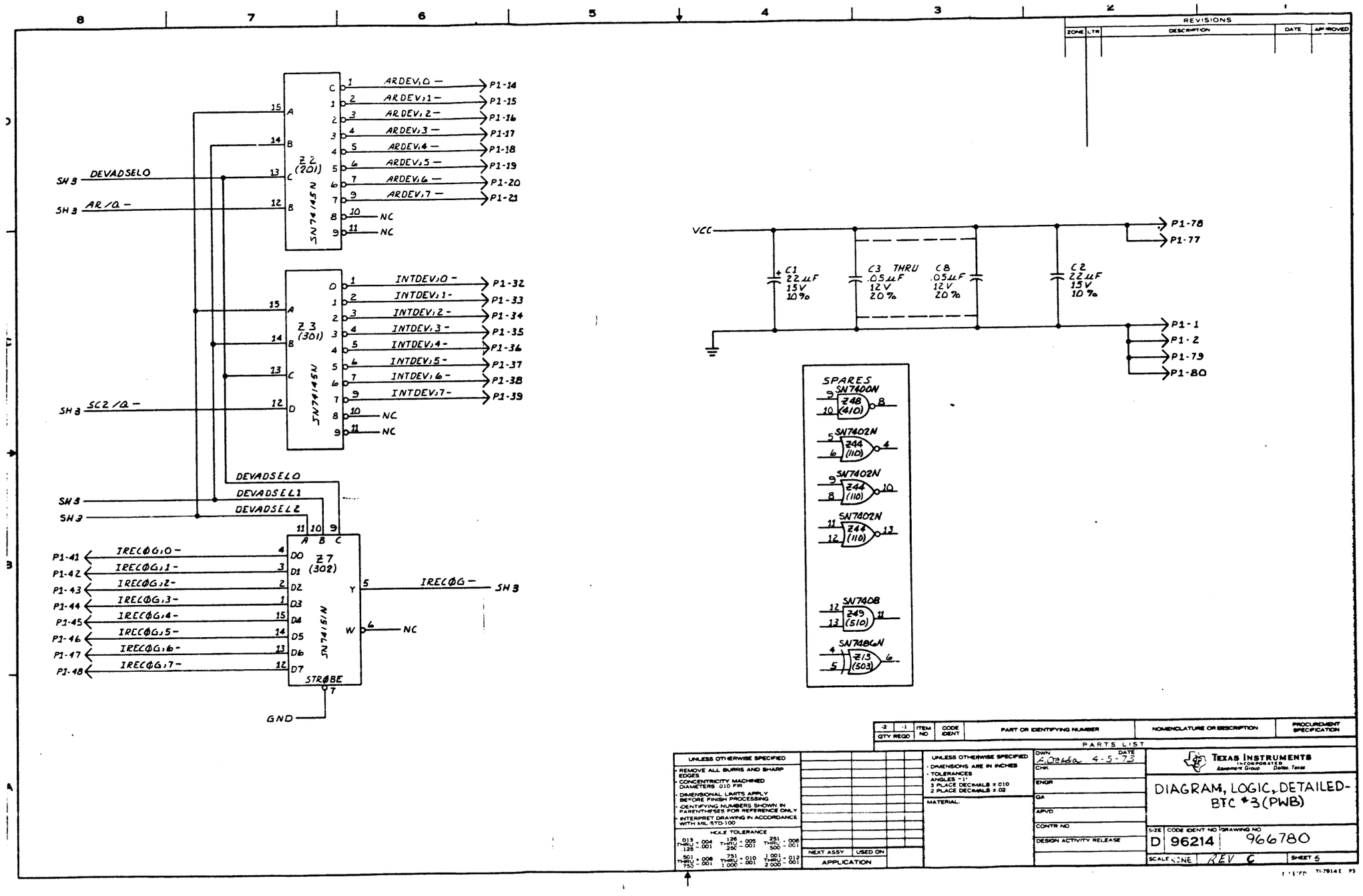
BTC*3 (PWB)
D 96214 966780
SCALE NONE REV C
SHEET 3
4-4-73
UNLESS OTHERWISE SPECIFIED
APPLICATION
SN74175N
SN7495N
SN74151N
SN7400N
SN7404N
SN7408N
SN7410N
SN7402N
SN74H11N
BUFRFULL-
BUFRMTY-
AG/D
DRICLKENA


MEMREAD P1-59
SYCL-SH1
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
P1-57 MCΦ- Z4(401) SN7404N MCΦC
SN7400N Z19 (105) MEMCYC- SN7404N MEMCYC
Z35(208) SN7404N
SN74H11N Z10 (203) MC1/DC
SH1 DEVREAD LC3/Q LC4/Q SN7402N Z23 (505)
SH3 LC3+LC4
SN7400N Z33 (507) MEMREAD
MC4/DC- Z35(208) SN7404N MC4/DC MC6/DC
SH1 STATBUSY-
SN7404N Z4(401) MEMREADC- SN7408N Z5 (501) DB2/Q-
SH3
VCC
SN7420N Z31 (307)
SH2 STATBUSY
Z40 (209) SN7400N
MC6/DC- Z45(210) SN7404N
P1-4 AG SN7404N Z6(102) AG/A-
SN7400N Z24 (104) AG/Q AG/D
SH3 AG/D
SH2 SC5/Q
P1-24 DECΦUNT-
R6 VCC
CLOCK Z34 SN74174N (108) CLEAR
MC1/QC SH3
MC4/QC SH3
MC5/QC SN7404N Z45(210) MC5/QC- MC6/QC SH3
MC7/QC SN7404N Z6(102) MC7/QC- SH2
SN7400N Z9 (103) SC5Φ- SN7400N Z11 (303) CNTADV
SN7402N Z12 (403) CNTUP- P1-22
LIST3 SH1
MEMRD- P1-75
SH3 DRF1/Q
SN7400N Z40 (209) DRF1/D
VCC PRESET Z29 (107) SN74H74N CLOCK CLEAR
SH3 DRICLKENA-
SN7410N Z41 (309) DR1CLKEN
SH1 MEMEN-
SH1 SYCLC
SN7400N Z48 (410) DR1F1/CLK-
DRF1/Q- SH2
RESETA- SH1
ACK SH1
SH3 SC2/Q
SH3 SC2/R
SN7400N Z46 (310) SC3A/S-
VCC PRESET Z29 (107) SN74H74N CLOCK CLEAR
SC3/Q
SC3/Q SH2
SN7402N Z27 (404) STCY- SH3
STATBUSY ZONE C-8
16 VCC R1 1 ACK-
Z26(306) SN7404N ACK
P1-8 ACK-
SH5 AR/Q-
SH2 SC3/R
Z9 (109) SN7400N SC3A/R
SN7400N Z19 (105) SC3/R
SN7410N Z30 (207) SC3/D
INTEN
SN7404N (210) Z45
SH3 SCΦ/R
P1-40 INTEN-
SN7400N Z25 (204) SC3B/S-
R5 VCC
-2 -1 QTY REQD ITEM NO CODE IDENT PART OR IDENTIFYING NUMBER NOMENCLATURE OR DESCRIPTION PROCUREMENT SPECIFICATION
PARTS LIST
UNLESS OTHERWISE SPECIFIED
• REMOVE ALL BURRS AND SHARP EDGES
• CONCENTRICITY MACHINED DIAMETERS .010 FIR
• DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
• IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
• INTERPRET DRAWING IN ACCORDANCE WITH MIL STD-100
HOLE TOLERANCE
.013 THRU .104 ± .001 .125
.126 THRU .500 ± .005 .001
.251 THRU .500 ± .006 .001
.501 THRU .750 ± .008 .001
.751 THRU 1.000 ± .010 .001
1.001 THRU 2.000 ± .012 .001
NEXT ASSY USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED
• DIMENSIONS ARE IN INCHES
• TOLERANCES ANGLES ±1°
3 PLACE DECIMALS ± .010
2 PLACE DECIMALS ± .02
MATERIAL
DWN DATE 4-5-73
CHK
ENGR
IA
APVD
CONTR NO
DESIGN ACTIVITY RELEASE
TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas Texas
DIAGRAM, LOGIC, DETAILED- BTC*3 (PWB)
SIZE D CODE IDENT NO 96214 DRAWING NO 966730
SCALE NONE REV C SHEET 3


8
7
6
5
4
3
2
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
Z2 (201) SN74145N
SH 3 DEVADSEL0
SH 3 AR/Q -
ARDEV;0 - P1-14
ARDEV;1 - P1-15
ARDEV;2 - P1-16
ARDEV;3 - P1-17
ARDEV;4 - P1-18
ARDEV;5 - P1-19
ARDEV;6 - P1-20
ARDEV;7 - P1-21
NC
NC
Z3 (301) SN74145N
SH 3 SC2/Q -
INTDEV;0 - P1-32
INTDEV;1 - P1-33
INTDEV;2 - P1-34
INTDEV;3 - P1-35
INTDEV;4 - P1-36
INTDEV;5 - P1-37
INTDEV;6 - P1-38
INTDEV;7 - P1-39
NC
NC
DEVADSEL0
DEVADSEL1
DEVADSEL2
SH 3
SH 3
Z7 (302) SN74151N
P1-41 IREC0G;0 -
P1-42 IREC0G;1 -
P1-43 IREC0G;2 -
P1-44 IREC0G;3 -
P1-45 IREC0G;4 -
P1-46 IREC0G;5 -
P1-47 IREC0G;6 -
P1-48 IREC0G;7 -
STROBE
IREC0G - SH 3
NC
GND
VCC
C1 22µF 15V 10%
C3 THRU C8 .05µF 12V 20%
C2 22µF 15V 10%
P1-78
P1-77
P1-1
P1-2
P1-79
P1-80
SPARES
SN7400N Z48 (410)
SN7402N Z44 (110)
SN7402N Z44 (110)
SN7402N Z44 (110)
SN7408 Z49 (510)
SN7486N Z13 (503)
PARTS LIST
-2 QTY REQD -1 ITEM NO CODE IDENT PART OR IDENTIFYING NUMBER NOMENCLATURE OR DESCRIPTION PROCUREMENT SPECIFICATION
UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIR
- DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
- IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
- INTERPRET DRAWING IN ACCORDANCE WITH MIL STD-100
HOLE TOLERANCE
.013 THRU .124 +.004 -.001
.126 THRU 250 +.005 -.001
251 THRU 500 +.006 -.001
501 THRU 755 +.008 -.001
751 THRU 1.000 +.010 -.001
1.001 THRU 2.000 -.012 -.001
NEXT ASSY USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES
ANGLES ±1°
3 PLACE DECIMALS ± .010
2 PLACE DECIMALS ± .02
MATERIAL
DWN A.Ortega DATE 4-5-73
CHK
ENGR
QA
APVD
CONTR NO
DESIGN ACTIVITY RELEASE
TEXAS INSTRUMENTS INCORPORATED Assembly Group Dallas, Texas
DIAGRAM, LOGIC, DETAILED- BIC #3 (PWB)
SIZE D CODE IDENT NO 96214 DRAWING NO 966780
SCALE NONE REV C SHEET 5
TI-7914E P3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	378488 (E) 8/31/73 Dick Wilson 1. ON SH 1: AREA D-7, ADDED "SH 2" TO "PERROR." AREA C-3, ADDED "SN 2" TO ENRFW & ENRFR. 2. ON SH 2: AREA A-6, ADDED CHART. AREA D-5, ADDED "SN 1" TO "HARESET." AREA C-5, ADDED "SN 1" & GRD TO "PERROR." AREA B-4, ADDED "SN 1" TO "ENRFW" AREA B-3, ADDED "SEE CHART" TO C14 WIRE PLUG.	9/31/73	

NOTES: UNLESS OTHERWISE SPECIFIED
1. N.C DENOTES NO CONNECTIONS
2. ALL RES. ARE 470Ω, .125W ±5%

SPARES

SN7408N A4 · SN7400N A3 · SN7408N A4 · SN7400N B5 · SN7410N B4 · SN7402N B6 · SN7486N C1 · SN7402N B6 · SN7486N C1 · SN7404N C6 · SN7404N C6

QTY REQD	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIR
- DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
- IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
- INTERPRET DRAWING IN ACCORDANCE WITH MIL STD-100

HOLE TOLERANCE

.013 THRU .064 / .128 THRU .001	.125 THRU .009 / .250 THRU .001	.251 THRU .006 / .500 THRU .001
.501 THRU .008 / .750 THRU .001	.751 THRU .010 / 1.000 THRU .001	1.001 THRU .012 / 2.000 THRU .001

NEXT ASSY | USED ON | APPLICATION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES ANGLES ±1°
  3 PLACE DECIMALS ±.010
  2 PLACE DECIMALS ±.02

MATERIAL

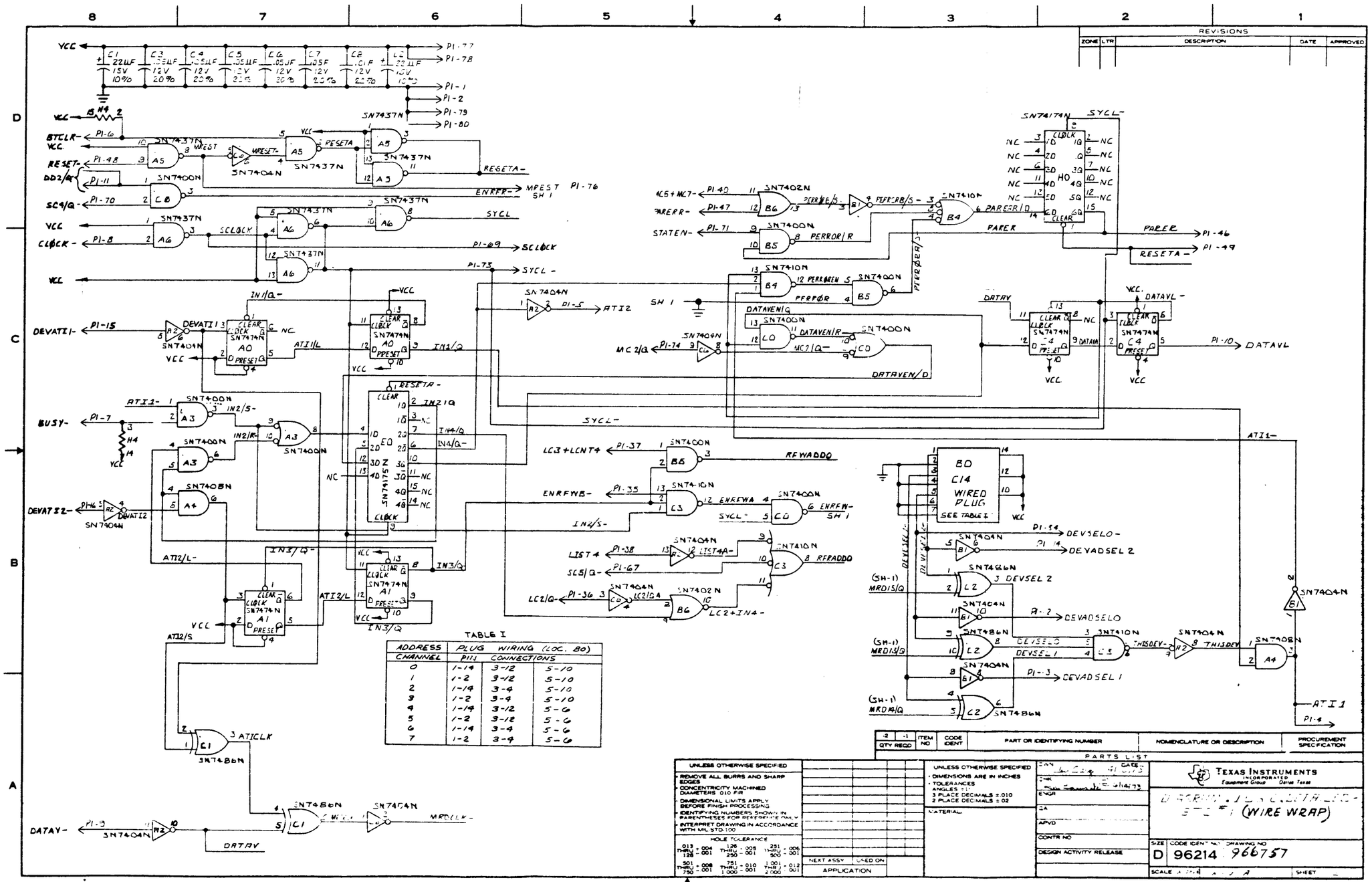
DRN | DATE
CHK
ENGR
APVD
CONTR NO
DESIGN ACTIVITY RELEASE

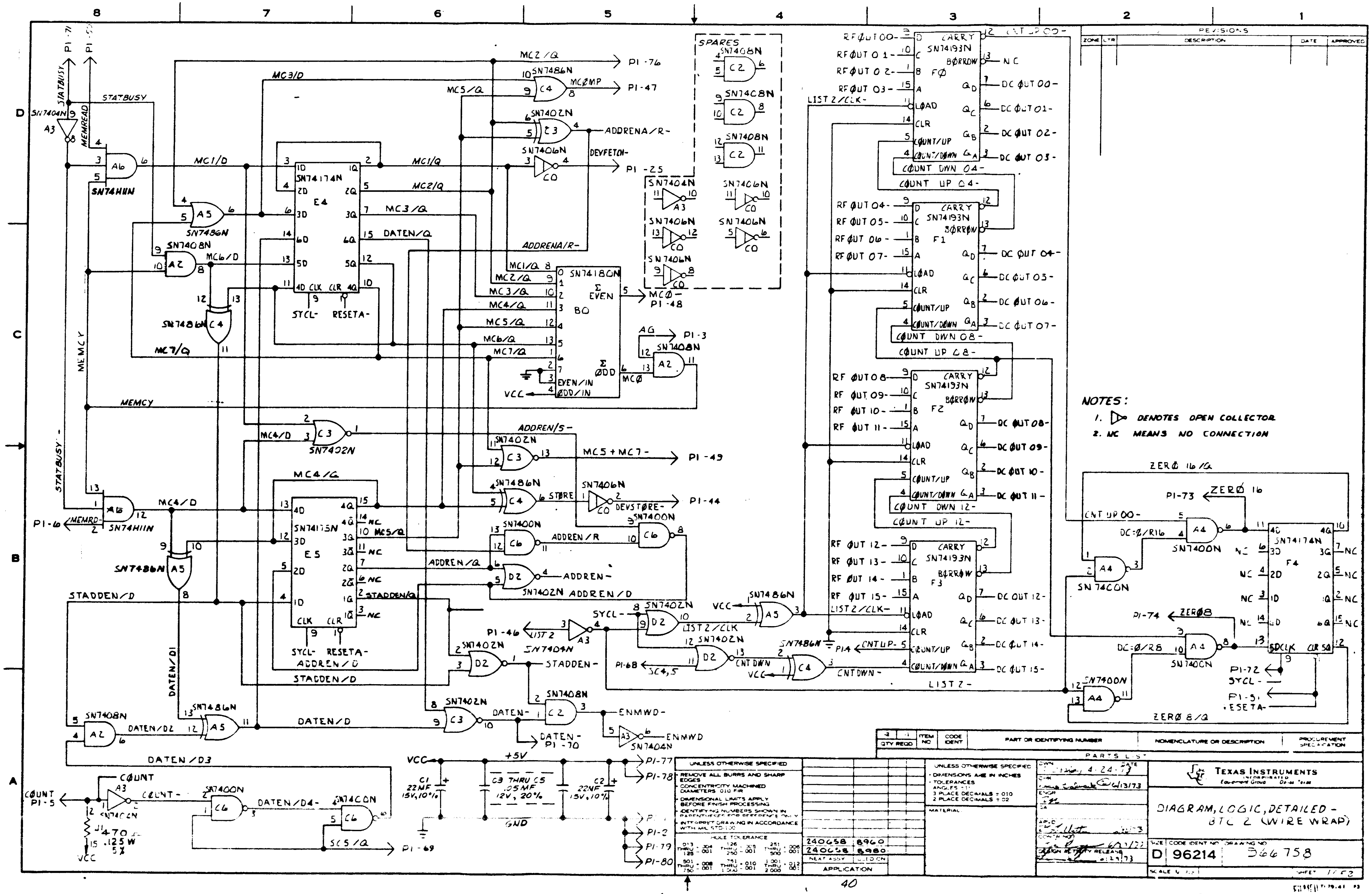
TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas Texas

DIAGRAM, LOGIC, DETAILED
BIC #1 (WIRE WRAP)

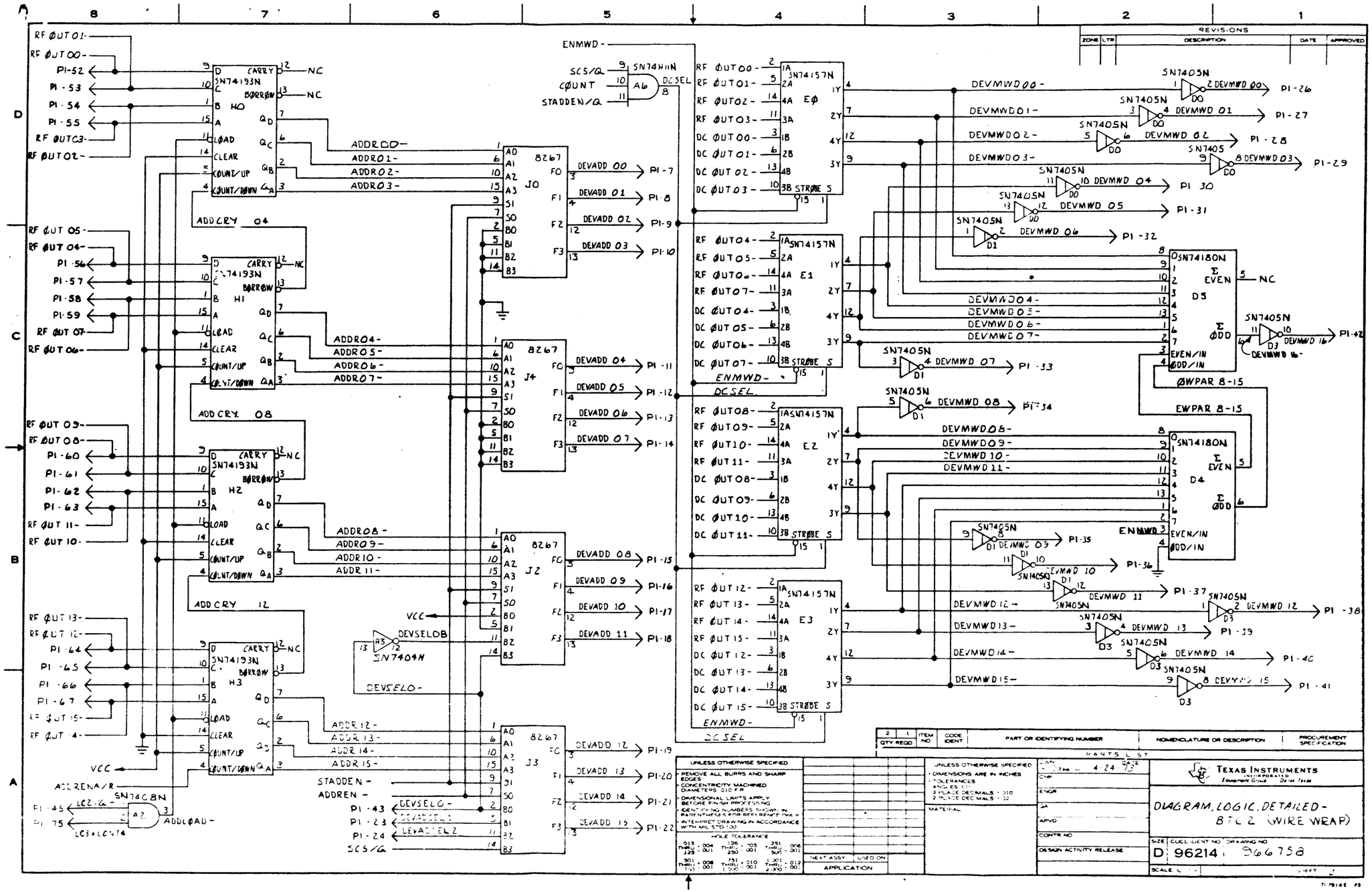
SIZE D | CODE IDENT NO 96214 | DRAWING NO 966757
SCALE NONE | REV A | SHEET 1 OF 2

T-79148 P3


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
TABLE I
ADDRESS CHANNEL | PLUG WIRING (LOC. B0) PIN CONNECTIONS
0 | 1-14 | 3-12 | 5-10
1 | 1-2 | 3-12 | 5-10
2 | 1-14 | 3-4 | 5-10
3 | 1-2 | 3-4 | 5-10
4 | 1-14 | 3-12 | 5-6
5 | 1-2 | 3-12 | 5-6
6 | 1-14 | 3-4 | 5-6
7 | 1-2 | 3-4 | 5-6
PARTS LIST
QTY REQD | ITEM NO | CODE IDENT | PART OR IDENTIFYING NUMBER | NOMENCLATURE OR DESCRIPTION | PROCUREMENT SPECIFICATION
UNLESS OTHERWISE SPECIFIED
• REMOVE ALL BURRS AND SHARP EDGES
• CONCENTRICITY MACHINED DIAMETERS .010 FIR
• DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
• IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
• INTERPRET DRAWING IN ACCORDANCE WITH MIL STD-100
HOLE TOLERANCE
.013 THRU .064 = ±.001
.126 THRU .250 = ±.001
.251 THRU .500 = ±.001
.501 THRU .750 = ±.001
.751 THRU 1.000 = ±.001
1.001 THRU 2.000 = ±.001
NEXT ASSY | USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED
• DIMENSIONS ARE IN INCHES
• TOLERANCES
ANGLES ±1°
3 PLACE DECIMALS ± .010
2 PLACE DECIMALS ± .02
MATERIAL
DRAWN
CHK
ENGR
QA
APVD
CONTR NO
DESIGN ACTIVITY RELEASE
TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas Texas
SIZE D | CODE IDENT NO 96214 | DRAWING NO 966757
SCALE | SHEET
TI-79144 #3



NOTES:
1. DENOTES OPEN COLLECTOR
2. NC MEANS NO CONNECTION
SPARES
SN74174N
SN74193N
SN74180N
SN7486N
SN7402N
SN7406N
SN7408N
SN7404N
SN7400N
UNLESS OTHERWISE SPECIFIED
PARTS LIST
APPLICATION
TEXAS INSTRUMENTS
DIAGRAM, LOGIC, DETAILED - BTC 2 (WIRE WRAP)
D 96214
366758
40


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
RF OUT01-
RF OUT00-
PI-52
PI-53
PI-54
PI-55
RF OUT03-
RF OUT02-
SN74193N
ADDR00-
ADDR01-
ADDR02-
ADDR03-
ADD CRY 04
RF OUT 05-
RF OUT 04-
PI-56
PI-57
PI-58
PI-59
RF OUT 07-
RF OUT 06-
ADDR04-
ADDR05-
ADDR06-
ADDR07-
ADD CRY 08
RF OUT 09-
RF OUT 08-
PI-60
PI-61
PI-62
PI-63
RF OUT 11-
RF OUT 10-
ADDR08-
ADDR09-
ADDR10-
ADDR 11-
ADD CRY 12
RF OUT 13-
RF OUT 12-
PI-64
PI-65
PI-66
PI-67
RF OUT 15-
RF OUT 14-
ADDR 12-
ADDR 13-
ADDR 14-
ADDR 15-
VCC
ADDRENA/R
SN74C8N
LC2+G-
LC3+LC4+14
ADDLOAD-
STADDEN-
ADDREN-
PI-43
PI-23
PI-24
SCS/G
DEVSELO-
DEVADDEL2
LEDADDEL2
8267
J0
J4
J2
J3
DEVADD 00
DEVADD 01
DEVADD 02
DEVADD 03
DEVADD 04
DEVADD 05
DEVADD 06
DEVADD 07
DEVADD 08
DEVADD 09
DEVADD 10
DEVADD 11
DEVADD 12
DEVADD 13
DEVADD 14
DEVADD 15
PI-7
PI-8
PI-9
PI-10
PI-11
PI-12
PI-13
PI-14
PI-15
PI-16
PI-17
PI-18
PI-19
PI-20
PI-21
PI-22
ENMWD-
SCS/Q
COUNT
STADDEN/Q
SN74H11N
DCSEL
DEVSELOB
SN7409N
SN74157N
RF OUT00-
RF OUT01-
RF OUT02-
RF OUT03-
DC OUT00-
DC OUT01-
DC OUT02-
DC OUT03-
E0
STROBE S
RF OUT04-
RF OUT05-
RF OUT06-
RF OUT07-
DC OUT04-
DC OUT05-
DC OUT06-
DC OUT07-
E1
RF OUT08-
RF OUT09-
RF OUT10-
RF OUT11-
DC OUT08-
DC OUT09-
DC OUT10-
DC OUT11-
E2
RF OUT12-
RF OUT13-
RF OUT14-
RF OUT15-
DC OUT12-
DC OUT13-
DC OUT14-
DC OUT15-
E3
SCSEL
DEVMWD00-
DEVMWD01-
DEVMWD02-
DEVMWD03-
DEVMWD04-
DEVMWD05-
DEVMWD06-
DEVMWD07-
DEVMWD08-
DEVMWD09-
DEVMWD10-
DEVMWD11-
DEVMWD12-
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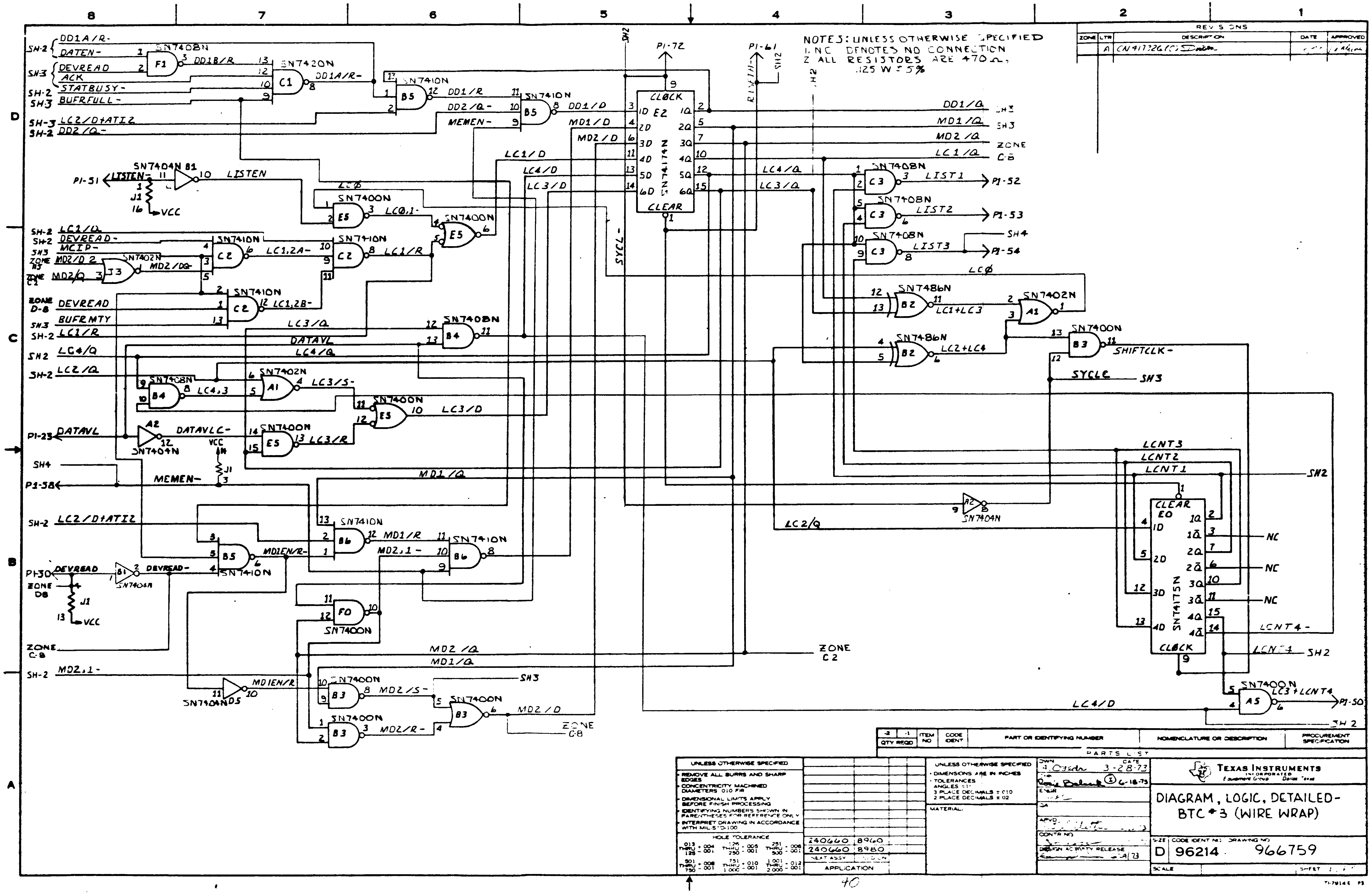
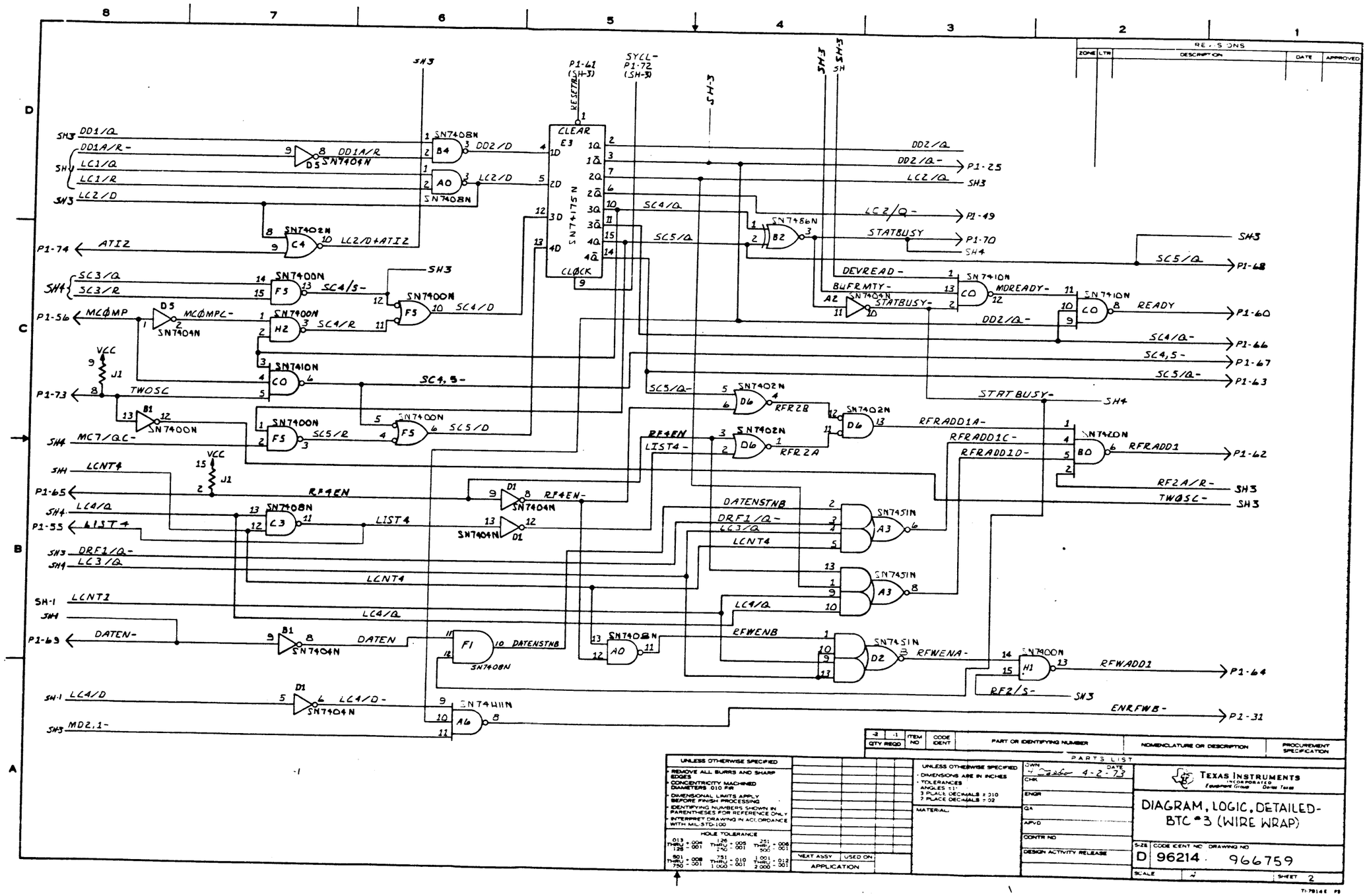
DEVMWD 10
DEVMWD 11
DEVMWD 12
DEVMWD 13
DEVMWD 14
DEVMWD 15
PI-26
PI-27
PI-28
PI-29
PI 30
PI-31
PI-32
PI-33
PI-34
PI-35
PI-36
PI-37
PI-38
PI-39
PI-40
PI-41
SN74180N
D5
D4
EVEN
ODD
EVEN/IN
ODD/IN
ØWPAR 8-15
EWPAR 8-15
DEVMWD 16
PI-42
PARTS LIST
ITEM NO
CODE IDENT
PART OR IDENTIFYING NUMBER
NOMENCLATURE OR DESCRIPTION
PROCUREMENT SPECIFICATION
UNLESS OTHERWISE SPECIFIED
REMOVE ALL BURRS AND SHARP EDGES
CONCENTRICITY MACHINED DIAMETERS .010 F.I.M.
DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
IDENTIFYING NUMBERS SHOWN IN PARENTHESES ARE REFERENCE ONLY
INTERPRET DRAWING IN ACCORDANCE WITH MIL STD 100
MATERIAL
NEXT ASSY
USED ON
APPLICATION
DRAWN 4-24-73
CHK
ENGR
APVD
CONTR NO
DESIGN ACTIVITY RELEASE
TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas Texas
DIAGRAM, LOGIC, DETAILED - BTL2 (WIRE WRAP)
SIZE D
CODE IDENT NO 96214
DRAWING NO 966758
SCALE
SHEET


NOTES: UNLESS OTHERWISE SPECIFIED
1. NC DENOTES NO CONNECTION
2. ALL RESISTORS ARE 470 Ω, .125 W ± 5%
DIAGRAM, LOGIC, DETAILED-BTC #3 (WIRE WRAP)
TEXAS INSTRUMENTS INCORPORATED
D 96214 966759
APPLICATION
240660 8960
240660 8980



QTY REQD	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIR
- DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
- IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
- INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100

HOLE TOLERANCE

.013 THRU .128 ± .001	.126 THRU .250 ± .001	.251 THRU .500 ± .001	
.501 THRU .750 ± .001	.751 THRU 1.000 ± .001	1.001 THRU 2.000 ± .002	

NEXT ASSY | USED ON | APPLICATION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES ANGLES ±1°
  3 PLACE DECIMALS ± .010
  2 PLACE DECIMALS ± .02

MATERIAL

DWN	DATE 4-2-73
CHK	
ENGR	
QA	
APVD	
CONTR NO	
DESIGN ACTIVITY RELEASE	

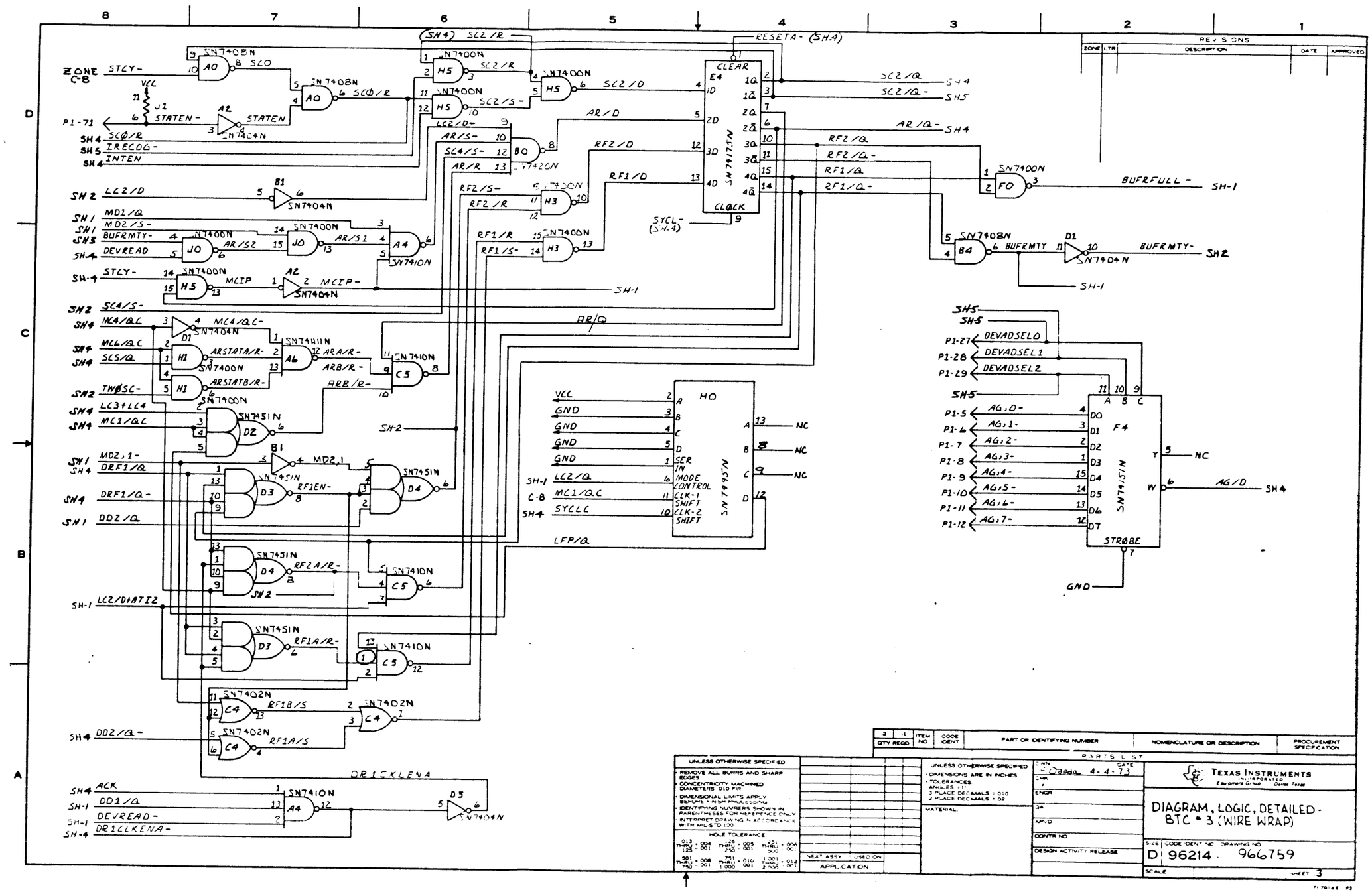
TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas Texas

DIAGRAM, LOGIC, DETAILED- BTC #3 (WIRE WRAP)

SIZE	CODE IDENT NO	DRAWING NO
D	96214	966759

SCALE | SHEET 2

TI-7914E PS



ZONE	LTR	DESCRIPTION	DATE	APPROVED

REVISIONS

QTY REQD	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIR
- DIMENSIONAL LIMITS APPLY BEFORE FINISH PHLASSING
- IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
- INTERPRET DRAWING IN ACCORDANCE WITH MIL STD 100

HOLE TOLERANCE

.013 THRU .125 ± .004 .001	.126 THRU .250 ± .005 .001	.251 THRU .500 ± .006 .001
.501 THRU .750 ± .008 .001	.751 THRU 1.000 ± .010 .001	1.001 THRU 2.000 ± .012 .001

NEXT ASSY USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES
  ANGLES ± 1°
  3 PLACE DECIMALS ± .010
  2 PLACE DECIMALS ± .02

MATERIAL

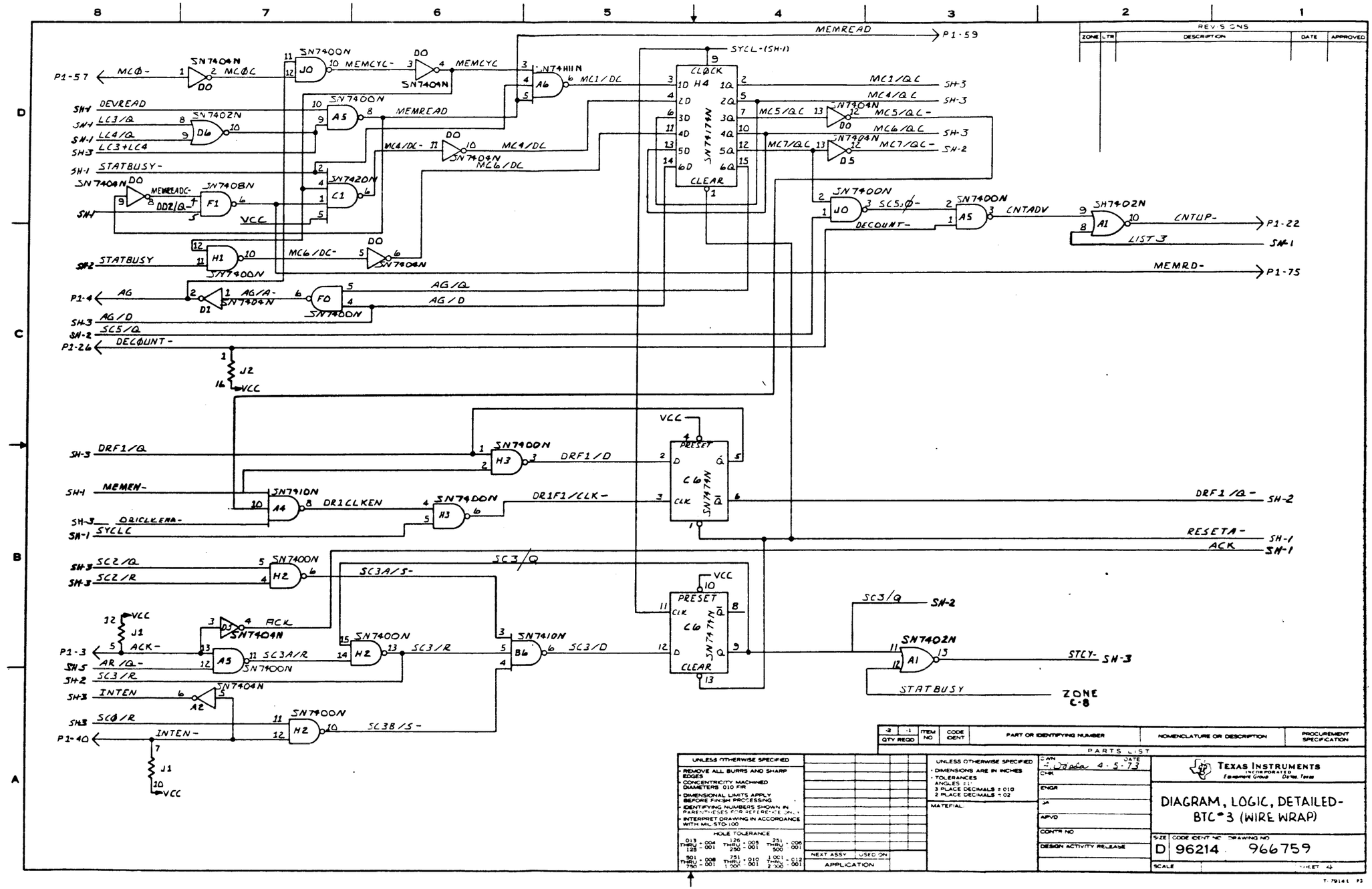
		DATE
DRAWN	J. Dodd	4-4-73
CHK		
ENGR		
QA		
APVD		
CONTR NO		
DESIGN ACTIVITY RELEASE		

TEXAS INSTRUMENTS INCORPORATED
Equipment Group Dallas Texas

DIAGRAM, LOGIC, DETAILED - BTC * 3 (WIRE WRAP)

SIZE	CODE IDENT NO	DRAWING NO
D	96214	966759

SCALE — SHEET 3



-3 QTY REQD	-1	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIR
- DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
- IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
- INTERPRET DRAWING IN ACCORDANCE WITH MIL STD-100

HOLE TOLERANCE

.013 THRU .125 = .004 .001	.126 THRU .250 = .005 .001	.251 THRU .500 = .006 .001
.501 THRU .750 = .008 .001	.751 THRU 1.000 = .010 .001	1.001 THRU 2.100 = .012 .001

NEXT ASSY | USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES
  ANGLES ±1°
  3 PLACE DECIMALS ± .010
  2 PLACE DECIMALS ± .02

MATERIAL

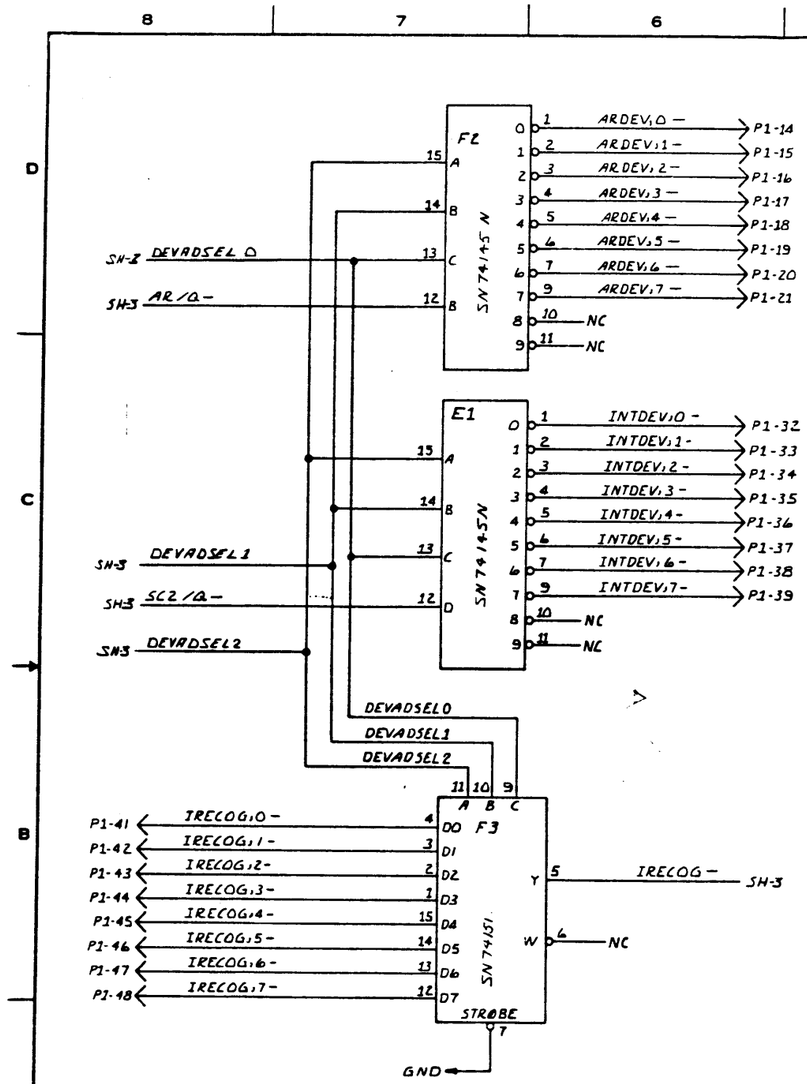
DWN — Dallas 4-5-73 (DATE)
CHK
ENGR
PM
APVD
CONTR NO
DESIGN ACTIVITY RELEASE

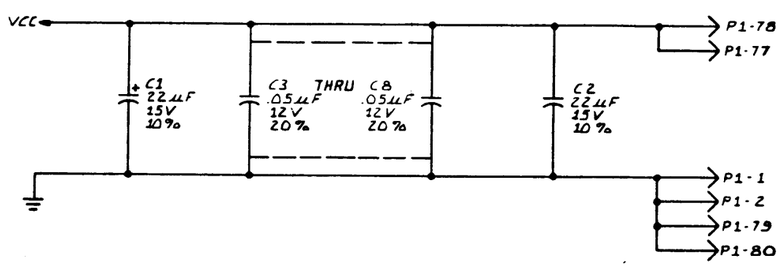
TEXAS INSTRUMENTS INCORPORATED
Equipment Group Dallas, Texas

DIAGRAM, LOGIC, DETAILED-BTC*3 (WIRE WRAP)

SIZE D | CODE IDENT NO 96214 | DRAWING NO 966759
SCALE | SHEET 41

T-79141 P3





ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED

-2 QTY REQD	-1	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 F/R
- DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
- IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
- INTERPRET DRAWING IN ACCORDANCE WITH MIL STD 100

HOLE TOLERANCE

.013 THRU .064 / .128 .001	.126 THRU .500 / .250 .001	.251 THRU .500 / .505 .001
.501 THRU .008 / .750 .001	.751 THRU 1.000 .010 / 1.000 .001	1.001 THRU 2.000 .012 / 2.000 .001

NEXT ASSY | USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES
  ANGLES ± 1°
  3 PLACE DECIMALS ± .010
  2 PLACE DECIMALS ± .02

MATERIAL

DWN J. Jarabo DATE 4-5-73
CHK
ENGR
QA
APVD
CONTR NO
DESIGN ACTIVITY RELEASE

TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas Texas

DIAGRAM, LOGIC, DETAILED- BTC*3 (WIRE WRAP)

SIZE D | CODE IDENT NO 96214 | DRAWING NO 966759
SCALE | A | SHEET 5

TI 70146 F3

ALPHABETICAL INDEX

ALPHABETICAL INDEX

INTRODUCTION

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections–References to Sections of the manual appear as "Section x" with the symbol x representing any numeric quantity.
- Appendixes–References to Appendixes of the manual appear as "Appendix y" with the symbol y representing any capital letter.
- Paragraphs–References to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph is found.
- Tables–References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number:

  Tx-yy

- Figures–References to figures in the manual are represented by the capital letter F followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the figure). The second character is followed by a dash (-) and a number:

  Fx-yy

- Other entries in the Index–References to other entries in the index are preceded by the word "See" followed by the referenced entry.

USER'S RESPONSE SHEET

Manual Title: Block Transfer Controller Maintenance Manual (240802-9701)

Manual Date: 1 November 1976 **Date of This Letter:** _____

User's Name: _____ **Telephone:** _____

Company: _____ **Office/Department:** _____

Street Address: _____

City/State/Zip Code: _____

Please list any discrepancy found in this manual by page, paragraph, figure, or table number in the following space. If there are any other suggestions that you wish to make, feel free to include them. Thank you.

CUT ALONG LINE

Location in Manual	Comment/Suggestion
_____	_____
	_____
	_____
	_____
_____	_____
	_____
	_____
	_____
_____	_____
	_____
	_____
	_____

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FOLD

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UNITED STATES

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DIGITAL SYSTEMS GROUP

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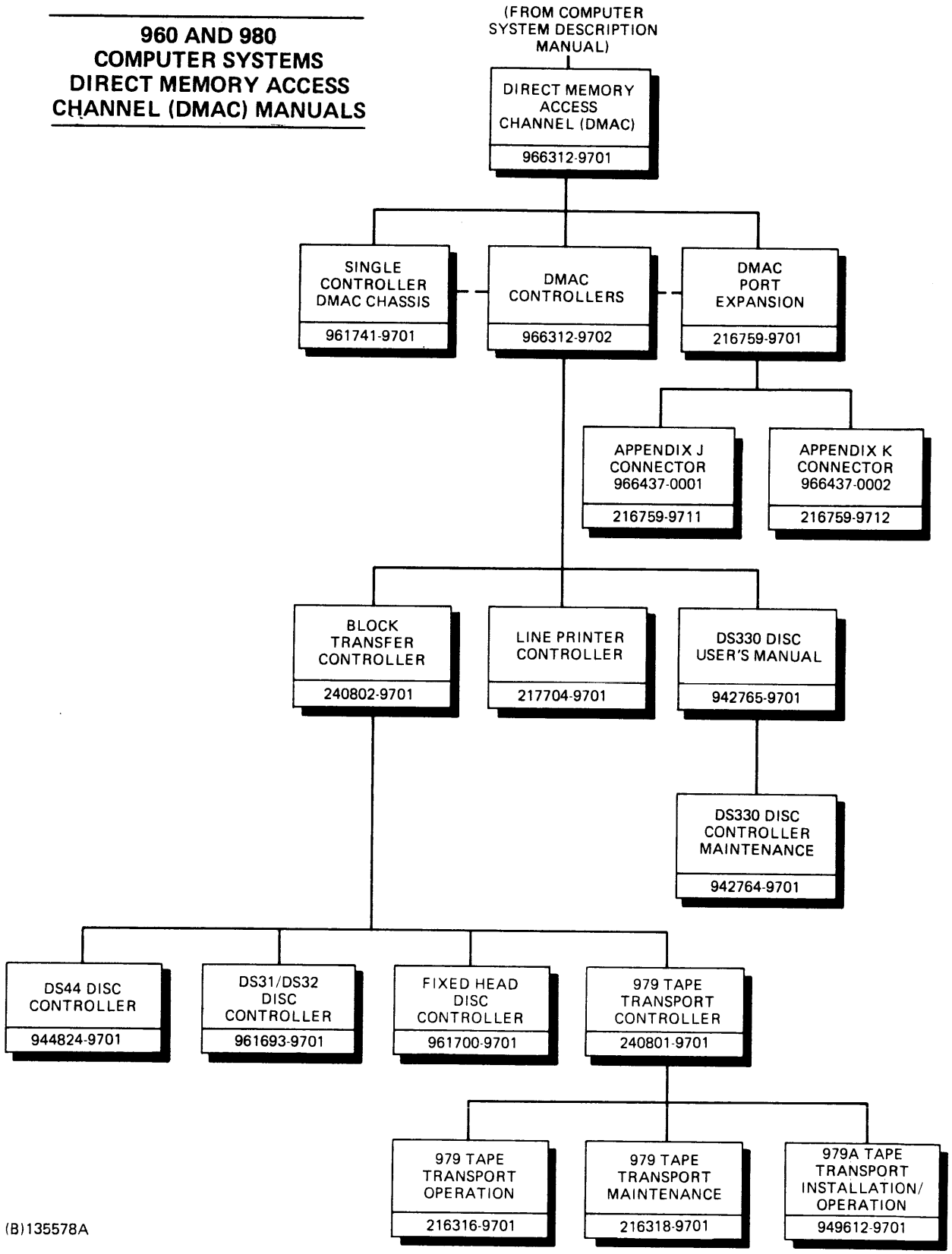
Austin, Texas 78769

FOLD

960 AND 980 COMPUTER SYSTEMS DIRECT MEMORY ACCESS CHANNEL (DMAC) MANUALS



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