DIAGNOSTICS

(DIAGNOSTIC NN(AA*BB)

NN = DIAGNOSTIC NUMBER
AA = TASK ID
BB = LOGICAL UNIT NUMBER

DIAGNOSTIC	MEANING
00	CARD READER ERROR – read card again
01	DISC WRITE LOCKOUT – write attempted on a write protect area of disc
02	DISC PARITY ERROR OR READ AFTER WRITE ERROR – parity error during a read or read after write error during a write
03	SEQUENTIAL ACCESS BOUND ERROR – attempt made to read, write, or forward space beyond end of a sequential file
04	MAGNETIC TAPE ERROR – write ring error
05	MAGNETIC TAPE ERROR – off-line
06	MAGNETIC TAPE ERROR – parity or data transfer error during a read
07	HIGH SPEED PAPER TAPE PUNCH ERROR – low tape indication
08	DEVICE BROKEN ERROR
09	DISC NOT READY
0A . . 0F	RESERVED

TASK ERRORS

When a worker task has a detectable error (which does not destroy the supervisor), it is disabled and a message of the following form is output on logical unit 9 and 0.

TASK 3F, ERROR 03, AT 093F.

This message means that the task, the identifier being 3F, made an invalid supervisor call from location X'093F'. The meaning of the error codes are:

ERROR	MEANING
00	Illegal Computer Instruction
01	Protected Memory Violation
02	Memory Parity Error
03	Invalid Supervisor Call
04	Invalid Logical Unit Number
05 . . 09	RESERVED
0A	PCL ERROR – Argument count inconsistent with call
0B	PCL ERROR – I/O unit number not defined
0C	PCL ERROR – Input mode inconsistent with format
0D	PCL ERROR – Illegal format
0E	PCL ERROR – Read error
0F	RESERVED

LIST OF SUPERVISOR CALLS

SERVICE MODULE	PSM	PAM	PAM/D	FUNCTION	OP. CODE 16-BIT	OP. CODE 8-BIT
IOQ	X	X	X	NORMAL I/O REQUEST	0000	00
EOP	X	X	X	END OF PROGRAM	0400	01
SIDT		X	X	SID TASK	0800	02
MULTPY	X	X	X	MULTIPLY	0C00	03
DIVIDE	X	X	X	DIVIDE	1000	04
SCLD	X	X	X	SHIFT CIRCULAR LEFT DOUBLE	1400	05
EOJ	X	X	X	END OF JOB	1800	06
SQRT	X	X	X	SQUARE ROOT	1C00	07
CBHA	X	X	X	CONVERT BINARY TO HEXADECIMAL ASCII	2000	08
CHAB	X	X	X	CONVERT HEXADECIMAL ASCII TO BINARY	2400	09
CBDA	X	X	X	CONVERT BINARY TO DECIMAL ASCII	2800	0A
CDAB	X	X	X	CONVERT DECIMAL ASCII TO BINARY	2C00	0B
TIMDLY		X	X	TIME DELAY	3000	0C
WAIT		X	X	UNCONDITIONAL WAIT	3400	0D
UNBUSP		X	X	ACTIVATE WAITING TASK	3800	0E
WTINT		X	X	WAIT FOR INTERRUPT	3C00	0F
GTDATE		X	X	GET DATE AND TIME	4000	10
GTDBLK		X	X	GET DATA BLOCK	4400	11
FIXFLT	X	X	X	CONVERT FIXED POINT TO FLOATING POINT	4800	12
FLTFIX	X	X	X	CONVERT FLOATING POINT TO FIXED POINT	4C00	13
FLTADD	X	X	X	FLOATING POINT ADD	5000	14
FLTSUB	X	X	X	FLOATING POINT SUBTRACT	5400	15
FLTMUL	X	X	X	FLOATING POINT MULTIPLY	5800	16
FLTDIV	X	X	X	FLOATING POINT DIVIDE	5C00	17
CONVBE	X	X	X	CONVERT FLOATING TO ASCII–E FORMAT	6000	18
FSIN	X	X	X	SINE	6400	19
FCOS	X	X	X	COSINE	6800	1A
ARCTAN	X	X	X	ARCTANGENT	6C00	1B
WTIOC			X	WAIT FOR I/O COMPLETE	7000	1C
LOVLY			X	LOAD OVERLAY FROM DISC	7400	1D
MWBUFC			X	MESSAGE WRITER OUTPUT REQUEST	7800	1E
PCLIO	X	X	X	PCL I/O FORMAT EDITOR	7C00	1F
PCLRP	X	X	X	PCL RUN-TIME PACKAGE	8000	20
PCLWT	X	X	X	PCL TIME DELAY	8400	21
PCLOV			X	LOAD PCL INTERPRETER OVERLAY	8800	22

OP Codes 8C00(23) – 9000(24) are reserved for PCL in PSM, PAM, PAM/D.
Parameter words are indicated for each monitor system. All calls may not be implemented in all systems since many are optional.

PROGRAMMER REFERENCE CARD

Model 960A Computer

TEXAS INSTRUMENTS
INCORPORATED
DIGITAL SYSTEMS DIVISION
P.O. BOX 1444 HOUSTON, TEXAS 77001

November 1, 1971 TI030-5M-11/71

DEDICATED MEMORY LOCATIONS

MEMORY ADDR$_{16}$	FUNCTION	MEMORY ADDR$_{16}$	FUNCTION
90 - 91	Internal Interrupt	9A - 9B	Status, Device Controller 1
92 - 93	External Interrupt	9C - 9D	Status, Device Controller 2
94 - 95	Communication Register Unit Interrupt	9E - 9F	Status, Device Controller 3
		A0 - A1	Status, Device Controller 4
96 - 97	Direct Memory Access Interrupt Status	A2 - A3	Status, Device Controller 5
		A4 - A5	Status, Device Controller 6
98 - 99	Status, Device Controller 0	A6 - A7	Status, Device Controller 7

HEXADECIMAL AND DECIMAL CONVERSION

To find the decimal number, locate the Hex number and its decimal equivalent for each position. Add these to obtain the decimal number. To find the Hex number, locate the next lower decimal number and its Hex equivalent. Each difference is used to obtain the next Hex number until the entire number is developed.

BYTE				BYTE			
0123		4567		0123		4567	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0
1	4,096	1	256	1	16	1	1
2	8,192	2	512	2	32	2	2
3	12,288	3	768	3	48	3	3
4	16,384	4	1,024	4	64	4	4
5	20,480	5	1,280	5	80	5	5
6	24,576	6	1,536	6	96	6	6
7	28,672	7	1,792	7	112	7	7
8	32,768	8	2,048	8	128	8	8
9	36,864	9	2,304	9	144	9	9
A	40,960	A	2,560	A	160	A	10
B	45,056	B	2,816	B	176	B	11
C	49,152	C	3,072	C	192	C	12
D	53,248	D	3,328	D	208	D	13
E	57,344	E	3,584	E	224	E	14
F	61,440	F	3,840	F	240	F	15
4		3		2		1	

CHARACTERS RECOGNIZED BY SAL

ASCII	H. CODE	CH.	ASCII	H. CODE	CH.	ASCII	H. CODE	CH.
20	Null	SP.	36	6	6	48	11•2	K
21	11•8•2	!	37	7	7	4C	11•3	L
22	8•7	"	38	8	8	4D	11•4	M
23	8•3	#	39	9	9	4E	11•5	N
24	11•8•3	$	3A	8•2	:	4F	11•6	O
25	0•8•4	%	3B	11•8•6	;	50	11•7	P
26	12	&	3C	12•8•4	<	51	11•8	Q
27	8•5	'	3D	8•6	=	52	11•9	R
28	12•8•5	(	3E	0•8•6	>	53	0•2	S
29	11•8•5	)	3F	0•8•7	?	54	0•3	T
2A	11•8•4	*	40	8•4	@	55	0•4	U
2B	12•8•6	+	41	12•1	A	56	0•5	V
2C	0•8•3	,	42	12•2	B	57	0•6	W
2D	11	-	43	12•3	C	58	0•7	X
2E	12•8•3	.	44	12•4	D	59	0•8	Y
2F	0•1	/	45	12•5	E	5A	0•9	Z
30	0	0	46	12•6	F	5B	UD	
31	1	1	47	12•7	G	5C	UD	
32	2	2	48	12•8	H	5D	UD	
33	3	3	49	12•9	I	5E	UD	
34	4	4	4A	11•1	J	5F	UD	
35	5	5						

UD = UNDEFINED; Control Character ASCII - 17, 0•9•6 = EOB, block end

WORKER TASK BLOCK*

	0	15	
0	SAVED EC (RETURN ADDRESS)		
1	SAVED STATUS 0 1 2 3 4 5 6 7 8	15	
2	RANK		All flags except EACT (Bit 3) are cleared when a task is installed.
3	SAVED WR0		
4	SAVED WR1		
5	WR2		
6	WR3		
7	WR4 (DATA BASE ADDR.) USUALLY WR8(0)		Loaded by job control when task is installed.
8	WR5 (PROCEDURE BASE ADDR.)		Loaded by job control if a procedure is attached.
9	WR6 (FLAG BASE ADDR.)		
10	WR7 (CRU BASE ADDR.)		
11	INITIAL STATUS		
12	PROCEDURE ENTRY POINT		Loaded by job control if a procedure is attached.
13	TIMER		
14	LINK TO NEXT TASK		
15	PROC. I.D.	TASK I.D.	PROC. I.D. is set to FF by job control unless a procedure is attached.
16	END ACTION STATUS		These two words are present only if EACT=1.
17	END ACTION ENTRY POINT		

*First sixteen consecutive locations of task data segment. (Eighteen if end action specified.)

BIT	BIT USE (WTB WORD 2)
0	ABLE, set when the task is able to be executed. Cleared when task makes an error.
1	BID, set when the task is bid, or has been requested to execute.
2	SUSP, set when the task is suspended (normally awaiting I/O completion)
3	EACT, set by the user when end-action is desired; cleared when end-action is taken.
4	MW, set when the task is waiting for service of the message writer.
5	TD, set when the task is a time delay.
6	RESERVED
7	RESERVED

PHYSICAL RECORD BLOCK

	0	15
0	WTB ADDRESS	
1	DATA BUFFER ADDRESS	
2	DATA BUFFER LENGTH (CHARACTER COUNT)	
3	DATA RECORD LENGTH (CHARACTER COUNT)	
4	BUSY ERR EOF IN/EX* CON* R/W* B/A* WT LUNO †	

*Set by calling task † Logical unit number 0-1F system reserved; FF illegal

BIT		FLAG USE (PRB WORD 4)
0	BUSY	1 = I/O in progress, 0 = I/O complete
1	ERR	1 = Error on last operation, 0 = No error.
2	EOF	1 = End of File (/*) on last call, 0 = No End of File.
3	IN/EX	1 = Initiate Call (control returned to task immediately), 0 = Execute Call (control returned to task when I/O is complete).
4	CON	1 = Control Call, 0 = Character I/O.
5	R/W	1 = Read (input), 0 = Write (output).
6	B/A	1 = Binary record, 0 = ASCII record.
7	WT	1 = A task is waiting for this record to be complete, 0 = No one waiting.

NOTES

NOTES

INSTRUCTION LIST BY MNEMONIC

MNEM.	OP CODE	FORM.	NAME	EX. TIME
A	4C00 0000	1	ADD TO REGISTER	3.58
AA	4C80 0000	1	ADD ADDRESS TO REGISTER	2.83
ADAC	2400 0000	1	ACTIVATE DIRECT MEMORY ACCESS CHANNEL	4.00
AMI	2000 0000	2	ADD TO MEMORY IMMEDIATE	4.33
ARB	0C00 0000	1	ADD TO REGISTER AND BRANCH ON NO SIGN CHANGE	3.16–4.00
B	7082 0000	1	UNCONDITIONAL BRANCH	2.83–3.41
BC	E080 0000	1	BRANCH ON CONDITION	3.00–3.25
BBNE	3000 0000	3	BRANCH ON BIT NOT EQUAL	3.08–3.16
BFNE	8400 0000	3	BRANCH IF FLAG NOT EQUAL	4.08–4.16
BL	7480 0000	1	BRANCH AND LINK	2.75
BRRL	2800 0000	2	BRANCH RELATIVE AND LINK	3.33
CM	1000 0000	2	COMPARE MEMORY TO MEMORY	4.91–5.41
CMI	1C00 0000	2	COMPARE MEMORY IMMEDIATE	3.83–4.33
CML	1800 0000	2	COMPARE MEMORY TO LIMITS IN MEMORY	5.91–6.66
CR	C000 0000	1	COMPARE REGISTER WITH MEMORY	3.66
CRA	C080 0000	1	COMPARE REGISTER WITH EFFECTIVE ADDRESS	2.83
CRL	C400 0000	1	COMPARE REGISTER WITH MEMORY (LOGICAL)	3.66
CRLA	C480 0000	1	COMPARE REGISTER WITH EFFECTIVE ADDRESS (LOGICAL)	2.83
L	4400 0000	1	LOAD REGISTER	3.33
LA	4480 0000	1	LOAD REGISTER WITH ADDRESS	2.66
LDCR	0800 0000	3	LOAD COMMUNICATION REGISTER	4.16***
LDS	7C00 0000	1	LOAD STATUS BLOCK	4.07–5.83
LOT	5400 0000	1	LOAD ONE'S TALLY	7.75
LOTA	5480 0000	1	LOAD ONE'S TALLY OF ADDRESS	7.00
MLA	6000 0000	1	SHIFT MEMORY LEFT ARITHMETIC	3.75
MLAX	6080 0000	1	SHIFT MEMORY LEFT ARITHMETIC COUNT IN REGISTER R	3.58
MOV	1400 0000	2	MOVE MEMORY WORD	4.66
MRA	6400 0000	1	SHIFT MEMORY RIGHT ARITHMETIC	3.75
MRAX	6480 0000	1	SHIFT MEMORY RIGHT ARITHMETIC COUNT IN REGISTER R	3.58
MRR	6800 0000	1	ROTATE MEMORY RIGHT LOGICAL	3.75
MRRX	6880 0000	1	ROTATE MEMORY RIGHT LOGICAL COUNT IN REGISTER R	3.58
N	5800 0000	1	LOGICAL AND	3.58
NA	5880 0000	1	LOGICAL AND WITH ADDRESS	2.83
NOP	7007 0000	1	NO OPERATION	2.25
OR	9C00 0000	1	LOGICAL OR	3.58
ORA	9C80 0000	1	LOGICAL OR WITH ADDRESS	2.83
S	5000 0000	1	SUBTRACT FROM REGISTER	3.58
SA	5080 0000	1	SUBTRACT ADDRESS FROM REGISTER	2.83
SAT	6C00 0000	1	SHIFT AND ADD TALLY OF LEADING ZEROS	5.33–9.08
SETB	3400 0000	3	SET CRU OUTPUT BIT	2.83
SETF	8800 0000	3	SET SOFTWARE FLAG	4.33
SS	7886 0000	1	STORE STATUS BLOCK	4.25–4.83
SSB	7882 0000	1	STORE STATUS BLOCK AND BRANCH	5.25–6.41
ST	4680 0000	1	STORE REGISTER	3.58
STCR	2C00 0000	3	STORE COMMUNICATION REGISTER	7.91**
STPS	E480 0000	1	STORE PANEL SWITCHES	3.00
SXBS	7880 0000	1	STORE STATUS BLOCK, TRANSFER AND BRANCH IN SUPERVISOR MODE	5.50–6.66
SXBW	7881 0000	1	STORE STATUS BLOCK, TRANSFER AND BRANCH IN WORKER MODE	5.50–6.66
SXS	7884 0000	1	STORE STATUS BLOCK AND TRANSFER TO SUPERVISOR MODE	4.50–5.16
SXW	7885 0000	1	STORE STATUS BLOCK AND TRANSFER TO WORKER MODE	4.50–5.16
TSBX	3C00 0000	3	TEST INPUT BIT AND SWITCH MODE OR OUTPUT BIT	3.08–3.41
XBNE	3800 0000	3	SWITCH MODE ON BIT NOT EQUAL	3.08–3.33
XFNE	8000 0000	3	SWITCH MODE IF FLAG NOT EQUAL	4.08
XOR	4000 0000	1	EXCLUSIVE OR	3.58
XORA	4080 0000	1	EXCLUSIVE OR WITH EFFECTIVE ADDRESS	2.83
XS	7004 0000	1	TRANSFER TO SUPERVISOR MODE	2.50
XSB	7080 0000	1	TRANSFER TO SUPERVISOR MODE AND BRANCH	2.75–3.33
XW	7005 0000	1	TRANSFER TO WORKER MODE	2.50
XWB	7081 0000	1	TRANSFER TO WORKER MODE AND BRANCH	2.75–3.33
*B	7002 0000	1	UNCONDITIONAL BRANCH INDIRECT	3.58–4.16
*BC	E000 0000	1	BRANCH ON CONDITION INDIRECT	3.75–4.00
*BL	7400 0000	1	BRANCH INDIRECT AND LINK	3.50
*XSB	7000 0000	1	SWITCH TO SUPERVISOR MODE AND BRANCH INDIRECT	3.50–4.08
*XWB	7001 0000	1	SWITCH TO WORKER MODE AND BRANCH INDIRECT	3.50–4.08

FOR INSTRUCTIONS UTILIZING ADDRESS MODIFICATION, ADD THE FOLLOWING TIMES:
INDIRECT – 3/4 MICROSEC., INDEXED – 3/5 MICROSEC., INDIRECT AND INDEXED – 1-1/3 MICROSEC.
FOR INSTRUCTIONS INVOLVING SHIFTING, ADD 1/4 MICROSECONDS PER BIT SHIFTED.
*THE ASTERISK SYMBOL IS A PART OF THE MNEMONIC.
**ADD 250 NANOSECONDS FOR EACH EXTERNAL BIT ADDRESS.
***ADD THE TIME: (NUMBER OF BITS)/4 MICROSECONDS.

OPTIONAL INSTRUCTIONS

MNEM.	OP CODE	FORM.	NAME	EX. TIME
DAD	E800 0000	1	DOUBLE ADD	6.17
D	D000 0000	1	DIVIDE	10.42–10.92
DA	D080 0000	1	DIVIDE IMMEDIATE	9.67–10.17
DLA	C800 0000	1	SHIFT MEMORY DOUBLE LEFT ARITHMETIC	6.25
DLAX	C880 0000	1	SHIFT MEMORY DOUBLE LEFT ARITHMETIC COUNT IN REGISTER R	6.83
DRA	D400 0000	1	SHIFT MEMORY DOUBLE RIGHT ARITHMETIC	6.25
DRAX	D480 0000	1	SHIFT MEMORY DOUBLE RIGHT ARITHMETIC COUNT IN REGISTER R	6.83
DRL	D800 0000	1	SHIFT MEMORY DOUBLE RIGHT LOGICAL	6.25
DRLX	D880 0000	1	SHIFT MEMORY DOUBLE RIGHT LOGICAL COUNT IN REGISTER R	6.83
DRR	DC00 0000	1	DOUBLE RIGHT ROTATE	6.25
DRRX	DC80 0000	1	DOUBLE RIGHT ROTATE COUNT IN REGISTER R	6.83
M	CC00 0000	1	MULTIPLY	6.66
MA	CC80 0000	1	MULTIPLY IMMEDIATE	7.83
DS	EC00 0000	1	DOUBLE SUBTRACT	6.17

SAL INSTRUCTION LIST BY OP CODE

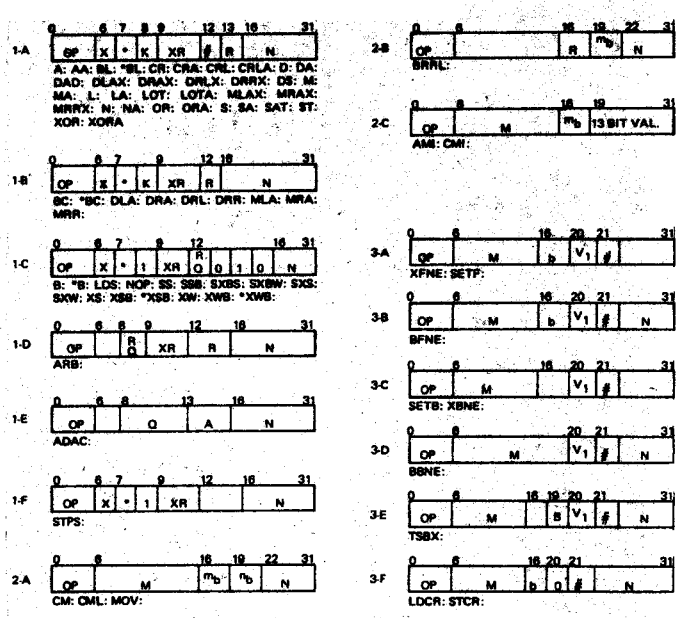
OP. CODE	MNEM.	OP. CODE	MNEM.	OP. CODE	MNEM.
0800 0000	LDCR	5080 0000	SA	7081 0000	XWB
0C00 0000	ARB	5400 0000	LOT	7082 0000	B
1000 0000	CM	5480 0000	LOTA	7400 0000	*BL
1400 0000	MOV	5800 0000	N	7480 0000	BL
1800 0000	CML	5880 0000	NA	7880 0000	SXBS
1C00 0000	CMI	5C00 0000	OR	7881 0000	SXBW
2000 0000	AMI	5C80 0000	ORA	7882 0000	SSB
2400 0000	ADAC	6000 0000	MLA	7884 0000	SXS
2800 0000	BRRL	6080 0000	MLAX	7885 0000	SXW
2C00 0000	STCR	6400 0000	MRA	7886 0000	SS
3000 0000	BBNE	6480 0000	MRAX	7C00 0000	LDS
3400 0000	SETB	6800 0000	MRR	8000 0000	XFNE
3800 0000	XBNE	6880 0000	MRRX	8400 0000	BFNE
3C00 0000	TSBX	6C00 0000	SAT	8800 0000	SETF
4000 0000	XOR	7000 0000	*XSB	C000 0000	CR
4080 0000	XORA	7001 0000	*XWB	C080 0000	CRA
4400 0000	L	7002 0000	*B	C400 0000	CRL
4480 0000	LA	7004 0000	XS	C480 0000	CRLA
4800 0000	ST	7005 0000	XW	E000 0000	*BC
4C00 0000	A	7007 0000	NOP	E080 0000	BC
4C80 0000	AA	7080 0000	XSB	E480 0000	STPS
5000 0000	S				

OPTIONAL INSTRUCTION LIST BY OP CODE

OP. CODE	MNEM.	OP. CODE	MNEM.	OP. CODE	MNEM.
C800 0000	DLA	D080 0000	DA	DC00 0000	DRR
C880 0000	DLAX	D400 0000	DRA	DC80 0000	DRRX
CC00 0000	M	D480 0000	DRAX	E800 0000	DAD
CC80 0000	MA	D800 0000	DRL	EC00 0000	DS
D000 0000	D	D880 0000	DRLX		

NOTES

INSTRUCTION FORMATS



OP – The operation code field of an instruction.
* – The bit of the instruction used to specify indirect addressing.
X – The bit of the instruction used to specify that indexing is to be done.
K – Immediate operand indicator.
XR – The field of the instruction used to specify an index register.
– The field of the instruction used to specify alternate mode registers.
R – The field of the instruction that specifies a register in the register file or specifies a shift count.
N – The field of an instruction used as an address field.
M – The field of an instruction used as an address field in two address instructions.
m_b – The field of instruction used to specify a base register to be used with the M address field.
n_b – The field of instruction used to specify a base register with an N address field.
V_1 – A bit used as an immediate value in flag and bit instructions.
b – Used to specify a flag address in a memory word or the no. of communication reg. bits.
RQ – The bit used to indicate the use of a relative address.
A – Specifies the device address in the ADAC instruction.
Q – is optional and may specify additional device address data in some ADAC instructions.
B – Specifies the value of the output bit for an equal compare on the TSBX instruction.

STATUS REGISTER

M1 MODE INDICATOR: If M1=0, execution is in Supervisor Mode. If M1=1, execution is in Worker Mode.
OI OVERFLOW INDICATOR: If OI=1, an overflow condition exists; otherwise OI is reset.
MP MEMORY PARITY ERROR INDICATOR: If MP=1, memory parity error is present.
PF POWER FAILURE: If PF=1, a power failure is indicated.
UC UNDEFINED CODE: If UC=1, an undefined operation code has been detected.
MV MEMORY VIOLATION: If MV=1, an attempt has been made to alter protected memory.
IM INDEX MODE: If IM=0, pre-indexing is performed; 1 = post indexing.
II INTERNAL INTERRUPT MASK: If 11=0, the internal interrupt is enabled.
DI DMAC INTERRUPT MASK: If DI=0, the DMAC interrupt is enabled.
CI CRU INTERRUPT MASK: If CI=0, the CRU interrupt is enabled.
CB COMPARISON INDICATORS:
If comparison is 'greater than' then Bit 10=1, otherwise Bit 10=0.
If comparison is 'equal' then Bit 11=1, otherwise Bit 11=0.
If comparison is 'less than' then Bit 12=1, otherwise Bit 12=0.

See table below for order of comparison and instructions which effect these bits.

CO CARRY OUT INDICATOR: CO=1 indicates a carry out of bit position 0 for A, AA, S, SA, SAT, and AMI instructions, otherwise CO=0.
Bits 14 and 15 are reserved for future use.

STATUS REGISTER COMPARISON INDICATORS

These status bits will be set as follows for the compare algebraic and compare logical instructions:

(REGISTER) { > / = / < } EFFECTIVE OPERAND OR ADDRESS

These bits will also be used to indicate a comparison of instruction results (as 16-bit signed two's complement quantities) with zero as follows:

(RESULT) { > / = / < } ZERO

INSTRUCTION	RESULT TESTED
L,LA	Final value loaded into the Register
ST	Final value stored into Memory
A, AA	Sum placed in the Register
S, SA	Difference placed in the Register
LOT, LOTA	Tally placed in the Register
N, NA	Result of 'AND' placed in the Register
OR, ORA	Result of 'OR' placed in the Register
XOR, XORA	Result of 'XOR' placed in the Register
SAT	Result after adding Tally placed in the Register
MLA, MLAX	Result placed in Memory after the Shift
MRA, MRAX	Result placed in Memory after the Shift
MRR, MRRX	Result placed in Memory after the Shift
ARB	Result placed in Register after the Addition
AMI	Result placed in Memory after the Addition
MOV	Value moved
STPS	Value stored in Memory from the Data Switches
STCR	Value stored in Memory from the CRU
M, MA	Most significant half of product placed in Memory
D, DA	Remainder
All Double Length Shifts, Add,Subtract	Most significant half of result placed in Memory

REGISTER FILE

REG. NUM.	SUPERVISOR REGISTER ADDR.$_{16}$	WORKER REGISTER ADDR.$_{16}$	FUNCTIONAL USE BY BIT AND FIELD MANIPULATING INSTRUCTIONS
0	80	88	GENERAL REGISTER
1	81	89	GENERAL REGISTER
2	82	8A	GENERAL REGISTER
3	83	8B	GENERAL REGISTER
4	84	8C	BASE OF MACHINE DATA
5	85	8D	BASE OF MACHINE PROCEDURES
6	86	8E	BASE OF SOFTWARE FLAG AREAS
7	87	8F	BASE OF CRU ADDRESS

FUNCTIONAL USE BY ARITHMETIC INSTRUCTIONS All registers may be used as either general arithmetic or index registers.

NOTES