Tektronix®
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4907
FILE MANAGER

SERVICE MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

This manual supports the following versions of this product: B010250 and up

MANUAL REVISION STATUS

REV.	DATE	DESCRIPTION
@	10/78	Original Issue

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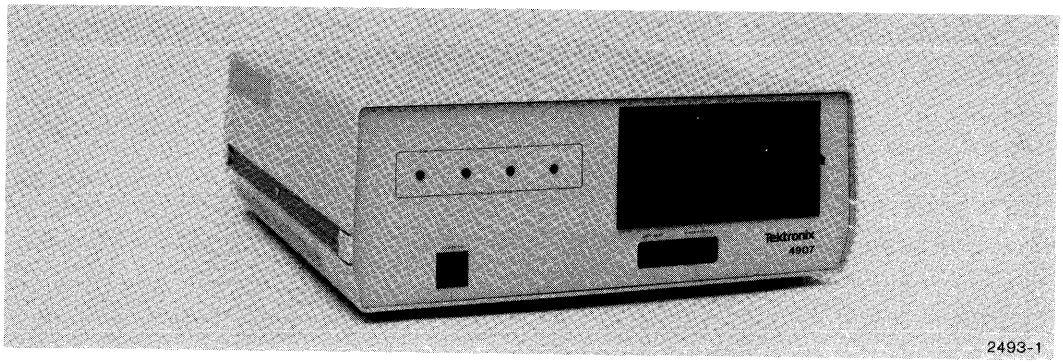
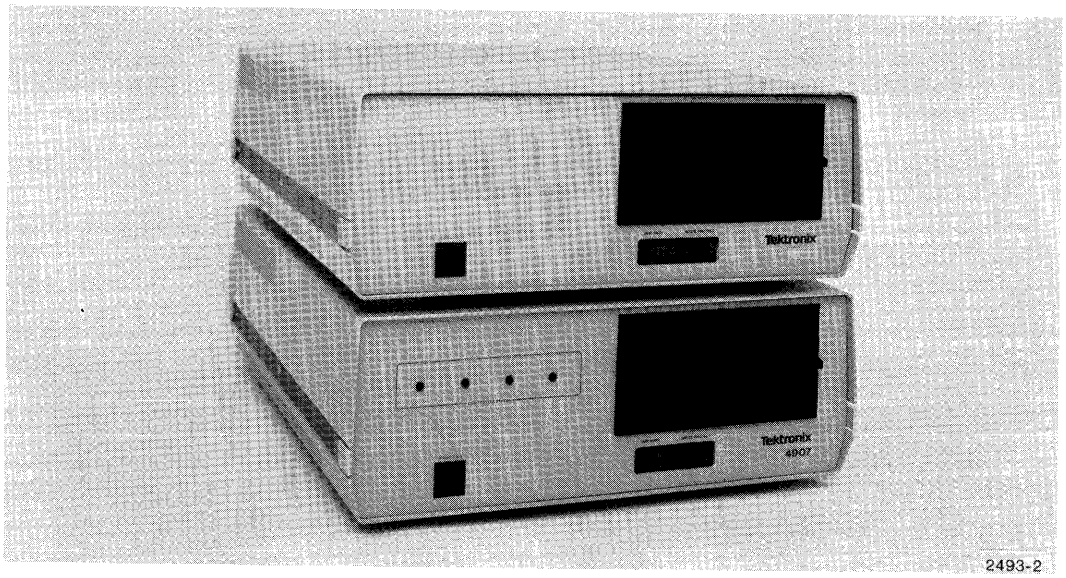
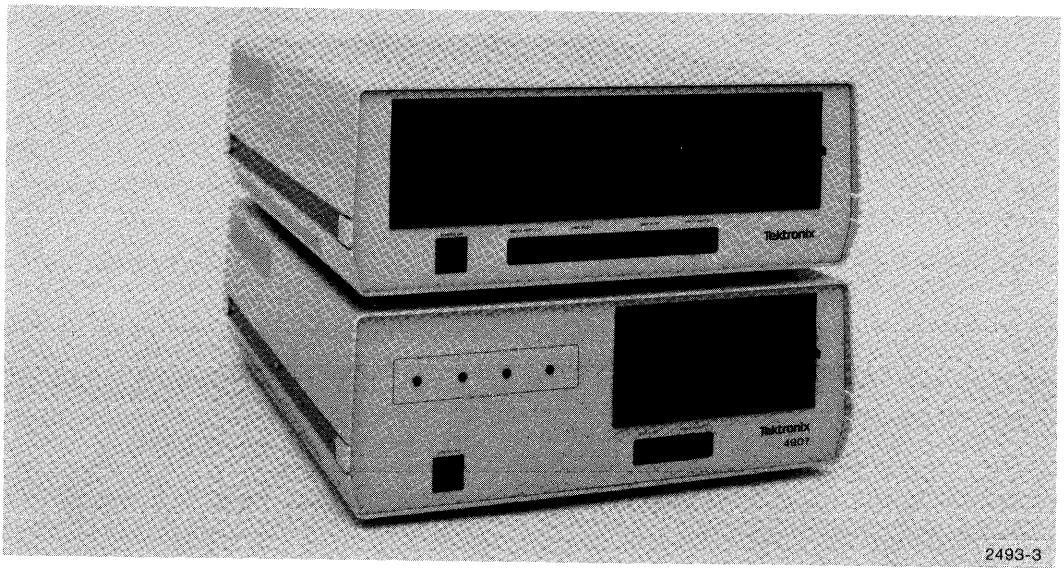


A. 4907 (Single drive).



B. Option 30 includes F30 (two drives).



C. Option 31 includes F31 (three drives).

Figure 1-1. 4907 Configurations.

Section 1

INTRODUCTION

USING THIS MANUAL

The purpose of this manual is to provide you, the service person, with information required for routine maintenance, as well as troubleshooting and repairs, of 4907 units requiring either factory or field service. This manual documents the servicing of the 4907 Main and Auxiliary Cabinets and File Manager ROM Pack.

The primary user interface to the 4907 File Manager System is a 405X Graphic System **(NOTE 1)** (or 4014, 15, 16 Terminals with Option 5). These instruments have their own Service documentation.

This manual contains preventive maintenance information, calibration and test procedures, system block diagrams, and replaceable parts lists for the 4907 Main and Auxiliary Cabinets. Detailed service information on the 405X Graphic System and 119-0977-00 Flexible Disc Drives is contained in separate documentation.

RELATED MANUALS

More detailed or supporting service information is contained in the following Tektronix manuals:

- 119-0977-00 Flexible Disc Drive Service
- 405X Graphic System Service (Vol. 1 and Vol.2)
- 4907 File Manager Operator's Manual

(1)Throughout this manual, the notation "405X" denotes any 4050-Series instrument.

- 4907 Installation Guide
- 4907 Pocket Reference Card
- 067-0746-00 System Test Fixture Manual

GENERAL DESCRIPTION

Throughout this manual the term "4907 File Manager System", or "4907 System", refers to a complete system as listed.

On the other hand, the term "4907", or "4907 File Manager", refers only to the Main Cabinet and Auxiliary Cabinet (if any).

The 4907 File Manager System consists of:

- 4907 Main Cabinet
- 405X Graphic System (or 4014, OPTION 5)
- 4907 File Manager ROM Pack
- GPIB Connecting Cable
- Flexible Disc Media

The heart of the File Manager System is the 4907 Main Cabinet containing:

- A Flexible Disc Drive
- A 6800 Microprocessor-based Controller Board
- Firmware on a ROM Board
- A Power Supply Board

The 4907 is a GPIB-compatible **(NOTE 2)** mass storage device designed as a companion for 405X Graphic Systems containing level 5, or greater, firmware. The 4907 is a direct access, flexible disc unit, with a double density recording format that provides up to 630,000 byte capacity per disc.

(2)General Purpose Interface Bus; The GPIB is defined by the IEEE 488 - 1975 standard.

NOTE

Double density recorded discs cannot be used with single density products. Neither can single density recorded discs be used with double density products.

ROMs in the 4907 and the 405X File Manager ROM Pack contain the 4907 operating system. No bootstrapping is required. The 4907 uses 405X/4907 BASIC commands and a multiple level file-by-name system to create libraries and files.

The 4907 allows open, password protected, and secret (execute only) files. Up to nine files can be open simultaneously. Programs and data may be stored and retrieved in either ASCII or Binary formats. The 4907 contains a real-time clock which must be set before the system will operate. Internal data handling is facilitated by fifteen, 256-byte buffers ("disc caches"). In addition to parity checks, a Cyclic Redundancy Checking (CRC) system is incorporated to insure greater reliability in data processing.

OPTIONAL SYSTEMS

The 4907 Auxiliary Cabinets (Options 30 and 31) contain power supply boards and additional flexible disc drives (one in the Option 30, and two in the Option 31). See Figure 1-2. An Option 5 module for the 4014 Option 40/41 allows the 4907 to communicate with a TEKTRONIX 4014 Terminal and its host computer. This option is described in the 4010-Series Option 5 GPIB Interface Instruction Manual.

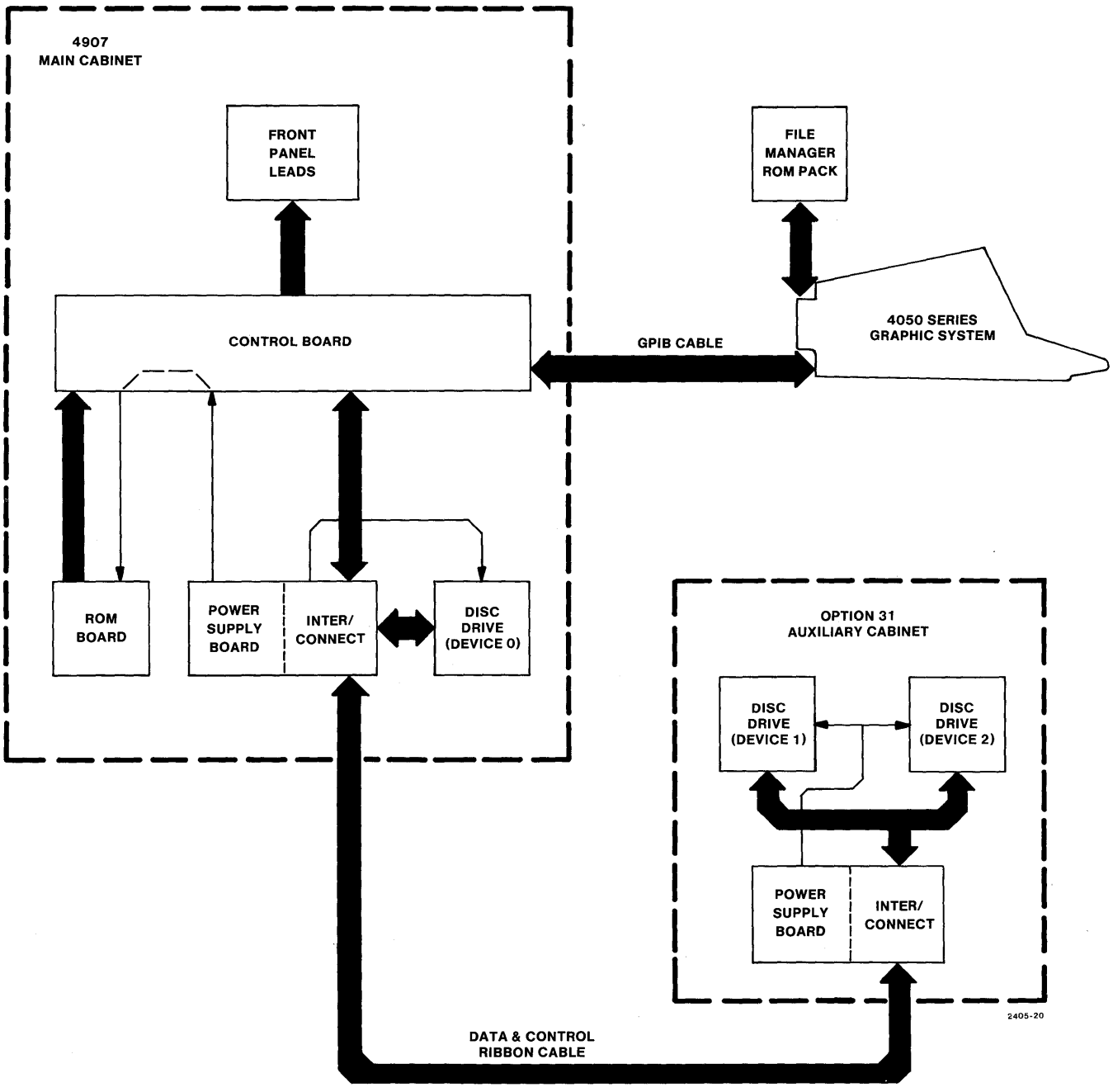
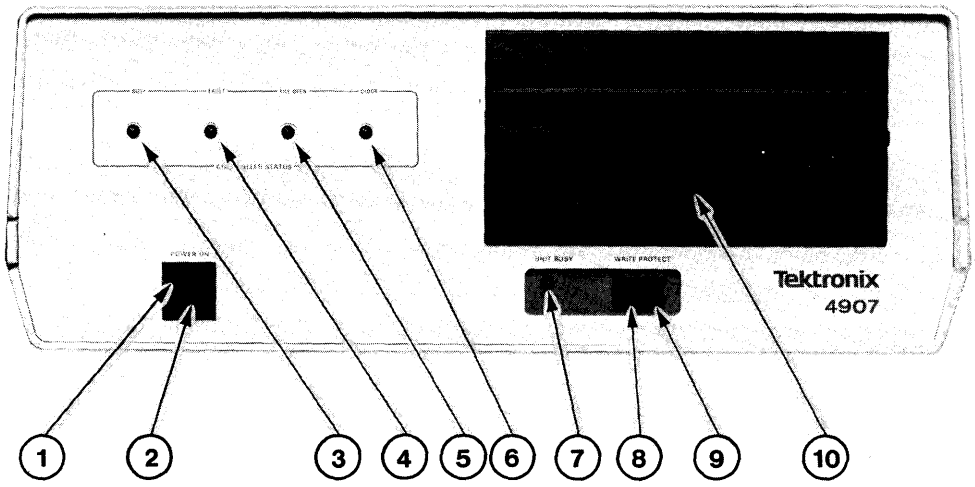


Figure 1-2. System Block Diagram.



2380-4

Figure 1-3. Controls and Indicators.

4907 SYSTEM OPERATION

Front Panel Controls and Indicators

The 4907 front panel contains the following controls and indicators (see Figure 1-3):

- Power Indicator (light in power switch).
- Power Switch (4907 Main and Auxiliary Cabinets each have separate switches).
- BUSY indicator. When lit, this LED indicates the drive is executing a data transfer or track move operation.
- FAULT indicator. If lit, the 4907 is inoperative. If power cycling fails see Section 5 (RAM Tests).
- FILE OPEN indicator. If lit, one or more files on the disc are open. (Some commands cannot be executed if files are open; see Section 5 of 4907 Operator's Manual.)

- o CLOCK indicator. Will remain lit after power up until real time clock is set.
- o BUSY indicator. If lit, a disc operation is being carried out.
- o WRITE PROTECT switch - if lit, indicates that the flexible disc media is write-protected. (Serves the same purpose as the write protect hole on the flexible disc media.)
- o WRITE PROTECT indicators. Shows that the device or disc is write protected.
- o Drive door release (contains an "activity light" whose function is replaced by the BUSY indicator).

The BUSY, FAULT, FILE OPEN, and CLOCK indicators are grouped together and referred to as CONTROLLER STATUS lights.

Basic Operating Procedures and Commands

We will now look at an abbreviated operating procedure tailored to the service person who wants to get the 4907 running. Detailed operating instructions for the 4907 are contained in the 4907 Operator's Manual.

1. Place a floppy disc in the disc drive unit (face up). If you wish to write on the disc, it should contain available writing space and opaque adhesive tape should be covering the write-protect hole.

   Observe the following special installation considerations:

2. Verify that the 405X (with the proper ROM Pack inserted), the 4907 Main Cabinet, and the Auxiliary Cabinet (if any) are all connected via GPIB or ribbon cables as indicated by Figure 1-4. (If the 4907 is used with a 4051, the 4051 must contain level 5 firmware.)

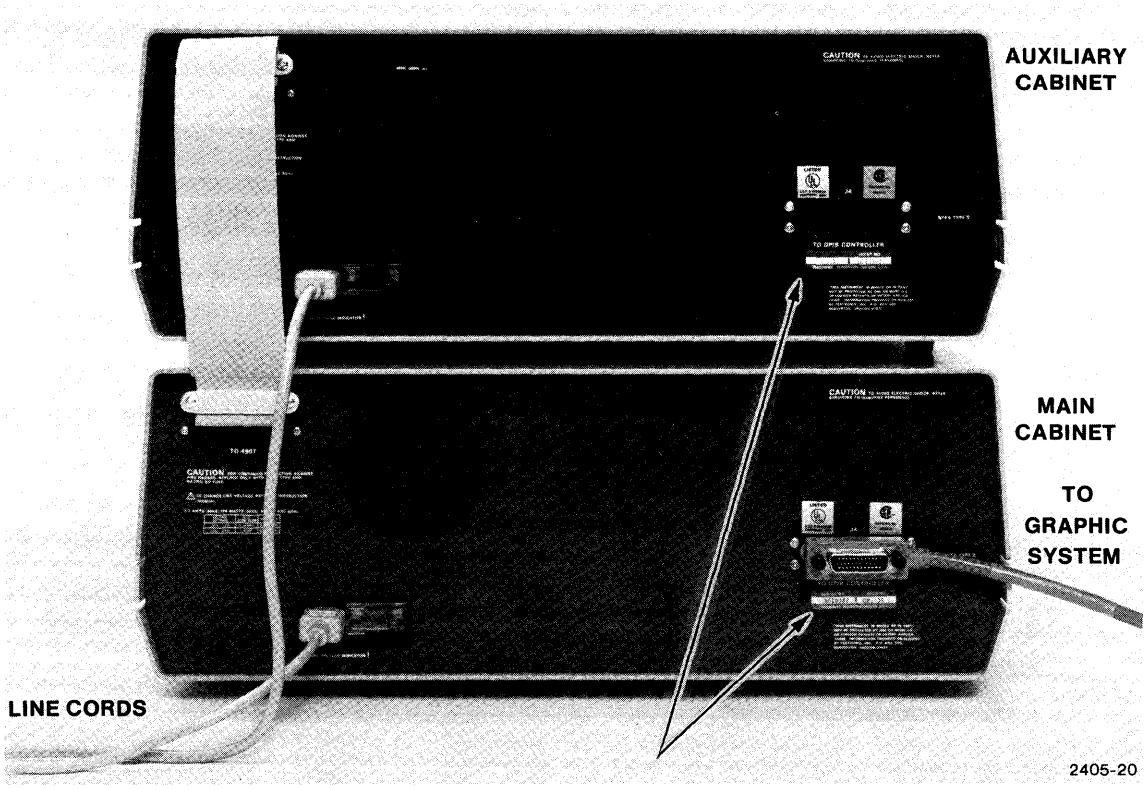


Figure 1-4. Rear Panels; OPTION 30/31 Systems.

3. Any 4662 plotter connected to the 405X Graphic System must have firmware level 3 or higher.

4. If a 405X Option 10 (Printer Interface) is used, it should be installed in the right hand slot of the backpack (device address 51). A simple mod (#33190) must also be done on the Option 10. This mod lifts pin 23 of U11 and grounds it at U21, pin 8.

5. If the File Manager ROM Pack is used with the 405X E01 ROM Expander Unit, see that the serial number of the E01 is B020199 or higher. If lower, the File Manager ROM Pack will not work in the E01, unless the E01 has been modified. Check with your Tektronix, Inc., Service Center if your E01 is numbered lower than B020199. If your E01 Expander is not modified to support the File Manager ROM Pack, install the ROM Pack in the extra ROM Pack slot on the back of the 405X.

6. With the System installed properly, power-up the 4907 Auxiliary Cabinet (if included), 4907 Main Cabinet, and 405X, in that order. The 4907 CLOCK light should be lit and all other CONTROLLER STATUS lights off.

NOTE

If several devices are connected to the GPIB, at least one more than 50% of the devices must be turned on (whether or not they are used); otherwise the bus may be loaded down by spurious SRQ signals and not operate.

The following discussion presents a simple procedure which you can use to operate the 4907. Throughout the rest of this manual, each operator entry via the 405X keyboard is indicated by bold type.

7. Type **INIT** on the 405X keyboard. This initializes the 4907 controller and is usually the first step.

8. The 4907 has a real time clock which must be set each time the system is powered-up. This is done with the **"SETTIM"** command. The correct syntax is as follows:

   CALL "SETTIM", "15-JUN-78 14:30:00"

   The month must be abbreviated to three letters. The entry in the seconds column is optional; without specifying seconds, the last colon is also omitted. Example:

   CALL "SETTIM", "15-JUN-78 14:30"

   After this command is entered, the CLOCK LED should extinguish.

9. This step and the next two relate to formatting a disc. (If your disc has been previously formatted, proceed to step 12.) Before formatting a disc, you must first "reserve" the drive unit containing that disc with a **CALL "DRES", A** statement (where "A" is the drive's address).

10. Now format the disc. The formatting procedure checks for bad blocks and prepares the disc for read/write operations.

    The CALL "FORMAT" statement is used to format the disc. This statement has the general syntax:

    CALL "FORMAT",A,A$,1,1,B$,C$,B,C,D,E,F

    Where
    A = Device Address **(NOTE 3)**
    A$ = Content or Volume I.D.
    B$ = Owner I.D.
    C$ = Password
    and B,C,D,E, and F are densities for the five levels of files.

(3)See Section 4 (Maintenance), Device (Drive) Address Selection.

A typical "FORMAT" statement might look like this:

```
CALL "FORMAT",0,"VOLUME",1,1,
 "OWNER","PASSWORD",7,7,3,3,3
```

11. Having just completed a "FORMAT" operation, the disc is already mounted for you. You need only execute a **CALL "DREL"**,A (where "A" is the drives address). This will release the drive for read/write operations.

12. If a disc is removed and reinserted, it will be necessary to remount the disc, using the CALL "MOUNT" command with syntax as follows:

```
CALL"MOUNT",A,A$
```

where "A" is the drive's address and A$ is the target string variable where the device status message is to be sent. To receive the entire 186 characters of the message the variable should be dimensioned to 200 (larger than normal 72 characters). This can be done by entering:

```
INIT
DIM A$(200)
CALL "MOUNT",0,A$
```

Then, just enter **PRINT A$** or just **A$** and press RETURN.

Transferring Data To and From the Disc

With the 4907 running and the disc mounted, you are ready to perform some diagnostic data transfers. You should first use the DIRECTORY command to see what libraries and files are already contained on the disc. (If the disc is new or just formatted there will be none.)

The following steps tell you how to use the DIRECTORY command, how to transfer data to and from the Graphic System's tape unit, and how to write and read data to/from a disc.

1. The DIR command lists the names of files stored on the disc. Its simplest form is to enter from the keyboard or under program control. This will list all programs in the "SCRATCHLIB". To get a complete disc directory without regard to libraries, type in **DIR2, "@"**. The "2" determines the amount of information on each displayed file. It can be 0, 1, or 2 with 0 giving only file names.

2. The SAVE and OLD commands are used to transfer data to/from a magnetic tape to/from the 4907's disc.

   With a disc in the 4907, now load a program into the 405X's memory from its internal tape drive. Give that program a descriptive name (say "NAME"), type **SAVE "NAME"** on the keyboard, and press **RETURN**. This places your program on the disc. To load that same program back into the 405X, type **OLD"NAME"**, and press **RETURN**. The 405X's memory will be erased and the program will be read in from the disc. Programs saved in this manner are in binary form and are put into "SCRATCHLIB", the default library. (To store programs in ASCII or libraries other than "SCRATCHLIB", refer to the 4907 Operator's Manual.)

3. If you wish to write data on a disc and then read it back, use a program similar to one of the following. These programs make use of certain commands which: CREATE a file (either RANdom or SEQuential), OPEN a file, READ or WRITE to a file on the disc, CLOSE that file, and then PRINT the contents of the file on the display screen. A full explanation of these commands is beyond the scope of this manual and is contained in the 4907 Operator's Manual. The following short example programs illustrate how to operate on random and sequential files.

OPERATING ON A SEQUENTIAL FILE

```
10 INIT
20 CREATE "SEQ";256,0
30 OPEN "SEQ";1,"F",Q$
40 WRITE#1:"ABCD",4.5,"EFGH"
50 CLOSE

60 OPEN "SEQ";1,"R",Q$
70 READ#1:A$,A,B$
80 PRINT A$,A,B$

90 CLOSE
```

OPERATING ON A RANDOM FILE

```
10 INIT
20 CREATE "RAN";1,1000
30 OPEN "RAN";1,"F",Q$
40 WRITE#1,1:"ABCD",4.5,"EFGH"
50 CLOSE
60 OPEN "RAN";1,"R",Q$
70 READ#1,1:A$,A,B$
80 PRINT A$,A,B$

90 CLOSE
```

These are the simplest possible examples of writing and reading data onto the disc. To better understand file structure and determining size requirements, refer to the 4907 Operator's Manual.

Sample Checkout Program

Here is a typical 4907 installation/checkout program. This program executes an I/O performance check plus File Status, Directory, Devices Status, and Hard Error Status for each device (drive unit) on the 4907 system. A program description precedes the actual listing.

PROGRAM DESCRIPTION

100	Initialize
120 - 160	Set System Clock if necessary
170 - 190	Enter the total number of system devices
200 - 240	Enter the device addresses **(NOTE 4)**
250	Print heading
260 - 290	Format disc
300	Create ASCII sequential file
310	Create Binary random file
320 - 370	Open each file and store message
380	Rewind sequential file
390 - 430	Access file and display message

(4)See Section 5 (Testing and Calibration) The CALL "HERRS" Diagnostic.

440 }
490 } Display each file status

500 Close both files

510 }
520 } Display d sc directory

530 }
550 } Display device (drive) status

560 }
610 } Display hard error status

620

630

SAMPLE CHECKOUT PROGRAM

```
100 INIT
110 DIM R$(2000),F$(200),G$(200)
120 CALL 'TIME',R$
130 IF LEN(R$)>0 THEN 170
140 PRINT 'ENTER DATE AND TIME (DD-MON-YY HH:MM:SS):';
150 INPUT A$
160 CALL 'SETTIME',A$
170 PRINT 'HOW MANY DEVICES ON YOUR SYSTEM?:';
180 INPUT N
190 DIM D(N)
200 LET C$='ENTER '
210 LET D$='DEVICE ADDRESSES:'
220 PRINT C$;D$;
230 INPUT D
240 FOR I=1 TO N
250 PRINT 'JJTHIS IS A SAMPLE PROGRAM FOR DEVICE ';D(I);'J'
260 CALL 'UNIT',D(I)
270 CALL 'DRES',D(I)
280 CALL 'FORMAT',D(I),'SAMPLE',1,1,'OWNER','PASS',3,3,3,3,3
290 CALL 'DREL',D(I)
300 CREATE 'ASCFILE','AUCM';3,0
310 CREATE 'BINFILE';1,256
320 OPEN 'ASCFILE';1,'F',F$
330 CALL 'TIME',R$
340 PRINT #1:'THIS IS AN ASCII SAMPLE (SEQUENTIAL FILE) FOR ';D$,D(I)
350 PRINT #1:R$
360 OPEN 'BINFILE';2,'F',G$
370 WRITE #2,1:'THIS IS A BINARY SAMPLE (RANDOM FILE)'
380 CALL 'REWIND',1
390 INPUT #1:S$,T,U$
400 PRINT S$;T
410 PRINT U$;'J'
420 READ #2,1:S$
430 PRINT S$
440 CALL 'FILE',D(I),'ASCFILE',F$
450 PRINT 'JJJTHIS IS ASCII FILE STATUSJ'
460 PRINT F$
470 CALL 'FILE',D(I),'BINFILE',G$
480 PRINT 'JJJTHIS IS BINARY FILE STATUSJ'
490 PRINT G$
500 CLOSE
510 PRINT 'JJJJJJTHIS IS THE DIRECTORYJ'
520 DIRECTORY 2,'@'
530 CALL 'DSTAT',D(I),F$
540 PRINT 'JJJTHIS IS DEVICE STATUS FOR DEVICE ';D(I);'J'
550 PRINT F$
560 CALL 'HERRS',D(I),G,J,K,P
570 PRINT 'JTHIS IS THE HARD ERROR STATUS FOR DEVICE ';D(I);'J'
580 PRINT 'NO. OF RETRIES LAST I/O',G;'J'
590 PRINT 'NO. OF ACCUMULATED RETRIES',J;'J'
600 PRINT 'NO. OF SUCCESSFUL I/O RECOVERIES',K;'J'
610 PRINT 'NO. OF UNSUCCESSFUL I/O OPERATIONS',P;'J'
620 NEXT I
630 END
```

SAMPLE PRINTOUT

```
RUN
ENTER DATE AND TIME (DD-MON-YY HH:MM:SS):15-FEB-78 10:50:00
HOW MANY DEVICES ON YOUR SYSTEM?:1
ENTER DEVICE ADDRESSES:0

THIS IS A SAMPLE PROGRAM FOR DEVICE 0

FORMAT REQUESTED, OK TO DESTROY DATA ON DEVICE  0?Y
THIS IS AN ASCII SAMPLE (SEQUENTIAL FILE) FOR DEVICE ADDRESSES:0
15-FEB-78 10:50:06

THIS IS A BINARY SAMPLE (RANDOM FILE)


THIS IS ASCII FILE STATUS

     A U C  M ATR          256 ALLOC     15-FEB-78 10:50 ALT
                            86 USED      15-FEB-78 10:50 USED
           1 OPEN            0 REC LEN   15-FEB-78 10:50 CREATED
SCRATCHLIB/A


THIS IS BINARY FILE STATUS

     B R SC N ATR          508 ALLOC     15-FEB-78 10:50 ALT
                           256 USED      15-FEB-78 10:50 USED
           1 OPEN          256 REC LEN   15-FEB-78 10:50 CREATED
SCRATCHLIB/B

THIS IS THE DIRECTORY

SCRATCHLIB/ASCFILE
     A U C  M ATR          256 ALLOC     15-FEB-78 10:50 ALT
                            86 USED      15-FEB-78 10:50 USED
           0 OPEN            0 REC LEN   15-FEB-78 10:50 CREATED
SCRATCHLIB/BINFILE
     B R SC N ATR          508 ALLOC     15-FEB-78 10:50 ALT
                           256 USED      15-FEB-78 10:50 USED
           0 OPEN          256 REC LEN   15-FEB-78 10:50 CREATED


THIS IS DEVICE STATUS FOR DEVICE 0

4907         DEV ID   SAMPLE     VOL ID   OWNER                    OWNER
  628992 FREE      630784 SIZE             0 LOST     256 BLK SIZE
15-FEB-78 10:50 FORMATTED      0 FILES OPEN


THIS IS THE HARD ERROR STATUS FOR DEVICE 0

NO. OF RETRIES LAST I/O              0

NO. OF ACCUMULATED RETRIES           0

NO. OF SUCCESSFUL I/O RECOVERIES     0

NO. OF UNSUCCESSFUL I/O OPERATIONS   0
```

Section 2

CHARACTERISTICS

4907 ELECTRICAL CHARACTERISTICS

Power Requirements

A rear panel line voltage selector matches the 4907 transformer inputs to four different line voltages. 50 Hz systems can be used by changing the pulley and belt in the disc drives. See Section 4, Maintenance. Table 2-1 shows the allowable voltages:

Table 2-1

LINE VOLTAGES

Line Voltage	Tolerance	Frequency	Fuse	Type
100 Vac	90-110 Vac		2 A Slow Blow	3 AG
120 Vac	108-132 Vac	50 or 60 Hz	2 A Slow Blow	3 AG
220 Vac	198-242 Vac		1 A Slow Blow	3 AC
240 Vac	216-264 Vac	± 1%	1 A Slow Blow	3 AC

Power Consumption

120 Vac 170 W maximum

Heat Dissipation

580 BTU/HR

Power Cord and Grounding Requirements

This instrument has a detachable three-wire cord with a three-wire polarized plug for connection to the power source and safety earth. The safety earth terminal of the plug is

directly connected to the instrument frame for electric-shock protection. Insert this plug in a mating outlet with a safety earth contact or otherwise connect the frame of the unit to a safety earth system.

WARNING

To avoid electrical shock or equipment damage, be sure to replace the cord set only with another of the same polarity.

Table 2-2

POWER CORD CONDUCTOR IDENTIFICATION

Conductor	Color	Alternate Color
Ungrounded (Line)	Brown	Black
Grounded (Neutral	Blue	White
Grounding (Earthing)	Green-Yellow	Green-Yellow

See Figure 2-1 for standard power cords. Use only these cords. (For Tektronix part numbers, see Section 9.) For use outside the USA, replace the standard plug with a plug that satisfies local authorities.

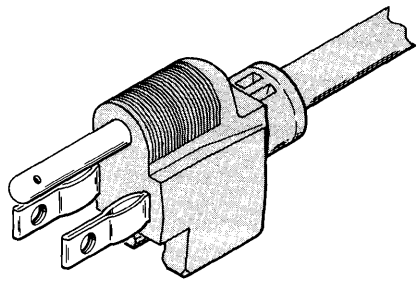
Power Supply Characteristics

Table 2-3

POWER SUPPLY

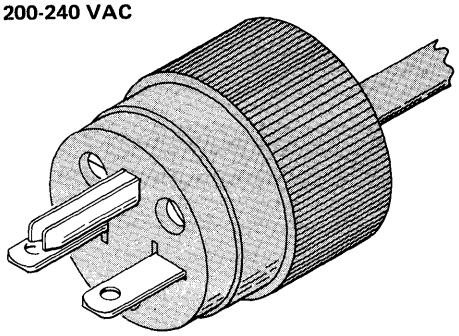
SUPPLIES	+24V	+5V	-15V
Currents:			
4907	1.30 A	3.40 A	0.08 A
Option 30	1.30	1.00	0.05
Option 31	1.30	2.00	.09
Tolerance	±5%	±5%	-12 to -21 VDC
Ripple	5.0mu	2.5mu	unregulated
Maximum Load	1.5 A	3.5 A	0.3 A
Overload Protection	>2.9 A	>4.5 A	unprotected

100-120 VAC



P/N 161-0066-00

200-240 VAC



P/N 161-0066-01

Power Cord Conductor Identification

Conductor	Color	Alternate Color
Ungrounded (Line)	Brown	Black
Grounded (Neutral)	Blue	White
Grounding (Earthing)	Green-Yellow	Green-Yellow

2131-3

Figure 2-1. USA Standard Power Cords.

ENVIRONMENTAL CHARACTERISTICS

The environmental limitations of the 4907 are detailed in Table 2-4.

CAUTION

The 4907 will require more frequent maintenance if it is operated in an extremely dusty or dirty environment. Conditions of extreme heat or cold may also damage the unit.

Table 2-4

ENVIRONMENTAL CHARACTERISTICS

	Operation	Storage (Non-Op)
Temperature	10 to 38 degrees C. (50 to 100 degrees F.)	10 to 52 degrees C. (50 to 125 degrees F.)
Altitude	Up to 10,000 feet (3,048 m)	Up to 50,000 feet (15,240 m)
Humidity	20% to 80%	8% to 80%
Vibration	The unit will not suffer damage or fail to operate when subjected to the following vibration for a period of 5 minutes along each main axis. 5 to 55 Hz at .005 in displacement	 5 to 25 Hz at .008 in displacement 25 to 55 at .005 in displacement
Shock	(Non-operating) Unit will not suffer damage or fail to operate when subjected to 3 impact shocks of 20 g's in each direction along each main axis. Shock time is 11 ± 1 ms.	

PERFORMANCE CHARACTERISTICS

Data File Storage Capacity (formatted and accessible by operator)

Per Drive (includes 256-byte directory)	630,528 bytes
Per Track	8,192 bytes
Per Sector	256 bytes

GPIB Data Transfer Rate

Burst	3,900 bytes/sec
Sustained	1,300 bytes/sec

Error Rate

Refer to DISC DRIVE UNIT CHARACTERISTICS

PHYSICAL CHARACTERISTICS

Figures 2-2 through 2-4 give the weight and dimensions of the various 4907 configurations.

DISC MEDIA CHARACTERISTICS

Type

Double-density compatible

Storage Environment

Temperature	40 degrees F to 140 degrees F (5 degrees C to 69 degrees C)
Humidity	8% to 80%

Media Lifetime

Passes per track	3.5×10^6
Insertions	>30,000

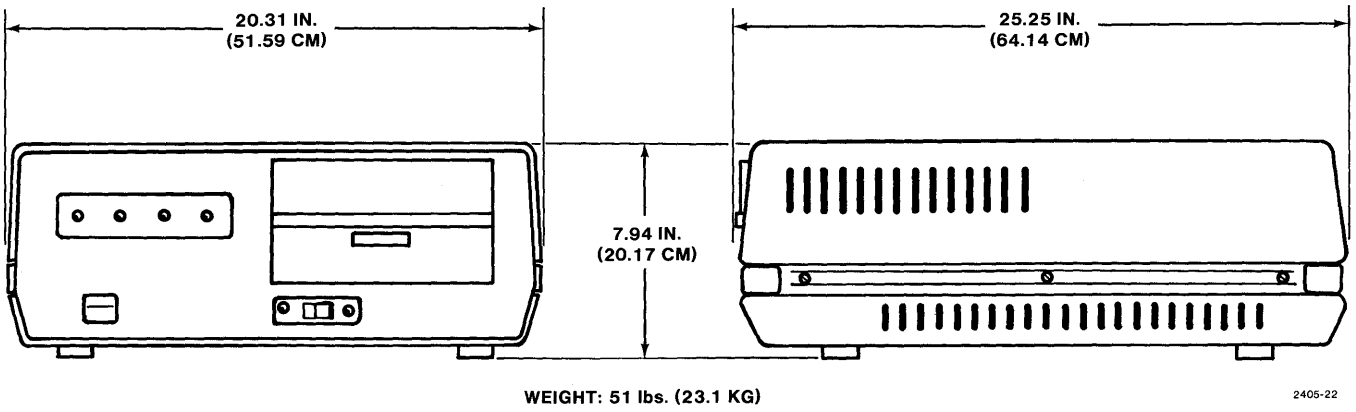


Figure 2-2. 4907, Main Cabinet.

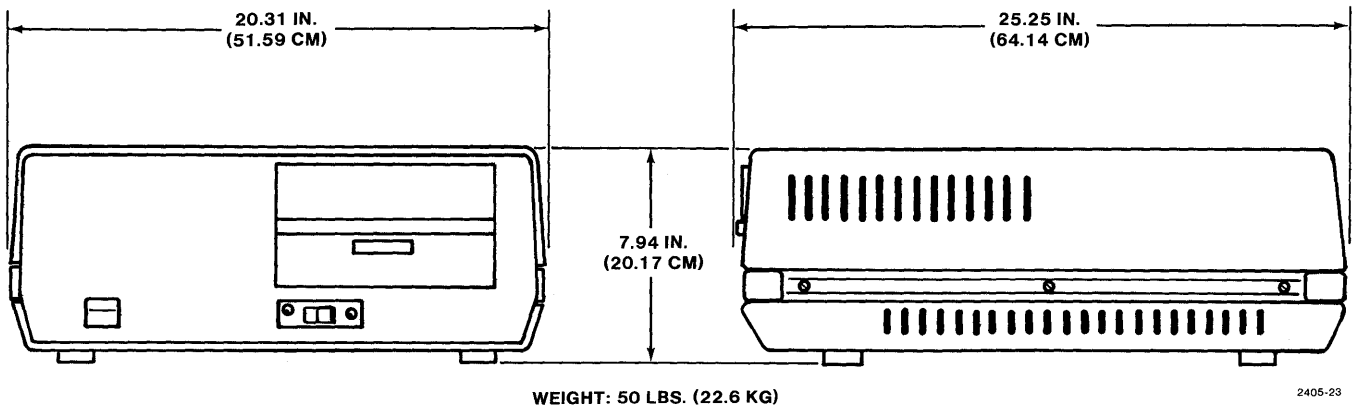


Figure 2-3. 4907 Option 30, Auxiliary Cabinet.

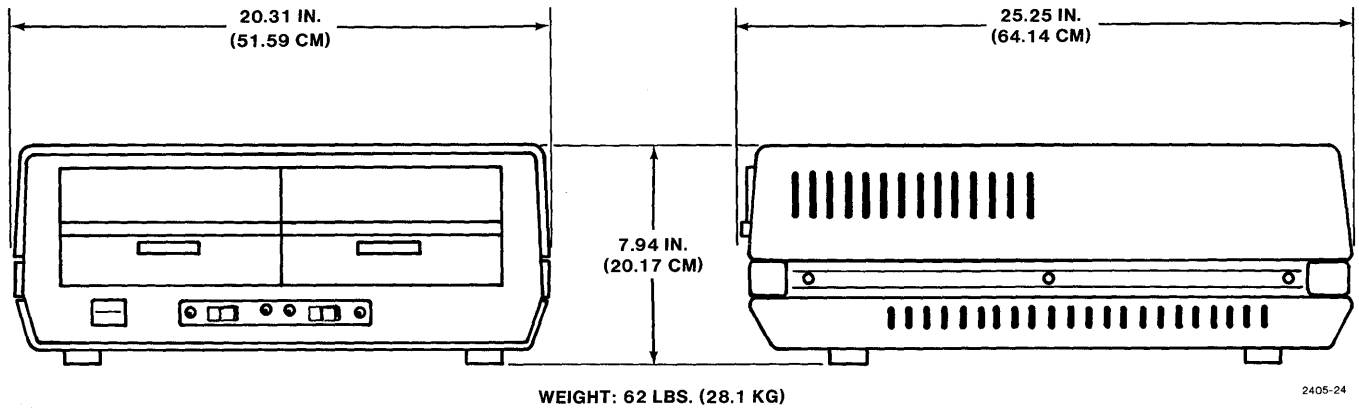


Figure 2-4. 4907 Option 31, Auxiliary Cabinet.

DISC DRIVE UNIT CHARACTERISTICS

Type

Rackmount Flexible Disc Drive, with hard sector (32), write-protect hole detect, and double-density recording.

Performance Characteristics

Capacity (Unformatted)	
Per Disc	6.4 megabits
Per Track	83.4 kilobits
Transfer Rate	500 kilobits/sec
Latency (average)	83 ms
Access Time	
Track to Track	8 ms
Average	260 ms
Settling Time	8 ms
Head Load Time	35 ms
Index Pulse Width	1.7 $\pm$ .5 ms
Index/Sector Pulse Width	.4 $\pm$ .2 ms
Error Rate	
Soft Read Errors	1 per 10^9 bits read
Hard Read Errors	1 per 10^{12} bits read
Seek Errors	1 per 10^6 seek operations

Functional Characteristics of Drive Unit

Rotational Speed	360 rpm
Recording Density (inside track)	6400 bpi
Flux Density	6400 fci
Track Density	48 tpi
Tracks	77
Physical Sectors	32
Index	1
Encoding Method	MFM (Modified Frequency Modulation)-With Write Pre-Compensation

ROM PACK CHARACTERISTICS

Dimensions

Length	4.66 in (11.84 cm)
Width	2.62 in (6.65 cm)
Depth	0.88 in (2.24 cm)
Weight	8 oz (0.23 kg)

Power Requirements (from 405X)

+5 Vdc 300 mA

Section 3

GENERAL PURPOSE INTERFACE BUS

GENERAL OPERATION

The 4907 communicates with the 405X and the outside world by means of a General Purpose Interface Bus, whose operation is defined in IEEE Standard 488-1975. This section summarizes the pertinent parts of that standard.

The GPIB is a collection of 24 wires in a common shielded cable. Eight of the wires are grounds; the other sixteen are functionally grouped into three busses: the data, management, and transfer busses. The GPIB attaches to the 4907 at rear-panel connector J 4, whose pin arrangement is shown in Figure 3-1.

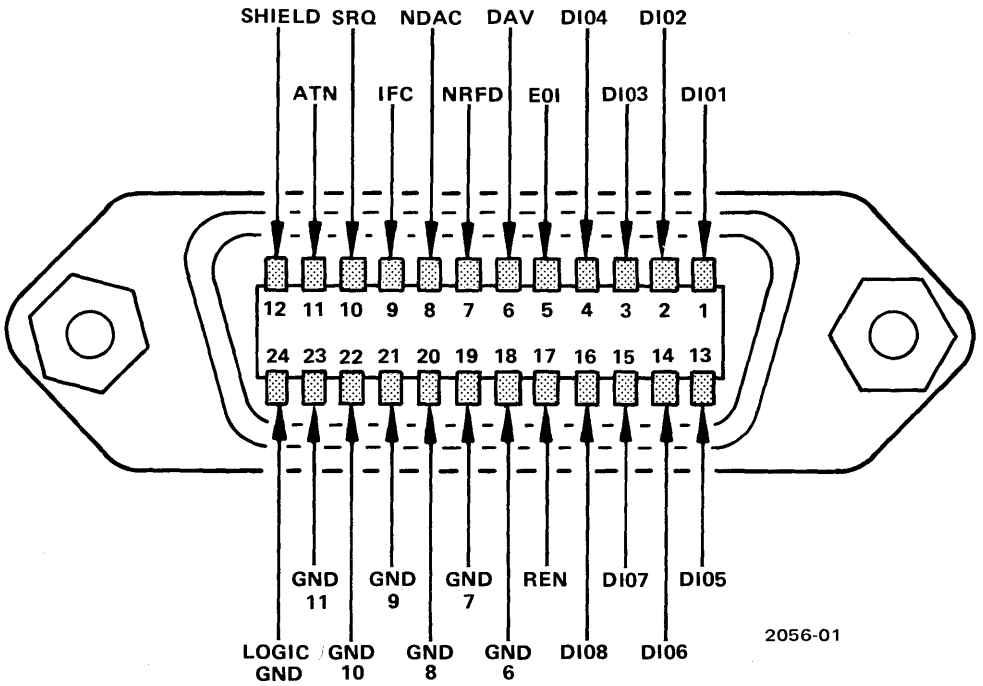


Figure 3-1. GPIB Connector.

All devices on the GPIB are connected in parallel, and all the lines of the GPIB's three busses are active low, passive high. A line is low if any device on the GPIB pulls it low (i.e., to ground) and high only if all devices let it float to a TTL high (i.e., +3.4 V); that is, the devices are connected to the GPIB lines in a "wired-OR" configuration.

Data Bus

The Data Bus contains eight bidirectional active-low signal lines. One byte of information (eight bits) is transferred over the bus at a time. DIO1 (Data In-Out bit 1) represents the least significant bit in the byte; DIO8 (Data In-Out 8) represents the most significant bit. Each byte represents a primary or secondary address, a universal command, or a data byte. (Primary and secondary addresses and universal commands are distinguished from data bytes by having the ATN line - in the management bus - activated while they are sent. With ATN asserted, certain bytes are reserved for universal commands and others for primary and secondary addresses.)

Management Bus

The Management Bus is a group of five signal lines used to control data transfers over the Data Bus. Their signal definitions are:

ATN (Attention!) — This line is activated by the controller while devices on the GPIB are being assigned as listeners and talkers. Only device addresses (primary or secondary) and control messages can be transferred over the Data Bus when ATN is active low. After ATN goes high, only the devices assigned as listeners and talkers can take part in the data transfer.

SRQ (Service Request)	The 4907 will set SRQ active low whenever an error occurs. The GPIB controller should respond to the SRQ by initiating a serial poll. The 405X will automatically handle errors from the disc via the File Manager ROM Pack - without a Software on SRQ Service Routine. **(NOTE 1)** The ROM Pack will execute a Read Error Message command and print the message on the screen; or take other appropriate action on EOF. See Appendix B (Error Messages) and Appendix D (Reference Tables) for related information.
IFC (Interface Clear)	The IFC message may be sent by the GPIB controller to put all devices on the GPIB into a known quiescent state. If the 4907 is performing some task when the controller pulls IFC active low, it interrupts that task and goes into a quiescent state, awaiting possible commands from the controller.
REN (Remote Enable)	The REN message is used in some GPIB systems to transfer devices from manual operation to operation by remote control. The 4907 **does not** respond to the REN LINE.
EOI (End or Identify)	The EOI signal can be used by the talker to indicate the end of a data transfer sequence. The talker activates EOI as the last byte of data is transmitted.

(1)4050-Series Graphic System Reference Manual

Handshake (Transfer) Bus

A handshake sequence is executed by the talker and the listeners over the handshake bus each time a byte is transferred over the data bus. The following are the definitions of the handshake bus signal lines:

NRFD (Not Ready For Data)	An active low NRFD signal indicates that one or more assigned listeners are not ready to receive the next byte. When all of the listeners for a particular data transfer have released NRFD, the NRFD line goes inactive high. This tells the talker that it may place the next byte on the data bus.
DAV (Data Valid)	The DAV line is activated by the talker shortly after placing a valid byte on the data bus. An active low DAV signal tells each listener to capture the data presented on the data bus. The talker cannot activate DAV when NRFD is active low.
NDAC (Data Not Accepted)	The NDAC signal is held active low by each listener until it has captured the byte currently presented on the data bus. When all listeners have captured the byte, NDAC goes inactive high. This notifies the talker that it may remove the byte from the data bus.

Handshake Sequence

Figure 3-2 illustrates the "handshake" sequence by which the Handshake Bus regulates the exchange of data bytes over the Data Bus.

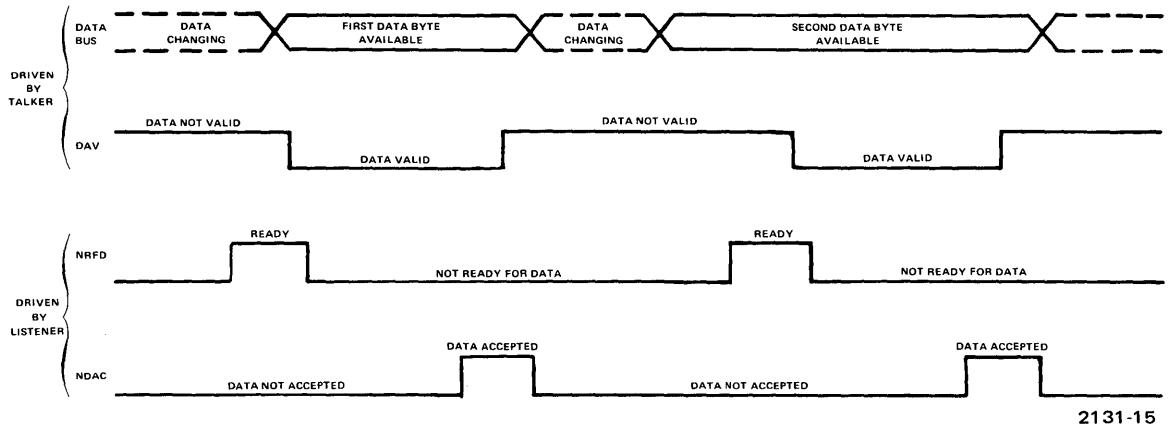


Figure 3-2. GPIB Bus Handshake Sequence.

Initially, the listeners are holding NDAC (Data Not Accepted) active low, and the talker leaves DAV (Data Valid) inactive high. One or more of the listeners may be holding NRFD (Not Ready For Data) low, indicating that it is not yet ready to accept a data byte.

When all listeners are ready for data, NRFD goes inactive high. The talker then places a data byte on the Data Bus, waits briefly for this data to settle, and then pulls DAV low, indicating to the listeners that valid data is available on the Data Bus.

The listeners capture the data. Before beginning to accept the data, each listener pulls NRFD active low, indicating that it is not ready for the talker to place another data byte on the Data bus; then it reads the data, and, having done so, releases NDAC. When the slowest listener has captured the data, NDAC goes inactive high, signaling the talker that all listeners have received the byte.

The talker then releases the DAV line and changes the data byte on the Data Bus. The listeners, sensing DAV go high, pull down NDAC, preparing for the next data byte.

4907 GPIB COMMAND CHARACTERISTICS

The 4907 and 405X communicate via three general types of GPIB commands:

1. Those that have no data associated with them.
2. Those that have data to send to the 4907.
3. Those that expect data from the 4907.

1. For those commands that have no data:

   The GPIB controller (in the 405X) sets up the 4907 as a listener. It sends the command code and command data with an EOI on the last byte, and then sends "unlisten".

2. For those commands that have data to send to the 4907: (Write and Free Write)

   The controller sets up the 4907 as a listener. It sends the 4907 a command byte, followed by logical file number and data location, and terminates by an EOI. The controller then sends the file data, terminated by an EOI accompanying the last byte. Finally, unlisten is sent to the 4907.

3. For those commands that expect file data or return messages from the 4907:

   The 4907 is set up as a listener. The controller sends the command byte and command data, if any. The controller sends the last message byte, accompanied by an EOI. The controller then addresses the 4907 as a talker (unlisten is unnecessary) and waits for information to be returned. (The controller may send "untalk" to the 4907 at anytime. This will be interpreted as the end of the current command.)

   There are several commands that may give multiple return messages. They will be terminated with the character string X'FF' accompanied by an EOI (end of messages signal).

The Free Read and Read commands will send an EOI with the last valid data byte in the file; this EOI should be interpreted as an end of file mark.

The 4907 may optionally be addressed as a talker at the end of any command. The 4907 will send an "FF" EOI when the command is completed.

The Interface Clear Line on the GPIB indicates current operation abort. The 4907 stops and returns to idle. It may take awhile in some cases (long format cannot be aborted).

The SRQ Line signals an error to the controller. The 4907 will return a status byte 64 (decimal) during serial-poll if it issued the SRQ. Decimal 65 will be sent if the error was an attempt to read past the end of a file. The 4907 will refuse all further commands except control unit disconnect or read error message, both of which will clear the error condition. Table 3-1 classifies the 4907 GPIB messages.

Table 3-1

GPIB MESSAGES CLASSIFICATION

Routine	No Data	User Data To 4907	Data From 4907				Hex Code
			User Data	One Message With EOI	Multiple Messages	Multiple Error Messages	
Status Messages:							
Control Unit Status					X		20
Device Status				X			21
Named File Status				X			22
Read Error Message				X			23
Read Error Status (Herrs)				X			24
Set Time/Date	X						25

Table 3-1 (cont)

Routine	No Data	User Data To 4907	Data From 4907				Hex Code
			User Data	One Message With EOI	Multiple Messages	Multiple Error Messages	
Read Time/Date				X			26
Device Management Messages:							
Device Format	X						40
Device Fast Format	X						41
Device Compress	X						42
Device Duplicate						X	43
Device Reserve	X						44
Device Release	X						45
Control Unit Disconnect	X						46
Device Disconnect	X						47
Initial Program Load (Read IPL)			X				48
Mark Bad Block Group Directory	X				X		49 4A
Mount				X			4B
Dismount	X						4C
File Management Messages:							
Attribute	X						60
Delete						X	61
Open File Status				X			62
Open				X			63

Table 3-1 (cont)

Routine	No Data	User Data To 4907	Data From 4907				Hex Code
			User Data	One Message With EOI	Multiple Messages	Multiple Error Messages	
Close	X						64
Block Open				X			65
Next File				X			66
Copy						X	67
Rename						X	68
File Reserve	X						69
File Release	X						6A
Space	X						6B
Read			X				80
Free Read			X				81
Write		X					82
Free Write		X					83
Type				X			84
Request Location				X			85
Relocate Pointer	X						86
Power Down Request	X						E0
Future Extended Device Commands							E1
Diagnostic Seek	X						E1

Section 4

MAINTENANCE

INTRODUCTION

This section contains recommended service procedures for the 4907 File Manager and optional units. Only qualified technicians should perform these procedures. Avoid personal injury or damage to the unit by following the steps of the service procedures. Detailed service information on the disc drive unit is also contained in the 119-0977-00 Flexible Disc Drive Instruction Manual.

INSTALLATION

The information provided here is part of the complete procedure found in the 4907 Installation Guide. This information is included in this section so you can verify that a particular unit has been properly installed. Refer to the following information on safety, voltage/frequency selection, and strapping as required. The disassembly and assembly information is in a later part of this section.

Safety Considerations

CAUTION

The 4907 is intended to be operated from a single-phase power source which has one of its current-carrying conductors (the neutral conductor) at ground (earth) potential. Operation from other power sources where both current-carrying conductors are live with respect to ground (such as phase-to-phase on a multi-phase system, or across the legs of a 117-234 V single-phase three-wire system) is not recommended.

The 4907 has a three-wire power cord with a three-terminal polarized plug for connection to the power source. The grounding terminal of the plug is directly connected to the

instrument frame as recommended by national and international safety codes. See Figure 2-1 for power cord and plug information.

Line Voltage and Frequency Considerations

The 4907 operates on 100, 120, 220 or 240 volt power sources. Only 120 volt operation is recommended in the U.S.A. The voltage setting for your particular 4907 may be seen through the plastic viewport in the rear of the cabinet. This voltage is printed on the voltage selector card, located just under the fuse in the Line Selector/Filter unit.

When changing the power source it is necessary to remove and reorient this voltage selector card. The procedure is as follows:

1. Remove power cord.
2. Move the sliding viewport to the left.
3. Remove the fuse by pulling out lever marked FUSE PULL (Figure 4-1).

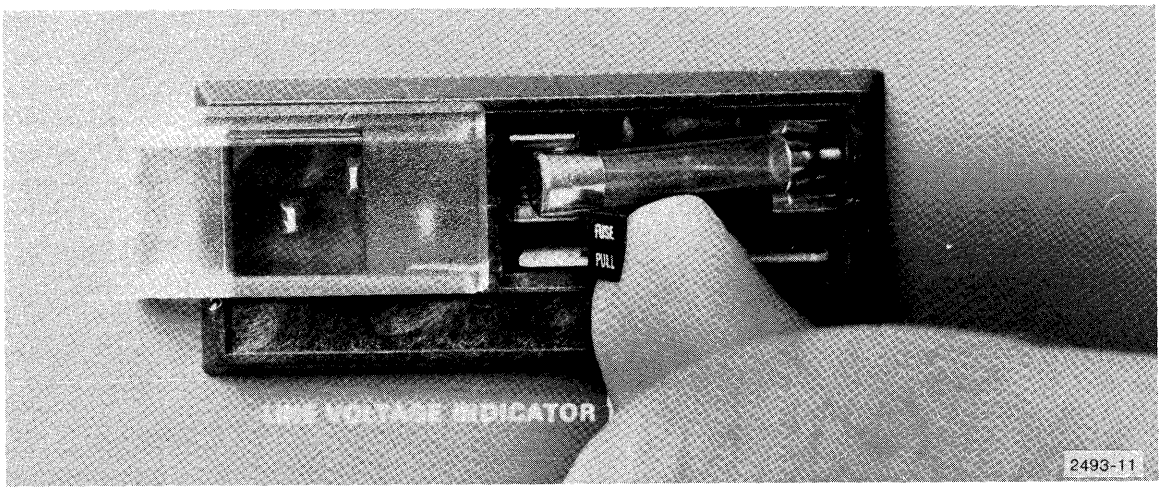


Figure 4-1. Removing Main Fuse.

4. Remove the line voltage selector card using pliers or a pointed object (Figure 4-2).

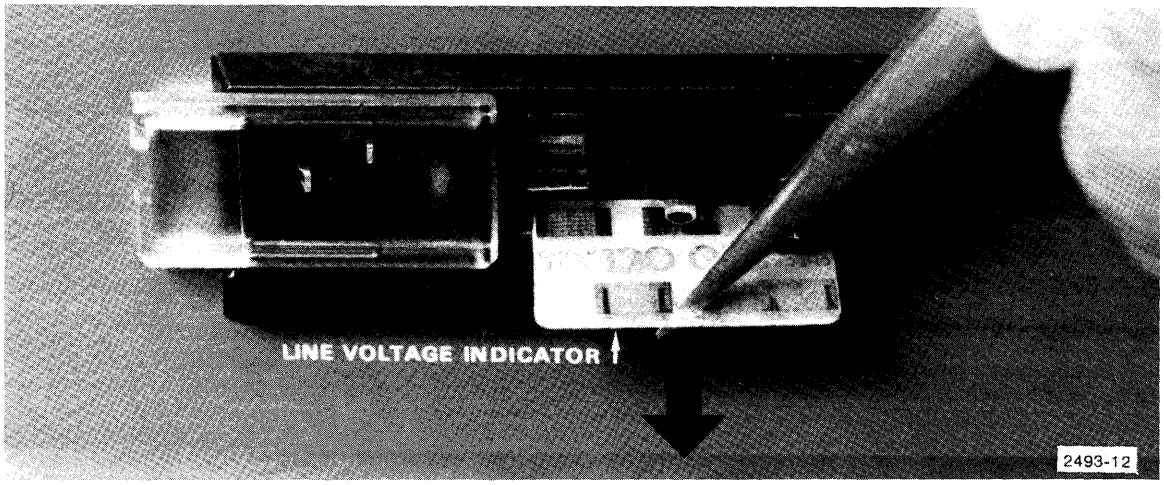


Figure 4-2. Removing Line Voltage Selector Card.

5. Turn the card over and/or end-for-end, so only the line voltage desired may be read after the card is inserted and the viewport closed. Insert card and close viewport.

NOTE

When the line voltage is changed to 50 Hz from the normal 60 Hz, it is also necessary to change a pulley and drive belt in the disc drive unit. See 119-0977-00 Disc Drive Service Manual for details.

GPIB Address Selection

The GPIB address selector switch is located near the GPIB cable jack on the rear end of the Control Board. See Figure 4-3. Normally, the 4907 is connected via the GPIB to a 405X only. In this case the 4907 GPIB address selector switch must be set to address 0. This means the rocker switches must be depressed toward the numbers on the board, and away from "OPEN" printed on the GPIB address selector switch. (Switch element #6 is not used.)

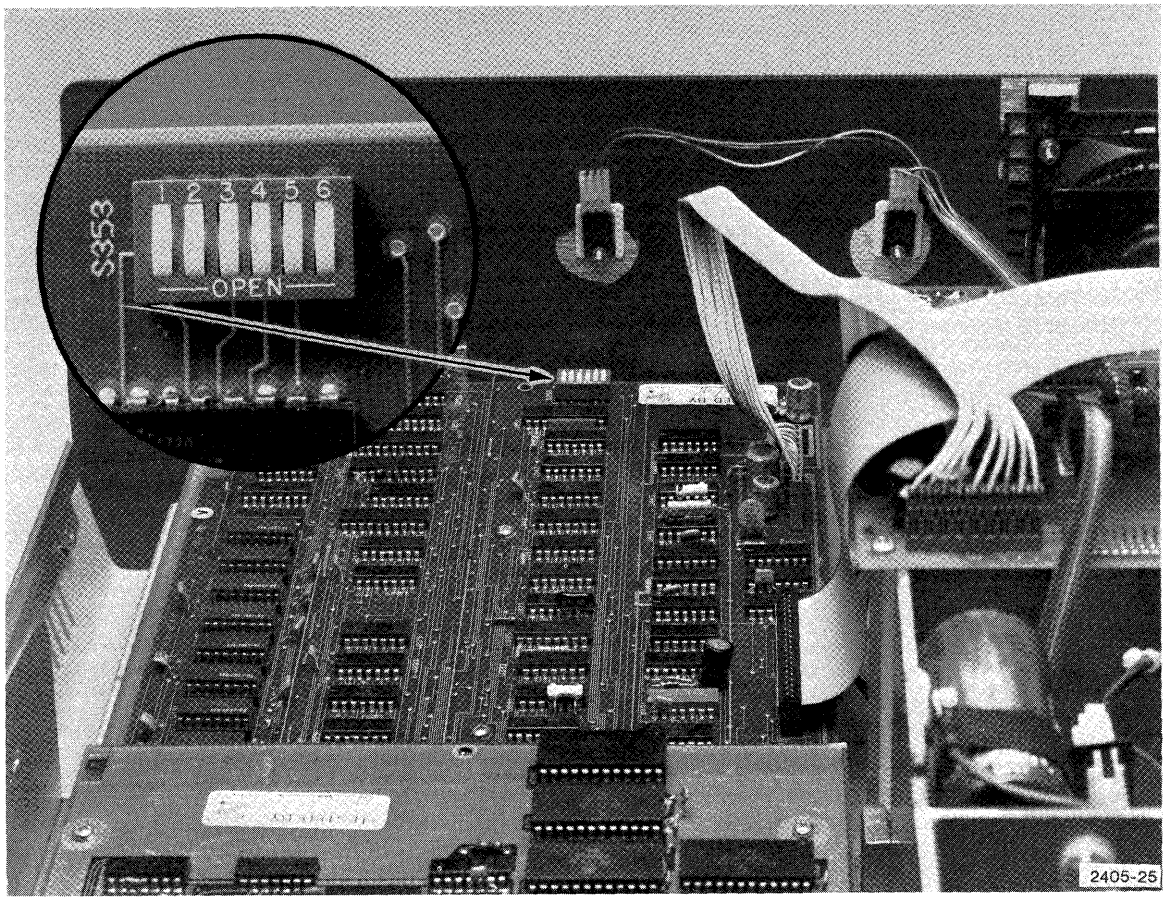


Figure 4-3. GPIB Address Switch.

If the 4907 is to be used on some other type of GPIB system, refer to that system documentation for the 4907's new GPIB address; then set this switch accordingly.

Device (Drive) Address Selection

The address of any device (disc drive) in the 4907 can be specified as an integer from 0 to 3. The address is determined by the location of the address straps on the circuit board of the disc drive. The factory-set address strapping for each 4907 configuration is shown below (Table 4-1).

Table 4-1

DEVICE ADDRESS STRAPS

Device	Device Address	Address Straps
4907 (single drive)	0	DS1 and T1
4907 Opt. 30 (2 drives)		
Main Cabinet Drive	0	DS1 and T1
Aux. Cabinet Drive	1	DS2 and T1
4907 Opt. 31 (3 drives)		
Main Cabinet Drive	0	DS1 and T1
Aux. Cabinet left Drive	1	DS2 and T1
Aux. Cabinet right Drive	2	DS3 and T1

If an address in one of the devices must be changed, the address strapping must be altered.

To change the Device Address:

1. See Bottom Cover Panel Removal and Replacement (part of Disassembly/Assembly and Component Replacement, later in this section). Place the cabinet on its back and remove bottom cover panel accordingly. This exposes the underside of the disc drive board.

2. Locate the jumper straps labeled DS1 (Drive Select 1), DS2, DS3, DS4, (see Figure 4-4). The strap that is jumpered is the device address plus one. As illustrated, a jumper on DS1 gives that drive a device address of 0.

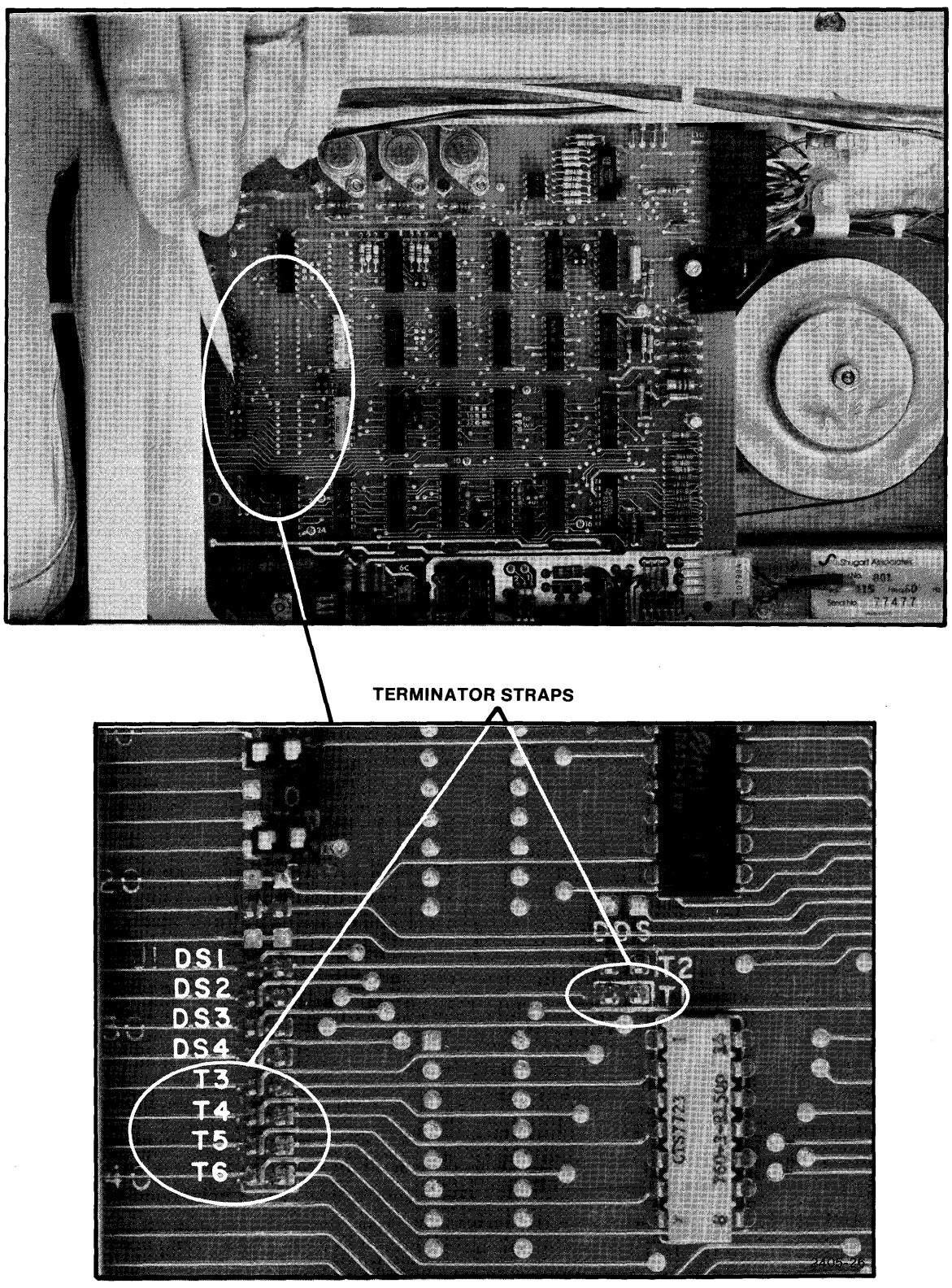


Figure 4-4. Drive Address Strap Location.

3. Observe the device addresses (see front panel address labels) and verify that each drive is strapped accordingly. Since it is easy to change device addresses to suit the preference of the individual user, you may find 4907 systems with configurations different than the factory settings. For instance, you could find Option 31s addressed 0, 2, 1; 1,3,2; etc.

4. Notice the resistor termination straps T1 and T2, and T3 through T6. See Figure 4-4. T2 is always strapped. T1 and T3 through T6 are strapped only for the device the farthest cable distance away from the Main Cabinet Connector J1. In an Option 31, the farthest device is the top left drive unit (indicated by shading in Figure 4-5).

5. Check all address and termination straps, and front panel address labels, before replacing bottom cabinet covers.

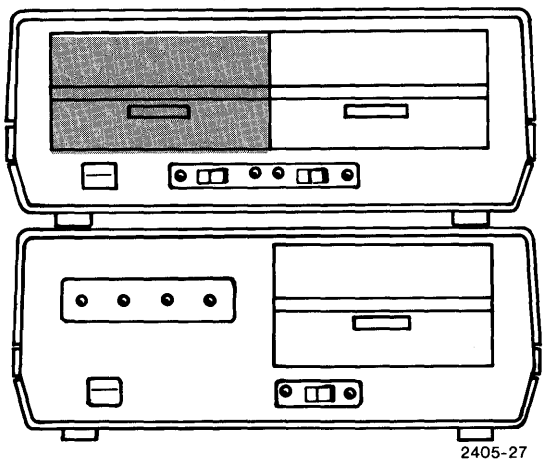


Figure 4-5. Drive Unit With Terminators (Indicated by Shading).

ROUTINE MAINTENANCE

The 4907 and auxiliary cabinets are designed to require a minimum of maintenance and servicing. Once a year you should give the unit(s) a general inspection, looking for loose

screws, connectors, and switches. Observe and clean any accumulated dust. Inspect fan motor shaft play for excessive wear.

CAUTION

Do not attempt to oil any of the three motors in your unit. These motors have sealed bearings and therefore do not require lubrication.

As a general rule, the 4907 does not require lubrication of any bearings or spindles, and any oil added will only catch dust and create greater wear problems.

Table 4-2 below is a routine maintenance schedule for the flexible disc drive units. This schedule is also included in the 4907 Operator's Manual. Procedures 1 and 2 may be performed by the operator. Procedures 3 through 6 are the responsibility of a technician and are fully described in the 119-0977-00 Flexible Disc Drive Instruction Manual.

Table 4-2

DISC DRIVE UNIT MAINTENANCE SCHEDULE

Procedure	Item	Inspect For	Interval	Action Required
1	Read/write head	Oxide buildup resulting in repeated hard or soft error	12 months	Clean read/write head
2	Read/write head	Worn felt	12 months	Replace button
3	Stepper motor and lead screw	Nicks, burrs, and dirt	12 months	Clean off oil, dust, and dirt. Dress down nicks or burrs, or replace part.
4	Belt	Frayed or weak areas	12 months	Replace

Table 4-2 (cont)

Procedure	Item	Inspect For	Interval	Action Required
5	Base	Loose screws, switches, and connectors.	12 months	Tighten serews, connectors, and switches.
		Check for dust and dirt.		Clean off dust and dirt.
6	Read/Write head	Aborted I/O commands or distorted results.	12 months	Align head. (See Section 5 Testing and Calibration.)

Fuse Replacement

If power is absent after you turn on the power switch, check the main power fuse. Its value is indicated in Table 2-1 (Characteristics). The main power fuse is located in the filter/power cord connector unit on the rear panel of main and auxiliary cabinets. The fuse is just above the voltage selector and behind a sliding plastic viewport.

1. Remove power cable.
2. Move the viewport to the left.
3. Remove the fuse by pulling out lever marked FUSE PULL. Refer back to Figure 4-1.

A +5 volt power loss could mean fuse F163 on the power supply board needs replacing. Remove cabinet cover and look under ribbon cable connecting controller and power boards for this fuse. F163 is a 3AG, 7.5 amp at 32 volts. (This fuse is shown in Figure 5-4.)

Read/Write Head Cleaning

The Read/Write head should be cleaned after each 12 months of normal use. The procedure is as follows:

1. Remove power cable.

2. Remove top cover of cabinet.

3. Use a cotton swab and denatured alcohol to remove accumulated oxide from the head (Figure 4-6).

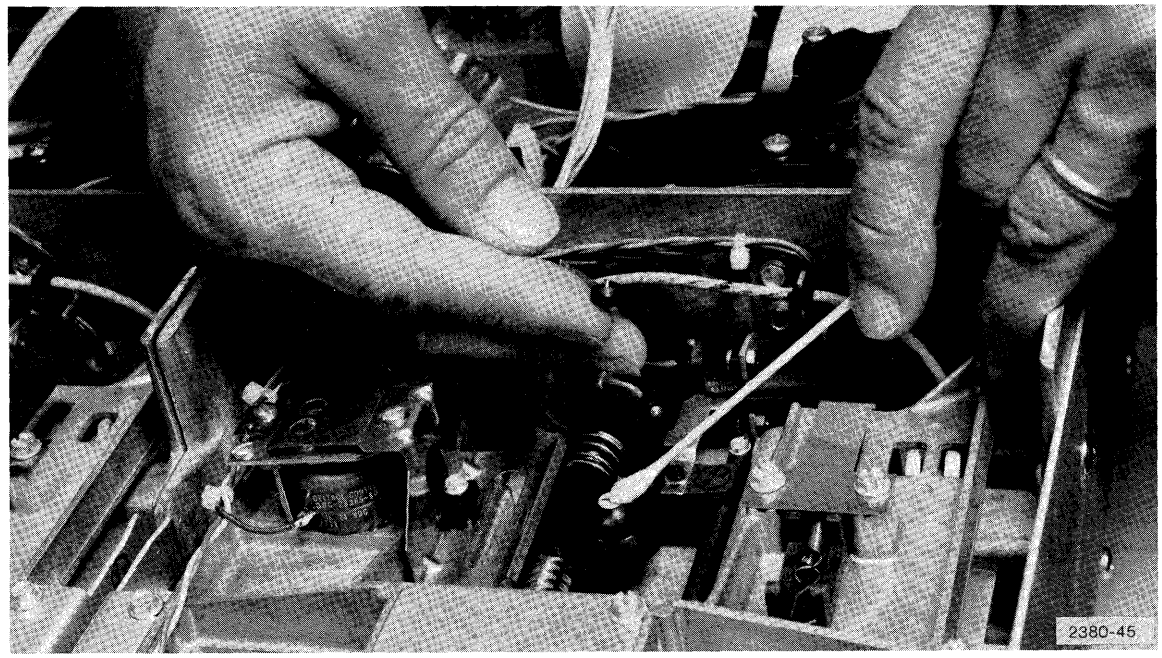


Figure 4-6. Cleaning Read/Write Head.

NOTE

The head should not require frequent cleaning. Clean once a year, as necessary.

CAUTION

(Observe when cleaning head or replacing load button.) To prevent possible damage to the torsion spring, the load arm should never be opened over 90 degrees from the carriage assembly, or while at track 00.

Read/Write Head Load Button

The Read/Write head load button should be replaced after 12 months of normal use.

1. With cabinet cover removed, grasp the load button arm with one hand and hold the arm away from the head.

2. Using needle nose pliers, squeeze together the locking tabs on button, while pushing the button out the bottom of the arm (Figure 4-7).

3. Check the felt on the new load button to see that it is firmly attached and in good condition (Figure 4-8).

4. Then install button by pressing it into the arm from the head side. It will snap into place.

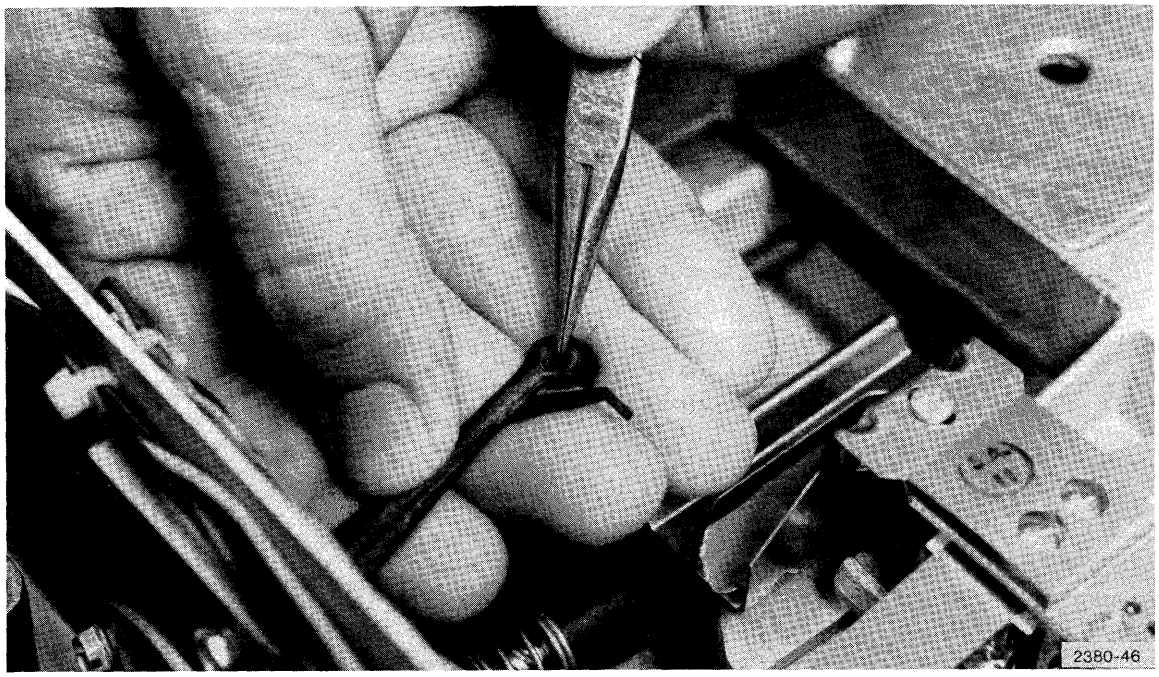


Figure 4-7. Removing Head Load Button.

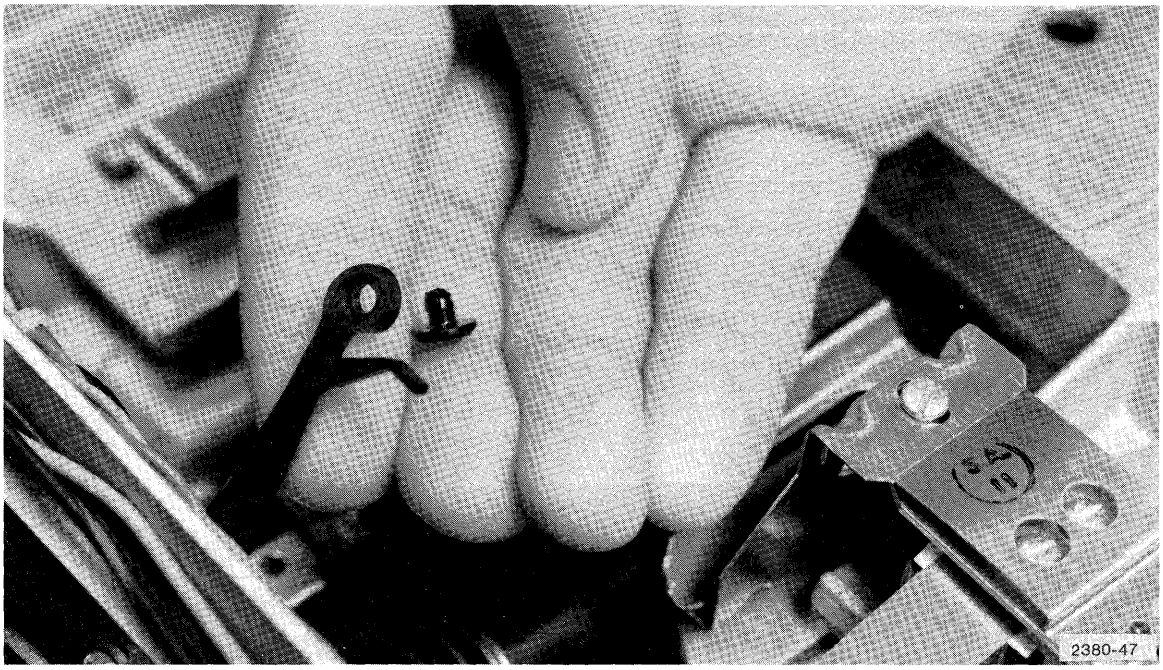


Figure 4-8. Inspecting New Load Button.

Disc Belts and Motors

The maintenance procedure for the Drive Unit Stepper Motor and Lead Screw is as follows:

1. Once a year, clean off all oil, dust and dirt.
2. Inspect for nicks and burrs.

Once a year the drive belt should be inspected for frayed or weakened areas. To give the belt a thorough inspection, use the following procedure:

1. Remove the drive unit from the cabinet. (See Disc Drive Unit Removal discussion later in this section.)
2. Then lay the drive upside down, and remove its circuit board and connected wires and cables that might interfere.

3. Now you have clear access to the belt and both pulleys. Inspect the belt for frayed or weakened areas. Replace the belt, if necessary. (See Figure 4-9.)

4. Replace the Disc Drive Unit, after properly installing its circuit board.

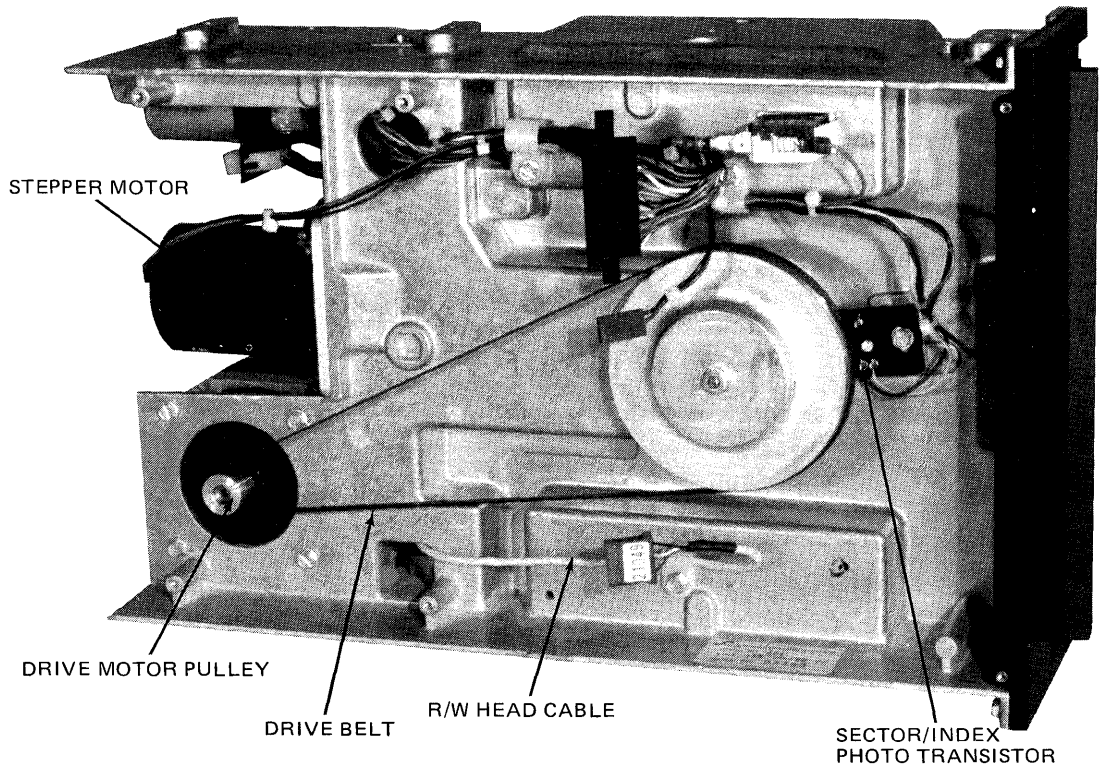


Figure 4-9. Inspecting Drive Belt.

DISASSEMBLY/ASSEMBLY AND COMPONENT REPLACEMENT

Top Cover Panel Removal and Replacement

WARNING

The 4907 main cabinet and F30, F31 auxiliary cabinets are not equipped with safety interlock switches. Therefore you should disconnect the power cord before removing either the top or bottom cover panel. If power is required to perform tests or calibration with panels removed, exercise due caution at all times.

1. To remove the top cover, unscrew the three screws located in the channels on each side of the cabinet cover.
2. Lift the cover off.
3. Replacement is simply the reverse procedure; however, care should be exercised to orient the cover with the vent holes toward the front of the cabinet. This is necessary for proper cooling.

Bottom Cover Panel Removal and Replacement

1. Turn cabinet over and carefully place it on a soft cloth.
2. Remove ten bottom screws, then lift off base (Figure 4-10). Do not remove feet.

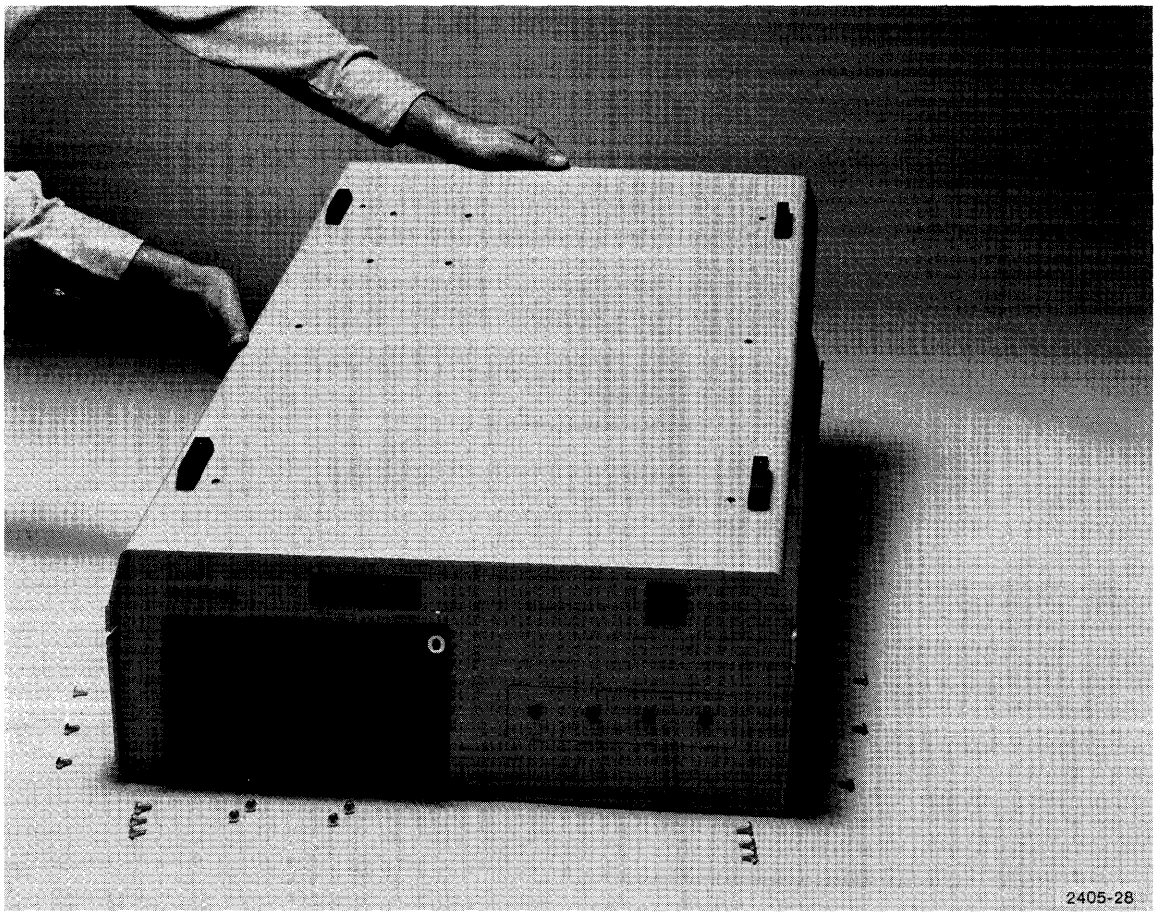


Figure 4-10. Removing Bottom Panel.

Disc Drive Unit

Disc Drive Unit Removal

1. Remove top cover panel (see first part of this section).

2. Disconnect 3 prong AC power plug P4 from connector J4.

3. Disconnect 6 prong DC power plug P5 from connector J5.

4. Disconnect signal interface harmonica plug P1 from connector J1.

5. Loosen fork/clamp holding drive to chassis (Figure 4-11).

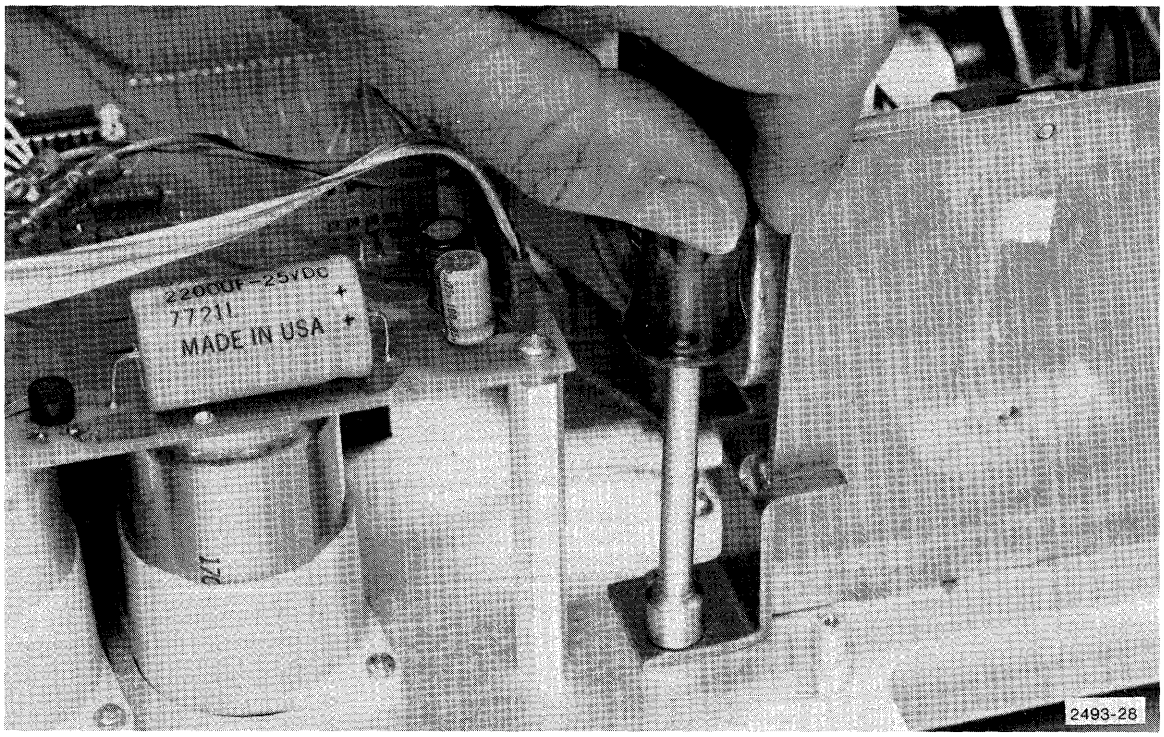


Figure 4-11. Loosening Drive Unit Fork/Clamp.

6. Remove the two posidrive screws from the side of drive unit.

7. Place cabinet top down on a soft cloth.

8. Reach under the drive and support with one hand while removing the four bottom screws from the cabinet and drive (Figure 4-12). This prevents the drive from dropping sharply onto the work surface.

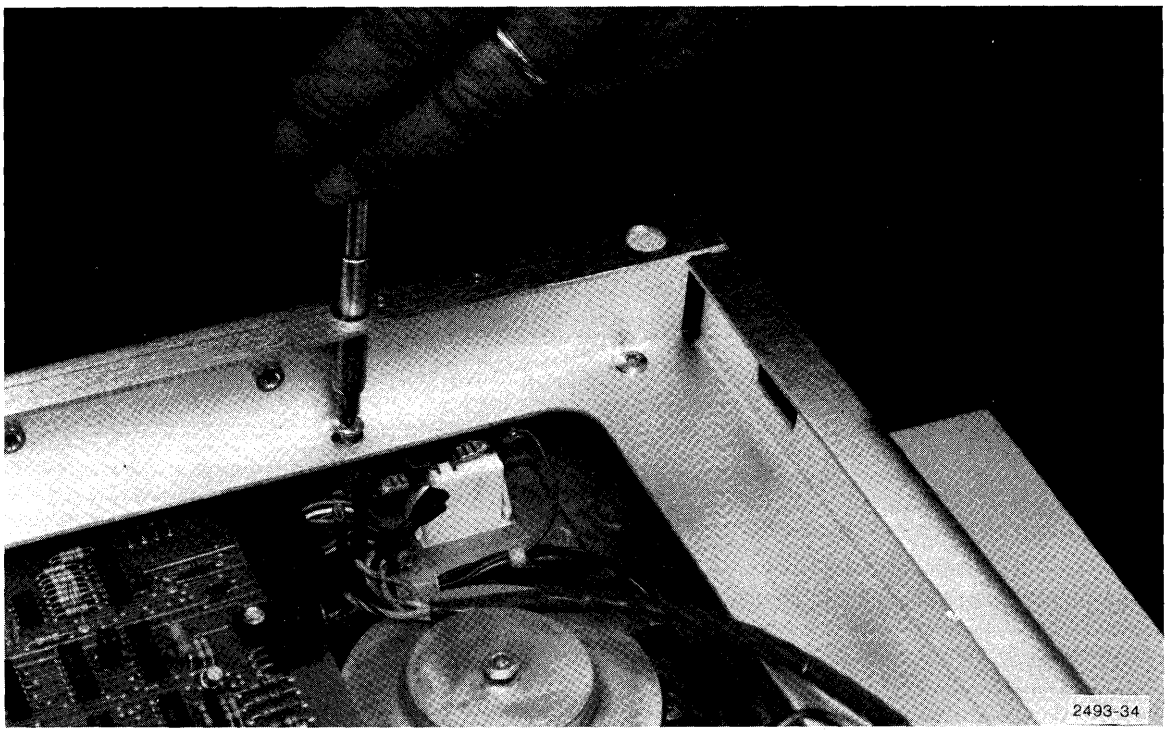


Figure 4-12. Removing Bottom Drive.

9. Let the drive settle gently onto the cloth on your workbench.

10. Now raise the cabinet, rear first, up and away from the free drive unit.

Disc Drive Replacement

Before installing a new drive unit, read the section of text immediately following this (119-0977-00 Internal Straps and Modifications). Be sure all straps are properly jumpered and all circuit mods in place.

1. To replace a drive unit, place it on its back as before and bring the main cabinet down carefully on the top of it.

2. Lift up under the drive, and slide it forward into the door hole (in front of the cabinet).

3. While holding the drive in position with one hand, replace the rear side mounting screw. Then replace the four bottom screws and the remaining side screw.

4. Reconnect plugs to J1, J4, and J5.

5. Check to see that the drive address is correctly strapped, as indicated in the Installation section (Drive Address Selection).

119-0977-00 Internal Straps and Modifications

In addition to the address strap settings, the following internal jumper strap settings are required for the 119-0977-00 Flexible Disc Drive when used in a 4907 Main or Auxiliary Cabinet. These internal straps and some component addition modifications are indicated in Figure 4-13. Table 4-3 indicates which straps are to have jumpers installed and those with jumpers removed. Be sure these straps and modifications are in place before you replace a new drive unit.

Disc Drive Parts Replacement

Complete parts replacement procedures for the drive unit parts are found in the 119-0977 Disc Drive Service manual. (For head load button replacement see the routine maintenance discussion earlier in this section.)

Table 4-3

DRIVE UNIT INTERNAL STRAPS

Jumper Installed	Jumper Removed
T2	HL
DS	Z
C	X
DC	800
A	L
B	Y
801	D

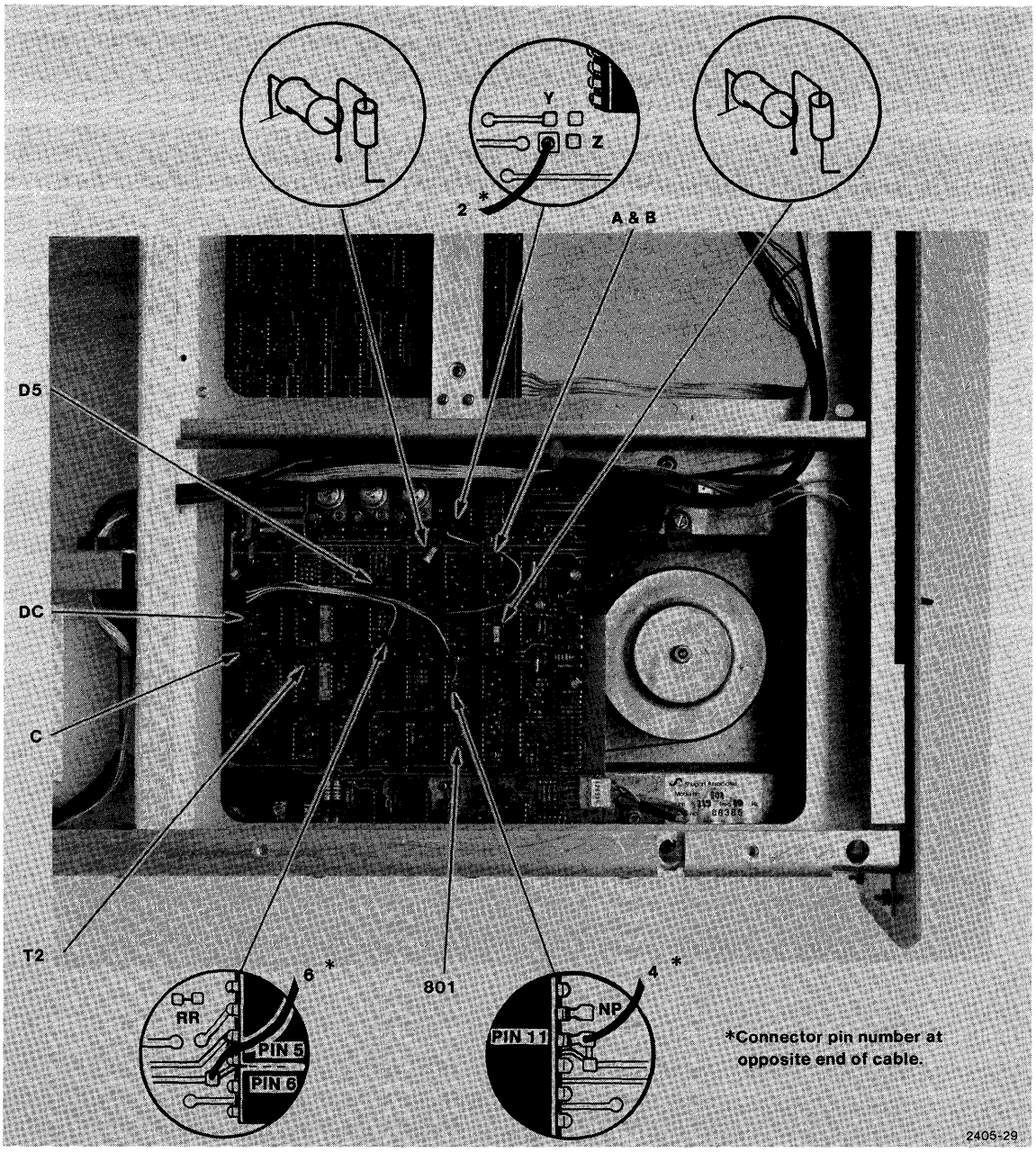


Figure 4-13. Disc Drive Board Straps and Wiring Modifications.

Removing Boards and Connectors

ROM Board

Replacement of certain power supply components and control board parts and straps necessitate removal of the ROM and Power Supply Boards. For instance, the controller address straps, J107 and J213, can be accessed only by removing the ROM board. Likewise, to replace the clock crystal, microprocessor, and other chips, you must remove the ROM board. Four screws hold the ROM board in place, and once these screws are removed, the board can be easily set aside with the ribbon cable still connected to the control board. This allows you to perform certain logic checks.

CAUTION

Put some insulating cloth around the ROM board to prevent contact with the case or components that could cause devastating shorts.

If for any reason the ribbon cable connector is removed from the ROM board, or any board, be sure to replace it correctly. It is possible to shift a connector one pin to the right or left of its proper location when replacing it. Avoid this problem and connector end swapping by rechecking connector positions as you replace them. (See Figure 4-14.) The red indexing stripe on one edge of each ribbon cable should be oriented as indicated in the cabling diagrams, Figures 8-1 through 8-4.

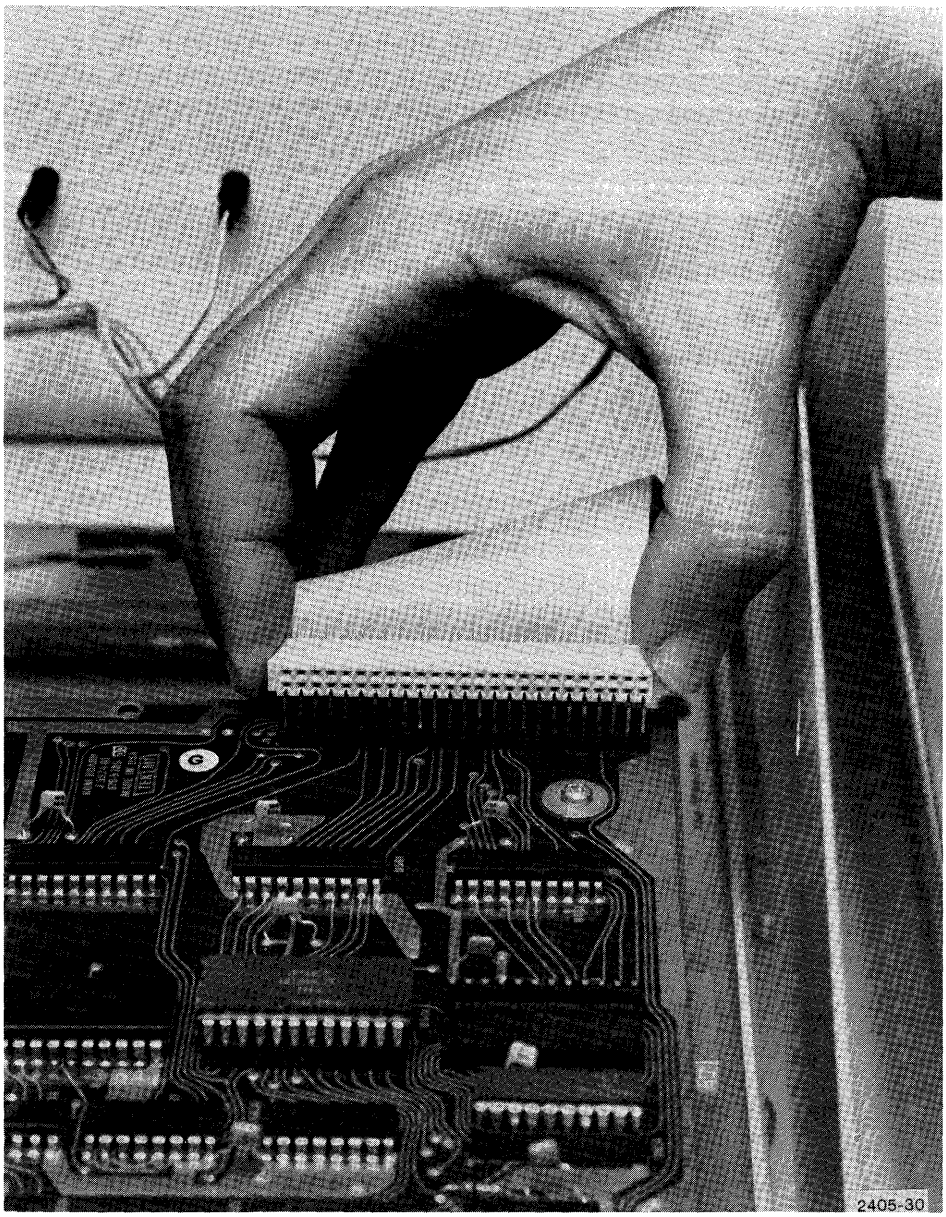


Figure 4-14. Removing ROM Board and Cable.

Power Supply Board

The only component replacement that requires removal of the power supply board is the power transformer. The transformer wires should first be unsoldered from the power supply board. When reconnecting these wires, refer to Figure 8-2. Each of the two main electrolytic filter capacitators can be replaced by removing its two attaching screws and sliding it out the bottom of the cabinet through the nylon shield.

Any time an interconnect ribbon cable on the power supply board is removed, be sure it is replaced properly. The correct mounting positions for these ribbon cables are shown in Figure 8-4 for each of the three basic systems: 4907, Option 30 and Option 31. Once again, be sure jack and connector are correctly matched.

Control Board

If the Control Board needs to be removed:

1. First, remove the ROM Board.
2. Then, disconnect the cable plugs J300, J533, and J545.
3. Next, remove the four screws from the GPIB jack on the outside of the rear panel. (This allows the Control Board to be removed without unsoldering the pins on J151.)
4. Finally, remove the five remaining board mounting screws (one holds a ground wire), and lift the board out.

Power Selector/Filter Unit Replacement

If this unit appears to be faulty, simply replace it rather than attempting a repair.

1. First note carefully in writing the color coding for each of the connecting wires and which terminal(s) they are attached to.

   Color codes are duplicated, so note where the wires come from. (See Table 4-4 for unit connections in a 4907.)

2. Grasp each MALCO or spade connector with pliers and disconnect wires from unit terminal pins.

Table 4-4

LINE SELECTOR/FILTER CONNECTIONS

Selector Unit Terminal	Transformer Wires	A.C. Motor Wires	On/Off Switch Wires
A	8-5 grey/green		
B			8-02 grey/red/black
C	8-3 grey/orange	8-1 grey/brown	
D	8-04 grey/yellow/black		
E	8-19 grey/brown/white	8-2 grey/red	
F	8-2 grey/red		
G		5-4 (to safety ground) green/yellow	
J			8-29 grey/red/white
L			8-01 grey/black/brown
N			8-19 grey/brown/white

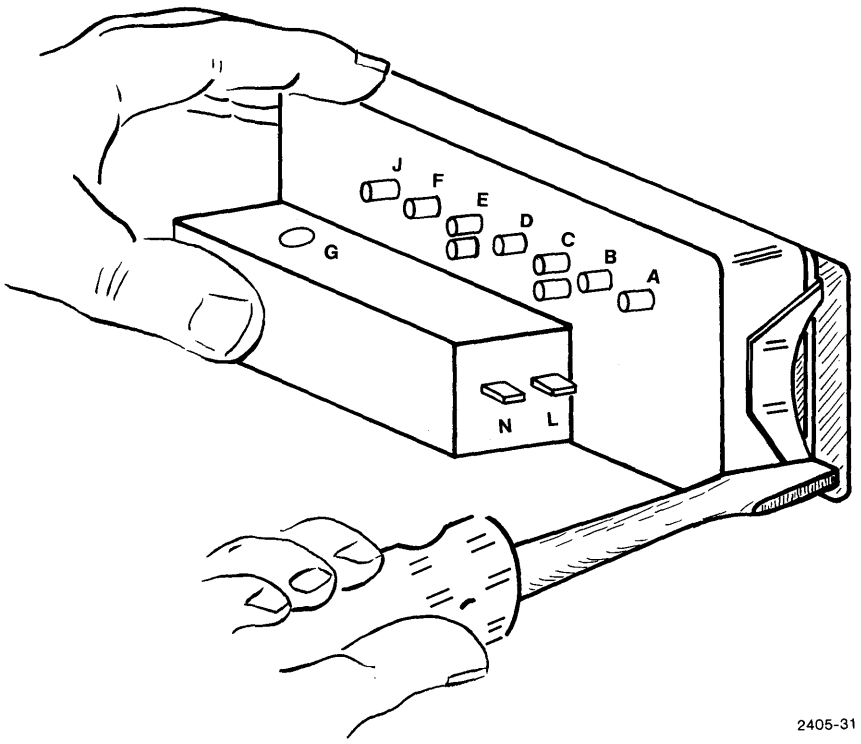


Figure 4-15. Depress Spring Retainers to Remove Line Selector.

3. To remove the unit:

   a. Use a screwdriver to depress the spring clips on one side first (Figure 4-15).

   b. Twist the unit slightly in that direction.

   c. Pull the depressed clips into the panel opening (which keeps them depressed).

   d. Then repeat for the other side of the unit.

   e. Rock the unit slightly to side while pulling unit through the rear panel opening.

f. A screwdriver blade between the outside face of the rear panel and the lip on the unit gives additional needed leverage for quick removal.

4. To replace line selector unit.

   a. Push new unit into rear panel from open side.

   b. Reconnect wires as before. (Check Table 4-3.)

   c. See that the voltage selector card is oriented for the correct line voltage. (Refer to Installation Section "Line Voltage and Frequency Considerations").

Power Switch Replacement

The front panel mounted power switch contains an incandescent power indicator lamp. This lamp is not accessible for replacement, so the entire power switch is replaced when it burns out. To remove the switch:

1. Remove cabinet bottom panel.

2. Verify that the color codes of switch connecting wires correspond to Figure 4-16.

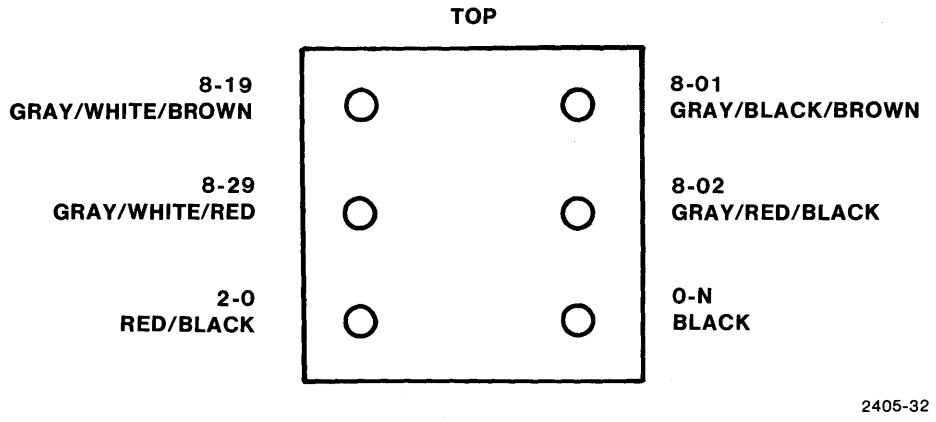


Figure 4-16. Power Switch Wiring Code.

3. Then remove the wiring connectors from the power switch.

4. Inserting a screwdriver between the cabinet frame and the retainer tabs on the switch, use leverage to depress the tabs (Figure 4-17).

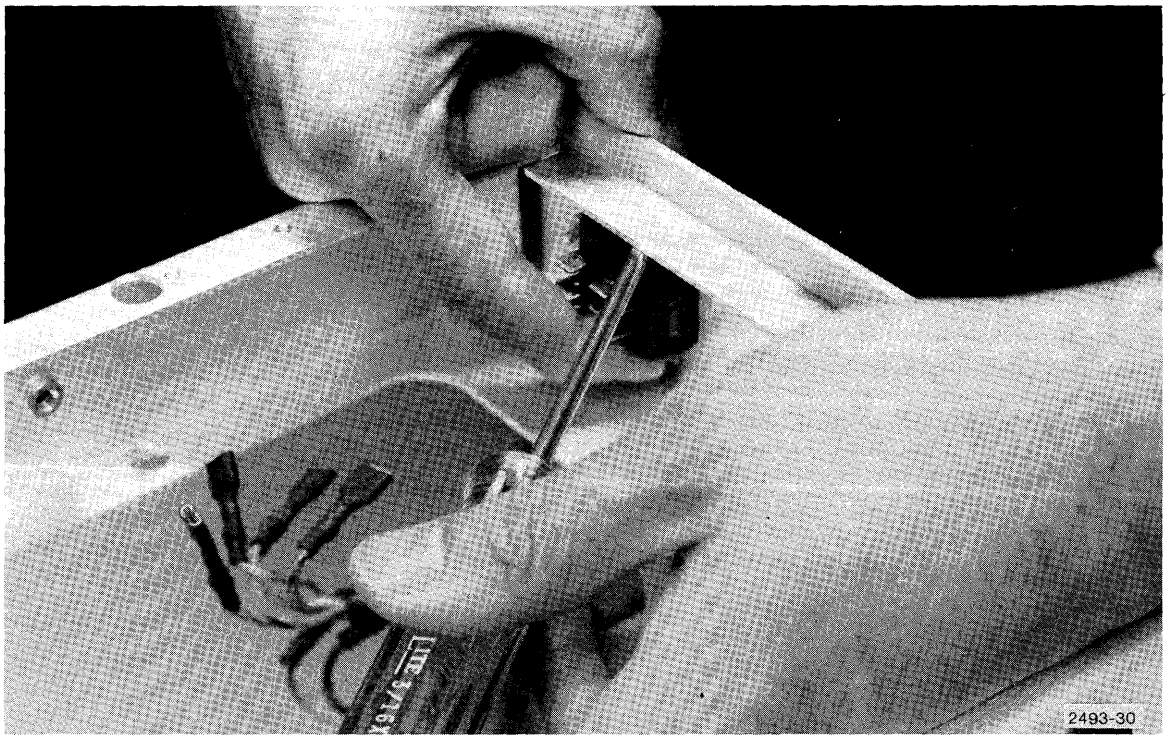


Figure 4-17. Removing Power Switch.

5. Simultaneously press forward on the switch and it will pop out of the panel on the front side.

6. To reinstall the switch, simply press it into the panel hole and reconnect wires as in Figure 3-14.

Cooling Fan Replacement

When replacing the cooling fan, be sure it is mounted with the fan blades next to the cabinet panel. By mounting the fan in this direction, air is pulled through the cabinet for increased cooling effect. Polarity of the A.C. power wires is not important. (See Figure 4-18.)

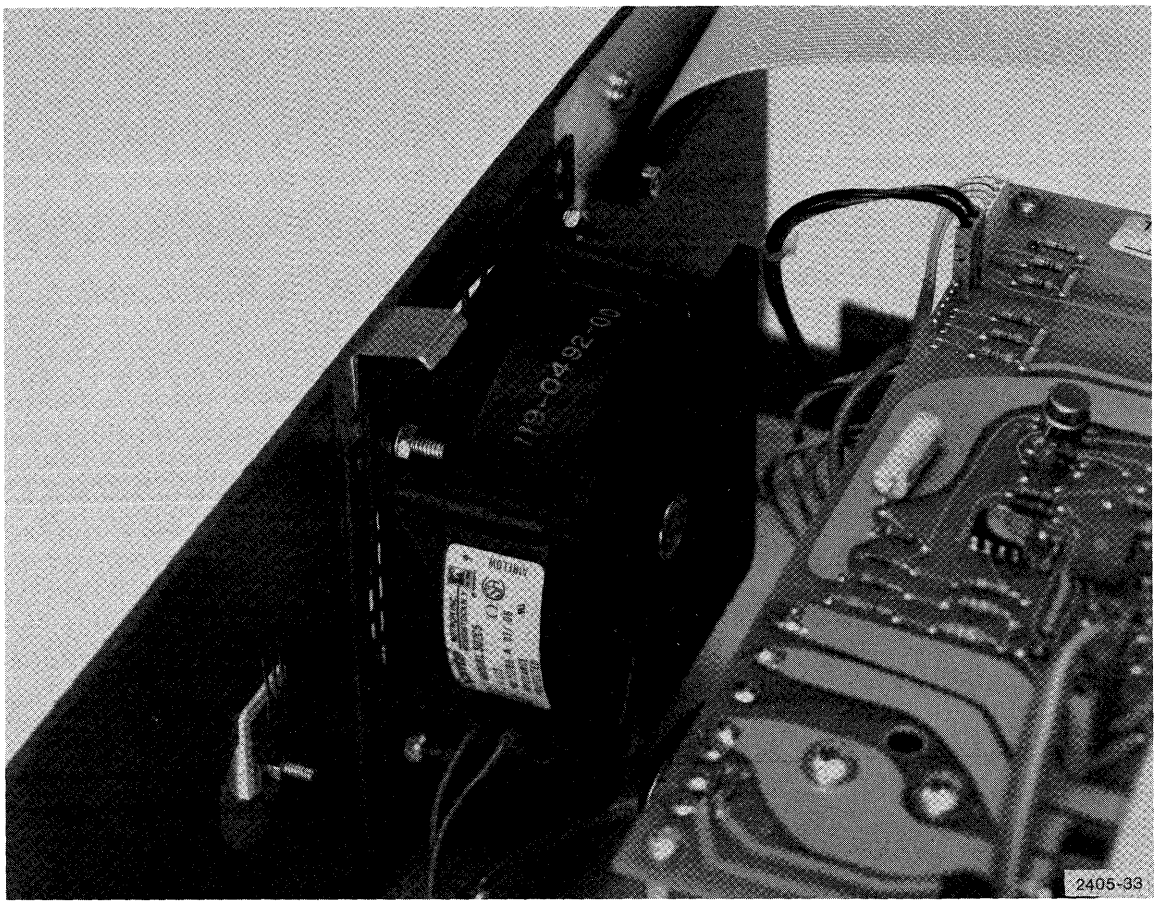


Figure 4-18. Cooling Fan Mounted Properly.

Power Darlington Transistors

When you replace one of the power transistors, observe the following procedure and cautions. Also see Figure 4-19.

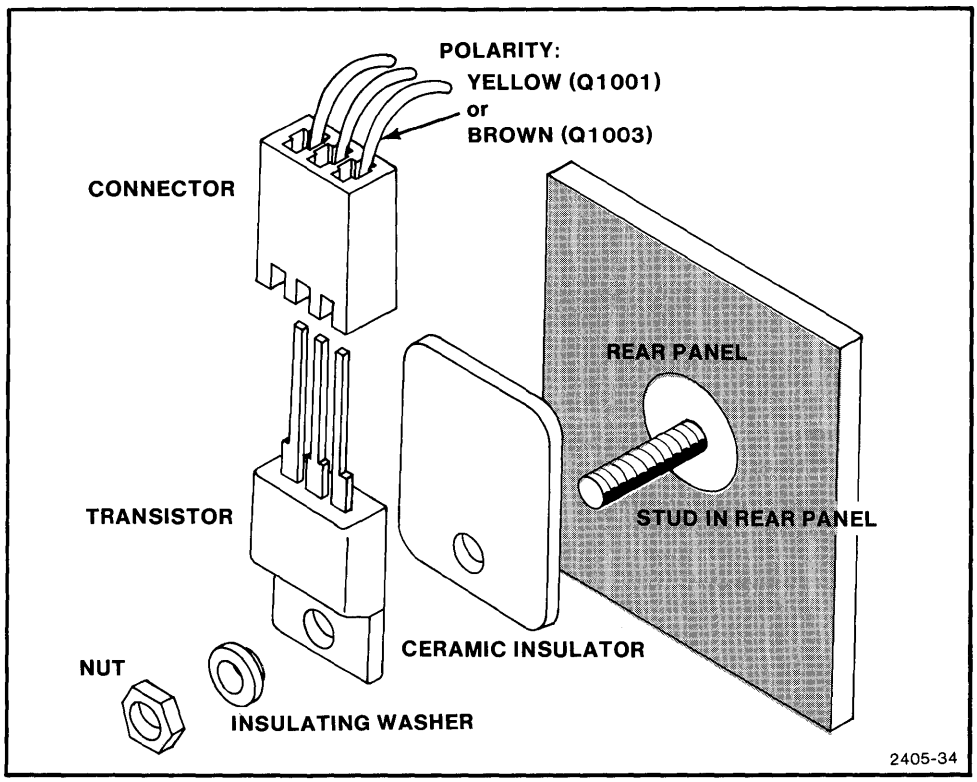


Figure 4-19. Mounting Power Transistors.

Place a ceramic (heat pass) insulator and the new transistor over the mounting stud and against rear cabinet panel.

NOTE

When placing insulator between transistor and case, no grease is needed (unless a mica insulator is substituted for the ceramic one).

WARNING

Silicon grease can cause severe eye irritation. If such grease is used, wash hands thoroughly after contact with it.

Now place an insulating washer over the mounting stud, against the new transistor. Then screw the fastening nut onto the stud and against this washer.

CAUTION

Omitting the insulating washer will cause a short circuit.

Also be careful to not over-tighten and crack the ceramic insulator when securing the mounting nut.

After the new transistor is mounted, reconnect the three-wire plug.

CAUTION

Be sure the transistor plug is oriented for correct polarity as indicated by the color code in Figure 4-19.

Connecting Cable Assemblies

If there is a question about what type of cable assembly connects to a certain component, or where it should run, see Figures 8-1 through 8-4 (Cabling Diagrams). If a defective cable needs replacement, use the numbers (by each cable) to reference to the cable assembly parts list.

Components With Polarity Observation

The following items are easily replaced, but exercise care to observe polarities and orientation of connectors.

- The six front panel indicator LEDs push out the front side of the front panel.
- Write protect switch.
- The GPIB address selector is located near the GPIB connector on the Control Board. The rocker switches should be depressed toward 1, 2, 3, 4, 5, 6 (away from OPEN). This gives the 4907 a 0 address on the bus.

  When replacing the switch its numbers (1, 2, 3, 4, 5, 6) are on the same side as 1, 2, 4, 8, 16 printed on the board. (See Figure 4-3.)
- Q168 SCR mounted near fuse F163.
- CR 1001. Large square diode bridge unit (Figure 8-4).
- CR 1003. Long narrow diode bridge unit (Figure 8-4).
- RAMs and ROMs.

Section 5

TESTING AND CALIBRATION

MATERIALS FOR SERVICING

General Test Equipment

General testing procedures for the 4907 require the following equipment:

- Test Oscilloscope. Must have two channels (one with Invert and one with ADD) and Ext. Sync. For example, a Tektronix Model 465 Oscilloscope.
- Frequency Counter. Tektronix Model DC503 or equivalent.
- Digital Multimeter. Tektronix Model DC501 or equivalent.
- 405X Graphic System.
- Formatted Scratch Disc.
- Assorted screwdrivers and handtools (including 1/4" flex nut drive).

Special Test Equipment

Particular tests will require special test equipment, as follows:

- 6800 System Test Fixture. To test RAMs and ROMs on control and ROM boards. Tektronix part number: 067-0746-00.
- Buffer Adapter Test Board. Used with System Test Fixture. Tektronix part number: 067-0811-00.
- 4907 PROM Package. Plugs into System Test Fixture and contains programs for testing the 4907. Tektronix part number: 067-0856-00.

- Alignment Disc. For Read/Write Head radial and azimuth alignment and Sector photo-detector alignment. Tektronix part number 119-0896-00 (Dysan 240S hard sectored).

- Cartridge (disc) Guide Adjustment Tool. For aligning the cartridge guide after replacement. Tektronix part number: 003-0831-00.

- Load Bail Gauge. For aligning the Head Load Actuator. Tektronix part number: 003-0832-00.

- Spanner Wrench. For replacing the spindle pulley. Tektronix part number: 003-0830-00.

TROUBLE ISOLATION AND TESTS

General Troubleshooting

When you encounter a malfunctioning 4907 system, you should first verify that the system components are cabled and connected properly (see Section 1, Introduction).

Then be sure the operator is not overlooking a command syntax error. (This may even be something as simple as using a lower case L instead of 1, or O instead of 0.) Run through a simple program, similar to the checkout program in Section 1, to determine the general nature of the problem. If the problem is in the power connector or power supply this should be obvious (no pilot light, no DC voltages, etc.). Refer to the following text under sub-title Power Supply Problems.

Error Messages

Usually a 4907 malfunction causes an error message on the 405X screen. A complete list of error messages appears in Appendix B. These error messages are explained, and troubleshooting clues accompany the hardware related errors.

A typical hardware (or firmware) type error message appears on the 4051 screen in the following format:

ERROR 15—DEVICE I/O ERROR—DEVICE ADDRESS 0—010000AC 40

This means that drive unit (device) 0 has experienced some kind of read problem. It also means that the problem occurred at address 010000AC on the disc. The last two digits, 40, indicate a CRC or header parity error. This suggests a head amplitude (or similar read hardware) problem. (See Appendix B for complete list of Message 15 I/O Errors.)

This same error message could also indicate a defective area on the disc. To isolate the problem, first insert a disc media which you know is not defective. If the problem is solved, the first disc media is defective. Use the CALL "MRKBBG" (Mark Bad Block Group) command to remove this portion of the disc from service (see 4907 Operator's Manual). If the problem persists, this indicates a hardware error which you can proceed to isolate.

The CALL "HERRS" Diagnostic

The CALL "HERRS" (Hard Error Status) command is a general diagnostic tool which indicates the overall condition of the instrument. Using this command is like "taking the 4907's temperature or blood pressure." It will tell you if the instrument is beginning to have trouble but it will not tell you specifically where the problem is located.

Specifically, this command accesses a routine that counts and sorts the number of successful I/O operations and unsuccessful attempted I/O operations (retries). This routine will not destroy information on your working discs, so no scratch disc is needed.

Typically, you might request the hard error status on device zero after several I/O operations, if problems are suspected. See the following sample conversation (user inputs are in bold):

CALL "HERRS",0,A1,A2,A3,A4	0 is the device (drive) address, A1-A4 are numeric variables
A1 10	Number of retries in last I/O operation.
A2 13	Total accumulated retries since power on.
A3 2	Total soft errors (increments if A1 is less than 10)
A4 1	Total hard errors (increments if A1 is 10 or more)

1. After the command line is entered, reenter **A1** on the next line. The 405X will then print the number of retries involved in retrieving the data during the last I/O operation.

2. Enter **A2**. The next line then shows the total number of retries accumulated since the last system power up. (Each successive disc read operation will add its retries to this total until the system is turned off.)

3. Enter **A3**. The following line shows the number of successful data recoveries. If the 4907 is able to recover the desired data with less than ten retries, it views this as a "soft error" (recoverable and random in nature). Each so-called soft error is then added to the number printed back on the line following A2.

   If, on the other hand, the 4907 is unable to recover the desired data in ten retries, it gives up and calls this a "hard error".

4. Now enter **A4**, and the total number of these unsuccessful recoveries (hard errors) is displayed.

The sample conversation shows one hard error (under A4), which is related to the ten unsuccessful retries (under A1). Before that the system experienced thirteen retries, in two separate successful I/O operations, and thus set the soft errors counter to two.

Whenever the system increments the hard error counter by one, the firmware checks the problem and sends the appropriate error message to the 405X display.

The counters that increment the hard and soft error tabulations run constantly and independent of the CALL "HERRS" command; the command is used only to access this information. In a sense, the error counters function as an on-going monitor until power-down.

A few comments about interpreting the Hard (and Soft) Errors Status report. Usually you are forced to deal with hard errors directly as they arise; an error message is displayed and you go to isolate and solve a specific problem.

On the other hand, if a 4907 has intermittent problems or if random I/O performance is suspected, use the CALL "HERRS" to analyze apparent "soft errors". Often a soft error is caused by a chip or drive unit mechanism which is operating close to a tolerance boundary; this can cause the random behavior pattern. In this case further tests would be required to isolate and solve the particular hardware problem. First determine that the flexible disc media is good, before looking for mechanical or electrical hardware problems.

Power Supply Problems

If the power supply appears to be the source of a problem, first verify that fuses are good and that the line voltage selector is set for the proper line voltage.

Then, be sure all straps are jumpered properly on each power supply board. On all supplies the "4905/4907" straps are jumpered across "4907". The "CONT" strap is jumpered only on the Main Cabinet's power supply board. Also check for misaligned or faulty interconnect ribbon cables and connectors. (See Ribbon Cable Interconnect Configurations, Section 8.)

Next, go to the Power Supply Calibration procedure (later in this section) and check all supply voltages and control signals.

Finally, if sporadic or undiagnosed problems remain, read the Power Supply Board Theory of Operation for a detailed circuit description.

Isolating Faulty Memories

Using the System Test Fixture

The following RAM and ROM Tests use the Tektronix 067-0746-00 6800 System Test Fixture. This test fixture connects to a special Buffer Adapter Board (061-0811-00). The 50 pin jack on the Buffer Board mates with the free hanging plug on the ROM Board to Control Board Ribbon Calls. See Figure 5-1.

CAUTION

Be sure the component side of the Buffer Adapter Board is facing up. This insures that the ribbon cable plug and Buffer Board jack are properly matched. Accidentally connecting this jack and plug backwards will severely damage the System Test Fixture. (NOTE 1)

(1)The Buffer Board ground (pin 7 of U75) should be connected to the 4907 circuit ground at B1, B2, and B25 of J1 on the ROM Board. The Buffer Board +5 volt (pin 14 of U75) should be connected to the +5 volt on the ROM Board at B3 and B24 of J1.

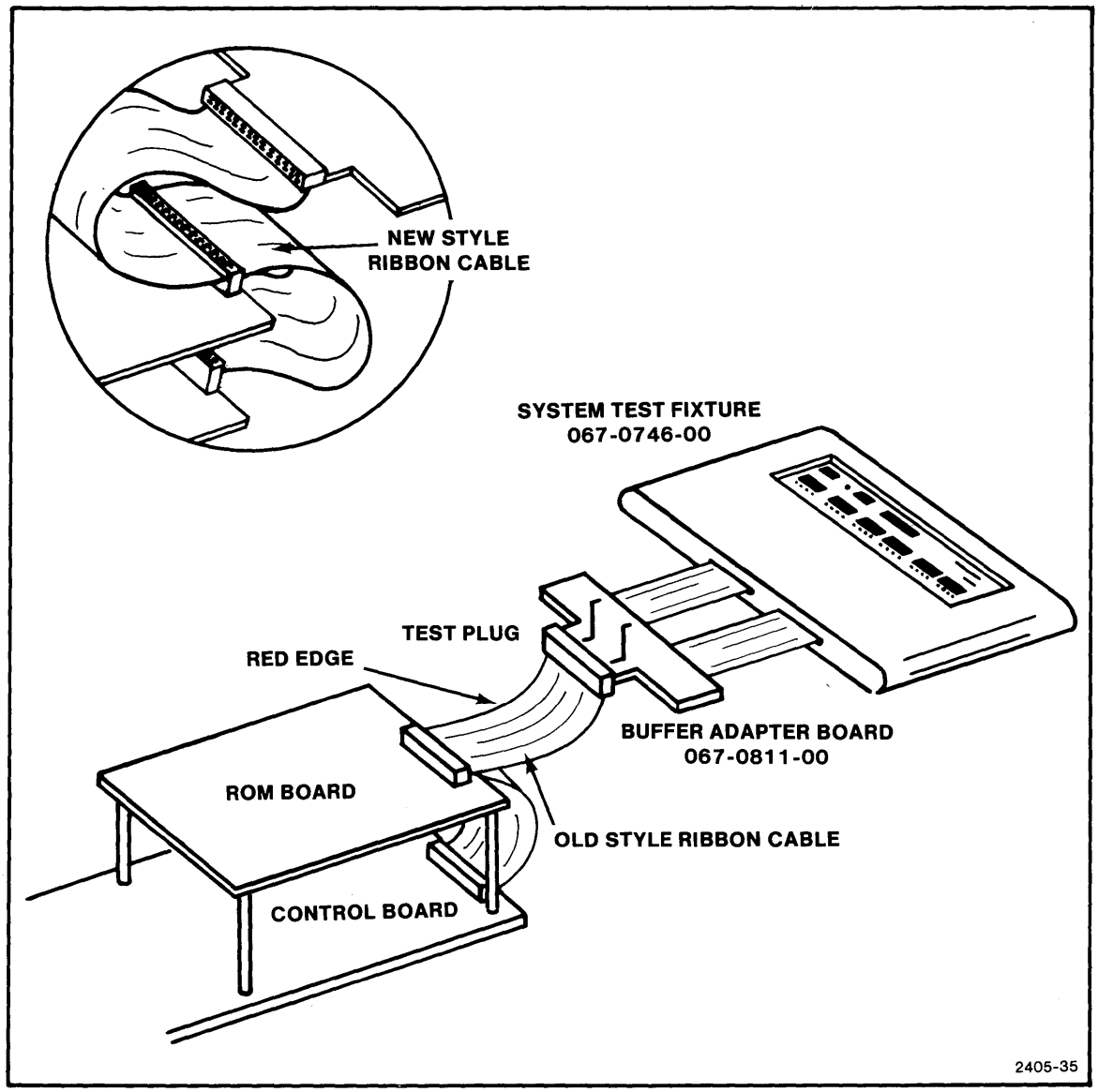


Figure 5-1. System Test Fixture connection.

The various control switches on the test fixture are fully explained in the 405X Service Manual (Vol. 1); see System Test Fixture Switch Functions in Section 5 (Troubleshooting Aids) of that manual.

The indicator lights (LEDs) on the System Test Fixture present information in binary format. Since the following memory tests use hexadecimal notation, you may find it convenient to use Table 5-1, Hexadecimal-to-Binary; in your 405X Service Manual (just preceding the Test Fixture Switch Functions).

If you need more detailed information about the operation of this test fixture, see the 067-0746-00 System Test Fixture Instruction Manual.

RAM Tests

A comprehensive 4907 RAM Test is contained in the 4907 Test PROM (part number 067-0856-00). This test PROM is designed to be installed in the U 81 socket of the System Test Fixture.

Be sure the internal Address Jumper in the test fixture is set for position 9.

If it is necessary to locate a faulty RAM without the aid of the special Test PROM, you may refer to the alternate procedure: Checking RAMs Without Test PROM (later in this section).

The correct procedure is:

1. Turn the 4907 OFF.
2. Connect the System Test Fixture to the 4907 as in Figure 5-1.
3. Turn the 4907 ON.
4. If the ABA LED is off, press STOP then RESTART. This should turn the ABA LED on.
5. Turn the 4907 off and remove ROM Board from on top of Control Board.
6. Move the RAM ADDRESS SELECT strap (on the Control Board) to connect pin 1 and 2 of J213.

7. Replace the Control Board.

8. Set all the control switches on the System Test Fixture to the ON position, except the DATA BREAK switch. Set the DATA BREAK switch OFF.

9. Set the Data Switches for X'9C' and the Address Switches for X'FFFE'. See Figure 5-2.

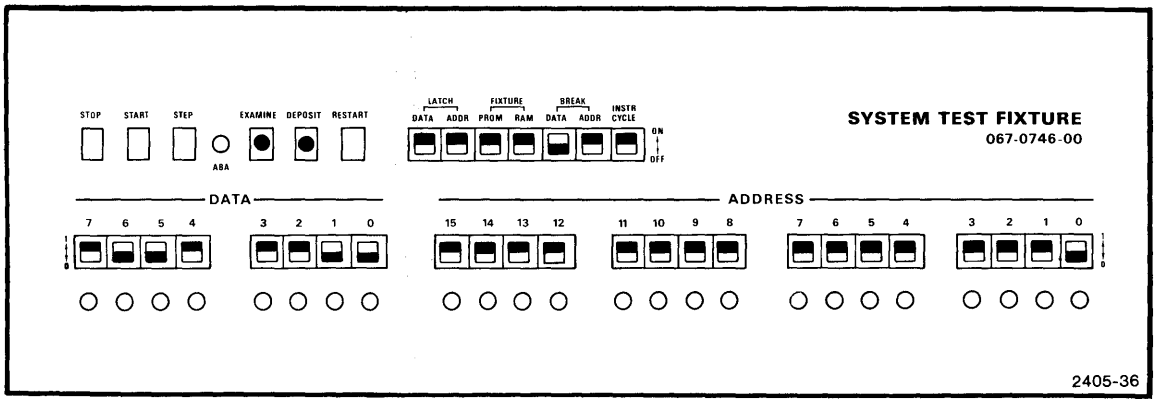


Figure 5-2. Test Fixture Controls and Indicators.

10. Press DEPOSIT.

11. Press EXAMINE to verify that X'9C' was loaded into X'FFFE'.

12. Set the Data Switches for X'00' and the Address Switches for X'FFFF'.

13. Press DEPOSIT and then EXAMINE to verify that X'00' was loaded into X'FFFF'.

14. With the Data Switches at X'00', set the Address Switches for X'FFFD'.

15. Press RESTART, then START.

    When the program stops, the ABA LED turns on . The Address LEDs at this point indicate the faulty address location, if there is one, with the Data LEDs indicating the faulty data bit or bits. If no faulty memory location exists, the highest-numbered address existing in RAM, plus one, is displayed. For the 4907, the RAM address in the Address LEDs for a correct test is X'2000'. If the test indicates an error, refer to Table 5-1 to locate the defective RAM. If the test indicates no errors, continue with Step 16.

    If the ABA LED turns off and the Address LEDs are flashing, the error is in the parity bit. The Address LEDs indicate the defective address and Table 5-1 shows the defective RAM.

16. Press START twice to begin a pattern sensitivity test that takes about 15 minutes.

    If this test is completed without error, the ABA LED turns on, the Address LEDs indicate X'FFFC' and the Data LEDs X'FF'. If an error is detected, the ABA LED turns on, the faulty address is displayed in the Address LEDs, and the Data LEDs corresponding to the faulty bits are lit. Flashing Address LEDs indicates a defective parity bit. Refer to Table 5-1 to locate the defective RAM. Return the RAM ADDRESS SELECT strap J213 to its normal position (pins 2 and 3 connected).

Table 5-1

RAM Addresses

RAM Address Range	Data Bit 0	Data Bit 1	Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7	Parity Bit
X'0000'-'0FFF'	U109	U111	U113	U115	U117	U119	U121	U123	U107
X'1000'-'1FFFF'	U127	U129	U131	U133	U135	U137	U139	U141	U125

Checking RAMs Without Test PROM

The following is an automatic diagnostic check for bad RAMs which is done by the 4907's firmware at power up. This may be useful to find a problem without the test PROM.

If the FAULT light comes on at power up, this indicates the possibility of a bad RAM. When the FAULT light comes on, the data in address locations X'0081' and X'0082' indicates the beginning of the stack. The 4907's microprocessor system is programmed to show where bad memory is located by accessing these addresses. For instance, suppose that addresses X'0081' and '0082' show data of X'00' and 'F5', respectively. The X'00' and X'F5' are the most and least significant portions, respectively, of the first address in the stack. Typically we would work through (the stack) from X'00F5' to X'00FC', while writing down the corresponding data. Table 5-2 shows a typical result and how to interpret such results to locate the bad memory RAMs. The information under the KEY column applies only if the address referred to by X'0081' is X'00'.

Notice that X'FE' was written in but X'FF' was read back. Anytime these two data values are different, look for the bad address in the next two lines. In this case the address in question is X'2000'. Since this is just beyond the last actual memory location, it indicates that ADDRESS STRAP J213 is not in the correct position.

Suppose that the data written by the processor was X'FF' but the data read back was X'FD'. By comparing bit pairs, you can see that bit two is in error. (See Figure 5-3.)

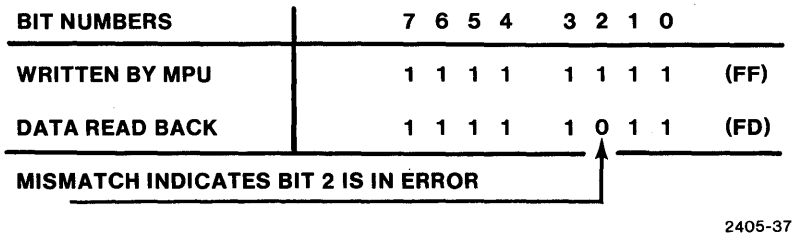


Figure 5-3. Comparing Bit Pairs.

This indicates that RAMs U113, or U131 may be faulty, depending on the memory location. (See Table 5-1 or Schematic sheet 1-3.) If the same data, X'FF', is read back, the parity RAM may be faulty.

Table 5-2

AUTOMATIC RAM TEST ROUTINE

Hexadecimal Address	Hexadecimal Data	Register	Key	
00F5	5C		Ignore	
00F6	D8	condition code	Top of stack	
00F7	FE	"B"	Written into Memory	Different? See next lines for bad memory location
00F8	FF	"A"	Read back from Memory	
00F9	20	h	Most signif.--Bad memory address	
00FA	00	X1	Least signif.--See Table 4-1 for corresponding RAMs	
00FB	FA	Program	Return address to	
00FC	61	Counter	routine that found problem	

ROM Tests

To test the ROMs on the 4907 ROM Board, the 4907 Test PROM (067-0856-00) must be installed in the System Test Fixture socket U81. The System Test Fixture's ADDRESS SELECT jumper should be in its position number 9 (decimal).

NOTE

Before testing the ROM Board ROMs, be sure the 4907 RAMs are good. The "ROM Test" is executed from the 4907 RAMs. The ROM Board must be properly grounded, so it should be mounted in its normal position above the Control Board.

To test the 4907 ROMs, proceed as follows:

1. With the 405X turned OFF, connect the System Test Fixture to the 4907 using the Buffer Adapter Board, as in the preceding RAM tests. Then turn the 4907 ON.

2. If the test fixture ABA LED is off, push STOP then RESTART. This should turn the ABA LED on.

3. Turn on the System Test Fixtures RAM, PROM, DATA LATCH, ADDR LATCH, ADDR BRK and INSTR CYCLE switches. Turn the DATA BREAK SWITCH OFF.

4. Set the Data Switches for X'9E' and the Address Switches for X'FFFE'.

5. Press DEPOSIT and the EXAMINE to verify that X'9E' was loaded into X'FFFE'.

6. Set the Data Switches for X'00' and the Address Switches for X'FFFF'.

7. Press DEPOSIT then EXAMINE.

8. With the Data Switches at X'00', set the Address Switches for X'FFFD'.

9. Press RESTART, then START.

   This starts a "down load" routine which copies the test routine from the System Test Fixture's ROM U81 into the 4907 RAM. The down load routine will stop with ABA LED on.

10. With the Data Switches at X'00', change the address Switches to X'00FD'.

11. Turn the RAM switch off.

12. Press START.

    The program computes a checksum for one of the 4907 ROMs and stops with the checksum displayed in the System Test Fixture's "data" LEDs, and the address of the ROM in the "address" LEDs. Refer to Table 5-3 and compare this checksum to the checksum given in the table for the particular version of the ROM being tested. If the checksums do not agree, the ROM is probably defective.

13. To continue the test, push START. Each time START is pushed, the program will compute the checksum for another ROM. When it has checked the last ROM, it will start over again with the first ROM in the list.

Table 5-3

4907 FIRMWARE CHECKSUMS

Part Number	Circuit Number	Starting Address (Hexadecimal)	Version 1 Without FPLA (Hexadecimal)	Version 1 With FPLA (Hexadecimal)	Version 1.1 With FPLA* (Hexadecimal)
156-1067-XX	U121	A000	CF (00)	CF	CF (00)
156-1068-XX	U131	A800	2B (00)	9F	AE (00)
156-1069-XX	U141	B000	64 (00)	64	64 (00)
156-1070-XX	U151	B800	A4 (00)	A1	5D (00)
156-1071-XX	U161	C000	C1 (00)	C1	C1 (00)
156-1072-XX	U201	C800	E8 (00)	E8	E8 (00)
156-1073-XX	U211	D000	5A (00)	5A	5A (00)
156-1074-XX	U221	D800	39 (00)	39	0D (00)
156-1075-XX	U231	E000	79 (00)	79	79 (00)
156-1076-XX	U241	E800	47 (00)	47	47 (00)
156-1077-XX	U251	F000	AA (00)	AA	AA (00)
156-1078-XX	U261	F800	0E (00)	0E	2A (00)
156-1079-XX	U271 U271	6000 6800	6C (00) 6C (00)	5B 5B	5B (00) 5B (00)
156-0960-XX	U631	8000	99 (00)	E3(06)	76 (07)

*Version 1.1 FPLA part number: 156-0940-14

If the ROM checksums indicate a ROM is defective and an FPLA (Field Programmable Logic Array) is installed in ROM board socket U541, you must determine if the ROM or the ROM fix is defective. To do this, turn off the 4907, remove the FPLA U541 and repeat the ROM checksum test. Table 5-3 shows the correct checksums with and without the FPLA.

ROM Pack ROM Tests

To check the File Manager ROM Pack ROMs, remove the ROM chips from the ROM Pack and substitute them for the ROMs on the ROM Board. Replacing U121, 131, 141, and 151 is suggested, as they correspond with the first addresses to be checked. Do not replace U271 on the ROM Board. Be sure the FPLA U541 is removed from the ROM Board. Also remember that the ROM Board must be mounted for proper grounding.

Repeat the ROM Test procedure as before, comparing indicated checksums with Table 5-4.

Table 5-4

ROM PACK CHECKSUMS

Part Number	Typical Locations	Version 1 Without FPLA (Hexadecimal)
156-1102-XX	U121	EB
156-1103-XX	U131	34
156-1104-XX	U141	EE
156-1105-XX	U151	28

CALIBRATION AND ALIGNMENT

Power Supply Calibration Procedure

1. Check the line voltage selector circuit card for the proper setting. The correct local line voltage (110, 120, 220, or 240) should be visible through the plastic window.

2. Remove the top cover panel from the 4907 cabinet.

3. Locate the strap CONT on the Power Supply board. When calibrating or testing a supply separately, this strap should be in place.

NOTE

During normal operation the CONT strap is in place only on the 4907 Main Cabinet power supply; it is removed on the Auxiliary Cabinet supplies.

4. To calibrate the +5 volt supply, connect a digital volt meter (such as the Tektronix DM501) between pin 2 of J1 (top right corner of power supply board) and ground.

5. If necessary, adjust potentiometer R 350 (Figure 5-4) for +5.15 VDC $\pm$ 10 mV.

6. Check the ripple for 25 mV maximum.

7. To calibrate the +24 volt supply, connect the digital volt meter between pin 1 of J1 and ground.

8. Check for +24 VDC $\pm$ 5% (1.2 VDC).

9. Check the ripple for 50 mV Maximum.

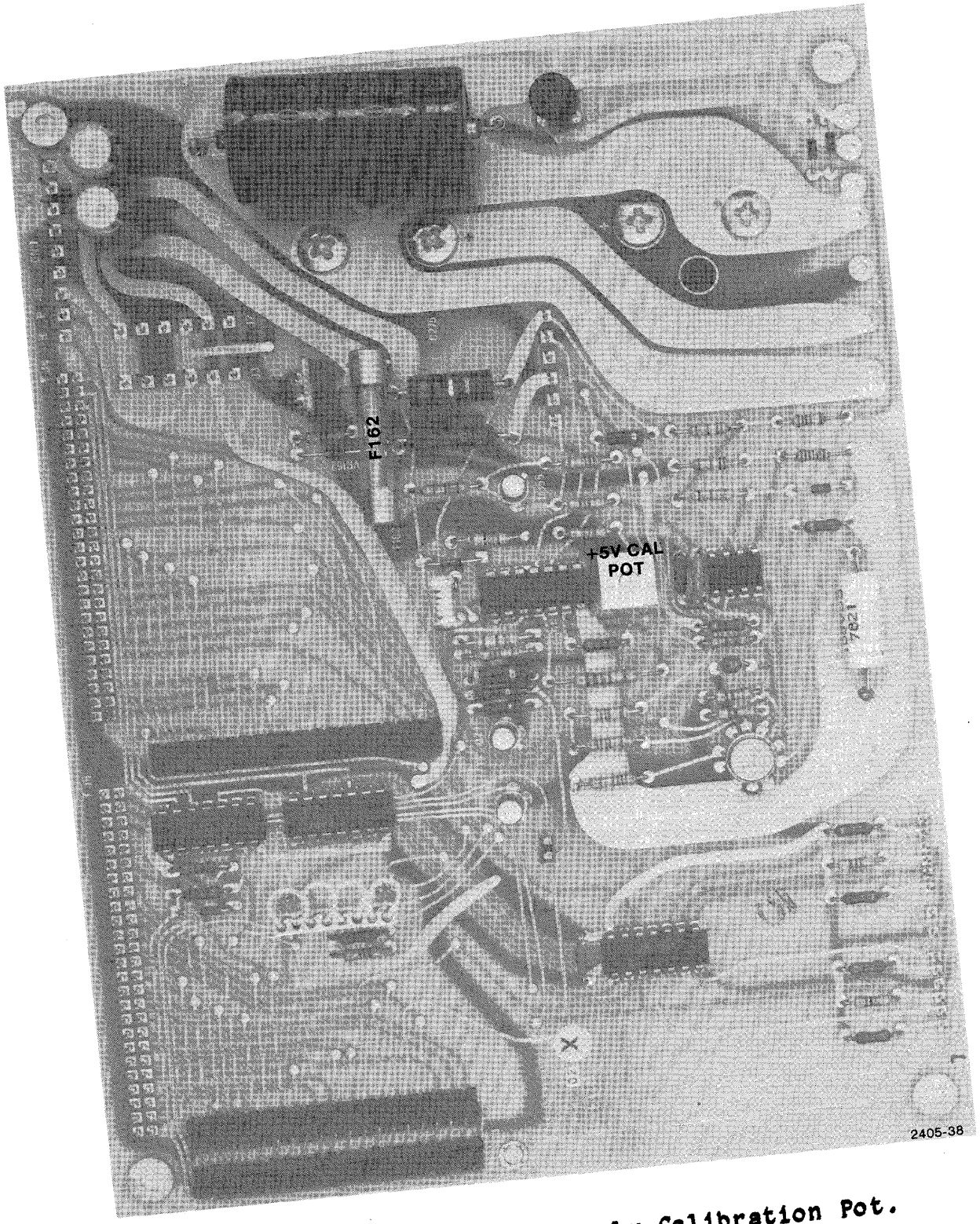


Figure 5-4. Power Supply Calibration Pot.

There are no adjustments for timing of the control signals (RESTART, PWR ALRM, 24 off/on). To find out if these signals are timed properly, refer to the diagrams and text under Power Control in Section 6 (Theory of Operation). If timing of a particular control signal is the only problem, you must locate and replace the defective part (OP. AMP., resistor, etc.) in that circuit.

Disc Drive Alignment

Remove the top and bottom covers of the 4907 and place the chassis on its side. All cabling inside the 4907, plus the GPIB cable to the 405X, should remain connected as for normal operation.

The 4907 Alignment Program uses the user keys of the 405X to select functions. The 4907 Alignment Program listing is located in Appendix E of this manual. All tests, except the writing of X'2F' pattern for head amplitude check, will operate independently of the 4907 ROM Pack.

Be sure that the Hard Sectored Alignment Disc (119-0896-00) is used, and not the Shugart Soft Sectored Alignment disc (SA 120). Alignment with the Soft Sectored Alignment Disc makes the 4907 incompatible with other 4907's; also, the 4907 Alignment Program from 405X will not work.

The only head alignment operations described in this manual are those that contain specifications peculiar to the 4907. All other adjustments are described in the 119-0977-00 Flexible Disc Drive Instruction Manual, and consist of the following:

Write Protect Detector
Head Load Actuator Mechanical Adjustment
Index/Sector Photo Transistor Potentiometer
Cartridge Guide
Stepper Carriage Assembly
Read/Write Head Load Button
Head Penetration
Read/Write Azimuth

Head Radial Alignment

The following steps describe the proper procedure for aligning the radial orientation of the Read/Write Head.

NOTE

Head Radial Alignment should be checked prior to adjusting track 00 and Sector to data timing.

a. Insert the 119-0896-00 Alignment Disc in the drive.

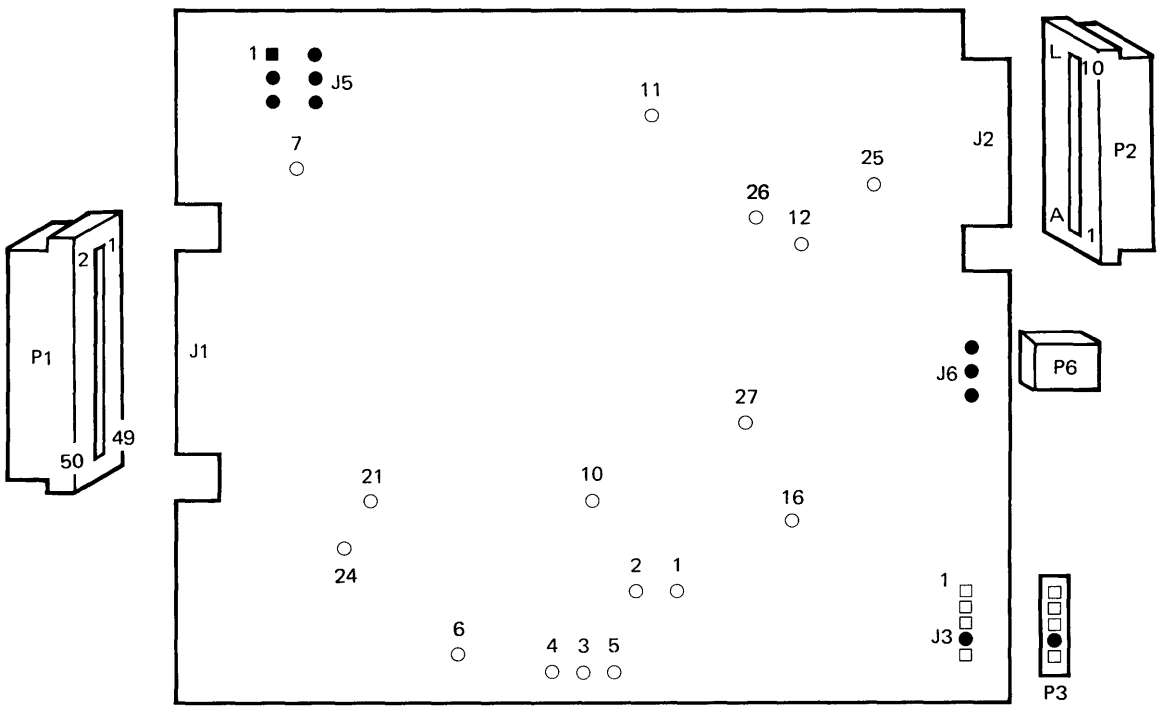
b. Set up oscilloscope as follows:

SYNC: EXT. NEG
20msec/div
Connect ext. probe to TP-10 (-CE Index)(see Figure 5-5 for test point locations).

CHAN 1: AC
100 mv/div.
Connect probe to TP-1

CHAN 2: AC
100 mv/div.
Connect probe to TP-2

MODE: ADDED
Chan. 2 inverted



KEY

Test Point	Signal	Test Point	Signal
1	Read Data Signal	11	+ Head Load
2	Read Data Signal	12	– Index and 801 Sector Pulses
3	Read Data (Differentiated)	16	+ Read Data
4	Read Data (Differentiated)	21	– Data Separator Time + 1
5	Signal Ground	24	– Data Separator Time + 2
6	Signal Ground	25	+ Write Protect
7	Signal Ground	26	+ Detect Track 00
10	– Index	27	+ Gated Step Pulses

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Figure 5-5. Drive Unit Test Points.

c. Step the carriage to track 38. (user key #6)

d. The two lobes or "cat eyes" will now be displayed. The two lobes must be within 70% amplitude of each other. See Figure 5-6. If the lobes do not fall within the specification, continue at step e. If the lobes are within the specification, continue at step h.

e. Loosen the two mounting screws which hold the motor clamp to the mounting plate.

CAUTION

Do not loosen the three screws coated with glyptol.

f. Rotate the stepper motor to radially move the head in or out. If the left lobe is less than 70% of the right, turn the stepper motor counterclockwise as viewed from the rear. If the right lobe is less than 70% of the left lobe, turn the stepper motor clockwise as viewed from the rear.

g. When the lobes are of equal amplitude, tighten the motor clamp mount screws.

h. Check the adjustment by stepping off one track (user key #2 and #3) and returning. Check in both directions and readjust as required.

i. Whenever head alignment has been adjusted, track 00 alignment must be checked and readjusted if necessary.

Track 00 Alignment

The following steps tell how to adjust the Track 00 Flag. A separate Track 00 Stop adjustment is described in the 119-0977 Flexible Disc Drive Instruction Manual.

a. Insert the Alignment Disc.

b. Set the oscilloscope as follows:

SYNC: Auto, internal, neg, or pos
Time/div ... to any continuous sweep

CHAN 1: DC
1 volt/div
Connect probe to TP-26

MODE: Chan 1

c. Check head radial alignment and adjust, if necessary, before proceeding.

d. Step carriage to Track 01 (user key #5). TP-26 should be high (+5 volts).

e. If TP-26 is not high, loosen screw holding Track 00 flag and move flag towards stepper until TP-26 goes high.

f. Step carriage to Track 2 (user key #2). TP-26 should go low. If TP-26 is not low, adjust flag towards spindle until TP-26 goes low.

g. Check adjustment by stepping carriage between Tracks 00 and 02, observing that TP-26 is low at Track 02 and high at Track 01 and 00. (User keys #2 and #3).

h. Verify that the head radial alignment is still correct.

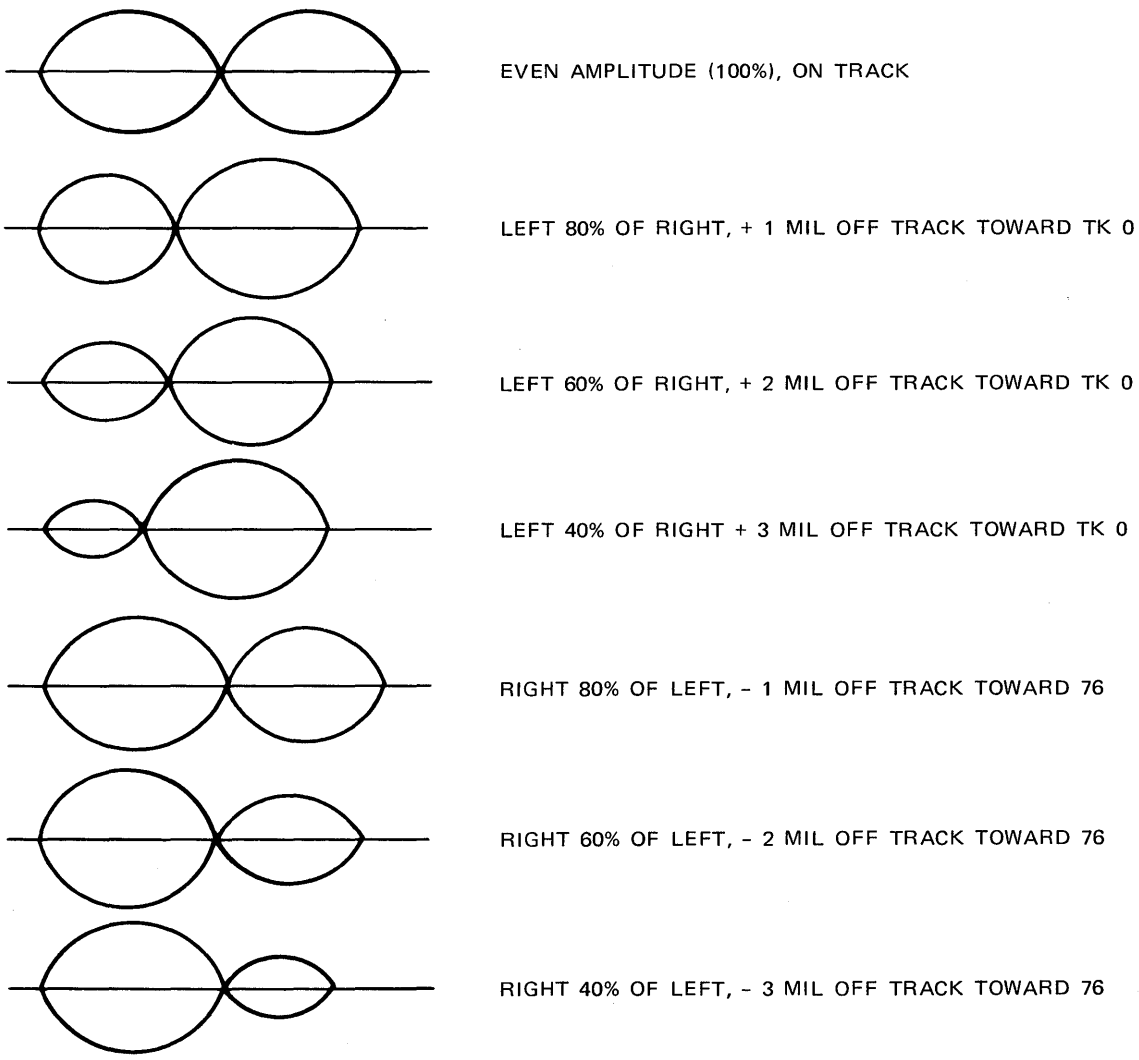

Figure 5-6. Read/Write Head Radial Alignment.

Sector to Data Alignment

The timing between each sector pulse and the data that follows in that sector is called "Index to Data". The following steps describe the adjustment of this variable in the drive unit.

a. Insert the Alignment disc in the drive.

b. Set oscilloscope as follows:

SYNC: EXT. NEG.
50 sec/div
Connect ext. probe to TP-10
(- Index)

CHAN 1: AC
200 mv/div
Connect probe to TP-1.

CHAN 2: AC
200 mv/div
Connect probe to TP-2

MODE: ADDED
Channel 2 inverted

c. Step carriage to Track 01. (User key #5)

d. Observe the timing between the start of the sweep and the leading edge of data burst. This should be 200 ± 50 usec. (see Figure 5-7). If the timing is not within tolerance, continue on with step e. If it is within tolerance, then go to step i.

e. Loosen the holding screw in the Index/sector Transducer until the Transducer is just able to be moved.

f. Observing the timing, adjust the Transducer until the timing is 200 ± 50 usec. Insure that the Transducer assembly is against the registration surface on the base casting.

g. Tighten the holding screw.

h. Recheck the timing.

i. Seek to Track 76 (user key #8) and reverify that the timing is 200 ± 50 usec.

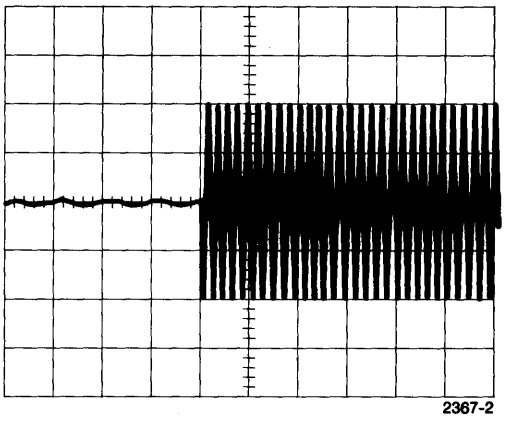

Figure 5-7. Sector to Data Delay Waveform.

Head Load Actuator Timing

See 119-0977-00 Flexible Disc Drive Manual for a general Head Load Actuator adjustment which specifies the mechanical tolerances of the up-stop and down-stop screws. The same manual also includes a general tension adjustment for the Read/Write Head Load Button. The following procedure describes the adjustment of the down-stop screw to achieve proper head load timing. See Figure 5-8.

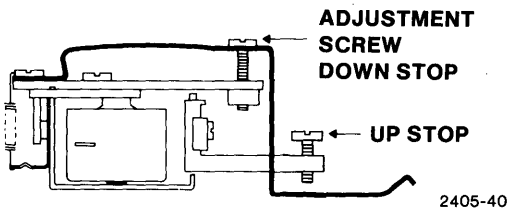

Figure 5-8. Head Load Actuator Down-Stop Adjustment Screw.

a. Insert Alignment Disc in the drive.

b. Set up oscilloscope as follows:

SYNC: EXT. Positive, TP-11,
10 msec/div.

CHAN 1: AC
100 mv/div.
Connect probe to TP-1.

CHAN 2: AC
100 mv/div
Connect probe to TP-2

MODE: ADDED
Channel 2 inverted

c. Step Track 75 (user key #15).

d. With head unloaded, load the head and observe the read signal on the scope. The signal must be at 50% of full amplitude by 35 msec. See Figure 5-9. (4907 Alignment Program has a function that loads and unloads the head at Track 75 automatically when user key #15 is selected.)

e. If this timing is not met, adjust down-stop screw clockwise until timing is met.

NOTE

Do not adjust the down-stop screw clockwise more than one-quarter turn. Turning this screw too far in will increase wear on head load button.

f. If you cannot adjust the down-stop screw to meet timing requirements, refer to Head Load Actuator Adjustment in the 119-0977-00 Flexible Disc Drive Instruction Manual.

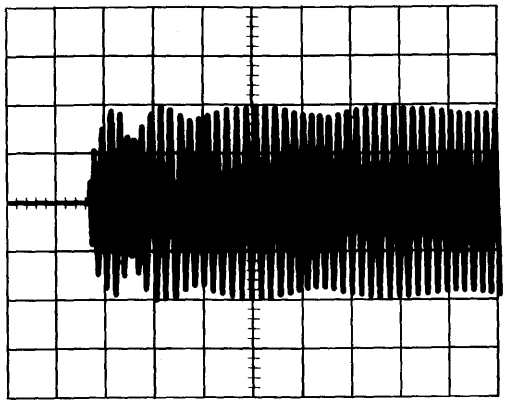

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Figure 5-9. Head Load Timing.

Head Amplitude Check

The following procedure describes the measurement of the Read/Write Head's output signal level. No adjustments are included because a low reading calls for cleaning or replacement of the head.

a. Install a good (no bad blocks) formatted scratch disc.

b. Set up oscilloscope as follows:

SYNC: EXT. Neg.
1 msec/div
Connect the Ext. probe to TP-12 (-Index)

CHAN 1: AC
50 mv/div
Connect probe to TP-1

CHAN 2: AC
50 mv/div
Connect probe to TP-2

MODE: ADDED
Channel 2 inverted

c. The scope probes on TP-1 and TP-2 must be removed while writing on Track 76.

d. Step to Track 76 (with user key #12) and write the entire track with X'2F' signal. ("FDCAL" alignment program allows writing a X'FF' pattern on track 76.)

e. Read back Track 76. Check that the average minimum amplitude, peak to peak, is 110 millivolts. This is typically 170 millivolts or better when new.

f. If the output is below minimum, the load pad should be replaced, the head cleaned and a different media tried. If the output is still low, it will be necessary to install a new head and carriage assembly.

Section 6

THEORY OF OPERATION

INTRODUCTION

This section provides the service technician with information about the operating principles of 4907 systems. This information serves as background material for servicing or troubleshooting. The discussion begins with an overview of the system architecture, showing the basic blocks and their relationships to each other. Next is a description of the memories and addressing scheme used in the 4907. This is followed by a discussion of the format and data structure on the flexible disc media.

The next major portion of this section contains the intermediate and detailed level circuit descriptions for the parts of the 4907 control board.

The section concludes with a discussion of the ROM board, file manager ROM Pack, and the system power supplies.

SYSTEM ARCHITECTURE

The 4907 File Manager system is composed of several basic block units which are illustrated in Figure 6-1. The 4907 Main Cabinet contains one flexible disc drive unit with the hardware and firmware necessary to control writing and reading data to and from the flexible disc media. A Motorola 6800 Microprocessor unit (MPU) is the heart of the 4907's control board. This MPU uses the contents of read-only memory (ROM) to specify how the system is to perform. A separate ROM board contains the ROMs holding these firmware routines. Temporary storage of data and MPU instructions is handled by random-access memories (RAM) located on the Control Board.

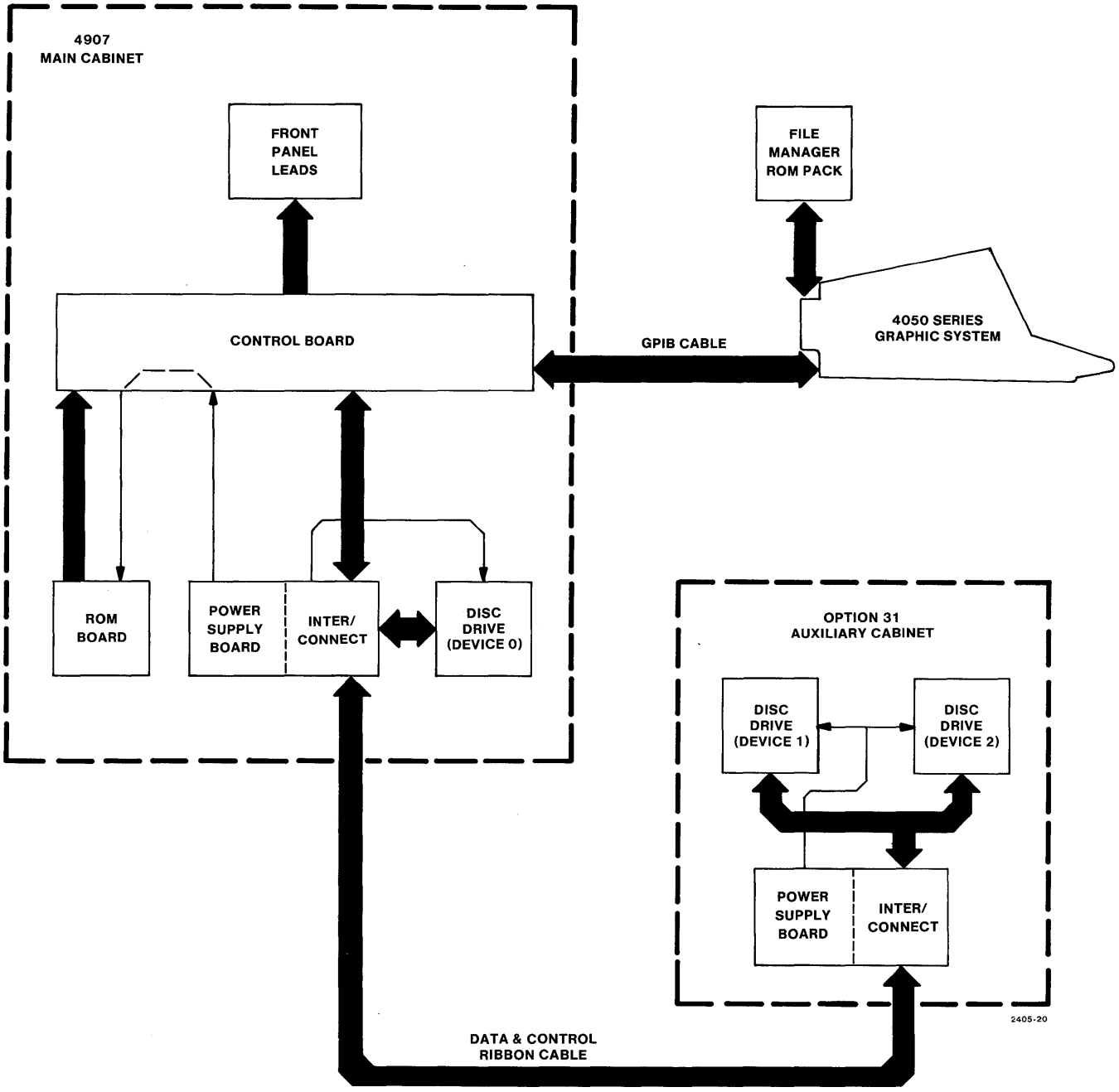


Figure 6-1. Basic System Block Diagram.

The flexible disc drive unit (with its own drive board) receives control and data information from the MPU through special encoders. Likewise, the disc unit sends status and data back to the MPU through a decoder. If the OPTION 30 or 31 Auxiliary Cabinet is connected, this places one or two additional disc drives under the control of the 4907's MPU. These extra drive units are connected to the main cabinet via a special ribbon cable.

The 4907 File Manager system is incomplete without a 405X Graphic System, which serves as the primary operator interface. **(NOTE 1)**

The 405X acts like a host computer and the 4907 serves as a mass storage peripheral connected via the GPIB **(NOTE 2)** cable. A 405X, with its own 6800 MPU, is preset to act as "controller" on whatever GPIB system it is connected. In this context the 405X and 4907 pass the standard control signals back and forth on the "management" and "transfer" lines of the GPIB. An additional requirement for system communication is a mutual format for command and data bytes, to be transferred over the GPIB's data bus. The 405X translates BASIC commands into GPIB bytes of a machine language form which the 4907 can understand. However, the 405X's repertoire of BASIC commands does not include the special file management commands needed for the 4907, so a ROM pack firmware extender is provided (which plugs into the back of the 405X).

Power supplies for logic circuits and disc drive are located on the 4907 Power Supply Board. An identical supply is also contained in the auxiliary cabinet.

SYSTEM ADDRESSING AND MEMORIES

The Motorola 6800 MPU uses 64K of address space to access the read only memories (ROM), random-access memories (RAM), and peripheral/interface circuits in the 4907. The memory map (Figure 6-2) shows how the addresses are allocated among memory and peripherals. The lower 16K bytes (X'0000' through X'3FFF') are dedicated for system RAM devices. The upper 48K bytes (X'4000' through X'FFFF') are used for ROM devices and peripheral interface circuitry.

(1)The Option 5 module for the 4014 Option 40/41 allows a 4014 terminal to replace the 405X in a 4907 File Manage System.

(2)General Purpose Interface Bus: IEEE 488,1978 (see Section 4).

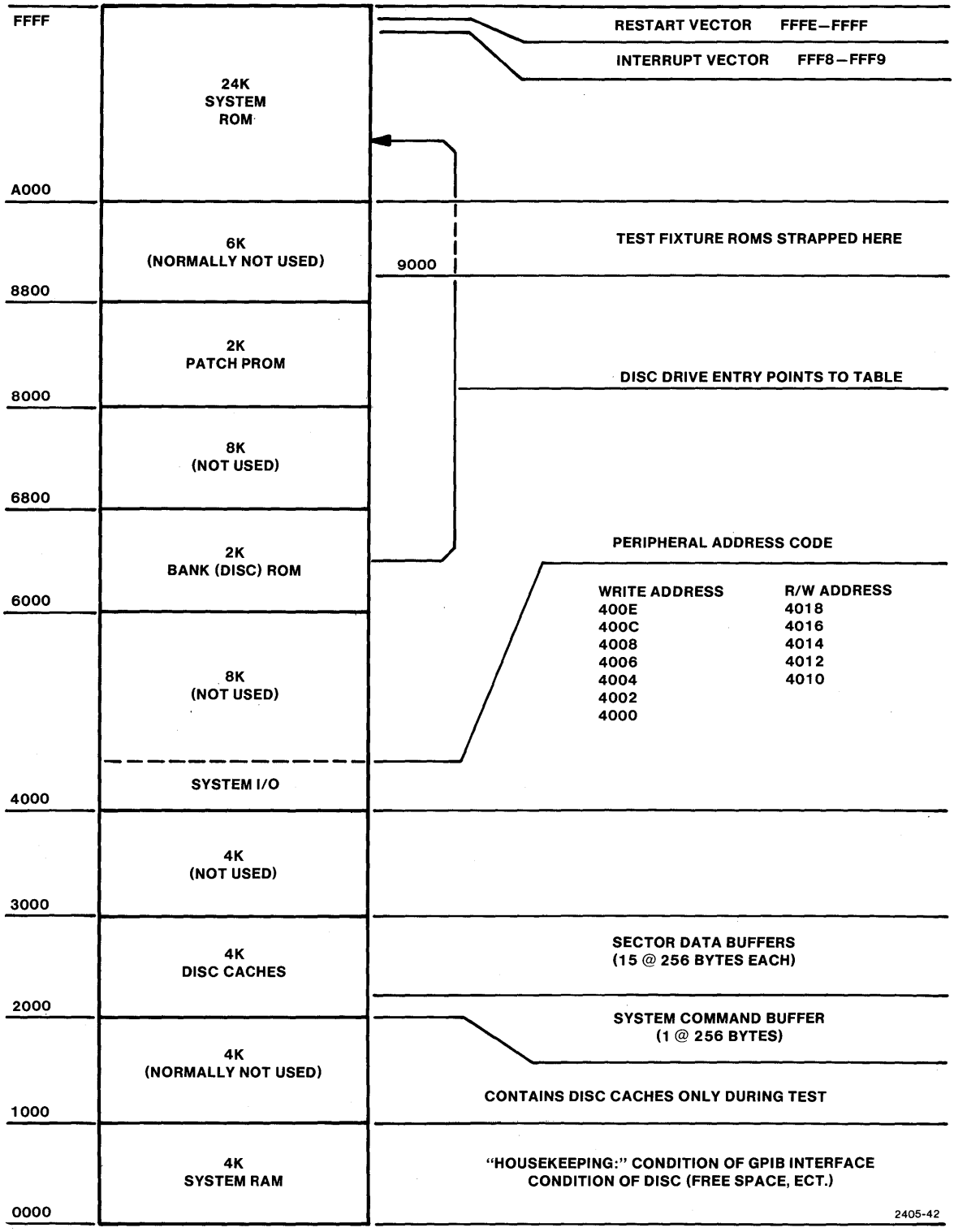


Figure 6-2. System Address and Memory Map.

The lowest 4K of RAM (X'0000' through X'0FFF') is designated system RAM. This part of memory is reserved for general "housekeeping" type activity: condition of the discs (free space, bad blocks, etc.) and condition of the GPIB interface.

The upper 4K of RAM (X'2000' to '2FFF') contains 16 buffers for temporary data and command storage. The first of these 256 byte buffers is used exclusively for storing system commands. The other 15 buffers, called "disc caches," contain the sector data of the most recent reads from the disc. Such a system allows this data to be accessed from the cache buffers rather than going back to the disc again, thus saving time. Each time a sector is read from the disc, its data is stored in the highest priority (front) cache. With each successive read, this buffered data is shifted back to the next lower priority. When the caches are full the oldest data is overwritten by the new data. If data that is already stored in cache is requested, this buffer then goes to the front of the chain. In all cases the most recent read, whether from the disc or a cache, resides at the front of the priority list. This logical description implies that data is shifted around from buffer to buffer; in actuality the 15 caches are readdressed by the firmware to prioritize them.

The portion of address space between X'4000' and X'5FFF' is used for accessing peripheral and interface circuits. The 4907 uses discrete logic, instead of monolithic P.I.A.s, for decoding the peripheral addresses. The GPIB interface, disc interface (SSDA, etc.), and indicator lights are accessed by addresses between X'4000' and X'4018'. See Hardware Address Table (Appendix D).

The 4907 firmware is located on a ROM board at addresses X'6000' through X'FFFF'. The 2K of address space at X'6000' through X'67FF' is used for GPIB and disc interface control. The first part of this space contains entry points for vectors to subroutines and programs in the system firmware. The 24K of system firmware is located at the top of the address structure, from X'A000' through X'FFFF'. If firmware correction is later needed, this may be implemented by using an FPLA (field programmable logic array) to intercept addresses which are then routed to a patch ROM inserted at X'8000' through X'87FF'. The FPLA is described in the ROM Board Theory of Operation (later in this section).

DATA ORGANIZATION ON THE FLEXIBLE DISC

The flexible disc media, also called a "floppy disc" or "diskette," is comprised of a thin, flexible plastic disc coated with magnetic oxide. The round disc is permanently enclosed and protected by a square, hard paper jacket. The magnetic disc is visible through holes in the jacket provided for indexing and read/write access.

The 4907, through its disc drive, records data on the disc at addressed locations, in a track/sector format. Given the address of data on the disc, the read/write head quickly locates and retrieves the desired data in a random access fashion. As the disc spins, serial binary data is recorded or read on concentric circles called tracks. Figure 6-3 shows track 00 on the outer edge of the disc; the innermost track is track 76. Each of the tracks is divided into 32 sectors, with each sector marked by boundary holes punched in the disc. An additional hole, INDEX, is positioned approximately 180 degrees before sector 0. Each track starts with a pulse initiated by a sector hole. The location of a sector is found by comparing the position of its sector hole with that of the Index hole (as sensed by the Index/Sector detector LED) Notice that the physical length of sectors varies directly in proportion to the distance of the track from the center of the disc; data bits are closer together on the higher numbered tracks. Given this organization each track contains 32 sectors of 256 bytes--8192 data bytes per track. With 77 tracks, there is room for 630,784 data bytes per disc.

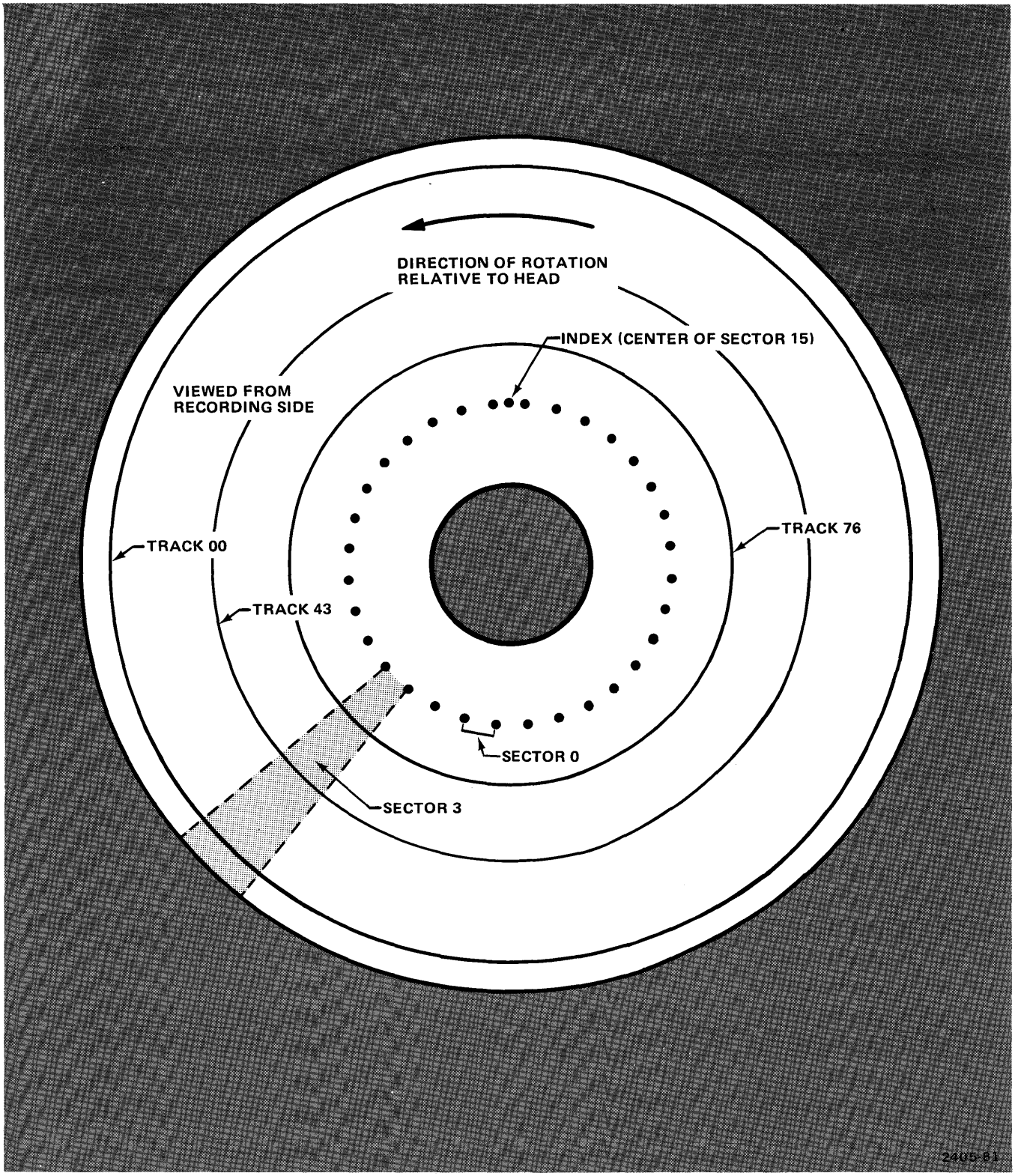


Figure 6-3. Flexible Disc Track and Sector Locations.

Sector Data Structure

Information stored on the flexible disc is contained in uniquely addressable physical units called sectors. Each sector contains format (address), data, and check space, as indicated by Figure 6-4. The sector begins with a preamble, which allows for timing and speed variations in the disc drive. This preamble contains 32 bytes, all zeroes. A one-byte sync character, with value X'01', follows immediately after the preamble. The header character that follows next contains two bytes of address information (including a parity check bit). Both sector and track addresses are coded into the header as indicated in Figure 6-4. The data space that follows next contains 256 bytes.

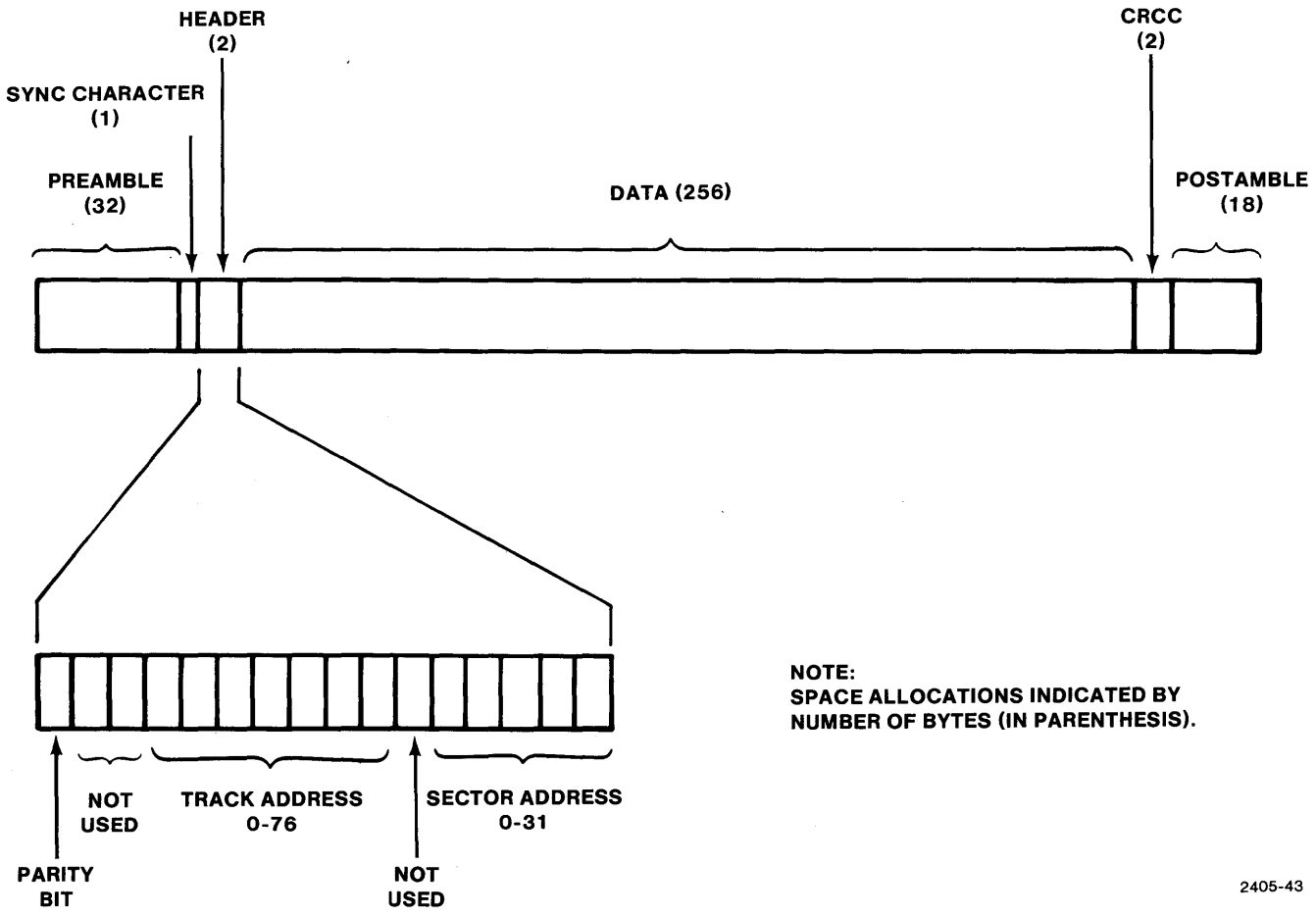


Figure 6-4. 4907 Disc Sector Format.

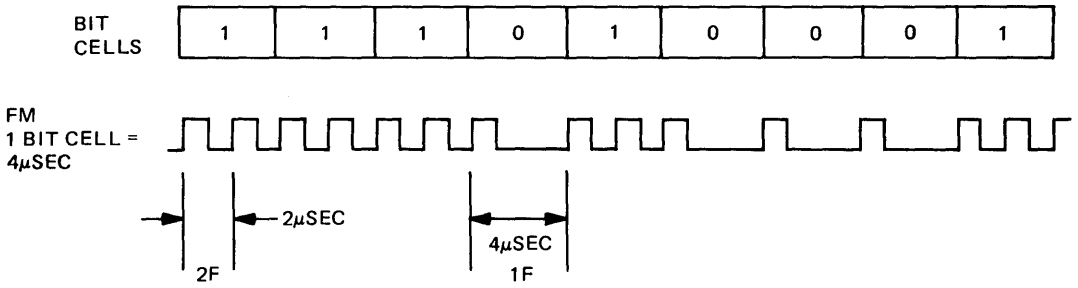
The data space is the only part of the sector accessible during normal I/O operation. The header is used in normal operation to verify the physical position of the disc (relative to the R/W head).

The system firmware programs arrange the physical data sectors into logical files for the most efficient use of disc space and in accordance with the 4907 library/file structure.

After the data bytes are written, the disc interface hardware automatically inserts two error-checking bytes, which form the cyclic redundancy check character (CRCC-Code 16 FWD). This character is developed from the bit pattern of the sector's data bytes and is used to detect errors after reading back the data from the disc. The sector ends with a postamble of 18 bytes, all zeroes. This postamble serves as a buffer between the next sector; and it also allows some blank time so the CRC can complete its work without interference.

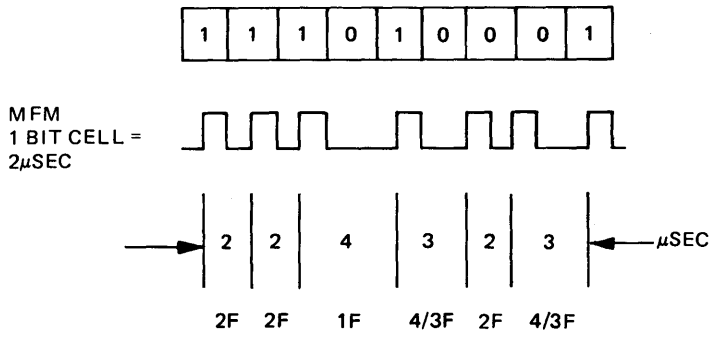
MFM Disc Encoding Format

The 4907 incorporates a disc encoding system called MFM (modified frequency modulation), which allows twice the storage capacity of the usual (frequency modulation or FM) encoding method. The drive unit produces flux reversals on the disc by changing polarity (north-to-south or south-to-north) of the field applied by the write head. Looking at the FM system (see Figure 6-5A) a clock flux reversal marks the beginning of each bit cell, which is 4 usec long. An additional flux reversal between clocks indicates a data bit "one" in this cell. Conversely, a "zero" bit call has no flux reversal between clocks. By comparison, the MFM system retains the one-zero coding but omits the automatic clocks in each cell. Instead, a clock reversal occurs only when two or more zeroes follows in succession; clocks are inserted at the boundaries of these adjacent zero cells. Also, as in FM, a reversal occurs for every one cell (see Figure 6-5B). By eliminating clocks where data reversals exist, the bit cells can be 2 usec long--half the space needed for FM encoding. This effectively doubles the storage capacity of the MFM encoded disc.



A: FM Encoding

A flux reversal occurs in the center of every bit cell containing a ONE.
A flux reversal occurs at the leading edge of every bit cell containing a ZERO.



B: MFM Encoding

A flux reversal occurs at the leading edge of every bit cell containing a ONE.
A flux reversal occurs between two adjacent bit cells containing ZEROS.

NOTE:
In MFM, the write oscillator frequency is doubled, while maintaining the same flux changes per inch as FM. Thus, the bit cell in MFM is ½ that in FM. Data transfer rate is also doubled, since a 1 to 1 relationship exists between flux changes per inch and bits per inch (2 to 1 in FM).

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Figure 6-5. Flexible Disc Encoding Formats.

Write Pre-Compensation

The 4907 incorporates a scheme for adjusting flux reversal locations to maintain a uniform timing of read pulses; this system is called write pre-compensation. It is normal for magnetic flux reversals to relax (move) to a stable location shortly after they are written on the disc. The extent and direction of these reversal movements depends on the pattern of adjacent zero/one bits in the write stream. There are many bit combinations that cause a shift, but only the worst cases require compensation in order for the read head to sense the reversal where it expects to find it. The Write Pre-Compensation circuit, ROM U425, looks at the serial bit patterns before they are written on the disc. Then it adjusts the write times by plus 250 nsec, minus 250 nsec, or none, depending on the bit pattern. The resulting reversals will finally relax into the uniform bit cell spaces.

This relaxation movement problem is more noticeable where bit cells are closer together, as on the inner tracks of the disc. Tracks 00 to 41 do not require this compensation, so we only enable the Write Pre-Compensation circuit for the area above Track 41. This is controlled by the AT-41 signal.

CONTROL BOARD CIRCUIT BLOCKS

The remaining part of the theory of operation consists of functional block descriptions of the three boards in the 4907. The largest board, and the first to be discussed, is the Control Board. A block diagram illustrating the various functional units within the Control Board is located on a pull-out sheet in Section 8, Schematics. The operating theory of each of these circuit blocks is described in the following text.

A ROM Board, ROM Pack, and Power Supply Board description follows the Control Board discussion. (A small piece of power supply circuitry is located on the Control Board; this is described in the Power Supply Board section.) The circuit board in the disc drive unit is described in the 119-0977-00 Flexible Disc Drive Instruction Manual.

Clocks and Timing

The clock circuit provides all of the timing signals needed by the MPU and peripheral blocks. This circuit is found on schematic sheet 1-1. A timing circuit block diagram is illustrated by Figure 6-6 and is treated in the following text.

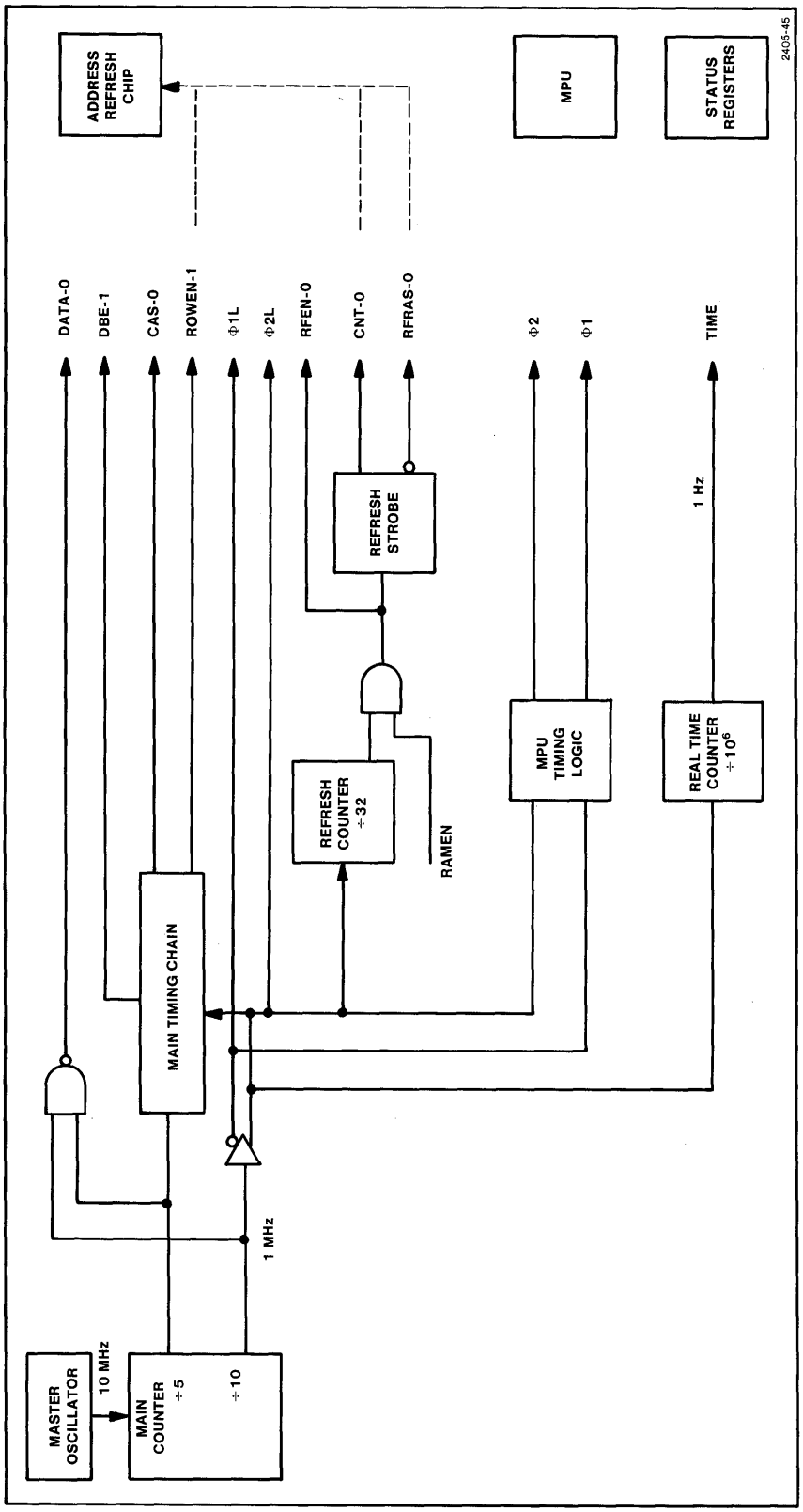


Figure 6-6. Timing Circuits Block Diagram.

Master Oscillator and Counter

The master oscillator is a 10MHz crystal-controlled circuit. Crystal Y505, with the appropriate feedback components forms a series resonant oscillator. Its output feeds a counter (U407) with divide-by-five and divide-by-ten outputs. The divide-by-ten output is the basis for the two-phase clocks. The divide-by-five signal feeds the main timing chain circuit. Also, the divide-by-five and -ten signals are NANDed by U411 to produce DATA-0, which is used by the write only registers.

Two-Phase Clocks

The 1 MHz, 1us, output of U407 enters a driver, U409A, with complimentary outputs. These phase one and phase two outputs pass through a conditioning circuit before entering pins 3 and 37 of the MPU. This MPU timing logic block conditions these clocks, so there is no overlap of their "high" states and so their edges (transistions) have sufficiently fast rise and fall times.

This conditioning is done by set-reset flip-flops comprised of two gates followed by inverting circuitry. The gates prevent Φ1 from going high until I2 has gone low, and vice versa. Timing signals needed for the system test fixture are extracted in front of the conditioning circuit and are called Φ1L and Φ2L. Also, a Φ2L signal drives a divide by 10 6 counter which sends a 1 Hz signal (TIME-1) to the real time counter, U341 (in the interrupt/status circuits).

Main Timing Chain and Refresh Clock

The divide-by-five output of counter, U407, feeds a series of flip-flops and gates called a timing chain. This block of circuitry produces the following timing signals: DBE-1 (data bus enable), CAS-0 (column address strobe), and ROWEN-0 (row enable). The Φ2 clock is used to synchronize the flip-flops in the chain.

The remaining refresh and memory clocks are produced by the refresh clock circuits. The Φ2L signal passes through a divide-by-32 counter, then is ANDed with the RAMEN signal from the address decoder, U207.

This AND gate is enabled when refresh is requested, if the read/write memory is not in use.

When the gate is enabled the RFEN-0 (refresh enable) line goes active low. The same signal also feeds the refresh strobe circuit, U417; its complementary outputs are: CNT-0 (control) and RFRAS-0 (row address strobe).

Figure 6-7 is a timing diagram showing the relationships between the main timing signals in the 4907.

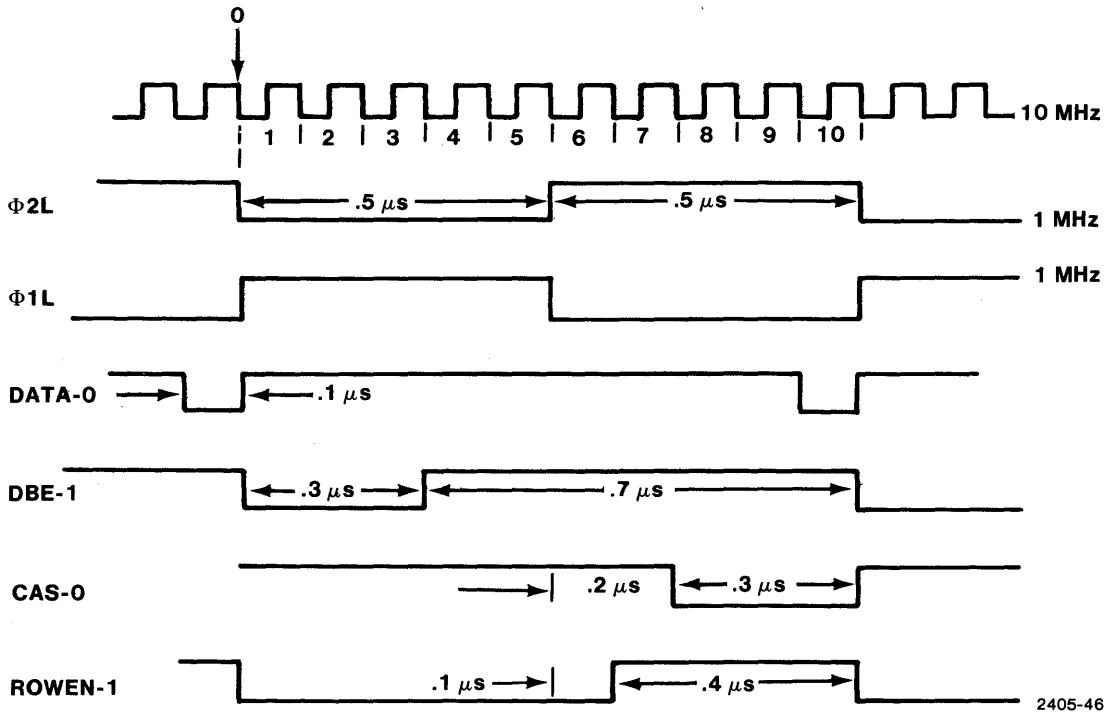


Figure 6-7. Main Clocks Timing Diagram.

Microprocessor Unit (MPU)

The MPU block (schematic 1-2) consists of the Motorola MC 6800 microprocessor and its address and data bus buffers.

The MC 6800 microprocessor follows instructions stored in ROM and acts on signals sent from other parts of the 4907, or from the outside world via the GPIB. It issues commands to the various parts of the 4907 (and auxiliary drive units) causing drive unit selection, R/W (read/write) head movement for track selection, reading or writing data to or from a disc, and sending or receiving data on the GPIB. The MPU uses the Φ1 and Φ2 clock signals to time its internal operations, as well as to synchronize these operations with the rest of the 4907's circuitry.

From one perspective, the MPU is performing a variety of control tasks for the 4907. However, to the MPU, it is merely looking at instructions (one to three bytes long) and passing data to and from memory locations. The 6800 is called a memory oriented machine, because it sees its peripheral address decoder and interfaces, as well as RAMs and ROMs, as memory.

The MPU communicates with its memories via various signal lines, grouped functionally into three "busses": the Data, Address, and Control busses.

Data Bus

The Data Bus, lines DB0 to DB7, carries bytes of data between the MPU and its memories. Since the MPU's data pins D0 to D4 are limited in their drive capability, a pair of "data bus transceivers" interface the 6800 to the data bus. These transceivers, enabled by the MPU's R/W signal (pin 34), will only drive the control board data bus during a write cycle.

Address Bus

The address lines A0 to A15 interface the MPU to the control board address bus through tri-state buffer-drivers, U301 and U302. These buffers store the last address presented by the 6800 and provide the needed driving capability.

Control Bus

The Control bus is the set of lines which control the flow of addresses and data over the other two busses. These control lines are:

- R/W (same as RWOC for Read/Write Open Collector). This signal tells whether data is to be read from, or written to, a memory location. It may be pulled low by an external system test fixture or by the MPU.

- HALT-0 stops the MPU for a Direct Memory Access (DMA) operation. It is used by the System Test Fixture only.

- VMA (Valid Memory Access) indicates the availability of a valid memory address on the address bus.

- BA (Bus Available) is used with VMA to enable the RAM Address Decoders. ENABLE = VMA + BA

  BA goes high in response to a HALT-0 input, after the MPU has stopped. This indicates that address and data lines from the MPU are in a tri-state (disconnected) condition, and these bus lines may be driven by a DMA device.

- Φ2L (Phase Two Clock) is used to time memory access operations.

- RESET, initializes MPU and decoders on power-up and power-fail. Initialization causes the MPU to fetch the starting address of the control program and resets the status and interrupt registers.

- IRQ (Interrupt Request) is used by peripheral devices to notify the MPU of their request for service.

- NMI (Non-Maskable Interrupt) is not used by the 4907.

Figure 6-8 is a functional block representation of the circuitry within the 6800 MPU. The following discussion examines briefly the internal operating patterns in the MPU.

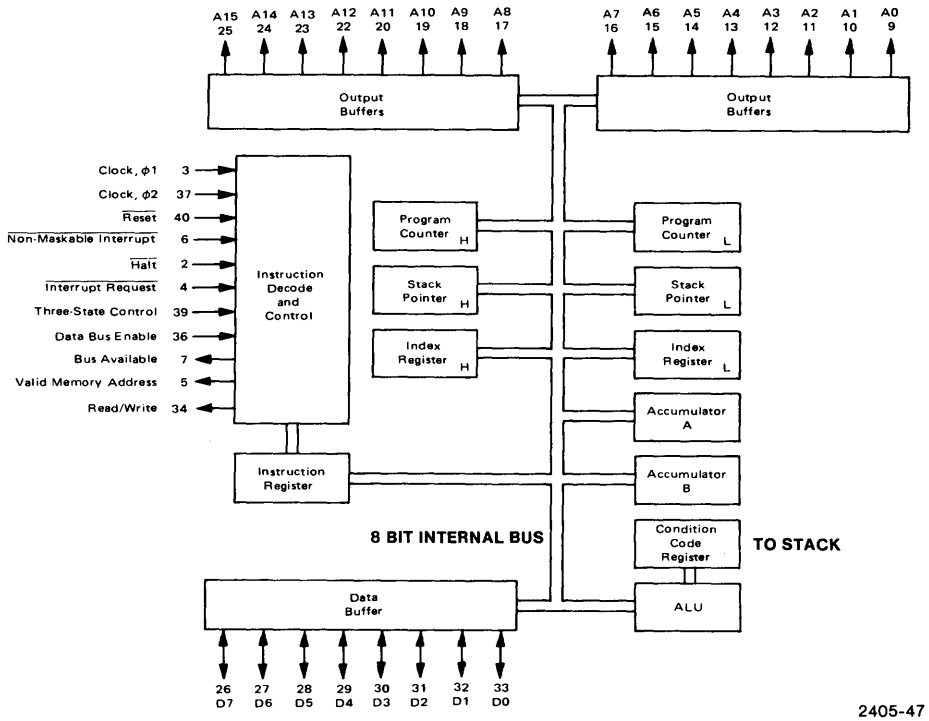


Figure 6-8. MPU Internal Block Diagram.

Consider a typical three-byte instruction which loads data from the disc into the MPU's Accumulator A. The first byte activates the required series of internal microcodes, which initially opens Accumulator A. The next two bytes follow with the address of the "memory" (disc interface) where the desired data is located. The address bus then contains the address of that memory, and the interface responds by placing its data contents on the data bus. Finally, the MPU places this data in Accumulator A, and looks at the next set of instructions coming in on the data bus.

Many instructions will address a portion of firmware in ROM, which will then feed more instructions back into the MPU.

The MPU keeps track of progress through instruction sets with the program counter. Often this information and the condition codes need to be retained and stored outside the MPU, so a stack is created in RAM. The stack pointer contains the address of the top of this stack, so the MPU can fetch this information later.

Read/Write Memory

A general overview of the 4907 address structure is found at the beginning of the Theory of Operation Section.

The 4907's read/write memory is comprised of an 8K RAM arrangement (refer to schematic page 1-3). The RAM, together with its address decoder and parity check generator, comprises a functional grouping. The diagram in Figure 6-9 shows this grouping with its component blocks. The physical operation of the read/write memory's component blocks follows under subheadings. The relative location of the read/write memory in 4907's address structure and the logical arrangement of its 8K memory are discussed earlier in this section under "System Memories and Addressing".

RAM Structure

The 4907 RAMs consist of 4K by 1 bit chips arranged in two banks of nine. Each bank of nine chips provides a 4K storage, one chip for each of the 8 data bus bits and one chip for a parity bit. The lower 4K of memory consists of U107 through U123; the upper 4K, of U125 through U141. U107 and U125 store the parity bits.

The non-parity RAMs place their data on the data bus through tri-state buffer drivers, U234A through U234H.

To find a specific memory location, the MPU first selects the particular RAM bank; then it sends a row address and a column address. The RAMs have one address bus, which is switched between the row and column addresses. The CAS-0 (column address strobe) and RAS-0 (Row Address Strobe) inputs tell the RAMs whether an address is for columns or rows.

RAM Refresh

The RAM Refresh block (U103) contains both refresh counter and multiplex functions. This block, along with the Enable Gates, implements the control of the RAMs during read, write, and refresh.

Figure 6-9 shows the three-way multiplexer in the Refresh block. The Multiplexor switches the RAM address bus between the row address lines (AB 0-5), the column address lines (AB 6-11), and refresh. The switch, control lines, RFEN and ROWEN, determine which input bus is selected. If RFEN and ROWEN are both high, the Row address lines are selected. However, anytime RFEN goes low the column/row selector is over-ridden, and refresh is selected.

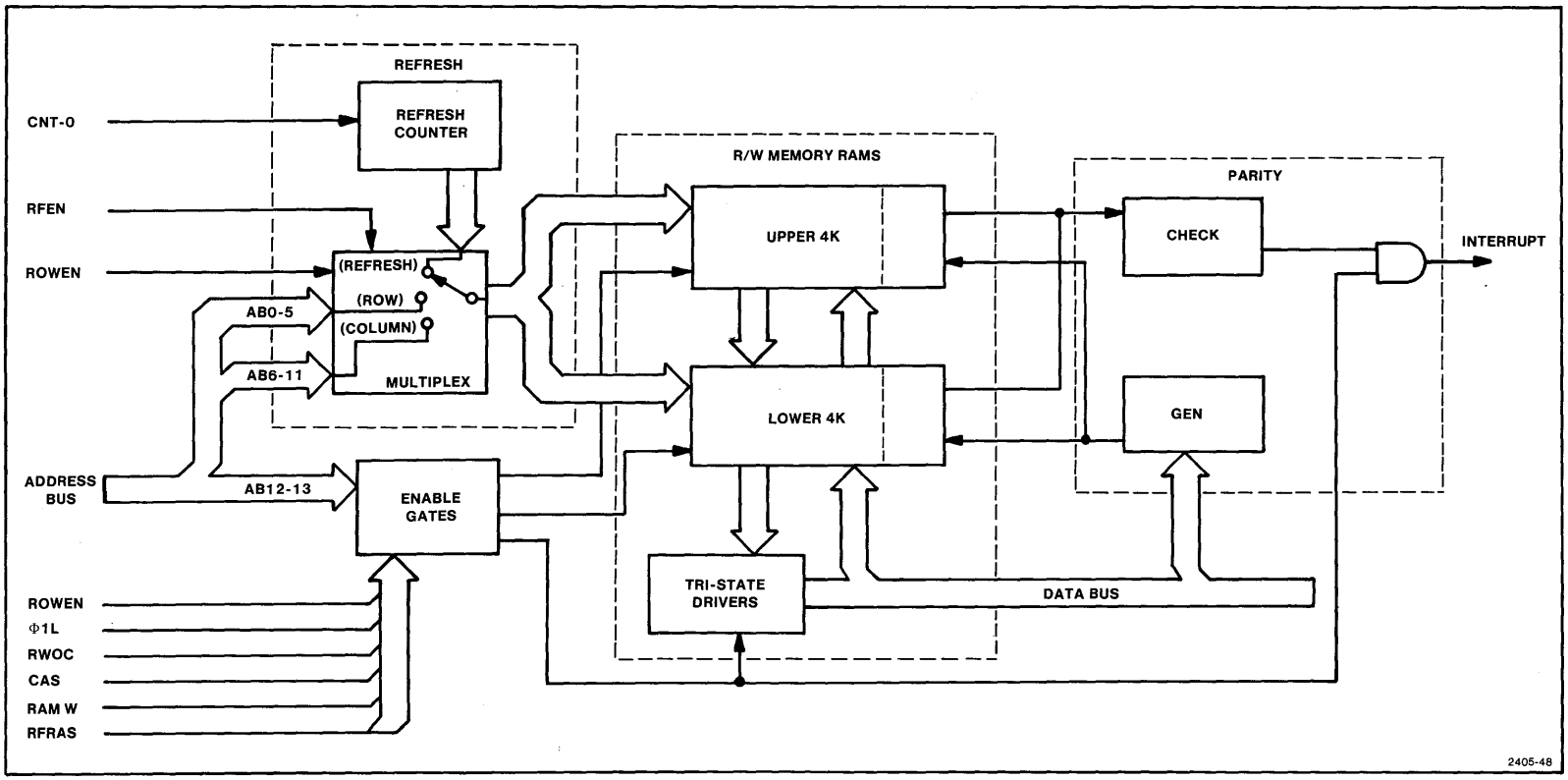


Figure 6-9. R/W Memory Block Diagram.

The Refresh Counter part of this block contains a six-bit binary counter which keeps track of the location in RAM to be refreshed next. At the end of a refresh cycle, the CNT-0 line is pulsed low to increment the counter. The counter then contains the address for the next refresh cycle. This address will be requested every 64 usec.

Enable Gates

The section of circuitry called Enable Gates combines address signals and control signals to enable the appropriate RAM banks, tri-state output driver, and parity output. The address lines 12 through 14 pass through a 3 line to 8 line decoder, U207. (This is actually part of the Peripheral Address Decoder circuitry and is treated later in detail.) The upper and lower RAM banks are addressed by the decoder outputs Y/0 and Y/2, respectively. Figure 6-10 represents this functional block.

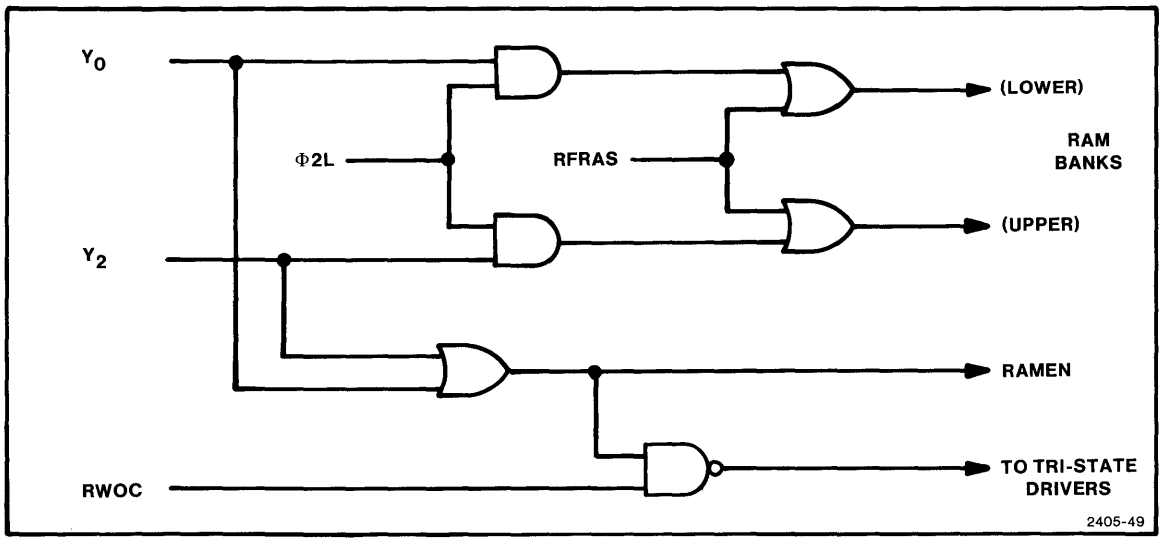


Figure 6-10. Enable Gates Diagram.

The Y/0 and Y/2 outputs are first ANDed with the Φ1L-0 (or Φ2L-1) system clock and then ORed with the RFRAS (Refresh Row Address Strobe) signal. In addition, Y/0 and Y/2 are ORed to produce RAMEN for the system clock. RAMEN is further ANDed with the RWOC signal to give the proper enable for the tri-state RAM driver and parity check output.

The other enable lines are not gated. The CAS (Column Address Strobe) and RAMW (RAM Write) signals enter RAM chips directly, and ROWEN (ROW Enable) enters the refresh chip directly. Figure 6-11 shows the timing of these various clocks for read, write, and refresh operations.

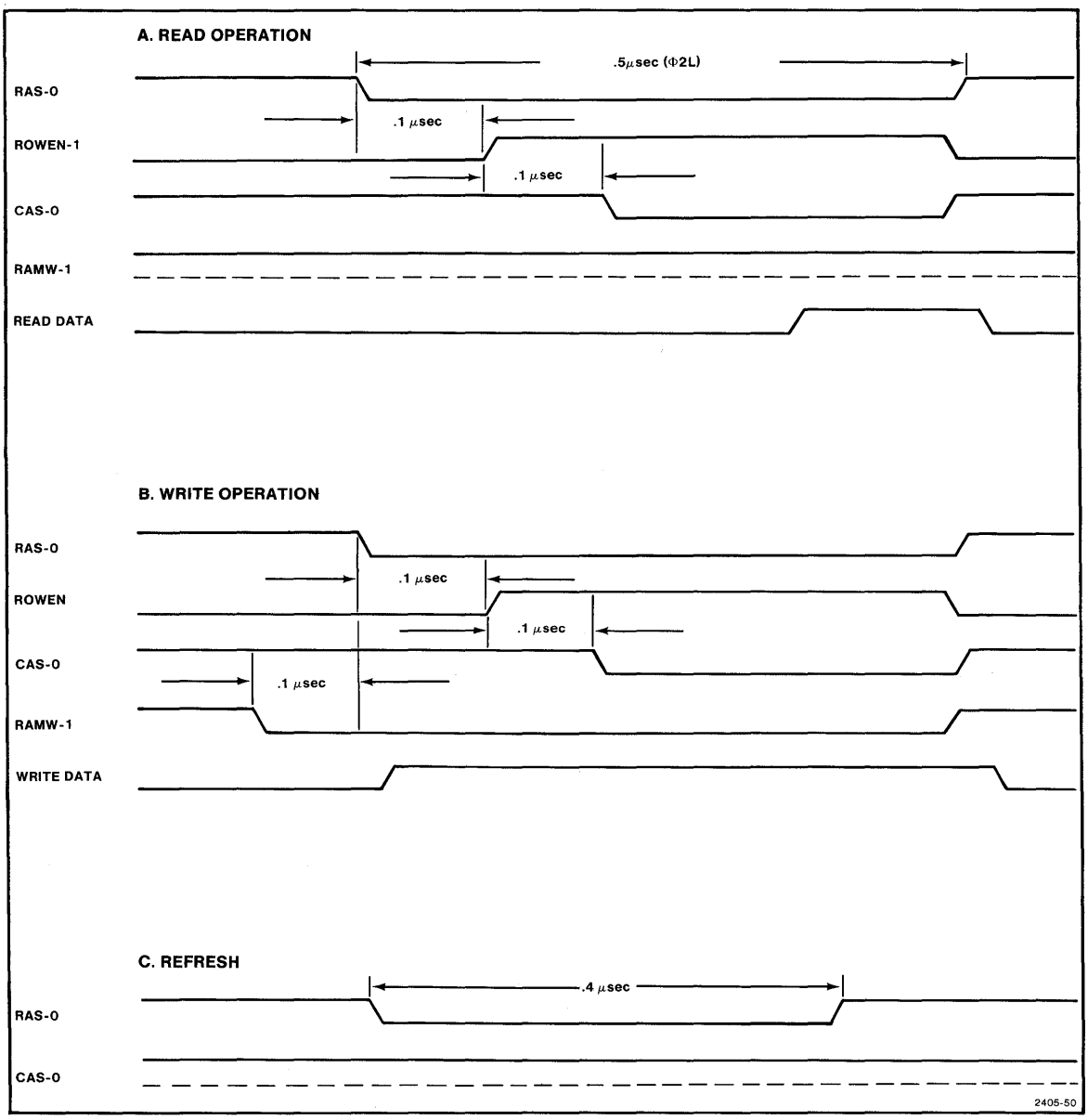


Figure 6-11. Memory Timing Diagram.

Parity

A Parity-type error check accompanies all data transfers from RAM to the microprocessor. When data is read off the data bus into RAM, it is simultaneously analyzed by the parity circuit. The parity generator contains a series of cascaded exclusive OR gates, which tells if the sum of the 1 bits from the 8 data lines is odd or even. The parity generator adds a 0 or 1 bit, as needed, to make the sum even. This parity bit is then stored next to the data in its separate RAM bit column (U107 or U125).

When the data is read back from RAM it passes through a similar device which exclusive-ORs the data bits again, but this time it adds in the parity bit making the sum odd if all bits were read correctly. If a bit is in error, the parity checker will generate an even sum, and this error condition will be stored in the interrupt register. See the Parity Circuit Block Diagram in Figure 6-12.

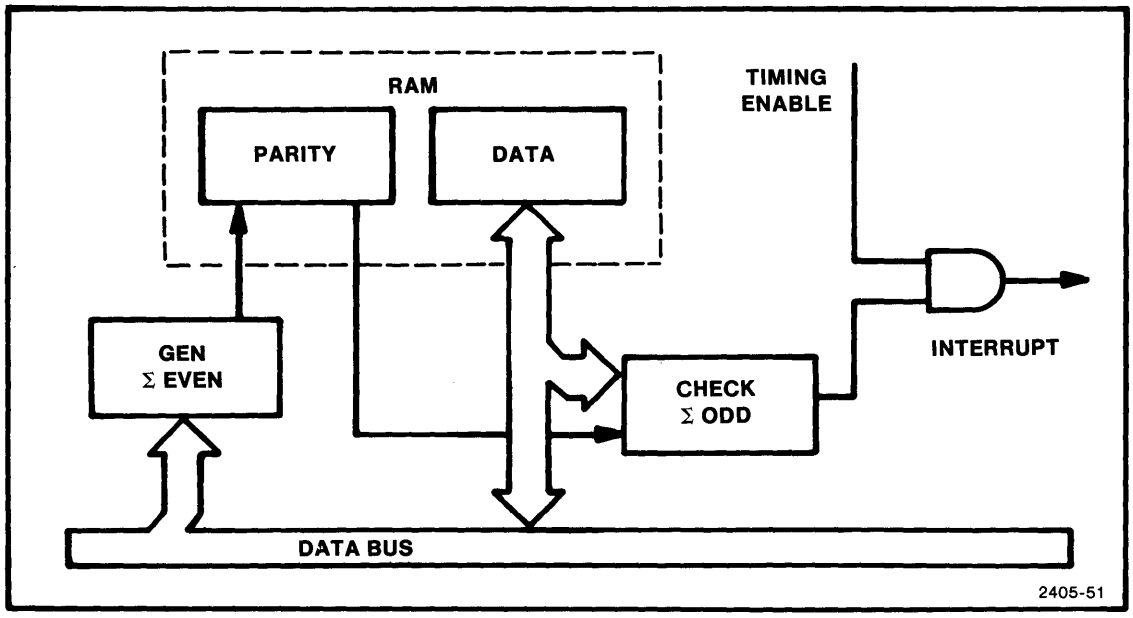


Figure 6-12. Parity Circuit Diagram.

Peripheral Address Decoders

In addition to the RAM address decoding there are additional decoding circuits to address the MPU's status and control peripheral blocks. These peripherals are addressed by 3 line to 8 line decoders using address lines AB1 through AB4 and AB12 through AB15. The block diagram in Figure 6-13 represents this decoding circuit. The address space X'4XXX' (from address lines AB12 to AB15) is first preselected by decoder U207.

The Y/4 output of U207 then enables the read and write peripheral decoders. These 3 line to 8 line decoders run off of address lines AB1 to AB3. The first decoder, U217, provides the signals which enable the read only peripherals and the SSDA (the only read-write peripheral). The only enable for this decoder is AB4, which must be high. The second decoder, U219, accesses the write only peripherals and requires additional timing and enable gates. For instance, the AB4 address line is ANDed with a timing signal DATA-0, thus limiting write peripheral operation to the last 100 nanoseconds of Φ2. Also, the Y/4 address enable line from U207 is ANDed with a control signal, RWOC-1, from the MPU. This signal tells the decoder whether the MPU is in a read or write operation -- a high signal indicates an MPU read cycle.

Front Panel Indicator Lights

The first of the major peripheral blocks is the front panel indicators. The four indicator lights are all LEDs and are designated "busy", "file open", "fault", and "clock." These lights are driven by a control latch, U305. See Schematic sheet 1-5. The latch's inputs are connected to the MPU's data bus lines DB0 through DB3. (Lines DB4 and 5, pins 13 and 14, are not used.) Upon receipt of a clock-enable WP0 from the peripheral address decoder, the information on the data bus is held or latched into the chip. The "flag" (data bit) then appears on the corresponding output (D1 to Q1, D2 to Q2, etc.). The LEDs are then connected via buffers and current limiting resistors. A SYSRS-0 signal is placed on the inverting input, pin 1, of U305 when the 4907 restarts after power failure. This turns all the lights off, waiting for initialization of the system.

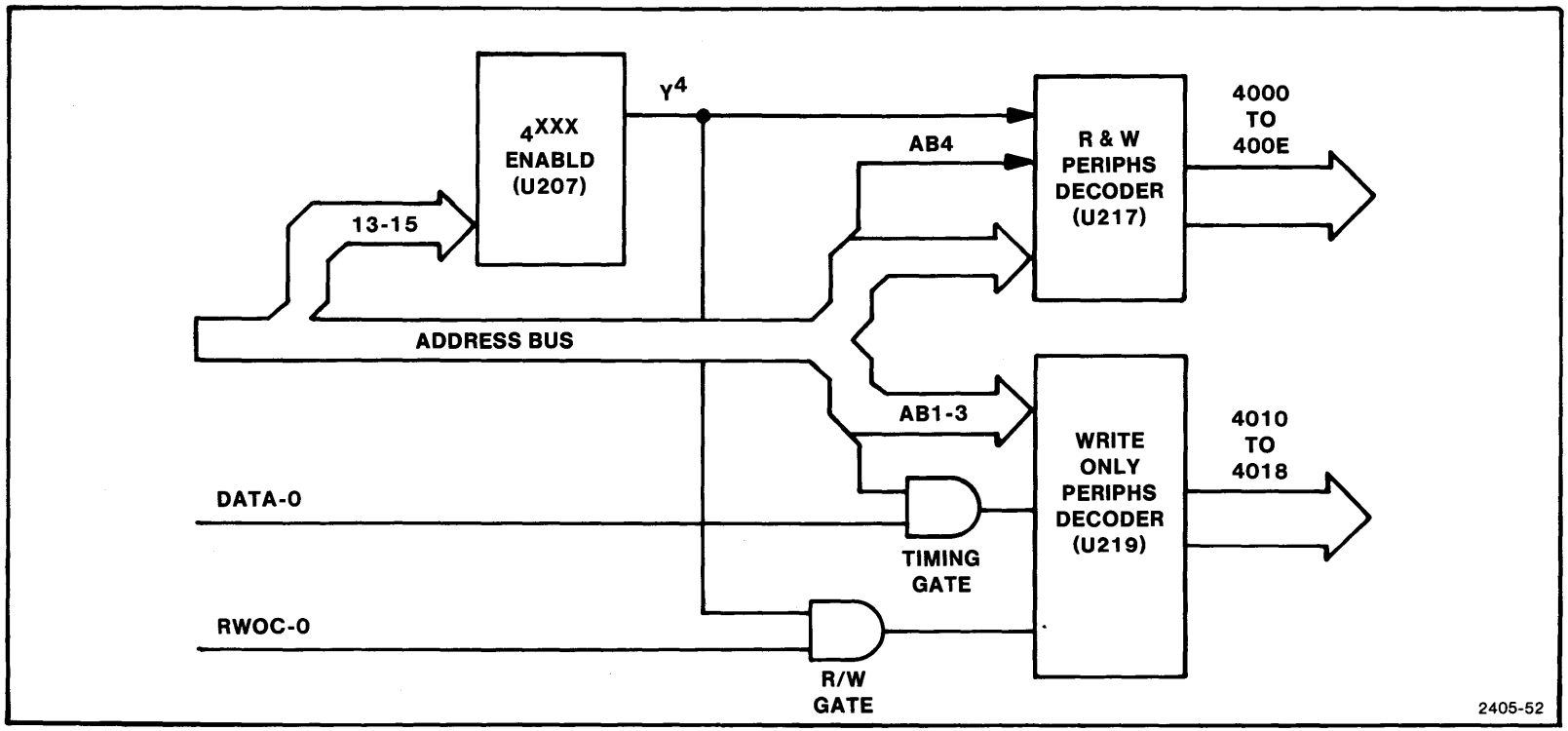


Figure 6-13. Peripheral Address Decoder.

Status/Interrupt Registers

The microprocessor is subjected to peripheral status and interrupt reports. The 6800 MPU receives this status information via its data bus, and is interrupted by control bus signals (namely IRQ). The status/interrupt information comes from peripherals of the MPU. This information is then stored in the designated registers, whose outputs may trigger an MPU interrupt. These outputs are also placed on the data bus, via buffers, so the MPU can read the status of the registers at any time.

Figure 6-14 shows the processing of the seven status/interrupt signals in this circuit block. Three of the lines come from the GPIB section: DBIFCLR-1 (interface clear), DBHAND-1 (handshake), and DBATN-1 (attention). A 1 Hz clock signal, TIME-1, and parity check are also monitored by these registers. The TOUT-1 (time out) and INDEX-1 signals are related to disc drive operation. TOUT is a 10 msec delay timing signal that paces disc operations such as head loading, stepping, and reading data from the disc. The INDEX signal is sent to the index register when an index pulse is received from the disc. Notice that the register's INDEX output is not connected to the interrupts, since it is only a status line. Consequently, it connects only to the status buffer and data. (The other register outputs are also connected to the data bus.)

The five outputs, excluding TOUT and INDEX, are ORed together and then enabled by an interrupt mask gate. When the firmware instructs the MPU to ignore these five interrupts, the MPU sends INTMSK-1 (via DB7-1 and WP2-0) to the mask AND gate U327C. The TOUT signal ignores the MPU's interrupt mask signal. The outputs of TOUT and the mask AND gate are finally ORed to produce the IRQ line going to the MPU.

These registers store the interrupt/status bits until they are reset by the microprocessor. To reset, the MPU first addresses the write peripheral decode, U219; the decoder's Y/4 output then enables the reset NAND gates. Next the MPU sets the appropriate data bus lines which pass through the NAND gates, finally resetting only the registers it wants to clear.

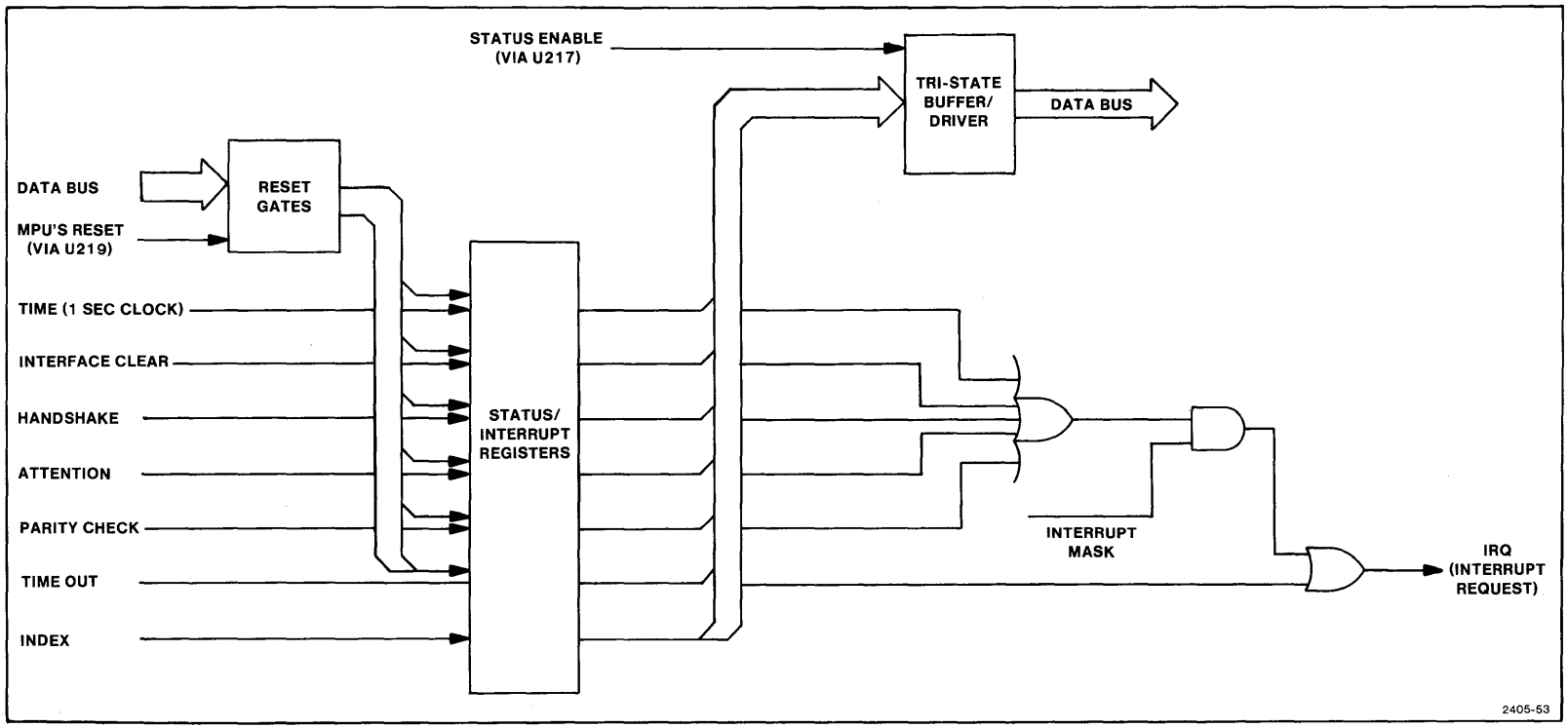


Figure 6-14. Status and Interrupt Registers Diagram.

GPIB Interface

The GPIB Interface (on the Control Board) interfaces between the General Purpose Interface Bus and the 4907's microprocessor. Figure 6-15 shows the entire Interface block subdivided into functional sub-blocks. The GPIB Interface includes:

- Control Register
- Address/Status Latch
- Bus Handshake Transceiver
- Management Bus Transceiver
- Bus Handshake Steering
- Data Bus Interface
- Listen/Talk Steering
- Debouncers
- "Hello" Circuit
- Hand Gating
- Source Handshake Circuit
- Acceptor Handshake Circuits (AH1 and AH2)
- AH Enable

Before reading the GPIB Interface circuit descriptions, be sure to read Section 3, which describes the GPIB's functions.

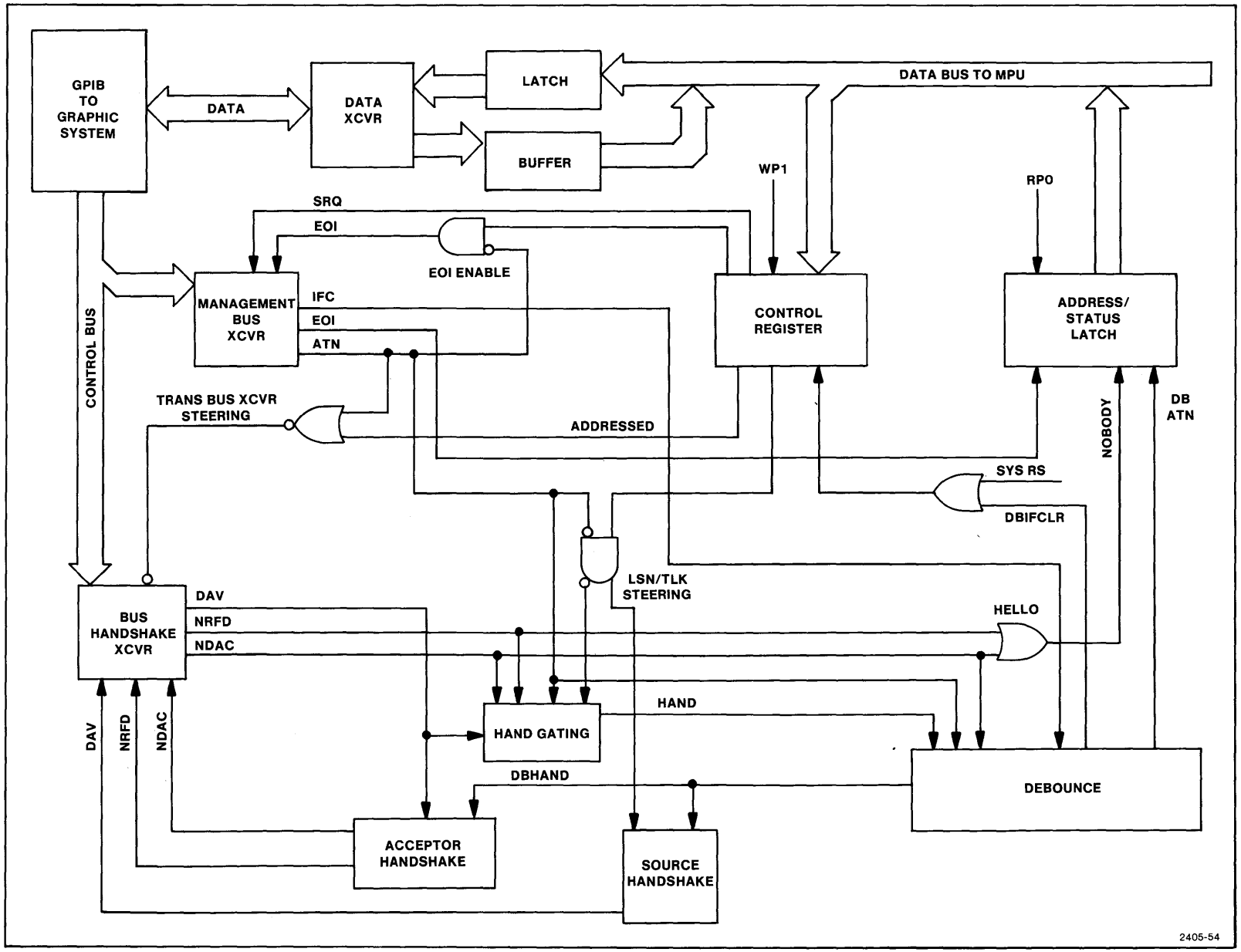


Figure 6-15. GPIB Interface Blocks.

Control Bus Interface

Bus Handshake Transceiver. The Bus Handshake Transceiver provides interfacing to the three GPIB handshake lines DAV, NRFD and NDAC, and to one of the management bus lines, EOI. The transceiver's internal schematic is illustrated in Figure 6-16. Each input or receive port (such as A1) at all times follows the signal presented to the corresponding GPIB port (A). An output or transmit port (such as A0) drives the corresponding GPIB line only if the transceiver is enabled with a low. The GPIB ports are active-low to conform with the GPIB standard, while the receive ports and transmit ports are active-high.

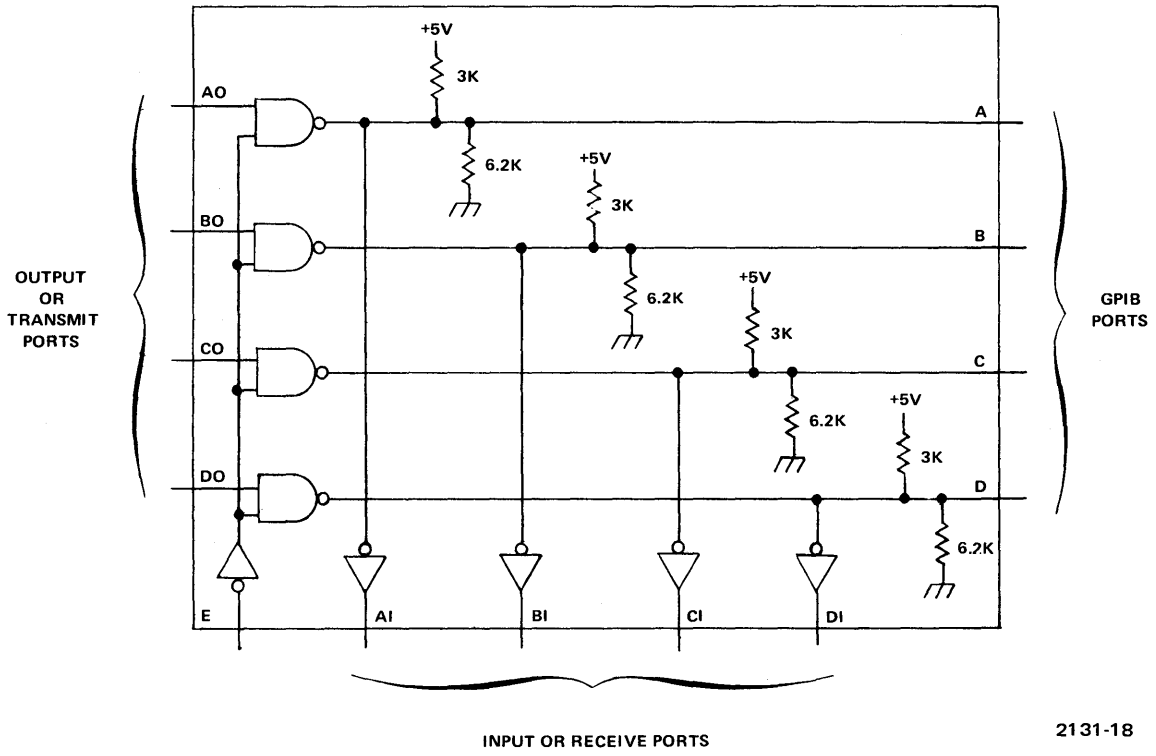


Figure 6-16. GPIB Transceiver Block.

Management Bus Transceiver. The Management Bus Transceiver, like the Bus Handshake Transceiver, is a type 3441 GPIB transceiver. Unlike the Transfer Bus Transceiver, it is always enabled to transmit. (Its enable input is grounded.) However, since the 4907 is not permitted to send the ATN, IFC or REN signals over the GPIB, the corresponding transmit ports (CO, BO, AO) are grounded. Any time that a high is presented at its DO port, however, it will transmit the SRQ (Service Request) message on the GPIB.

Bus Handshake Transceiver Steering. The Bus Handshake Transceiver is only enabled to transmit when the 4907 is to receive or send bytes over the GPIB. This occurs when the 4907 has been addressed as a "talker" or "listener", or when the controller is holding ATN active, commanding all GPIB devices to "listen" to the addresses or commands on the GPIB data bus. The Bus Handshake Transceiver Steering gate detects these two conditions (ADRS and ATN) and enables the Bus Handshake Transceiver when either of them occurs.

Interfacing the ATN Line. The ATN signal cannot be sent by the 4907; hence, the CO port of the Management Bus Transceiver is tied to ground.

When the ATN signal is received, it is fed from the Bus Handshake Transceiver's CI port to:

a. the Debouncers, which present a debounced version of DBATN to the status and interrupt register to tell if ATN is being asserted or if it is going away.

b. the Bus Handshake Steering, which enables the Handshake Bus so that "acceptor handshake" signals may be transmitted.

c. the AH Enable gate, which enables the Acceptor Handshake circuitry.

d. the Listen Talk Steering, which immediately disables the Data Bus Interface from talking.

When the MPU responds to the interrupt, it steers the GPIB Interface into "listen" mode (if it is not already in that mode), enabling the Data Bus Interface to pass the received byte onto the 4907's data bus.

As long as ATN is held active, the 4907 is in "listen" mode, receiving universal commands or device addresses from the GPIB controller. If the MPU, in receiving these bytes, recognizes its own talk or listen address, it causes the control register to send the ADDRESSED signal to the Bus Handshake Transceiver Steering gate. (Then, when the ATN line is released, the Bus Handshake Transceiver is still enabled to transmit.)

When the GPIB controller releases the ATN line, and DBATN signals this to the MPU via the IRQ line, the MPU follows any commands just given it by the controller.

Interfacing Other GPIB Management Bus Lines. The 4907 can send, but not receive, the SRQ message. The control register is used by the MPU to send SRQ which requests service from the GPIB controller. Since the 4907 may not respond to the SRQ message, the DI port of the Management Bus Transceiver is left unconnected. (Consequently, it is not even shown in Schematic 1-2.)

The 4907 cannot send the IFC (Interface Clear) message, so the Management Bus Transceiver's BO is tied to ground. When an IFC message is received, it is sent from the Management Bus Transceiver's BI port, through the Debouncer, to the interrupt register where it causes an MPU interrupt. It also clears the GPIB control register, forcing the Interface into the idle mode. (This interrupt informs the MPU that the GPIB control register has been set in the idle mode.)

The 4907 may neither receive nor send the REN message; so the Management Bus Transceiver's AO is tied to ground and its A1 port left unconnected.

When a series of data bytes is sent over the GPIB, the EOI (End Or Identify) message is used by the "talker" to mark the last byte in the data string. When acting as a "talker", the 4907 sends this signal from the control register along the TRANSMIT EOI line and through the Bus Handshake Transceiver out onto the GPIB. When the 4907 is a "listener", any EOI signal it receives will appear at the Bus Handshake Transceiver's DI port and be sent from there to the A1 status latch input.

Data Bus Interface

The Data Bus Interface, as its name implies, is an interface between the GPIB and 4907 data busses. It includes two GPIB transceivers similar to the ones used as the Transfer Bus and Management Bus Transceivers. The GPIB data lines connect to the two way ports on the transceivers. On the other side of the transceiver are one-way in and out lines to the 4907 data bus. These incoming one-way lines pass through a latch which stores the data on the 4907 bus when addressed by the MPU (WGPIB). The Talk/Listen Steering logic then send a "talk" signal by allowing the transceiver enable input to go high.

A "listen" (logic 0) signal on a transceiver enable allows the GPIB data to pass through to the one-way output ports. These output lines are then buffered to the 4907 data bus. The buffer is a tri-state device and is effectively disconnected from the bus until the MPU enables it with a "read" signal (RGPIB).

GPIB Control Register

The microprocessor controls the handshaking and steering circuits and sends SRQ and EOI messages to the GPIB via a five-line data register. The MPU enables the register by sending a WP1 (active low) via the peripheral address decoder. This places the contents of lines D0 through D4 on the register's outputs as SHAKE, ADDRESSED, EOI, SRQ, and LSN/TLK (respectively). The register may then be cleared by a SYSRS (system restart) or DBIFCLR (debounced interface clear) signal.

GPIB Address/Status Latch

The microprocessor reads GPIB status information from register U351. Three of the eight inputs are designated DBATN, EOI, and NOBODY, and come from the handshaking and debounce circuits. The five remaining inputs are connected to a five line rocker switch used to set the 4907's GPIB primary address.

Listen/Talk Steering

The Q5 output of the GPIB control register is sent low by the MPU when bytes are to be received over the GPIB; it is sent high when bytes are to be transmitted. The Listen/Talk Steering Circuitry consists of an AND gate, U409C, with inverting and noninverting outputs. This circuit uses the Q5 LSN/TLK signal and the ATN signal received from the GPIB as inputs, and provides outputs to steer various circuit blocks in the GPIB Interface between their "listen" and "talk" modes:

a. When the Q5 LSN/TLK line says "listen", or ATN is active, the Data Bus Interface's GPIB transceivers are disabled from transmitting. On "talk", with ATN inactive, they are enabled.

b. The Data Bus Interface includes separate "talk" and "listen" buffer/latches, which are in separate paths and therefore always enabled.

c. The SH (Source Handshake) circuitry's output is enabled on "talk", and disabled on "listen".

d. The AH Enable and Hand Gating circuits are provided inputs to indicate whether "listen" or "talk" mode is active.

Debouncers

The Debouncers comprise four-sixths of an MC14490 contact bounce eliminator. They "clean up" the ATN, IFC, NDAC and HAND signals, to prevent false MPU interrupts due to "ringing" on these lines. They debounce both the rising and the falling edges of the signal.

Hello

The Hello circuit is a gate used by the 4907 to detect, prior to transmitting data over the GPIB, whether there are any "listeners" on the GPIB to receive the data. If a listener is on the line, then it will be pulling either the NRFD (Not Ready For Data) or NDAC (Data Not Accepted) line active. If neither line is in its active state, then no listener is on the line, and the Hello circuit will signal this fact to the MPU by pulling the NOBODY line high.

Hand Gating

The Hand Gating circuitry is used during the three-wire "handshake" procedure by which the GPIB transfer bus regulates the flow of data bytes over the data bus. This circuit's output is passed through a debouncer, becoming the DB HAND signal. This signal is applied to an interrupt register to generate an MPU interrupt.

When data is to be transmitted, this interrupt informs the MPU that the "listeners" on the GPIB have all released the NRFD line and that the 4907 may now place a byte on the data bus. (When that byte has been placed, the MPU will send the SHAKE signal, causing the SH circuitry to transmit the DAV message.)

When data is to be received, the HAND interrupt informs the MPU that the "talker" on the GPIB has sent the DAV (Data Valid) signal, indicating that a byte has been placed on the GPIB data bus. (When the 4907 has read that byte, the MPU will send the SHAKE signal, causing the AH circuitry to transmit the "data accepted" message.)

The Hand Gating Circuitry, then, is a logic tree which sends the HAND signal when (a) the 4907 is in "listen" mode and the DAV signal is true, or (b) the 4907 is in "talk" mode, and the NRFD signal is false.

Source Handshake

The SH (Source Handshake) circuitry is used to generate "handshake" signals on the GPIB's transfer bus during the transmission of data from the 4907.

The SH circuitry includes a flip-flop which is set when (a) the 4907 is in "listen" mode or, (b) the DAC (Data Accepted) signal is true. When the "listeners" on the GPIB indicate that they are all ready to accept data (NRFD false), the HAND signal from the Hand Gating circuitry causes the MPU to place a byte on the data bus and send the SHAKE signal. This SHAKE signal clears the flip-flop in the SH circuitry, sending its output high. This sends a "1" through an AND gate to the Transfer Bus Transceiver, which sends the DAV signal on the GPIB.

The AND gate on the output of the flip-flop disables the SH circuitry, preventing it from transmitting the DAV signal when the 4907 is in "listen" mode.

Acceptor Handshake

The Acceptor Handshake circuitry, Figure 6-17, is used to generate "handshake" signals for the GPIB transfer bus during reception of bytes from the GPIB data bus. It feeds its outputs to the Transfer Bus Transceiver which keys the appropriate GPIB transfer bus lines.

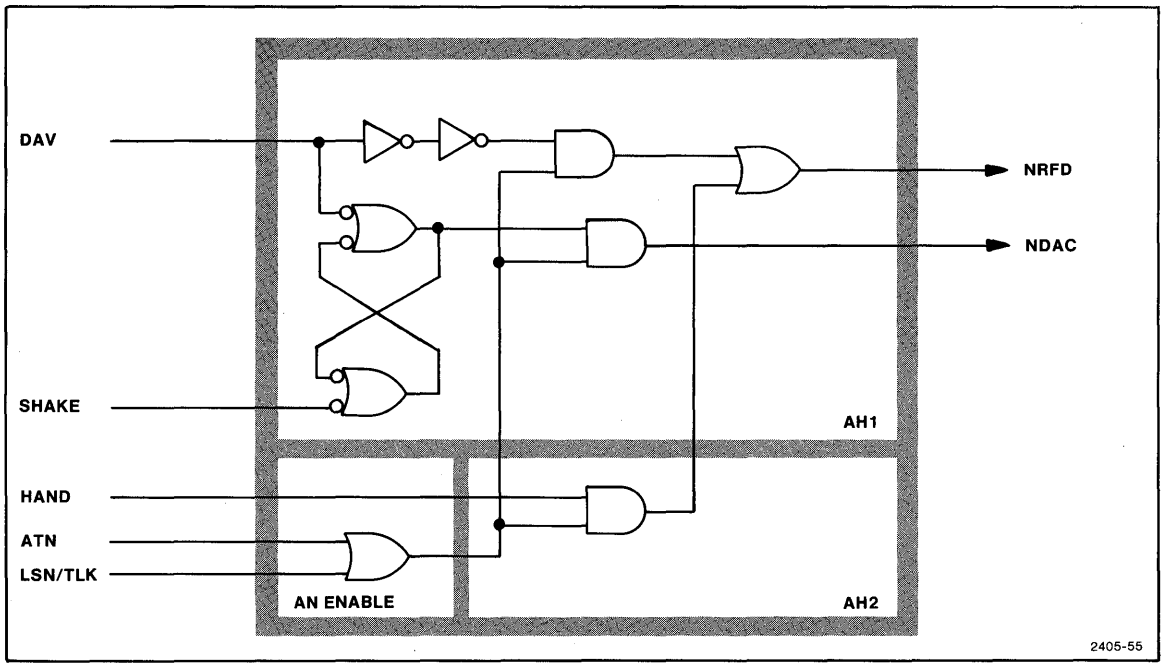


Figure 6-17. Acceptor Handshake Block.

The OR gate U239D acts as an AH circuit enable, as well as a Hand Gating circuit enable. This gate enables the AH circuitry whenever the 4907 is not in "talk" mode, and also whenever the ATN signal is true. So even if the 4907 is not addressed, the AH circuitry is enabled. This does not matter, however, as the Bus Handshake Transceiver Steering gate prevents the Bus Handshake Transceiver from transmitting.

The 4907 will be ready to accept data when (a) the AH circuitry is enabled, and (b) the talker has not yet placed a new byte on the GPIB data bus (DAV false). (With DAV false, the set-reset flip-flop in the AH block is set.) Under these circumstances, the logic in the AH block provides a "0" to the Bus Handshake Transceiver's BO port, signaling to the GPIB that the 4907 is ready to accept data.

When all GPIB "listeners" are ready for data, the GPIB's NRFD line goes inactive high (NRFD false). The "talker" then places a byte on the data bus, and sends the DAV message.

Immediately on receipt of the DAV message, the logic in the AH block causes the Transfer Bus Transceiver to send the NRFD message, inhibiting the "talker" from placing another byte on the data bus. Also the Hand Gating circuitry and its associated debouncer produce the DB HAND signal, which generates an MPU interrupt. The interrupt causes the MPU to read the byte available on the data bus, and then to send the SHAKE signal.

The DBHAND signal is also fed to the logic in the AH block, which acts a a "NRFD hold" circuit. That is, it prevents the 4907 from sending the "ready for data" signal until the DAV signal has gone away and this information has had time to clock its way through the debouncer to send the HAND signal low. This prevents the 4907 from missing a HAND interrupt when a very fast "talker" is on the line.

Until the MPU has read the data byte, the flip-flop in the AH block will be set, providing a "1" to the Bus Handshake Transceiver's CO port. This causes a NDAC message to be sent on the GPIB. When the MPU has read the data, however, it sends the SHAKE signal. This signal resets this flip-flop and causes the Bus Handshake Transceiver to signal that the 4907 has accepted the data by letting the NDAC line go inactive high.

When all "listeners" on the GPIB have accepted the data, the "talker" can place another byte on the data bus and start the handshake procedure again by sending the DAV message.

Disc Control and Status Blocks

This first of three sections on disc interface circuitry covers the operation of the disc control and disc status reporting circuits. Figure 6-18 is a functional representation of the disc status and control blocks.

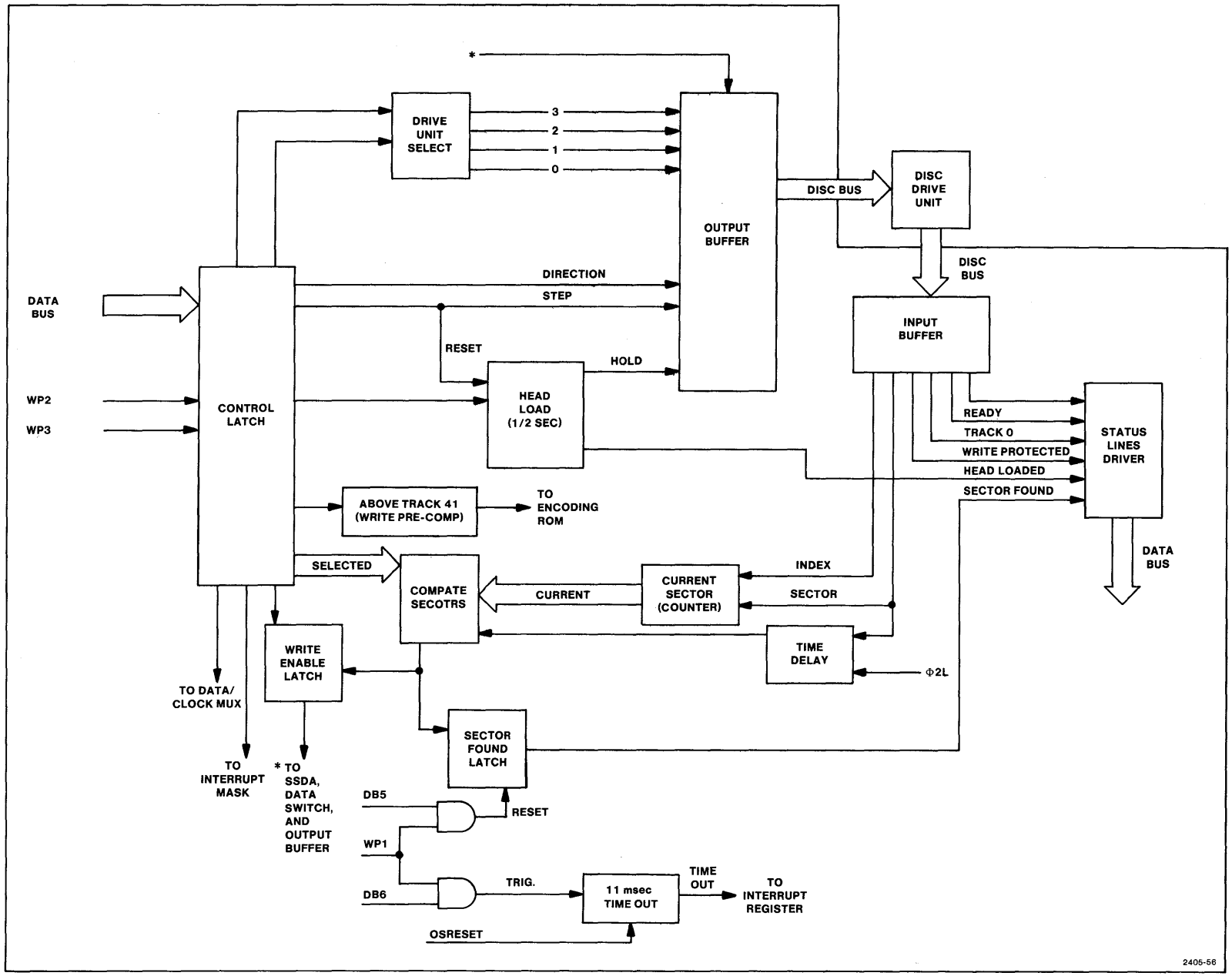


Figure 6-18. Disc Control and Status Interface.

The microprocessor controls its several disc drive units by writing over its internal data bus to a control latch, whose outputs are disc interface control lines. This control function is split between two latches, U205 and U317. Each latch reads the data bus when enabled by its write peripheral address decode line (WP3 and WP2 respectively). The controlling functions performed via the control latch circuit are:

1. Drive unit select - selects one of four possible drive units.
2. Head move control - head move in and out (track seek) and head load.
3. Disc sector select.
4. Write pre-compensation control.
5. Interrupt mask control.
6. Internal read data multiplexor control.

Drive Unit Selection

The drive unit select sub-block is a decoder that listens to the MPU in binary and tells the devices (drive units) which one the MPU wants to talk or listen to. The drive unit select circuit is first enabled by the UNIT SELECT ENABLE line from the control latch. Then the decoder looks at its inputs, UNIT SELECT 0 and UNIT SELECT 1 (from the control latch), and sends one of its four output lines low. (Only three of these four lines are actually used because that is the maximum number of drives in a 4907 system.) These output lines then pass through signal drivers on the way to their separate drive unit.

R/W Head Move Control

The three kinds of Read/Write (R/W) head movement are step in, step out, and load. Loading the head places it against the disc media just before a read or write on the disc. Likewise, the head is unloaded if the unit is deselected or if stepping to a location more than 3 tracks away. The head also unloads 1/2 second after the last R/W operation.

The disc drive unit requires two Control Latch signals to step in or out to a different track. Initially the STEP line goes active low, then the drive reads the condition of the DIRECTION line. An active low DIRECTION means step in (toward the center of the disc). Step out is toward track 00 and away from the center (DIRECTION line is high). These two lines are buffered before reaching the interconnect, where they fan out to the several drive units.

The head loading is signalled by TRIGGER HEAD LOAD from the Control Latch. This signal is sent to the Head Load block (Figure 6-16), a one-shot timing circuit. When the one-shot receives the trigger signal, it sends its output active low for 1/2 sec (HEAD LOAD-0). This timer in reset by the same STEP signal mentioned earlier. Also a complimentary output, HEAD LOAD-1, is sent to the disc status register, so the MPU knows when the head is loaded onto the flexible disc.

Sector Select

Several interrelated sub-blocks of circuitry are used to select a desired sector on the disc media.

In order to write to or read from a certain sector, the MPU first selects the address of this sector via control lines. It then examines the addresses of sectors which pass under the read/write head as the disc spins, constantly comparing these with the address of the desired sector. When the sector addresses match, and when a synchronization signal is received, the write function is enabled and a MY SECTOR report is sent back to the MPU via the disc status buffer.

Current Sector. The determination of the current sector is achieved by a counter circuit, U213, that counts SECTOR pulses received from the disc. The SECTOR line connects to the clock input of a 16 bit counter, and the INDEX line connects to its reset. So each time an INDEX pulse is received, the counter is cleared and resynchronized. Consequently, each sector pulse following INDEX is called sector one; then each succeeding sector pulse increments the counter to create new sector addresses up through sector 32.

Compare Sectors. The Compare Sectors block in Figure 6-18 consists of a six bit comparator, U209. Five of the six lines are used to compare the sector selected by the MPU against the current sector. A timing delay signal is inserted on the other line.

Since it takes a certain amount of time for the sector pulses to ripple through the current sector counter, we need to delay the comparison until a stable and valid count is achieved. This delay signal comes from the Time Delay block and then enters comparator pin 15, to be compared with a zero logic lead on the opposite pin 14.

The output of the Compare Sectors Block is a line called MY SECTOR which comes from the sector found latch and goes to the Disc Status Buffer. This line is also used to trigger the Write Enable line which goes to the Data Switch and Serial/Parallel Data Converter.

The MY SECTOR line is reset by a SECTOR FOUND RESET line which the microprocessor accesses via WP1 and D55.

Time Out. The WP1 and DB6 lines also trigger a 11 msec Time Out circuit that sends an interrupt after 11 msec to the Interrupt/Status Registers. This Time Out (TOUT-0) signal provides a waiting period while the disc performs head step and load operations.

Time Delay. Another timing circuit, Time Delay, consists of two flip-flops, U201A and U201B, and is used to delay the sector pulse signal. The sector pulse is first clocked into Part A. Before the signal can pass through Part B, it must be clocked by the Φ2L pulse. This two stage delay is sufficient time to allow the sector counter to stabilize, and provides a 1 usec strobe for the comparator at the start of the sector.

Other Control Lines

Three of the Disc Control Latch lines serve circuits located outside the disc units. These lines are Interrupt Mask Control (INTMSK-1), Internal Data/Clock Multiplexer Control (DATAMUX-1), and Write Precompensation Control (AT41-0). Interrupt Mask Control is discussed under "Status/Interrupt Registers" earlier in this section. Data Multiplexer Control (DATAMUX) and Write Pre-Compensation Control are discussed under "Data Encoding and Decoding Circuits" later in this section.

Disc Status

The disc drive units send status information to the control board via six lines: Track 0, Sector, Index, Disc Change, Write Protect, and Ready. These lines are fed through an Input Buffer, U433. Some of these lines are used to enable control circuits while others report disc status to the microprocessor via the Status Lines Driver U105, a tri-state device.

Disc Data Interface

The data portion of the disc interface can be logically divided into two major sections: the parallel-to-serial data adapter (with CRC check), and the MFM disc format encoder/decoder. Furthermore, these circuit sections function somewhat differently for a write than for a read operation.

The following discussion first describes each circuit block in the parallel-to-serial adapter (S.S.D.A) section as they function in the write mode. The discussion then covers the operation of this same circuitry (with slightly different parts) in the read mode. After this the data encoder/decoder circuits are described for the read and write modes.

Data Adapter/CRC (Write Operation)

Figures 6-19A and 6-19B are illustrations of the functional sub-blocks found in the Data Adapter/CRC circuitry. Figure 6-19A pertains to write operations and should be referred to while studying the following section.

SSDA. The Synchronous Serial Data Adapter (SSDA) sub-block converts parallel data bytes into serial bits for entry on the flexible disc. This functional circuit block is contained in a single Motorola 6852 SSDA chip, U307. Figure 6-20 illustrates the SSDA's internal functional blocks.

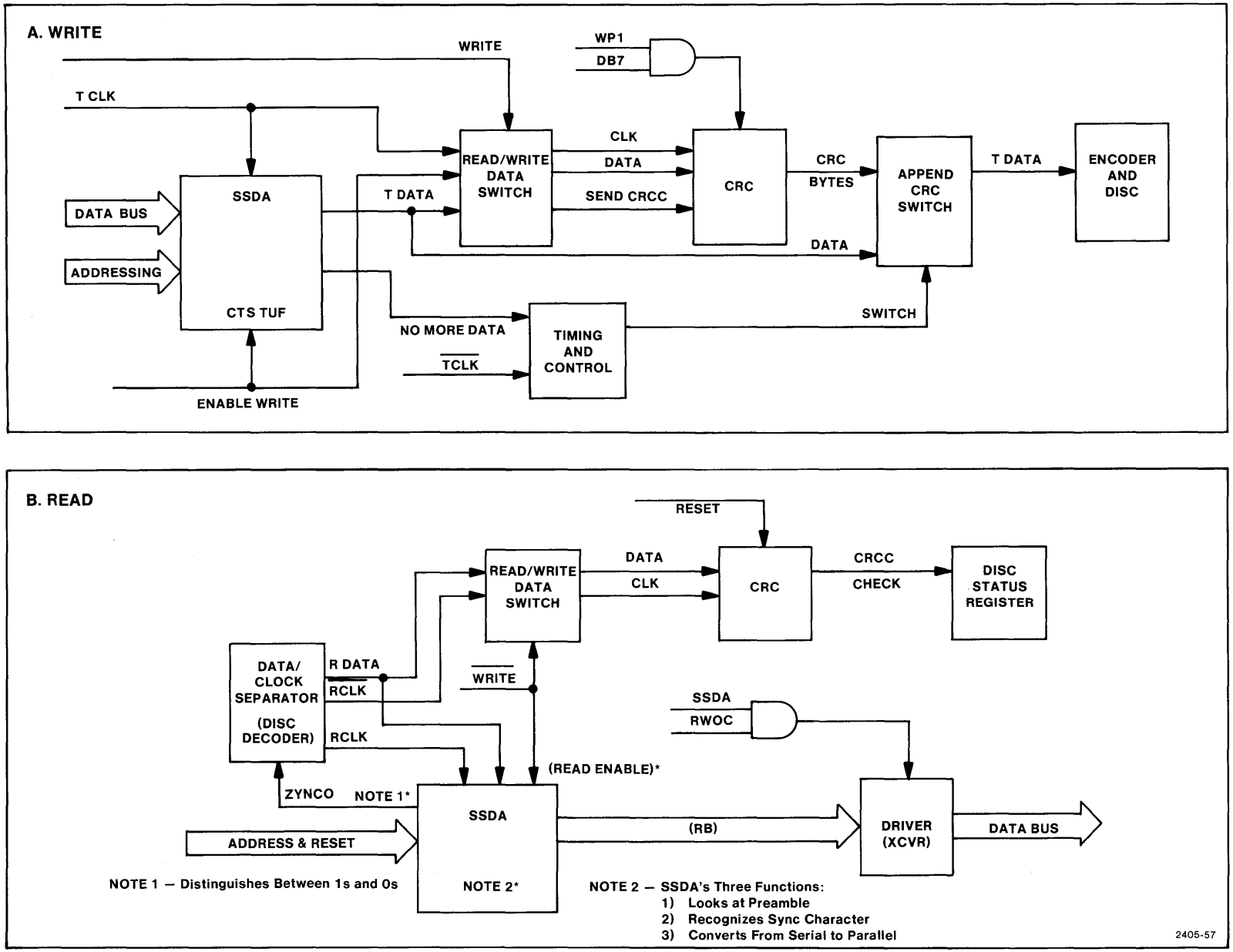


Figure 6-19. Data Adaptor/CRC Blocks.

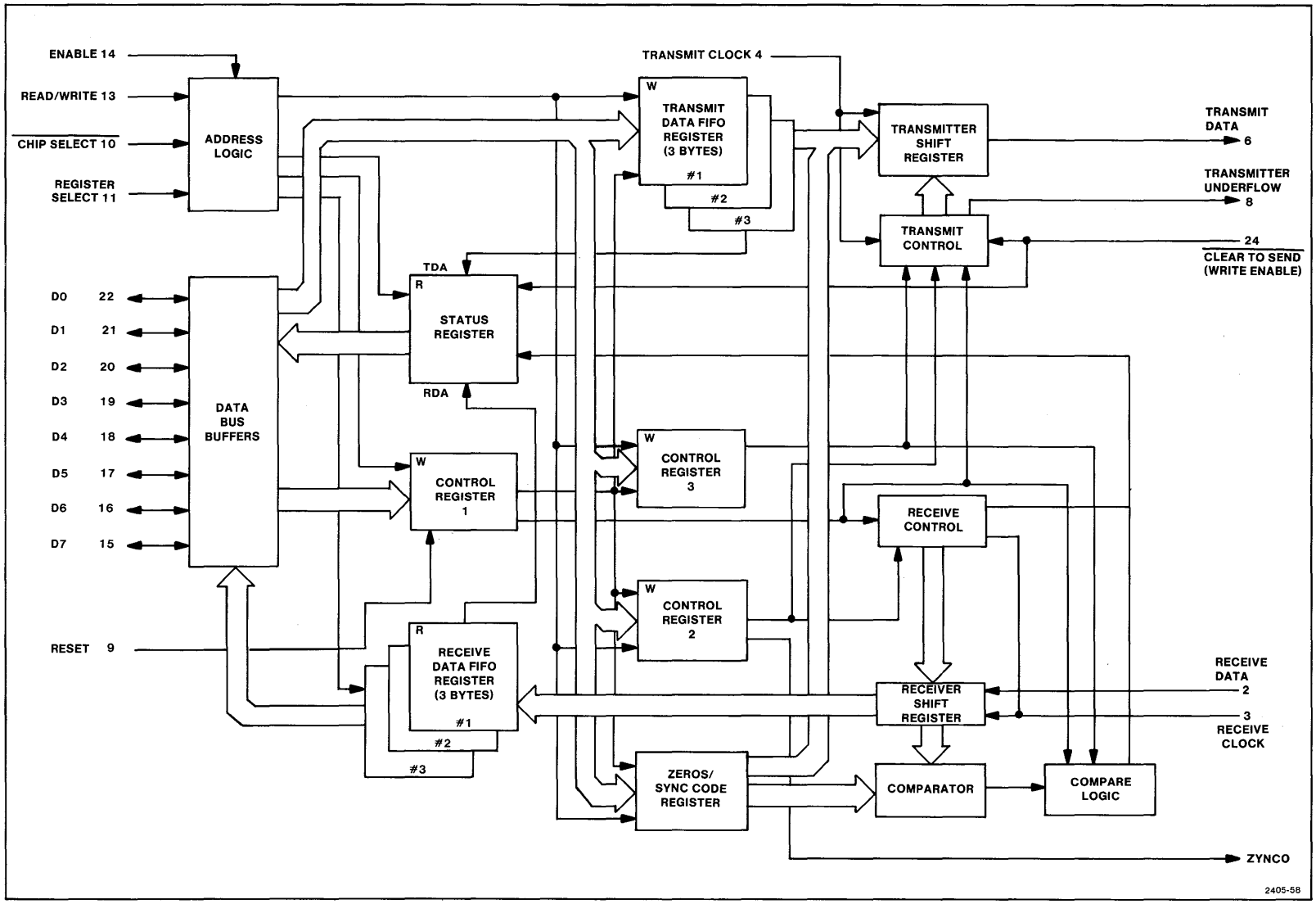


Figure 6-20. SSDA Internal Block Diagram.

The SSDA is addressed by a combination of lines: SSDA (connected to Chip Select), RWOC (connected to Read or Write), and AB0 (connected to Register Select). A Reset comes from SYSRS (System Restart). The Address Logic recognizes when the SSDA is selected and addresses the particular internal registers needed for this write operation. The SSDA contains seven registers; five are write-only (W) and two are read-only (R). Those registers involved in a write to disc are: Transmit Data FIFO (W), and Control Registers 1, 2, and 3 (all W). The Control Registers receive firmware instructions to manage internal operation of the SSDA.

Write data first passes from the data bus into the SSDA's Transmit Data FIFO (First-In First-Out) Register. Once inside the three byte FIFO, data moves to the last empty location. When the Transmit shift register becomes available, it automatically pulls the first byte from the bottom level of the Register. The Φ2L pulse on the Enable input synchronizes this step. The firmware is designed to keep data moving into the FIFO at the correct speed. If no more data is found in the FIFO (called data "underflow condition") the Transmitter Shift Register is automatically loaded with 0's. These zeroes come from the firmware and are loaded through the zero-Sync code Register during Write mode. The zeroes are required so there will be no interference with the CRC pattern which follows the main data stream. The underflow condition sets the NO MORE DATA line, which activates the Append CRC Switch via a Timing and Control Circuit.

Timing and Control. A pair of flip flops, U215 A and B, serve dual functions: (1) to enable the CRC Append Switch at a clock pulse, and (2) to enable the CRC's CWE input via the third path through the Data Switch. The flip flops are cleared by a SECTOR pulse on the reset A part.

Read/Write Data Switch. The Data Switch functions as a double throw triple pole switch, whose A and B pole positions are controlled by an S (switch) input. During the write operation this switch selects the T DATA line (data bytes serialized by the SSDA), and sends it to the CRC generator.

CRC Generator (Write). The CRC (Cyclic Redundancy Check) Generator is a single chip circuit that performs an error checking function on each sector of data written to and read from the disc. In the write mode, the CRC chip looks at the data stream and does a running division on it by a polynomial divisor; this polynomial is X16 + X15 + X2 + 1. When the division is completed on a sector of data, the remainder comprises the CRC character. This remainder (CRCC) is appended to the data stream and written on the disc.

CRC (Read). When the data is read from the disc, it passes through the CRC generator and the same process is repeated. If the remainder calculated during the Read (including the written CRCC) is zero, the data passes through as valid.

The internal functioning of the CRC circuit is represented in Figure 6-21 by a series of 16 registers. These registers have exclusive OR feedback loops inserted corresponding to each term of the polynomial. The Q outputs of the registers are all ORed together to form the CRCC check output. A CWE line interrupts and clears the feedback paths to allow outputting the CRCC at the end of write data.

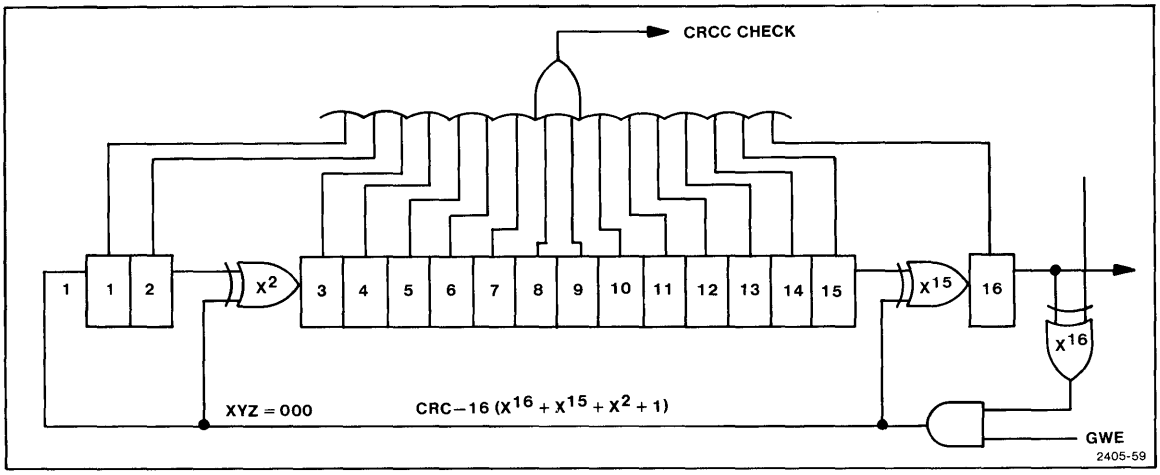


Figure 6-21. CRC Circuit Functional Diagram.

Append CRC Switch (Write). After the CRC generator processes the TDATA stream, it sends the resulting CRCC bytes to one of two inputs on the Append CRC Switch.

During a Write operation the Append CRC Switch passes TDATA coming directly from the SSDA. When the SSDA senses the end of the data stream, it sends the NO MORE DATA message to the Append CRC switch. The switch flips over from TDATA to CRC BYTES, and the CRC bytes are inserted the data stream without interruption. The output of this switch goes into the Encoder circuits and finally to the selected disc drive unit.

Data Adapter/CRC (Read Operation)

SSDA. Some disc data interfacing circuits are involved in both Write and Read operations, but their functions and interconnections are quite different for each operation. Consider the Read part of Figure 6-19B. The SSDA receives a serial data stream RDATA from the disc via a decoder circuit (to be discussed later). A receive clock signal, RCLK-1, enters the SSDA also; its compliment, RCLK-0, enters the R/W Data Switch. The RCLK signal controls the serial-to-parallel data conversion. Figure 6-22A shows the read timing relationship.

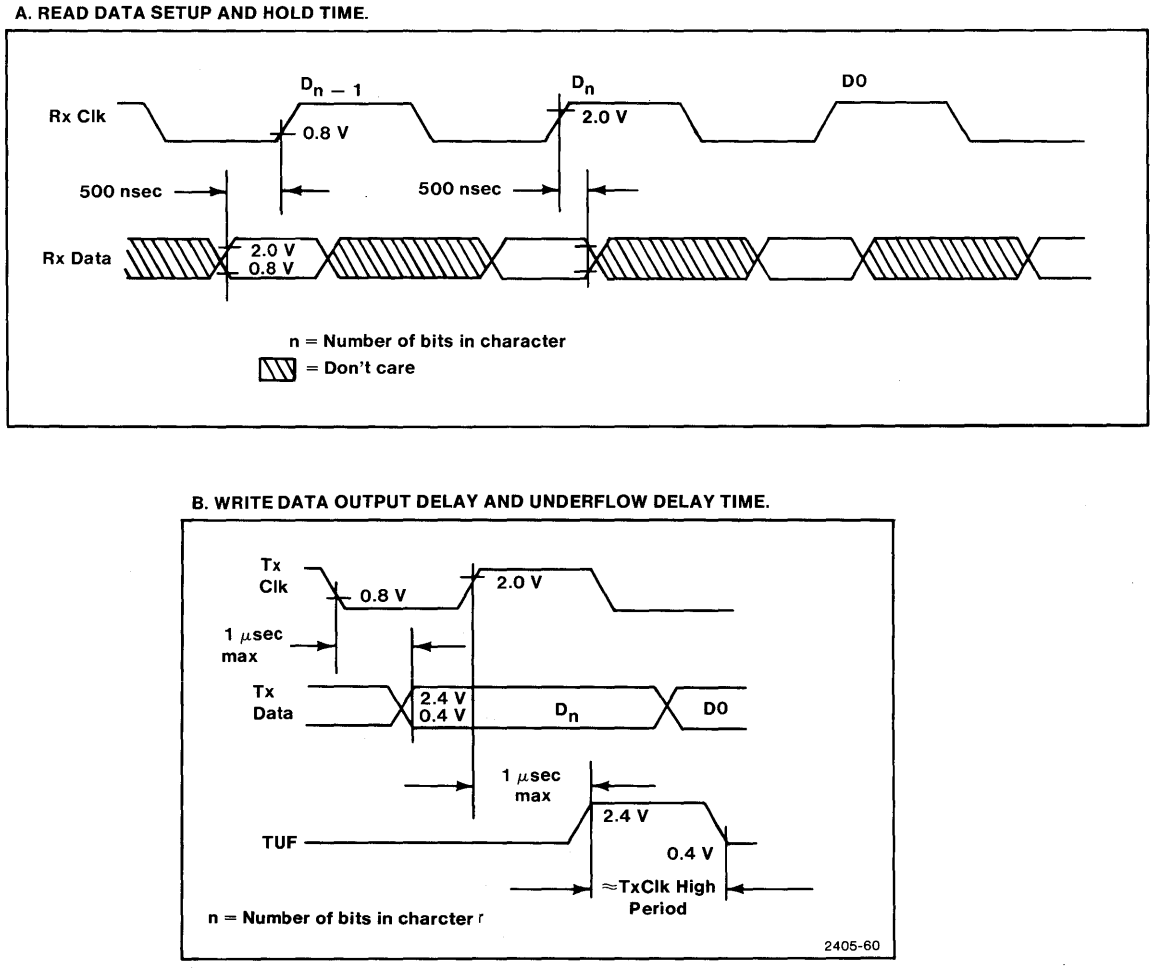


Figure 6-22. Transmit/Receive Clock Timing.

When the SSDA's Receiver Register first begins looking at data, it sees a string of zeroes called the Preamble. The first 01 pattern (following these zeroes) is recognized by the comparator in the SSDA as a Sync Character. This means that data follows next. The Receiver Shift Register immediately begins segmenting the data stream into 8-bit bytes. These bytes are sent in parallel mode to the three byte Receive Data FIFO Register.

At the beginning of a read operation the firmware writes an 01 into the Sync Code Register in the SSDA. Bytes are clocked through to the last empty location by Φ2L Enable pulses. We are in a two-byte transfer mode, so when the last two-byte locations are full, the RDA (receive data abailable) status bit signals the MPU that data is ready. The MPU then signals the SSDA's Data Bus Buffers to pull data from the bottom two registers, to be read over the 4907's data bus.

A separate function of the SSDA is to control the ZYNCO (zero sync.) line, which is used by the Data/Clock Separator and the Zeroes/Ones Circuit to distinguish between a string of all zeroes and all ones. The function of the ZYNCO line is explained later in the "Zeroes/Ones" block description.

Read/Write Data Switch (Read). When the Write line on the Data Switch input goes high this indicates Read mode, and the Data Switch selects the Receive Data and Receive Clock lines. The serial data stream then passes through this switch and into the CRC block.

The CRC checks for a mismatch between data written to and read from the disc. (The CRC read function was described earlier with the CRC write process.) If a sector data stream checks valid, this is indicated on the CRCC check line of the U105 Disc Status Register. On the other hand, if a mismatch occurs, the CRCC line reports this to the MPU through a status line.

Data Encoding and Decoding Circuits (Read Operation)

The disc data encoding and decoding circuits are found on schematic sheet 1-1. These two circuit sections are also represented in block form in Figures 6-23 and 6-24. The functional operation of the circuitry during read operation is discussed in this section. The operation of this same circuitry during write operation is discussed in the next subsection.

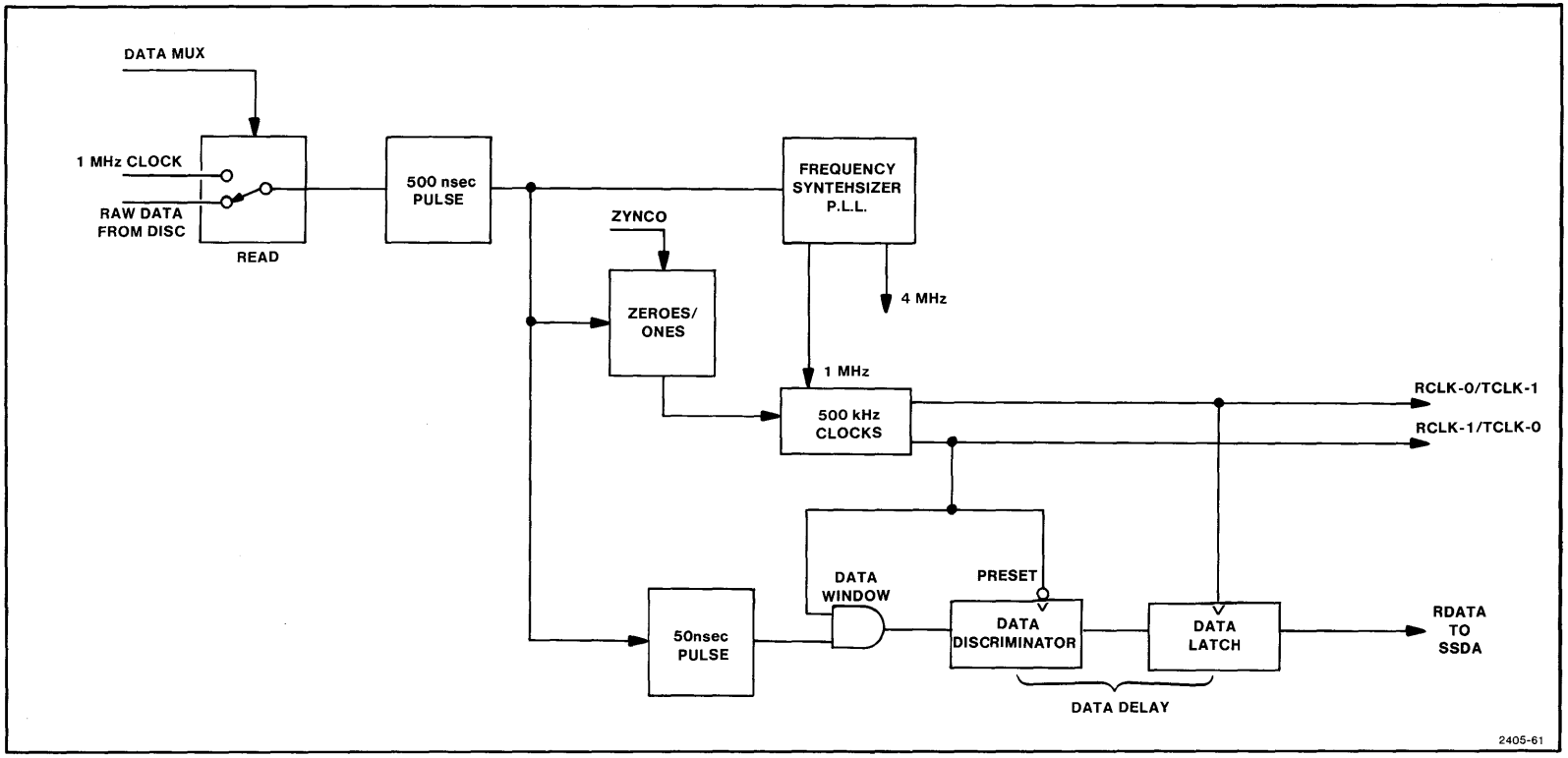


Figure 6-23. Read Data Decoder and Synthesizer.

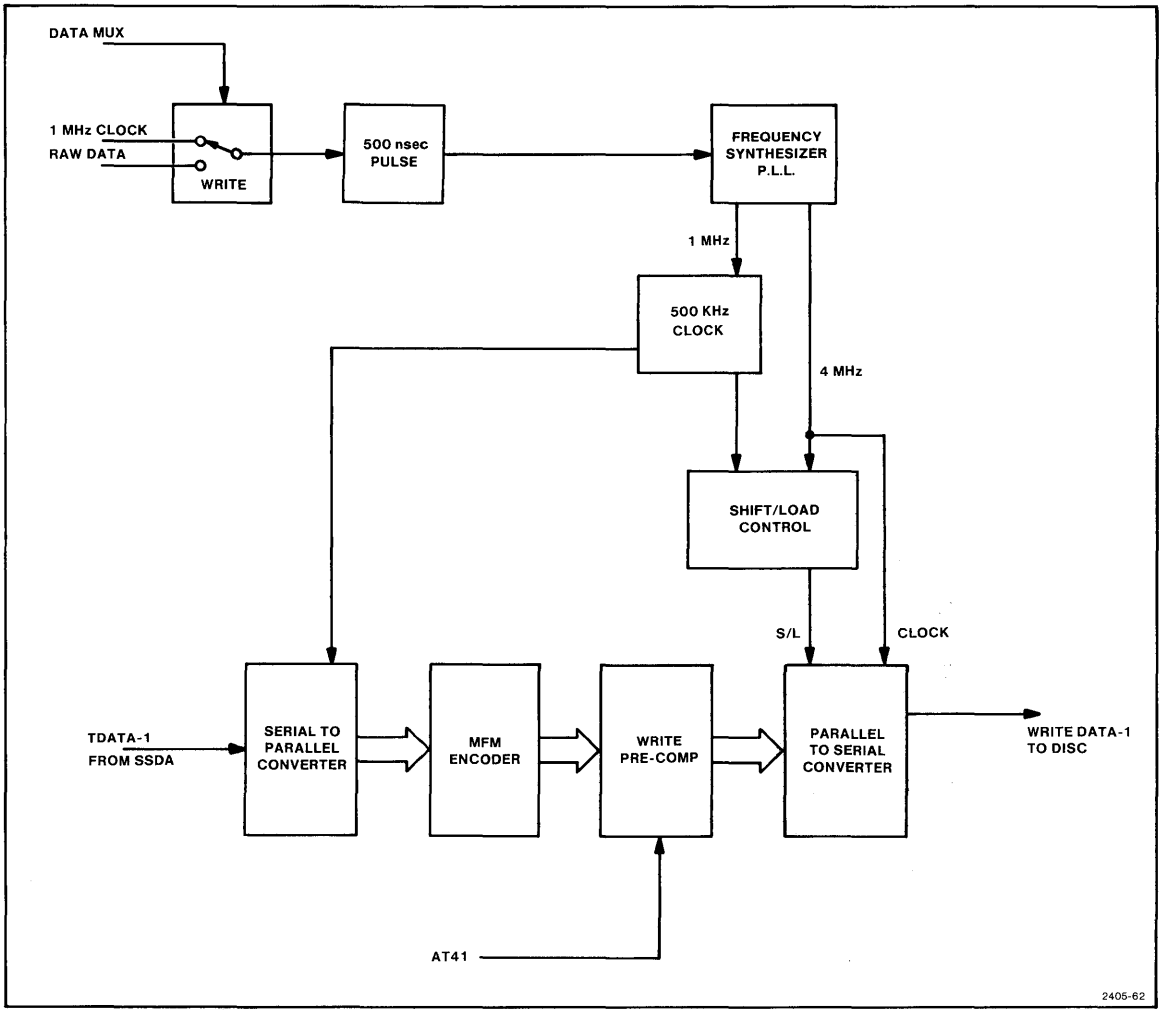


Figure 6-24. Write Data Encoder and Synthesizer.

During a read operation, the decoding circuitry takes a RAW DATA stream from the disc and uses a phase-locked loop to filter out jitter, producing a uniformly timed data stream.

A pair of clock signals, derived from the data stream timing (RCLK-1 and RCLK-0) are sent to the SSDA for synchronization during read. Compliments of the signals (TCLK-0 and TCLK-1) are produced by the same circuit for a write operation.

Data Mux. The line carrying RAW DATA from the disc enters the read data decoder at the Data Mux switch. This switch selects between the RAW DATA stream and a 1MHZ clock (from the Master oscillator/counter). During a read operation, the RAW DATA input is selected. The control signal for this switch is the DATAMUX-1 line coming from the MPU via the Disc Interface Control Latch (discussed earlier in the Theory of Operation).

500nsec Pulse. The RAW DATA then enters a one-shot, U 335B, whose function is to control/stretch the data pulses to the desired 500 nanosec width. This timing operation is required because the raw disc data enters the interface through a buffer, U 433, and can be any pulse width (usually 2 to 3 hundred nanoseconds) when it leaves. The Q output of the one shot, passes the shaped data stream onto the phase-locked loop, and the data-clock separator. The "Q not" output feeds the zeroes/ones discriminator circuit.

Phase-Locked Loop. In order for the decoder circuits to be synchronized during a read operation, certain clock signals are required. These clocks must be derived from the timing of the raw data from the disc. Rather than use a simple one shot, the 4907 incorporates a phase-locked loop circuit. This allows the decoder to track directly on the row data stream, and eliminate the jitter caused by variations in disc motor speed, and timing skews caused by magnetic interactions on the disc.

Figure 6-25 shows a conventional phase-locked loop diagram for the 4907. The phase-locked loop functions as a frequency synthesizer and stabilizer. The incoming data stream first passes through a "phase detector" where it is compared against an error signal on a feedback input. The resulting difference is translated into an analog signal by the "current pump." This signal is then integrated, to give a picture of trends occuring over time, and then enters the voltage controlled oscillator (VCO). The oscillator produces a digital clock signal that is shifted plus or minus according to the errors present. This error signal is fed back into the phase comparator, so the whole circuit acts like a frequency regulating servo. A counter in the feedback path divides the oscillator frequency down to 1 MHZ. This signal is further halved by U537B, forming the complimentary 500 KHZ clocks: TCLK-1/RCLK-0 and TCLK-0/RCLK-1.

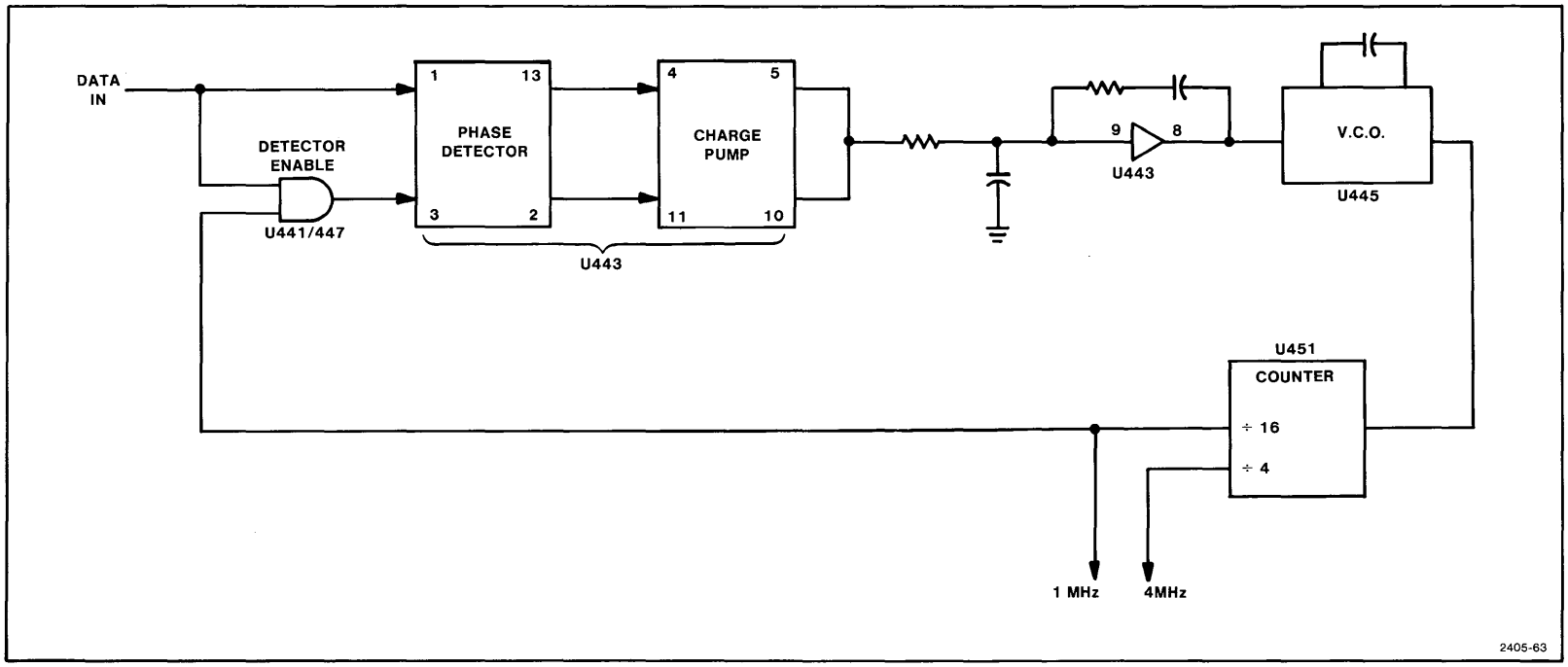


Figure 6-25. Phase-Locked Loop.

A final portion of the feedback loop is a detector enable circuit comprised of U441 and U447. Ordinarily, the VCO/counter is feeding constant 1 MHZ (approx.) pulses into the feedback input on the phase comparator. At the same time data stream pulses, at approximately 500 KHz, are entering the main input (pin 1) of the Phase Detector. Furthermore, there are times when this MFM data stream goes several feedback pulses without producing a clock or data pulse. This means that the feedback VCO pulses are not always accompanied by a data/clock pulse; and the phase-locked loop misreads this as a drastic change in input frequency. Consequently the VCO tries to shift its output accordingly, producing a large and unnecessary error correction.

The detector enable circuit solves this problem by interrupting the feedback VCO unless there is a data pulse present for a valid comparison. The circuit, comprised of flip-flops and inverters, acts basically like an AND gate. The purpose of the inverters is to provide the necessary pulse width for the flip-flops.

Data/Clock Separator. After leaving the 500 nsec Pulse circuit, the data path splits between the phase-locked loop, detector enable, zeroes/ones enable, and the input to the data/clock separator. The data/clock separator block extracts valid read data from the data stream, while producing the transmit/receive clock signals required by the SSDA. Refer again to Figure 6-23. The data stream first passes through a 50 nsec one shot, U335A, which produces the proper pulse width for subsequent timing comparisons.

This data pulse then enters a "data window" (AND gate, U541B) where it is compared against the 500KHz clocks, RCLK-1. This read clock is high only during the second half (data portion) of the 2 usec bit cell. A raw data pulse occuring at this time passes the window and is interpreted as a logical 1. No pulse, of course, is a logical zero. (If a pulse occurs during the first half of the bit cell time, it is seen as a clock pulse instead of a data pulse. Since the AND gate is not enabled, it filters out the clock pulses.)

Next, the read data pulse (from the data window) is clocked into a flip-flop, U537A -- by the same RCL-1 that enabled the AND gate. This sets the flip-flop to logic zero at the start of each data cell. The data is assumed to be zero unless a preset (data) pulse is received. A second flip-flop, U539B, follows immediately and is clocked by the complimentary RCLK-0. This flip-flop provides synchronization between the read clock and the data being sent to the SSDA over the RDATA line. These two flip-flops combine functions to hold and delay the pulse until the SSDA is ready to receive it -- a total delay time of 2 usec.

Zeroes/Ones. A further piece of decoding circuitry is required to distinguish between a pattern of all zeroes and all ones -- since these look the same in MFM encoding format.

In the 4907 we have defined the preamble, beginning each sector, to be a pattern of all zeroes. (See Data Organization on the Flexible Disc, Section 6.) The microprocessor thus reads a sector pulse followed by preamble and instructs the SSDA to send a zero sync pulse, ZYNCO, to the decoder circuits. This tells the zeroes/ones circuit to look at whatever data is arriving as all zeroes. The ZYNCO pulse is only on for about 5 usec; just long enough to trigger the synchronization process. This sync signal is ANDed with a data pulse and then sent to the divide by two 500KHz clock generators, U537B. This synchronizes the clock and says that we are receiving all zeroes; and from this point on the data decoder will decode the data in the correct sense.

Data Encoding and Decoding Circuits (Write Operation)

This subsection describes the process of encoding the data so it may be written onto the disc in the proper format. Some of the same circuits used in the read operations are also employed in the write process. This description begins by showing how the Data Mux switch, Phase-locked loop, and clocks are used to time the Encoder. Next the Write Data Encoder (including shift registers, shift/load control, and encoding ROM) is described. Here the serial data stream from the SSDA is transformed into MFM format (with pre-compensation where needed). The resulting WRITE DATA stream is finally sent to the selected disc drive unit. Figure 6-24 is a block illustration of the Write Data Encoding circuits.

Encoder Timing. To provide the needed Encoder timing, the Phase-locked Loop (PLL) is fed by a 1MHz oscillator signal from the Data Mux switch. These oscillator pulses pass through the 500nsec Pulse one-shot, as did the RAW DATA stream during a read. The PLL once again acts as a frequency synthesizer. The Detector Enable circuit serves no purpose during a write operation because the 1MHz pulses from the Data Mux are continuous running. The PLL produces 1MHz and 4MHz clocks. The 1MHz is divided down to 500KHz to serve the Shift/Load control and Serial to Parallel converter. The 4MHz clock serves the Shift/Load control and the Parallel to Serial Converter.

Write Data Encoder. The serial data from the SSDA, TDATA-1, enters the encoding circuits via a serial to parallel converter. The write data is encoded to include pre-compensation as needed. Therfore, the encoding circuits must be able to look ahead along the data stream and determine whether to adjust the write data pulses. To accomplish this, we run the serial data through a 4-bit shift register. The four lines coming out of this register feed the encoder/pre-compensation circuit directly. This register is clocked by TCLK-1 pulses.

The task of actually encoding the write data according to the MFM format, and adding the required compensation, is handled by a ROM circuit U425. This ROM contains the instructions and circuitry needed to arrange the TDATA stream into the MFM format. The ROM views four bits at a time, decides how to encode the data, and whether it should be pre-compensated either in the plus or minus time direction. A fifth input on the ROM carries an AT41-0 signal, which enables the write pre-compensation circuit. When the R/W head (on the disc) is above track 41, pre-compensation is required because the bit cells are packed closer toward the center of the disc. When this condition exists the AT41 line (from the decoders) goes active low -- thus enabling the pre-compensation program in the ROM.

Coming out of the ROM are eight bits of information, each representing 250 nsec of serial data in time. The 250 nsec times eight equals 2 usec, which is the time for a single data cell on the disc. The eight data output lines from the ROM enter a parallel to serial shift register. This converts the data from parallel back to a serial stream with the proper MFM encoding and write pre-compensations. The serial output, WRITE DATA, goes directly to the selected disc drive unit.

Shift/Load Control. The parallel to serial shift register has a Shift/Load (S/L) control input. When the Shift/Load line is low (S/L-0), a 4MHz clock pulse loads eight parallel bits into the register. When the S/L line goes high, the next eight clock pulses will shift the eight data bits through the registers and out. The S/L line is controlled by a circuit consisting of a pair of flip-flops.

The flip-flops and their clock inputs are arranged so a 500KHz TCLK-1 triggers the timing process. It does this by clocking the first flip-flop on. A 4MHz clock pulse is received by the second flip-flop passing on the information from the first flip-flop to its output (pulling the S/L low). The S/L output also resets the first flip-flop. On the next 4MHz clock, the S/L line is returned to the high state. The S/L line remains released until seven 4MHz pulses later, when another 500KHz pulse pulls this line low again. See Figure 6-26.

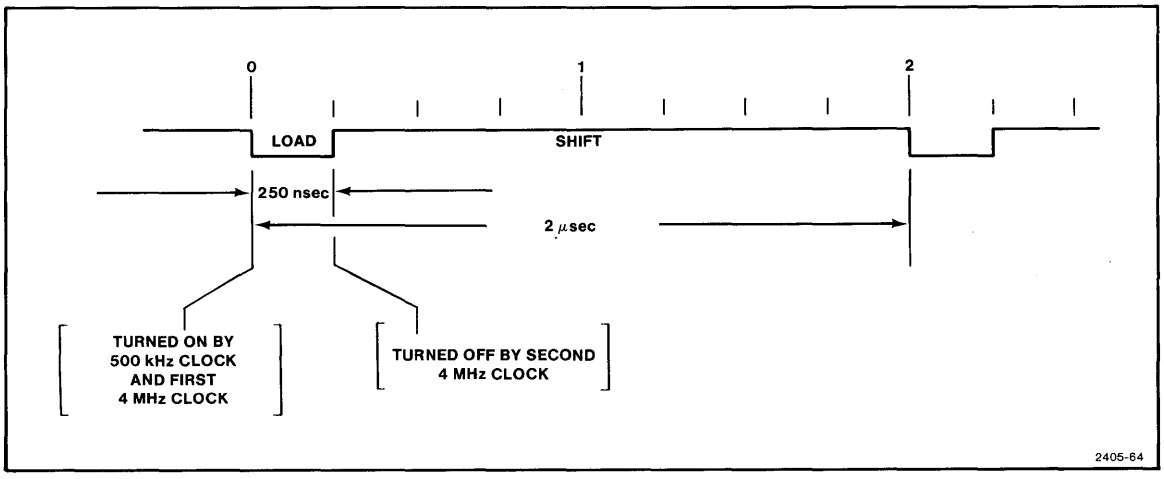


Figure 6-26. Shift/Load Timing.

FILE MANAGER ROM PACK

The File Manager ROM Pack is provided to extend the BASIC language interpreter capability of the 405X. The additional commands used with the 4907 File Manager are stored in this external ROM Pack, which plugs into the 405X's back pack unit.

The ROM Pack consists of four 2K ROM chips with their decoder/selector and power switch. See schematic sheet 4-1. The ROM inputs are connected directly to address lines AB0 through AB10. The remaining five lines of the address bus (AB11 through AB15) are used for chip selection. Since the ROM Pack operates in the 405X address space, X'8800' through X'A7FF', the decoder/selector, U5, will read any of these addresses and select the proper ROM (U1 through U4).

The power supply for the ROM chips is switchable by transistor Q. The control for Q is the right or left bank switch (BSL/R-0), depending on which ROM pack slot the ROM Pack is plugged into. This bank switch line also turns on/off the decoder/selector.

ROM BOARD

General Operation

The ROM Board, located just above the Control Board, contains the firmware instructions for the microprocessor. Figure 6-27 shows the functional block organization of the ROM Board. The following text describes these sub-blocks and how they are interrelated. General ROM Board operation is described first (including Test Fixture provisions). After this the Firmware Correction hardware is described.

System ROMs and Main Decoder

Most of the 4907 firmware is located in the System ROMs: twelve 2K by 8 bit chips, U121 through U261. These ROMs are selected by the outputs of the Main Decoder, U441. This decoder looks at four input lines, A11 through A14, and decodes them into twelve ROM enable lines: RE4 through RE15. These outputs individually enable the twelve system ROMs. Three other outputs Y0, Y3, and Y4 (corresponding to RE0, 3, and 4) serve to enable patch ROMs and output buffer gates.

The main decoder has two enable inputs. The first enable (pin 18) connects to address line A15, and selects the decoder when we are in address space X'8000' and higher. The other enable input (pin 19) is used to disable the main decoder only when a piece of firmware needs correction.

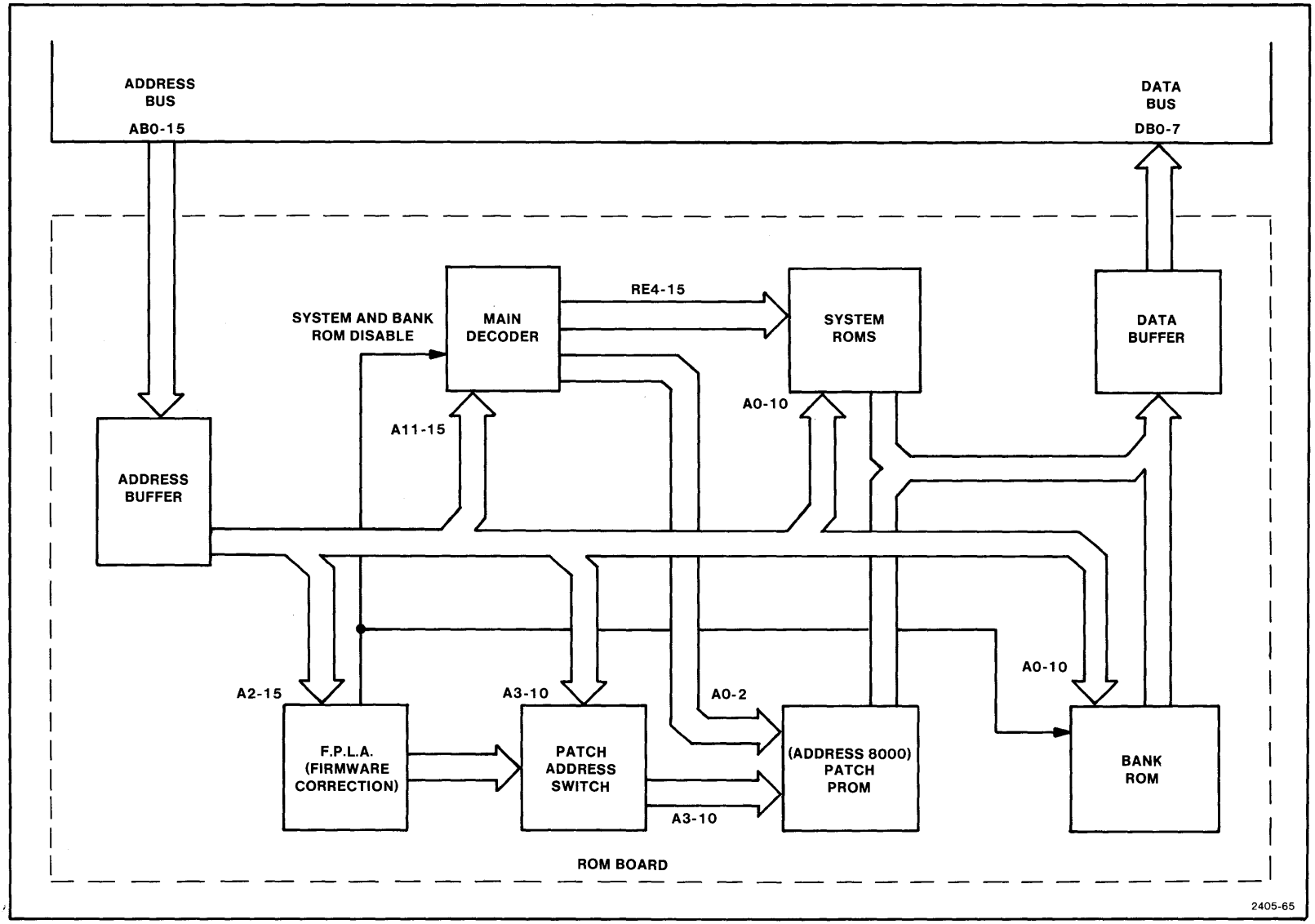


Figure 6-27. ROM Board Block Diagram.

Bank ROM

A separate ROM called the Bank ROM handles certain firmware routines related to Disc Drive Operation. This ROM occupies the address space X'6000' to X'67FF' and is enabled by a separate line, BNKROM, coming from the Address Decoder on the Control Board. The Bank ROM is fed by address bus lines, A0 through A10.

Address and Data Buffers

The 16-line address bus and 8-line data bus enter the ROM Board at J1 (a set of square pins, two rows of 25 each). The 50-conductor ribbon cable passes all power, control, address, and data lines; these all come from the Control Board.

The internal and external address busses are connected by the Address Buffer (U361 and U561). Likewise, the data busses interact through the tri-state output Data Buffer (U661). The Data Buffer is enabled by inputs 1G and 2G whenever the System ROMs or Bank ROM are sending out data. The BNKROM line enables the Data Buffer (via NOR gate U321C) at the same time it enables the Bank ROM.

Test Fixture Provisions

This discussion describes how the 6800 System Test Fixture affects operation of the ROM Board during ROM testing. First, all of the Data Buffer enable functions are over-ridden by the ROM disable lines, ROMDIS-1, which come from the Test Fixture. Also, anytime an address of X'9000' through X '9FFF' appears on the bus, the Main Decoder's Y2 or Y3 outputs go active. When this happens, the Data Buffer is disabled through a series of gates (U331A and C, and U321C). This allows the Test Fixture to substitute its Test PROMs into this address space without interference from the ROM Board ROMs.

Firmware Correction

The 4907's ROM Board contains hardware provisions for correcting and updating the system firmware. In the event that a segment of firmware needs correcting, this segment is replaced by translating its System ROM address into a corresponding address in Patch PROM. The FPLA (field programmable logic array) is programmed to recognize the addresses of firmware segments needing correction. The FPLA then disables the System ROM and enables a Patch Decoder, which addresses the firmware's replacement in the Patch PROM. The following discussion examines this process in more detail.

The FPLA

The FPLA is actually an array of programmable AND gates connected to programmable OR gates. See Figure 6-28. Each of the 48 AND gates has 14 inputs, and each AND input can be connected by programming to either the true or negative sense of the 14 chip inputs. The eight OR gates have 48 switchable inputs. The manner in which the input gates are connected to the output gates (by which switches are closed) allows us to translate a 14 line input address into an 8 line patch address. (With 48 AND gates in this particular type of chip, we can accommodate the same number of correction patches.)

NOTE

Each time a correction is implemented we simply program the inputs and outputs of the next AND gate and, of course, add the firmware correction into the Patch PROM. This means that old FPLAs and Patch PROMs are essentially recyclable and should be returned to TEKTRONIX factory service, after you install a new firmware correction package.

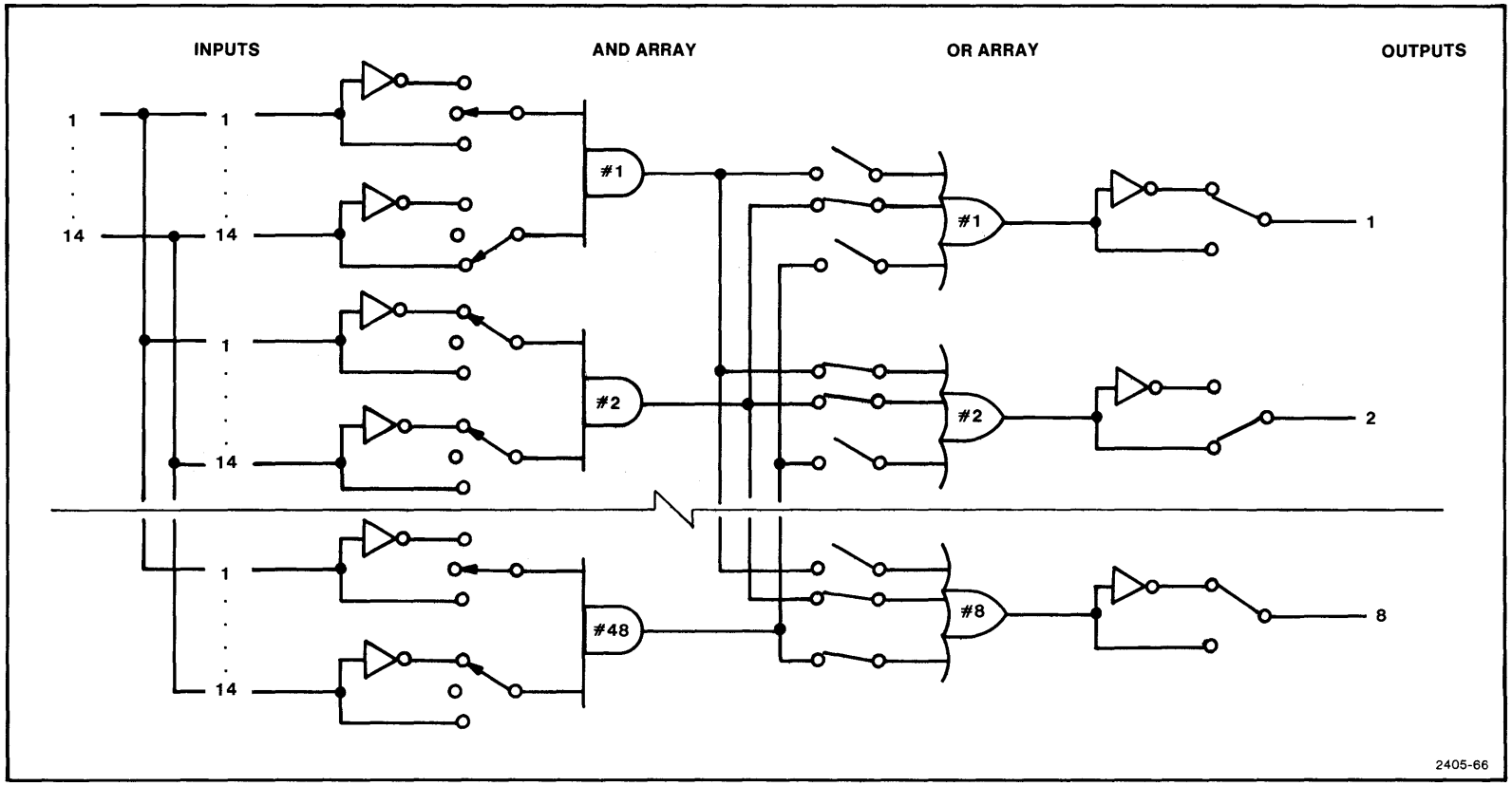


Figure 6-28. Simplified FPLA Diagram.

The FPLA's inputs are address lines A2 through A15, coming from the Address Buffer. Six of the FPLA's output lines connect to the A3 through A8 inputs on the Patch Decoder. The remaining two outputs perform other enable/disable functions. The seventh output enables an exclusive OR gate that accesses the A2 input on the Patch PROM. (The functional purpose of this circuitry is discussed in the Patch PROM section which follows.)

The seventh FPLA output connects to the main Decoder and Bank ROM. This line goes active low and disables the System ROM and Bank ROM whenever the FPLA needs to implement a correction.

Patch PROM and Patch Address Switch

The 4907 ROM Board contains two Patch PROM sockets; however, only one Patch PROM chip is to be installed at a time. The Patch PROM is addressed via the Patch Address switch. This switch selects addresses from the FPLA or from the Address Buffer. Normally a firmware error is small and requires an in-place correction. If the problem is more extensive, use the correction address in PROM to execute a jump to a routine in the upper space of the PROM. The jump instruction then exits via the data bus and returns via the main address bus. Consequently, you must include the Patch Address switch to allow reception of addresses directly from the Address bus (bypassing the FPLA).

The Patch Address switch is enabled by the same FPLA line that was used to disable the System ROMs and Bank ROM. This line also is ORed with the Y0 output of the Main Decoder, so that the Patch PROM may be enabled by either the FPLA or the Main ROM Decoder.

One further item of discussion relates to a space saving feature in the Patch PROM. The 4907 patch hardware is set up to replace firmware in 4 or 8 byte blocks. To allow this choice, and properly utilize the space in the Patch PROM, it is necessary to give the FPLA control over the PROM's AZ input. It is also necessary to include the current state of AB2 in the control structure. Therefore, PROM input A2 is controlled by AB2 exclusive-ORed with FPLA output F6, thus allowing the FPLA to use 4 or 8 byte boundaries within the PROM.

POWER SUPPLY BOARD

The 4907 power supply board provides voltages for the Controller and ROM boards and the flexible disc driver in the master 4907. The same power supply is contained in the OPTION 30/31 unit for one or two additional disc units.

Line Voltage Selection

Line voltage selection (100V, 120V, 220V, or 240V) is accomplished by the orientation of a circuit card inserted in the integral fuse holder, line cord receptacle, and line filter unit located on the back of the 4907. The selected voltage appears printed on this card when viewed through the sliding plastic window. (Card is inserted just below the fuse.) Filtered line voltage is thereby fed to the proper transformer input taps. Transformer outputs pass through conventional diode bridge networks to provide power for the -15V unregulated supply and source for the +5V and +24V regulated supplies. The fan and disc motor(s) receive a fixed 120VAC from the selector card, regardless of line voltage and card position.

Regulated Power Supplies

Essentially, this power supply is a traditional "series-pass transistor" design.

The +24V regulated supply derives its power from rectifier CR 1001. Regulation is provided by an I.C. regulator circuit, U351. This regulator circuit has its own internal zener voltage reference, an operational amplifier, and current limiting circuitry built in. Calibration of the +24V (and +5V) outputs is accomplished by setting R250 (voltage divider) so +5.1V is taken from the internal voltage reference. The +24V output voltage is passed through a resistive divider to place +5V on the negative (regulating) input of the voltage regulator. A Darlington transistor Q1001 provides the current necessary to maintain the +24V power source.

The +5V regulated power supply is controlled by the operational amplifier U451A, which feeds a series-pass power Darlington Q1003. Power is drawn from the rectifier network CR1003. Once again the +5.1V reference is used to regulate the output, by comparison with the output sample fed back to the inverting input via resistor R448. Frequency compensation is provided by feedback capacitor C452. Current limiting is provided by transistor Q355 in conjunction with the resistance network on its base. Overvoltage protection is afforded by the crowbar unit: Q168 SCR, VR162, and R165. When the output voltage causes R165 to see an appropriate positive voltage (+0.6V), the SCR triggers and shunts the power supply to ground.

Power Control Lines

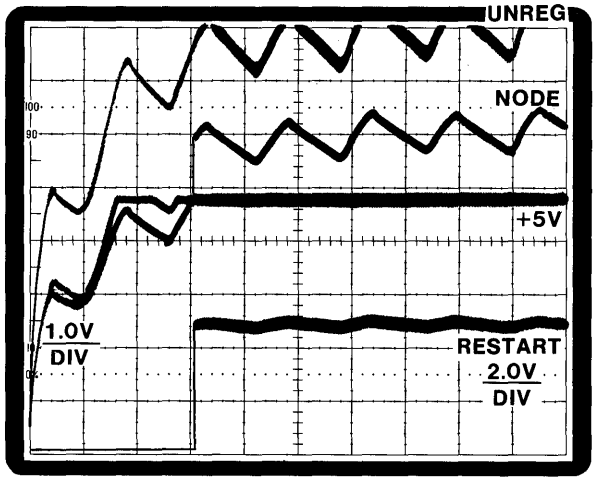
Incorporated in this power supply are three system power control circuits: Power Alarm, Restart, and 24 Off/On. Each is designed to prevent faulty processing in a part of the instrument as power is lost and then returns.

Restart

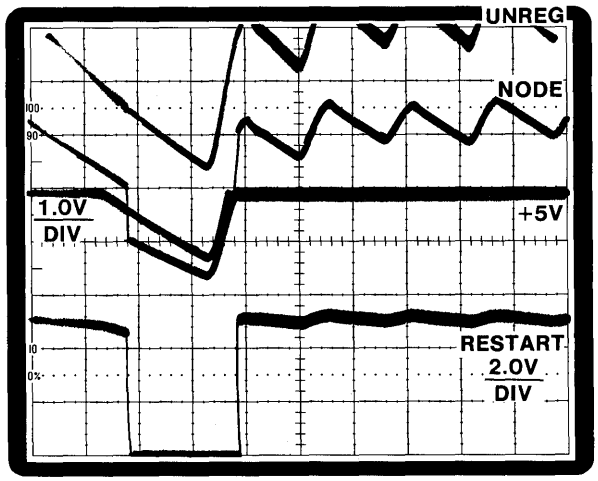
The RESTART signal is generated by the +5V power supply and restart circuit during power-up operations. At power loss, voltages fall off until a certain threshold is reached; at such time the RESTART-1 goes low (RESTART-0). This tells the 6800 microprocessor that insufficient voltage is available and terminates controller operation. By the time power is restored (and proper voltage recovery) the controller will have been initialized and a RESTART-1 signal will start the 6800 up again.

The "restart circuit" uses a comparator, U435A, to detect voltage changes at power-down and power-up. The voltage at the non-inverting input (pin 3) corresponds to a feedback node point, and is also proportional to the unregulated +5V supply waveform. When the nodal point voltage reaches the +5.1V reference level (power-up) the comparator output will switch high to +5.25V (RESTART-1). At this time the nodal point is influenced upward by the RESTART output, holding it well above the +5.1V reference level. (See Figure 6-29A.) It is normal for the RESTART-1 signal to contain some ripple as illustrated.

When power is lost the unregulated and nodal point waveforms fall until the nodal point voltage reaches the +5.1V reference. The U435A output goes low (RESTART-0) with its feedback pulling the node even lower. See Figure 6-29B.



A. POWER UP.

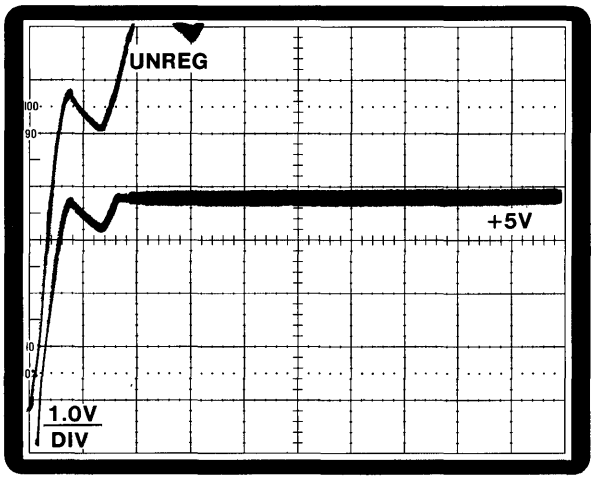


B. POWER DOWN.

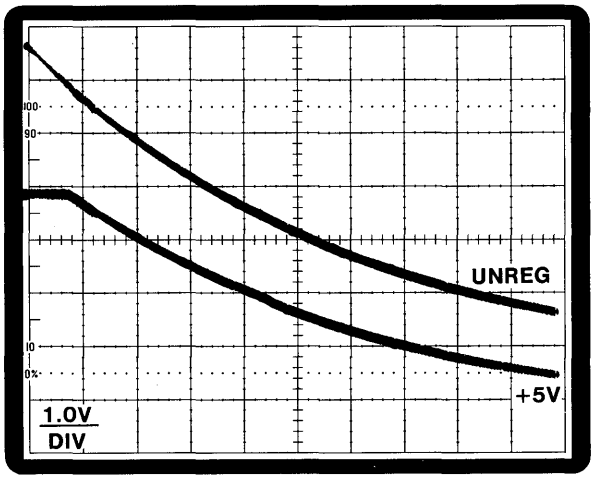
2405-67

Figure 6-29. RESTART Timing (A and B).

Waveforms in Figures 6-30A and B show the relationship between the +5.1V reference and the unregulated supply, as they are influenced by the voltage drop across the series-pass Darlington. Power-up shows a +2.0V drop associated with conduction, and power-off shows a +1.0V drop across the same Q1003 for non-conduction. These signal voltage differences determine the values for R342, R340, and R335, so that the nodal voltage line will intercept the reference line at the proper time to create the conditions shown in Figures 6-29A and B.



A. POWER UP.



B. POWER DOWN, THEN UP. 2405-68

Figure 6-30. +5 Volt Control.

Power Alarm

The "power alarm" circuit senses power failure ahead of the "restart" circuit. It sends a PWRALRM-0 signal to the disc as a warning, allowing enough time for the disc to complete its work (writing a sector) before the RESTART-0 comes (which shuts everything off). Without this PWRALRM signal, the disc could lose power in the middle of a sector.

The PWRALRM signal guarantees that the disc will have sufficient time to complete a sector write, because the disc checks the state of the PWRALRM signal before it begins each sector. If it sees PWRALRM-0, of course a disc is disabled and must wait for RESTART-1 when power returns. If the PWRALRM-0 signal arrives while the disc is writing, it will complete that sector, but cannot go to the next sector until power returns. It is possible for power to be interrupted momentarily while the disc is writing. As long as power returns by the time the disc looks back for a PWRALRM-1 signal, it will continue to write, moving on to the next sector as if nothing happened. On the other hand, if power returns only momentarily (during a power-off period) the disc will not be activated; it must see power (PWRALRM-1) at the proper time indicated by * in Figure 6-31.

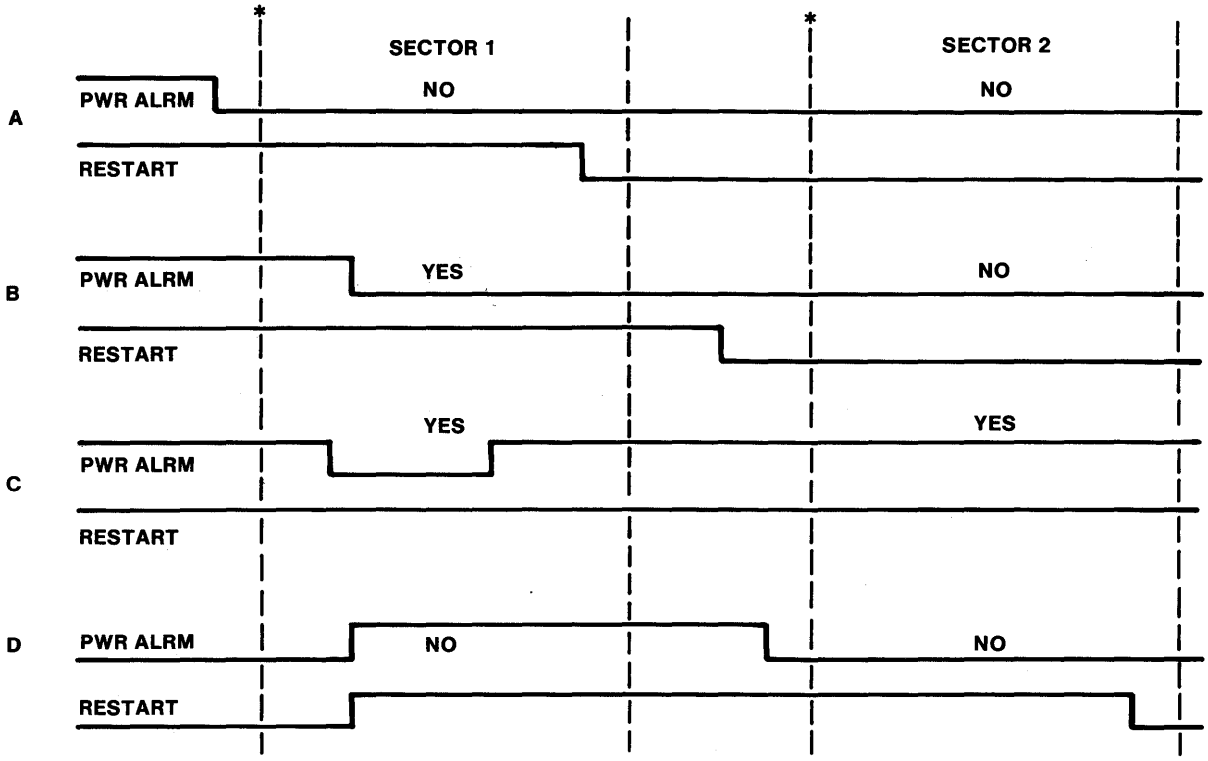


Figure 6-31. RESTART and PWR ALRM Timing.

The theory of operation of the power alarm circuit is now discussed. A +2V signal appears at pin 5 of U451B as a reference. A signal is taken from the unfiltered rectifier array (CR482, CR484). U451B's positive going output passes through diode CR458 and is integrated by capacitor C445. CR448 keeps C445 from leaking current back through U451B and its feedback resistor.

The +5.1V reference appears at the inverting input (pin 9) of U435B, a voltage comparator. The partially integrated output of U451B reaches the non-inverting input (pin 8) of U435B. If the voltage on pin 8 drops below the +5.1V reference on pin 9, the output of U435B goes from +5V to 0. A typical situation is depicted in Figure 6-32. This shows how power loss for a half-cycle or more will allow pin 8 voltage to drop enough to trigger the PWRALRM-0 condition.

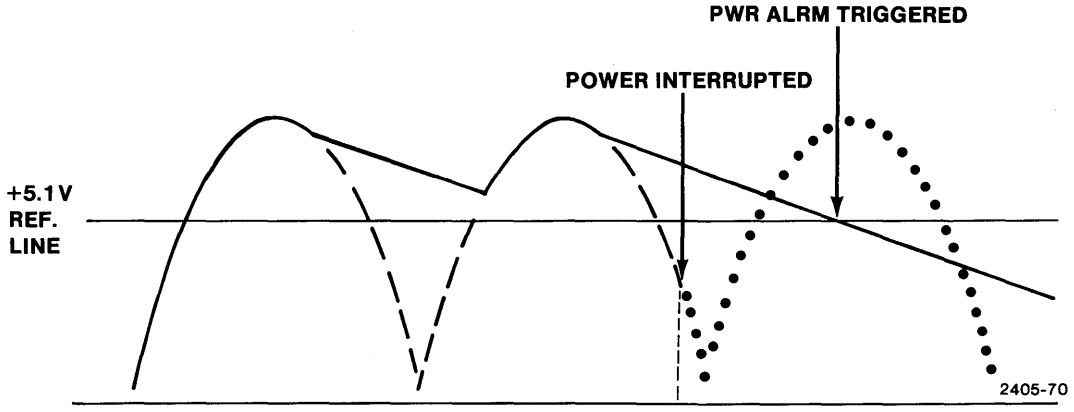


Figure 6-32. PWR ALRM Trigger Timing.

24 Off/On

The purpose of this circuit is to prevent any and all discs from writing when any unit is turned off. When power is completely restored, INGO's come up and RESTART comes up; then all disc supplies are again enabled.

The 24 OFF/ON points on all power supplies (for master unit and each optional disc drive) are tied together. The master unit power supply contains a connected strap (behind nand gate U35C). When power is interrupted to any one of these supplies, its OUTGO signal will indicate a false INGO to the

other supplies. This condition will series through the supplies to the master, where its gate U35C outputs the 24 OFF condition. As 24 OFF/ON goes low this turns on all Q245 transistors, grounding corresponding frequency compensation inputs; this turns off the regulators. Residual +24V from capacitor C185 is shunted to ground through diode CR251 and Q245. Diode CR251 also prevents possible back-bias of transistor Q1001 and the U351 output. The resistor R245 has a value chosen to work with C185 providing a time constant sufficient to limit surge through transistor Q245.

The SYS 5 line allows powered supplies to share +5V with a power-off supply (allowing its transistor Q235 to function, passing the proper OUTGO condition to the other supplies).

Section 7
REPLACEABLE
ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

ACTR	ACTUATOR	PLSTC	PLASTIC
ASSY	ASSEMBLY	QTZ	QUARTZ
CAP	CAPACITOR	RECP	RECEPTACLE
CER	CERAMIC	RES	RESISTOR
CKT	CIRCUIT	RF	RADIO FREQUENCY
COMP	COMPOSITION	SEL	SELECTED
CONN	CONNECTOR	SEMICOND	SEMICONDUCTOR
ELCTLT	ELECTROLYTIC	SENS	SENSITIVE
ELEC	ELECTRICAL	VAR	VARIABLE
INCAND	INCANDESCENT	WW	WIREWOUND
LED	LIGHT EMITTING DIODE	XFMR	TRANSFORMER
NONWIR	NON WIREWOUND	XTAL	CRYSTAL

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
0000L	MATSUSHITA ELECTRIC	200 PARK AVENUE, 54TH FLOOR	NEW YORK, NY 10017
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P O BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
02777	HOPKINS ENGINEERING COMPANY	12900 FOOTHILL BLVD.	SAN FERNANDO, CA 91342
03508	GENERAL ELECTRIC COMPANY, SEMI-CONDUCTOR PRODUCTS DEPARTMENT	ELECTRONICS PARK	SYRACUSE, NY 13201
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867, 19TH AVE. SOUTH	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
09353	C AND K COMPONENTS, INC.	103 MORSE STREET	WATERTOWN, MA 02172
14752	ELECTRO CUBE INC.	1710 S. DEL MAR AVE.	SAN GABRIEL, CA 91776
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
33096	COLORADO CRYSTAL CORPORATION	2303 W 8TH STREET	LOVELAND, CO 80537
50522	MONSANTO CO., ELECTRONIC SPECIAL PRODUCTS	3400 HILLVIEW AVENUE	PALO ALTO, CA 94304
50558	ELECTRONIC CONCEPTS, INC.	526 INDUSTRIAL WAY WEST	EATONTOWN, NJ 07724
56289	SPRAGUE ELECTRIC CO.		NORTH ADAMS, MA 01247
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
72619	DIALIGHT, DIV. AMPEREX ELECTRONIC	203 HARRISON PLACE	BROOKLYN, NY 11237
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
73559	CARLINGSWITCH, INC.	505 NEW PARK AVENUE	WEST HARTFORD, CT 06110
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
80294	BOURNS, INC., INSTRUMENT DIV.	6135 MAGNOLIA AVE.	RIVERSIDE, CA 92506
82877	ROTRON, INC.	7-9 HASBROUCK LANE	WOODSTOCK, NY 12498
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY AND CO., INC.	3029 E WASHINGTON STREET P O BOX 372	INDIANAPOLIS, IN 46206
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-5362-01			CKT BOARD ASSY:CONTROL	80009	670-5362-01
A2	670-5421-01			CKT BOARD ASSY:ROM PAC	80009	670-5421-01
A3	670-5385-00			CKT BOARD ASSY:ROM BOARD	80009	670-5385-00
A4	670-5441-00	B010100	B010114	CKT BOARD ASSY:POWER SUPPLY	80009	670-5441-00
A4	670-5441-01	B010115		CKT BOARD ASSY:POWER SUPPLY	80009	670-5441-01

A1 CKT BOARD ASSY:CONTROL

A1	670-5362-01			CKT BOARD ASSY:CONTROL	80009	670-5362-01
C102	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C105	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C107	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C108	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C111	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C112	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C113	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C114	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C115	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C119	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C120	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C121	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C122	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C123	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
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C128	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C129	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C131	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C132	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
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C136	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C137	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C139	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C144	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
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C238	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C244	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C302	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C303	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C308	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C310	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C314	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C317	290-0245-00			CAP.,FXD,ELCTLT:1.5UF,10%,10V	56289	150D155X9010A2
C318	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	56289	502D226
C319	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M

CONTROL (CONT)

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
C320	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C326	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C330	281-0501-00			CAP.,FXD,CER DI:4.7PF,+/-1PF,500V	72982	301-000S2H0479F
C332	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C335	283-0635-00			CAP.,FXD,MICA D:51PF,1%,100V	00853	D151E510F0
C338	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C344	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C400	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C401	283-0060-00			CAP.,FXD,CER DI:100PF,5%,200V	72982	855-535U2J101J
C402	283-0116-00			CAP.,FXD,CER DI:820PF,5%,500V	72982	801-547B821J
C403	283-0060-00			CAP.,FXD,CER DI:100PF,5%,200V	72982	855-535U2J101J
C404	283-0116-00			CAP.,FXD,CER DI:820PF,5%,500V	72982	801-547B821J
C408	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C412	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C416	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C424	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C430	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C432	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	56289	502D226
C438	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C442	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C443	285-1076-00			CAP.,FXD,PLSTC:0.2UF,5%,100V	14752	230B1B204J
C444	281-0578-00			CAP.,FXD,CER DI:18PF,5%,500V	72982	301-050C0G0180J
C445	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C505	283-0054-00			CAP.,FXD,CER DI:150PF,5%,200V	72982	855-535U2J151J
C506	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C508	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C512	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C516	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C524	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C528	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C538	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C542	283-0065-00			CAP.,FXD,CER DI:0.001UF,5%,100V	72982	805-518-Z5D0102J
C543	283-0220-00			CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N075X7R0103M
C544	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	56289	502D226
C545	290-0771-00			CAP.,FXD,ELCTLT:220UF,+50-10%,10VDC	0000L	ECE-A10V220L
C547	290-0779-00			CAP.,FXD,ELCTLT:10UF,+50-10%,50VDC	56289	502D237
C551	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	56289	502D226
CR319	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02
CR417	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02
CR431	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	80009	152-0066-00
CR432	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	80009	152-0066-00
CR500	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02
CR501	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02
CR502	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02
CR503	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02
Q501	151-0188-00			TRANSISTOR:SILICON,PNP	80009	151-0188-00
Q503	151-0188-00			TRANSISTOR:SILICON,PNP	80009	151-0188-00
R226	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	01121	206A102
R303	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R304	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R305	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	80294	4306R-101-103
R314	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	01121	206A102

CONTROL (CONT)

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R316	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	01121	206A102
R317	321-0326-00			RES.,FXD,FILM:24.3K OHM,1%,0.125W	91637	MFF1816G24301F
R320	315-0333-00			RES.,FXD,CMPSN:33K OHM,5%,0.25W	01121	CB3335
R335	321-0303-00			RES.,FXD,FILM:14K OHM,1%,0.125W	91637	MFF1816G14001F
R336	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
R350	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	80294	4306R-101-103
R400	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
R401	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
R402	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
R403	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
R404	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
R405	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
R431	307-0362-00			RES.,FXD,FILM:13 RES NETWORK	73138	899-1-R120
R442	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
R444	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
R500	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
R501	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
R505	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R506	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R507	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R508	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R517	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	01121	206A102
R529	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R542	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R549	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	01121	CB4315
S253	260-1589-00			SWITCH,PUSH:(6)SPST,0.1A,5V	00779	435166-4
U101	156-0928-00			MICROCIRCUIT,DI:OCTAL BUFFER W/3 STATE OUT	80009	156-0928-00
U103	156-0965-01			MICROCIRCUIT,DI:ADRS MUX REFRESH CNTR	80009	156-0965-01
U105	156-0916-00			MICROCIRCUIT,DI:EIGHT 2-INP 3-STATE BFR	80009	156-0916-00
U107	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U107	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U109	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U109	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U111	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U111	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U113	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U113	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U115	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U115	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U117	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U117	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U119	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U119	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U121	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U121	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U123	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U123	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U125	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U125	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U127	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U127	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U129	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00

CONTROL (CONT)

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U129	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U131	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U131	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U133	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U133	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U135	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U135	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U137	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U137	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U139	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U139	156-1027-01	B010115				
U141	156-1027-00	B010100	B010114	MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-00
U107	156-1027-01	B010115		MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1027-01
U143	156-0600-00			MICROCIRCUIT,DI:QUAD BUS XCVR	80009	156-0600-00
U145	156-0600-00			MICROCIRCUIT,DI:QUAD BUS XCVR	80009	156-0600-00
U147	156-0915-00			MICROCIRCUIT,DI:9-BIT ODD/EVEN PARITY GEN ER	80009	156-0915-00
U149	156-0600-00			MICROCIRCUIT,DI:QUAD BUS XCVR	80009	156-0600-00
U151	156-0600-00			MICROCIRCUIT,DI:QUAD BUS XCVR	80009	156-0600-00
U201	156-0928-00			MICROCIRCUIT,DI:OCTAL BUFFER W/3 STATE OUT	80009	156-0928-00
U205	156-0865-00			MICROCIRCUIT,DI:OCTAL D TYPE FF W/CLEAR	80009	156-0865-00
U207	156-0469-00			MICROCIRCUIT,DI:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
U209	156-0845-00			MICROCIRCUIT,DI:6-BIT COMPARATOR	27014	DM8160N
U211	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	01295	SN74LS74N
U213	156-0617-00			MICROCIRCUIT,DI:DUAL 4 BIT BIN COUNTER	01295	SN74393N
U215	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	01295	SN74LS74N
U217	156-0469-00			MICROCIRCUIT,DI:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
U219	156-0469-00			MICROCIRCUIT,DI:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
U221	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	01295	SN74LS02N
U225	156-0969-00			MICROCIRCUIT,DI:CY REDUNDANCYCHK GEN/CHKR	07263	9401PC
U227	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U229	156-0479-00			MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE	27014	DM74LS32N
U231	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U233	156-0915-00			MICROCIRCUIT,DI:9-BIT ODD/EVEN PARITY GEN ER	80009	156-0915-00
U235	156-0567-00			MICROCIRCUIT,DI:DUAL J-K NEG EDGE TRIG F-F	01295	SN74LS113N
U239	156-0479-00			MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE	27014	DM74LS32N
U241	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U243	156-0916-00			MICROCIRCUIT,DI:EIGHT 2-INP 3-STATE BFR	80009	156-0916-00
U245	156-0465-00			MICROCIRCUIT,DI:8-INPUT NAND GATE	27014	DM74LS304
U247	156-0916-00			MICROCIRCUIT,DI:EIGHT 2-INP 3-STATE BFR	80009	156-0916-00
U249	156-0916-00			MICROCIRCUIT,DI:EIGHT 2-INP 3-STATE BFR	80009	156-0916-00
U251	156-0865-00			MICROCIRCUIT,DI:OCTAL D TYPE FF W/CLEAR	80009	156-0865-00
U253	156-0391-00			MICROCIRCUIT,DI:HEX LATCH WITH CLEAR	01295	SN74LS174N
U301	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
U302	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
U303	156-0426-00			MICROCIRCUIT,DI:MICROPROCESSOR	80009	156-0426-00
U305	156-0391-00			MICROCIRCUIT,DI:HEX LATCH WITH CLEAR	01295	SN74LS174N
U307	156-1013-00			MICROCIRCUIT,DI:SYN SERIAL DATA ADAPTER	80009	156-1013-00
U311	156-0928-00			MICROCIRCUIT,DI:OCTAL BUFFER W/3 STATE OUT	80009	156-0928-00
U313	156-0928-00			MICROCIRCUIT,DI:OCTAL BUFFER W/3 STATE OUT	80009	156-0928-00
U315	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	01295	SN74LS74N
U317	156-0865-00			MICROCIRCUIT,DI:OCTAL D TYPE FF W/CLEAR	80009	156-0865-00
U319	156-0405-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	07263	9602PC
U321	156-0479-00			MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE	27014	DM74LS32N

CONTROL (CONT)

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U323	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U325	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U327	156-0480-00			MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	80009	156-0480-00
U329	156-0763-00			MICROCIRCUIT,DI:HEX CONT BOUNCE ELIMINATOR	80009	156-0763-00
U331	156-0480-00			MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	80009	156-0480-00
U335	156-0733-00			MICROCIRCUIT,DI:DUAL MONOSTABLE MV	80009	156-0733-00
U337	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	01295	SN74LS02N
U339	156-0567-00			MICROCIRCUIT,DI:DUAL J-K NEG EDGE TRIG F-F	01295	SN74LS113N
U341	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	01295	SN74LS74N
U343	156-0480-00			MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	80009	156-0480-00
U345	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	01295	SN74LS74N
U347	156-0479-00			MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE	27014	DM74LS32N
U349	156-0479-00			MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE	27014	DM74LS32N
U351	156-0916-00			MICROCIRCUIT,DI:EIGHT 2-INP 3-STATE BFR	80009	156-0916-00
U401	156-0093-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN7416N
U403	156-0922-00			MICROCIRCUIT,DI:HEX INVERTER W/OPEN COLL	80009	156-0922-00
U405	156-0479-00			MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE	27014	DM74LS32N
U407	156-0656-00			MICROCIRCUIT,DI:DECADE COUNTER	80009	156-0656-00
U409	156-0696-00			MICROCIRCUIT,DI:QUAD CMPLM-OUTPUT & NAND	01295	SN4265N
U411	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U413	156-0852-00			MICROCIRCUIT,DI:HEX BUS DRIVER W/3-STATE	01295	SN74L5367N
U415	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	01295	SN74LS74N
U417	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	01295	SN74LS74N
U419	156-0910-00			MICROCIRCUIT,DI:DUAL DECADE COUNTER	80009	156-0910-00
U423	156-0651-00			MICROCIRCUIT,DI:8-BIT PRL-OUT,SER SHF RGTR	01295	SN74LS164N
U425	156-0785-00			MICROCIRCUIT,DI:256 BIT PROM,W/3 STATE OUT	80009	156-0785-00
U427	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U429	156-0541-00			MICROCIRCUIT,DI:DECODER/DEMULTIPLEXER	27014	DM74LS139N
U433	156-0455-00			MICROCIRCUIT,DI:HEX.BUS VEC	27014	DM8837N
U435	156-0140-00			MICROCIRCUIT,DI:HEX BFR,15V,TTL	01295	SN7417N
U437	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U439	156-0093-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN7416N
U441	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	01295	SN74LS74N
U443	156-0124-00			MICROCIRCUIT,DI:SGL FREQ/PHASE DETECTOR	80009	156-0124-00
U445	156-0121-00			MICROCIRCUIT,DI:DUAL VOLTAGE-CONT MV	80009	156-0121-00
U447	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U451	156-0646-00			MICROCIRCUIT,DI:4 BIT BINARY COUNTER	01295	SN74LS93N
U507	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U509	156-0386-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10N
U511	156-0567-00			MICROCIRCUIT,DI:DUAL J-K NEG EDGE TRIG F-F	01295	SN74LS113N
U513	156-0646-00			MICROCIRCUIT,DI:4 BIT BINARY COUNTER	01295	SN74LS93N
U515	156-0910-00			MICROCIRCUIT,DI:DUAL DECADE COUNTER	80009	156-0910-00
U519	156-0910-00			MICROCIRCUIT,DI:DUAL DECADE COUNTER	80009	156-0910-00
U523	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	01295	SN74LS74N
U525	156-0301-00			MICROCIRCUIT,DI:8-BIT PAR-IN SER-OUT SR	07263	74166PC
U527	156-0140-00			MICROCIRCUIT,DI:HEX BFR,15V,TTL	01295	SN7417N
U537	156-0567-00			MICROCIRCUIT,DI:DUAL J-K NEG EDGE TRIG F-F	01295	SN74LS113N
U539	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	01295	SN74LS74N
U541	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U549	156-0285-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR,12V,1A	80009	156-0285-00
VR548	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	80009	152-0195-00
Y505	158-0107-00			XTAL UNIT,QTZ:10MHZ,0.0015%,SERIES	33096	PB1094

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				A2 CKT BOARD ASSY:ROM PAC		
A2	670-5421-01			CKT BOARD ASSY:ROM PAC	80009	670-5421-00
C1	290-0106-00			CAP.,FXD,ELCTLT:10UF,+75-10%,15V	56289	30D106G015BA9
C2	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
Q1	151-0324-00			TRANSISTOR:SILICON,PNP	80009	151-0324-00
R1	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R2	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
U1	156-1102-00			MICROCIRCUIT,DI:ROM,CUSTOM,MASK	80009	156-1102-00
U2	156-1103-00			MICROCIRCUIT,DI:ROM,CUSTOM MASK	80009	156-1103-00
U3	156-1104-00			MICROCIRCUIT,DI:ROM,CUSTOM MASK	80009	156-1104-00
U4	156-1105-00			MICROCIRCUIT,DI:ROM,CUSTOM MASK	80009	156-1105-00
U5	156-0469-00			MICROCIRCUIT,DI:3-LINE TO 8-LINE DECODER	01295	SN74LS138N

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				A3 CKT BOARD ASSY:ROM BOARD		
A3	670-5385-00			CKT BOARD ASSY:ROM BOARD	80009	670-5385-00
C121	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C131	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C141	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C151	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C161	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C209	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C211	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C221	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C231	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C241	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C251	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C261	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C271	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C321	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C331	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C341	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C361	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C431	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C481	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	56289	502D226
C541	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C561	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C621	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C631	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C641	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C661	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
R311	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
R621	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
U121	156-1067-00			MICROCIRCUIT,DI:2048 X 8 ROM CUSTOM MASK	80009	156-1067-00
U131	156-1068-00			MICROCIRCUIT,DI:2048 X 8 ROM CUSTOM MASK	80009	156-1068-00
U141	156-1069-00			MICROCIRCUIT,DI:2048 X 8 ROM CUSTOM MASK	80009	156-1069-00
U151	156-1070-00			MICROCIRCUIT,DI:2048 X 8 ROM CUSTOM MASK	80009	156-1070-00
U161	156-1071-00			MICROCIRCUIT,DI:2048 X 8 ROM CUSTOM MASK	80009	156-1071-00
U201	156-1072-00			MICROCIRCUIT,DI:2048 X 8 ROM CUSTOM MASK	80009	156-1072-00
U211	156-1073-00			MICROCIRCUIT,DI:2048 X 8 ROM CUSTOM MASK	80009	156-1073-00
U221	156-1074-00			MICROCIRCUIT,DI:2048 X 8 ROM CUSTOM MASK	80009	156-1074-00
U231	156-1075-00			MICROCIRCUIT,DI:2048 X 8 ROM CUSTOM MASK	80009	156-1075-00
U241	156-1076-00			MICROCIRCUIT,DI:2048 X 8 ROM CUSTOM MASK	80009	156-1076-00
U251	156-1077-00			MICROCIRCUIT,DI:2048 X 8 ROM CUSTOM MASK	80009	156-1077-00
U261	156-1078-00			MICROCIRCUIT,DI:2048 X 8 ROM CUSTOM MASK	80009	156-1078-00
U271	156-1079-00			MICROCIRCUIT,DI:2048 X 8 ROM CUSTOM MASK	80009	156-1079-00
U321	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	01295	SN74LS02N
U331	156-0480-00			MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	80009	156-0480-00
U361	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-00
U431	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U441	156-1026-00			MICROCIRCUIT,DI:4 LINE TO 1 LINE DECODER	80009	156-1026-00
U521	156-0381-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATES	01295	SN74LS86N
U531	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00

ROM BOARD (CONT)

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U541	156-0940-09			MICROCIRCUIT,DI:FPLA PROGRAMMED	80009	156-0940-09
U561	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-00
U621	156-0645-00			MICROCIRCUIT,DI:SCHMITT-TRIG POS NAND GATE	01295	SN74LS14N
U631	156-0960-06			MICROCIRCUIT,DI:PROM,PROGRAMMED	80009	156-0960-06
U641	156-0973-00			MICROCIRCUIT,DI:1024 X 8 PROM	80009	156-0973-00
U661	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				A4 CKT BOARD ASSY:POWER SUPPLY		
A4	670-5441-00	B010100	B010114	CKT BOARD ASSY:POWER SUPPLY	80009	670-5441-00
A4	670-5441-01	B010115		CKT BOARD ASSY:POWER SUPPLY	80009	670-5441-01
C168	290-0526-00			CAP.,FXD,ELCTLT:6.8UF,20%,6V	90201	TDC685M006EL
C180	290-0771-00			CAP.,FXD,ELCTLT:220UF,+50-10%,10VDC	0000L	ECE-A10V220L
C185	290-0770-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	502D230
C251	281-0525-00			CAP.,FXD,CER DI:470PF,+/-94PF,500V	04222	7001-1364
C275	290-0471-00			CAP.,FXD,ELCTLT:17000UF,+75-10%,25V	56289	36D8084
C285	290-0760-00			CAP.,FXD,ELCTLT:2200UF,+50-10%,25V	56289	D76253
C325	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C445	285-1133-00			CAP.,FXD,PLSTC:0.33UF,1%,100V	50558	MH12D334F
C449	290-0534-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	196D105X0035HA1
C451	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C452	283-0028-00			CAP.,FXD,CER DI:0.0022UF,20%,50V	56289	19C606
C475	290-0828-00			CAP.,FXD,ELCTLT:8800UF,+75-10%,40V	90201	CGS882U040U3C3PL
CR30	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02
CR251	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02
CR385	152-0585-00			SEMICOND DEVICE:SILICON,BRIDGE,75V,75MA	80009	152-0585-00
CR458	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02
CR482	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02
CR484	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02
F162	159-0096-00			FUSE,CARTRIDGE:3AG,7.5A,32V,0.5 SEC	71400	AGC 7 1/2
Q168	151-0521-00			SCR:SI,C122B,MU-27	03508	C122B
Q235	151-0302-00			TRANSISTOR:SILICON,NPN	80009	151-0302-00
Q245	151-0302-00			TRANSISTOR:SILICON,NPN	80009	151-0302-00
Q355	151-0302-00			TRANSISTOR:SILICON,NPN	80009	151-0302-00
R32	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
R34	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
R125	315-0121-00	XB010116		RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
R126	315-0121-00	XB010116		RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
R165	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
R245	315-0510-04			RES.,FXD,CMPSN:51 OHM,5%,0.25 W	01121	CB5105
R246	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
R247	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
R248	321-0348-00			RES.,FXD,FILM:41.2K OHM,1%,0.125W	91637	MFF1816G41201F
R249	321-0173-00			RES.,FXD,FILM:619 OHM,1%,0.125W	91637	MFF1816G619R0F
R252	321-0170-00			RES.,FXD,FILM:576 OHM,1%,0.125W	91637	MFF1816G576R0F
R260	321-0230-00			RES.,FXD,FILM:2.43K OHM,1%,0.125W	91637	MFF1816G24300F
R262	308-0643-00			RES.,FXD,WW:0.1 OHM,3%,3W	91637	RS2B-ER1000H
R268	308-0701-00			RES.,FXD,WW:0.12 OHM,5%,2W	75042	BWH-R1200J
R335	321-0342-00			RES.,FXD,FILM:35.7K OHM,1%,0.125W	91637	MFF1816G35701F
R340	321-0328-00			RES.,FXD,FILM:25.5K OHM,1%,0.125W	91637	MFF1816G25501F
R342	321-0283-00			RES.,FXD,FILM:8.66K OHM,1%,0.125W	91637	MFF1816G86600F
R345	322-0225-00			RES.,FXD,FILM:2.15K OHM,1%,0.25W	91637	MFF1421G21500F
R348	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
R350	311-1223-00			RES.,VAR,NONWIR:250 OHM,10%,0.50W	32997	3386F-T04-251
R352	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
R355	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	01121	CB1625
R360	321-0033-00			RES.,FXD,FILM:21.5 OHM,1%,0.125W	91637	MFF1816G21R50F
R362	315-0510-04			RES.,FXD,CMPSN:51 OHM,5%,0.25 W	01121	CB5105

POWER SUPPLY (CONT)

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R418	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
R420	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R422	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
R428	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
R430	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R432	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
R442	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R445	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R447	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
R448	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
R453	315-0433-00			RES.,FXD,CMPSN:43K OHM,5%,0.25W	01121	CB4335
R458	321-0283-00			RES.,FXD,FILM:8.66K OHM,1%,0.125W	91637	MFF1816G86600F
R460	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
R461	321-0336-00			RES.,FXD,FILM:30.9 OHM,1%,0.125W	91637	MFF1816G30901F
R462	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
R463	321-0336-00			RES.,FXD,FILM:30.9 OHM,1%,0.125W	91637	MFF1816G30901F
U35	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U135	156-0171-00			MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE	01295	SN7432N
U325	156-0140-00			MICROCIRCUIT,DI:HEX BFR,15V,TTL	01295	SN7417N
U351	156-0071-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	80009	156-0071-00
U435	156-0570-00			MICROCIRCUIT,LI:DUAL HIGH SPEED COMPARATOR	80009	156-0570-00
U451	156-0158-00			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	80009	156-0158-00
VR162	152-0175-00			SEMICOND DEVICE:ZENER,0.4W,5.6V,5%	80009	152-0175-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS		
A1001	119-0813-00			SELECTOR,VOLTS:W/LINE FLTR RCPT & FUSE	02777	F65003
B1003	119-0492-00			FAN,AXIAL:MUFFIN TYPE,3 INCH DIA,115V	82877	SU2C5
B1005	----- -----			PART OF 119-0977-00		
B1007	----- -----			PART OF 119-0977-00		
CR1001	152-0475-00			SEMICOND DEVICE:RECT,SILICON,50V,12A	80009	152-0475-00
CR1003	152-0618-00			SEMICOND DEVICE:RECT,SI,50V,15A,HV BRDG	80009	152-0618-00
DS1001	150-1001-00			LT EMITTING DIO:RED,660NM,100MA MAX(OPT 31)	50522	MV5024
DS1002	150-1001-00			LT EMITTING DIO:RED,660NM,100MA MAX(OPT30;31)	50522	MV5024
DS1003	150-1052-00			LT EMITTING DIO:RED,655NM,50MA(OPT 31)	72619	559-0101-001
DS1004	150-1052-00			LT EMITTING DIO:RED,655NM,50MA	72619	559-0101-001
DS1005	150-1052-00			LT EMITTING DIO:RED,655NM,50MA	72619	559-0101-001
DS1006	150-1052-00			LT EMITTING DIO:RED,655NM,50MA	72619	559-0101-001
DS1007	150-1052-00			LT EMITTING DIO:RED,655NM,50MA	72619	559-0101-001
DS1008	150-1052-00			LT EMITTING DIO:RED,655NM,50MA	72619	559-0101-001
F1001	159-0019-00			FUSE,CARTRIDGE:3AG,1A,250V,SLOW BLOW	71400	MDL1
F1001	159-0023-00			FUSE,CARTRIDGE:3AG,2A,250V,SLOW-BLOW(OPT 30)	14400	MDX 2
Q1001	151-0656-00			TRANSISTOR:SILICON,NPN	04713	SJE1972
Q1003	151-0656-00			TRANSISTOR:SILICON,NPN	04713	SJE1972
S1001	260-1804-00			SWITCH,ROCKER:DPDT,15A,125VAC,ON/OFF	73559	LTGM-0501-GNXTE5
S1002	260-1822-00			SWITCH,TOGGLE:SPDT,0.4A,W/INDICATOR BEZEL	09353	7101J62-Z-B-E-22
S1003	260-1822-00			SWITCH,TOGGLE:SPDT,0.4A,W/INDICATOR BEZEL	09353	7101J62-Z-B-E-22
T1001	120-1168-00			XFMR,PWR,STPDN:	80009	120-1168-00

Section 8

SCHEMATICS AND DIAGRAMS

Symbols and Reference Designators

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).

Resistors = Ohms (Ω).

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

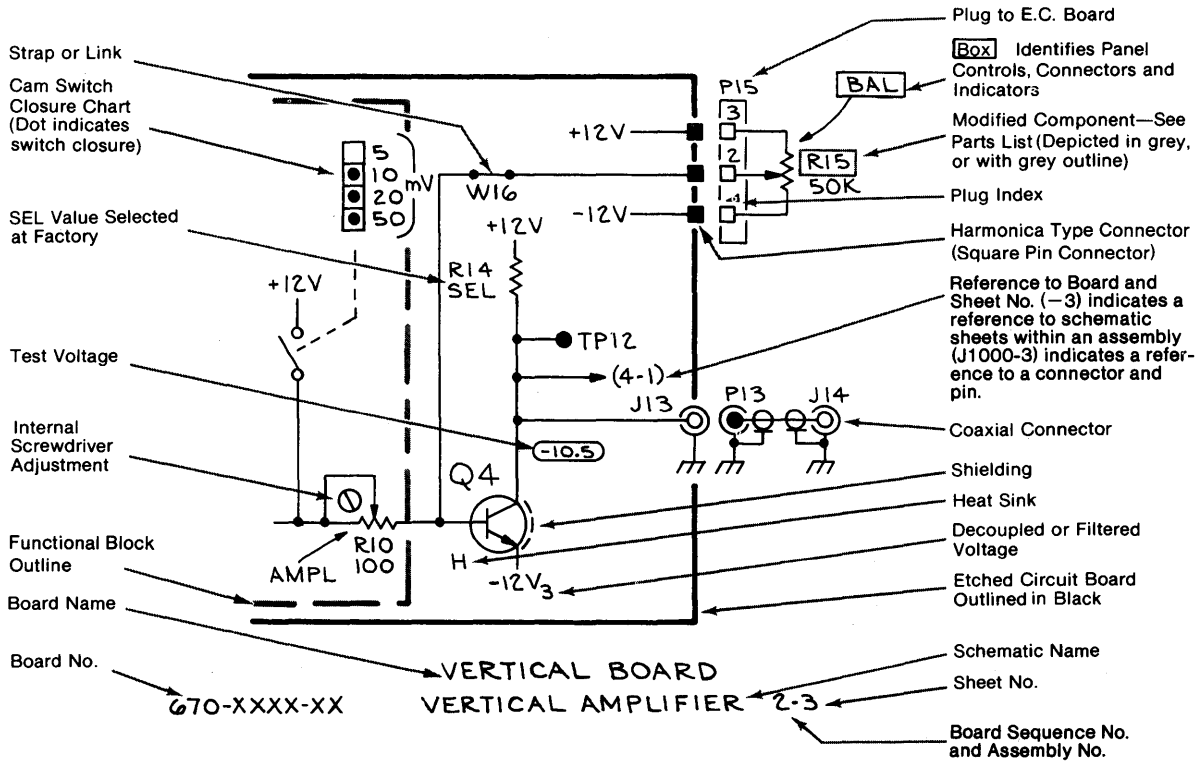
Abbreviations are based on ANSI Y1.1-1972.
Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

The following prefix letters are used as reference designators to identify components or assemblies on the diagrams.

A	Assembly, separable or repairable (circuit board, etc)	H	Heat dissipating device (heat sink, heat radiator, etc)	S	Switch or contactor
AT	Attenuator, fixed or variable	HR	Heater	T	Transformer
B	Motor	HY	Hybrid circuit	TC	Thermocouple
BT	Battery	J	Connector, stationary portion	TP	Test point
C	Capacitor, fixed or variable	K	Relay	U	Assembly, inseparable or non-repairable (integrated circuit, etc.)
CB	Circuit breaker	L	Inductor, fixed or variable	V	Electron tube
CR	Diode, signal or rectifier	M	Meter	VR	Voltage regulator (zener diode, etc.)
DL	Delay line	P	Connector, movable portion	W	Wirestrap or cable
DS	Indicating device (lamp)	Q	Transistor or silicon-controlled rectifier	Y	Crystal
E	Spark Gap, Ferrite bead	R	Resistor, fixed or variable	Z	Phase shifter
F	Fuse	RT	Thermistor		
FL	Filter				

The following special symbols may appear on the diagrams:



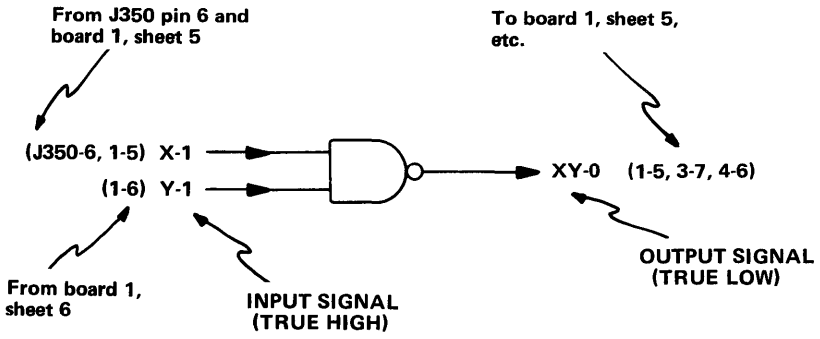
1. TRUE HIGH and TRUE LOW Signals

Signal names on the schematics are followed by −1 or −0. A TRUE HIGH signal is indicated by −1, and a TRUE LOW signal is indicated by −0.

SIGNAL−1 = TRUE HIGH
SIGNAL−0 = TRUE LOW

2. Cross-References

Schematic cross-references (from/to information) are included on the schematics. The "from" reference only indicates the signal "source," and the "to" reference lists all loads where the signal is used. All from/to information will be enclosed in parentheses.



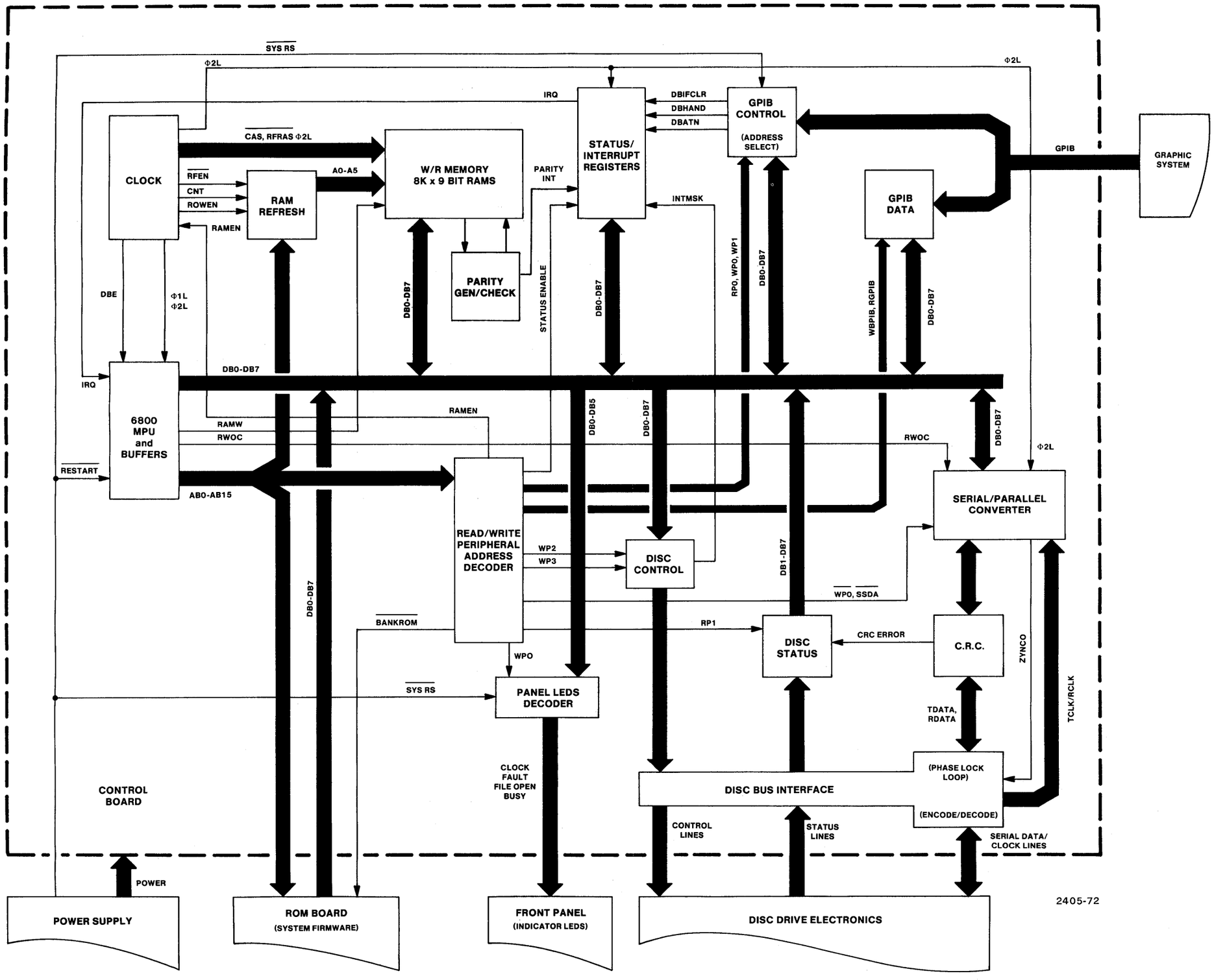


Figure 8-1. Control Board Block Diagram.

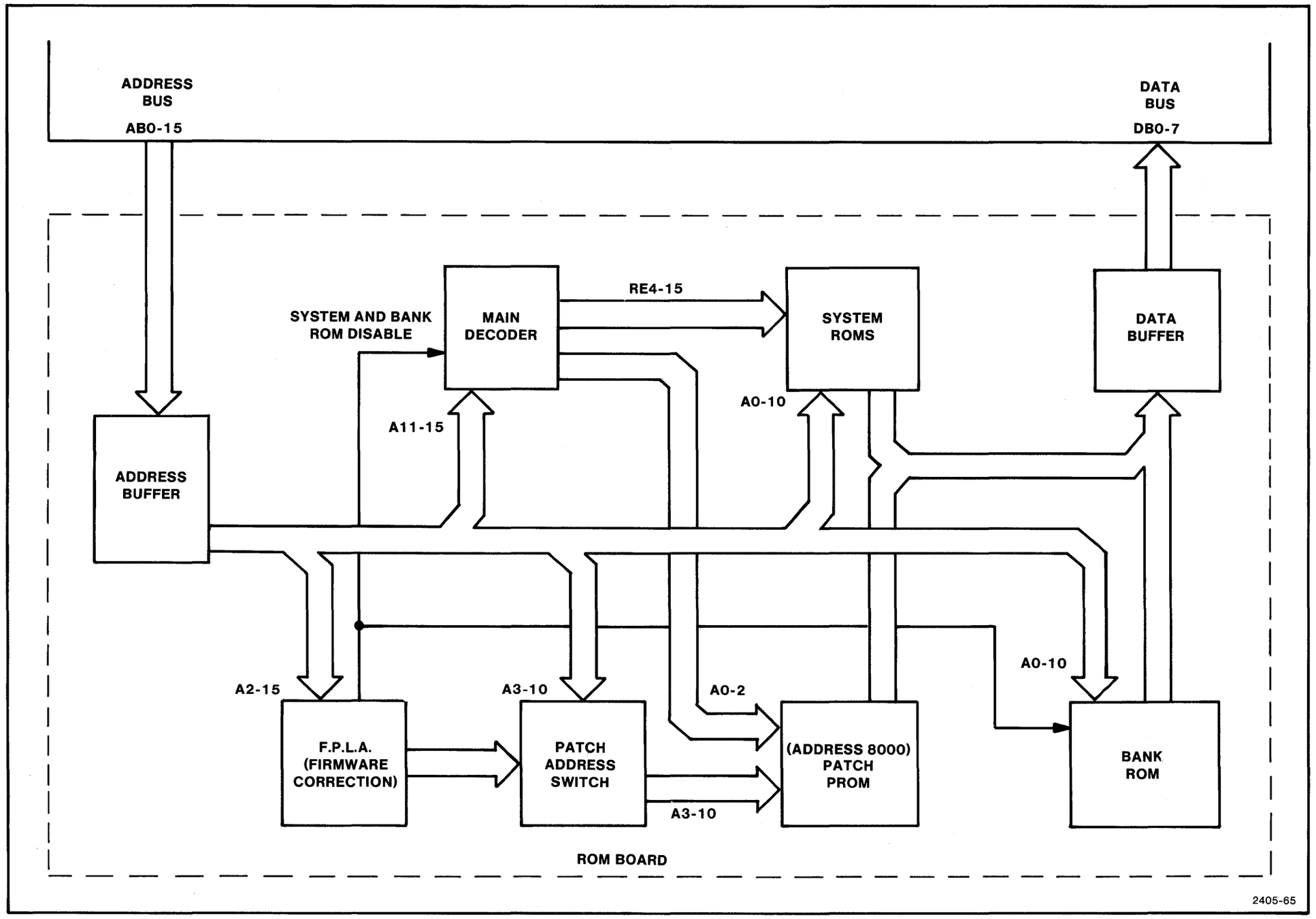


Figure 8-2. ROM Board Block Diagram.

INDEX

CABLING DIAGRAMS

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Table 8-1

CABLE ASSEMBLIES KEY

Cabling Diagram Code	Mech. Illustr. Fig/Index	Description	Part Number
1	2-114	Power Supply J1 to Control Board J533; 40 cond. ribbon assy.	175-2120-00
2	-115	Power Supply J6 to Disc Drive Board J1; 50 cond. ribbon assy.	175-2147-00
3	-10	Control Board J300 to ROM Board J1; 50 cond. ribbon assy.	175-2147-00
4	-111	Power Supply J1 to Control Board J545; 9 cond., 1 end brown/1 end black	Part of wire set: 198-3814-00
5	-93	Power Supply J12 to Power Transistors (Q1001 & Q1003); 6 cond. ribbon/brown conn.	Part of wire set: 198-3813-00
6	-110	Control Board J500 to Indicator LEDS; 8 cond. ribbon assy.	Part of wire set: 198-3814-00
7	-91	Power Supply J2/J3 to Disc Drive Board J5; 6 cond. ribbon/orange connector.	Part of wire set: 198-3813-00
8	-92	Power Switch to Line Selector/Filter; 4 cond. twisted assy.	198-3813-00
9	-93	Power Supply J9 to "Unit Busy: Write Protect"; 6 cond. ribbon/white connector.	198-3813-00
11		Line Selector/Filter to Disc Drive J4 to Fan	198-3897-00
12	-96	Power Supply J10 to Power Switch; 2 wire with green connector (352-0198-05)	Part of wire set: 198-3813-00
10	-114	Main Cabinet to Aux. Cabinet; 40 cond. "armored" ribbon cable	175-2122-00
13	2 in OPTION 31	Rear Panel J1 to Interconnect J7 & J5; 40 cond. ribbon	175-2149-00
14	2 in OPTION 30	Rear Panel J1 to Interconnect J7 (only); 40 cond. ribbon	175-2121-00
15	OPTION 31	Power Supply J6 to Second Disc Drive Board J1; 50 cond. ribbon assy.	175-2148-00
16	OPTION 31	Power Supply J2 to Second Drive Board J5; 6 cond. ribbon assy./pink connector.	Part of wire set: 198-3815-00

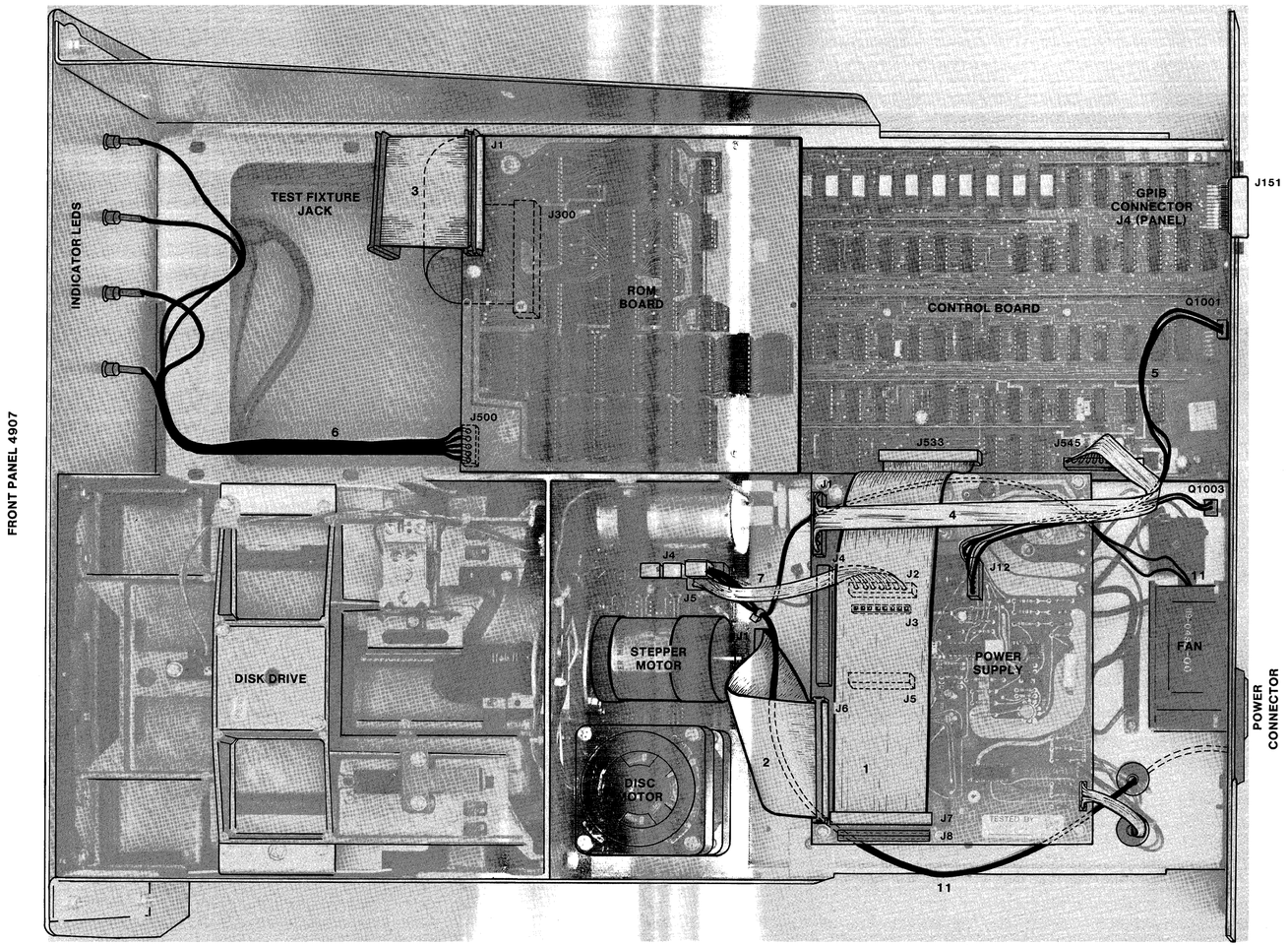


Figure 8-3. Main Cabinet Cabling Diagram (Exposed Runs).

Table 8-2

TRANSFORMER WIRING CODE

Connect Points (Figure 8-4)	Wire Colors [Number Code]
A	RED [2] Spagetti
B	RED [2] Spagetti
C	YELLOW [4] Spagetti
D	YELLOW [4] Spagetti
0 (Both)	BLACK [0]
1	BROWN [1] Spagetti
5	RED (BLACK/WHITE STRIPES) [2-0-9]
6 (Both)	BLUE [6] Spagetti
7	VIOLET (BLACK/WHITE STRIPES)[7-0-9]

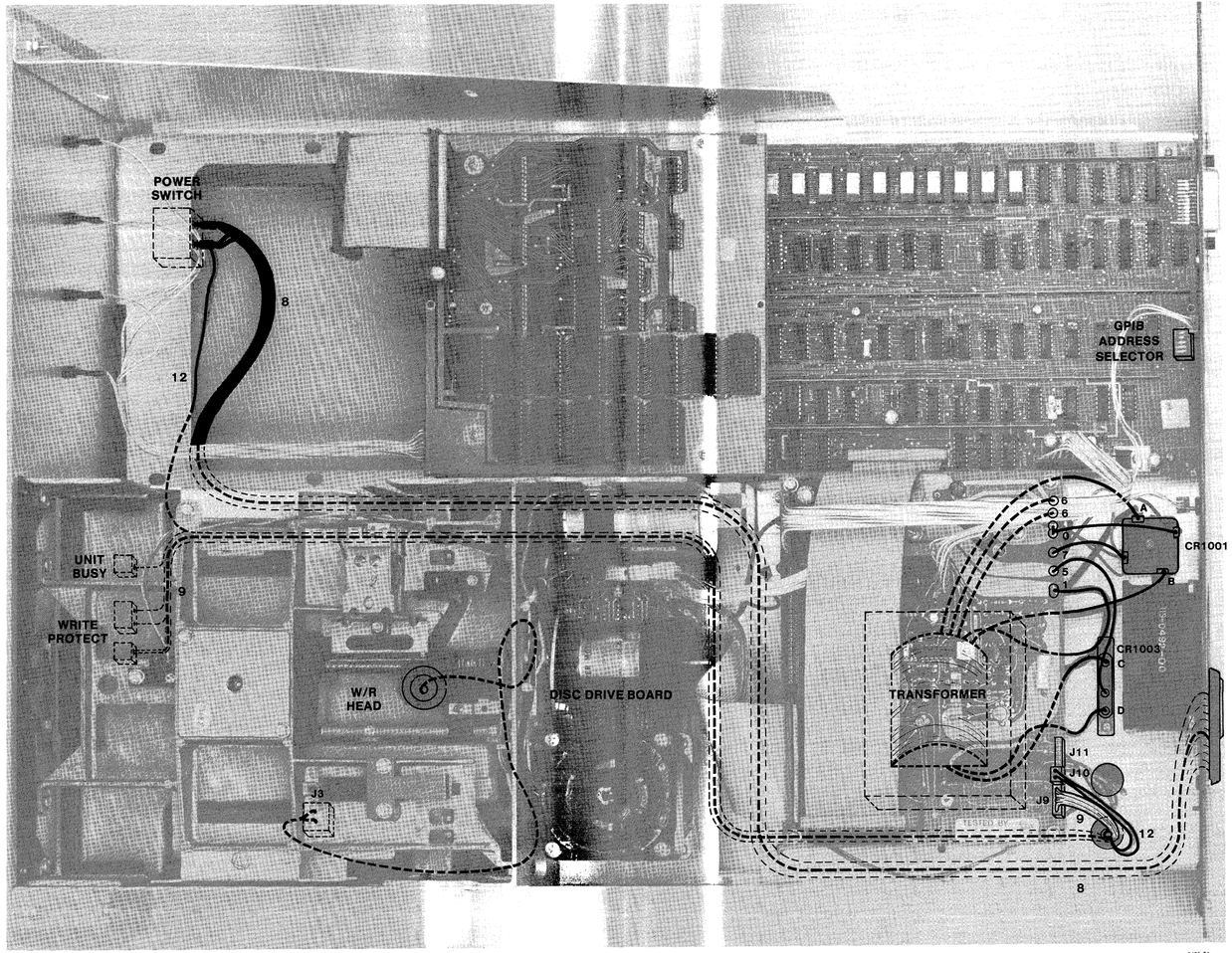


Figure 8-4. Main Cabinet Cabling (Hidden Runs).

See Interconnect Schematic Sheets 3-2 and 3-3.

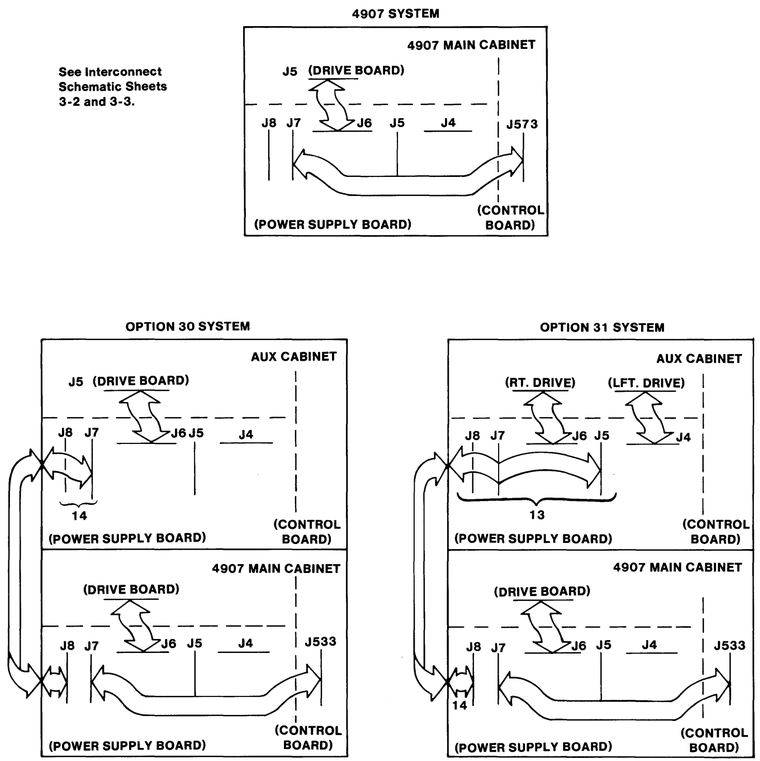


Figure 8-5. Power Supply Interconnect Configurations.

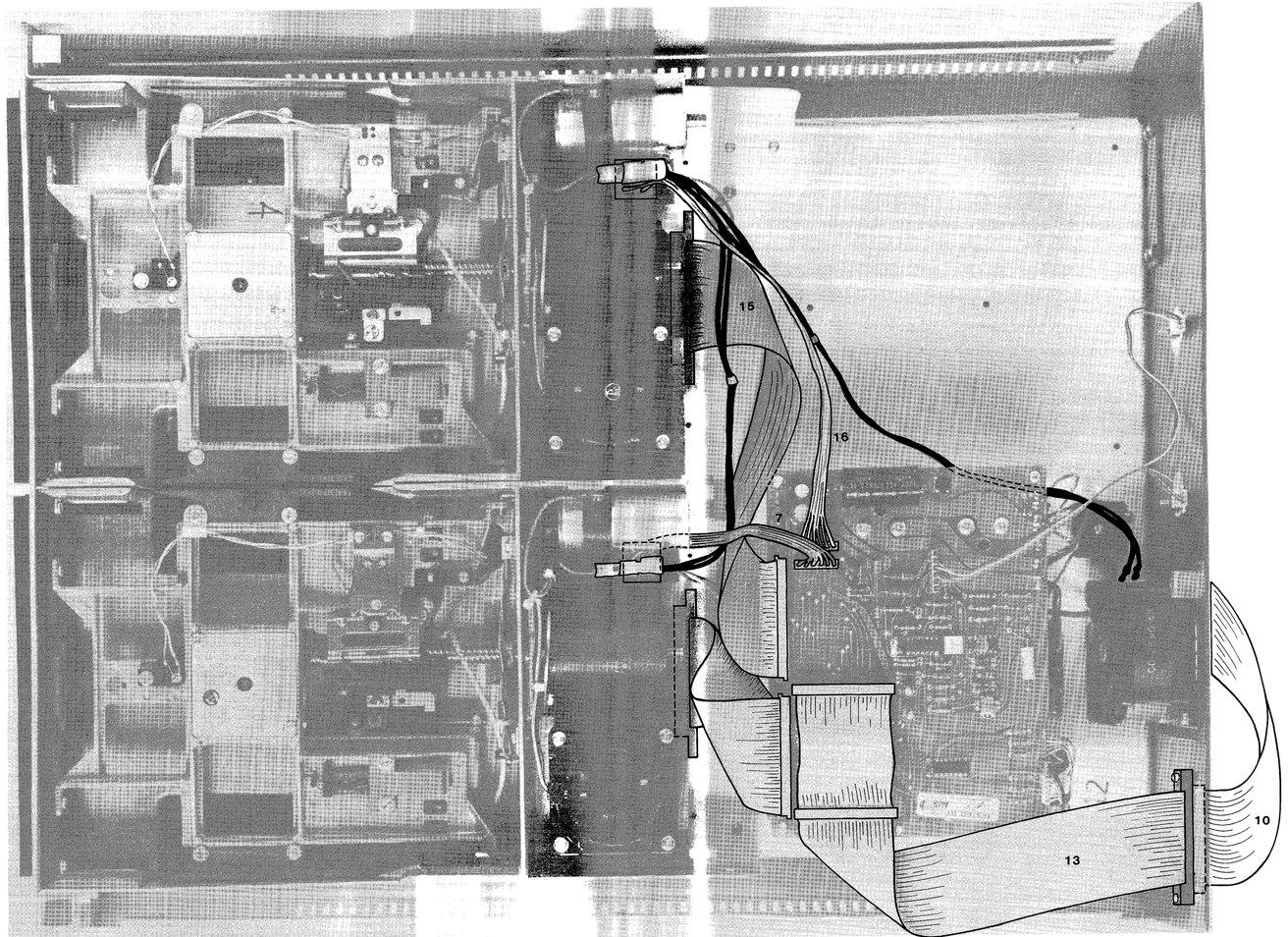


Figure 8-6. Auxiliary Cabinets Cabling.

INDEX

CONTROL BOARD

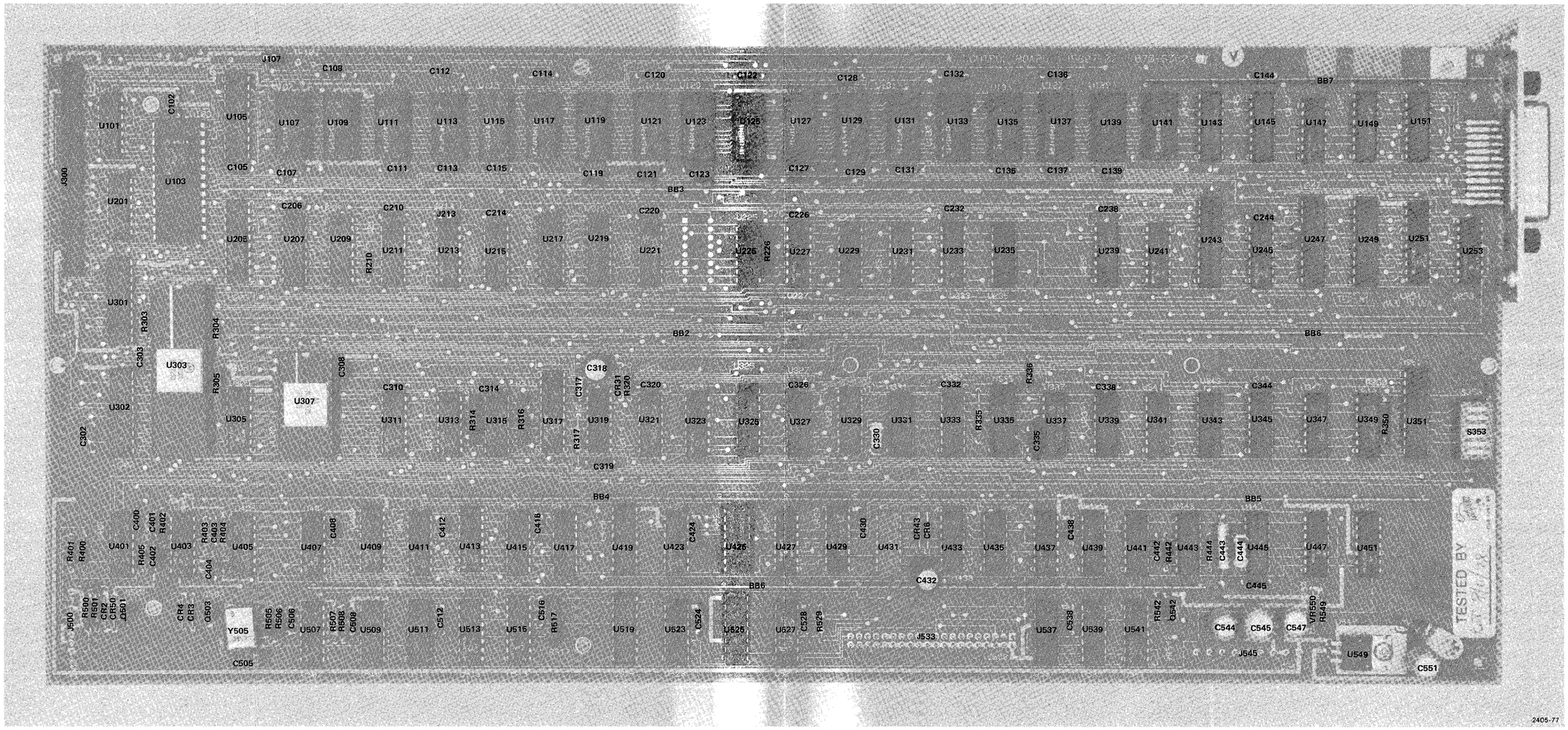
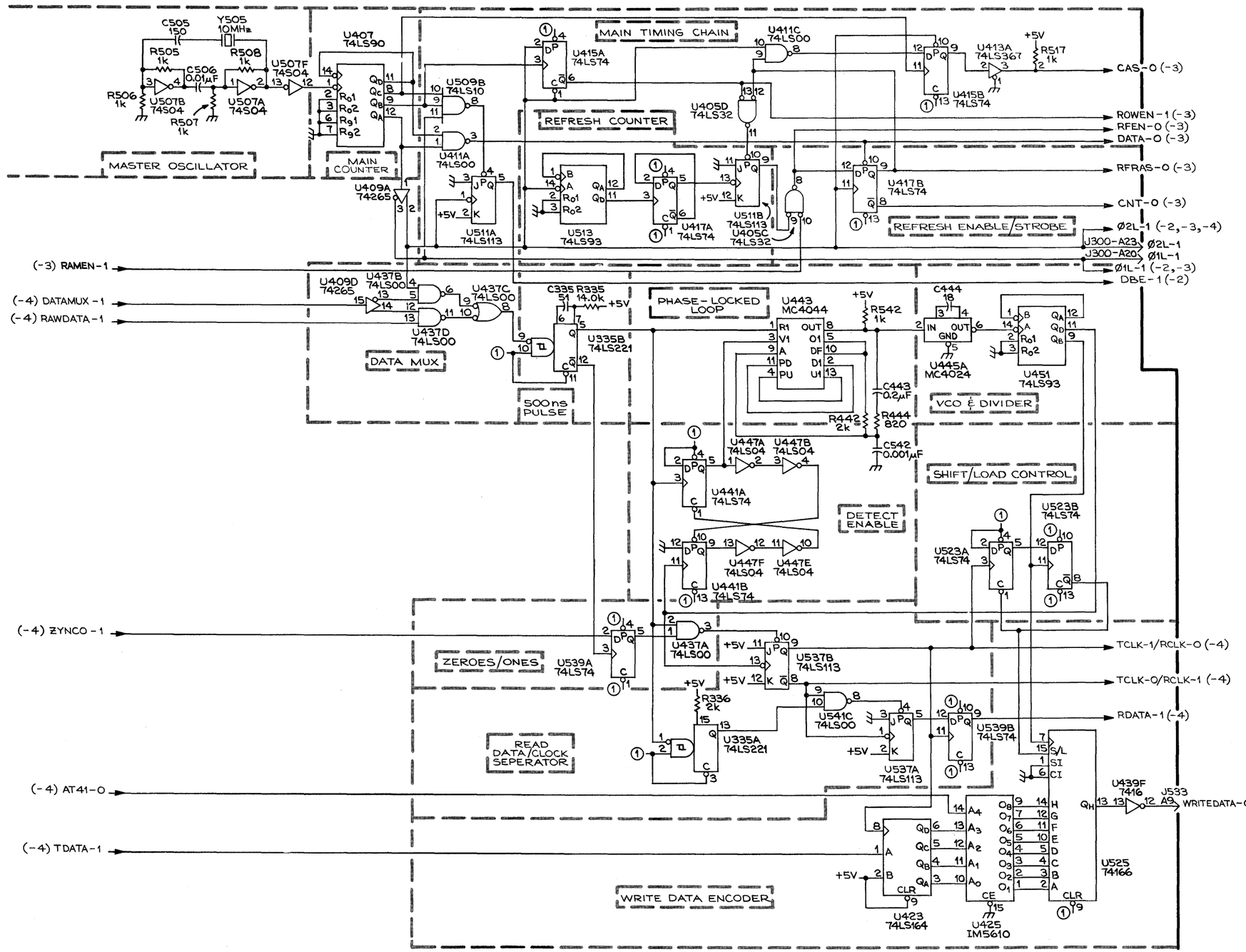


Figure 8-7. Control Board Component Locations (670-5362-01).

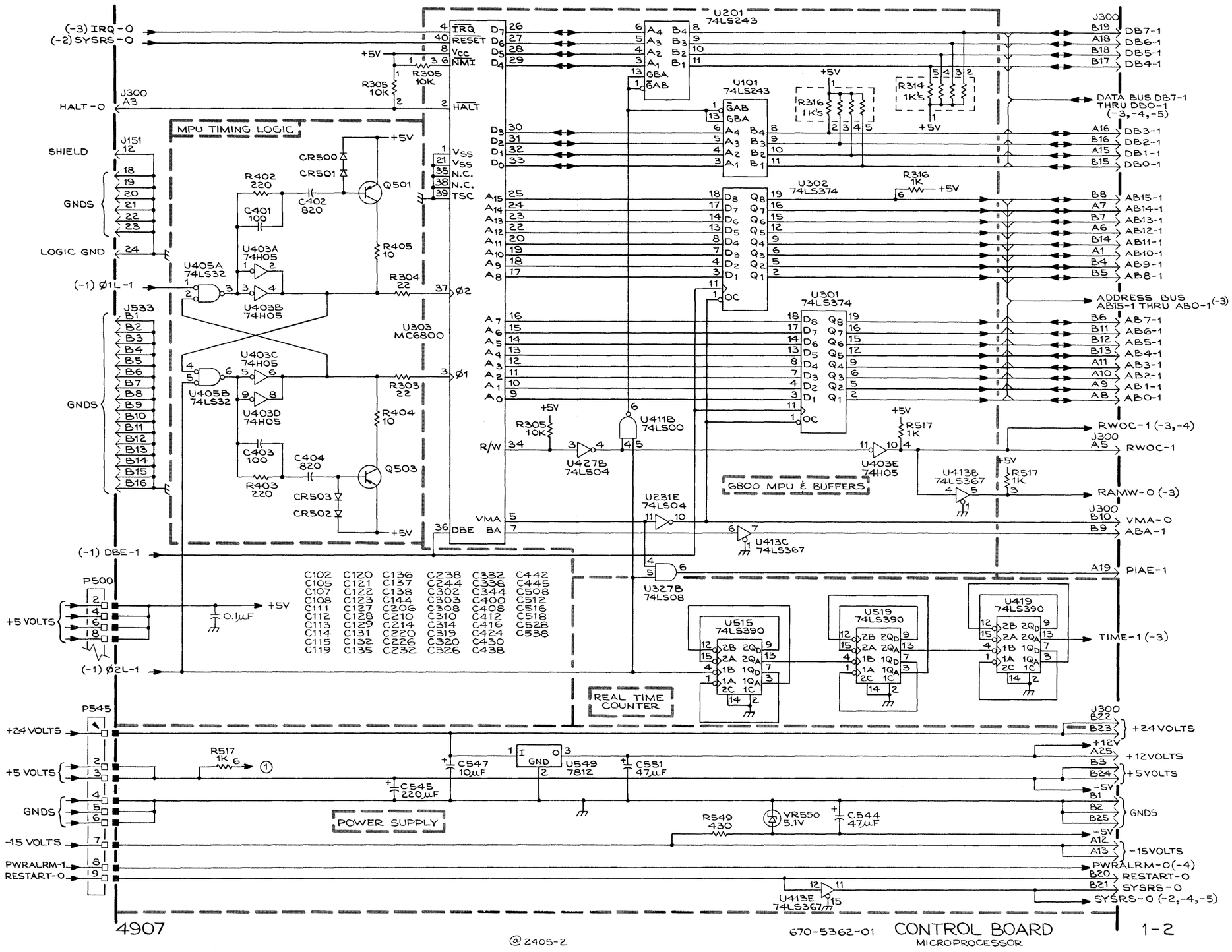


CONTROL BOARD
TIMING, ENCODE, DECODE
(670-5362-01)
1-1

4907

@ 2405-1

670-5362-01 CONTROL BOARD
TIMING, ENCODE, DECODE 1-1

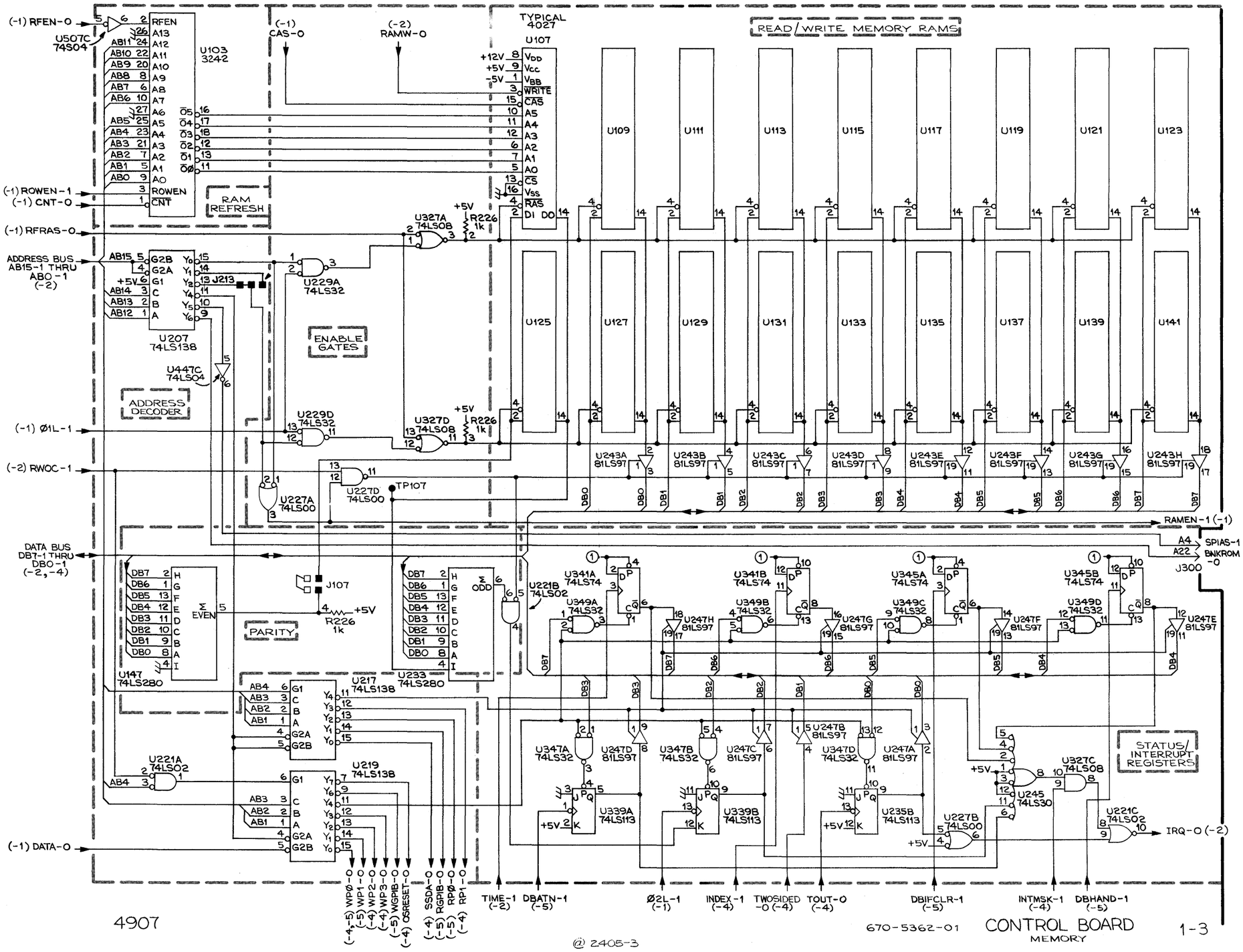


4907

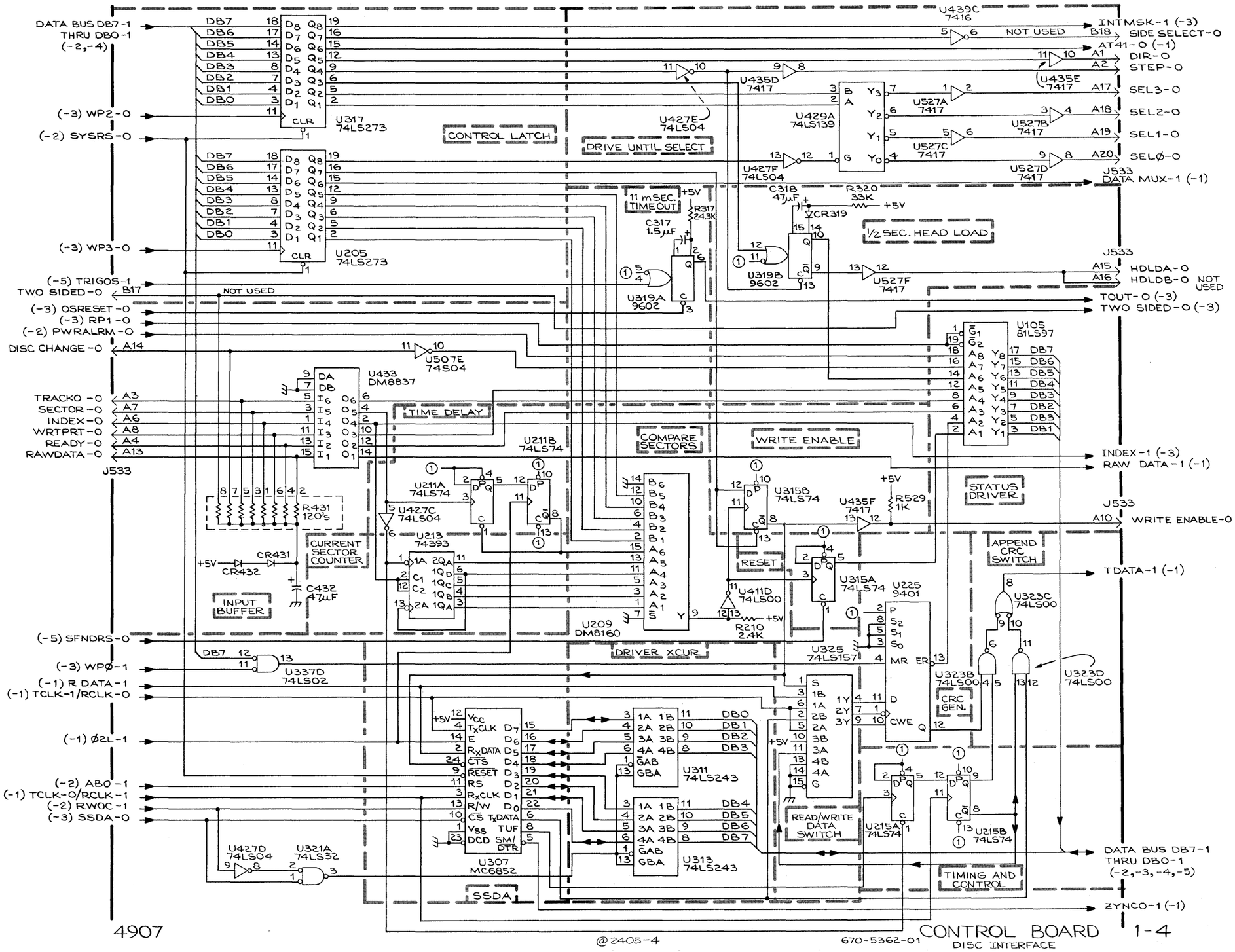
@2405-2

670-5362-01 CONTROL BOARD MICROPROCESSOR 1-2

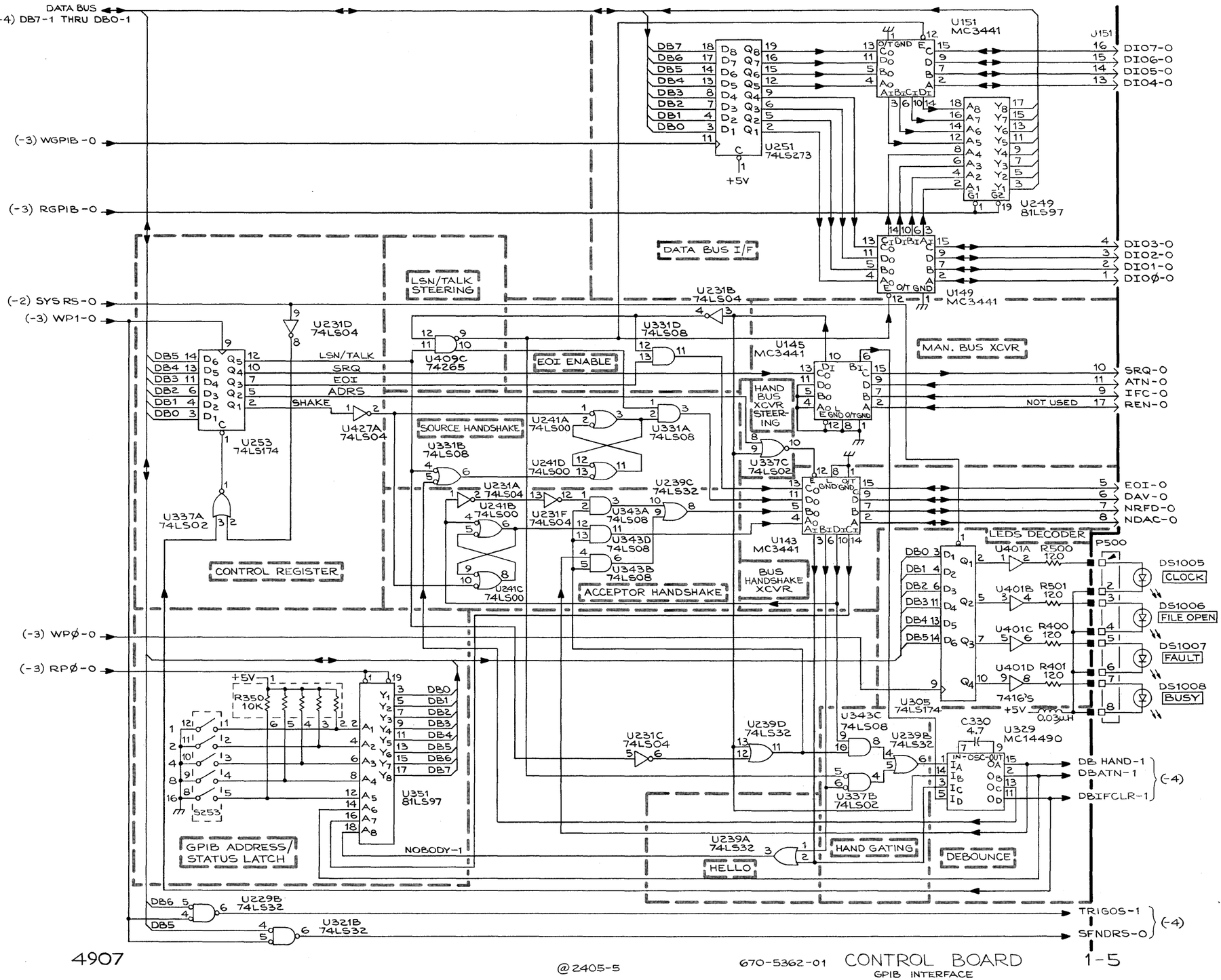
CONTROL BOARD
MICROPROCESSOR
(670-5362-01)
1-2



CONTROL BOARD
MEMORY
(670-5362-01)
1-3



CONTROL BOARD
DISC INTERFACE
(670-5362-01)
1-4


DATA BUS
(-2,-4) DB7-1 THRU DB0-1
(-3) WGPIB-0
(-3) RGPIB-0
(-2) SYS RS-0
(-3) WP1-0
(-3) WPØ-0
(-3) RPØ-0
U251 74LS273
+5V
U151 MC3441
U249 81LS97
U149 MC3441
DIO7-0
DIO6-0
DIO5-0
DIO4-0
DIO3-0
DIO2-0
DIO1-0
DIOØ-0
DATA BUS I/F
LSN/TALK STEERING
U231B 74LS04
U231D 74LS04
U253 74LS174
U337A 74LS02
CONTROL REGISTER
LSN/TALK
SRQ
EOI
ADRS
SHAKE
U427A 74LS04
U409C 74265
EOI ENABLE
U331D 74LS08
U145 MC3441
MAN. BUS XCVR
SRQ-0
ATN-0
IFC-0
NOT USED
REN-0
HAND BUS XCVR STEERING
U337C 74LS02
SOURCE HANDSHAKE
U241A 74LS00
U331A 74LS08
U331B 74LS08
U241D 74LS00
U239C 74LS32
U231A 74LS04
U241B 74LS00
U231F 74LS04
U343A 74LS08
U343D 74LS08
U343B 74LS08
U241C 74LS00
ACCEPTOR HANDSHAKE
U143 MC3441
BUS HANDSHAKE XCVR
EOI-0
DAV-0
NRFD-0
NDAC-0
LEDS DECODER
P500
DS1005 CLOCK
DS1006 FILE OPEN
DS1007 FAULT
DS1008 BUSY
U401A R500 120
U401B R501 120
U401C R400 120
U401D R401 120
7416's
+5V
0.03µH
U305 74LS174
C330 4.7
U329 MC14490
DB HAND-1
DBATN-1
DBIFCLR-1
(-4)
R350 10K
S253
U351 81LS97
GPIB ADDRESS/ STATUS LATCH
NOBODY-1
U231C 74LS04
U239D 74LS32
U343C 74LS08
U239B 74LS32
U337B 74LS02
U239A 74LS32
HELLO
HAND GATING
DEBOUNCE
U229B 74LS32
U321B 74LS32
TRIGOS-1
SFNDRS-0
(-4)

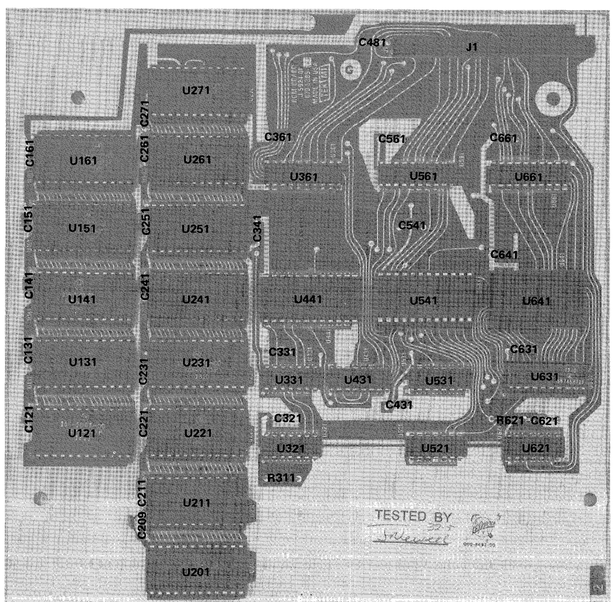
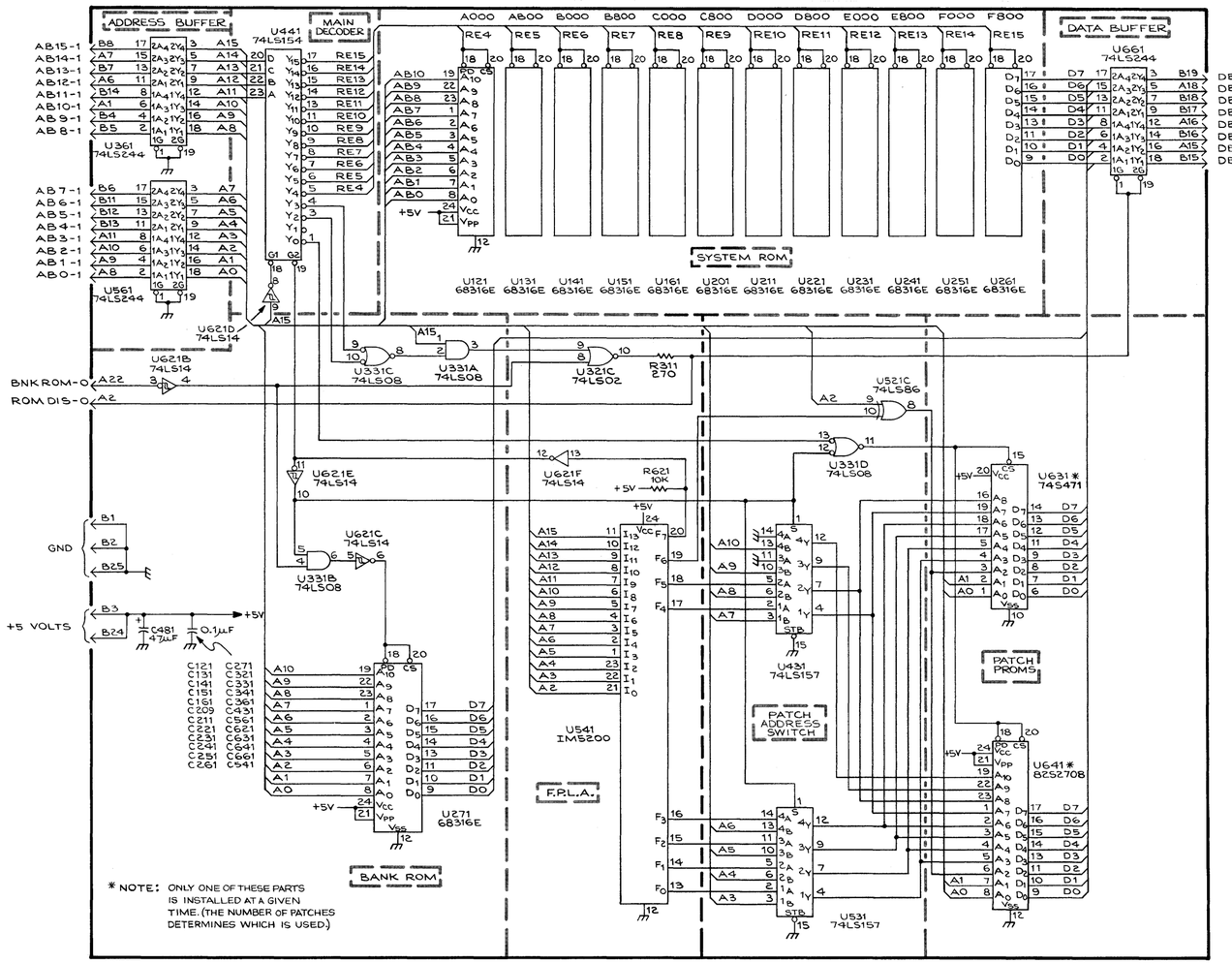
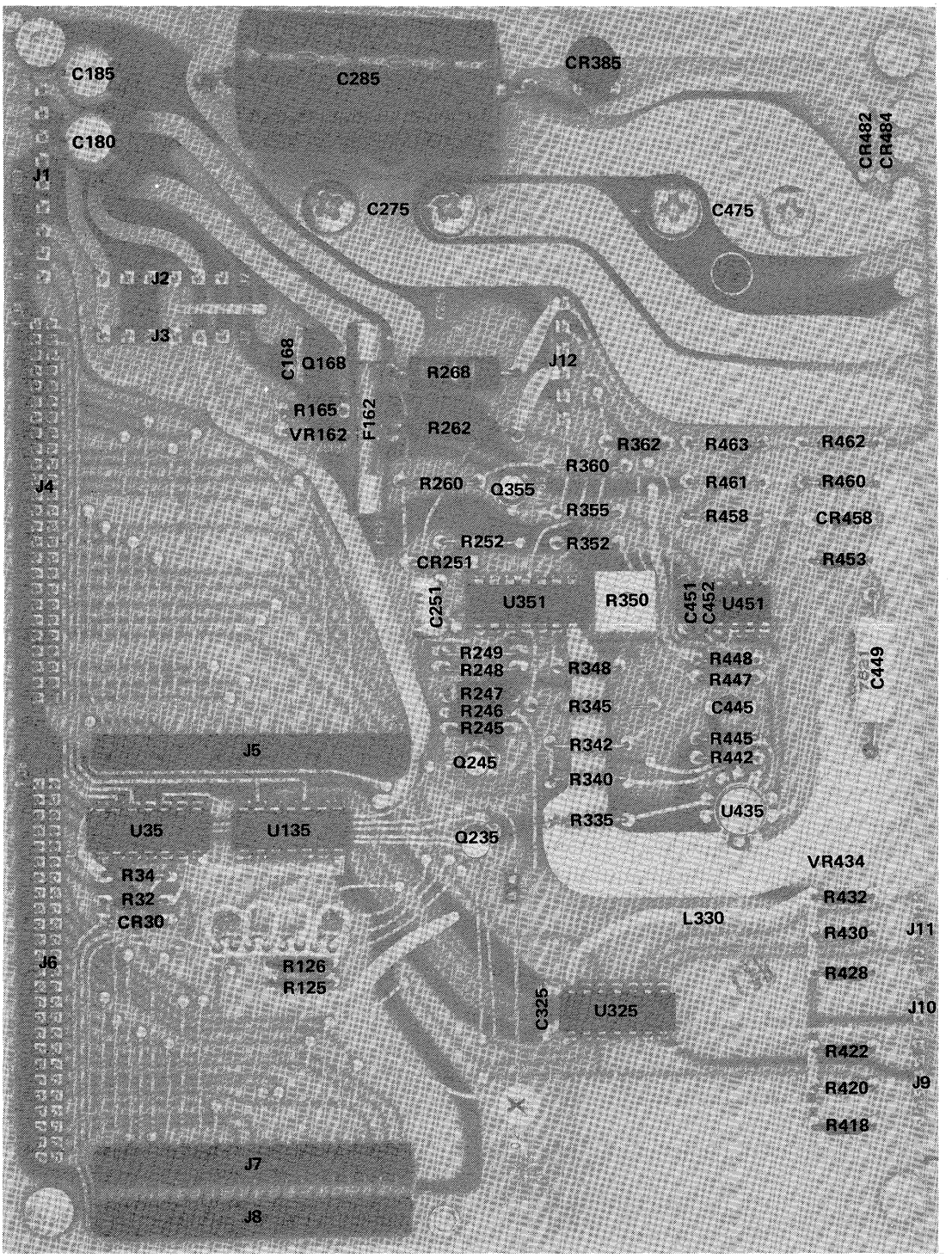


Figure 8-8. ROM Board Component Locations (670-5385-00).



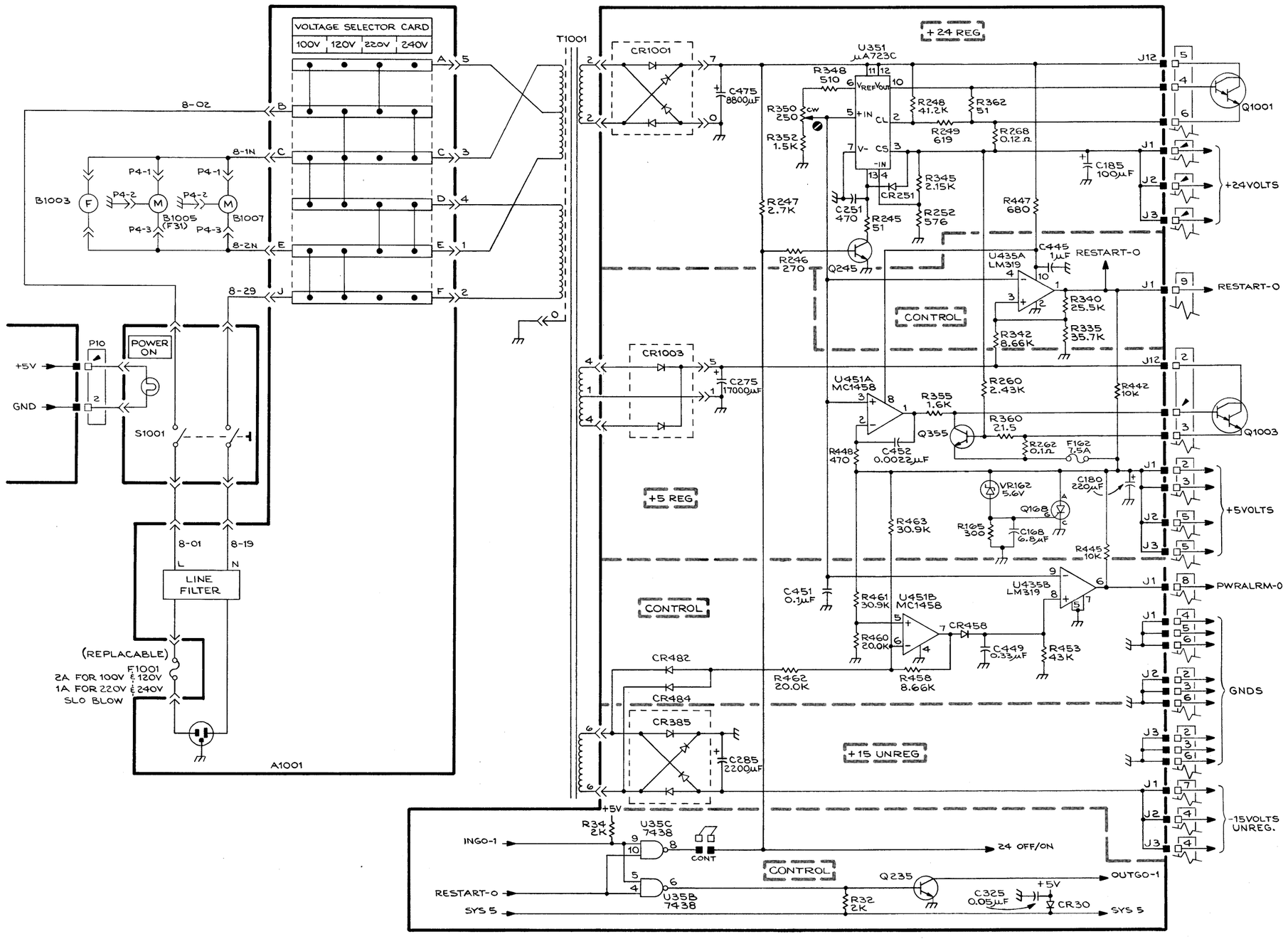
INDEX

POWER SUPPLY BOARD

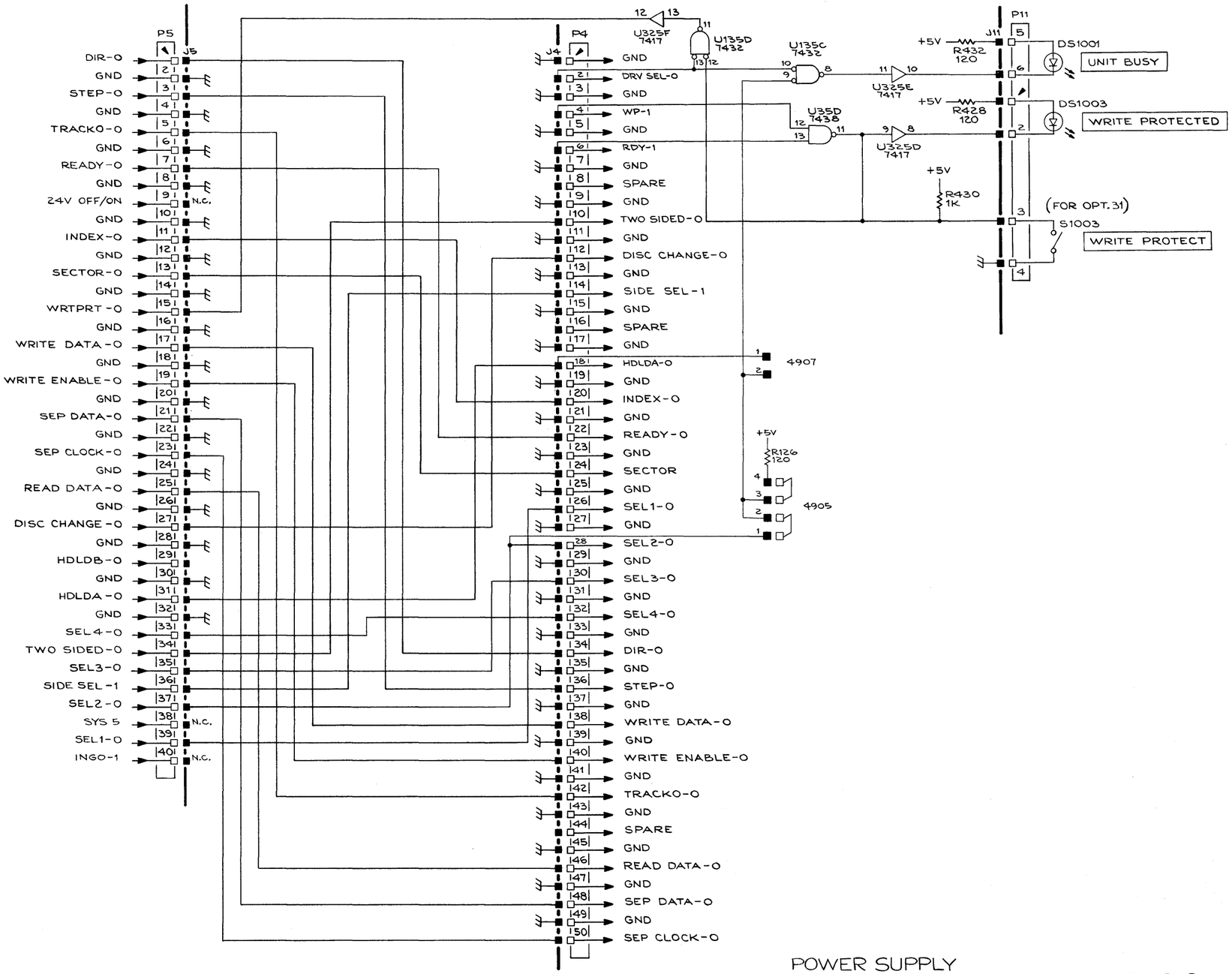


2405-79

Figure 8-9. Power Supply Board Component Locations.



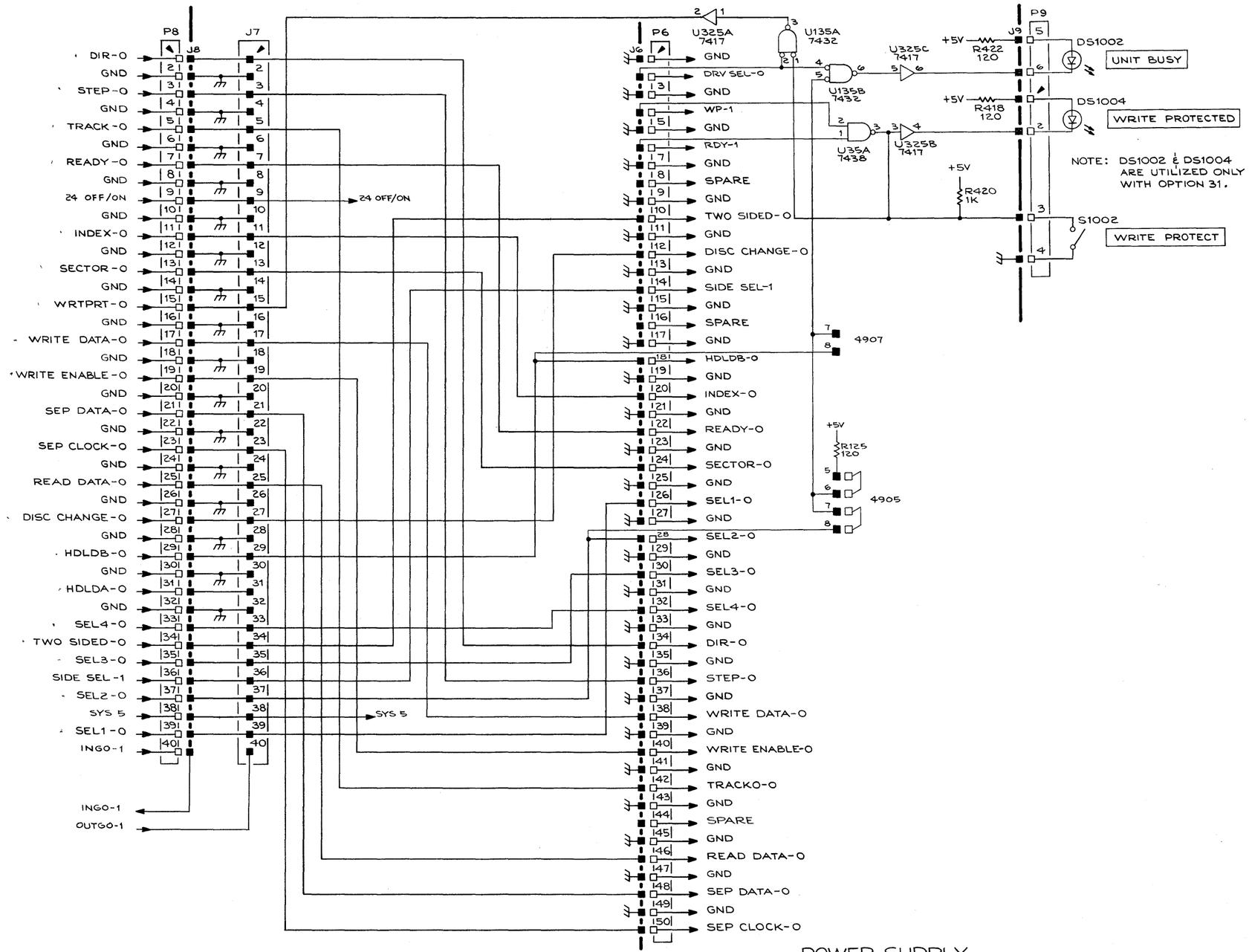
POWER SUPPLY BOARD
POWER SUPPLY
(670-5441-02)
3-1



POWER SUPPLY BOARD
RIGHT DISC DRIVE INTERCONNECT
(670-5441-02)
3-2

4907

670-5441-01 POWER SUPPLY RIGHT DISC DRIVE INTERCONNECT 3-2
(USED WITH F31 ONLY)



POWER SUPPLY BOARD
LEFT DISC DRIVE INTERCONNECT
(670-5441-02)
3-3

4907

@ 2405-9

670-5441-01

POWER SUPPLY
LEFT DISC DRIVE INTERCONNECT 3-3
(USED WITH 4907, F30, F31.)

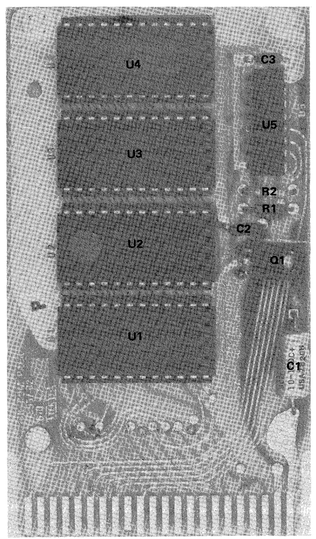
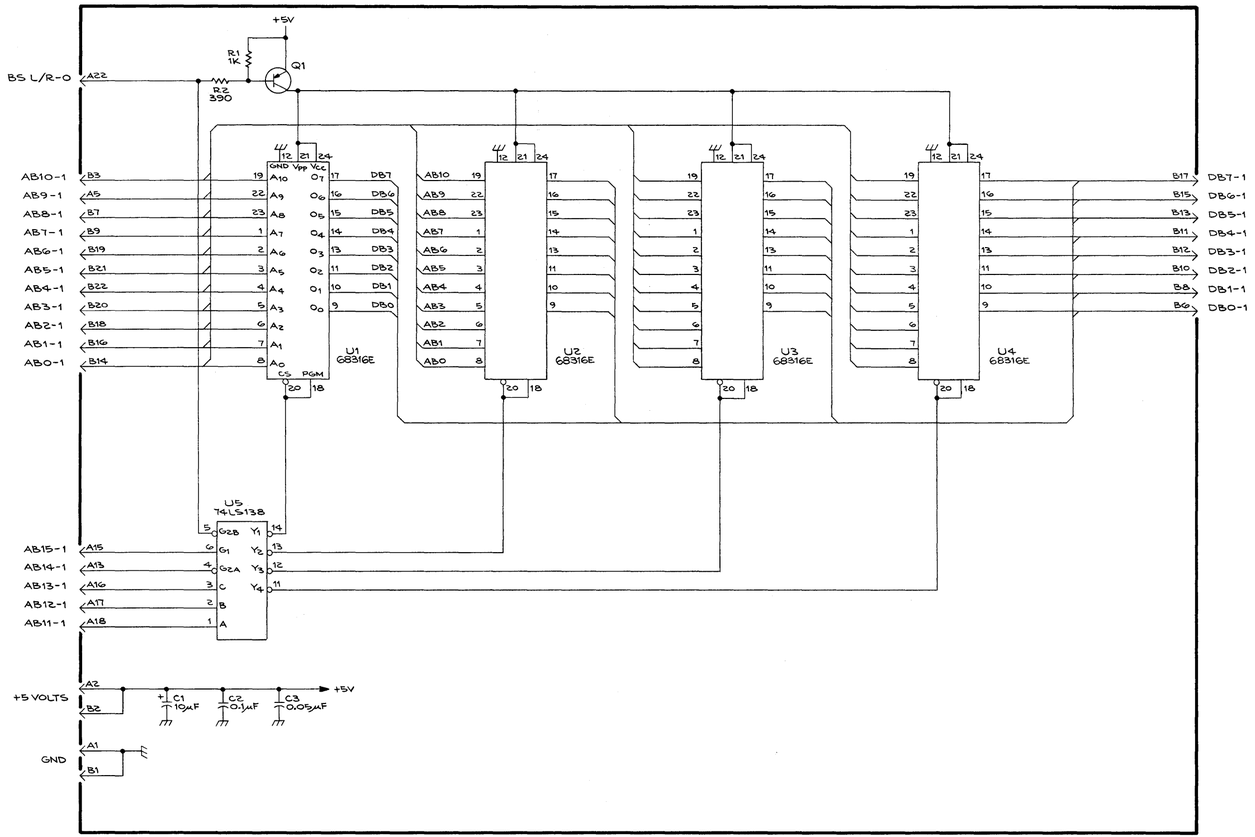


Figure 8-10. File Manager ROM Pack Component Locations.



020-0279-00
(FOR USE WITH 4906 & 4907)

@ 2405-10

670-6188-00 ROM PACK

Section 9
REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
\- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
\- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
\- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000DD	BIG CAMERA LITHO PREP.	2785 SW CEDAR HILLS BLVD.	BEAVERTON, OR 97005
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
06383	PANDUIT CORPORATION	17301 RIDGELAND	TINLEY PARK, IL 60477
08261	SPECTRA-STRIP CORP.	7100 LAMPSON AVE.	GARDEN GROVE, CA 92642
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
12624	NORTON CO., TAPE DIV., SEALANT OPERATION	12 BENNETT DRIVE	GRANVILLE, NY 12832
13511	AMPHENOL CARDRE DIV., BUNKER RAMO CORP.		LOS GATOS, CA 95030
21994	TEX WIRE CO.	P O BOX 278	HILLSDALE, NJ 07642
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
27264	MOLEX PRODUCTS CO.	5224 KATRINE AVE.	DOWNERS GROVE, IL 60515
52905	SIMPLEX MFG. COMPANY	5224 NE 42ND AVENUE	PORTLAND, OREGON 97218
55420	DYSAN CORPORATION	2388 WALSH AVENUE	SANTA CLARA, 95050
56481	SHUGART ASSOCIATES	415 OAKMEAD PKY	SUNNYVALE, CA 94086
59730	THOMAS AND BETTS COMPANY	36 BUTLER ST.	ELIZABETH, NJ 07207
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
77250	PHEOLL MANUFACTURING CO., DIVISION OF ALLIED PRODUCTS CORP.	5700 W. ROOSEVELT RD.	CHICAGO, IL 60650
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
82647	TEXAS INSTRUMENTS, INC., CONTROL PRODUCTS DIV.	34 FOREST ST.	ATTLEBORO, MA 02703
82877	ROTRON, INC.	7-9 HASBROUCK LANE	WOODSTOCK, NY 12498
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
86445	PENN FIBRE AND SPECIALTY CO., INC.	2032 E. WESTMORELAND ST.	PHILADELPHIA, PA 19134
86928	SEASTROM MFG. COMPANY, INC.	701 SONORA AVENUE	GLENDALE, CA 91201
91886	MALCO A MICRODOT CO.	12 PROGRESS DRIVE	MONTGOMERYVILLE, PA 18936
93907	CAMCAR SCREW AND MFG. CO.	600 18TH AVE.	ROCKFORD, IL 61101

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	390-0611-00			1		CAB.TOP,CONT:	80009	390-0611-00
						(ATTACHING PARTS)		
-2	212-0023-00			6		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-3	426-0928-02			4		FRAME,TRIM:GRAY PLASTIC	80009	426-0928-02
						(ATTACHING PARTS)		
-4	213-0088-00			4		SCR,TPG,THD CTG:4-24 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-5	334-2864-00			4		PLATE,IDENT:BLANK	80009	334-2864-00
-6	426-1477-00			2		FRAME SECT,CAB.:UPPER LEFT	80009	426-1477-00
						(ATTACHING PARTS)		
-7	210-0457-00			6		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-8	650-0085-00			1		DISC DRIVE ASSY:	80009	650-0085-00
	650-0085-00			1		DISC DRIVE ASSY:(OPT 30)	80009	650-0085-00
	650-0085-00			2		DISC DRIVE ASSY:(OPT 31)	80009	650-0085-00
						(ATTACHING PARTS)		
-9	212-0068-00			6		SCREW,MACHINE:8-32 X 0.312 INCH,TRH STL	77250	OBD
						- - - * - - -		
-10	426-1475-00			1		FR SECT,CONT:RIGHT	80009	426-1475-00
						(ATTACHING PARTS)		
-11	212-0507-00			6		SCREW,MACHINE:10-32 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-12	426-1476-00			1		FR SECT,CONT:LEFT	80009	426-1476-00
						(ATTACHING PARTS)		
-13	212-0507-00			6		SCREW,MACHINE:10-32 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-14	426-1479-00			2		FRAME SECT,CAB.:LOWER	80009	426-1479-00
						(ATTACHING PARTS)		
-15	210-0457-00			6		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-16	348-0128-00			4		BUMPER,PLASTIC:CABINET MTG,2.022 INCH LONG	80009	348-0128-00
						(ATTACHING PARTS)		
-17	212-0091-00			8		SCREW,MACHINE:8-32 X 0.625",FILH STL,CD PL	93907	OBD
						- - - * - - -		
-18	390-0610-00			1		CAB.BOT.CONT:	80009	390-0610-00
						(ATTACHING PARTS)		
-19	212-0023-00			2		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-20	334-3304-00			1		MKR SET,IDENT:MKD 4051 FILE MGR	80009	334-3304-00
-21	380-0384-01			1		HSG,HALF,RDOUT:	80009	380-0384-01
						(ATTACHING PARTS)		
-22	211-0102-00			4		SCREW,MACHINE:4-40 X 0.500",FLH,STL	83385	OBD
						- - - * - - -		
-23	----- -----			1		CKT BOARD ASSY:ROM PAK(SEE A2 EPL)		
-24	136-0578-00			4		. SOCKET,PLUG-IN:24 DIP,LOW PROFILE	01295	C952402
-25	380-0343-01			1		HSG,HALF,PTR:INNER PLASTIC	80009	380-0343-01
-26	367-0189-00			1		HANDLE,BOW:	80009	367-0189-00

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-1	----- -----			1		SWITCH,ROCKER:DPST(SEE S1001 EPL)		
	----- -----			1		SWITCH ROCKER:DPST(SEE S1001 EPL,OPT 30)		
	----- -----			1		SWITCH ROCKER:DPST(SEE S1001 EPL,OPT 31)		
-2	----- -----			4		LT EMITTING DIO.:(SEE DS1005,1006,1007,1008 EPL)		
-3	210-1281-00			4		WASHER,RECESSED:0.25 ID X 0.059 THK,PLSTC	80009	210-1281-00
-4	333-2394-00			1		PANEL,FRONT:CONTROLLER	80009	333-2394-00
	333-2393-00			1		PANEL,REAR:(OPT 30,31)	80009	333-2393-00
	333-2392-00			1		PANEL,FRONT:(OPT 31)	80009	333-2392-00
						(ATTACHING PARTS)		
-5	210-0457-00			4		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
	131-2270-00			2		CONTACT,ELEC:GROUNDING,CU-BE	80009	131-2270-00
	210-0949-00			2		WASHER,FLAT:0.141 ID X 0.50 INCH OD,BRS	12327	OBD
-6	426-1507-00			1		FRAME,SIDE:LEFT	80009	426-1507-00
						(ATTACHING PARTS)		
-7	211-0534-00			3		SCR,ASSEM,WSHR:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-8	426-1508-00			1		FRAME,SIDE:RIGHT	80009	426-1508-00
						(ATTACHING PARTS)		
-9	211-0534-00			3		SCR,ASSEM,WSHR:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-10	175-5087-00			1		CA ASSY,SP,ELEC:50,28 AWG,6.0L	80009	175-5087-00
-11	----- -----			1		CKT BOARD ASSY:ROM BOARD(SEE A3 EPL)		
						(ATTACHING PARTS)		
-12	211-0144-00			4		SCREW,MACHINE:4-40 X 1.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-13	131-1857-00			2		. TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
-14	136-0578-00			15		. SOCKET,PLUG-IN:24 DIP,LOW PROFILE	01295	C952402
-15	136-0634-00			1		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	C952002
-16	----- -----			1		CKT BOARD ASSY:CONTROL(SEE A1 EPL)		
						(ATTACHING PARTS)		
-17	211-0008-00			4		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
-18	211-0507-00			4		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-19	124-0301-00			3		. TERMINAL STRIP,:CKT BD MT,6 TAB,BRASS	80009	124-0301-00
-20	124-0302-00			4		. TERMINAL STRIP,:CKT BD MT,14 TAB,BRASS	80009	124-0302-00
-21	131-0589-00			9		. TERM,PIN:0.46 L X 0.025 SQ.PH BRZ GL	22526	47350
-22	131-0608-00			54		. TERMINAL,PIN:0.365 L X 0.25 PH,BRZ,GOLD PL	22526	47357
-23	131-0993-00			2		. LINK,TERM.CONNE:2 WIRE BLACK	00779	530153-2
-24	131-1857-00			2		. TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
-25	136-0260-02			19		. SOCKET,PLUG-IN:16 CONTACT,LOW CLEARANCE	82647	C9316-18
-26	136-0578-00			1		. SOCKET,PLUG-IN:24 DIP,LOW PROFILE	01295	C952402
-27	136-0623-00			1		. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	C954002
-28	253-0135-00			1		. PLASTIC STRIP:PRESS,SENS,ADH CTD BS	12624	V592-1/2
	276-0543-00			1		. SHLD BEAD,ELEK:FERRITE	80009	276-0543-00
	210-0201-00			1		. TERMINAL,LUG:SE #4	86928	A373-157-2
-29	----- -----			1		. MICROCIRCUIT,LI:(SEE U549 EPL)		
						(ATTACHING PARTS)		
-30	211-0008-00			1		. SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
-31	210-0586-00			1		. NUT,PLAIN,EXT W:4-40 X 0.25 INCH,STL	78189	211-041800-00
						- - - * - - -		
-32	386-3370-01			1		. PLATE,CONN MTG:REAR,W/HARDWARE	80009	386-3370-01
-33	----- -----			1		CKT BOARD ASSY:POWER SUPPLY(SEE A4 EPL)		
	----- -----			2		CKT BOARD ASSY:POWER SUPPLY(SEE A4 EPL,OPT 31)		
						(ATTACHING PARTS)		
-34	211-0504-00			4		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
-35	212-0518-00			4		SCREW,MACHINE:10-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-36	131-0589-00			29		. CONTACT,ELEC:0.46 INCH LONG	22526	47350
-37	131-0608-00			126		. TERMINAL,PIN:0.365 L X 0.25 PH,BRZ,GOLD PL	22526	47357
-38	131-1857-00			6		. TERM SET,PIN:36/0.025 SQ. PIN	22526	65500-136
-39	131-0993-02			1		. LINK,TERM.CONNE:2 WIRE RED	00779	1-530153-0
-40	131-1777-00			1		. LINK,TERM.CONNE:WHITE,3,26 AWG,600V	80009	131-1777-00

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-41	344-0159-00	B010100	B010114	2		. CLIP,ELECTRICAL:	80009	344-0159-00
	344-0154-00	B010115		2		. CLIP,ELECTRICAL:FOR 0.25 INCH DIA FUSE	80009	344-0154-00
-42	348-0064-00			5		GROMMET,PLASTIC:GRAY,ROUND,0.582 ID	80009	348-0064-00
-43	129-0149-00			4		POST,ELEC-MECH:6-32 X 0.25 X 3.406"LONG	80009	129-0149-00
-44	210-0457-00			1		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
-45	210-0202-00			1		TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
-46	120-1168-00			1		XFMR,PWR,STPDN:	80009	120-1168-00
						(ATTACHING PARTS)		
-47	212-0522-00			4		SCREW,MACHINE:10-32 X 2.50",HEX HD STL	83385	OBD
-48	210-0812-00			4		WASHER,NONMETAL:#10,FIBER	86445	OBD
-49	166-0457-00			4		INSUL SLVG,ELEC:0.19 ID X 1.875"LONG MYLAR	80009	166-0457-00
-50	220-0410-00			4		NUT,EXTENDED WA:10-32 X 0.375 INCH,STL	83385	OBD
						- - - * - - -		
-51	407-2133-00			2		BRACKET,SUPPORT:ALUMINUM	80009	407-2133-00
-52	----- -----			1		SEMICOND DVC,DI:RECT.(SEE CR1001 EPL)		
						(ATTACHING PARTS)		
-53	211-0511-00			1		SCREW,MACHINE:6-32 X 0.50 INCH,PNH STL	83385	OBD
						- - - * - - -		
-54	----- -----			1		SEMICOND DVC,DI:RECT.(SEE CR1003 EPL)		
						(ATTACHING PARTS)		
-55	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-56	----- -----			1		CAP.,FXD,ELCTLT:8800UF(SEE C475 EPL)		
						(ATTACHING PARTS)		
-57	211-0511-00			2		SCREW,MACHINE:6-32 X 0.50 INCH,PNH STL	83385	OBD
	210-0457-00			2		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
-58	432-0114-00			1		BASE,CAPACITOR:1.75 INCH DIA,PLASTIC	80009	432-0114-00
						- - - * - - -		
-59	----- -----			1		CAP.,FXD,ELCTLT:1700UF,(SEE C275 EPL)		
						(ATTACHING PARTS)		
-60	211-0511-00			2		SCREW,MACHINE:6-32 X 0.50 INCH,PNH STL	83385	OBD
-61	210-0457-00			2		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
-62	432-0114-00			1		BASE,CAPACITOR:1.75 INCH DIA,PLASTIC	80009	432-0114-00
						- - - * - - -		
-63	129-0685-00			6		SPACER,POST:0.61 L W/4-40 THRU THD	80009	129-0685-00
						(ATTACHING PARTS)		
-64	211-0008-00			6		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-65	343-0758-00			1		CLAMP,DISC DR:STEEL	80009	343-0758-00
						(ATTACHING PARTS)		
-66	210-0457-00			2		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-67	210-0457-00			1		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
	211-0504-00			1		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
-68	210-0202-00			2		TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
-69	346-0154-00			2		STRAP,TIEDOWN:6.125 L,PLASTIC	06383	PLP1.51-M
-70	386-3878-00			1		SUPPORT,CKT CD:	80009	386-3878-00
						(ATTACHING PARTS)		
-71	211-0008-00			4		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-72	129-0686-00			2		SPACER,POST:0.486 L W/4-40 THRU THD	80009	129-0686-00
						(ATTACHING PARTS)		
-73	211-0198-00			2		SCREW,MACHINE:4-40 X 0.438 PNH,STL,POZ	77250	OBD
						- - - * - - -		
-74	----- -----			1		LT EMITTING DIO:RED(SEE DS1003 EPL)		
	----- -----			1		LT EMITTING DIO:RED,655NM,50MA(OPT 30)		
	----- -----			2		LT EMITTING DIO:RED,655NM,50MA(OPT 31)		
	210-1281-00			1		WASHER,RECESSED:0.25 ID X 0.059 THK,PLSTC	80009	210-1281-00
-75	----- -----			1		LT EMITTING DIO:RED,660NM,100MA (SEE DS1001 EPL)		
	----- -----			1		LT EMITTING DIO:RED,660NM,100MA MAX(OPT 30)		
	----- -----			2		LT EMITTING DIO:RED,660NM,100MA MAX(OPT 31)		
-76	----- -----			1		SWITCH,TOGGLE:SPDT,0.4A,W/IND BEZ(SEE S1002 EPL)		
	----- -----			1		SWITCH,TOGGLE:SPDT,0.4A,W/IND BEZEL(OPT 30)		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-	----- -----			2		SWITCH,TOGGLE:SPDT,0.4A,W/IND BEZEL(OPT 31)		
-77	441-1414-01			1		CHAS,CONTROLLER:W/FRAME	80009	441-1414-01
-78	119-0492-00			1		FAN,AXIAL:MUFFIN TYPE,3 INCH DIA,115V	82877	SU2C5
						(ATTACHING PARTS)		
-79	210-0407-00			4		NUT,PLAIN,HEX.:6-32 X 0.25 INCH,BRS	73743	3038-0228-402
-80	210-0006-00			4		WASHER,LOCK:INTL,0.146 IDX 0.288 OD,STL	78189	1206-00-00-0541C
						- - - * - - -		
	131-2270-00			1		CONTACT,ELEC:GROUNDING,CU-BE	80009	131-2270-00
-81	378-0091-00			1		SCREEN,FAN:	80009	378-0091-00
-82	----- -----			1		SELECTOR,VOLTS:W/LINE FLTR(SEE A1001 EPL)		
-83	386-3872-00			1		PLATE,COVER:	80009	386-3872-00
						(ATTACHING PARTS)		
-84	211-0097-00			2		SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-85	----- -----			2		TRANSISTOR:NPN,SI(SEE Q1001 Q1003 EPL)		
						(ATTACHING PARTS)		
-86	210-0406-00			2		NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
-87	210-1171-00			2		WSHR,SHOULDERED:0.116 ID X 0.138 INCH OD	52905	A7148516P2
						- - - * - - -		
-88	342-0328-00			2		INSULATOR,PLATE:XSTR,ALUMINA	80009	342-0328-00
-89	333-2393-00			1		PANEL,REAR:	80009	333-2393-00
						(ATTACHING PARTS)		
-90	210-0457-00			4		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-91	386-3873-00			1		PLATE,COVER:(OPT 30;31)	80009	386-3873-00
						(ATTACHING PARTS)		
-92	211-0507-00			4		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
	198-3813-00			1		WIRE SET,ELEC:	80009	198-3813-00
-93	175-0859-00			AR		. WIRE,ELECTRICAL:6 WIRE RIBBON	08261	SS-0622-1910610C
-94	175-1577-00			AR		. CABLE,SP,ELEC:4,18 AWG,TWISTED	80009	175-1577-00
-95	175-0829-00			AR		. WIRE,ELECTRICAL:6 WIRE RIBBON	08261	SS-0626-710610C
-96	175-0831-00			AR		. WIRE,ELECTRICAL:8 WIRE RIBBON	08261	OBD
-97	175-0856-00			AR		. WIRE,ELECTRICAL:9 WIRE RIBBON	08261	SS-0922-1910610C
-98	352-0169-09			1		. CONN BODY,PL,EL:2 WIRE WHITE	80009	352-0169-09
-99	352-0164-09			1		. CONN BODY,PL,EL:6 WIRE WHITE	80009	352-0164-09
-100	352-0166-00			1		. HLDR,TERM CONN:8 WIRE,BLACK	80009	352-0166-00
	352-0169-00			1		. HLDR,TERM CONN:2 WIRE,BLACK	80009	352-0169-00
-101	352-0198-05			1		. CONN BODY,PL,EL:2 WIRE GREEN	80009	352-0198-05
-102	352-0202-01			1		. CONN BODY,PL,EL:6 WIRE BROWN	80009	352-0202-01
	352-0202-03			1		. CONN BODY,PL,EL:6 WIRE ORANGE	80009	352-0202-03
-103	352-0205-00			4		. CONN BODY,PL,EL:9 WIRE BLACK	80009	352-0205-00
	352-0205-01			2		. CONN BODY,PL,EL:9 WIRE BROWN	80009	352-0205-01
-104	204-0678-00			2		. CONN BODY,PL,EL:FOR 3 FEMALE CONTACTS	27264	10-17-2032
-105	131-1815-00			6		. CONTACT,ELEC:22-30 AWG,FEMALE,BRASS	27264	08-56-0110
-106	131-2065-00			2		. TERM,QIK DISC:18-22 AWG,BRASS TIN PLATED	00779	2-350799-2
	198-3897-00			1		WIRE SET,ELEC:	80009	198-3897-00
-107	131-2009-00			2		. TERM,QIK DISC:FEMALE ACCOM 0.187 X 0.02	00779	60291-1
-108	131-1981-00			2		. TERM,QIK DISC:16-20 AWG,BRASS	91886	122-0202-019
-109	131-0621-00			12		. CONTACT,ELEC:0.577"L,22-26 AWG WIRE	22526	75694-006
-110	131-0707-00			10		. CONNECTOR,TERM.:0.48" L,22-26AWG WIRE	22526	75691-005
	131-1159-00			4		. CONTACT,ELEC:QUICK-DISCONNECT,W/INSUL	00779	60041-2
-111	131-0677-00			2		. CONNECTOR,TERM:18 AWG	91886	122-0192-019
	131-1620-00			3		. CONTACT,ELEC:CONN,FEMALE,MATE-N-LOCK	00779	60619-1
-112	204-0609-00			1		. CONN BODY RCPT:3 FEMALE CONTACTS	00779	1-480303-0
	343-0549-00			6		. STRAP,TIEDOWN:0.091 W X 3.62 INCH LONG	59730	TY23M
	198-3814-00			1		WIRE SET,ELEC:	80009	198-3814-00
	131-0621-00			18		. CONTACT,ELEC:0.577"L,22-26 AWG WIRE	22526	75694-006
	131-0707-00			24		. CONNECTOR,TERM.:0.48" L,22-26AWG WIRE	22526	75691-005
-113	131-1620-00			12		. CONTACT,ELEC:CONN,FEMALE,MATE-N-LOCK	00779	60619-1
-114	343-0549-00			5		. STRAP,TIEDOWN:0.091 W X 3.62 INCH LONG	59730	TY23M
-115	204-0802-00			1		. CONN BODY,ELEC:MATE-N-LOCK	00779	1-480270-0

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-117	175-2147-00			1		CA ASSY,SP,ELEC:50,28 AWG,7.25 L	80009	175-2147-00
-118	175-2121-00			1		CA ASSY,SP,ELEC:40,28 AWG,11.0 L	80009	175-2121-00
						(ATTACHING PARTS)		
-119	211-0061-00			2		SCREW,MACHINE:4-40 X 0.500 INCH,FIL STL	83385	OBD
-120	210-0586-00			2		NUT,PLAIN,EXT W:4-40 X 0.25 INCH,STL	78189	211-041800-00
						- - - * - - -		
	175-2122-00			1		CA ASSY,SP,ELEC:40.28 AWG,21.0 L(OPT 30;31)	80009	175-2122-00
-121	343-0725-00			1		CLAMP,CABLE:2.75 L,ALUMINUM(OPT 30)	80009	343-0725-00
	343-0725-00			2		CLAMP,CABLE:2.75 L,ALUMINUM(OPT 31)	80009	343-0725-00
						(ATTACHING PARTS)		
-122	211-0513-00			4		SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	OBD
						- - - * - - -		
-123	175-2148-00			1		CA ASSY,SP,ELEC:50,28 AWG,13.0 L	80009	175-2148-00
	334-1378-00			1		PLATE,IDENT:MKD SERIAL NO.	80009	334-1378-00
	334-2148-00			1		MARKER,IDENT:MARKED SERIAL NO.	80009	334-2148-00
	334-3388-00			1		MARKER,IDENT:MKD TEK BEAVERTON OR(OPT 30;31)		

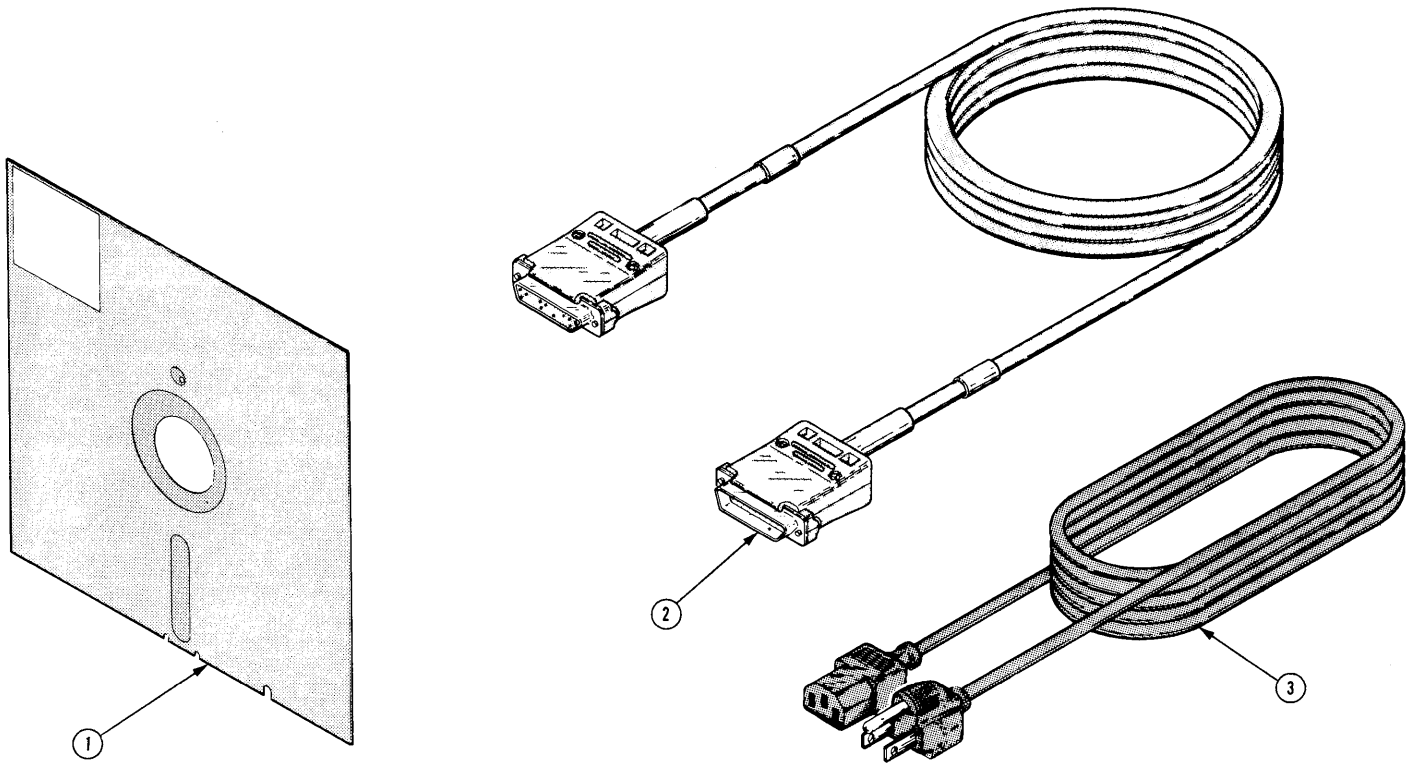
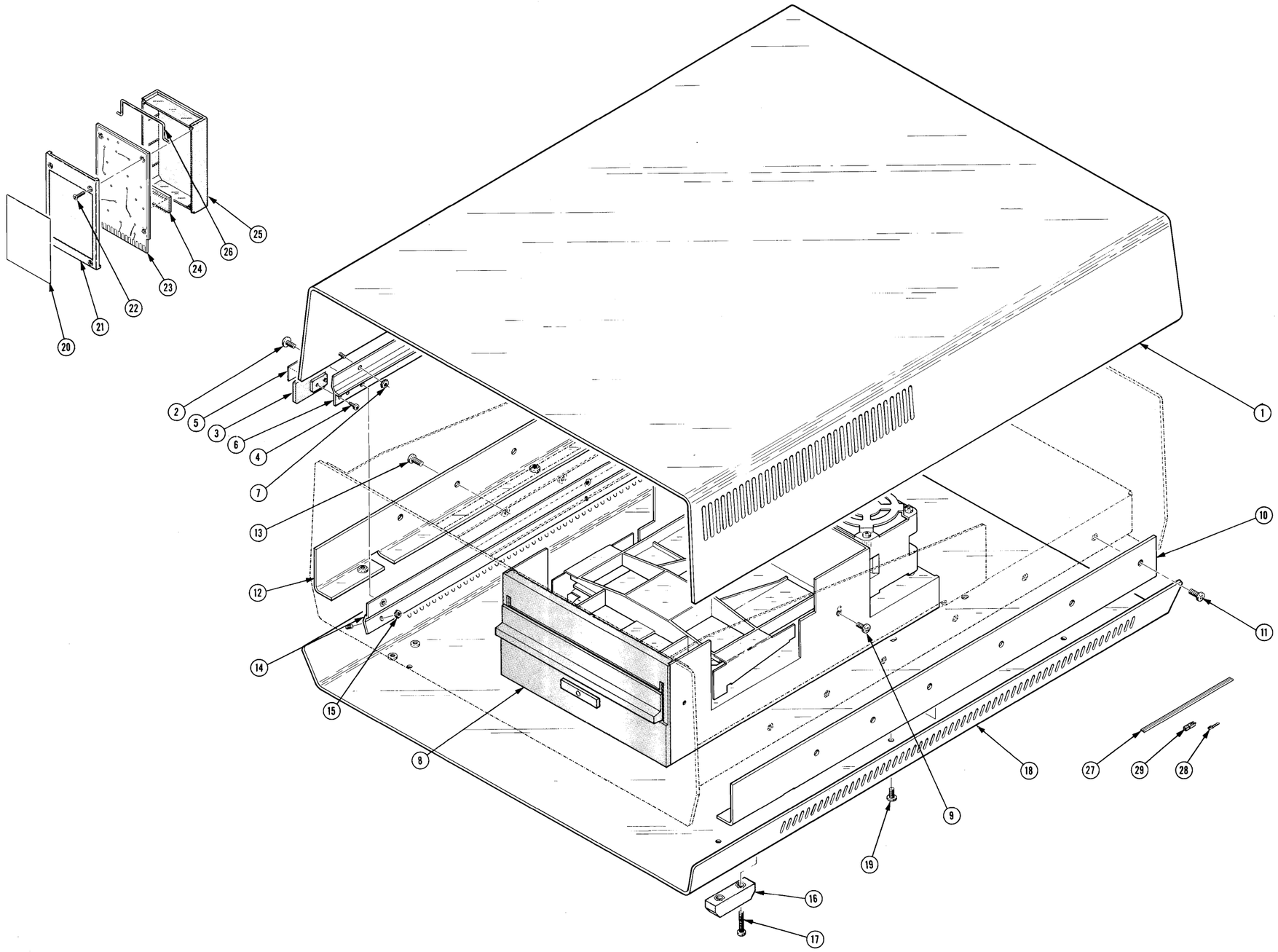


Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty 1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
					STANDARD ACCESSORIES		
3-1	062-3492-02			1	SOFTWARE PKG:	80009	062-3492-02
-2	012-0630-03			1	CABLE,INTCON:2 METER L	13511	AC30147-102
-3	161-0066-00			1	CABLE ASSY,PWR,:3 WIRE,98 INCH LONG	80009	161-0066-00
	006-2398-00			1	PAD,CLEANER:MAG TAPE HEAD & DISC	21994	TX-801-B
	020-0279-00			1	ACCESSORY PKG:ROM PACK	80009	020-0279-00
	016-0367-00			1	BDR,LOOSE-LEAF:2.0 CAP RING,VINYL COVER	80009	016-0367-00
	334-3430-00			1	MARKER,IDENT:	80009	334-3430-00
	334-3340-00			1	MKR SET,IDENT:MARKED 0 THRU 9	000DD	OBD
	070-2380-00			1	MANUAL,TECH:OPERATORS	80009	070-2380-00
	070-2381-00			1	CARD,INFO:REFERENCE,4907	80009	070-2381-00
	070-2493-00			1	MANUAL,TECH:INSTALLATION GUIDE	80009	070-2493-00
					OPTIONAL ACCESSORIES		
	012-0630-04			1	CABLE,INTCON:4 METERS L	13511	AC30147-104
	119-0896-00			1	ALIGNMENT DISK:DYSAN 240	55420	240S 800570
	119-1011-01			1	FLEXIBLE DISC:PACKAGE OF 10	56481	SA103
	070-2381-00			1	CARD,INFO:REFERENCE,4907	80009	070-2381-00
	070-2405-00			1	MANUAL,TECH:SERVICE,4907	80009	070-2405-00
	070-2494-00			1	MANUAL,TECH:GPIB SUPPORT APPLICATIONS	80009	070-2494-00
	070-2504-00			1	MANUAL,TECH:SERVICE,119-0977-00	80009	070-2504-00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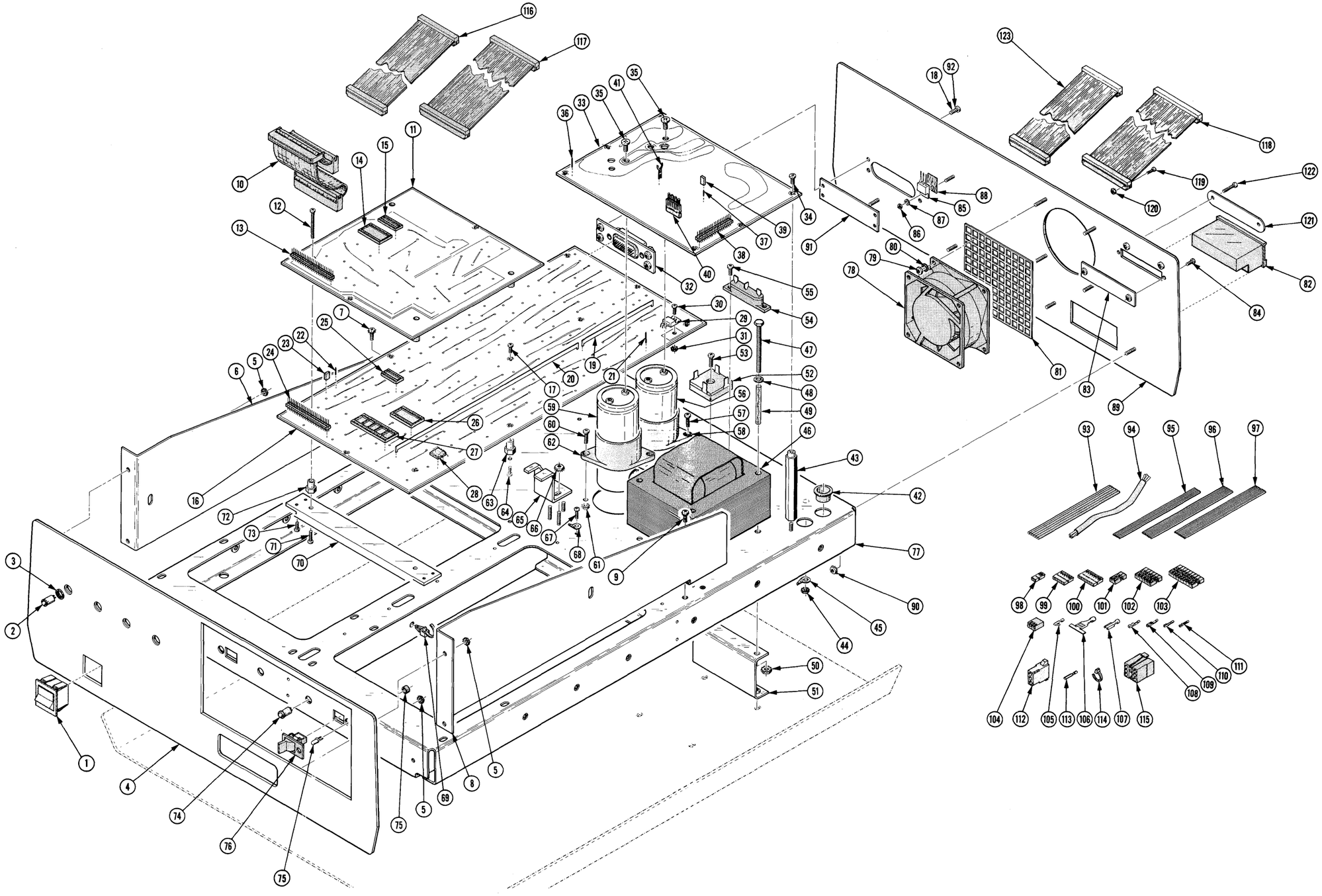


Appendix A

SIGNAL NAMES

SIGNAL	SOURCE/ DESTINATION(S)	DESCRIPTION
24 OFF/ON	3-1 Main/ 3-1 Aux. Supply	+24V supply control.
ABO(-15)-1	1-2/1-3,4	MPU's 16 line address bus.
ABA-1	1-2	Address Bus Available
AT41-0	1-1/1-4	Enables write-precompensation when disc is Above Track 41.
ATN-1	1-5	GPIB Attention bus management line.
BNKROM-0	1-3/2-1	Enables Bank (Disc) ROM on ROM Board.
CAS-0	1-1/1-3	RAM Column Address Strobe (Selector).
CNT-0	1-1/1-3	RAM Refresh Counter Clock.
DATA-0	1-1/1-3	Write peripheral timing/enable for data transfer.
DATAMUX-1	1-1/1-4	Phase-locked loop's input data multiplexer control.
DAV-0	1-5	Data on the GPIB is Valid.
DBO(-7)-1	1-2/1-3,4,5	MPU's 8 line Data Bus.
DBATN-1	1-3/1-5	Debounced GPIB Attention line.
DBE-1	1-2	MPU's Data Bus Enable line.

DBHAND-1	1-3/1-5	Debounced GPIB Handshake line.
DBIFCLR-1	1-3/1-5	Debounced GPIB Interface Clear line.
DIO 0(-7)-0	1-5	GPIB Data In/Out (8 line bus).
DIR-0	1-4	Selects Direction (in/out) of R/W Head move for selected disc drive unit.
DISC CHANGE-0	1-4	Tells MPU a disc media was changed (removed from its drive unit).
EOI-0	1-5	GPIB End or Identify control line.
HALT-0	1-2	MPU's Halt line; only used with System Test Fixture.
HDLD A-0	1-4	Disc's R/W Head Load.
HDLDB-0	1-4	Not used.
IFC-0	1-5	GPIB Interface Clear control line.
INDEX-0/INDEX-1	1-4/1-3	Used with Sector pulses to locate R/W head on proper disc sector.
INGO-1	3-1	Used in Option 30/31 Systems, OUTGO from main power supply controls power in Auxiliary supplies as INGO.
INTMSK-1	1-4/1-3	Mask for the MPU's IRQ Interrupt.
IRQ-0	1-3/1-2	Maskable Interrupt Request line to the MPU.

NDAC-1	1-5	GPIB's Not Data Accepted control line.
NRFD-1	1-5	GPIB's Not Ready for Data control line.
OS RESET-0	1-3/1-4	10msec One-Shot Reset.
OUTGO-1	3-1	See INGO (Power Supply control signals).
PIAE-1	1-2	This PIA Enable is used only with the System Test Fixture.
PWRALRM-0	3-1/1-2,4	This Power Alarm senses impending power loss and prevents starting a disc write operation.
RAMEN-1	1-1/1-3	This line Enables the RAMs' data out buffers.
RAMW-0	1-2/1-3	This places the RAMs in the Write mode.
RAWDATA-0	1-4/1-4	Raw Data from the disc.
RAWDATA-1	1-4/1-1	Inverted (buffered) Raw disc data.
RDATA-1	1-1/1-4	Read Data from disc after clock pulses are removed from Raw Data.
READY-0	1-4	Indicates a Ready response from the selected disc drive unit.
REN-1	1-5	GPIB Remote Enable (not used).
RESTART-0	3-1/1-2	Power control signal Re-starts the MPU.

RFEN-0	1-1/1-3	RAM Refresh Enable/Timing line.
RFRAS-0	1-1/1-3	RAM Refresh Row Address Strobe.
RGPIB-0	1-3/1-5	Enables GPIB data buffer to Read data from the bus.
ROMDIS-0	2-1	System Test Fixture Disables ROM Board ROMs.
ROWEN-1	1-1/1=3	Enables (switches) the Row/Column RAM Address Multiplexor.
RP0-0	1-3/1-5	Sent by the Address Decoder to enable certain Read Peripherals.
RP1-0	1-3/1-4	Similar to RP0.
RWOC-1	1-3/1-3,4	MPU Read/Write Open Collector control line.
SECTOR-0	1-4	A disc drive unit sends this pulse to the disc interface indicating the beginning of a Sector.
SEL0-0	1-4	Sent by the disc interface to select device 0 (one of four possible disc drive units).
SEL1-0	1-4	Selects device 1.
SEL2-0	1-4	Selects device 2.
SEL3-0	1-4	Selects device 3.
SFNDRS-0	1-4/1-5	The Sector Found flip-flop is reset by this line.
SIDE SEL-0	1-4	Not used.

SPIAS-1	1-3	Not used.
SRQ-1	1-5	A GPIB Service Request control bus line.
SSDA-0	1-3/1-4	The decoder enables the SSDA circuit with this line.
STEP-0	1-4	Sent with DIR to the selected disc drive unit to step the R/W head one track (in or out).
SYS 5	3-1	This is a partially sustained +5 volt system supply, only used during power loss.
SYSRS-0	1-2/1-4,5	This line clears the System buffers at power up (a buffered version of the Restart line).
TCLK-0/RCLK-1	1-1/1-4	This 500 KHz transmit/receive clock line is used to time the data decoders and encoders.
TCLK-1/RCLK-0	1-1/1-4	The compliment of TCLK-0/RCLK.
TDATA-1	1-1/1-4	Transmit Data is encoded into WRITE DATA-0 which is then sent to the disc.
TIME-1	1-2/1-3	This is the 1 Hz Real Time Clock signal.
TOUT-0	1-4/1-3	The 10 msec One-Shot has timed out.

TRACK0-0	1-4	Disc reports its R/W head is at Track 0.
TRIGOS-1	1-5/1-4	The MPU triggers the 10 msec One-Shot via this line.
TWO SIDED-0	1-4/1-3	Not used.
VMA-0	1-2	Valid Memory Address is sent by the MPU when an address is placed on the bus.
WGPIB-0	1-3/1-5	The Peripheral Decoder sends this Write enable to the GPIB data buffer.
WP0(-3)-0	1-3/1-3,4,5	These lines are sent by the Address Decoder to enable the various Write Peripherals.
WRITE ENABLE-0	1-4	This line enables the selected disc drive unit to write on its disc.
WRITE DATA-0	1-1	This line carries the encoded write data stream to the disc drive unit.
WRTPRT-0	1-4	A disc drive unit reports a write protected condition to the disc interface.
ZYNCO-1	1-4/1-1	This line enables a decoder circuit which synchronizes on a zero data stream in the sector preamble.

Appendix B

ERROR MESSAGES AND RECOVERY PROCEDURES

(*Asterisks indicate that additional information will be displayed, further defining the error.)

Error Message	Cause	Correction
ERROR 1 BUS I/O ERROR*	GPIB data transfer error often caused by static electricity.	Execute an INIT then reissue command. If this is not successful, restarting program may be necessary.
ERROR 2 ILLEGAL COMMAND	4907 or 4051 error If 4051 and ROM Pack is not being used, be sure the "read byte" or "write byte" format is legal (correct).*	This message may also appear during a WRITE command if a device I/O error has occurred. If so, be sure the 4907 has been loaded and is operating correctly. If error message repeats, check for the following problems:

***The 4907 system is designed to handle commands without a ROM Pack by using "read byte" (RBYTE) and "write byte" (WBYTE) commands to the 405X. See FDCAL Program (Appendix E) lines: 5, 38, 130, 620.**

Error Message	Cause	Correction
		1) bad ROM Pack, 2) bad GPIB Cable, 3) 4907 ROMs, 4) or other 405X or 4907 hardware problems.
ERROR 3 COMMAND FORMAT	4907 or 405X error. This message indicates the command is legal but syntax or format is wrong.	See Error 2 correction (problem is with ROM Pack or "read byte"/"write byte" syntax error).
ERROR 4 ILLEGAL COMMAND FIELDS	One or more entries in the CALL "FORMAT" or CALL "FFRMT" commands are illegal: volume number entry is not 1, number of volumes entry is not 1, number of directory chains is 0 or greater than 10.	Execute command again with correct entries.

Error Message	Cause	Correction
ERROR 5 ILLEGAL MASTER PASS-WORD	An attempt has been made to execute a command containing an illegal entry in the master password field.	Master password field can contain no more than 10 characters. The first character must be alpha and the rest alphanumeric. No spaces may be entered between characters.
ERROR 7 ILLEGAL FILE IDENTI-FIER	An F.I. has incorrect construction or illegal characters.	See FILE IDENTIFIER CONSTRUCTION in Section 4, 4907 Operator's Manual.
ERROR 8 ILLEGAL VOLUME IDEN-TIFIER	The volume I.D. field in a formatting command has illegal characters, incorrectly located spaces, or is blank.	The volume I.D. field can contain no more than 10 characters. The first character must be alpha. No spaces may be entered between characters. The field cannot be blank.

Error Message	Cause	Correction
ERROR 10 DEVICE NOT FOUND	The system cannot find the device with the address specified in the command.	Re-execute command with correct address. If this message appears the first time the system is used, the adjustable strapping in the controller may have been positioned incorrectly. See Section 4, Device (Drive) Address Selection.
ERROR 11 DEVICE WRITE PROTECTED	An attempt was made to write to a disc that is write-protected.	Be sure the device should be written to, and then turn off the write protect switch for the device. Be sure the write-protect tape is covering the write-protect hole on the disc.

Error Message	Cause	Correction
ERROR 12 DEVICE RESERVED	The device was reserved and a command requiring a free device was attempted.	Release the device with a CALL "DREL" command and continue.
ERROR 13 DEVICE NOT RESERVED	The device was not reserved and a command requiring a reserved device was attempted.	Execute a CALL "DRES" command and continue.
ERROR 14 DEVICE HAS FILES OPEN	A CALL "DRES" command was issued to a device with open files.	Close all files on that device and continue.
ERROR 15 DEVICE I/O ERROR	A hard error has occurred on a device. Data was read back incorrectly (CRC error).	See CALL "HERRS" command description in Section 5. If a particular location on a disc is causing repeated errors, it may be taken out of use with a CALL "MRKBBG" command.

DEVICE I/O ERROR (15) SUBMESSAGES

NUMBER/NAME	CAUSE/REMEDY
02 NO TRACK ZERO DETECTED**	Solve problem in track detector or circuitry to MPU.
04 VOLUME ADDRESS OUT OF RANGE ERROR***	Can happen when creating file on write protected disc/CALL DISMOUNT, then CALL MOUNT. May also indicate firmware problem/check ROM Board ROMs.
08 INDEX PULSE TIME-OUT ERROR**	Index pulse got lost between drive unit and the MPU/check this hardware path.
10 "FIND SECTOR" TIME-OUT ERROR**	The format comparitor is not receiving sector pulses to compare with counter bytes/Check sector and index pulse receiver and circuits to sector counter.
20 SEEK INCOMPLETE ERROR**	This message relates to format, and could be caused by a sticking head, head seeking to wrong track, etc.
40 CRC OR HEADER PARITY ERROR***	R/W head is not reading at proper amplitude; or related read hardware problem/check disc alignment, etc.
80 VOLUME ADDRESS DOESN'T AGREE	Look for problem in the Address Comparator or Sector Pulse Counter/Comparator circuits. This message would also be sent if another disc in the system were sending sector pulses at the same time as the addressed disc.

****These messages indicate strictly hardware problems.**
*****These messages may be caused by bad media; also, they are not related to positional operations on the disc.**

Error Message	Cause	Correction
ERROR 16 DEVICE NOT READY*	This message appears if: 1. The disc is not in place. 2. The disc has been loaded improperly. 3. The door has not been closed. 4. The device is not up to speed.	Make sure address is correct, that the disc is properly loaded, and that the device is up to speed.
ERROR 17 DEVICE NOT MOUNTED*	An attempt was made to use an unmounted disc.	Execute a CALL "MOUNT" command and continue
ERROR 18 NO SPACE*	There is not enough space left on the disc for further storage.	Delete any unneeded files (KILL), gather the remaining free space in a single area and with the CALL "COMPRS" command 1I/O command may then be reissued.

Error Message	Cause	Correction
ERROR 20 CONTROL UNIT ERROR TABLE SPACE EX- HAUSTED	A command requiring space equivalent to two files was attempted with either 8 or 9 files already open. This eliminates room necessary for execution of the command.	Close two files and reissue the command.
ERROR 22 CONTROL UNIT PROCES- SOR ERROR RAM FAILED	This message is prompted by a parity error, which generally means the system has detected a RAM failure.	Do RAM Tests found in Section 5.
ERROR 23 CLOCK NOT READY	The system is not operating.	Execute a CALL "SETTIM" command
ERROR 32 DIRECTORY CHAIN DAM- AGE*	This may occur when attempting a CALL "MOUNT" command.	Execute CALL "DUP". Then reattempt CALL "MOUNT" on new disc. Information may be unrecoverable on a disc generating this massage.

Error Message	Cause	Correction
ERROR 34 DATA AREA DAMAGE*	This results from damaged or bad blocks on a disc.	Copy the file to another disc or to another area on the same disc. Then: 1. Kill old file. 2. Reserve device (CALL "DRES"). 3. Execute CALL "MRKBBG". 4. Release device (CALL "DREL").
ERROR 35 BLOCK USAGE CONFLICT	The system has incorrectly assigned a physical block to two of these three categories: 1. Directory use. 2. Data use. 3. Bad block group. Since no block can be assigned to more than one use at a time or overlap an adjacent block, this error message appears.	Execute a CALL "DUP" command.

Error Message	Cause	Correction
ERROR 40 LOGICAL FILE NUMBER NOT FOUND*	A command execution has been attempted specifying a logical file number that does not exist. This occurs when the lfn in a command does not match the lfn specified in an earilier OPEN command.	Execute an OPEN command with the correct lfn.
ERROR 41 ACTIVE LOGICAL FILE NUMBER*	An OPEN or OPEN "G" command specifying an illegal lfn has been issued. This lfn has already been assigned to a file which is currently active.	Execute another OPEN command with an unused lfn, or close old file.
ERROR 42 FILE NOT FOUND*	The device involved does not contain a file with the specified name.	Be sure the device address and the F.I. are correct and reissue the command.

Error Message	Cause	Correction
ERROR 43 DUPLICATE FILE IDEN- TIFIER*	An attempt was made to create a new file with an F.I. belonging to an existing file.	Use a different F.I. in the CREATE command.
ERROR 44 LIBRARY NAME CON- FLICT	A file cannot be created at any level where there is already a library of the same name.	Change the name of the file and reissue the CREATE command.
ERROR 45 FILE LOCKED*	An attempt was made to open a file without using the passwords specified in the CREATE command.	Reissue the OPEN command using the correct passwords.
ERROR 50 FILE IS WRITE PRO- TECTED*	An attempt was made to WRITE to a file opened for read access only.	If you do wish to write to the file, close it and then reopen it for "full" access.
ERROR 51 FILE IS RESERVED*	A GPIB OPEN command was issued without setting the "wait if file reserved" bit.	This message only appears when commands not involving the ROM pack have been issued.

Error Message	Cause	Correction
ERROR 52 ILLEGAL FILE OPERATION*	An attempt was made to perform an illegal file operation.	Review commands involved in carrying out the operation to be sure they are valid for the file or information being accessed.
ERROR 53 END OF FILE*	An attempt has been made to read past the end of a file.	This message does not appear if an ON EOF command is used.
ERROR 54 ILLEGAL FILE EXPANSION*	An attempt has been made to write additional data to a noncontiguous location on the disc for a file specified "contiguous."	The attribute C (contiguous) may be changed to S (scattered) using the ASSIGN command.
ERROR 55 NO SPACE*	There is not enough uncommitted space left on the disc for further storage.	Delete any unneeded files (KILL), and gather the remaining free space in a single area with the CALL "COMPRS" command. I/O command may then be reissued.

Error Message	Cause	Correction
ERROR 56 POINTER NOT AT ITEM BOUNDARY*	This message results from improper system operation, and relates to item file firmware routines.	Check for bad ROMs (see Section 5).
ERROR 57 ILLEGAL ITEM HEADER*	The TYPE function has encountered an illegal item header for a standard item file.	See TYP command description in Section 5.
ERROR 60 FORMAT FAILED*	If the CALL "FORMAT" command was issued, it has failed because the disc has too many bad blocks or the first block containing the volume label is bad. If the CALL "FFRMT" command was issued, it may have failed because the old volume label was illegible due to damage.	If message appears after attempting a complete, accurate "full" format, choose another disc.

Error Message	Cause	Correction
ERROR 61 MARK BAD BLOCK GROUP FAILED*	The CALL "MRKBBG" command failed because the bad block table in the volume label is too full or hardware errors are involved.	It is most likely that the particular disc's memory volume is bad. Simply copy files to a new disc media.
ERROR 62 ILLEGAL ATTRIBUTE CHANGE*	The ASSIGN command contains attribute entries which conflict with the existing file type.	Reissue the ASSIGN command with correct attribute entries.
ERROR 63 ILLEGAL IPL FILE*	The file name extension is not valid or the file is not a host binary type.	Reissue the command with the correct extension construction.
ERROR 70 COPY SKIPS LOCKED FILE*	A COPY . . . TO command without correct passwords was issued to a locked file.	Reissue the COPY . . . TO command using the correct passwords. If the F.I. uses special characters to copy multiple files, copying will continue with the next file.

Error Message	Cause	Correction
ERROR 71 COPY SKIPS OPEN FILE*	A COPY . . . TO command was attempted on an open file.	If you wish to copy this file to an- other loca- tion, it must first be closed. If the F.I. in the command uses special characters to copy multiple files, copy- ing will con- tinue with the next file.
ERROR 74 DELETE SKIPS LOCKED FILE*	A KILL com- mand was is- sued to a locked file.	Reissue the KILL command. If you wish to delete files with passwords, those pass- words must be entered in the F.I. or the master password must be used. If the specific passwords or the master pasword is not used, the locked files cannot be deleted.

Error Message	Cause	Correction
ERROR 75 DELETE SKIPS OPEN FILE*	A KILL command was attempted on an open file.	If you do intend to delete this file, close it and then reissue the KILL command.
ERROR 78 RENAME SKIPS LOCKED FILE*	A CALL "RENAME" command without correct passwords was attempted on a locked file.	Reissue the CALL "RENAME" command with the correct passwords.

Appendix C

DATA STRUCTURES

This appendix is a group of definitions for the various tables and subroutines that the 4907 uses.

The following is a list of the data types used to describe the data structures.

Data Type	Use and/or Meaning
BIN	Binary Data, usually unsigned integers.
CHAR	ASCII character data.
DATA	User Data that the 4907 need not examine.
MASK	A mask for extracting bits of data from a byte.
FLAG	Single bit flags.
CODE	Encoded types or descriptor identifications.
VAL	A constant value.

STANDARD ITEM FORMATS

This is a description of the standard item formats used by the 4907. The 405X uses only part of these items; namely:

Byte	for inputs only
Short Integer	for inputs only
Long Floating Point	
ASCII String	
End of Record	
Null (Long and Short)	

All items begin with a one byte identifier. The rest of the information is described in the following formats.

Data Type	Field Size	Meaning of Data
BIN	1	The item header
Byte Item:		
CODE	X'01'	Byte item code
DATA	1	One byte of data
Pointer Item:		
CODE	X'02'	Pointer item code
DATA	3	24 bit pointer
Short Integer Item:		
CODE	X'03'	Short integer item code
DATA	2	16 bit signed integer
Long Integer Item:		
CODE	X'04'	Long integer item code
DATA	4	32 bit signed integer
Short Floating Point Item:		
CODE	X'05'	Short floating point item code
DATA	4	32 bit floating point number
Long Floating Point Item:		
CODE	X'06'	Long floating point item code
DATA	8	64 bit long floating point number
ASCII String Item:		
CODE	X'07'	ASCII string item code
BIN	3	Number of bytes of data
DATA	X	ASCII data
Tek Code String Item:		
CODE	X'08'	Tek code string item code
BIN	3	Number of bytes of data
DATA	X	Tek code data

Data Type	Field Size	Meaning of Data
Byte String Item:		
CODE	X'09'	Byte string item code
BIN	3	Number of bytes of data
DATA	X	Byte data
End of Record Item:		
CODE	X'14'	End of record item code
End of File Item:		
CODE	X'15'	End of file item code
Short Null Items:		
CODE	X'10'	Short null item (1 byte) code
CODE	X'11'	Short null item (2 byte) code
DATA	1	Undefined
CODE	X'12'	Short null item (3 byte) code
DATA	2	Undefined
Long Null Item:		
CODE	X'13'	Long null item code
BIN	3	Number of trash bytes
DATA	X	Undefined
Array Item:		
CODE	X'1E'	Array item code
BIN	3	Number of bytes of data
BIN	4	Rest of item header
DATA	X	Dimension information and data
Template Item:		
CODE	X'1F'	Template item code
BIN	3	Number of bytes of data
BIN	1	Rest of the header information
DATA	X	Template definition data

Data Type	Field Size	Meaning of Data
Structure Item:		
CODE	X'80' To X'FE'	Structure item codes
BIN	3	Number of bytes of data
DATA	X	Data

STATUS MESSAGES

The following two message formats are used by the control unit to return status information to the host system. The device status message contains information about a physical I/O device. The file status message describes one file.

Device Status Message:

Data Type	Field Size	Meaning of Data
BIN	1	Device address
CHAR	12	Device identification (part number)
BIN	4	Size (space on an empty volume)
BIN	4	Used space on this volume
CHAR	10	Volume identification
CHAR	24	Owner identification
BIN	2	Block length
BIN	4	Time/date the volume was formatted
BIN	2	Number of files open
BIN	1	Flag byte
FLAG	X'80'	Device is reserved
FLAG	X'40'	Write protected
VAL	64	Message size

SPECIAL DATA FIELD

Attribute Byte:

The following is a description of the attribute byte that appears in the several messages, commands and in the system directories.

Data Type	Field Size	Meaning of Data
MASK	X'F0'	File type
CODE	X'00'	Not active (deleted entry)
CODE	X'10'	Library entry
CODE	X'20'	ASCII file
CODE	X'30'	(Host) Binary file
CODE	X'40'	Item file
FLAG	X'08'	Public access (is allowed)
FLAG	X'04'	Contiguous allocation (is requested)
FLAG	X'02'	Delete null items (when copying file)

File Status Message:

BIN	1	Attribute byte
BIN	4	Time/date file was created
BIN	4	Time/data last used
BIN	4	Time/date last altered
BIN	4	File size (allocated in bytes)
BIN	4	End of file point (in bytes)
BIN	3	Logical record length
BIN	1	Reserved status
CODE	X'00'	Not reserved
CODE	X'01'	Write reserved
CODE	X'02'	Full reserved
BIN	1	Number of users that have the file open
CHAR	X	File name
VAL	26+Name	Message size

I/O COMMANDS

The following is a list of the command formats. All of the I/O commands are proceeded by a command code byte. This byte is not listed in the command formats since it is repeated for all commands.

Data Type	Field Size	Meaning of Data
Command Header:		
BIN	1	Command code
Control Unit Status:		
CODE	X'20'	Control unit status code
Device Status:		
CODE	X'21'	Device status code
BIN	1	Device address
Named File Status:		
CODE	X'22'	Named file status code
BIN	1	Device address
CHAR	X	File name
Read Error Message:		
CODE	X'23'	Read error message code
Read Error Status:		
CODE	X'24'	Read Error Status Code
BIN	1	Device address
(Return Message Format:)		
BIN	2	Retries in last I/O operation
BIN	2	Soft errors on the device
BIN	2	Hard errors on the device
BIN	2	Soft errors on the drive
BIN	2	Hard errors on the drive

Data Type	Field Size	Meaning of Data
Set Time/Date:		
CODE	X'25'	Set time/date code
BIN	4	Time/date
Read Time/Date:		
CODE	X'26'	Read time/date code
(Return Mesage Format:)		
BIN	4	Time/date
BIN	1	State of the clock
CODE	X'00'	Okay (clock is set and running)
CODE	X'01'	Stopped
Device Format:		
If this information is changed, BLDVL will have to be recoded.		
CODE	X'40'	Device format code
BIN	1	Device address
CHAR	10	Volume identification
CHAR	24	Owner identification
BIN	1	Volume number
BIN	1	Number of volumes
BIN	1	Number of directory chains at the first level
BIN	1	Level 2
BIN	1	Level 3
BIN	1	Level 4
BIN	1	Level 5
CHAR	10	Master password

Data Type	Field Size	Meaning of Data
Device Fast Format:		
CODE	X'41'	Device fast (quick) format code
		The rest of the message is identical to the format command
Device Compress:		
CODE	X'42'	Device compress code
BIN	1	Device address
BIN	1	Flags
Flag	X'80'	Delete unused space in files
Device Duplicate:		
CODE	X'43'	Device duplicate code
BIN	1	Sending device address
BIN	1	Receiving device address
BIN	1	Flags
Flag	X'80'	Delete unused space in files
Device Reserve:		
CODE	X'44'	Device reserve code
BIN	1	Device address
Device Release:		
CODE	X'45'	Device release code
BIN	1	Device address
Control Unit Disconnect:		
CODE	X'46'	Control unit disconnect code
Device Disconnect:		
CODE	X'47'	Device disconnect code
BIN	1	Device address

Data Type	Field Size	Meaning of Data
Initial Program Load:		
CODE	X'48'	Initial program load code
BIN	1	Device address
CHAR	4	File name extension
Mark Bad Block Group:		
CODE	X'49'	Mark bad block group code
BIN	1	Device address
CHAR	10	Volume identification
CHAR	10	Master password
CHAR	8	Bad block group control data
VAL	30	Command data size
Directory:		
CODE	X'4A'	Directory code
BIN	1	Device address
CHAR	X	File name
Mount:		
CODE	X'4B'	Mount code
BIN	1	Device address
Dismount:		
CODE	X'4C'	Dismount code
BIN	1	Device address
Current Operation Abort		
CODE	X'4D'	Current operation abort code This command is signaled with the IFC line on the GPIB.
Attribute:		
CODE	X'60'	Attribute code
BIN	1	Logical unit
BIN	1	New attribute byte

Data Type	Field Size	Meaning of Data
Delete:		
CODE	X'61'	Delete code
BIN	1	Device address
CHAR	10	Master password
CHAR	X	File name
Open File Status:		
CODE	X'62'	Open file status
BIN	1	Logical unit
Open:		
CODE	X'63'	Open code
BIN	1	Device address
BIN	1	Logical unit
BIN	1	Flag byte
FLAG	X'80'	Wait state error requested
FLAG	X'40'	Write protect file
BIN	1	Attribute byte
BIN	4	File size (bytes)
BIN	3	Logical record length
CHAR	X	File name
Close:		
CODE	X'64'	Close code
BIN	1	Logical unit
BIN	4	Data location
BIN	1	Flag byte
FLAG	X'80'	Return unused space
FLAG	X'40'	Current logical pointer is new EOF

Data Type	Field Size	Meaning of Data
Block Open:		
CODE	X'65'	Block open code
BIN		Device address
BIN	1	Logical unit number
BIN	1	Flags
FLAG	X'80'	Wait state is not allowed
FLAG	X'40'	Write protect file
CHAR	X	File name
Next File:		
CODE	X'66'	Next file code
BIN	1	Logical unit number
Copy:		
CODE	X'67'	Copy code
BIN	1	Sending device address
BIN	1	Receiving device address
BIN	1	Flags
FLAG	X'80'	Squeeze (delete extra space)
CHAR	X	Old file name
CHAR	X	New file name
Rename:		
CODE	X'68'	Rename code
BIN	1	Device address
CHAR	X	New file name
CHAR	X	Old file name
File Reserve:		
CODE	X'69'	File reserve code
BIN	1	Logical unit
BIN	1	Write reserve if not zero

Data Type	Field Size	Meaning of Data
File Release:		
CODE	X'6A'	File release code
BIN	1	Logical unit
Space:		
CODE	X' 6B'	Space code
BIN	1	Logical unit
BIN	4	New size
Return message format.		
BIN	4	Space required (bytes)
BIN	4	Space allocated (bytes)
Read:		
CODE	X'80'	Read code
BIN	1	Logical unit
BIN	4	Data location
Free Read:		
CODE	X'81'	Free read code
BIN	1	Logical unit
BIN	4	Data location
Write:		
CODE	X'82'	Write code
BIN	1	Logical unit
BIN	4	Data location
		The command header and the data must be separated with an EOI.
X	X	Users data

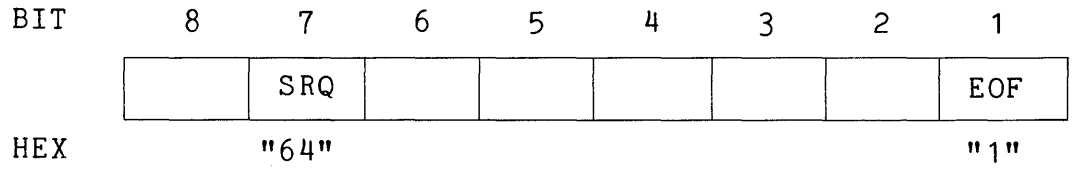
Data Type	Field Size	Meaning of Data
Type:		
CODE'84'	Type code	
BIN	1	Logical unit
BIN	4	Data location
Request Location:		
CODE	X'85'	Request location code
BIN	1	Logical unit
Return Message:		
BIN	4	Current location
Relocate Pointer:		
CODE	X'86'	Relocate pointer code
BIN	1	Logical unit
BIN	4	Data location
Diagnostic Seek:		
CODE	X'E1' To X'FF'	Extended device command codes
BIN	1	Device address
	0	Data for extended commands, may be 0 or greater

Appendix D

REFERENCE TABLES

SERIAL POLL STATUS BYTE

The status byte which is sent in response to a serial poll has the form:



BIT	NAME	FUNCTION
1	EOF	End of File has occurred.
2		Unassigned, will not be used.
3		-
4		-
5		-
6		-
7	SRQ	4907 is requesting service.
8		Unassigned, will not be used.

GPIB FUNCTION SUBSETS

The following list of "interface function subsets" are supported by the 4907. Refer to IEEE Standard 488-1975 for definitions of these subsets.

Interface Function	Subset Code
Source Handshake	SH1
Acceptor Handshake	AH1
Talker	T2
Listener	L4
Service request	SR1
Remote Local	RL0
Parallel Poll	PP0
Device Clear	DC0
Device Trigger	DT0
Controller	C0

APPENDIX D

HARDWARE ADDRESS TABLE

This table shows which circuits are enabled by the 40XX addresses and corresponding peripheral decoder lines. Any 400X address accesses a write-only circuit, while a 401X address accesses a read-only (or SSDA) circuit. The column labeled FLAG BYTE tells which data bits are set in the following flag byte scheme.

80	40	20	10	8	4	2	1

MSB LSB

Hex Address	Decoder Lines	Flag Byte	Circuit Addressed	Logic State
4000	WP-0		Indicator lights	
		8	BUSY	1-on
		4	FAULT	1-on
		2	FILE OPEN	1-on
		1	CLOCK	1-on
4002	WP1		GPIB and Disc control.	
		80	CRC reset	0-reset
		40	10 msec One-shot trigger	0-fire One-shot
		20	Reset Sector found	0-reset
		10	Talk/listen mode select	0-listen/ 1-talk
		8	Send SRQ	1-asserted
		4	Send EOI	1-asserted
		2	Enable Talk/Listen	1-enabled
		1	Handshake software pulse to assert DAV or DAC.	
4004	WP2		Disc control and Interrupt masks.	
		80	Mask for disc read/writes.	9-mask on
		40	(not used)	
		20	Write pre-compensation flag.	0-WPC on
		10	Step direction.	1-in/0-out
		8	Software pulse to step carriage.	

Hex Address	Decoder Lines	Flag Byte	Circuit Addressed	Logic State
		4	Head load trigger software pulse to load 1/2 sec.	
	WP2/WP3	11	Unit Select 3.	
		10	Unit Select 2.	
		01	Unit Select 1.	
		00	Unit Select 0.	
4006	WP3		Disc Control (write only).	
		80	Unit Select enable.	0-no unit selected
		40	Write enable.	1-write on
		20	Read Data Mux control.	0-normal/ 1-raw data
		10	Sector address select 4.	
		8	Sector address select 3.	
		4	Sector address select 2.	
		2	Sector address select 1.	
		1	Sector address select 0.	
4008	FLRESET		Interrupt flag reset (write only).	0-clear
400A			More data byte counters.	
400C	WGPIG		GPIB talk data.	
400E	OSRESET		Clears One-shot	
4010	SSDA		SSDA registers (A side)	
4012	RGP113		GPIB list to data.	
4014	RP0		GPIB status register.	
		80	Bus handshake lines valid.	1-valid
		40	EOI present.	1-asserted
		20	Attention.	1-asserted
4016	RP1		Disc status.	
		80	Power alarm.	1-alarm
		40	Disc removed.	1-removed
		20	Head loaded.	1-loaded

Hex Address	Decoder Lines	Flag Byte	Circuit Addressed	Logic State
		10	Write protect.	1-protected
		8	Track 00.	1-at 00
		4	Disc ready.	1-ready
		2	CRCC error.	1-error
		1	Sector selected by sector address is present.	1-present
4018	STAT EN		Interrupt flags (read only).	
		80	1 sec clock interrupt.	0-int. occurred
		40	Disc index pulse interrupt.	0-int. occurred
		20	Interface clear on GPIB.	0-int. occurred
		10	GPIB handshake ready to process.	0-int. occurred
		8	Attention released	0-int. occurred
		4	RAM parity error.	0-int. occurred
		2	Disc type.	0-int. occurred
		1	10 msec. One-shot time-out.	0-int. occurred

ASCII CODE CHART

B7 B6 B5 / BITS B4 B3 B2 B1	Ø Ø Ø	Ø Ø 1	Ø 1 Ø	Ø 1 1	1 Ø Ø	1 Ø 1	1 1 Ø	1 1 1
	COMMAND		DEFOCUSED		FOCUSED		INTENSITY	
	ADRSD	UNIV						
Ø Ø Ø Ø	NUL (0)	DLE (16)	SP 14% (32)	0 56% (48)	@ 0% (64)	P 4% (80)	\ 14% (96)	p 56% (112)
Ø Ø Ø 1	SOH GTL (1)	DC1 LLO (17)	! 16% (33)	1 62% (49)	A 1% (65)	Q 4% (81)	a 16% (97)	q 62% (113)
Ø Ø 1 Ø	STX (2)	DC2 (18)	" 17% (34)	2 69% (50)	B 1% (66)	R 4% (82)	b 17% (98)	r 69% (114)
Ø Ø 1 1	ETX (3)	DC3 (19)	# 19% (35)	3 75% (51)	C 1% (67)	S 5% (83)	c 19% (99)	s 75% (115)
Ø 1 Ø Ø	EOT SDC (4)	DC4 DCL (20)	$ 20% (36)	4 81% (52)	D 1% (68)	T 5% (84)	d 20% (100)	t 81% (116)
Ø 1 Ø 1	ENQ PPC (5)	NAK PPU (21)	% 22% (37)	5 88% (53)	E 1% (69)	U 5% (85)	e 22% (101)	u 88% (117)
Ø 1 1 Ø	ACK (6)	SYN (22)	& 23% (38)	6 94% (54)	F 1% (70)	V 6% (86)	f 23% (102)	v 94% (118)
Ø 1 1 1	BEL (7)	ETB (23)	' 25% (39)	7 100% (55)	G 2% (71)	W 6% (87)	g 25% (103)	w 100% (119)
1 Ø Ø Ø	BS GET (8)	CAN SPE (24)	(28% (40)	8 56% (56)	H 2% (72)	X 7% (88)	h 28% (104)	x 56% (120)
1 Ø Ø 1	HT TCT (9)	EM SPD (25)	) 31% (41)	9 62% (57)	I 2% (73)	Y 8% (89)	i 31% (105)	y 62% (121)
1 Ø 1 Ø	LF (10)	SUB (26)	* 34% (42)	: 69% (58)	J 2% (74)	Z 9% (90)	j 34% (106)	z 69% (122)
1 Ø 1 1	VT (11)	ESC (27)	+ 38% (43)	; 75% (59)	K 2% (75)	[10% (91)	k 38% (107)	{ 75% (123)
1 1 Ø Ø	FF (12)	FS (28)	, 41% (44)	< 81% (60)	L 3% (76)	\ 11% (92)	l 41% (108)	¦ 81% (124)
1 1 Ø 1	CR (13)	GS (29)	- 44% (45)	= 88% (61)	M 3% (77)	] 12% (93)	m 44% (109)	} 88% (125)
1 1 1 Ø	SO (14)	RS (30)	. 47% (46)	> 94% (62)	N 3% (78)	∧ 12% (94)	n 47% (110)	~ (126)
1 1 1 1	SI (15)	US (31)	/ 50% (47)	? 100% (63)	O 3% (79)	_ 13% (95)	o 50% (111)	RUBOUT (DEL) (127)

THIS CHART ALSO CONTAINS GPIB COMMAND AND ADDRESS INFORMATION.

Appendix E

"F.D.CAL." 4907 DISC ALIGNMENT PROGRAM

```
1 GO TO 100
4 GOSUB 1020
5 WBYTE @63:
6 END
7 REM  T=THE TRACK BEING SELECTED
8 T=T+1
9 IF T<77 THEN 11
10 T=76
11 GO TO 520
12 T=T-1
13 IF T>-1 THEN 15
14 T=0
15 GO TO 520
16 T=0
17 GO TO 520
20 T=1
21 GO TO 520
24 T=38
25 GO TO 520
28 T=75
29 GO TO 520
32 T=76
33 GO TO 520
36 GOSUB 1020
37 REM  WBY TO SEEK AND LOAD THE HEAD
38 WBYTE @32:225,D,0,A,B,-ASC("$")
39 GO TO 38
40 GOSUB 1020
41 END
44 W=1
45 PRINT "GGGGGGGGGG"
46 PRINT "WRITE MODE ENABLED JJ **INSERT SCRATCH DISC**"
47 END
48 IF W=0 THEN 1070
49 W=0
50 PRINT "JDOING FAST FORMAT FOR HEAD AMPLITUDE CHECK"
51 GO TO 670
52 GOSUB 1020
53 GO TO 500
56 GOSUB 1020
57 PRINT USING "1/FAS":"INPUT DEVICE ADDRESS (0-3) :"
58 INPUT D
59 END
60 T=75
61 L=1
62 GO TO 520
100 INIT
105 REM  WRITTEN BY SERVICE SUPPORT     23-JAN-78
110 PAGE
120 REM  SET THE 4907'S CLOCK
130 WBYTE @32:37,0,0,0,-1
140 PRINT "                4907 DISC CALIBRATION PROGRAM"
150 PRINT
160 PRINT "This program allows alignment of the 4907 disc drive."
170 PRINT "The 4051 user keys select the various functions."
180 PRINT "All tests except the writing of a 2f pattern for Head "
190 PRINT "amplitude use the DYSAN 240S hard sectored alignment disc."
200 PRINT "When doing the head amplitude check a scratch  disc that has"
```

```
210 PRINT "had a long format performed on it MUST be used."
220 PRINT
230 PRINT "USER KEY.............FUNCTION.............................."
240 PRINT "1                    STOP-EXIT"
250 PRINT "2                    STEP IN(ONE TRACK)"
260 PRINT "3                    STEP OUT(ONE TRACK)"
270 PRINT "4                    SEEK TRACK 0"
280 PRINT "5                    SEEK TRACK 1"
290 PRINT "6                    SEEK TRACK 38"
300 PRINT "7                    SEEK TRACK 75"
310 PRINT "8                    SEEK TRACK 76"
320 PRINT "9                    LOAD HEAD"
330 PRINT "10                   UNLOAD HEAD"
340 PRINT "11                   ARMS WRITE MODE"
350 PRINT "12                   WRITES TRACK 76 WITH A 2F PATTERN"
360 PRINT "13                   SELECT YOUR OWN TRACK"
370 PRINT "14                   CHANGE DEVICE ADDRESS"
380 PRINT "15                   AUTO LOAD AND UNLOAD THE HEAD ON TRACK 75"
390 PRINT
400 M=32
410 PRINT "WHAT IS THE DEVICE ADDRESS (0-3)? :";
420 INPUT D
430 PRINT
440 PRINT "SELECT ANY USER KEY"
450 SET KEY
460 T=0
470 L=0
480 W=0
490 GO TO 4
500 PRINT USING "1/FAS":"TRACK (0-76)? :"
510 INPUT T
520 GOSUB 1020
530 REM  EQUATIONS FOR WBY THAT DOES A SEEK AND HEAD LOAD
540 T1=T*M
550 A=INT(T1/256)
560 B=T1-A*256
570 PRINT "TRACK ";T
580 IF L=1 THEN 600
590 GO TO 36
600 L=0
610 REM  THE NEXT FOUR LINES DO AUTO LOAD AND UNLOAD OF THE HEAD
620 WBYTE @32:225,D,0,A,B,-ASC("$")
630 FOR S=1 TO 400
640 NEXT S
650 GO TO 620
660 REM  SET SIZE OF FILES TO BE CREATED
670 F0=76*32*256-768
680 F1=32*256
690 REM  DOING A FAST FORMAT TO CLEAR DISC OF ALL FILES
700 CALL "DRES",D
710 CALL "FFRMT",D,"AMPLITUDE",1,1,"HEAD","",1,1,1,1,1
720 CALL "DREL",D
730 PRINT
740 PRINT "WRITING 2F PATTERN ON TRACK 76"
750 DIM C$(256)
760 CALL "MOUNT",D,A$
770 CALL "UNIT",D
780 REM  CREATE TWO FILES F0 AND F1
790 KILL "F0"
800 CREATE "F0","A";F0,0
```

```
810 KILL "F1"
820 CREATE "F1","A";F1,0
830 C$=CHR(0)
840 REM  CREATING A 2F CHARACTER= TO C$
850 FOR K=1 TO 8
860 C$=C$&C$
870 NEXT K
880 M$=CHR(13)
890 C$=REP(M$,256,1)
900 REM  OPENS FILE F1(TRACK 76) AND WRITES C$ INTO F1
910 OPEN "F1";3,"F",A$
920 FOR I=1 TO 32
930 PRINT #3;C$;
940 NEXT I
950 CLOSE
960 T=76
970 REM  GOES INTO A READ OF TRACK 76
980 PRINT
990 PRINT "NOW READING ON ";
1000 GO TO 520
1010 REM  DISABLES WRITE MODE
1020 IF W=0 THEN 1060
1030 W=0
1040 PRINT "GGGG"
1050 PRINT "WRITE MODE DISABLED"
1060 RETURN
1070 PRINT "GGGGG"
1080 PRINT
1090 PRINT "WRITE MODE ISN'T ENABLED"
1100 END
```