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THEORY OF OPERATION

INTRODUCTION

The standard 4404 Mass Storage Unit includes a 40M byte hard disk subsystem with a 5 1/4-inch floppy disk as standard. A 40M byte hard disk with a 1/4-inch streaming tape for backup is optional. Access to the mass storage is through the standard Small Computer Standard Interface (SCSI). See Figure 2-1.

Figure 2-1. Mass Storage Unit Components.

This section describes first the Small Computer Standard Interface (SCSI), then the circuitry of the Mass Storage Unit disk drives, controllers, and power supply. The back of this section contains information on multiple unit installation and strap options.

THE SMALL COMPUTER STANDARD INTERFACE

The Small Computer Standard Interface (SCSI) is a Tektronix adaptation of the Small Computer System Interface (SCSI) described in ANSI document x3T9.2/82-2. The SCSI is a parallel data bus designed to allow device-independent communication between as many as eight compatible MSU's. The bus is dedicated to transferring data to and from Mass Storage Units, such as disk drives.

Figure 2-2 shows a simple system in which the CPU is connected through the SCSI to two different kinds of disk controllers. In any transfer over the SCSI, one device acts as an "Initiator" and one dewvice acts a "Target". The Initiator begins a bus operation by selecting the Target. Once the Target has been selected it takes over and controls the operation until it is completed.

Figure 2-2. An SCSI System.

As an example, suppose that the CPU wants to send a data file to the second Mass Storage Unit. First, the CPU's interface, acting as Initiator, selects the appropriate MSU as its Target. After being selected as Target, the interface in the MSU must request information from the terminal telling it how much data is to be transferred, the direction of the transfer, and how the data is to be stored on the disk.

Next, the interface in the MSU requests data bytes from the CPU. The transfer operation can involve a single byte or many bytes; it can consist of commands, data, or status information. When the proper number of bytes has been transferred, the MSU signals the CPU that the operation is complete and the bus is released for other devices to use.

Physically, the SCSI consists of eight data bus lines and nine control signal lines. Table 2-1 describes the signals. Timing information for operations is contained under "Hard Disk Controller" later in this section.

Table 2-1

SIGNALS

Name	Definition
I-O/O-1 (In/Out)	The Hard Disk Controller drives this line low to indicate that it is sending data over the to the host system. A logic high on this line indicates that data is coming from the host to the Hard Disk Controller. For this signal to be valid, REQ-O must be true.
C-O/D-1 (Command/Data)	This signal indicates whether information currently coming over the consists of command bytes or data bytes; a low means command bytes, a high means data bytes. For this signal to be valid, REQ-O must be true.

Table 2-1 (cont)

SIGNALS

Name	Definition
BUSY-O	The Hard Disk Controller pulls this signal low when it has been addressed by the host. This tells the host that the Hard Disk Controller is ready to participate in transactions.
MSG-O (Message)	The Hard Disk Controller pulls this signal low to indicate to the host that a command has been completed. As long as MSG-O is true, I-O/O-1 is low; this is so that the Hard Disk Controller can drive the . For MSG-O to be valid, REQ-O must be true.
REQ-O (Request)	The Hard Disk Controller pulls this signal low for each byte it transfers across the . When this signal goes low it indicates that I-O/O-1, C-O/D-1, MSG-O, and DATA are valid.
ACK-O (Acknowledge)	The host pulls this signal low in response to each REQ-O from the Hard Disk Controller. This indicates that the host is ready to send or receive a byte over the . The host must send an ACK-O for each REQ-O from the Hard Disk Controller.
RST-O (Reset)	The host pulls this signal low to force the Hard Disk Drive to the idle state. The Hard Disk Drive clears to its initial state and all signals to the drives are deactivated.

Table 2-1 (cont)

SIGNALS

Name	Definition
SEL-O (Select)	The host pulls this signal to initiate a command transaction. Simultaneously with SEL-O, the host asserts one of the data bus lines to select a particular Hard Disk Controller. The Controller must not be busy (BUS-O low) and the host must deactivate SEL-O before the end of the current command transaction.
DBO-O thru DB7-O	These data lines carry data and command bytes. They are also used one at a time to select an individual Hard Disk Controller in a multicontroller system. (DBO-O selects controller O, DB1-O selects controller 1, and so on.)

FUNCTIONAL OVERVIEW

The 4404 Mass Storage Unit has the following functional blocks:

- The Floppy Disk Controller
- The Floppy Disk Drive
- The Hard Disk Controller
- The Hard Disk Drive
- The Power Supply

Since the Floppy Disk Drive is described in detail in the 119-1636-00 Floppy Disk Drive Service Manual, this section contains only a general functional description.

The Floppy Disk Controller and the Hard Disk Controller are described in detail in this manual. The Hard Disk Controller is common to both standard and optional Mass Storage Unit in the 4400 series.

Since the Hard Disk Drive is described in detail in the 119-1644-00 Hard Disk Drive Service Manual, this section contains only a general functional description, showing how the drive fits into the architecture of the 4400 series.

The majority of the Floppy Disk and Hard Disk Controllers' circuitry is not repairable to the component level. Therefore, this manual describes both controllers in general functional terms without detailed module information. See the Schematics section for the first level of interface circuitry. ~~Refer to Appendices A and B for descriptions of the Controllers' command sets.~~

FLOPPY DISK CONTROLLER

Figure 2-3 is a block diagram of the Floppy Disk Controller. The Floppy disk Controller's functional blocks are described in detail in the following paragraphs.

Figure 2-3. Floppy Disk Controller Block Diagram.

6502A MICROPROCESSOR

The 6502A Microprocessor supervises all Floppy Disk Controller operation. Acting upon instructions contained in ROM, the 6502A sets up the Disk Controller for disk read/write operations, and it sets up the interface to control disk data transfers between the host and the Floppy Disk Controller.

The 6502A's inputs and outputs function as follows:

- A0 through A15: the address bus.
- D0 through D7: the data bus.
- PHASE2-0: a clock output that synchronizes read/write operations.
- R-1/W-0: controls the direction of data flow on the data bus.
- PHASE0-0: the master clock input to the 6502A.
- PFAIL-0: an input from the power supply that indicates power failure.
- IRQ-0: indicates to the 6502A that the Disk Controller finished a seek operation or completed a command.

RAM

You use the RAM primarily as a buffer to hold disk data. The RAM consists of a single 6116 2K x 8 bit static RAM chip. You enable the RAM by asserting RAMCS-0 for addresses in the range of 0 to 07FF (hexadecimal).

ROM

The ROM is a 2732A 4K x 8-bit EPROM. It contains instructions for the 6502A Microprocessor. ROMCS-0 enables the ROM for addresses in the range of F000 to FFFF (hex).

ADDRESS DECODER

The Address Decoder consists of two Programmable Array Logic Devices. Each PAL contains an array of logic gates that is programmed to decode certain address bits and control signals and provide select signals for Floppy Disk Controller functions. Address mapping in hexadecimal for the Floppy Disk Controller is as follows:

RAM	0 through 07FF
ROM	F000 through FFFF
DATA	0801
CONTROL/STATUS	0800
DISK CONTROLLER CONTROL	0804
DISK CONTROLLER STATUS	0805
TERMINAL COUNT	0803

The Address decoder's outputs are as follows:

- RD-O (Read). This signal is true when the 6502A is reading data.
- WR-O (Write). This signal is true when the 6502A is writing data.
- STATUSEN-O (Status Enable). This signal enables the status register in the Interface.
- OUTCLK-O (Output Clock). This signal clocks the output data register in the Interface.
- OUT-O (Data Out). This signal enables the data output driver in the Interface.
- IN-O (Data In). This signal enables the data input register in the Interface.
- CMDCLK-O (Command Clock). This signal clocks the command register in the Interface.
- TC-O (Terminal Count). This signal indicates to the Disk Controller that the last byte has transferred in a disk read or write operation.
- FDCCS-O (Floppy Disk Controller Chip Select). This signal enables the uPD765 Floppy Disk Controller chip.
- ROMCS-O (ROM Chip Select). This signal enables the ROM.
- RAMCS-O (RAM Chip Select). This signal enables the RAM.

See the following truth table (Table 2-2) for the Address Decoder's inputs and outputs.

Table 2-2

ADDRESS DECODER TRUTH TABLE*

	INPUT				
OUTPUT	R-1/W-0	Phase 2-1	Busy-1	I-0/O-1	A15
RD-O	H	H	X	X	X
WR-O	L	H	X	X	X
STATUSEN-O	H	H	X	X	L
OUT-O	X	X	H	H	X
OUTCLK-O	X	X	X	X	L
IN-O	X	H	X	L	L
CMDCLK-O	L	H	X	X	L
TC-O	X	H	X	X	L
FDCCS-O	X	H	X	X	L
ROMCS-O	X	X	X	X	H
RAMCS-O	X	X	X	X	L

* Convention: L = Low Logic Level
H = High Logic Level
X = Don't Care

Table 2-2 (cont)

ADDRESS DECODER TRUTH TABLE*

OUTPUT	INPUT A14	A13	A12	A11	A10	A2	A1	A0
RD-0	X	X	X	X	X	X	X	X
WR-0	X	X	X	X	X	X	X	X
STATUSEN-0	L	L	L	H	L	L	L	L
OUT-0	X	X	X	X	X	X	X	X
OUTCLK-0	L	L	L	H	L	L	L	H
IN-0	L	L	L	H	L	L	L	H
CMDCLK-0	L	L	L	H	L	L	L	L
TC-0	L	L	L	H	L	L	H	H
FDCCS-0	L	L	L	H	L	H	L	L
ROMCS-0	H	H	H	X	X	X	X	X
RAMCS-0	L	L	L	L	X	X	X	X

* Convention: L = Low Logic Level
H = High Logic Level
X = Don't Care

INTERFACE

The Interface consists of several registers that the 6502A Microprocessor uses to conduct data transfers:

- The 6502A writes into the command register and driver (U145 and U45) to assert the control signals.
- The 6502A reads status signals through U150.
- The 6502A sends data through the output data register and driver, U155 and U160, and it receives data through the input data register, U165.

The signal lines are defined under "The Mass Storage Interface Bus" earlier in this section. The control signals for the various registers are defined under "Address Decoder."

DISK CONTROLLER

The Disk Controller does most of the interfacing tasks, such as data encoding and read/write head stepping for the floppy disk drives. Except for a few auxiliary circuits, the Disk Controller consists of a single large-scale integrated circuit, U225, which will be called the FDC in the following discussion.

The FDC has an instruction set that the 6502A Microprocessor uses to control drive operation. For example, to read data from a disk, the 6502A first sends the Seek command, then a Sense Interrupt Status command, followed by a Read Data Command.

The Seek command tells the FDC which track on the disk to send the read/write head to; the FDC then steps the head in or out to the proper track. The 6502A issues the Sense Interrupt Status command to see if the seek operation was successful and to set up the FDC receive the Read Data command.

The Read Data command tells the FDC which sectors on the selected track to read and how the data is formatted (number of bytes per sector, etc.). To carry out the Read Data Command, the FDC begins to assemble the serial data from the disk into 8-bit bytes. The FDC signals the 6502A as each byte is available, using the RQM bit of the main status register in the uPD765 (FDC). The 6502A stores the byte in a RAM buffer. When the proper number of bytes is transferred, the 6502A signals the FDC by asserting TC-O (Terminal Count). The FDC signals its completion by giving IRQ.

As shown in Figure 2-4, the FDC contains seven functional blocks:

Data Bus Buffer. The Data Bus Buffer links the FDC's internal data bus with the 6502A's data bus.

Read/Write Control Logic. The Read/Write Control Logic controls 6502A access to the FDC.

Registers. The FDC contains an 8-bit main status register and a data register stack consisting of several sequentially accessed registers where the 6502A writes commands and data.

Serial Interface Controller. During disk write operations, the Serial Interface Controller converts data bytes from the 6502A into an MFM encoded serial data stream for the disk; during reads, it converts the serial data from the disk back into bytes.

Drive Interface Controller. The Drive Interface Controller oversees drive operation. It controls such functions as head stepping and drive selection.

Input and Output Ports. The Input and output ports provide the electrical interface between the Drive Interface Controller and the drives.

Figure 2-4. FDC Block Diagram.

CLOCK GENERATOR

The Clock Generator supplies timing signals for the 6502A Microprocessor, the FDC, and the Data Separator.

U360, the master oscillator, generates a 16 MHz reference clock. This signal drives a counter, U260, where it is divided to produce several square wave outputs: 8 MHz (Pin 11), 4 MHz (Pin 10), 2 MHz (Pin 9), 1 MHz (Pin 8), 500 KHz (Pin 3), and 250 KHz (Pin 4). These outputs are applied to U255, a dual 4-to-1 multiplexer.

The purpose of the multiplexer is to select clock frequencies for the Data Separator and FDC. The frequencies selected are controlled by the multiplexer's A and B inputs (Pins 14 and 2). The A input, controlled by MFM-1 from the FDC, selects between single (FM) and double density (MFM) data encoding. The B input, controlled by MINISEL-0, selects between between 5 1/4" and 8" drive operation. Since the Mass Storage Unit uses only double density recording and 5 1/4" drives, A is always high and B is always low. This results in 4 MHz and 500 KHz clock signals at multiplexer outputs 1Y and 2Y, respectively.

Output 2Y drives U250A, which, together with U250B generates WCLOCK-1. WCLOCK-1 is a positive-going 250 ns pulse ocurring at 500 KHz. Output 1Y is CLOCK-1, a 4 MHz square wave that drives the Data Separator, FDC, and motor off/on timing circuit.

DATA SEPARATOR

When it is reading a disk, the disk drive sends back a serial bit stream that contains both clock and data bits. The Data Separator, U345, converts the bit stream into separate clock and data signals for the FDC, which cannot distinguish between data and clock bits. Since the read data stream can vary in frequency, the Data Separator must lock onto the clock bits in the data stream and maintain a constant phase relationship between the separated clock and data signals. For the timing relationships of the Data Separator's inputs and outputs, see Figure 2-5.

Figure 2-5. Data Separator Block Diagram and Timing.

Figure 2-6. Typical System Configuration.

WRITE PRECOMPENSATION LOGIC

The purpose of the Write Precompensation Logic is to compensate for bit shift. Bit shift arises when the flux transitions by which data and clock bits are stored on the disk become very closely spaced, especially on the inner tracks of the disk during double density recording. When data is read back from the disk, current changes induced in the read head cannot take place instantaneously. The read head is still responding to one transition when the next one comes along; this means that the next transition is partially cancelled. The effect of this is to spread the current peaks apart, causing a shift in timing.

The Write Precompensation Logic corrects for bit shift by preshifting the write data in a direction opposite to the expected bit shift. The FDC has two outputs, PRESHIFT0-1 and PRESHIFT1-1, that tell the Write Precompensation Logic which direction to shift the data bits.

The Write Precompensation Logic consists of an 8-bit, serial-in, parallel-out shift register (U220) and a multiplexer (U210). The 8 MHz output of the Clock Generator clocks the shift register. (The jumper at J7 selects between 8 MHz and 16 MHz, but the Mass Storage Unit and 4926 Option 25 use only 8 MHz.)

The serial input to the shift register, WDATA-1 (Write Data), advances through the register at 125 ns per stage. This means that outputs QA, QC, and QE represent WDATA-1 delays of 0, 250 ns, and 500 ns, respectively. The multiplexer selects among these delayed outputs for precompensation: QA is selected for 250 ns early preshift, QC for no preshift, and QE for 250 ns late preshift. The multiplexer's output is inverted and becomes WDATA-0, the precompensated write data output to the disk drive.

DRIVE SELECT DECODER

<this will change>

The Drive Select Decoder decodes SEL0-0 and SEL1-0 from the FDC and provides select signals for four drives. Only DSEL0-0 and DSEL1-0 are used in the Mass Storage Unit. Jumpers must be installed at UNIT0 and UNIT1 in order to drive the RDY-0 (Ready) signal line.

DISK CONTROL MULTIPLEXER

Several pins on the FDC have a dual function: During Seek operations, they carry one signal; during read/write operations, they carry another. The purpose of the Drive Control Multiplexer is to steer the appropriate signal to or from the drives at the right time. Signal routing is controlled by RW-0/SEEK-1 from the FDC.

The Disk Multiplexer's outputs are as follows:

- DIR-0 (Direction). This signal controls whether the read/write head steps in or out.
- STEP-0 (Step Head). This signal steps the read/write head in or out one track for each low to high transition.
- WPROT-0 (Write Protect). This signal, when low indicates that the diskette in the drive is write protected.
- TK-0 (Track 0). This signal indicates that the read/write head is at track 0.

FLOPPY DISK DRIVE

FUNCTIONAL CHARACTERISTICS

The Floppy Disk Drive consists of read/write and control electronics, drive mechanism, read/write head, and precision track positioning mechanism. These components perform the following functions:

- Interpret and generate control signals.
- Move read/write heads to the desired track.
- Read and write data.

See Figure 2-7 for the interface signals and their relationship to the internal functions.

Read/Write and Control Electronics

The electronics package contains:

- Index detector circuits
- Head position actuator driver
- Read/write amplifier and transition detector
- Write protect detector
- Drive select circuit
- Drive motor control

Drive Mechanism

The dc drive motor under servo speed control (using an integral tachometer) rotates the spindle at 300 rpm through a direct drive system. An expandable collet/spindle assembly provides precision media positioning to ensure data interchange.

Positioning Mechanics

The read/write head assembly is accurately positioned through the use of a band positioner which is attached to the head carriage assembly. This positioner rotates in discrete increments by a stepping motor to accomplish precise track location.

Figure 2-7. Floppy Disk Drive Functional Diagram.

Read/Write Heads

A single element ceramic read/write head with tunnel trace elements provide erased areas between data tracks. Thus, normal interchange tolerances between media and drives do not degrade the signal-to-noise ratio. This ensures the interchangeability of floppy disks.

The read/write heads are mounted on a carriage which is located on precision carriage ways. A platen on the base casting holds the floppy disks on a plane perpendicular to the read/write heads. This precise registration assures compliance with the read/write heads (which are in direct contact with the floppy disk.

Recording Formats

The format of the data recorded on the floppy disk is totally a function of the CPU. This format takes maximum advantage of the available bits that can be written on any one track.

FUNCTIONAL OPERATIONS

Power Sequencing

Applying dc power to the Floppy Disk Drive can be done in any sequence. However, during power up, the WRITE GATE line must be held inactive or at a high level. This prevents possible "glitching" of the media. After applying dc power, introduce a 100 ms delay before performing any operation.

After powering on, the initial position of the read/write heads with respect to the data tracks on the media is indeterminant. In order to assure proper positioning of the read/write heads after power on, perform a Step Out operation until the TRACK 00 line becomes active (Recalibrate).

Drive Selection

When you jumper the DRIVE SELECT line you want to activate, then that line alone responds to input lines or gate output lines.

Motor On

In order for the host system to read or write data, you must turn on the dc drive motor by activating the MOTOR ON line. You should introduce a 500 ms delay (after activating this line) to allow the motor to come up to speed before attempting to read or write.

The host system must turn off the motor by deactivating the the MOTOR ON line. The control electronics keep the motor active for three seconds, after MOTOR ON is deactivated. This allows reselecting during copy operations.

Track Accessing

Seeking the read/write heads from one track to another is accomplished by:

- Activating the DRIVE SELECT line
- Selecting the desired direction by using the DIRECTION SELECT line
- WRITE GATE being inactive
- Pulsing the STEP line.

Multiple track accessing is accomplished by the repeated pulsing of the STEP line (with direction valid) until reaching the desired track. Each pulse on the STEP line causes the read/write heads to move one track either in or out, depending on the DIRECTION SELECT line. Head movement is initiated on the trailing edge of the step pulse.

Step Out

With the DIRECTION SELECT line at a plus logic level (2.4 to 5.25 V), a pulse on the STEP line causes the read/write heads to move one track away from the disk center. The pulse(s) applied to the STEP line should have the timing characteristics shown in Figures 2-8 and 2-9.

Step In

With the DIRECTION SELECT line at a minus logic level (0 to 0.4 V), a pulse on the STEP line causes the read/write heads to move one step closer to the disk center. The pulse(s) applied to the STEP line should have the timing characteristics shown in Figures 2-8 and 2-9.

Side Selection

Head selection is controlled via the I/O signal line designated SIDE SELECT. A plus logic level on the SIDE SELECT line selects the read/write head on the side 0 surface of the floppy disk. A minus logic level selects the side 1 read/write head. When switching from one side to the other, a 100 us delay is required after SIDE SELECT changes state before a read or write operation can be initiated. Figure 2-10 shows the use of SIDE SELECT prior to a read operation.

Figure 2-8. STEP to READ Timing Characteristics.

Figure 2-9. WRITE to STEP Timing Characteristics.

Figure 2-10. READ to WRITE Timing Characteristics.

Read Operation

You read data from the Floppy Disk Drive by:

- Activating the DRIVE SELECT line
- Selecting the head
- WRITE GATE being active

Write Operation

You write data to the Floppy Disk Drive by:

- Activating the DRIVE SELECT line
- Selecting the head
- Activating the WRITE GATE line
- Pulsing the WRITE DATA line with the data to be written.

Sequence of Events

The timing diagrams shown in the preceding Figures 2-8, 2-9, and 2-10, and in Figure 2-11 that follows, indicate the necessary sequence of events (with associated timing restrictions) for proper operation.

Figure 2-11. POWER ON to STEP Timing Characteristics.

ELECTRICAL INTERFACE

All lines in the signal interface (control and data transfer) are digital in nature; and provide signals either to the drive (input) or to the host (output), via interface connector P1/J1. See Figure 2-12 for all interface connections.

Figure 2-12. Interface Connections.

HARD DISK CONTROLLER

As shown in the block diagram, Figure 2-13, the Hard Disk Controller contains the following functional blocks:

- Host Interface. The Host Interface connects the Hard Disk Controller's internal data bus to the . The movement of data through the Host Interface is controlled by the State Machine.
- Processor. All functions within the Hard Disk Controller are under the general control of an 8-bit microprocessor.
- State Machine. The State Machine synchronizes the operation of the Host Interface, the Serializer/Deserializer, and the Sector Buffer.
- Serializer/Deserializer. The Serializer/Deserializer converts parallel data coming over the internal data bus to a NRZ (Non-Return to Zero) serial data stream suitable for the Data Separator. It converts serial data coming from the Data Separator to parallel format for transfer over the internal data bus.
- Data Separator. The Data Separator converts the serial NRZ data stream coming from the Serializer/Deserializer to serial MFM (Modified Frequency Modulation) encoded data suitable for the Hard Disk Drive. The Data Separator also converts MFM data coming back from the drive to NRZ format.
- The Sector Buffer. The Sector Buffer temporarily holds data during transfers between the disk drive and the host; its function is to prevent overrunning the host or the drive.

Figure 2-13. Hard Disk Controller Block Diagram.

Figures 2-14, 2-15, and 2-16 show signal timing for the Hard Disk Controller.

Figure 2-14. Hard Disk Controller Select Timing.

Figure 2-15. Hard Disk Controller Data Output Timing.

Figure 2-16. Hard Disk Controller Data Input Timing.

HARD DISK DRIVE

As shown in the block diagram, Figure 2-17, the Hard Disk Drive's circuitry is divided into the following functional devices:

- Control Logic
- Read Write Circuits
- Stepping Motor Control
- Motor Speed Control

The following paragraphs describe each of these devices.

Figure 2-17. Hard Disk Drive Block Diagram.

CONTROL LOGIC

The Control Logic includes all circuitry that directs and coordinates the drive's operation. Most Control Logic functions are performed by an 8-bit microprocessor. The microprocessor's responsibilities include the following functions:

- Determining when the spindle motor is up to operating speed.
- Monitoring the Track 0 Sensor in the Head Positioning Mechanism to see if the read/write heads are at track 0 (required in order to calibrate head position).
- Controlling and monitoring track-to-track head stepping.
- Receiving control signals from and transmitting status signals to the Hard Disk Controller.

READ/WRITE CIRCUITS

The read circuit converts the raw MFM data signal from the read/write heads to a differential, serial data stream suitable for the Hard Disk Controller.

The write circuit converts the differential MFM data from the Hard Disk Controller into a write signal current within the read/write heads.

STEPPING MOTOR CONTROL

As directed by the Control Logic, the Stepping Motor Control drives the stepping motor in the Head Positioning Mechanism, causing the read/write heads to move from track to track.

MOTOR SPEED CONTROL

The Motor Speed Control drives the Spindle Motor at a constant speed of 3600 rpm. A Hall-Effect sensor within the Spindle Motor provides feedback to the Motor Speed Control, allowing it to maintain a constant speed.

DRIVE INPUT/OUTPUT SIGNALS

Tables 2-3, 2-4, and 2-5 describe the input/output signals for the Hard Disk Drive.

Table 2-3

DRIVE CONTROL INPUT SIGNALS

Name	Description
REDUCED WRITE CURRENT-O	This signal, when asserted at the same time as WRITE GATE-O, causes the write circuitry to write on the disk with reduced write current. Not all makes and models of the drive use the Reduced Write Current signal line.
WRITE GATE-O	When low, this signal enables the write circuitry; when high, it enables the read circuitry.
DIRECTION IN-O	This signal determines the direction of the read/write head's motion during stepping. When DIRECTION IN-O is low, the head moves toward the center of the disk (higher numbered tracks).
STEP-O	This signal moves the read/write head in or out, as determined by DIRECTION IN-O. Movement takes place on the low-to-high transition of STEP-O.
DRIVE SELECT1-O thru DRIVE SELECT4-O	These signals activate the drive. Only one signal is used for a particular drive; a shunt block (strap option) within the drive determines which DRIVE SELECT signal is used.

Table 2-4

DRIVE CONTROL OUTPUT SIGNALS

Name	Description
SEEK COMPLETE-O	This signal goes true when the read/write head has settled on the final track at the end of a seek operation. SEEK COMPLETE indicates that reading or writing can now take place.
TRACKO-O	This signal goes true when the read/write head is positioned at Track 0, the outermost data track.
WRITE FAULT-O	This signal, when low, indicates a fault condition that may cause improper writing on the disk. Further writing and stepping are inhibited until the fault is corrected. These conditions are detected: o Write current while WRITE GATE is not true, or no write current with WRITE GATE true and DRIVE SELECTED true. o Multiple heads selected, no head selected, or head improperly selected. o DC voltages grossly out of tolerance.
INDEX-O	This signal goes true once each revolution of the disk to indicate the beginning of a track. The low-to-high transition of the signal is the index.

Table 2-5

DRIVE DATA TRANSFER LINES

Name	Description
DRIVE SELECTED-0	This signal, when low, indicates to the host that the drive is in the selected state.
MFM READ DATA-0 and MFM READ DATA-1	This differential pair of signal lines carries the serial MFM data stream recovered from the disk. The transition of MFM READ DATA-1 to a level more positive than MFM READ DATA-0 represents a flux transition on the track being read.
MFM WRITE DATA-0 and MFM WRITE DATA-1	This differential pair of signal lines carries the serial MFM data to be written on the disk. The transition of MFM WRITE DATA-1 to a level more positive than MFM WRITE DATA-0 produces a flux reversal on the track being recorded. These signal lines must be driven to their inactive states during read operations.

POWER SUPPLY

The MSU Power Supply uses a high efficiency, pulse-width modulated inverter to generate +5 Vdc and +12 Vdc regulated outputs. The supply rectifies and filters the line voltage, then chops the resulting DC voltage at approximately 20 KHz. The 20 KHz chopped current passes through a transformer to two secondary windings where it is rectified, filtered, and regulated to produce the +5 Vdc and +12 Vdc outputs. The +5 Vdc output is regulated by varying the duty cycle of the 20 KHz chopped current; the +12VDC output is regulated independently by a conventional series pass regulator.

The following paragraphs describe the Power Supply's circuitry in detail. Refer to the block diagram, Figure 2-18, and to the schematic diagram while reading the circuit descriptions.

Figure 2-18. Power Supply Block Diagram.

VDE FILTER

The VDE Filter prevents electromagnetic interference from entering or leaving the power supply by way of the ac power lines. The filter is designed to meet the requirements of the Verband Deutscher Electrotekniker (VDE), which is the certifying agency for electromagnetic compatibility in the Federal Republic of Germany.

TRIAC/TRIGGER

The TRIAC/Trigger circuit serves two functions: it controls ac power to the power supply and it supplies start-up power to the Schmitt Trigger, Base Drive, and Pulse-Width Modulator circuits.

TRIAC Q130 acts as a switch to control AC power to the power supply. To turn on power, the TRIAC must be triggered; this is the function of the triggering circuitry. Triggering, in turn, is enabled and disabled by the Logical On/Off Switch.

As long as the 4926 is plugged into the power mains, a portion of the line voltage appears, by way of voltage divider R138/137, across the primary (Pins 2 and 3) of T140. The triggering voltage for the TRIAC is developed across the secondary winding between Pins 4 and 5 of T140. The winding between Pins 7 and 9 of T140 controls TRIAC triggering, as follows: During power-off, the Logical On/Off Switch presents an effective short circuit across Pins 7 and 9. This reflects a very low impedence back into the primary of T140 and prevents sufficient triggering voltage from being developed across Pins 4 and 5. At power-up, the Logical On/Off circuit releases the short from Pins 7 and 9, thereby allowing the TRIAC to be triggered.

As the short is removed from Pins 7 and 9 of T140, a voltage is developed across that winding as well. This voltage is rectified and supplies (through CR153 and R153) start-up power to the Schmitt Trigger, Base Drive, and Pulse-Width Modulator circuits.

LOGICAL ON/OFF SWITCH

The Logical On/Off Switch allows remote on/off control of power to the power supply. The circuit consisting of Q155, Q157, and their associated components acts as an SCR that can be turned off or on by the ON-O signal line. As long as ON-O is held at TTL logic high, the SCR will switch on whenever the voltage across Pins 7 and 9 of T140 tries to rise above a low value. This, in effect, shorts out T140 and prevents the power control TRIAC from being triggered.

When ON-O is pulled low, the SCR action of Q155 and Q156 is disabled. This allows two things to happen: First, the TRIAC can now be triggered. Second, the voltage across Pins 7 and 9 can rise to its full value. This voltage, after rectification, supplies start-up power to the Schmitt Trigger, Base Drive, and Pulse-Width Modulator circuits.

SCHMITT TRIGGER

The Schmitt Trigger circuit controls power to the Base Drive and Pulse-Width Modulator circuits. At power-up, full-wave rectified current supplied through CR153 and R153 from the Logical On/Off Switch charges C140. When the charge on C140 reaches about 18 V, the Schmitt Trigger (Q140 and Q145) switches state, turning on Q150 and Q160; this turns on power to the Base Drive and Pulse-Width Modulator circuits, which then begin to drive the Switching Transistors. C140 contains enough charge to sustain operation until the rectified, filtered voltage in the +12 Vdc Supply comes up to a high enough level that it can take over and supply power to the Schmitt Trigger through CR153.

PULSE WIDTH MODULATOR

The Pulse-Width Modulator (PWM), U150, is the driving and regulating element in the 20 KHz switching portion of the power supply. Figure 2-19 is a simplified block diagram of U150 and its associated components. Within U150, an oscillator alternately switches on two output transistors, Qa and Qb, at approximately 20 KHz. The ratio of on time to off time (duty cycle) of the oscillator's outputs is controlled by an error amplifier. Qa and Qb, acting through the Base Drive circuit, each control the on time of one of the Switching Transistors. (Qa controls Q435 and Qb controls Q430.)

Through its INV and NINV inputs, the error amplifier compares a sample (one-half) of the +5 Vdc Supply's output voltage with a reference voltage generated by a stable regulator within U150. The reference voltage supplied to the error amplifier may be adjusted by R165. Any difference in voltage sensed by the error amplifier causes the oscillator's duty cycle to change; this changes the output voltage of the +5 Vdc Supply in such a direction as to bring it back to its set point.

The current-limiting circuit samples the voltage across a 50 milliohm resistor in the +5V return line. When current from the +5 Vdc Supply goes beyond approximately 7 A, the output of the current limiting amplifier begins to decrease the duty cycle of the oscillator. This lowers the output voltage of the +5 Vdc Supply and prevents excessive current from being drawn.

Figure 2-19. Pulse Width Modulator.

BASE DRIVE AND SWITCHING TRANSISTORS

The Base Drive circuit drives the Switching Transistors through transformer T240. The driver transistors Q240 and Q250 conduct alternately. Transistor Q255 switches on as one driver transistor is turning on and the other is turning off; this aids the switching process by shunting current produced by the collapsing field in T240 and preventing the off Switching Transistor from prematurely turning on.

The Switching Transistors alternately switch current through the primary of T340. Current flows first in one direction, through Q435, from the +160 V output of the Rectifier and DC Filter; then it flows in the opposite direction, through Q430, from the -160 V output. The resulting alternating current in T340's secondaries powers the +5 Vdc and +12 Vdc Supplies. Diodes CR433 and CR430 prevent reverse voltage damage to Q430 and Q435. A snubber circuit, C332 and R434, helps to prevent transients and minimize ringing during transistor off time.

LINE VOLTAGE SELECTOR, RECTIFIER, AND D.C. FILTER

Line current is rectified by CR139 and filtered by C110 and C210. During 220 Vac operation, CR139 acts as a full-wave bridge, producing about 160 volts each across C110 and C210. During 115 Vac operation, switch S310 connects one side of the ac line at the junction between C110 and C210. This causes CR139, C110, and C210 to act as a voltage doubler, again producing 160 V across each capacitor.

Several components (L430, L225, T330, C221, C234) provide additional filtering. A neon lamp, DS320, flashes when voltage greater than 85 V is present on C110 and C210. One side of the fan is connected to the junction of C110 and C210; this provides 115 Vac to the fan regardless of whether S310 is in the 230 V or the 115 V position. Capacitors C221 and C234 act as an ac voltage divider; they provide about 160V across each of the Switching Transistors. The common point between C221 and C234 is the return path for the 20 KHz switched current through T340.

+5 VDC SUPPLY

The +5 Vdc Supply voltage is developed from the center-tapped secondary winding between Pins 5 and 7 of T340. The output of this winding is full-wave rectified then filtered by an LC filter. The output of the filter is the +5 Vdc Supply. A sample of the +5 Vdc output is fed back, through R173 and voltage divider R149/148, to the Pulse Width Modulator to stabilize the voltage.

+12 VDC SUPPLY

The +12 Vdc Supply voltage is developed from the secondary winding between Pins 2 and 4 of T340. After rectification and filtering, the output of this winding is regulated by a conventional series-pass voltage regulator consisting of U350B and Q460. Q360 prevents excessive current from being drawn from +12 Vdc Supply by turning on, thereby decreasing drive to Q460, when the current exceeds approximately 5 A.

MULTIPLE UNIT INSTALLATION

Figure 2-20 shows a typical multiple unit installation. The procedure for connecting more than one Mass Storage Unit to the CPU differs from the single unit procedure in the following ways:

- Each unit must be given a unique unit address. This means that the factory default setting on all but one unit must be changed.
- The cables must be connected from host to unit and from unit to unit.
- Remove the factory-installed terminator boards or resistors R50 and R60 from all but the last unit on the SCSI.

Figure 2-20. Multiple Unit Installation.

To set up a multiple unit installation, proceed as follows:

1. Make sure that the proper tools and materials are available:

   - o Crosspoint screwdriver
   - o BNC tee connectors for the "Remote Power On" connectors, if the optional Remote Power Control cables are used. A tee connector is needed for all units except the last one in the installation.
   - o Small soldering iron suitable for working on etched circuit boards.
   - o Jumper wire: 30 gauge "wire-wrap" wire is adequate.
   - o Sharp, thin-bladed knife.

   NOTE

   The soldering iron, wire, and knife are necessary only to set the addresses.

2. Set the device addresses:

   a. Remove the top covers from all of the units except the last unit on the SCSI. The last unit is left at the factory default address setting of 0 (Hard Disk Controller) and/or 1 (Floppy Disk Controller).

   b. Using the procedure given under "Strap Options" later in this section, set each of the other devices to a unique device address. Do not use device address 7, which is reserved for the CPU.

3. Remove the external terminator from the rear of the MSU's.

4. Place the units at convenient locations near the host. The first unit must be within 6 ft (2 m) of the host.

5. Connect the 2m cables (supplied with units) from the host to the first unit and from unit to unit (see Figure 2-21). At the end position on the SCSI, place the unit with the terminator.

Figure 2-21. Connecting the 2m Cables.

6. Install a suitable power cord on each unit and connect the power cords to the power outlets.

7. Turn on power to the CPU and to all the Mass Storage Units. Check each unit to see that the fan is operating, indicating that the unit has power.

9. Check the operation of each unit, preferably by using CPU resident test commands. If these commands are not available, transfer a data file to each unit. Verify that the transferred file is identical to the original.

STRAP OPTIONS

HARD DISK CONTROLLER STRAP OPTIONS

Figure 2-22 shows the four strap options on the Hard Disk Controller. When shipped from the factory, these strap options are set as follows:

Name	Function	Condition
W1	Factory test	Must be installed
W2	Factory test	Must be installed
W3	Sector size	Set to 5 (512 bytes/sector)
S	Bus address select	Default is 0. May be set to 1-6. 7 is reserved for host.

Under ordinary circumstances, W1, W2, and W3 never need to be changed; however, when troubleshooting the MSU, check these options to see that they are installed properly.

Remove IC5J (if present) because the Terminator board terminates the same lines. The Floppy Disk Controller has full terminators also.

In systems having more than one MSU (or other unit) on the same SCSI, the Hard Disk Controller's address select strap option must be set so that each device responds to a unique bus address. To change the bus address from the factory default value you will need a sharp knife, a soldering iron and a piece of jumper wire about 1" long. Perform the change as follows:

1. Cut the circuit board trace connecting "S" to "0" (refer to Figure 2-22).

2. Install a jumper between "S" and the position (labeled 0 through 7) corresponding to the desired bus address. The first device on the SCSI should use the factory default setting, the second device will need a jumper installed to position 1, and s on through position 6. Position 7 (8OH) is reserved for the host.

Figure 2-22. Hard Disk Controller Strap Options.

DRIVE SELECT OPTION

The DRIVE SELECT option (on shunt block) determines which DRIVE SELECT signal line activates the drive. Use only DRIVE SELECT 1-0 and DRIVE SELECT 2-0.

The shunt block plugs into Pins 2 through 15. When you troubleshoot or install a drive, check the shunt block for proper installation.

Terminator Resistor Pack

I.C.6E should be present in the last drive on the control cable; that is, in Drive 0 for single drive configuration, and in Drive 1 for dual drive configuration.

Board to Chassis Grounding

The manufacturer of the disk drive module provides electrical isolation between the circuit board and the frame by means of two plastic washers under the rear circuit board mounting screws. You should remove these washers (then reinsert and tighten screws) to avoid frequent data errors.

Figure 2-23. Hard Disk Drive Strap Options.

FLOPPY DISK CONTROLLER STRAP OPTIONS

The four locations of strap options on the Floppy Disk Controller are:

- o J5 - ADDRESS SELECT jumper
- o J6 - DEVICE READY jumper
- o J7 - WRITE PRECOMPENSATION jumper
- o J8 - Factory Test jumper (always installed)

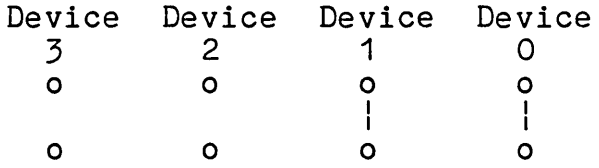
The ADDRESS SELECT setting at J5 selects the unique address of that Floppy Disk device, according to the selection matrix in Table 2-6. (The normal address is 1, unless you install multiple units.

Table 2-6

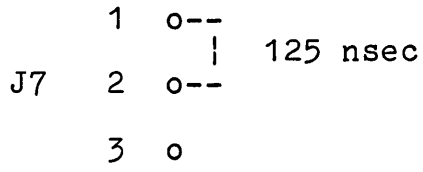
J5 ADDRESS SELECTION

	ADDRESS	1-2	3-4	5-6
	0	OFF	OFF	OFF
Factory setting:	1	ON	OFF	OFF
	2	OFF	ON	OFF
	3	ON	ON	OFF
	4	OFF	OFF	ON
	5	ON	OFF	ON
	6	OFF	ON	ON
	7	ON	ON	ON

Two UNIT READY jumpers at J6 should be placed on Device 0 and Device 1, as follows:



The WRITE PRECOMPENSATION jumper at J7 selects 125 nsec when set at the normal position on Pins 1 and 2.



(3): FLOPPY DISK DRIVE STRAP OPTIONS

Figure 2-24 shows the DRIVE SELECT (DS) device address selection for each Floppy Disk Drive. You jumper DS1 on the lower Floppy Disk Drive circuit board, and DS2 on the upper Floppy Disk Drive circuit board.

Jumpers should also be in place on the MM and HS strap option pins, as in Figure 2-24. Do not place jumpers on the MS, HM, HL, and IU pins.

Figure 2-24. Floppy Disk Drive Strap Options.

LINE VOLTAGE SELECTION

The Mass Storage Unit line voltage configuration depends on the power option (standard, A1, A2, A3, A4, or A5) that you order. The procedure for selecting the proper voltage is described in the Field Service Manual.