LMMY/UNIBUS INTERFACE

Preliminary Specification

by
Walter A. Wallach

Technical Note No. 88

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Stanford, California

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Abstract

An interface unit to allow communication between the EMMY System bus and a DEC PDP-11 Unibus* is described. The interface consists of three functionally independent elements- an EMMY master/Unibus slave unit, a Unibus master/EMMY slave unit, and a memory management unit.

The EMMY master unit allows the EMMY system to act as bus master on the Unibus. The 32 bit EMMY bus address is truncated for use on the Unibus. The Unibus master unit allows the Unibus to act as master on the EMMY bus. The 18 bit Unibus address is mapped into the 24 bit EMMY address space through the use of one of two techniques. The first utilizes a Page Table consisting of four Page Setup Registers. A CAM is used to associate 2k (16 bit) halfword pages of Unibus address space with 1k (32 bit) word pages of EMMY addess space. The memory management element makes the Page Setup Registers accessible to both system buses as device registers on the Unibus. The second uses a fixed page address and demultiplexor to recognize addresses for translation.

The memory management facility provides mapping of pages in the Unibus address space other than the base page and the upper two pages (which are reserved for use as device registers by Unibus convention). Logical pages may be removed from the Unibus by associating them with the base page or device register area.

The reader is assumed familiar with the EMMY system [1,2], and the DEC PDP-11 Unibus [3].

* - DEC, PDP, and Unibus are the registered trademarks of Digital Equiptment Corporation, Maynard, Massachusetts.

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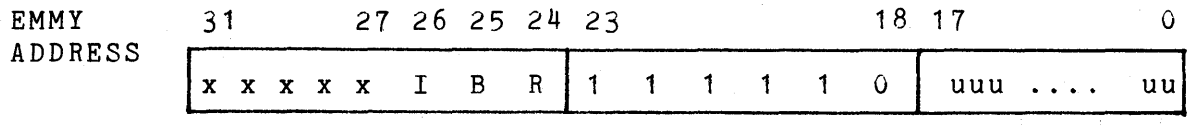
1.0 Introduction

The EMMY/Unibus interface provides a means of communication between the 32-bit EMMY bus system and the 18 bit DEC Unibus r System. Facilities are provided whereby either system may act as master on the other bus and both systems have interrupt capability. The entire address space of each system is available to the other system.

Status of each system is available to the other system through the interface. The EMMY may interrogate any CPU or device register on the Unibus directly through the interface. The DEC PDP-11 provides all status information directly on the bus. The PDP-11 may access EMMY status by reading the microstatus register (file register 0) via the memory management facility, or by reading a status register on the Unibus, which returns the EMMY status information available on the direct status lines (such as Run/Halt, Power, Timeout, etc). Bus conditions such as timeout may or may not be passed between systems, under program control.

2.0 EMMY Master Element

A device on the EMMY bus may communicate with the Unibus through the EMMY Master Element. The EMMY device will issue a 32 bit address as described below:



I - indicates an interrupt is to be isued to the PDP-11
a halfword write must be indicated by B and R
the data indicates the interrupt vector

B - 1 = byte operation for write - ignored for read
this bit corresponds to the C0 control line of the Unibus

R - 1 = write, 0 = read
this bit corresponds to the C1 control line of the Unibus

uuu ... uu the low 18 bits are used as an 18 bit Unibus address

The data portion of the EMMY bus transaction specifies 16 bits of data right justified and zero filled. Two operations must be performed to transfer a 32 bit value.

2.1 EMMY Master Element

2.1.1 Bus Structure

The structures of the two busses differ in certain strategic areas. The Unibus provides seperate data, address, control, and protocol lines. Address space is 18 bits, data words 16 bits. Once a Master has obtained control of the bus, it may hold it as long as it wants. The EMMY bus, on the other hand, multiplexes data and address over the same 32 lines. Protocol is provided to signal presence of data, address, or interrupt vector information.

2.1.2 EMMY Master Transaction

A master on the EMMY bus requests service of the interface by specifying an address with a unit address of F8 (hex). The low 18 bits of the EMMY address (low 2 bits of unit address plus device address) are used as the 18 bit Unibus address. The interface attempts to gain control of the Unibus. If the Unibus is busy (BBSY asserted), REJECT is issued to the EMMY master. Even though the interface may obtain control of the Unibus before the current transaction is complete, the EMMY bus may timeout before the

requested transaction can start.

The EMMY side of the interface must monitor BBSY, NPR, and the BR lines, to determine the status of the Unibus. Care must be taken in designing the EMMY side the prevent race conditions, where the EMMY side fails to obtain the Unibus even though it has sent AACK to the requesting device. It would be best to wait for NPG before returning AACK.

Once the Unibus has been obtained (through the use of a DEC M7821 Interrupt Control Module and M796 Bus Master Control Module), the Unibus address and control portions of the EMMY address are latched and AACK asserted. This frees the EMMY Bus to transfer data. For write operations, the low 16 bits of the EMMY bus are gated to the 16 Unibus data lines when DSIG is recieved, and START signalled to the M796. When END CYCLE is signalled by the M796, DACK is asserted and the write is complete. If the Unibus protocol causes timing problems for the EMMY bus address and data can be latched and the EMMY bus released before the bus transaction is completed.

For read operations, the Unibus address and control are passed to the Unibus and START signalled to the M796. When SSYN is recieved, indicating the Unibus slave has completed its transaction, DATA WAIT will go low, strobing data onto the EMMY bus and asserting DSIG. When DACK is recieved, DATA ACCEPTED is asserted, releasng the Unibus. Data can also be be latched and the Unibus released as soon as data becomes available.

If the Unibus times out during an interface transaction, this condition will be passed to the EMMY system as an interrupt. The interrupt vector will be chosen later.

2.2 Interrupts of the PDP-11 System

An interrupt of the PDP-11 System is specified by addressing any location with the interface unit address and setting bit 26 of the EMMY address. The interface obtains control of the Unibus via the M7821 Interrupt Control Module by asserting INTR and INTR ENB lines. This makes a bus request on the BR level. When the bus has been obtained, MASTER is asserted by the M7821. The interface then asserts AACK to the EMMY bus and waits for DSIG. The low 16 bits of data are placed on the Unibus data lines and INTR START asserted to the VECTOR ADDRESS portion of the M7821. INTR DONE will be recieved when the transaction is completed. DACK may then be asserted and both buses released. Again, data may be latched and the EMMY bus released before INTR DONE is recieved.

3.0 Memory Management Facility

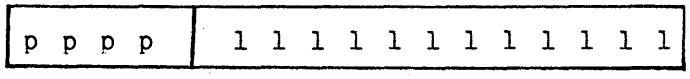
The EMMY Slave Element provides the Unibus with a means of addressing the EMMY system. Since the Unibus provides only 16 bits of processor address space, a Page Table is provided to translate Unibus references to EMMY references.

The 32K halfword address space of the Unibus is partitioned into 3 regions. The upper 4K is reserved by DEC convention for device and processor registers. The lower 8K is occupied by core memory supplied with the PDP-11/10 processor. The 20K region in between is available for mapping into the EMMY address space.

Two schemes have been developed for translating 16-bit Unibus addresses into 32 bit EMMY bus addresses. One utilizes a content-addressable memory (CAM) to associate one of 4 2K halfword Unibus pages with a 1K word EMMY page. Ten such Unibus pages are available. The other partitions the available Unibus address space into 5 fixed 4K halfword pages.

3.1 CAM-Based Memory Management Facility

The CAM-based system maps 4 pages of 2K (16 bit) halfwords of Unibus address space into 4 pages of 1K (32 bit) words of EMMY address space. Both Unibus and EMMY page addresses may be specified under program control from either system. A CAM is used to associate Unibus page addresses with EMMY pages.



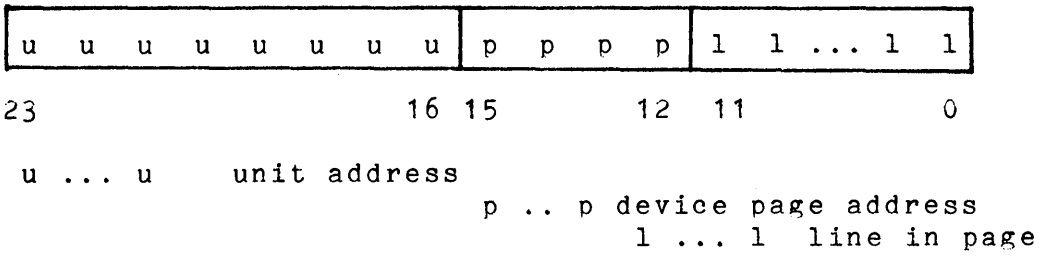
Unibus Address

p p p p indicates a 2K halfword Unibus page

1 1 ... 1 1 indicates line in page

Pages 1110 and 1111 and the base page are not recognized for translation, since the base page is always present and the upper 4K halfwords are reserved by Unibus convention for device

registers.



3.1.1 Page Setup Registers - Page Table

A Page Table of 4 16-bit setup registers is provided, addressable as Unibus device registers. The low 12 bits specify a 12 bit EMMY page address, ie a unit address and 4 bit device page address. The high 4 bits specify the Unibus page address to be associated with this EMMY page. Each Unibus page consists of 2K 16-bit halfwords. The low 12 bits of the Unibus address are used to complete the EMMY address by concatenation.

These Page Registers are independent of the rest of the interface and may be addressed from the EMMY side through the interface.

A Page Setup Register is loaded by writing a 16 bit halfword to the proper Unibus address. The page table will occupy four contiguous words in the user device register area. The high 4 bits are placed in a 4-bit CAM and low 12 bits placed in the proper EMMY-address setup register.

3.1.2 EMMY Address Completion

The translation process proceeds as follows:

when a Unibus address is displayed such that Unibus A(15:12) match a Unibus page address specified in the Page Table, the Unibus address is recognized. (Addresses within the base page or the upper 4K halfwords are not recognized for translation. A port may be logically removed from the system by setting its Unibus page address to the base page or one of the upper 2 pages). The 12 bits of the associated EMMY page address are concatenated on the low side with the low 12 bits of the Unibus address to form an effective EMMY address.

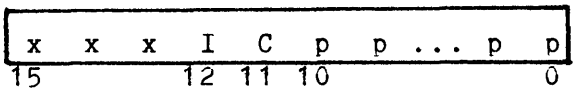
If an already existant page is associated with an EMMY address, two devices will respond and results are unpredictable.

The 32 bit EMMY bus address is completed by concatenating an 8 bit control field on the high side. The control field normally indicates right justified data and odd parity. Bit 24 (read/write) is gated directly from Unibus C1.

3.2 Fixed-Page Memory Management Facility

The fixed page scheme uses Unibus A(15:13) to drive the translation hardware. A demultiplexor determines if the referenced page is within the available address space (pages other than the low 8K and high 4K halfwords). Pages 2 through 5 cause one of 4 16 bit setup registers to be read out.

The high 5 bits contain flags which control the translation process. These include inhibit and control byte completion information. If the setup register indicated translation is to proceed, the low 11 bits are concatenated on the low side with the low 13 bits of the Unibus address, forming a 24 bit EMMY address. The 8 bit control field is completed either by default for halfword/byte transfer (as specified by Unibus C(1:0)), or by setup register (for maintainance purposes). The interface does not respond to pages where the inhibit bit is set.



Setup Register
Flags

x x x - unspecified
I-Inhibit 0=translate this page reference
1=inhibit response to this page

C-Control Byte
0=generate MMC byte by default
1=MMC byte specified by setup register

pp...pp- high 11 bits of 24 bit EMMY address

3.3 Halfword Ports

Three of the Page Setup Registers specify halfword/byte ports into the EMMY system. These ports use common logic to transfer 16 bit halfwords and 8 bit bytes between the two systems under Unibus control. Address specification reflects 2 byte or 1 byte transfer for write (C0 gated directly from Unibus) and 2 byte transfer always indicated for read. When byte data is to be written to the EMMY system (Bus C(1:0) = 11), the appropriate byte is gated to the low side (bits 7:0) of the EMMY bus (data is right justified). These ports are intended to communicate with the EMMY main storage system.

MMC Byte (halfword port)	Read	Write
	1 0 1 1 0 0 0 0	1 b 1 1 0 0 0 1

b - indicated by Unibus C0 -
1=byte transfer

3.3.1 Halfword Transaction

When a location associated with the halfword port is accessed by a Unibus master, the interface responds and completes the EMMY system address. The EMMY bus is obtained and the address

displayed along with ASIG when MSYN is recieved.

If the operation is a halfword write, after MSYN is recieved, data is latched and SSYN returned to the Unibus. Data is placed on the low 16 bits of the EMMY bus and DSIG asserted. When DACK is recieved, the transaction is completed.

If the operation is a read, when DSIG is recieved the low 16 bits of the EMMY bus are latched and gated to the Unibus data lines. DACK and SSYN are asserted to their respective buses. This completes the slave's responsibility in the transfer. The EMMY bus is freed.

3.4 Word Port

One Page Setup Register specifies a word port into the EMMY bus system. Halfwords from the Unibus are buffered to 32 bits before transfer to or from the EMMY system. This is intended primarily as a means to access the EMMY Control Store and Register file, but may address any location on the EMMY bus.

3.4.1 Read Request

Address recognition preceeds as for the halfword ports. When a read request is made to an even halfword associated with the word port, 32 bits are read out of the translated EMMY bus location. The low 16 bits are placed on the Unibus data lines and the high 16 bits latched. When a read request for an odd halfword associated with the word port is made, the contents of the latch are placed on the Unibus data lines. The read of the EMMY system is made by shifting the translated EMMY address right by 2 bits to form a word address and concatenating an MMC byte of zeros (read 4 bytes on a word address).

To properly read a word of EMMY storage, an even/odd halfword pair must be read in ascending order by the Unibus device.

3.4.2 Write Request

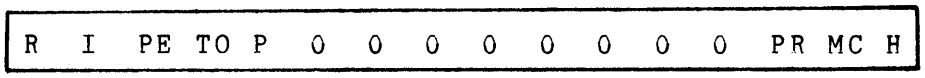
When a write request is made to an even halfword associated with the word port, the data on the Unibus data lines is latched. When a write request for an odd halfword is recognized, the translated EMMY address is shifted right 2 bits, an MMC byte of 00000001 concatenated on the left to complete the EMMY address. Data on the Unibus data lines is concatenated on the left with latched data and used as the 32 bit EMMY data value. To properly

write a word of EMMY storage, an even/odd halfword pair must be written in ascending order.

3.5 Bus Status

A Unibus register location is provided which returns status information for the EMMY system. A read of this register returns the EMMY direct sense lines. A write of this register sets the EMMY direct control lines.

The EMMY can access any status information on the Unibus directly.



R - run/halt indicator 1=halted
I - EMMY interrupts enabled (=1)
PE - parity error
TO - EMMY bus timeout
P - EMMY powered up (=1)
PR - parity reset
MC -master clear
H -halt

Status Control

EMMY Status Register

3.6 Interrupts of the EMMY

The Unibus may interrupt the EMMY CPU by writing an interrupt vector to an Interrupt register. When this register is addressed, the interface obtains control of the EMMY bus and gates the data lines to the low 16 bits of the EMMY bus and asserts ISIG.

4.0 Implementation Notes

DEC provides modules which handle the Unibus protocols in obtaining Master status and controlling DMA transfers. (M796 and M7821). The M7821 provides bus mastership for both DMA (through NPR) and Interrupt (through BR). The protocols for slave devices are straightforeward and an M105 Address Selector will be used to access the Page Table and Registers. A modified M105 may be used to respond to virtual Unibus addresses. Bus buffering will be accomplished through an M785 Transciever Module.

An EMMY bus arbiter has been developed and will be used on the EMMY side. The interface must have high priority on the EMMY

bus, since all disk transfers will use the interface.

A trivial Unibus arbiter will be included in the interface unit. Initially, the only devices competing for control on the Unibus will be the disk controller and the interface. When the disk requests use of the interface, it will have priority over the EMMY (the EMMY will already be aware that the disk is busy, since it is the only device which will initiate disk operations). The arbiter will function by returning request signals on grant lines. This will allow the disk and interface to be used prior to delivery of the PDP-11 CPU.

5.0 Acknowlegement

The author wishes to thank Ronald Crane and David Lu for assistance in understanding the PDP-11 system, and Charles Neuhauser and Michael Fung for suggestions and comments on the various translation schemes.

References

1. Neuhauser, Charles, An Emulation Oriented, Dynamic Microprogrammable Processor (Version 3), TN 65, October 1975, Digital Systems Lab, Stanford University, Stanford, California 94305.

2. Neuhauser, Charles, EMMY System Peripherals, TN 77, December 1975, Digital Systems Lab, Stanford University, Stanford, California 94305.

3. Digital Equiptment Corporation, PDP11 Peripherals Handbook, Digital Equiptment Corporation, Maynard, Massachusetts 01754.

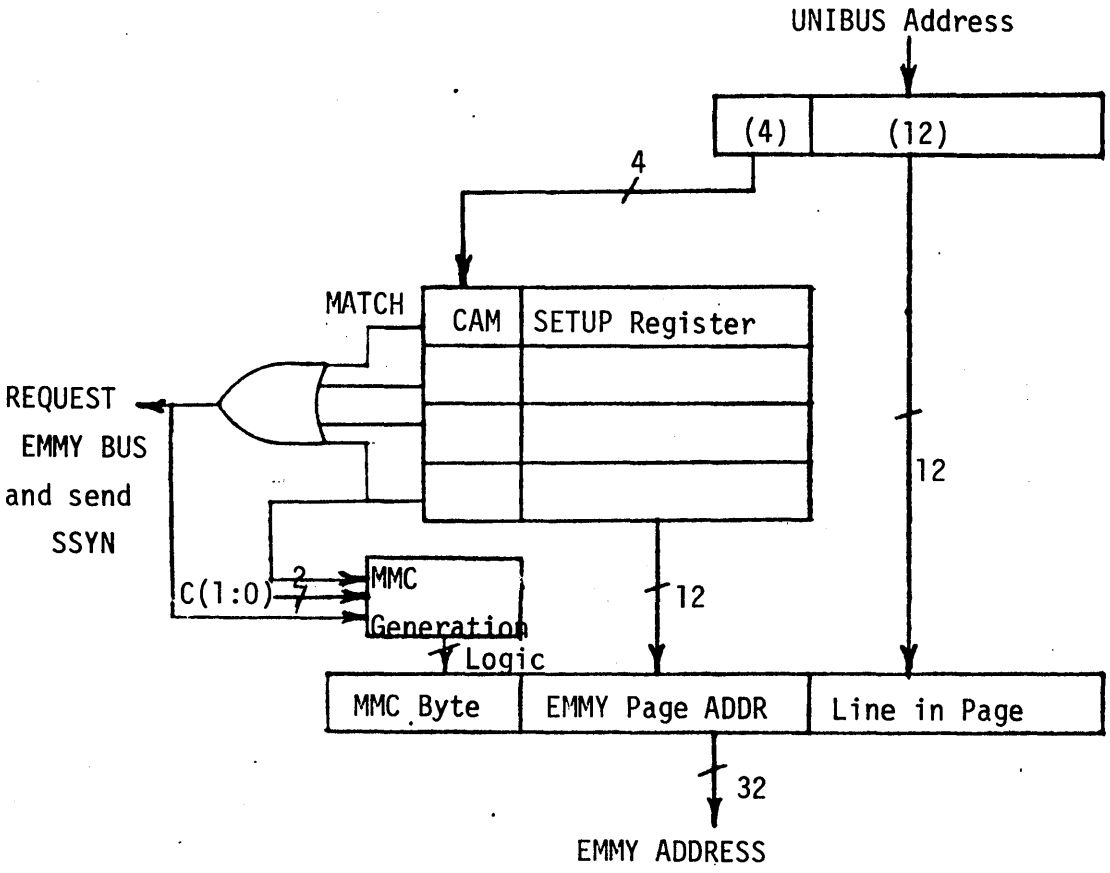


Figure 1 CAM-Based Memory Management Facility

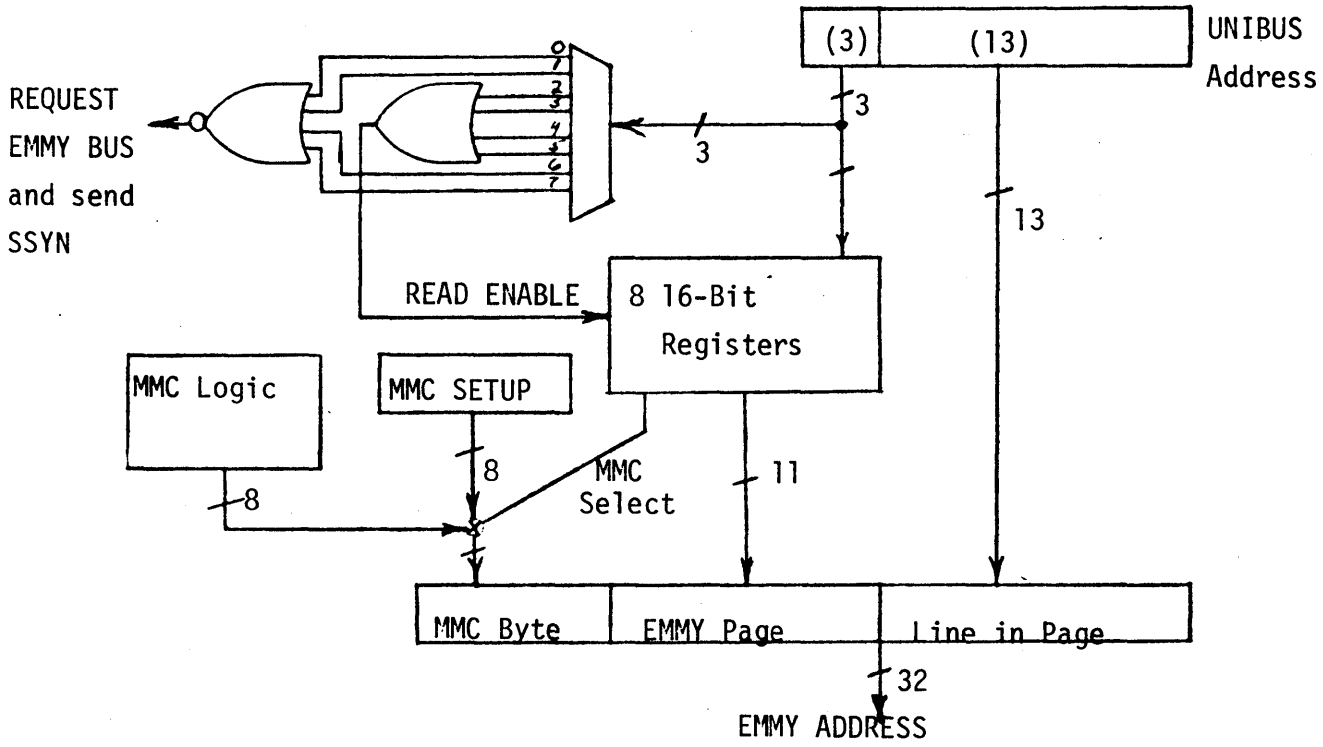


Figure 2 Fixed-Page Memory Management Facility

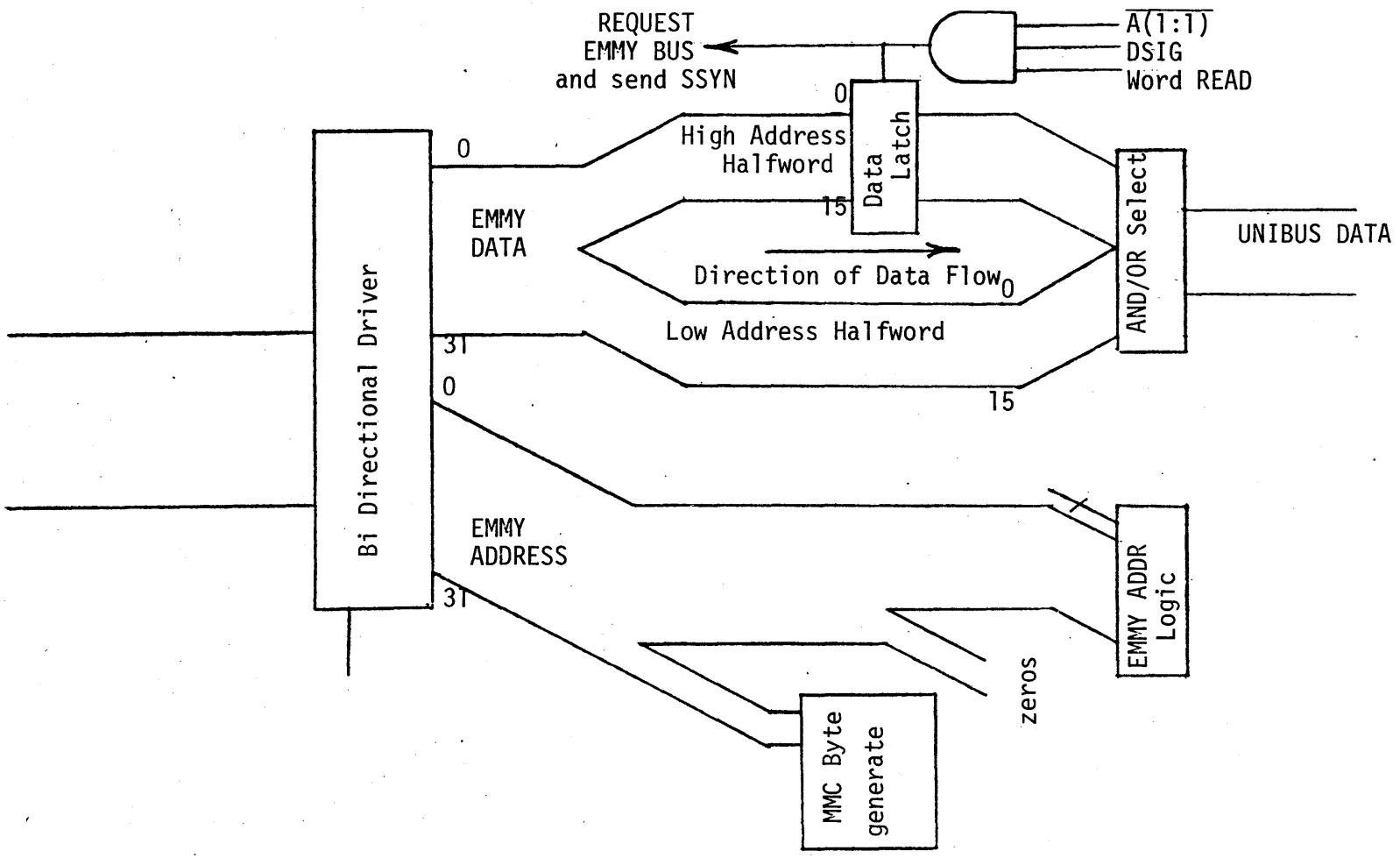


Figure 3 Word Read Data Flow

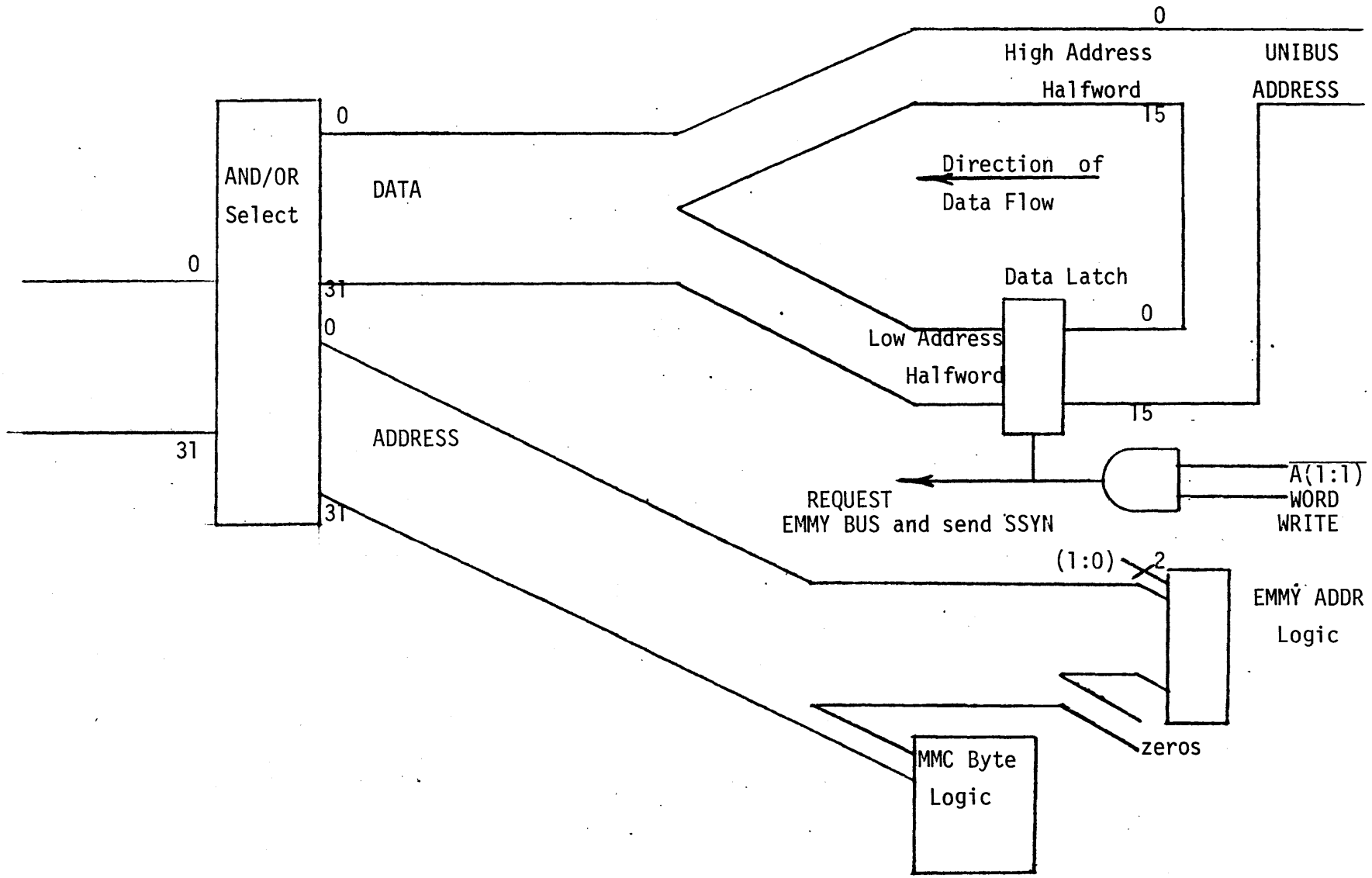


Figure 4 Word Write Data Flow