

IOP  
MINIFLOW  
INSTRUCTIONS



(with control fields)

|                      |                                  | Bit Positions |           |   |   |   |   |   |   |           |                      |                  |             |   |   |   |   |   |   |         |   |   |   |      |
|----------------------|----------------------------------|---------------|-----------|---|---|---|---|---|---|-----------|----------------------|------------------|-------------|---|---|---|---|---|---|---------|---|---|---|------|
|                      |                                  | 0             | 1         | 2 | 3 | 4 | 5 | 6 | 7 | 8         | 9                    | 0                | 1           | 1 | 1 | 1 | 1 | 1 | 1 | 1       |   |   |   |      |
| Engine Class         | Immediate Operand                | 0             |           |   |   |   |   |   |   |           | Immediate Data Field |                  |             |   |   |   |   |   |   |         |   |   |   |      |
|                      | Scratch Memory Operand           | 1             | O         | P | S |   |   |   |   | 0         | 0                    | T                | R           | L | E |   |   |   |   | SM Addr |   |   |   |      |
| Single Operand Class | One's Complement of the AC       | 1             | 0         | 1 | 1 |   | A | C |   | 0         | 0                    | [Hatched]        |             |   |   |   |   |   |   |         |   |   |   |      |
|                      | Shift the AC                     | 1             | 0         | 0 | D |   |   |   | 1 | 0         | [Hatched]            |                  |             |   |   |   |   |   |   |         |   |   |   |      |
|                      | Rotate AC1 and AC2 Left          | 1             | 0         | 1 | 0 | 0 | 0 |   | 1 | 0         |                      | C                | Shift Count |   |   |   |   |   |   |         |   |   |   |      |
|                      | Normalize AC1 Left               | 1             | 0         | 1 | 0 | 0 | 1 |   | 1 | 0         | [Hatched]            |                  |             |   |   |   |   |   |   |         |   |   |   |      |
| Transfer Class       | Transfer Direct                  | 1             |           |   |   |   |   |   |   | 0         | 1                    | Transfer Address |             |   |   |   |   |   |   |         |   |   |   |      |
|                      | Transfer Indirect                | 1             | T         | V | P |   | T | Y | 1 | 1         | 0                    | [Hatched]        |             |   |   |   |   |   |   |         |   |   |   |      |
|                      | Transfer on Target PRI & DIR Reg | 1             | [Hatched] |   |   |   |   |   |   | 1         | 1                    | 1                | SM Addr     |   |   |   |   |   |   |         |   |   |   |      |
| Control Class        | Halt IOP MINIFLOW                | 1             | 1         | 0 | 1 | 0 | 0 | 1 | 0 | [Hatched] |                      |                  |             |   |   |   |   |   |   |         |   |   |   |      |
|                      | Unhang CPU Level 4 MINIFLOW      | 1             | 1         | 0 | 1 | 0 | 0 | 1 | 0 |           | R                    |                  | E           |   |   |   |   |   | 0 | 0       | 0 | 0 |   |      |
|                      | Set CPU Trap Request             | 1             | 1         | 0 | 1 | 0 | 0 | 1 | 0 |           |                      |                  |             |   |   |   |   |   |   |         | 0 | 0 | 1 | 0    |
| Data Access Class    | Store AC to Scratch Memory       | 1             | 1         | 0 | 1 | A | C |   | 1 | 0         | [Hatched]            |                  |             |   |   |   |   |   |   |         |   |   |   |      |
|                      | Access General Register Direct   | 1             | 1         | 0 | 0 | 1 | 1 | 1 | 0 |           | M                    |                  | 0           |   |   |   |   |   |   |         |   |   | R | Addr |
|                      | Access General Register Indirect | 1             | 1         | 0 | 0 | 1 | 1 | 1 | 0 |           |                      | R                |             | 1 |   |   |   |   |   |         |   |   |   |      |
|                      | Read Main Memory Indirect        | 1             | 1         | 0 | 0 | 0 | 0 | 1 | 0 | 1         |                      |                  | R           |   | B | R |   |   |   |         |   |   |   |      |
|                      | Write Main Memory Indirect       | 1             | 1         | 0 | 0 | 0 | 0 | 1 | 0 | 0         | [Hatched]            |                  |             |   |   |   |   |   |   |         |   |   |   |      |
|                      | Access IOP Memory Indirect       | 1             | 1         | 1 |   |   | 1 | 0 | 1 | 0         | [Hatched]            |                  |             |   |   |   |   |   |   |         |   |   |   |      |
|                      | IOP, CPU, Channel Memory Direct  | 1             | 1         | 1 | M |   | M | U | 1 | 0         | Memory Address       |                  |             |   |   |   |   |   |   |         |   |   |   |      |

|  |  |  |  |  |
|--|--|--|--|--|
| <b>AC</b><br>00 All 3<br>01 AC1<br>10 AC2<br>11 AC3  | <b>OP</b><br>00 Add<br>01 And<br>10 Or<br>11 Pass  | <b>L</b><br>0 No Link<br>1 Link Carry in and Zero Test               | <b>S</b><br>0 Test Only<br>1 Load & Test | <b>T</b><br>0 Set Engine PRI's<br>1 Set Target PRI's |
| <b>TY</b><br>00 Transfer or Continue<br>01 Call or Continue<br>10 Transfer or Return<br>11 Transfer or Exit  | <b>TV</b><br>00 Always False<br>01 Carry False<br>10 Zero<br>11 CF or Zero   | <b>C</b><br>0 Use Shift Count Field<br>1 Use Shift Register Contents | <b>D</b><br>0 Left<br>1 Right            | <b>E</b><br>0 Continue<br>1 Exit                     |
| <b>MU</b><br>*00 Active CPU Control Core<br>01 IOP Control Core<br>*11 Channel Registers or IOP Control Core if addr. > 77<br>* Active Channel Ptr ORed with bits 16 & 17 of Addr. | <b>BR</b><br>00 AC1-2 Only<br>01 AC1-2 & DR 7-13, 18-35<br>10 AC1-2 & DR 0-6, 14-17<br>11 AC1-2 & Directive Register | <b>P</b><br>0 Transfer if False<br>1 Transfer if True                | <b>R</b><br>0 Continue<br>1 Return       | <b>M</b><br>0 Write<br>1 Read                        |

## SCRATCH MEMORY ASSIGNMENTS

| <u>OCTAL ADDRESS</u> | <u>LENGTH</u> | <u>WRITE DATA PATH</u> | <u>USE-DESCRIPTION-REMARK</u>                                  |
|----------------------|---------------|------------------------|--|
| 00                   | 18            | YES                    | target location counter (sched. increments by 1)               |
| 01                   | 18            | YES                    | general purpose  |
| 02                   | 18            | YES                    | general purpose  |
| 03                   | 18            | YES                    | general purpose  |
| 04                   | 7             | YES                    | shift counter (bit 11 replicated into 0-10 on read)            |
| 05                   | 3             | ONLY                   | active channel (bits 16-17) & active CPU (bit 15)              |
| 06                   | 2             | YES                    | target CF (bit 16) and zero (bit 17) indicators                |
| 07                   | 18            |                        | AC 3   |
| 10                   | 18            | YES                    | general purpose  |
| 11                   | 18            | YES                    | general purpose  |
| 12                   | 18            | YES                    | general purpose  |
| 13                   | 18            | YES                    | general purpose  |
| 14 to 17             | 0             |                        | AC Decode Options  |
| 20                   | 7             |                        | directive reg 0-6  |
| 21                   | 3             |                        | directive reg 7-9 (CF set on fetch if bit 7 is one)            |
| 22                   | 4             |                        | directive reg 10-13 (zero set on fetch is <u>not</u> all zero) |
| 23                   | 4             |                        | directive reg 14-17  |
| 24                   | 6             |                        | directive reg 18-23  |
| 25                   | 6             |                        | directive reg 24-29  |
| 26                   | 6             |                        | directive reg 30-35  |
| 27                   | 18            | YES                    | directive reg 18-35  |
| 30                   | 0             |                        | may be read as all zero's                                      |
| 31                   | 1             |                        | may be read as constant of one                                 |
| 32 to 37             | 0             |                        | spare  |

All fields read in right justified (to bit 17) and fill with leading zeros if not 18 bits long (except SM4 fills with 'sign', i.e. bit 11).